IBM Maintenance Library

SYSTEM/32 Theory—Diagrams

SY31-0346-4

INTR | CPU | CHAN | μIRPT | μINSTR | IMPL | ERR HDL | CNSL | DISK | 33FD | PTR | DISP | KBD | S-PTR

PREFACE

This manual contains theory information and diagrams for IBM System/32.

Other manuals to be used with this one are:

- *IBM System/32 Operator's Guide,* GC21-7591
- *IBM System/32 Functions Reference Manual,* GC21-9176

For maintenance information including checks, adjustments, removals, and replacements, see *IBM System/32 Maintenance Library, Introduction and Maintenance,* SY31-0373.

In addition, refer to the *IBM System/32 Diagnostic User's Guide* for further information on system diagnostics.

Fifth Edition (May 1977)

•This is a major revision of, and obsoletes, SY31-0346-3. This edition adds theory and diagrams for the 285 line-per-minute belt printer, and 120 cps serial printer, and the 120 cps compatible printer attachments. All other changes are indicated by a vertical line at the left of the change. Changes are periodically made to the information herein; any such change will be reported in subsequent revisions or technical newsletters.

A Reader's Comment Form is at the back of this publication. If the form is gone, address your comments to IBM Corporation, Publications, Department 245, Rochester, Minnesota 55901.

Contents

LIST OF ABBREVIATIONS

μINSTR	micro instruction
μIRPT	microinterrupt
Adr	address
AGC	automatic gain control
ALU	arithmetic/logical unit
AM	address mark
ASCII	American National Standard Code for Information Interchange
BC	byte control
BFR	buffer
BH	behind home
BI	bidirectional
BP	belt position
BPC	block processor clock
BPC	belt position counter
BR	bit ring
BSCA	binary synchronous communications adapter
C	clock pause
CBI	command bus in
CBO	command bus out
Chan	channel
CPS	characters per second
CPU	processing unit
CRC	cyclic redundancy check
CRT	cathode ray tube
CS	control storage
CS	cycle steal
CSILSW	control storage interrupt level status word
cmd	command
cnt	count
ctrl	control
ctr	counter
DAR	display address register
DBI	data bus in
DBO	data bus out
DCD	decode
DCP	diagnostic control program
DE	disk enclosure
demod	demodulator
diag	diagram
DLY	delay
ECC	emitter column counter
EOF	end of forms
ERAP	error recording and analysis procedure
FD	disk drive
FET	field effect transistor
GB	guard band
gen	generate/generator
hmr	hammer
Hz	Hertz
I/O	input/output
ID	identification
IMPL	initial microprogram load
IOB	input/output block
KANA	Katakana
KYB	keyboard
KYBD	keyboard
LM	left margin
LSR	local storage register
Lth	latch
LZ	landing zone
MAB	micro address backup register
MAR	memory address register
	microaddress register
MCI	machine check interrupt
MCU	Mag Card Unit
mega	million
MFM	modified frequency modulation
MOD	modifier
MOR	micro operation register
mtr	motor
op	operation
OSC	oscillator
P	position pulse
PC	parity check
PCR	processor condition register
PFN	print fire number
PG	parity generate
Ph	polarity hold
PLO	phase lock oscillator
POR	power on reset
PP	parity predict
PP	print position
prt	print
PSS	print sub scan
ptr	printer
RAM	random access memory
rd	read
reg	register
RIB	request indicator byte
ROS	read only storage
SAR	storage address register
SBAR	storage buffer address register
SC	sequence counter
SCP	system control program
SDLC	system data link control
sel	select/selector
SERDES	serializer/deserializer
sns	sense
stg	storage
svc	supervisor call
SWG	start write gap
sync	synchronize
S3ILSW	system interrupt level status word
tr	trigger
TRA	trigger A
TRC	trigger C
TRD	trigger D
TRE	trigger E
TRF	trigger F
UNI	unidirectional
vert	vertical
VFL	velocity follow latch
VFO	variable frequency oscillator
WC	worst case
WR	(N) H or L = work register (N) high or low
WR	work register
WTC	World Trade Corp.
Xfer	Transfer

MICRO INSTRUCTION ABBREVIATIONS

ACYR	add registers with carry
AI	add immediate
AR	add registers
B	branch
BAL	branch and link
CI	compare immediate
DEC	decrement register by 1
HBN	hex branch numeric
HBZ	hex branch zone
IOCL	I/O control load
IOCS	I/O control sense
IOL	I/O load
IOS	I/O sense
INC	increment register by 1
JC	branch on condition
JCY	branch on carry
JE	branch on equal
JFLG	branch on flag
JH	branch on high
JIO	branch on I/O condition
JL	branch on low
JM	branch on mixed
JN	branch on negative
JNE	branch not equal
JNH	branch not high
JNL	branch not low
JNN	branch not negative
JNP	branch not positive
JO	branch all ones
JP	branch on positive
JSR	branch service request
JNZ	branch not zero
JZ	branch on zero
L	load direct to control storage
LA1	logical/arithmetic 1
LA2	logical/arithmetic 2
LC	load from control storage
LI	load immediate
LM	load from main storage
LSAR	load/sense address register
MPL	microprocessor load
MPLF	microprocessor load for special functions
MPS	microprocessor sense
MVR	move LSR
MZN	move zone to numeric
MZZ	move zone to zone
NCR	AND complement
OCR	OR complement
RDCH/L	I/O store to control storage high/low
RDM	I/O store to main storage
RETRN	return
SBF	set bits off
SBN	set bits on
SCYR	subtract with borrow
SI	subtract immediate
SILSB	sense interrupt level status byte
SLL	shift left logical
SLLD	shift left logical double
SR	subtract registers
SRL	shift right logical
SRLD	shift right logical double
ST	store direct to control storage
STC	store to control storage
STM	store to main storage
TM	test mask
WTCH/L	I/O load from/to control storage high/low
WTM	I/O load from/to main storage
XR	exclusive OR

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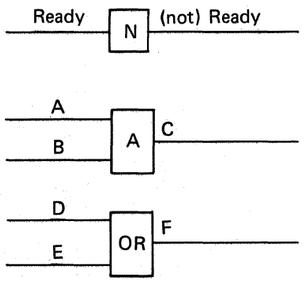
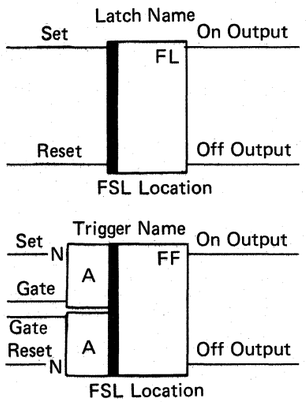
Legend

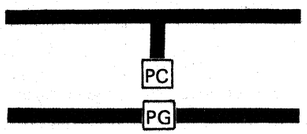


Negator inverts logic on positive logic diagrams.

A and B must be active for C to be active.

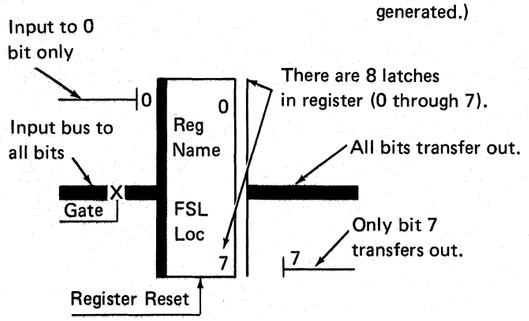
D or E active causes F to be active.

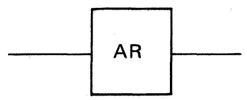




Parity Check on Bus Line

Parity Generator (Correct parity is generated.)

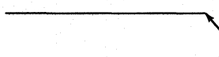




Amplifier

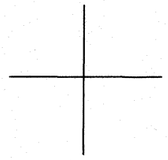
On-Page Connector

On-Page Connector

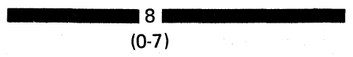


A note is shown this way on a diagram.

Joining Lines



Lines cross over but do not join.

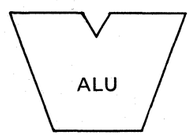


8 lines on bus bits 0, 1, 2, 3, 4, 5, 6 and 7

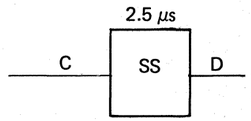
Boolean Algebra Symbols

- ● In a line name means AND
- \+ In a line name means OR

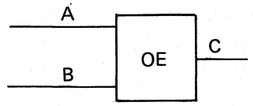
(xx - - - x) Indicates a line name that does not exist as an actual FSL name, but used to better explain the function of a line or block



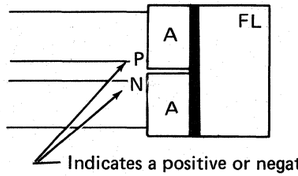
Arithmetic Logic Unit (located in the CPU)



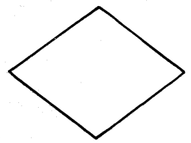
A shift on C causes a 2.5 μs shift on D.



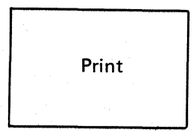
Exclusive OR. Either A or B must be active for C to be active, but if both are active or neither active, C will be inactive.



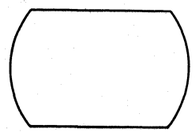
Indicates a positive or negative shift is required after the gate pulse is present.



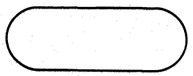
Decision Block on a Flowchart (asks a question)



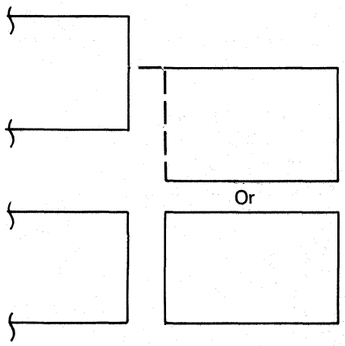
Processing block on a flowchart



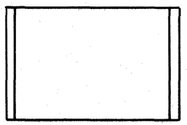
Keying Operation on Flowchart



Terminal on a flowchart

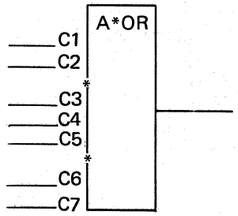


Note on a Flowchart



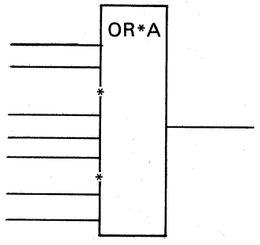
Refers to another Flowchart

Legend

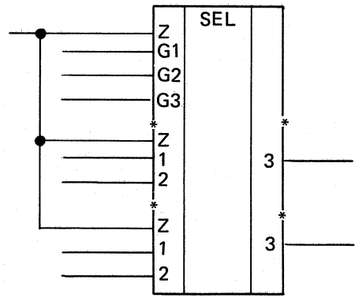


In this example three AND blocks feed an OR block. The three AND block functions are separated by asterisks.

The asterisk is a delimiter and separates groups of inputs



This is an example of three OR blocks feeding an AND block. The three OR block functions are separated by asterisks.



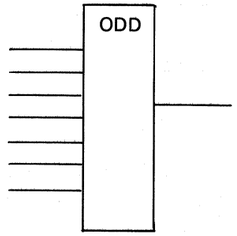
The selector block is a gating device. The upper section of the block contains the gates (G) and the lower section contains the gated data lines.

In this example gate 1 and gate 2 each control a set of input data lines.

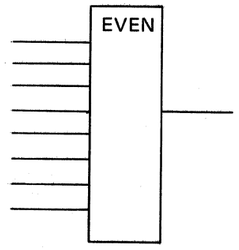
Gate 3 controls both output lines.

Thus for data to pass through this block, it is necessary that one of the input gates (G1 or G2) be active, and the output gate (G3) must also be active.

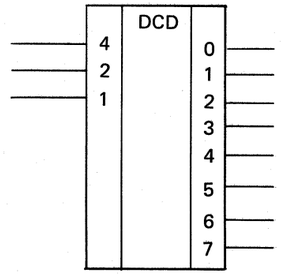
This example of the selector also contains Z inputs. A Z input is used when a line is common to a number of functions. Thus if the input to Z is active and G3 is active, both output lines will be active.



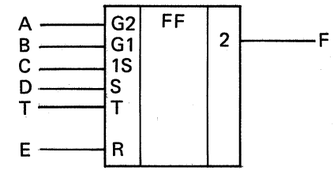
The output of the odd count block is active only when an odd number of inputs are active.



The output of the even count block is active when an even number of inputs are active.

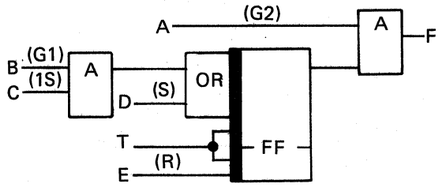


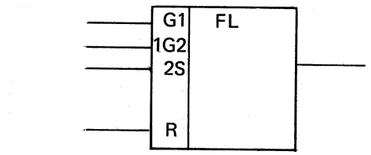
The decode translates a group of related inputs into a specific output. The inputs are numbered in binary progression; 1, 2, 4, 8 and so on. The number on the output equals the sum of the active inputs. For example, when the inputs to 4 and 1 are active, the 5 output will be active.



The FF trigger can be set with the S input and reset with the R input. A T (toggle) input can also be used to complement the current status of the trigger.

In this example there are 2 sets and 1 reset. The second set requires that gate 1 along with the input to 1S be active to turn the trigger on. Also in this example, gate 2 must be active to get an active output.



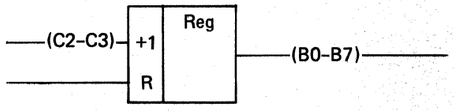


In this example of a flip latch, G is a gate used to gate other signals. Gate 1 (G1) must be active along with the input to gate 2 (G2) for gate 2 to become active.

The latch will turn on if gate 2 is active and the input to 2S becomes active.

When the R line is activated, the register will be reset.

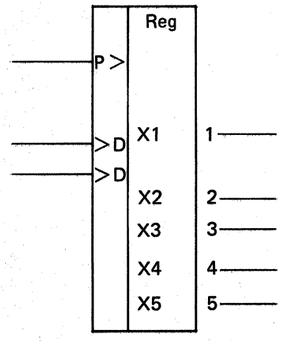
Legend



This example of a register illustrates bundled lines on both the input and output. The input contains 2 lines, C2 and C3, and an output that contains 8 lines, B0 through B7.

The + symbol indicates the register will be incremented by 1 when the input line becomes active. A minus symbol would indicate decrementing. The number following the + or – symbol indicates the amount of incrementing or decrementing.

When the R line is activated, the register will be reset.



This is an example of a shift register. The symbol > indicates shift down while < would indicate shift up. In order to shift down by 1, the input to one of the > lines must be active and a shift must occur on the P> input.

The positions in the register are denoted by X1, X2, X3, and so on.

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Introduction to IBM System/32

The IBM System/32 is a desk-sized business system with the following features:

- Programs are written in system language and executed by a machine language microprogram.
- Large storage capacity is provided by disk drive.
- Operating instructions and prompting messages are displayed.
- I/O and CPU errors are recorded and can be retrieved.
- Diagnostic programs are automatically run after the initial microprogram load.
- Whenever possible, conditions that caused errors are automatically retried.

The CPU contains 16K, 24K, or 32K addressable positions of main storage and 4K or 8K addressable positions of control storage. Each position of main storage is one byte wide; each position of control storage is two bytes wide. FET technology is used for both main and control storage. The CPU also contains registers, gates, and ALUs that are controlled by the microprogram.

The disk drive is an integrated disk that provides 3.2, 5.0, 9.1, or 13.7 million bytes of accessible storage. In addition, various diagnostic programs reside on the disk.

The CE control panel contains lights and switches used in the maintenance of the system.

The display screen is used for operator prompting, job output, and other messages. Up to six lines of 40 characters-per-line can be displayed at one time.

The keyboard is used to control various system functions and as a data input device.

The IBM System/32 can be ordered with either the serial printer or the belt printer.

The serial printer has 132 print positions and uses a 64 character set. It is a 7 X 7 wire matrix printer. The serial printer has 132 print positions and uses a 64 character set. It is a 7 X 7 wire matrix printer. The serial printer is available in three models:

120 cps (characters per second) bidirectional
80 cps bidirectional
40 cps bidirectional
40 cps unidirectional

The two models of the 40 cps printer are identical. The attachment circuitry controls whether they print only left to right or in both directions.

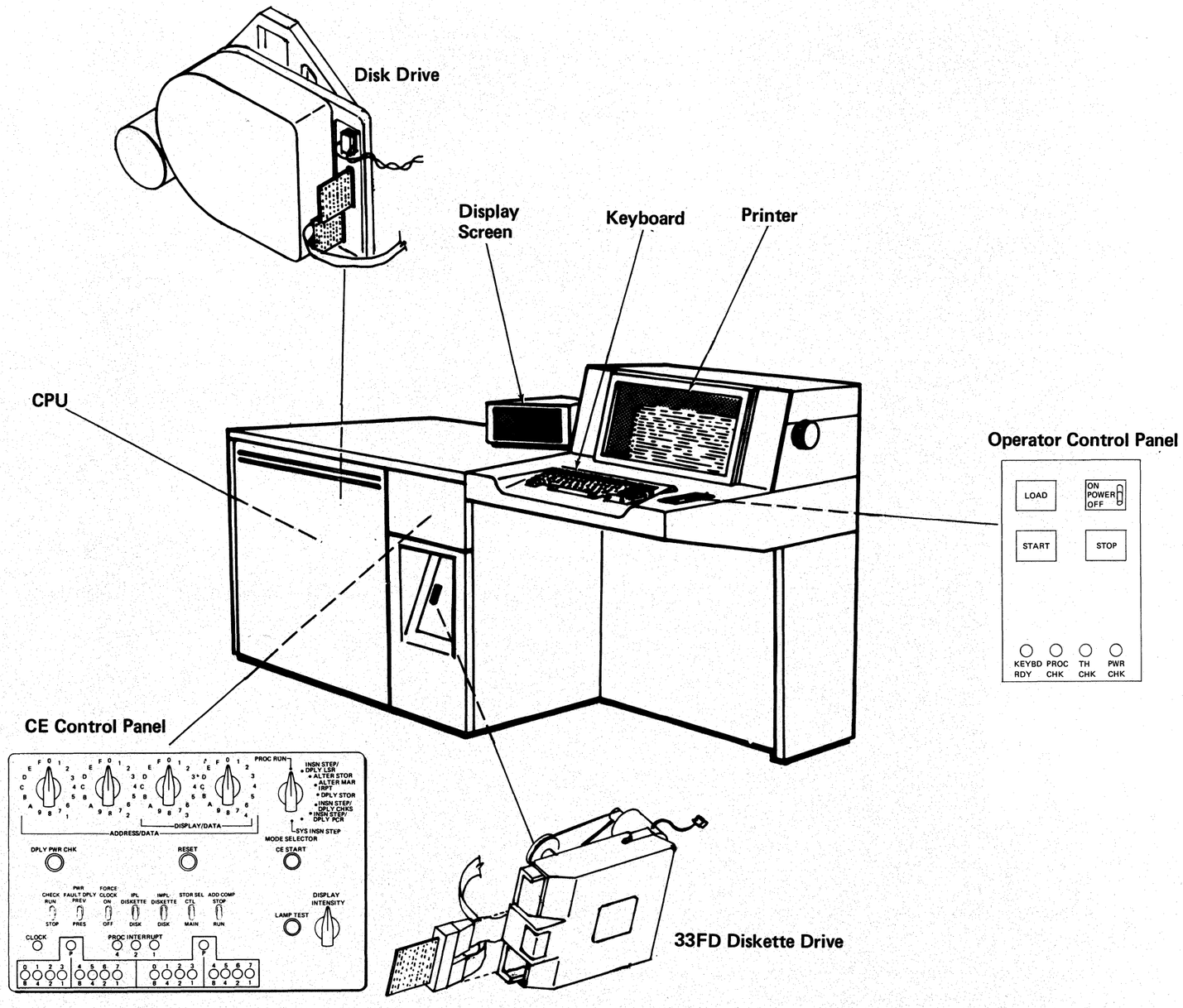
The belt printer has 132 print positions and a 48, 64, or 96 character set. The printing speed is 50, 100, 155, or 285 lines per minute with a 48 character set.

The operator control panel has switches to turn power off and on, start the loading of the diagnostic programs and control program, and start and stop the execution of system level instructions. Keyboard ready, processor check, thermal check, and power check lights are also included.

The 33FD diskette drive uses IBM diskettes as input and output to the system. Data can be entered on the diskettes by key entry devices such as the IBM 3740 Data Entry System. In addition, certain diagnostic programs reside on the diskettes.

All the functions performed by the system are controlled by a microprogram which must be loaded into control storage before any processing can begin. This loading (initial microprogram load) is done from either the disk drive or the 33FD (CE only).

The microprogram processes system instructions, data in storage, and channel operations. The microprogram is composed of microroutines of varying sizes, each having a specific task to perform. Each microroutine is composed of bit-significant instructions that, in effect, are machine language instructions.



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CPU Functional Units

Main Storage

Main storage contains 16K, 24K, or 32K addressable positions; each position is 1 byte wide.

Control Storage

Control storage contains 4K addressable positions (8K positions on machines with the Control Storage Increment Feature); each position is 2 bytes wide. Control storage is loaded from the disk drive in a normal operation, or from the 33FD when running diagnostic programs. The loading of control storage occurs during the IMPL (initial microprogram load) sequence. When loaded, control storage contains the microprogram used to control the CPU and I/O devices.

Storage Address Register (SAR)

SAR is a 16-bit register used to address both main storage and control storage.

Micro Operation Register (MOR)

The MOR is a 16-bit register that holds each micro instruction as it is fetched from control storage. From here, the micro instruction is analyzed to control the data flow such as gate selection, ALU operation, LSR selection, etc.

Process Condition Register (PCR)

The PCR is an 8-bit register that contains information to be tested by branch instructions. For example, from the PCR, the result of a previous arithmetic instruction can be determined to be positive, negative, or zero. The PCR also contains results from compare or test mask instructions.

Storage Data Register (SDR)

The SDR is a 16-bit register that serves as an intermediate buffer for all micro instructions and data bytes fetched from storage. Each micro instruction, being 2 bytes wide, uses all 16 bit positions. Data from main storage, being only 1 byte wide, uses bit positions 8 through 15.

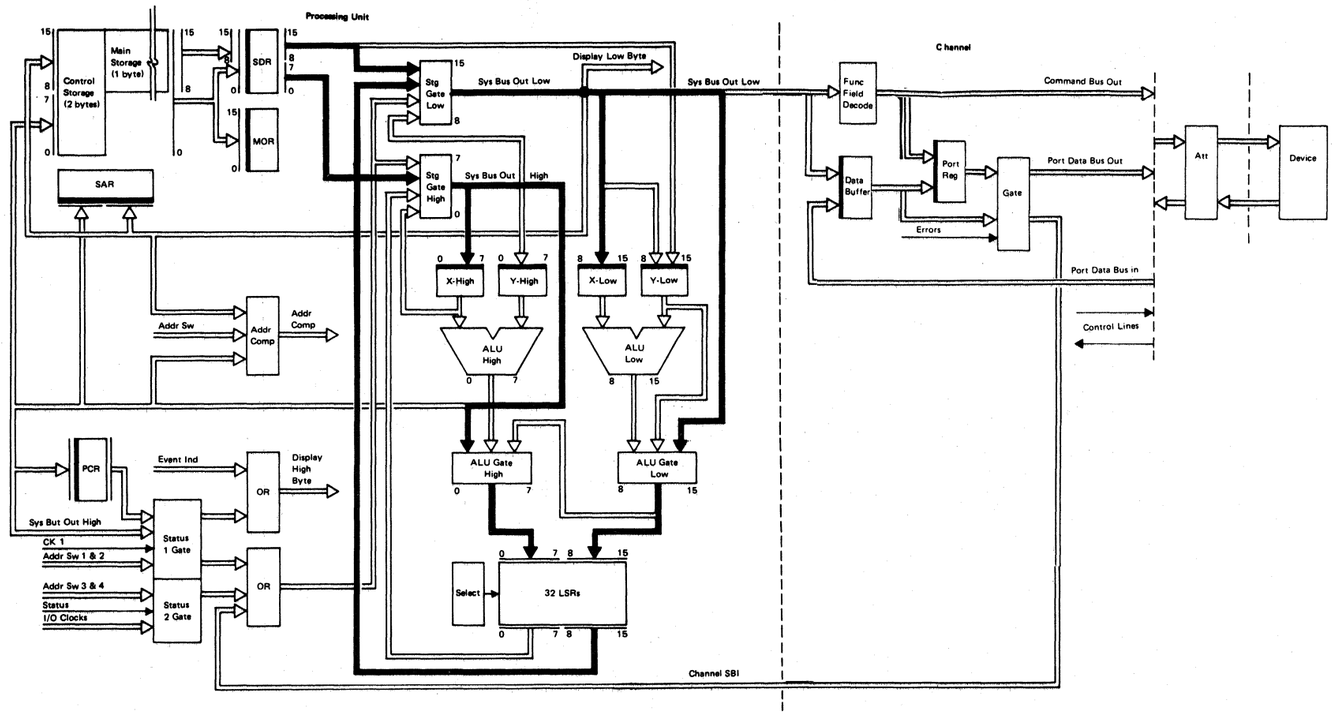
X and Y Registers

These four registers are 8-bit registers that serve as the buffer input for the two ALUs. The X-high and Y-high registers serve as input to ALU high while the X-low and Y-low registers serve as input to ALU low. The data for these registers comes from the local storage registers or the immediate data field of some micro instructions.

Arithmetic Logical Unit (ALU)

There are two ALUs in the system, ALU high and low. ALU high processes bits 0-7 when 2-byte data fields are involved. ALU low processes bits 8-15 when either 1-byte or 2-byte data fields are involved. The ALUs always present 2 bytes of data to the LSR input bus. When 2 bytes are involved in the ALU operation, both bytes (high and low) are placed on the LSR input bus and simultaneously written into bits 0-7 and bits 8-15 of the LSR. When the ALU output is only 1 byte, the byte is presented to both the high and low LSR input bus lines. In these cases, the micro instruction selects only 1 byte to be written into an LSR.

System Data Flow Through the Functional Units



Note: Channel, as used in this system, refers to the internal interface between the processor and logic for control of I/O function. The channel contains a port through which part of this control passes.

Local Storage Registers (LSRs)

The LSR stack contains 64 LSRs; the first 32 are used by the base system and the remaining 32 are reserved for optional features. Each LSR contains 16 bits: bits 0-7 are the high LSR and bits 8-15 are the low LSR. The LSRs are called work registers (WR) and are used as data buffers and address registers for both main and control storage. In addition, the LSRs are used as operand registers for calculations and as I/O control data registers that can be loaded from or sent to the I/O attachments.

The first 32 LSRs are subdivided into four groups. The current micro interrupt level determines which group is used. The first group (hex address 00-07) is used by micro interrupt level 0 (machine check interrupt) and also by the main program level. The second group of LSRs (hex address 08-0F) contains the MAR/MAB (microprogram address register/ microprogram address backup) stack. MAR contains the address of the next micro instruction to be executed. MAB contains the return address when a branch and link instruction is executed. The third group (hex address 10-17) is used by micro interrupt level 1 (disk drive), and the fourth group (hex address 18-1F) is used by micro interrupt level 2 (printer, BSCA, and keyboard).

Optional features use the remaining 32 LSRs. The first group (hex address 20-27) is used by micro interrupt level 3 as work registers. The second group (hex address 28-2F) contains the MAR/MAB for micro interrupt level 3 (hex address 28-29).

Micro Interrupts

The CPU handles micro instructions one at a time; one micro instruction is followed by the next sequential micro instruction. This sequence of execution of micro instructions can be changed by a branch instruction. This sequence can also be changed if the main level of processing or a micro interrupt level is interrupted by a higher micro interrupt level.

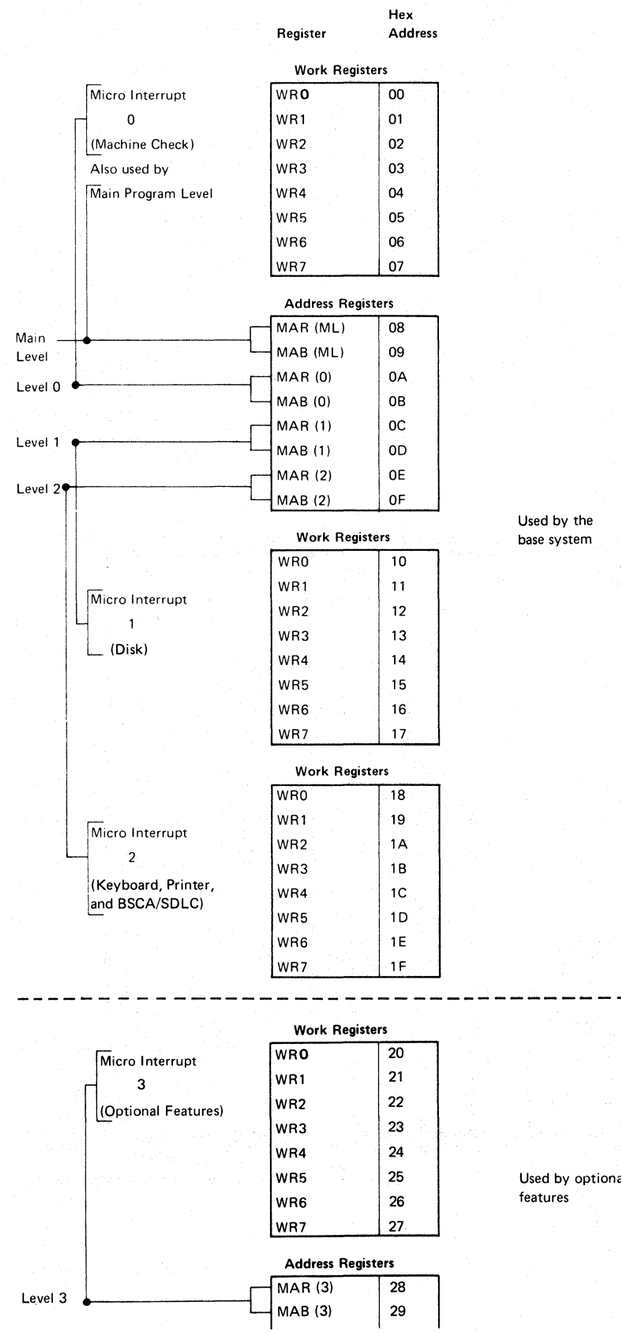
The system has six levels of micro interrupts, only level 0, level 1, level 2, and level 3 are used (levels 4 and 5 are reserved). Level 0 has the highest priority and level 3 the lowest micro interrupt priority. The display screen and 33FD cannot cause micro interrupts. Interrupts having a higher priority take precedence over those having a lower priority. For example, a micro interrupt on level 0 will interrupt the processing of a level 1, 2, or 3 micro interrupt.

A machine check interrupt occurs whenever the system detects a CPU parity check, invalid address, or microprogram check. This micro interrupt can also be initiated by a port check. These checks are described on page CNSL-6. A level 1 interrupt occurs whenever the disk drive requires attention. The printer, BSCA, and keyboard operate on interrupt level 2. BSCA has highest priority, printer second, and the keyboard last.

Level 0, machine check interrupt, shares a set of work registers with the main level microroutines. Micro interrupt levels 1, 2, and 3 have a unique set of registers in the LSR stack. The set of LSRs for each micro interrupt level consists of:

8 16-bit work registers.
1 MAR (microprogram address register) used to store the address of the current micro instruction.
1 MAB (microprogram address backup) used to store the return address when a branch and link instruction is executed.

LSR Subdivision and Micro Interrupt Levels



System Checking and Parity Generation

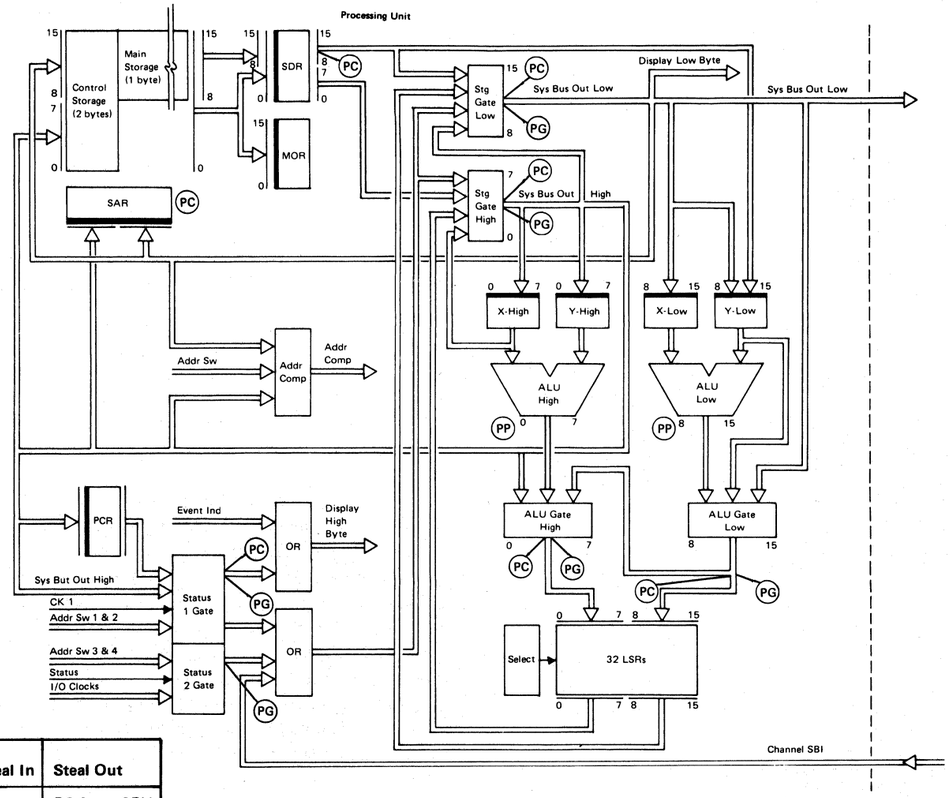
Various errors that occur in the system are recorded in the CPU error byte and in the port check byte. These errors can be displayed on the CE panel and are described on CNSL-6.

Odd parity (by byte) is maintained in the CPU data flow. To ensure correct parity, parity checking stations and parity generating stations are provided throughout the CPU.

Parity predict circuits are used as a check on the ALU portion of the CPU. By analyzing the operation being performed and the input data, parity predict circuits predict whether the output of ALU will require a P-bit, and then generate the P-bit if required. The parity of the output of the ALU is compared to the output of the parity predict circuits to determine whether the ALU is working correctly.

Parity errors may be detected between the port and the CPU, or the port and an I/O attachment. Normally, the port operates in odd parity, however, some diagnostic programs use even parity.

Parity Checking and Generation in the CPU



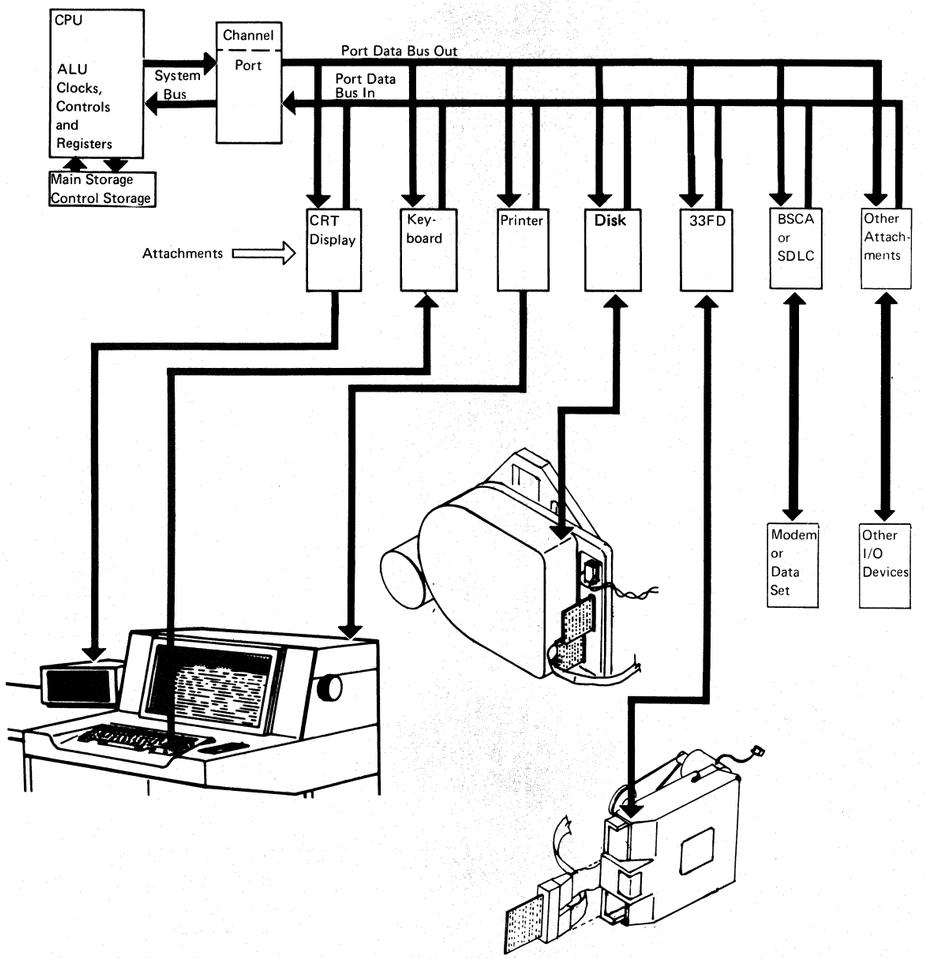
	IOCL	IOCS	Interrupt Level Status	Steal In	Steal Out
Channel	PG	PC	No PC, PG in Channel	PC	PC from CPU PG to DBO
Display	PC	PG	—	N/A	N/A
Keyboard	PC	PG	—	N/A	N/A
Printer (Belt or Serial)	PC	[1]	—	N/A	N/A
33FD	PC	PG on Data Transfer Only[1]	—	PG[2]	N/A
Disk	PC	PG on Data Transfer Only[1]	—	PG	PC
BSCA	PC	PG	—	N/A	N/A

PC — Parity Checked
PG — Parity Generated

[1] Attachment activates CBI 4 line to CPU, which denotes that parity is not generated on DBI for transfers to the channel.

[2] 33FD cycle steals on IMPL only.

Note: Attachments generate a parity bit on the DBI when responding to a jump I/O command whether or not the condition true response (CBI 4) is met.



Retry and Error Logging

If errors occur during some operations, the operation is retried. Operations that cause errors while the emulator is analyzing system instructions and some operations that cause errors during the execution of the system instructions are retried at the system level.

Error logging is used by the system to assist the CE in the analysis of intermittent errors. All error conditions that can be retried are logged in control storage and where possible, are recorded on the disk drive. Error conditions that are recorded may be retrieved and printed using ERAP program (error recording and analysis procedure).

Essentially, two types of error information are recorded for each device and the CPU, error history and error count. In addition, the number of I/O operations performed by each device is also recorded.

Each device except the display screen has an error history table in which to record a number of entries. If the table becomes full, the most recent entries are retained.

Error count tables contain the number of times a specific error has occurred. When these tables reach their maximum value, this value is retained until cleared by the CE.

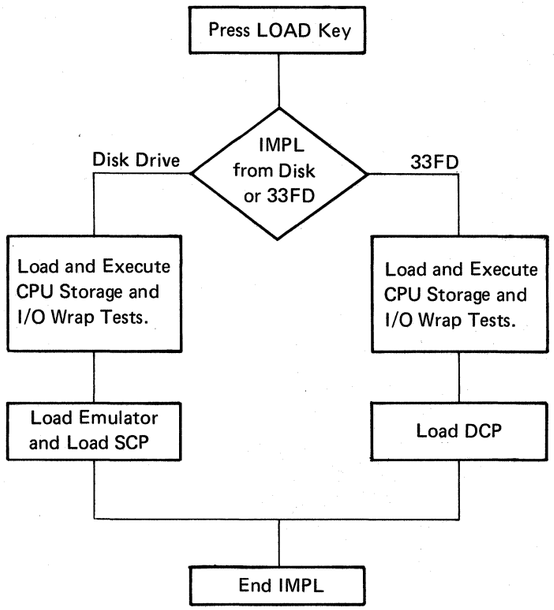
Details of the error history and error count tables are in the *Diagnostic Service Guide.*

Initial System Checkout

To ensure the system circuitry is functioning properly, a series of diagnostic tests are run each time LOAD is pressed. These tests fall into two groups. The first group checks out the CPU, main storage, and control storage. The second group, called I/O wrap tests, checks out the I/O attachments. However, the I/O wrap tests do not cause the I/O devices to operate (individual diagnostic programs may be run later to exercise the selected I/O device).

To assist in isolating a failing area, an event register is displayed in the leftmost display byte on the CE panel. When LOAD is pressed, all nine indicators turn on. As various portions of the system checkout are completed, the event indicators are turned off in sequence. Thus, it is possible to narrow the area of failure. A more detailed description of the event indicators is found on IMPL-1.

After the tests are successfully completed, the emulator and SCP (system control program) are loaded from the disk drive if the device select switch is in the IMPL DISK position. If the switch is in the IMPL DISKETTE position and the DIAG 01 diskette has been inserted in the 33FD, the DCP (diagnostic control program) is loaded from the 33FD following the successful completion of the system checkout. With the DCP loaded, additional diagnostic programs can be run to exercise I/O devices.



Processing Unit

The CPU (processing unit) consists of five cards on gate 1A, board A1 and has the following functions:

- Emulates system instructions.
- Assists control of system I/O.
- Handles some of the SCP (system control programming).
- Handles system I/O.

The five CPU cards and the hardware on each card are as follows:

System Control Card
- ALU control lines
- ALU carry in control lines
- Storage gate high/low control lines
- ALU gate high/low control lines
- LSR addressing and control
- MOR (micro operation register)
- Control panel display
- CPU clocks

Storage Control Card
- SAR (storage address register)
- System reset logic
- Storage clocks
- Invalid address checking
- Display bits 8-11
- IMPL sequence control
- Oscillator

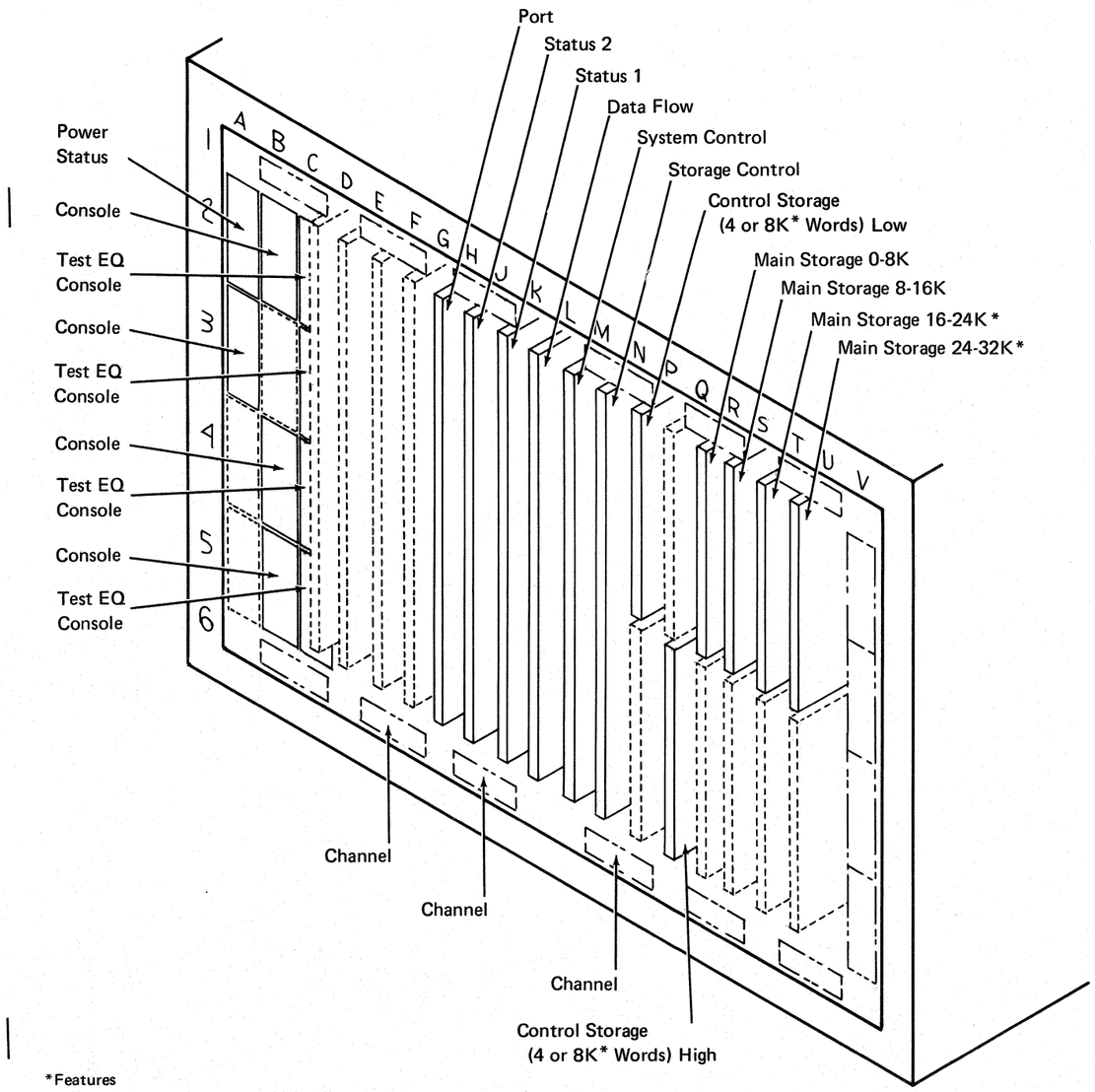
Status 1 Card
- PCR (processor condition register)
- CPU checks register
- Address switches 1 and 2
- Event indicators
- Display bits 0-7, P high
- Address compare high logic

Status 2 Card
- Address compare low
- Display bits 12-15, P low
- Control panel functions
- Control panel sense byte
- I/O clocks

Data Flow Card
- LSRs (local storage registers)
- ALUs (arithmetic and logical units)
- SDR (storage data register)
- Storage gates high and low
- ALU gates high and low
- X and Y registers
- Parity predict

The five CPU cards and the main and control storage cards are located as shown.

Card Side of Gate 1A, Board A1



*Features

CPU Data Flow

CPU data can be handled either 1 byte at a time or 2 bytes at a time. The quantity of data (1 byte or 2 bytes) and the exact path of that data depends on the micro instruction being executed.

System bus in from the channel is 1 byte but that byte can be handled as either a high or low byte once into the data flow.

Data can be cross gated from the high byte of the LSRs to the low byte of the data path. Main storage data can be loaded to either the high or low side of the LSRs. ALU operations can be either 1 or 2 bytes, or combinations.

Parity Checking

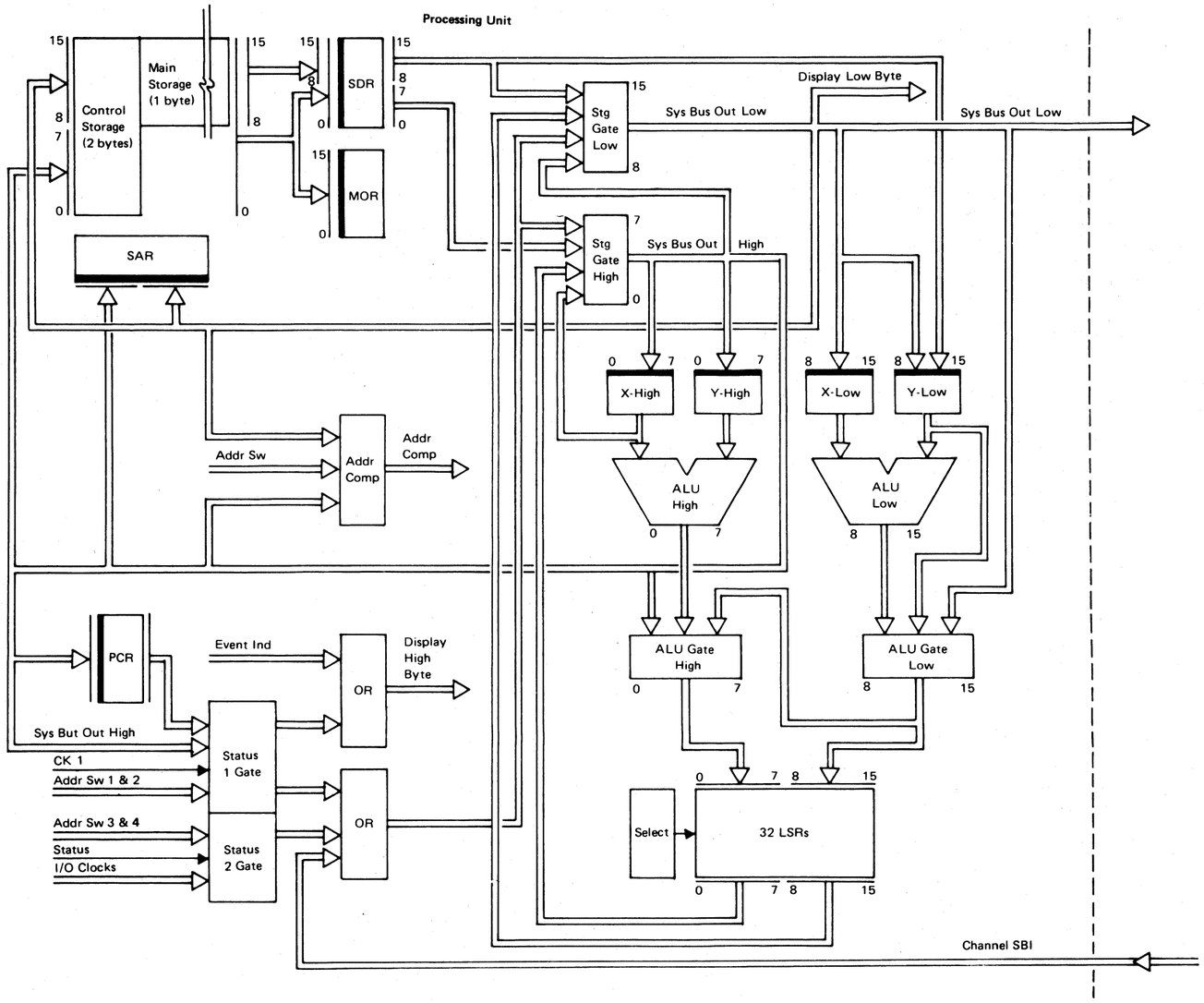
Odd parity by byte is maintained in the data flow. To ensure correct parity, checking and generating stations are used throughout the system. Parity checking is done on SAR, SDR, storage gates high and low, ALU gates high and low, and MOR. In addition, parity is checked on the channel data lines.

Parity generating stations are provided for status register, control panel, switch bytes, and other internally generated data pertinent to the CPU (storage gate high and ALU gates high and low).

CPU Default Conditions

If no hardware conditions are specified for the CPU by the micro instruction, the system has certain built-in selections and functions. These selections are called default conditions. The default conditions for the functional units in the CPU are as follows:

Unit	Default
Storage gate high	LSR high
Storage gate low	LSR low
ALU gate high	ALU high
ALU gate low	ALU low
ALU function	X plus 1



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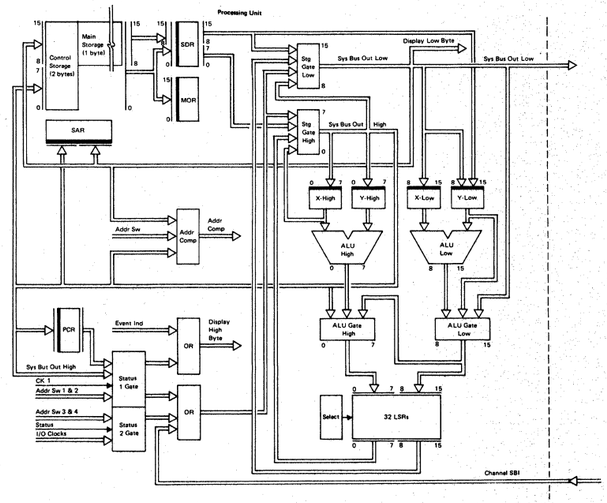
CPU Functional Units



ALU (PL060, PL070)

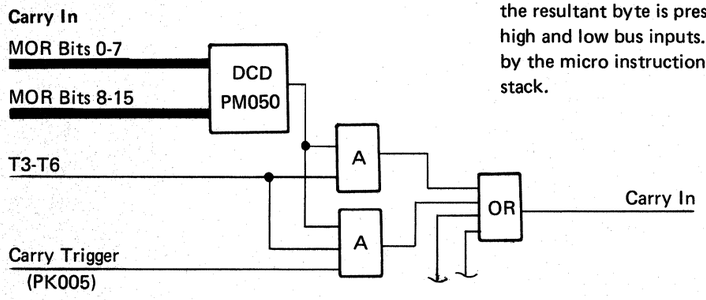
The ALU (arithmetic/logical unit) is divided into two parts. The ALU high unit operates on bits 0-7 when 2-byte data fields are involved; and the ALU low unit operates on bits 8-15 when a 1-byte or 2-byte data field is involved.

The ALU can perform the following arithmetic and logical functions:

Function	F0	F1	F2	F3	Carry In
X XR Y	0	0	0	1	0
X OR Y	0	0	1	1	0
X AND (not) Y	0	1	0	1	0
X AND Y	0	1	1	0	0
X OR (not) Y	0	1	1	1	0
X minus one	1	0	0	0	0
X plus Y plus carry	1	0	0	1	C
X minus Y (16/8)	1	0	1	0	1
X plus Y (16 or 8)	1	0	1	1	0
X minus Y (16 or 8)	1	1	0	0	1
X plus Y (16/8)	1	1	0	1	0
X minus Y minus one plus carry	1	1	1	0	C
X plus one (carry in)	1	1	1	1	1

16/8—One field 16 bits, second field 8 bits.
16 or 8—Both fields 16 bits or both fields 8 bits.

Carry In
C = Carry used (carry trigger from previous operation)
1 = Force carry to 1 (by hardware, T-times, and instruction)
0 = Not used



The four function bits are generated in the system control card (PM040) as determined from the instruction (MOR bits) and the T-times. The carry in line (PM050) is brought up either by the 'carry trigger' which is on from a previous operation (force carry to one) or when the instruction MOR bits are decoded to show carry trigger needed (carry used).

Any data sent to the ALU is first loaded into the X-high and Y-high registers for the high bytes and the X-low and Y-low registers for the low bytes. The X-registers provide the data for one operand and the Y-registers provide the data for the other operand that is used in the current ALU operation. Depending on the micro instruction and its function, either 1 byte or 2 bytes are affected by the ALU.

The ALU can handle arithmetic operations involving two 16-bit words, one 16-bit word plus/minus one 8-bit byte, or one 8-bit byte plus/minus one 8-bit byte. The instruction logical/arithmetic 1 is used for 8 by 8-bit arithmetic. Logical/arithmetic 2 is generally used for 16 by 16-bit arithmetic and 16 by 8-bit arithmetic. When doing 16 by 8-bit arithmetic, the line 'reset Y high reg' (generated on the data flow card) is used to reset the unused 8 bits of the Y-register.

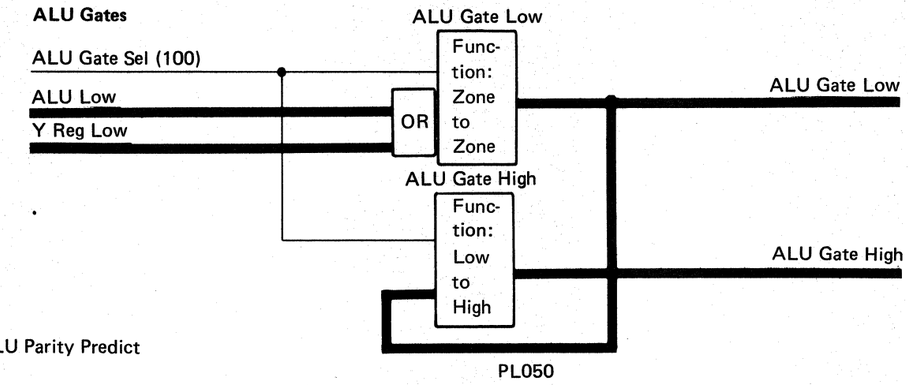
Instructions involving increment or decrement of the X-register are handled by activating the lines 'reset Y high reg' and 'reset Y low reg' and forcing 'carry in' (turn on 'carry trigger'). This causes only the X-register to be affected by the instruction.

The output of the ALU always presents 2 bytes of data to the LSR stack input bus. If 2 bytes are required by the ALU operation, both bytes are directly placed on the input LSR bus and simultaneously written into the LSR stack. If only 1 byte was operated on by the ALU, the resultant byte is presented to both the high and low bus inputs. Only the byte selected by the micro instruction is written into the LSR stack.

ALU Gates

The ALU gates high and low control the final destination of the ALU data. The decode of 'ALU gate high/low sel 0, 1, 2' lines gate data through the ALU gates (selectors) and control the selection of the source data (PL050). These select lines are generated (PM045) by a decode of MOR bits and the T-times.

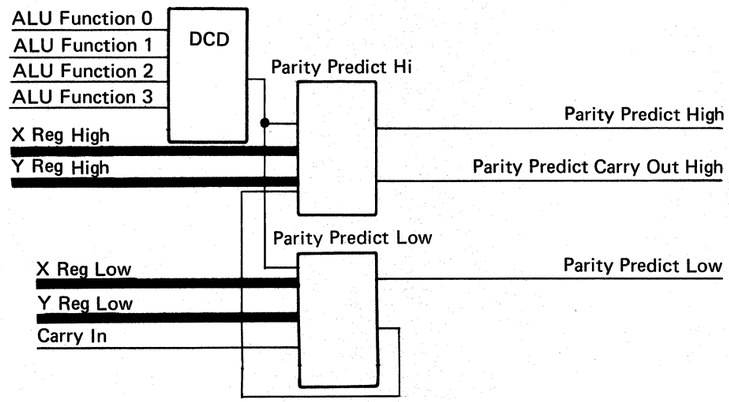
Example: LA1 [0][1][1][0]
0 3
ALU gate sel = 100 (PM045)
ALU gate low = Zone to zone (from ALU bits low or Y reg low)
ALU gate high = Low to high (from ALU gate high)



ALU Parity Predict

Parity predict circuits (PK060) predict the parity of the result of the ALU operation. This predicted parity is compared against the actual parity of the result. If a discrepancy exists, a parity check results.

Parity Predict Circuits



Local Storage Registers (LSR)

The LSRs (PL040) are used by the microprocessor as:

- Data buffers and address registers for main and control storage.
- Operand registers for internal calculations.
- I/O control data registers that can be loaded from or stored in I/O attachments.

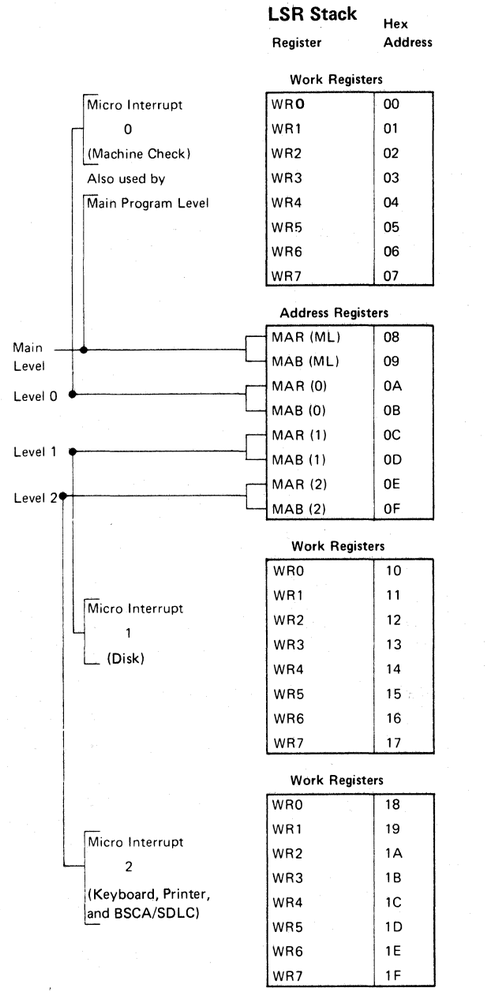
The first 32 LSRs are subdivided into four groups as shown. The micro instruction address register/ micro instruction address backup (MAR/MAB) stack is used by main level, machine check, interrupt level 1, and interrupt level 2. Each of the other three groups can be used only by the named level. Work register (WR) 4 of interrupt level 1 is also used as a work register (data address register) by burst mode (disk drive).

Optional features use 10 of the remaining 32 LSRs. The first group (hex address 20-27) is used by micro interrupt level 3 as work registers. The second group (hex address 28-2F) contains the MAR/MAB for micro interrupt level 3 (hex address 28-29).

Each LSR is 16 bits wide (plus a parity bit for each byte).

LSR Addressing

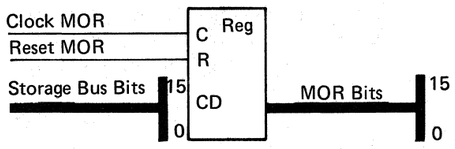
LSR addressing is controlled by the system control card (PM060, PM065). The appropriate addressing bits are turned on by a decode of the MOR bits and T-times. Writing LSRs (PM070) is controlled by MOR bits, T-times, and (not) 'trigger A'.



Micro Operation Register (MOR)

The micro operation register (PM010) holds the micro instruction as it is fetched from control storage (storage bus bits). The micro instruction is used for gate selection, ALU functions, setting the microstatus register, and address selection for LSRs.

Micro Operation Register



Storage Data Register (SDR)

The storage data register (PL020) is used as an intermediate buffer for each micro instruction and all data bytes fetched from storage. The SDR high order bits (0-7) are gated through storage gate high to the high order X-register and Y-register and subsequently to the ALU. The SDR low order bits (8-15) are gated to the low order X-register and Y-register and subsequently to the ALU.

X-Registers

The X-registers (PL010) are buffers for base factors of the ALU. Data comes from the immediate field of some branch instructions or from the LSRs.

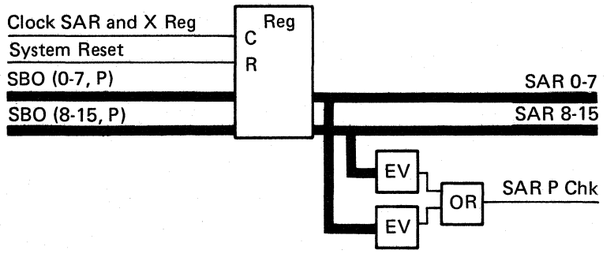
Y-Registers

The Y-registers (PL010) act as buffers for modifying factors of the ALU. The data comes from the immediate field of some branch instructions or from the LSRs.

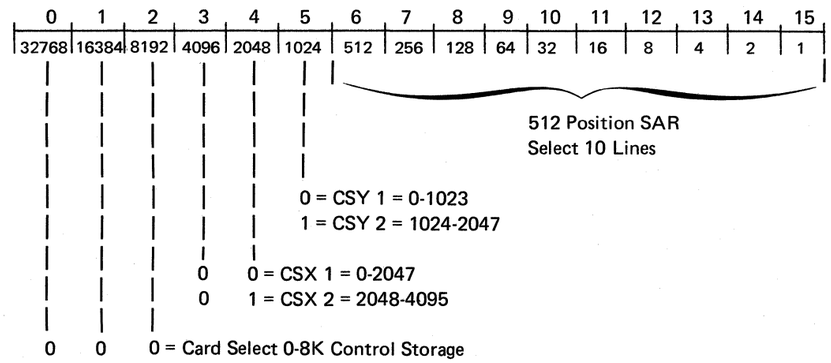
Storage Address Register (SAR)

The storage address register (PN010) holds all storage addresses which are transferred from the LSR or built from the LSR, X-high, and SDR data. The data transferred in does not change during the storage cycle.

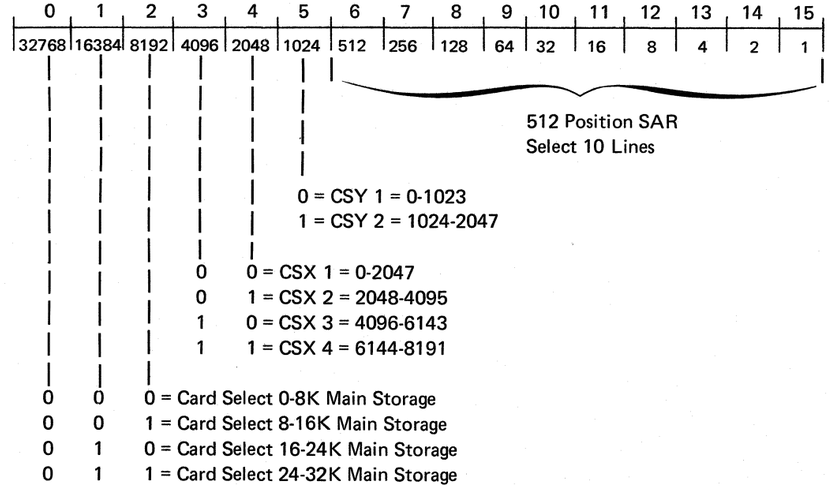
Storage Address Register

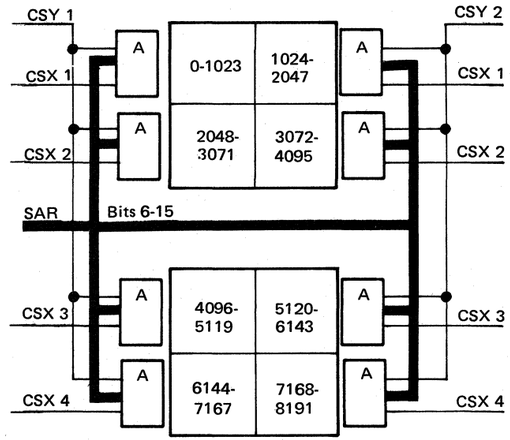


SAR Decoding (PN020) Control Storage



SAR Decoding (PN020) Main Storage



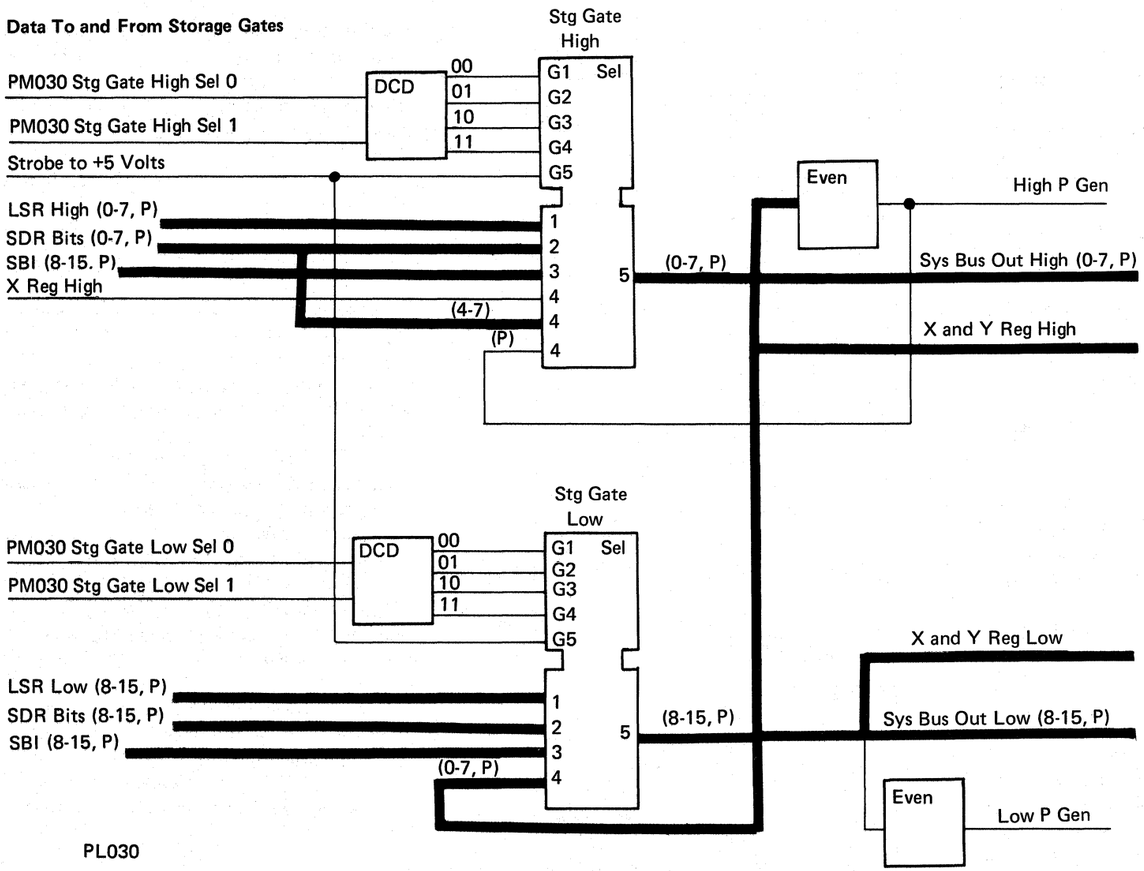


Storage Gates

The storage gates (data flow card PL030) make data coming from SDR, LSR, system bus in, and X-register available to system bus out and to the X- and Y- registers.

The selection bits are developed in the system control card (PM030) by the MOR bits and the T-times.

Data To and From Storage Gates



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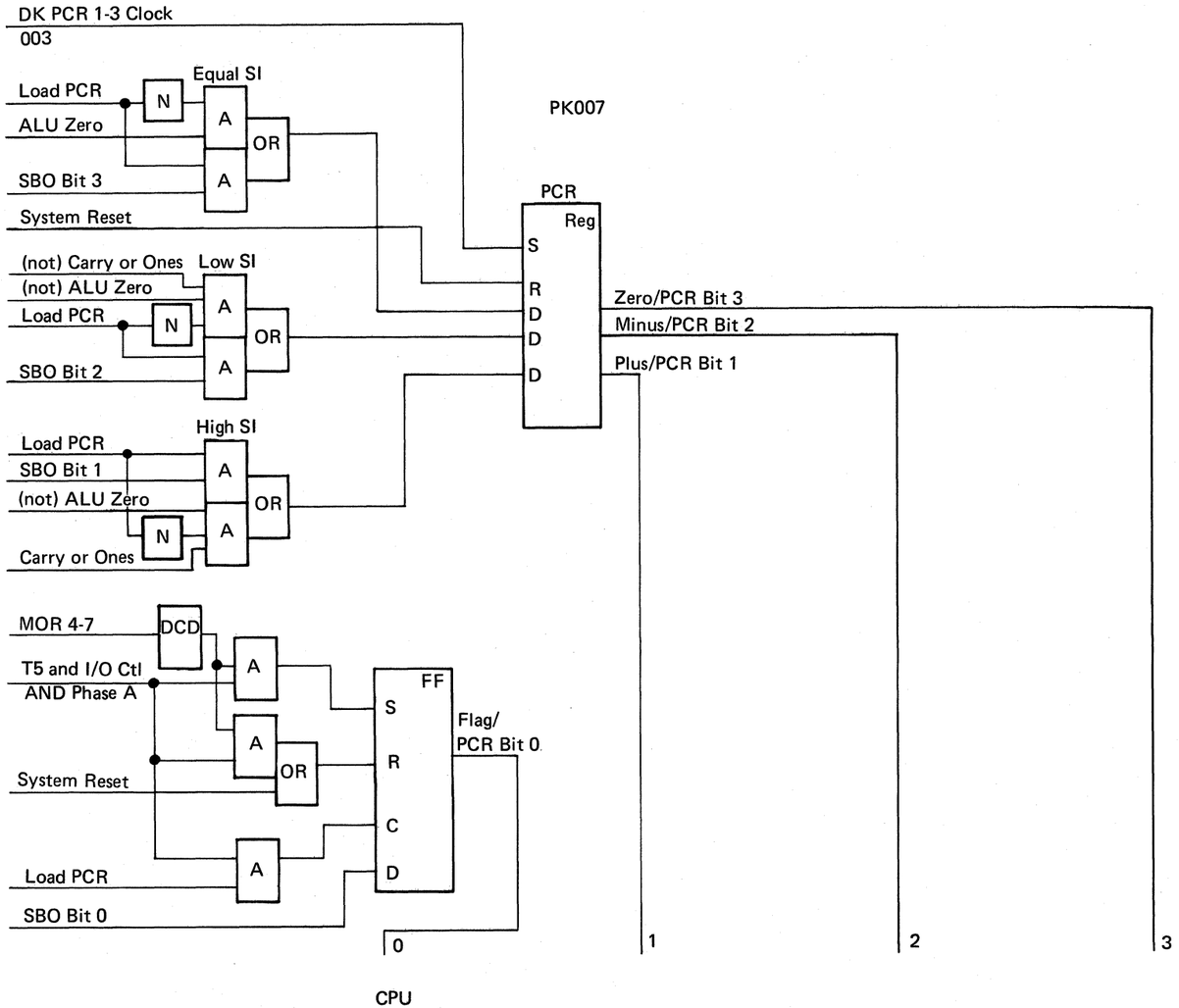
Processor Condition Register (PCR)

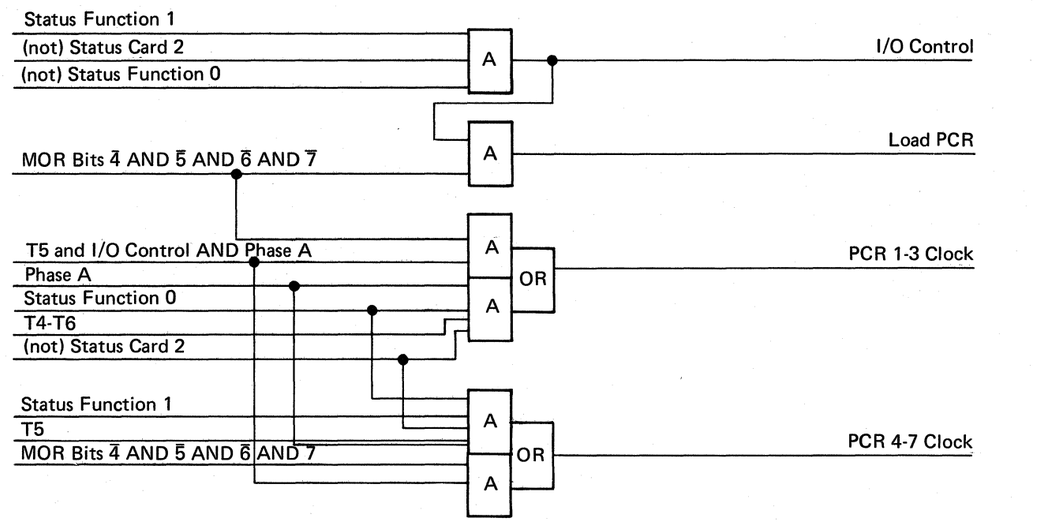
The PCR (PK005, PK007) contains the processor conditions that are tested by the branch on condition instruction. The PCR is changed by system reset, program loading, or instructions that modify register bits. These conditions are modified by the micro instructions that perform the add, subtract, test mask, compare immediate, subtract immediate, and R1 linked with R2 functions.

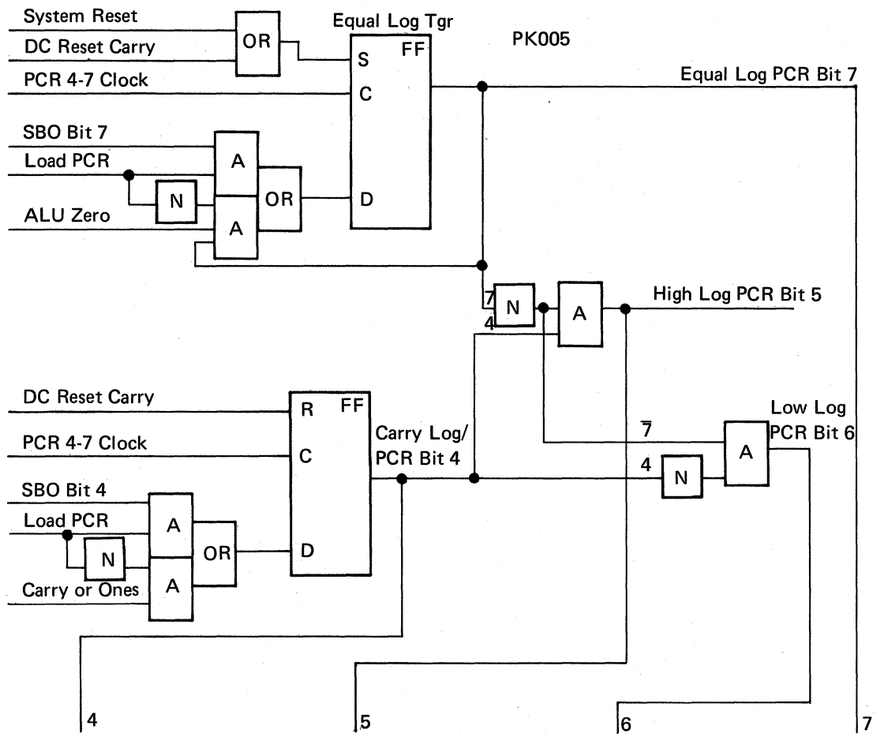
The PCR clocks (PK003) gate the data into the PCR. These clocks are shown on the right.



CPU

PCR Clocks (PK003)





Processor Condition Register

PCR		Flag Bit 0	Positive Bit 1	Negative Bit 2	Zero Bit 3	Carry Bit 4	High Bit 5	Low Bit 6	Equal Bit 7
LA1 or LA2 Logical	Set		Result of logical operation does not equal zero *and* (R1 or $\overline{R2}$ equals all ones).	Result of logical operation does not equal all zeros *and* (R1 or $\overline{R2}$ does not equal all ones).	Result equals all zeros.				
	Reset		Result of logical operation equals all zeros *or* (R1 or $\overline{R2}$ does not equal all ones).	Result of logical operation equals all zeros *or* (R1 or $\overline{R2}$ equals all ones).	Result does not equal all zeros.				
(See also μINSTR-9)									
LA1 or LA2 Arithmetic	Set		Result has a carry and does not equal zero.	Result has no carry and does not equal zero.	Result equals zero.	Result had a carry (add), or no borrow (subtract).	Result has a carry and does not equal zero.	Result has no carry and does not equal zero.	
	Reset		Result has no carry or equals zero.	Result has a carry or equals zero.	Result does not equal zero.	Result has no carry (add) or a borrow (subtract).	Result has no carry or equals zero.	Result has a carry or equals zero.	Result does not equal zero.
Test Mask	Set		Tested bits equal all ones.	Tested bits do not equal all ones and do not equal all zeros.	All tested bits equal zero (or no bits tested).				
	Reset		Tested bits do not equal all ones.	Tested bits equal all ones or all zeros.	Tested bits do not equal zero.				
Compare or Subtract Immediate	Set		Register data is greater than immediate data.	Register data is less than immediate data.	Register data is equal to immediate data.				
	Reset		Register data is not greater than immediate data.	Register data is not less than immediate data.	Register data is not equal to immediate data.				
I/O Immediate Reset Carry – Set Equal	Set								Equal set on.
	Reset					Carry set off.	Decoded from carry, equal, and set off.	Decoded from carry, equal, and set off.	
I/O Immediate Load PCR	Set	Loaded bit 0 is on.	Loaded bit 1 is on.	Loaded bit 2 is on.	Loaded bit 3 is on.	Loaded bit 4 is on.	Loaded bit 4 on and bit 7 off.	Loaded bit 4 off and bit 7 off.	Loaded bit 7 is on.
	Reset	Loaded bit 0 is off.	Loaded bit 1 is off.	Loaded bit 2 is off.	Loaded bit 3 is off.	Loaded bit 4 is off.	Loaded bit 4 off or bit 7 on.	Loaded bit 4 on or bit 7 on.	Loaded bit 7 is off.
System Reset	Set								Equal set on.
	Reset	Set off.	Set off.	Set off.	Set off.	Carry set off.	Decoded from 4 and 7 and set off.	Decoded from 4 and 7 and set off.	
I/O Immediate Flag Latch	Set	Set on.							
	Reset	Set off.							

Main Storage

Main storage consists of 16,384 bytes of FET storage. Each byte is 8 bits plus one parity bit. One byte of information is available to the CPU for each storage access.

Control Storage

Control storage contains 4096 locations (8192 locations on machines with the Control Storage Increment Feature). Each location is 2 bytes wide. Micro instructions that control CPU and I/O operations are loaded into control storage at IMPL time. A map of control storage is shown here.

Control Storage

Direct Area
Fixed Communications Area
Keyboard Katakana Converter (if KANA is used)
Keyboard Decode Table/CRT Buffer
System Emulator
Disk I/O
Printer I/O
Keyboard/Display Screen I/O
Transient Area
Microinterrupt Handler
Nucleus Functions

Control Storage Increment Feature

(additional 4K words of control storage)

The direct area and fixed communications area are common areas used by portions of the micro-program. These areas contain machine check log area, system registers, and interrupt branch tables.

Keyboard decode table contains a table to decode the data bits coming from the key-board. This is necessary because the bits coming from the keyboard are not in a standard code.

The CRT buffer stores the message to be dis-played on the CRT. This buffer is then trans-ferred to the buffer in the CRT attachment. If the display is to be printed, the printer I/O area prints from the CRT buffer.

The system emulator classifies system instructions as CPU instructions or as I/O device instructions. When the instruction is a CPU instruction, the emulator also executes the CPU instruction. If the instruction is an I/O device instruction, it is executed by the appropriate I/O area of control storage.

After the emulator has classified a system instruction as an I/O operation for one of these devices, control is passed to the appropriate area. For example, if the instruction is a printer instruction, control is passed to the printer I/O area of control storage.

The micro interrupt handler is used to process I/O interrupts.

The transient area is used for devices whose I/O microroutines are not resident in control storage; for example, the 33FD microroutines. If the required microroutine is not in control storage when called, it will be loaded into the transient area.

The area called nucleus functions contains pointers, routines and subroutines such as 'system reset/restart', 'save/restore registers', 'SVC processors', etc.

Direct Area of Control Storage

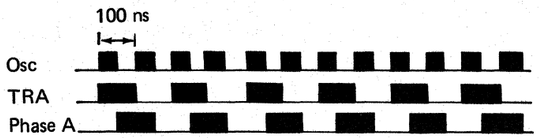
The first 128 words of control storage function are directly accessible locations within the system. The contents of this direct area are shown in the fixed control storage map.

Hex Address	High Order Byte	Low Order Byte
0000	Address of reset routine	
0001 to 000D	Transient work space and storage	
000E to 0011	Not used	
0012	Temporary work space for microprogram interrupt levels	
0013	Interrupt level 0—PCR save	Machine check counter
0014	Interrupt level 0 register save	
0015	Address of machine check log area	
0016	Interrupt level 1—PCR save	
0017	Interrupt level 2—PCR save	
0018	Register save for interrupt level 2 interrupt handler	
0019	Register save for interrupt level 2 interrupt handler	
001A to 001C	Reserved	
001D	Register save on main program level	
001E	Register save on main program level	
001F	Register save on main program level	
0020	Disk control flags	Disk device address
0021	Current head	Not used
0022	Save area of data address for physical retry	
0023	Save area of log control	Command for alternate sector
0024	Save area for subroutine return	
0025	Address of last disk sector processed	Unused
0026	Completion code	Q-byte
0027	R-byte	High byte disk address
0028	Low byte disk address	N-byte (sector count -1)
0029	Storage address of data	
002A	Sense word 1	
002B	Sense word 2	
002C	Error byte	Flag byte
002D	Priority byte	
002E	N-byte	F-byte
002F	Cylinder address	
0030	Head	Sector
0031	Storage address control field	
0032	Address of main storage IOB	
0033	Read verify occurrences	
0034	Write data occurrences	
0035	Read data or scan occurrences	
0036	Seek occurrences (nonzero seeks only)	
0037	Disk current cylinder	
0038	Previous disk cylinder	
0039	Save area for Q- and R-bytes for issued op code	
003A	N-byte	F-byte
003B	Cylinder address	
003C	Head	Sector
003D	MAB save	
003E	Print data address register	
003F	Forms length	Current print line
0040	Work space	Character set size
0041	Status byte	Device address
0042	Interrupt condition	
0043	Save area for WR3 between interrupts	
0044	Console/display IOB address	
0045	Status information	Keyboard device address
0046	Constant record start address	
0047	Cursor location limit	
0048	Constant cursor position	
0049	CRT buffer start address	
004A		Bit 6=1 for Katakana
004B to 004F	Transient work space	
0050	Status information (used as error count on IPL)	
0051	Physical cylinder	Logical cylinder
0052	Address of control storage transient area	
0053	Address of start of transient status word table	
0054	Address of I/O device branch table	
0055	Address of end of register stack	
0056	Address of system interrupt branch table	
0057	Address of control storage interrupt branch table	
0058	Address of control storage interrupt level status word backup (CSILSWBK)	
0059	Address of control storage interrupt level status word (CSILSW)	
005A	Address of IOB save area in direct area	
005B	Address of start of RIB status word table	
005C	Address of program level communication area	
005D	Address of disk error log out area	
005E	Address of return from main storage transient area	
005F	Address of loader parameter list in system communication area	
0060	Address of low order byte of entry address in loader parameter list	
0061	Address of queue zero header	
0062	Address of disk queue header	
0063	Address of system transient disk address table -3	
0064	Address of main storage transient area	
0065	Address of main storage disk IOB for nucleus	
0066	Address of next trace log entry	
0067	Disk address of next push save area	
0068	Disk address of end of push save area	
0069	Address of current stack entry	
006A	Address of next push stack entry	
006B	Displacement of branch to transient in the I/O device branch table	
006C	Control storage interrupt level status word (CSILSW) interrupt mask	
006D	System interrupt level status word (S3ILSW) interrupt mask	
006E	Control storage interrupt level status word backup	
006F	System interrupt level status word backup	
0070	Nucleus job terminator errors	
0071	Disk address of transient currently in main storage	
0072		Interrupt level indicator
0073	Miscellaneous system indicator bits	Miscellaneous system indicator bits
0074 0075	Not used	
0076	Index register 1	
0077	Index register 2	
0078	Main storage op code	Main storage Q-byte
0079	Instruction address register	
007A	Program status register	
007B	Address recall register	
007C	Address recall register for decimal operations	
007D	Address of system op code being executed	
007E	Control storage interrupt level status word (CSILSW) Bit 0 1 Keyboard (I/O control) 2 Printer (I/O control) 3 Disk IOS 4 5 Trace Instructions 6 Machine Check Logout 7 Inquiry 8 through 15 must be zero	
007F	System interrupt level status word (S3ILSW) Bit 0 1 BSCA 2 Keyboard 3 4 5 6 7 8 through 15 must be zero	

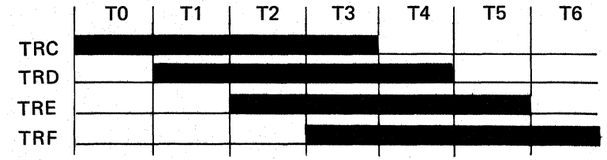
CPU Clocks

System Clocks

The system has a free running 100 ns oscillator. The rise of this oscillator causes TRA to change state, while the fall of the oscillator causes phase A to change state.

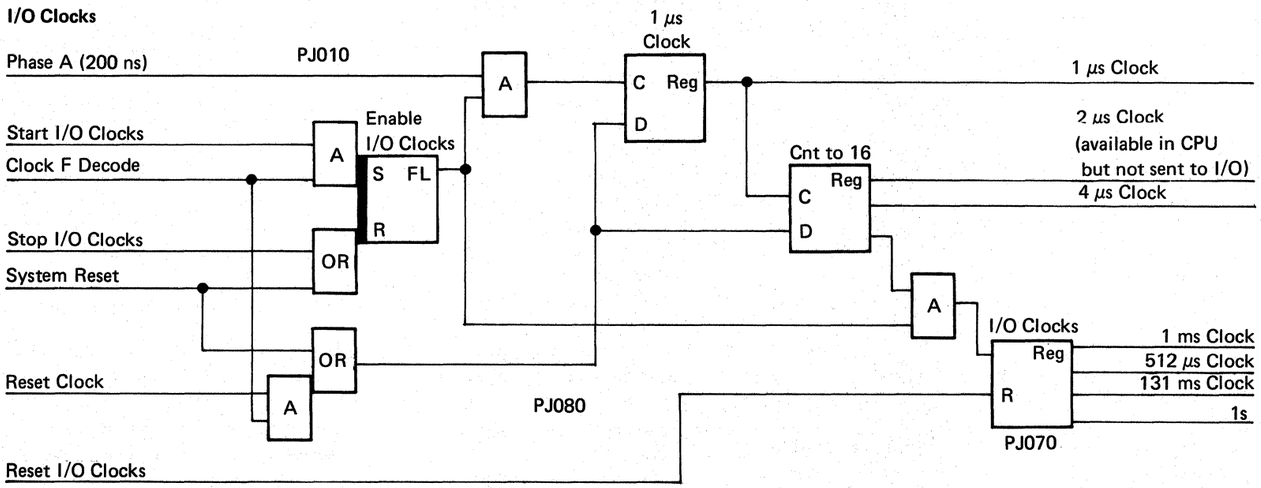


Four system clock triggers are decoded to determine the T-times. These triggers change state with the output of the AND of (not) 'phase A' and the oscillator.



When the current instruction is decoded, the system determines if some of the T-times are not needed and controls the gating of the triggers to skip the unneeded T-times.

I/O Clocks



I/O Clocks

The CPU supplies seven continuously running clocks which are used by the I/O attachments. These seven clocks can be stopped and started for diagnostic testing. One clock is the 100 ns free running internal oscillator and this oscillator generates 'phase A' which in turn, generates the other six clocks. The periods of these clocks are:

100 ns (generated by oscillator only)
1 μs
4 μs
1 ms
512 μs
131 ms
1s

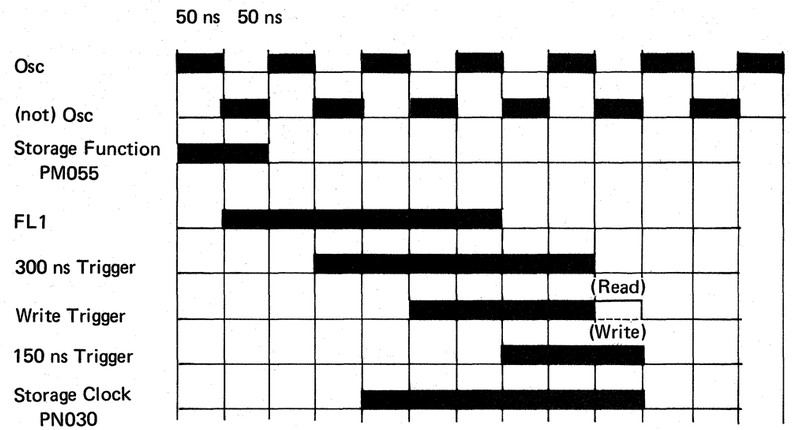
These clocks are part of the timers sensed by the I/O immediate instruction.

Storage Clocks

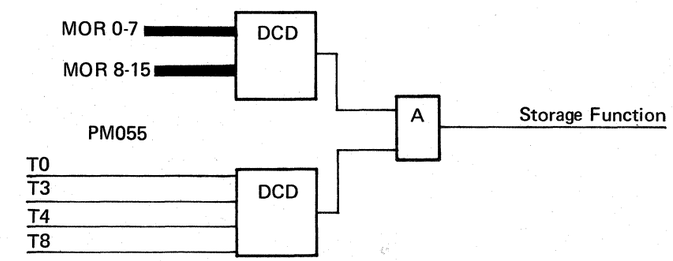
During micro instruction fetch time T0 through T2, T0 time is used to establish the address in control storage for the next instruction and to place this address into the storage address register (SAR). During T1 and T2, the storage address is accessed for reading the data.

The storage clocks are also used during burst mode operations. When an I/O device raises 'block processor clock', the CPU finishes whatever micro instruction it is processing and then goes to the T7 state where it is held until 'block processor clock' is dropped. The rise of 'FD/RD (IMPL) BC REQ' while BPC is active generates 'storage cycle request' which in turn generates T8; T8 is then used to establish the storage address in the storage address register (SAR) just as T0 is used in the normal run mode previously described. After the operation is completed, 'block processor clock' is dropped and the system clocks are allowed to run.

Storage Access Sequence



Storage Function

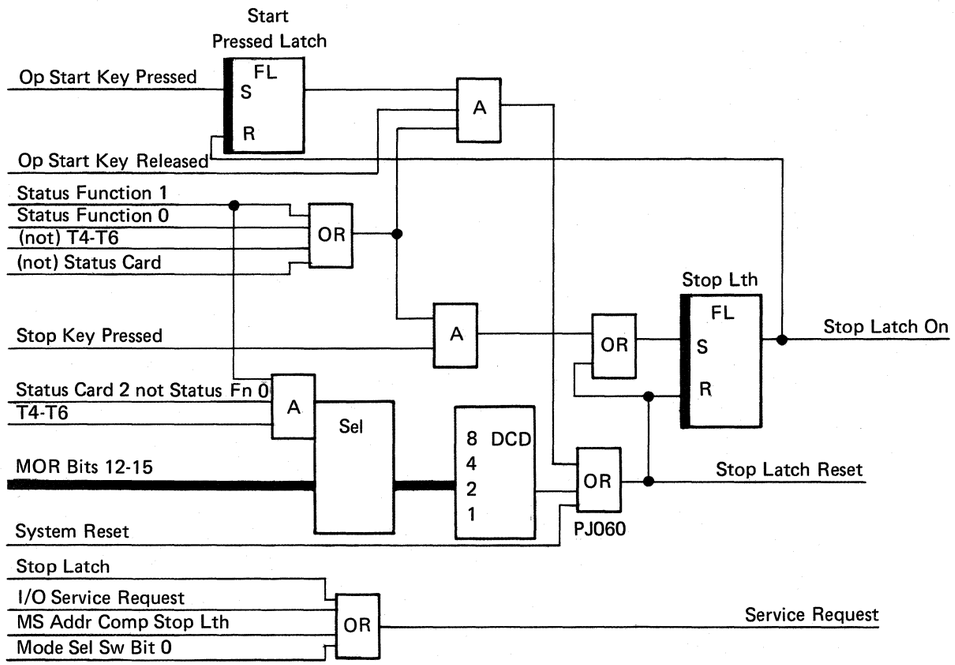


Service Request

Service request comes up whenever the operator or CE requests service through the operator control panel or the CE control panel.

System Reset

System reset (PN060) occurs whenever the RESET is pressed or power on reset is generated. System reset also occurs when LOAD is pressed initiating an IMPL sequence. Pressing LOAD sets 'IMPL pressed lth' which brings up system reset. Releasing the load key completes the set of the 'IMPL cycle lth' which resets 'IMPL pressed lth' and drops system reset.



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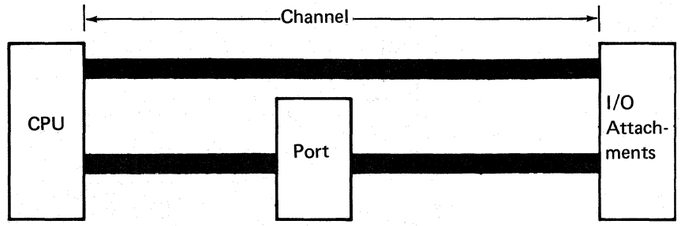
Channel

The channel transfers data and commands between the CPU, main and control storage, and all I/O devices. It also provides data buses and synchronizing controls to complete transfers between I/O attachments, CPU, and storage.

The channel has some lines that go directly from the CPU to the I/O attachments and some lines that go to a port.



Channel, as used in this system, refers to the internal interface between the processor and logic for control of I/O functions. The channel contains a port through which part of this control passes.

Channel Interfaces

The channel has three unique interfaces as follows:

1. Main and control storage through CPU data flow.
2. CPU data flow and LSRs.
3. Disk storage.

These interfaces provide all necessary controls to support the following:

1. I/O instructions.
2. Micro interrupts (two levels).
3. Disk.
4. Error logging.
5. Timing and control lines.

Main/Control Storage Through CPU Data Flow Interface

The channel gates the data from the CPU to the port and subsequently to the I/O attachment. Data to main/control storage from an I/O attachment is latched in the port and transferred through the CPU to storage. All storage addressing, storage write control, and address updates are controlled by the CPU.

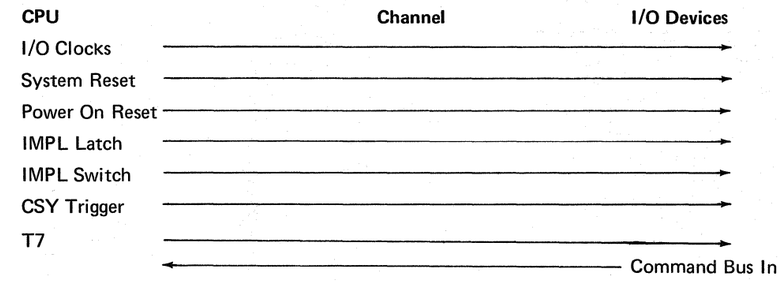
The data path of the port is 1 byte wide (8 data bits and 1 parity bit). The port provides all necessary controls to support I/O instructions, micro interrupts, and burst mode.

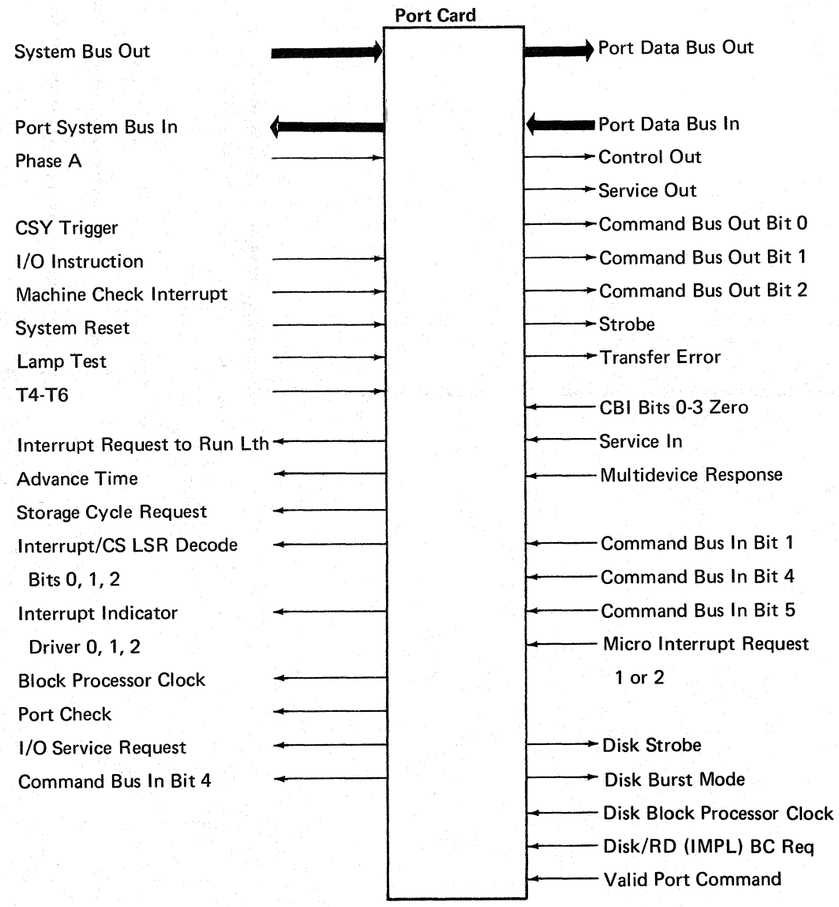
CPU Data Flow and LSRs Interface

The CPU interfaces with the channel directly when transferring data into or out of the CPU LSRs. The CPU handles all CPU LSR selector write controls directly from the I/O instruction fields. The channel gates data from the CPU LSR to the port and subsequently to the attachment.

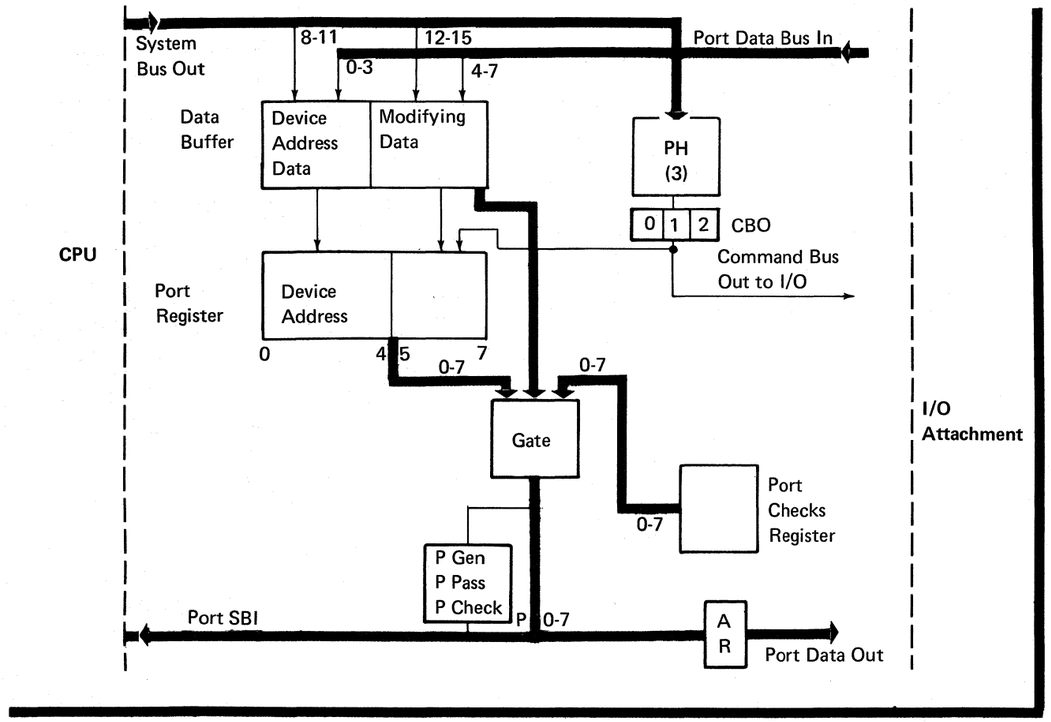
Disk Storage Interface

The CPU and the channel have the storage addressing, appropriate timings, and interlock controls to support the disk drive. This interface is internal to the CPU/channel/disk drive and is not available to any other devices in the system except during IMPL. The fast data transfer rates of the disk make this restriction necessary.

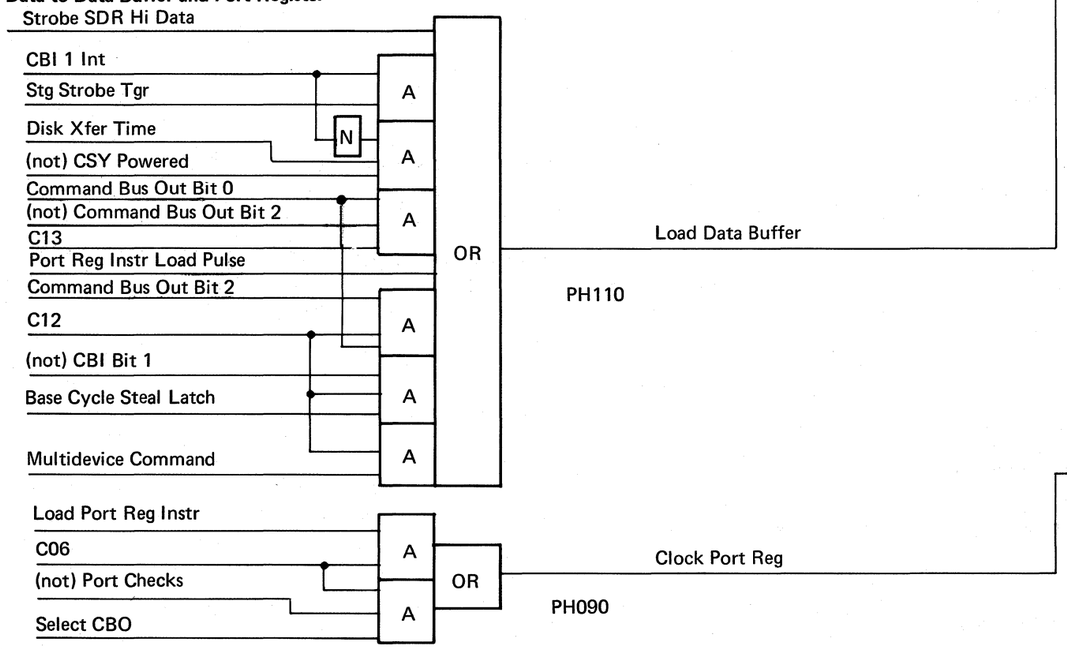


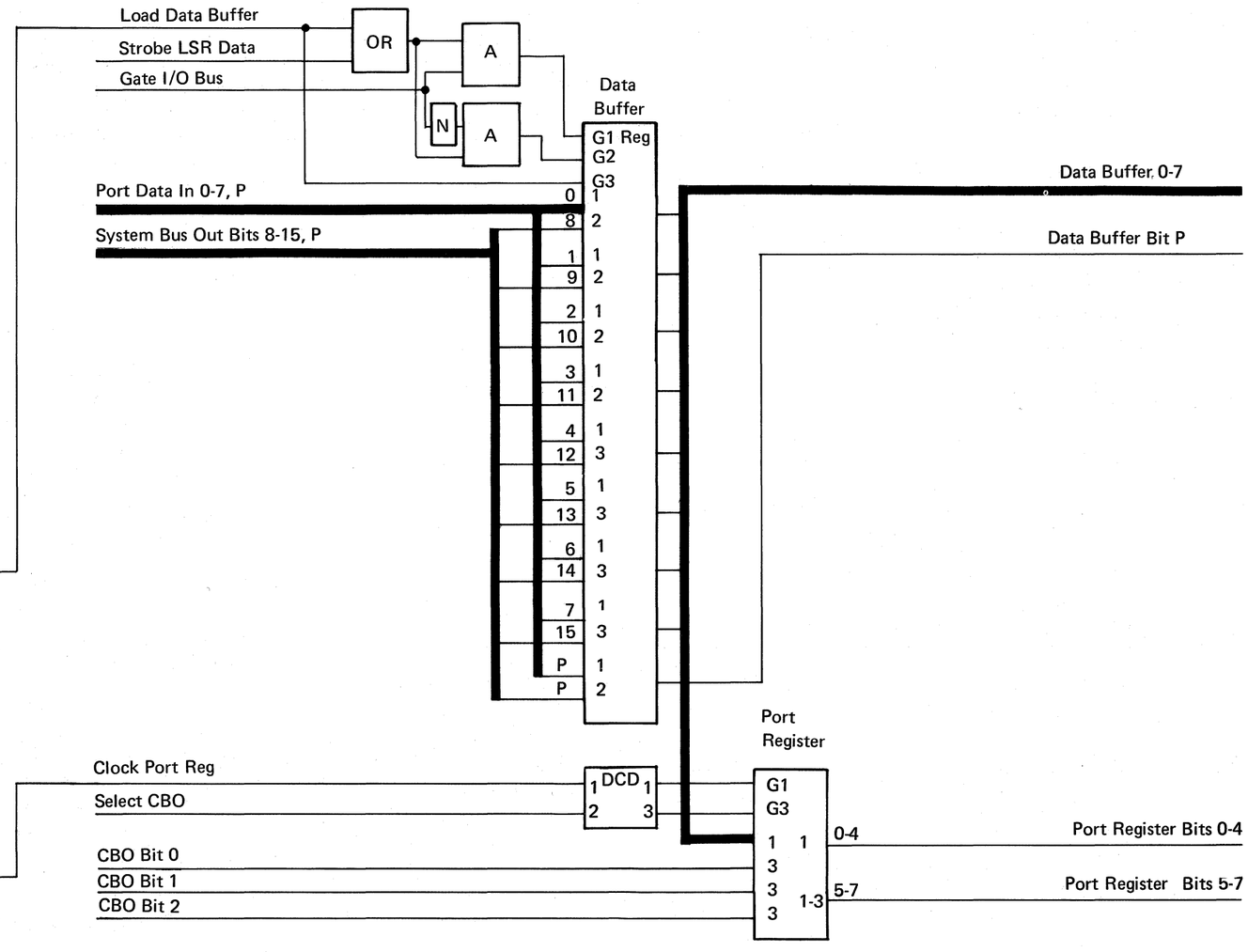


Port Data Flow

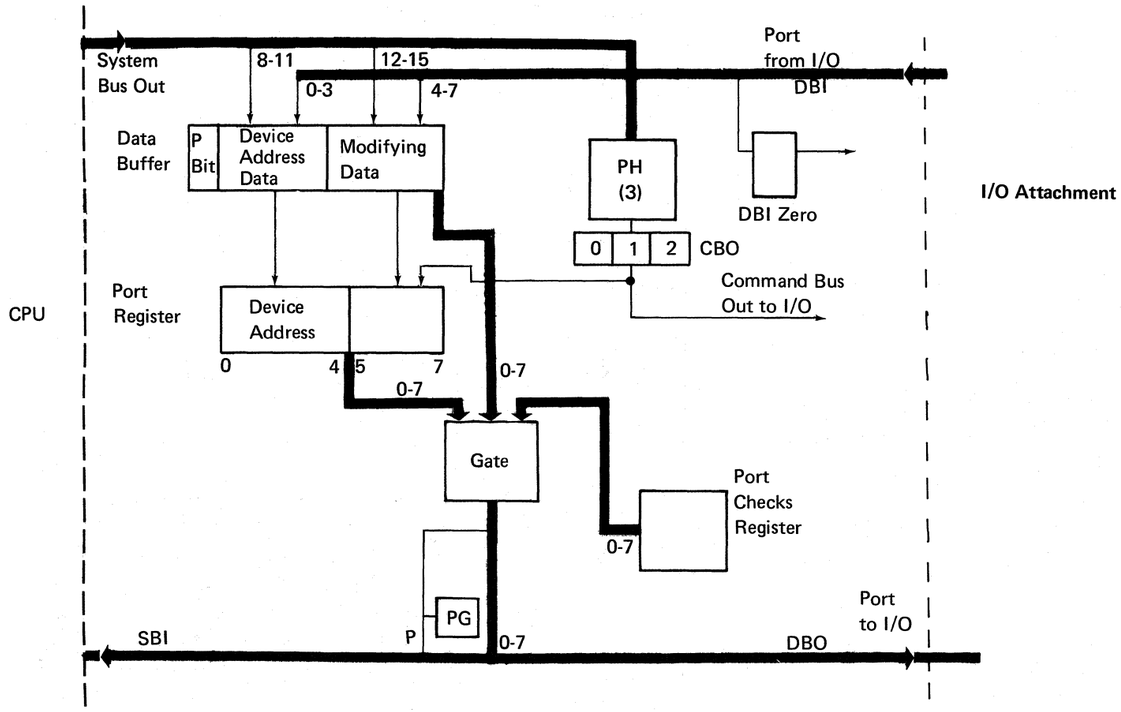


Data to Data Buffer and Port Register





Port Parity



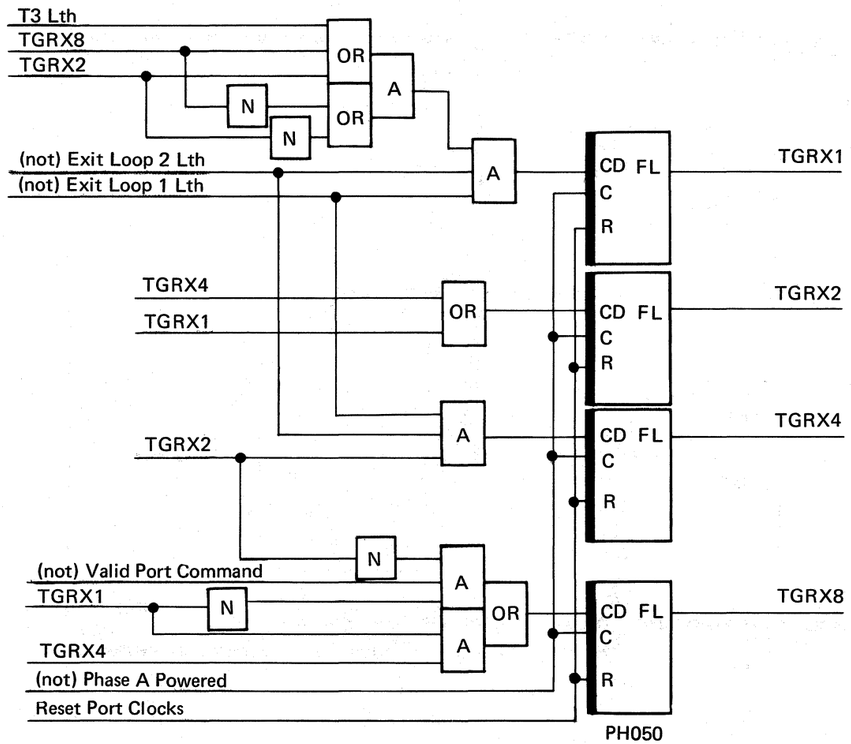
PG = Parity Generate
PC = Parity Check

The port normally operates in odd parity mode. For diagnostic purposes, the port (through an I/O control load) can be set to operate in even parity. In this case, data received from the CPU or I/O device is expected to have even parity. Because the CPU operates with odd parity, the port creates a CPU check when sending data to the CPU in the even mode of operation. System reset sets the port to odd parity (PH140).

Port Clocks

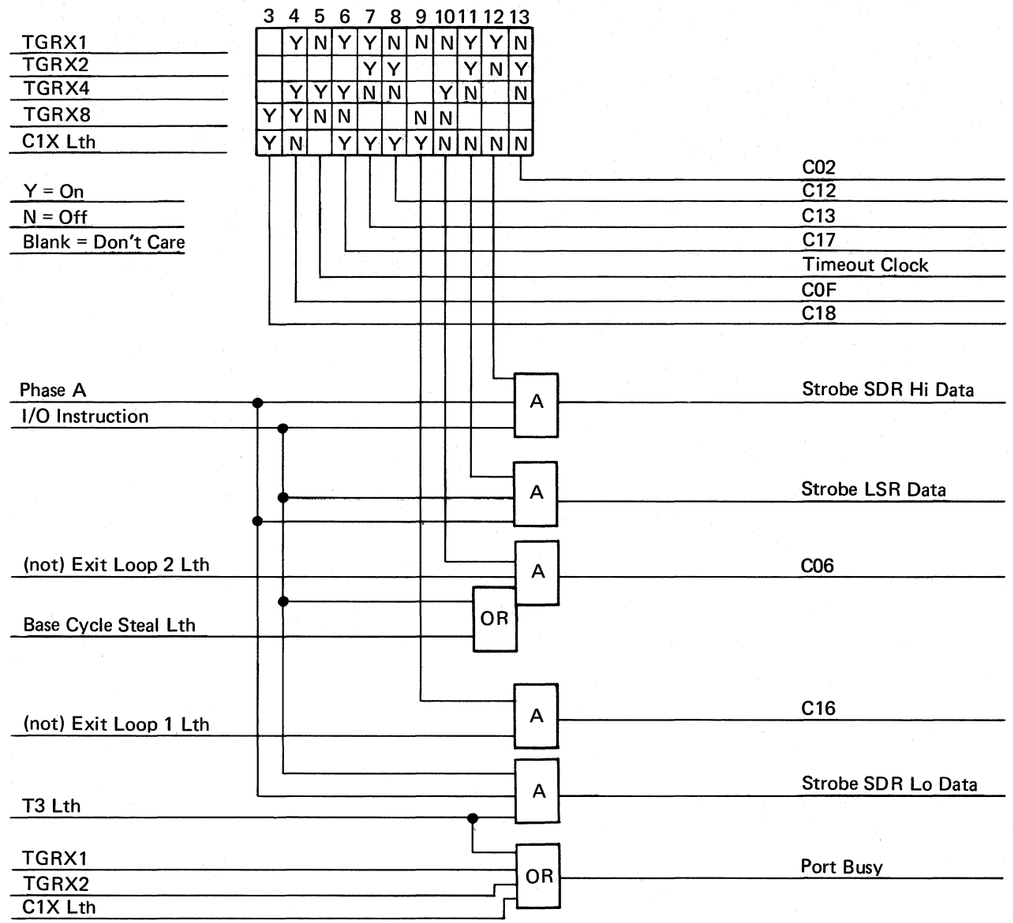
The port clocks generate the interface timings between the CPU and the I/O attachments. The port clocks run only for I/O instructions, otherwise, they are all reset. When the CPU decodes an I/O instruction, it raises 'I/O instruction' during T3; this line stays active through the end of T6. 'I/O instruction' causes the CPU clocks to extend T3 and simultaneously gates the port clock triggers, which are clocked by the shift of 'phase A'

Generation of Triggers



PH050

Generation of Port Clocks



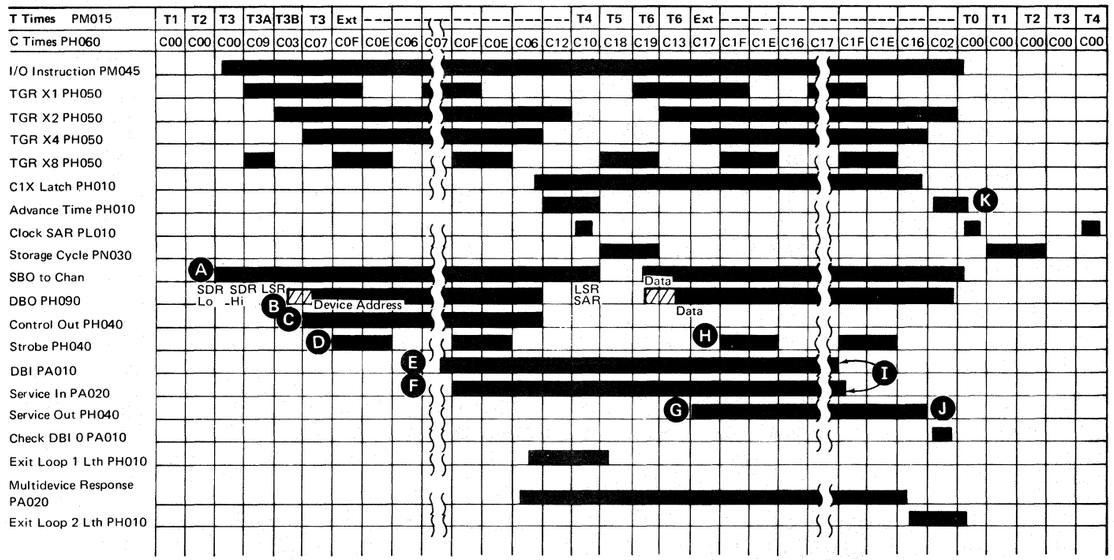
PH060

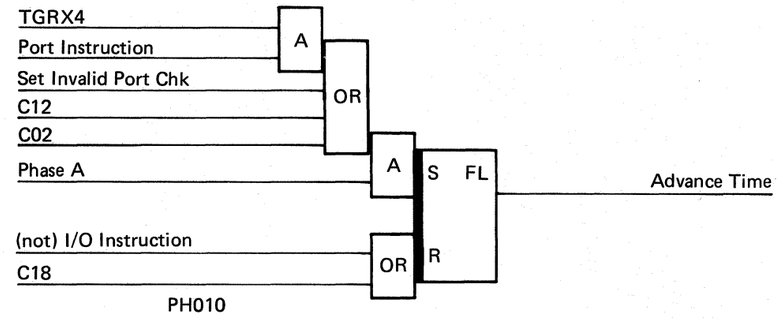
During the first three 200 ns increments of the extended T3 times, SDR low, SDR high, and the selected LSR low contents are gated to the port card **A** . During the succeeding T3 times, port 0 gates the device address out on the DBO lines **B** , raises 'control out' **C** , and sends a strobe line ('strobe') **D** out to the device attachment. When 'control out' is raised, the port clocks loop sending out strobe pulses (C07, C0F, C0E, C06, C07, etc) while waiting for the I/O device to respond (or until a timeout occurs).

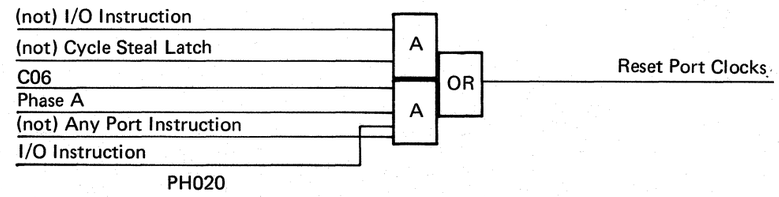
When the device responds, it places data on DBI **E** (or indicates it is ready for data) and raises 'service in' **F** ; the rise of 'service in' (or a timeout) advances the port clocks and the port raises 'advance time' to signal the CPU clocks to advance to T4. The system clock continues to advance normally to T6.

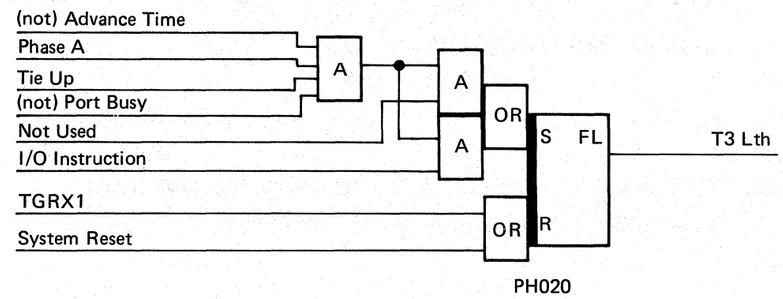
A similar situation occurs during T6. The port sends 'service out' **G** , which indicates either: data is ready to be sent, or data was received.

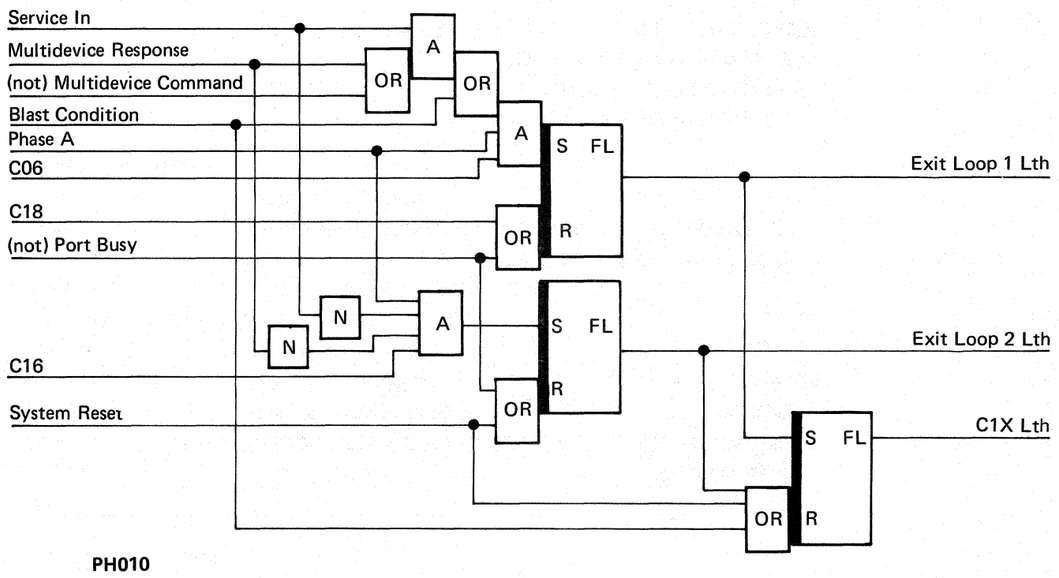
'Strobe' **H** is again sent for the I/O device to use. The port clocks loop with 'service out' active and strobe pulses continue to be generated while the port waits for the I/O device to respond (or a timeout to occur). The I/O device responds by taking the data off the DBI line (or if data was sent to the CPU, turning off DBI) and turning off 'service in' **I** . The port responds to advancing the port clocks to turn off 'service out' **J** and then raises 'advance time' **K** causing the CPU clocks to run again to T0.







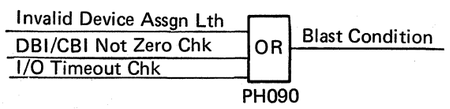




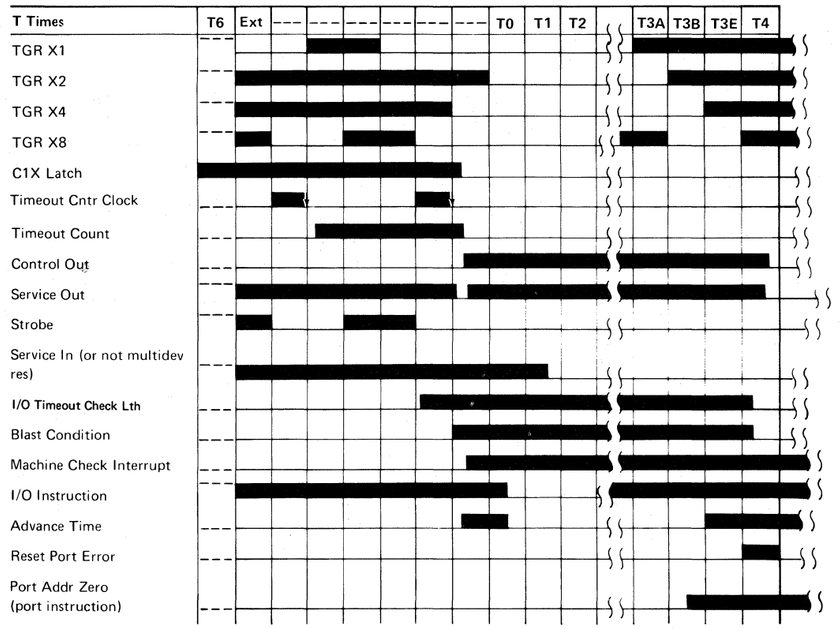
Blast Condition (PH090)

Blast condition causes all I/O devices to reset and the CPU to branch to the machine check interrupt routine. After dropping 'service out' the port checks to be certain DBI, CBI, 'service in' and 'multidevice response' are all shut off. If any of these is not zero, the port causes a blast condition by raising 'service out' and 'control out' simulanteously.

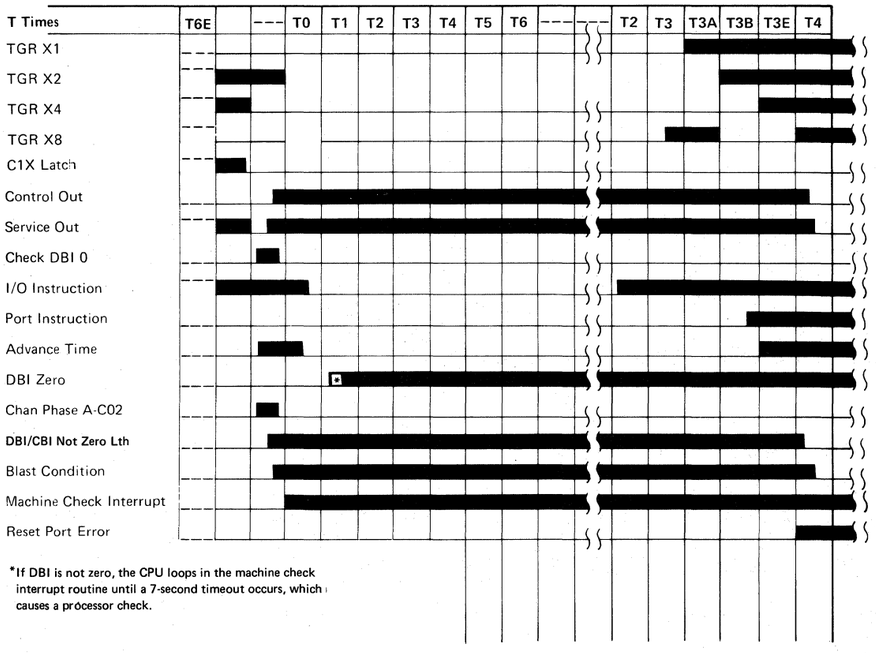
A blast condition is also generated if the I/O device addressed does not respond within 5.4 μs after 'control out' and 'service out'.



Blast Condition Due to Timeout Check

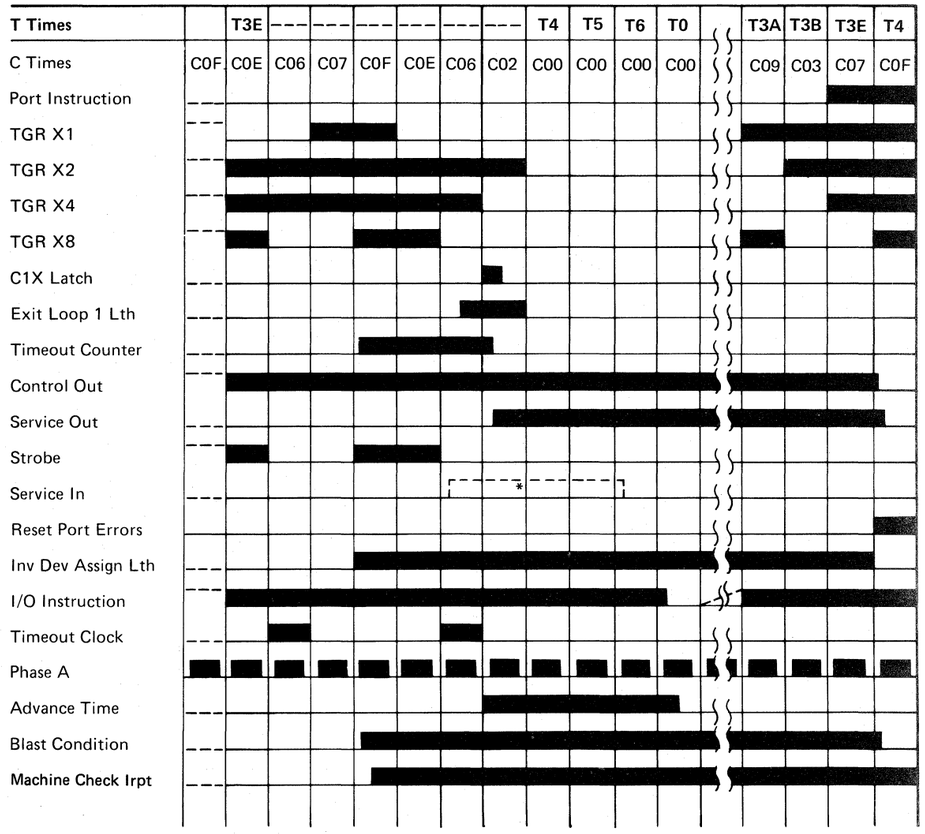


Blast Condition Due to DBI Not Zero



*If DBI is not zero, the CPU loops in the machine check interrupt routine until a 7-second timeout occurs, which causes a processor check.

Blast Condition Due to Invalid Device Assigned



*If 'service in' becomes active in this area, the blast condition will continue.

Controls

Control Out: rise indicates the data on 'port data out' and 'command bus out' is valid and can be sampled.

'Control out' together with 'service out' indicates a blast condition.

Service Out

Data to Port: tells adapter that port is finished with data and transfer can be terminated; 'service in' and input data can be dropped.

Data from Port: tells adapter that 'port data out' contains valid data and can now be sampled. When the I/O device drops 'service in', 'port data out' should no longer be sampled.

Strobe: comes up 200 ns after 'control out/ service out' and pulses with a period of 800 ns with an on duration of 400 ns until the rise or fall of 'service in'. Stops with rise or fall of 'service in' guaranteeing a full pulse width upon completion. Use of the pulse is device dependent.

If the device uses the line to generate 'service in', system operates in a synchronous manner.

The I/O devices use 'strobe' to generate appropriate data strobes and timing for loading information from the port and providing required timing to 'CBI/port data bus in' before the rise or fall of 'service in'.

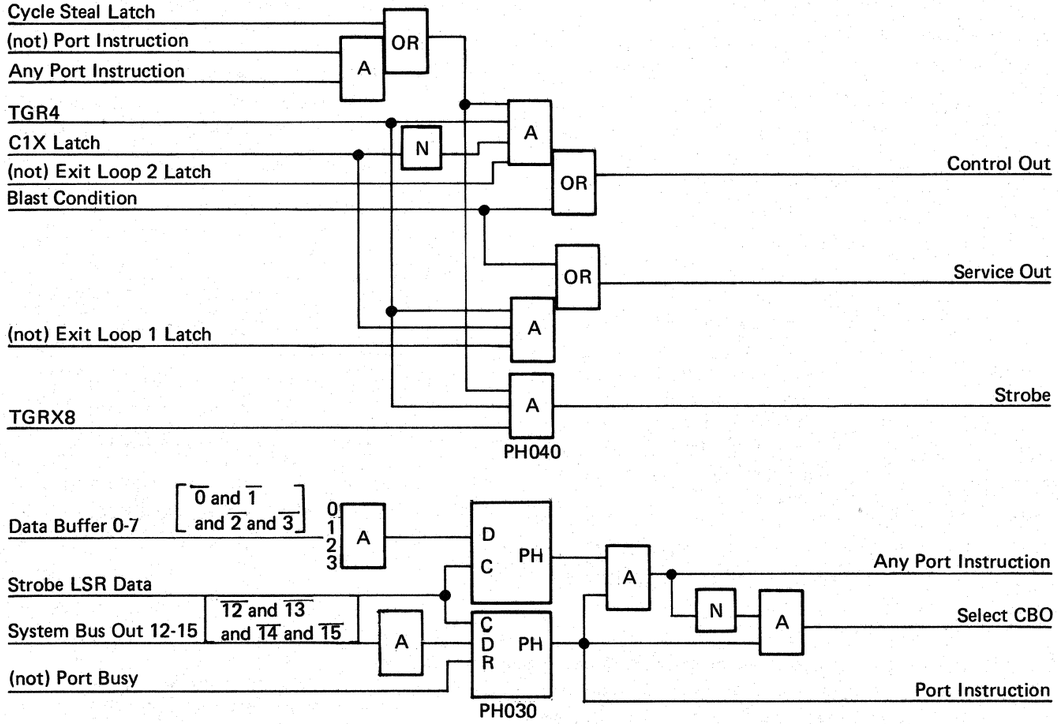
Data on 'port data out' and CBO remains valid from the trailing edge of the last 'strobe' for 100 ns. This allows the last strobe to be used for clocking.

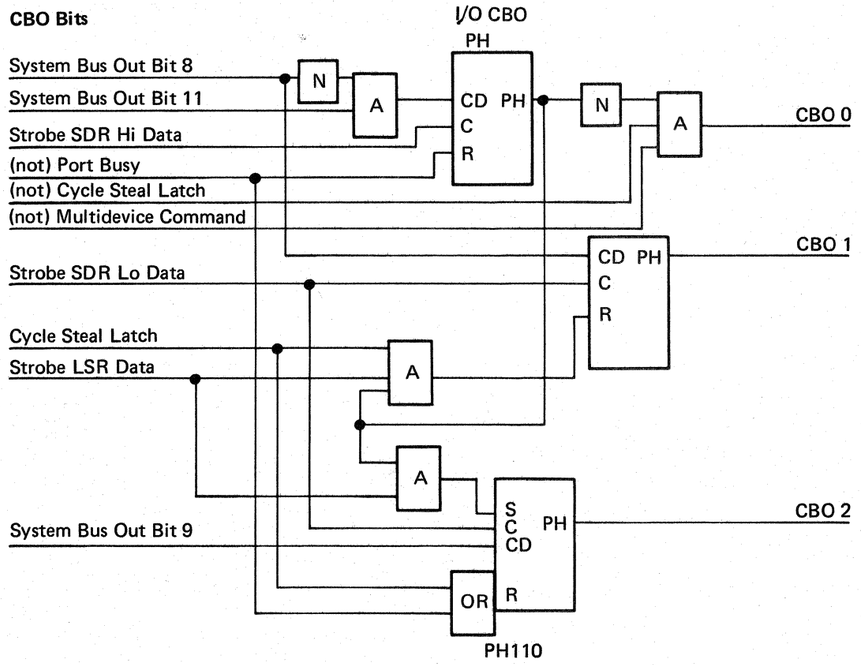
Command Bus Out: CBO is valid at the interface from the rise of 'control out' until the fall of 'service out' at the port interface. CBO, together with 'control out', indicates what data is on 'port data out'. The addressed attachment responds by raising 'service in' with the appropriate information gated on 'port data in' and 'command bus in'.

CBO bits are defined as follows:

0	1	2	
0	0	0	Unused
0	0	1	Sense interrupt status
0	1	0	Interrupt/burst mode response
0	1	1	Branch
1	0	0	Load
1	0	1	Sense
1	1	0	Control load
1	1	1	Control sense

Control Lines





I/O Instructions

The three micro instructions that communicate with the CPU, port, and the I/O attachments are:

- I/O Storage
- I/O Immediate
- I/O Branch

During execution of the I/O command, the CPU selects WR0(L) and sends its contents to the channel and thus to the port. The format of WR0(L) is:

0 3 4 7

Device	Address	
Port	0	0
Keyboard	1	0
Display Screen	4	0
MCU/MCR/Data Recorder	5	0
BSCA/SDLC	8	0
Disk Drive	A	0
33FD	D	0
Printer	E	0

The port links the instruction modifier field (bits 4-7 of the I/O instruction) onto the device address and transfers this information over the port interface to the appropriate attachment.

The port register stores the last CBO and device address issued by the port. This information is not destroyed after an error is detected and therefore can be sampled by the machine check interrupt routine to determine what device caused the check.

The port register is also used to read data from the LSRs or write data into the LSRs. When used in this manner, previous information about the device address and CBO is destroyed.

The CPU operates with odd parity; the port, however, can be set to either even or odd parity.

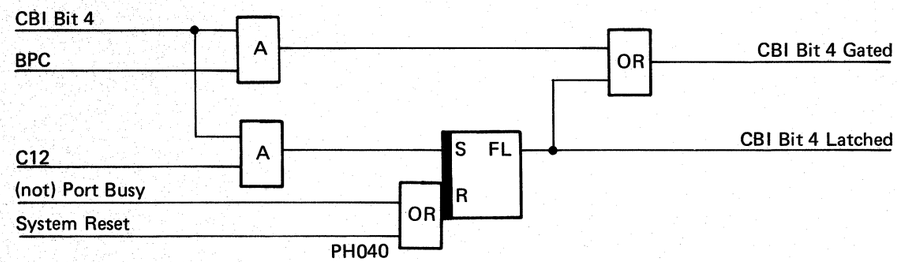
The attachments use 'CBI bit 4' for the following:

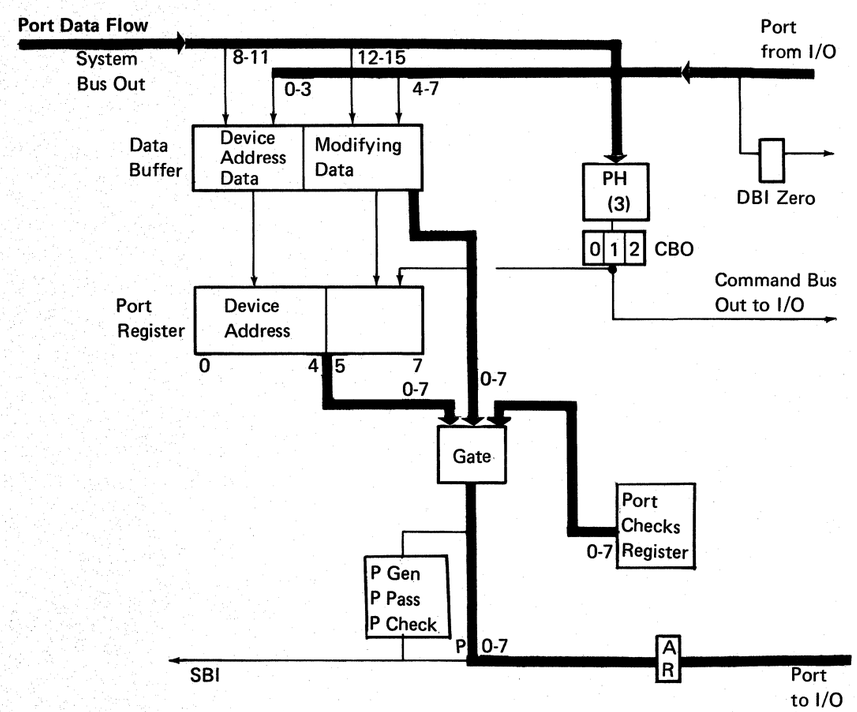
- Show that the condition tested by I/O branch on condition is met and that the CPU should take the branch.
- Signify invalid parity on DBO.
- Indicate to the CPU when to address control storage during a storage operation.

'Transfer error' is brought up from the CPU to show I/O branch echo met, that is, the CPU received CBI bit 4 correctly and the branch will be taken. This line is also used to indicate that invalid parity was detected during an I/O operation.

The following I/O immediate micro instructions are directed at the channel:

B 6 4 Reg	Sense port register
B 1 4 Reg	Sense port check byte
B 0 8 X	Disable 33FD timeout
B 1 8 X	Load port register
B 2 8 X	Reset port errors
B 3 8 X	Enable 33FD timeout
B 5 8 X	Set port odd parity
B 6 8 X	Set port even parity





Disk Drive Support

The system has a burst mode data transfer capability to support the high data rate of the disk drive.

The disk attachment raises 'FD block processor clock' (BPC) which forces the CPU to T7. (If the CPU is executing an instruction, T7 does not become active until the instruction is completed.)

'Command bus in' must be correctly set at T7 time. CBI controls selection of the LSRs which contain the address of the storage location; CBI bit 1 also controls the direction of data transfer. CBI bits also identify whether the data is to go into main or control storage, and controls incrementing of the storage addresses. Control storage locations are 2 bytes wide and main storage locations are 1 byte wide.

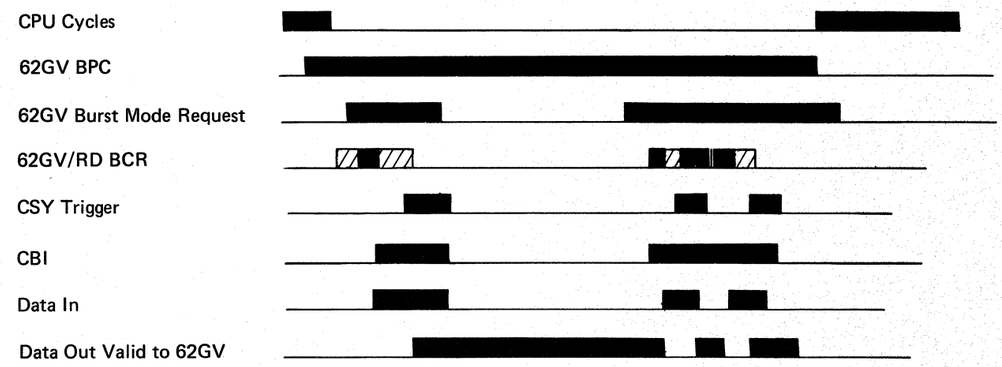
CBI Bit Description

Bits 0 1 2 3 4 5	
0 0	Burst mode sense—no increment
0 1	Burst mode load—no increment
1 0	Burst mode sense—increment
1 1	Burst mode load—increment
0 0	Burst mode LSR select 0
0 1	Burst mode LSR select 1
1 0	Burst mode LSR select 2
1 1	Burst mode LSR select 3
0	Main storage
1	Control storage
1	Port data bus out parity check

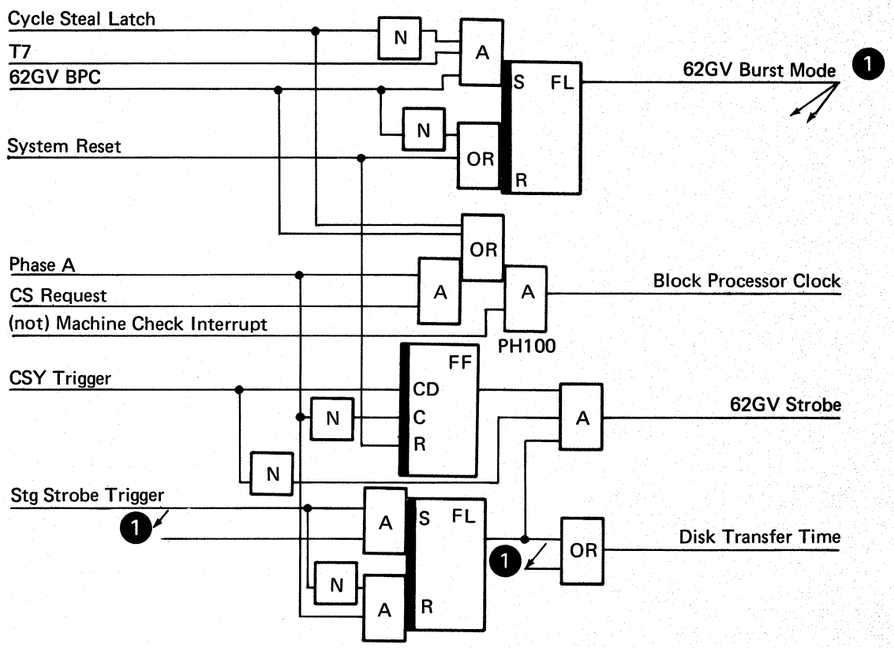
When T7 and 'FD burst mode' come up, the disk attachment raises 'FD burst cycle request' and loads the first byte of data onto DBI. The burst cycle request is granted and the rise of 'CSY trigger' gates the data into the data buffer. This data is gated onto 'system bus in' and from there into the storage address indicated by SAR. Each time 'burst cycle request' is raised, a byte of data is transferred. If 'FD burst cycle request' is kept active, the CPU continues to take storage cycles at the maximum data transfer rate.

During data transfers to disk, 'FD strobe' clocks the data from the port data buffer into the data buffer in the disk attachment. The disk attachment then writes the data on the disk.

Disk Drive Support Timing



Disk Drive Support Lines



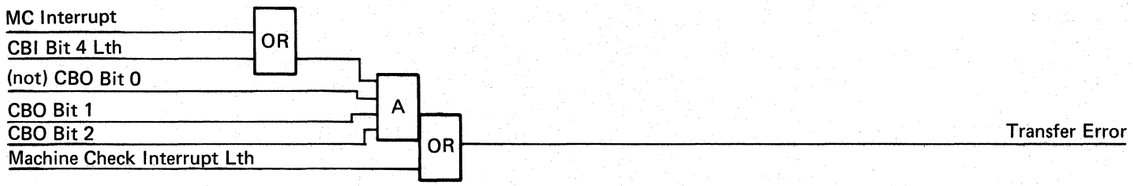
Port Checks

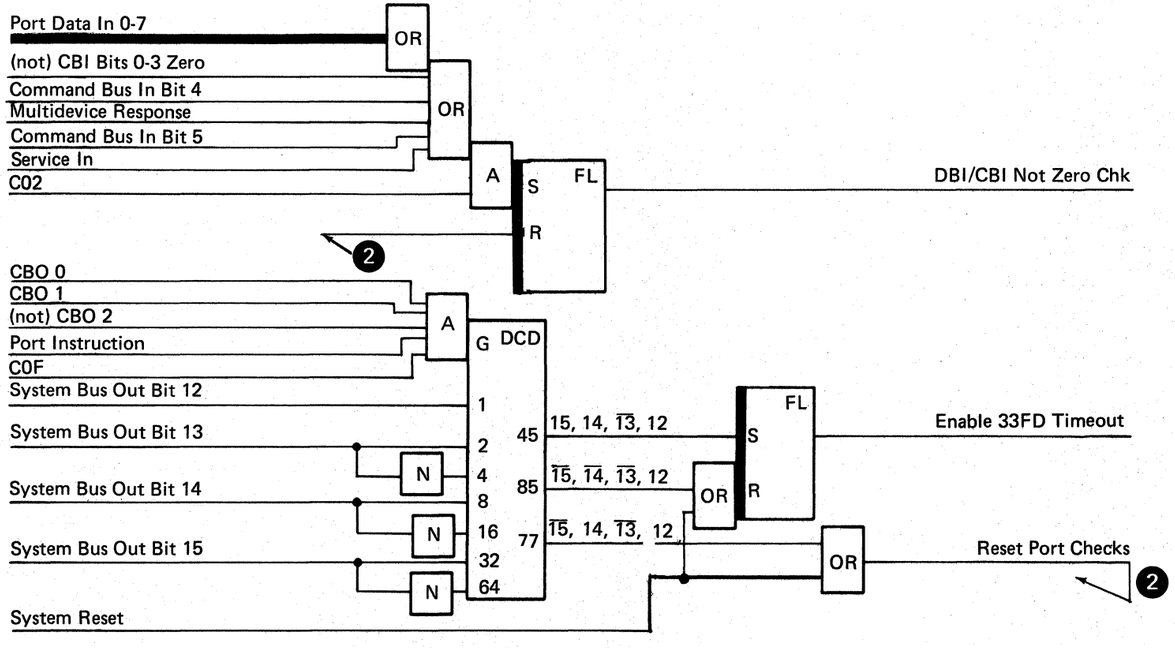
Port associated errors are logged in main storage by the machine check interrupt routine. Retry of the instruction that caused an error condition is executed whenever possible.

Intermittent device errors are cleared by the port blast command. The devices are informed when a transfer error has occurred. This information is stored in the device sense byte. Error conditions detected by the device (for example, invalid command) are also included in sense byte information.

Transfer Error: Indicates to the adapter that invalid parity was detected in port or in the CPU.

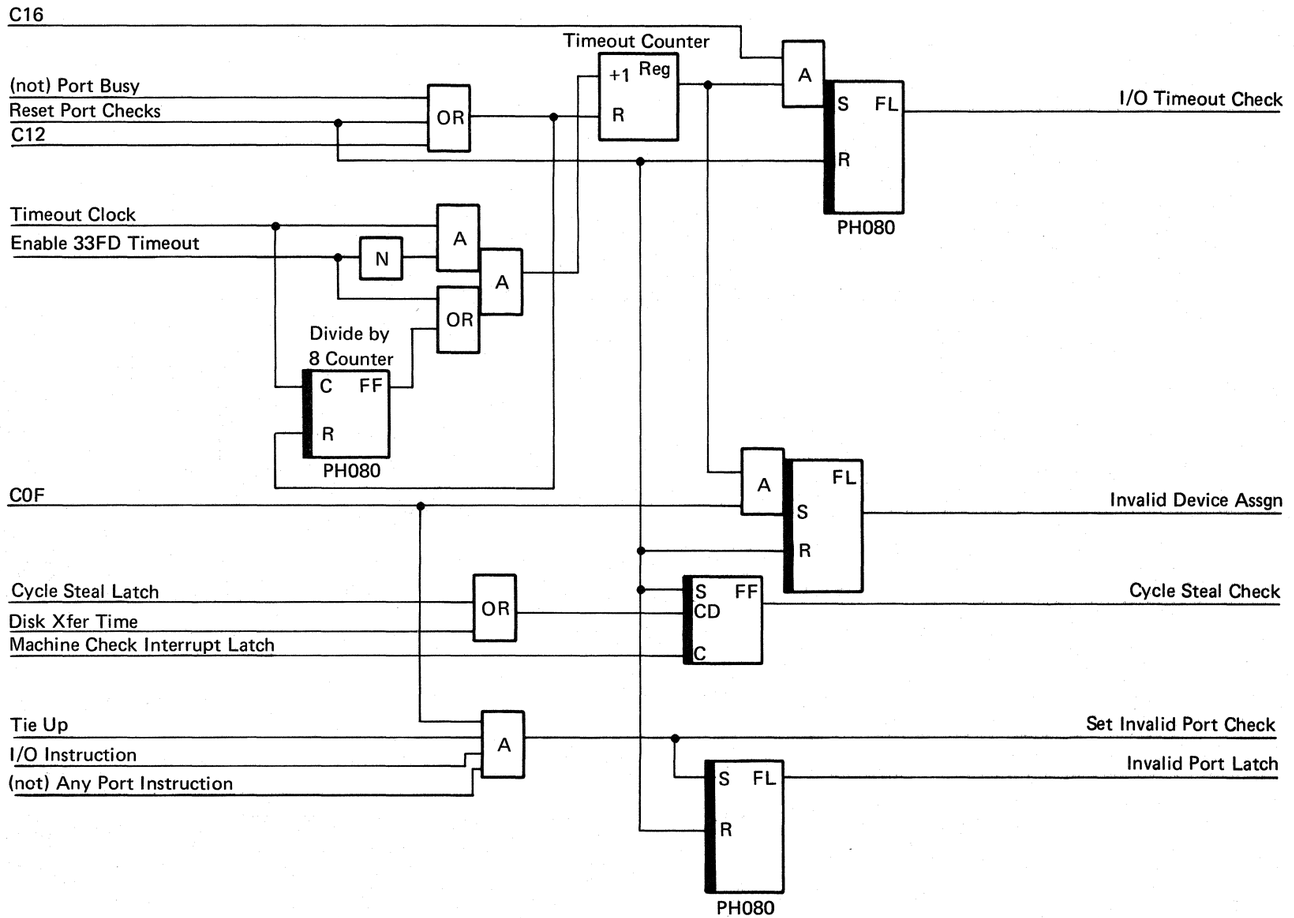
Transfer error is also used to indicate I/O branch met echo that tells the adapter that the port received the I/O branch met (CBI bit 4) and the branch will be taken by the CPU. This enables testing of asynchronous I/O device conditions with the I/O branch instruction and does not require the adapter to latch this line prior to raising 'service in'.





Timeout Conditions: If the device addressed is not on the system or port data out contains bad parity, none of the devices answer the 'control out' sequence. Port times out under these conditions. At the completion of the timeout sequence, the timeout condition is posted in the port status registers. . A blast is sent from the port and clears all inbound data and control lines from the I/O adapters and causes a machine check interrupt.

If the device addressed initially responds with 'service in' but fails to drop 'service in' within a predetermined time after receiving 'service out', the port times out. This condition is posted in the port status register and the port creates a blast condition, which clears all inbound data and control lines and causes a machine check interrupt.

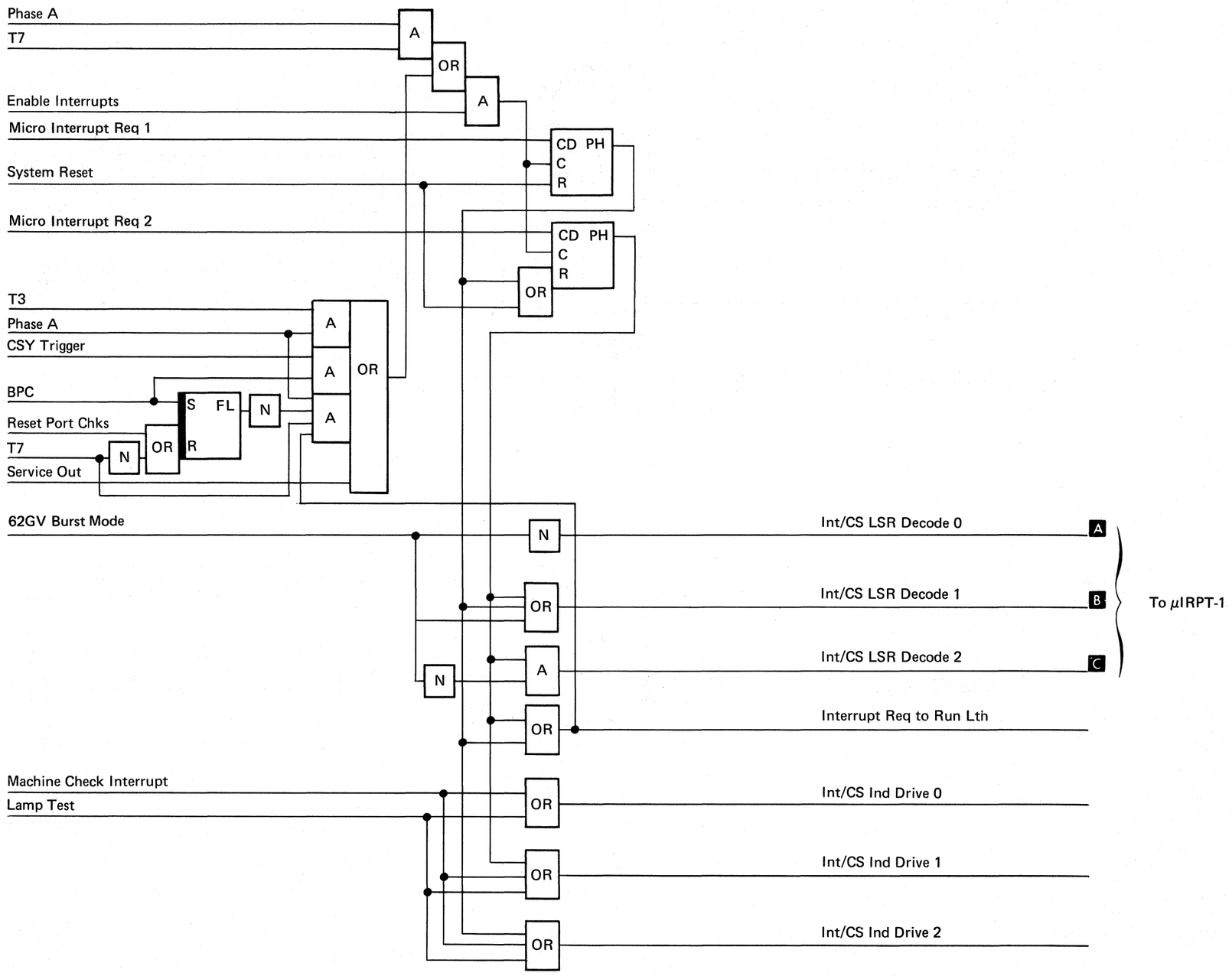


LSR Selection

Interrupt/CS LSR decodes 0, 1, 2 are used to control LSR selection bits 0, 1, 2 during instruction and burst mode processing. These lines allow selection of one of the four groups of registers dedicated to micro interrupts and burst mode.

The 'interrupt/CS indicator drivers' are used to display the active interrupt as the system is running.

'Interrupt request to run latch' is used to take the CPU out of the 'wait' state (created by the processor wait instructions) whenever a micro interrupt request is detected by port.



Micro Interrupts

The channel has three levels of micro interrupts; the priority is set by hardware. Interrupt level 0 has the highest priority. All I/O devices that require processing generate a micro interrupt to the system. The system receives the interrupt through the port. The interrupt levels and the devices on each are:

Interrupt Level	Description
0	Machine check
1	Disk drive
2	Keyboard, BSCA, Printer
3	MCU, Magnetic character reader or Data Recorder (optional features)

If none of the above interrupt levels are active, micro instructions are processed from the main level MAR.

Each interrupt level has a unique set of registers in their LSR stack; machine check interrupt and the main level microroutines use the same set of registers. Each set of LSRs consists of:

Eight 16-bit work registers (WRs)
One MAR
One MAB

Having a unique set of registers for each interrupt level means that no data loss occurs when a higher level interrupts a lower level. After the higher level is reset, the microprogram returns to the lower level taking the data out of the registers.

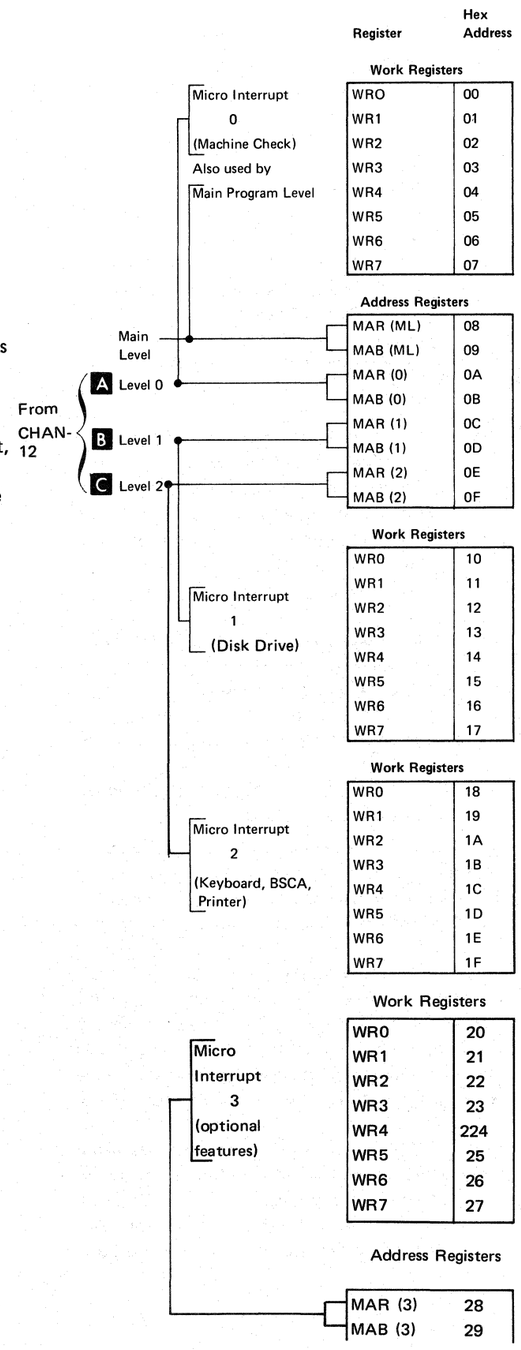
The entire system uses the same processor condition register, therefore, the PCR must be saved when entering the interrupt routine, and then restored when leaving the interrupt routine. This save/restore process assures that the contents of PCR are correctly associated with the level of processing. (If the micro interrupt routine does not alter the PCR, then the save/restore is not necessary.)

When the port senses the micro interrupt, either complete service may be initiated, or service may be posted until the system can conveniently handle the request without affecting system throughput. Therefore, microprocessing of interrupts can be grouped into two classes:

1. Immediate Action: Any device or system condition that requires attention because of critical response times is handled immediately. The microroutine services the request until it is complete or to a point that the critical response is complete and service can be continued at a time when system facilities become available. Examples of this class of microprograms are machine check and disk interrupt routines.

2. Delayed Action: After servicing the interrupt, the microprogram determines that complete service can be temporarily postponed because of noncritical response time for the device; that is, the device is probably unable to cause another request during the time that it takes to execute a system instruction. Therefore, the interrupt request is posted and service is delayed until the completion of the current system instruction.

LSR Stack



Level 0—Machine Check Interrupt

Machine check interrupt occurs whenever one of the following is detected:

- A parity check (SDR, SAR, STG gate, MOR, or ALU gate),
- An invalid address (main or control storage),
- A port check, or
- A micro instruction loop timeout.

MCI brings up 'machine check interrupt' from the CPU to the port which stops all I/O functions.

A machine check interrupt has priority over all other interrupts. The work registers (WRs) used by the MCI are the same ones used by the main program level (LSRs 0-7).

The machine check interrupt routine places the following information in control storage and then logs this information on one sector of the disk.

WR0 Main Level
Port Check Byte/Port Register
CPU Error Byte/Console Status Byte
MAR Interrupt Level 1
MAR Interrupt Level 2
MAR Interrupt Level 3
MAB Main Program Level
MAR Main Progam Level
Instruction located at MAR-1
Date

The four most current errors are stored on the four sectors reserved for this purpose.

This information is taken from control storage and logged on the disk at the time retry occurs. By having this information in control storage, it can be displayed if the disk drive is not working.

After the error information is logged on the disk, the machine check interrupt routine retries the current operation at the system level whenever possible.

The machine check interrupt causes a program check when the interrupt is caused by an invalid main storage address. The machine check interrupt routine provides this information to the system control program when program checks are handled.

Levels 1, 2, and 3-Disk Drive, Printer Keyboard, BSCA/SDLC, and Mag Card Unit, Magnetic Character Reader, or Data Recorder

Level 1 is dedicated to the disk drive. The micro interrupt request is normally processed as an immediate interrupt. (See *Disk Drive Support* for further description of burst mode.)

On level 2, the devices have noncritical response times compared to system instruction execution times. Thus, processing of the conditions which initiated the micro interrupt are delayed until the completion of the current system instruction.

When a micro interrupt occurs on level 2, the micro interrupt routine first does a multidevice sense interrupt status command. Each device has a preassigned bit on the data bus in; this bit is activated by the interrupting device during the multidevice sense interrupt command. The microroutine branches to a posting routine because no level 2 device requires immediate attention.

On level 3, the devices have response times that require immediate processing. Thus, the conditions that cause a level 3 interrupt must be serviced on that interrupt level.

Since the devices that are on level 3 (Mag Card Unit or Data Recorder) are mutually exclusive, a sense interrupt level status byte is not required to determine which device caused the interrupt.

The micro interrupt routine for levels 1 and 2 performs the following functions:

1. Stores PCR
2. Initializes PCR
3. Interrupts service routine
4. Restores PCR
5. Resets micro interrupt

The micro interrupt routine for level 3 performs the following functions:

1. Stores PCR [WR1 (H) is dedicated on level 3]
2. Tests for the proper code in the transient area
3. Branches to the transient area entry address
4. Restores the PCR
5. Resets micro interrupt

A device initiates an interrupt by raising micro interrupt request through its adapter whenever that device requires program interaction.

The lines 'interrupt/burst mode LSR decode 0, 1, 2' control LSR selection bits 0, 1, and 2 during instruction processing. These lines select one of the four groups of registers dedicated to micro interrupts.

The 'interrupt indicator drivers' display the active interrupt level to the operator as the system is running.

The interrupt levels are sampled during T3 times. The interrupt request signal to the CPU is inhibited when the CE mode switch is not turned to PROCESS.

Posting Interrupt Requests

In the fixed area of control storage, two reserved locations are used as posting words as follows:

Location 007E

Control storage interrupt level status word (CSILSW)

Bit 0 Transient I/O Features
1 Keyboard (I/O control)
2 Printer (I/O control)
3 Disk IOS (I/O control)
4
5 Trace instructions
6 Machine check logout
7 Inquiry
8 through 15—Must be zero

Location 007F

System interrupt level status word (S3ILSW)

Bit 0
1 Keyboard
2 BSCA/SDLC
3
4
5
6
7
8 through 15—Must be zero

A posting routine is executed as part of a micro interrupt routine, an SCP routine, or as part of a system I/O instruction; the routine consists of setting the appropriate bit to a one in either of the above two words.

The posted requests in the I/O device post locations are serviced between system instructions, and the system interrupt level status words posted requests are serviced after the I/O device post requests are complete. That is, the I/O post requests have priority over the system status words.

If a system interrupt is already in process, it must be completed before another system interrupt can be started. The only exception is program check which can interrupt a system interrupt routine.

Interrupt Interface

At the completion of a system instruction, the microroutine tests the service request flag. If it is found on, the microprogram branches to the I/O post routine and any posted bits are serviced until the I/O post word becomes zero.

The microprogram then tests the console functions (SYS INSN STEP, START, STOP) to determine if any of these functions caused the service request flag to come on. If STOP has been pressed, the system branches to the microstop loop. This loop allows micro interrupts to occur and I/O post word routines to be operational.

If none of the console functions was invoked, the microprogram continues and determines if the SCP is already servicing system interrupts. If they are being processed, INTBUSY bit at $INTLVL (location 0072 of direct area of control storage) will be a one. If this bit is zero, the system interrupt level status word is tested for any bit on. If found, a branch and link SCP interrupt is executed and control is passed to the SCP interrupt handler.

The SCP interrupt handler examines the S3ILSW to determine priorities if more than one bit is on. It then sets INTBUSY at location $INTLVL to a one to signal the system interrupt test routine to continue with main level processing. When the SCP examines the S3ILSW for a bit, it includes the following instruction steps:

1. Mask micro interrupts.
2. Test for S3ILSW bit on.
3. Reset bit and restore S3ILSW to control storage.
4. Unmask micro interrupts.

The SCP also includes instructions to save the main level system registers (IAR, PSR, XR1, XR2, ARR) in the control storage and replace them with the contents of the interrupt level system registers that are to be used when processing the detected interrupt.

When all system interrupts are processed, the main level system registers are restored, the flag bit at location $INTLVL should be set to zero, and a return instruction executed. The return instruction causes the main level program to continue at the system instruction that was being executed before the system interrupt was taken.

Micro Instructions

The System/32 microprogram has the following functions:

- Read, decode, and operate on system instructions and data located in main storage.
- Handle I/O operations for the system attachments.
- Handle console operations.
- Perform diagnostic operations.
- Perform some SCP functions.

The microprogram is composed of microroutines, each of which performs a specific function in the system operation. The execution of each function requires many steps in the microroutine. These steps are micro instructions that are read out and executed in a particular sequence. To change the execution sequence, a branch and link instruction stores a link address in a backup register. This is the address of the next micro instruction that would have been executed had the branch and link function not occurred.

Each micro instruction is a bit-significant word (16 bits) that represent a machine instruction. This instruction has specific fields defined for controlling data flow of the system. A zone digit is the hex value represented in the high 4 bits of a byte (bits 0-3). A numeric digit is the hex value represented in the low 4 bits of a byte (bits 4-7).

System/32 has 19 micro instructions. Bits 0, 1, 2, 3, (and sometimes bits 8 and 12) of the instruction identify the type of instruction. The significance of the remaining bits is unique to the instruction.

The 19 micro instructions are:

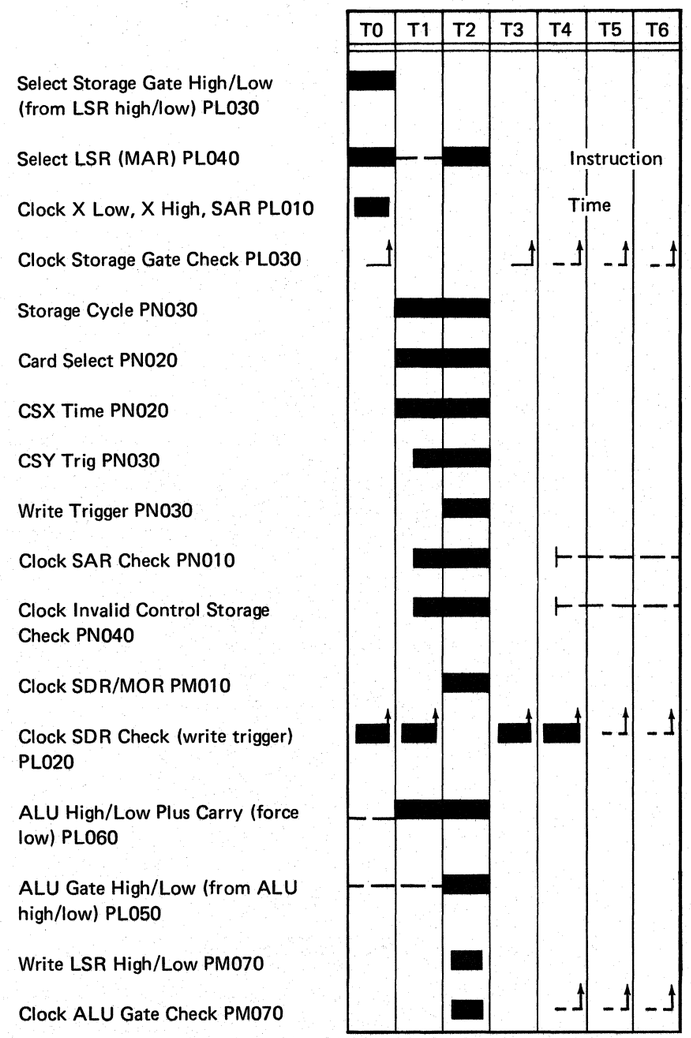
Branch
Branch and Link
Branch On Condition
I/O Branch On Condition
I/O Storage
Storage
Test Mask
Logical/Arithmetic 1
Logical/Arithmetic 2
Set Off
Set On
Immediate
I/O Immediate
Compare Immediate
Subtract Immediate
Storage Direct
Move Local Storage Register
Hex Branch
Hex Move

Micro Instruction Fetch

During micro instruction fetch, the storage gates are selected from the LSR MAR. This data is clocked into SAR and into the ALU. The 'carry in' line comes up which adds one to the data going through the ALU (address from MAR). Thus the data gated through the ALU and back into the LSR is the new address for the next fetch.

Micro instructions are executed in two phases, a fetch phase and an execution phase.

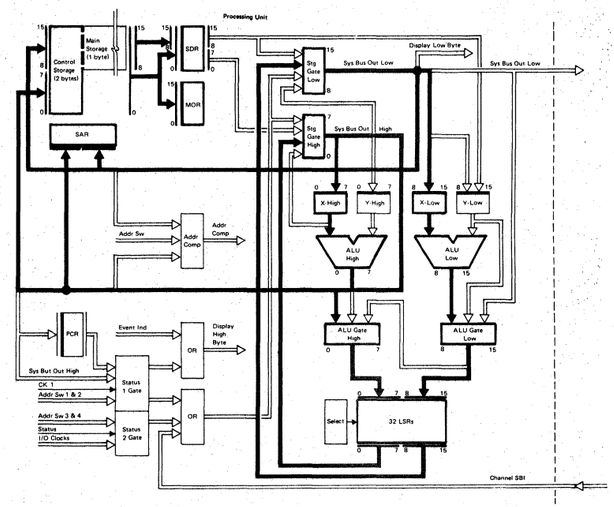
Timing of CPU Functions

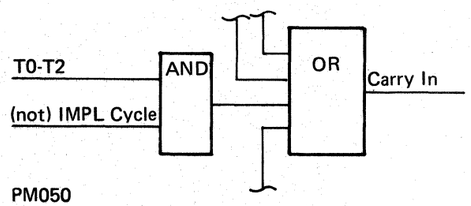


↑ means that check is done at that time.

- - -↑ means line is up but not used.

Specific CPU Data Path





Microlisting

Microroutines are printed out on a micro-listing. The fields are explained here:

Module Names

Name	Function
$AD1	Alter/display transient
$ALT	Alternate sector transient
$EOJ	End-of-job transient
$I11	33FD transient
$MP1	Matrix printer
$CDA	KYBD XLATE
$CFM	Cut forms (matrix)

Module Name

Microroutine Name

```
IBM 5320 CONTROL PROGRAM $MP1-17        PART NO. 2547056   EC NO. 825410    DATE 30DEC74   PAGE     6A
$MP1    MPCARR@@ -- MATRIX PRINTER MICROCODE
 LOC   OBJ    STMT SOURCE STATEMENT            COPYRIGHT IBM CORP 1974

                3151 ************************************************************************
                3152 *    ENTRY POINT IF R BYTE OF 1 SHOULD BE FORCED                       *
                3153 ************************************************************************
0738            3154 PTCARRS1 EQU   *
0738 A601       3155          LI    WR6(L),1            FORCE R BYTE TO 1
                3156 ************************************************************************
                3157 *    MAIN ENTRY POINT, INCLUDING INITIALIZATION OF PARAMETERS AND      *
                3158 *    DETERMINATION OF THE REQUESTED OPERATION.                         *
                3159 ************************************************************************
0739            3160 PTCARR@@ EQU   *
0739 A748       3161          LI    WR7(L),X'48'        ASSUME DISABLE EOF SWITCH
073A 9820       3162          SBN   WR0(H),PTCGACTV     SET CARRIAGE BUSY AND INTRPT REQ
073B C600       3163          CI    WR6(L),0            CARRIAGE MOVEMENT SPECIFIED?
073C 2658       3164          JZ    PTCARR04            NO
073D E23F       3165          L     PTFLCL,WR2          FETCH LINE POSITION & FORMS LENGTH
073E E43F       3166          L     PTFLCL,WR4          LOAD UP WORKING COPY
073F 5102       3167          TM    WR1(L),PTIOBFSK     SKIP OPERATION?
0740 2448       3168          JO    PTCARR00            YES-PROCESS THE SKIP

                3170 ************************************************************************
                3171 *    SPACE OPERATION PROCESSING                                        *
                3172 ************************************************************************
0741 C603       3173          CI    WR6(L),3            IS THE # OF SPACES SPECIFIED > 3?
0742 2458       3174          JP    PTCARR04            YES-NO SPACING
0743 6286       3175          AR    WR2(L),WR6(L)       ADD # OF SPACES TO CURRENT LINE
0744 6CC2       3176          SR    WR4(H),WR2(L)       DID SPACE GO PAST FORMS LENGTH?
0745 2454       3177          JP    PTCARR03            NO
0746 62CA       3178          SR    WR2(L),WR2(H)       YES-SUBTRACT FORMS LENGTH
0747 0752       3179          B     PTCARR02            ENTERING NEW PAGE,ENABLE EOF

                3181 ************************************************************************
                3182 *    SKIP OPERATION PROCESSING                                         *
                3183 ************************************************************************
0748 6CC6       3184 PTCARR00 SR    WR4(H),WR6(L)       LINE # > FORMS LENGTH?
0749 2558       3185          JN    PTCARR04            YES-NO SKIPPING
                3186 *         MVHR  WR2(L),WR6(L)       MOVE NEW LINE NUMBER
074A A200       3187          LI    WR2(L),0                CLEAR DESTINATION REGISTER
074B 62B6       3188          AR    WR2(L),WR6(L)           MOVE SOURCE TO DESTINATION
                3189 *** END OF EXPANSION **
074C 66C4       3190          SR    WR6(L),WR4(L)       CALC NUMBER OF SPACES TO NEW LINE
074D 274F       3191          JFLG  *+2 ----------+     SIO ENTRIES DO NOT SKIP IF RESULT=0
074E 0750       3192          B     *+2 ----------|--+  FUNC. KEY ENTRY WILL SKIP F.L. IF=0
074F 2658       3193          JZ    PTCARR04 <---+  |   NO SPACE REQUIRED
0750 2454       3194          JP    PTCARR03 <------+   LINE IS ON THIS PAGE-PROCEED
0751 66BA       3195          AR    WR6(L),WR2(H)       ADD FORMS LENGTH TO THE DISTANCE

                3197 ************************************************************************
                3198 *    ROUTINE EXIT POINTS                                               *
                3199 ************************************************************************
0752 D7F8       3200 PTCARR02 AI    WR7(L),X'08'        NEW PAGE,ENABLE EOF
0753 9880       3201          SBN   WR0(H),PTNEWPAG     INHIBIT ANY PRT OPS
0754 D6FF       3202 PTCARR03 AI    WR6(L),1            HARDWARE REQUIRES DISTANCE+1
0755 8886       3203          IOCL  WR6(L),X'86'        SEND # OF LINES TO PRINTER
0756            3204 PTCARR@N EQU   *                   ENTRY POINT FOR UPDATING PARAMETERS

$MP1    MPCARR@@ -- MATRIX PRINTER MICROCODE
 LOC   OBJ    STMT SOURCE STATEMENT            COPYRIGHT IBM CORP 1974

0756 EA3F       3205          ST    PTFLCL,WR2          STORE NEW LINE
0757 8C87       3206          IOCL  WR7(L),X'C'         SEND CRG CONTROL BYTE AS NOW DFND
0758 2F00       3207 PTCARR04 RETRN
```

Control Storage Address (2 bytes)

Machine Code

Statement Sequence Number

Source Statement:

Name Field—column 1, length 8
Operation Field—column 10, length 5
Operand Field—column 16, length 56 (if used)
Comment Field—column 40, length 32
Column 72 is blank
Asterisk (*) in column 1 indicates a comment
(see statement 3157 for example)

Micro Instruction Mnemonics

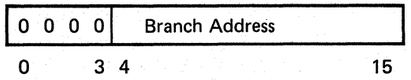
Micro Instruction	Mnemonic	Op Code
Branch	B	0
Branch and Link	BAL	1
Branch On Condition	JC	2
Branch On Carry	JCY	
Branch On High	JH	
Branch On Low	JL	
Branch On Equal	JE	
Branch On Positive	JP	
Branch On Negative	JN	
Branch On Mixed	JM	
Branch On Zero	JZ	
Branch All Ones	JO	
Branch On Flag	JFLG	
Branch Service Request	JSR	
Branch Not High	JNH	
Branch Now Low	JNL	
Branch Now Equal	JNE	
Branch Now Positive	JNP	
Branch Not Negative	JNN	
Branch Not Zero	JNZ	
Return	RETRN	
Branch On I/O Condition	JIO	3
I/O Load From Control Storage High/Low	WTCH/L	4 (Bit 8)
I/O Store to Control Storage High/Low	RDCH/L	
I/O Load from Main Storage	WTM	
I/O Store to Main Storage	RDM	
Load from Control Storage	LC	4 (Bit 8)
Load from Main Storage	LM	
Store to Control Storage	STC	
Store to Main Storage	STM	
Subtract Immediate	SI	D
Add Immediate	AI	D
Test Mask	TM	5
Logical Arithmetic 1	LA1	6
Logical Arithmetic 2	LA2	7
Exclusive OR	XR	
OR	OR	
AND Register	NR	
AND Complement	NCR	
OR Complement	OCR	
Decrement Register by 1	DEC	
Add Registers with Carry	ACYR	
Subtract Register	SR	
Add Register	AR	
Subtract with Borrow	SCYR	
Increment Register by 1	INC	

Micro Instruction	Mnemonic	Op Code
Set Bits On	SBN	9
Set Bits Off	SBF	8
Load Immediate	LI	A
Compare Immediate	CI	C
Sense Interrupt Level Status Byte	SILSB	B
I/O Load	IOL	
I/O Sense	IOS	
I/O Control Load	IOCL	
I/O Control Sense	IOCS	
Microprocessor Load	MPL	
Microprocessor Sense	MPS	
Microprocessor Load for Special Functions	MPLF	
Move LSR	MVR	E (Bit 8)
Load Direct from Control Storage	L	E (Bit 8)
Store Direct to Control Storage	ST	E (Bit 8)
Hex Branch Numeric	HBN	F (Bit 12)
Hex Branch Zone	HBZ	
Shift Right Logical	SRL	F (Bit 12)
Shift Right Logical Double	SRLD	
Shift Left Logical	SLL	
Shift Left Logical Double	SLLD	
Move Zone to Numeric	MZN	
Move Zone to Zone	MZZ	
Transfer	XFER	

Note: Notes in parentheses (for example: Bit 8) refer to bits that further differentiate instructions.

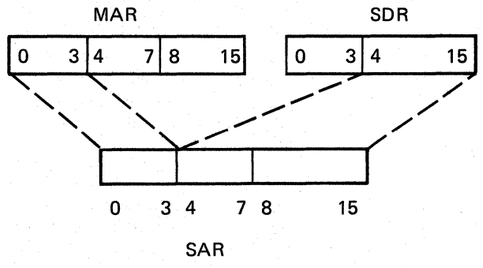
Branch

Mnemonic: B



The branch instruction is used for an unconditional branch to one of 4096 addresses in control storage only. During the first cycle, the branch address is placed in X high, X low, and SAR. During the next cycle, T0 is skipped so that no new LSR is selected, and X and SAR are not clocked again. The instruction is fetched from the address loaded into SAR during T3 of the first cycle. ALU gate high/low is gated during T2 time and the incremental address data is written into LSR high and low.

Branch Address: 12-bit branch address. These 12 bits and X high bits 0-3 replace the corresponding 12 bits in the storage address register (SAR). Hence, the branch address becomes the next sequential instruction. The microprogram address register (MAR) is then updated during T2 of the next cycle.



Condition Code

No change.

Timing of CPU Functions

Select LSR (MAR) PL040

Select Storage Gate High (from X high (0-3)/SDR (4-7)) PL030

Select Storage Gate Low (from SDR low 8-15)

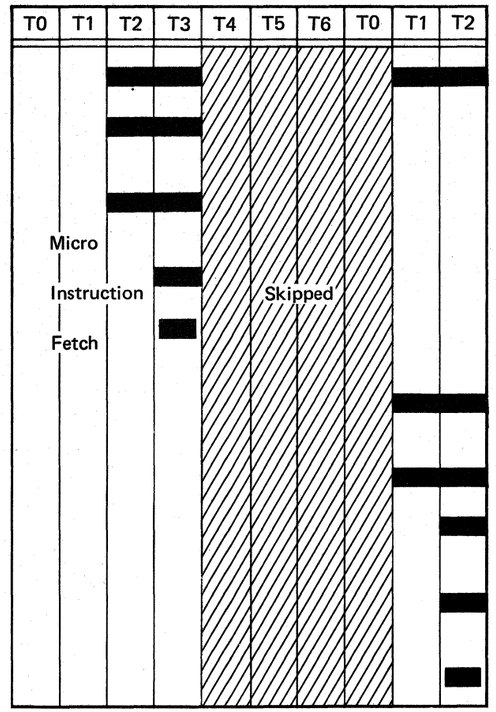
Advance Clock PH010

Clock X Low, X High, SAR PL010

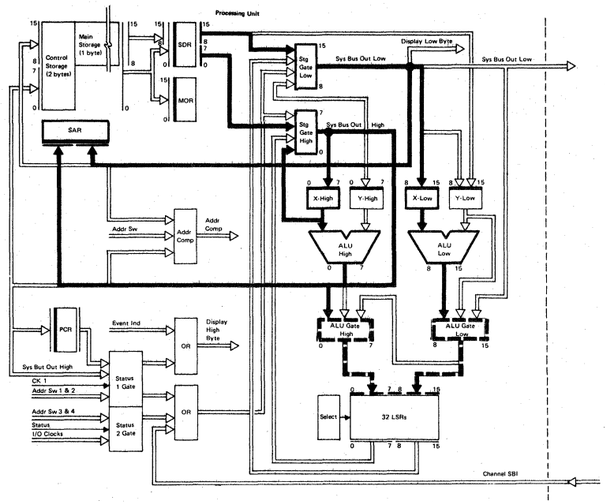
Second Micro Instruction Fetch:

- ALU High/Low Plus Carry (force low) PL060
- Storage Cycle PN030
- Clock SDR/MOR (write trigger) PL020
- ALU Gate High/Low (from ALU high/low) PL050
- Write LSR High/Low PM070

T-Times = 200 ns

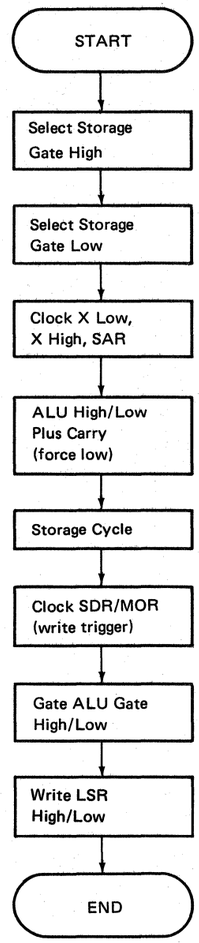


Specific CPU Data Path



Cycle One
Cycle Two
(second micro instruction fetch)

Sequence of CPU Functions



Branch (Stop Condition)

Clocks T4, T5, and T6 can be taken if the processor is executing a branch and the run latch is reset by:

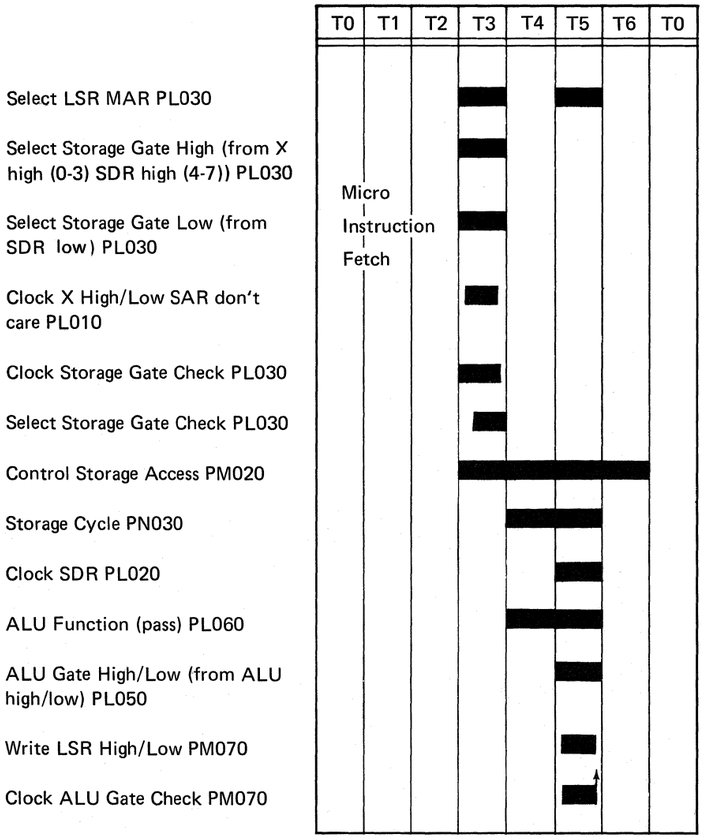
- A control storage address compare stop,
- Micro instruction step mode, or
- Processor check stop condition.

This stop condition can be caused by any of the following:

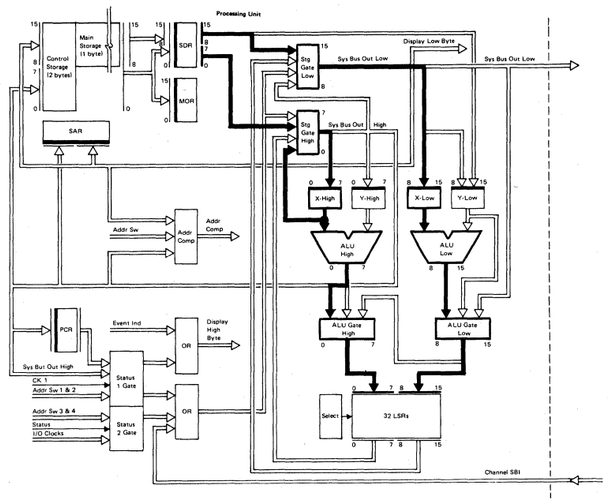
- Mode switch not in PROCESS mode,
- CS address compare, or
- Processor check.

With the use of INSN STEP position of mode selector switch, this condition permits single stepping through the branch instruction. An attempt to single step through a branch that is located in the last valid address of control storage will cause an invalid control address check.

Timing of CPU Functions for Branch Stop Condition

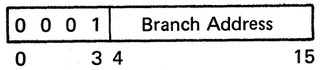


Specific CPU Data Path of Branch Stop Condition



Branch And Link

Mnemonic: BAL



This instruction is used for an unconditional branch and link operation. It allows branching to any one of the 4096 addresses in control storage.

Branch Address: 12-bit branch address that replaces the corresponding 12 bits in MAR.

When this instruction is executed, the address in MAR (of the next sequential instruction) is saved in the microprogram address backup register (MAB). The address in MAB is the link address. The 12-bit branch address in the branch and link instruction replaces the address in MAR. The address placed MAR is now the next sequential instruction. A return instruction (RETRN) is used to return to the next sequential instruction following the branch and link instruction. The return instruction causes the address saved in MAB to be placed into MAR. Hence, MAR is now pointing to the instruction following the branch and link instruction.

Condition Code

No change.

Timing of CPU Functions

Select Storage Gate High/Low (from LSR high/low) PL030

Select LSR (MAR) PL040

Clock X Low and X High (SAR don't care) PL010

Clock Storage Gate Check PL030

ALU High/Low Pass PL060

Select LSR (MAB) PL040

Select Storage Gate High (from X hi (0-3)/SDR (4-7)) PL030

Select Storage Gate Low (from SDR low) PL030

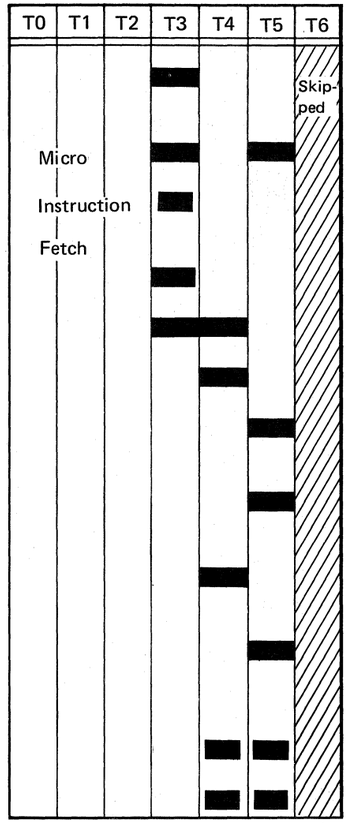
Select ALU Gate High/Low (from ALU high/low) PL060

Select ALU Gate High/Low (from storage gate high/low) PL050

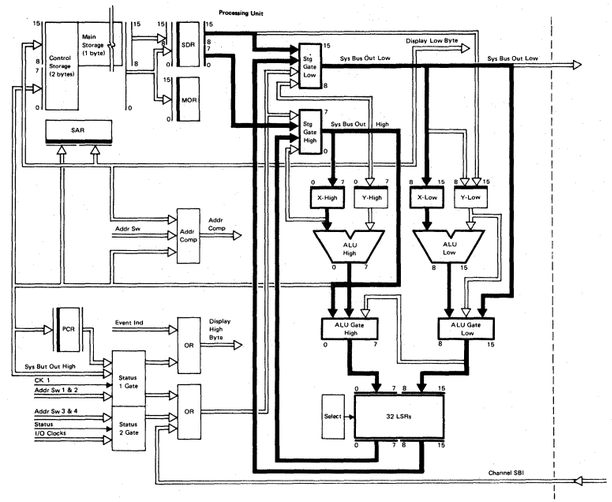
Write LSR High/Low PM070

Clock ALU Gate Check PM070

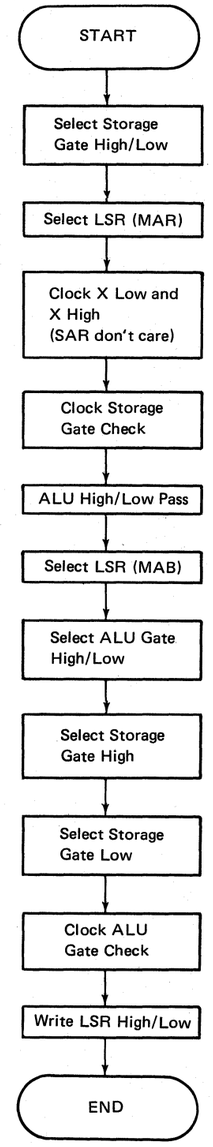
T-Times = 200 ns



Specific CPU Data Path of Branch and Link



Sequence of CPU Functions



Branch On Condition

Mnemonic: JC

0	0	1	0	Condition	Page Address
0			3	4 7	8 15

This instruction allows branching within 256 locations (defined by bits 8-15) if the conditon specified by bits 4-7 is met. If the condition is met, the 8-bit page address replaces the corresponding bits in MAR and SAR to form the address of the next sequential instruction.

During the first cycle, the page address is placed in X high. During the next cycle, T0 is skipped so no new LSR is selected and X low, X high, and SAR are not clocked again. ALU gate high/low is gated during T2 time of the next sequential instruction and the incremented data is written into LSR high and low.

Condition (Bits 4-7): These 4 bits indicate the function to be tested as follows:

Bits 4-7	Mnemonic	Test Condition
0000	JCY	Carry
0001	JH	High (condition code bit 5)
0010	JL	Low (condition code bit 6)
0011	JE	Equal (condition code bit 7)
0100	JP	Positive (condition code bit 1)
0100	JO	All ones (condition code bit 1)
0101	JN	Negative (condition code bit 2)
0101	JM	Mixed (condition code bit 2)
0110	JZ	Zero (condition code bit 3)
0111	JFLG	Flag
1000	JSR	Service request
1001	JNH	Not high
1010	JNL	Not low
1011	JNE	Not equal
1100	JNP	Not positive
1101	JNN	Not negative
1110	JNZ	Not zero
1111	RETRN	Return

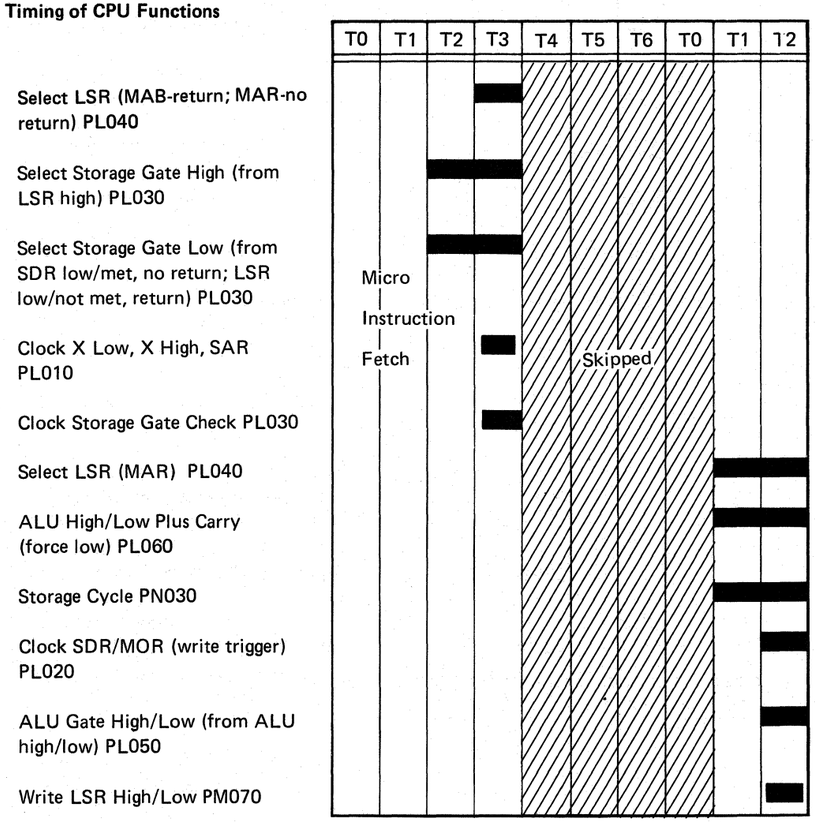
Page Address (Bits 8-15): 8-bit field to allow branching to one of 256 locations in control storage only. The 8-bit page address replaces the lower 8 bits in MAR when the tested condition is met.

Note: For the return condition (bits 4-7 equal 1011), the page address is not used. In this case, MAB is selected for the next sequential instruction.

Condition Code

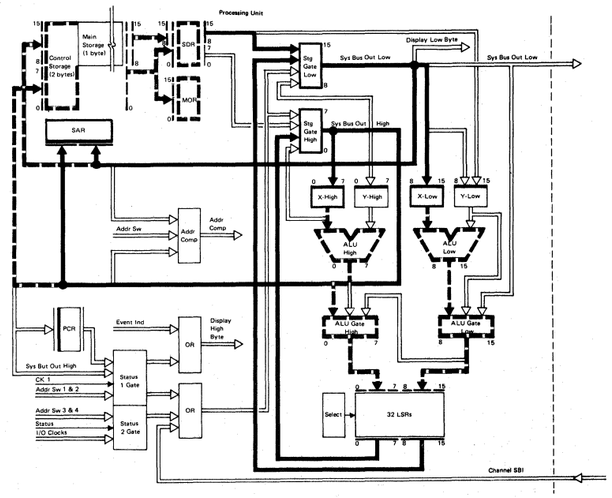
No Change.

Timing of CPU Functions



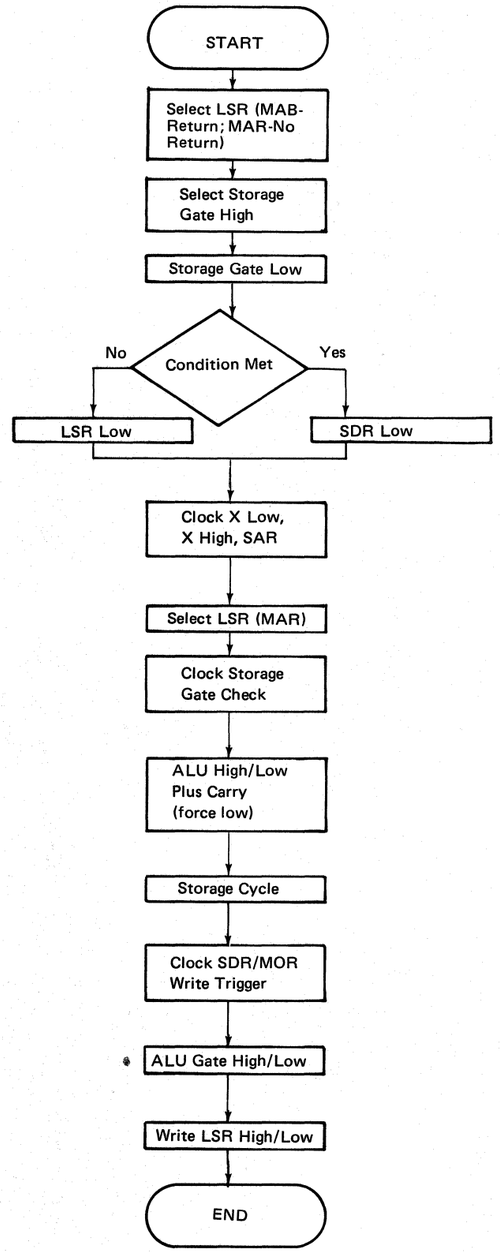
T-Times = 200 ns

Specific CPU Data Path



Cycle One ━━━━
Cycle Two ━ ━ ━ ━

Sequence of CPU Functions



Branch On Condition (Stop Condition)

Clocks T4, T5, and T6 can be taken if the processor is executing a branch on condition and the run latch is reset by:

- A control storage address compare stop,
- Micro instruction steps mode, or
- Processor check stop condition.

This can be caused by any of the following:

- Mode switch not turned to PROCESS mode,
- Control storage address compare, or
- Processor check.

With the use of INSN STEP position of mode selector switch, this condition permits single instruction stepping through the branch on condition instruction. An attempt to single step through a branch on condition which is located in the last valid address of control storage causes an invalid control address check.

Timing of CPU Functions

Select LSR (MAR: no return, MAB: return) PL040

Select Storage Gate High (from LSR high) PL030

Select Storage Gate Low (from LSR low: not met, SDR low: met) PL030

Clock X High/Low (SAR don't care) PL010

Clock Storage Gate Check PL030

Control Storage Access PN020

Storage Cycle PN030

Clock SDR PN010

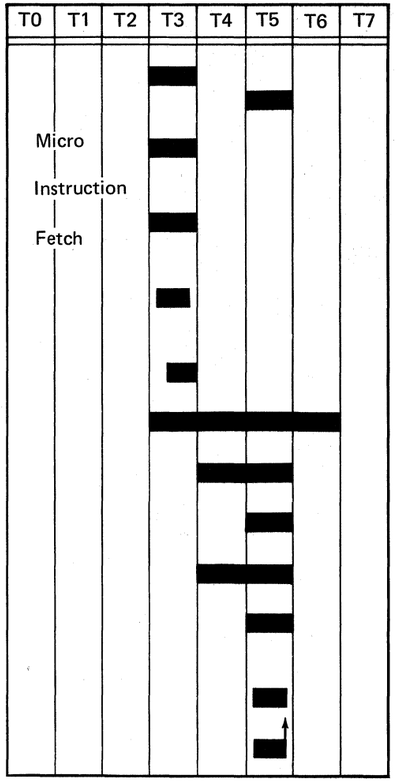
ALU Function (pass) PL060

ALU Gate High/Low (from ALU high/low) PL050

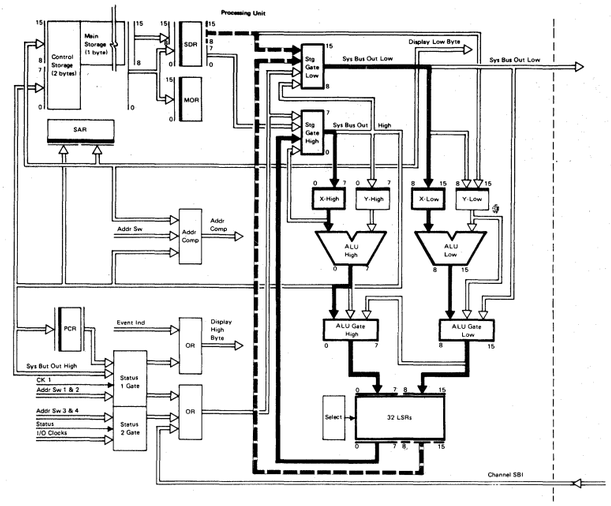
Write LSR High/Low PN070

Clock ALU Gate Check PM070

T-Times = 200 ns



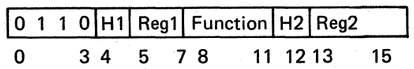
Specific CPU Data Path



▬ ▬ ▬ ▬ Depends on the condition being met.

Logical/Arithmetic 1

Mnemonic: LA1



This instruction allows arithmetic and logical type functions to be processed through the ALU. The logical/arithmetic 1 instruction is for 1-byte operations only.

H1 (Bit 4): Indicates which byte of the selected LSR (Reg1) is to be used in the current function.

- H1 = 0: Low byte of the register is to be used.
- H1 = 1: High byte of the register is to be used.

Reg1 (Bits 5-7): Selects one of eight registers in the LSR stack for the current operating level. The selected register is operand 1 of the function and is modified at the completion of the function.

Function (Bits 8-11): Determines the basic function to be performed. The logical/arithmetic functions that can be performed are shown in a table on the following page.

H2 (Bit 12): Indicates which byte of the selected LSR register (Reg2) is to be used in the current function.

- H2 = 0: Low byte of the register is to be used.
- H2 = 1: High byte of the register is to be used.

Reg2 (Bits 13-15): Selects one of the eight registers of the LSR stack appropriate for the current operating level. The selected register is operand 2 of the function. The selected register is not modified by the operation being performed.

Condition Code

Set as follows for *logical* operations:

On logical operations, two things are done:

1. The logical operation (OR, AND, EXCLUSIVE OR, etc) is performed.
2. R1 contents are ORed with the ones complement of R2 contents. This is expressed as (R1 or $\overline{R2}$).

The condition code is set to reflect the outcome of *both* operations except when the result of the logical operation is zeros (bit 3 of the PCR).

Positive (Bit 1 of PCR)—Set if the result of the logical operation was not equal to zero, *and* (R1 or $\overline{R2}$ equals all ones). Reset if the result of the logical operation equals all zeros, *or* (R1 or $\overline{R2}$ equals all ones).

Negative (Bit 2 of PCR)—Set if the result of the logical operation is not equal to all zeros, *and* (R1 or R2 not equal to all ones). Reset if the result of the logical operation equals all zeros, *or* (R1 or $\overline{R2}$ equals all ones).

Zero (Bit 3 of PCR)—Set if the result of the logical operation equals all zeros. Reset if the result of the logical operation is not equal to all zeros.

Set as follows for *arithmetic* operations:

Positive (Bit 1 of PCR)—Turns on if the result of the operation had a carry and was not equal to zero. Turns off if the result is zero or there was no carry.

Negative (Bit 2 of PCR)—Turns on if the result of the operation had no carry and was not equal to zero. Turns off if the result is zero or there is a carry.

Zero (Bit 3 of PCR)—Turns on if the result of the operation is zero. Turns off if the result does not equal zero.

Carry (Bit 4 of PCR)—Turns on if the arithmetic operation resulted in a carry. Turned off by the I/O immediate function reset carry—set equal, by system reset, or if the arithmetic operation resulted in no carry.

High (Bit 5 of PCR)—Same as positive (bit 1).

Low (Bit 6 of PCR)—Same as negative (bit 2).

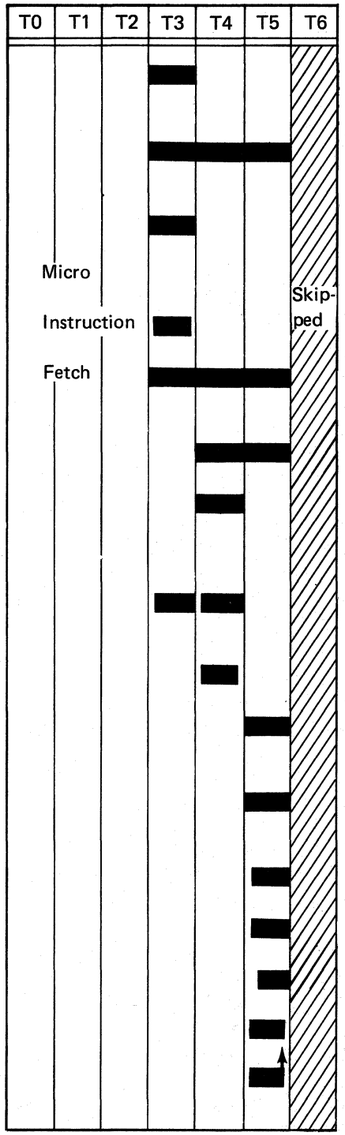
Equal (Bit 7 of PCR)—Turns off if the result of the operation does not equal zero. Turned on only by the I/O immediate function reset carry—set equal, or by system reset.

Logical/Arithmetic Functions

Bits 8 9 10 11	Mnemonic	Function	Description	Example
0 0 0 0		Not used		
0 0 0 1	XR	R1 (XOR) R2→R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU performs an exclusive OR function and the result is placed back in the register 1 location.	R1 10111100 R2 00110101 R1 10001001
0 0 1 0		Not used		
0 0 1 1	OR	R1 (OR) R2→R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU performs an OR function and the result is placed back in the register 1 location.	R1 10111100 R2 00110101 R1 10111101
0 1 0 0		Not used		
0 1 0 1	NCR	R1 (AND) $\overline{R2}$→R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU complements the Y register contents (R2), performs an AND function on the registers, and the result is placed back in the register 1 location.	R1 10111100 R2 00110101 $\overline{R2}$ 11001010 R1 10001000
0 1 1 0	NR	R1 (AND) R2→R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU performs an AND function and the result is placed back in the register 1 location.	R1 10111100 R2 00110101 R1 00110100
0 1 1 1	OCR	R1 (OR) $\overline{R2}$→R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU complements the Y register contents (R2), performs an OR function on the register contents, and the result is placed back in the register 1 location.	R1 10111100 R2 00110101 $\overline{R2}$ 11001010 R1 11111110
1 0 0 0	DEC	R1 - 1→R1	The contents of register 1 is placed in the X register. This data is gated into the ALU, and the ALU performs an X minus 1 function and the result is written back into the register 1 location.	R1 10111100 -1 00000001 R1 10111011
1 0 0 1	ACYR	R1 + R2 + C→R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The contents of the two registers are added together and added to the result of the carry trigger from a previous operation. The result is written back into the R1 location.	R1 10111100 R2 00110101 11110001 +C 00000001 R1 11110010
1 0 1 0		Not used		
1 0 1 1[1]	AR	R1 + R2→R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The contents of the two registers are added together in the ALU and the result is written back into the R1 location.	R1 10111100 R2 00110101 R1 11110001
1 1 0 0	SR	R1 - R2→R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The Y register contents is subtracted from the X register contents, the result is written back into the R1 location.	R1 10111100 R2 00110101 R1 10000111
1 1 0 1		Not used		
1 1 1 0	SCYR	R1 - R2 - C → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The Y register contents is subtracted from the X register contents; if the carry trigger was on from a previous operation, 1 is subtracted from the result. The final result is written back into the R1 location.	R1 10111100 R2 00110101 10000111 -C 00000001 R1 10000110
1 1 1 1	INC	R1 + 1→R1	The contents of register 1 is placed in the X register. The carry in line is activated by the instruction, and 1 is added to the contents of the X register by the ALU. The result is written back into the R1 location.	R1 10111100 +1 00000001 R1 10111101

[1] By adding a register to itself, (R1 + R1→R1) the function shift left logical can be executed. This function causes the 8 bits to be shifted one position to the left and the low order bit (bit 7) to be replaced with a zero. Mnemonic = SLL.

Timing of CPU Functions



Select LSR (bits 13, 14, 15) PL040

Select Storage Gate High (from LSR high) PL030

Select Storage Gate Low (from LSR low: 12=0; storage gate high: 12=1) PL040

Clock Y Reg PL010

Select ALU Function (bits 8, 9, 10, 11) PL060

Select LSR (bits 5, 6, 7) PL040

Select Storage Gate Low (from LSR low: 4=0; storage gate high: 4=1) PL030

Clock Storage Gate Check PL030

Clock X Reg PL010

Select ALU Gate Low (from ALU low) PL050

Select ALU Gate High (from ALU gate low) PL050

Clock ALU Gate Check PM070

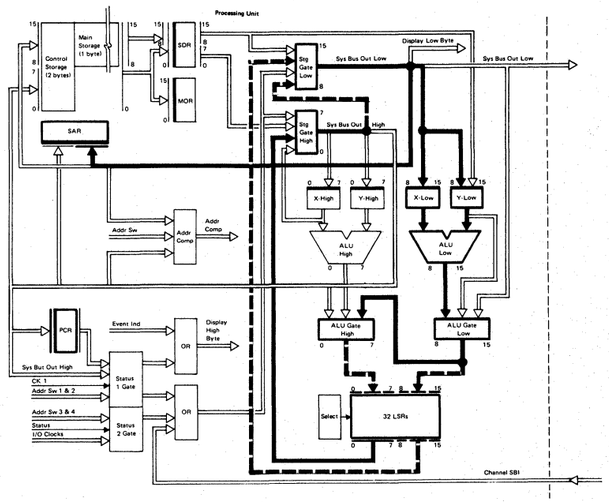
Write LSR High (bit 4=1) PM070

Write LSR Low (bit 4=0) PM070

Clock PCR (1, 2, 3) PK003

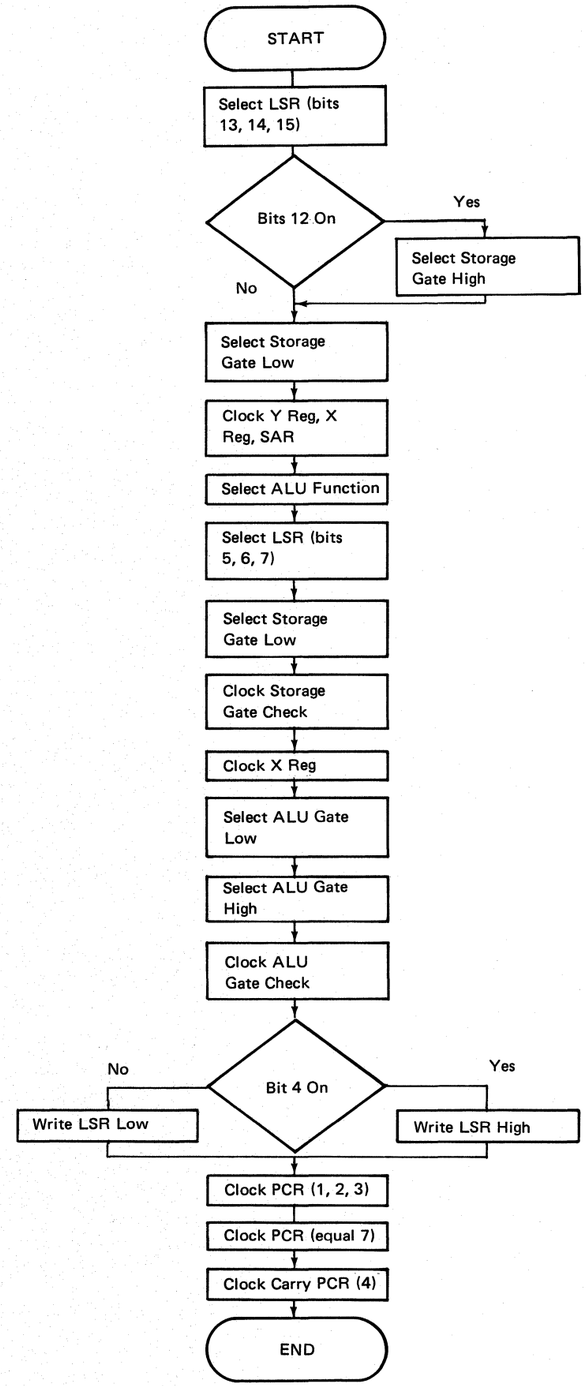
Clock PCR 4, 7 (arithmetic) 5, 6, (decode) PK003

Specific CPU Data Path



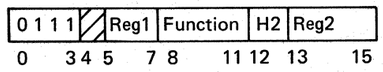
▬ ▬ ▬ Options depending upon the contents of bits 4 and 12.

Sequence of CPU Functions



Logical/Arithmetic 2

Mnemonic: LA2



This instruction allows arithmetic and logical type functions to be processed through the ALU. The logical/arithmetic 2 instruction always involves both bytes of Reg1 (operand 1) and one or both bytes of Reg2 (operand 2) depending on the function involved.

Reg1 (Bits 5-7): Selects one of the eight registers in the LSR stack. Both bytes of the selected register represent operand 1. The selected register is modified at the completion of the function being performed.

Function (Bits 8-11): Determines the basic logical or arithmetic function to be performed.

H2 (Bit 12): Indicates which byte of the selected LSR (Reg2) is to be used in the current function.

Reg2 (Bits 13-15): Selects one of the eight registers of the LSR stack appropriate for the current operating level. The selected register is operand 2 of the function. The selected register is not modified by the operation being performed.

Condition Code

Set as follows for *logical* operations:

On logical operations, two things are done:

1. The logical operation (OR, AND, EXCLUSIVE OR, etc) is performed.
2. R1 contents are ORed with the ones complement of R2 contents. This is expressed as (R1 or $\overline{R2}$).

The condition code is set to reflect the outcome of *both* operations except when the result of the logical operation is zeros (bit 3 of the PCR).

Positive (Bit 1 of PCR)—Set if the result of the logical operation was not equal to zero, *and* (R1 or $\overline{R2}$ equals all ones). Reset if the result of the logical operation equals all zeros, *or* (R1 or $\overline{R2}$ equals all ones).

Negative (Bit 2 of PCR)—Set if the result of the logical operation is not equal to all zeros, *and* (R1 or $\overline{R2}$ not equal to all ones). Reset if the result of the logical operation equals all zeros, *or* (R1 or $\overline{R2}$ equals all ones).

Zero (Bit 3 of PCR)—Set if the result of the logical operation equals all zeros. Reset if the result of the logical operation is not equal to all zeros.

Set as follows for *arithmetic* operations:

Positive (Bit 1 of PCR)—Turns on if the result of the operation has a carry and does not equal zero. Turns off if the result is zero or not carry.

Negative (Bit 2 of PCR)—Turns on if the result of the operation has no carry and does not equal zero. Turns off if the result is zero or has a carry.

Zero (Bit 3 of PCR)—Turns on if the arithmetic operation resulted in a carry. Turned off by the I/O immediate function reset carry—set equal, by system reset, or if the arithmetic operation resulted in no carry.

High (Bit 5 of PCR)—Same as positive (bit 1).

Low (Bit 6 of PCR)—Same as negative (bit 2).

Equal (Bit 7 of PCR)—Turns off if the result of the operation does not equal zero. Turned on only by I/O immediate function reset carry—set equal, or by system reset.

Logical/Arithmetic Functions

Bits 8 9 10 11	Mnemonic	Function	Description	Example
0 0 0 0		Not used		
0 0 0 1	XR	R1 (XR) R2 → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU performs an exclusive OR function and the result is placed in the register 1 location.	R1 1011110011001101 R2 0011010110101001 R1 1000100101100100
0 0 1 0		Not used		
0 0 1 1	OR	R1 (OR) R2 → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU performs an OR function and the result is placed in the register 1 location.	R1 1011110011001101 R2 0011010110101001 R1 1011110111101101
0 1 0 0		Not used		
0 1 0 1	NCR	R1 (AND) $\overline{R2}$ → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU complements the Y register contents, performs an AND function on the register contents, and writes the results in the register 1 location.	R1 1011110011001101 R2 0011010110101001 $\overline{R2}$ 1100101001010110 R1 1000100001000100
0 1 1 0	NR	R1 (AND) R2 → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU performs an AND function and the result is written in the register 1 location.	R1 1011110011001101 R2 0011010110101001 R1 0011010010001001
0 1 1 1	OCR	R1 (OR) $\overline{R2}$ → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The ALU complements the Y register contents (R2), performs an OR function on the register contents, and the result is written in the register 1 location.	R1 1011110011001101 $\overline{R2}$ 0011010110101001 $\overline{R2}$ 1100101001010110 R1 1111111101101111
1 0 0 0	DEC	R1 - 1→R1	The contents of register 1 is placed in the X register. This data is gated into the ALU, and the ALU performs an X minus 1 function, and the result is written into the register 1 location.	R1 1011110011001101 -1 0000000000000001 R1 1011110011001100

Bits 8 9 10 11	Mnemonic	Function	Description	Example
1 0 0 1	ACYR	R1 + R2 + C → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The contents of the two registers are added together and added to the result of the carry trigger from a previous operation. The result is written into the register 1 location.	R1 1011110011001101 R2 0011010110101001 1111001001110110 +C 0000000000000001 R1 1111001001110111
1 0 1 0	SR	R1 - R2 + 1 → R1 (1 byte)	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The Y register contents is subtracted from the X register contents. The result is written into the R1 location.	R1 1011110011001101 R2 10101001 R1 1011110000100100 +1 0000000000000001 R1 1011110000100101
1 0 1 1[1]	AR	R1 + R2 → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The contents of the two registers are added together in the ALU and the result is written into the register 1 position.	R1 1011110011001101 R2 0011010110101001 R1 1111001001110110
1 1 0 0	SR	R1 - R2 → R1	Same as (1010) SR.	R1 1011110011001101 R2 0011010110101001 R1 1000011100101100
1 1 0 1	AR	R1 + R2 → R1 (1 byte)	Same as (1011) AR.	R1 1011110011001101 R2 10101001 R1 1011110101110110
1 1 1 0	SCYR	R1 - R2 - 1 - C → R1	The contents of register 1 is placed in the X register; the contents of register 2 is placed in the Y register. The Y register contents is subtracted from the X register contents; the carry trigger from a previous operation is subtracted from the result. The final result is written back into the R1 location.	R1 1011110011001101 R2 0011010110101001 1000011100100100 -C 0000000000000001 R1 1000011100100011
1 1 1 1	INC	R1 + 1→R1	The contents of register 1 is placed in the X register. The carry in line is activated by the instruction, and this is added to the contents of the X register by the ALU. The result is written into the register 1 location.	R1 1011110011001101 +1 0000000000000001 R1 1011110011001110

[1] By adding a register to itself (R1 + R1→R1), the function shift left double can be executed. This function causes the 16 bits to be shifted one position to the left and the low order bit (15) to be replaced with a zero. Mnemonic = SLLD.

Timing of CPU Functions

Select LSR (13, 14, 15) PL040

Select Storage Gate Low (from LSR low: 12=0; storage gate high: 12=1) PL030

Select Storage Gate High (from LSR high) PL030

Clock Y Reg (high/low) (X low, X high, and SAR don't care) PL010

Reset Y High (16/8 arithmetic) PL010

Select ALU Function (8, 9, 10, 11) PL060

Clock Storage Gate Check PL030

Select LSR (5, 6, 7) PL040

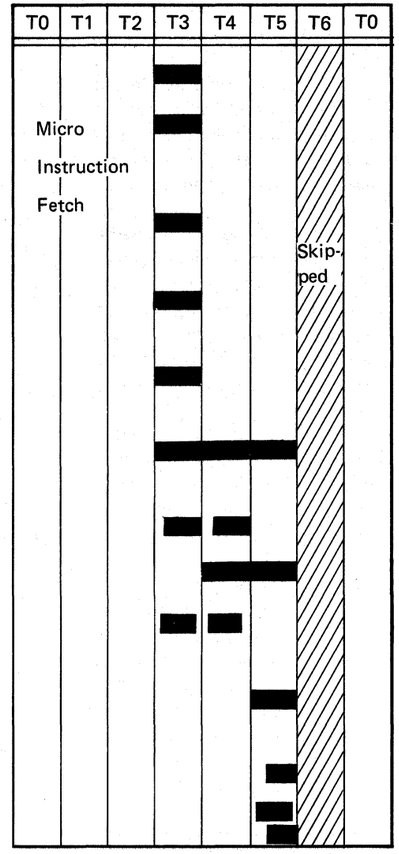
Clock X Low, and X High (SAR don't care) PL010

Select ALU Gate High/Low (from ALU high/low) PL050

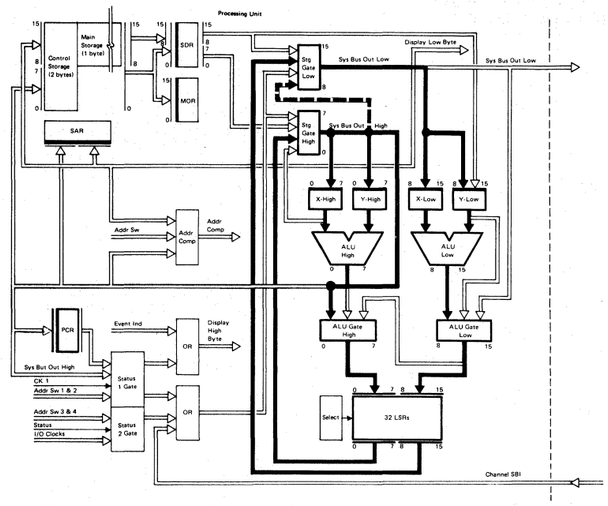
Write LSR High/Low PM070

Clock PCR PK003

T-Times = 200 ns

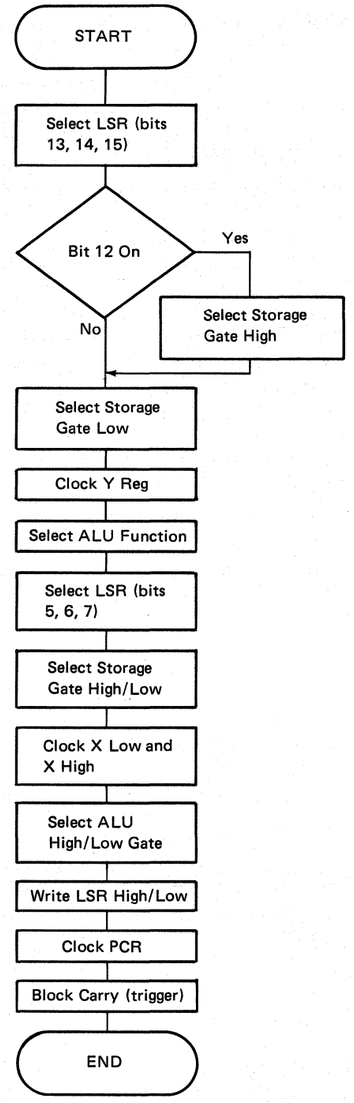


Specific CPU Data Path



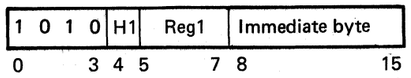
▬ ▬ ▬ Options depending on the contents of bit 12.

Sequence of CPU Functions



Immediate

Mnemonic: LI



This instruction takes the data in the immediate byte and loads it directly into a selected register of the appropriate LSR stack. Data can be placed into the high or low byte of the selected register.

H1 (Bit 4): Indicates which byte of the selected register in the LSR stack is to be used:

- H1 = 0: Low byte of the register is to be used.
- H1 = 1: High byte of the register is to be used.

Reg1 (Bits 5-7): Selects one of the eight registers in the appropriate LSR stack. The immediate byte in the instruction replaces the byte in the selected LSR.

Immediate byte (Bits 8-15): The 1 byte data field is loaded into the selected LSR.

Condition Code

No change.

Timing of CPU Functions

Select LSR (5, 6, 7) PL040

Select Storage Gate Low (from SDR low) PL030

Reset Y Reg Low PL010

Clock X Low, Y Low, (X high, Y high, SAR don't care) PL010

Clock Storage Gate Check PL030

ALU Function (pass) PL060

Select ALU Gate Low (from ALU low) PL050

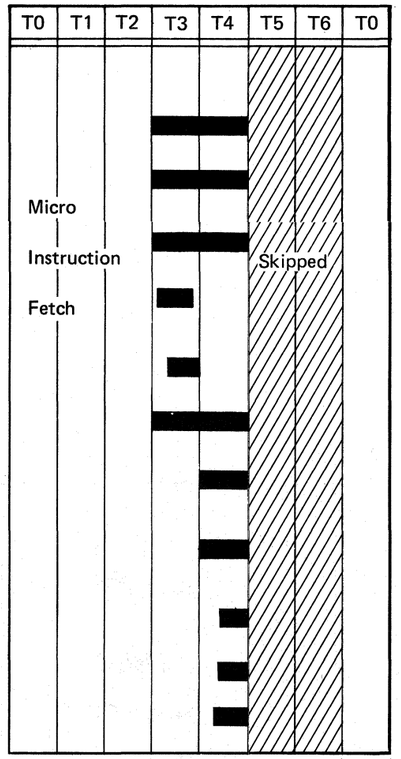
Select ALU Gate High (from ALU gate low) PL050

Write LSR High (4=1) PM070

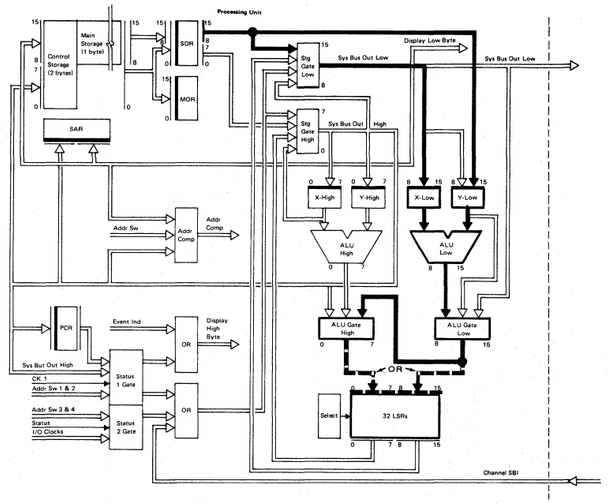
Write LSR Low (4=0) PM070

Clock ALU Gate Check PM070

T-Times = 200 ns

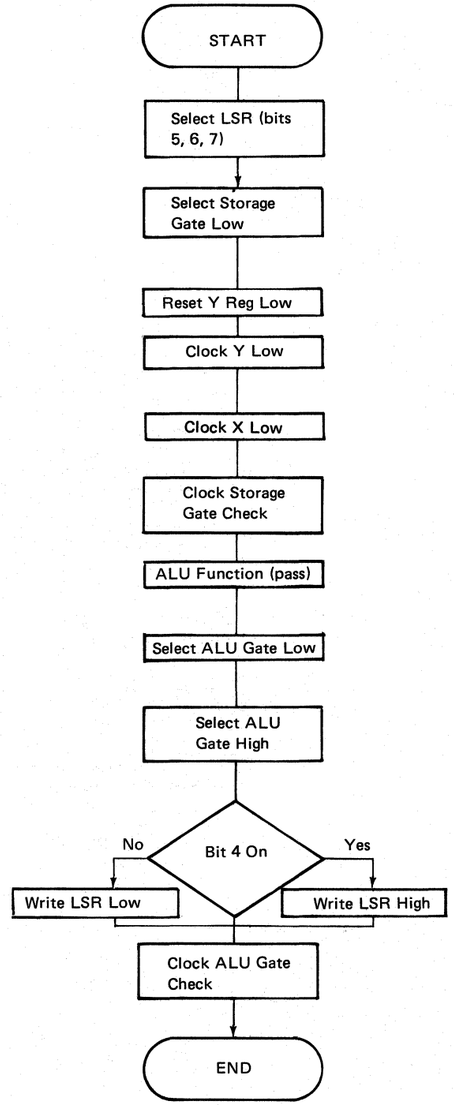


Specific CPU Data Path



▬ ▬ ▬ Options depending on the contents of bit 4.

Sequence of CPU Functions



Compare Immediate

Mnemonic: CI

1 1 0 0	H1	Reg1	Immediate byte
0 3	4	5 7	8 15

This instruction is used to compare the 8 bits of data in the selected LSR with the corresponding 8 bits of data in the immediate field. The results of the compare are reflected in the condition code setting. The selected LSR is not altered by the compare immediate instruction.

H1 (Bit 4): Indicates which byte of the selected register in the LSR stack is to be used in the compare:

- H1 = 0: Low byte of the register is to be used.
- H1 = 1: High byte of the register is to be used.

Reg1 (Bits 5-7): Selects one of the eight registers in the appropriate LSR stack. The byte in the immediate field is compared to the data in the selected LSR.

Immediate byte (Bits 8-15): Contains the data to be compared to the data in the selected LSR.

Condition Code

Set as follows:

Positive (bit 1 of PCR)—Register data greater than data field.

Negative (bit 2 of PCR)—Register data less than the data field.

Zero (bit 3 of PCR)—Register data equals data field.

Timing of CPU Functions

Select LSR (5, 6, 7) PL040

Select Storage Gate Low (from LSR low: 4=0; storage gate high: 4=1) PL030

Select Storage Gate High (from LSR high) PL030

Select Y Data PL010

Clock Y Low, High PL010

Clock X Low, High and SAR (don't care) PL010

Clock Storage Gate P Check PL030

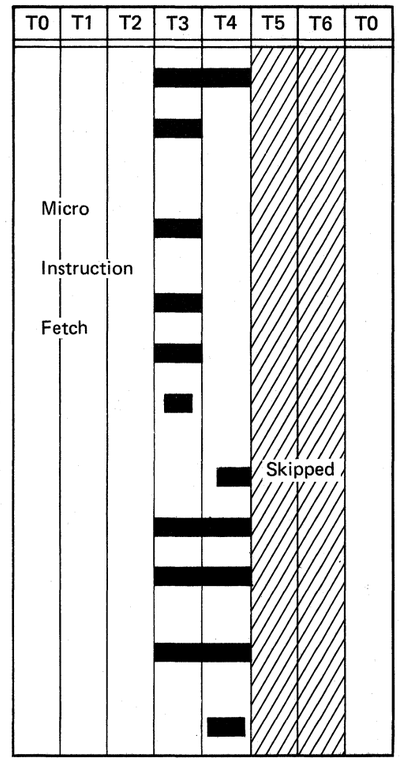
ALU Function (X plus $\overline{Y}$) PL060

Select ALU Gate Low (from ALU low) PL050

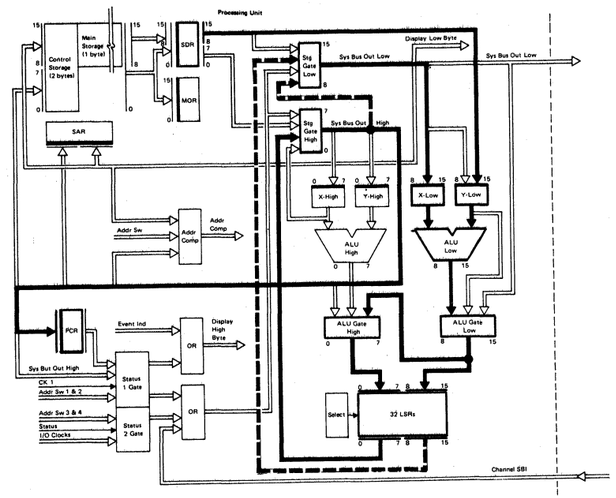
Select ALU Gate High (from ALU gate low) PL050

Clock PCR (1, 2, 3) PK003

T-Times = 200 ns

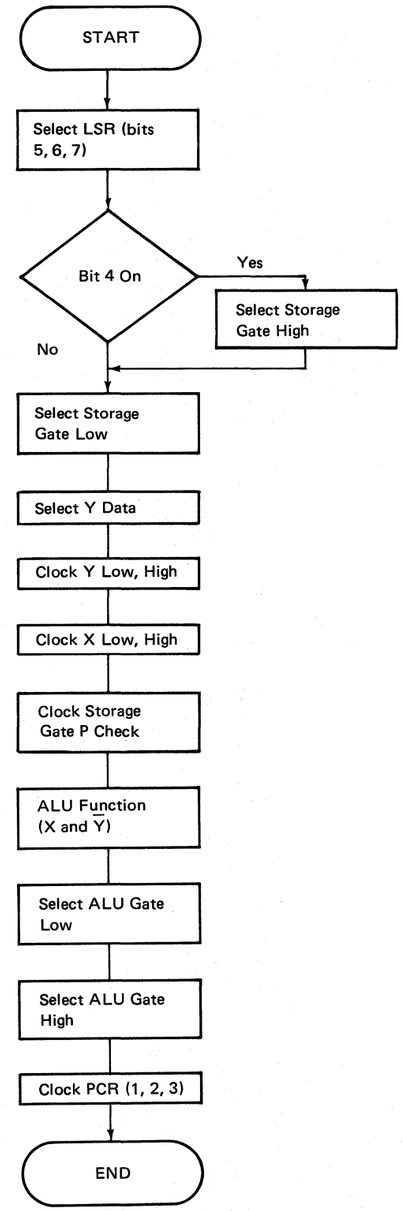


Specific CPU Data Path



▬▬ Options depending on the contents of bit 4.

Sequence of CPU Functions



Subtract Immediate

Mnemonic: SI (subtract immediate)
AI (add immediate)

1 1 0 1	H1	Reg1	Immediate byte
0 3	4	5 7	8 15

The data in the immediate byte of this instruction is subtracted from the data in the specified LSR (Reg 1).

To add immediate, the immediate data is complemented before insertion in the immediate field of the instruction (complement subtraction = addition).

When the contents of Reg 1 don't matter after execution, this instruction can be used to perform a compare function by testing the condition code after execution.

H1 (Bit 4): Indicates which byte of the selected register in the LSR stack is to be used in the subtraction:

H1 = 0: Low byte of the register is to be used.
H1 = 1: High byte of the register is to be used.

Reg1 (Bits 5-7): Selects one of eight registers in an LSR stack. The data field is subtracted from the data in the selected LSR.

Immediate byte (Bits 8-15): Contains the data to be subtracted from the data in the selected register.

Condition Code

Set as follows:

Positive (bit 1 of PCR)—Register data is greater than data field.

Negative (bit 2 of PCR)—Register data is less than data field.

Zero (bit 3 of PCR)—Register data and data field are equal.

Timing of CPU Functions

Select LSR (5, 6, 7) PL040

Select Storage Gate Low (from LSR low: 4=0; storage gate high: 4=1) PL030

Select Storage Gate High (from LSR high) PL030

Select Y Data (from SDR) PL010

Clock Y Reg PL010

Clock X Low (X high and SAR don't care) PL010

Clock Storage Gate P Check PL030

ALU Function (X plus $\overline{Y}$) PL060

Select ALU Gate Low (from ALU low) PL050

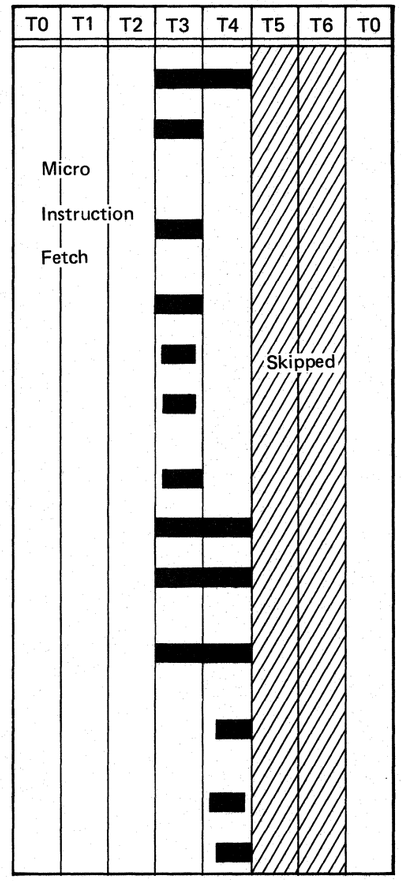
Select ALU Gate High (from ALU low) PL050

Write LSR: Low 4=0, High 4=1 PM070

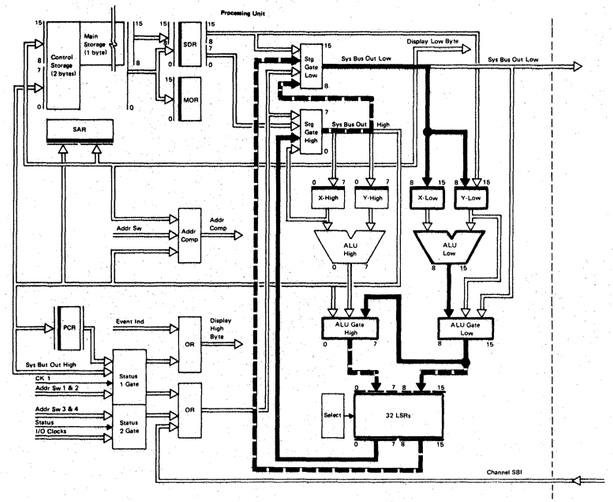
Clock PCR (1, 2, 3) PK003

Clock ALU Gate P Check PM070

T-Times = 200 ns

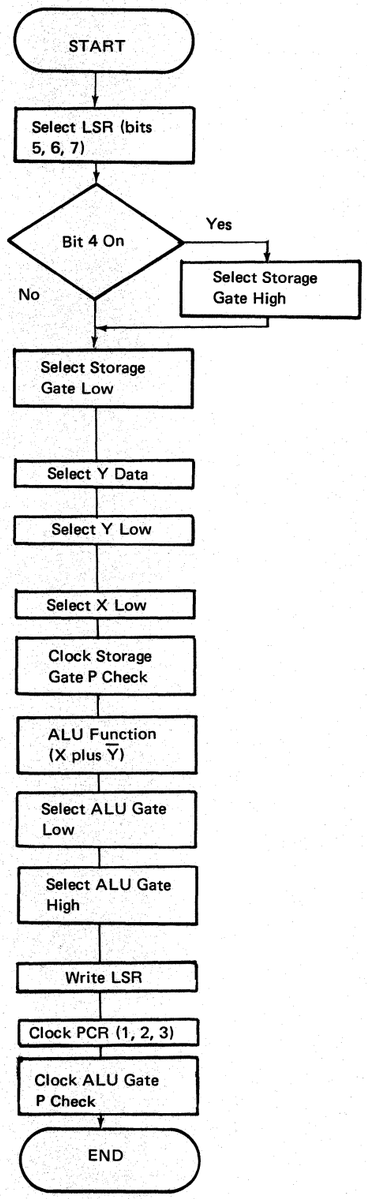


Specific CPU Data Path



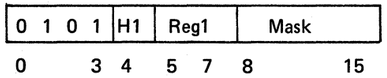
▬ ▬ ▬ Options depending on the contents of bit 4.

Sequence of CPU Functions



Test Mask

Mnemonic: TM



The bits in 1 byte of a working register may be tested by this micro instruction. A mask in the immediate data field of the micro instruction identifies the bits to be tested. As a result of this test, one of three conditions will be set in the PCR:

1. The tested bits are all equal to 1 (PCR 1 bit set on).
2. The tested bits are a mixture of ones and zeros (PCR 2 bit set on).
3. The tested bits are equal to zero (PCR 3 bit set on).

H1 (Bit 4): Selects low or high byte of register:

H1 = 0: Low byte of register used.

H1 = 1: High byte of register used.

Reg1 (Bit 5-7): Selects one of the working registers in the specified interrupt level.

Mask (Bits 8-15): Any bit set to 1 indicates the corresponding bit in the selected byte is to be tested.

Any bit set to 0 indicates the corresponding bit is to be ignored.

Condition Code

Result of Test	Condition Code
Tested bits all = 1	Positive
Tested bits are mixed	Negative
Tested bits all = 0	Zero

Example:

H1 = 0

Reg1 = 011

Interrupt level = 0

Mask = 0 0 1 0 1 0 0 1

LSR3 = 0 1 1 0 1 1 0 1

Bits 2, 4, and 7 in LSR 3 are to be tested.

Condition Code Set: Positive

PCR = 01000000

Bits tested all equal 1.

Bits 5 6 7	Selected LSR Interrupt Level 0	1	2
0 0 0	0	16	24
0 0 1	1	17	25
0 1 0	2	18	26
0 1 1	3	19	27
1 0 0	4	20	28
1 0 1	5	21	29
1 1 0	6	22	30
1 1 1	7	23	31

Timing of CPU Functions

Select LSR (5, 6, 7) PL040

Select Storage Gate High (from LSR high) PL030

Select Storage Gate Low (LSR low if 4=0, storage gate high if 4=1) PL030

Clock X Reg and SAR PL010

Select Y Reg (from SDR) PL010

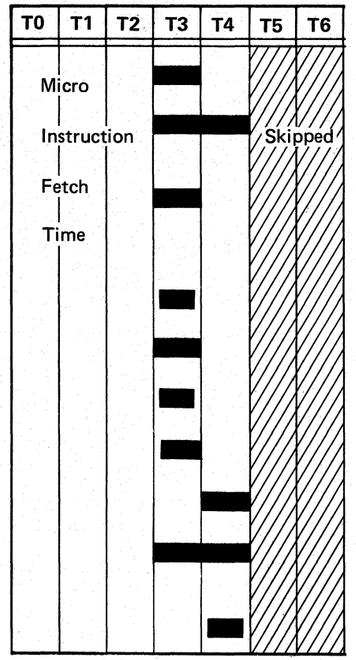
Clock Y Reg PL010

Clock Storage Gate Check PL030

ALU Gate High/Low PL050

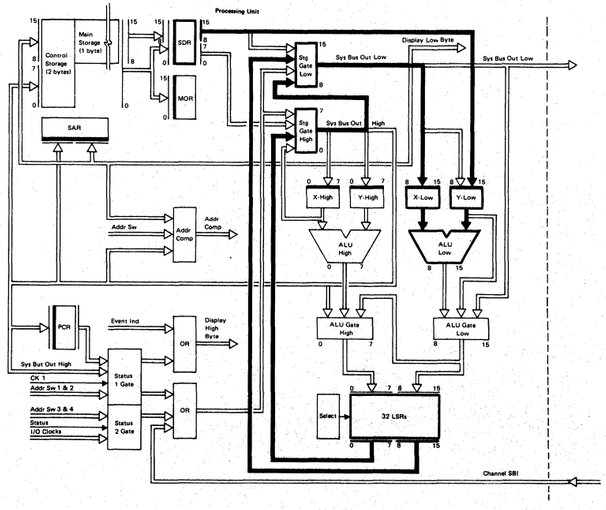
ALU Function (X and Y) OR Logic (X OR $\overline{Y}$) PL060

Clock PCR (1, 2, 3) PK000

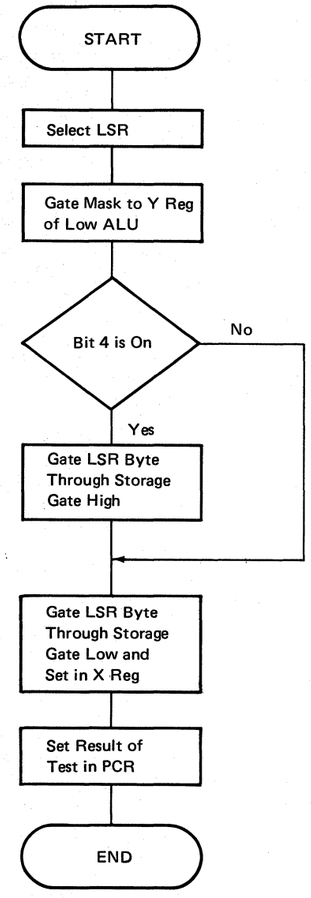


T-Times = 200 ns

Specific CPU Data Path

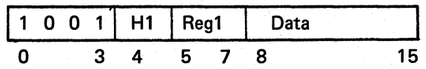


Sequence of CPU Functions



Set Bits On

Mnemonic: SBN



This instruction is used to set bits on in the specified byte of the selected register in the LSR stack.

H1 (Bit 4): Indicates which byte of the selected register in the LSR stack is to be used:

- H1 = 0: Low byte of the register is to be used.
- H1 = 1: High byte of the register is to be used.

Reg1 (Bits 5-7): Selects one of eight registers in the appropriate LSR stack. The byte of the register is ORed with the data in the data field.

Data (Bits 8-15): The 8 bits of this field correspond to the eight bits in the selected register. Any bit in the data field that is set to one causes its corresponding bit in the register to be set to one. Any bits in the data field that are set to zero do not affect their corresponding bits in the selected register.

Condition Code

No change.

Timing of CPU Functions

Select LSR 5, 6, 7 PL040

Select Storage Gate Low (from LSR low: 4=0, storage gate high: 4=1) PL030

Select Storage Gate High (from LSR high) PL030

Select Y Data (from SDR low) PL010

Clock Y High/Low PL010

Clock X High/Low (SAR don't care) PL010

Clock Storage Gate Check PL030

ALU Function (X OR Y) PL060

Select ALU Gate Low (from ALU low) PL050

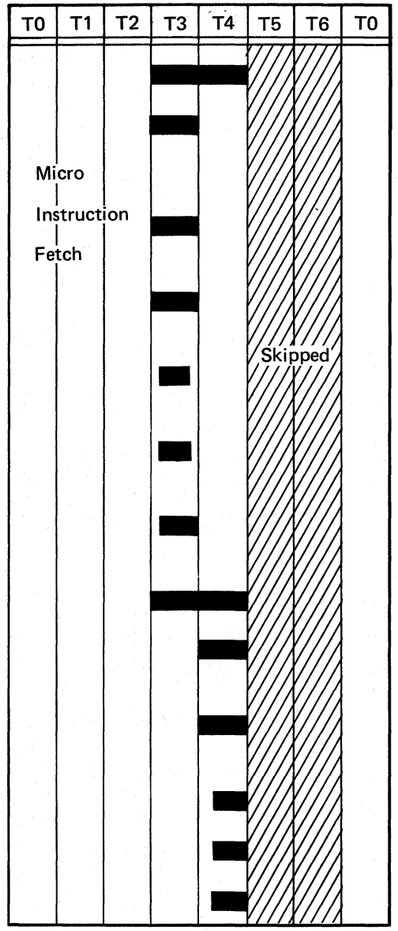
Select ALU Gate High (from ALU gate low) PL050

Write LSR High (4=1) PM070

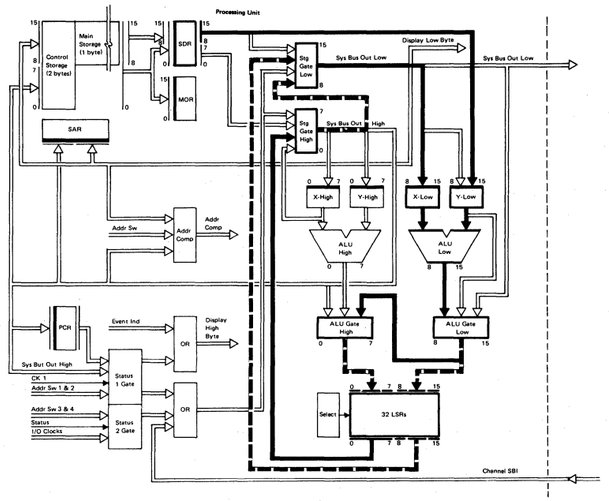
Write LSR Low (4=0) PM070

Clock ALU Gate Check PM070

T-Times = 200 ns

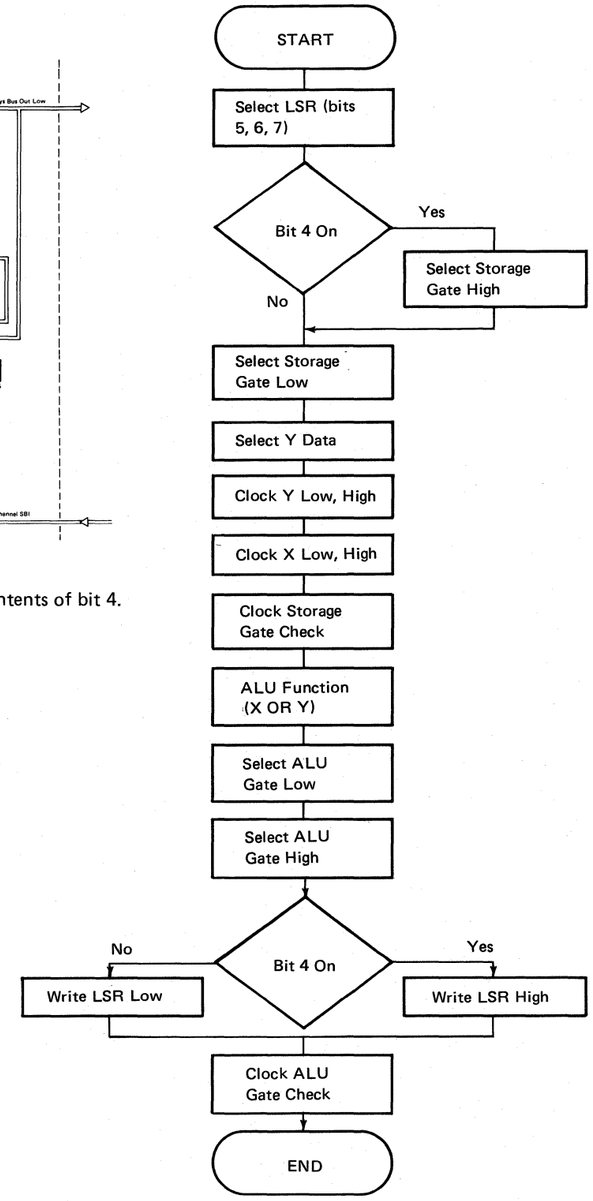


Specific CPU Data Path



▬ ▬ ▬ Options depending on the contents of bit 4.

Sequence of CPU Functions



Set Bits Off

Mnemonic: SBF

1 0 0 0	H1	Reg1	Data
0 3	4	5 7	8 15

Set off is used to set bits off in the specified byte of the selected register in the LSR stack.

H1 (Bit 4): Indicates which byte of the selected register in the LSR stack is to be used:

- H1 = 0 Low byte of the register is to be used.
- H1 = 1: High byte of the register is to be used.

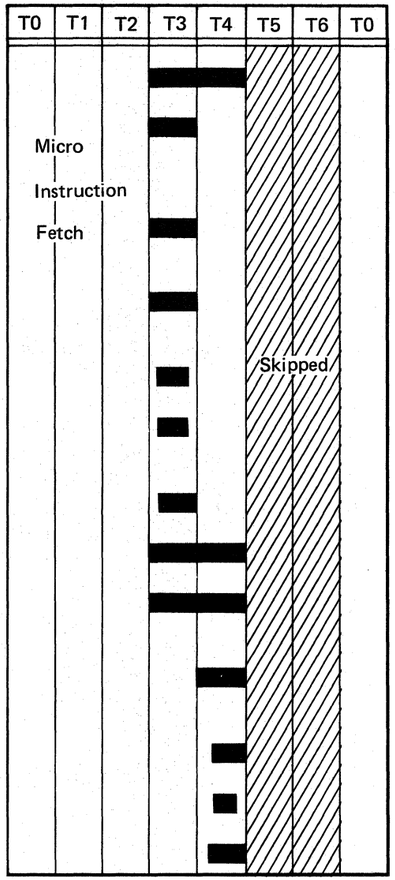
Reg1 (Bits 5-7): Selects one of the eight registers in the appropriate LSR stack. The byte of the register is ANDed with the complement of the data in the data field.

Data (Bits 8-15): The 8 bits in this field correspond to the eight bits of the selected register. Any bit in the data field that is set on (equal to one) causes its corresponding bit in the register to be set to zero. Any bits in the data field that are off (equal to zero) do not affect any bits in the register.

Condition Code

No change.

Timing of CPU Functions



Select LSR (5, 6, 7) PL040

Select Storage Gate Low (from LSR low: 4=0, storage gate high: 4=1) PL030

Select Storage Gate High (from LSR high) PL030

Select Y Data (from SDR low) PL010

Clock Y High/Low PL010

Clock X High/Low (SAR don't care) PL010

Clock Storage Gate Check PL030

ALU Function (X AND $\overline{Y}$) PL060

Select ALU Gate Low (from ALU low) PL050

Select ALU Gate High (from ALU gate low) PL050

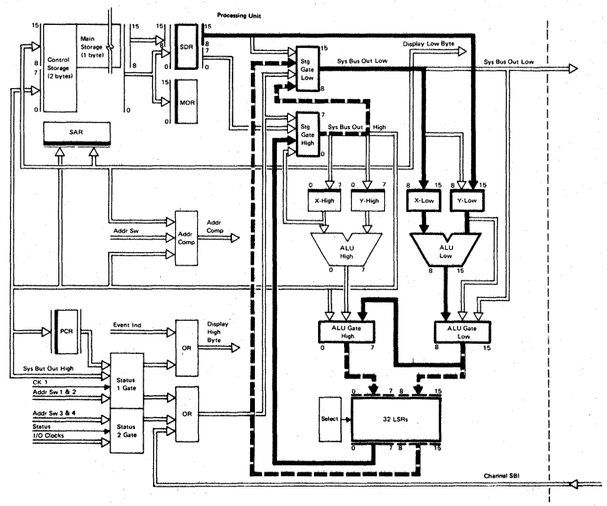
Write LSR High (4=1) PM070

Write LSR Low (4=0) PM070

Clock ALU Gate Check PM070

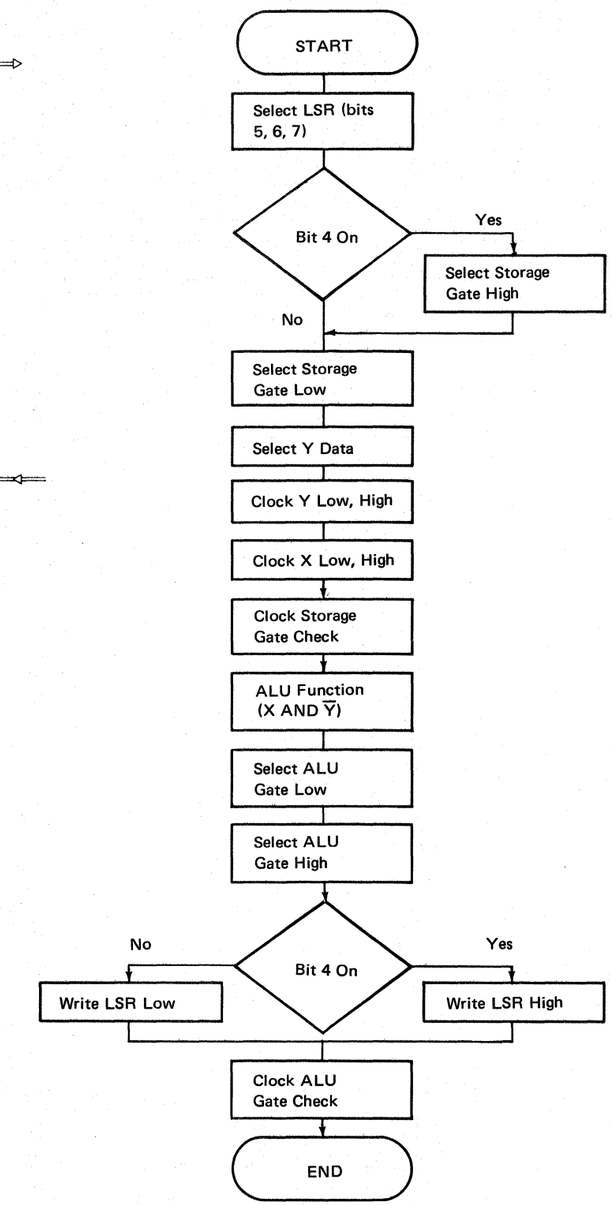
T-Times = 200 ns

Specific CPU Data Path

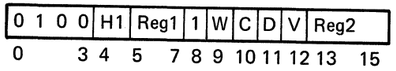


▬ ▬ ▬ Options depending on the contents of bit 4.

Sequence of CPU Functions



Storage



The storage instruction is used for accessing either control storage or main storage. Data can be transferred to or from the LSRs.

H1 (Bit 4):

H1 = 0: Select low byte of LSR stack specified by bits 5-7 (Reg1).
H1 = 1: Select high byte of LSR stack specified by bits 5-7 (Reg1).
Not used when bit 10 is on.

Reg1 (Bits 5-7): Selects one of the eight registers of the appropriate LSR stack. Data is transferred to or from this register.

Bit 8: Modifier to the op code (bits 0-3). If bits 8=0, the instruction is I/O storage; if bit 8=1, the instruction is storage.

W (Bit 9): Identifies the direction of transfer:

W = 0: Read from storage and transfer to the LSR stack.
W = 1: Transfer from the LSR stack and write to storage.

C (Bit 10): Selects main or control storage:

C = 0: Selects main storage.
C = 1: Selects control storage.

D (Bit 11): Indicates whether the address in the LSR (specified by bits 13-15) should be incremented (D = 0) or decremented (D = 1).

V (Bit 12): Indicates the amount the address in the LSR (specified by bits 13-15) should be incremented or decremented. If V = 0, the address in the selected LSR is not changed; if V = 1, the address in the selected LSR is incremented or decremented by one depending on the bit setting of the D field.

Reg2 (Bits 13-15): Selects one of the eight LSRs dedicated to the present operating level that contains the storage address needed for the data transfer. The address in the specified LSR may be updated depending on bits 11 (D field) and 12 (V field).

Storage Instruction List

4	8	9	10	11	12	Mnemonic	Description
X	1	0	1	0	1	LC	Load from ctrl str, increase R2 by 1.
X	1	0	1	1	1	LC	Load from ctrl str, decrease R2 by 1.
X	1	0	1	0	0	LC	Load from ctrl str, R2 (no change).
X	1	1	1	0	1	STC	Store to ctrl str, increase R2 by 1.
X	1	1	1	1	1	STC	Store to ctrl str, decrease R2 by 1.
X	1	1	1	0	0	STC	Store to ctrl str, R2 (no change).
H	1	0	0	0	1	LM	Load from main str, increase R2 by 1.
H	1	0	0	1	1	LM	Load from main str, decrease R2 by 1.
H	1	0	0	0	0	LM	Load from main str, R2 (no change).
H	1	1	0	0	1	STM	Store to main str, increase R2 by 1.
H	1	1	0	1	1	STM	Store to main str, decrease R2 by 1.
H	1	1	0	0	0	STM	Store to main str, R2 (no change).

Bit 4:

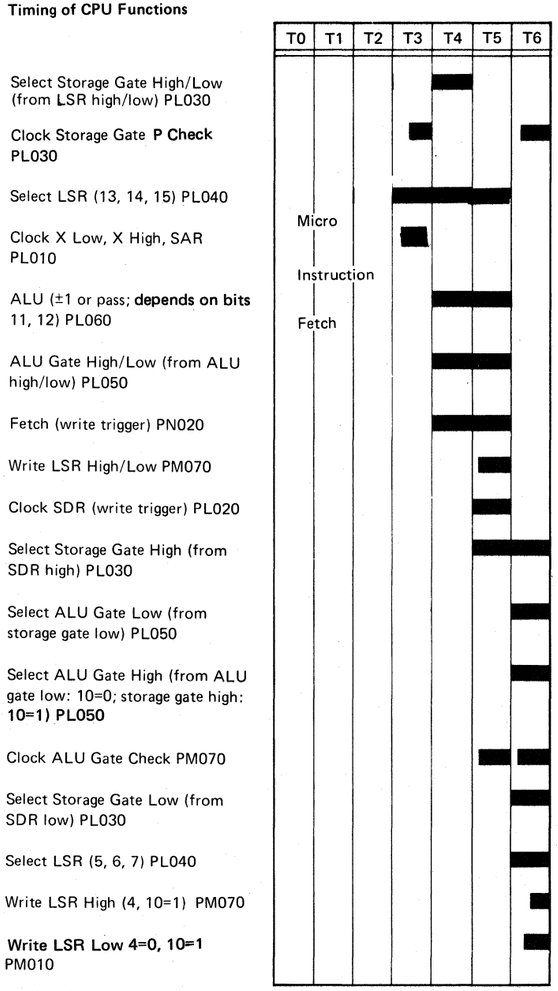
X: Not used
H = 1: High byte
H = 0: Low byte

Condition Code

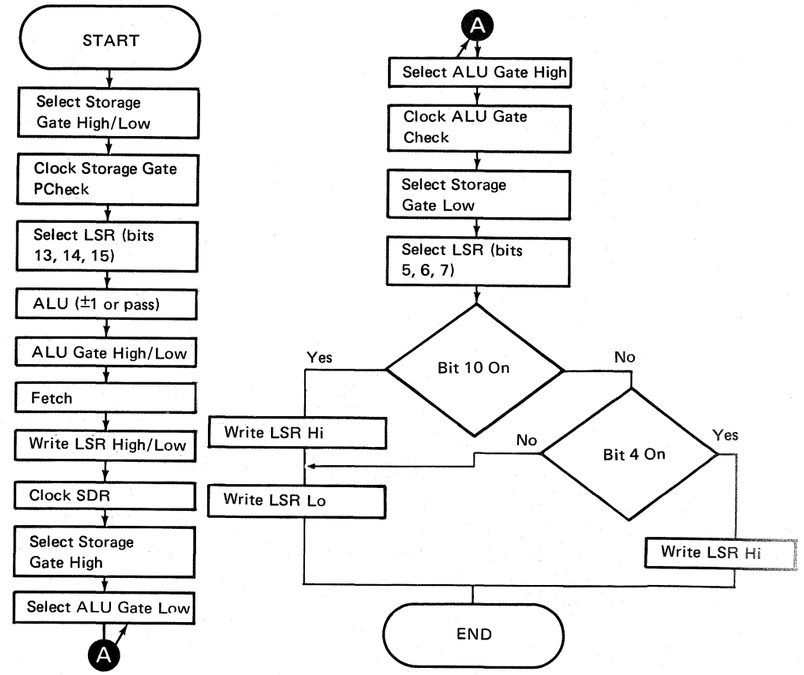
No change.

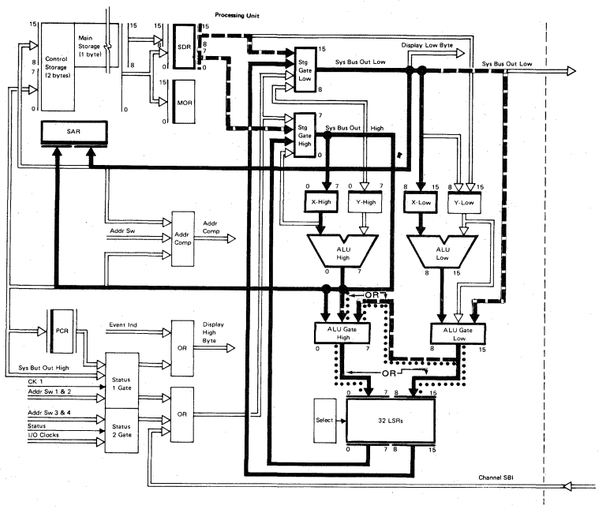
Storage (Read)

Timing of CPU Functions



Sequence of CPU Functions

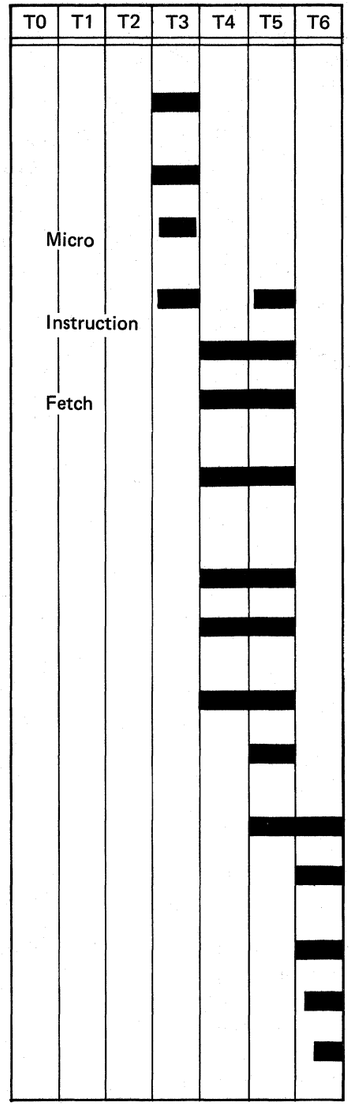




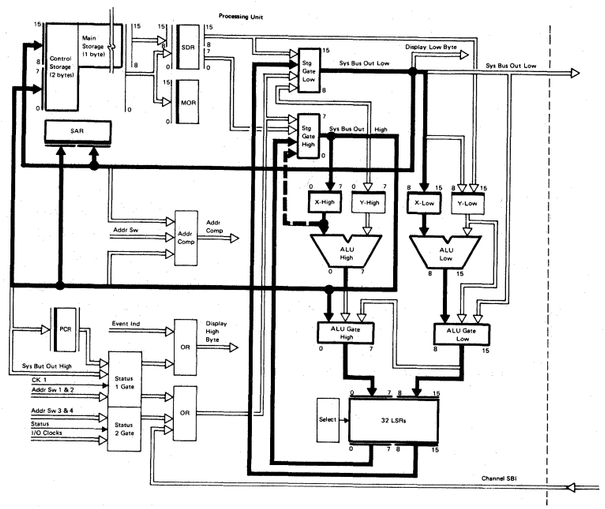
First time activated.
Second time activated.
Options depending on contents of bits 4 and 10.

Storage (Write)

Timing of CPU Functions

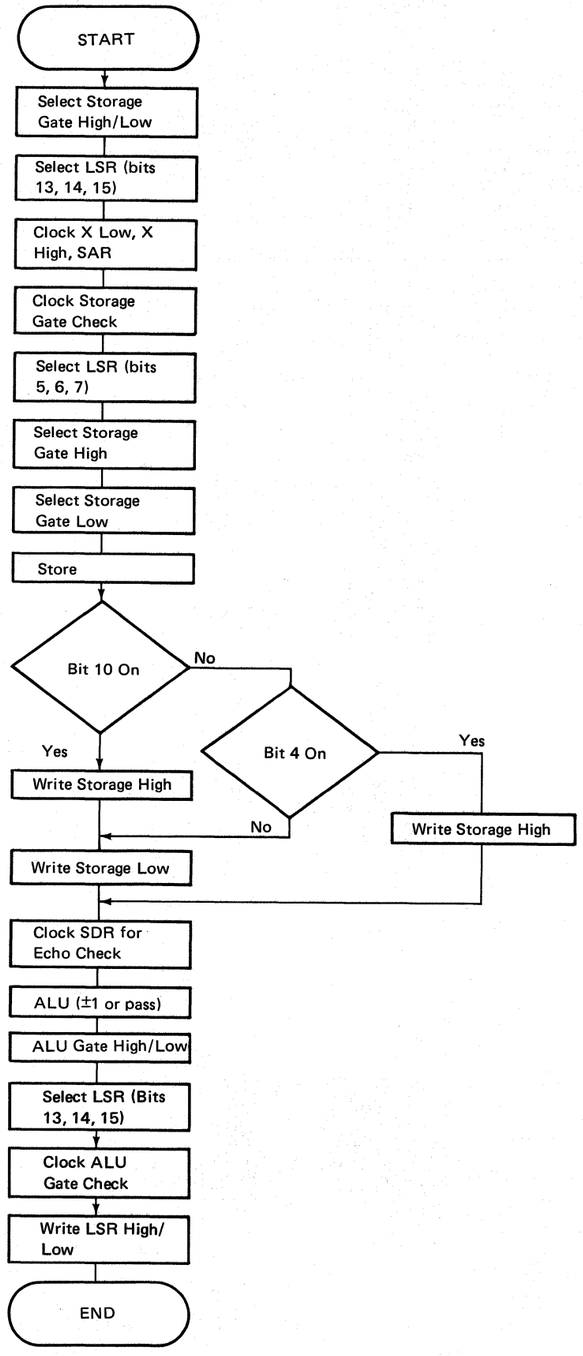


Specific CPU Data Path



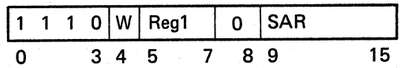
▬ ▬ ▬ Options depending on contents of bits 4 and 10.

Sequence of CPU Functions



Storage Direct

Mnemonic: L (load reg)
ST (store reg)



This instruction directly accesses any of 128 addresses of control storage (the fixed storage area; addresses 0000-007F) during read or write operations. Main storage cannot be accessed with this instruction, Two bytes of data are transferred.

W (Bit 4): Indicates whether a read or write operation is to occur:

- W = 0: Read from control storage to the selected register.
- W = 1: Write to control storage using the selected register for source.

Reg1 (Bits 5-7): Selects one of eight registers in the LSR stack. Two bytes of data are transferred between this register and control storage.

Bit 8: Always 0, a modifier bit to the op code (bits 0-3).

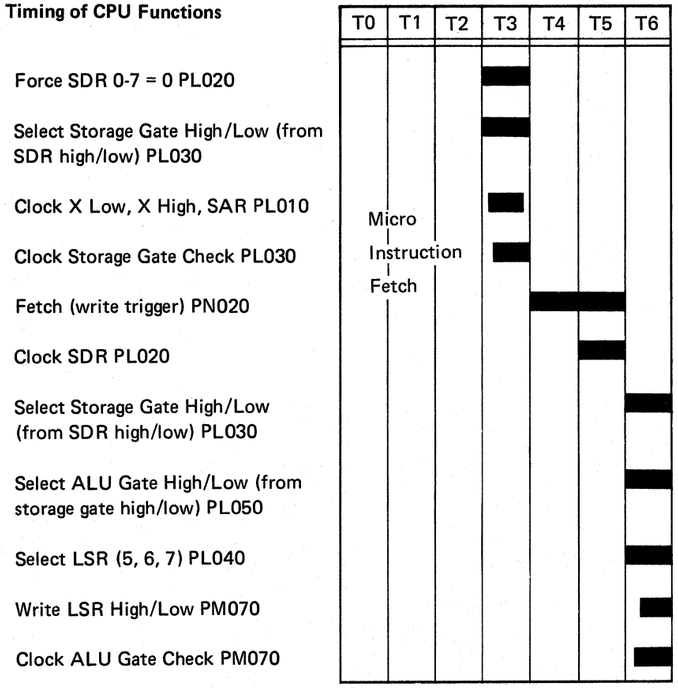
SAR (Bits 9-15): Specifies one of the first 128 locations in control storage. These 7 bits directly replace the corresponding 7 bits in the storage address register (SAR). Bits 0 through 8 of SAR are set to zeros.

Condition Code

No change.

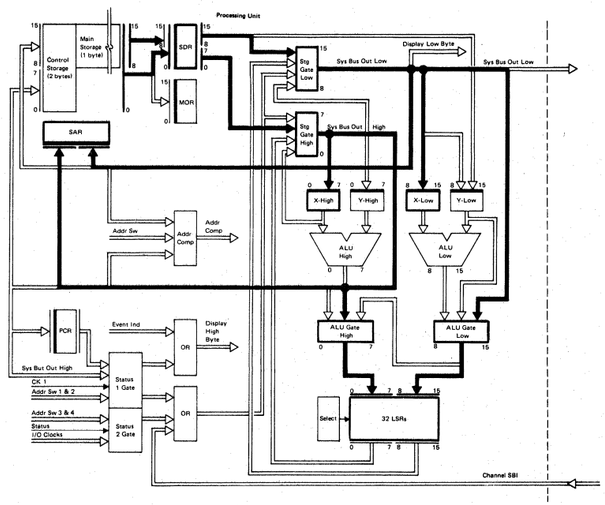
Storage Direct (Read from Control Storage)

Timing of CPU Functions

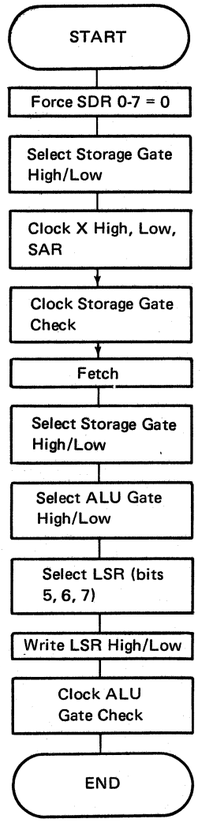


T-Times = 200 ns

Specific CPU Data Path

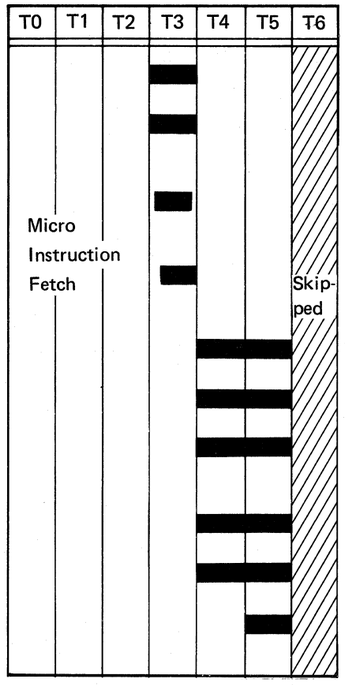


Sequence of CPU Functions



Storage Direct (Write to Control Storage)

Timing of CPU Functions



Force SDR 0-7 = 0 PL020

Select Storage Gate High/Low (from SDR high/low) PL030

Clock X Low, X High, SAR PL010

Clock Storage Gate Check PL030

Storage Cycle PN030

Select LSR (5, 6, 7) PL040

Select Storage Gate High/Low (from LSR high/low) PL030

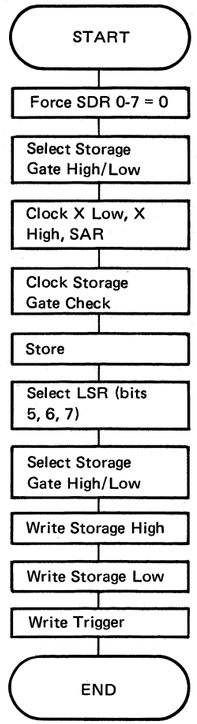
Write Storage High PN030

Write Storage Low PN030

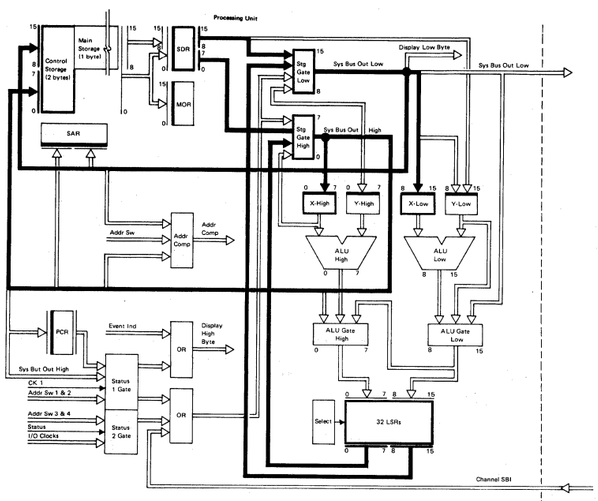
Clock SDR (write trigger) PL020

T-Times = 200 ns

Sequence of CPU Functions

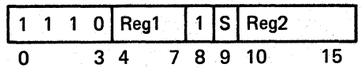


Specific CPU Data Path



Move LSR

Mnemonic: MVR



This instruction moves the contents of one LSR to another LSR. Two bytes of data are always moved. Any of the 32 LSRs in the stack can be accessed. Data can be moved either from Reg1 to Reg2 or from Reg2 to Reg1 depending on the setting of bit 0.

Reg1 (Bits 4-7): Selects one of 16 LSRs. The group being selected depends on the program level currently being processed. Eight of these registers are always the MAR/MAB stack (specified by bit 4 = 1). The other 8 of the 16 registers that can be specified in the Reg1 field are the work registers (WRs) associated with the program level currently selected. These registers are selected by specifying 0-7 in the Reg1 field.

Bit 8: Always a 1, bit 8 is a modifier to the op code (bits 0-3).

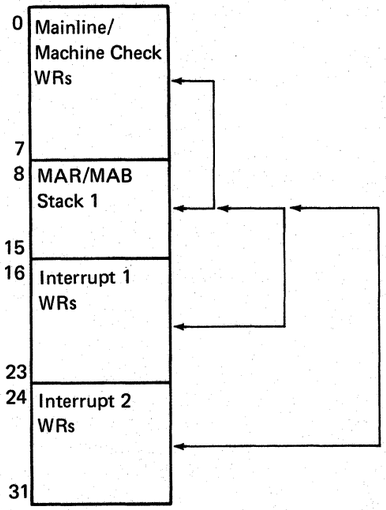
S (Bit 9): Indicates the direction in which the data is to be transferred. S = 0 means Reg1 is the source register and 2 bytes of data are transferred from Reg1 to Reg2. S = 1 means Reg2 is the source register and 2 bytes of data are transferred from Reg2 to Reg1.

Reg2 (Bits 10-15): The low order 5 bits of this field select one of the 32 LSRs in the data flow (bit 10 = 0). Two bytes of data are moved to or from this field depending on the bit setting of the S field.

Condition Code

No change.

Valid Reg1 Field Register Specification



Valid combinations that can be specified in the Reg1 field of move LSR are:

1. If in mainline or machine check, the registers that can be specified are 0-7 and 8-15.
2. If in interrupt level 1, the registers that can be specified are 16-23 and 8-15.
3. If in interrupt level 2, the registers that can be specified are 24-31 and 8-15.

Timing of CPU Functions

Select LSR (4-7 if 9=0 10-15 if 9=1) PL040

Clock X Low and X High (SAR don't care) PL010

Clock Storage Gate Check PL030

ALU (pass)

Select Storage Gate High/Low (from LSR high/low) PL060

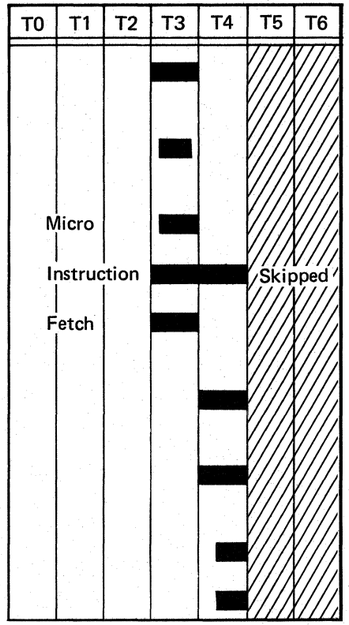
Select LSR (10-15 if 9=0; 4-7 if 9=1) PL040

Select ALU Gate High/Low (from ALU high/low) PL050

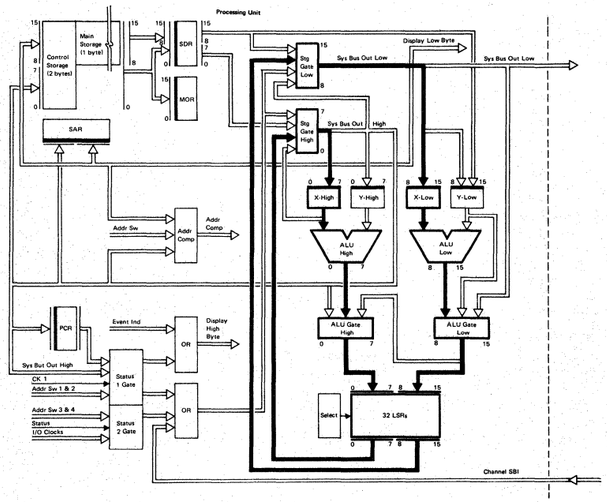
Write LSR High/Low PM070

Clock ALU Gate Check PM070

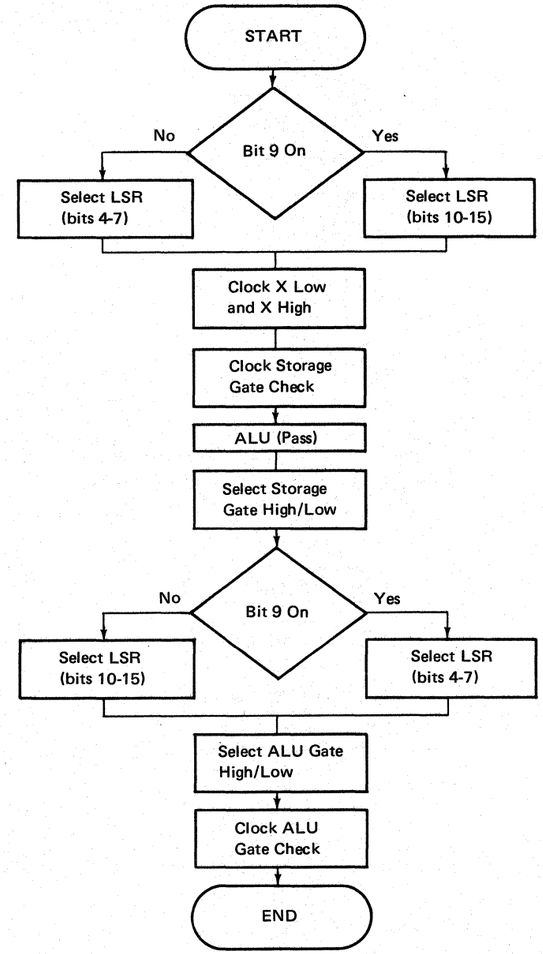
T-Times = 200 ns



Specific CPU Data Path

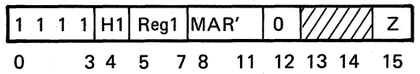


Sequence of CPU Functions



Hex Branch

Mnemonic: HBN (numeric)
HBZ (zone)



This instruction operates as a 16 way unconditional branch. Either the zone or digit portion of either the high or low byte of the selected register is used to replace bits 12-15 of MAR. Bits 8-11 of MAR are replaced by the bit settings of MAR'.

H1 (Bit 4): Indicates which byte of the selected register in the LSR stack is to be used in the hex branch:

- H1 = 0: Low byte of the register is to be used.
- H1 = 1: High byte of the register is to be used.

Reg1 (Bits 5-7): Causes selection of one of eight registers in an LSR stack. The zone or digit portion of the selected register is used and replaces bits 12-15 of MAR.

MAR' (Bits 8-11): Replaces bits 8-11 of MAR. Bits 0-7 of MAR are not changed by this instruction.

Bit 12: Always 0, a modifier to the op code (bits 0-3).

Bits 13 and 14: Not used in the next branch instruction.

Timing of CPU Functions

Select LSR (5, 6, 7) PL040

Select Storage Gate High (from LSR high) PL030

Select Storage Gate Low (from LSR low: 4=0, storage gate high: 4=1) PL030

Clock X High, X Low, SAR (don't care) PL010

Clock Storage Gate Check PL030

Select Y Data (from SDR) PL010

Clock Y Reg, Block Reset Y PL010

ALU Function (pass) PL060

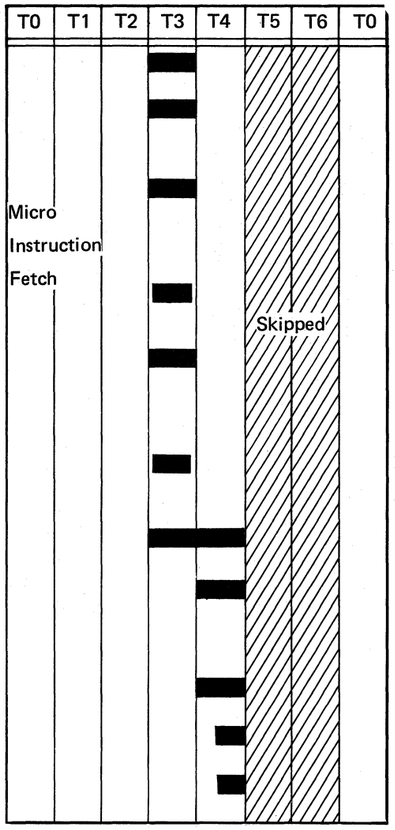
ALU Gate Low (from Y zone X numeric: 15=0; Y zone X zone: 15=1) PL050

Select LSR (MAR) PL040

Write LSR Low PM070

Clock ALU Gate Check PM070

T-Times = 200 ns



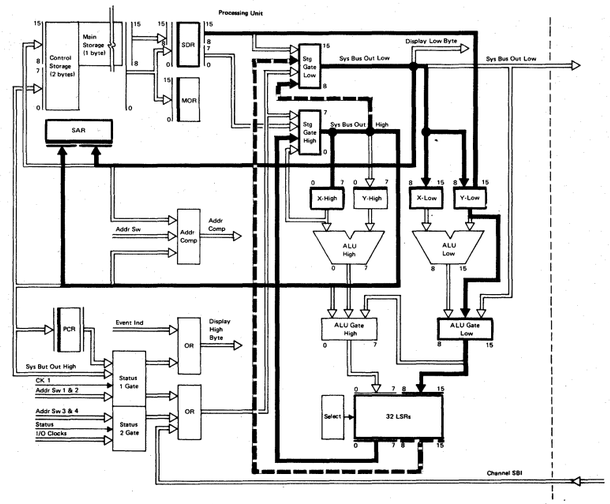
Z (Bit 15): Causes either the zone or digit portion of the selected register to be used in the hex branch function:

- Z = 0: Digit portion of data byte of selected register replaces bits 12-15 of MAR.
- Z = 1: Zone portion of data byte of selected register replaces bits 12-15 of MAR.

Condition Code

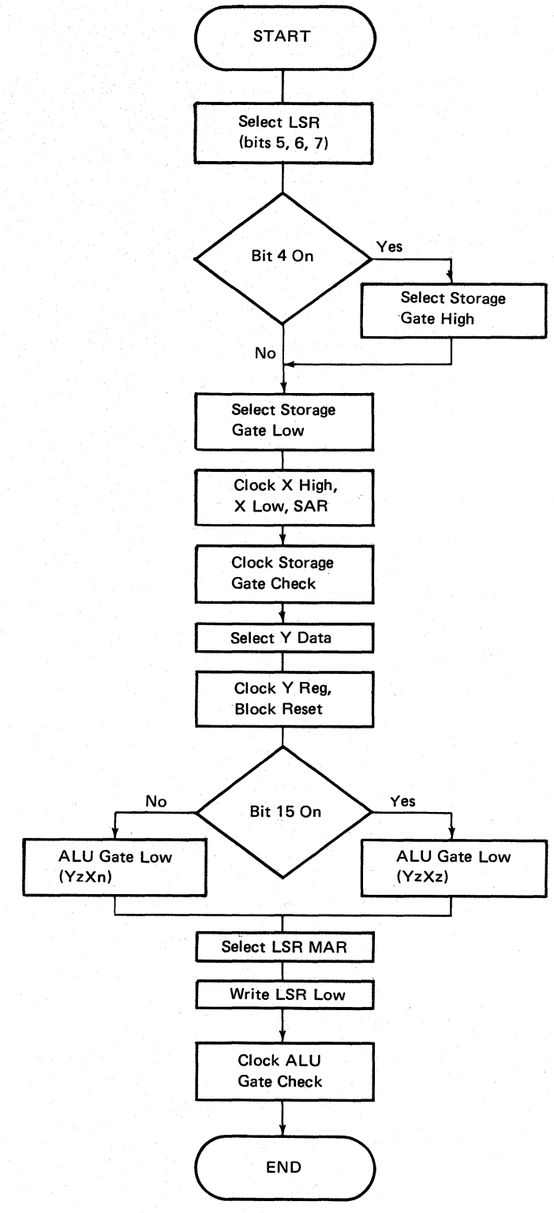
No change.

Specific CPU Data Path

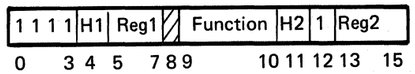


▬ ▬ ▬ Options depending on contents of bit 4.

Sequence of CPU Functions



Hex Move



Mnemonics: SRL
SRLD
MZZ
MZN

This instruction performs the following functions:

1. Shift right logical 8 bits of register (Reg1).
2. Shift right logical double 16 bits of register (Reg1).
3. Link the zone portion of Reg2 to the zone portion of Reg1 and put the result into Reg1 in the following format:

Reg2 Zone	Reg1 Zone

4. Link the zone portion of Reg2 to the numeric portion of Reg1 and put the results into Reg1 in the following format:

Reg2 Zone	Reg1 Numeric

H1 (Bit 4): Indicates which byte of the selected register in the LSR stack is to be used:

H1 = 0: Low byte of the register is to be used.
H1 = 1: High byte of the register is to be used.

The H1 field is not used for the shift right logical double function.

Reg1 (Bits 5-7): Causes selection of one of eight registers in an LSR stack.

Bit 8: Not used.

Function (Bits 9 and 10): Specifies one of the following functions:

Bits 9 and 10 = 00: Reg1 shift right logical (SRL). The 8 bits of the selected byte are shifted one position to the right. The high order (leftmost) bit is replaced with a zero. The Reg2 and H2 fields of the hex move instruction are not used for the shift right logical function.

Bits 9 and 10 = 01: Reg1 shift right logical double (SRLD). The 16 bits of the selected register are shifted one position to the right. The high order bit (bit 0) is replaced with a zero. The H1, H2, and Reg2 fields of the hex move instruction are not used for the shift right logical double.

Bits 9 and 10 = 10: Link zone portion of Reg2 to the zone portion of Reg1 (MZN). The zone digit of the register specified in Reg2 is moved to the zone position of the register specified in Reg1. The zone digit of the register specified by Reg1 is moved to the numeric portion of the register specified in Reg1. The results are put in the register specified by Reg1 and have the following format:

Reg2 Zone	Reg1 Zone

Example: Reg1 0110 1000
Reg2 1111 0010
Result 1111 0110

Bits 9 and 10 = 11: Link the zone portion of Reg2 to the numeric portion of Reg1 (MZZ). The zone digit of the register specified in Reg2 is moved to the zone position of the register specified by Reg1 and the numeric digit of the register specified in Reg1 is unchanged. The results are put in the register specified by Reg1 and have the following format:

Reg2 Zone	Reg1 Numeric

Example: Reg1 0110 1001
Reg2 1111 0010
Result 1111 1001

H2 (Bit 11): Indicates which byte of the selected register (specified by Reg2) in the LSR stack is to be used:

H2 = 0: Low byte of the register is to be used.
H2 = 1: High byte of the register is to be used.

The H2 field is not used in the shift right logical and shift right logical double functions.

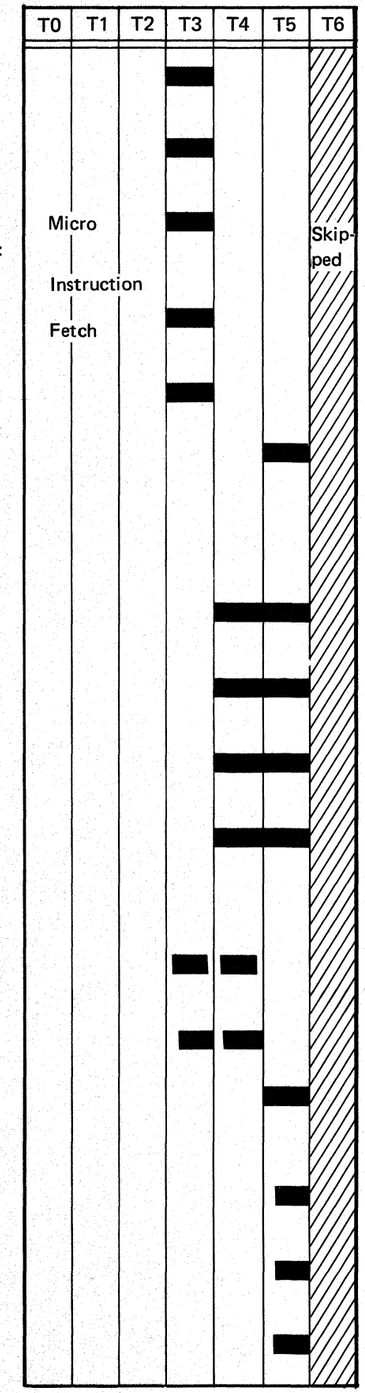
Bit 12: Always 1, a modifier to the op code (bits 0-3).

Reg2 (Bits 13-15): Causes selection of one of eight registers in the LSR stack. The Reg2 field is not used in the shift right logical and shift right logical double functions.

Condition Code

No change.

Timing of CPU Functions



Select LSR (13, 14, 15) (Reg2) PL040

Select Storage Gate High (from LSR high) PL030

Select Storage Gate Low (from LSR low: 11=0, storage gate high: 11=1) PL030

Select Y Data (from storage gate) PL010

Clock Y, X High, and SAR (block reset) PL010

ALU Gate Low (Bits 9, 10)
0 0 R1 SRL1→R1
0 1 R1 SRDL1→R1
1 0 R2(Z) R1 (Z)→R1
1 1 R2(Z) R1 (N)→R1
PL050

ALU Function (pass; block reset Y) PL060

Select LSR (5, 6, 7) (Reg1) PL040

Select Storage Gate High (from LSR high) PL030

Select Storage Gate Low (from LSR low: 4=0, or 9, 10=01, storage gate high: 4=1 and 9, 10=$\overline{01}$) PL030

Clock X Low, X High, SAR PL010

Clock Storage Gate Check PL030

Select ALU Gate High (from ALU gate low: 4=1 and 9,10=$\overline{11}$) PL050

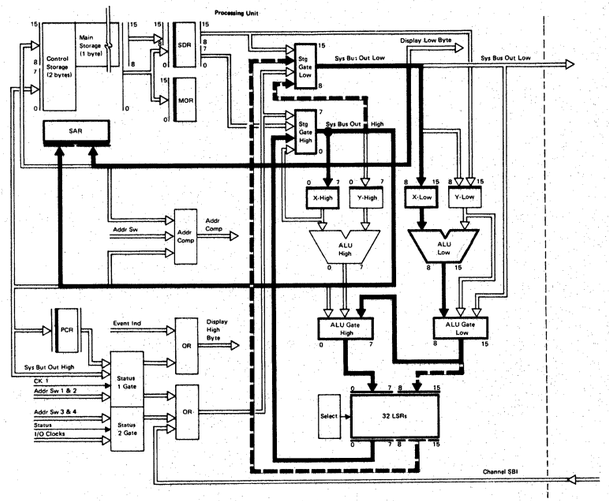
Write LSR High (4=1 or 9,10=01) PM070

Write LSR Low (4=0 or 9,10=01) PM070

Clock ALU Gate Check PM070

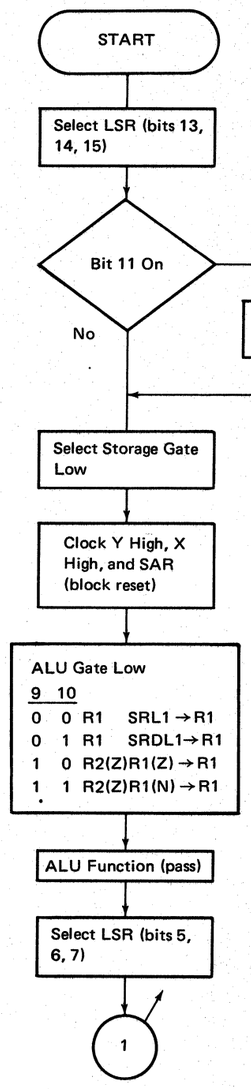
T-Times = 200 ns

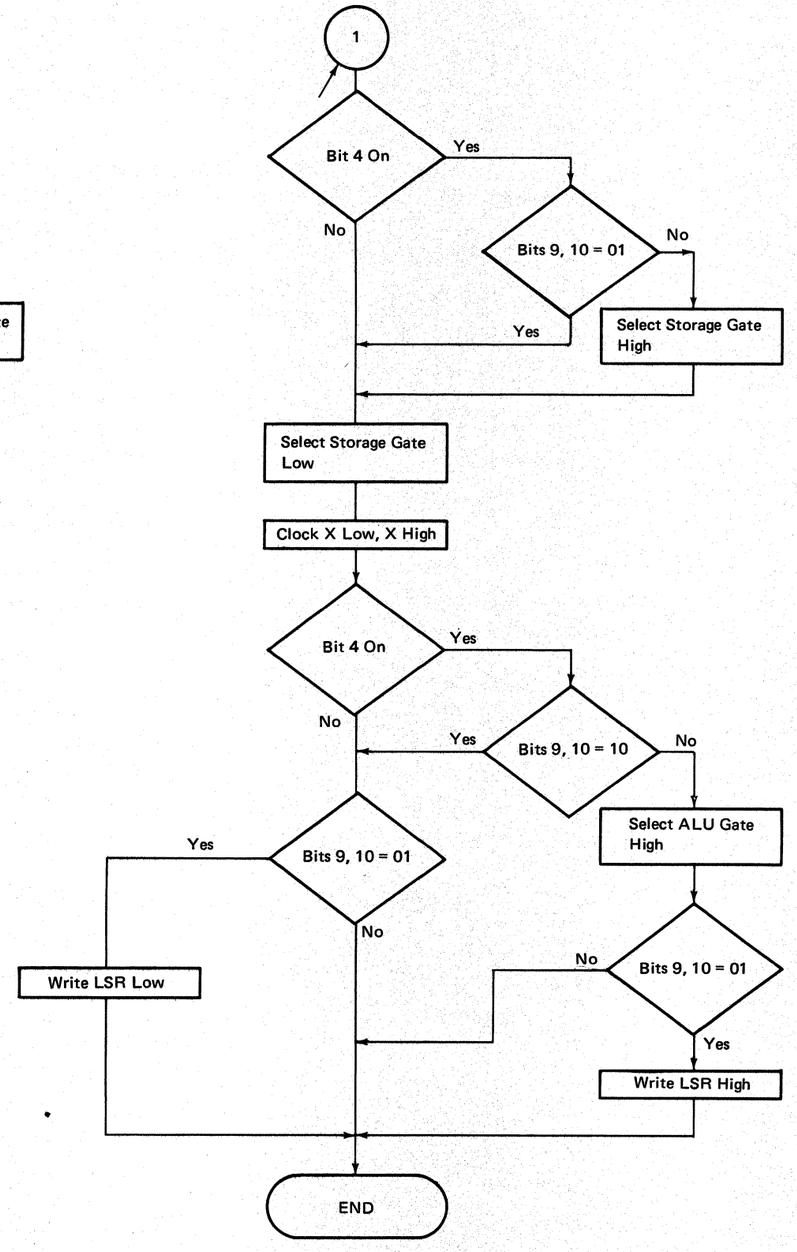
Specific CPU Data Path



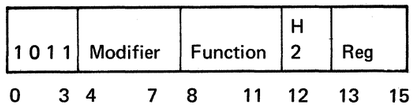
▬ ▬ ▬ Options depending on the contents of bits 4, 9, 10 and 11.

Sequence of CPU Functions





I/O IMMEDIATE



The I/O immediate instruction has two main functions:

1. Transfer a single byte of data between the LSRs and I/O devices, and
2. Direct control of CPU, channel, and I/O functions that may or may not include data transfer.

Modifier (Bits 4-7): The modifier bits are device dependent and are sent to the attachment. Along with the CBO bits, these bits define what is to be done.

Function (Bits 8-11): The function bits are sent to the port where they are decoded as one of the following commands:

Load
Sense
Control load
Control sense

This command is then sent to the attachment on the CBO.

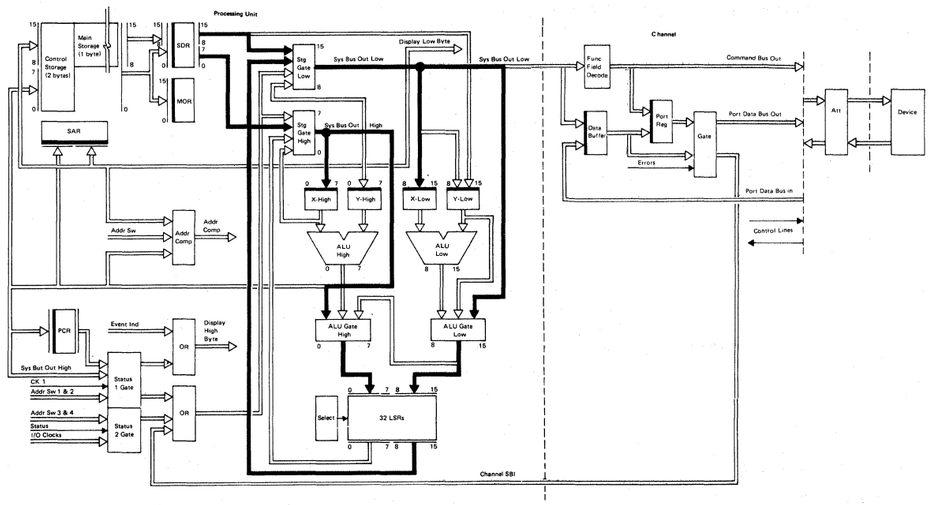
If bits 10 and 11 = 10, the command does not go to the port but stays in the CPU. For further definition of the commands, see μINSTR-30.

H2 (Bit 12): This bit is used to select the high or low byte of the selected LSR.

Reg (Bits 13-15): This field selects one of eight registers in an LSR stack. This register is used for the byte of data or control information that is to be sent or received.

Note: For CPU control instructions, bits 12-15 are used as a second set of modifier bits.

Specific CPU Data Path



Timing of CPU Functions

Select LSR (WR0) PL040

SDR High
SDR Low
LSR Low PL030

Select Storage Gate High (from SDR high) PL030

Clock SAR, X High, X Low PL010

Advance Time PH010

Select LSR 13, 14, 15 PL040

Select Storage Gate High (from LSR high) PL030

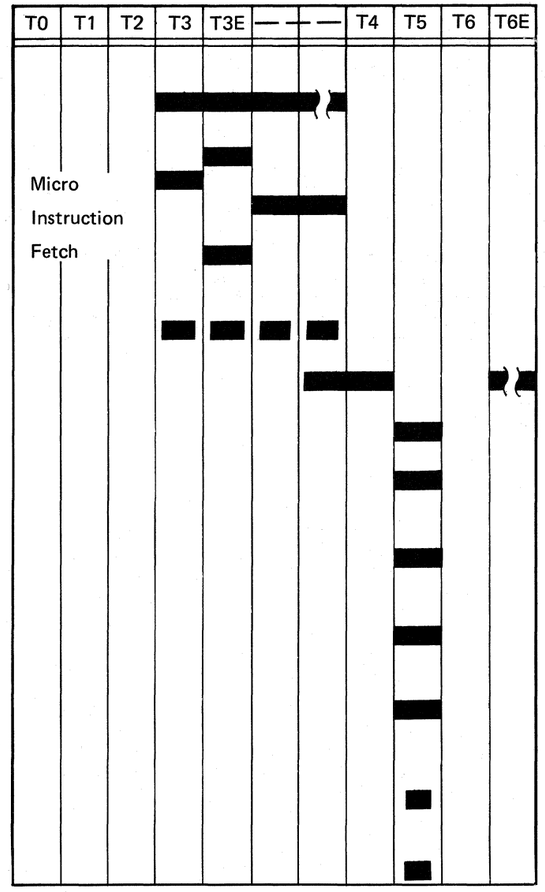
Select Storage Gate Low (from channel bus:9= 1; LSR:9=0) PL030

Select ALU Gate Low (from storage gate low) PL050

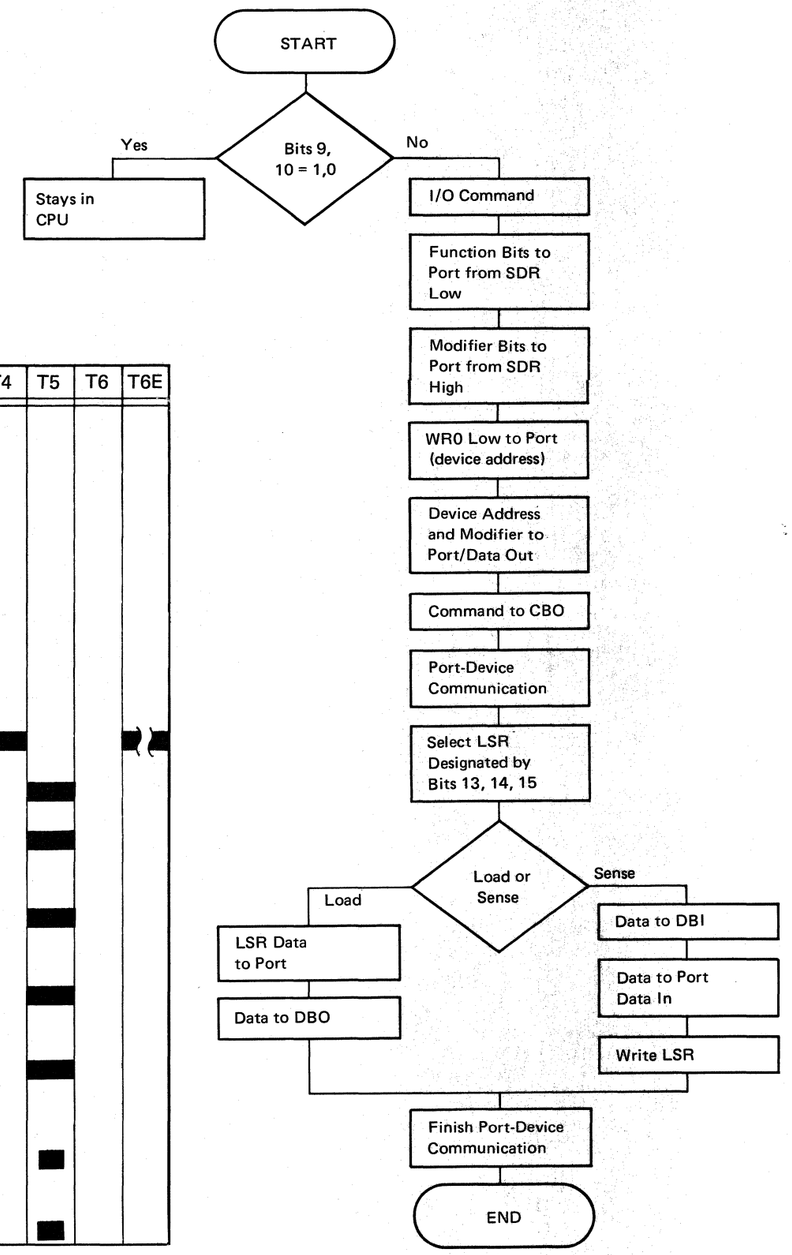
Select ALU Gate High (from ALU gate low) PL050

Write LSR Low (9=1, 12=0) PM070

Write LSR High (9=1, 12=1) PM070



CPU/Port Communications



I/O IMMEDIATE (continued)

Order of Significance →

Op Code	Function	Device Address	Modifier	Address of LSR Containing Data Used by Instruction
0 1 2 3	8 9 10 11	WR0 Low	4 5 6 7	12 13 14 15
1 0 1 1				

0 = I/O Load (See μINSTR-31.)

- 10 = Keyboard, KBD-6
- 40 = Display Screen, DISP-14
- 50 = MCU, Magnetic character reader, or Data Recorder (if installed)
- A0 = Disk, DISK-11
- D0 = 33FD, 33FD-16
- E0 = Printer, PTR-8; S-PTR-10

4 = I/O Sense (See μINSTR-32.)

- 00 = Channel, see A this page
- 10 = Keyboard, KBD-12
- 40 = Display Screen, DISP-19
- 50 = MCU, Magnetic character reader, or Data Recorder (if installed)
- A0 = Disk, DISK-13
- D0 = 33FD, 33FD-18
- E0 = Printer, PRT-14; S-PTR-14

8 = I/O Control Load (See μINSTR-31.)

- 00 = Channel, see B this page
- 10 = Keyboard, KBD-8
- 40 = Display Screen, DISP-16
- 50 = MCU, Magnetic character reader, or Data Recorder (if installed)
- A0 = Disk, DISK-11
- D0 = 33FD, 33FD-20
- E0 = Printer, PTR-10; S-PTR-12

C = I/O Control Sense (See μINSTR-32.)

- 10 = Keyboard, KBD-14
- 40 = Display Screen, DISP-21
- 50 = MCU, Magnetic character reader, or Data Recorder (if installed)
- A0 = Disk, DISK-13
- D0 = 33FD, 33FD-32
- E0 = Printer, PTR-14; S-PTR-16

5 = Sense Interrupt Level Status Byte (See μINSTR-33.)

- 10 = Disk, DISK-14 (WR0[L] contains interrupt level being sensed)
- 20 = Keyboard, KBD-18; Printer, PTR-18; S-PTR-18
- 30 = MCU, Magnetic character reader, or Data Recorder (if installed)

6 = Microprocessor Sense See C this page.

A = Microprocessor Load See D this page.

1, 3, 7, B, D, E, F Invalid

A Channel I/O Sense

4 5 6 7	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0000 Sense Port Register	Data							
0001	Port Data Bus Out	Invalid Device Address	DBI P Check	I/O Timeout Check	CBI/ DBI Not Zero	System Bus P Check	Cycle Steal Check	Invalid Channel

B Channel I/O Control Load

Modifier Bits 4-7	Function	Bits 12-15
0000	Disable 33FD Timeout	Not Used
0001	Load Port Register	H Reg 2 2 Data to be Loaded
0010	Reset Port Errors	Not Used
0011	Enable 33FD Timeout	Not Used
0100	Reset Start Light	Not Used
0101	Set Channel Odd Parity	Not Used
0110	Set Channel Even Parity	Not Used
0111	Set Start Light	Not Used

C CPU Microprocessor Sense

The contents of these bytes or switches are moved to an LSR. This data can then be used by the program.

4 5 6 7	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0 1 0 0 Console Status Byte	Stop Key	Main Storage Address Compare	Overlap Off	IPL Device Select Switch	I/O Request	Sys Step Mode	Go Flag	Micro Interrupt Check
0 1 0 1 Address Data Switches 3 and 4	Switch 3 8	Switch 3 4	Switch 3 2	Switch 3 1	Switch 4 8	Switch 4 4	Switch 4 2	Switch 4 1
0 1 1 0 I/O Clocks Low Byte[1]	8.19 ms	16.38 ms	32.77 ms	65.54 ms	131.1 ms	262.1 ms	524.3 ms	1s
0 1 1 1 I/O Clocks High Byte[1]	32 μs	64 μs	128 μs	256 μs	512 μs	1.02 ms	2.05 ms	4.10 ms
1 0 0 1 Address Data Switches 1 and 2	Switch 1 8	Switch 1 4	Switch 1 2	Switch 1 1	Switch 2 8	Switch 2 4	Switch 2 2	Switch 2 1
1 0 1 0 CPU Error Byte	SDR P Check	MOR P Check	Storage Gate P Check	ALU Gate P Check	Control Storage Invalid Addr/ SAR Check	Main Storage Invalid Addr/ SAR Check	Not Used	Microloop Check
1 0 1 1 PCR	Flag	Plus	Minus	Zero	Carry Log	Hi Log	Low Log	Equal Log

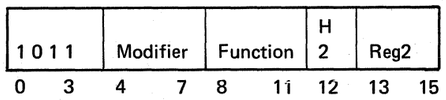
[1] Contents of these bytes are in 1's complement form.

D Micro Processor Load

Modifier Bits 4-7		Modifier 2 Bits 12-15
0000	Load PCR, PK003 (Modifier 2 is high byte of WR7)	1111
0001	Reset Carry-Set Equal	1111
0010	Reset Event Indicator 2, PK001	1111
0011	Reset Event Indicator 3, PK001	1111
0100	Reset Event Indicator 4, PK001	1111
0101	Reset Event Indicator 5, PK001	1111
0110	Reset Event Indicator 6, PK001	1111
0111	Reset Event Indicator 7, PK001	1111
1000	Set Flag	1111
1001	No-Op	1111
1010	No-Op	1111
1011	Reset Flag	1111
1100	No-Op	1111
1101	No-Op	1111
1110	No-Op	0000
1110	Set I/O Service Request, PJ040	0001
1110	Reset I/O Service Request, PJ040	0010
1110	Processor Check Halt, PJ010	0011
1110	Disable Checks, PJ010	0100
1110	Enable Interrupts, PJ040	0101
1110	Disable Interrupts, PJ040	0110
1110	Enable Checks, PJ010	0111
1110	No-Op	1000
1110	No-Op	1110
1111	Set CPU Working, PJ020	0000
1111	Reset Stop Latch, PJ060	0001
1111	Reset MCI Latch, PJ010	0010
1111	Reset Go Latch, PJ020	0011
1111	Enable Microloop Timeout (not) Reset Timeout, PJ010, (PJ060)	0100
1111	Set Stop Latch	0101
1111	Reset Retry/Microloop Time-out and Set Go Latch	0110
1111	Set Retry, PJ020	0111
1111	Enable I/O Clocks, PJ080	1000
1111	No-Op	1001
1111	Reset I/O Clocks, PJ080	1010
1111	Disable I/O Clocks, PJ080	0011
1111	No-Op	1100
1111	Reset CPU Working, PJ020	1101
1111	Processor Wait, PJ060	1110

I/O Load

Mnemonic: IOL, IOCL



This function of the I/O immediate instruction is used to transfer 1 byte of data or control information from an LSR to an I/O attachment.

Instruction Fields

Modifier: The modifier bits are device dependent and are sent to the attachment along with the command. They define what is to be done with the data byte that will be sent.

Function: The function bits are sent to the channel where they are decoded as one of the following commands:

Load
Control Load

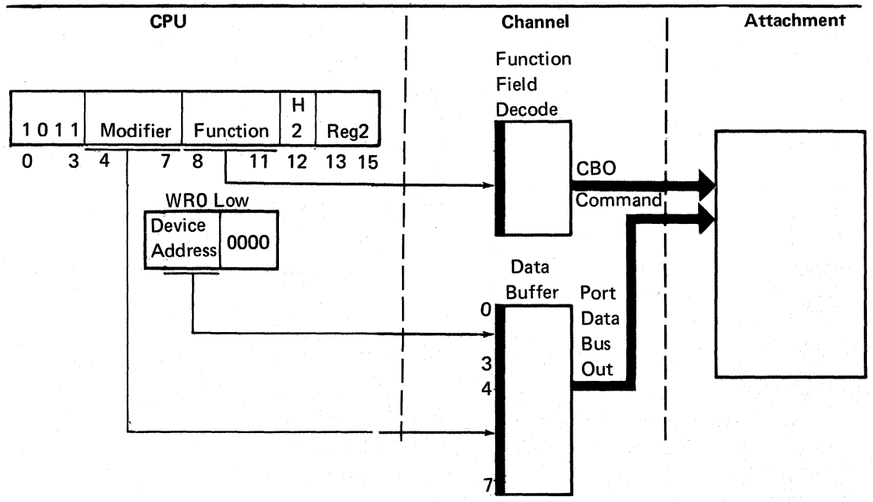
This command is then sent to the attachment on the CBO.

H2: This bit is used to select the high or low byte of the selected LSR:

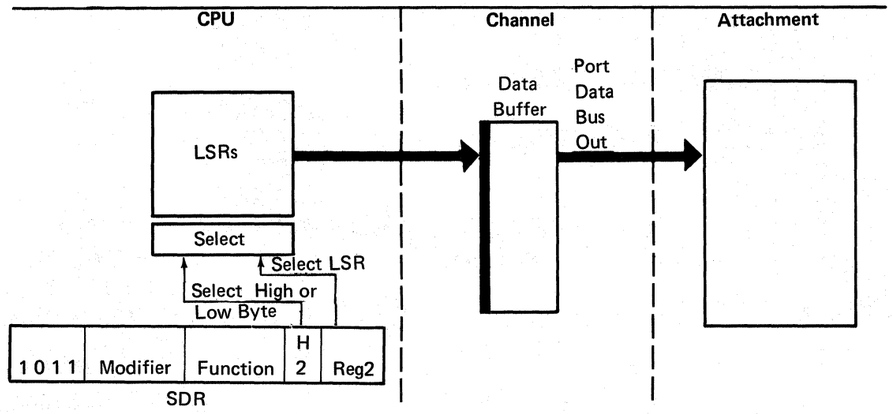
H2 = 0: Select low byte.
H2 = 1: Select high byte.

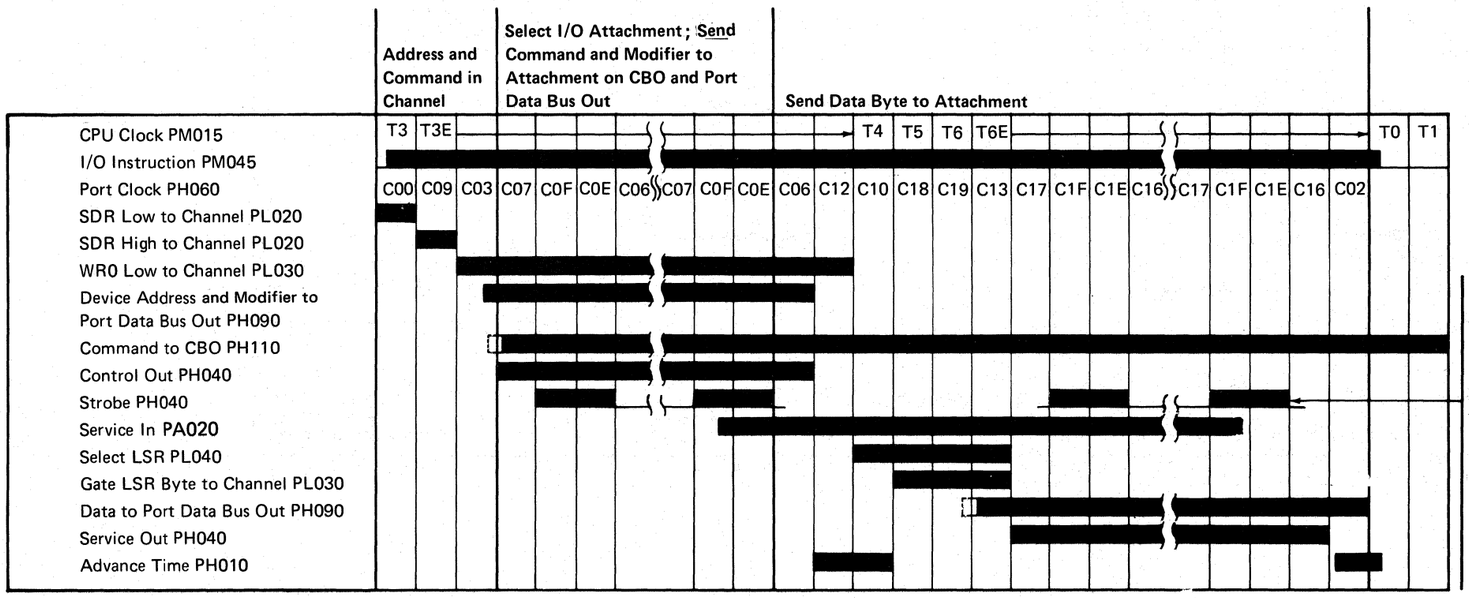
Reg2: This field selects one of eight registers in an LSR stack. This register will contain the byte of data or control information that is to be sent to the attachment.

Select Attachment
(Address, Modifier and Command to Attachment)



Send Data Byte to Attachment

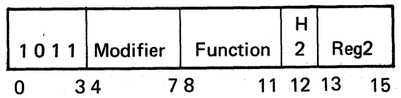




— The first 'strobe' after the rise of 'control out' signals the attachment that the address and command information on the CBO and port data out is valid. The rise of 'service in' signals the port that the attachment has taken the information from the CBO and port data bus out and is ready to receive data.
— The first 'strobe' after the rise of 'service out' signals the attachment that the data byte on the DBO is valid. The fall of 'service in' signals the port that the attachment has taken the data byte from the DBO.

I/O Sense

Mnemonic: IOS, IOCS



This function of the I/O immediate instruction is used to transfer 1 byte of data or status type information from an I/O attachment to an LSR.

Instruction Fields

Modifier: The modifier bits are device dependent and are sent to the attachment along with the command. They define what data byte is to be sent.

Function: The function bits are sent to the port where they are decoded as one of the following commands:

Sense
Control Sense

This command is sent to the attachment on the CBO.

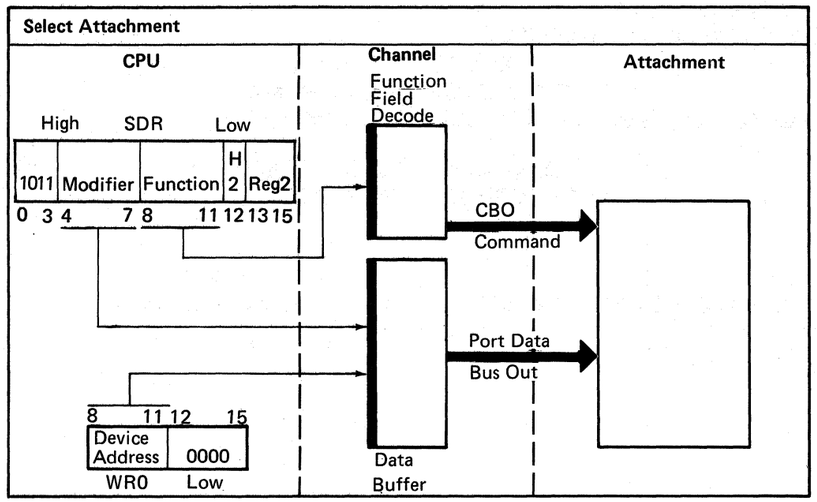
H2: This bit is used to select the high or low byte of the selected LSR:

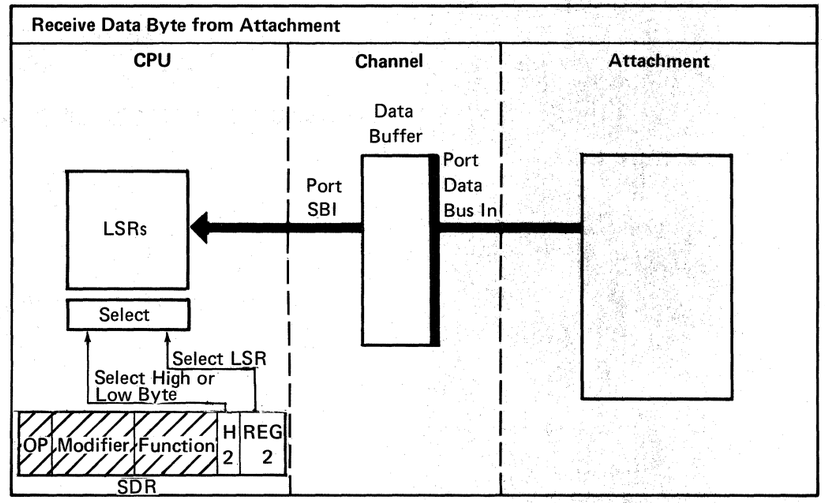
H2 = 0: Select low byte.
H2 = 1: Select high byte.

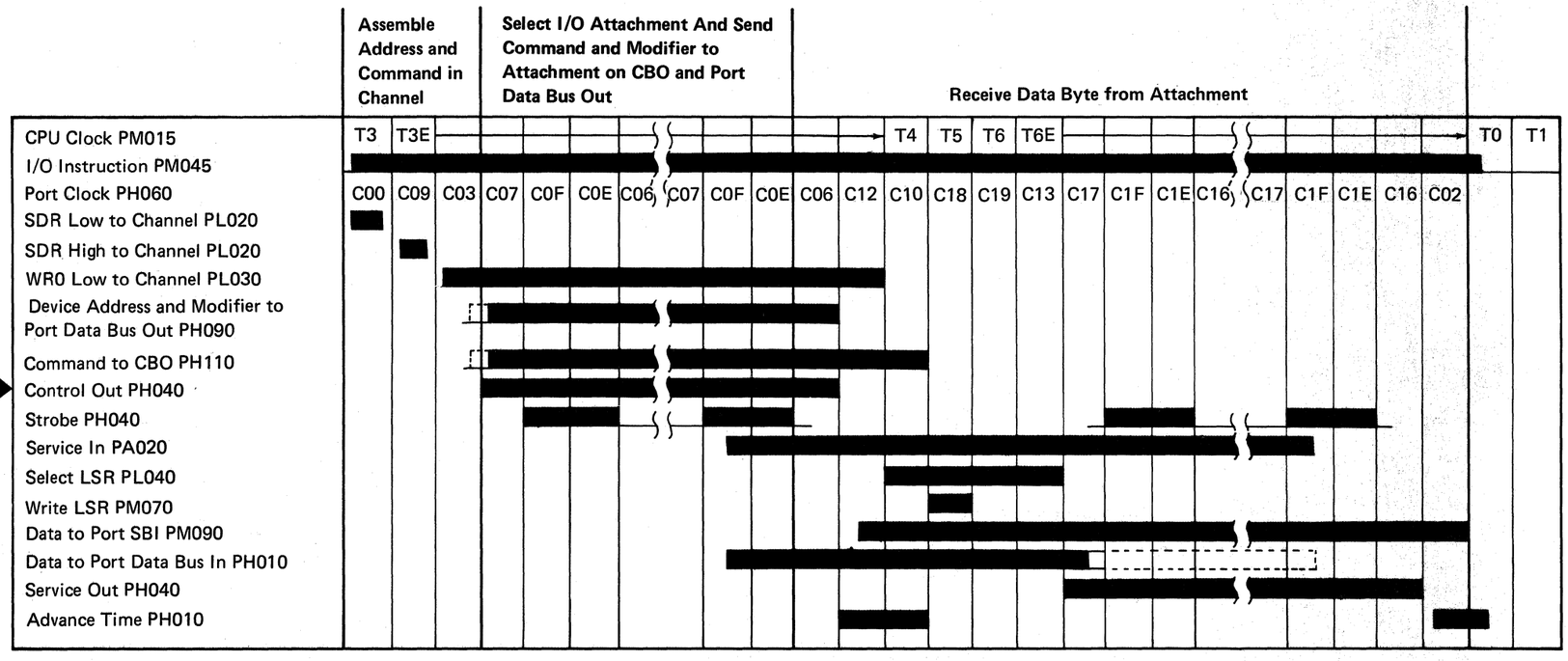
Reg2: This field selects one of eight registers in an LSR stack. The byte of data being sent from the attachment will be placed in this LSR.

The 1st 'strobe' after the rise of 'control out' signals the attachment that the address and command information on the CBO and port data bus out is valid.

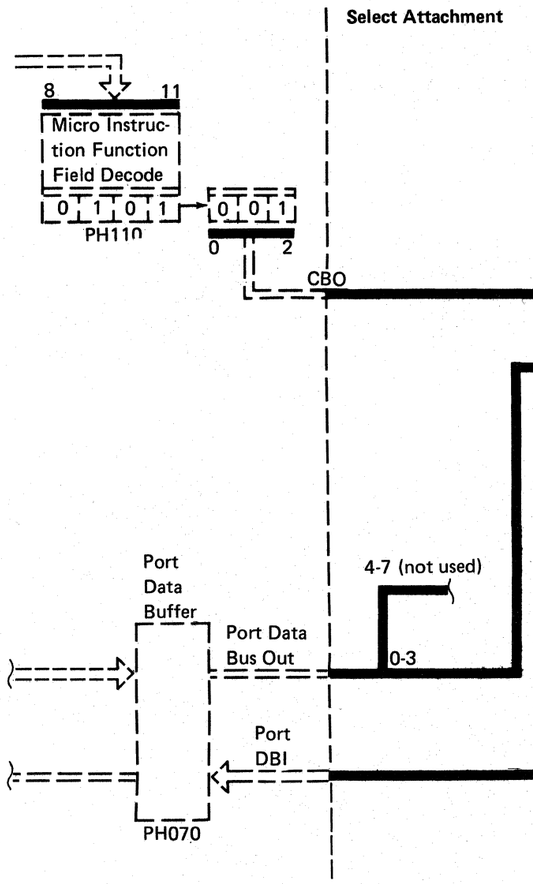
The rise of 'service in' signals the port that the attachment has taken the information from the CBO and port data out. The rise of 'service in' also signals the port that the data byte on the port data bus is valid. The rise of 'service out' signals the attachment that the channel has taken the byte from the port data bus in.







Sense Interrupt Level Status Command



Select Attachment

Send Status Byte To Channel

		DBI							
		Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
0 0 1	0 0 0 1 Interrupt Level 1								Disk drive
	0 0 1 0 Interrupt Level 2		Keyboard	BSCA/SDLC	Printer				
	0 0 1 1 Interrupt Level 3		MCU, Magnetic Character Reader, or Data Recorder						

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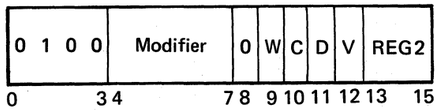
I/O Storage



The function of I/O storage is to transfer 1 byte of data between main/control storage and the I/O attachment.

Modifier (Bits 4-7): Control fields for the I/O attachment. The field is transferred to the attachment through the port. Bit 4 of this field is used in the CPU to select the high or low byte of control storage. When main storage is being accessed, bit 4 is not used by the CPU.

Bit 8: Modifier to the op code (bits 0-3). Bit 8 is a zero for I/O storage.

W (Bit 9): Identifies the direction of the transfer. W = 0 causes a read from storage and a transfer to the I/O attachment, W = 1 causes a write to storage.

C (Bit 10): Selects main storage or control storage. C = 0 selects main storage; C = 1 selects control storage.

D (Bit 11): Indicates whether the address in the LSR (specified by bits 13-15) are to be incremented (D = 0) or decremented (D = 1).

V (Bit 12): Indicates the amount the address in the LSR (specified by bits 13-15) should be incremented or decremented. If V = 0, the address in the selected LSR is not changed. If V = 1, the address in the selected LSR is decremented or incremented by one depending on the bit setting of the D field.

REG2 (Bits 13-15): Selects one of the eight LSRs dedicated to the present operating level that contains the storage address needed for the data transfer. The address in the specified LSR may be updated depending on bits 11 (D field) and 12 (V field).

Condition Code

Not affected.

Bits 8-11 are sent to the port where they are decoded as one of the following commands:

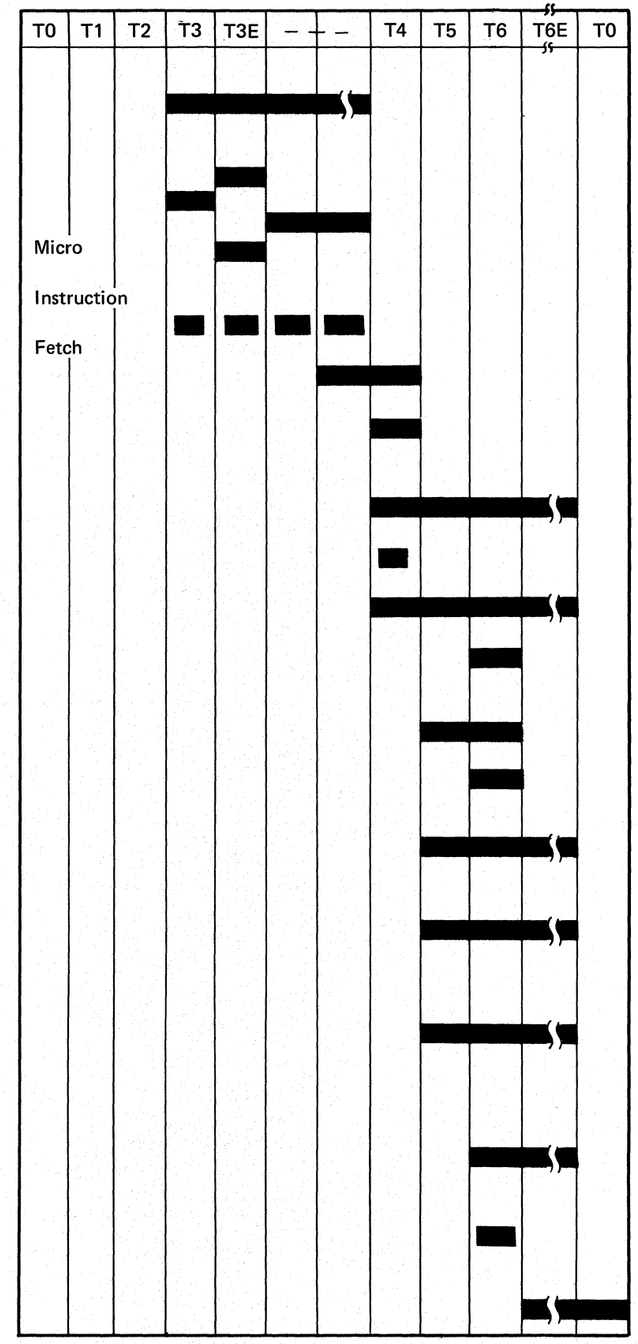
Load
Sense

This command is then sent to the attachment on the CBO.

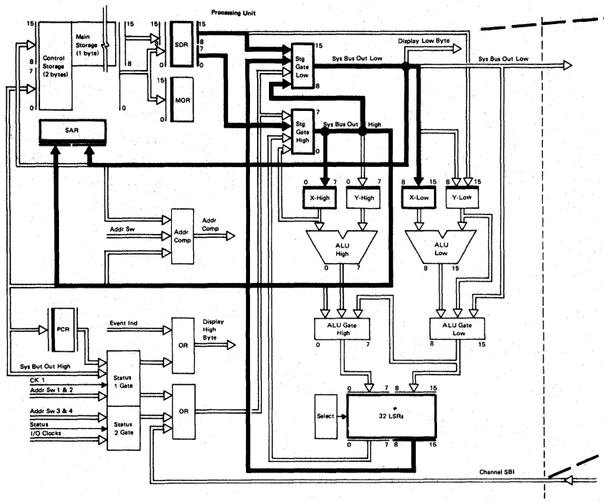
Bits 4 8 9 10 11 12	Mnemonic	Description
0 0 1 1 0 1 / 1 0 1 1 0 1	WTCL / WTCH	I/O load to control storage increase R2 by 1.
0 0 1 1 1 1 / 1 0 1 1 1 1	WTCL / WTCH	I/O load to control storage decrease R2 by 1.
0 0 1 1 0 0 / 1 0 1 1 0 0	WTCL / WTCH	I/O load to control storage R2 (no change)
0 0 0 1 0 1 / 1 0 0 1 0 1	RDCL / RDCH	I/O storage from control storage increase R2 by 1.
0 0 0 1 1 1 / 1 0 0 1 1 1	RDCL / RDCH	I/O storage from control storage decrease R2 by 1.
0 0 0 1 0 0 / 1 0 0 1 0 0	RDCL / RDCH	I/O storage from control storage. R2 (no change).
X 0 1 0 0 1	WTM	I/O load to main storage, increase R2 by 1.
X 0 1 0 1 1	WTM	I/O load to main storage, decrease R2 by 1.
X 0 1 1 1 1	WTM	I/O load to main storage, no change to R2.
X 0 0 0 0 1	RDM	I/O storage from main storage, increase R2 by 1.
X 0 0 0 1 1	RDM	I/O store from main storage, decrease R2 by 1.
X 0 0 0 0 0	RDM	I/O store from main storage, no change to R2.

X = Not used.

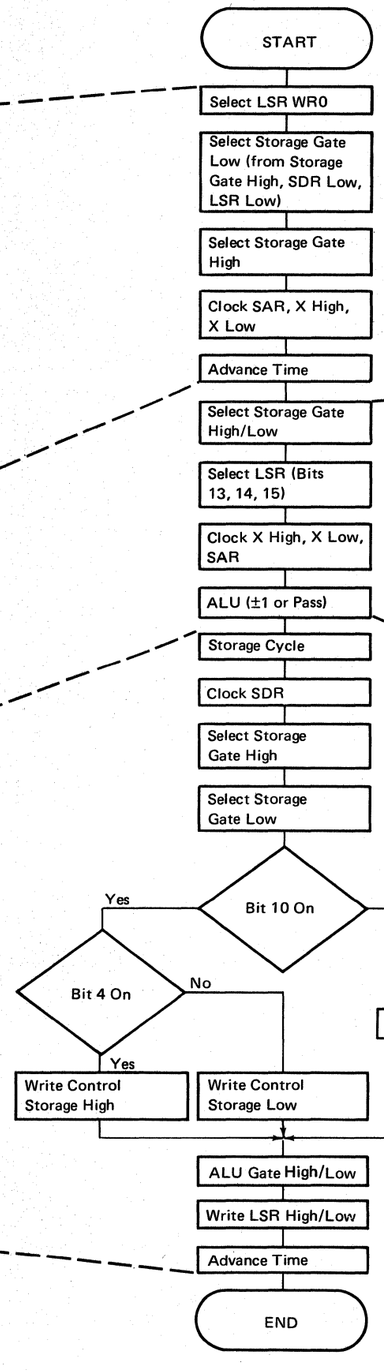
Timing of CPU Functions

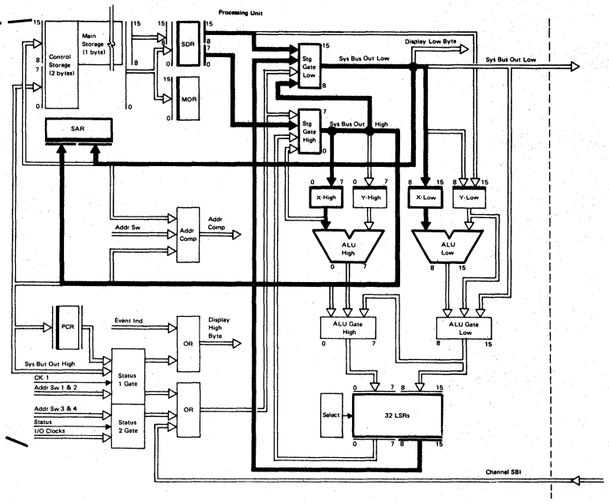


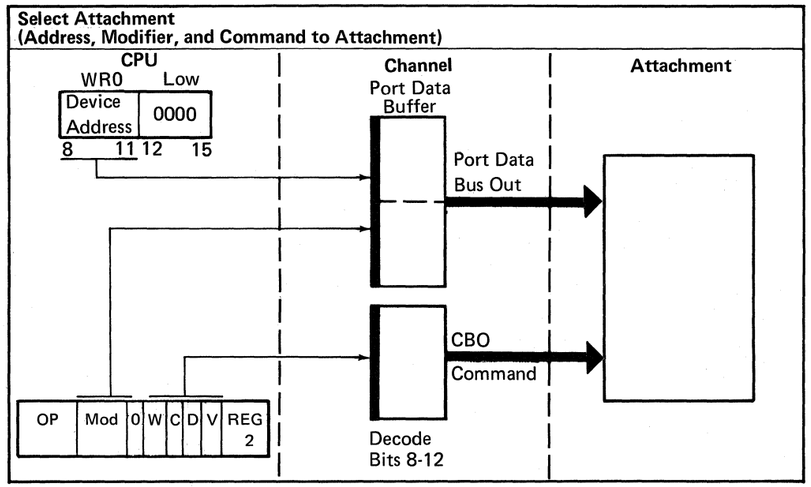
Specific CPU Data Path

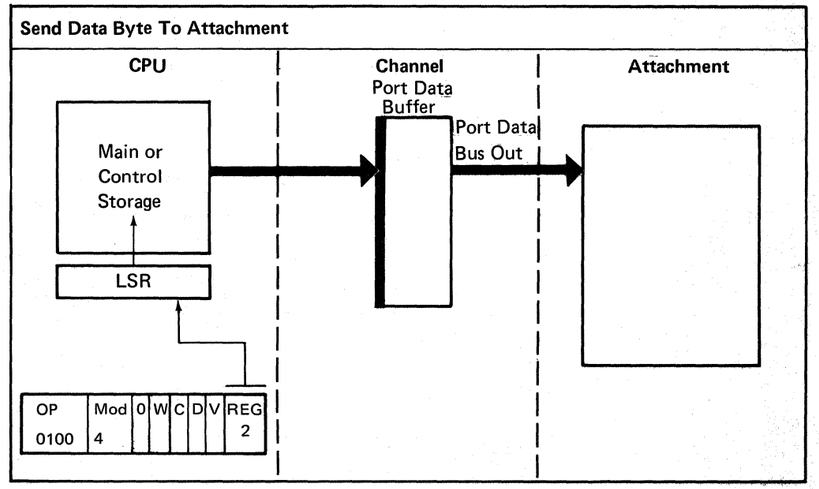


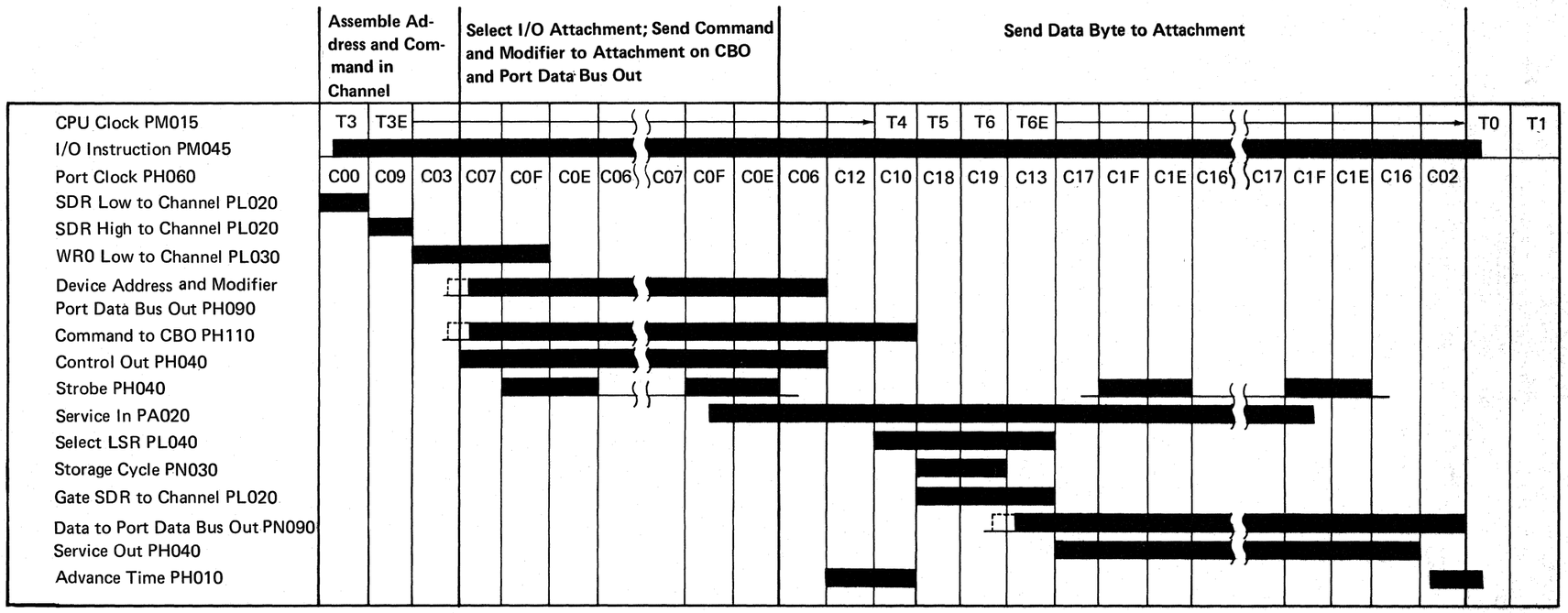
Sequence of CPU Functions



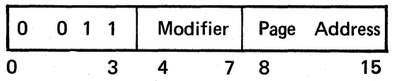



Select Attachment
(Address, Modifier, and Command to Attachment)
CPU
WR0 Low
Device Address
0000
8 11 12 15
Channel
Port Data Buffer
Attachment
Port Data Bus Out
CBO Command
OP Mod 0 W C D V REG 2
Decode Bits 8-12


Send Data Byte To Attachment
CPU
Channel
Port Data Buffer
Attachment
Main or Control Storage
LSR
Port Data Bus Out
OP 0100 Mod 4 0 W C D V REG 2


Assemble Address and Command in Channel
Select I/O Attachment; Send Command and Modifier to Attachment on CBO and Port Data Bus Out
Send Data Byte to Attachment
CPU Clock PM015
I/O Instruction PM045
Port Clock PH060
SDR Low to Channel PL020
SDR High to Channel PL020
WR0 Low to Channel PL030
Device Address and Modifier Port Data Bus Out PH090
Command to CBO PH110
Control Out PH040
Strobe PH040
Service In PA020
Select LSR PL040
Storage Cycle PN030
Gate SDR to Channel PL020
Data to Port Data Bus Out PN090
Service Out PH040
Advance Time PH010
T3 T3E T4 T5 T6 T6E T0 T1
C00 C09 C03 C07 C0F C0E C06 C07 C0F C0E C06 C12 C10 C18 C19 C13 C17 C1F C1E C16 C17 C1F C1E C16 C02

I/O Branch On Condition (JIO)



Mnemonic: JIO

This instruction tests I/O conditions. If the condition tested is active, this instruction will cause a branch. If not, the next sequential instruction is executed.

This op code (bits 0-3) is sent to the port where the bits are decoded as a jump I/O command. This command is then sent to the attachment on the CBO.

Modifier (Bits 4-7): 4-bit control field for I/O devices. This field's usage is device dependent. The modifier field is transferred to the attachment through the port.

Some of the modifier combinations are predefined to provide a common code for those conditions which are used by most I/O devices. The modifier usage (when applicable to a device) is defined as follows:

Modifier Field Setting 4 5 6 7	Description
0 0 0 0	Adapter check
0 0 0 1	Adapter not ready
0 0 1 0	Busy condition 1
0 0 1 1	Busy condition 2
0 1 0 0	Interrupt enabled
0 1 0 1	Diagnostic true
0 1 1 0	Diagnostic false
0 1 1 1 through 1 1 1 1	Available for device requirements

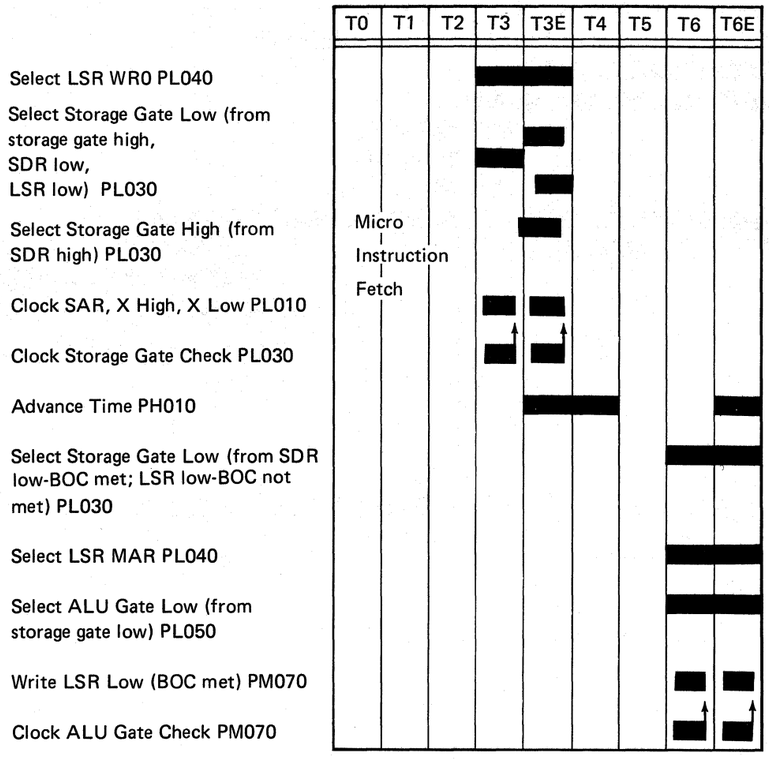
Note: For further descriptions, see sections DISK-15, PTR-20, S-PTR-18, DISP-24, KBD-16, and 33FD-38.

Page Address (Bits 8-15): 8-bit field to allow branching to one of 256 address only in control storage. The page address must be located on the same page boundaries as the I/O branch on condition. This field replaces the lower 8 bits of MAR if the I/O device indicates that the branch condition is met. Port line 'CBI bit 4' is used to determine if the I/O condition is met.

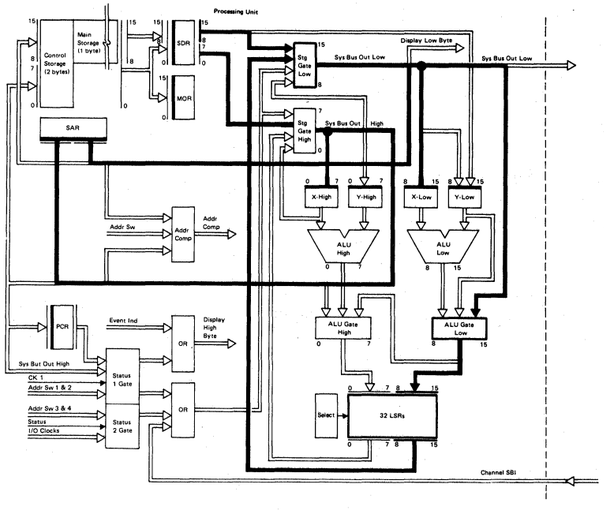
Condition Code

No change.

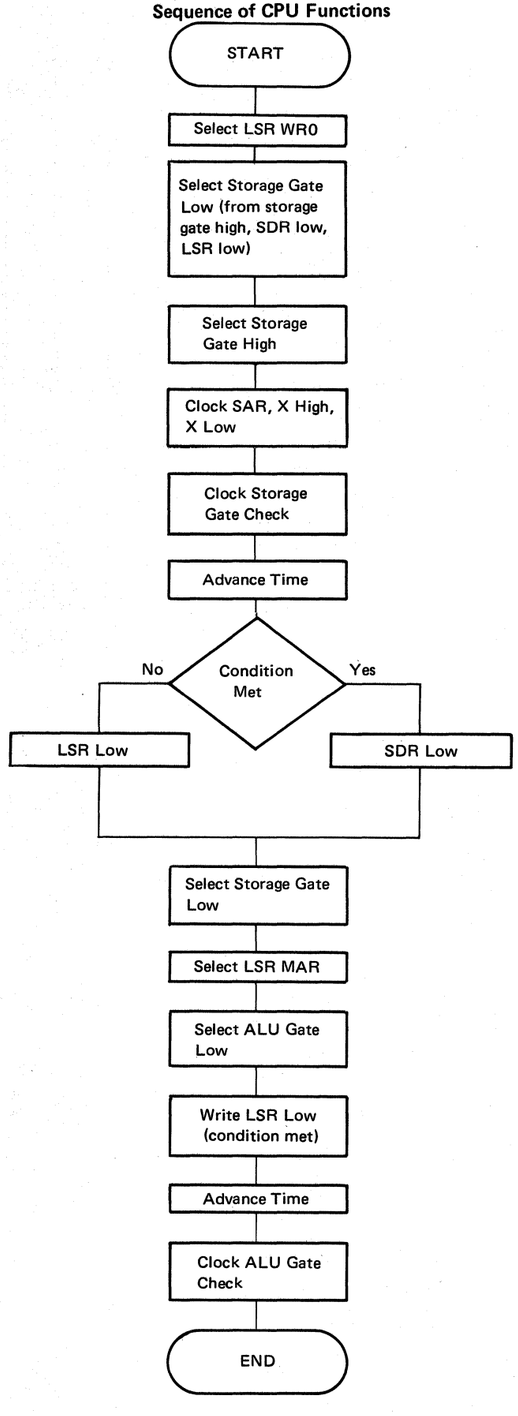
Timing of CPU Functions

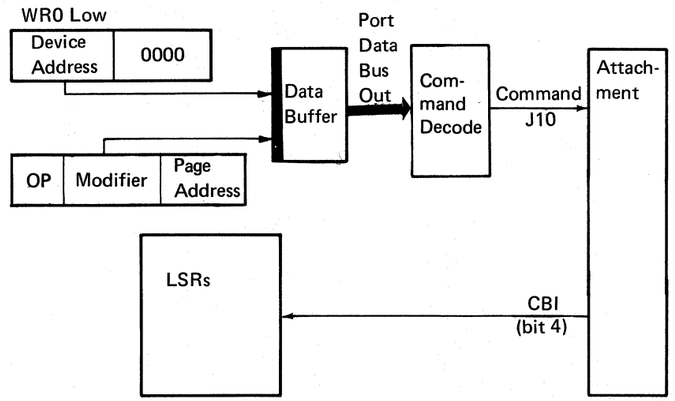


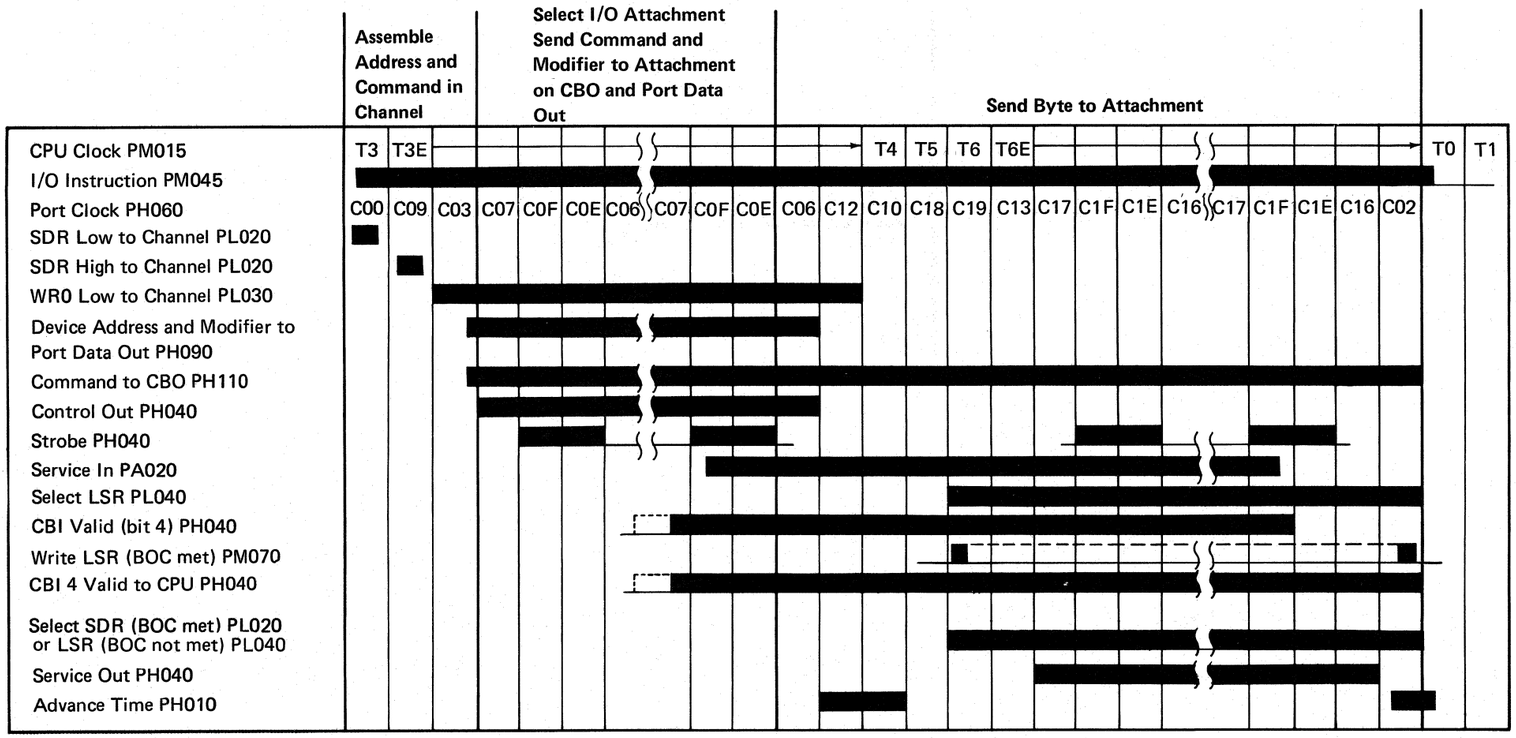
Specific CPU Data Path



Sequence of CPU Functions




WR0 Low
Device Address
0000
OP
Modifier
Page Address
Data Buffer
Port Data Bus Out
Com-mand Decode
Command J10
Attach-ment
LSRs
CBI (bit 4)


Assemble Address and Command in Channel
Select I/O Attachment Send Command and Modifier to Attachment on CBO and Port Data Out
Send Byte to Attachment
CPU Clock PM015
I/O Instruction PM045
Port Clock PH060
SDR Low to Channel PL020
SDR High to Channel PL020
WR0 Low to Channel PL030
Device Address and Modifier to Port Data Out PH090
Command to CBO PH110
Control Out PH040
Strobe PH040
Service In PA020
Select LSR PL040
CBI Valid (bit 4) PH040
Write LSR (BOC met) PM070
CBI 4 Valid to CPU PH040
Select SDR (BOC met) PL020 or LSR (BOC not met) PL040
Service Out PH040
Advance Time PH010
T3 T3E T4 T5 T6 T6E T0 T1
C00 C09 C03 C07 C0F C0E C06 C07 C0F C0E C06 C12 C10 C18 C19 C13 C17 C1F C1E C16 C17 C1F C1E C16 C02

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IMPL

IMPL (initial microprogram load) covers loads, displays, and testing that occur when the operator or CE presses LOAD. Loading is normally done from the disk; the 33FD CE diskette is available as a diagnostic device for the CE if the disk drive is not working.

The tests run during the IMPL sequence check that the circuitry of the system is functioning properly. These tests are automatically performed and, as long as no failures are detected, are unseen by the operator. If, however, the tests detect failures, then one or more of the following occurs:

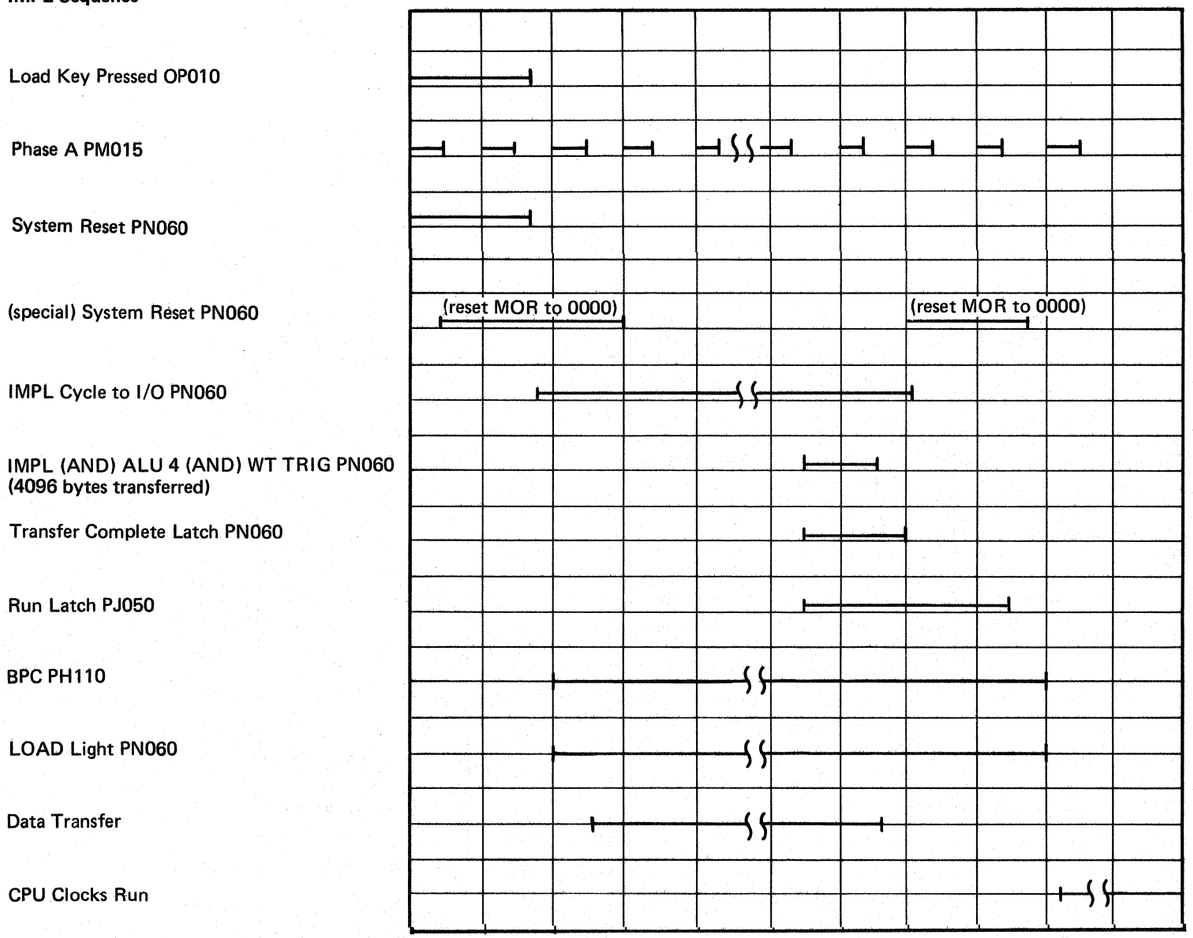
- The processor check lights come on,
- One or more event indicators will be on, or
- An error message appears on the display screen.

No mechanical portions of the I/O devices are tested with the exception of the fixed disk and the printer. To completely check the I/O devices, run the system tests which test the mechanical portions, the emulator, the SCP, and the I/O routines.

IMPL Sequence (PN060)

Pressing and releasing the LOAD key starts the IMPL cycle and causes the LOAD indicator to come on. IMPL cycle along with 'ALU bit 4' and 'write trigger' causes 'transfer complete' to be activated.

IMPL Sequence



If BPC is not deactivated or a processor check occurs; the LOAD light stays on.

Event Indicator Sequence

The LOAD light and all 9 event indicator lights (high byte display on CE panel) are turned on when LOAD is pressed. When LOAD is released, the IMPL sequence starts and 2K words are transferred into control storage (from either 33FD or disk drive). At the same time, the LOAD light and all the event indicators turn off (these lights may flash intermittently). If IMPL is not completed successfully, the lights that represent the incomplete portion of IMPL turn back on and stay on. The MODE SELECTOR switch must be in the PROC RUN position for the event indicators to be displayed.

Each event indicator is turned off and stays off as follows:

[1] P	Adapter received the load signal and initiated action in response (BPC).
[1] 0	First cycle steal request received, data transfer has started (write trigger).
[1] 1	Transfer of 4096 bytes of data was completed (ALU bit 4 AND write trigger).
[1] LOAD	Data transfer completed with no data check (ALU bit 4 AND write trigger AND (not) processor check).
2	Branching and conditional branching routines complete. LSRs are cleared of bad parity. Reset occurs during routine 2.
3	Load 1 complete. The loader is invoked to load the second 2K words of test.
4	First micro instruction of load 2. This indicated that load 2 transferred correctly. Reset occurs during routine 36.
5	First instruction of the control storage test (routine 64). Indicates all previous routines (36-63) ran correctly.
6	Last instruction of control storage test (routine 64). Indicates the control storage test ran correctly.
7	First instruction of IMPL load 3 (wrap test load). Indicates that load 1 and load 2 ran correctly and that the third load has started execution.

[1] Reset by hardware controls. The other lights are reset by micro instructions.

Disk IMPL Operation

When LOAD is pressed, the IMPL sequence does three partial control store loads and then loads the system emulator and SCP portion from cyliner 0, track 1, sectors 1-26 which then takes control at location 0A00 of control storage.

The initial 2K words are loaded by hardware into control store location 0000-07FF. These words contain the following:

Direct area (UDT data, addresses)	128 words
CPU instruction test	1664 words
33FD/62GV loader	256 words

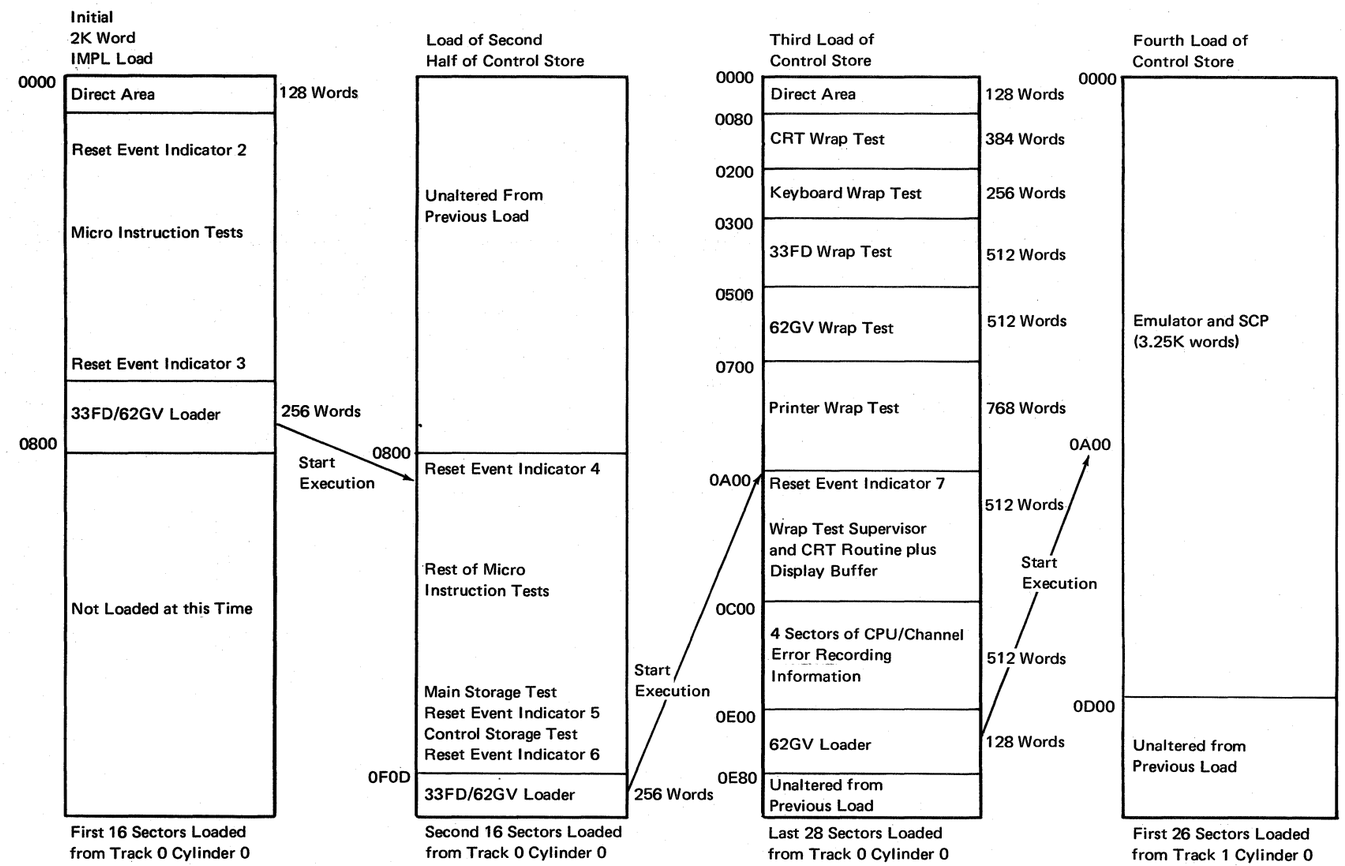
The second 2K words are loaded by the 62GV loader into locations 0800-0FFF. These words contain the following:

Rest of CPU instruction test	1280 words
Main storage test	256 words
Control storage test	256 words
33FD/62GV loader	256 words

The third 3.5K words are loaded by the 62GV loader into location 0080-0E7F. These words contain the following:

CRT wrap test	384 words
Keyboard wrap test	256 words
33FD wrap test	512 words
62GV wrap test	512 words
Printer wrap test	768 words
Wrap test supervisor and CRT display routine	512 words
Four sectors of CPU and port error recording data	512 words
62GV loader (loads emulator and SCP into control storage)	128 words

Disk IMPL Diagnostic Sequence



33FD CE Diskette IMPL Operation

The 33FD CE diskette IMPL consists of three (or optionally up to seven) partial control storage loads before the diagnostic control program is loaded from 33FD tracks 8 and 9 into control storage and given control at control storage location 0000.

The initial 2K words (track 0, special sector of 4096 bytes) are loaded by hardware into control storage locations 0000-07FF. These words contain the following:

Direct area (UDT data, addresses)	128 words
CPU instruction tests	1664 words
33FD/62GV loader	256 words

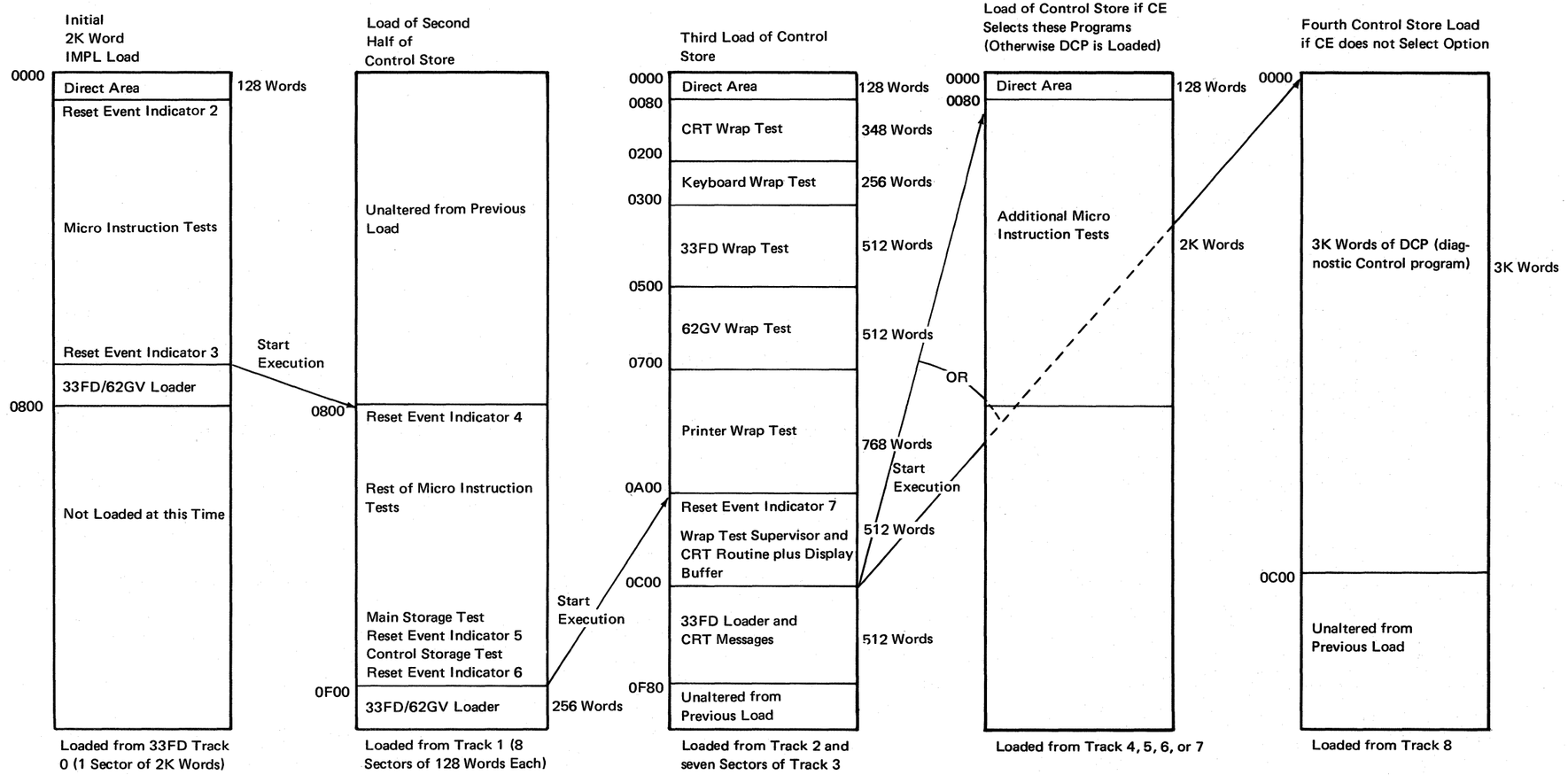
The second 2K words (track 1, 8 sectors) are loaded by the 33FD loader. They are loaded into control storage locations 0800-0FFF. These words contain the following:

Rest of CPU instruction tests	1280 words
Main storage test	256 words
Control storage test	256 words
33FD/62GV loader	256 words

The third 3.75K words (track 2 and seven sectors of track 3) are loaded by the 33FD loader. These words are loaded into control storage location 0080-0F7F. These words contain the following:

CRT wrap test	384 words
Keyboard wrap test	256 words
33FD wrap test	512 words
62GV wrap test	512 words
Printer wrap test	768 words
Wrap test supervisor and CRT display routine and the 33FD loader which loads either 3K words of diagnostic control program or optional micro code tests from track 4, 5, 6, or 7 depending on the result of the CE option select routine.	Rest of control storage

33FD IMPL Diagnostic Sequence



33FD IMPL Timing

The following charts show the sequence of events on a 33FD IMPL operation.

Ground A2, K2, S12 (DK510). Grounding this pin prevents the reset of 'seek counter' and can be used anytime to hold the head on one track.

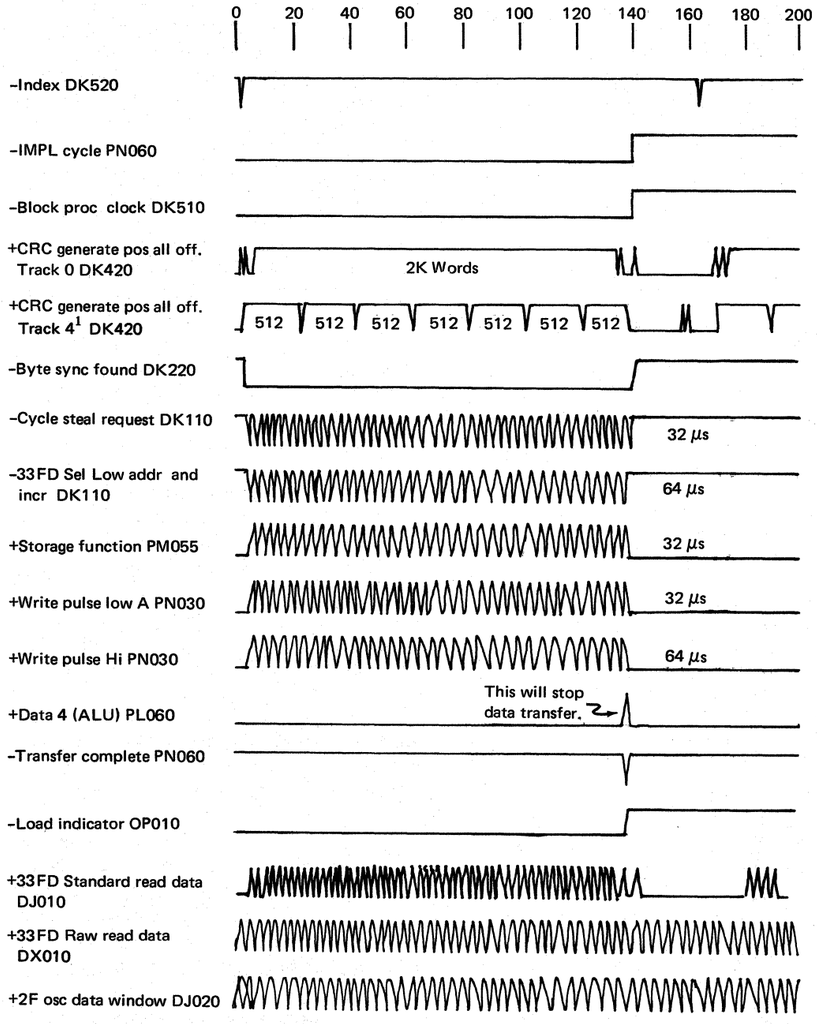
Turn the MODE SELECTOR switch to INSN STEP.

Set STORE SEL to CTL and ADDR COMP to STOP.

Set ADDRESS/DATA switches to 0000.

Sync scope (-) A2K2 P02 20 ms/div.

Continue to press LOAD.



[1] Manually crank head to track 4.

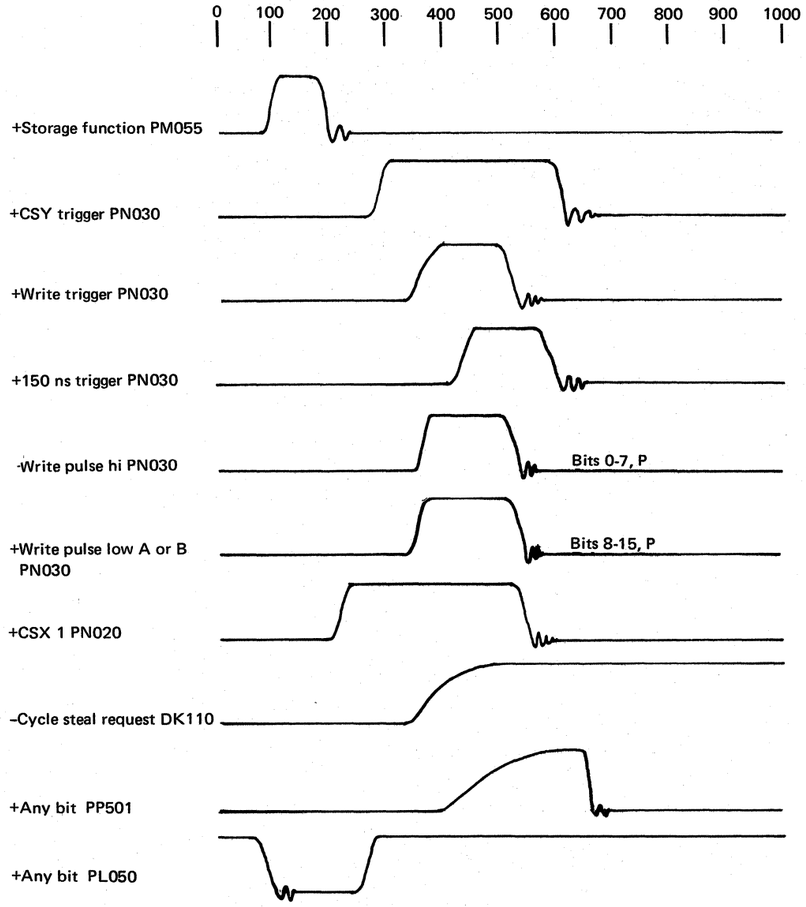
Storage Cycle Function for 33FD IMPL

Jumper A1L2 S07 to ground (+ carry in) which causes all data to be loaded into control storage location 0000.

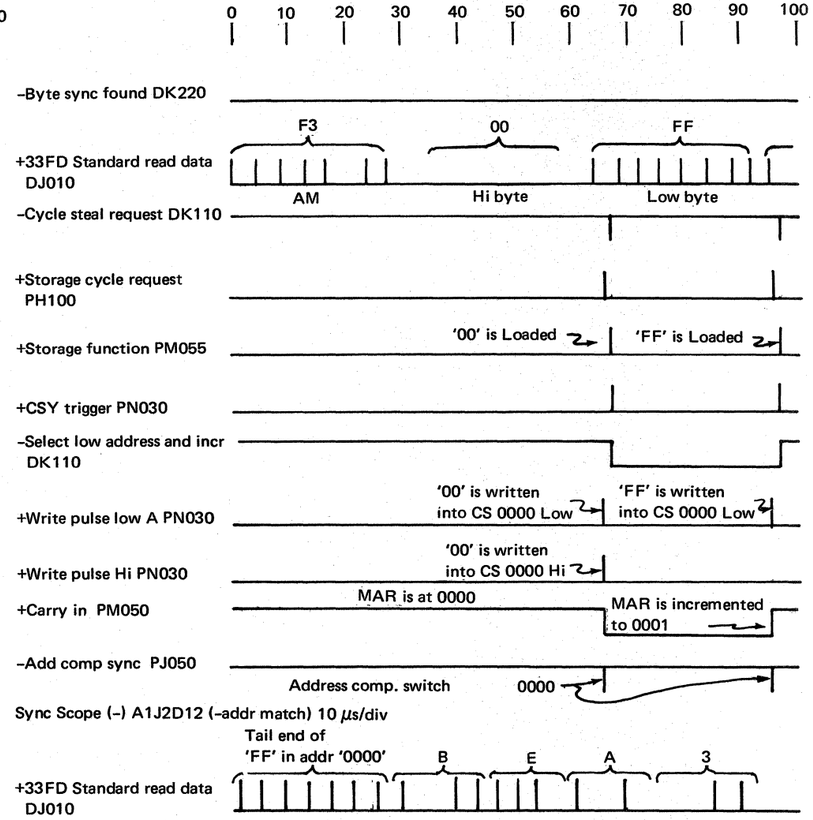
Jumper A2K2 S12 to ground, DK510.

Set IMPL switch to DISKETTE.

Sync scope (+) A1N2 J05 + storage function 100 ns/div, 2 V/div.

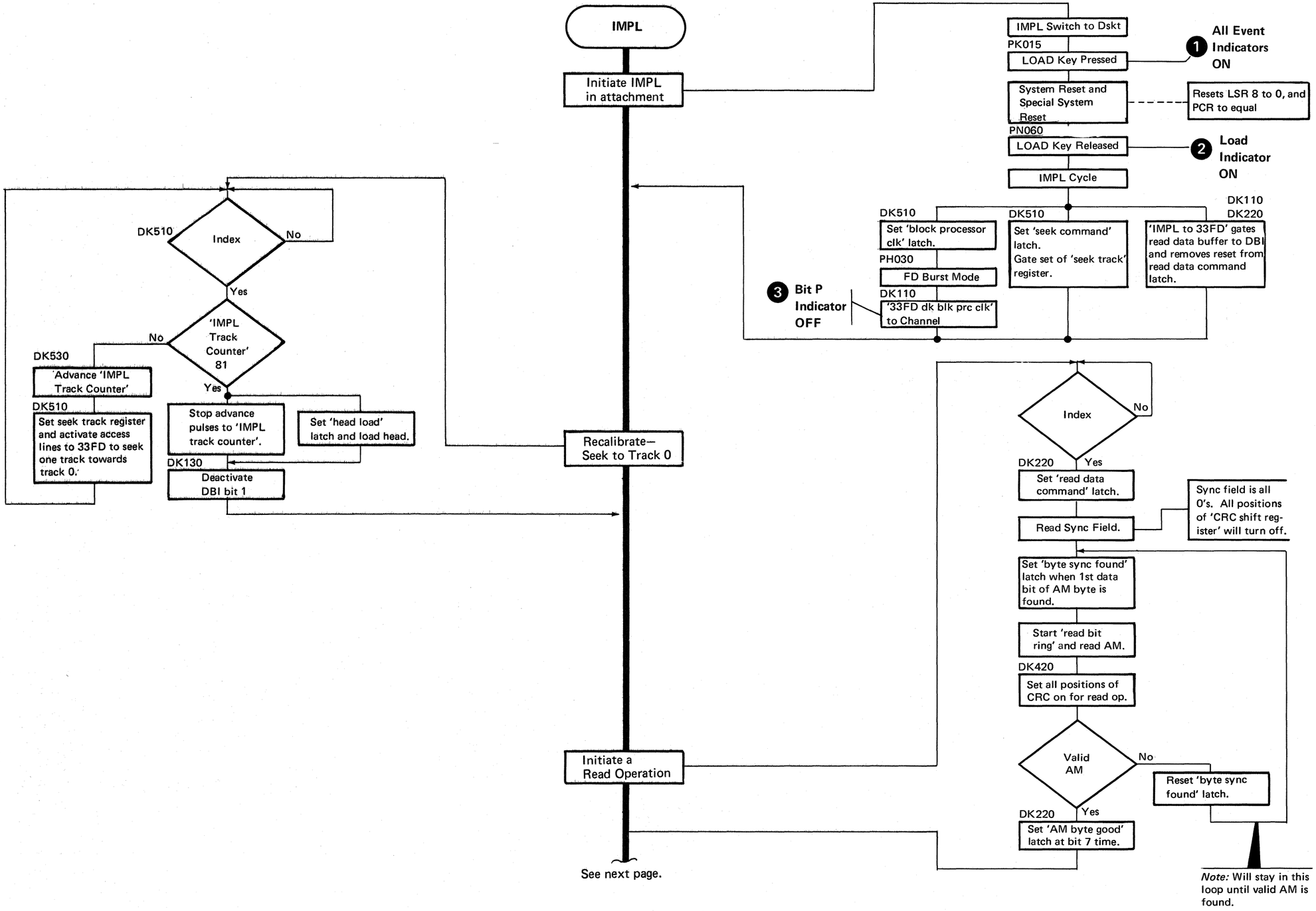


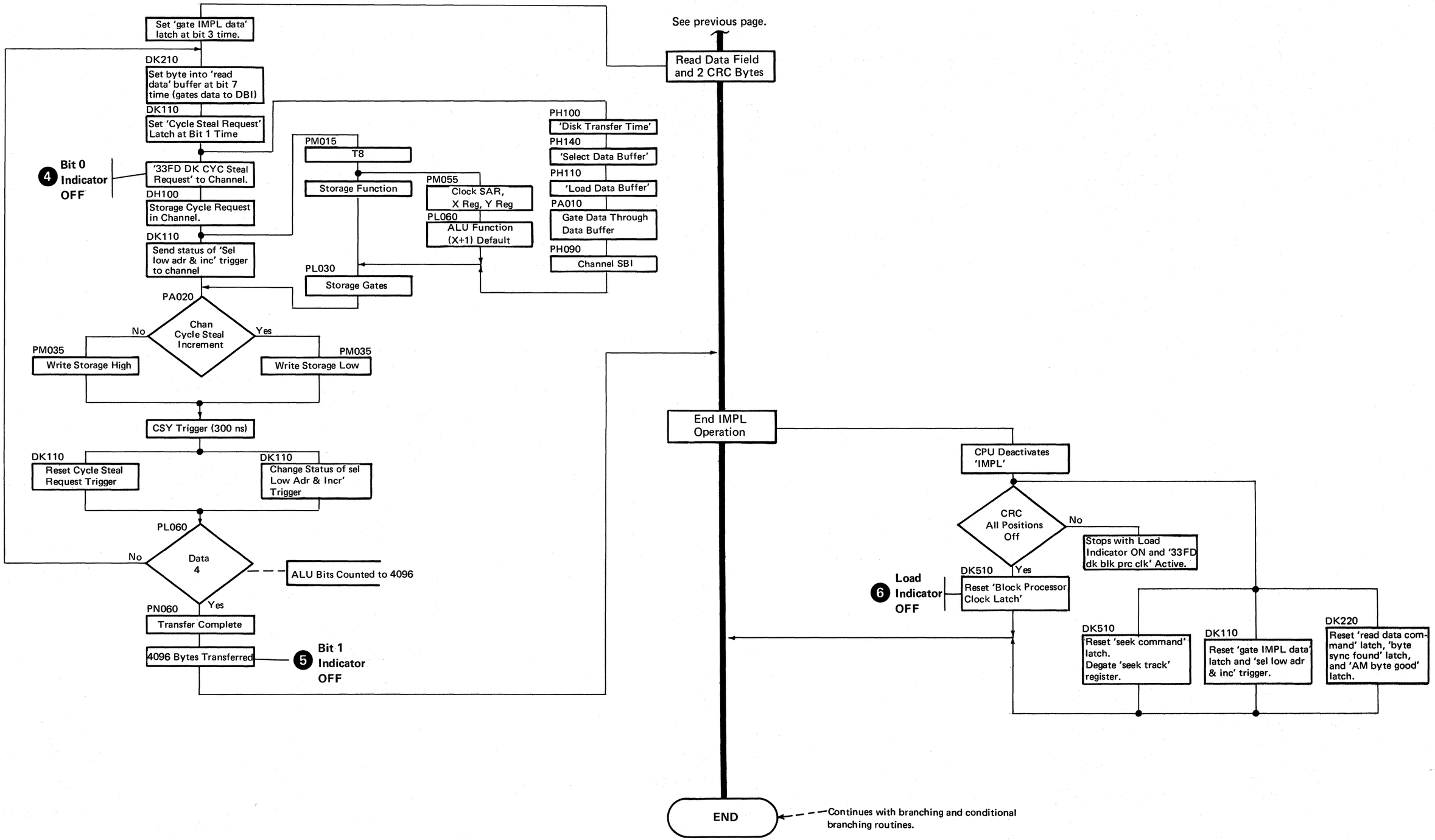
Sync scope (-) A2K2 U02 10 µs/div DK220



Sync Scope (-) A1J2D12 (-addr match) 10 µs/div

33FD IMPL Flowchart




See previous page.
Read Data Field and 2 CRC Bytes
Set 'gate IMPL data' latch at bit 3 time.
DK210
Set byte into 'read data' buffer at bit 7 time (gates data to DBI)
DK110
Set 'Cycle Steal Request' Latch at Bit 1 Time
4 Bit 0 Indicator OFF
'33FD DK CYC Steal Request' to Channel.
DH100
Storage Cycle Request in Channel.
DK110
Send status of 'Sel low adr & inc' trigger to channel
PM015
T8
Storage Function
PM055
Clock SAR, X Reg, Y Reg
PL060
ALU Function (X+1) Default
PL030
Storage Gates
PH100
'Disk Transfer Time'
PH140
'Select Data Buffer'
PH110
'Load Data Buffer'
PA010
Gate Data Through Data Buffer
PH090
Channel SBI
PA020
Chan Cycle Steal Increment
No
Yes
PM035
Write Storage High
PM035
Write Storage Low
CSY Trigger (300 ns)
DK110
Reset Cycle Steal Request Trigger
DK110
Change Status of sel Low Adr & Incr' Trigger
PL060
Data 4
No
ALU Bits Counted to 4096
PN060
Yes
Transfer Complete
4096 Bytes Transferred
5 Bit 1 Indicator OFF
End IMPL Operation
CPU Deactivates 'IMPL'
CRC All Positions Off
No
Stops with Load Indicator ON and '33FD dk blk prc clk' Active.
DK510
Yes
6 Load Indicator OFF
Reset 'Block Processor Clock Latch'
DK510
Reset 'seek command' latch. Degate 'seek track' register.
DK110
Reset 'gate IMPL data' latch and 'sel low adr & inc' trigger.
DK220
Reset 'read data command' latch, 'byte sync found' latch, and 'AM byte good' latch.
END
Continues with branching and conditional branching routines.

IMPL Error Indications

If after pressing LOAD, the appropriate display does not appear within the designated time and the event indicators do not turn off, suspect a machine failure. First, check the setting of the CE panel switches and check that the diskette is properly inserted in the machine.

Machine errors are of two types:

1. Wrap test errors: The IMPL diagnostic wrap test detected an error in a device adapter. Usually the CRT can still be used to display the error as shown:

```
     1    2    3    4
1    0    0    0    0
XXXX XXXX XXXX XXXX XXXX                1
19 Error                                6
```

   If this display occurs or STOP comes on, the same information is in the machine main level registers WR1-WR6 as well as in control storage locations 0017-001B.

2. Processor check: The IMPL diagnostic tests detected an error and forced a processor check (check halt instruction). WR3(L) contains the failing routine number when the failure occurs in routine 12 or above. Check the event indicators to determine when the failure occurred. Use the IMPL diagnostic listings and the error address to determine what specific function of the machine failed.

Summary of IMPL Diagnostic Options

Address Switch Setting	Function Invoked
F100	Run keyboard diagnostic tests.
F7XX	Same function as option FFXX but no CRT display occurs. The contents of WR1-WR6 indicate if any wrap test errors occurred.
F800	Load 33FD diagnostics when loading from the disk drive.
F90X X=4,5,6,7	Load optional microcode test from track X of the IMPL basic diskette.
FA01	Stop after execution of 2K words.
FA02	Stop after execution of 4K words.
FB01	Loop on first 2K words.
FB02	Loop on first 4K words.
FC01	Loop on first 2K words and bypass errors.
FC02	Loop on first 4K words and bypass errors.
FDXX	Loop on routine XX.
FEXX	Loop on routine XX and bypass errors.
FFXX	Run only selected wrap tests indicated by bits on.

Hex Value	
80	33FD wrap test
40	Not used
20	Not used
10	Not used
08	CRT wrap test
04	Keyboard wrap test
02	Printer wrap test
01	62GV wrap test
00	Bypasses all wrap tests and skips configuration sensitive CPU tests. Use this setting if CE diskette from another system with a different storage configuration is used. Also use this if additional storage is being added to the system and the CE diskette has not yet been reconfigured.

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Error Handling

System error handling detects circuit malfunctions and stops the system when necessary. Machine check interrupt (micro interrupt level 0) logs error information in control storage and retries intermittent errors whenever possible.

For the machine check interrupt routine functions to be successful, at least one of the following must be true:

- Detected error is intermittent,
- Detected error has disappeared when MCI routine uses the affected checking circuitry, or
- Detected error is solid but the circuitry used during MCI routine does not require the bad circuitry.

Machine check interrupt request is generated when an error is detected by the port or CPU hardware.

The affect of these checks on the run latch is shown on CNSL-8.

CPU Checks

CPU checks are stored in the processor check byte (CPU error byte) register which can be sensed by I/O immediate. This instruction loads the contents of the processor check byte register into the specified work register so that the CPU check conditions may be interrogated. These checks can also be displayed in the left byte of the indicator lights on the CE panel by setting the mode switch to DPLY CHKS.

Processor Check Byte

SDR P Chk	MOR P Chk	Stg Gate P Chk	ALU Gate P Chk	CS Invalid Addr/SAR Chk	MS Invalid Addr/SAR Chk	Not Used	Micro Code Check

SDR P Check (Light 0): The data read from storage contains even parity.

MOR P Check (Light 1): The data contained in the micro operation register contains even parity.

Storage Gate P Check (Light 2): Even parity was detected on data:

- Read from SDRs.
- Read from LSRs.
- Coming from system bus in (port, status 1, status 2).

ALU Gate P Check (Light 3):

- Even parity was detected on data written into the LSRs, or
- Predicted parity of an ALU operation did not agree with the result.

Invalid Control Storage Address/SAR Check (Light 4): Address loaded in SAR exceeds the maximum available control storage (control storage is addressed).

Note: Lights 4 and 5, if both on, indicate SAR P check.

Micro Code Check (Light 7): 6-second timer is not reset by micro instruction 'turn on GO latch'. If this timer is not reset within 6 seconds, the system assumes that the microprogram somehow branched into a microloop with no exit.

The system executes the instruction 'turn on GO latch' when entering the I fetch phase of a system instruction or when in a micro stop loop (operator pressed STOP or SYS INSN STEP is active). This action prevents the check from coming on.

Invalid Main Storage Address/SAR Check (Light 5): Address loaded in SAR exceeds the maximum available main storage (main storage is addressed).

Port Checks

The following checks are detected by the port hardware. These checks are stored in the port check byte register and can be loaded into a work register. These checks can also be displayed by the rightmost byte of the indicator lights on the CE panel by setting the mode switch to DPLY CHKS.

Port Check Byte

DBO P Chk	Invalid Device Assgmt	DBI P Chk	Time Out Check	CBI-DBI Not Zero	SYS Bus P Chk	Cycle Steal Op Chk	Invalid Port

DBO P Check (Light 0): An I/O attachment detected a parity error on port data bus out during a transfer of commands or data. The attachment signals this error to the port and the port stores it.

Invalid Device Assignment (Light 1): Port raises 'control out' to address an I/O adapter and the attachment does not activate 'service in' within 5.4 μs. This check can also occur if DBO has bad parity during 'control out' or the addressed device is not installed.

DBI P Check (Light 2): Parity error detected by the port during the transfer of data from the I/O attachment to the CPU (and CBI bit 4 is not on).

Timeout Check (Light 3): Attachment did not deactivate 'service in' within 5.4 μs after the rise of 'service out'.

CBI-DBI Not Zero (Light 4): DBI, CBI, 'service in', and 'multidevice response' are not all deactivated at the end of the port I/O interchange. These lines are not checked during 62GV burst mode.

System Bus P Check (Light 5): Parity error detected on the data sent from the CPU to the port when 'service out is active, or when data is sent to the 62GV during burst mode.

Burst Mode Operation Check (Light 6): Any check was detected in the CPU or port while burst mode was in progress.

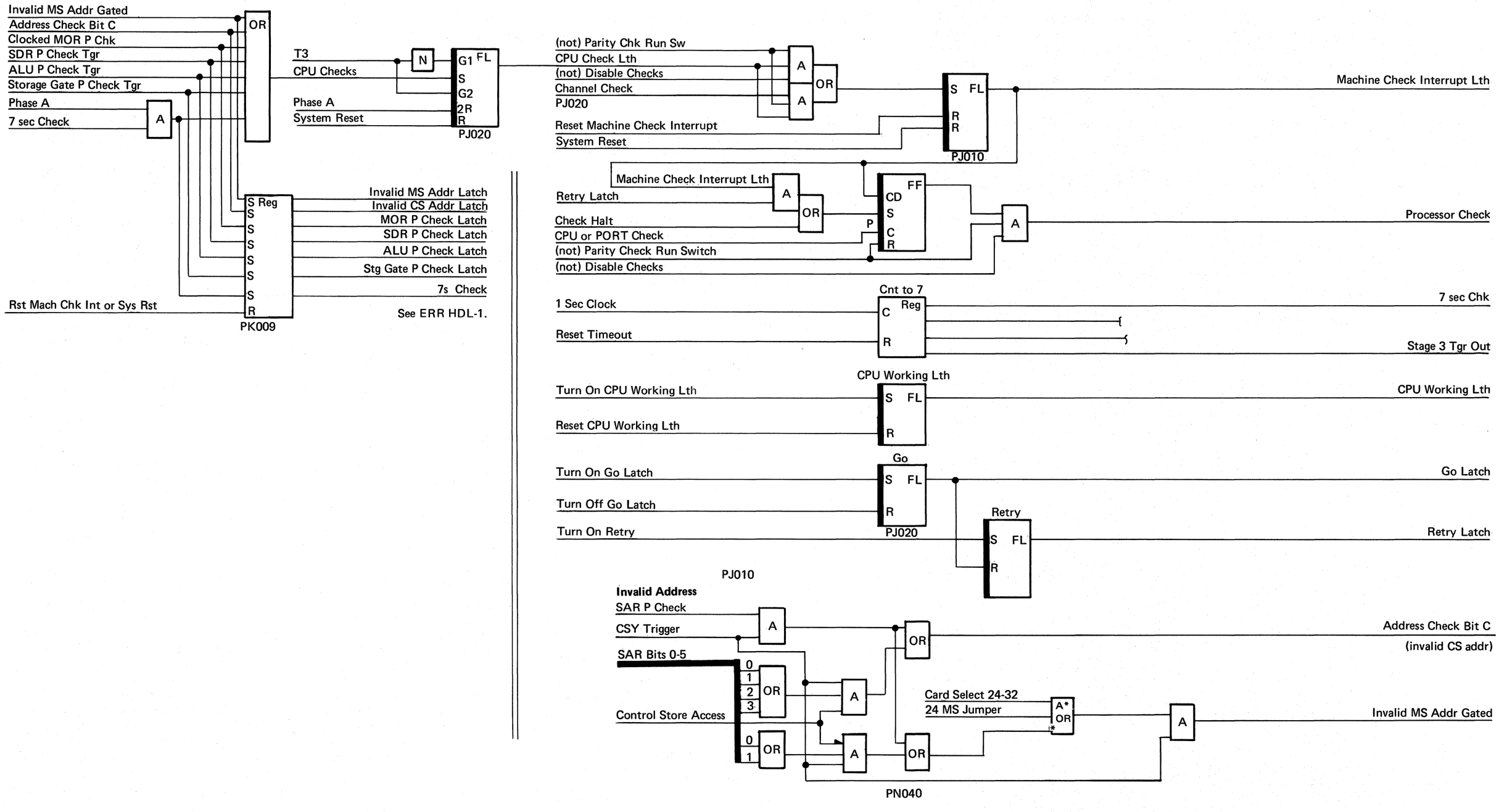
Invalid Port (Light 7): Bits 12-15 of WR0(L) were not 0000.

In addition to these checks, information about the last port operation is stored in the port register. This register contains the device address of the I/O attachment and the command (CBO bits) last executed by the channel. If any checks are present in the port register alteration of the port register is inhibited until the error is reset. See CHAN section in this manual for decode of device address and command bus out.

Port Register

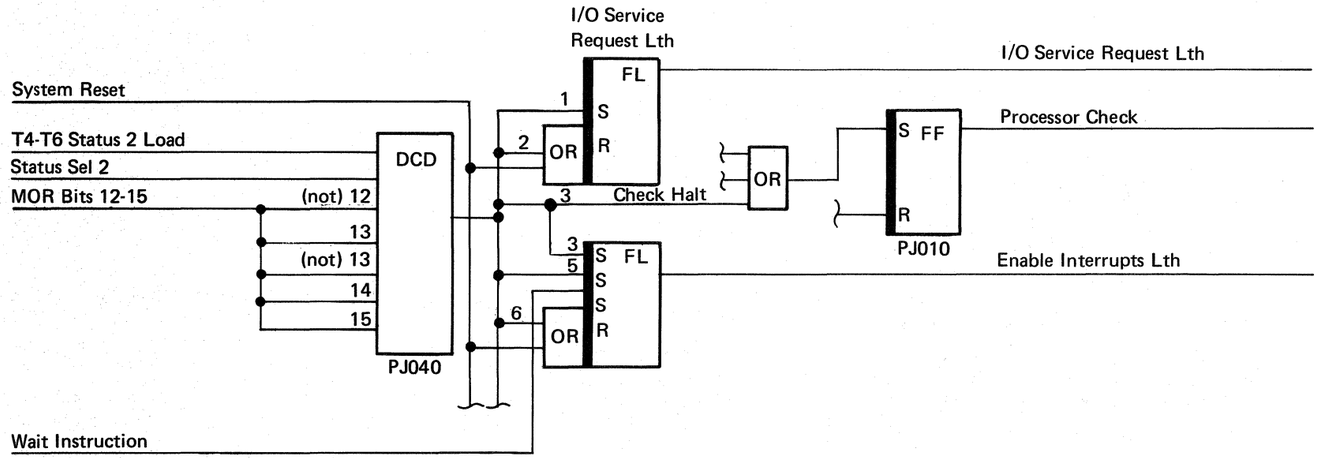
Device Address	Not Used	Command Bus Out
0 3	4 5	7

Check Generation



Check Halt

Check halt is a microprocessor load micro instruction (BEA3) that is used to fill unused areas of storage. If, because of an error, the system branches to one of these unused locations, the check halt will cause the system to stop and the processor check (PROC CHK) light to come on.



Machine Check Interrupt Routine

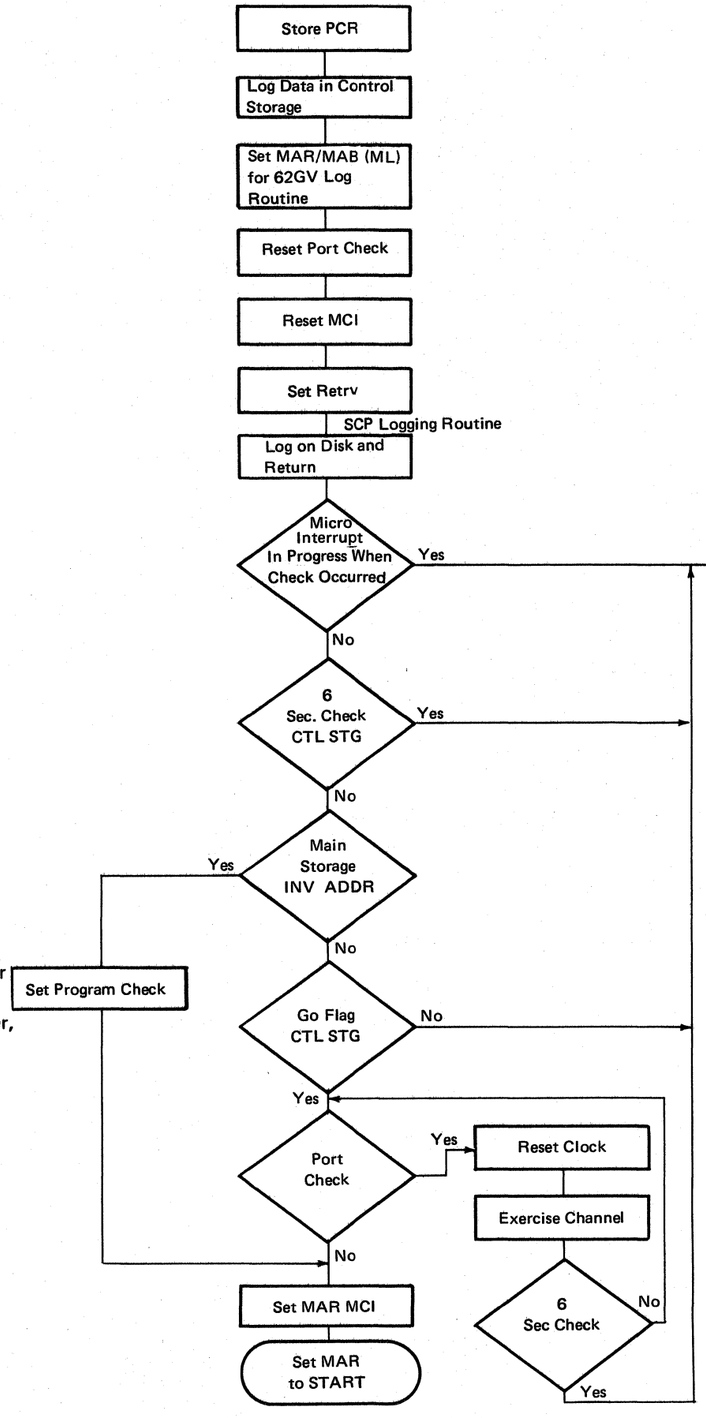
Machine check interrupt request is generated when an error is detected by the port or CPU hardware. Occurrence of MCI brings up 'machine check interrupt' from the CPU to the port which stops all I/O functions. If machine check interrupt routine determines that no retry is possible, MCI issues a check halt instruction which creates a processor check. A processor check (or a manual stop from the CE panel) stops the CPU clock and raises 'T7' to the attachment which causes the attachment to deactivate the critical circuitry.

Error Logging

When a check is detected, MCI routine logs the following information in control storage:

WR0 main level
Interface error byte/interface register
CPU error byte/console status byte
MAR interrupt level 1
MAR interrupt level 2
MAR interrupt level 3
MAB main level
MAR main level
Instruction located at MAR-1
Date

Once this information is saved in control storage, MCI routine branches to SCP which takes this information and logs it on one sector of the disk. Sectors 55-58 on cylinder 0, track 0 are reserved for logging information. Each time error information is written on a sector, machine check counter in the direct area of control storage is incremented by 1. This counter determines which sector is to be used. These four sectors contain information about the last four errors detected. If, however, an error occurs while MCI is running, a processor check occurs and error logging is not completed.



Error Retry

Errors that occur while the processor is executing any of the following are retried.

I fetch of all system instructions.

E phase of the following system instructions:

ZAZ[1]
MVX[1]
L[1]
BC[1]
JC[1]
TBN
TBF
MVI
A[1]
ITC[1]
ED[1]
LA
CLI[1]
CLC

The GO flag is checked by MCI to determine if retry is possible.

Errors which are detected during the following are not retried:

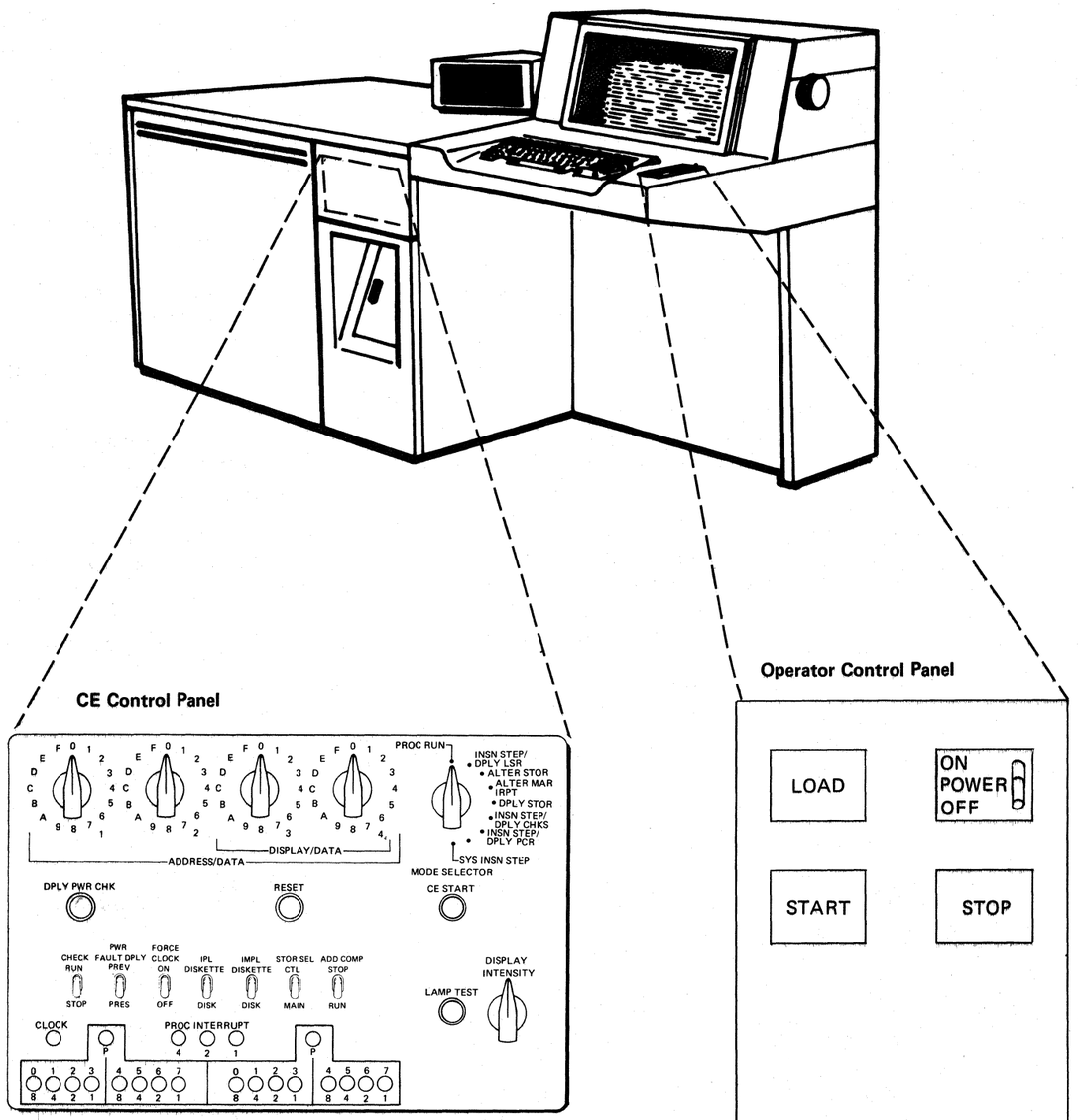
Any micro interrupt is in progress.
The SCP is running.
The system is in the E phase of the following instructions:

SBN
SVC
LIO
TIO
SIO

---

[1] Indicates that error retry will be attempted *only* if the instruction has not gone far enough to alter the data in an operand.

Console



CE Control Panel discussed on next page.

Operator Control Panel

Load Switch/Light (LOAD)

This key is pressed to start the initial program loading; IMPL followed by IPL.

The LOAD light turns on when the switch is pressed and remains on until the first 4096 bytes of the IMPL have been successfully loaded.

Start Switch/Light (START)

This micro instruction controlled switch is turned on at IPL time. It is turned off when one of the following occurs:

1. STOP is pressed.
2. The mode selector switch is in the SYS INSN STEP position.
3. An address compare stop occurs.

When the STOP light is on, the microprogram is looping and interrogating the START switch. When START is pressed, the START light turns on and the STOP light turns off. Processing of the system instruction will then continue.

Keyboard Ready Light (KEYBD RDY)

This light is on whenever the keyboard is enabled and ready to operate.

Processor Check Light (PROC CHK)

This light is turned on whenever an unrecoverable error is detected by the CPU. Whenever this occurs the only way to restart is by initiating an IMPL via the LOAD switch.

Power On/Off Switch (POWER ON/OFF)

This switch initiates a power on or power off sequence. As part of the power on sequence, a system reset is performed to initalize the system. At the completion of the power on sequence (approximately 35 seconds), the STOP light turns on.

The contents of the registers and storage are destroyed during power off.

Stop Switch (STOP)

When this micro instruction controlled switch is pressed, the system is stopped at the end of the current system instruction and the STOP light is turned on. At the end of each system instruction, the stop switch is interrogated by the microprogram and if the switch is active, the microprogram loops in a stopped state.

On power-up, this light turns on when the power-up sequence has been completed. It turns off when LOAD is pressed.

The STOP light is also turned on if the microprogram is loaded and a main storage address compare stop occurs or the mode selector switch is placed in the SYS INSN STEP position.

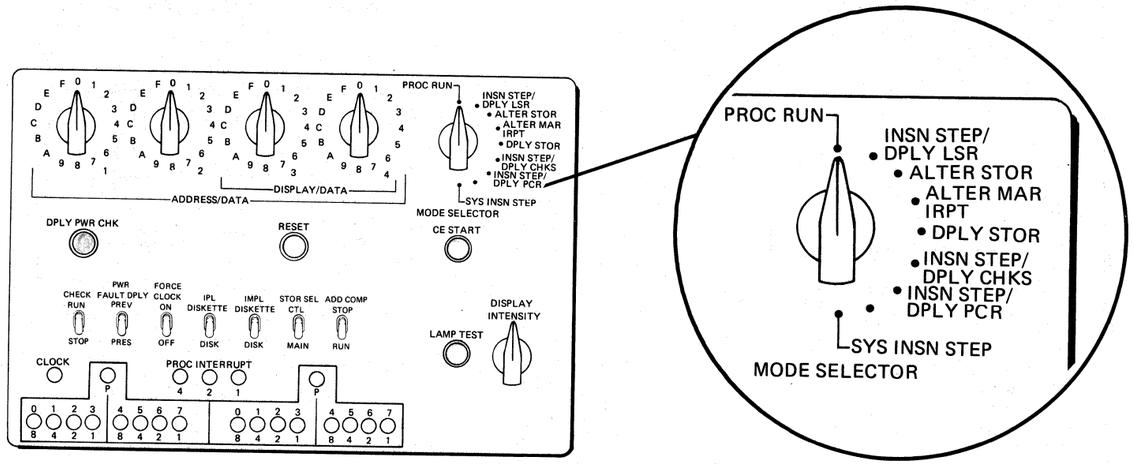
Power Check Light (PWR CHK)

This light indicates that a check in the power system has occurred and that power has been removed. However, voltage necessary to display the check condition is still on.

Thermal Check Light (TH CHK)

This indicator is turned on whenever an over temperature condition is detected in the A gate, power supplies, or printer. Power is removed from the system when the thermal check occurs. After the thermal condition has gone away, system power may again be brought up.

CE Control Panel



MODE SELECTOR Switch

When this switch is moved from the PROC RUN position, the CPU clock stops after execution of the current micro instruction.

To restart the CPU, return the switch to PROC RUN and press CE START. The CPU starts at the micro instruction addressed by MAR.

PROC RUN

This is the normal position of the mode selector switch when the system is running.

INSN STEP/DPLY LSR

With the mode selector switch in this position, each time the CE START switch is pressed, the next sequential micro instruction or branch is executed. In addition, the contents of a selected LSR are displayed. The LSR to be displayed is specified by the display switches 3 and 4. The values hex '00' through '1F' selects LSRs 0 through 31 respectively.

ALTER STOR (PM025)

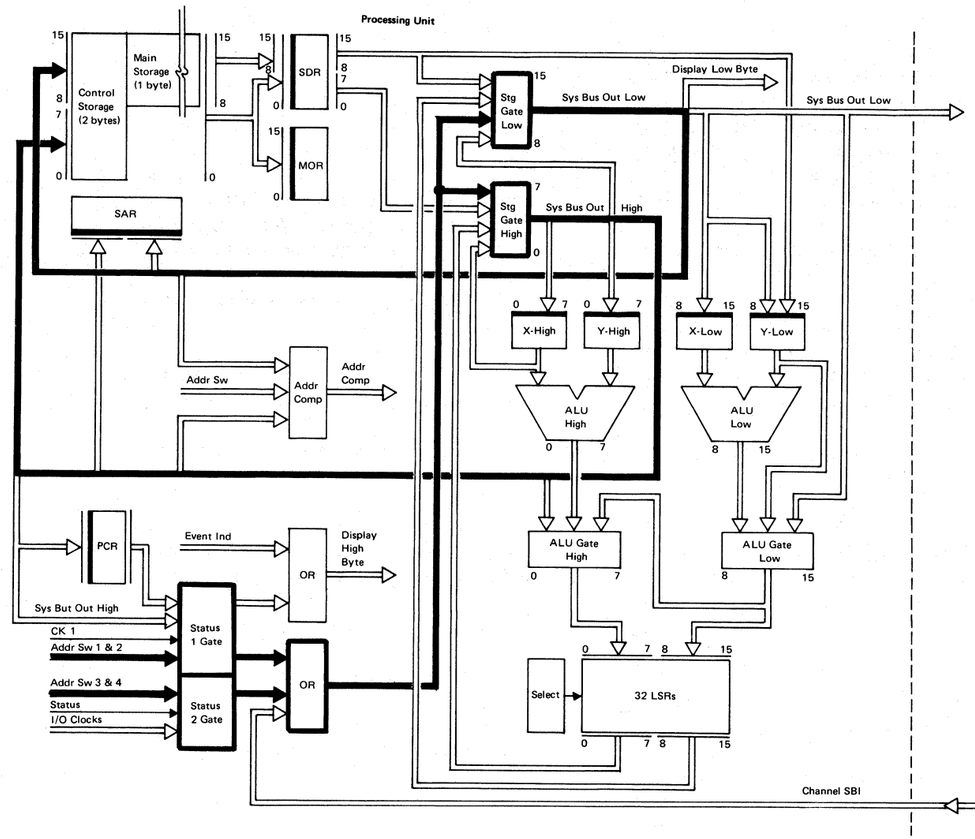
This position is used to alter the contents of main storage or control storage. It is used in conjunction with the STOR SEL switch, MAR, and the data switches.

The STOR SEL switch controls whether main storage or control storage will be accessed. MAR will contain the address of the location to be altered.

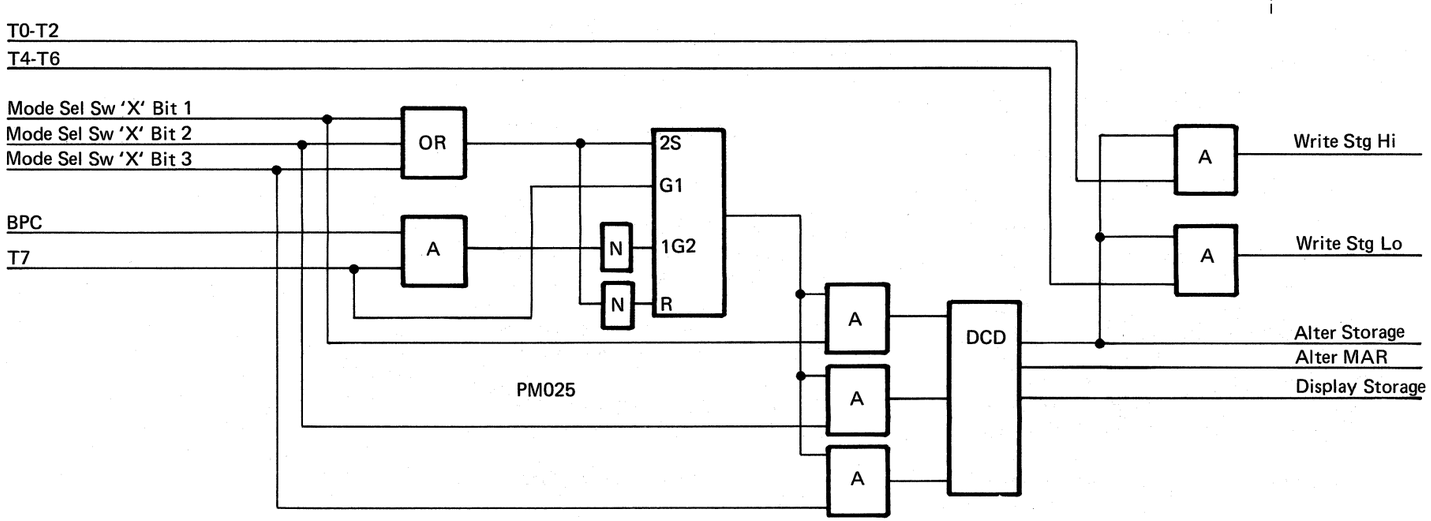
If main storage is being addressed, the contents of data switches 3 and 4 are stored in the addressed location. If control storage is being addressed, the contents of switches 1, 2, 3, and 4 are stored. Data switch settings are displayed in the display lights.

Pressing CE START initiates the alter storage operation and causes a CPU cycle to occur. During this cycle the address in MAR is incremented by one. Thus it is possible to alter several sequential positions of storage without entering a new address in MAR each time.

Specific CPU Data Flow for Alter Storage



Alter Storage Function



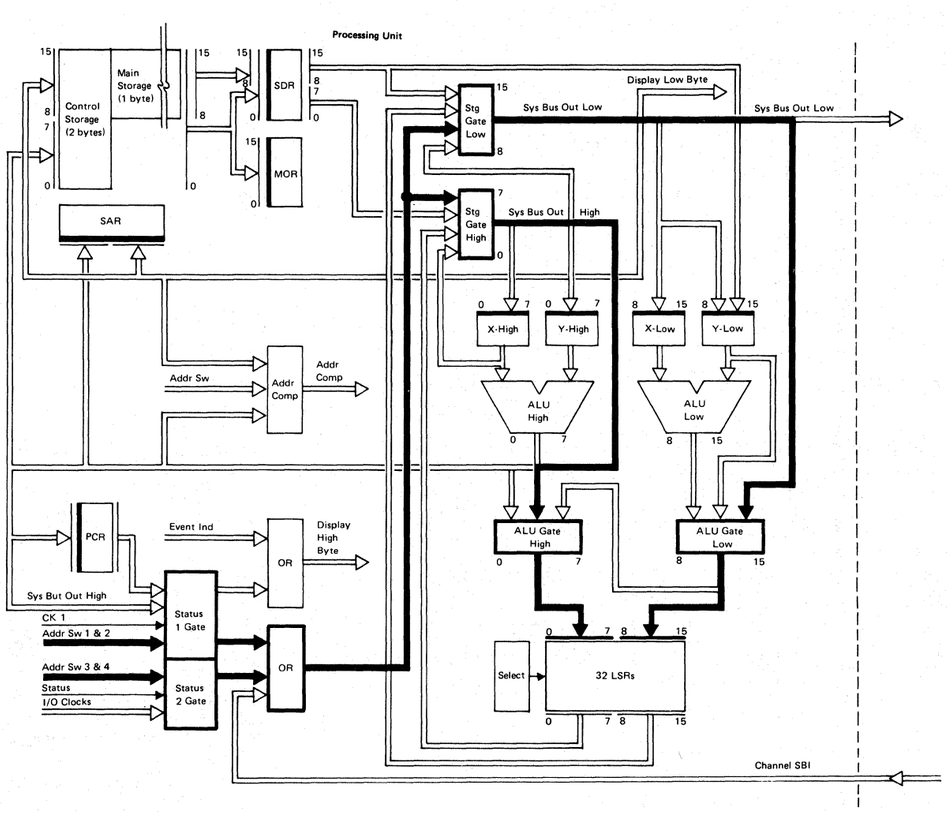
ALTER MAR IRPT

This position of the mode selector switch allows the MAR for the current interrupt level to be altered.

With the switch in this position, the 16 binary bits from the data switches 1, 2, 3, and 4 are entered into the current MAR when CE START is pressed. Data switch settings are displayed in the display lights.

When altering this register for the display or alter function, note the initial contents of the register by displaying the contents and then writing it down. This register must be reinitialized to its original value before restarting in the microprogram.

Specific CPU Data Flow for ALTER MAR IRPT



DPLY STOR

This position is used to display the contents of SDR, or the contents of main storage or control storage. When displaying main storage or control storage, the switch is used in conjunction with the STOR SEL switch and MAR.

Turning the mode selector switch to this position displays the current contents of SDR.

To display the contents of a position of main storage or control storage:

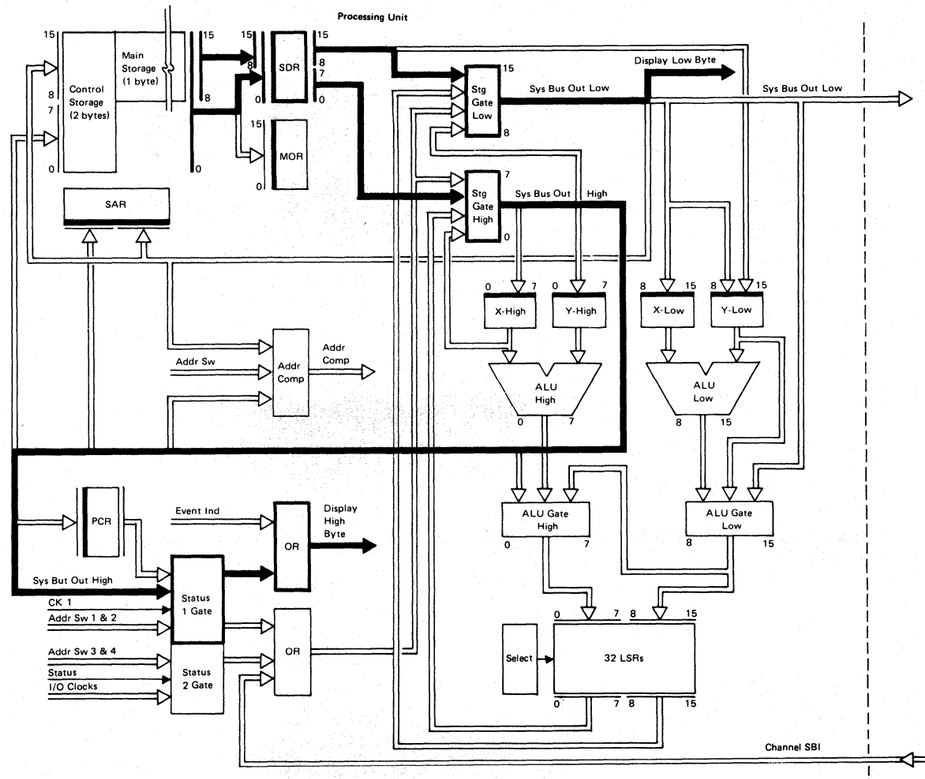
1. Set the data switches to the address to be displayed.
2. Press ALTER MAR.
3. Press CE START. This puts the address in WR0.
4. Select main storage or control storage with the STOR SEL switch.
5. Turn the mode selector switch to DPLY STOR, then press CE START to initiate the operation.

During the storage cycle, which is initiated by pressing CE START, the contents of storage are set into the SDR and displayed in the lights. MAR is incremented by one. Thus, sequential bytes can be displayed without setting a new address into MAR each time.

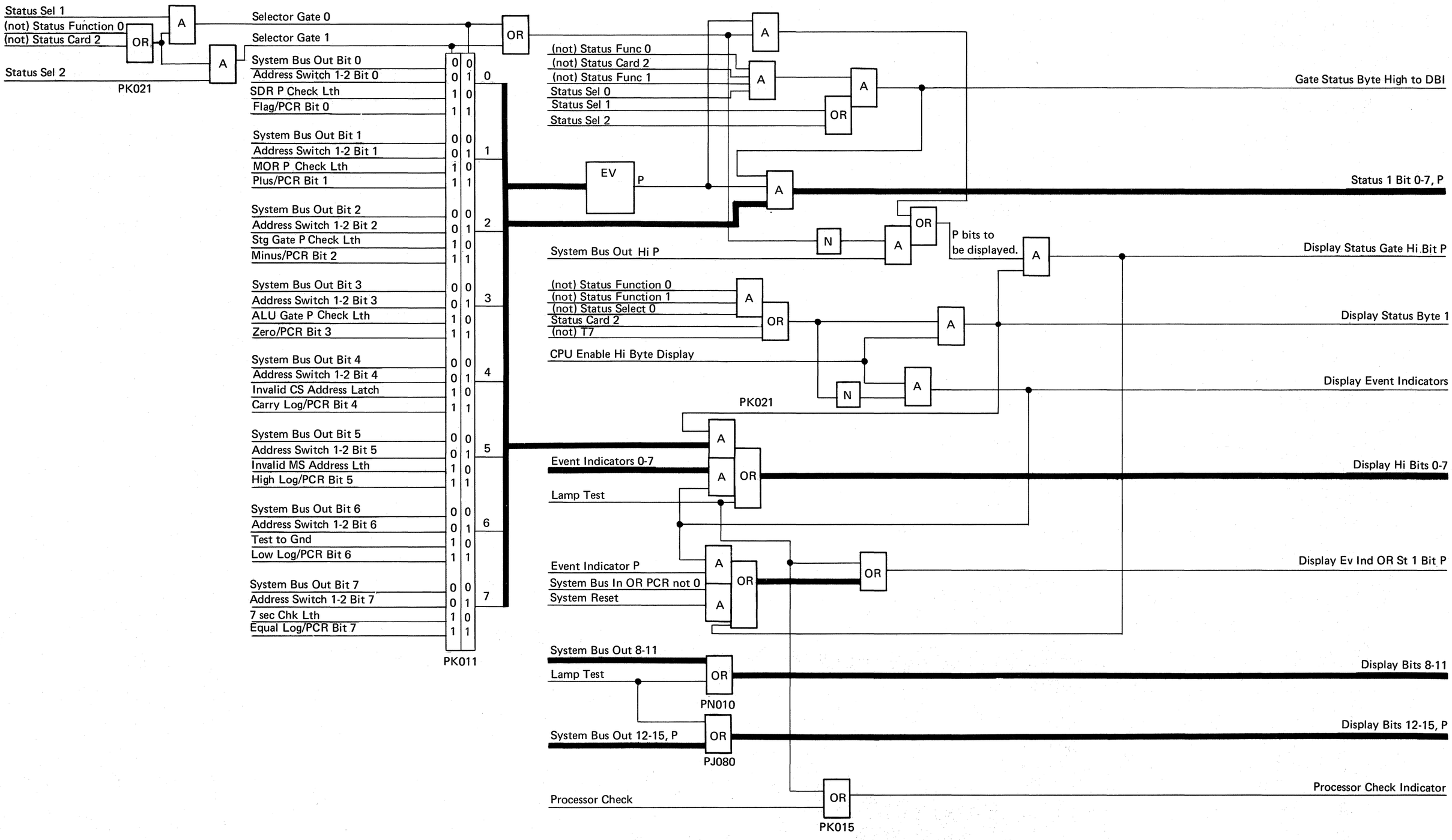
When control storage is displayed, all 18 bits appear in the lights. When main storage is displayed, the 9 bits are displayed in the rightmost byte of the display lights. The leftmost byte is not significant (contains all bits on).

See CNSL-4 for circuit details.

Specific CPU Data Flow for Display Storage



Display Circuits



INSN STEP/DPLY CHKS

Various CPU and port errors that occur can be displayed via the CE panel lights. These errors are recorded in the CPU error byte and the port check byte. Set the mode selector switch to the DPLY CHKS position to display these 2 bytes. Each time CE START is pressed, the next sequential micro instruction or branch is executed.

CPU ERROR BYTE (Left Byte)

Bit	Error	Cause
0	SDR parity check	Parity is incorrect in the storage data register.
1	MOR parity check	Parity is incorrect in the micro operation register.
2	Storage gate parity check	Parity is incorrect at the output of the storage gate in the data flow.
3	ALU gate parity check	Parity predicted does not agree with the generated parity at the ALU gate.
4	Invalid control storage address/SAR	Indicates that control storage was being addressed outside its boundaries.
5	Invalid main storage address/SAR	Indicates that main storage was being addressed outside its boundaries.
4 and 5	SAR P check	Parity is incorrect in the storage address register.
6	Not used	
7	Microcode check	Indicates that the microprocessor has been in a loop for 6 seconds.

PORT CHECK BYTE (Right Byte)

Bit	Error	Cause
0	DBO parity check	Incorrect parity has been detected by an I/O attachment on the 'data bus out'.
1	Invalid device assignment	Indicates that the port has put an address on the DBO but no response has been received from an attachment within the required time. (Port has raised 'control out' to address an attachment and the attachment has not responded by activating 'service in' within 5.4 μs.) This check can also occur if the DBO has incorrect parity during the transmission of an address.
2	DBI parity check	Incorrect parity has been detected by the port during the transfer of data from an I/O attachment.
3	Timeout check	The port has detected an error in the normal port sequence. (This check occurs if an attachment does not deactivate 'service in' within 5.4 μs after the rise of 'service out'.)
4	CBI/DBI not zero	The I/O interface lines were not cleared at the specified time. The I/O is required to clear CBI and DBI prior to deactivating 'service out' during T6 after transferring a byte of data to or from an I/O device.
5	System bus parity check	Incorrect parity has been detected on the data sent from the CPU to the port. The check is made while 'service out' is active; or incorrect parity has been detected on data being sent to the disk attachment during a burst mode operation.
6	Cycle steal or burst mode operation check	If any of the CPU or port errors listed under DPLY CHKS occurs during a cycle steal operation, this bit will be turned on. In addition, if any CPU or channel parity error is detected during a burst mode operation, this bit will be turned on.
7	Invalid port	Bits 4-7 of WR0(L) were not 0000.

INSN STEP/DPLY PCR

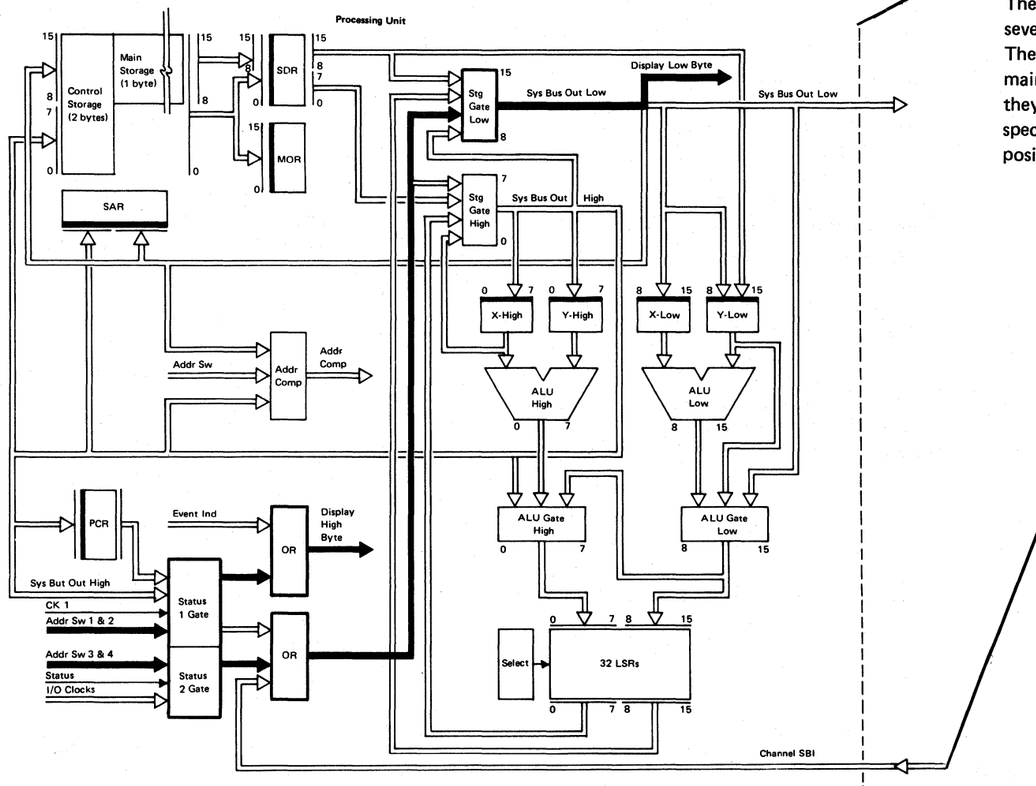
With the mode selector switch in this position, each time CE START is pressed, the next sequential instruction is executed. Also, the 8 bits of the processor condition register are displayed in the leftmost byte of the display lights. The rightmost byte is not significant.

SYS INSN STEP

When the mode selector switch is turned to this position, the STOP light comes on. Each time START is pressed and released, one system instruction is executed. One exception to this is the supervisor call instruction (SVC) which is not executed.

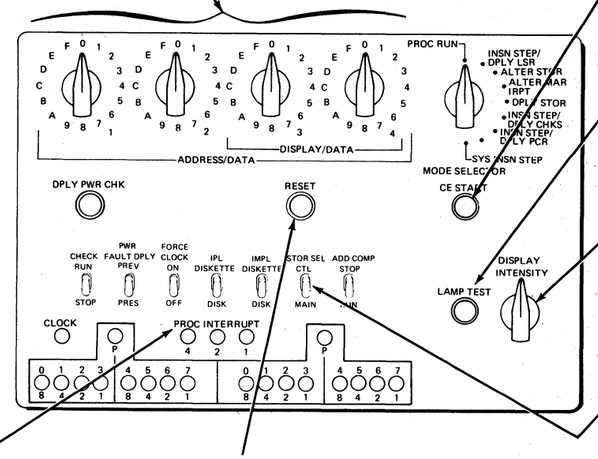
If the CPU was running when the mode selector switch was moved to the SYS INSN STEP position, CE START must be pressed and released to complete the system instruction that was in progress.

Specific CPU Data Flow for Display Switches



Address—Data—Display Switches

These switches are used in conjunction with several positions of the mode selector switch. They are used to enter addresses and data into main storage or control storage. In addition they are used to address the LSRs. Their specific use is covered under the various positions of the mode selector switch.



CE START Switch

Pressing this switch causes execution of instructions to begin at the address specified by the current micro address register.

LAMP TEST Switch

When this switch is pressed, all system lights are turned on unless they or their circuits are defective.

DISPLAY INTENSITY Control

This control adjusts the intensity of the CRT display.

STOR SEL Switch

This switch controls whether main storage or control storage is addressed on manual operations and address compare operations.

When addressing main storage on a manual operation or address compare operation, the switch must be in the MAIN position. To address control storage on a manual operation or address compare operation, the switch must be in the CTL position.

PROC INTERRUPT Lights

These lights indicate which interrupt level is currently in progress. The interrupt is indicated in the lights as follows:

Lights			Interrupt Level
4	2	1	
X	X	X	Zero (Machine Check)
		X	One
	X		Two
	X	X	Three
			Main Level

RESET Switch

Pressing this switch causes the following to occur:

1. The micro address register (MAR) is initialized to '0000'.
2. Present power fault conditions are transferred to previous power fault conditions and the present power fault condition latches are reset.
3. The CPU timing circuitry is set to an initialized state.
4. Error and status indicators are reset.
5. The PCR is initialized to the equal condition.

The RESET switch is also used to check for system bus in and the PCR bits remaining at the wrong state. If a bit is on, the P bit high is displayed while RESET is pressed.

To restart the system, press CE START. To reload, press LOAD.

CHECK RUN/STOP Switch

This switch controls whether the system runs or stops when a parity error occurs.

When the switch is in the STOP position, the system stops at the end of the current micro-instruction when a parity error occurs. When in the RUN position, the error is retained but the system continues to run.

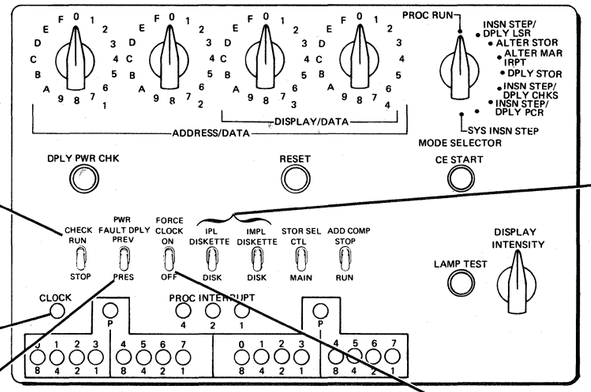
CLOCK Light

This indicator is turned on by the run latch or the 'block processor clock' signal from an I/O device.

PWR FAULT DPLY Switch and DPLY PWR CHK Switch

When a system power failure occurs, the power supply at fault and the type of failure are stored in latches. These latches are on the power sequence card and retain the information as long as the main line switch is kept on. These latches are known as the 'present power fault' latches. When RESET is pressed and the console power brought up (or on a power off sequence), the information recorded in the 'present power fault' latches is transferred to another set of latches known as the 'previous power fault' latches. Thus the reason for a current power failure and the reason for a preceding power failure can be stored in latches. The content of the power fault latches may be displayed even though console power is down.

To display the 'present power fault' latches, the PWR FAULT DPLY switch must be in the PRES position when the DPLY PWR CHK switch is pressed. If the PWR FAULT DPLY switch is in the PREV position, the 'previous power fault' latches are displayed.



The power fault conditions are displayed in the leftmost byte on the CE panel. The meaning of the specific bits is as follows:

Bits 0 and 1
- 01 — Undervoltage
- 10 — Overvoltage
- 11 — Overvoltage

Bits 2 and 3
- 01 — Multilevel supply
- 11 — Dual-level supply Note 2

Bits 4 through 7
- 0000 — Note 1
- 0001 — -4V at fault
- 0010 — +5V at fault
- 0011 — -5V at fault
- 0100 — +6V at fault
- 0101 — +8.5V at fault
- 0110 — +12V at fault
- 0111 — -12V at fault

  (Multilevel supply)
- 1000 — +24V at fault
- 1001 — -24V at fault

  (Dual-level supply (Note 3))
- 1111 — Plus and minus 24V dual-level supply failure or +5V, +8.5V and -12V failing in the multi-level supply.

Notes:

1. If the voltage level being monitored is near the trip point of the respective monitoring circuit, bits 0 through 7 will indicate one of the following:
   - 0101 0000 — Undervoltage in multilevel supply
   - 0111 0000 — Undervoltage in dual-level supply
   - 1001 0000 — Overvoltage in multi-level supply
   - 1011 0000 — Overvoltage in dual-level supply
2. A previous power fault indication of 1111 1111 may be indicated when the main line switch is switched from OFF to ON.
3. If power is up when a short occurs in the +24 Vdc distribution, the fault indications will be as shown in the chart. If the short exists when power is brought up, an under-voltage indication will probably occur.

IMPL-IPL Switches

The IMPL and IPL switches select the IMPL (initial microprogram load) and IPL (initial program load) devices. The IMPL and IPL devices are the disk drive (disk) and the 33FD (diskette).

During normal operations, both IMPL (control storage load) and IPL (main storage load) are from the disk drive. When LOAD is pressed, control storage is first loaded with system diagnostic tests from the IMPL device. After successful completion of these tests, the emulator and SCP (system control program) are loaded. The micro-program then loads main storage from the selected IPL device.

IMPL Switch

This switch selects the IMPL device. In the DISK position (normal position), IMPL is done from the disk drive when LOAD is pressed. In the DISK-ETTE position, IMPL is done from the 33FD.

IPL Switch

The DISK position (normal position) of this switch selects the disk drive as the IPL device. In the DISK-ETTE position, IPL is from the 33FD.

FORCE CLOCK ON/OFF Switch

This switch initiates continuous CPU cycles. With the mode selector switch in the ALTER STOR position, the contents of the data switches are transferred to consecutive main or control storage location (depends on STOR SEL switch setting) when FORCE CLOCK is turned ON. The system also operates in the check run mode; that is, a processor check will not stop the machine. The starting address is contained in MAR. Turning the switch to OFF terminates the operation.

ADD COMP STOP/RUN Switch

This switch is used in conjunction with the STOR SEL switch and the address switches. An address compare sync signal (A-A1J2D12) is provided whenever the address switches match an address in SAR. The STOR SEL switch determines if the sync occurs on a main storage or control storage address.

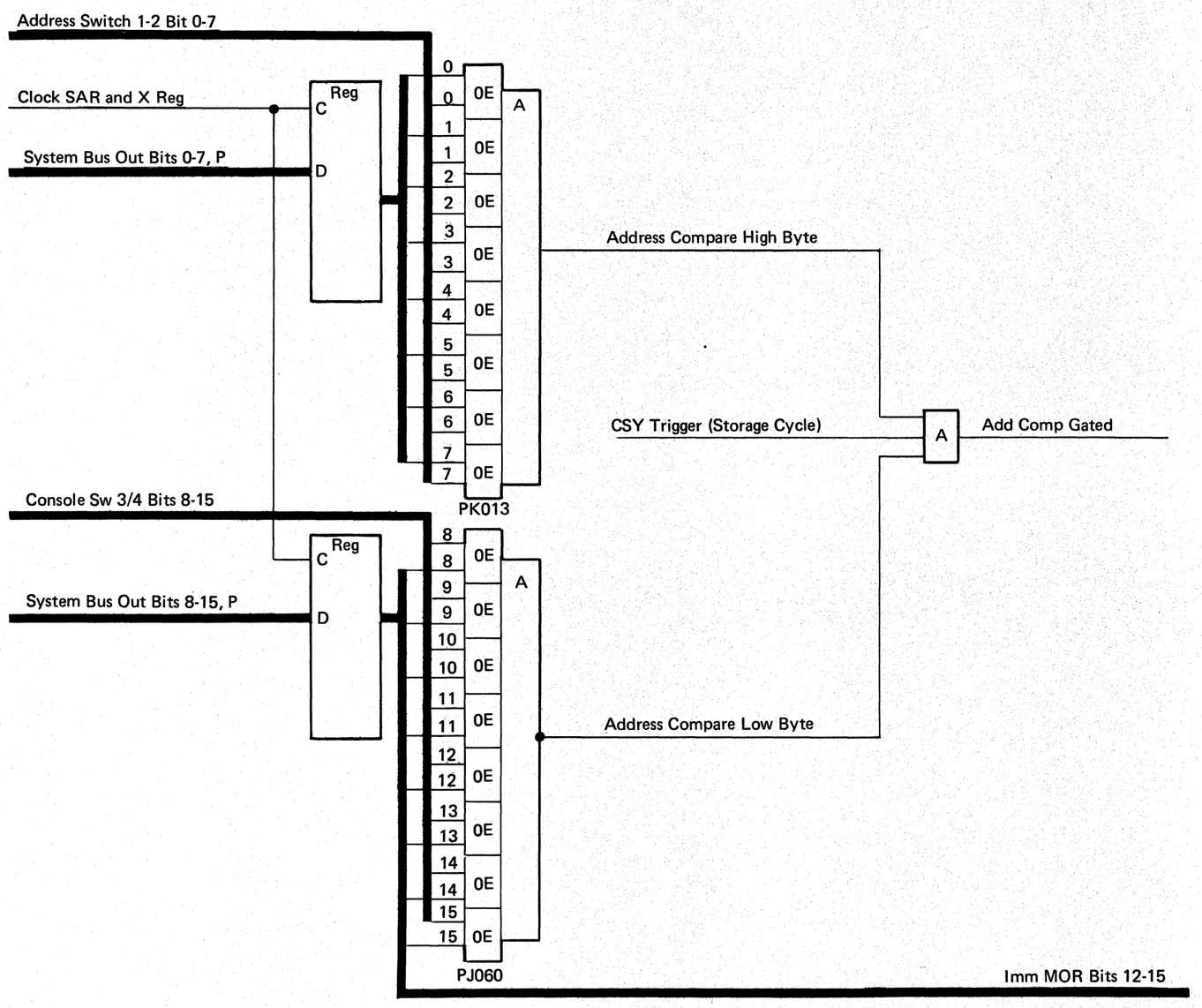
If the switch is in the RUN position, the system will continue after a compare occurs.

If the switch is in the STOP position, the system will stop. The exact time the system will stop is determined by the following:

- If the address stop is on a main storage address, the emulator completes the system instruction being executed and then stops all system level operations with STOP light on. The system may be restarted by pressing the operator panel start key.
- An address compare on a control storage address stops the CPU clock after executing the micro instruction at that address. To restart, press CE START.

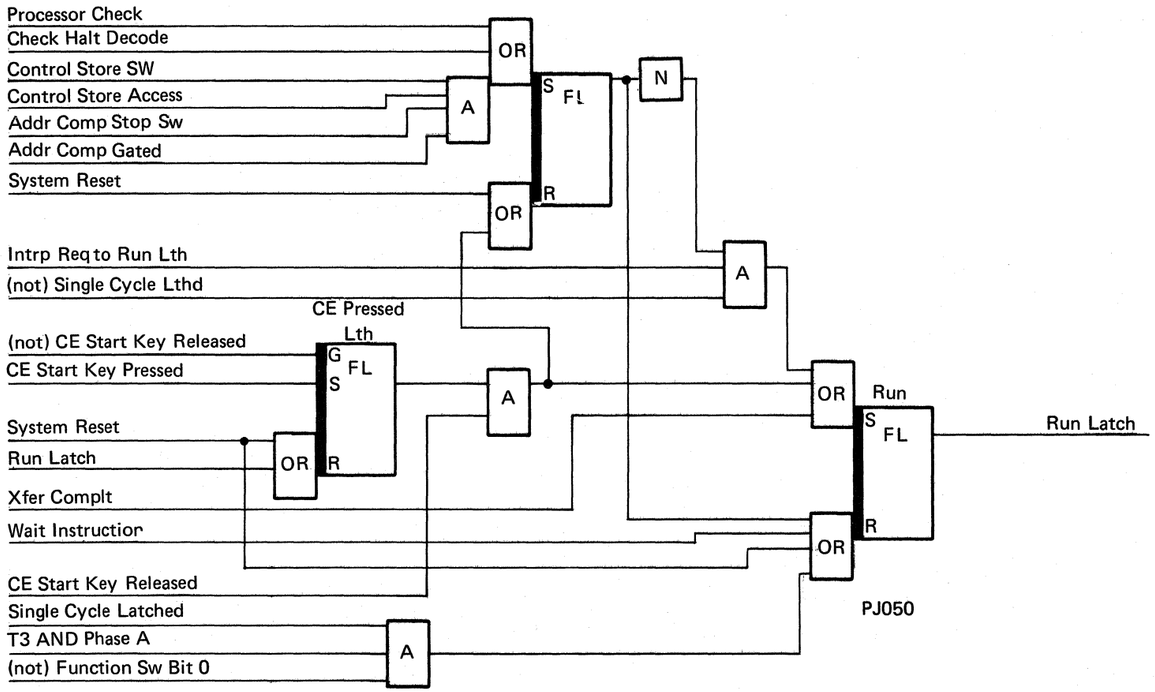
If an address compare stop is made on a control storage address during the execution of a system I/O instruction, the results of the instruction are unpredictable.

Circuit detail is shown at the right.



Run Signal

The circuits that set and reset the run latch are shown here. The switches that affect the run latch are described on the opposite page. Checks that reset the run latch (or inhibit the set) are described on ERR HDL-1.



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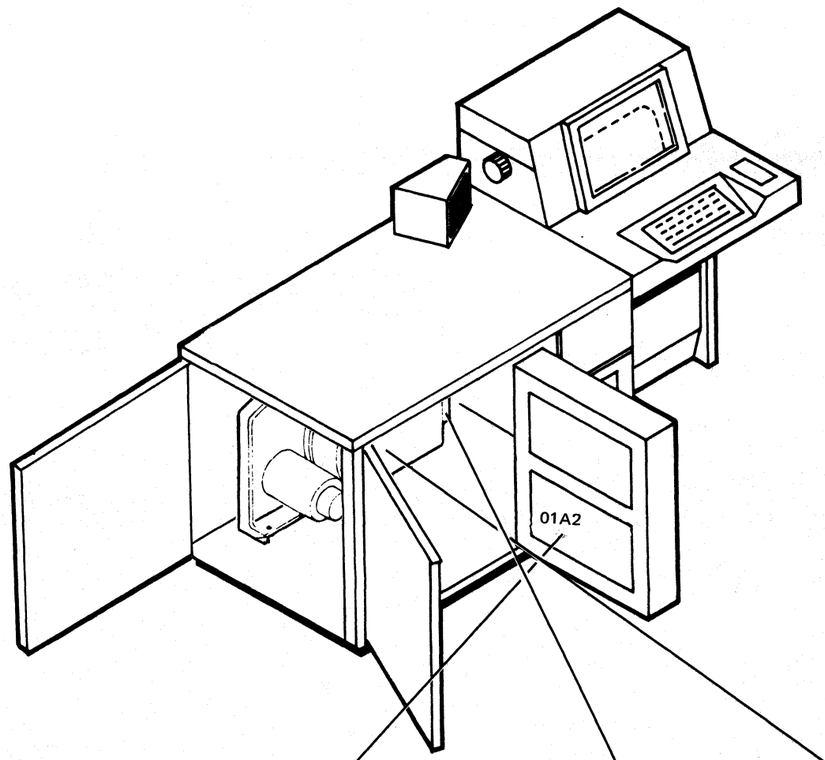
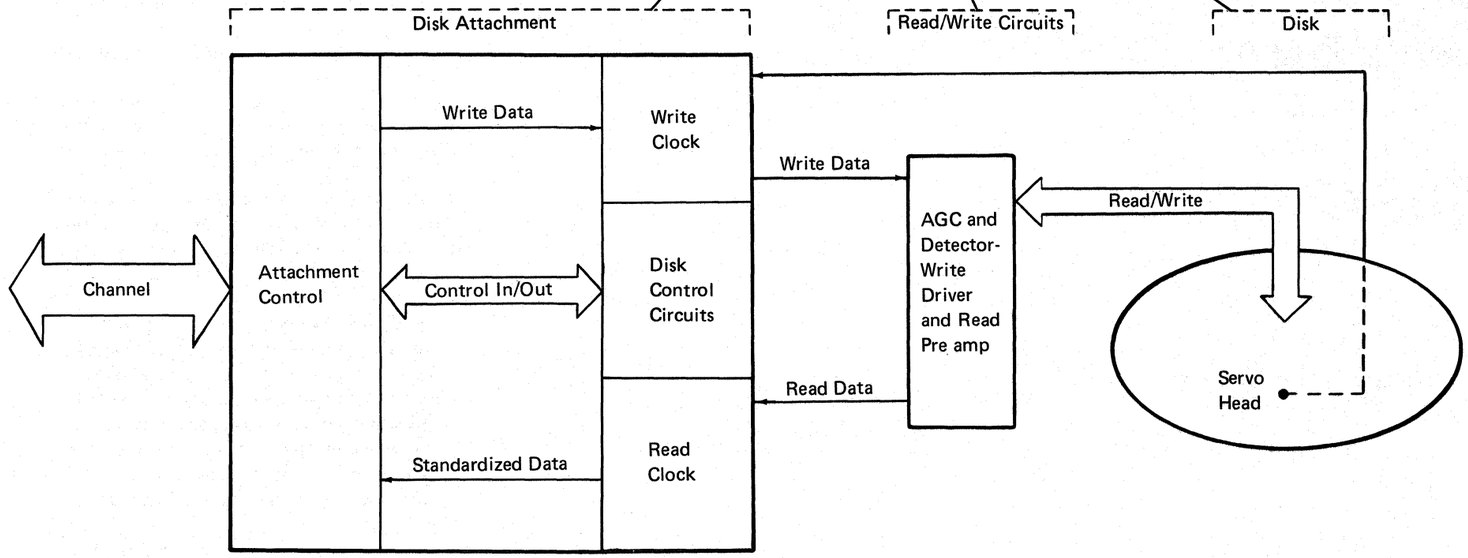
Disk Drive

The IBM disk drive has one permanently mounted magnetic coated disk. Data is written and read from the disk by heads attached to the swinging actuator. The disk drive has 3.2, 5.0, 9.1, or 13.7 megabytes of storage, depending on the system model number.

The disk circuitry is housed in two separate areas; on the disk enclosure and on the 01A2 board (I/O board). The servo head output preamplifier is mounted on the actuator arm. Part of the head selection circuitry is mounted on the disk enclosure. The remainder of the file electronic circuits are mounted on the 01A2 board (I/O board).





Data Tracks

Data heads record data on (and read data from) the data tracks. Each track is divided into 60 sectors. The data stored in one sector is called a record. Each record consists of 256 bytes; therefore, it is possible to store 15,360 bytes per track. The tracks that can be read without moving the actuator are called a cylinder.

The capacities of the various models are shown in the following chart:

Disk Capacity in Megabytes	3.2	5.0	9.1	13.7
Number of Tracks	218	338	606	909
Number of Cylinders	109	169	303	303
Data Heads — Tracks per Cylinder	2			3
Bytes per Sector — (record)	256			
Sectors (records) per Track	60			

Because the disk is formatted into cylinders and sectors, each record on the disk has a definite address consisting of cylinder, head, and sector numbers. This address (part of the identification field) is recorded at the physical location of the record on the disk.

Some areas of the disk are reserved; these areas are shown in the *IBM System/32 Diagnostic User's Guide* (PN 2547690).

Servo Tracks

The servo tracks of the disk contain prewritten patterns on the outer half of the disk. These patterns correspond to each data track location and consist of missing clock pulses and position pulses in a specific sequence. The 2.1 μs clock pulses develop the 140 ns write clock pulses in the attachment. The position pulses keep the data heads over the specified track (see DISK-6).

Specific combinations of clock and position pulses define either the beginning of a track (index pulse that indicates sector 00) or the beginning of sectors 01 through 59 (sector pulse).

The servo tracks are used by the servo head to keep the data heads on track and to perform seek operations.

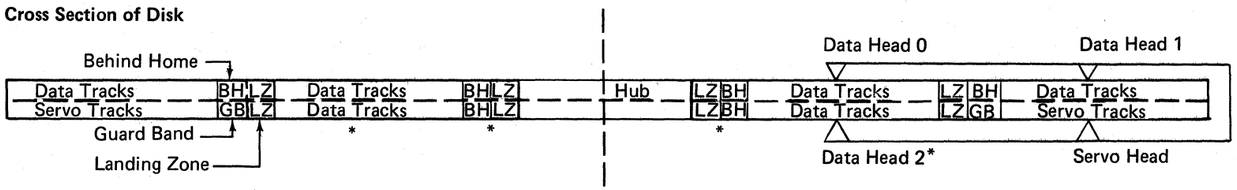
Landing Zone (LZ)

Because the heads touch the disk when it slows to less than 400 rpm, the heads are retracted to a landing zone to avoid destruction of data. No information is written in the landing zone.

Guard Band (GB)

Between the servo tracks and the landing zone is the guard band. The guard band is a servo track area that contains clock and position pulses but no prewritten patterns. When the servo head is in the guard band position, the data heads are behind home (BH).

Cross Section of Disk

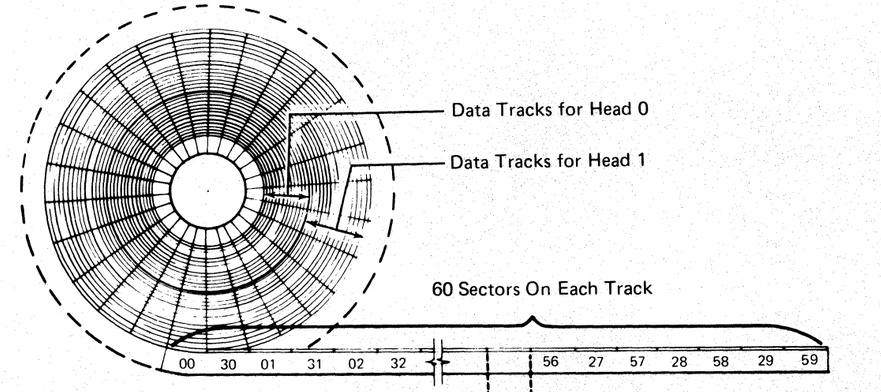


*13.7 megabytes only

Sector Format

Before writing in the data field, the ID field must be read to verify that the data is being written in the correct sector. The recovery time from the write operation to the read operation is too long to allow writing of consecutive sectors because the microprogram requires time to set up the next operation. For this reason, the sectors are numbered: 00, 30, 01, 31 . . . 06, 36, 07, 37, etc, as shown in the illustration.

Sector 06		Sector 36		Sector 07		Sector 37	
ID	Data	ID	Data	ID	Data	ID	Data
Recovery Time		Rd	Write	Recovery Time		Rd	Write



VFO sync is 12 bytes of hex FF used to synchronize the read clock with data bits from the disk.

When the 12 VFO sync bytes are being written on the disk, the attachment forces 8 bytes of hex FF, and then cycle steals the other 4 bytes from a 10 byte field of hex FFs in storage.

Note: If a sector defect occurs within the ID region (VFO sync through the ID field CRC), this VFO sync is extended 64 bytes (12 plus 64 equals 76 bytes), and then the address of an alternate sector is written.

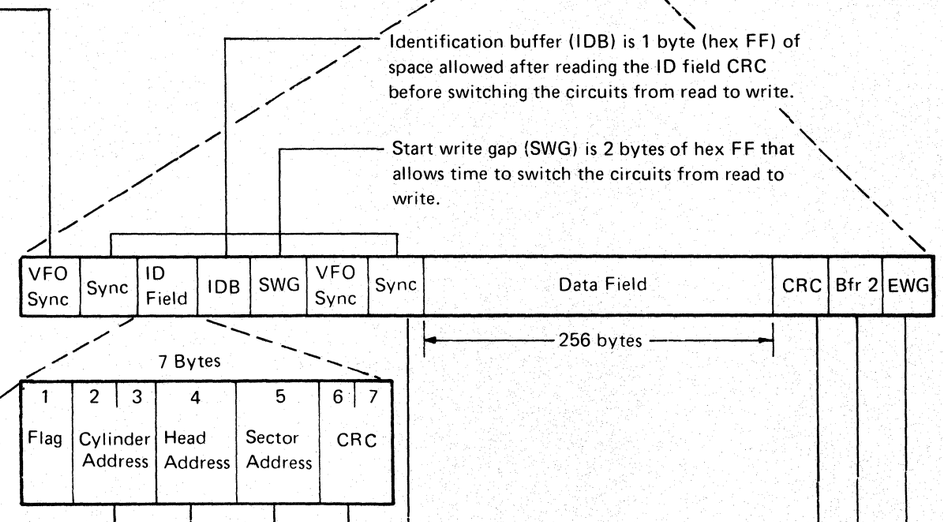
ID field is 7 bytes as described below.

Flag Byte:

Bits	Meaning	
0-4	Unassigned	
5	Data in sector might not be good	
6-7	00	Good primary sector
	10	Defective primary sector
	01	Good alternate sector
	11	Defective alternate sector

The cylinder address is 2 bytes.

Disk Capacity	Cylinder Address
3.2 Megabytes	0 to 108
5.0 Megabytes	0 to 168
9.1 Megabytes	0 to 302
13.7 Megabytes	0 to 302



Identification buffer (IDB) is 1 byte (hex FF) of space allowed after reading the ID field CRC before switching the circuits from read to write.

Start write gap (SWG) is 2 bytes of hex FF that allows time to switch the circuits from read to write.

Sync is 1 byte, hex 0E, used to synchronize the bit ring. The bit ring gates the bits read from the disk into the serializer-deserializer to be formed into recognizable bytes.

CRC (cyclic redundancy check) is 2 bytes of check characters to verify that the data was read correctly from the data field.

Buffer 2 (Bfr) is 4 bytes (hex FF) of space allowed after writing the data field CRC before switching the circuits back to read.

End write gap (EWG) is 2 bytes of hex FF to allow time to switch the circuits from write to read.

The head address is 1 byte, hex 000 for head 0, hex 01 for head 1, or hex 02 for head 2.

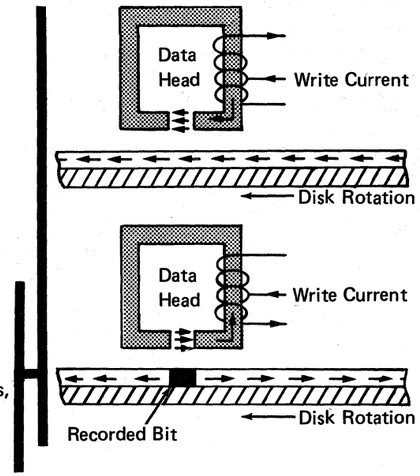
The sector address is 1 byte, 0 to 59.

CRC (cyclic redundancy check) is 2 bytes of check characters to verify that the data was read correctly from the ID field.

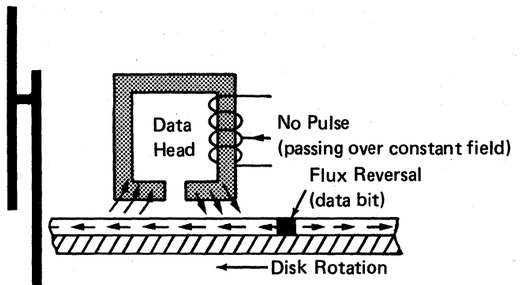
Data Recording

Data is read and written by data heads when the disk is spinning at 2964 rpm. When the disk is stationary, the heads are in the landing zone, and are in contact with the disk. To minimize head wear, the start and stop times of the disk are controlled (high torque start motor when starting, motor brake when stopping).

During a write operation, a 0 or 1 bit is recorded by reversing the direction of the current in the coil, which reverses the flux direction in the pole piece and reverses the flux in the gap. At the instant that the flux in the pole piece gap reverses, the direction of magnetization changes on the disk surface. Each reversal represents a recorded 0 or 1 bit.

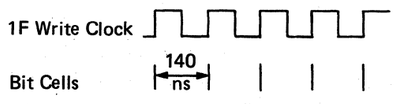


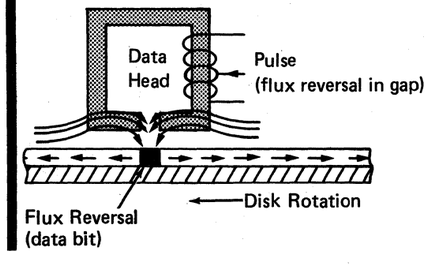
During a read operation, with the recording surface magnetized in one horizontal direction, constant flux flows and the coil registers no output voltage. However, when a recorded bit (180 degrees horizontal flux reversal) passes the gap, the flux flowing through the ring and coil reverses and produces a voltage output pulse.



Only data bits are written on the disk data tracks. For write operations the attachment uses clock pulses read from the servo tracks to develop the write clock. However, on read operations the read clock is developed from the VFO sync fields and from the data being read.

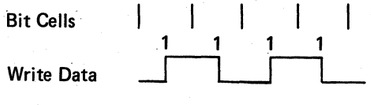
The period of time during which a data bit may be written is known as a bit cell. A bit cell is 140 ns long and is defined by the '1F write clock' line:





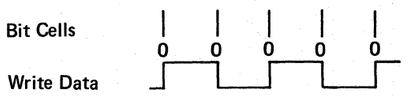
Writing 1-Bits

One bits are always written at the middle of a bit cell:

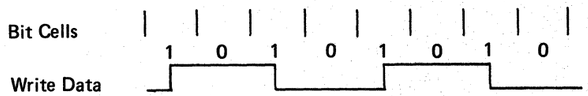


Writing 0-Bits

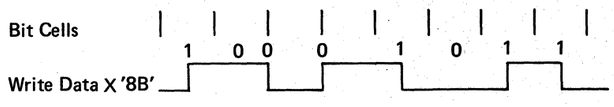
With one exception, 0 bits are always written at the beginning of a bit cell:



The exception to writing 0 bits at the beginning of a bit cell is when the 0 bit immediately follows a 1 bit. In this case, no bit is actually written and the 0 bit is represented by the absence of change during its bit cell time:



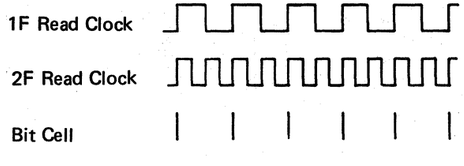
By writing X'88' both methods of writing 0 bits and the method of writing 1 bits can be illustrated:



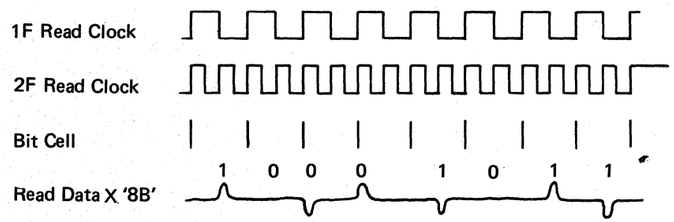
The data to be written is transmitted to the write circuits mounted on the disk drive via the two 'data transmission lines' A . For each transition on the 'data transmission lines' a 0 or 1 bit is written on disk. These transitions cause the current to be switched in the write head which results in a polarity change on the disk track.

Reading Data Bits

When data is read from the disk, the read clock is synchronized to the incoming data by the VFO sync field. This field consists of 12 bytes of 1 bits. The read clock output consists of two lines, '1F read clock' and '2F read clock'. Because the read clock has been synchronized by the 1 bits of the VFO sync field, these lines may be used to define bit cell time:

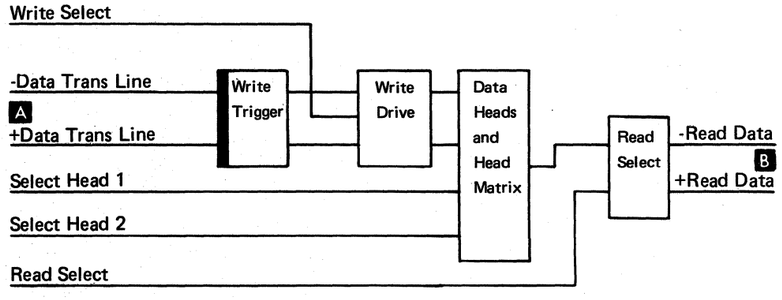


Bits that occur on the read data line may be identified as 0's or 1's depending on when they occur relative to the read clock times (or bit cell):



The signals on the 'read data' lines B are signals shaped in the disk drive circuits mounted on the attachment gate.

The variable frequency oscillator (VFO) driving the read clock constantly monitors the bits being read and varies its frequency to keep the read clock and incoming data in sync.



Seek Operation

During a seek operation, the track following signal to the actuator driving circuits is overridden by signals from the seek controls. A seek is executed by activating the drivers to move the actuator at the correct velocity to the specified track. At the end of a seek, the seek lines to the drivers are deactivated; this allows the track following circuits to hold the actuator at the selected track.

Seek control causes the actuator to leave track following mode, and accelerates the actuator over a specified number of tracks. Seek control then drives the actuator at a constant velocity until it is a specified number of tracks from the required destination. Then the actuator is decelerated and stops at the required destination. At this point, track following signals take control.

Recalibrate Operation

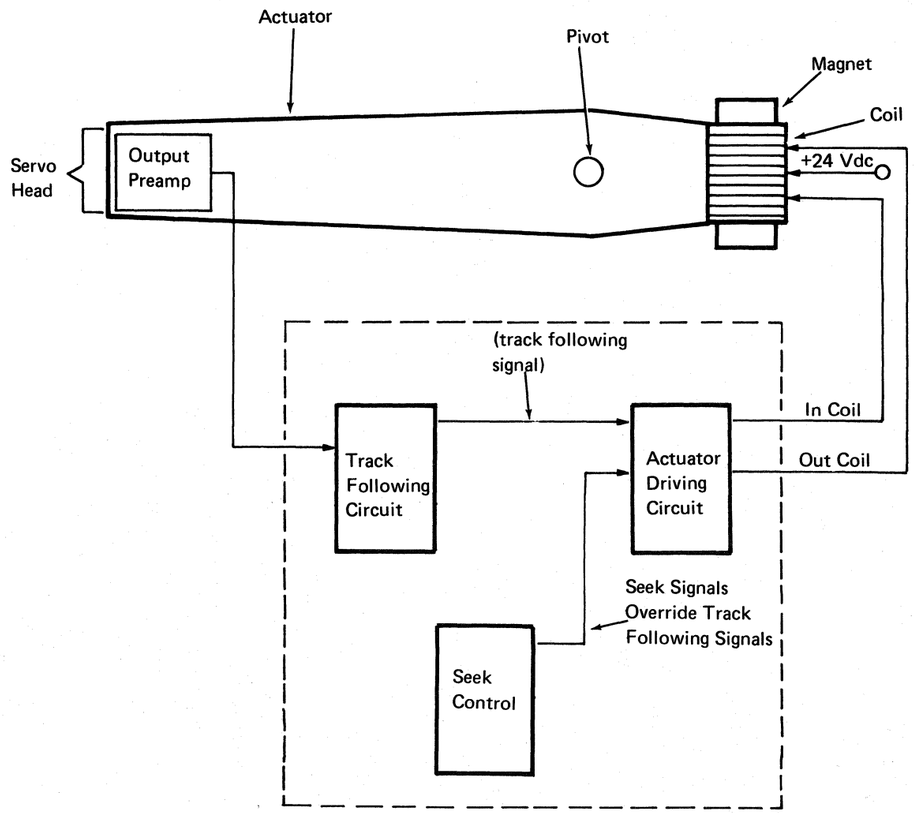
The recalibrate operation moves the heads across the tracks into the guard band area, then out to data track 0 (home).

Recalibrate is initiated:

1. During a normal power on sequence.
2. When an invalid sector identifier (ID) is read.
3. After data unsafe is reset.

Behind Home

If the data heads attempt to seek a track that is farther in than track 0, the seek in command is dropped. When the heads stop, the actuator seeks to track 0 and home is indicated.

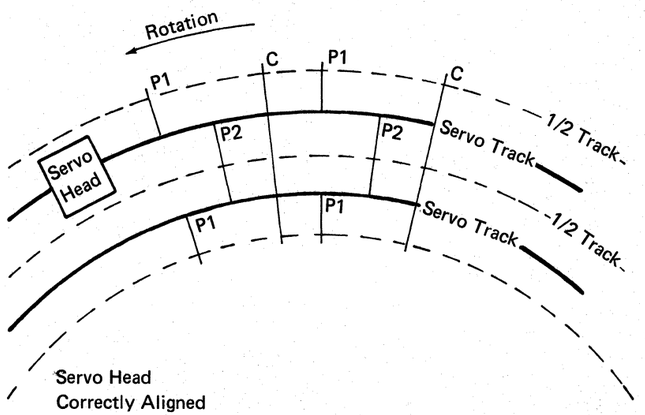


Disk Drive Circuit on 01A2 (I/O board)

Servo Track Following

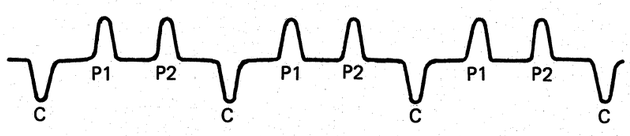
Servo Head Correctly Aligned

The direction of rotation shown is as seen from the read/write heads. Format of C and P pulses are prewritten around the servo tracks. The servo head is shown correctly aligned on a servo track.



Servo Head
Correctly Aligned

Signal at Servo Head when Correctly Aligned



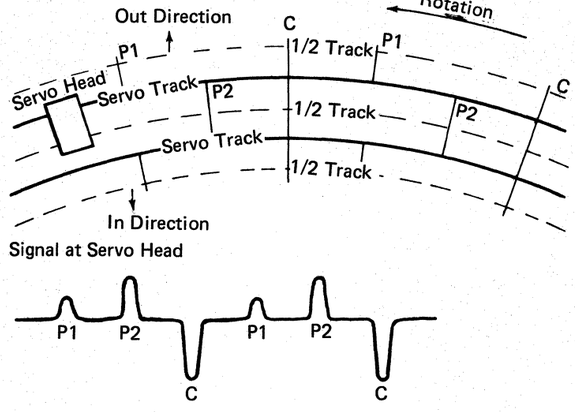
Servo Head Offset

The servo control ensures that the position pulses are received at equal amplitudes.

If the servo head moves off track, one position pulse is received at a reduced amplitude, and the other position pulse is received at an increased amplitude.

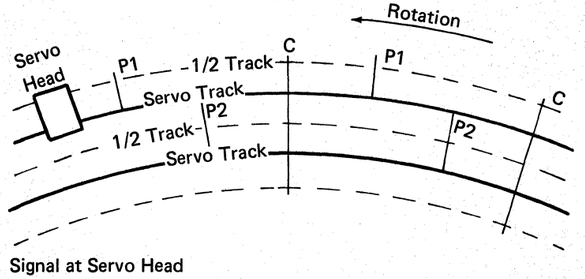
The servo control drives the head in the direction that increases the amplitude of the reduced position pulses (P1 or P2). The direction and degree of movement of the heads, to compensate for the error, is determined by the track being odd or even and the difference between the P1 and P2 pulses.

Servo Head Offset (in direction)

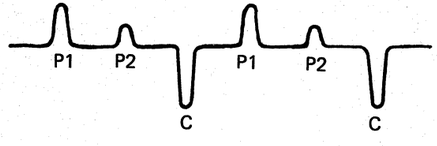


Signal at Servo Head

Servo Head Offset (out direction)



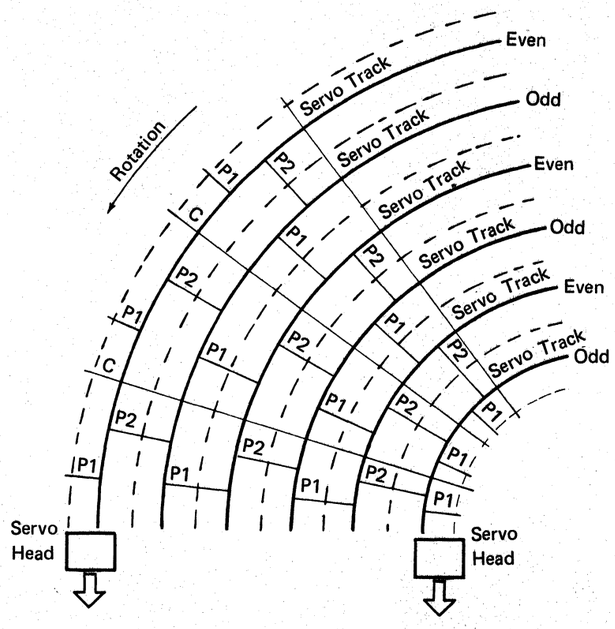
Signal at Servo Head



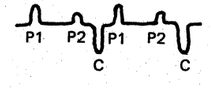
Servo Head Offset, Odd and Even Tracks

During a seek operation, 'seek 2' drops one track before the required track. The servo control then takes over and aligns the servo head onto the correct track.

The signal 'even track' (+ for even, – for odd) determines whether P1 or P2 is selected to gate the in or out demodulator; the demodulators keep the servo head moving in the direction of the seek, until the position pulses are the same amplitude.



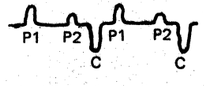
Even track, servo head offset. Servo head signal.



P1 minus P2 = Required servo head movement.

When the seek is to an even track P1 is gated to the in demodulator, P2 is gated to the out demodulator.

Odd track, servo head offset. Servo head signal.

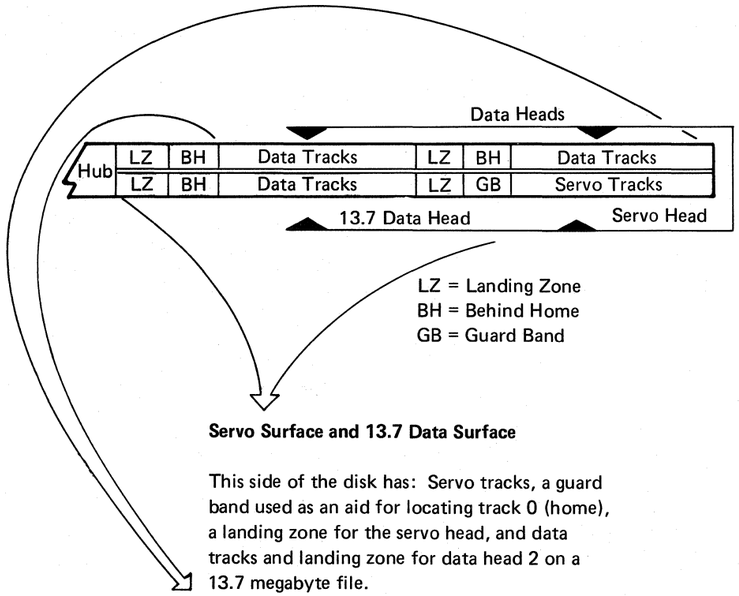


P1 minus P2 = Required servo head movement.

When the seek is to an odd track P1 is gated to the out demodulator, P2 is gated to the in demodulator.

Head Positioning and Disk Layout

One side of the disk is a data surface only. The other side is the servo surface and the additional data surface for the 13.7 data head.



Servo Surface and 13.7 Data Surface

This side of the disk has: Servo tracks, a guard band used as an aid for locating track 0 (home), a landing zone for the servo head, and data tracks and landing zone for data head 2 on a 13.7 megabyte file.

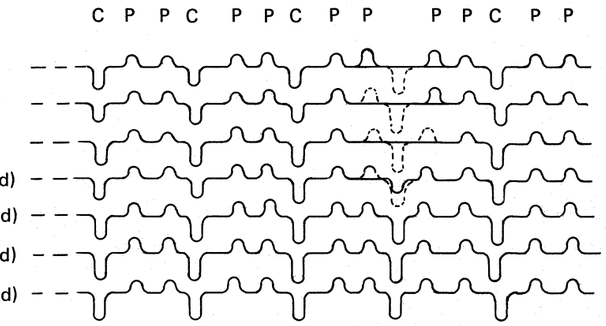
Data Surface

Two data areas and two landing zones on this side of the disk. One data area and landing zone for data head 0, and one data area and landing zone for data head 1. No data is written in the landing zones.

P – Position pulse
C – Clock pulse

Missing Clock Pulse (and Position Pulses)

Patterns of missing clock pulses decode into index pulses, sector pulses, or sector midpoints (activates the "data area" line).



Data Track–Servo Track Relationship

Servo circuits determine data track positions by analyzing signals received from the odd and even servo tracks.

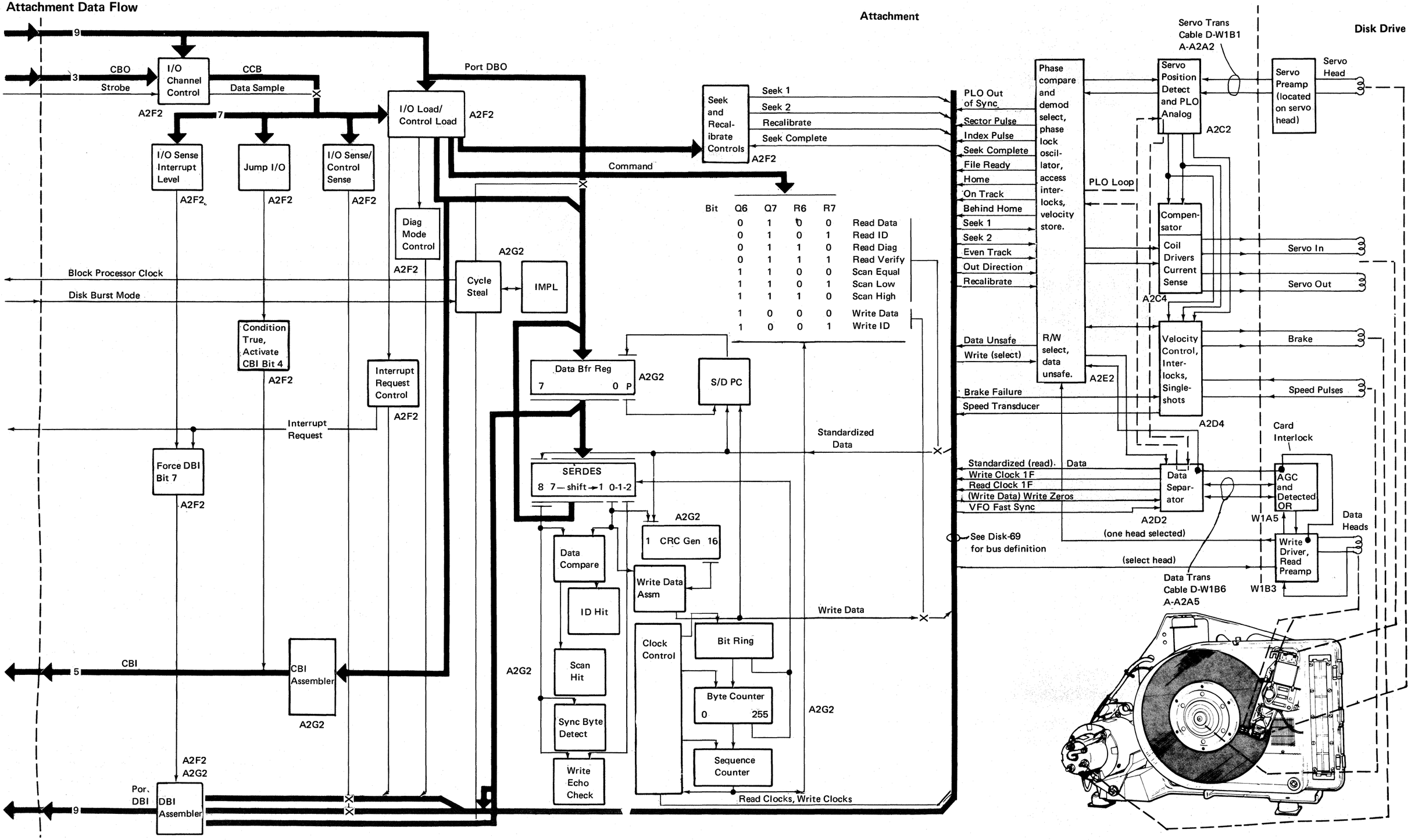
Positioning the servo head directly over the border between two adjacent servo tracks, positions the data heads (mounted on a common carriage) over the corresponding data tracks.

Guard Band

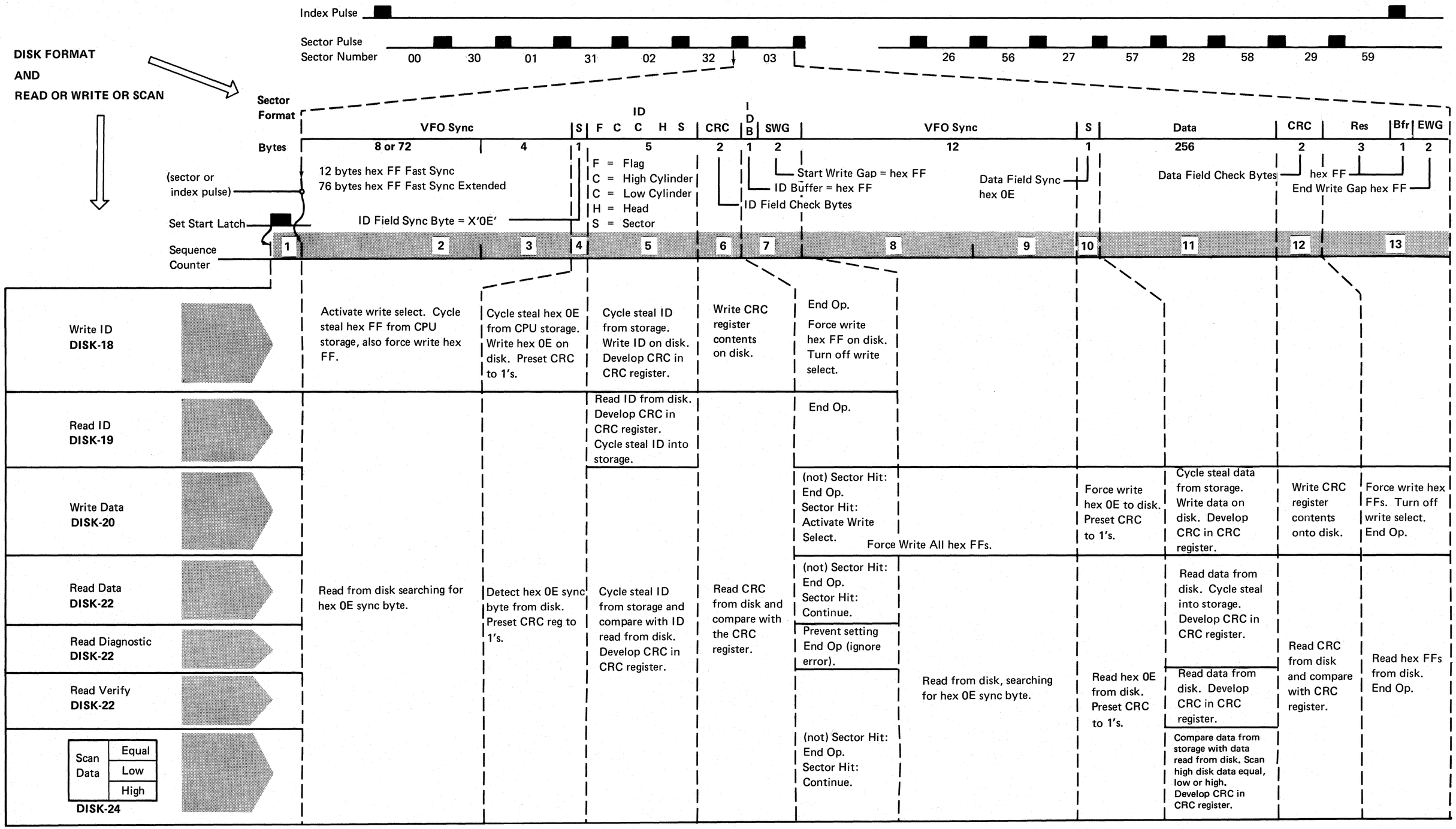
Guard band is a normal servo track area that has no index pulse, sector pulse, or sector midpoint. The guard band is detected at the servo track that has no missing clock pulses, which in turn indicates no data area pulses. The absence of data area pulses allows a 270 μs singleshot for 3.2 and 5.0 megabytes, or a 135 μs for 9.1 and 13.7 megabytes to timeout, which indicates guard band.

The guard band indicates that the data heads are behind home (data track 0). When guard band is detected, the attachment positions the data heads over track 0.

Attachment Data Flow



Read–Write–Scan–Data Destination



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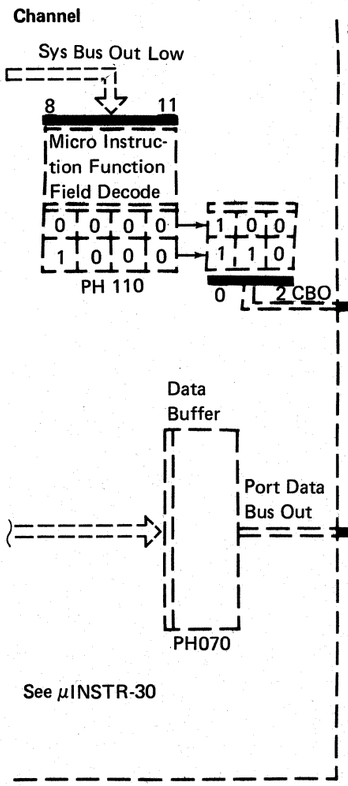
Load Command — Control Load Command



Select Attachment

DA 0-3 → Device Address Hit

Send Data Byte to Attachment DBO 0-7

Mod 4-7

CCB 012	CCB (Latched) 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
100 Load	0 0 1 0 Set interrupt request **DISK-64**								
	0 0 1 1 Reset Interrupt Request **DISK-64**								
	0 1 1 0 Enable Interrupt Request Control **DISK-64**					Data Op End **DISK-64**	Sector Pulse **DISK-64**	Index Pulse **DISK-64**	Seek Op End **DISK-64**
	1 0 0 1 Load Data Buffer Register **DISK-8**	Data Buffer Register (Load the data buffer register with a byte from an LSR located in the CPU.)							
	1* 0 1 1 Enable Diagnostic Mode **DISK-12**								
	1* 1 0 0 Disable Diagnostic Mode **DISK-12**								
	1* 1 0 1 Diagnostic Mode Control **DISK-12**	CSY Trigger **DISK-12**	Disk Cycle Strobe	Set Sector Pulse **DISK-12**	1F Write Clock Toggle **DISK-12**	1F Read Clock Toggle **DISK-12**	Increment Seek Counters **DISK-12**	Index Pulse **DISK-12**	Set (1)/Reset (0) Read Data Bit Buffer **DISK-12**
	1 1 1 1 Reset Checks (reset error conditions) **DISK-46**								
110 Control Load	0 0 0 0 Rd/Wr/Scan Control **DISK-9 DISK 18-25**	Set start latch, set hit latch, reset op end latch reset scan hit latch (initiate rd, wr or scan).	Reset index pulse and sector pulse (reset latches for next command).	Set I/O working latch.	Set BR7 Late (diagnostic use)* **DISK-8**	Program DC Reset (programmable system reset). **DISK-46**		1=Control Store for ID 0=Main Store for ID **DISK-53**	(set) FD Busy **DISK-68**
	0 0 0 1 Seek Control **DISK-45**	Set Seek 1 and Seek Busy **DISK-45**	Recalibrate **DISK-45**	Seek In (direction) **DISK-45**	Seek Even **DISK-45**				High order bit of the track counter.
	0 0 1 0 Command Byte **DISK-9 DISK-18-25**	Fast sync extended (1=set, 0=reset). (note on **DISK-18**)	1=Control Store for data. 0=Main Store for data. **DISK-53**	R6	R7		Cycle steal low byte only (1=set, 0=reset). **DISK-53**	Q6	Q7
	0 0 1 1 Head Select **DISK-68**							Select Head 2 **DISK-68****	Select Head (0 = head, 0, 1 = head 1) **DISK-68**
	0 1 0 0 Load # of Tracks – 1 **DISK-45, 40**	Load # of Tracks–1 **DISK-45, 40**							
	0 1 0 1 Seek 1, Seek 2 Counters **DISK-45, 40**		Seek 1 Compare Value **DISK-45, 40**				9.1 or 13.7 megabyte file and 16 track or greater seek.	Seek 2 Count **DISK-45, 40**	
	0 1 1 0 End of Operation Reset								

(reset seek busy, file busy, R6, R7, Q6, Q7 latches)

R6	R7	Q6	Q7	Read, Write, or Scan	
0	0	0	1	Read Data	**DISK-22**
0	1	0	1	Read ID	**DISK-19**
1	0	0	1	Read Diagnostic	**DISK-22**
1	1	0	1	Read Verify	**DISK-22**
0	0	1	1	Scan Equal	**DISK-24**
0	1	1	1	Scan Low	**DISK-24**
1	0	1	1	Scan High	**DISK-24**
0	0	1	0	Write Data	**DISK-20**
0	1	1	0	Write ID	**DISK-18**

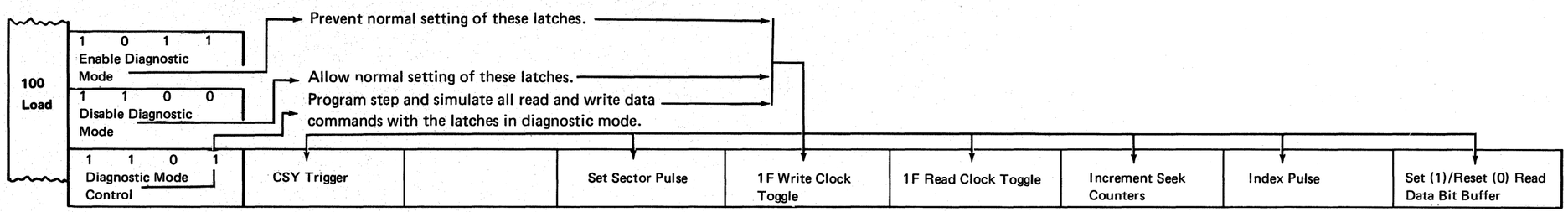
*For diagnostic purposes only — see next page.
**13.7 megabyte file only.

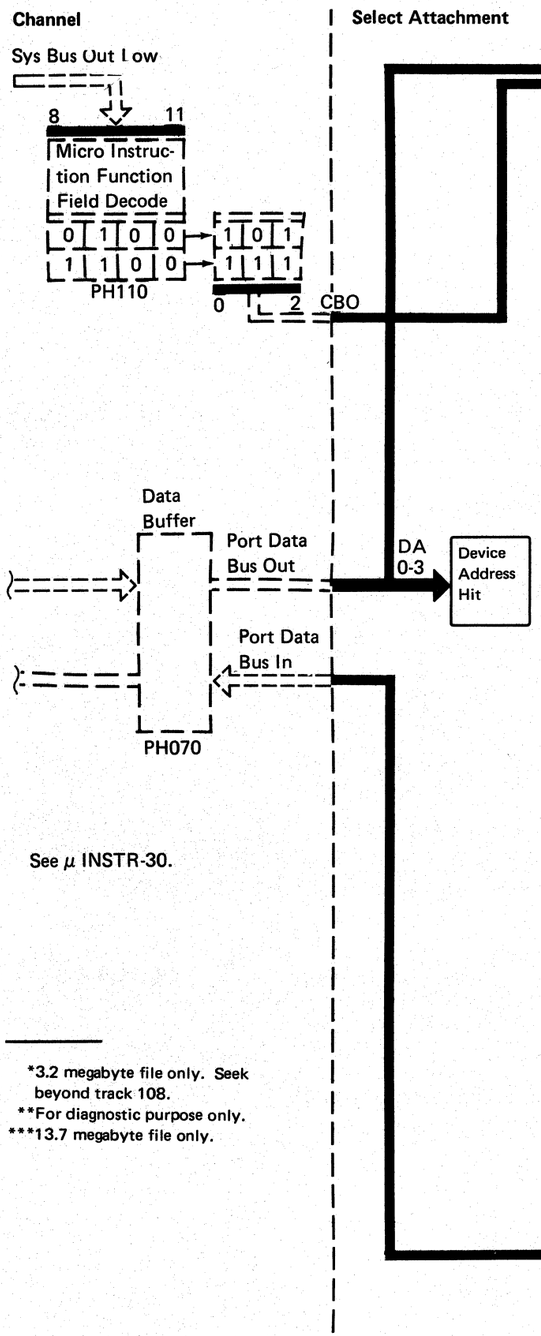
Diagnostic Load

Diagnostic Mode

Enable diagnostic mode degates the main control lines between the channel and the attachment and between the attachment and the disk drive. Then, diagnostic mode control can simulate these main control lines, which allows diagnostic programs to simulate all attachment operations.

This is the diagnostic portion of the load command shown on DISK-11.



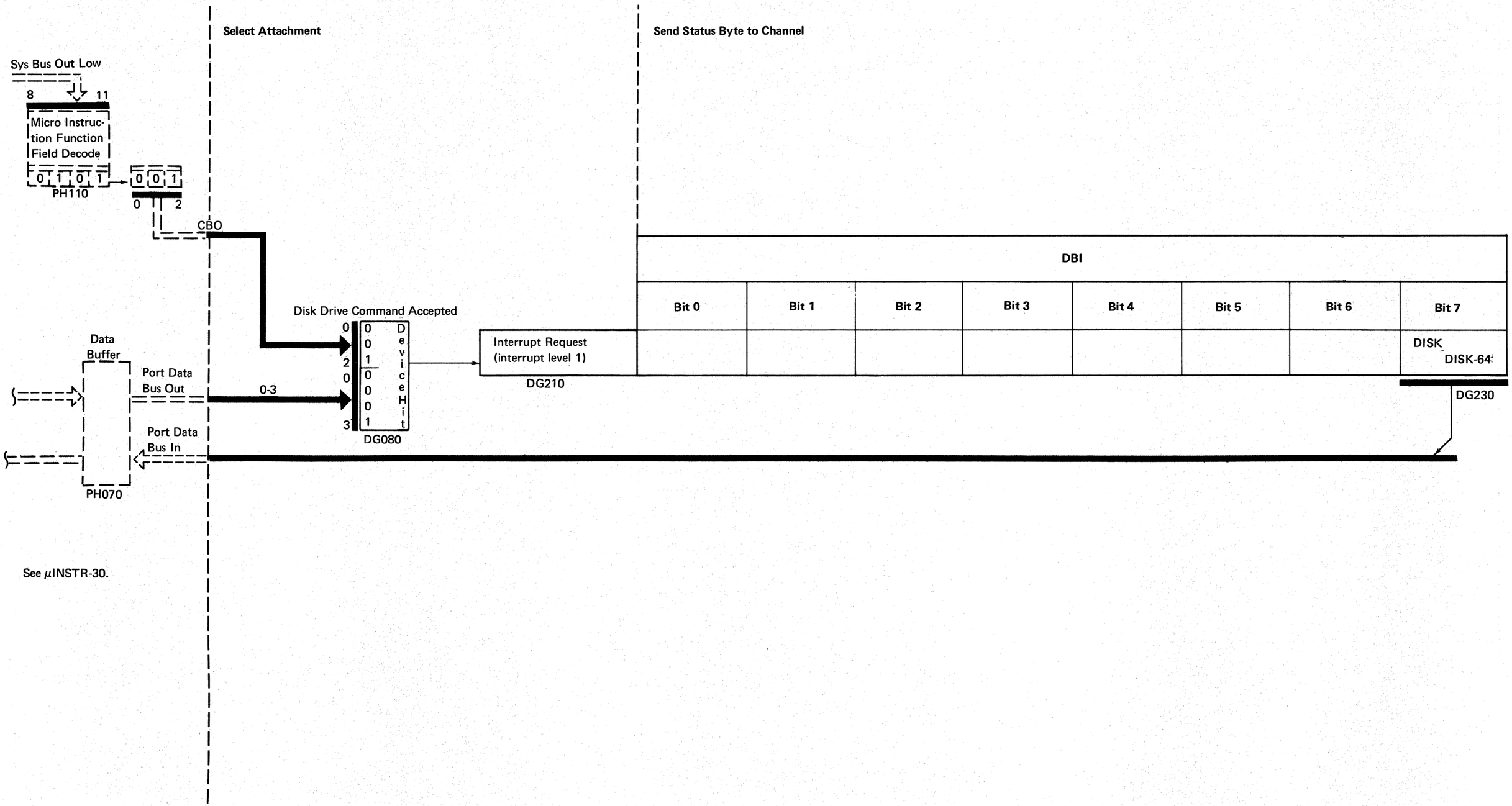


See μ INSTR-30.

CCB 0 1 2	CCB (Latched) 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense 101	0 0 0 0 Status Byte 0 DISK-15	Disk Not Ready DISK-65		Sector Sync Check Latch DISK-61	Off Track Error Latch DISK-62	CRC Check Trigger DISK-58	DBO Parity Check Latch DISK-55	Write Data Echo Check DISK-59	Cycle Steal Overrun Trigger DISK-56
	0 0 0 1 Status Byte 1 DISK-15	No-op	Data Unsafe DISK-65, DISK-38	Invalid Seek*	Adapter Check DISK-15	No Record Found	Scan Equal DISK-67	(not) Scan Hit Latch DISK-67	PLO Out of Sync Check (seek check) DISK-63
	0 0 1 0 Status Byte 2 DISK-15	Serdes Parity Check Trigger DISK-57	Write Check Trigger DISK-54	Channel Transfer Check Latch DISK-60		Interrupt Time Out DISK-64		Head 2 Selected ***	Head Selected (0 = head 0, 1 = head 1)
	0** 0 1 1 Diagnostic Byte DISK-8	CRC Generate Position 9-16 DISK-8							
	0 1 1 0 Interrupt Condition DISK-64				Interrupt Time Out DISK-64	Op end enabled op end latch. DISK-64	Sector Enabled — Sector Pulse Latch DISK-64	Index Enabled — Index Pulse Latch. DISK-64	Seek Op End DISK-64
	1 0 0 1 Data Buffer DISK-8				Data Buffer Register DISK-8	(Transfer data buffer register contents to a LSR located in the CPU.)			
Control Sense 111	0** 0 0 1 Diagnostic Sense DISK-45				Track Counter is 0 DISK-45	(not) Seek 1=Tracks 0 to 4. DISK-45	(not) Seek 2 Counter at 0. DISK-45		
	0** 0 1 0 Diagnostic Sense DISK-9, DISK-18-25					Op End Latch DISK-9	Sector Pulse Latch DISK-9	On Track DISK-45	
	0** 1 0 0 Diagnostic Sense DISK-8	Serdes Bit 0 DISK-8	Byte Counter Bit 4 DISK-8	Byte Counter Bit 256 DISK-8	Sequence Counter 3 DISK-8	Sequence Counter 6 DISK-8	Bit Ring 1 DISK-8	Cycle Steal Request Trigger DISK-48, DISK-51	Serial Write Data to File DISK-26
	0** 1 0 1 Diagnostic Sense DISK-45	(not) Seek 1 to File (wrap) DISK-45	(not) Seek 2 to File (wrap) DISK-45	(not) Recalibrate Command to File (wrap) DISK-45	(not) Seek Out to File (wrap) DISK-45	(not) Odd Track Destination to File (wrap) DISK-45	(not) Power on Delay to File DISK-46	Home DISK-65	Behind Home DISK-69
	0** 1 1 0 Diagnostic Sense DISK-28, 38, 46		Select Unsafe (head select error) DISK-38	Write Unsafe (write error) DISK-38	Brake Failure DISK-46	Servo Unsafe (servo error) DISK-38			Fast Sync to File (VFO fast sync) DISK-28
	0** 1 1 1 Diagnostic Sense DISK-28, 34, 40, 45	(not) File Guard Band DISK-34	(not) File VFL (velocity follow latch) DISK-40	(not) Select Out Drive (seek out) DISK-45	(not) Select In Drive (seek in) DISK-45		Linear Region DISK-40	Read Select/(not write select) DISK-28	

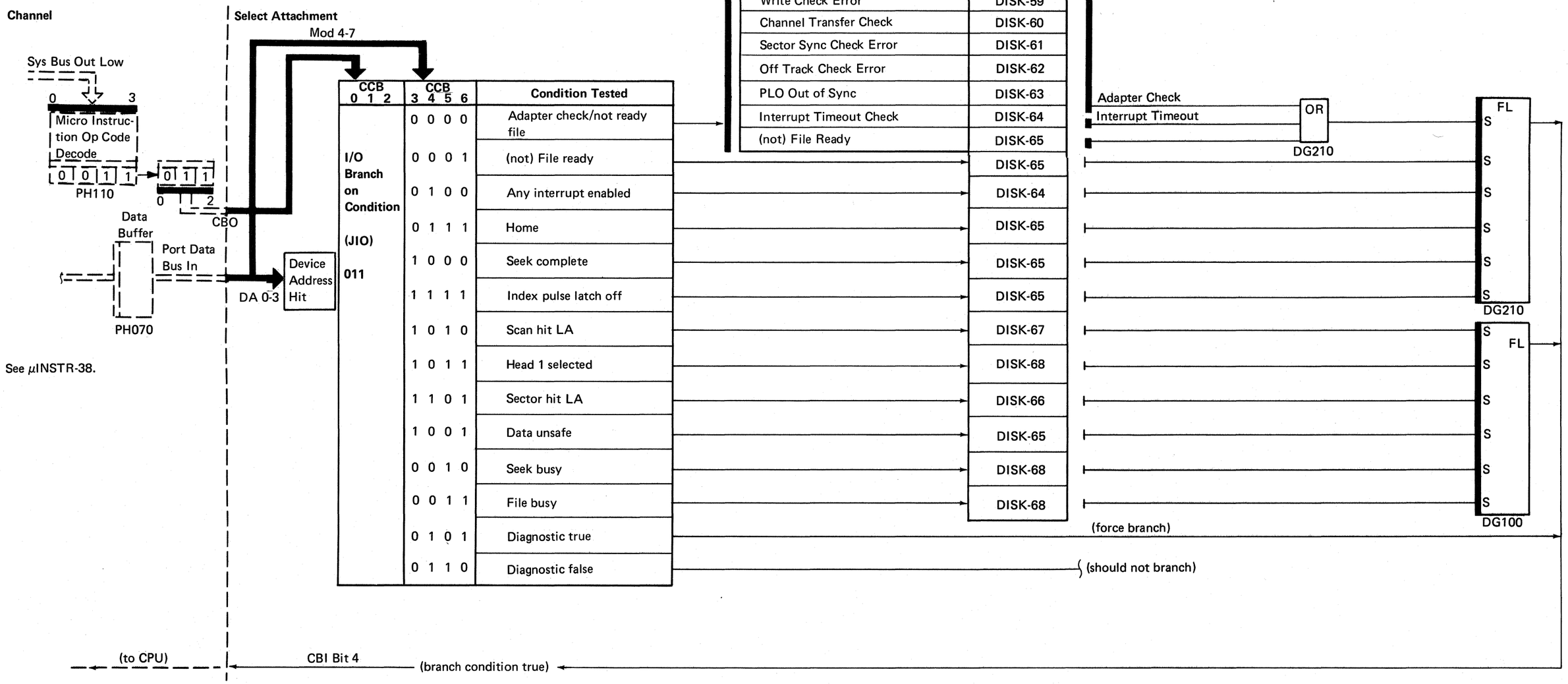
*3.2 megabyte file only. Seek beyond track 108.
**For diagnostic purpose only.
***13.7 megabyte file only.

Sense Interrupt Level Status Command



See μINSTR-30.

Jump I/O Command



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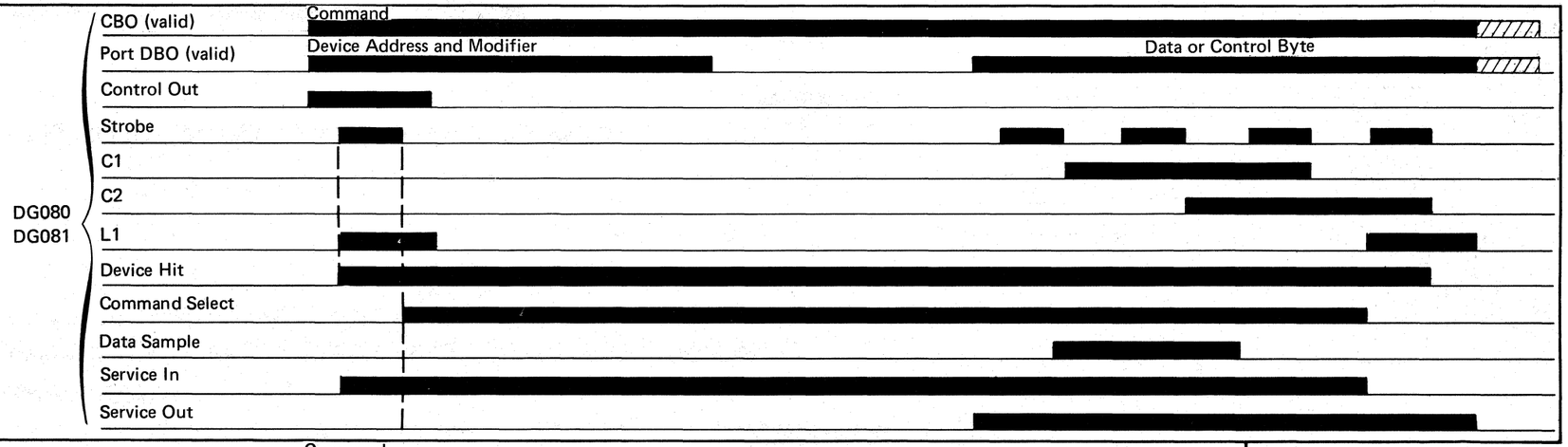
Command Timing Charts

Load Command—Control Load Command

The purpose of this command is:

1. Start a seek operation, write operation, or a read operation.
2. Transfer a data byte to the attachment.
3. Perform CE (diagnostic) functions.

This timing chart shows the sequence of events for the load command—control load command. See DISK-11.



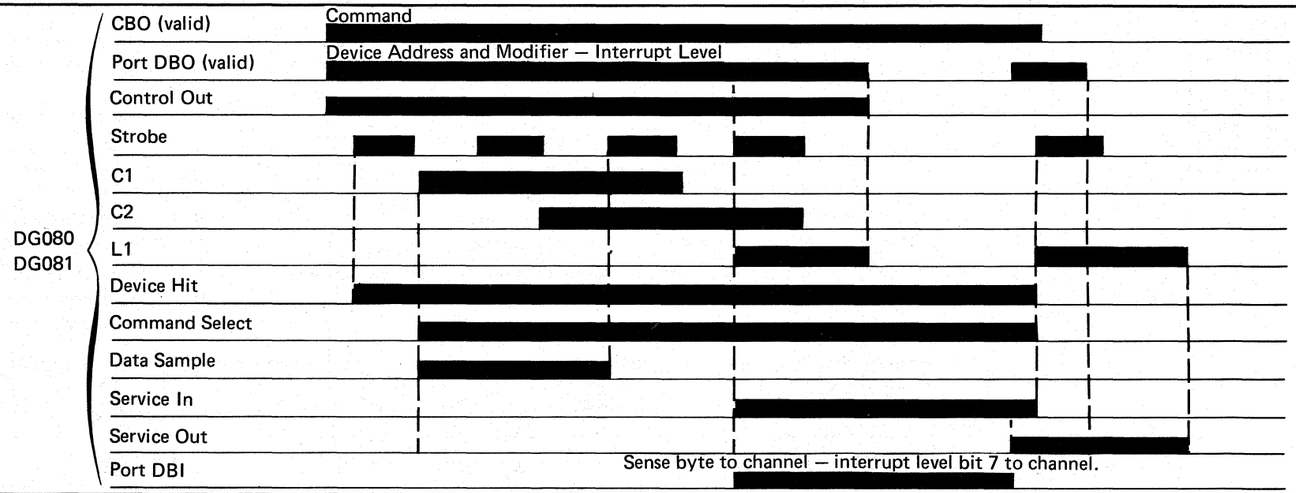
Sense Command—Control Sense Command

The purpose of this command is to transfer a data byte, an error byte, a control byte, or a CE (diagnostic) byte from the attachment to the channel. These bytes are called sense bytes and are transferred to the channel on the DBI.

Sense Interrupt Level Status Command

This command tests for an interrupt request from the disk attachment. If the disk attachment is requesting an interrupt, DBI bit 7 is activated to the CPU.

The timing chart shows the sequence of events for the sense command—control sense command—sense interrupt level status command. See DISK-13 and DISK-14.



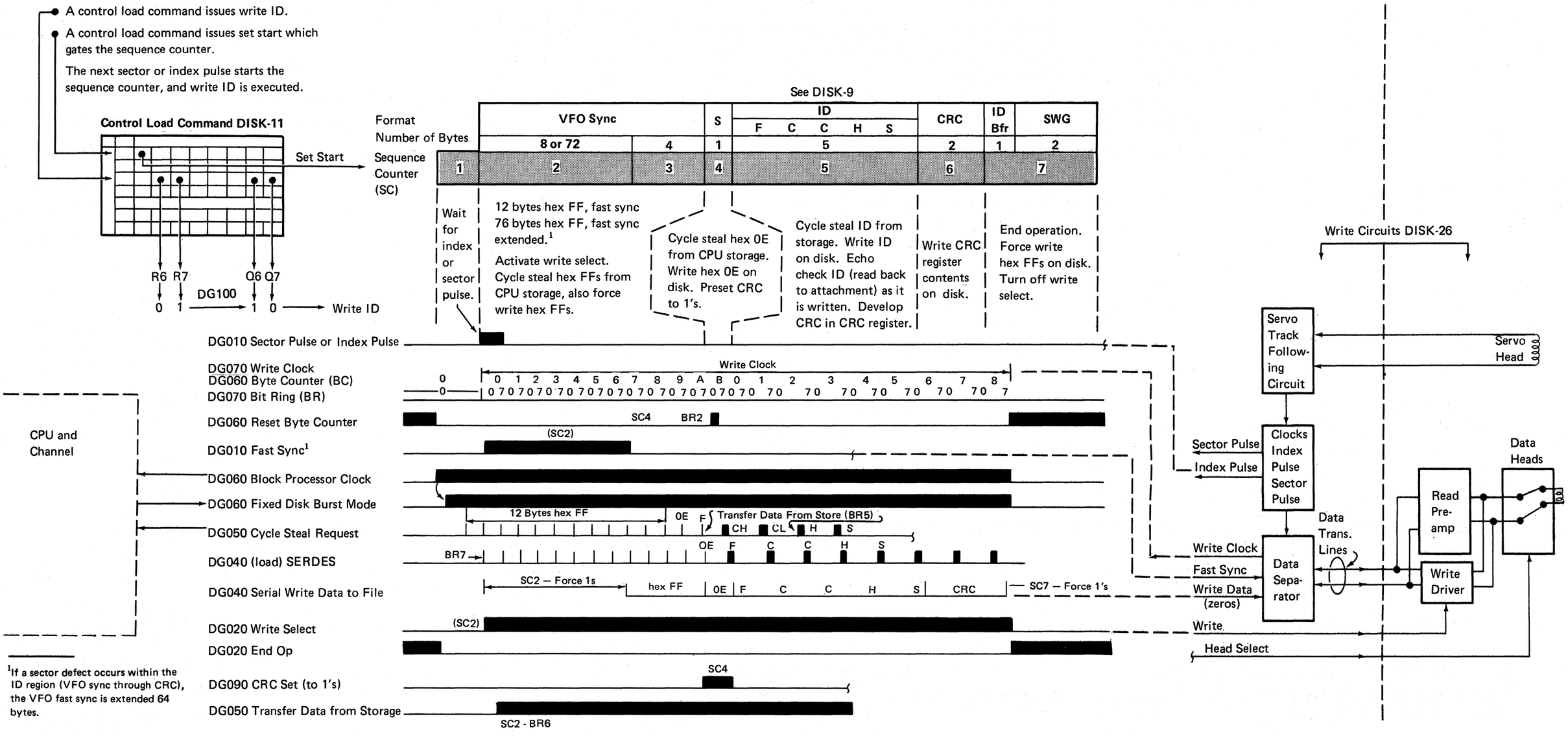
Jump I/O Command

The purpose of this command is to detect error conditions on main attachment and disk drive status conditions. If the condition tested for is present, CBI bit 4 is activated to the channel. If the condition tested for is not present, CBI bit 4 is inactive. See DISK-15.

Write Identifier (ID)

Write ID

The primary use of write ID is to rewrite an ID field when a defective sector has been detected. When a permanent error is encountered for a given sector, its ID field must be rewritten to indicate where the data has been relocated and to flag that sector as being defective.



Read Identifier (ID)

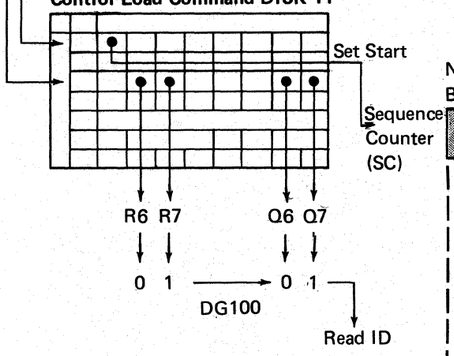
Read ID

The primary use of read ID is to bring the ID field over to the CPU so it can be examined. Normally the ID field is compared in the attachment so the CPU never really gets its contents. But if the ID search never results in a sector hit, the program may want to read the ID field to determine why that particular sector cannot be found. Therefore, read ID transfers the contents of the ID field to the CPU.

- A control load command issues read ID.
- A control load command issues set start which gates the sequence counter.

  The next sector or index pulse starts the sequence counter, and read ID is executed.

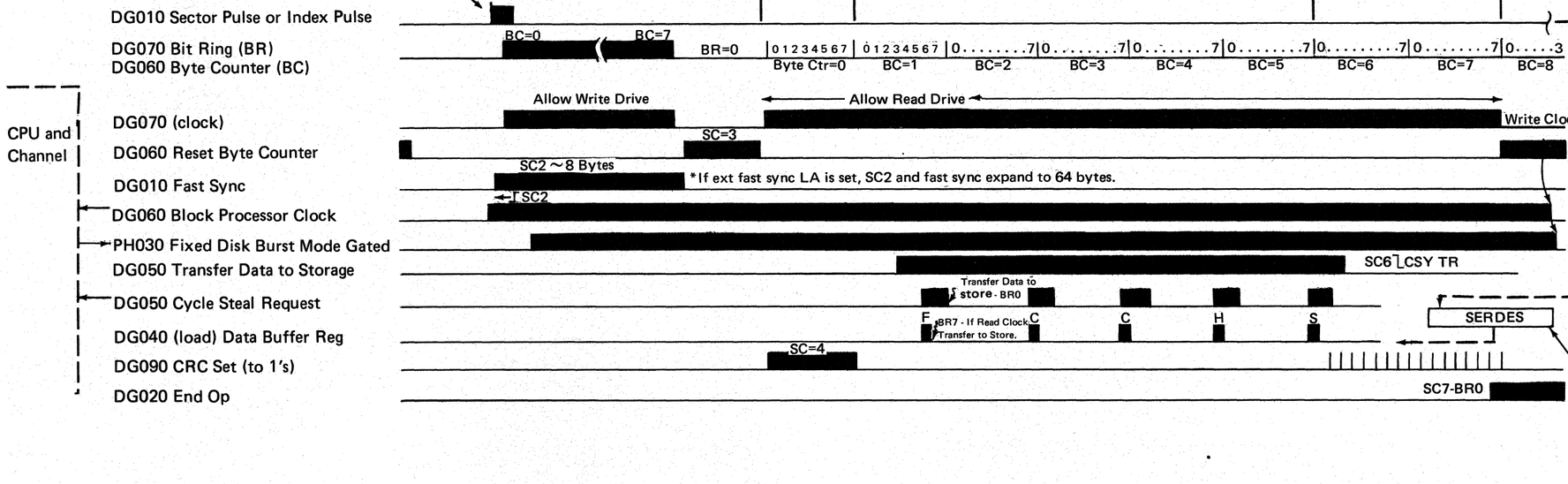
Control Load Command DISK-11

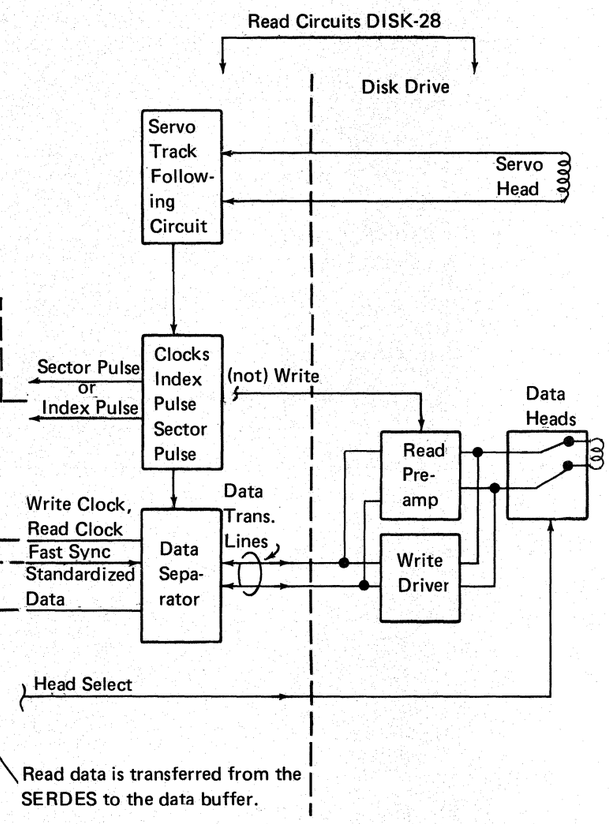


Attachment

See DISK-9.

Format				ID							
Number of Bytes	VFO Sync		S	F	C	C	H	S	CRC	ID Bfr	SWG
	8 or 72	4	1	5					2	1	2
	1	2	3	4	5				6	7	
	Wait for index or sector pulse.	Read from disk searching for hex 0E sync byte.		Detect hex 0E sync byte from disk. Preset CRC reg to 1's.	Read ID from disk. Develop CRC in CRC register. Cycle steal ID into storage.				Read CRC from disk and compare with the CRC register.	End Op	



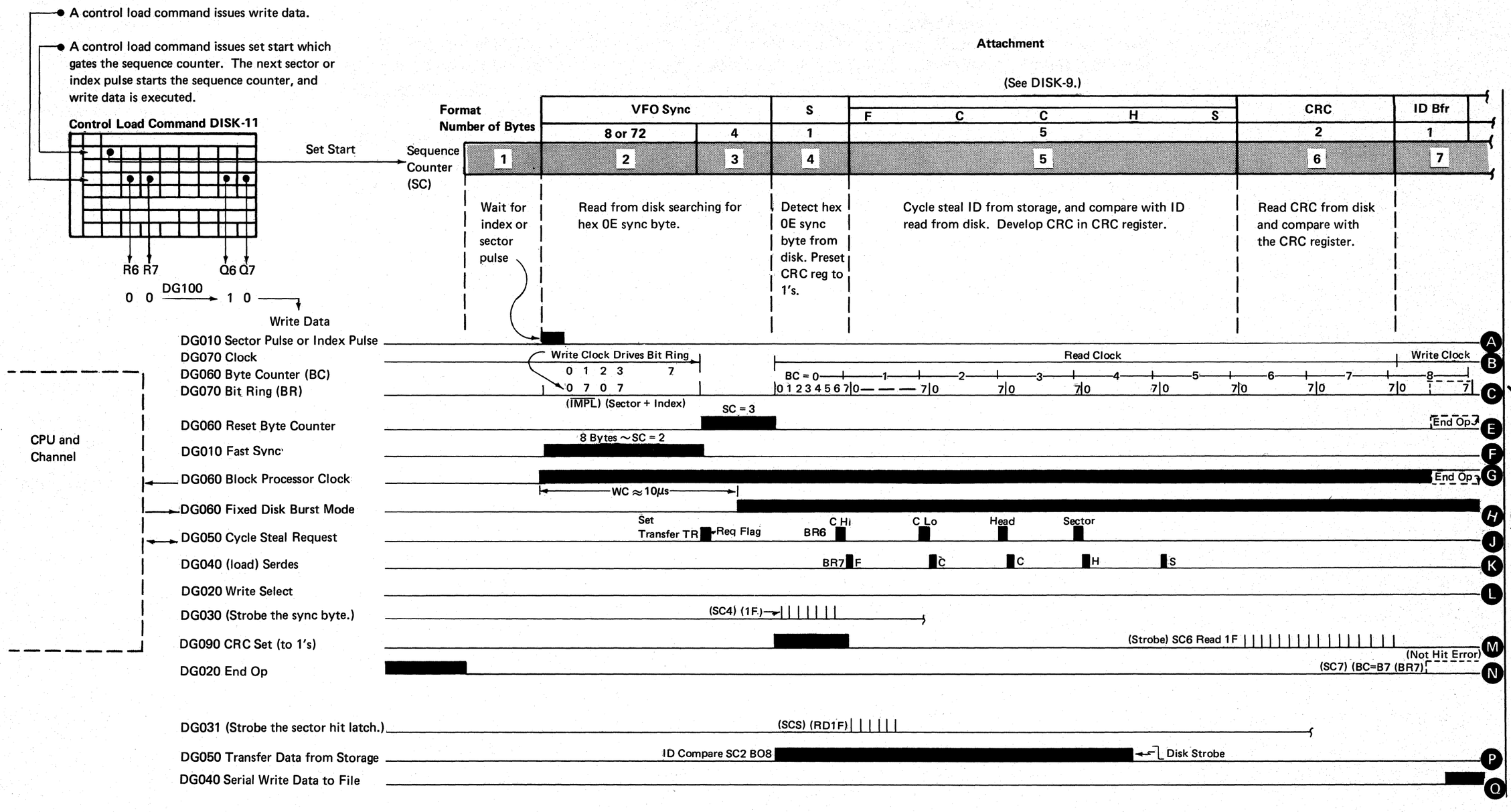


Write Data

Write data transfers 256 bytes of data from CPU storage and writes the 256 bytes into the data field of a sector on the disk.

A control load command issues write data.

A control load command issues set start which gates the sequence counter. The next sector or index pulse starts the sequence counter, and write data is executed.



Write Data (Continued)

Attachment

(See DISK-9.)

SWG	VFO Sync		S	Data	CRC	Res	Bfr	EWG
2	12		1	256	2	3	1	2
7	8	9	10	11	12	13		

Compare hit. Activate write select.

Force write all hex FFs.

Force write hex 0E to disk. Preset CRC to 1's.

Cycle steal data from storage. Write data on disk. Echo check data (read back to attachment) as it is written.

Write CRC register contents onto disk.

Force write hex FFs. Turn off write select end op.

From facing page.

A

B — Write Clock

C — 9 A B C D E F 10 11 12 13 14 15 16 | 0 | 1 | 2 | 255 | 256 | 256+1 | 256+2 | +3 | +4 | +5 | +6 | +7 | +8

E — SC10 - BR2

F — SC8

G

H

J — SC8-BC=12 D0 Transfer from Store BR6 D1 D2 D3 D255

K — D0 D1 D254 D255

L — (SC7) (BC9) (BR3) (Write Data Command)

M — SC 10

N

P — SC10 - BR6 BC255 Disk Cycle Strobe

Q — SC7 + 8 + 9) = Force 1's | SC10 Force 0E | Gate Data From S/D | Gate CRC Data SC12 | (SC13) = Force 1's.

Write Circuits DISK-26

Disk Drive

Servo Track Following Circuit

Servo Head

Sector Pulse

Index Pulse

Clocks Index Pulse Sector Pulse

Data Heads

Read Pre-amp

Data Trans. Lines

Read Clock, Write Clock

Fast Sync

Write Data (zeros)

Data Separator

Write Driver

Write

Head Select

Read Data or Read Diagnostic or Read Verify

Read Data

Read data reads 256 bytes of data from the data field of a sector on the disk, and transfers the 256 bytes of data to CPU storage.

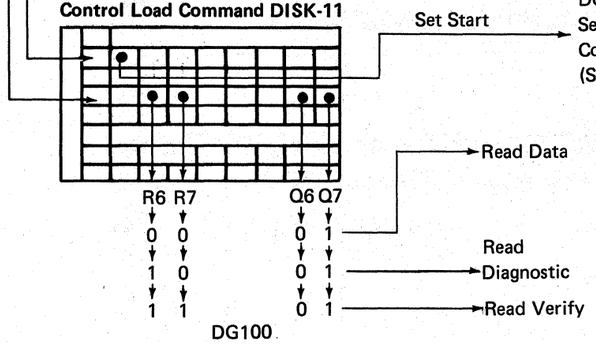
Read Diagnostic

Normally the data field of a particular record can only be read if there has been a sector hit during the ID search. The hit indicates that the record looked for has been found. But if an ID field becomes defective after the data has been written, it is possible that a sector hit during the ID search may not occur. If that is the case, the program can issue read diagnostic, which causes a normal read operation bypassing the ID search. This allows the CPU to recover data that might otherwise be lost if the ID field becomes defective.

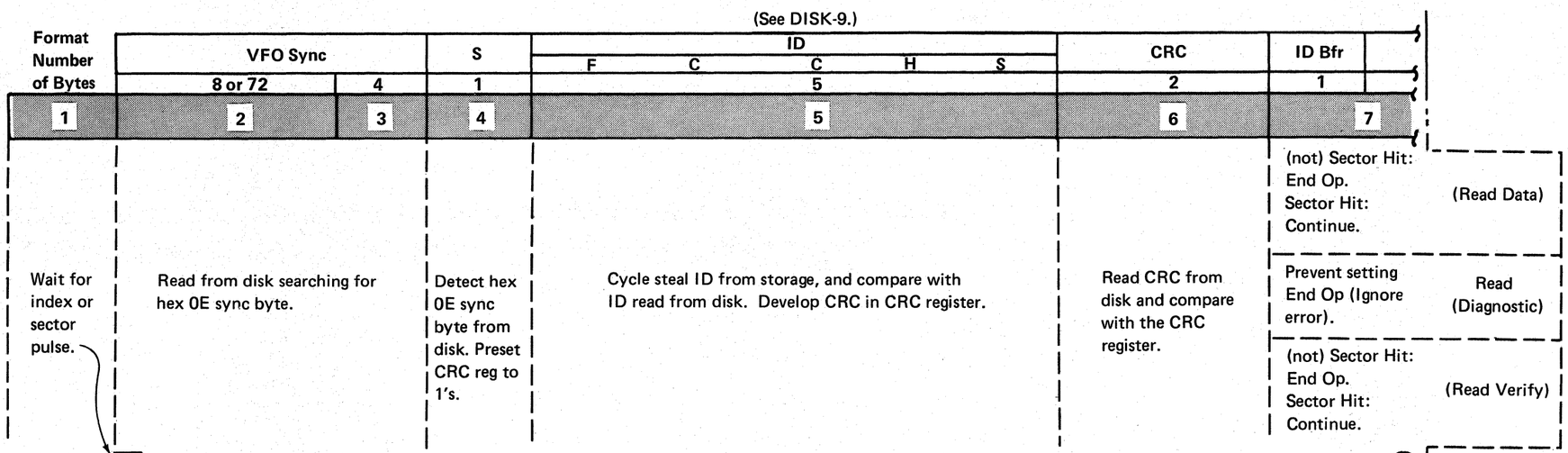
Read Verify

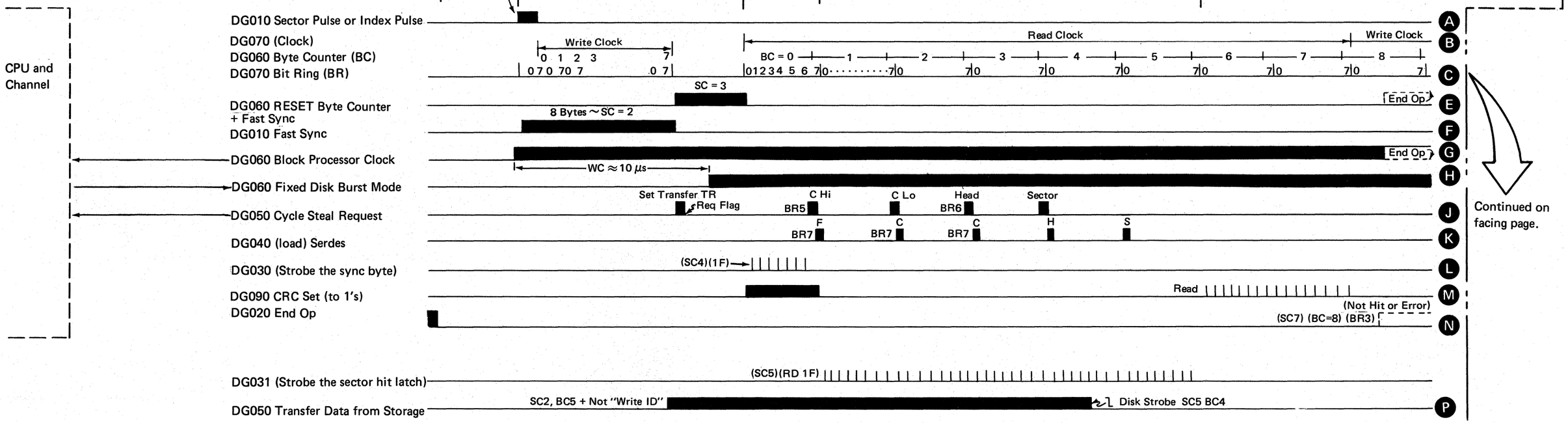
Read verify is used to double check the contents of the data field after it has been written. It simulates read data as far as the disk is concerned, but no data is transferred to the CPU. As the record is read, it is creating a CRC character and if there is no CRC check following the reading of the entire record, read verify is completed.

- A control load command issues read data or read diagnostic or read verify.
- A control load command issues set start which gates the sequence counter: the next sector or index pulse starts the sequence counter, and read data or read diagnostic or read verify is executed.



Attachment (See DISK-9.)





Continued on facing page.

Read Data, Read Diagnostic or Read Verify (Continued)

Attachment

(See DISK-9.)

SWG	VFO Sync		S	Data	CRC	RES	Bfr	EWG
2	12		1	256	2	3	1	2
7	8	9	10	11	12	13		

Read from disk, searching for hex 0E sync byte.

Read hex 0E from disk. Preset CRC to 1's.

(Read Data)

(Read Diagnostic)

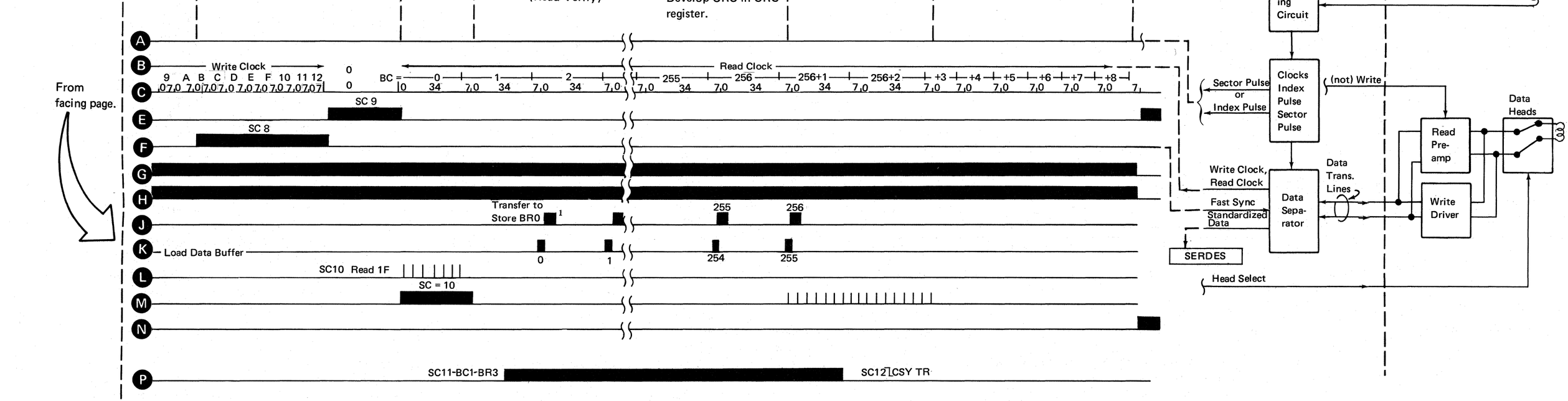
Read data from disk. Cycle steal data into storage. Develop CRC in CRC register.

(Read Verify)[1]

Read data from disk. Develop CRC in CRC register.

Read CRC from disk and compare with CRC register.

Read hex FFs from disk. End Op.



From facing page.

[1] During read verify at sequence counter time, cycle steals are not requested.

Scan Data

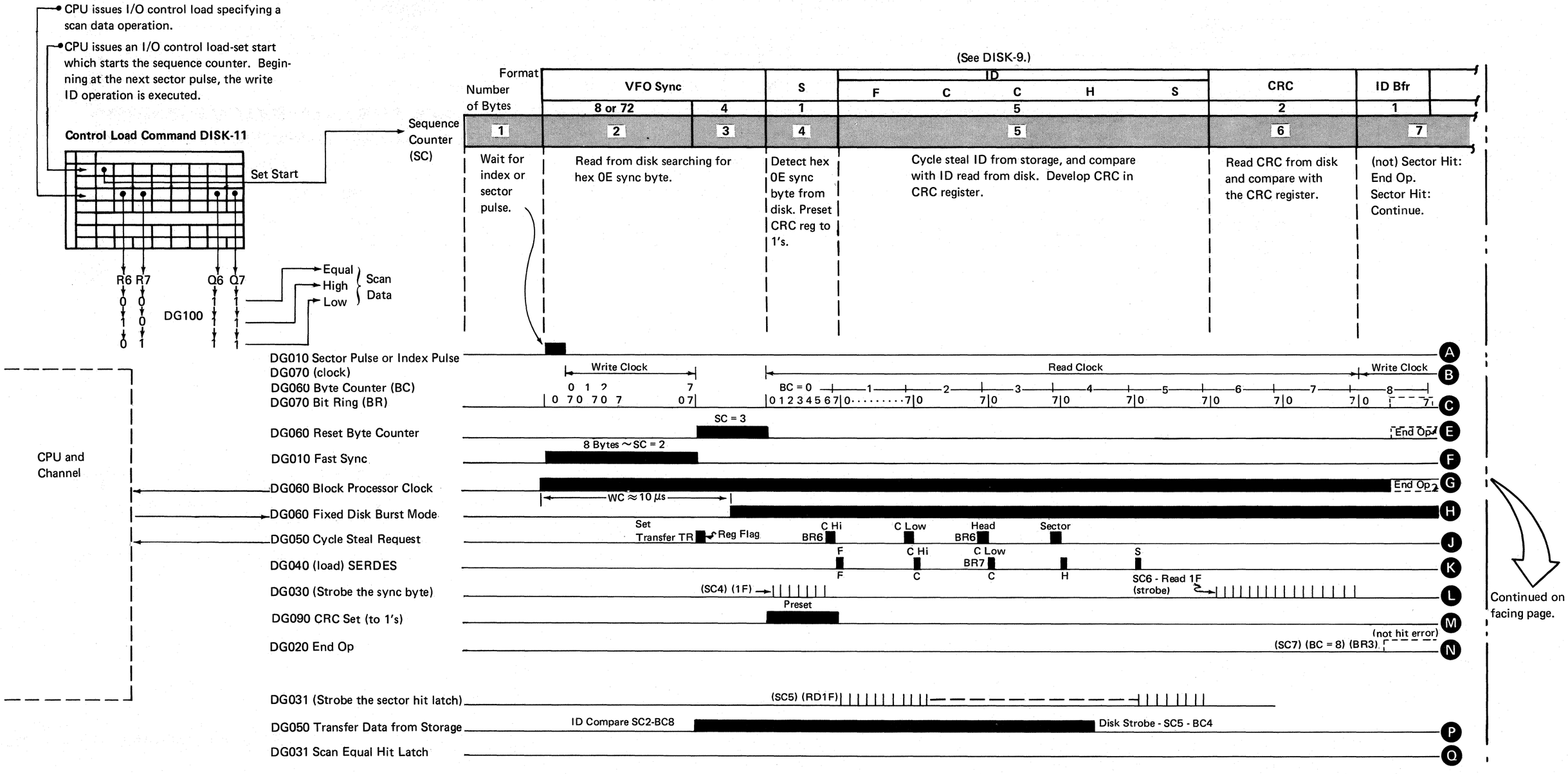
CPU issues I/O control load specifying a scan data operation.

CPU issues an I/O control load-set start which starts the sequence counter. Beginning at the next sector pulse, the scan operation is executed.

Scan Data, Hi or Low, or Equal

The contents of all or portions of the disk data field can be compared to a fixed data field in the CPU and the results indicated as being high or low or equal.

The result of this operation is simply an indication of the comparison with neither the data on the disk or in the CPU being changed in any way.



Continued on facing page.

Scan Data (Continued)

Attachment

(See DISK-9.)

SWG.	VFO Sync		S	Data	CRC	Res	Bfr	EWG
2	12		1	256	2	3	1	2
7	8	9	10	11	12	13		

Read from disk, searching for hex 0E sync byte.

Read hex 0E from disk. Preset CRC to 1's.

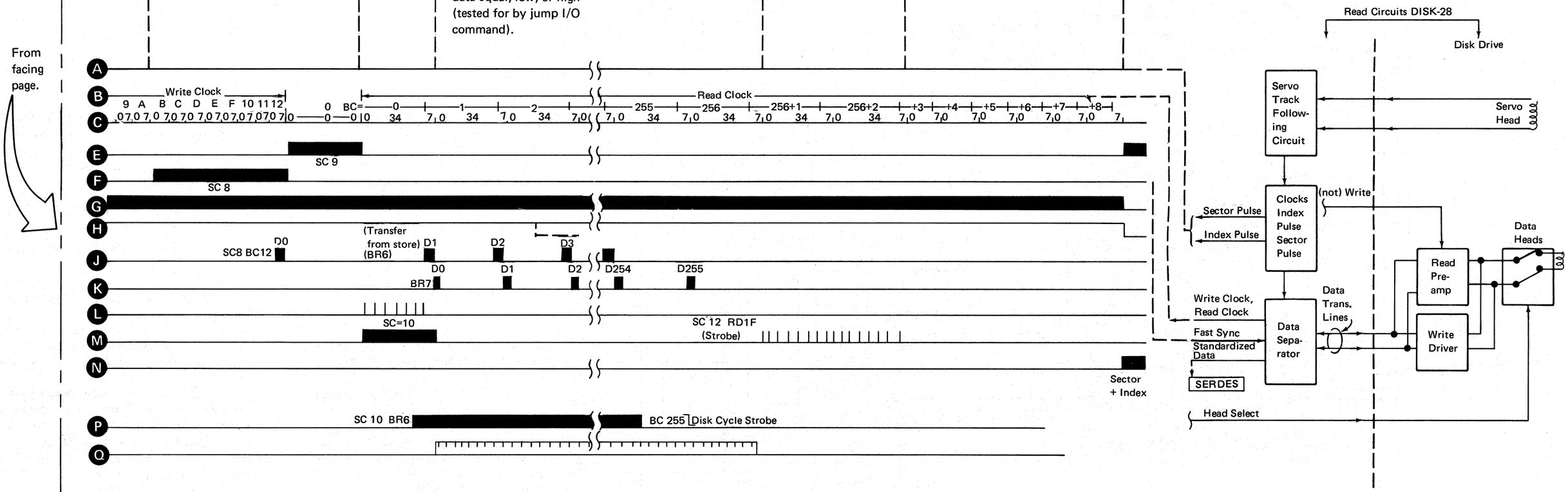
Compare data read from storage with data read from disk. Scan hit disk data equal, low, or high (tested for by jump I/O command).

Develop CRC in CRC register.

Read CRC from disk and compare with CRC register.

Read hex FFs from disk. End Op.

From facing page.



DISK

Write

Write zeros (data bits) is gated, in the MFM encoder/shift register, by '1F write clock' pulses to produce coded data. Both leading and trailing edges of the coded data pulses are defined in an edge clocking latch. Coded and defined data is transmitted, via the line driver and receiver, to the write data trigger.

Write gate sets the write data trigger and the data is transmitted to the write drivers.

Modified Frequency Modulation (MFM)

MFM is the form in which data is recorded on the data tracks.

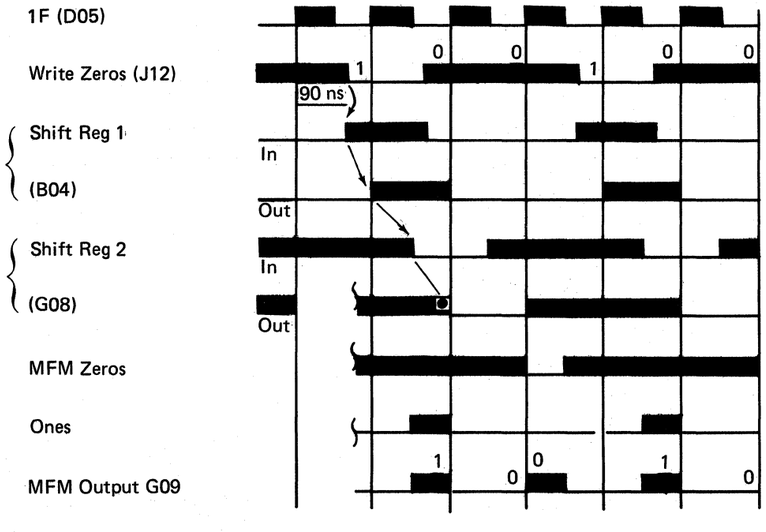
Data is transmitted on the write zeros line; when the line is positive, a 1 is indicated and when the line is negative, a 0 is indicated.

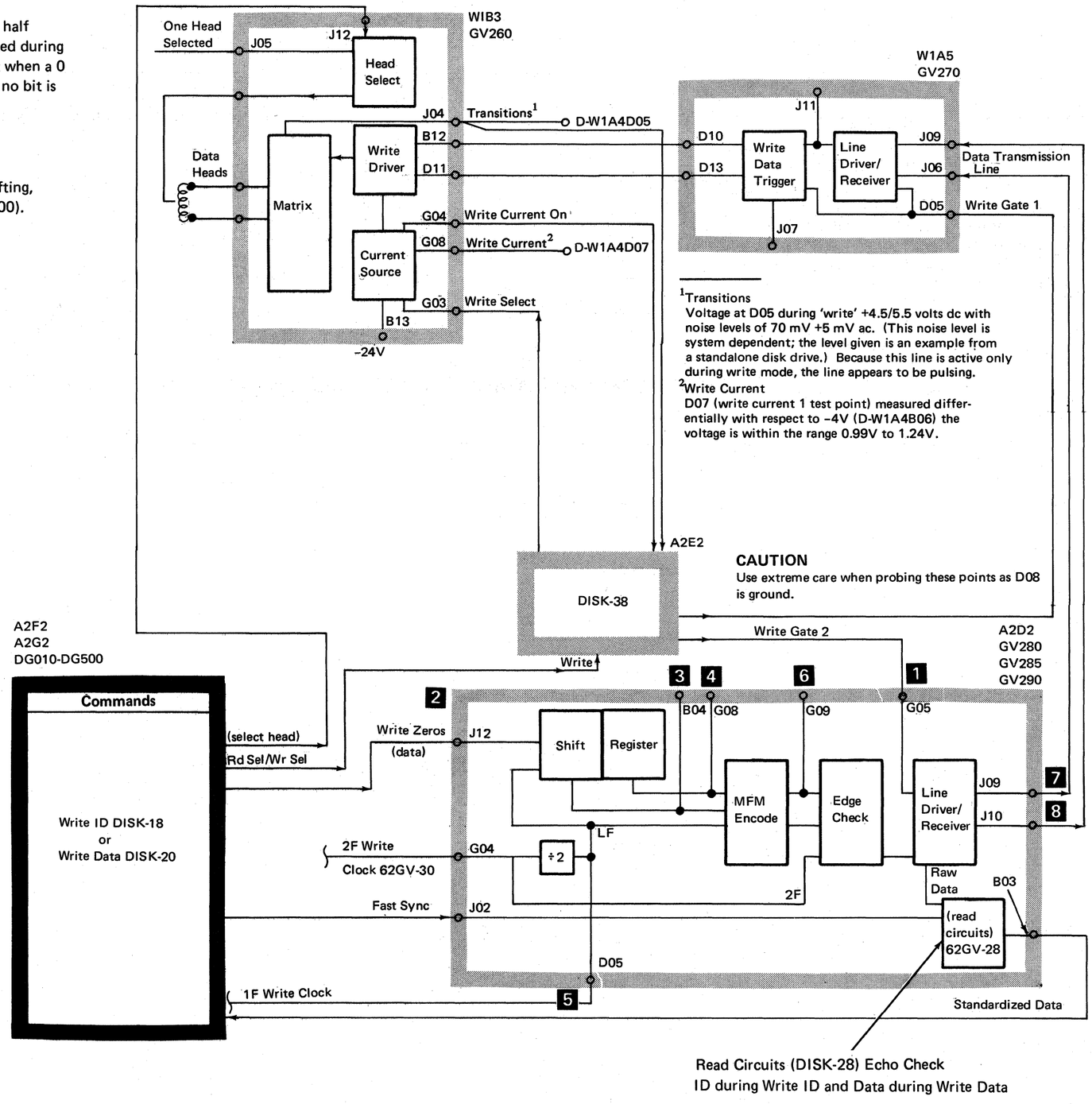
A two stage shift register and the MFM encoder shift the data bits by one 1F clock cycle.

A 1 bit is transmitted during the second half of a 1F clock cycle. A 0 bit is transmitted during the first half of a 1F clock cycle, except when a 0 immediately follows a 1 bit, in this case no bit is transmitted during the 1F clock cycle.

MFM Encoding

The diagram below shows the input, shifting, and encoding and writing of data (100100).





Write ID and Write Data Wave Forms

All wave forms use write gate—A2D2G05 as a sync point, with a times 10 grounded probe. The amplitude of signals may vary from one machine to another. Two scope signals are shown on one picture in order to:

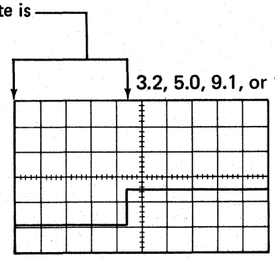
- Show opposite polarities of signals.
- Save space on page.

Write ID

Pictures taken while running Friend test using the following commands and options:

Write ID
Sector 0
Select head 0
Restore original control field
Loop on table

This wave form shows write gate. Write gate is active once during a write ID command.



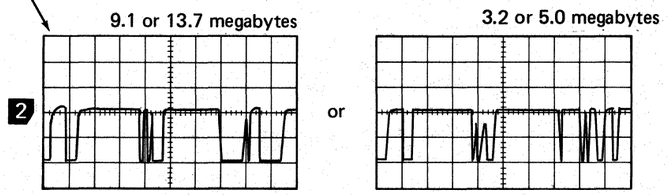
Chan 1 Write Gate D2G05
Sync Internal - Write Gate D2G05

Voltage: 0.1 V/div
Time: 5.0 μs/div
DC Input

Dial the delay time multiplier to zero, then slowly advance the multiplier to get this picture.

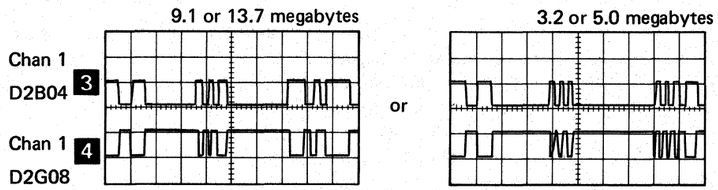
Chan 1 Write Zeros D2J12
Sync External - Write Gate D2G05

Voltage: 0.2 V/div
Time: Main sweep 20 μs/div
Delayed sweep 1.0 μs/div
DC Input



Sync External - Write Gate G05

Voltage: 0.1 V/div
Time: Main sweep 20 μs/div
Delayed sweep 1.0 μs/div
DC Input



Write Data

All of these wave forms of hex A were taken while writing hex A's while looping on the Friend test.

9.1 or 13.7 megabytes, track 302 (hex 012E), sector 0, head 0.
5.0 megabytes, track 168 (hex 00A8), sector 0, head 0.
3.2 megabytes, track 108 (hex 006C), sector 0, head 0.

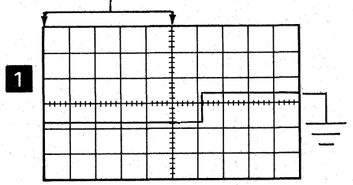
Pictures taken while running Friend test using the following commands and options:

Write data
Sector 0
Select head 0
M/S data field 1
Loop on table
Set/dump data fields
Preset M/S data field 1
Enter hex AAAAs

This wave form shows write gate. Write gate is active once during a write data command.

Chan 1 Write Gate D2G05
Sync Internal - Write Gate D2G05

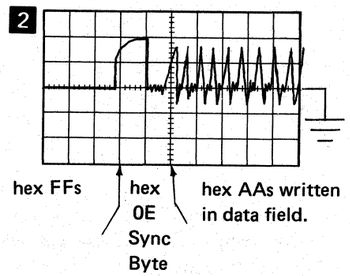
Voltage: 0.1 V/div
Time: 50 μs/div
DC Input

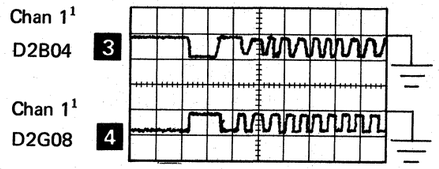


Dial the delay time multiplier to zero, then slowly advance the multiplier to get this picture..

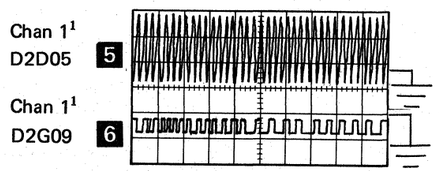
Chan 1 Write Zeros D2J12
Sync External - Write Gate D2G05

Voltage: 0.2 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input

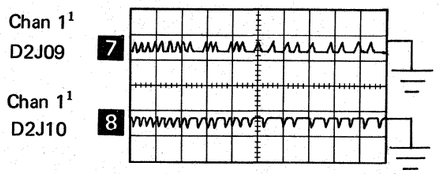




Sync External - Write Gate D2G05
Voltage: 0.1 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input



Sync External - Write Gate D2G05
Voltage: 0.1 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input



Sync External - Write Gate D2G05
Voltage: 0.1 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input

[1]Two wave forms shown on one picture.

Read

Read Circuits

When 'read select' and 'head select' from the attachment are activated, raw data is read from the disk and preamplified.

The raw data is amplified by a variable gain amplifier and filtered. Raw data signals are clipped and detected before being differentiated, squared, gated by the read gate, and fed into a line receiver. The detected raw data signal is integrated and fed back to control the variable gain amplifier.

Read Clock and Divide-by-Two Counter

The data separator card receives the raw data and feeds it into a line driver/receiver. The read clock, which runs at 14.22 MHz, is synchronized to the incoming data (see *Fast Sync* on this page).

The basic clock runs at twice bit cell frequency (2F) and is locked to the average phase of all the incoming bits. The clock is halved to produce the 1F clock (bit cell frequency) and from then on, the 1F clock is in phase with the bit cell.

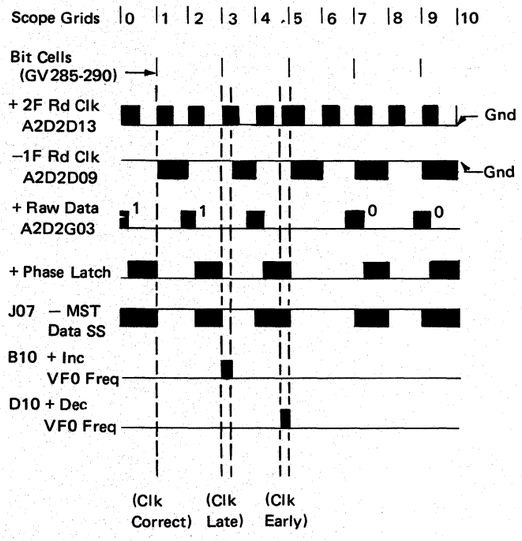
Phase and frequency synchronization is maintained by a phase-locked loop to the read clock.

Read Clock Control

To lower the frequency of the clock (that is, delay the phase), the control voltage is reduced. To raise the clock frequency, the control voltage is increased. Thus, to keep the clock locked to the data stream, the positive current source is turned on if the clock is behind phase with the data and the negative source is turned on if it runs in advance of the data.

Data/Read Clock Sync

Current control is obtained from the data early and data late pulses that are logically derived from the data. The data early and data late pulses derived from the data, control the read clock as follows: Each data bit sets the data SS and the phase latch whose output is compared (see *Timings* on the next page). This detects either early date, or late data (in respect to the read clock 2F). Therefore, if data is late, the frequency of the read clock is decreased; if data is early the frequency of the read clock is increased.



Data Latch and Standardized Data Latch

Input to the data latch comes from the 2F clock, 1F clock and the phase latch. The phase latch activates the standardized data latch. The standardized data (read data) is then gated to the SERDES.

Fast Sync

Fast sync is activated during the execution of all commands. For example, if a read ID command (62GV 19) is initiated, the VFO field of 1's (hex FF) is the first field read from disk. Fast sync is activated at the beginning of this field. After fast sync falls, the next VFO sync field bit causes the read clock to sync to these 1's. This must be done because the read clock cannot distinguish between 1's or 0's. Therefore, by synchronizing the read clock to known 1's, the read clock detects 1's and 0's properly for the remainder of the record (read ID command).

[1]Left floating, so always active.

Read ID and Read Data Wave Forms

All wave forms use the index pulse—A2E2D13 as a sync point, with a times 10 grounded probe. A scope hood may be needed to see signals. The amplitude of signals may vary from one machine to another. Two scope signals are shown on one picture in order to:

- Show opposite polarities of signals.
- Save space on this page.

Read ID

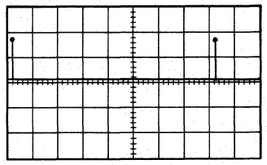
9.1 or 13.7 megabytes, track 302 (hex 012E), sector 0, head 0.
5.0 megabytes, track 168 (hex 00A8), sector 0, head 0.
3.2 megabytes, track 108 (hex 006C), sector 0, head 0.

Wave forms shown while running Friend test, scope loop option, read ID from CE Track (head 0, sector 0).

12 5.0, 9.1, or 13.7 megabytes

Chan 1 Fast Sync D2J02
Sync + Internal Chan 1

Voltage: 0.2 V/div
Time: 5.0 ms/div
AC Input

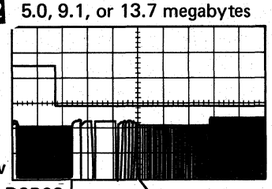


12 5.0, 9.1, or 13.7 megabytes

Chan 1 Fast Sync D2J02
Sync + Internal Chan 1

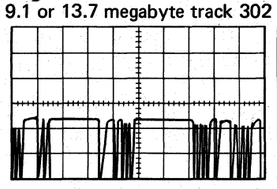
Voltage: 0.2 V/div
Time: Main Sweep 5.0 μs/div
Delayed Sweep 1 μs/div
Chan 2 Standardized Data D2B03

10

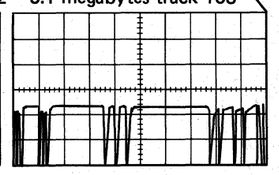


This portion delayed

9.1 or 13.7 megabyte track 302



5.1 megabytes track 168

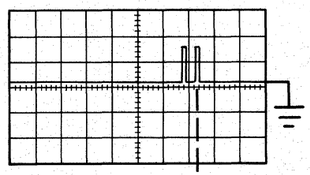


Read Data

All of these wave forms of hex A were taken while looping on the Friend test and reading from the CE track (head 0, hex sector 1E). Before these wave forms are scoped, all hex A's must be written (on the CE track) by using the Friend test. See DISK-27.

This wave form shows fast sync. Fast sync is active twice during a read data command (see DISK-22).

12

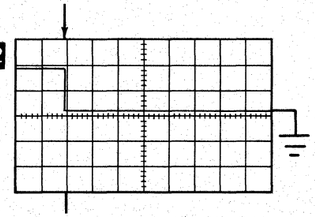


Chan 1 Fast Sync D2J02
Sync + Index Pulse E2D13

Voltage: 0.2 V/div
Time: 50 μs/div
DC Input

Last 4 μs of second fast sync pulse shown using delayed sweep.

12

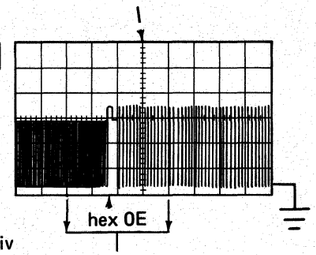


Chan 1 Fast Sync D2J02
Sync + Index Pulse E2D13

Voltage: 0.2 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 2 μs/div
DC Input

Fast sync shown in relationship to standardized data.

10



Chan 1 Standardized Data D2B03
Sync + Index Pulse E2D13

Voltage: 0.2 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 2 μs/div
DC Input

hex 0E

Standardized Data (expanded) Move hex 0E to left before expanding.

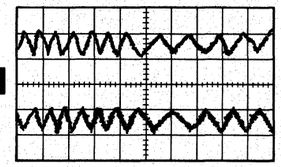
[1]May need card extender.

Chan 1[1] W1A4D04

Chan 1[1] W1A4D02
Sync + Index Pulse E2D13

Voltage: 20 mv/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
AC Input

1

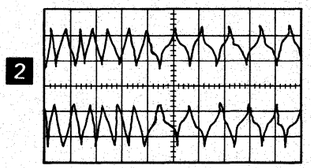


Chan 1[1] W1A4D13

Chan 1[1] W1A4B10
Sync + Index Pulse E2D13

Voltage: 50 mv/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
AC Input

2



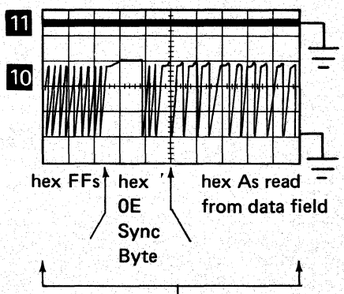
Chan 1 Error Voltage D2J13

11

10

Chan 1 Standardized Data D2B03
Sync + Index Pulse E2D13

Voltage: 0.2 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input



hex FFs | hex 0E Sync Byte | hex As read from data field

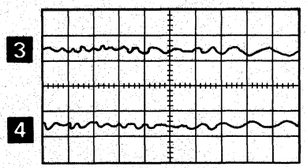
Chan 1[1] W1A4B12

3

Chan 1[1] W1A4D11
Sync + Index Pulse E2D13

4

Voltage: 5 mv/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
AC Input

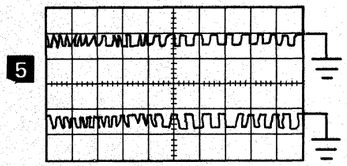


Chan 1[1] A2D2J09

5

Chan 1[1] A2D2J10
Sync + Index Pulse E2D13

Voltage: 0.1 Vcm
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input



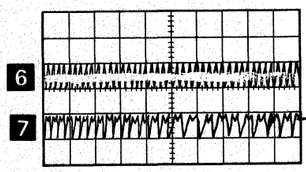
Chan 1 D2D13

6

Chan 1 D2J07
Sync + Index Pulse E2D13

7

Voltage: 0.1 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input



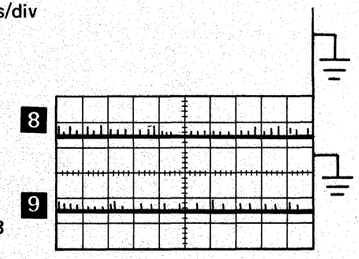
Chan 1 D2B10

8

Chan 1 D2D10
Sync + Index Pulse E2D13

9

Voltage: 0.1 V/div
Time: Main Sweep 50 μs/div
Delayed Sweep 0.5 μs/div
DC Input



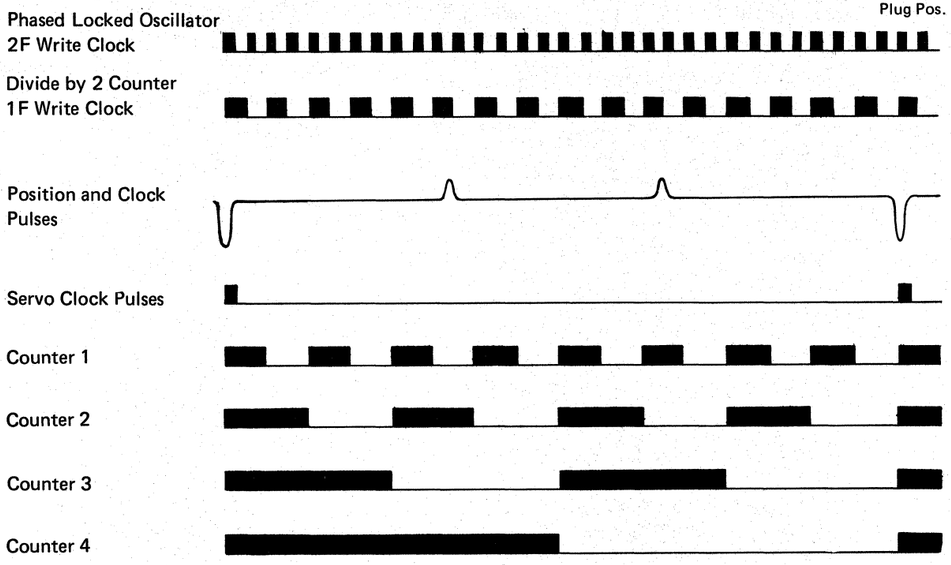
Track Following

Track following aligns the access heads on the track at the completion of each seek operation and maintains head/track alignment during read and write operations.

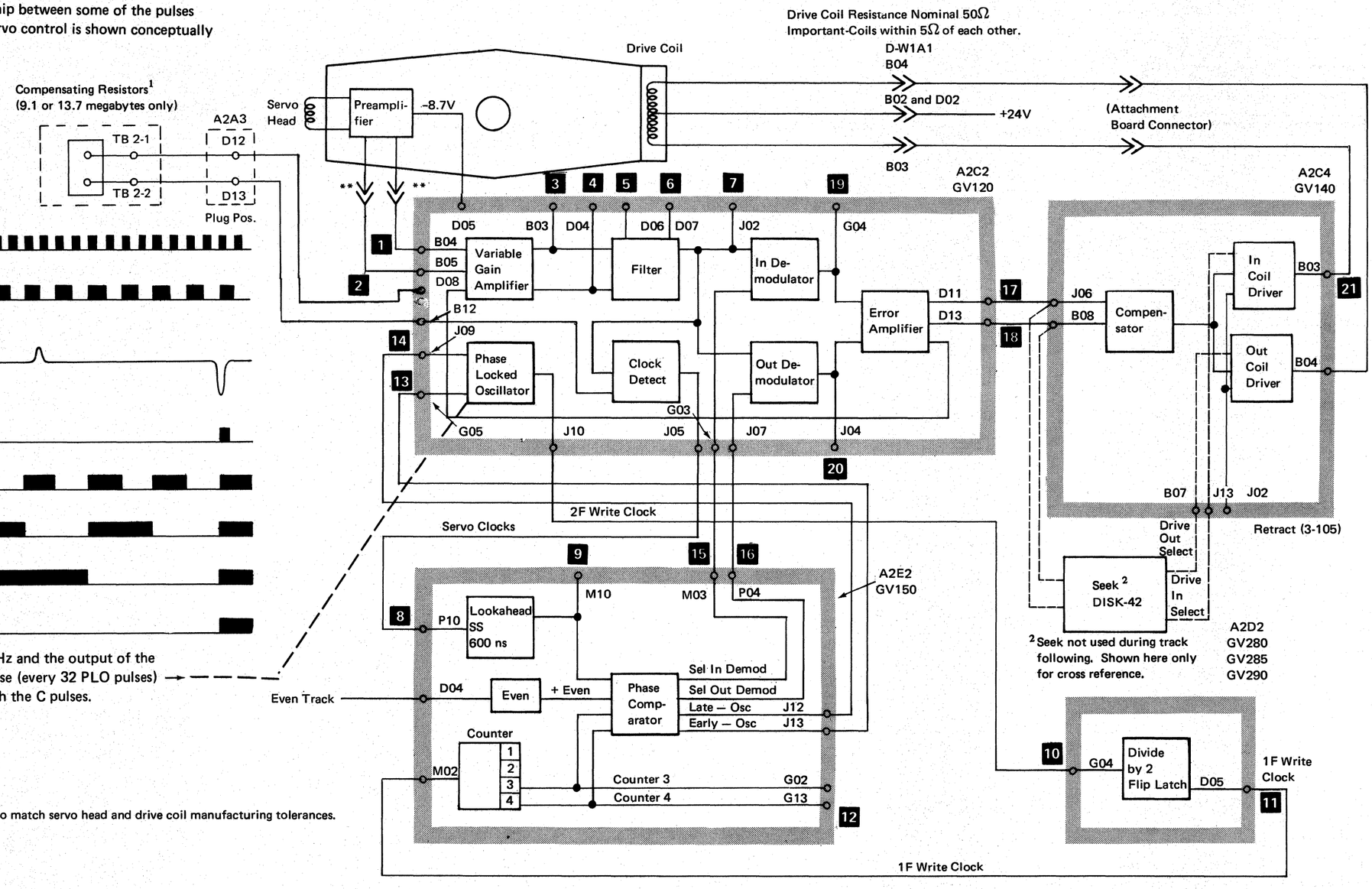
The servo head reads a prewritten pattern that is aligned with each data track. The prewritten pattern is made up of position pulses (P1 and P2) and servo clock pulses (C) repeated around each servo track.

Sequences of missing clock pulses identify the index point, the start of each sector, and the tracks in the data area of the disk (see DISK-34).

The relationship between some of the pulses used in the servo control is shown conceptually below.



The phased locked oscillator (PLO), operates at a frequency of 14.2 MHz and the output of the 'divide by 2 counter' has a frequency of 7.1 kHz. The 'servo clocks' pulse (every 32 PLO pulses) is used as a reference to keep the 1F write clock in synchronization with the C pulses.



[1] Factory selection of the resistors is required to match servo head and drive coil manufacturing tolerances.

Track Following Operation

The servo track signal is amplified, filtered, and separated into two component signals (clock pulses and position pulses). These signals are then detected on the position detection and PLO analog card A2C2. If no servo clock pulses can be detected, see DISK-33.

On the control and safety card, (A2E2) each detected servo clock pulse fires a 600 ns singleshot called the lookahead singleshot. This singleshot allows a phase comparison between the servo clock and the frequency divided write clock to be performed.

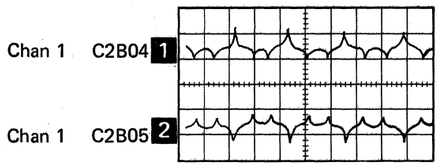
The phase locked oscillator (PLO), the main component of the PLO loop, is controlled by the 'oscillate early' and 'oscillate late' signals. The PLO runs at 14.2 MHz. The output frequency, the '2F write clock' (A2C2J10), is divided by two to provide the '1F write clock' (7.1 MHz). The '1F write clock' is further divided by 16 in a four-stage counter to provide 'select in demod' and 'select out demod'. These demodulator gates are synchronized with the servo pattern and switched so that one position pulse is gated to the 'in demodulator' and the other is gated to the 'out demodulator'. The polarity of even track (up for even and down for odd) is used to define which position pulse is gated to which demodulator ('select in' or 'select out').

When the polarity of the line is defined, it maintains this state until the next seek is initiated; this allows the error signal to be used to keep the head on the desired polarity and therefore the desired track. The position pulses, which produce the differential error signal, are peak detected on the position detection card and their sum is returned on the 'automatic gain control' (AGC) line to control the variable gain amplifier.

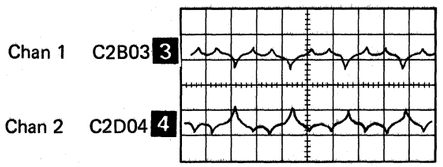
The differential error signals are formed into a single signal in the compensator and combined with current sense signals from the drive transistors to power one or other of the coil drivers. The coil drivers move the actuator in the required direction to correct the position of the servo head over the selected track.

Track Following Waveforms

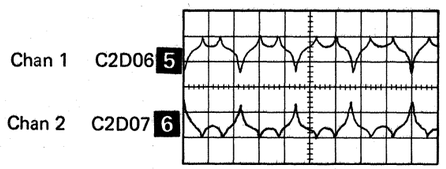
The following waveforms are obtainable if the servo operation is functioning correctly and the head is positioned on a track. *All pictures were taken with a times 10 probe.*



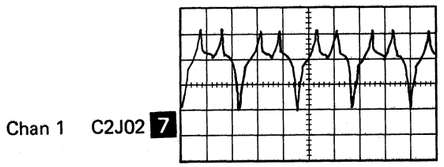
Voltage: 10 mV/div
Time: 1 μs/div
Trigger: External + E2P11 - Sector Pulse
AC Input



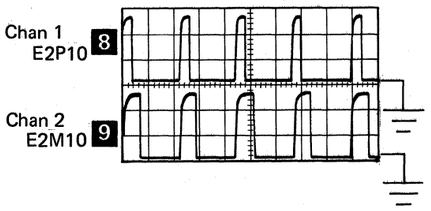
Voltage: 10 mV/div
Time: 1 μs/div
Trigger: External + E2P11, Chopped
AC Input



Voltage: 20 mV/div
Time: 1 μs/div
Trigger: External + E2P11, Chopped
AC Input

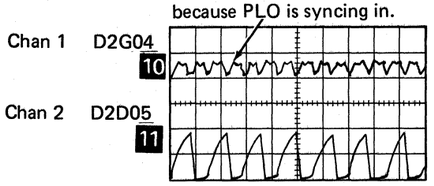


Voltage: 0.1 0V/div
Time: 1 μs/div
Trigger: External + E2P11, Chopped
AC Input

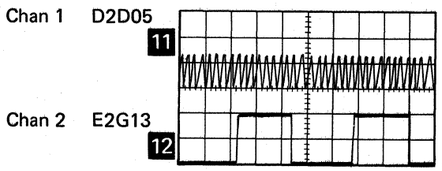


Voltage: 0.2 V/div
Time: 1.0 μs/div
Trigger: External + E2P11, Chopped
DC Input

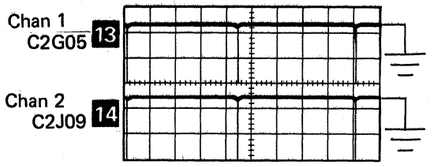
May be distorted at beginning because PLO is syncing in.



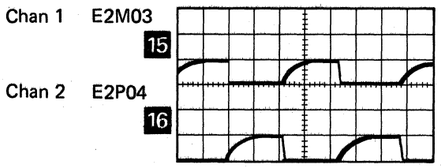
Voltage: 0.2 V/div
Time: 0.1 μs/div
Trigger: External + E2P11, Chopped
AC Input



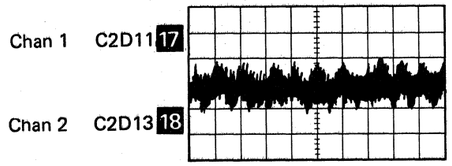
Voltage: 0.2 V/div
Time: 0.5 μs/div
Trigger: External + E2P11, Chopped
AC Input



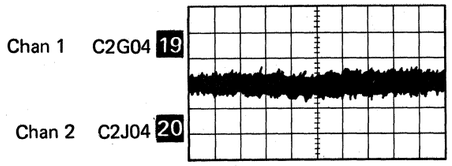
Voltage: 0.2 V/div
Time: 0.5 μs/div
Trigger: Internal + Channel 1, Chopped
AC Input



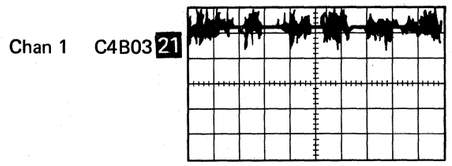
Voltage: 0.5 V/div
Time: 0.5 μs/div
Trigger: Internal + Channel 1, Chopped
AC Input



Voltage: 5 mV/div
Time: 2 ms/div
Trigger: Internal + Channel 1
Vertical Mode: Add, Invert chan 2
Signal is inverted and therefore differential.



Voltage: 10 mV/div
Time: 0.2 ms/div
Trigger: Internal + chan 1
Vertical Mode: Add, Invert + chan 2
Signal is inverted and therefore differential.



Voltage: 1 V/div
Time: 1 ms/div
Trigger: External + D4J13 - Speed Transducer

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Simulated Servo Test Procedure

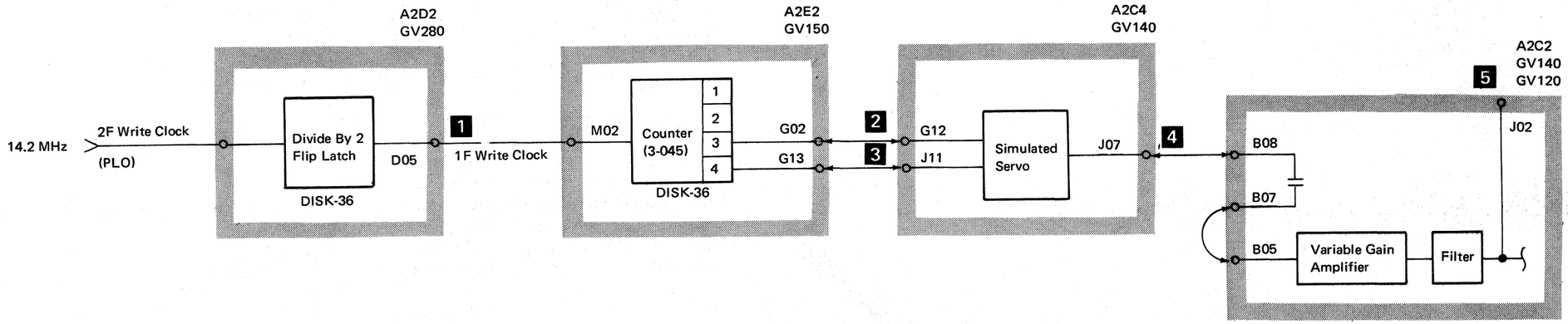
The simulated servo generates an accurate on-track signal for use in finding fault conditions when the servo is not operating correctly.

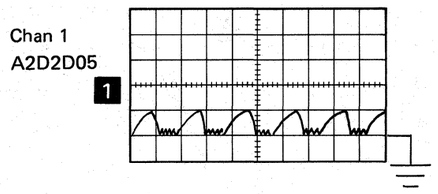
The simulated servo is operating correctly if the illustrated signals are obtained on the oscilloscope when probing the pins shown.

The simulated servo is installed by unplugging the paddle card at D W1B1 and installing seven jumpers on the 01A2 board. The jumpers are:

(A2C2) B05 to (A2C2) B07
(A2E2) G02 to (A2C4) G12
(A2E2) G13 to (A2C4) J11
(A2D4) D09 to (A2D4) D08 (ground)
(A2E2) S09 to (A2E2) D08 (ground)
(A2E2) P09 to (A2E2) P08 (ground)

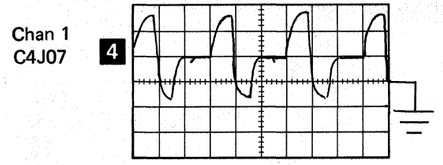
Use pin extender to probe jumpered lines.



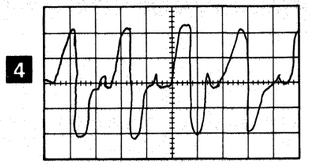


Voltage: 0.5 V/div
Time: 0.1 μs/div
Trigger: Internal channel 1 AC +
DC Input

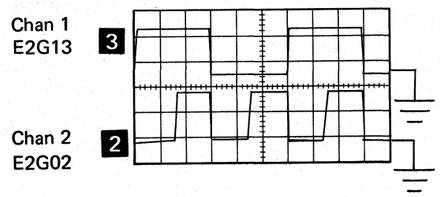
9.1 or 13.7 megabytes



3.2 or 5.0 megabytes

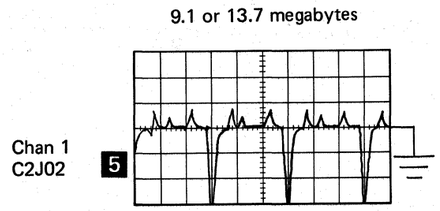


Voltage: 0.1 V/div
Time: 1 μs/div
Trigger: Internal channel 1 AC +
DC Input

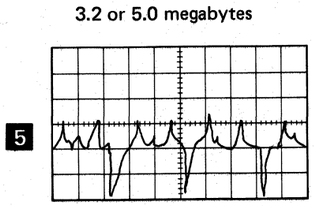


Voltage: 0.5 V/div
Time: 0.5 μs/div
Trigger: Internal channel 1 AC +
DC Input

9.1 or 13.7 megabytes

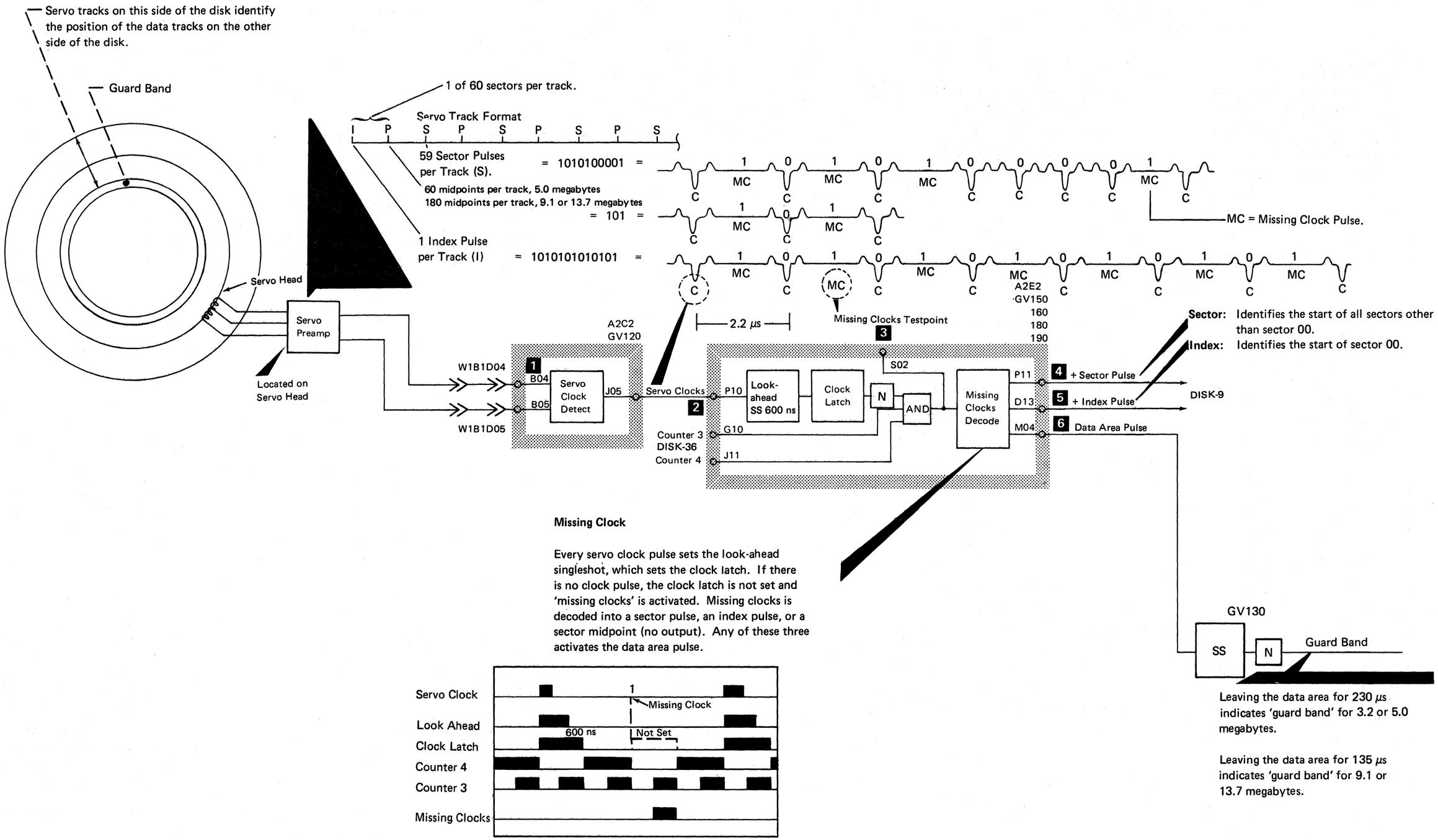


3.2 or 5.0 megabytes



Voltage: 0.1 V/div
Time: 1 μs/div
Trigger: Internal channel 1 AC +
DC Input

Servo, Index and Sector Pulse, Data Area and Guard Band Detection



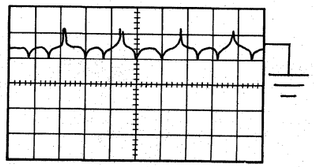
Missing Clock

Every servo clock pulse sets the look-ahead singleshot, which sets the clock latch. If there is no clock pulse, the clock latch is not set and 'missing clocks' is activated. Missing clocks is decoded into a sector pulse, an index pulse, or a sector midpoint (no output). Any of these three activates the data area pulse.

Index and Sector Pulse and Data Area Wave Forms

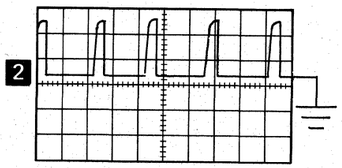
All pictures taken with a times 10 probe.

Chan 1
C2B04 1



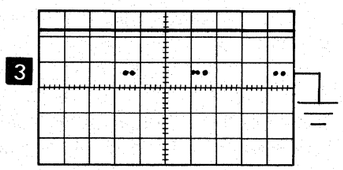
Voltage: 10 mV/div
Time: 1 μs/div
Trigger: External + E2P11 Sector Pulse
DC Input

Chan 1
E2P10 2



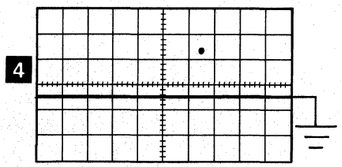
Voltage: 0.20 V/div
Time: 1.0 μs/div
Trigger: External + E2P11 Sector Pulse
DC Input

Chan 1
E2S02 3



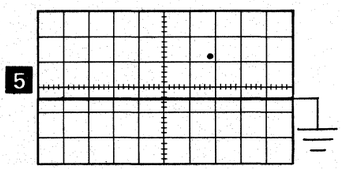
Voltage: 0.2 0V/div
Time: 50 μs/div
Trigger: External + E2D13
DC Input

Chan 1
E2P11 4



Voltage: 0.2 0V/div
Time: 50 μs/div
Trigger: External + E2P11
DC Input

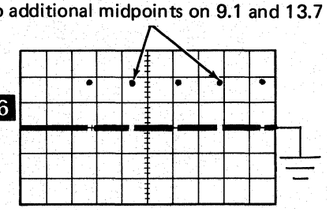
Chan 1
E2D13 5



Voltage: 50 mV/div
Time: 50 μs/div
Trigger: External + E2D13
DC Input

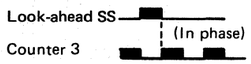
Two additional midpoints on 9.1 and 13.7 megabyte files.

Chan 1
E2M04 6



Phase Locked Oscillator (PLO) Synchronization

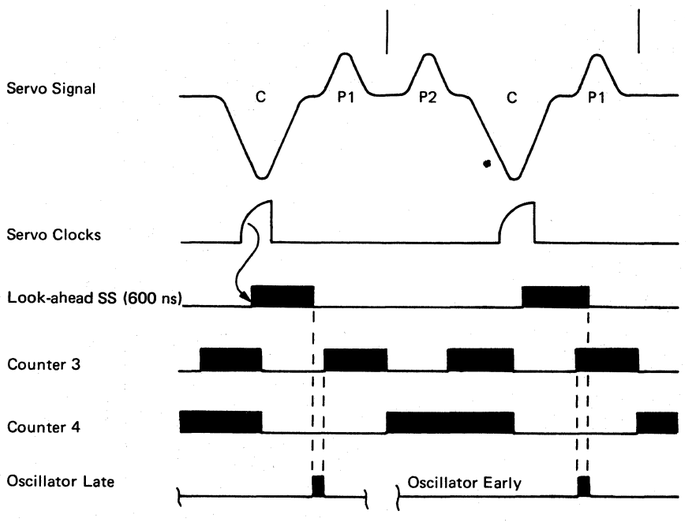
The PLO synchronizes when each 30-second PLO pulse is in phase with the servo clock pulse (DISK-30). This synchronization is indicated when the trailing edge of the look-ahead single-shot is in phase with the leading edge of 'counter 3'.



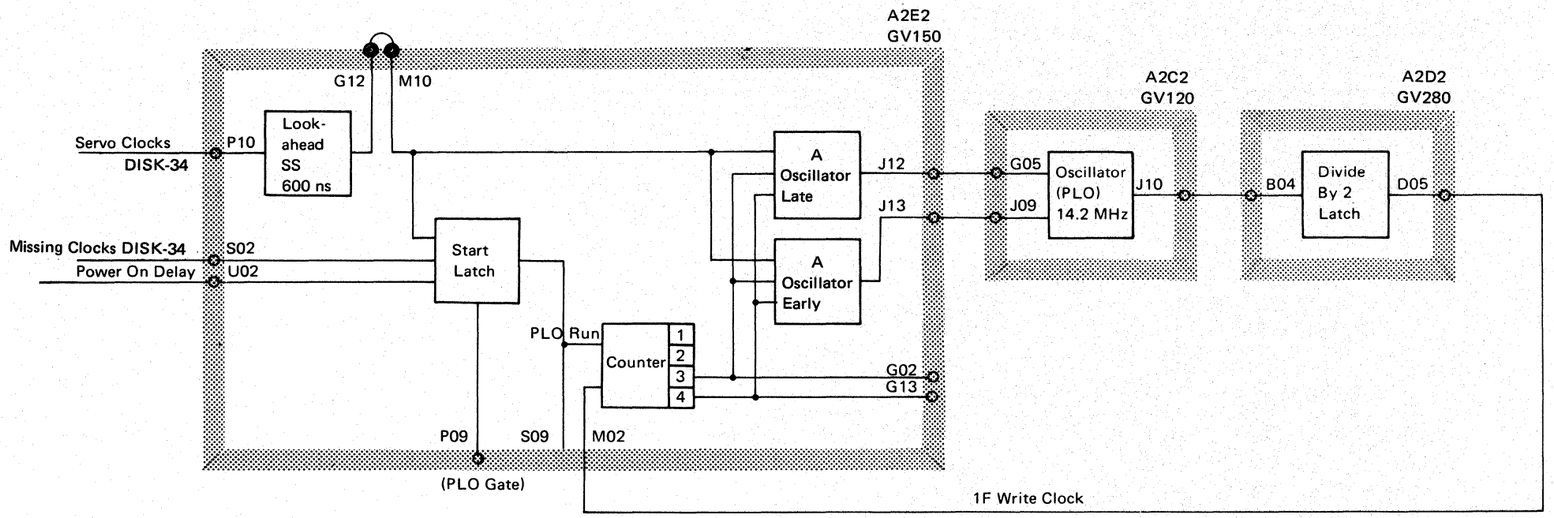
'Counter 3' is directly related to the PLO and the 'look-ahead' singleshot is directly related to the 'servo clocks' pulse.

When the 'look-ahead singleshot' and 'counter 3' are out of time, the difference between them produces an 'oscillator early' or 'oscillator late' pulse. The width of this oscillator pulse is an indication of the difference between the 'look-ahead' single-shot and 'counter 3' pulses. The early and late oscillator pulses are used as an input to adjust the PLO to synchronize with the servo clock pulses.

Relationship of Pulses in the PLO Circuits



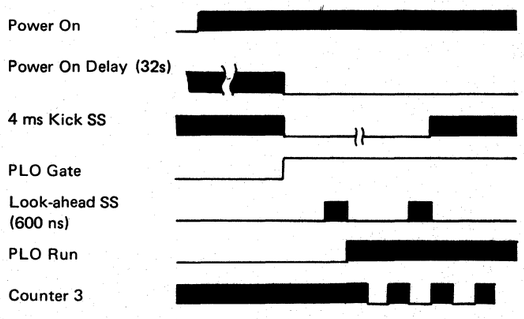
Note: This is a simplified timing diagram. Oscillator late and early pulses do not occur on consecutive servo clock pulses.



Synchronization After Power On

When power is applied to the system, the 'power on delay' line blocks 'PLO gate' until all voltages are established. When the 'power on delay' line drops, the 4ms kick singleshot operates on the access control and moves the heads out and a recalibration operation starts (see DISK-47).

At the same time as the 4 ms kick singleshot operates, the 'PLO gate' is set and synchronization starts. As the access heads move out, the servo head is reading servo clock pulses and synchronization takes place.



PLO Out of Synchronization

Two conditions cause the PLO to be out of synchronization with the servo clocks pulses:

1. Loss of four or more servo clock pulses.
2. A phase error of 90° or more, between the 'look-ahead' singleshot and 'counter 3'.

If the PLO becomes unsychronized during normal operation, both demodulator gates are selected. This forces a zero position error signal to maintain the on track signal.

If the PLO becomes unsynchronized during a write operation, a data unsafe condition occurs.

Recalibrate

The recalibrate operation moves the heads across the tracks to the guard band area (approximately track - 4), then out to settle on track zero (home).

Recalibrate is initiated:

1. When an invalid sector identifier (ID) is read.

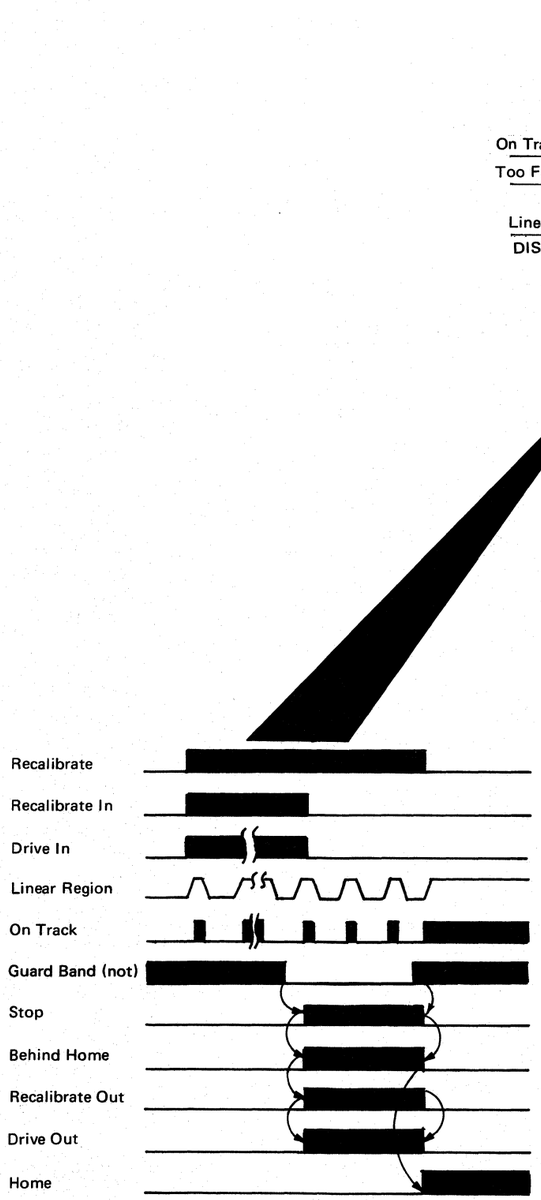
2. After 'data unsafe' is reset.

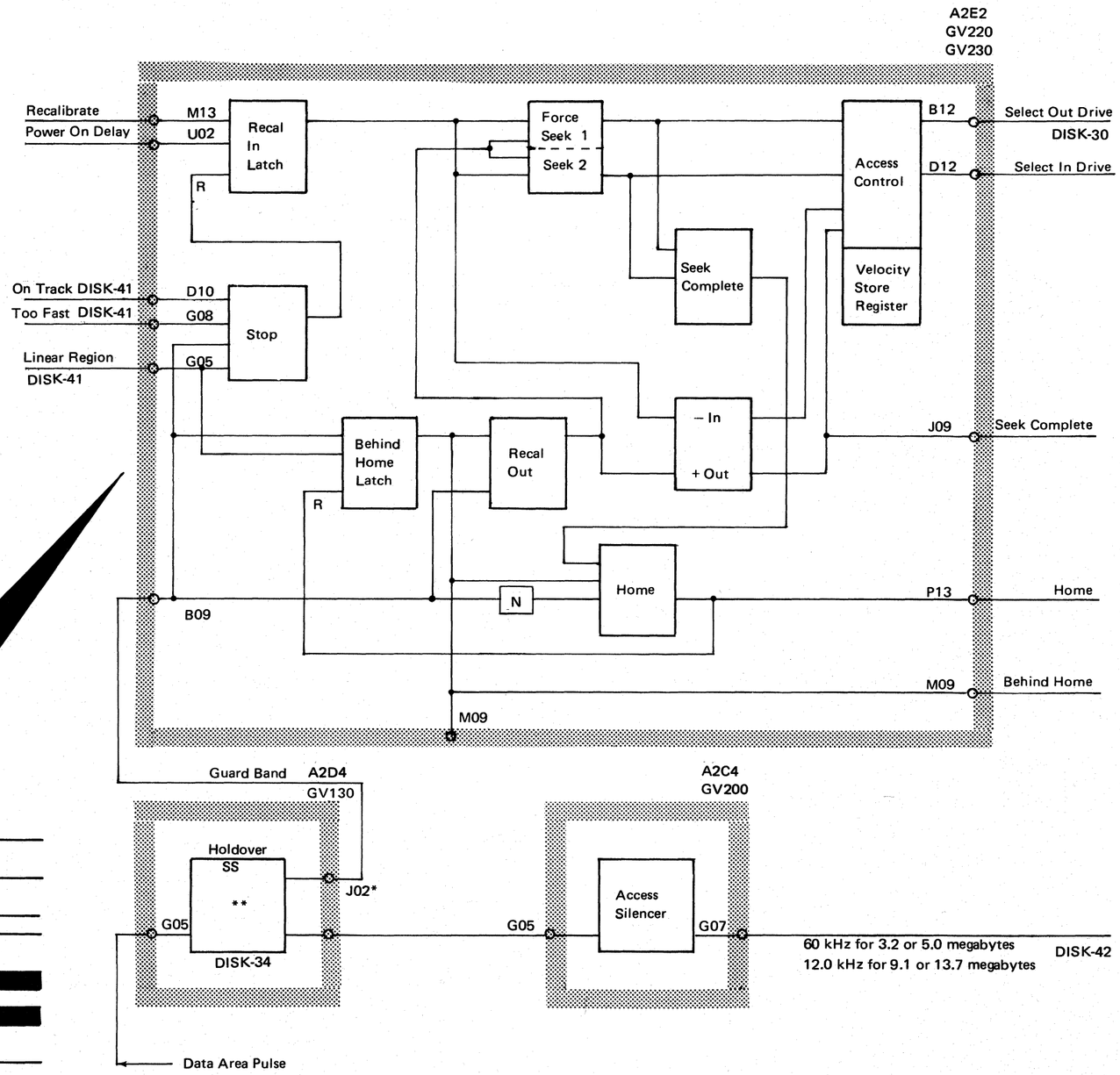
3. During a normal power on sequence.

During recalibration the heads move at low velocity as in a normal 1 or 2 track seek operation.

When the recalibrate line is set, it switches on the 'recalibrate in' latch; 'seek 1 and 2' is forced and 'drive in' is selected. The heads are driven out towards the guard band area. 'Guard band' is active when the heads are behind home; 'guard band' sets the 'behind home' latch, which sets 'recalibrate out', which selects out drive. When 'select out drive' is set, the heads are moved away from the spindle and out of the guard band area. (The two halves of the drive coil always operated in buck/boost.) As the heads move towards track zero, 'guard band' is reset, 'behind home' latch is reset, 'select out drive' is reset and 'home' is set. The heads are then positioned at track zero (home).

In a power on sequence the heads start from behind home. Recalibrate is initiated by 'power on delay' and 'guard band'.





*J02. +5V when heads in data area
0V when heads in guard band.

**270 μs for 3.2 or 5.0 megabytes.
135 μs for 9.1 and 13.7 megabytes.

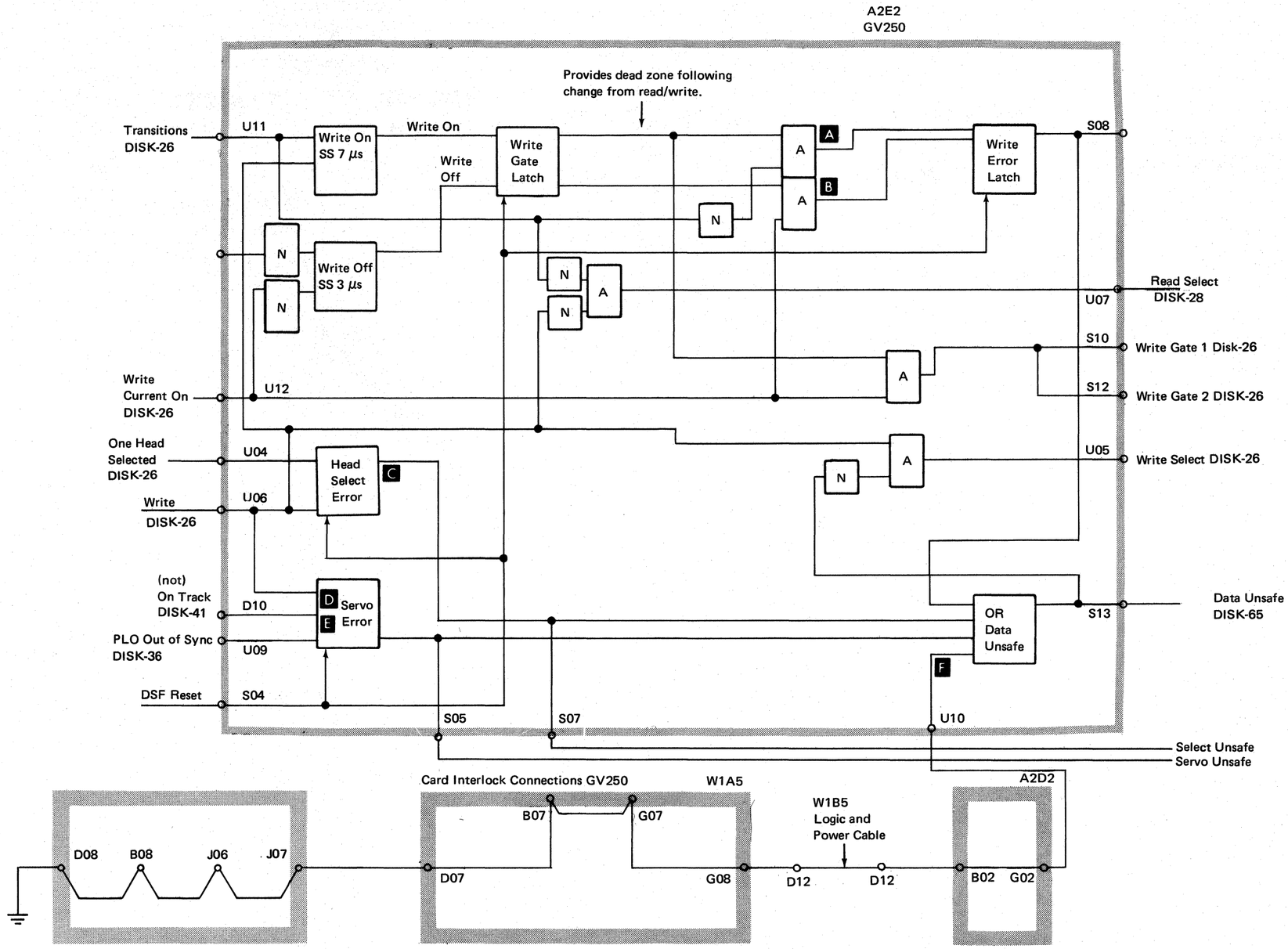
Data Unsafe

When the 'data unsafe' line is active, one or more of the following fault conditions exist:

Fault Condition	Latch
Write selected and no write transitions detected.	Write Error A
Write current source on but not write selected.	Write Error B
Write selected and more than one or no heads selected	Head Select Error C
Write selected and off track detected.	Servo Error D
Write selected and PLO not synchronized.	Servo Error E
Any data channel card incorrectly plugged or seated.	No latch set,but data unsafe indicated F

CAUTION

Continuously pulsing of the 'DSF reset' line to attempt to clear an unsafe condition can cause data to be erased. During 'data unsafe' all read and write operations are inhibited. 'Ready' is dropped and can only be reset by a recalibrate operation after data unsafe is cleared.



DSF (Disk) Ready

DSF (disk) ready is activated when the data heads are at the home (track zero) following a successful power up or recalibrate operation.

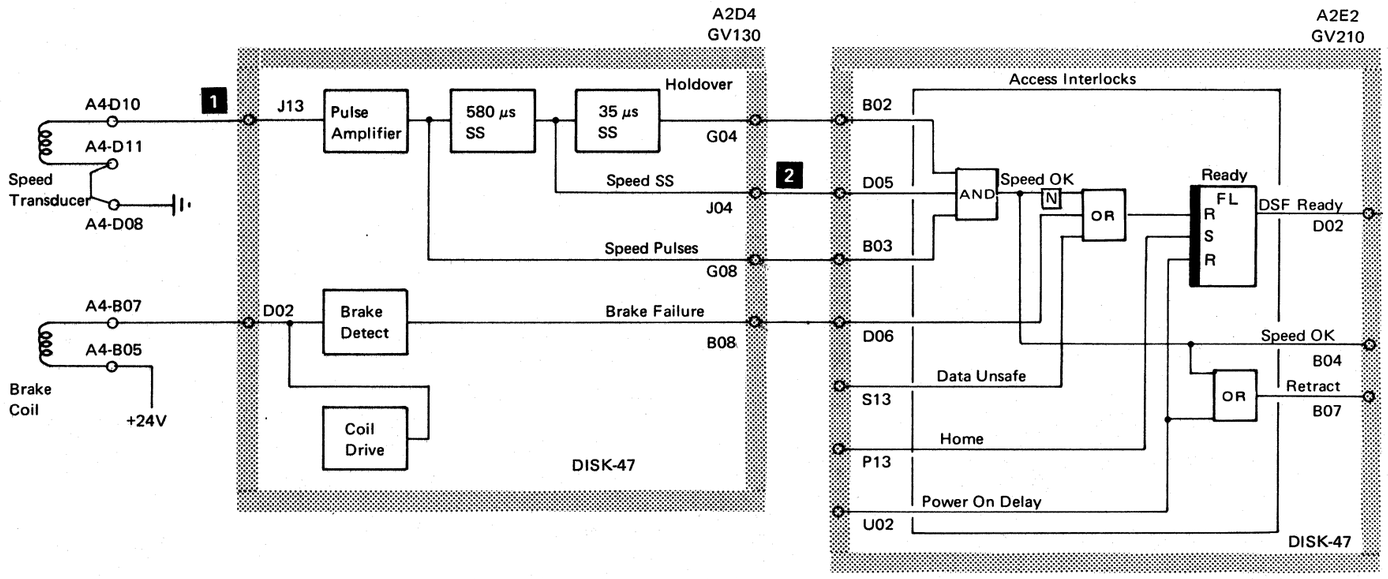
The disk may become not ready or fail to become ready after powering up for the following reasons:

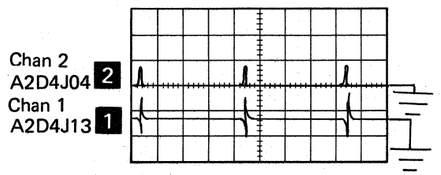
1. A data unsafe condition exists, see DISK-38. 'Data unsafe' indicates that one or more of the three data unsafe latches in the file attachment was set, or that a card is incorrectly plugged or seated.

2. There is an electrical failure of the brake (see DISK-46). A brake failure is indicated if the brake coil becomes open or short circuited. The motor can override the brake, so the attachment removes ac power when there is a brake failure.

3. The disk is not up to the correct speed (see DISK-46). If the disk does not reach the correct speed, the access arm is kept at the inner stop. If the disk loses speed after successfully powering up, the ready indication drops.

Note: The actuator is retracted during power on delay or if the disk speed is too slow.





Voltage: 0.5 V/div
Time: 5.0 ms/div
Trigger: Internal + Channel 1, Chopped
DC Input

Seek Operation

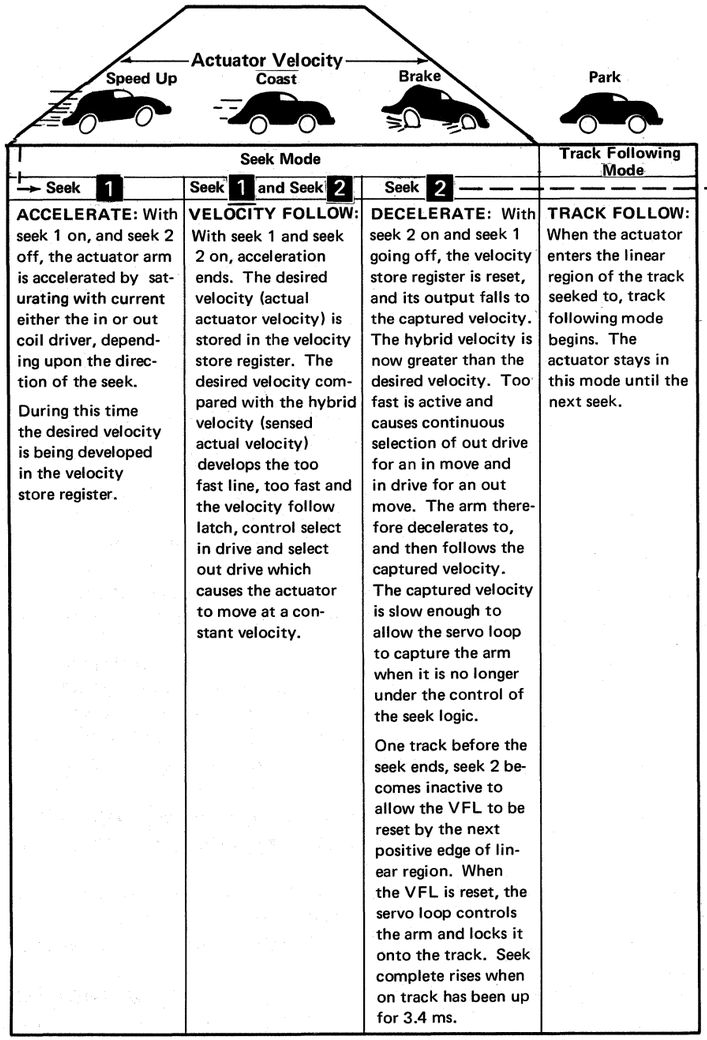
3.2 or 5.0 Megabytes

The 3.2 and 5.0 megabytes seek operations are identical except that when a 3.2 seek operation goes beyond track 108, an invalid seek indication causes an adapter check.

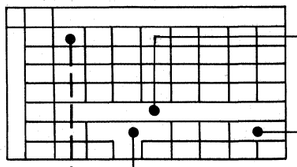
Seek operations move the actuator heads (that is, servo head, data head 0, and data head 1). Movement of the heads is controlled by the attachment specifying the direction of movement, whether the seek is to an even or odd number track, and activating seek 1 and seek 2.

Seek 1 and 2 are out of phase by an amount depending on the number of tracks to be crossed. Initially seek 1 and (not) seek 2 accelerates the actuator to a desired track-crossing velocity. Then seek 1 and seek 2 together gate access velocity feedback to maintain the actuator at the desired velocity. (The desired velocity is derived, as a voltage level, from the digital output of the velocity store register.) Finally, (not) seek 1 and seek 2 decelerates the actuator to stop at the required track.

When seek 2 is made inactive, track following mode is allowed to align the actuator heads on the new track and maintain head track alignment until the next seek operation.



Control Load Command DISK-11



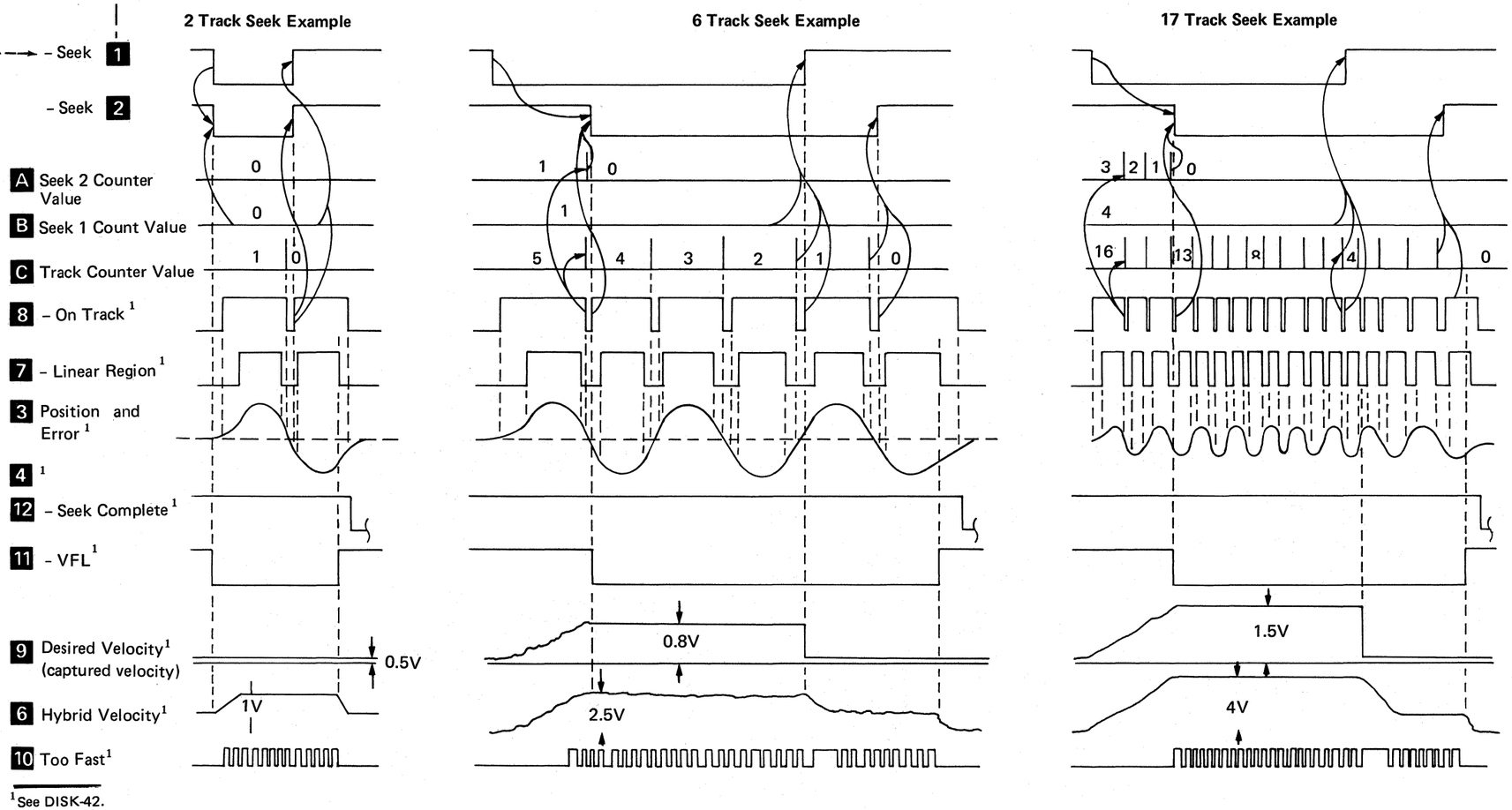
3.2 or 5.0 Megabyte Disk				
Track Counter	1 or 2	3 to 7	8 or greater	C
Seek 2 Counter	0	1	3	A
Seek 1 Count	0	1	4	B

C — This value is the number of tracks desired to seek. The track counter is actually set to this value -1.

A — This value equals the number of tracks that seek 1 allows the actuator to accelerate before seek 2 is turned on.

B — This value equals the number of tracks that seek 2 decelerates the actuator after seek 1 is turned off. The seek 1 counter acts as a register (not stepped).

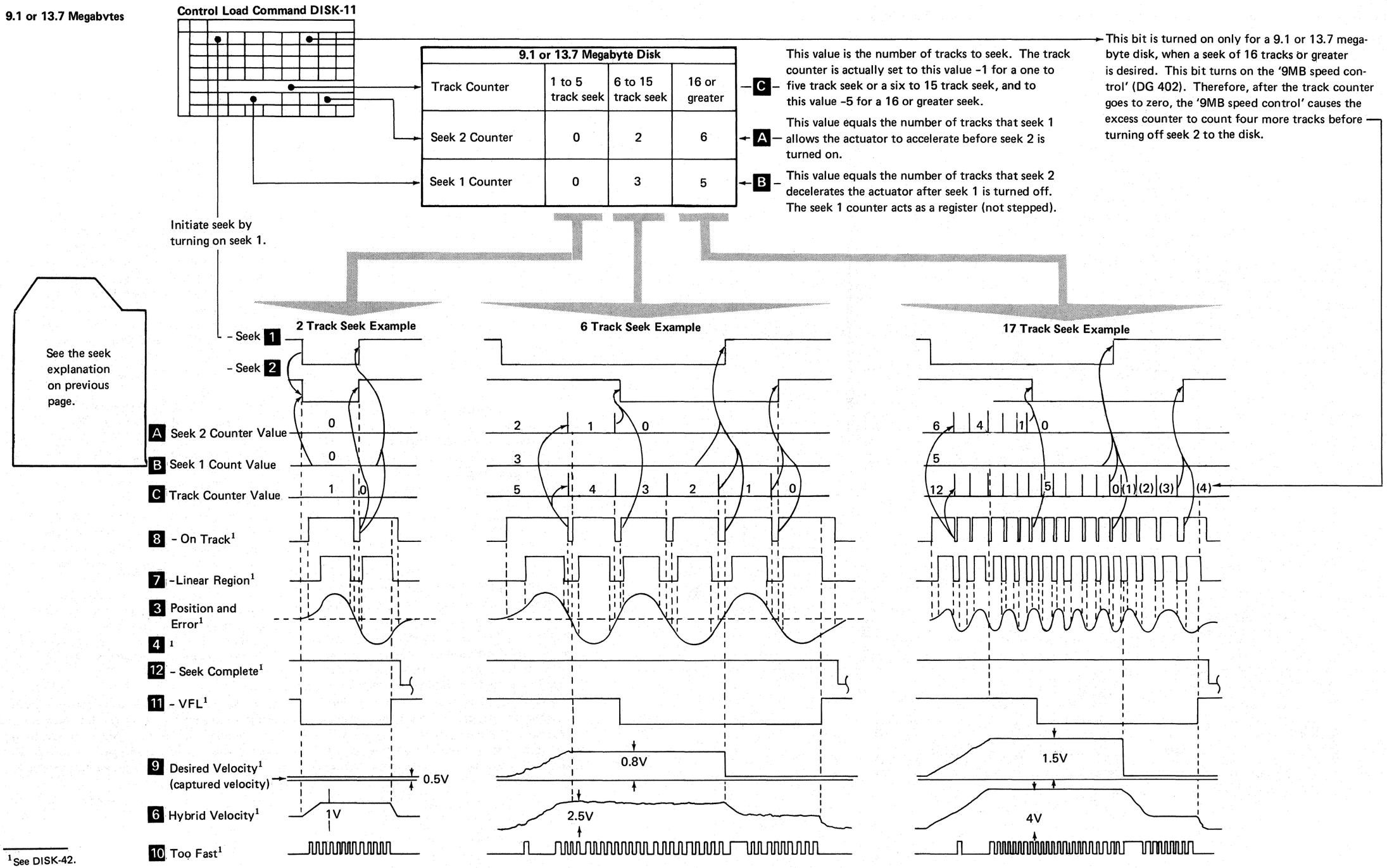
Initiate Seek by Turning On Seek 1



[1] See DISK-42.

Seek Operation

9.1 or 13.7 Megabytes



[1] See DISK-42.

Actuator Feedback During Seek

Position Error **3** *and* **4**

As the actuator moves across the tracks, the position error signal from the servo heads changes from maximum (halfway between tracks) to minimum (on track) and back to maximum as each track is crossed. Signals derived from the error signal are:

1. On Track **8** becomes active each time the head passes through a track alignment; the occurences of on track step the seek 2 counter and track counter, for the setting/ resetting of seek 1 and seek 2.

2. Linear Region **7** becomes active when head/track alignment error is low enough to be corrected by track follow mode; at the end of a seek operation, the leading edge of the linear region pulse switches from seek mode to track following mode.

3. Hybrid Velocity **6** is proportional to the rate of change of the error signal and thus to the speed of the actuator. In other words, indicates the speed of the actuator.

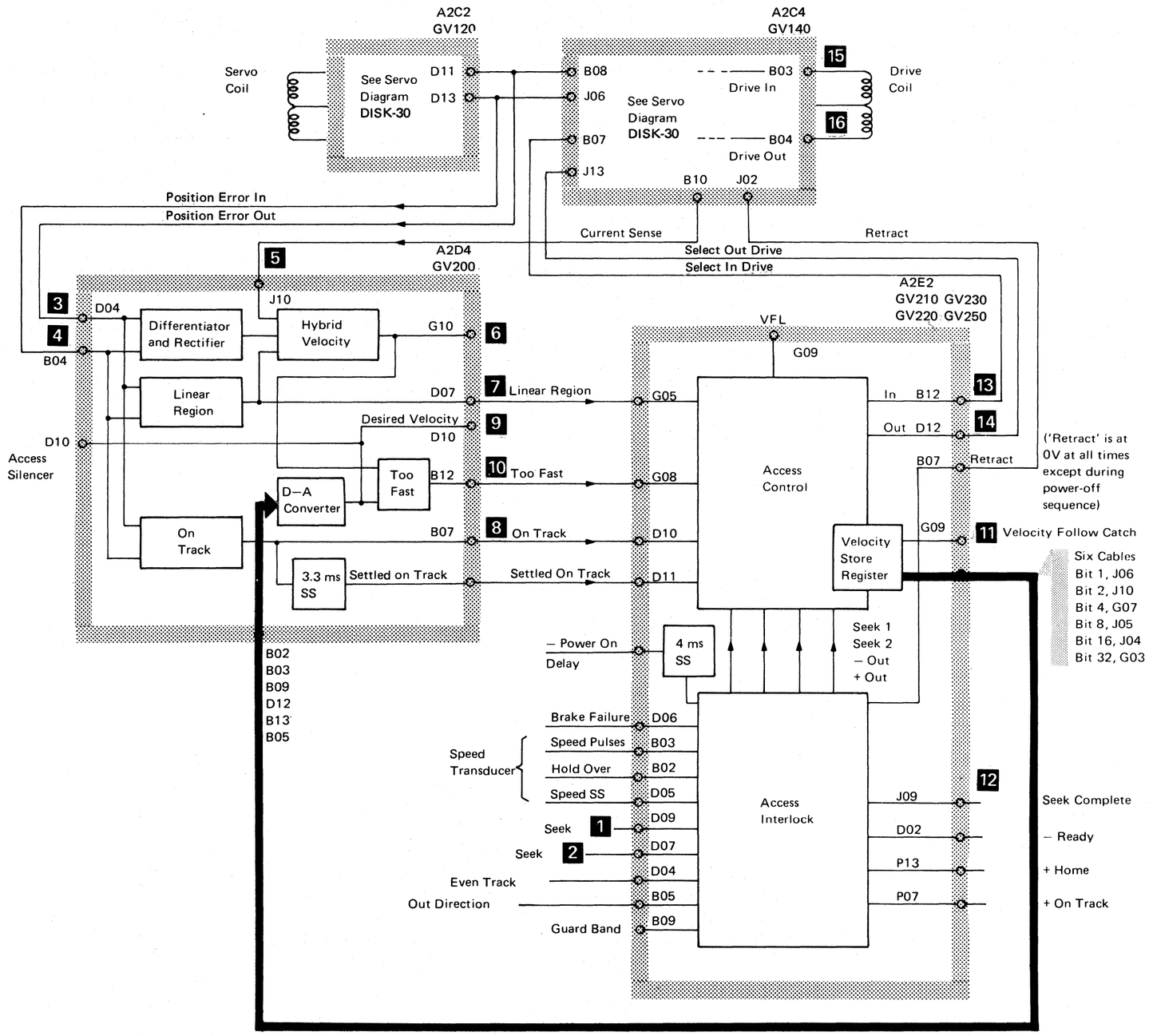
4. Too Fast **10** active, during the velocity fedback controlled phase. If hybrid velocity is greater than desired velocity. (Desired velocity is set during acceleration to a value depending on the number of tracks to be crossed, >3 tracks, [3 to 7 tracks] or >7 tracks.) The velocity follow latch gates too fast to select either in or out (depending respectively on access out or access in) to decelerate the access arm. (Equally [not] too fast allows the access arm to accelerate.)

Desired Velocity **9**

Desired velocity is set during seek acceleration to a value depending on the number of tracks to be crossed. The servo clock counter is allowed to step up the value in the velocity store register as long as acceleration continues. For example, because of longer acceleration, a >7 track seek allows a greater value in the velocity store register than a 3 to 7 track seek. Therefore, during the seek acceleration mode of a >7 track, seek the hybrid velocity (actual access velocity) is allowed to go higher until it compares with the higher velocity store value. Then too fast and VFL take control.

Velocity Follow Latch (VFL) **11**

This latch is set at the end of the accelerate phase by the 'seek 2' line. During this time, the select in drive and select out drive is constantly switched by the too fast line gated by VFL to alternately select the coil drivers to control the speed of the actuator.



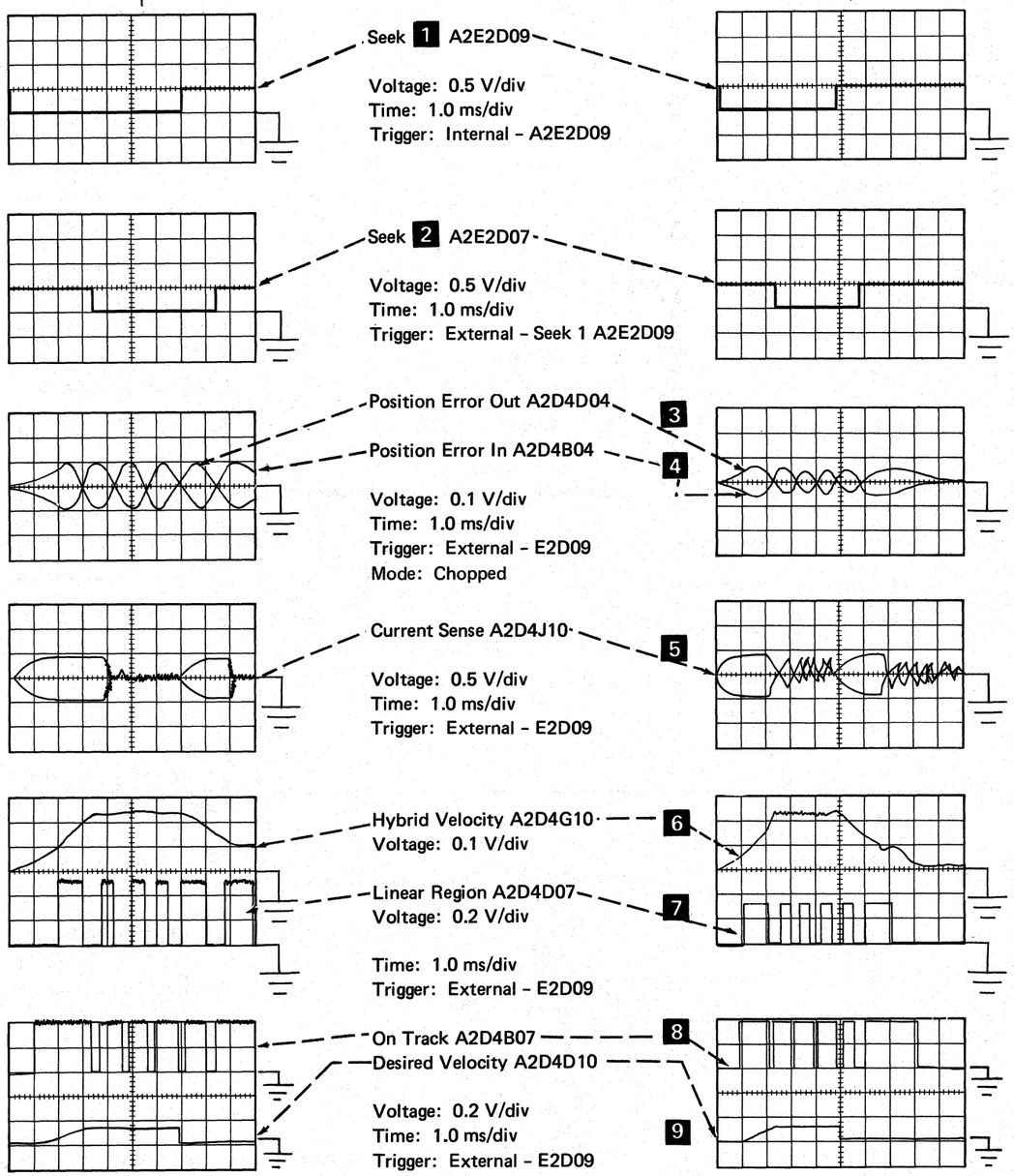
Seek Wave Forms

Use CE Friend Test, + -Seek Option and 0006 Tracks

All pictures taken with a times 10 probe.

3.2 or 5.0 megabyte disk

9.1 or 13.7 megabyte disk



Seek 1 A2E2D09

Voltage: 0.5 V/div
Time: 1.0 ms/div
Trigger: Internal - A2E2D09

Seek 2 A2E2D07

Voltage: 0.5 V/div
Time: 1.0 ms/div
Trigger: External - Seek 1 A2E2D09

Position Error Out A2D4D04 — 3

Position Error In A2D4B04 — 4

Voltage: 0.1 V/div
Time: 1.0 ms/div
Trigger: External - E2D09
Mode: Chopped

Current Sense A2D4J10 — 5

Voltage: 0.5 V/div
Time: 1.0 ms/div
Trigger: External - E2D09

Hybrid Velocity A2D4G10 — 6

Voltage: 0.1 V/div

Linear Region A2D4D07 — 7

Voltage: 0.2 V/div

Time: 1.0 ms/div
Trigger: External - E2D09

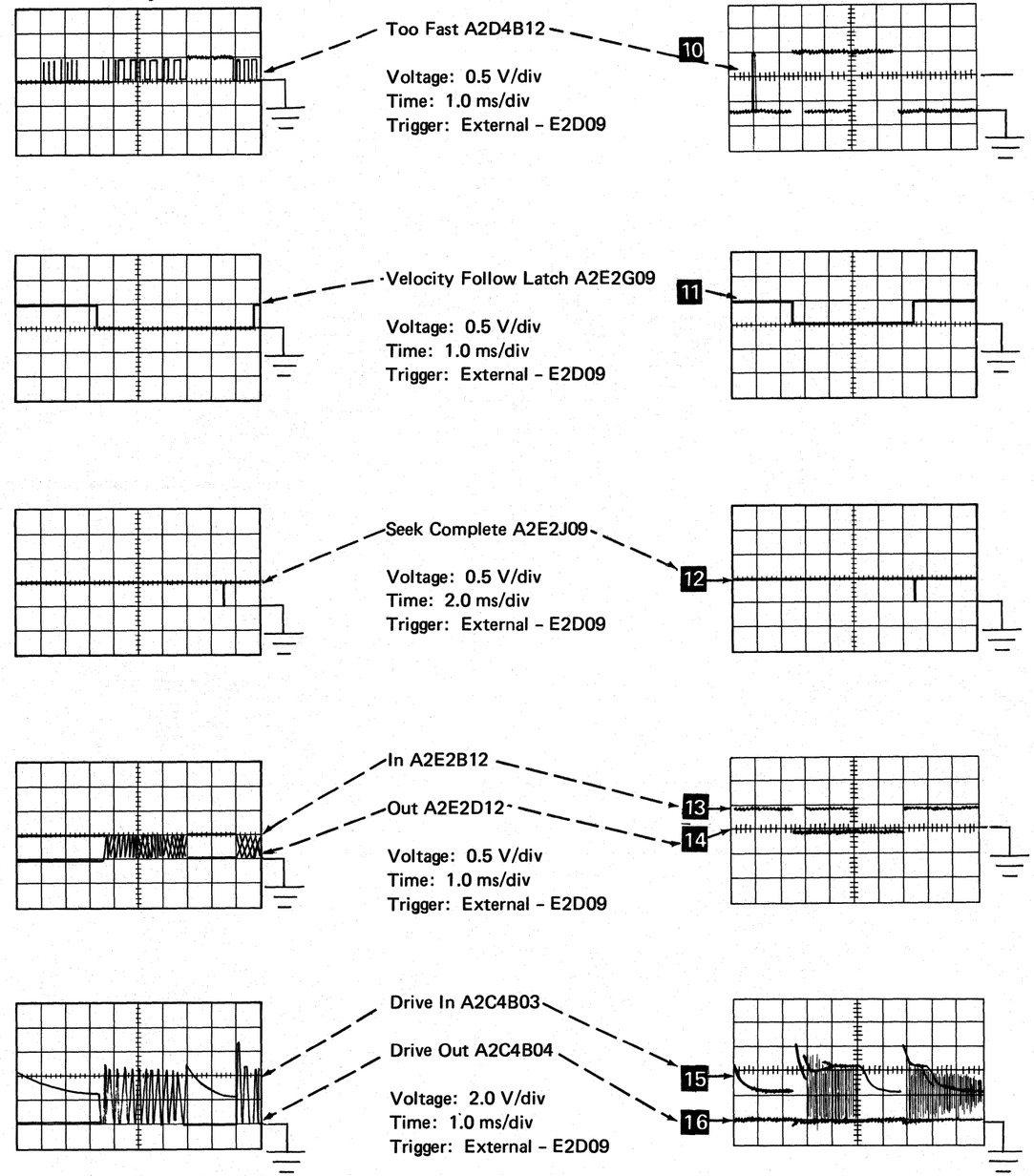
On Track A2D4B07 — 8

Desired Velocity A2D4D10 — 9

Voltage: 0.2 V/div
Time: 1.0 ms/div
Trigger: External - E2D09

3.2 or 5.0 megabyte disk

9.1 or 13.7 megabyte disk



Too Fast A2D4B12 — 10

Voltage: 0.5 V/div
Time: 1.0 ms/div
Trigger: External - E2D09

Velocity Follow Latch A2E2G09 — 11

Voltage: 0.5 V/div
Time: 1.0 ms/div
Trigger: External - E2D09

Seek Complete A2E2J09 — 12

Voltage: 0.5 V/div
Time: 2.0 ms/div
Trigger: External - E2D09

In A2E2B12 — 13

Out A2E2D12 — 14

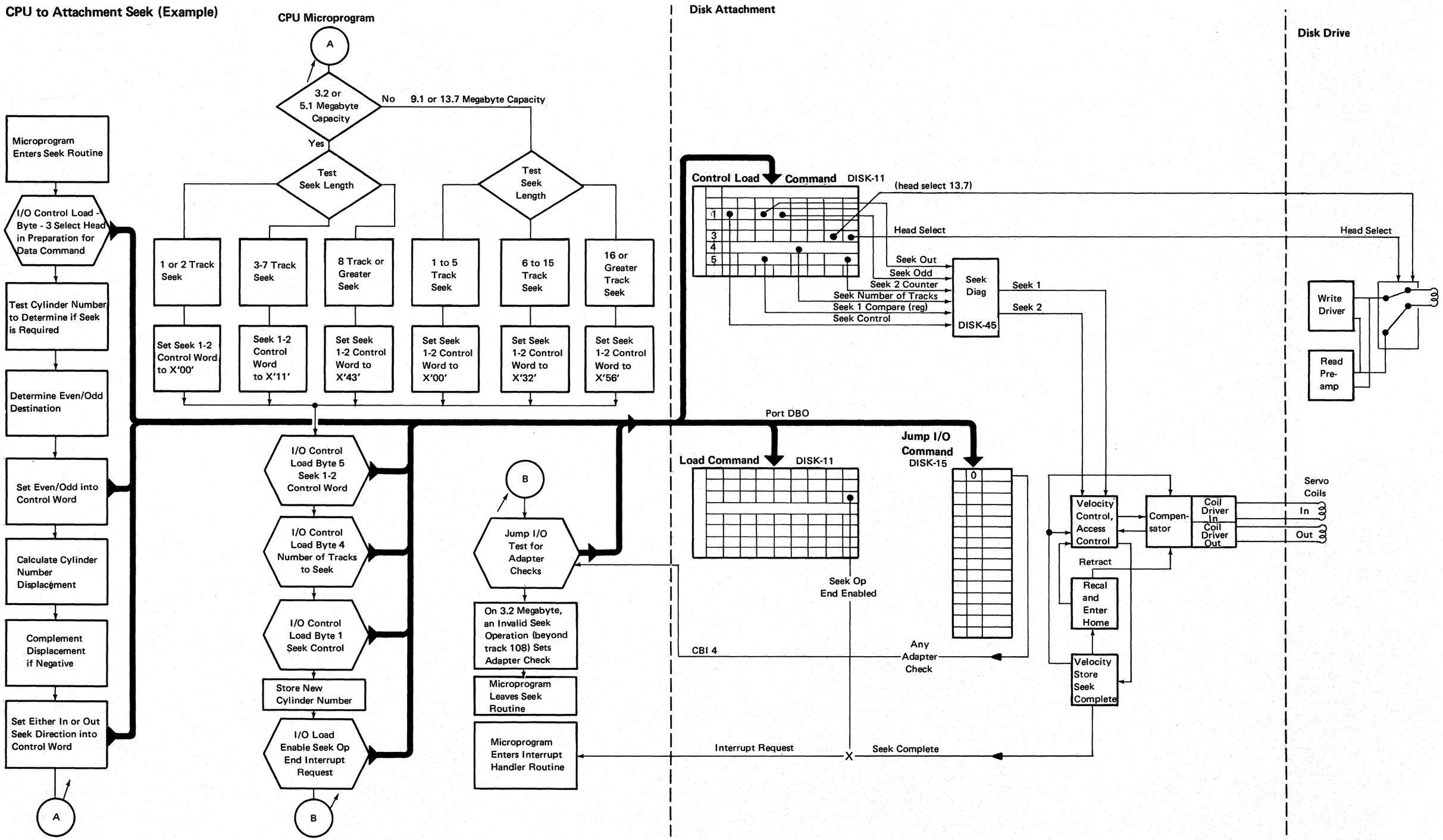
Voltage: 0.5 V/div
Time: 1.0 ms/div
Trigger: External - E2D09

Drive In A2C4B03 — 15

Drive Out A2C4B04 — 16

Voltage: 2.0 V/div
Time: 1.0 ms/div
Trigger: External - E2D09

CPU to Attachment Seek (Example)



Recalibrate and Seek Out (Example)

Recalibrate: A recalibrate positions the moving heads over track 0.

Seek: This example shows a 3.2 or 5.0 megabyte five track seek. The seek 1 track counter is loaded with a value of 4 that indicates how many tracks to seek minus 1. (In this example, seek 5 tracks.)

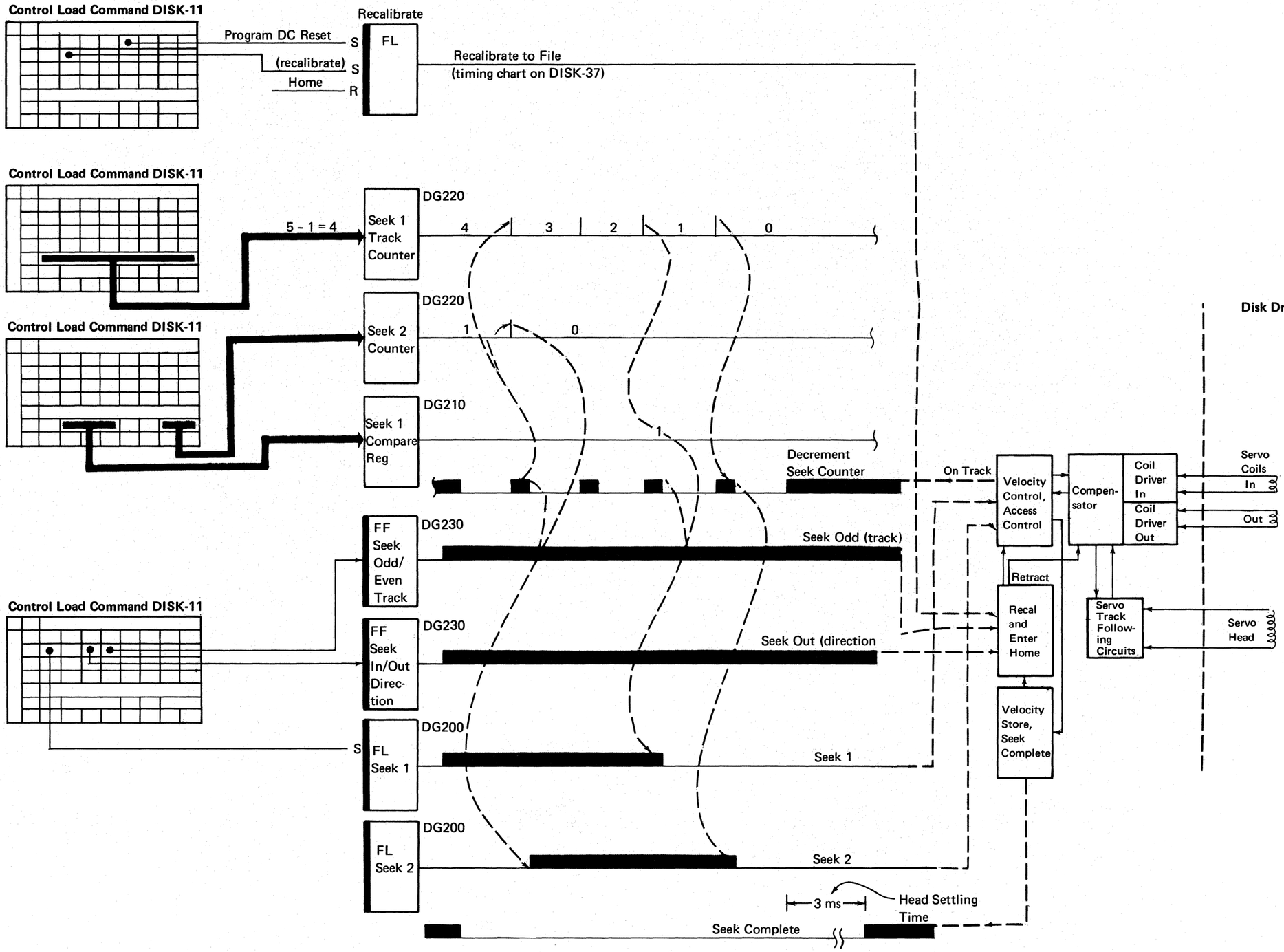
The seek 2 counter is loaded with a value that indicates how many tracks past the first track seeked that the seek 2 FL is set.

The seek 1 compare reg is loaded with a value that indicates how many tracks before the last track seeked that the seek 1 FL is reset. Indicates when the servo is over a data track (on track).

The seek odd/even track FF is set on when a seek to an odd track is desired. It is set off when a seek to an even track is desired.

The 'seek out direction' FF is set on when a seek toward the outer edge of the disk (higher track number) is desired. It is set off when a seek toward the inner edge of the disk (lower track number) is desired.

The seek 1 FL and the seek 2 FL control the servo arm velocity.



Power On/Off

The power on switch and K1 activate the dc power supplies A .

The brake coil circuit B allows K2 to pick, and the disk drive motor C to start. If the brake coil circuit indicates a brake failure, which indicates the brake is on, K2 cannot pick. This prevents ac to the drive motor.

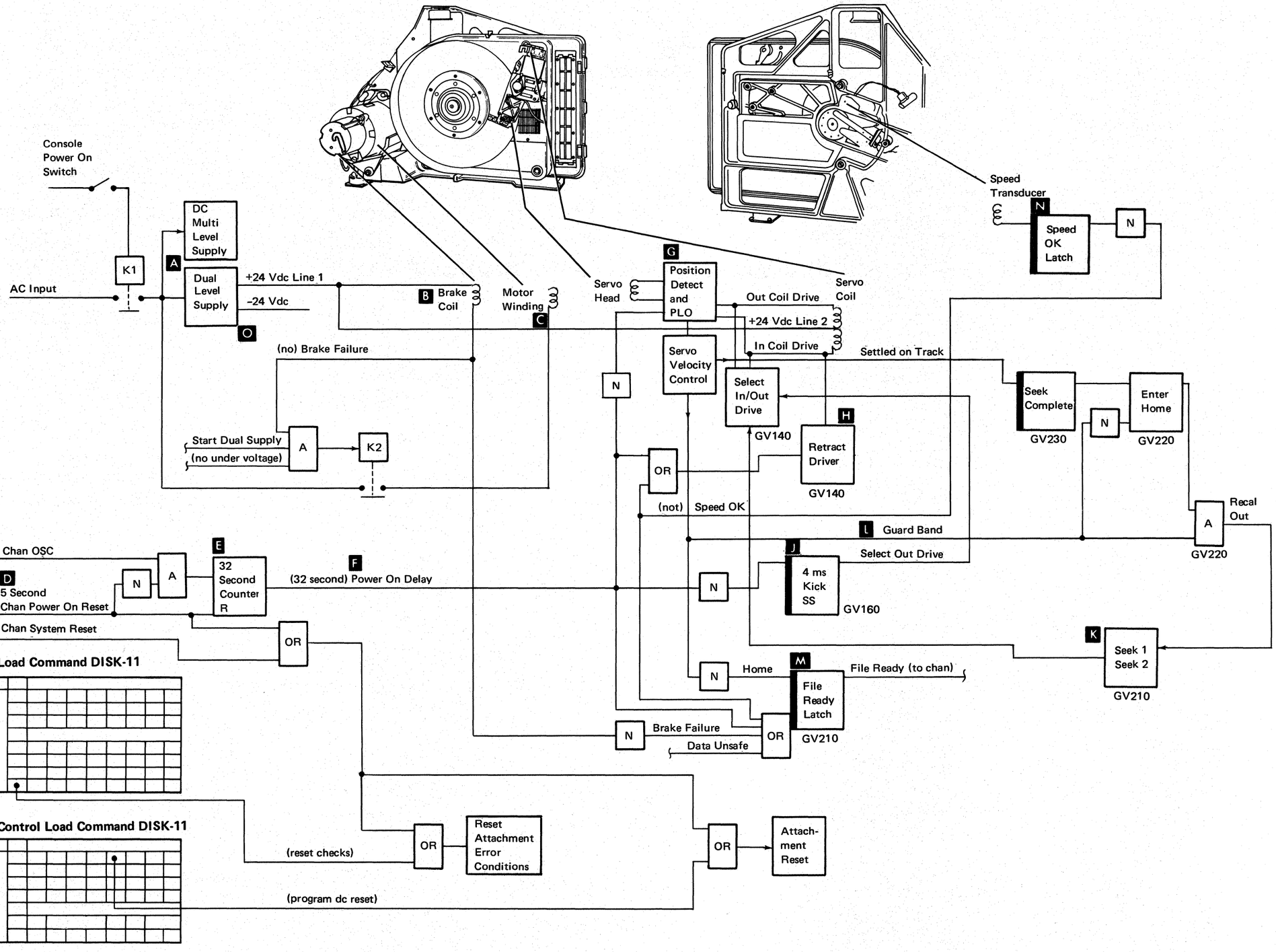
The '5-second channel power on reset' line D holds the 32 second counter E reset. After 5 seconds, the 32 second counter starts to run. All during this time, 'power on delay' F is active. At the end of the 32 second delay the PLO G synchronizes to the servo clock pulses.

During power on delay, the retract H line holds the actuator against the inner (spindle) stop.

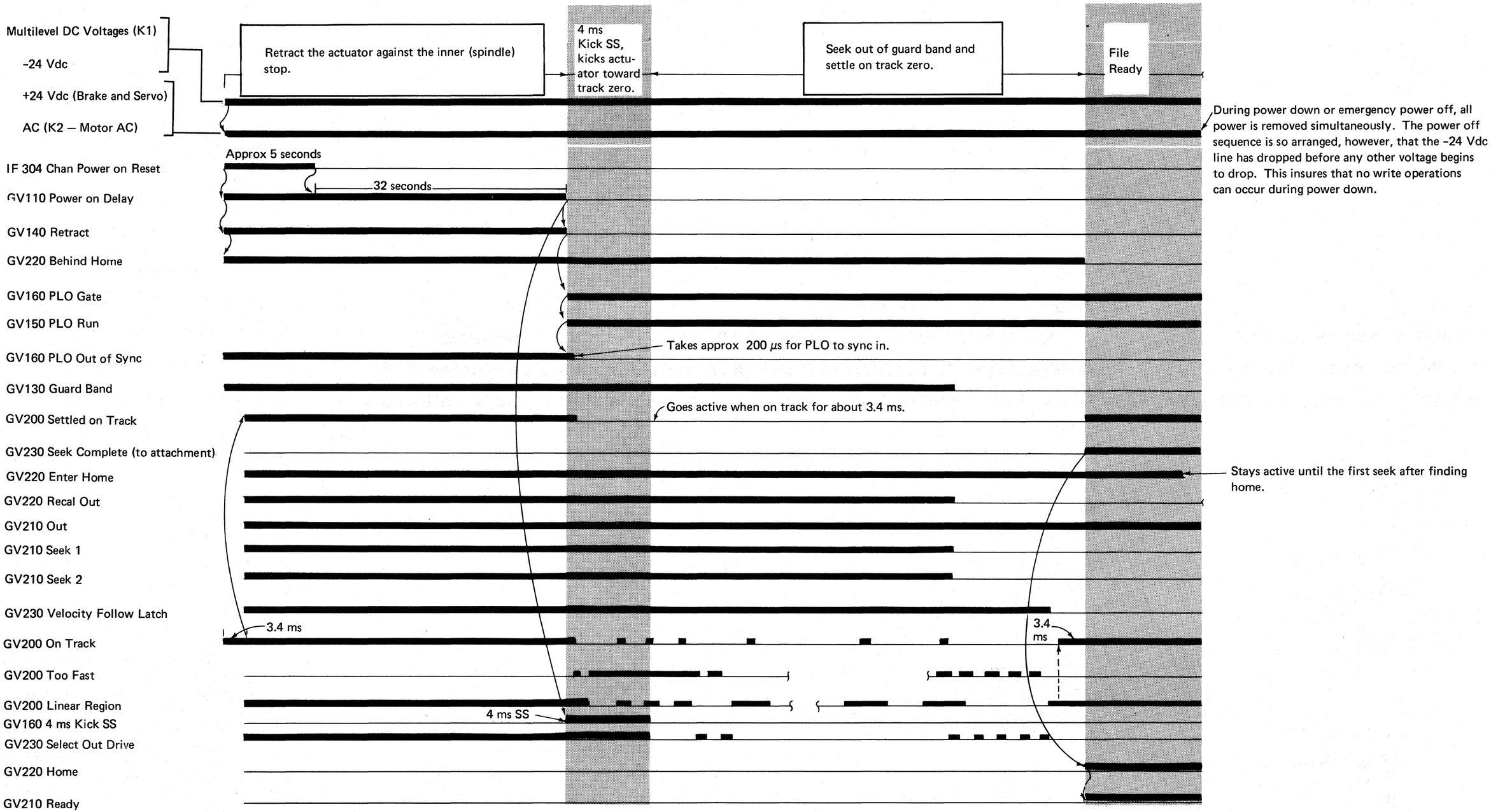
At the end of the power on delay, the 4 ms kick SS J starts the actuator outward movement, then seek 1 and seek 2 K continue the movement. Detecting data area deactivates guard band L . The outward seek is dropped and the actuator stops the data heads over track zero; and home and file ready M is activated.

The disk heads which are mounted on the actuator, fly above the disk as the disk comes up to speed. If the disk speed drops to approximately 1800 rpm, the speed OK latch N is reset and the disk drive goes not ready. Then the actuator arm is retracted H against the inner (spindle) stop. This ensures that the heads land over the landing zone.

During all power down conditions the actuator arm is retracted against the inner (spindle) stop by the +24 Vdc power supply O . A magnetic catch holds the actuator in the retracted position.



Power On and Seek Home

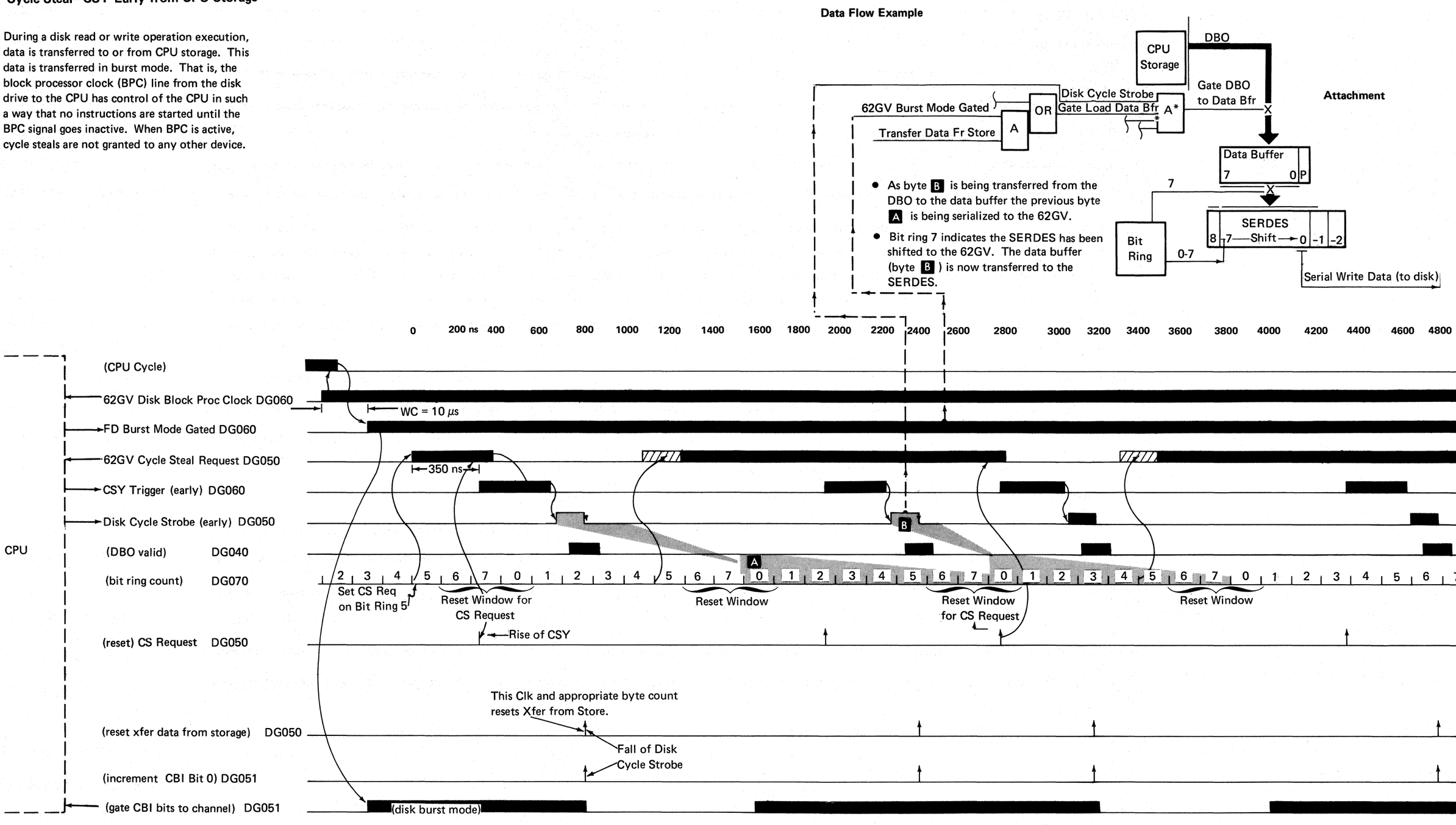


During power down or emergency power off, all power is removed simultaneously. The power off sequence is so arranged, however, that the -24 Vdc line has dropped before any other voltage begins to drop. This insures that no write operations can occur during power down.

CYCLE STEAL

Cycle Steal—CSY Early from CPU Storage

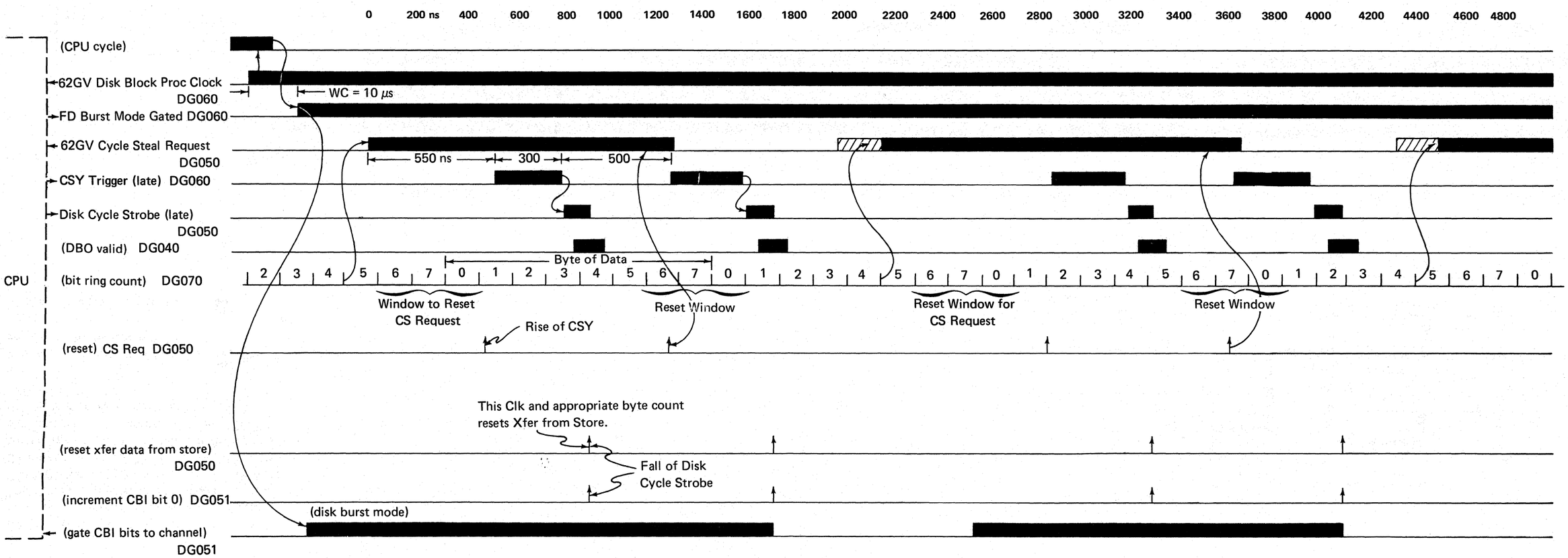
During a disk read or write operation execution, data is transferred to or from CPU storage. This data is transferred in burst mode. That is, the block processor clock (BPC) line from the disk drive to the CPU has control of the CPU in such a way that no instructions are started until the BPC signal goes inactive. When BPC is active, cycle steals are not granted to any other device.



Cycle Steal—CSY Late from CPU Storage

During a disk read or write operation execution, data is transferred to or from the CPU storage. This data is transferred in burst mode. That is, 'disk block processor clock' line from the disk drive to the CPU has control and no instructions are started until 'disk block processor clock' goes inactive. During this time, cycle steals are not granted to any other devices.

See data flow on previous page.

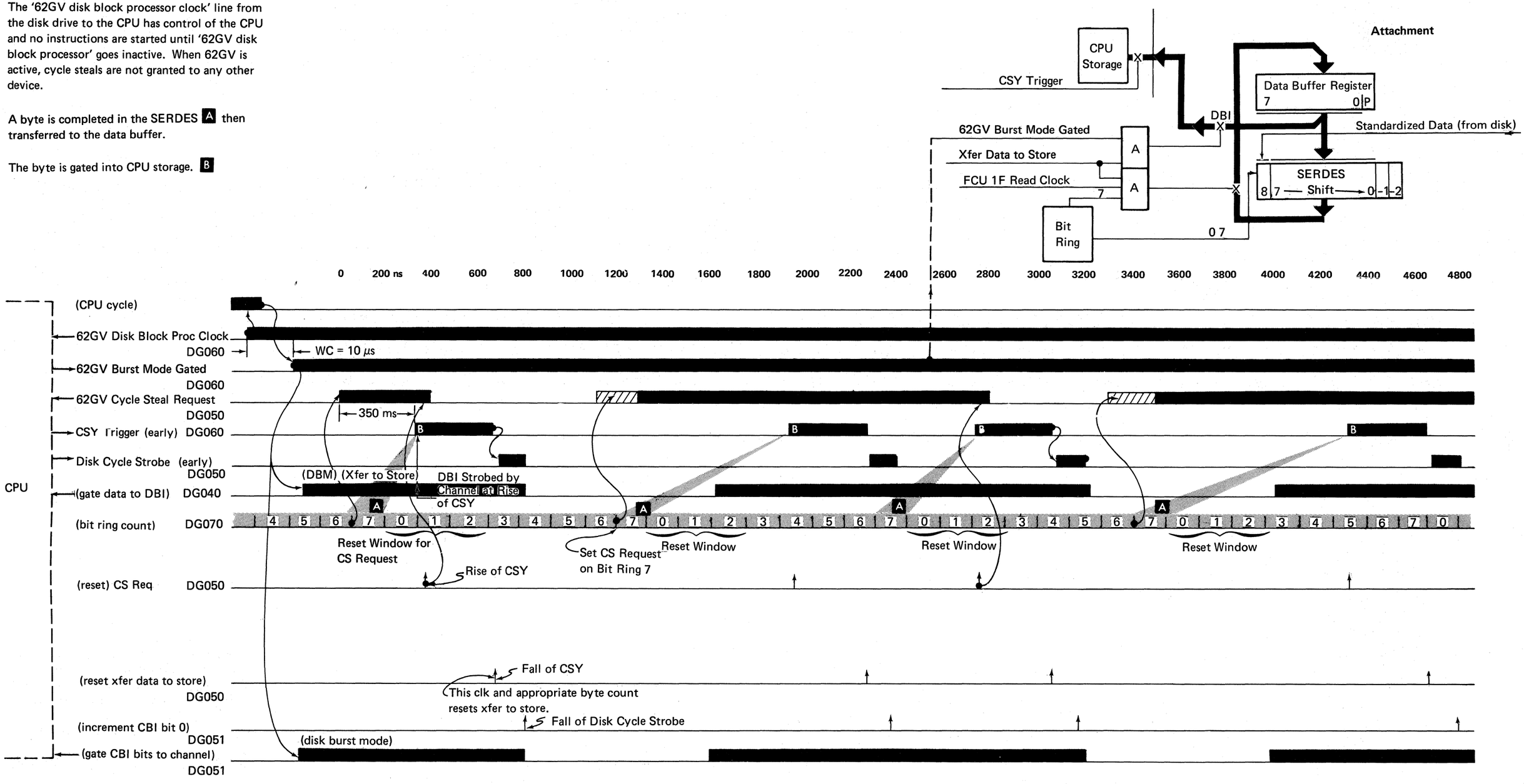


Cycle Steal—CSY Early to CPU Storage

During execution of a disk read or write operation, data is transferred to or from CPU storage. This data is transferred in burst mode. That is, The '62GV disk block processor clock' line from the disk drive to the CPU has control of the CPU and no instructions are started until '62GV disk block processor' goes inactive. When 62GV is active, cycle steals are not granted to any other device.

A byte is completed in the SERDES **A** then transferred to the data buffer.

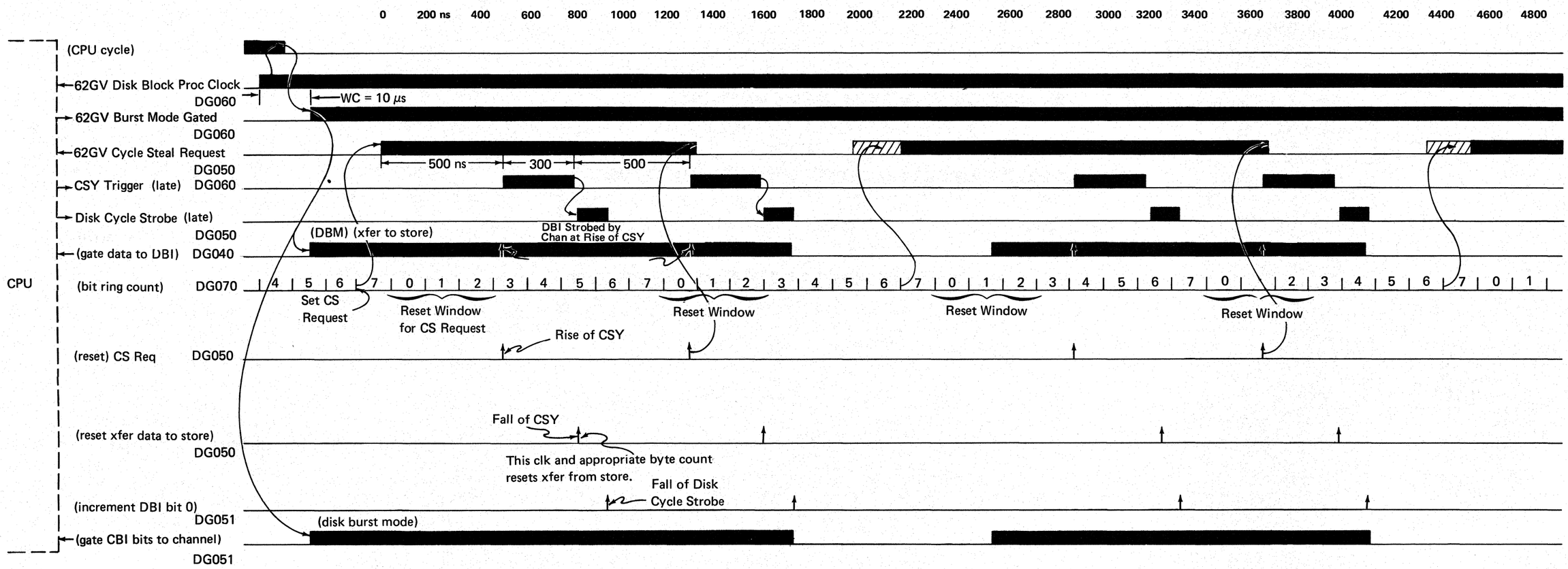
The byte is gated into CPU storage. **B**



Cycle Steal—CSY Late to CPU Storage

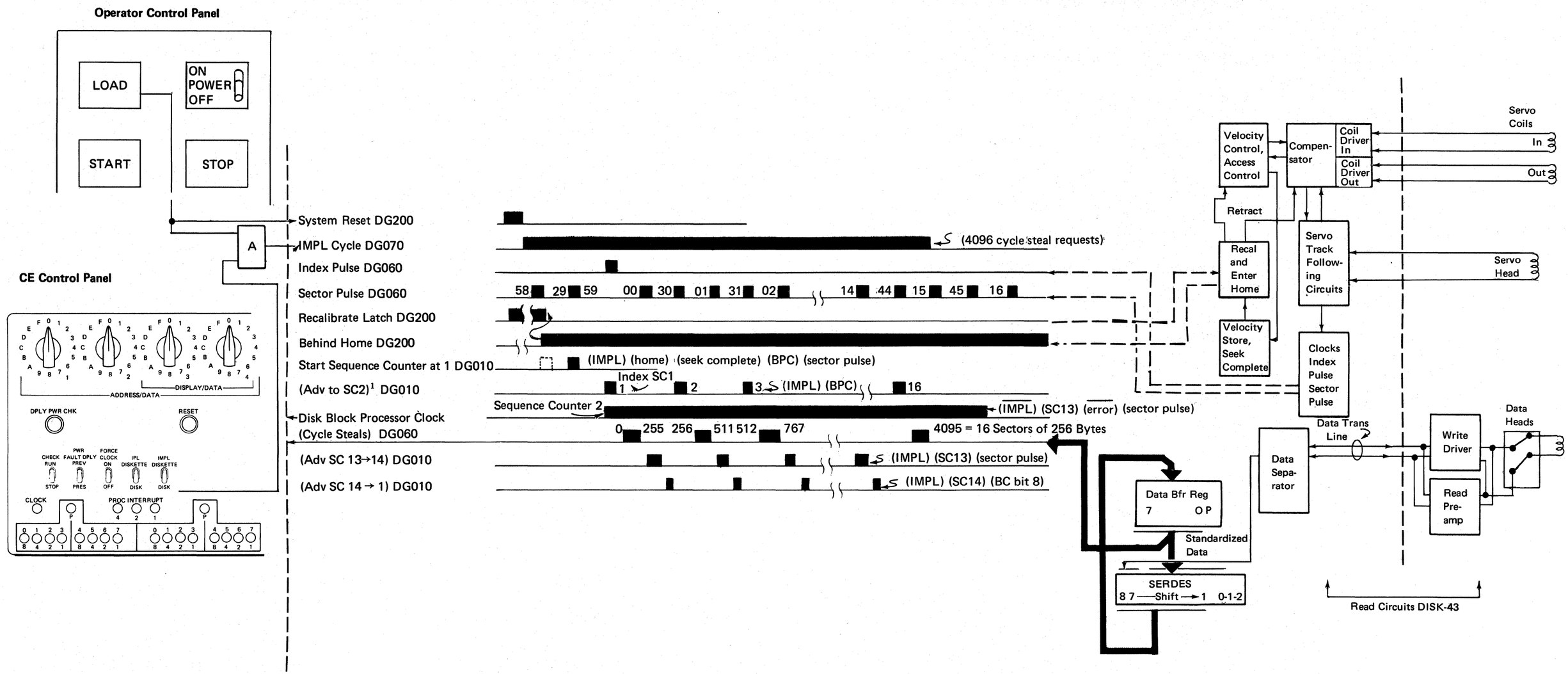
During execution of a disk read or write operation, data is transferred to or from CPU storage. This data is transferred in burst mode. That is, the '62GV disk block processor clock' line from the disk drive to the CPU has control of the CPU and no instructions are started until '62GV disk block processor' goes inactive. When disk is active, cycle steals are not granted to any other device.

See data flow on previous page.



INITIAL MICROPROGRAM LOAD (IMPL)

IMPL



[1] Data transfers operate like read data or read diagnostic operations. Sector hit is forced.

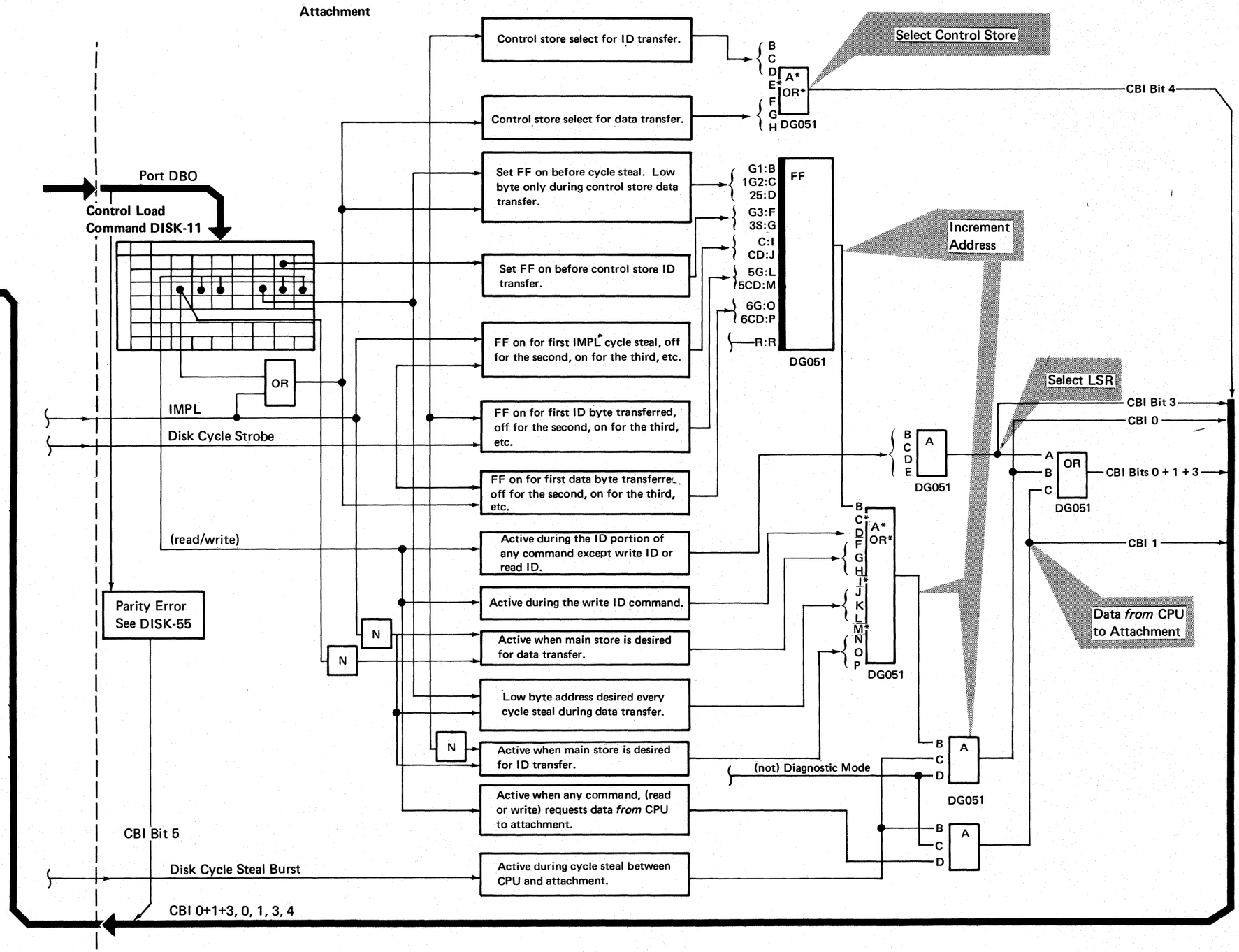
COMMAND BUS IN (CBI)

Before any read or write operations between the CPU and disk are executed, a control load command sets the desired DBI control information into the attachment. This control information selects and holds the desired CBI configuration needed and sends it back to the CPU, therefore controlling data and addressing (as indicated below) between the CPU and attachment during subsequent read or write operations.

Command Bus In

Bits 0 1 3 4 5

- 0 0 = Cycle steal data to CPU — no increment to MAR.
- 0 1 = Cycle steal data from CPU — no increment to MAR.
- 1 0 = Cycle steal data to CPU — increment MAR.
- 1 1 = Cycle steal data from CPU — increment MAR.
- 0 = Cycle steal LSR 0 (WR 4 interrupt level-1) select — data field address.
- 1 = Cycle steal LSR 1 (WR 5 interrupt level-1) select — ID field address.
- 1 = Select control store during cycle steals/ Indicates to the CPU not to check parity of DBI during a sense command/jump I/O condition met.
- 1 = Data bus out parity check. See DISK-55.



ERROR CONDITIONS

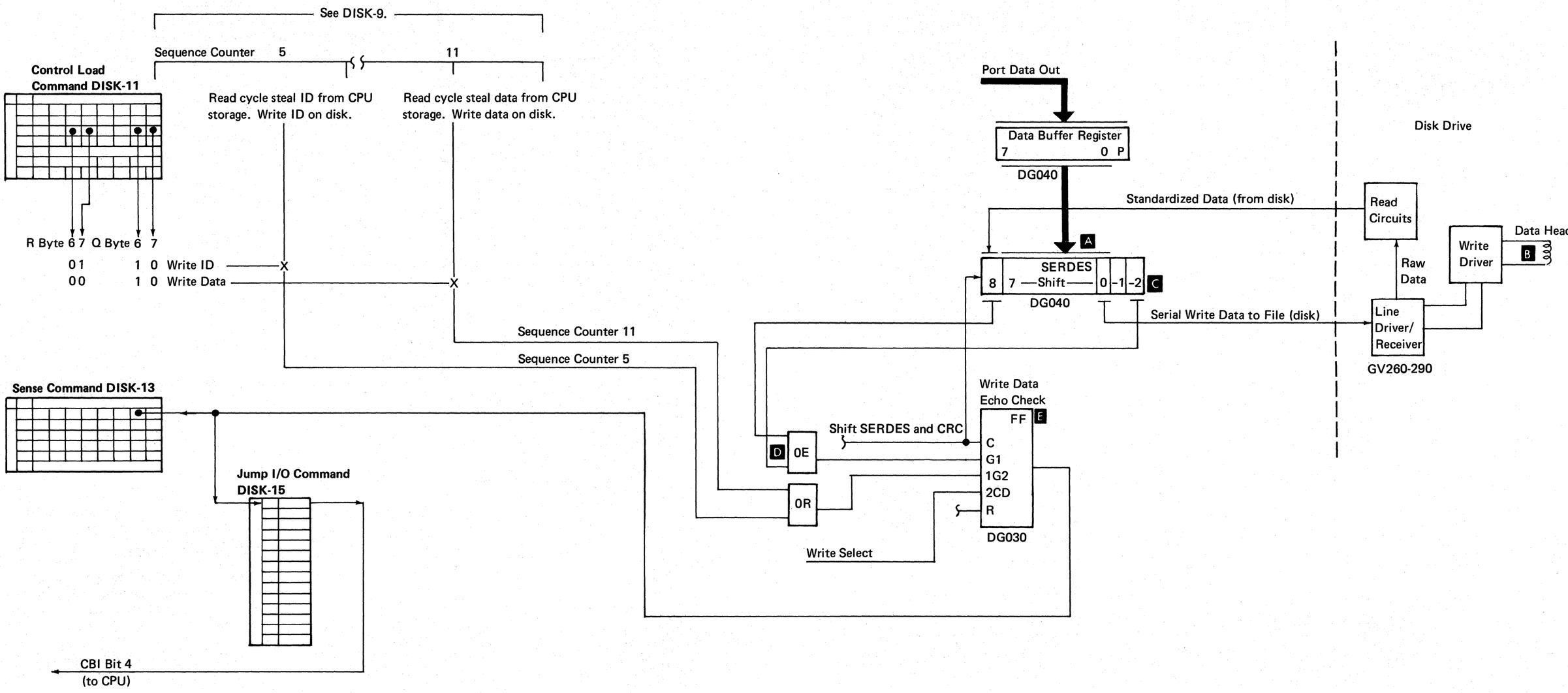
Write Data Echo Check

A bit written to the line driver/receiver fails to appear as a bit read from the read circuits 2 bit times later.

A write data echo check error condition can be detected when one of the following read or write operations is executing.

As each ID or data byte is read from CPU storage, it goes to the DBO to data buffer register, to the SERDES A . The contents of the SERDES is shifted out of position 0 a bit at a time and sent to the data head B and written on the disk. Also, as the contents of the SERDES is shifted out of position 0, it is shifted a bit at a time through the SERDES to position -2 C .

By the time a bit written on the disk is shifted into position -2, the bit should appear as a bit read from the line driver/receiver. The position -2 bit is compared to the read bit D . If bits written do not compare with the bits read, the write data echo check FF is turned on E



DBO Parity Check

Pick or drop bit(s) during transfer of data bytes or a micro instruction on the DBO.

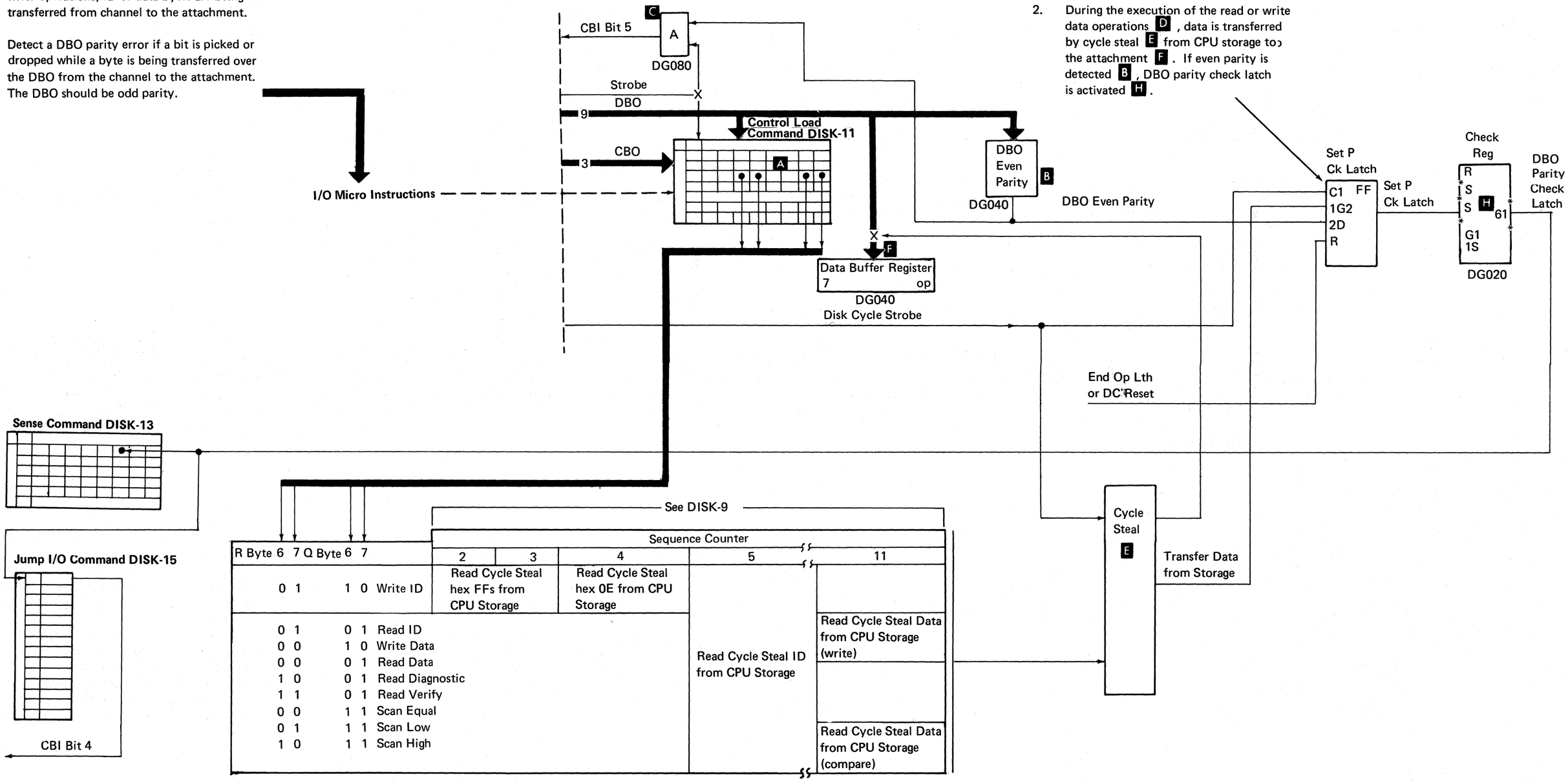
A DBO parity error condition can be detected when the following micro instructions, read or write operations, ID or data bytes are being transferred from channel to the attachment.

Detect a DBO parity error if a bit is picked or dropped while a byte is being transferred over the DBO from the channel to the attachment. The DBO should be odd parity.

The DBO is checked for correct parity under two conditions:

1. When a micro instruction is sent to the attachment [A], the DBO is checked for correct odd parity. If even parity is detected [B], CBI bit 5 is activated [C]

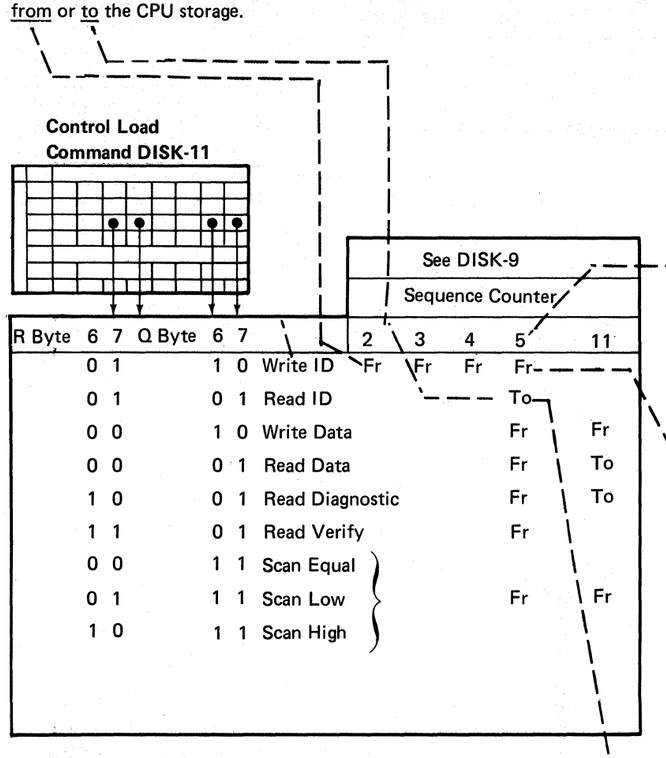
2. During the execution of the read or write data operations [D], data is transferred by cycle steal [E] from CPU storage to the attachment [F]. If even parity is detected [B], DBO parity check latch is activated [H].

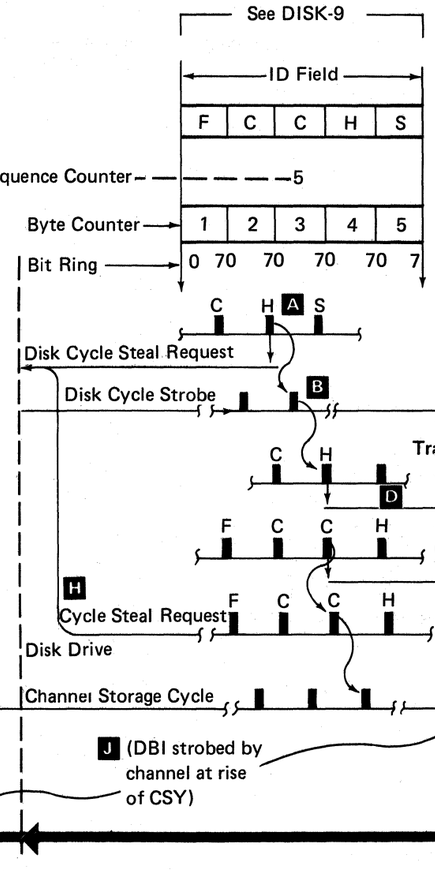


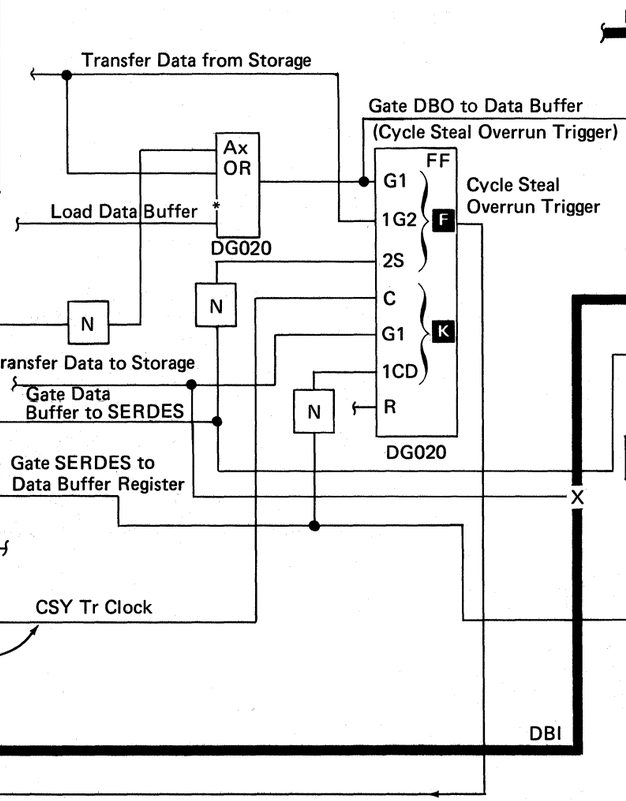
Cycle Steal Overrun Check

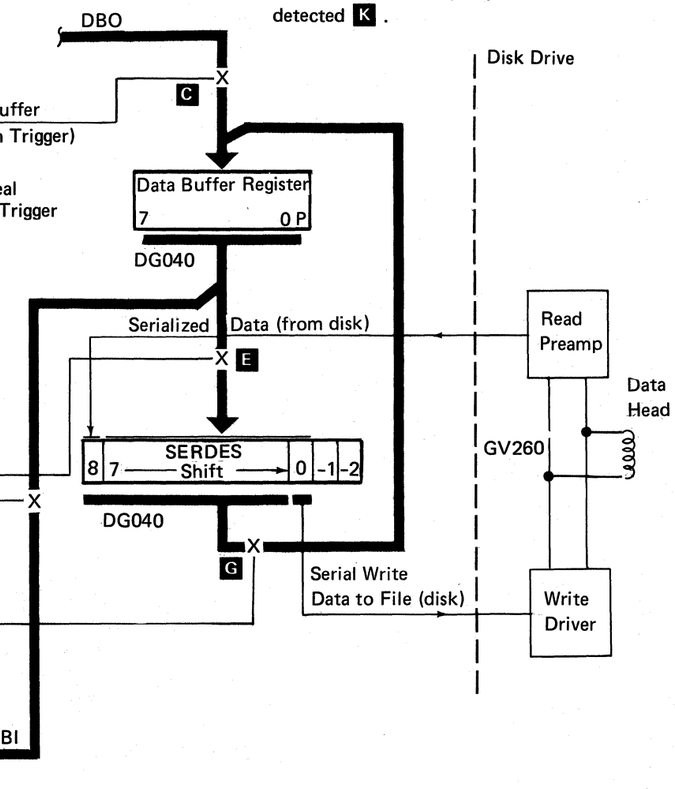
Data is being transferred from the channel to the data buffer at the same time the data buffer is being transferred to the SERDES; or data is being transferred from the data buffer to the channel at the same time the SERDES is being transferred to the data buffer.

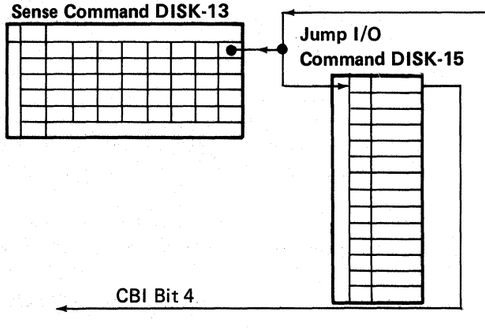
A cycle steal overrun check error condition can be detected when any one of the following read or write operations is transferring ID or data from or to the CPU storage.











Error Detection

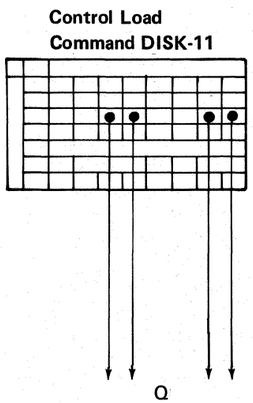
Example 1: During write ID, the head select byte A requested is strobed B into the data buffer register C , then the data buffer register is transferred to the SERDES and D and E . Now, if the head select byte is strobed into the data buffer register at the same time as the data buffer register is transferred to the SERDES, a cycle steal overrun is detected F .

Example 2: During read ID, the cylinder select byte is gated from the SERDES to the data buffer register G . A cycle steal is requested H . The cylinder select byte is strobed to the channel Now, if the cylinder select byte is being transferred from the SERDES to the data buffer register at the same time as the data buffer register is being transferred to the channel, a cycle steal overrun is detected K .

SERDES Parity Check

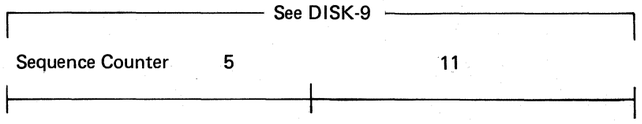
Pick or drop bit(s) during ID or data transfer.

A SERDES parity check error condition can be detected when one of the four following read or write operations are executing.



Control Load Command DISK-11

R Byte	6	7	Q Byte	6	7	
0	1			1	0	Write ID
0	0			1	0	Write Data
0	1			0	1	Read ID
0	0			0	1	Read Data



Read cycle steal ID from CPU storage, test for a SERDES parity check, and write the ID on disk.

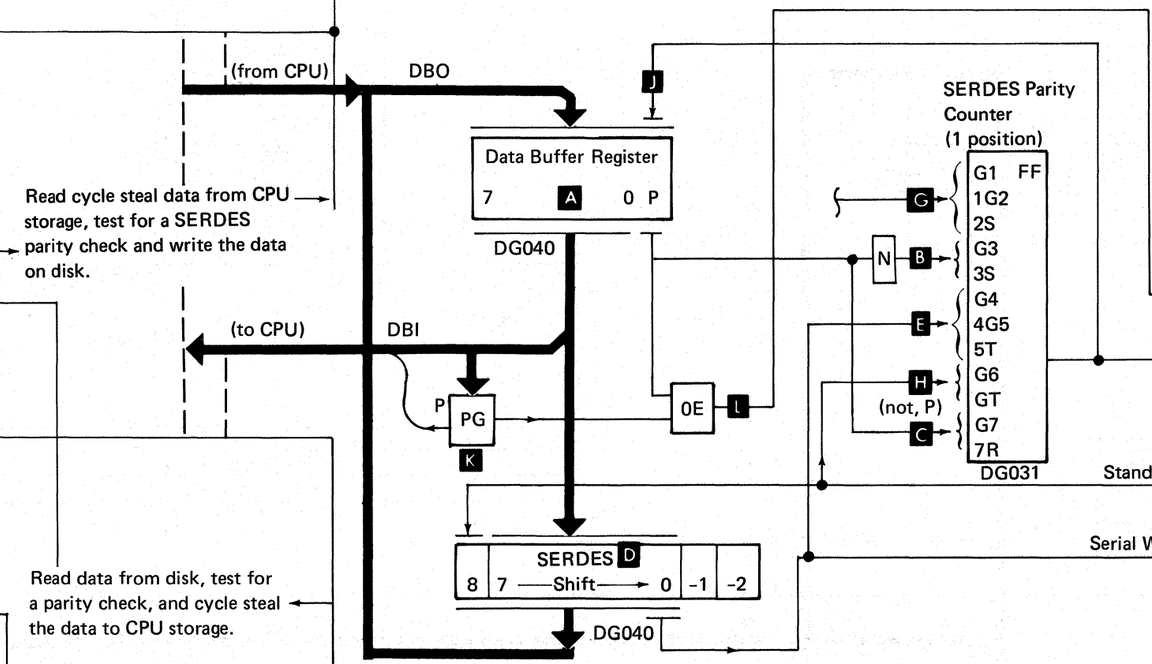
Read cycle steal data from CPU storage, test for a SERDES parity check and write the data on disk.

Read ID from disk, test for a Serdes parity check, and cycle steal the ID to CPU storage.

Read data from disk, test for a parity check, and cycle steal the data to CPU storage.

During the transfer of each byte, detect a dropped or picked up bit between the data buffer register, and write data (to disk).

Load a byte from the DBO into the data buffer register A . Place the P bit B or C into the SERDES parity counter. Load the data buffer register into the SERDES D . As each bit is shifted out of the SERDES position 0 to the disk, the SERDES parity counter is complemented E . When the byte is completely written to the disk, the SERDES parity counter should be off. If the SERDES parity counter is on when the byte is completely written, the SERDES parity check is turned on F .

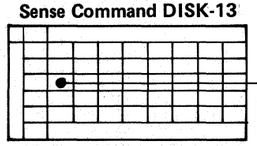


During the transfer of each byte, detect a dropped or picked up bit between the standardized data (from disk) to the DBI.

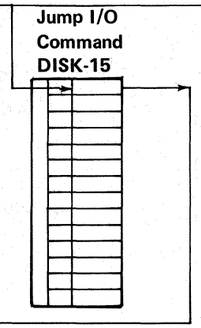
Preset the SERDES parity counter on G . As each bit is read from the disk, the SERDES parity counter is complemented H . Also these bits or (no) bits are placed in position 8 of the SERDES D and shifted.

When the complete byte (less P bit) is shifted into the SERDES, it is transferred to the data buffer register A .

If the SERDES parity counter is now on, the data buffer register parity bit is turned on J . The byte in the data buffer is transferred over the DBI to store. A P bit is generated K if required. If the P bit generated does not compare with the P bit in the data buffer register, the SERDES parity check is turned on L .



Sense Command DISK-13



Jump I/O Command DISK-15

CBI Bit 4 (to CPU)

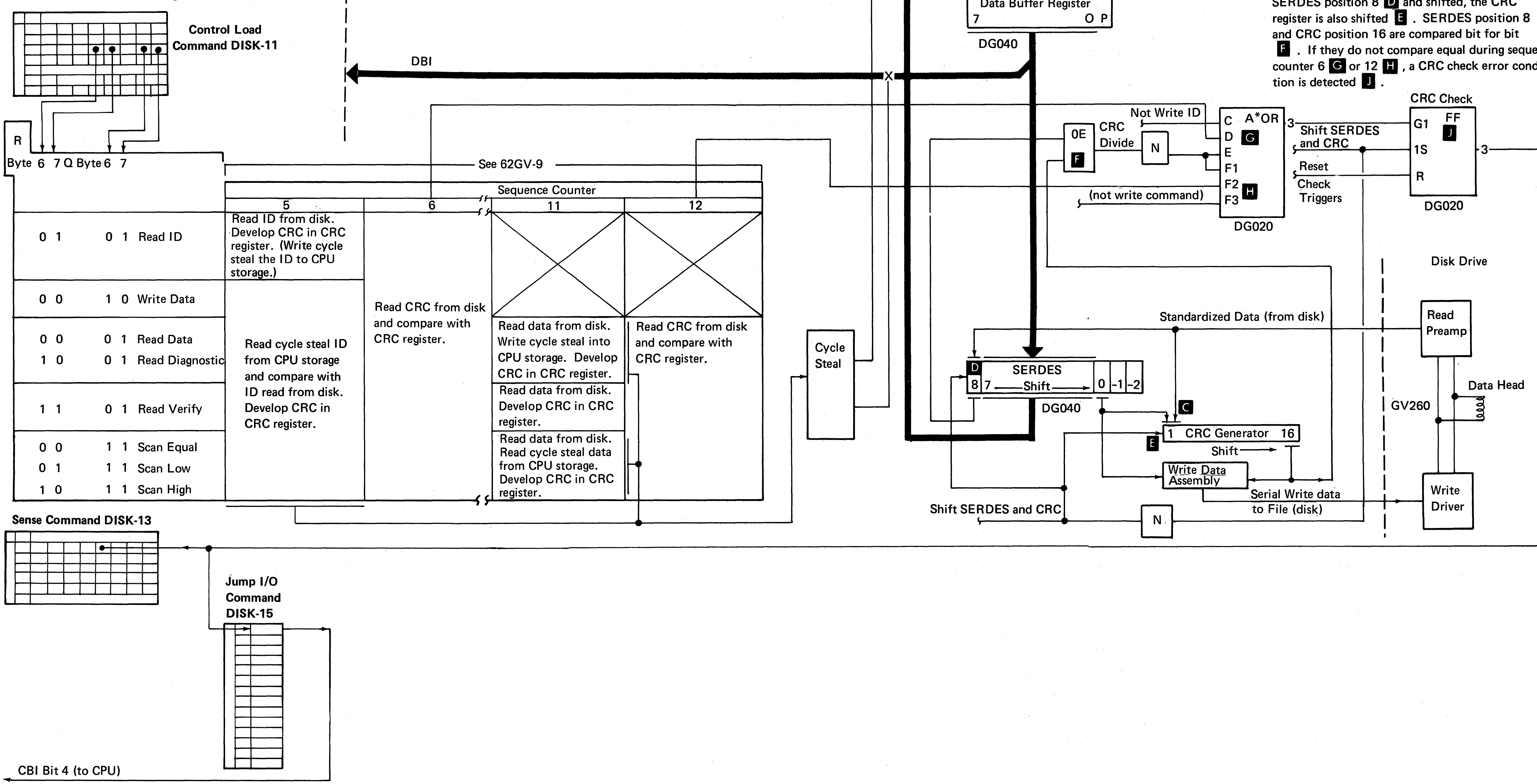
Cyclic Redundancy Check (CRC)

Pick or drop bit(s) during any data transfer between the attachment and the disk.

A cyclic redundancy check (CRC) error condition can be detected when one of the following read or write operations are executing.

Test that the CRC register contents compare equal to the CRC read from disk.

During sequence counter 5 **A** or 11 **B**, as ID or data is read from the disk, the CRC is developed in the CRC register **C**. During sequence counter 6 or 12, as the CRC is read from the disk into SERDES position 8 **D** and shifted, the CRC register is also shifted **E**. SERDES position 8 and CRC position 16 are compared bit for bit **F**. If they do not compare equal during sequence counter 6 **G** or 12 **H**, a CRC check error condition is detected **J**.



Write Check

Current is supplied (write current on) to the data heads when it should not be.

A write check error condition can be detected when one of the following write operations are executing.

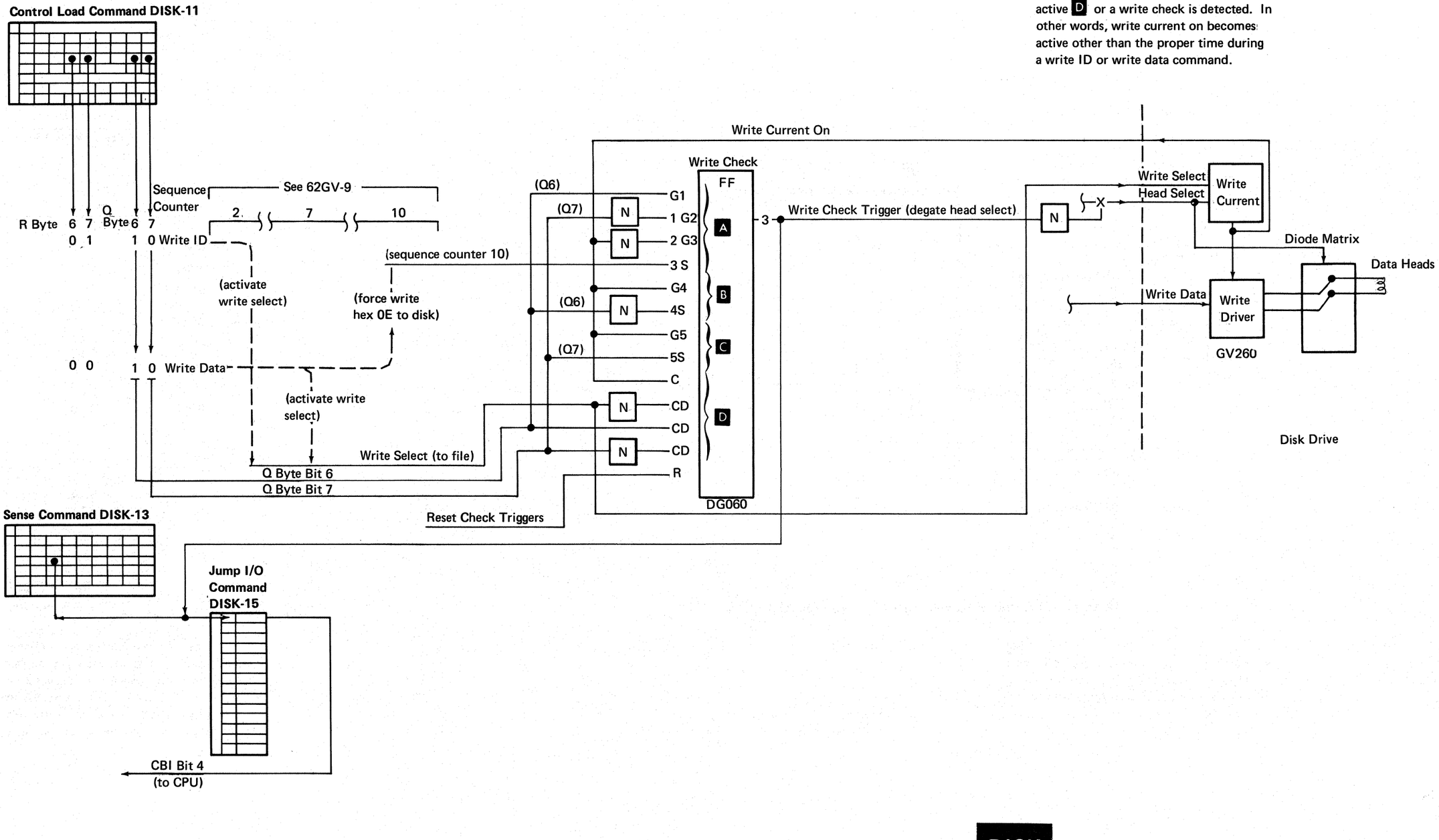
Detect a write check if write current is applied to the data heads other than the proper time during a write operation.

Write current is checked in three ways:

1. During a write data operation when the sync byte is being written, write current on should be active. If not, a write check is detected A.

2. During a write operation Q-byte, bit 6 must be active B and Q-byte, bit 7 must be inactive C indicating a write operation. If not, a write check is detected.

3. If 'write current on' is active, a write operation and the correct Q-byte bit must be active D or a write check is detected. In other words, write current on becomes active other than the proper time during a write ID or write data command.

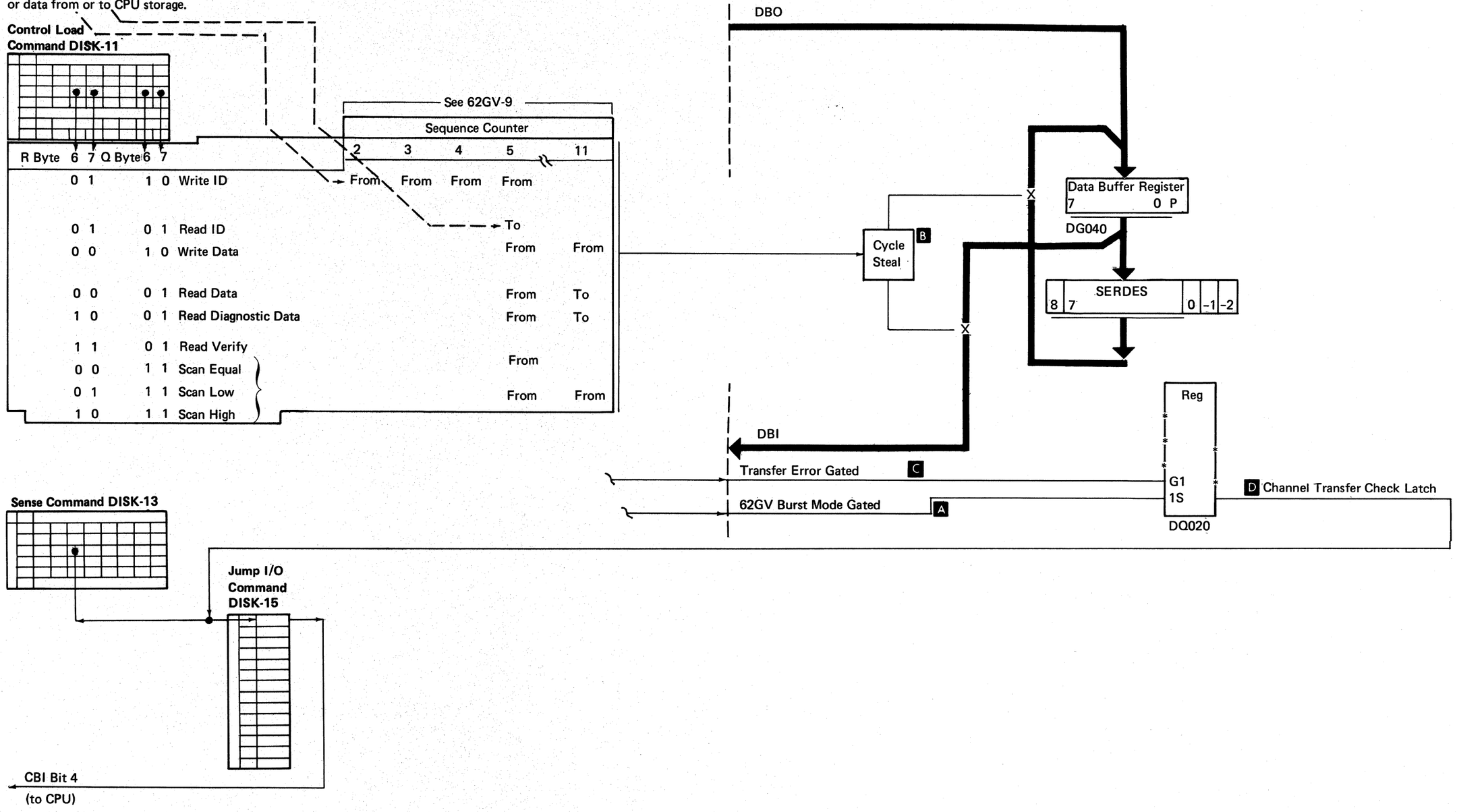


Channel Transfer Check

Any CPU or channel check occurring during cycle steal data transfer from or to the attachment.
A channel transfer check error condition can be detected when any one of the following read or write operations are transferring ID or data from or to CPU storage.

Test that a CPU or channel check does not occur while the disk attachment is in cycle steal burst mode.

When a data operation is executing, disk burst mode A is active, and cycle steals B transfer data between CPU storage and the attachment. During this time, if a CPU or channel check occurs C , a channel transfer check is detected D .



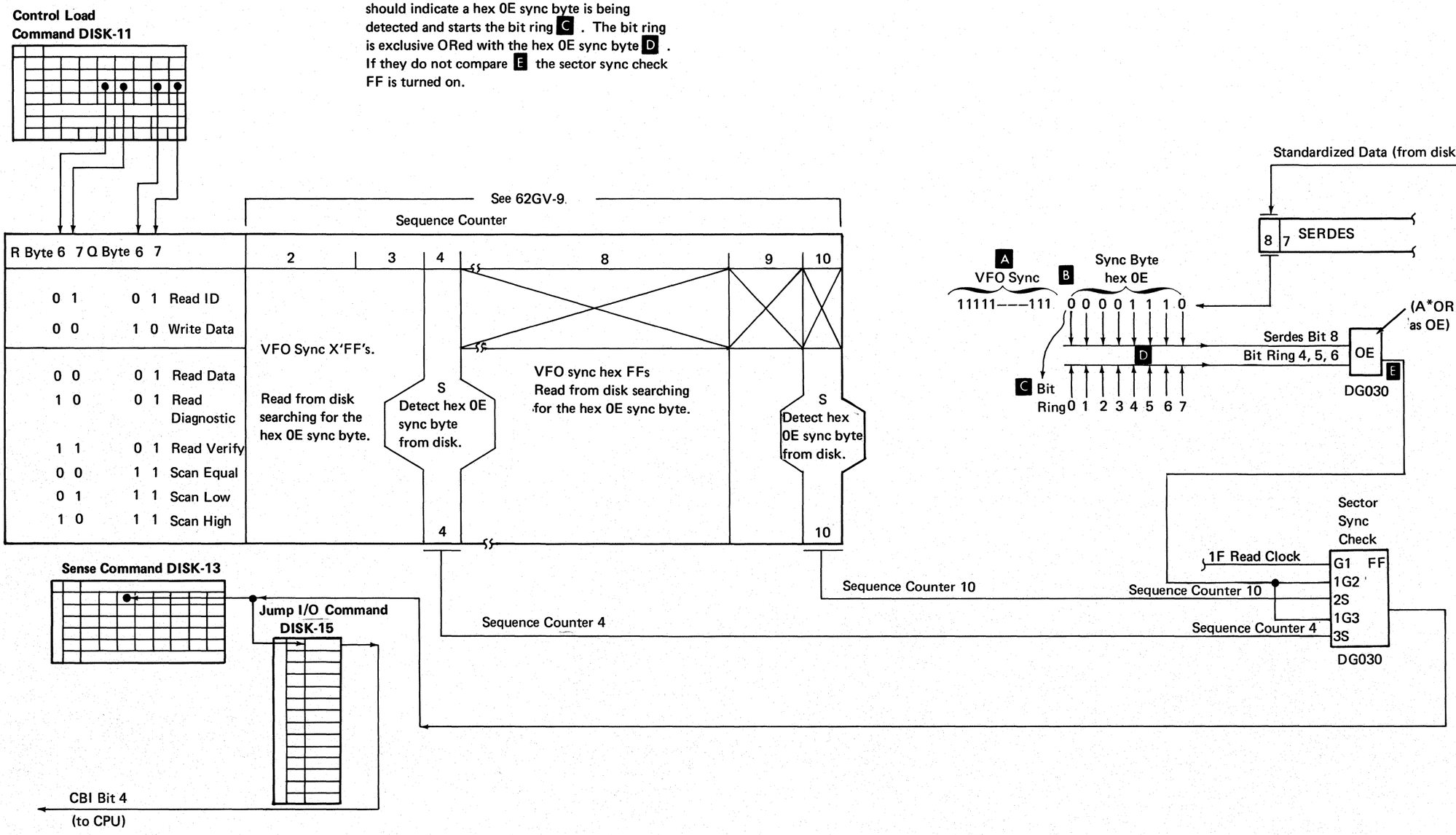
Sector Sync Check

A false sync byte hex 0E is detected.

A sector sync check error condition can be detected when one of the following read or write operations is executing.

Detect a sector sync check if a bit is picked or dropped while searching for or reading the sync byte. A sync byte is detected by comparing the bit ring with sync byte.

VFO hex FFs A are read from the disk through SERDES position 8. The first zero bit B, should indicate a hex 0E sync byte is being detected and starts the bit ring C. The bit ring is exclusive ORed with the hex 0E sync byte D. If they do not compare E the sector sync check FF is turned on.

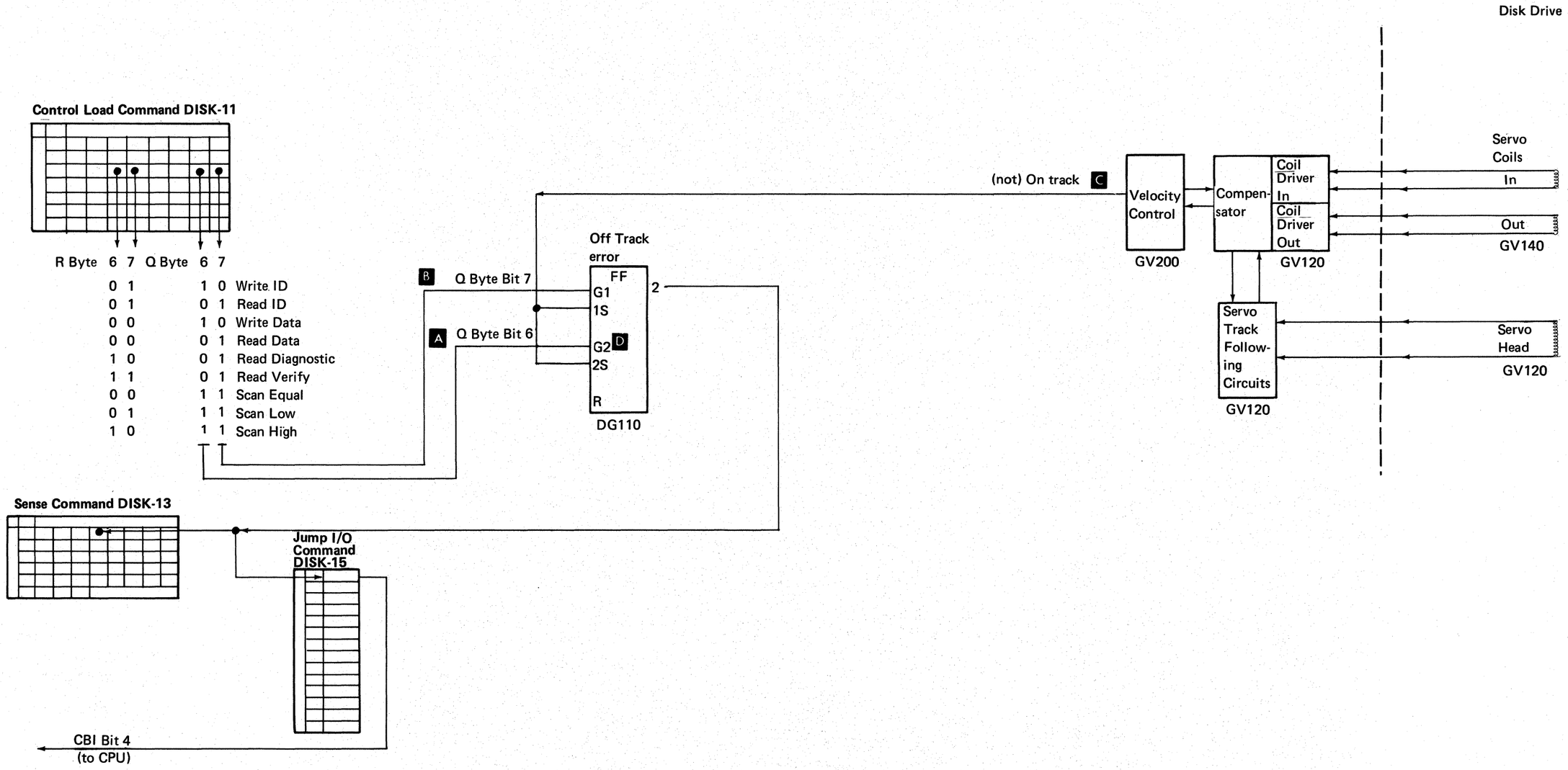


Off Track Check

The disk drive servo arm moves off track during execution of a data operation.

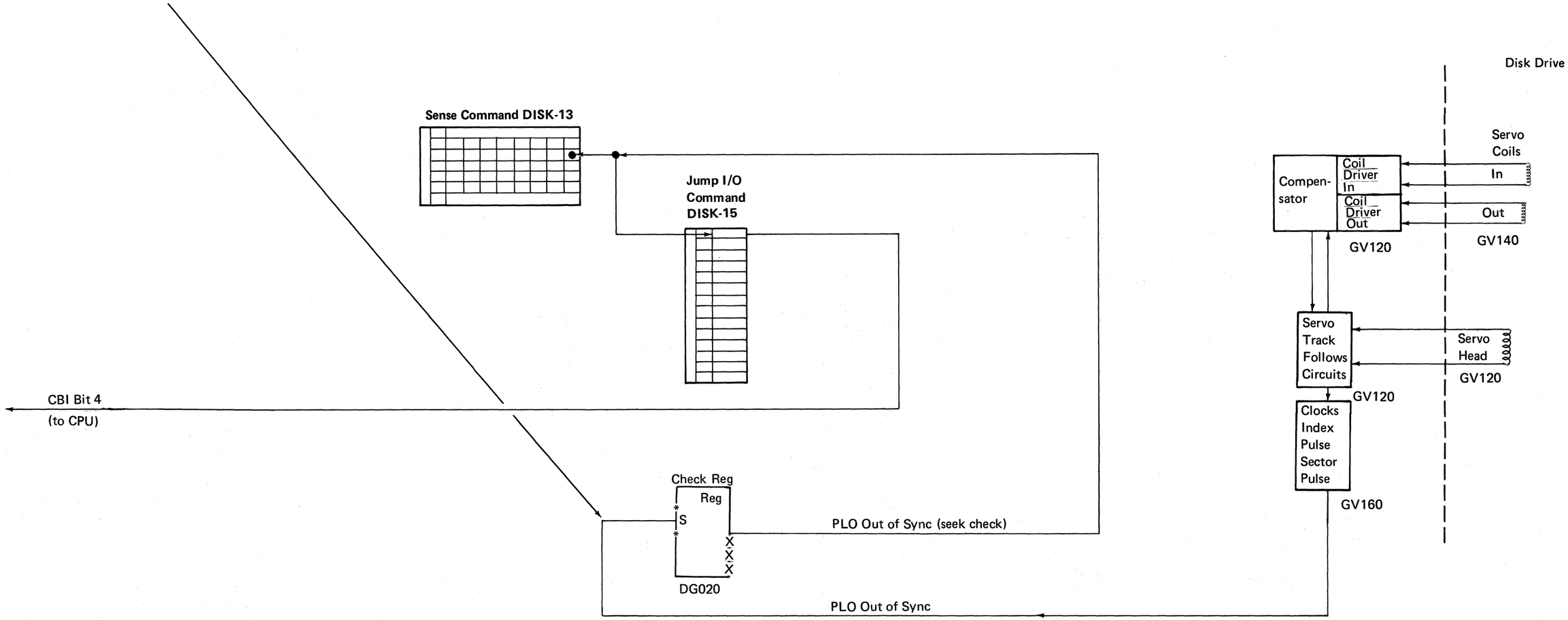
An off track check error condition can be detected when any of the following read or write operations are executing.

During the execution of a read or write operation either Q byte bit 6 A is active or Q byte bit 7 B is active. If the servo goes off track C , an off track error is detected D .



PLO Out of Sync

This line becomes active when there is a loss of four or more servo clock pulses, or a 90° phase error. See DISK-36



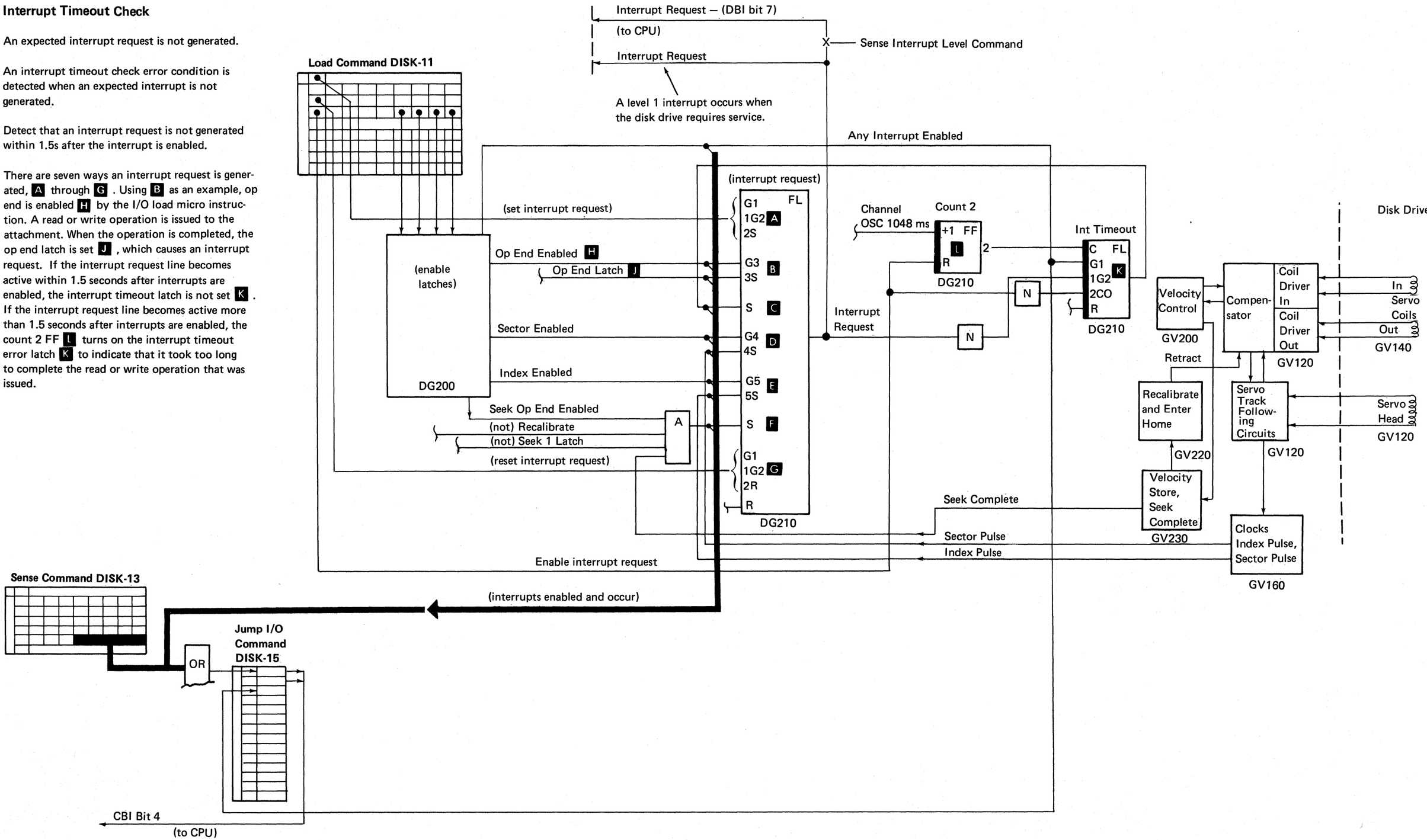
Interrupt Timeout Check

An expected interrupt request is not generated.

An interrupt timeout check error condition is detected when an expected interrupt is not generated.

Detect that an interrupt request is not generated within 1.5s after the interrupt is enabled.

There are seven ways an interrupt request is generated, A through G . Using B as an example, op end is enabled H by the I/O load micro instruction. A read or write operation is issued to the attachment. When the operation is completed, the op end latch is set J , which causes an interrupt request. If the interrupt request line becomes active within 1.5 seconds after interrupts are enabled, the interrupt timeout latch is not set K . If the interrupt request line becomes active more than 1.5 seconds after interrupts are enabled, the count 2 FF L turns on the interrupt timeout error latch K to indicate that it took too long to complete the read or write operation that was issued.



JUMP I/O CONDITIONS

Five jump I/O conditions are shown on this diagram.

- (File) Home — A
- Seek Complete — B
- Index Pulse — C
- File Ready — D
- Data Unsafe — E

A *Home:* An active level on this line indicates that the moving heads are positioned over home (track zero). Home is only active at the end of a power-up cycle or after a recalibrate (not during normal seeks to track zero). An access error which forces the moveable heads into the guard band results in automatic recalibration to track zero and an active level on the 'home' line.

B *Seek Complete:* When the servo head has settled over a track following a seek command, the line goes to a down level. All further seek commands are inhibited until the line returns to an up level. When the moving heads are positioned over a track for longer than 3 ms, 'seek complete' becomes an active level. 'Seek complete' becomes inactive when 'seek 1' becomes active.

C *Index Pulse:* One pulse (2.25 μs nominal) appears on this line for every revolution of the disk.

D *File Ready:* Following a power-on sequence, this line goes to an active level and remains so unless by either a data unsafe condition, a drop in disk speed below 1000 rpm, an active level on the 'brake failure' line, or power off.

Following power up, the 62GV should not be used for read operations until one minute after 'file ready' becomes active, and for write operations until two minutes after 'file ready' becomes active. 'File ready' indicates only that:

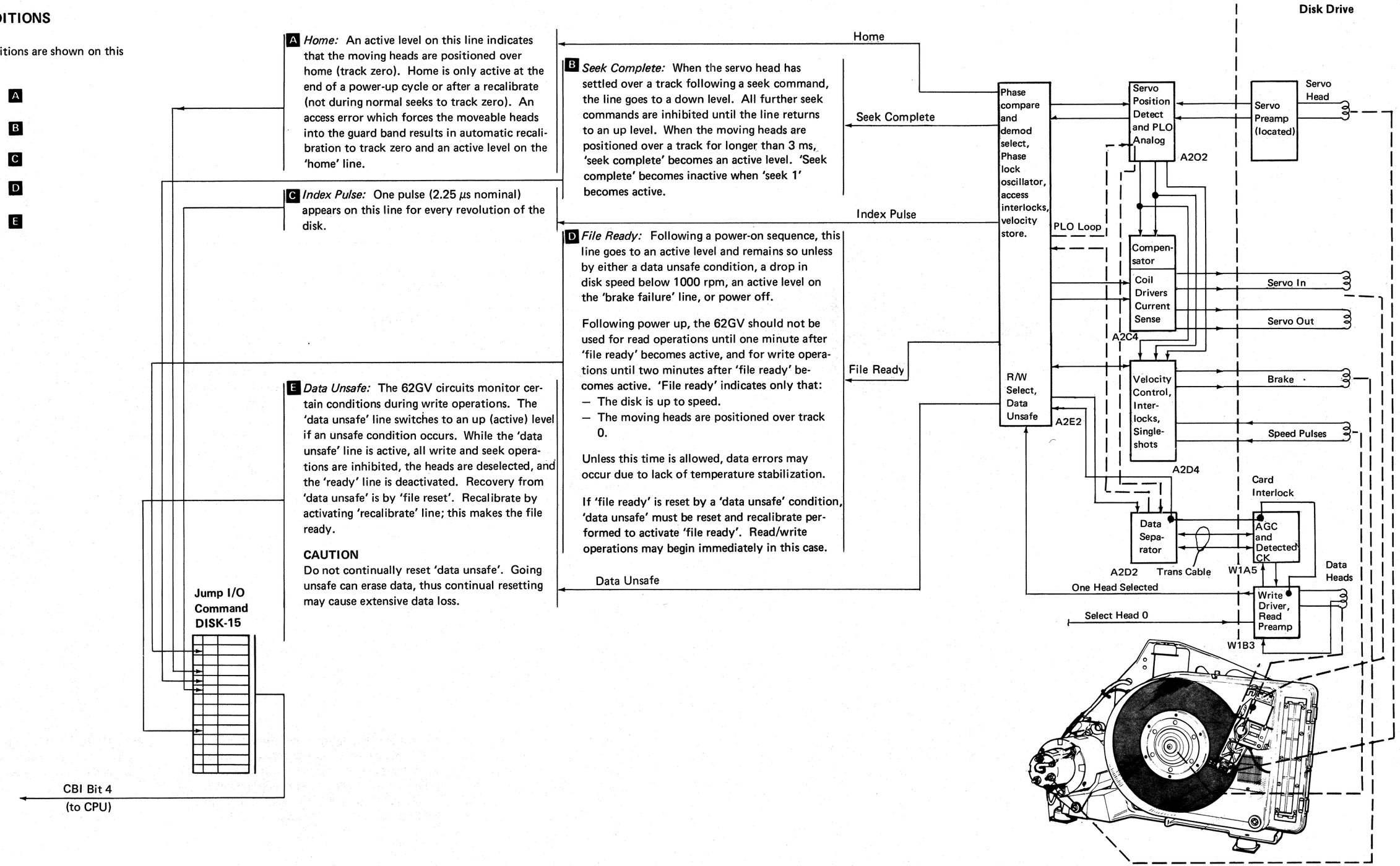
- The disk is up to speed.
- The moving heads are positioned over track 0.

Unless this time is allowed, data errors may occur due to lack of temperature stabilization.

If 'file ready' is reset by a 'data unsafe' condition, 'data unsafe' must be reset and recalibrate performed to activate 'file ready'. Read/write operations may begin immediately in this case.

E *Data Unsafe:* The 62GV circuits monitor certain conditions during write operations. The 'data unsafe' line switches to an up (active) level if an unsafe condition occurs. While the 'data unsafe' line is active, all write and seek operations are inhibited, the heads are deselected, and the 'ready' line is deactivated. Recovery from 'data unsafe' is by 'file reset'. Recalibrate by activating 'recalibrate' line; this makes the file ready.

CAUTION
Do not continually reset 'data unsafe'. Going unsafe can erase data, thus continual resetting may cause extensive data loss.

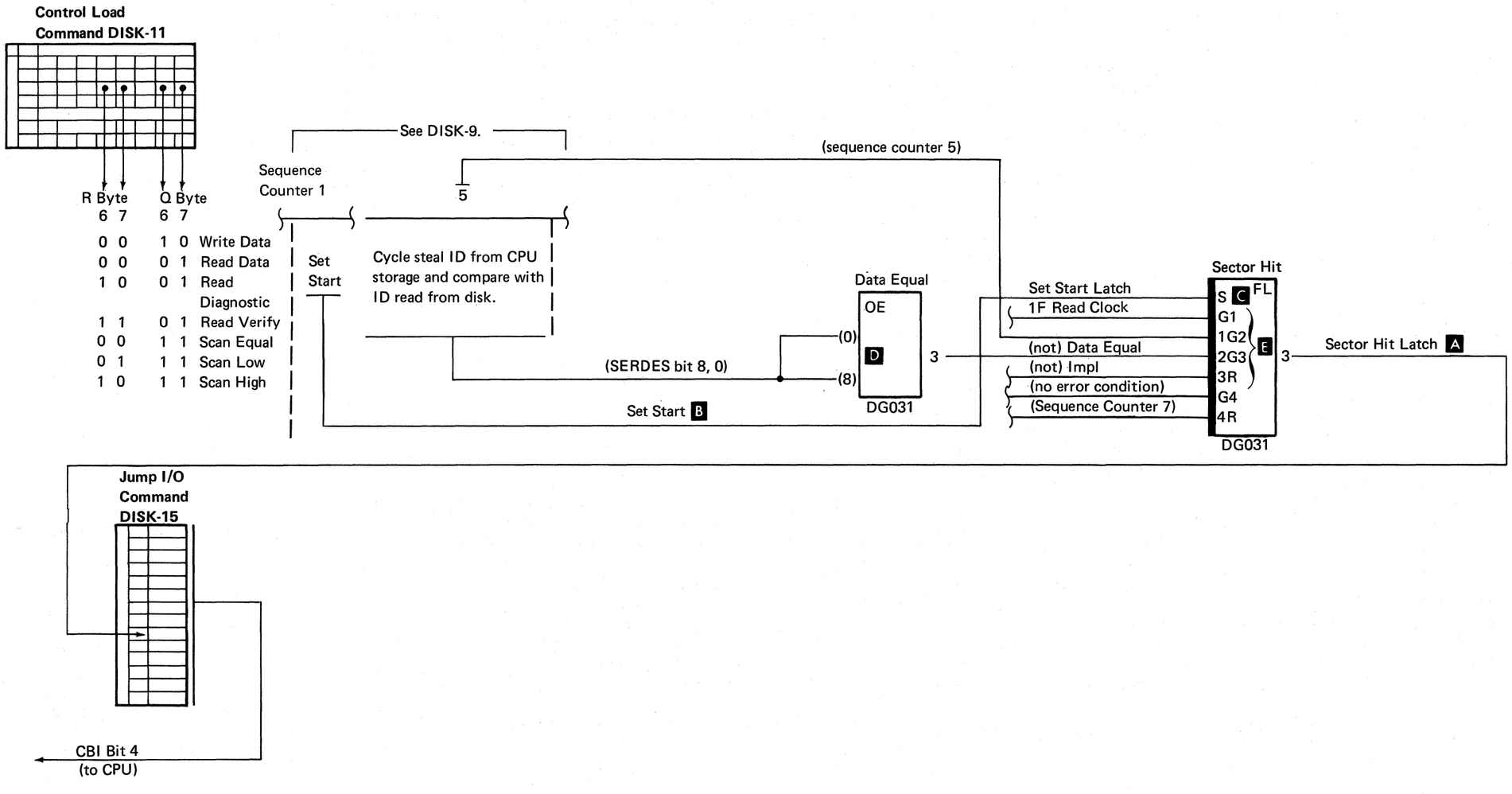


Jump I/O Conditions (Continued)

The sector hit jump I/O condition is tested on this diagram.

Sector hit A means the CPU ID field and the disk ID field compare equal. A sector hit is searched for during the following read or write data operations.

When a data operation is started, 'set start' B turns on the 'sector hit' latch C. During sequence counter 5, ID fields are compared D for equal. If the ID fields compare equal, the sector hit latch stays on. If the ID fields do not compare equal, the sector hit latch is reset F.



Jump I/O Conditions (Continued)

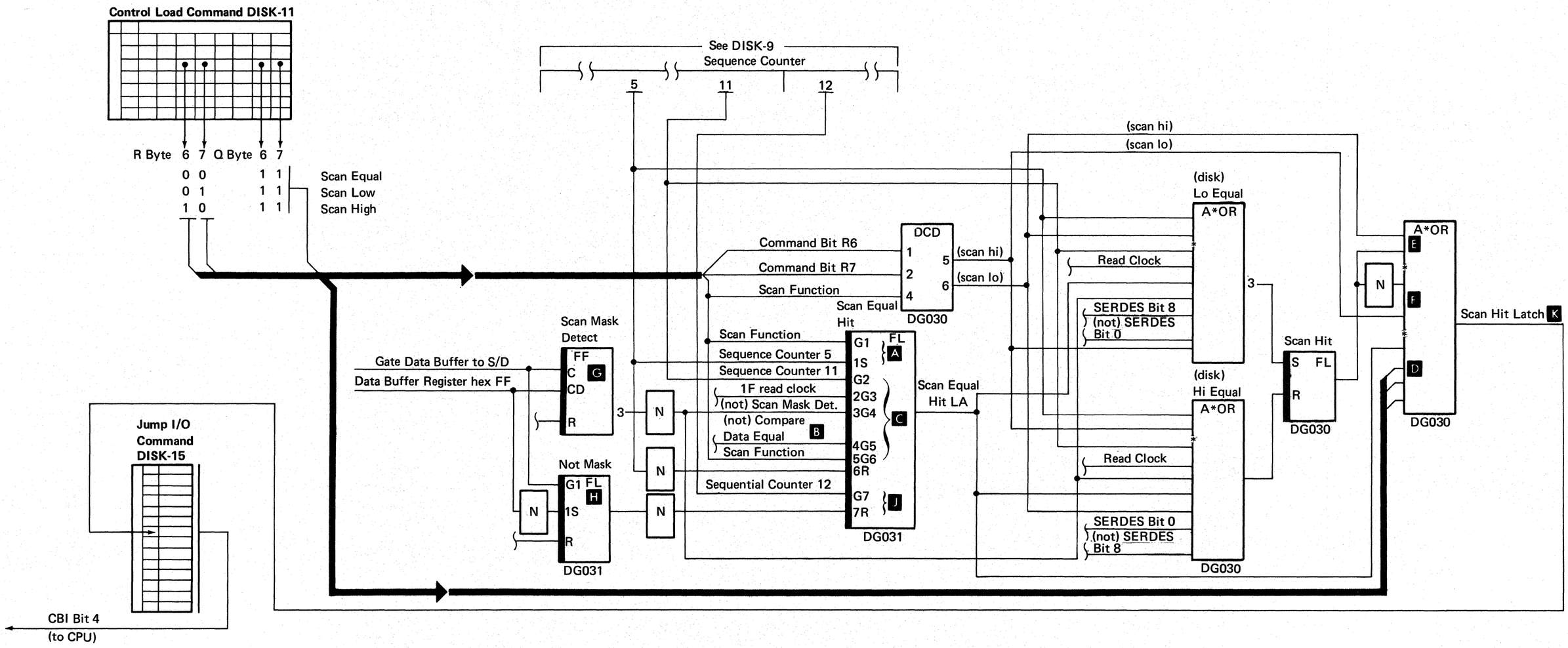
Scan hit K means, the equal condition, the low condition, or the high condition (CPU data field being compared to the disk data field) is met. A scan hit is searched for during the following scan data operations.

During sequence counter 5 of a scan data operation, the scan equal hit latch A is turned on. During sequence counter 11, read data from disk is compared B to read data from CPU storage. If the data is unequal, the scan equal hit latch is reset C . If the data is equal, the scan equal hit latch is not reset, and scan hit D is detected.

During a scan low data operation, if data from the disk compares low to the data from CPU storage, scan hit is detected.

During a scan high data operation, if data from the disk compares high to the data from CPU storage, scan hit is detected F .

If a hex FF is detected from CPU storage, scan mask detect G latch prevents a compare for that byte time. Also, if the 'not mask' latch H is not turned on during a scan data command, it indicates that CPU storage compared data is all hex FFs, therefore, the scan equal hit latch is reset at the end of data compare J .



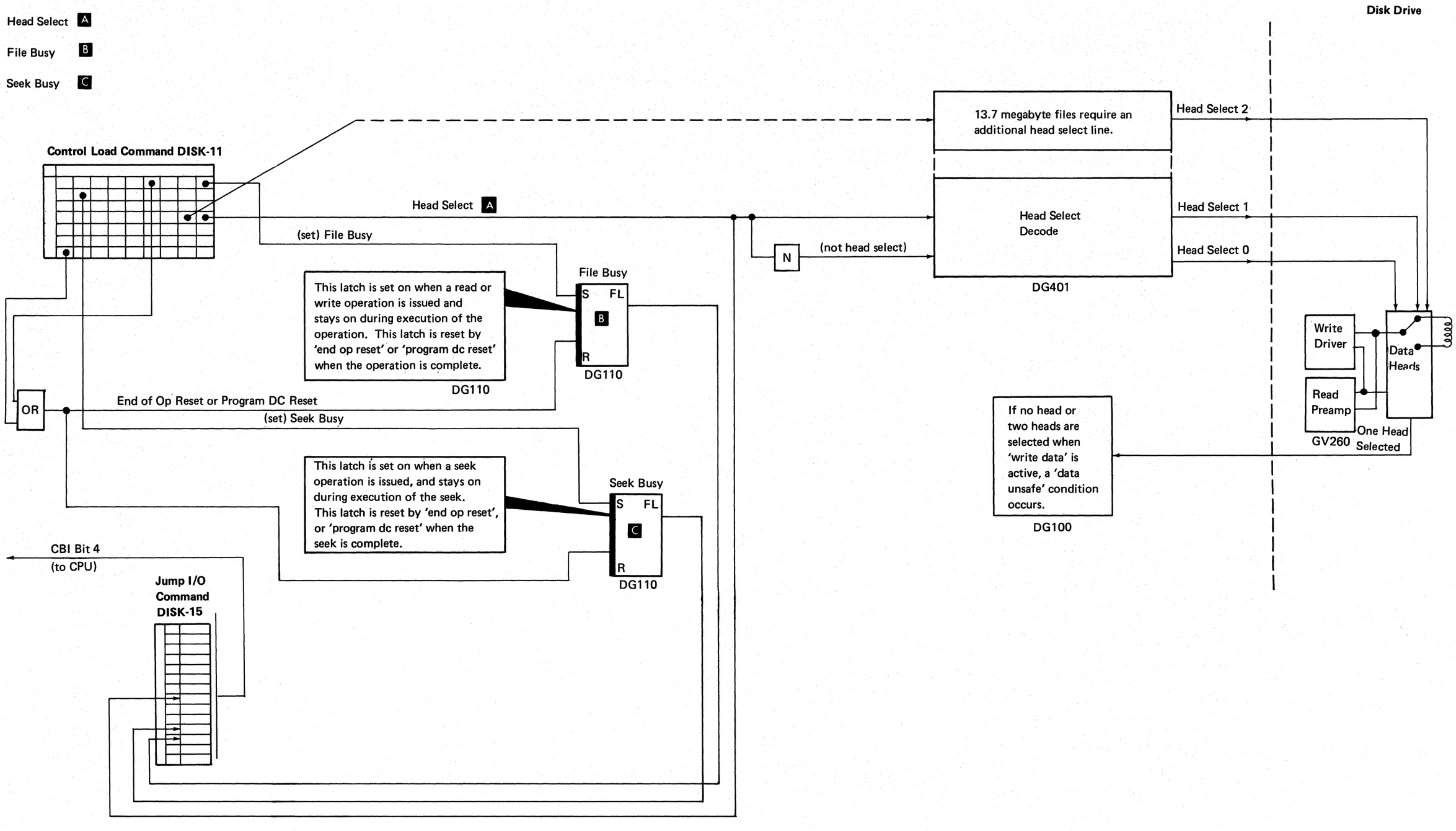
Jump I/O Conditions (Continued)

Three jump I/O conditions are shown below:

Head Select A

File Busy B

Seek Busy C



INPUT/OUTPUT AND SENSE LINES

Output Bus Lines (see DISK-8)

Line	Indicates/Purpose	Cause/Conditions
Standardized Data	Carries data read from the disk and echoes data being written.	
Read Clock 1F		Pulse is derived from the read oscillator.
Data Unsafe	Failure condition.	Brought up by: 'write error', 'head select error', 'servo error', or incorrectly plugged card.
Write Unsafe	Unsafe condition.	Caused by 'write selected' and no write current or by 'write not selected' and 'write current'.
Select Unsafe	Unsafe condition.	Caused by a write selection where more than one head or no head is selected.
Servo Unsafe	Unsafe condition.	Caused by 'write' being selected when the access heads are off track or the PLO is out of sync.
Write Clock 1F	Pulse is used as a reference during 'write'.	Derived from the phase locked oscillator (PLO).
DSF Ready	The DSF is ready to be used.	1. The disk is up to speed. 2. The access heads are at cylinder zero (PWR UP). 3. No 'data unsafe' condition. 4. No electrical failure in the drive motor brake.
Index Pulse	Indicates track starting point.	Active once per revolution.
Home	Heads are at cylinder 0.	Only active after: 1. Power up. 2. Recalibration. 3. An access that forces the heads into the guard band.
Behind Home	Heads are between track 0 and the landing zone.	
Guard Band	Access heads are in the guard band.	
Seek Complete	Access head is at the correct track after a 'seek'.	
On Track	The access heads are at a data track.	
Speed Pulses	Used to calculate disk speed.	Active once per revolution of the disk.
Brake Failure	Electrical failure of the drive motor brake.	

Input Bus Lines (see DISK-8)

Line	Indicates/Purpose	Cause/Conditions
Read/Write Operation	Always active.	
Fast Sync	Gates continuous ones to the read clock to achieve fast synchronization with read data.	
Write	Selects read (inactive) or write (active).	
Select Head	3.2, 5.0 and 9.1 megabyte files use two head select lines. An additional line is used for 13.7 megabyte files.	
Write Zeros	Carries the data to be written on the disk: up for 0, down for 1.	
DSF Reset	Resets latches in the DSF during power up or a reset after an unsafe condition.	
Power On Delay	A power up or down is in operation.	Permits disk to achieve speed before any actions can occur.
Seek 1 Seek 2	Control the start and end of accessing.	
Out Direction	Controls the direction of seeks: active for out, inactive for in.	
Even Track	Directs the access heads to an even-numbered track when active, an odd-numbered track when inactive.	
Recalibrate	Moves the access heads to cylinder 0.	After power on delay or access error.

Sense Lines Used with MAPs (see DISK-8)

Line	Indicates/Purpose	Cause/Conditions
PLO Out of Sync	PLO is not synchronized to the servo clock pulses.	
Select Out Drive	Actuator is driven away from the spindle.	
Select In Drive	Actuator is driven toward the spindle.	
VFL (velocity follow latch)	Actuator has reached its normal velocity.	Used after an initial acceleration period.
Linear Region	Servo head is over a track.	Derived from the error signal which is generated when the access arm moves across a track.
Sector Pulse	Beginning of each sector.	Derived from the servo track. Sector 0 uses the index pulse.
Too Fast	Slows the arm during access.	A composite signal from desired and actual access arm velocity.

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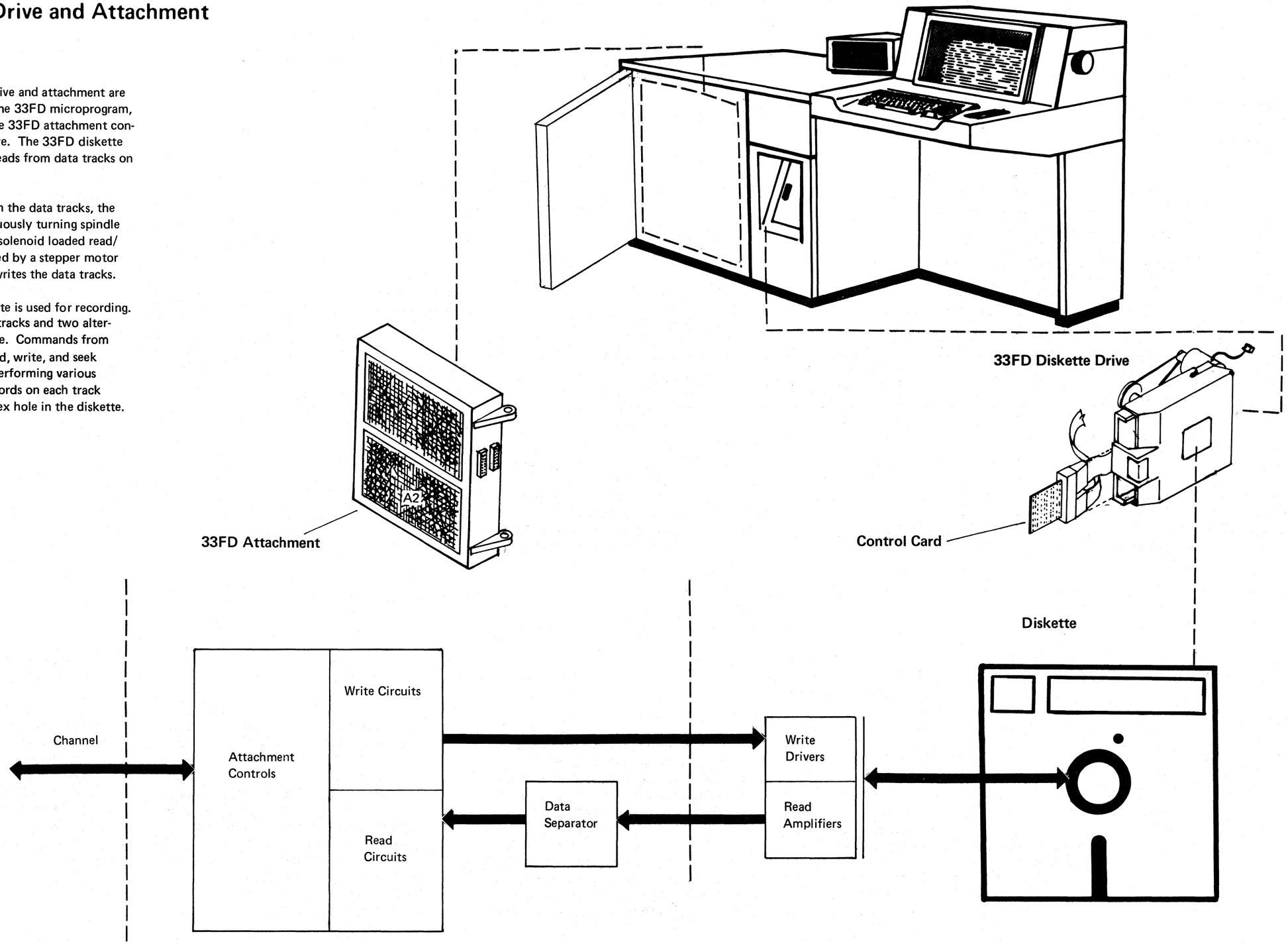
33FD Diskette Drive and Attachment

The IBM 33FD diskette drive and attachment are mounted in the system. The 33FD microprogram, located in the CPU, and the 33FD attachment control the 33FD diskette drive. The 33FD diskette drive seeks, writes on, or reads from data tracks on a removable diskette.

In order to read or write on the data tracks, the diskette drive has a continuously turning spindle that turns the diskette. A solenoid loaded read/write head that is positioned by a stepper motor driven leadscrew reads or writes the data tracks.

Only one side of the diskette is used for recording. There are 75 primary data tracks and two alternate data tracks per diskette. Commands from the channel initiate the read, write, and seek operations in addition to performing various control functions. The records on each track are referenced from an index hole in the diskette.



Diskette Format

There are 77 tracks on the diskette surface; a track being a circular path on the surface of the diskette. The tracks are numbered 00 through 76. Track 00 is the outside track and track 76 is the inside track. Of the 77 tracks, only 74 tracks are data tracks. Track 00 is a label track and tracks 75 and 76 are reserved as alternates to be used in place of tracks that become defective. Some diskettes that are interchanged with other systems may contain only 73 data tracks; track 74 not being used.

Each track is divided into either 8 or 26 sectors. The content of each sector is described in the illustrations on this page.

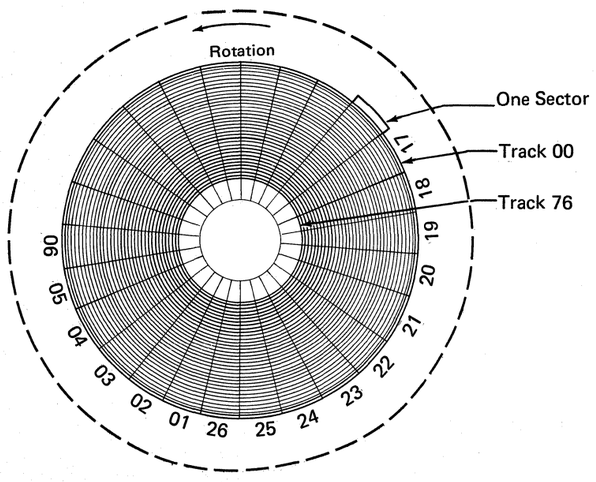
The data stored in one sector is called a record. When the tracks are divided into 8 sectors, each record contains 512 bytes; when divided into 26 sectors, each record contains 128 bytes. Thus, diskettes that contain 74 data tracks and are divided into 8 sectors per track have a capacity of 303,104 bytes of data; those divided into 26 sectors have a capacity of 246,272 bytes of data.

In some diagnostic programs only one sector is written on a track. Each sector contains 4096 bytes of data.

The formula for record length is 128×2^n where n can be 0, 1, 2, 3, 4, or 5. Thus record lengths can be 128, 256, 512, 1024, 2048, or 4096 bytes long. The value of n is recorded in the record length byte.

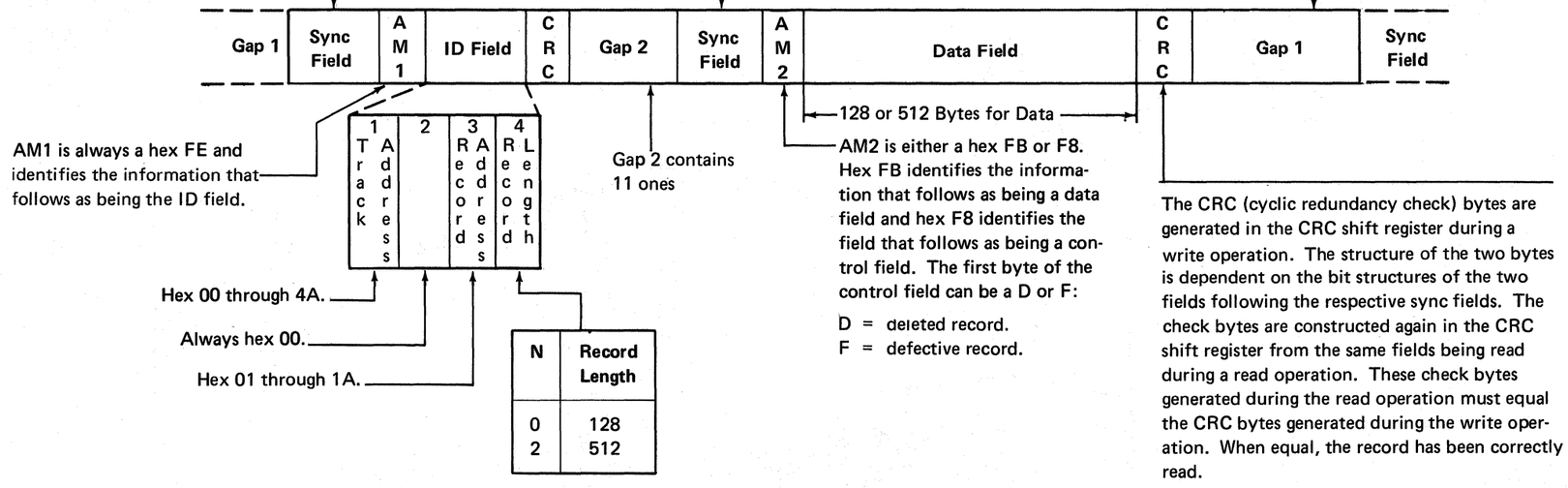
Because the diskette is formatted into tracks and sectors, each record on the diskette has a definite address consisting of a track and record address. The record address is recorded at the records physical location on the diskette.

Diskettes that contain prerecorded record addresses are known as initialized diskettes. Initialized diskettes contain an ID field for each record. Each record consists of two parts; the first part contains identification information and the second part contains data.



26 Sector Diskette

Each sync field contains 6 bytes of zeros. This field is required to synchronize the attachment circuitry to the information being read from the diskette.



N	Record Length
0	128
2	512

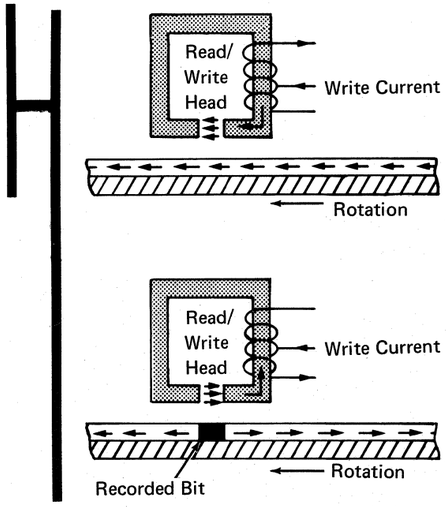
Gap 1 consists of a variable number of zeros or ones; the number being dependent on the diskette speed. The last gap before index consists of zeros; the rest of the gaps consist of ones.

The CRC (cyclic redundancy check) bytes are generated in the CRC shift register during a write operation. The structure of the two bytes is dependent on the bit structures of the two fields following the respective sync fields. The check bytes are constructed again in the CRC shift register from the same fields being read during a read operation. These check bytes generated during the read operation must equal the CRC bytes generated during the write operation. When equal, the record has been correctly read.

Read/Write Circuit Principles

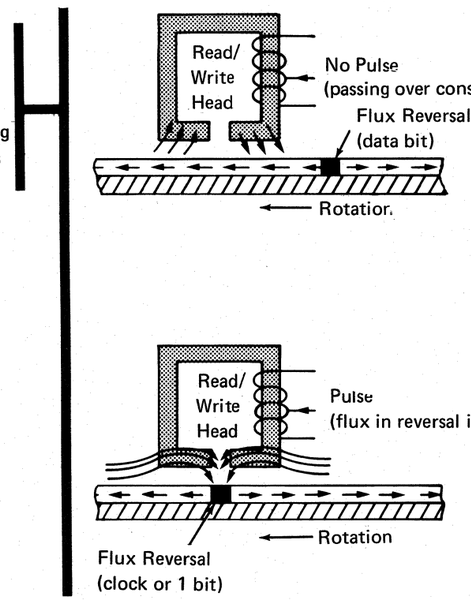
Writing

During a write operation, a clock or 1 bit is recorded by reversing the direction of the current in the coil, which reverses the flux direction in the pole piece and reverses the flux in the gap. At the instant that the flux in the pole piece gap reverses, the direction of magnetization changes on the diskette surface. Each reversal represents a recorded clock or 1 bit.



Reading

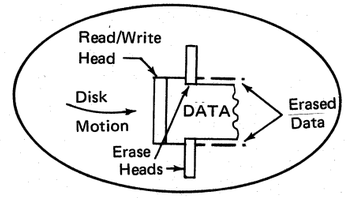
During a read operation, with the recording surface magnetized in one horizontal direction, constant flux flows and the coil registers no output voltage. However, when a recorded bit (180 degrees horizontal flux reversal) passes the gap, the flux flowing through the ring and coil also reverses and produces a voltage output pulse.



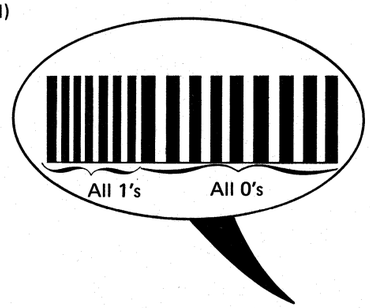
Controls

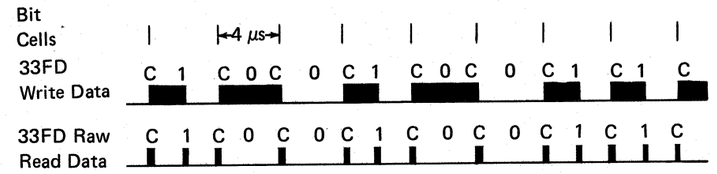
'Gated wt current gate' **A** is active during a write operation. This line allows current to flow through the read/write head **B** and also degates the read circuits. When write gate is inactive, the write circuits are deconditioned and the read circuits are conditioned to read.

'Gated tunnel erase' **C** is also active during a write operation. This causes the edges of the data track to be erased. The edges are erased to provide a gap between tracks and to ensure that old data is completely erased.



'33FD low wt current' **D** is under microprogram control and is active from logical track 42 on up to 76. When this line is active, the current through the write head is reduced.



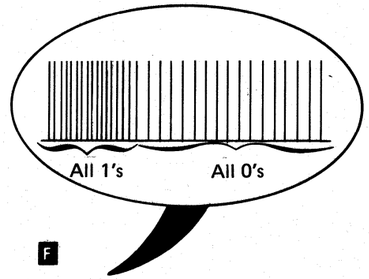


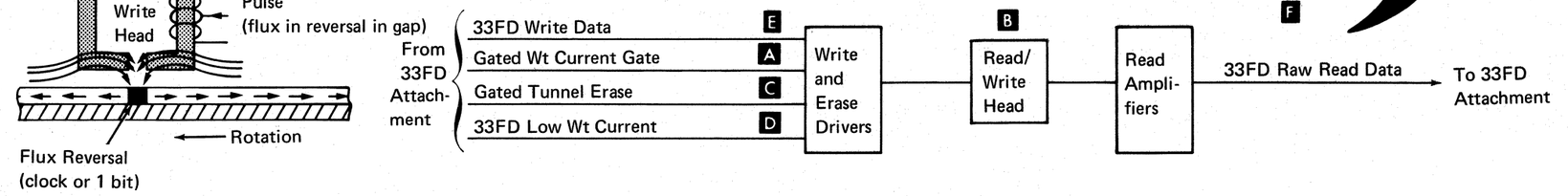
The above 1001 0011 represents a hex 93.

Data Representation

For each transition of the '33FD write data' line **E** a clock bit or a 1 bit is written on the diskette. The absence of a change between clock bits represents a zero or a no-bit. Transitions of the write data line cause the current to be switched in the read/write head which results in a polarity change on the diskette track. Thus a polarity change on the diskette represents a clock bit or a 1 bit. The period of time from one clock bit to the next clock bit is known as a bit cell and is a nominal 4 µs in length. Data bits are written in the middle of the data cell.

By comparison, bits represented on the 'write data' line as transitions are represented on the '33FD raw read data' line **F**, when read, as positive pulses with a nominal width of 150 ns. The separation of clock bits and data during a read operation takes place in the VFO card in the 33FD attachment circuits.





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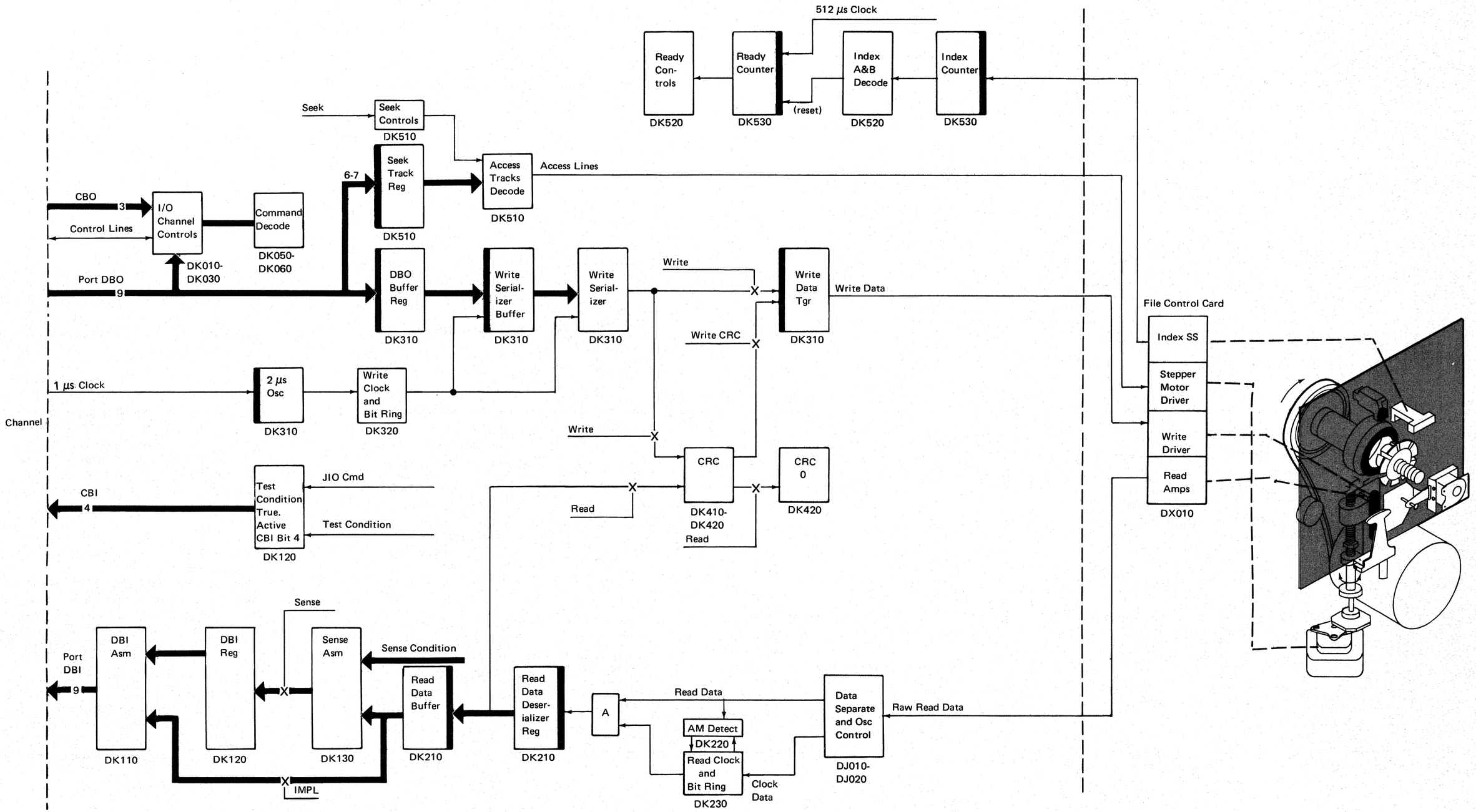
33FD Data Flow



Seek Operations

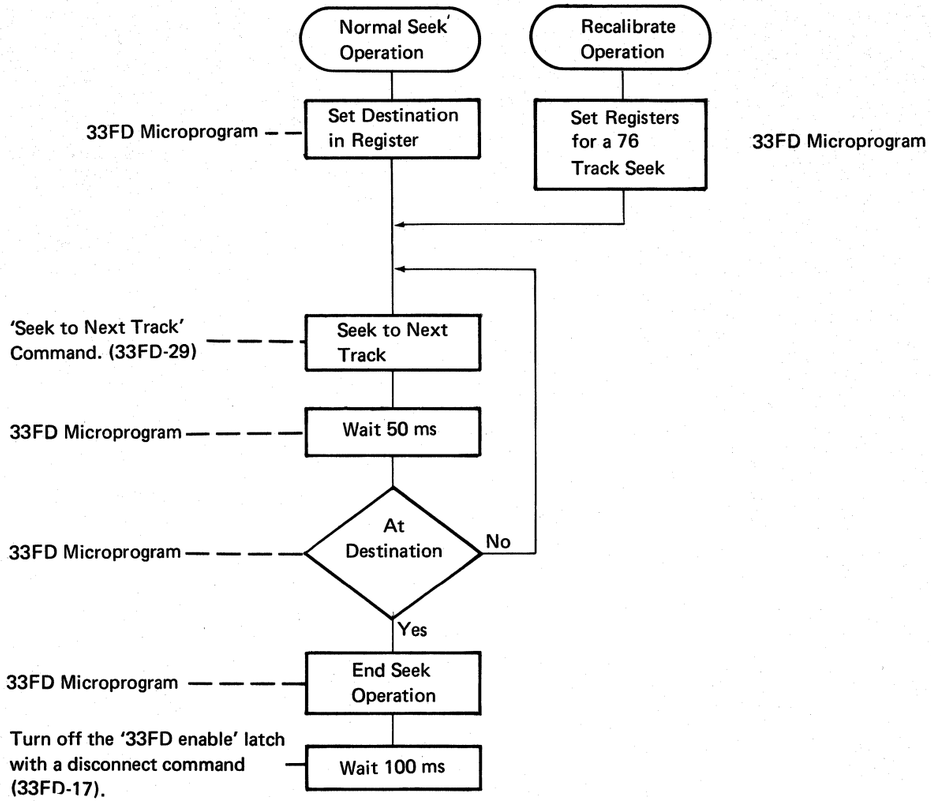
The 33FD seek operations are:

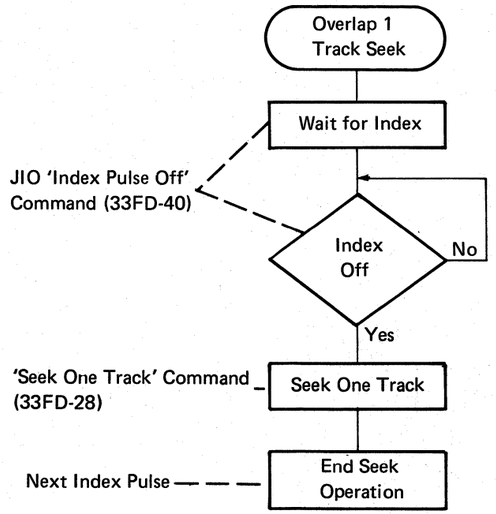
- Normal: Seek from present known track to a specified destination track.
- Recalibrate: Seek from the present location (might be unknown) to track zero.
- Overlap: This seek is used when dumping the 62GV onto the 33FD diskettes.

In all three cases, the microprogram controls the operation. The microprogram must know the track location of the head before starting the operation (except for recalibration), and also know the destination track. Seek commands that move the head one track per command are issued until the destination is reached or the operation is terminated.

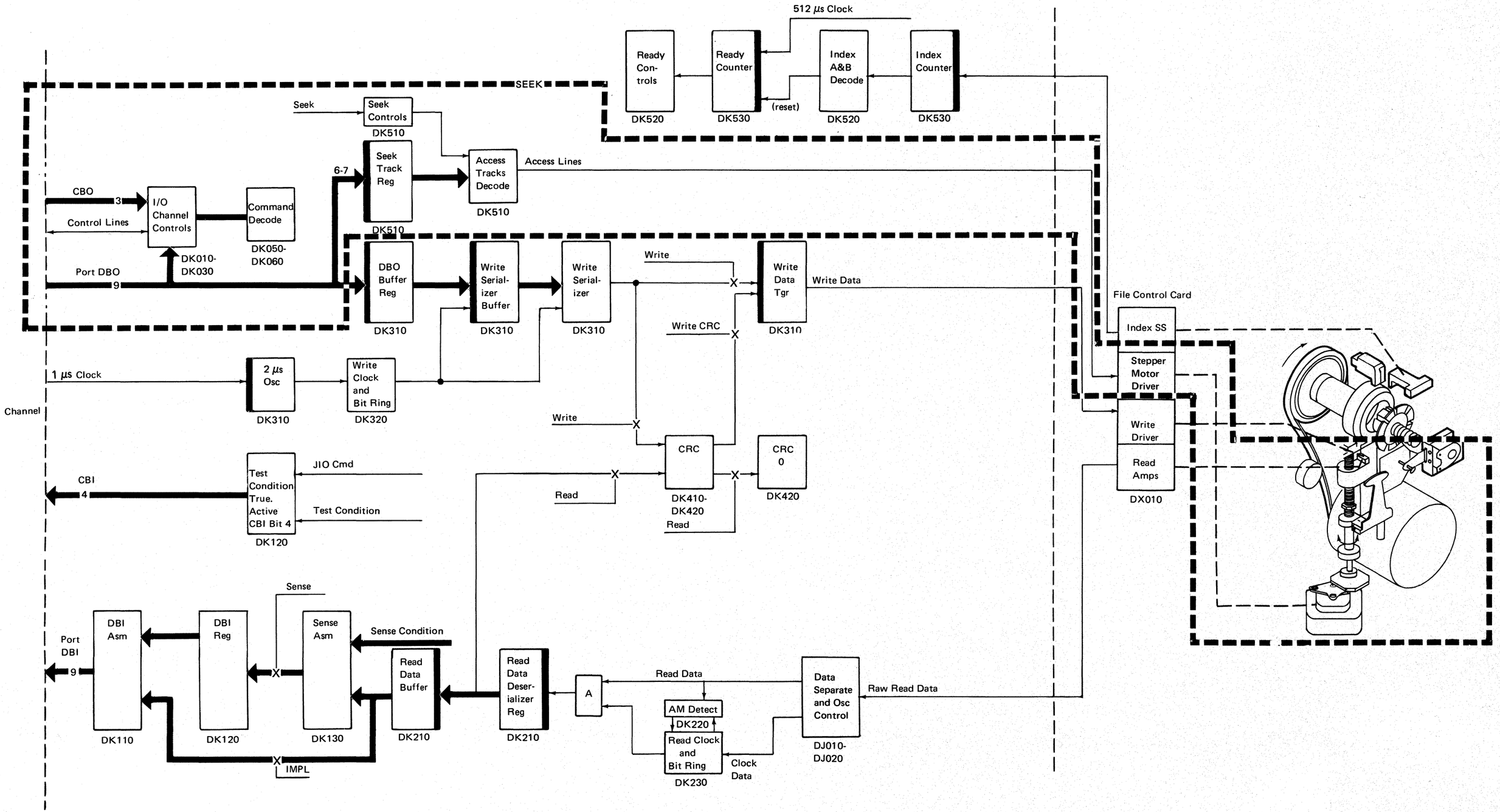
The recalibration operation is necessary when the track location of the head is unknown. The 33FD microprogram sets up a seek of 76 tracks. Because there are only 77 tracks on the diskette, this is just enough to drive the head to track zero from any location. After arriving at track zero, the access mechanism comes against a final stop and even though seek commands continue to be issued, the head remains at track zero.

The overlap seek is one track seek and starts just after index time. The operation is terminated after one revolution of the diskette, at the next index time. During the time this seek is in progress, data can be gathered from the 62GV and if available, is written during the next revolution of the diskette.





Seek Data Flow



Read Operation

The accompanying flowchart describes the reading of one sector from the diskette. As each byte is read, one micro instruction is required to transfer each byte from the attachment to the channel. The data flow for the read operation is shown on the next page.

After the reading of bytes has started, the microprogram must take the bytes at a nominal rate of 1 byte every 32 μs. A failure to take the bytes fast enough causes a read overrun.

The major control in the attachment that defines the read operation is the 'read data command' latch. This latch is on twice to read one sector (assuming a good ID field and data field); once to find and read the ID field, and once to find and read the data field. In both cases the 'read data command' latch remains on until the CRC bytes are read.

The read clock and read bit ring synchronize the attachment to the data being read. The read clock runs continously except in diagnostic step mode. The read bit ring however only runs from the time an AM byte is found until after the CRC bytes have been read.

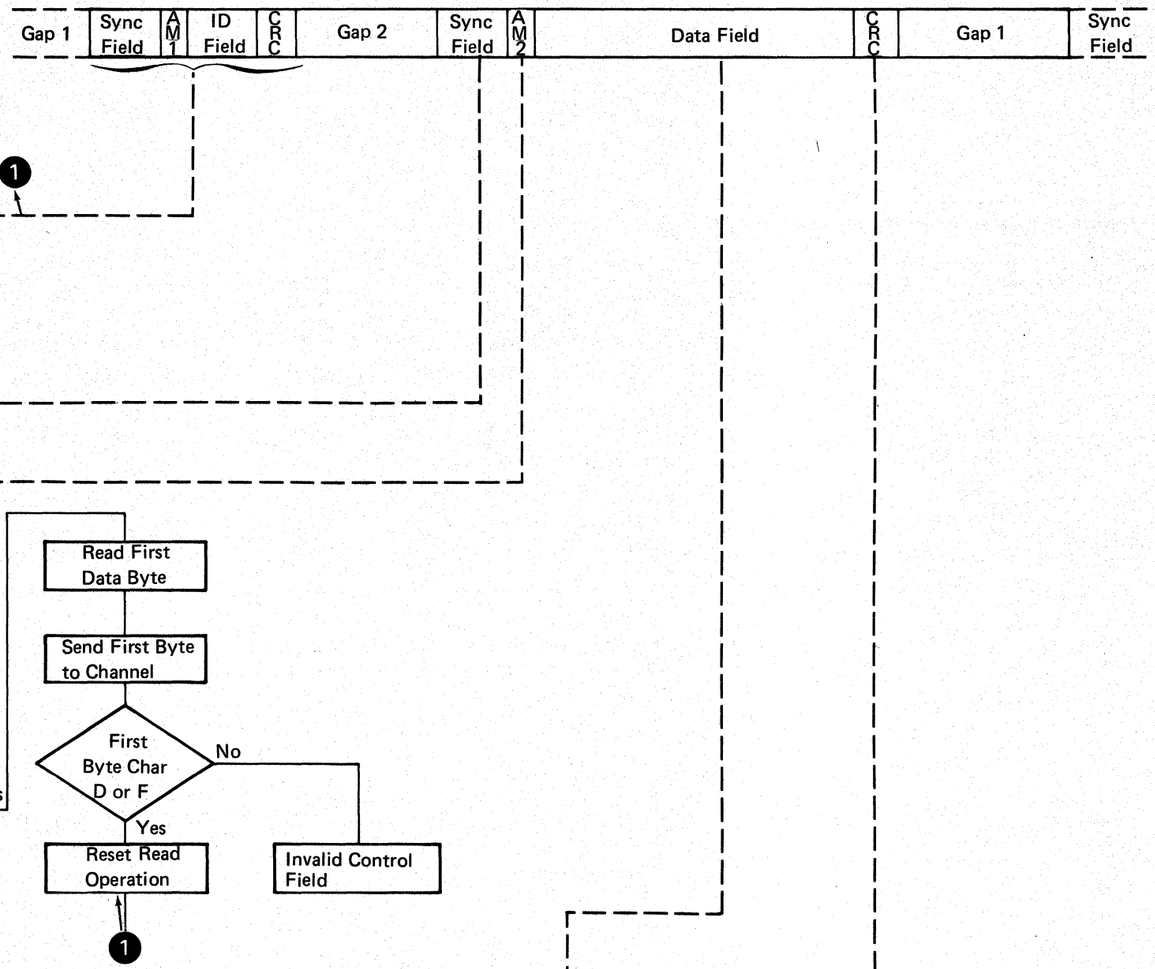
The 'byte sync found' latch turns on when the first data bit of the AM is read. This latch remains on until the 'read data command' latch is reset or until the attachment has determined the byte being read is not a valid AM.

Valid AMs are hex F8, FB, or FE without read clock pulses at bit ring 2, 3, and 4 time. The attachment considers an invalid AM as one that:

1. Is missing data bits 1, 2, 3, or 4.
2. Is missing a clock bit at bit ring 1, 5, 6, or 7 time.
3. Has a clock pulse at bit ring 2, 3, or 4 time.

The first data byte following a control AM can be either a D or a F:

D = Deleted record
F = Defective record



See *Find ID Operation* on 33FD-12.

The 'search for AM byte' command (33FD-30) initiates the operation by turning on the 'read data command' latch.

Six bytes of zeros in the sync field allow the bit synchronization; bits read from the diskette can be identified as clock bits or data bits. After reading the 6 bytes of zeros, all positions of the CRC shift register will be off.

The first data bit of the AM byte turns on the 'byte sync found' latch and allows the bit ring to start. This gives byte synchronization; data bits can then be identified as a particular data bit (0 through 7).

A check is made in the attachment to determine whether the AM byte read is any valid AM byte. If not, the 'byte sync found' latch is reset, and the attachment looks for the next AM.

The AM byte is sent to the channel using the 'sense data byte' command (33FD-34).

The 33FD microprogram determines whether the AM is a control AM, data AM, or neither (Table 1). If a control AM, the first byte of the data field is sent to the channel using the 'sense data byte' command (33FD-34).

The data field and CRC bytes are sent to the channel using the 'sense data byte' command (33FD-34). CRC data is accumulated.

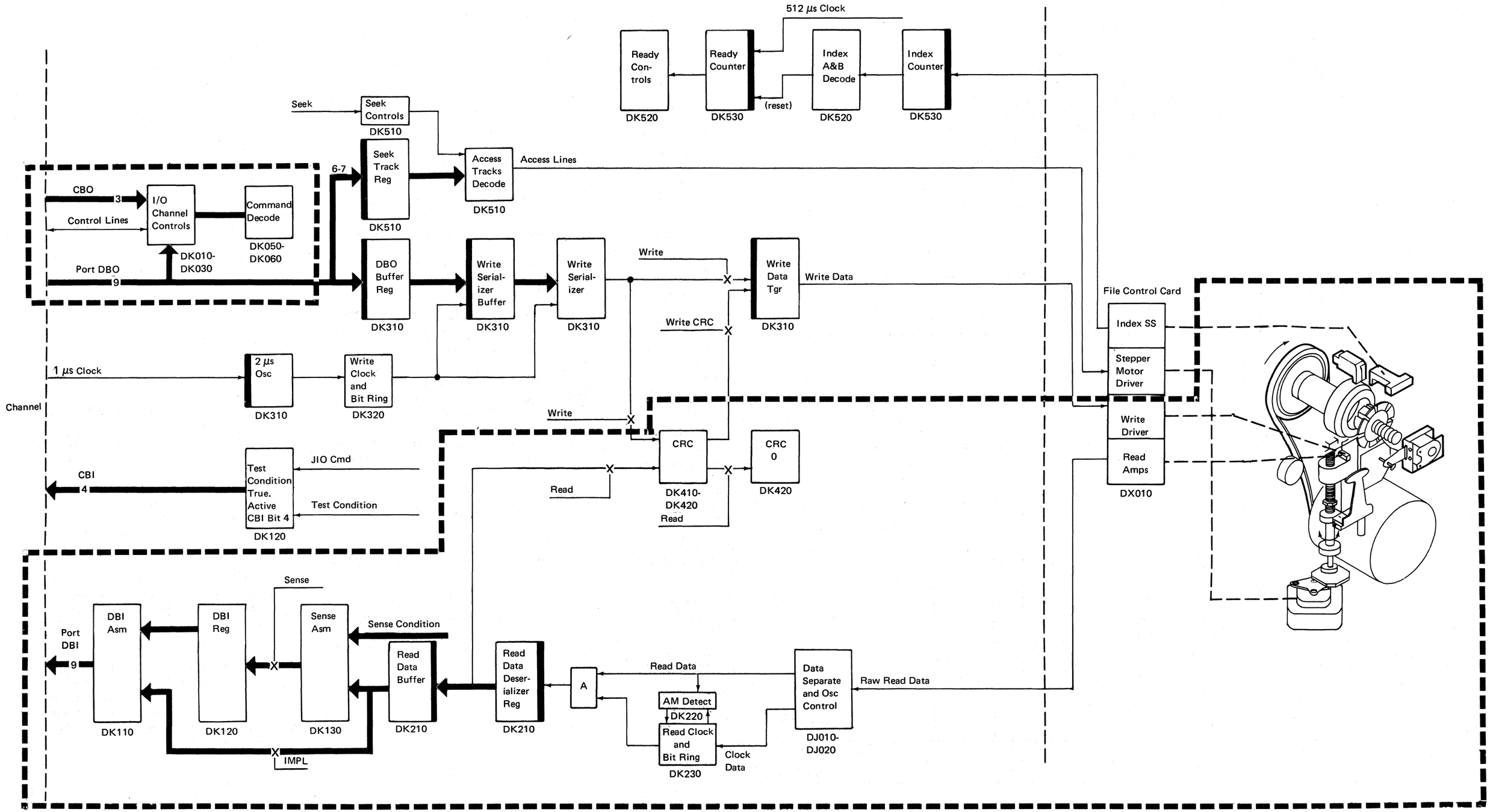
Note: The CRC bytes are allowed to go to the CPU but are not used there.

The attachment portion of the read operation is terminated by issuing a 'reset sector op' command (33FD-41). This resets the 'read data command' latch.

Table 1

AM	Explanation
F8	Field that follows is a control field.
FB	Field that follows is a data field.
FE	Field that follows is an ID field.

Read Data Flow



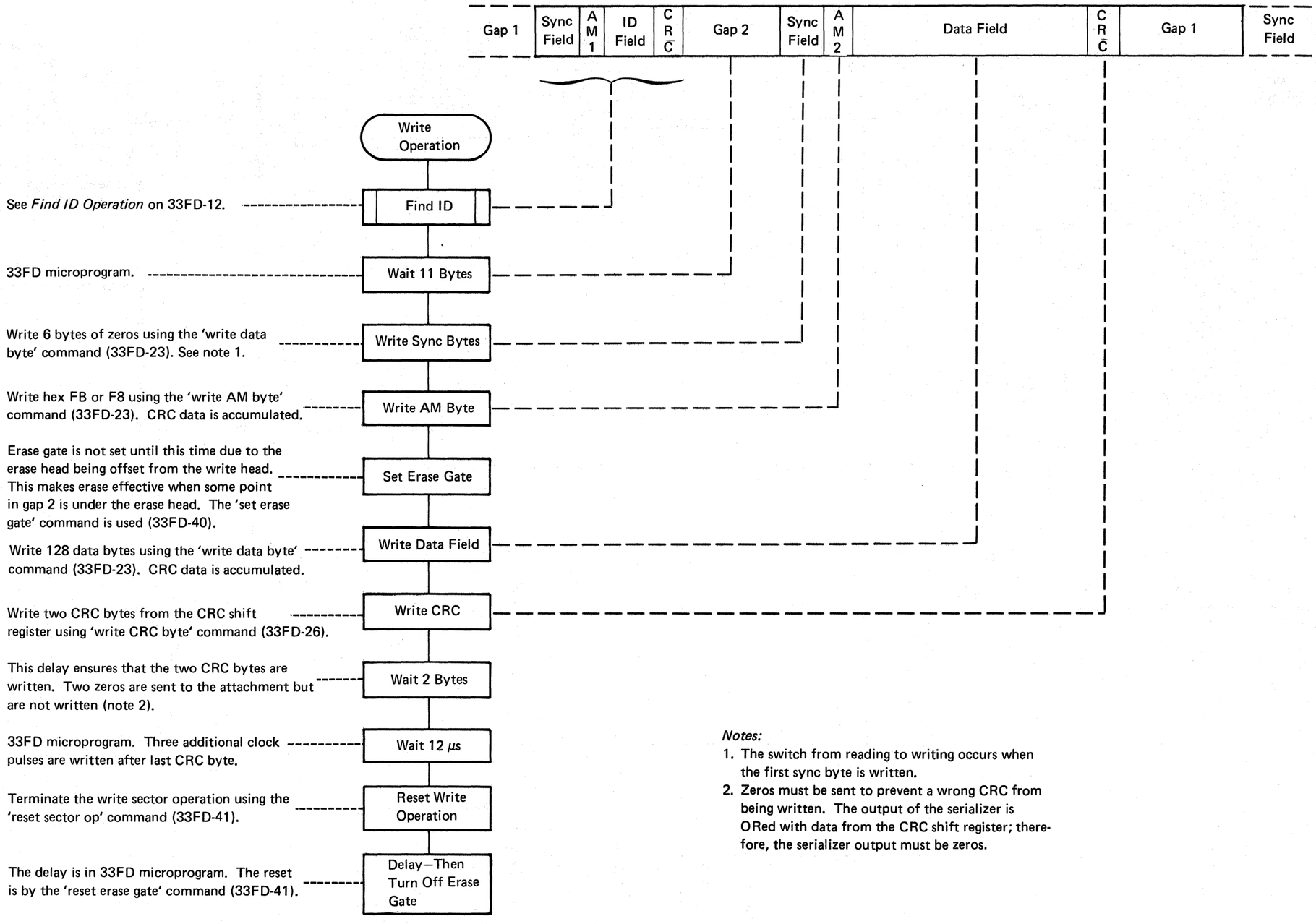
Write Operation

The accompanying flow chart describes the writing of one sector on the diskette. The structure of the fields written are controlled by the 33FD microprogram to the extent that one I/O micro instruction is required for each byte written. The microprogram also controls the required delays. The data flow for the write operation is shown on the next page.

After the writing of bytes has started, the microprograms must supply bytes fast enough so they may be written every 32 μs. A failure to provide bytes fast enough results in a write overrun.

The major control in the attachment that defines the write operation is 'write gate'. This remains active from the time the first sync byte is written until after the last CRC byte is written. The write clock and write bit ring runs as long as 'write gate' is active.

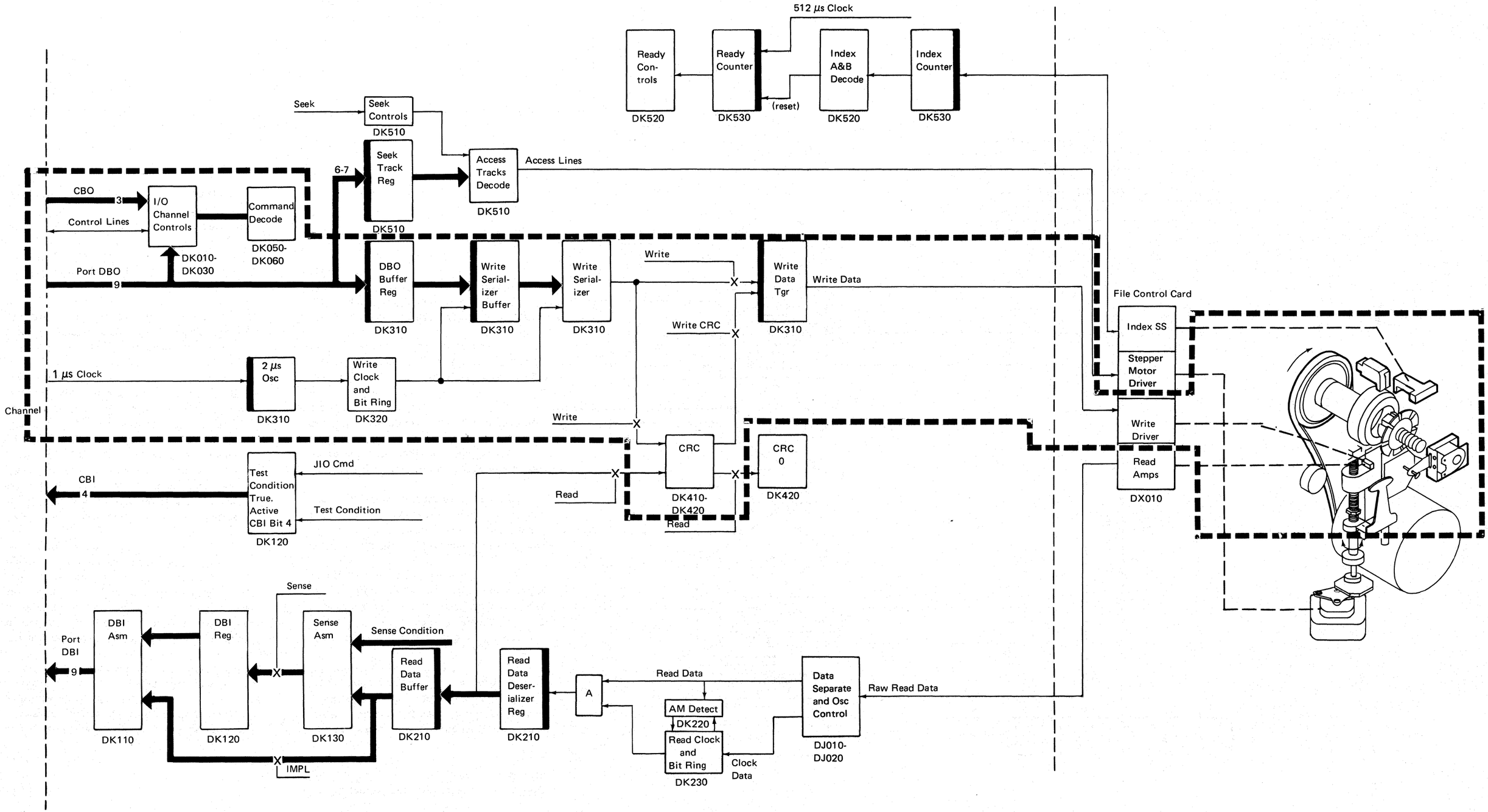
Verification of the write operation is accomplished by reading the record that was written and comparing it to the original data.



Notes:

1. The switch from reading to writing occurs when the first sync byte is written.
2. Zeros must be sent to prevent a wrong CRC from being written. The output of the serializer is ORed with data from the CRC shift register; therefore, the serializer output must be zeros.

Write Data Flow



Find ID Operation

Find ID operations:

- Synchronize the read clock and read bit ring with the bits being read from the diskette.
- Find an ID field.
- Comparison of ID field being searched for and the one found is made by the 33FD microprogram.

The accompanying flowchart describes the find ID operation. This operation can be started with the heads at any position on the diskette. The operation continues reading from the diskette until a valid AM is found or until the microprogram has determined the ID being searched for is not on the cylinder being read.

The major controls in the attachment that define the find ID operation are the 'read data command' latch (DK220) and the 'byte sync found' latch. The 'read data command' latch remains on until the last CRC byte of the ID field has been read. The 'byte sync found' latch turns on when the first data bit of the AM is read. This latch stays on until the 'read data command' latch is reset or until the attachment has determined the byte being read is not a valid AM.

Valid AMs are hex F8, FB, or FE without read clock pulses at bit ring 2, 3, and 4 times (Table 1). The attachment considers an invalid AM as one that:

- Is missing data bits 1, 2, 3, or 4.
- Is missing a clock bit at bit ring 1, 5, 6, or 7 times.
- Has a clock pulse at bit ring 2, 3, or 4 times.

The controls for the find ID operation are on DK220.

The 'search for AM byte' command (33FD-30) initiates the operation by turning on the 'read data command' latch.

Six bytes of zeros in the sync field allow for bit synchronization; bits read from the diskette can be identified as clock bits or data bits. After reading the 6 bytes of zeros, all positions of the CRC shift register will be off.

The first data bit of the AM byte turns on the 'byte sync found' latch and allows the bit ring to start. This gives byte synchronization; data bits read from the diskette can be identified as a particular data bit (0 through 7).

A check is made in the attachment to determine whether the AM byte read is any valid AM byte. If not, the 'byte sync found' latch is reset and and the attachment looks for the next AM.

The AM byte is sent to the channel using the 'sense data byte' command (33FD-34).

The 33FD microprogram determines whether the AM is an ID AM.

The ID field and the CRC bytes are sent to the channel using the 'sense data byte' command (33FD-34). CRC data is accumulated.

The attachments portion of the find ID operation is terminated by issuing a 'reset sector op' command (33FD-41). This resets the 'read data command' latch.

33FD microprogram.

Reset the '33FD enable' latch by issuing a 'disconnect' command (33FD-17).

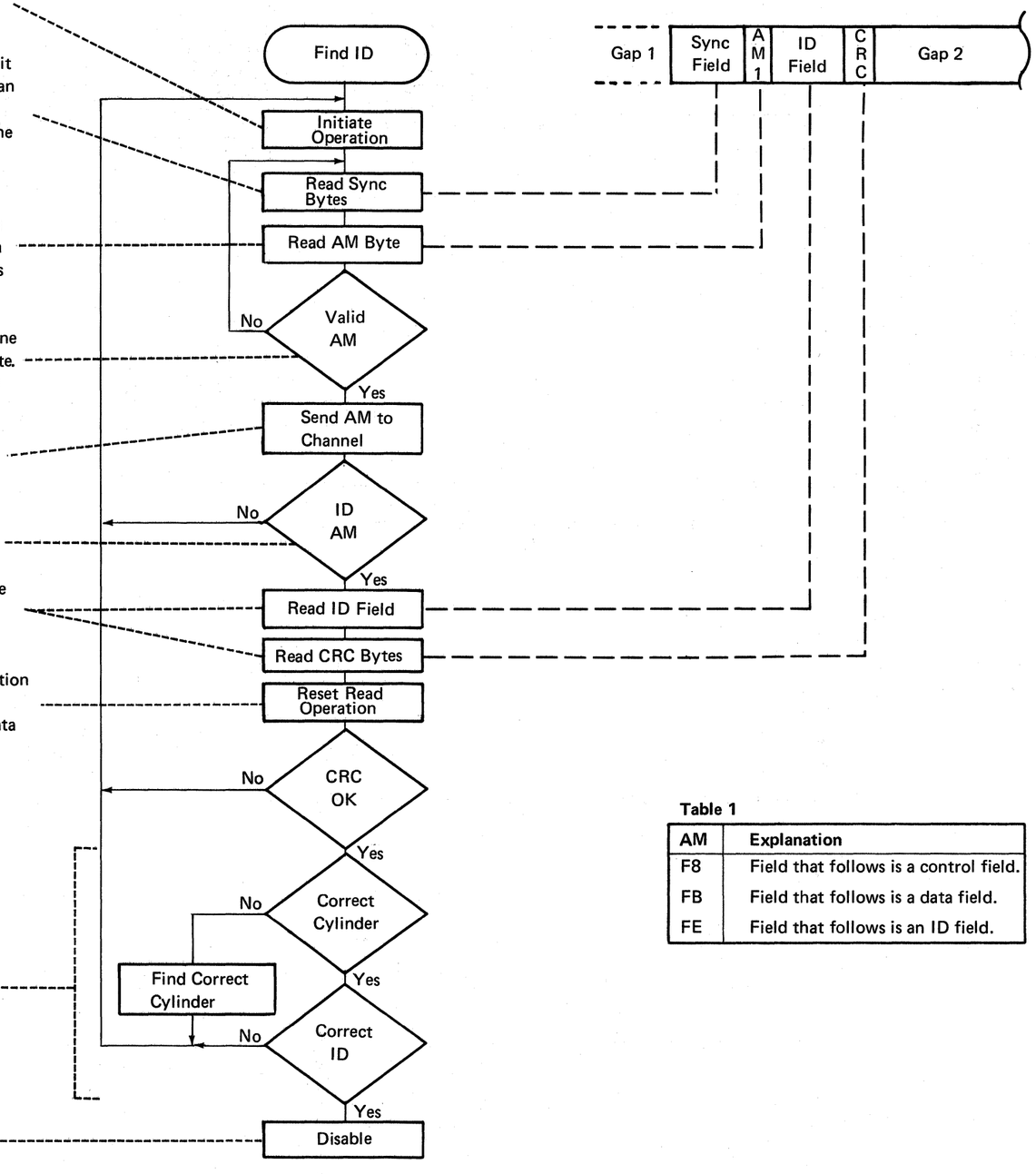
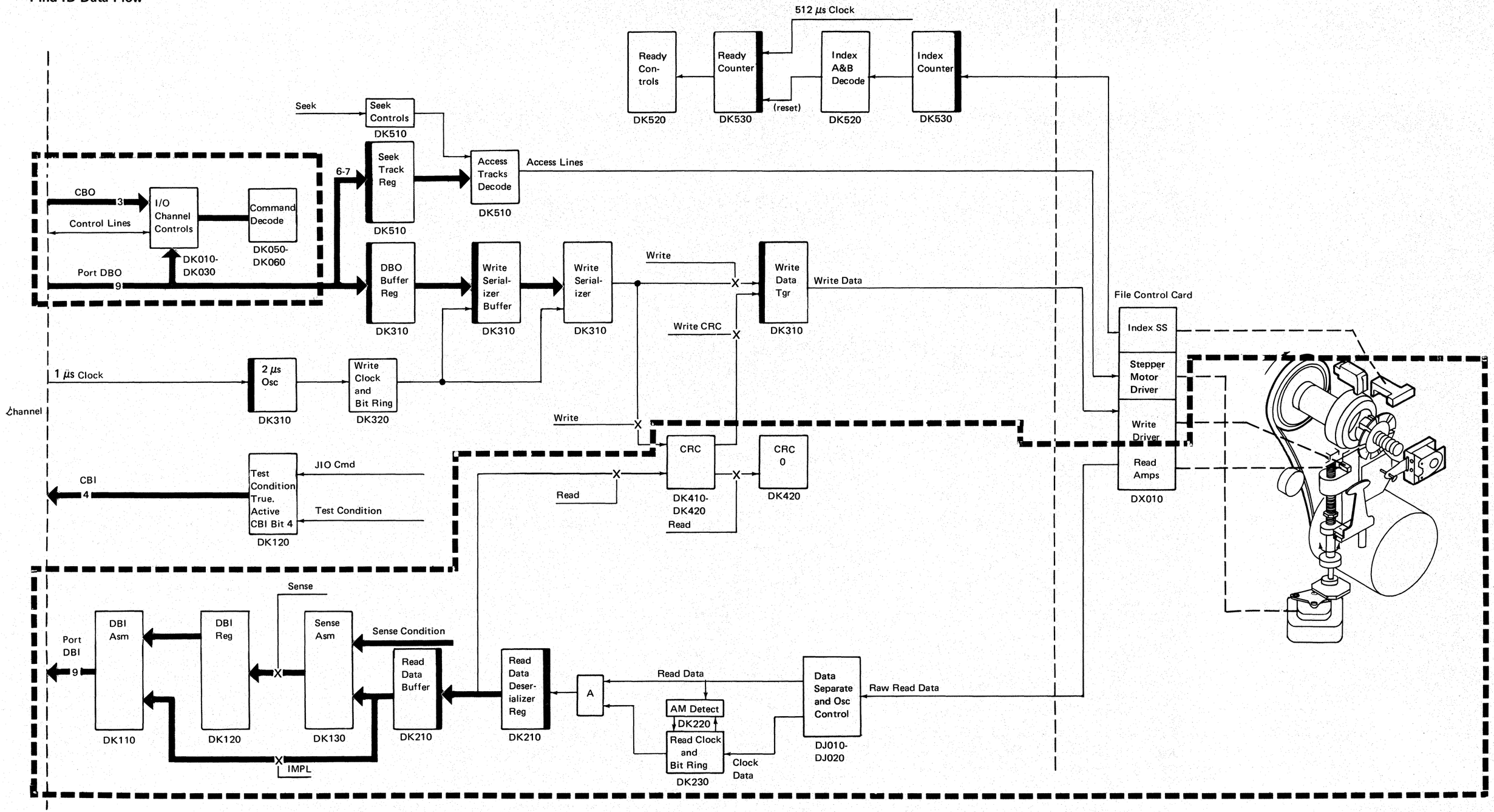


Table 1

AM	Explanation
F8	Field that follows is a control field.
FB	Field that follows is a data field.
FE	Field that follows is an ID field.

Find ID Data Flow



Write ID Operation

The accompanying flow chart describes the write ID operation. This operation is used to initialize a diskette. During this operation either 26 or 8 sectors may be set up. The data field is 128 or 512 bytes long respectively. During the initialization process each data field is written with the same data supplied by the user program. The data flow for the write ID operation is the same as for the write operation and is shown on the next page.

Write ID is controlled entirely by the microprogram After writing has started, the microprogram must supply bytes fast enough so they may be written every 32 μs. A failure to provide bytes fast enough results in a write overrun.

The major control in the attachment that defines the write ID operation is 'write gate'. This remains active from the time the first bytes are written until the last 2 bytes of zeros are written. The write clock and write bit ring will run as long as 'write gate' is active.

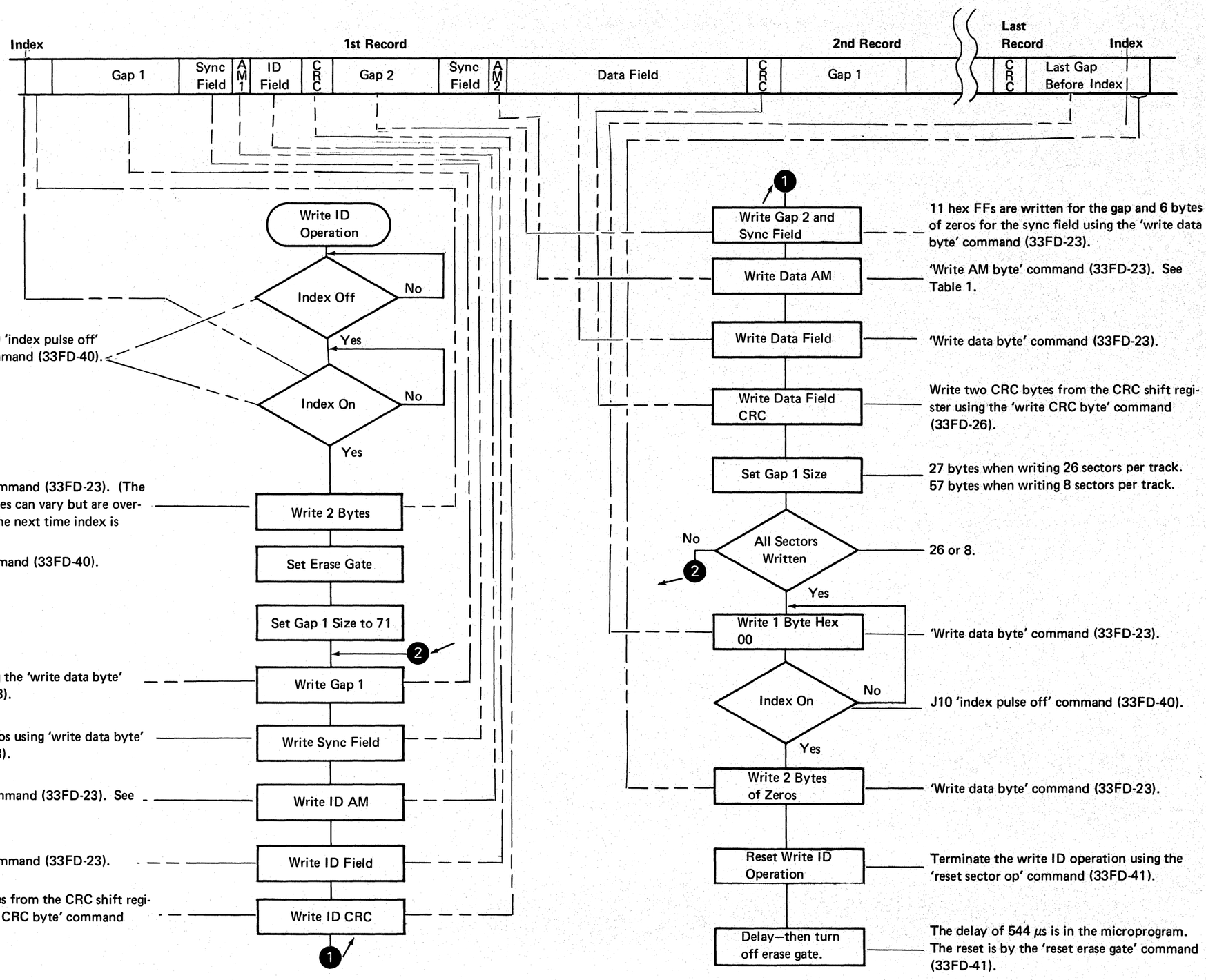
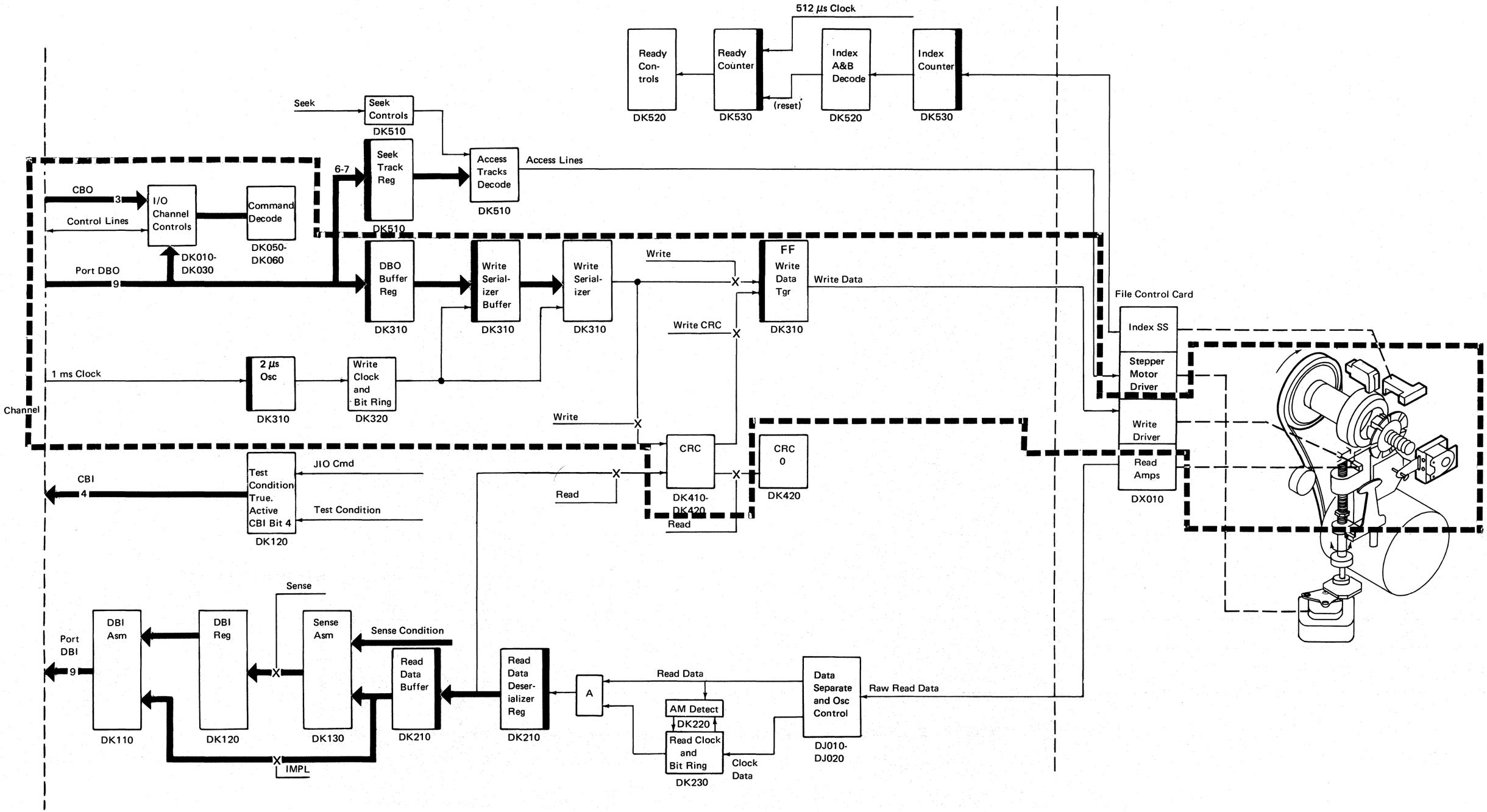


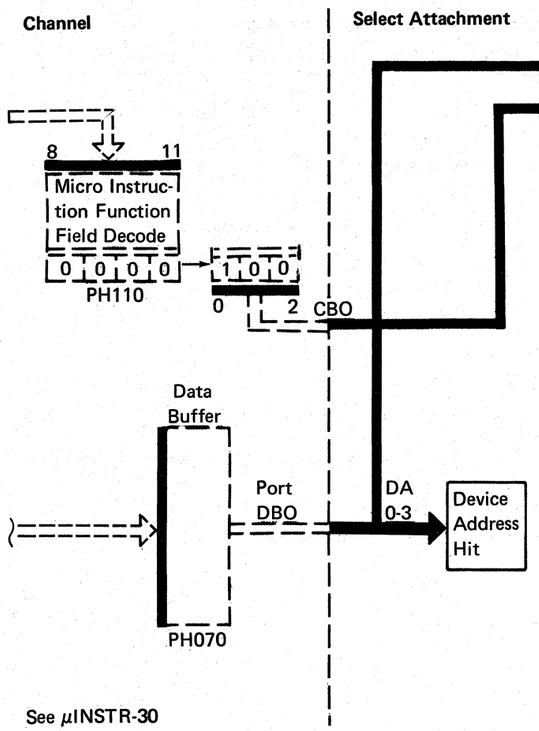
Table 1

AM (hex)	Explanation
F8	Field that follows is a control field.
FB	Field that follows is a data field.
FE	Field that follows is an ID field.

Write ID Data Flow



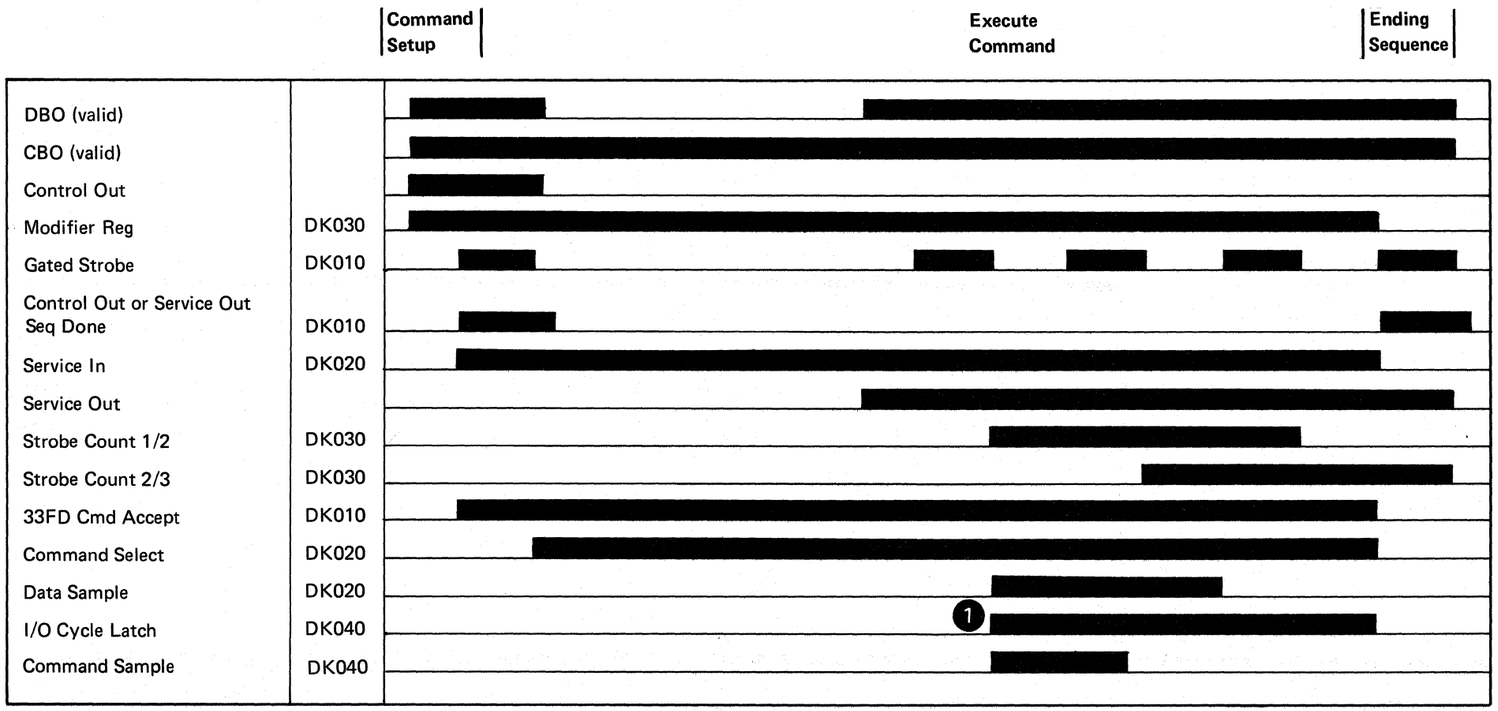
Load Command



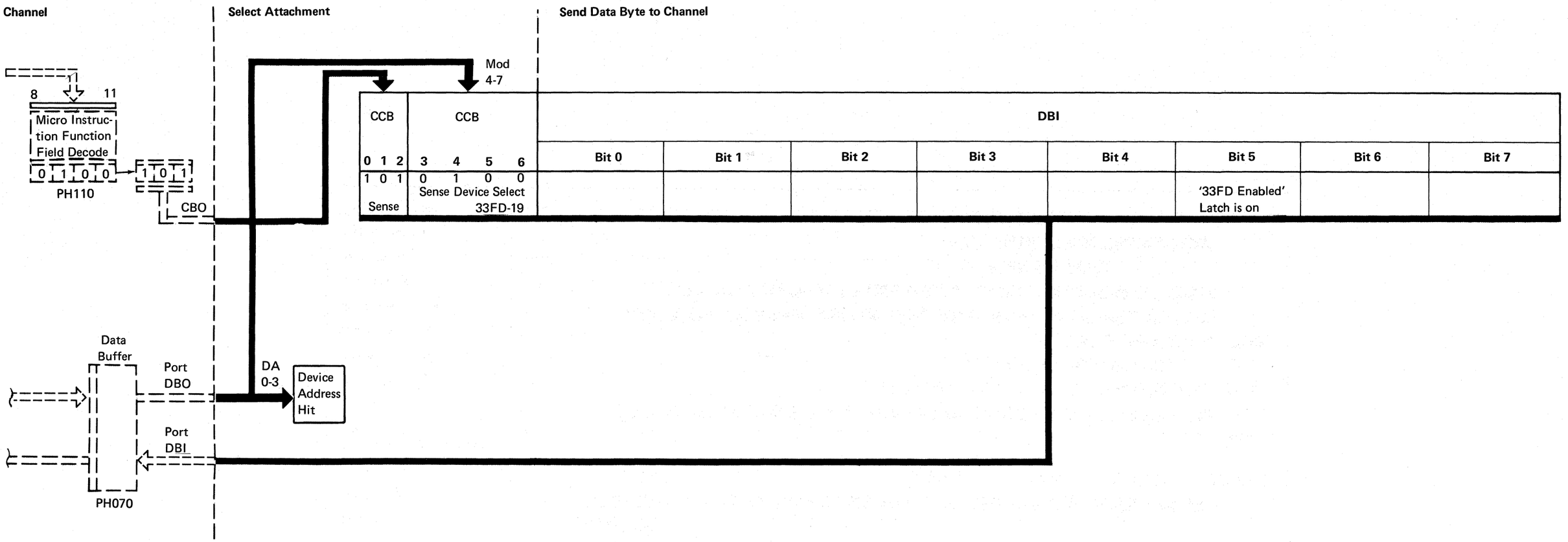
CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 0 0 I/O	0 0 0 0 Disconnect 33FD-17								
Load	0 0 0 1 Connect 33FD-17	1	1	0	1				

Load Command (Continued)

Modifier DBO 4, 5, 6, 7 (Hex)	DBO Data Bits	Command	Action Taken	Feald Page	Timing
0000 (0)		Disconnect	Reset the '33FD enable' latch.	DK040	❶
0001 (1)	0, 1, 3	Connect	Sets the '33FD enable' latch. This latch must be on for the 33FD to perform any function.	DK040	❶

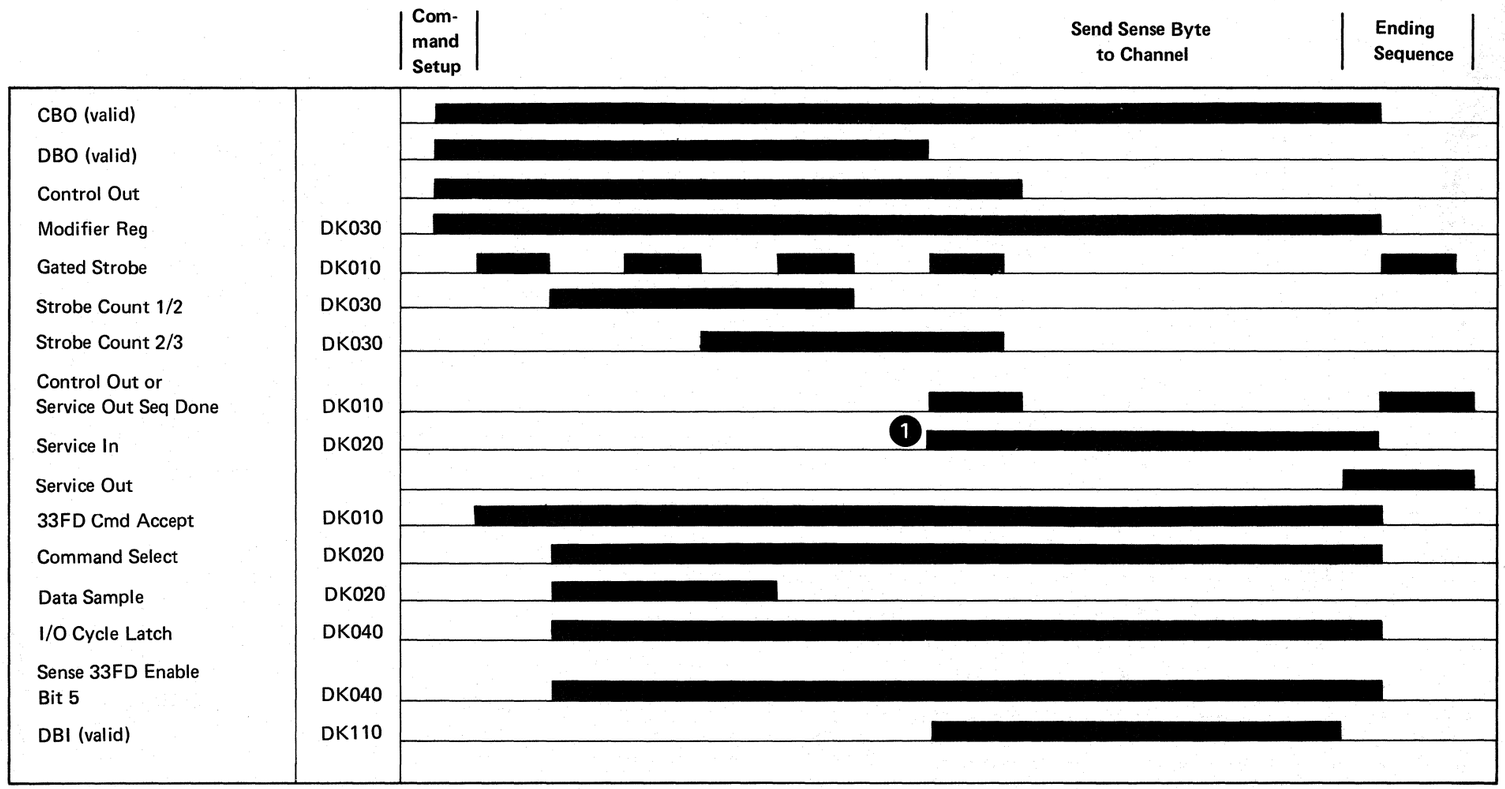


Sense Command

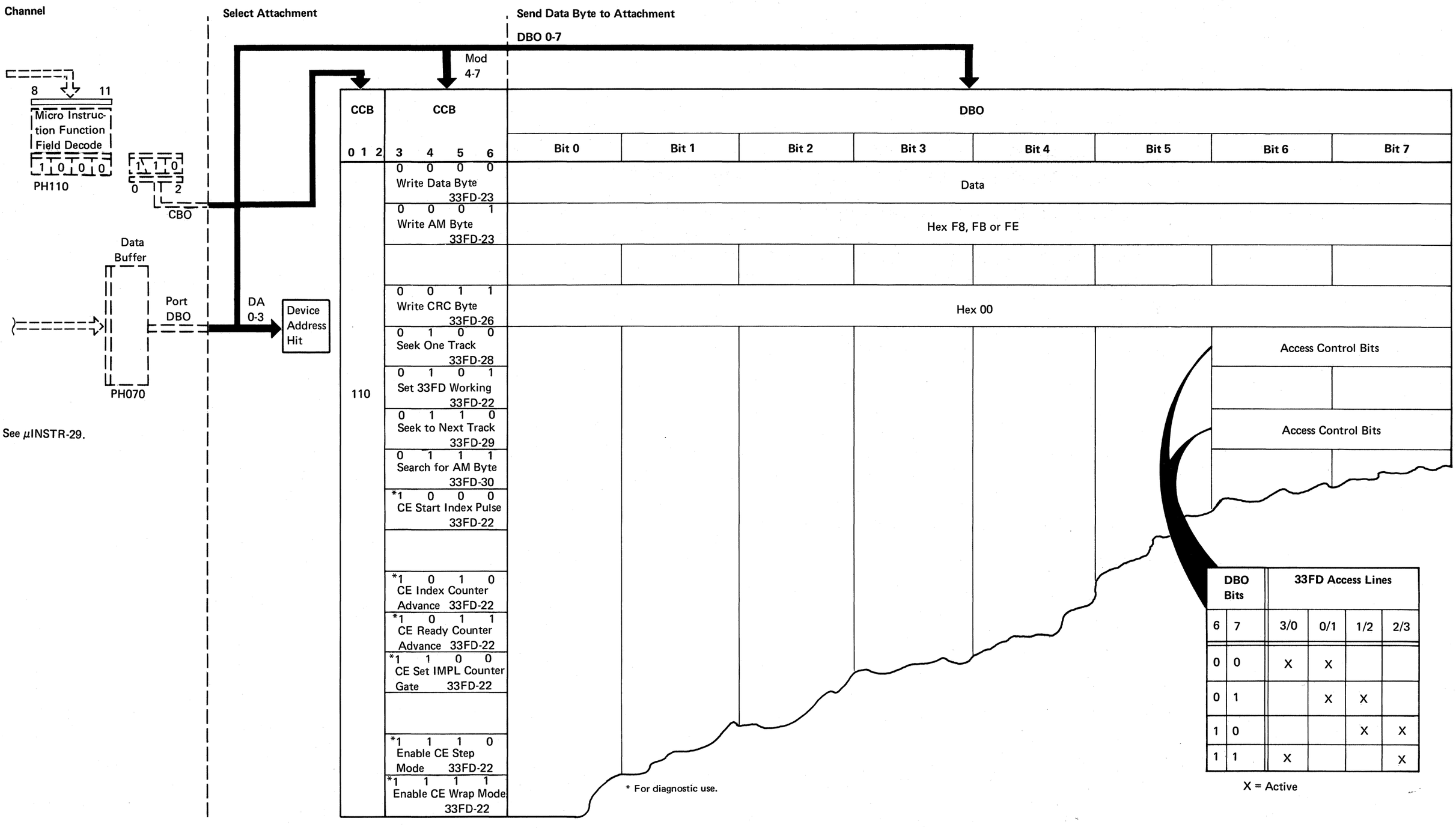


See μINSTR-30

Modifier DBO 4, 5, 6, 7 (Hex)	DBI Data Bit	Command	Action Taken	ALD Page	Timing
0100 (4)	5	Sense device select.	Senses status of '33FD enable' latch. If latch is on, DBI 5 bit will be sent to the channel.	DK040	❶



Control Load Command



See μINSTR-29.

* For diagnostic use.

DBO Bits		33FD Access Lines			
6	7	3/0	0/1	1/2	2/3
0	0	X	X		
0	1		X	X	
1	0			X	X
1	1	X			X

X = Active

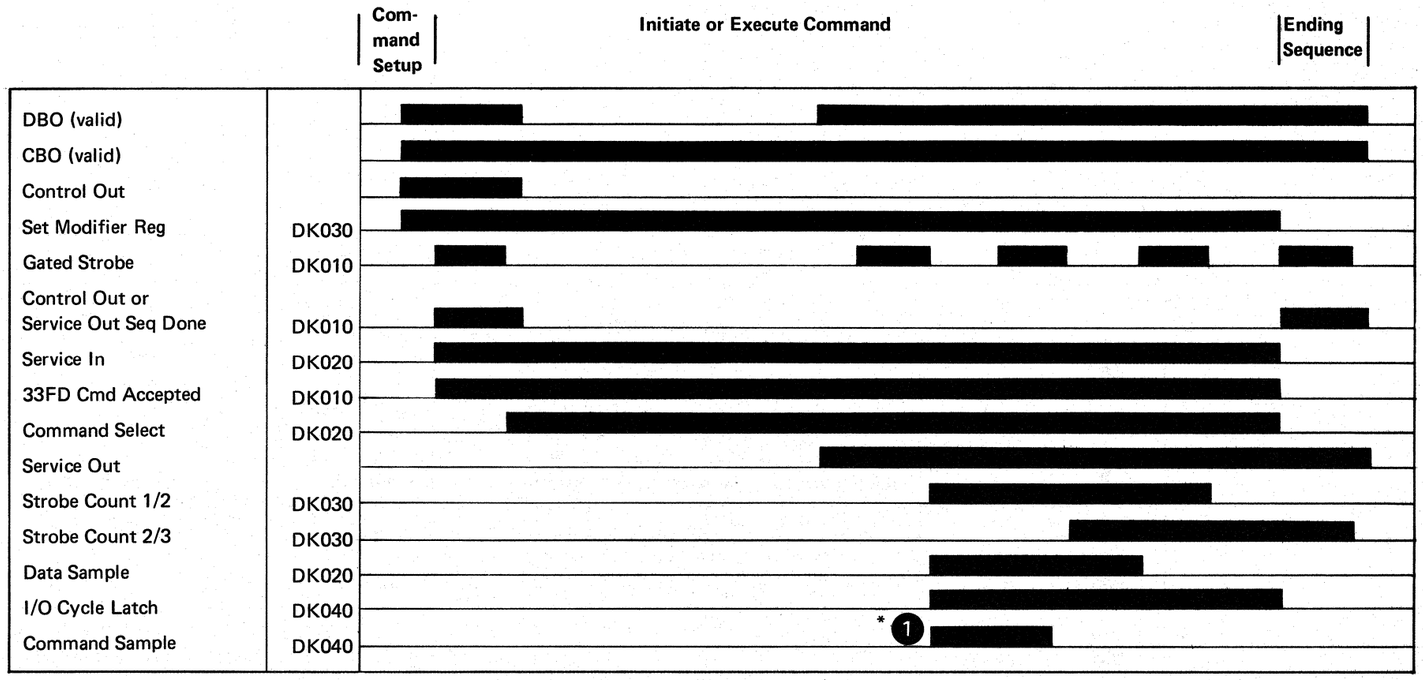
Control Load Command (Continued)

The main purposes of the IOCL command are to:

- Initiate a write operation, seek operation, or a read operation.
- Transfer a data byte to the attachment.
- Perform CE (diagnostic) functions.

All IOCL commands make a data byte available to the attachment. However, in some cases the data byte has no significance and is not used.

The timing chart on this page shows the sequence of events for the IOCL command. The details of the individual commands (specified by the modifier) are covered on the following pages. References will be made to this page for the interface sequences.



*See 33FD-22

Control Load Command (Continued)

Modifier DBO 4, 5, 6, 7 (Hex)	DBO Data Bits	Command	Action Taken	ALD	Timing[1]
0000 (0) 0001 (1) 0011 (3) 0100 (4) 0110 (6) 0111 (7)		Write data byte Write AM byte Write CRC byte Seek one track Seek to next track Search for AM byte	These control load commands are covered in detail on the following pages.		
0101 (5)	Not used	Set 33FD working	Sets the '33FD working' latch; the status of the latch can be checked by the IOCS command.	DK060	1
1000 (8)	Not used	CE start index pulse[2]	Turns on the 'CE mode index' latch. This latch is used to simulate an index pulse. The latch is reset by a 'reset sector op' command.	DK520	1
1010 (A)	Not used	CE index counter advance[2]	Generates an advance pulse to the index counter. This command will cause the index counter to advance one position.	DK520 DK530	1
1011 (B)	Not used	CE ready counter advance[2]	Advances the ready counter by 1.	DK530	1
1100 (C)	Not used	CE set IMPL counter gate[2]	Turns on the 'CE IMPL' latch. This will allow the IMPL counter to step, the head to load, and the 'read data command' latch to turn on. Refer to *IMPL Operation* for the sequence of IMPL events.	DK510	1
1110 (E)	Not used	Enable CE step mode[2]	Turns on the 'step' latch. This latch degates 'write gate' and 'gated tunnel erase'. It also degates '33FD standard read data' (DK210), '33FD standard read clock' (DK230), '1 μs chan osc' (DK310), '33FD index SS' (DK520), and 'chan S12 ns osc' (DK530).	DK060	1
1111 (F)	Not used	Enable CE wrap mode[2]	Turns on the 'wrap' latch. This latch degates 'write gate' and 'gated tunnel erase'. In addition, data instead of being written on diskette is gated into the data separator to be read (DJ020).	DK060	1

[1] Refer to 33FD-10.
[2] For diagnostic use.

Write Data Byte and Write AM Byte

- Attachment receives 'write data byte' or 'write AM byte' command.
- Data byte or AM byte is received on the DBO and set in the DBO buffer.
- The byte is transferred to the serializer and then written on the diskette along with the clock bits.
- The 'write AM byte' command drops three of the clock bits.

The control load command is received on the CBO and remains there until after the data byte to be written is received by the attachment. The device address and modifier are received on the DBO. The modifier is set in the modifier register and used later in conjunction with the IOCL command to set the 'write gate'. Write gate remains on for the entire write operation after which it is reset by a 'reset sector op' instruction.

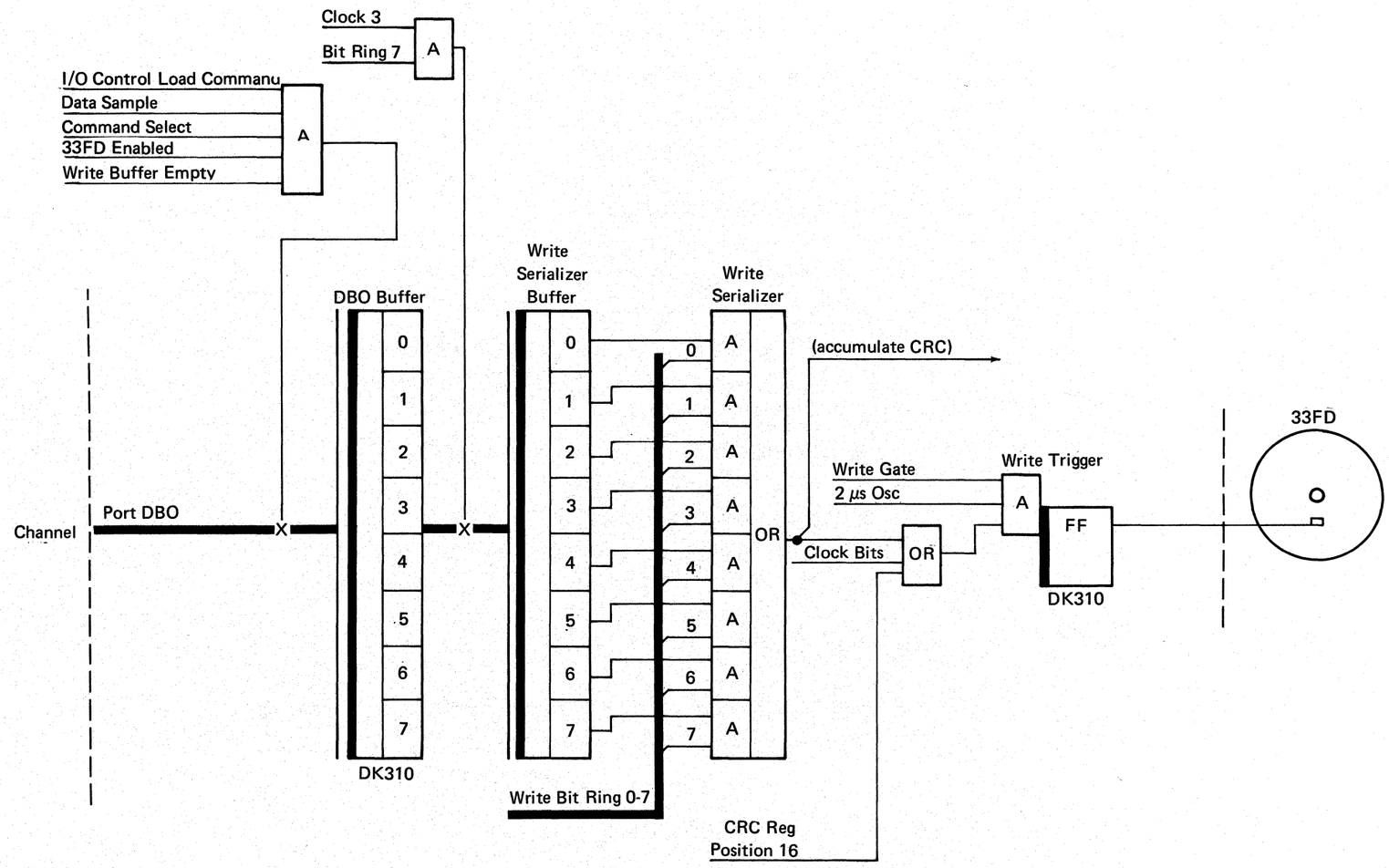
The data byte is received on the DBO and into the DBO buffer. At the same time 'write gate' is set and the write clock and bit ring are started. The write bit ring has been held reset to 6 by not 'write gate'. At bit ring 7 and clock 3 the data byte is transferred to the serializer.

Note: 'Write gate' is on if bytes have already been written.

Bits are gated sequentially from the serializer, ORed with clock bits and sent to the '33FD write data' trigger. Each shift on the input to the trigger causes it to flip which in turn causes the current through the write head to change direction.

The three clock bits that are missing when the AM byte is written are used later during a read operation for byte synchronization.

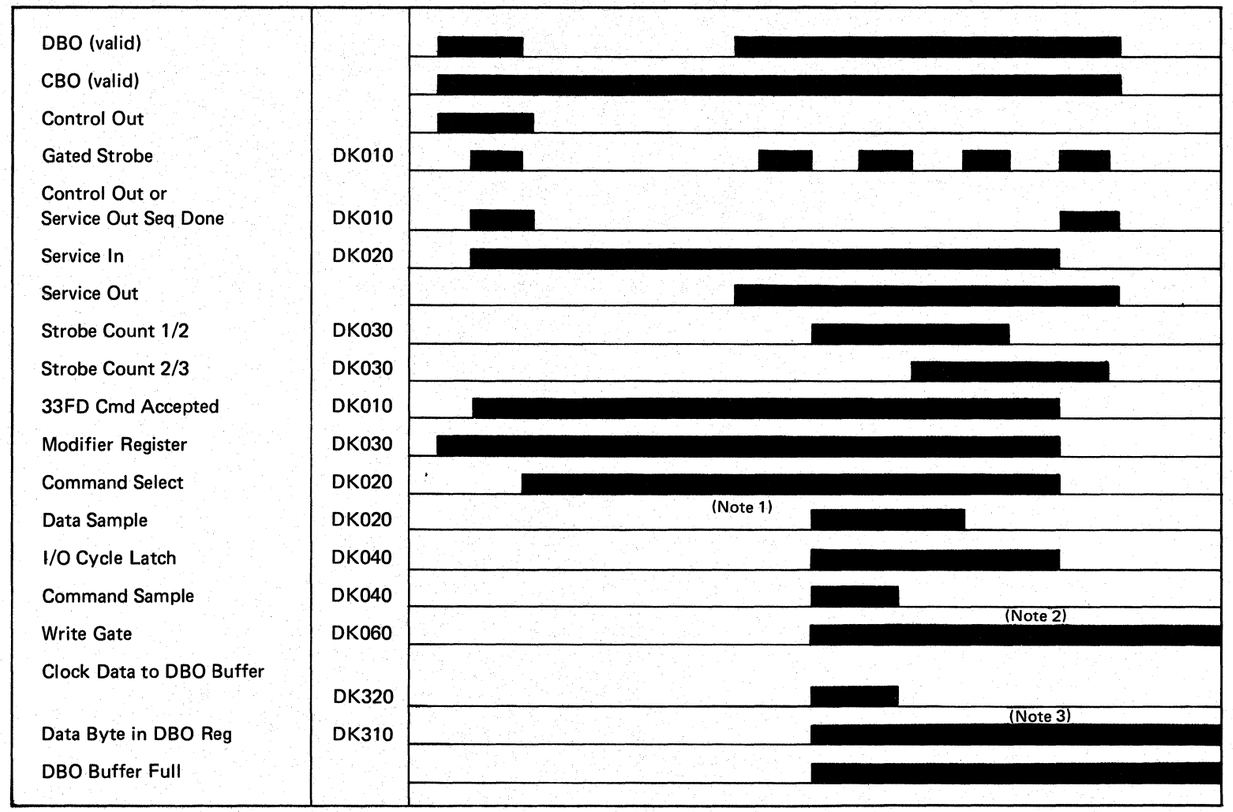
The data and AM bits are also sent to the CRC shift register (33FD-49).



Write Data Byte and Write AM Byte (Continued)

This chart illustrates the setting of the 'write data byte' and 'write AM byte' controls and the transfer of the byte to the DBO buffer.

The serializing and writing of the byte is illustrated in the chart on the next page.

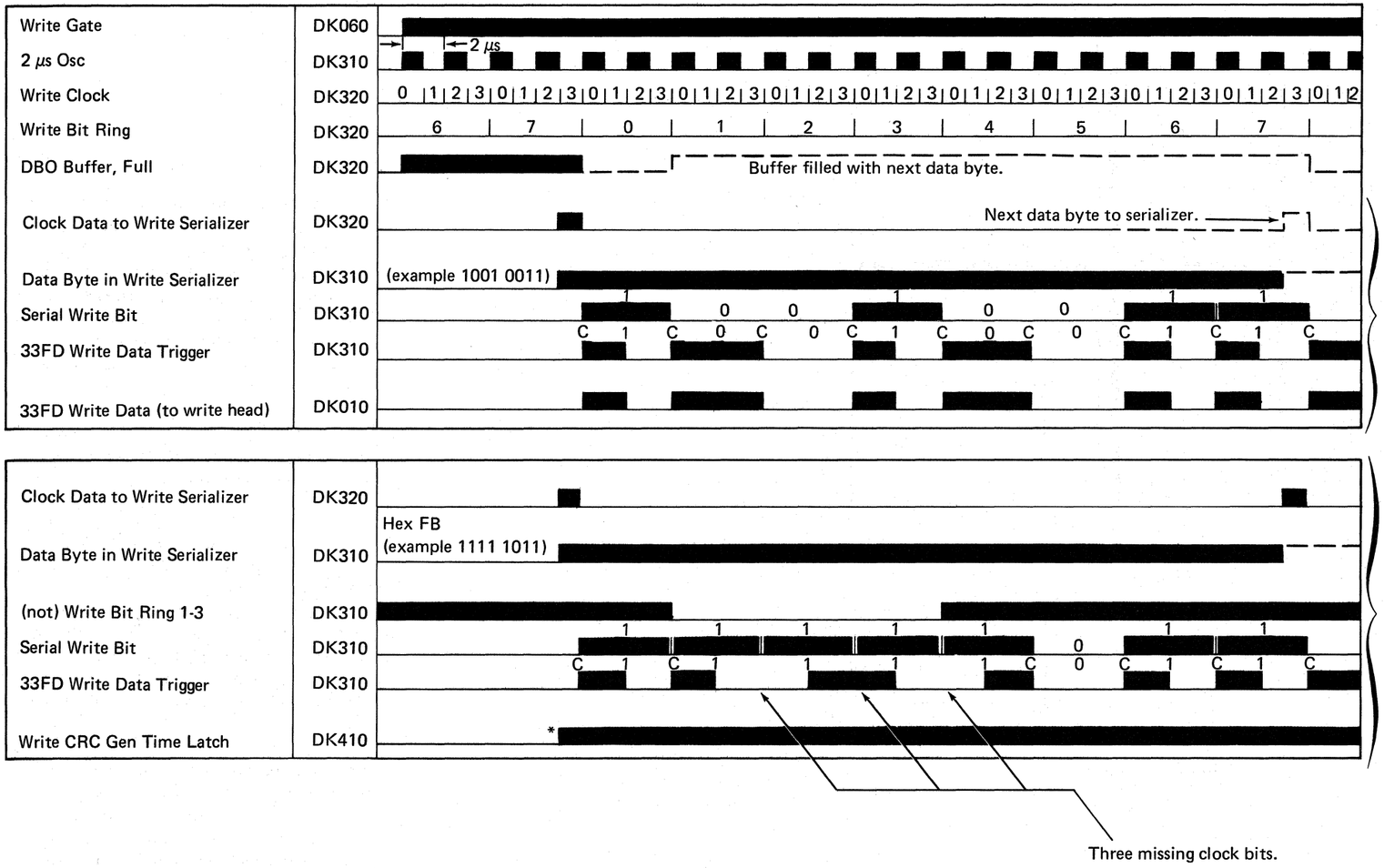


Notes:

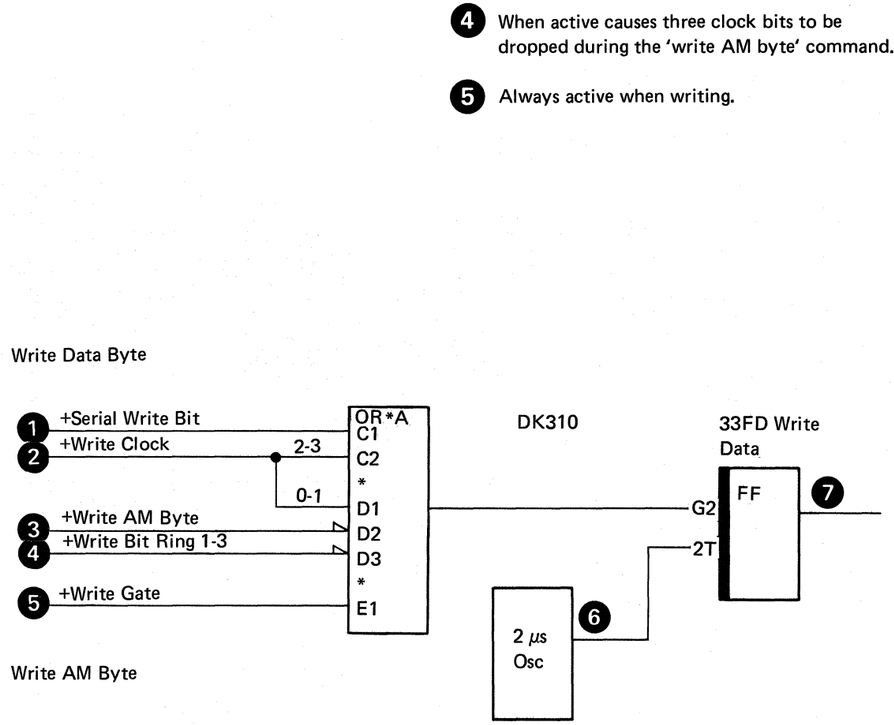
1. 'Command sample' and 'gated strobe' pulses are delayed if the DBO buffer has not transferred the preceding byte to the serializer.
2. 'Write gate' stays active until a 'reset sector op' command is received.
3. Data stays in the DBO register until the next byte is received.

Write Data Byte and Write AM Byte (Continued)

This chart illustrates the serializing and writing of the data byte and the AM byte that has previosuly been transferred to the DBO buffer. 'Write gate' is repeated from the preceding timing chart as a point of reference.

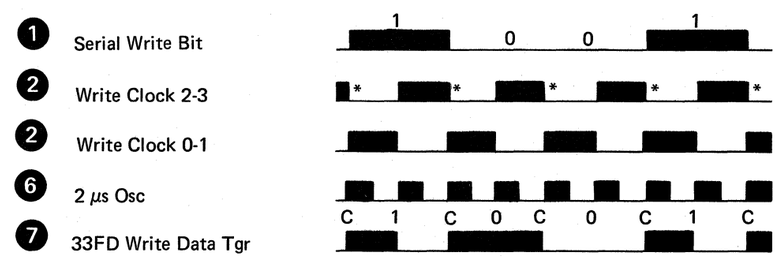


*Allows CRC shift register to accumulate CRC bytes.



33FD Write Data Trigger

1. Active to write data bits.
2. 2-3 active to write clock bits and 0-1 active to write data bits.
3. Inactive during 'write data byte' command. Allows data bits and clock bits to be written.
4. When active causes three clock bits to be dropped during the 'write AM byte' command.
5. Always active when writing.



*Gate to trigger remains active long enough for clock bits to be written at these times.

Write CRC Byte

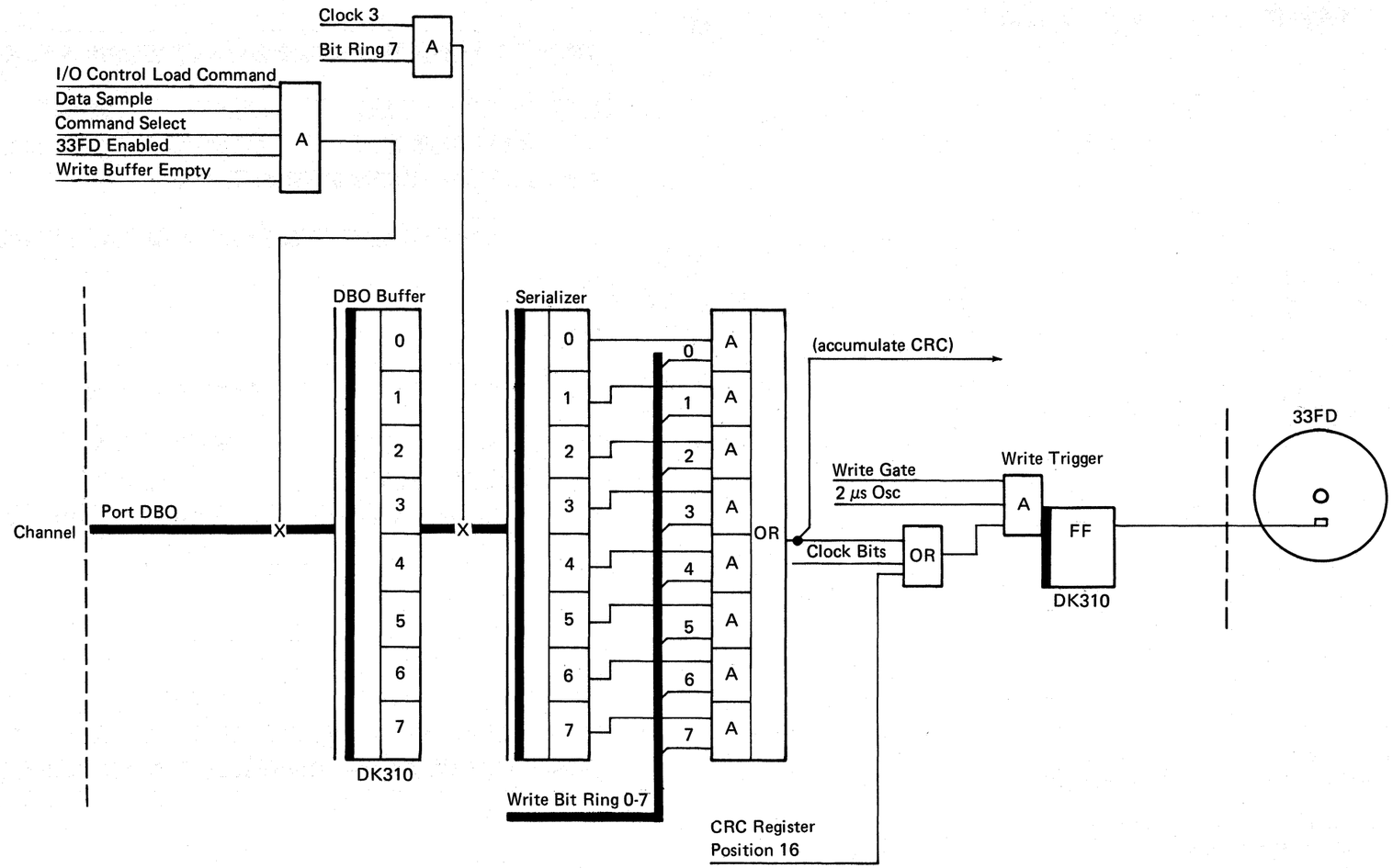
This command initiates the following sequence of events:

- Attachment receives two 'write CRC byte' commands.
- CRC shift register is advanced and each time position 16 is turned on, a CRC bit will be written on the diskette.
- A 'reset sector op' command follows the last 'write CRC byte' command if this is the last sector to be written.

The initiation of the 'write CRC byte' command is the same as for the 'write data byte' command. The data byte on the DBO (must be zero) is set into the DBO register. Just as in a 'write data byte' command, the contents of the DBO buffer is sent to the serializer. The output of the serializer is ORed with the CRC register position 16. Therefore, the DBO byte must be zero so the correct CRC byte will be written.

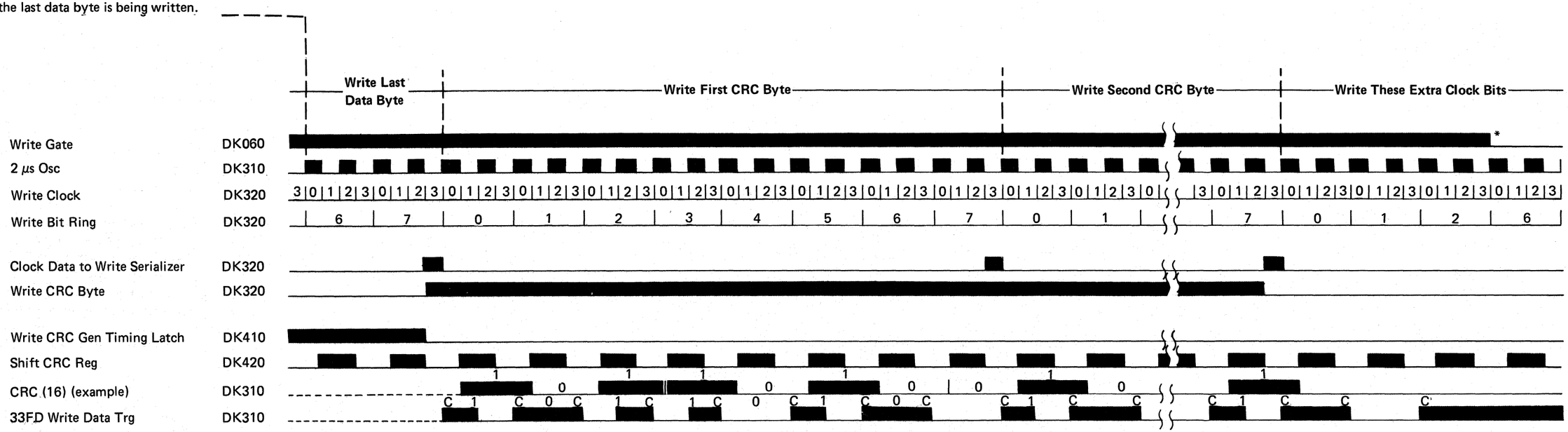
Two 'write CRC byte' commands must be sent in order to write all 16 bits (2 bytes) of the CRC character.

A 2 byte delay to allow the CRC bytes to be written is accomplished by sending 2 bytes of zeros to the attachment using the 'write data byte' command. These two comamnds place a zero in the DBO buffer and in the serializer. A 'reset sector op' command follows and resets 'write gate'. However, before resetting 'write gate' three extra clock bits are written. This ensures correct reading of the last CRC bit.



Write CRC Byte (Continued)

See the 'write data byte' timing chart (33FD-24) for the initiation of this command. As a point of reference, the zero is set into the DBO buffer at this time as the last data byte is being written.



*Reset by a 'reset sector op' command.

Seek One Track

This command initiates the following sequence of events:

- Attachment receives a 'seek one track' command.
- Control information to move the head to the next track is received on the DBO.
- The read/write head is loaded.
- The head is moved one track by rotating the stepper motor 90 degrees.
- The operation is completed by the time the next index pulse occurs.

This operation differs from the 'seek to next track' command in the following respects:

- The command is initiated by the 33FD microprogram just after index time.
- The command causes the read/write head to load.
- The operation is reset by the next index pulse.

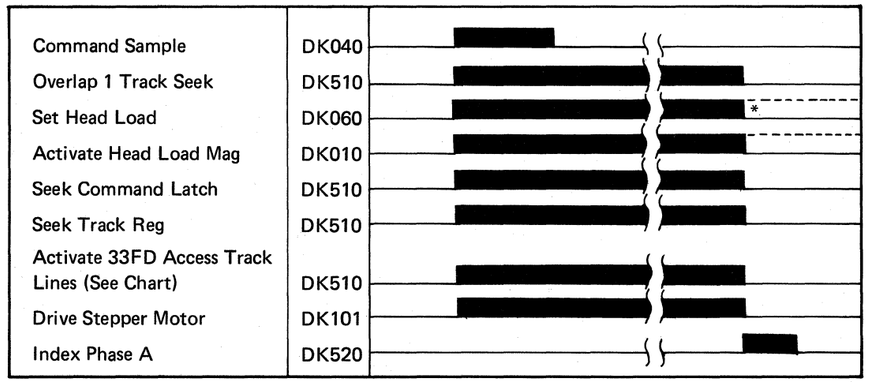
A single 'seek one track' command can only move the read/write head one track. The 33FD microprogram must know where the head is and send the correct data byte to move the head one track. However, only bits 6 and 7 on the DBO are used to control the access lines to the 33FD disk drive (see chart on this page).

The initiation of the operation is the standard sequence for the control load command. At command sample time the attachment sets the 'overlap 1 track seek' latch and data bits 6 and 7 are set in the track address register. As a result the head is loaded, the 'seek command' latch turned on and the output of the track address register selects the proper 33FD access lines to move the head one track. A 'disconnect' command activates the reset to the 'seek command' latch. However the set overrides the reset and the latch remains on until the 'overlap 1 track seek' latch is reset.

At the next 'index pulse A' time, the operation is ended by resetting the 'overlap 1 track seek' latch. The minimum time between index pulses is slightly over the 150 ms required to do a seek of one track.

Refer to ALD DK510.

See the control load timing chart (33FD-21) for the initiation of this command. 'Command sample' is used as the point of reference.



*If 33FD has been enabled by this time, the head remains loaded.

Access Chart

Move Head to Track →		0	1	2	3	4	5	6		74	75	76
DBO Bits	6	0	0	1	1		0	1		1	1	0
	7	0	1	0	1	0	1	0		0	1	0
Access Lines Energized	3/0	X			X	X					X	X
	0/1	X	X			X	X					X
	1/2		X	X			X	X		X		
	2/3			X	X			X		X	X	

Seek to Next Track

This command initiates the following sequence of events:

- Attachment receives a 'seek to next track' command.
- Control information to move the head to the next track is received on the DBO.
- The read/write head is moved one track by rotating the stepper motor 90 degrees.

A single 'seek to next track' command can only move the read/write head one track in either direction. The 33FD microprogram must know where the head is and place the proper data byte on the DBO. Only bits 6 and 7 on the DBO are required to control the access lines to the 33FD disk drive.

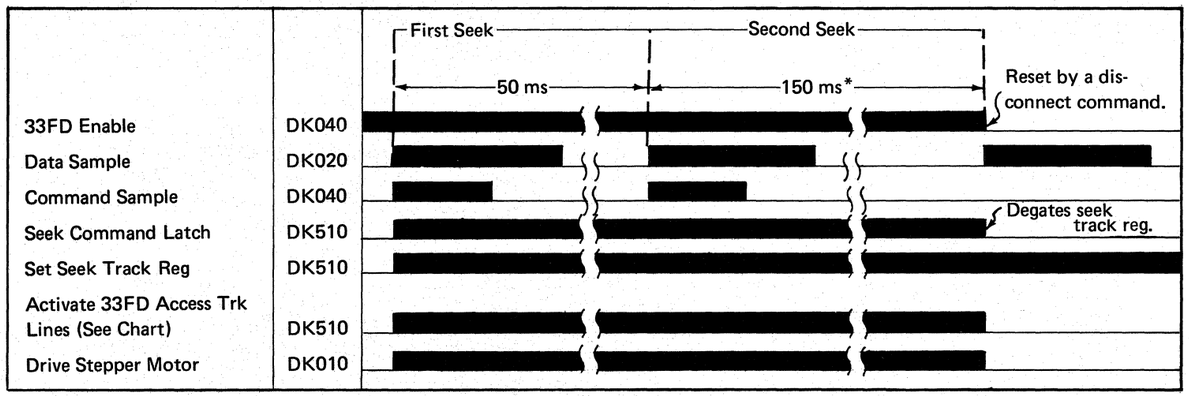
The initiation of the operation is the standard sequence for the IOCL command. At command sample time, the attachment sets the 'seek command' latch and data bits 6 and 7 are set in the track address register. The output of the track address register selects the proper 33FD access lines to move the head one track.

If the head is to be moved more than one track, the 33FD microprogram issues another 'seek to next track' command after 50 ms. After the last seek has been issued, the microprogram waits 150 ms and then resets the seek by issuing a 'disconnect' command.

The disconnect resets the '33FD enabled' latch which in turn resets the 'seek latch' and ends the seek operation.

Refer to ALD DK510.

The 'seek to next track' commands are initiated by the control load sequence (33FD-21). 'Data sample' and 'command sample' may be used as a point of reference to continue on this chart.

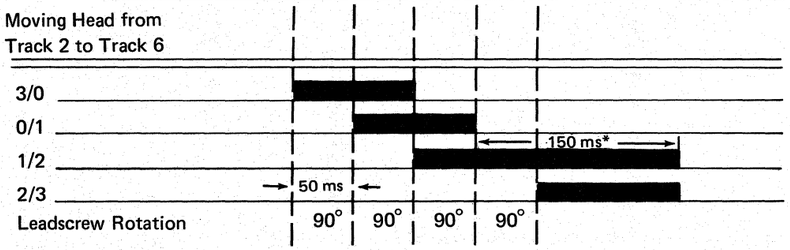


*50 ms to seek and 100 ms for seek mechanism to stabilize.

Access Chart

Move Head to Track →		0	1	2	3	4	5	6	...	74	75	76
DBO Bits	6	0	0	1	1	0	0	1		1	1	0
	7	0	1	0	1	0	1	0		0	1	0
Access Lines Energized	3/0	X			X	X					X	X
	0/1	X	X			X	X					X
	1/2		X	X			X	X		X		
	2/3			X	X			X		X	X	

Example: Moving Head from Track 2 to Track 6



Search for AM Byte

This command initiates the following sequence of events:

- Attachment receives 'search for AM byte' command.
- This command initiates a read operation by turning on the 'read data command' latch.
- Attachment searches for a sync field and an AM byte.
- The data separator, read clock, and read bit ring are synchronized.
- AM byte is deserialized and placed in the 'read data buffer'.

The 'search for AM byte' command is used to initiate the reading of the ID field or the data field of a record. It causes the bytes being read to move through the deserializer and into the 'read data buffer'. The 'sense data byte' command is then required to transfer each byte of data to the channel.

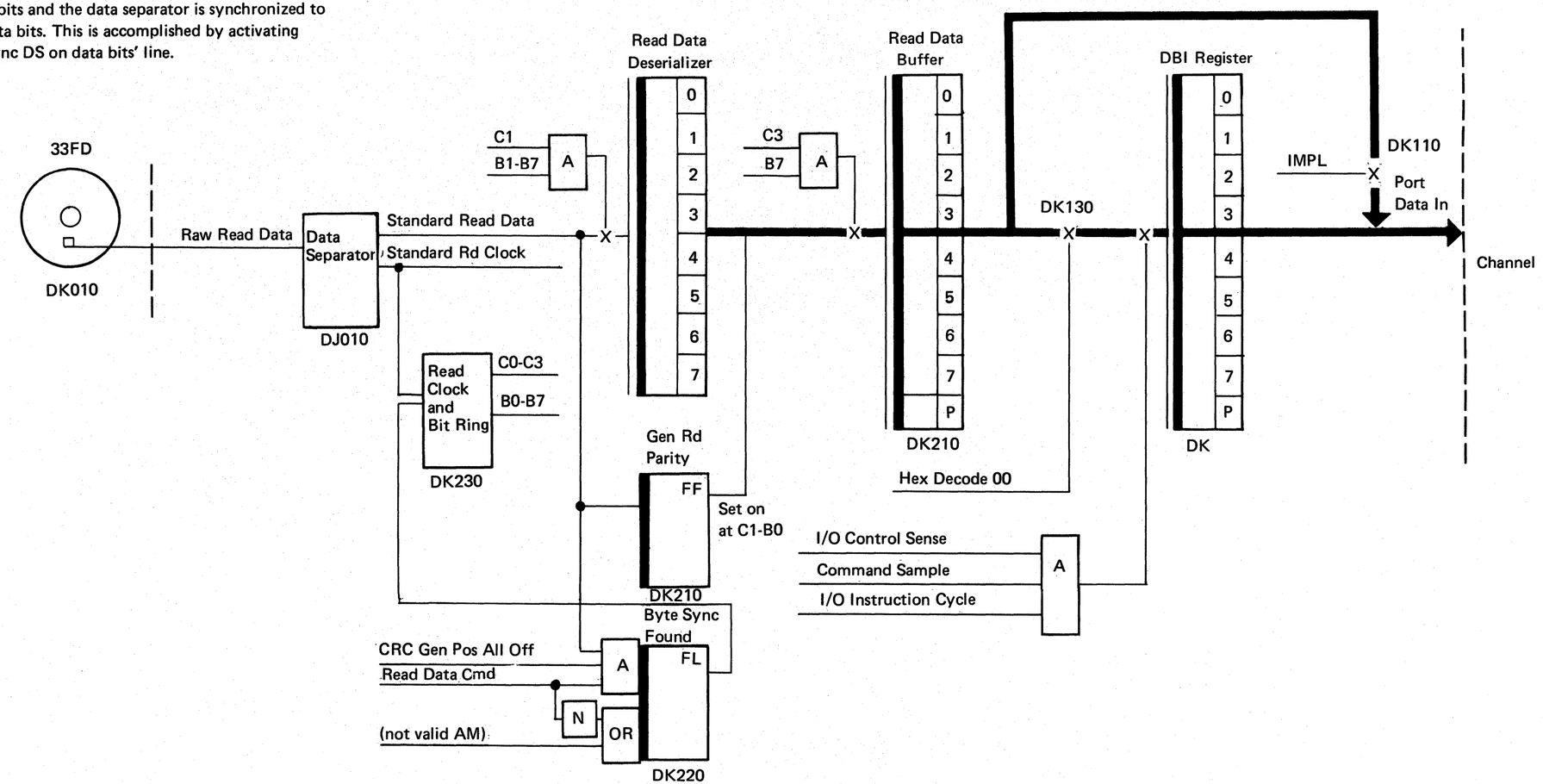
The initiation of this command is the standard sequence for the 'control load' command (33FD-21). At command sample time the 'read data command' latch is set and the search for a sync field is started. After 16 consecutive zeros are read, it is assumed to be a sync field. Sixteen zeros fed to the CRC circuits turn all positions of the 'CRC shift register' off (33FD-49).

The search then continues for the first data bit of the AM (address mark). This bit will turn on the 'byte sync found' latch and allow the read bit ring to start running. In addition, the 'CRC shift register' is initialized for reading by turning all positions of the 'CRC shift register' on.

If a valid AM is found, the 'byte sync found' latch is left on and reading of subsequent data continues. If a valid AM is not found, the 'byte sync found' latch is turned off and the attachment looks for another sync field.

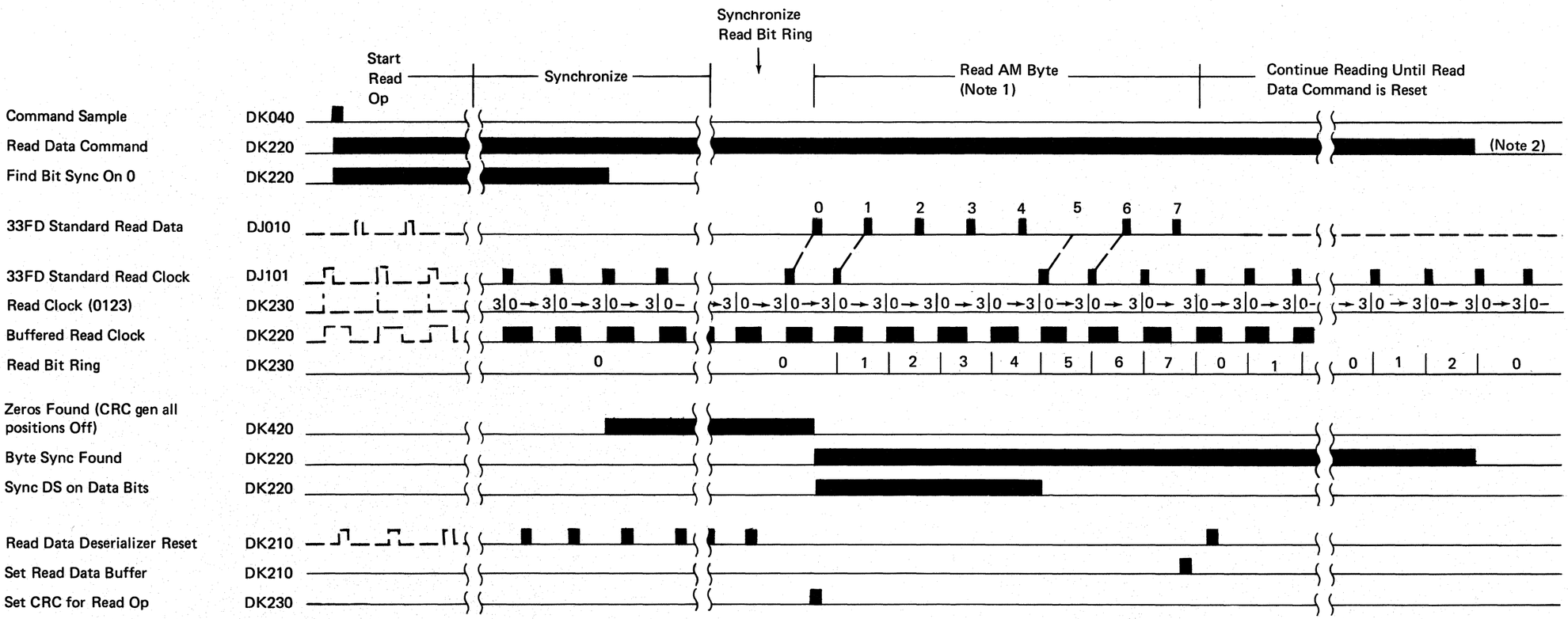
After the AM byte is read into the deserializer it is transferred to the 'read data buffer'. A 'sense data byte' command is then required to gate this byte into the 'DBI register' and on to the channel.

Normal synchronization between the diskette and the data separator is accomplished by synchronizing to the clock bits. However, during bit ring 2, 3, and 4 time when reading the AM, there are no clock bits and the data separator is synchronized to the data bits. This is accomplished by activating the 'sync DS on data bits' line.



Search for AM Byte (Continued)

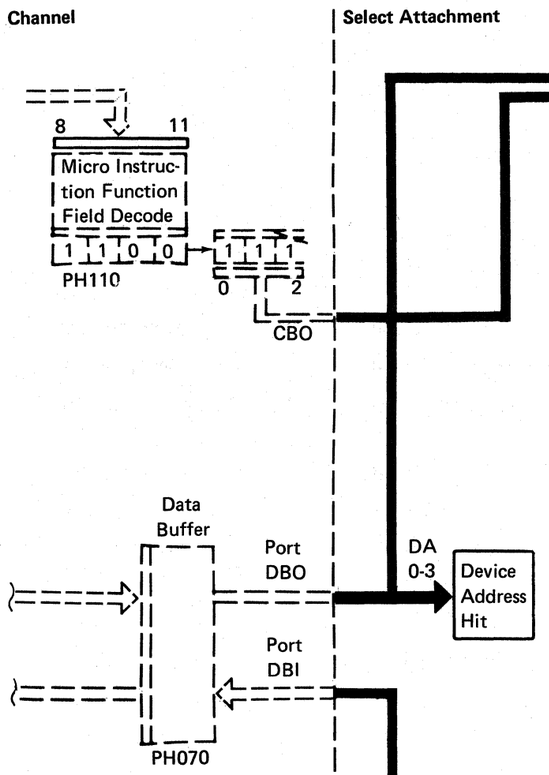
See the 'control load' timing chart (33FD-21) for the initiation of this command. 'Command sample' is the point of reference between the two charts.



Notes:

1. AM byte example is FB.
2. Read operation is ended by a reset sector op command.

Control Sense



See μINSTR-30.

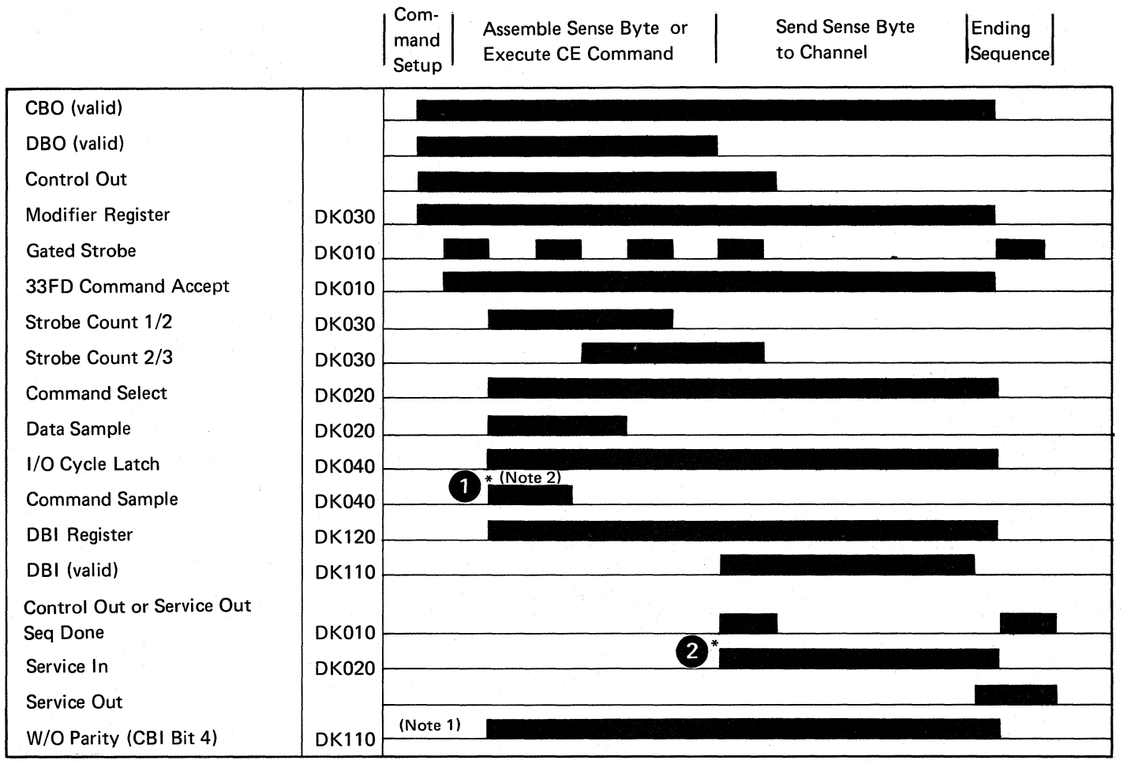
0 1 2	3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
	0 0 0 0 Data Byte 33FD-34	Data Bits							
	0 0 0 1 Error Byte 1 33FD-34	33FD Fast 33FD-42	Not Ready 33FD-42	End of Cylinder	Missing Record 33FD-45	Read Overrun 33FD-43		Write Overrun 33FD-43	Write Parity Check 33FD-43
	0 0 1 0 Error Byte 2 33FD-34	Write or Erase Gate Unsafe 33FD-44	Missing Erase Gate 33FD-44					33FD I/O Working	
	0 0 1 1* 33FD Control 33FD-34	Head Load	Low Write Current	Write Current Gate	Gated Tunnel Erase	Track 3 or 0	Track 0 or 1	Track 1 or 2	Track 2 or 3
	0 1 0 0* Read Control 33FD-35	Write Data	Data Wrap Mode	Find Bit Sync on Zeros	Sync on Data Bits	AM Byte Good		Read Clock C1-C2	Read Clock C2-C3
	0 1 0 1* Write Control 33FD-35		CE Wrap Data			Write AM	Write CRC	Write Clock 1	Write Clock 2
	0 1 1 0* Bit Rings 33FD-35	Read Bit Ring 1-4	Read Bit Ring 2-5	Read Bit Ring 3-6	Read Bit Ring 4-7	Write Bit Ring 1-4	Write Bit Ring 2-5	Write Bit Ring 3-6	Write Bit Ring 4-7
	0 1 1 1* Counters & CRC 33FD-36		IMPL Counter not 81	Index Counter 8	Ready Counter not 170, 032 μs	CRC not Zero	CRC not Divide	CRC Reg Position 1	CRC Reg Position 16
	1 0 0 0* CE Write Clock Advance 33FD-36	Hex 00							
	1 0 0 1* CE Standard Read Data Pulse 33FD-36								
	1 0 1 0* CE Standard Read Clock 33FD-36								
	1 0 1 1* CE 8F Read Clock 33FD-36								
	1 1 0 0* Sense for Hex 00 33FD-36								
	1 1 0 1* Set DBI Reg to Hex FF 33FD-36	Hex FF							
	1 1 1 0* Set DBI Reg to Hex 0F 33FD-36	Hex 0F							
	1 1 1 1* Set DBI Reg to Hex F0 33FD-36	Hex F0							

*For diagnostic use.

Control Sense (Continued)

The control sense command transfers a data byte, an error byte, or a byte of attachment control information to the channel. However, some commands are sent to perform CE (diagnostic) functions such as simulating a 'standard read data pulse' or setting a specific value in the DBI register. All control sense commands return a sense byte to the channel. In some cases it is only a hex 0 with no real significance other than indicating the DBI register is reset to 0.

The timing chart on this page shows the sequence of events for the control sense command. The chart is referenced from the following control sense pages.



Notes:

1. Parity is not generated unless a data byte is being sent to the channel (DBO modifier hex 0) and the 33FD is enabled. The CBI bit 4 line is active if parity is not generated.
2. 'Command sample' and 'gated strobe' pulses are delayed if the read data buffer does not contain the next data byte for a sense data byte command (DBO modifier hex 0).

*See 33FD-34, 35, and 36

Control Sense (Continued)

Modifier DBO 4, 5, 6, 7 (Hex)	DBI Data Bits	Command	Action Taken		ALD	Timing
0000 (0)	0-7, P	Sense Data Byte	Transfers contents of the read data buffer (DK210) to the DBI register and on to the DBI bit lines to the channel. Signals channel that data byte is available.		DK120 DK110	1 2
0001 (1)		Sense Error Byte 1	Transfers 1 byte of error information to the channel.		DK110 DK130	1
	0 1 2 3 4 6 7		Error bits are gated through selector blocks on DK130 and set in DBI register on DK120. From here the byte goes through a selector block and on to the DBI on DK110 (note):	33FD fast 33FD not ready End of cylinder Missing record Read overrun Write Overrun Serial write parity check	DK520 DK520 DK610 DK610 DK610 DK610 DK610	
			Signals that error byte is available.			2
0010 (2)		Sense Error Byte 2	Same as for error byte 1. Bit 6 is not an error condition but is an indication the head is loaded or the working is not on.		DK110 DK130	1 & 2
	0 1 6			Write or erase gate unsafe Missing erase gate 33FD I/O working	DK610 DK610 DK110	
0011 (3)		Sense 33FD Control[1]	Transfers 1 byte of control information to the channel. Each bit tells the status of a specific 33FD control line (note). Bits are gated through selector block (DK130), to DBI register (DK120), and to DBI (DK110).		DK110 DK130	1
	0 1 2 3 4 5 6 7			Head load Low write current Write current gate Gated tunnel erase Access track 3/0 Access track 0/1 Access track 1/2 Access track 2/3	DK060 DK060 DK060 DK060 DK510 DK510 DK510 DK510	
			Signals channel byte is available.			2

[1] For diagnostic use.

Note: Parity not generated.

Modifier DBO 4, 5, 6, 7 (Hex)	DBI Data Bits	Command	Action Taken		ALD	Timing
0100 (4)		Sense Read Control[1]	Transfers 1 byte of control information to the channel. Each bit tells the status of a specific control line (note). Bits are gated through selector (DK130), to DBI register (DK120), and to DBI (DK110).		DK110 DK130	1
	0			Write data	DK310	
	1			Data wrap mode	DK060	
	2			Find bit sync on zeros	DK220	
	3			Sync on data bits	DK220	
	4			AM byte good	DK220	
	6			Read clock C1-C2	DK230	
	7			Read clock C2-C3	DK230	
			Signals channel byte is available.			2
0101 (5)		Sense Write Control[1]	Same as read control (note).		DK110 DK130	1 & 2
	1			CE wrap data	DK310	
	4			Write AM command	DK060	
	5			Write CRC command	DK060	
	6			Write clock C1-C2	DK320	
	7			Write clock C2-C3	DK320	
0110 (6)		Sense Bit Rings[1]	Transfers 1 byte of read bit ring and write bit ring information to the channel. Each bit tells the status of a specific read or write bit ring line (note). Bits are gated through selector (DK130), to DBI register (DK120) and to DBI (DK110).		DK110 DK130	1
	0			Read bit ring 1-4	DK230	
	1			Read bit ring 2-5	DK230	
	2			Read bit ring 3-6	DK230	
	3			Read bit ring 4-7	DK230	
	4			Write bit ring 1-4	DK320	
	5			Write bit ring 2-5	DK320	
	7			Write bit ring 4-7	DK320	
			Signals channel byte is available.			2

[1] For diagnostic use.

Note: Parity not generated.

Control Sense (Continued)

Modifier DBO 4, 5, 6, 7 (Hex)	DBI Data Bits	Command	Action Taken	ALD	Timing
0111 (7)	1 2 3 4 5 6 7	Sense Counters and CRC[1]	Transfers one byte of counter and CRC information to the channel. Each bit tells the status of a specific counter line or CRC line (note). Bits are gated through selector (DK130), to DBI register (DK120) and to DBI (DK110) (note). IMPL counter not 81 — DK510 Index counter 8 — DK530 Ready counter not 170,032 μs — DK520 CRC not zero — DK520 CRC not divide — DK420 CRC register position 1 — DK410 CRC register position 16 — DK420 Signals channel byte is available.	DK110 DK130	1 2
1000 (8)	Hex 0	CE Write Clock Advance[1]	Advances the write clock two positions. Also resets DBI register to zero and sends hex 0 to the channel (note).	DK320 DK120 DK110	1
1001 (9)	Hex 0	CE Standard Read Data Pulse[1]	Generates a gated standard read data pulse. Also resets DBI register to zero and sends hex 0 to the channel (note).	DK210 DK120 DK110	1 2
1010 (A)	Hex 0	CE Standard Read Clock[1]	Generates a gated standard read clock pulse. Also resets the DBI register to zero and sends hex 0 to the channel (note).	DK230 DK120 DK110	1 2
1011 (B)	Hex 0	CE 8F Read Clock[1]	Advances the read clock one position. Also resets the DBI register to zero and sends hex 0 to the channel (note).	DK230 DK120 DK110	1 2
1100 (C)	Hex 0	Sense for Hex 00[1]	Resets the DBI register to zero and sends hex 0 to the channel (note).	DK120 DK110	1 2
1101 (D)	Hex FF	Set DBI Register to Hex FF[1]	Sets the DBI register to hex FF. Then sends hex FF to the channel (note).	DK120 DK110	1 2
1110 (E)	Hex 0F	Set DBI Register to Hex 0F[1]	Sets the DBI register to hex 0F, then sends hex 0F to the channel (note).	DK120 DK110	1 2
1111 (F)	Hex F0	Set DBI Register to Hex F0[1]	Sets the DBI register to hex F0, then sends hex F0 to the channel (note).	DK120 DK110	1 2

[1] For diagnostic use.

Note: Parity not generated.

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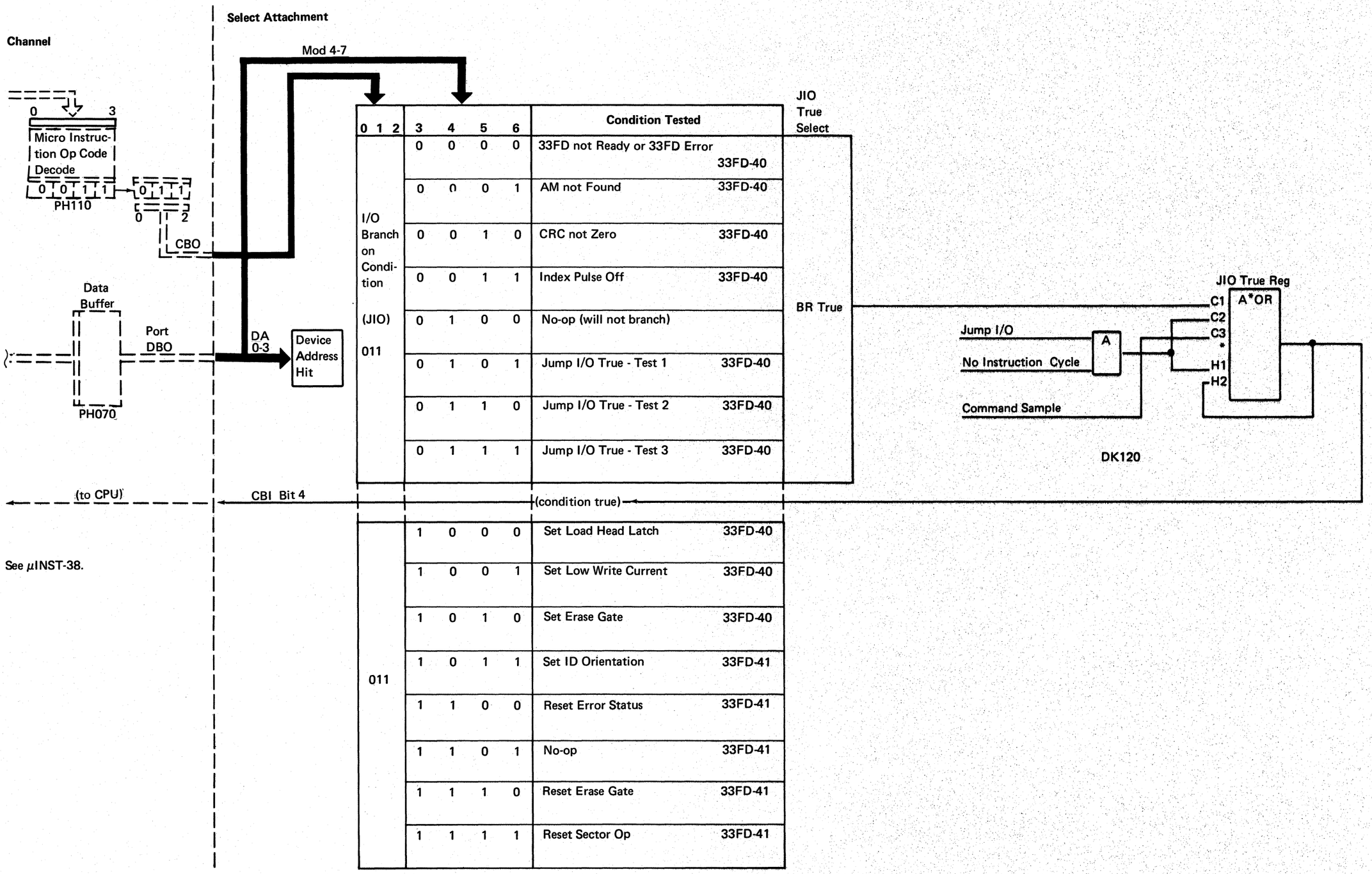
Jump I/O



0 1 2	3	4	5	6	Condition Tested	
I/O Branch on Condition (JIO) 011	0	0	0	0	33FD not Ready or 33FD Error	33FD-40
	0	0	0	1	AM not Found	33FD-40
	0	0	1	0	CRC not Zero	33FD-40
	0	0	1	1	Index Pulse Off	33FD-40
	0	1	0	0	No-op (will not branch)	
	0	1	0	1	Jump I/O True - Test 1	33FD-40
	0	1	1	0	Jump I/O True - Test 2	33FD-40
	0	1	1	1	Jump I/O True - Test 3	33FD-40
011	1	0	0	0	Set Load Head Latch	33FD-40
	1	0	0	1	Set Low Write Current	33FD-40
	1	0	1	0	Set Erase Gate	33FD-40
	1	0	1	1	Set ID Orientation	33FD-41
	1	1	0	0	Reset Error Status	33FD-41
	1	1	0	1	No-op	33FD-41
	1	1	1	0	Reset Erase Gate	33FD-41
	1	1	1	1	Reset Sector Op	33FD-41

See μINST-38.

Jump I/O (Continued)

The jump I/O command is divided into two parts:

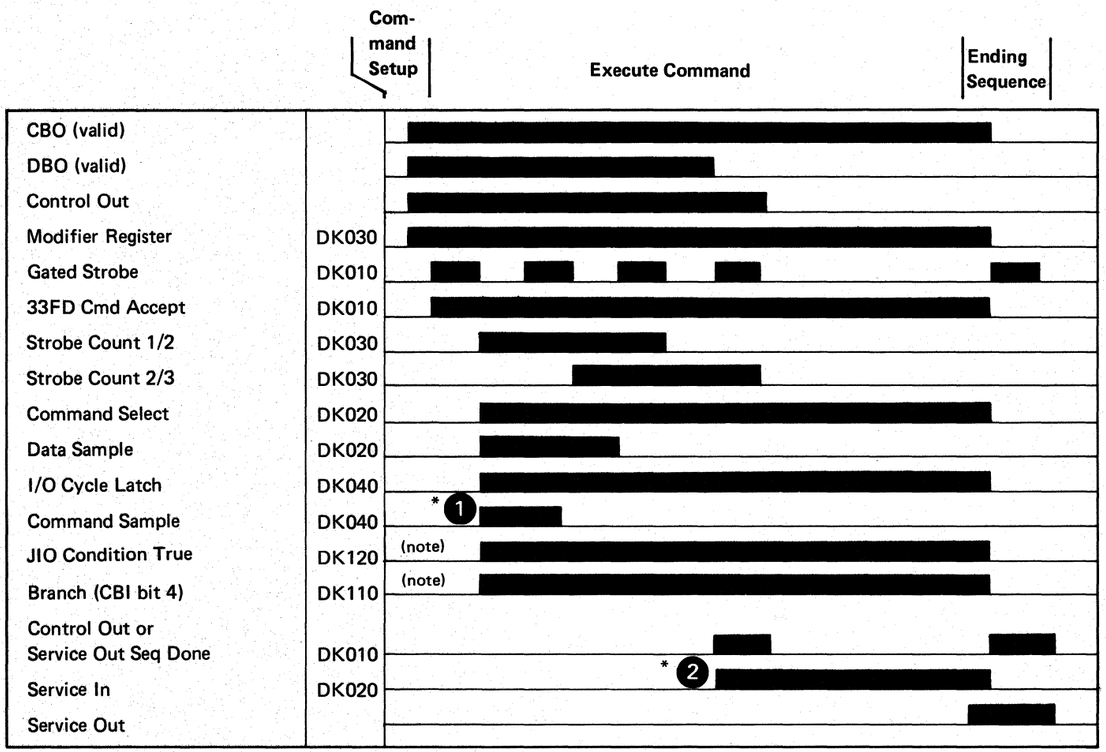
1. Part 1 commands have modifiers of hex 0 through hex 7.

2. Part 2 commands have modifiers of hex 8 through hex F.

The commands that fall within the first part test the attachment for a specific condition. If the condition is true, a positive response is sent to the CPU by activating the CBI bit 4 line. In this attachment the CBI bit 4 line is called '33FD C Stg/W-0 P/Br'*. It is so named to indicate multiple usage.

Each command that falls within the second part performs a specific function such as setting or resetting a latch. No jump test is made for this group. An explanation of these commands is on the following page.

*33FD control storage (without parity/branch).



*See 33FD-40, and 41

Note: These lines can only be activated by the JIO commands that have a modifier of hex 0 through hex 7.

Jump I/O (Continued)

Modifier DBO 4, 5, 6, 7 (Hex)	CBI Bit Note 1	Condition Tested	Action Taken	ALD	Timing
0000(0)	4	33FD not ready or 33FD error.	Tests for the following conditions and if any of the listed conditions are found, the CBI bit 4 will be sent to the CPU. Conditions tested: Not ready Running fast Read Overrun Serial write parity check Write overrun Missing erase gate Write or erase gate unsafe Missing record End of cylinder	DK120 DK520 DK520 DK610 DK610 DK610 DK610 DK610 DK610 DK610	2
0001(1)	4	AM not found	Tests the AM byte good latch. If the latch is off, CBI bit 4 is sent to the CPU.	DK120	2
0010(2)	4	CRC not zero	Tests the test CRC gen 0 latch. If the latch is off, CBI bit 4 is sent to the CPU.	DK120	2
0011(3)	4	Index pulse off	Tests the 33FD index singleshot. If singleshot is off, CBI bit 4 is sent to the CPU.	DK120	2
0100(4)		No op	Will perform normal channel sequence for JIO. No test is made and CBI bit 4 is not sent to the CPU.	DK120	2
0101(5)	4	Jump I/O true test 1	This is a diagnostic test. It tests the ability at JIO true latch to be set by; read overrun, AM not found, or CRC not zero.	DK120	2
0110(6)	4	Jump I/O true test 2	This is a diagnostic test. It tests the ability of the JIO true latch to be set by; write overrun or serial write parity check.	DK120	2
0111(7)	4	Jump I/O true test 3	This is a diagnostic test. It tests the ability of the JIO true latch to be set; not ready, running fast, write or erase gate unsafe, missing erase gate, missing record, end of cylinder, or index off.	DK120	2
1000(8)		Set load head latch	Sets the head load latch and energizes the head load magnet.	DK060 DK010	2
1001(9)		Set low write current	Sets the low current latch and decreases the current through the write head.	DK060 DK010	2
1010(A)		Set erase gate	Sets the erase latch and energizes the erase coil driver.	DK610	2

Jump I/O (Continued)

Modifier DBO 4 5 6 7 (Hex)	CBI Data Bit	Condition Tested	Action Taken	ALD	Timing
1011(B)		Set ID orientation	Sets ID orientation latch. This latch degates the set of missing record, and gates the sent of end of cylinder.	DK610	2
1100(C)		Reset error status	Resets the following conditions by activating error resets. Condition reset: Not ready—(turns on ready latch) Running fast—(resets latch) Read overrun—(resets latch) Serial write parity check (resets latch) Write overrun (resets latch) Missing erase gate (resets latch) Write or erase gate unsafe(resets latch) Missing record (resets latch) End of cylinder (resets latch)	DK610 DK520 DK520 DK610 DK610 DK610 DK610 DK610 DK610 DK610	2
1101(D)		No op	Performs the normal channel sequence for JIO but no tests are made and no latches are set or reset.		
1110(E)		Reset erase gate	Resets the erase latch and deenergizes the erase coil driver.	DK060 DK010	2
1111(F)		Reset sector op	Ends a write operation by resetting the write gate latch and the write CRC latch. Ends a read operation by resetting the read data command latch. Resets the CE mode index latch.	DK060 DK220 DK520	2 1 1

Error Conditions

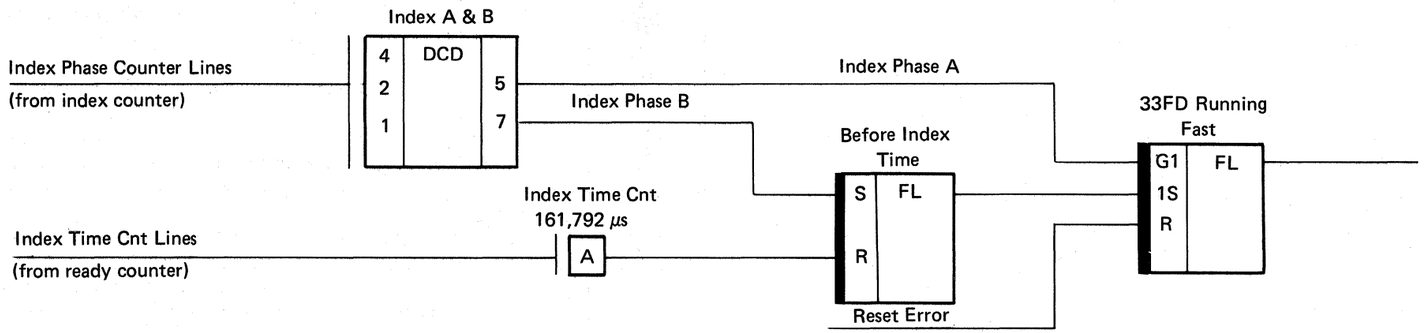
The jump I/O command with a modifier of hex 0 (33FD-38) is used to detect a 'not ready' condition or an 'error' condition. The control sense command is then required to determine the specific error (33FD-32).

Refer to ALD DK120.

33FD Running Fast

A 33FD running fast error occurs when the diskette is turning so fast that index pulses occur more often then every 161,792 μs.

The 'before index time' latch is turned on by the 'index, phase B' line. If the index counter has not counted to 161,792 μs by the time the next 'index phase A' pulse occurs, the '33FD running fast' latch is turned on.

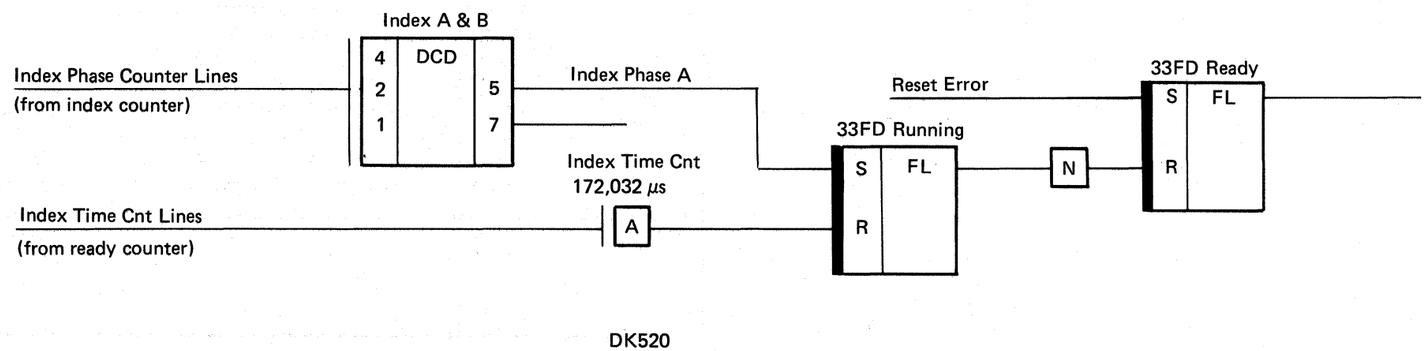


DK520

33FD Not Ready

A 33FD not ready condition occurs when the diskette is turning so slowly that index pulses occur farther apart than every 172,032 μs.

The ready counter is reset by the 'index, phase B' line. It is then allowed to advance. If the counter has not been reset again before it reaches 172,032 μs, the '33FD running' latch and the '33FD ready' latch is turned off.

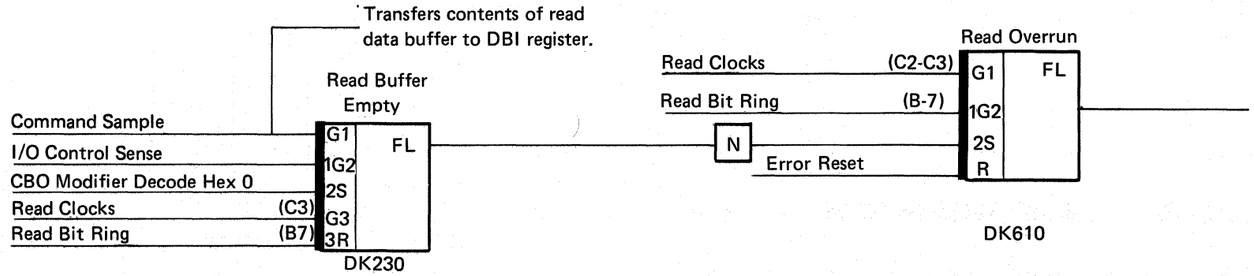


DK520

Read Overrun

A read overrun occurs when another byte of data is ready to be set into the read data buffer and the channel has not taken the previous byte soon enough.

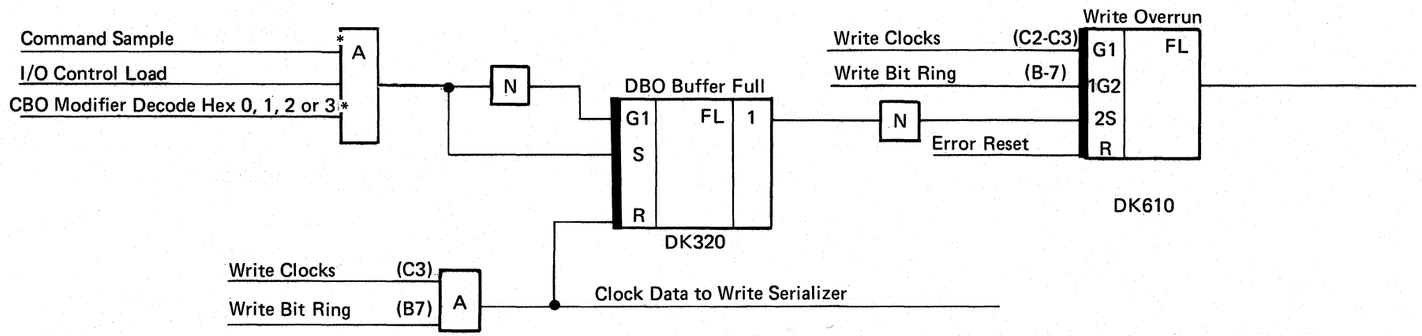
The contents of the read data deserializer is transferred to the read data buffer at B7-C3 time. If the contents of the read data buffer has not been set into the DBI register by B7-C2 time the 'read overrun' latch is set.



Write Overrun

A write overrun occurs when the attachment is ready to write another byte on diskette and the channel has not sent another byte soon enough.

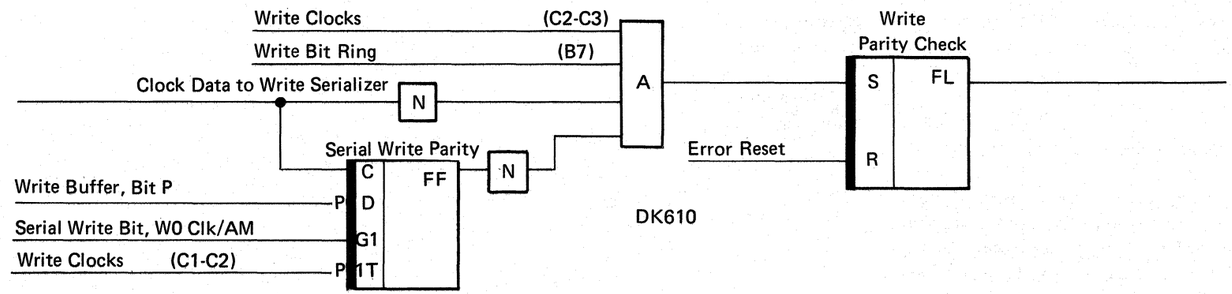
The contents of the DBO buffer register is transferred to the write serializer register at B7-C3 time. If the channel has not responded in time with another byte, the 'DBO buffer full' latch is not set and at B7-C2 time the 'write overrun' latch is set.



Write Parity Check

A write parity check occurs when an even number of bits is detected while writing a byte on diskette.

The data bits being written and the P-bit position of the DBO buffer are sent to the 'serial write parity' trigger. If the total number of bits are even the trigger will be off, and at B7-C2 time the 'write parity chk' latch will be set.



Write or Erase Gate Unsafe and Missing Erase Gate

These checks occur if write or erase current is not active when it should be. They also detect if write current is active when it should not be.

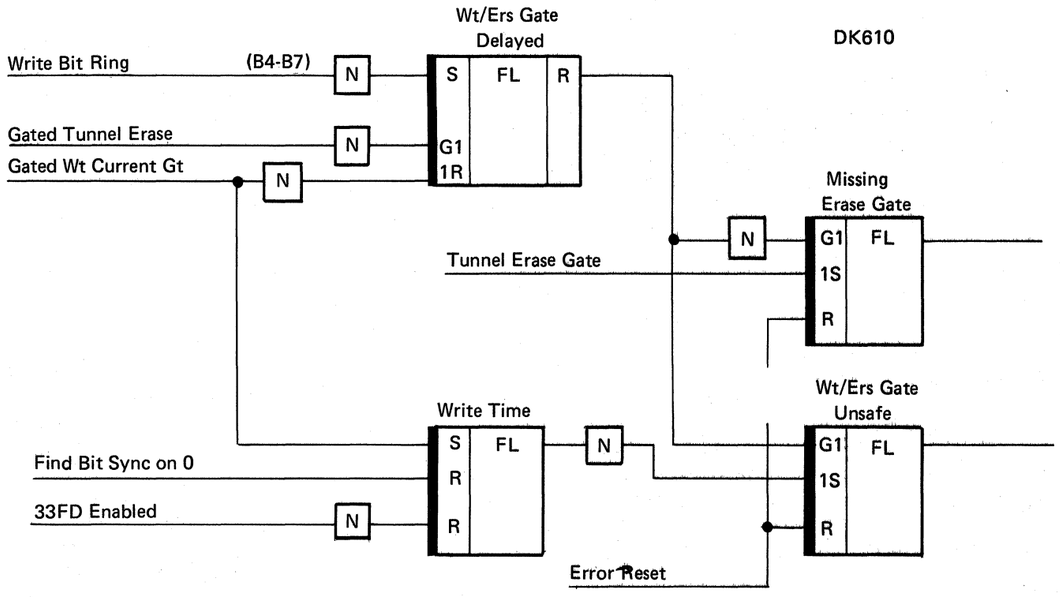
These checks occur if write or erase current is not active during a write operation. The circuits also detect if write current is active when a write operation is not in progress.

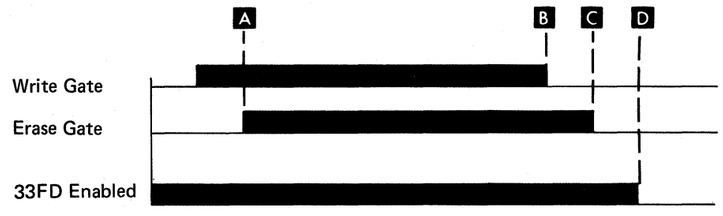
Due to the erase head being offset from the write head, 'erase gate' and 'write gate' are not turned on at the same time. The relative times are shown in the accompanying timing chart.

'Write gate' causes the write clocks and bit ring to run and will activate 'gated write current gate'.

'Erase gate' activates 'tunnel erase gate' and 'gated tunnel erase'. As pointed out in the error explanations, it is significant that due to circuit delays, 'gated wt current gt' becomes active slightly after 'tunnel erase gate'.

Error Condition	Explanation
'Gated wt current gt' missing at A.	'Write time' latch does not turn on at end of B4-B7 time, 'WT/ERS gate delayed' turns on causing the 'WT/ERS gate unsafe' latch to turn on. In addition because 'gated tunnel erase' comes up slightly after 'tunnel erase gate' the 'WT/ERS gate delayed' is held reset for this slight period of time and 'missing erase gate' latch is also turned on.
'Gated tunnel erase' is missing from B to C.	'WT/ERS gate delayed' latch is reset and the 'missing erase gate' latch is turned on.
'Gated wt current gt' is active at C.	'WT/ERS gate delayed' is not reset. At D when the 33FD is disabled, the 'write time' latch is forced off and the 'WT/ERS gate unsafe' latch is turned on.
'Gated tunnel erase' stays active after C.	'WT/ERS gate delayed' is not reset. At D when the 33FD is disabled, the 'write time' latch is forced off and the 'WT/ERS gate unsafe' latch is turned on.





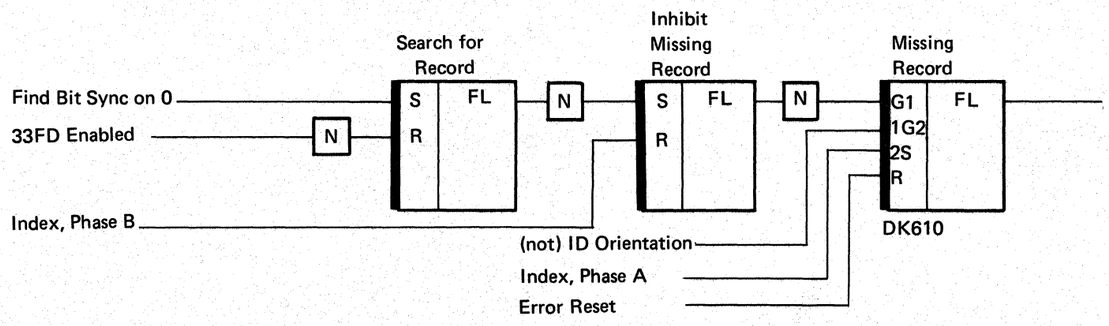
Missing Record

A missing record error occurs when the record being searched for has not been found by the time two index pulses have been sensed.

A find ID operation is initiated by the 'search for AM byte' command. At the start of the search 'find bit sync on 0' is activated and the 'search for record' latch turns on removing the set to the 'inhibit missing record' latch. The next 'index phase B' turns the 'inhibit missing record' latch off providing a set gate for the 'missing record' latch.

After an ID field has been found, the 33FD is disabled resetting the 'search for record' latch and turning on the 'inhibit missing record' latch, thus degating the 'missing record' latch.

If the search for an ID field has not been successful, the next 'index, phase A' sets the missing record' latch.

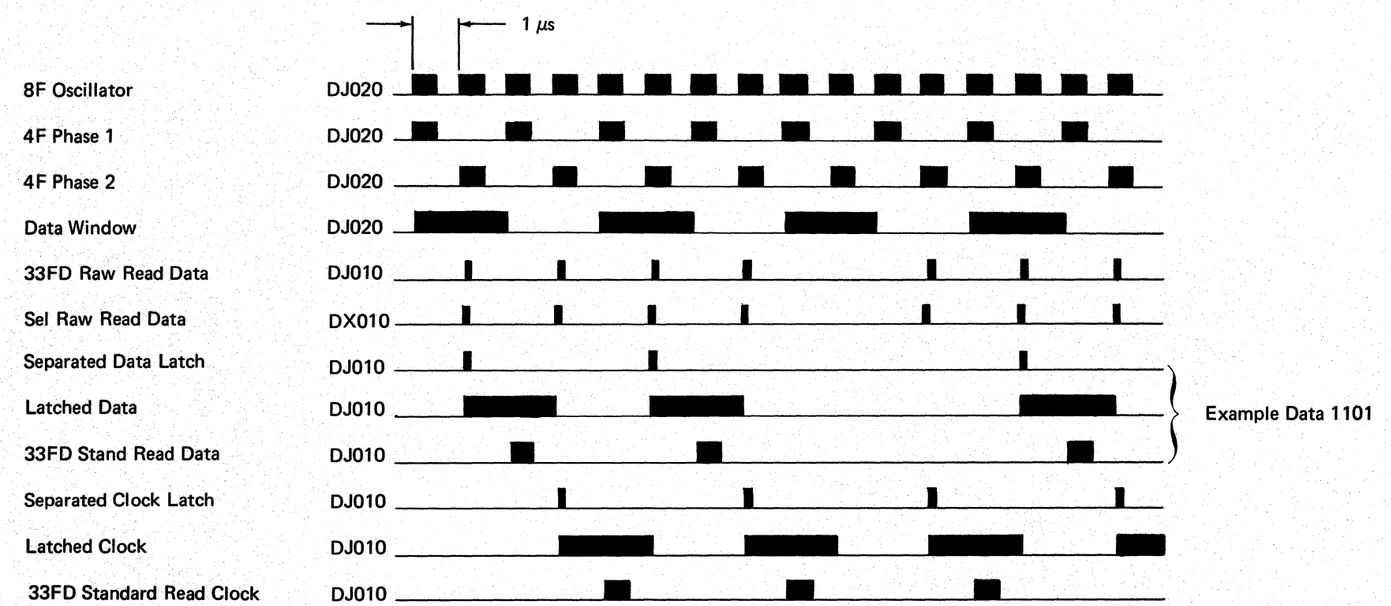


Data Separator

Separate data pulses from clock pulses.

The data separator oscillators have been synchronized with '33FD raw read data' from disk. As a result, data pulses occur when the 'data window' line is active and clock pulses occur when 'data window' is inactive.

Refer to ALD DJ010 and DJ020.



Index Counter

The index counter provides timing pulses that are used during the time the index singleshot is active. The counter is reset to zero and reset held until the index SS is activated. Advance pulses then advance the counter until the count reaches eight. At this point the advance pulses are stopped and the counter remains at eight until the index SS turns off. The counter is then reset to zero.

If the index pulse does not last until the counter reaches four, the pulse is not considered a valid index pulse and the counter is reset.

Ready Counter

The ready counter is a binary counter used to check the rotational speed of the 33FD. It is reset every time an index pulse is sensed. Between index pulses it is allowed to advance with each 'chan 512 ns osc' pulse.

The output of the counter is sent to the speed check control circuits where it can be determined if the diskette is running too fast or too slow (33FD-42).

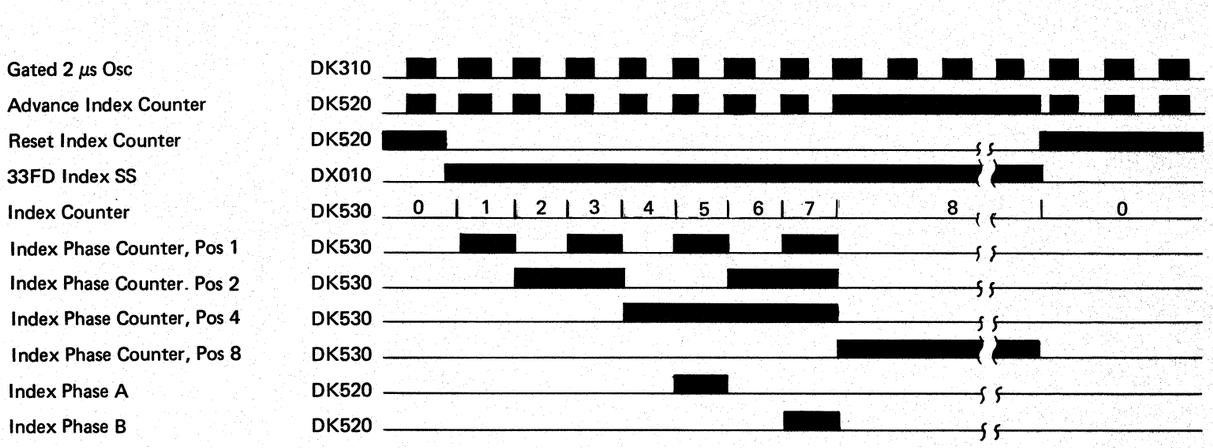
Refer to ALD DK530.

IMPL Counter

Used to control recalibrate operation during IMPL.

The 'IMPL counter' serves two functions during IMPL. It counts the number of one track seeks (80) and controls the bits being set in the 'seek track register'. The counter is reset to 1 and during the IMPL operation advances at each 'index, phase B' time.

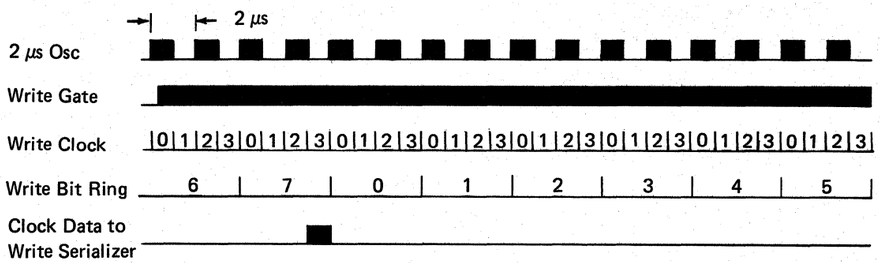
Refer to ALD DK530.



Write Clock and Write Bit Ring

Provides clock timings for write operations.

The advance of the write clock and write bit ring is controlled by 'write gate'. The write clock steps with both the rise and fall of the 'gated 2 μs osc' line any time 'write gate' is active. The write bit ring is reset to 6 when 'write gate' is inactive.

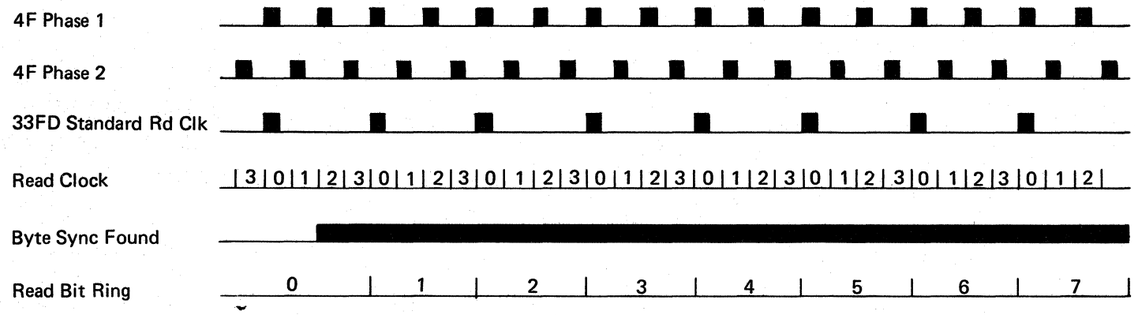


Read Clock and Read Bit Ring

Provides clock timings for read operations.

The read clock runs continuously except when in diagnostic step mode. However, the read bit ring only runs after the AM byte has been found when reading. After the first data bit of the AM byte is found, the 'byte sync found' latch is turned on allowing the read bit ring to step. Byte synchronization is obtained becuase the first data bit of an AM byte is always a 0 bit.

Refer to ALD DK220.



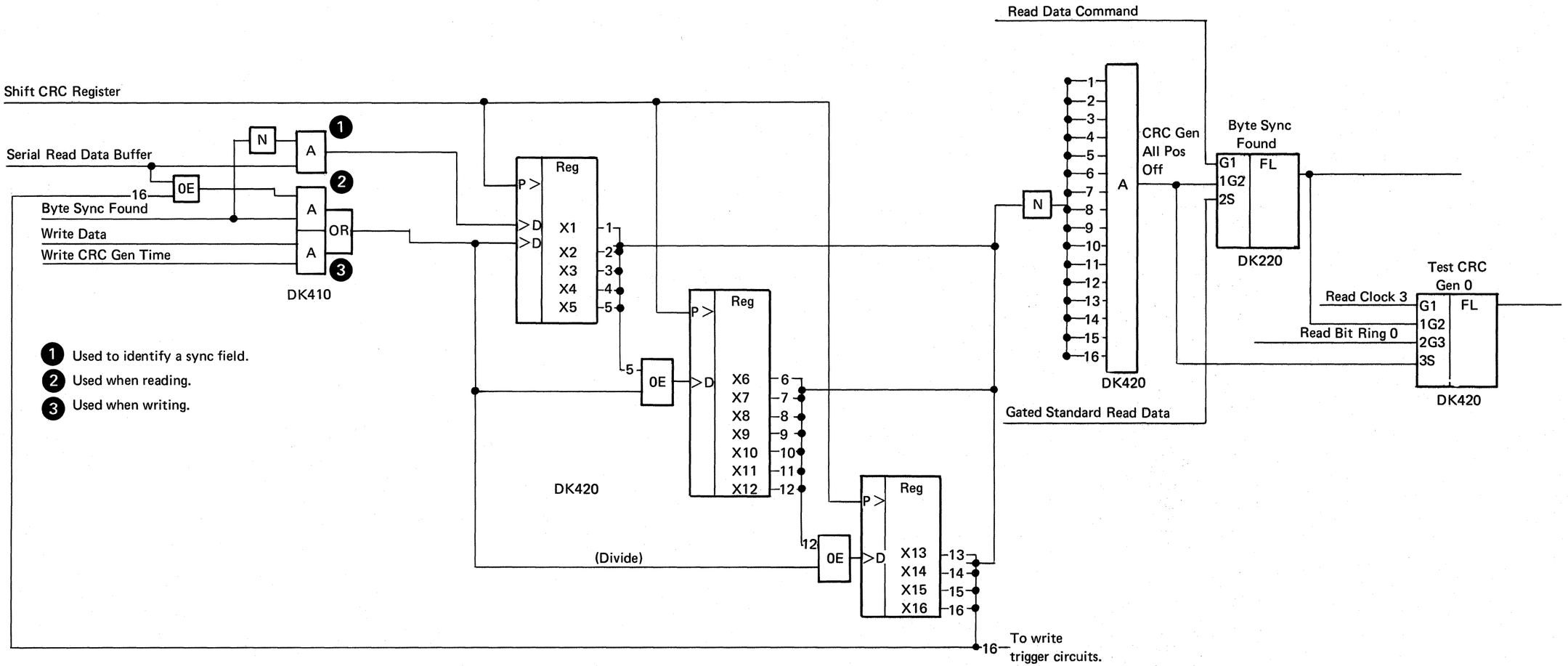
CRC Shift Register

- Used to check the reading of data.
- Used to generate two CRC bytes when writing.
- Used to identify sync fields.

When reading or writing, the CRC shift register functions as three separate shift registers connected by exclusive OR circuits. When the CRC shift register is used to identify sync fields, the bottom legs of the connecting exclusive ORs are never active and funcitonally the three registers now become a single 16 position shift register.

A sync field consists of 6 bytes of clock bits (no data bits). Consequently AND block ❶ is never made when reading a sync field. After reading 16 clock bits of a sync field all positions of the shift register will be off regardless of their status at the start. The first data bit in the AM following the sync field will turn on the 'byte sync found' latch.

When reading or writing, the shift register must be considered as consisting of the three previously mentioned parts. The shifting of bits from one part to the next, or from the last back to the first is controlled by the exclusive ORs. For example, position X6 can turn on with the shift pulse when position X5 is on or the 'divide' line is active; position X6 will not turn on if neither or both inputs to the exclusive OR are active.



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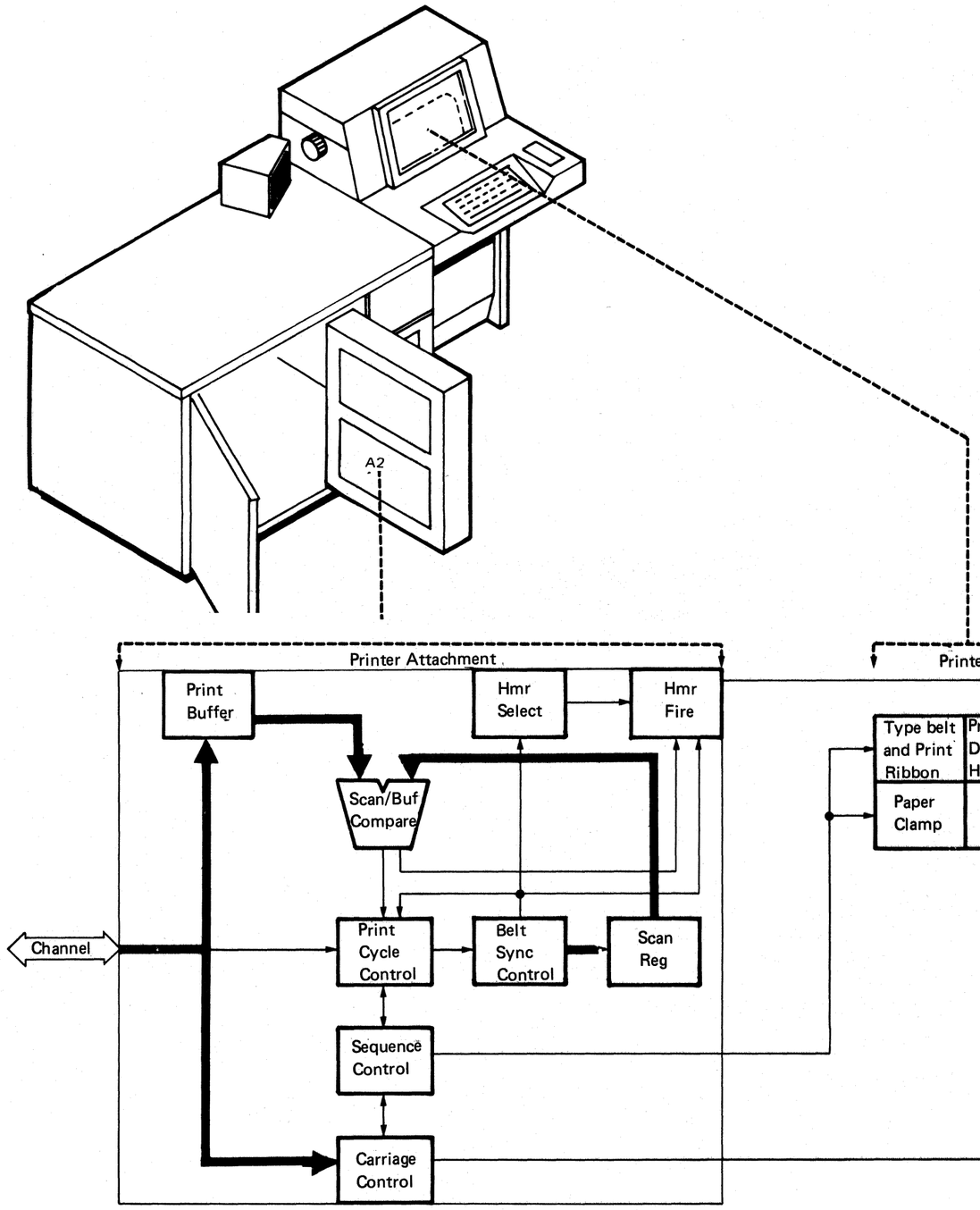
Printer

This belt printer is permanently mounted in the system. Data is sent to the print hammers. The print hammers push the paper to be printed against a continuously turning type belt and printing takes place.

Circuitry Location

The printer circuitry is housed in two separate areas: in and on the printer, and on the 01-A2 board (I/O board).

The 50, 100, and 155 line-per-minute printers share common theory information. However, due to extensive electrical and mechanical differences in the 285 line-per-minute printer, a separate subsection has been written for its theory. This subsection begins on PTR-51.



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CPU/Attachment/Printer Operation

Printer operation is controlled by the microprogram commands in the CPU. The commands are:

LOAD
CONTROL LOAD
SENSE
CONTROL SENSE
JUMP I/O

Interrupts if enabled occur at the completion of a printed line, a carriage function, or when the elapsed time counter reaches zero. The next command is then initiated.

Data Area

Output data flow to the printer is from a 132-byte I/O area in main storage, called the line printer data area. Beginning at the leftmost byte, this data area in main storage corresponds character for character to the print line beginning at print position one.

Belt Image Area

A character set image is defined as the sequence of print characters as they appear on the type belt. Before printer operations begin, a given character set size must be provided and the image must be loaded into the belt image area of control store. For reference by the printer microcode, the belt image is then transferred to main storage location.

Three character sets are available: 48, 64, and 96. The 48-character set is:

A-Z 0-9 $, . + - * / % @ # & '

The 64-character set consists of the above 48 characters plus the special characters:

( ) = _ : ; " ? ¢ > < | ! ¬ \

The 96-character set includes all characters in the 48-character set, the lowercase alphabetic characters, plus the following special characters:

[ ] ! ¼ _ : " + ² ¶ ◦ ± ¢ ( ) ; ½ ? = ® § ³ £ '

Forms Control

Forms movement is also controlled by the printer microprogram. Forms length must first be defined by the program located in control storage. The printer must also be initialized to a line within that forms length. The maximum length of forms is 84 lines.

The forms length and current print line values (destination print line when the carriage is moving) are maintained by the printer microprogram.

End of Operation Interrupts

Any operation initiated by the printer microprogram results in an interrupt at the end of the operation. These interrupts are processed by the microprogram. Any checks that occurred during the execution of the completed operation are handled immediately to prevent loss of the check status.

Attachment Operation

A print buffer is located in the attachment. It permits overlap of line printing and carriage spacing with other I/O device operations and CPU execution.

The data in the print buffer is compared to the value of the scan register. If they are equal, the corresponding hammer is selected and fired.

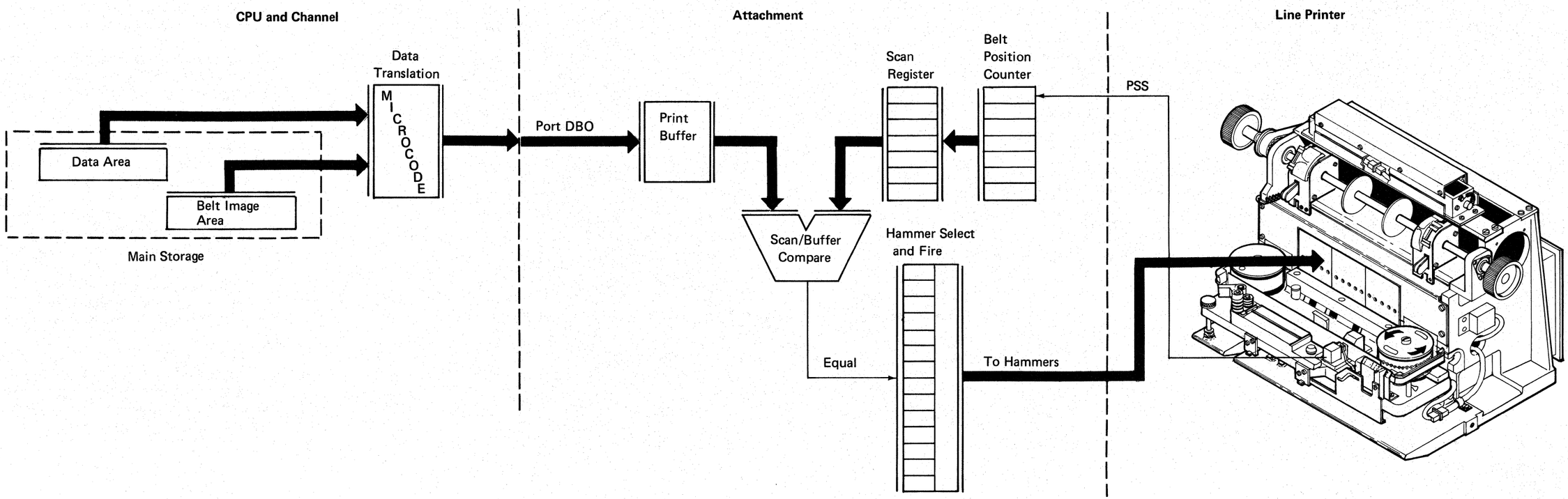
The data area, located in main storage, containing the print line is not changed by printing. This leaves the complete print line available for error recovery procedures (ERP).

The following keyboard functions are provided for operator control of the printer:

Carriage restore
New line (space one line)
Reset line counter to 1 (tells the system the form is on line 1).

When the printer function keys are used, all pending check conditions are reset prior to executing the function. Also an interrupt occurs at completion of the function, thus initiating any pending operations (commands).

Display of check or not ready conditions, and recovery procedures are provided by the display screen. Operator response is always through the keyboard.



Theory of Printing (50, 100, and 155 lpm)

The belt printer has 66 hammers, one hammer for each two print positions. Therefore, to print one line of 132 positions, each hammer is fired twice. The print operation is separated into these functions:

- *Subscans:* A subscan is the time required to option every tenth print position to every fourth belt position. Five subscans make one print scan.
- *Print scan:* A print scan is the time required to option one character to all odd print positions or all even print positions.
- *Print line:* A print line is 48 odd print scans and 48 even print scans for a 48-character set[1] (standard). That is, every character on the set is optioned to every print position.

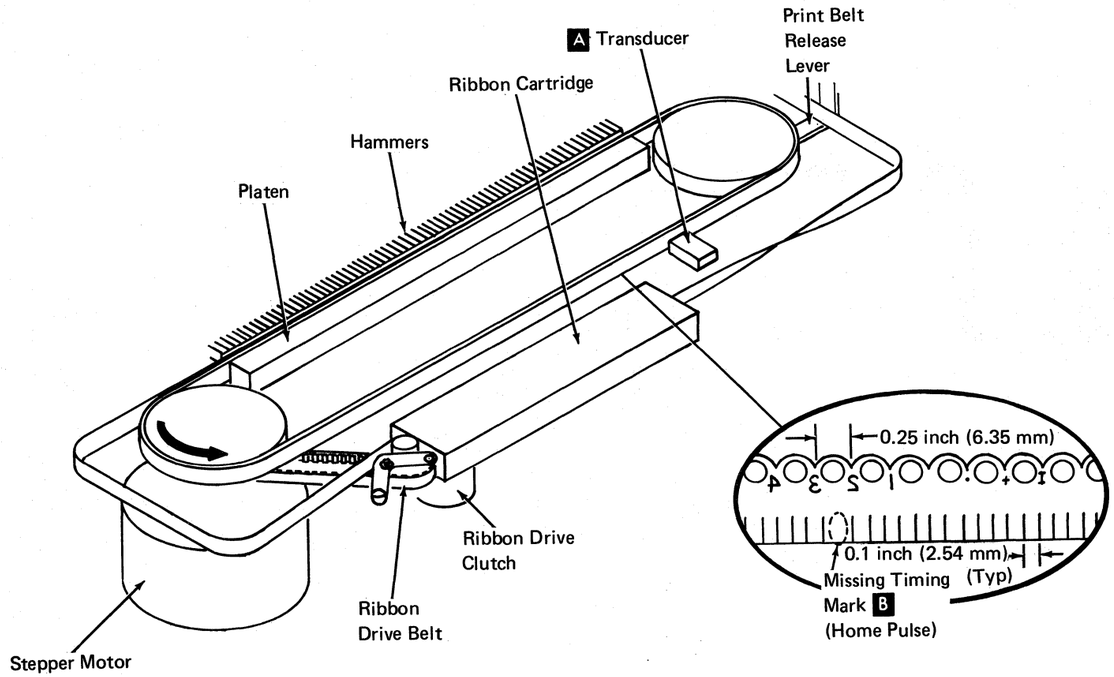
Each print position can print only one character per print line (when the print position is optioned and the character specified for that position is equal to the character aligned at that position).

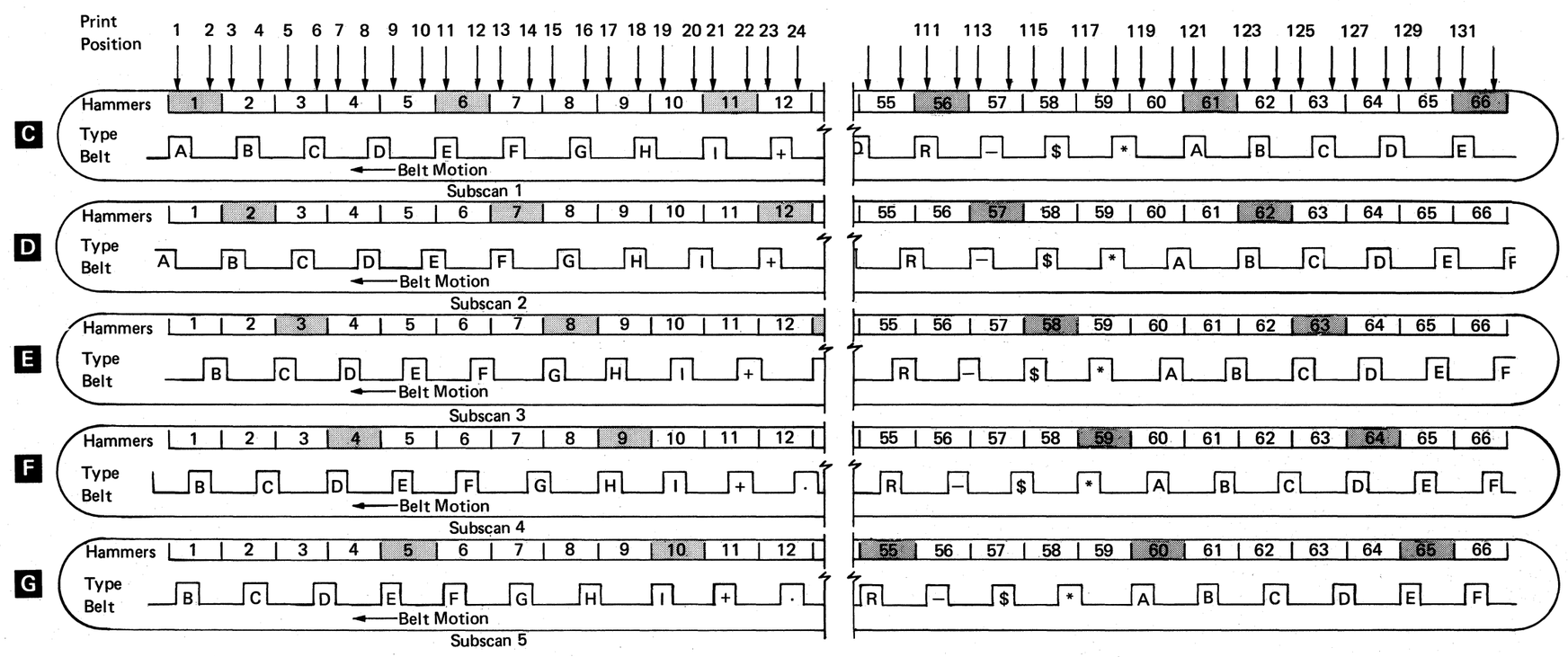
During a subscan, the hammers selected for firing are buffered in the attachment, and they are gang-fired at the start of the next subscan. Odd or even print scans are stopped early if all optioned hammers are fired.

To synchronize the type belt to the attachment, two types of pulses are required—a home pulse and the subscan pulses.

The home pulse is generated from the type belt by the transducer **A** sensing the missing timing mark **B** that identifies the home position. The home pulse occurs one subscan before the first character of each character set is aligned to print in position 1. Sensing the first home pulse initiates a continuing check of the synchronism of the home pulse with the belt position counter.

[1]The subscan pulses are generated by the transducer. Detecting the 64-character set takes 64 odd print scans and 64 even print scans. Two subscan pulses are developed from each timing mark.





Theory of Printing (50, 100, and 155 lpm)—Continued

When synchronism is verified (sensing a second home pulse) printing can start.

Because the printer has a continuously moving type belt, the attachment must determine when to fire a hammer to print the specified character. Using the illustration C as a reference, observe the relationship between the moving type belt and the hammer positions. This shows the character A aligned with hammer 1 in print position 1.

Print optioning can start when a character is aligned with print position 1. The belt position counter keeps track of what character is aligned to print in print position 1. This value is set into the scan register at the beginning of each print scan. During the first hammer option cycle, the character specified for position 1 is compared to the character aligned at position 1. During this first subscan, every tenth position (1, 11, 21, 31, 41, etc) is compared with its respectively aligned character (every fourth belt character). If the character specified and the character aligned compare equal, the hammer is fired at the beginning of the next subscan D . This sequence, starting at print position 1, is called subscan 1.

At the end of subscan 1, the type belt movement aligns the character B with print position 3 and hammer 2, as shown in the illustration D . Print optioning now continues with print position 3 and proceeds through every tenth print position until the character aligned with print position 123 is optioned. This sequence, starting with print position 3, is called subscan 2.

Belt movement has now aligned the character C with print position 5, as shown in the illustration E . Print optioning continues for every tenth position until the character aligned with print position 125 is optioned. This sequence, starting with print position 5, is called subscan 3.

Subscans 4 and 5 follow the same pattern (illustration F and G). Subscan 4 starts optioning with print position 7 and every tenth position through print position 127. Subscan 5 starts optioning with print position 9 and every tenth position through print position 129. These five subscans make the first odd print scan.

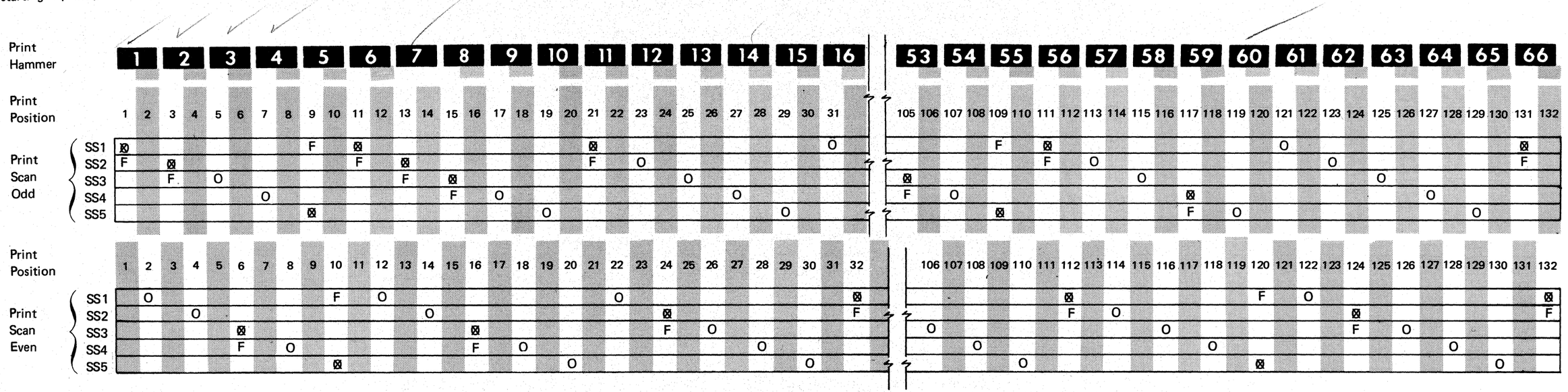
During this first odd print scan, each of the odd print positions was optioned to print one character, but only those hammers are fired that had the aligned character compare equally with the specified character.

The first print scan started with character A aligned at print position 1. Now, the character B is aligned with print position 1 and the second print scan is started.

After the second five subscans, all odd positions are now optioned to print a second character. To option the 46 remaining characters to each odd print position, 46 more odd print scans are taken.

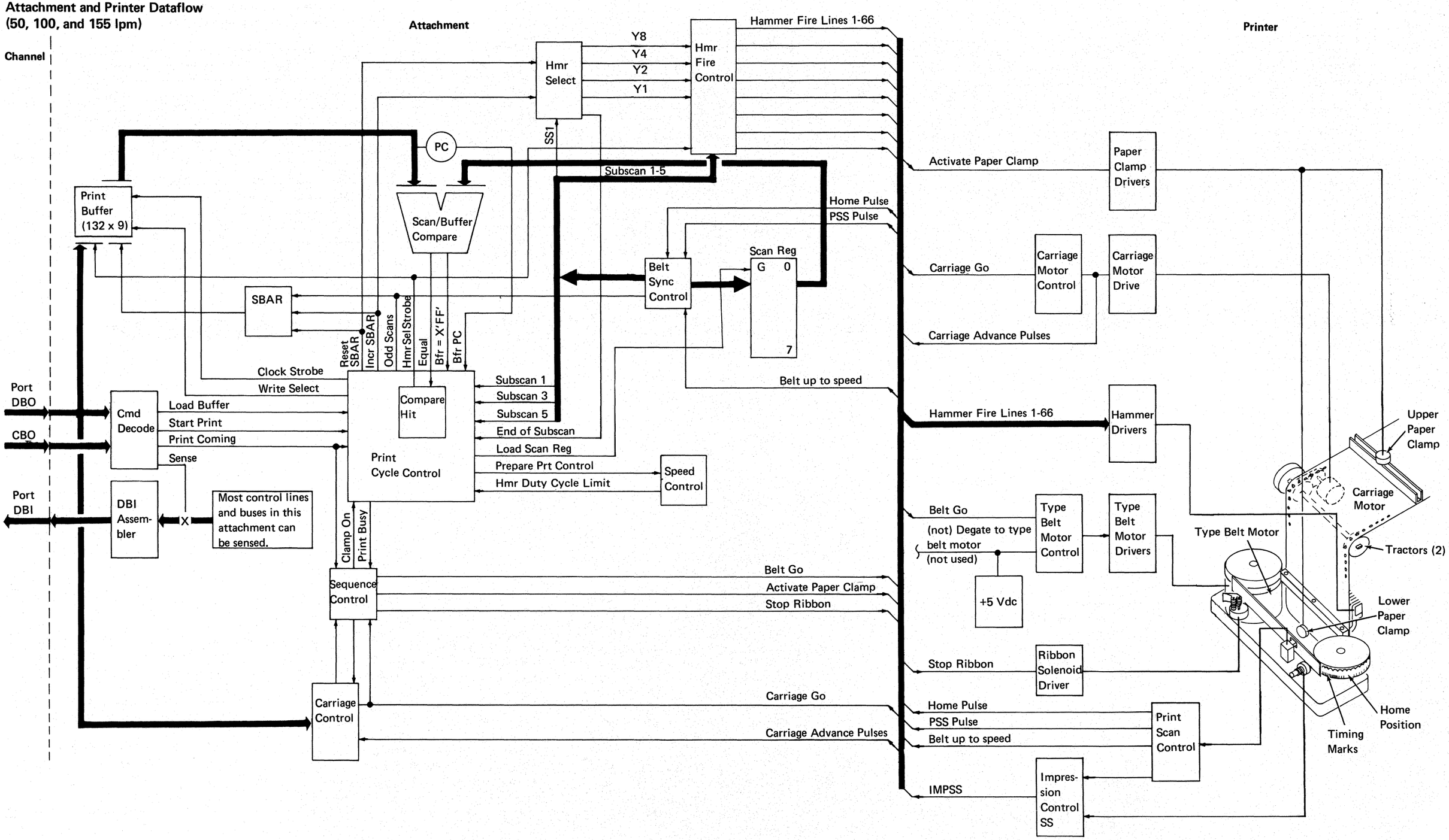
Hammers are fired for the optioned print positions that compare equal on each succeeding subscan. To reduce the hammer power requirements, only five hammers are allowed to fire on one subscan. If more than five optioned print positions compare equal, optioning starts again with 48 new print scans. Scanning starts again at print position 1 and positions not printed are optioned again.

After the 48 odd print scans, there is a delay (18 dummy subscans) to allow the hammers to fire and settle. Then the even positions are scanned starting with print position 2 and every tenth position through print position 132 on subscan 1. Subscan 2 starts with print position 4 and every tenth position through print position 124. Subscan 3 starts with print position 6 and every tenth position through print position 126; subscan 4 starts with print position 8 and every tenth position through print position 128; subscan 5 starts with print position 10 and every tenth position through print position 130. This sequence continues through 48 even print scans to option every character on the type belt to every even print position. An additional print scan (49) is taken to fire hammers selected during subscan 5 of print scan 48.

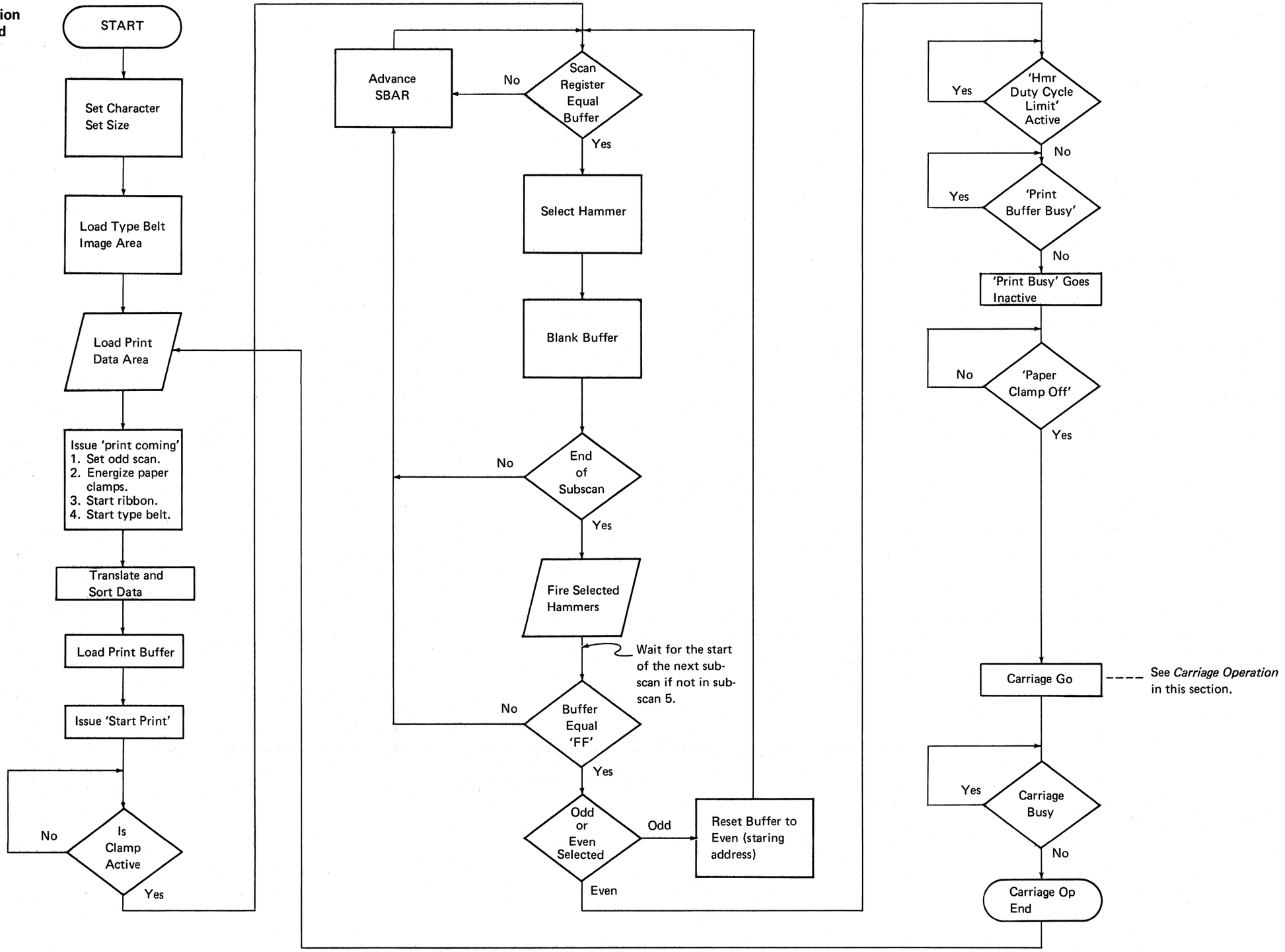


⊠ or O Hammer optioned (every 10th print position)
⊠ Hammer optioned and compare equal
F Hammer fired (fired on subscan after compare equal)

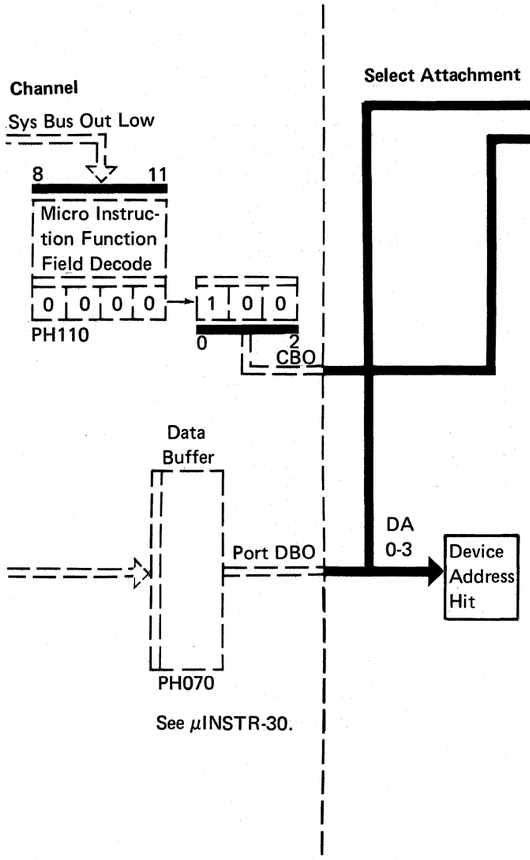
Attachment and Printer Dataflow (50, 100, and 155 lpm)



Print Operation (50, 100, and 155 lpm)



Load Command



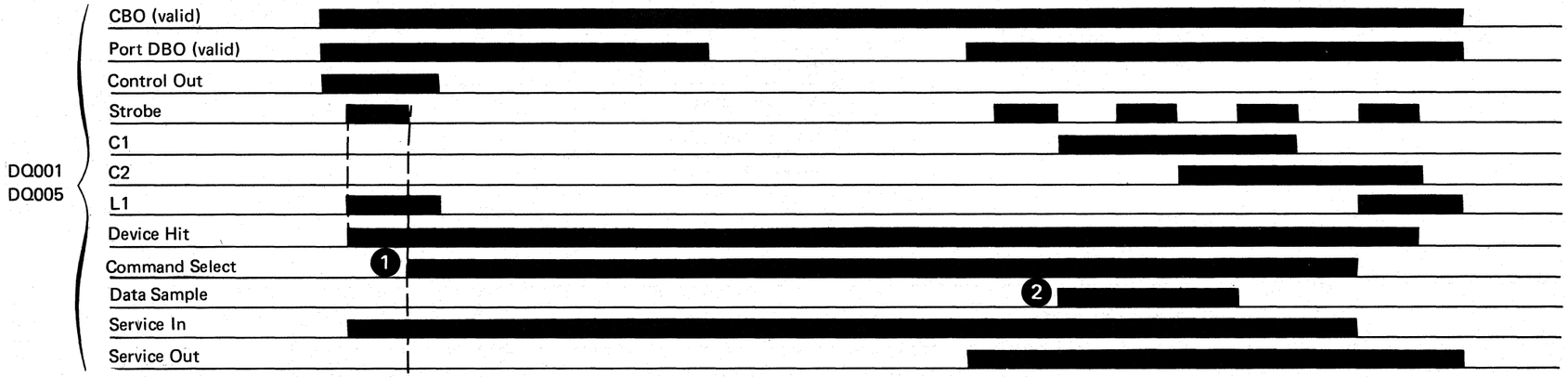
Send Data Byte to Attachment
DBO 0-7

Mod 4-7

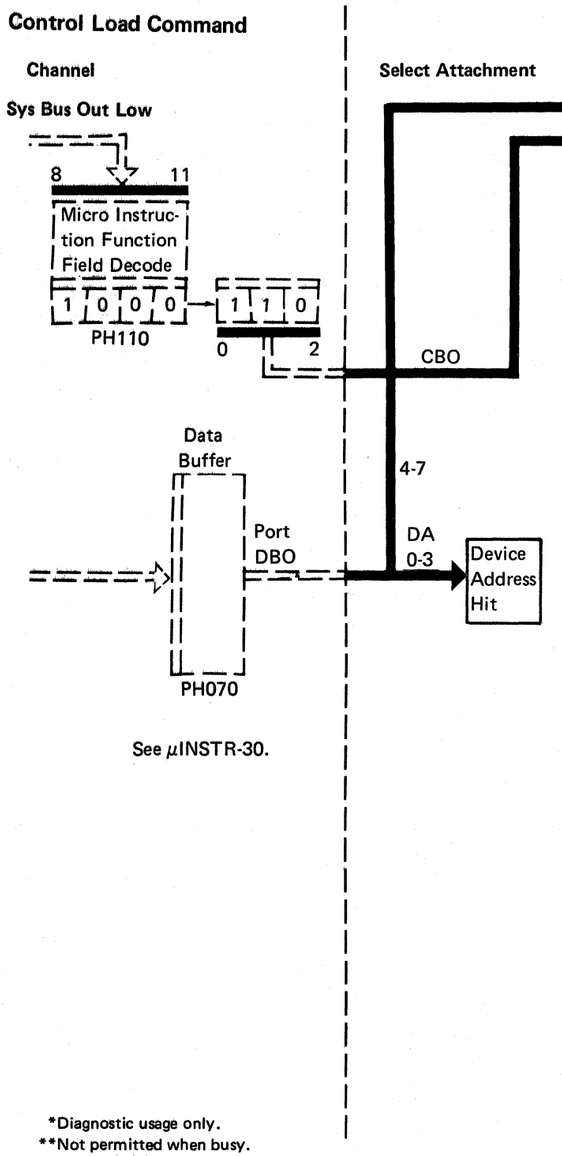
CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 0 0	0 0 1 0 Set Interrupt Request								
	0 0 1 1 Reset Interrupt Request								
	0 1 1 0 Interrupt Request Control				Print Busy Off	Carriage Busy Off			Elapsed Time Counter
	1 0 0 1 Print Buffer**	Data to Print Buffer							
	1 0 1 1 Enable Diagnostic Mode*								
	1 1 0 0 Disable Diagnostic Mode*								
	1 1 0 1 Diagnostic Mode Control Byte*	2 μs Osc	Subscan	Home		Motor Up to Speed	Coil 1 Current	Coil 2 Current	Coil 3 Current
	1 1 1 1 Check Reset								

*Diagnostic usage only.
**Not permitted when busy.

Load Command (Continued)



Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
0010(2)		Set Interrupt Request	Sets the micro interrupt request latch which initiates an interrupt.	DQ270	1
0011(3)		Reset Interrupt Request	Resets the micro interrupt request latch.	DQ270	1
0110(6)	3	Interrupt Request Control	Turns on the interrupt print op end latch which allows the micro interrupt request latch to be turned on when print busy latch turns off.	DQ270	2
	4		Turns on the interrupt carriage op end latch which allows the micro interrupt request latch to be turned on when the carriage busy latch turns off.	DQ270	
	7		Turns on the interrupt elapsed 0 latch which allows the micro interrupt request latch to be turned on when the elapsed time counter reaches 0.	DQ270	
1001(9)	0-7	Print Buffer	Used to load the print buffer with the data on port DBO.	DQ180	2
1011(B)		Enable Diagnostic Mode	Turns on the diagnostic mode latch which is used to substitute test signals for actual signals (such as type belt emitter pulses).	DQ200	1
1100(C)		Disable Diagnostic Mode	Resets the diagnostic mode latch (see above).	DQ200	1
1101(D)	0	Diagnostic Mode Control Byte	Allows port DBO 0 bit to step the clocking triggers instead of the 1 μs osc.	DQ170	2
	1		Allows port DBO 1 pulse to be used to generate the subscan pulses instead of the raw PSS pulses.	DQ200	
	2		Uses port DBO 2 to represent home pulse rather than the actual home pulse.	DQ210	
	4		Substitutes the port DBO 4 bit for the motor up to speed line.	DQ260	
	5		Uses port DBO 5 in place of the coil 1 current line.	DQ090	
	6		Uses port DBO 6 in place of the coil 2 current line.	DQ090	
	7		Uses port DBO 7 in place of the coil 3 current line.		
1111(F)		Check Reset	Resets all pending checks and brings up printer reset.	DQ090	1



Select Attachment

Send Data Byte to Attachment
DBO 0-7

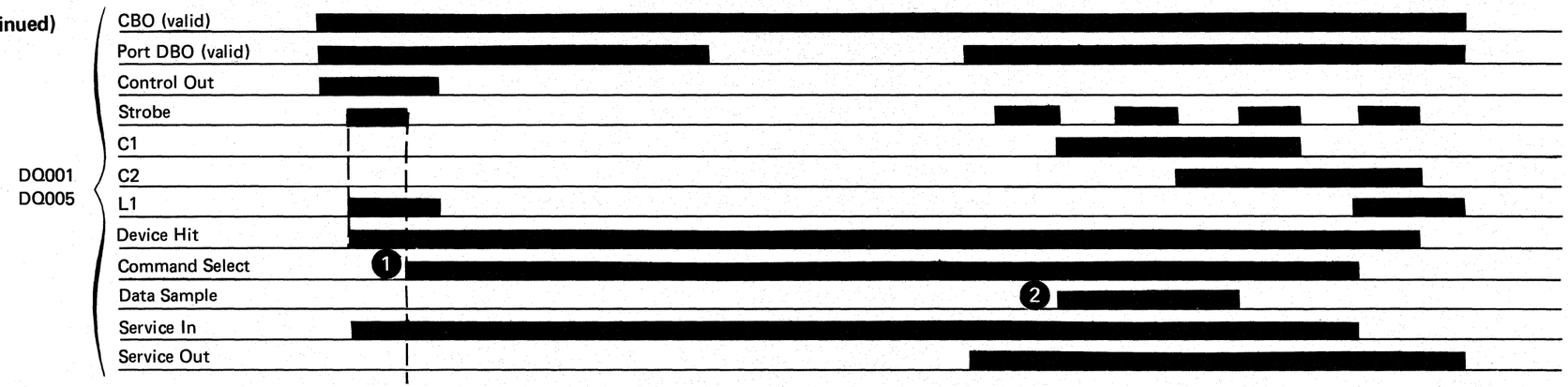
Mod 4-7

CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 1 0	0 0 0 0 Diagnostic Adapter Control*	Select Odd Scans	Select Even Scans	Reset Hammer Matrix	Force Motor Up-to-Speed	Turn Motor On	Drop 24V to Hammers	Printer Reset	Reset CE Latch
	0 0 0 1 Character Set Size		Character Set Size Code						
	0 0 1 0 Diagnostic Hammer Control*					Y8	Hammer Select Latch Y4	Y2	Y1
	0 1 0 0 Enable Adapter								
	0 1 0 1 Disable Adapter								
	1 0 0 0 Reset Scan Buffer Address**								
	1 0 0 1 Print and Space Control	Start Printing	Enable EOF Detect	Disable EOF Detect	Print Coming			Disable Forms Jam Detect	Enable Forms Jam Detect
	1 0 1 0 Special Functions		Set Diagnostic Print Busy	Reset Diagnostic Print Busy	Start Timer	Set Carriage Reverse***	Reset Carriage Reverse***		
	1 0 1 1 Carriage Space Counter		Set Space Counter Value						
	1 1 0 0 Diagnostic Carriage Control*		Carriage Go	Carriage Stop	Activate Paper Clamp	Deactivate Paper Clamp	End Carriage Space Time		
	1 1 0 1 Elapsed Time Counter		Set Elapsed Time Counter Value						

Bit 1	Bit 2	
0	0	48-Character Set
0	1	64-Character Set
1	0	96-Character Set
1	1	128-Character Set (Katakana)

*Diagnostic usage only.
**Not permitted when busy.
***Half Line Space Feature only.

Control Load Command (Continued)



Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
0000(0)	0	Diagnostic Adapter Control	Turns on the odd scans latch.	DQ110	
	1		Sets the odd scans latch off.	DQ110	
	2		Turns on the hammer matrix reset latch which resets the hammer fire circuitry.	DQ210	
	3		Turns on the belt start complete latch which brings up motor up-to-speed.	DQ220	2
	4		Turns on the belt go latch which allows the print belt motor to start up.	DQ220	
	5		Sets the coil check counter to 8, setting coil check on.	DQ090	
	6		Turns on the printer reset latch.	DQ090	
	7		Turns off the CE latch. The latch is turned on by attaching the input (set) to a desired test point.	DQ250	
0001(1)	0-1	Character Set Size	Depending on the condition of these 2 bits (on or off) the character set size is set in latches 0 and 1 (00 = 48, 01 = 64, 10 = 96, 11 = 128).	DQ190	2
0010(2)	4-7	Diagnostic Hammer Control	Allows the hammer select control value to be set to fire a certain hammer.	DQ290	2
0100(4)		Enable Adapter	Turns off the adapter reset latch.	DQ090	1
0101(5)		Disable Adapter	Turns on the adapter reset latch.	DQ090	1
1000(8)		Reset Scan Buffer Address	Resets the SBAR to 0.	DQ110	1
1001(9)	0	Print and Space Cycle Control	Turns on the start printing latch which initiates the printing sequence.	DQ110	
	1		Turns on the EOF enabled latch.	DQ210	
	2		Resets the EOF enabled latch.	DQ210	2
	3		Set odd(scan) latch, paper clamp, print belt go and ribbon go.	DQ220	
	6		Holds system sense byte 0, bit 0 off to prevent forms jam from being detected.	DQ210	
	7		Allows forms jam to be detected.	DQ210	
1010(A)	1	Special Functions	Turns on the diagnostic print busy latch.	DQ310	
	2		Turns off the diagnostic print busy latch.	DQ310	2
	3		Enables the elapsed time counter to be stepped by the 1 ms oscillator.	DQ300	
	4		Initiates a half line space operation.	FJ101	
	5		Resets a half line space operation.	FJ101	

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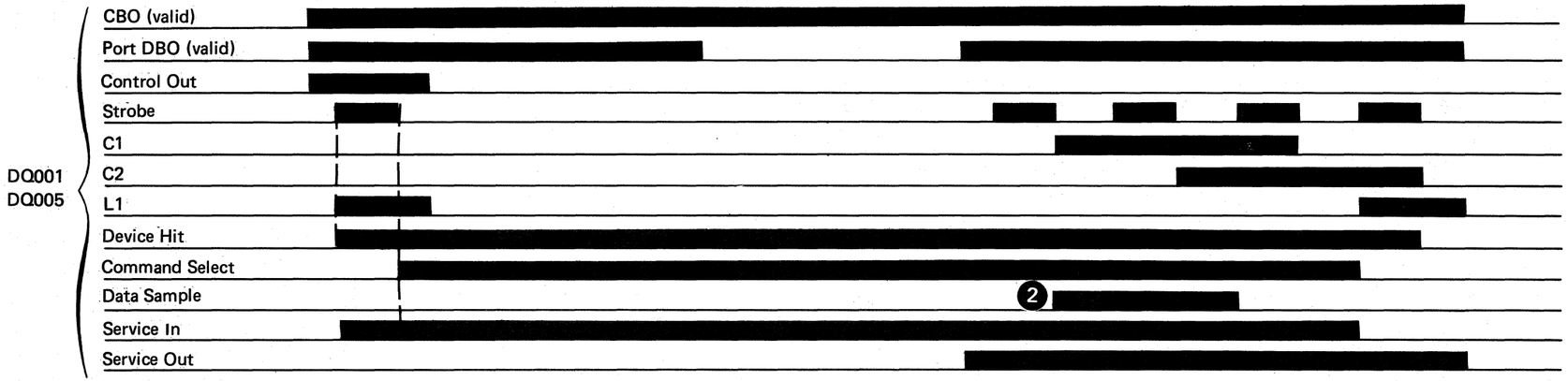
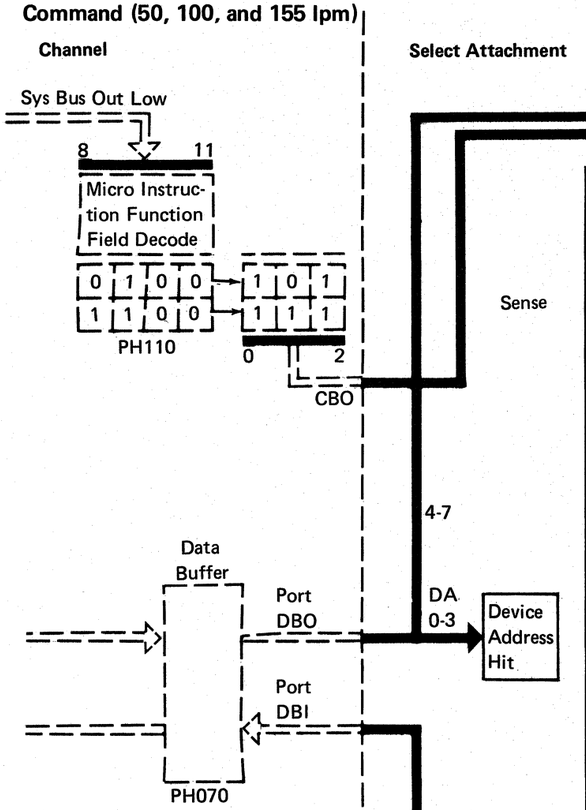
Control Load Command (Continued)



Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
1011(B)	0-7	Carriage Space Counter	Used to load the space counter with the data on port DBO.	DQ100	2
1100(C)	1 2 3 4 5	Diagnostic Carriage Control	Turns on the carriage go latch and the carriage busy latch (starting carriage motion). Turns off the carriage go latch. Turns on the activate clamp latch. Turns on the reset clamp active latch. Turns off the space time latch which ends a carriage operation.	DQ80 DQ80 DQ230 DQ230 DQ80	2
1101(D)	0-7	Elapsed Time Counter	Used to load the elapsed time counter with the data port DBO.	DQ300	2

Sense Command—Control Sense Command (50, 100, and 155 lpm)



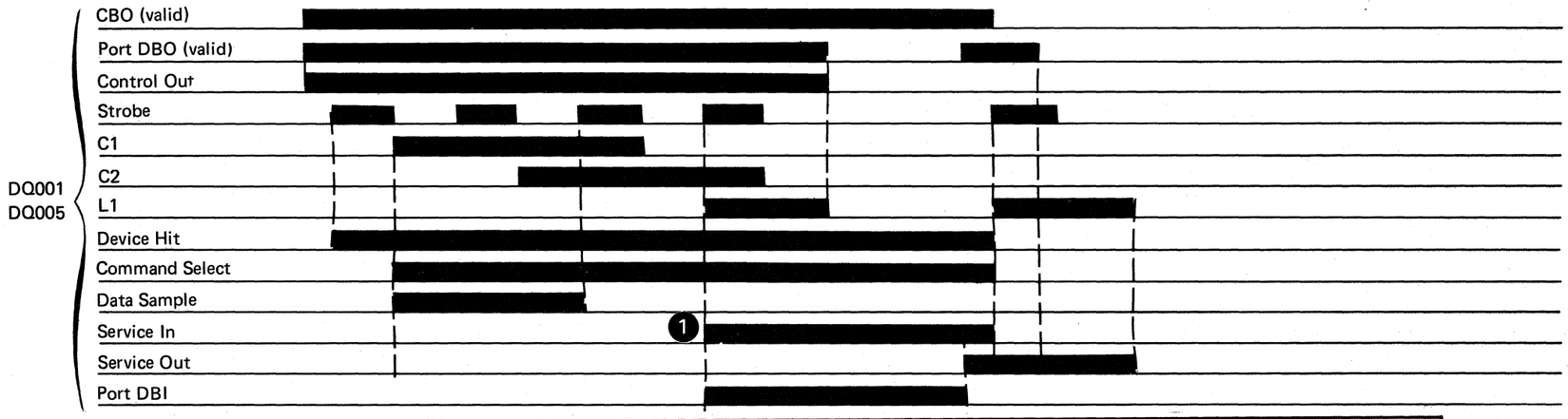
See μINSTR-30.

CCB 0 1 2	CCB 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 0 1	0 0 0 0 System Sense Byte 0	Forms Jam Check	Belt Speed Check	Carriage Sync Check	End of Forms	Throat Open	Coil Current Check	Belt Sync Check	Cover Open
	0 0 0 1 System Sense Byte 1	Coil 1 Parity Odd	Coil 2 Parity Odd	Coil 3 Parity Odd	Emitter Check	Buffer Data Check	Hammer Parity Check		
	0 1 1 0 Interrupt Condition				Print Busy Off	Carriage Busy Off			Elapsed Time Counter
	1 0 0 1** Print Buffer								
	1 0 1 1* Diagnostic Sense hex 00								
	1 1 0 0* Diagnostic Sense hex 55								
	1 1 0 1* Diagnostic Sense hex AA								
	1 1 1 0* Diagnostic Sense hex FE								
Control Sense 1 1 1	0 0 0 1 Diagnostic Clamp Status				Clamp On	Clamp Off			
	0 0 1 0* Diagnostic Inputs		Carriage Advance Pulses	CE Latch	Home	Belt Motion		Print Subscan Emitter	
	0 0 1 1** Belt Position								
	0 1 0 0* Diagnostic Wrap	Belt Go	Carriage Go	Printer Reset	Hammer Power On	Hammer Select Latch Feedback			
	0 1 0 1* Diagnostic Wrap	Paper Clamp	Hammer Select Strobe	Hammer Matrix Reset	Subscan 5	Subscan 4	Subscan 3	Subscan 2	Subscan 1
	0 1 1 0* Diagnostic Wrap	Stop Ribbon	Prepare Print Control	Adapter Reset			Coil Current Check		
	0 1 1 1* Diagnostic Sense Byte	1 ms Osc Off	131 ms Osc	System Reset Off	Power Fault	Hammer Duty Cycle Limit Off	Impression Singleshot		

*Diagnostic usage only.

**Not permitted when busy.

Sense Command—Control Sense Command (50, 100, and 155 lpm)—Continued



Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
0000(0)	0 1 2 3 4 5 6 7	System Sense Byte 0 (senses the condition of checks and interlocks).	Forms jam check. Belt speed check. Carriage sync check. End of forms (EOF). Throat closed. Coil (current) check. Belt sync check. Cover closed.	DQ210 DQ220 DQ080 DQ210 ZZ320 DQ090 DQ190 DQ220	1
0001(1)	0 1 2 3 4 5	System Sense Byte 1	Senses the condition of the coil 1 line. Senses the condition of the coil 2 line. Senses the condition of the coil 3 line. Senses the condition of the emitter check latch. Senses the condition of the buffer data check latch. Senses the condition of the hammer parity check latch.	DQ090 DQ090 DQ090 DQ260 DQ170 DQ100	1
0110(6)	3 4 5	Interrupt Condition	Sets port DBI bit 3 when the print busy latch is off. Sets port DBI bit 4 when the carriage busy latch is off. Sets port DBI bit 5 when the 'elapsed time counter is zero' line is active.	DQ110 DQ080 DQ300	1
1001(9)	0-7	Print Buffer	Gates the output of the print buffer to the channel on port DBI.	DQ180	1
1011(B)	0-7	Diagnostic Sense hex 00	Gates hex 00 to the channel on port DBI to check for no bits on.	DQ050, DQ060	1
1100(C)	0-7	Diagnostic Sense hex 55	Gates hex 55 to the channel on port DBI to check for alternate bits on.	DQ050, DQ060	1
1101(D)	0-7	Diagnostic Sense hex AA	Gates hex AA to the channel on port DBI to check opposite bits from 55.	DQ050, DQ060	1
1110(E)	0-7	Diagnostic Sense hex FE	Gates hex FE to the channel on port DBI to check for parity bit on.	DQ050, DQ060	1

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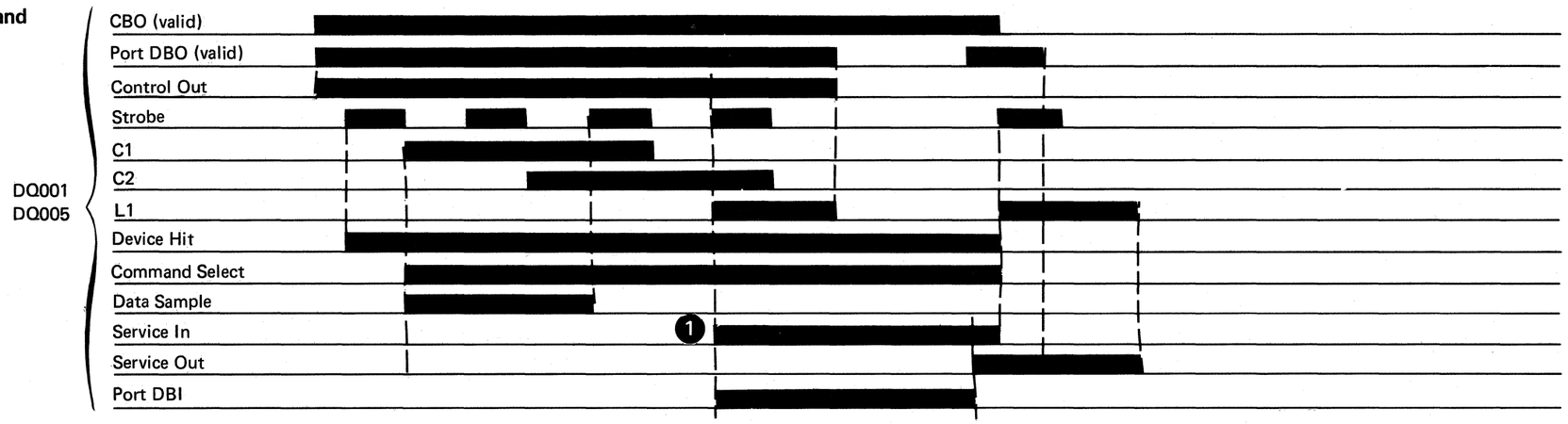
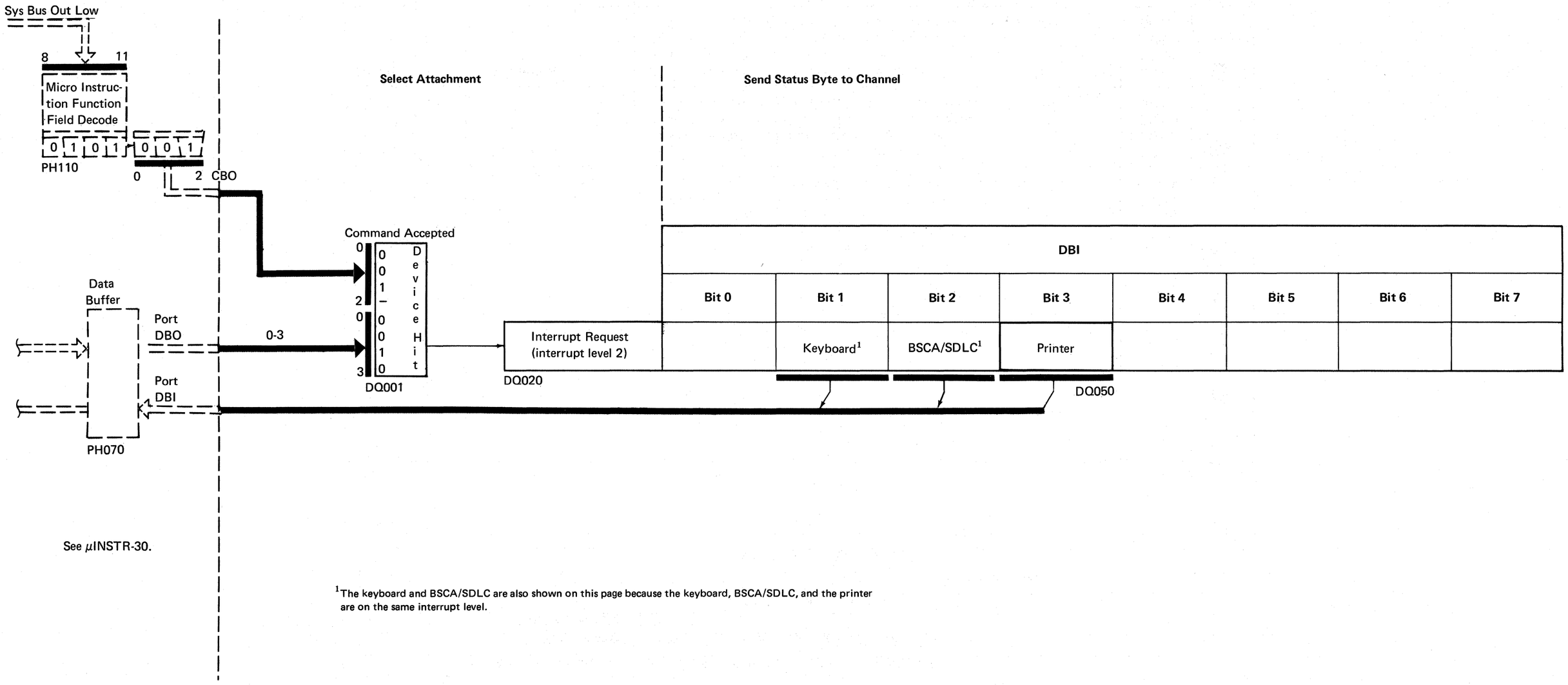


Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
0001(1)	3 4	Diagnostic Clamp Status	Turns on port DBI bit 3 if the clamp on latch is on. Turns on port DBI bit 4 if the clamp off latch is on.	DQ240 DQ240	1
0010(2)	1 2 3 4 6	Diagnostic Inputs	Turns on port DBI bit 1 when the carriage advance line is active. Turns on port DBI bit 2 if the CE latch is on. Turns on port DBI bit 3 when the home line is active. Turns on port DBI bit 4 when the belt motion line is active. Turns on port DBI bit 6 when the print subscan line is active.	ZZ580 DQ250 DQ210 ZZ580 DQ200	1
0011(3)	0-7	Belt Position	Sends value of the belt position counter through the scan key to the channel on port DBI.	DQ200	1
0100(4)	0 1 2 3 4-7	Diagnostic Wrap	Turns on port DBI bit 0 when the belt go latch is on. Turns on port DBI bit 1 when the carriage go latch is on. Turns on port DBI bit 2 if the printer reset latch is on. Turns on port DBI bit 3 when the hammer fault line is active. Sends the Y hammer select line values to the channel on port data in.	DQ220 DQ080 DQ090 DQ090 DQ290	1
0101(5)	0 1 2 3-7	Diagnostic Wrap	Turns on port DBI bit 0 when the clamp latch is on. Turns on port DBI bit 1 when the hammer select strobe line is active. Turns on port DBI bit 2 when the hammer matrix reset line is active. Turns on corresponding port DBI bits when the subscan lines 5-1 are active.	DQ240 DQ140 DQ210 DQ200	1
0110(6)	0 1 2 5	Diagnostic Wrap	Turns on port DBI bit 0 when the stop ribbon line is active. Turns on port DBI bit 1 if the prepare print control latch is on. Turns on port DBI bit 2 if the adapter reset latch is on. Turns on port DBI bit 5 if the coil (current) check counter output is active.	DQ220 DQ110 DQ090 DQ090	1
0111(7)	0 1 2 3 4 5	Diagnostic Sense Byte	Turns on port DBI bit 0 when the 1 ms oscillator output is active. Turns on port DBI bit 1 when the 131 ms oscillator output is active. Turns on port DBI bit 2 when the system reset line is active. Turns on port DBI bit 3 when the power fault line is active. Turns on port DBI bit 4 when the hammer duty cycle limit line is active. Turns on port DBI bit 5 when the impression singleshot is active.	PJ070 PJ070 PN060 DQ050 DT010 ZZ580	1

Sense Interrupt Level Status Command



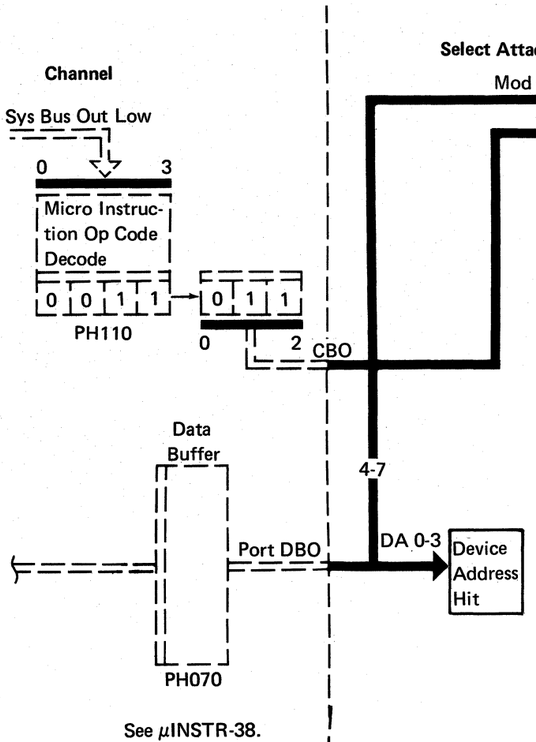
See μINSTR-30.

[1]The keyboard and BSCA/SDLC are also shown on this page because the keyboard, BSCA/SDLC, and the printer are on the same interrupt level.

Sense Interrupt Level Status Command (Continued)

Modifier Port DBO	Port DBI Interrupt Bit	Command	Action Taken	FEALD Page	Timing
0010(2)	3	Sense Interrupt Level	If an interrupt request is pending, port data in bit 3 (interrupt request) is sent to CPU.	DQ050	1

Jump I/O Command

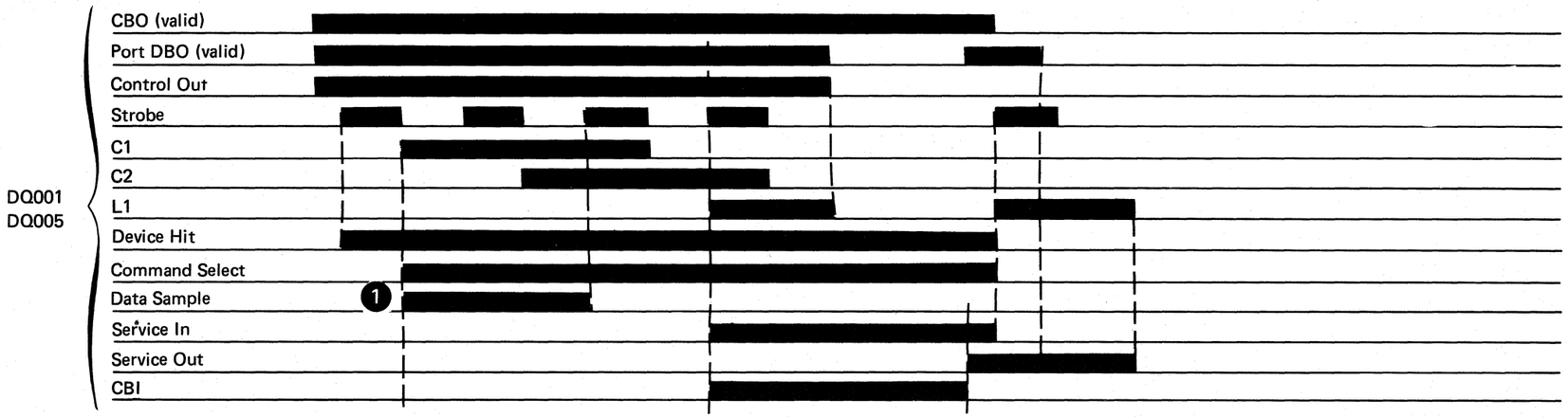


CCB 0 1 2	CCB 3	4	5	6	Condition Tested
0 1 1	0	0	0	0	Adapter Check
	0	0	0	1	Not Ready
	0	0	1	0	Carriage Busy
	0	0	1	1	Print Busy
	0	1	0	0	Interrupt Enabled
	0	1	0	1	Diagnostic True[1]
	0	1	1	0	Diagnostic False[1]
	0	1	1	1	Reserved
	1	0	0	0	Elapsed Time Counter Busy
	1	0	0	1	Motor Not Up To Speed
	1	0	1	0	Even Scans Selected
	1	0	1	1	Subscan Reset On
	1	1	0	0	Reserved
	1	1	0	1	Reserved
	1	1	1	0	Reserved
	1	1	1	1	Reserved

Forms jam
Belt speed check
Carriage sync check
Coil current check
Belt sync check
Emitter check
Buffer data check
Hammer parity check

End of forms
Throat open
Cover open

[1] Diagnostic usage only.



Modifier Port DBO 4, 5, 6, 7 (Hex)	Command	Action Taken	FEALD Page	Timing
0000(0)	Adapter Check	Turns on CBI bit 4 if any of the indicated check conditions are active.	DQ070	1
0001(1)	Not Ready	Turns on CBI bit 4 if any of the indicated interlock conditions are active.	DQ070	1
0010(2)	Carriage Busy	Allows a branch (CBI bit 4 on) if the carriage busy latch is on.	DQ080	1
0011(3)	Print Busy	Allows a branch (CBI bit 4 on) if the print busy line is active.	DQ110	1
0100(4)	Interrupt Enabled	Branches if one or more of the following latches are on: — Interrupt print op end. — Interrupt carriage op end. — Interrupt elapsed 0.	DQ270	1
0101(5)	Diagnostic True	Turns on CBI bit 4 to check that the bit actually turns on when expected.	DQ070	1
0110(6)	Diagnostic False	Turns on no latches to be sure that the CBI bit 4 does not turn on except when tested conditions are met.	DQ070	1
1000(8)	Elapsed Time Counter Busy	Turns on CBI bit 4 when the elapsed time counter 0 line is inactive.	DQ300	1
1001(9)	Motor Not Up To Speed	Branches when the motor up-to-speed line is inactive.	DQ260	1
1010(A)	Even Scans Selected	Branches when the odd latch (odd scans) is on.	DQ110	1
1011(B)	Subscan Reset On	Branches if the subscan reset latch is on.	DQ200	1

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Paper Clamps DQ240

There are two clamps in the printer. The upper paper clamp, although it clamps the paper, is used for noise suppression only. When the clamp solenoid is energized, it closes the air gap the paper passes through. This reduces the noise level at the back of the printer by dampening the paper noise.

The second paper clamp (lower) is just below the print line. The purpose of this clamp is to prevent horizontal skewing of the paper. The type belt is continuously turning and has a tendency to pull the paper along with it. Since there are no feed rolls in the lower portion of the printer, the paper clamp is necessary to hold the paper in position.

1 For diagnostic purposes, the activate clamp command A is issued to turn on the paper clamps. This command sets the 'activate clamp' latch (DQ240) which turns on the paper clamp solenoids. The 'activate clamp' latch also resets the 'clamp off' latch and gates the 'clamp on' latch to be set by the paper clamp timer. The 'clamp on' latch is set after the paper clamp timer has counted 15 μs.

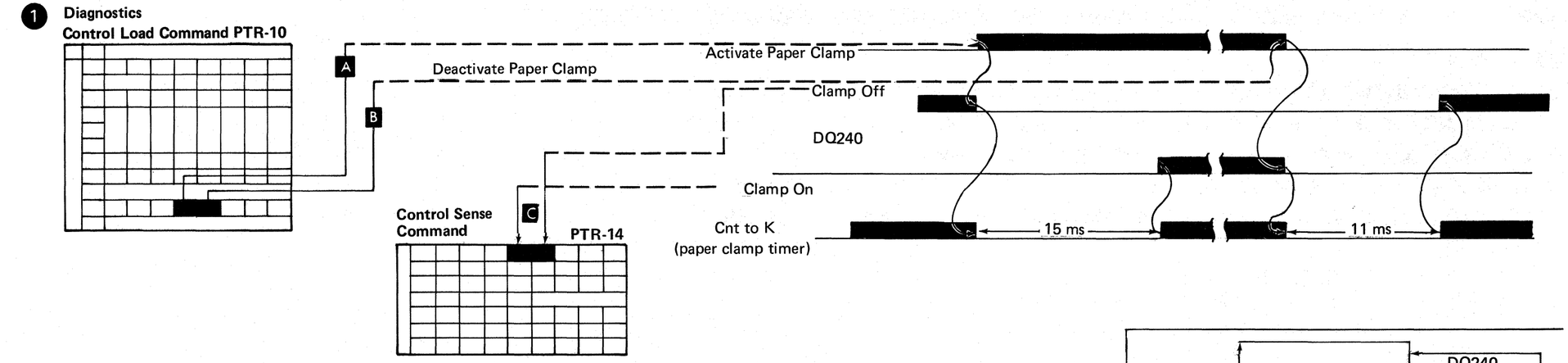
A similar operation is used to turn the clamps off. A deactivate clamp command B resets the 'activate clamp' latch. This in turn resets the 'clamp on' latch and gates the 'clamp off' latch to be set by the paper clamp timer. The 'clamp off' latch is set after the paper clamp timer has counted 11 μs.

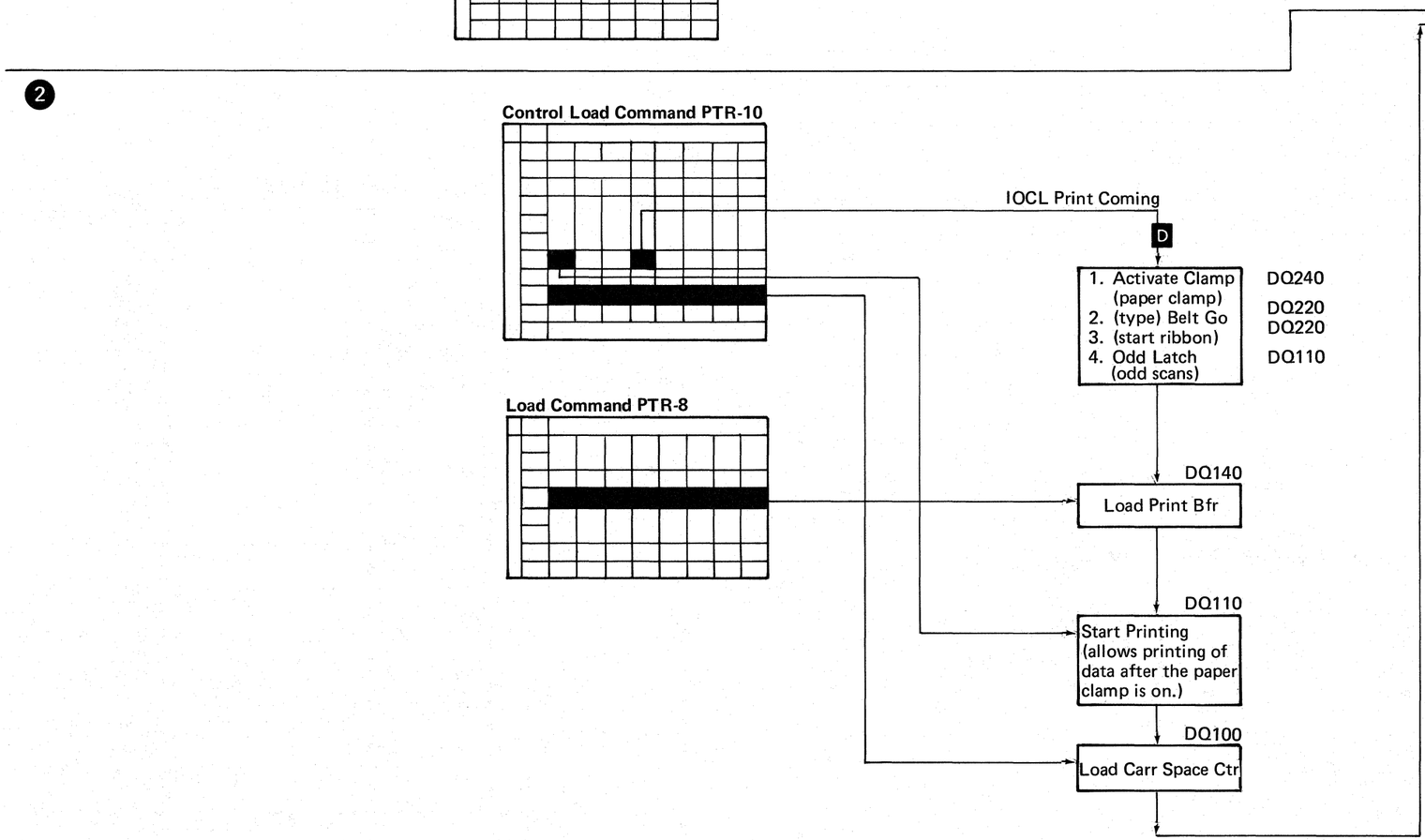
The 'clamp on' and 'clamp off' latches signal that enough time has elapsed to complete their respective operations. There is no check to see if the clamp solenoids are actually energized or not.

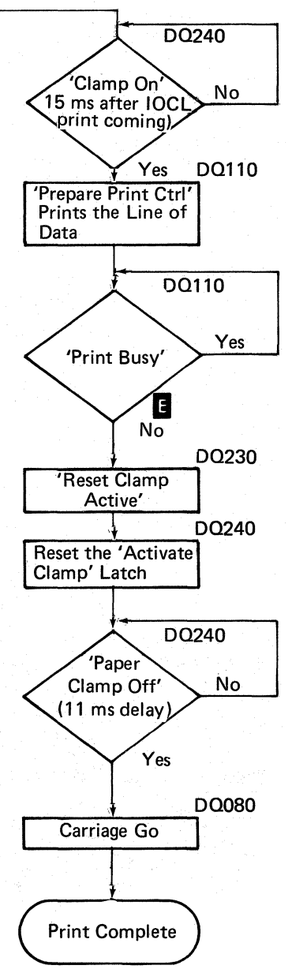
The 'clamp on' and 'clamp off' latches can be sensed C .

2 During a normal print operation, IOCL print coming active D activates the paper clamps and 'print busy' going inactive E turns off the paper clamp.

The above timing chart applies to both diagnostic and normal clamp control.







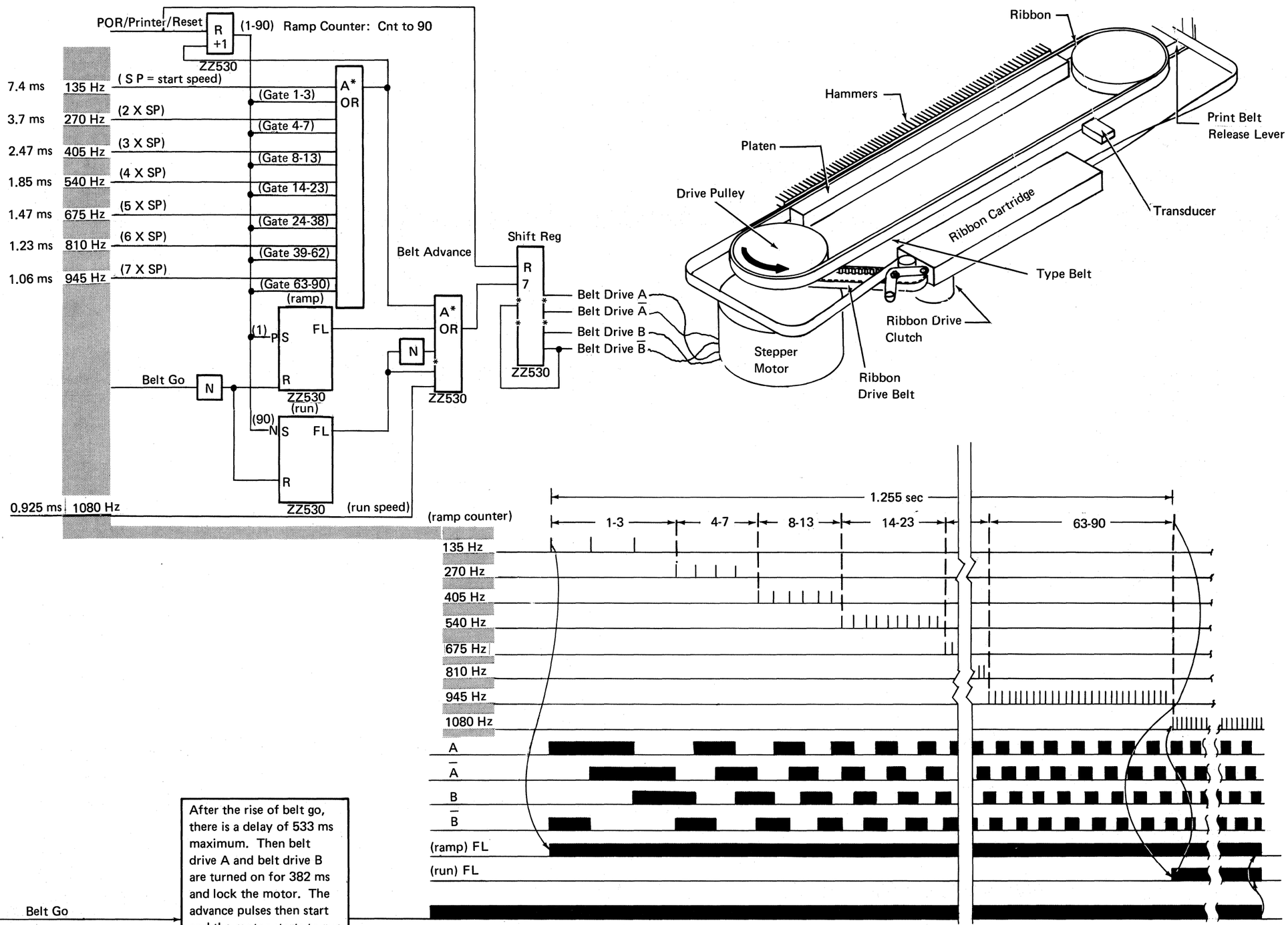
Type Belt Start and Run (50, 100, and 155 lpm)

The type belt is directly driven by a stepper motor mounted under the left pulley. The right pulley has a release lever mounted on it to remove tension from the type belt. When the release lever is operated, the type belt can be removed.

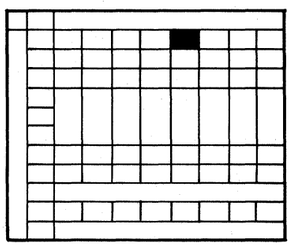
After POR, the count to 90 (ramp counter) runs continuously. When belt go is activated, there is a delay of 533 ms. Then belt drive A and belt drive B are turned on for 382 ms which locks the motor. After the 382 ms motor locks, the first count of 1 turns on the ramp latch which allows the belt advance pulse to shift the shift register. The output of the shift register causes the type belt stepper motor to start accelerating.

The first three drive pulses are 135 Hz, the next four at 270 Hz, five at 405 Hz, etc. This ramping sequence continues until a count of 90 is reached. At the fall of count 90, the run latch is set. The run latch blocks the ramp drive pulses and allows the shift register to be driven by 1080 Hz (run frequency). The type belt stepper motor is now up to full operating speed and remains at this speed until belt go is deactivated.

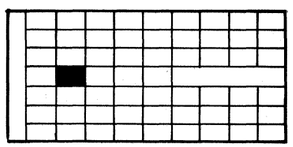
Note: Dual ramping card values are 70 percent of the values shown, until '—Belt Motion' is active.



Control Load Command PTR-10



Control Sense Command PTR-14



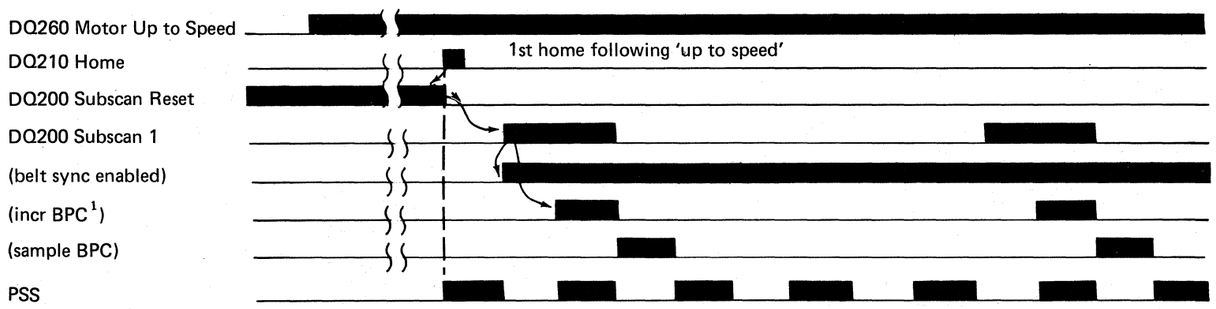
Type Belt Sync Timing

After the type belt has reached an up-to-speed condition, the sensing of the timing marks on the type belt is started. The first home pulse after up-to-speed turns off subscan reset and allows the BPC (belt position counter) and the subscan counter to start stepping. This synchronizes the stepping of the BPC and the subscan counter. When subscan 1 comes up, the belt sync enabled latch is turned on. The next PSS pulse after subscan 1 increments the BPC.

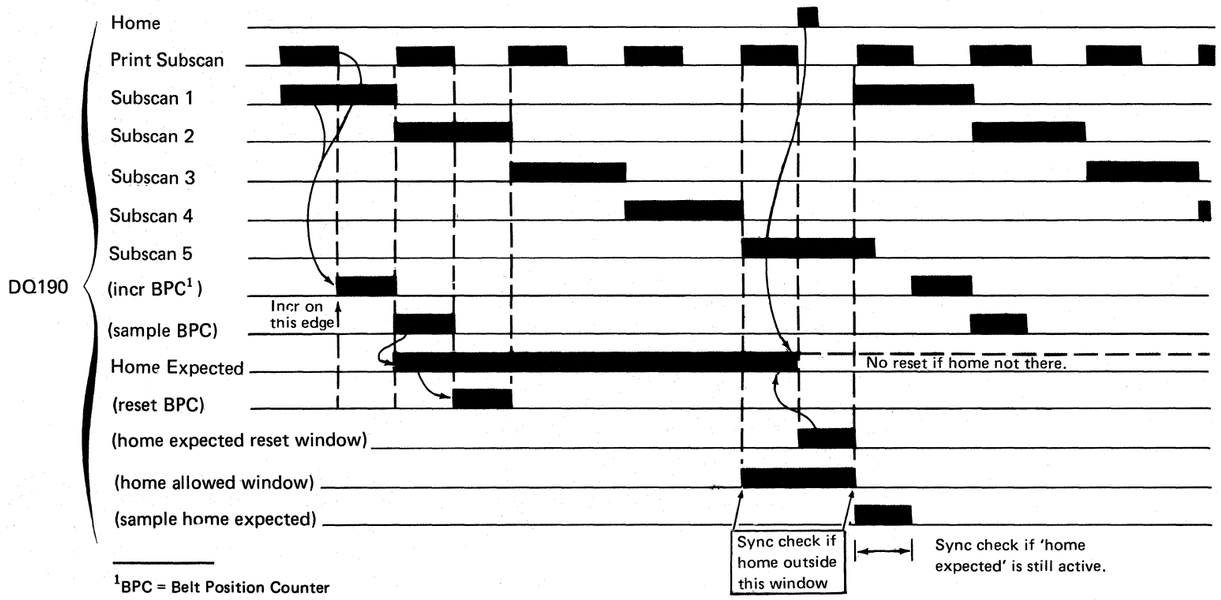
The BPC and the subscan counter are synchronized with each other by the home pulse. Once the home pulse has been received, the BPC and the subscan counter are allowed to continue stepping. Synchronism continues to be verified by the home pulse. If a home pulse occurs when not expected or fails to occur when expected, the belt sync check is set.

The print buffer contains PFN (print fire numbers) that indicate the print scan on which a position is printed. The BPC contains the number of the current print scan and the subscan counter selects the hammers to be optioned within each print scan. In this manner, the characters to be printed are synchronized with the characters on the type belt.

Initiating the Belt Sync Timing Sequence

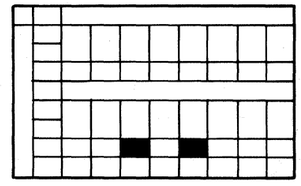


Type Belt Sync Timing

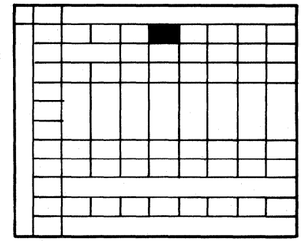


[1]BPC = Belt Position Counter

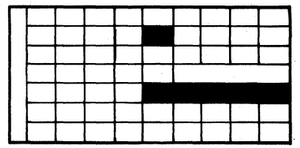
Load Command PTR-8



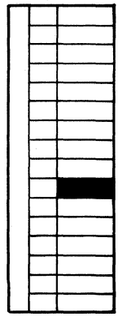
Control Load Command PTR-10



Control Sense Command PTR-14



Jump I/O Command PTR-20



Ribbon Drive/Type Belt Transducer (50, 100, and 155 lpm)

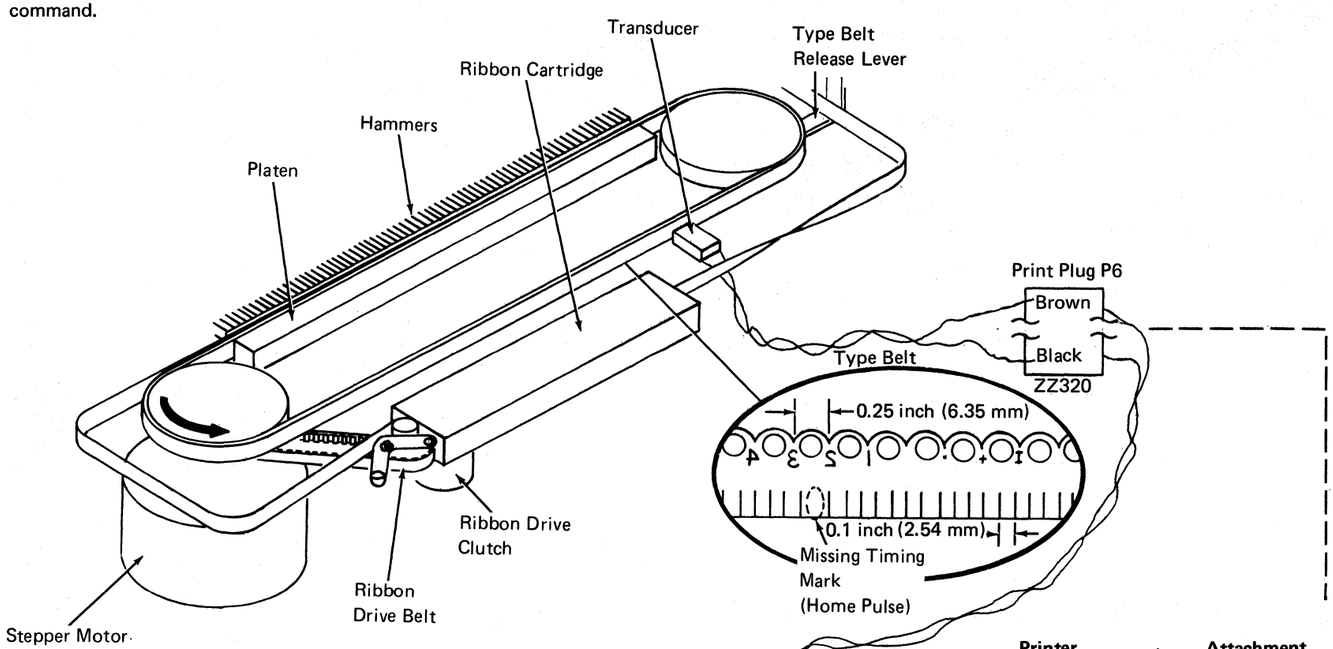
Ribbon Drive

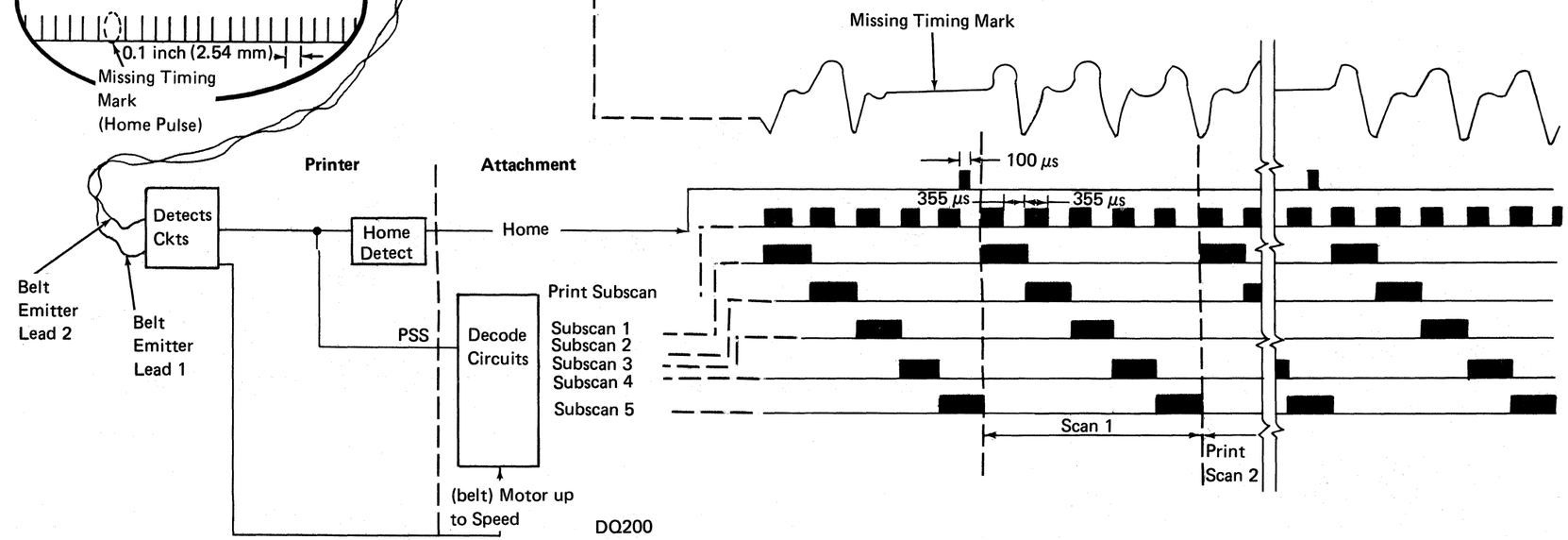
The ribbon is driven by a belt mounted on the type belt drive pulley. The drive mechanism also includes a solenoid-driven clutch to disengage the drive from the ribbon when no printing is taking place. The disengaging of the clutch prevents smudging of the paper while the printer is idle. This is under control of the printer control card, and happens five seconds after the last print command.

The ribbon is a continuous 1/2 inch wide fabric ribbon contained in a cartridge mounted on the front of the printer. The ribbon is fed into the left side of this cartridge and pulled out the right side (as viewed from the front of the machine).

Type Belt Transducer

The type belt transducer detects the raised timing marks on the type belt. These marks are converted to emitter pulses in the transducer and sent to the control card. The control card uses these pulses to generate the home pulse, subscan pulses, and the belt up-to-speed signal. The home pulse and subscan pulses are used to synchronize the mechanical and electrical portions of the print operation. The belt up-to-speed signal is sent to the attachment to indicate that the type belt is up to operating speed.



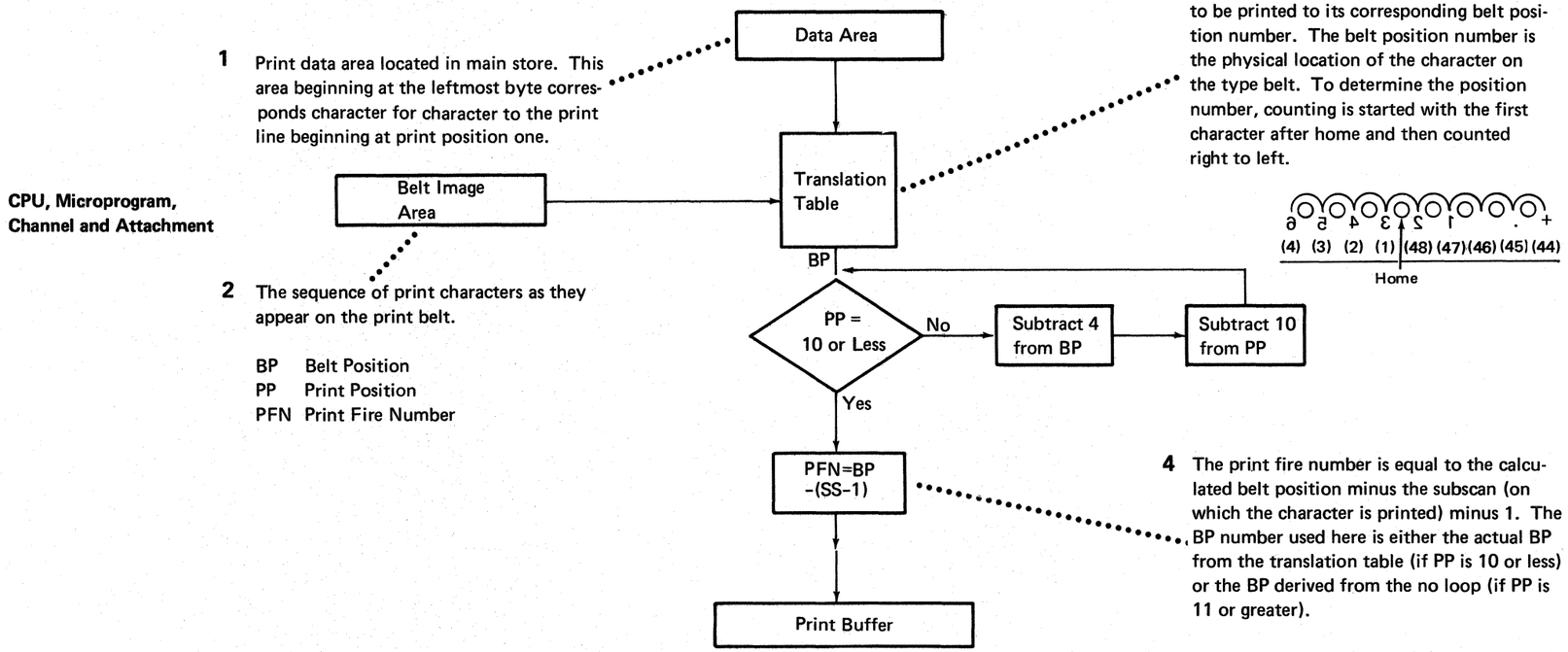


Print Buffer Load DQ180 (50, 100, and 155 lpm)

The print buffer is loaded by a print buffer load command, 1 byte per command. The data is in the form of PFN (print fire numbers) rather than actual print image data. The flowchart at the right shows how the value of the PFN is determined.

Prior to loading the buffer the SBAR is reset to zero by a reset scan buffer address control load command. Issuing of the print buffer load command gates the DBO data to the print buffer. It also brings up the 'incr bfr adr' lines; which steps the SBAR, and 'write select' line which gates data into the print buffer when it is active. The print buffer load command ANDed with 'data sample' brings up 'ram clock strobe' which sets the data into the print buffer.

The SBAR is then incremented to the next print buffer position (as shown below). If that position is to be written, another print buffer load command must be issued to load it.

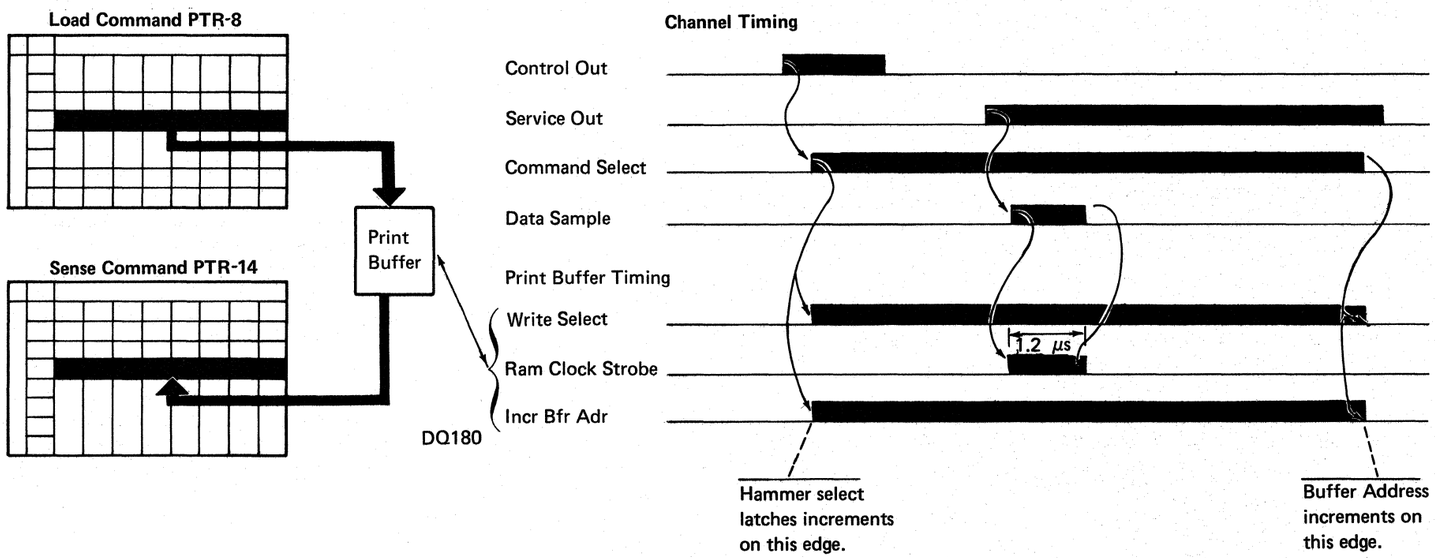


If the last digit of PP =

1 or 2	subscan = 1
3 or 4	2
5 or 6	3
7 or 8	4
9 or 0	5

5 The print buffer contains the sorted print fire numbers (PFN). They are sorted into the sequence in which they are addressed.

Print Buffer	PP
0	1
1	11
2	21
3	31
etc.	

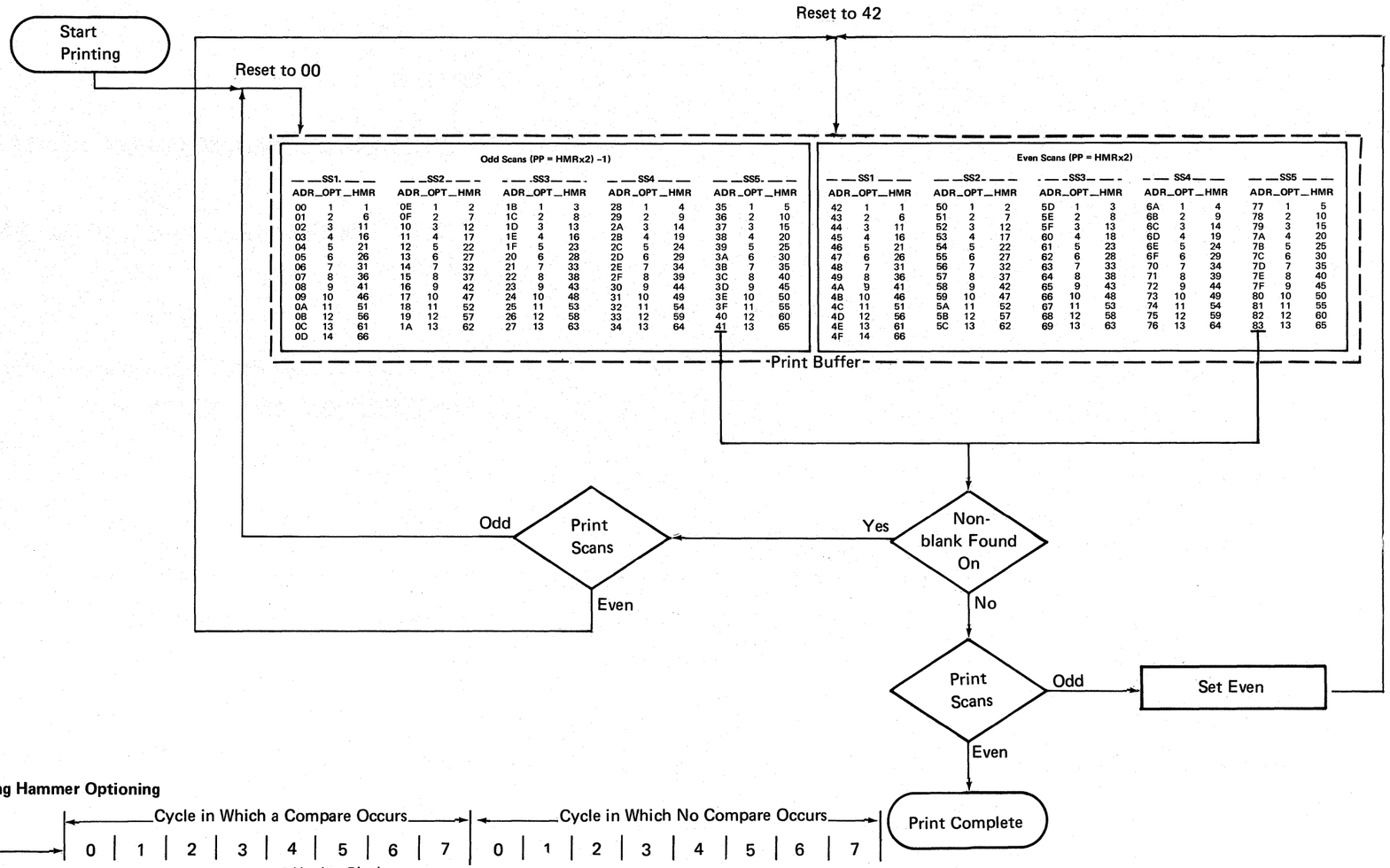


Print Buffer Read DQ180 (50, 100, and 155 lpm)

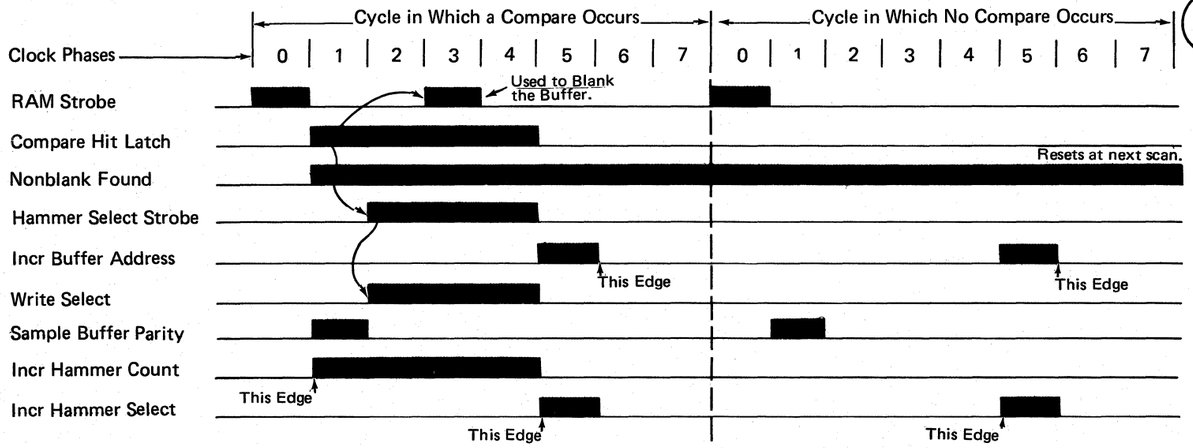
To start reading from the print buffer, a start printing command must be issued and write select must be inactive (indicating read select active). The 'ram clock strobe' line is used to read out the data.

The data is then compared with the value of the scan register and checked for equal or not equal. If not equal, SBAR is incremented to the next buffer position and the above sequence is repeated. If equal, 'hammer select strobe' and 'write select' are activated. 'Hammer select strobe' fires the hammer being addressed and 'write select' allows a hex FF to be written, blanking the buffer position being addressed. SBAR is then incremented to the next buffer position.

When the end of odd scans (hex 41) is reached, the output of the nonblank found latch is checked. If it was set by a valid buffer character, SBAR is reset to the starting address (hex 00) of the odd position of the buffer. If the nonblank found latch was not set (no valid characters in the buffer), SBAR is set to hex 42 to start addressing the even scans. The even portion is addressed in the same manner as the odd (shown at the right). When the end of the buffer is reached and the nonblank found latch is off, the end of superscan is set.

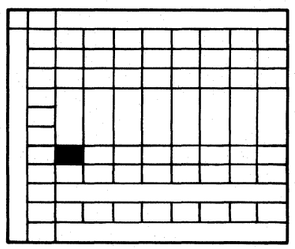


Typical Cycles During Hammer Optioning

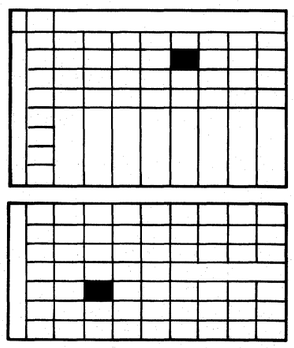


(Incr buffer address is the active line used.)

Control Load Command PTR-10



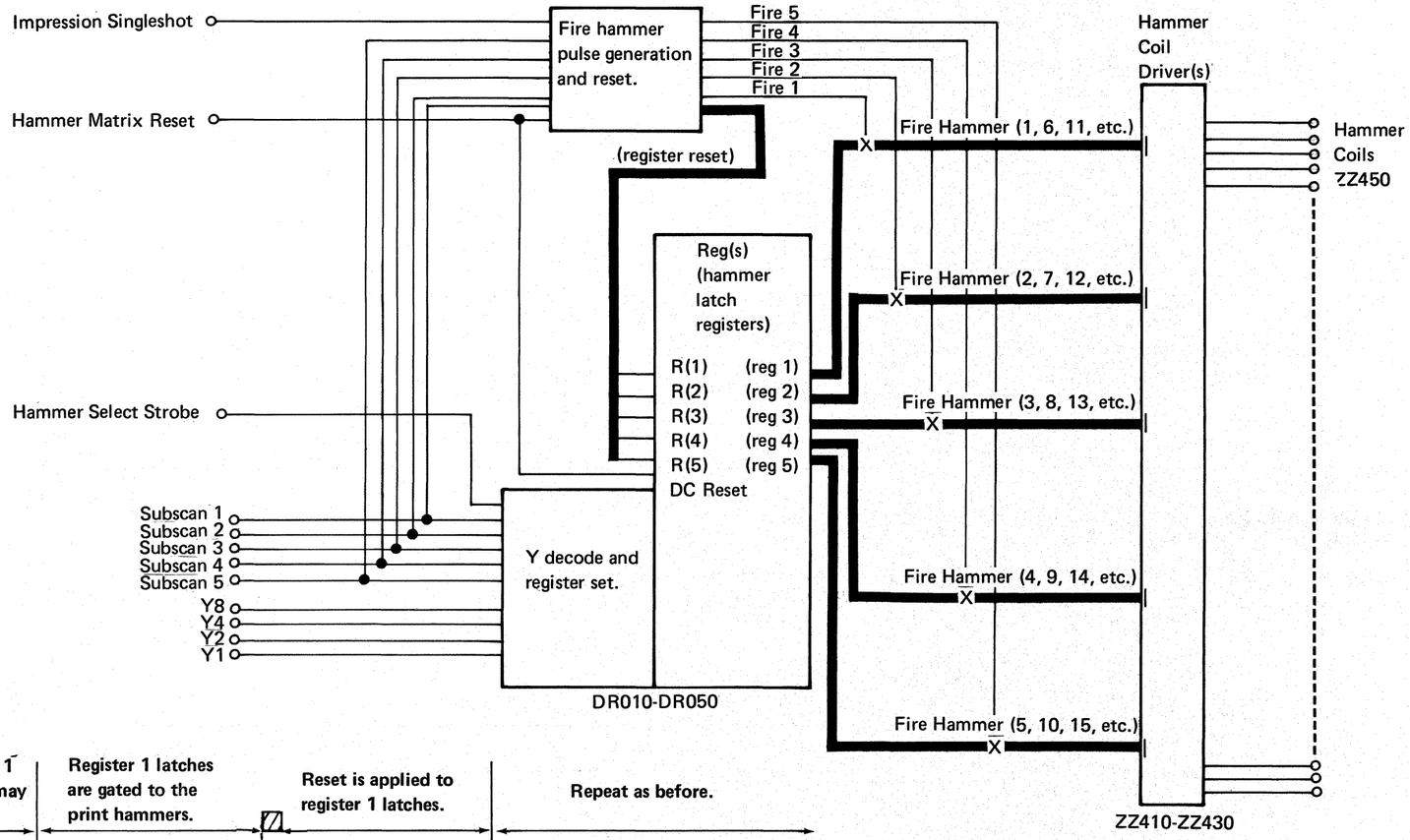
Sense Control Sense Command PTR-14



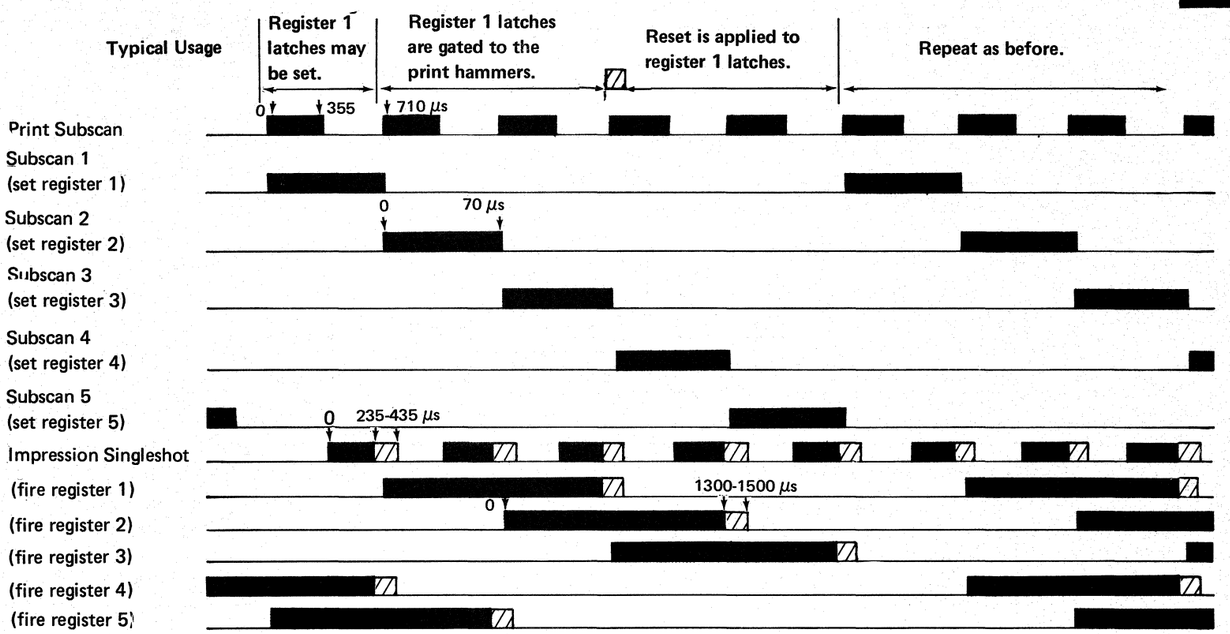
Hammer Selection and Firing (50, 100, and 155 lpm)

During subscan 1, the Y lines are stepped from 1 to 14 to address all the hammer latches in reg1. During subscan 2, the Y lines are stepped from 1 to 13 to address all the hammer latches in reg2. This sequence continues through subscan 5. If any optioned hammers are to be fired (scan/buffer equal) they are set into the hammer latches by the 'hammer select strobe' line.

Once a hammer has been set to fire, it is actually fired by the fire pulses. These pulses occur one subscan after the hammer latch registers have been set, that is, a hammer set on subscan 1 is fired on subscan 2. The fire pulses are set by the subscan pulse and reset after two impression singleshot pulses. If the impression singleshot does not become active, the fire pulse stays on until the coil current check is activated. The setting of the impression singleshot determines the duration of the fire pulse.



Hammer Fire Pulse Timing



Hammer Selection and Firing (50, 100, and 155 lpm) — Continued

Hammer Latch Select (50, 100, and 155 lpm)

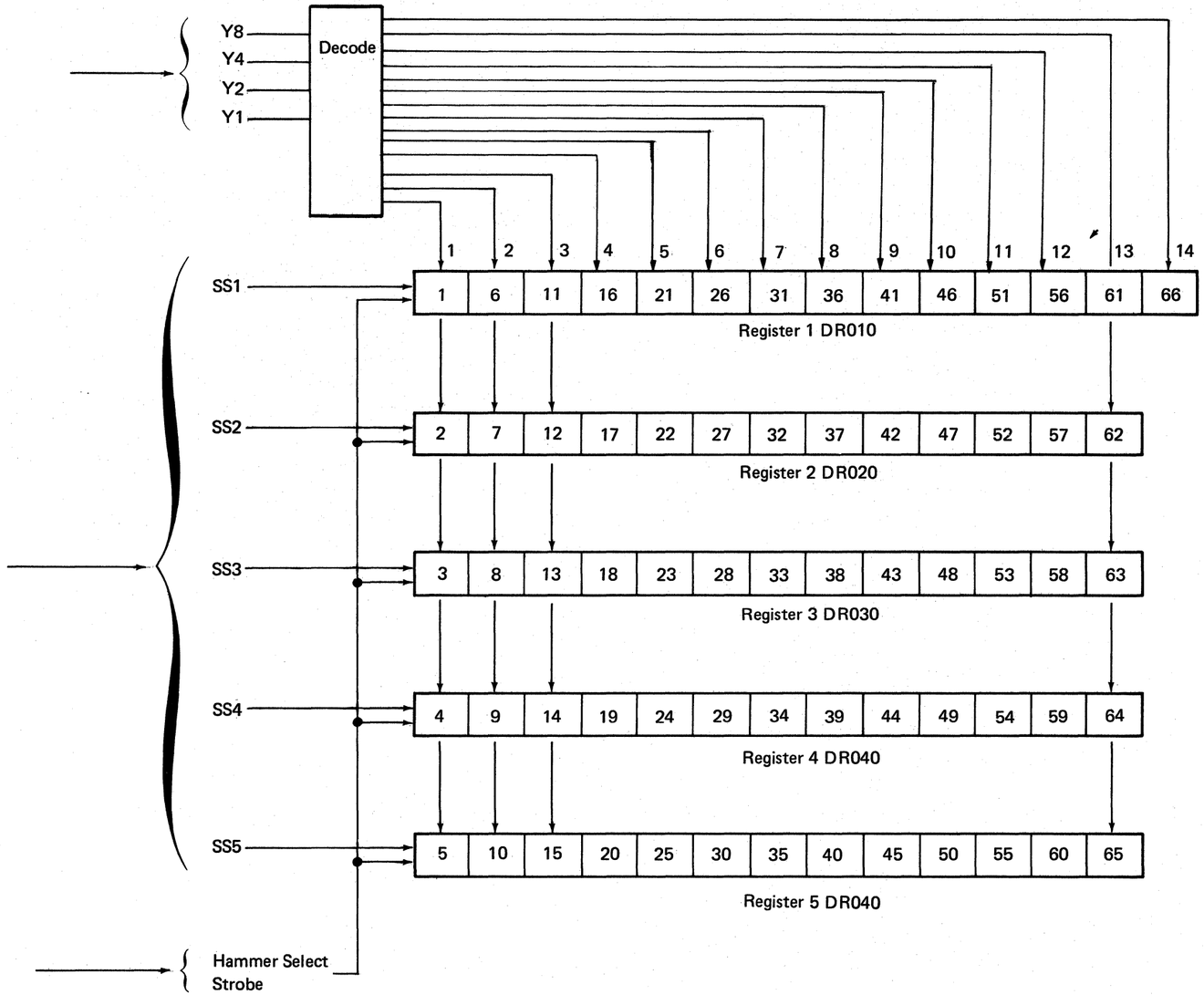
The individual hammer latch within each register is selected by decoding the value of Y lines (value 1 to 14 for register 1 and 1 to 13 for registers 2 to 5).

Register Select (50, 100, and 155 lpm)

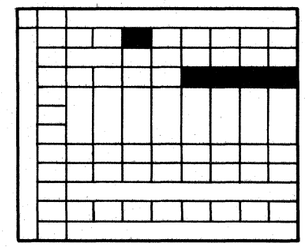
Each register is selected by its corresponding subscan line (subscan 1 to 5).

Hammer Select Strobe (50, 100, and 155 lpm)

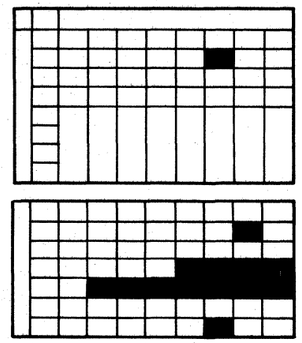
If the scan/buffer compare results is in equal condition, 'hammer select strobe' is activated and sets the particular hammer latch being selected.



Control Load Command PTR-8



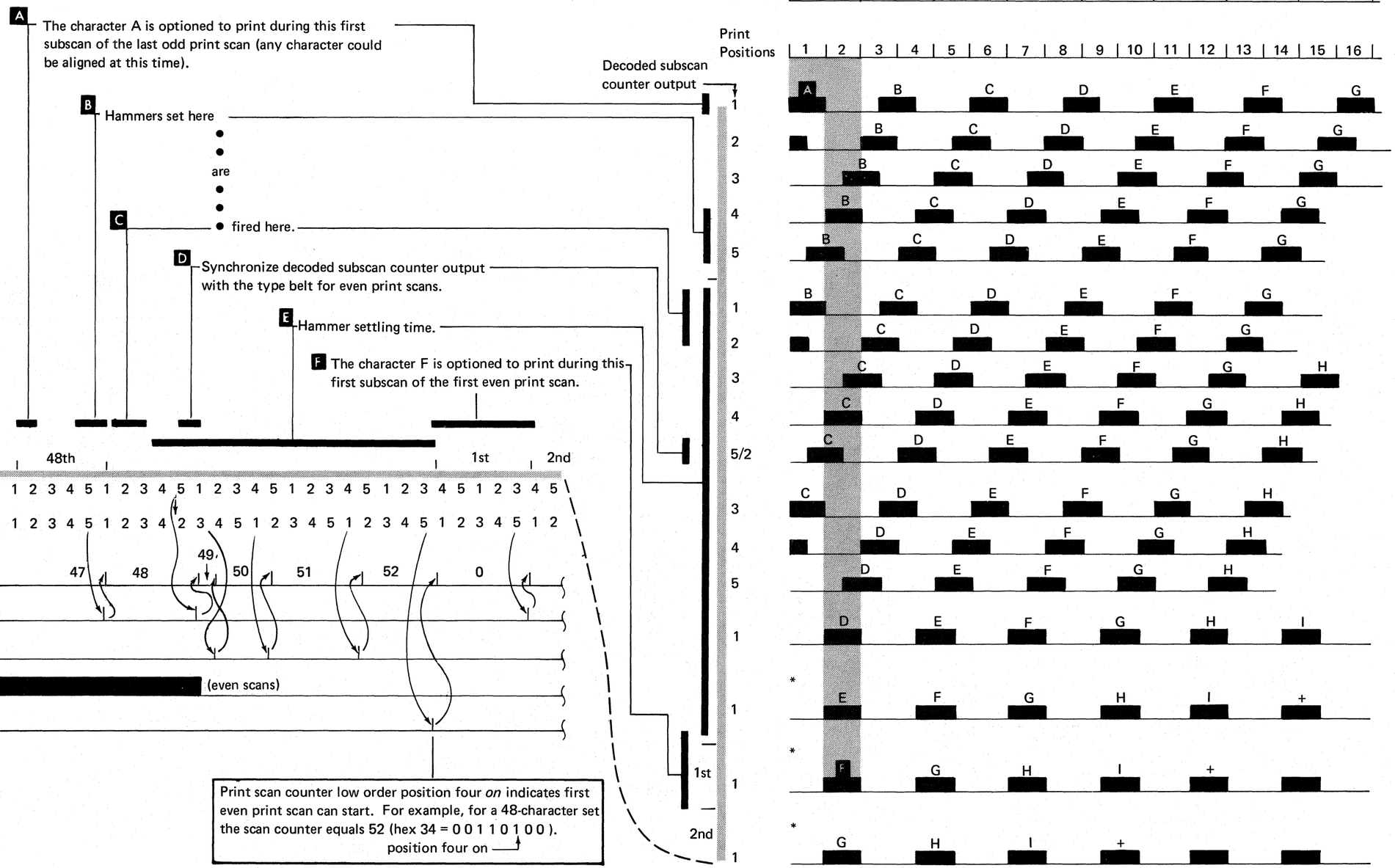
Sense — Control Sense Command PTR-14



Hammer Settling and Type Belt Synchronization (50, 100, and 155 lpm)

The four main objectives of this diagram are to show what takes place between the odd and even print scans (48-character set shown).

1. A and F show the relationship between the first character alignment for the last odd print scan, and the first character alignment for the first even print scan.
2. B and C show that hammers optioned in the last two subscans of print scan 48, are actually firing (if selected) during the first two subscans of the next print scan (beginning at hammer settling time).
3. D shows the changing of the subscan counter selected output (5 time decoded to 2 time, 1 to 3, 2 to 4, etc). Therefore when the subscan counter selected output is 1, the character F is aligned to print.
4. E Hammer settling time is the time which allows the hammers fired during the odd print scans to settle down (quit bouncing) in preparation for firing during the even print scans.

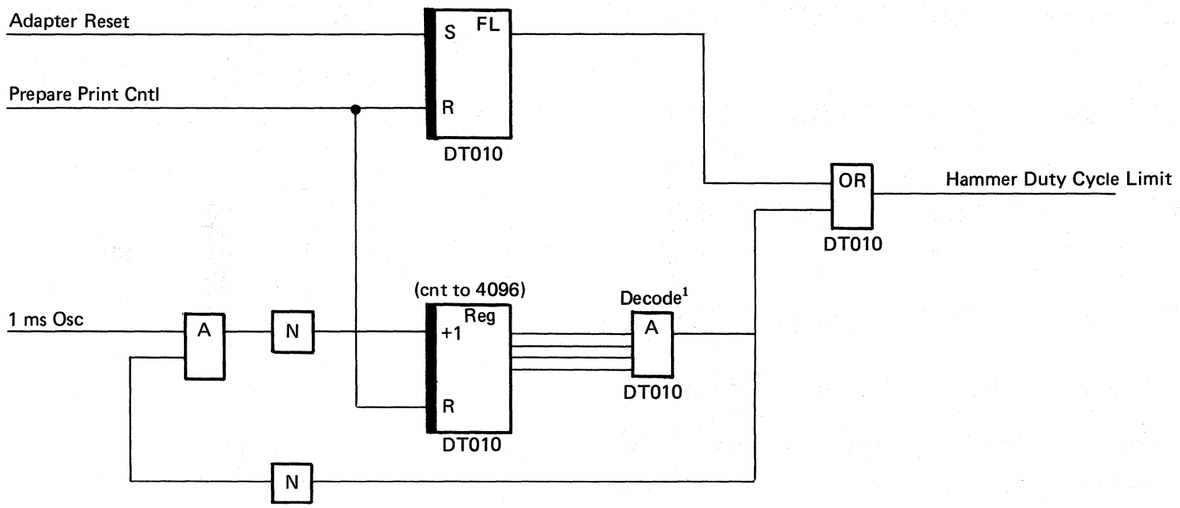


*Subscans 2-5 not shown.

Printer Speed Control

The speed of printing is controlled by the value of a 12 position binary counter (cnt to 4096). The value decoded from the counter determines how long 'hammer duty cycle limit' is active.

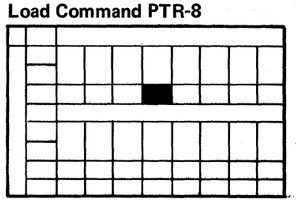
The 'hammer duty cycle limit' line holds up 'print busy' to the channel thus limiting the printing speed.



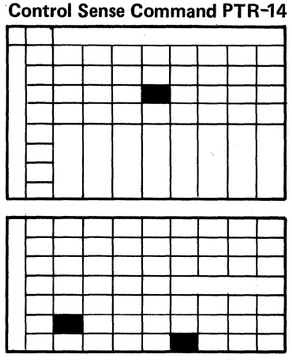
[1]The value decoded from the counter determines the speed of printing. The values used are:

1164 ms for 50 lpm
560 ms for 100 lpm
344 ms for 155 lpm
168 ms for 285 lpm

Load Command PTR-8



Sense —
Control Sense Command PTR-14



Carriage Operation (50, 100, and 155 lpm)

The printer uses a stepper motor driven pin feed carriage. The carriage uses a vertical spacing of 6 lines per inch.

The carriage advance pulses, generated from the 606 Hz oscillator drive the carriage shift register. The shift register provides the A and B drive lines for the carriage stepper motor. The start pulse brings up 'inhibit detent' which gates the carriage drive lines to the stepper motor.

The number of lines to be spaced must be loaded by a carriage space counter control load command and to initiate a carriage operation. The number of stepper motor steps is equal to 8N–2 where N is the number of lines to be spaced. The space counter is then decremented until the 'steps 2' line is activated (meaning two more stepper motor advances left). 'Steps 2' resets 'carriage go' which turns off the run latch and sets the stop latch. The stop latch gates two more carriage advance pulses to the stepper motor. The last carriage advance pulse (carriage feedback pulse) brings up the line 'steps 0' which resets the 'space time' latch, ending the carriage operation.

The keyboard functions that control the carriage are:

- Carriage restore
- New line (space one line)
- Reset line counter to 1 (tells the system the form is on line 1)

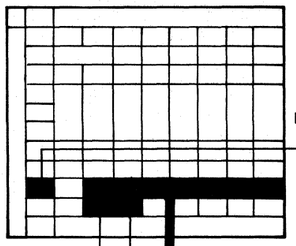
Carriage Detent

When the carriage is not spacing the 1080 Hz line (approximately 1 ms) gates the A, $\overline{A}$, B and $\overline{B}$ drive lines to the print carriage motor. Because the 1080 Hz line is oscillating, it gates the A, $\overline{A}$, B, and $\overline{B}$ drive lines half the time, which allows half current through the stepper motor. This provides the carriage electrical detent.

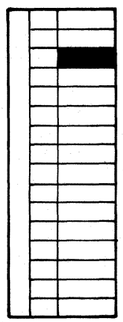
Note: Dual ramping card values are 70 percent of the values shown until '—Belt Motion' is active.

Loss of 24 Vdc or power on reset removes the detent.

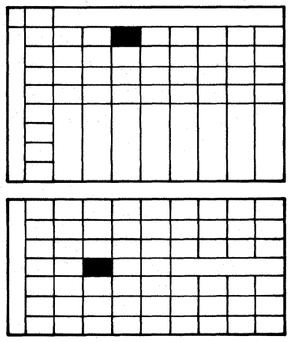
Control Load Command PTR-10



Jump I/O Command PTR-20



Sense —
Control Sense Command PTR-14



Attachment

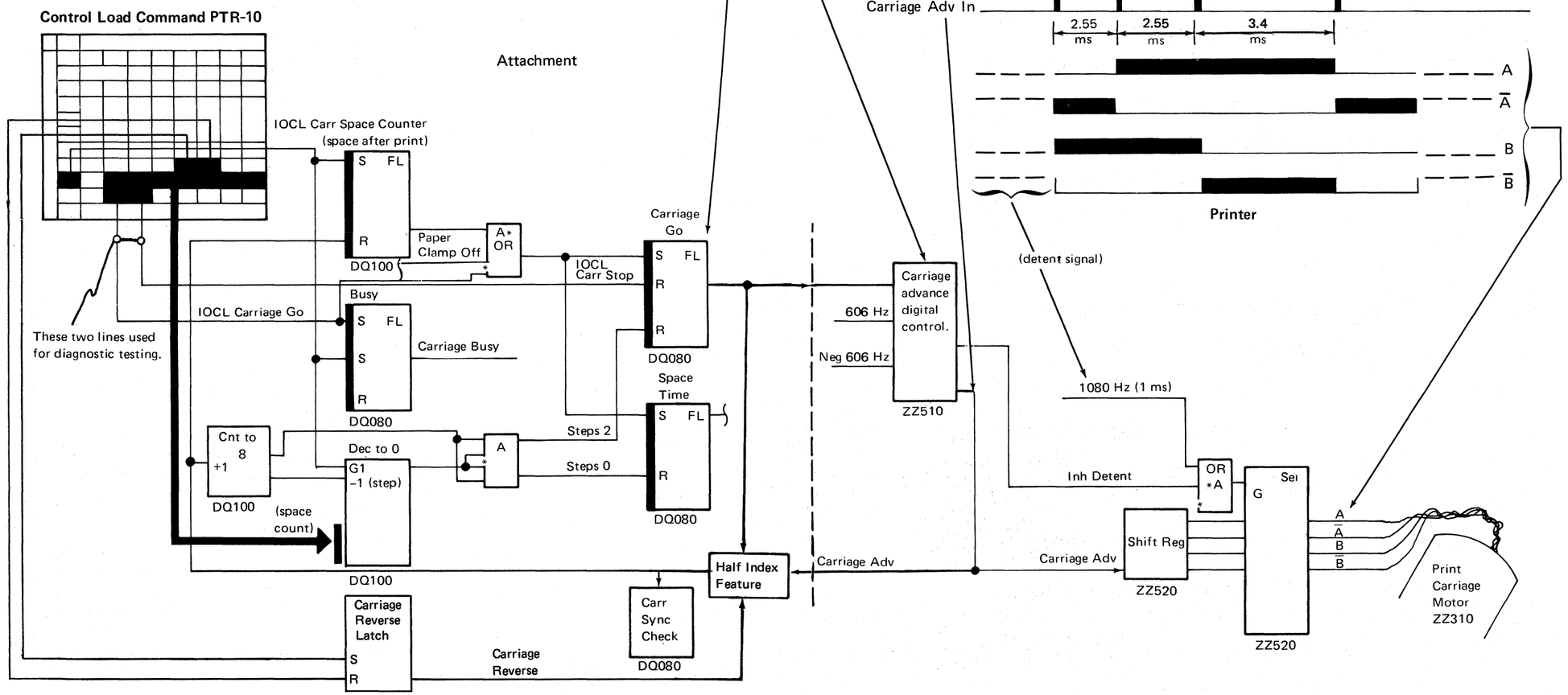
Half Line Space Operation (50, 100, and 155 lpm)

The half line space print feature permits indexing of the printer one half space above or below the normal print line. This spacing is used for super-scripting or subscripting a character on the print belt.

The half line space print feature supplies the printer attachment with eight carriage advance pulses when only four carriage advance pulses are sent by the printer to the carriage advance shift register. During the half line space operation, when the first carriage advance pulse is received by the half index card, five fast (64 μs) carriage advance pulses are generated from the 4 μs clock and sent to the printer attachment before the second carriage advance pulse is received from the printer. When the second pulse is received from the printer, it is passed unaltered to the printer attachment. This pulse becomes the sixth carriage advance pulse to the printer attachment and carriage go is dropped. The deceleration function begins and the third and fourth carriage advance pulses from the printer are received by the printer attachment. These are the seventh and eighth pulses in the carriage line position counter (count to eight). Because the printer attachment has received eight pulses in the carriage line position counter, the acceleration and deceleration timing of a full index is retained and forms jam and carriage sync checking are performed.

A half index is initiated by setting the carriage reverse bit (bit 4) in a control load command (IOCL) with a modifier of A. Half index mode is reset by bit 5 of the command and the half index feature card is reset by bit 5 of the command, dropping carriage go, or resetting the printer attachment.

Half index complete (for diagnostics only not shown) indicates that the five fast pulses to the printer attachment have been generated and the completion of the index operation is under control of the carriage advance digital control in the printer.



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Input/Output Lines (50, 100, and 155 lpm)

A = from attachment
P = from printer

POR/Printer Reset (A)

POR/printer reset line is initiated during the power up sequence to reset the printer circuits to their starting condition. It is also activated if a carriage sync check is detected.

Close (+24V) Contactor (A)

Close contactor must be activated to switch the +24V into the printer. This line is deactivated when a hammer parity check is sensed to protect the hammer coils.

Belt Go (A)

Belt go is activated to start the belt oscillator. The belt oscillator furnishes pulses to run the type belt drive circuits.

Belt Motion (P)

The belt motion signal is active when the type belt reaches operating speed. It becomes inactive when the belt speed decreases to approximately 10 per cent below the operating speed. The home pulse and the subscan pulses become active when the belt is up to speed.

PSS (Subscan) (P)

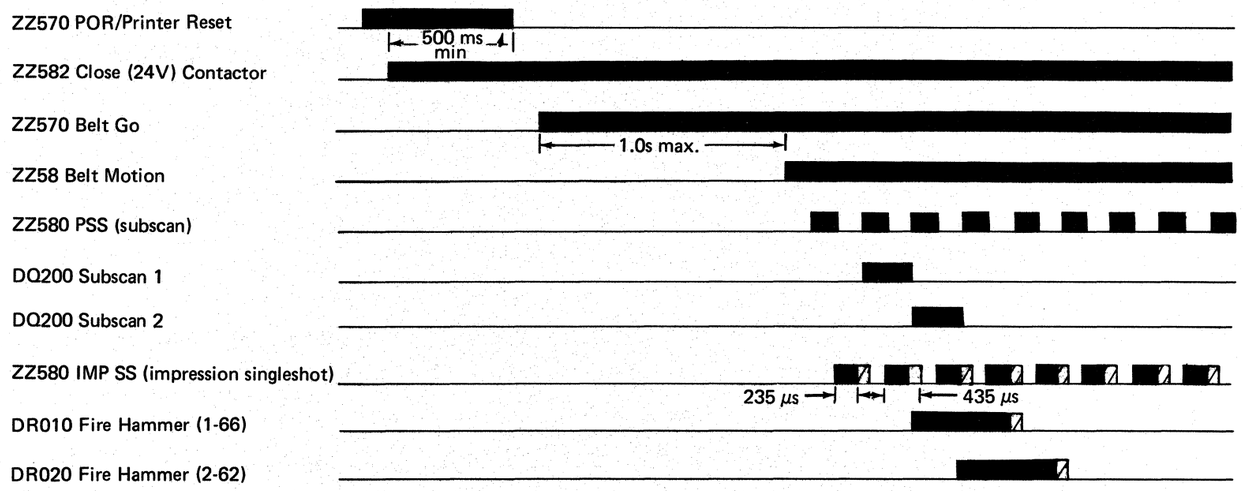
The PSS pulses are generated from the raised timing marks on the type belt. The subscan pulses synchronize the print controls between the attachment and the printer. When the home pulse is detected, a dummy pulse is generated because of the missing timing mark.

IMPSS (Impression Singleshot) (P)

IMPSS is added to the hammer fire pulse to control the time the hammers are fired for different forms thickness. This signal is activated when the subscan pulse goes inactive (halfway into a subscan) and remains active 235 μs to 435 μs depending on the setting of the forms thickness control.

Fire Hammer (A)

Fire hammer lines are activated to fire the corresponding print hammers (fire hammer 1 = print hammer 1, etc).



Activate Paper Clamps (A)

This signal energizes the upper and lower paper clamps. It is deactivated during a spacing operation and when the printer is idle.

Home Pulse (P)

On the type belt there is a double space between two of the timing marks. This space (missing timing mark) generates the home pulse that signals the start of the type set on the type belt. The home pulse is used to synchronize the type belt and the belt position counter.

Hammer Check 1-22 (also 23-44 and 45-66) (P)

The hammer check lines determine that in each group an odd number of hammers is on (when active). They are used as input for the hammer parity check and the coil current check.

Carriage Go (A)

This line activates the carriage advance digital control circuits. These circuits furnish pulses to run the carriage drive circuits.

Stop Ribbon (A)

The stop ribbon line is activated if the printer is idle for five seconds. When the signal is activated, the ribbon stops moving to prevent smudging the paper.

Carriage Advance (P)

The carriage go line activates the carriage advance digital control circuits. These circuits generate the carriage advance pulses. Each carriage advance pulse advances a shift register which advances the print carriage motor by one increment (eight increments per line). Therefore, eight carriage advance pulses decrement the space count once per line. When the space count goes to zero the carriage operation is complete, which resets carriage go. The carriage advance pulse is also used for carriage sync check detection.

Printer Thermal Switch (P)

This line signals that the temperature in the printer circuitry is too high. It indicates a thermal check in case of overheating. The switch opens at 145°F, ±5°F (63°C ± 3°C).

Cover Closed Switch (P)

The cover must be closed to make the printer ready.

Forms Sensed Switch (P)

This line indicates to the attachment whether or not there are forms in the printer.

Throat Closed Switch (P)

This line sends the condition of the casting throat interlock switch to the attachment. It must show a throat closed condition to make the printer ready.

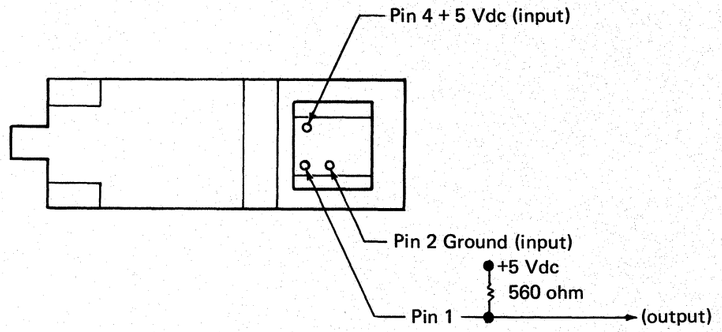
Switch Assemblies

CAUTION
These are electronic switches and do not have conventional switch contacts. A high current source (test light or ohm meter) will permanently damage the switch.

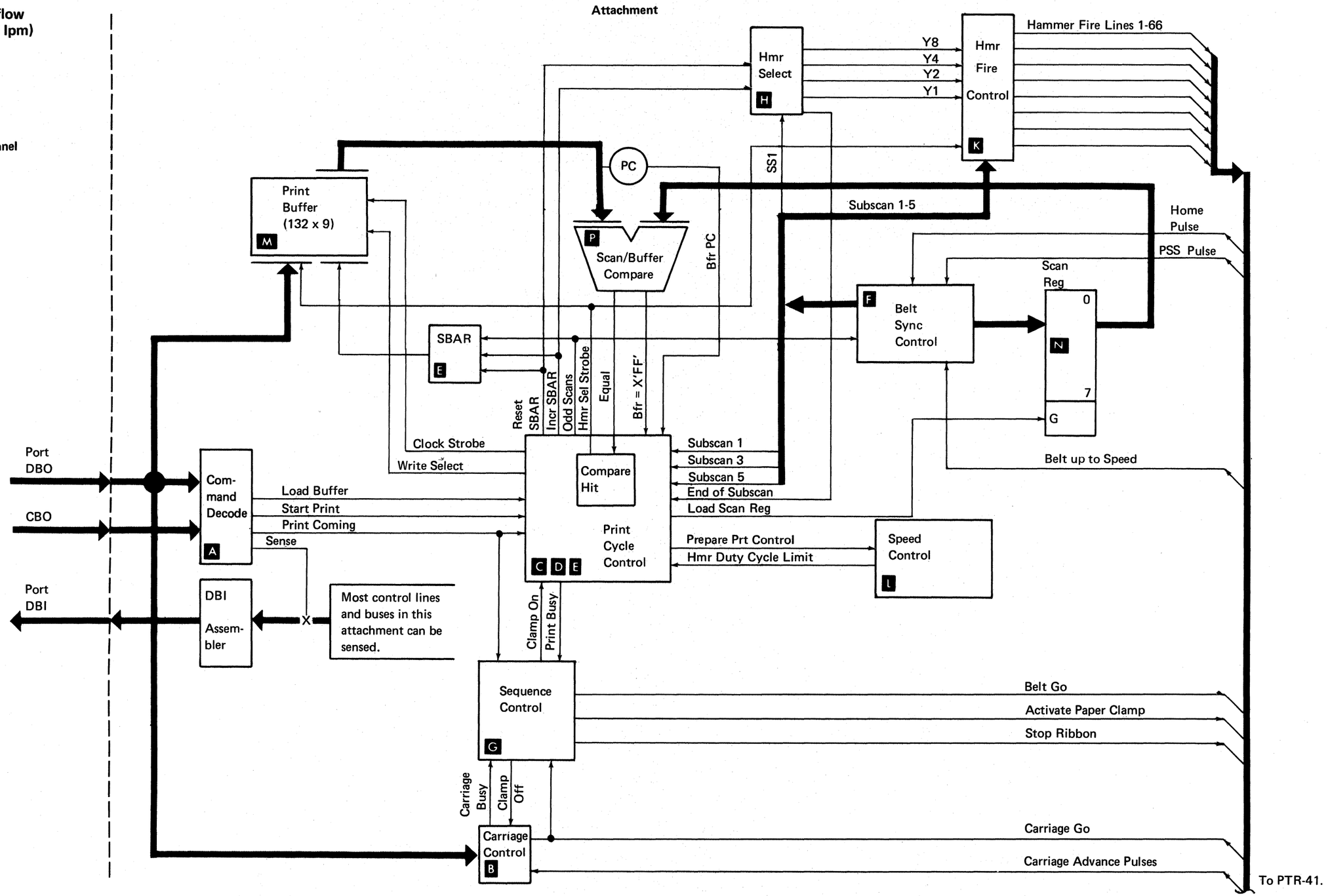
There are two types of switches:

1. Normally ON, red plunger. The south pole of a permanent magnet is positioned over an integrated circuit thus holding the output stage on. Pressing the switch plunger moves the permanent magnet, placing the north pole over the integrated circuit and the output turns off. The plunger is returned to the normal state by a return spring.

2. Normally OFF, black plunger. The north pole of a permanent magnet is positioned over an integrated circuit thus holding the output stage off. Pressing the switch plunger moves the permanent magnet, placing the south pole over the integrated circuit and the output turns on. The plunger is returned to the normal state by a return spring.



Attachment Dataflow (50, 100, and 155 lpm)



To PTR-41.

Attachment Functional Units (50, 100, and 155 lpm)

Printer Command Decode DQ020, 030, 040 A [1]

The printer command decode selects the various I/O device operations by decoding the values of DBO and CBO sent to the attachment. The values and their meanings are:

I/O load
I/O control load
I/O sense
I/O control sense
I/O jump

Space Counter DQ100 B

The space counter is a 7 position binary counter. The number of lines to be spaced or skipped is set into the space counter by the micrprogram. The counter is then decremented by one for each line spaced until it reaches 0. This brings up the 'steps 0' line which resets the space time latch and stops the carriage operation.

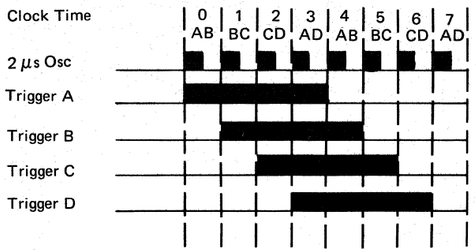
Scan Counter DQ160 C

The scan counter is a 8 position binary counter used to count the number of print scans taken to determine when to end the print scans. The output is decoded into 49 or 65 depending on the character set size being used.

Clocking Triggers DQ170 D

The clocking trigger pulses are generated by a 4 position binary counter. These pulses provide the basic timing used during a print operation.

There are four basic timing pulses generated (trigger A, B, C, and D). The clock pulses 5, 6, and 7 are generated by ANDing certain conditions of the clocking triggers.



Storage Buffer Address Register (SBAR) DQ180 E

The SBAR is an 8 position binary counter used to sequentially address the print buffer. See PTR-28 for the addressing sequence.

Belt Position Counter (BPC) DQ200 F

The BPC is an 8 position binary counter which maintains a count of the character position currently aligned with print position one.

The output of the counter is used as an input to the scan register and the home detection circuits.

Paper Clamp Timer DQ240 G

The paper clamp timer is a 4 position binary counter used to signal the condition of the paper clamps to the attachment.

The paper clamp should be on 15 ms after it is told to turn on by the microprogram. There is no feedback to insure that the clamp is actually on. The clamp is considered to be on when the timer has timed 15 ms. When it reaches 15 ms the timer turns on the clamp on latch.

Similarly, when the clamp is told to turn off, it should be off after 11 ms. When the timer reaches 11 ms it turns on the clamp off latch.

Hammer Select Control DQ290 H

The hammer select control is a 4 position binary counter used to generate the hammer select lines (Y8, Y4, Y2, and Y1). These hammer select lines, in conjunction with the subscan lines (SS1, 2, 3, 4, and 5) determine which hammer will be optioned to fire at any given time. The hammer select lines provide an input to the hammer fire control, where hammer optioning takes place.

Elapsed Time Counter DQ300 J

The elapsed time counter is a 10 position binary counter used to generate an interrupt after a selected time delay. The selected delay is loaded by an I/O control load micro instruction. The counter is then decremented by one until it reaches 0. This brings up the 'elapsed time counter is 0' line which sets the interrupt.

Hammer Fire Control (50, 100, and 155 lpm) K

The combination of hammer select lines (Y8, 4, 2, 1) and the subscan lines (SS1, 2, 3, 4, 5) selects which hammers are optioned:

Hammer Select Lines	+ Subscan	= Hammer
1	1	1
2	1	11
3	1	21
1	2	2
2	2	12
3	2	22

The hammer select strobe line becomes active when the optioned hammer is to be fired. On the following subscan, the hammer that was set to fire is fired by the fire 1, 2, 3, 4, or 5 pulse.

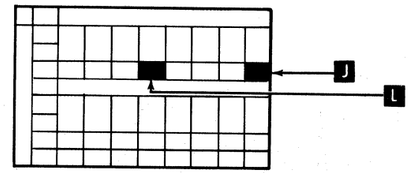
Printer Speed Control L

The speed of printing is controlled by the value of a 12 position binary counter. The value decoded from the counter determines how long 'hammer duty cycle limit' is active:

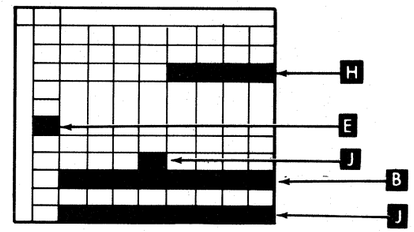
1164 ms for 50 lpm
564 ms for 100 lpm
364 ms for 155 lpm

The 'hammer duty cycle limit' line holds up 'print busy' to the channel thus limiting the printing speed.

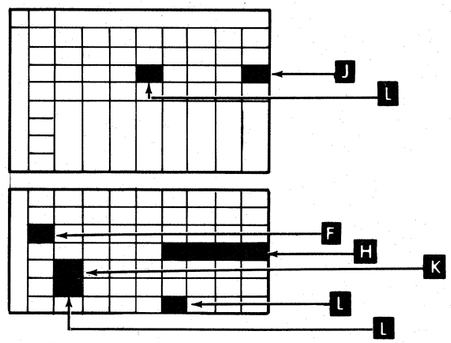
Load Command PTR-8



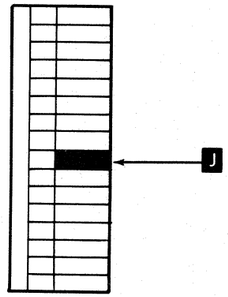
Control Load Command PTR-10



Sense — Control Sense Command PTR-14



Jump I/O Command PTR-20



[1] These keys also refer to PTR-38.

Attachment Functional Units (50, 100, and 155 lpm) — Continued

Print Buffer DQ180 M [1]

The print buffer consists of a 128 x 9 bit RAM (random access module) and an auxillary 4 x 9 bit RAM. The two combine to make up the 132 positions for the entire print line. The print buffer contains PFN (print fire numbers) arranged in the sequence in which they are optioned:

Print Buffer	Print Position
00	01
01	11
02	21
03	31

See PTR-28 for buffer arrangement and PTR-27 to determine the value of the PFN.

The PFN is compared to the contents of the scan register. When a match occurs, the print position being addressed is fired. This buffer position is then blanked by writing a hex FF into it.

Scan Register DQ200 N [1]

The scan register is used as a holding register for the value of the BPC. It is set on subscan one held through subscan five of each print scan.

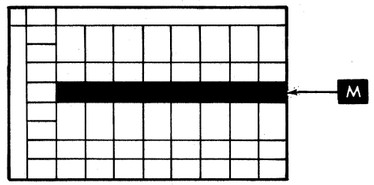
The output of the scan register is used in the scan/buffer compare to determine when to print a given print position.

Scan/Buffer Compare DQ280 P [1]

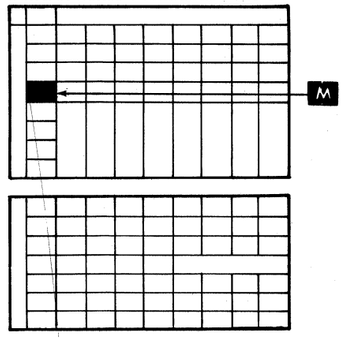
This circuit is used to compare the contents of the scan register with the contents of the print buffer. The data is checked for an equal compare and also for a blank (all positions printed) condition. The nonblank found latch is reset at the beginning of each print scan. It is set when any PFN is found in the print buffer. If no PFN is found by the end of the print scan, the nonblank found latch remains reset and this sets the early end of superscan latch.

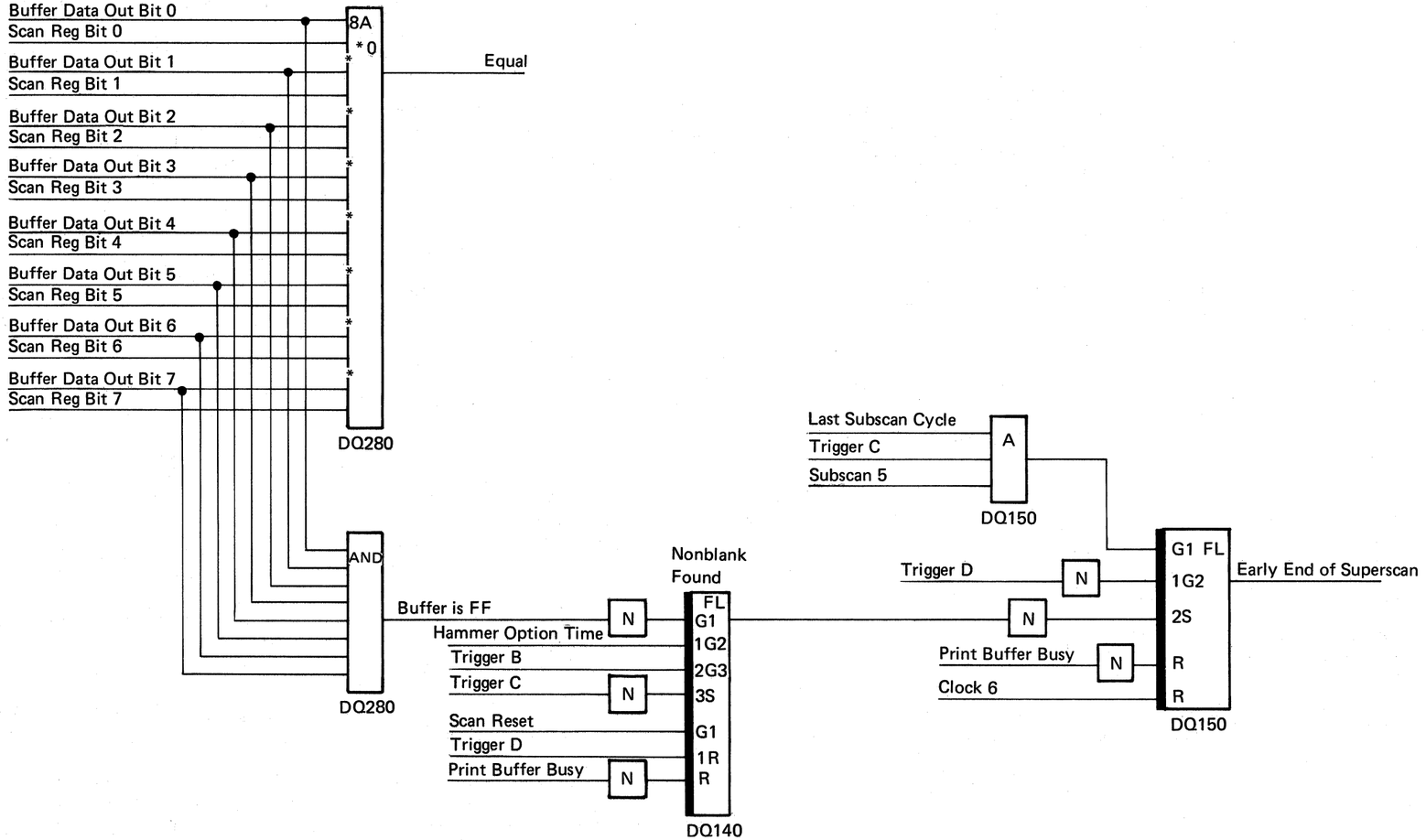
[1] These keys also refer to PTR-38.

Load Command PTR-8



Sense — Control Sense Command PTR-14





Printer Functional Units and Dataflow (50, 100, and 155 lpm)

A Type Belt Motor and Drive

The 'belt go' signal from the attachment starts the type belt motor. The motor accelerates in increments up to running speed and maintains this speed as long as 'belt go' is active. 'Belt up to speed' becomes active a maximum of one second after 'belt go' is activated.

B Home Pulse and Print-Subscan Pulse Generation

These pulses, generated as the timing marks on the type belt pass a transducer tip, are valid only when the type belt is up to speed. Home pulses (one between each complete character set) are generated by sensing a missing timing mark on the belt. When the belt is up to speed, the continuing home pulses verify that the attachment is in sync with the printer. If the printer is not in sync with the attachment, a belt sync check is indicated.

Print subscan pulses are produced by the timing marks on the belt and by an electronically inserted pulse between each mark.

C Forms Thickness Control

The forms thickness control mechanically adjusts the print unit forward or back for different form thicknesses. The control also adjusts a potentiometer for varying the duration of the singleshot hammer-fire pulse. As the print unit is adjusted for thicker forms, the pulse duration is increased.

D Ribbon Drive

When the ribbon solenoid is deenergized, a clutch engages to drive the ribbon. The ribbon begins to move when printing starts (or during the completion of the first line printed) and continues to move only during printing. After printing stops, the ribbon continues to move until the solenoid is energized to disengage the clutch.

E Paper Clamps

The upper paper clamp consists of one magnet and a clamp bar. The lower paper clamp consists of two solenoids and a clamp bar. Both clamps are activated by the attachment clamp holding the paper during printing.

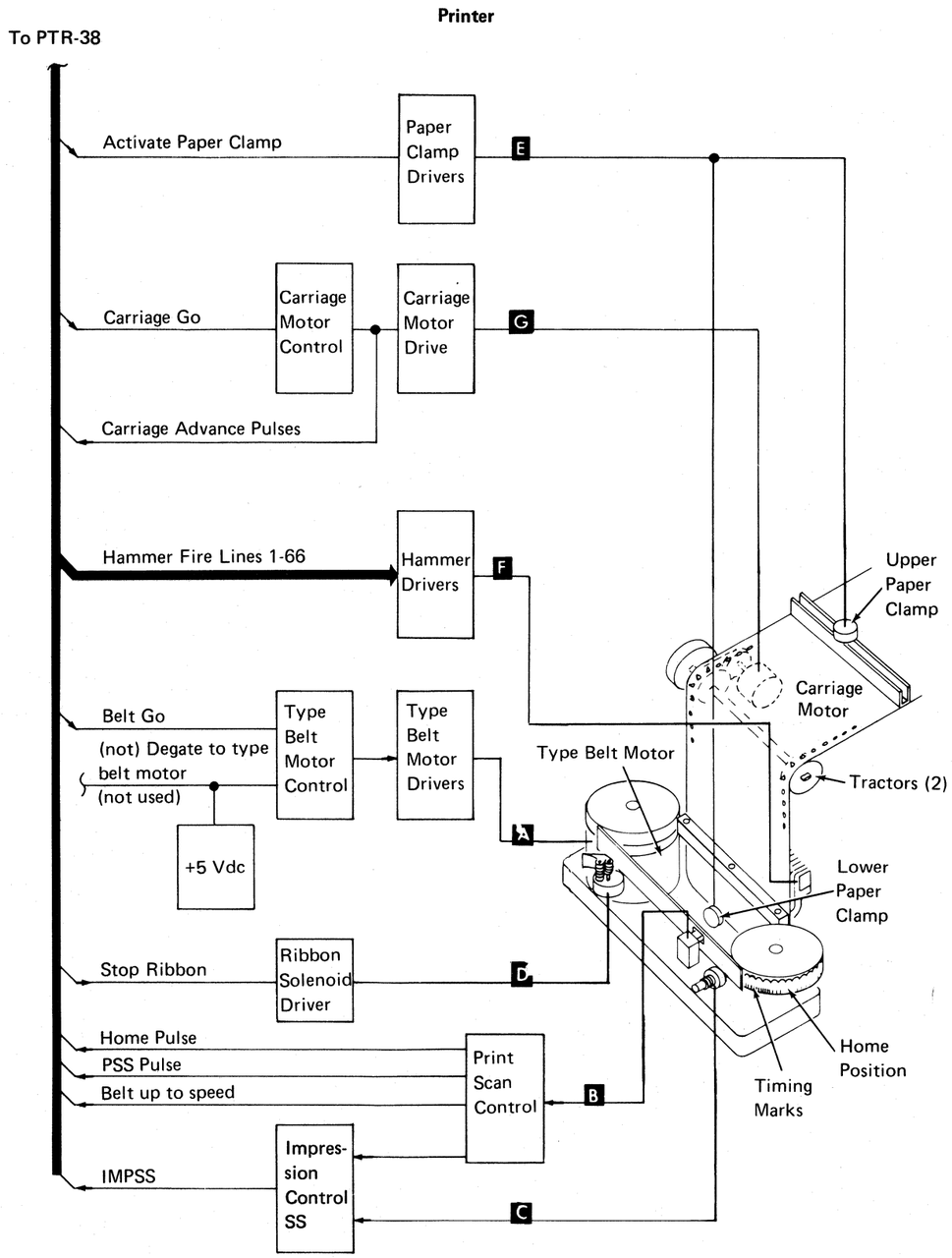
F Firing the Hammers

Each hammer spans two print positions. For each print line, a hammer is addressed to print twice; first for printing the odd print position, then for the even print position. Hammer firing is controlled by the attachment with the timing provided by the printer.

G Carriage Spacing

When a print line is complete, the attachment releases the paper clamps. The forms can now be advanced. To advance the forms, the attachment activates 'carriage go'. The printer electronics then generates 'carriage advance' pulses which control the carriage motor. The attachment counts the advance pulses and deactivates 'carriage go' on the sixth step. Deactivating 'carriage go' initiates two stop pulses for a total of eight stepper motor pulses. This moves the paper 1/6 inch (4.22 mm).

The printer is ready for the next print line cycle. If printing is continuous, steps D through E are repeated.



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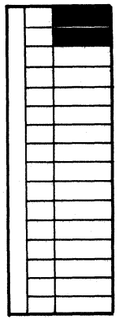
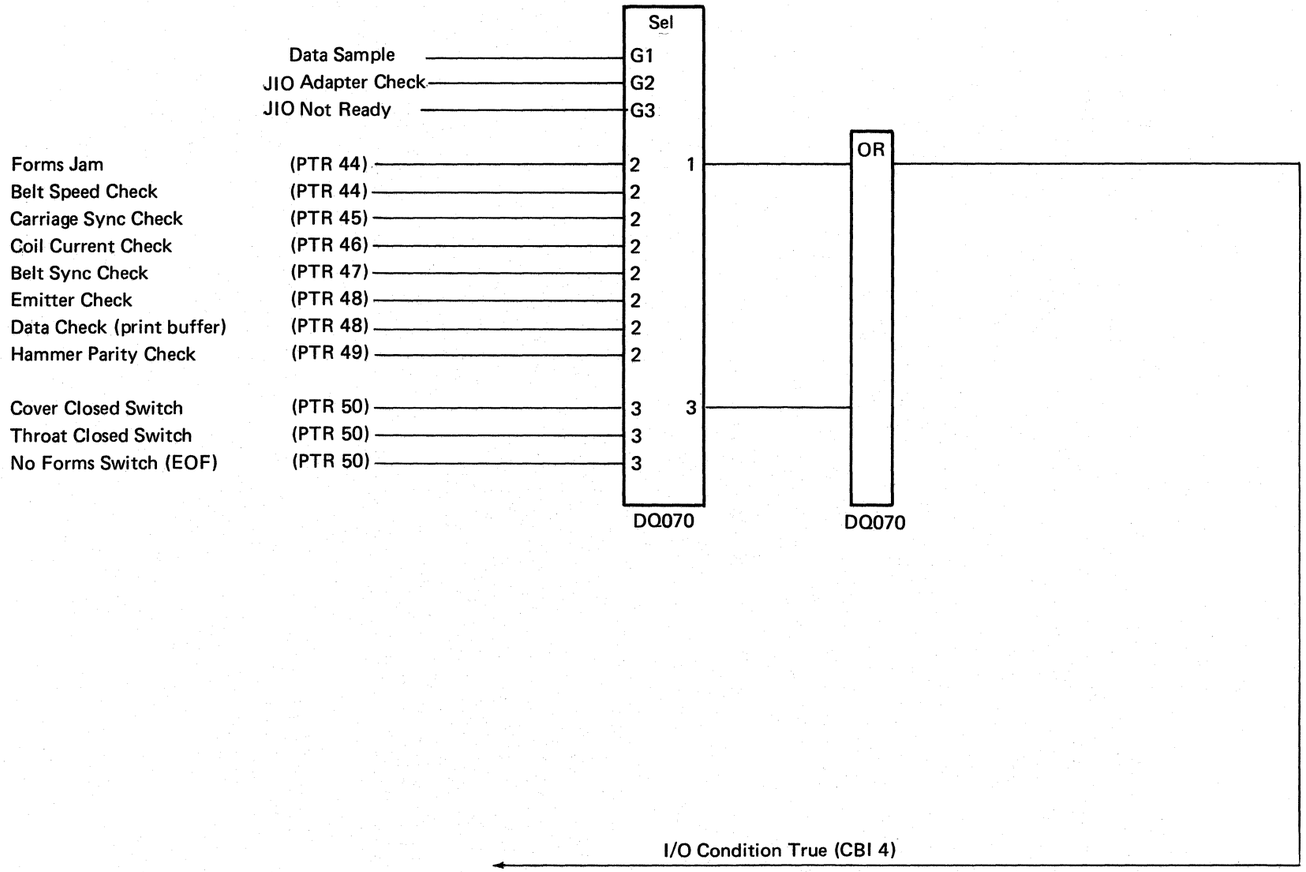
Error Conditions (50, 100, and 155 lpm)

The jump I/O command (see PTR-20) detects either the adapter check or not ready condition. A sense command is then required to determine the specific error. See *Sense Command* on PTR-14.

Jump I/O Command PTR-20





Unprintable Character

One or more of the characters requested to be printed were not in the print image. Unprintable character is checked entirely by the microprogram. There is not hardware checking involved. Setting of this check is a programmer option.

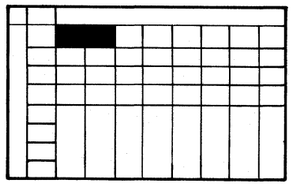
Forms Jam Check/Belt Speed Check (50, 100, and 155 lpm)

Forms Jam Check

The forms jam check indicates that the carriage tractor was told to move, but no paper motion occurred. A light emitting diode detects the time between holes in the paper. If no hole is detected in eight lines, the forms jam is set.

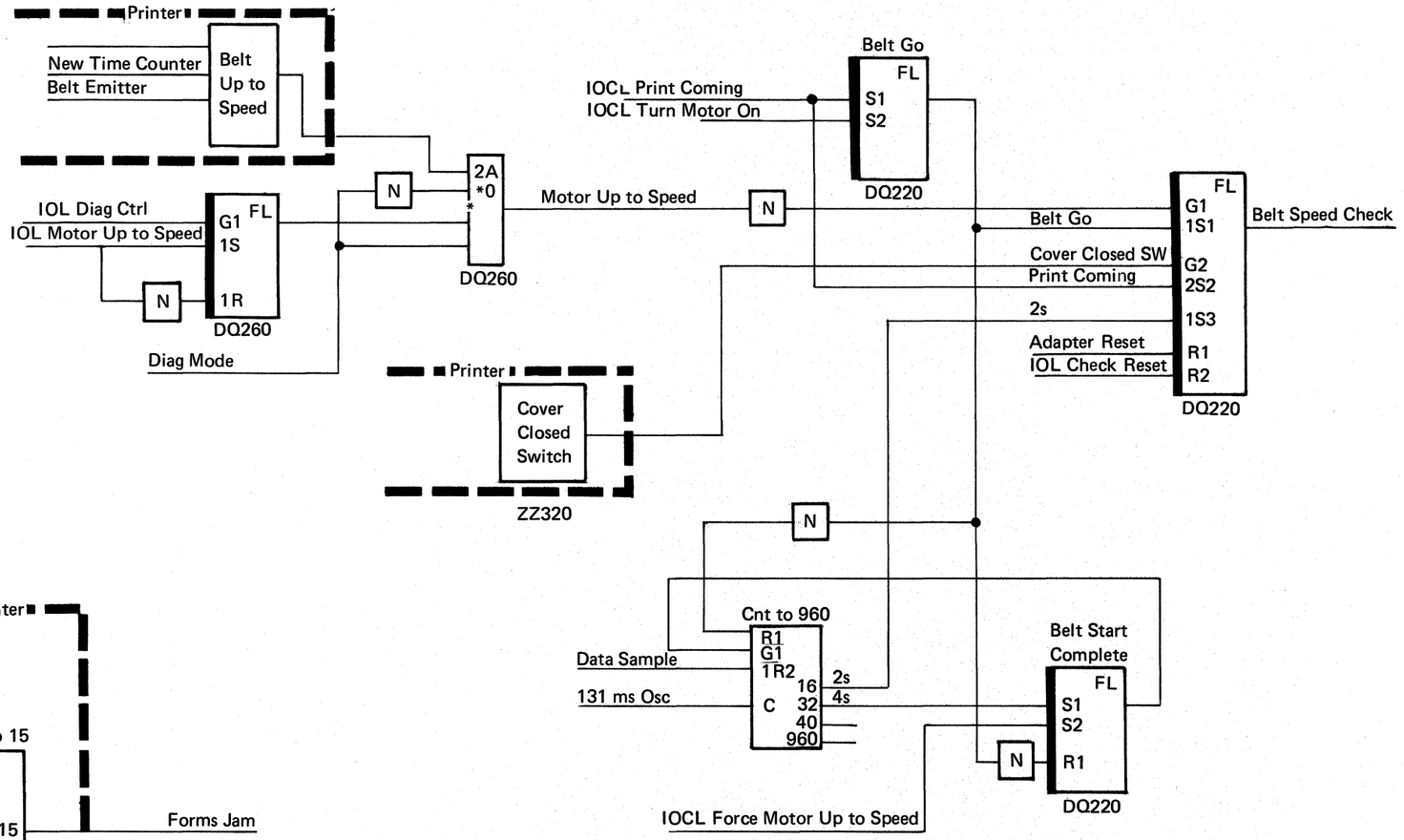
Note: The light emitting diode is infrared so you cannot see the light.

Control Sense Command PTR-14



Belt Speed Check

This check indicates that either the belt has failed to get into motion within two seconds after the start time or the printer belt motion is lost after having reached an up-to-speed condition. Motion is considered lost if there is a 25 per cent loss in operating velocity. The speed is determined by measuring the time between timing marks on the print belt.

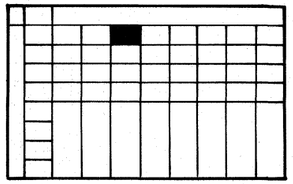


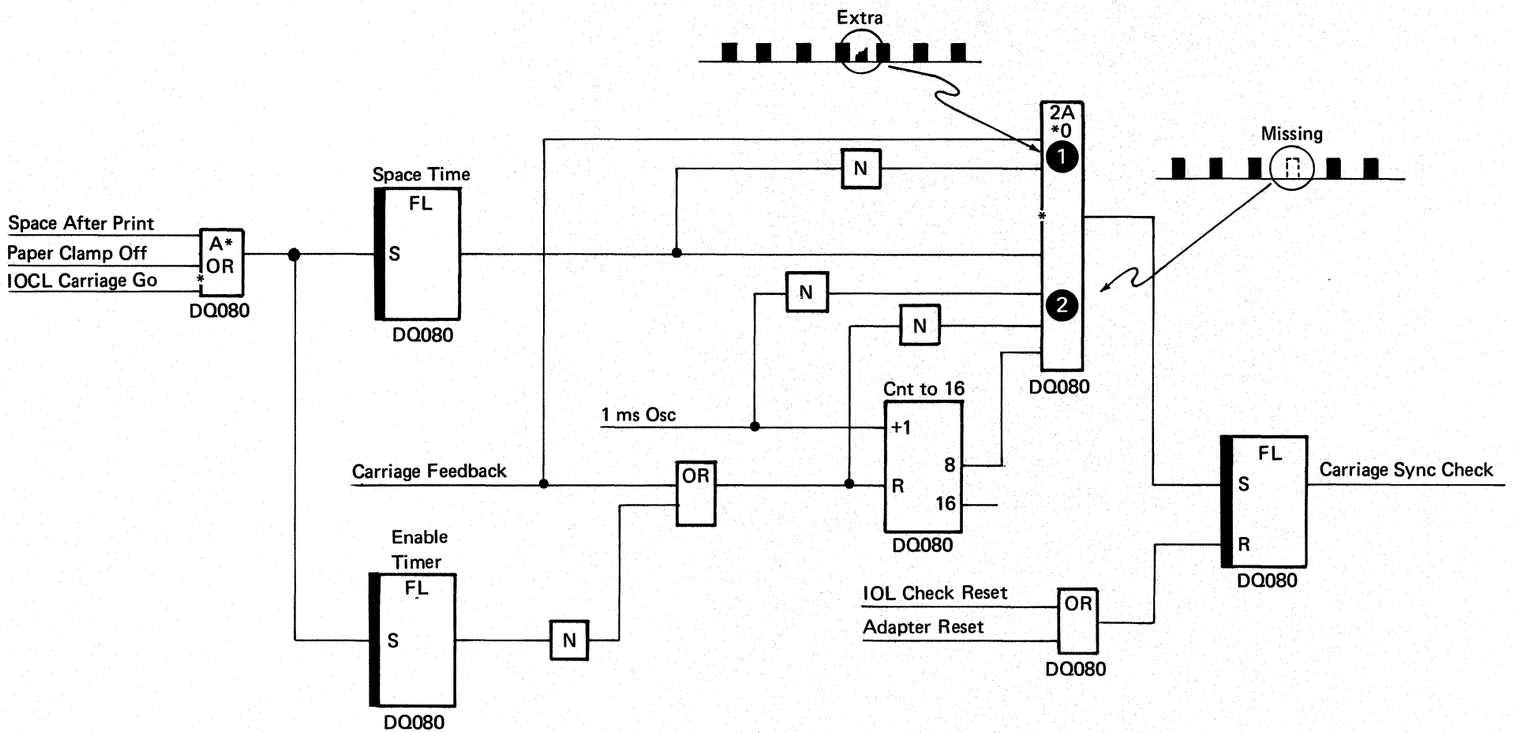
Carriage Sync Check

Two conditions may set this check:

1. If a carriage feedback pulse (carriage advance pulse) occurs when no carriage motion has been initiated.
2. If a carriage feedback pulse fails to occur within 8 ms, during carriage space time.

Sense Command PTR-14

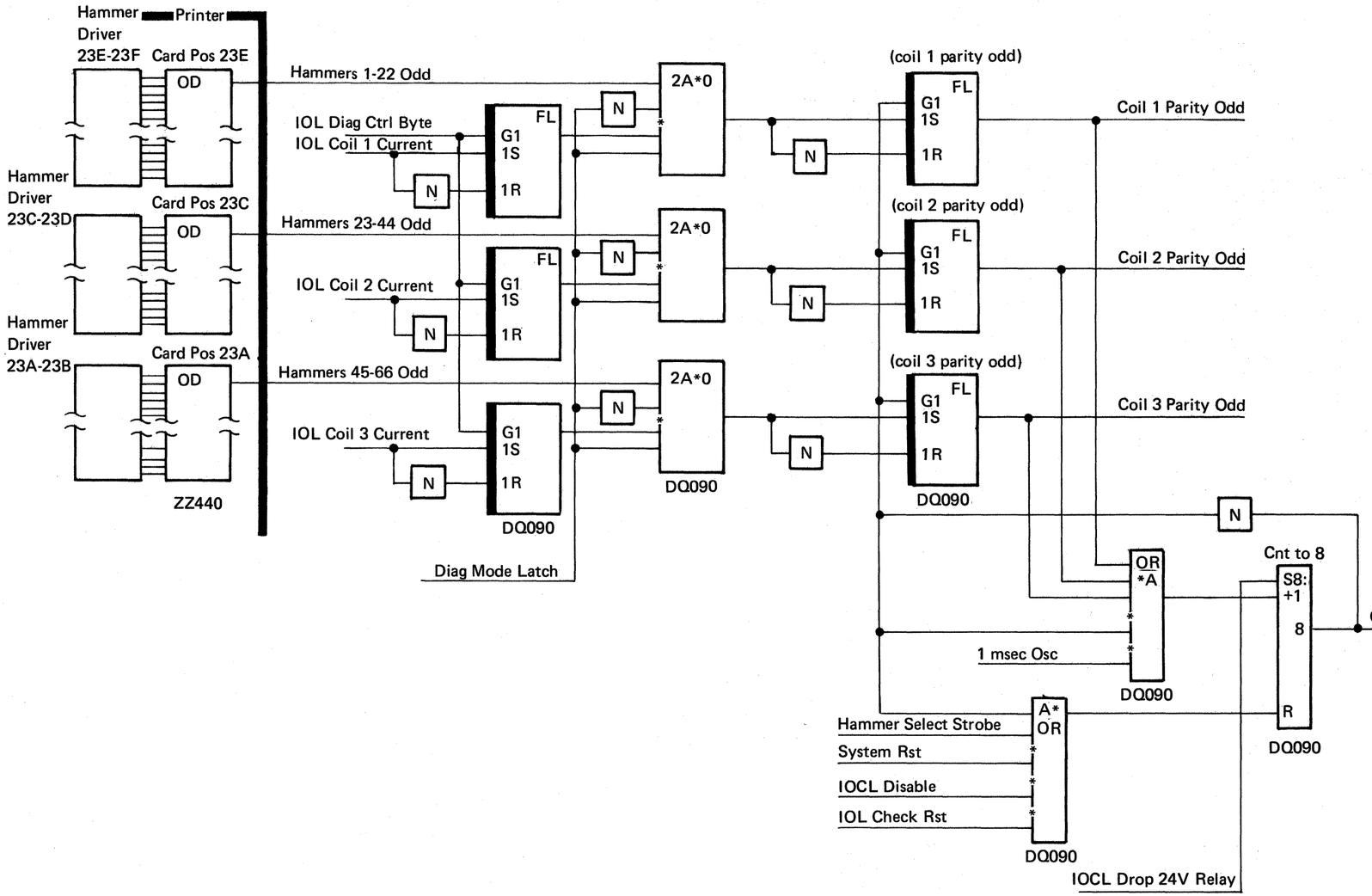




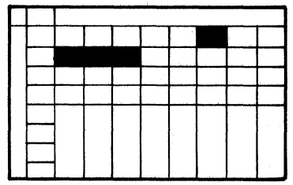
Coil Current Check (50, 100, and 155 lpm)

An 8 ms timer (cnt to 8) is started when hammer select strobe sets a hammer latch. Coil parity odd, coil 2 parity odd, and coil 3 parity odd lines are monitored for the possibility of a hammer being on longer than 8 ms. If this condition is detected, power is dropped to the printer and coil, current check is set. The status of the coil 1 parity odd, coil 2 parity and coil 3 parity odd lines is saved in their respective latches. This is because the coil check line being active degates the reset of the latches.

Note: If an even number of hammers, on one hammer driver card, are on (longer than 8 ms), the coil current check is not set. This is because the hammer and odd lines are only active for an odd condition within any one of the three card positions.



Sense Command PTR-14



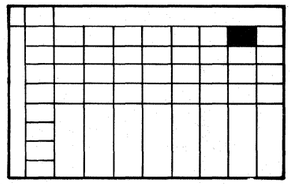
Belt Sync Check

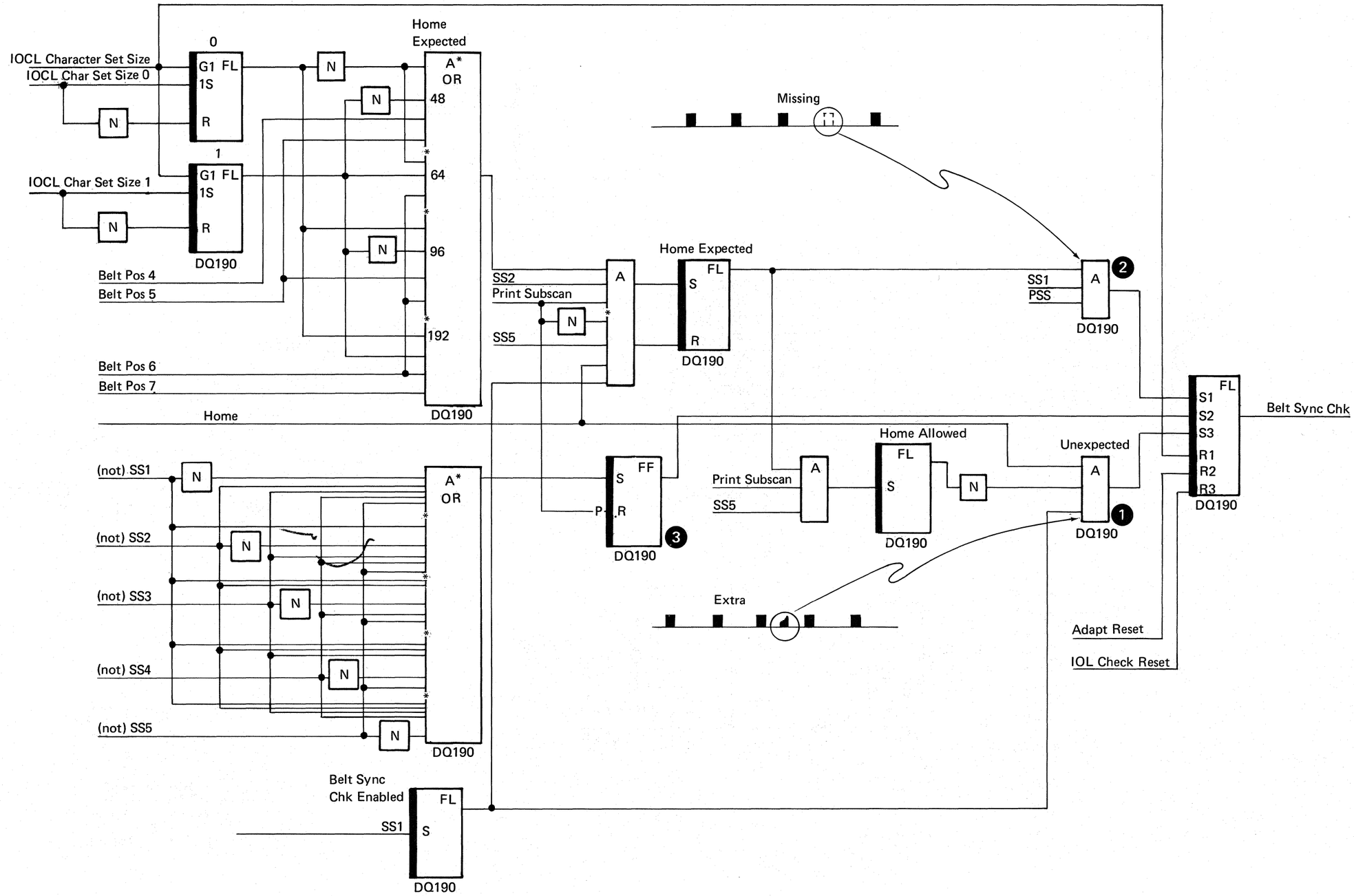
This check can be set by three possible conditions:

1. If a home pulse occurs when not expected.
2. If a home pulse fails to occur when expected.
3. The bit ring generating the five subscan pulses is continuously monitored for an abnormal condition. Normal is one, and only one pulse on at any time.

The timing for the home pulse is determined by counting the number of print scans. This count is compared with the character set size (only one home pulse per character set).

Sense Command PTR-14



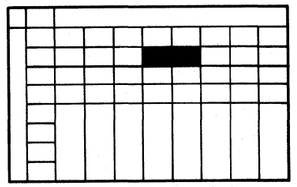


Emitter Check/Data Check

Emitter Check

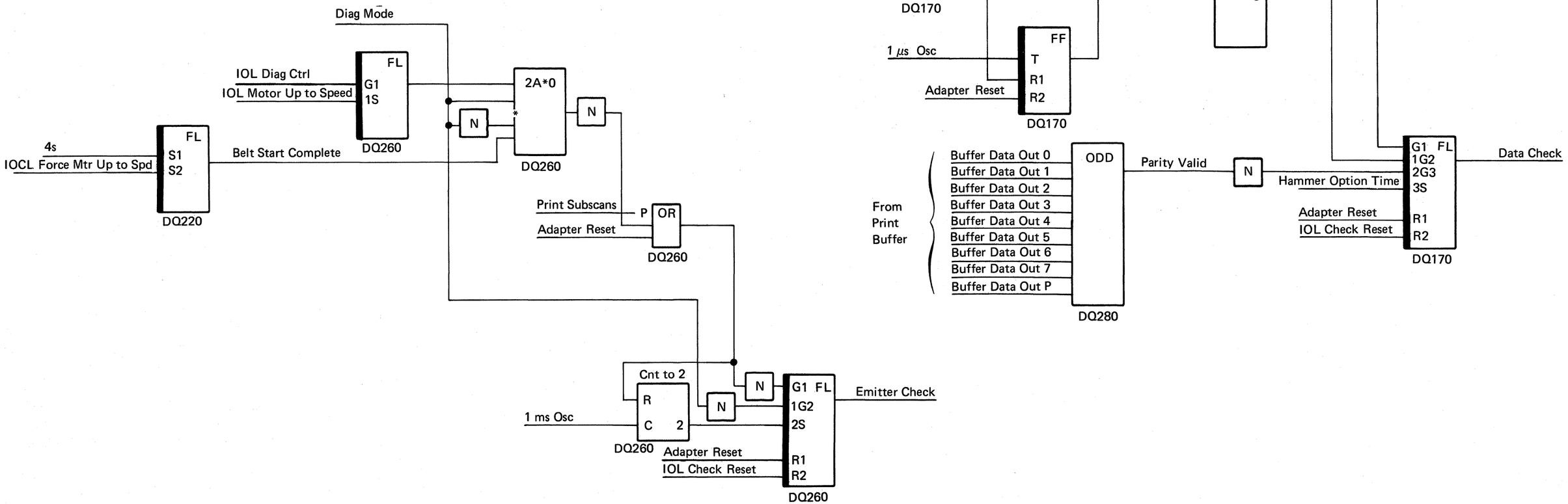
Once the print belt motor has reached an up-to-speed condition, the print subscan line is monitored to verify that it is oscillating. If no change occurs during any 2 ms period, the emitter check is set. This check supplements the belt sync check which cannot detect a broken or stopped belt.

Sense Command PTR-14



Data Check

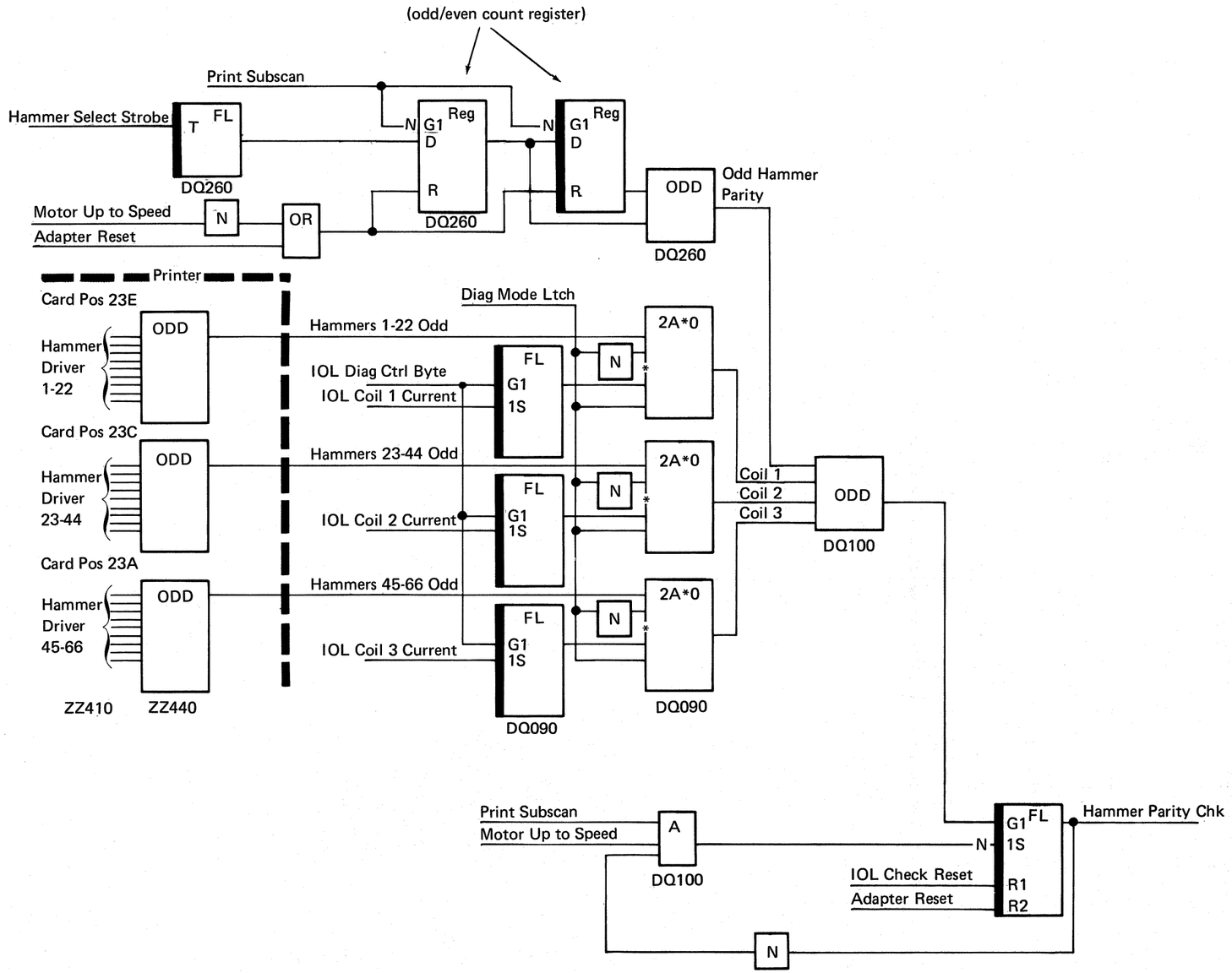
Parity is maintained on the data in the print buffer. If invalid parity is detected during a print cycle, this data check is set.



Hammer Parity Check (50, 100, and 155 lpm)

An odd/even count of the hammer select strobe pulses is kept track of by the two position odd/even count register. The output of this register indicates whether an odd or even number of hammers have been selected to fire (one hammer select strobe pulse for each hammer selected). The hammer odd line is active for each hammer odd card that indicates an odd number of hammers are being fired. The odd/even count register is compared to the status of the three hammer odd lines during each print subscan pulse. If a mismatch occurs the hammer parity check latch is set.

Sense Command PTR-14

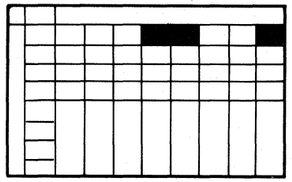


End of Forms/Cover Closed/Throat Closed (50, 100, and 155 lpm)

End of Forms (EOF)

End of forms is checked on the first line printed of each new form. If no forms is indicated by the no forms switch, the printer will go not ready.

Sense Command PTR-14

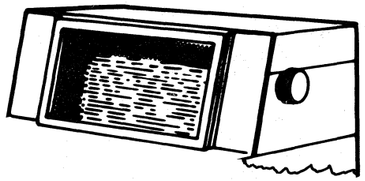


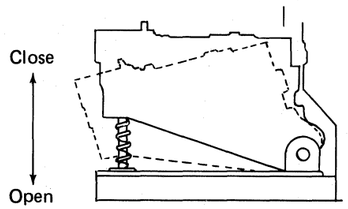
Cover Closed

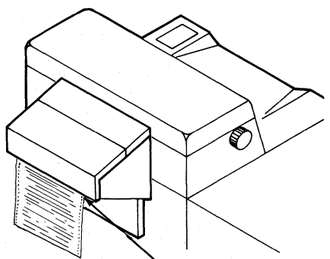
The printer is not ready if the cover is open.

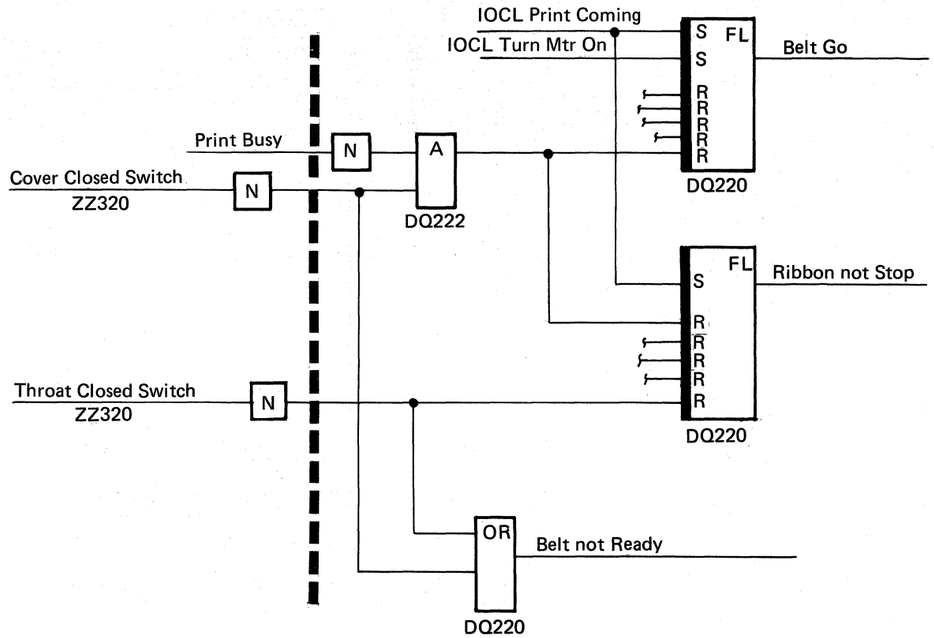
Throat Closed

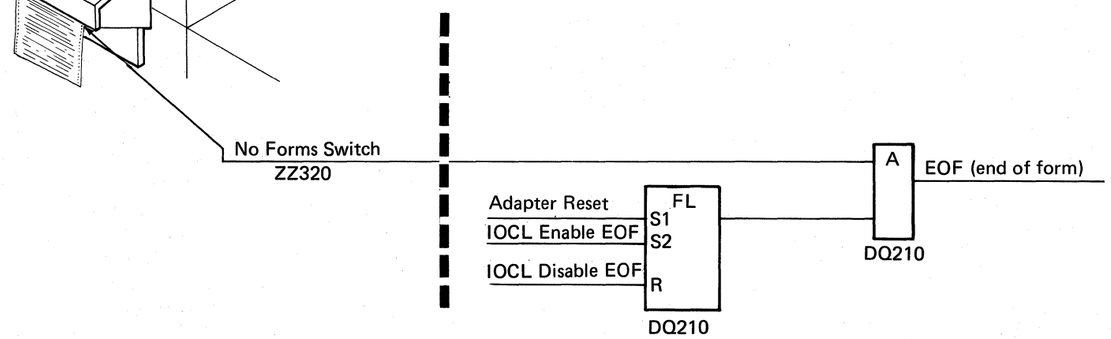
The printer is not ready if the throat is not closed on the paper path.











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CPU/Attachment/Printer Operation

Printer operation is controlled by the microprogram commands in the CPU. The commands are:

LOAD
CONTROL LOAD
SENSE
CONTROL SENSE
JUMP I/O

Interrupts if enabled occur at the completion of a printed line, a carriage function, or when the elapsed time counter reaches zero. The next command is then initiated.

Data Area

Output data flow to the printer is from a 132-byte I/O area in main storage, called the line printer data area. Beginning at the leftmost byte, this data area in main storage corresponds character for character to the print line beginning at print position one.

Belt Image Area

A character set image is defined as the sequence of print characters as they appear on the type belt. Before printer operations begin, a given character set size must be provided and the image must be loaded into the belt image area of control store. For reference by the printer microcode, the belt image is then transferred to main storage location.

Three character sets are available: 48, 64, and 96. The 48-character set is:

A-Z 0-9 $, . + - * / % @ # & '

The 64-character set consists of the above 48 characters plus the special characters:

( ) = _ : ; " ? ¢ > < | ! ¬ \

The 96-character set includes all characters in the 48-character set, the lowercase alphabetic characters, plus the following special characters:

[ ] ! ¼ _ : " + ² ¶ ◦ ± ¢ ( ) ; ½ ? = ® § ³ £ '

Forms Control

Forms movement is also controlled by the printer microprogram. Forms length must first be defined by the program located in control storage. The printer must also be initialized to a line within that forms length. The maximum length of forms is 84 lines.

The forms length and current print line values (destination print line when the carriage is moving) are maintained by the printer microprogram.

End of Operation Interrupts

Any operation initiated by the printer microprogram results in an interrupt at the end of the operation. These interrupts are processed by the microprogram. Any checks that occurred during the execution of the completed operation are handled immediately to prevent loss of the check status.

Attachment Operation

A print buffer is located in the attachment. It permits overlap of line printing and carriage spacing with other I/O device operations and CPU execution.

The data in the print buffer is compared to the value of the scan register. If they are equal, the corresponding hammer is selected and fired.

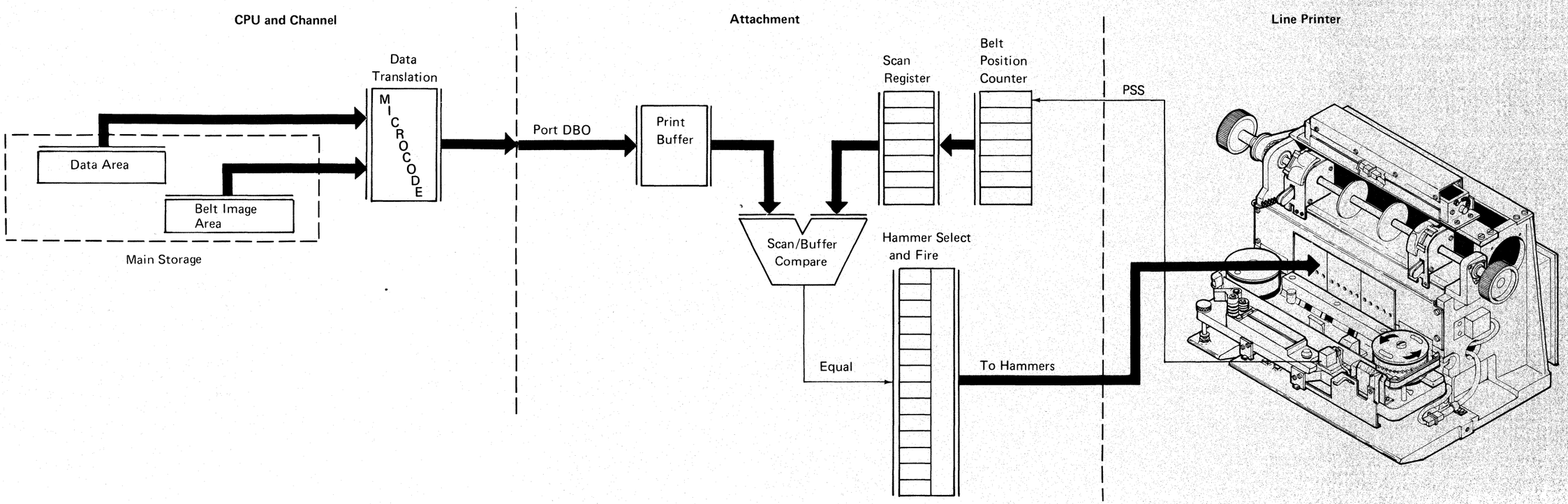
The data area, located in main storage, containing the print line is not changed by printing. This leaves the complete print line available for error recovery procedures (ERP).

The following keyboard functions are provided for operator control of the printer:

Carriage restore
New line (space one line)
Reset line counter to 1 (tells the system the form is on line 1.)

When the printer function keys are used, all pending check conditions are reset prior to executing the function. Also an interrupt occurs at completion of the function, thus initiating any pending operations (commands).

Display of check or not ready conditions and recovery procedures are provided by the display screen. Operator response is always through the keyboard.



Theory of Printing (285 lpm)

The belt printer has 132 hammers, one hammer for each print position. The print operation is separated into these functions:

- *Subscans:* A subscan is the time required to option every fifth print position to every other belt position. Five subscans make one print scan.
- *Print scan:* A print scan is the time required to option one character to all print positions.
- *Print line:* A print line is 48 print scans for a 48-character set[1] (standard). That is, every character on the set is optioned to every print position.

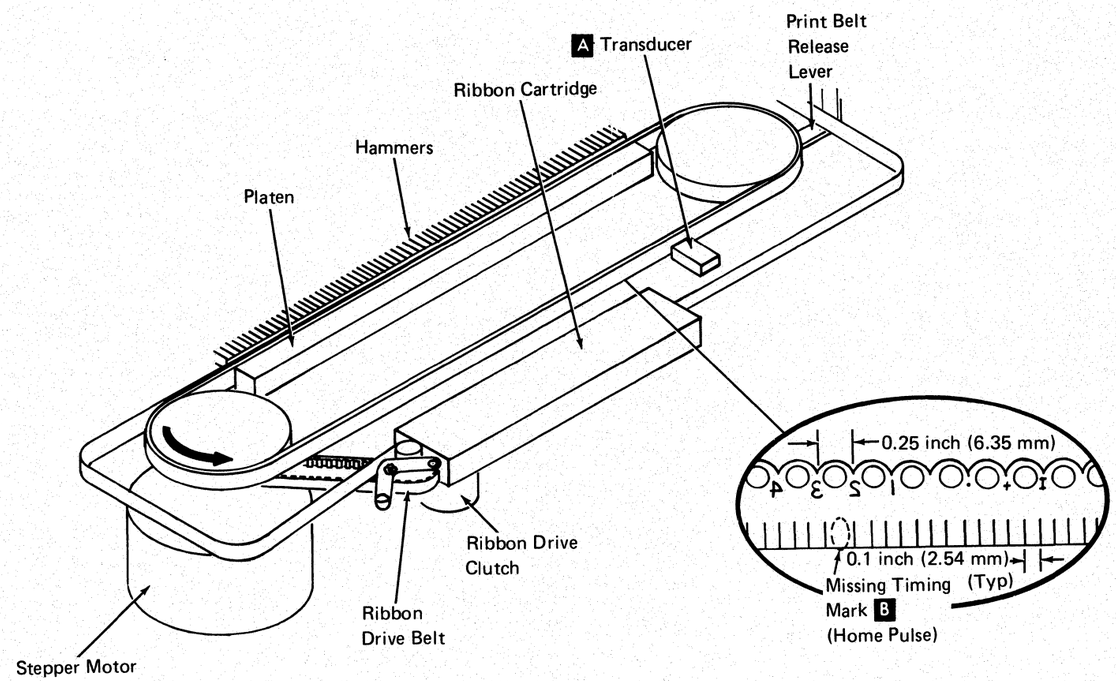
Each print position can print only one character per print line (when the print position is optioned and the character specified for that position is equal to the character aligned at that position).

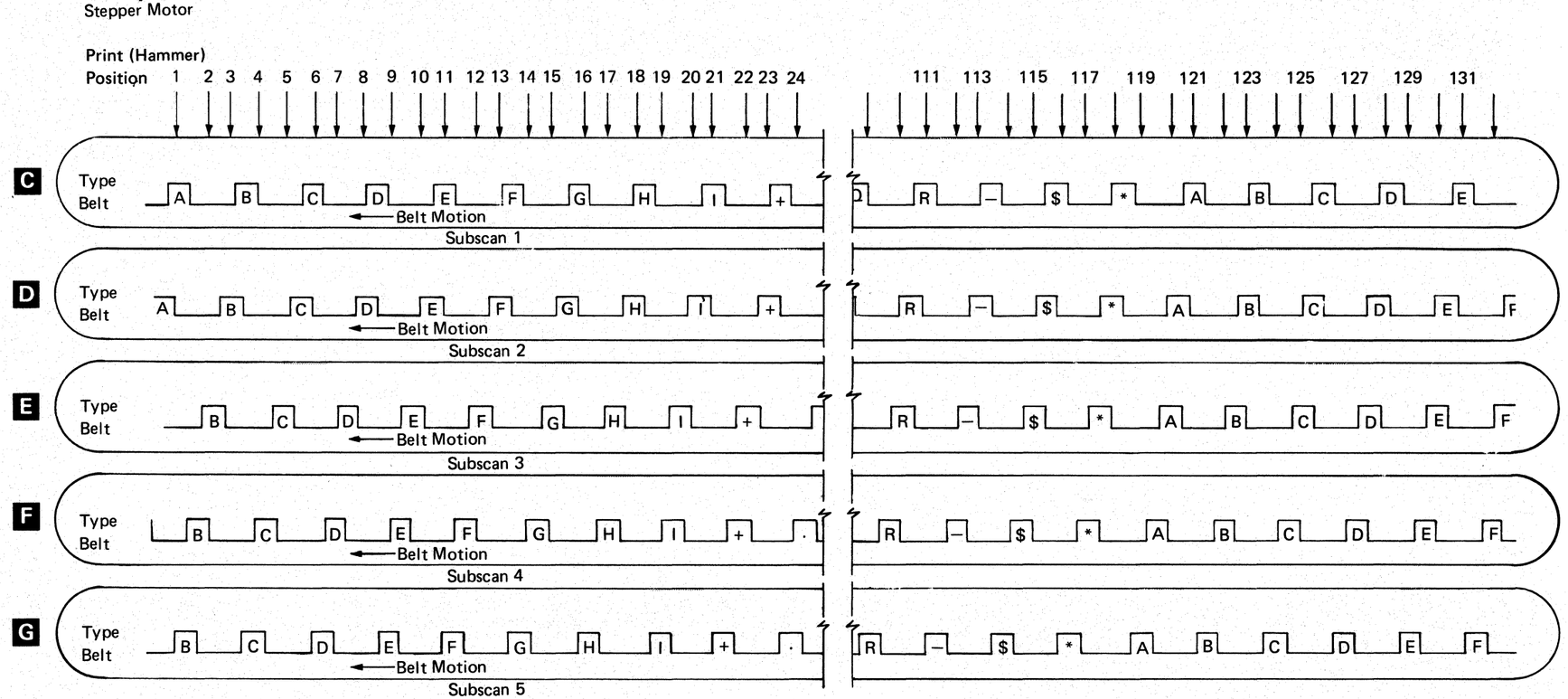
During a subscan, the hammers selected for firing are buffered in the attachment, and they are gang-fired at the start of the next subscan. Print scans are stopped early if all optioned hammers are fired.

To synchronize the type belt to the attachment, two types of pulses are required—a home pulse and the subscan pulses.

The home pulse is generated from the type belt by the transducer **A** sensing the missing timing mark **B** that identifies the home position. The home pulse occurs one subscan before the first character of each character set is aligned to print in position 1. Sensing the first home pulse initiates a continuing check of the synchronism of the home pulse with the belt position counter.

[1] The subscan pulses are generated by the transducer. Detecting the 64-character set takes 64 print scans; detecting the 96-character set takes 96 print scans. Two subscan pulses are developed from each timing mark.





Theory of Printing (285 lpm)—Continued

When synchronism is verified (sensing a second home pulse) printing can start.

Because the printer has a continuously moving type belt, the attachment must determine when to fire a hammer to print the specified character. Using the illustration C as a reference, observe the relationship between the moving type belt and the hammer positions. This shows the character A aligned with hammer 1 in print position 1.

Print optioning can start when a character is aligned with print position 1. The belt position counter keeps track of what character is aligned to print in print position 1. This value is set into the scan register at the beginning of each print scan. During the first hammer option cycle, the character specified for position 1 is compared to the character aligned at position 1. During this first subscan, every fifth position (1, 6, 11, 16, 21, etc) is compared with its respectively aligned character (every other belt character). If the character specified and the character aligned compare equal, the hammer is fired at the beginning of the next subscan D . This sequence, starting at print position 1, is called subscan 1.

At the end of subscan 1, the type belt movement aligns the character B with print position 3 as shown in the illustration D . Print optioning now continues with print position 3 and proceeds through every fifth print position until the character aligned with print position 128 is optioned. This sequence, starting with print position 3, is called subscan 2.

Belt movement has now aligned the character C with print position 5, as shown in the illustration E . Print optioning continues for every fifth position until the character aligned with print position 130 is optioned. This sequence, starting with print position 5, is called subscan 3.

Subscans 4 and 5 follow the same pattern (illustration F and G). Subscan 4 starts optioning with print position 2 and every fifth position through print position 132. Subscan 5 starts optioning with print position 4 and every fifth position through print position 129. These five subscans make the first print scan.

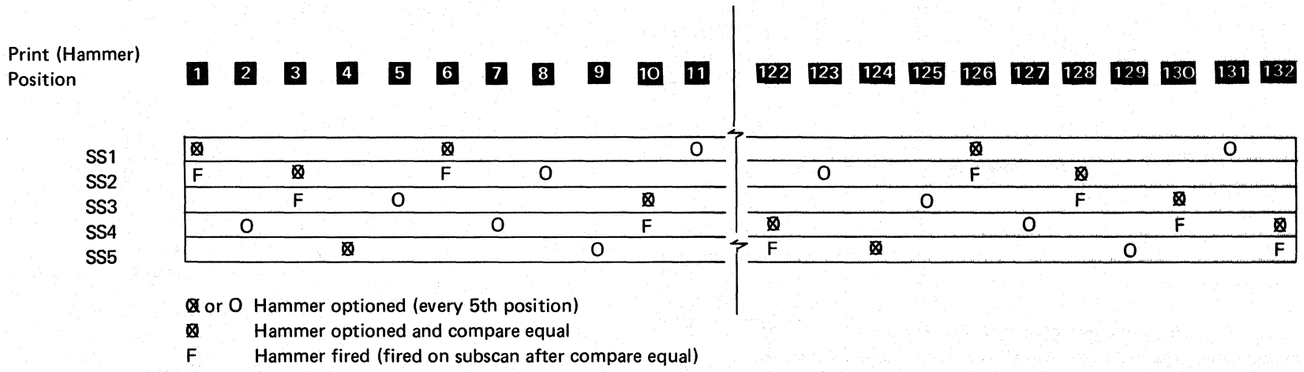
During this first print scan, each of the print positions was optioned to print one character, but only those hammers are fired that had the aligned character compare equally with the specified character.

The first print scan started with character A aligned at print position 1. Now, the character B is aligned with print position 1 and the second print scan is started.

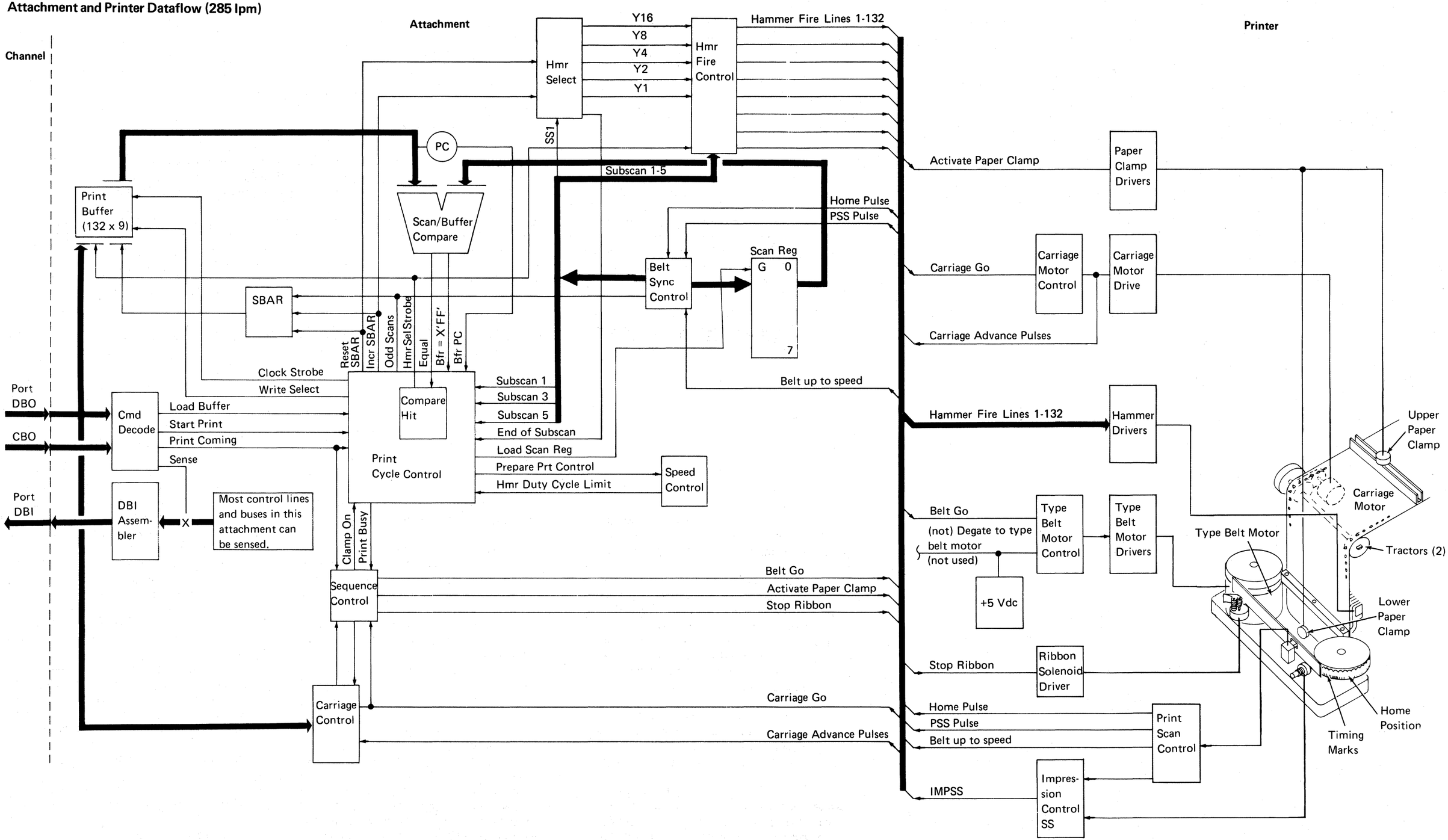
After the second five subscans, all positions are now optioned to print a second character. To option the 46 remaining characters to each print position, 46 more print scans are taken.

Hammers are fired for the optioned print positions that compare equal on each succeeding subscan. To reduce the hammer power requirements, only five hammers are allowed to fire on one subscan. If more than five optioned print positions compare equal, optioning starts again with 48 new print scans. Scanning starts again at print position 1 and positions not printed are optioned again.

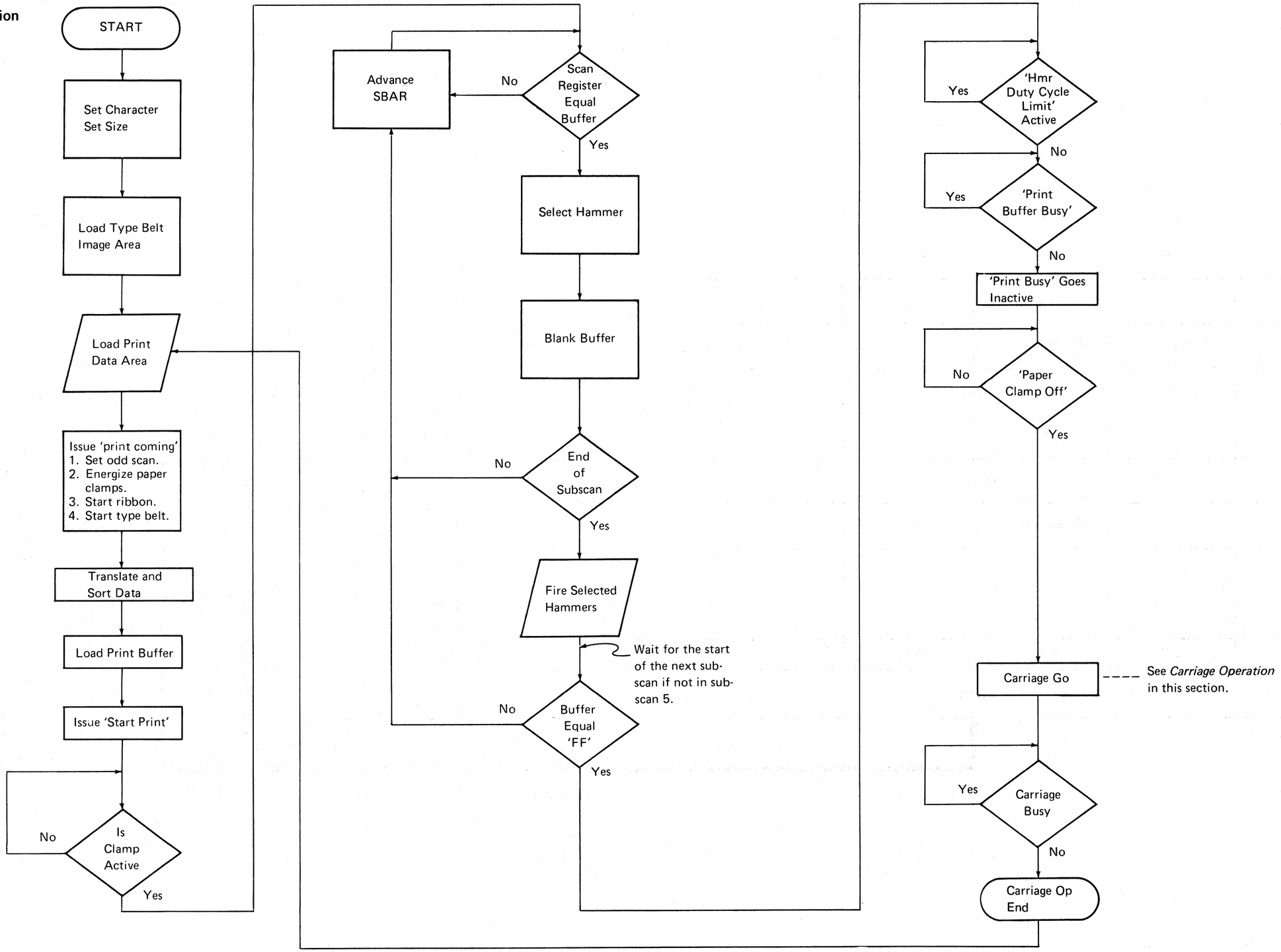
After the 48 print scans, an additional print scan (49) is taken to fire hammers selected during subscan 5 of print scan 48.



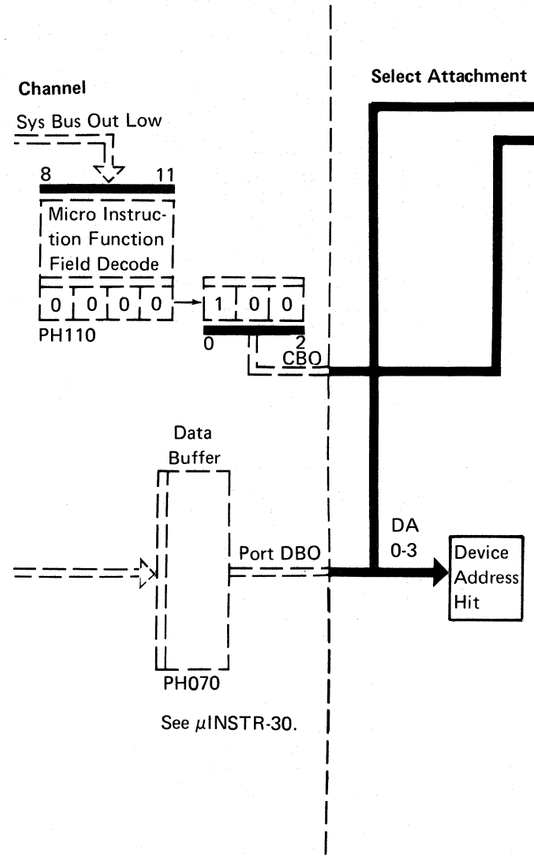
Attachment and Printer Dataflow (285 lpm)



Print Operation (285 lpm)



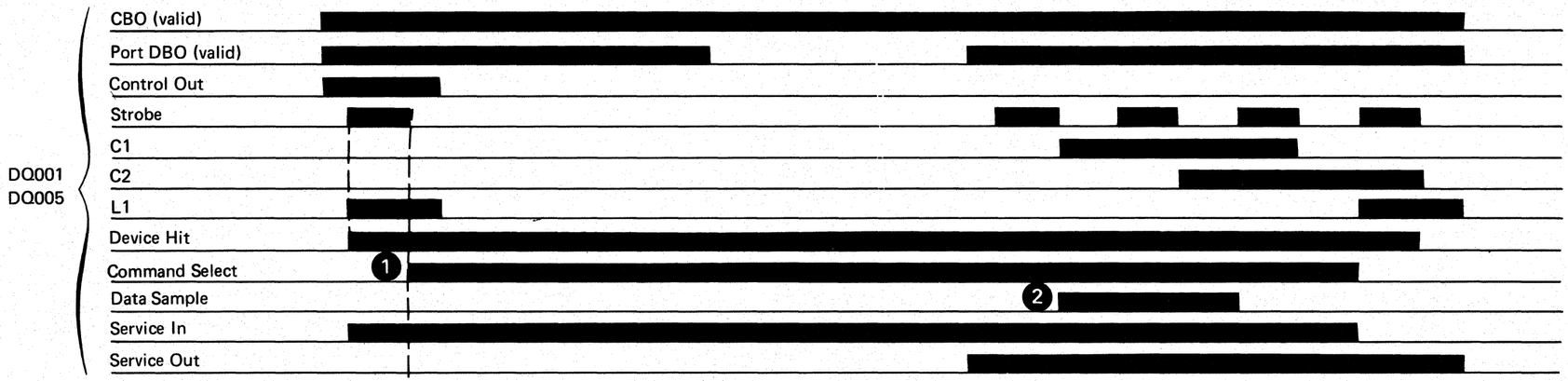
Load Command



CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 0 0	0 0 1 0 Set Interrupt Request								
	0 0 1 1 Reset Interrupt Request								
	0 1 1 0 Interrupt Request Control				Print Busy Off	Carriage Busy Off			Elapsed Time Counter
	1 0 0 1 Print Buffer**	Data to Print Buffer							
	1 0 1 1 Enable Diagnostic Mode*								
	1 1 0 0 Disable Diagnostic Mode*								
	1 1 0 1 Diagnostic Mode Control Byte*	2 μs Osc	Subscan	Home		Motor Up to Speed	Coil 1 Current	Coil 2 Current	Coil 3 Current
	1 1 1 1 Check Reset								

*Diagnostic usage only.
**Not permitted when busy.

Load Command (Continued)



Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
0010(2)		Set Interrupt Request	Sets the micro interrupt request latch which initiates an interrupt.	DQ270	1
0011(3)		Reset Interrupt Request	Resets the micro interrupt request latch.	DQ270	1
0110(6)	3	Interrupt Request Control	Turns on the interrupt print op end latch which allows the micro interrupt request latch to be turned on when print busy latch turns off.	DQ270	2
	4		Turns on the interrupt carriage op end latch which allows the micro interrupt request latch to be turned on when the carriage busy latch turns off.	DQ270	
	7		Turns on the interrupt elapsed 0 latch which allows the micro interrupt request latch to be turned on when the elapsed time counter reaches 0.	DQ270	
1001(9)	0-7	Print Buffer	Used to load the print buffer with the data on port DBO.	DQ180	2
1011(B)		Enable Diagnostic Mode	Turns on the diagnostic mode latch which is used to substitute test signals for actual signals (such as type belt emitter pulses).	DQ200	1
1100(C)		Disable Diagnostic Mode	Resets the diagnostic mode latch (see above).	DQ200	1
1101(D)	0	Diagnostic Mode Control Byte	Allows port DBO 0 bit to step the clocking triggers instead of the 1 μs osc.	DQ170	2
	1		Allows port DBO 1 pulse to be used to generate the subscan pulses instead of the raw PSS pulses.	DQ200	
	2		Uses port DBO 2 to represent home pulse rather than the actual home pulse.	DQ210	
	4		Substitutes the port DBO 4 bit for the motor up to speed line.	DQ260	
	5		Uses port DBO 5 in place of the coil 1 current line.	DQ090	
	6		Uses port DBO 6 in place of the coil 2 current line.	DQ090	
	7		Uses port DBO 7 in place of the coil 3 current line.		
1111(F)		Check Reset	Resets all pending checks and brings up printer reset.	DQ090	1

Control Load Command

Channel

Sys Bus Out Low

8 11

Micro Instruction Function Field Decode

1 0 0 0 → 1 1 0

PH110

0 1 2

CBO

Data Buffer

4-7

Port DBO

DA 0-3

Device Address Hit

PH070

See μINSTR-30.

Select Attachment

Send Data Byte to Attachment
DBO 0-7

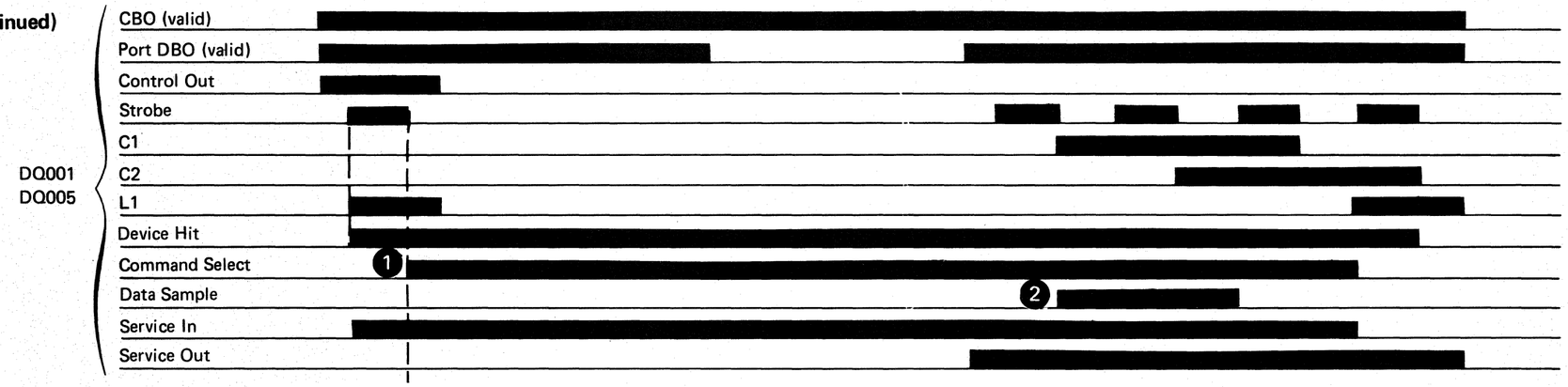
Mod 4-7

CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 1 0	0 0 0 0 Diagnostic Adapter Control*	Select Odd Scans	Select Even Scans	Reset Hammer Matrix	Force Motor Up-to-Speed	Turn Motor On	Drop 24V to Hammers	Printer Reset	Reset CE Latch
	0 0 0 1 Character Set Size		Character Set Size Code						
	0 0 1 0 Diagnostic Hammer Control*					Y8	Hammer Select Latch Y4	Y2	Y1
	0 1 0 0 Enable Adapter								
	0 1 0 1 Disable Adapter								
	1 0 0 0 Reset Scan Buffer Address**								
	1 0 0 1 Print and Space Control	Start Printing	Enable EOF Detect	Disable EOF Detect	Print Coming			Disable Forms Jam Detect	Enable Forms Jam Detect
	1 0 1 0 Special Functions		Set Diagnostic Print Busy	Reset Diagnostic Print Busy	Start Timer	Set Carriage Reverse***	Reset Carriage Reverse***		
	1 0 1 1 Carriage Space Counter		Set Space Counter Value						
	1 1 0 0 Diagnostic Carriage Control*		Carriage Go	Carriage Stop	Activate Paper Clamp	Deactivate Paper Clamp	End Carriage Space Time		
	1 1 0 1 Elapsed Time Counter		Set Elapsed Time Counter Value						

Bit 1	Bit 2	
0	0	48-Character Set
0	1	64-Character Set
1	0	96-Character Set
1	1	128-Character Set (Katakana)

*Diagnostic usage only.
**Not permitted when busy.
***Half Line Space Feature only.

Control Load Command (Continued)



Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
0000(0)	0	Diagnostic Adapter Control	Turns on the odd scans latch.	DQ110	
	1		Sets the odd scans latch off.	DQ110	
	2		Turns on the hammer matrix reset latch which resets the hammer fire circuitry.	DQ210	
	3		Turns on the belt start complete latch which brings up motor up-to-speed.	DQ220	2
	4		Turns on the belt go latch which allows the print belt motor to start up.	DQ220	
	5		Sets the coil check counter to 8, setting coil check on.	DQ090	
	6		Turns on the printer reset latch.	DQ090	
	7		Turns off the CE latch. The latch is turned on by attaching the input (set) to a desired test point.	DQ250	
0001(1)	0-1	Character Set Size	Depending on the condition of these 2 bits (on or off) the character set size is set in latches 0 and 1 (00 = 48, 01 = 64, 10 = 96, 11 = 128).	DQ190	2
0010(2)	4-7	Diagnostic Hammer Control	Allows the hammer select control value to be set to fire a certain hammer.	DQ290	2
0100(4)		Enable Adapter	Turns off the adapter reset latch.	DQ090	1
0101(5)		Disable Adapter	Turns on the adapter reset latch.	DQ090	1
1000(8)		Reset Scan Buffer Address	Resets the SBAR to 0.	DQ110	1
1001(9)	0	Print and Space Cycle Control	Turns on the start printing latch which initiates the printing sequence.	DQ110	
	1		Turns on the EOF enabled latch.	DQ210	
	2		Resets the EOF enabled latch.	DQ210	2
	3		Set odd(scan) latch, paper clamp, print belt go and ribbon go.	DQ220	
	6		Holds system sense byte 0, bit 0 off to prevent forms jam from being detected.	DQ210	
	7		Allows forms jam to be detected.	DQ210	
1010(A)	1	Special Functions	Turns on the diagnostic print busy latch.	DQ310	
	2		Turns off the diagnostic print busy latch.	DQ310	2
	3		Enables the elapsed time counter to be stepped by the 1 ms oscillator.	DQ300	
	4		Initiates a half line space operation.	FJ101	
	5		Resets a half line space operation.	FJ101	

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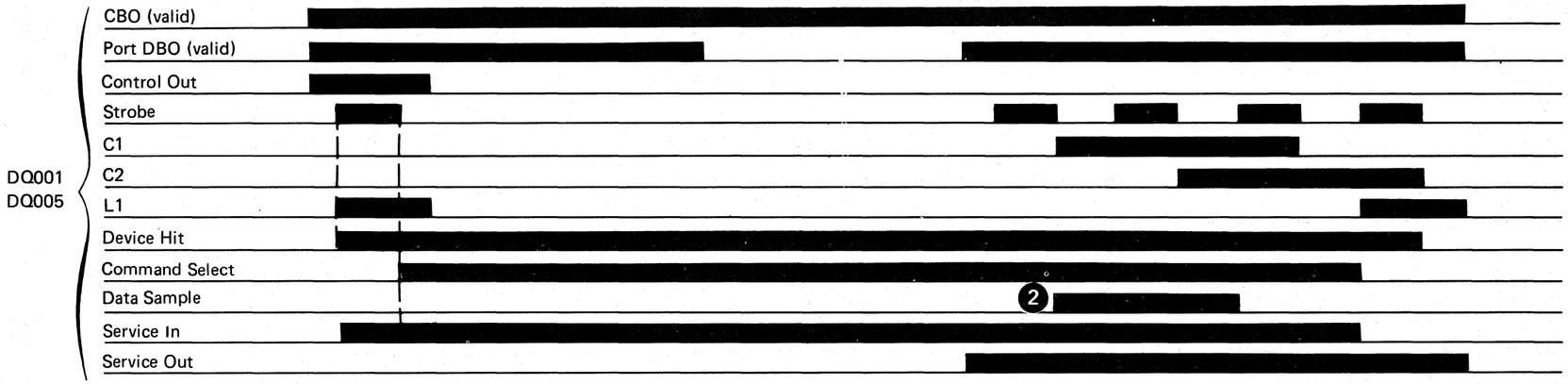
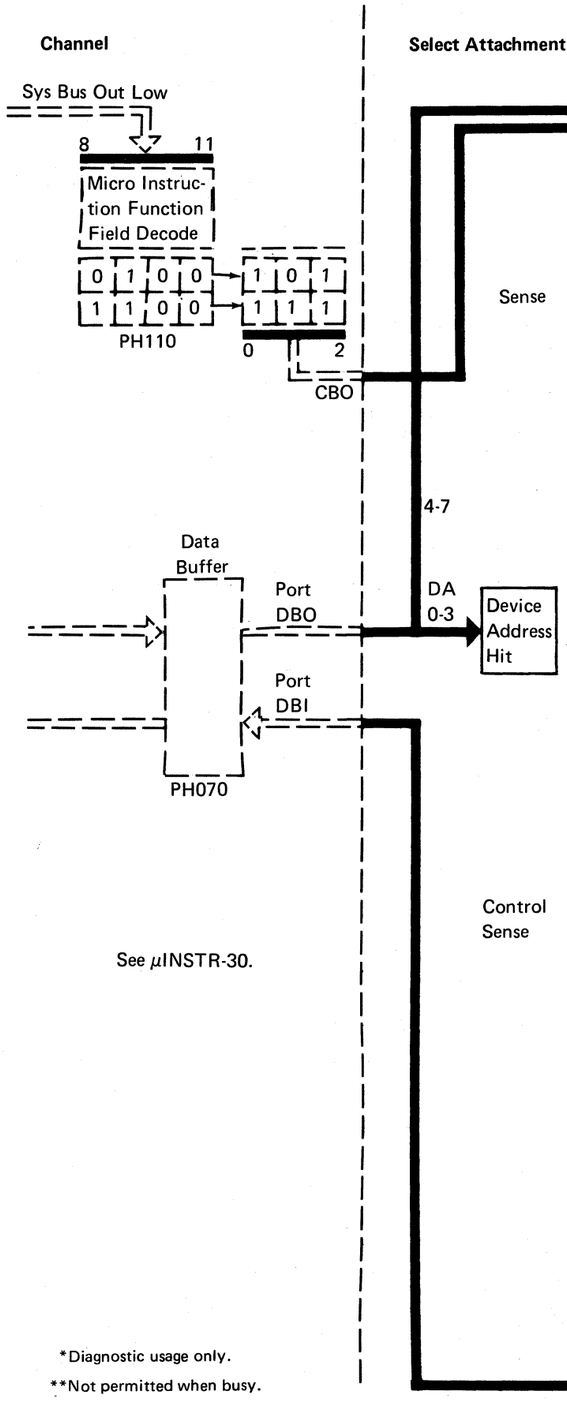
Control Load Command (Continued)



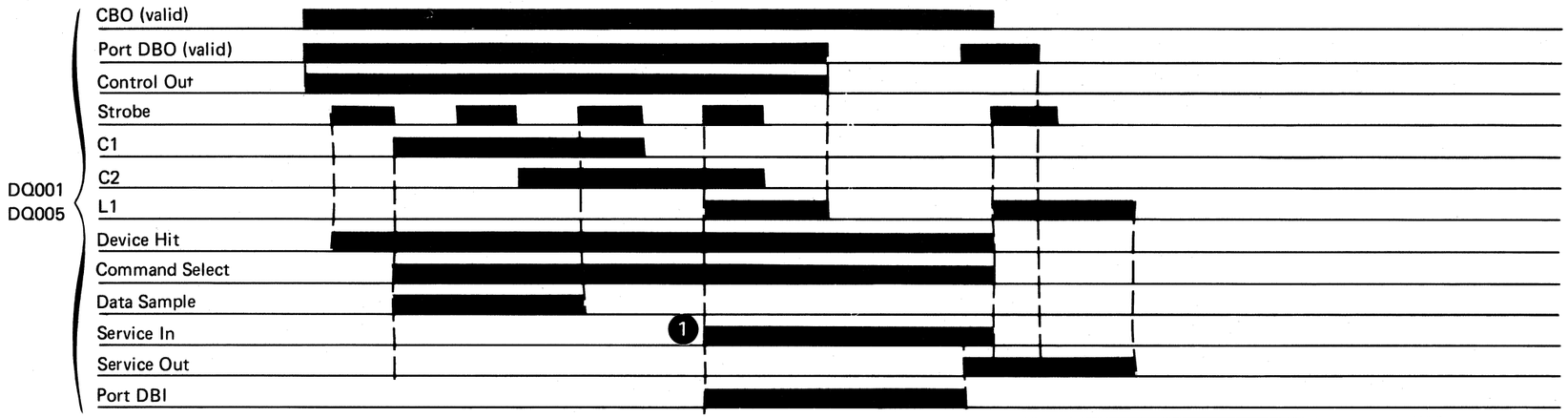
Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
1011(B)	0-7	Carriage Space Counter	Used to load the space counter with the data on port DBO.	DQ100	2
1100(C)	1 2 3 4 5	Diagnostic Carriage Control	Turns on the carriage go latch and the carriage busy latch (starting carriage motion). Turns off the carriage go latch. Turns on the activate clamp latch. Turns on the reset clamp active latch. Turns off the space time latch which ends a carriage operation.	DQ80 DQ80 DQ230 DQ230 DQ80	2
1101(D)	0-7	Elapsed Time Counter	Used to load the elapsed time counter with the data port DBO.	DQ300	2

Sense Command—Control Sense Command (285 lpm)



CCB 0 1 2	CCB 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 0 1	0 0 0 0 System Sense Byte 0	Forms Jam Check	Belt Speed Check	Carriage Sync Check	End of Forms	Throat Open	Coil Current Check	Belt Sync Check	Cover Open
	0 0 0 1 System Sense Byte 1	Coil 1 Parity Odd	Coil 2 Parity Odd	Coil 3 Parity Odd	Emitter Check	Buffer Data Check	Hammer Parity Check		
	0 1 1 0 Interrupt Condition				Print Busy Off	Carriage Busy Off			Elapsed Time Counter
	1 0 0 1** Print Buffer								
	1 0 1 1* Diagnostic Sense hex 00								
	1 1 0 0* Diagnostic Sense hex 55								
	1 1 0 1* Diagnostic Sense hex AA								
	1 1 1 0* Diagnostic Sense hex FE								
Control Sense 1 1 1	0 0 0 1 Diagnostic Clamp Status				Clamp On	Clamp Off			
	0 0 1 0* Diagnostic Inputs		Carriage Advance Pulses	CE Latch	Home	Belt Motion		Print Subscan Emitter	
	0 0 1 1** Belt Position								
	0 1 0 0* Diagnostic Wrap	Belt Go	Carriage Go	Printer Reset	Hammer Power On	Hammer Select Latch Feedback			
	0 1 0 1* Diagnostic Wrap	Paper Clamp	Hammer Select Strobe 1	Hammer Matrix Reset	Subscan 5	Subscan 4	Subscan 3	Subscan 2	Subscan 1
	0 1 1 0* Diagnostic Wrap	Stop Ribbon	Prepare Print Control	Adapter Reset	MCU Half Index Complete	MCU Half Index Mode	Coil Current Check		Hammer Select Strobe 2
	0 1 1 1* Diagnostic Sense Byte	1 ms Osc Off	131 ms Osc	System Reset Off	Power Fault	Hammer Duty Cycle Limit Off	Impression Singleshot		

Sense Command—Control Sense Command (285 lpm) — Continued



Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
0000(0)	0 1 2 3 4 5 6 7	System Sense Byte 0 (senses the condition of checks and interlocks).	Forms jam check. Belt speed check. Carriage sync check. End of forms (EOF). Throat closed. Coil (current) check. Belt sync check. Cover closed.	DQ210 DQ220 DQ080 DQ210 ZZ320 DQ090 DQ190 DQ220	1
0001(1)	0 1 2 3 4 5	System Sense Byte 1	Senses the condition of the coil 1 line. Senses the condition of the coil 2 line. Senses the condition of the coil 3 line. Senses the condition of the emitter check latch. Senses the condition of the buffer data check latch. Senses the condition of the hammer parity check latch.	DQ090 DQ090 DQ090 DQ260 DQ170 DQ100	1
0110(6)	3 4 5	Interrupt Condition	Sets port DBI bit 3 when the print busy latch is off. Sets port DBI bit 4 when the carriage busy latch is off. Sets port DBI bit 5 when the 'elapsed time counter is zero' line is active.	DQ110 DQ080 DQ300	1
1001(9)	0-7	Print Buffer	Gates the output of the print buffer to the channel on port DBI.	DQ180	1
1011(B)	0-7	Diagnostic Sense hex 00	Gates hex 00 to the channel on port DBI to check for no bits on.	DQ050, DQ060	1
1100(C)	0-7	Diagnostic Sense hex 55	Gates hex 55 to the channel on port DBI to check for alternate bits on.	DQ050, DQ060	1
1101(D)	0-7	Diagnostic Sense hex AA	Gates hex AA to the channel on port DBI to check opposite bits from 55.	DQ050, DQ060	1
1110(E)	0-7	Diagnostic Sense hex FE	Gates hex FE to the channel on port DBI to check for parity bit on.	DQ050, DQ060	1

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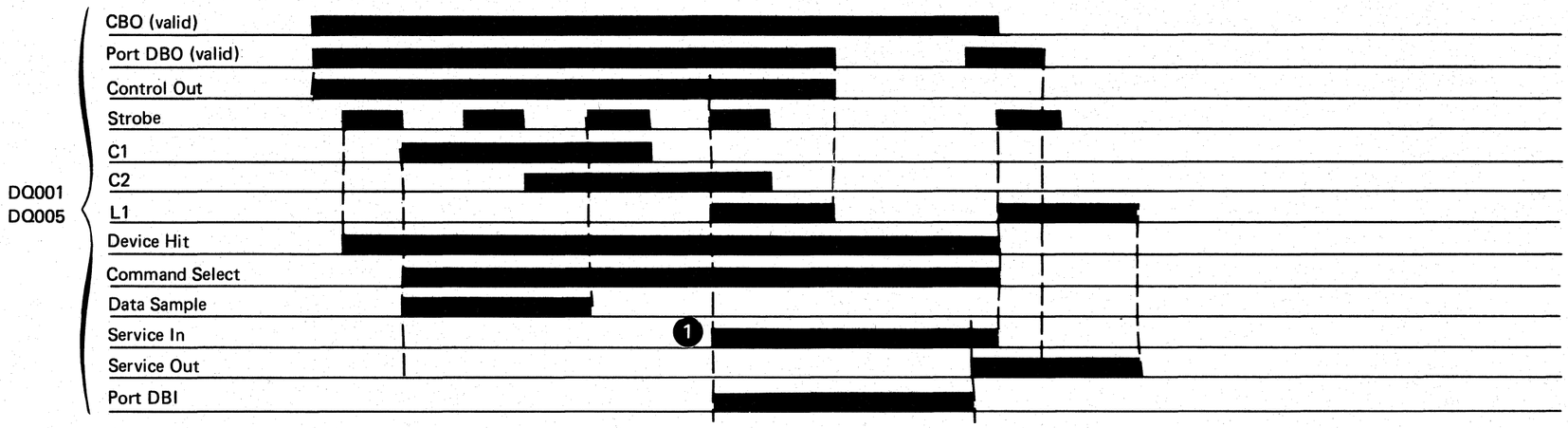
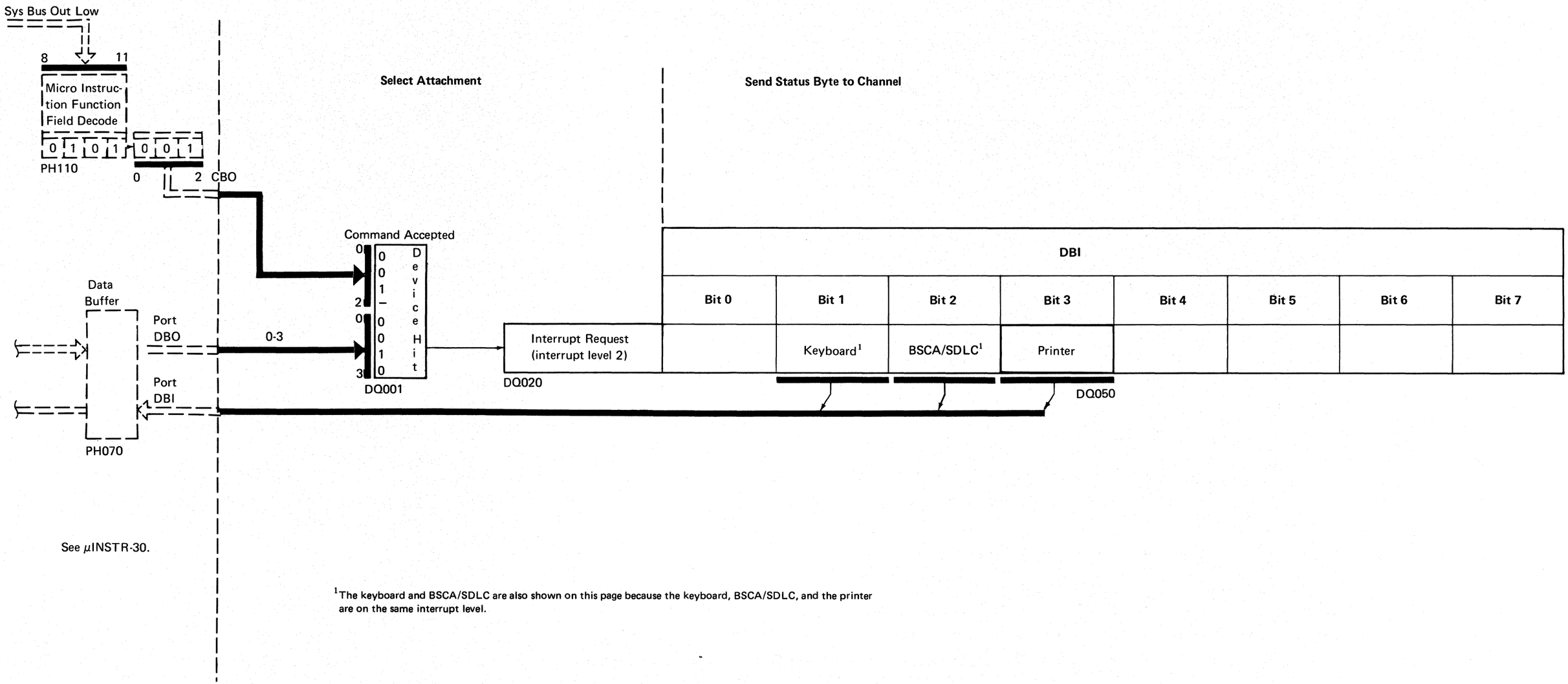


Modifier Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action Taken	FEALD Page	Timing
0001(1)	3 4	Diagnostic Clamp Status	Turns on port DBI bit 3 if the clamp on latch is on. Turns on port DBI bit 4 if the clamp off latch is on.	DQ240 DQ240	1
0010(2)	1 2 3 4 6	Diagnostic Inputs	Turns on port DBI bit 1 when the carriage advance line is active. Turns on port DBI bit 2 if the CE latch is on. Turns on port DBI bit 3 when the home line is active. Turns on port DBI bit 4 when the belt motion line is active. Turns on port DBI bit 6 when the print subscan line is active.	ZZ581 DQ250 DQ210 ZZ581 DQ200	1
0011(3)	0-7	Belt Position	Sends value of the belt position counter through the scan key to the channel on port DBI.	DQ200	1
0100(4)	0 1 2 3 4-7	Diagnostic Wrap	Turns on port DBI bit 0 when the belt go latch is on. Turns on port DBI bit 1 when the carriage go latch is on. Turns on port DBI bit 2 if the printer reset latch is on. Turns on port DBI bit 3 when the hammer fault line is active. Sends the Y hammer select line values to the channel on port data in.	DQ220 DQ080 DQ090 DQ090 DQ290	1
0101(5)	0 1 2 3-7	Diagnostic Wrap	Turns on port DBI bit 0 when the clamp latch is on. Turns on port DBI bit 1 when the hammer select strobe line is active. Turns on port DBI bit 2 when the hammer matrix reset line is active. Turns on corresponding port DBI bits when the subscan lines 5-1 are active.	DQ240 DQ140 DQ210 DQ200	1
0110(6)	0 1 2 5	Diagnostic Wrap	Turns on port DBI bit 0 when the stop ribbon line is active. Turns on port DBI bit 1 if the prepare print control latch is on. Turns on port DBI bit 2 if the adapter reset latch is on. Turns on port DBI bit 5 if the coil (current) check counter output is active.	DQ220 DQ110 DQ090 DQ090	1
0111(7)	0 1 2 3 4 5	Diagnostic Sense Byte	Turns on port DBI bit 0 when the 1 ms oscillator output is active. Turns on port DBI bit 1 when the 131 ms oscillator output is active. Turns on port DBI bit 2 when the system reset line is active. Turns on port DBI bit 3 when the power fault line is active. Turns on port DBI bit 4 when the hammer duty cycle limit line is active. Turns on port DBI bit 5 when the impression singleshot is active.	PJ070 PJ070 PN060 DQ050 DT010 ZZ581	1

Sense Interrupt Level Status Command



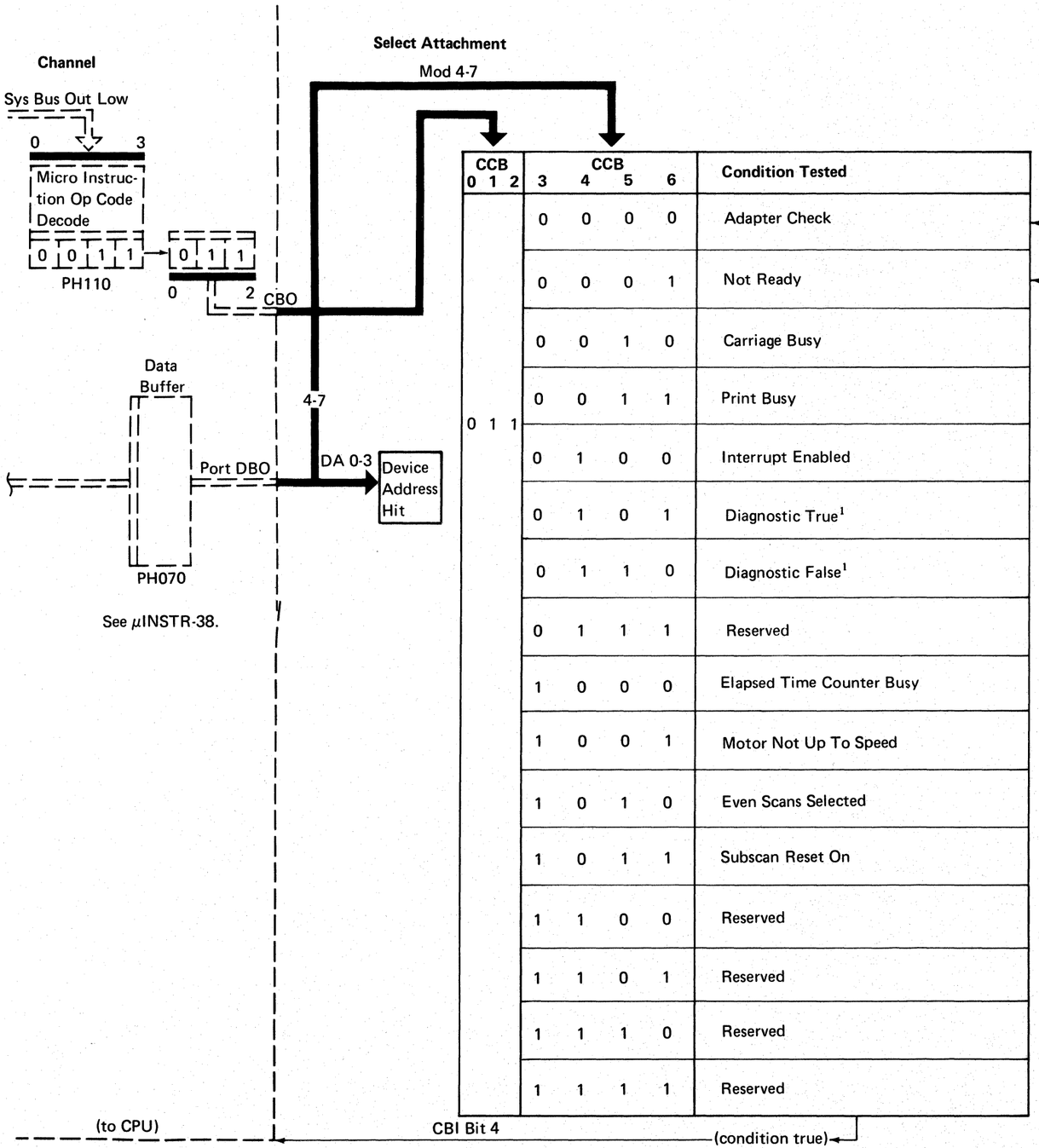
See μINSTR-30.

[1]The keyboard and BSCA/SDLC are also shown on this page because the keyboard, BSCA/SDLC, and the printer are on the same interrupt level.

Sense Interrupt Level Status Command (Continued)

Modifier Port DBO	Port DBI Interrupt Bit	Command	Action Taken	FEALD Page	Timing
0010(2)	3	Sense Interrupt Level	If an interrupt request is pending, port data in bit 3 (interrupt request) is sent to CPU.	DQ050	1

Jump I/O Command



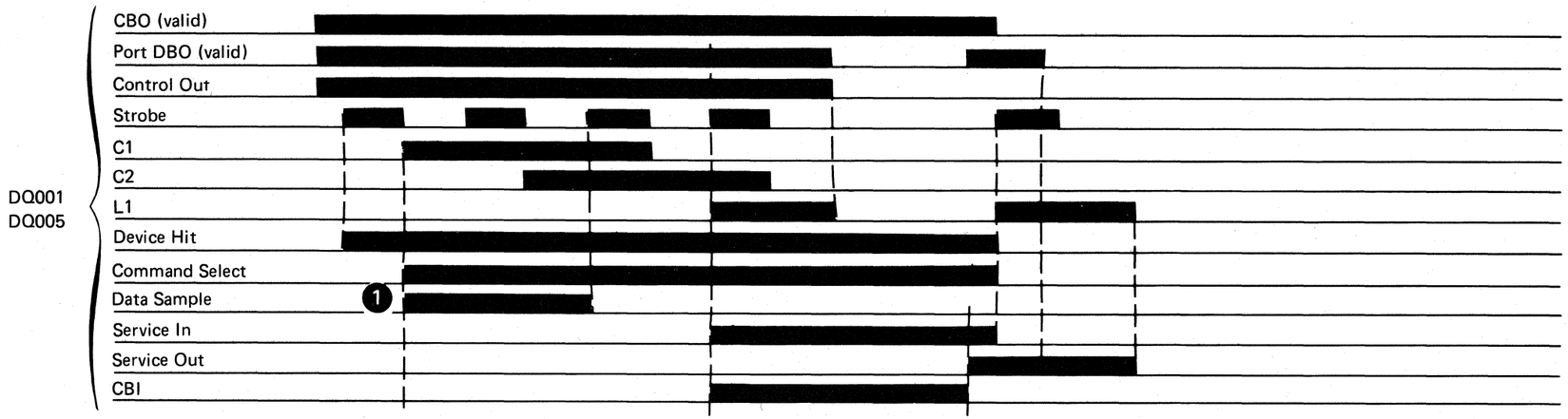
CCB 0 1 2	CCB 3 4 5 6	Condition Tested
0 1 1	0 0 0 0	Adapter Check
	0 0 0 1	Not Ready
	0 0 1 0	Carriage Busy
	0 0 1 1	Print Busy
	0 1 0 0	Interrupt Enabled
	0 1 0 1	Diagnostic True[1]
	0 1 1 0	Diagnostic False[1]
	0 1 1 1	Reserved
	1 0 0 0	Elapsed Time Counter Busy
	1 0 0 1	Motor Not Up To Speed
	1 0 1 0	Even Scans Selected
	1 0 1 1	Subscan Reset On
	1 1 0 0	Reserved
	1 1 0 1	Reserved
	1 1 1 0	Reserved
	1 1 1 1	Reserved

Forms jam
Belt speed check
Carriage sync check
Coil current check
Belt sync check
Emitter check
Buffer data check
Hammer parity check

End of forms
Throat open
Cover open

[1] Diagnostic usage only.

Jump I/O Command (Continued)



Modifier Port DBO 4, 5, 6, 7 (Hex)	Command	Action Taken	FEALD Page	Timing
0000(0)	Adapter Check	Turns on CBI bit 4 if any of the indicated check conditions are active.	DQ070	1
0001(1)	Not Ready	Turns on CBI bit 4 if any of the indicated interlock conditions are active.	DQ070	1
0010(2)	Carriage Busy	Allows a branch (CBI bit 4 on) if the carriage busy latch is on.	DQ080	1
0011(3)	Print Busy	Allows a branch (CBI bit 4 on) if the print busy line is active.	DQ110	1
0100(4)	Interrupt Enabled	Branches if one or more of the following latches are on: – Interrupt print op end. – Interrupt carriage op end. – Interrupt elapsed 0.	DQ270	1
0101(5)	Diagnostic True	Turns on CBI bit 4 to check that the bit actually turns on when expected.	DQ070	1
0110(6)	Diagnostic False	Turns on no latches to be sure that the CBI bit 4 does not turn on except when tested conditions are met.	DQ070	1
1000(8)	Elapsed Time Counter Busy	Turns on CBI bit 4 when the elapsed time counter 0 line is inactive.	DQ300	1
1001(9)	Motor Not Up To Speed	Branches when the motor up-to-speed line is inactive.	DQ260	1
1010(A)	Even Scans Selected	Branches when the odd latch (odd scans) is on.	DQ110	1
1011(B)	Subscan Reset On	Branches if the subscan reset latch is on.	DQ200	1

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Paper Clamps DQ240

There are two clamps in the printer. The upper paper clamp, although it clamps the paper, is used for noise suppression only. When the clamp solenoid is energized, it closes the air gap the paper passes through. This reduces the noise level at the back of the printer by dampening the paper noise.

The second paper clamp (lower) is just below the print line. The purpose of this clamp is to prevent horizontal skewing of the paper. The type belt is continuously turning and has a tendency to pull the paper along with it. Since there are no feed rolls in the lower portion of the printer, the paper clamp is necessary to hold the paper in position.

1 For diagnostic purposes, the activate clamp command A is issued to turn on the paper clamps. This command sets the 'activate clamp' latch (DQ240) which turns on the paper clamp solenoids. The 'activate clamp' latch also resets the 'clamp off' latch and gates the 'clamp on' latch to be set by the paper clamp timer. The 'clamp on' latch is set after the paper clamp timer has counted 15 μs.

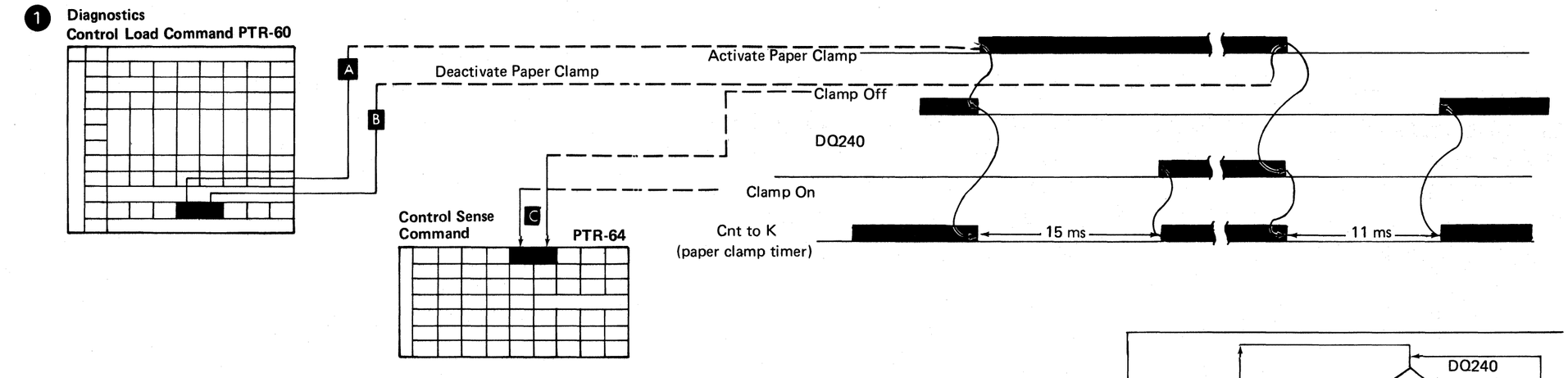
A similar operation is used to turn the clamps off. A deactivate clamp command B resets the 'activate clamp' latch. This in turn resets the 'clamp on' latch and gates the 'clamp off' latch to be set by the paper clamp timer. The 'clamp off' latch is set after the paper clamp timer has counted 11 μs.

The 'clamp on' and 'clamp off' latches signal that enough time has elapsed to complete their respective operations. There is no check to see if the clamp solenoids are actually energized or not.

The 'clamp on' and 'clamp off' latches can be sensed C

2 During a normal print operation, IOCL print coming active D activates the paper clamps and 'print busy' going inactive E turns off the paper clamp.

The above timing chart applies to both diagnostic and normal clamp control.



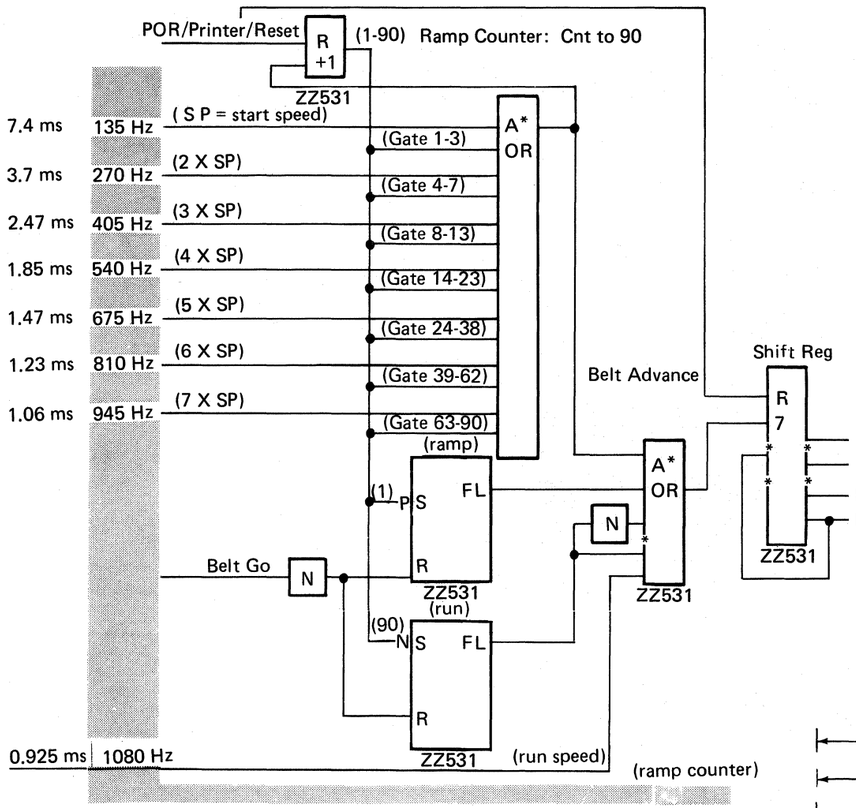
Type Belt Start and Run (285 lpm)

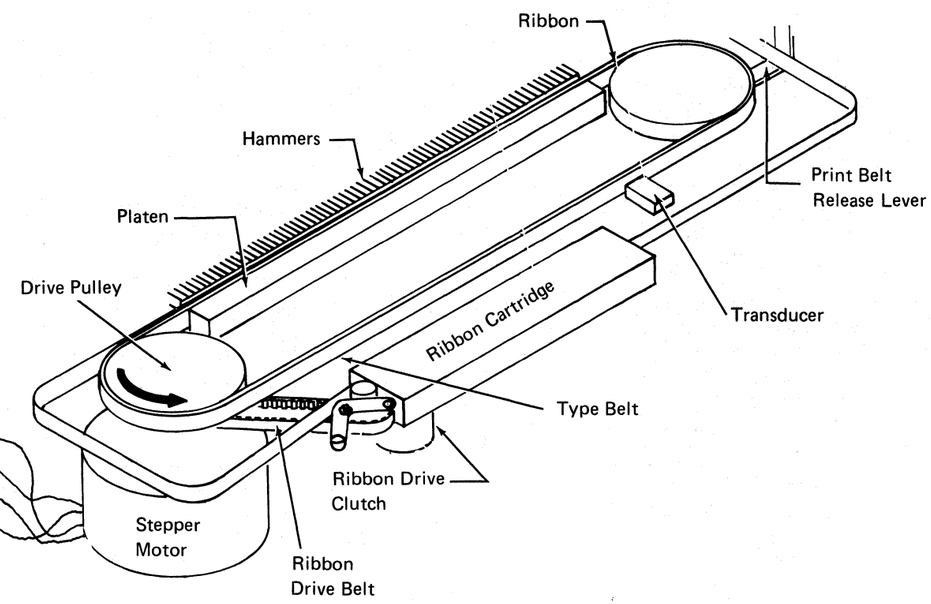
The type belt is directly driven by a stepper motor mounted under the left pulley. The right pulley has a release lever mounted on it to remove tension from the type belt. When the release lever is operated, the type belt can be removed.

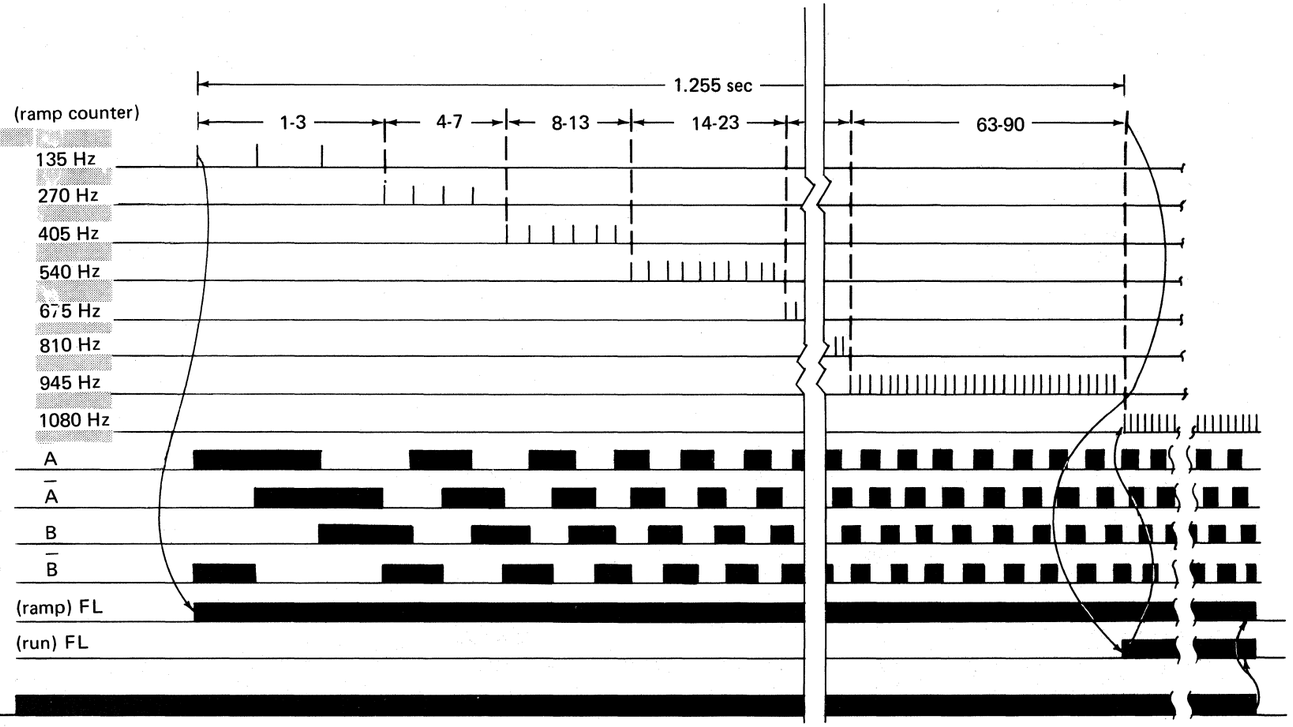
After POR, the count to 90 (ramp counter) runs continuously. When belt go is activated, there is a delay of 533 ms. Then belt drive A and belt drive B are turned on for 382 ms which locks the motor. After the 382 ms motor locks, the first count of 1 turns on the ramp latch which allows the belt advance pulse to shift the shift register. The output of the shift register causes the type belt stepper motor to start accelerating.

The first three drive pulses are 135 Hz, the next four at 270 Hz, five at 405 Hz, etc. This ramping sequence continues until a count of 90 is reached. At the fall of count 90, the run latch is set. The run latch blocks the ramp drive pulses and allows the shift register to be driven by 1080 Hz (run frequency). The type belt stepper motor is now up to full operating speed and remains at this speed until belt go is deactivated.

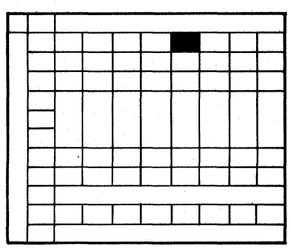
Note: Dual ramping card values are 70 percent of the values shown, until '—Belt Motion' is active.



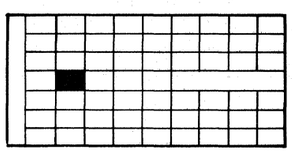




Control Load Command PTR-60



Control Sense Command PTR-64



Belt Go → After the rise of belt go, there is a delay of 533 ms maximum. Then belt drive A and belt drive B are turned on for 382 ms and lock the motor. The advance pulses then start and the motor starts to run.

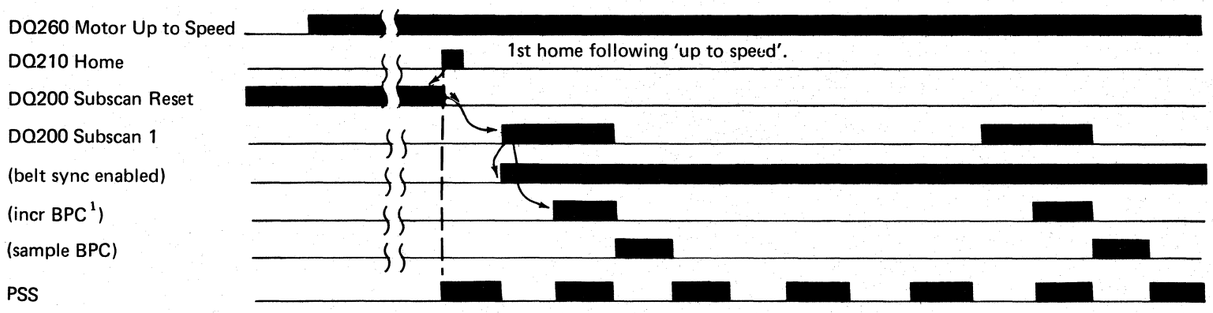
Type Belt Sync Timing

After the type belt has reached an up-to-speed condition, the sensing of the timing marks on the type belt is started. The first home pulse after up-to-speed turns off subscan reset and allows the BPC (belt position counter) and the subscan counter to start stepping. This synchronizes the stepping of the BPC and the subscan counter. When subscan 1 comes up, the belt sync enabled latch is turned on. The next PSS pulse after subscan 1 increments the BPC.

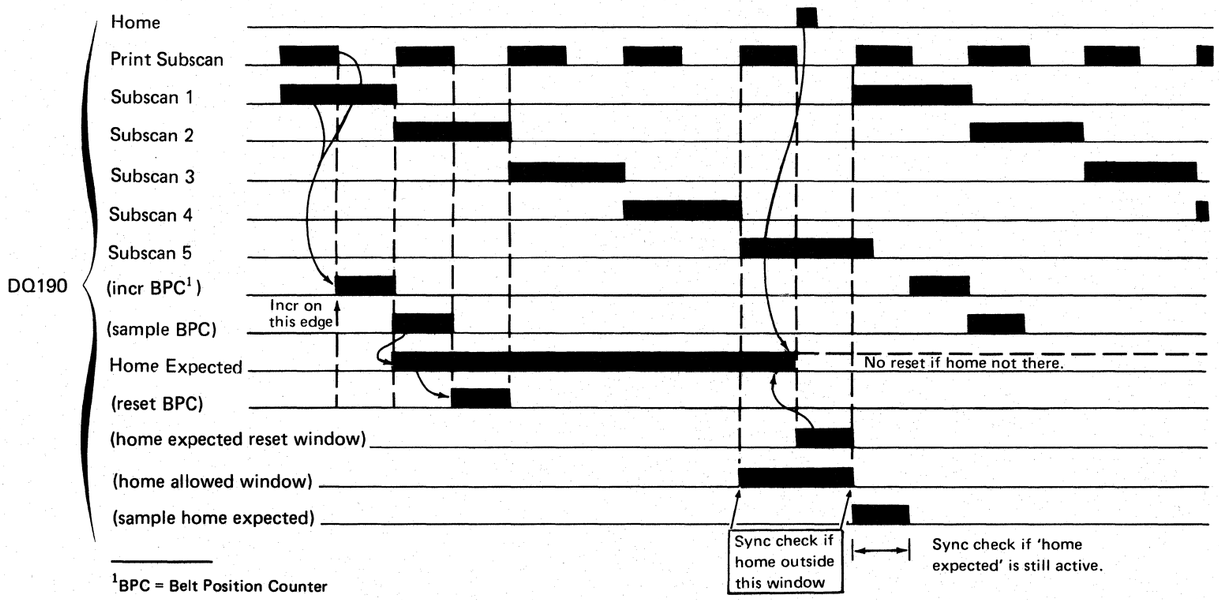
The BPC and the subscan counter are synchronized with each other by the home pulse. Once the home pulse has been received, the BPC and the subscan counter are allowed to continue stepping. Synchronism continues to be verified by the home pulse. If a home pulse occurs when not expected or fails to occur when expected, the belt sync check is set.

The print buffer contains PFN (print fire numbers) that indicate the print scan on which a position is printed. The BPC contains the number of the current print scan and the subscan counter selects the hammers to be optioned within each print scan. In this manner, the characters to be printed are synchronized with the characters on the type belt.

Initiating the Belt Sync Timing Sequence

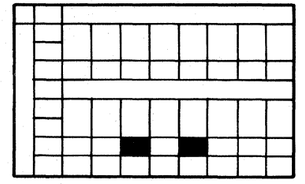


Type Belt Sync Timing

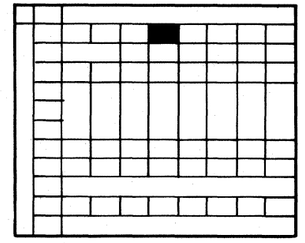


[1]BPC = Belt Position Counter

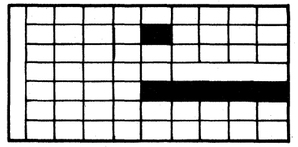
Load Command PTR-58



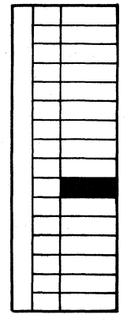
Control Load Command PTR-60



Control Sense Command PTR-64



Jump I/O Command PTR-70



Ribbon Drive/Type Belt Transducer (285 lpm)

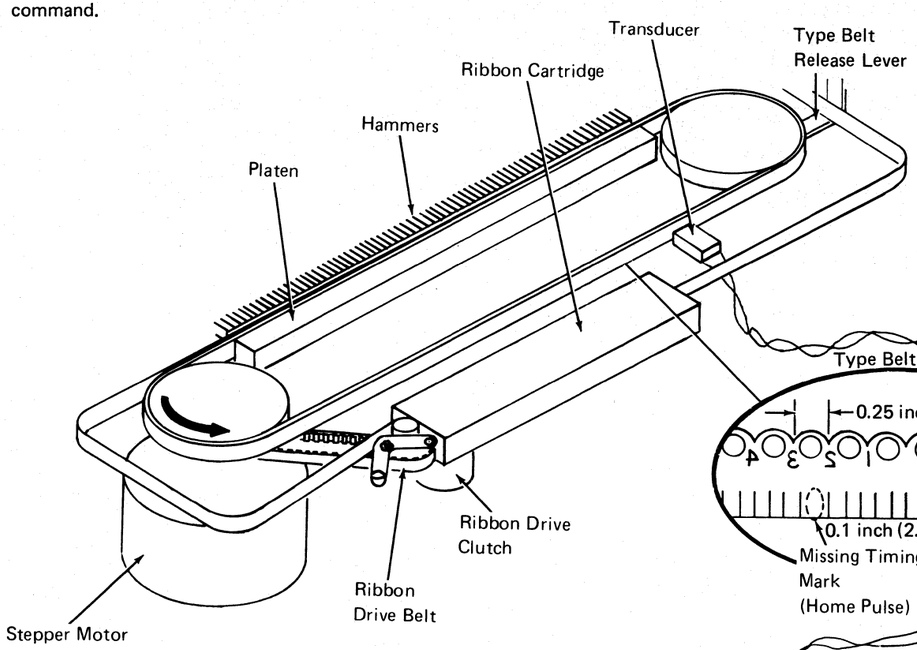
Ribbon Drive

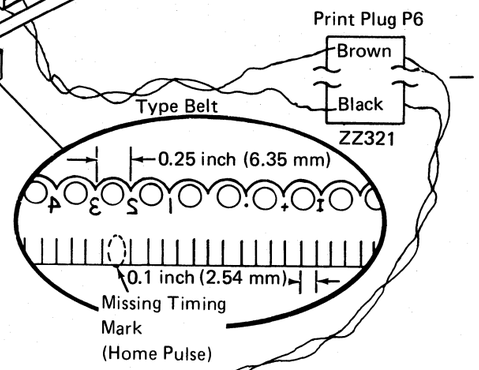
The ribbon is driven by a belt mounted on the type belt drive pulley. The drive mechanism also includes a solenoid-driven clutch to disengage the drive from the ribbon when no printing is taking place. The disengaging of the clutch prevents smudging of the paper while the printer is idle. This is under control of the printer control card, and happens five seconds after the last print command.

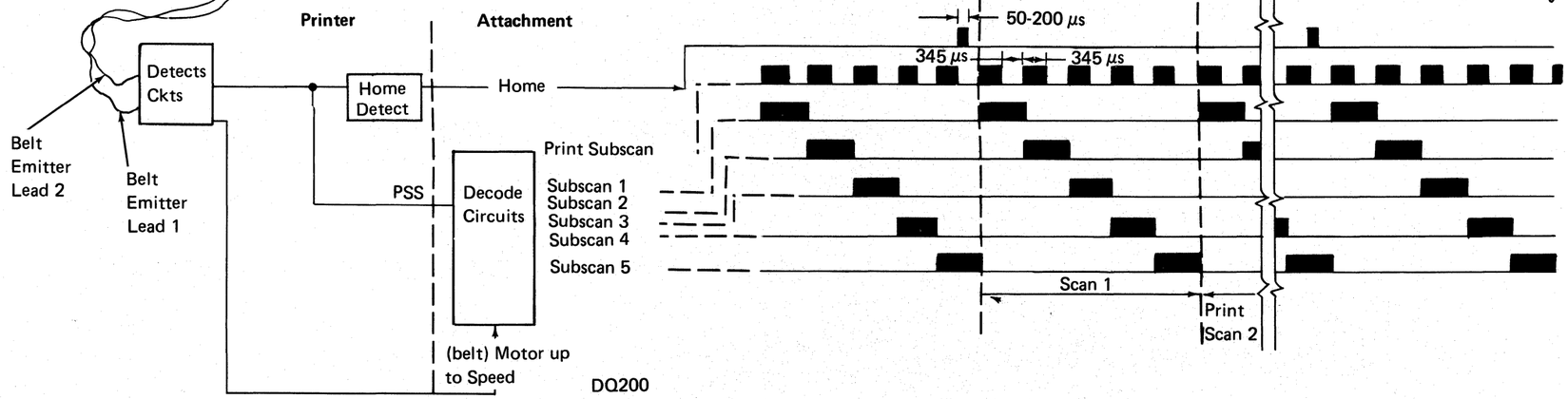
The ribbon is a continuous 1/2 inch wide fabric ribbon contained in a cartridge mounted on the front of the printer. The ribbon is fed into the left side of this cartridge and pulled out the right side (as viewed from the front of the machine).

Type Belt Transducer

The type belt transducer detects the raised timing marks on the type belt. These marks are converted to emitter pulses in the transducer and sent to the control card. The control card uses these pulses to generate the home pulse, subscan pulses, and the belt up-to-speed signal. The home pulse and subscan pulses are used to synchronize the mechanical and electrical portions of the print operation. The belt up-to-speed signal is sent to the attachment to indicate that the type belt is up to operating speed.





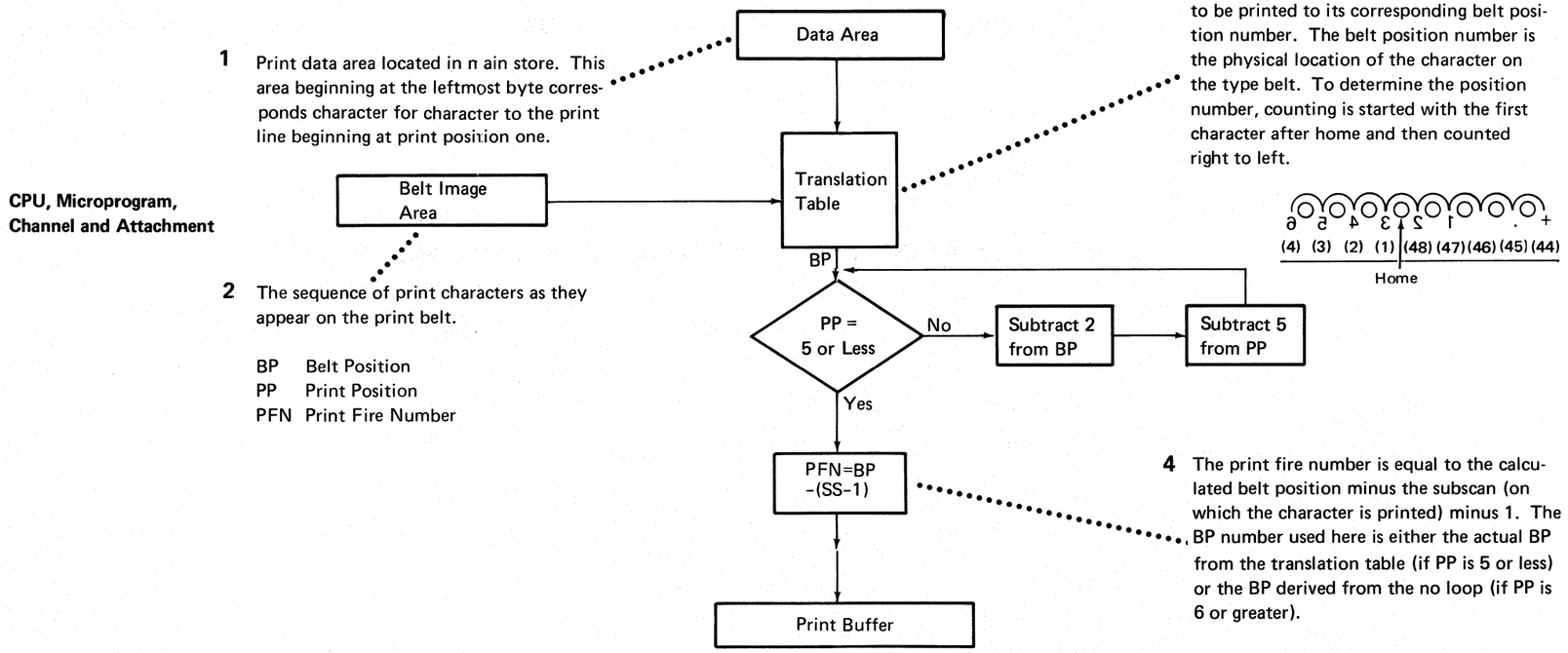


Print Buffer Load DQ180 (285 lpm)

The print buffer is loaded by a print buffer load command, 1 byte per command. The data is in the form of PFN (print fire numbers) rather than actual print image data. The flowchart at the right shows how the value of the PFN is determined.

Prior to loading the buffer the SBAR is reset to zero by a reset scan buffer address control load command. Issuing of the print buffer load command gates the DBO data to the print buffer. It also brings up the 'incr bfr adr' lines; which steps the SBAR, and 'write select' line which gates data into the print buffer when it is active. The print buffer load command ANDed with 'data sample' brings up 'ram clock strobe' which sets the data into the print buffer.

The SBAR is then incremented to the next print buffer position (as shown below). If that position is to be written, another print buffer load command must be issued to load it.



1 Print data area located in n ain store. This area beginning at the leftmost byte corresponds character for character to the print line beginning at print position one.

2 The sequence of print characters as they appear on the print belt.

BP Belt Position
PP Print Position
PFN Print Fire Number

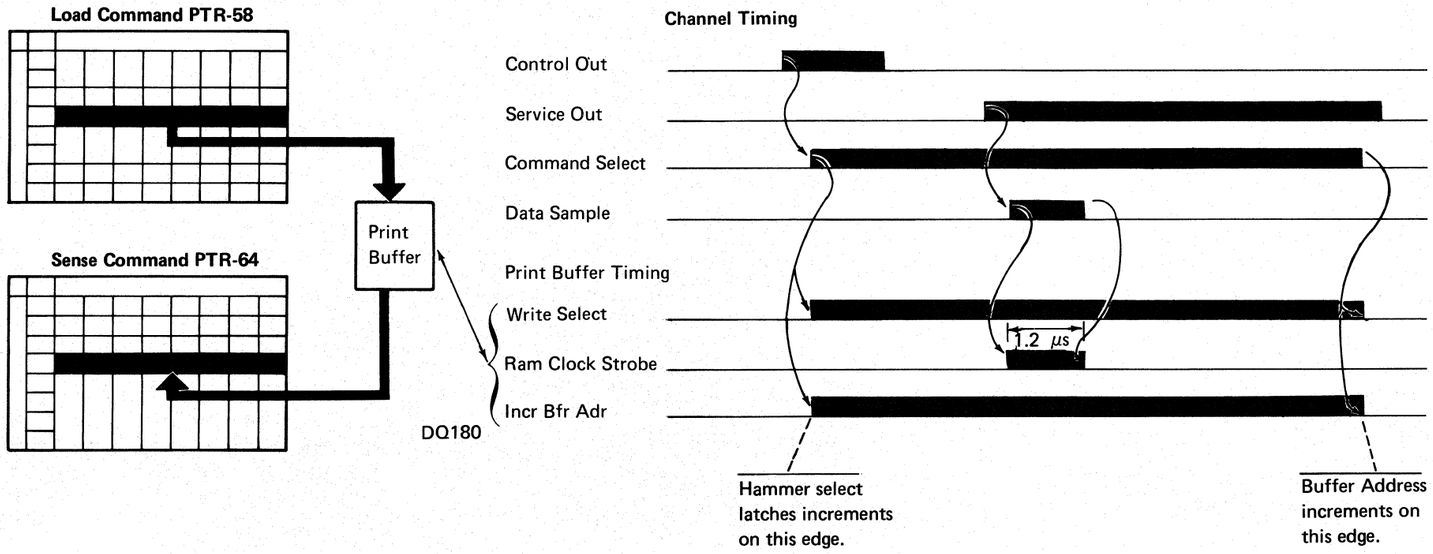
3 The translation table converts the character to be printed to its corresponding belt position number. The belt position number is the physical location of the character on the type belt. To determine the position number, counting is started with the first character after home and then counted right to left.

4 The print fire number is equal to the calculated belt position minus the subscan (on which the character is printed) minus 1. The BP number used here is either the actual BP from the translation table (if PP is 5 or less) or the BP derived from the no loop (if PP is 6 or greater).

If the last digit of PP =	subscan =
1 or 6	1
3 or 8	2
5 or 0	3
2 or 7	4
4 or 9	5

5 The print buffer contains the sorted print fire numbers (PFN). They are sorted into the sequence in which they are addressed.

Print Buffer	PP
0	1
1	6
2	11
3	16
etc.	

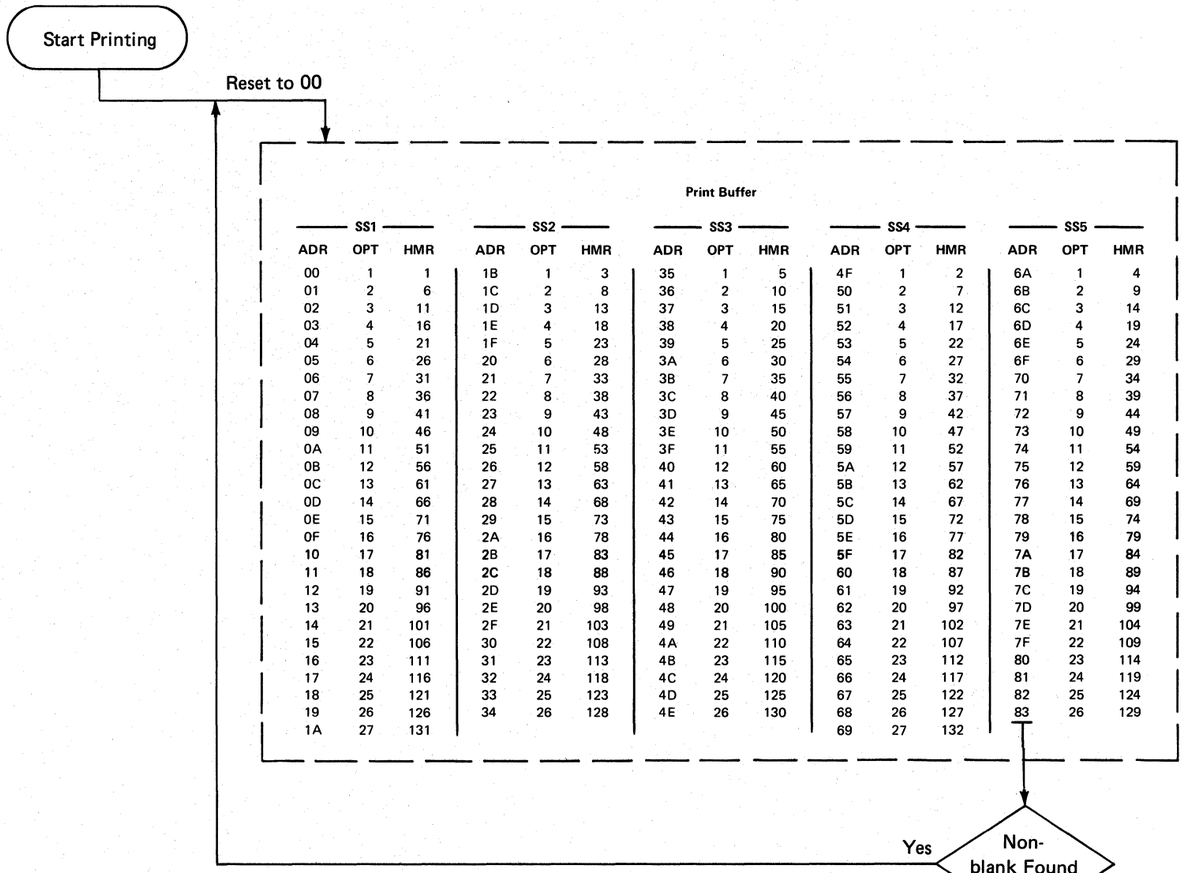


Print Buffer Read DQ180 (285 lpm)

To start reading from the print buffer, a start printing command must be issued and write select must be inactive (indicating read select active). The 'ram clock strobe' line is used to read out the data.

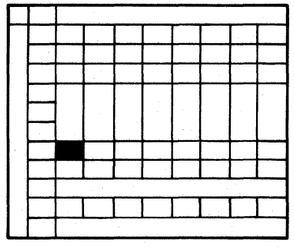
The data is then compared with the value of the scan register and checked for equal or not equal. If not equal, SBAR is incremented to the next buffer position and the above sequence is repeated. If equal, 'hammer select strobe' and 'write select' are activated. 'Hammer select strobe' fires the hammer being addressed and 'write select' allows a hex FF to be written, blanking the buffer position being addressed. SBAR is then incremented to the next buffer position.

When the end of the scan is reached (hex 83), the nonblank found latch is checked. If it was set by a valid buffer character, SBAR is reset to the starting address (hex 00) of the buffer. If the nonblank found latch was not set (no valid characters in the buffer), the end of superscan is set.

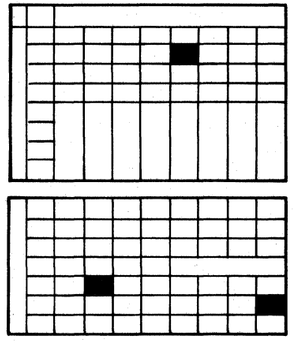


SS1			SS2			SS3			SS4			SS5		
ADR	OPT	HMR	ADR	OPT	HMR	ADR	OPT	HMR	ADR	OPT	HMR	ADR	OPT	HMR
00	1	1	1B	1	3	35	1	5	4F	1	2	6A	1	4
01	2	6	1C	2	8	36	2	10	50	2	7	6B	2	9
02	3	11	1D	3	13	37	3	15	51	3	12	6C	3	14
03	4	16	1E	4	18	38	4	20	52	4	17	6D	4	19
04	5	21	1F	5	23	39	5	25	53	5	22	6E	5	24
05	6	26	20	6	28	3A	6	30	54	6	27	6F	6	29
06	7	31	21	7	33	3B	7	35	55	7	32	70	7	34
07	8	36	22	8	38	3C	8	40	56	8	37	71	8	39
08	9	41	23	9	43	3D	9	45	57	9	42	72	9	44
09	10	46	24	10	48	3E	10	50	58	10	47	73	10	49
0A	11	51	25	11	53	3F	11	55	59	11	52	74	11	54
0B	12	56	26	12	58	40	12	60	5A	12	57	75	12	59
0C	13	61	27	13	63	41	13	65	5B	13	62	76	13	64
0D	14	66	28	14	68	42	14	70	5C	14	67	77	14	69
0E	15	71	29	15	73	43	15	75	5D	15	72	78	15	74
0F	16	76	2A	16	78	44	16	80	5E	16	77	79	16	79
10	17	81	2B	17	83	45	17	85	5F	17	82	7A	17	84
11	18	86	2C	18	88	46	18	90	60	18	87	7B	18	89
12	19	91	2D	19	93	47	19	95	61	19	92	7C	19	94
13	20	96	2E	20	98	48	20	100	62	20	97	7D	20	99
14	21	101	2F	21	103	49	21	105	63	21	102	7E	21	104
15	22	106	30	22	108	4A	22	110	64	22	107	7F	22	109
16	23	111	31	23	113	4B	23	115	65	23	112	80	23	114
17	24	116	32	24	118	4C	24	120	66	24	117	81	24	119
18	25	121	33	25	123	4D	25	125	67	25	122	82	25	124
19	26	126	34	26	128	4E	26	130	68	26	127	83	26	129
1A	27	131							69	27	132			

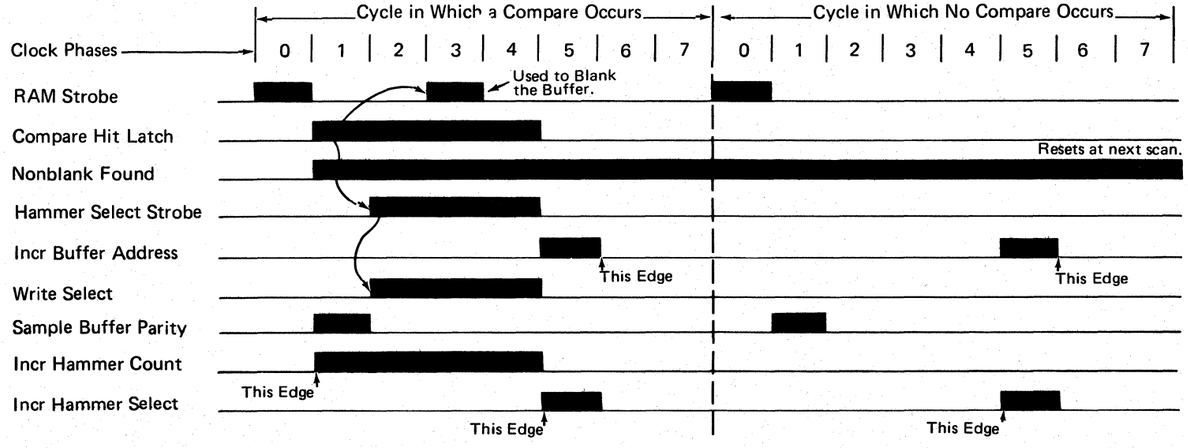
Control Load Command PTR-60



Sense Control Sense Command PTR-64



Typical Cycles During Hammer Optioning

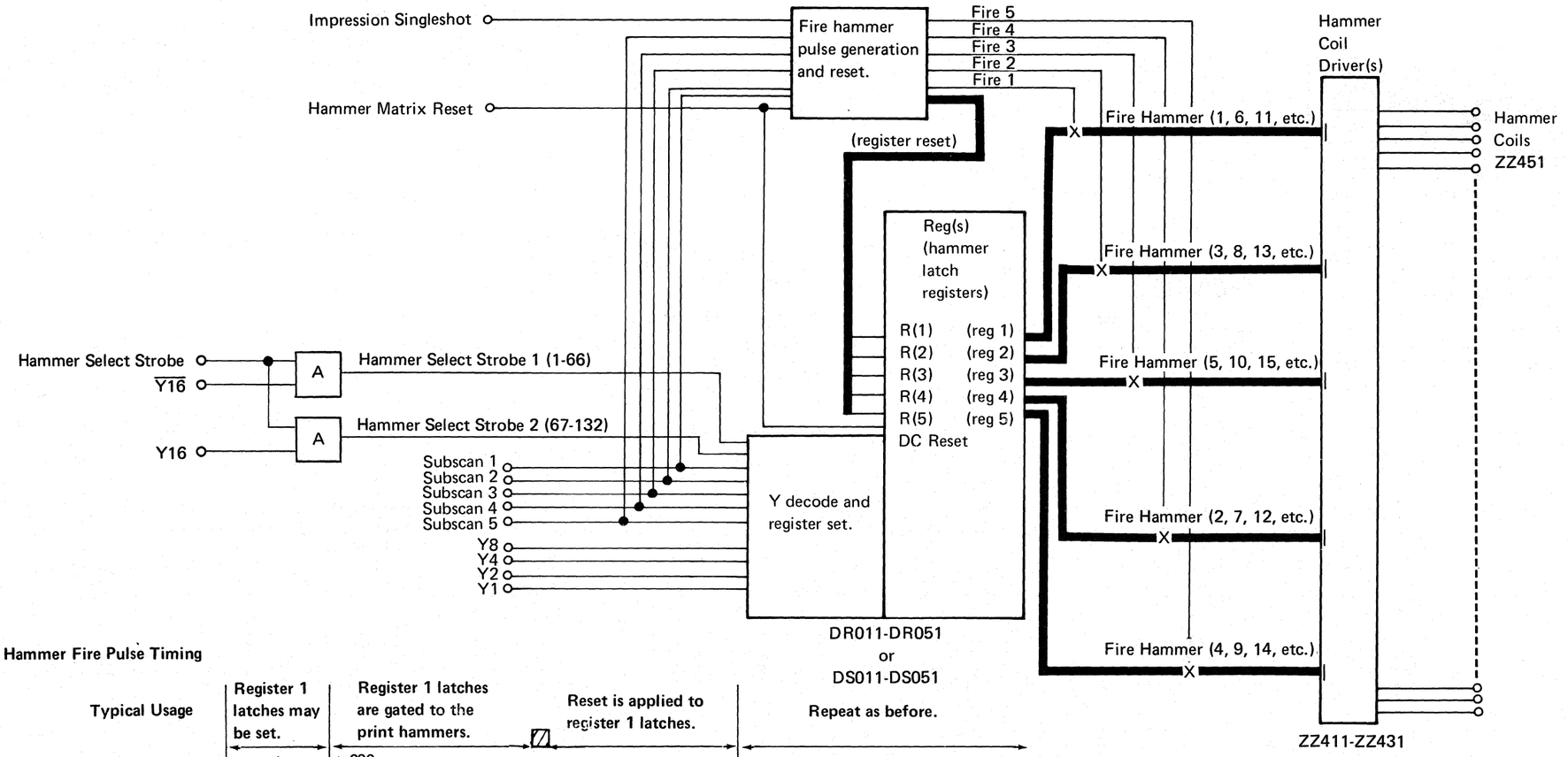


(Incr buffer address is the active line used.)

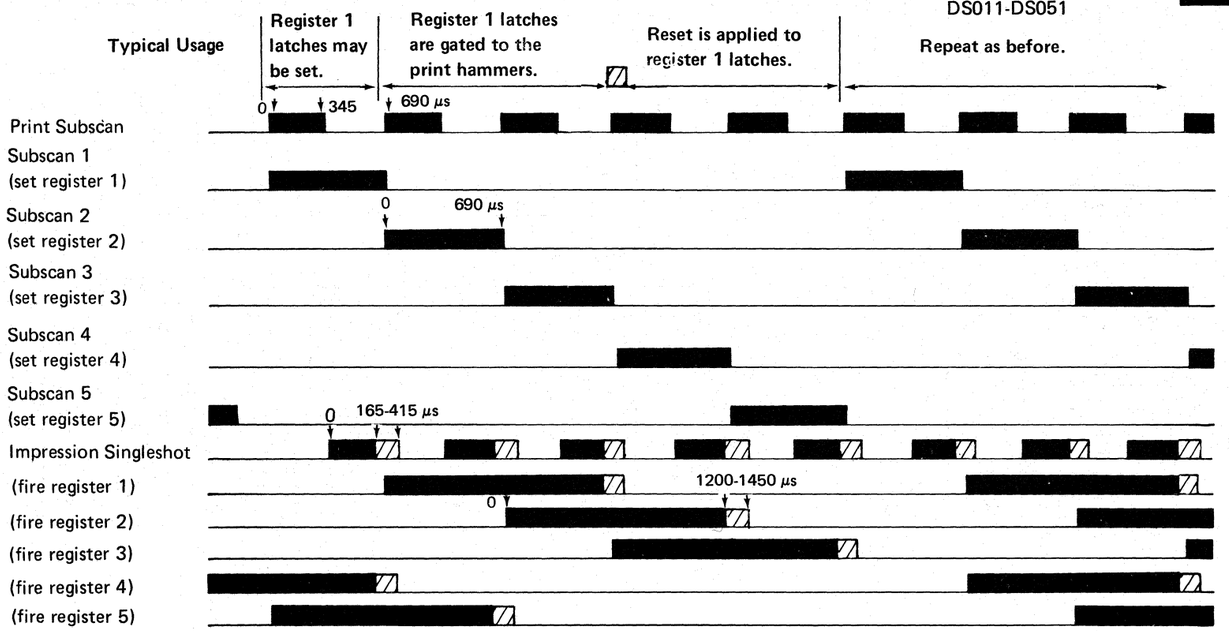
Hammer Selection and Firing (285 lpm)

During subscans 1 and 4, the Y lines are stepped from 1 to 27 to address all the hammer latches in regs 1 and 4 respectively. During subscans 2, 3, and 5, the Y lines are stepped from 1 to 26 to address all the hammer lattches in regs 2, 3, and 5 respectively. If any optioned hammers are to be fired (scan/buffer equal), they are set into the hammer latches by the 'hammer select strobe' line.

Once a hammer has been set to fire, it is actually fired by the fire pulses. These pulses occur one subscan after the hammer latch registers have been set, that is, a hammer set on subscan 1 is fired on subscan 2. The fire pulses are set by the subscan pulse and reset after two impression singleshot pulses. If the impression singleshot does not become active, the fire pulse stays on until the coil current check is activated. The setting of the impression singleshot determines the duration of the fire pulse.



Hammer Fire Pulse Timing



Hammer Selection and Firing (285 lpm) — Continued

Hammer Latch Select (285 lpm)

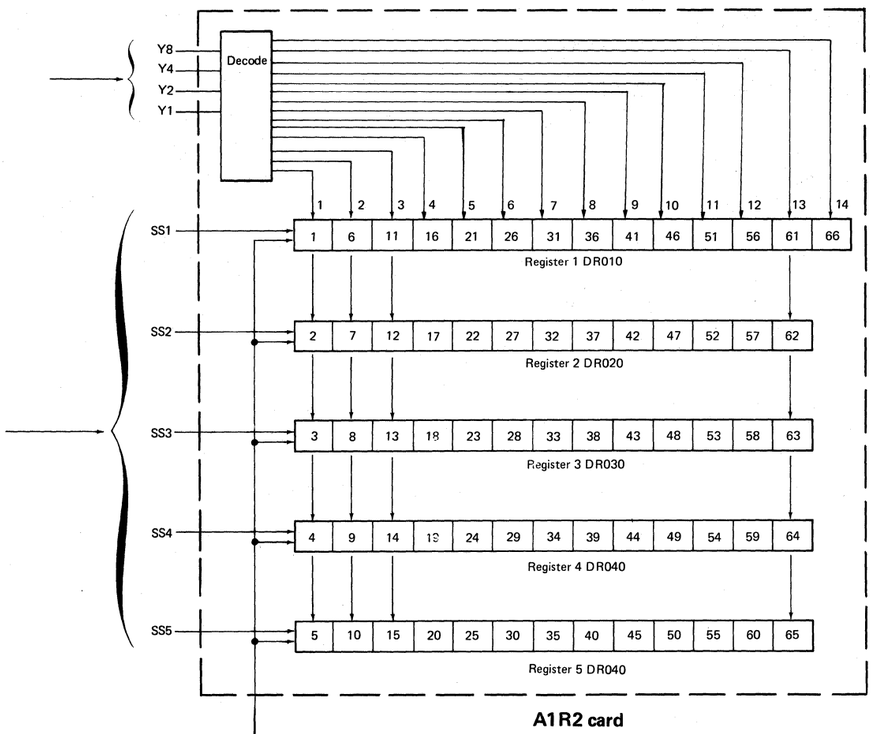
The individual hammer latch within each register is selected by decoding the value of Y lines (value 1 to 27 for registers 1 and 4, and 1 to 26 for registers 2, 3, and 5).

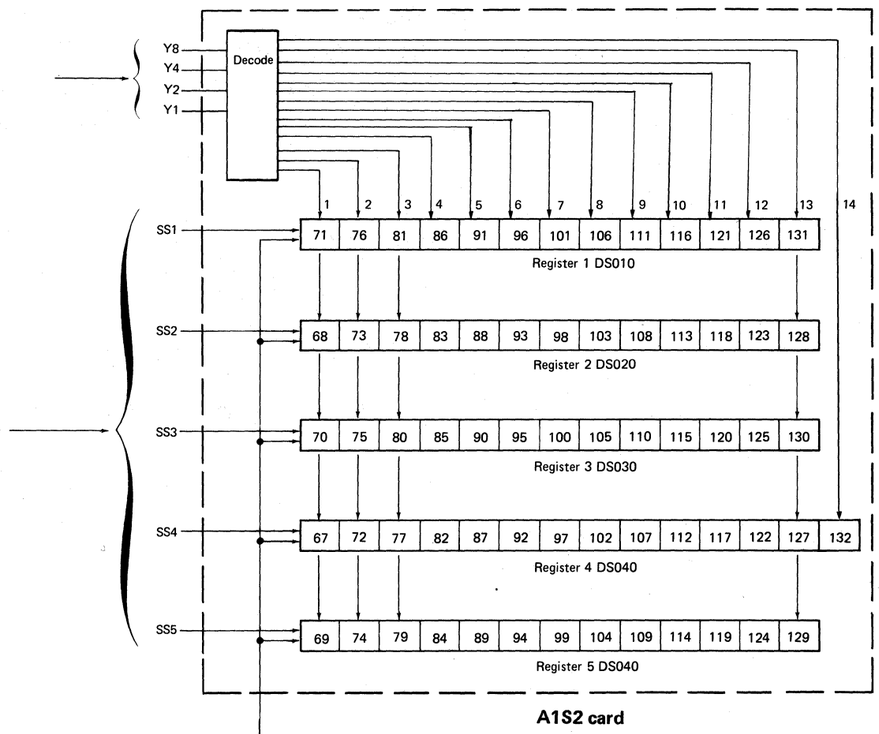
Register Select (285 lpm)

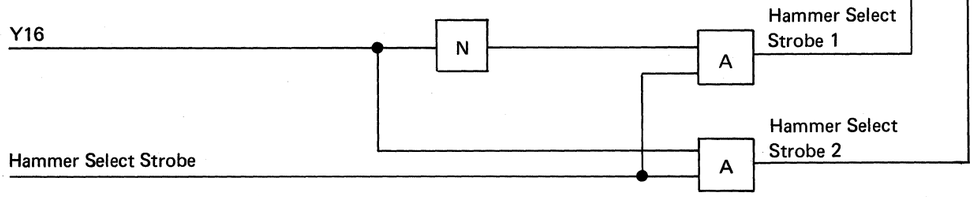
Each register is selected by its corresponding subscan line (subscan 1 to 5).

Hammer Select Strobe (285 lpm)

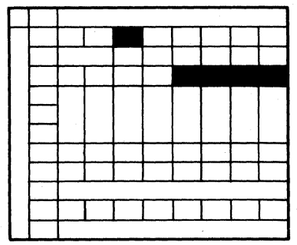
If the scan/buffer compare results is in equal condition, 'hammer select strobe' is activated and sets the particular hammer latch being selected.



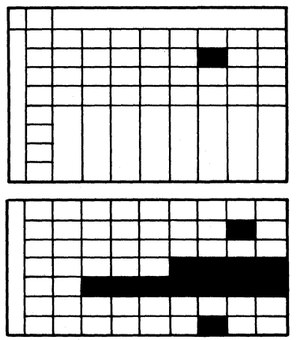




Control Load Command PTR-58



Sense — Control Sense Command PTR-64



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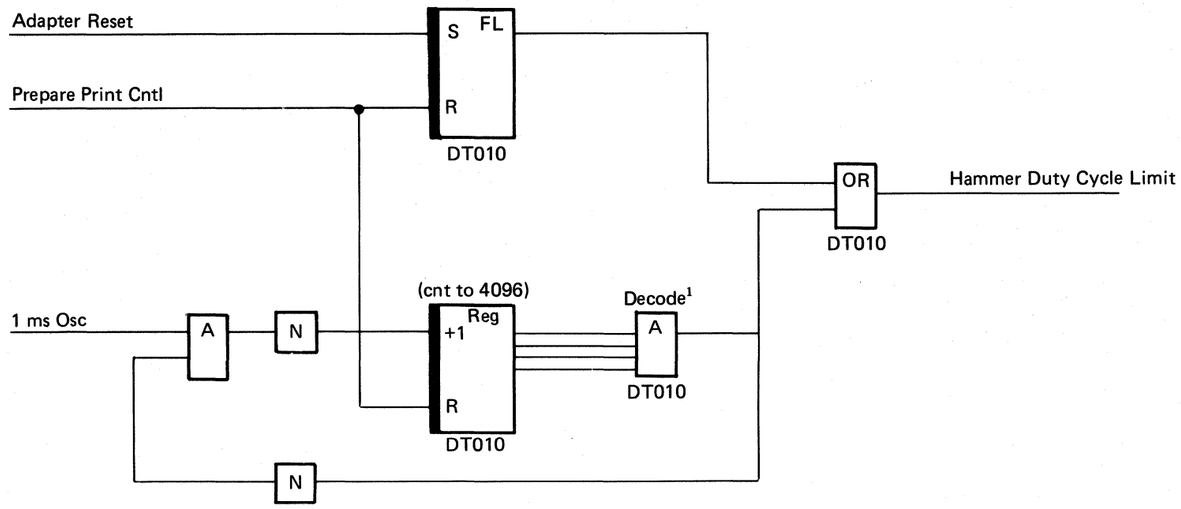
Printer Speed Control

The speed of printing is controlled by the value of a 12 position binary counter (cnt to 4096). The value decoded from the counter determines how long 'hammer duty cycle limit' is active.

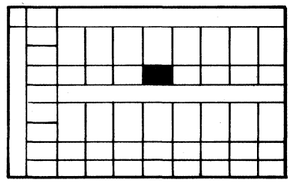
The 'hammer duty cycle limit' line holds up 'print busy' to the channel thus limiting the printing speed.



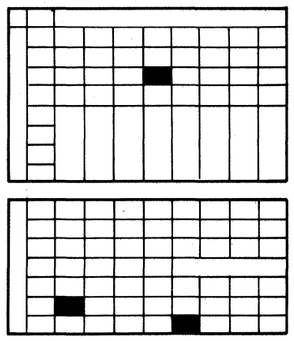
[1]The value decoded from the counter determines the speed of printing. The values used are:

1164 ms for 50 lpm
560 ms for 100 lpm
344 ms for 155 lpm
168 ms for 285 lpm

Load Command PTR-58



Sense — Control Sense Command PTR-64



Carriage Operation (285 lpm)

The printer uses a stepper motor driven pin feed carriage. The carriage uses a vertical spacing of 6 lines per inch.

The carriage advance pulses, generated from the 606 Hz oscillator drive the carriage shift register. The shift register provides the A and B drive lines for the carriage stepper motor. The start pulse brings up 'inhibit detent' which gates the carriage drive lines to the stepper motor.

The number of lines to be spaced must be loaded by a carriage space counter control load command and to initiate a carriage operation. The number of stepper motor steps is equal to 8N–2 where N is the number of lines to be spaced. The space counter is then decremented until the 'steps 2' line is activated (meaning two more stepper motor advances left). 'Steps 2' resets 'carriage go' which turns off the run latch and sets the stop latch. The stop latch gates two more carriage advance pulses to the stepper motor. The last carriage advance pulse (carriage feedback pulse) brings up the line 'steps 0' which resets the 'space time' latch, ending the carriage operation.

The keyboard functions that control the carriage are:

- Carriage restore
- New line (space one line)
- Reset line counter to 1 (tells the system the form is on line 1)

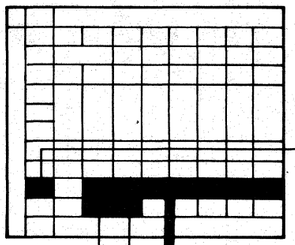
Carriage Detent

When the carriage is not spacing the 1080 Hz line (approximately 1 ms) gates the A, $\overline{A}$, B and $\overline{B}$ drive lines to the print carriage motor. Because the 1080 Hz line is oscillating, it gates the A, $\overline{A}$, B, and $\overline{B}$ drive lines half the time, which allows half current through the stepper motor. This provides the carriage electrical detent.

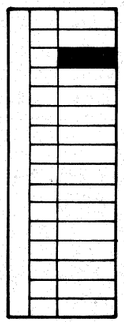
Note: Dual ramping card values are 70 percent of the values shown until '—Belt Motion' is active.

Loss of 24 Vdc or power on reset removes the detent

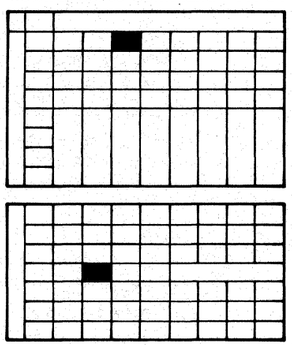
Control Load Command PTR-60



Jump I/O Command PTR-70



Sense —
Control Sense Command PTR-64



Attachment

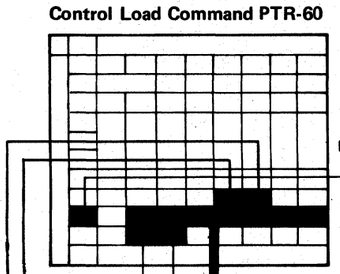
Half Line Space Operation (285 lpm)

The half line space print feature permits indexing of the printer one half space above or below the normal print line. This spacing is used for super-scripting or subscripting a character on the print belt.

The half line space print feature supplies the printer attachment with eight carriage advance pulses when only four carriage advance pulses are sent by the printer to the carriage advance shift register. During the half line space operation, when the first carriage advance pulse is received by the half index card, five fast (64 μs) carriage advance pulses are generated from the 4 μs clock and sent to the printer attachment before the second carriage advance pulse is received from the printer. When the second pulse is received from the printer, it is passed unaltered to the printer attachment. This pulse becomes the sixth carriage advance pulse to the printer attachment and carriage go is dropped. The deceleration function begins and the third and fourth carriage advance pulses from the printer are received by the printer attachment. These are the seventh and eighth pulses in the carriage line position counter (count to eight). Because the printer attachment has received eight pulses in the carriage line position counter, the acceleration and deceleration timing of a full index is retained and forms jam and carriage sync checking are performed.

A half index is initiated by setting the carriage reverse bit (bit 4) in a control load command (IOCL) with a modifier of A. Half index mode is reset by bit 5 of the command and the half index feature card is reset by bit 5 of the command, dropping carriage go, or resetting the printer attachment.

Half index complete (for diagnostics only not shown) indicates that the five fast pulses to the printer attachment have been generated and the completion of the index operation is under control of the carriage advance digital control in the printer.



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Input/Output Lines (285 lpm)

A = from attachment
P = from printer

POR/Printer Reset (A)

POR/printer reset line is initiated during the power up sequence to reset the printer circuits to their starting condition. It is also activated if a carriage sync check is detected.

Close (+24V) Contactor (A)

Close contactor must be activated to switch the +24V into the printer. This line is deactivated when a hammer parity check is sensed to protect the hammer coils.

Belt Go (A)

Belt go is activated to start the belt oscillator. The belt oscillator furnishes pulses to run the type belt drive circuits.

Belt Motion (P)

The belt motion signal is active when the type belt reaches operating speed. It becomes inactive when the belt speed decreases to approximately 10 per cent below the operating speed. The home pulse and the subscan pulses become active when the belt is up to speed.

PSS (Subscan) (P)

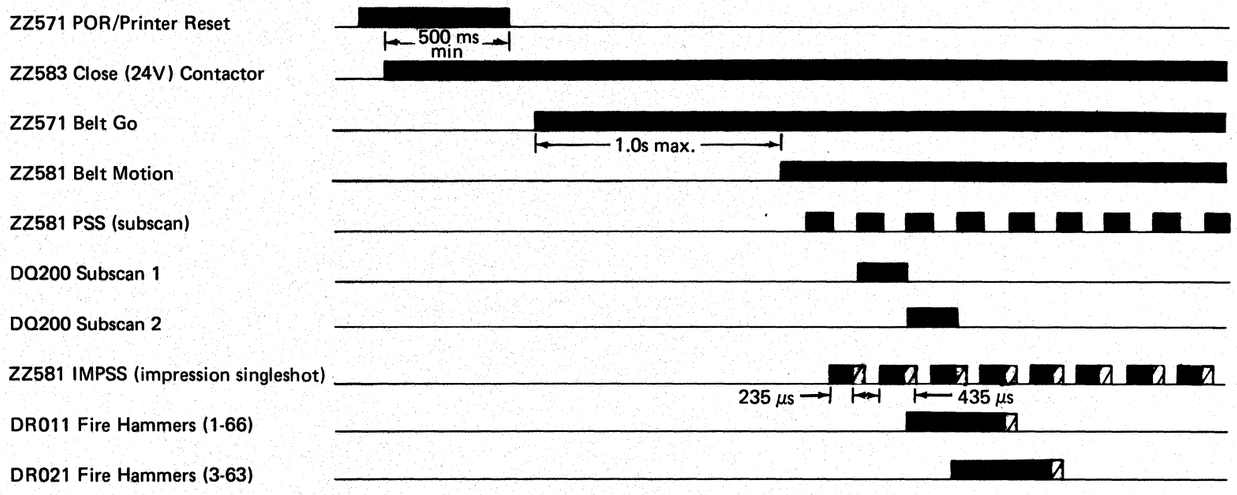
The PSS pulses are generated from the raised timing marks on the type belt. The subscan pulses synchronize the print controls between the attachment and the printer. When the home pulse is detected, a dummy pulse is generated because of the missing timing mark.

IMPSS (Impression Singleshot) (P)

IMPSS is added to the hammer fire pulse to control the time the hammers are fired for different forms thickness. This signal is activated when the subscan pulse goes inactive (halfway into a subscan) and remains active 140 μs to 423 μs depending on the setting of the forms thickness control.

Fire Hammer (A)

Fire hammer lines are activated to fire the corresponding print hammers (fire hammer 1 = print hammer 1, etc).



Activate Paper Clamps (A)

This signal energizes the upper and lower paper clamps. It is deactivated during a spacing operation and when the printer is idle.

Home Pulse (P)

On the type belt there is a double space between two of the timing marks. This space (missing timing mark) generates the home pulse that signals the start of the type set on the type belt. The home pulse is used to synchronize the type belt and the belt position counter.

Hammer Check 1-44, 45-88, 89-132 (P)

The hammer check lines determine that in each group an odd number of hammers is on (when active). They are used as input for the hammer parity check and the coil current check.

Carriage Go (A)

This line activates the carriage advance digital control circuits. These circuits furnish pulses to run the carriage drive circuits.

Stop Ribbon (A)

The stop ribbon line is activated if the printer is idle for five seconds. When the signal is activated, the ribbon stops moving to prevent smudging the paper.

Carriage Advance (P)

The carriage go line activates the carriage advance digital control circuits. These circuits generate the carriage advance pulses. Each carriage advance pulse advances a shift register which advances the print carriage motor by one increment (eight increments per line). Therefore, eight carriage advance pulses decrement the space count once per line. When the space count goes to zero the carriage operation is complete, which resets carriage go. The carriage advance pulse is also used for carriage sync check detection.

Printer Thermal Switch (P)

This line signals that the temperature in the printer circuitry is too high. It indicates a thermal check in case of overheating. The switch opens at 145°F, ±5°F (63°C ± 3°C).

Cover Closed Switch (P)

The cover must be closed to make the printer ready.

Forms Sensed Switch (P)

This line indicates to the attachment whether or not there are forms in the printer.

Throat Closed Switch (P)

This line sends the condition of the casting throat interlock switch to the attachment. It must show a throat closed condition to make the printer ready.

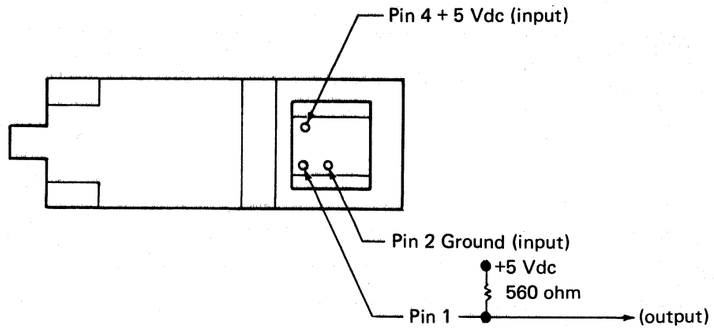
Switch Assemblies

CAUTION
These are electronic switches and do not have conventional switch contacts. A high current source (test light or ohm meter) will permanently damage the switch.

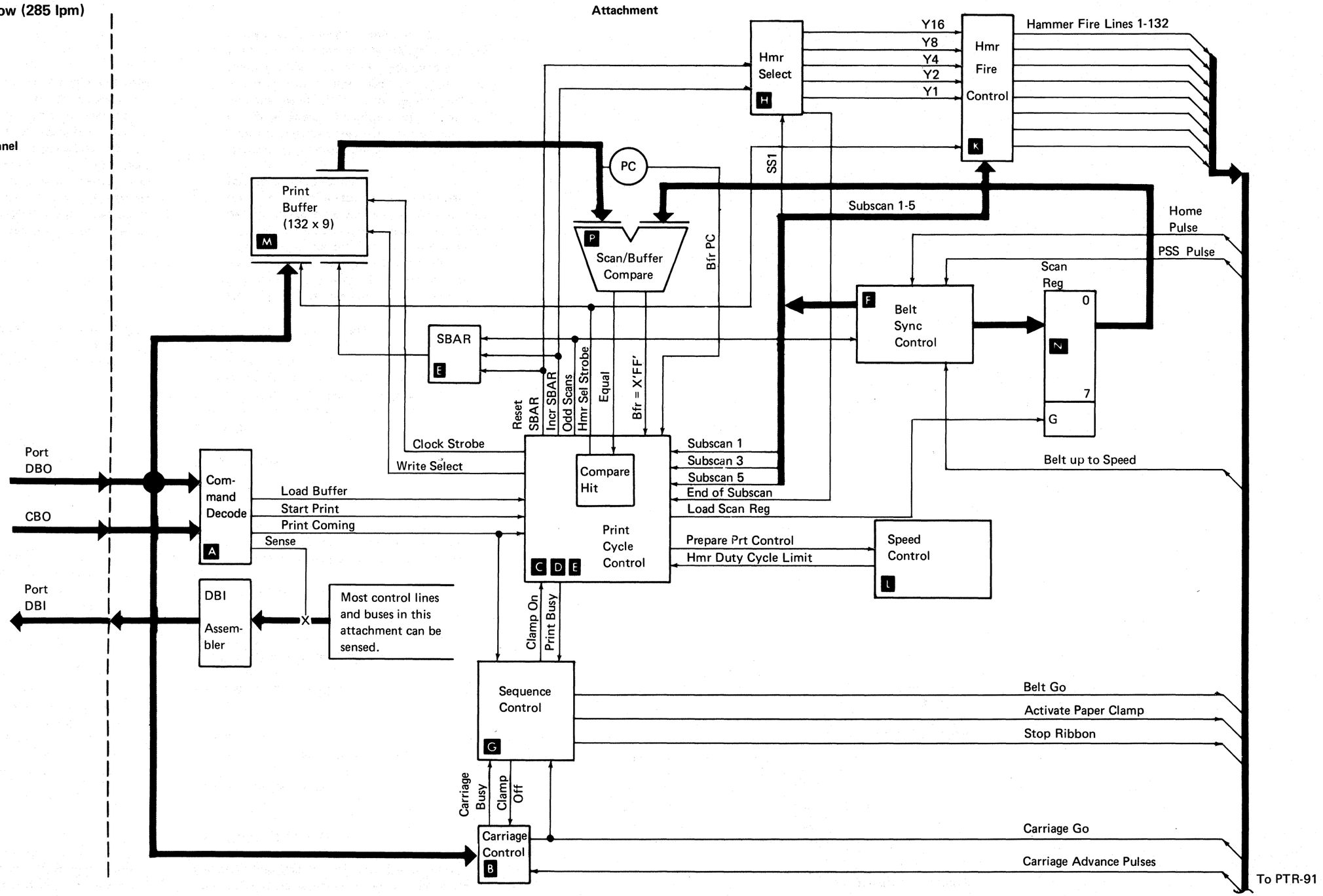
There are two types of switches:

1. Normally ON, red plunger. The south pole of a permanent magnet is positioned over an integrated circuit thus holding the output stage on. Pressing the switch plunger moves the permanent magnet, placing the north pole over the integrated circuit and the output turns off. The plunger is returned to the normal state by a return spring.

2. Normally OFF, black plunger. The north pole of a permanent magnet is positioned over an integrated circuit thus holding the output stage off. Pressing the switch plunger moves the permanent magnet, placing the south pole over the integrated circuit and the output turns on. The plunger is returned to the normal state by a return spring.



Attachment Dataflow (285 lpm)



Attachment Functional Units (285 lpm)

Printer Command Decode DQ020, 030, 040 A [1]

The printer command decode selects the various I/O device operations by decoding the values of DBO and CBO sent to the attachment. The values and their meanings are:

I/O load
I/O control load
I/O sense
I/O control sense
I/O jump

Space Counter DQ100 B

The space counter is a 7 position binary counter. The number of lines to be spaced or skipped is set into the space counter by the microprogram. The counter is then decremented by one for each line spaced until it reaches 0. This brings up the 'steps 0' line which resets the space time latch and stops the carriage operation.

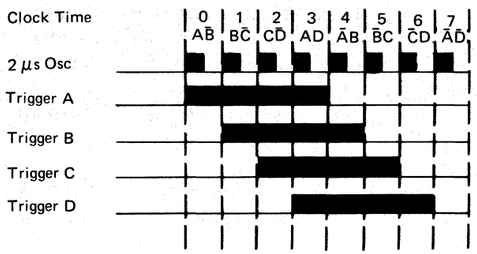
Scan Counter DQ160 C

The scan counter is a 8 position binary counter used to count the number of print scans taken to determine when to end the print scans. The output is decoded into 49 or 65 depending on the character set size being used.

Clocking Triggers DQ170 D

The clocking trigger pulses are generated by a 4 position binary counter. These pulses provide the basic timing used during a print operation.

There are four basic timing pulses generated (trigger A, B, C, and D). The clock pulses 5, 6, and 7 are generated by ANDing certain conditions of the clocking triggers.



Storage Buffer Address Register (SBAR) DQ180 E

The SBAR is an 8 position binary counter used to sequentially address the print buffer. See PTR-28 for the addressing sequence.

Belt Position Counter (BPC) DQ200 F

The BPC is an 8 position binary counter which maintains a count of the character position currently aligned with print position one.

The output of the counter is used as an input to the scan register and the home detection circuits.

Paper Clamp Timer DQ240 G

The paper clamp timer is a 4 position binary counter used to signal the condition of the paper clamps to the attachment.

The paper clamp should be on 15 ms after it is told to turn on by the microprogram. There is no feedback to insure that the clamp is actually on. The clamp is considered to be on when the timer has timed 15 ms. When it reaches 15 ms the timer turns on the clamp on latch.

Similarly, when the clamp is told to turn off, it should be off after 11 ms. When the timer reaches 11 ms it turns on the clamp off latch.

Hammer Select Control DQ290 H

The hammer select control is a 4 position binary counter used to generate the hammer select lines (Y8, Y4, Y2, and Y1). These hammer select lines, in conjunction with the subscan lines (SS1, 2, 3, 4, and 5) determine which hammer will be optioned to fire at any given time. The hammer select lines provide an input to the hammer fire control, where hammer optioning takes place.

Elapsed Time Counter DQ300 J

The elapsed time counter is a 10 position binary counter used to generate an interrupt after a selected time delay. The selected delay is loaded by an I/O control load micro instruction. The counter is then decremented by one until it reaches 0. This brings up the 'elapsed time counter is 0' line which sets the interrupt.

Hammer Fire Control (285 lpm) K

The combination of hammer select lines (Y16, 8, 4, 2, 1) and the subscan lines (SS1, 2, 3, 4, 5) selects which hammers are optioned:

Hammer Select Lines	+ Subscan =	Hammer
Y1	1	1
Y2	1	6
Y1, Y2	1	11
Y1	2	3
Y2	2	8
Y1, Y2	2	13

The hammer select strobe line becomes active when the optioned hammer is to be fired. On the following subscan, the hammer that was set to fire is fired by the fire 1, 2, 3, 4, or 5 pulse.

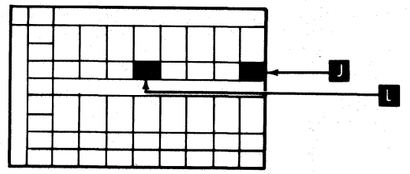
Printer Speed Control L

The speed of printing is controlled by the value of a 12 position binary counter. The value decoded from the counter determines how long 'hammer duty cycle limit' is active:

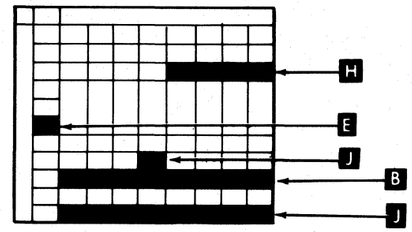
1164 ms for 50 lpm
564 ms for 100 lpm
364 ms for 155 lpm
168 ms for 285 lpm

The 'hammer duty cycle limit' line holds up 'print busy' to the channel thus limiting the printing speed.

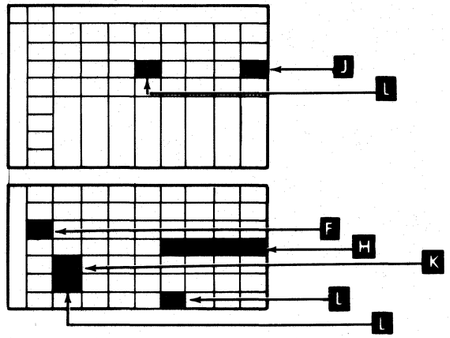
Load Command PTR-58



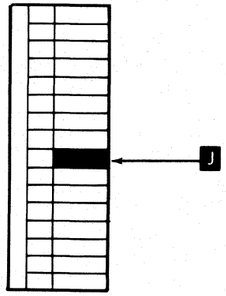
Control Load Command PTR-60



Sense — Control Sense Command PTR-64



Jump I/O Command PTR-70



[1] These keys also refer to PTR-88.

Attachment Functional Units (285 lpm) — Continued

Print Buffer DQ180 M [1]

The print buffer consists of a 128 x 9 bit RAM (random access module) and an auxillary 4 x 9 bit RAM. The two combine to make up the 132 positions for the entire print line. The print buffer contains PFN (print fire numbers) arranged in the sequence in which they are optioned:

Print Buffer	Print Position
00	01
01	6
02	11
03	16

See PTR-28 for buffer arrangement and PTR-27 to determine the value of the PFN.

The PFN is compared to the contents of the scan register. When a match occurs, the print position being addressed is fired. This buffer position is then blanked by writing a hex FF into it.

Scan Register DQ200 N [1]

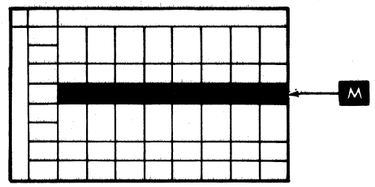
The scan register is used as a holding register for the value of the BPC. It is set on subscan one held through subscan five of each print scan.

The output of the scan register is used in the scan/buffer compare to determine when to print a given print position.

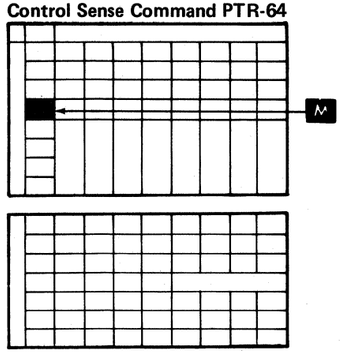
Scan/Buffer Compare DQ280 P [1]

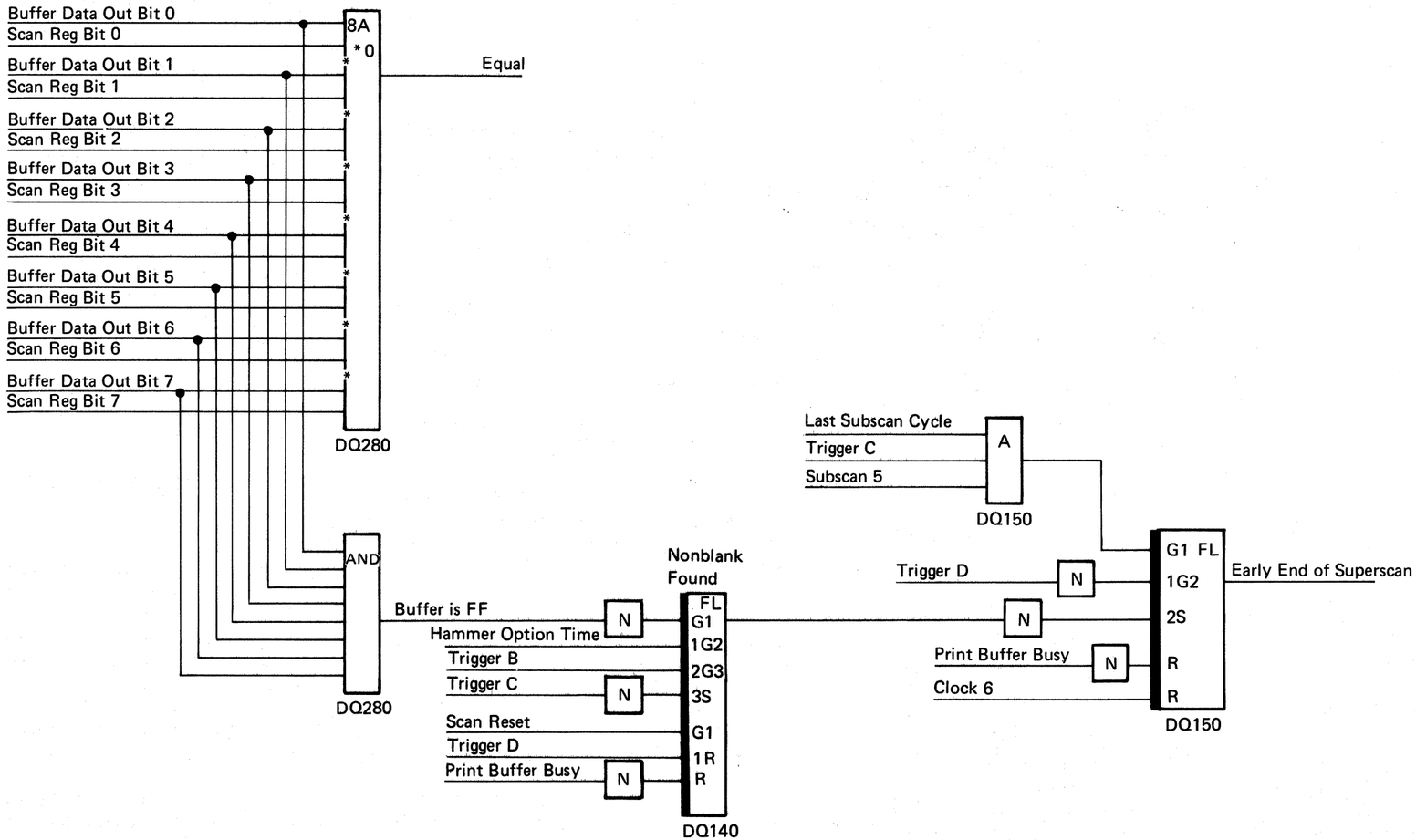
This circuit is used to compare the contents of the scan register with the contents of the print buffer. The data is checked for an equal compare and also for a blank (all positions printed) condition. The nonblank found latch is reset at the beginning of each print scan. It is set when any PFN is found in the print buffer. If no PFN is found by the end of the print scan, the nonblank found latch remains reset and this sets the early end of superscan latch.

Load Command PTR-58



Sense — Control Sense Command PTR-64





[1] These keys also refer to PTR-88.

Printer Functional Units and Dataflow (285 lpm)

A Type Belt Motor and Drive

The 'belt go' signal from the attachment starts the type belt motor. The motor accelerates in increments up to running speed and maintains this speed as long as 'belt go' is active. 'Belt up to speed' becomes active a maximum of one second after 'belt go' is activated.

B Home Pulse and Print-Subscan Pulse Generation

These pulses, generated as the timing marks on the type belt pass a transducer tip, are valid only when the type belt is up to speed. Home pulses (one between each complete character set) are generated by sensing a missing timing mark on the belt. When the belt is up to speed, the continuing home pulses verify that the attachment is in sync with the printer. If the printer is not in sync with the attachment, a belt sync check is indicated.

Print subscan pulses are produced by the timing marks on the belt and by an electronically inserted pulse between each mark.

C Forms Thickness Control

The forms thickness control mechanically adjusts the print unit forward or back for different form thicknesses. The control also adjusts a potentiometer for varying the duration of the singleshot hammer-fire pulse. As the print unit is adjusted for thicker forms, the pulse duration is increased.

D Ribbon Drive

When the ribbon solenoid is deenergized, a clutch engages to drive the ribbon. The ribbon begins to move when printing starts (or during the completion of the first line printed) and continues to move only during printing. After printing stops, the ribbon continues to move until the solenoid is energized to disengage the clutch.

E Paper Clamps

The upper paper clamp consists of a magnet and a clamp bar. The lower paper clamp consists of a solenoid and a clamp bar. Both clamps are activated by the attachment clamp holding the paper during printing.

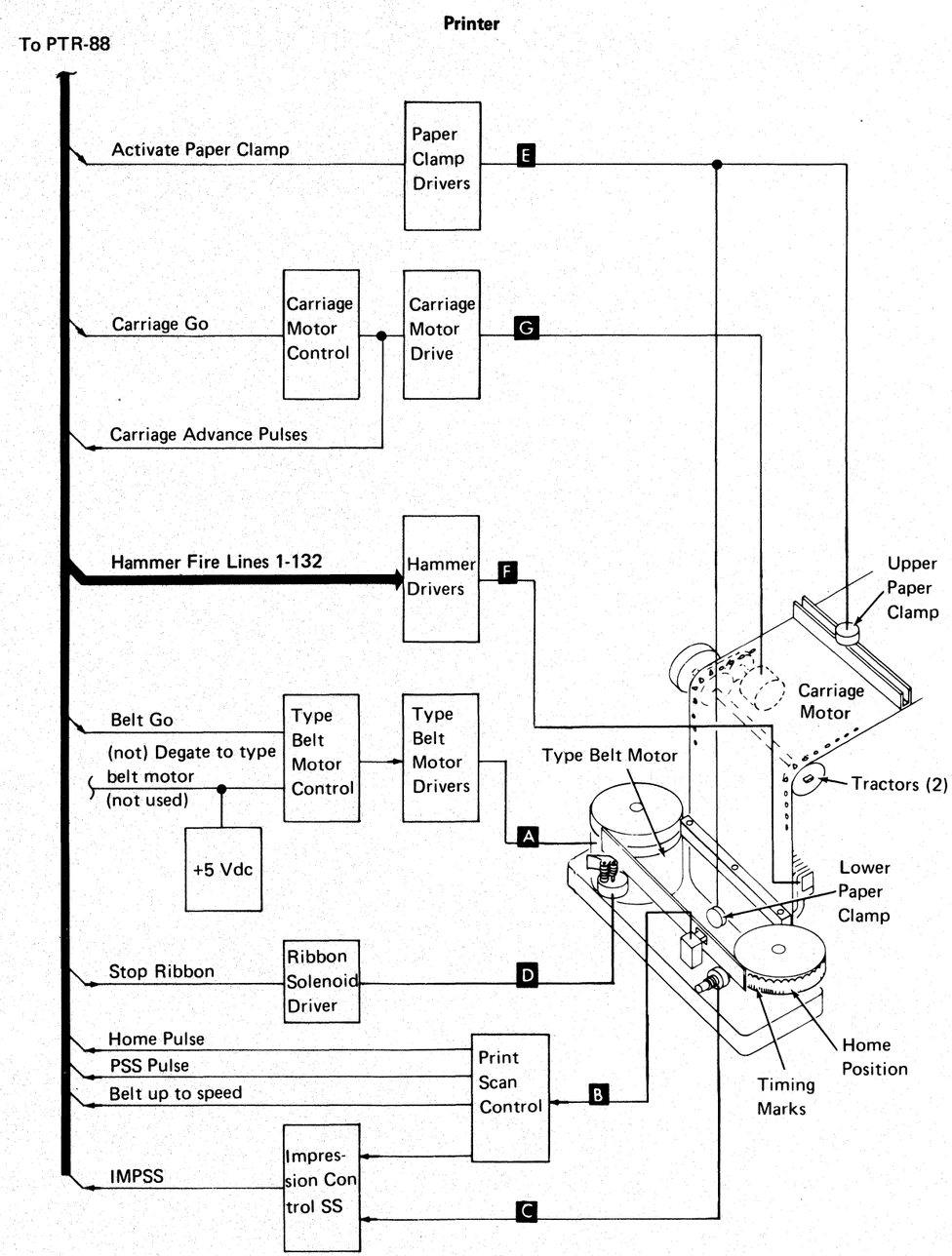
F Firing the Hammers

There is one hammer for each print position. Hammer firing is controlled by the attachment with the timing provided by the printer.

G Carriage Spacing

When a print line is complete, the attachment releases the paper clamps. The forms can now be advanced. To advance the forms, the attachment activates 'carriage go'. The printer electronics then generates 'carriage advance' pulses which control the carriage motor. The attachment counts the advance pulses and deactivates 'carriage go' on the sixth step. Deactivating 'carriage go' initiates two stop pulses for a total of eight stepper motor pulses. This moves the paper 1/6 inch (4.22 mm).

The printer is ready for the next print line cycle. If printing is continuous, steps D through E are repeated.



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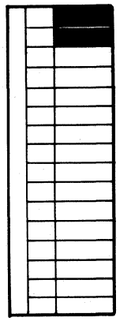
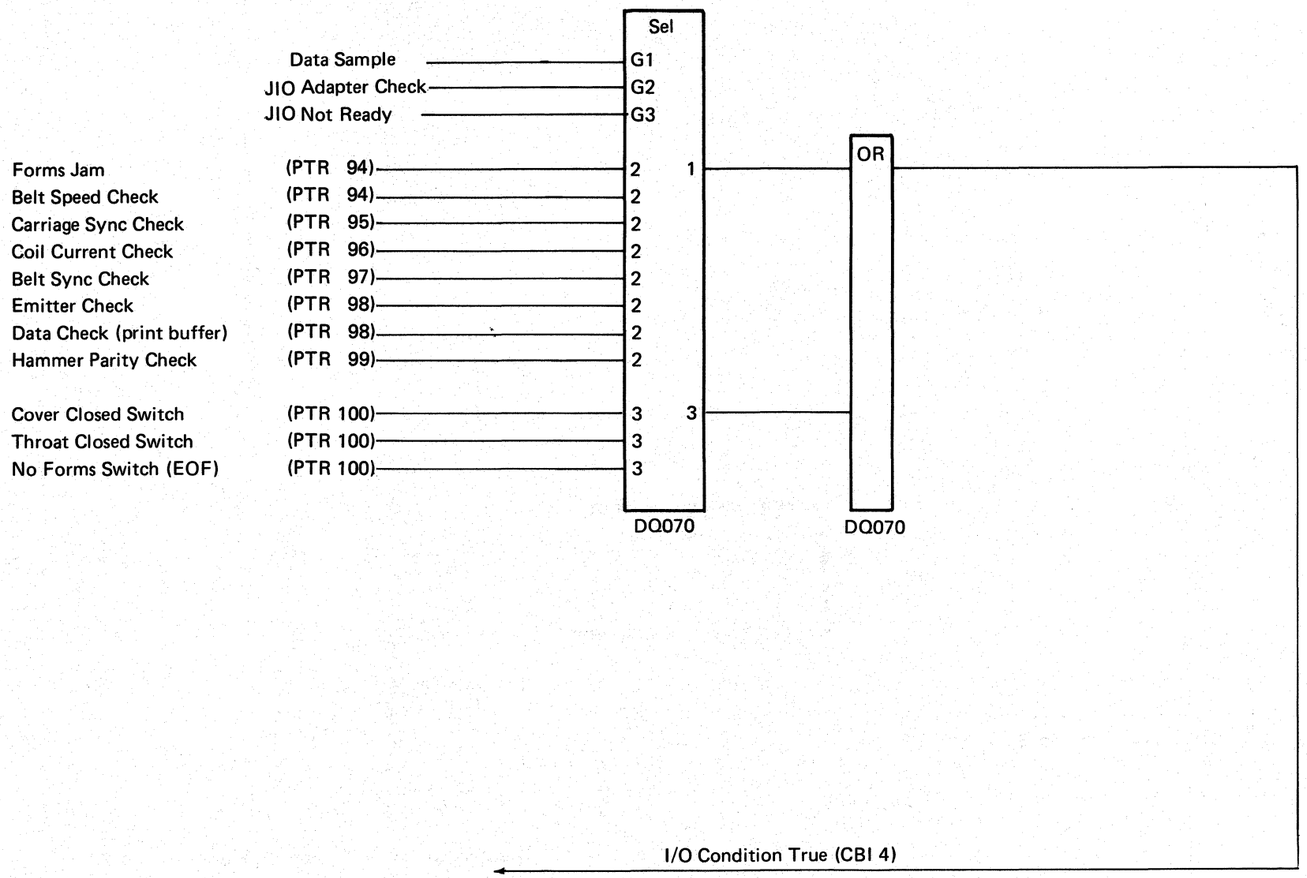
Error Conditions (285 lpm)

The jump I/O command (see PTR-70) detects either the adapter check or not ready condition. A sense command is then required to determine the specific row. See *Sense Command* on PTR-64.

Jump I/O Command PTR-70





Unprintable Character

One or more of the characters requested to be printed were not in the print image. Unprintable character is checked entirely by the microprogram. There is not hardware checking involved. Setting of this check is a programmer option.

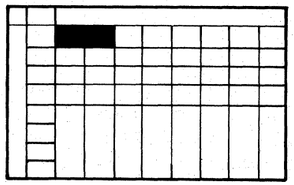
Forms Jam Check/Belt Speed Check (285 Ipm)

Forms Jam Check

The forms jam check indicates that the carriage tractor was told to move, but no paper motion occurred. A light emitting diode detects the time between holes in the paper. If no hole is detected in eight lines, the forms jam is set.

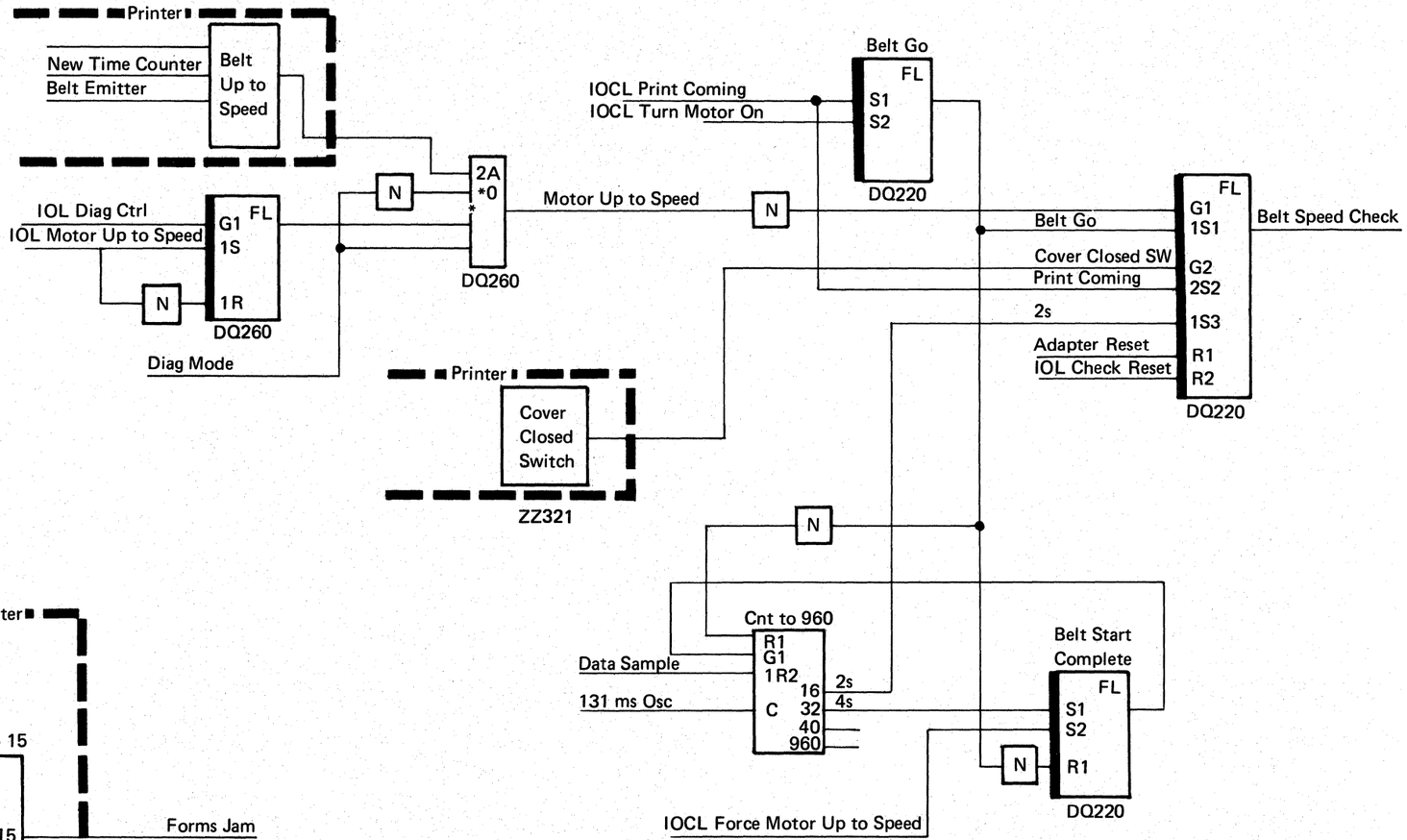
Note: The light emitting diode is infrared so you cannot see the light.

Control Sense Command PTR-64



Belt Speed Check

This check indicates that either the belt has failed to get into motion within two seconds after the start time or the printer belt motion is lost after having reached an up-to-speed condition. Motion is considered lost if there is a 25 per cent loss in operating velocity. The speed is determined by measuring the time between timing marks on the print belt.

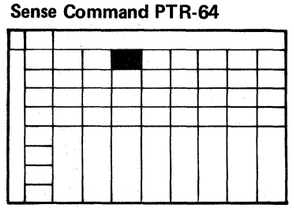


Carriage Sync Check

Two conditions may set this check:

1. If a carriage feedback pulse (carriage advance pulse) occurs when no carriage motion has been initiated.
2. If a carriage feedback pulse fails to occur within 8 ms, during carriage space time.

Sense Command PTR-64

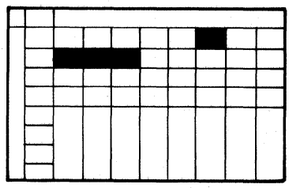


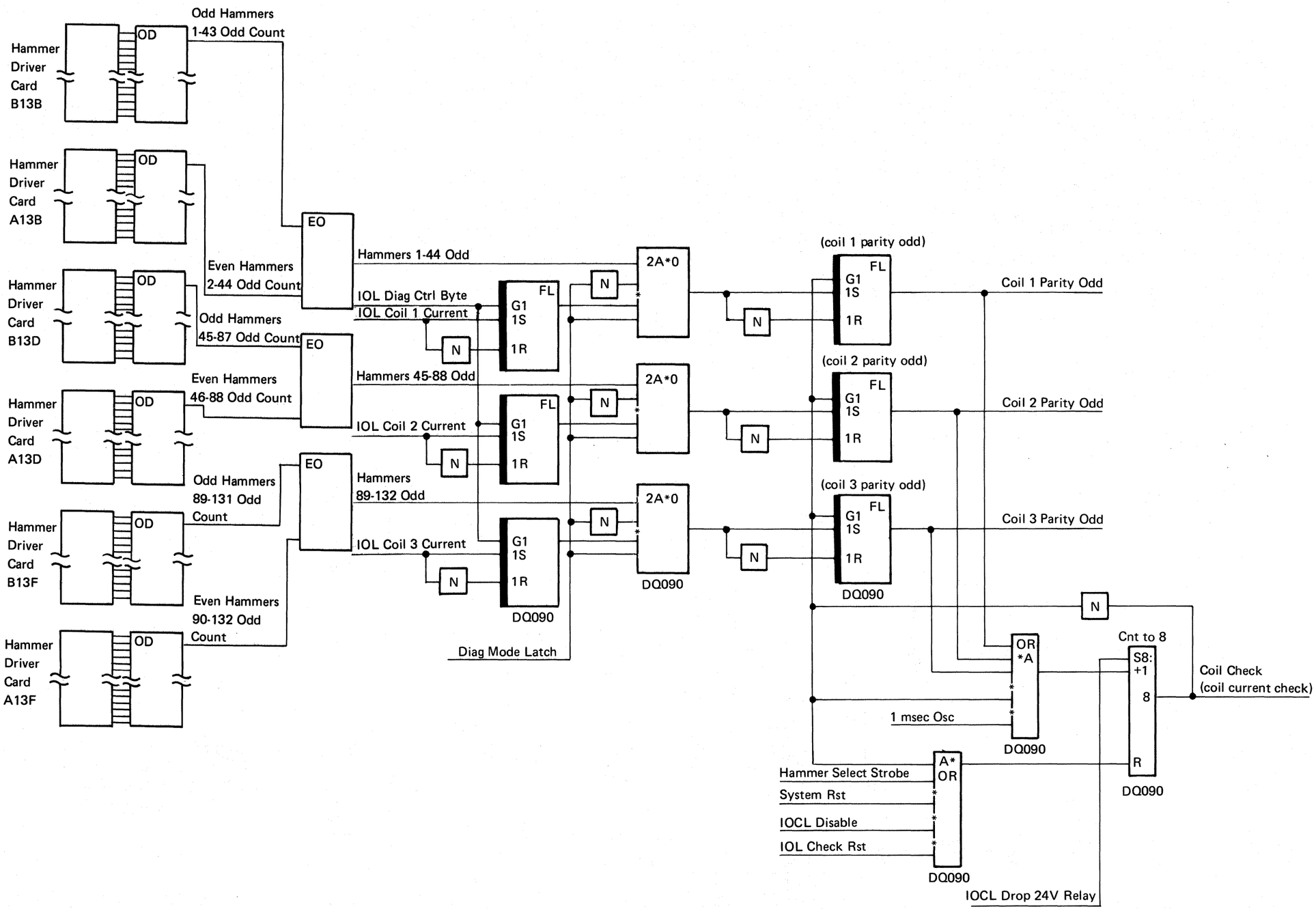
Coil Current Check (285 lpm)

An 8 ms timer (cnt to 8) is started when hammer select strobe sets a hammer latch. Coil parity odd, coil 2 parity odd, and coil 3 parity odd lines are monitored for the possibility of a hammer being on longer than 8 ms. If this condition is detected, power is dropped to the printer and coil, current check is set. The status of the coil 1 parity odd, coil 2 parity and coil 3 parity odd lines is saved in their respective latches. This is because the coil check line being active degates the reset of the latches.

Note: If an even number of hammers, on one hammer driver card, are on (longer than 8 ms), the coil current check is not set. This is because the hammer and odd lines are only active for an odd condition within any one of the three card positions.

Sense Command PTR-64





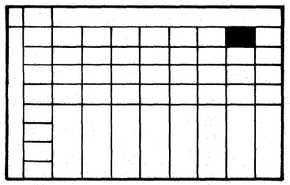
Belt Sync Check

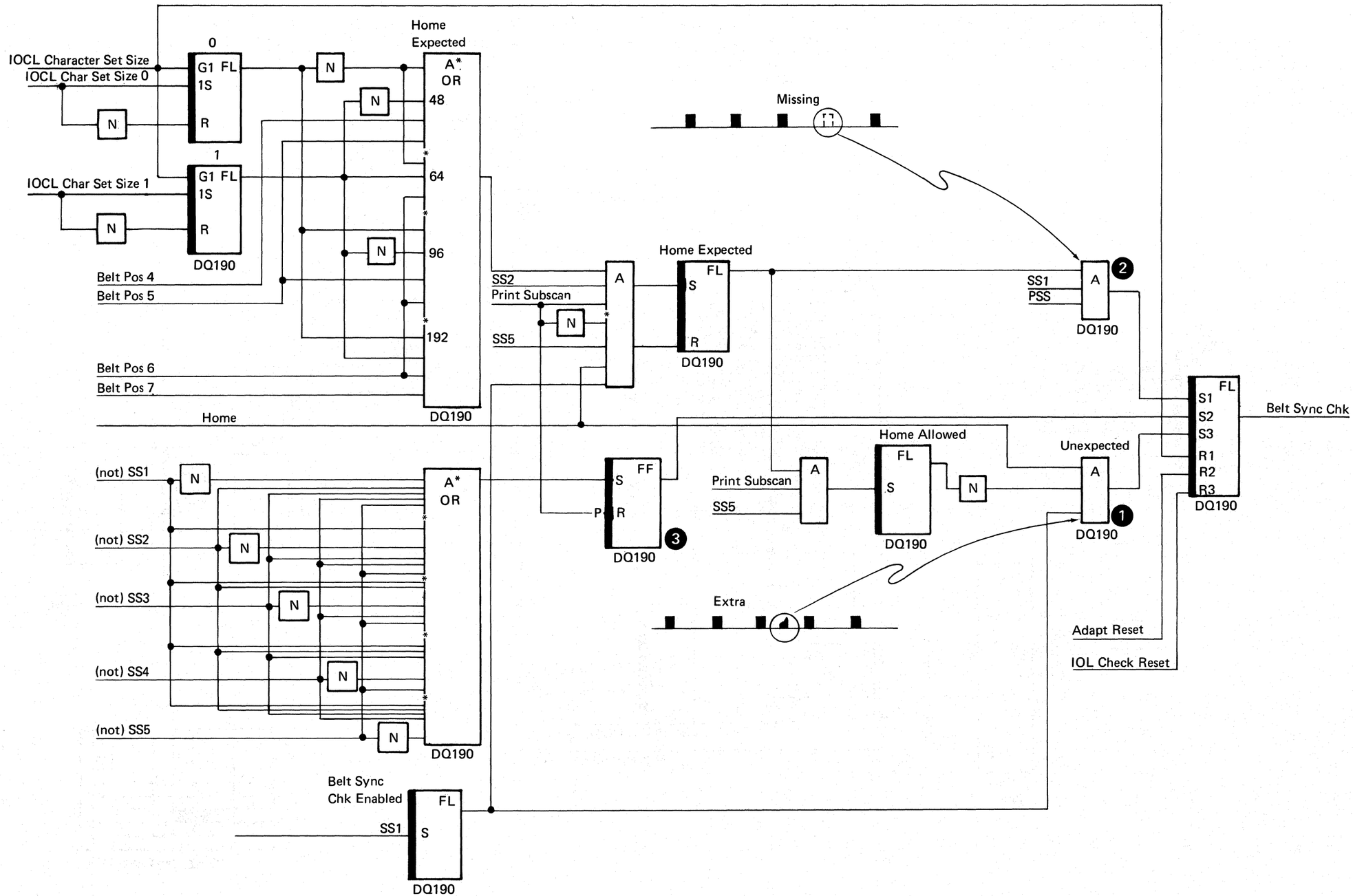
This check can be set by three possible conditions:

1. If a home pulse occurs when not expected.
2. If a home pulse fails to occur when expected.
3. The bit ring generating the five subscan pulses is continuously monitored for an abnormal condition. Normal is one, and only one pulse on at any time.

The timing for the home pulse is determined by counting the number of print scans. This count is compared with the character set size (only one home pulse per character set).

Sense Command PTR-64



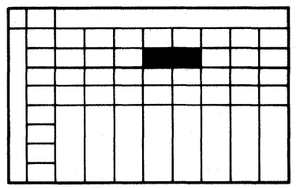


Emitter Check/Data Check

Emitter Check

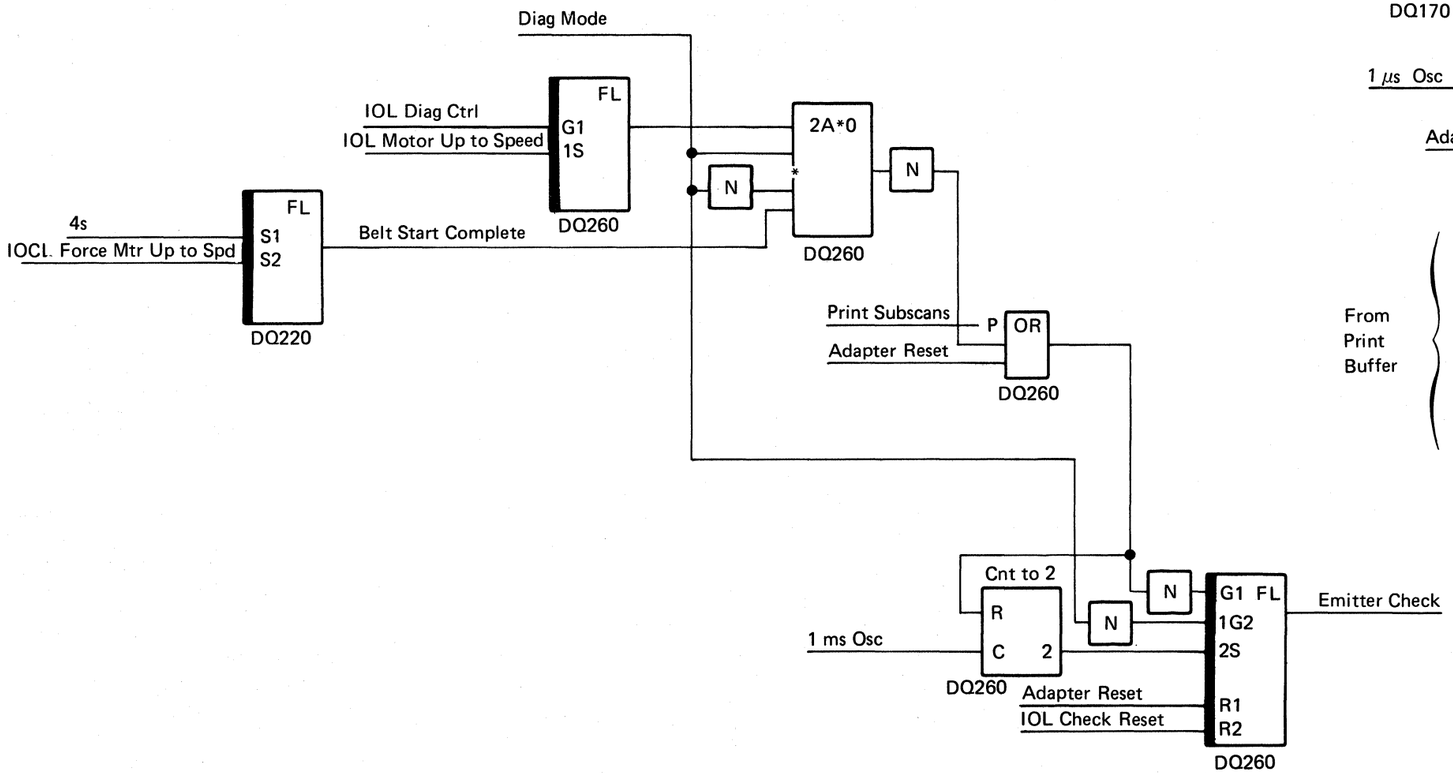
Once the print belt motor has reached an up-to-speed condition, the print subscan line is monitored to verify that it is oscillating. If no change occurs during any 2 ms period, the emitter check is set. This check supplements the belt sync check which cannot detect a broken or stopped belt.

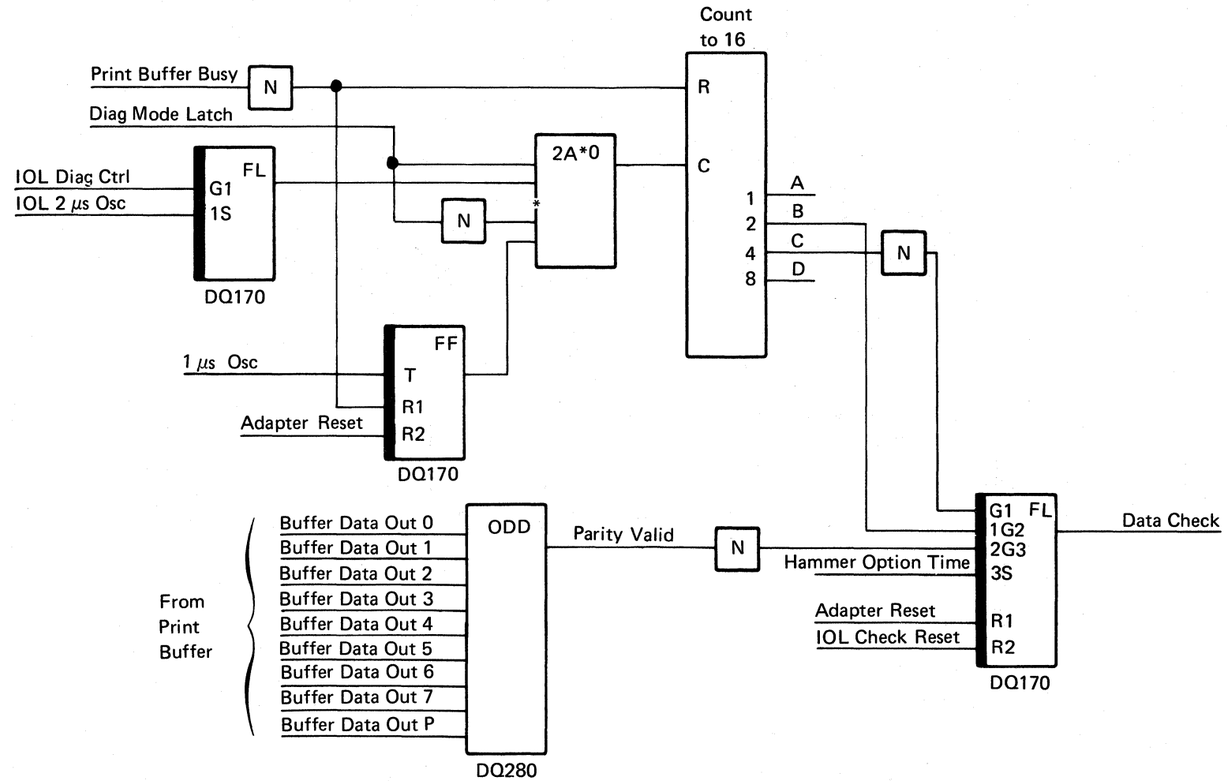
Sense Command PTR-64



Data Check

Parity is maintained on the data in the print buffer. If invalid parity is detected during a print cycle, this data check is set.

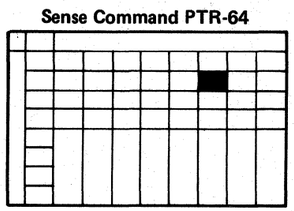


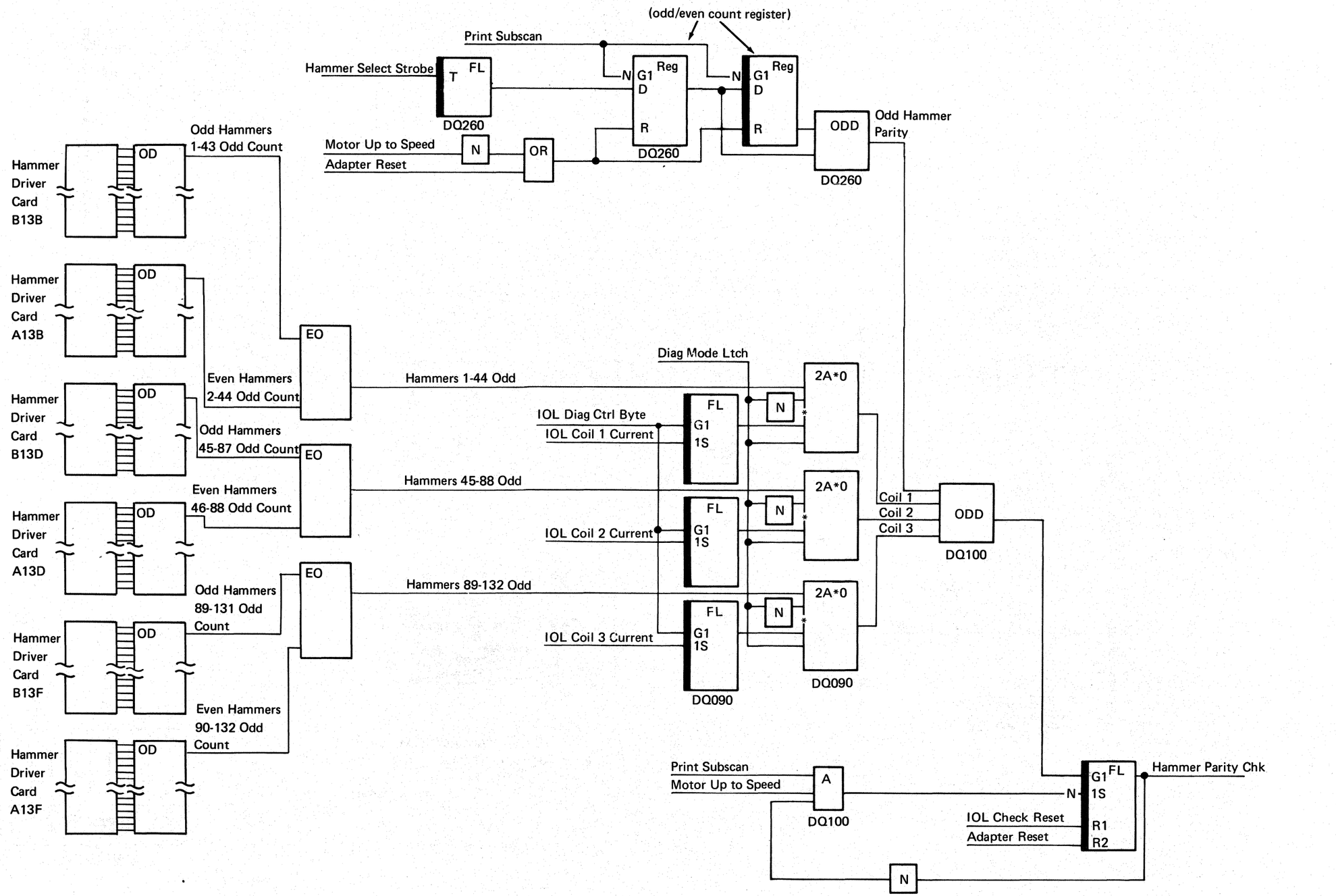


Hammer Parity Check (285 lpm)

An odd/even count of the hammer select strobe pulses is kept track of by the two position odd/even count register. The output of this register indicates whether an odd or even number of hammers have been selected to fire (one hammer select strobe pulse for each hammer selected). The hammer odd line is active for each hammer odd card that indicates an odd number of hammers are being fired. The odd/even count register is compared to the status of the three hammer odd lines during each print subscan pulse. If a mismatch occurs the hammer parity check latch is set.

Sense Command PTR-64



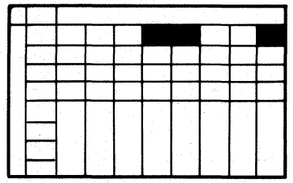


End of Forms/Cover Closed/Throat Closed (285 Ipm)

End of Forms (EOF)

End of forms is checked on the first line printed of each new form. If no forms is indicated by the no forms switch, the printer will go not ready.

Sense Command PTR-64

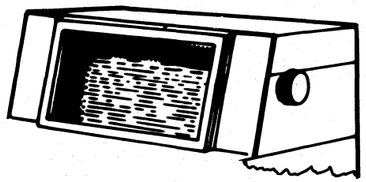


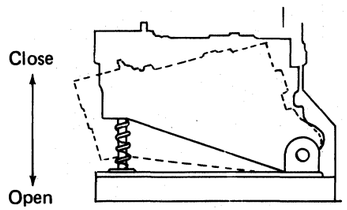
Cover Closed

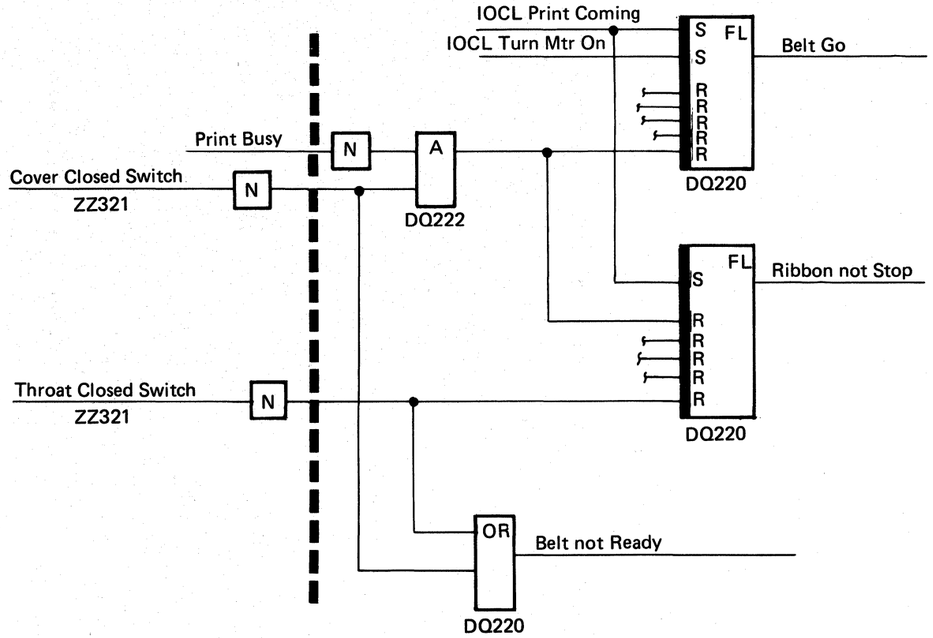
The printer is not ready if the cover is open.

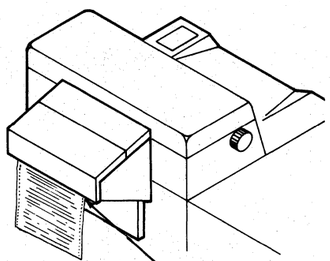
Throat Closed

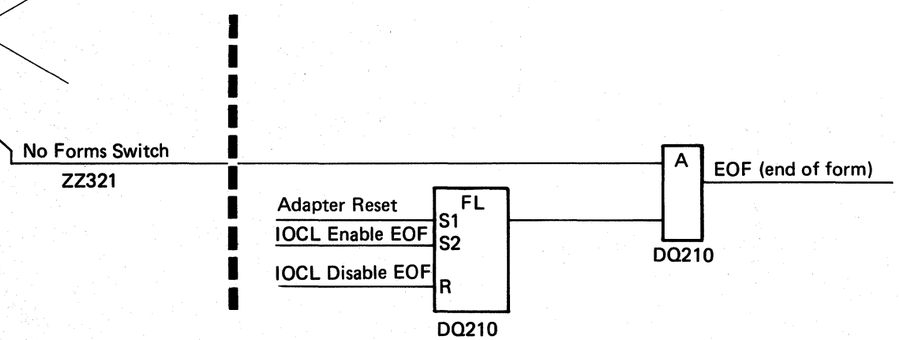
The printer is not ready if the throat is not closed on the paper path.











Display Screen

The display screen attachment occupies the same card as the keyboard attachment. Both attachments use the same:

- CBO (command bus out)
- DBO (port data bus out)
- CBI (command bus in)
- DBI (port data bus in)

Only one of these attachments uses the lines at any time. Which attachment uses the lines is determined by the device address in WR0(L) which is subsequently placed on the DBO lines 0-3.

The display screen attachment has five main functions:

1. Interface with the channel to execute the micro instructions.
2. Accept 240 bytes of data from the channel DBO and store it in the RAM (random access memory) buffer.
3. Increment the display address register to sequentially display the 240 characters on the display screen.
4. Control display of the 240 characters by controlling the video, wiggle, horizontal, and vertical interface lines to the CRT. Up to forty characters per line are displayed on six lines.
5. Load and sense the RAM buffer, the LSAR (load/sense address register), and the DAR (display address register) and send the data to the channel.

The channel:

1. Places decoded micro instruction data on CBO 0-2, device address on DBO 0-3, and micro instruction modifier data on DBO 4-7.
2. Activates 'control out' to indicate that a command is on the channel.

Each attachment checks the address; if it is the display screen address, the attachment activates 'CRT command select' so that the display screen can accept the command.

If the command is sense, control sense, or jump, data from the LSAR, data from the DAR, data from the RAM buffer, or the status of various latches is placed on the DBI lines. The attachment brings up 'service in' to indicate to the channel that the data is on DBI. The channel accepts the data and responds with 'service out' to indicate that the data was received. The attachment then drops 'CRT command select' and completes communication with the channel.

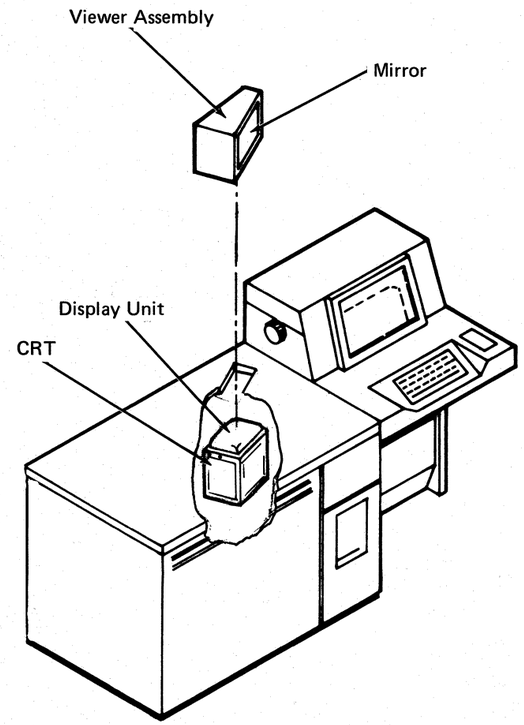
If the command is sense interrupt level status byte, the attachment does not accept the command but brings up 'service in' and 'multi-device response' to indicate to the channel that the command was detected and not accepted.

If the command is load or control load, the attachment again checks the device address and raises 'CRT command select'. The attachment sets or resets latches per the command and responds with 'service in' to indicate that the command was accepted. The channel responds with 'service out' to indicate that the data on DBO is now valid. The attachment then activates the 'data sample' which gates data on the DBO to the load/sense address register, the display address register, or to additional latches. The attachment drops 'CRT command select' to terminate communications with the channel.

Whenever data is on DBO, the attachment checks for odd parity. If the parity is not odd, the attachment activates CBI 5 to indicate that the data is bad.

Attachment Functions

1. The attachment interfaces with the channel to execute the micro instructions as follows:
   - Accepts 'control out' to establish communication.
   - Recognizes and accepts the address of 0100. Decodes CBO to determine what micro instruction is being sent and accepts only valid micro instructions.
   - Decodes DBO 4-7 (modifier bits) to determine the conditions to be established.
   - Raises 'service in' to indicate that the command has been accepted.
2. The attachment accepts 240 bytes of data (one byte at a time) from DBO and stores each byte in the RAM buffer as determined by the LSAR:
   - An I/O load of the LSAR gates the address data from DBO to the LSAR. This address is used to control the destination of the 240 bytes of character data being loaded into the RAM buffer.
   - An I/O load of 'load buffer' gates the 'bfr data set' and presents a character of data from DBO to the RAM buffer. This command conditions 'bfr read/write' to write condition so that the buffer will store the character at clock buffer time (DISP-5). The RAM buffer cannot be loaded when a character to be displayed is being read from the RAM buffer. Therefore, 'bfr read/write' is switched to write only during IOL 'load bfr' and not during RR9 time CC3-42.
   - An I/O sense of sense buffer senses a character addressed by the LSAR. The RAM buffer cannot be sensed during RR9 of the CC3-42 since DAR is fetching the character to be displayed.
3. After the RAM buffer has been loaded with the 240 characters to be displayed:
   - 'Bfr read/write' is placed in read mode. If a load buffer command is in operation, the line will switch to write mode during load buffer time but not during RR9 time of CC3-42.
   - 'Clock bfr' is active at BR0-10 time during RR9 time of CC3-42. 'Clock bfr', along with 'bfr read/write' conditions the RAM buffer to read out the character at the address designated by the display address register and decode circuitry.
   - The character from the RAM buffer is loaded into the character register at BR7 of RR9 time during CC3-42.
   - During BR7 time of RR9 and CC3-42, the next character to be displayed is fetched from RAM through DAR and placed in the character register. The first character is displayed during RR0-6 of CC3-41 time and the last character is displayed during RR0-6 time of CC2.
   - At BR0-10 time of RR8 time of CC3-42 the DAR is incremented by one to locate the next character.



- The character is presented to the character generator and decoded for each wiggle 0-6 of the character. One wiggle at a time of the character is presented to the video assembler. The video assembler serializes the 9 bits of data so that video is gated to the display screen at BR2-10 time along with a corresponding character generator output bit. BR0 is gated to the display screen if the cursor bit is active.
- Characters are displayed during CC2-41 and RR0 through 6. At RR8 during CC3-42 time, after a character has been displayed, the DAR is incremented by one so that the RAM buffer is addressed to read out the next character at RR9 during CC3-42. At RR9 and BR7 during CC3-42 time the character is set into the character register. This character is then available to the character generator to control 'video' to display the next character.
- This operation continues for 40 characters; then vertical control shifts the beam to the next line and the next 40 characters are displayed. After all six lines are displayed, the counters are reset and the display starts over. Any new characters loaded into the buffer are displayed.

4. The attachment controls the video, wiggle, horizontal, and vertical interface lines to the display screen to control displaying of the 240 characters (DISP-6).

   - *Video Line:* 'Video CRT' is sent to the display screen to control an amplifier which increases or decreases the intensity of the beam and creates spots or blanks on the display screen. The 2.25 MHz clock increments 'bit ring count to 16' to produce bit ring pulses that are on for 444 ns. Each 'on' increments the bit ring which counts from 0 through 15. (The counter resets to 15 during a reset condition.) BR0 gates the cursor bit, BR1 time is blank, and BR2-10 gates character generator lines 1 through 9 to the video line to brighten the 11 possible spots on the vertical sweep of the wiggle. BR11-15 are used for retrace time to return the spot to the base line.
   - *Wiggle Sweep:* The wiggle sweep signal is sent to a coil in the CRT to move the beam up and down the height of a character. The wiggle sweep signal is active and sweeps up during BR0-10 and is inactive and sweeps down during BR11-15. Each character has 10 wiggles which are counted by the ROS ring register (RR0-RR9). The first seven wiggles display the characters; the last three wiggles are used for spacing between characters. The ROS ring register is incremented by the bit ring register at BR11 time. At RR7 time, the ROS ring increments the character. The wiggle line is active from CC0 through CC42 and inactive from CC42 through CC53.
   - *Horizontal Line:* The horizontal line, when active, conditions a coil in the CRT to move the beam to the right at a constant speed for a 42 character line. The first two character positions are used for beam speed up time, then 40 characters are displayed. When the horiztontal line is inactive, the beam sweeps to the left at a constant speed for 12 character times (CC42-53) for retrace. The character count register (CC0-53) conditions the horizontal line.
   - *Vertical Line:* The 'vert 1', 'vert 2' and 'vert 4' lines increment the beam to the six possible display lines. The line counter (LC0-LC5) is incremented at CC42 time so that the beam goes to the next line during retrace. The 'vert 1', 'vert 2', and 'vert 4' lines are decoded to determine which of the six lines is required. When all three lines are inactive, display line 1 is selected.

     The line counter increments from 0 through 5 and then back to 0 to start over and refresh the display.

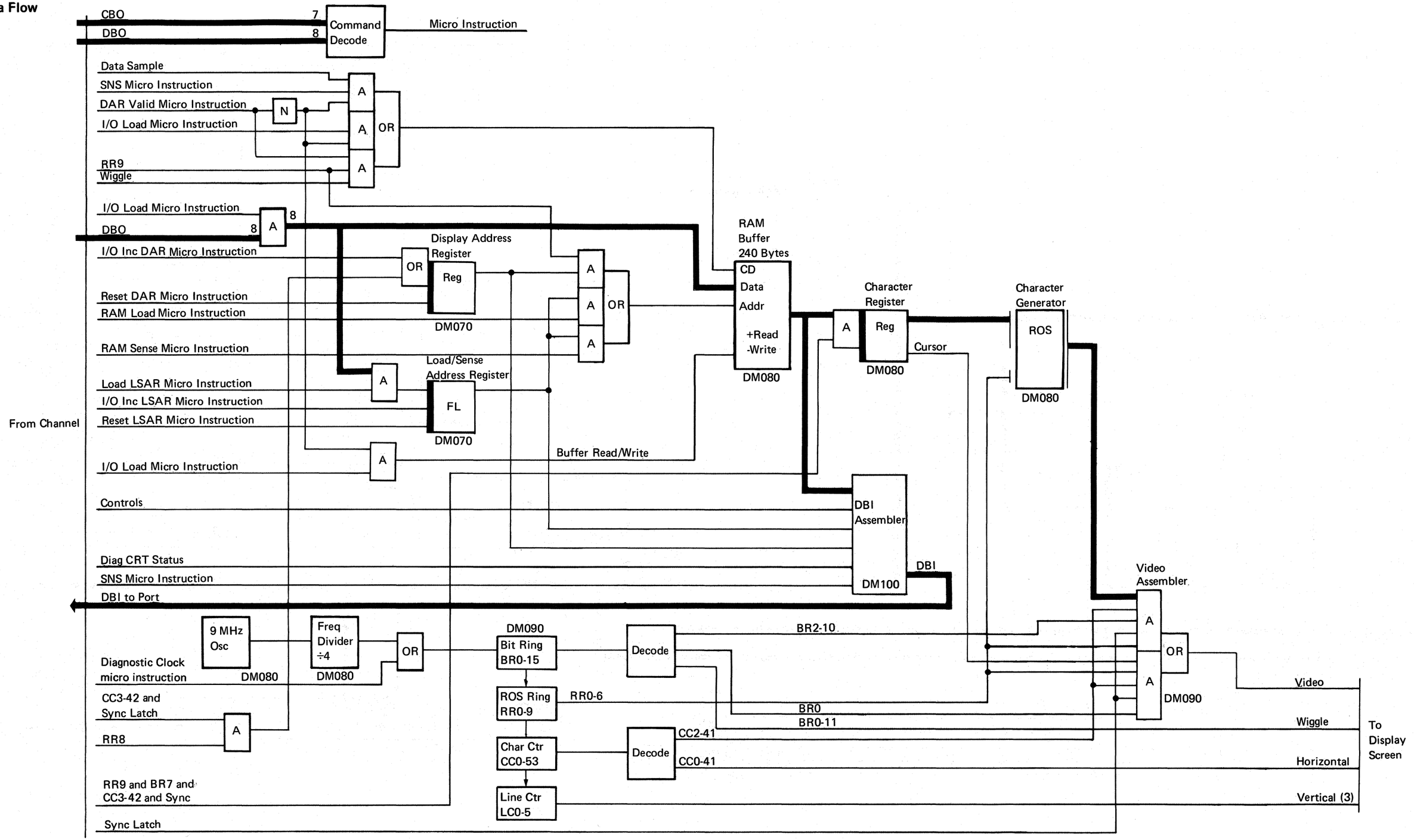
5. The attachment senses the status of the LSAR, DAR, and the control latches.

   - At sense the LSAR command causes the address in the LSAR to be placed on DBI. (This cannot be done during display time, BR0-10 of RR9 during CC3-42.)
   - At BR0-10 time of RR9 during CC3-42, the address is read from DAR and placed on DBI.
   - The control latches are sensed by appropriate sense commands and the data placed on DBI. (See the appropriate sense command charts, DISP-30, -32.

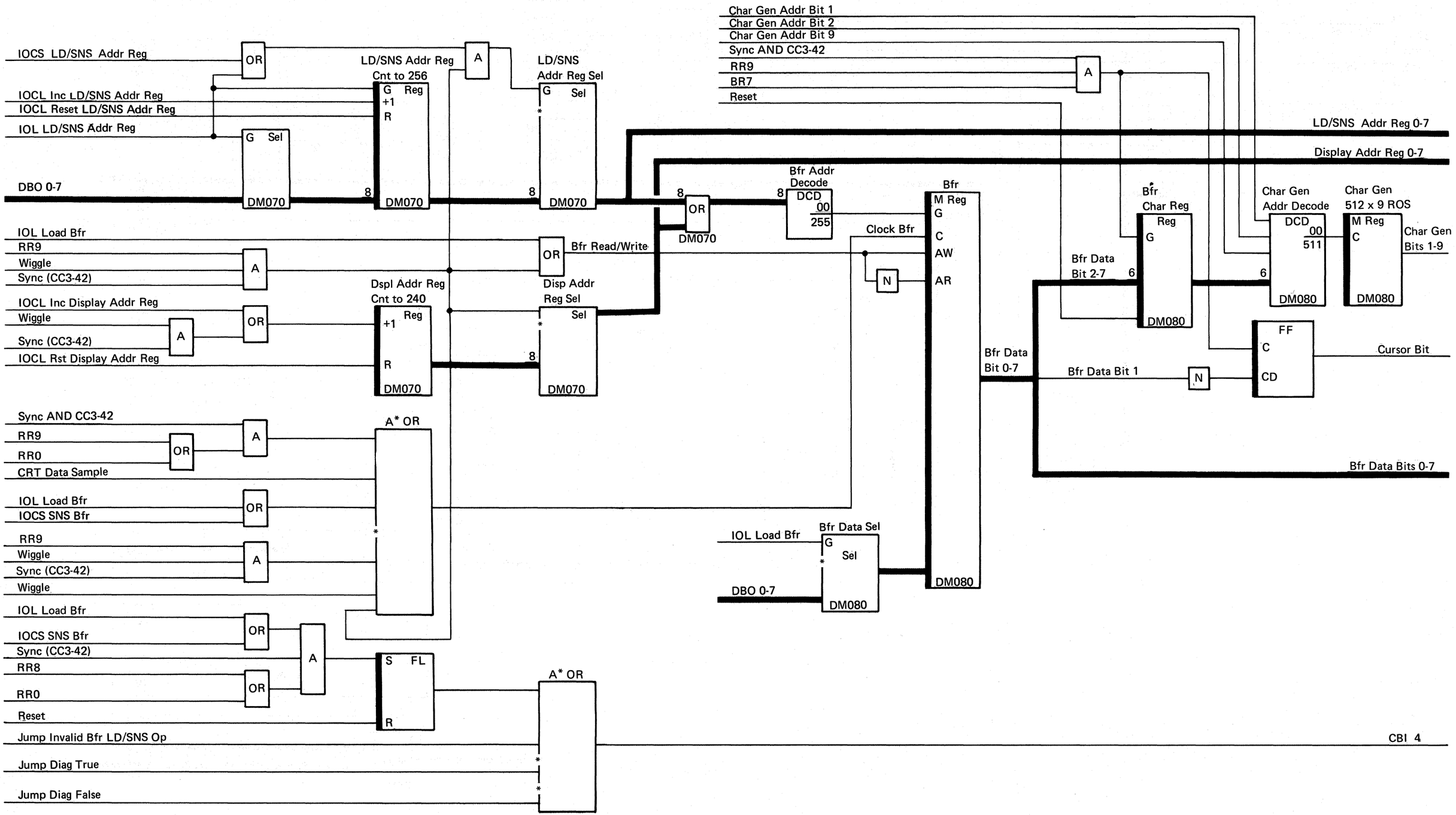
Display Line	Vertical Input DM090		
	Vert 1	Vert 2	Vert 4
1	0	0	0
2	1	0	0
3	0	1	0
4	1	1	0
5	0	0	1
6	1	0	1

1 = Line Active

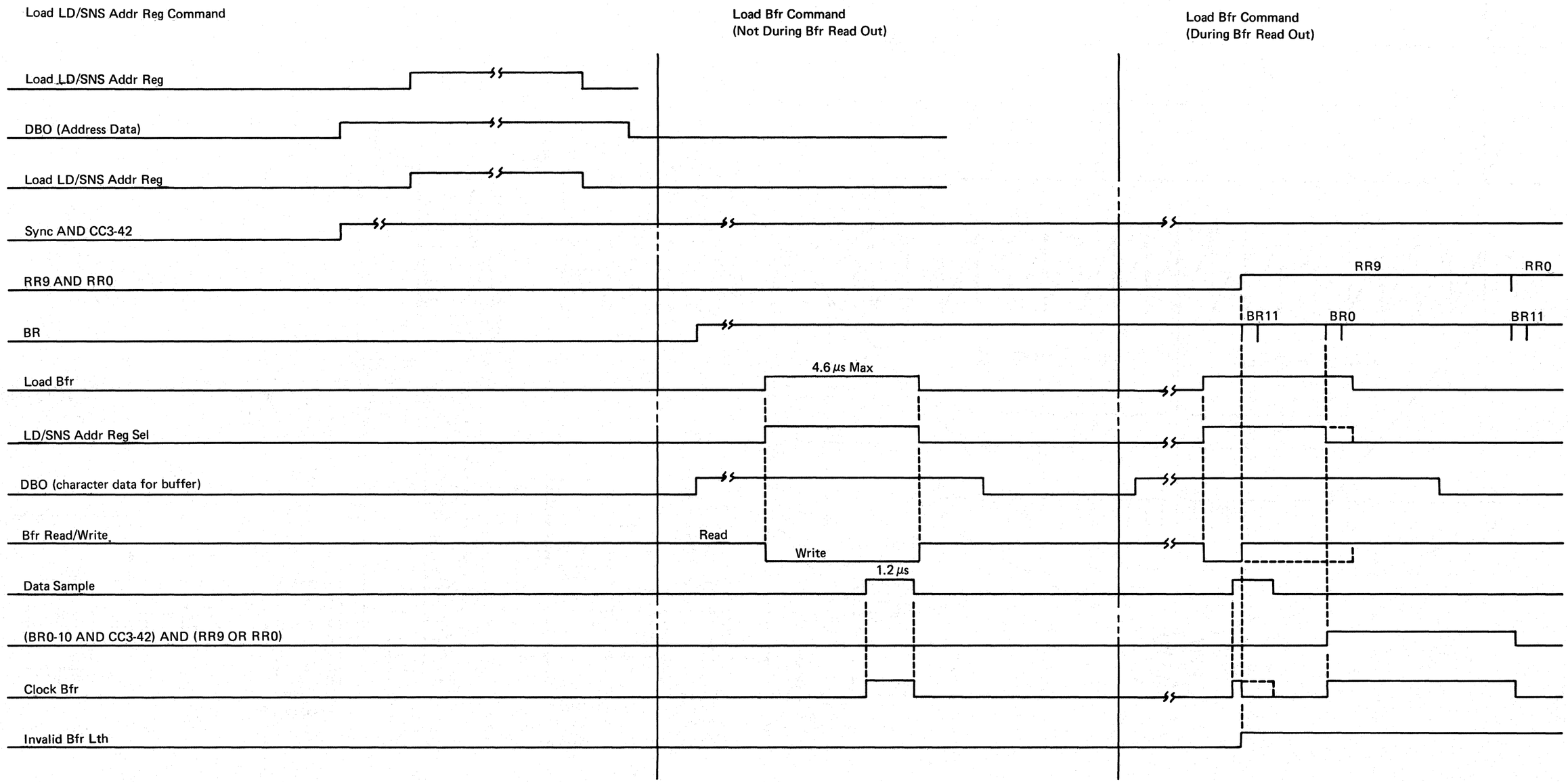
Data Flow


CBO
7
DBO
8
Command Decode
Micro Instruction
Data Sample
SNS Micro Instruction
DAR Valid Micro Instruction
I/O Load Micro Instruction
N
A
A
A
OR
RR9
Wiggle
I/O Load Micro Instruction
DBO
8
A
8
I/O Inc DAR Micro Instruction
Display Address Register
OR
Reg
DM070
Reset DAR Micro Instruction
RAM Load Micro Instruction
RAM Sense Micro Instruction
A
A
A
OR
RAM Buffer 240 Bytes
CD
Data
Addr
+Read
-Write
DM080
Load/Sense Address Register
Load LSAR Micro Instruction
I/O Inc LSAR Micro Instruction
Reset LSAR Micro Instruction
A
FL
DM070
From Channel
A
Character Register
Reg
DM080
Cursor
Character Generator
ROS
DM080
I/O Load Micro Instruction
A
Buffer Read/Write
Controls
DBI Assembler
DM100
DBI
Diag CRT Status
SNS Micro Instruction
DBI to Port
Video Assembler
A
A
OR
DM090
9 MHz Osc
DM080
Freq Divider ÷4
DM080
OR
Diagnostic Clock micro instruction
CC3-42 and Sync Latch
RR8
A
DM090
Bit Ring BR0-15
ROS Ring RR0-9
Char Ctr CC0-53
Line Ctr LC0-5
Decode
Decode
BR2-10
RR0-6
BR0
BR0-11
CC2-41
CC0-41
Video
Wiggle
Horizontal
Vertical (3)
To Display Screen
RR9 and BR7 and CC3-42 and Sync
Sync Latch

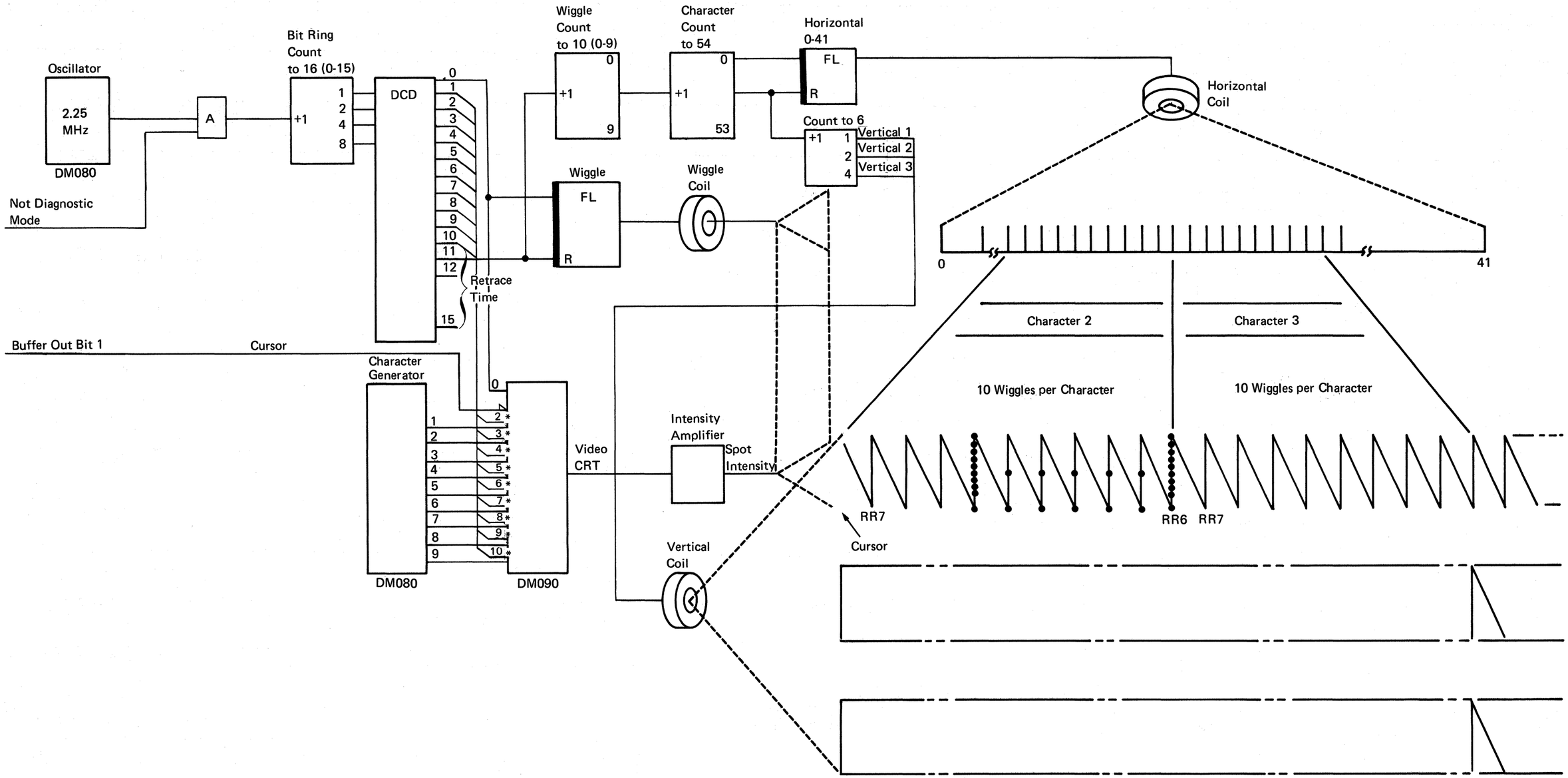
LSAR/DAR, RAM Buffer, Character Generator



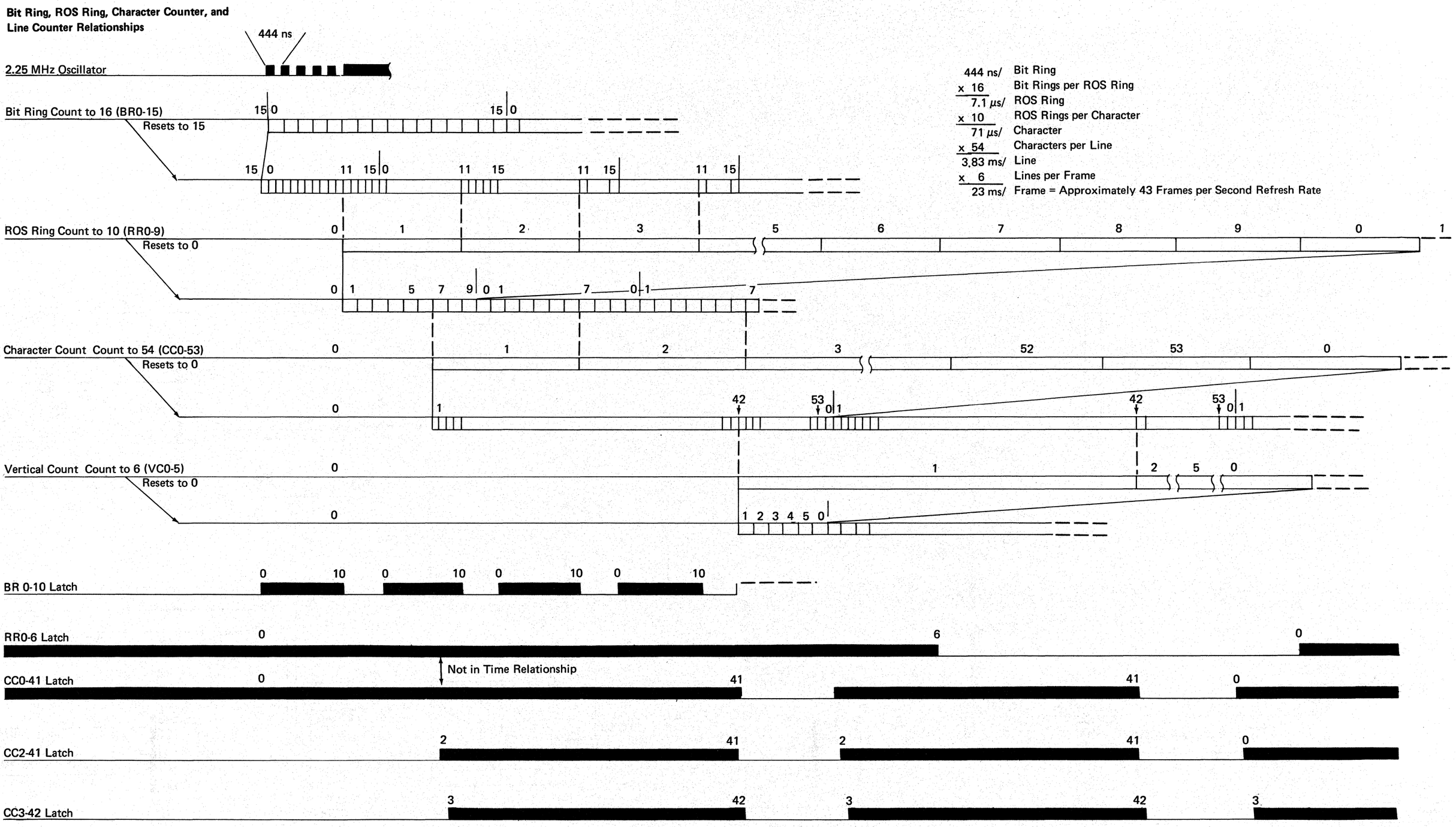
Loading Address in Address Register and 1 Byte of Data in RAM Buffer



Character Display

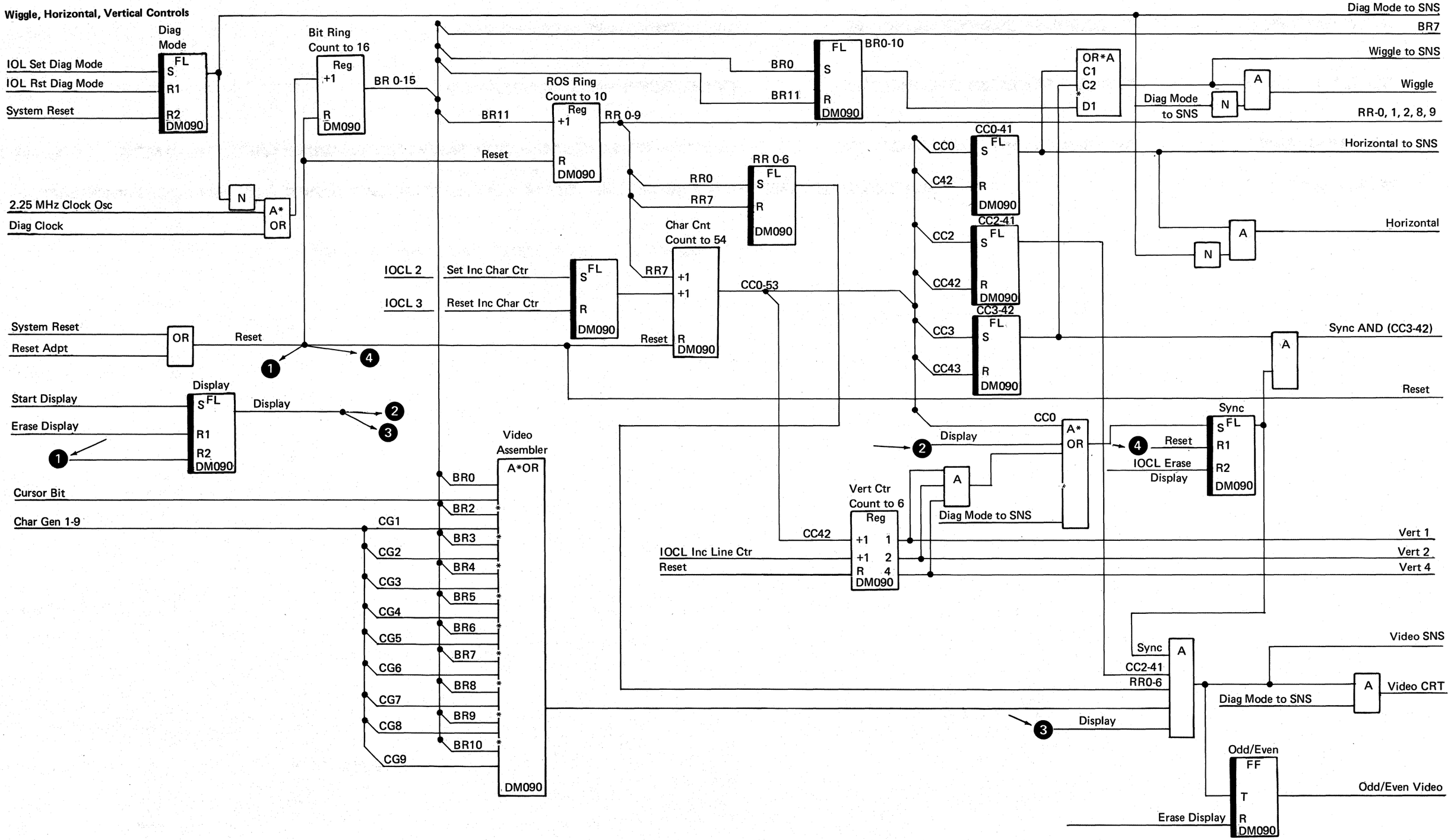


Bit Ring, ROS Ring, Character Counter, and Line Counter Relationships

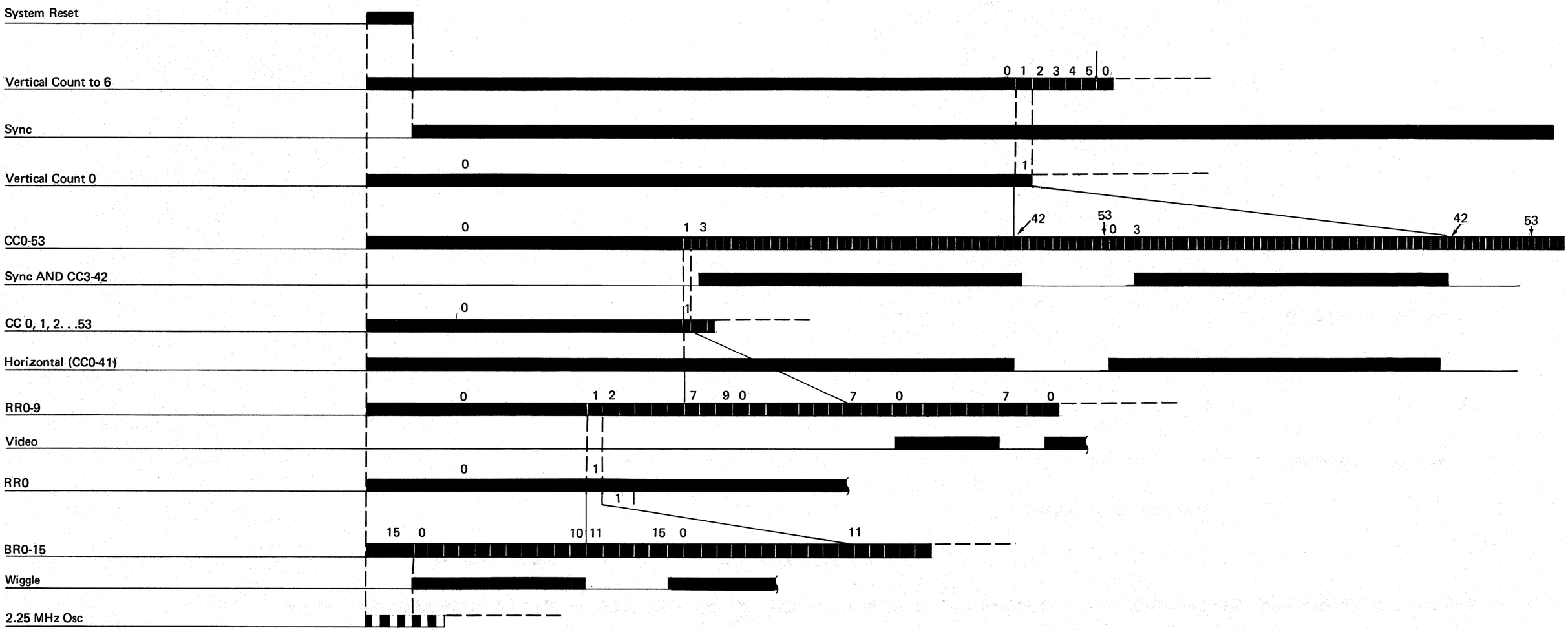


444 ns/ Bit Ring
x 16 Bit Rings per ROS Ring
7.1 µs/ ROS Ring
x 10 ROS Rings per Character
71 µs/ Character
x 54 Characters per Line
3.83 ms/ Line
x 6 Lines per Frame
23 ms/ Frame = Approximately 43 Frames per Second Refresh Rate

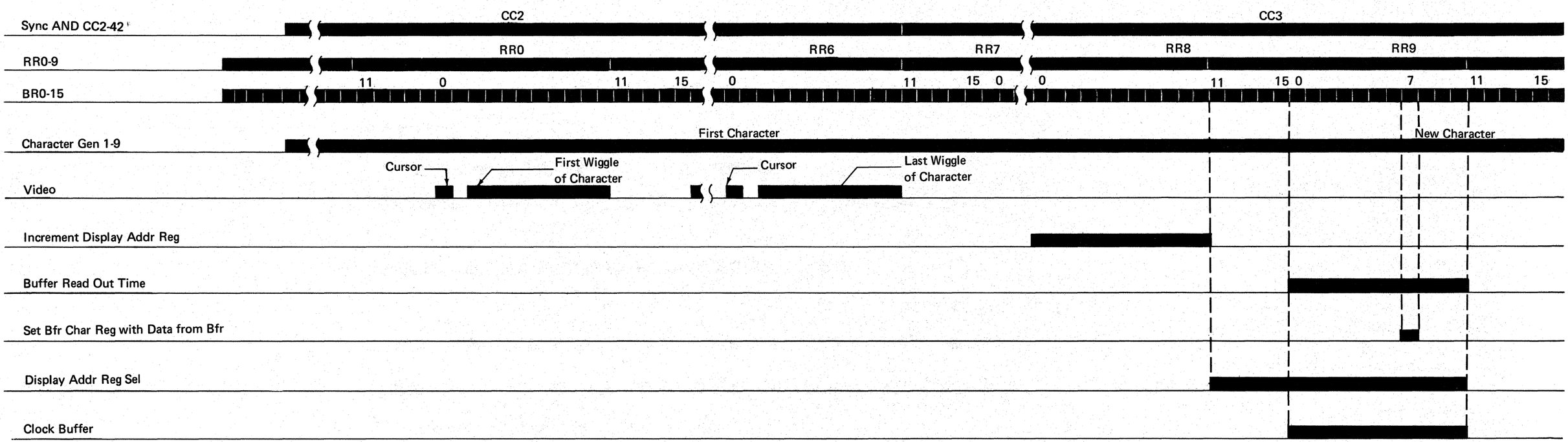
Wiggle, Horizontal, Vertical Controls



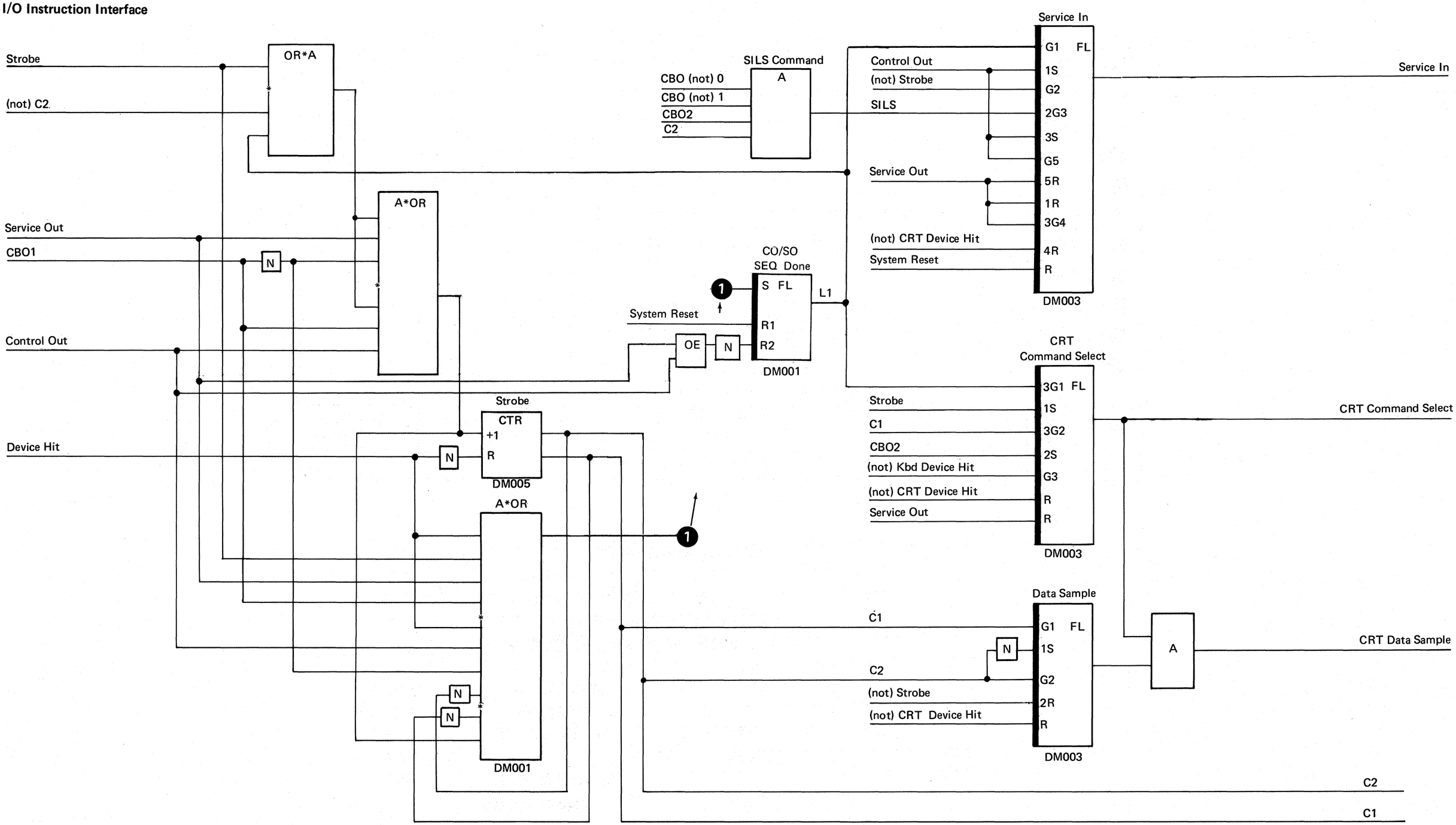
Sync, Video, Wiggle, Horizontal



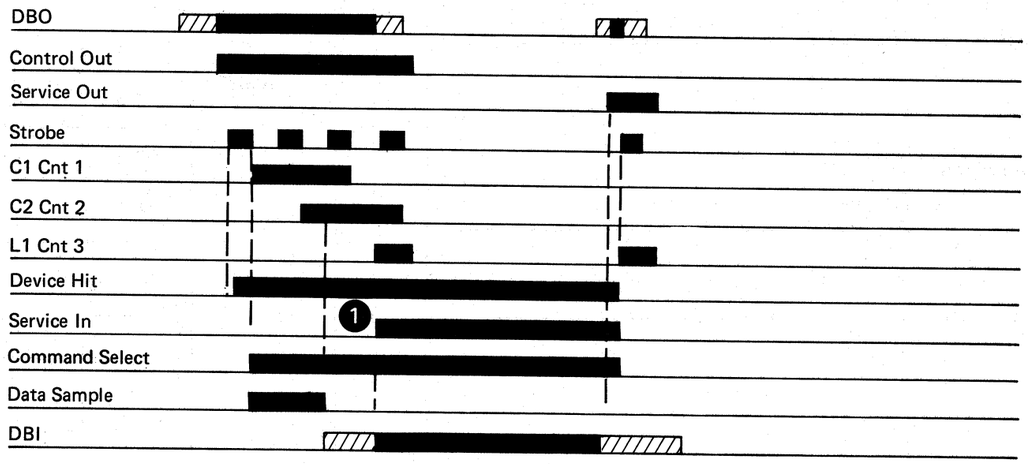
Display Buffer



I/O Instruction Interface



Control Sense Command



Modifier DBO 4, 5, 6, 7 (Hex)	DBI Data Bit	Command	Action Taken	FSL Page	Timing
0		Adapter Status 0	Conditions DBI selector to put status data on the DBI lines.	DM110	
	0	Vert 1	Turns on DBI bit 0 if 'vert 1' line is active.	DM090	1
	1	Vert 2	Turns on DBI bit 1 if 'vert 2' line is active.	DM090	1
1		Adapter Status 1	Conditions DBI selector to put status data on the DBI lines.	DM090	1
	0	Vert 4	Turns on DBI bit 0 if 'vert 4' line is active.	DM090	1
	1	Video	Turns on DBI bit 1 if 'video sense' line is active.	DM090	1
2		Adapter Status 2	Conditions the DBI selector to put status data on the DBI lines.	DM110	1
	0	Diagnostic Mode	Turns on DBI bit 0 if 'diagnostic mode' latch is set.	DM090	1
	1	Odd/Even Video	Turns on DBI bit 1 if 'odd/even' latch is on which indicates odd count.	DM090	1
3		Adapter Status 3	Conditions DBI selector to put status data on the DBI lines.	DM090	1
	0	Horizontal	Turns on DBI bit 0 if 'horizontal sense' is active.	DM090	1
	1	Wiggle	Turns on DBI bit 1 if 'wiggle sense' is active.	DM090	1

Load, Control Load Timing

Load Command

Channel

System Bus Out

8 11

Micro Instruction Function Field Decode

0 0 0 0

PH110

1 0 0

0 2

CBO

Data Buffer

Port Data Bus Out

PH070

4-7

DA 0-3

Device Address Hit

Select Attachment

Mod 4-7

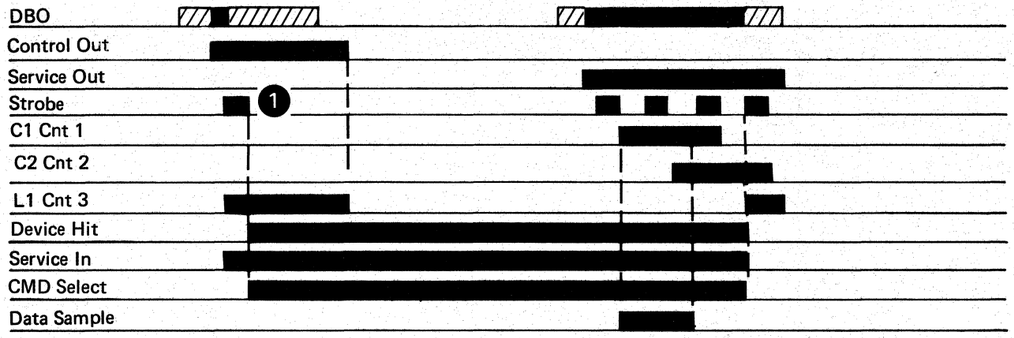
Send Data Byte to Attachment
DBO 0-7

CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
100									
	1 0 0 1 Load Bfr	Note 1 → Data							
	1 0 1 0 Load LD/SNS Addr Reg	Address Data							
	1 0 1 1 Set Diag Mode	Note 2							
	1 1 0 0 Reset Diag Mode	Note 2							
	1 1 0 1 Diag Clock	Note 2							

See μINSTR-30.

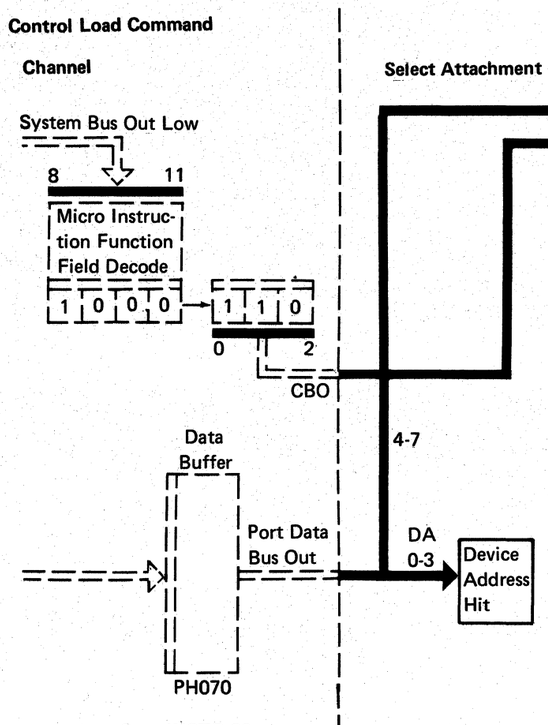
Notes:
1. Data out to buffer per address in load/sense address register.
2. Issue only when in diagnostic mode.

Load Command



Modifier DBO 4, 5, 6, 7 (Hex)	DBO Data Bit	Command	Action Taken	FSL Location	Timing
9	0-7	Data Out Buffer	1. Activates 'clock bfr', which increments the buffer. 2. Sets 'DAR invalid' latch at RR0 or RR9 time when 'sync AND CC3-42' is active. 3. Activates 'bfr read/write', which causes the buffer to store the data supplied on the DBO lines. 4. Causes data from the DBO lines to be put in the buffer.	DM070	
A	0-7	Buffer Address Out	1. Causes data from the DBO to be put in the load/sense address register. 2. Conditions the load/sense address register to accept data.	DM070	
B		Set Diagnostic Mode[1]	Sets diagnostic mode latch.	DM090	1
C		Reset Diagnostic Mode[1]	Resets diagnostic mode latch.	DM090	1
D		Diagnostic Clock[1]	Increments count to 16 register to provide controlled stepping of the 'video', 'horizontal', 'vertical', and 'wiggle' lines so they can be sensed.	DM090	1

[1] Use only when in diagnostic mode.



See μINSTR-30.

Notes:

1. Used only when in the diagnostic mode.
2. Blanks video only and does not alter data in the buffer.

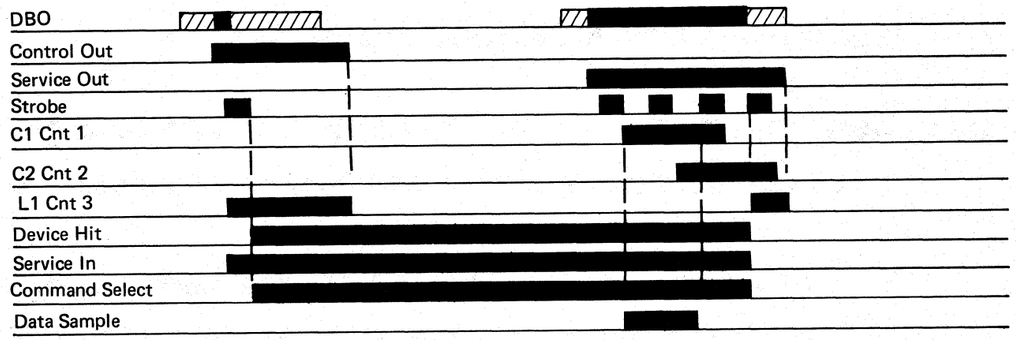
Select Attachment

Send Data Byte to Attachment
DBO 0-7

Mod 4-7

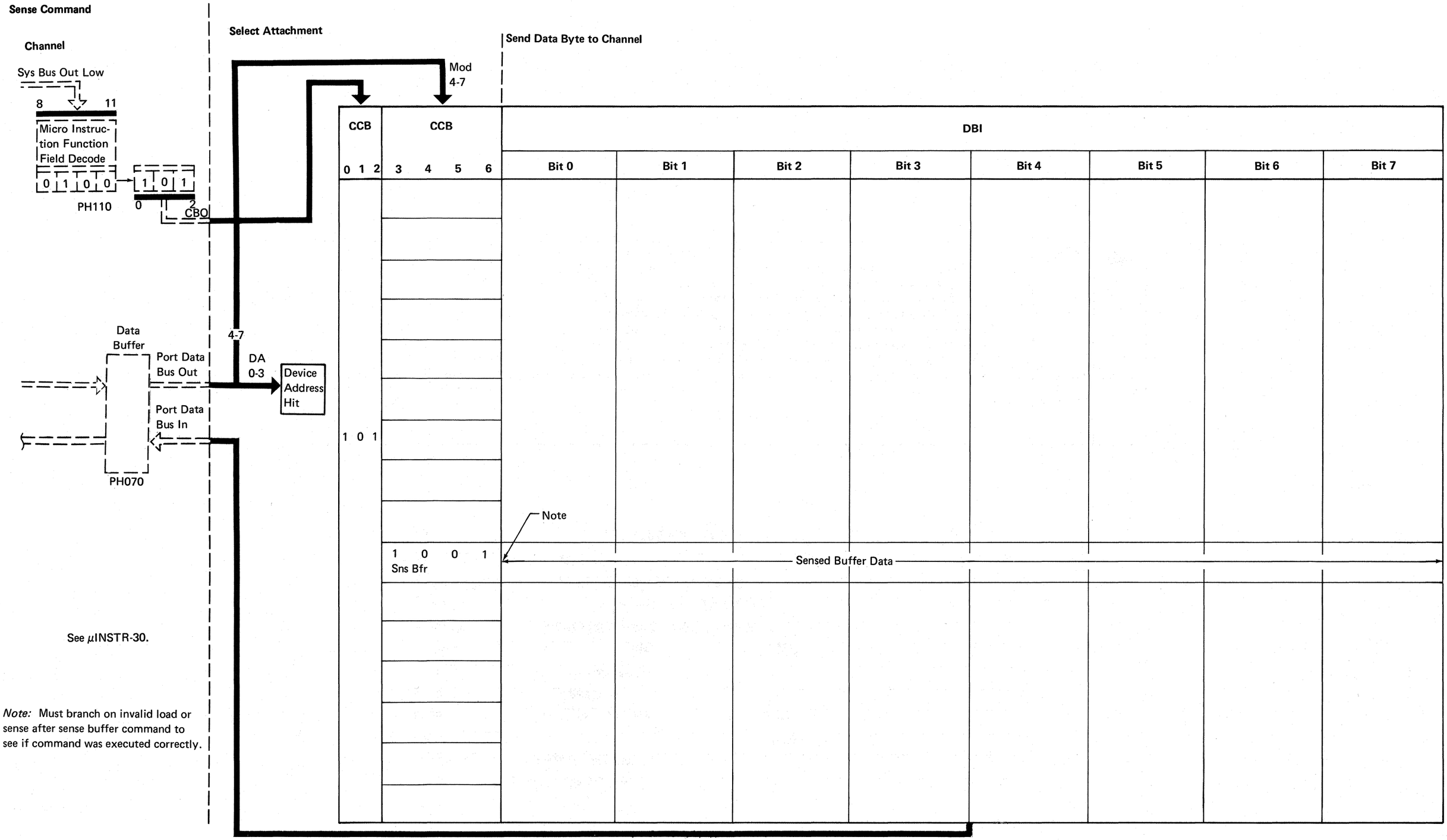
CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
	0 0 0 0 Adapter Cntrl	INC LD/SNS Adr Reg	INC Display Adr Reg	Reset LD/SNS Adr Reg	Reset Display Adr Reg				
	0 0 0 1 Inc Line Cntr	← Note 1							
	0 0 1 0 Set Inc Char Ctr	← Note 1							
	0 0 1 1 Reset Inc Char Ctr	← Note 1							
	0 1 0 0 Reset Adapt								
	0 1 0 1 Start Display								
	0 1 1 0 Erase Display	← Note 2							
110									

Control Load Command



Modifier DBO 4, 5, 6, 7 (Hex)	DBO Data Bit	Command	Action Taken	FSL Location
0		Adapter Control	Conditions DBO selector to accept command data.	DM110
	0	Increment Load/Sense Address Register	Increments the load/sense address register which addresses the characters into the RAM buffer for loading the character register.	DM070
	1	Increment Display Address Register	Increments the display address register which addresses the characters in the RAM buffer for display of any of 240 characters.	DM070
	2	Reset Load/Sense Address Register	Resets the load/sense address register.	DM070
	3	Reset Display Address Register	Resets the display address register.	DM070
1		Increment Line Counter	Increments line counter to advance to the next display line.	DM090
2		Set Increment Character Counter	Sets 'increment character counter' latch which increments the character counter. This command is used only when in the diagnostic mode (must issue a reset increment character counter after a set increment character counter.	DM090
3		Reset Increment Character Counter	Resets 'increment character counter' latch. This command is used only when in the diagnostic mode.	DM090
5		Start Display	Sets the 'start display' latch. The 'start display' latch AND CC0 sets the 'sync' latch which activates the 'video' line.	DM090
6		Erase Display	Resets 'display' latch so 'video' line is not active; only blanks video, does not alter data in the buffer.	DM090

Timing for Sense, Control Sense, and Jump Commands

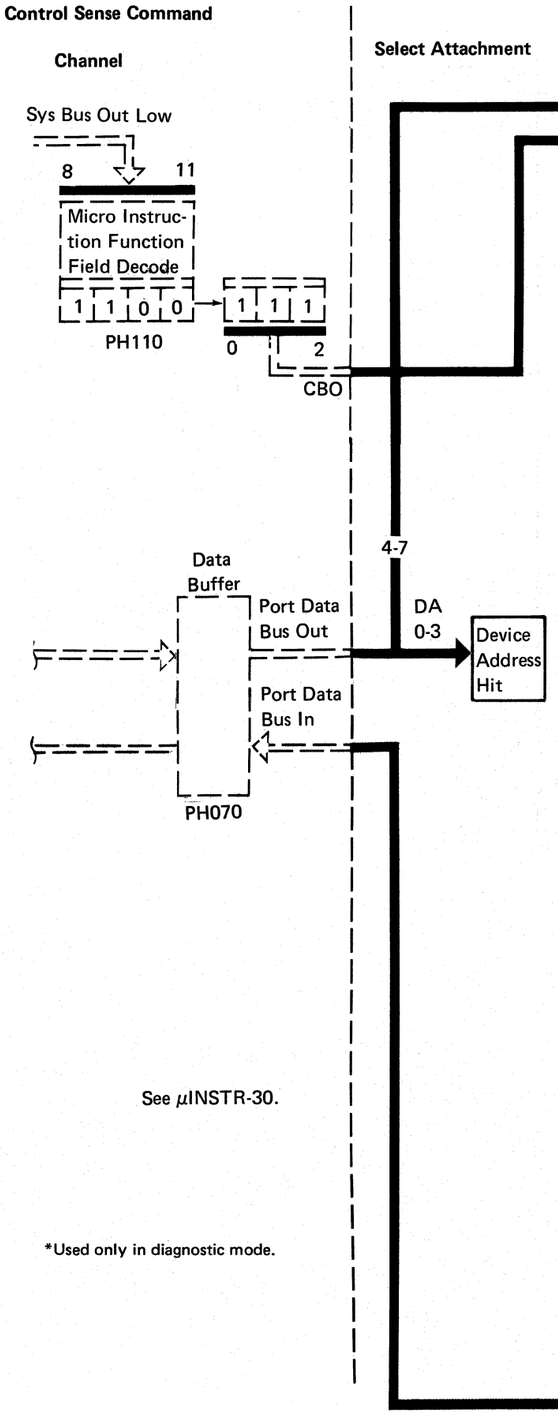


See μINSTR-30.

Note: Must branch on invalid load or sense after sense buffer command to see if command was executed correctly.

Sense Command

Modifier DBO 4, 5, 6, 7 (Hex)	DBI Data Bit	Command	Action Taken	FSL Page	Timing
9	0-7	Sense Buffer	Conditions 'clock bfr' which allows data to be read out of the 240 x 9 RAM buffer at data sample time and loaded into the DBI assembler. Data is put on the DBI lines, 'clock bfr' will not come up if the command is given while data is changing in the buffer at (RR0 OR RR9) and (CC3-42 AND sync) time. If buffer data is changing while sense buffer command is being executed, the 'invalid load/sense' latch is set. A sense buffer command must be followed with a jump on invalid load/sense command to determine if the sense buffer command was executed.	DM070	1



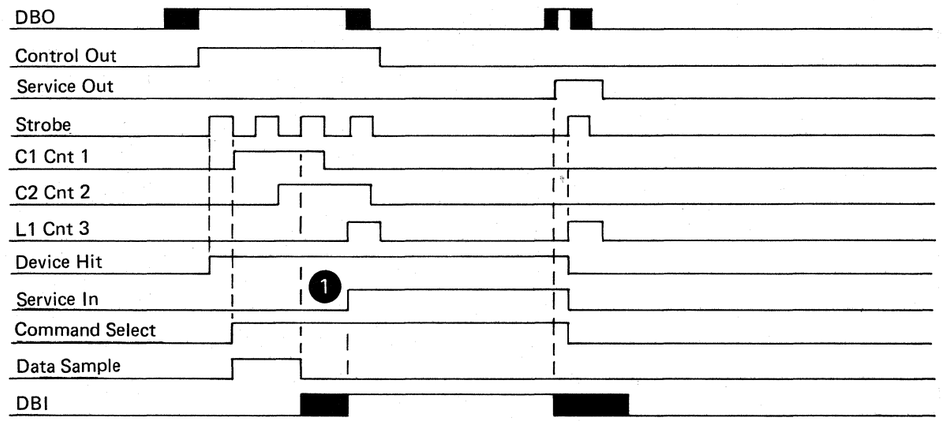
See μINSTR-30.

*Used only in diagnostic mode.

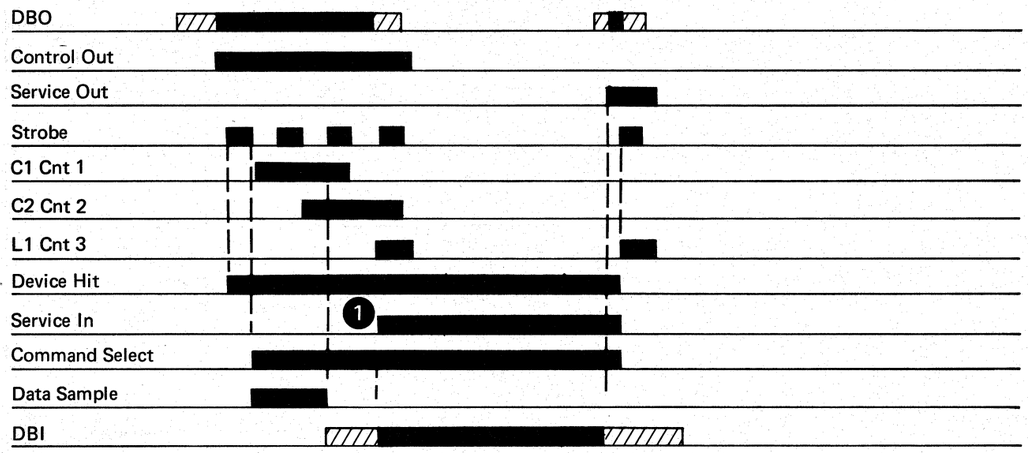
Send Data Byte to Channel

CCB 0 1 2	CCB 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
111	0 0 0 0 Adapt Status 0*	Vert 1	Vert 2						
	0 0 0 1 Adapt Status 1*	Vert 4	Video CRT						
	0 0 1 0 Adapt Status 2*	Diag Mode	Odd/Even						
	0 0 1 1 Adapt Status 3*	Horizontal	Wiggle						
	0 1 0 0 SNS LD/SNS Addr Reg*	LD/SNS Adr Reg 7	LD/SNS Adr Reg 6	LD/SNS Adr Reg 5	LD/SNS Adr Reg 4	LD/SNS Adr Reg 3	LD/SNS Adr Reg 2	LD/SNS Adr Reg 1	LD/SNS Adr Reg 0
	0 1 0 1 SNS Disp Addr Reg*	Display Adr Reg 0	Display Adr Reg 1	Display Adr Reg 2	Display Adr Reg 3	Display Adr Reg 4	Display Adr Reg 5	Display Adr Reg 6	Display Adr Reg 7

Control Sense Command

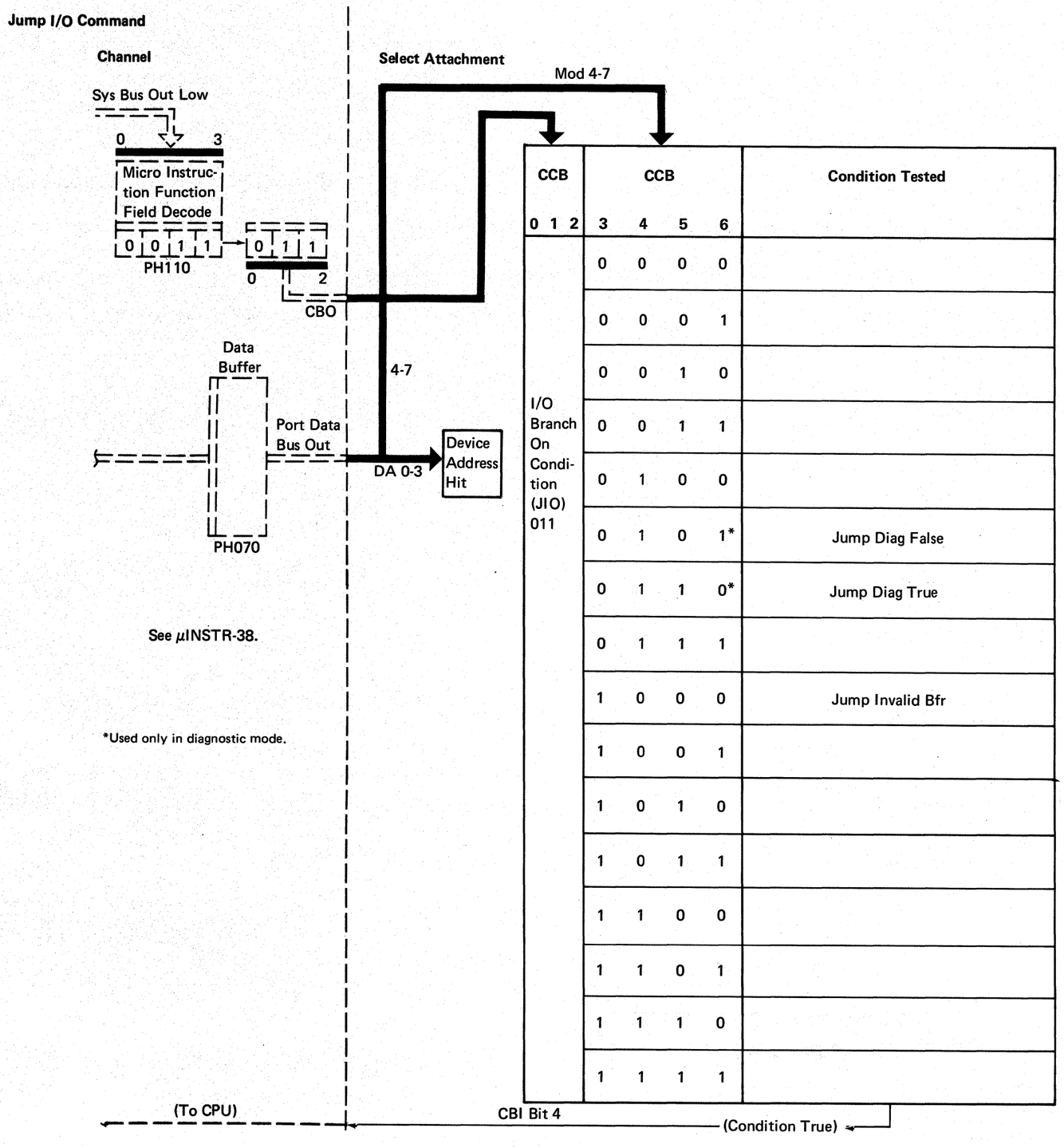


Modifier DBO 4 5 6 7 Hex	DBI Data Bit	Command	Action Taken	FSL Page	Timing
0		Adapter Status 0	Conditions DBI selector to put status data on the DBI lines.	DM110	
	0	Vert 1	Turns on DBI bit 0 if 'vert 1' line is active.	DM090	1
	1	Vert 2	Turns on DBI bit 1 if 'vert 2' line is active.	DM090	1
1		Adapter Status 1	Conditions DBI selector to put status data on the DBI lines.	DM090	1
	0	Vert 4	Turns on DBI bit 0 if 'vert 4' line is active.	DM090	1
	1	Video	Turns on DBI bit 1 if 'video sense' line is active.	DM090	1
2		Adapter Status 2	Conditions the DBI selector to put status data on the DBI lines.	DM110	1
	0	Diagnostic Mode	Turns on DBI bit 0 if 'diagnostic mode' latch is set.	DM090	1
	1	Odd/Even Video	Turns on DBO bit 1 if 'odd/even' latch is on which indicates odd count.	DM090	1
3		Adapter Status 3	Conditions DBI selector to put status data on the DBI lines.	DM090	1
	0	Horizontal	Turns on DBI bit 0 if 'horizontal sense' is active.	DM090	1
	1	Wiggle	Turns on DBI bit 1 if 'wiggle sense' is active.	DM090	1



Modifier DBO 4, 5, 6, 7 Hex	DBI Data Bit	Command	Action Taken	FSL Page	Timing
4	0-7	Sense Load/Sense Address Register	1. Conditions the DBI selector to put address stored in the load/sense address register on DBI.	DM100	1
			2. Conditions the load/sense address register select to provide data (the address stored in the load/sense address register) to the DBI selector.	DM070	1
5	0-7	Sense Display Address Register*	Conditions the DBI selector to put the address stored in the display address register on DBI. The address is moved from the display address register to the DBI selector by the display address register selector.	DM100	1

*Issue only when 'sync' latch is not set.



CCB 0 1 2	CCB 3 4 5 6	Condition Tested
I/O Branch On Condition (JIO) 011	0 0 0 0	
	0 0 0 1	
	0 0 1 0	
	0 0 1 1	
	0 1 0 0	
	0 1 0 1*	Jump Diag False
	0 1 1 0*	Jump Diag True
	0 1 1 1	
	1 0 0 0	Jump Invalid Bfr
	1 0 0 1	
	1 0 1 0	
	1 0 1 1	
	1 1 0 0	
	1 1 0 1	
	1 1 1 0	
	1 1 1 1	

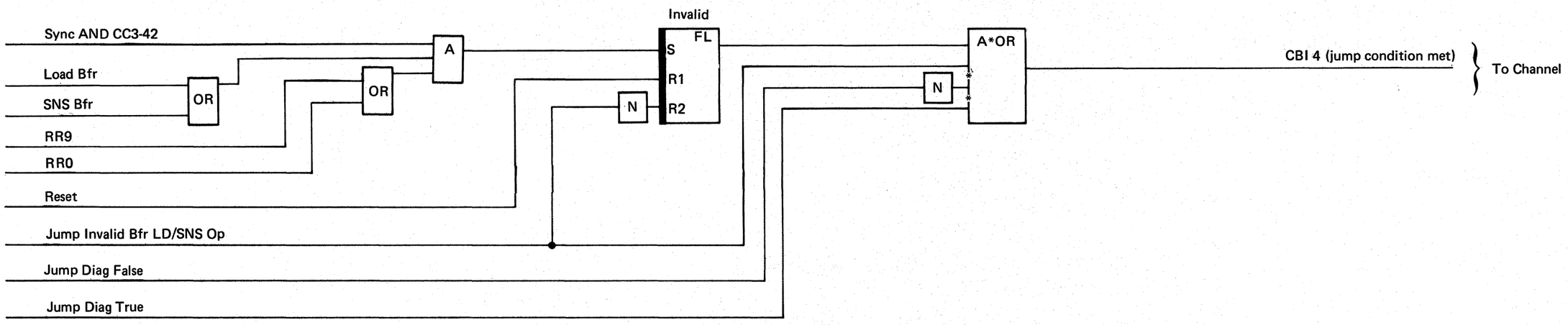
Jump I/O Command

Modifier DBO 4, 5, 6, 7 Hex	DBI Data Bit	Command	Action Taken	FSL Page	Timing
5		Diagnostic Jump False	Diagnostic command that does not activate CBI bit 4.	DM070	
6		Diagnostic Jump True	Diagnostic command to activate DBI bit 4 to test the ability of CBI bit 4 to switch.	DM070	1
8		Jump Invalid Buffer	Used with 'invalid load/sense' latch (and if 'load/sense' latch is set) to activate CBI bit 4. 'Invalid load/sense' latch is set with (RR0 or RR9) AND CC3-42 AND a load buffer or sense buffer command.	DM070	1

CBI 4 Function

During a jump invalid buffer load/sense command, CBI 4 is active when 'invalid' latch has been set. 'Invalid' latch is set when an attempt has been made to load or sense the buffer during the time the buffer is in a read mode to read a new character to the character register to satisfy the display. This tells the CPU that the data was not loaded properly.

During a diagnostic jump true command, CBI 4 goes active and during a diagnostic jump false command, CBI 4 stays inactive. This is for diagnostic purposes to guarantee that the line will switch from active to inactive.



Keyboard Attachment

The keyboard attachment occupies the same card as the display screen attachment. Both attachments use the same:

- CBO (command bus out)
- DBO (port data bus out)
- CBI (command bus in)
- DBI (port data bus in)

Only one of these attachments uses the lines at any time. Which attachment uses the lines is determined by the address in WR0(L) which is subsequently placed on the DBO lines 0-3.

The keyboard attachment has four main operations:

1. Interface with the channel to execute the micro instructions.
2. Store data from the keyboard unit in the keyboard register.
3. Send data to the channel.
4. Control the keyboard unit.

The channel:

1. Places decoded micro instruction data on CBO 0-2, device address on DBO 0-3, and micro instruction modifier data on DBO 4-7.
2. Activates 'control out' to indicate that a command is on the channel.

Each attachment checks the address; if it is the keyboard attachment address, the attachment activates 'kbd command select' so that the keyboard attachment can accept the command.

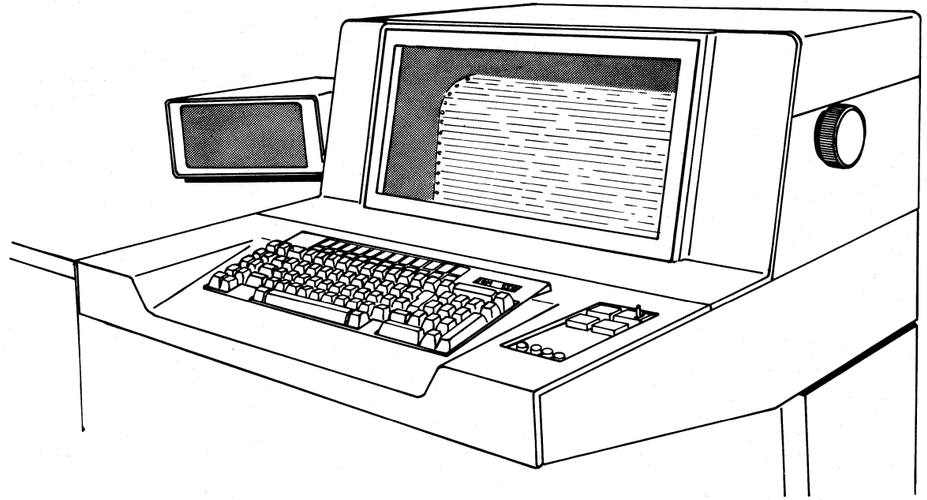
If the command is sense, control sense, or sense interrupt level status byte, data from the keyboard register or the status of the latches is placed on the DBI lines. The jump command places data on CBI 4. The attachment brings up 'service in' to indicate to the channel that the data is on DBI (CBI for jump command). The channel accepts the data and responds with 'service out' to indicate that the data was received. The attachment then drops 'kbd command select' and completes communication with the channel.

If the command is a load or control load, the attachment again checks the device address and raises 'kbd command select'. The attachment sets or resets latches per the command and responds with 'service in' to indicate that the command was accepted. The channel responds with 'service out' to indicate that the data on DBO is now valid. The attachment then activates 'data sample' which gates data on DBO to additional latches or to the keyboard data register. Upon the fall of 'service out' the attachment deactivates 'kbd command select' to terminate communication with the channel.

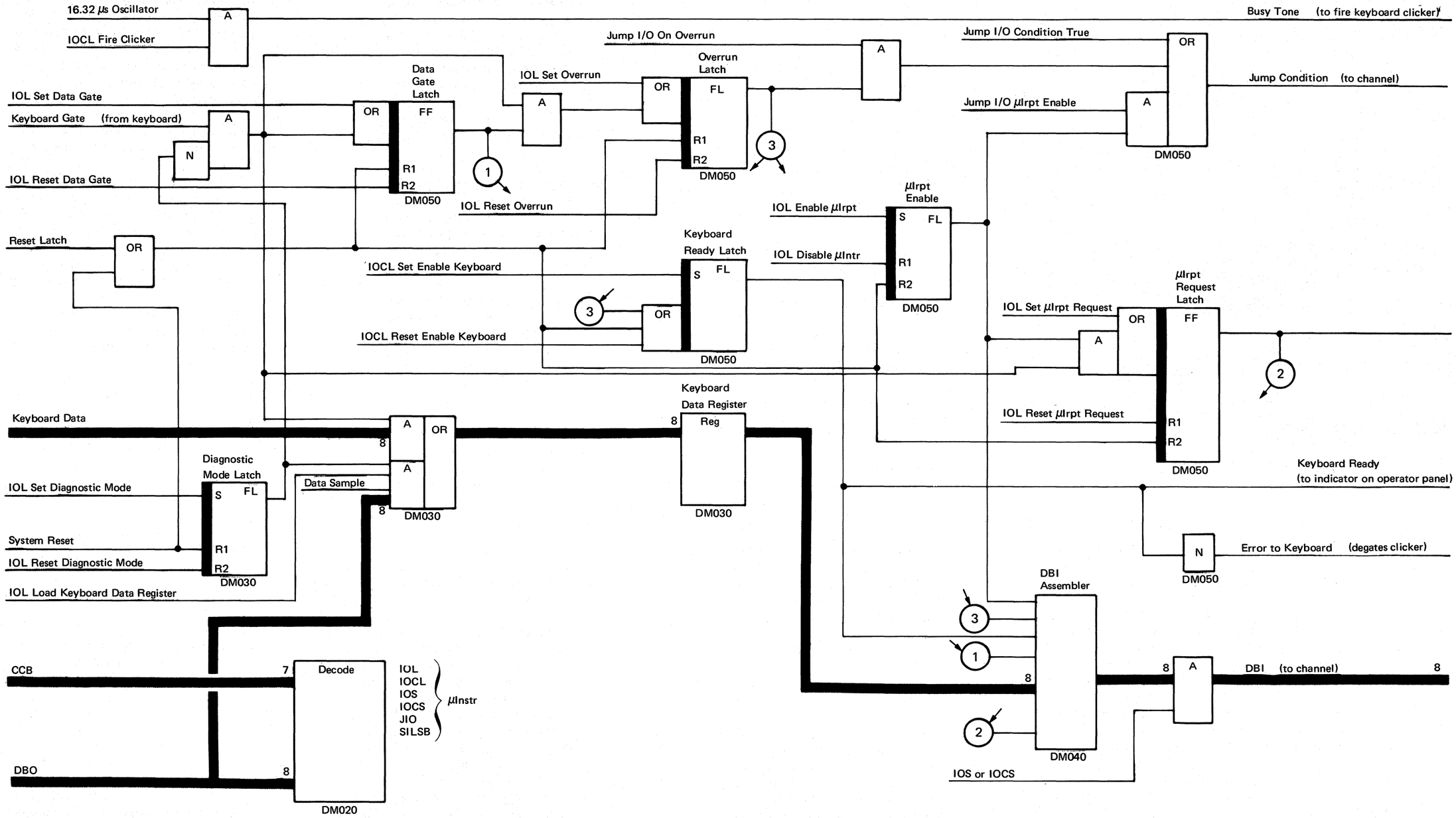
Whenever data is on DBO, the attachment checks for odd parity. If parity is not odd, the attachment activates CBI 5 to indicate that the data is bad.

Attachment Functions

1. The attachment interfaces with the channel to execute the proper micro instructions as follows:
   - Accepts the channel out lines to establish communication with the channel.
   - Recognizes and accepts the keyboard attachment address of 0001.
   - Decodes the CBO lines to determine what micro instructions are being sent to the channel.
   - Accepts only valid micro instructions.
   - Decodes DBO 4-7 micro instruction modifier bits to determine conditions to be established.
   - Indicates to the channel by raising 'service in' that the command has been accepted.
2. The attachment stores data from the keyboard as follows:
   - Pressing a key on the keyboard unit activates 'keyboard gate' and sets the data gate latch (providing the diagnostic mode latch is not set).
   - 'Kybd gate not diag' gates the data from the keystroke into the keyboard data register so that the data can be sensed later.
   - 'Kybd gate not diag' sets the micro interrupt request latch if the keyboard micro interrupt enable latch is set.
   - The micro interrupt request latch is sensed with a sense interrupt level status byte command to determine that data is ready to be transferred to the channel.
3. The attachment sends data to the channel as follows:
   - Data is supplied to the channel through the data buffer to the channel DBI.
   - The data is gated through DBI select by one of the nine gates created by decoding the modifier of an IOS, IOCS, or SILSB command.
   - The data comes from one of the following sources:
     a. Keyboard data register: this data is collected from the keyboard unit. Each time data is sensed from the keyboard data register, the keyboard data register and the data gate latch are reset. Also, the overrun latch is tested. If overrun is set, data is discarded and an error condition is indicated.
     b. Sensing the latches: these latches are set or reset by previous commands or by conditions detected in the attachment.
     c. Diagnostic sense micro instructions gating certain established configurations to DBI. This data is for diagnostics.
4. The attachment controls the keyboard unit to:
   - Allow the clicker to fire when the keyboard is disabled. (The 'error' line to the keyboard degates the clicker.) An IOCL command sets the fire clicker latch. This latch, along with the 16.384 ms oscillator line from the CPU, provides a pulse on the 'clicker' line to the keyboard unit so that it can emit a click.
   - Resets the keyboard. An IOCL command sets or resets the keyboard reset latch. (A 'system reset' also resets the keyboard.) A keyboard reset latch being set or 'system reset' sets 'kybd device rst' to the keyboard unit.
   - Enable the keyboard clicker and degate the 'error' line to the keyboard.



Keyboard Attachment Data Flow



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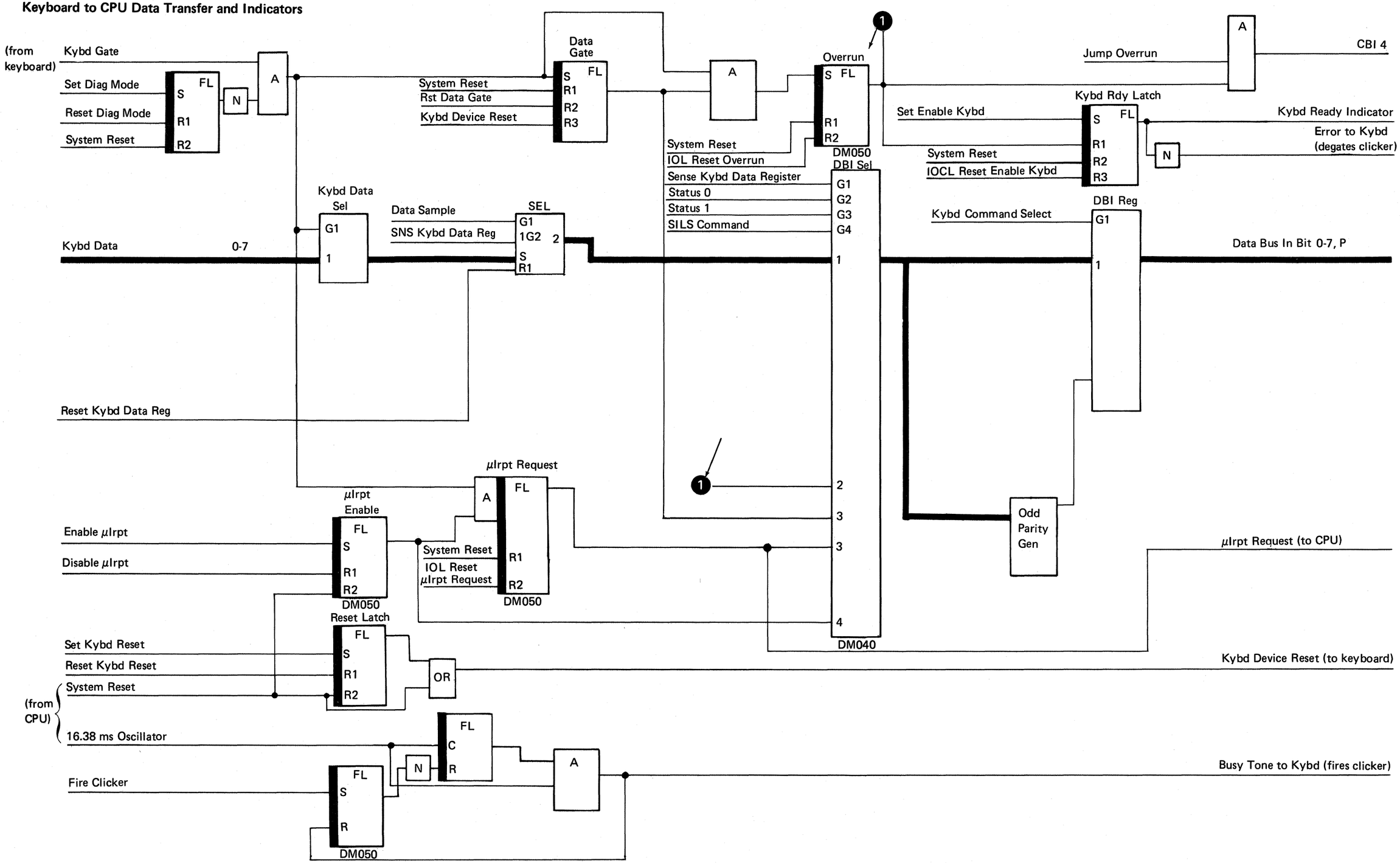
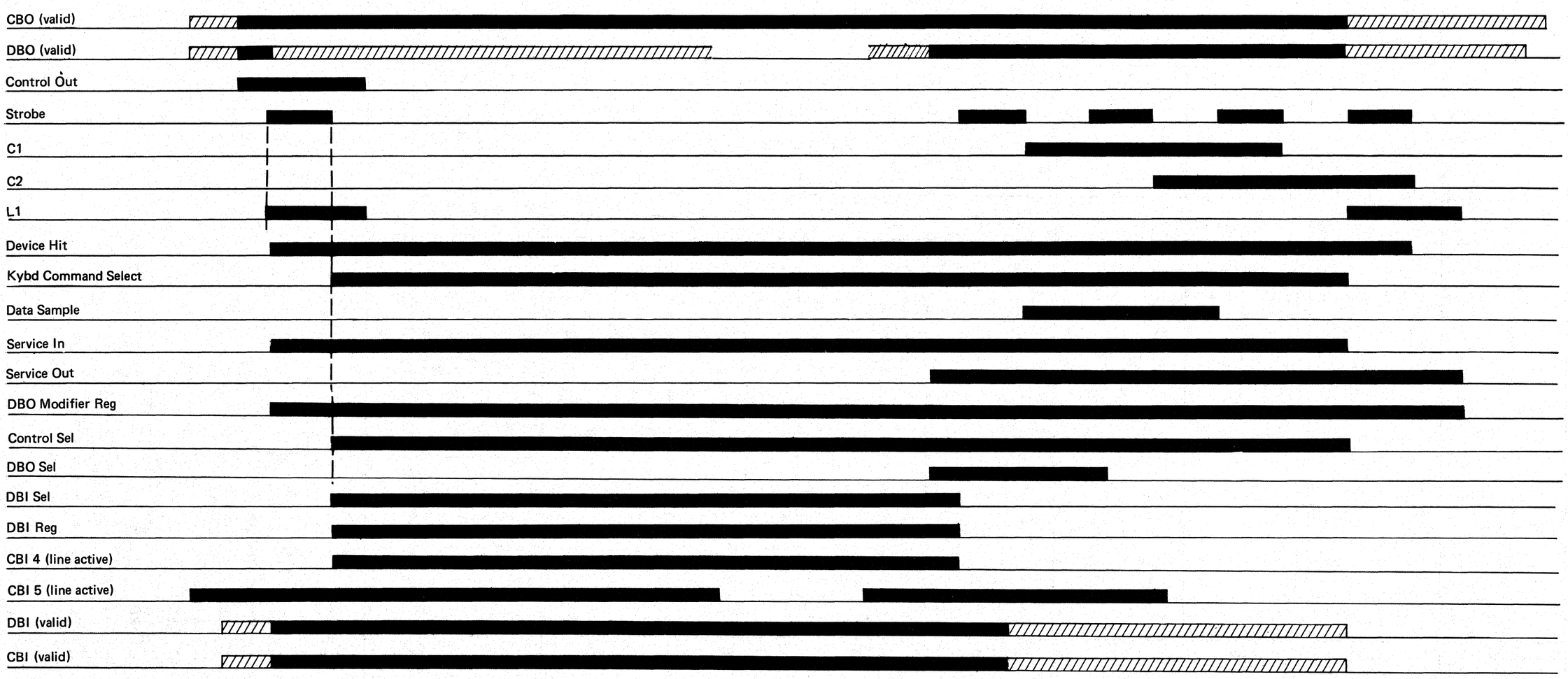
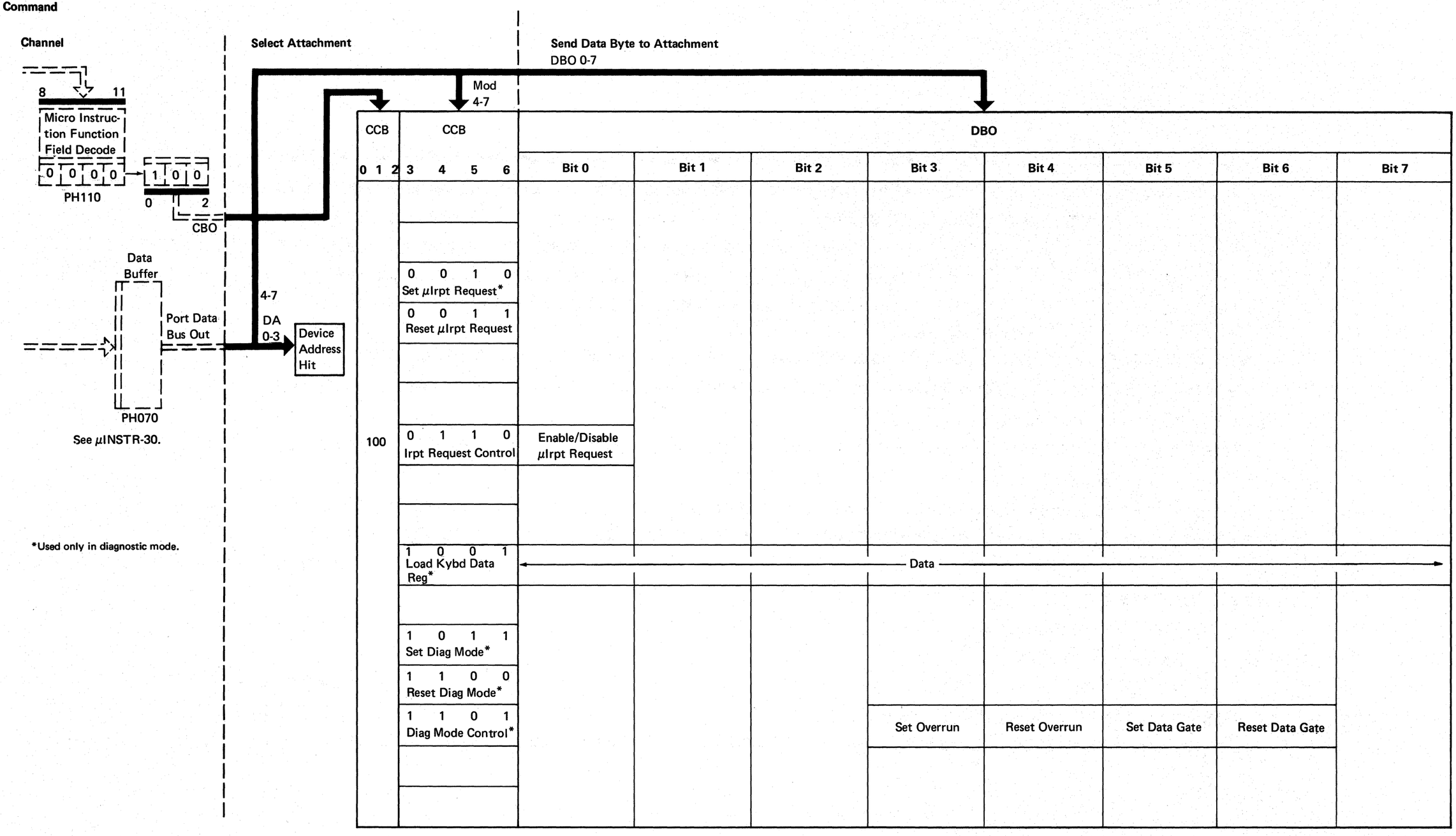
Keyboard to CPU Data Transfer and Indicators



Load, Control Load Timing



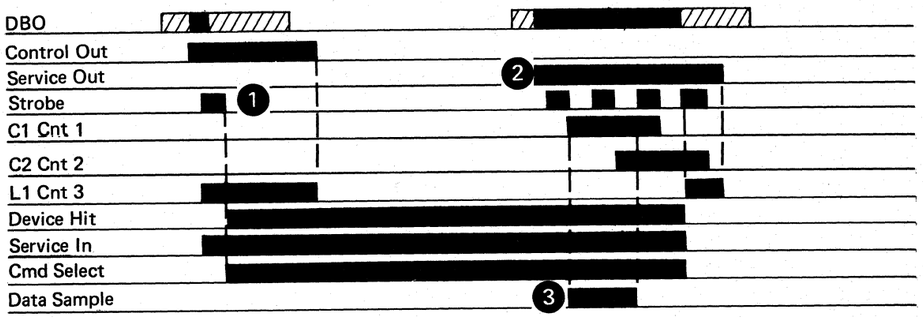
Load Command



See µINSTR-30.

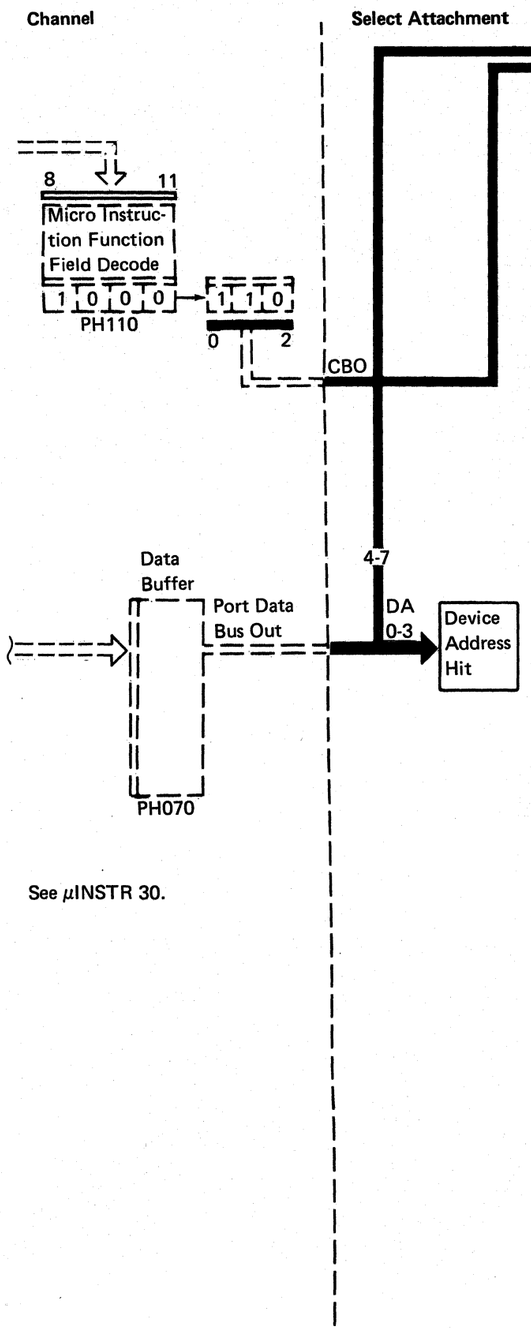
*Used only in diagnostic mode.

Load Command



Modifier DBO 4, 5, 6, 7 Hex	DBO Data Bit	Command	Action Taken	FSL Location	Timing
2		Set Micro Interrupt Request	Sets micro interrupt request latch.	DM050	1
3		Reset Micro Interrupt Request	Resets micro interrupt request latch.	DM050	1
6	1	Enable Interrupt Request	Sets enable interrupt request latch.	DM050	2
	0	Disable Interrupt Request	Resets enable interrupt request latch.	DM050	2
9	0-7	Load Keyboard Data Register	Conditions DBO select to enter data from DBO to the keyboard select.	DM020	3
B		Set Diagnostic Mode	Sets 'diagnostic mode' latch.	DM030	1
C		Reset Diagnostic Mode	Resets 'diagnostic mode' latch.	DM030	1
D		Diagnostic Mode Control	Controls diagnostic mode.	DM030	
	3	Set Overrun	Sets 'overrun' latch.	DM050	2
	4	Reset Overrun	Resets 'overrun' latch.	DM050	2
	5	Set Data Gate Latch	Sets 'data gate' latch.	DM050	2
	6	Resets Data Gate Latch	Resets 'data gate' latch.	DM050	2

Control Load Command



See μINSTR 30.

CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
110	0 0 0 0 Misc Control	Set Enable Kybd	Reset Enable Kybd	Reset Kybd Data Reg	Reset Overrun Latch	Reset Data Gate Latch		Set Kybd Reset	Reset Kybd Reset
	0 0 0 1 Fire Clicker								

Control Load Command

Modifier DBO 4, 5, 6, 7 Hex	DBO Data Bit	Command	Action Taken	FSL Location	Timing
0		Adapter Control			
	0	Enable Keyboard	Sets 'enable keyboard' latch.	DM050	2
	1	Disable Keyboard	Resets 'enable keyboard' latch.	DM050	2
	2	Reset Data Register	Resets keyboard data register.	DM030	2
	3	Reset Overrun Latch	Resets 'overrun' latch.	DM050	2
	4	Reset Data Gate Latch	Resets 'data gate' latch.	DM050	2
	6	Set Reset Latch	Sets 'keyboard reset' latch.	DM050	2
	7	Reset Reset Latch	Resets 'keyboard reset' latch.	DM050	2
1		Fire Clicker	Sets 'fire clicker' latch (fires clicker once each time issued).	DM050	1

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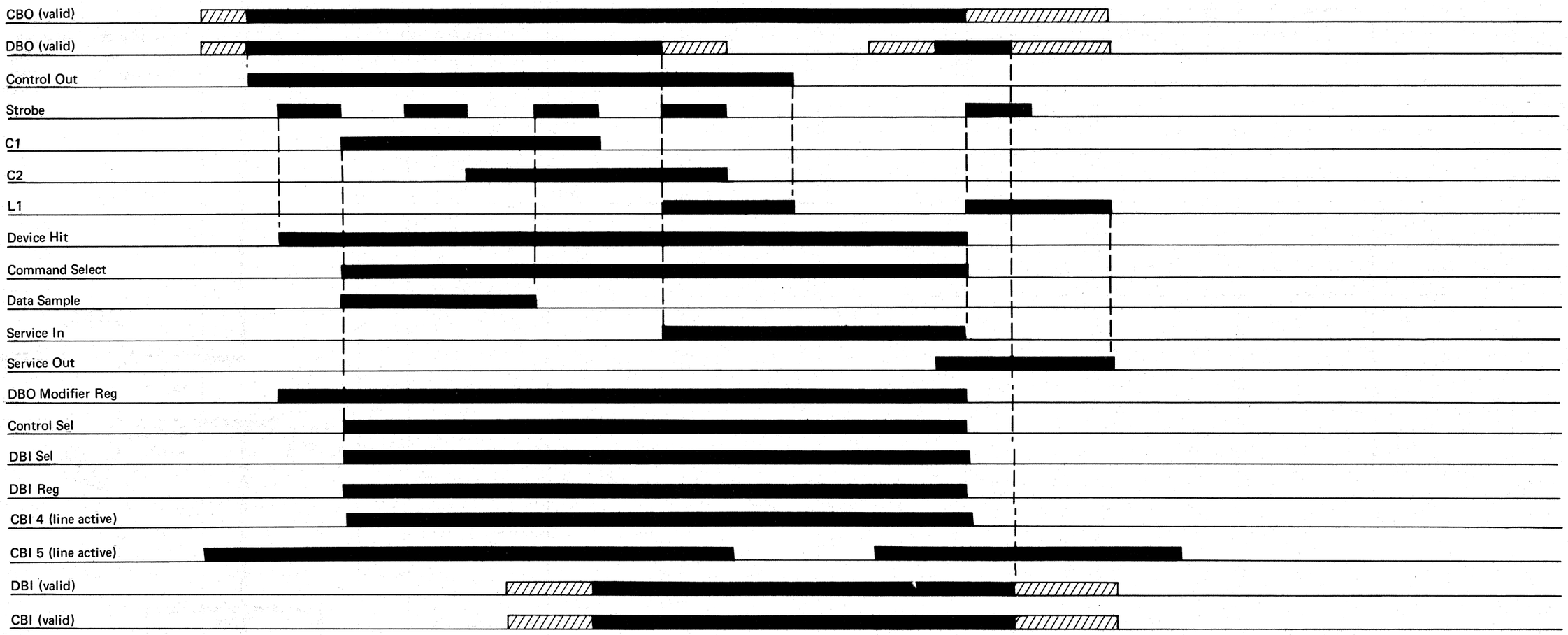
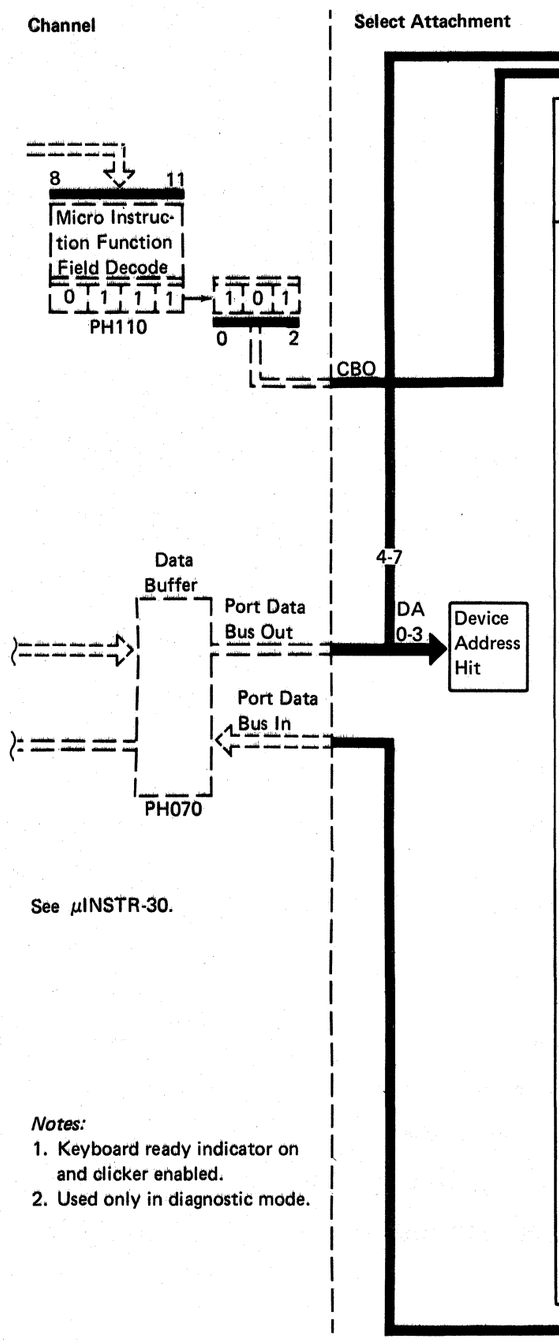
Sense, Control Sense, Jump I/O and SILSB Timing



Sense Command



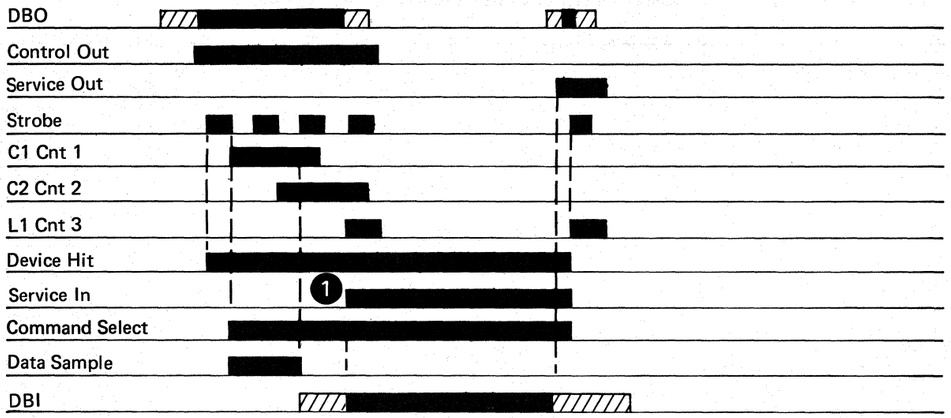
See μINSTR-30.

Notes:

1. Keyboard ready indicator on and clicker enabled.
2. Used only in diagnostic mode.

CCB 0 1 2	CCB 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
101	0 0 0 0 Adapter Status 0	Overrun							
	0 0 0 1 Adapter Status 1	Data Gate	Diag Mode	Kybd Enable	← Note 1				
	1 0 0 1 SNS Kybd Data Reg	←			← Data in from Kybd	→			
	1 0 1 1 Diag hex 00 Command	Note 2 ←			← Data hex 00	→			
	1 1 0 0 Diag hex 55 Command	Note 2 ←			← Data hex 55	→			
	1 1 0 1 Diag hex AA Command	Note 2 ←			← Data hex AA	→			
	1 1 1 0 Diag hex FE Command	Note 2 ←			← Data hex FE	→			

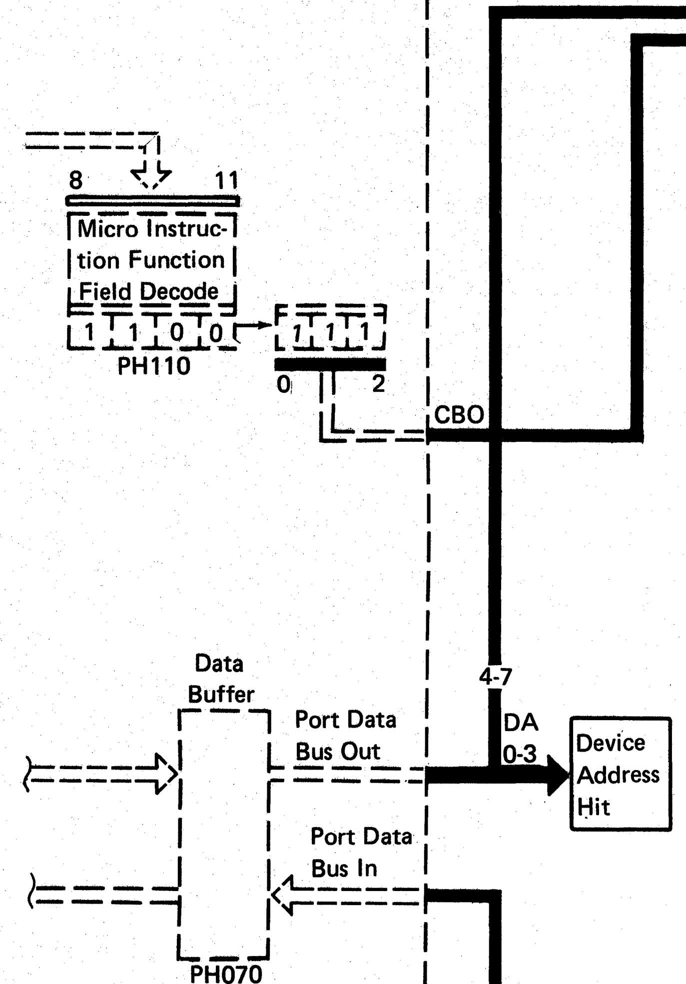
Sense Command



Modifier DBO 4, 5, 6, 7 Hex	DBI Data Bit	Command	Action Taken	FSL Page	Timing
0	0	Overrun	Conditions the DBI select to provide a 0 bit when the 'overrun' latch is set.	DM040	1
1		Adapter Status 1	Conditions the DBI select to provide bits on the DBI lines to check status of the 'data gate', 'diagnostic mode', and 'keyboard enable' latches.	DM040	
	0	Data Gate	Turns on DBI bit 0 if the 'data gate' latch is set.	DM050	1
	1	Diagnostic Mode	Turns on DBI bit 1 if the 'diagnostic mode' latch is set.	DM050	1
	2	Keyboard Enable	Turns on DBI bit 2 if the 'keyboard enable' latch is set.	DM050	1
9	0-7	Data in from Keyboard	Conditions the DBI select to provide data bits on the DBI lines. Data is taken from the keyboard register.	DM040	1
B	00	Diag hex 00	Conditions the DBI select to provide bits to DBI. Data is generated in the attachments for all four commands (one at a time). All DBI lines 0-7 are checked for switching, shorts to ground, shorts to voltage, shorts between lines, and opens.	DM040	1
C	55	Diag hex 55			
D	AA	Diag hex AA			
E	FE	Diag hex FE			

Control Sense Command

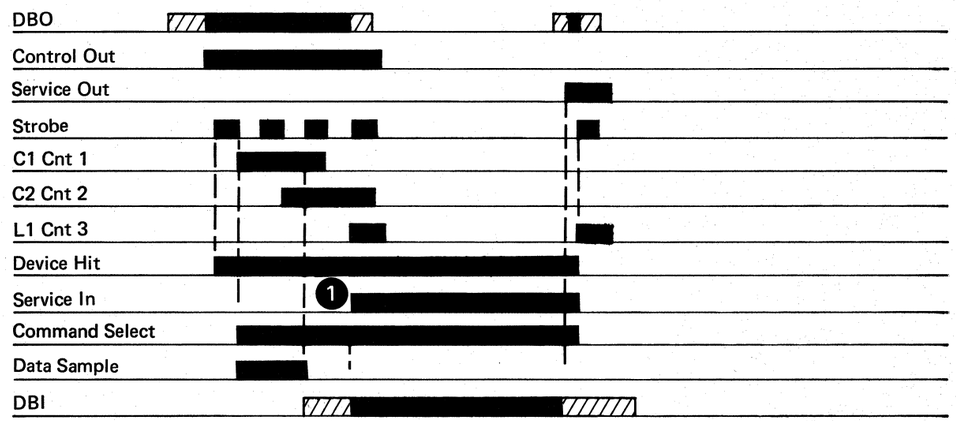
Channel | **Select Attachment** | **Send Data Byte to Channel**



CCB 0 1 2	CCB 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
1 1 1	0 0 0 0 SNS μIrpt Enable			μIrpt Enabled					

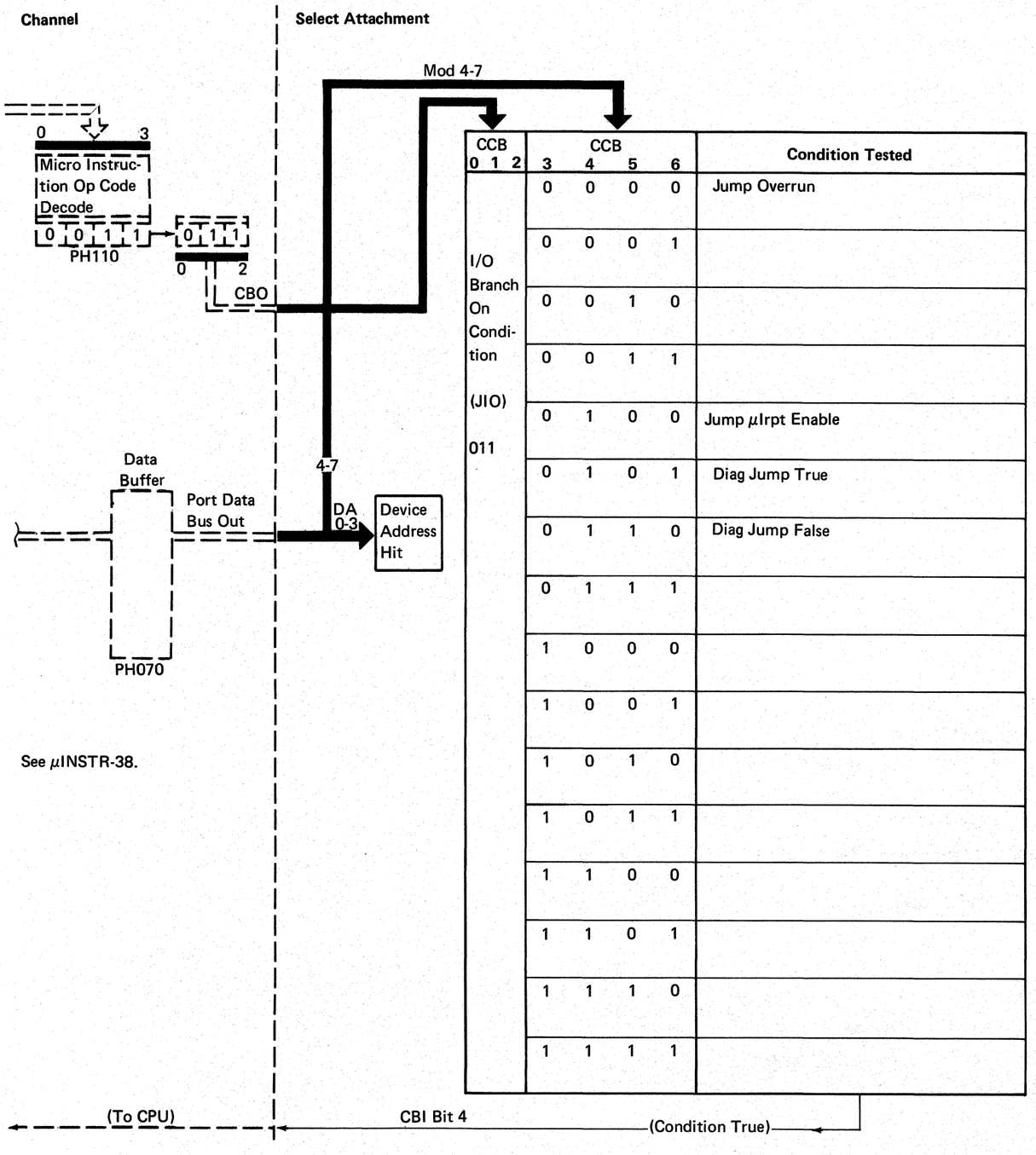
See μINSTR-30 .

Control Sense Command



Modifier DBO 4, 5, 6, 7 Hex	DBI Data Bit	Command	Action Taken	FSL Page	Timing
0	2	Adapter Status 2	Provides a 2 bit on DBI lines if 'keyboard enable' latch is set.	DM050	1

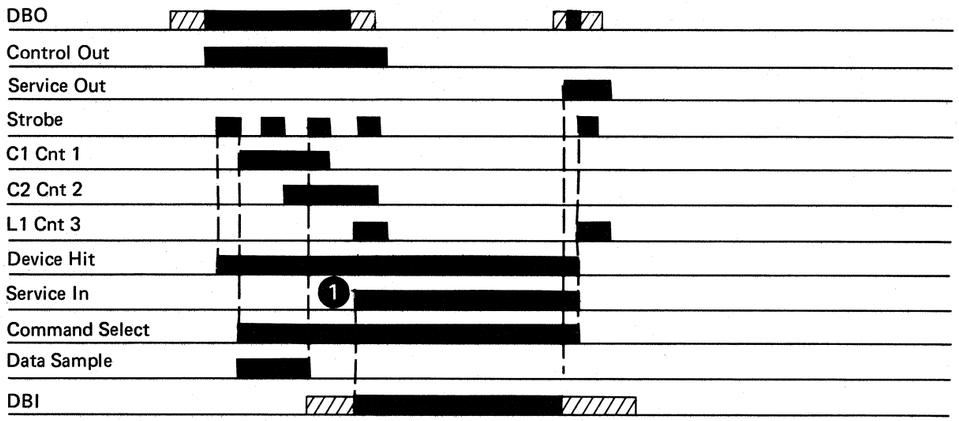
Jump I/O Command



CCB 0 1 2	CCB 3	4	5	6	Condition Tested
I/O Branch On Condition (JIO) 011	0	0	0	0	Jump Overrun
	0	0	0	1	
	0	0	1	0	
	0	0	1	1	
	0	1	0	0	Jump μIrpt Enable
	0	1	0	1	Diag Jump True
	0	1	1	0	Diag Jump False
	0	1	1	1	
	1	0	0	0	
	1	0	0	1	
	1	0	1	0	
	1	0	1	1	
	1	1	0	0	
	1	1	0	1	
	1	1	1	0	
	1	1	1	1	

See μINSTR-38.

Jump I/O Command



Modifier DBO 4, 5, 6, 7 Hex	DBI Data Bit	Command	Action Taken	FSL Page	Timing
0		Jump Overrun	Activates CBI bit 4 if 'overrun' latch has been set.	DM050	1
4		Jump Micro Interrupt	Activates CBI 4 if the 'micro interrupt' latch has been set.	DM050	1
5		Diagnostic Jump True	Activates CBI 4. This is used in diagnostics to guarantee the line will go active.	DM050	1
6		Diagnostic Jump False	Does not activate CBI 4. This is used in diagnostics to guarantee the line will go inactive.	DM050	

Sense Interrupt Level Status Byte Command

Select Attachment

Send Data Byte to Channel

Channel

Mod 4-7

8 11

Micro Instruction Function Field Decode

0 1 0 1

PH110

0 0 1

0 2

CBO

4-7

Data Buffer

Port Data Bus Out

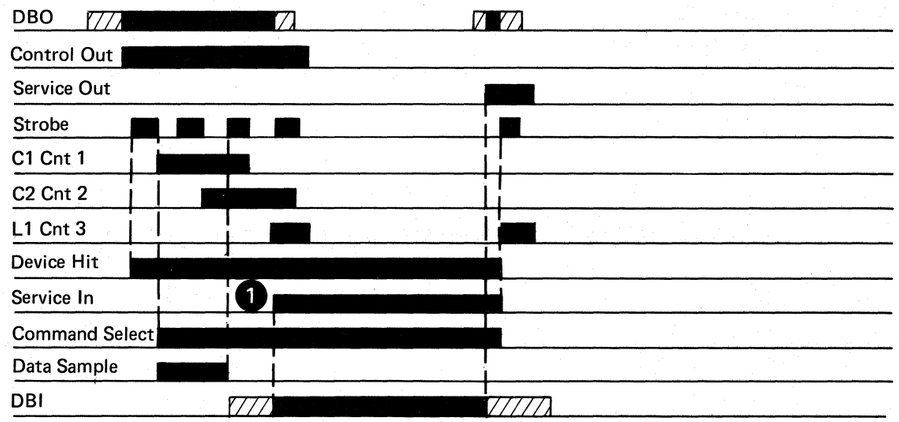
Port Data Bus In

PH070

See μINSTR-30.

CCB 0 1 2	CCB 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
	0 0 1 0 SILS Command		μIrpt Request						
001									

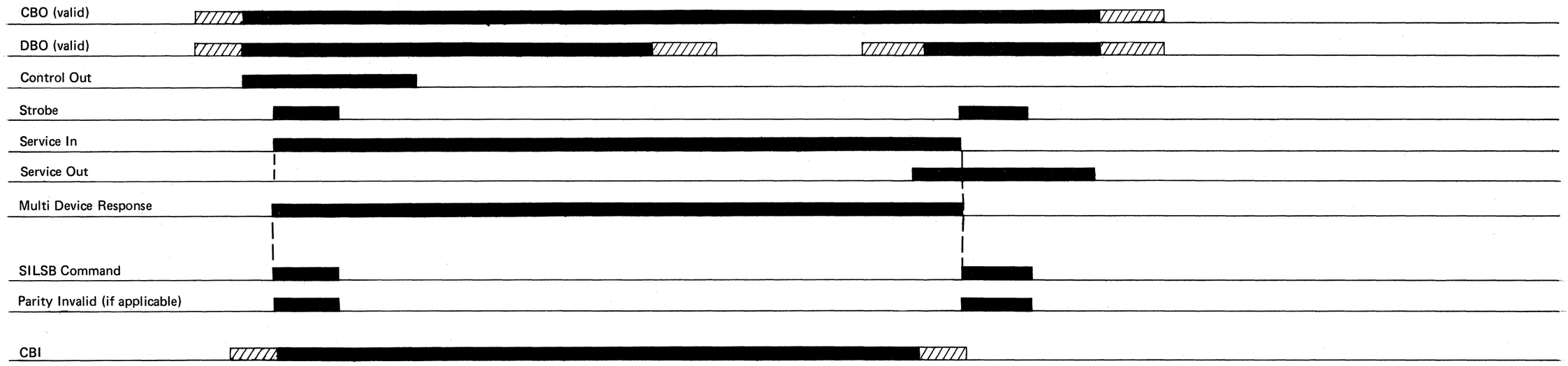
Sense Interrupt Level Status Byte Command



Modifier DBO 4, 5, 6, 7 Hex	DBI Data Bit	Command	Action Taken	FSL Page	Timing
2	1	Sense Interrupt Level Status Byte	Conditions DBI selector to put the status of the micro interrupt request latch on the DBI lines.	DM040	1

SILSB Command and (not) Keyboard Interrupt Level

A sense interrupt level status byte command and not keyboard interrupt level occurs when the microprogram issues the sense interrupt level status byte command with other than 0010 on DBO 0-3. At 'strobe' time after 'control out', the keyboard and display screen attachments will analyze CBO 0-2 and if this is 001 (SILSB command), the attachment will respond by activating 'service in' and 'multi device response' lines immediately. These lines stay active until 'strobe' time after the channel brings up 'service out'. Because 'multi device response' is plus when active it can be ORed with other attachments in the channel such that the channel knows that all attachments have responded.

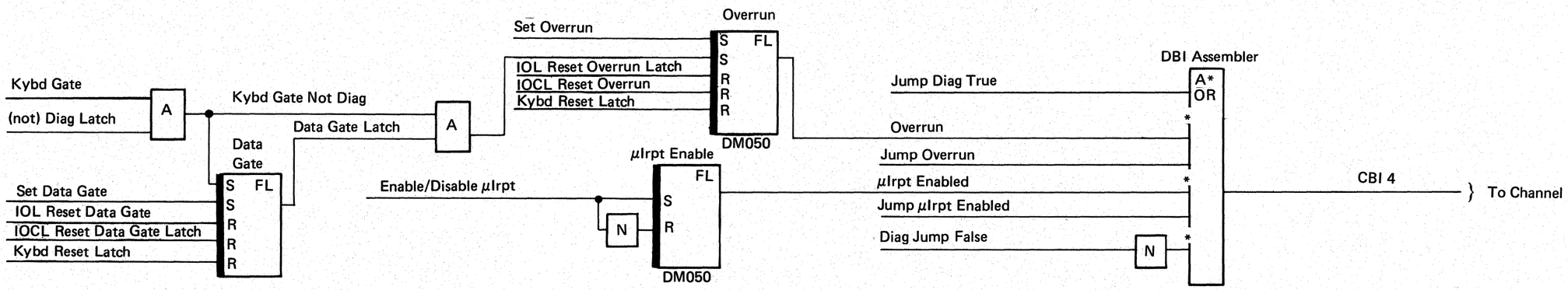


CBI 4 Function

'Kybd gate' is active when a key is pressed on the keyboard. The first key pressed sets the 'data gate' latch. If the data is not accepted by the CPU and the 'data gate' latch is not reset prior to a second key being pressed, the 'overrun' latch sets. When a jump overrun command is issued, CBI 4 goes active indicating to the channel that there is an overrun condition.

The other three conditions which affect CBI 4 are diagnostic checking conditions:

- A jump diagnostic true command activates CBI 4.
- A jump diagnostic false command does not activate CBI 4.
- A jump micro interrupt enable activates CBI 4 if 'μinterrupt enable' latch has been set with an enable/disable micro interrupt enable IOL command.



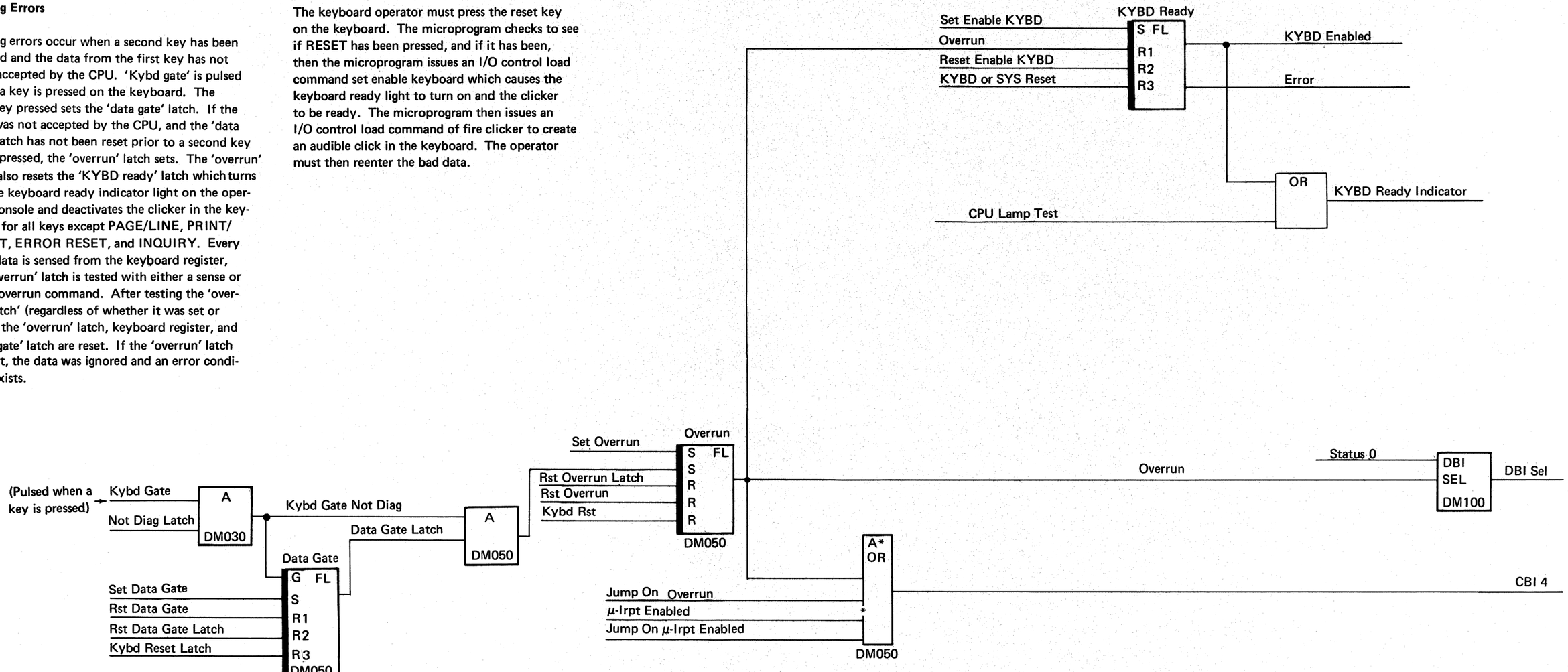
Error Conditions

Keying Errors

Keying errors occur when a second key has been pressed and the data from the first key has not been accepted by the CPU. 'Kybd gate' is pulsed when a key is pressed on the keyboard. The first key pressed sets the 'data gate' latch. If the data was not accepted by the CPU, and the 'data gate' latch has not been reset prior to a second key being pressed, the 'overrun' latch sets. The 'overrun' latch also resets the 'KYBD ready' latch which turns off the keyboard ready indicator light on the operator console and deactivates the clicker in the keyboard for all keys except PAGE/LINE, PRINT/RESET, ERROR RESET, and INQUIRY. Every time data is sensed from the keyboard register, the 'overrun' latch is tested with either a sense or jump overrun command. After testing the 'overrun latch' (regardless of whether it was set or reset) the 'overrun' latch, keyboard register, and 'data gate' latch are reset. If the 'overrun' latch was set, the data was ignored and an error condition exists.

Error Recovery

The keyboard operator must press the reset key on the keyboard. The microprogram checks to see if RESET has been pressed, and if it has been, then the microprogram issues an I/O control load command set enable keyboard which causes the keyboard ready light to turn on and the clicker to be ready. The microprogram then issues an I/O control load command of fire clicker to create an audible click in the keyboard. The operator must then reenter the bad data.



Serial Printer

INTRODUCTION

The IBM System/32 can be ordered with either a serial printer or a belt printer.

The serial printer is available in four models:

120 cps (characters per second) bidirectional
80 cps bidirectional
40 cps bidirectional
40 cps unidirectional

The two models of the 40 cps printer are identical. The attachment circuitry controls whether they print only left to right, or in both directions.

Serial printer theory of operation is model and EC level dependent. In this section, theory differences will be listed under the following headings:

- 40/80 cps
- 40/80 cps – 120 compatible
- 120 cps

To determine whether your 40 or 80 cps printer is 120 compatible, see plug chart page AY039, in the field service logics.

Characters are printed by selectively energizing any of seven print wire magnets as the print head is moved along the print line by a stepper motor. An eighth print wire magnet is used for underscore.

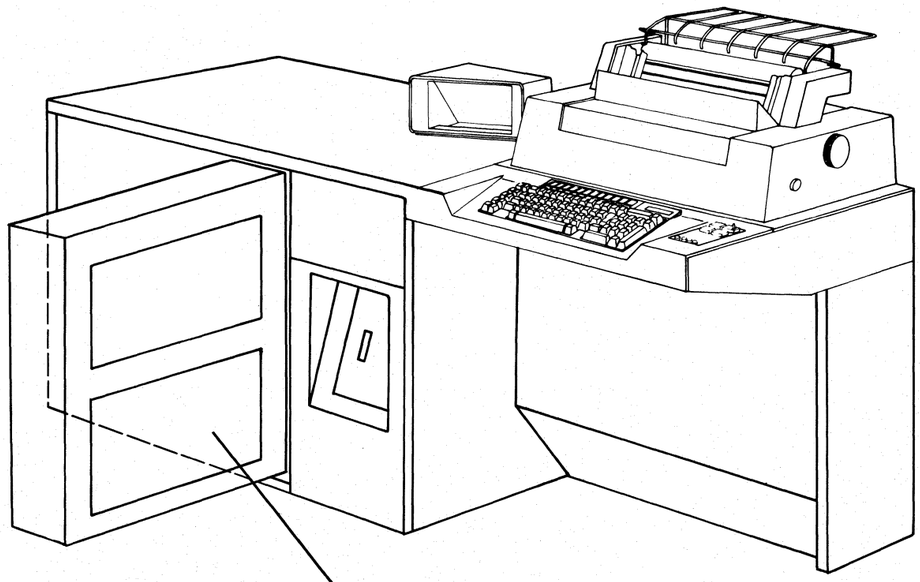
The attachment for the serial printer is contained on two cards located at A2R2 and A2Q2. The cards contain a 1/2K by 9 RAM (random access memory) and a 1K by 18 ROS (read only storage).

RAM is reloaded each IMPL with variable data such as print head home position, print emitter timings, print head motor timings, and eight characters that change for the different character sets (U.S./WTC/ASCII). The eight changeable characters are stored in a wire image.

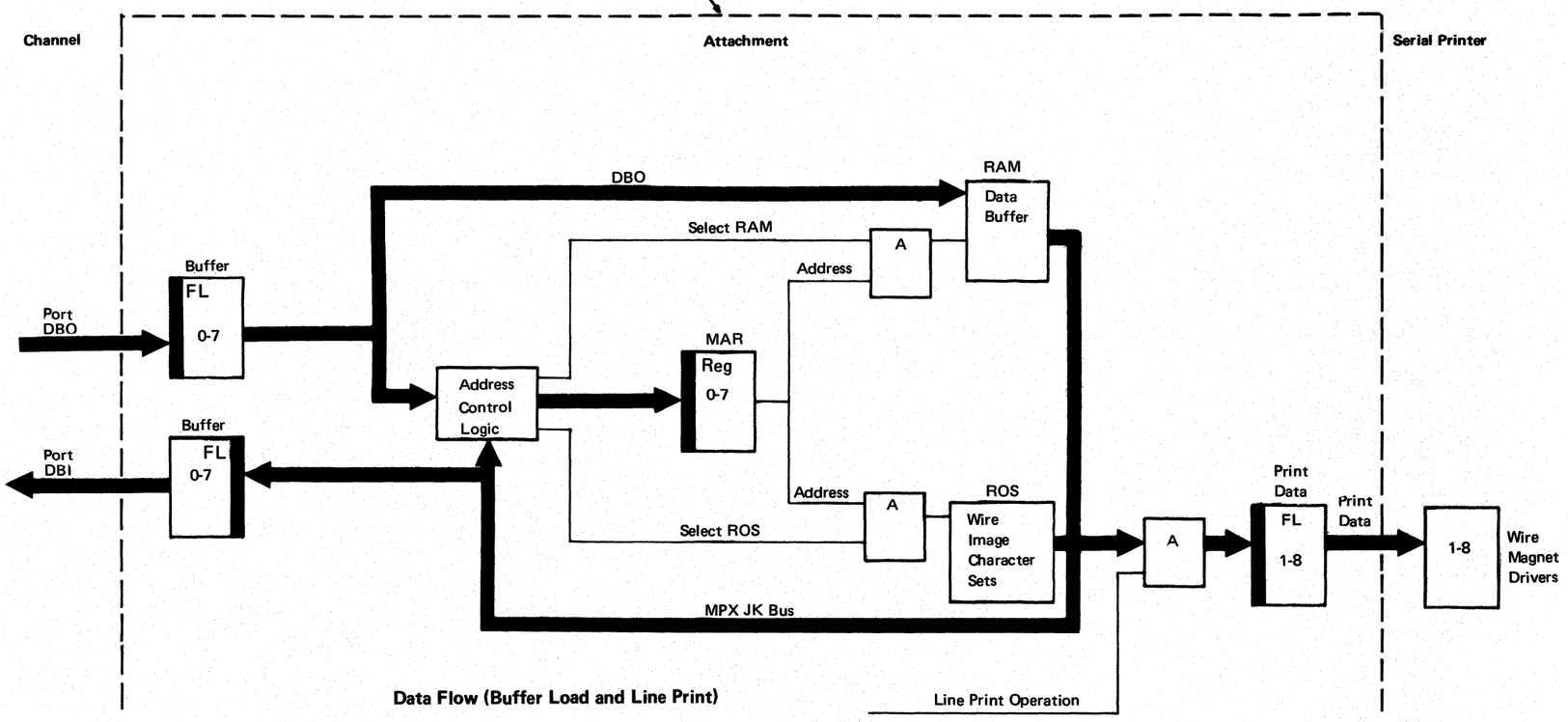
ROS stores information that does not change. The 56 characters that are common to all U.S., WTC, and ASCII character sets and the Katakana character set are stored in ROS.

Before printing, the microprogram loads the image of each line (132 positions in EBCDIC) into the data buffer. The data buffer is the first 132 positions of RAM. The tabs, which represent the location of the first and last significant characters of each line, are also loaded into RAM before printing.

Forms movement is also controlled by the microprogram. Forms are moved by the forms stepper motor, which is geared to the platen. When the forms are moved, the forms emitter sends pulses to the attachment to update the forms line/print time counter, which is used to advance the stepper motor.



Attachment and Serial Printer Data Flow



Data Flow (Buffer Load and Line Print)

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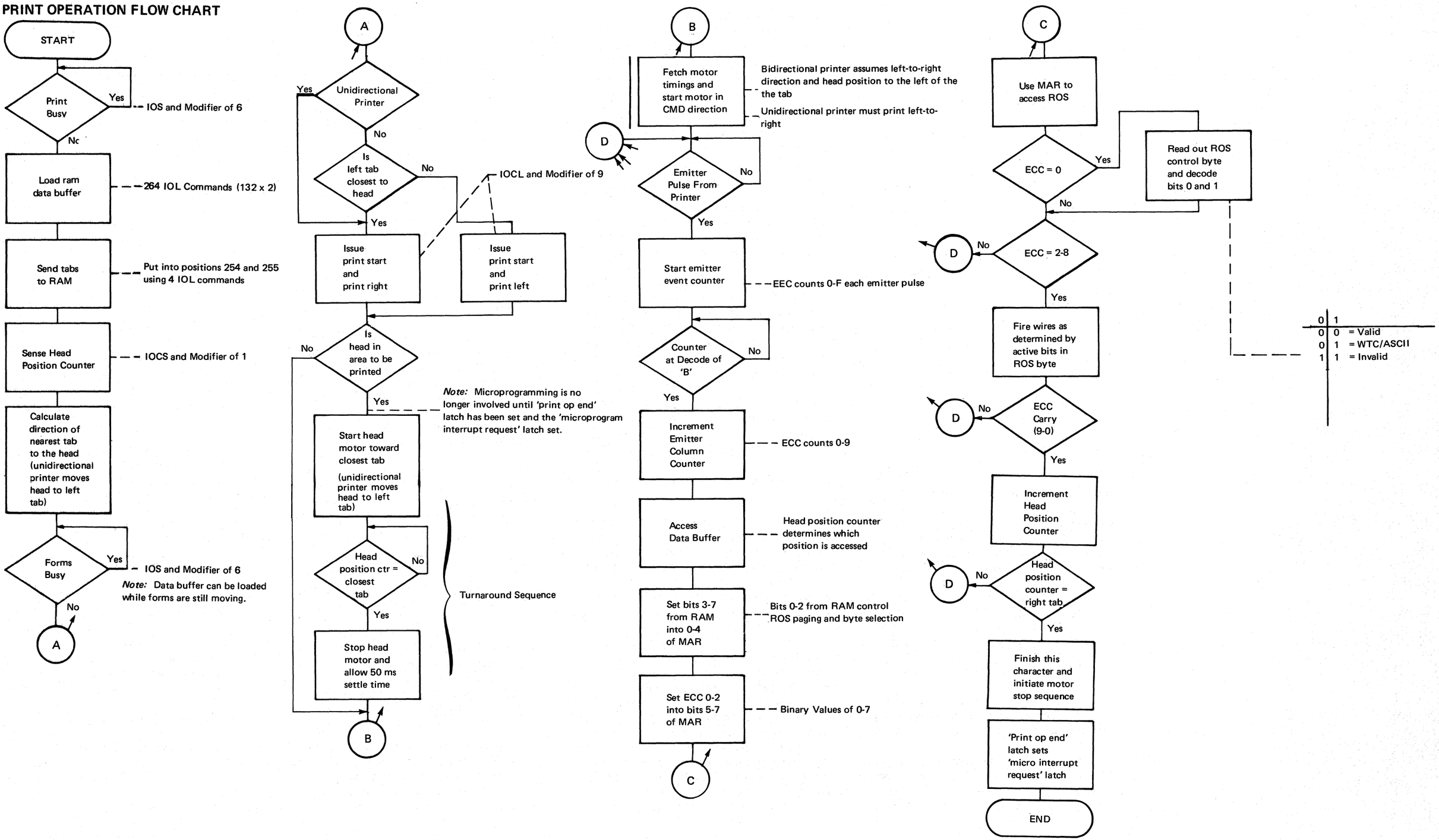
PRINT OPERATION FLOW CHART



THEORY OF PRINTING

To print a line, four things are done:

1. Load the data buffer (microprogram operation).
2. Position the print head (attachment operation).
3. Print the data from the buffer (attachment operation).
4. Move the forms to a new line (both microprogram and attachment). Forms movement is not a part of the printing operation, but is described because the system programmer usually issues SIO instructions to print and then space.

Loading The Data Buffer

Two IOL commands are needed to transfer one character from the CPU to the data buffer in RAM. The first IOL command sets a buffer address into the attachment MAR (memory address register). The second command loads the addressed buffer position with the EBCDIC code of the character to be printed.

Microprogramming loads the data buffer by using 264 IOL commands (132 x 2). It is necessary to load all 132 positions, regardless of the length of the line to be printed to clear any residual data from the previous line. If no character is to be printed from the addressed RAM location, a blank (hex 40) is loaded.

Positioning The Print Head

In preparation for printing a line, the system programmer sets up an area of main storage in the CPU that is referred to as the data buffer. This is *not* the same data buffer that is part of RAM, but it *is* the area from which the RAM buffer is loaded. Once the RAM data buffer is loaded, the two areas contain identical data.

When control is passed to the printer microprogram, it scans the main storage data buffer to locate the first position that is not a blank. A value of three is subtracted from that position, which becomes the left tab. The left tab is then loaded into RAM location 255 (hex FF).

Then the main storage data buffer is scanned in the opposite direction to locate the position of the last significant character of the line to be printed. Three is added to that position. That value becomes the right tab and is loaded into RAM location 254 (hex FE).

The microprogram now senses the attachment to determine the position of the print head. If the head position counter contains a value less than the value of the left tab, the microprogram sends an IOCL command to the attachment to start print and print right (left to right).

If the value of the right tab is less than the value in the head position counter, the attachment is commanded to start print and print left (right to left).

Note: The unidirectional printer always prints from left-to-right beginning at the left tab. If it is commanded to print right-to-left (print left), the command is ignored by the attachment and no printer action occurs.

If the head is *in* the area to be printed, the value in the head position counter is equal to or greater than the value of the left tab and less than or equal to the value of the right tab. The microprogram computes which tab is nearer to the present head position. Based upon that computation, the attachment is told to start print and either print right or print left.

Note: From here on, the attachment is independent of the microprogram until the 'print op end' latch causes the attachment to request an interrupt.

Assuming the print head is in the area to be printed and the attachment is told to print right, the head must be moved left past the left tab, stopped, allowed to settle, started in a left to right direction, and be at printing speed by the time the first character is read out of the RAM data buffer. The reason for subtracting three from the location of the first significant character in a line less than 132 print positions is to allow the print head to come up to speed after turning around and before printing the first character of the line.

Positioning of the print head is controlled by the value in the head position counter and the value of the left tab, which is brought out of RAM and stored in a 1 byte buffer. The head is moved left until the value in the head position counter equals the value of the left tab. At that time, the head is stopped and allowed to settle for 50 ms. After the settle time, the print head stepper motor is started going right, and continues to move until the head position value equals the right tab value. The head is stopped, and another 50 ms settle time occurs before the end of the print operation.

When the print head is at the right edge of the left margin (LM), the head position counter contains a value of hex 00. When the head moves into the left margin, the value goes from hex 00 to FF, FE, FD, or FC depending upon how far into the left margin the head moves. The counter value is increased as the head moves to the right.

Printing The Data From The Buffer

The data buffer is the first 132 positions of RAM. ROS contains the wire image of the U.S., WTC/ASCII, and Katakana character sets. RAM contains the wire image of the eight changeable U.S., ASCII and World Trade special characters.

Eight bytes **B** are needed to store the wire image of each character **C**. The first byte of the eight is the control byte. The two high order bits of the control byte indicate whether the character is a changeable U.S., ASCII, World Trade special character, or invalid **E**.

Data to be printed is loaded into the RAM data buffer (in EBCDIC) by the microprogram before the printing operation. During printing, RAM is accessed to determine which character to print. Assume the character from RAM is an A, which is hex C1 **A**. ROS is then accessed eight times as the print head moves through the first print position of the line. As the head moves through that print position, the print wire magnets are fired as determined by the bits that are on in the eight ROS bytes **D**.

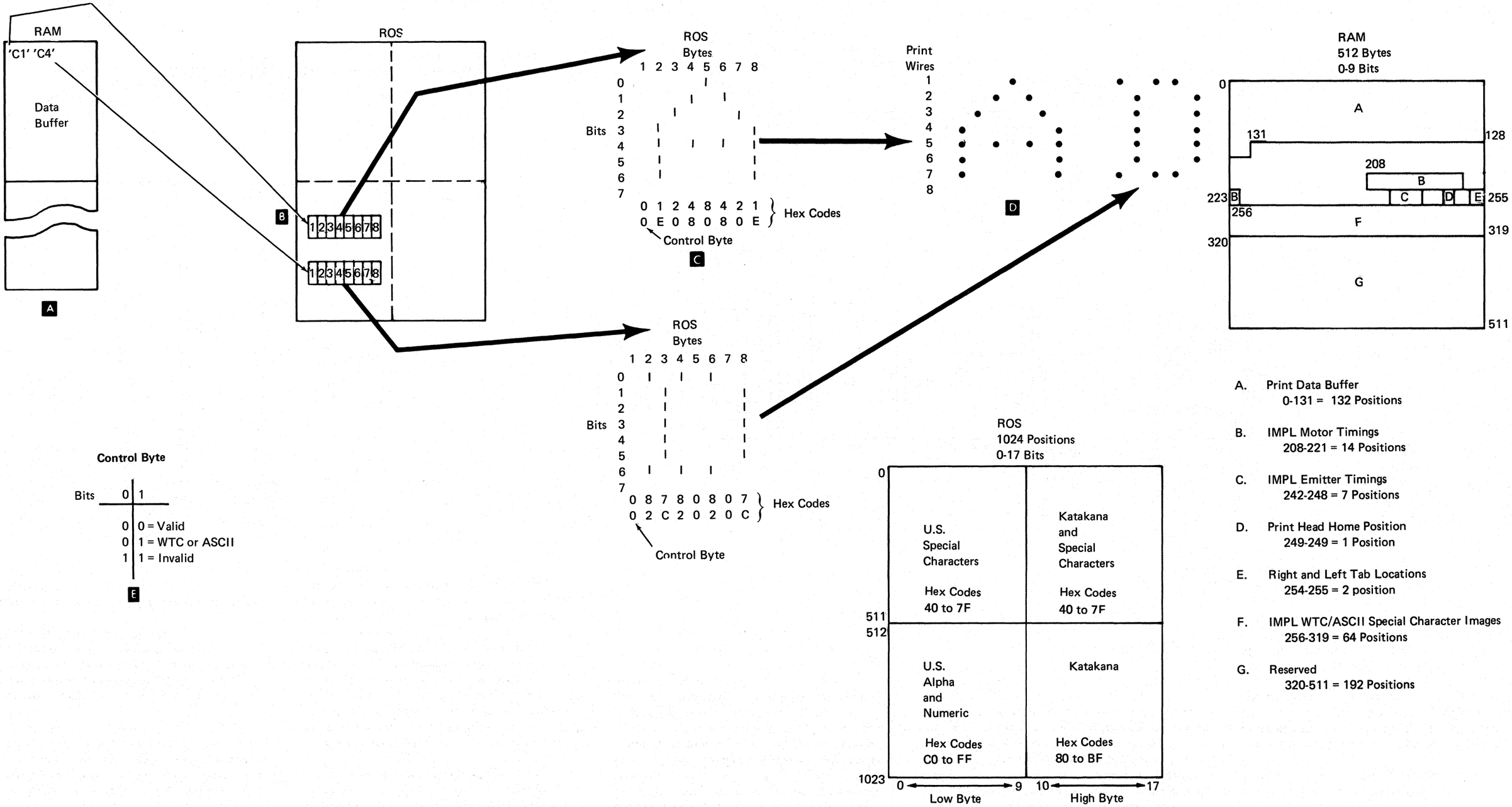
RAM is accessed again for the second character. For example, assume the letter D, which is hex C4. ROS is then accessed eight more times (as the head moves through the second print position) to determine which print wire magnets to fire.

If the character is a changeable U.S., ASCII, or World Trade special character, RAM must be accessed eight times to print the wire image. (See *ROS Addressing* in this section.)

Control information for the attachment is loaded into RAM beginning at the following fixed locations:

Location	Description
208	Print head motor timings
242	Print emitter timings
249	Print head home position
254	Right and left tabs

The attachment can access RAM for control information during printing except when it is accessing the EBCDIC character from RAM or the wire image from either RAM or ROS. Control information for print head home position is used only during a head restore operation. (See *Head Restore* in this section.)



A. Print Data Buffer
0-131 = 132 Positions

B. IMPL Motor Timings
208-221 = 14 Positions

C. IMPL Emitter Timings
242-248 = 7 Positions

D. Print Head Home Position
249-249 = 1 Position

E. Right and Left Tab Locations
254-255 = 2 position

F. IMPL WTC/ASCII Special Character Images
256-319 = 64 Positions

G. Reserved
320-511 = 192 Positions

- Katakana Mode Selects ROS High Byte.

ROS and RAM Layouts

Print Motor Drive

The print head stepper motor is driven by four lines from the attachment: 'prt drv A', 'prt drv not A', 'prt drv B', and 'prt drv not B'.

When the head is starting, printing/spacing, stopping, or settling, only two of the four drive lines are active at any one time. When the head is stopped for a length of time that is greater than the settling time, none of the four drive lines is active.

Each time the phase (status) of the four lines is changed, two degrees of motor rotation results. The length of time that the lines stay in each phase is controlled by the IMPL motor timings that are stored in RAM locations 208-221.

The contents of these 14 RAM locations are divided into three groups of intervals:

	At RAM Location	Decimal Value 40/80 cps	40/80 cps — 120 Compatible	120 cps	
Start Intervals	208	73	72	72	
	209	91	90	91	
	210	82	81	81	
	211	63	62	48	
Up-to-speed Intervals	212	52	51	31	Slow Rates (120 cps only)
	213	52	51	39	
	214	52	51	48	
	215	52	52	44	
	216	52	52	44	
	217	52	52	35	Up to Speed (120 cps only)
	218	52	52	35	
	219	52	52	35	
Stop Intervals	220	63	62	109	
	221	110	109	62	

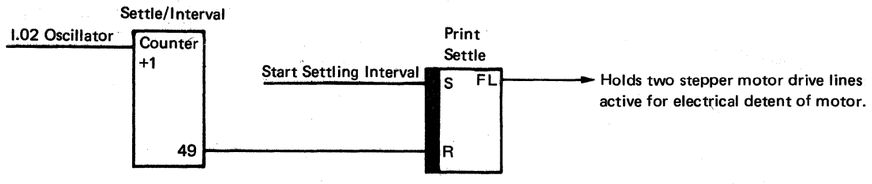
Note: The interval time values for 40 and 80 cps machines are the same because the print head speed difference is achieved mechanically. Because the speed difference in the 120 cps is achieved electrically, the interval time values are different.

Settling Intervals

The settling intervals are not stored in RAM. They are created by using a 1.02 ms oscillator to increment the 'settle/interval' counter. When the counter reaches 49 (50 ms), the settling interval is over.

If characters are to be printed after the settle interval, the interval is called a start settle interval. Start settle intervals activate two of the drive lines (in the same configuration as the preceding stop settle interval) for 50 ms. This ensures that the two activated drive lines are holding the stepper motor and drive belt steady when the next start interval is initiated.

If no characters are to be printed after the settle interval, the interval is called a stop settle interval. Only after a stop settle interval are the four drive lines deactivated.



Start Intervals

After a 50 ms start settle interval, the motor event counter is used to access RAM for an IMPL motor time. The motor time is set into the motor elapse counter, and the motor event counter is incremented by one. A 64 μs oscillator is used to decrement the motor elapse counter. When this counter gets down to one, the stepper motor drive line phase is changed, which causes two degrees of motor rotation, and the next sequential position of RAM is read out into the motor elapse counter.

Up-to-speed Intervals

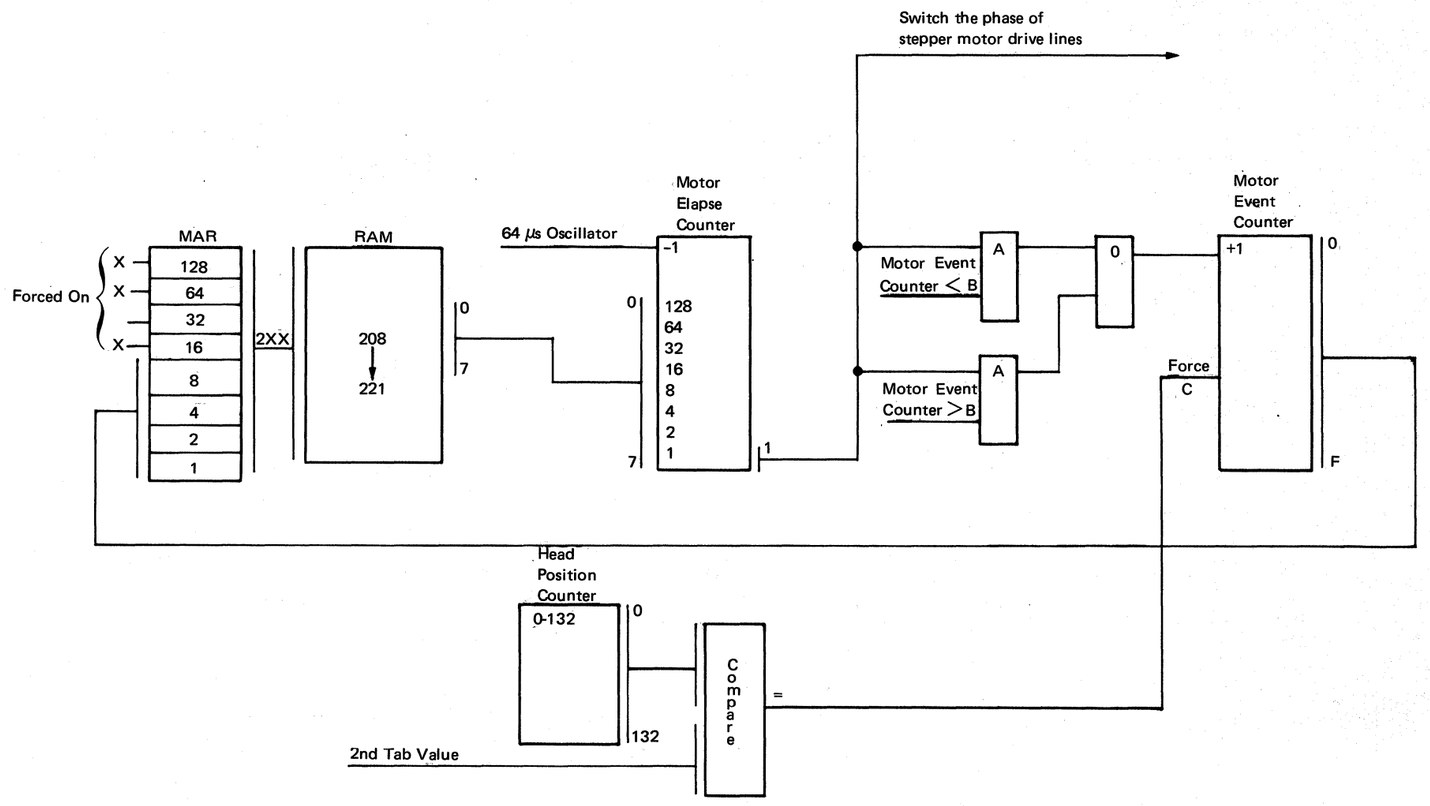
This sequence repeats until the event counter reaches hex B or the print head reaches the second tab. If the print head has not reached the tab by the time the counter reaches hex B, advance pulses to the event counter are blocked and the same position of RAM is accessed repeatedly and read out into the motor elapse counter until the head position counter equals the tab. A stop sequence is initiated when the head reaches the tab.

Stop Intervals

When the tab and the head position counter compare equal, the motor event counter is forced to hex C and the first of two stop settle times is accessed from RAM and loaded into the motor elapse counter.

The motor elapse counter is again decremented by the 64 μs oscillator, and when the counter gets to one, the second stop time is accessed from RAM and loaded into the motor elapse counter.

The motor event counter is incremented to hex E and when the motor elapse counter reaches one, the settle/interval counter begins to time the 50 ms stop settle time.



Note: Compare equal forces the first stop interval to be read out of RAM.

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Underscore

The EBCDIC code for an underscore is hex 6D. ROS contains a wire image of the underscore at location 360-367.

If the system programmer wants to underscore some characters of a print line, he must issue an SIO instruction to print the line, then issue another SIO instruction to underscore the characters that are to be emphasized.

Head Restore

A head restore operation causes the head to move left into the left margin and stop where the head retract ramp moves the head away from the paper. Restoring the head prevents ribbon ink from bleeding on the paper and makes paper insertion easier.

When the head is restored, it is said to be unloaded, at print head home, retracted, or in the forms loading/unloading position.

As the head moves left through the right edge of the left margin, the head position counter is forced to hex 00 for recalibration. As the head moves farther left into the left margin, every tenth emitter pulse decrements the position counter to hex FF, FE, FD, etc.

If the head is not in the left margin when the restore operation is begun, it is started going left. The print head home position value is read out of RAM and compared to the head position counter during each emitter time. When they compare equal, the head is stopped and allowed to settle for 50 ms.

If the head is in the left margin when the restore operation is begun, it is started going right until the 'left margin' line is no longer active. It is then stopped, allowed to settle for 50 ms, and started going left. The operation from this point on is explained in the previous paragraph.

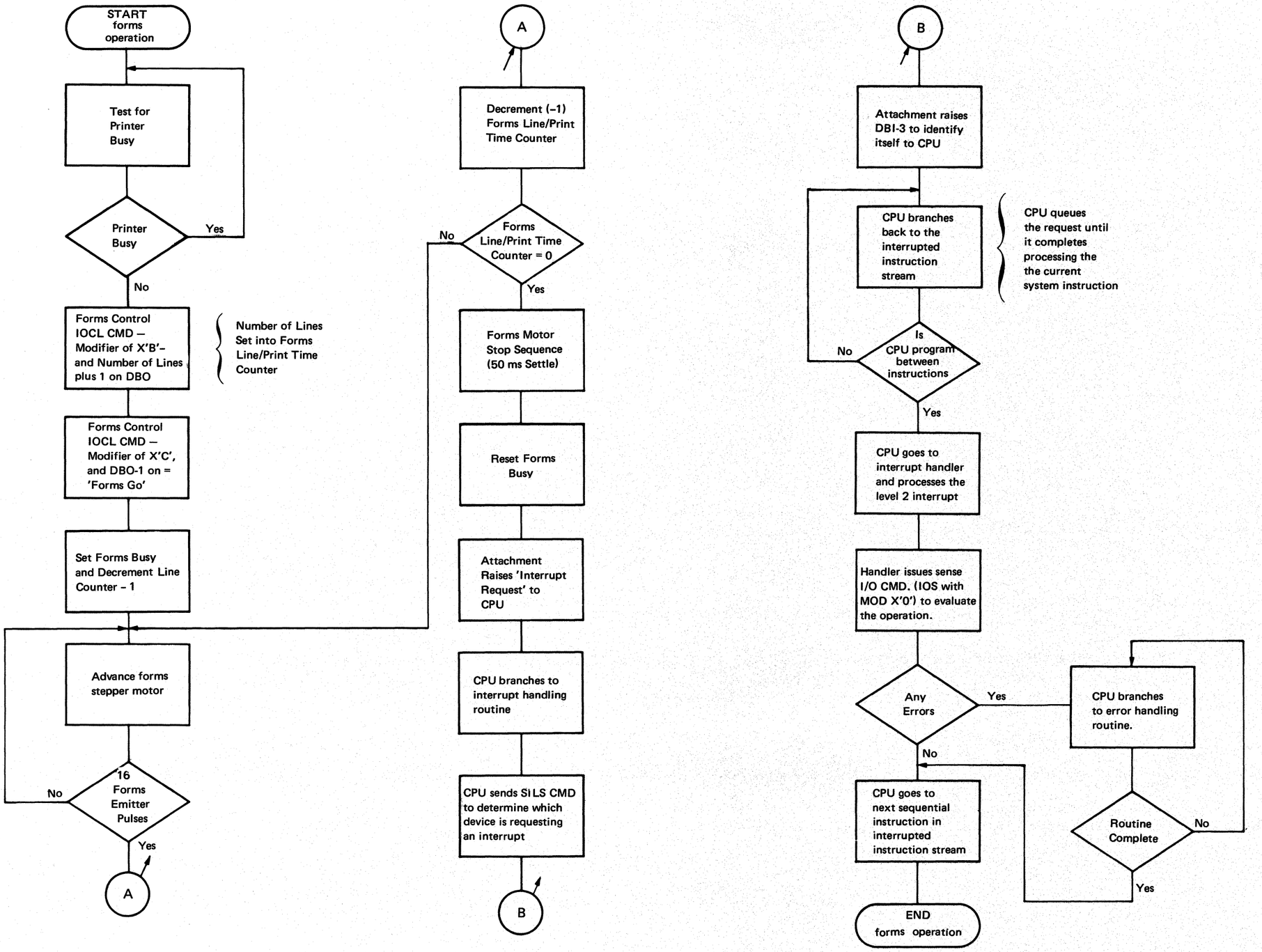
Head restore operations can be started in three ways:

1. The print motor elapse counter is used to time a two minute interval after each I/O micro instruction is executed. If no micro instructions are received by the attachment within two minutes, the attachment restores the print head.

2. If the microprogram issues a check reset command to the serial printer, the print head is restored by the attachment.

3. If the microprogram issues a restore head command to the serial printer, the print head is restored by the attachment.

FORMS OPERATION FLOWCHART



Moving The Forms

After the line is printed, the attachment requests an interrupt and the microprogram branches to an interrupt handling routine to evaluate the print operation. If there were no errors, the microprogram issues an IOCL command with a modifier for forms control.

The system programmer must tell the attachment how many lines to space or which line to skip to before telling it to go. This is done with a system SIO instruction that causes the microprogram to issue an IOCL command to the attachment. The IOCL has a modifier of hex C that tells the attachment to set the line count plus one that is on the DBO into the forms line/print time counter. The microprogram then issues another IOCL command to bring up the 'forms go' line in the attachment to start the forms stepper motor.

As the forms emitter disk rotates, forms emitter pulses are sent to the forms emitter counter in the attachment. The forms emitter counter is a binary counter that counts from 0 to 15. Its output is decoded so that at each emitter count of 15 (16 emitter pulses), the forms line/print time counter is decreased by one.

When the forms line/print time counter reaches zero, a 1 ms stop interval and 50 ms settle interval occur, the 'forms busy' latch is reset, the 'carriage op end' latch is set, and the attachment raises the 'interrupt request' line to the port (channel).

COMMANDS

Seven microprogram commands control all serial printer operations and communicate the status of the printer to the microprogram.

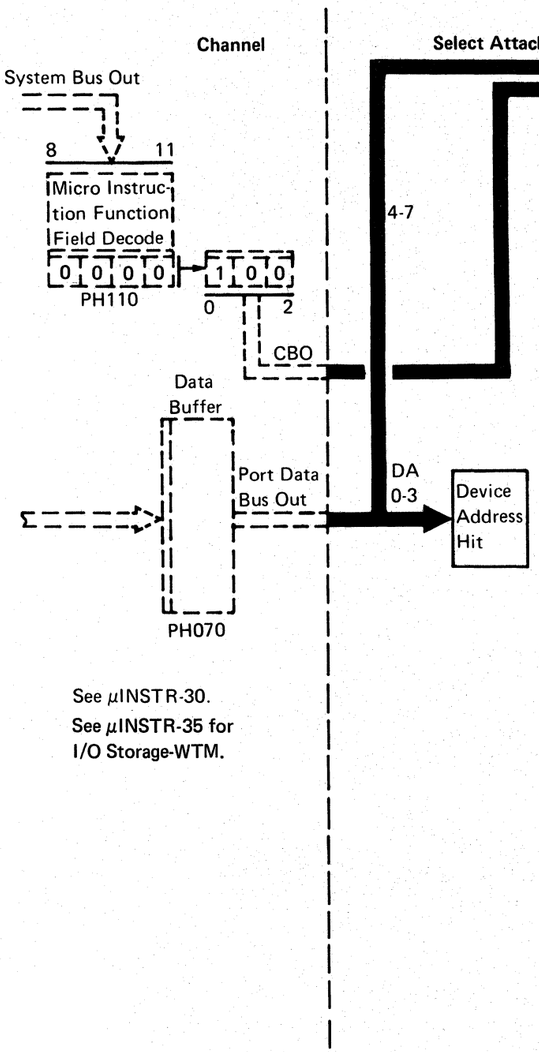
I/O Load	IOL
I/O Control Load	IOCL
I/O Sense	IOS
I/O Control Sense	IOCS
Jump I/O	JIO
Sense Interrupt Level Status	SILS
I/O Storage	

I/O storage, IOL and IOCL commands control printing and forms movement; the other commands evaluate previous operations.

Load Command

I/O Load (IOL)

(I/O Storage [WTM])



See μINSTR-30.
See μINSTR-35 for I/O Storage-WTM.

CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
100 Load	0 0 1 0 Set Interrupt Request	Immediate							
	0 0 1 1 Reset Interrupt Request								
	0 1 0 1 Special Diagnostic Control	Bit 0 — Prevents motor elapse counter from being loaded to 121 when 'clock stepping' in diagnostic mode —					— (Blocks 2 minute head restore)		
	0 1 1 0 Interrupt Request Control			Forms Busy Off	Print Busy Off				
	1 0 0 1 Memory Load	— Loads DBO byte into the addressed RAM location —							
	1 0 1 0 Load MAR	— Loads DBO byte into the Memory Address Register —							
	1 0 1 1 Enable Diagnostic Mode	Immediate — Sets diagnostic mode and invokes disable motors —							
	1 1 0 0 Disable Diagnostic Mode	— Resets diagnostic mode —							
	1 1 0 1 Diagnostic Mode Control Byte	Diagnostic Control Mode	Print Emitter E1	Print Emitter E2	Diagnostic Control*	Base Oscillator	Print Emitter E3	Diagnostic Clock 64 μs	Left Margin
	1 1 1 0 Diagnostic Mode Control Byte		Forms Emitter B	Forms Emitter A		Wire Check			
	1 1 1 1 Check Reset	Immediate — Includes serial printer reset and restores print head and enables motors —							

*Not used in 120 cps attachment.

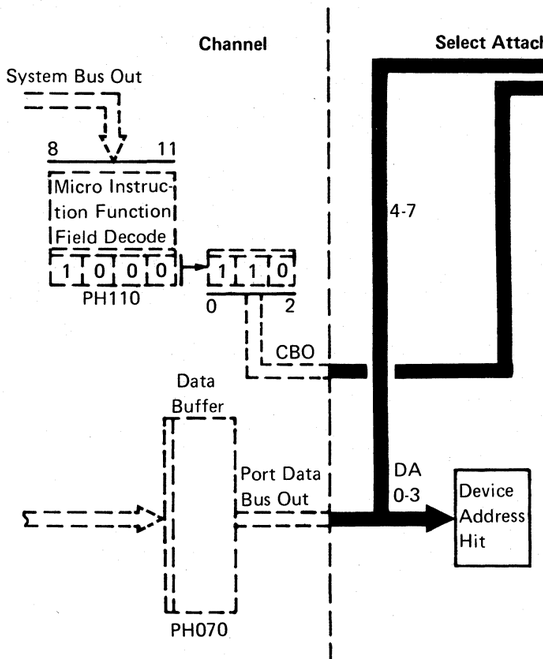
IOL (Continued)

Modifier: Port DBO 4, 5, 6, 7 (Hex)	Port DBO Bit	Command	Action	FEALD Page
0010 (2)	–	Set Interrupt Request	Sets the 'micro interrupt request' latch on, which initiates an interrupt	FR141, 241
0011 (3)	–	Reset Interrupt Request	Resets the 'micro interrupt request' latch.	FR141, 241
0101 (5)	–	Special Diagnostic Control	Prevents a set to motor elapse counter so that the head doesn't restore at 2 minutes.	FR127, 227
0110 (6)	2	Interrupt Request Control	Turns on the 'print op end' latch when print busy falls which allows the 'micro interrupt request' latch to turn on.	FR141, 241
	3		Turns on the 'carriage op end' latch when forms busy falls which allows the 'micro interrupt latch' to turn on.	FR141, 241
1001 (9)	0-7	Memory Load	Loads the DBO byte to the RAM position as determined by MAR.	FQ070
1010 (A)	0-7	Load MAR	Loads the Memory Address Register (-DBO bits 0-7)	FQ014
1011 (B)	–	Enable Diagnostic Mode	Sets the diagnostic latches to simulate actual signal lines and invoke 'disable motors'.	FR120, 220 FR131, 231 FR145, 245
1100 (C)	–	Disable Diagnostic Mode	Resets the diagnostic latches.	
1101 (D)	0	Diagnostic Mode Control Byte	Allows DBO bit 0 to set/reset diagnostic control mode.	FR156, 256
	1		Allows DBO bit 1 to set/reset the diagnostic print emitter 1 latch.	FR156, 256
	2		Allows DBO bit 2 to set/reset the diagnostic print emitter 2 latch.	FR156, 256
	3		Allows DBO bit 3 to set/reset allow diagnostic control.*	FR156, 256
	4		Allows DBO bit 4 (multiplex-4) to flip-flop the base oscillator.	FR131, 230
	5		Allows DBO bit 5 (multiplex-5) to set the diagnostic print emitter 3 latch.	FR156, 256
	6		Allows DBO bit 6 to pulse the 64 μs clock.	FR145, 245
	7		Allows DBO bit 7 (multiplex-7) to set the left margin latch.	FR120, 220
1110 (E)	1	Diagnostic Mode Control Byte (2)	Allows DBO 1 bit to bring up forms emitter B.	FR145, 245
	2		Allows DBO 2 bit to bring up forms emitter A.	FR145, 245
	4		Allows DBO 4 bit to set wire check.	FR141, 241
1111 (F)	–	Check Reset	Resets all pending checks, restores the head, and brings up 'printer reset'.	FR150, 250

*Not used in 120 cps attachment.

Control Load Command

I/O Control Load (IOCL)



See μINSTR-30.

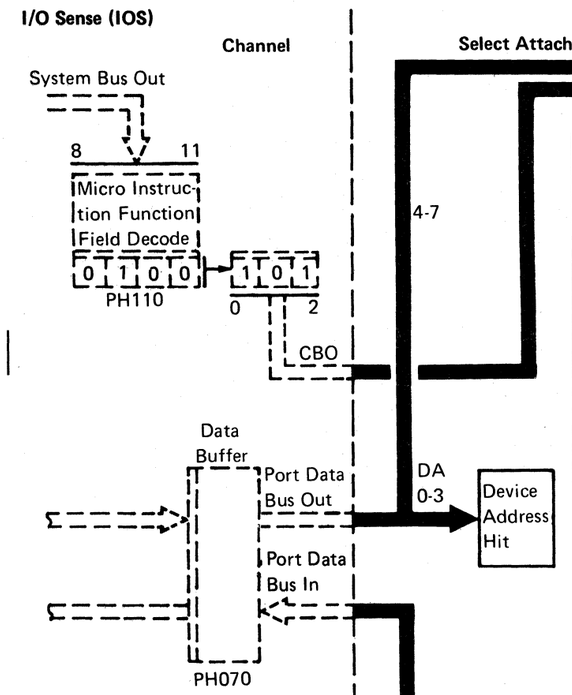
CCB 0 1 2	CCB 3 4 5 6	DBO Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
110 Control Load	0 0 0 0 Diagnostic Adapter Control		Set Kana Mode (FR131, 231)	Reset Kana Mode (FR131, 231)	Disable Motors	Sets Memory Data Check Latch On			
	0 0 0 1 Diagnostic Wire Control	Wire Latch 1	Wire Latch 2	Wire Latch 3	Wire Latch 4	Wire Latch 5	Wire Latch 6	Wire Latch 7	Wire Latch 8
	0 1 0 0 Enable Adapter 0 1 0 1 Disable Adapter	Immediate — Invokes adapter and serial printer resets —							
	1 0 0 0 Buffer Page/ Byte Selection	Page Select High	Page Select Low	Ram (0)/ROS (1) Select	Select Low (0)/High (1) ROS Byte				
	1 0 0 1 Print Cycle Control	Start Print	Disable Unprintable Character Detection (FR131, 231)	Enable Unprintable Character Detection	Restore Head (not when forms busy)			Print Right (FR114)	Print Left* (FR114)
	1 0 1 0	— Reserved —					Set 120 cps Mode (FR 160, 260)	Reset 120 cps Mode (FR 160, 260)	
	1 0 1 1 Load Forms Line Counter	— Loaded with number of lines plus 1 —							
	1 1 0 0 Diagnostic Forms Control		Forms Go		Enable EOF Detect	Disable EOF Detect		Reserved for Forms Jam Disable	Reserved for Forms Jam Enable
	1 1 0 1 Head Position Counter	Test Decrement	Test Increment						End Test Mode

*The unidirectional printer attachment ignores this bit on an IOCL command with a modifier of 9 (FQ020).

Modifier: CCB 3, 4, 5, 6 (Hex)	Port DBO Bit	Command	Action	FEALD Page
0000 (0)	1 2 3 4	Diagnostic Adapter Control (+IOCL Byte 0)	Allows DBO bit 1 to set Kana mode latch. Allows DBO bit 2 to reset Kana mode latch. Allows DBO bit 3 to set the disable motors latch. Allows DBO bit 4 to set the memory data check latch.	FR131, 231 FR131, 231 FR145, 245 FR131, 231
0001 (1)	0-7	Diagnostic Wire Control	Allows DBO bits 0-7 to pass through the JK selector and become direct data input from the microprogram to the wire latches.	FQ060
0100 (4)	–	IOCL Enable Adapter	Resets the system/adapter reset latch.	FR143, 243
0101 (5)	–	IOCL Disable Adapter	Sets the system/adapter reset latch.	FR143, 243
1000 (8)	0 1 2 3	Buffer Page/Byte Selection	Allows DBO bit 0 to select high page. Allows DBO bit 1 to select low page. DBO bit 2 off selects RAM. DBO bit 2 on selects ROS. DBO bit 3 off selects low ROS byte. DBO bit 3 on selects high ROS byte.	FQ010 FQ010 FQ010 FQ010
1001 (9)	0 1 2 3 6 7	Print Cycle Control (+IOCL Byte 9)	Allows DBO bit 0 to enable start print. Allows DBO bit 1 to disable unprintable character detection. Allows DBO bit 2 to enable unprintable character detection. Allows DBO bit 3 to restore the print head when then carriage is not busy. Allows DBO bit 6 to set print direction to the right and allow print (FR114). Allows DBO bit 7 to set print direction to the left (reset print direction right) and allow print (FR114).*	FR123, 223 FR131, 231 FR131, 231 FR123, 223 FR123, 223 FR123, 223
1010 (A)	5 6		Sets 120 cps mode. Resets 120 cps mode.	FR260 FR260
1011 (B)	0-7	Load Forms Line Counter (+IOCL Line Count)	Loads the forms line/print time counter with the number of lines plus 1.	FR130, 230
1100 (C)	1 3 4 6 7	Diagnostic Forms Control (+IOCL Byte C)	Allows DBO bit 1 to set forms go and reset Kana mode. Allows DBO bit 3 to set the end of forms enable latch. Allows DBO bit 4 to reset the end of forms enable latch. Reserved. Reserved.	FR143, 243 FR143, 243 FR143, 243
1101 (D)	0 1 7	Head Position Counter (+Diagnostic Test Mode)	Allows DBO bit 0 to set the test mode latch and the diagnostic decrement counter. Allows DBO bit 1 to set the test mode latch and the diagnostic increment counter. Allows DBO bit 7 to reset the test mode latch.	FR110, 210 FR110, 210 FR110, 210

*The unidirectional printer attachment ignores this bit on an ICOL command with a modifier of 9 (FQ020).

Sense Command



See μINSTR-30.

Send Data Byte to Channel DBI

CCB 0 1 2	CCB 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
101 Sense	0 0 0 0 Sense Byte 0	Forms Hung Check (FR149, 249)	Horizontal Check*	Forms Runaway Check	End of Forms				
	0 0 0 1 Sense Byte 1	Serial Printer Not Ready	Wire Check			Memory Data Check	Print Emitter too Fast**	Unprintable Character	
	0 1 1 0 Interrupt Condition			Forms Busy Off	Print Busy Off				
	1 0 0 1 Memory Sense								
	1 0 1 0 Sense MAR								
	1 0 1 1 X'00' Diagnostic Sense								
	1 1 0 0 X'55' Diagnostic Sense								
	1 1 0 1 X'AA' Diagnostic Sense								
	1 1 1 0 X'FE' Diagnostic Sense								

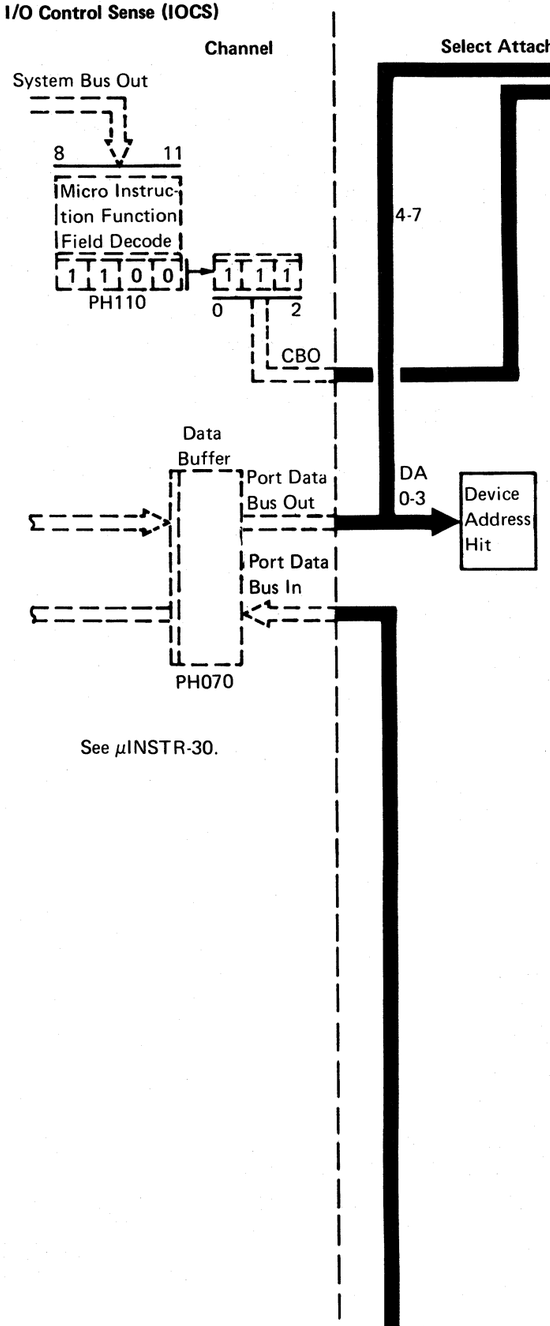
*Includes: Emitters out of order
Emitters too fast
Print head hung
Memory data check
Unprintable character
Printer not ready

**120 cps and 120 cps compatible attachments only.

Modifier: Port DBO 4, 5, 6, 7 (Hex)	Port DBI Bit	Command Bit	Action	FEALD Page
0000 (0)	0	Sense Byte 0	The forms motor hung latch is set on if forms emitter pulses aren't received for 125 ms when 'forms go' is active.	FR149, 249
	1		Sets any check dot to DBI 1. Any check refers to the last print operation and sets the horizontal check latch. Any of the following conditions may set this bit:	FR143, 243
			– Emitters out of order (sampled from the head direction latch).	FR110, 210
			– Emitters too fast (set by the emitters too fast check latch).	FR132, 232
			– Print head hung (set by the print head hung latch).	FR110, 210
			– Unprintable character (set by the invalid character latch because of an undefined character).	FR131, 231
			– Printer not ready (developed by sampling the +10.8 and +24 voltages. It is also forced by wire check).	
			– Memory data check (developed from memory data check latch).	FR131, 231
	2		Sets forms runaway latch if the time needed to move 127 lines is exceeded.	FR149, 249
	3		Sets end of forms latch if the end of forms switch senses the absence of forms.	FR143, 243
0001 (1)	0	Sense Byte 1	Serial printer not ready is a result of testing the printer ready line.	WK 120
	1		A wire check indicates that a print wire magnet was energized too long. It also forces byte 1 bit 0.	FR141, 241
	4	*Note:* These 5 bits also set bit 1 of byte 0 on.	A memory data check indicates that an out of parity byte was read out of ROS or RAM.	FR131, 231
	5		Print emitter too fast indicates that the print head is moving too fast for proper synchronization.	FR131, 231
	6		An unprintable character check indicates a character was requested but not defined (invalid character).	FR131, 231
0110 (6)	2	Interrupt Condition (+IOS Byte 6)	Reflects the status of the forms busy go latch.	FR147
	3		Reflects the status of the print busy latch.	FR126, 226
1001 (9)	—	Memory Sense (+IOS Byte 9)	Gates data from RAM or ROS to the DBI.	FR131, 231
1010 (A)	—	Sense MAR	Gates the value in MAR to the DBI.	FQ012
1011 (B)		Diagnostic Sense (+IOS Byte B)	Gates a hex 00 onto the DBI for diagnostic purposes.	
1100 (C)		Diagnostic Sense (+IOS Force 55)	Gates a hex 55 onto the DBI for diagnostic purposes.	FR151, 251 FR152, 252 FR153, 253 FR154, 254 FR155, 255
1101 (D)		Diagnostic Sense (+IOS Force AA)	Gates a hex AA onto the DBI for diagnostic purposes.	
1110 (E)		Diagnostic Sense (+IOS Force FE)	Gates a hex FE onto the DBI for diagnostic purposes.	

Control Sense Command

I/O Control Sense (IOCS)



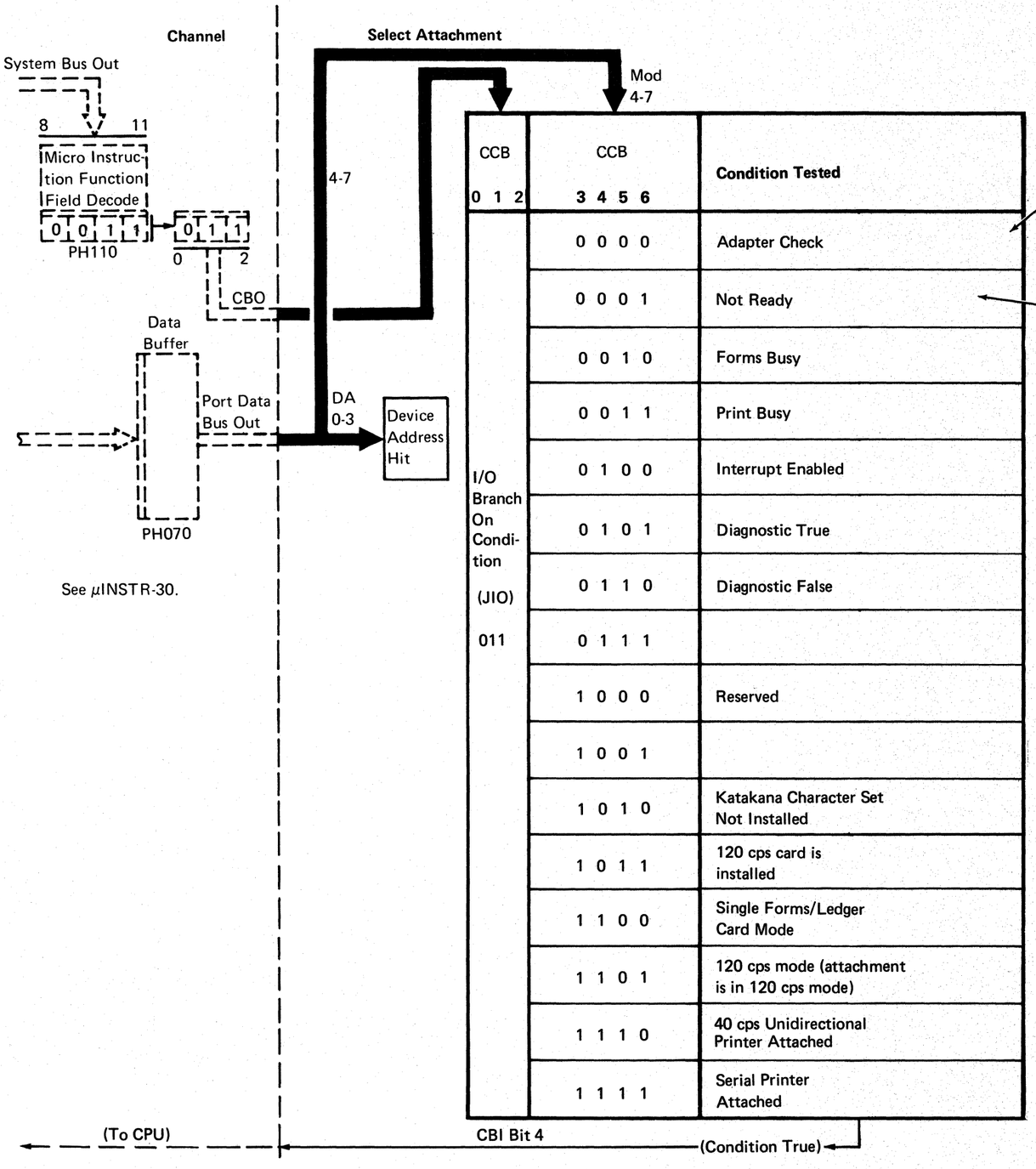
Send Data Byte to Channel DBI 0-7

CCB 0 1 2	CCB 3 4 5 6	DBI Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
111 Control Sense	0 0 0 0 Diagnostic Sense Bits				Print Right Selected			Emitter Interval Latch A	Emitter Interval Latch B
	0 0 0 1 Head Position Counter	1	2	4	8	16	32	64	128
	0 0 1 0 Diagnostic Inputs	Forms Emitter A	Forms Emitter B						Left Margin Switch
	0 1 0 0 Diagnostic Wrap	Wire 1	Wire 2	Wire 3	Wire 4	Wire 5	Wire 6	Wire 7	Wire 8
	0 1 0 1 Diagnostic Wrap	Forms Drive A		Forms Drive B		Serial Printer Reset	Print Drive A	Base Oscillator	Print Drive B
	0 1 1 1 Diagnostic Sense Mod 1	Emitter Event Counter 8	Emitter Event Counter 4	Emitter Event Counter 2	Emitter Event Counter 1	Start Trigger Set			
	1 0 0 1 Diagnostic Sense Mod 1	JK Multiplex DBO Bit 4	JK Multiplex DBO Bit 5	JK Multiplex DBO Bit 6	JK Multiplex DBO Bit 7	Emitter Column Counter (ECC) 4	Emitter Column Counter (ECC) 3	Emitter Column Counter (ECC) 2	Emitter Column Counter (ECC) 1
	1 0 1 0 Diagnostic Sense Mod 2					Motor Elapse Counter 8	Motor Elapse Counter 4	Motor Elapse Counter 2	Motor Elapse Counter 1
	1 0 1 1 Diagnostic Sense		Settle/Interval Counter Low 3	Low 2	Low 1	Motor Elapse Counter 128	Motor Elapse Counter 64	Motor Elapse Counter 32	Motor Elapse Counter 16
	1 1 0 0 Diagnostic Sense		Settle/Interval Counter High 6	High 5	High 4	Motor Event Counter 8	Motor Event Counter 4	Motor Event Counter 2	Motor Event Counter 1
	1 1 0 1 Diagnostic Sense	Forms Emitter Counter 3	Forms Emitter Counter 2	Forms Emitter Counter 1	Forms Emitter Counter 0		Head Compare Low	Head Compare Equal	Head Compare High
	1 1 1 0 Diagnostic Sense Mod 3					Forms Line/Print Time Counter 4	3	2	1
	1 1 1 1 Diagnostic Sense Mod 3					Forms Line/Print Time Counter 8	7	6	5

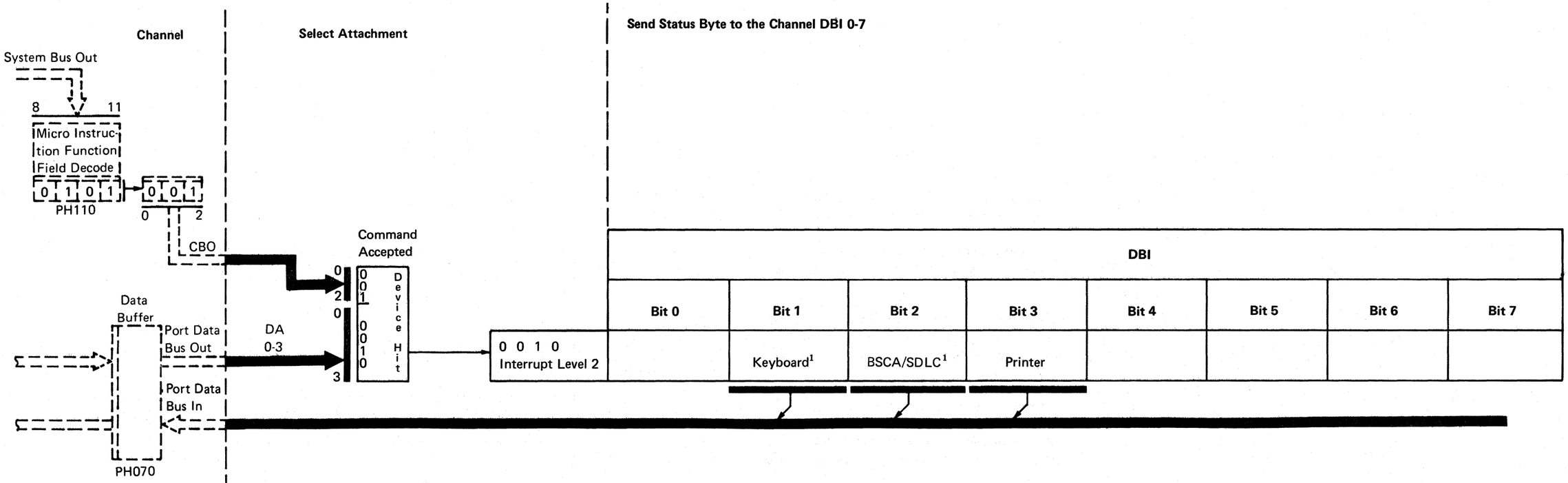
Modifier: Port DBO 4, 5, 6, 7 (Hex)	Port DBI Bit	Command	Action	FEALD Page
0000 (0)	4 6 7	Diagnostic Sense Bits (+ Control Sense Byte 0)	Print right selected Emitter interval Latch A Emitter interval Latch B } These signals are gated to the DBI for diagnostic purposes.	FR154, 254 FR155, 255 FR155, 255
0001 (1)	0-7	IOCS Head Position Counter	This command gates the value of the head position counter onto the DBI.	FR 112, 212
0010 (2)	0 1 7	Diagnostic Inputs (+ IOCS Byte 2)	Forms emitter A Forms emitter B Left margin switch } These signals are gated to the DBI for diagnostic purposes.	FR145, 245 FR145, 245 WK 120
0100 (4)	0-7	Diagnostic Wrap	Wire wrap data (1-8) used to test the print latches without actually printing.	FR143, 243
0101 (5)	0, 2 4 5 6 7	Diagnostic Sense	Forms drive A, Forms drive B Serial printer reset Print drive A Base oscillator Print drive B } These signals are gated to the DBI for diagnostic purposes.	FR145, 245 FR112, 212 FR157, 257 FR156, 256 FR157, 257
0111 (7)	0-3 4	Diagnostic Sense Mod 1	Sense emitter event counter (bit 0 = 8, bit 1 = 4, bit 2 = 2, bit 1 = 1 = 8 μs clock). Sense start trigger set.	FR114, 214 FR114, 214
1001 (9)	0-3 4-7	Diagnostic Sense Mod 1 (+ SNS Emitter Column Counter)	Gate multiplex JK bits 4-7 onto DBI bits 0-3 Gate the emitter column counter onto DBI 4-7.	FQ060 FR112, 212
1010 (A)	4-7	Diagnostic Sense Mod 2 (+ Control Sense Byte A)	Gates the results of the motor elapse counter (8, 4, 2, 1) onto the DBI.	FR127, 227
1011 (B)	1-3 4-7	Diagnostic Sense (+ IOCS Sense Byte B/ Settle/Interval Low)	Gates the settle/interval counter onto the DBI (low) Gates the results of the motor elapse counter (128, 64, 32, 16) onto the DBI.	FR145, 245 FR127, 227
1100 (C)	1-3 4-7	Diagnostic Sense (+ IOCS Sense Byte C/ Settle/Interval High)	Gates the settle/interval counter onto the DBI (high). Gates the results of the motor event counter onto the DBI.	FR145, 245 FR123, 223
1101 (D)	0-3 5-7	Diagnostic Sense (+ IOCS Sense Byte D)	Gates the results of the forms emitter counter onto the DBI Gates head compare low (bit 5), equal (bit 6) and high (bit 7) onto the DBI	FR143, 243 FR112, 212
1110 (E)	4-7	Diagnostic Sense Mod 3	Gates forms line/print time counter (low) onto the DBI	FR130, 230
1111 (F)	4-7	Diagnostic Sense Mod 3	Gates forms line/print time counter (high) onto the DBI.	FR130, 230

Jump Command

Jump I/O (JIO)



Sense Interrupt Level Status Byte (SILSB)



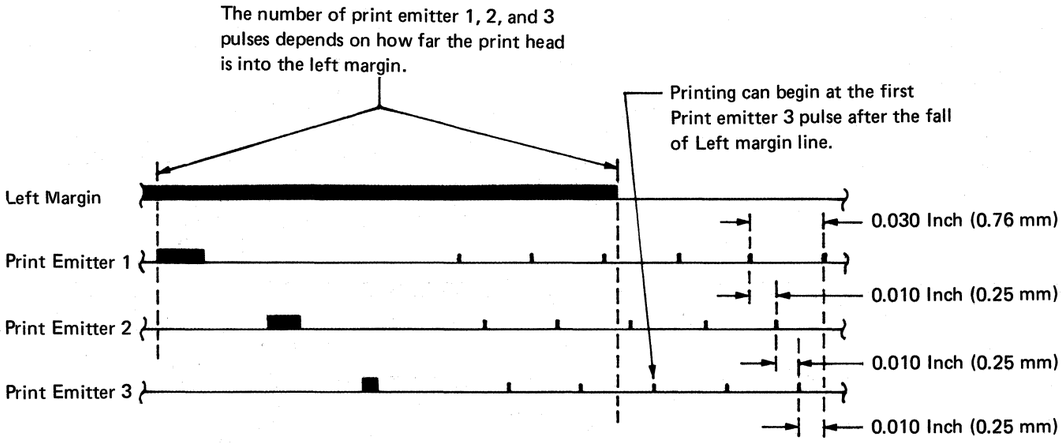
See μINSTR-30.

[1]The keyboard and BSCA/SDLC are also shown on this page because the keyboard, BSCA/SDLC, and the printer are on the same interrupt level.

ATTACHMENT FUNCTIONAL UNITS (40/80 cps only)

Print Emitter

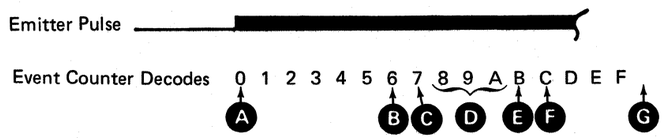
The print emitter **A** sends a pulse to the attachment for each 1/10 inch (0.254 mm) of print head movement. Print head direction determines the sequence of emitter pulses. 1, 2, 3, 1 equals left to right and 3, 2, 1, 3 equals right to left. The sequence is monitored by the 'emitter history' latch (FR110). Emitter pulses are used by the attachment to determine head position, head direction, and when to fire the print wire magnets.



Print Head Moving Left to Right

Print Emitter Event Counter (FR114)

Each print emitter pulse starts the emitter event counter **B**. It counts from hex 0 to F each time it is started and then stops at F. The following functions are performed at the indicated decodes of the event counter:



A – Event counter starts with the rise of any print emitter pulse.

B – If emitter is not still active, resets the event counter and waits for a longer emitter pulse.

C – Samples previous head direction and starts printing sequence.

D – Compares previous and present head directions.

E – Increases or decreases the emitter column counter.

F – Sets latches with present head direction and samples if emitter pulse is still active.

G – Resets event counter and waits for next emitter to start the event counter again.

Emitter Column Counter [ECC] (FR112)

The ECC (emitter column counter) **C** counts print emitter pulses from the serial printer, divides each print position into 10 equal parts, and sets MAR bits 5, 6, and 7 for RAM or ROS addressing. It also updates the print head position counter when the head is in the space between print positions.

Three models of the serial printer are bidirectional, consequently, the operation of the ECC is not the same for printing left to right as for printing right to left.

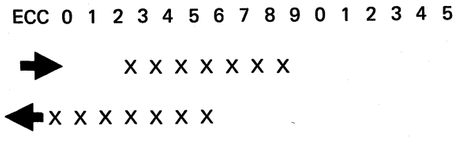
Printing Left to Right

The ECC counts up from 0 to 9 and then starts over again at zero. An emitter pulse occurs for each 1/100 inch (0.254 mm) of head movement. Each emitter pulse advances the ECC so that it counts from 0 to 9 for each 1/10 inch (2.54 mm) of print head movement. Each print position on the line is 1/10 inch and the ECC divides each position into 10 increments of time and distance.

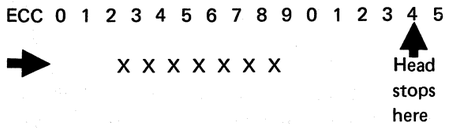
As the head moves to the right through a print position, print wire magnets may be fired on ECC counts 2 through 8. ECC counts 9, 0, and 1 become the column space (space between characters). When the count steps from 9 to 0, the print head position counter is increased by one.

Printing Right to Left (Bidirectional Only)

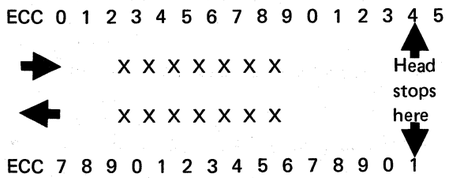
The ECC counts down from 9 to 0 and then starts over at nine. Print wire magnets can be fired on ECC counts 6 through 0. ECC counts of 9, 8, and 7 become the column space. When the count steps from 0 to 9, the value in the head position counter is decreased by one.



As shown in the preceding diagram, there is a three ECC count difference in the positioning of a character that is printed right and then printed left. This difference is compensated for in the turnaround sequence. Assume that the head printed the first character going right and then stopped moving with a count of 4 in the emitter column counter.



If the next character is to be printed going left, a value of 3 is subtracted from the ECC when the head changes direction.



If the first character had been printed going left and the second was to be printed going right, a value of 3 would have been *added* to the ECC when the head changed direction.

Print Head Position Counter (FR112)

The position of the print head on the print line is indicated by an eight position binary counter called the print head position counter D . The microprogram can sense the contents of the counter by using an IOCS command with a modifier of hex 01.

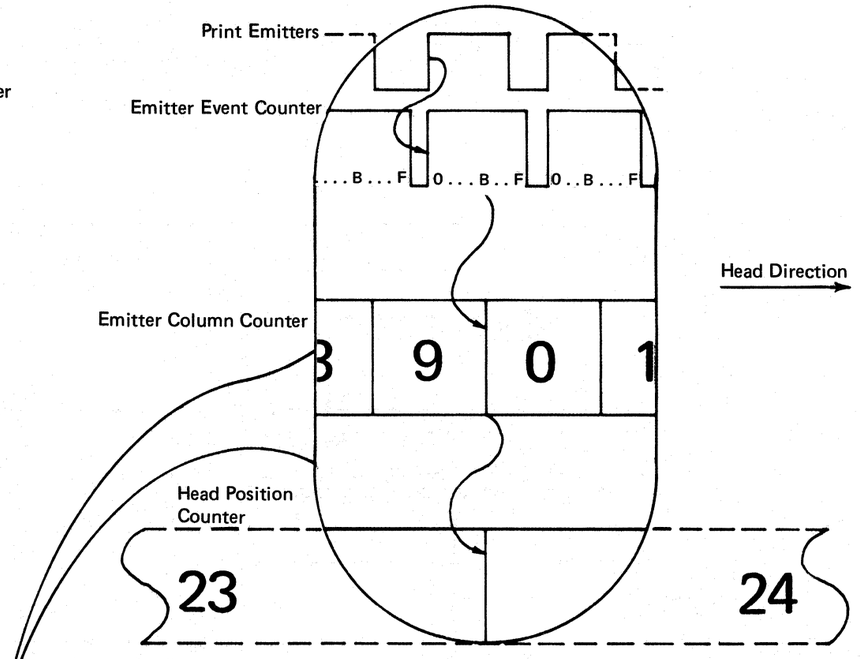
When print head motion is left to right, the contents of the head position counter is *increased* by one for every tenth emitter column counter pulse. The head position counter value is *decreased* in a similar manner when head motion is from right to left. When the head is at the right edge of the left margin, the value in the counter is hex 00.

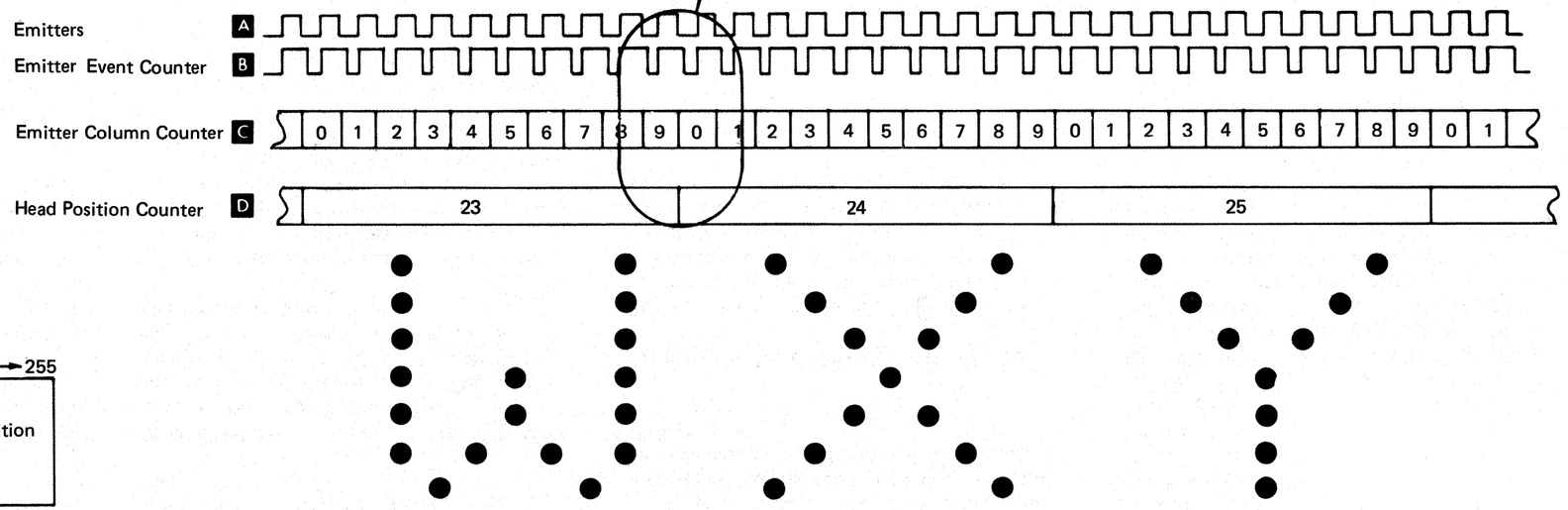
As the head moves left into the left margin, the counter goes from 00 to FF, FE, FD, to FC. Because these values are much larger than decimal 131, the attachment can determine if the head is in the left margin or to the right of print position 131.

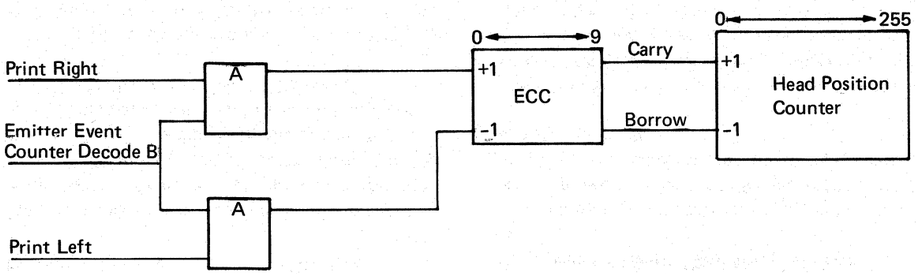
When the Fx value in the counter turns on the two high order bits, the 'buffer 6/7' latch is set to indicate that the head is in the left margin. When the two high order bits are on, that value is at least 192. Because it is impossible to move the head to the right as far as print position 192, it is assumed that the head is left of (or inside) the left margin.

Counter Relationships

1. Each print emitter pulse starts the print emitter event counter.
2. Print emitter event counter counts 0-F and advances the emitter column counter at hex B time.
3. Emitter column counter supplies MAR bits 5, 6, and 7 for ROS accessing of the wire image of the character.
4. Head position counter is stepped when the emitter column counter goes from 9 to 0. Head position counter supplies the RAM address for the EBCDIC character to be printed.







Memory Address Register (FQ014)

MAR is an eight bit register that is used to address either RAM or ROS. An eight bit register can only address 256 positions (0-255) or one page of storage. A set of latches (controlled by the attachment or an IOCL command) is used to select either RAM or ROS and the correct RAM/ROS page.

RAM has 512 positions and is divided into two pages of 256 bytes each. ROS has 1024 positions and is divided into four pages of 256 bytes each.

When loading the data buffer in RAM, the correct RAM/ROS page is selected by the microprogram and then MAR is set to each buffer address by the microprogram before transferring each EBCDIC character to the buffer. During printing, the head position counter sets an address into MAR for RAM accessing of the data buffer to get the EBCDIC code of the character to be printed.

Settle/Interval Counter (FR145)

A six position binary counter times the following functions:

1. The 50 ms start and stop settling times for the print head stepper motor, and the 50 ms stop settling time for the forms stepper motor.
2. The 1 ms stop interval for the forms stepper motor.
3. The 125 ms timeout for the print head hung check.
4. The 125 ms timeout for the forms hung check.
5. The 6 to 7 second timeout for the forms runaway check.

The rate of advancing the settle/interval counter is determined by the operation that is being performed.

Print Motor Event Counter (FR123)

This counter is a four position binary counter. It is used to access RAM for IMPL motor times while the print head stepper motor is in start, up-to-speed, and stop intervals.

The motor event counter starts with a value of zero. When the stepper motor is using start or up-to-speed intervals, advance pulses are allowed to increment the counter until it reaches a count of hex B. As long as the head is moving, the event counter is held at a count of hex B. When a stop sequence is initiated, the event counter is forced to hex C and then advanced to hex E. In other words, the counter is advanced by one up to hex B as long as RAM is being accessed for motor times, the print head stepper motor drive line phases are being switched, and a stop interval is not being initiated.

The motor event counter is reset to zero when the stop settle interval is ended. See *Print Motor Drive* in this section for information about motor intervals.

Print Motor Elapse Counter (FR127)

This is an eight position binary counter. It controls the length of time that the four stepper motor drive lines (A, not A, B, not B) are held in any given phase.

When the print head is moving, the 14 IMPL motor times are read out of RAM one at a time and set into the print motor elapse counter. The value in the counter is decremented by a 64 μs oscillator. When the counter reaches a value of one, two functions are performed:

1. The phase of the four stepper motor drive lines is changed to cause motor rotation. (The length of time that the drive lines are held in a given phase is the function of the value of the motor timings that are set into RAM at IMPL time.)
2. The print motor event counter is advanced. (See *Print Motor Drive* in this section for print operations.)

The print motor elapse counter is also used to time the two minute interval for head restoring.

After the execution of each I/O micro instruction, the counter is set with a value of 121. An oscillator begins to decrement that value. If the counter value reaches one before another I/O micro instruction is received by the attachment, the attachment restores the head to print head home position. (See *Head Restore* in this section.)

Forms Emitter Counter (FR143)

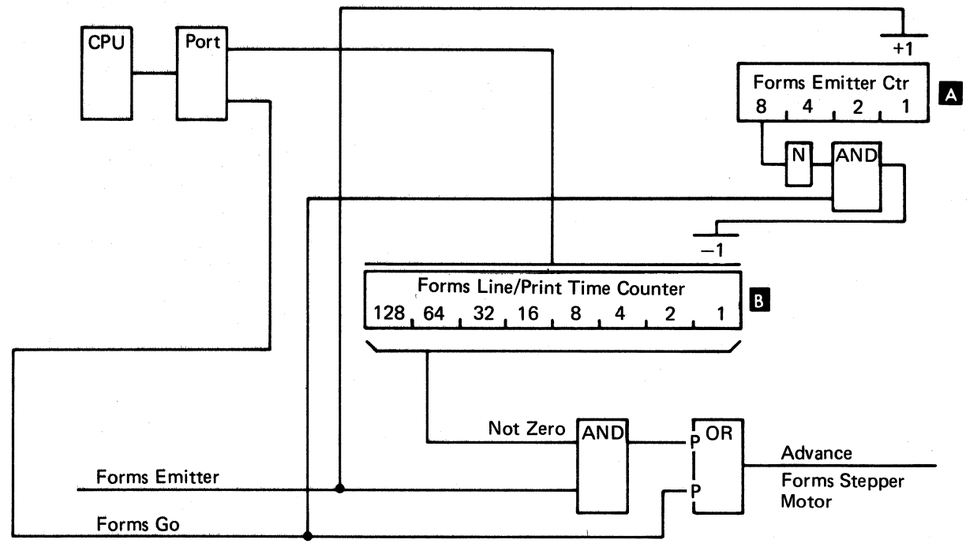
The forms emitter counter **A** is a four position binary counter. It is advanced by each forms emitter pulse. Each time the 8 latch of the counter is turned off (counter goes from F to 0), a value of one is subtracted from the forms line/print time counter.

Forms Line/Print Time Counter (FR130)

The forms line/print time counter **B** is an eight position binary counter. It is a multipurpose counter that is shared by forms and printing operations. In either case, a value is set into the counter and then reduced to provide a specific sequence of events or amount of time.

Forms Operation

When the forms line/print time counter is used for a forms operation, the number of lines plus one to be spaced is set into the counter before the 'forms go' line is activated. 'Forms go' starts the stepper motor and decreases the counter by one. Stepper motor rotation causes forms emitter pulses to advance the forms emitter counter. The sixteeth emitter pulse (one line was spaced) turns off the 8 latch in the forms emitter counter. Each time the 8 latch goes off, the forms line/print time counter is decremented by one. When the counter value gets to zero, forms go is deactivated and stops the stepper motor and emitter pulses. After a 50 ms settle time, none of the stepper motor drive lines is active.



Print Operation

The forms line/print time counter is used during a print operation to perform the following functions (see Storage Accessing—Print Timing Chart):

1. Delay the firing of print wire magnets until the latest print emitter pulse is checked for proper sequence and duration.

2. Control the length of time (one vertical row of dots) that print wire magnets are energized.

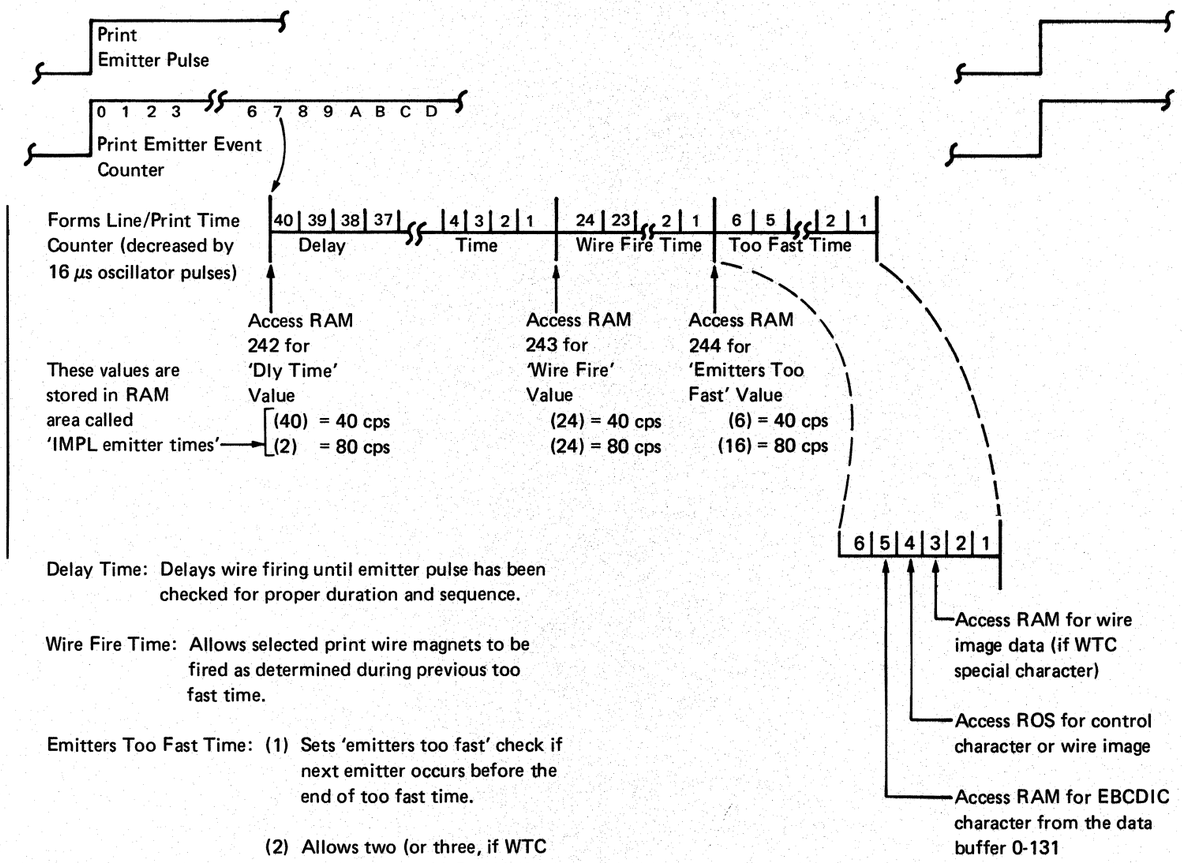
3. Monitor the frequency of print emitter pulses (emitters too fast check).

4. Time the readout of RAM and ROS for the configuration of print wire magnets to be fired during the next wire fire time (after the next emitter pulse is received from the printer).

During printing operations, this counter is used as a timer. It is set with some value and decremented to one. The time that elapses is determined by the value set into the counter. A 16 μs clock decrements the counter for the three IMPL emitter times.

The values of the IMPL emitter times are not the same for the 40 and 80 cps bidirectional printers because of speed differences. However, the IMPL emitter times are the same for both 40 cps printer models.

Storage Accessing—Print Timing Chart



Delay Time: Delays wire firing until emitter pulse has been checked for proper duration and sequence.

Wire Fire Time: Allows selected print wire magnets to be fired as determined during previous too fast time.

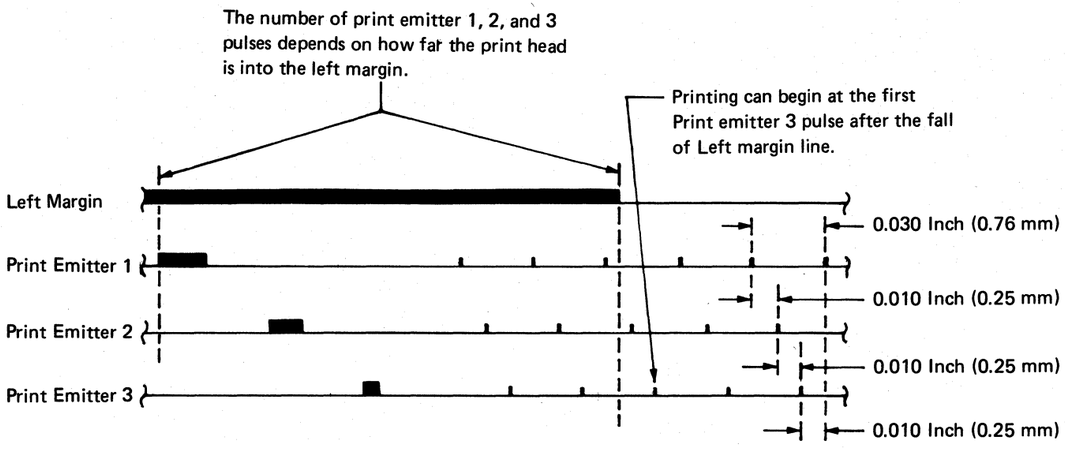
Emitters Too Fast Time: (1) Sets 'emitters too fast' check if next emitter occurs before the end of too fast time.

(2) Allows two (or three, if WTC special character) RAM/ROS accesses to determine which print wire magnets are to be fired during the next wire fire time.

ATTACHMENT FUNCTIONAL UNITS (40/80 cps — 120 compatible only)

Print Emitter

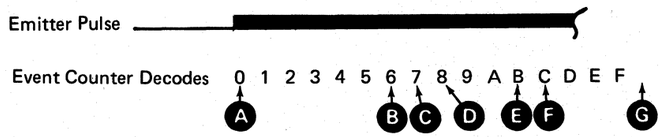
The print emitter A sends a pulse to the attachment for each 1/10 inch (0.254 mm) of print head movement. Print head direction determines the sequence of emitter pulses. 1, 2, 3, 1 equals left to right and 3, 2, 1, 3 equals right to left. The sequence is monitored by the 'emitter history' latch (FR210). Emitter pulses are used by the attachment to determine head position, head direction, and when to fire the print wire magnets.



Print Head Moving Left to Right

Print Emitter Event Counter (FR214)

Each print emitter pulse starts the emitter event counter B . It counts from hex 0 to F each time it is started and then stops at F. The following functions are performed at the indicated decodes of the event counter:



A — Event counter starts with the rise of any print emitter pulse.

B — If emitter is not still active, resets the event counter and waits for a longer emitter pulse.

C — Samples previous head direction and starts printing sequence.

D — Compares previous and present head directions.

E — Increases or decreases the emitter column counter.

F — Sets latches with present head direction and samples if emitter pulse is still active.

G — Resets event counter and waits for next emitter to start the event counter again.

Emitter Column Counter [ECC] (FR212)

The ECC (emitter column counter) C counts print emitter pulses from the serial printer, divides each print position into 10 equal parts, and sets MAR bits 5, 6, and 7 for RAM or ROS addressing. It also updates the print head position counter when the head is in the space between print positions.

Three models of the serial printer are bidirectional, consequently, the operation of the ECC is not the same for printing left to right as for printing right to left.

Printing Left to Right

The ECC counts up from 0 to 9 and then starts over again at zero. An emitter pulse occurs for each 1/100 inch (0.254 mm) of head movement. Each emitter pulse advances the ECC so that it counts from 0 to 9 for each 1/10 inch (2.54 mm) of print head movement. Each print position on the line is 1/10 inch and the ECC divides each position into 10 increments of time and distance.

As the head moves to the right through a print position, print wire magnets may be fired on ECC counts 1 through 7, ECC counts 8, 9 and 0 become the column space (space between characters). When the count steps from 9 to 0, the print head position counter is increased by one.

Printing Right to Left (Bidirectional Only)

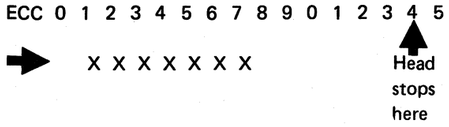
The ECC counts down from 9 to 0 and then starts over at nine. Print wire magnets can be fired on ECC counts 7 through 1. ECC counts of 0, 9 and 8 become the column space. When the count steps from 0 to 9, the value in the head position counter is decreased by one.

ECC 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5

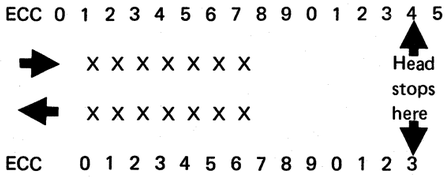
→ X X X X X X X

← X X X X X X X

As shown in the preceding diagram, there is a one ECC count difference in the positioning of a character that is printed right and then printed left. This difference is compensated for in the turnaround sequence. Assume that the head printed the first character going right and then stopped moving with a count of 4 in the emitter column counter.



If the next character is to be printed going left, a value of 1 is subtracted from the ECC when the head changes direction.



If the first character was to be printed going left and the second was to be printed going right, a value of 1 would be *added* to the ECC when the head changed direction.

Print Head Position Counter (FR212)

The position of the print head on the print line is indicated by an eight position binary counter called the print head position counter **D** . The microprogram can sense the contents of the counter by using an IOCS command with a modifier of hex 01.

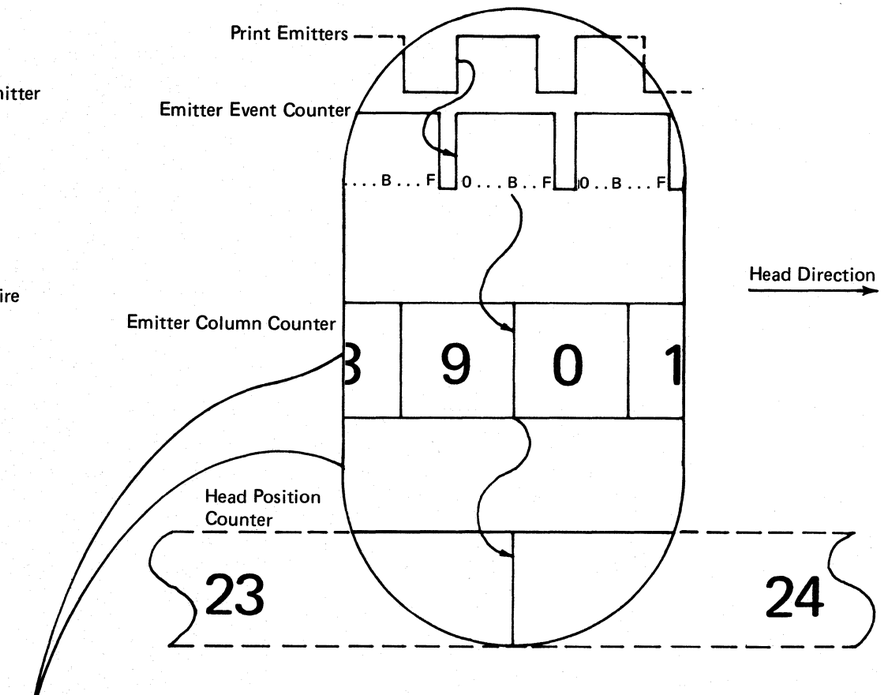
When print head motion is left to right, the contents of the head position counter is *increased* by one for every tenth emitter column counter pulse. The head position counter value is *decreased* in a similar manner when head motion is from right to left. When the head is at the right edge of the left margin, the value in the counter is hex 00.

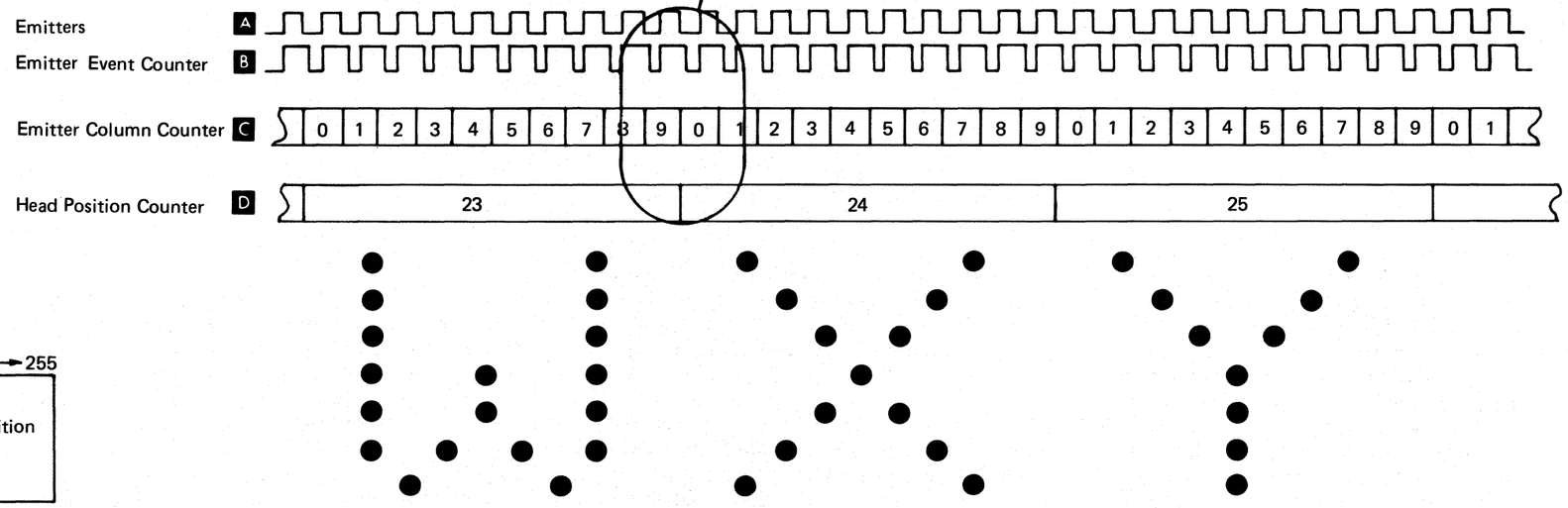
As the head moves left into the left margin, the counter goes from 00 to FF, FE, FD, to FC. Because these values are much larger than decimal 131, the attachment can determine if the head is in the left margin or to the right of print position 131.

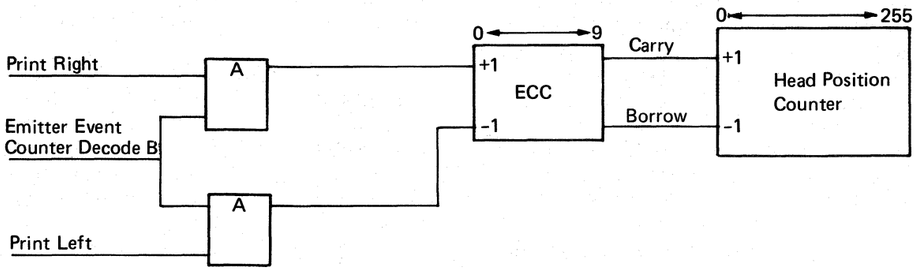
When the Fx value in the counter turns on the two high order bits, the 'buffer 6/7' latch is set to indicate that the head is in the left margin. When the two high order bits are on, that value is at least 192. Because it is impossible to move the head to the right as far as print position 192, it is assumed that the head is left of (or inside) the left margin.

Counter Relationships

1. Each print emitter pulse starts the print emitter event counter.
2. Print emitter event counter counts 0-F and advances the emitter column counter at hex B time.
3. Emitter column counter supplies MAR bits 5, 6, and 7 for ROS accessing of the wire image of the character.
4. Head position counter is stepped when the emitter column counter goes from 9 to 0. Head position counter supplies the RAM address for the EBCDIC character to be printed.







Memory Address Register (FQ014)

MAR is an eight bit register that is used to address either RAM or ROS. An eight bit register can only address 256 positions (0-255) or one page of storage. A set of latches (controlled by the attachment or an IOCL command) is used to select either RAM or ROS and the correct RAM/ROS page.

RAM has 512 positions and is divided into two pages of 256 bytes each. ROS has 1024 positions and is divided into four pages of 256 bytes each.

When loading the data buffer in RAM, the correct RAM/ROS page is selected by the microprogram and then MAR is set to each buffer address by the microprogram before transferring each EBCDIC character to the buffer. During printing, the head position counter sets an address into MAR for RAM accessing of the data buffer to get the EBCDIC code of the character to be printed.

Settle/Interval Counter (FR245)

A six position binary counter times the following functions:

1. The 50 ms start and stop settling times for the print head stepper motor, and the 50 ms stop settling time for the forms stepper motor.
2. The 1 ms stop interval for the forms stepper motor.
3. The 125 ms timeout for the print head hung check.
4. The 125 ms timeout for the forms hung check.
5. The 6 to 7 second timeout for the forms runaway check.

The rate of advancing the settle/interval counter is determined by the operation that is being performed.

Print Motor Event Counter (FR223)

This counter is a four position binary counter. It is used to access RAM for IMPL motor times while the print head stepper motor is in start, up-to-speed, and stop intervals.

The motor event counter starts with a value of zero. When the stepper motor is using start or up-to-speed intervals, advance pulses are allowed to increment the counter until it reaches a count of hex B. As long as the head is moving, the event counter is held at a count of hex B. When a stop sequence is initiated, the event counter is forced to hex C and then advanced to hex E. In other words, the counter is advanced by one up to hex B as long as RAM is being accessed for motor times, the print head stepper motor drive line phases are being switched, and a stop interval is not being initiated.

The motor event counter is reset to zero when the stop settle interval is ended. See *Print Motor Drive* in this section for information about motor intervals.

Print Motor Elapse Counter (FR227)

This is an eight position binary counter. It controls the length of time that the four stepper motor drive lines (A, not A, B, not B) are held in any given phase.

When the print head is moving, the 14 IMPL motor times are read out of RAM one at a time and set into the print motor elapse counter. The value in the counter is decremented by a 64 μs oscillator. When the counter reaches a value of one, two functions are performed:

1. The phase of the four stepper motor drive lines is changed to cause motor rotation. (The length of time that the drive lines are held in a given phase is the function of the value of the motor timings that are set into RAM at IMPL time.)
2. The print motor event counter is advanced. (See *Print Motor Drive* in this section for print operations.)

The print motor elapse counter is also used to time the two minute interval for head restoring.

After the execution of each I/O micro instruction, the counter is set with a value of 121. An oscillator begins to decrement that value. If the counter value reaches one before another I/O micro instruction is received by the attachment, the attachment restores the head to print head home position. (See *Head Restore* in this section.)

Forms Emitter Counter (FR243)

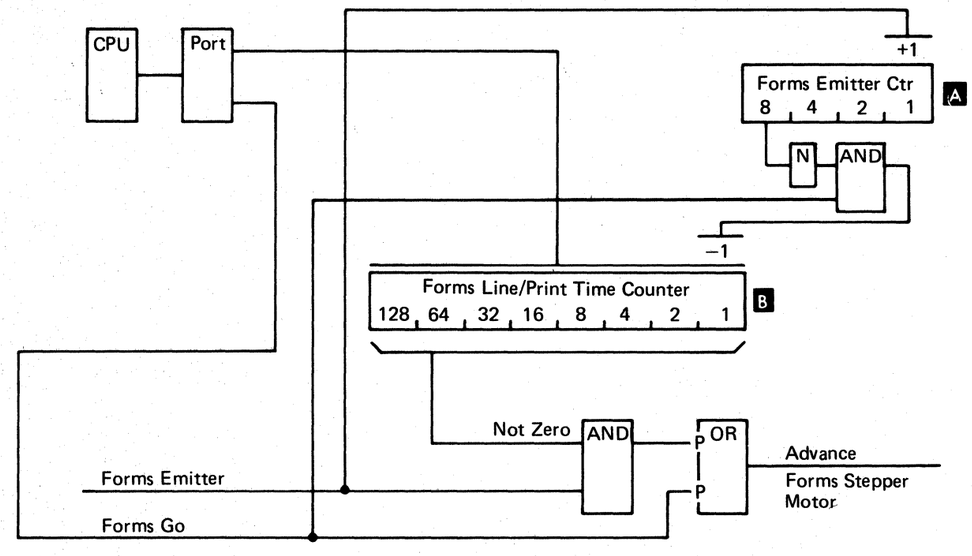
The forms emitter counter **A** is a four position binary counter. It is advanced by each forms emitter pulse. Each time the 8 latch of the counter is turned off (counter goes from F to 0), a value of one is subtracted from the forms line/print time counter.

Forms Line/Print Time Counter (FR230)

The forms line/print time counter **B** is an eight position binary counter. It is a multipurpose counter that is shared by forms and printing operations. In either case, a value is set into the counter and then reduced to provide a specific sequence of events or amount of time.

Forms Operation

When the forms line/print time counter is used for a forms operation, the number of lines plus one to be spaced is set into the counter before the 'forms go' line is activated. 'Forms go' starts the stepper motor and decreases the counter by one. Stepper motor rotation causes forms emitter pulses to advance the forms emitter counter. The sixteeth emitter pulse (one line was spaced) turns off the 8 latch in the forms emitter counter. Each time the 8 latch goes off, the forms line/print time counter is decremented by one. When the counter value gets to zero, forms go is deactivated and stops the stepper motor and emitter pulses. After a 50 ms settle time, none of the stepper motor drive lines is active.



Print Operation

The forms line/print time counter is used during a print operation to perform the following functions (see Storage Accessing—Print Timing Chart):

1. Delay the firing of print wire magnets until the latest print emitter pulse is checked for proper sequence and duration.

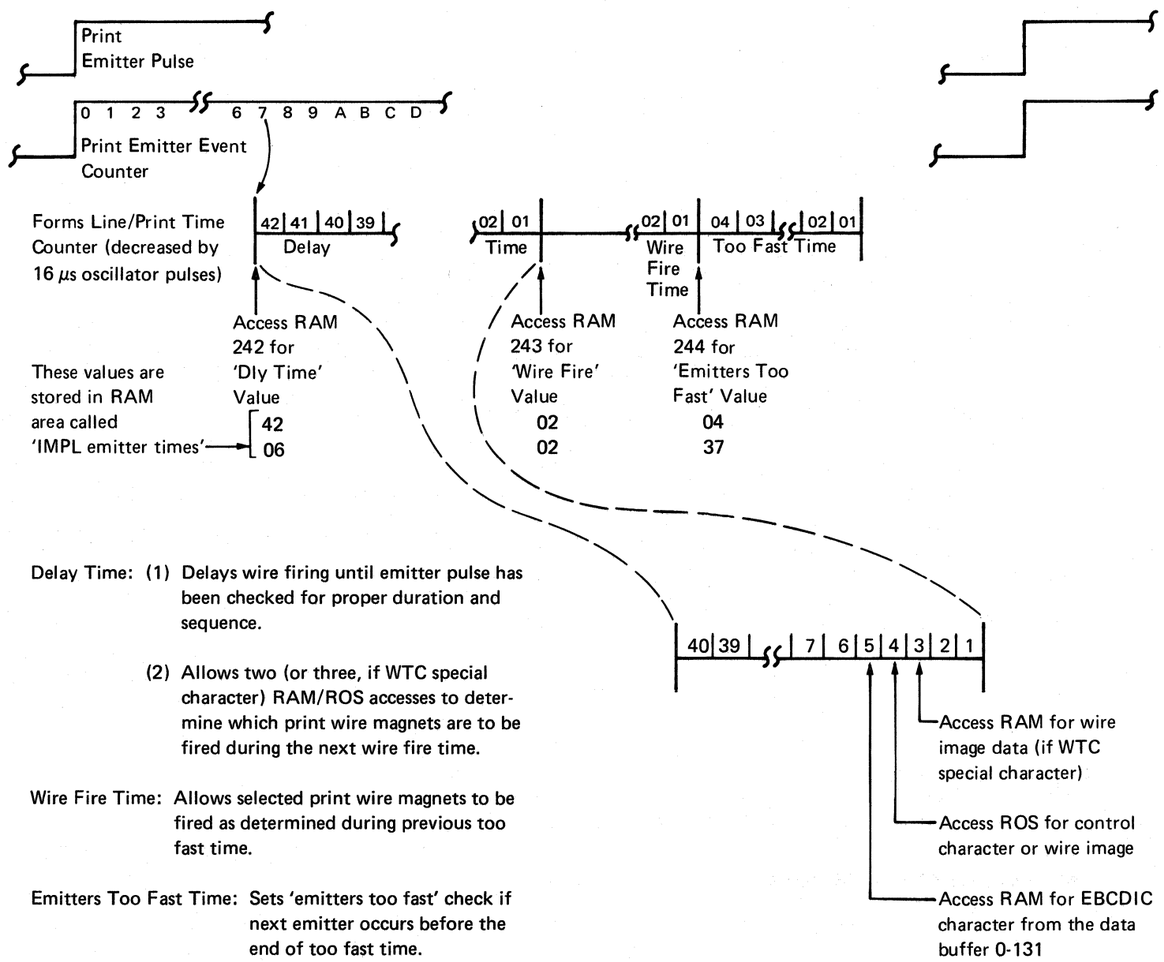
2. Control the length of time (one vertical row of dots) that print wire magnets are energized.

3. Monitor the frequency of print emitter pulses (emitters too fast check).

4. Time the readout of RAM and ROS for the configuration of print wire magnets to be fired during the next wire fire time (after the next emitter pulse is received from the printer).

During printing operations, this counter is used as a timer. It is set with some value and decremented to one. The time that elapses is determined by the value set into the counter. A 16 μs clock decrements the counter for the three IMPL emitter times.

Storage Accessing—Print Timing Chart



Delay Time: (1) Delays wire firing until emitter pulse has been checked for proper duration and sequence.

(2) Allows two (or three, if WTC special character) RAM/ROS accesses to determine which print wire magnets are to be fired during the next wire fire time.

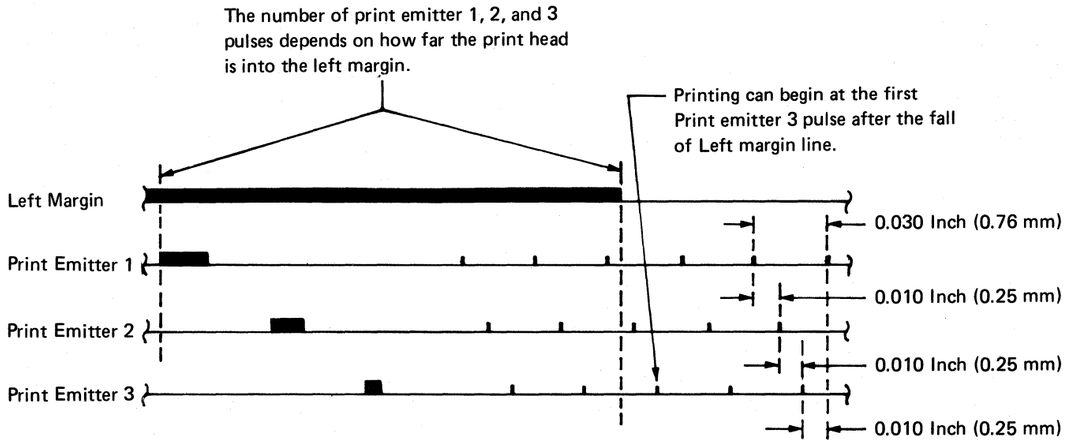
Wire Fire Time: Allows selected print wire magnets to be fired as determined during previous too fast time.

Emitters Too Fast Time: Sets 'emitters too fast' check if next emitter occurs before the end of too fast time.

ATTACHMENT FUNCTIONAL UNITS (120 cps printer only)

Print Emitter

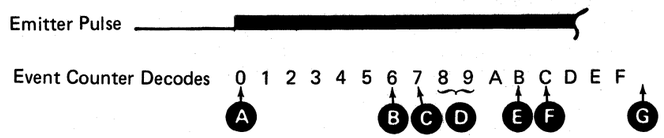
The print emitter **A** sends a pulse to the attachment for each 1/10 inch (0.254 mm) of print head movement. Print head direction determines the sequence of emitter pulses. 1, 2, 3, 1 equals left to right and 3, 2, 1, 3 equals right to left. The sequence is monitored by the 'emitter history' latch (FR210). Emitter pulses are used by the attachment to determine head position, head direction, and when to fire the print wire magnets.



Print Head Moving Left to Right

Print Emitter Event Counter (FR214)

Each print emitter pulse starts the emitter event counter **B**. It counts from hex 0 to F each time it is started and then stops at F. The following functions are performed at the indicated decodes of the event counter:



A — Event counter starts with the rise of any print emitter pulse.

B — If emitter is not still active, resets the event counter and waits for a longer emitter pulse.

C — Samples previous head direction and starts printing sequence.

D — Compares previous and present head directions.

E — Increases or decreases the emitter column counter.

F — Sets latches with present head direction and samples if emitter pulse is still active.

G — Resets event counter and waits for next emitter to start the event counter again.

Emitter Column Counter [ECC] (FR212)

The ECC (emitter column counter) **C** counts print emitter pulses from the serial printer, divides each print position into 10 equal parts, and sets MAR bits 5, 6, and 7 for RAM or ROS addressing. It also updates the print head position counter when the head is in the space between print positions.

Printing Left to Right

The ECC counts up from 0 to 9 and then starts over again at zero. An emitter pulse occurs for each 1/100 inch (0.254 mm) of head movement. Each emitter pulse advances the ECC so that it counts from 0 to 9 for each 1/10 inch (2.54 mm) of print head movement. Each print position on the line is 1/10 inch and the ECC divides each position into 10 increments of time and distance.

As the head moves to the right through a print position, print wire magnets may be fired on ECC counts 1 through 7. ECC counts 8, 9, and 0 become the column space (space between characters). When the count steps from 9 to 0, the print head position counter is increased by one.

Printing Right to Left (Bidirectional Only)

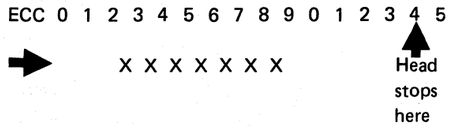
The ECC counts down from 9 to 0 and then starts over at nine. Print wire magnets can be fired on ECC counts 7 through 1. ECC counts of 0, 9, and 8 become the column space. When the count steps from 0 to 9, the value in the head position counter is decreased by one.

ECC 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5

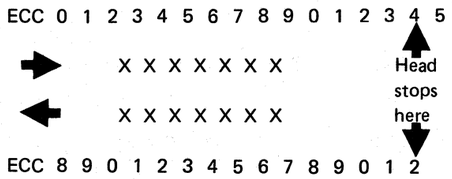
→ X X X X X X X

← X X X X X X X

As shown in the preceding diagram, there is a two ECC count difference in the positioning of a character that is printed right and then printed left. This difference is compensated for in the turnaround sequence. Assume that the head printed the first character going right and then stopped moving with a count of 4 in the emitter column counter.



If the next character is to be printed going left, a value of 2 is subtracted from the ECC when the head changes direction.



If the first character was printed going left and the second was to be printed going right, a value of 2 would be *added* to the ECC when the head changed direction.

Print Head Position Counter (FR212)

The position of the print head on the print line is indicated by an eight position binary counter called the print head position counter D . The microprogram can sense the contents of the counter by using an IOCS command with a modifier of hex 01.

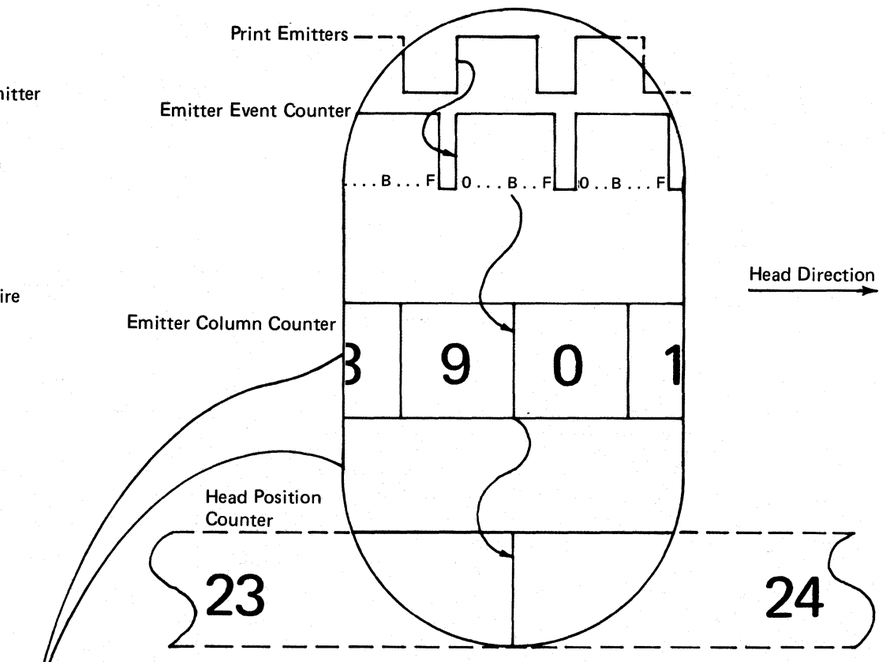
When print head motion is left to right, the contents of the head position counter is *increased* by one for every tenth emitter column counter pulse. The head position counter value is *decreased* in a similar manner when head motion is from right to left. When the head is at the right edge of the left margin, the value in the counter is hex 00.

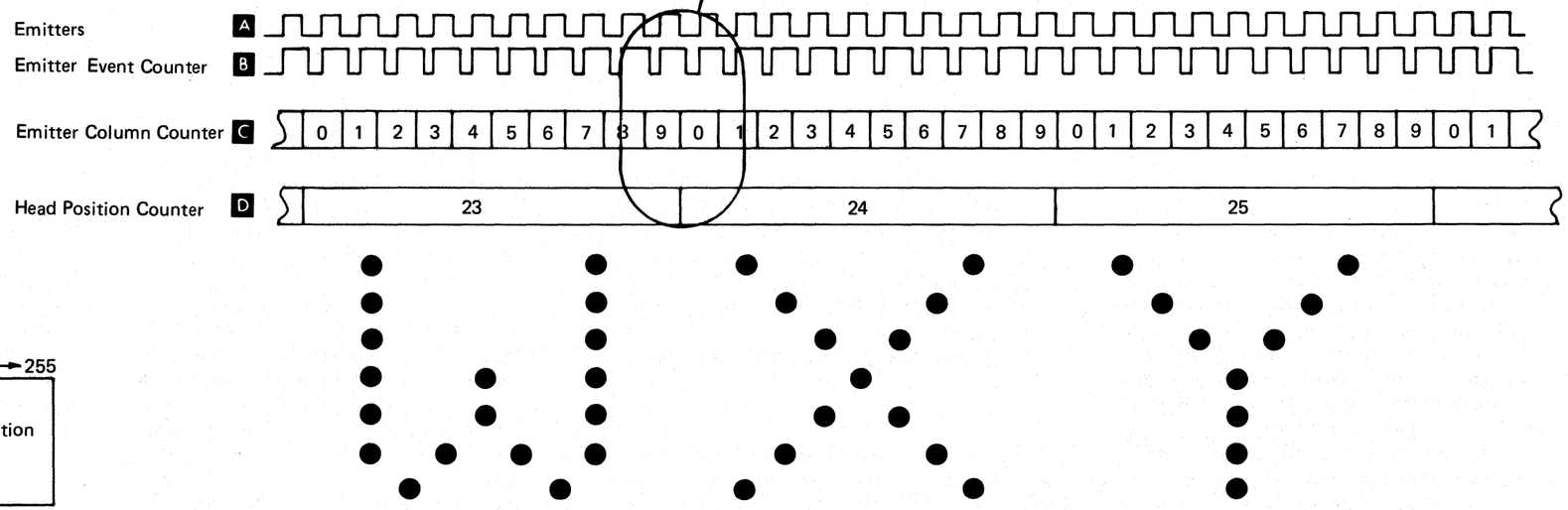
As the head moves left into the left margin, the counter goes from 00 to FF, FE, FD, to FC. Because these values are much larger than decimal 131, the attachment can determine if the head is in the left margin or to the right of print position 131.

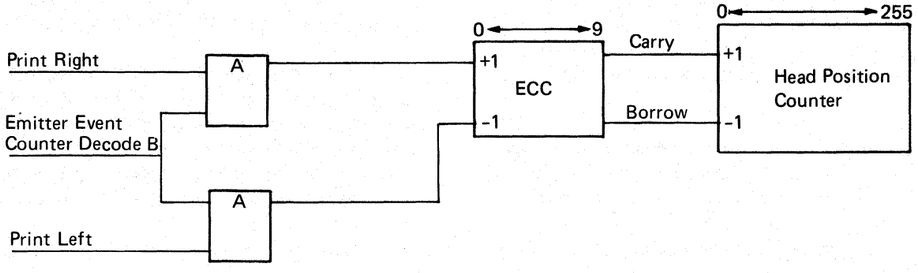
When the Fx value in the counter turns on the two high order bits, the 'buffer 6/7' latch is set to indicate that the head is in the left margin. When the two high order bits are on, that value is at least 192. Because it is impossible to move the head to the right as far as print position 192, it is assumed that the head is left of (or inside) the left margin.

Counter Relationships

1. Each print emitter pulse starts the print emitter event counter.
2. Print emitter event counter counts 0-F and advances the emitter column counter at hex B time.
3. Emitter column counter supplies MAR bits 5, 6, and 7 for ROS accessing of the wire image of the character.
4. Head position counter is stepped when the emitter column counter goes from 9 to 0. Head position counter supplies the RAM address for the EBCDIC character to be printed.







Memory Address Register (FQ014)

MAR is an eight bit register that is used to address either RAM or ROS. An eight bit register can only address 256 positions (0-255) or one page of storage. A set of latches (controlled by the attachment or an IOCL command) is used to select either RAM or ROS and the correct RAM/ROS page.

RAM has 512 positions and is divided into two pages of 256 bytes each. ROS has 1024 positions and is divided into four pages of 256 bytes each.

When loading the data buffer in RAM, the correct RAM/ROS page is selected by the microprogram and then MAR is set to each buffer address by the microprogram before transferring each EBCDIC character to the buffer. During printing, the head position counter sets an address into MAR for RAM accessing of the data buffer to get the EBCDIC code of the character to be printed.

Settle/Interval Counter (FR245)

A six position binary counter times the following functions:

1. The 50 ms start and stop settling times for the print head stepper motor, and the 50 ms stop settling time for the forms stepper motor.
2. The 1 ms stop interval for the forms stepper motor.
3. The 125 ms timeout for the print head hung check.
4. The 125 ms timeout for the forms hung check.
5. The 6 to 7 second timeout for the forms runaway check.

The rate of advancing the settle/interval counter is determined by the operation that is being performed.

Print Motor Event Counter (FR223)

This counter is a four position binary counter. It is used to access RAM for IMPL motor times while the print head stepper motor is in start, up-to-speed, and stop intervals.

The motor event counter starts with a value of zero. When the stepper motor is using start or up-to-speed intervals, advance pulses are allowed to increment the counter until it reaches a count of hex B. As long as the head is moving, the event counter is held at a count of hex B. When a stop sequence is initiated, the event counter is forced to hex C and then advanced to hex E. In other words, the counter is advanced by one up to hex B as long as RAM is being accessed for motor times, the print head stepper motor drive line phases are being switched, and a stop interval is not being initiated.

The motor event counter is reset to zero when the stop settle interval is ended. See *Print Motor Drive* in this section for information about motor intervals.

Print Motor Elapse Counter (FR227)

This is an eight position binary counter. It controls the length of time that the four stepper motor drive lines (A, not A, B, not B) are held in any given phase.

When the print head is moving, the 14 IMPL motor times are read out of RAM one at a time and set into the print motor elapse counter. The value in the counter is decremented by a 64 μs oscillator. When the counter reaches a value of one, two functions are performed:

1. The phase of the four stepper motor drive lines is changed to cause motor rotation. (The length of time that the drive lines are held in a given phase is the function of the value of the motor timings that are set into RAM at IMPL time.)
2. The print motor event counter is advanced. (See *Print Motor Drive* in this section for print operations.)

The print motor elapse counter is also used to time the two minute interval for head restoring.

After the execution of each I/O micro instruction, the counter is set with a value of 121. An oscillator begins to decrement that value. If the counter value reaches one before another I/O micro instruction is received by the attachment, the attachment restores the head to print head home position. (See *Head Restore* in this section.)

Forms Emitter Counter (FR243)

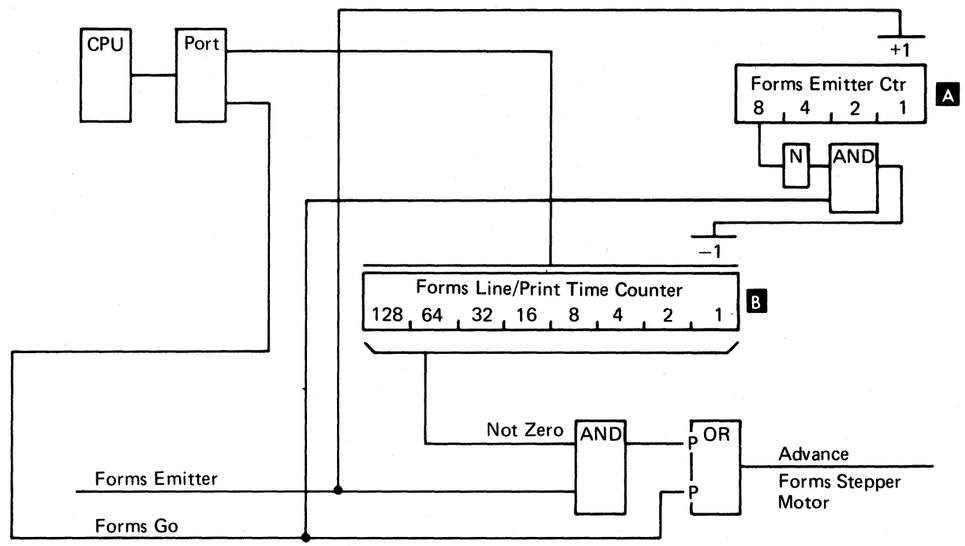
The forms emitter counter **A** is a four position binary counter. It is advanced by each forms emitter pulse. Each time the 8 latch of the counter is turned off (counter goes from F to 0), a value of one is subtracted from the forms line/print time counter.

Forms Line/Print Time Counter (FR230)

The forms line/print time counter **B** is an eight position binary counter. It is a multipurpose counter that is shared by forms and printing operations. In either case, a value is set into the counter and then reduced to provide a specific sequence of events or amount of time.

Forms Operation

When the forms line/print time counter is used for a forms operation, the number of lines plus one to be spaced is set into the counter before the 'forms go' line is activated. 'Forms go' starts the stepper motor and decreases the counter by one. Stepper motor rotation causes forms emitter pulses to advance the forms emitter counter. The sixteeth emitter pulse (one line was spaced) turns off the 8 latch in the forms emitter counter. Each time the 8 latch goes off, the forms line/print time counter is decremented by one. When the counter value gets to zero, forms go is deactivated and stops the stepper motor and emitter pulses. After a 50 ms settle time, none of the stepper motor drive lines is active.



Print Operation

The forms line/print time counter is used during a print operation to perform the following functions (see Storage Accessing—Print Timing Chart):

1. Delay the firing of print wire magnets until the latest print emitter pulse is checked for proper sequence and duration.

2. Control the length of time (one vertical row of dots) that print wire magnets are energized.

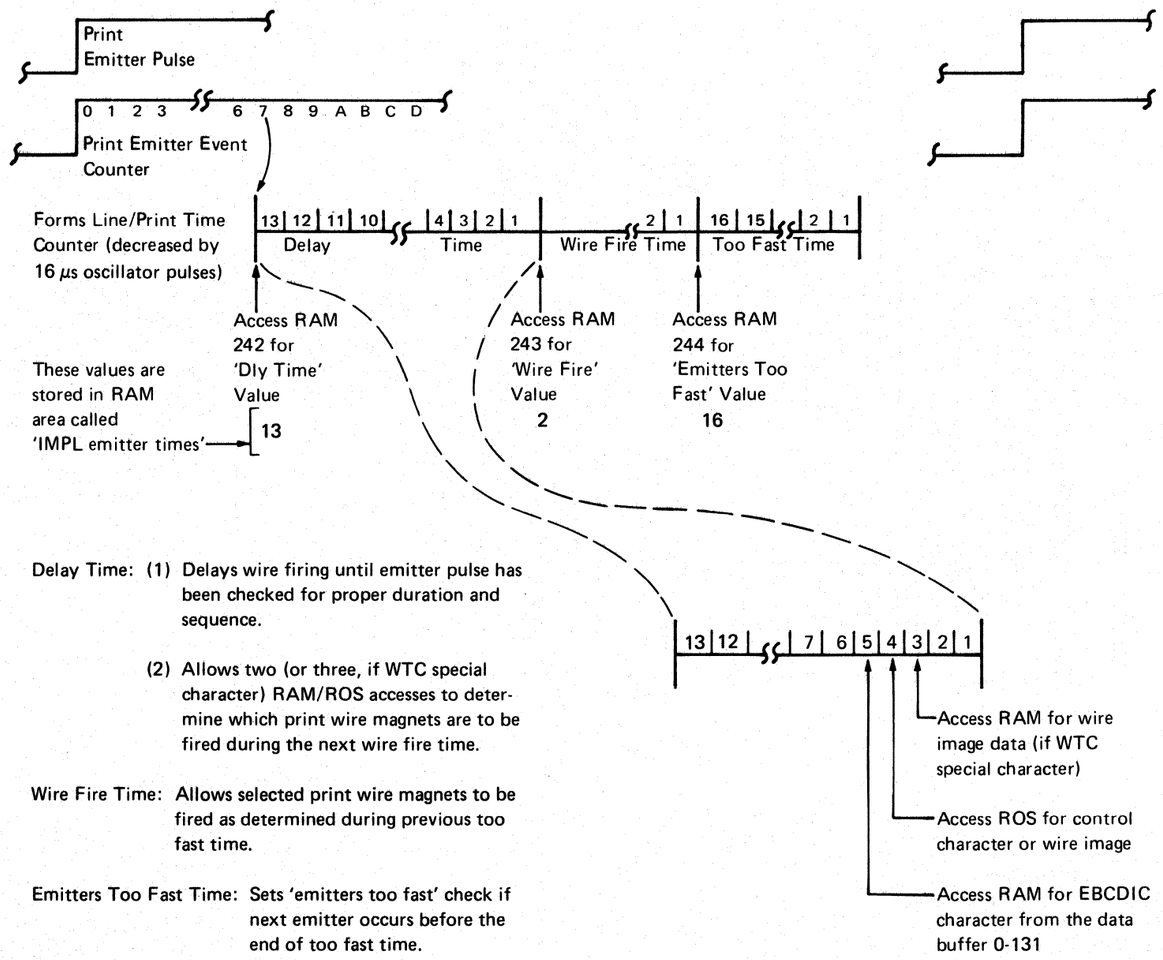
3. Monitor the frequency of print emitter pulses (emitters too fast check).

4. Time the readout of RAM and ROS for the configuration of print wire magnets to be fired during the next wire fire time (after the next emitter pulse is received from the printer).

During printing operations, this counter is used as a timer. It is set with some value and decremented to one. The time that elapses is determined by the value set into the counter. A 16 μs clock decrements the counter for the three IMPL emitter times.

The values of the IMPL emitter times are not the same for the three models of bidirectional printers, because of speed differences. However, the IMPL emitter times are the same for both 40 cps printer models.

Storage Accessing—Print Timing Chart



Delay Time: (1) Delays wire firing until emitter pulse has been checked for proper duration and sequence.

(2) Allows two (or three, if WTC special character) RAM/ROS accesses to determine which print wire magnets are to be fired during the next wire fire time.

Wire Fire Time: Allows selected print wire magnets to be fired as determined during previous too fast time.

Emitters Too Fast Time: Sets 'emitters too fast' check if next emitter occurs before the end of too fast time.

ROS ADDRESSING

The 56 characters that are the same for U.S., WTC, and ASCII character sets are stored in ROS. The other eight characters are stored in RAM. For these eight characters, ROS contains addresses for RAM accesses to get the wire image of the eight changeable special characters.

Each wire image in ROS uses 8 bytes. The first byte of each image is the control byte that denotes whether the character is valid, invalid, or one of the eight changeable special characters. The next seven consecutive bytes store the wire image of the character (or the RAM address of the wire image of the special characters).

As shown in the illustration, ROS is divided into four parts called *pages*. Each page contains 256 addresses. Paging is controlled by bits 0, 1, and 2 of the EBCDIC byte that is read out of RAM data buffer **A**.

Bit 0	Bit 1	Bit 2	Addresses
0	1	0	0-255
0	1	1	256-511
1	1	0	512-767
1	1	1	768-1023

To print a character in print position 1, RAM is accessed at the first position of the data buffer, and an EBCDIC character is set into the RAM data register. Bits 0, 1, and 2 of the character are decoded to determine which page of ROS contains the wire image of the EBCDIC character.

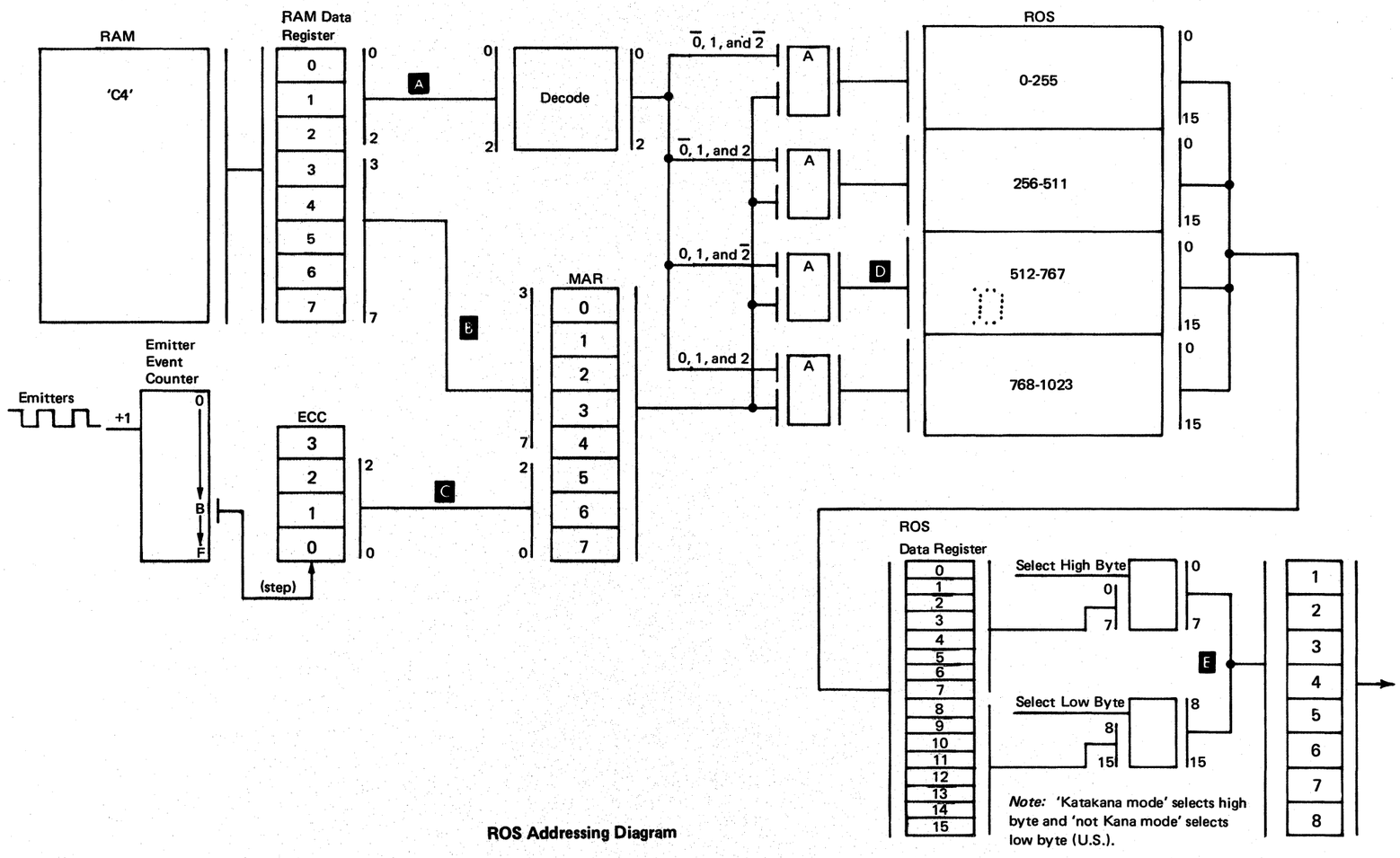
On the same access, MAR is forced to the ROS address of the control byte of the wire image of the character to be printed. Bits 3-7 of the RAM data register are set into positions 0-4 of MAR **B**. Positions 5-7 of MAR are set to the value of 000 from the emitter column counter **C**. Essentially, bits 0-4 of MAR determine the amount of displacement into the ROS page, and bits 5-7 determine which of the 8 bytes of the wire image to read out.

For example, to print the letter D in print position 1, hex C4 was loaded into the first position of the data buffer in RAM. When this byte is read out of the buffer while printing, bits 0, 1, and 5 (hex C4) are set on in the RAM data register. Because bits 0 and 1 are on and bit 2 is off, the wire image for the letter D is stored somewhere in the 512-767 address range of ROS **D**. Bits 0-4 of MAR are set to 00100 from positions 3-7 of the RAM data register because bit 5 was on in the data register.

On this first of eight ROS accesses, the emitter column counter value is 000. This counter value is set into positions 5-7 of MAR. In binary, the MAR contents (00100000) add up to 32. When 32 is added to the paging value of 512, the address of the control byte of the letter D becomes ROS location 544.

The emitter column counter value is stepped up by 1 each time a print head emitter pulse is received. The value 001 is forced into positions 5-7 of MAR on the next emitter pulse and the MAR address is now at 545. This second ROS access is the first that could contain wire image data because the first byte is the control byte. As subsequent emitter pulses advance the emitter column counter, its value is forced into positions 5-7 of MAR, and consecutive ROS positions are accessed until the entire wire image of the letter D is printed.

Each position of ROS is 2 bytes wide (1K x 18 module). When a position of ROS is accessed, 16 significant bits can be read out into the ROS data register. Either the high or low byte can be gated out of the data register **E**. Bit 1 of the EBCDIC character that is read out of RAM determines whether the high or low byte is gated out of ROS. If bit 1 is on, the low byte (U.S.) is used; if the bit is off, the high byte (Katakana) is used.



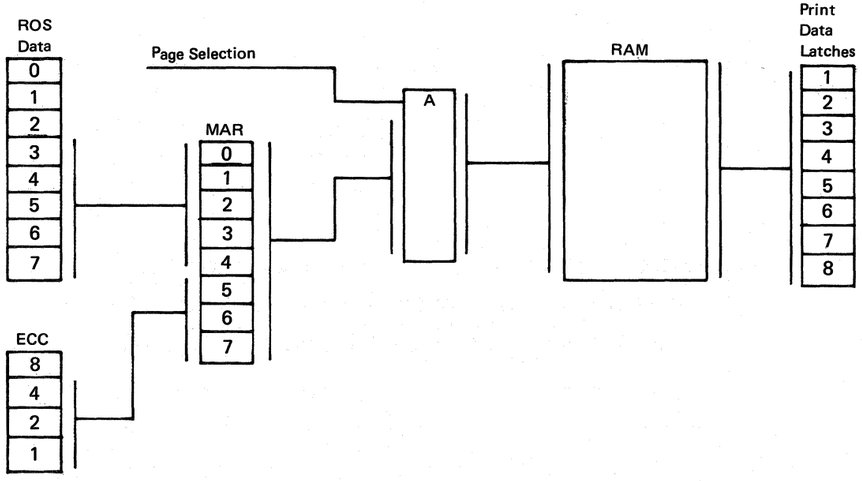
ROS Addressing Diagram

WTC/ASCII/U.S. Special Character Addressing

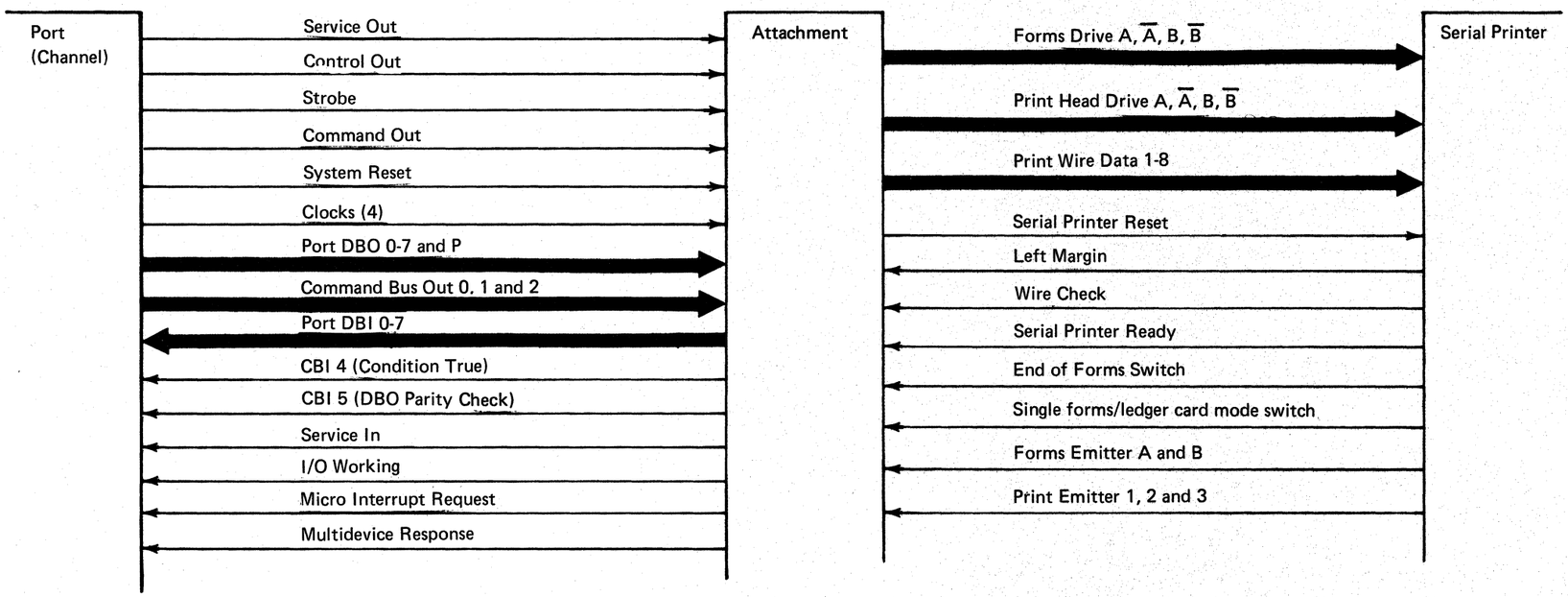
ROS contains the wire images of the U.S., WTC, and ASCII characters that do not change. There are eight EBCDIC codes that can represent various graphic symbols depending upon which language is being used.

At IMPL time, the wire images of the eight symbols that are unique to the language specified by the user are loaded into *RAM*. When one of the eight EBCDIC codes is loaded into the data buffer to be printed, RAM is accessed for the EBCDIC code and ROS is accessed for the control character that denotes WTC/ASCII/U.S. changeable special character. This sets a latch called 'WTC/ASCII' that stays on for the entire character.

When the 'WTC/ASCII' latch is on, ROS data is used with the value in the emitter column counter to develop the RAM address of the wire image of the special character.



INPUT/OUTPUT LINES



ERROR CONDITIONS

Microprogramming checks a print or forms operation by issuing IOS commands to the attachment after the print or forms operation is complete. If any of the eight check conditions occurred during the print or forms operation, the attachment sets bits on in sense bytes 0/1 to communicate which checks occurred (see IOS command under *Commands* in this section).

The following is a list of the meanings of the bits in sense bytes 0 and 1:

Byte 0, Bit 0 — Forms Hung Check

This check monitors the forms emitter lines any time the 'forms go' line is active. If the emitter pulses do not occur within 125 ms of each other, the forms hung check is set on.

Byte 0, Bit 1 — Horizontal Check

This check indicates that an error occurred in the last print operation (as opposed to a forms operation). It can be set on by the following error conditions:

Emitters Out Of Order

When the head is going to the right, the sequence of emitters should be 1, 2, 3, 1. When the head is going to the left, the sequence should be 3, 2, 1, 3. If the emitter sequence is not valid for the defined head direction, this error condition turns on the horizontal check.

Print Head Hung

If the print head stepper motor is being told to go and there are no print head emitter pulses for 125 ms from the printer, print head hung is set on.

Emitters Too Fast

This error condition indicates that the print head is being moved across the line too fast for proper synchronization for print alignment.

Memory Data Check

This condition indicates that an even parity byte was read out of ROS or RAM.

Unprintable Character Check

This condition indicates that a character was requested for printing that was not in the defined character set. The condition occurs when the position of ROS that is addressed is coded as an invalid character by its control byte. A check will occur only if unprintable character check has been enabled by bit 0 of the flag byte in the IOB. If the check has not been enabled, a blank (space) will be printed.

Printer Not Ready

The printer is not ready any time the +10.8 volt supply is undervoltage, +24 volt supply is undervoltage or overvoltage, or when a wire check occurs. (Wire check is described later in this topic.)

Byte 0, Bit 2 — Forms Runaway Check

This check monitors the time from when the 'forms go' line becomes active until the forms line/print time counter gets to zero. If this time exceeds the time needed to move 127 lines, the forms runaway check is set on.

Byte 0, Bit 3 — End of Forms

End of forms is set when the end-of-forms switch senses the absence of forms if the platen pressure rolls are not engaged.

Byte 1, Bit 0 — Printer Not Ready

See horizontal check.

Byte 1, Bit 1 — Wire Check

A wire check indicates that a print wire magnet was energized too long (more than 1.6 ms). This check forces a microcode delay of 250 ms, unless the system has BSC or SDLC. If the condition causing the wire check goes away, the 'wire check' latch stays on until a check reset command is sent to the attachment. The ready comes on as soon as the condition that caused the wire check goes away.

Byte 1, Bit 4 — Memory Data Check

See horizontal check.

Byte 1, Bit 5 — Emitter Too Fast Check

See horizontal check.

Byte 1, Bit 6 — Unprintable Character Check

See horizontal check.

Any bit that is turned on in byte 1 forces a horizontal check (byte 0, bit 1). The microprogram can issue an IOS command with a modifier of hex 0 and determine that a horizontal check has occurred; then an IOS command with a hex 1 modifier can further define the cause of the horizontal check.

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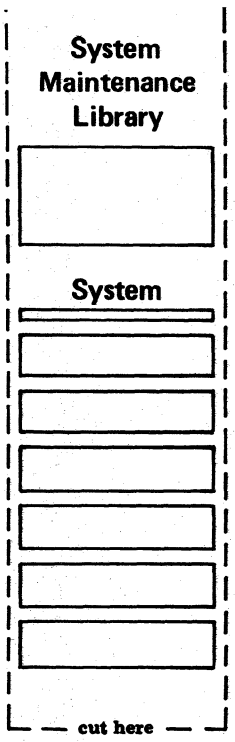

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