FE13 FE1 - CPU MODULE FOR SYSTEM TEST

```
ERR LOC OBJECT CODE      ADDR STMT SOURCE STATEMENT

                              2         DECK  1
   CCC0                       3 FE1     START 0
   CA00                       4         ORG   X'0A00'
                              5
                              6 ********************************************************************************
                              7 *             SYSTEM/3 CPU MODULE FOR SYSTEM  TEST                             *
                              8 ********************************************************************************
                              9 *             SECTION PREFACE                                                  *
                             10 *                                                                              *
   0A00 FE13             0A01 11         DC    XL2'FE13'             PROGRAM ID                               *
   0A02 80               0A02 12         DC    XL1'80'               SECTION FLAGS                            *
   0A03 01               0A03 13         DC    XL1'01'               ROUTINE NO.                              *
   0A04 CCCC             0A05 14         DC    XL2'00'               RESERVED                                 *
   0A06 0A0A             0A07 15         DC    AL2(TST01)            ADDRESS OF FIRST ROUTINE PREFIX          *
   0A08 FFFF             0A09 16         DC    XL2'FFFF'             FILLER                                   *
                             17 *                                                                              *
                             18 ********************************************************************************
                             19 *             ROUTINE PREFACE                                                  *
                             20 *                                                                              *
   0A0A 01               0A0A 21 TST01   DC    XL1'01'               ROUTINE NUMBER                           *
   0A0B 00               0A0B 22         DC    XL1'00'               ROUTINE FLAGS                            *
   0A0C FFFF             0A0D 23         DC    XL2'FFFF'                                                      *
                             24 *                                                                              *
                             25 ********************************************************************************
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FE13 FE1 - CPU MODULE FOR SYSTEM TEST

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ERR LOC OBJECT CODE      ADDR STMT SOURCE STATEMENT

   0A0E C0 87 C212           27 TST01A E     TEST                .TEST FOR VALID DCP ENTRY IN DATA SW
   0A12 38 80 C204           28        TBN   CPU,X'80'            TEST FOR DUAL PROGRAM FEATURE
   0A16 F2 90 4B             29        JF    TST013              BYPASS IF NOT PRESENT
   0A19 35 8C CD81           30        L     ERRINT,IAR0         LOAD INTERRUPT IAR FOR ERROR
   0A1D 3C 80 CA57           31        MVI   BRANCH+1,X'80'      SET BRANCH INST. TO NOP
   0A21 F3 CC C0             32        SIO   0,0                 DISABLE DUAL PGM.
   0A24 35 2C CDAD           33        L     ADBY,P1IAR          LOAD PROGRAM LEVEL 1 IAR
   0A28 35 4C CDAF           34        L     ADBZ,P2IAR          LOAD PROGRAM LEVEL 2 IAR
   0A2C 35 40 0DAB           35 DPY    L     ADRX,P2IAR          LOAD PROGRAM LEVEL 2 IAR
   0A30 F1 0C C0             36 DPZ    APL   0                   ADVANCE PROGRAM LEVEL
   0A33 F2 87 C6             37        J     DP2                 TO NEXT TEST
                             38
   0A36 C0 87 C222           39 DPX    E     HALT                GO HALT -0C32- BECAUSE APL INSTR
   0A3A FE32           0A3B  40        DC    XL2'FE32'            CAUSED PROGRAM ADVANCE WHEN NOT
                             41 *                                   ENABLED.
                             42
   0A3C F3 0C C6             43 DP2    SIC   X'06',X'0'          ENABLE DUAL PGM.
   0A3F 35 80 CD7F           44        L     INTRPT,IAR0         LOAD INTERRUPT LEVEL 0 IAR
   0A43 35 2C CDB1           45        L     ADBA,P1IAR          LOAD PROGRAM LEVEL 1 IAR
   0A47 35 2C CDB3           46        L     ADBB,P1IAR          LOAD PROGRAM LEVEL 1 IAR
   0A4B 35 4C CDE5           47        L     ADBC,P2IAR          LOAD PROGRAM LEVEL 2 IAR
   0A4F 35 4C CDE3           48 DPA    L     ADBE,P2IAR          LOAD PROGRAM LEVEL 2 IAR
   0A53 F1 CC C0             49 DPC    APL   0                   ADVANCE PROGRAM LEVEL
   0A56 C0 87 CA53           50 BRANCH E     DPC
                             51
   0A5A C0 87 0222           52        E     HALT                GO TO HALT -0C31- BECAUSE APL DID
   0A5E FE31           0A5F  53        DC    XL2'FE31'            NOT CAUSE AN ADVANCE WHEN DUAL
                             54 *                                   PROGRAM WAS ENABLED.
                             55
   0A60 3C 87 0A57           56 DPB    MVI   BRANCH+1,X'87'      SET BRANCH TO UNCONDITIONAL
                             57
                       CA64  58 TST01B EQU   *
                             59
   0A64 35 03 C2C3           60 A      L     CORSIZ,3            LOAD CORE SIZE IN XR1& XR2
   0A68 3D FF C203           61        CLI   CORSIZ,X'FF'            .CHECK IF CPU HAS 64K OF CORE.
   0A6C F2 01 C4             62        JNE   B                      IF NOT, CONTINUE NORMALLY. IF
   0A6F 35 03 CD94           63        L     ZERO,3                 YES  ENTER X'0000' IN XR1 & XR2
   CA73 36 03 CDA7           64 B      A     NEG128,3              .SUBTRACT 128 BY ADDING X'FF80'
   0A77 F2 81 CC             65        JZ    TEST2                 .IF ALL CORE TESTED, END TEST.
   0A7A 9D 7F 7F 7F          66        CLC   127(128,XR2),127(,XR1)   IF NOT, CHECK PARITY OF 128
   CA7E CC 87 CD35           67        E     EXIT                   BYTES AND CHECK WITH SUPERVISOR
   0A82 C0 87 CA73           68        B     B                      BEFORE CHECKING NEXT 128 BYTES.
                       0A86  69 TEST2  EQU   *
   0A86 3C 00 CDB6           70        MVI   TSTFLD,0                    SET TEST FIELD TO ZERO
   CA8A 38 FF CDE6           71        TBN   TSTFLD,X'FF'                TEST ALL BITS FOR ON
   0A8E F2 90 C6             72        JF    *+9                         BYPASS HALT IF ALL OFF
   0A91 CC 87 C222           73        E     HALT                        TO HALT IF ANY TEST ON
   CA95 FEC1           0A96  74        DC    XL2'FE01'           HALT ID
                             75
   CA97 39 FF CDB6           76        TBF   TSTFLD,X'FF'                TEST ALL BITS FOR OFF
   0A9B F2 10 C6             77        JT    *+9                 BYPASS HALT IF ALL OFF
   CA9E C0 87 0222           78        E     HALT                TO HALT IF ANY  ON
   0AA2 FEC2           0AA3  79        DC    XL2'FE02'           HALT ID
                             80
   0AA4 3C FF CDE6           81        MVI   TSTFLD,X'FF'        SET TEST FIELD TO 'FF'
   CAA8 39 FF CDB6           82        TBF   TSTFLD,X'FF'        TEST ALL BITS FOR OFF
   CAAC C0 90 CAB6           83        BF    *+10                BYPASS HALT IF ALL ON
   0AB0 C0 87 C222           84        E     HALT                TO HALT IF ANY TEST OFF
   0AB4 FE03           0AB5  85        DC    XL2'FE03'           HALT ID
                             86
   0AB6 38 FF CDB6           87        TBN   TSTFLD,X'FF'        TEST ALL BITS FOR ON
   0ABA F2 10 C6             88        JT    *+9                 BYPASS HALT IF ALL ON
   0ABD C0 87 0222           89        E     HALT                TO HALT IF ANY TEST OFF
   0AC1 FEC4           0AC2  90        DC    XL2'FE04'           HALT ID
                             91
   0AC3 3C 00 CDB6           92        MVI   TSTFLD,0            SET TEST FIELD TO ZERO
   0AC7 3A FF CDB6           93        SBN   TSTFLD,X'FF'        SET ALL BITS ON
   0ACB 38 FF CDB6           94        TBN   TSTFLD,X'FF'        TEST ALL BITS FOR ON
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FE13 FE1 - CPU MODULE FOR SYSTEM TEST

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ERR LOC OBJECT CODE      ADDR STMT SOURCE STATEMENT

   CACF C0 10 0AD9             95         BT    *+10                BYPASS HALT IF ALL ON
   0AD3 CC 87 C222             96         B     HALT                TO HALT IF ANY TEST OFF
   0AD7 FEC5           0AD8    97         DC    XL2'FE05'           HALT ID
                               98
   0AD9 3C FF CDE6             99         MVI   TSTFLD,X'FF'        SET TEST FIELD TO ALL BITS
   CADD 3B FF CDE6            100         SBF   TSTFLD,X'FF'        SET ALL BITS OFF
   0AE1 39 FF CDB6            101         TBF   TSTFLD,X'FF'        TEST ALL BITS FOR OFF
   CAE5 C0 1C CAEF            102         BT    *+10                BYPASS HALT IF ALL OFF
   0AE9 C0 87 C222            103         B     HALT                TO HALT IF ANY TEST ON
   0AED FEC6           0AEE   104         DC    XL2'FE06'           HALT ID
                              105
   CAEF 3C C0 CDE6            106         MVI   TSTFLD,0            SET TEST FIELD TO ZERO
   0AF3 3A CC CDB6            107         SBN   TSTFLD,0            SET NO BITS ON
   0AF7 3D 00 CDE6            108         CLI   TSTFLD,0            TEST FOR NO CHANGE
   0AFB F2 81 C6              109         JE    *+9                 JUMP OVER HALT IF OK
   CAFE C0 87 0222            110         B     HALT                TO HALT IF ANY TEST ON
   CB02 FEC7           0B03   111         DC    XL2'FE07'           HALT ID
   0B04 3C FF CDE6            112         MVI   TSTFLD,X'FF'        SET ON ALL BITS IN TEST FIELD
   CB08 3B 00 CDE6            113         SBF   TSTFLD,0            SET NO BITS OFF
   0B0C 3D FF CDB6            114         CLI   TSTFLD,X'FF'        TEST FOR NO CHANGE
   0B10 F2 81 C6              115         JE    *+9                 JUMP OVER HALT IF OK
   0B13 CC 87 C222            116         B     HALT                TO HALT IF ANY TEST OFF
   0B17 FEC8           0B18   117         DC    XL2'FE08'           HALT ID
   0B19 C0 87 CD35            118         B     EXIT                TO SUPERVISOR
                              119
   0B1D 04 20 CDEF 0D91       120         ZAZ   WORK+9(3),UNITS(1)  ZERO THE WORK AREA
   CB23 C6 20 CDEF CD92       121         AZ    WORK+9(3),DEONE(1)  ADD DECIMAL ONE
   0B29 C7 20 CDEF 0D92       122         SZ    WORK+9(3),DEONE(1)  SUBTRACT DECIMAL ONE
   0B2F 3C F6 CDB6            123         MVI   WORK,X'F6'          SET WORK AREA TO F6
   0B33 04 C0 CIE6 0D8A       124         ZAZ   WORK(1),UNITS-7(1)  ZERO & ADD DEC. 3
   0B39 3D F3 CDE6            125         CLI   WORK,X'F3'          CHECK FOR DEC 3,
   0B3D C0 81 CB47            126         BE    *+10                BYPASS HALT IF OK
   0B41 CC 87 CD22            127         B     HALT                TO HALT IF NOT EQUAL TO F3
   0B45 FEC9           0B46   128         DC    XL2'FE09'           HALT ID
                              129
   0B47 3C D0 CDBE            130         MVI   WORK+8,X'D0'
   0B4B 0C C7 CIBD CDBE       131         MVC   WORK+7(8),WORK+8
   0B51 C6 C8 CIBE CD90       132         AZ    WORK+8(9),UNITS-1(9)
   0B57 0D C8 CIBE 0D90       133         CLC   WORK+8(9),UNITS-1
   0B5D F2 81 C6              134         JE    *+9
   CB60 C0 87 C222            135         B     HALT
   0B64 FECA           0B65   136         DC    XL2'FECA'           HALT ID
                              137
   CB66 35 01 CD96            138         L     XFF,XR1             SET XR1 TO FF
   0B6A 35 02 CD94            139         L     ZERO,XR2            SET XR2 TO 00
   0B6E 34 01 CDE7            140         ST    WORK+1,XR1          STORE BOTH
   CB72 34 02 CDB9            141         ST    WORK+3,XR2          IN WORK AREA
   CB76 CD 01 CIB7 0D96       142         CLC   WORK+1(2),XFF       CHECK VALUE FROM XR1
   CB7C F2 81 C6              143         JE    *+9                 JUMP OVER HALT IF OK
   CB7F C0 87 0222            144         B     HALT                TO HALT IF NOT OK
   CB83 FE0E           0B84   145         DC    XL2'FE0E'           HALT ID
   CB85 0D 01 CDB9 0D94       146         CLC   WORK+3(2),ZERO      CHECK VALUE FROM XR2
   CB8B F2 81 C6              147         JE    *+9                 JUMP OVER HALT IF OK
   CB8E C0 87 C222            148         B     HALT                TO HALT IF NOT OK
   CB92 FE0C           0B93   149         DC    XL2'FE0C'           HALT ID
                              150
   CB94 35 01 CDA1            151         L     WORK5,XR1           LOAD ADDRESS OF WORK+5 IN XR1
   CB98 7C FD C0              152 MVI1    MVI   0(,XR1),X'FD'       MOVE IMEADATE WITH INDEXING
                              153
   CB9B 3D FD CDEB            154         CLI   WORK+5,X'FD'        CHECK RESULT
   CB9F F2 81 C6              155         JE    *+9                 JUMP OVER HALT IF OK
   CBA2 C0 87 0222            156         B     HALT                TO HALT IF NOT OK
   CBA6 FE0D           0BA7   157         DC    XL2'FE0D'           HALT ID
                              158
   CBA8 35 02 CDA1            159         L     WORK5,XR2           LOAD ADDRESS OF WORK+5 IN XR2
   CBAC BC AA C0              160 MVI2    MVI   0(,XR2),X'AA'       MOVE IMEADATE WITH INDEXING
                              161
   CBAF 3D AA CDBB            162         CLI   WORK+5,X'AA'        CHECK RESULT
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FE13 FE1 - CPU MODULE FOR SYSTEM TEST

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ERR LOC OBJECT CODE      ADDR STMT SOURCE STATEMENT

   0BB3 F2 81 C6              163        JE     *+9                 JUMP OVER HALT IF OK
   0BB6 C0 87 0222            164        E      HALT                TO HALT IF NOT OK
   0BBA FE0E            0BBB  165        DC     XL2'FE0E'           HALT ID
                              166
   0BBC C2 01 C000            167        LA     0,XB1               LOAD ZERO IN XB1
   0BC0 34 01 0DB7            168        ST     WORK+1,XB1          STORE
   0BC4 0D 01 0DB7 0D94       169        CLC    WORK+1(2),ZERO      COMPARE
   0BCA F2 81 C6              170        JE     *+9                 JUMP OVER HALT IF OK
   0BCD C0 87 0222            171        E      HALT                TO HALT IF NOT OK
   0BD1 FECF            0BD2  172        DC     XL2'FECF'           HALT ID
                              173
   0BD3 C2 01 C000            174        LA     0,XB1               ZERO XB1
   0BD7 D2 01 C2              175 LOAD1  LA     2(,XB1),XB1         STEP BY 2
   0BDA 34 01 0DA9            176        ST     REGSAV,XB1          SAVE
   0BDE 0D 01 0DA9 0DA5       177        CLC    REGSAV(2),MINUS2    COMPARE
   0BE4 C0 01 CED7            178        BNE    LOAD1               LOOP TILL EQUAL TO 00FE
                              179
   0BE8 C2 02 C000            180        LA     0,XB2               ZERO XB2
   0BEC E2 02 02              181 LOAD2  LA     2(,XB2),XB2         STEP BY 2
   0BEF 34 02 0DA9            182        ST     REGSAV,XB2          SAVE
   0BF3 0D 01 0DA9 0DA5       183        CLC    REGSAV(2),MINUS2    COMPARE
   0BF9 C0 01 CEEC            184        BNE    LOAD2               LOOP TILL EQUAL TO 00FE
   0BFD C0 87 0D35            185        E      EXIT
                              186
                              187
   0C01 3C 0F 0DE6            188        MVI    WORK,X'0F'          SET WORK AREA
   0C05 3C F0 0DB7            189        MVI    WORK+1,X'F0'
   0C09 C8 00 0DE6 0DB7       190        MZZ    WORK,WORK+1         MOVE ZONE TO ZONE
   0C0F 3D FF 0DE6            191        CLI    WORK,X'FF'          CHECK MOVE
   0C13 F2 81 C6              192        JE     *+9                 JUMP OVER HALT IF OK
   0C16 C0 87 0222            193        E      HALT                TO HALT IF ERROR
   0C1A FE1C            0C1B  194        DC     XL2'FE1C'           HALT
                              195
   0C1C C8 01 0DE6 0DB7       196        MZN    WORK,WORK+1         MOVE NUMERIC TO ZONE
   0C22 3D 0F 0DE6            197        CLI    WORK,X'0F'          CHECK MOVE
   0C26 F2 81 C6              198        JE     *+9                 JUMP OVER HALT IF OK
   0C29 C0 87 0222            199        E      HALT                TO HALT IF ERROR
   0C2D FE11            0C2E  200        DC     XL2'FE11'           HALT ID
                              201
   0C2F C8 03 0DE6 0DB7       202        MNN    WORK,WORK+1         MOVE NUMERIC TO NUMERIC
   0C35 3D 00 0DE6            203        CLI    WORK,X'00'          CHECK MOVE
   0C39 F2 81 C6              204        JE     *+9                 JUMP OVER HALT IF OK
   0C3C C0 87 0222            205        E      HALT                TO HALT IF ERROR
   0C40 FE12            0C41  206        DC     XL2'FE12'           HALT ID
                              207
   0C42 C8 02 0DE6 0DB7       208        MNZ    WORK,WORK+1         MOVE ZONE TO NUMERIC
   0C48 3D 0F 0DE6            209        CLI    WORK,X'0F'          CHECK MOVE
   0C4C F2 81 C6              210        JE     *+9                 JUMP OVER HALT IF OK
   0C4F C0 87 0222            211        E      HALT                TO HALT IF ERROR
   0C53 FE13            0C54  212        DC     XL2'FE13'           HALT ID
   0C55 0C 01 0DA9 0D96       213        MVC    REGSAV(2),XFF       SET SAVE AREA
   0C5B C2 01 0DE6            214        LA     WORK,XB1            LOAD ADDRESS OF WORK IN XB1
   0C5F D2 02 C0              215        LA     0(,XB1),XB2         PUT XB1 IN XB2
   0C62 34 02 0DA9            216        ST     REGSAV,XB2          SAVE XB2
   0C66 0D 01 0DA9 0D9F       217        CLC    REGSAV(2),WORK0     CHECK RESULT
   0C6C F2 81 C6              218        JE     *+9                 JUMP OVER HALT IF OK
   0C6F C0 87 0222            219        E      HALT                TO HALT IF ERROR
   0C73 FE14            0C74  220        DC     XL2'FE14'           HALT ID
                              221
   0C75 0C 01 0DA9 0D96       222        MVC    REGSAV(2),XFF       SET SAVE AREA
   0C7B C2 02 0DE6            223        LA     WORK,XB2            LOAD ADDRESS OF WORK IN XB2
   0C7F E2 01 C0              224        LA     0(,XB2),XB1         PUT XB2 IN XB1
   0C82 34 01 0DA9            225        ST     REGSAV,XB1          SAVE XB1
   0C86 0D 01 0DA9 0D9F       226        CLC    REGSAV(2),WORK0     CHECK RESULT
   0C8C F2 81 C6              227        JE     *+9                 JUMP OVER HALT IF OK
   0C8F C0 87 0222            228        E      HALT                TO HALT IF ERROR
   0C93 FE15            0C94  229        DC     XL2'FE15'           HALT ID
                              230
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FE13 FE1 - CPU MODULE FOR SYSTEM TEST

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ERR LOC OBJECT CODE      ADDR  STMT SOURCE STATEMENT

   0C95 F2 88 CC              231        JCZ   *+3                 RESET DECIMAL OVERFLOW
   0C98 3C D9 0DB6            232        MVI   WORK,X'D9'          SET WORK TO MINUS DECIMAL 9
   0C9C 06 00 0DB6 0D97       233        AZ    WORK(1),XD9(1)      ADD MINUS DEC. 9 TO WORK
   0CA2 F2 88 C6              234        JCZ   *+9                 JUMP OVER HALT IF DECIMAL OVER FLOW
   0CA5 C0 87 0222            235        B     HALT                TO HALT IF ERROR
   0CA9 FE16            0CAA  236        DC    XL2'FE16'           HALT ID
                              237
   0CAB 3C D9 0DB6            238        MVI   WORK,X'D9'          SET WORK TO MINUS DECIMAL 9
   0CAF C6 C0 0DB6 0D97       239        AZ    WORK(1),XD9(1)      ADD MINUS DEC. 9 TO WORK
   0CB5 C0 88 0CBF            240        BCZ   *+10                BRANCH OVER HALT IF DECIMAL OVERFLOW
   0CB9 C0 87 C222            241        B     HALT                TO HALT IF ERROR
   0CBD FE17            0CBE  242        DC    XL2'FE17'           HALT ID
                              243
   0CBF C0 C8 0CC9            244        BNOZ  *+10                BRANCH OVER HALT IF NO OVERFLOW
   0CC3 C0 87 C222            245        B     HALT                TO HALT IF ERROR
   0CC7 FE18            0CC8  246        DC    XL2'FE18'           HALT ID
                              247
   0CC9 F2 08 C6              248        JNCZ  *+9                 JUMP OVER HALT  IF NO OVERFLOW
   0CCC C0 87 C222            249        B     HALT                TO HALT IF ERROR
   0CD0 FE19            0CD1  250        DC    XL2'FE19'           HALT ID
                              251
   0CD2 0C 01 0DE7 0D9D       252        MVC   WORK+1(2),X2020     SET WORK TO HEX-2020-
   0CD8 0A 01 0DB7 0D99       253        ED    WORK+1(2),XE1F0     EDIT
   0CDE 0D 01 0DB7 0D9B       254        CLC   WORK+1(2),XF1F0     CHECK RESULT
   0CE4 F2 81 C6              255        JE    *+9                 JUMP OVER HALT IF OK
   0CE7 C0 87 C222            256        B     HALT                TO HALT IF ERROR
   0CEB FE1A            0CEC  257        DC    XL2'FE1A'           HAL. ID
                              258
   0CED 3C F0 0DD6            259        MVI   WORK+32,C'0'        SET A NUMERIC VALUE AT END OF FLD
   0CF1 3C C0 0DD5            260        MVI   WORK+31,0
   0CF5 0C 1E 0DD4 0DD5       261        MVC   WORK+30(31),WORK+31 ZERO WORK
   0CFB 3C FF 0DFF            262        MVI   WORK+73,X'FF'
   0CFF 0C 1D 0DFE 0DFF       263        MVC   WORK+72(30),WORK+73 COMPARE FIELD
   0D05 0B 1E 0DB6 0D96       264        ITC   WORK(31),XFF        INSERT FF
   0D0B 34 C8 0DD8            265        ST    WORK+34,ARR         SAVE ARR
   0D0F 0D 1E 0DD4 0DFF       266        CLC   WORK+30(31),WORK+73 CHECK
   0D15 F2 81 C6              267        JE    *+9                 JUMP OVER HALT IF OK
   0D18 C0 87 C222            268        B     HALT                TO HALT IF ERROR
   0D1C FE1C            0D1D  269        DC    XL2'FE1C'           HALT ID
   0D1E 0D 01 0DD8 0DA3       270        CLC   WORK+34(2),WORK31   CHECK ARR VALUE AFTER THE ITC
   0D24 F2 81 C6              271        JE    *+9                 JUMP OVER HALT IF SET CORRECTLY
   0D27 C0 87 C222            272        B     HALT                TO HALT IF NOT
   0D2B FE1E            0D2C  273        DC    XL2'FE1E'           HALT ID
                              274
   0D2D C0 87 0D35            275        B     EXIT                TO SUPERVISOR
   0D31 CC 87 CA0E            276        B     TST01A
   0D35 34 C8 0D44      EXIT  277        ST    BR+3,ARR            SAVE EXIT ADDRESS
   0D39 3D FE CA00            278        CLI   X'CA00',X'FE'
   0D3D C0 01 0A0A              9        BNE   ENTRY
   0D41 C0 87 C0C0              0 BR     B     *-*
                                1
   0D45 34 20 0D85            282 INTOK  ST    P1SAV,X'20'         SAVE P1-IAR
   0D49 34 40 0D87            283        ST    P2SAV,X'40'         SAVE P2-IAR
                              284
   0D4D 35 60 0D83            285        L     PADINT,X'60'        LOAD P1 & P2 IARS TO ADDR OF SETARR
                              286
   0D51 F1 00 C0              287        APL   0                   TRY TO ADVANCE PROG LEVEL IN INT LEV
                              288
   0D54 C0 80 0D6D            289 NOOCP  BC    INTERR,X'80'        NO-OP BRANCH TO TEST IAR/ARR SELECT
                              290
   0D58 C0 87 0D5F            291 UNCND  B     NEWLD               UNCONDITIONAL BRANCH TO TEST
   0D5C F2 87 CE              292        J     INTERP               IAR/ARR SELECT
                              293
   0D5F F3 00 C6              294 NEWLD  SIO   6,0                 ENABLE  INTERRUPTS & DUAL PROG MODE
                              295
   0D62 35 20 0D85            296        L     P1SAV,X'20'         RESTORE P1-IAR
   0D66 35 40 0D87            297        L     P2SAV,X'40'         RESTORE P2-IAR
                              298
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FE13 FE1 - CPU MODULE FOR SYSTEM TEST

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ERR LOC OBJECT CODE      ADDR STMT SOURCE STATEMENT

    0D6A F2 87 C4              299         J      RESETT              GO RESET THE INTERRUPT.
    0D6D 35 60 CD83            300 INTERR  L      BADINT,X'60'        LOAD P1-IAR & P2-IAR WITH THE
                               301 *                                   ADDRESS OF SETABR INSTRUCTION.
                               302
    0D71 F3 00 C               303 RESETT  SIC    5,0                 RESET & DISABLE INTERRUPTS
                               304
    0D74 C0 87 C222            305 SETABR  B      HALT                GO TO HALT -FE89- IF INT LEV 0 ERR
    0D78 FE89            CD79  306         DC     XL2'FE89'
                               307
    0D7A CC 87 CD6D            308         B      INTERR              RESETT FAILED, TRY AGAIN
    0D7E 0D45            0D7F  309 INTFPT  DC     AL2(INTCK)
    0D80 0D6D            0D81  310 ERRINT  DC     AL2(INTERR)
    0D82 0D74            0D83  311 BADINT  DC     AL2(SETABR)
    0D84                 0D85  312 P1SAV   DS     CL2
    0D86                 0D87  313 P2SAV   DS     CL2
    0D88 F1F2F3F4F5F6F7F8 CD91 314 UNITS   DC     CL10'1234567890'
    0D90 F9F0                  314
    0D92 F1              0D92  315 ONE     DC     CL1'1'
    0D93 0000            0D94  316 ZERO    DC     XL2'0'
    0D95 FFFF            0D96  317 XFF     DC     XL2'FFFF'
    0D97 D9              0D97  318 XD9     DC     XL1'D9'
    0D98 E1F0            0D99  319 XE1FC   DC     XL2'E1F0'
    0D9A F1F0            0D9B  320 XF1F0   DC     XL2'F1F0'
    0D9C 2020            0D9D  321 X202C   DC     XL2'2020'
    0D9E 0DE6            0D9F  322 WORK0   DC     AL2(WORK)
    0DA0 0DEE            0DA1  323 WORK5   DC     AL2(WORK+5)
    0DA2 0DD5            0DA3  324 WORK31  DC     AL2(WORK+31)
    0DA4 00FE            0DA5  325 MINUS2  DC     XL2'00FE'
    0DA6 FF80            0DA7  326 NEG128  DC     XL2'FF80'
    0DA8 0000            0DA9  327 REGSAV  DC     XL2'0'
    0DAA 0A36            0DAB  328 ADRX    DC     AL2(DPX)
    0DAC 0A2C            0DAD  329 ADRY    DC     AL2(DPY)
    0DAE 0A30            0DAF  330 ADRZ    DC     AL2(DPZ)
    0DB0 0A4F            0DB1  331 ADRA    DC     AL2(DPA)
    0DB2 0A6C            0DB3  332 ADRB    DC     AL2(DPB)
    0DB4 0A53            0DB5  333 ADRC    DC     AL2(DPC)
                         0DB6  334 WORK    EQU    *
    0DB6                 0DFF  335         DS     CL74
                         0001  336 XR1     EQU    01
                         0002  337 XR2     EQU    02
                         0008  338 ABR     EQU    08
                         0080  339 IAR0    EQU    X'80'
                         0020  340 P1IAR   EQU    X'20'               PROGRAM LEVEL 1 IAR
                         0040  341 P2IAR   EQU    X'40'               PROGRAM LEVEL 2 IAR
                         0203  342 CORSIZ  EQU    X'203'
                         0204  343 CPU     EQU    X'204'
                         0A0A  344 ENTRY   EQU    X'A0A'
                         0222  345 HALT    EQU    X'222'
                         0212  346 TEST    EQU    X'212'
                         0DB6  347 TSTFLD  EQU    WORK
                         0A0E  348         END    TSTG1A
```

FE13 FE1 - CPU MODULE FOR SYSTEM TEST

CROSS-REFERENCE

SYMBOL	T	LEN	VALUE	DEFN	REFERENCES
A	A	0C4	CA64	0060	
ADRA	A	0C2	CDE1	0331	0045
ADRE	A	0C2	CDE3	0332	0046 0048
ADRC	A	0C2	CDE5	0333	0047
ADRX	A	0C2	CDAB	0328	0035
ADRY	A	0C2	CDAD	0329	0033
ADRZ	A	0C2	CDAF	0330	0034
ARR	C	0C1	C0C8	0338	0265 0277
E	A	0C4	CA73	0064	0062 0068
BADINT	A	0C2	CD83	0311	0285 0300
BR	A	0C4	CD41	0280	0277*
BRANCH	A	0C4	CA56	0050	0031* 0056*
CORSIZ	C	0C1	0203	0342	0060 0061
CPU	C	0C1	02C4	0343	0028
DEGSE	A	0C1	CD92	0315	0121 0122
DPA	A	0C4	CA4F	0048	0331
DPB	A	0C4	CA6C	0056	0332
DPC	A	0C3	CA53	0049	0050 0333
DPX	A	0C4	CA36	0039	0328
DPY	A	0C4	CA2C	0035	0329
DPZ	A	0C3	CA30	0036	0330
DP2	A	0C3	CA3C	0043	0037
ENTRY	C	0C1	CA0A	0344	0279
ERRINT	A	0C2	CD81	0310	0030
EXIT	A	0C4	CD35	0277	0067 0118 0185 0275
FE1	A	0C1	C00C	0003	
HALT	C	001	0222	0345	0039 0052 0073 0078 0084 0089 0096 0103 0110 0116 0127 0135 0144 0148 0156 0164 0171 0193 0199 0205 0211 0219 0228 0235 0241 0245 0249 0256 0268 0272 0305
IAR0	C	0C1	0C80	0339	0030* 0044*
INTERR	A	0C4	CD6D	0300	0289 0292 0308 0310
INTCK	A	0C4	CD45	0282	0309
INTRPT	A	0C2	CD7F	0309	0044
LOAD1	A	0C3	CED7	0175	0178
LOAD2	A	0C3	CEEC	0181	0184
MINUS2	A	0C2	CDA5	0325	0177 0183
MVI1	A	0C3	CE98	0152	
MVI2	A	0C3	CEAC	0160	
NEG128	A	0C2	CDA7	0326	0064
NEWLD	A	003	CD5F	0294	0291
NOOOP	A	0C4	CD54	0289	
P1IAR	C	001	C020	0340	0033* 0045* 0046*
P1SAV	A	0C2	CD85	0312	0282* 0296
P2IAR	C	001	C040	0341	0034* 0035* 0047* 0048*
P2SAV	A	0C2	CD87	0313	0283* 0297
REGSAV	A	0C2	CDA9	0327	0170* 0177 0182* 0183 0213* 0216* 0217 0222* 0225* 0226
RESFTT	A	0C3	CD71	0303	0299
SETJBP	A	0C4	CD74	0305	0311
TEST	C	0C1	C212	0346	0027
TEST2	A	001	CA86	0069	0065
TSTFLD	A	001	0286	0347	0070* 0071 0076 0081* 0082 0087 0092* 0093* 0094 0099* 0100* 0101 0106* 0107* 0108 0112* 0113* 0114
TST01	A	0C1	CA0A	0021	0015
TST01A	A	004	0ACE	0027	0276 0348
TST01B	A	0C1	0A64	0058	0029
UNCND	A	0C4	CD58	0291	
UNITS	A	010	CD91	0314	0120 0124 0132 0133
WORK	A	0C1	0DE6	0334	0120* 0121* 0122* 0123* 0124* 0125 0130* 0131 0131* 0132* 0133 0140* 0141* 0142 0146 0154 0162 0168* 0169 0188* 0189* 0190 0190* 0191 0196 0196* 0197 0202 0202* 0203 0208 0208* 0209 0214 0223 0232* 0233* 0238* 0239* 0252* 0253* 0254 0259* 0260* 0261 0261* 0262* 0263 0263* 0264* 0265* 0266 0266 0270 0322 0323 0324 0347
WORK0	A	0C2	CD9F	0322	0217 0226
WORK31	A	0C2	CDAD	0324	0270
WORK5	A	0C2	CDA1	0323	0151 0159
XD9	A	0C1	CD97	0318	0233 0239

PE13 FE1 - CPU MODULE FCB SYSTEM TEST

CROSS-REFERENCE

SYMBOL	T	LEN	VALUE	DEFN	REFERENCES
XE1FO	A	0C2	CD99	0319	0253
XFF	A	0C2	CD96	0317	0138 C142 0213 0222 0264
XF1FO	A	0C2	CD9E	0320	0254
XR1	C	0C1	0001	0336	0066 0138* 0140 C151* 0152 C167* 0168 0174* 0175 C175* 0176 C214* 0215 C224* 0225
XR2	C	0C1	0002	0337	0066 0139* 0141 C159* 0160 0180* 0181 0181* 0182 0215* 0216 0223* 0224
X2020	A	0C2	CD9D	0321	0252
ZERO	A	0C2	CD94	0316	0063 0139 0146 C169

TOTAL STATEMENTS FLAGGED IN THIS ASSEMBLY = 0

FE13 FE1 - CPU MODULE FOR SYSTEM TEST

OBJECT CARD LISTING

THE CHARACTER ' INDICATES A BLANK COLUMN AND THE CHARACTERS D̄ Ē H̄ INDICATE NUMERIC SHIFT.

CL 1 THROUGH 16	CL 17 THROUGH 32	CL 33 THROUGH 48	CL 49 THROUGH 64	CL 65 THROUGH 80	CL 81 THROUGH 96
T('Y4"/+''&''E-,	""0D'"""'/0HK+H'	EA|H̄&K3C'CQD@-'Z	P@0''(K'(,LM'CĒ@	5&'6,@&''@Y*'.2%	XHA0G9QHFE130001
T<O7YA%BG'S.=<?<	'ATC'CP@5H'61(K'	(%3N'C$M5&'63@&'	'OH*H̄M@BG'S.=<L2	GPV*5'CHC|&'>IA4	HEJD(@JOFE130002
T<CD̄*"OHC@-DD(&<	(VCQCCĒ¬2-&2)¬7'	"CH*((*EG=X<@''6	6+|?(_?Ē&A%BG'S.	='LX"C'$2D''1IE'	*F'4IJ$'FE130003
T<O,&A%BG'S.='I3	"C$Q9"066CI'H̄_%B	G'S.='3I"C$$2D'$	'/0HS"-&@''66+?@	(_TT"C$'D''1.KU	*D-8H̄8Y@FE130004
T<-%CB_X'/0ES"-M	@"066+"@(_TX"C$$	'D',?0H*BH?8F|''	(_IY'C$Q'''66@YD	FOH*BH?8G'EUVHJ*	LC0%A3LHFE130005
T.0%3||@(_I%'C$Q	'"066@YDFOH*BH?8	HOH*((&&-C$@(U$Q	-C$@(U-*-C$@(UT3	6C$QD'E8D̄ĒB&SG/0	QB0*C)A8FE130006
T.O_T''66CQY'@C6	6OHD.J@BG'S.=BL3	&C$8<AC6'C$8FE'6	=CB'(E'6=CRC2-&$	'/0HS'B-WHS'*F/Q	<B'&B:/@FE130007
T<&>N"-Y&'&6O(&H	(VC&AC$*4'-69C&D	(_C6O@YDFOH*BH?8	.C&D(>&6B@YDFOH*	BH?8<(&D''EQUE1M	JC&UEL&'FE130008
T<Q?ICĒB@"E'''86	*@YDFOH*BH?8((&H	(Y$2D̄'C6D̄C$?2-&$	'/0HS"-'@B'&''('D	(_C4AC$*(V''3<K4	*E&-A4ĒOFE130009
T<-?@@YDFOE*EH?8	|O-D''(HA'T&ACĒU	('&6ZCĒP''&?P0-H	''+HE'T&BCĒU('&6	ZCĒP''&?%'CH>.B-	)FJ*IJ&&FE130010
T<&O>OH*((IO|C$Q	@@'67B''(_-6/|¬@	(_?H̄AA%BG'S.=D'-	AC$Q(_34|C$$2-&$	'/CHS"/D'H̄E&SEJD	|B0*CP10FE130011
T<&1-B'<(_-67|&	(_?Ē@A%EG'S.=D--	BC$Q(_34|C$$2-&$	'/CHS"/<<'&6ZCB$	B'&664-H'.2%ZGA-	OE&HC3ZDFE130012
T<&2K'C&BCĒU(S6	Z(R"2-&$'/0HS"/&	<'&6ZCB$B'-668-D	'(D(D̄&4ACĒU(X"H̄	AA%BG'SH'H̄S-UGJU	PE--D*H̄-FE130013
T<-3E"/P2S''@&&6	6A-'(_-6P@Y-FOH*	BH?8O|(U(_-Q'C$Q	(V@EHC."/0HS"/¬	'B'3IOH*B'E@VHJ@	$C-OH&SOFE130014
T<'36H?&Q@--FOH*	BH?8RC'(_06)B-D	(_06RC&D(_C6$@YD	FOH*EH?8Ē||'(5TO	'C)M<G-'''E8D̄GJ%	PEJD|504FE130015
T.-4VC)&(5L3"C¬@	<G&7=C¬@.G-66CBQ	4B'7QCJ&(5'7"@YD	FOH*EH?8*C&D(6'6	T@YD'.BY)F1*LD&4	.A0<A41<FE130016
T<O5R@A%BG'.=G%L	GCLP'/0Y+('-(JC7	=B-C''&YH̄OH*''C&	-CQ%4&'6G(O'(-"D	''<B'CC7'/O'1H̄SQ	SI-8H̄MS*FE130017
TH̄66CCM"Z/O@3''2	5H'6E(M'(/"H̄GACN	-CQ|3''P'/OHS"YX	'/05_CMB($&54'''	'''''''''''EUXIK<	CC0%A@LUFE130018
T.&&5@¬.3'|E.'"T	9@|D''|"'6;G0@¬	-B'66C$%(5&C="8'	'''Y6BSOH̄<'Z|BW'	H̄MO''''''.K%ZI2M	TF1UP;D̄HFE130019
EB-9*E7*¬1C"PH$	="7%&F|'''|''C'	''P%'''ASC'''R'A	SO'''Q'''''''''''	''''''0654080C4710	809719$HFE130020

LAST PAGE