IBM System/3 Program Support Field Engineering Handbook

Second Edition (October 1970)
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A form for readers' comments is provided at the back of this publication. If the form has been removed, comments may be addressed to IBM Corporation, FE Technical Operations, Department 900, Rochester, Minnesota 55901.

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ABBREVIATIONS

AAR	Operand 2 Address Register
ALD	Automated Logic Diagram
ALU	Arithmetic and Logic Unit
APL	Advance Program Level
ARR	Address Recall Register
Asynchronous	Without regular time relationships
BAR	Operand 1 Address Register
Bit	Binary digit; smallest unit of information
BM	Bill of Material
BSCA	Binary Synchronous Communications Adapter
BSM	Basic Storage Module
Byte	Eight bits of information plus parity bit
Channel	A hardware device that connects the CPU and main storage with the I/O control units
CPU	Central Processing Unit
CRR	Condition Recall Register
DBI	Data Bus In
DBO	Data Bus Out
DCF	Disk Control Field
DCP	Diagnostic Control Program
DFC	Dual Feed Carriage
DFCR	Disk File Control Register
DFDR	Disk File Data Register
DPF	Dual Program Feature
DRR	Data Recall Register
DSD	Disk Storage Drive
EC	Engineering Change
ECA	Engineering Change Announcement
FBM	Field Bill of Material
FEALD	Field Engineering Automated Logic Diagram
FIP	Fault Isolation Program
IAR	Instruction Address Register
Interrupt	A signal from an I/O device wanting service which causes the central processor to cease its normal execution of instructions and branch out to a new instruction stream.
I/O	Input-Output
IPL	Initial Program Load
ITC	Initial Table of Contents
K	Thousand
L	Length Count
LCR	Length Count Register
LCRR	Length Count Recall Register
LPDAR	Line Printer Data Address Register
LPIAR	Line Printer Image Address Register
LSR	Local Store Register
MES	Miscellaneous Equipment Specification
MFCU	Multi-Function Card Unit

ABBREVIATIONS (continued)

MLC	Machine Level Control
MPCAR	MFCU Punch Data Address Register
MPTAR	MFCU Print Data Address Register
MRDAR	MFCU Read Data Address Register
MST	Monolithic System Technology
PAIR	Product Analysis Incident Report
PEB	Printer Electronic Board
PSR	Program Status Register
REA	Request for Engineering Action
RPQ	Request Price Quotation
SAR	Storage Address Register
SDR	Storage Data Register
SIOC	Serial Input/Output Channel
SLD	Solid Logic Dense
SLT	Solid Logic Technology
SMS	Standard Modular System
S/Z	Sense/Inhibit
TAP	Timing Analysis Program
UCS	Universal Character Set
XR1	Index Register 1
XR2	Index Register 2
XR	Index Register
XRD	X Read
XWR	X Write
YRD	Y Read
YWR	Y Write
Z	Inhibit

PUBLICATIONS

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Theory of Operations	
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IBM System/3 Halt Procedures Guide	GC21-7540

PROGRAM IDENTIFICATION AND SERVICE NUMBER

Program Name	Program Ident	Service Number
Card RPGII	5701-RG1	200041
Card Utilities	5701-UT1	200035
Disk Assembler	5702-AS1	200036
Disk RPGII	5702-RG1	200037
Disk Sort/Merge	5702-SM1	200038
Disk-Card Utilities	5702-UT1	200039
Disk-1255 Utility	5702-UT2	200166
Card SCP	5701-SC1	100000
Disk SCP	5702-SC1	100001

HEX AND DECIMAL CONVERSION/ADDITION

To find the decimal number, locate the Hex number and its decimal equivalent for each position. Add these to obtain the decimal number. To find the Hex number, locate the next lower decimal number and its Hex equivalent. Each difference is used to obtain the next Hex number until the entire number is developed.

BYTE				BYTE				BYTE			
0123		4567		0123		4567		0123		4567	
HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC	HEX	DEC
0	0	0	0	0	0	0	0	0	0	0	0
1	1,048,576	1	65,536	1	4,096	1	256	1	16	1	1
2	2,097,152	2	131,072	2	8,192	2	512	2	32	2	2
3	3,145,728	3	196,608	3	12,288	3	768	3	48	3	3
4	4,194,304	4	262,144	4	16,384	4	1,024	4	64	4	4
5	5,242,880	5	327,680	5	20,480	5	1,280	5	80	5	5
6	6,291,456	6	393,216	6	24,576	6	1,536	6	96	6	6
7	7,340,032	7	458,752	7	28,672	7	1,792	7	112	7	7
8	8,388,608	8	524,288	8	32,768	8	2,048	8	128	8	8
9	9,437,184	9	589,824	9	36,864	9	2,304	9	144	9	9
A	10,485,760	A	655,360	A	40,960	A	2,560	A	160	A	10
B	11,534,336	B	720,896	B	45,056	B	2,816	B	176	B	11
C	12,582,912	C	786,432	C	49,152	C	3,072	C	192	C	12
D	13,631,488	D	851,968	D	53,248	D	3,328	D	208	D	13
E	14,680,064	E	917,504	E	57,344	E	3,584	E	224	E	14
F	15,728,640	F	983,040	F	61,440	F	3,840	F	240	F	15
6		5		4		3		2		1*	

HEXADECIMAL ADDITION

	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
1	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10
2	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11
3	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12
4	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13
5	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14
6	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
7	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16
8	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17
9	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18
A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19
B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A
C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B
D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C
E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D
F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E

5410 CONSOLE LIGHTS/SWITCHES

PROCESSOR CHECKS

I/O LSR	Indicates selection of an LSR by an I/O device was not performed correctly.
LSR F1	Parity is incorrect on the output of the LSR Feature 1.
LSR F2	Parity is incorrect on the output of the LSR Feature 2.
LSR HI	Parity is incorrect on the output of the LSR High.
LSR LO	Parity is incorrect on the output of the basic LSR Low.
SAR HI	Parity is incorrect in the Storage Address Register High.
SAR LO	Parity is incorrect in the Storage Address Register Low.
INV ADDR	Indicates that the SAR contains an invalid address.
SDR	Parity is incorrect in the Storage Data Register.
CAR	Indicates the carry out of the ALU is incorrect.
A/B	Indicates the A or B Register has incorrect parity.
ALU	Indicates the output of the ALU has incorrect parity.
DBI	Parity is incorrect on the CPU end of the Data Bus In.
CPU DBO	Parity is incorrect on the CPU end of the Data Bus Out.
OP/Q	Parity is incorrect in the OP Register or Q Register.
INV OP	Indicates an invalid OP Code in the OP Register.
CHAN DBO	Parity is incorrect on the I/O Device end of the Data Bus Out.
INV Q	Indicates an invalid Q byte is present in an I/O instruction.

I/O ATTENTION

The I/O attention light indicates to the operator that one or more of the attached I/O devices requires attention caused by a 'normal' I/O condition. 'Normal' is defined as: empty hopper, full stacker, out of forms, etc. as opposed to check conditions.

Recovery - Operator must determine cause of indication, rectify the cause and return device to the READY status.

Note Refer to individual devices for 'normal' definition, recovery and/or restart procedures for that device.

UNIT CHECK

TESTABLE INDICATORS

Unit check handling of testable indicators is controlled by software.

Restart procedures are conveyed to the operator via programmed HALT operation, HALT IDENTIFIER'S displayed on the console and recovery/restart procedure listings.

5410 CONSOLE LIGHTS/SWITCHES (continued)

Note: Switches should only be altered with the system in a stop state.

ADDRESS/DATA SWITCHES

These switches are used to set up addresses or data. An address can be loaded into the Storage Address Register. Data can be entered into main storage.

CE KEY SWITCH

This key switch, when switched to the CE position, prevents the customer Usage Meter from running.

CE MODE SELECTOR

This rotary switch selects one of the three processor operating modes: the normal PROCESS mode, the STEP mode, or the TEST mode. PROCESS is the mode for normal programmed system operation.

A. In the STEP mode, the rotary switch setting controls the manner in which the processor performs the stored program.
   1. *Instruction Step.* Each depression and release of the Start key causes one complete instruction to be performed. The I-Phase is performed while the key is pressed, and the E-Phase, if any, when it is released.
   2. *Machine Cycle Step.* Each Start key depression and release advances the instruction through one machine cycle. Depression of the key causes data in storage to be accessed, modified as required, and result to be displayed in the ALU indicators of the console display. Upon release of the key, depending upon the operation being performed, either the old data or the new result is written back into storage.
   3. *Clock Step.* Each depression of the Start key causes the clock to advance through an odd-numbered clock, and each release through an even-numbered one.

      Note: If no DPF on the system, the halt ID lights will not light.

      Note: The integrity of I/O data transfers is preserved by allowing the clock to 'idle' from I-Phase end of every executable Start I/O instruction, until data transfer to or from the device is complete.

B. The switch settings under the TEST mode permit the following:
   1. *Alter SAR.* The address, set up in the address switches, is transferred into SAR by the Start key via the current IAR. Both SAR and IAR are modified.
   2. *Alter Storage.* Depression of the Start key transfers data, set up in the rightmost two Data Switches, into the A register. Releasing the key causes this data to be placed in the storage location specified by SAR and into the Q register.
   3. *Display Storage.* The contents of the storage location specified by SAR are transferred into the B register when the Start key is pressed. These contents are rewritten into storage when the key is released, and are also transferred into the Q register.

      Note: The STORAGE TEST SWITCH must be in the STEP position to avoid a processor check when changing the CE MODE SELECTOR from ALTER STORAGE position to DISPLAY STORAGE position and vice versa. Invalid address are not checked for while the system is in the TEST mode.

5410 CONSOLE LIGHTS/SWITCHES (continued)

STORAGE TEST SWITCH

This switch enables the altering or displaying of storage as follows:

A. In the STEP position, a storage location is accessed with each depression of the Start key.
B. In the RUN position, following the Start key depression, core storage is exercised by accessing either the same location repetively or all of core sequentially (see Address Increment Switch).

ADDRESS INCREMENT SWITCH

This switch enables address incrementing when in the CE test modes of Alter or Display storage. With the switch in the ON position, the contents of SAR are incremented by one after each storage access. When the switch is in the OFF position, SAR is not incrementing.

I/O OVERLAP SWITCH

This switch modifies control of the system so that I/O operations may be executed in either an overlap or a non-overlap mode. With the switch in the normal ON position, I/O operations are executed in an overlap mode. When the switch is in the OFF position, I/O operation is completed prior to execution of the next sequential instruction.

LSR DISPLAY SELECTOR (Should be in the normal position when processing.)

This rotary switch selects the Local Storage Register (LSR) whose contents are to be displayed.

LSR's that can be manually selected for display via this switch are: IAR, ARR, XR1, and XR2.

Refer to MST Tie-Up Data for procedure to display other LSRs.

When the switch is in the Normal or OFF position, the system controls the selection and display of the LSR's. If the switch is in other than the Normal position, the specified LSR is selected and its contents are available for display whenever the processor clock is stopped, or if the clock is running, when no CPU machine cycles and no I/O data transfer cycles are being taken. In the OFF position LSR selection by the CPU is inhibited and if no I/O device is selecting an LSR, the LSR display will have all bits OFF.

5410 CONSOLE LIGHTS/SWITCHES (continued)

SYSTEM RESET KEY

A system reset causes the system to enter an immediate 'idle' state. All I/O machine registers, controls, and status indicators are reset and the processor clock is allowed to 'idle'. A complete program restart is normally required after a system reset.

The following LSR's are reset to zero by a system reset:

P1 - IAR
P1 - PSR
P2 - PSR

The other LSR's are not changed by a system reset.

Note: The CE mode selector must be in process mode for the system reset key to be effective.

CHECK RESET KEY

This pushbutton is pressed to cause a reset of the Processors and/or I/O check conditions, and also resets a system power check to allow a power on retry.

A check reset removes the current error conditions, thus allowing the processor to resume its operation after the Start key is depressed.

FILE WRITE SWITCH

This switch when in the OFF position will inhibit all writing on all disk surfaces.

DPF Switches

P1 Switch - Dual Program Level One. When OFF, inhibits branching into Program Level One.
P2 Switch - Dual Program Level Two. When OFF, inhibits branching into Program Level Two.

Warning - Unpredictable errors will occur if both P1 and P2 switches are off.

5410 CONSOLE LIGHTS/SWITCHES (continued)

ADDRESS COMPARE SWITCH

This switch allows stopping the program when the setting of the (Address/Data) switches matches SAR. This switch will only be functional when the register display is positioned to SAR and the system is in the PROCESS mode.

With the switch in the RUN position, comparison of address switches to SAR via the register display is performed, but no processor stop is initiated when a match occurs. The 'matched' signal is provided as a CE 'sync' point.

When the switch is in the STOP position, a match of the address switches and the register display results in a processor stop at the completion of the storage read-write cycle.

The processor is restarted by activating the Start key.

Note: The integrity of I/O data transfers is preserved. The contents of SAR do not necessarily match the setting of the address switches at stop time.

I/O CHECK SWITCH

This switch, when on, forces the processor to come to an immediate stop on certain I/O errors.

The switch is normally set to RUN. With the switch set to STOP, the processor stops on an I/O error with the console display frozen to indicate the processor status at the time the error stop occurred, and the I/O device turns ON the I/O check light.

A check reset followed by the Start key is the normal restart after an I/O error stop.

Note: When the I/O check switch is in the STOP position and an I/O error occurs, the processor check light will turn ON.

PARITY CHECK SWITCH

This switch enables override of the processor parity errors.

The switch is normally set to STOP. This causes the processor to come to an immediate stop whenever a parity error is detected. A check reset followed by the Start key is the normal restart after a parity stop. With the parity switch in the RUN position, parity errors are detected and displayed, but the processor is not stopped.

ADDRESS COMPARE LIGHT

This light is on whenever the address switches match the contents of the Storage Address Register, the register display is positioned to SAR and the address compare switch is in the STOP position.

5410 CONSOLE LIGHTS/SWITCHES (continued)

BSCA Panel

(X) DT TERM READY
Lights when the BSCA is enabled and the data terminal ready line to the MODEM is on. In case of the connect data set to line requirement, the indicator lights when the connect data set to line signal is activated.

(X) TEST MODE
Lights when an SIO instruction has been issued by the program to place the BSCA in test mode.

(X) BSCA ATTN
Lights when the BSCA rejects an SIO instruction because operator intervention is required because:

1. The data set ready latch is off when a receive, receive and transmit, or receive initial SIO instruction is executed.
2. The auto call unit power is off or the data line is occupied when an SIO auto call or an SIO receive initial instruction is executed (switched networks).
3. The BSCA is disabled.
4. The external test switch is on and the BSCA is not in test mode. An SIO control instruction is used to enable the BSCA and to place the BSCA in test mode.
5. If the data ready signal from the MODEM is de-activated unexpectedly while the BSCA is enabled.

(X) TSM MODE
Lights when the BSCA is to perform a transmit operation.

(X) RECEIVE MODE
Lights when the BSCA is to perform a receive operation.

(X) RECEIVE INITIAL
Lights when a receive initial SIO instruction is received. It turns off at the end of the receive initial operation.

(X) CONTROL MODE
(Station Select Feature) Lights when an EOT sequence is detected in a transmit, receive, or receive initial monitor operation. It turns off by the decode of an SOH or STX or a receive timeout.

(X) ACU PWR OFF
(Auto Call Feature) Lights when the auto call unit has power off.

5410 CONSOLE LIGHTS/SWITCHES (continued)

BSCA Panel

(X) DATA MODE
Lights when an SOH or STX is decoded during a transmit or a receive operation. It is turned off at the end of the operation.

(X) DT SET READY
Lights when the data set ready line from the MODEM is active and the MODEM is ready for use.

(X) EXT TEST SW
Lights when the switch at the MODEM end of the medium speed MODEM cable is in the test position or the switch on the CPU CE panel for high-speed feature is in the local test position.

(X) TSM TRIGGER
Lights when the transmit trigger is at a binary zero state (equivalent to a space on the communication line).

(X) RECEIVE TRIGGER
Lights when the receive trigger is at a binary zero state (equivalent to a space on the communication line).

(X) UNIT CHECK
Lights when unit check condition exists. Turned on by any bit in status byte 2 (see SNS inst "N" code 011).

(X) DIGIT PRESENT
(Auto Call Unit Feature) Lights when the BSCA has a digit present on the auto call unit interface to be used for dialing.

(X) DT LINE IN USE
(Auto Call Unit Feature) Lights when the data line occupied from the ACU is active.

(X) CLEAR TO SEND
Lights when the line from the MODEM is active. The BSCA may now transmit.

(X) CHAR PHASE
Lights when the adapter has established character synchronization with the transmitting station by receiving two successive SYN characters. The indicator is turned off at the end of the receive operation.

(X) BUSY
Lights when the BSCA is executing a receive initial, transmit and receive, auto call, receive, or loop test instruction.

(X) CALL REQUEST
(Auto Call Unit Feature) Lights when the BSCA receives an auto call SIO instruction and is performing an auto call operation.

5410 CONSOLE LIGHTS/SWITCHES (continued)

I/O Check Light

This light is turned on when the following I/O errors are detected:

1442

1. A SIO instruction is issued to the 1442 and the NO-OP bit is on.

2. Whenever the 1442 Attachment detects the following:
   - Punch check
   - Read reg
   - Overrun
   - Any condition that turns on the 1442 check light

This light is turned OFF by a system reset, a check reset, an NPRO, the SNS instruction which senses the NO-OP bit (if a NO-OP was the cause), or by a SIO instruction to the 1442 in the case of a read check or a punch check.

5424 MFCU

1. An SIO instruction is issued to the 5424 and the NO-OP bit is ON.

2. Whenever the 5424 Attachment detects the following:
   PRINT DATA CHECK
   PRINT CLUTCH CHECK
   PUNCH CHECK
   PUNCH INVALID CHECK
   READ CHECK

This light is turned OFF by a system reset, a check reset, or an NPRO for all of the above checks. It may also be reset by the SNS instruction to the MFCU in the case of NO-OP, print data check, print clutch check or a punch invalid check, or by a SIO instruction to the MFCU in the case of a read check or a punch check.

SIOC

Indicates a data transfer register parity error occurred.

This light is turned off by a system reset, check reset or by a SIO instruction.

5410 CONSOLE LIGHTS/SWITCHES (continued)

I/O Check Light

PRINTER - 5203

1. A SIO instruction is issued to the 5203 and the 5203 check light is ON.

2. Whenever the 5203 Attachment detects the following:
   INCREMENTOR FAILURE CHECK
   HAMMER ECHO CHECK
   ANY HAMMER ON CHECK

This light is turned off by a system reset, a check reset, the printer start key or by the SNS instruction which senses the check bit.

FILE - 5444

None

KEYBOARD PRINTER 5471

None

KEYBOARD - 5475

None

BSCA

Indicates a unit check has occurred. See BSCA SNS inst, N code 011, byte 2 for specific error.

This light is turned off by a system reset, a check reset, or through programming in the case of retry.

LOCAL STORE REGISTERS

BASE SYSTEM

HIGH	LOW	LSR Acronym
Program level 1 instruction address register		P1-IAR
Program level 1 address recall register		P1-ARR
Operand 2 address register		AAR
Spare		
Program level 1 index register 1		P1-XR1
Length count recall register	Condition recall register	P1-PSR
Operand 1 address register		BAR
MFCU print data address register		MPTAR
Program level 1 index register 2		P1-XR2
Line printer data address register		LPDAR
Line printer image address register		LPIAR
MFCU punch data address register		MPCAR
MFCU read address register		MRDAR
Length count registers	Data recall register	LCR DRR
Interrupt level 1 instruction address register		IAR-1
Interrupt level 1 address recall register		ARR-1

FEATURE 1

HIGH	LOW	LSR Acronym
Program level 2 instruction address register		P2-IAR
Program level 2 address recall register		P2-ARR
Bi-sync comm adapter address register		BSCAR
Serial I/O channel address register		SIAR
Program level 2 status register		P2-PSR
Interrupt level 4 instruction address register		IAR-4
Interrupt level 4 address recall register		ARR-4
Disk file control address register		DFCR
Program level 2 index register 2		P2-XR2
Spare		Spare
Interrupt level 2 instruction address register		IAR-2
Interrupt level 2 address recall register		ARR-2
Disk file data address register		DFDR
Program level 2 index register 1		P2-XR1
Interrupt level 0, instruction address register		IAR-0
Interrupt level 0 address recall register		ARR-0

ENVIRONMENTAL RECORDING

CARD SYSTEM

Errors detected during an RPG object program run will be stored in the communications area starting at core location /0180/. Forty-two bytes have been reserved for this, broken into two sections of 10 and 32 bytes. The 6-byte section is used to record 5203 hammer echo checks. Each of the 6 bytes will contain the failing print position. (Refer to Table 3 in the 5203 map charts.) In case more than six errors have occured, only the last six will be shown. The 32-byte section is made up of eight 4-byte sections showing the last eight errors to occur. Each 4-byte section will contain the Q, R, and 2 sense bytes of data about the failing instruction. These 42 bytes of information along with the date will be punched out into a card during a system installation run. This card will be merged with the system initialization program deck and will be the card just preceding the end card. This data will be the error data accumulated since the last system initialization run.

The card format for the card punched out is:

Col 1 - W
Col 2 thru 65 - Error history table in hex. Eight sections of 4 bytes each containing the Q, R, and 2 sense bytes.
Col 66 thru 77 - 5203 hammer echo check data
Col 78 thru 93 - Reserved
Col 94 thru 96 - Date (coded)
(Card format effective with SIP Vers 1 Mod 3)

DISK SYSTEM

Statistical Data Recording (SDR)

Statistical data is recorded in a table occupying sectors X'0C' through X'18'. This table consists of 512 two-byte counters. Each device is allotted an area consistent with the number of distinguishable errors possible for that device. Devices such as the 5444 and BSCA will have counters to record both temporary and permanent error occurrences. A permanent error is defined as one which persists throughout the maximum number of retries outlined in the device's error recovery procedures. A temporary error is defined as one where recovery occurs before the maximum number of retries.

For example:

Disk File

	Overrun	Data Check in ID	
Temp	2 bytes	2 bytes	etc
Perm	2 bytes	2 bytes	etc

ENVIRONMENTAL RECORDING (continued)

Out Board Recording (OBR)

Each error, whether temporary or permanent, is entered in a history table. This table is two sectors long (sectors 1C and 20 and provides 63 8-byte entries. The first four bytes of this sector will be two 2-byte displacements. The first will be the displacement of the next available entry in the table and the second will be the end of the table. This table will be recursive and no overflow or stop logic will be provided. The 64th time an entry is made, it will overlay the first entry; the 65th time will overlay the second, etc. Therefore, the table will always contain entries for the 63 most recent errors.

The basic entry for each device will consist of the following:

Q	R	PRIMARY SENSE REGISTER	DEVICE DEPENDENT INFO
1 byte	1 byte	2 bytes	4 bytes

Disk errors will require two entries (16 bytes).

In addition to SDR and OBR recording, statistics are kept on each disk volume to help detect surface degradation. Each volume has an area to record the number of write and non-write SIOs issued to that volume, a count of temporary errors and a table of permanent errors occurring on that volume. A master table of all writes and non-writes issued to each unit on the system is kept on cylinder 0, sector 0C. Control SIOs are not included in these statistics.

The master table for a dual drive, full capacity system looks like this:

		Displacement X'0C' ↓ Writes & Verifies	Reads & Scans
DRIVE 1	REM	4 bytes	4 bytes
	FIXED	4 bytes	4 bytes
DRIVE 2	REM	4 bytes	4 bytes
	FIXED	4 bytes	4 bytes

CODE CONVERSION CHART

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
000	00	C		4	1	00000000	
001	01	DCBA 1		A @	A 3	00000001	
002	02	DCBA 2		B @	B 3	00000010	
003	03	DCBA 21		C @	C 3	00000011	
004	04	DCBA 4	ZAZ	D @	D 3	00000100	
005	05	DCBA 4 1		E @	E 3	00000101	
006	06	DCBA 42	AZ	F @	F 3	00000110	
007	07	DCBA 421	SZ	G @	G 3	00000111	
008	08	DCBA8	MVX	H @	H 3	00001000	
009	09	DCBA8 1		I @	I 3	00001001	
010	0A	CBA8 2	ED	¢ 4	ç 1	00001010	
011	0B	CBA8 21	ITC	. 4	. 1	00001011	
012	0C	CBA84	MVC	< 4	< 1	00001100	
013	0D	CBA84 1	CLC	(4	(1	00001101	
014	0E	CBA842	ALC	+ 4	+ 1	00001110	
015	0F	CBA8421	SLC	| 4	| 1	00001111	
016	10	C A8 2		& 4	& 1	00010000	
017	11	DCB 1		J @	J 3	00010001	
018	12	DCB 2		K @	K 3	00010010	
019	13	DCB 21		L @	L 3	00010011	
020	14	DCB 4	ZAZ	M @	M 3	00010100	
021	15	DCB 4 1		N @	N 3	00010101	
022	16	DCB 42	AZ	O @	O 3	00010110	
023	17	DCB 421	SZ	P @	P 3	00010111	
024	18	DCB 8	MVX	Q @	Q 3	00011000	
025	19	DCB 8 1		R @	R 3	00011001	
026	1A	CB 8 2	ED	! 4	! 1	00011010	
027	1B	CB 8 21	ITC	$ 4	$ 1	00011011	
028	1C	CB 84	MVC	* 4	* 1	00011100	
029	1D	CB 84 1	CLC	) 4	) 1	00011101	
030	1E	CB 842	ALC	; 4	; 1	00011110	
031	1F	CB 8421	SLC	¬ 4	¬ 1	00011111	
032	20	CB		4	1	00100000	
033	21	C A 1		, 4	, 1	00100001	
034	22	DC A 2		S ‘	S 3	00100010	
035	23	DC A 21		T ’	T 3	00100011	
036	24	DC A 4	/AZ	U “	U 3	00100100	
037	25	DC A 4 1		V ”	V 3	00100101	
038	26	DC A 42	AZ	W •	W 3	00100110	
039	27	DC A 421	SZ	X –	X 3	00100111	
040	28	DC A8	MVX	Y —	Y 3	00101000	
041	29	DC A8 1		Z ˜	Z 3	00101001	
042	2A	DCBA	ED	} ™	} 3	00101010	
043	2B	C A8 21	ITC	. 4	. 1	00101011	
044	2C	C A84	MVC	< 4	% 1	00101100	
045	2D	C A84 1	CLC	_ 4	_ 1	00101101	
046	2E	C A842	ALC	> 4	> 1	00101110	
047	2F	C A8421	SLC	? 4	? 1	00101111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
048	30	DC A	SNS	0 @	0 3	00110000	
049	31	DC 1	LIO	1 @	1 3	00110001	
050	32	DC 2		2 @	2 3	00110010	
051	33	DC 21		3 @	3 3	00110011	
052	34	DC 4	ST	4 @	4 3	00110100	
053	35	DC 4 1	L	5 @	5 3	00110101	
054	36	DC 42	A	6 @	6 3	00110110	
055	37	DC 421		7 @	7 3	00110111	
056	38	DC 8	TBN	8 @	8 3	00111000	
057	39	DC 8 1	TBF	9 @	9 3	00111001	
058	3A	C 8 2	SBN	4	: 1	00111010	
059	3B	C 8 21	SBF	# 4	# 1	00111011	
060	3C	C 84	MVI	@ 4	@ 1	00111100	
061	3D	C 84 1	CLI	' 4	' 1	00111101	
062	3E	C 842		= 4	= 1	00111110	
063	3F	C 8421		" 4	" 1	00111111	
064	40	None				01000000	Space
065	41	D BA 1		A 8	A 2	01000001	
066	42	D BA 2		B 8	B 2	01000010	
067	43	D BA 21		C 8	C 2	01000011	
068	44	D BA 4	ZAZ	D 8	D 2	01000100	
069	45	D BA 4 1		E 8	E 2	01000101	
070	46	D BA 42	AZ	F 8	F 2	01000110	
071	47	D BA 421	SZ	G 8	G 2	01000111	
072	48	D BA8	MVX	H 8	H 2	01001000	
073	49	D BA8 1		I 8	I 2	01001001	
074	4A	BA8 2	ED	¢	¢	01001010	¢
075	4B	BA8 21	ITC	.	.	01001011	.
076	4C	BA84	MVC	<	<	01001100	<
077	4D	BA84 1	CLC	(	(	01001101	(
078	4E	BA842	ALC	+	+	01001110	+
079	4F	BA8421	SLC	|	|	01001111	|
080	50	A8 2		&	&	01010000	&
081	51	D B 1		J 8	J 2	01010001	
082	52	D B 2		K 8	K 2	01010010	
083	53	D B 21		L 8	L 2	01010011	
084	54	D B 4	ZAZ	M 8	M 2	01010100	
085	55	D B 4 1		N 8	N 2	01010101	
086	56	D B 42	AZ	O 8	O 2	01010110	
087	57	D B 421	SZ	P 8	P 2	01010111	
088	58	D B 8	MVX	Q 8	Q 2	01011000	
089	59	D B 8 1		R 8	R 2	01011001	
090	5A	B 8 2	ED	!	!	01011010	!
091	5B	B 8 21	ITC	$	$	01011011	$
092	5C	B 84	MVC	*	*	01011100	*
093	5D	B 84 1	CLC	)	)	01011101	)
094	5E	B 842	ALC	;	;	01011110	;
095	5F	B 8421	SLC	¬	¬	01011111	¬

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
096	60	B		–	–	01100000	–
097	61	A 1		/	/	01100001	/
098	62	D A 2		S 8	S 2	01100010	
099	63	D A 21		T 8	T 2	01100011	
100	64	D A 4	ZAZ	U 8	U 2	01100100	
101	65	D A 4 1		V 8	V 2	01100101	
102	66	D A 42	AZ	W 8	W 2	01100110	
103	67	D A 421	SZ	X 8	X 2	01100111	
104	68	D A8	MVX	Y 8	Y 2	01101000	
105	69	D A8 1		Z 8	Z 2	01101001	
106	6A	D BA	ED	} 8	} 2	01101010	
107	6B	A8 21	ITC	,	,	01101011	,
108	6C	A84	MVC	%	%	01101100	%
109	6D	A84 1	CLC	_	_	01101101	_
110	6E	A842	ALC	>	>	01101110	>
111	6F	A8421	SLC	?	?	01101111	?
112	70	D A	SNS	0 8	0 2	01110000	
113	71	D 1	LIO	1 8	1 2	01110001	
114	72	D 2		2 8	2 2	01110010	
115	73	D 21		3 8	3 2	01110011	
116	74	D 4	ST	4 8	4 2	01110100	
117	75	D 4 1	L	5 8	5 2	01110101	
118	76	D 42	A	6 8	6 2	01110110	
119	77	D 421		7 8	7 2	01110111	
120	78	D 8	TBN	8 8	8 2	01111000	
121	79	D 8 1	TBF	9 8	9 2	01111001	
122	7A	8 2	SBN			01111010	
123	7B	8 21	SBF	#	#	01111011	#
124	7C	84	MVI	@	@	01111100	@
125	7D	84 1	CLI	'	'	01111101	'
126	7E	842		=	=	01111110	=
127	7F	8421		"	"	01111111	"
128	80	DC		@	3	10000000	
129	81	CBA 1		A 4	A 1	10000001	
130	82	CBA 2		B 4	B 1	10000010	
131	83	CBA 21		C 4	C 1	10000011	
132	84	CBA 4	ZAZ	D 4	D 1	10000100	
133	85	CBA 4 1		E 4	E 1	10000101	
134	86	CBA 42	AZ	F 4	F 1	10000110	
135	87	CBA 421	SZ	G 4	G 1	10000111	
136	88	CBA8	MVX	H 4	H 1	10001000	
137	89	CBA8 1		I 4	I 1	10001001	
138	8A	DCBA8 2	ED	c @	c 3	10001010	
139	8B	DCBA8 21	ITC	. @	. 3	10001011	
140	8C	DCBA84	MVC	< @	< 3	10001100	
141	8D	DCBA84 1	CLC	(@	(3	10001101	
142	8E	DCBA842	ALC	+ @	+ 3	10001110	
143	8F	DCBA8421	SLC	! @	! 3	10001111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
144	90	CBA		] 4	} 1	10010000	
145	91	CB 1		J 4	J 1	10010001	
146	92	CB 2		K 4	K 1	10010010	
147	93	CB 21		L 4	L 1	10010011	
148	94	CB 4	ZAZ	M 4	M 1	10010100	
149	95	CB 4 1		N 4	N 1	10010101	
150	96	CB 42	AZ	O 4	O 1	10010110	
151	97	CB 421	SZ	P 4	P 1	10010111	
152	98	CB 8	MVX	Q 4	Q 1	10011000	
153	99	CB 8 1		I 4	I 1	10011001	
154	9A	DCB 8 2	ED	! @	! 3	10011010	
155	9B	DCB 8 21	ITC	$ @	$ 3	10011011	
156	9C	DCB 84	MVC	* @	* 3	10011100	
157	9D	DCB 84 1	CLC	) @	) 3	10011101	
158	9E	DCB 842	ALC	; @	; 3	10011110	
159	9F	DCB 8421	SLC	¬ @	¬ 3	10011111	
160	A0	DCB		- @	- 3	10100000	
161	A1	DC A 1		/ @	/ 3	10100001	
162	A2	C A 2		S 4	S 1	10100010	
163	A3	C A 21		T 4	T 1	10100011	
164	A4	C A 4	ZAZ	U 4	U 1	10100100	
165	A5	C A 4 1		V 4	V 1	10100101	
166	A6	C A 42	AZ	W 4	W 1	10100110	
167	A7	C A 421	SZ	X 4	X 1	10100111	
168	A8	C A8	MVX	Y 4	Y 1	10101000	
169	A9	C A8 1		Z 4	Z 1	10101001	
170	AA	DC A8 2	ED	& @	& 3	10101010	
171	AB	DC A8 21	ITC	. @	. 3	10101011	
172	AC	DC A84	MVC	% @	% 3	10101100	
173	AD	DC A84 1	CLC	_ @	_ 3	10101101	
174	AE	DC A842	ALC	> @	> 3	10101110	
175	AF	DC A8421	SLC	? @	? 3	10101111	
176	B0	C A	SNS	0 4	0 1	10110000	
177	B1	C 1	LIO	1 4	1 1	10110001	
178	B2	C 2		2 4	2 1	10110010	
179	B3	C 21		3 4	3 1	10110011	
180	B4	C 4	ST	4 4	4 1	10110100	
181	B5	C 4 1	L	5 4	5 1	10110101	
182	B6	C 42	A	6 4	6 1	10110110	
183	B7	C 421		7 4	7 1	10110111	
184	B8	C 8	TBN	8 4	8 1	10111000	
185	B9	C 8 1	TBF	9 4	9 1	10111001	
186	BA	DC 8 2	SBN	: @	: 3	10111010	
187	BB	DC 8 21	SBF	# @	# 3	10111011	
188	BC	DC 84	MVI	@ @	@ 3	10111100	
189	BD	DC 84 1	CLI	' @	' 3	10111101	
190	BE	DC 842		= @	= 3	10111110	
191	BF	DC 8421		" @	" 3	10111111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
192	C0	D	BC	& 8	2	11000000	
193	C1	BA 1	TIO	A	A	11000001	A
194	C2	BA 2	LA	B	B	11000010	B
195	C3	BA 21		C	C	11000011	C
196	C4	BA 4		D	D	11000100	D
197	C5	BA 4 1		E	E	11000101	E
198	C6	BA 42		F	F	11000110	F
199	C7	BA 421		G	G	11000111	G
200	C8	BA8		H	H	11001000	H
201	C9	BA8 1		I	I	11001001	I
202	CA	D BA8 2		Ç 8	Ç 2	11001010	
203	CB	D BA8 21		. 8	. 2	11001011	
204	CC	D BA84		< 8	< 2	11001100	
205	CD	D BA84 1		(8	(2	11001101	
206	CE	D BA842		+ 8	+ 2	11001110	
207	CF	D BA8421		| 8	| 2	11001111	
208	D0	BA	BC	}	}	11010000	}
209	D1	B 1	TIO	J	J	11010001	J
210	D2	B 2	LA	K	K	11010010	K
211	D3	B 21		L	L	11010011	L
212	D4	B 4		M	M	11010100	M
213	D5	B 4 1		N	N	11010101	N
214	D6	B 42		O	O	11010110	O
215	D7	B 421		P	P	11010111	P
216	D8	B 8		Q	Q	11011000	Q
217	D9	B 8 1		R	R	11011001	R
218	DA	D B 8 2		! 8	! 2	11011010	
219	DB	D B 8 21		$ 8	$ 2	11011011	
220	DC	D B 84		* 8	* 2	11011100	
221	DD	D B 84 1		) 8	) 2	11011101	
222	DE	D B 842		; 8	; 2	11011110	
223	DF	D B 8421		¬ 8	¬ 2	11011111	
224	E0	D B	BC	- 8	- 2	11100000	
225	E1	D A 1	TIO	/ 8	/ 2	11100001	
226	E2	A 2	LA	S	S	11100010	S
227	E3	A 21		T	T	11100011	T
228	E4	A 4		U	U	11100100	U
229	E5	A 4 1		V	V	11100101	V
230	E6	A 42		W	W	11100110	W
231	E7	A 421		X	X	11100111	X
232	E8	A8		Y	Y	11101000	Y
233	E9	A8 1		Z	Z	11101001	Z
234	EA	D A8 2		& 8	& 2	11101010	
235	EB	D A8 21		. 8	. 2	11101011	
236	EC	D A84		% 8	% 2	11101100	
237	ED	D A84 1		_ 8	_ 2	11101101	
238	EE	D A842		> 8	> 2	11101110	
239	EF	D A8421		? 8	? 2	11101111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

CODE CONVERSION CHART (continued)

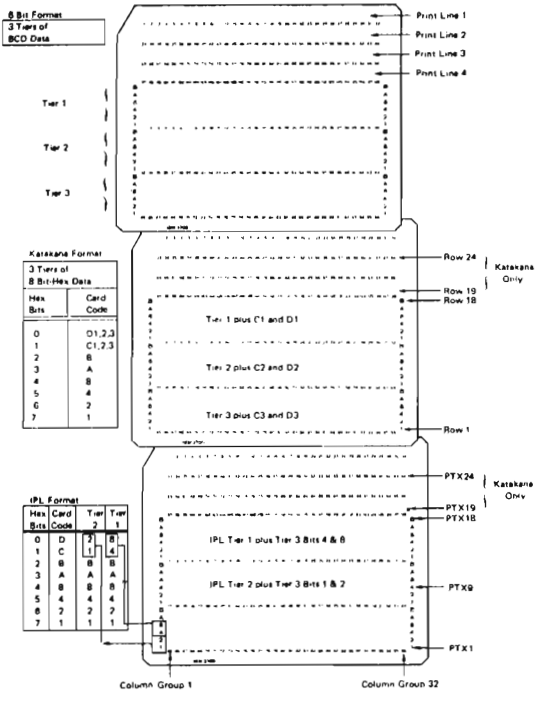
Dec Val	Hex Val	Card Code DCBA8421	Mnem	IPL* T1T3	IPL* T2T3	EBCDIC	Symbol
240	F0	A	HPL	0	0	11110000	0
241	F1	1	APL	1	1	11110001	1
242	F2	2	JC	2	2	11110010	2
243	F3	21	SIO	3	3	11110011	3
244	F4	4		4	4	11110100	4
245	F5	4 1		5	5	11110101	5
246	F6	42		6	6	11110110	6
247	F7	421		7	7	11110111	7
248	F8	8		8	8	11111000	8
249	F9	8 1		9	9	11111001	9
250	FA D	8 2		: 8	: 2	11111010	
251	FB D	8 21		# 8	# 2	11111011	
252	FC D	84		@ 8	@ 2	11111100	
253	FD D	84 1		' 8	' 2	11111101	
254	FE D	842		= 8	= 2	11111110	
255	FF D	8421		" 8	" 2	11111111	

* If both tier 1 and tier 2 columns are being used, the tier 3 punches are added together as shown in the table at the end of this chart.

*Tier 3 character addition table

Tier 3 card bits required by tier 1 character \ Tier 3 card bits required by tier 2 character		1	2	3 (1+2 bits)
	4	5 (4+1 bits)	6 (4+2 bits)	7 (4+2+1 bits)
	8	9 (8+1 bits)	: (8+2 bits)	# (8+2+1 bits)
	@ (4+8 bits)	' (8+4+1 bits)	= (8+4+2 bits)	" (8+4+2+1 bits)

96 COLUMN CARD LAYOUT



STANDARD INSTRUCTION SET

	Mnem	Op	Q	Operands				Comments
Two Address Instruction	ZAZ	4	L_1L_2					Zero and add zoned
	AZ	6	L_1L_2					Add zoned decimal
	SZ	7	L_1L_2					Subtract zoned decimal
	MVX	8	L_1L_2					Move hex characters
	ED	A	L_1					Edit
	ITC	B	L_1					Insert and test characters
	MVC	C	L					Move characters
	CLC	D	L					Compare logical characters
	ALC	E	L					Add logical characters
	SLC	F	L					Subtract logical characters

0	Op1	Op2	Op1 direct, Op2 direct
1	Op1	Op2	Op1 direct, Op2 indexed by XR1
2	Op1	Op2	Op1 direct, Op2 indexed by XR2
4	Op1	Op2	Op1 indexed by XR1, Op2 direct
5	Op1	Op2	Op1 indexed by XR1, Op2 indexed by XR1
6	Op1	Op2	Op1 indexed by XR1, Op2 indexed by XR2
8	Op1	Op2	Op1 indexed by XR2, Op2 direct
9	Op1	Op2	Op1 indexed by XR2, Op2 indexed by XR1
A	Op1	Op2	Op1 indexed by XR2, Op2 indexed by XR2

STANDARD INSTRUCTION SET (continued)

One Address Instruction (Non-Branch)	SNS	0	DA M N			Sense I/O
	LIO	1	DA M N			Load I/O
	ST	4	Reg			Store register
	L	5	Reg			Load register
	A	6	Reg			Add to register
	TBN	8	Mask			Test bits on
	TBF	9	Mask			Test bits off
	SBN	A	Mask			Set bits on
	SBF	B	Mask			Set bits off
	MVI	C	I_2			Move logical immediate
	CLI	D	I_2			Compare logical immediate
		3		Op1 Addr		Op1 direct
		7		Op1		Op1 indexed by XR1
		B		Op1		Op1 indexed by XR2
One Address Instruction (Branch)	BC	0	Cond.			Branch on condition
	TIO	1	DA M N			Test I/O and branch
	LA	2	Bit 6-XR2 Bit 7-XR1			Load address
		C		Op 1 Addr		Op 1 direct
		D		Op 1		Op 1 indexed by XR1
		E		Op 1		Op 1 indexed by XR2
Command Instruction	HPL	F0	Tens	Unit		Halt program level
	APL	F1	DA M N	N U		Advance program level
	JC	F2	Cond.	Number of bytes to jump		Jump on condition
	SIO	F3	DA M N	Control		Start I/O

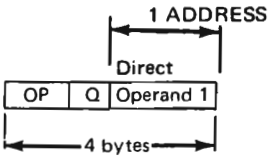
INSTRUCTION FORMATS

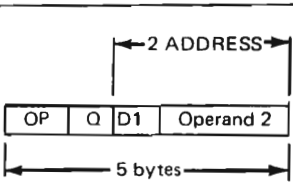
INSTRUCTION FORMAT REFERENCE

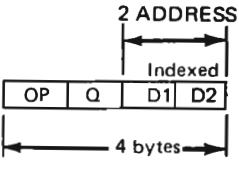
OP	MNEMONIC	TYPE
04	ZAZ	
06	AZ	2 ADDRESS
07	SZ	
08	MVX	Direct
0A	ED	OP | Q | Operand 1 | Operand 2
0B	ITC	
0C	MVC	6 bytes
0D	CLC	
0E	ALC	
0F	SLC	
14	ZAZ	
16	AZ	2 ADDR
17	SZ	
18	MVX	Direct Indexed
1A	ED	OP | Q | Operand 1 | D2
1B	ITC	
1C	MVC	5 bytes
1D	CLC	
1E	ALC	XR1
1F	SLC	
24	ZAZ	
26	AZ	2 ADDR
27	SZ	
28	MVX	Direct Indexed
2A	ED	OP | Q | Operand 1 | D2
2B	ITC	
2C	MVC	5 bytes
2D	CLC	
2E	ALC	XR2
2F	SLC	

INSTRUCTION FORMAT REFERENCE (continued

OP	MNEMONIC	TYPE
30	SNS	
31	LIO	
34	ST	
35	L	
36	A	
38	TBN	
39	TBF	
3A	SBN	
3B	SBF	
3C	MVI	
3D	CLI	
44	ZAZ	
46	AZ	
47	SZ	
48	MVX	
4A	ED	
4B	ITC	
4C	MVC	
4D	CLC	
4E	ALC	
4F	SLC	
54	ZAZ	
56	AZ	
57	SZ	
58	MVX	
5A	ED	
5B	ITC	
5C	MVC	
5D	CLC	
5E	ALC	
5F	SLC	



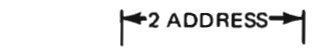
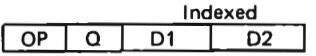
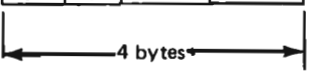
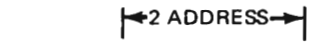
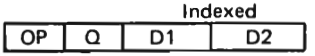
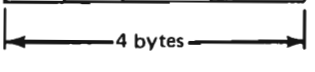
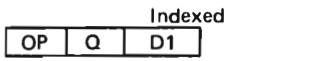
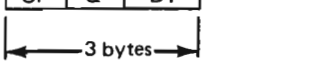




INSTRUCTION FORMAT REFERENCE (continued)

OP	MNEMONIC	TYPE
64	**ZAZ**	
66	AZ	2 ADDRESS
67	SZ	
68	MVX	
6A	ED	OP Q D1 D2
6B	ITC	
6C	MVC	4 bytes
6D	CLC	
6E	ALC	XR1 XR2
6F	SLC	
70	SNS	
71	LIO	1 ADDRESS
74	ST	
75	L	
76	A	OP Q D1
78	TBN	
79	TBF	3 bytes
7A	SBN	
7B	SBF	
7C	MVI	XR1
7D	CLI	
84	ZAZ	
86	AZ	2 ADDRESS
87	SZ	
88	MVX	Indexed Direct
8A	ED	OP Q D1 Operand 2
8B	ITC	
8C	MVC	5 bytes
8D	CLC	
8E	ALC	XR2
8F	SLC	

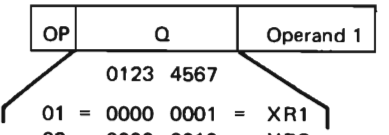
INSTRUCTION FORMAT REFERENCE (continued)

OP	MNEMONIC	TYPE
94	ZAZ	
96	AZ	
97	SZ	
98	MVX	
9A	ED	
9B	ITC	
9C	MVC	
9D	CLC	
9E	ALC	XR2 XR1
9F	SLC	
A4	ZAZ	
A6	AZ	
A7	SZ	
A8	MVX	
AA	ED	
AB	ITC	
AC	MVC	
AD	CLC	
AE	ALC	XR2 XR2
AF	SLC	
B0	SNS	
B1	LIO	1 ADDRESS
B4	ST	
B5	L	
B6	A	
B8	TBN	
B9	TDF	
BA	SBN	
BB	SBF	
BC	MVI	XR2
BD	CLI	

INSTRUCTION FORMAT REFERENCE (continued)

OP	MNEMONIC		TYPE
C0	BC		
C1	TIO	OP | Q | Address	
C2	LA	←4 bytes→	
D0	BC		
D1	TIO	OP | Q | D2	+XR1
D2	LA	←3 bytes→	
E0	BC		
E1	TIO	OP | Q | D2	+XR2
E2	LA	←3 bytes→	
F0	HPL		
F1	APL		
F2	JC	OP | Q | R	
F3	SIO	←3 bytes→	

LOAD & STORE REGISTER Q CODES

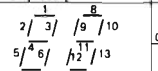


01	=	0000 0001	=	XR1
02	=	0000 0010	=	XR2
04	=	0000 0100	=	PSR
08	=	0000 1000	=	ARR
10	=	0001 0000	=	IAR
20	=	0010 0000	=	P1 - IAR
40	=	0100 0000	=	P2 - IAR
80	=	1000 0000	=	IAR - 0
C0	=	1100 0000	=	IAR - 1
A0	=	1010 0000	=	IAR - 2
90	=	1001 0000	=	IAR - 3
88	=	1000 1000	=	IAR - 4

LOAD I/O (LIO) INSTRUCTION FORMATS

Op Code	O Code			Operand 1	
0 7	DA 8 11	M 12	N 13 15	16	
31					Direct addressing – Operand 1 = 2 bytes
71					Indexed by XR-1 – Operand 1 = 1 byte
81					Indexed by XR-2 – Operand 1 = 1 byte
	1110				Device address line printer (E)
		0			M-bit is not used, a zero is preferred
5203 Printer			000		Load form length. One byte for each carriage
			100		Select line printer image address register
			110		Select line printer data address register
					Note: All other N codes invalid
	1111				Device address MFCU (F)
		0			Normal mode
5424 MFCU		1			Diagnostic mode
			100		MFCU print address register
			101		MFCU read address register
			110		MFCU punch address register
					Note: All other N codes invalid
	1010				Device address disk drive 1 (A)
5444 Disk	1011				Device address disk drive 2 (B)
		0			M-bit not used
			011		Diagnostic CE
			100		DFDR
			110		DFCR
					Note: All other N codes invalid
	0001				Device address keyboard (1)
		0	000		M and N must be zero

5475 Keyboard



Data at operand Address-1									Data at operand 1 Address								
0	1	2	3	4	5	6	7		0	1	2	3	4	5	6	7	
								Prog 1 ID									Prog 2 ID
1	2	3	4	5	6	7			8	9	10	11	12	13	14		
Indicator 1									Indicator 2								

LOAD I/O (LIO) INSTRUCTION FORMATS (continued)

Op Code	O Code			Operand 1	
	DA	M	N		
0 7	8 11	12	13 16	16	
31					Direct addressing—Operand 1 = 2 bytes
71					Indexed by XR-1—Operand 1 = 1 byte
B1					Indexed by XR-2—Operand 1 = 1 byte
SIOC	0011				Device address SIOC (3)
		0			Must be zero
			001		Load I/O function register
			010		Load SIOC length count register
			100		Load SIOC data address register
			101		Load data transfer register
					Note: All other N codes invalid.
5471 Printer Keyboard	0001				Device address printer keyboard (1)
		1			Select printer must be a 1, 0 is invalid.
			000		Load EBCDIC character to be printed (N code must be zero)
					Storage address can be one byte or two bytes in length (direct addressed, or indexed). The character to be printed is loaded from the first operand address + 1. All other N codes invalid.
BSCA	1000				Device address BSCA (8)
		0			Must be zero
			001		Stop address register
			010		Transition address register
			100		Current address register
			110		Current address register (not subject to busy)
					Note: All other N codes invalid.
1442	0101				Device address 1442 (5)
		0			Must be zero
			000		Load punch LCR
			100		Load 1442 DAR
					Note: All other N codes invalid

START I/O (SIO) INSTRUCTION FORMATS

Op Code	Q Code				Control Code		
	DA	M	N				
0 7	8 11	12	13 15		16 23		
F3							
5203 Printer	1110						Device address printer (E)
		0					Left carriage is used (single feed carriage)
		1					Right carriage is used
			000				Space only
			001				Invalid
			010				Print followed by spacing
			011				Invalid
			100				Skip only
			101				Invalid
			110				Print followed by skip
			111				Invalid
					0000	0000	No space
					0000	0001	One space
					0000	0010	Double space
					0000	0011	Triple space
					0000	0001	Skip to line 1
					0000	0010	Skip to line 2
					0110	1111	Skip to line 110
					0111	0000	Skip to line 112
							A number greater than 3 is not permitted and will result in a space zero operation.
							A number greater than /00F0/ may result in a carriage runaway. 112 lines are the maximum length of a form (8 lines per inch).
5424 MFCU	1111						Device Address MFCU (F)
		0					Primary card path is used
		1					Secondary card path is used
			000				Feed
			001				Read
			010				Punch feed
			011				Punch read
			100				Print feed
			101				Print read
			110				Punch print feed
			111				Punch print read
					0		Printbuffer 1 is used
					1		Printbuffer 2 is used
					1		8 bit IPL read
					1		Print 4 lines
					x		Reserved
						x	Reserved
						000	No selection
						100	Select stacker 4
						101	Select stacker 1
						110	Select stacker 2
						111	Select stacker 3
5475 Keyboard	0001	0	0000				Device Address Keyboard, M and N must be zero
					1		Program numeric shift
					1		Program lower shift
					1		Turn error indicator on
						1	Restore key
						1	Unlock keyboard
						0	Disable interrupt
						1	Enable interrupt
						1	Turn off interrupt request

START I/O (SIO) INSTRUCTION FORMATS (continued)

Op Code	Q Code			Control Code		
	DA	M	N			
0 7	8 11	12	13 15	16	23	
F3						
	1000					Device address BSCA (8)
		0				Must be zero
			000			Control
			001			Receive
			010			Transmit and receive
			011			Receive initial
			100			Auto call
			101			Invalid
			110			Loop test
			111			Invalid
				1xxx	x	If a 1, bits 1, 2, 3, and 4 of control code are effective
BSCA				0xxx	x	If a 0, bits 1, 2, 3, and 4 of control code are disregarded
				1		Enable BSCA
				0		Disable BSCA
				1		Enable test mode
				0		Disable test mode
				1		Enable step mode
				0		Disable step mode
					x	Spare (no effect)
					1	Start two second timeout
					0	Cancel two second timeout
					1	Enable interrupt
					0	Disable interrupt
					1	Reset interrupt request
					0	No action
						Note: The control code is effective with every "N" code function except that the start two second timeout must be used only with the control function ("N" = 000).
	0001					Device address - printer keyboard - (1)
		0				Select keyboard
			000			Must be zero – All other N codes invalid
				00xx	0xxx	Zero indicates unused position - Must be zero
				1		Turn on request pending indicator
				0		Turn off request pending indicator
				1		Turn on proceed indicator
				0		Turn off proceed indicator
5471					1	Enable request key interrupts
Printer					0	Disable request key interrupts
Key-					1	Enable data key interrupts
board					0	Disable data key interrupts
					1	Reset request or data key interrupts
		1				Select printer
			000			Must be zero – All other N codes invalid
				1		Start print
				0		Don't print
				1		Start carrier return (and index)
				0		Don't carrier return
				1		Force a printer feedback switch response
				1		Force a printer long function switch response
					0	Not used - Must be zero
					1	Enable printer interrupt
					0	Disable printer interrupt
					1	Degate printer magnets
					1	Reset printer interrupt

START I/O (SIO) INSTRUCTION FORMATS (continued)

Op Code	Q Code			Control Code			
	DA	M	N				
0 7	8 11	12	13 15	16		23	
F3							
	1010						Device address disk drive 1 (A)
	1011						Device address disk drive 2 (B)
		0					Removable disk
5444 Disk		1					Fixed disk
			000	0000	0000		Control - Seek
			001	0000	0000		Read - Data
			001	0000	0001		Read - Identifier
			001	0000	0010		Read - Diagnostic
			001	0000	0011		Read - Verify
			010	0000	0000		Write - Data
			010	0000	0001		Write - Identifier
			011	0000	0000		Scan - Equal
			011	0000	0001		Scan - Low or equal
			011	0000	0010		Scan - High or equal
							Note: 1. Bits 16-21 are not used by the attachment 2. All other N codes invalid.
	0011						Device address SIOC (3)
		0					Not used - A zero is preferred
			000	0000	0001		Reset interrupt request
			000	0000	0010		Enable interrupt ability
			000	0000	0100		Reset interrupt ability
			000	0000	1000		Remove SIOC from busy state
			000	0001	0000		Set interrupt request
			001	0000	0000		Read I/O device
			010	0000	0000		Write I/O device
SIOC			011				I/O Control 1
				1			I/O Select 8
				1			I/O Select 7
				1			I/O Select 6
				1			I/O Select 5
					1		I/O Select 4
					1		I/O Select 3
					1		I/O Select 2
					1		I/O Select 1
			100				I/O Control 2
				1			I/O Select 14
				1			I/O Select 13
				1			I/O Select 12
				1			I/O Select 11
					1		I/O Select 10
					1		I/O Select 9
					1		I/O Unit 2 Select
					1		I/O Unit 1 Select
	0000	0	000				Device address DPF M and N must be zero
				0000	0		Not used
					1		Enable dual programming mode
DPF					0		Disable dual programming mode
					1		Enable interrupt level 0 (system control panel interrupt key
					0		Disable interrupt level 0
					1		Reset interrupt request 0
	0101						Device address - 1442 RPQ (5)
		0					Must be zero
			000				Feed
			001				Read translate mode
1442			010				Punch and feed
			011				Read C1 mode
			100				Punch - No feed
				xxxx	x001		Note: All other N codes invalid. Select stacker 2. x indicates "don't care" bits. Any other control code combination than 001 is invalid and will result in the card going to stacker 1.

These control codes may also be used with N codes 001 or 010 below

All other N codes invalid.

All other N codes invalid.

SENSE (SNS) INSTRUCTION FORMATS

1442 SENSE (SNS)

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR 1	Byte 2 = Operand 1 address-1	
80				Operand 1 = 1 byte Indexed by XR 2		
	0101			Device address 1442 (5)		
		0		Must be zero		
				Low Core Address	High Core Address	
			011	Byte 2 (EB2)	Byte 1 (EB1)	
				0 Not assigned	0 Read compare	
				1 Not assigned	1 Last card indicator	
				2 Not assigned	2 Punch check	
				3 Read station jam	3 Data overrun	
				4 Hopper misfeed	4 I/O attention	
				5 Feed clutch	5 No-op latch	
				6 Punch station jam	6 Feed check	
				7 Transport jam	7 Invalid card code	
			001	0 Not assigned	0 All cells on	
				1 Not assigned	1 Read cells 7, 8, 9	
				2 Not assigned	2 Read cells 4, 5, 6	
				3 Punch incremental drive CB A	3 Read cells 1, 2, 3	
				4 Punch CB 2	4 Read cells 12, 11, 0	
				5 Punch CB 1	5 Read emitter	
				6 Punch incremental drive CB B	6 Feed CB 2, 3, 4	
				7 CE diagnostic bit 1	7 Feed CB 1	
			010	0 Punch echo 9	0 Punch echo 1	
				1 Punch echo 8	1 Punch echo 0	
				2 Punch echo 7	2 Punch echo 11	
				3 Punch echo 6	3 Punch echo 12	
				4 Punch echo 5	4 Punch echo valid	
				5 Punch echo 4	5 Not assigned	
				6 Punch echo 3	6 Punch cell dark	
				7 Punch echo 2	7 CE diagnostic bit 2	
			100	Store 1442 DAR		
			*	xxxx xxxx	Operand address (sense bytes destinations)	

* Note: All other N codes invalid

SENSE (SNS) INSTRUCTION FORMATS (continued)

6203 PRINTER SENSE (SNS)

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12	13 15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
B0				Operand 1 = 1 byte Indexed by XR-2		
	1110			Device address printer (E)		
		0		Must be zero		
					Low Core Address	High Core Address
			000		Byte 2 (EB2)	Byte 1 (EB1)
					0 Left carriage line location 7	0 Right carriage line location 7
			001		0 Binary amount to be added or subtracted to the line printer data address register (LPDAR) 7	0 Not printing - contains character in chain counter equal to character at print position 1. Printing - contains character in chain counter indicating character at position being addressed. 7
			010		0 Left or right carriage emitter 1 Execute print latch 2 Chain emitter SS 3 PSS 1 4 Print time 5 CE sense bit latched 6 HMR unit at extreme left (M1) 7 Home gate	0 Hammer shift clutch 1 Print start SS - emitter pulse 2 Left or right carriage clutch 3 Print cycle 1 4 Print cycle 2 5 Print cycle 3 6 Hammer set latch 7 Hammer bar right
			011		0 Carriage sync check 1 Carriage space check 2 Forms jam check 3 Incrementer failure check 4 CE sense bit latched 5 Hammer echo check 6 Any hammer on check 7 No op	0 Chain sync check 1 Incrementer sync check 2 Hammer unit thermal check 3 Not used 4 5 48 character chain installed 6 Unprintable character 7 CE sense bit
			100		0 LPIAR - Hi 7	0 LPIAR - Lo 7
			101		Invalid	
			110		0 LPDAR - Hi 7	0 LPDAR - Lo 7
			111		Invalid	
				xxxx xxxx	Operand address (sense bytes destinations)	

SENSE (SNS) INSTRUCTION FORMATS (continued)

5410 CPU SENSE (SNS)

Op Code	Q Code			Operand 1		
	DA	M	N			
0 7	8 11	12 13	15	16		
30				Operand 1 = 2 bytes Direct addressing		Byte 1 = Operand 1 address
70				Operand 1 = 1 byte Indexed by XR-1		Byte 2 = Operand 1 address-1
B0				Operand 1 = 1 byte Indexed by XR-2		
	0000			Device address CPU (0)		
		0		Must be zero		
				Low Core Address Byte 2 (EB2)	High Core Address Byte 1 (EB1)	
			000	0 1 2 3 Address switch 1	0 1 2 3 Address switch 3	
			*	4 5 6 7 Address switch 2	4 5 6 7 Address switch 4	
				xxxx xxxx	Operand address (sense bytes destinations)	

* Note: All other N codes invalid

SENSE (SNS) INSTRUCTION FORMATS (continued)

5424 MFCU SENSE (SNS)

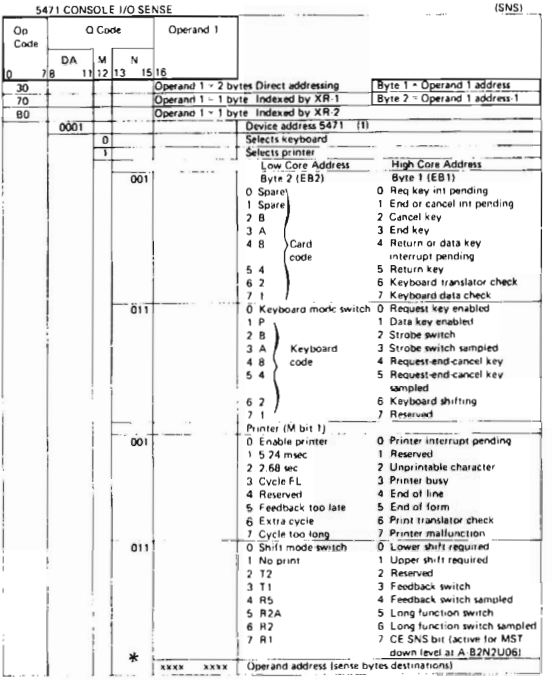
Op Code	O Code				Operand 1		
	DA	M	N				
0 7	8 11	12	13 15	16			
30					Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70					Operand 1 = 1 byte Indexed by XR-1	Byte 2 = Operand 1 address-1	
80					Operand 1 = 1 byte Indexed by XR-2		
	1111				Device address for MFCU (F)		
		0			Must be zero		
						Low Core Address	High Core Address
			000			Byte 2 (EB2)	Byte 1 (EB1)
						0 Punch CB	0 Hopper 1 or 2 magnet
						1 Punch strobe	1 Hopper cell covered
						2 Punch magnet one	2 Gear count 1, 3, 5, 7, 9, 11
						3 Ind 1 Byte 2 bit 3 (spare)	3 Read cell one exposed
						4 Print time	4 Read cell 18 exposed
						5 Print fire CB	5 Allow read
						6 Print magnet 1 (A1) 9(A2)	6 Hopper CB
						7 Ind 1 Byte 2 bit 7 (spare)	7 Ind 1 Byte 1 bit 7 (spare)
			001			0 Corner kick magnet	0 Punch registration roll 1 or 2
						1 Print stepper clutch magnet	1 Prepunch cell covered
						2 Post-print cell covered	2 Punch gate magnet
						3 Print inject CB	3 Punch eject roll magnet
						4 Print kick CB	4 Punch stepper roll magnet
						5 Print stepped CB	5 Corner cell covered
						6 Print allow, punch execute	6 Punch stepper CB
						7 Ind 2 Byte 2 bit 7 (spare)	7 Ind 2 Byte 1 bit 7 (spare)
			011			0 Print buffer 1 busy	0 Read check
						1 Print buffer 2 busy	1 Punch check
						2 Card in wait 1	2 Punch invalid
						3 Card in wait 2	3 Print data check
						4 Reserved	4 Print clutch check
						5 Hopper cycle not complete	5 Hopper check
						6 Card in transport counter bit 2	6 Feed check
						7 Card in transport counter bit 1	7 No op
			010		Invalid		
			100		MFCU print address register	Stores register	
			101		MFCU read address register	Contents at	
			110		MFCU punch address register	operand address 1 and	
			111		Invalid	operand address 1 minus one.	
				xxxx xxxx	Operand address (sense bytes destination)		

SENSE (SNS) INSTRUCTION FORMATS (continued)

5444 FILE SENSE (SNS)

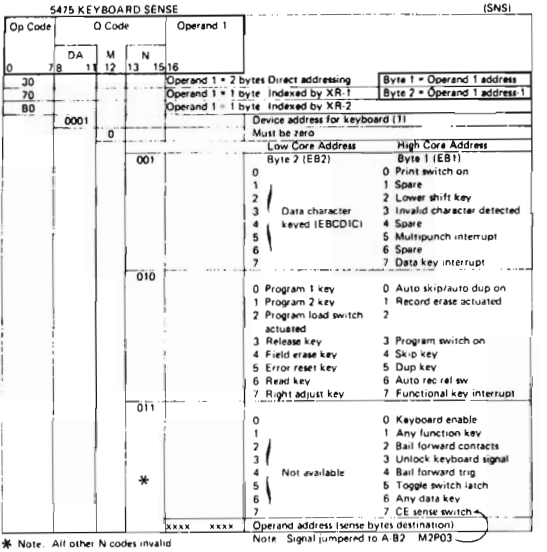
Op Code	Q Code				Operand 1		
0 7	DA 8 11	M 12	N 13 15	16			
30					Operand 1 = 2 bytes	Direct addressing	Byte 1 = Operand 1 address
70					Operand 1 = 1 byte	Indexed by XR-1	Byte 2 = Operand 1 address-1
80					Operand 1 = 1 byte	Indexed by XR-2	
	1010				Device address disk drive 1 (A)		
	1011				Device address disk drive 2 (B)		
		0			Removable disk		
		1			Fixed disk		
					Low Core Address		High Core Address
					Byte 2 (EB2)		Byte 1 (EB1)
			000		Invalid		
			001		Invalid		
			010		0 No op		0 Scan equal hit
					1 Invervention required		1 Cylinder zero
					2 Missing address marker		2 End of cylinder
					3 Equipment check		3 Seek busy
					4 Data check		4 100 cylinder
					5 No record found		5 Overrun
					6 Track condition check		6 Reserved
					7 Seek check		7 Disk drive 2 sel
			011		0 Unsafe		0 Reserved
					1 TAP line A		1 Jumperable CE bit
					2 TAP line B		2 Jumperable CE bit
					3 TAP line C		3 Not bit ring inhibit
					4 Index		4 Standard write trigger
					5 Head settling		5 Condition priority request
					6 Jumperable CE bit		6 Bit ring 0
					7 Reserved		7 Not CC reg position 17
			100		DFDR		
			101		Invalid		
			110		DFCR		
			111		Invalid		
				xxxx xxxx	Operand address (sense bytes destination)		

SENSE (SNS) INSTRUCTION FORMATS (continued)



* Note: All other N codes invalid

SENSE (SNS) INSTRUCTION FORMATS (continued)



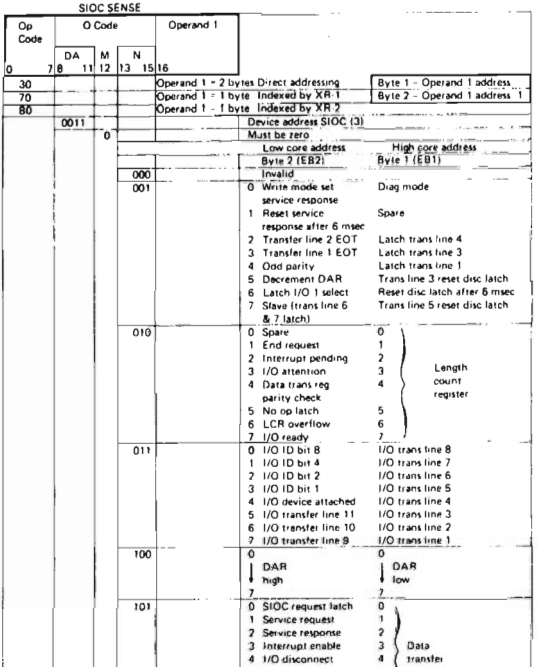
* Note: All other N codes invalid

SENSE (SNS) INSTRUCTION FORMATS (continued)

BSCA SENSE

Op Code	O Code			Operand 1		
	DA	M	N			
0 7	8 11	12 13	15	16		
30				Operand 1 = 2 bytes Direct addressing	Byte 1 = Operand 1 address	
70				Operand 1 = 1 byte Indexed by XR 1	Byte 2 = Operand 1 address+1	
80				Operand 1 = 1 byte Indexed by XR 2		
	1000			Device address BSCA (B)		
		0		Must be zero		
					Low core address Byte 2 (EB2)	High core address Byte 1 (EB1)
		000		0 Reserved	0 Reserved	
				1 Bit time counter 4	1 Reserved	
				2 Bit time counter 2	2 Reserved	
				3 Bit time counter 1	3 Reserved	
				4 Reserved	4 Block cycle steal request (ITB, BCC or VRC check)	
				5 Transmit trigger	5 LSR/shift reg parity check	
				6 Receive trigger	6 I/O cycle steal overrun	
				7 CE SNS bit	7 DB) parity check	
		001		Stop address register		
		010		Transition address register		
		011		0 Timeout	0 Reserved	
				1 CRC/LRC/VRC	1 Reserved	
				2 Adapter check on transmit	2 Reserved	
				3 Adapter check on receive	3 Reserved	
				4 Invalid ASCII character	4 Reserved	
				5 Abortive disconnect	5 Reserved	
				6 Disconnect timeout	6 Data set ready	
				7 Reserved	7 Data line occupied	
		100		Current address register		
		101		Invalid		
		110		0	0	
				1	1	
				2	2	
				3 CRC high (zeros for ASCII)	3 CRC low (LRC for ASCII)	
				4	4	
				5	5	
				6	6	
				7	7	
		111		Invalid		
			xxxx xxxx	Operand address (sense byte destination)		

SENSE (SNS) INSTRUCTION FORMATS (continued)



TEST I/O AND BRANCH (TIO) INSTRUCTION FORMATS

Op Code	O Code			Control Code		
0 7	DA 8 11	M 12	N 13 15	16		
C1						Direct addressing – Operand 1 = 2 bytes
D1						Indexed by XR-1 – Operand 1 = 1 byte
E1						Indexed by XR-2 – Operand 1 = 1 byte
	1111					Device address MFCU (F)
		0				Primary
		1				Secondary
5424 MFCU			000			Feed not ready or error
			001			Read feed busy (condition 1)
			010			Punch data busy (condition 2)
			011			Condition 1 or 2
			100			Print data busy (condition 4)
			101			Condition 1 or 4
			110			Condition 2 or 4
			111			Condition 1, 2 or 4
				xxxx	xxxx	Branch to address if condition met Op codes D1 and E1 are indexed
	1110					Device address printer (E)
		0				Left carriage
		1				Right carriage
5203 Printer			000			Not ready
			001			Invalid
			010			Print buffer busy
			011			Invalid
			100			Carriage busy
			101			Invalid
			110			Printer busy
			111			Invalid
				xxxx	xxxx	Branch to address if condition met Op codes D1 and E1 are indexed
5471 and 5475	0001					Device address keyboard (1)
						Test I/O is invalid and will result in invalid O byte processor check.
	1010					Device address disk drive 1 (A)
	1011					Device address disk drive 2 (B)
		0				Removable disk
		1				Fixed disk
5444 Disk			000			Not ready or error*
			010			Busy - Data transfer in process
			100			Scan found
			*			*Condition may vary depending on Disk drive selected - Refer to status byte
				xxxx	xxxx	Branch to address if condition is met
	0000					Device address DPF (0)
		0				Must be zero
DPF			0xx			Program level 1
			1xx			Program level 2
			x00			Cancel program level
			x01			Load program level from MFCU
			x10			Load from console I/O
			*	xxxx	xxxx	Branch to address if condition is met Op codes D1 and E1 are indexed

Tests setting of DPF switch

* Note: All other N codes invalid

TEST I/O AND BRANCH (TIO) INSTRUCTION FORMATS (continued)

Op Code	Q Code			Control Code	
	DA	M	N		
0 7 8 11 12 13 15 16					
C1					Direct Addressing – Operand 1 = 2 bytes
D1					Indexed by XR-1 – Operand 1 = 1 byte
E1					Indexed by SR-2 – Operand 1 = 1 byte
	0011				Device address SIOC (3)
		0			Must be zero
			000		Test for SIOC not ready
			010		Test for SIOC busy Note: All other N codes invalid
				xxxx xxxx	Branch to address if condition is met D1 and E1 are indexed
	1000				Device address BSCA (8)
		0			Must be zero
			000		Not ready / Unit check
			001		Op end interrupt
			010		Busy
BSCA			011		ITB interrupt
			100		Interrupt pending
			101		Invalid
			110		New data
			111		Invalid
				xxxx xxxx	Branch to address if condition is met D1 and E1 are indexed
	0101				Device address 1442 (5)
		0			Must be zero
			000		Test for 1442 not ready
1442			010		Test for 1442 busy Note: All other N codes invalid
				xxxx xxxx	Branch to address if condition is met D1 and E1 are indexed

CONDITION REGISTER SETTINGS

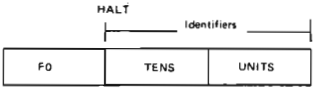
Binary Value	8	4	2	1	8	4	2	1
Bits	0	1	2	3	4	5	6	7
Meaning			*B0	Test False	**D0	HI	LO	EQ
DECIMAL								
ADD Decimal			–	–	overflow	> zero	< zero	zero
SUB Decimal			–	–	overflow	> zero	< zero	zero
ZERO & ADD			–	–		> zero	< zero	zero
LOGICAL								
ADD Logical			overflow	–	–	Carry	No Carry	zero
SUB Logical			–	–	–	1>2	1<2	zero
COMPARE			–	–	–	1>2	1<2	EQ
CLI						1>I	1<I	1 = I
EDIT (second operand)			–	–	–	> zero	< zero	zero
Test Bits ON			–	Note 1	–	–	–	–
Test Bits OFF			–	Note 2	–	–	–	–
BRANCH ON CONDITION	X		–	Note 3	–	–	–	–

When ONE, branch if any of the tested bits are ON
When ZERO, branch when all the tested bits are OFF

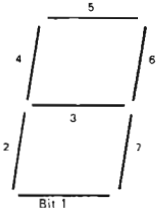
*B0 = Binary overflow
**D0 = Decimal overflow

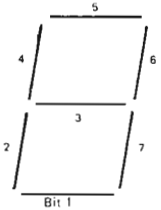
1. Selected bits are not all one.
2. Selected bits are not all zero
3. Turn off if tested.

HALT IDENTIFIERS



Hex Value	Character Displayed
00 Blank	
02 Quote	1
03	1
07	7
1B	4
10 Dash	—
3B	H
3C	L
3E	P
3F	R
57	3
5D	S
5F	g
63	J
68	L
6B	n
6C	L
6F	o
76	H
7C	L
7D	S
7F	R





EXAMPLE:

F0	7C	63

DISPLAYS

Note: Not the same as 5475 keyboard indicators - See 5475 LIO.

MACHINE INSTRUCTION DESCRIPTION

ZAZ = 1. Second operand placed byte by byte into first operand
2. High order zeros inserted
3. Zone bits except rightmost set to ones
4. Operands addressed by rightmost byte
5. Q byte designates length of both operands

AZ = 1. Second operand added algebraically to first operand
2. Operands addressed by rightmost bytes
3. Zone bits except rightmost set to ones
4. Q byte specifies length of both operands
5. Second operand remains unchanged unless overlapped
6. No check is made for valid digits in operands

SZ = 1. Operand 2 subtracted algebraically from Op 1 byte by byte; result in Op 1
2. Operands addressed by rightmost byte
3. Q byte specifies length of operands
4. No check for valid decimal digits

ALC = 1. Positive binary number in Op 2 is added byte by byte to positive binary number in operand 1; result stored in Op 1
2. Q byte specifies length of operands
3. Operand 2 not changed unless it overlaps operand 1

SLC = 1. Positive binary number in operand 2 subtracted from positive binary number in operand 1; result stored in operand 1
2. Result can never be negative
3. Q byte specifies length of operands
4. Both operands must be same length
5. Second operand not changed unless overlap

A = 1. Positive binary number contained in operand address added to register selected by Q code
2. Result replaces contents of register
3. Operand addressed by rightmost byte
4. If Bit 0 of Q code is zero, remaining bits cause modification of registers as follows:

Bits
1 = PL2 IAR
2 = PL1 IAR
3 = IAR in use when "A" instruction is executed
4 = ARR
5 = Prog Status Reg
6 = IX2
7 = IX1

5. If high order byte is 1, alter 5 interrupt level IAR

Bit
None = IL0
1 = IL1
2 = IL2
3 = IL3
4 = IL4

Note: Must not be used to add to more than one register at a time

MACHINE INSTRUCTION DESCRIPTION (continued)

MVX = 1. Numeric portion or zone portion of single byte second operand is placed in corresponding portion of first operand
2. Q byte specifies portion of each operand
00 = Z to Z
01 = N to Z
02 = Z to N
03 = N to N
3. Condition register not affected

MVC = 1. Second operand placed byte by byte in first operand location
2. Operands addressed by rightmost byte
3. Q byte specifies length of operation
4. Does not affect condition register

ED = 1. Decimal numeric characters in operand replace bytes containing 20 in first operand
2. Operands addressed by rightmost byte
3. Q byte specifies length of Op 1

ITC = 1. Single character at second operand address replaces all the characters in the first operand to the first significant digit
2. First operand addressed by *leftmost* byte that can contain a character that should be replaced
3. Q code contains length in bytes of operand 1

MVI = Data contained in Q byte moved to byte located at operand address

SBN = Byte of data contained in mask is used to set to one the corresponding bits in byte located at operand address

SBF = Byte of data set into Q byte is used to set to zero corresponding bits of the byte located at operand address

ST = Contents of register specified by Q code are placed in field addressed by operand address
Note: Not to be used for setting more than one register at a time

L = Contents of two byte field addressed by operand are placed in LSR specified by Q byte
Note: Not to be used for setting more than one register at a time

LA = 1. If instruction is D2 or E2, one byte operand is added to contents of index register specified by operand code and loaded into LSR specified by Q code
2. If instruction is C2, operand is loaded into register specified by Q byte

CLC = 1. First operand compared to second operand. Condition register is set
2. Operands addressed by rightmost byte
3. Q code specifies length of operands

CLI = Binary immediate operand contained in Q byte is compared with binary operand in storage location of operand address; result sets condition register; neither operand is changed

TBN = Bits of storage located at operand address are tested for bit = 1 as defined by mask contained in Q byte; storage operand is not changed

TBF = Bits of storage located at operand address are tested for bit = 0 as defined by mask contained in Q byte

BC = Condition register is tested under control of Q byte; if condition register satisfied condition tested for the next instruction is taken from the branch address

MACHINE INSTRUCTION DESCRIPTION (continued)

JC = Condition register is tested under control of Q code. If condition register satisfies condition tested for, the control code is added to the IAR and the sum becomes the address of the next instruction.

HPL = Prevents the execution of the next sequential instruction and displays a halt identifier which is controlled by the bytes in the halt identifier bytes

I/O

SIO = 1. No Op if unit check condition that prevents the execution of the SIO exists in addressed device
2. Is executed if it specifies the reset of an interrupt condition regardless of unit check condition
3. Resets any unit check condition that does not prevent execution of that SIO
4. If dual program feature is installed, an SIO instruction addressed to a device that is busy results in program level advance
5. On systems without dual programming, this condition results in a test for busy loop

SNS = Contents of data source specified by N portion of Q byte are placed in two byte field specified by operand address

LIO = 1. The contents of the two bytes addressed by the operand are transferred to the destination specified by the N code of the Q byte
2. A Q byte of 00 results in a No Op
3. With dual programming installed, a LIO to a busy device results in a program level advance

TIO = Condition specified by Q byte is tested in the addressed device if condition is present. Branch to address is transferred to IAR. If condition is not present, branch to address is transferred to ARR (no branch).

APL = 1. With dual program feature, the program level advances if condition specified by N code of Q byte is present.
2. If condition is not present, the instruction is No Oped.
3. If dual program feature is not installed, instruction acts loop if busy.

96 COL CARD CODE TO HEXADECIMAL CONVERSION TABLE

96 col card code to hexadecimal conversion table. Numeric bits across the top. Zone bits down the left side.

		1	2	21	4	4 1	42	421	8	8 1	8 2	8 21	84	84 1	842	8421	
	40	F1 1	F2 2	F3 3	F4 4	F5 5	F6 6	F7 7	F8 8	F9 9	7A :	7B #	7C @	7D '	7E =	7F "	GRAPHICS
A	F0 0	61 /	E2 S	E3 T	E4 U	E5 V	E6 W	E7 X	E8 Y	E9 Z	50 &	6B ,	6C %	6D _	6E >	6F ?	GRAPHICS
B	60 -	D1 J	D2 K	D3 L	D4 M	D5 N	D6 O	D7 P	D8 Q	D9 R	5A !	5B $	5C *	5D)	5E ;	5F ¬	GRAPHICS
C C A CB CBA	BA 00 B0 20 90	D0 J 81 21 91 81	C1 A B1 A1 91 81	C2 B B2 A2 92 82	C3 C B3 A3 93 83	C4 D B4 A4 94 84	C5 E B5 A5 95 85	C6 F B6 A6 96 86	C7 G B7 A7 97 87	C8 H B8 A8 98 88	C9 I 89 A9 99 89	4A ¢ 3A 10 1A 0A	4B . 3B 2B 1B 0B	4C < 3C 2C 1C 0C	4D (3D 2D 1D 0D	4E + 3E 2E 1E 0E	4F | 3F 2F 1F 0F	GRAPHICS
D D A D B D BA	C0 70 E0 6A	71 E1 51 41	72 62 52 42	73 63 53 43	74 64 54 44	75 65 55 45	76 66 56 46	77 67 57 47	78 68 58 48	79 69 59 49	FA EA DA CA	FB EB DB CB	FC EC DC CC	FD ED DD CD	FE EE DE CE	FF EF DF CF	
DC DC A DCB DCBA	90 30 A0 2A	31 A1 11 01	32 22 12 02	33 23 13 03	34 24 14 04	35 25 15 05	36 26 16 06	37 27 17 07	38 28 18 08	39 29 19 09	BA AA 9A 8A	BB AB 9B 8B	BC AC 9C 8C	BD AD 9D 8D	BE AE 9E 8E	BF AF 9F 8F	

CARD FORMATS

PTF Header

P (identifies a PTF header)	cc 1
Program Number	cc 2-12
Version/Modification Level of the component	cc 13-16
Component ID	cc 17
Unreferenced	cc 18-85
Self Check Number	cc 86 88
Unreferenced	cc 89-96

A. Header Card

Program Number	cc 20-30
Modification Level of Component	cc 31-32
Component Card Count	cc 55-58
Version of Component	cc 59-60
Module Card Count	cc 61-63
Header ID (C-Component or M-Module)	cc 64
*Update Type	cc 85
Self Check Number	cc 86-88
Module Modification Level	cc 89-90
Component ID	cc 91
Module ID	cc 92-93
Sequence Number (000)	cc 94-96

B. PTF Card

Unreferenced	cc 1-85
Self Check Number	cc 86-88
PTF ID (P)	cc 89
PTF Number	cc 90
Component ID	cc 91
Module ID	cc 92-93
Sequence Number	cc 94-96

C. Program

Unreferenced	cc 1-85
Self Check Number	cc 86-88
Module Modification Level	cc 89-90
Component ID	cc 91
Module ID	cc 92-93
Sequence Number (001-998)	cc 94-96

D. End Card

Unreferenced	cc 1-85
Self Check Number	cc 86-88
Module Modification Level	cc 89-90
Component ID	cc 91
Module ID	cc 92-93
Sequence Number (999)	cc 94-96

A. The header card is the first card of every module or component

*Update Type: 0 = changes to a module, and changes to modification levels.
1 = complete replacement of a module or addition of a complete new module, and changes to modification levels.
2 = changes to a module, but no change in modification levels.
3 = complete replacement of a module or addition of a complete new module, but no change in modification levels.

B. PTF cards are corrections to IBM System/3 programs.

C. A program card is any card that is not a PTF and has a sequence number between 001 and 998.

D. The end card is the last card of a module or component. It must have the sequence number 999.

BOOT STRAP FOR LOADER

Card 1

Moved to **Load I/O**

	0000	C2 01 0000	**LA**	XR1 = 0000
	0004	5C 0B FF2B	**MVC**	Relocate
	0008	5C 07 6733	**MVC**	I/O Inst.
	000C	3A 0F 017E	**SBN**	Core Size
	0010	D0 00 F4	**BC**	To I/O Inst.
00F4	0020	71 F5 FF	**LIO**	MRDAR = 0000
00F7	0023	F3 F1 40	**SIO**	IPL Mode
00FA	0026	F1 F1 00	**APL**	Reader Busy
00FD	0029	D0 00 00	**BC**	
0060	002C	F0 7C 60	**HPL**	Portion of
0063	002F	70 F3 5F	**SNS**	Loader
0066	0032	79 FF	**TBF**	

Card 2 Through 5

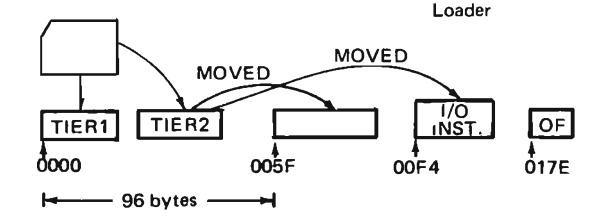
0000 5C L Address Address **MVC**
0004 5C L Address Address **MVC**

Locates each card in core

0008 D0 00 F4 **BC** to I/O instructions.

Card 6

0000	5C 05 E9 25	**MVC**	
0004	4C 00 D9 017E	**MVC**	For Size Check
0009	D0 00 6F	**BC**	To Start of Loader



First Card Logic

TEXT AND END CARD IN CORE

TEXT CARD in CORE "T"

0000	E3
0001 - 0016	INSIGNIFICANT BYTES
0017	Length of text data -1
0018 - 0019	Right most Address of text data
001A - 0058	Text data
0059 - 005F	Identification & Sequence

END CARD in CORE "E"

0000		C5		
0001 - 0016		INSIGNIFICANT BYTES		
	0017	00 00	Two byte address of program entry	
	0019	0C 17 0077 0044	MVC	
	001F	3C 40 00FF	MVI	
	0023	0C 86 00FE 00FF	MVC	
	0029	35 10 0018	L	(IAR)
0060	002D	F0 00 00	HPL	LSR Display Routine Instructions
0063	0030	F0 00 00	HPL	
0066	0033	30 00 006B	SNS	
006A	0037	30 00 0062	SNS	
006E	003B	0C 00 0064 0062	MVC	
0074	0041	C0 87 0060	BC	

LSR DISPLAY ROUTINE PROCEDURE

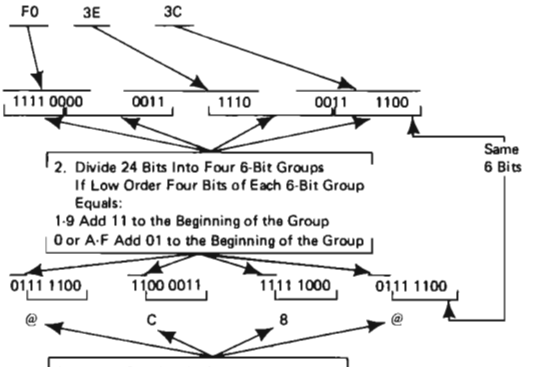
1. Set the IAR to X'66' for card; X'EB' for disk.
2. Set the console address/data switches as follows:
   a. The left two switches to 34 to store a register or to 30 to sense a register.
   b. The right two switches to the register to be displayed.
3. Press the START button. A halt condition is displayed on the console. The Q byte of the first halt is the high order byte of the register being displayed.

When the START button is pressed again, another halt condition occurs. The Q byte of the second halt is the low order byte of the register being displayed.

Another register can be displayed by changing the setting of the two rightmost console address/data switches and pressing the START button.

RPG II COMPRESSION

1. Original Data in Storage



Exceptions:

Original 6 Bits	New Char
11 00 00	11 11 00 00
10 00 01	01 10 00 01
10 10 10	11 01 00 00

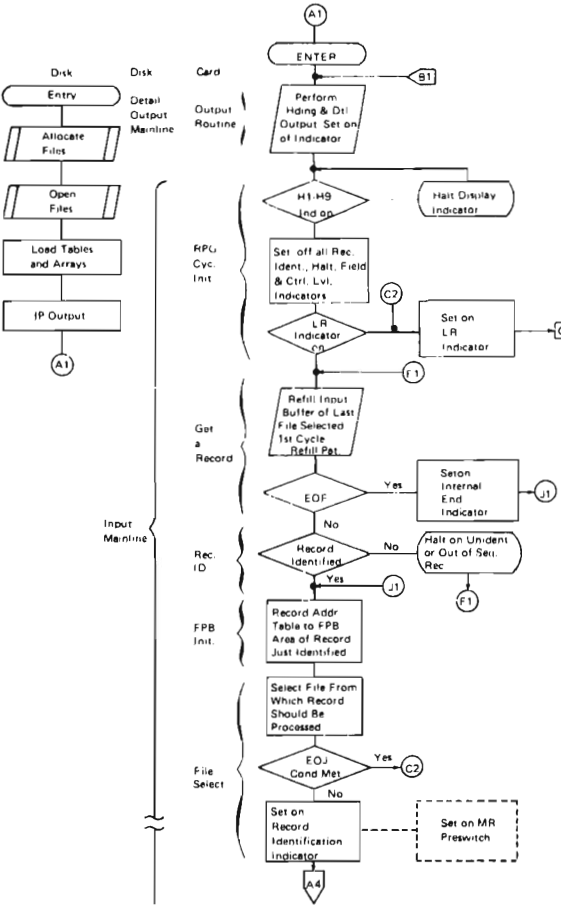
3. Compression is just the reverse. That is, remove the two high-order bits from each 8-bit group. You'll end up with the original 24 bits.

RPG INDICATOR SETTINGS

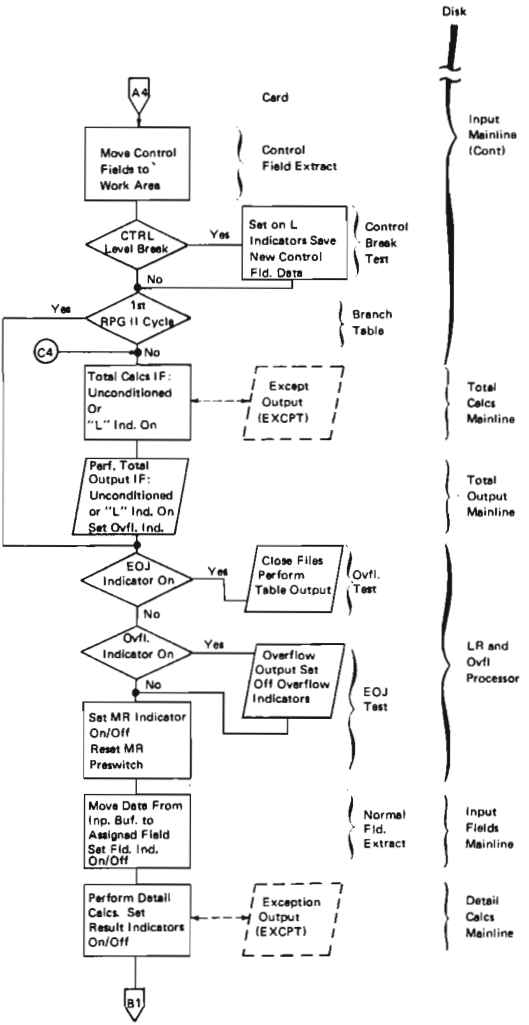
* Not Valid for Look Ahead Fields
** When Field Named Is Not Match or Control Field
*** Only for Detail or Heading Lines
**** Must Be Positive for Exception Line
***** Not Valid for Table Input Files

INDICATOR	FILE DESCRIPTION SPECIFICATION	INPUT SPECIFICATIONS			CALCULATION SPECIFICATION			OUTPUT FORMAT SPECIFICATION
	File Conditioning 71 - 72	Record * Identifying Indicator 19 - 20	Field * Record Relation 63 - 64	Field Indicator 65 - 70	Control Level Indicator 7 - 8	Conditioning Indicator 9 - 17	Resulting Indicator 54 - 59	Conditioning Indicator 23 - 31
01 - 99		X	X	X		X	X	X X
H1 - H9		X		X		X	X	X
1P								X***
MR			X*			X		X
OA-OG & OV						X	X	X****
L0					X			X
L1 - L9		X	X**		X	X	X	X
LR		X			X	X	X	X
U1 - U8	X*****		X			X		X

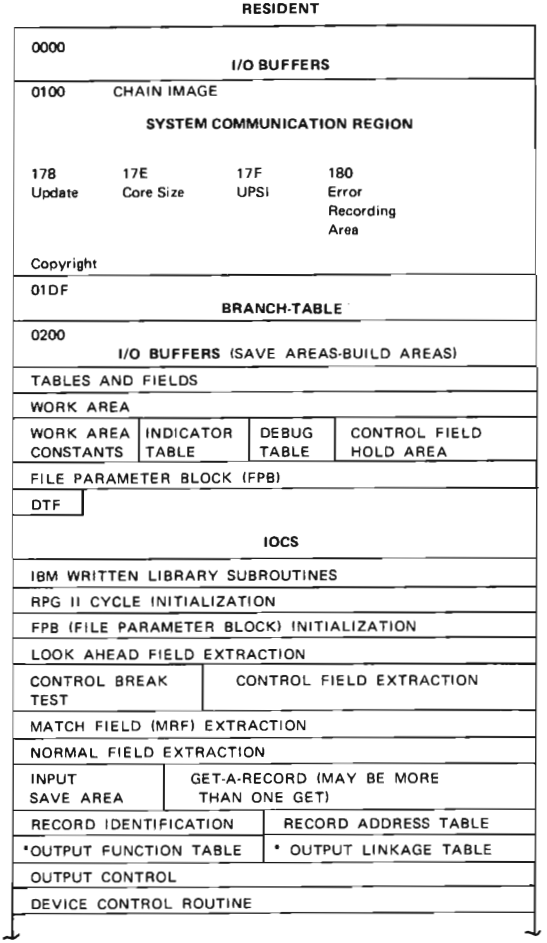
RPG II PROGRAM OBJECT CYCLE



RPG II PROGRAM OBJECT CYCLE (continued)



MAIN STORAGE DURING RPG II PROGRAM EXECUTIONS



* MAY BE SEVERAL WITH EACH GET

(Card Only)

MAIN STORAGE DURING RPG II PROGRAM EXECUTIONS

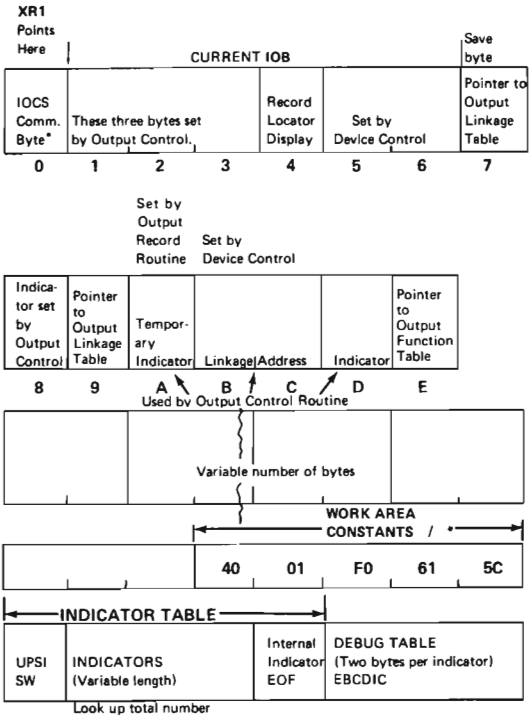
PRE-OVERLAY

BUILD FIRST PAGE OUTPUT RECORD
FIRST PAGE RECORD OUTPUT
PRE-OVERLAY INITIALIZATION
LOAD TABLES
OPEN FILES
EXECUTE OVERLAY
UNUSED
UNUSED

POST-OVERLAY

BUILD OUTPUT RECORD			
OVERFLOW TEST AND OVERFLOW OUTPUT RECORD			
EXCEPTION OUTPUT RECORD			
HEADING AND DETAIL OUTPUT RECORD			
TOTAL OUTPUT RECORD			
END OF JOB TEST		TABLE OUTPUT	
CURRENT PRIMARY	LAST PRIMARY	LAST SELECTED	CURRENT SELECTED
FPB MAIN HOLD AREA		FPB TEMP HOLD AREA	
FILE SELECTION (MULTIFILE LOGIC)			
DETAIL CALCS			
TOTAL CALCS			
USER WRITTEN LIBRARY SUBROUTINE			
POST-OVERLAY INITIALIZATION			

INDICATOR TABLE AND WORK AREA



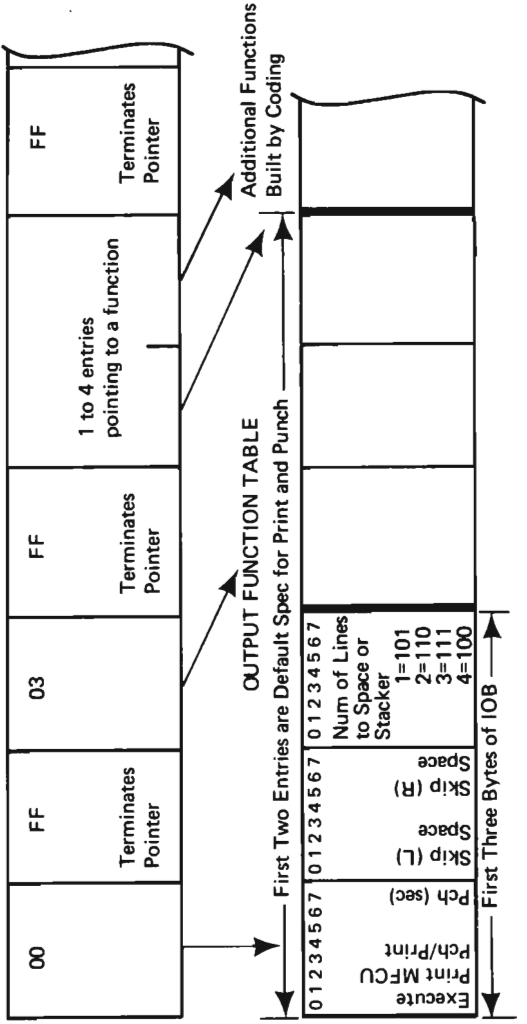
*Printer only 00 = overflow 01 = no overflow

PARAMETERS AND POINTERS

PARAMETER That Follows a Branch to the Indicator Set Routine
Variable Number of Indicators May Be Used

POINTER That Follows a Branch to IOCS

OUTPUT TABLES



(Card Only)

TABLE/ARRAY CONTROL BLOCK

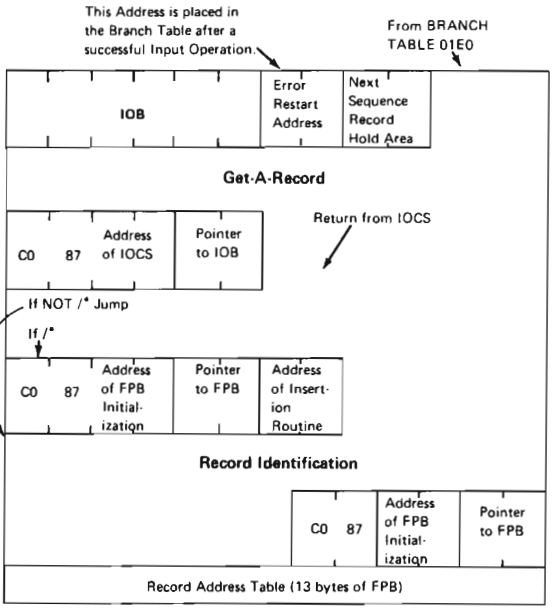
1	2	3	4	5	6	7	8
Address of First Element		Address of Last Element		Addr of Last Element Found (Table Only)		Length of One Element	

Control blocks are located after fields and before short literals. One control block per table or array in the same order as the tables and arrays were defined.

(Card Only)

BRANCH TABLE

INPUT PROGRAM BLOCK



FILE PARAMETER BLOCK

1	2	3	4
ADDRESS OF GET–A–RECORD		ADDRESS OF NEXT SEQUENTIAL RECORD HOLD AREA	

Only byte in FPB if record is /*

5	6	7	8	9	10	11	12	13	14	15	16	17
MATCH FIELD EXTRACTION		NORMAL FIELD EXTRACTION		CONTROL FIELD EXTRACTION		MASK–DISP. RECORD IDENT. INDICATOR		STACKER & SEQUENCE	NEXT SEQUENCED RECORD			SEQUENCE CONTROL BYTE ADDRESS

Not in the FPB if records are not sequence checked

The *Record Address Table* immediately follows the instructions which test record identification codes in the Record Identification Routine. The record address table is placed in file parameter block bytes 5 through 17.

ZONE	DIGIT
0000 = DEFAULT	0000 = UNSEQUENCED
0101 = 1	0001 = SEQUENCED
0110 = 2	0011 = N-MANDATORY
0111 = 3	
0100 = 4	

MFCU DTF AND IOB

Each branch to IOCS is followed by a two byte address that points to the IOB.

PRINTER DTF AND IOB

Each branch to IOCS is followed by a two byte address that points to the IOB (ending address).

1442 DTF AND IOB

IOB

1	2	3	4	5	6
0 1 2 3 4 5 6 7 Punch Read	Reserved	0 1 2 3 4 5 6 7 Stacker 1 1 0 1 2 1 1 0	Last used position in Record (Binary)	Points to Last Byte of DTF	

0 = Wait
1 = Execute

DTF

Bytes	Read/Punch No Feed	Read Column Binary	Read Only	Punch Only
1-2	Read Buffer Address			Punch Buffer Address
3-4	Punch Buffer Address	Q & R bytes on ERROR		
5-6	Q & R bytes on error	Status bytes on error		
7-8	Status bytes on error			

Term or Expression	Length Attribute
1. Name entry symbol of a machine-instruction	Length, in bytes, of the instruction.
2. Location-counter reference (*)	Length, in bytes, of the instruction in which it appears (except in the EQU assembler statement, where the length attribute assigned is one).
3. Expression	Length attribute of the leftmost term in the expression.
4. Self-Defining Term	Length attribute is one.

NOTE: See also the length subfield of data-definition statements, under Assembler Instruction Statements.

Operand Groups

Machine-instruction statement operands are divided into six groups. The characteristics of each group are as follows:

Group 1: Two-operand format in which a length is explicit or implied in both operands.

Group 2: Two-operand format in which a length can be explicit in either operand, but not in both. If a length is not explicit in either operand, the assembler uses the implied length of operand 1.

Group 3: Two-operand format in which a length cannot be specified.

Group 4: One-operand format in which only immediate data may be used.

Group 5: Two-operand format in which both operands are immediate data.

Group 6: Two-operand format in which operand 1 is used by the assembler to calculate a positive displacement and operand 2 is immediate data.

BASIC ASSEMBLER LANGUAGE (continued)

The following chart shows the allowable operand formats for each operand group. The instructions using each operand group are also listed.

For the extended mnemonics of the MVX instruction, the I-field information is inherent in the mnemonic and the I-field is omitted from the operand. For the extended mnemonics of the BC and JC instructions, the second operand (I-field) is not used, since the information is inherent in the mnemonic (see Extended Mnemonic Codes).

Data movement is from operand 2 to operand 1 in a two-address format instruction (group 1 and group 2). This operand order is equivalent to that of machine instructions.

In groups 3, 4, 5, and 6, the Q code operand is always on the right.

BASIC ASSEMBLER LANGUAGE (continued)

GROUP	INSTRUCTIONS	ALLOWABLE OPERAND FORMAT			
1	ZAZ,AZ,SZ	A,A A,A(L) A,D(,R) A,D(L,R)	A(L),A A(L),A(L) A(L),D(,R) A(L),D(L,R)	D(,R),A D(,R),A(L) D(,R),D(,R) D(,R),D(L,R)	D(L,R),A D(L,R),A(L) D(L,R),D(,R) D(L,R),D(L,R)
2	MVC,CLC,ALC SLC,ITC,ED	A,A A,A(L) A,D(,R) A,D(L,R)	A(L),A A(L),D(,R)	D(,R),A D(,R),A(L) D(,R),D(,R) D(,R),D(L,R)	D(L,R),A D(L,R),D(,R)
	MVX	A,A(I) A,D(I,R)	A(I),A A(I),D(,R)	D(,R),A(I) D(,R),D(I,R)	D(I,R),A D(I,R),D(,R)
3	MVI,CLI,SBN SBF,TBN,TBF TIO,SNS,LIO BC	A,I		D(,R),I	
	L,ST,A,LA	A,R		D(,R),R	
4	APL	I			
5	HPL,SIO	I,I			
6	JC	A,I			

The following codes are used to describe the possible operand formats

CODE	MEANING	ACCEPTABLE FORM
A	Address	Relocatable expression, absolute expression, or self-defining value.
D	Displacement	Relocatable expression, absolute expression, or self-defining value.
L	Length	Absolute expression or self-defining value.
R	Register	Absolute expression or self-defining value.
I	Immediate Data (bit masks, condition bit masks, or control bits to be used in the instruction)	Absolute expression or self-defining value.

BASIC ASSEMBLER LANGUAGE (continued)

EXTENDED MNEMONIC CODES:

Move Hex Character (MVX)

Move To Zone From Zone	MZZ
Move To Numeric From Zone	MNZ
Move To Zone From Numeric	MZN
Move To Numeric From Numeric	MNN

Branch On Condition (BC)

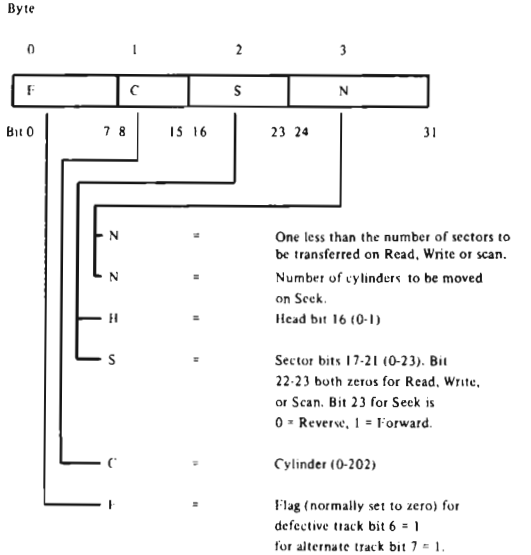
Branch	B
Branch High	BH
Branch Low	BL
Branch Equal	BE
Branch Not High	BNH
Branch Not Low	BNL
Branch Not Equal	BNE
Branch Overflow Zoned	BOZ
Branch Overflow Logical	BOL
Branch No Overflow Zoned	BNOZ
Branch No Overflow Logical	BNOL
Branch True	BT
Branch False	BF
Branch Plus	BP
Branch Minus	BM
Branch Zero	BZ
Branch Not Plus	BNP
Branch Not Minus	BNM
Branch Not Zero	BNZ

Jump On Condition (JC)

Jump	J
Jump High	JH
Jump Low	JL
Jump Equal	JE
Jump Not High	JNH
Jump Not Low	JNL
Jump Not Equal	JNE
Jump Overflow Zoned	JOZ
Jump Overflow Logical	JOL
Jump No Overflow Zoned	JNOZ
Jump No Overflow Logical	JNOL
Jump True	JT
Jump False	JF
Jump Plus	JP
Jump Minus	JM
Jump Zero	JZ
Jump Not Plus	JNP
Jump Not Minus	JNM
Jump Not Zero	JNZ

DISK FILE CONTROL REGISTER

The DFCR Disk File Control Register contains the two byte address of the four byte Disk Control Field in storage. The format of the four byte Disk Control Field in core is:



The Seek operation uses the S, and N bytes of the Disk Control Field.

DISK FILE DATA REGISTER

The DFDR keeps track of the memory address of the current data byte.

FILE ORGANIZATION AND PROCESSING

PRIMARY AND SECONDARY FILES				
FILE ORGANIZATION	METHODS OF PROCESSING	RECORD ARRANGEMENT	NEW ENTRIES	WHEN USED
INDEXED	1. By Addrout File 2. Sequentially by Key 3. Sequentially Within Limits	Records - Ordered Unordered Index - Always Ordered	Added at End of Last Record in File Update to Orig Loc	Low Activity (% of Entries Used Per Job) Random Selection High Volatility
DIRECT	1. Consecutively 2. By Addrout File		Added by Using Update to Act Loc	
SEQUENTIAL	1. Consecutively 2. By Addrout File	Ordered Unordered	Added at End of Last Record in File Update to Orig Loc	High Activity Consec Processing Low Volatility
CHAINED FILES				
INDEXED	1. Randomly by Key	Records - Ordered Unordered Index Always Ordered	Same	Same
DIRECT	1. Randomly by Relative Record Number		As	As
SEQUENTIAL	1. Randomly by Relative Record Number	Ordered Unordered	Above	Above

(Disk Only)

PROGRAM NAMES

Program	Name
Alternate Track Assignment	$ALT
Alternate Track Rebuild	$BUILD
List	$CLIST
Reproduce and Interpret	$REPRO
Disk Copy/Dump	$COPY
Disk Sort	$DSORT
File Delete	$DELET
File and Volume Label Display	$LABEL
Data Verifying	$DVER
Data Recording	$DREC
Disk Initialization	$INIT
Library Maintenance	$MAINT
MFCU Sort/Collate	$CSORT
RPG Compiler	$RPG

OCL STATEMENTS

File Parameters

- NAME-filename (in program)
- PACK-name
- UNIT-code
- LABEL-filename (on disk)
- DATE-date
- RETAIN-code
- RECORDS-number or TRACKS-number
- LOCATION-track number

The NAME, PACK, and UNIT parameters are always required. The others are required only under certain conditions.

NAME: The NAME parameter is always needed. It tells the system the name that your program uses to refer to the file. The NAME parameter must be placed on the first card or line if two or more cards (or lines) are used for the FILE statement.

If your program is an RPG II program, the filename assigned in the file description specifications for the program is the name you must use in the NAME parameter.

For some of the programs, you must use certain names for certain files.

Program	File	Name
Copy Disk	Input	COPYIN
	Output	COPYO
Disk Sort	Input	INPUT
	Work	WORK
	Output	OUTPUT

OCL STATEMENTS

STATEMENT	FUNCTION	PLACEMENT		RESTRICTION ON USE
		STATEMENT APPEARS IN JOB STREAM	STATEMENT APPEARS IN A PROCEDURE	
// DATE	Supplies the system with a date; this date is given to disk files being created	Must follow LOAD or CALL statement and precede the RUN statement except at IPL time where it must precede LOAD or CALL statement	Must follow the LOAD statement, precede RUN statement (if RUN is used)	Must be supplied at least once during the initial program loading time. If used after IPL time change is temporary
// LOAD*	Identifies the program to be run and indicates it was loaded from cards following the RUN statement	Must follow LOAD or CALL statement and precede the RUN statement	Must be the first statement	Cannot be used in program level 2
// LOAD	Identifies the program to be run and indicates the disk that contains the object library from which it is to be loaded			
// RUN	Indicates the end of the OCL statements for a program and tells system to run the program	Must be the last OCL statement	May be the last statement	Required for each program which is to be run, in the job stream
// SWITCH	Used to set one or more external indicators on or off	Must follow LOAD or CALL statement and precede the RUN statement	Must follow the LOAD statement and precede the RUN statement	
// COMPILE	Tells the system where the source program is located and where to place the object program	Must follow LOAD or CALL statement and precede the RUN statement	Must follow the LOAD statement and precede the RUN statement	

OCL STATEMENTS

STATEMENT	FUNCTION	PLACEMENT		RESTRICTIONS ON USE
		STATEMENT APPEARS IN JOB STREAM	STATEMENT APPEARS IN A PROCEDURE	
// HALT	Instructs system to halt when program ends, cancels the effect of the NOHALT statement	Anywhere	Must follow the LOAD statement and precede the RUN statement	
Comment Statement	Used to explain the job or give the operator instructions, does not affect the system	Anywhere	Anywhere	
// PAUSE	Tells the system to stop in order to give the operator extra time. Operator must restart	Anywhere	Must follow the LOAD statement and precede the RUN statement	
/&	Provides OCL security from previous job	Recommended as the first statement	Not allowed in a procedure	
// FILE	Supplies information about the file to the system	Must follow LOAD or CALL statement and precede the RUN statement	Must follow the LOAD statement and precede the RUN statement	Required for every new file created and old files being used
// CALL	Identifies procedure to be merged into job stream and the disk containing the procedure library from which to read it	Job stream only; must be followed by a RUN statement	Not allowed in a procedure	Can be used in the job stream only

STATEMENT	FUNCTION	PLACEMENT		RESTRICTIONS ON USE
		STATEMENT APPEARS IN JOB STREAM	STATEMENT APPEARS IN A PROCEDURE	
// IMAGE	Tells the system to replace the chain image area with characters indicated in the subsequent cards	Anywhere	Must follow the LOAD statement and precede the RUN statement	Required if the printer chain has been changed
// PARTITION	Tells the system the size of program level 2	Anywhere	Must follow the LOAD statement and precede the RUN statement	
// FORMS	Instructs the system to change the number of lines printed per page	Anywhere	Must follow the LOAD statement and precede the RUN statement	Will be ignored in DPF when other partition has device allocated
// LOG	Instructs system to start or stop printing OCL statements and codes and indicates the device to be used to print them	Anywhere	Must follow the LOAD statement and precede the RUN statement	In program level 2 device cannot be specified
// READER	Changes the system input device used to read OCL statements	Must follow the RUN statement and precede the LOAD or CALL statement or before initial LOAD or CALL statement	Not allowed in a procedure	Can be used in job stream only
// NOHALT	Instructs system to continue without stopping when a program ends	Anywhere	Must follow the LOAD statement and precede the RUN statement	

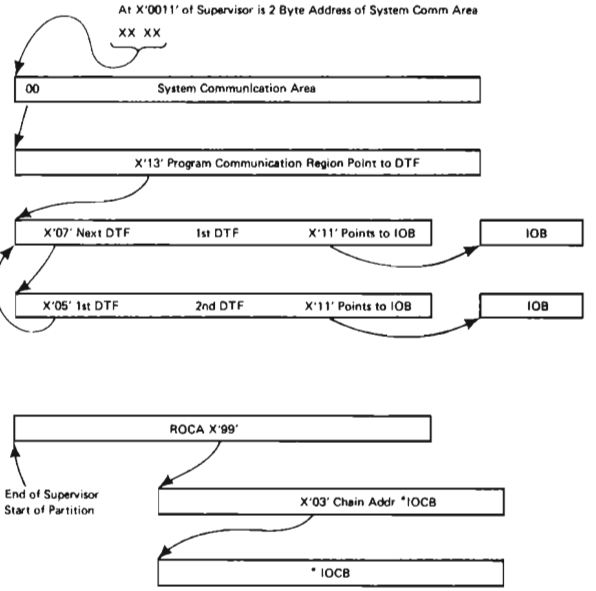
OCL STATEMENTS

STATEMENT	PARAMETER	CODE	MEANING
// DATE	date	MM/DD/YY or DD/MM/YY	System date or date within a set of statements
// LOAD	asterisk	*	Program is to be loaded from cards
	program name	name	Name of program that is to be loaded from disk
	unit		Object library resides upon:
		R1	Removable disk on drive one
		R2	Removable disk on drive two
		F1	Fixed disk on drive one
		F2	Fixed disk on drive two
// RUN	none		
// SWITCH	indicator	Refer to SWITCH Statement	
// COMPILE	SOURCE	SOURCE-name	Location of source program
	UNIT	UNIT-R1	Where disk that contains the
		R2	source library is located
		F1	(the meanings of the unit codes
		F2	are the same as for LOAD)
	OBJECT	OBJECT-R1	Where to place the object
		F1	program (the meanings of the
		R2	unit codes are the same as
		F2	for LOAD)
// IMAGE	format	HEX	To indicate characters from cards are in hexadecimal form
		CHAR	To indicate characters from cards are in EBCDIC form
		MEMBER	To indicate characters are from the source library
	number	value	Number of new characters
	name	name	Identifies the characters in the library
	unit	R1	Where the disk containing the
		R2	library is located (the meanings
		F1	of the unit codes are the same
		F2	as for LOAD)
// PARTITION	size	value	Minimum size of program level two

OCL STATEMENTS

STATEMENT	PARAMETER	CODE	MEANING
// FORMS	DEVICE	DEVICE-name	Indicates which carriage of the system printer is used
	LINES	LINES-value	Indicates number of lines to be printed per page
// LOG	device name	CONSOLE	Use printer/keyboard as logging device
		PRINTER	Use printer as logging device
		OFF	Stop printing
		ON	Start printing
// READER	input device	CONSOLE	Printer/keyboard
		MFCU2	Secondary hopper for MFCU
		MFCU1	Primary hopper for MFCU
		1442	Card read/punch
// NOHALT	none		
// HALT	none		
Comment	none		
// PAUSE	none		
/&	none		
// FILE	NAME	NAME-filename	Name the program uses to refer to the file
	PACK	PACK-name	Name of disk containing the file
	UNIT	UNIT-R1	Where the disk containing the file is located (The meanings of the unit codes are the same as for LOAD)
		R2	
		F1	
		F2	
	LABEL	LABEL-filename	Name by which your file is identified on disk
	DATE	DATE-MM/DD/YY	Tells the system date of file as created previously
		DD/MM/YY	
	RETAIN	RETAIN-T	Temporary file
		S	Scratch file
		P	Permanent file
		A	Access scratch file
	RECORDS or TRACKS	RECORDS-number or TRACKS-number	Amount of space needed on a disk for a file
	LOCATION	LOCATION-track number	Number of track on which a file begins

SYSTEM LINKAGE

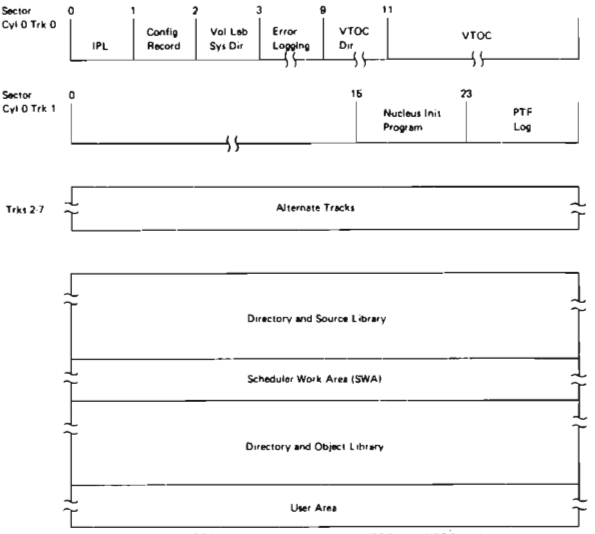


*Bytes 4 and 5 of each IOCB point to associated DTF.

SECTOR/TRACK ADDRESS TABLE

Sector No.	Track 0 (Even)	Sector No.	Track 1 (Odd)
0	00	24	80
1	04	25	84
2	08	26	88
3	0C	27	8C
4	10	28	90
5	14	29	94
6	18	30	98
7	1C	31	9C
8	20	32	A0
9	24	33	A4
10	28	34	A8
11	2C	35	AC
12	30	36	B0
13	34	37	B4
14	38	38	B8
15	3C	39	BC
16	40	40	C0
17	44	41	C4
18	48	42	C8
19	4C	43	CC
20	50	44	D0
21	54	45	D4
22	58	46	D8
23	5C	47	DC

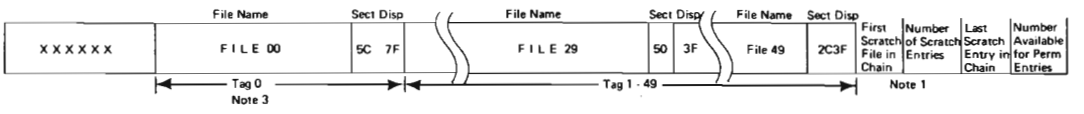
SYSRES LAYOUT



1. Data file retrieval is: VTOC pointer in system directory to VTOC dir to VTOC to file.
2. To get any library entry (object or source): System dir to library dir to library

VOLUME LABEL AND SYSTEM DIRECTORY

VTOC Directory



VTOC (File Labels - Format 1)

ID	Chain Addr	File Name	Date	RTN	File Type	Rec L	Key L	Key Loc	CSD Last Rec	CSD Last Key	CS Start Data	CS End Data	CS Start Index	CS End Index	No. of Rec or No. of TR Creation
0	1 2	3 4 5 6 7 8 9 10	11 12 13 14 15 16	17	18 19	20 21	22	23 24	25 26 27	28 29 30	31 32	33 34	35 36	37 38	39 40 41

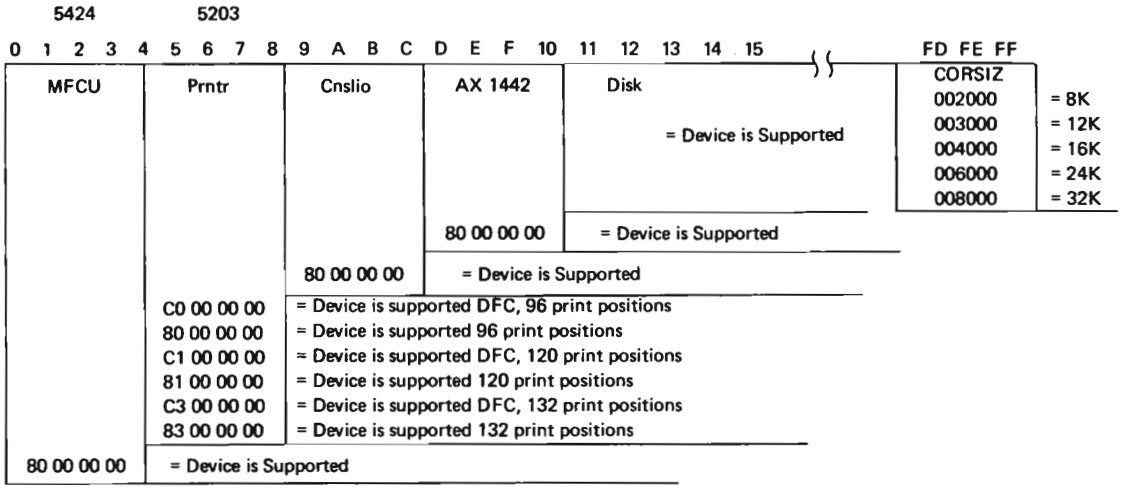
Vol Seq	Bkwd Chain PTR	Pack ID	File Name	Dev	Attribute	DTF SWA Ind	IOS Open Save	Not Used
42	43 44	45 46 47 48	49 50 51 52 53 54 55 56	57	58 59 60	61	62	63

Note 2

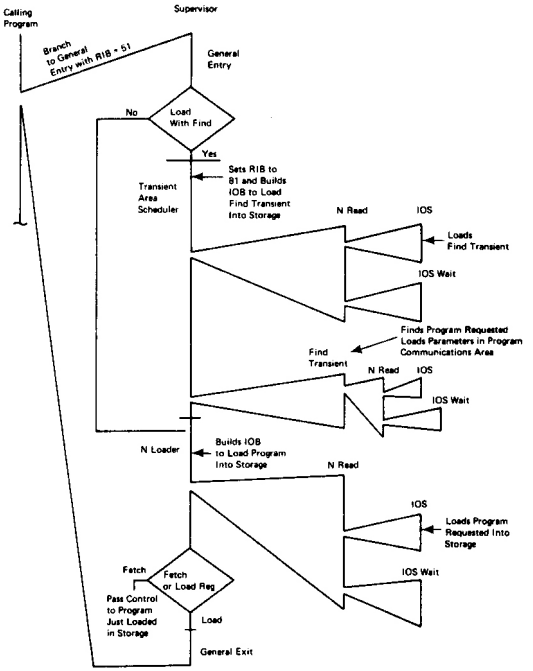
Note 1: Byte 39 bit 0 off = no. of records
bit 0 on = no. of tracks

Note 2: Bytes 45-63 in SWA only

Note 3: VTOC dir tag 0 points to the VTOC file label 01 which is located at the highest disk address of VTOC.


5424
5203
0 1 2 3 4 5 6 7 8 9 A B C D E F 10 11 12 13 14 15
FD FE FF
MFCU
Prntr
Cnslio
AX 1442
Disk
= Device is Supported
CORSIZ
002000 = 8K
003000 = 12K
004000 = 16K
006000 = 24K
008000 = 32K
80 00 00 00
= Device is Supported
80 00 00 00
= Device is Supported
C0 00 00 00 = Device is supported DFC, 96 print positions
80 00 00 00 = Device is supported 96 print positions
C1 00 00 00 = Device is supported DFC, 120 print positions
81 00 00 00 = Device is supported 120 print positions
C3 00 00 00 = Device is supported DFC, 132 print positions
83 00 00 00 = Device is supported 132 print positions
80 00 00 00
= Device is Supported

RIB REQUEST


Calling Program
Supervisor
Branch to General Entry with RIB = 51
General Entry
No
Load With Find
Yes
Sets RIB to 81 and Builds IOB to Load Find Transient Into Storage
Transient Area Scheduler
N Read
IOS
Loads Find Transient
IOS Wait
Finds Program Requested Loads Parameters in Program Communications Area
Find Transient
N Read
IOS
IOS Wait
N Loader
Builds IOB to Load Program Into Storage
N Read
IOS
Loads Program Requested Into Storage
IOS Wait
Fetch
Fetch or Load Req
Pass Control to Program Just Loaded in Storage
Load
General Exit

REQUEST INDICATOR BYTE

Meaning	Bit 0	1	2	3	4	5	6	7	Hex
Load XR2 with calling prog level comm address	0	0	0	0	0	0	0	0	00
Use System IOB	0	1	1	0	0	0	0	0	60
Use Program IOB	0	1	0	0	0	0	0	0	40
FETCH	0	1	0	1	0	0	0	0	50
FETCH to Address	0	1	0	1	1	0	0	0	58
System FETCH	0	1	0	1	0	1	0	0	54
LOAD	0	1	0	0	1	0	0	0	48
RPG LOAD	0	1	0	0	0	0	0	0	40
Without FIND	0	1	0	0	0	0	0	0	40
With FIND	0	1	0	0	0	0	0	1	41

The above values can be combined to form multiple RIB meanings. The following examples indicate some of the possibilities. The hexadecimal value on the right is used as the RIB value.

Examples	0	1	2	3	4	5	6	7	Hex
FETCH, SYS IOB	0	1	1	1	0	0	0	0	70
FETCH, PGM IOB	0	1	0	1	0	0	0	0	50
FETCH, PGM IOB, FIND	0	1	0	1	0	0	0	1	51
FETCH TO @, SYS IOB	0	1	1	1	1	0	0	0	78
FETCH TO @, PGM IOB	0	1	0	1	1	0	0	0	58
FETCH TO @, SYS IOB, FIND	0	1	1	1	1	0	0	1	79
System FETCH, SYS IOB	0	1	1	1	0	1	0	0	74
System FETCH, PGM IOB	0	1	0	1	0	1	0	0	54
LOAD, SYS IOB	0	1	1	0	1	0	0	0	68
LOAD, PGM IOB	0	1	0	0	1	0	0	0	48
LOAD, PGM IOB, FIND	0	1	0	0	1	0	0	1	49
LOAD USER PROG	0	1	0	1	1	1	0	0	5C

REQUEST INDICATOR BYTE (Transients)

TRANSIENT	NORMAL VALUE	REFRESH VALUE
Request Transient by C/S/#	80	C0
Find ($$SPFN)	81	C1
Open	82	C2
Close	83	C3
End of Job ($$SPEJ)	84	C4
Supported Halt/Syslog	85	C5
Supported SYSIN	86	C6
Scheduler Work Area - GET ($$SSGT)	87	C7
Scheduler Work Area - PUT ($$SSGT)	88	C8
Scheduler Work Area - R/W ($$SSSC)	89	C9
VTOC Read/Write ($$SSVT)	8A	CA
Allocation Initiator ($$STAI)	8B	CB
Program Protect ($$SYPP)	8C	CC
Roll-in ($$STRI)	8D	CD
Roll-out ($$STRO)	8E	CE
RPG Halt Processor	8F	CF
OBR/SDR	90	D0

DISK DTF PRE-OPEN

DISK DATA MGMT PRE-OPEN DTF X=UNUSED AREAS OF PRE-OPEN DTF

1	DTFDEV DEVICE O CODE	0
1	DTFUPS EXT IND	1
2	DTFATR ATTRIBUTES	2
3	DTFCHA RECORD LENGTH	2
5	DTFCHB @ OF NEXT DTF	2
7	DTFWKB LOGICAL REC AREA	2
D	DTFIOB IOB AREA ADD	2
11	DTFBKL BLOCK LENGTH	2
15	DTFMVF @ OF EXTENT TBL (MVF)	2
18	DTFNUM NUM OF EXTENTS	2
1D		X

7	DTFNAM FILENAME	26
26	DTFKAD @ OF KEY OF CURR REC	2
32	DTFKAD @ OF KEY BEING RETRIEVED	(2)
32	DTFHI @ OF HIGH KEY	(2)
32	DTFKL KEY LENGTH	2
38	DTFKD DISP OF KEY IN RECORD	2
3C	DTFMIX CORE @ OF MASTER INDEX	2
3E	DTFBYT NUM BYTES IN MASTER INDEX	2
40	(NOT USED)	77
80	LAST BYTE	

NAME PURPOSE — FLD LEN — LEFTMOST FLD ADD

DISK DTF POST OPEN

DISK DTF POST OPEN (continued)

DISK DTF POST OPEN (continued)

MFCU DTF FORMATS

Pre-Open	
Device	0
UPSI	1
Attributes	2
Rec Length	4
Addr Nxt DTF	6
U N U S E D	8
Addr 2nd Rd IOB	E
Addr 2nd Rd I/O Area	10
Addr 2nd Pch IOB	12
Addr 2nd Pch I/O Area	14
Unused	16
Pointer to Print IOB	17
Addr 1st Rd IOB	19
Addr 1st Rd I/O Area	1B
Addr 1st Pch IOB	1D
Addr 1st Pch I/O Area	1F
Addr 1st PR I/O Area	21
UNUSED	23

Post-Open Chgs and Adds	
	0
	1
	2
DTFCHN A(Bkwd)	4
DTFCHN B (Fwd)	6
Arr Save Area	8
XRI Save Area	A
Logical Rec Addr	C
Comp Code	E
Operation	F
Stacker Sel	10
WORK AREA	11
Err Area Addr	17
Work Area	19
Curr Rd IOB Addr	1B
Curr Pch IOB Addr	1D
Curr Pch I/O Area Addr	1F
Pointer to Print IOB	21
	23
	24

PRINTER DTF FORMATS

Pre-Open		Post-Open Chgs and Adds	
Device	0		0
UPSI	1		1
Attributes	2		2
Record Length	4	DTF Chn A (Bkwd)	4
Addr Nxt DTF	6	DTF Chn B (Fwd)	6
U N U S E D	8	Arr Save Area	8
		XRI Save Area	A
		Logical Rec Addr	C
Addr 2nd I/O Area	E	Comp Code	E
Addr 2nd IOB	10	Operation	F
U N U S E D	12	Skip Before	10
		Space Before	11
		Skip After	12
		Space After	13
		Q Byte (Device)	14
		R Byte	15
		Work Area	16
		Err Area Addr	17
		Work Area	19
Addr 1st IOB	1C	Err Recovery Addr	1C
Addr 1st I/O Area	1E	Prev IOB Addr	1E
Unused	20	Curr I/O Area Addr	20
OF Line	21		
Max No Lines	22	Rec Lng	22
Err Area Addr	23	OF Line	23
		Pos Ctr	24

XR2 Points to

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13
First		Last		Self		F	C	S	N	SNS Save		Add of Self (Nxt Q)		Logical (Last) Cyl		Alt Tracks Physical C	S	Q & R Save For Write/ Verify	Flag '01' Drive Not Rdy

Work Area for Q

0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	10	11	12	13
WKFCSD				DCFADR		(DC) One				Recal B FCSN Pointer		RECALB FCSN				Nxt Cyl		DS DT AD Dual Spindle Arr Save for End of Cyl	
Init to — 00	00	00	00			00	00	00	01			00	00	00	FF	00	24		

DISK IOB FORMAT

DISK IOB

0 1	2	3	4	5	6	7	8 9
IOBCHN	IOBCMP	IOBQB	IOBRB	IOBCB	IOBSB	IOBNB	IOBDAT

40 - Normal Completion
41 - Permanent Error
42 - Scan Not Found
44 - Scan Equal Found

0X - Queued
8X - Seek Started
AX - Data Transfer Pending
BX - Data Transfer Started
4X - Operation Completed
X8 - IOB Wait
X5 - IOB Purged Due to Error in Associated IOB
X4 - Scan Equal
X2 - Scan Not Found
X1 - Permanent Error

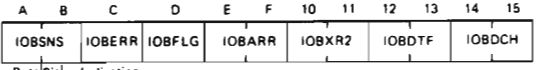
Removable Disk	
A 0	Control
A 1	Read
A 2	Write
A 3	Scan

Fixed Disk	
A 8	Control
A 9	Read
A A	Write
A B	Scan

Control	0 0	Seek
Read	0 0	Data
	0 1	Identifier
	0 2	Diagnostic
	0 3	Verify
Write	0 0	Data
	0 1	Identifier
Scan	0 0	Equal
	0 1	Low or Equal
	0 2	High or Equal

TR 0	1st Sector
0 0	2nd Sector
0 4	3rd Sector
0 8	4th Sector
0 C	
Etc	
TR 1	
8 0	
8 4	
D C	

DISK IOB



Byte	Bit	Indication
0	0	I/O No-Op (Single Only)
	1	Intervention Required
	2	Missing Address Mark
	3	Equipment Check
	4	Data Check
	5	No Record Found
	6	Track Condition Check
	7	Seek Check
1	0	Scan Equal
	1	Access Arm at Cyl 0
	2	End of Cyl
	3	Seek Busy
	4	Hundred Cyl's
	5	Device Overrun
	6	Status Address A
	7	Status Address B

Bit	Meaning
0	No Recovery if Sns Bits 2-4-5-6 Byte 1
1	No Verify on Write
2	No Err Log on Disk I/O
3	IOS Does Not Use C and S in IOB
4	Does Not Use Disk Data Mgmt (IOB Not Assoc DTF)
5	No Load I/O for DFDR
6	Err Logging in Progress
7	Data Xfer Involving Hlt Procedure

BSCA DTF AND IOB FORMATS

BSCA IOB FIELDS

Q Code of Last Op (Byte 2)

80 Control
81 Receive Only
82 Transmit and Receive
83 Receive Initial
84 Auto Dial

Sense Area (Byte 8)

80 Time Out Error
40 Data Check
30 Adapter Check
08 Invalid USACII
06 Lost Connection

Flag (Byte 5)

02 Delay IOB
04 1st Time Logic
08 Exec Channel Program
10 Last Block (ITB-Trans)
80 Enq Has Been Sent

Flag (Byte 6)

80 Input Both on For Conversational
40 Output
20 ITB
10 Transparent
08 Primary Receive
04 Operation

Completion Codes (Byte 7)
The following are the completion codes expected from DMIOCS for the read or get:

40 Normal Completion
41 Soft Abort Requested
42 End of File
44 No Record Found, Out of Extent, DU, DG, DO
4D Invalid Call by User - BSCA
4E Programmer Lost Communication - BSCA
4F No Connection

The following are the completion codes expected from DMIOCS for a put or write:

40 Normal Completion
41 Soft Abort Requested
46 Conversational Reply Requested for BSCA
48 Overflow
4B Invalid ASCII
4D Invalid Call by User - BSCA
4E Programmer Lost Communication - BSCA
4F No Connection
50 Key Changed
60 Duplicate Add
62 Key Out of Sequence on Load or Add
70 End of Extent
80 Buffer Partly Processed
84 Buffer Ready for Transmit
88 Buffer is Being Transmitted

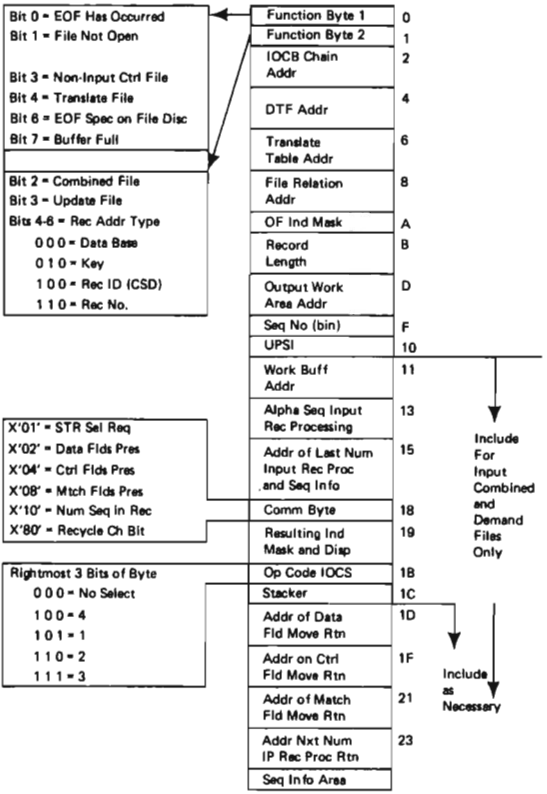
PRINTER IOB FORMAT

0	1	2	3	5	8	A	C	E	F	10
PIOQ	PIOR	PIOSTA	PIOSVA	PIOWKA	PIOERP	Not Used	PIOUFA	Not Used	PIOOVA	PIOPOS
Q Byte	R Byte	Status Info	Addr Perm IOS/ERP Save Area	Work Area	Disk Addr of ERP		Curr Prog I/O Area		0F Line	POS Ctr

If Printer Data Management is Bypassed Use Format Above
If Not - Use Bytes 20-36 of the DTF for IOB - Format Below

14	15	16	17	19	1B	1C	1E	20	22	23	24
PDFQ	PDFR	PDFSTA	PDFSVA	PDFSNS	PDFWKA	PDFERP	PDFIOB	PDFPRA	PDFDFL	PDFDFL	PDFPCT
Q Byte	R Byte	Comp Stat Byte	IOS/ERP Perm Save	Sense Area	Work Area	Disk Addr of ERP	Addr of Buff Assoc IOB	Addr Curr I/O Area	Log Recl	0F Line	Pos Ctr

INPUT/OUTPUT CONTROL BLOCK



OVERLAY LINKAGE

Pointers to follow a branch to overlay fetch routine

C0	87	Address of Overlay Fetch Routine	Overlay Fetch Table Entry Displacement for Overlay to be Fetched	Branch Address Used to Enter the Overlay After it is Fetched

Overlay Fetch Table Entry

Cylinder/Sector Displacement From Start of Root on Disk of this Overlay	Number of Text Sectors in Overlay	Storage Load Address	RLD Disp	Flag

X'80' = Overlay in Storage
X'40' = Main Overlay Area Used
X'20' = Sub Overlay Area Used
X'60' = Both Areas Used

RESERVED OBJECT COMMUNICATION AREA

INDICATOR TABLE

Displacement	Hex Byte Mask							
from XR1	80	40	20	10	08	04	02	01
C2	H4	H3	H2	H1		MR(Int.)	MR(Ex.)	1P
C3	L1	L0	LR	H9	H8	H7	H6	H5
C4	L9	L8	L7	L6	L5	L4	L3	L2
C5	U1	U2	U3	U4	U5	U6	U7	U8
C6								
C7								
C8								
C9	07	06	05	04	03	02	01	
CA	15	14	13	12	11	10	09	08
CB	23	22	21	20	19	18	17	16
CC	31	30	29	28	27	26	25	24
CD	39	38	37	36	35	34	33	32
CE	47	46	45	44	43	42	41	40
CF	55	54	53	52	51	50	49	48
D0	63	62	61	60	59	58	57	56
D1	71	70	69	68	67	66	65	64
D2	79	78	77	76	75	74	73	72
D3	87	86	85	84	83	82	81	80
D4	95	94	93	92	91	90	89	88
D5					99	98	97	96
D6	OV Ex.	OG Ex.	OF Ex.	OE Ex.	OD Ex.	OC Ex.	OB Ex.	OA Ex.
D7	OV 1st Int.	OG 1st Int.	OF 1st Int.	OE 1st Int.	OD 1st Int.	OC 1st Int.	OB 1st Int.	OA 1st Int.
D8	OV 2nd Int.	OG 2nd Int.	OF 2nd Int.	OE 2nd Int.	OD2nd Int.	OC 2nd Int.	OB 2nd Int.	OA 2nd Int.
D9	Total cycle switch	Control fields processed	Overflow being processed	EOF on look-ahead	******RESERVED			
DA-DC	Not used							

Note: For each overflow indicator there are two internal indicators. The first internal indicator indicates that overflow has occurred; the second indicator indicates that the overflow output code has been fetched.

Ex. = External
Int. = Internal

SYSTEM COMMUNICATION REGION - - NCPL1

This area is used to pass information between system programs. The following charts show the name of each entry, its displacement from the entry point (NCHIMG), its byte count and its contents. The address of this communication region is located at X'11'.

SYSTEM COMMUNICATION REGION (continued)

SEGMENT NAME	HEX DISPLACEMENT	NUMBER OF BYTES	CONTENTS
NCPL1	1	2	Address of Program Level 1 Communication Area
NCPL2	3	2	Address of Program Level 2 Communication Area
NCXTAB	5	2	Address of transient scheduler tables
NCFCTR	6	1	Fetch trace ID
NCSGEN	6	1	SYSGEN byte X'01' - Indicates to the Linkage Editor that SYSTEM has control and wants the current chain image placed in the new supervisor. X'80' - Indicates that $$ SGNPP has read the first record from SWA.
NCPRTZ	7	1	Printer size
NCLPSZ	8	1	Left tractor page size
NCRPSZ	9	1	Right tractor page size
NCSYSL	A	1	System printer ID
NCSLOG	D	3	System indicator C/S/Device (HALT/SYSLOG)
NCSWRK	F	2	Address of Scheduler Work Area
NCSYSQ	10	1	Q byte for system
NCOLIB	12	2	Address of system Object Library
NCSCH1	13	1	Scheduler Switches X'80' - Log device status X'40' - System date received X'20' - DPF system X'10' - Scheduler interlock for Program Level 1 X'08' - Scheduler interlock for Program Level 2

SYSTEM COMMUNICATION REGION (continued)

SEGMENT NAME	HEX DISPLACEMENT	NUMBER OF BYTES	CONTENTS
			X'04' - Date format Indicator off - MM/DD/YY Indicator on - DD/MM/YY X'02' Disk Drive Configuration X'01' 00 = F1, R1 01 = F1, R1, R2 11 = F1, R1, R2, F2
NXSMV1	14	1	Data Management/Scheduler Switches (Program Level 1) X'04' - Consecutive multivolume files on R2 X'08' - Consecutive multivolume files on R1 X'01' - Other file on R2 X'02' - Other file on R1
NCSMV2	15	1	Data Management/Scheduler Switches (Program Level 1) X'04' - Consecutive multivolume files on R2 X'08' - Consecutive multivolume files on R1 X'01' - Other file on R2 X'02' - Other file on R1
NCSCH	16	1	Scheduler byte X'80' - 22 LC interlock bit X'40' - Roll-in bit X'08' - Inquiry handled X'04' - Partition stmt received X'02' - Roll-out bit X'01' - Inquiry pending
NCDSKQ	18	1	Disk queue
NCSCH2	19	1	Partition value for level 2
NCMBSV	1A	1	Reserved
NCXTA	1B	1	Reserved

SYSTEM COMMUNICATION REGION (continued)

SEGMENT NAME	HEX DISPLACEMENT	NUMBER OF BYTES	CONTENTS
NCSTOR	2F	20	Transient storage area
NC@CIO	21	2	Address of console I/O Routine
NCRCSS	34	3	ROLLOUT C/S/
The following data areas are used only by a DPF system			
NCSXR1	36	2	
NCSXR2	38	2	This is a storage area for interrupt level 0
NCSPSR	3A	2	
NCSNS	3B	1	Reader select sense information X'80' - ON = level 1 OFF = level 2 X'40' - Cancel X'20' - MFCU X'10' - AUX reader X'08' - Printer keyboard
NCHALT	3D	2	Address of Resident Halt Routine (NPHALT)

PROGRAM LEVEL COMMUNICATION REGION - - N1COMM

This region is used to pass information between system programs. The following charts show the name for each entry, its displacement from the entry point (NPIOB), its byte count and its contents.

The address of this area is returned in XR2 after the user branches to General Entry with a Request Indicator Byte (RIB) of X'00'.

PROGRAM LEVEL COMMUNICATION REGION (continued)

SEGMENT NAME	HEX DISPLACEMENT	NUMBER OF BYTES	CONTENTS	
NPIOB	0	0	Entry for program level IOB	
NPCHAN	1	2	IOS chain pointer	
NIOCMP	2	1	Completion code (disk IOS)	
NIOQB	3	1	IOB Q byte	
NIORB	4	1	IOB R byte	
NIOCB	5	1	IOB cyclic byte	
NIOSB	6	1	IOB sector byte	
NIONB	7	1	Number of sectors to be read -1	
NIODAT	9	2	Data buffer address	
NIOSNS	B	2	Sense bytes (disk IOS)	
NIOERR	C	1	IOS error retry counter	
NIOFLG	D	1	Flag bits (disk IOS)	
NIOOBR	11	4	OBR - SDR transient save areas (ARR, XR2)	
NPDTF@	13	2	First DTF address	
NPRIB	14	1	Program request indicator byte (RIB)	
NPBEG	16	2	Program level beginning address	
NPEND	18	2	Program level end address	
NPQ	19	1	Program level Q byte (as in the // LOAD statement)	
NPRLF	1B	2	Program relocation factor	
NPCYL	1D	2	C/S of first load for this program level	
NPOLIB	1F	2	C/S of program object library	
NPXR1	21	2	Register 1 save area	Used as save area for the program requesting general entry (INENTRY)
PRXR2	23	2	Register 2 save area	
NPNSI	25	2	Return address	

PROGRAM LEVEL COMMUNICATION REGION

(continued)

SEGMENT NAME	HEX DISPLACEMENT	NUMBER OF BYTES	CONTENTS
NPORLF	27	2	Overlay relocation factor
NPTXT	29	2	Overlay text address
NPTEMP	2B	2	Temporary storage for resident loader (NLOADR)
Parameter List for the Resident Loader (NLOADR)			
NPCS	2D	2	C/S address of module to be loaded
NP#S	2E	1	Number of sectors to be read
NPLNK	30	2	Linkage editor address
NPRLD	31	1	Displacement of Relocation Directory (RLD)
NPENT	33	2	Address of entry point of loaded module
NPLOD	35	2	Load address
NPEOJ	36	1	End of Job ID X'01' RPG Call Linkage Editor
NPUPSI	37	1	UPSI switches
NPNAME	3D	6	Program name that is currently being executed
NPRELS	3E	1	Release level
NPDATE	44	6	Program date
NPSYSI	48	4	SYSIN indicator (C/S Device information)
Scheduler parameters			
NPSCH1	49	1	Reader/Interpreter switches X'01' - IPL mode X'02' - INTER mode X'04' - INTRA mode X'08' - Override request X'10' - Procedure request X'20' - // SWITCH received X'40' - // COMPILE received X'80' - // DATE received (INTRA)

PROGRAM LEVEL COMMUNICATION REGION

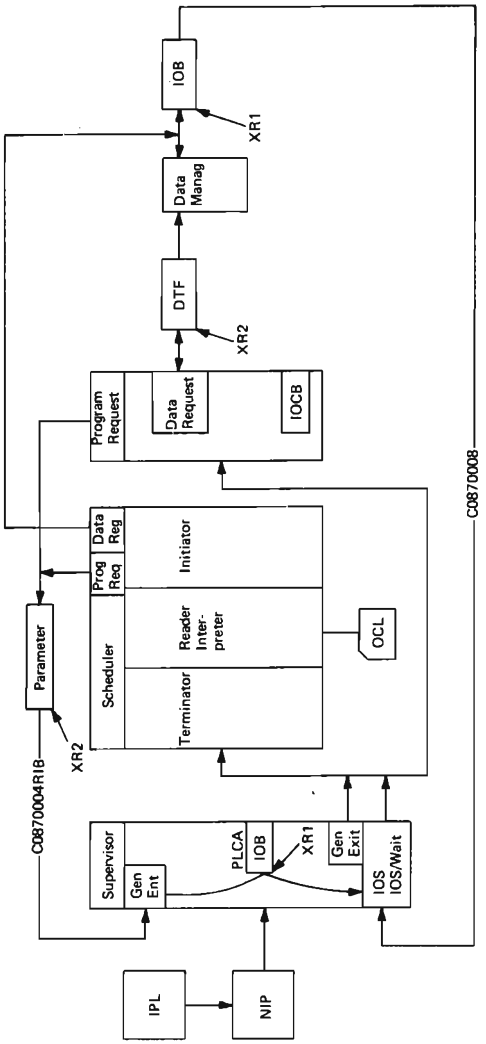
(continued)

SEGMENT NAME	HEX DISPLACEMENT	NUMBER OF BYTES	CONTENTS
NPSCH2	4A	1	Scheduler Switch X'01' - Controlled cancel X'02' - Immediate cancel X'04' - Clear X'08' - End of Job indicator X'10' - A file statement received X'20' - / READ from SYSIN device X'40' - Utility control cards in Scheduler Work Area X'80' - Continuation
NPSCH3	4B	1	Scheduler Switches X'80' - Tag Sort required X'40' - Allocate transient required X'20' - Source required X'10' - Logging (HALT/SYSLOG) Indicator off - logging specified Indicator on - logging not specified Statement Origin X'08' - From procedure X'04' - Additional procedure statement X'02' - Match/merge statement from SYSIN device X'01' - Program level Indicator off - level 1 Indicator on - level 2
NPOBJO	4C	1	Object deck output O code
NPBPSD	4D	1	Available status of SYSIN device X'80' - MFCU X'40' - Console I/O X'20' - 1442 X'10' - AUX on reader select switch X'08' - Console on reader select switch
NPSCH4	4E	1	Allocation information X'80' - Operation bit X'40' - // IMAGE received

PROGRAM LEVEL COMMUNICATION REGION (continued)

SEGMENT NAME	HEX DISPLACEMENT	NUMBER OF BYTES	CONTENTS
			X'20' - // FORMS received X'10' - F1 needed for allocation X'08' - R1 needed for allocation X'04' - R2 needed for allocation X'02' - R2 needed for allocation X'01' - EOJ Scheduler bit
NPSCH8	4F	1	Type of files needed X'04' - Allocate unsuccessful X'02' - Maximum request met X'01' - Minimum request met
NPSCH5	50	1	
NPSCH6	52	2	Save area for IAR pointer
NPSCH7	53	1	Save of last SYSIN assignment
NPWKB	55	2	Disk IOS work area
NPSCH9	56	1	Disk log unit ID for EOJ
The following data areas are used only by the Resident Halt Routine (NPHALT)in a DPF system			
NPHALT	57	1	Program level HPL
NPHLTO	58	1	O code for HPL
NPHLTR	59	1	R code for HPL
NPHBCH	5D	4	Branch for Resident Halt Routine (NPHALT)
NPHXR2	5F	2	Parameter save area
NPHTRN	66	7	Transient storage area
NPHQSV	83	29	Transient queue save area

DISK SYSTEM PROGRAM LOGIC FLOW



NOTES

ROCA- RESERVED OBJECT
COMMUNINCATION AREA
DTF- DEFINE THE FILE
IOCB- INPUT OUTPUT CONTROL BLOCK
RIB- REQUEST INDICATOR BYTE
PLCA- PROGRAM LEVEL
COMMUNICATION AREA

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