IBM

Series/1

GA34-1561-0

File No. S1-14

IBM Series/1

Series/1 to Series/1 Attachment

RPQs D02241 and D02242

Custom Feature

Preface

This publication describes the IBM Series/1 to Series/1 Attachment, RPQ D02241 and RPQ D02242, custom features designed for the IBM Series/1. The intended audience for this publication is customer executives, programmers, and maintenance personnel who will use this information to order products, prepare machine language code, and supplement other maintenance aids. The subject matter is presented in two chapters and two appendixes. Chapter 1 introduces the RPQs and gives configuration and planning information. Chapter 2 describes the data transfer operations the Series/1 to Series/1 Attachment uses. Appendix A contains Operate I/O and DPC operation reference material. Appendix B contains diagnostic command information.

Related Publications

IBM Series/1 4955 Processor and Processor Features Description, GA34-0021
IBM Series/1 4953 Processor and Processor Features Description, GA34-0022
IBM Series/1 System Summary, GA34-0035
IBM Series/1 Customer Site Preparation Manual, SA34-0050

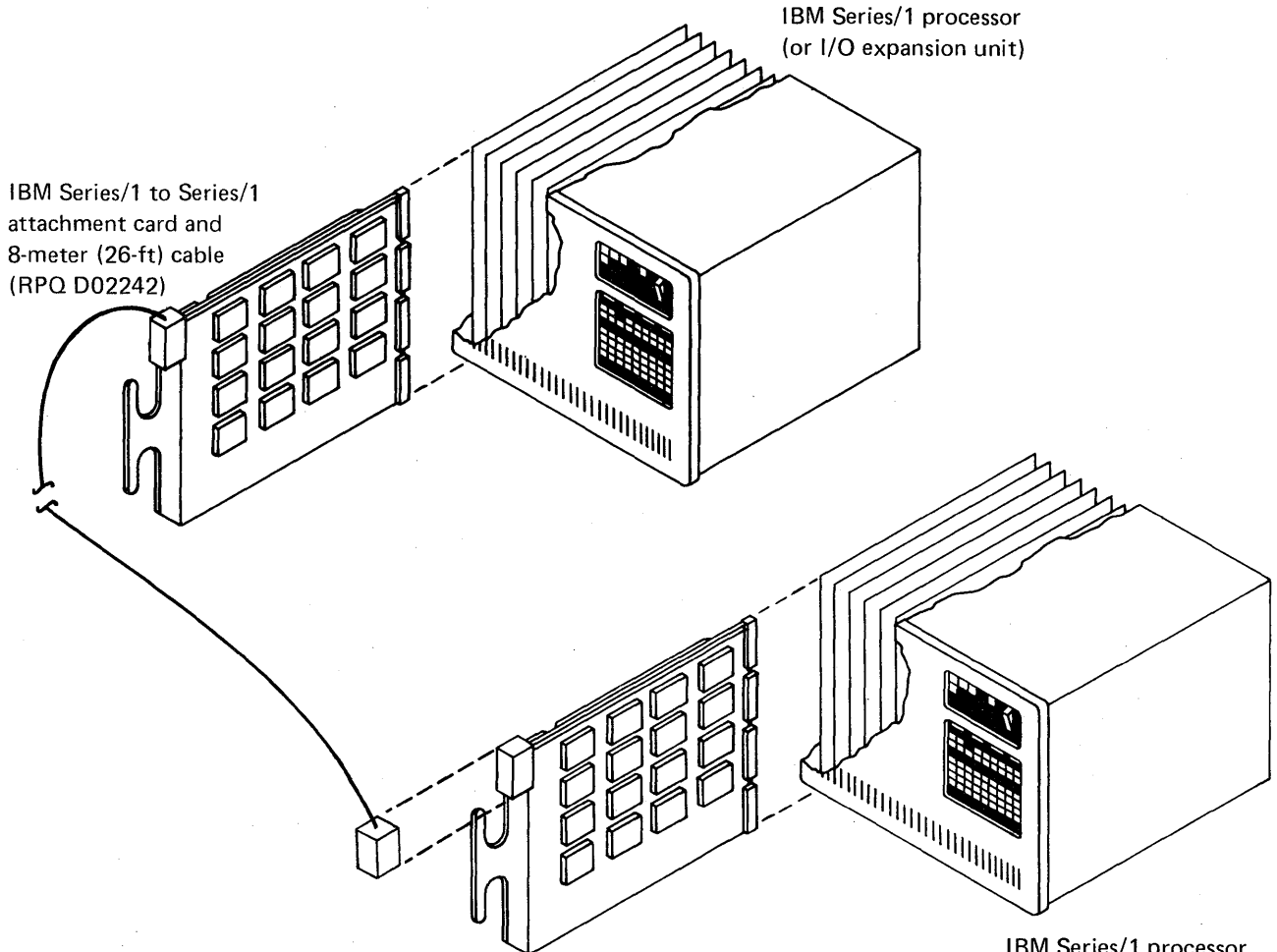
Additional publications are listed in *IBM Series/1 Graphic Bibliography*, GA34-0055.

First Edition (December 1978)

Contents

Chapter 1. Introduction and Planning

The IBM Series/1 to Series/1 Attachment RPQs D02241 and D02242 expand the communication capability of the Series/1 processor to meet applications requiring processor-to-processor communication. This communication link is accomplished by an attachment card plugged into each processor's I/O channel and connected via the supplied 8-meter (26-foot) cable. (See Figure 1-1.) This interface provides programmable error detection capabilities at a maximum instantaneous data rate of 65 kilobytes per second. (Data rate is dependent upon the block size of data transferred and cable length.)



Note: RPQ D02246 provides additional 3-meter (10-ft) increments to the 8-meter (26-ft) cable included in RPQ D02242.

Figure 1-1. Series/1 to Series/1 Attachment configuration

Configuration

RPQ D02241 contains an IBM Series/1 attachment card that will have priority if a contention period for data transfer should occur between this attachment and the complementary attachment, RPQ D02242. RPQ D02246 provides additional 3-meter (10-foot) increments to the 8-meter (26-foot) cable included in RPQ D02242. With a maximum order quantity of four extra cable increments, the maximum allowable cable length is 20 meters (65 feet).

If a replacement cable is required for use with RPQs D02241 and D02242, RPQ D02268 must be ordered, along with the appropriate quantity of extra cable increments (RPQ D02246).

The maximum instantaneous data rate that can be achieved by the Series/1 to Series/1 Attachment is 65 kilobytes per second. Throughput, however, can vary and is dependent upon the block size of the data which is transferred and cable length.

Multiple Series/1 to Series/1 Attachments may be employed in any configuration. That is, any Series/1 processor could contain only RPQ D02241 feature cards, or only RPQ D02242 feature cards, or any combination of them both. Figure 1-2 shows an example of a configuration in which four Series/1 processors are linked. In this example, processor A has priority over processors B and C. However, processor D has priority over processor A.

Note: Multiple Series/1 to Series/1 Attachments cannot utilize a single communications link; that is, each attachment must have its own distinct cable.

Referring still to Figure 1-2, note that the RPQ ordering information for the illustrated configuration is given on the right, broken down by the requirements for each Series/1 processor.

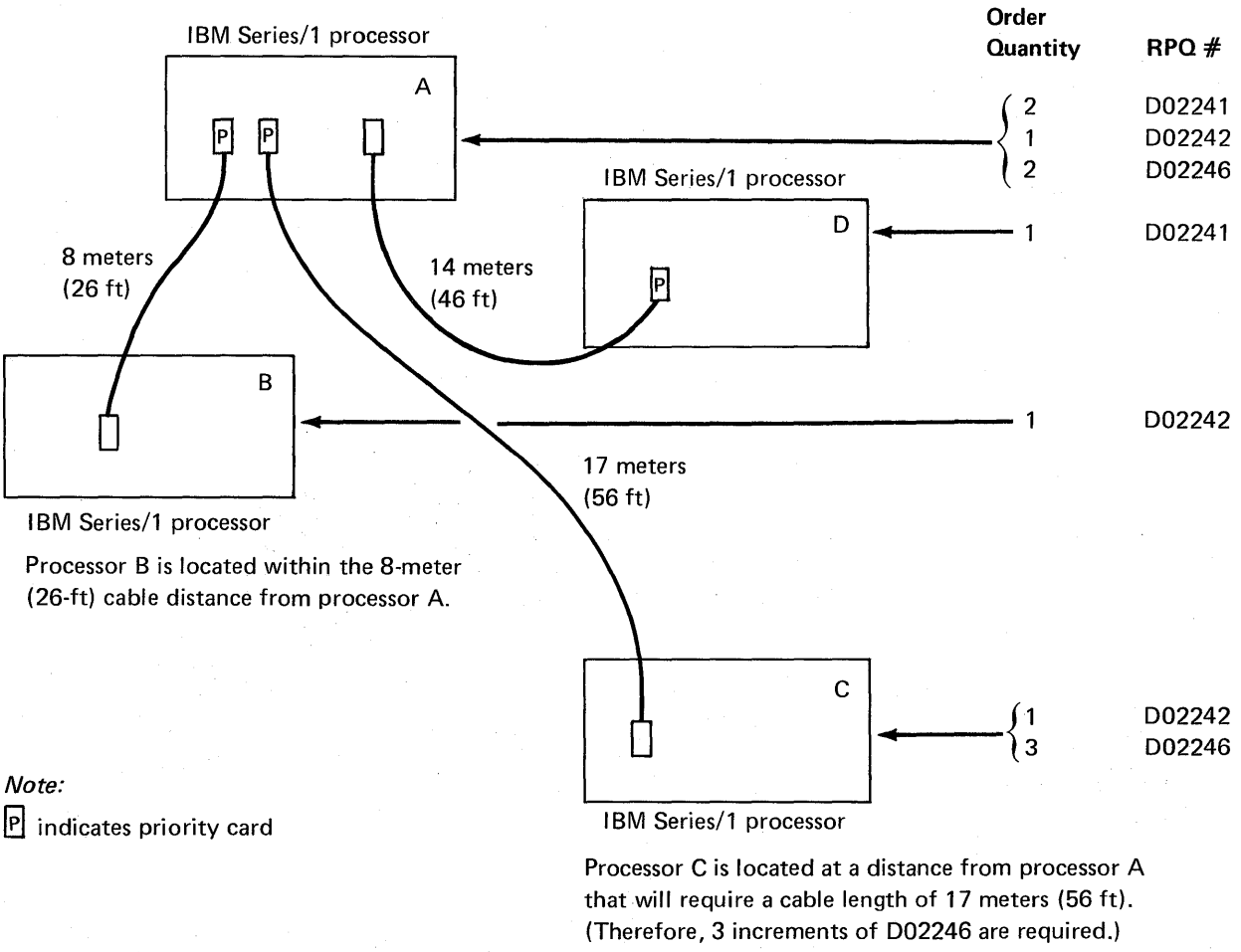


Figure 1-2. Multiple attachments configuration

Planning

Internal cable routing in a 1.8 meter rack (i.e., with the processor mounted at the top) would use a maximum of 2.5 meters (8.2 feet) of cable. See Figure 1-3.

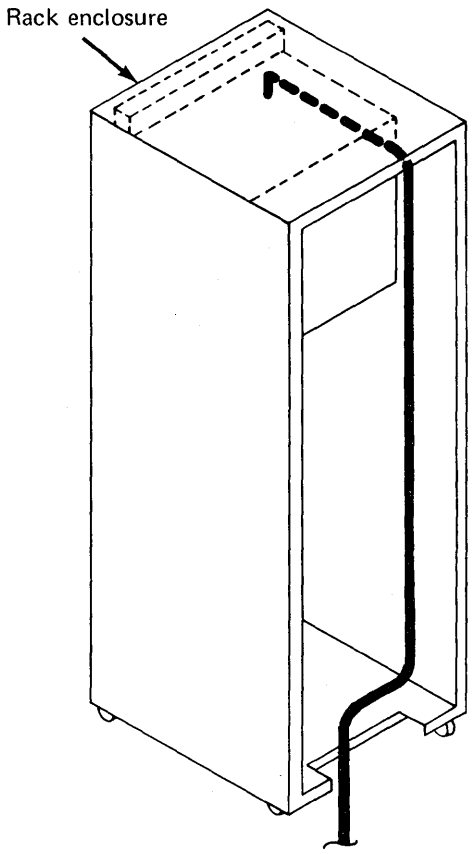


Figure 1-3. Cable routing

Cable Connections

Cable connection information is shown in Figure 1-4. Pin designations are given in the following table:

J1 & J2 connector pins	Line name
A12	DIO 1
A11	DIO 2
A10	DIO 3
A09	DIO 4
A08	Checksum Error Detected
A07	Data Valid (DAV)
A06	Not Ready for Data (NRFD)
A05	Not Data Accepted (NDAC)
A04	Active RPQ D02241
A03	RPQ D02242 Request
A01	Active RPQ D02242
B02	Shield (ground)
B12	DIO 5
B11	DIO 6
B10	DIO 7
B09	DIO 8
B08	RPQ D02241 Enable Operation
B07	DAV Ground
B06	NRFD Ground
B05	NDAC Ground
B04	Active RPQ D02241 Ground
B03	RPQ D02242 Request Ground
B01	Active RQP D02242 Ground
A02	Logic Ground

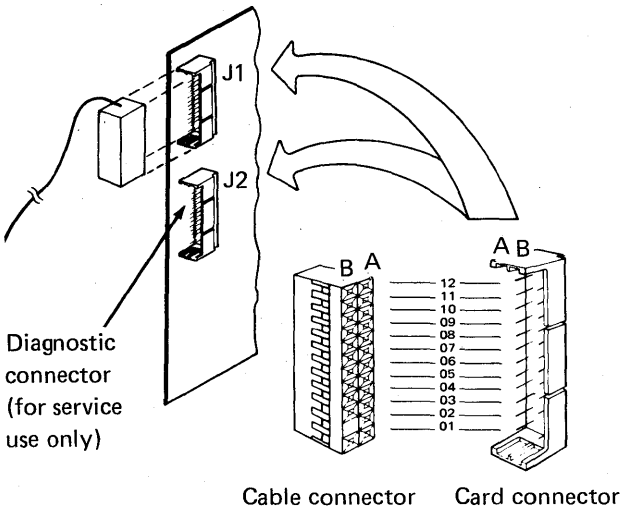


Figure 1-4. Cable connections

Chapter 2. Programming and Operation

This chapter, intended primarily for the programmer, describes the Series/1 to Series/1 direct communications operations. Data transfers are byte serial under cycle steal mode via a 16-line bidirectional interface cable. For a detailed review of basic Operate I/O and DPC operations (Read ID, Prepare, and Device Reset), see Appendix A.

Cycle Steal Data Transfers

Command execution in cycle steal mode permits overlapping of I/O and other processor operations.

The processor transfers the IDCB under direct program control (DPC) from processor storage to the Series/1 to Series/1 attachment. See Figure 2-1 1.

After the attachment accepts the IDCB:

1. It returns an Operate I/O condition code to the processor 2. The processor is now freed to continue with other operations.
2. The attachment uses the information in the IDCB to execute the command. The IDCB immediate data field contains the address of an 8-word device control block (DCB) defining the operation.
3. The attachment steals the DCB words 3 and data 4 needed to perform the command.
4. Each data transfer reduces a preset byte count in DCB word 6.
5. When the data transfer ends (i.e.,byte count equals zero), the attachment sends an interrupt request to the processor.

The processor then accepts the interrupt condition code and an Interrupt ID word from the attachment.

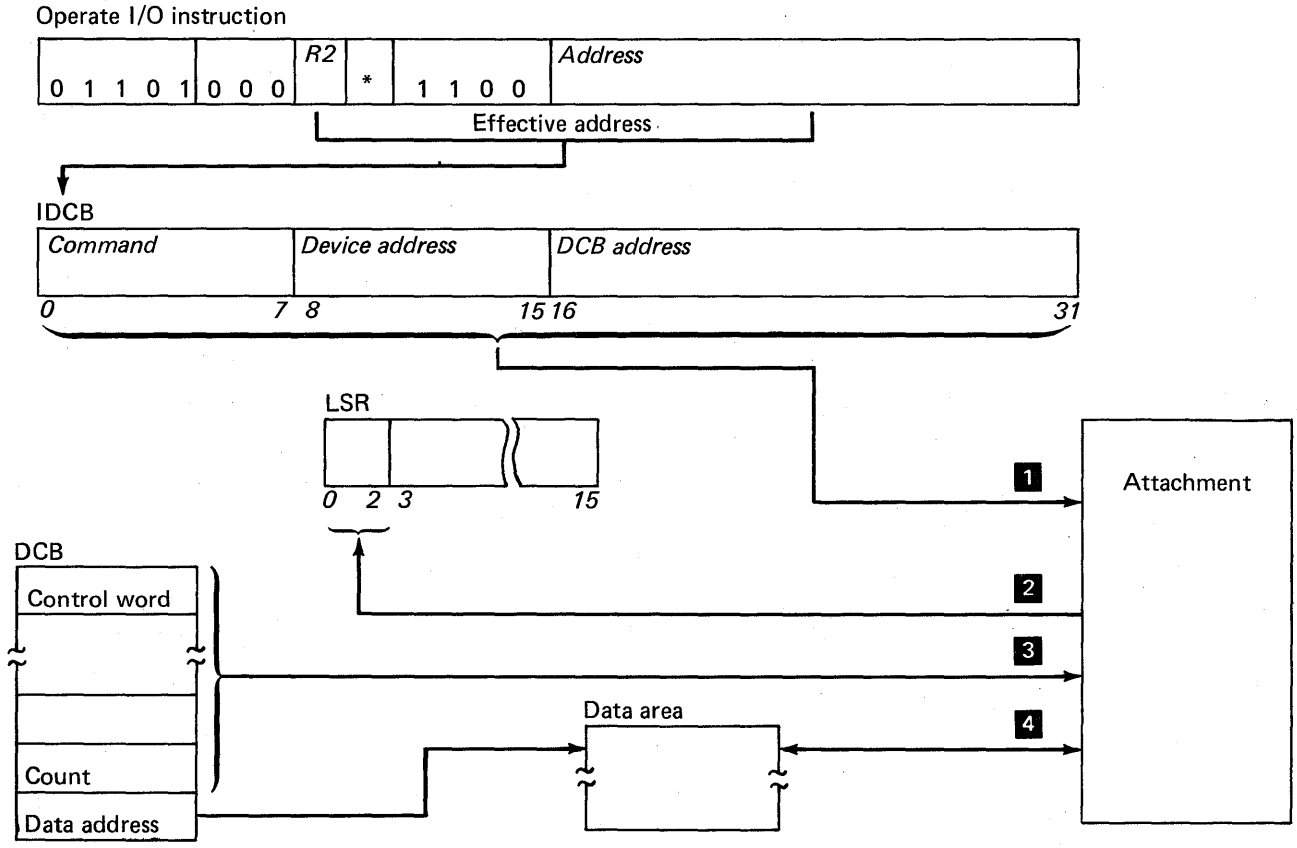
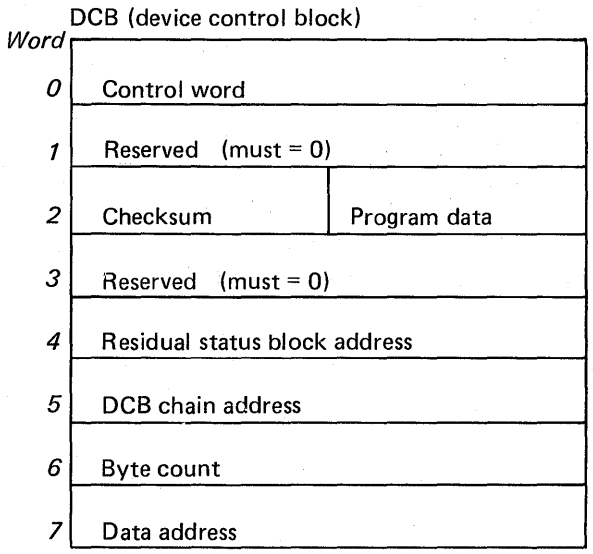
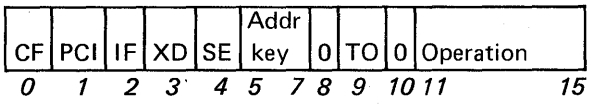


Figure 2-1. Cycle steal operation

Device Control Block (DCB)



DCB Word 0—Control Word



Bit 0 Chaining flag (CF). This bit equal to one indicates a DCB chaining operation. After completing the current DCB operation the attachment will not interrupt but will cycle steal the next DCB pointed to by the chaining address contained in word 5 of the current DCB.

Bit 1 This bit is not used and must be zero.

Bit 2 Input flag (IF). This bit indicates to the attachment the direction of the data transfer. If this bit equals zero, data transfer is from main storage to the attachment (output). If this bit equals one, data transfer is from attachment to main storage (input).

Bit 3 XD bit is not used and must be zero.

Bit 4 Not used.

Bits 5–7 Cycle steal address key. A program assigned three bit processor storage protect access key used by the attachment during data transfers for storage access authorization.

Bit 8 This bit is not used and must be zero.

Bit 9 Timer override (TO). An exception interrupt will occur if the data transfer is not complete in one second and bit 9 is equal to a zero. With bit 9 equal to a one, the attachment will wait indefinately for the data transfer to complete.

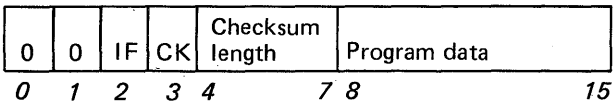
Bit 10 This bit is not used and must be zero.

Bits 11–15 Operation field. Bits 11–15 specify the operation to be performed.
10101 Read Header
10110 Read Data
10111 Write Data
11000 Write Abort

DCB Word 1—Reserved

Bits 0–15 These bits are not used and must be zero.

DCB Word 2—Checksum/Program Data



Bits 0–1 These bits are not used and must be zero.

Bit 2 The value of this bit should equal the value of the IF bit (bit 2 of DCB word 0).

Bit 3 Checksum bit specifies if error detection will occur during data transfer. Bit 11 equal to a one specifies error detection via checksum will occur during data transfer, and that the value in the checksum (bits 12–15) will be used to control the checksum block length. The checksum block length is the number of data bytes from which a checksum total will be generated and transmitted as the final byte.

Bits 4–7 These bits will control the number of data bytes from which a checksum byte will be generated.
0000 32 bytes
0001 16 bytes
0011 8 bytes
0111 4 bytes
1111 2 bytes

Bits 8–15 Program dependent data can be used by the Series/1 programmer for any status or information required.

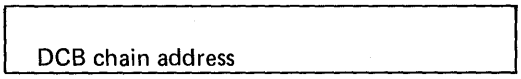
DCB Word 3—Reserved

These bits are not used and must be zero.

DCB Word 4—Reserved

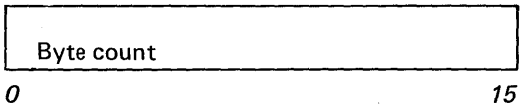
These bits are not used and must be zero.

DCB Word 5—DCB Chain Address



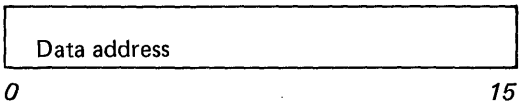
The DCB chain address word specifies the main storage address of the next DCB in the chain. To chain DCBs, set the chaining flag bit in the DCB control word (DCB word 0 bit 0) to a one. The address must be an even number or a DCB specification check will result.

DCB Word 6—Byte Count



The byte count word contains a 16-bit unsigned integer representing the number of data bytes to be transferred for the current DCB. Count is specified in bytes with a range of 0 to 65,534 and must be even or a DCB specification check will result.

DCB Word 7—Data Address



The data address word contains the starting main storage address for the data transfer and must start on a word boundary or a DCB specification check will result.

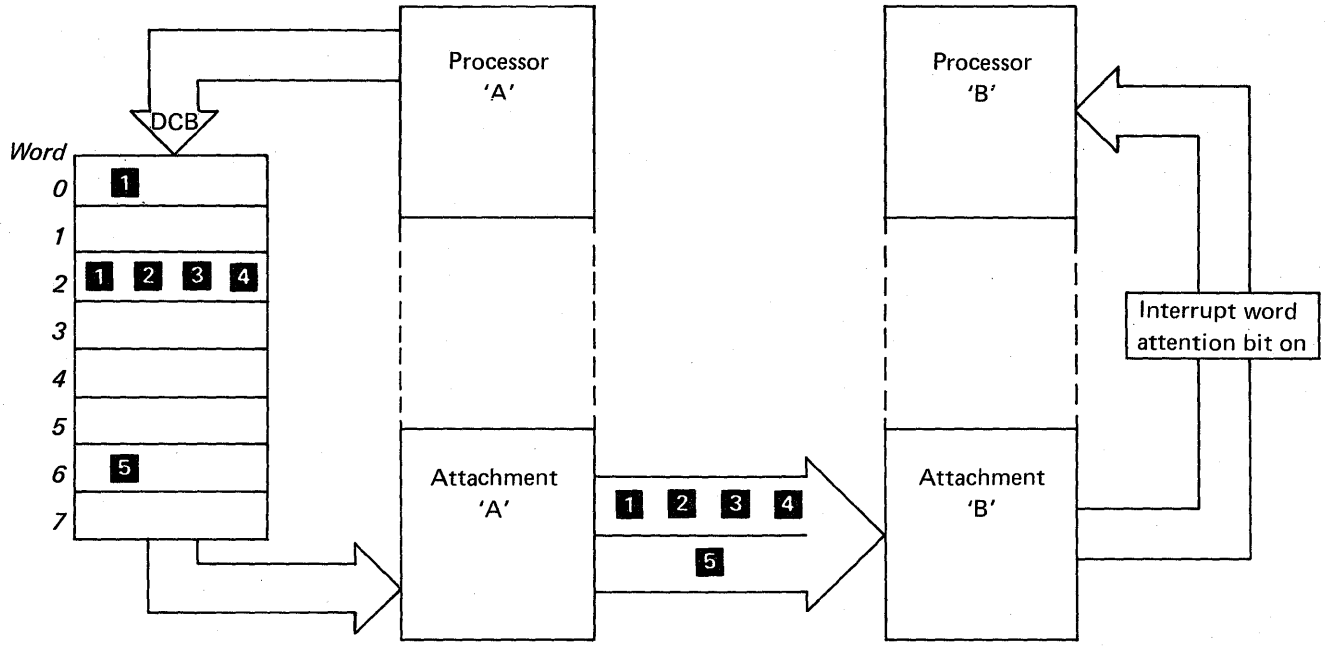
Start Command

The Start command initiates I/O operations that transfer data to or from processor storage in cycle steal mode. The control information and parameters required for a particular operation must be stored in the DCB associated with each Start command. The operations that the Start command initiates are contained in DCB word 0 bits 11–15 and are:

- Read Header
- Read Data
- Write Data
- Write Abort

Figure 2-2 gives an overview of a data transfer operation.

Processor 'A' initiates a data transfer operation to processor 'B'. Processor 'A' attachment uses information in the DCB to configure and transmit a two-word header.



The two-word header made up by the attachment is:

Word 1

Bit 0 is zero

Bit 1 is zero

Bit 2 is equal to DCB word 0, bit 2 (read/write bit) and DCB word 2, bit 2 (read/write bit) 1

Bit 3 is equal to DCB word 2, bit 3 (checksum) 2

Bits 4–7 are equal to DCB word 2, bits 4–7 (checksum control) 3

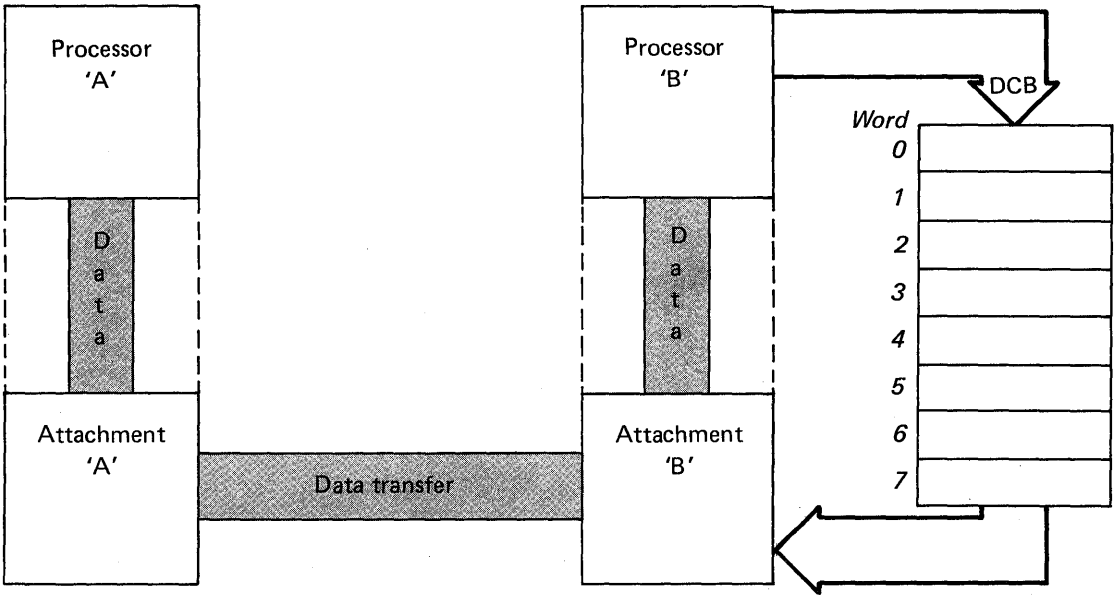
Bits 8–15 are equal to DCB word 2, bits 8–15 (program parameters) 4

Word 2 is equal to DCB word 6 (byte count) 5

Processor 'B' attachment receives the two-word header and inverts the read/write bit (bit 2 of word 1) and causes an interrupt with the attention bit on.

Figure 2-2. Data transfer operation (part 1 of 2)

Processor 'B' now accepts the interrupt from its attachment and initiates a read header operation. A user-written program within processor 'B' then interrogates the two word header and uses this information to build a new DCB and issue the appropriate Start command. Data is transferred between the two processors with each attachment cycle stealing data to/from its main memory.



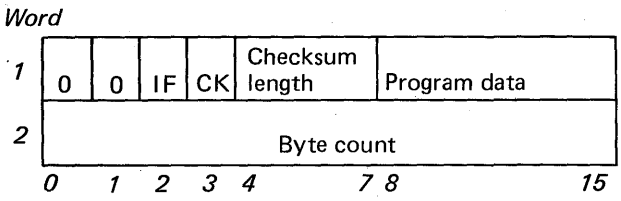
Either processor can initiate a data transfer operation, if processor 'A' initiates a write operation then processor 'B' would respond with a read operation, and the opposite is true.

One of the attachments (D02241) will take priority in data transfer to resolve any contention problem if both processors should initiate data transfer simultaneously.

Figure 2-2. Data transfer operation (part 2 of 2)

Read Header

The Read Header operation is used to transfer the two-word (four-byte) header into main memory when an Attention interrupt or an Attention and Exception interrupt has been received. These two interrupts specify that an information transfer has been initiated by the other processor and a "matching" Read Data or Write Data operation is required to transfer the information. In order for the "matching" Read Data or Write Data operation to be performed, a user-written program must interrogate the two-word header that is stored in main memory to build a new DCB and issue the appropriate Start command.



Read Data

The Read Data operation will cause an input of data into main memory. The Read Data operation can initiate a data transfer operation, or it can be in response to a Write Data operation. Information needed for this data transfer operation will be contained in the DCB.

Write Data

The Write Data operation will cause the output of data from main memory. The Write Data operation can initiate a data transfer operation, or it can be in response to a Read Data operation. Information needed for this data transfer operation will be contained in the DCB.

Write Abort

The Write Abort operation is used by the responding processor to end the data transfer operation by giving the initiating processor an exception interrupt. For example, the responding processor may want to terminate a data transfer operation after receiving the header if the byte count specified is too large.

Start Cycle Steal Status Command

The Start Cycle Steal Status Command initiates a cycle steal operation to obtain residual parameters from the attachment (11 Cycle Steal Status Words) if the previous cycle steal operation terminated due to an error or exception condition, or any time residual status is desired.

Cycle Steal Status Word 0

Bits	Function
0–15	Residual Address. The Residual Address word contains the main storage address of the last attempted cycle steal transfer associated with a Start command. If an error occurs during a Start Cycle Status operation this address is not altered. The residual address may be a data address, a DCB address, or a residual status block address and is cleared only by a power on reset.

Cycle Steal Status Word 1

Bits	Function
0–15	Residual byte count. The Residual Byte Count word is the last cycle steal operation count less the number of bytes successfully transferred.

Cycle Steal Status Word 2—Not Used

Cycle Steal Status Word 3—Not Used

Cycle Steal Status Word 4—Error Status

Bits	Function
0	Bus timed out on Acceptor Handshake. The attachment was attempting to receive data from the bus.
1	Reserved.
2	Bus timed out on Source Handshake. The attachment was attempting to send data to the bus.
3–15	Reserved, must be zero.

Cycle Steal Status Word 5

Bits	Function
0	Status of DIO line 8 after power on.
1	Status of DIO line 7 after power on.
2	Status of DIO line 6 after power on.
3	Status of DIO line 5 after power on.
4	Status of DIO line 4 after power on.
5	Status of DIO line 3 after power on.
6	Status of DIO line 2 after power on.
7	Status of DIO line 1 after power on.
8	Status of active RPQ D02241 after power on.
9	Status of active RPQ D02242 after power on.
10	Status of RPQ D02242 request operation after power on.
11	Status of checksum error detected after power on.
12	Status of RPQ D02241 enable slave operation after power on.
13	Status of NRFD line after power on.
14	Status of NDAC line after power on.
15	Status of DAV line after power on.

Cycle Steal Status Word 6

Bits	Function
0–15	This word contains the current status of the interface. The structure of this word is the same as for Cycle Steal Status Word 5.

Cycle Steal Status Word 7

Bits	Function
0–7	This byte contains abort message condition codes generated by the system that issued an abort operation.
8–15	Not used.

Cycle Steal Status Word 8

Bits	Function
0–3	Bits 0–3 indicate the cause of the DCB specification check.
	0000 Not used 0001 Odd DCB address 0010 Invalid PCI bit 0011 Invalid IF bit 0100 Invalid XD bit 0101 Invalid SE bit 0110 Invalid DCB word 0 bit 8 0111 Invalid timer bit 1000 Invalid DCB word 0 bit 10 1001 Non-zero unused word 1010 Odd RSB address 1011 Odd chaining address 1100 Invalid byte count 1101 Invalid command code for configuration 1110 Not used 1111 Not used
4–8	Not used and must be zero
9–11	Indicate the following status:
	0000 Not used 0001 Invalid header IF bit 0010 Invalid check bit 0011 Invalid checksum 0100 Invalid program word 0101 Not used 0110 through 0111 Not used
12–15	Not used and must be zero

Cycle Steal Status Word 9

Bits	Function
0–3	Reserved
4	Other system not active
5	Invalid command sequence
6	Checksum error detected
7	Not used (equals zero)
8–15	Contain the checksum byte used

Cycle Steal Status Word 10

Bits	Function
0–15	This word will contain the starting address of the last DCB used by the attachment.

Condition Codes

Operate I/O

Condition codes (CC) are reported after execution of each Operate I/O instruction. See Figure 2-3. The appropriate condition code is transferred into the even, carry, and overflow bit positions of the level status register (LSR) in the processor.

Command	CC0	CC1	CC2	CC3	CC4	CC5	CC6	CC7
Read ID	X	X	X			X		X
Prepare	X					X		X
Device reset	X							X
Start	X	X	X			X		X
Start cycle steal status	X	X	X			X		X

CC Value	Meaning
0	Device not attached
1	Busy
2	Busy after reset
3	Command reject
4	Intervention required (not reported)
5	Interface data check
6	Controller busy (not reported)
7	Satisfactory

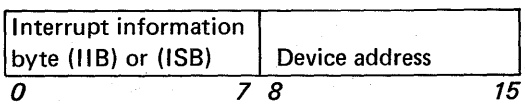
Figure 2-3. Condition code responses to Operate I/O instructions

Interrupt

Interrupt condition codes pertain to operations that continue beyond execution of the Operate I/O instruction (such as cycle stealing of data). The condition codes that are reported are:

CC Value	Meaning
2	Exception
3	Device end
4	Attention
6	Attention and exception

Along with the interrupt condition code the attachment also transfers an interrupt ID word to the processor. Bits 0–7 of the interrupt ID word are called the interrupt information byte (IIB) or Interrupt Status Byte depending on the condition code, and bits 8–15 are the device address.



If the condition code is 3 (device end) and bit 0 of the IIB equals one, a permissive end has occurred. If the condition code is 4 (attention) or 6 (attention and exception) and bit 1 of the IIB equals one, the other processor has requested service. In addition, if bit 2 equals one, a data exchange has been initiated by the other system.

For condition code 2, the IIB has a special format and is called an interrupt status byte (ISB). The ISB is coded as follows:

Bit 0 — *Device dependent status available.* When set to one, this bit signifies that further status is available. This status is obtained using the Start Cycle Steal Status command. This bit is set to one for incorrect length records and when an error was encountered during execution of the on-line diagnostic test.

Bit 1 — *Delayed command reject.* This bit is set to one if the device cannot execute the command due to one of the following conditions:

1. The IDCB contains an incorrect parameter. Examples are (a) an odd-byte DCB address or (b) an incorrect function/modifier combination.
2. The present state of the device, such as 'not ready' condition, prevents execution of an I/O command specified in the IDCB.

Delayed command reject is set in the ISB only if the device cannot report I/O instruction condition codes for the condition. The operation is terminated. DCB is not fetched.

Bit 2 — Not used.

Bit 3 — *DCB specification check.* This bit is set to one when the device cannot execute a command due to an incorrect parameter specification in the DCB. Examples are (1) an odd-byte DCB chaining or status address, (2) the byte count is odd for a word-only device, (3) an odd-byte data address for a word-only device,

(4) an invalid command or invalid bit settings in the control word, or (5) an incorrect count.

The operation is terminated.

Bit 4 *Storage data check.* This error condition applies to cycle steal output operations only. If the bit is set to one, it indicates that the main storage location accessed during the current output cycle contained bad parity. Parity in main storage is not corrected. The attachment terminates the operation. The bad parity data is not transferred to the I/O data bus. No machine check condition occurs.

Bit 5 *Invalid storage address.* When set to one, this bit indicates that during a cycle steal operation, the attachment has presented a main storage address that is outside the storage size of the system. The operation immediately terminates.

Bit 6 *Protect check.* When set to one, this bit indicates that the attachment attempted to access a main storage location and presented an incorrect address key.

Bit 7 *Interface data check.* When set to one, this bit indicates that a parity error is detected on the I/O interface during a cycle steal data transfer. The operation immediately terminates.

Appendix A. Operate I/O and DPC Operations

Operate I/O

The processor initiates I/O operations by issuing an Operate I/O instruction, and then uses the processor I/O channel to transfer data to and from the attachment. The Operate I/O instruction is a privileged instruction. Its effective address (the combination of the R2 and address fields) points to an immediate device control block (IDCB) in main storage. The IDCB contains an I/O command, a device address, and an immediate-data field. See Figure A-1. The command defines the type of I/O operation; the device address identifies the device on which the operation is to be performed. The use of the information in the immediate data field depends on the mode of operation. For direct program control (DPC) operations, the immediate-data field is used as a data word; for cycle-steal operations, this field points to a device control block (DCB) that contains additional information needed to perform the operation. The IDCB must be on a fullword boundary. Refer to the *IBM Series/1 4955 Processor and Processor Features Description*, GA34-0021 or the *IBM Series/1 4953 Processor and Processor Features Description*, GA34-0022, for a more detailed description.

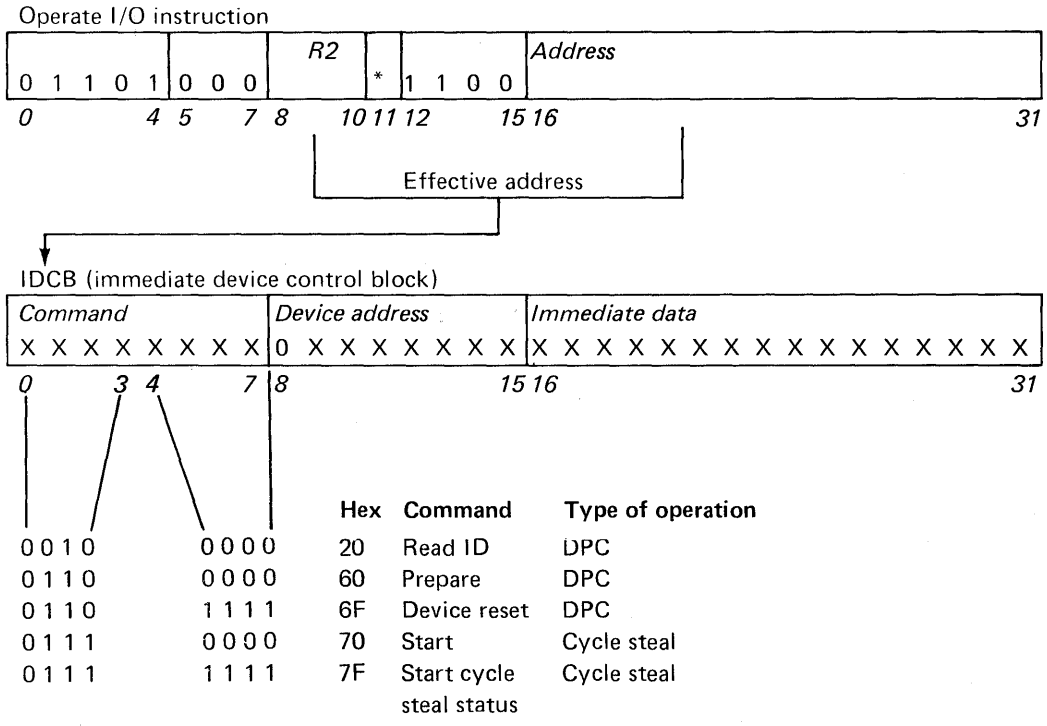


Figure A-1. Operate I/O instruction and IDCB formats

Direct Program Control (DPC)

A command executed under direct program control causes an immediate transfer of data or control information to or from the attachment. This attachment recognizes only the following DPC-type commands:

Command	Hex	IDCB Immediate Data Field Contents
Read ID	20	Device ID word
Prepare	60	Interrupt parameters
Device Reset	6F	Zeros

An Operate I/O instruction must be executed for each of the above commands. Each execution consists of the following events (see Figure A-2).

1. The Operate I/O instruction points to an IDCB in main storage. 1
2. The attachment uses the IDCB's device-address field 3 to determine its address, and the command field 2 to determine the operation to perform.
3. The processor transfers the contents of the immediate-data field to the attachment, or transfers information from the attachment to the immediate-data field, depending on the command being executed. 4
4. The attachment sends a condition code to the level status register (LSR) in the processor. 5

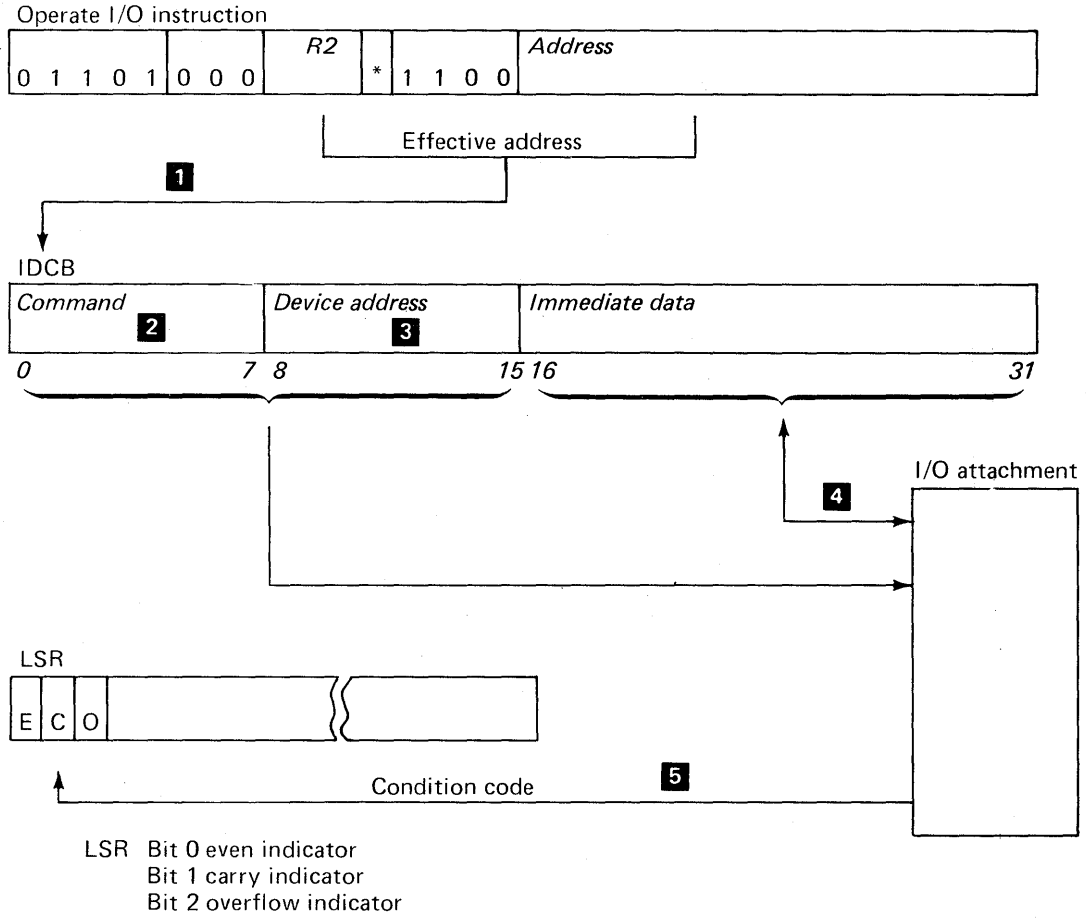


Figure A-2. Direct program control I/O operation

Read ID Command

The Read ID command transfers an identification (ID) word from the attachment to the immediate-data field of the IDCB. For this attachment, the ID word is X'0F06'.

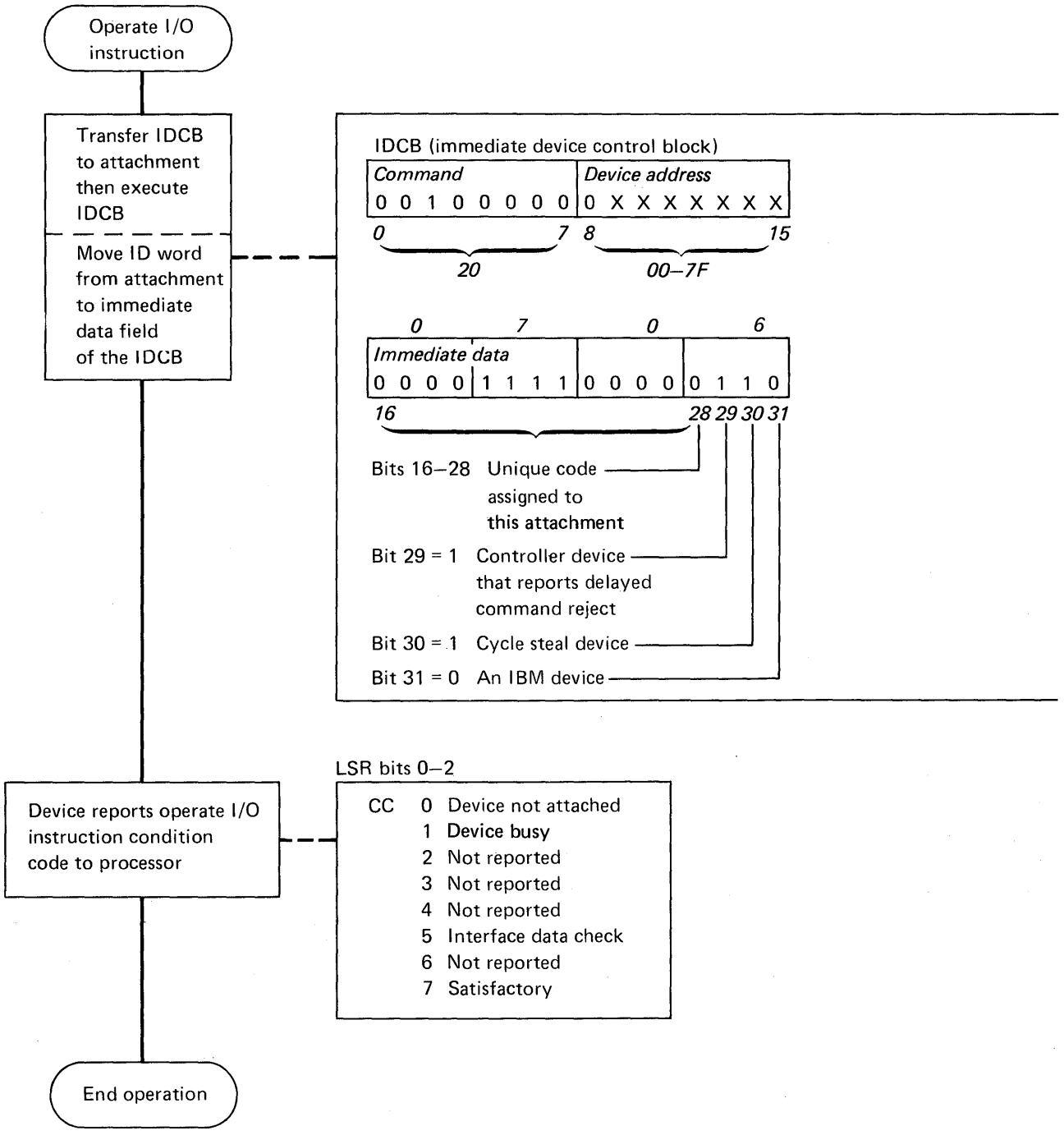


Figure A-3. Read ID command operation

Prepare Command

Before the attachment can request interrupts, the processor must supply interrupt parameters. The user places these parameters in the IDCB's immediate-data field. The Prepare command transfers the parameters to the attachment. The parameters include an interrupt-enable bit to control whether or not the device is allowed to interrupt, and the priority-interrupt level to which the attachment requests interrupt service.

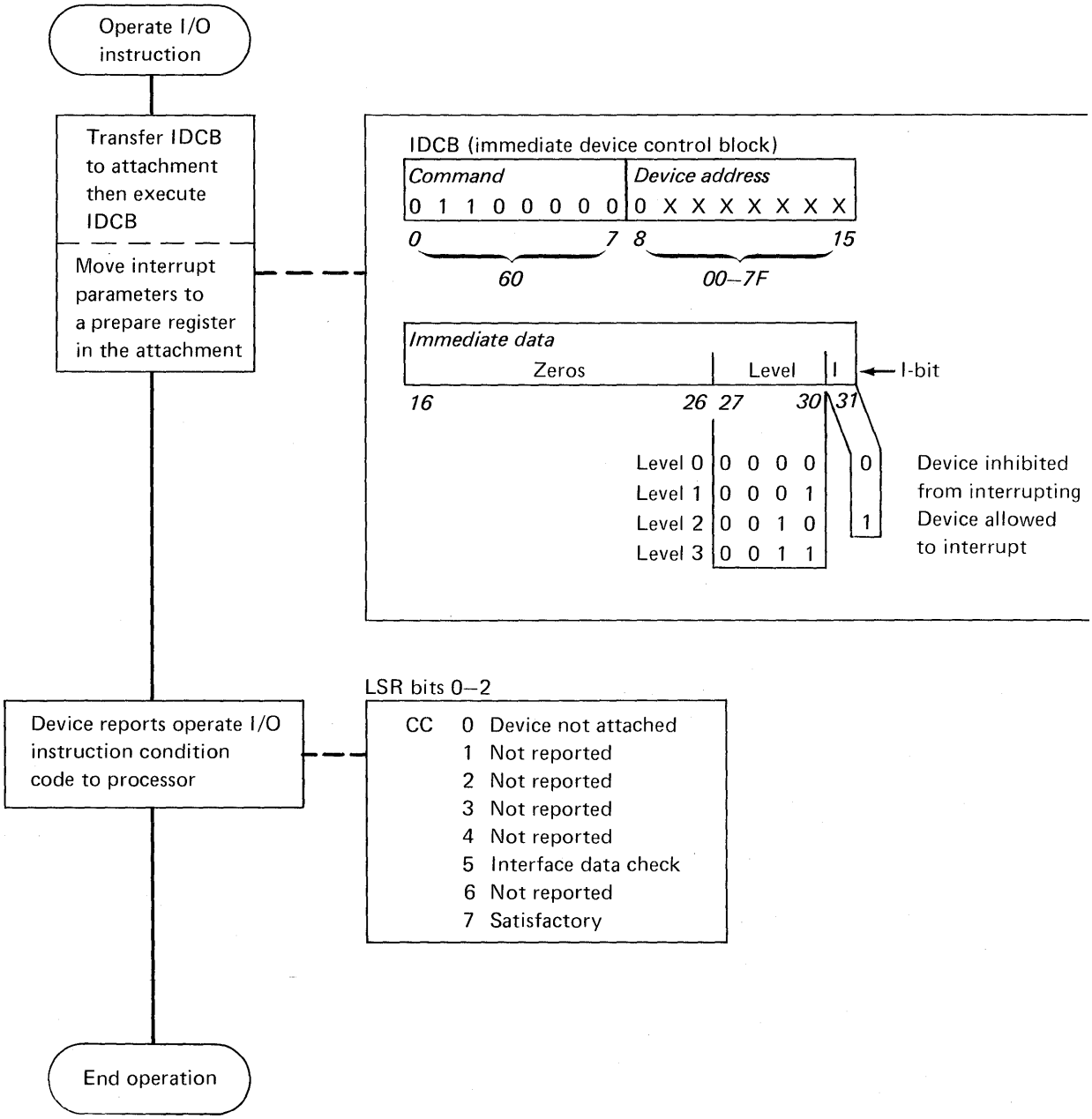


Figure A-4. Prepare command operation

Device Reset Command

The Device Reset command resets the addressed attachment. Any pending interrupt or busy condition is cleared. The device interrupt-enable bit, the assigned priority level, and the residual address (cycle steal status word 0) are not affected.

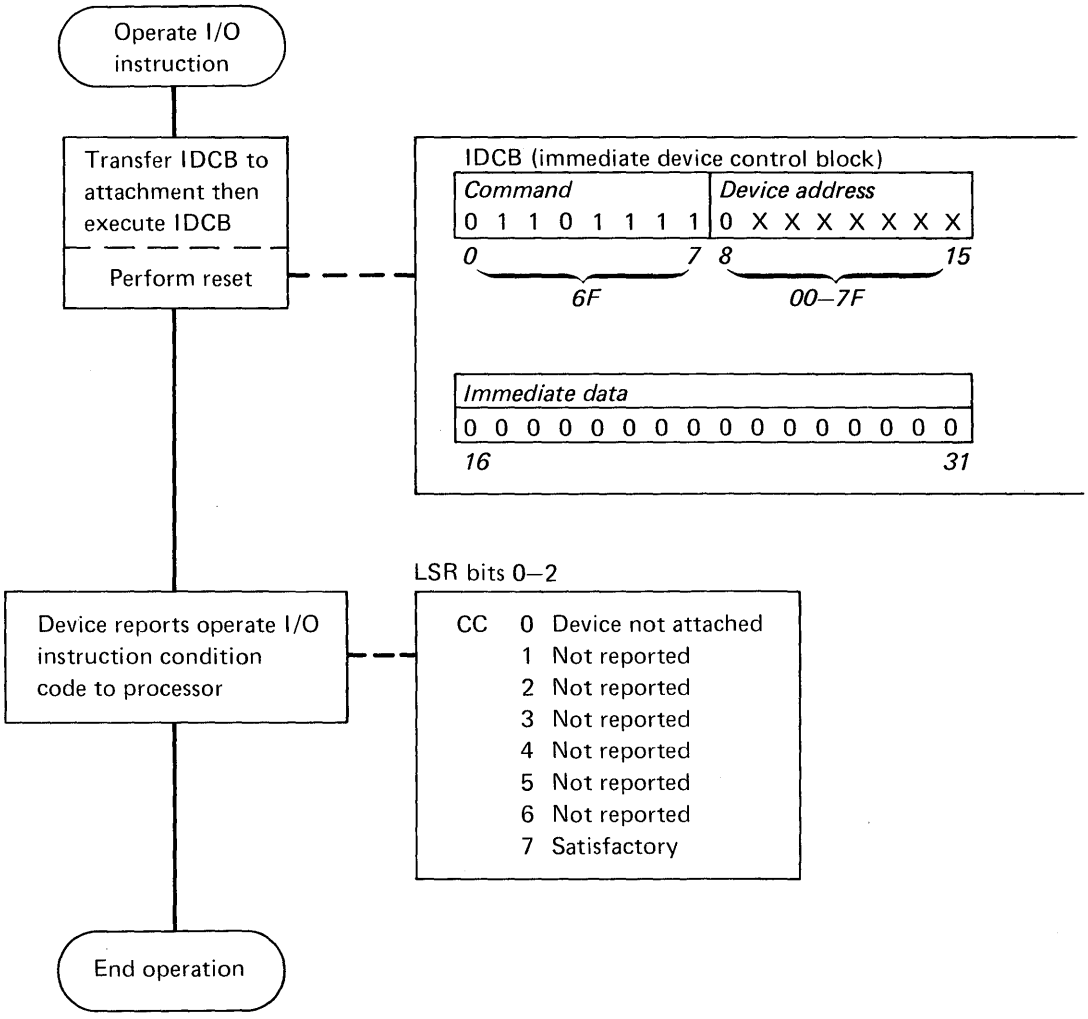


Figure A-5. Device reset command operation

Appendix B. Diagnostic Commands

Diagnostic commands are used to verify correct operation of the Series/1 to Series/1 Attachment. These commands are executed during the diagnostic MAP sequence and provide actual attachment internal testing results. The following commands compose the diagnostic command group.

Diagnostic 1

This command causes an internal microdiagnostic test to be performed on the microprocessor, the memory modules, and the Series/1 interface modules.

Diagnostic 2

This command causes an internal microdiagnostic test to be performed on the device-dependent logic which is associated with the Series/1 to Series/1 Attachment operation.

Diagnostic 3

This command causes a microdiagnostic test to be performed on the Series/1 to Series/1 Attachment driver/receiver modules. This test manipulates actual bus signal lines and should be used only with the Series/1 to Series/1 Attachment cable disconnected.

Diagnostic 4

This command causes a microdiagnostic test to be performed on the Series/1 to Series/1 Attachment associated cable. This test requires that the attachment cable be disconnected from the secondary Series/1 and instead be connected to a cable wrap connector.

Diagnostic Read Jumpers

This diagnostic command is used to confirm that the jumpers have been installed correctly on the attachment card.

Diagnostic Patch Command

This command is used to modify attachment storage.

Note: Since this command will modify the attachment function, it should be used only under direct authorization of Series/1 product engineering, General Systems Division of the IBM Corporation.

Diagnostic Command Structure

These commands operate under the cycle steal mode and should be generated and executed as described in the cycle steal portion of this document. The DCB structure should be as follows:

Word	
0	Control word
1	Reserved (must = 0)
2	Reserved (must = 0)
3	Reserved (must = 0)
4	Reserved (must = 0)
5	Reserved (must = 0)
6	Byte count
7	Data address

DCB Word 0—Control Word

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	0	0	Addr key			0	0	0	Diag. operation				

Bit 0 This bit is not used and must be zero.

Bit 1 This bit is not used and must be zero.

Bit 2 Input flag (IF). This bit is used and must be one.

Bit 3 This bit is not used and must be zero.

Bit 4	This bit is not used and must be zero.
Bits 5–7	Cycle steal address key. This is a program-assigned 3-bit processor storage protect access key used by the attachment during data transfers for storage access authorization.
Bit 8	This bit is not used and must be zero.
Bit 9	This bit is not used and must be zero.
Bit 10	This bit is not used and must be zero.
Bits 11–15	Identify the diagnostic operation to be performed: 11010 Diagnostic Read Jumper 11011 Diagnostic Patch Command 11100 Diagnostic 1 11101 Diagnostic 2 11110 Diagnostic 3 11111 Diagnostic 4

DCB Word 1—Not Used, Must be Zero

DCB Word 2—Not Used, Must be Zero

DCB Word 3—Not Used, Must be Zero

DCB Word 4—Not Used, Must be Zero

DCB Word 5—Not Used, Must be Zero

DCB Word 6—Byte Count

The following hex codes are required for the associated command. All other codes will result in a DCB specification check.

Diagnostic 1	X'000C'
Diagnostic 2	X'0004'
Diagnostic 3	X'0004'
Diagnostic 4	X'0004'
Diagnostic Read Jumper	X'0002'
Diagnostic Patch	X'XXXX'

DCB Word 7—Data Address

The data address word contains the starting main storage address for the data transfer. This starting address must be located on an even word boundary in Series/1 main storage.

Diagnostic Command Results

After completion of a diagnostic command, the microdiagnostic testing results can be interpreted to determine correct functional operation. The results of each diagnostic command are as follows.

Diagnostic 1

Yields six words of status in the following format:

Word 1—Channel Test Word 1
- Pass—X'5555'
- Fail—X'D555'

Word 2—Channel Test Word 2
- Pass—X'AAAA'
- Fail—X'2AAA'

Word 3—Memory Module 1 Test
- Pass—Part number of memory module 1
- Fail—X'FXXX'

Word 4—Memory Module 2 Test
- Pass—Part number of memory module 2
- Fail—XFXXX'

Word 5—Memory Module 3 Test
- Pass—Part number of memory module 3
- Fail—X'FXXX'

Word 6—Memory Test Results on Module 4
- Pass—X'0000'
- Fail—X'XXXX' (non-zero)

Diagnostic 2

Yields two words of status in the following format:

Word 1—Device Logic Test Word 1
- Pass—X'0000'
- Fail—X'1XXX'

Word 2—Device Logic Test Word 2
- Pass—X'0000'
- Fail—X'1XXX'

Diagnostic 3

Yields two words of status in the following format:

Word 1—Device Logic Test Word 1
- Pass—X'0000'
- Fail—X'1XXX'

Word 2—Device Logic Test Word 2
- Pass—X'0000'
- Fail—X'XXXX'

Diagnostic 4

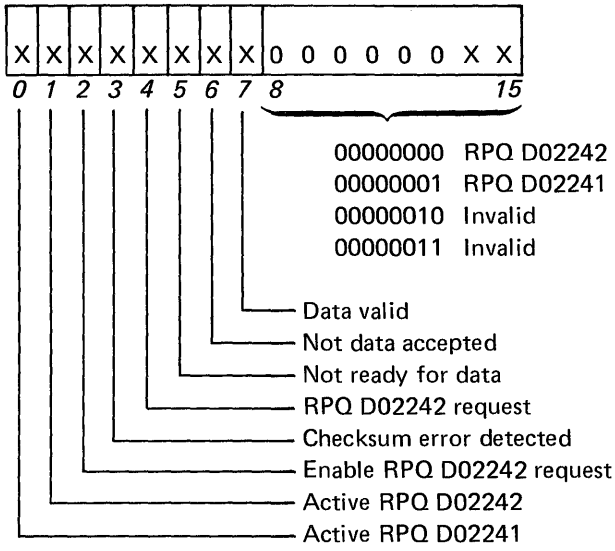
Yields two words of status in the following format:

Word 1—Device Logic Test Word 1
Pass—X'0000'
Fail—X'1XXX'

Word 2—Device Logic Test Word 2
Pass—X'0000'
Fail—X'XXXX'

Diagnostic Read Jumper

Yields one word of status in the following format:



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