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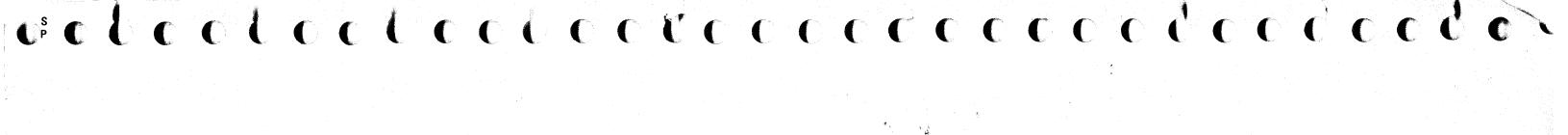
INDEX MLX LGND START FSI MSG SENSE MICRO	OLT OPER PANEL CTL-I	DEV-I DATA
VOL. R01	VOL. R02	VOL.

Volumes R01 through R06 accompany each Control Module and support all 3350s attached.

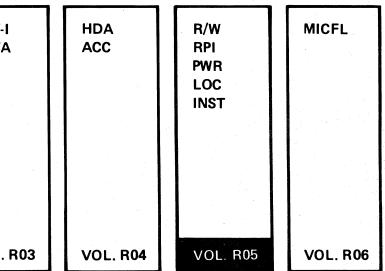
Disk Storage

EA0000 2358632 441300 3350 31 Mar 76 Seq. 1 of 2 Part No.

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## **Maintenance Information**



## PREFACE

#### MAINTENANCE INFORMATION MANUAL ORDERING PROCEDURE (IBM Internal)

Individual pages of the 3350 Maintenance Information Manual can be ordered from the San Jose plant by using the Wiring Diagram/Logic Page Request (Order No. 120-1679). In the columns headed "Logic Page" enter the page identifier information: sequence number, sheet number, part number, and EC number. Groups of pages can be ordered by including a description (section, volume, etc.) and the machine serial number.

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	3350	EA0000 Seq. 2 of 2	<b>2358632</b> Part No.	441300 31 Mar 76				
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## SAFETY

#### **CE SAFETY PRACTICES**

All Customer Engineers are expected to take every safety precaution possible and observe the following safety practices while maintaining IBM equipment:

- 1. You should not work alone under hazardous conditions or around equipment with dangerous voltage. Always advise your manager if you MUST work alone.
- Remove all power, ac and dc, when removing or assembling major components, working in immediate areas of power supplies, performing mechanical inspection of power supplies, or installing changes in machine circuitry.
- After turning off wall box power switch, lock it in the Off position or tag it with a "Do Not Operate" tag, Form 229-1266. Pull power supply cord whenever possible.
- 4. When it is absolutely necessary to work on equipment having exposed operating mechanical parts or exposed live electrical circuitry anywhere in the machine, observe the following precautions:
- a. Another person familiar with power off controls must be in immediate vicinity.
- b. Do not wear rings, wrist watches, chains, bracelets, or metal cuff links.
- c. Use only insulated pliers and screwdrivers.
- d. Keep one hand in pocket.
- When using test instruments, be certain that controls are set correctly and that insulated probes of proper capacity are used.
- f. Avoid contacting ground potential (metal floor strips, machine frames, etc.). Use suitable rubber mats, purchased locally if necessary.
- 5. Wear safety glasses when:
- a. Using a hammer to drive pins, riveting, staking, etc.
- b. Power or hand drilling, reaming, grinding, etc.
- c. Using spring hooks, attaching springs.
- d. Soldering, wire cutting, removing steel bands.
- e. Cleaning parts with solvents, sprays, cleaners, chemicals, etc.
- Performing any other work that may be hazardous to your eyes. REMEMBER – THEY ARE YOUR EYES.
- 6. Follow special safety instructions when performing specialized tasks, such as handling cathode ray tubes and extremely high voltages. These instructions are outlined in CEMs and the safety portion of the maintenance manuals.
- 7. Do not use solvents, chemicals, greases, or oils that have not been approved by IBM.
- Avoid using tools or test equipment that have not been approved by IBM.
- 9. Replace worn or broken tools and test equipment.
- 10. Lift by standing or pushing up with stronger leg muscles this takes strain off back muscles. Do not lift any equipment or parts weighing over 60 pounds.
- 11. After maintenance, restore all safety devices, such as guards, shields, signs, and grounding wires.
- 12. Each Customer Engineer is responsible to be certain that no action on his part renders products unsafe or exposes customer personnel to hazards.
- Place removed machine covers in a safe out-of-the-way place where no one can trip over them.
- 14. Ensure that all machine covers are in place before returning machine to customer.
- Always place CE tool kit away from walk areas where no one can trip over it; for example, under desk or table.

- 16. Avoid touching moving mechanical parts when lubricating, checking for play, etc.
- 17. When using stroboscope, do not touch ANYTHING it may be moving.
- Avoid wearing loose clothing that may be caught in machinery. Shirt sleeves must be left buttoned or rolled above the elbow.
- Ties must be tucked in shirt or have a tie clasp (preferably nonconductive) approximately 3 inches from end. Tie chains are not recommended.
- 20. Before starting equipment, make certain fellow CEs and customer personnel are not in a hazardous position.
- 21. Maintain good housekeeping in area of machine while performing and after completing maintenance.
  - Knowing safety rules is not enough. An unsafe act will inevitably lead to an accident. Use good judgment - eliminate unsafe acts.

#### **ARTIFICIAL RESPIRATION**

#### **General Considerations**

- Start Immediately Seconds Count Do not move victim unless absolutely necessary to remove from danger. Do not wait or look for help or stop to loosen clothing, warm the victim, or apply stimulants.
- 2. Check Mouth for Obstructions
- Remove foreign objects.
- 3. After victim is breathing by himself or when help is available:
  - a. Loosen clothing.
  - b. Place victim on his side, c. Keep victim warm
- 4. Remain in Position
- After victim revives, be ready to resume respiration if necessary.
- 5. Call a Doctor
- Have someone summon medical aid.
- Don't Give Up Continue without interruption until victim is breathing without help or is certainly dead.

#### **Rescue Breathing for Adults**

 Place victim on back; lift neck and tilt head way back. (Quickly remove any noticeable food or objects from mouth.)



2. Pinch nose closed; make airtight seal around victim's mouth with your mouth; and forcefully breathe into victim until chest rises (expands).



- 3. Continue breathing for the victim 12 times per minute WITHOUT STOPPING.
- 4. If chest does not rise (expand), roll victim onto side and pound firmly between shoulder blades to remove blocking material. Also, try lifting jaw higher with your fingers. Resume rescue breathing.

PREFACE/SAFETY

## **R/W CONTENTS**

R/W SAFETY MAPS	R/W 100 - 287
R/W DATA MAPS Data Checks Data Check Sense Byte	R/W 300 - 378
Analysis	
Read Home Address (Read G1 – Tag '0E' Bus '4E')	R/W 360
READ HA SEQUENCE CHART.	R/W 362 - 364
READ DATA CABLE DIAGRAM	R/W 370
HDA CABLE CHECK PROCEDURE	R/W 372
HDA VOLTAGE CHECK PROCEDURE	R/W 376
BASE PLATE GROUND CHECK PROCEDURE	R/W 378
ADDRESS CONVERSION	R/W 400 - 415
TROUBLE NOT FOUND	<b>R/W 990</b> - 995

#### **REFERENCE TO OTHER SECTIONS**

HDA Cable Swap Procedure. . HDA 713 Read/Write Operation . . . . OPER 210 - 236

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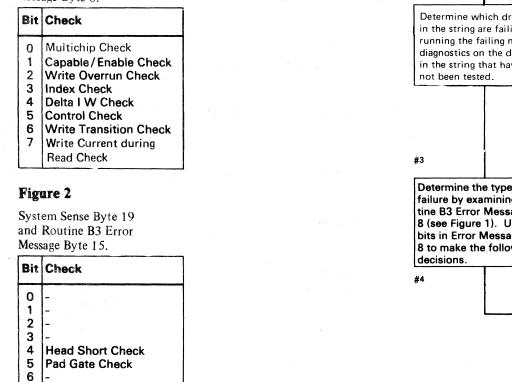


## **READ/WRITE CHECK**

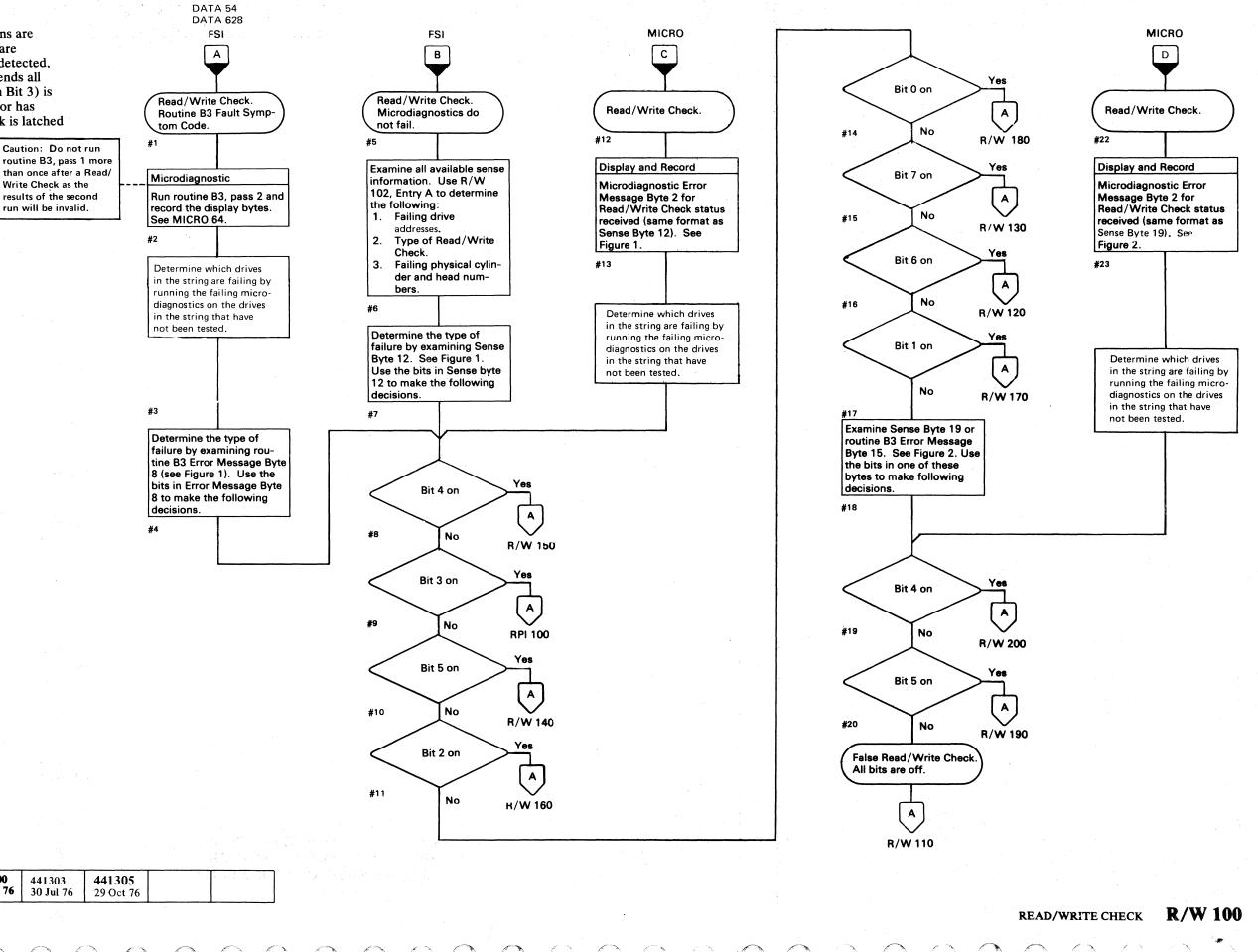
During Write operations, all safety conditions are monitored to ensure that all Write controls are functioning correctly. If a Safety Check is detected, Read/Write Safe is deactivated which suspends all further writing. Read/Write Check (Bus In Bit 3) is activated to signal the controller that an error has occurred and the type of Read/Write Check is latched for further sensing. Caution: Do not run

#### Figure 1

System Sense Byte 12 (Format 1) and Routine B3 Error Message Byte 8.



Write Check as the



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3350	EC0001 Seq. 2 of 2	<b>2358189</b> Part No.	441300 31 Mar 76	441303 30 Jul 76	<b>441305</b> 29 Oct 76		e vil die Re

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#### READ/WRITE CHECK **R/W 100**

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## **READ/WRITE CHECK SENSE BYTE ANALYSIS**

#### **Read/Write Checks**

- Sense Byte 8, bit 3 active indicates a Read/Write Check. The Read/Write Check is further defined by Sense Bytes 12 and 19. See Figure 1.
- A Read/Write Check causes a Fault Symptom Code to be developed from Sense Bytes 8, 12, and 19. The Fault Symptom Code is then placed in Sense Bytes 22 and 23.

If Sense Bytes 12 and 19 are both '00', Fault Symptom Code 1400 is developed.

If Sense Byte 12 = '00' and Sense Byte 19, bits 4 or 5 are active, Fault Symptom Code 14F4 or 14F8 is developed.

If Sense Byte 12 = '01' to 'FF', Fault Symptom Code 14XX is developed (XX = value of Sense)Byte 12).

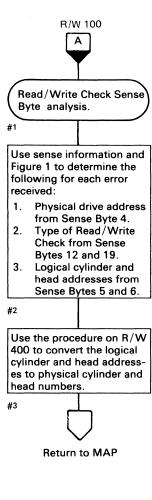
#### **Physical Drive Address**

Sense Byte 4 contains the bit significant drive address but does not indicate the string on multistring subsystems (see Figure 1). The string must be determined from the logical unit address.

#### **Cylinder And Head Address**

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The logical cylinder and head addresses can be determined from Sense Bytes 5 and 6. See R/W 400 to convert logical cylinder and head addresses to physical cylinder and head numbers.



	Figur	e 1.	Sense	e Byt	e Def	initio	ons												****					
			1		Г	1	<u>т</u>				e Byte						[		1	<u> </u>				
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
					Phy Addr	Cyl Addr Lo		For- mat	*				R/W Chk							R/W Chk			Fault Symp Code	otom
							i ii	Sense Indicate Theck.				ve ,							F					
Sense Byte 4	Physi	cal Dr	ive					ļ		Bit	С	heck			Carloghacystics, without office	9800 A 8798 8800				Bit	c	heck		
in Hex		ddress			i			0 Multichip Check						0			-							
80		0						Į		1 Capable/Enable Check						1		-						
40 .		1			i			\$		2 Write Overrun Check						2			-					
20		2						ļ		3 Index Check						3			_					
10		3			į			I		4 Delta I W Check						4	F	lead S	hort C	heck				
08		4			 			1		5 Control Check						5	P	ad Ga	te Che	eck				
04		5			į					6	V	Vrite <sup>-</sup>	Fransit	ion Cl	heck					6				
02		6		Ī						7	V	Vrite (	Curren	t Duri	ing Re	ad Ch	eck			7		-		
01		7		/					ļ										1.000					
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Sense Byte 5 Cy	linder A	Addres	ss Lo			ſ			Τ			Ser	nse By	te 6										
128 64 32	2 16	8	4	2	1		Μ	ode		Cylind	er Add	ress H	li	Hea	d Adc	lress								
							3350 3330			-	Cyl 512		Cyl 256	16		8	4		2	1				
							3330	⊦1.			- Cyl 256			16		8	4		2	1				

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#### READ/WRITE CHECK SENSE BYTE ANALYSIS **R/W 102**

READ/WRITE CHECK SENSE BYTE ANALYSIS **R/W 102** 

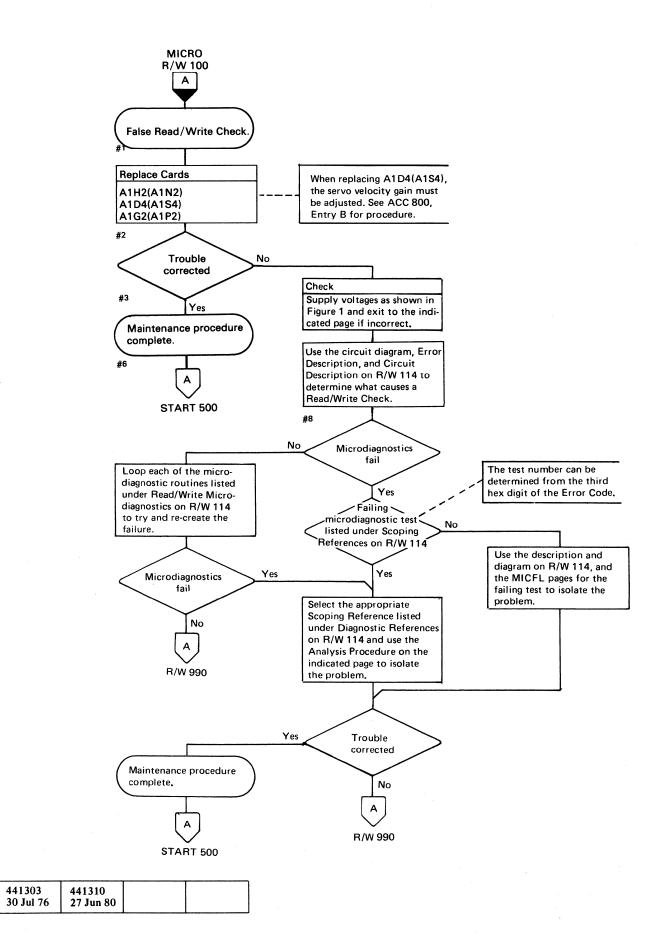


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#### **READ/WRITE CHECK**





3350

EC0110

Seq. 1 of 2

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Part No.

441300

31 Mar 76

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READ/WRITE CHECK **R/W 110** 

Test Point	Tolerance	Maximum** AC Ripple	Page Entry
A1C2 (A1T2) B06(-) to A1K2D08(+) A1F2 (A1Q2) B11(+) to A1F2 (A1Q2) D08(-)	-3.85 to -4.50 ∨ +5.76 to +6.24 ∨		PWR 255, A PWR 260, A
digital voltmeter to check voltages.			00145

\* Use a digital voltmeter to check voltages.

Figure 1. Drive Voltage

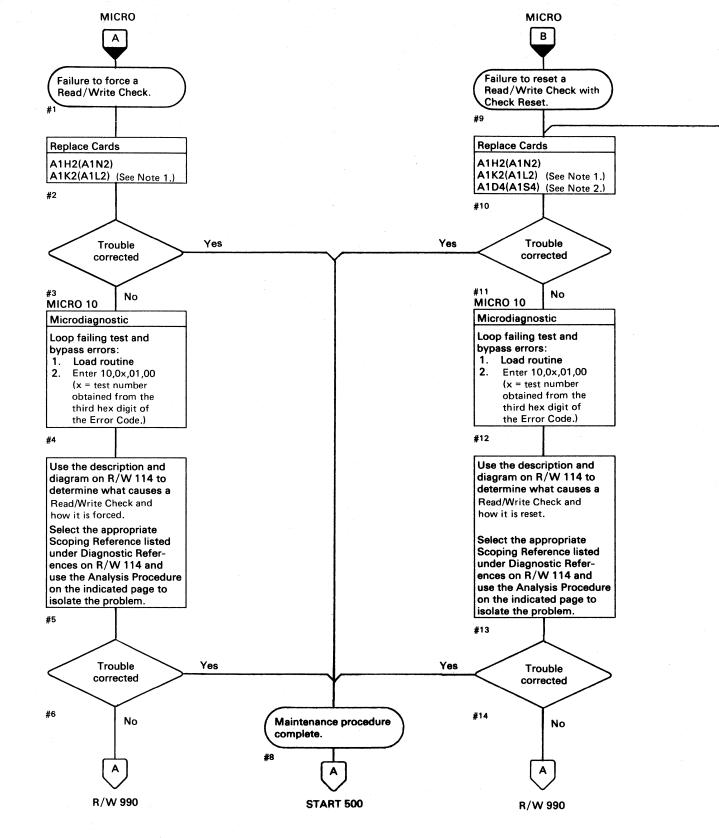
Voltage\*

-4 V +6 V

\*\* Use a scope to measure the ripple. See PWR 290 for the procedure.

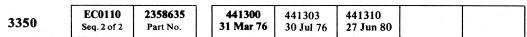
READ/WRITE CHECK **R/W 110** 

#### **READ/WRITE CHECK**

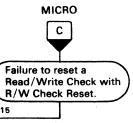


Note 1. When replacing A1K2(A1L2), check the addressing jumpers. See INST 6.

Note 2: When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.



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#### READ/WRITE CHECK **R/W 112**

#### **READ/WRITE CHECK**

#### **Error Description**

Read/Write Check is a drive failure indicating that an unsafe condition occurred during a Read or Write operation. Read/Write Check is sent to the controller on Inbus bit 3 when:

- Set Read/Write is active.
- A drive tag that senses drive status is active. See OPER 100 and 101.

#### Force Read/Write Check

Read/Write Check is forced on when any one of the checks A is forced. Microdiagnostic routine B8, test F is the first test in the linked series of microdiagnostics that forces Read/Write Check. Test D forces Capable/Enable Check which in turn forces Read/Write Check. Tests in microdiagnostic routines A5 and AD force Read/Write Check using the other check conditions A.

#### **Reset Read/Write Check**

Read/Write Check is reset when the check condition that is causing the Read/Write Check is reset. The check conditions are reset by:

Check Reset. Read/Write Reset. Pwr On CE Reset.

#### **Circuit Description**

Read/Write Check is activated when one of eleven unsafe conditions (A) is active. Each of these unsafe conditions is sensed separately by either a Sense Read/Write or a Sense Status 0 drive tag. When Read/Write Check is active and the eleven unsafe conditions are sensed and found to be inactive, the Read/Write Check is false.

#### **Diagnostic References**

#### **READ/WRITE MICRODIAGNOSTICS**

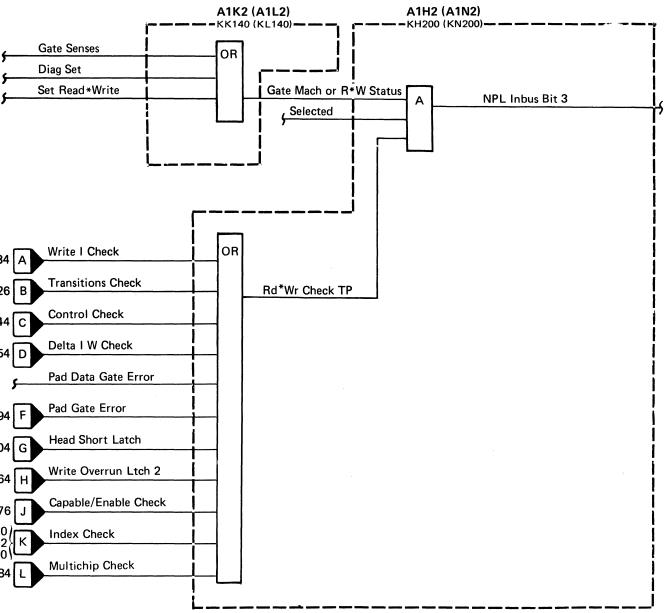
The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

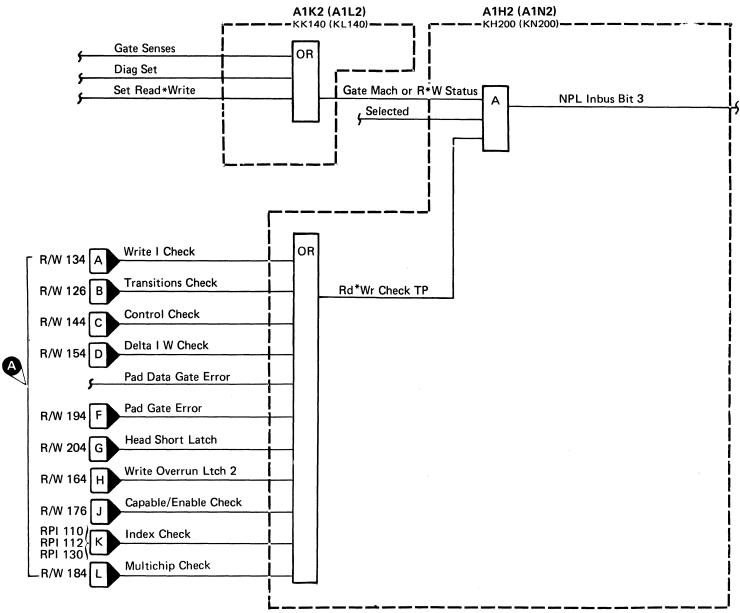
Routine A5	(MICFL 130)
Routine AD	(MICFL 240)
Routine AF	(MICFL 320)
Routine B2	(MICFL 380)
Routine B8	(MICFL 630)
Routine BB	(MICFL 740)

#### SCOPING REFERENCES

Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5, test 3	(R/W 250)
Routine AD, test 1	(R/W 260)
Routine AD, test 8	(R/W 266)
Routine AD, test 9	(R/W 270)
Routine B8, test D	(R/W 276)
Routine B8, test F	(R/W 280)
Routine BB, test 1	(R/W 286)



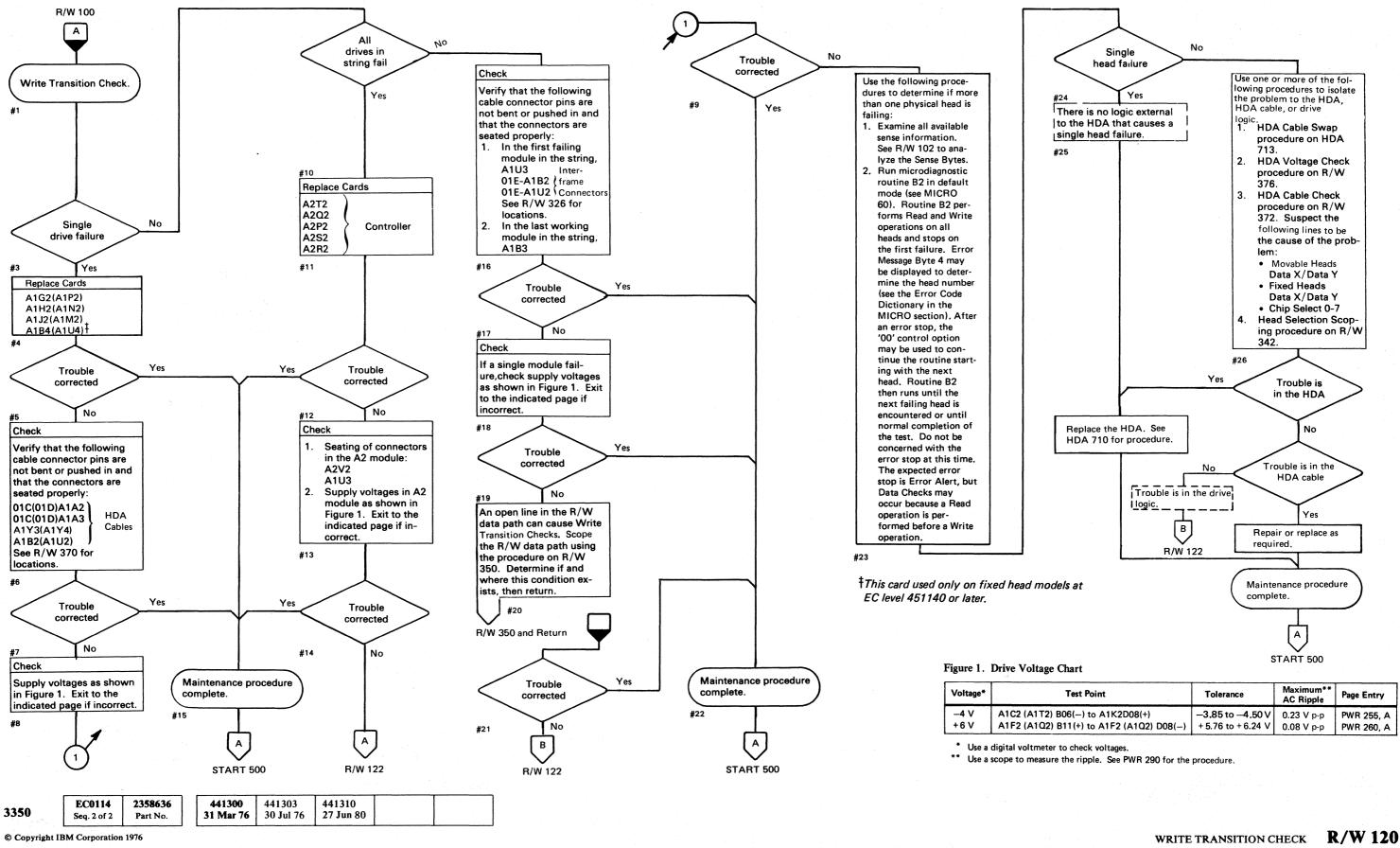


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#### READ/WRITE CHECK **R/W 114**

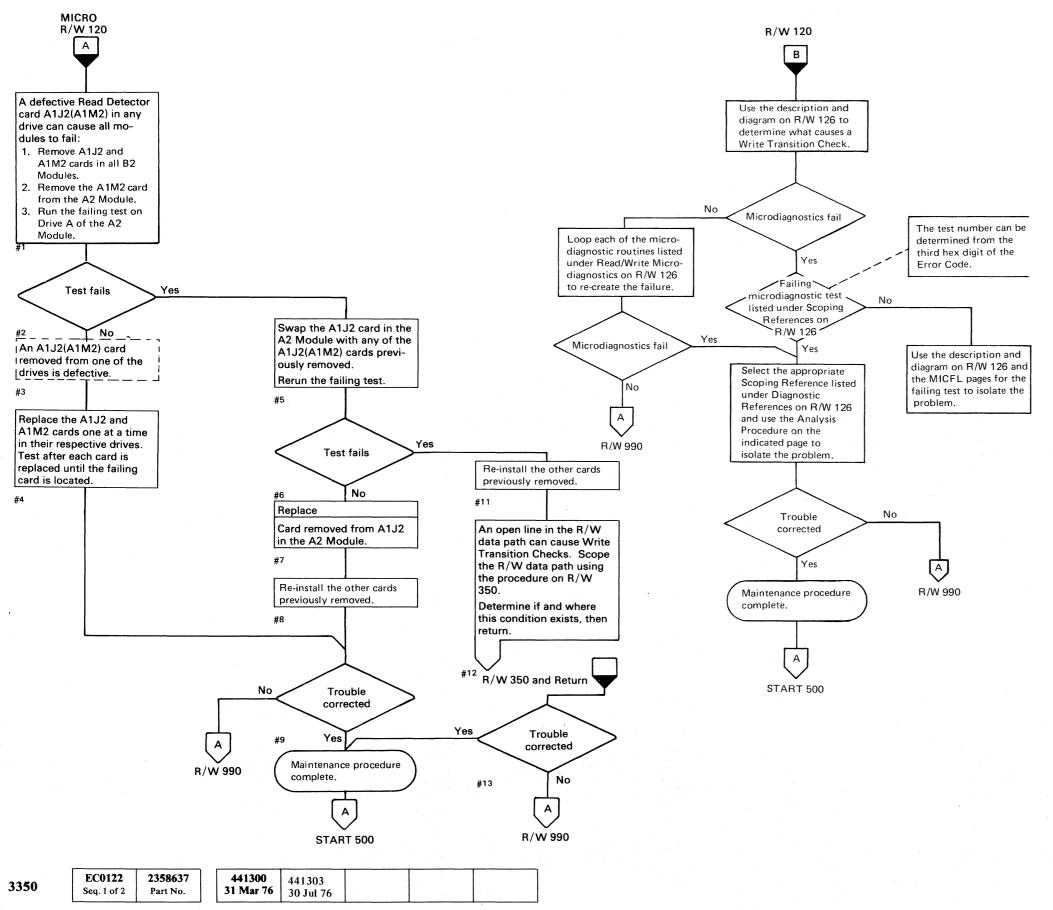
#### READ/WRITE CHECK **R/W 114**

#### WRITE TRANSITION CHECK



Test Point	Tolerance	Maximum** AC Ripple	Page Entry
806() to A1K2D08(+)	-3.85 to -4.50 V		PWR 255, A
811(+) to A1F2 (A1Q2) D08()	+ 5.76 to + 6.24 V		PWR 260, A

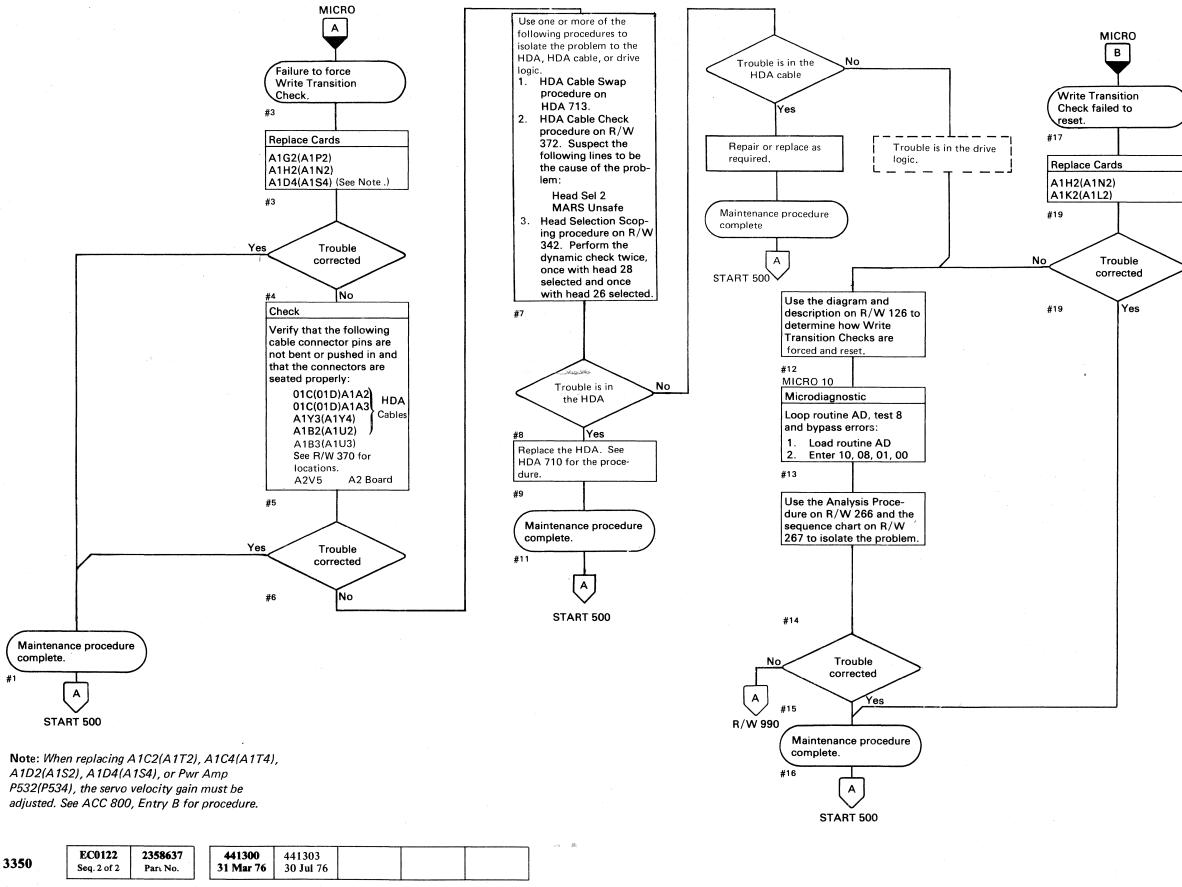
#### WRITE TRANSITION CHECK



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#### WRITE TRANSITION CHECK **R/W 122**

#### WRITE TRANSITION CHECK



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#### WRITE TRANSITION CHECK R/W 124

When replacing A1K2(A1L2), check the addressing jumpers. See INST 6. #20

#### WRITE TRANSITION CHECK

#### **Error Description**

Write Transition Check indicates that Write Transitions were not detected within 8 microseconds after Write Gate Control is turned on. Each of the following conditions must exist for Write Transitions to occur:

Head is selected. Write Select is active. Write Current is active. Write Data is active.

Write Transition Checks can be caused by a control line failure or an open data path. These failures can be in the controller logic, drive logic, or in the HDA.

#### **Circuit Description**

Write Transition errors are detected in the HDA and transferred to the Write Transition Check latch in the drive on the MARS Unsafe line. Write Transition Check activates Read/Write Check which causes the controller to send Error Alert to the storage control. Write Transition Check is indicated to the storage control by Inbus Bit 6 being active during a Sense Read/Write operation. See OPER 101.

#### **Force Write Transition Check**

Microdiagnostic routine AD, test 8 forces Write Transition Check by selecting an invalid head and then activating Write Gate. The Head Address Register is set to '3C' (this activates Chip Select 7 and Head Select 2) in an attempt to select physical head 30 (a non-existent head). The HDA logic activates Unsafe Current which causes the Write Transition Check latch to set.

#### **Reset Write Transition Check**

The Write Transition Check latch is reset by the following:

> Check Reset. Rd\*Wr Reset. Pwr On CE Reset.

#### **Diagnostic References**

#### **READ/WRITE MICRODIAGNOSTICS**

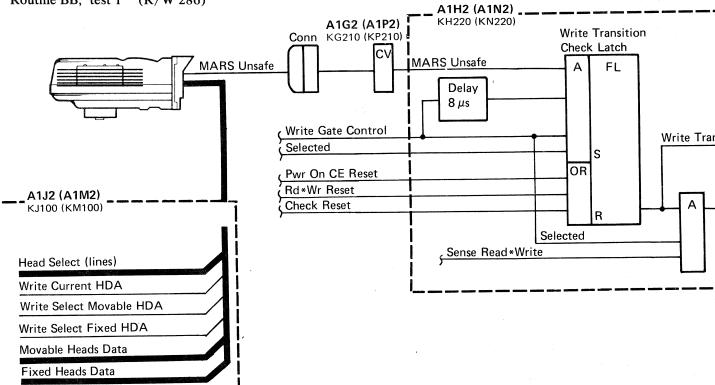
The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

Routine A5	(MICFL 130)
Routine AD	(MICFL 240)
Routine AF	(MICFL 320)
Routine B2	(MICFL 380)
Routine B8	(MICFL 630)
Routine BB	(MICFL 740)

SCOPING REFERENCES

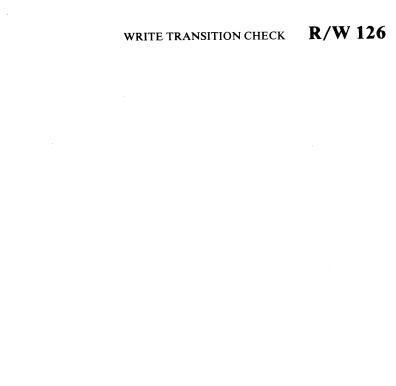
Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5, test 3	(R/W 250)
Routine AD, test 1	(R/W 260)
Routine AD, test 8	(R/W 266)
Routine AD, test 9	(R/W 270)
Routine B8, test D	(R/W 276)
Routine B8, test F	(R/W 280)
Routine BB, test 1	(R/W 286)



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ansition Check	B R/W 114
	NPL Inbus Bit 6 (Write Transition Check)
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#### WRITE CURRENT DURING READ CHECK (Write I Check)

Α

Read Check.

#2

#3

Check

#5

Check

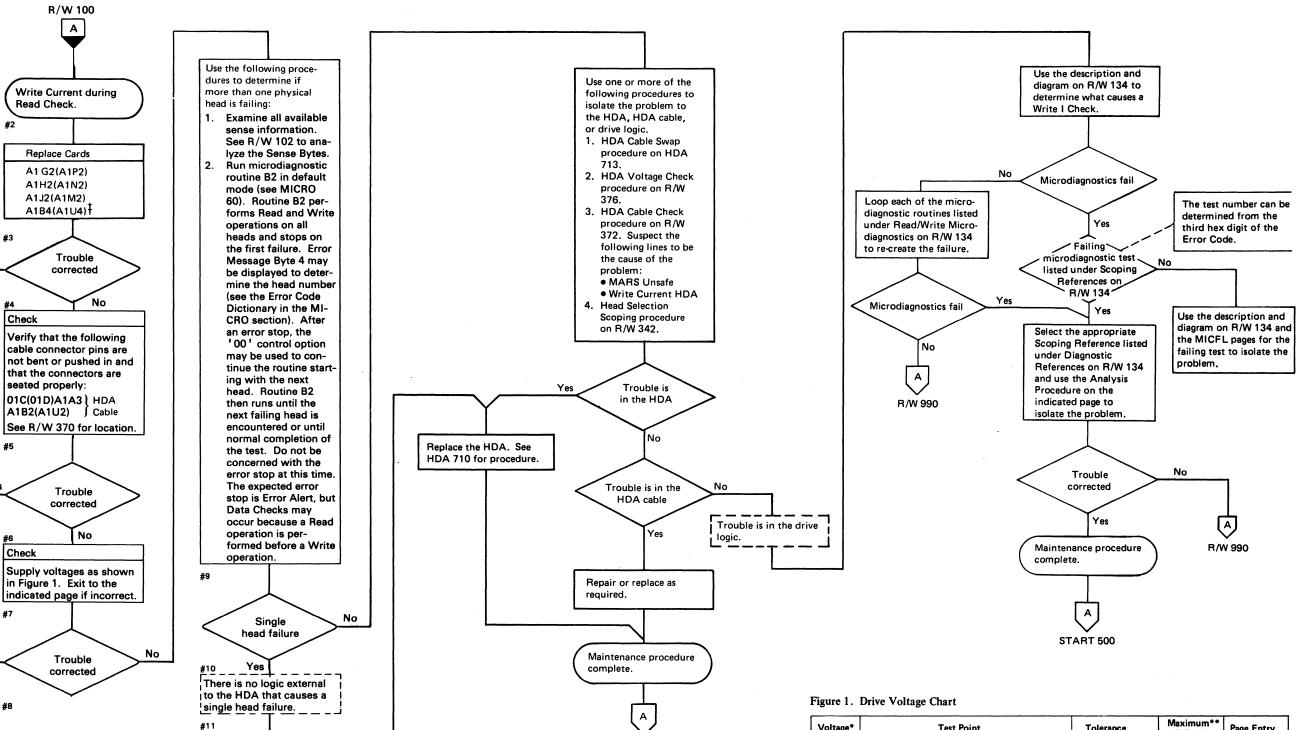
#7

#8

Yes

Yes

Yes



START 500

Voltage*	Test Point	Tolerance	Maximum** AC Ripple	Page Entry
-4 V	A1C2 (A1T2) B06(-) to A1K2D08(+)	-3.85 to -4.50 V	0.23 V p-p	PWR 255, A
+6 V	A1F2 (A1Q2) B11(+) to A1F2 (A1Q2) D08(-)	+ 5.76 to + 6.24 V	0.08 V p-p	PWR 260, A

Use a digital voltmeter to check voltages.

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**†**This card used only on fixed head models at EC level 451140 or later.

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Maintenance procedure

A

START 500

complete.

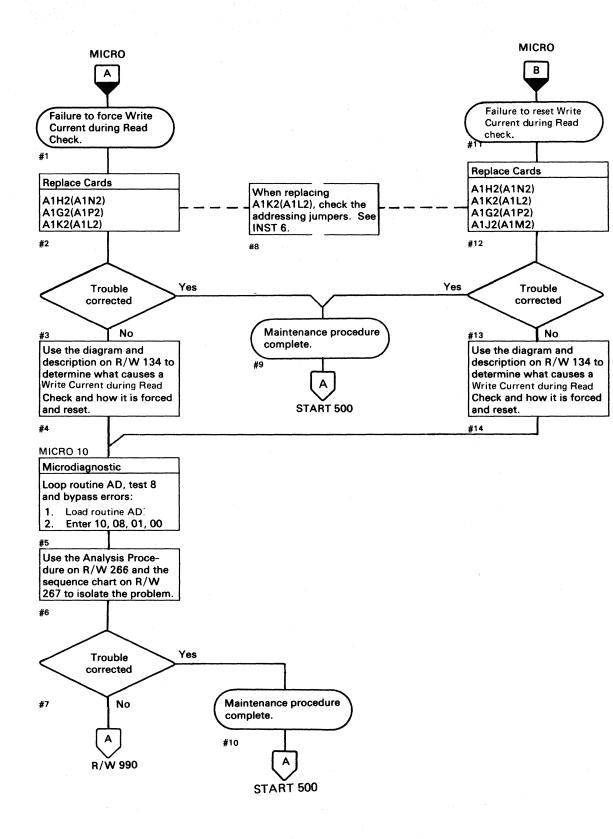
#### WRITE CURRENT DURING READ CHECK (Write I Check) R/W 130

\*\* Use a scope to measure the ripple. See PWR 290 for the procedure.

WRITE CURRENT DURING READ CHECK (Write I Check)

**R/W 130** 

#### WRITE CURRENT DURING READ CHECK (Write I Check)



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WRITE CURRENT DURING READ CHECK (Write I Check) R/W 132

WRITE CURRENT DURING READ CHECK (Write I Check) R/W 132

#### WRITE CURRENT DURING READ CHECK (Write I Check)

#### **Error Description**

Write Current during Read Check (Write I Check) indicates that logic internal to the HDA detected Write Current during a Read operation. This condition is indicated to the drive logic by the MARS Unsafe line. MARS Unsafe, Set Read\*Write and MST Outbus Bit 3 (Read Gate), set the Write I Check latch. Write I Check activates R/W Check (see R/W 114). Write I Check is sent to the controller on Inbus Bit 7 during a Sense R/W command.

#### **Force Write I Check**

Microdiagnostic routine AD, test 8 forces Write Current during Read Check (Write I Check) by setting the diagnostic latch and performing a Set Read\*Write command with MST Outbus Bit 3 active. The diagnostic latch is set by the Diagnostic Set command and Outbus Bit 6 (see OPER 101).

#### **Reset Write I Check**

The Write I Check latch is reset by the following:

Check Reset. Rd\*Wr Reset. Pwr On CE Reset

#### **Diagnostic References**

#### **READ/WRITE MICRODIAGNOSTICS**

The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

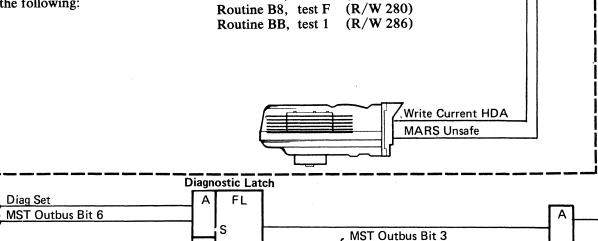
(MICFL 130)
(MICFL 240)
(MICFL 320)
(MICFL 380)
(MICFL 630)
(MICFL 740)

#### SCOPING REFERENCES

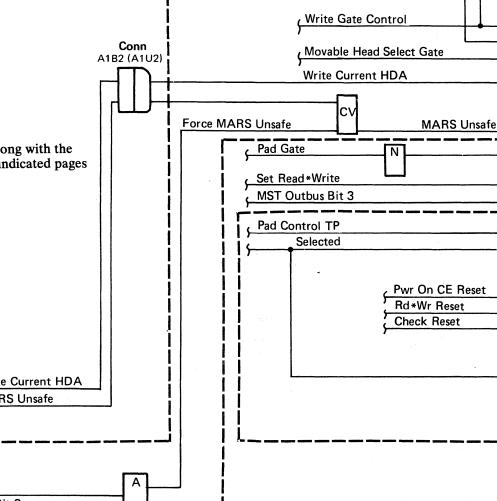
AF

Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5, test 3	(R/W 250)
Routine AD, test 1	(R/W 260)
Routine AD, test 8	(R/W 266)
Routine AD, test 9	(R/W 270)
Routine B8, test D	
Routine B8, test F	
Routine BB, test 1	(R/W 286)



Set Rd \*Wr or Pad Ctrl



A1G2 (A1P2)

KG200 (KP200)

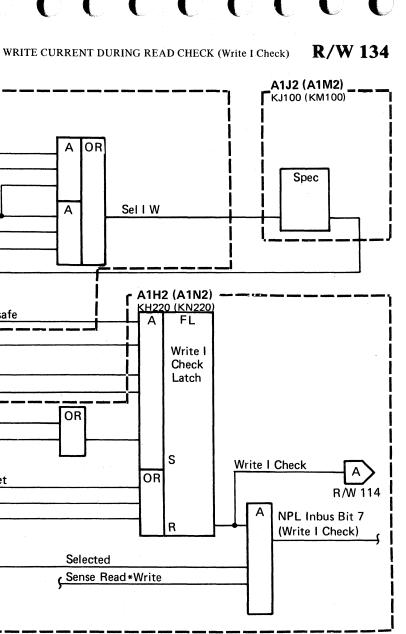
**Fixed Head Select Gate** 

Write Gate Sel or Pad

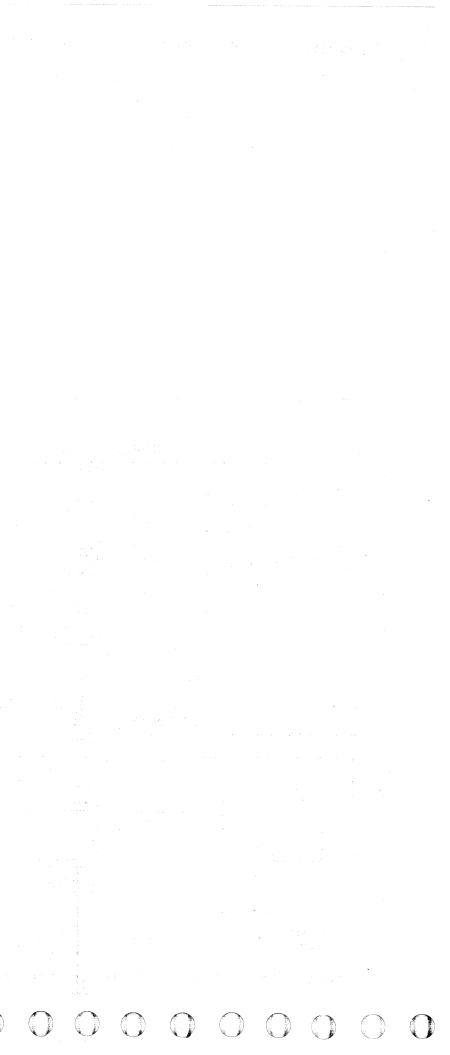
3350	EC0134 Seq. 1 of 1	<b>2358640</b> Part No.	441300 31 Mar 76	441303 30 Jul 76		

Diag Set

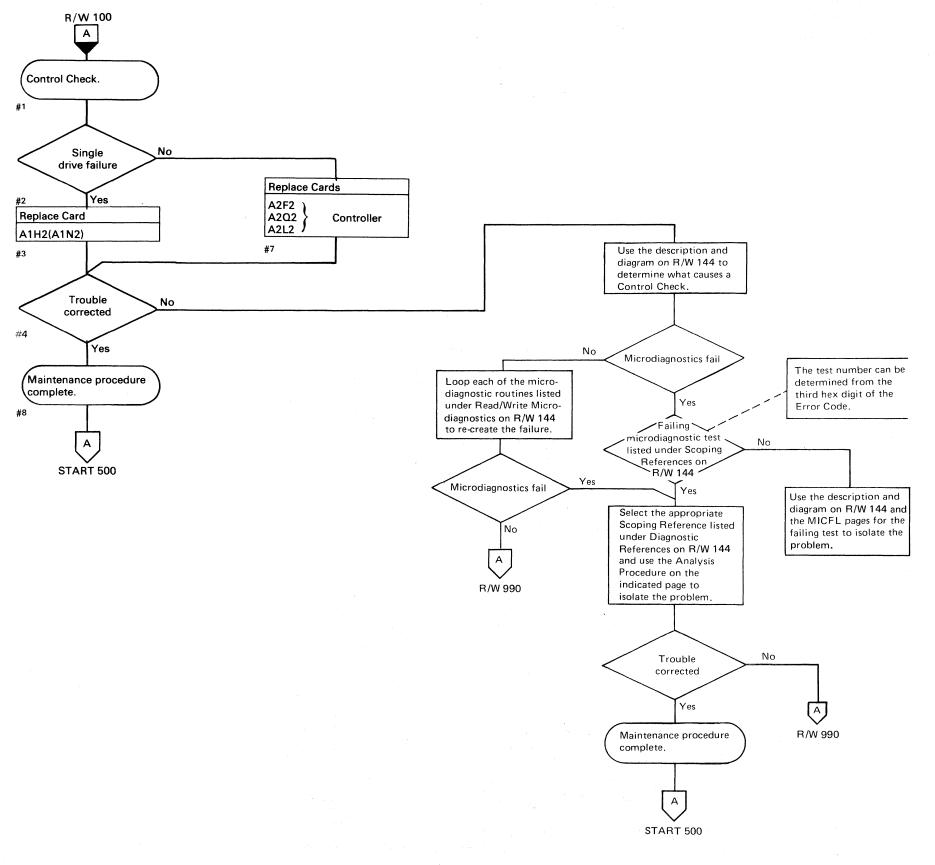
**Selected** 



**R/W 134** 



#### **CONTROL CHECK**

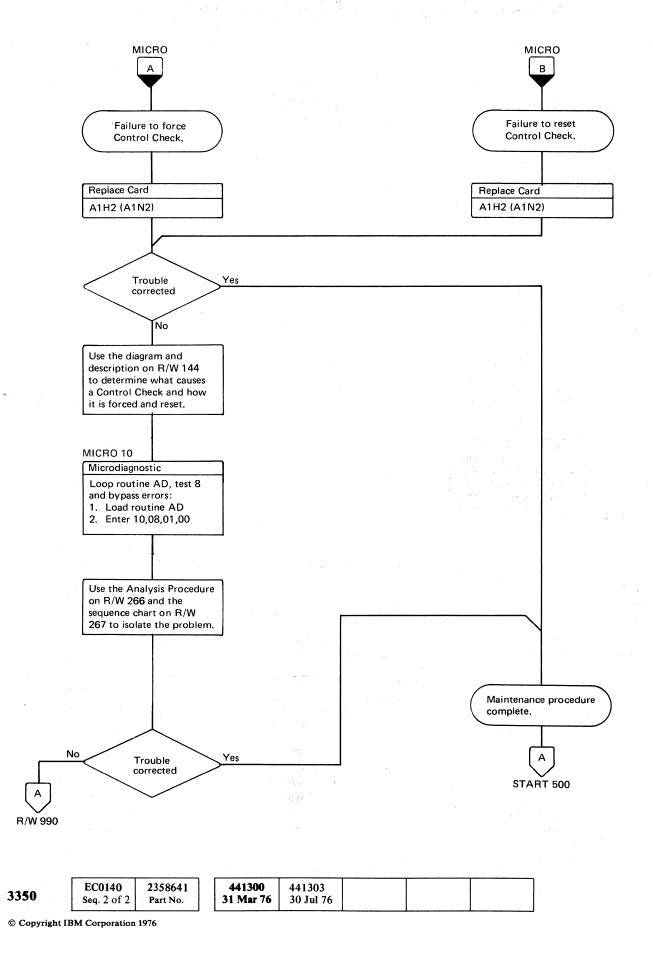


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CONTROL CHECK R/W 140

#### CONTROL CHECK R/W 140

## **CONTROL CHECK**



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CONTROL CHECK R/W 142

CONTROL CHECK R/W 142

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#### **CONTROL CHECK**

#### **Error Description**

Control Check is caused by MST Outbus Bit 1 (Write Gate) and MST Outbus Bit 3 (Read Gate) both being active when Set Read\*Write is active. Control Check activates R/W Check (see R/W 110). Control Check is sent to the controller on Inbus Bit 5 during a Sense Read\*Write command.

#### **Force Control Check**

Microdiagnostic routine AD, test 8 forces Control Check by a diagnostic Set Read\*Write command with MST Outbus bits 1 and 3 active.

#### **Reset Control Check**

Control Check is reset by the following:

**Check Reset** Rd\*Wr Reset Pwr On CE Reset

#### **Diagnostic References**

**READ/WRITE MICRODIAGNOSTICS** 

The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

(MICFL 130)
(MICFL 240)
(MICFL 320)
(MICFL 380)
(MICFL 630)
(MICFL 740)

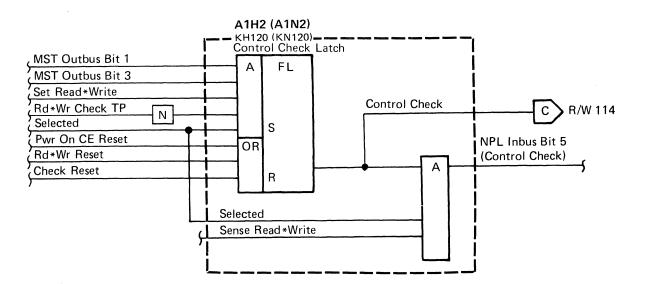
SCOPING REFERENCES

Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5,		(R/W 250)
Routine AD, Routine AD,	test 8	(R/W 260) (R/W 266)
Routine AD, Routine B8,		(R/W 270) (R/W 276)
Routine B8, Routine BB,		(R/W 280) (R/W 286)

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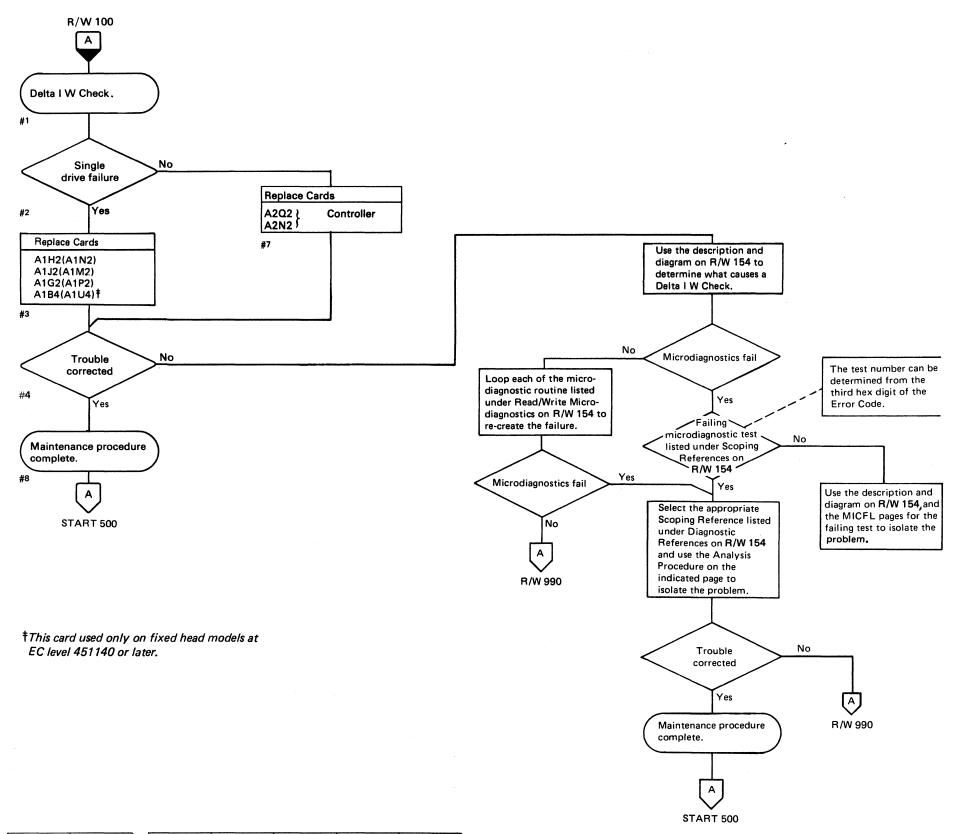
CONTROL CHECK **R/W 144** 

## CONTROL CHECK **R/W 144**

 $\sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t} = \sum_{i=1}^{n} \frac{\partial \mathbf{x}_{i}}{\partial t}$ 



#### **DELTA I W CHECK**



3350	EC0150 Seq. 1 of 2	<b>2358643</b> Part No.	441300 31 Mar 76	441303 30 Jul 76	441310 27 Jun 80	

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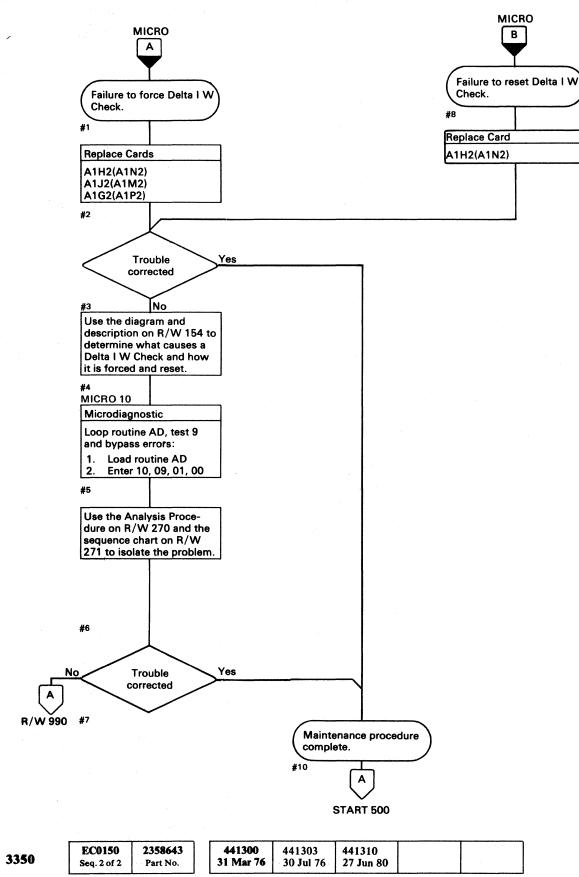
## DELTA I W CHECK R/W 150

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## DELTA I W CHECK R/W 150

## **DELTA I W CHECK**



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## DELTAIW CHECK R/W 152

## DELTAIWCHECK R/W 152

#### **DELTA I W CHECK**

#### **Error Description**

Delta I W Check indicates that one of the following conditions occurred:

- Writing was attempted on an outer (even numbered) movable head or a fixed head and Delta Write current was not detected.
- Writing was attempted on an inner (odd numbered) movable head and Delta Write current was detected.

Delta I W Check activates R/W Check (see R/W 110). Delta I W Check is sent to the controller on Inbus Bit 4 during a Sense Read/Write command.

#### Force Delta I W Check

Microdiagnostic routine AD, test 9 forces Delta I W Check by selecting physical head 1 and issuing a diagnostic set command with Outbus Bit 2 active. The diagnostic set command with Outbus Bit 2 active forces Delta Write current.

#### **Reset Delta I W Check**

Delta I W Check is reset by the following:

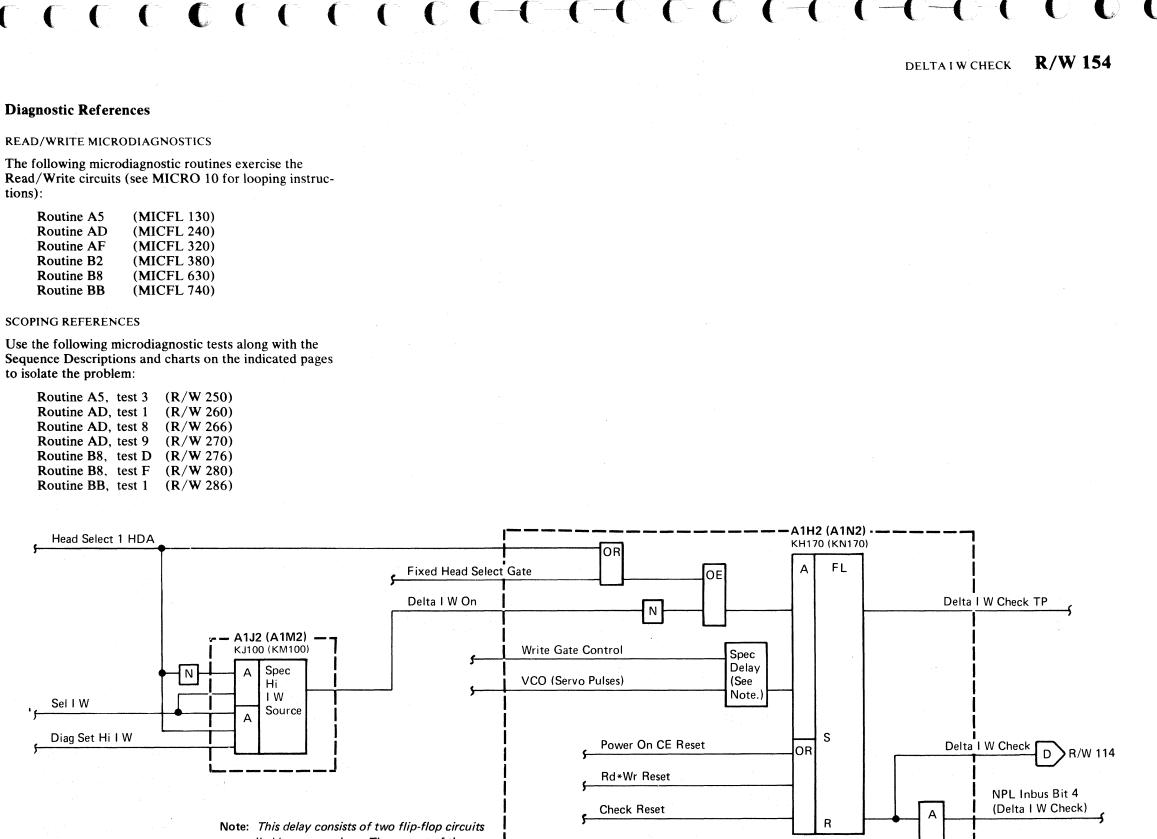
Check Reset. Rd\*Wr Reset. Pwr On CE Reset.

Read/Write circuits (see MICRO 10 for looping instructions):

Routine A5	(MICFL 130)
Routine AD	(MICFL 240)
Routine AF	(MICFL 320)
Routine B2	(MICFL 380)
Routine B8	(MICFL 630)
Routine BB	(MICFL 740)

Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5,	test 3	(R/W 250)
Routine AD,	test 1	(R/W 260)
Routine AD,	test 8	(R/W 266)
Routine AD,	test 9	(R/W 270)
Routine B8,	test D	(R/W 276)
Routine B8,	test F	(R/W 280)
Routine BB,	test 1	(R/W 286)



controlled by servo pulses. The output of the delay is active approximately 2 servo pulses times after Write Gate Control comes active.

3350	EC0154 Seq. 1 of 1	<b>2358644</b> Part No.	1	441300 31 Mar 76	-		

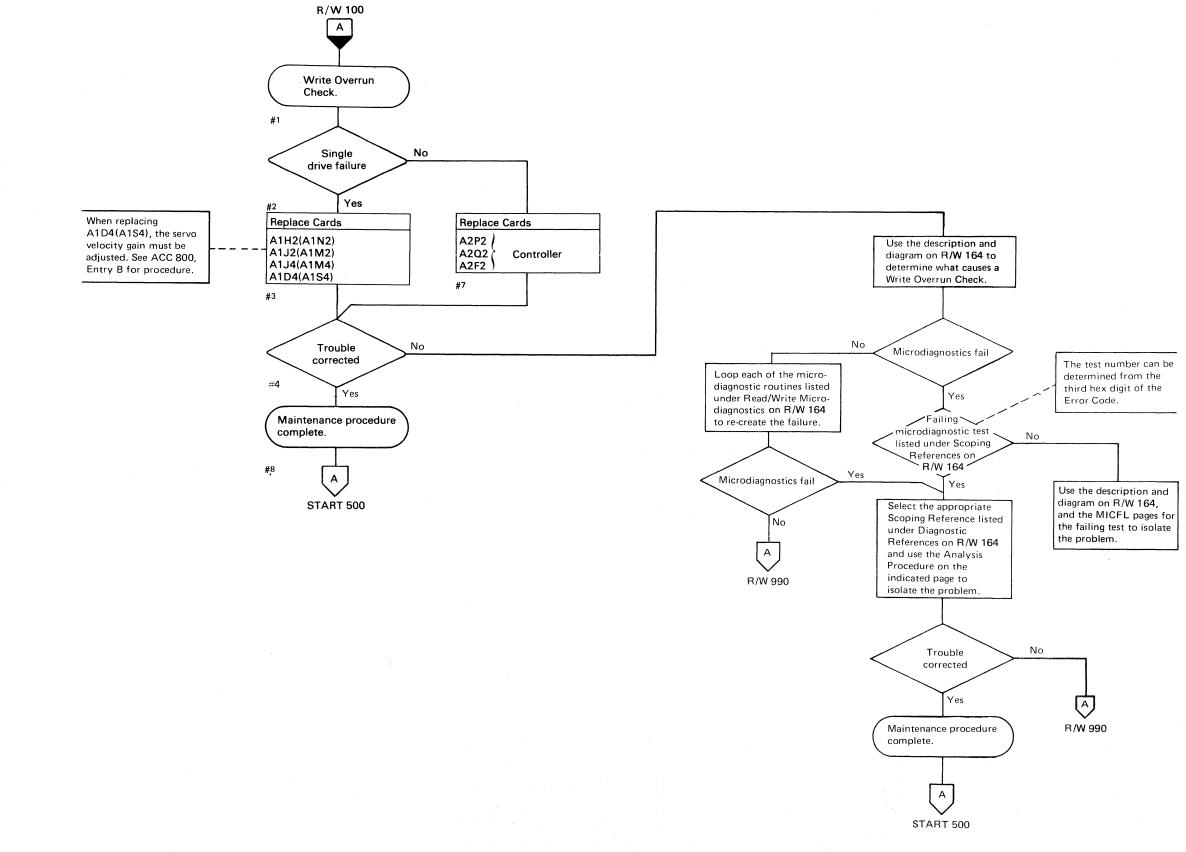
DELTAIWCHECK **R/W 154** 

Selected

Sense Read \* Write



## WRITE OVERRUN CHECK

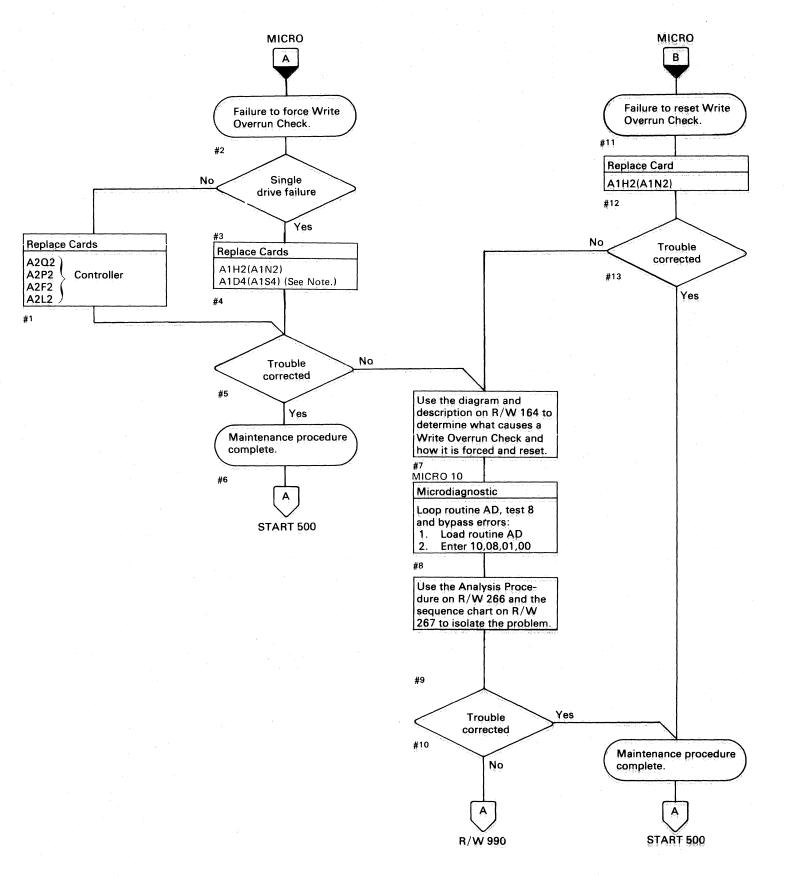


3350	EC0160 Seq. 1 of 2	<b>2358645</b> Part No.		441300 31 Mar 76	441303 30 Jul 76				
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#### WRITE OVERRUN CHECK **R/W 160**

WRITE OVERRUN CHECK **R/W 160** 

## WRITE OVERRUN CHECK



Note: When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.

3350	EC0160 Seq. 2 of 2	2358645 Part No.	441300 31 Mar 76	441303 30 Jul 76		

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#### WRITE OVERRUN CHECK

**R/W 162** 

R/W 162

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WRITE OVERRUN CHECK

#### WRITE OVERRUN CHECK

#### **Error Description**

Write Overrun indicates that writing was attempted through an Index Mark. (Writing into or out of an Index is valid but not both.)

MST Outbus Bit 1 activates Write Gate Control when Set Read/Write is active. If Write Gate Control is active through an Index Mark, Write Overrun is indicated and Read/Write Check is set on. A subsequent Sense Read/Write command indicates Write Overrun Check (Bus In Bit 2).

#### **Force Write Overrun Check**

Microdiagnostic routine AD, test 8 forces Write Overrun Check by:

- 1. Setting Read/Write
- 2. Orienting on Index
- 3. Waiting until just before the next Index then activating Write Gate Control (MST Outbus Bit 1) and keeping it active through Index.

#### **Reset Write Overrun Check**

Write Overrun Check is reset by the following:

Check Reset Rd\*Wr Reset Pwr On CE Reset

#### **Diagnostic References**

**READ/WRITE MICRODIAGNOSTICS** 

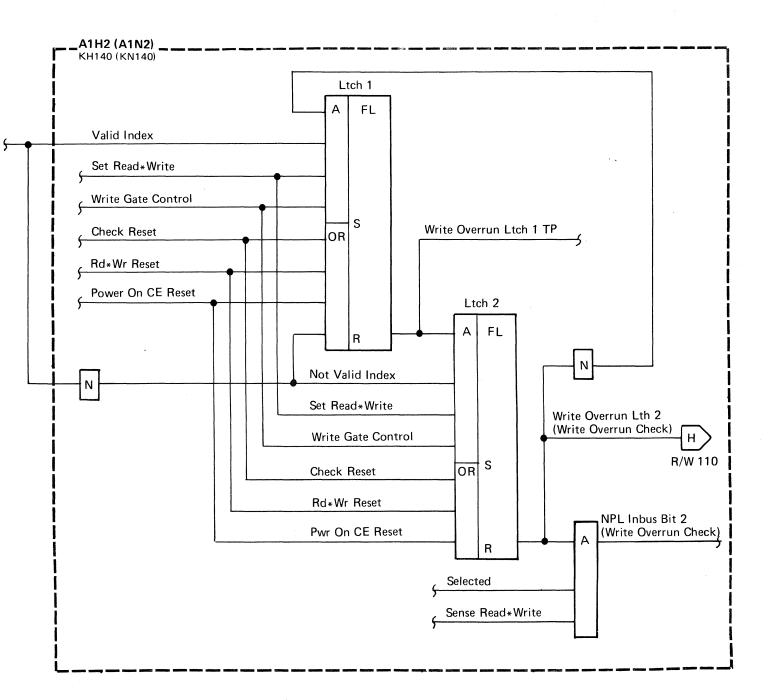
The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

Routine A5 (MICFL 130) Routine AD (MICFL 240) Routine AF (MICFL 320) Routine B2 (MICFL 380) Routine B8 (MICFL 630) Routine BB (MICFL 740)

#### SCOPING REFERENCES

Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5, test 3 (R/W 250)Routine AD, test 1 (R/W 260)Routine AD, test 8 (R/W 266)Routine AD, test 9 (R/W 270)Routine B8, test D (R/W 276)Routine B8, test F (R/W 280)Routine BB, test 1 (R/W 286)



3350	EC0164 Seq. 1 of 1	2358646 Part No.	441300 31 Mar 76	441303 30 Jul 76		
	-					

#### WRITE OVERRUN CHECK **R/W 164**

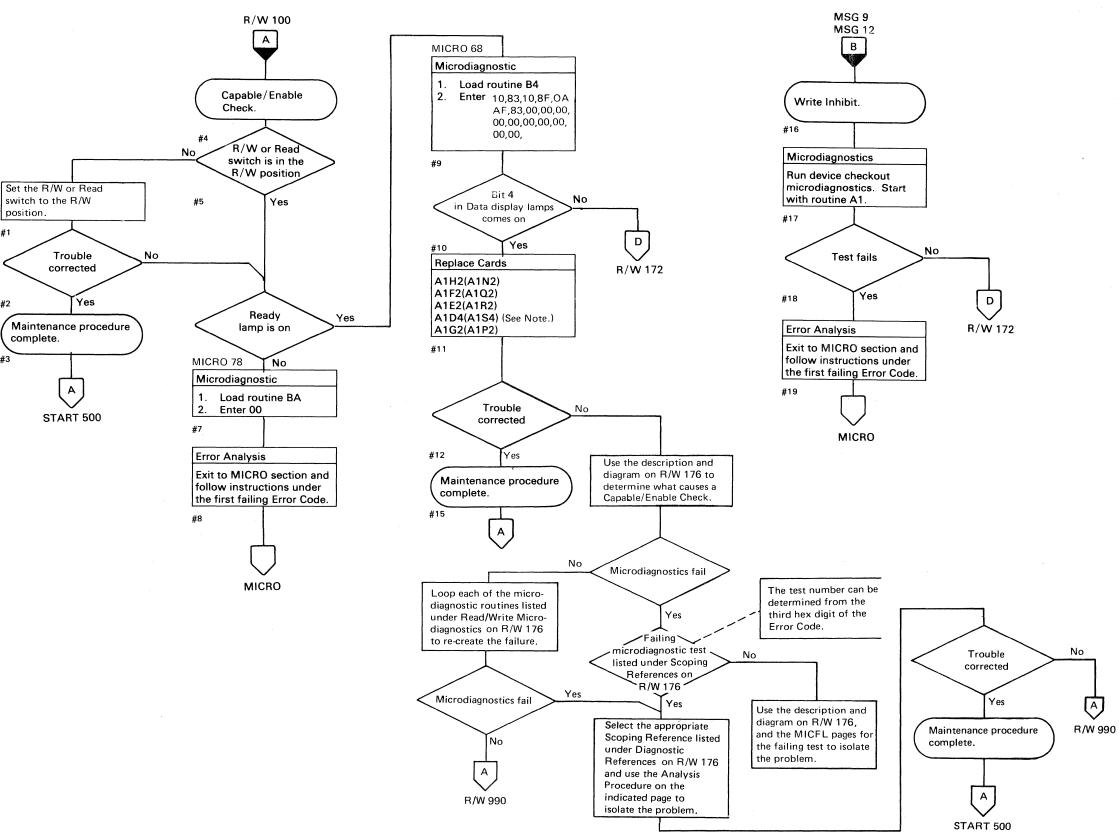


#1

#2

#3

## **CAPABLE/ENABLE CHECK**

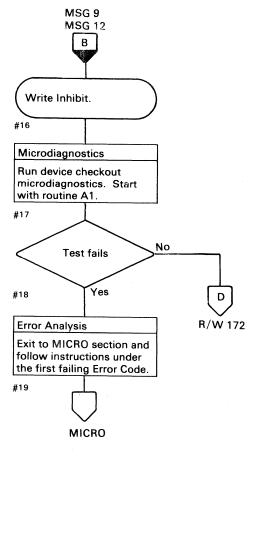


Note: When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure,

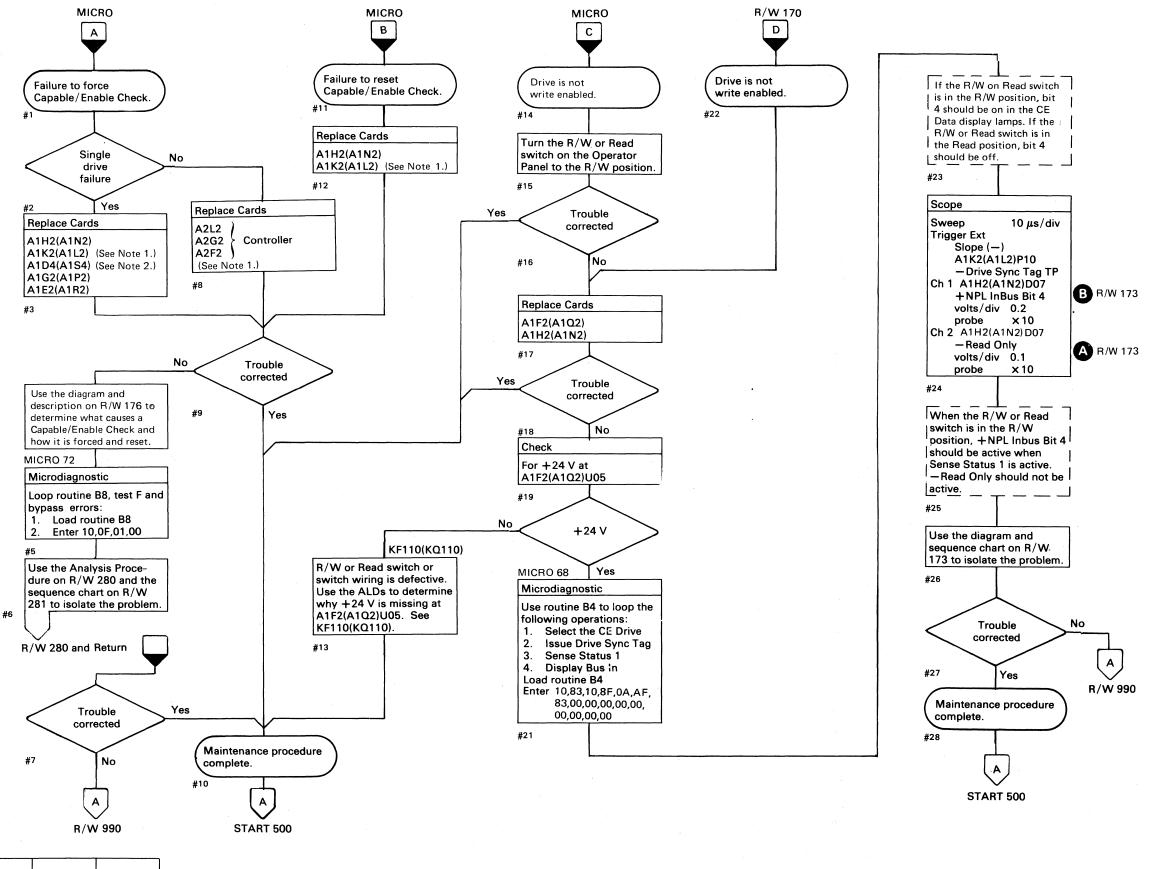
3350	<b>EC0170</b> Seq. 1 of 2	<b>2358647</b> Part No.	441300 31 Mar 76	441303 30 Jul 76		
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CAPABLE/ENABLE CHECK **R/W 170** 

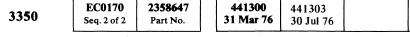


#### **CAPABLE/ENABLE CHECK**



Note 1: When replacing A1K2(A1L2) and/or A2G2, check the addressing jumpers. See INST 6.

Note 2: When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800, Entry B for procedure.



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#### CAPABLE/ENABLE CHECK R/W 172

#### CAPABLE/ENABLE CHECK **R/W 172**

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## **CAPABLE/ENABLE CHECK**

#### Write Enable

Write operations are enabled by turning the R/W or Read switch to the R/W position. The storage control determines if the drive is write enabled by issuing a Sense Status 1 Tag and looking for an active Inbus Bit 4.

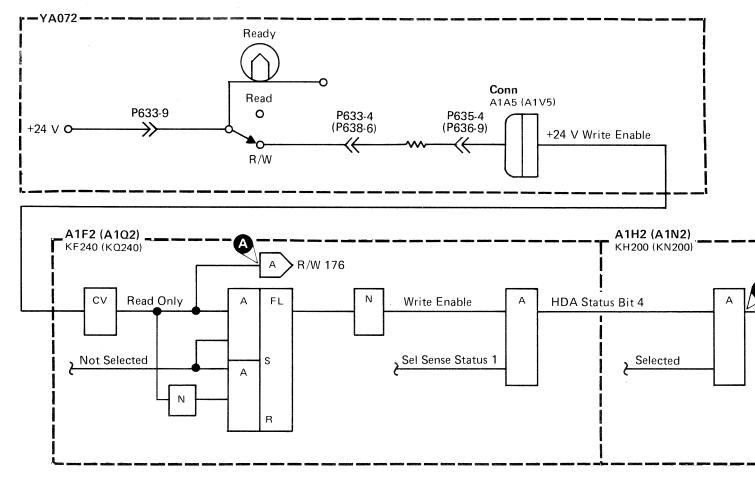


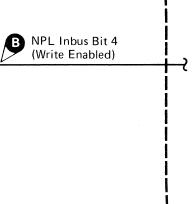
Chart Line No.	Line Name	ALD	Test Point					
1	+Select A(B)	KK140 (KL140)	A1K2 (A1L2) G12				-	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09					
3	-Drive Sync Tag TP	KK170 (KL170)	A1K2 (A1L2) P10					
4	-Sense Status 1	KK170 (KL170)	A1K2 (A1L2) U05					
5	+NPL Inbus Bit 4*	KH200 (KN200)	A1H2 (A1N2) D07	B				
6	-Read Only*	KH130 (KN130)	A1H2 (A1N2) G10	A		Inactive		

\*R/W or Read switch must be in the R/W position.

3350	EC0173 Seq. 1 of 2	2358648 Part No.	441300 31 Mar 76	441303 30 Jul 76		

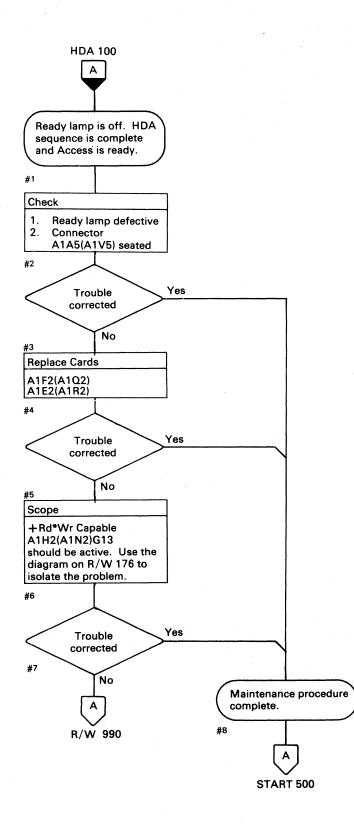


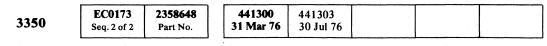
#### CAPABLE/ENABLE CHECK R/W 173



**R/W 173** CAPABLE/ENABLE CHECK

## **CAPABLE/ENABLE CHECK**





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## CAPABLE/ENABLE CHECK R/W 174

#### CAPABLE/ENABLE CHECK **R/W 174**

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#### **CAPABLE/ENABLE CHECK**

#### **Error Description**

Capable/Enable Check indicates that one of the following conditions occurred:

- Writing was attempted with the R/W or Read switch set to the Read position.
- Reading or Writing was attempted with the drive not Ready or with the Servo not track following.

Capable/Enable Check activates R/W Check (see R/W 114). Capable/Enable Check is indicated to the controller on Inbus Bit 1 during a Sense Read\*Write tag.

#### Force Capable/Enable Check

Microdiagnostic routine B8, test F forces Capable/Enable Check by issuing a Rezero command immediately followed by a Set Read/Write command. Since the drive is not track following when the Set Read/Write command is issued, Set Rd\*Wr Capable Check TP becomes active and sets the Capable/Enable Check latch.

#### **Reset Capable/Enable Check**

Capable/Enable Check is reset by the following:

Check Reset. Rd\*Wr Reset. Pwr On CE Reset.

#### **Diagnostic References**

#### **READ/WRITE MICRODIAGNOSTICS**

The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

Routine A5 (MICFL 130) Routine AD (MICFL 240) Routine AF (MICFL 320) Routine B2 (MICFL 380) Routine B8 (MICFL 630) Routine BB (MICFL 740)

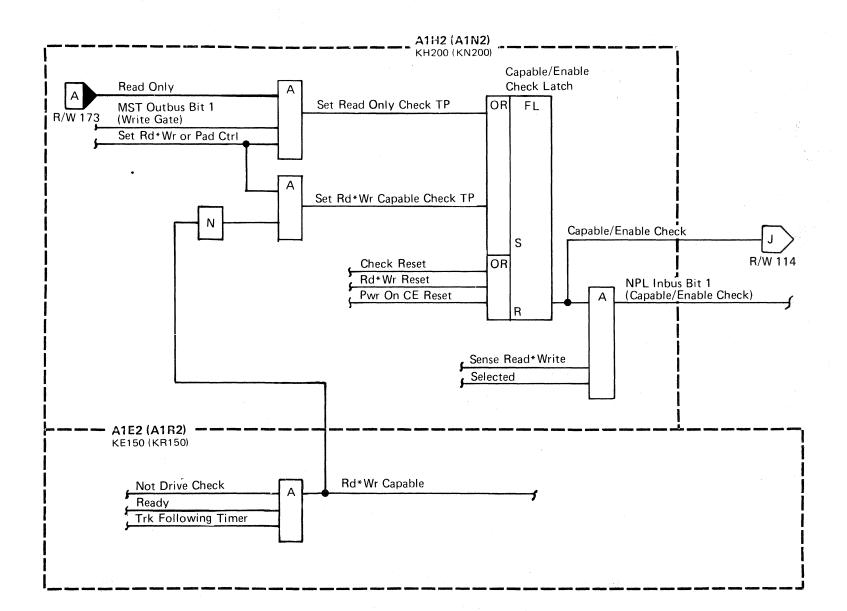
#### SCOPING PROCEDURES

Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5, test 3 (R/W 250) Routine AD, test 1 (R/W 260) Routine AD, test 8 (R/W 266)

3350         ECU1/6         2558049         441300         441303           Seq. 1 of 1         Part No.         31 Mar 76         30 Jul 76	3350	EC0176 Seq. 1 of 1	2358649 Part No.		441300 31 Mar 76	441303 30 Jul 76					
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Routine AD, test 9 (R/W 270) Routine B8, test D (R/W 276) Routine B8, test F (R/W 280) Routine BB, test 1 (R/W 286)

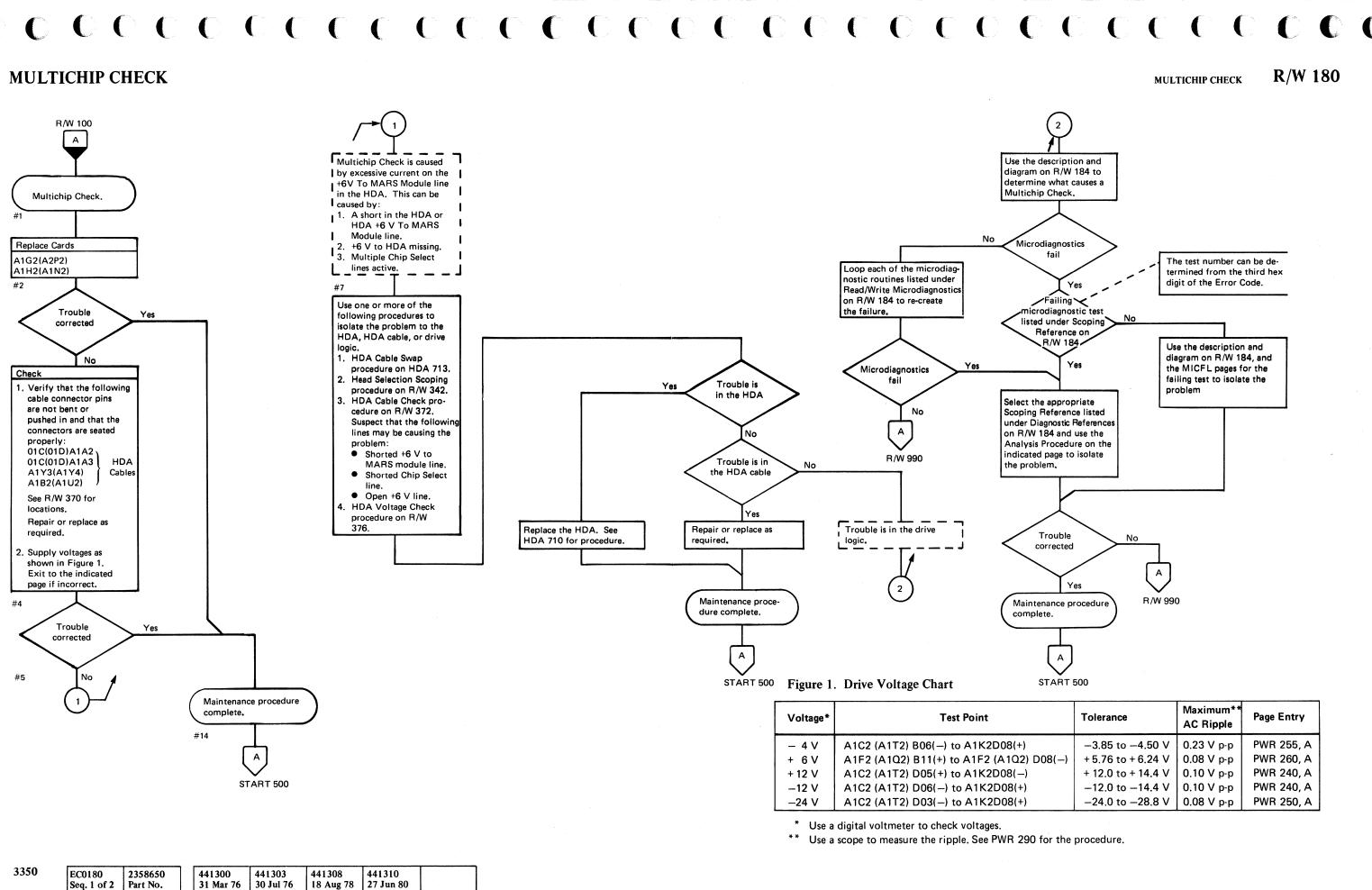


CAPABLE/ENABLE CHECK **R/W 176** 

#### CAPABLE/ENABLE CHECK **R/W 176**

a na shekara ta shekar "我们的这些,我们是不是"要我们的。 这些时代,我们就不是你们,要就是你。



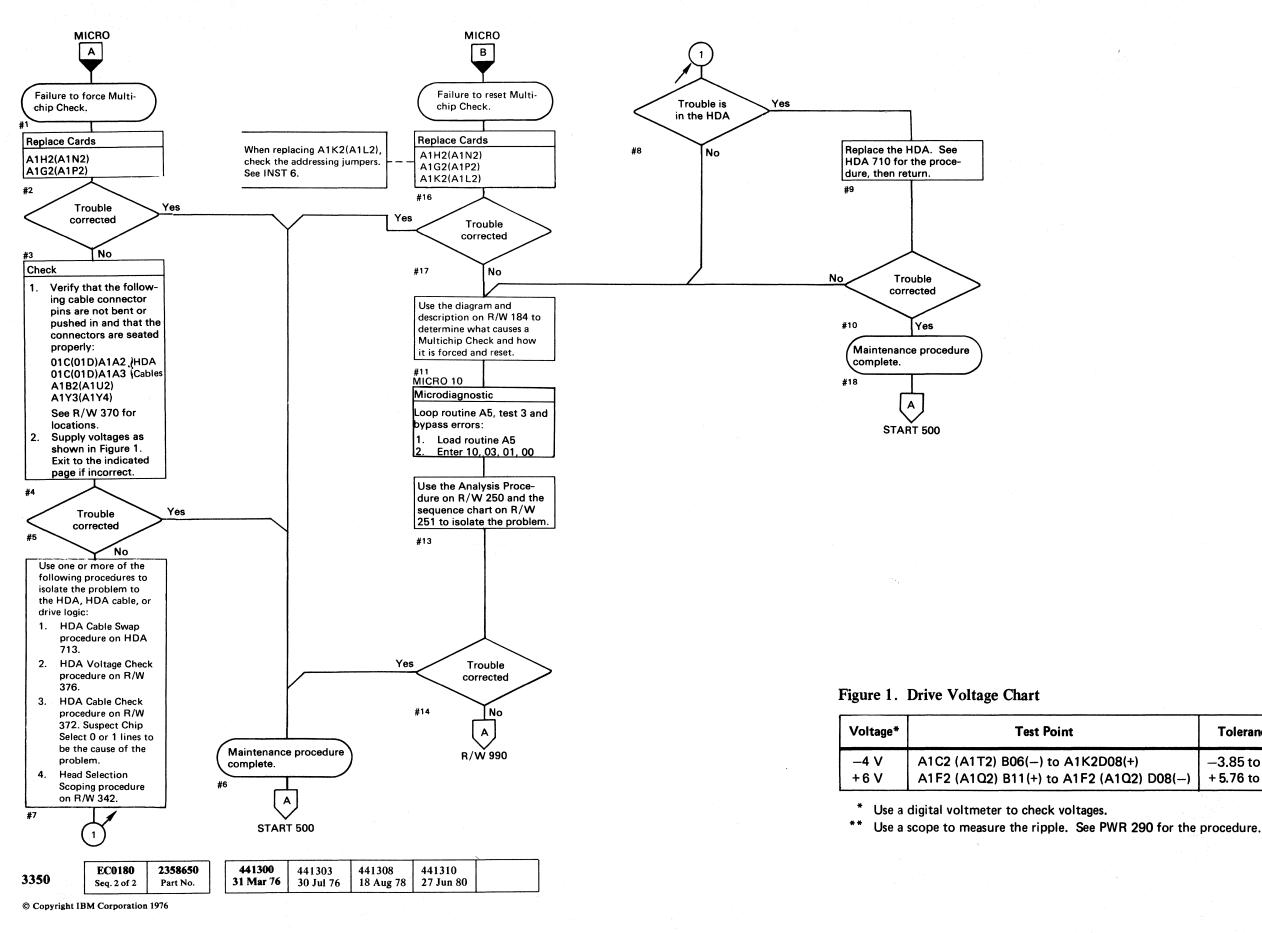


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	Tolerance Maximum* AC Ripple		Page Entry
08(+)	-3.85 to -4.50 V	0.23 V p-p	PWR 255, A
A1Q2) D08()	+ 5.76 to + 6.24 V	0.08 V p-p	PWR 260, A
08(—)	+ 12.0 to + 14.4 V	0.10 V p-p	PWR 240, A
08(+)	-12.0 to -14.4 V	0.10 V p-p	PWR 240, A
08(+)	-24.0 to -28.8 V	0.08 V p-p	PWR 250, A

#### MULTICHIP CHECK

## **MULTICHIP CHECK**



MULTICHIP CHECK **R/W 182** 

	Tolerance	Maximum** AC Ripple	Page Entry
-) 2) D08()	3.85 to4.50 ∨ + 5.76 to + 6.24 ∨	0.23 V p-p 0.08 V p-p	PWR 255, A PWR 260, A
	Ne granden en e		00145

MULTICHIP CHECK **R/W 182** 

## MULTICHIP SELECTED (Multihead Check)

#### **Error Description**

Multiple chips selected indicate that two or more head select chips were active at the same time and a Read or Write operation was attempted.

The +6 V to MARS Module line is monitored for excessive current. If excessive current is detected, the Multichip Selected line becomes active and the Multichip Check latch is set. Multichip Check activates Read/Write Check (see R/W 114). Multichip Check is indicated to the controller on Inbus Bit 0 during a Sense Read/Write Status command.

#### **Force Multi-Chip Check**

Microdiagnostic routine A5, test 3 forces Multichip Check by setting HAR to '08' and activating Chip Select 1 line. The routine then issues a Diagnostic Set command which turns on the Diagnostic latch, forcing Chip Select 0.

#### **Reset Multichip Check**

Multichip Check is reset by the following:

Check Reset. Rd\*Wr Reset. Pwr On CE Reset.

#### **Diagnostic References**

**READ/WRITE MICRODIAGNOSTICS** 

The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

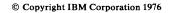
Routine A5	(MICFL 130)
Routine AD	(MICFL 240)
Routine AF	(MICFL 320)
Routine B2	(MICFL 380)
Routine B8	(MICFL 630)
Routine BB	(MICFL 740)

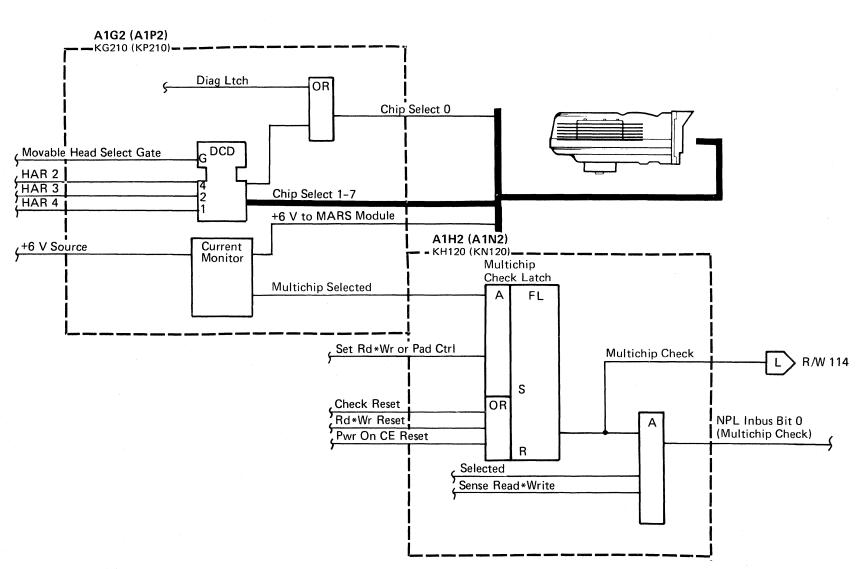
#### SCOPING REFERENCES

Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5, test 3	3 (R/W 250)
Routine AD, test 1	
Routine AD, test 8	3 (R/W 266)
Routine AD, test 9	
Routine B8, test I	O(R/W 276)
Routine B8, test I	
Routine BB, test 1	(R/W 286)

EC0184         23580           Seq. 1 of 2         Part N		441303 30 Jul 76				
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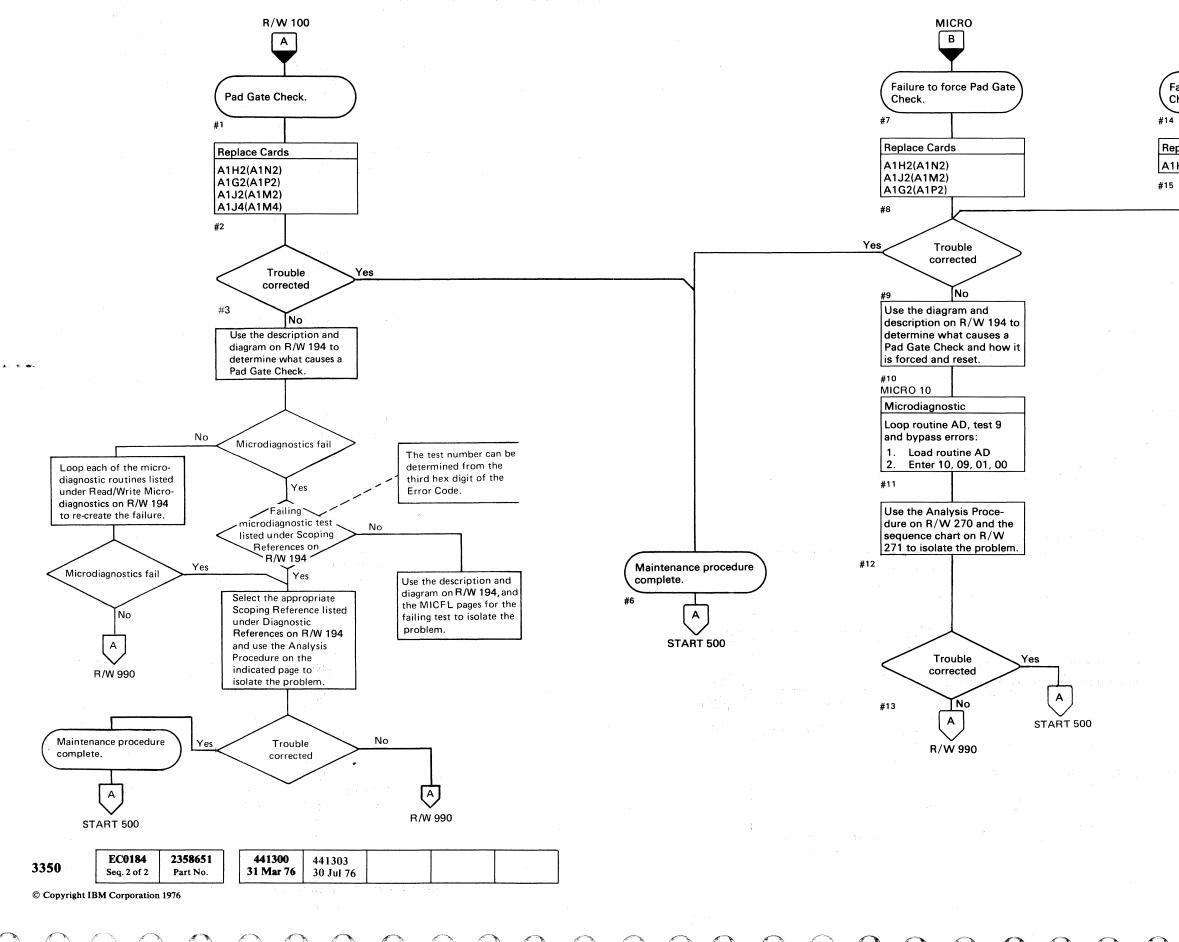


#### MULTICHIP SELECTED (Multihead Check)

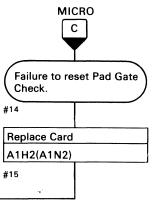
**R/W 184** 

## MULTICHIP SELECTED (Multihead Check) **R/W 184**

**PAD GATE CHECK** 



## PAD GATE CHECK **R/W 190**





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## **PAD GATE CHECK**

#### **Error Description**

Pad Gate Check indicates that Pad Gate (Outbus Bit 2) and Write Gate (Outbus Bit 1) are both active when Set Read\*Write is active. Pad Gate Check causes a Read/Write Check (see R/W 114). Pad Gate Check is indicated to the controller on Inbus Bit 5 during a Sense Status 0 Tag.

#### **Force Pad Gate Check**

Microdiagnostic routine AD, test 9 forces Pad Gate Check with a Set Diagnostic tag and an active MST Outbus Bit 4.

#### **Reset Pad Gate Check**

Pad Gate Check is reset by the following:

Check Reset. Rd\*Wr Reset. Pwr On CE Reset.

#### **Diagnostic References**

#### **READ/WRITE MICRODIAGNOSTICS**

The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

Routine A5	(MICFL 130)
Routine AD	(MICFL 240)
Routine AF	(MICFL 320)
Routine B2	(MICFL 380)
Routine B8	(MICFL 630)
Routine BB	(MICFL 740)

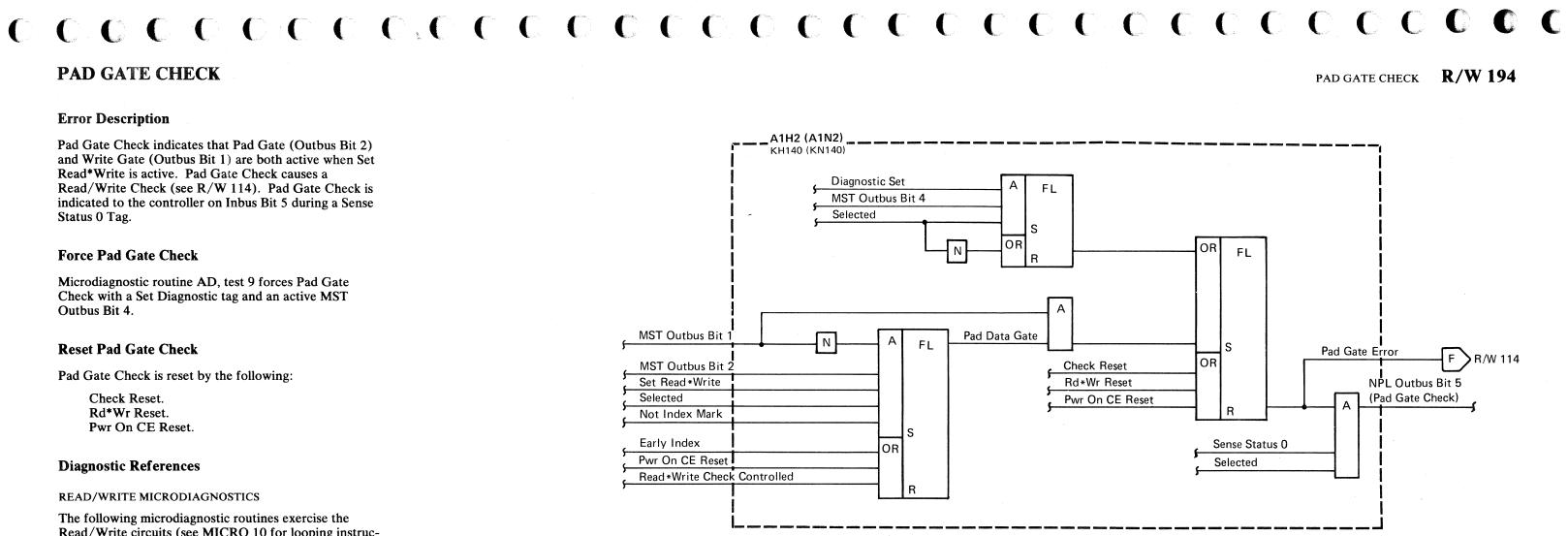
#### SCOPING REFERENCES

Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

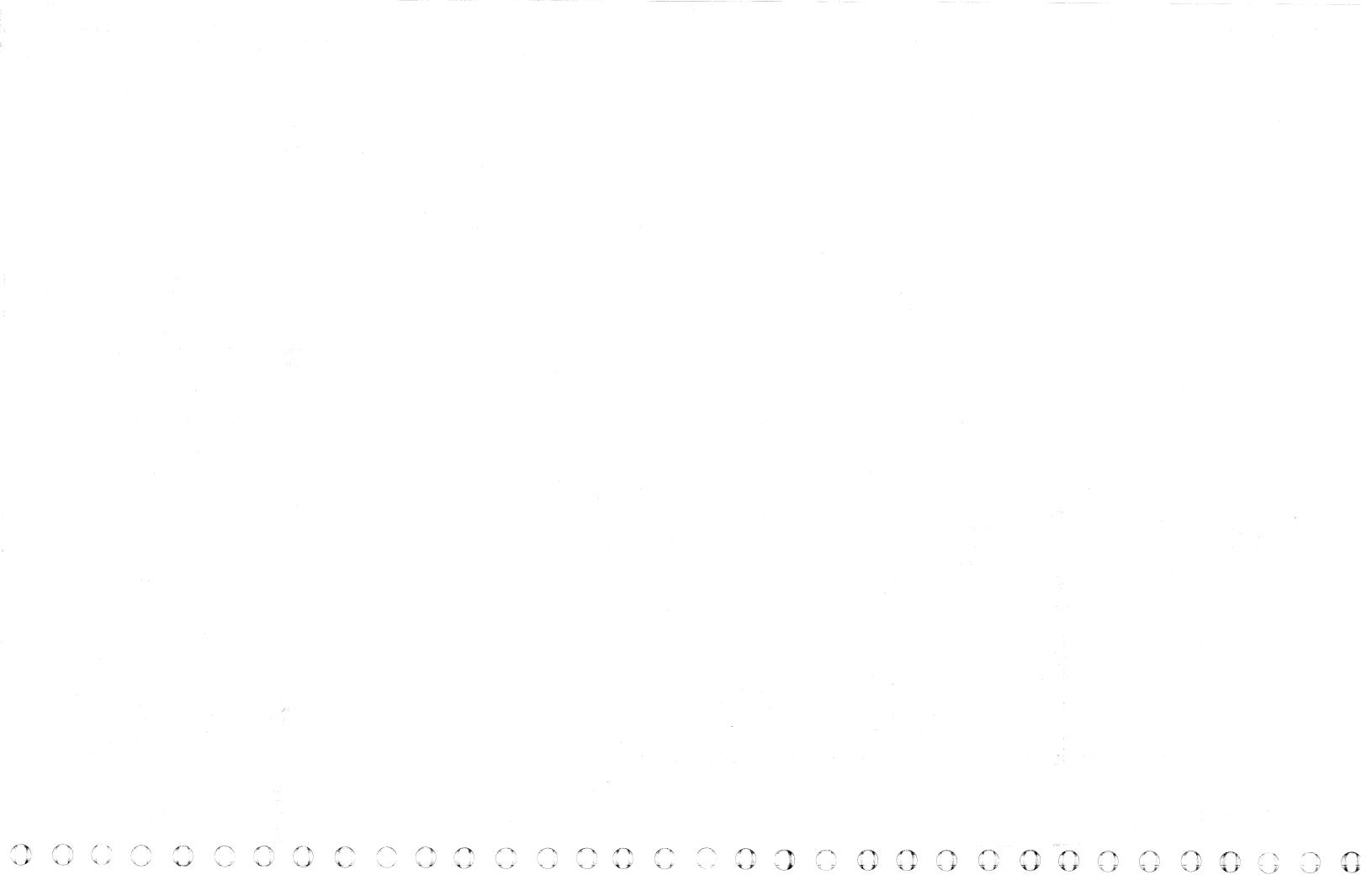
Routine A5,	test 3	(R/W 250)
Routine AD	, test 1	(R/W 260)
Routine AD	, test 8	(R/W 266)
Routine AD	, test 9	(R/W 270)
Routine B8,	test D	(R/W 276)
Routine B8,	test F	(R/W 280)
Routine BB	, test 1	(R/W 286)
0 1 J	,	· **

3350	EC0194 Seq. 1 of 1	2358652 Part No.	441300 31 Mar 76	441303 30 Jul 76		

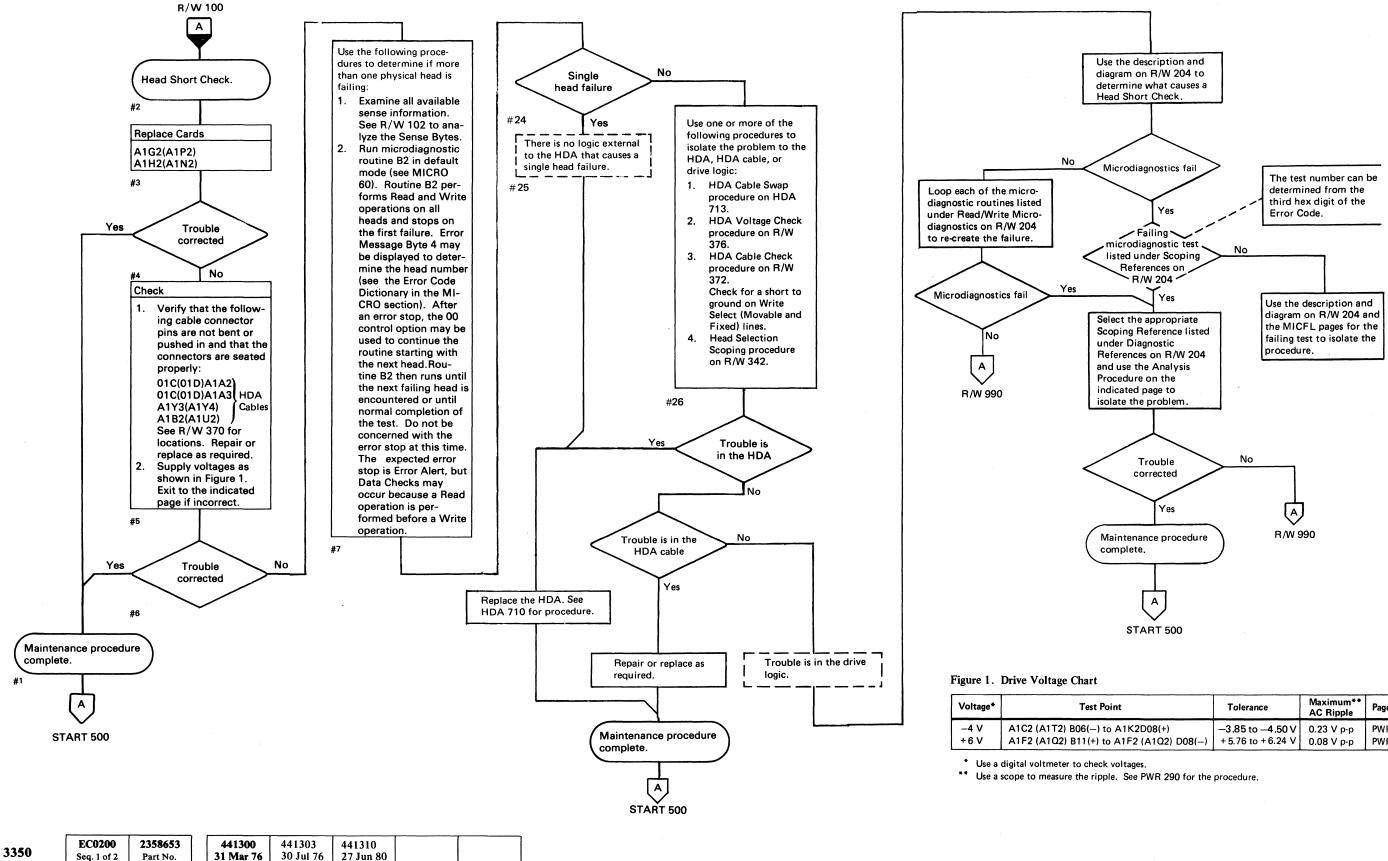




#### PAD GATE CHECK **R/W 194**



## **HEAD SHORT CHECK**



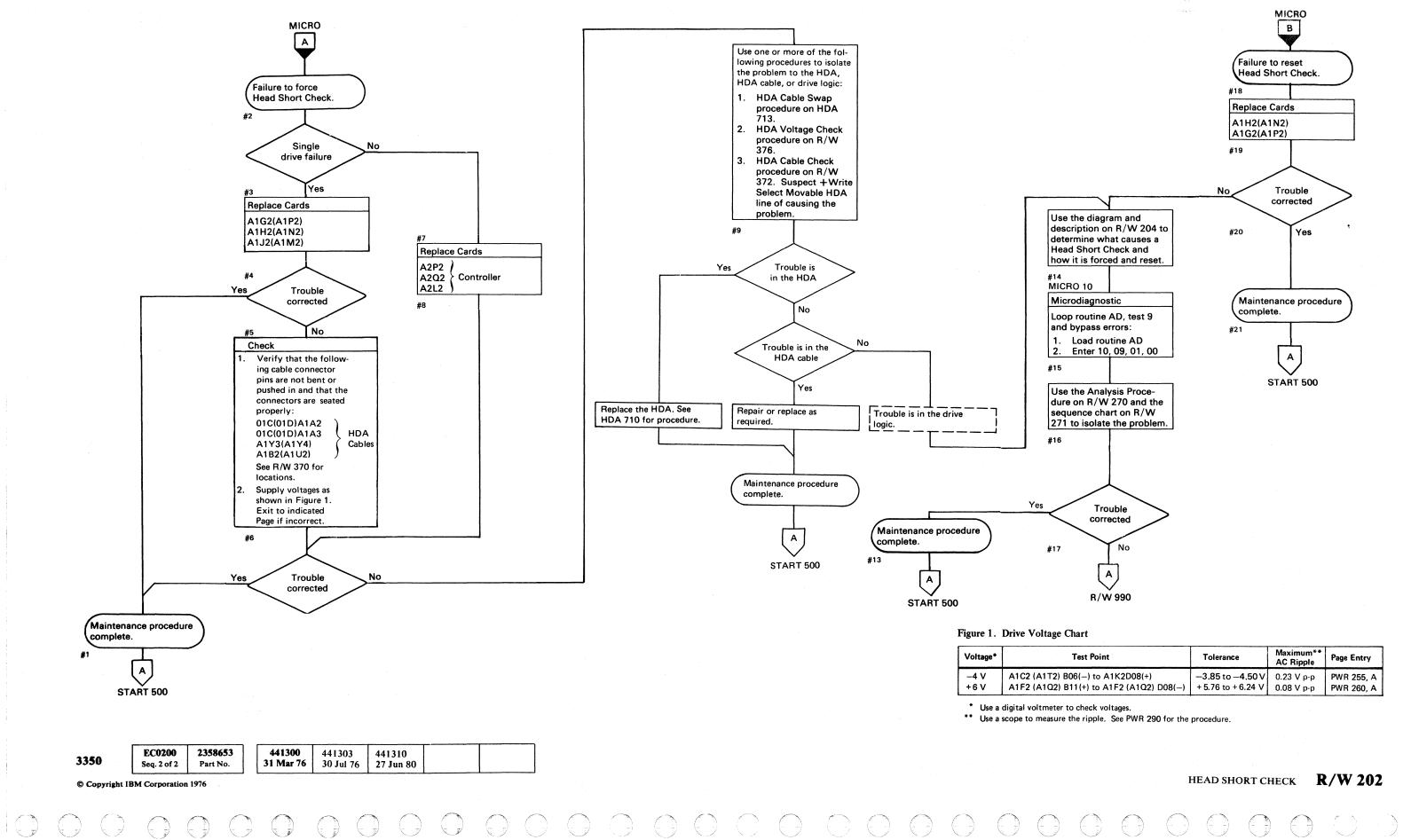
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#### HEAD SHORT CHECK **R/W 200**

int	Tolerance	Maximum** AC Ripple	Page Entry
A1K2D08(+)	-3.85 to -4.50 V	• •	PWR 255, A
A1F2 (A1Q2) D08()	+ 5.76 to + 6.24 V		PWR 260, A

HEAD SHORT CHECK **R/W 200** 

## **HEAD SHORT CHECK**



HEAD SHORT CHECK **R/W 202** 

Test Point	Tolerance	Maximum** AC Ripple	Page Entry	
) B06(–) to A1K2D08(+)	-3.85 to -4.50 V		PWR 255, A	
) B11(+) to A1F2 (A1Q2) D08(–)	+ 5.76 to +6.24 V		PWR 260, A	

6

## **HEAD SHORT CHECK**

#### **Error Description**

Head Short Check indicates that excessive current was detected on the Movable or Fixed Write Select line during a Write operation. The Write Select line is wired in parallel to all of the head center taps. If any head is shorted to ground, excessive current is drawn through the Write Select line during a Write operation (a head shorted to another head is indicated by a Multichip Check).

Head Short Check activates R/W Check (see R/W 114). Head Short Check is sent to the controller on +NPL Inbus Bit 4 during a Sense Status 0 command.

#### **Force Head Short Check**

Microdiagnostic routine AD, test 9 forces Head Short Check by doing the following:

- Diagnostic Set with Outbus Bit 6 active (sets Diagnostic Latch).
- Diagnostic Set Read/Write with Outbus equal to '4F' (activates Write Gate Control).

This causes excessive current to flow on the Write Select Movable HDA line.

#### **Reset Head Short Check**

Head Short Check is reset by the following:

Check Reset. Rd\*Wr Reset. Pwr On CE Reset.

#### **Diagnostic References**

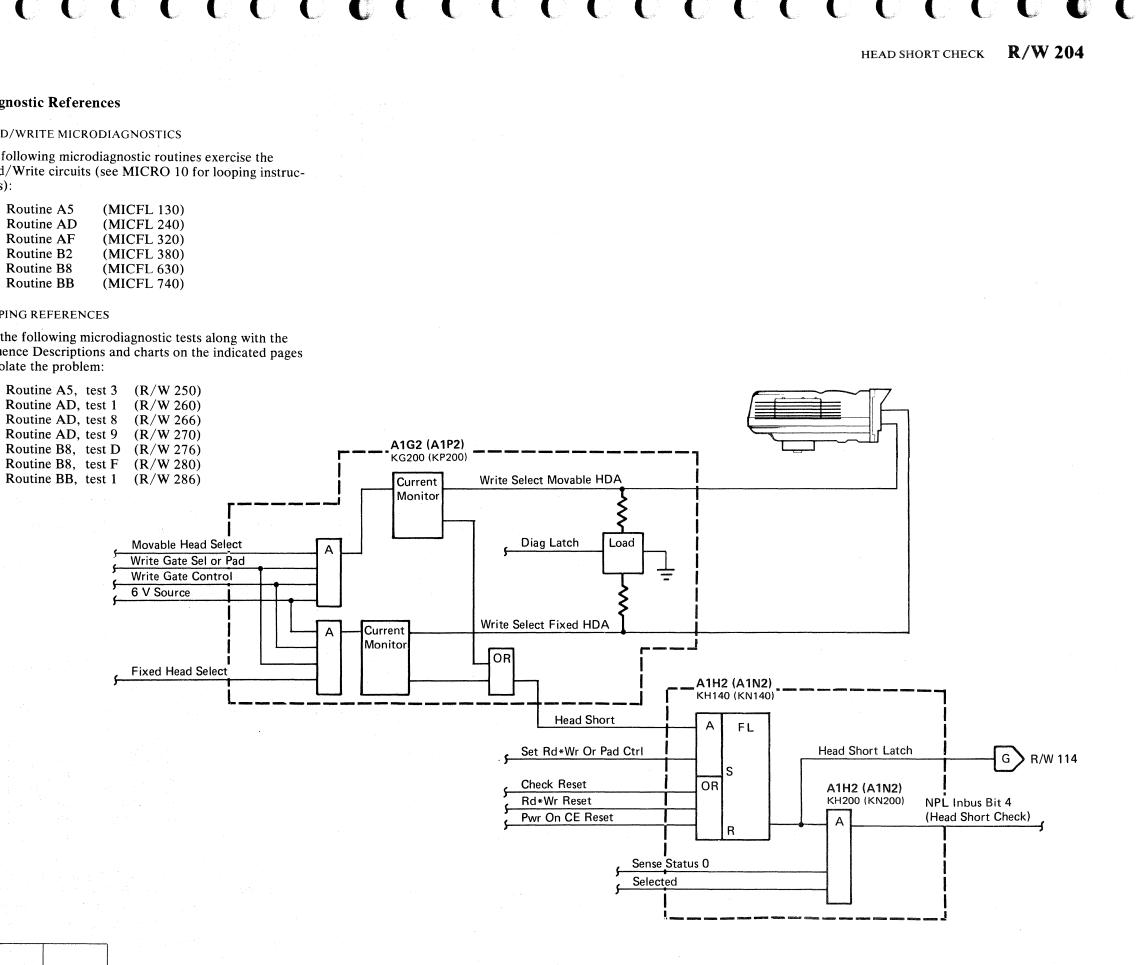
#### **READ/WRITE MICRODIAGNOSTICS**

The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

Routine A5	(MICFL 130)
Routine AD	(MICFL 240)
Routine AF	(MICFL 320)
Routine B2	(MICFL 380)
Routine B8	(MICFL 630)
Routine BB	(MICFL 740)
Routine DD	(WHCFL/40)

#### **SCOPING REFERENCES**

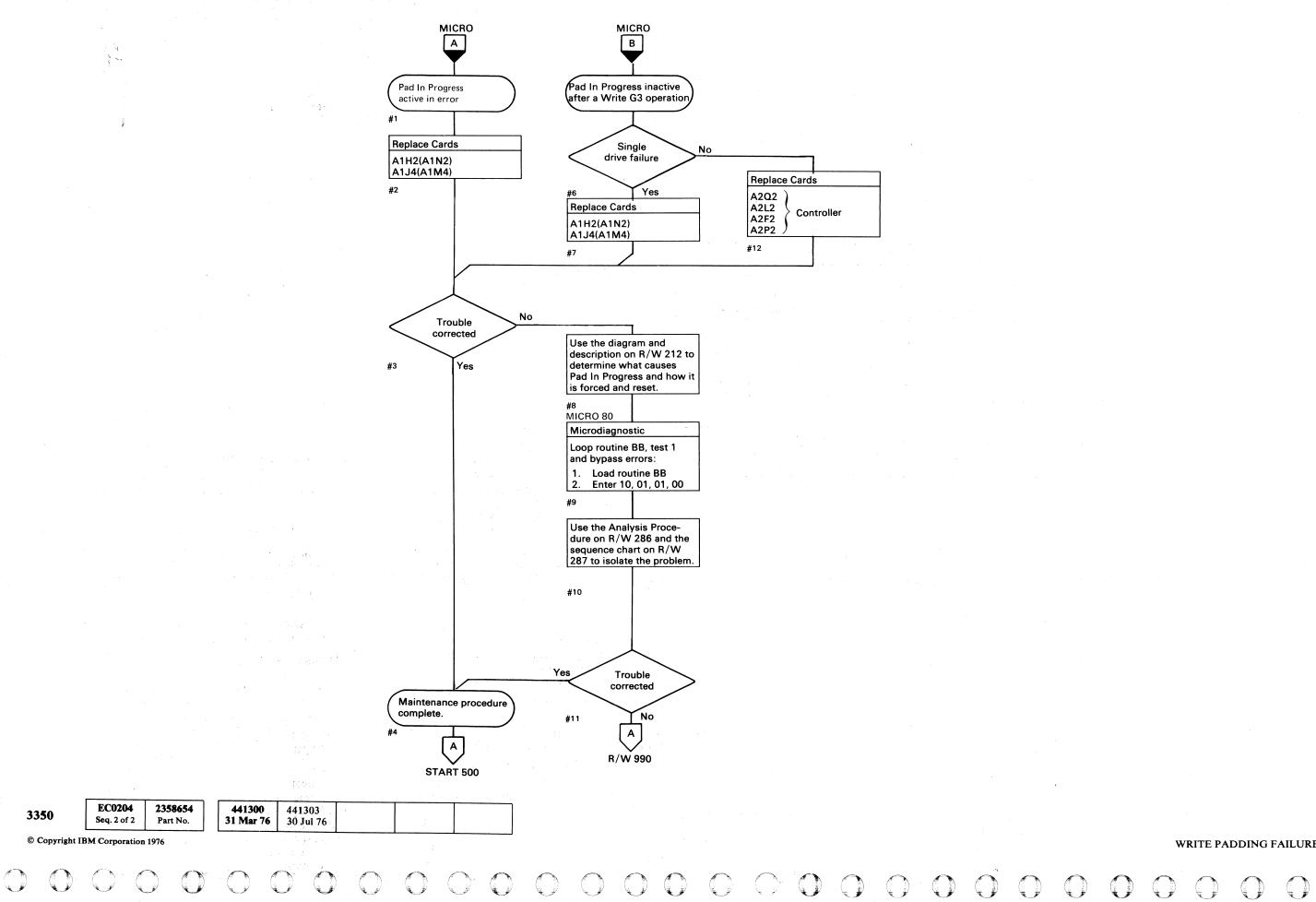
Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:



3350	EC0204 Seq. 1 of 2	<b>2358654</b> Part No.	441300 31 Mar 76	441303 30 July 76	.		
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HEAD SHORT CHECK **R/W 204** 

WRITE PADDING FAILURE



### WRITE PADDING FAILURE **R/W 210**

## WRITE PADDING FAILURE **R/W 210**

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### **PAD IN PROGRESS FAILURE**

#### **Pad Operation Description**

The Pad operation pads the track with clock bits from the end of the last Data field to Index. The pad operation is performed by the drive, independent of the controller, after a Write G3 operation (Write Data field). The controller activates Outbus Bit 2, then de-activates Outbus Bit 1 (Write Gate). This activates Pad Data Gate in the drive and the Pad operation is started. Pad In Progress is indicated to the storage control by Outbus Bit 5 while Set Read/Write is active. After the Pad operation is started, the storage control can reset Read/Write and disconnect from the controller without affecting padding. When Set Read/Write is not active, Pad In Progress is indicated to the storage control on Inbus Bit 0 during a Sense Status 1 tag.

#### **Force Pad In Progress**

Microdiagnostic routine BB, test 1 forces Pad In Progress by performing a 1-byte Write G3 operation, then checking for Pad In Progress (Inbus Bit 5) while Set Read/Write is still active.

#### **Reset Pad In Progress**

Pad In Progress is reset by the following:

Early Index. Pwr On CE Reset. Read/Write Check. Index Mark.

#### **Diagnostic References**

#### **READ/WRITE MICRODIAGNOSTICS**

The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

Routine A5	(MICFL 130)
Routine AD	(MICFL 240)
Routine AF	(MICFL 320)
Routine B2	(MICFL 380)
Routine B8	(MICFL 630)
Routine BB	(MICFL 740)

#### SCOPING REFERENCES

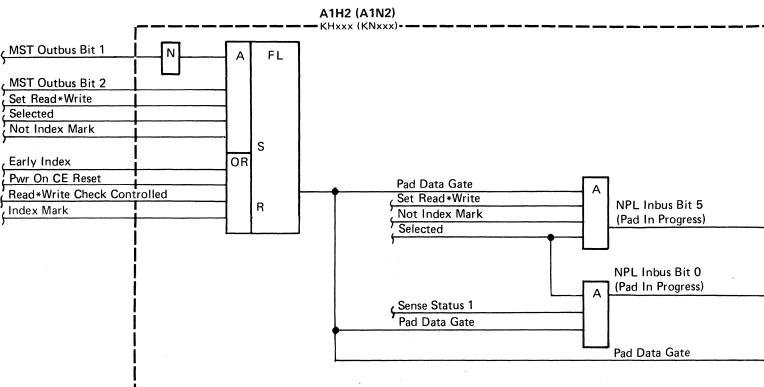
Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5, test 3	(R/W 250)
Routine AD, test 1	(R/W 260)
Routine AD, test 8	(R/W 266)

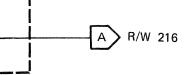
3350	EC0212 Seq. 1 of 2	<b>2358655</b> Part No.		441300 31 Mar 76	441303 30 Jul 76				
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Routine AD,	test 9	(R/W 270)
Routine B8,	test D	(R/W 276)
Routine B8,	test F	(R/W 280)
Routine BB,	test 1	(R/W 286)

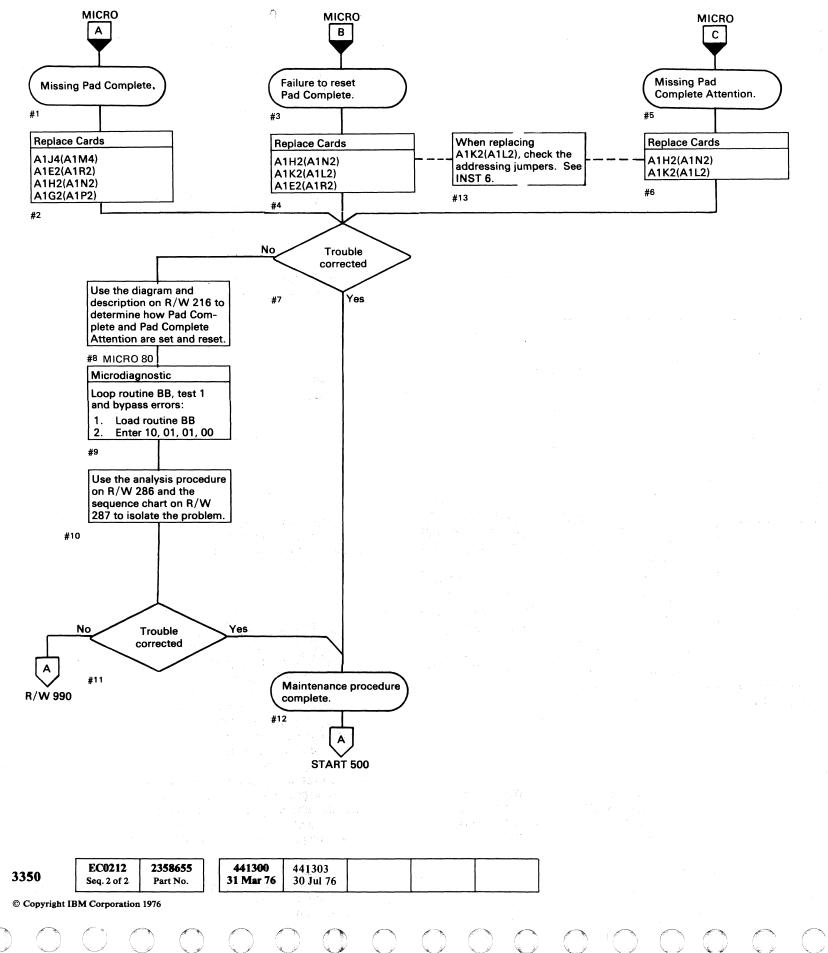


### PAD IN PROGRESS FAILURE **R/W 212**



## PAD IN PROGRESS FAILURE **R/W 212**

## WRITE PADDING FAILURE



#### WRITE PADDING FAILURE

**R/W 214** 

## WRITE PADDING FAILURE **R/W 214**

## **PAD COMPLETE FAILURE**

#### **Pad Operation Description**

The Pad operation pads the track with clock bits from the end of the last Data field to Index. The operation is performed by the drive, independent of the controller, after a Write G3 operation (Write Data field). The controller activates Outbus Bit 2, then de-activates Outbus Bit 1 (Write Gate). This activates Pad Data Gate in the drive and the Pad operation is started. The storage control is now free to disconnect from the drive. When the drive senses Early Index, the Pad operation is reset and the Pad Attention latch is set. This activates an Attention to the storage control. The storage control reselects the drive to determine the type of Attention. The Pad Complete Attention is indicated to the Storage Control on NPL Inbus Bit 7 during a Sense Drive Status Tag.

#### **Force Pad Complete**

Microdiagnostic routine BB, test 1 forces Pad Complete by performing a 1-byte Write G3 operation and then waiting until Index is passed before checking for Pad Complete. Test 1 then deselects the drive and checks for Attention to be active.

#### **Reset Pad Complete**

Pad Complete is reset by the following:

Attention Reset. Pwr On CE Reset. Read/Write Check.

#### **Diagnostic References**

#### **READ/WRITE MICRODIAGNOSTICS**

The following microdiagnostic routines exercise the Read/Write circuits (see MICRO 10 for looping instructions):

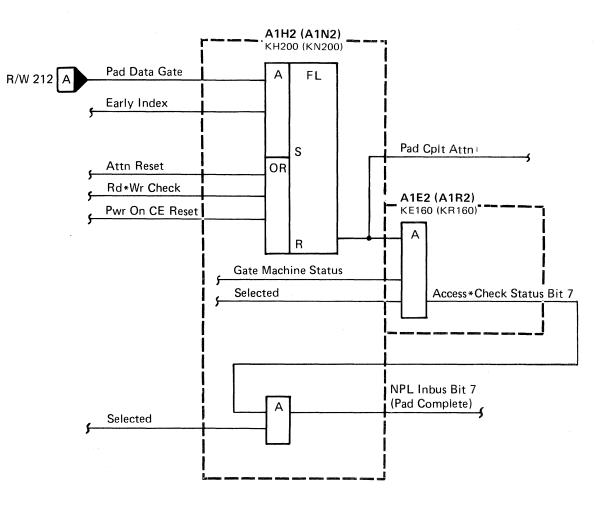
Routine A5	(MICFL 130)
Routine AD	(MICFL 240)
Routine AF	(MICFL 320)
Routine B2	(MICFL 380)
Routine B8	(MICFL 630)
Routine BB	(MICFL 740)

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#### SCOPING REFERENCES

Use the following microdiagnostic tests along with the Sequence Descriptions and charts on the indicated pages to isolate the problem:

Routine A5,	test 3	(R/W 250)
Routine AD,	test 1	(R/W 260)
Routine AD,	test 8	(R/W 266)
Routine AD,	test 9	(R/W 270)
Routine B8,	test D	(R/W 276)
Routine B8,	test F	(R/W 280)
Routine BB,	test 1	(R/W 286)



### PAD COMPLETE FAILURE **R/W 216**

## **SEQUENCE DESCRIPTION – ROUTINE A5, TEST 3**

#### **INTRODUCTION**

Use Figure 1 (Sequence Chart Description) on this page, the Sequence Chart on R/W 251, and the machine ALDs to isolate the problem.

#### **ANALYSIS PROCEDURE**

- 1. Read the Microdiagnostic Test Description.
- 2. Loop the microdiagnostic test (see Looping Instructions).
- 3. Review the Sequence Number Description column in Figure 1.
- 4. Relate the Sequence Numbers and Chart Line Numbers in Figure 1 to the Sequence Numbers and Chart Line Numbers in the Sequence Chart on R/W 251. The Sequence Number refers to the series of events as they occur in the microdiagnostic test. The Chart Line Numbers relate the lines on the Sequence Chart on R/W 251 to the events taking place in the microdiagnostic test.
- 5. The Sequence Chart on R/W 251 shows the active and inactive level for the lines used in the test. Select a sync point as noted in the Sequence Number Description column in Figure 1 and scope the drives using delayed sweep. The position of the signal scoped can be related to the Tag Gate pulses (Chart Line Number 2).

#### **MICRODIAGNOSTIC**

#### **Test Description**

Routine A5, test 3 forces a Multichip Check with the aid of a special diagnostic command (Tag '8A' Bus '02'). The test also verifies that a Read/Write Check is generated by the Multichip Check.

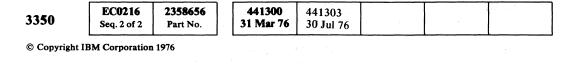
**Looping Instructions** 

#### To loop the test and bypass errors:

- 1. Load routine A5.
- 2. Enter 10, 03, 01, 00.

Figure 1. Sequence Chart Description

Test Function	Sequence Number	Sequence Number Description	Chart Line Number	Error Code	MICFL
	1	Select CE Drive	1		
	2	Drive Sync Tag (Use as a sync)	3		
	3	Attention Reset	15		
	4	Check Reset	5		
	5	Device Interface Checks (Sense Interface)	16		
Force	6	Set HAR to select additional head	8		
Multi-		Sense Read/Write	9		130
chip	7	Verify that Multichip Check is inactive (NPL Inbus Bit 0)	13	A537	
Check		Verify that Read/Write Check is inactive (NPL Inbus Bit 3)	10	A538	
	8	Diagnostic Force Multichip Check	6		
	9	Diagnostic Set Read/Write	4		
		Sense Read/Write	9		
	10	Verify that Multichip Check is active (NPL Inbus Bit 0)	13	A530	
		Verify that Read/Write Check is active	10	A531	
		Set Read/Write	4		
		Check for Error Alert active		A532	
	12	Read/Write Check Reset	7		
	13	Select CE Drive	1		
	14	Diagnostic Set Read/Write	4		
		Sense Read/Write	9		
	15	Verify that Multichip Check is inactive (NPL Inbus Bit 0)	13	A533	
		Verify that Read/Write Check is inactive (NPL Inbus Bit 3)		A534	



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#### SEQUENCE DESCRIPTION-ROUTINE A5, TEST 3

**R/W 250** 

SEQUENCE DESCRIPTION-ROUTINE A5, TEST 3

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**R/W 250** 

**SEQUENCE CHART – ROUTINE A5, TEST 3** 

Chart Line	Line Name	ALD	Tané Dalaé	Τ	- Leer					Seque	ence Ni	umbers		c						
No.			Test Point		2	3	4	5	6	7	8	9	10	11	12	13	14	15	and a second and the second and the second	
1	+Select A(B)	KK140 (KL140)	A1K2 (A1L2) G12																	
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09																	
3	—Drive Sync Tag TP	KK170 (KL170)	A1K2 (A1L2) P10							Γ										
4	+Set Read <sup>*</sup> Write	KK170 (KL170)	A1K2 (A1L2) U13																	
5	–Check Reset	KK170 (KL170)	A1K2 (A1L2) M10																	
6	+Diag Set	KG150 (KP150)	A1G2 (A1P2) B03																	
7	-Read *Write Reset	KK170 (KL170)	A1K2 (A1L2) P12																	
8	+Set HAR	KK120 (KL120)	A1K2 (A1L2) G13			Į														
9	-Sense Read <sup>*</sup> Write	KH100 (KN100)	A1H2 (A1N2) M03																	
10	-Read*Write Check TP	KH100 (KN100)	A1H2 (A1N2) J10																	
11	—Chip Sel 0 HDA	KG170 (KP170)	A1G2 (A1P2) J11								Marian I.									
12	—Chip Sel 1 HDA	KG170 (KP170)	A1G2 (A1P2) P02																	
13	+NPL Inbus Bit 0	KH200 (KN200)	A1H2 (A1N2) B05																	
14	-Multichip Selected	KH120 (KN120)	A1H2 (A1N2) J09									8								
15	-Attention Reset	KK170 (KL170)	A1K2 (A1L2) J02																	
16	+Sense Interface	KK120 (KL120)	A1K2 (A1L2) J09										-							
17																				
18								-												
19																				
20																				
21													I							
22										Ι					Γ					
23																				T

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	SEQUENC	E CHART –	ROUTINE A5	5, TEST 3	R/W 25
	2011-2011-2011-2011-2011-2011-2011-2011		Legend		Inactive leve Active level Tolerance
an alle and a second se					
				n na na na mar	

SEQUENCE CHART – ROUTINE A5, TEST 3 R/W 251

## **SEQUENCE DESCRIPTION – ROUTINE AD, TEST 1**

#### **INTRODUCTION**

Use Figure 1 (Sequence Chart Description) on this page, the Sequence Chart on R/W 261, and the machine ALDs to isolate the problem.

#### **ANALYSIS PROCEDURE**

- 1. Read the Microdiagnostic Test Description.
- 2. Loop the microdiagnostic test (see Looping Instructions).
- 3. Review the Sequence Number Description column in Figure 1 for the function selected.
- 4. Relate the Sequence Numbers and Chart Line Numbers in Figure 1 to the Sequence Numbers and Chart Line Numbers in the Sequence Chart on R/W 261. The Sequence Number refers to the series of events as they occur in the microdiagnostic test. The Chart Line Numbers relate the lines on the Sequence Chart on R/W 261 to the events taking place in the microdiagnostic test.
- 5. The Sequence Chart on R/W 261 shows the active and inactive level for the lines used in the test. Select a sync point as noted in the Sequence Number Description column in Figure 1 and scope the drives using delayed sweep. The position of the signal scoped can be related to the Tag Gate pulses (Chart Line Number 2).

#### MICRODIAGNOSTIC

#### **Test Description**

Routine AD, test 1 checks drive status to verify that I Write Sense is not active prior to the initiation of any Write operation.

The test checks that the Diagnostic Inhibit Write Gate mode is operational. This is done by orienting on Index, initiating a Write G1 operation, re-orienting on Index, and waiting for approximately 10 microseconds to get past Index. Drive status is then sensed for an active I Write Sense (NPL Inbus Bit 1).

The above sequence is repeated with Diagnostic Inhibit Write Gate mode active, then checking for an inactive I Write Sense (NPL Inbus Bit 1). This ensures that the Diagnostic Inhibit Write Gate mode circuit is operational.

The test then verifies that Gap Counter error is inactive.

The test then attempts to force a Gap Counter error by setting Diagnostic Inhibit Write Gate mode and Diagnostic Invert Bus Out Parity mode, then initiating a Write G1 operation. The microdiagnostic expects Gap Counter error, Write Data Check, and Controller error. This activity also forces Phase error. The microdiagnostic verifies that Phase error is active. The test then issues a Controller Reset and ensures that Gap Counter error and Phase error are both reset.

#### **Looping Instructions**

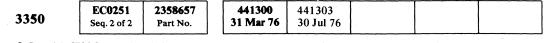
To loop the test and bypass errors:

- 1. Load routine AD.
- 2. Enter 10, 01, 01, 00.

#### Figure 1. Sequence Chart Description

1.

Test Function	Sequence Number	Sequence Number Description	Chart Line Number	Error Code	MICFL
	1	Select CE Drive (Use as a sync)	1		
		Verify that there is no outstanding Attention (NPL Inbus Bit 5)		AD12	
	2	Check Reset	4		
	3	Sense Interface	5		
		Set Read/Write	3		
	4	Verify that I Write Sense is inactive (NPL Inbus Bit 1)	7	AD13	
		Verify that I Write Sense is active (NPL Inbus Bit 1)	7	AD15	
Check	5	Check Reset	4		
Diagnostic	6	Set Read/Write	3		
Inhibit	7	Check Reset	4		240
Mode		Verify that I Write Sense is inactive (NPL Inbus Bit 1)	7	AD16	
		Set Read/Write	3		
		Verify the following:			1.
		No Gap Counter Error		AD19	
		Gap Counter Error		AD18	
	8	Write Data Check		AD1A	
		Phase Error		AD1D	
		Controller Error		AD1B	
		No Gap Counter Error		AD1C	
		No Phase Error		AD1E	
	9	Check Reset	4		



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#### SEQUENCE DESCRIPTION-ROUTINE AD, TEST 1 R/W 260

SEQUENCE DESCRIPTION-ROUTINE AD, TEST 1 **R/W 260** 

**SEQUENCE CHART – ROUTINE AD, TEST 1** 

Chart Line	Line Name	ame ALD Test Point							Sequ	ience Num	bers			
No.			Test Point		0	2	3	4		5	6		7	8
1	+Select A(B)	KK140 (KL140)	A1K2 (A1L2) G12									<b>.</b>		
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09										4	
3	+Set Read*Write	KK170 (KL170)	A1K2 (A1L2) U13											
4	Check Reset	KK170 (KL170)	A1K2 (A1L2) M10											
5	+Sense Interface	KK120 (KL120)	A1K2 (A1L2) J09											
6	Read*Write Check TP	KH100 (KN100)	A1H2 (A1N2) J10						Inact	ive				
7	+NPL Inbus Bit 1	KH200 (KN200)	A1H2 (A1N2) D05							:				
8	–Write Gate Ctrl	KH160 (KN160)	A1H2 (A1N2) G12											
9	—Sel I W	KJ100 (KM100)	A1J2 (A1M2) B02											Τ
10	+Delta I W Check	KH170 (KN170)	A1H2 (A1N2) P10						Inact	ive				
11	+Write Sel Movable HDA	KG200 (KP200)	A1G2 (A1P2) S08											Τ
12	–Read Only	KH130 (KN130)	A1H2 (A1N2) G10						Inact	ive				T
13	+Pad Gate	KH130 (KN130)	A1H2 (A1N2) S07						Inact					
14	-Read Transmit	KH170 (KN170)	A1H2 (A1N2) U04						- 36	5 bits		- 36	bits	
15														
16														
17														
18														
19						,								
20														
21				-										T
22					1		1							T
23					1		1							Ť

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SEQUENCE CHART – ROUTINE AD, TEST 1 R/W 261

			Legend:		nactive level
					Active level Tolerance
8		9			
				-	
	76	bits			
-					
	ана 1997 - Сарана 1997 - Сара			-	

SEQUENCE CHART – ROUTINE AD, TEST 1 R/W 261

## **SEQUENCE DESCRIPTION – ROUTINE AD, TEST 8**

#### **INTRODUCTION**

Use Figure 1 (Sequence Chart Description) on this page, the Sequence Chart on R/W 267, and the machine ALDs to isolate the problem.

#### **ANALYSIS PROCEDURE**

- 1. Read the Microdiagnostic Test Description.
- 2. Loop the microdiagnostic test (see Looping Instructions).
- 3. Select the function to be scoped from the Test Function column in Figure 1.
- 4. Review the Sequence Number Description column in Figure 1 for the function selected.
- 5. Relate the Sequence Numbers and Chart Line Numbers in Figure 1 to the Sequence Numbers and Chart Line Numbers in the Sequence Chart on R/W 267. The Sequence Number refers to the series of events as they occur in the microdiagnostic test. The Chart Line Numbers relate the lines on the Sequence Chart on R/W 267 to the events taking place in the microdiagnostic test.
- 6. The Sequence Chart on R/W 267 shows the active and inactive level for the lines used in the test. Select a sync point as noted in the Sequence Number Description column in Figure 1 and scope the drives using delayed sweep. The position of the signal scoped can be related to the Tag Gate pulses (Chart Line Number 2).

### MICRODIAGNOSTIC

#### **Test Description**

Routine AD, test 8 selects the CE drive, then checks for outstanding Spindle Attention. A Check Reset is issued and a check is made to make sure that Read/Write Check is inactive.

The test then forces a Control Check by activating Read Gate and Write Gate to the drive at the same time.

The test then forces a Write Overrun Check by orienting near the end of the active track, activating Write Gate to the drive, and holding it active beyond Index.

The test forces a Transition Check by activating Write Gate to the drive without Bus Out bit 4 being active.

The test forces Write Current During Read Check (Read Unsafe) by setting Multichip Select latch on, and activating Read Gate in the drive.

The test makes sure that each of the above error conditions forces a Read/Write Check. After each error is forced, the test issues a Check Reset then verifies that the error is reset.

#### **Looping Instructions**

To loop the test and bypass errors:

1. Load routine AD.

2. Enter 10, 08, 01, 00.

#### Figure 1. Sequence Chart Description

Test Function	Sequence Number	Sequence Number Description	Chart Line Number	Error Code	MICFL
Reset Read/Write	1	Select CE Drive (Use as a sync) Verify that there is no outstanding Attention (NPL Inbus Bit 5)	1	AD81	240
Checks	2	Check Reset Verify that Read/Write Check is inactive	5 10	AD82	210
	3	Set Read/Write	4		
	4	Drive Sync Tag (Use as a sync)	3		
Farra	5	Activate Read Gate and Write Gate Simultaneously	21 14		
Force Control Check	6	Sense Read/Write Verify that Control Check is active (NPL Inbus Bit 5) Verify that Read/Write Check is active	9 11 10	AD84 AD8C	240
	7	Check Reset	5		
	8	Sense Read/Write Verify that Control Check is inactive (NPL Inbus Bit 5)	9 11	AD85	
	9	Set Read/Write	4		
	10	CE Sync Point (Diagnostic Reset Read/Write) (Use as a sync)	7		
Force	11	Activate Write Gate	14		
Force Write Overrun Check	12	Sense Read/Write Verify that Write Overrun is active (NPL Inbus Bit 2) Verify that Read/Write Check is active	9 15 10	AD86 AD8D	240
	13	Check Reset	5		
	14	Sense Read/Write Verify that Write Overrun is inactive (NPL Inbus Bit 2)	9 15	AD87	: :
	15	Set HAR	8		
	16	Activate Write Gate	14		
Force Transition	17	Sense Read/Write Verify that Transition Check is active (NPL Inbus Bit 2) Verify that Read/Write Check is active	9 18 10	AD88 AD8E	240
Check	18	Check Reset	5		
	19	Sense Read/Write Verify that Transition Check is inactive (NPL Inbus Bit 6)	9 18	AD89	
	20	Set Head = 1	8	,	
	21	Attention Reset			
<b>F</b>	22	Diagnostic Set Multiheads (Use as a sync)	6		
Force Write	23	Activate Read Gate	21		
Current During Read	24	Sense Read/Write Verify that Read Unsafe is active (NPL Inbus Bit 7) Verify that Read/Write Check is active	9 20 10	AD8A AD8F	240
Check	25	Check Reset	5		
	26	Sense Read/Write Verify that Read Unsafe is inactive (NPL Inbus Bit 7)	9 20	AD8B	N B C

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SLQUENCE DESCRIPTION - ROUTINE AD, TEST 8

**R/W 266** 

SEQUENCE DESCRIPTION – ROUTINE AD, TEST 8 **R/W 266** 

**SEQUENCE CHART – ROUTINE AD, TEST 8** 

Chart Line	Line Name	ALD	Test Point										Sequ	ienc	e Numbers					
No.			i est roint	12	3	1994), 199 <sub>101</sub> - 1 <b>9</b> 01 INDE	4	5	6	7	8	9	[	0	11	12	13	14	15	1
1	+Selection A(B)	KK140 (KL140)	A1K2 (A1L2) G12									× .		-						
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09							_										
3	–Drive Sync Tag TP	KK170 (KL170)	A1K2 (A1L2) P10						Γ				Γ			Γ				
4	+Set Read <sup>*</sup> Write	KK170 (KL170)	A1K2 (A1L2) U13		***		Γ											T		
5	–Check Reset	KK170 (KL170)	A1K2 (A1L2) M10												-				Tapina Laborat & Hange Harrow	
6	+Diag Set	KK120 (KL120)	A1K2 (A1L2) G07																	Τ
7	-Read <sup>*</sup> Write Reset	KK170 (KL170)	A1K2 (A1L2) P12																	Ι
8	+Set HAR	KK120 (KL120)	A1K2 (A1L2) G13																	
9	-Sense Read *Write	KH100 (KN100)	A1H2 (A1N2) M03	• • • • • • • • • • • • • • • • • • •																
10	-Read <sup>*</sup> Write Check TP	KH100 (KN100)	A1H2 (A1N2) J10	e - verin disentes suscenses	Ī	an a														
11	+NPL Inbus Bit 5	KH200 (KN200)	A1H2 (A1N2) D02								1									Ī
12	-MST Outbus Bit 1	KH140 (KN140)	A1H2 (A1N2) M09								Ī									
13	-MST Outbus Bit 3	KH160 (KN160)	A1H2 (A1N2) U09																	
14	-Write Gate Control	KH160 (KN160)	A1H2 (A1N2) G12				· .	1	See N	lote.										
15	+NPL Inbus Bit 2	KH200 (KN200)	A1H2 (A1N2) B09			,							-							T
16	-Chip Select 7 HDA	KG170 (KP170)	A1G2 (A1P2) M05																	
17	–Head Select 2	KG170 (KP170)	A1G2 (A1P2) D07													1				Ī
18	+NPL Inbus Bit 6	KH200 (KN200)	A1H2 (A1N2) B02			-				, <sup>6</sup>		: •	- 							T
19	-MARS Unsafe	KG210 (KP210)	A1G2 (A1P2) G05	- -																
20	+NPL Inbus Bit 7	KH200 (KN200)	A1H2 (A1N2) D06									· · · · · · · · · · · · · · · · · · ·								T
21	-Read Transmit	KJ100 (KM100)	A1J2 (A1M2) B09														· · ·			T
22	Write Current HDA	KJ100 (KM100)	A1J2 (A1M2) J06			1		1				1. A.					· .			
23	MST Outbus Bit 6	KG170 (KP170)	A1G2 (A1P2) D13				1													

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Part No.

## Sequence chart – Routine Ad, test 8 R/W 267

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Inactive level Active level Tolerance

16 17 18 19 20 21 22 23 24 25 26 Note: This pulse has a very short duration and can be easily overlooked. - See Note.

SEQUENCE CHART – ROUTINE AD, TEST 8 R/W 267

## **SEQUENCE DESCRIPTION – ROUTINE AD, TEST 9**

#### **INTRODUCTION**

Use Figure 1 (Sequence Chart Description) on this page, the Sequence Chart on R/W 271, and the machine ALDs to isolate the problem.

#### **ANALYSIS PROCEDURE**

- 1. Read the Microdiagnostic Test Description.
- 2. Loop the microdiagnostic test (see Looping Instructions).
- 3. Select the function to be scoped from the Test Function column in Figure 1.
- 4. Review the Sequence Number Description column in Figure 1 for the function selected.
- 5. Relate the Sequence Numbers and Chart Line Numbers in Figure 1 to the Sequence Numbers and Chart Line Numbers in the Sequence Chart on R/W 271. The Sequence Number refers to the series of events as they occur in the microdiagnostic test. The Chart Line Numbers relate the lines on the Sequence Chart on R/W 271 to the events taking place in the microdiagnostic test.
- 6. The Sequence Chart on R/W 271 shows the active and inactive level for the lines used in the test. Select a sync point as noted in the Sequence Number Description column in Figure 1 and scope the drives using delayed sweep. The position of the signal scoped can be related to the Tag Gate pulses (Chart Line Number 2).

#### MICRODIAGNOSTIC

#### **Test Description**

Routine AD, test 9 verifies proper operation of the Head Short Check, Pad Gate Check, and Delta I Write Check circuits.

The test first verifies that the 11 error bits and Read/Write Check are inactive. The test then forces a Pad Gate Check, Head Short Check, and Delta I Write Check using the Drive Diagnostic command. Read/Write Check is forced as a result of the above errors. The test then issues a Check Reset and expects all the error bits to be reset, including the Read/Write Check.

#### **Looping Instructions**

#### To loop the test and bypass errors:

- 1. Load routine AD.
- 2. Enter 10, 09, 01, 00.

Figure 1.	Sequence	Chart	Description
-----------	----------	-------	-------------

Test Function	Sequence Number	Sequence Number	Chart Line Number	Error Code	MICFL
		Select CE Drive ( <b>Use as a sync</b> ) Verify that there is no outstanding Attention (NPL Inbus Bit 5) Verify that there is no Drive Check (NPL Inbus Bit 2)	1 21 18	AD91 AD90	
	2	Sense Interface	23		
Reset	3	Check Reset	5		
Read/Write	4	Set HAR = Head 1	6		240
Check	5	Sense Status 0 Verify that Pad Check is inactive (NPL Inbus Bit 5) Verify that Head Short Check is inactive (NPL Inbus Bit 4)	12 21 20	AD92 AD99	240
	6	Sense Read/Write Verify that Delta I Write Check is inactive (NPL Inbus Bit 4) Verify that Read/Write Check is inactive	7 20 4	AD9C AD93	
	7	Set Read/Write	3	-	
	8	CE Drive Sync (Use as a sync)	8		
	9	Set Drive Diag. Mode = Force Head Short Check	11		
	10	Raise Write Gate to Drive	10		
Force	11	Sense Status 0	12	·	
Head Short Check	12	Reset Potential Intf Check Verify that Head Short Check is active (NPL Inbus Bit 4) Verify that Read/Write Check is active	11 20 4	AD98 AD95	240
1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 -	13	Select CE Drive	1	and the	
	14	Check Reset	5		
	15	Sense Status 0 Verify that Head Short Check is inactive (NPL Inbus Bit 4)	12 20	AD9A	
	16	Set Read/Write	3		
	17	Set Drive Diagnostic Mode = Force Pad Gate Check	11		
Force	18	Activate Write Gate to drive	10		
Pad Gate Check	19	Sense Status 0 Verify that Pad Gate Check is active (NPL Inbus Bit 5) Verify that Read/Write Check is active	12 21 4	AD94 AD95	240
Oneck	20	Select Service Drive	1	a a a are	
	21	Check Reset	5		
	22	Sense Status 0 Verify that Pad Gate Check is inactive (NPL Inbus Bit 5)	12 21	AD96	
	23	Set HAR = Head 0	6	and the second	
	24	Set Read/Write	3		
	25	Sense Read/Write Status Verify that Delta I Write Check is inactive (NPL Inbus Bit 4)	7 20	AD9B	
	26	Sense Status 1 (Use as a sync)	14		
Force Delta I	27	Set HAR = Head 1	6		
Write	28	Set Drive Diagnostic Mode = Force Delta I Write Check	11	1.1	240
Check	29	Set Read/Write	3		240
	30	Sense Read/Write Status Verify that Delta I Write Check is active (NPL Inbus Bit 4) Verify that Read/Write Check is active	7 20 4	AD9D AD95	
	31	Check Reset	5		
	32	Sense Read/Write Status Verify that Delta I Write Check is inactive (NPL Inbus Bit 4) Verify that Read/Write Check is inactive	7 20 4	AD9E AD97	

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#### SEQUENCE DESCRIPTION – ROUTINE AD, TEST 9

**R/W 270** 

SEQUENCE DESCRIPTION – ROUTINE AD, TEST 9 **R/W 270** 

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**SEQUENCE CHART – ROUTINE AD, TEST 9** 

Chart Line	Line Name	ALD	Test Point					Seq	uence Num	nbers					
No.				1234	567	8910	1112	13 14 15	16	17 18	19	202122	2324	25	26
1	+Select A(B)	KK140 (KL140)	A1K2 (A1L2) G12												
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09												
3	+Set Read *Write	KH140 (KN140)	A1H2 (A1N2) S13					,							
4	-Read*Write Check TP	KH100 (KN100)	A1H2 (A1N2) J10												
5	Check Reset	KK170 (KL170)	A1K2 (A1L2) M10												
6	+Set HAR	KK120 (KL120)	A1K2 (A1L2) G13												
7	-Sense Read *Write	KH100 (KN100)	A1H2 (A1N2) M03												
8	Drive Sync Tag TP	KK170 (KL170)	A1K2 (A1L2) P10												
9	—Head Short	KG200 (KP200)	A1G2 (A1P2) M12			N.	— See No	ote.							
10	–Write Gate Control	KH160 (KN160)	A1H2 (A1N2) G12			×	— See No	ote.							
11	+Diag Set	KK120 (KL120)	A1K2 (A1L2) G07												
12	—Sense Status 0	KK170 (KL170)	A1K2 (A1L2) U10				68				632				
13	+Delta I Wr Check TP	KH170 (KN170)	A1H2 (A1N2) P10												
14	-Sense Status 1	KK170 (KL170)	A1K2 (A1L2) U05												
15	MST Outbus Bit 4	KK110 (KL110)	A1K2 (A1L2) P11												
16	MST Outbus Bit 2	KH170 (KN170)	A1H2 (A1N2) P09									,			
17	-Head Sel 1	KG170 (KP170)	A1G2 (A1P2) D10												
18	+NPL Inbus Bit 2	KH200 (KN200)	A1H2 (A1N2) B09			Inactive	4								
19	+NPL Inbus Bit 3	KH200 (KN200)	A1H2 (A1N2) D10												
20	+NPL Inbus Bit 4	KH200 (KN200)	A1H2 (A1N2) D07												
21	+NPL Inbus Bit 5	KH200 (KN200)	A1H2 (A1N2) D02												
22	+NPL Inbus Bit 6	KH200 (KN200)	A1H2 (A1N2) B02				<u>en</u>								1
23	<b>≠S</b> ense Interface	KK120 (KL120)	A1K2 (A1L2) J09												

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			The last a made
SEQUENCE	CHART – ROUTINI	AD TEST O	R/W 271
SEQUENCE	CHART = ROUTINI	AD, IDSI 9	

Active 2728 29 30 31 32	loval
272829 30 31 32	
	g tar tri
-See Note.	
Note: This pulse has a very short duration can be easily overlooked.	and

SEQUENCE CHART – ROUTINE AD, TEST 9 R/W~271

## **SEQUENCE DESCRIPTION – ROUTINE B8 TEST D**

#### **INTRODUCTION**

Use Figure 1 (Sequence Chart Description) on this page, the Sequence Chart on R/W 277, and the machine ALDs to isolate the problem.

#### **ANALYSIS PROCEDURE**

- 1. Read the Microdiagnostic Test Description.
- 2. Loop the microdiagnostic test (see Looping Instructions).
- 3. Review the Sequence Number Description column in Figure 1 for the function selected.
- 4. Relate the Sequence Numbers and Chart Line Numbers in Figure 1 to the Sequence Numbers and Chart Line Numbers in the Sequence Chart on R/W 277. The Sequence Number refers to the series of events as they occur in the microdiagnostic test. The Chart Line Numbers relate the lines on the Sequence Chart on R/W 277 to the events taking place in the microdiagnostic test.
- 5. The Sequence Chart on R/W 277 shows the active and inactive level for the lines used in the test. Select a sync point as noted in the Sequence Number Description column in Figure 1 and scope the drives using delayed sweep. The position of the signal scoped can be related to the Tag Gate pulses (Chart Line Number 2).

#### MI

#### **Test Description**

Routine B8, test D makes sure that Set R/W Tag '85' operates error free.

#### **Looping Instructions**

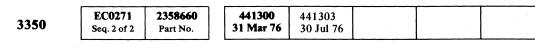
To loop the test and bypass errors:

- 1. Load routine B8.
- 2. Enter 10, 00, 01, 00.

Figure 1. Sequence Chart Description

Test Function	Sequence Number	Sequence Number Description	Chart Line Number	Error Code	MICFL
		Select CE Drive (Use as a sync)	1		• •
	2	Sense Interface	5		
Check	3	Check Reset	4		
Set		Verify that Controller Status Byte is OK	este de la	B8D0	
Read/Write	4	Set Read/Write	3		
Tag '85'		Verify that Normal End is inactive	and the second sec	B8D1	630
	Λ	Check for Error Alert	and the second second		
		If Error Alert is active, check for Controller Check active			
		If Controller Check is not active, check for Read/Write Check active			
÷ 1		If Read/Write Check is active, check for:			
		Read/Write Safety Checks active		B8D8	and and a second se
		Sense Status 0 Checks active		B8DA	
		(False) Read/Write Check active		B8D9	18-14 19-16

CRODIAGN	OSTIC		



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#### **R/W 276 SEQUENCE DESCRIPTION – ROUTINE B8 TEST D**

SEQUENCE DESCRIPTION – ROUTINE B8 TEST D

**SEQUENCE CHART – ROUTINE B8, TEST D** 

Chart				T	Sequence I	Numbers		 				
Line No.	Line Name	ALD	Test Point		2	3	4					
1	+Select A(B)	KK140 (KL140)	A1K2 (A1L2) G12		na produkti na	ት በመቀት በ 1 መቀት በማ ነው እን መድግኘ አንኳ ስር የሆኑ	an a	 an an a	and a subset on the subset of the set	and a second		Γ
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09						• • • •		••••••••••••••••••••••••••••••••••••••	
3	+Set Read*Write	KK170 (KL170)	A1K2 (A1L2) U13									1
4	–Check Reset	KK170 (KL170)	A1K2 (A1L2) M10						• • • • • •			
5	+Sense Interface	KK120 (KL120)	A1K2 (A1L2) J09									Ī
6	-Read <sup>*</sup> Write Check TP	KH100 (KN100)	A1H2 (A1N2) J10		Inac	tive						
7	-Attention Reset	KK170 (KL170)	A1K2 (A1L2) J02									
8												
9												
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11												
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23								 				

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C		4			
		E CHART -	ROUTINE B8	8, TEST D	R/W 27
			Legend		Inactive leve Active leve! Tolerance
an to a general lagor group of					
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SEQUENCE CHART – ROUTINE B8, TEST D R/W 277

## **SEQUENCE DESCRIPTION – ROUTINE B8, TEST F**

#### **INTRODUCTION**

Use Figure 1 (Sequence Chart Description) on this page, the Sequence Chart on R/W 281, and the machine ALDs to isolate the problem.

#### **ANALYSIS PROCEDURE**

- 1. Read the Microdiagnostic Test Description.
- 2. Loop the microdiagnostic test (see Looping Instructions).
- 3. Review the Sequence Number Description column in Figure 1 for the function selected.
- 4. Relate the Sequence Numbers and Chart Line Numbers in Figure 1 to the Sequence Numbers and Chart Line Numbers in the Sequence Chart on R/W 281. The Sequence Number refers to the series of events as they occur in the microdiagnostic test. The Chart Line Numbers relate the lines on the Sequence Chart on R/W 281 to the events taking place in the microdiagnostic test.
- 5. The Sequence Chart on R/W 281 shows the active and inactive level for the lines used in the test. Select a sync point as noted in the Sequence Number Description column in Figure 1 and scope the drives using delayed sweep. The position of the signal scoped can be related to the Tag Gate pulses (Chart Line Number 2).

#### MICRODIAGNOSTIC

#### **Test Description**

Routine B8, test F checks the operation of the Servo Off Track Error logic. Servo Off Track (Access Status Bit 2) generates a Drive Check as the primary indication, but it is always accompanied by one of the following:

Read/Write and Capable/Enable Check Read/Write Check Index Check

The servo off track error is caused by setting Read/Write latch on during a Rezero operation.

#### **Looping Instructions**

To loop the test and bypass errors:

- 1. Load routine B8.
- 2. Enter 10, 0F, 01, 00.

#### Figure 1. Sequence Chart Description

Test Function	Sequence Number	Sequence Number Descript
	1	Select CE Drive
	2	Attention Reset
	3	Check Reset
	4	Drive Sync Tag (Use as a sync)
		Rezero
	5	Verify that Busy is active (NPL Inbus B
Force	6	Sense Status 1 (Use as a sync)
Servo	7	Set Read/Write
Off	8	Sense Status 0 - Sync Point only
Track		Access Status (Sense Status 4)
Error	9	Verify that Servo Off Track Error is act
	10	Attention Reset
		Verify that Drive Check is active (NPL
		Sense Read/Write Status
		Verify that Capable/Enable Check is ac
		Verify that Index Check is active (NPL
		Verify that Read/Write Check is active
	12	Check Reset
	13	Diagnostic Go Home to reset Access Er
		Verify that Drive Check is inactive (NP
		Sense Read/Write Status
		Verify that Capable/Enable Check is in
	14	Verify that Index Check is inactive (NP
		Verify that Read/Write Check is inactiv
	15	Reselect CE Drive
	16	Rezero
		Verify that Busy is active (NPL Inbus B
	17	Access Status (Sense Status 4)
	17	Test for correct Ending Status
Yeshen are	18	Attention Reset

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SEQUENCE DESCRIPTION-ROUTINE B8, TEST F

tion	Chart Line Number	Error Code	MICFL
	1		
· · · · · · · · · · · · · · · · · · ·	10		
and a second	5	-	
	3		
	11		
Bit 6)		B8F0	
	13		
	4		
	6	-	
	12		
tive (NPL Inbus Bit 2)		B8F2	
	10		
Inbus Bit 2)		B8F3	
	7		
tive (NPL Inbus Bit 1)	9	B8F4	630
Inbus Bit 3)		B8F5	
	8	B8F6	
	5		
rors			
L Inbus Bit 2)		B8F7	
	7		
active (NPL Inbus Bit 1)	9	B8F8	(.)
PL Inbus Bit 3)		B8F9	
/e	8	B8FA	
	1		
	11		
Bit 6)		B8F0	
	12		
		B8FB	
	10		

SEQUENCE DESCRIPTION-ROUTINE B8, TEST F

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**R/W 280** 

SEQUENCE CHART ROUTINE B8, TEST F

Chart Line	Line Name	ALD	Test Point						Seq	uence Numb	oers					loter commune or oge				falsfall i standarana	***
No.			Test Fomt		2	3	4	5	6	7	8	9	10	<u> </u>	12	13	14	15	16	17	18
1	+Select A(B)	KK140 (KL140)	A1K2 (A1L2) G12																		
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09																		
3	-Drive Sync Tag TP	KK170 (KL170)	A1K2 (A1L2) P10	Τ																	Γ
4	+Set Read <sup>*</sup> Write	KK170 (KL170)	A1K2 (A1L2) U13		ar a solution of				•••••												
5	-Check Reset	KK170 (KL170)	A1K2 (A1L2) M10						••••											ang and an an angle of the second	
6	—Sense Status 0	KK170 (KL170)	A1K2 (A1L2) U10				the fact is because and												Ī		
7	-Sense Read <sup>*</sup> Write	KH100 (KN100)	A1H2 (A1N2) M03																		
8	-Read*Write Check TP	KH100 (KN100)	A1H2 (A1N2) J10																		
9	+NPL Inbus Bit 1	KH200 (KN200)	A1H2 (A1N2) D05																		
10	-Attention Reset	KK170 (KL170)	A1K2 (A1L2) J02				Î														
11	–Rezero	KK170 (KL170)	A1K2 (A1L2) M11				Î														
12	-Sense Status 4	KK170 (KL170)	A1K2 (A1L2) S08								1										
13	-Sense Status 1	KK170 (KL170)	A1K2 (A1L2) U05															:			Γ
14																					
15																					
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	SEQUE	NCE CHART	ROUTINE B8	, TEST F	R/W 281	
			Legend		nactive level active leve! folerance	
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SEQUENCE CHART ROUTINE B8, TEST F  $\sim R/W/281$ 

## **SEQUENCE DESCRIPTION – ROUTINE BB, TEST 1**

#### **INTRODUCTION**

Use Figure 1 (Sequence Chart Description) on this page, the Sequence Chart on R/W 287, and the machine ALDs to isolate the problem.

#### **ANALYSIS PROCEDURE**

- 1. Read the Microdiagnostic Test Description.
- 2. Loop the microdiagnostic test (see Looping Instructions).
- 3. Review the Sequence Number Description column in Figure 1 for the function selected.
- 4. Relate the Sequence Numbers and Chart Line Numbers in Figure 1 to the Sequence Numbers and Chart Line Numbers in the Sequence Chart on R/W 287. The Sequence Number refers to the series of events as they occur in the microdiagnostic test. The Chart Line Numbers relate the lines on the Sequence Chart on R/W 287 to the events taking place in the microdiagnostic test.
- 5. The Sequence Chart on R/W 287 shows the active and inactive level for the lines used in the test. Select a sync point as noted in the Sequence Number Description column in Figure 1 and scope the drives using delayed sweep. The position of the signal scoped can be related to the Tag Gate pulses (Chart Line Number 2).

#### **MICRODIAGNOSTIC**

#### **Test Description**

Routine BB, test 1 selects the CE drive, Write G3, checks for Pad In Progress, waits for at least 17 ms for the padding to complete, then checks that Pad In Progress is not present, and that Pad Complete is active.

#### **Looping Instructions**

To loop the test and bypass errors:

- 1. Load routine BB.
- 2. Enter 10, 01, 01, 00.

### Figure 1. Sequence Chart Description

Test Function	Sequence Number	Sequence Number Description	Chart Line Number	Error Code	MICFL
	1	Select CE Drive	1		
	2	Sense Interface (Use as a sync)	14		
	3	Check Reset	4		
	4	Attention Reset	5		
Write		Set Read/Write	3		
Padding		Verify the following:			
Test		Pad in Progress is inactive (NPL Inbus Bit 5)	10	BB12	740
	5	Pad in Progress is active (NPL Inbus Bit 5)	10	BB13	
		Error Alert is inactive		BB15	
		Pad Complete (NPL Inbus Bit 7)	16	BB16	
		Pad Complete Attention (NPL Inbus Bit 0)	12	BB17	
	6	Select CE Drive	1		
	<b>E</b> 71	Attention Reset	5		
and a second and a s	<b>7</b>	Verify that Pad Complete is inactive (NPL Inbus Bit 7)	15	BB1A	NJ. 4

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SEQUENCE DESCRIPTION – ROUTINE BB, TEST 1

**R/W 286** 

SEQUENCE DESCRIPTION – ROUTINE BB, TEST 1 R/W 286

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## **SEQUENCE CHART ROUTINE BB, TEST 1**

Chart Line	Lino Namo	Line Name ALD	T	Para ang ang ang ang ang ang ang ang ang an	Γ		Sequence Numbers						
No.		ALD	Test Point			2	3	4	5		6	7	
1	+Select A(B)	KK140 (KL140)	A1K2 (A1L2) G12										
2	+NPL Tag Gate	KK100 (KL100)	A1K2 (A1L2) P09										
3	+Set Read*Write	KK170 (KL170)	A1K2 (A1L2) U13										
4	Check Reset	KK170 (KL170)	A1K2 (A1L2) M10										
5	-Attention Reset	KK170 (KL170)	A1K2 (A1L2) J02		1								
6	–Format G3	BH140	A2Q2 D03										
7	–MST Outbus Bit 1	KK110 (KL110)	A1K2 (A1L2) S07							v F S€	e Note.		Note and a
8	–MST Outbus Bit 2	KK110 (KL110)	A1K2 (A1L2) S09										
9	+NPL Inbus Bit 5	KH110 (KN110)	A1H2 (A1N2) D02										
10	+Pad Gate	KH140 (KN140)	A1H2 (A1N2) S07										
11	+Pad Cplt Att A(B)	KH210 (KN210)	A1H2 (A1N2) P05		I								
12	+Pad Control	KH100 (KN100)	A1H2 (A1N2) M02										
13	+Sense Interface	KK120 (KL120)	A1K2 (A1L2) J09										
14	-Read *Write Check TP	KH100 (KN100)	A1H2 (A1N2) J10						Inad	l ctive		9	
15	+NPL Inbus Bit 7	KH200 (KN200)	A1H2 (A1N2) D06										
16													
17													
18													
19													
20													
21													
22													
23				1			1	1					ĺ

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SEQUENCE CHART ROUTINE BB, TEST 1 R/W 287



### **DATA CHECKS**

A Data Check is an error indicating an unsuccessful termination of a Read operation. There are four types of Data Checks: No Sync Byte Found, ECC Data Check, No Data Found, and No AM Found During Retry.

#### **NO SYNC BYTE FOUND**

No Sync Byte Found is an error indicating a failure to detect a Sync Byte prior to a field. There are four types of No Sync Byte Found errors:

- No Sync Byte Found HA field
- No Sync Byte Found Count Field
- No Sync Byte Found Key field
- No Sync Byte Found Data field

#### ECC DATA CHECK

ECC Data Check is an error indicating an unsuccessful compare of the ECC characters at the end of a field with the ECC data tabulated during the Read operation. There are four types of ECC Data checks:

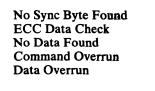
- ECC Data Check HA field
- ECC Data Check Count field
- ECC Data Check Key field
- ECC Data Check Data field

#### **NO DATA FOUND**

No Data Found is a controller error indicating that data was not detected coming from the drive during a Read operation. No Data Found is caused by the controller not detecting clock bits from the HDA during a VFO Fast Sync. VFO Fast Sync occurs in the Gap just prior to a field.

#### NO AM FOUND DURING RETRY

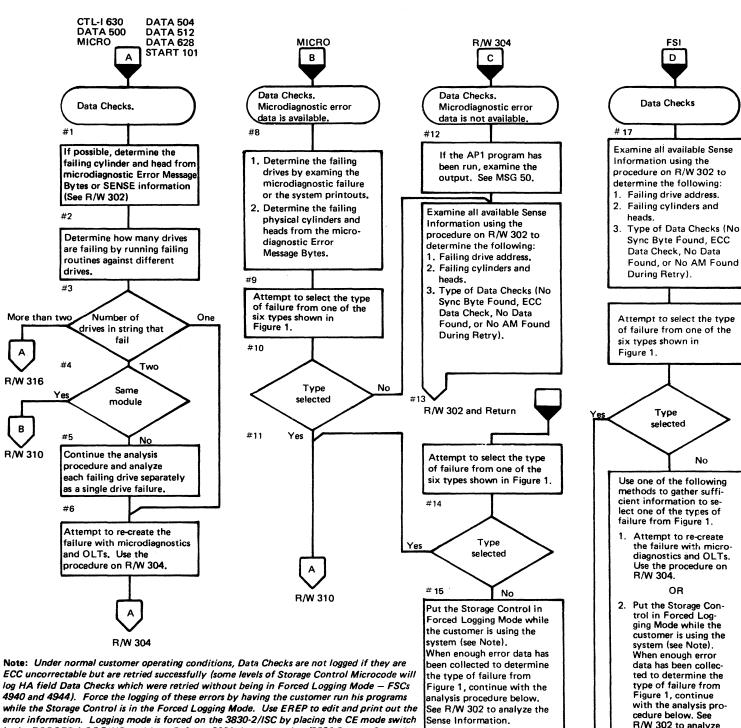
No AM Found During Retry is a microprogram detected error indicating a failure to find an Address Mark after attempting to reorient on a failing record 27 times. The initial failure causing the retry operation is due to one of the following conditions occurring in a Count or Data field of a record other than Record 0 (R0):



EC0300

Seq. 1 of 2

3350



ECC uncorrectable but are retried successfully (some levels of Storage Control Microcode will log HA field Data Checks which were retried without being in Forced Logging Mode - FSCs 4940 and 4944). Force the logging of these errors by having the customer run his programs while the Storage Control is in the Forced Logging Mode. Use EREP to edit and print out the error information. Logging mode is forced on the 3830-2/ISC by placing the CE mode switch in the FORCED LOGGING position. Refer to 3880 documentation (3880 Storage Control, 3350 MLX ENTRY 4) for information on how to place the 3880 in Forced Logging Mode.

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4

3880 MLX Chart

441311

21 Jan 81

441310

27 Jun 80

2358664

See EC

History

441308

18 Aug 78

441309

15 Jul 79

DATA CHECKS **R/W 300** 

#### Figure 1. Data Check Failure.

Γ	Types of Failures	Examples
1	Single Drive Failure RANDOM OR SINGLE TRACK FAILURE One drive with one to three tracks failing (three or less tracks fail). For example 3, also review type 4 failure.	<ol> <li>One track fails on the CE cylinder (Cylinder '0230').</li> <li>One track* fails (movable or fixed) on any cylinder.</li> <li>One head fails on 3 different cylinders.</li> <li>Three heads fail on one cylinder.</li> <li>Three or less random tracks fail.</li> </ol>
2	Single Drive Failure SINGLE HEAD FAILURE One drive with one physical head failing on more than three cylinders.	<ol> <li>One head fails on 4 cylinders.</li> <li>One head fails on 50 cylinders.</li> <li>One head fails on all cylinders.</li> </ol>
3	Single Drive Failure MULTIPLE HEAD FAILURE One drive with two or more physical heads failing on more than three tracks.*	<ol> <li>Two heads fail – one fails on one cylinder and the other fails on three cylinders.</li> <li>Four heads fail – any number of cylinders.</li> <li>All heads fail on all cylinders.</li> <li>Four fixed heads fail.</li> <li>All fixed heads fail.</li> </ol>
4	Single Drive Failure MULTIPLE FAILURES ON UPPER HEADS ONLY ('14''1D') One drive with one or more upper heads failing on multiple cylinders.	<ol> <li>One upper head fails on several cylinders.</li> <li>Two or more upper heads fail on several cylinders.</li> </ol>
5	Multiple Drive Failure SINGLE MODULE FAILURE One module (both physical drives) failing on more than three tracks* per drive. If less than three tracks per drive are failing, treat as an individual drive failure and classify each drive in types 1 or 2 above.	<ol> <li>Both drives fail on four tracks.</li> <li>Both drives fail on all tracks.</li> </ol>
6	Multiple Drive Failure MULTIPLE MODULE FAILURE More than one module or all drives on string failing on more than three tracks per drive. If less than three tracks per drive are failing, treat as an individual drive failure and classify each failing drive in types 1 or 2 above.	<ol> <li>Two modules (four drives) fall on all tracks.</li> <li>All drives fail on four tracks each.</li> <li>All drives fail on all tracks</li> </ol>

\*1 Track = 1 cylinder and 1 head

No

the Sense Informa-

tion.

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R/W 310

DATA CHECKS **R/W 300** 

## DATA CHECK SENSE BYTE ANALYSIS

#### Data Check Failures

Sense Byte 0, bit 4 = 1 indicates a Data Check.

Sense Byte 7 = '53' indicates a Data field ECC correctable Data Check. The error is corrected in main storage using the error pattern and displacement information. The error is logged.

Sense Byte 7 = 4x' indicates an ECC uncorrectable Data Check and the Fault Sumptom Code is 494x where x defines the Field and type of error. The record is retried by the Storage Control by rereading the record. If the retry operation is successful, a count is placed in bytes 14 and 15 of the Usage and Error Statistics record (Format 6). If the functional microcode disk is at E/C 437467 or later for the 3830-2/ISC or at E/C 450555E or later for a 3880, ECC uncorrectable errors in the HA Field will also be logged as a Format 4 temporary error (with Byte 1, Bit 0 = 0). If the retry operation is unsuccessful in any field after a minimum of 27 retries, the Data Check is permanent (indicated by Sense Byte 1, Bit 0 = 1) and is logged as a Format 4 record.

Logging of all ECC uncorrectable errors may be forced when it is desirable to gather detailed sense information to better analyze a problem. Logging Mode is forced on the 3830-2/ISC by placing the CE Mode switch in the Forced Logging position. Refer to 3880 documentation (3880 Storage Control, 3350 MLX ENTRY 4) for information on how to place the 3880 in Forced Logging Mode.

Sense Byte 17 = 'C0' or 'C1' indicates No Data Found. The Fault Sumptom Code is 92C0. This is the error that occurs if unable to read at all.

#### **Physical Drive Address**

Sense Byte 4 contains the bit significant drive address but does not indicate the string on multistring subsystems. The string must be determined from the logical unit address (see START 103).

#### Cylinder and Head Address

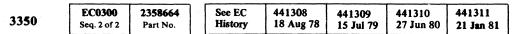
Logical cylinder and head addresses can be determined from Sense Bytes 5 and 6. The procedure on R/W 400 can be used to convert logical cylinder and head addresses to the physical cylinder and head numbers.

Sense Bytes 8 through 13 contain the Logical CCHH, Record, and Sector numbers, respectively, as read from the disk. These bytes are not valid for Data Checks in the Home Address and Count fields and are not valid for No Data Found errors.

#### **OLT 3350 PSC**

This OLT (Routine M5) will analyze a selected track or range of adjacent tracks on a single surface and develop the necessary skip displacement data to skip any defect found. This is preferable to assigning an alternate track. Do not use this OLT for data checks occurring at random addresses.

CAUTION: Data on track prior to this OLT will be destroyed.



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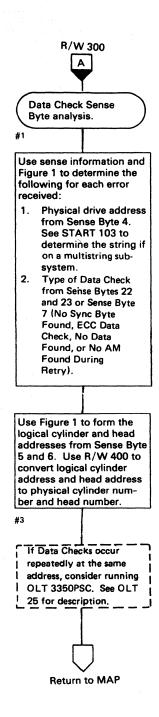
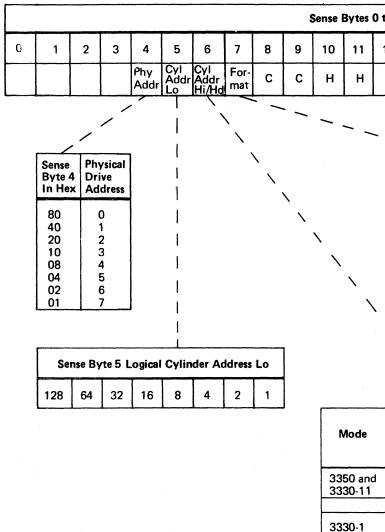


Figure 1. Sense Byte Definitions



#### DATA CHECK SENSE BYTE ANALYSIS

**R/W 302** 

						and a second					
) throu	ugh 2:	3									
12	13	14	15	16	17	18	19	20	21	22	23
R	S									Faul Sym Code	ptom
	7 (F	Sense Byte Fault 7 (Format) Symptom In Hex Code					De	script	ion		
		40 41 42		4940 4941 4942		ECC D ECC D ECC D	ata C	Count	field		
		43 44 45		4943 4944 4945			nc By	te Foi	und H	ield A field ount fi	
		46 47 49		4946 1947 1949		No Sy No AN	nc By 1 Fou	te Foi nd Du	und D Iring F		
		53 		0000* 92C0	1	ECC D No Da			Data f	ield	
*Some versions of EREP generate a pseudo Fault Symptom Code of 5353 for ECC Data Checks to use when summarizing data.											
				Se	nse By	rte 6					
	Cyli		jical Addre	ss Hi	Lo	Logical Head Address					
	-	C 5		Cyl 256	16	8	4	2	1		

8

16

Cyl 256

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4

2

### DATA CHECK SENSE BYTE ANALYSIS **R/W 302**

## **DATA CHECK ERROR RE-CREATION**

#### **Microdiagnostics**

#### **ROUTINE B1**

In Default mode, Read operations are performed on all physical movable heads on cylinder 4 and then on all fixed heads (if installed). If Data Checks occur, the routine continues on error until all heads have been read. A summary of the failing heads can then be obtained from the Error Message Bytes (Errors Codes B1FD through B1FF).

Options are available to stop on error, loop on error, and run on any selected track. See MICRO 56 for running instructions.

#### **ROUTINE B2**

Read and Write operations are performed on all physical movable heads on the CE cylinder. The sequence is as follows:

1. Seek.

- 2. Read Home Address.
- 3. Write R0 and R1.
- 4. Read R0 and R1.
- 5. Repeat Steps 2, 3, and 4 for each CE track.
- 6. Read full CE cylinder.

See MICRO 60 for running instructions.

#### OLTS

#### OLT T3350PSA

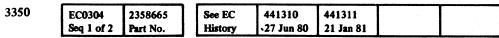
The Home Address and Record 0 are read and checked on all tracks scanned. The CCHH bytes of the Home Address are compared to the CCHH bytes of the R0 Count field. Alternate track assignment is checked to make sure that all Home Addresses that are flagged as defective point to an alternate track and that the alternate track points back to the defective track. Unused alternate tracks point back to themselves. See OLT 20 for running instructions.

#### OLT T3350PSB

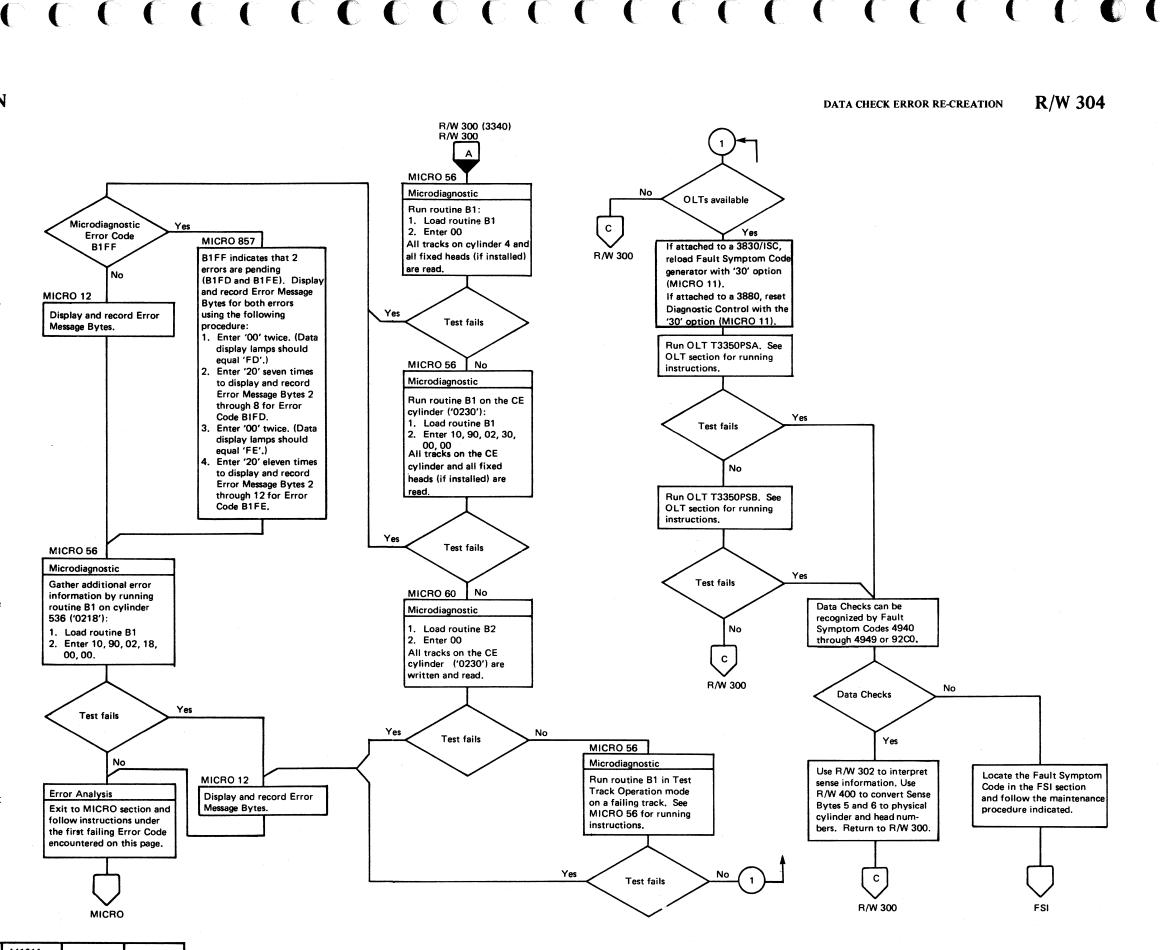
All data records are read and checked on all tracks scanned. CE cylinders are not checked. See OLT 24 for running instructions.

#### OLT T3350PSC

Creates a track-by-track directory of nonzero skip displacement information on cylinder 561. After the directory has been created, this OLT can be used to restore HA/ROs with skip displacement information obtained from the directory. This OLT can also be used to assign a skip displacement for a defective track, a method preferable to assigning an alternate track. Do not use this OLT for data checks occurring at random addresses.



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#### DATA CHECK ERROR RE-CREATION

## DATA CHECKS – UPPER HEADS

#### **Data Check Failures – Upper Heads**

ECC Uncorrectable Data Checks can occur on upper heads due to a shift of track to head position. Physical head addresses of decimal 20 through 29 (hex '14' through '1D') have been used to describe upper heads, however, the condition may occassionally be found outside of this range. Most frequently, the condition will result in Fault Symptom Codes of 4940, 4941, 4944, or 4945 and can be corrected by rewriting the HDA. OLT 3350 PSC or any utility program which completely rewrites the HDA including Home Addresses with proper skip displacements can be used.

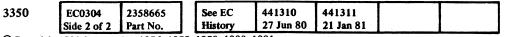
#### Format 4 Error Logging

Sense Byte 7 = 4x' indicates an ECC uncorrectable Data Check and the Fault Symptom Code is 494x where x defines the Field and type of error. The record is retried by the Storage Control by rereading the record. If the retry operation is successful, a count is placed in bytes 14 and 15 of the Usage and Error Statistics record (Format 6). If the functional microcode disk is at E/C 437467 or later for the 3830-2/ISC or at E/C 450555E or later for a 3880, ECC uncorrectable errors in the HA Field will also be logged as a Format 4 temporary error (with Byte 1, Bit 0 = 0). If the retry operation is unsuccessful in any field after a minimum of 27 retries, the Data Check is permanent (indicated by Sense Byte 1, Bit 0 = 1) and is logged as a Format 4 record.

Logging of all ECC uncorrectable errors may be forced when it is desirable to gather detailed sense information to better analyze a problem. Logging Mode is forced on the 3830-2/ISC by placing the CE Mode switch in the Forced Logging position. Refer to 3880 documentation (3880 Storage Control, 3350 MLX ENTRY 4) for information on how to place the 3880 in Forced Logging Mode.

#### Recovery

- 1. Temporary Errors Only (Sense Byte 1, Bit 0 = 0) A. Have customer dump data from HDA.
- B. Verify that an SD Directory exists on cylinder 561 of HDA. If Directory does not exist, create one using OLT 3350 PSC (see OLT 25).
- C. Rewrite HDA using OLT 3350 PSC, Routine M3 or any available utility which completely rewrites the HDA (including Home Addresses with proper skip displacements).
- 2. Permanent Errors (Sense Byte 1, Bit 0 = 1)
- A. Tracks with permanent errors cannot be read in the normal manner for data recovery. A CE tool is available to provide a slight head offset. Use of this tool will usually enable complete recovery. The tool, which is a servo card with built in offset, is available in B/M 2354577. The card P/N is 5864500.

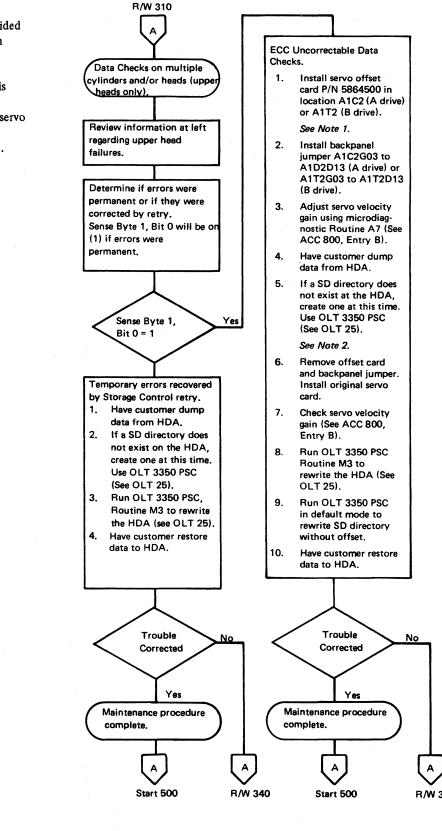


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- B. Install offset card and jumper per instructions provided with the Bill of Material. Adjust servo velocity gain using microdiagnostic routine A7.
- C. Have customer dump his data from the HDA.

D. Create new SD Directory with OLT 3350 PSC. This Directory will be offset and must be restored later.

- E. Remove offset card and jumper. Reinstall original servo card and verify servo velocity gain.
- F. Rewrite the HDA with OLT 3350 PSC Routine M3.
- G. Create new SD Directory with OLT 3350 PSC.
- H. Return machine to customer and check for proper operation.



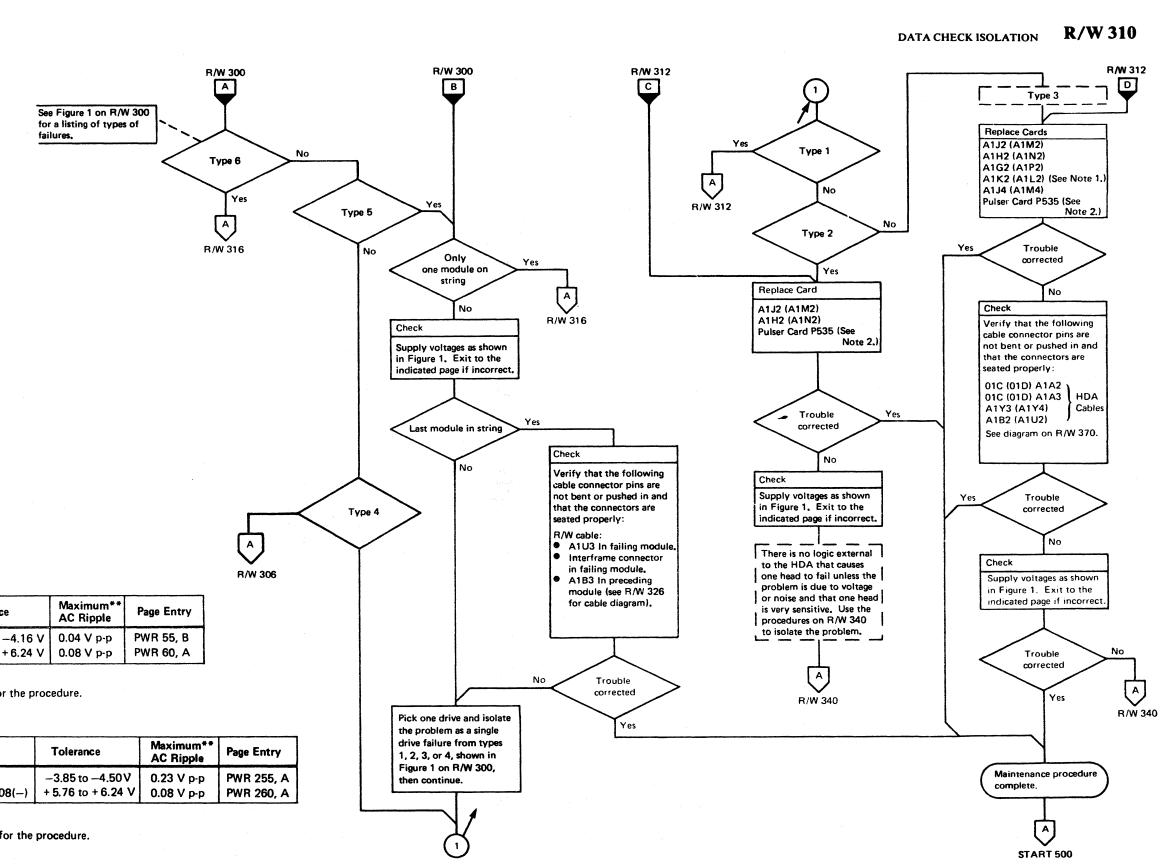
Note 1: Bill of Material 2354577 contains servo offset card 5864500 and is available as a FE Regional tool or as an "as required" Field Bill.

Note 2: This step creates an SD Directory which is offset from the normal head tracking position by the servo offset card. The SD Directory must be rewritten after the offset card is removed and the HDA rewrite is completed.

R/W 340

**DATA CHECKS – UPPER HEADS** 

## DATA CHECK ISOLATION



Note 1: When replacing A1K2(A1L2), check the addressing jumpers. See INST 6.

Note 2: To determine if the pulser card is causing the failure, either disconnect P535 from the pulser card (the drive will run with P535 disconnected) or disconnect P535. rotate it by 180 degrees, and reconnect P535 (this moves the problem from one drive to the other).

#### Figure 1. Voltage Charts

#### Controller

Voltage*	Test Point	Tolerance	Maximum** AC Ripple	Page Entry
-4 V	A2T2B06(-) to A2T2D08(+)	-3.84 to -4.16 V	0.04 V p-p	PWR 55, B
+6 V	A2T2G11(+) to A2T2J08(-)	+ 5.76 to + 6.24 V	0.08 V p-p	PWR 60, A

\* Use a digital voltmeter to check voltages.

\*\* Use a scope to measure the ripple. See PWR 90 for the procedure.

#### Drive

Voltage*	Test Point	Tolerance	Maximum** AC Ripple	Page Entry
-4 V	A1C2 (A1T2) B06(-) to A1K2D08(+)	-3.85 to -4.50 V	0.23 V p-p	PWR 255, A
+6 V	A1F2 (A1Q2) B11(+) to A1F2 (A1Q2) D08(-)	+ 5.76 to + 6.24 V	0.08 V р-р	PWR 260, A

Use a digital voltmeter to check voltages.

\*\* Use a scope to measure the ripple. See PWR 290 for the procedure.

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DATA CHECK ISOLATION

## **DATA CHECK SINGLE TRACK**

#### **ISOLATED SINGLE TRACK FAILURES**

#### Skip Displacement

A single defective track can usually be corrected by using a Skip Displacement. The displacement can be developed and assigned using OLT 3350PSC (see OLT 25).

Note: This method applies to either movable or fixed heads and is preferable to alternate track assignment described below.

#### Alternate Track Assignment

A single defective track is re-assigned by the customer to an alternate track (see OLT 30). Tracks that are flagged as defective and their assigned alternates can be determined by running OLT 3350PSA (see OLT 220). For further information on alternate tracks, see OLT 30.

#### **Fixed Head Track Failures**

A defective fixed head track can be re-assigned by the customer to one of the movable head alternate tracks. If this is not acceptable to the customer, the only alternative is to replace the HDA.

Note: See Skip Displacement, above.

**Note:** To determine if the pulser card is

P535 disconnected) or disconnect P535,

rotate it by 180 degrees, and reconnect

P535 (this moves the problem from one

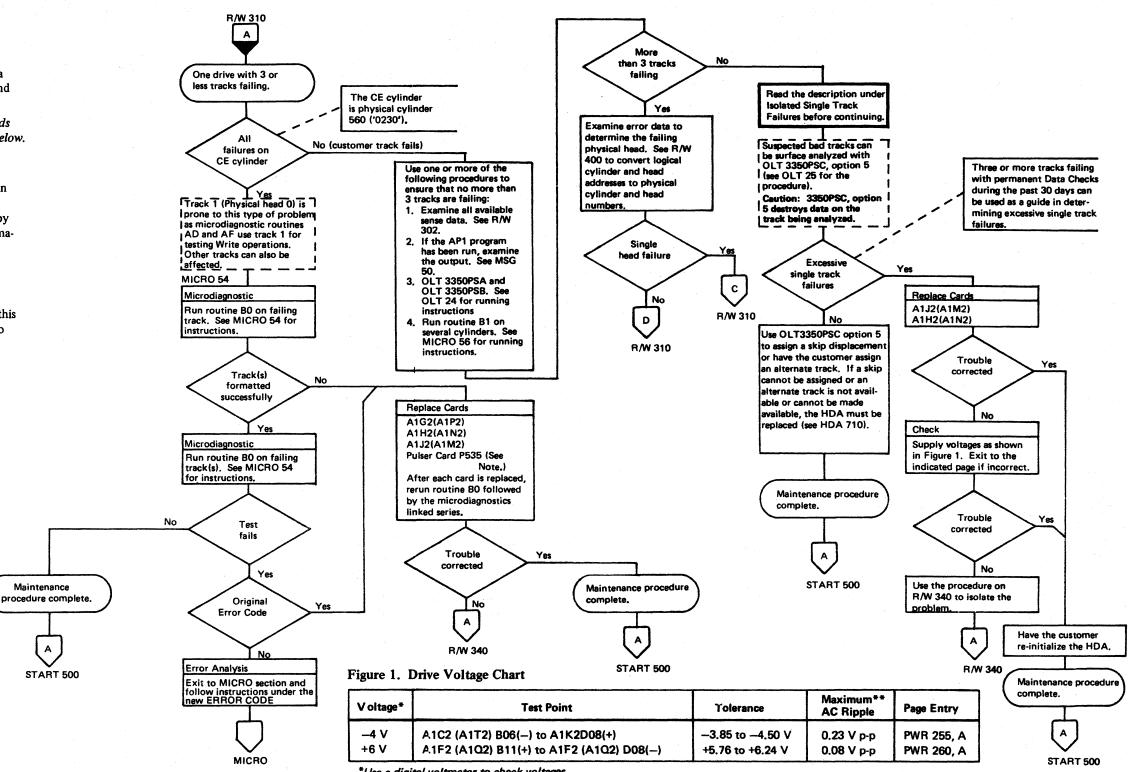
EC0310

drive to the other).

3350

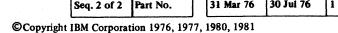
causing the failure, either disconnect P535

from the pulser card (the drive will run with



\*Use a digital voltmeter to check voltages.

\*\* Use a scope to measure the ripple. See PWR 290 for the procedure.



2358666

Part No.

A

441306

1 Apr 77

441310

27 Jun 80

441303

30 Jul 76

441300

31 Mar 76

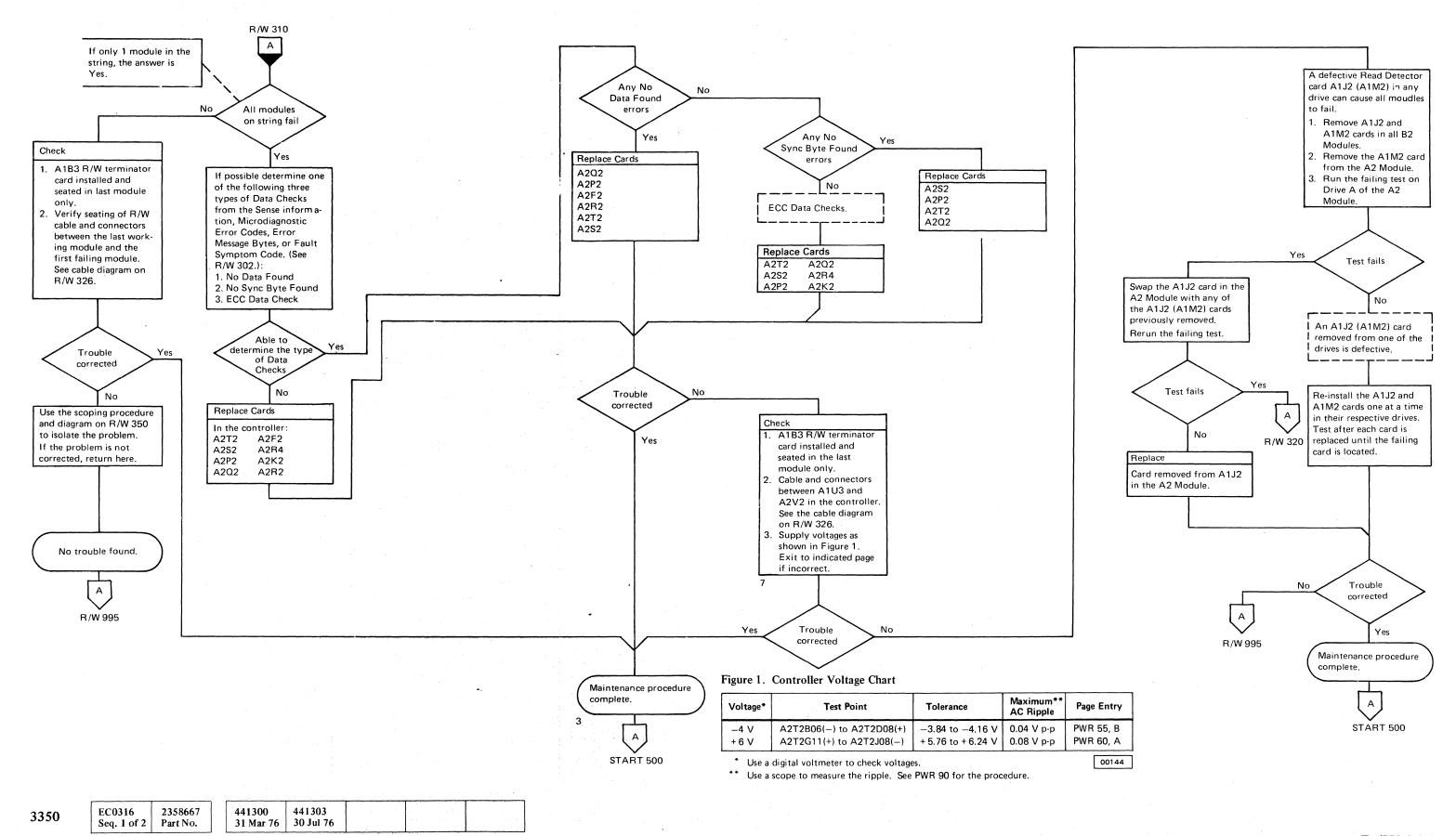
441311

21 Jun 81

DATA CHECK SINGLE TRACK

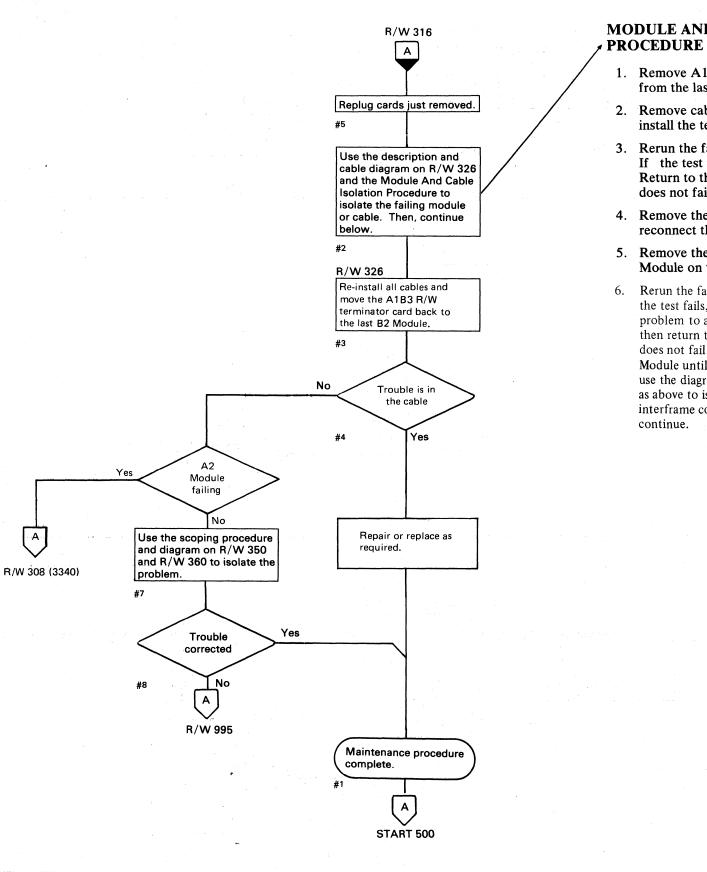
**R/W 312** 

## **DATA CHECK ANALYSIS**



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#### DATA CHECK ANALYSIS **R/W 316**



3350	EC0316 Seq. 2 of 2	2358667 Part No.	441300 31 Mar 76	441303 30 Jul 76		

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### **MODULE AND CABLE ISOLATION**

1. Remove A1B3 (R/W and PLO terminator card) from the last module on the string.

2. Remove cable from A1B3 in the A2 Module and install the terminator card.

3. Rerun the failing test on Drive A of the A2 Module. If the test fails, the problem is in the A2 Module. Return to the flowchart and continue. If the test does not fail, continue with the next step.

4. Remove the terminator card from A1B3 and reconnect the cable.

5. Remove the cable from A1B3 in the first B2 Module on the string and install the terminator card.

6. Rerun the failing test on Drive A of the A2 Module. If the test fails, use the diagram on R/W 326 to isolate the problem to a module, cable, or interframe connector, then return to the flowchart and continue. If the test does not fail, repeat Steps 4 through 6 on each B2 Module until the problem is isolated to a module, and use the diagram on R/W 326 and the same procedure as above to isolate the problem to a module, cable, or interframe connector, then return to the flowchart and

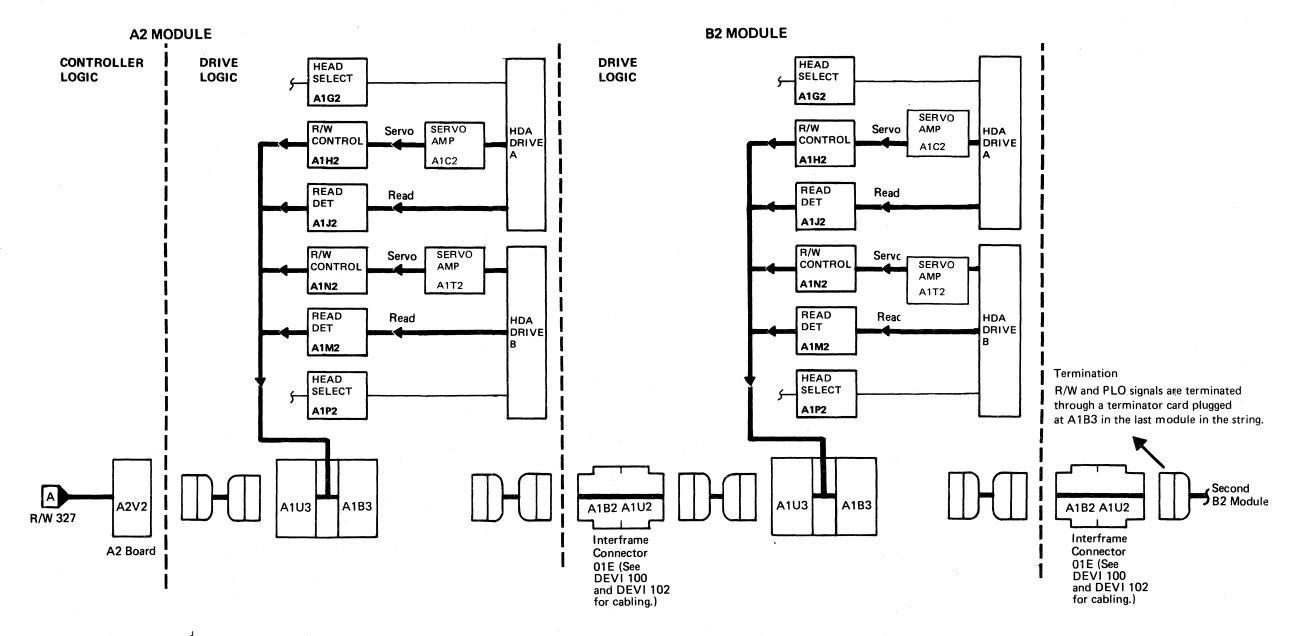
continue.

### DATA CHECK ANALYSIS **R/W 320**

C

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# **READ DATA PATH**



2250	EC0326 Seq. 1 of 1	2358668 Part No.		441300 31 Mar 76	441303 30 Jul 76	441308 18 Aug 78			
------	-----------------------	---------------------	--	---------------------	---------------------	---------------------	--	--	--

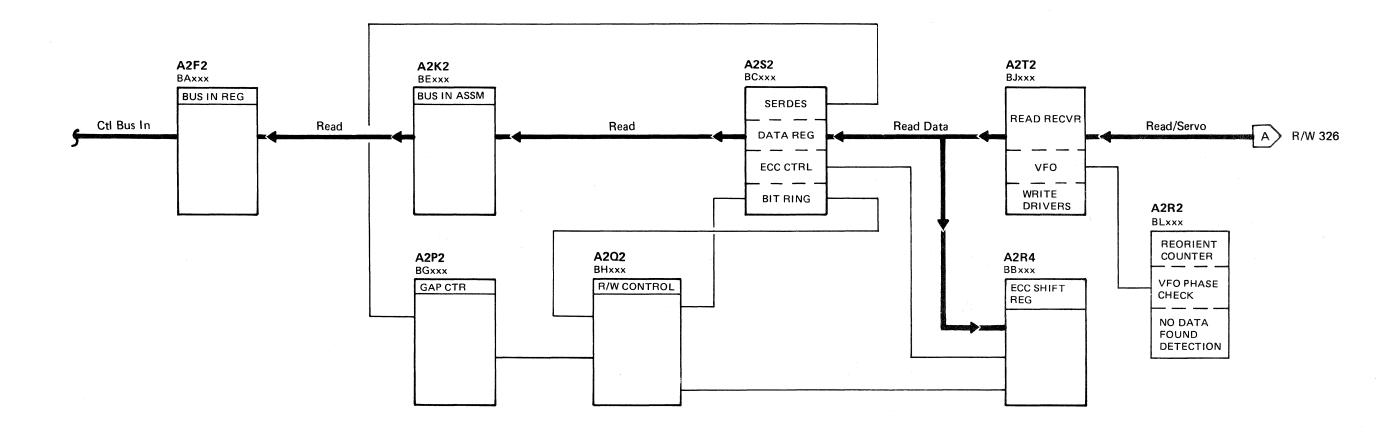
READ DATA PATH **R/W 326** 

READ DATA PATH **R/W 326** 



**READ DATA PATH** 

CONTROLLER



3350	EC0327 Seq. 1 of 2	2358669 Part No.		441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77			
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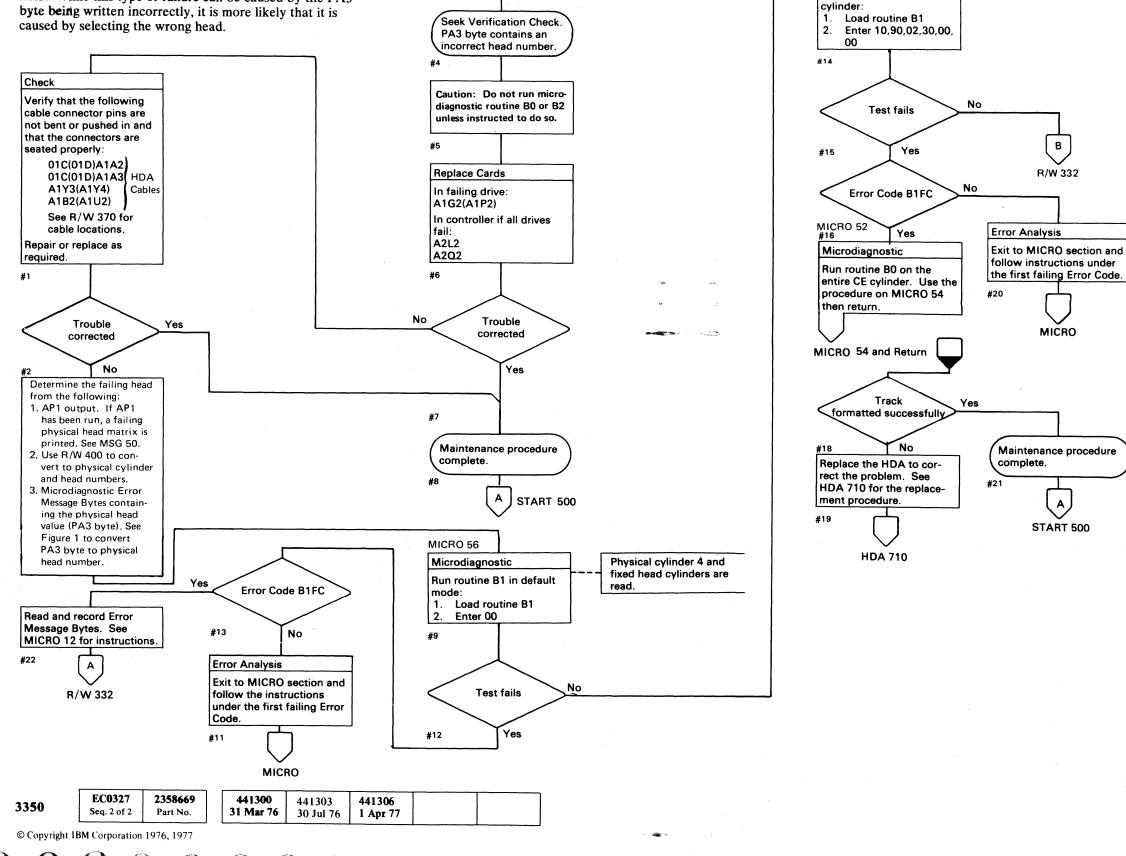


# READ DATA PATH **R/W 327**

### READ DATA PATH **R/W 327**

# **HEAD SELECTION FAILURE**

Head selection failures are detected after a Seek operation by reading an incorrect physical address from the PA3 byte in the Home Address or from the Count field. While this type of failure can be caused by the PA3 byte being written incorrectly, it is more likely that it is



ACC 501

A

MICRO 56

Microdiagnostic

Run routine B1 on the CE

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HEAD SELECTION FAILURE **R/W 330** 

Figure 1.	PA3 Byte Conversion to Physical Head
•	Number

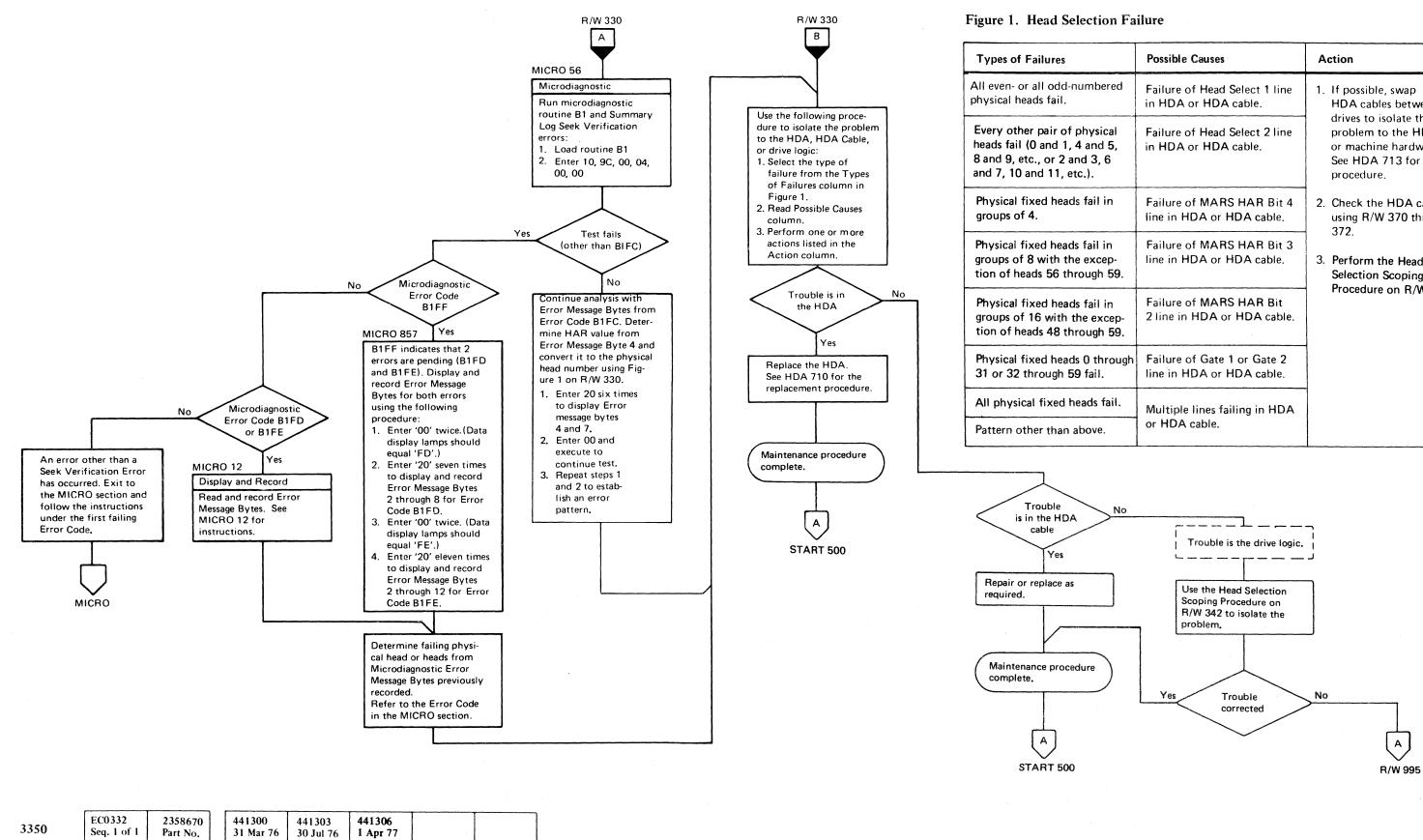
Movab	le Head		Fixed Hea	ds	
Hex Value PA3	Movable Head Number	Hex Value PA3	Fixed Head Number	Hex Value PA3	Fixed Head Number
00	00	40	00	7C	30
02	01	42	01	7E	31
04	02	44	02	80	32
06	03	46	03	82	33
08	04	48	04	84	34
0A	05	4A	05	86	35
0C	06	4C	06	88	36
0E	07	4E	07	8A	37
10	08	50	08	8C	38
12	09	52	09	8E	39
14	10	54	10	90	40
16	11	56	11	92	41
18	12	58	12	94	42
1A	13	-5A	13	96	43
1C	14	5C	14	98	44
1E	15	5E	15	9A	45
20	16	<b>6</b> 0	16	9C	46
22	17	62	17	9E	47
24	18	64	18	A0	48
26	19	66	19	A2	49
28	20	68	20	A4	50
2A	21	6A	21	A6	51
2C	22	6C	22	A8	52
2E	23	6E	23	AA	53
30	24	70	24	AC	54
32	25	72	25	AE	55
34	26	74	26	B0	56
36	27	76	27	B2	57
38	28	78	28	B4	58
3A	29	- 7A	29	B6	59、

HEAD SELECTION FAILURE **R/W 330** 

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# **HEAD SELECTION FAILURE**



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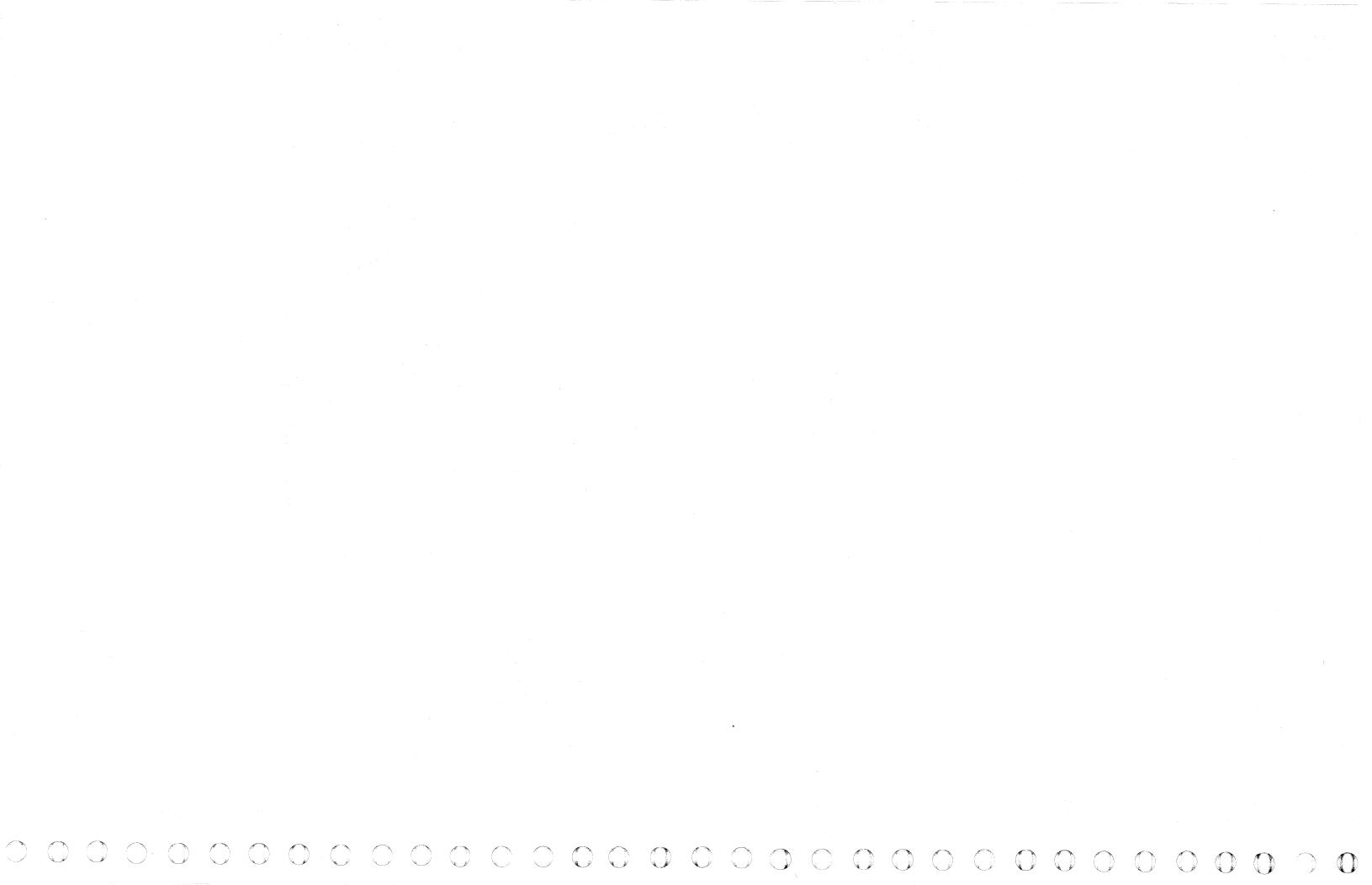
HEAD SELECTION FAILURE

R/W 332

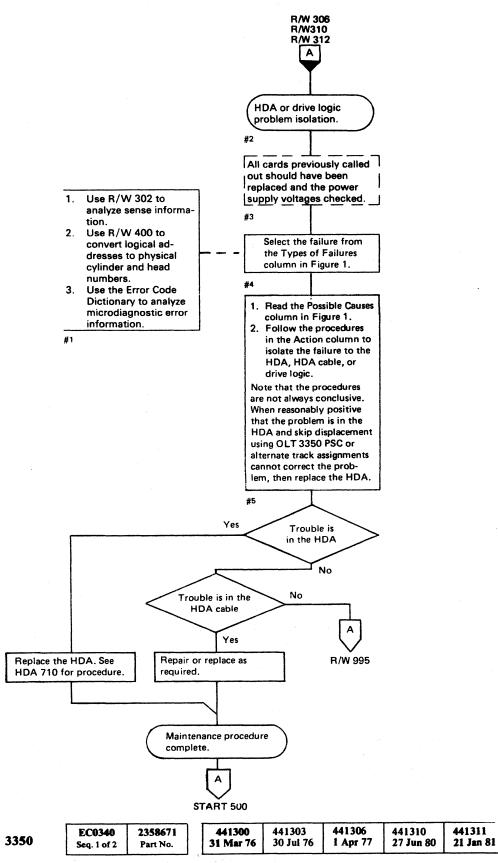
1		,
	Possible Causes	Action
ed	Failure of Head Select 1 line in HDA or HDA cable.	<ol> <li>If possible, swap HDA cables between drives to isolate the</li> </ol>
al 5,	Failure of Head Select 2 line in HDA or HDA cable.	problem to the HDA or machine hardware. See HDA 713 for the procedure.
ו	Failure of MARS HAR Bit 4 line in HDA or HDA cable.	2. Check the HDA cable using R/W 370 through 372.
) 5- 59.	Failure of MARS HAR Bit 3 line in HDA or HDA cable.	3. Perform the Head Selection Scoping
n ep- 59.	Failure of MARS HAR Bit 2 line in HDA or HDA cable.	Procedure on R/W 342.
ough	Failure of Gate 1 or Gate 2 line in HDA or HDA cable.	
il.	Multiple lines failing in HDA or HDA cable.	

**R**/W 332

#### HEAD SELECTION FAILURE



# DATA CHECK (HDA Isolation)



#### Figure 1. Failure Isolation

Types of Failures	Possible Causes	Ac
All Movable heads on the same arm fail. Arm Physical Heads 0 0 to 3 1 4 to 7 Head 19 2 8 to 11 is not used 3 12 to 15 for 3330 4 16 to 19 Compatibility 5 20 to 23 Mode 6 24 to 27 7 28 and 29	<ol> <li>HDA internal logic.</li> <li>A Chip Select line in the HDA cable or logic board land pattern.</li> <li>Physical Chip Heads Select</li> <li>0 to 3</li> <li>4 to 7</li> <li>8 to 11</li> <li>12 to 15</li> <li>16 to 19</li> <li>4</li> <li>20 to 23</li> <li>5</li> <li>24 to 27</li> <li>8 and 29</li> <li>7</li> </ol>	1. 2. 3. 4. 5.
Fixed Heads 0 through 31 (Address 32 through 63) or 32 through 59 (address 64 through 91) fail. Heads 57, 58, and 59 are not used for 3330 Compatibility Mode (movable heads do not fail).	<ol> <li>HDA internal logic.</li> <li>Fixed Heads 0 through 31 or Fixed Heads 32 through 59 lines in the HDA cable or logic board land pattern.</li> </ol>	
All fixed heads fail. Movable heads do not fail.	<ol> <li>HDA internal logic.</li> <li>+6 V to MARS Module, Fixed Hd Select Gate, or Fixed Heads Data X, or Fixed Heads Data Y lines in the HDA cable or logic board land pattern.</li> </ol>	1. 2. 3. 4. 5. 6.
Failures on upper heads only. (Decimal 20 through 29, Hex '14' through '1D' as a guide.)	1. Possible shift of track to head position.	1.
None of the above.	<ol> <li>Bad head or internal logic to the HDA.</li> <li>Voltages or noise.</li> <li>HDA cable Data X or Data Y lines.</li> <li>Noisy power amplifier in the adjacent drive.</li> <li>Servo off track.</li> </ol>	1. 2. 3. 4. 5. 6. 7. 8. 9.

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# DATA CHECK (HDA Isolation) R/W 340

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	Swap HDA cables. See HDA 713 for procedure. Note: If cables cannot be swapped, continue with Step 2. Check HDA cables. See R/W 370 through 372 for procedure. Scope Head Select lines. See R/W 342 for procedure. Replace HDA. See HDA 710 for procedure. Trouble not found. Go to R/W 995, Entry A.
	Swap HDA cables. See HDA 713 for procedure. Note: If cables cannot be swapped, continue with Step 2. Check HDA voltages. See R/W 376 for procedure. Check HDA cables. See R/W 370 through 372 for procedure. Scope Head Select lines. See R/W 342 for procedure. Replace HDA. See HDA 710 for procedure. Trouble not found. Go to R/W 995, Entry A.
	If not already done, follow procedure on R/W 306 to recover data and rewrite HDA.
	Swap HDA cables. See HDA 713 for procedure. Note: If cables cannot be swapped, continue with Step 2. Check HDA voltages. See R/W 376 for procedure. Check HDA cables. See R/W 370 through 372 for procedure. Scope read data. See R/W 346 for procedure. Check base plate grounding. See R/W 378 for procedure. Perform Servo/HDA Checkout. See ACC 660 for the procedure. Replace power amplifier in adjacent drive. See LOC 4 or 14. Use OLT 3350 PSC to assign a skip displacement if errors are limited to 1 or 2 tracks. Do not use if errors are recurring on random addresses. If skip displacement cannot be assigned have customer assign alternate tracks or replace HDA. See HDA 710 for replacement procedure. Trouble not found. Go to R/W 995, Entry A.

DATA CHECK (HDA Isolation) R/W 340

#### HEAD SELECTION SCOPING PROCEDURE

#### PURPOSE

The purpose of the Head Selection Scoping Procedure is to check that all head selection lines are at the correct level with:

- 1. A Static Check with no heads selected.
- 2. A Dynamic Check while looping a microdiagnostic that selects a single head.

#### **STATIC CHECK**

#### Microdiagnostic

Power on the drive and do not load microdiagnostics.

#### Action

Check all Head Select lines for the inactive level using Figure 1. See Note.

Are the signals correct for all lines?

- Yes---- Perform Dynamic Check.
- No----- ► Use the cable checkout procedure on R/W 372 and the ALDs to isolate the problem.

#### **DYNAMIC CHECK**

#### Microdiagnostic

Loop routine B1 on a failing head and bypass errors.

1. Load routine

2. See MICRO 56 for parameter entries.

Use R/W 344 to determine which Select lines should be active and inactive for the head selected in the microdiagnostic.

#### Scope Setup

Sweep  $20 \,\mu s/div$ Trigger Slope (+) A1H2(A1N2)M05 +Selected A(B) Ch 1 See Figures 1 through 4. Ch 2

#### Action

Check all Head Select lines for the proper levels (active and inactive) using Figures 1 through 4. All scope pictures (Figures 2 through 4) show the active level.

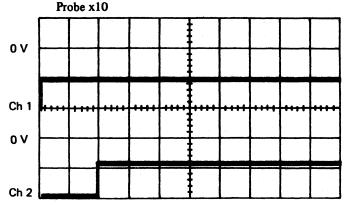
Are the signals correct for all Head Select lines?

- Yes— Return to MAP.
- No----  $\blacktriangleright$  Use the cable checkout procedure on R/W 372 and the ALDs to isolate the problem.



Ch 1 A1G2(A1P2)S02 +Selected A(B) Volts/div 0.1 Probe x10

Ch 2 + Movable (or Fixed) Hd Select Gate (See Figure 1.) Volt/div 0.1



#### Figure 1. Head Selection

Line Name*	Pin Location	Active Level	Inactive Level
+ Movable Hd Select Gate	A1G2 (A1P2) P12	+MST	-MST
+ Fixed Hd Select Gate	A1G2 (A1P2) P10	+MST	-MST
-Chip Select 0	A1G2 (A1P2) J11	Gnd	+6∨
-Chip Select 1	A1G2 (A1P2) P02		
-Chip Select 2	A1G2 (A1P2) M03		
-Chip Select 3 (See	A1G2 (A1P2) P04		
-Chip Select 4 Note)	A1G2 (A1P2) M04	1.00	
-Chip Select 5	A1G2 (A1P2) M02		
-Chip Select 6	A1G2 (A1P2) P03		
-Chip Select 7	A1G2 (A1P2) M05		↓ ↓
-Fixed Heads 32-59	A1G2 (A1P2) S09	-MST	+MST
-Fixed Heads 0-31	A1G2 (A1P2) S10		
-MARS HAR Bit 2	A1G2 (A1P2) U11		
-MARS HAR Bit 3	A1G2 (A1P2) U12		
-MARS HAR Bit 4	A1G2 (A1P2) U10		
-Head Sel 1	A1G2 (A1P2) D10		
-Head Sel 2	A1G2 (A1P2) D07	+ :	°. ♦

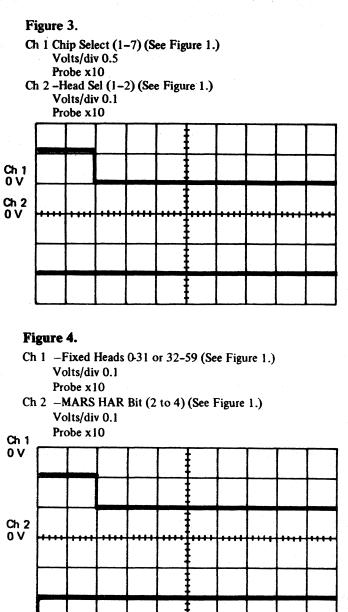
\*All lines listed may be found on ALD page KG170 (Drive A) or KP170 (Drive B).

Note: The +6 V measured on a Chip Select line during the inactive state comes from the HDA, not the driver card. An open Chip Select line causes the voltage at the driver card, A1G2(A1P2), to float to the ground level. A Chip Select line shorted to ground causes multichip select failures, not Data Checks.

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#### HEAD SELECTION SCOPING PROCEDURE R/W 342



#### HEAD SELECTION SCOPING PROCEDURE **R/W 342**

# HEAD SELECTION SCOPING PROCEDURE

#### Movable Heads

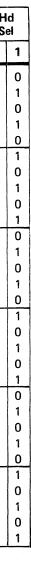
	Fixed Heads										
Physical Fixed He	ads	Chip	Fix Hea			RS R B	its		d el		
Decimal	Hex	Sel	32/59	0/31	2	3	4	2	1		
0	'0'	-	0	1	0	0	0	0	0		
1	11'	-	0	1	0	0	0	0	1		
2	'2'	-	0	1	0	0	0	1	0		
3	'3'		0	1	0	0	0	1	1		
4	'4'	-	0	1	0	0	1	0	0		
5	'5'	-	0	1	0	0	1	0	1		
6	'6'	-	0	1	0	0	1	1	0		
7	'7'		0	1	0	0	1	1	1		
8	'8'	-	0	1	0	1	0	0	0		
9	'9'		0	1	0	1	0	0	1		
10	'A'		0	1	0	1	0	1	0		
11	'B'		0	1	0	1	0	1	1		
12	'C'	-	0	1	0	1	1	0	0		
13	'D'	-	0	1	0	1	1	0	1		
14	'E'	-	0	1	0	1	1	1	0		
15	'F'	-	0	1	0	1	1	1	1		
16	'10'	-	0	1	1	0	0	0	0		
17	'11'	-	0	1	1	0	0	0	1		
18	'12'		0	1	1	0	0	1	0		
19	'13'	`	0	1	1	0	0	1	1		
20	'14'	_	0	1	1	0	1	0	0		
21	'15'		0	1	1	0	1	0	1		
22	'16'	_	0	1	1	0	1	1	0		
23	'17'		0	1	1	0	1	1	1		
24	'18'		0	1	1	1	0	0	0		
25	'19'	-	0	1	1	1	0	0	1		
26	'1A'	_	0	1	1	1	0	1	0		
27	'1B'		0	1	1	1	0	1	1		
28	'1C'	_	0	1	1	1	1	0	0		
29	'1D'	_	0	1	1	1	1	0	1		

Fixed Heads

Fixed HeadsChip SelHeadsHAR BitsSel $32/59$ $0/31$ $2$ $3$ $4$ $2$ $30$ '1E' $ 0$ $1$ $1$ $1$ $1$ $1$ $31$ '1F' $ 0$ $1$ $1$ $1$ $1$ $1$ $32$ '20' $ 1$ $0$ $0$ $0$ $0$ $33$ '21' $ 1$ $0$ $0$ $0$ $0$ $34$ '22' $ 1$ $0$ $0$ $0$ $0$ $36$ '24' $ 1$ $0$ $0$ $0$ $1$ $36$ '24' $ 1$ $0$ $0$ $0$ $1$ $37$ '25: $ 1$ $0$ $0$ $1$ $0$ $38$ '26' $ 1$ $0$ $0$ $1$ $0$ $39$ '27' $ 1$ $0$ $0$ $1$ $0$ $41$ '29' $ 1$ $0$ $0$ $1$ $0$ $41$ '29' $ 1$ $0$ $0$ $1$ $0$ $44$ '2C' $ 1$ $0$ $0$ $1$ $1$ $44$ '2C' $ 1$ $0$ $0$ $1$ $1$ $44$ '2C' $ 1$ $0$ $1$ $1$ $0$ $44$ '2C' $ 1$ $0$ $1$ $1$ $0$ $44$ '2C' $ 1$ $0$ $1$ $1$ $0$ $44$ <									
DecimalHex $32/59$ $0/31$ $2$ $3$ $4$ $2$ $30$ '1E'-0111110 $31$ '1F'-0111110 $32$ '20'-1000000 $33$ '21'-1000000 $34$ '22'-100001 $35$ '23'-100010 $36$ '24'-100010 $37$ '25:-100011 $39$ '27'-100111 $40$ '28'-100101 $41$ '29'-100101 $43$ '2B'-100110 $44$ '2C'-100111 $44$ '2C'-100111 $44$ '2E'-100111 $44$ '2C'-100111 $45$ '2D'-100111 $45$ '2D'-100111<							its	H Se	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Decimal	Hex	Sei	32/59	0/31	2	3	4	2
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	30	'1E'	-	0	1	1	1	1	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	31	'1F'	-	0	1	1	1	1	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	32	'20'	-	1	0	0	0	0	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	33	'21'	_	1	0	0	0	0	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$			_		0	0	0	0	
$\begin{array}{cccccccccccccccccccccccccccccccccccc$	35	'23'	-	1	0	0	0	0	1
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		'24'	-	1	0	0	0	1	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	37	'25:	-	1	0	0	0	1	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	38	'26'	-	1	0	0	0	1	1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	39	'27'	_	1	0	0	0	1	1
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	40	'28'	-	1	0	0	1	0	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	41	'29'	-	1	0	0	1	0	0
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	42	'2A'	_	1	0	0	1	0	1
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	43	'2B'		1	0	0	1	0	1
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	44	'2C'	-	1	0	Ó	1	1	0
$ \begin{array}{cccccccccccccccccccccccccccccccccccc$	45	'2D'	-	1	0	0	1	1	0
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	46	'2E'	<u> </u>	1	0	0	1	1	1
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	47	'2F'	_	1	0	0	1	1	1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	48	'30'	-	1	0	1	0	0	0
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	49	'31'	-	1	0	1	0	0	0
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	50	'32'	-	1	0	1	0	0	1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	51	'33'	-	1	0	1	0	0	1
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	52	'34'	-	1	0	1	0	1	0
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	53	'35'	-	1	0	1	0	1	0
56         '38'         -         1         0         1         1         0         0           57         '39'         -         1         0         1         1         0         0           58         '3A'         -         1         0         1         1         0         1			_		0		0		
57         '39'         -         1         0         1         1         0         0           58         '3A'         -         1         0         1         1         0         1	55	'37 <b>'</b>	-	1	0	1	0	1	1
58 '3A' - 1 0 1 1 0 1	56	'38'	-	1	0	1	1	0	0
	57	'39'	-	1	0	1	1	0	0
	58	'3A'	-	1	0	1	1	0	1
59  '3B' - 1 0 1 1 0 1	59	'3B'	-	1	0	1	1	0	1

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# HEAD SELECTION SCOPING PROCEDURE **R/W 344**



#### HEAD SELECTION SCOPING PROCEDURE **R/W 344**



# **READ DATA SIGNAL SCOPING PROCEDURE**

#### Purpose

The purpose of the Read Data Signal Scoping Procedure is to provide a method of scoping the HDA Read signal while looping a single track Read operation. The Read signal cannot be scoped directly. An amplifier that is not functional to machine operation is located on the Read Detector card to allow scoping of the Read signal.

Scoping the Read signal determines:

- If the amplitude of the Read signal from a suspected bad head is adequate.
- If the combined frequency response of the head and the disk surface of a suspected bad head or track is within tolerance.

#### **Track Format**

The track to be read must be formatted with the standard HA, R0 (Count and Data), and R1 (Count and Data). The R1 Count field must be written to reflect the R1 data length and the R1 Data field must be written with an alternating data pattern of 8 bytes of 'AA' and 8 bytes of 'FF'. This pattern must be repeated at least ten times.

Most microdiagnostics and OLTs that write on the CE cylinder leave the CE tracks formatted with the proper data pattern for this procedure. To format the CE cylinder, run microdiagnostic routine B0 in default mode (see MICRO 52). To format any track, including those used by the customer, use OLT T3350WT (see OLT 25) or FRIEND. When formatting customer tracks, be sure data is removed since it will be destroyed.

### Looping Instructions

A Read operation can be looped on a specific head using FRIEND or OLT T3350PSB, but microdiagnostic routine B1 is preferred (see MICRO 57, Scope Loop-Physical, for procedure).

#### Scope Setup (See Figure 1.)

Sweep	0.1 ms/div
Mode	ADD (with Ch 2 inverted)
Trigger	
Slope (+) A1H2(A1N2)J13 +Squelch A(B) Ch 1 A1J2(A1M2)B05	
Differential Read X T	TP A(B)
Volts/div Probe	10 to 20 mV (See Note.) x10 and grounded.
Ch 2 A1J2(A1M2)B07	
Differential Read Y T	<b>P</b> A(B)
Volts/div	10 to 20 mV (See Note.)
Probe	x10 and grounded.

#### Action

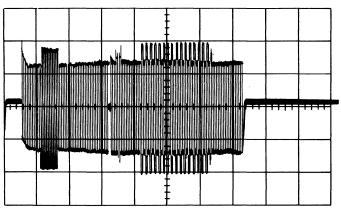
Use Figures 1 and 2 to obtain the scope picture shown in Figure 3.

#### Analysis

The frequency of the repetitive 'AA' pattern is 1/2 of the frequency of the repetitive 'FF' pattern. The amplitude of the 'FF' pattern is less than that of the 'AA' pattern. This difference in amplitude is due to the combined frequency response (head resolution) of the head and disk surface.

The peak-to-peak amplitude of the 'FF' pattern should not fall below 165 millivolts and must be equal to a minimum of 55% of the average peak-to-peak amplitude of the 'AA' pattern. This is determined by dividing the average peak-to-peak value of the 'FF' pattern by the average peak-to-peak value of the 'AA' pattern.

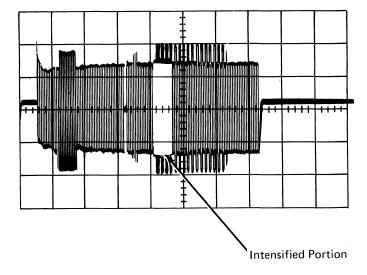
As shown in Figure 3, the average peak-to-peak value of the 'AA' pattern is about 4 divisions and the average peak-to-peak value of the 'FF' pattern is about 3 divisions (3/4=0.75). Head resolution is equal to 0.75 or 75%. The average peak-to-peak amplitude measurements should be made as close as possible to the nearest tenth of a division. Figure 1. Scope Setup.

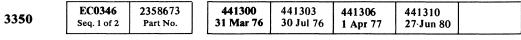


Scope picture may vary depending on the number of 'FF' and 'AA' patterns written.

Figure 2. Use the same scope setup as Figure 1 and change:

Delay Time -Delay Sweep = 5  $\mu$ s Horizontal Display = A Intensified during B Sweep Mode = B Starts After Delay Time Delay-Time Multiplier – adjust intensified portion to obtain scope picture as shown on Figure 2.

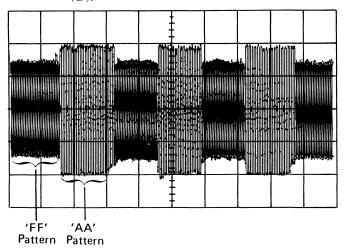




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**Figure 3**. Use the same scope setup as Figure 2 and change Horizontal Display to Delayed Sweep (B).



Note: Even-numbered movable physical heads and all fixed physical heads normally have about 1.5 times the peak-to-peak voltage amplitude of the odd numbered movable physical heads. This difference in peak-to-peak value is due to the even numbered physical heads and the fixed physical heads having been written with Hi I W (Hi Write Current).

READ DATA SIGNAL SCOPING PROCEDURE **R/W 346** 

# **READ DATA PATH SCOPING PROCEDURE**

#### Purpose

The purpose of the Read Data Path Scoping Procedure is to provide information to allow scoping of the read data path and associated control lines while looping a Read Home Address operation.

#### Microdiagnostic

Run microdiagnostic routine AF on the first failing drive (nearest the controller). If all the drives are failing, run microdiagnostic routine AF on Drive A of the A2 Module.

Loop test 1 and bypass errors:

1. Load routine AF

2. Enter 10,01,01,01,00

A Read Home Address operation is looped using physical head 1.

#### **Scope Setup**

10 μs/div
•
50 mV
×10
50 mV
×10

#### Action

 $\bigcirc$ 

1. The signal should be the same as shown in Figure 1.

2. Scope the same points differentially (ADD Mode and Ch 2 inverted). Compare signals to Figure 2.

The amplitude after the gap should be 1 V peak-to-peak ± 10%.

The portion of the signal that is before the gap is composed of Clock bits coming from the controller. The portion of the signal that is after the gap is composed of Clock and Data bits coming from the HDA.

Are the signals correct	for both Figures 1 and 2?
-------------------------	---------------------------

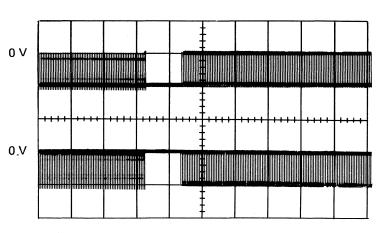
- Yes— Return to MAP and continue.
- No----- ► Scope test point A (of drive being tested) using the previous Scope Setup and Action Steps 1 and 2. The signals should be the same as shown in Figures 1 and 2.

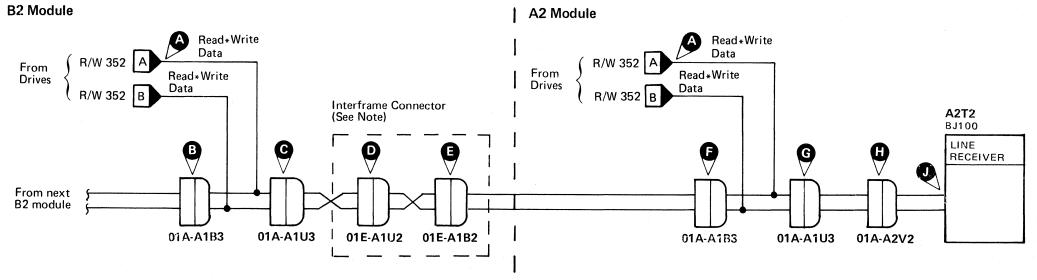
Are the signals correct?

- Yes— Use the diagram to isolate the problem.
- No----  $\triangleright$  Go to R/W 352 and continue with the Read Data Path Scoping Procedure.

#### Figure 1. Read Data

Mode = ALT





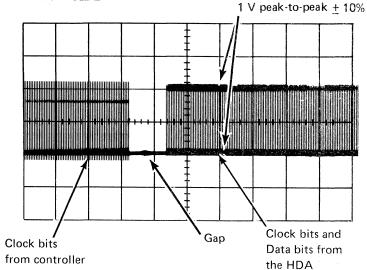
Test Point	A	B	G	D	G	G	G	0	0
+Read * Write Data	A1J2 (A1M2) D13	A1B3 B12	A1U3 B12	A1U2 D12	A1B2 B12	A1B3 B12	A1U3 B12	A2V2 B12	A2T2 D07
-Read • Write Data	A1J2 (A1M2) D12	A1B3 B13	A1U3 B13	A1U2 D13	A1B2 B13	A1B3 B13	A1U3 B13	A2V2 B13	A2T2 B05

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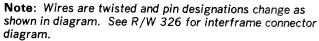
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# R/W 350



### Figure 2. Read Data Differentially

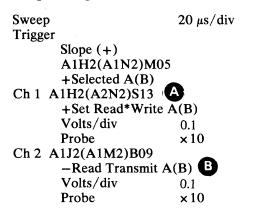
Mode = ADD



READ DATA PATH SCOPING PROCEDURE **R/W 350** 

# **READ DATA PATH SCOPING PROCEDURE**

#### **Scope Setup**



#### Action

The signal should be the same as shown in Figure 1.

Are the signals correct?

Yes --- > Go to the next sc

No----- ► Use the diagram of procedure on R/V

#### **Scope Setup**

Sweep	20 μs/div
Trigger	
Slope (+)	
A1H2(A1N2	)M05
+Selected A(	(B)
Ch 1 A1J2(A1M2)J	D5 🕑
- Squelch Ga	ate A(B)
Volts/div	0.1
Probe	×10

#### Action

The signals should be the same as shown in Figure 2.

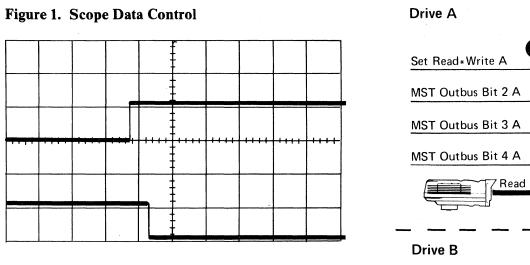
Are the signals correct?

- Yes— Use the diagram on this page and the procedure on R/W 350 to isolate the problem.
- No----- Use the diagram on this page and the procedure on R/W 360 to isolate the problem.

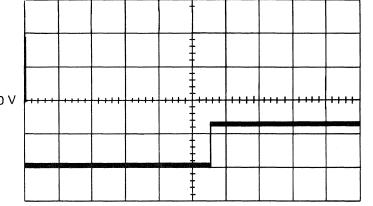
cope setup.						
on this page and the				-		
W 360 to isolate the problem.				-	ŀ	
w 500 to isolate the problem:	0.1/		 		ŧ	
	0 V	 	 			1
				-		
		 <u> </u>	 			
$20 \ \mu s/div$				-		

0 V

0 V



#### Figure 2. Scope Data Control



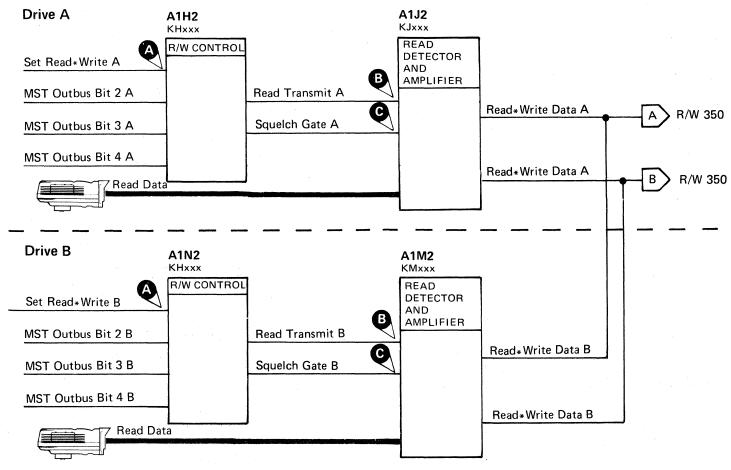


Chart Line No.	Line Name	ALD	Test Point	Test Point				
1	+Set Read*Write A(B)	KH140 (KN140)	A1H2 (A1N2) S13	A				
2	-MST Outbus Bit 2 A(B)	KH160 (KN160)	A1H2 (A1N2) P09					
3	-MST Outbus Bit 3 A(B)	KH160 (KN160)	A1H2 (A1N2) U09					
4	-MST Outbus Bit 4 A(B)	KH160 (KN160)	A1H2 (A1N2) P02					
5	—Read Transmit A(B)	KJ100 (KM100)	A1J2 (A1M2) B09	B				
6	-Squelch Gate A(B)	KJ100 (KM100)	A1J2 (A1M2) J05	C				
7	+Read*Write Data A(B)	KJ100 (KM100)	A1J2 (A1M2) D13					
8	–Read*Write Data A(B)	KJ100 (KM100)	A1J2 (A1M2) D12					

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## READ DATA PATH SCOPING PROCEDURE **R/W 352**

READ DATA PATH SCOPING PROCEDURE

**R/W 352** 

# **READ HOM E ADDRESS (Read G1 – Tag '0E' Bus '4E')**

The following is a description of a Read G1 operation as it is used in microdiagnostic routine AF, test 01:

See OPER 230 through 233 for a general description of a Read operation.

- 1. Before the Read G1 tag is executed, the CE drive is selected (Tag '83' Bus '10') and a Set Read/Write (Tag '85') is issued.
- 2. As soon as the drive is oriented on Index, the Gap Counter is reset and the microdiagnostic issues a Sync tag (Tag '0B') to aid in scoping. (Sync pulse will be available at the RAS test point.)
- 3. The microdiagnostic issues the Read G1 tag (Tag '0E' Bus ' $4\overline{E}$ '). The 'E' in Bus Out bits 4 through 7 is the modulo count (units position of the byte count). This indicates that 14 bytes are to be transferred.
- 4. At Count 64 time, the controller activates Read Gate to the drive.
- 5. At Count 76 time, the controller activates Unsquelch to the drive.
- 6. At Count 102 time, the Gap Counter is reset to zero.
- 7. At Count 1 time, the VFO is locked to data and put in Fast Sync mode.
- 8. At Count 8 time, VFO Fast Sync is reset and the hardware starts searching for a Sync Byte in SERDES ('19').
- 9. After the Sync Byte is detected, Data Good is activated. This indicates that the next byte entering SERDES is the data byte. If no Sync Byte is detected by Count 22 time, the G1 Retry latch (BG140) is set to allow for a possible skip defect. At Count 128 time, the Gap Counter is reset to zero. VFO is locked to data again and if a Sync Byte is not detected by Count 21 time, a Check End condition with a No Sync Byte Found indication results.

#### See OPER 232 for additional information on the Sync Byte.

- 10. Read Mode, Run ECC, and Run Modulo are activated and the Gap Counter is again reset to zero.
- 11. The Gap Counter is set to the inverted modulo count, which in this case is 1 (see number 3 above, for modulo count). The Sync Byte is placed on Bus In and Sync In is sent to the storage control.

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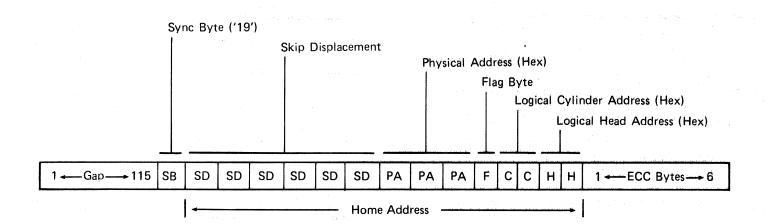
EC0352 2358674 441300 441303 3350 Seq. 2 of 2 Part No. 31 Mar 76 30 Jul 76

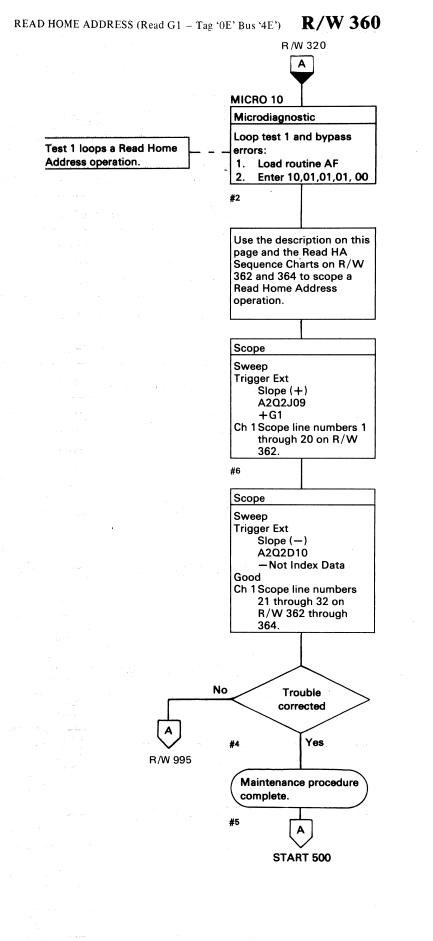
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 $\bigcirc$ 

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- 12. Sync Out is returned from the storage control.
- 13. Fourteen more Sync In and Sync Out cycles transfer the Home Address to the storage control. The data transfer is ended when the Gap Counter equals 15.
- 14. End Data and Transfer ECC are activated and Read Mode is de-activated.
- 15. The six ECC Bytes are transferred to the ECC Shift Register. If ECC Zeros Compare is active after the six ECC Bytes are transferred, ECC Data Check is blocked.
- 16. Op End is activated and Normal End is sent to the storage control. If ECC Data Check was not blocked (see number 15 above), Check End, Command Overrun (Bus In bit 0), and ECC Data Check (Bus In bit 3) are sent to the storage control instead.
- 17. End Response is returned from the storage control.
- 18. Reset End Condition is activated in the controller.





READ HOME ADDRESS (Read G1 – Tag '0E' Bus '4E') **R/W 360** 

 $\bigcirc$ 

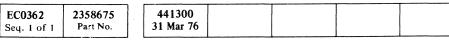
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# **READ HA SEQUENCE CHART**

GAP COUNTER VALUE

Chart									OP		SET RE	AD GATE	VEC	FAST	SYNC	DATA AND ECC DATA TRANSFER		END DATA OP
Line No.	Line Name	ALD	Test Point	15		28	64	67	76	102		8	15					
	-Ct 1	BG140	A2P2 J04						I									
2		BG120	A2P2 B09															
3		BH140	A2Q2 G09															
4		BH120	A2Q2 G07		181_25_3,													
.5		BH140	A2Q2 M08															
6	-Reset Ctr	BG100	A2P2 G09									<	>_					
7	-Phy Index	BA140	A2F2 G09			<								5				
8	-Index Alert	BH150	A2Q2 J11				ſ				n n a na sa							
9	– Read Gate	BH140	A2Q2 P09							5								
10	- Orientated	вн130	A2Q2 J06															
11	-RAS TP	BD100	A2L2 J11															
12	-Read Op 'OE'	BD100	A2L2 M02															
13	+G1	BH120	A2Q2 J09															
14	-Transfer Sector Count	BH120	A2Q2 J07															
15	– Unsquelch	BH140	A2Q2 M09															
16	+VFO to Data	BG140	A2P2 G04										>					
17	+ Servo Mode	BC140	A2S2 G10			<	>											
18	–VFO Fast Sync	BC140	A2S2 S09							2				\$				
19	+Reset Fast Sync	BG140	A2P2 G04							>								
20	– Not Index Data Good	BH160	A2Q2 D10						· · ·									
21	-Read Mode Control	BG150	A2P2 D03						ан 									
22	-Run ECC Control	BG170	A2P2 J02				ļ								L			
23	– Read Mode	BG170	A2P2 D05		•													

3350



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READ HA SEQUENCE CHART **R/W 362** 

•



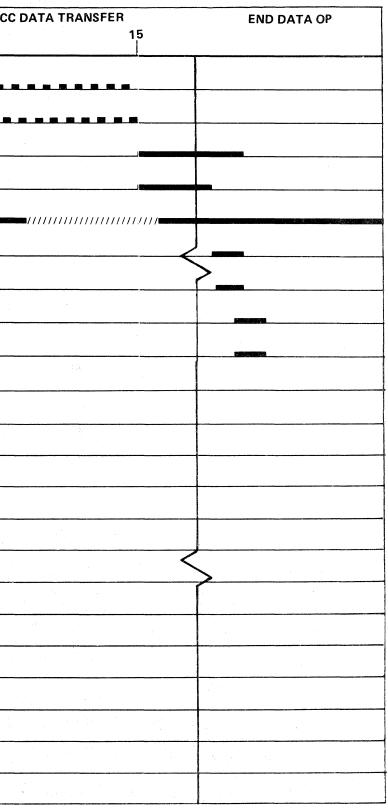
# **READ HA SEQUENCE CHART**

GAP COUNTER VALUE

Chart	! NI				READ OP		SET REA	DGATE	VFO	FAST	SYNC	DATA AND ECC
Line No.	Line Name	ALD	Test Point	15 	<b>28</b>	<b>64</b> 	67	76	102	1	8	
24	-Sync In	BC170	A2S2 S10									
25	+Sync Out	BC170	A2S2 S12									
26	+End Data	BG170	A2P2 G02									
27	-Xfer ECC Control	BG170	A2P2 J06									
28	–ECC Zeros Compare	BC150	A2S2 U06									
29	-Op End	BG170	A2P2 P04				and the second					
30	+Normal End NPL	BE160	A2K2 D11		<	$\leq$					J	
31	+End Response NPL	BF160	A1G2 S03			T I			2			>
32	+Reset End Condition	BF160	A2G2 G05					· · · ·	$\geq$			
										· ·		
								· · ·				
										S		
					· · · · · ·							
-						$\geq$	-					
						_					- -	
					· ·	_			$\leq$			
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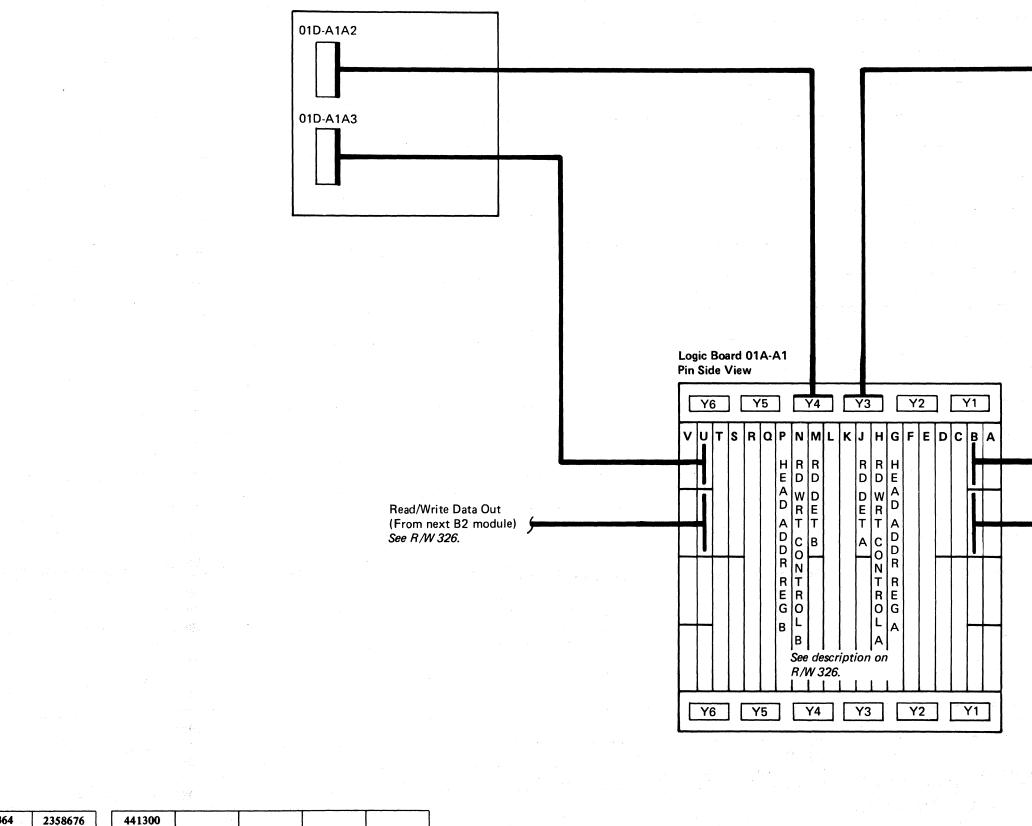
				 	 	•
3350	EC0364 Seq. 1 of 2	2358676 Part No.	441300 31 Mar 76			

READ HA SEQUENCE CHART R/W 364



# READ HA SEQUENCE CHART R/W 364

Drive B HDA (Rear View) Connectors

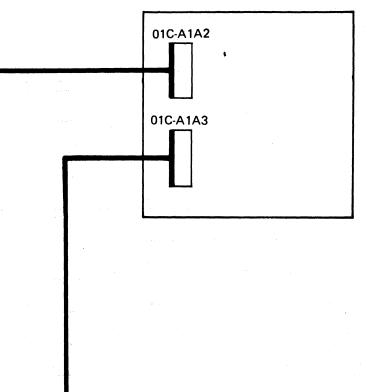


EC0364 3350 31 Mar 76 Seq. 2 of 2 Part No.

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#### READ DATA CABLE DIAGRAM **R/W 370**





Read/Write Data In (To controller) See R/W 326.

# READ DATA CABLE DIAGRAM **R/W 370**

# HDA CABLE CHECK PROCEDURE

#### Purpose

The purpose of this procedure is to check continuity of the HDA cable lines.

#### Procedure

- 1. Set the drive Start/Stop switch to the Stop position.
- 2. Turn the Drive DC Power switch to the Off position.
- 3. Remove the two cable connectors from the HDA, but do not remove the connectors from the A1 board: 01C (01D) A1A2 01C (01D) A1A3

#### See R/W 370 for the location.

4. Check continuity of cables using Figure 1 on this page and the cable diagram on R/W 370. Refer to the MAP page that was used to enter this procedure for an indication of the failing lines.

#### Action

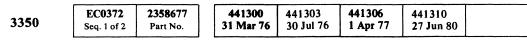
#### Are cables OK?

- Yes → Restore the HDA cables, turn the Drive DC Power switch to the On position, and return to the MAP page.
- No----► Repair or replace as required. Exit to START 500 when the trouble is corrected.

# 1 110 4 61 1 1 1

Line Name	ALD	Card	A1 Boar	d Connector	HDA Conn	
	ALD	Caru	Cable	Board	01C (01D)	
Movable Heads A(B) Data Y	KJ100 (KM100)	A1J2 (A1M2) G12	Y3B02 (Y4B02)	A1H1 A13 (A1L1 D13)	A1A2 B02	7
Movable Heads A(B) Data X	KJ100 (KM100)	A1J2 (A1M2) J12	Y3D02 (Y4D02)	A1H1 A11 (A1L1 D11)	A1A2 D02	
Gnd			Y3B03 (Y4B03	A1H1 B13 (A1L1 E13)	A1A2 B03	
Fixed Heads A(B) Data X	KG170 (KP170)		Y3D03 (Y4D03)	A1H1 B11 (A1L1 E11)	A1A2 D03	
Fixed Heads A(B) Data Y	KJ100 (KM100)	A1J2 (A1M2) G07	Y3B04 (Y4B04)	A1H1 C13 (A1M1 A13)	A1A2 B04	
Gnd			Y3D04 (Y4D04)	A1H1 C11 (A1M1 A11)	A1A2 D04	
-Fixed Heads 0-31 A(B)	KG170 (KP170)	A1G2 (A1P2) S10	Y3B05 (Y4B05)	A1H1 D13 (A1M1 B13)	A1A2 B05	
+6 V	KA100 (KV100)	A1E1 D11 (A1R1C11)		A1H1 D11 (A1M1 B11)	A1A2 D05	
-MARS HAR Bit 2 A(B)	KG170 (KP170)	A1G2 (A1P2) U11	Y3B06 (Y4B06)	A1H1 E13 (A1M1 C13)	A1A2 B06	
-Fixed Heads 32-59 A(B)	KG170 (KP170)	A1G2 (A1P2) S09	Y3D06 (Y4D06)	A1H1 E11 (A1M1 C11)	A1A2 D06	
Gnd			Y3B07 (Y4B07)	A1J1 A13 (A1M1 D13)	A1A2 B07	
-MARS HAR Bit 3 A(B)	KG170 (KP170)	A1G2 (A1P2) U12	Y3D07 (Y4D07)	A1J1 A11 (A1M1 D11)	A1A2 D07	HDA Connector
-MARS HAR Bit 4 A(B)	KG170 (KP170)	A1G2 (A1P2) U10	Y3B08 (Y4B08)	A1J1 B13 (A1M1 E13)	A1A2 B08	01C (01D) A1A2
Gnd			Y3D08 (Y4D08)	A1J1 B11 (A1M1 E11)	A1A2 D08	
+Fixed Heads HDA	KF110 (KQ110)	A1F2 (A1Q2) S03	Y3B09 (Y4B09)	A1J1 C13 (A1N1 A13)	A1A2 B09	
+MARS Unsafe Current A(B)	KG210 (KP210)	A1G2 (A1P2) G08	Y3D09 (Y4D09)	A1J1 C11 (A1N1 A11)	A1A2 D09	
-Chip Select 6 A(B)	KG170 (KP170)	A1G2 (A1P2) P03	Y3B10 (Y4B10)	A1J1 D13 (A1N1 B13)	A1A2 B10	
-Chip Select 7 A(B)	KG170 (KP170)	A1G2 (A1P2) M05	Y3D10 (Y4D10)	A1J1 D11 (A1N1 B11)	A1A2 D10	
Gnd			Y3B11 (Y4B11)	A1J1 E13 (A1N1 C13)	A1A2 B11	
-Chip Select 5 A(B)	KG170 (KP170)	A1G2 (A1P2) M02	Y3D11 (Y4D11)	A1J1 E11 (A1N1 C11)	A1A2 D11	
-Chip Select 4 A(B)	KG170 (KP170)	A1G2 (A1P2) M04	Y3B12 (Y4B12)	A1K1 A13 (A1N1 D13)	A1A2 B12	
Gnd			Y3D12 (Y4D12)	A1K1 A11 (A1N1 D11)	A1A2 D12	
-Chip Select 2 A(B)	KG170 (KP170)	A1G2 (A1P2) M03	Y3B13 (Y4B13)	A1K1 B13 (A1N1 E13)	A1A2 B13	
-Chip Select 3 A(B)	KG170 (KP170)	A1G2 (A1P2) P04	Y3D13 (Y4D13)	A1K1 B11 (A1N1 E11)	A1A2 D13	J
-Chip Select 1 A(B)	KG170 (KP170)	A1G2 (A1P2) P02	A1B2 (A1U2) B02		A1A3 B02	)
Chip Select 0 A(B)	KG170 (KP170)		A1B2 (A1U2) D02		A1A3 D02	
Write Current A(B) HDA	KJ100 (KM100)	A1J2 (A1M2) J06	A1B2 (A1U2) B03*	A1B2 (A1U2) D03*	A1A3 B03	
Write Current A(B) HDA	KJ100 (KM100)	A1J2 (A1M2) J06	A1B2 (A1U2) D03*	A1B2 (A1U2) B03*	A1A3 D03	
+MARS Unsafe Current A(B)	KG210 (KP210)	A1G2 (A1P2) G08	A1B2 (A1U2) B04		A1A3 B04	
+Write Select Fixed HDA	KG200 (KP200)	A1G2 (A1P2) U09	A1B2 (A1U2) D04		A1A3 D04	
-4 V	KA100 (KV100)	A1A2 (A1U2) C06	A1B2 (A1U2) B05		A1A3 B05	
-4 V	KA100 (KV100)		A1B2 (A1U2) D05		A1A3 D05	
-4 V	KA100 (KV100)		A1B2 (A1U2) B06		A1A3 B06	
-4 V	KA100 (KV100)	A1B2 (A1V2) C06	A1B2 (A1U2) D06		A1A3 D06	
-4 V	KA100 (KV100)	A1A2 (A1U2) C06	A1B2 (A1U2) B07		A1A3 B07	
+6 V to MARS Module A(B)	KG210 (KP210)		A1B2 (A1U2) D07		A1A3 D07	HDA Connector
–Head Sel 2 A(B)	KG170 (KP170)	A1G2 (A1P2) D07	A1B2 (A1U2) B08		A1A3 B08	01C (01D) A1A3
Gnd			A1B2 (A1U2) D08		A1A3 D08	
+ Write Select Movable HDA	KG200 (KP200)		A1B2 (A1U2) B09		A1A3 B09	
-Head Sel 1 A(B)	KG170 (KP170)	A1G2 (A1P2) D10	A1B2 (A1U2) D09		A1A3 D09	
Spare			A1B2 (A1U2) B10		A1A3 B10	
+6 V to MARS Modules HDA	KG210 (KP210)		A1B2 (A1U2) D10		A1A3 D10	
Servo Ground	KA100 (KV100)		A1B2 (A1U2) B11*	A1B2 (A1U2) D11*	A1A3 B11	
Servo Ground	KA100 (KV100)		A1B2 (A1U2) D11*	A1B2 (A1U2) B11*	A1A3 D11	
Raw Servo Signal 1 A(B)	KC100 (KT100)		A1B2 (A1U2) B12		A1A3 B12	
Raw Servo Signal 2 A(B)	KC100 (KT100)		A1B2 (A1U2) D12		A1A3 D12	
-8.3 V A(B)	KC100 (KT100)		A1B2 (A1U2) B13*	A1B2 (A1U2) D13*	A1A3 B13	
-8.3 V A(B)	KC100 (KT100)	A1C2 (A1T2) B02	A1B2 (A1U2) D13*	A1B2 (A1U2) B13*	A1A3 D13	

\* The pin in the B row is connected to the same pin on the D row on the pin side of the A1 Board.





HDA CABLE CHECK PROCEDURE **R/W 372** 

# **HDA VOLTAGE CHECK PROCEDURE**

#### Purpose

The purpose of this procedure is to check voltages at the HDA connectors. The voltages should have previously been checked at the A1 logic board. If not, check the voltages using Figure 1 on R/W 312 before continuing.

#### **Test Equipment Required**

**Digital Voltmeter** 

Scope

#### Procedure

- 1. Set the drive Start/Stop switch to the Stop position.
- 2. Turn the drive DC Power switch to the Off position.
- 3. Remove the two cable connectors from the HDA:

01C (01D) A1A2 01C (01D) A1A3

See R/W 370 for the location.

- 4. Turn the drive DC Power switch to the On position.
- 5. Check voltages and ripple at cable end using Figure 1. See Figure 2.

#### Action

Are the voltages and ripple correct?

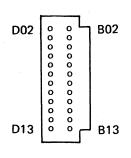
- Yes --- > Turn the drive DC Power switch to the Off position, restore the HDA cables, restore the power, and return to the MAP page.
- No---- ► The problem is in the HDA cables or the A1 logic board land pattern. See R/W 372 for voltage source. Repair or replace as required. Exit to START 500 when the trouble is corrected.

Figure 1. HDA Voltage Level

Voltage	Test Point 01C(01D)	Tolerance	Maximum AC Ripple
-4 V	A1A3 B05	−3.85 to − 4.50 V*	0.23 V p-p
-4 V	A1A3 D05	1	
-4 V	A1A3 B06		
-4 V	A1A3 D06		
-4 V	A1A3 B07		
+6 V	A1A3 D07	- +5.76 V to +6.24 V*	0.08 V p-p
+6 V	A1A3 D10		0.00
+6 V	A1A2 D05		

\* All voltages are referenced to ground at 01C (01D) A1A2D08 or 01C (01D) A1A3D08.

Figure 2. Cable End View Pin Locations



3350	EC0372 Seq. 2 of 2	2358677 Part No.	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77	441310 27 Jun 80	
		1					

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HDA VOLTAGE CHECK PROCEDURE **R/W 376** 

Correct any problems found, reinstall the ground wire

and HDA cable, then return to the MAP page.

# **BASE PLATE GROUND CHECK PROCEDURE**

#### Purpose

#### Action

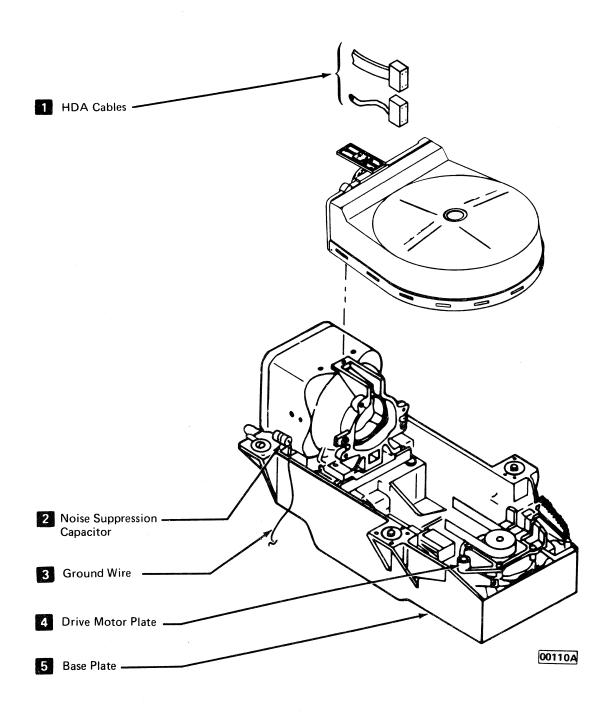
The purpose of this procedure is to check base plate grounding and base plate isolation from the frame and motor plate.

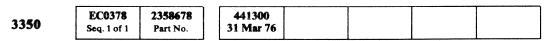
#### **Tools Required**

CE Meter.

#### Procedure

- 1. Set the DC Power switch to the Off position.
- 2. Remove the two cables from the HDA:
  01C (01D) A1A2 
  01C (01D) A1A3 
  See R/W 370 for the location.
- 3. Check for continuity from the base plate 5 to the frame. The base plate is grounded to the frame through a wire 3 attached to the left rear of the base plate mounting pad.
- 4. Remove the base plate ground wire and check for continuity again. The base plate should be isolated from the frame (minimum resistance is 2 Megohm). If the base plate is not isolated from the frame, the most probable cause is a short through the motor plate The motor plate and motor case should be isolated from the base plate when the HDA cables and the base plate ground wire are removed.
- 5. Check for continuity from the motor plate to the frame. The motor plate should be grounded to the frame through the motor cable and plug.
- 6. Check the noise suppression capacitor 22 for a shorted or open condition. To check the capacitor, do the following:
  - a. Momentarily short the capacitor lead to the capacitor case.
  - b. Set the CE Meter to RX 1000 and hold one meter lead on the capacitor lead and touch the other meter lead to the capacitor case. The meter should deflect very slightly, then return to 0.
  - c. Quickly reverse the meter leads to the capacitor. The meter should deflect almost twice as far as it did in Step b, then return to 0.





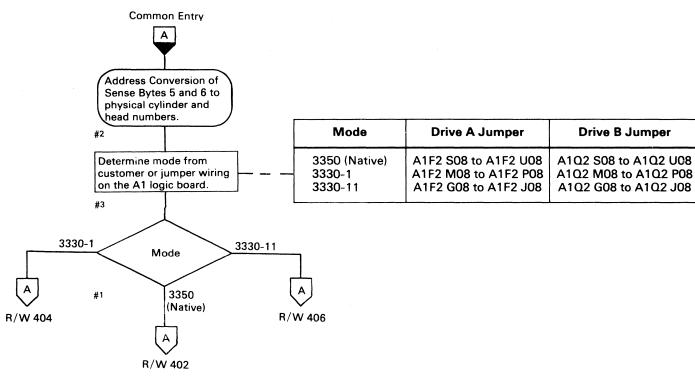
#### BASE PLATE GROUND CHECK PROCEDURE **R/W 378**

#### BASE PLATE GROUND CHECK PROCEDURE

**R/W 378** 



# **ADDRESS CONVERSION**



3350	EC0400 Seq. 1 of 1	2358679 Part No.	441300 31 Mar 76		

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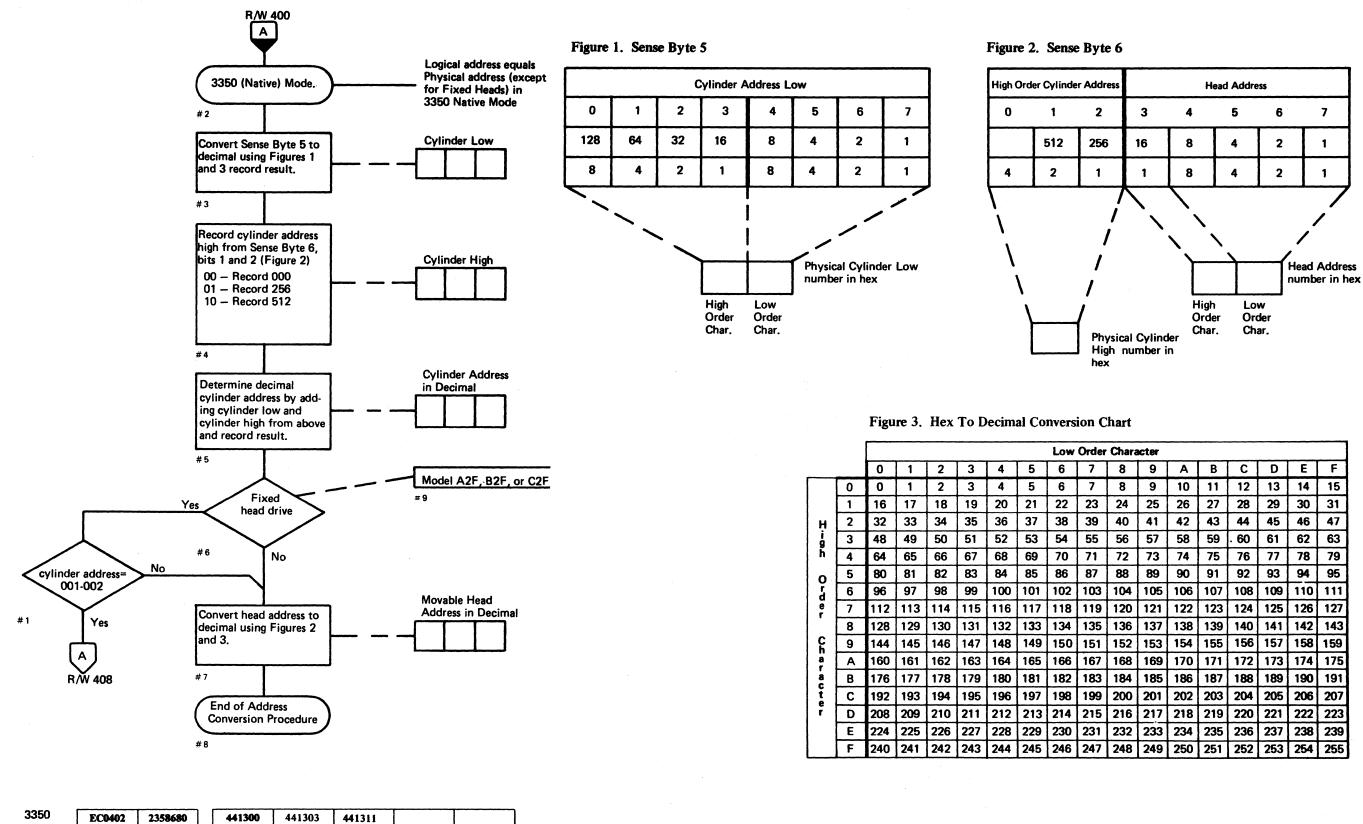


# ADDRESS CONVERSION **R/W 400**

# ADDRESS CONVERSION **R/W 400**



## ADDRESS CONVERSION – 3350 (Native) Mode



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Part No.

31 Mar 76

30 Jul 76

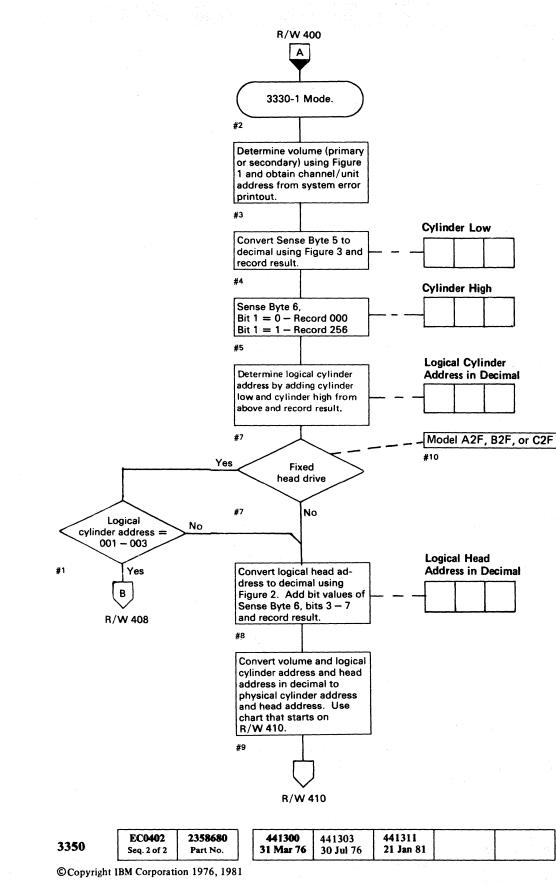
21 Jan 81

**R/W 402** 

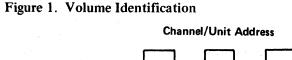


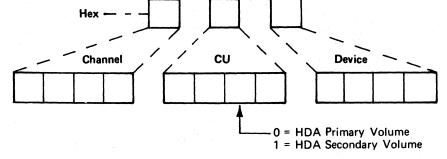
Chara	cter						
8	9	Α	В	С	D	Ε	F
8	9	10	11	12	13	14	15
24	25	26	27	28	29	30	31
40	41	42	43	44	45	46	47
56	57	58	59	· 60	61	62	63
72	73	74	75	76	77	78	79
88	89	90	91	92	93	94	95
104	105	106	107	108	109	110	111
120	121	122	123	124	125	126	127
136	137	138	139	140	141	142	143
152	153	154	155	156	157	158	159
168	169	170	171	172	173	174	175
184	185	186	187	188	189	190	191
200	201	202	203	204	205	206	207
216	217	218	219	220	221	222	223
232	233	234 235		236	237	238	239
248	249	250	251	252	253	254	255

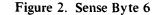
### **ADDRESS CONVERSION – 3330-1 MODE**



)







High Logic Addr	Order al Cyl	inder	L	ogical	Head	Addre	255
0	1	2	3	4	5	6	7
	Cyl 256		16	8	4	2	1

#### Figure 3. Hex To Decimal Conversion Chart

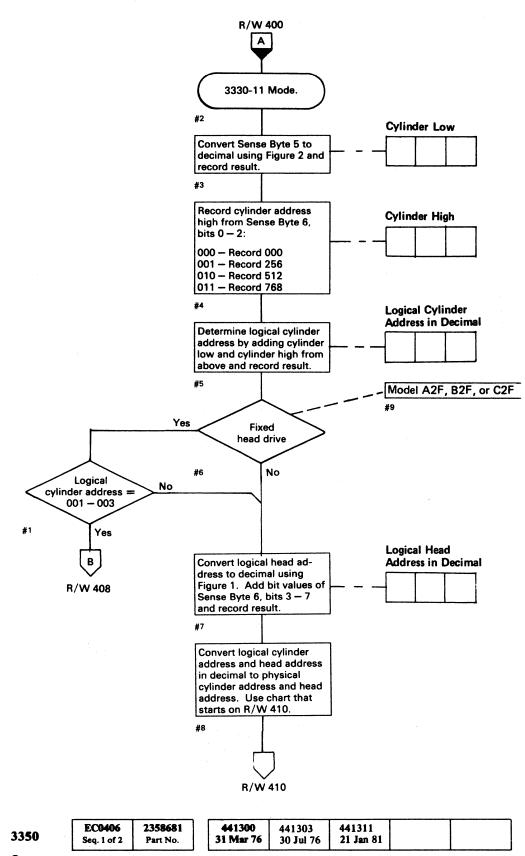
								Low	Order	Chara	cter						
		0	1	2	3	4	5	6	7	8	9	А	В	С	D	Е	F
,	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
н	2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
i 9 h	3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
ĥ	4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
0	5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
r	6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
e	7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
	8	128	129	130	131	132	1 <b>3</b> 3	134	135	136	137	138	139	140	141	142	143
C h	9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
a	Α	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
ac	В	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
t	С	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
ř	D	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
	Е	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
	F	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

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ADDRESS CONVERSION - 3330-1 MODE R/W 404

ADDRESS CONVERSION - 3330-1 MODE **R/W 404** 

# **ADDRESS CONVERSION – 3330-11 MODE**



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#### Figure 1. Sense Byte 6

	Order al Cyl		L	ogical	Head	Addre	255
0	1 -	2	3	4	5	6	7
	512	256	16	8	4	2	1

#### Figure 2. Hex To Decimal Conversion Chart

							,	Low	Order	Chara	cter						
		0	1	2	3	4	5	6	7	8	9	Α	В	С	D	E	F
	0	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
	1	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
H	2	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47
i g	3	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
h	4	64	65	66	67	68	69	70	71	72	73	74	75	76	77	78	79
0	5	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95
rd	6	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111
e r	7	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127
	8	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143
C h	9	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159
ar	А	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175
a C	В	176	177	178	179	180	181	182	183	184	185	186	187	188	189	190	191
t	С	192	193	194	195	196	197	198	199	200	201	202	203	204	205	206	207
ř	D	208	209	210	211	212	213	214	215	216	217	218	219	220	221	222	223
	Е	224	225	226	227	228	229	230	231	232	233	234	235	236	237	238	239
	F	240	241	242	243	244	245	246	247	248	249	250	251	252	253	254	255

ADDRESS CONVERSION - 3330-11 MODE **R/W 406** 

AD	DRES	S CON	VER	SION	- 333	0-11

1 MODE **R/W 406** 

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## ADDRESS CONVERSION (Fixed Head)

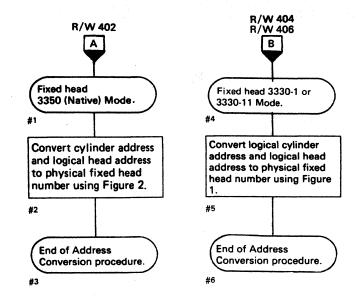


Figure 1. Logical Cylinder Address and Logical Head Address to Physical Fixed Head Number in Decimal

Logical Cylinder						-	1	.ogica	l Head	d Add	ress In	Deci	mal						
Address in Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
001	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
002	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
003	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56

Note: Heads 57, 58, and 59 are not used.

Figure 2. Cylinder Address and Logical Head Address to Physical Fixed Head Number in Decimal

Cylinder Add	7655									i. N		· .			Logica	al Hea	d Add	ress I	n Dec	imal	
in Decimal		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
001		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	
002		30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	

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#### ADDRESS CONVERSION (Fixed Head)

**R/W 408** 

21 22 27 28 21 22 24 25 26 51 52 

ADDRESS CONVERSION (Fixed Head) R/W 408

# **ADDRESS CONVERSION**

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	1.0	GICAL ADI	DRESS	PHYSI	CAL CYLIN	DER and HEAD		LC
	3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals		3330-1 Log Cyl Vol 1 *
	0 1 2	0 1 2	00-18 00-09 10-18 00-18	0 0 1 1	000 000 001 001	Log Hd Log Hd +20 Log Hd +10		36 37 38
	3	3	00-18 00-18		002	Log Hd		39
	4 5	3 4 5	00-09 10-18 00-18	2 2 3 3	002 003 003	Log Hd Log Hd +20 Log Hd +10		40 41
	6 7	6 7	00-18	4	004	Log Hd Log Hd		41 42 43
	, 8	8	00-09 10-18 00-18	4 5 5	004 005 005	Log Hd +20 Log Hd +10 Log Hd		43 44
	9 10	9 10	00-18 00-09 10-18	6 6 7	006 006 007	Log Hd Log Hd +20 Log Hd +10		45 46
	11	11	00-18	7	007	Log Hd		47
	12 13	12 13	00-18 00-09 10-18	8 8 9	008 008 009	Log Hd Log Hd +20 Log Hd +10		48 49
	14	14	00-18	9	009	Log Hd		50
	15 16	15 1,6	00-18 00-09 10-18	10 10 11	00A 00A 00B	Log Hd Log Hd +20 Log Hd +10		51 52
	17	17	00-18	11	00B	Log Hd		53
	18 19	18 19	00-18 00-09 10-18	12 12 13	00C 00C 00D	Log Hd Log Hd +20 Log Hd +10		54 55
	20	20	00-18	13	00D	Log Hd		56
	21 22	21 22	00-18 00-09 10-18	14 14 15	00E 00E 00F	Log Hd Log Hd +20 Log Hd +10		57 58
	23	23	00-18	15	00F	Log Hd		59
	24 25	24 25	00-18 00-09 10-18	16 16 17	010 010 011	Log Hd Log Hd +20 Log Hd +10		60 61
	26	26	00-18	17	011	Log Hd		62
	27 28	27 28	00-18 00-09 10-18	18 18 19	012 012 013	Log Hd Log Hd +20 Log Hd +10		63 64
	29	29	00-18	19	013	Log Hd		65
	30 31	30 31	00-18 00-09 10-18	20 20 21	014 014 015	Log Hd Log Hd +20 Log Hd +10		66 67
1	32	32	00-18	21	015	Log Hd		68
	33 34	33 34	00-18 00-09 10-18	22 22 23	016 016 017	Log Hd Log Hd +20 Log Hd +10		69 70
	35	35	00-18	23	017	Log Hd		71
							-	

LC	GICAL ADD	DRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
36 37 38	36 37 38	00-18 00-09 10-18 00-18	24 24 25 25	018 018 019 019	Log Hd Log Hd +20 Log Hd +10 Log Hd
39 40	39 40	00-18 00-09 10-18	26 26 27	01A 01A 01B	Log Hd Log Hd +20 Log Hd +10
41	41	00-18	27	01B	Log Hd
42 43 44	42 43 44	00-18 00-09 10-18 00-18	28 28 29 29	01C 01C 01D 01D	Log Hd Log Hd +20 Log Hd +10 Log Hd
45 46	45 46	00-18 00-09 10-18	30 30 31	01E 01E 01F	Log Hd Log Hd +20 Log Hd +10
47	47	00-18	31	01F	Log Hd
48 49 50	48 49 50	00-18 00-09 10-18 00-18	32 32 33 33	020 020 021 021	Log Hd Log Hd +20 Log Hd +10 Log Hd
51 52	51 52	00-18 00-09	34 34	022 022	Log Hd Log Hd +20
53	53	10-18 00-18	35 35	023 023	Log Hd +10 Log Hd
54 55	54 55	00-18 00-09 10-18	36 36 37	024 024 025	Log Hd Log Hd +20 Log Hd +10
56	56	00-18	37	025	Log Hd
57 58	57 58	00-18 00-09 10-18	38 38 39	026 026 027	Log Hd Log Hd +20 Log Hd +10
59 60	59	00-18	39	027	Log Hd
60 61 62	60 61 62	00-18 00-09 10-18 00-18	40 40 41 41	028 028 029 029	Log Hd Log Hd +20 Log Hd +10 Log Hd
63 64	63 64	00-18 00-09	42 42	02A 02A	Log Hd Log Hd +20
65	65	10-18 00-18	43 43	02B 02B	Log Hd +10 Log Hd
66 67	66 67	00-18 00-09 10-18	44 44 45	02C 02C 02D	Log Hd Log Hd +20 Log Hd +10
68 60	68	00-18	45	02D	Log Hd
69 70 71	69 70 71	00-18 00-09 10-18 00-18	46 46 47 47	02E 02E 02F 02F	Log Hd Log Hd +20 Log Hd +10 Log Hd
		- 10 - 10	- <b>T</b> /	<u>V</u> 21	LUYIIU

LC	GICAL ADD	ORESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
72 73 74	72 73 74	00-18 00-09 10-18 00-18	48 48 49 49	030 030 031 031	Log Hd Log Hd +20 Log Hd +10 Log Hd
75 76 . 77	75 76 77	00-18 00-09 10-18 00-18	50 50 51 51	032 032 033 033	Log Hd Log Hd +20 Log Hd +10
78 79 80	78 79 80	00-18 00-09 10-18 00-18	51 52 53 53	033 034 034 035 035	Log Hd Log Hd Log Hd +20 Log Hd +10
81 82	81 82	00-18 00-09 10-18	54 54 55	036 036 037	Log Hd Log Hd Log Hd +20 Log Hd +10
83 84 85	83 84 85	00-18 00-18 00-09 10-18	55 56 57	037 038 038 039	Log Hd Log Hd Log Hd +20 Log Hd +10
86 87 88	86 87 88	00-18 00-18 00-09 10-18	57 58 58 59	039 03A 03A 03B	Log Hd Log Hd Log Hd +20 Log Hd +10
89 90 91	89 90 91	00-18 00-18 00-09 10-18	59 60 60 61	03B 03C 03C 03D	Log Hd Log Hd Log Hd +20 Log Hd +10
92 93 94	92 93 94	00-18 00-18 00-09 10-18	61 62 63	03D 03E 03E 03F	Log Hd Log Hd Log Hd +20 Log Hd +10
95 96 97	95 96 97	00-18 00-18 00-09 10-18	63 64 64 65	03F 040 040 041	Log Hd Log Hd Log Hd +20 Log Hd +10
98 99	98 99	00-18 00-18	65 66	041 042	Log Hd Log Hd
100 101	100 101	00-09 10-18 00-18	66 67 67	042 043 043	Log Hd +20 Log Hd +10 Log Hd
102 103 104	102 103 104	00-18 00-09 10-18 00-18	68 68 69 69	044 044 045 045	Log Hd Log Hd +20 Log Hd +10 Log Hd
105 105 106	105 106	00-18 00-09 10-18	70 70 71	046 046 047	Log Hd Log Hd +20 Log Hd +10
107	107	00-18	71	047	Log Hd

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# ADDRESS CONVERSION **R/W 410**

L	GICAL ADD	IRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
108 109 110	108 109 110	00-18 00-09 10-18 00-18	72 72 73 73	048 048 049 049	Log Hd Log Hd +20 Log Hd +10 Log Hd
111 112	111 112	00-18 00-09 10-18	74 74 75	04A 04A 04B	Log Hd Log Hd +20 Log Hd +10
113 114 115	113 114 115	00-18 00-18 00-09 10-18	75 76 76 77	04B 04C 04C 04D	Log Hd Log Hd Log Hd +20 Log Hd +10
116 117 118	116 117 118	00-18 00-18 00-09 10-18	77 78 78 79	04D 04E 04E 04F	Log Hd Log Hd Log Hd +20 Log Hd +10
119 120 121	119 120 121	00-18 00-18 00-09 10-18	79 80 80 81	04F 050 050 051	Log Hd Log Hd Log Hd +20 Log Hd +10
122 123 124	122 123 124	00-18 00-18 00-09 10-18	81 82 82 83	051 052 052 053	Log Hd Log Hd Log Hd +20 Log Hd +10
125 126 127	125 126 127	00-18 00-18 00-09	83 84 84	053 054 054	Log Hd Log Hd Log Hd +20
128 129	128 129	10-18 00-18 00-18	85 85 86	055 055 056	Log Hd +10 Log Hd Log Hd
130 131 132	130 131 132	00-09 10-18 00-18 00-18	86 87 87 88	056 057 057 058	Log Hd +20 Log Hd +10 Log Hd Log Hd
133 134	133 134	00-18 00-09 10-18 00-18	88 89 89	058 058 059 059	Log Hd +20 Log Hd +10 Log Hd
135 136 137	135 136 137	00-18 00-09 10-18 00-18	90 90 91 91	05A 05A 05B 05B	Log Hd Log Hd +20 Log Hd +10 Log Hd
138 139 140	138 139 140	00-18 00-09 10-18 00-18	92 92 93 93	05C 05C 05D 05D	Log Hd Log Hd +20 Log Hd +10 Log Hd
141 142 143	141 142 143	00-18 00-09 10-18 00-18	94 94 95 95	05E 05E 05F 05F	Log Hd Log Hd +20 Log Hd +10 Log Hd

Continued on R/W 411.

# **ADDRESS CONVERSION**

L	GICAL ADD	DRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
144 145 146	144 145 146	00-18 00-09 10-18 00-18	96 96 97 97	060 060 061 061	Log Hd Log Hd +20 Log Hd +10 Log Hd
147 148 149	147 148 149	00-18 00-09 10-18 00-18	98 98 99 99	062 062 063 063	Log Hd Log Hd +20 Log Hd +10 Log Hd
150 151 152	150 151 152	00-18 00-09 10-18 00-18	100 100 101 101	064 064 065 065	Log Hd Log Hd +20 Log Hd +10 Log Hd
153 154 155	153 154 155	00-18 00-09 10-18 00-18	102 102 103 103	066 066 067 067	Log Hd Log Hd +20 Log Hd +10 Log Hd
156 157 158	156 157 158	00-18 00-09 10-18 00-18	104 104 105 105	068 068 069 069	Log Hd Log Hd +20 Log Hd +10 Log Hd
159 160 161	159 160 161	00-18 00-09 10-18 00-18	106 106 107 107	06A 06A 06B 06B	Log Hd Log Hd +20 Log Hd +10 Log Hd
162 163 164	162 163 164	00-18 00-09 10-18 00-18	108 108 109 109	06C 06C 06D 06D	Log Hd Log Hd +20 Log Hd +10 Log Hd
165 166 167	165 166 167	00-18 00-09 10-18 00-18	110 110 111 111	06E 06E 06F 06F	Log Hd Log Hd +20 Log Hd +10 Log Hd
168 169 170	168 169 170	00-18 00-09 10-18 00-18	112 112 113 113	070 070 071 071	Log Hd Log Hd +20 Log Hd +10 Log Hd
171 172 173	171 172 173	00-18 00-09 10-18 00-18	114 114 115 115	072 072 073 073	Log Hd Log Hd +20 Log Hd +10 Log Hd
174 175 176	174 175 176	00-18 00-09 10-18 00-18	116 116 117 117	074 074 075 075	Log Hd Log Hd +20 Log Hd +10 Log Hd
177 178 179	177 178 179	00-18 00-09 10-18 00-18	118 118 119 119	076 076 077 077	Log Hd Log Hd +20 Log Hd +10 Log Hd

	LOG	ICAL ADD	ORESS	PHYSI	CAL CYLIN	DER and HEAD
3330 Log C Vol 1	yl	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
180 181 182	1	180 181 182	00-18 00-09 10-18 00-18	120 120 121 121	078 078 079 079	Log Hd Log Hd +20 Log Hd +10 Log Hd
18: 184	1	183 184	00-18 00-09 10-18	122 122 123	07A 07A 07B	Log Hd Log Hd +20 Log Hd +10
185 186 187	5	185 186 187	00-18 00-18 00-09 10-18	123 124 124 125	07B 07C 07C 07D	Log Hd Log Hd Log Hd +20 Log Hd +10
18	-	188	00-18	125	07D	Log Hd
189 190 19	0	189 190 191	00-18 00-09 10-18 00-18	126 126 127 127	07E 07E 07F 07F	Log Hd Log Hd +20 Log Hd +10
19 192 193	2	192 193	00-18 00-18 00-09 10-18	127 128 128 129	080 080 081	Log Hd Log Hd Log Hd +20 Log Hd +10
194		194	00-18	129	081	Log Hd
199 190 191	5	195 196 197	00-18 00-09 10-18 00-18	130 130 131 131	082 082 083 083	Log Hd Log Hd +20 Log Hd +10 Log Hd
198 199	9	198 199	00-18 00-09 10-18	132 132 133	084 084 085	Log Hd Log Hd +20 Log Hd +10
200 201 202	1	200 201 202	00-18 00-18 00-09	133 134 134	085 086 086	Log Hd Log Hd Log Hd +20
203		203	10-18 00-18	135 135	087 087	Log Hd +10 Log Hd
204 205	5	204 205	00-18 00-09 10-18	136 136 137	088 088 089	Log Hd Log Hd +20 Log Hd +10
200		206 207	00-18	137 138	089 08A	Log Hd Log Hd
208 209		208 209	00-09 10-18 00-18	138 139 139	08A 08B 08B	Log Hd +20 Log Hd +10 Log Hd
210 217		210 211	00-18 00-09 10-18	140 140 141	08C 08C 08D	Log Hd Log Hd +20 Log Hd +10
212		212	00-18	141 142	08D	Log Hd
213 214 215	1	213 214 215	00-18 00-09 10-18 00-18	142 142 143 143	08E 08E 08F 08F	Log Hd Log Hd +20 Log Hd +10 Log Hd

L	GICAL AD	DRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
216	216	00-18 00-09	144 144	090 090	Log Hd Log Hd +20
217 218	217 218	10-18 00-18	145 145	091 091	Log Hd +10 Log Hd
219 220 221	219 220 221	00-18 00-09 10-18 00-18	146 146 147 147	092 092 093 093	Log Hd Log Hd +20 Log Hd +10 Log Hd
222 222 223	222 223	00-18 00-09 10-18	148 148 149	094 094 095	Log Hd Log Hd Log Hd +20 Log Hd +10
224	224	00-18	149	095	Log Hd
225 226 227	225 226 227	00-18 00-09 10-18 00-18	150 150 151 151	096 096 097	Log Hd Log Hd +20 Log Hd +10
228	228	00-18	152	097 098	Log Hd Log Hd
229 230	229 230	00-09 10-18 00-18	152 153 153	098 099 099	Log Hd +20 Log Hd +10 Log Hd
231 232	231 232	00-18 00-09 10-18	154 154 155	09A 09A 09B	Log Hd Log Hd +20 Log Hd +10
233 234 235	233 234 235	00-18 00-18 00-09	155 156 156	09B 09C 09C	Log Hd Log Hd Log Hd +20
236	236	10-18 00-18	157 157	09D 09D	Log Hd +10 Log Hd
237 238 230	237 238	00-18 00-09 10-18 00-18	158 158 159	09E 09E 09F	Log Hd Log Hd +20 Log Hd +10
239 240 241	239 240 241	00-18 00-18 00-09 10-18	159 160 160 161	09F 0A0 0A0 0A1	Log Hd Log Hd Log Hd +20
242	242	00-18	161	0A1	Log Hd +10 Log Hd
243 244 245	243 244 245	00-18 00-09 10-18 00-18	162 162 163	0A2 0A2 0A3	Log Hd Log Hd +20 Log Hd +10
245 246 247	245 246 247	00-18 00-18 00-09 10-18	163 164 164 165	0A3 0A4 0A4 0A5	Log Hd Log Hd Log Hd +20
248	248	00-18	165	0A5 0A5	Log Hd +10 Log Hd
249 250	249 250	00-18 00-09 10-18	166 166 167	0A6 0A6 0A7	Log Hd Log Hd +20 Log Hd +10
251	251	00-18	167	0A7	Log Hd

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# ADDRESS CONVERSION **R/W 411**

L	GICAL AD	DRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
252 253 254	252 253 254	00-18 00-09 10-18 00-18	168 168 169 169	0A8 0A8 0A9 0A9	Log Hd Log Hd +20 Log Hd +10 Log Hd
255 256 257	255 256 257	00-18 00-09 10-18 00-18	170 170 171 171	0AA 0AA 0AB 0AB	Log Hd Log Hd +20 Log Hd +10 Log Hd
258 259 260	258 259 260	00-18 00-09 10-18 00-18	172 172 173 173	OAC OAC OAD OAD	Log Hd Log Hd +20 Log Hd +10 Log Hd
261 262 263	261 262 263	00-18 00-09 10-18 00-18	174 174 175 175	OAE OAE OAF OAF	Log Hd Log Hd +20 Log Hd +10 Log Hd
264 265	264 265	00-18 00-09 10-18	176 176 177	0B0 0B0 0B1	Log Hd Log Hd +20 Log Hd +10
266 267 268 269	266 267 268 269	00-18 00-18 00-09 10-18 00-18	177 178 178 179 179	0B1 0B2 0B2 0B3 0B3	Log Hd Log Hd Log Hd +20 Log Hd +10
270 271 272	270 271 272	00-18 00-09 10-18 00-18	180 180 181 181	083 084 084 085 085	Log Hd Log Hd Log Hd +20 Log Hd +10 Log Hd
273 274 275	273 274 275	00-18 00-09 10-18 00-18	182 182 183 183	0B6 0B6 0B7 0B7	Log Hd Log Hd +20 Log Hd +10 Log Hd
276 277 278	276 277 278	00-18 00-09 10-18 00-18	184 184 185 185	0B8 0B8 0B9 0B9	Log Hd Log Hd +20 Log Hd +10 Log Hd
279 280 281	279 280 281	00-18 00-09 10-18 00-18	186 186 187 187	OBA OBA OBB OBB	Log Hd Log Hd +20 Log Hd +10 Log Hd
282 283 284	282 283 284	00-18 00-09 10-18 00-18	188 188 189 189	OBC OBC OBD OBD	Log Hd Log Hd +20 Log Hd +10 Log Hd
285 286	285 286	00-18 00-09 10-18	190 190 191	OBE OBE OBF	Log Hd Log Hd +20 Log Hd +10
287	287	00-18	191	OBF	Log Hd

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ADDRESS CONVERSION **R/W 411** 

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Log Head

00-18

00-09

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LOGICAL ADDRESS

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# **ADDRESS CONVERSION**

R/W 412 LH

LC	GICAL ADD	IRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
288 289 290	288 289 290	00-18 00-09 10-18 00-18	192 192 193 193	0C0 0C0 0C1 0C1	Log Hd Log Hd +20 Log Hd +10 Log Hd
291 292 293	291 292 293	00-18 00-09 10-18 00-18	194 194 195 195	0C2 0C2 0C3 0C3	Log Hd Log Hd +20 Log Hd +10 Log Hd
294 295 296	294 295 296	00-18 00-09 10-18 00-18	196 196 197 197	0C4 0C4 0C5 0C5	Log Hd Log Hd +20 Log Hd +10 Log Hd
297 298 299	297 298 299	00-18 00-09 10-18 00-18	198 198 199 199	0C6 0C6 0C7 0C7	Log Hd Log Hd +20 Log Hd +10 Log Hd
300 301 302	300 301 302	00-18 00-09 10-18 00-18	200 200 201 201	0C8 0C8 0C9 0C9	Log Hd Log Hd +20 Log Hd +10 Log Hd
303 304 305	303 304 305	00-18 00-09 10-18 00-18	202 202 203 203	OCA OCA OCB OCB	Log Hd Log Hd +20 Log Hd +10 Log Hd
306 307 308	306 307 308	00-18 00-09 10-18 00-18	204 204 205 205	OCC OCC OCD OCD	Log Hd Log Hd +20 Log Hd +10 Log Hd
309 310 311	309 310 311	00-18 00-09 10-18 00-18	206 206 207 207	OCE OCE OCF OCF	Log Hd Log Hd +20 Log Hd +10 Log Hd
312 313 314	312 313 314	00-18 00-09 10-18 00-18	208 208 209 209	0D0 0D0 0D1 0D1	Log Hd Log Hd +20 Log Hd +10 Log Hd
315 316	315 316	00-18 00-09 10-18	210 210 211	0D2 0D2 0D3	Log Hd Log Hd +20 Log Hd +10
317 318 319	317 318 319	00-18 00-18 00-09 10-18	211 212 212 213	0D3 0D4 0D4 0D5	Log Hd Log Hd Log Hd +20 Log Hd +10
320 321 322	320 321 322	00-18 00-18 00-09	213 214 214	0D5 0D6 0D6	Log Hd Log Hd Log Hd +20
323	323	10-18 00-18	215 215	0D7 0D7	Log Hd +10 Log Hd

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PHVQI		IDER and HEAD	Г		IGICAL ADD	IRESS	PHYSI		DER and HEAD
Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals	į L	3330-1 .og Cyl /ol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
216 216 217 217	0D8 0D8 0D9 0D9	Log Hd Log Hd +20 Log Hd +10 Log Hd		360 361 362	360 361 362	00-18 00-09 10-18 00-18	240 240 241 241	CFO OFO OF1 OF1	Log Hd Log Hd +20 Log Hd +10 Log Hd
218 218 219 219	ODA ODA ODB ODB	Log Hd Log Hd +20 Log Hd +10 Log Hd		363 364 365	363 364 365	00-18 00-09 10-18 00-18	242 242 243 243	0F2 0F2 0F3 0F3	Log Hd Log Hd +20 Log Hd +10 Log Hd
220 220 221 221	ODC ODC ODD ODD	Log Hd Log Hd +20 Log Hd +10 Log Hd		366 367 368	366 367 368	00-18 00-09 10-18 00-18	244 244 245 245	0F4 0F4 0F5 0F5	Log Hd Log Hd +20 Log Hd +10 Log Hd
222 222 223 223	ODE ODE ODF ODF	Log Hd Log Hd +20 Log Hd +10 Log Hd	Ň	369 370 371	369 370 371	00-18 00-09 10-18 00-18	246 246 247 247	0F6 0F6 0F7 0F7	Log Hd Log Hd +20 Log Hd +10 Log Hd
224 224 225 225	0E0 0E0 0E1 0E1	Log Hd Log Hd +20 Log Hd +10 Log Hd		372 373 374	372 373 374	00-18 00-09 10-18 00-18	248 248 249 249	0F8 0F8 0F9 0F9	Log Hd Log Hd +20 Log Hd +10 Log Hd
226 226 227 227	0E2 0E2 0E3 0E3	Log Hd Log Hd +20 Log Hd +10 Log Hd		375 376 377	375 376 377	00-18 00-09 10-18 00-18	250 250 251 251	OFA OFA OFB OFB	Log Hd Log Hd +20 Log Hd +10 Log Hd
228 228 229 229	0E4 0E4 0E5 0E5	Log Hd Log Hd +20 Log Hd +10 Log Hd		378 379 380	378 379 380	00-18 00-09 10-18 00-18	252 252 253 253	OFC OFC OFD OFD	Log Hd Log Hd +20 Log Hd +10 Log Hd
230 230 231 231	0E6 0E6 0E7 0E7	Log Hd Log Hd +20 Log Hd +10 Log Hd		381 382 383	381 382 383	00-18 00-09 10-18 00-18	254 254 255 255	OFE OFE OFF OFF	Log Hd Log Hd +20 Log Hd +10 Log Hd
232 232 233 233	0E8 0E8 0E9 0E9	Log Hd Log Hd +20 Log Hd +10 Log Hd		384 385 386	384 385 386	00-18 00-09 10-18 00-18	256 256 257 257	100 100 101 101	Log Hd Log Hd +20 Log Hd +10 Log Hd
234 234 235 235	OEA OEA OEB OEB	Log Hd Log Hd +20 Log Hd +10 Log Hd		387 388 389	387 388 389	00-18 00-09 10-18 00-18	258 258 259 259	102 102 103 103	Log Hd Log Hd +20 Log Hd +10 Log Hd
236 236 237 237	OEC OEC OED OED	Log Hd Log Hd +20 Log Hd +10 Log Hd		390 391 392	390 391 392	00-18 00-09 10-18 00-18	260 260 261 261	104 104 105 105	Log Hd Log Hd +20 Log Hd +10 Log Hd
238 238 239 239	OEE OEE OEF OEF	Log Hd Log Hd +20 Log Hd +10 Log Hd		393 394 395	393 394 395	00-18 00-09 10-18 00-18	262 262 263 263	106 106 107 107	Log Hd Log Hd +20 Log Hd +10 Log Hd

# ADDRESS CONVERSION **R/W 412**

L	DGICAL ADD	RESS	PHYSI	CAL CYLIN	LINDER and HEAD			
3330-1 Log Cyl Vol 1 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals			
396 397 398	396 397 398	00-18 00-09 10-18 00-18	264 264 265 265	108 108 109 109	Log Hd Log Hd +20 Log Hd +10 Log Hd			
399 400 401	399 400 401	00-18 00-09 10-18 00-18	266 266 267 267	10A 10A 10B 10B	Log Hd Log Hd +20 Log Hd +10 Log Hd			
402 403 404	402 403 404	00-18 00-09 10-18 00-18	268 268 269 269	10C 10C 10D 10D	Log Hd Log Hd +20 Log Hd +10 Log Hd			
405 406 407	405 406 407	00-18 00-09 10-18 00-18	270 270 271 271	10E 10E 10F 10F	Log Hd Log Hd +20 Log Hd +10 Log Hd			
408 409 410	408 409 410	00-18 00-09 10-18 00-18	272 272 273 273	110 110 111 111	Log Hd Log Hd +20 Log Hd +10 Log Hd			

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#### ADDRESS CONVERSION

**R/W 412** 

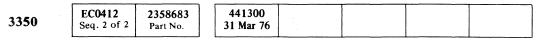
# **ADDRESS CONVERSION**

LOGICAL ADDRESS							
L	1		PHYSICAL CYLINDER and HEAD				
3330-1 Log Cyl Vol 2 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals		
0 1 2	411 412 413	00-18 00-09 10-18 00-18	274 274 275 275	112 112 113 113	Log Hd Log Hd +20 Log Hd +10 Log Hd		
3 4 5	414 415 416	00-18 00-09 10-18 00-18	276 276 277 277	114 114 115 115	Log Hd Log Hd +20 Log Hd +10 Log Hd		
6 7 8	417 418 419	00-18 00-09 10-18 00-18	278 278 279 279	116 116 117 117	Log Hd Log Hd +20 Log Hd +10 Log Hd		
9	420	00-18	280	118	Log Hd		
10	421	00-09	280	118	Log Hd +20		
10	421	10-18	281	119	Log Hd +10		
11	422	00-18	281	119	Log Hd		
12	423	00-18	282	11A	Log Hd		
13	424	00-09	282	11A	Log Hd +20		
13	424	10-18	283	11B	Log Hd +10		
14	425	00-18	283	11B	Log Hd		
15	426	00-18	284	11C	Log Hd		
16	427	00-09	284	11C	Log Hd +20		
16	427	10-18	285	11D	Log Hd +10		
17	428	00-18	285	11D	Log Hd		
18	429	00-18	286	11E	Log Hd		
19	430	00-09	286	11E	Log Hd +20		
19	430	10-18	287	11F	Log Hd +10		
20	431	00-18	287	11F	Log Hd		
21	432	00-18	288	120	Log Hd		
22	433	00-09	288	120	Log Hd +20		
22	433	10-18	289	121	Log Hd +10		
23	434	00-18	289	121	Log Hd		
24	435	00-18	290	122	Log Hd		
25	436	00-09	290	122	Log Hd +20		
25	436	10-18	291	123	Log Hd +10		
26	437	00-18	291	123	Log Hd		
27	438	00-18	292	124	Log Hd		
28	439	00-09	292	124	Log Hd +20		
28	439	10-18	293	125	Log Hd +10		
29	440	00-18	293	125	Log Hd		
30	441	00-18	294	126	Log Hd		
31	442	00-09	294	126	Log Hd +20		
31	442	10-18	295	127	Log Hd +10		
32	443	00-18	295	127	Log Hd		
33	444	00-18	296	128	Log Hd		
34	445	00-09	296	128	Log Hd +20		
34	445	10-18	297	129	Log Hd +10		
35	446	00-18	297	129	Log Hd		

L	)GICAL ADE	DRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 2 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
36	447	00-18	298	12A	Log Hd
37	448	00-09	298	12A	Log Hd +20
37	448	10-18	299	12B	Log Hd +10
38	449	00-18	299	12B	Log Hd
39	450	00-18	300	12C	Log Hd
40	451	00-09	300	12C	Log Hd +20
40	451	10-18	301	12D	Log Hd +10
41	452	00-18	301	12D	Log Hd
42	453	00-18	302	12E	Log Hd
43	454	00-09	302	12E	Log Hd +20
43	454	10-18	303	12F	Log Hd +10
44	455	00-18	303	12F	Log Hd
45	456	00-18	304	130	Log Hd
46	457	00-09	304	130	Log Hd +20
46	457	10-18	305	131	Log Hd +10
47	458	00-18	305	131	Log Hd
48	459	00-18	306	132	Log Hd
49	460	00-09	306	132	Log Hd +20
49	460	10-18	307	133	Log Hd +10
50	461	00-18	307	133	Log Hd
51	462	00-18	308	134	Log Hd
52	463	00-09	308	134	Log Hd +20
52	463	10-18	309	135	Log Hd +10
53	464	00-18	309	135	Log Hd
54	465	00-18	310	136	Log Hd
55	466	00-09	310	136	Log Hd +20
55	466	10-18	311	137	Log Hd +10
56	467	00-18	311	137	Log Hd
57	468	00-18	312	138	Log Hd
58	469	00-09	312	138	Log Hd +20
58	469	10-18	313	139	Log Hd +10
59	470	00-18	313	139	Log Hd
60	471	00-18	314	13A	Log Hd
61	472	00-09	314	13A	Log Hd +20
61	472	10-18	315	13B	Log Hd +10
62	473	00-18	315	13B	Log Hd
63	474	00-18	316	13C	Log Hd
64	475	00-09	316	13C	Log Hd +20
64	475	10-18	317	13D	Log Hd +10
65	476	00-18	317	13D	Log Hd
66	477	00-18	318	13E	Log Hd
67	478	00-09	318	13E	Log Hd +20
67	478	10-18	319	13F	Log Hd +10
68	479	00-18	319	13F	Log Hd
69	480	00-18	320	140	Log Hd
70	481	00-09	320	140	Log Hd +20
70	481	10-18	321	141	Log Hd +10
71	482	00-18	321	141	Log Hd

L	GICAL ADD	IRESS	PHYSICAL CYLINDER and HEAD			
3330-1 Log Cyl Vol 2 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals	
72	483	00-18	322	142	Log Hd	
73	484	00-09	322	142	Log Hd +20	
73	484	10-18	323	143	Log Hd +10	
74	485	00-18	323	143	Log Hd	
75	486	00-18	324	144	Log Hd	
76	487	00-09	324	144	Log Hd +20	
76	487	10-18	325	145	Log Hd +10	
77	488	00-18	325	145	Log Hd	
78	489	00-18	326	146	Log Hd	
79	490	00-09	326	146	Log Hd +20	
79	490	10-18	327	147	Log Hd +10	
80	491	00-18	327	147	Log Hd	
81	492	00-18	328	148	Log Hd	
82	493	00-09	328	148	Log Hd +20	
82	493	10-18	329	149	Log Hd +10	
83	494	00-18	329	149	Log Hd	
84	495	00-18	330	14A	Log Hd	
85	496	00-09	330	14A	Log Hd +20	
85	496	10-18	331	14B	Log Hd +10	
86	497	00-18	331	14B	Log Hd	
87	498	00-18	332	14C	Log Hd	
88	499	00-09	332	14C	Log Hd +20	
88	499	10-18	333	14D	Log Hd +10	
89	500	00-18	333	14D	Log Hd	
90	501	00-18	334	14E	Log Hd	
91	502	00-09	334	14E	Log Hd +20	
91	502	10-18	335	14F	Log Hd +10	
92	503	00-18	335	14F	Log Hd	
93	504	00-18	336	150	Log Hd	
94	505	00-09	336	150	Log Hd +20	
94	505	10-18	337	151	Log Hd +10	
95	506	00-18	337	151	Log Hd	
96	507	00-18	338	152	Log Hd	
97	508	00-09	338	152	Log Hd +20	
97	508	10-18	339	153	Log Hd +10	
98	509	00-18	339	153	Log Hd	
99 100	510 511	00-18 00-09 10-18	340 340 341	154 154 155	Log Hd Log Hd +20 Log Hd +10	
101	512	00-18	341	155	Log Hd	
102 103 104	513 514 515	00-18 00-09 10-18 00-18	342 342 343 343	156 156 157 157	Log Hd Log Hd +20 Log Hd +10 Log Hd	
105 106 107	516 517 518	00-18 00-09 10-18 00-18	344 344 345 345	158 158 159 159	Log Hd Log Hd +20 Log Hd +10 Log Hd	

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# ADDRESS CONVERSION R/W 413

· L(	GICAL ADD	IRESS	PHYSI	PHYSICAL CYLINDER and HEAD			
3330-1 Log Cyl Vol 2 *	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals		
108 109 110	519 520 521	00-18 00-09 10-18 00-18	346 346 347 347	15A 15A 15B 15B	Log Hd Log Hd +20 Log Hd +10 Log Hd		
111 112 113	522 523 524	00-18 00-09 10-18 00-18	348 348 349 349	15C 15C 15D 15D	Log Hd Log Hd +20 Log Hd +10 Log Hd		
114 115 116	525 526 527	00-18 00-09 10-18 00-18	350 350 351 351	15E 15E 15F 15F	Log Hd Log Hd +20 Log Hd +10 Log Hd		
117 118 119	528 529 530	00-18 00-09 10-18 00-18	352 352 353 353	160 160 161 161	Log Hd Log Hd +20 Log Hd +10 Log Hd		
120 121 122	531 532 533	00-18 00-09 10-18 00-18	354 354 355 355	162 162 163 163	Log Hd Log Hd +20 Log Hd +10 Log Hd		
123 124 125	534 535 536	00-18 00-09 10-18 00-18	356 356 357 357	164 164 165 165	Log Hd Log Hd +20 Log Hd +10 Log Hd		
126 127 128	537 538 539	00-18 00-09 10-18 00-18	358 358 359 359	166 166 167 167	Log Hd Log Hd +20 Log Hd +10 Log Hd		
129 130 131	540 541 542	00-18 00-09 10-18 00-18	360 360 361 361	168 168 169 169	Log Hd Log Hd +20 Log Hd +10 Log Hd		
132 133 134	543 544 545	00-18 00-09 10-18 00-18	362 362 363 363	16A 16A 16B 16B	Log Hd Log Hd +20 Log Hd +10 Log Hd		
135 136 137	546 547 548	00-18 00-09 10-18 00-18	364 364 365 365	16C 16C 16D 16D	Log Hd Log Hd +20 Log Hd +10 Log Hd		
138 139 140	549 550 551	00-18 00-09 10-18 00-18	366 366 367 367	16E 16E 16F 16F	Log Hd Log Hd +20 Log Hd +10 Log Hd		
141 142 143	552 553 554	00-18 00-09 10-18 00-18	368 368 369 369	170 170 171 171	Log Hd Log Hd +20 Log Hd +10 Log Hd		

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ADDRESS CONVERSION **R/W 413** 

# **ADDRESS CONVERSION**

LOGICAL ADDRESS			PHYSI	PHYSICAL CYLINDER and HEAD			LC	GICAL ADI	JR
3330-1 Log Cyl Vol 2	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals		3330-1 Log Cyl Vol 2	3330-11 Log Cyl	
144 145	555 556	00-18 00-09 10-18	370 370 371	172 172 173	Log Hd Log Hd +20 Log Hd +10		180 181	591 592	
146 147	557 558	00-18 00-18	371 372	173	Log Hd		182	593	
148	559	00-09 10-18	372 373	174 174 175	Log Hd Log Hd +20 Log Hd +10		183 184	594 595	
149 150	560 561	00-18 00-18	373	175	Log Hd		185	596	
151	562	00-09 10-18	374 374 375	176 176 177	Log Hd Log Hd +20 Log Hd +10		186 187	597 598	
152	563	00-18	375	177	Log Hd		188	599	
153 154	564 565	00-18 00-09 10-18	376 376 377	178 178 179	Log Hd Log Hd +20 Log Hd +10		189 190	600 601	
155	566	00-18	377	179	Log Hd		191	602	
156 157	567 568	00-18 00-09 10-18	378 378 379	17A 17A 17B	Log Hd Log Hd +20 Log Hd +10		192 193	603 604	
158	569	00-18	379	17B	Log Hd		194	605	
159 160	570 571	00-18 00-09 10-18	380 380 381	17C 17C 17D	Log Hd Log Hd +20 Log Hd +10		195 196	606 607	
161	572	00-18	381	17D	Log Hd		197	608	
162 163	573 574	00-18 00-09 10-18	382 382 383	17E 17E 17F	Log Hd Log Hd +20 Log Hd +10		198 199	609 610	
164	575	00-18	383	17F	Log Hd		200	611	
165 166	576 577	00-18 00-09 10-18	384 384 385	180 180 181	Log Hd Log Hd +20 Log Hd +10		201 202	612 613	
167	578	00-18	385	181	Log Hd		203	614	
168 169	579 580	00-18 00-09 10-18	386 386 387	182 182 183	Log Hd Log Hd +20 Log Hd +10		204 205	615 616	
170	581	00-18	387	183	Log Hd		206	617	
171 172	582 583	00-18 00-09 10-18	388 388 389	184 184 185	Log Hd Log Hd +20 Log Hd +10		207 208	618 619	
173	584	00-18	389	185	Log Hd		209	620	
174 175	585 586	00-18 00-09 10-18	390 390 391	186 186 187	Log Hd Log Hd +20 Log Hd +10		210 211	621 622	
176	587	00-18	391	187	Log Hd +10		212	623	
177 178	588 589	00-18 00-09 10-18	392 392 393	188 188 189	Log Hd Log Hd +20 Log Hd +10		213 214 214	624 625 625	
179	590	00-18	393	189	Log Hd		214	626	

L	DGICAL ADI	DRESS	PHYSI	PHYSICAL CYLINDER and HEAD				
3330-1 Log Cyl Vol 2	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals			
180 181 182	591 592 593	00-18 00-09 10-18 00-18	394 394 395 395	18A 18A 18B 18B	Log Hd Log Hd +20 Log Hd +10 Log Hd			
183 184	594 595	00-18 00-09 10-18	396 396 397	18C 18C 18D	Log Hd Log Hd +20 Log Hd +10			
185 186 187	596 597 598	00-18 00-18 00-09 10-18	397 398 398 399	18D 18E 18E 18F	Log Hd Log Hd Log Hd +20 Log Hd +10			
188 189 190	599 600 601	00-18 00-18 00-09 10-18	399 400 400 401	18F 190 190	Log Hd Log Hd Log Hd +20			
191 192	602 603	00-18	401 401 402	191 191 192	Log Hd +10 Log Hd			
192 193 194	604 605	00-09 10-18 00-18	402 402 403 403	192 192 193 193	Log Hd Log Hd +20 Log Hd +10 Log Hd			
195 196 197	606 607 608	00-18 00-09 10-18 00-18	404 404 405 405	194 194 195 195	Log Hd Log Hd +20 Log Hd +10 Log Hd			
198 199 200	609 610 611	00-18 00-09 10-18 00-18	406 406 407 407	196 196 197	Log Hd Log Hd +20 Log Hd +10			
201 202	612 613	00-18 00-09 10-18	408 408 409	197 198 198 199	Log Hd Log Hd Log Hd +20 Log Hd +10			
203 204 205	614 615 616	00-18 00-18 00-09 10-18	409 410 410 411	199 19A 19A 19B	Log Hd Log Hd Log Hd +20 Log Hd +10			
206 207	617 618	00-18 00-18	411 412	19B 19C	Log Hd Log Hd			
208 209	619 620	00-09 10-18 00-18	412 413 413	19C 19D 19D	Log Hd +20 Log Hd +10 Log Hd			
210 211 212	621 622 623	00-18 00-09 10-18 00-18	414 414 415 415	19E 19E 19F 19F	Log Hd Log Hd +20 Log Hd +10 Log Hd			
213 214 214 214 215	624 625 625 626	00-18 00-09 10-18 00-18	416 416 417 417	1A0 1A0 1A1 1A1	Log Hd Log Hd +20 Log Hd +10 Log Hd			

L	GICAL ADD	RESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 2	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
216 217 218	627 628 629	00-18 00-09 10-18 00-18	418 418 419 419	1A2 1A2 1A3 1A3	Log Hd Log Hd +20 Log Hd +10
219 220	630 631	00-18 00-09 10-18	420 420 421	1A4 1A4 1A5	Log Hd Log Hd Log Hd +20 Log Hd +10
221 222 223	632 633 634	00-18 00-18 00-09 10-18	421 422 422 423	1A5 1A6 1A6 1A7	Log Hd Log Hd Log Hd +20 Log Hd +10
224 225 226	635 636 637	00-18 00-18 00-09 10-18	423 424 424 425	1A7 1A8 1A8 1A9	Log Hd Log Hd Log Hd +20 Log Hd +10
227 228 229	638 639 640	00-18 00-18 00-09 10-18	425 426 426 427	1A9 1AA 1AA 1AB	Log Hd Log Hd Log Hd +20 Log Hd +10
230 231 232	641 642 643	00-18 00-18 00-09 10-18	427 428 428 429	1AB 1AC 1AC 1AD	Log Hd +20 Log Hd +10
233 234 235	644 645 646	00-18 00-18 00-09 10-18	429 430 430 431	1AD 1AE 1AE 1AF	Log Hd Log Hd Log Hd +20 Log Hd +10
236 237 238	647 648 649	00-18 00-18 00-09 10-18	431 432 432 433	1AF 1B0 1B0 1B1	Log Hd Log Hd Log Hd +20 Log Hd +10
239 240 241	650 651 652	00-18 00-18 00-09 10-18	433 434 434 435	1B1 1B2 1B2 1B3	Log Hd Log Hd Log Hd +20 Log Hd +10
242 243 244	653 654 655	00-18 00-18 00-09 10-18	435 436 436 437	1B3 1B4 1B4 1B5	Log Hd Log Hd Log Hd +20 Log Hd +10
245 246 247	656 657 658	00-18 00-18 00-09 10-18	437 438 438 439	185 186 186 187	Log Hd Log Hd Log Hd +20 Log Hd +10
248 249 250	659 660 661	00-18 00-18 00-09 10-18	439 440 440 441	187 188 188 189	Log Hd Log Hd Log Hd +20 Log Hd +10
251	662	00-18	441	1B9	Log Hd

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# ADDRESS CONVERSION **R/W 414**

LC	GICAL ADD	DRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 2	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
252 253 254	663 664 665	00-18 00-09 10-18 00-18	442 442 443 443	1BA 1BA 1BB 1BB	Log Hd Log Hd +20 Log Hd +10 Log Hd
255 256 257	666 667 668	00-18 00-09 10-18 00-18	444 444 445 445	1BC 1BC 1BD 1BD	Log Hd Log Hd +20 Log Hd +10 Log Hd
258 259 260	669 670 671	00-18 00-09 10-18 00-18	446 446 447 447	1BE 1BE 1BF 1BF	Log Hd Log Hd +20 Log Hd +10 Log Hd
261 262 263	672 673 674	00-18 00-09 10-18 00-18	448 448 449 449	1C0 1C0 1C1 1C1	Log Hd Log Hd +20 Log Hd +10 Log Hd
264 265 266	675 676 677	00-18 00-09 10-18 00-18	450 450 451 451	1C2 1C2 1C3 1C3	Log Hd Log Hd +20 Log Hd +10 Log Hd
267 268 269	678 679 680	00-18 00-09 10-18 00-18	452 452 453 453	1C4 1C4 1C5 1C5	Log Hd Log Hd +20 Log Hd +10 Log Hd
270 271 272	681 682 683	00-18 00-09 10-18 00-18	454 454 455 455	1C6 1C6 1C7 1C7	Log Hd Log Hd +20 Log Hd +10 Log Hd
273 274 275	684 685 686	00-18 00-09 10-18 00-18	456 456 457 457	1C8 1C8 1C9 1C9	Log Hd Log Hd +20 Log Hd +10 Log Hd
276 277 278	687 688 689	00-18 00-09 10-18 00-18	458 458 459 459	1CA 1CA 1CB 1CB	Log Hd Log Hd +20 Log Hd +10 Log Hd
279 280 281	690 691 692	00-18 00-09 10-18 00-18	460 460 461 461	1CC 1CC 1CD 1CD	Log Hd Log Hd +20 Log Hd +10 Log Hd
282 283 284	693 694 695	00-18 00-09 10-18 00-18	462 462 463 463	1CE 1CE 1CF 1CF	Log Hd Log Hd +20 Log Hd +10 Log Hd
285 286 287	696 , 697 698	00-18 00-09 10-18 00-18	464 464 465 465	1D0 1D0 1D1 1D1	Log Hd Log Hd +20 Log Hd +10 Log Hd

Continued on R/W 415.

# **ADDRESS CONVERSION**

L	OGICAL ADD	RESS	PHYSI	CAL CYLIN	IDER and HEAD	L	GICAL ADD	DRESS	PHYSI	CAL CYLIN	IDER and HEAD	L	OGICAL ADI	DRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 2	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals	3330-1 Log Cyl Vol 2	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals	3330-1 Log Cyl Vol 2	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
288 289 290	699 700 701	00-18 00-09 10-18 00-18	466 466 467 467	1D2 1D2 1D3 1D3	Log Hd Log Hd +20 Log Hd +10 Log Hd	324 325 326	735 736 737	00-18 00-09 10-18 00-18	490 490 491 491	1EA 1EA 1EB 1EB	Log Hd Log Hd +20 Log Hd +10 Log Hd	360 361 362	771 772 773	00-18 00-09 10-18 00-18	514 514 515 515	202 202 203 203	Log Hd Log Hd +20 Log Hd +10 Log Hd
291 292 293	702 703 704	00-18 00-09 10-18 00-18	468 468 469 469	1D4 1D4 1D5 1D5	Log Hd Log Hd +20 Log Hd +10 Log Hd	327 328 329	738 739 740	00-18 00-09 10-18 00-18	492 492 493 493	1EC 1EC 1ED 1ED	Log Hd Log Hd +20 Log Hd +10 Log Hd	363 364 365	774 775 776	00-18 00-09 10-18 00-18	516 516 517 517	204 204 205 205	Log Hd Log Hd +20 Log Hd +10 Log Hd
294 295 296	705 706 707	00-18 00-09 10-18 00-18	470 470 471 471	1D6 1D6 1D7 1D7	Log Hd Log Hd +20 Log Hd +10 Log Hd	330 331 332	741 742 743	00-18 00-09 10-18 00-18	494 494 495 495	1EE 1EE 1EF 1EF	Log Hd Log Hd +20 Log Hd +10 Log Hd	366 367 368	777 778 779	00-18 00-09 10-18 00-18	518 518 519 519	206 206 207 207	Log Hd Log Hd +20 Log Hd +10 Log Hd
297 298 299	708 709 710	00-18 00-09 10-18 00-18	472 472 473 473	1D8 1D8 1D9 1D9	Log Hd Log Hd +20 Log Hd +10 Log Hd	333 334 335	744 745 746	00-18 00-09 10-18 00-18	496 496 497 497	1F0 1F0 1F1 1F1	Log Hd Log Hd +20 Log Hd +10 Log Hd	369 370 371	780 781 782	00-18 00-09 10-18 00-18	520 520 521 521	208 208 209 209	Log Hd Log Hd +20 Log Hd +10 Log Hd
300 301 302	711 712 713	00-18 00-09 10-18 00-18	474 474 475 475	1DA 1DA 1DB 1DB	Log Hd Log Hd +20 Log Hd +10 Log Hd	336 337 338	747 748 749	00-18 00-09 10-18 00-18	498 498 499 499	1F2 1F2 1F3 1F3	Log Hd Log Hd +20 Log Hd +10 Log Hd	372 373 374	783 784 785	00-18 00-09 10-18 00-18	522 522 523 523	20A 20A 20B 20B	Log Hd Log Hd +20 Log Hd +10 Log Hd
303 304 305	714 715 716	00-18 00-09 10-18 00-18	476 476 477 477	1DC 1DC 1DD 1DD	Log Hd Log Hd +20 Log Hd +10 Log Hd	339 340 341	750 751 752	00-18 00-09 10-18 00-18	500 500 501 501	1F4 1F4 1F5 1F5	Log Hd Log Hd +20 Log Hd +10 Log Hd	375 376 376 376 377	786 787 787 788	00-18 00-09 10-18 00-18	524 524 525 525	20C 20C 20D 20D	Log Hd Log Hd +20 Log Hd +10 Log Hd
306 307 308	717 718 719	00-18 00-09 10-18 00-18	478 478 479 479	1DE 1DE 1DF 1DF	Log Hd Log Hd +20 Log Hd +10 Log Hd	342 343 344	753 754 755	00-18 00-09 10-18 00-18	502 502 503 503	1F6 1F6 1F7 1F7	Log Hd Log Hd +20 Log Hd +10 Log Hd	378 379 380	789 790 791	00-18 00-09 10-18 00-18	526 526 527 527	20E 20E 20F 20F	Log Hd Log Hd +20 Log Hd +10 Log Hd
309 310 311	720 721 722	00-18 00-09 10-18 00-18	480 480 481 481	1E0 1E0 1E1 1E1	Log Hd Log Hd +20 Log Hd +10 Log Hd	345 346 347	756 757 758	00-18 00-09 10-18 00-18	504 504 505 505	1F8 1F8 1F9 1F9	Log Hd Log Hd +20 Log Hd +10 Log Hd	381 382 383	792 793 794	00-18 00-09 10-18 00-18	528 528 529 529	210 210 211 211	Log Hd Log Hd +20 Log Hd +10 Log Hd
312 313 313 314	723 724 724 725	00-18 00-09 10-18 00-18	482 482 483 483	1E2 1E2 1E3 1E3	Log Hd Log Hd +20 Log Hd +10 Log Hd	348 349 350	759 760 761	00-18 00-09 10-18 00-18	506 506 507 507	1FA 1FA 1FB 1FB	Log Hd Log Hd +20 Log Hd +10 Log Hd	384 385 385 385 386	795 796 796 797	00-18 00-09 10-18 00-18	530 530 531 531	212 212 213 213	Log Hd Log Hd +20 Log Hd +10 Log Hd
315 316 317	726 727 728	00-18 00-09 10-18 00-18	484 484 485 485	1E4 1E4 1E5 1E5	Log Hd Log Hd +20 Log Hd +10 Log Hd	351 352 353	762 763 764	00-18 00-09 10-18 00-18	508 508 509 509	1FC 1FC 1FD 1FD	Log Hd Log Hd +20 Log Hd +10 Log Hd	387 388 389	798 799 800	00-18 00-09 10-18 00-18	532 532 533 533	214 214 215 215	Log Hd Log Hd +20 Log Hd +10 Log Hd
318 319 320	729 730 731	00-18 00-09 10-18 00-18	486 486 487 487	1E6 1E6 1E7 1E7	Log Hd Log Hd +20 Log Hd +10 Log Hd	354 355 356	765 766 767	00-18 00-09 10-18 00-18	510 510 511 511	1FE 1FE 1FF 1FF	Log Hd Log Hd +20 Log Hd +10 Log Hd	390 391 392	801 802 803	00-18 00-09 10-18 00-18	534 534 535 535	216 216 217 217	Log Hd Log Hd +20 Log Hd +10 Log Hd
321 322 323	732 733 734	00-18 00-09 10-18 00-18	488 488 489 489	1E8 1E8 1E9 1E9	Log Hd Log Hd +20 Log Hd +10 Log Hd	357 358 359	768 769 770	00-18 00-09 10-18 00-18	512 512 513 513	200 200 201 201	Log Hd Log Hd +20 Log Hd +10 Log Hd	393 394 395	804 805 806	00-18 00-09 10-18 00-18	536 536 537 537	218 218 219 219	Log Hd Log Hd +20 Log Hd +10 Log Hd

3350	EC0414 Seq. 2 of 2	2358684 Part No.	441300 31 Mar 76	441303 30 Jul 76			-	
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5-1-

# ADDRESS CONVERSION **R/W 415**

LC	GICAL ADD	IRESS	PHYSI	CAL CYLIN	DER and HEAD
3330-1 Log Cyl Vol 2	3330-11 Log Cyl	Log Head	Phy Cyl in Dec	Phy Cyl in Hex	Phy Head Equals
396 397 398	807 808 809	00-18 00-09 10-18 00-18	538 538 539 539	21A 21A 21B 21B	Log Hd Log Hd +20 Log Hd +10 Log Hd
399 400 401	810 811 812	00-18 00-09 10-18 00-18	540 540 541 541	21C 21C 21D 21D	Log Hd Log Hd +20 Log Hd +10 Log Hd
402 403 404	813 814	00-18 00-09 10-18 00-18	542 542 543 543	21E 21E 21F 21F	Log Hd Log Hd +20 Log Hd +10 Log Hd
405 406 407		00-18 00-09 10-18 00-18	544 544 545 545	220 220 221 221	Log Hd Log Hd +20 Log Hd +10 Log Hd
408 409 410		00-18 00-09 10-18 00-18	546 546 547 547	222 222 223 223	Log Hd Log Hd +20 Log Hd +10 Log Hd

End of Address Conversion Chart.

# ADDRESS CONVERSION **R/W 415**

0 0

## **TROUBLE NOT FOUND**

А

This page contains aids for problem resolution where insufficient error information is available to follow the maintenance analysis procedure. It may also be used as an aid in analyzing intermittent errors.

#### SENSE BYTE ANALYSIS

Examine all available system sense information for multiple error conditions (see R/W 102). If errors other than the primary error are occuring, exit to the appropriate page listed in the chart below.

	Sense I	Page		
Byte 7	Byte 17	Byte 12	Byte 19	Entry
4x	C0 or C1			R/W 300, D
		Bit 0=1 Bit 1=1 Bit 2=1 Bit 3=1 Bit 4=1 Bit 5=1 Bit 6=1 Bit 7=1	Bit 4=1 Bit 5=1	R/W 180, A R/W 170, A R/W 160, A R/I 100, A R/W 150, A R/W 140, A R/W 120, A R/W 130, A R/W 200, A R/W 190, A
		Other		FSI section

#### **EC INSTALLATION**

If an engineering change has been recently installed, check the EC Installation Instructions and determine where the change was made. Inspect the back panel for tight wire wraps.

#### **VOLTAGE CHECKS**

A2 Module –See the procedure on PWR 90, Entry B.

B2 Module -See the procedure on PWR 290, Entry B.

### **CABLES**

Verify that the following cable connector pins are not bent or pushed in and that the connectors are seated properly:

#### **HDA Cables**

A1Y3(A1Y4)	
A1B2(A1U2)	
01C(01D)A1A2	
01C(01D)A1A3	

**R/W** Data Cables

(if present)A1B3
A1U3
A1V5(A1A5)
A2V2(A2 Module)

#### JUMPERS

Check special voltage jumper from +6 Vdc to A1J3(A1M3)B11 (see YA090 or YB090).

#### **TERMINATION**

Check for correct R/W termination on the last module in the string (see R/W 326).

#### HDA

The HDA cable swapping procedure on HDA 713 can be used to help isolate an HDA problem. See HDA 710 for the HDA replacement procedure. See HDA 708 for voice coil replacement procedure.

#### **SUMMARY OF CARDS**

Reseat or Replace:

#### Drive

A1H2(A1N2)				
A1G2(A1P2)				
A1J2(A1M2)				
A1J4(A1M4)				
A1D4(A1S4)				
A1E2(A1R2)				
A1F2(A1Q2)				
A1K2(A1L2)				
Controller				

A2T2 A2Q2 A2F2 A2P2 A2L2 A2S2

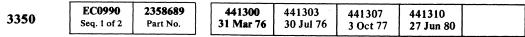
Read/Write Control Head Select and Read/Write Control Read Detector Pad Controls Index Capable/Enable Read Only-Capable/Enable Command Decode and Device Interface

Read/Write Driver and VFO Read/Write Control Device Interface Gap Counter Read/Write Latch SERDES

#### REFERENCES

Set Read/Write operation
Write operation
Read operation
HDA description
Track format
3330 compatibility
Fixed heads
Address conversion
Sense Byte analysis

OPER 210 and 211 OPER 225 and 226 OPER 230 through 233 OPER 30 OPER 33 through 37 OPER 40 through 52 **OPER 250 R/W 400 R/W 102** 



#### **R/W 990** TROUBLE NOT FOUND

R/W 990 TROUBLE NOT FOUND

# **TROUBLE NOT FOUND**

# A

This page contains aids for problem resolution where insufficient error information is available to follow the maintenance analysis procedure. It may also be used as an aid in analyzing intermittent errors.

#### **CHECK DEVICE ADDRESS**

Check EREP printouts to determine if more than one drive is failing. See START 103 to determine physical drive.

#### **EC INSTALLATION**

If an engineering change has been recently installed, check the EC Installation Instructions and determine where the change was made. Inspect the back panel for tight wire wraps.

#### **VOLTAGE CHECKS**

**Drive Voltage Chart** 

Voltage*	Test Point	Tolerance	Maximum** AC Ripple	Page Entry	
-4 V	A1C2 (A1T2) B06(-) to A1K2D08(+)	-3.85 to -4.50 V	0.23 V p-p	PWR 255, A	
+6 V	A1F2 (A1Q2) B11(+) to A1F2 (A1Q2) D08(-)	+ 5.76 to + 6.24 V	0.08 V p-p	. PWR 260, A	

Use a digital voltmeter to check voltages.

\*\* Use a scope to measure the ripple. See PWR 290 for the procedure.

#### **Controller Voltage Chart**

Voltage*	Test Point	Tolerance	Maximum** AC Ripple	Page Entry
-4 V	A2T2B06(-) to A2T2D08(+)	3.84 to4.16 V		PWR 55, B
+6 V	A2T2G11(+) to A2T2J08(-)	+ 5.76 to + 6.24 V		PWR 60, A

\* Use a digital voltmeter to check voltages.

\*\* Use a scope to measure the ripple. See PWR 90 for the procedure.

#### **ERROR RE-CREATION**

#### **Microdiagnostics**

Routine B1 is the primary tool used to re-create Data Check failures. Control options and parameters may be selected to:

1. Scan any single cylinder and stop on error.

#### 2. Scan any single cylinder and log error.

3. Scan any single cylinder, loop, and log error.

- 4. Scan any single track and stop on error.
- 5. Scan any single track, loop, and stop on error.

#### See MICRO 56 for operating instructions.

Routine B2 writes and reads on the CE cylinder. Control options and parameters may be selected to:

- 1. Write and read the entire CE cylinder and stop on error.
- 2. Write and read the entire CE cylinder, loop, and stop on error.
- 3. Write and read one CE track and stop on error.
- 4. Write and read one CE track, loop, and stop on error.

See MICRO 60 for operating instructions.

Routines AD, AF, and AE check Read/Write and ECC hardware in the controller. Any one of these routines may be looped using a control option.

#### OLTS

T3350PSA (Pack Scan A) reads Home Address and R0 fields then compares the CCHH bytes of both fields. Options may be selected to:

- 1. Read all logical cylinders and heads.
- 2. Read all logical cylinders and heads between specified limits.

See OLT 20 for operating instructions.

T3350PSB (Pack Scan B) reads all records on tracks scanned. Options may be selected to:

- 1. Read all logical cylinders and heads.
- 2. Read all logical cylinders and heads between specified limits.

See OLT 24 for operating instructions.

T3350WT (Track Analysis) writes and reads many different length records with worst case patterns on a specified track. Customer data will be destroyed. See OLT 25 for operating instructions.

#### SUMMARY OF CARDS

#### Reseat or Replace:

Drive

A1J2(A1M2) A1H2(A1N2) A1G2(A1P2) A1K2(A1L2) only)

Controller

A2T2 A2S2 A2Q2 A2P2 A2R4 A2K2 A2F2 A2R2

#### **REFERENCES**

Read data flow **Read** operation Set Read/Write HDA description Track format 3330 compatibility Fixed heads

EC0990 2358689 441300 441303 441307 441310 3350 31 Mar 76 30 July 76 27 Jun 80 Seq. 2 of 2 Part No. 3 Oct 77 © Copyright IBM Corporation 1976, 1977

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### TROUBLE NOT FOUND **R/W 995**

A1B2 (in last module

#### Servo Power Amplifiers

**Read Detector** Read/Write Control Head Selection File Control

Read/Write and PLO Termination (See LOC 4 or 14)

Driver/Receiver and VFO SERDES, Data Reg, and ECC Control **Read/Write Control** Gap Counter **ECC Shift Register** Bus In Assembler **Bus In Register** No Data Found Detection

**Read Home Address** Address conversion PA3 byte conversion Sense Byte analysis

R/W 326 and 327 OPER 230 through 233 R/W 360 through 364 OPER 210 and 211 OPER 30 OPER 33 through 37 OPER 40 through 52 **OPER 250 R/W 400 R/W 330 R/W 302** 

#### TROUBLE NOT FOUND **R/W 995**

## **RPI CONTENTS**

1

<b>RPI MAPS</b>			•	•		•		•	•	RPI 130 - 310	
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TROUBLE NOT FOUND . . . RPI 990

## **REFERENCE TO OTHER SECTIONS**

Index DetectionOPER 126Rotational Position SensingOPER 203 - 205

	3350	EE0001 Seq. 1 of 2	2358190 Part No. ( )	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		
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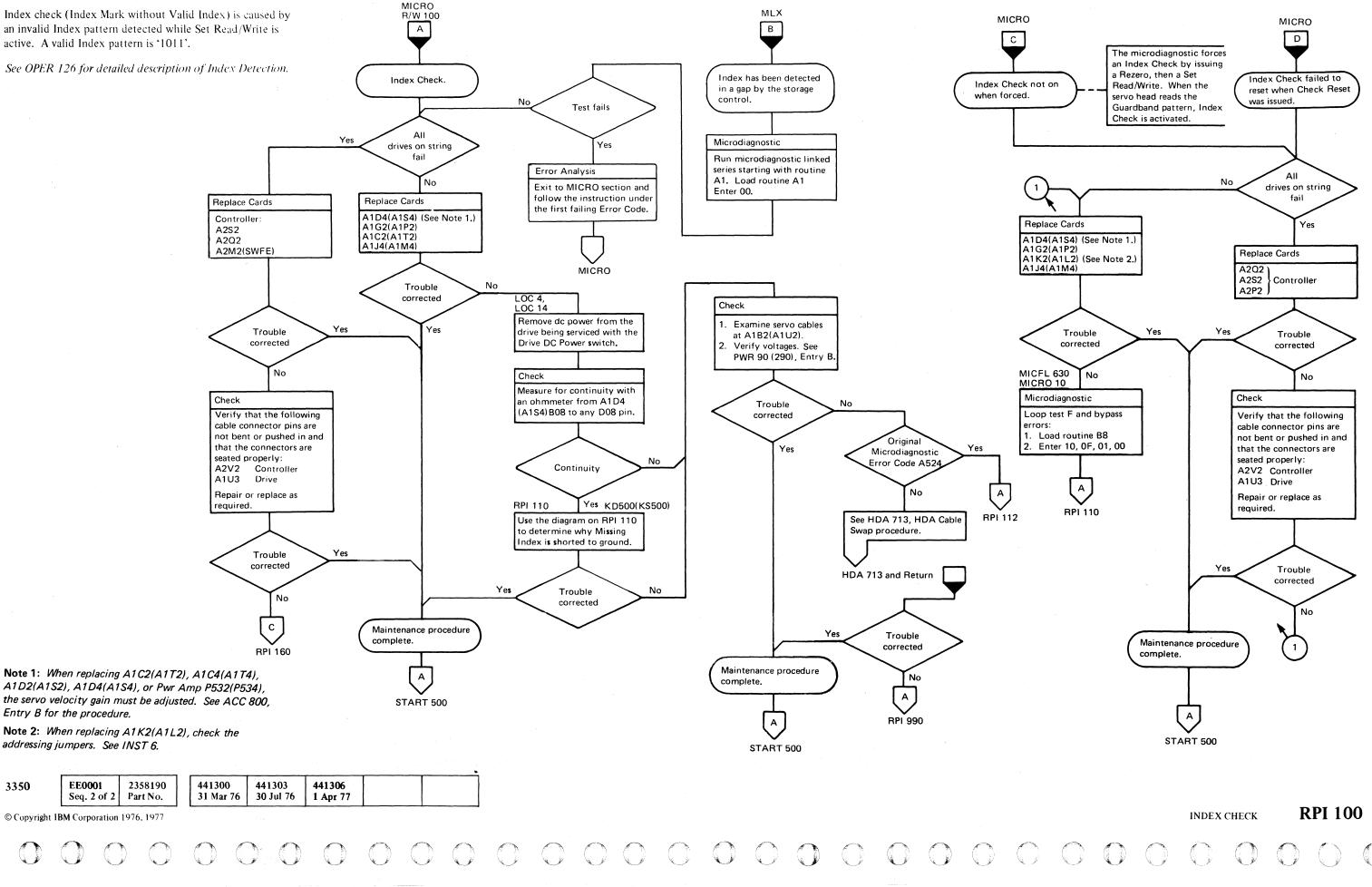
### **RPI CONTENTS**

RPI 1

#### **RPI CONTENTS**

Index check (Index Mark without Valid Index) is caused by an invalid Index pattern detected while Set Read/Write is active. A valid Index pattern is '1011'.

See OPER 126 for detailed description of Index Detection.



Seq. 2 of 2 © Copyright IBM Corporation 1976, 1977

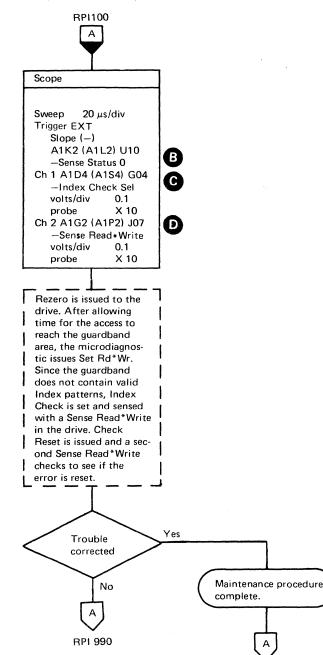
EE0001

Entry B for the procedure.

3350

Routine B8, test F contains long delay times (in excess of 400 ms). Because of the long delay times involved, the following sync points can be used to scope the set or reset of Index Check Sel without using delayed sweep:

- Setting of the error, sync on A1K2(A1L2) P10 (-Drive Sync Tag).
- Resetting of the error, sync on A1K2 (A1L2) U10 (-Sense Status 0).



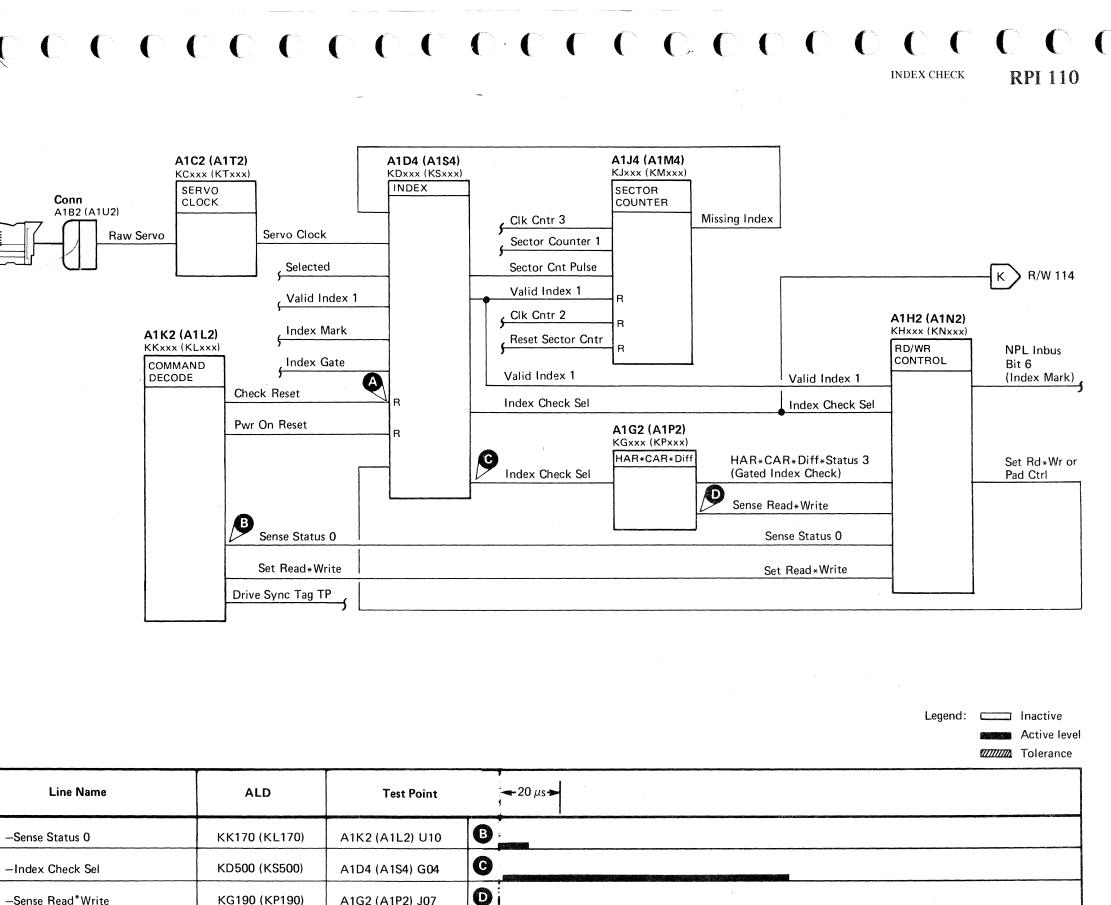
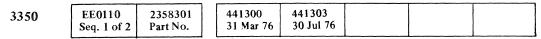


Chart Line No.	Line Name	ALD	Test Point		<b>←</b> 20 μs
1	-Sense Status 0	KK170 (KL170)	A1K2 (A1L2) U10	B	-
2	-Index Check Sel	KD500 (KS500)	A1D4 (A1S4) G04	C	·
3	-Sense Read <sup>*</sup> Write	KG190 (KP190)	A1G2 (A1P2) J07	D	
4	–Check Reset	KD510 (KS510)	A1D4 (A1S4) B12		



START 500

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Missing Index or an invalid Index Mark during a Set Read\*Write operation activates the Index Check Select latch. Index Check Select latch activates Read/Write Check. Sense Read\*Write and Selected gate the Read/Write Check to the interface as NPL Inbus Bit 3. Reading and writing are inhibited until the Index Check Select latch is reset by either Power On Reset or Check Reset.

#### **Missing Index**

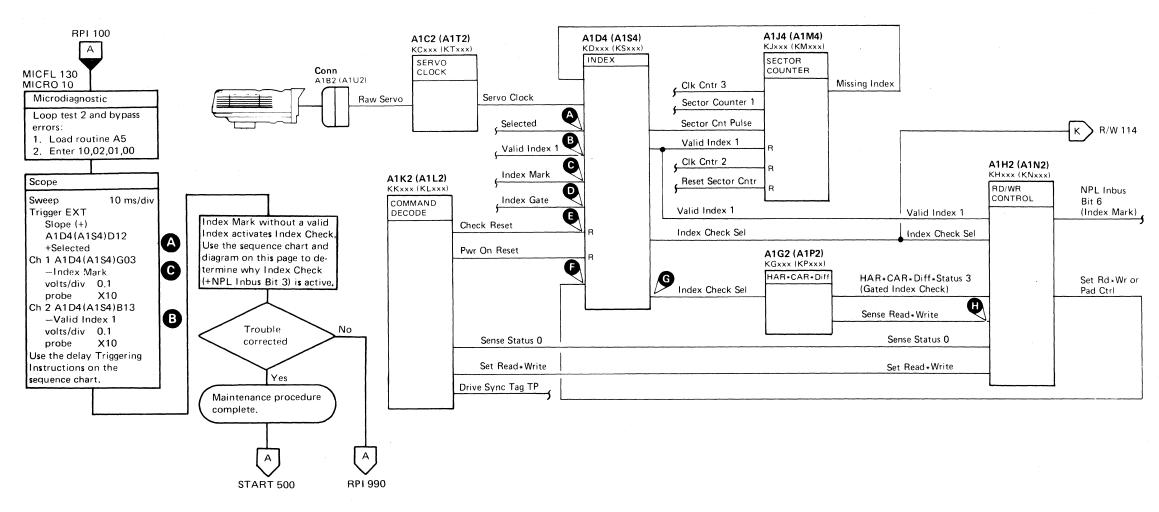
Missing Index is activated, after Sector 127, by the following conditions:

- Clock Counter 3 active.
- Valid Index 1 inactive.

#### Invalid Index Mark

Invalid Index Mark consists of the following conditions:

- Index Mark active.
- Valid Index 1 inactive.



#### Figure 1. Expanded Sequence Chart

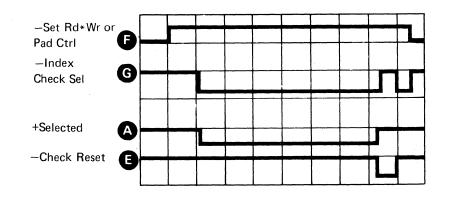
Change Delay Time-Delay Sweep to 1  $\mu$ s/div.

Use Ch 2 to scope each of the lines.

EE0110

3350

2358301



441300

441303

**Triggering Instructions** 

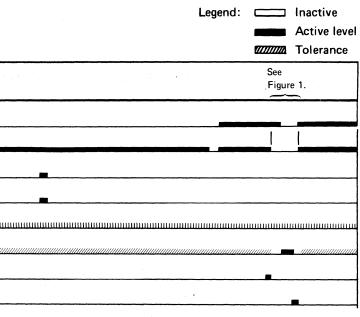
B Sweep Mode – B Starts After Delay Time Delay Time-Delay Sweep - 2 ms/div

A and B Time/Div – 10 ms/div Delay-Time Multiplier – 6.5

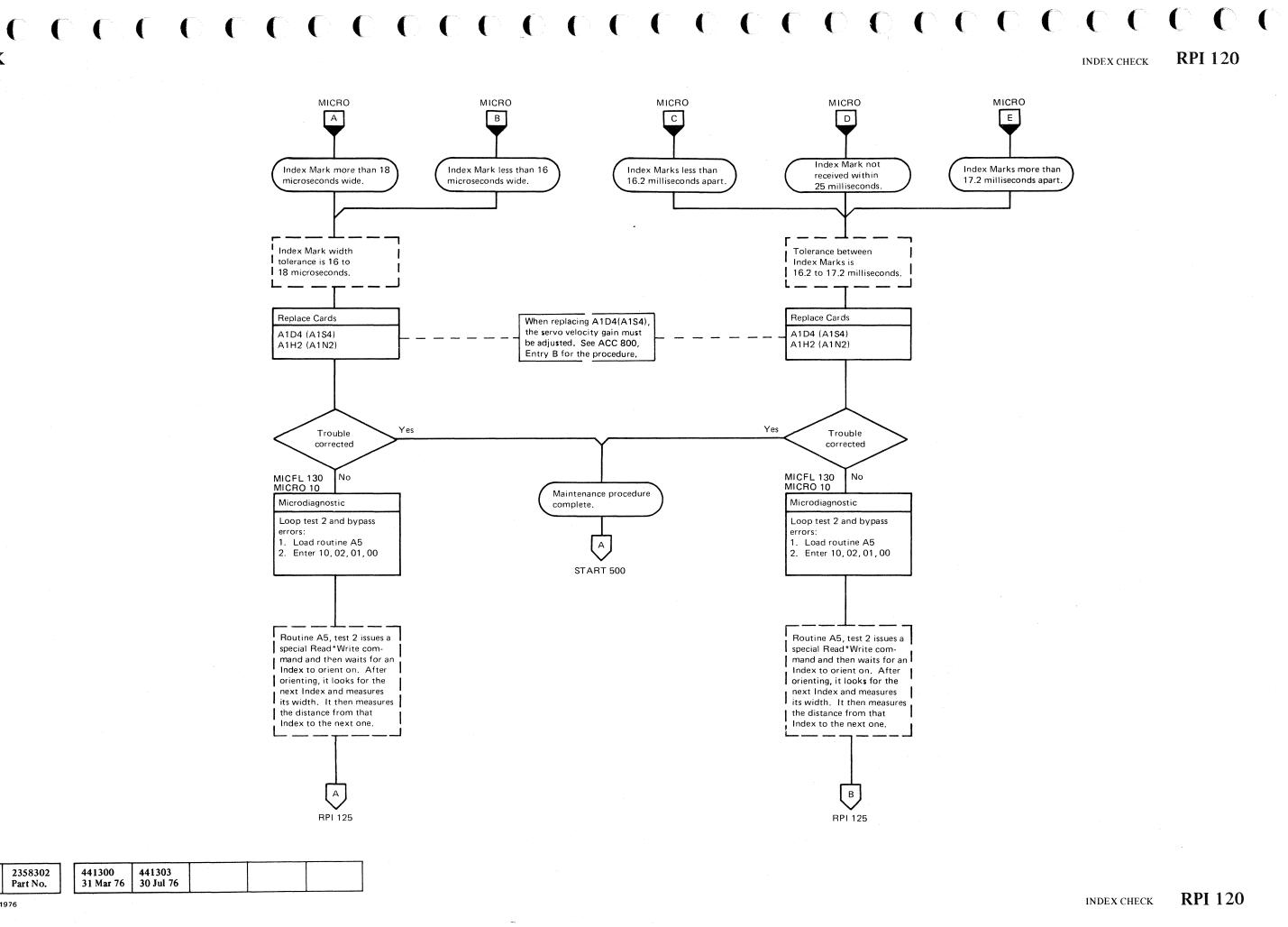
Slope -(+)Source – Int Ch 1

Chart Line No.	Line Name	ALD	Test Point		
1	+Selected	KD510 (KS510)	A1D4 (A1S4) D12	4	
2	-Set Rd*Wr or Pad Ctrl	KD500 (KS500)	A1D4 (A1S4) G02	G	
3	–Index Mark	KD500 (KS500)	A1D4 (A1S4) G03	G	
4	–Valid Index 1	KD520 (KS520)	A1D4 (A1S4) B13	B	
5	+Index Gate	KD500 (KS500)	A1D4 (A1S4) B07	O	
6	—Index Check Sel	KD500 (KS500)	A1D4 (A1S4) G04	G	1, 2, 4
7	-Sense Read <sup>*</sup> Write	KG190 (KP190)	A1G2 (A1P2) J07	0	
8	–Check Reset	KD510 (KS510)	A1D4 (A1S4) B12	8	

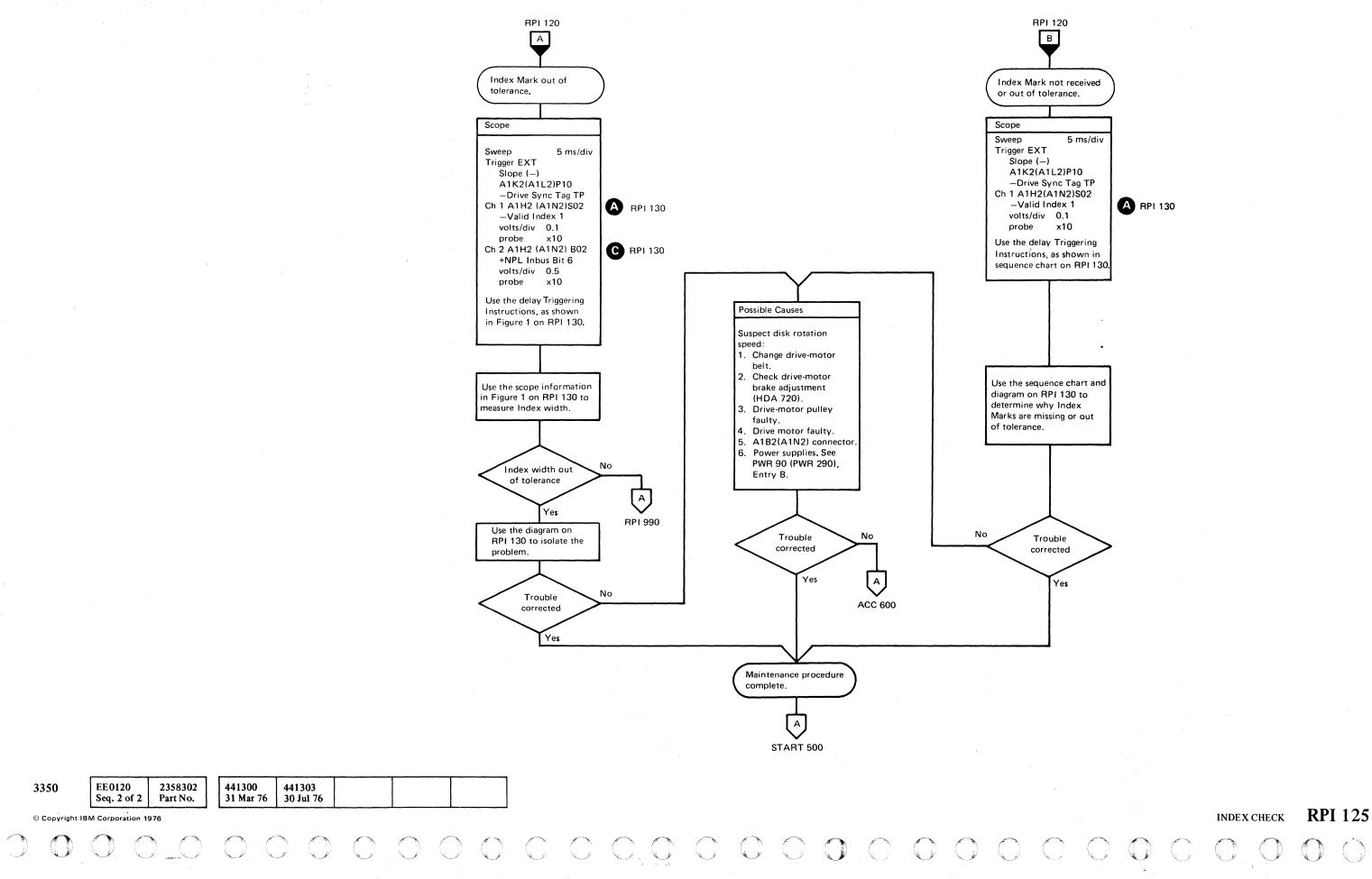
30 Jul 76 Seq. 2 of 2 31 Mar 76 Part No. 







3350	EE0120 Seq. 1 of 2	2358302 Part No.	441300 31 Mar 76	441303 30 Jul 76	-			
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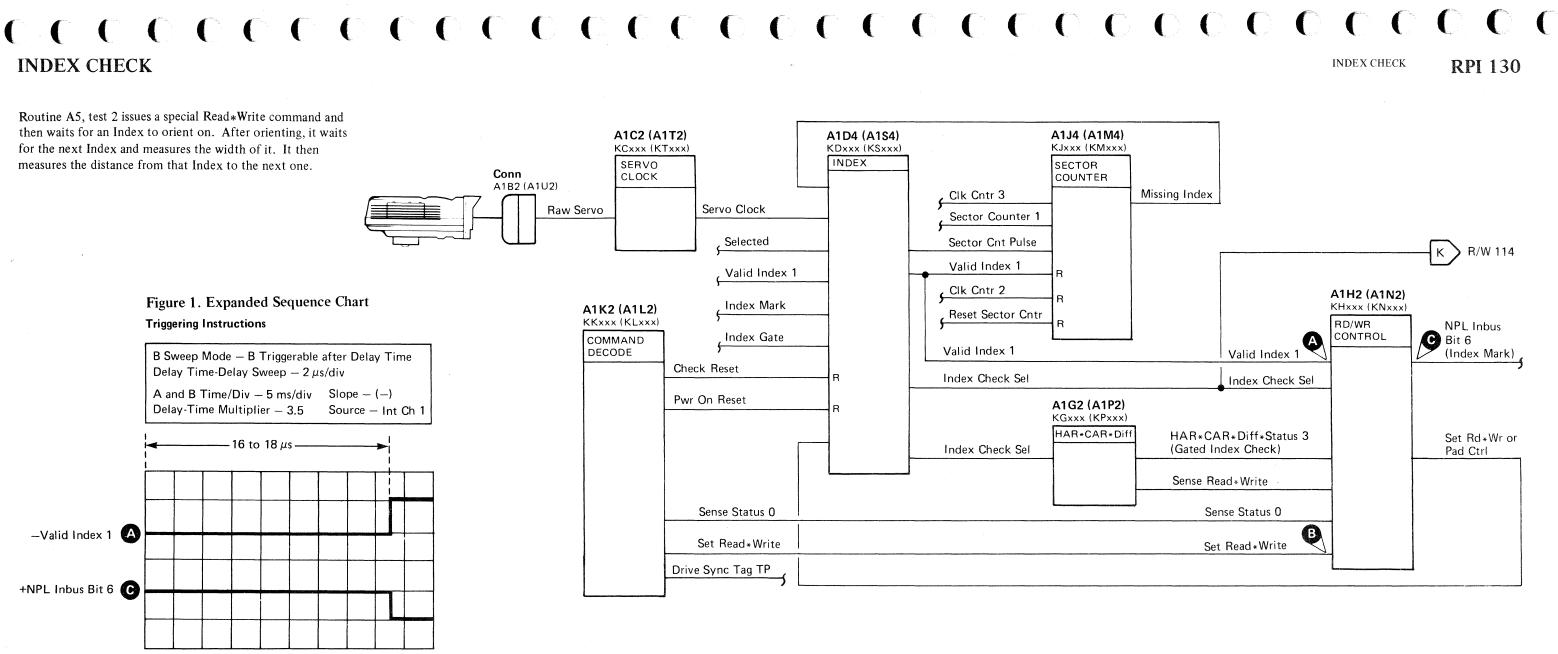


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3350	EE0120	2358302	441300	441303			
	Seq. 2 of 2	Part No.	31 Mar 76	30 Jul 76			 Í.
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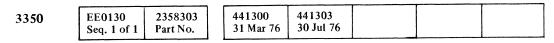
**RPI 125** 

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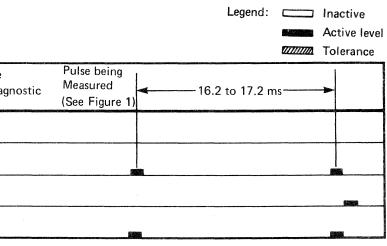


### Triggering Instructions

Irigger	ing instructions				
	p Mode – B Triggerable After I Time-Delay Sweep – 2 ms/div	,		pe — (—) ırce — Int Ch 1	
Chart Line No.	Line Name	ALD	Test Point		Orient Pulse for Microdiagr
1	—Drive Sync Tag TP	KK170 (KL170)	A1K2 (A1L2) P10		
2	–Valid Index 1	KH140 (KN140)	A1H2 (A1N2) S02	A	
3	+Set Read *Write	KH140 (KN140)	A1H2 (A1N2) S13	B	
4	+NPL Inbus Bit 6	KH200 (KN200)	A1H2 (A1N2) B02	G	

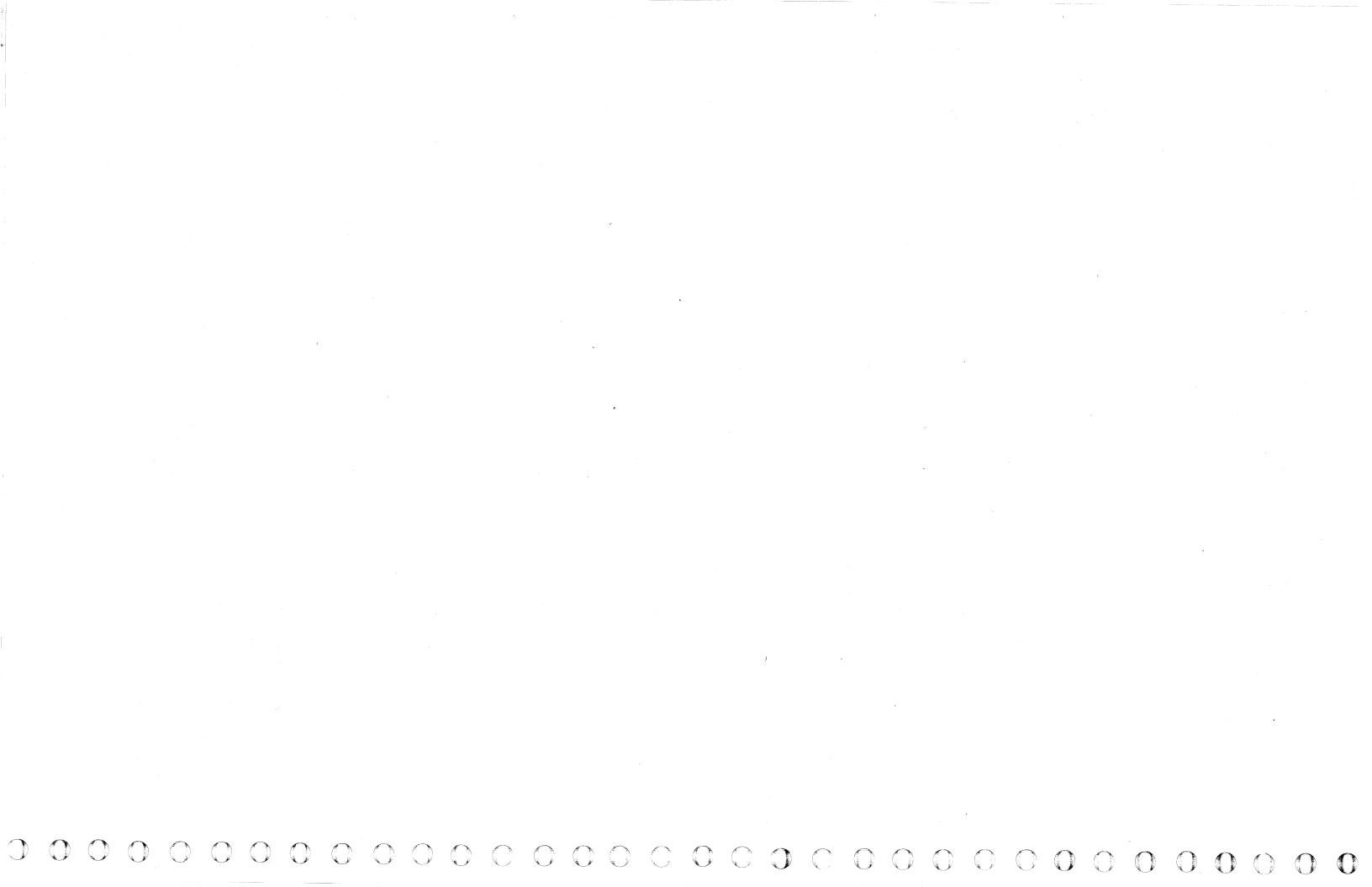


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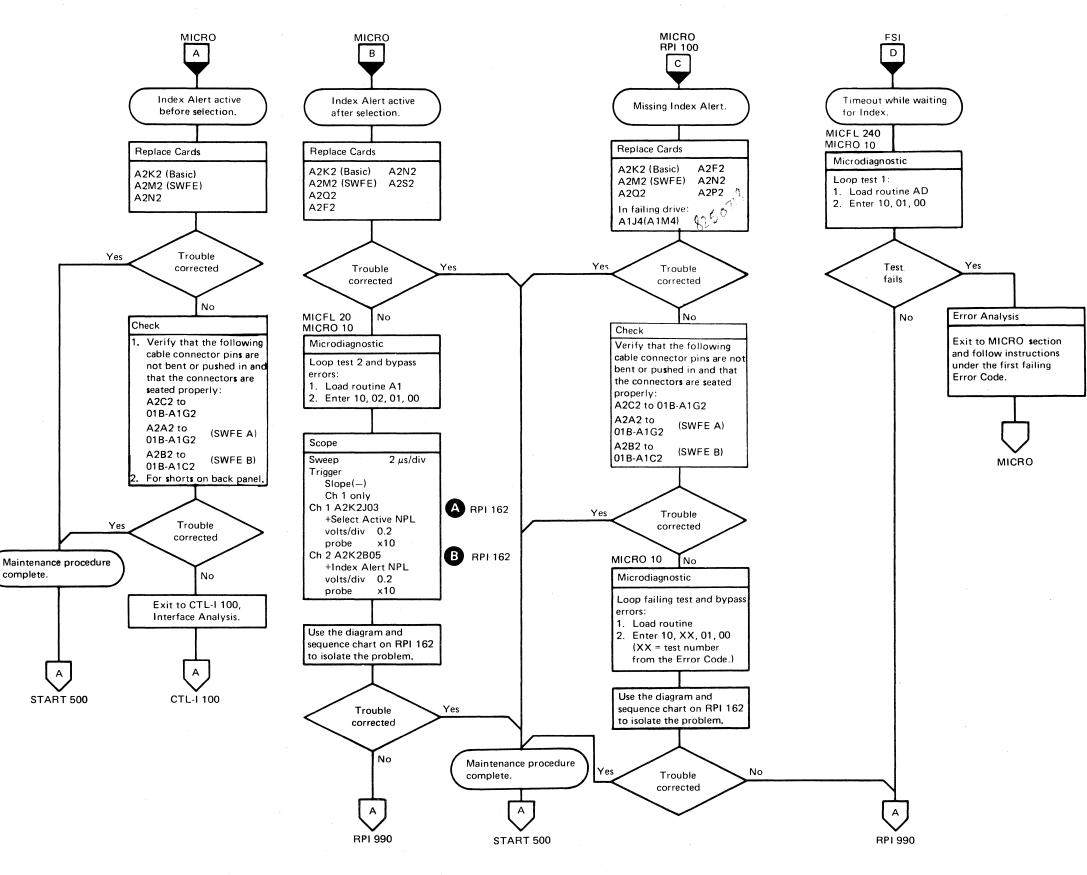
**RPI 130** 

INDEX CHECK



\*

## **INDEX ALERT ERROR**



3350	EE0160 Seq. 1 of 2	2358304 Part No.	441300 31 Mar 76	441303 30 Jul 76	441306 1 Apr 77		
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### INDEX ALERT ERROR

## **RPI 160**

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## **INDEX ALERT ERROR**

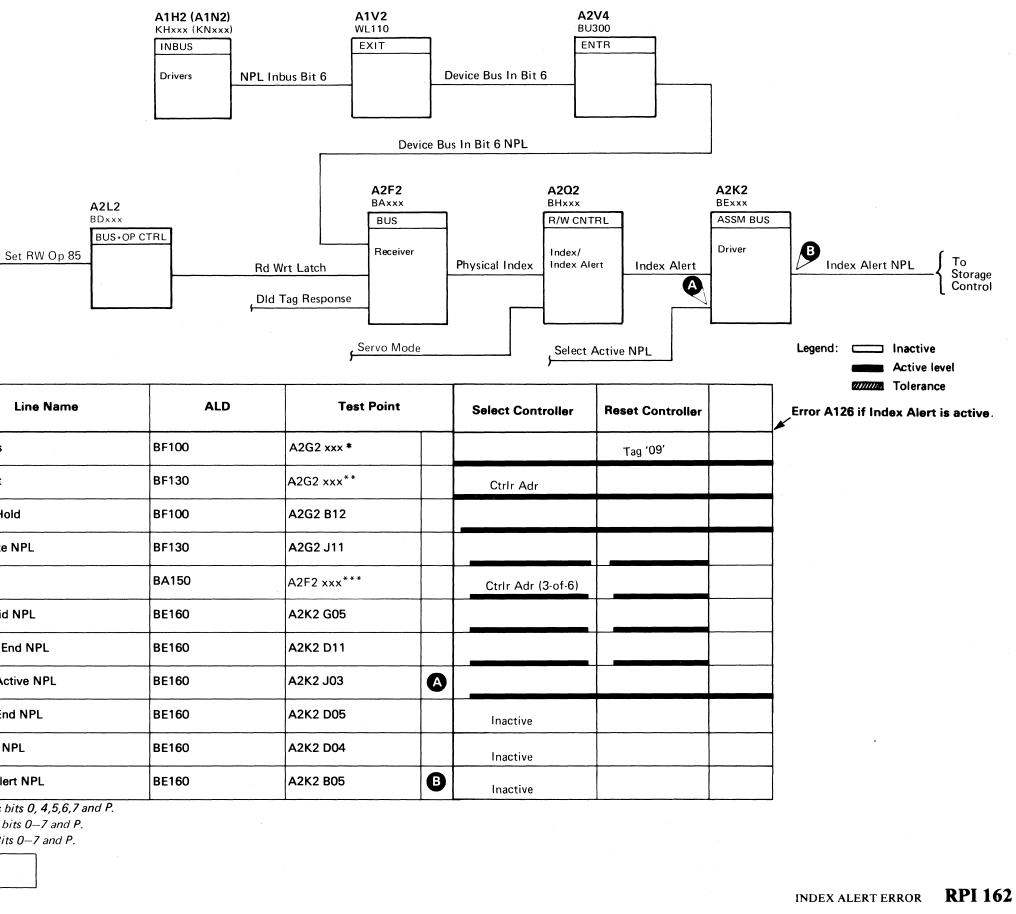


Chart Line No.	Line Name	ALD	Test Point		Select Controller	Reset Co	
1	+Tag Bus	BF100	A2G2 xxx *			Tag 'O	
2	+Bus Out	BF130	A2G2 xxx**		Ctrlr Adr		
3	+Select Hold	BF100	A2G2 B12				
4	+Tag Gate NPL	BF130	A2G2 J11				
5	+Bus In	BA150	A2F2 xxx***		Ctrlr Adr (3-of-6)		
6	+Tag Valid NPL	BE160	A2K2 G05				
7	+Normal End NPL	BE160	A2K2 D11				
8	+Select Active NPL	BE160	A2K2 J03				
9	+Check End NPL	BE160	A2K2 D05		Inactive		
10	+Sync In NPL	BE160	A2K2 D04		Inactive		
11	+Index Alert NPL	BE160	A2K2 B05	B	Inactive		

\*xxx = Tag Bus bits 0, 4,5,6,7 and P.

\*\*xxx = Bus Out bits 0-7 and P.

\*\*\* xxx = Bus In Bits 0-7 and P.

A2G2

BFxxx

BUS OUT

Op Decode

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## INDEX ALERT ERROR **RPI 162**

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## **INDEX ALERT ERROR**

#### Scope Setup

2 ms/div Sweep

Trigger

Slope (+) A2L2D13 +CE Alert Execute Ind

Ch 1/Ch 2 Use the diagram and sequence chart on this page.

#### Action

Use the diagram and sequence chart on this page to isolate the problem. The sequence chart shows microdiagnostic routine AD, test 1.

#### Microdiagnostic

Loop test 1 and bypass errors:

1. Load routine AD

2. Enter 10,01,01,00

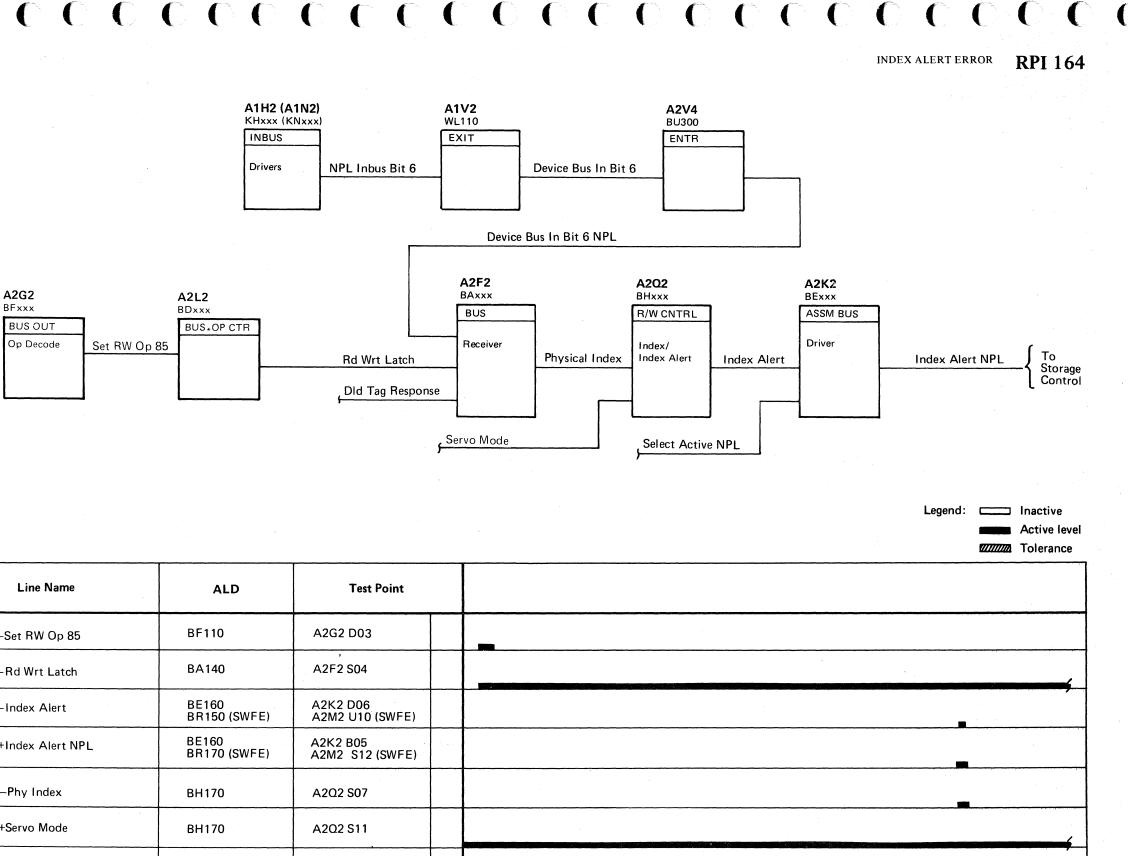


Chart Line No.	Line Name	ALD	Test Point	
1	–Set RW Op 85	BF110	A2G2 D03	
2	-Rd Wrt Latch	BA140	A2F2 S04	
3	–Index Alert	BE160 BR150 (SWFE)	A2K2 D06 A2M2 U10 (SWFE)	
4	+Index Alert NPL	BE160 BR170 (SWFE)	A2K2 B05 A2M2 S12 (SWFE)	
5	–Phy Index	BH170	A2Q2 S07	
6	+Servo Mode	BH170	A2Q2 S11	
7	-Bit Ring 3	BH170	A2Q2 M10	Pulses at Bit Ring Rate
8	-CT 63	BH170	A2Q2 P10	One CT 63 pulse each 220 $\mu$ s while Set RW Op

3350

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EE0164

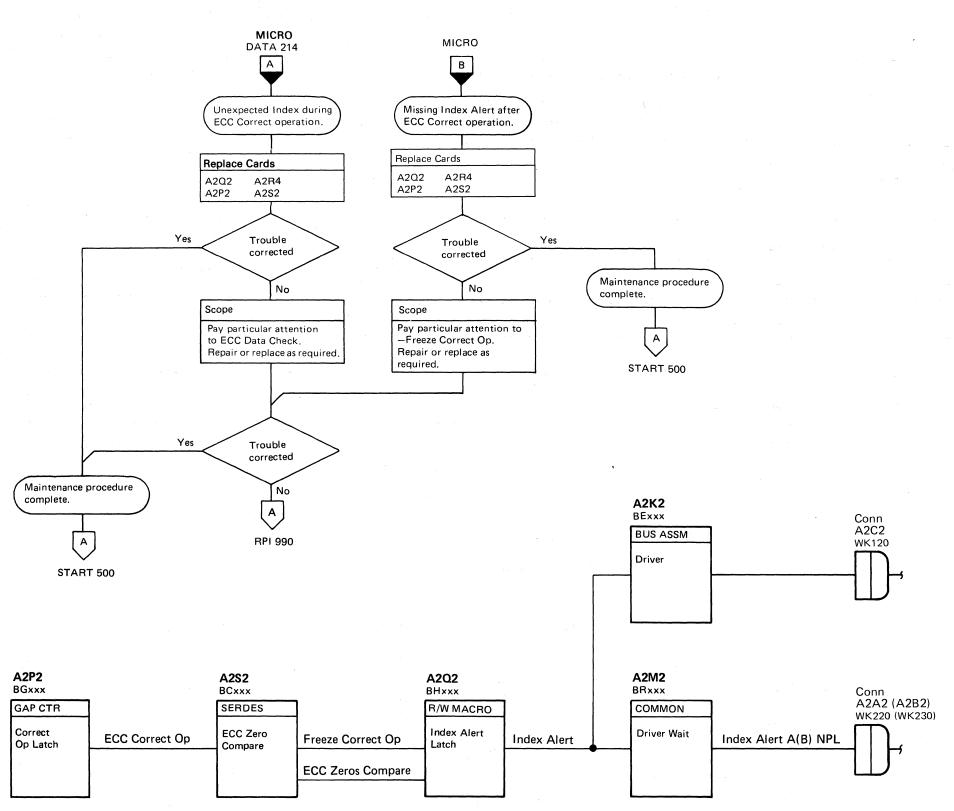
Seq. 1 of 2

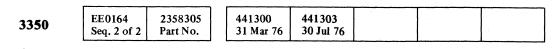
o 85 is active

## INDEX ALERT ERROR RPI 164

## **INDEX ALERT DURING CORRECT OPERATION**

After an ECC Data Check and during an ECC Correct operation, the controller ceases to transfer Index pulses from the device to storage control. Instead, when a correctable ECC pattern is found, as indicated by Freeze Correct Op, the controller generates an Index Alert signal to the storage control indicating that a pattern has been found. The ECC Shift Register then stops shifting and waits for the storage control to sense the pattern byte.





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INDEX ALERT DURING CORRECT OPERATION

**RPI 170** 

INDEX ALERT DURING CORRECT OPERATION

**RPI 170** 

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## **TRANSMIT TARGET ERROR**

#### SET TARGET - '8D'

Tag '8D' transfers the value on Bus Out to the Target Register of the selected drive for Rotational Position Sensing (RPS). The drive immediately begins a Search Sector operation to compare the Target Register with the Sector Counter until they compare equal.

#### **TRANSFER SECTOR COUNT**

Rotational Position Sensing (RPS) senses the angular position of a record on the disk and uses it to reduce rotational delay on subsequent operations.

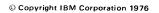
The drives contain a counter that counts the 128 sectors between Index Marks. When a G1 (Home Address) or a G3 (Count field) operation begins, the Transfer Sector Count line is activated in the controller and sent to the drive over Device Outbus bit 0. The drive uses bit 0 as a control to transfer the value in the Sector Counter into the Target Register. After the Read or Write operation is complete, the Target Register may be sensed and used for subsequent operations.

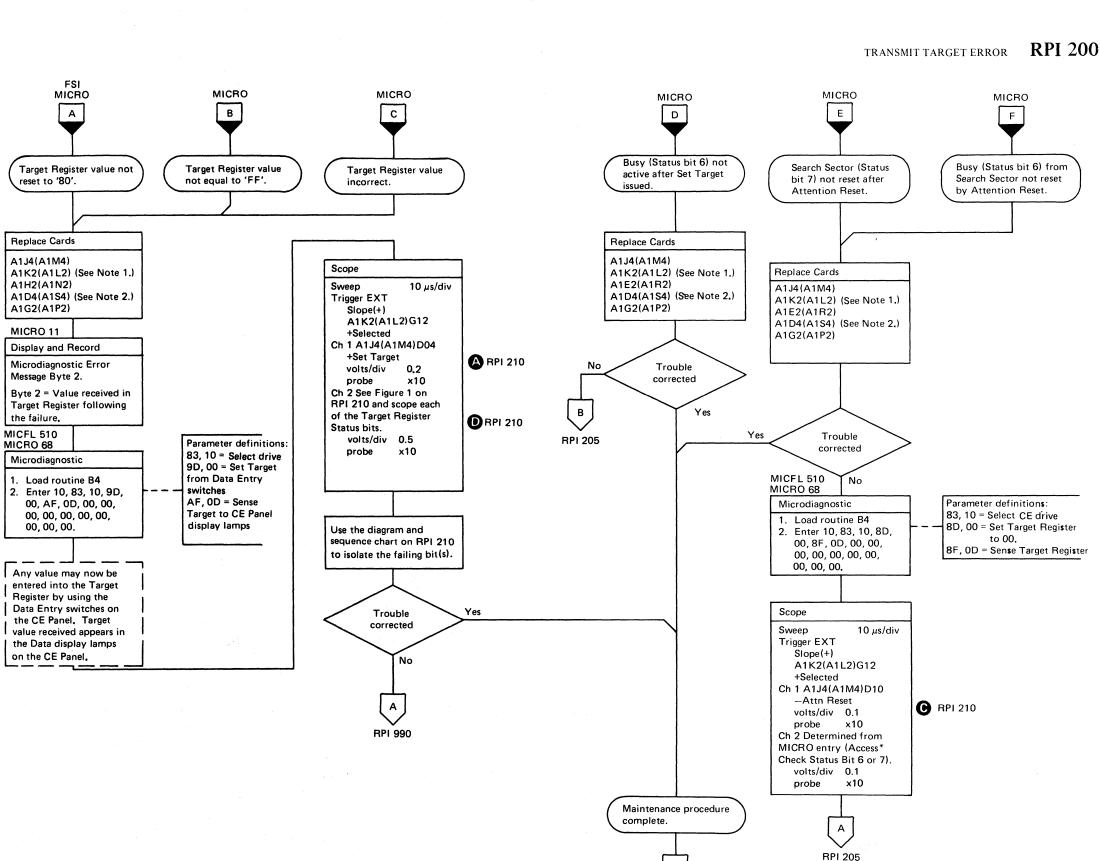
See OPER 203 through 205 for a more complete explanation of Rotational Position Sensing.

Note 1: When replacing A1K2(A1L2), check the addressing jumpers. See INST 6.

Note 2: When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800, Entry B for the procedure.

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3350	EE0200 Seq. 1 of 2	2358306 Part No.	441300 31 Mar 76	441303 30 Jul 76	441310 27 Jun 80		

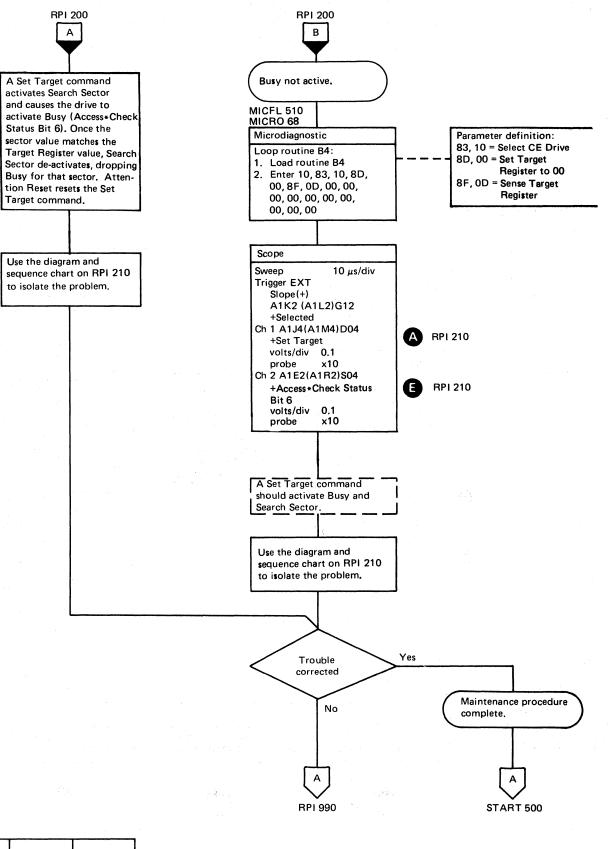




Α START 500

TRANSMIT TARGET ERROR RPI 200

## TRANSMIT TARGET ERROR



3350	EE0200 Seq. 2 of 2	2358306 Part No.	441300 31 Mar 76	441303 30 Jul 76	441310 27 Jun 80	
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#### TRANSMIT TARGET ERROR

**RPI 205** 

#### TRANSMIT TARGET ERROR

## TRANSMIT TARGET ERROR

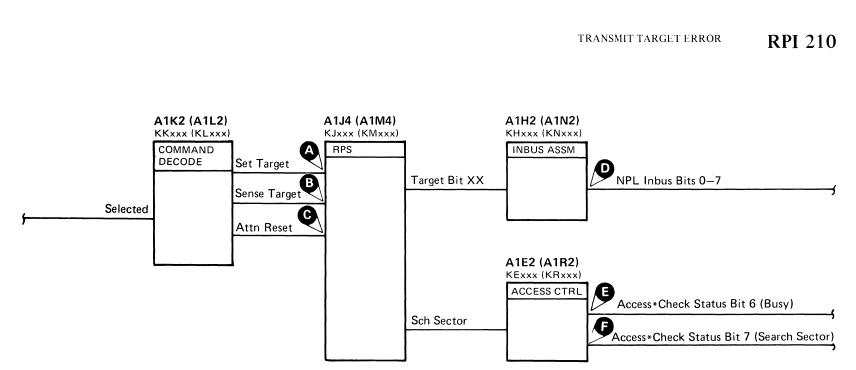
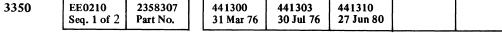


Figure 1. Target Register Status Bits

Bits 0	ALD KH200 (KN200)	Test Point A1H2 (A1N2) B05	Chart Line	Line Name	ALD	Test Point	T	Check for a Sense Targ
1	1	A1H2 (A1N2) D05	No.					
2 3		A1H2 (A1N2) B09 A1H2 (A1N2) D10	1	+Selected	KK140 (KL140)	A1K2 (A1L2) G12		
4		A1H2 (A1N2) D07 A1H2 (A1N2) D02	2	+Set Target	KJ530 (KM530)	A1J4 (A1M4) D04	•	
6 7	V	A1H2 (A1N2) B02 A1H2 (A1N2) D06	3	-Sense Target	KJ520 (KM520)	A1J4 (A1M4) B09	B	
			4	+Access*Check Status Bit 6	KE160 (KR160)	A1E2 (A1R2) S04	6	1
			5	+Access*Check Status Bit 7	KE160 (KR160)	A1E2 (A1R2) M13	G	
			6	–Attn Reset	KJ530 (KM530)	A1J4 (A1M4) D10	G	
			7	+NPL Inbus Bits 0–7	KH200 (KN200)	See Figure 1.	O	



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	Legend:	Inactive Active level Tolerance
r active Target Register bits during		
rget time.		
<u>م</u> ــــــــــــــــــــــــــــــــــــ		
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TRANSMIT TARGET ERROR

## **TRANSMIT TARGET ERROR**

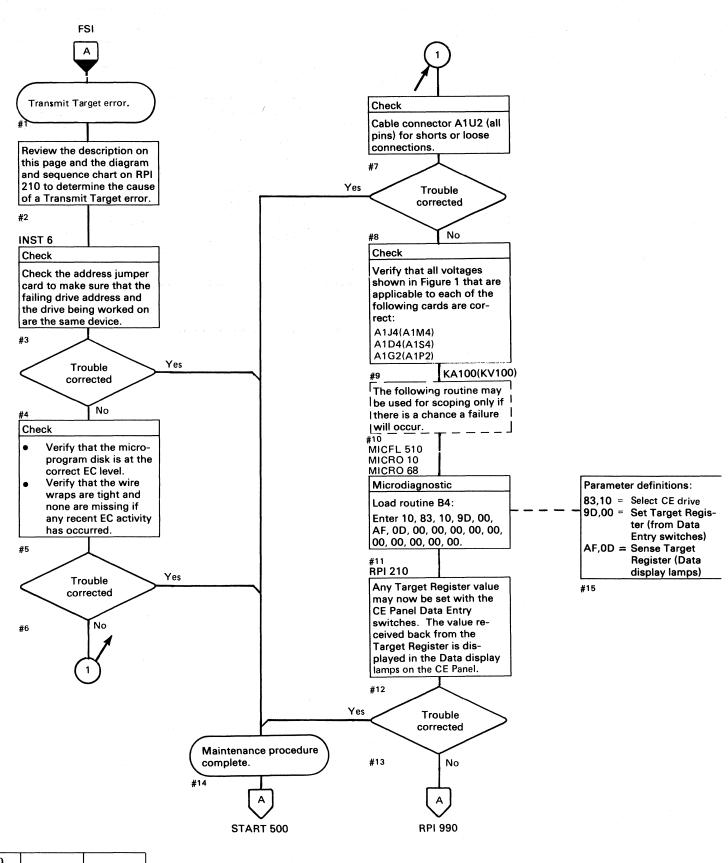
Target Status Bit 0 is always active when Sense Target command is issued.

The Set Target command sets the Target Register to the value of Bus Out. Power On Reset resets the register to '80'.

The Sense Target command puts the Target Register value on Bus In.

Transmit Target Register error indicates that the value received on Bus In when Sense Target command is issued does not equal the value set into the Target Register by the microprogram.

Device Busy is present (except during Sector Compare time) as long as the Search Sector latch is active. The latch is set by a Set Target command and reset by Attention Reset or Power On Reset.



3350	<b>EE0210</b> Seq. 2 of 2	2358307 Part No.		441300 31 Mar 76	441303 30 Jul 76	441310 27 Jun 80		
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#### TRANSMIT TARGET ERROR

**RPI 220** 

Figure 1. Voltage Check

Voltage	Test Point
-4 V	Use the ALD pages KA100
+6 V	(KV100) to determine applicable
+ 12 V	voltages and their test points.
—12 V	See PWR 290 for acceptable
–24 V	tolerances.

### TRANSMIT TARGET ERROR **RPI 220**

## **SEARCH SECTOR FAILURE**

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The Set Target command sets the value of Bus Out into the Target Register and starts a Search Sector operation. When the Sector Counter is equal to the value in the Target Register, a 124 to 136 microsecond Sector Compare pulse is generated. The Sector Compare pulse occurs at each revolution until an Attention Reset is issued.

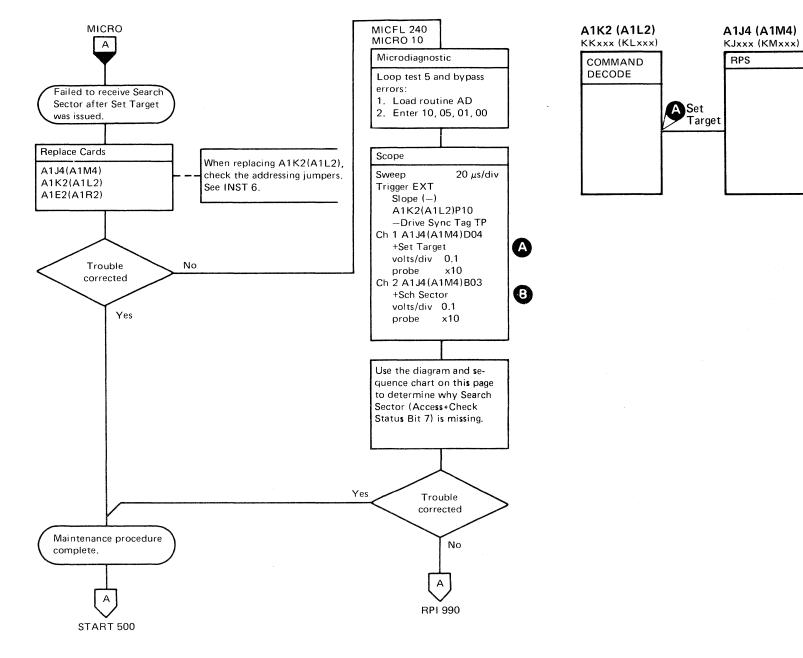
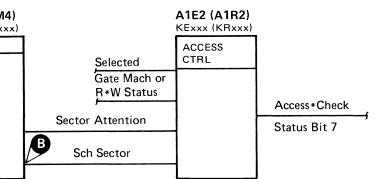


Chart Line No.	Line Name	ALD	Test Point		
1	+Set Target	KJ530 (KM530)	A1J4 (A1M4) D04	8	
2	+Sch Sector	KJ510 (KM510)	A1J4 (A1M4) B03	₿	

3350	EE0230 Seq. 1 of 1	2358308 Part No.	441300 31 Mar 76	441303 30 Jul 76		

#### SEARCH SECTOR FAILURE

**RPI 225** 



	Legend:	Inactive Active level Tolerance

#### SEARCH SECTOR FAILURE



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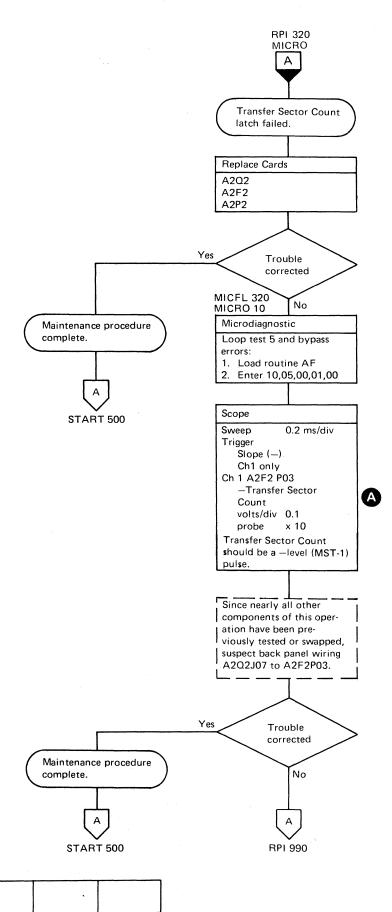
## **TRANSFER SECTOR COUNT LATCH FAILURE**

### **TRANSFER SECTOR COUNT**

Rotational Position Sensing (RPS) senses the angular position of a record on the disk and uses it to reduce rotational delay on subsequent operations.

The drives contain a counter that counts the 128 sectors between Index Marks. When a G1 (Home Address) or a G3 (Count field) operation begins, the Transfer Sector Count line is activated in the controller and sent to the drive over Device Outbus bit 0. The drive uses bit 0 as a control to transfer the value in the Sector Counter into the Target Register. After the Read or Write operation is complete, the Target Register may be sensed and used for subsequent operations.

See OPER 203 through 205 for a more complete explanation of Rotational Position Sensing.



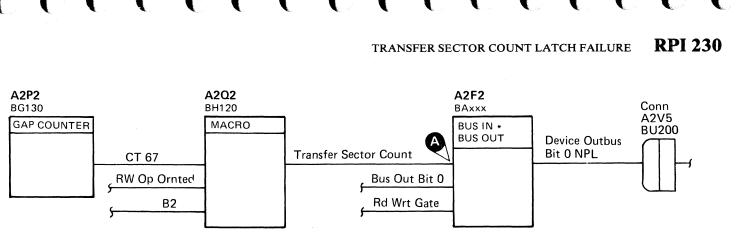


Chart Line No.	Line Name	ALD	
1	+ CT 67	BH120	A202 0
2	-Transfer Sector Count	BA140	A2F2 P
3	–Bus Out Bit 0	BA140	A2F2 N
4	– Rd Wrt Gate	BA140	A2F2 N

EE0300

Seq. 1 of 2

3350

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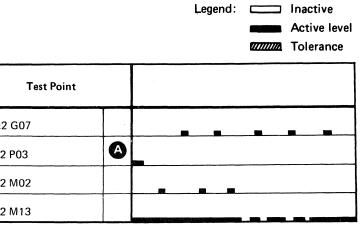
Part No.

441300

31 Mar 76

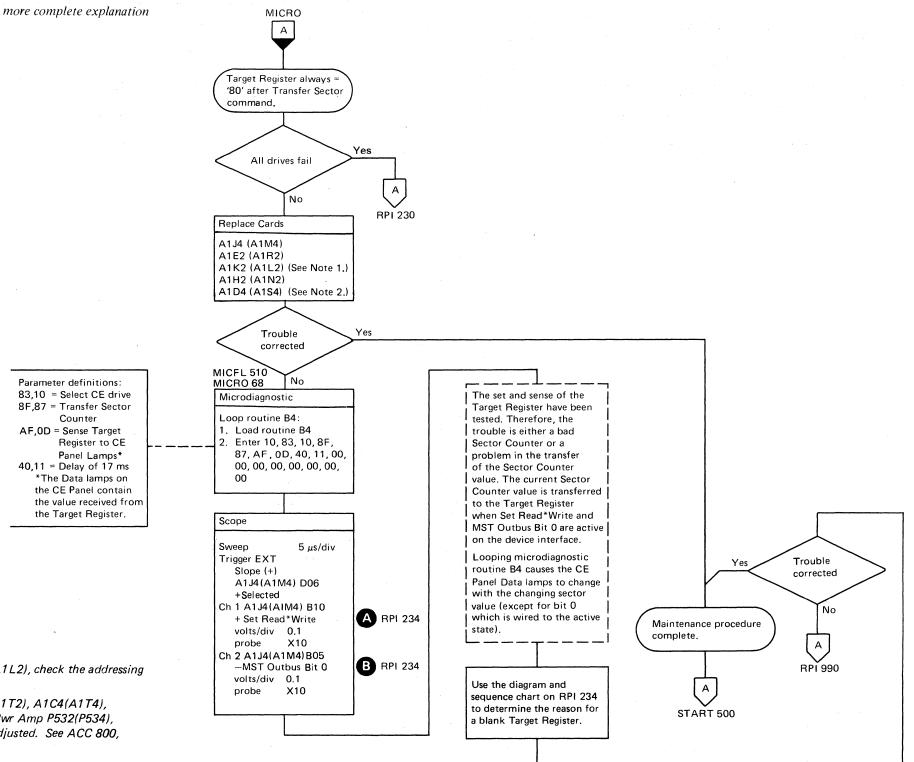
441303

30 Jul 76



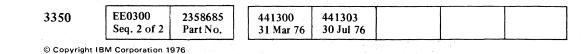
## TRANSFER SECTOR COUNT LATCH FAILURE

See OPER 203 through 205 for a more complete explanation of Rotational Position Sensing.



**Note 1:** When replacing A1K2(A1L2), check the addressing jumpers. See INST 6.

**Note 2:** When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800, Entry B for the procedure.



#### TRANSFER SECTOR COUNT LATCH FAILURE

**RPI 232** 

#### TRANSFER SECTOR COUNT LATCH FAILURE

**RPI 232** 

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## TRANSFER SECTOR COUNT LATCH FAILURE

The Sector Counter counts from 0 (at Index) to 127. The Sector Counter runs continuously while the drive is track following. Sector Count pulses are developed from the servo clock. The Sector Clock Counter (see OPER 204) accepts 39 sector count pulses before advancing the Sector Counter one count. After the Sector Counter reaches 127, the Valid Index 1 pulse resets the Sector Counter for the next revolution.

The Target Register performs two functions:

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- 1. It holds the starting sector location of the record to be read or written. The register is loaded at the beginning of all Read, Write, and Search CCWs by a Set Sector command. The sector number is retrieved from main storage.
- 2. It temporarily stores the beginning sector count transferred from the Sector Counter after a Write operation.

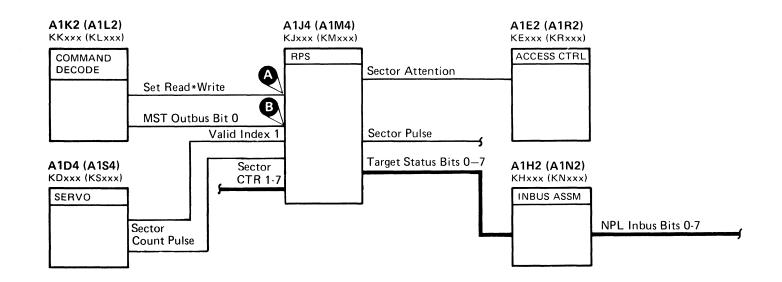
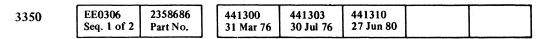


Chart Line No.	Line Name	ALD	Test Point		
1	+Selected	KJ520 (KM520)	A1J4 (A1M4) D06		· · · · · ·
2	+Set Read *Write	KJ510 (KM510)	A1J4 (A1M4) B10	A	
3	MST Outbus Bit 0	KJ510 (KM510)	A1J4 (A1M4) B05	B	
4	+Sector Pulse	KJ520 (KM520)	A1J4 (A1M4) B11		Check for the presence of pulses moving
5	-Sector Count Pulse	KJ520 (KM520)	A1J4 (A1M4) D05		across the scope face by changing the sweep time to 0.5 ms/div.
6	-Valid Index 1	KJ520 (KM520)	A1J4 (A1M4) D09		(Index is checked in an earlier routine.)





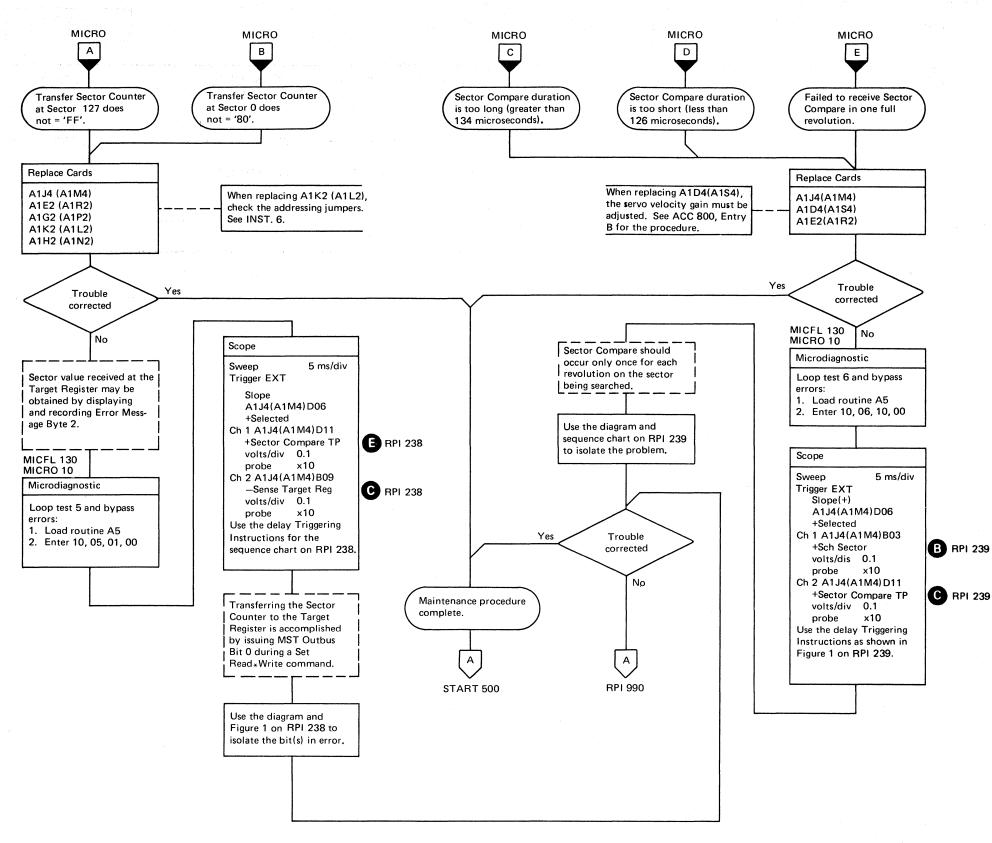
Legend:	Inactive Active level Tolerance
	 t.

## TRANSFER SECTOR COUNT LATCH FAILURE

Rotational Position Sensing (RPS) senses the angular position of a record on the disk and uses it to reduce rotational delay on subsequent operations.

The drives contain a counter that counts the 128 sectors between Index Marks. When a G1 (Home Address) or a G3 (Count field) operation begins, the Transfer Sector Count line is activated in the controller and sent to the drive over Device Outbus bit 0. The drive uses bit 0 as a control to transfer the value in the Sector Counter into the Target Register. After the Read or Write operation is complete, the Target Register may be sensed and used for subsequent operations.

See OPER 203 through 205 for a more complete explanation of Rotational Position Sensing.

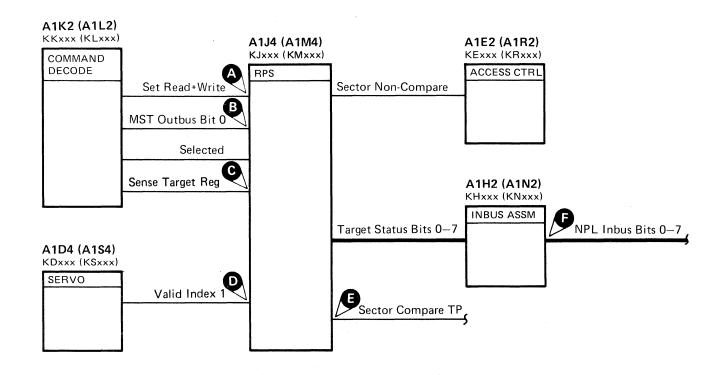


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1 <u>1</u> 1						

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### TRANSFER SECTOR COUNT LATCH FAILURE **RPI 236**

## TRANSFER SECTOR COUNT LATCH FAILURE



#### Figure 1. Target Register Status Bits

Figure 1. Target Reg	-	<b></b>	ering Instructions				<b>-</b>		Legend: Inactive
Bits         ALD           0         KH 200 (KN200)           1         I	A1H2 (A1N2) D05		eep Mode — B Triggerable After Ε Time-Delay Sweep — 50 μs/div			pe — (+) Irce — In			Active level
2 3 4 5	A1H2 (A1N2) B09 A1H2 (A1N2) D10 A1H2 (A1N2) D07 A1H2 (A1N2) D02	Chart Line No.	Line Name	ALD	Test Point		Transfer Sector 127	Transfer Sector 0	
5 6 7	A1H2 (A1N2) B02 A1H2 (A1N2) D06	1	+Selected	KJ520 (KM520)	A1J4 (A1M4) D06				
		2	+Sector Compare TP	KJ510 (KM510)	A1J4 (A1M4) D11	8			
		3	+Set Read*Write	KJ510 (KM510)	A1J4 (A1M4) B10	A			
		4	–MST Outbus Bit 0	KJ510 (KM510)	A1J4 (A1M4) B05	B		· · ·	
		5	-Sense Target Reg	KJ520 (KM520)	A1J4 (A1M4) B09	C			
		6	–Valid Index 1	KJ520 (KM520)	A1J4 (A1M4) D09	O			
		-> 7	+NPL Inbus Bits 0-7	KH200 (KN200)	See Figure 1.	G			

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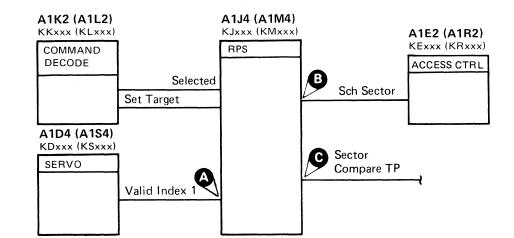


## TRANSFER SECTOR COUNT LATCH FAILURE

Rotational Position Sensing (RPS) senses the angular position of a record on the disk and uses it to reduce rotational delay on subsequent operations.

The drives contain a counter that counts the 128 sectors between Index Marks. When a GI (Home Address) or a G3 (Count field) operation begins, the Transfer Sector Count line is activated in the controller and sent to the drive over Device Outbus bit 0. The drive uses bit 0 as a control to transfer the value in the Sector Counter into the Target Register. After the Read or Write operation is complete, the Target Register may be sensed and used for subsequent operations

See OPER 203 through 205 for a more complete explanation of Rotational Position Sensing.



#### Figure 1. Expanded Sequence Chart

Triggering Instructions

	B Sweep Mode — B Triggerable After Delay Time Delay Time-Delay Sweep — 20 $\mu$ s/div	A and B Time/Div – 5 ms/div Delay-Time Multiplier – 4.0	Slope – (+) Source – Int Ch 1
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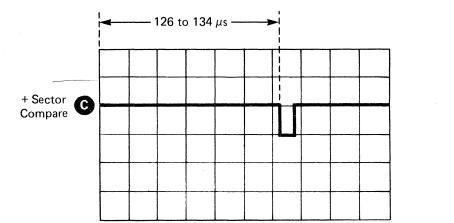


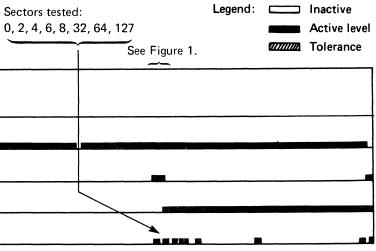
Chart Line No.	Line Name	ALD	Test Point		
1	+Selected	KJ520 (KM520)	A1J4 (A1M4) D06		
2	-Valid Index 1	KJ520 (KM520)	A1J4 (A1M4) D09	A	
3	+Sch Sector	KJ510 (KM510)	A1J4 (A1M4) B03	B	
4	+Sector Compare TP	KJ510 (KM510)	A1J4 (A1M4) D11	C	

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#### TRANSFER SECTOR COUNT LATCH FAILURE

**RPI 239** 



TRANSFER SECTOR COUNT LATCH FAILURE **RP** 



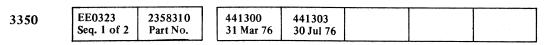
## SECTOR NON-COMPARE (Sector Compare Check)

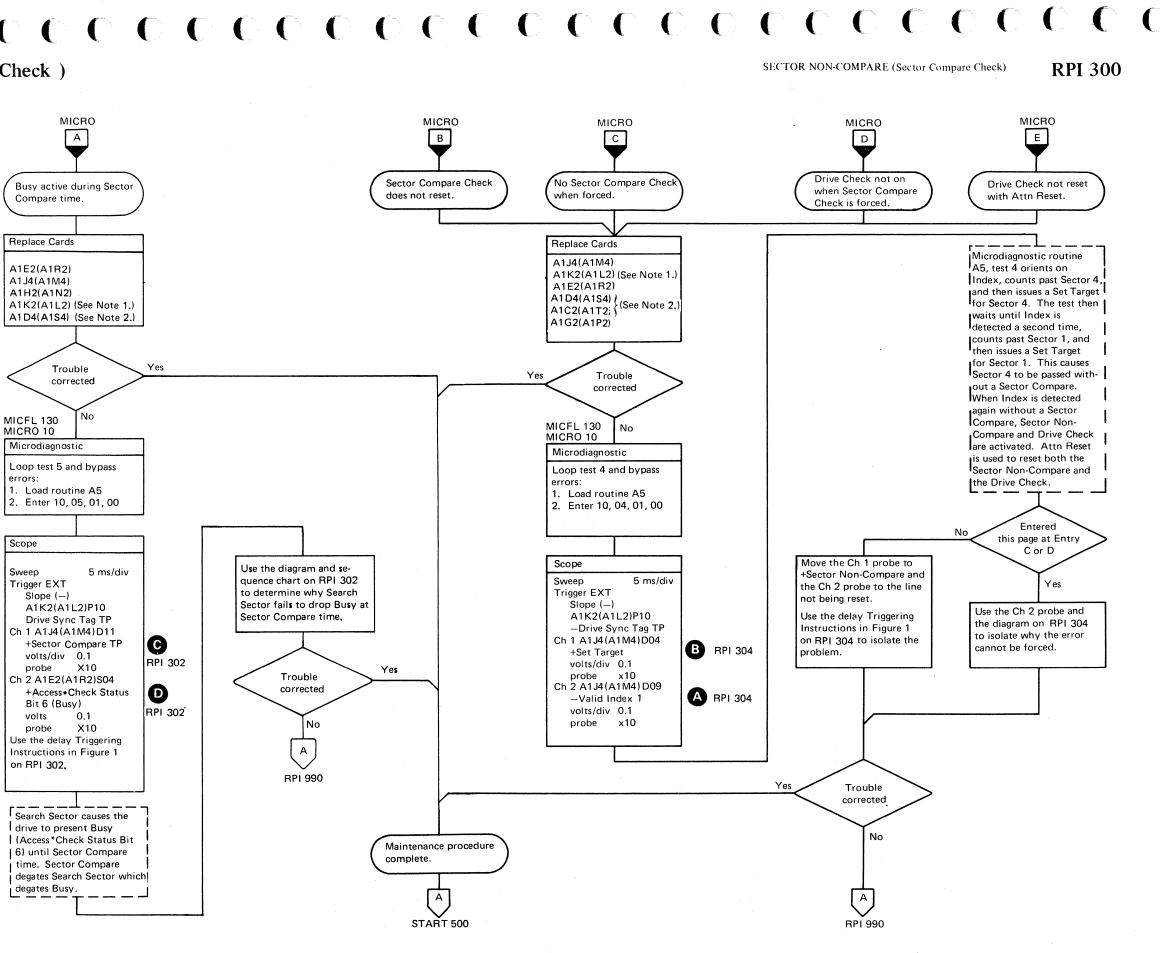
The Sector Non-Compare occurs as follows:

- 1. Set Target sets the Target Register and starts Search Sector.
- 2. At the first Valid Index (Index Mark), Sector Compare Check latch 1 is set. See ALD page KJ510(KM510).
- 3. At the fall of Index Mark, Sector Compare Check latch 2 is set.
- 4. If no Sector Compare occurs before the next Valid Index, Sector Compare Check latch 1 turns off.
- 5. Sector Compare Check latch 1 off and Sector Compare Check latch 2 on causes Sector Non-Compare.
- 6. Attention is set and remains on until Attention Reset or Check Reset is issued. Sector Compare Check is also indicated in Sense Status 1, bit 1.
- 7. Drive Check is turned on in Machine Status.

Note 1: When replacing A1K2(A1L2), check the addressing jumpers. See INST 6.

Note 2: When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800. Entry B for the procedure.

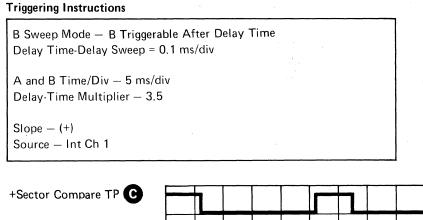




SECTOR NON-COMPARE (Sector Compare Check)

## SECTOR NON-COMPARE (Sector Compare Check)

## Figure 1. Expanded Sequence Chart



+Access\*Check Status Bit 6 (Busy) D

+Sch Sector

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П				
	-			

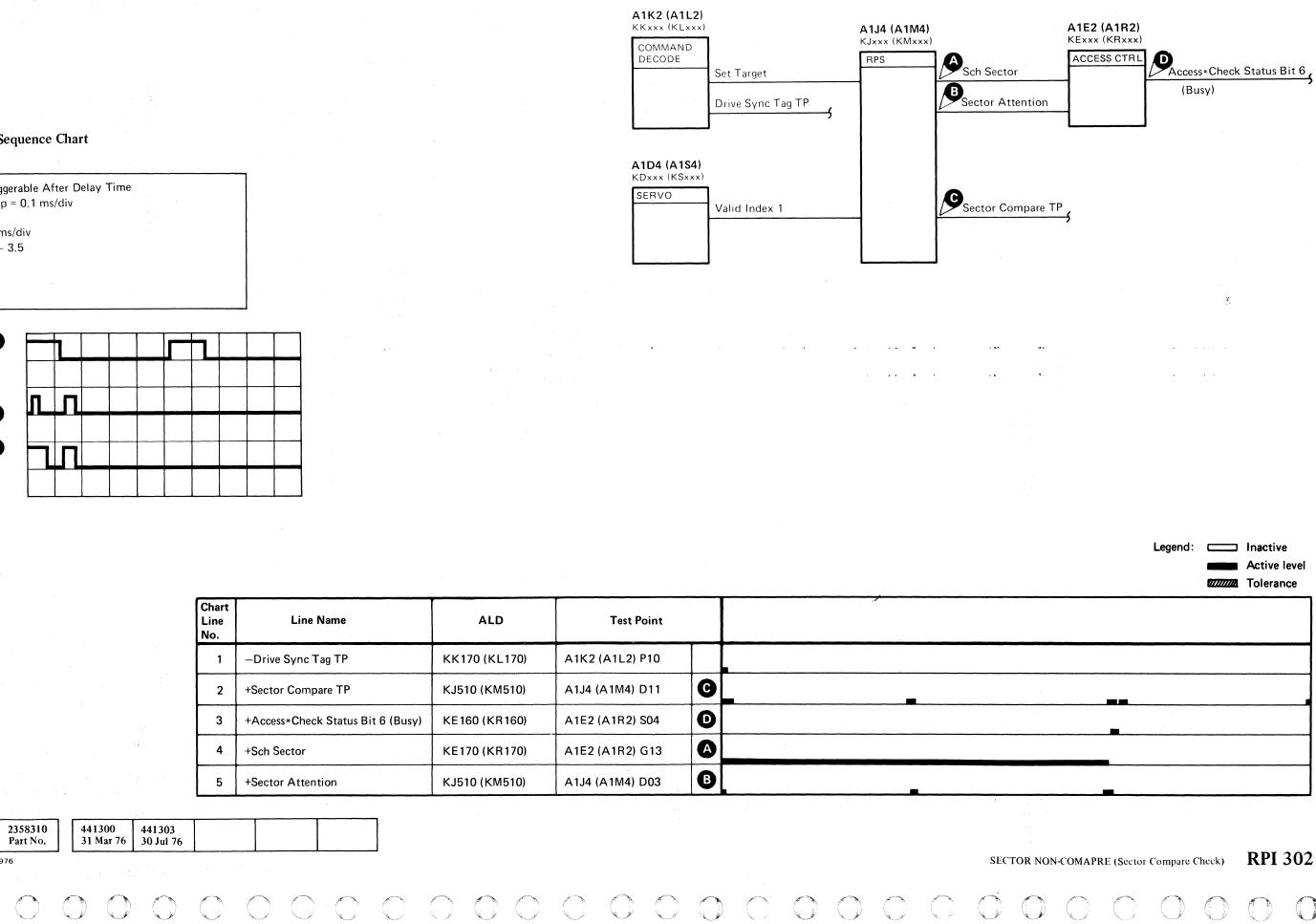
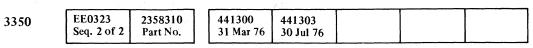


Chart Line No.	Line Name	ALD	Test Point		
1	-Drive Sync Tag TP	KK170 (KL170)	A1K2 (A1L2) P10		
2	+Sector Compare TP	KJ510 (KM510)	A1J4 (A1M4) D11	C	
3	+Access*Check Status Bit 6 (Busy)	KE160 (KR160)	A1E2 (A1R2) S04	O	
4	+Sch Sector	KE170 (KR170)	A1E2 (A1R2) G13	A	
5	+Sector Attention	KJ510 (KM510)	A1J4 (A1M4) D03	₿	



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#### SECTOR NON-COMPARE (Sector Compare Check)

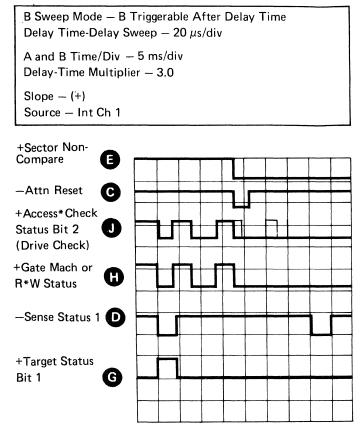
**RPI 302** 

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## SECTOR NON-COMPARE (Sector Compare Check)

#### Figure 1. Expanded Sequence Chart

#### **Triggering Instructions**



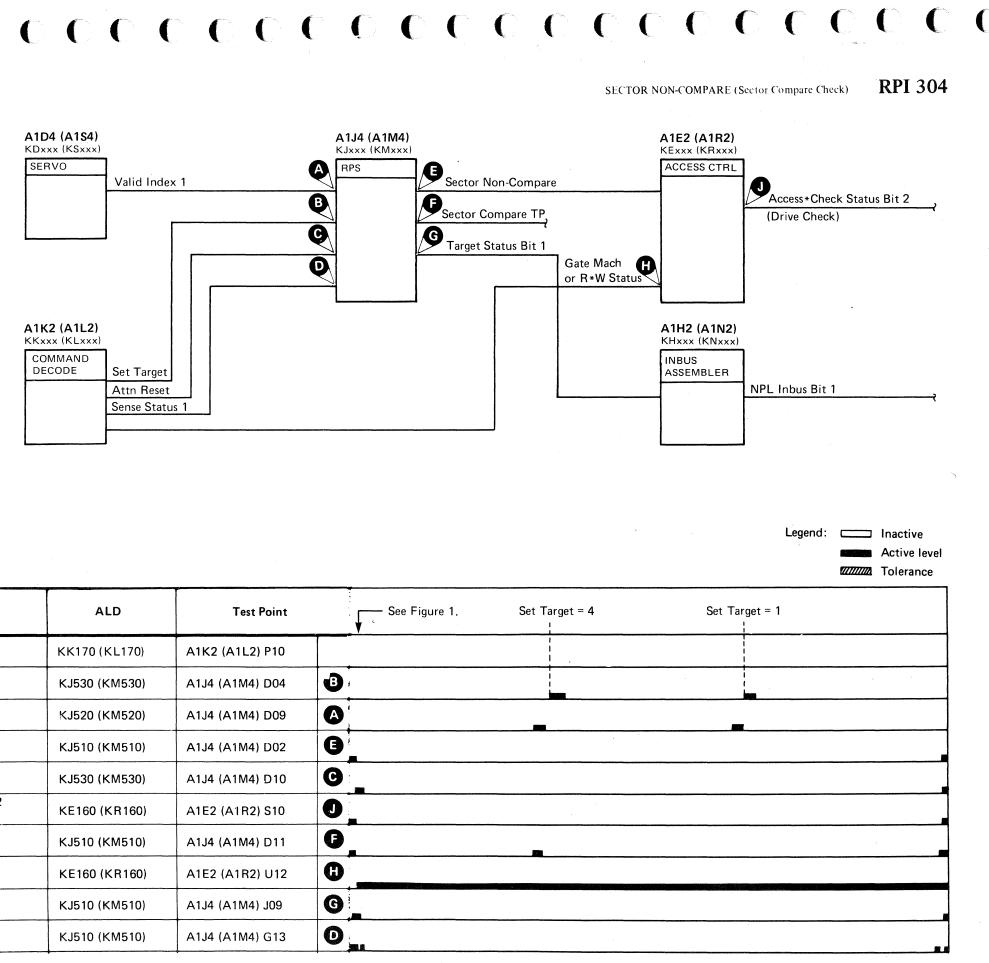


Chart Line No.	Line Name	ALD	Test Point	See Figure 1. Set Target =
1	—Drive Sync Tag TP	KK170 (KL170)	A1K2 (A1L2) P10	
2	+Set Target	KJ530 (KM530)	A1J4 (A1M4) D04	J.
3	-Valid Index 1	KJ520 (KM520)	A1J4 (A1M4) D09	
4	+Sector Non-Compare	KJ510 (KM510)	A1J4 (A1M4) D02	G
5	–Attn Reset	KJ530 (KM530)	A1J4 (A1M4) D10	0
6	+Access*Check Status Bit 2 (Drive Check)	KE160 (KR160)	A1E2 (A1R2) S10	0
7	+Sector Compare TP	KJ510 (KM510)	A1J4 (A1M4) D11	G
8	+Gat Mach or R*W Status	KE160 (KR160)	A1E2 (A1R2) U12	0
9	+Target Status Bit 1	KJ510 (KM510)	A1J4 (A1M4) J09	G
10	-Sense Status 1	KJ510 (KM510)	A1J4 (A1M4) G13	0

3350	EE0325 Seq. 1 of 1	2358311 Part No.	441300 31 Mar 76	441303 30 Jul 76		
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**RPI 304** SECTOR NON-COMPARE (Sector Compare Check)



## SECTOR NON-COMPARE (Sector Compare Check)

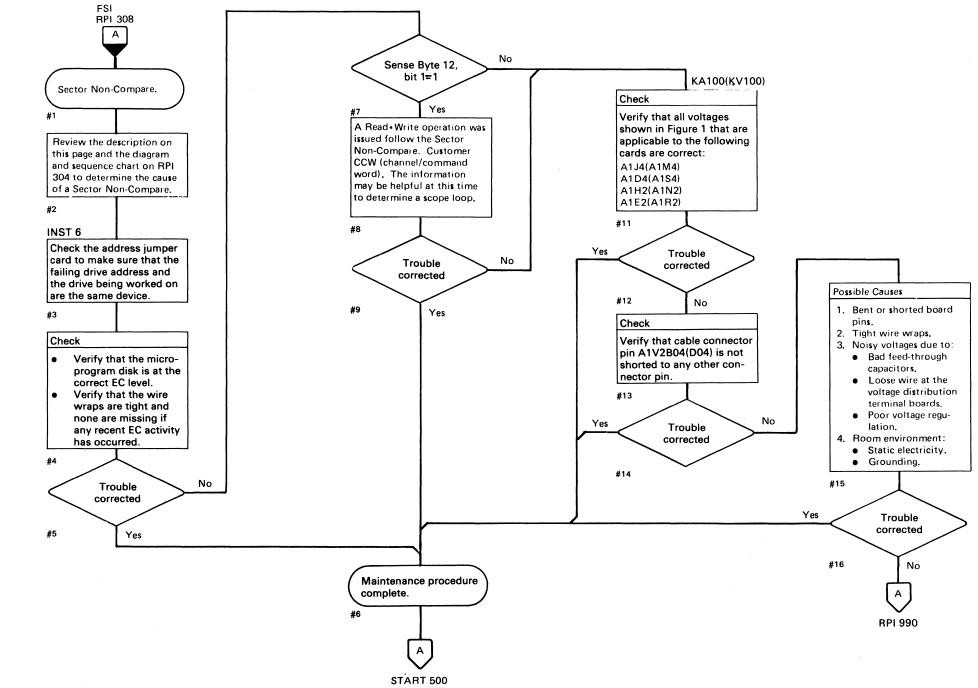
The Set Target command sets the value of Bus Out into the Target Register and starts a Search Sector operation. When the Sector Counter is equal to the value in the Target Register, a 124 to 136 microsecond Sector Compare pulse is generated. The Sector Compare pulse occurs at each revolution until an Attention Reset is issued.

Device Bus In bit 7 is active (except at Sector Compare time) while a Search Sector is in progress.

Device Bus In bit 6 is active except at Sector Compare time to indicate that the drive is busy.

Sector Non-Compare occurs if a Sector Compare is not found within two Index Marks. Sector Non-Compare activates Drive Check. The Sector Non-Compare occurs as follows:

- 1. Set Target sets the Target Register and starts Search Sector.
- 2. At the first Valid Index (Index Mark), Sector Compare Check latch 1 is set. See ALD page KJ510(KM510).
- 3. At the fall of Index Mark, Sector Compare Check latch 2 is set.
- 4. If no Sector Compare occurs before the next Valid Index, Sector Compare Check latch 1 turns off.
- Sector Compare Check latch 1 off and Sector Compare Check latch 2 on gives the condition for Sector Non-Compare.
- 6. Attention is set and remains on until Attention Reset or Check Reset is issued. Sector Compare Check is also indicated in Sense Status 1 bit 1.
- 7. Drive Check is turned on in Machine Status.



Bigs         EE0335         2358312         441300         441303         441310           3350         Seq. 1 of 2         Part No.         31 Mar 76         30 Jul 76         27 Jun 80	
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**RPI 306** 

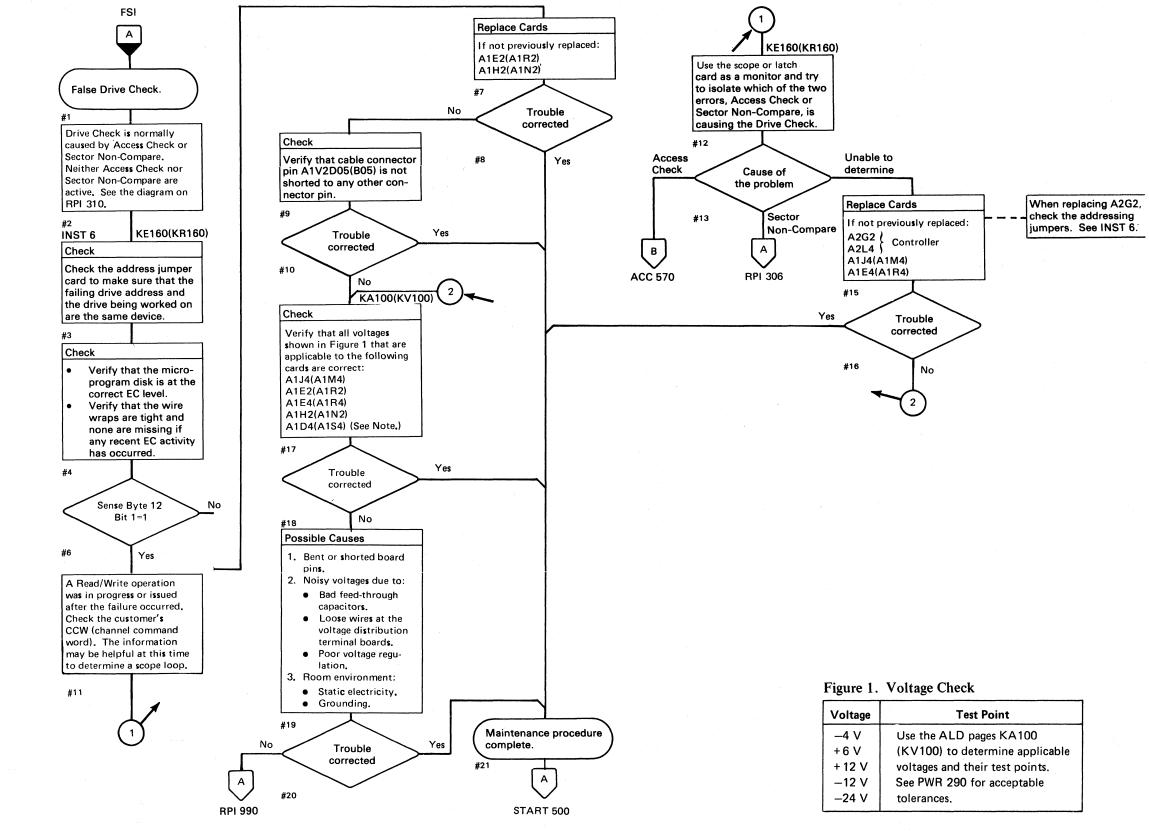
Figure	1.	Voltage	Check
--------	----	---------	-------

Voltage	Test Point
-4 V	Use the ALD pages KA100
+6 V	(KV100) to determine applicable
+ 12 V	voltages and their test points.
—12 V	See PWR 290 for acceptable
-24 V	tolerances.

**RPI 306** 

SECTOR NON-COMPARE (Sector Compare Check)

## **FALSE DRIVE CHECK**



Note: When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800, Entry B for the procedure.

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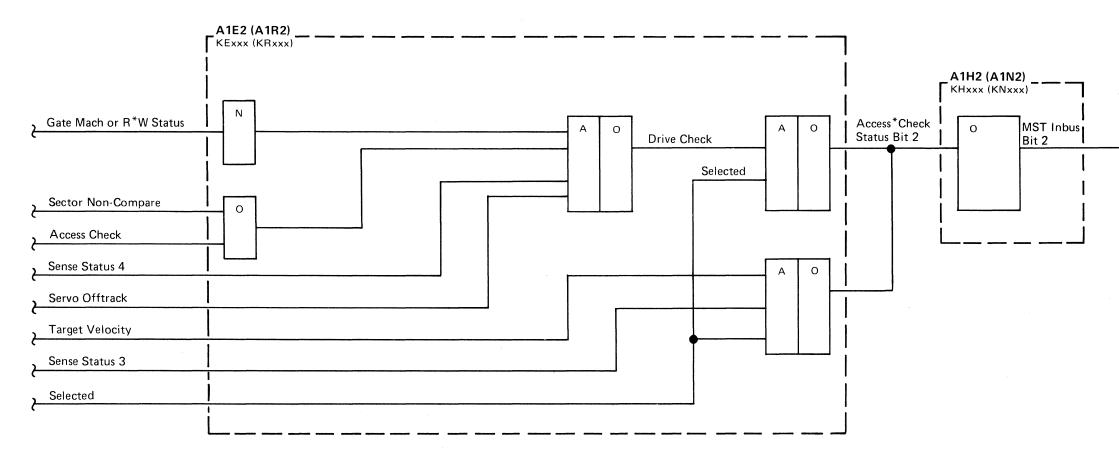
#### FALSE DRIVE CHECK **RPI 308**

Voltage	Test Point				
-4 V	Use the ALD pages KA100				
+6 V	(KV100) to determine applicable				
+ 12 V	voltages and their test points.				
-12 V	See PWR 290 for acceptable				
–24 V	tolerances.				

## FALSE DRIVE CHECK RPI 308

## **FALSE DRIVE CHECK**

Use this diagram for reference only.



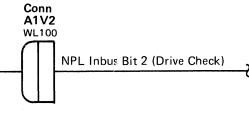
ę.

3350         EE0340         2358313           Seq. 1 of 1         Part No.	441300         441303           31 Mar 76         30 Jul 76	
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## FALSE DRIVE CHECK **RPI 310**



## **TROUBLE NOT FOUND**

This page contains aids for problem resolution where insufficent error information is available to follow the maintenance analysis procedure. It may also be used as an aid in analyzing intermittent errors.

## А

#### **CHECK DEVICE ADDRESS**

Check EREP printouts to determine if more than one device is failing.

#### CHECK MICRODIAGNOSTIC DISK

If the microdiagnostic failed, verify that the microdiagnostic disk used is the proper level for the device that failed.

## EC INSTALLATION

If an engineering change has been recently installed, check the EC installation instructions and determine where the change was made.

Inspect the back panel for tight wire wraps.

#### **DRIVE MOTOR**

Drive motor speed is incorrect. Check the following:

• Drive-motor belt (see HDA 760).

- Drive-motor pulley loose or faulty (see HDA 760).
- Drive-motor brake (see HDA 720).
- Drive motor faulty (see HDA 715 for replacement procedure).

### CABLE

Check for a loose or defective cable at:

A1B2 (A1U2)
A1Y3 (A1Y4)
01C (01D) A1A2
01C (01D) A1A3
A1A2
A1A3
A1V2
A1V3

#### **VOLTAGE CHECKS**

Incorrect Power Supply voltage.

Controller A2 Module – PWR 90 C2 Module – PWR 390 Drive

A2, B2, or C2 Modules – PWR 290

Seq. 1 of 1 Tattio. Stimat 70 S0 Jul 70	3350	EE0990 Seq. 1 of 1	2358314 Part No.	441300 31 Mar 76	441 303 30 Jul 76			
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### HDA

Use the HDA Cable Swap Procedure (HDA 713) to isolate the problems to the HDA. See HDA 710 for HDA replacement procedure.

#### SUMMARY OF CARDS

Reseat or replace:

A1E2(A1R2)A1D4(A1S4)\* A1G2(A1P2) A1C2(A1T2)\* A1H2(A1N2) A1K2(A1L2)\*\* A1J4(A1M4)

\*When replacing A1C2(A1T2), A1C4(A1T4), A1D2(A1S2), A1D4(A1S4), or Pwr Amp P532(P534), the servo velocity gain must be adjusted. See ACC 800, Entry B for the procedure.

\*\* When replacing A1K2(A1L2), check the addressing jumpers. See INST 6.

#### REFERENCES

Index theory on RPI 102 and OPER 126. Transmit Target theory on OPER 205 and 206.

## TROUBLE NOT FOUND **RPI 990**

## TROUBLE NOT FOUND RPI 990



# **PWR CONTENTS**

# 3350 WITHOUT C2 MODULE ATTACHED

## Controller

## SEQUENCING

Description						PWR 6
. Diagram						
Sequence Cha						

#### POWER SUPPLY FAILURE

Power Supply Failure Analysis			PWR 9
Power Supply Failure Analysis			PWR 10
AC Circuit Failure Analysis			<b>PWR 20</b>
AC Circuit Diagram			<b>PWR</b> 21
AC Circuit Failure Analysis	•		<b>PWR 22</b>
+24 Volt Bootstrap Failure Analysis			PWR 30
+24 Volt Bootstrap Diagram			PWR 31
+24 Volt Bootstrap Failure Analysis	•		<b>PWR 32</b>
+24 Volt Bootstrap Failure Analysis			<b>PWR 33</b>
-4 Volt Failure Analysis			<b>PWR 55</b>
—4 Volt and +6 Volt Regulator			
Diagram		•	<b>PWR 56</b>
+6 Volt Failure Analysis	•	•	PWR 60
FIX VERIFICATION AND VOLTAGE			
CHECKS			PWR 90
COMPONENT AND TEST POINT			
LOCATIONS	•	•	PWR 91

LOCATIONS	•	•	•	•	•	•	•	•	•	•	•	•

# Drive

### SEQUENCING

Analysis for A2 Module .						PWR 101
Diagram	•	•		•	•	PWR 111, 112
Analysis for B2 Module .		•				PWR 116, 117
AC Circuit Failure Analysis						
AC Circuit Diagram	•		•	•		PWR 121

## 3350 WITH C2 MODULE ATTACHED (ALTERNATE CONTROLLER)

### Controller

## SEQUENCING

Description .	, <b>.</b>		•		•	•	PWR 306
Diagram		•					PWR 307
Sequence Chart							PWR 308

## POWER SUPPLY FAILURE

Power Supply Failure Analysis	PWR 309
Power Supply Failure Analysis	PWR 310
AC Circuit Failure Analysis	PWR 320
AC Circuit Diagram	PWR 321
AC Circuit Failure Analysis	PWR 322
+24 Volt Bootstrap Failure Analysis	PWR 330
+24 Volt Bootstrap Diagram	PWR 331
+24 Volt Bootstrap Failure Analysis	PWR 332
+24 Volt Bootstrap Failure Analysis	PWR 333
–4 Volt Failure Analysis	PWR 355
–4 Volt and +6 Volt Regulator	
Diagram	PWR 356
+6 Volt Failure Analysis	PWR 360

#### FIX VERIFICATION AND VOLTAGE

### COMPONENT AND TEST POINT

LOCATIONS .	•	•	•	•	•	•	•	•	•	•	PWR 391
-------------	---	---	---	---	---	---	---	---	---	---	---------

# Drive

# SEQUENCING

Analysis for A2 Module .		•	•	PWR 401
Power Sequencing Analysis				
for A2 or C2 Module		•		PWR 402
Diagram				PWR 411, 412
Analysis for B2 Module .				PWR 415
Analysis for C2 Module .				PWR 416, 417
AC Circuit Failure Analysis				PWR 420
AC Circuit Diagram				PWR 421

# 3350 B2 MODULE

### POWER SUPPLY FAILURE

-12 Volt and +12 Volt Failure Analysis	•	PWR 240
-12 Volt and +12 Volt Diagram		PWR 241
-24 Volt Failure Analysis		PWR 250
-24 Volt Supply Diagram		PWR 251
-4 Volt Failure Analysis		PWR 255
-4 Volt Supply Diagram		PWR 256
+6 Volt Failure Analysis		PWR 260
+6 Volt Regulator Diagram		PWR 261
+24 Volt (Local) Failure Analysis		PWR 270
+24 Volt (Local) Supply Diagram		PWR 271
+24 Volt (Local) Failure Analysis		PWR 272
-36 Volt Failure Analysis		PWR 280
-36 Volt Supply Diagram		PWR 281

### FIX VERIFICATION AND VOLTAGE

11/1 / 10/14/		 			-	•••			_			
CHECKS	•	•	•	•	•	•	•	•	•	•	•	PWR 290

## COMPONENT AND TEST POINT

	 	 	-	 		
LOCATIONS			•			<b>PWR</b> 291

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# **PWR CONTENTS**

PWR<sup>1</sup>

(

#### PWR CONTENTS

PWR 1

# **POWER SUPPLY SEQUENCE**

# INTRODUCTION

Power for the entire disk storage string is routed through the A2 (control) Module. The ac power (three phase, 208 V, 60 Hz) is controlled by the sequencing circuits in the A2 Module.

Line filtering is accomplished by a capacitor between each phase of the 208 Vac connected at the output of CB200. A phase-detection circuit containing resistance, capacitance, and an ac relay (K202) is used to detect improper power phasing; this is done to ensure proper rotation of the blower and drive motors. Relay K202 picks only if the main ac phasing is correct. If phasing is incorrect, K202 fails to pick and the power-on sequence is prevented.

With three-phase power to the 3350 string, T201 is activated. The secondaries feed the convenience outlets (115 V) and the +24 V Bootstrap (BS) supply. The bootstrap voltage picks sequence and control relays in all modules. The convenience outlets are energized if the EPO control from the Storage Control is active to pick the EPO relay (K203).

There are two separate power supplies; a controller supply and a drive supply. The controller supply consists of a +24 V power sequence, a 115 Vac convenience outlet, and a -4 V and +6 V supply (T420) for the A2 logic board. The drive power supply for every module consists of two separate supplies (T531 and T532) that provide power for the A1 logic board, the servo power amplifiers, and the +24 V Local for relay operation.

Power-on sequencing begins with the controller and continues with the following steps:

- 1. Controller power-on is initiated by the using storage control or with a local Power On switch.
- DC power for the logic in each module is made active next, beginning with the A2 logic board in the A2 Module and stepping to the A1 logic board and servo amplifiers, then continuing to the end of the module string. The B2 Modules do not contain A2 logic boards.
- 3. With dc power on in all modules and all drive Start/ Stop switches in the Start position, Drive A in the A2 Module starts first, followed by Drive B. Drive A of the next (adjacent) module then starts, followed by Drive B. This stepping continues with Drive B in the last (end) module starting last. Refer to HDA 500 for details of drive motor start sequencing.

With the Power Off/Enable switch in the Enable position, a power-on sequence is initiated by the Power On switch if in Local mode, or by power pick, and power hold relays in the storage control if in Remote mode. AC power is provided to the controller power transformer and the blower motor through the Subsystem (String) Power contactor (K201). With the dc power supply transformer active, output from the -4 V and +6 V Regulators is available. A 6 V Sense relay (K602) is picked by the +6 V Regulator to indicate that the controller has powered on.

The dc power for drives is available when the AC Power Drives contactor (K331) is picked. K331 is picked from the controller when the 6 V Sense relay is picked. The Power Sequence Delay relay (K611) picks one second after K331 is picked and from the same source of voltage. The points of K611 enable +24 V Power Sequence (Out) to pick the K331 and K611 in the next module. Monitor points of K611 turn on the Power Sequence Complete indicator (LED).

# **POWER-ON SEQUENCE**

## Controller

- Three-phase power is supplied from the customer's power receptacle to activate the +24 V Bootstrap Supply and the 115 Vac outlets 1. K202 (Phase Rotation Detection) 2 picks if the phase is correct.
- 2. With the Power Off/Enable switch in the Enable position
  3 , the storage control pick relay or Power On
  9 switch picks K601 (Subsystem Sequence Start)
  4 if CPs are not tripped and the Logic Gate Thermal is not open.
- 3. The K601 points pick K201 (Subsystem Power) and the Power On lamp 5 comes on.
- 4. The blower motor comes on **6**.
- 5. The ferroresonant transformer (T420) 7 with its associated rectifiers and filters provide bulk dc voltages to the -4 V and +6 V Regulators.
- 6. K602 (6 V Sense) 8 is picked by the +6 V Regulator.
  +24 V Sense, -4 V Regulator, and the +6 V Bulk are required to activate the +6 V Regulator.
- Points of K602 supply the +24 V Bootstrap Sequence line and the +24 V Power Sequence line to power-on the string 23.
- 8. The controller power-on sequence is now complete except for picking the String Power Sequence Complete relay (K603) 10 by the Power Sequence Complete line. This line is activated through a jumper (T4 to T3)
  22 in the last module of the string when its Power Sequence Delay relay (K611) is picked. K603 signals the controlling storage control to advance to the next subsystem string. If the Service Bypass switch 14 of any module is on, K611 does not need to be picked for string power sequencing.

#### Drives

The drive power section components, labels, and numbers of each module are identical. This means that K351 19 is the drive motor contactor for Drive A whether it is located in an A2 or B2 Module. There are two exceptions, however. The first is that the blower 6 in the A2 Module receives power when contactor K201 is picked while contactor K331 a activates the blower 17 in the B2 Module. The second exception is the application of the series of auxiliary CP points 15 and 16 that pick K331. Both exceptions result because blowers must be turned on when power is applied to the logic boards. The drive power-on sequence for each module is:

- The +24 V Power Sequence line picks the AC Power Drives contactor (K331) 18 through the Off position of the Service Bypass switch and through the CP auxiliary point and Logic Gate Thermal points.
- Contactor K331 activates the dc power supplies and starts the blower motor in the B2 Module. Threephase power is also available to the drive motor contactors (K351 and K361) 19.
- DC power from the supplies is distributed to the drive logic panel 24 through CPs, the +6 V Regulator, and the Drive DC Power switch 21. The three-position Drive DC Power switch permits removal of DC power to one drive while the other continues to operate.
- 4. The Power Sequence Delay relay (K611) **1** picks one second after K331 is picked and from the same source of voltage. With K611 picked, the Power Sequence Complete (LED) **12** is turned on and +24 V Power Sequence is sent to the next module.

In the next module, drive power sequencing begins by picking K331 and K611. In the last module of the string, a jumper between T4 and T3 22 routes the +24 V Power Sequence Complete line to pick the String Power Sequence Complete relay (K603) 10. The K603 points signal the storage control to advance to the next subsystem string. Other points of K603 provide +24 V Drive Sequence and +24 V Poll lines 25 that with the +24 V Bootstrap line, start and stop the spindle drive motors.

With the Service Bypass switch in the On position, the Power Sequence Complete (LED) is on and the other drives remain active. The drives section of this module is not sequenced on (K331 dropped 13). K611 10 remains picked, but K612 (+6 V Sense) cannot pick; therefore the Power Check (LED) is on through K612-1 N/C 20.

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# **POWER-OFF SEQUENCE**

### Controller

- The Subsystem Power contactor (K201) drops all ac power to the string when the circuit to the Subsystem Sequence Start relay (K601) 4 opens. The hold circuit to K601 is through auxiliary points of CP420 and CP421, CP311 Aux, the Logic Gate Thermal, the power hold relay points of control storage, and the Power Off/Enable switch 3.
- 2. With K201 dropped, power is removed from the drive motors, blowers, and power supplies in all modules of the string.
- Circuits that remain active after the hold to K601 is lost are the Phase Rotation Detection relay 2, the +24 V Bootstrap Supply, and the convenience outlets if the EPO voltage remains on.

#### Drives

When the drives section of an A2 or B2 Module loses power because of a tripped CP, other modules of the string remain on.

 If contactor K331 18 is dropped, all power is removed from the dc power supplies and both drive motors in an A2 or B2 Module. In an A2 Module, K311 is held activated through CPs 531-536 auxiliary points 15, and the Service Bypass switch.

In a B2 Module, contactor K331 is held activated through the points of the Logic Gate Thermal, CP311 auxiliary points **16**, and the Service Bypass switch. CP311 monitors the auxiliary points of CPs 531-536. When an auxiliary point in the series opens, the increased current trips CP311 which opens its auxiliary points to drop K331.

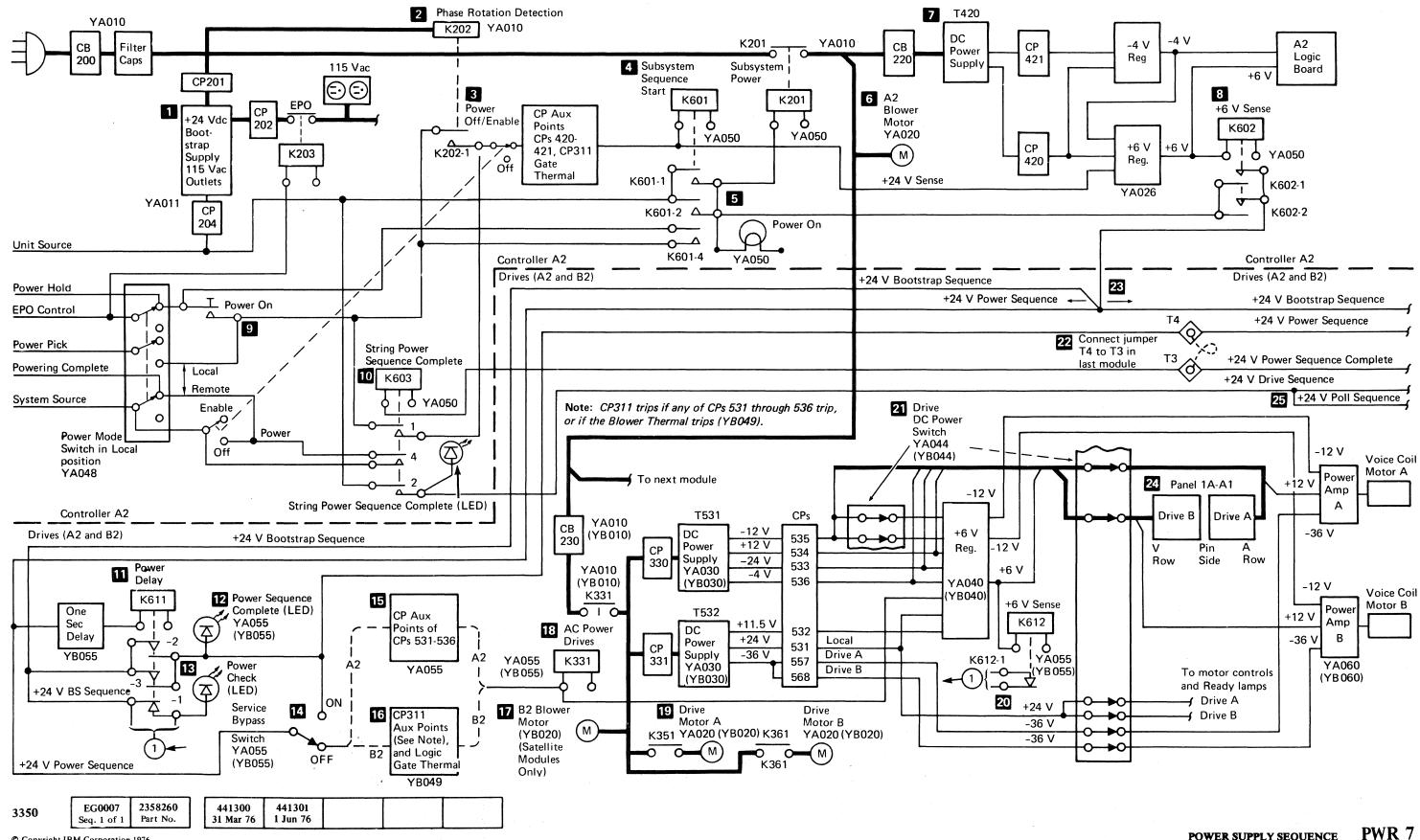
- With K331 dropped in an A2 or B2 Module, other modules of the string remain on because the Power Sequence Delay relay (K611) 11 is still picked to send +24 V Power Sequence to the next module. The Power Sequence Complete (LED) 12 is still on even though the drives are inactive.
- The Power Check (LED) 13 is also turned on when K331 is dropped because there is no +6 V Regulator output to pick the 6 V Sense relay (K612). The normally closed points of K612-1 20 complete the Power Check (LED) circuit.

POWER SUPPLY SEQUENCE

PWR 6

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# **POWER SUPPLY SEQUENCE**



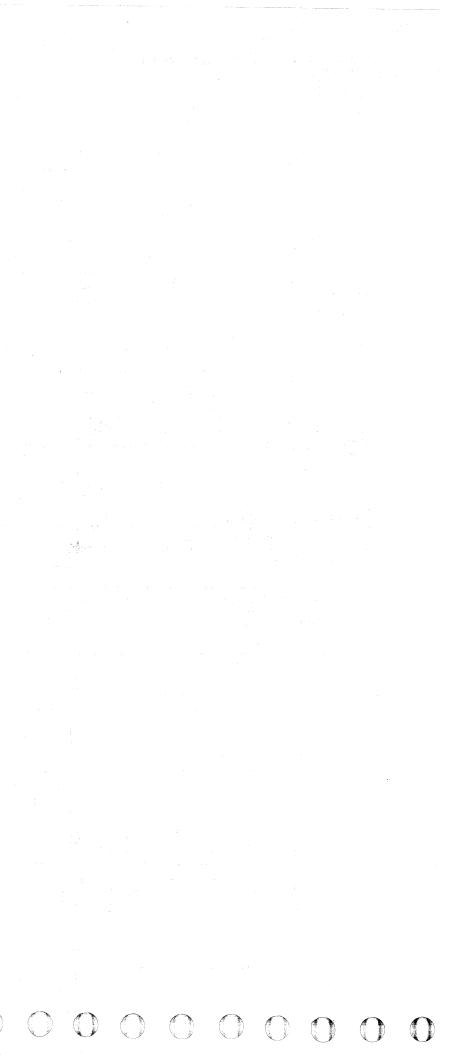
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#### POWER SUPPLY SEQUENCE

PWR 7

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#### POWER SUPPLY SEQUENCE



OW	ER ON SEQUENCE								POWER ON SEC	QUENCE <b>PWF</b>
				-	Sequence Panel, Board A Sequence Panel, Board B					
art ne	Line Name	ALD	Test Point		Press Power On Cor	ntroller DC On Drive D	Drive Drive	1	(B2) vance to next string	
	Controller and Drive Power in A2 M	Nodule						1		
1	K202 Phase Rotation	YA010								
2	K601 Subsystem Sequence Start	YA050	TP9	A	1					
3	Power On Lamp	YA050	TP5	A	2					
4	K201 Subsystem Pwr On	YA050	TP5	A	2					
5	A2 Blower Mtr On	YA020			4					
6	K602 +6 V Sense	YA050	TP8	A		4				
7	Power Check (LED)	YA055				6,9,10				
8	K331 AC Pwr Drives	YA055	TP9	B		6				
9	K611 Pwr Seq Delay	YA055	T4 (Jumper terminal)	B		<b> </b>	s f one	second	d delay	
0	K612 +6 V Sense Drive	YA055	TP7	B			8			
1	Power Seq Comp (LED)	YA055					9			
	Drive Power in B2 Module	••••••••••••••••••••••••••••••••••••••	-							
2	Power Check (LED)	YB055					9,14,16 /////			
3	K331 AC Pwr Drives	YB055	ТР9	B			9			
4	K611 Pwr Seq Delay	YB055	T4 (Jumper terminal)	₿	Repeat lines 12		<b>◄</b> _\$ <b>/</b> \$		9 one second delay	
5	B2 Blower Mtr On	YB020			B2 Module of the string	g.	12			
16	K612 +6 V Sense Drive	YB055	TP7	B				12		
17	Pwr Seq Complete (LED)	YB055			J			1	14	
	Setup to Start Spindles			-11-	······································				· · · · · · · · · · · · · · · · · · ·	
8	K603 String Power Seq Complete	YA050	TP10	<b>A</b>					14	
9	K631 Allow Start	YA055 (YB055)	TP1	B					18 (in all modules)	
20	K632 Start Drives	YA055	TP17	B					19 (in A2 Module first)	

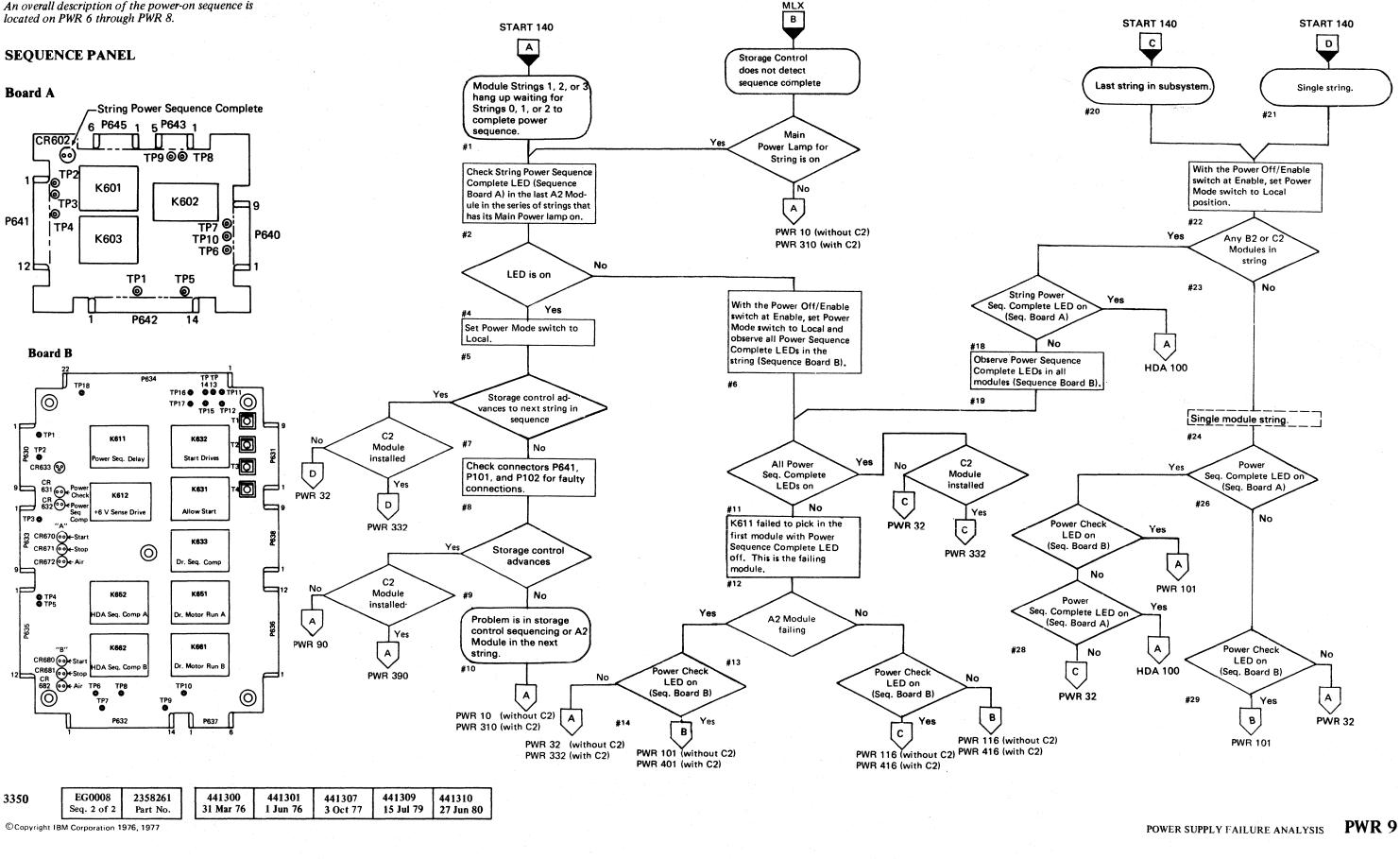
3350	EG0008	<b>2358261</b>	441300	441301	441307	441309	441310
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# **POWER SUPPLY FAILURE ANALYSIS**

An overall description of the power-on sequence is located on PWR 6 through PWR 8.

# **SEQUENCE PANEL**



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#### POWER SUPPLY FAILURE ANALYSIS

PWR 9

 $\bigcirc$ 

# C

# **POWER SUPPLY FAILURE ANALYSIS**

DANGER	
LETHAL VOLTAGES are present in the power servicing	
area. SAFETY cannot be overemphasized. Consider	
ALL CIRCUITS LIVE until measured otherwise.	
CAPACITORS are potentially explosive devices.	
WEAR SAFETY GLASSES. After replacing any capacitor,	
reinstall all SAFETY COVERS before powering on machine.	

An overall description of the power-on sequence is located on PWR 6 through PWR 8.

See PWR 91 and LOC pages for component locations.

See ZA100 for relay terminal numbering.

#### Component

Numbers	Located In		
2xx	Controller AC Compartment		
Зхх	Drive AC Compartment		
4xx	Controller DC Compartment		
5xx	Drive DC Compartment		
6xx	Sequence Panel		

# **SEQUENCE PANEL**

## **Board B**

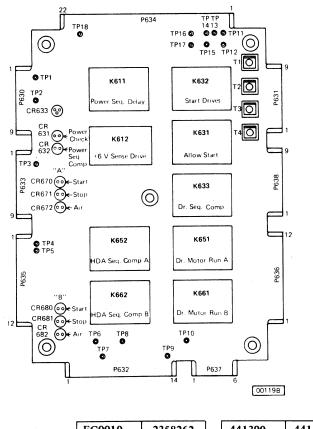


Figure 1.

CP or CB

CB200

CP201

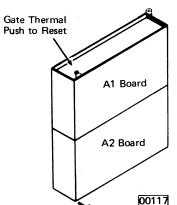
CP204

CP421

CP420

inch.

inch.

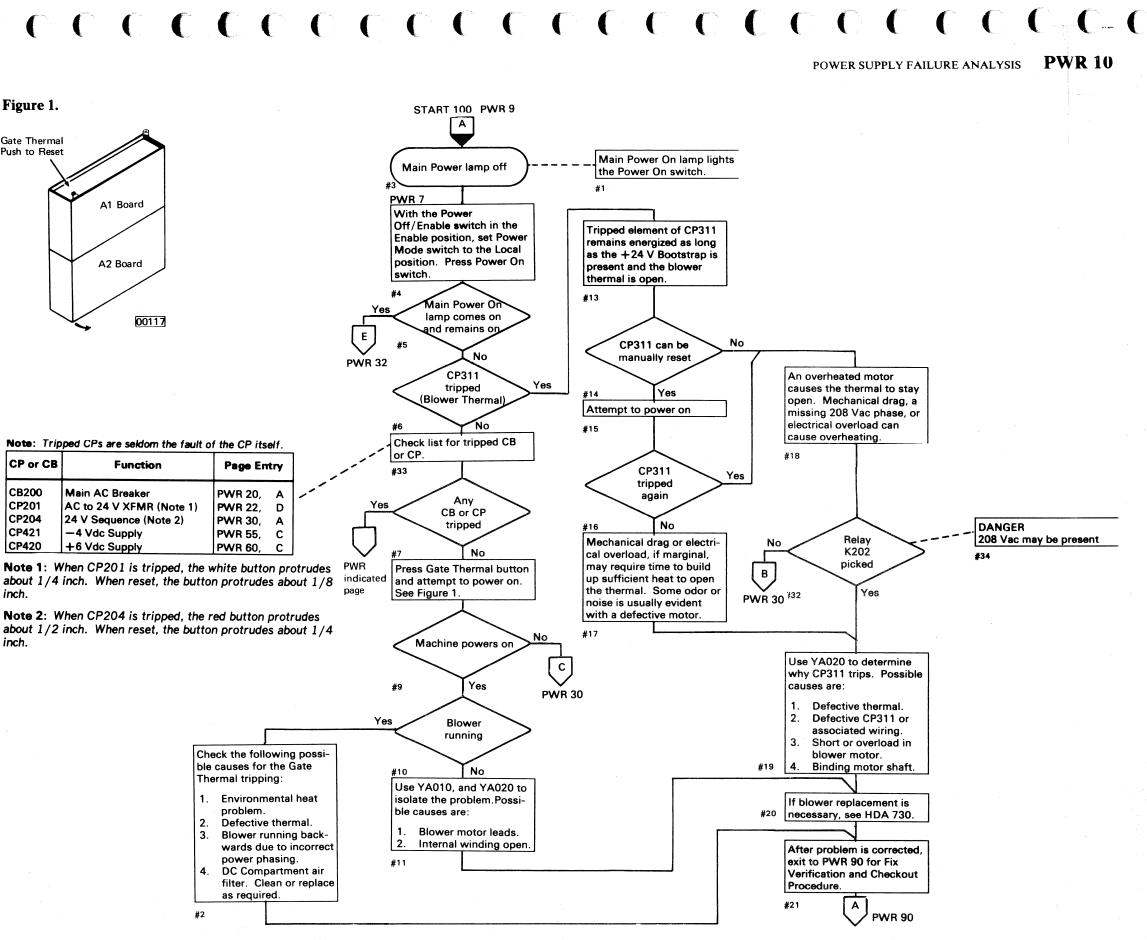


Function

Main AC Breaker

-4 Vdc Supply

+6 Vdc Supply



2358262 441300 441305 EG0010 3350 31 Mar 76 29 Oct 76 Seq. 1 of 2 Part No.

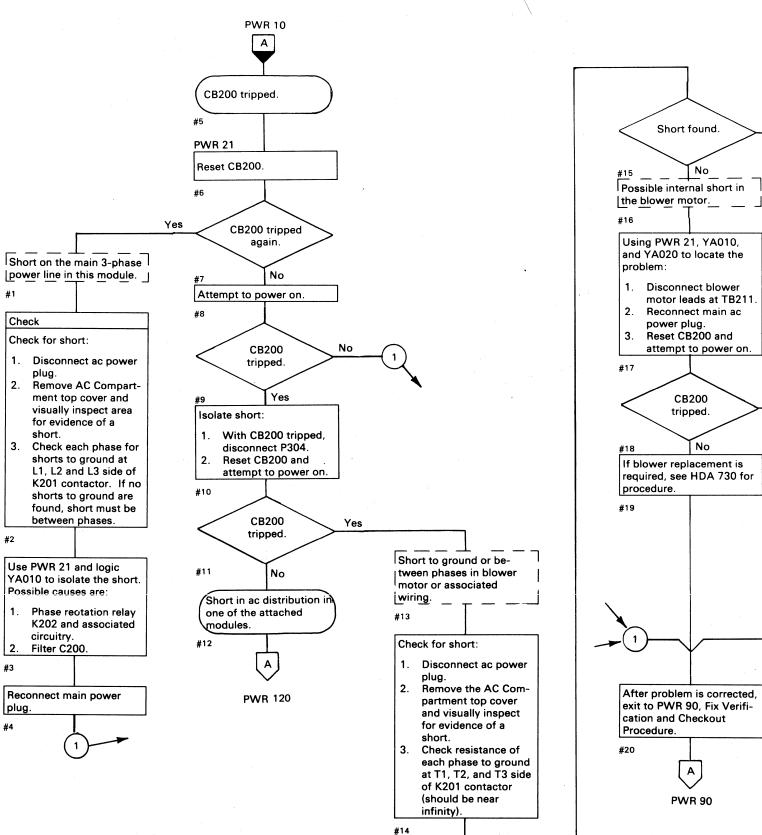
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POWER SUPPLY FAILURE ANALYSIS **PWR 10** 

# **AC CIRCUIT FAILURE ANALYSIS**

#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering on machine.



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#4

AC CIRCUIT FAILURE ANALYSIS

**PWR 20** 

Yes			
>			
7		Using PWR 2 and YA020, d terminals as r isolate the sh	lisconnect necessary to
		#21	
		Reset CB200 nect P304.	and recon-
		#22	
> Yes			
r	Using PWR 21, YA and YA020, carefu disconnect termina necessary to isolat short. Reconnect a power plug, reset ( and attempt to pow Repeat this proces necessary to isolat short.	lly als as e the ac CB200, ver on. s as	
	#23		
	Reconnect P304. #24	J	
<b></b>			<b>-</b>
<b>1</b> ,			

# AC CIRCUIT FAILURE ANALYSIS **PWR 20**

 $\bigcirc$ 

# AC CIRCUIT DIAGRAM (A2)

#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering on machine.

See ZA100 for relay and contactor point location.

СР

220

СВ

200

T201

**TB202** 

C200

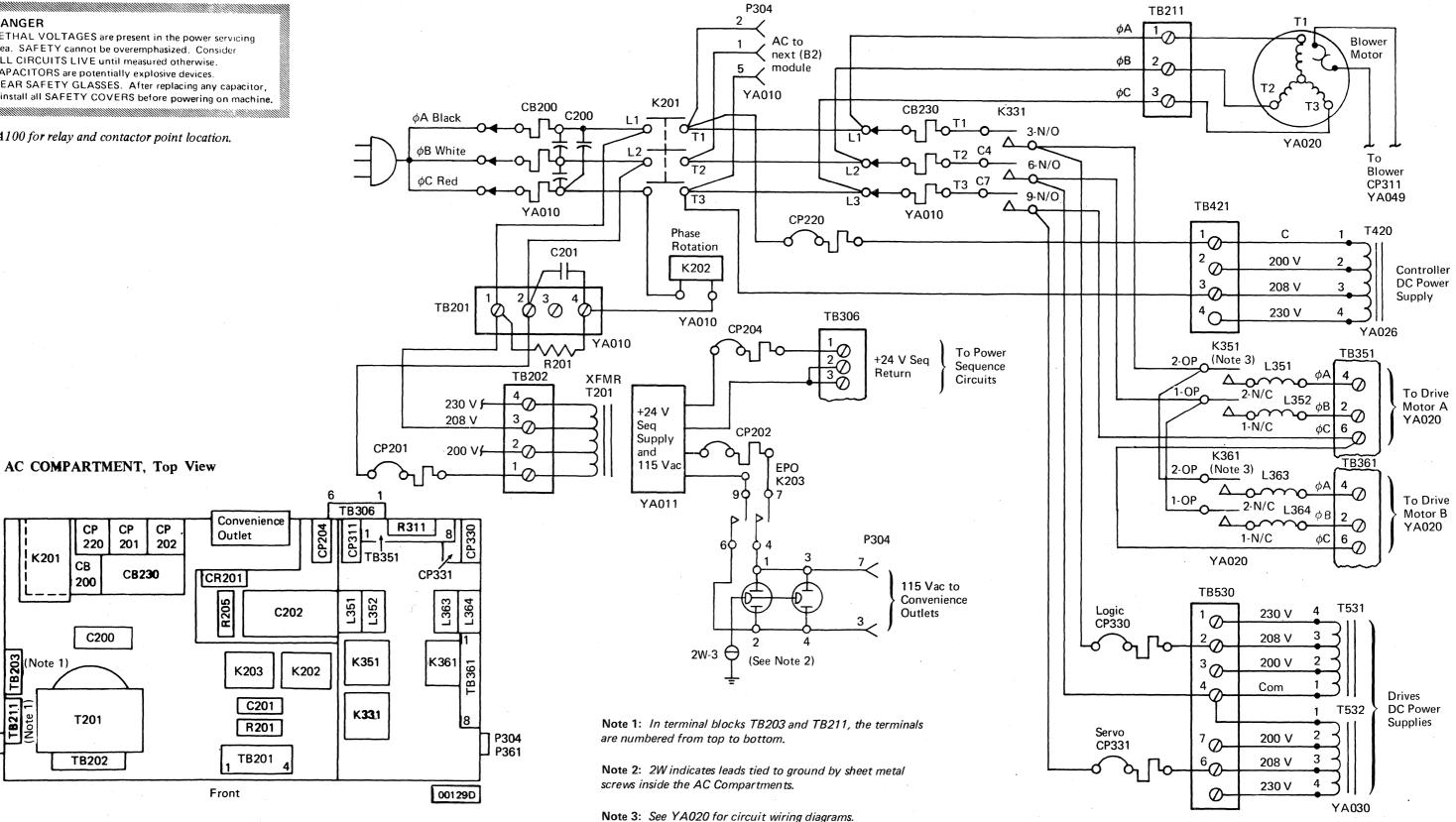
K201

(Note 1)

P351

CP

201



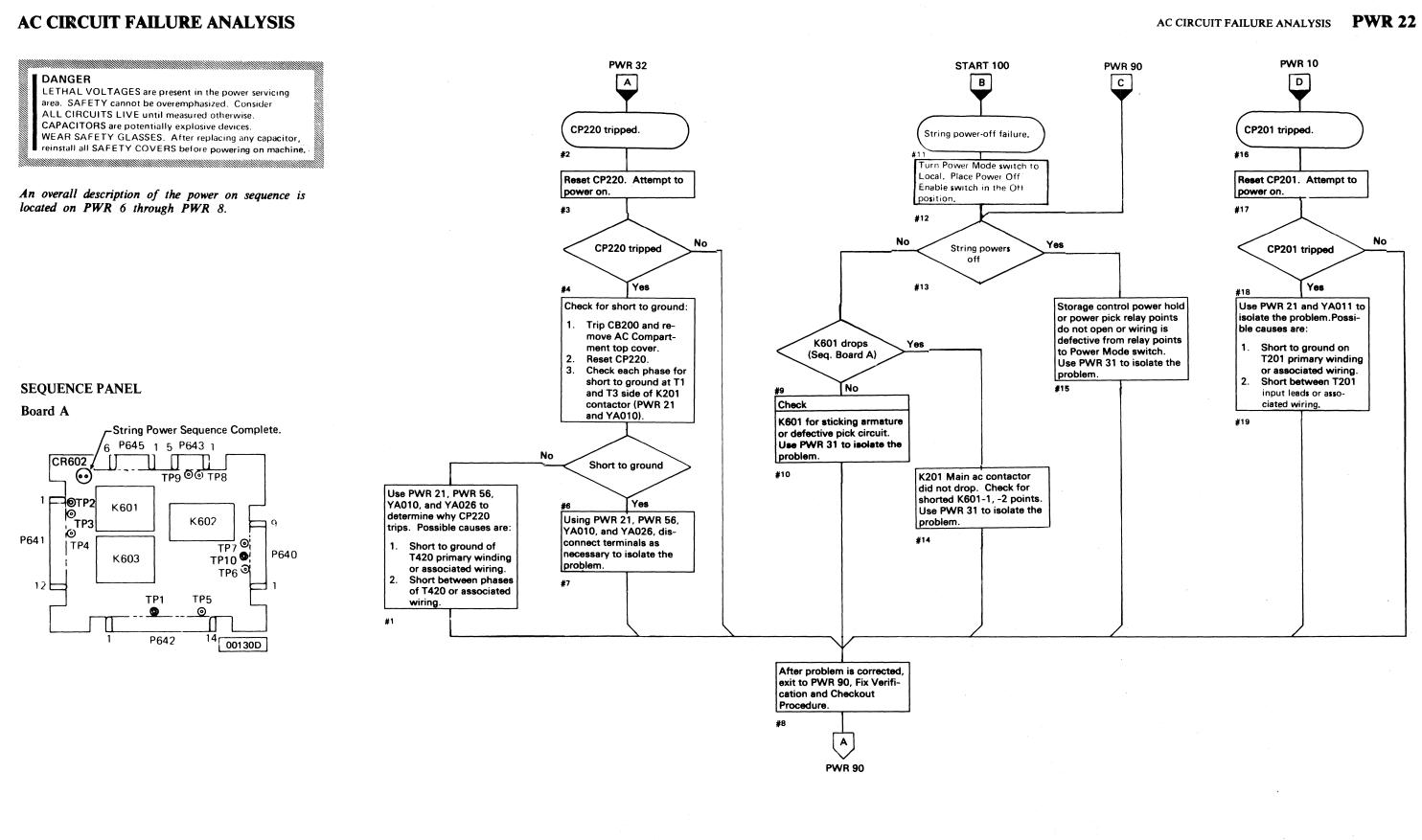
2358263 441300 EG0021 441301 441305 441306 3350 Seg. 1 of 1 Part No. 31 Mar 76 1 Jun 76 29 Oct 76 1 Apr 77

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AC CIRCUIT DIAGRAM (A2) **PWR 21** 

**PWR 21** 





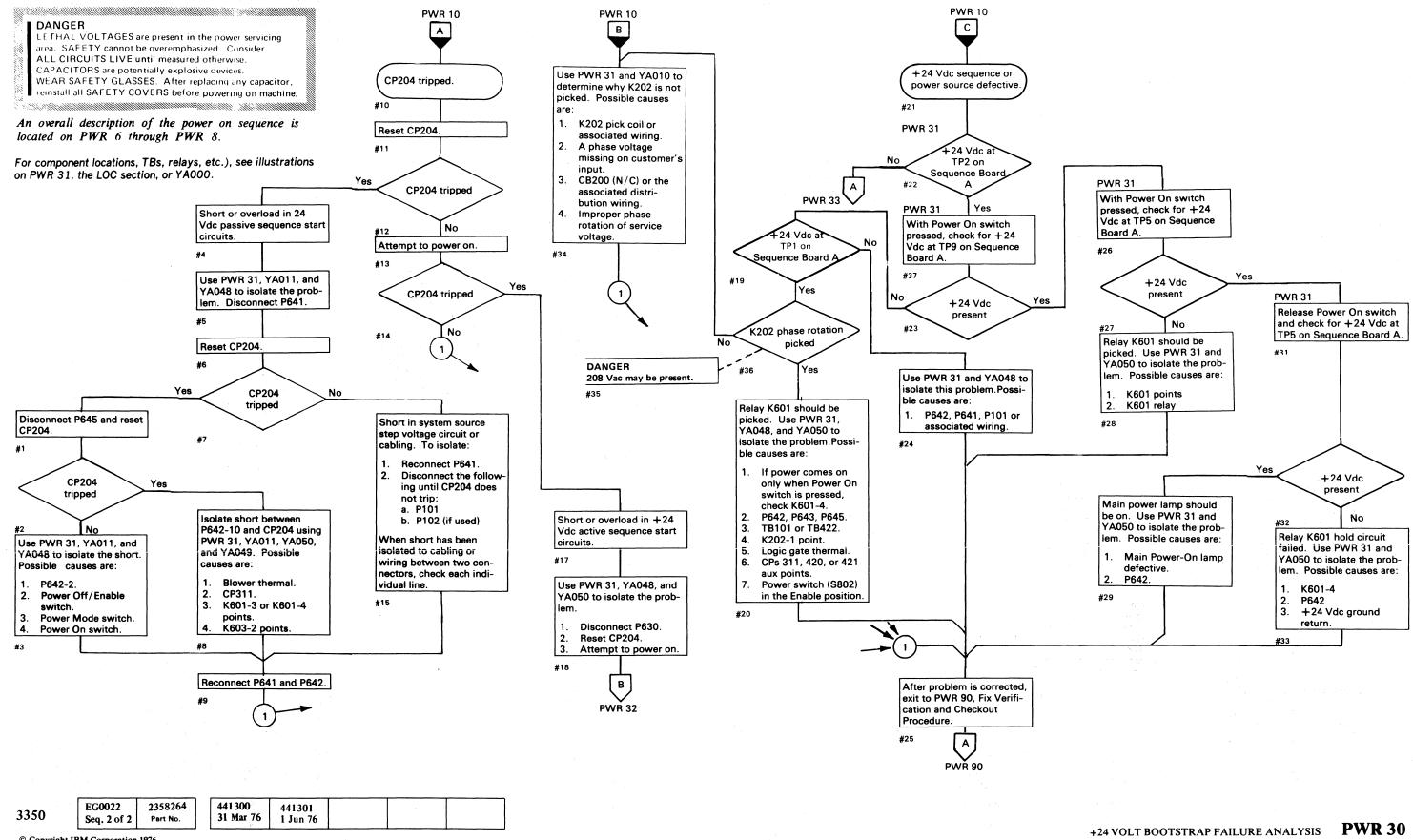
	3350	EG0022 Seq. 1 of 2	2358264 Part No.	441300 31 Mar 76	441301 1 Jun 76				
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AC CIRCUIT FAILURE ANALYSIS **PWR 22** 

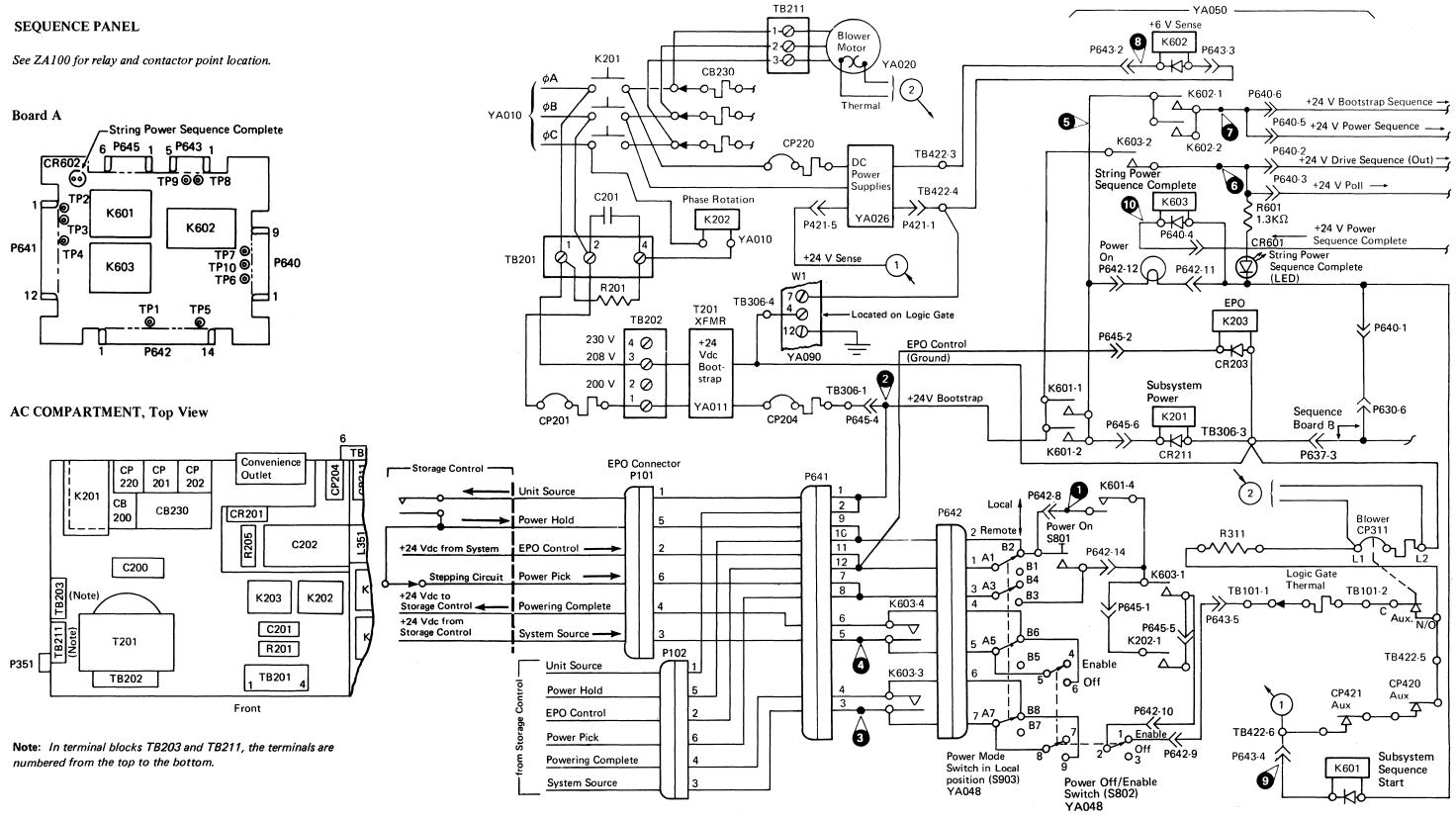
# +24 VOLT BOOTSTRAP FAILURE ANALYSIS

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# +24 VOLT BOOTSTRAP DIAGRAM



5550	EG0031	2358265	441300	441301	441305	441309	441310
	eq. 1 of 2	Part No.	31 Mar 76	1 Jun 76	29 Oct 76	15 Jul 79	27 Jun 80

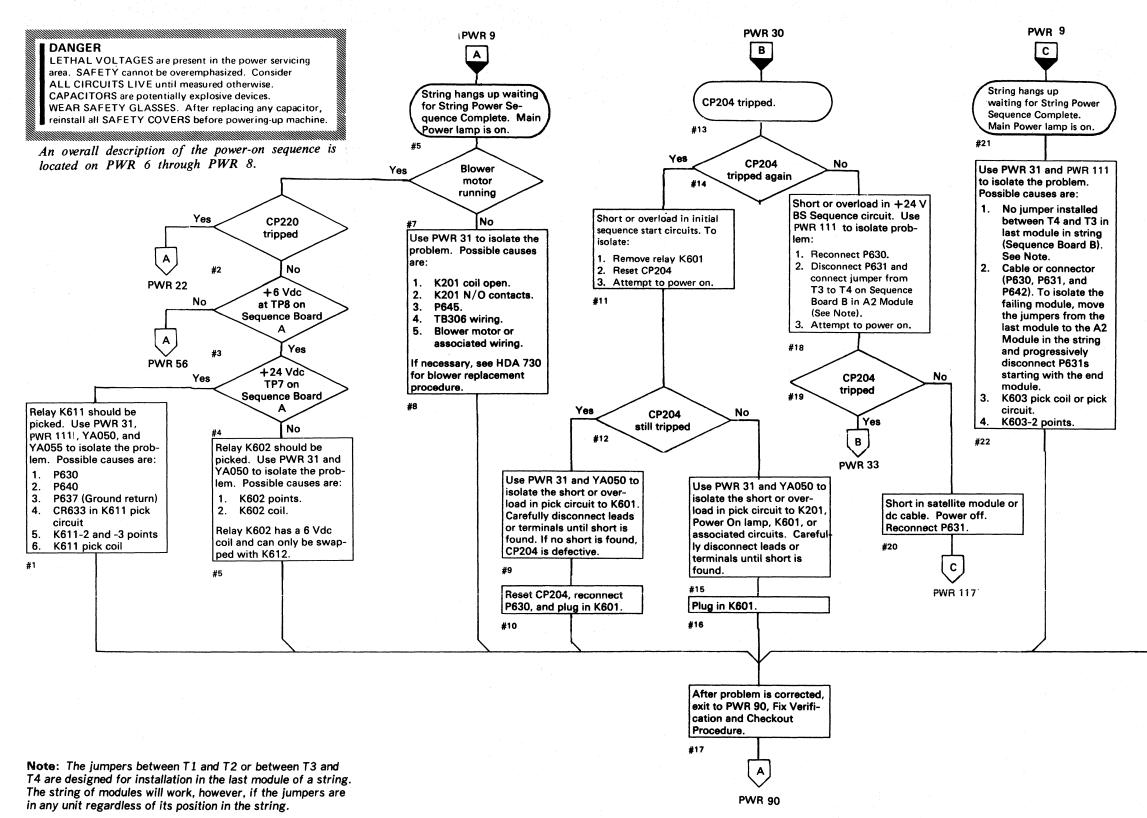
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+24 VOLT BOOTSTRAP DIAGRAM

**PWR 31** 

#### **PWR 31** +24 VOLT BOOTSTRAP DIAGRAM

# +24 VOLT BOOTSTRAP FAILURE ANALYSIS

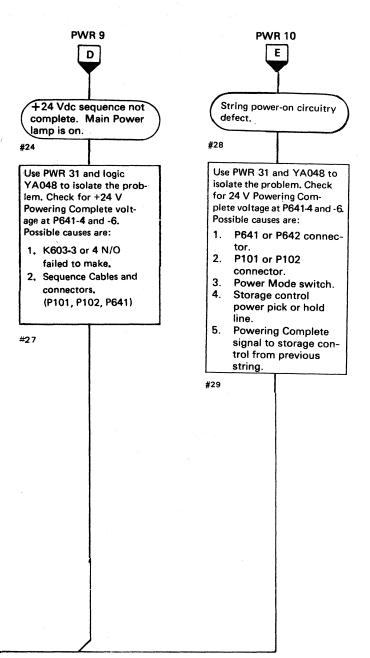


EG0031 2358265 441300 441301 441305 441309 441310 3350 Seq. 2 of 2 29 Oct 76 15 Jul 79 27 Jun 80 Part No. 31 Mar 76 1 Jun 76

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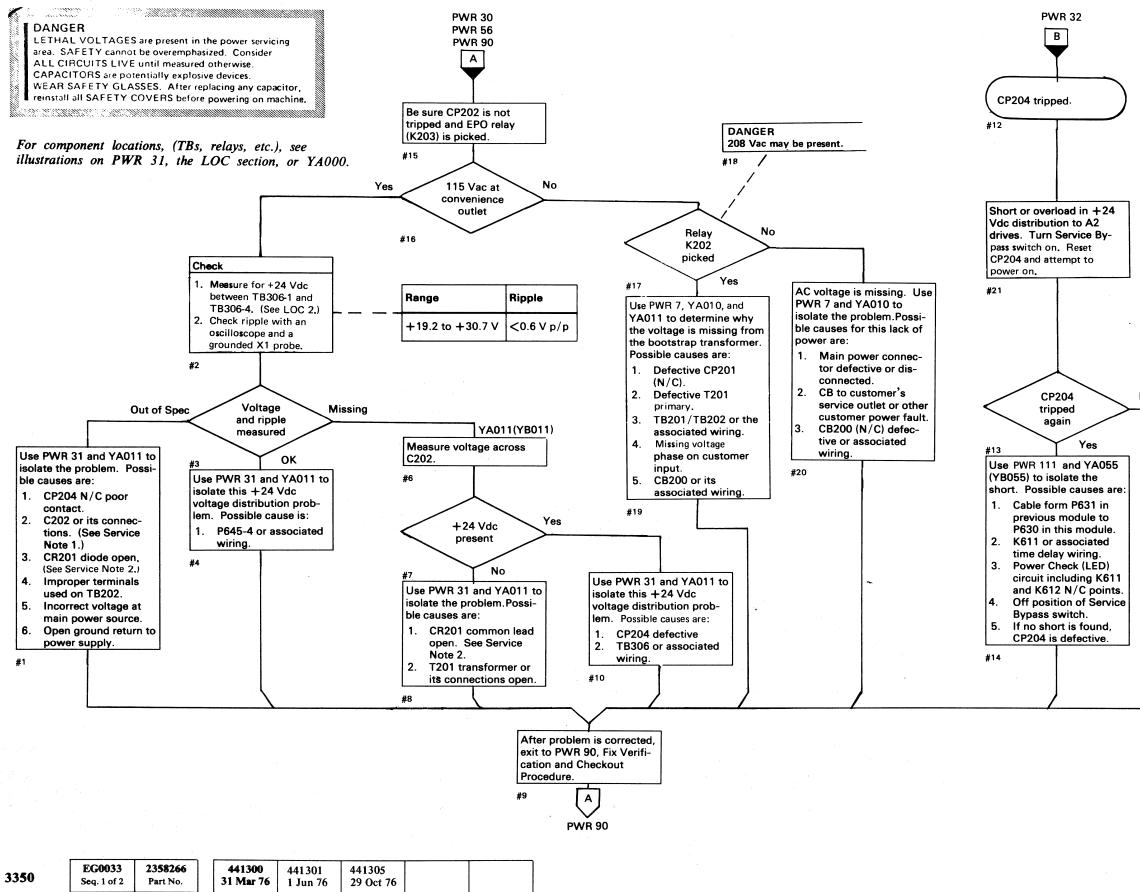
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# +24 VOLT BOOTSTRAP FAILURE ANALYSIS **PWR 32**



+24 VOLT BOOTSTRAP FAILURE ANALYSIS **PWR 32** 

# +24 VOLT BOOTSTRAP FAILURE ANALYSIS



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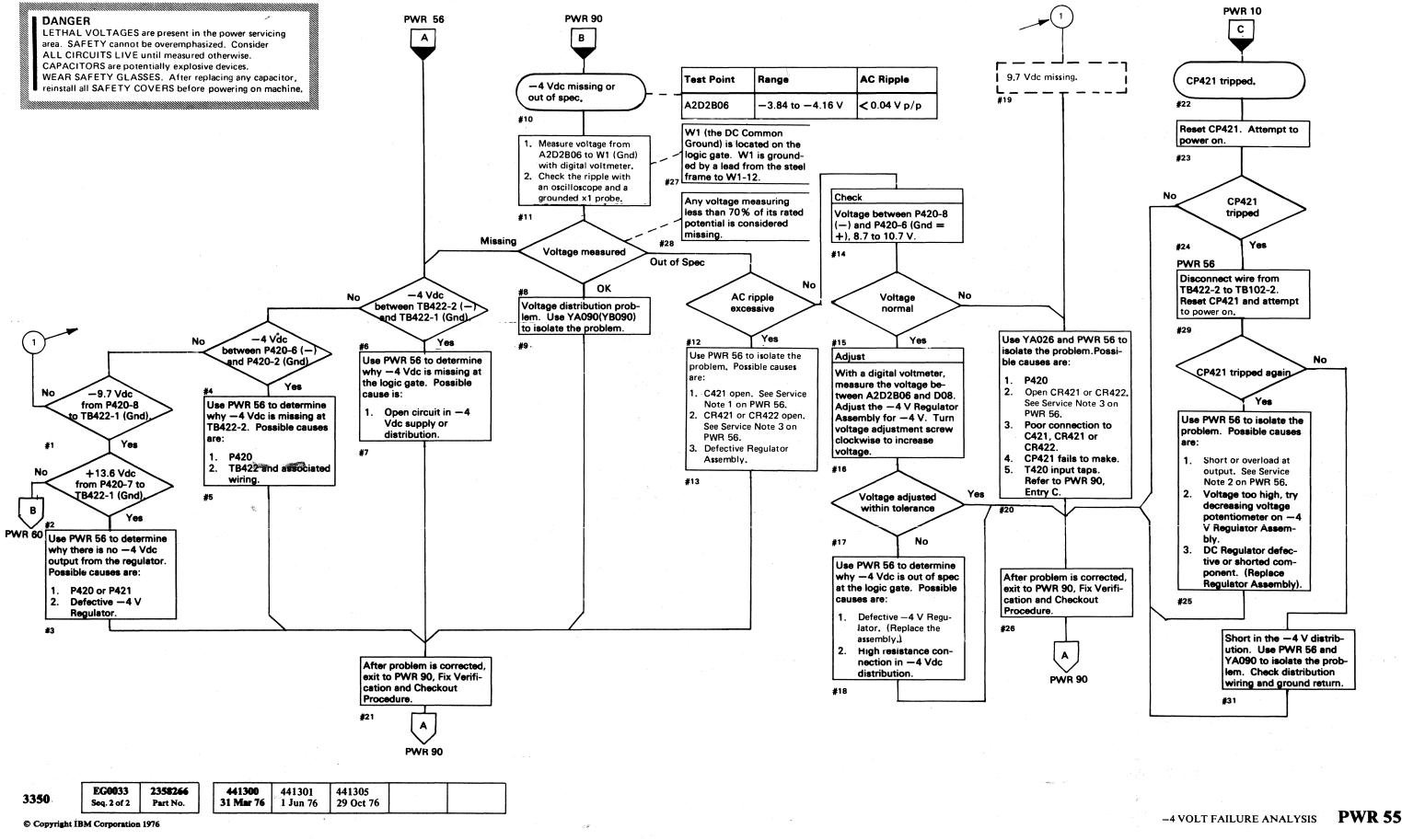
+24 VOLT BOOTSTRAP FAILURE ANALYSIS **PWR 33** 

### SERVICE NOTES

- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to  $R \times 10$ .
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to  $R \times 1$  to speed up the process.
- 2. Rectifier Check with CE Meter
  - a. Disconnect leads to CR201 assembly (PWR 31).
  - b. With the meter set to  $R \times 1$ , measure the forward resistance which should be from 5 to 15 ohms.
  - c. Set the meter to  $R \times 1000$  and reverse the meter leads. The resistance should be near infinity.

No		
		]
	(YB055) to is	1 and YA055 olate the ole causes are:
	mal or a tacts.	ntactor. at Gate Ther- uxiliary con- 632, or P637.
	#11	

# -4 VOLT FAILURE ANALYSIS

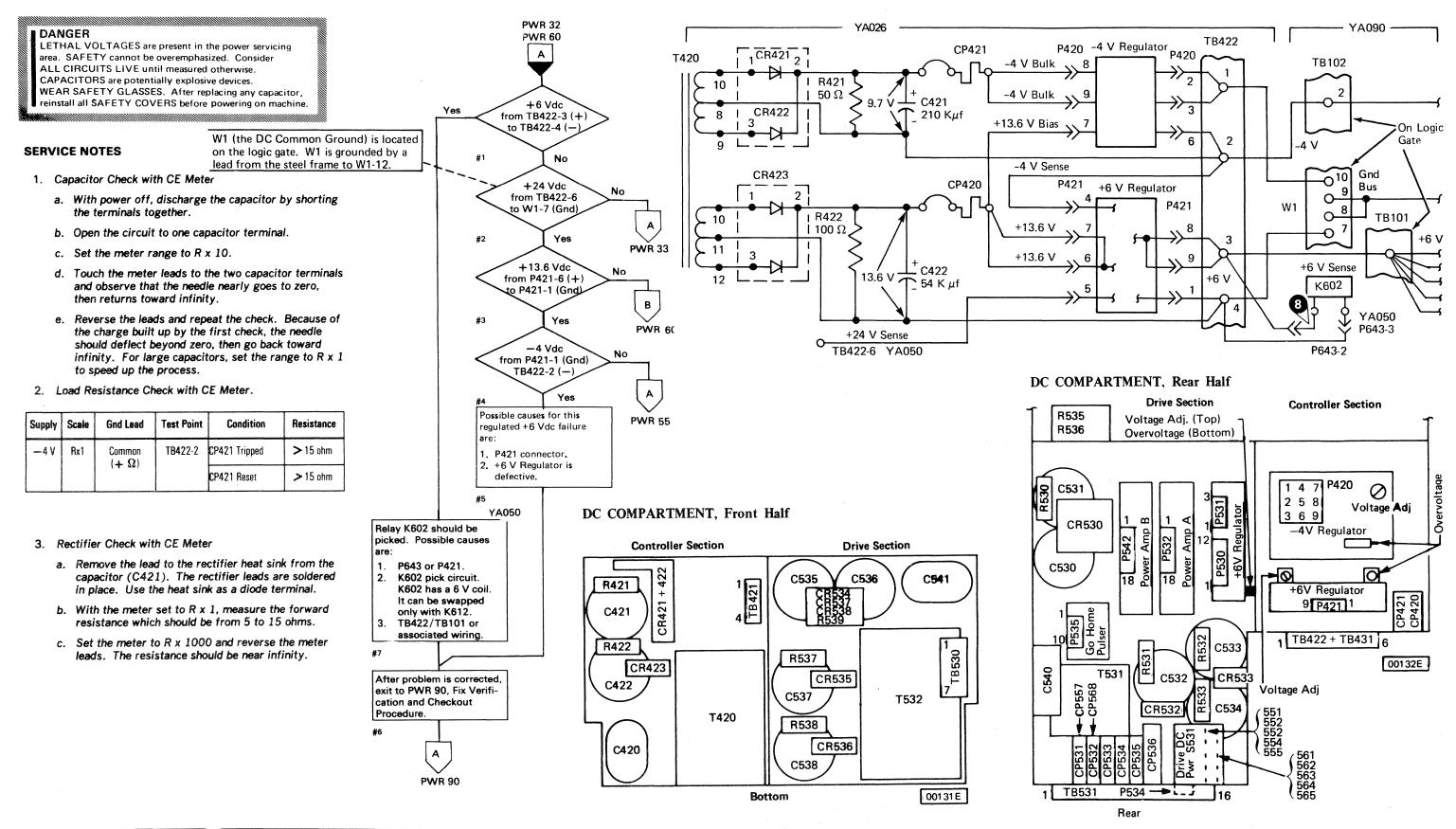


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**PWR 55** 

### -4 VOLT FAILURE ANALYSIS

# -4 V AND +6 V REGULATOR DIAGRAM

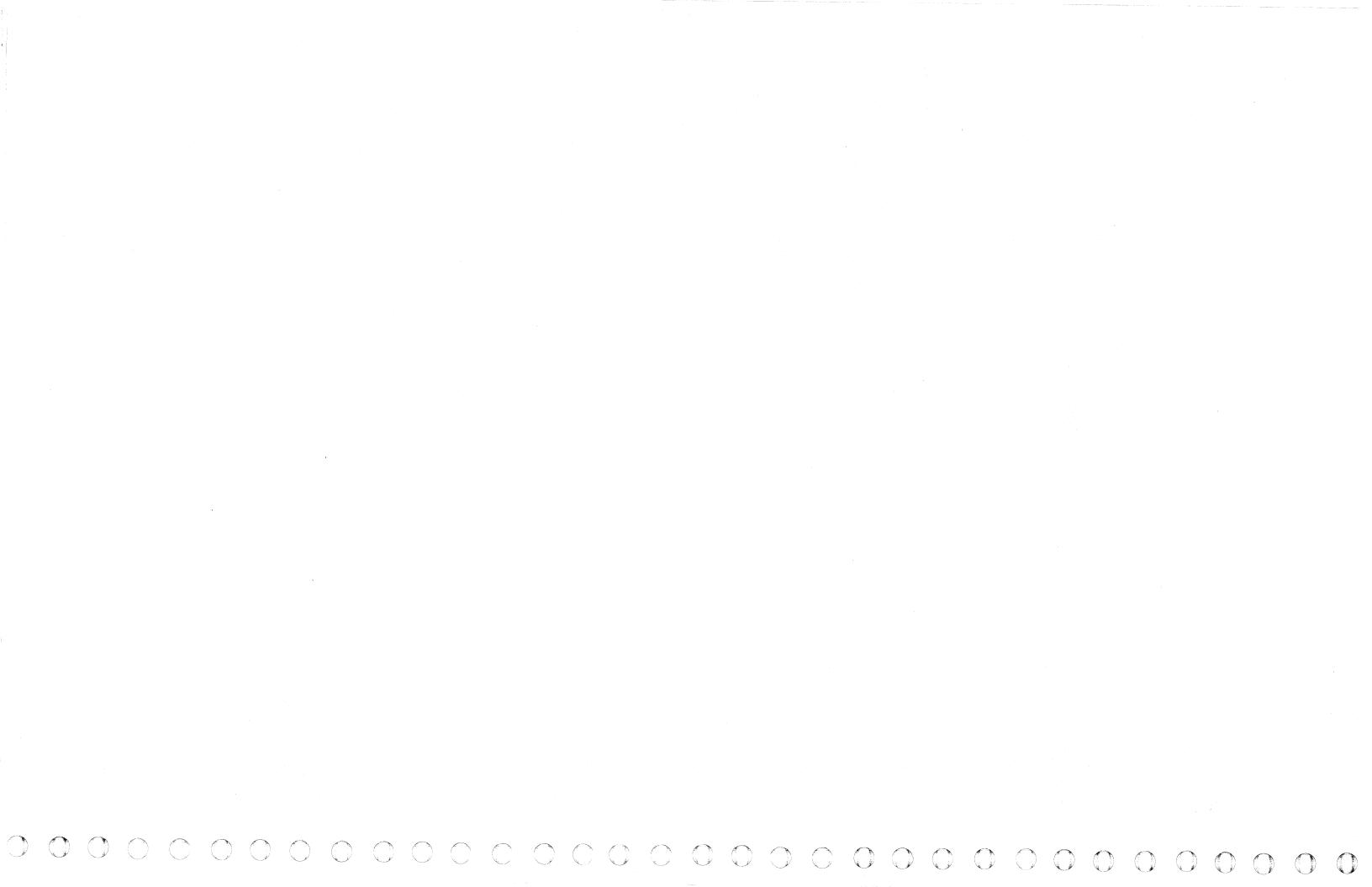


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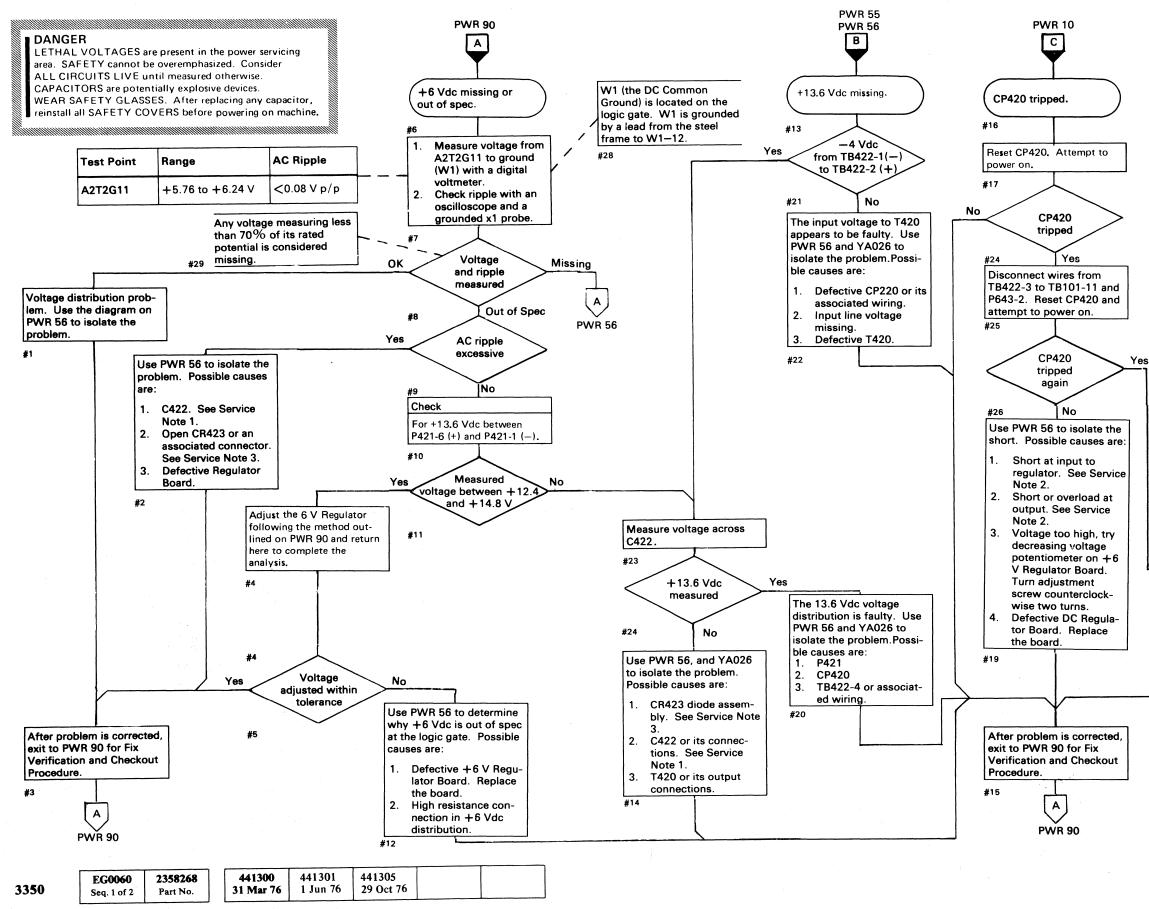
# -4 V AND +6 V REGULATOR DIAGRAM **PWR 56**

-4 V AND +6 V REGULATOR DIAGRAM

**PWR 56** 



# +6 VOLT FAILURE ANALYSIS



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+6 VOLT FAILURE ANALYSIS **PWR 60** 

#### SERVICE NOTES

- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to R x 10.
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to R x 1 to speed up the process.

Supply	Scale	Gnd Lead	Test Point	Condition	Resistance
+6V	Rx1	$\stackrel{Common}{(+ \Omega)}$	TB422-3	CP420 Tripped CP420 Reset	> 15 ohm > 15 ohm
		TB422-2	W 1*		<b>&gt;</b> 10 ohm

2. Load Resistance Check with CE Meter

\*Located on Logic Gate.

- 3. Rectifier Check with CE Meter
  - a. Disconnect leads to CR423 assembly (PWR 56).
  - b. With the meter set to R x 1, measure the forward resistance which should be from 5 to 15 ohms.
  - c. Set the meter to R x 1000 and reverse the meter leads. The resistance should be near infinity.

	Short in the +6 V distrib- ution. Use PWR 56 and YA090 to isolate the prob- lem. Possible causes are:
	1. Logic gate distrib-
	ution. 2. K602 or its associated pick circuit wiring.
#27	

# **FIX VERIFICATION AND VOLTAGE CHECKS**

PWR A

## **FIX VERIFICATION AND CHECKOUT PROCEDURE**

Complete the following checklist to ensure that the machine problem has been corrected. If a check cannot be completed, go to the referenced MIM page for aid in making a fix.

Note 1: It is not always necessary to check each step. Use your judgement for skipping all unneeded steps.

- 1. Set Power Mode switch to Local, then power off the string by placing the Power Off/Enable switch in the Off position. If the string does not power off, go to PWR 22, Entry C (controller).
- 2. Restore the string to normal operating conditions. (Remove all diagnostic jumpers and replace wiring, connectors, or parts that were removed.)
- 3. Power on the string, then set Power Mode switch to Remote.
- 4. Verify that the Power Sequence Complete (LED) and String Power Sequence Complete (LED) indicators and the blowers in each module all turn on. If not, go to PWR 9, Entry D.
- 5. Turn on the A and B Drive Start switches on the problem module(s). Verify that both Ready lamps turn on. If not, go to START 100, Entry B.
- 6. Check power supply voltages as shown in the Voltage Check Chart (this page). (See Note 2.)
- 7. Examine the DC Compartment air filter and clean or replace as necessary.
- 8. Replace all covers.
- 9. Run a string check. (See START 110.)
- 10. Go to START 500, Entry A.

PWR В

# **VOLTAGE CHECKS**

Note 2: The following checks should be made with the drives stopped or ready but with no Seek or Read/Write operations in progress.

### **DC Voltage Checks**

Measure each dc voltage in the order listed in the Voltage Check Chart. Only two voltages can be directly adjusted (-4 V and +6 V) for the controller board (A2). If adjustments are necessary, measure with a digital voltmeter. The adjustment potentiometers for -4 V and +6 V Regulators are accessible when the rear DC Compartment cover is removed. Be certain that only the voltage adjustment potentiometer on the regulator assembly is adjusted. (See PWR 56.) The overvoltage potentiometer on each card is adjusted at the plant and should not be changed. Turn the voltage adjustment potentiometer clockwise to increase the voltage.

The +24 V Bootstrap supply has no output voltage adjustment. The only adjustment possible is to change the transformer primary input taps. The primary taps at T201 determine the ac input to the +24 V Bootstrap supply. If this supply is not within specification, check the main 3-phase ac power and ensure that the machine is wired for the correct input voltage, as shown in the Transformer Primary Input Tap Wiring Chart on this page.

If the voltage checks are not completed successfully, exit to the appropriate MAP indicated in the Voltage Check Chart.

If this page is entered because of a known dc voltage problem, and the voltage checks are correct. the problem must be in the voltage distribution. Use the appropriate diagram listed in the chart to isolate the problem.

### **AC Ripple Checks**

If the peak-to-peak ac ripple exceeds the maximum listed in the chart, it is likely that a power supply part has failed.

To measure the ac ripple, use the ac input on a scope having a 0.01 volt per centimeter range and a X1 probe placed on the test points shown in the chart. Place the probe ground on any convenient ground point.

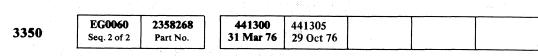
If the ac component is greater than the maximum listed, exit to the appropriate MAP referenced in the chart to correct the problem.

> W1 (the DC Common Ground) is located on the logic gate. W1 is grounded by a lead from the steel frame to W1-12.

# **VOLTAGE CHECK CHART** /

DC Supply	Test Point	Tolerance (Volts)	Adjustment	Logic Page	Maximum AC Ripple	Diagram	Page Entry
+24 V BS Seq.	TB306-1 to W1 (Gnd)	+19.2 to +30.7	None*	YA050	0.6 V p/p	PWR 31	PWR 33, A
–4 V Reg	A2D2B06 to A2T2D08	-3.84 to -4.16 (Adjust to 4.0)	Turn screw clockwise to in- crease voltage	YA090 BV100	0.04 V p/p	PWR 56	PWR 55, B
+6 V Reg	A2T2G11 to A2T2D08	+5.76 to 6.24 (Adjust to 6.0)	Turn screw clockwise to in- crease voltage	YA090 BV100	0.08 V p/p	PWR 56	PWR 60, A

\* Check transformer primary input taps, change to match available voltage. (See chart above.)



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FIX VERIFICATION AND VOLTAGE CHECKS **PWR 90** 



# **TRANSFORMER PRIMARY INPUT TAP** WIRING CHART

Voltage	TB202 (YA011)	TB421 (YA026)
200 V	Phase A to TB202-2	Phase C to TB421-2
208 V	Phase A to TB202-3	Phase C to TB421-3
230 V	Phase A to TB202-4	Phase C to TB421-4

Note 3: Before changing primary taps, check another dc output voltage that uses the same primary winding (except +24 Vdc Bootstrap).

FIX VERIFICATION AND VOLTAGE CHECKS **PWR 90** 

A2 MODULE

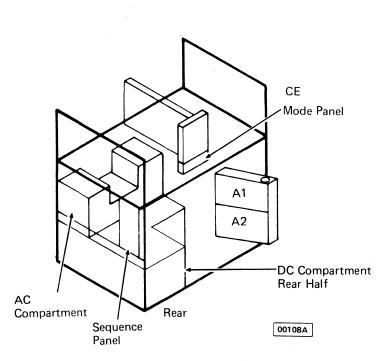
# **COMPONENT AND TEST POINT LOCATIONS**

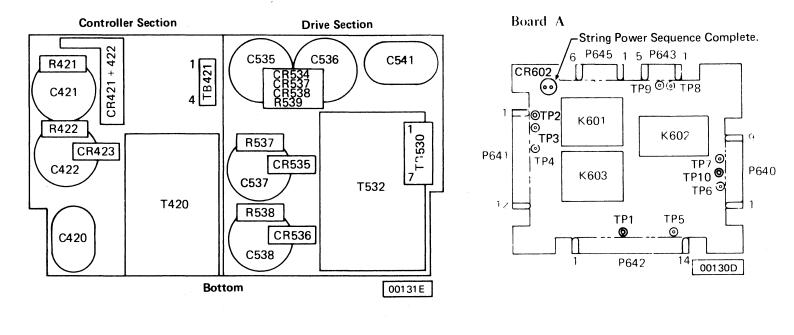
#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise

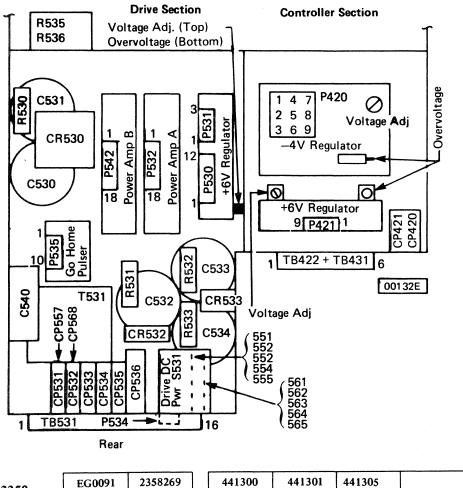
- CAPACITORS are potentially explosive devices.
- WEAR SAFETY GLASSES. After replacing any capacitor,
- reinstall all SAFETY COVERS before powering on machine.

# See ZA100 for relay and contactor point location.





# DC COMPARTMENT, Rear Half

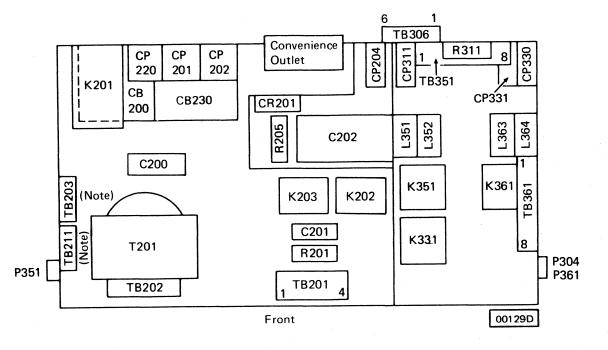


31 Mar 76

1 Jun 76

29 Oct 76

AC COMPARTMENT, Top View



DC COMPARTMENT, Front Half

Note: In terminal blocks TB203 and TB211, the terminals are numbered from top to bottom.

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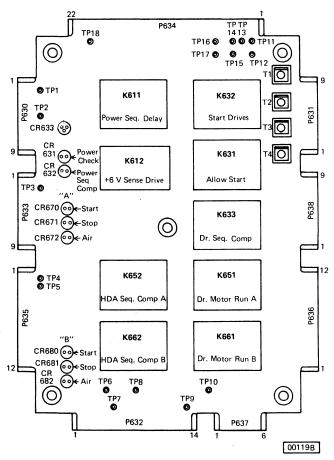
Seq. 1 of 1

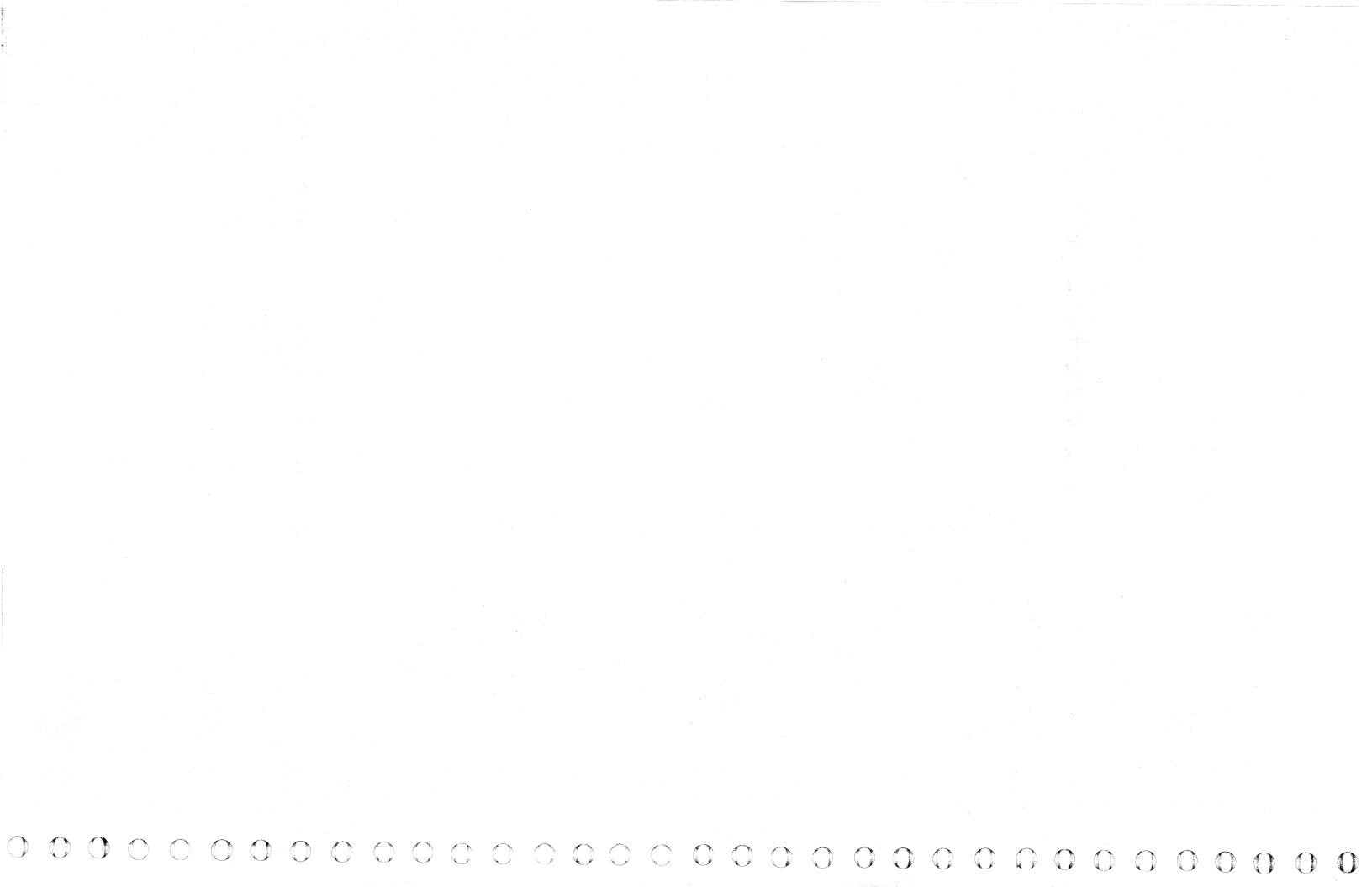
Part No.

3350

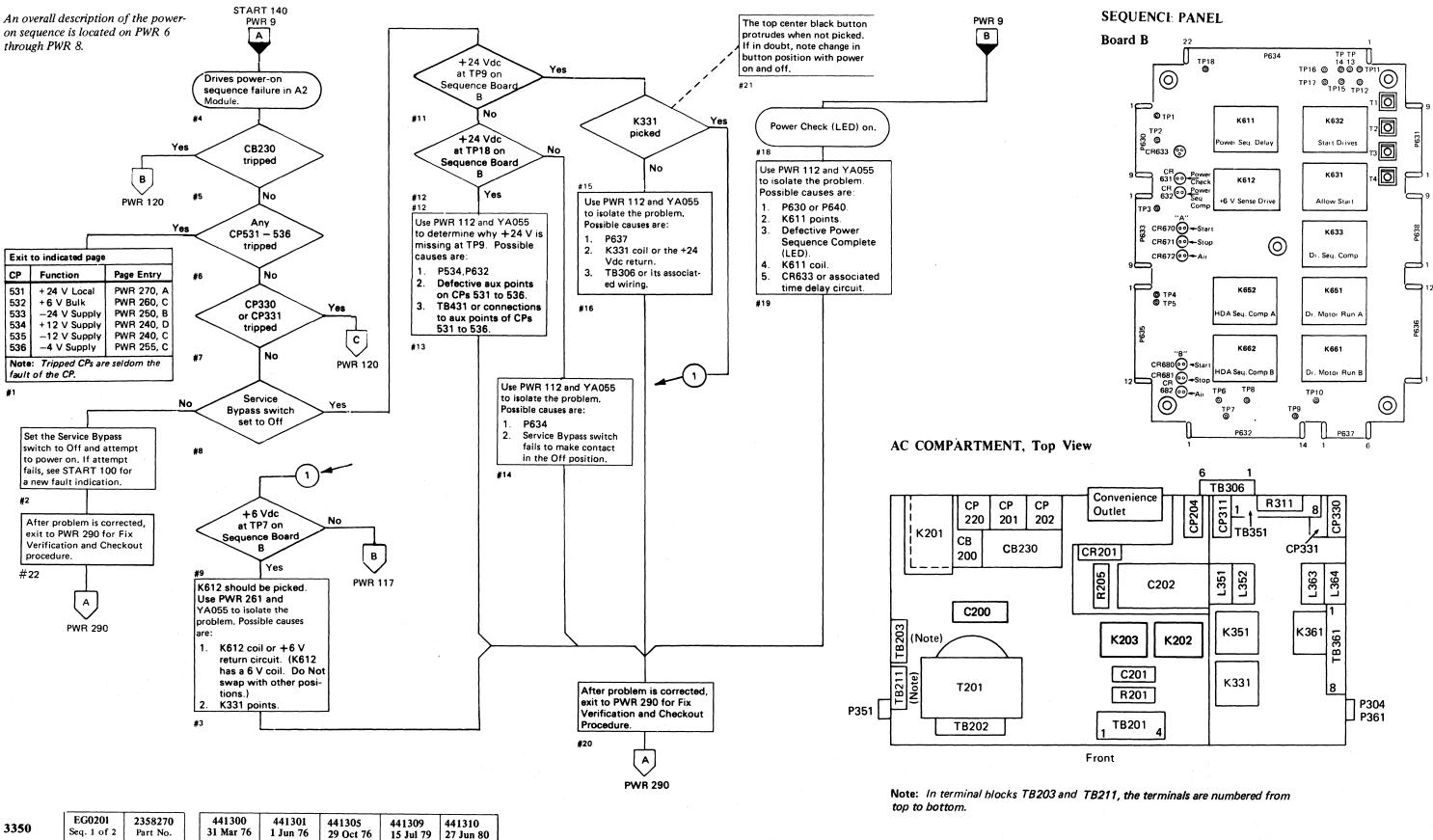
# **SEQUENCE PANEL, A2 MODULE**

**Board B** 





# **DRIVE POWER SEQUENCING ANALYSIS (A2)**



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**PWR 101** 

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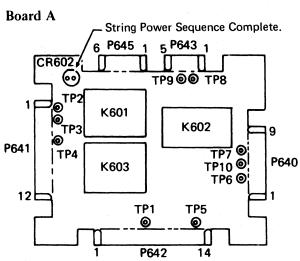
**DRIVE POWER SEQUENCING ANALYSIS (A2)** 

**PWR 101** 

# **DRIVE POWER SEQUENCING DIAGRAM**

# SEQUENCE PANEL

See ZA100 for relay and contactor point location.



СР

220 201 202

CB230

СР

Outlet

CR201

R205

Front

# AC COMPARTMENT, Top View

CP

СВ

200

C200

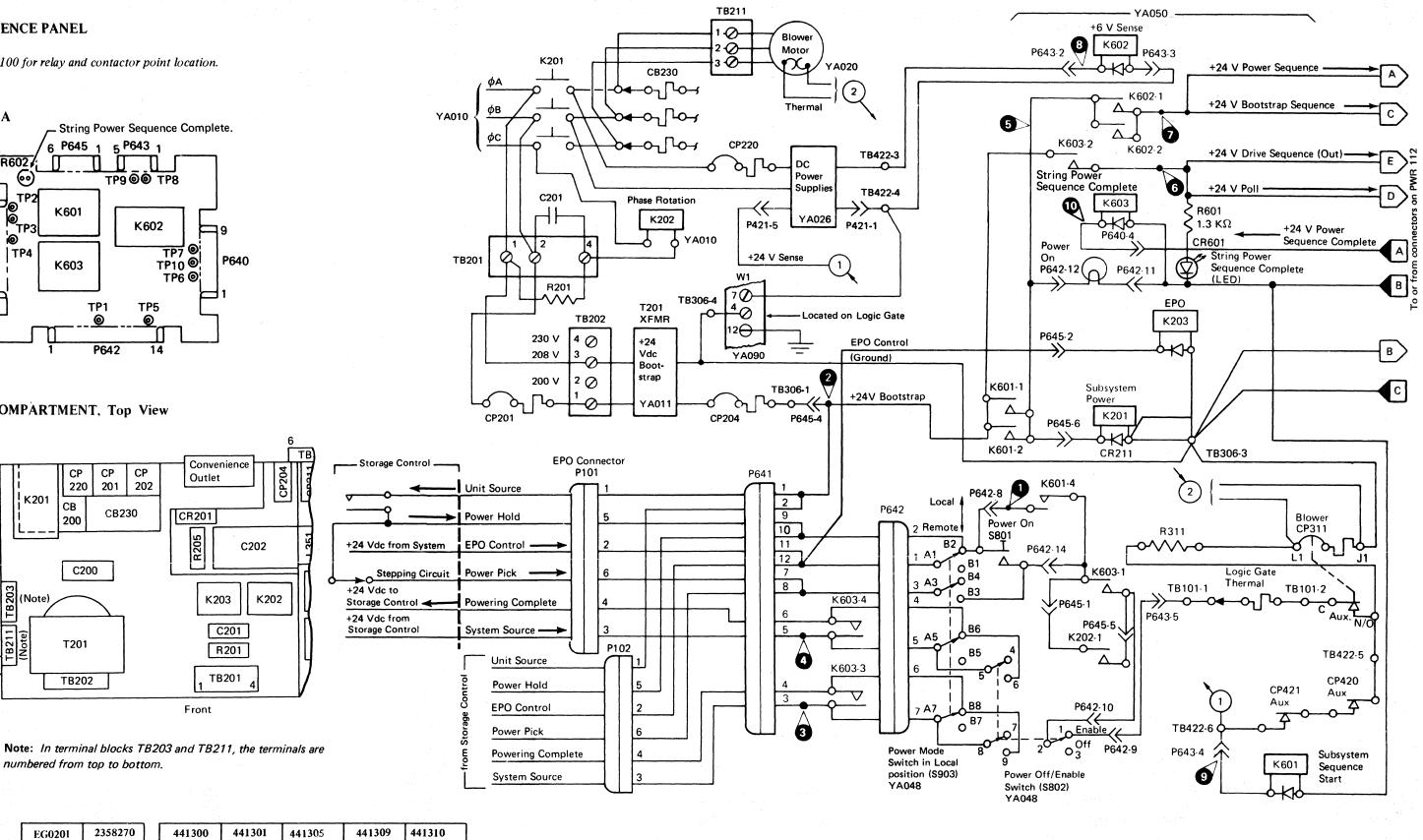
T201

TB202

K201

(Note)

P351



numbered from top to bottom.

3350	EG0201	2358270	441300	441301	441305	441309	441310
	Seq. 2 of 2	Part No.	31 Mar 76	1 Jun 76	29 Oct 76	15 Jul 79	27 Jun 80
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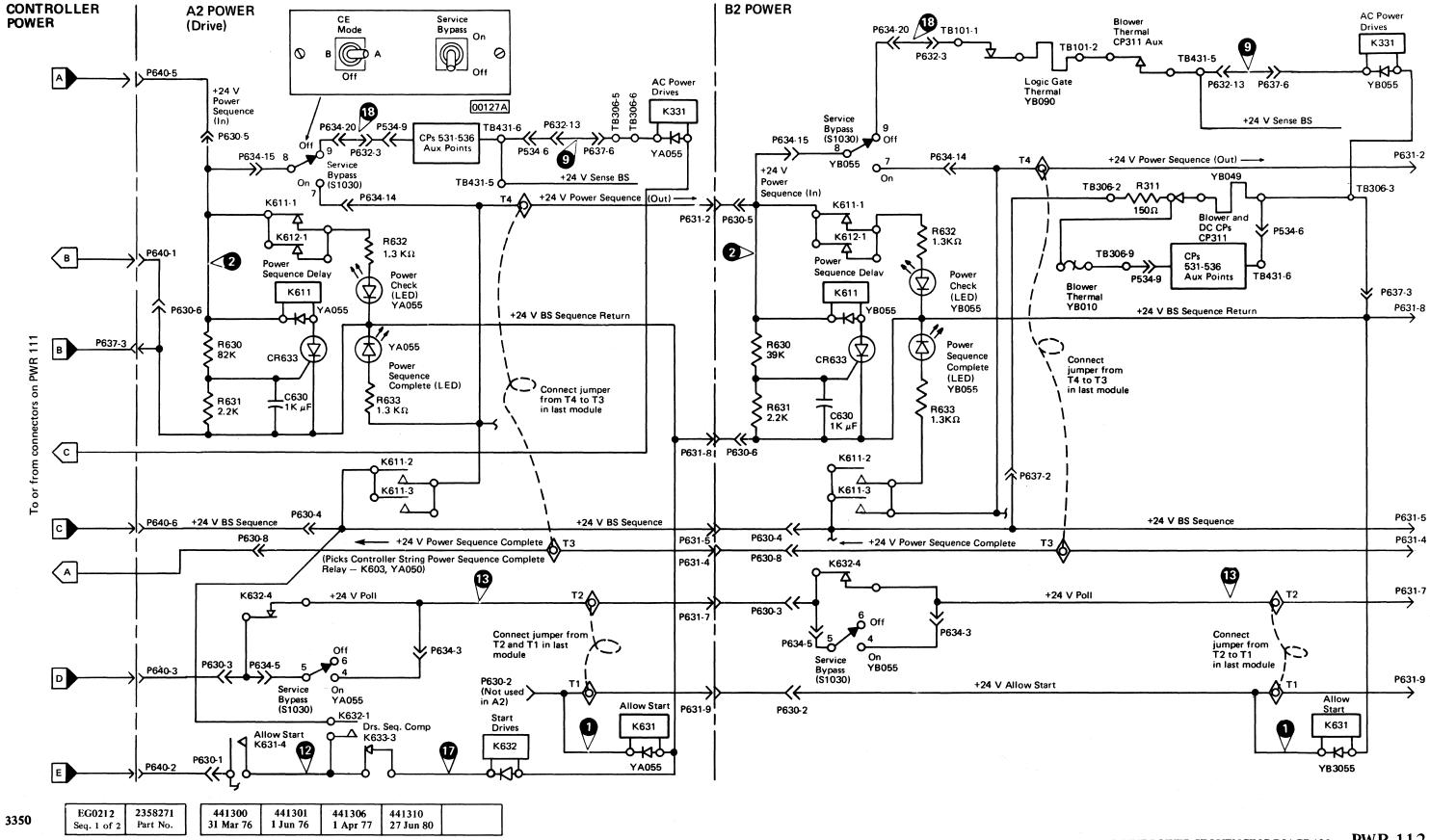
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DRIVE POWER SEQUENCING DIAGRAM

DRIVE POWER SEQUENCING DIAGRAM PWR 111

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# **DRIVE POWER SEQUENCING DIAGRAM**



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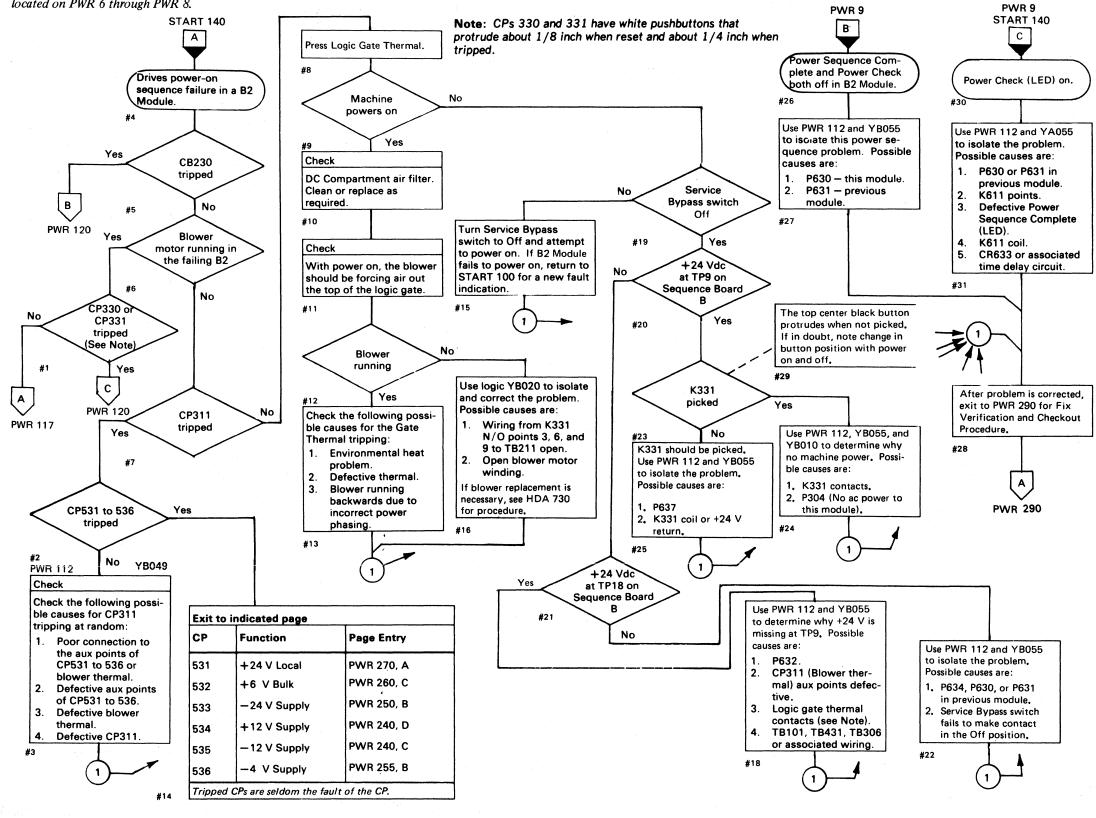
**PWR 112** 

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DRIVE POWER SEQUENCING DIAGRAM PWR 112

# **DRIVE POWER SEQUENCING ANALYSIS (B2)**

An overall description of the power-on sequence is located on PWR 6 through PWR 8.



441306 441310 3350 Seq. 2 of 2 Part No. 31 Mar 76 1 Jun 76 1 Apr 77 27 Jun 80 © Copyright IBM Corporation 1976, 1977

441300

441301

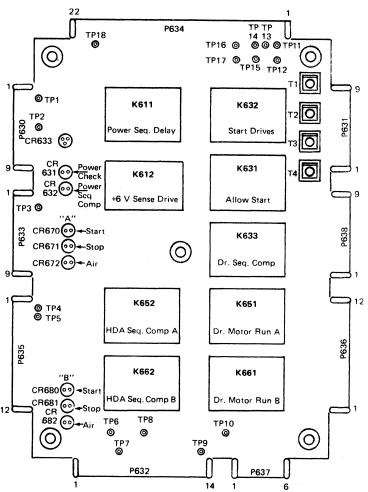
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EG0212

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#### DRIVE POWER SEQUENCING ANALYSIS (B2)

# **PWR 116**

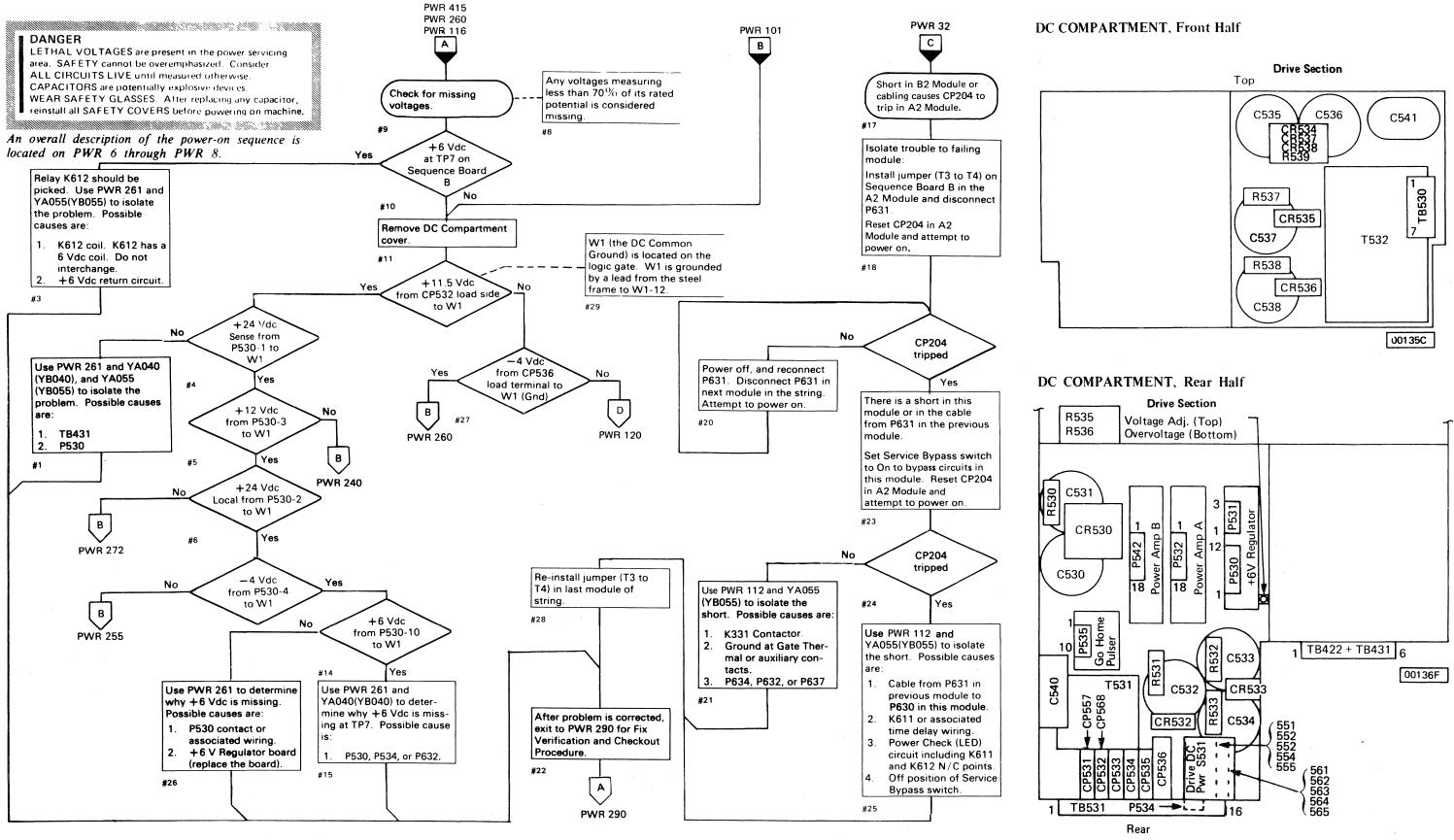


# SEQUENCE PANEL

**Board B** 

DRIVE POWER SEQUENCING ANALYSIS (B2) **PWR 116** 





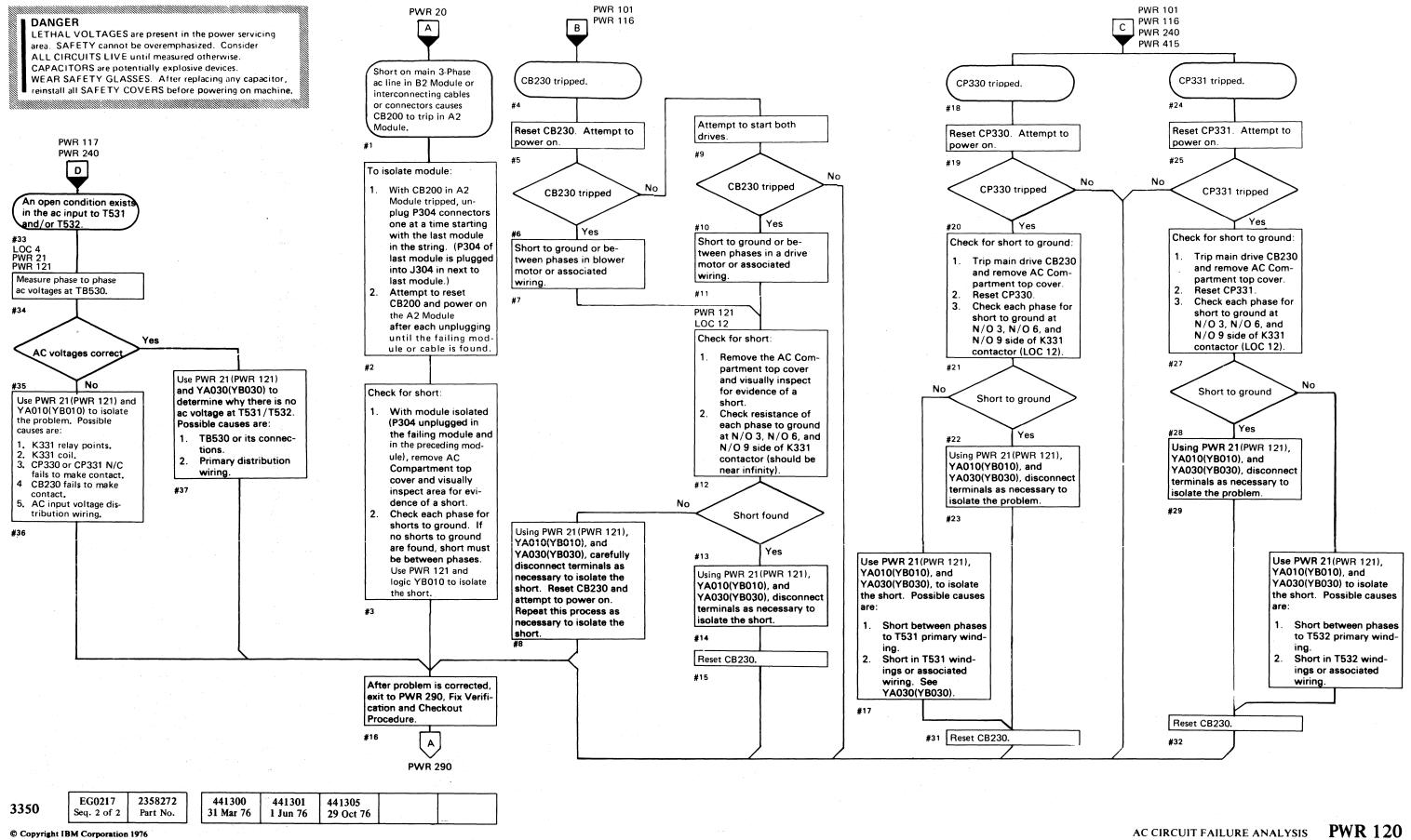
2358272 441300 441301 EG0217 441305 3350 31 Mar 76 Seq. 1 of 2 Part No. 1 Jun 76 29 Oct 76

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# POWER SUPPLY FAILURE ANALYSIS PWR 117

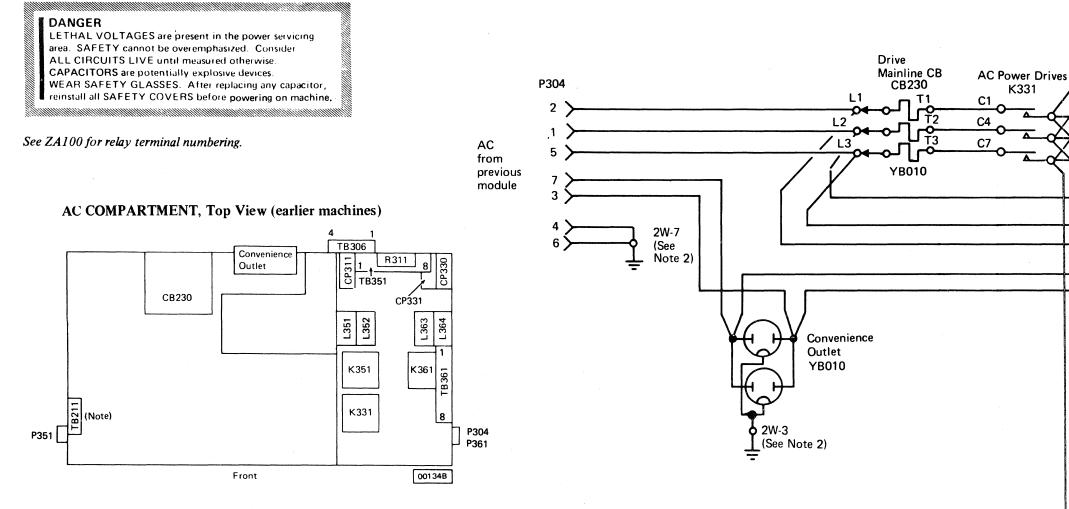
# **AC CIRCUIT FAILURE ANALYSIS**



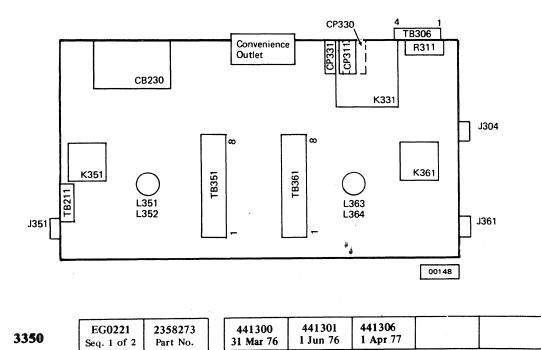
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# AC CIRCUIT FAILURE ANALYSIS PWR 120

# AC CIRCUIT DIAGRAM (B2)



# AC COMPARTMENT, Top View (later machines)



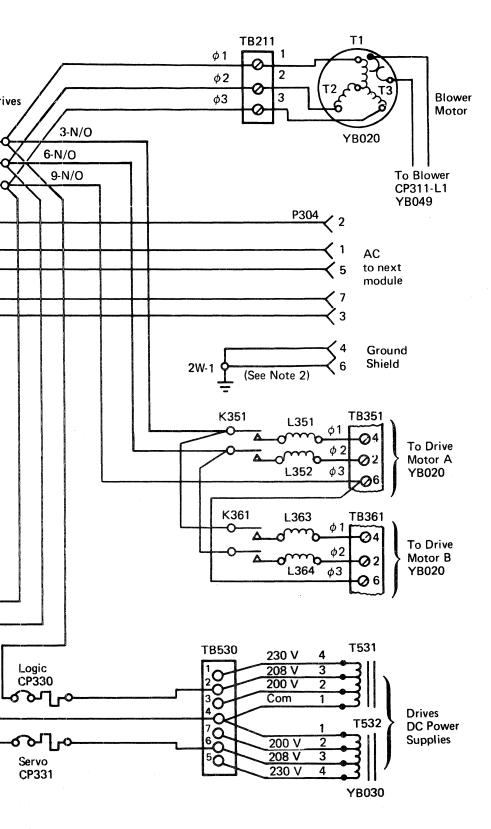
**Note 1**: In terminal block TB211, the terminals are numbered from top to bottom.

**Note 2:** 2W indicates leads tied to ground by sheet metal screws inside the AC Compartments.

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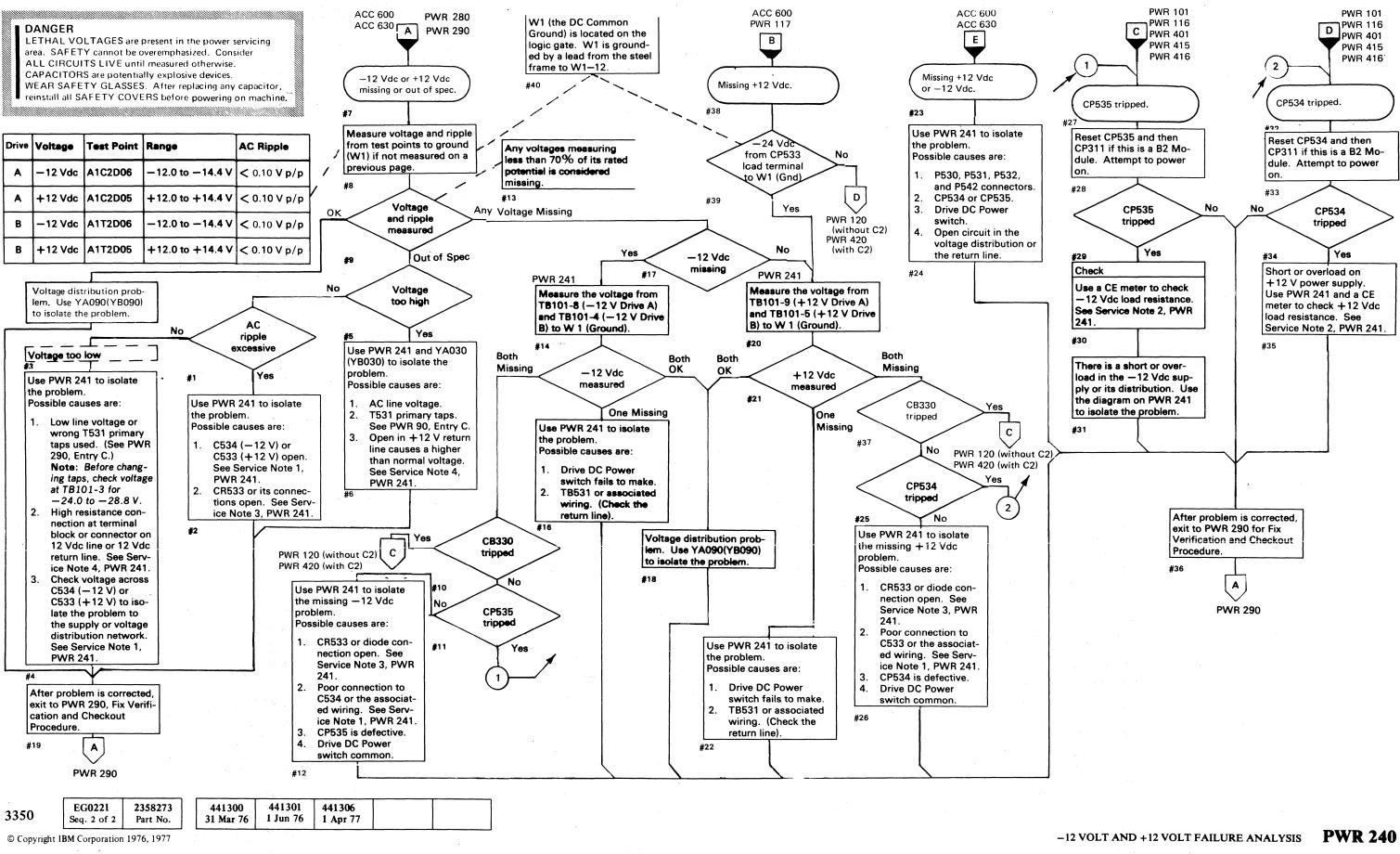
# AC CIRCUIT DIAGRAM (B2)

# **PWR 121**



# AC CIRCUIT DIAGRAM (B2) PWR 121

# -12 VOLT AND +12 VOLT FAILURE ANALYSIS



**PWR 240** 

# -12 VOLT AND +12 VOLT DIAGRAM

#### DANGER

- LETHAL VOLTAGES are present in the power servicing
- area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise
- CAPACITORS are potentially explosive devices.
- WEAR SAFETY GLASSES. After replacing any capacitor,
- reinstall all SAFETY COVERS before powering on machine.

#### See ZA100 for relay and contactor point location.

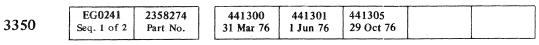
#### SERVICE NOTES

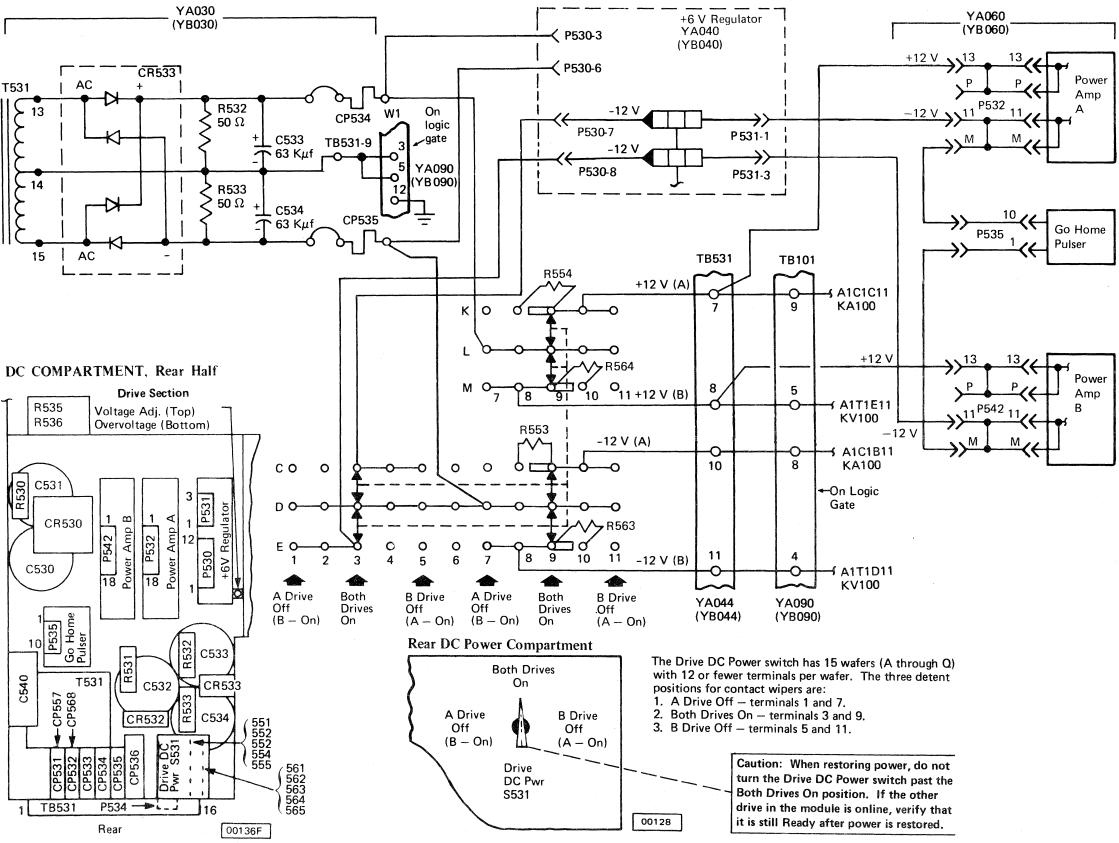
- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to R x 10.
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero. then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to R x 1 to speed up the process.
- 2. Load Resistance Check with CE Meter

#### Note: Meter slowly rises to value.

Supply	Scale	Gnd Lead	Test Point	Condition	Resistance
-12 V	Rx1	Common Load side $(+ \Omega)$ of CP535		CP535 Tripped	<b>&gt;</b> 60 ohm
				CP535 Reset	<b>&gt;</b> 20 ohm
+12 V	Rx1	Pos $(+ \Omega)$	Load side of CP534	CP534 Tripped	<b>&gt;</b> 30 ohm
	(+ 32) 0107334		CP534 Reset	<b>&gt;</b> 20 ohm	

- 3. Rectifier Check with CE Meter
  - a. Disconnect the leads to CR533 assembly.
  - b. With the meter set to R x 1, connect the common lead to one ac terminal and the other lead alternately to the + and - terminal, measure the resistance which should be from 5 to 15 ohms.
  - c. Set the meter to R x 1 and measure the resistance between the two ac terminals. The resistance should be near infinity.
- 4. An open 12 Vdc return line to the T531 12 V secondary center tap causes the -12 Vdc to drop below and the +12 Vdc to rise above specifications.
- 5. The power amp -12 volts is controlled by a transistor switch on the +6 volt regulator board. A drop in the +24 Vdc sequence supply immediately cuts off the -12 volts to the power amps.

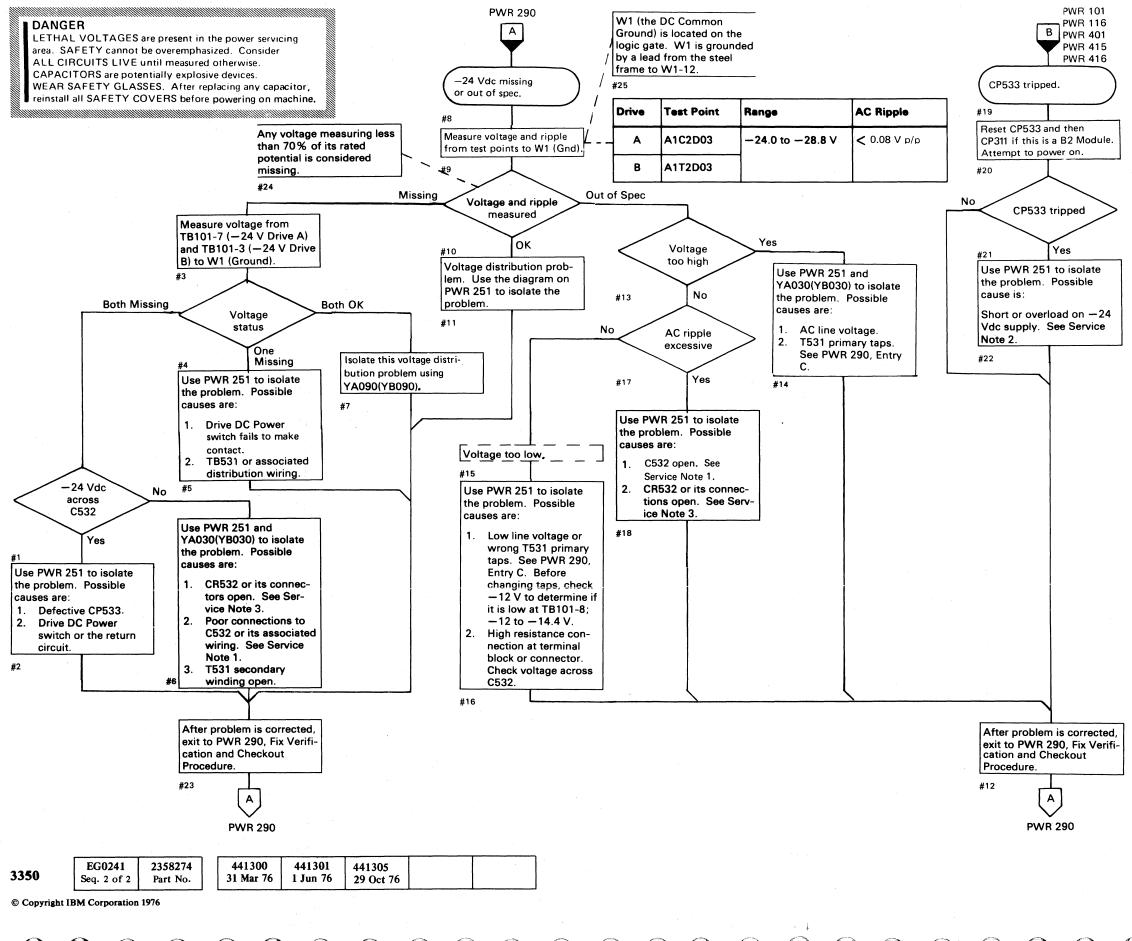






-12 VOLT AND +12 VOLT DIAGRAM PWR 241

# -24 VOLT FAILURE ANALYSIS



-24 VOLT FAILURE ANALYSIS

**PWR 250** 

#### SERVICE NOTES

- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to R x 10.
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to R x 1 to speed up the process.
- 2. Load Resistance Check with CE Meter

Supply	Scale	Gnd Lead	Test Point	Condition	Resistance		
		With Drive DC Power switch set to both on					
-24 V	Rx10	x10 Common $(+ \Omega)$	CP533 Load	CP533 Tripped	>750 ohm		
		(+ 52)	Term.	CP533 Reset	> 75 ohm		
		With Drive DC Power switch set to one off.					
-24 V	V Rx10 Common (+Ω)	CP533 Load	CP533 Tripped	>1500 ohm			
			Term.	CP533 Reset	> 75 ohm		

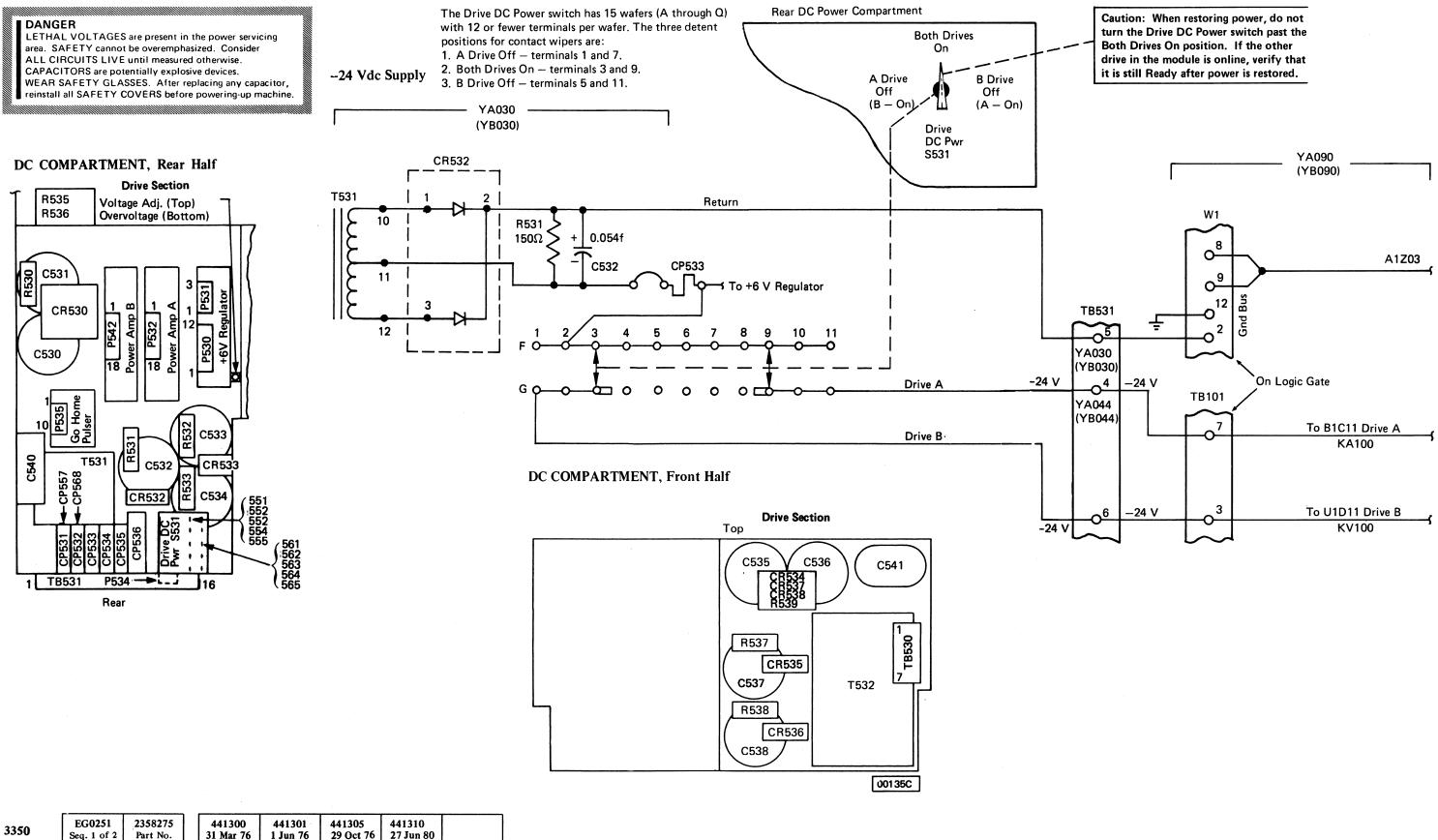
#### 3. Rectifier Check with CE Meter

- a. Disconnect the leads to CR532 assembly.
- b. With the meter set to R x 1, measure the forward resistance which should be from 5 to 15 ohms.
- c. Set the meter to R x 1000 and reverse the meter leads. The resistance should be near infinity.

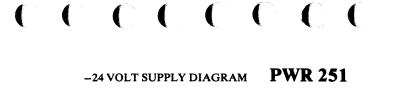
# -24 VOLT FAILURE ANALYSIS **PWR 250**

# -24 VOLT SUPPLY DIAGRAM

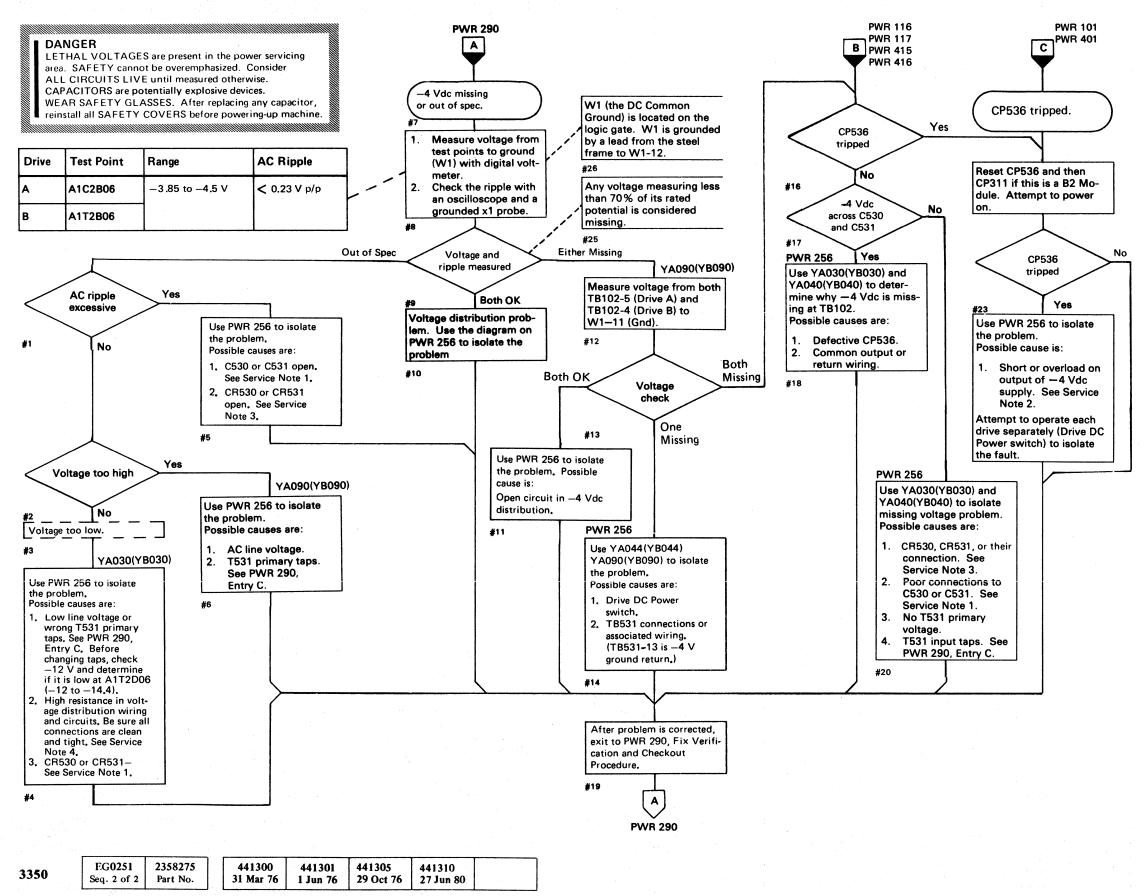
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# -4 VOLT FAILURE ANALYSIS



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-4 VOLT FAILURE ANALYSIS PWR 255

#### **SERVICE NOTES**

- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to R x 10.
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to R x 1 to speed up the process.

2. Load Resistance Check with CE Meter

Supply	Scale	Gnd Lead	Test Point	Condition	Resistance
-4 V	Rx1	1 Common CP536 $(+ \Omega)$ Load side		CP536 Tripped	<b>&gt;</b> 15 ohm
		17 201	L000 3106	CP536 Reset	<b>&gt;</b> 10 ohm

- 3. Rectifier Check with CE Meter
  - a. Remove heat-sink assembly from top of C530 and C531. The rectifier leads are soldered on. Use the heat-sink as the diode terminal.
  - b. With the meter set to  $R \times 1$ , measure the forward resistance which should be from 5 to 15 ohms.
  - c. Set the meter to R x 1000 and reverse the meter leads. The resistance should be near infinity.
- 4. The voltage across C530 and C531 should normally measure about 0.3 to 0.6 volts higher than the voltage measured at TB102-5/6 or TB102-3/4. Other typical voltages measurements are: (Refer to PWR 256)

A	to	B	0.06	volts	(Dri	ves A & B)
B	to	Ĉ	0.07	volts	(Dri	ves A & B)
С	to	D	0.15	volts	(Dri	ve A)
C	to	e	0.15	vo/ts	(Dri	ve B)
D	to	Ø	0.11	volts	(Dri	ve A)
Ø	to	G	0.11	vo/ts	(Dri	ve B)
0	to	A1C21	B <i>06</i>	0.02	vo/ts	(Drive A)
G	to	A1T21	B <i>06</i>	0.02	volts	(Drive B)
0	to	J	0.06	volts	(Dri	ves A & B)
0	to	ß	0.12	volts	(Dri	ves A & B)
Ø	to	A1C2I	D <b>08</b>	0.02	volts	(Drive A)
ß	to	A1T21	D <b>08</b>	0.02	volts	(Drive B)

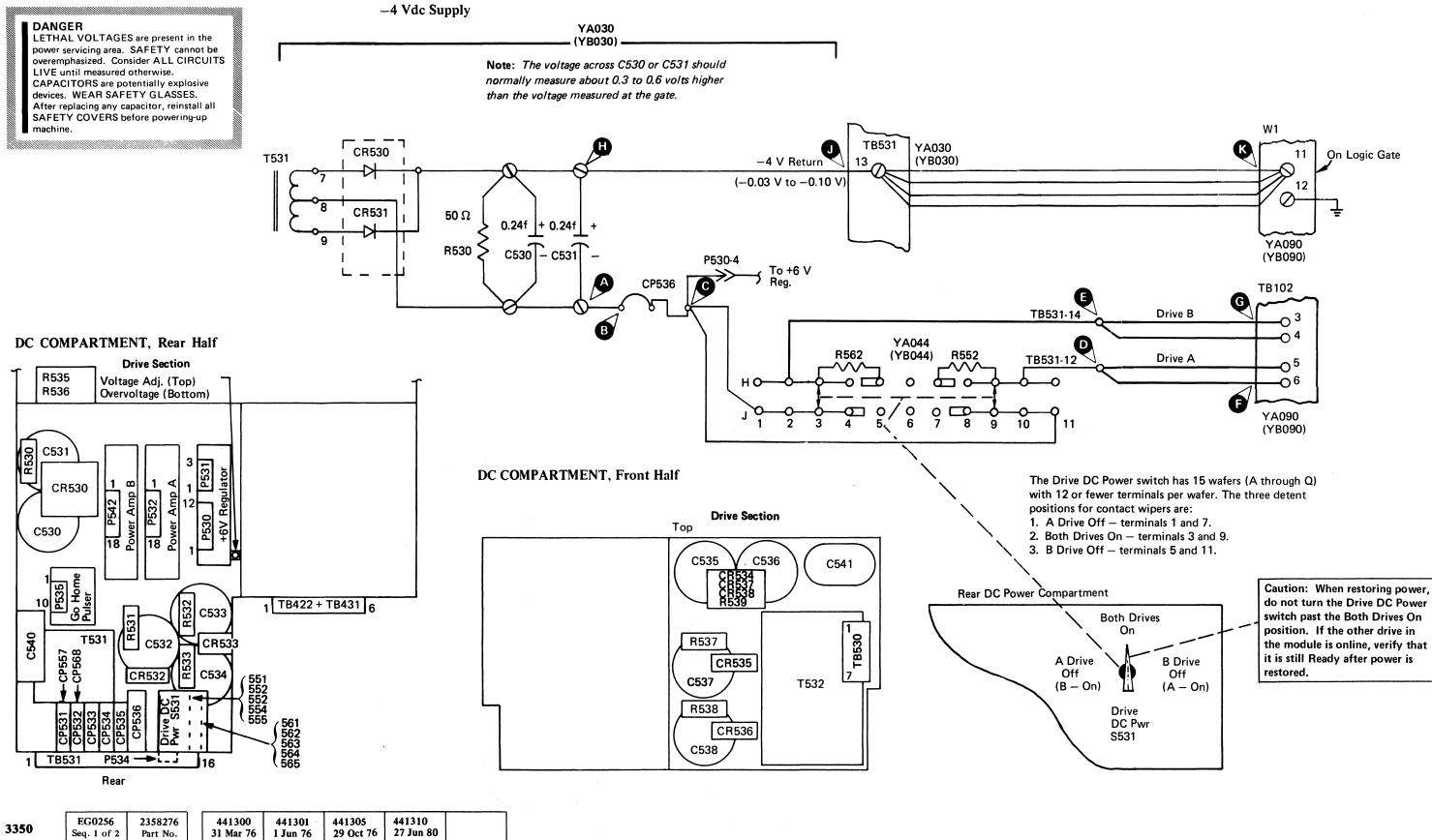
If voltage drops exceed these typical examples and voltage as measured at card is still below specification, recheck connections and/or replace parts as required.

-4 VOLT FAILURE ANALYSIS

**PWR 255** 

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# -4 VOLT SUPPLY DIAGRAM

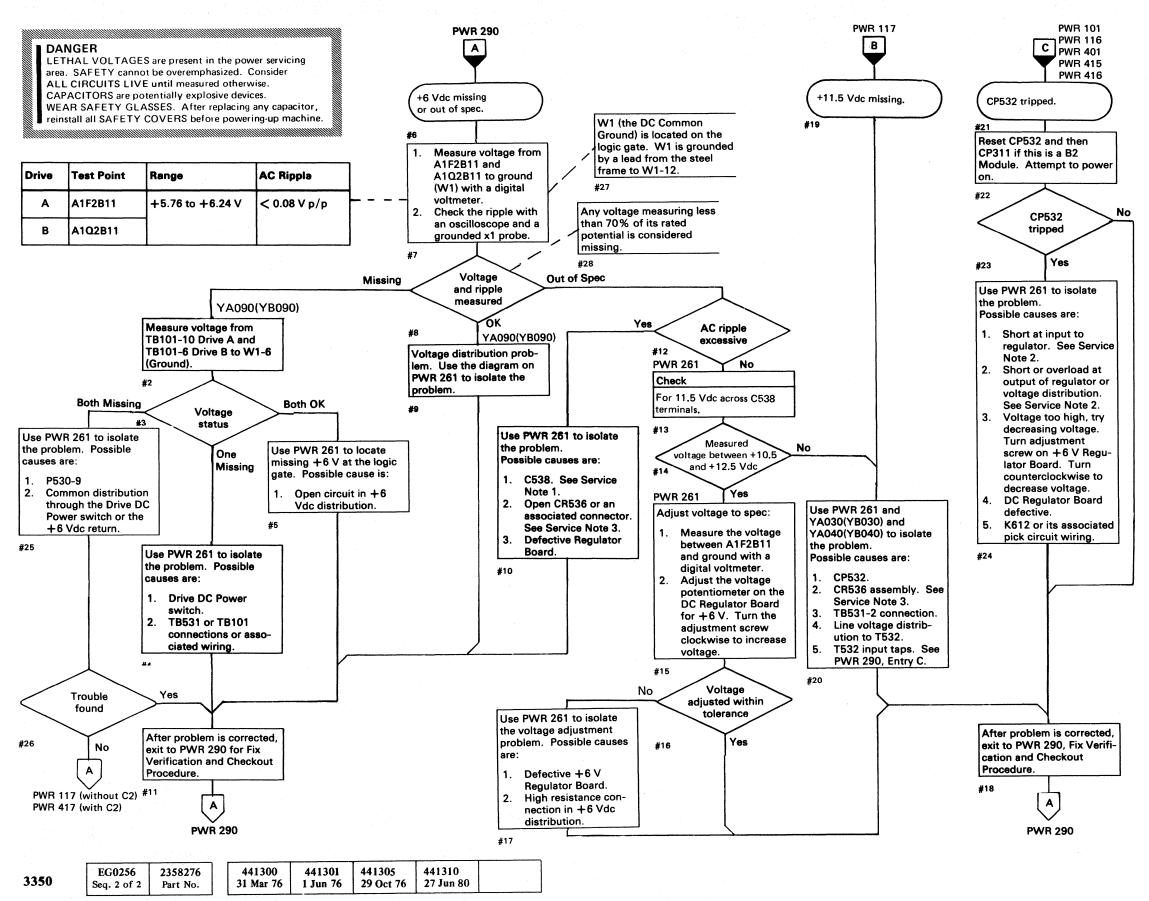


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#### **PWR 256** -4 VOLT SUPPLY DIAGRAM

do not turn the Drive DC Power switch past the Both Drives On position. If the other drive in the module is online, verify that it is still Ready after power is

# +6 VOLT FAILURE ANALYSIS



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#### +6 VOLT FAILURE ANALYSIS

# **PWR 260**

#### **SERVICE NOTES**

- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to R x 10.
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to R x 1 to speed up the process.

Supply	Scale	Gnd Lead	Test Point	Condition	Resistance
+6V	Rx10	Common (+ Ω)		CP532 Tripped CP532 Reset	>400 ohm > 30 ohm
		With Drive DC Po	ower switch se	t to both on.	
		W1	TP7 Seq Bd B	CP532 Reset	> 15 ohm
		With Drive DC Po	ower switch to	one off.	<b></b>
		W1	TP7 Seq Bd B	CP532 Reset	> 20 ohm

2. Load Resistance Check with CE Meter

#### 3. Rectifier Check with CE Meter

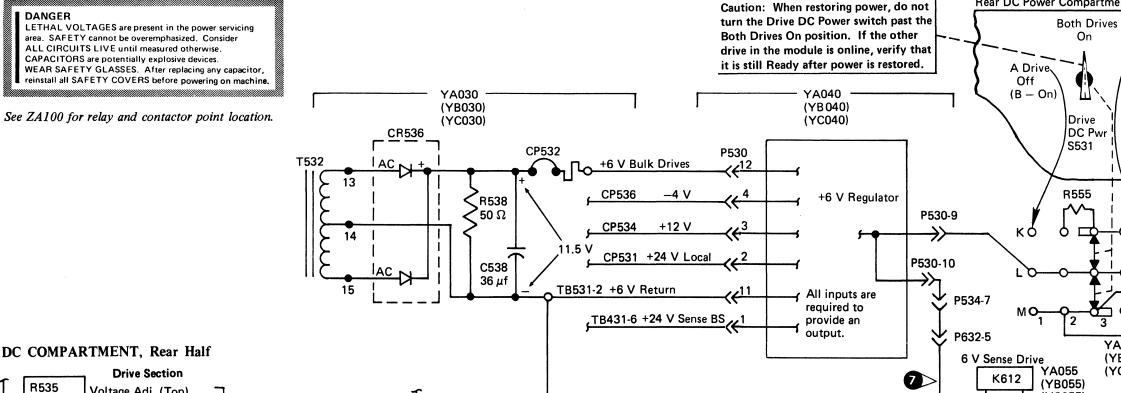
- a. Disconnect the leads to CR536 assembly.
- b. With the meter set to  $R \times 1$ , measure the forward resistance which should be from 5 to 15 ohms.
- c. Set the meter to R x 1000 and reverse the meter leads. The resistance should be near infinity.

# +6 VOLT FAILURE ANALYSIS **PWR 260**

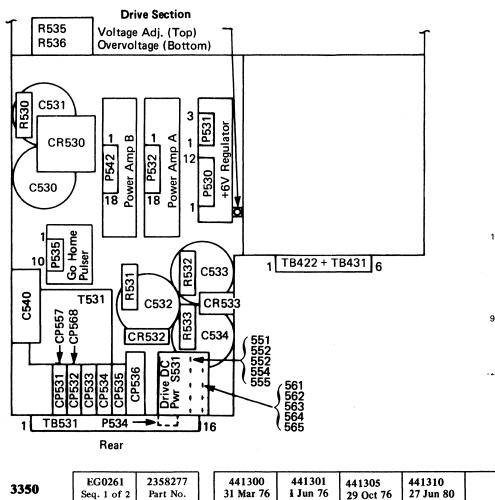
## +6 VOLT REGULATOR DIAGRAM

#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering on machine.

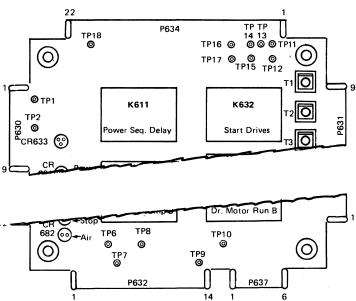


#### DC COMPARTMENT, Rear Half

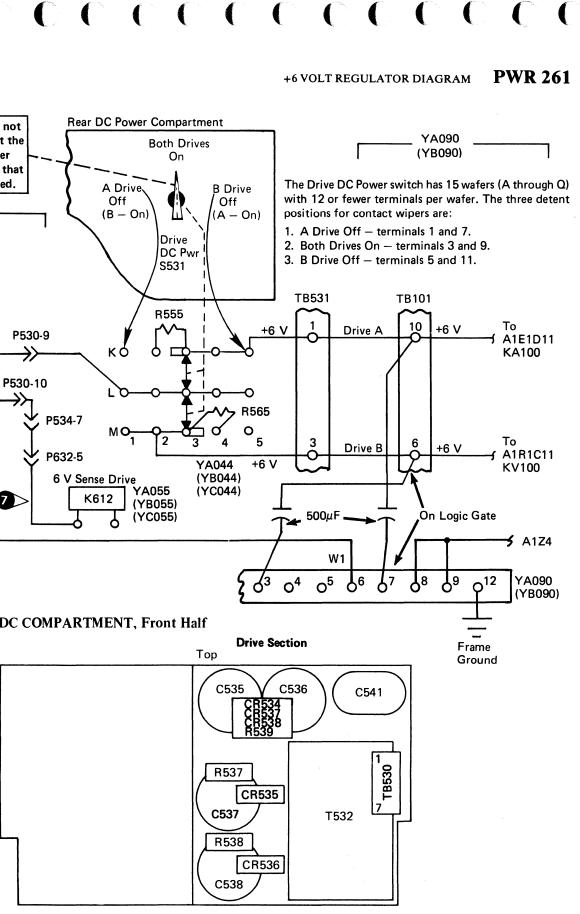


**SEQUENCE PANEL** 

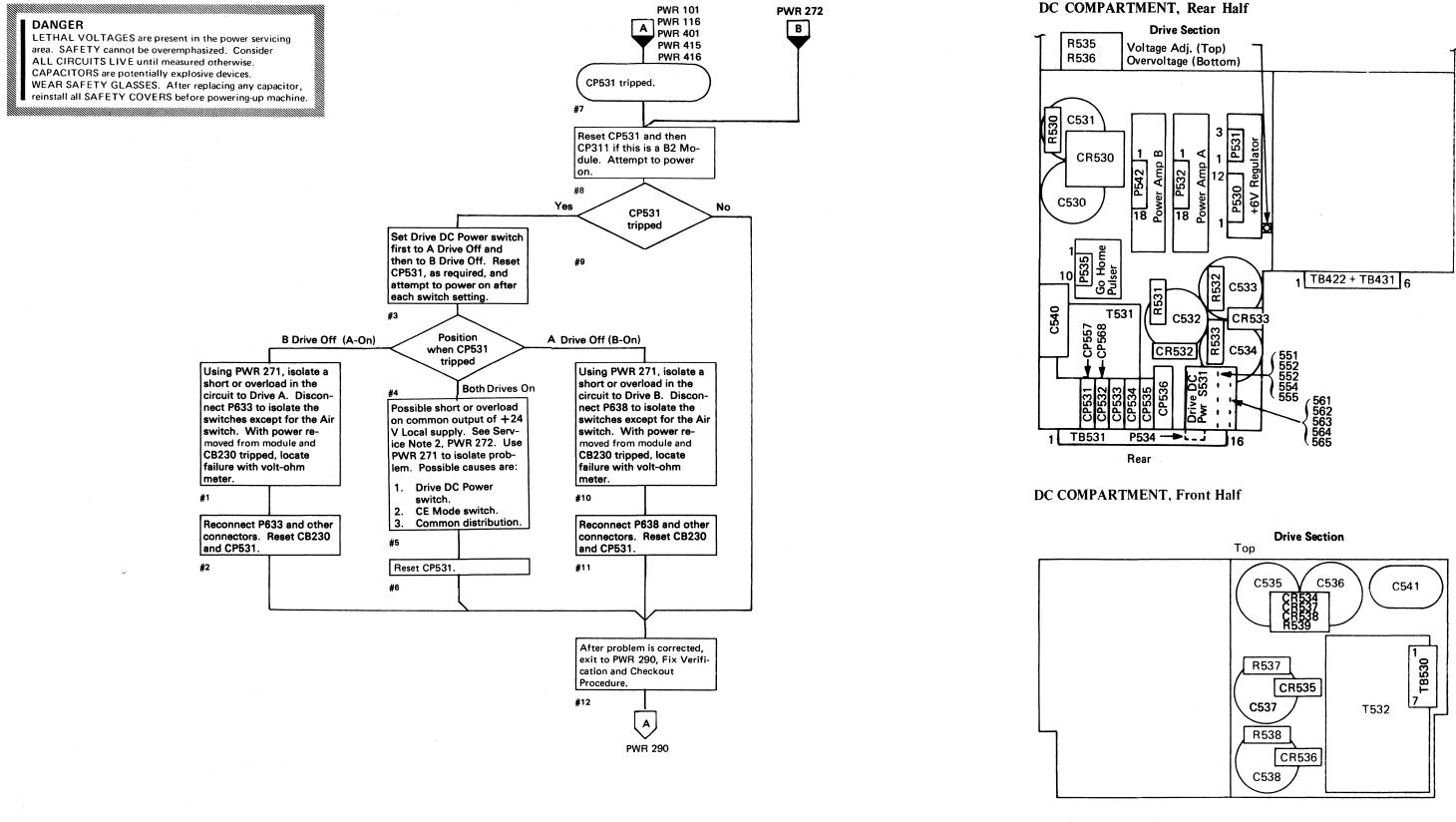
#### **Board B**



#### DC COMPARTMENT, Front Half



## +24 VOLT (Local) FAILURE ANALYSIS



3350	EG0261 Seq. 2 of 2	2358277 Part No.	441300 31 Mar 76	441301 1 Jun 76	441305 29 Oct 76	441310 27 Jun 80	

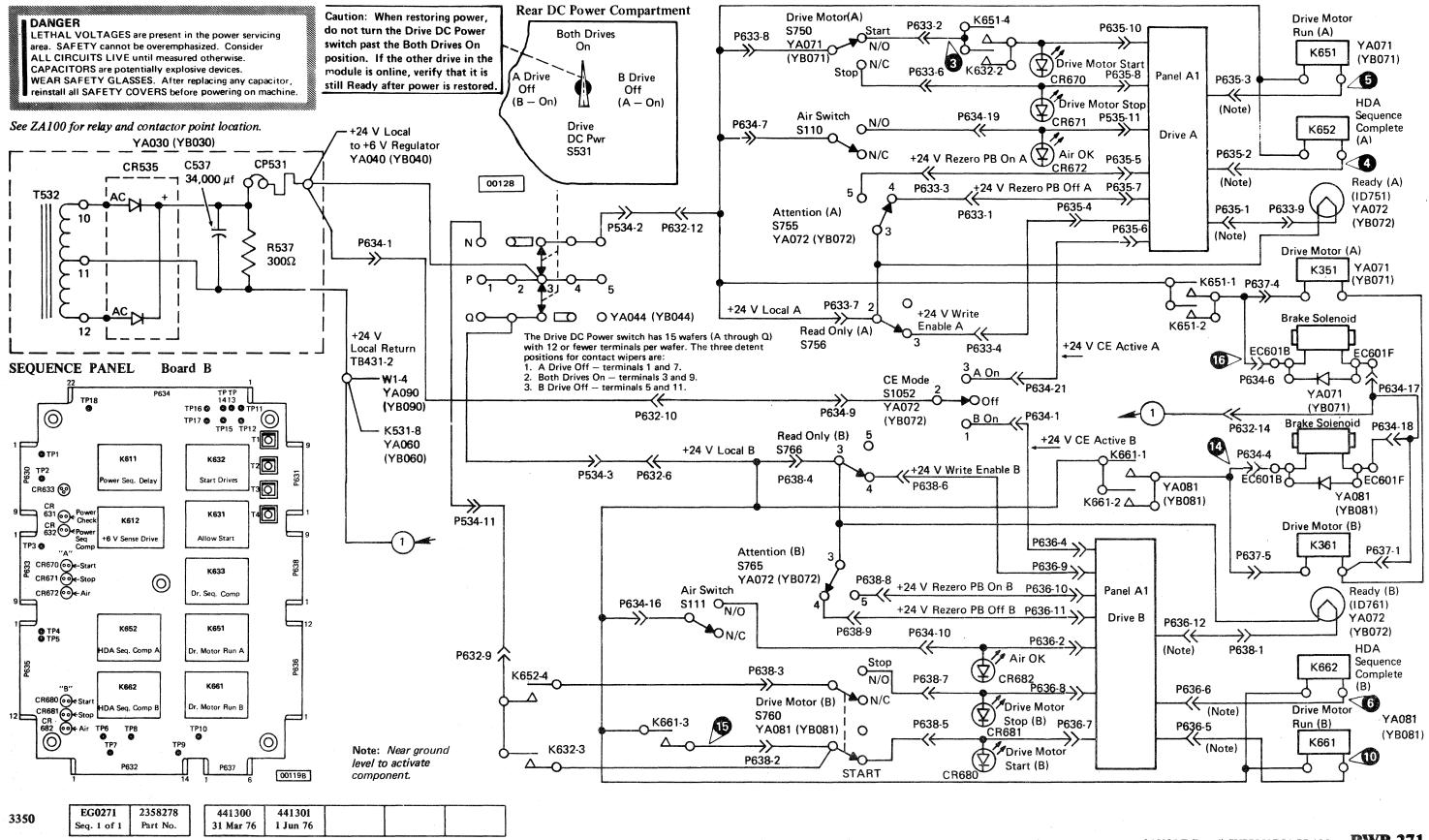
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### +24 VOLT (Local) FAILURE ANALYSIS PWR 270

+24 VOLT (Local) FAILURE ANALYSIS **PWR 270** 

 $\bigcirc$ 

## +24 VOLT (Local) SUPPLY DIAGRAM



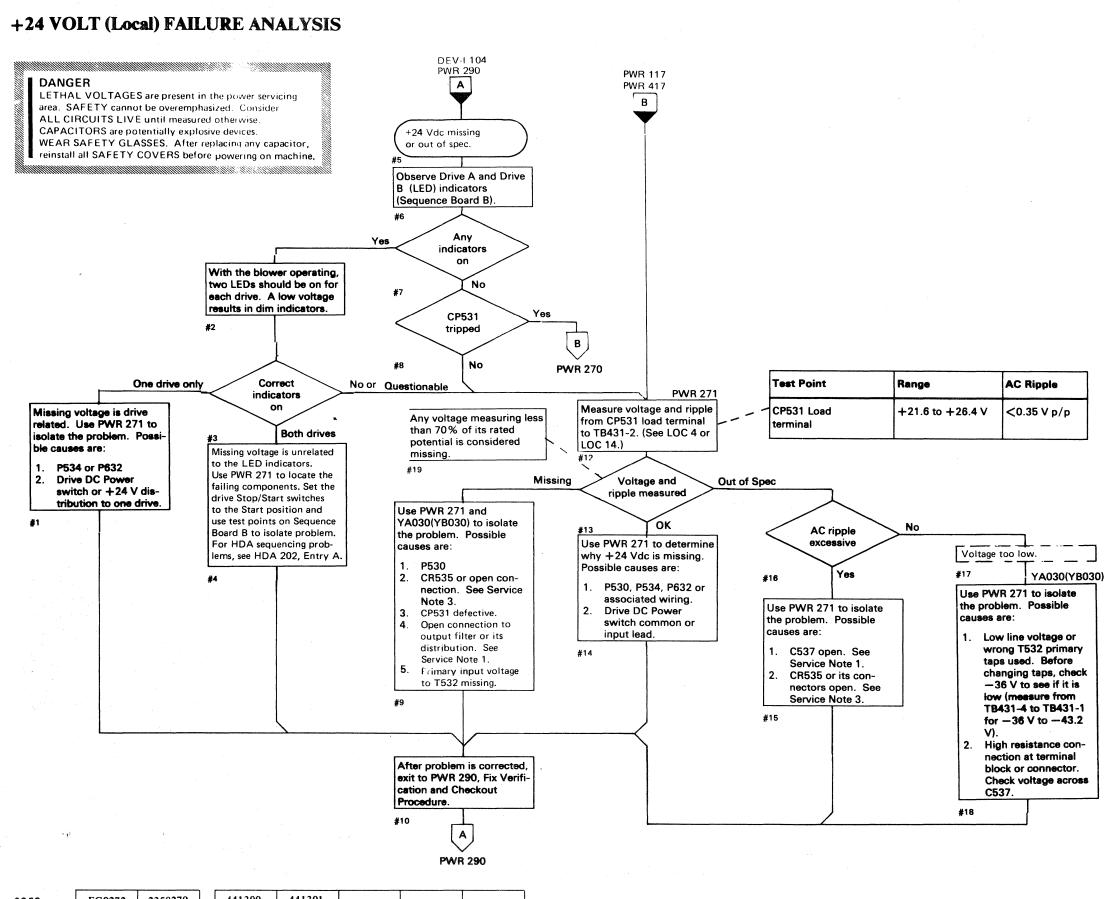
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**PWR 271** 

+24 VOLT (Local) SUPPLY DIAGRAM PWR 271





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+24 VOLT (Local) FAILURE ANALYSIS **PWR 272** 

#### SERVICE NOTES

- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to R x 10.
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to R x 1 to speed up the process.
- 2. Load Resistance Check with CE Meter. Drive DC Power switch in the Both Drives position.

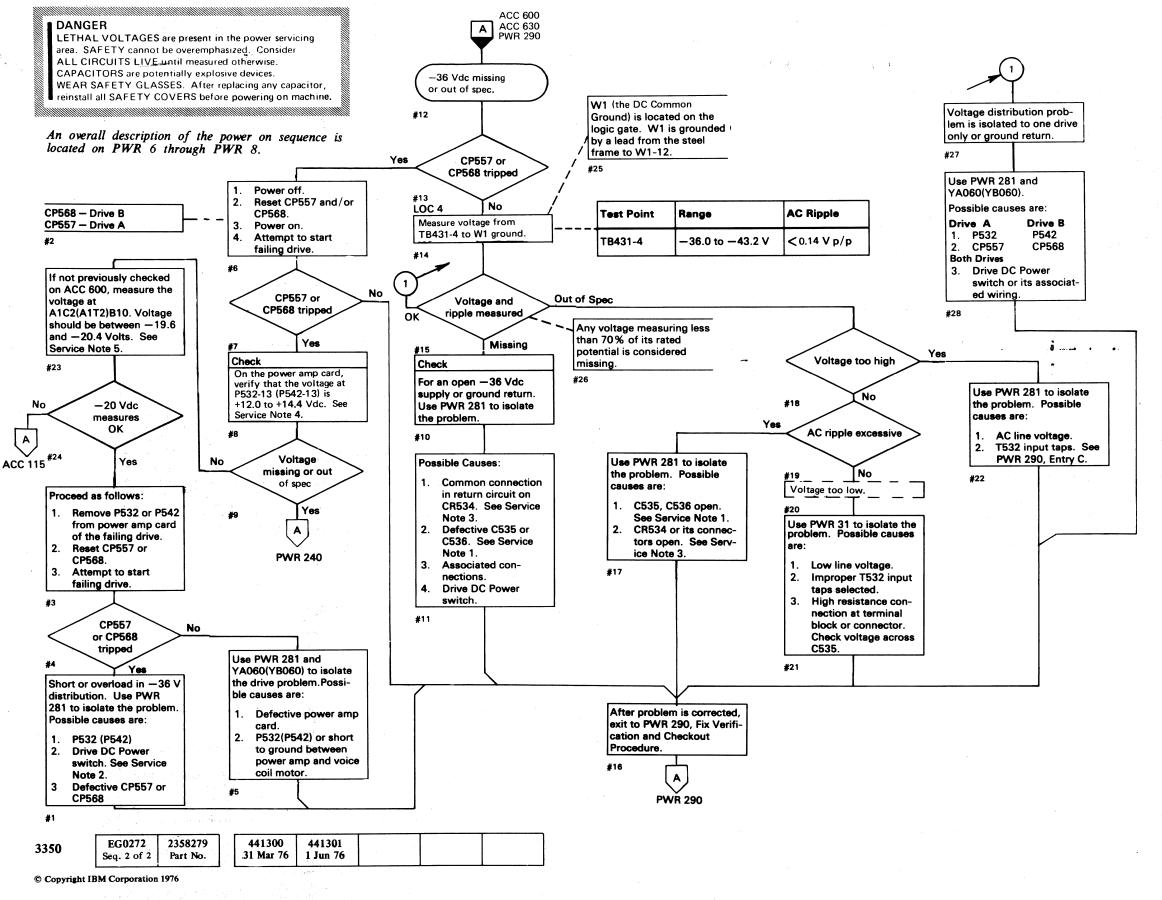
Supply	Scale	Gnd Lead	Test Point	Condition	Resistance
+24 V	Rx1	Common $(+ \Omega)$	Load side of CP531	CP531 Tripped	> 100 ohm
				CP531 Reset	> 15 ohm

3. Rectifier Check with CE Meter

- a. Disconnect the leads to CR535.
- b. With the meter set to  $R \ge 1$ , measure the forward resistance of each diode which should be from 5 to 15 ohms.
- c. Set the meter to R x 100 and reverse the meter leads. The resistance should be near infinity.

+24 VOLT (Local) FAILURE ANALYSIS

## -36 VOLT FAILURE ANALYSIS



-36 VOLT FAILURE ANALYSIS **PWR 280** 

#### **SERVICE NOTES**

- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to R x 10.
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to R x 1 to speed up the process.
- 2. Load Resistance Check with CE Meter

Supply	Scale	Gnd Lead	Test Point	Condition	Resistance
—36 V	Rx10 Rx1	Common $(+ \Omega)$	CP568	CP557/CP568 Tripped CP557/CP568 Reset	> 750 Ω > 30 Ω

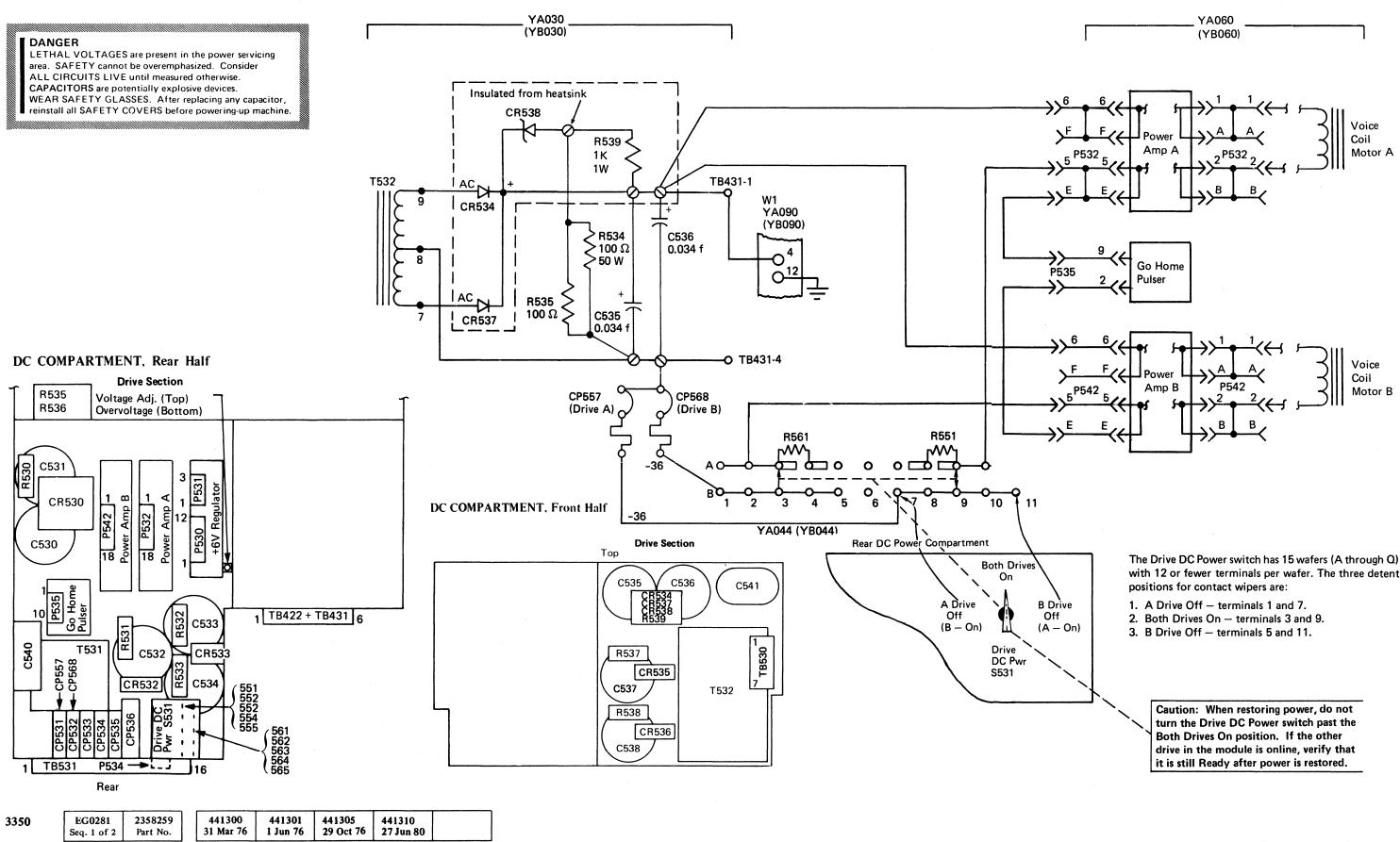
- 3. Rectifier Check with CE Meter
  - a. Disconnect the leads to the CR534 assembly.
  - b. With the meter set to R x 1, measure the forward resistance which should be from 5 to 15 ohms.
  - c. Set the meter to R x 1000 and reverse the meter leads. The resistance should be near infinity.
- 4. +12 Vdc missing at the power amplifier(s) causes an overload on the -36 Vdc supply which may cause CP557 and/or CP568 to trip. Measure voltages at P532-13 and P542-13 shown on PWR 281.
- 5. If -20 V is missing at A1C2(A1T2)B10, an overload is placed on the -36 Vdc supply which may trip CP557 and/or CP568.

## -36 VOLT FAILURE ANALYSIS **PWR 280**

## -36 VOLT SUPPLY DIAGRAM

#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise CAPACITORS are potentially explosive devices.



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## -36 VOLT SUPPLY DIAGRAM PWR 281

with 12 or fewer terminals per wafer. The three detent

-36 VOLT SUPPLY DIAGRAM PWR 281

## FIX VERIFICATION AND VOLTAGE CHECKS

## PWR Α

#### **FIX VERIFICATION AND CHECKOUT** PROCEDURE

Complete the following checklist to ensure that the machine problem has been corrected. If a check cannot be completed, go to the referenced MIM page for aid in making a fix.

Note 1: It is not always necessary to check each step. Use your judgement in skipping all unneeded steps.

- 1. Set Power Mode switch to Local, then power off the string by placing the Power Off/Enable switch to Off. If the string does not power off, go to PWR 22, Entry C (controller).
- 2. Restore the string to normal operating conditions. (Remove all diagnostic jumpers and replace wiring, connectors, or parts that were removed.)
- 3. Power-on the string, then set Power Mode switch to Remote.
- 4. Verify that the Power Sequence Complete (LED) and String Power Sequence Complete (LED) indicators and the blowers in each module all turn on. If not, go to PWR 9, Entry D (controller).
- 5. Turn on the A and B Drive Start switches on the problem module(s). Verify that both Ready lamps turn on. If not, go to START 100, Entry B.
- 6. Check power supply voltages as shown in the Voltage Check Chart (this page). (See Note 2.)
- 7. Examine the DC Compartment air filter and clean or replace as necessary.
- 8. Replace all covers.
- 9. Run a string check. (See START 110.)
- 10. Go to START 500, Entry A.

PWR В

### **VOLTAGE CHECKS**

Note 2: The following checks should be made with the drives stopped or Ready but with no Seek or Read/Write operations in progress.

#### **DC Voltage Checks**

With a digital voltmeter, measure each dc voltage in the order listed in the Voltage Check Chart. Only one voltage can be directly adjusted (+6 V)to the drives logic board (A1). If adjustments are necessary, the rear DC Compartment top cover must be removed. Be certain that only the voltage adjustment potentiometer on the regulator card is adjusted. (See PWR 261.) The overvoltage potentiometer is adjusted at the plant and should not be changed. Turn the voltage adjustment potentiometer clockwise to increase the voltage.

All power supplies, except the one mentioned above, have no output voltage adjustment. The only adjustment possible is to change the transformer primary input taps. The T531 primary taps determine the ac input for the -12 V, +12 V, -4.0 V, and -24 V supplies. The T532 primary taps determine the ac input for the -36 V, +11.5 Vand +24 V Local supplies. If any of these supplies are not within specification, check the main 3-phase ac power and ensure that the machine is wired for the correct input voltage, as shown in the Transformer Primary Input Tap Wiring Chart on this this page.

If the voltage checks are not completed successfully, exit to the appropriate MAP indicated in the Voltage Check Chart.

If the voltage checks are completed successfully, but this page is entered because of a known dc voltage problem, the problem must be in the voltage distribution. Use the appropriate diagram listed in the chart to isolate the problem.

#### **AC Ripple Checks**

If the peak-to-peak ac ripple exceeds the maximum listed in the chart, it is likely that a power supply part has failed.

To measure the ac ripple, use the ac input on a scope having a 0.01 volt per centimeter range and a X1 probe placed on the test points shown in the chart. Place the probe ground on any convenient ground point.

If the ac component is greater than the maximum listed, exit to the appropriate MAP referenced in the chart to correct the problem.

> W1 (the DC Common Ground) is located on the logic gate. W1 is grounded by a lead from the steel frame to W1-12.

## **VOLTAGE CHECK CHART**

DC Supply	Test Points	<ul><li>/ Tolerance (Volts)</li></ul>	Adjustment	Logic Page	Maximum AC Ripple	Diagram	Page Entry
+24 V Local	CP531 Load Terminal to W1 Ground Bus	+21.6 to +26.4	None*	YA030 YB030	0.35 V p/p	PWR 271	PWR 272, A
-24 V	A1C2D03 (Dr A)/ A1T2D03 (Dr B) to A1K2D08	-24.0 to -28.8	None*	YA090 YB090	0.08 V p/p	PWR 251	PWR 250, A
+12 V	A1C2D05 (Dr A)/ A1T2D05 (Dr B) to A1K2D08	+12.0 to +14.4	None*	YA090 YB090	0.10 V p/p	PWR 241	PWR 240, A
—12 V	A1C2D06 (Dr A)/ A1T2D06 (Dr B) to A1K2D08	-12.0 to -14.4	None*	YA090 YB090	0.10 V p/p	PWR 241	PWR 240, A
-4 V	A1C2B06 (Dr A)/ A1T2B06 (Dr B) to A1K2D08	-3.85 to -4.5	None*	YA090 YB090	0.23 V p/p	PWR 256	PWR 255, A
+6 V Reg	A1F2B11 (Dr A)/ A1Q2B11 (Dr B) to A1F2D08/ A1Q2D08	+5.76 to +6.24 (Adjust to 6.0)	Turn screw clockwise to in- crease voltage	YA090 YB090	0.08 V p/p	PWR 261	PWR 260, A
-36 V	TB431-4 to W1 Ground Bus	-36.0 to -43.2	None*	YA030 YB030	0.14 V p/p	PWR 281	PWR 280, A

\* Check transformer primary taps and change to match available voltage.

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FIX VERIFICATION AND VOLTAGE CHECKS **PWR 290** 



#### **TRANSFORMER PRIMARY INPUT TAP** WIRING CHART

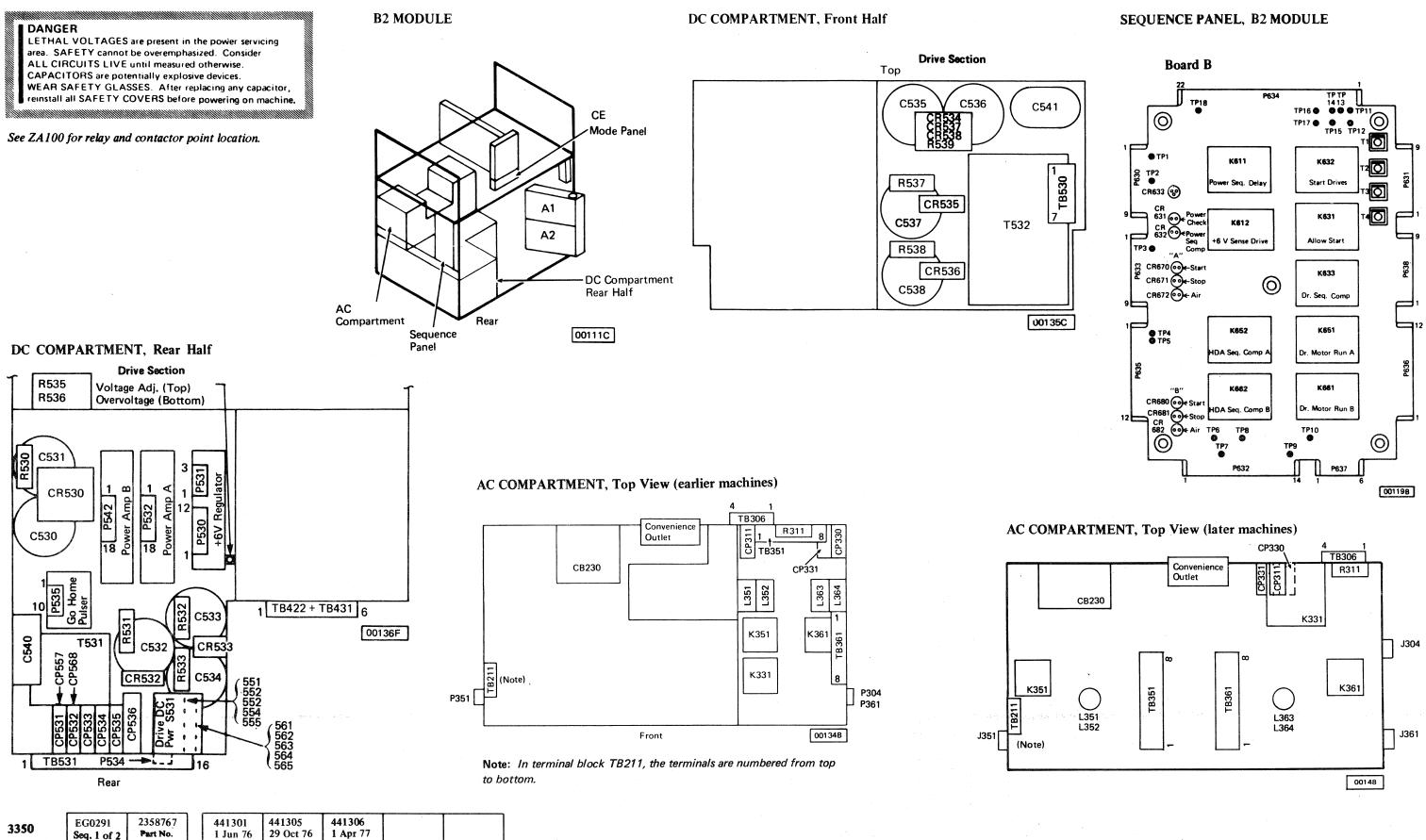
Voltage (YB030)	TB530 YA030 (YB030) Note 4
200 V	Phase A to TB530-3 Phase C to TB530-7
208 V	Phase A to TB530-2 Phase C to TB530-6
230 V	Phase A to TB530-1 Phase C to TB 530-5

Note 3:	Before ch	langing pi	rimary	taps,	check	another
dc outpi	it voltage	that uses	the san	ne pri	imary '	winding.

Note 4: Phase B to TB530-4 is common to both transformers.

FIX VERIFICATION AND VOLTAGE CHECKS **PWR 290** 

## **COMPONENT AND TEST POINT LOCATIONS**



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**PWR 291** 

#### COMPONENT AND TEST POINT LOCATIONS

## **POWER SUPPLY SEQUENCE**

### **INTRODUCTION**

Power for the entire disk storage string is routed through the A2 (control) Module. The ac power (three phase, 208 V, 60 Hz) is controlled by the sequencing circuits in the A2 Module. (See PWR 307.)

Line filtering is accomplished by a capacitor between each phase of the 208 Vac connected at the output of CB200.

A phase-detection circuit containing resistance, capacitance, and an ac relay (K202) is used to detect improper power phasing; this is done to ensure proper rotation of the blower and drive motors. Relay K202 picks only if the main ac phasing is correct. If phasing is incorrect, K202 fails to pick and the power-on sequence is prevented.

With three-phase power to the 3350 string, T201 is activated. The secondaries feed the convenience outlets (115 V) and the +24 V Bootstrap (BS) supply. The bootstrap voltage picks sequence and control relays in all modules.

All modules have a drive power supply. The control modules (A2 and C2) each have an additional supply for the controller board. The controller supply in the A2 Module consists of a +24 V power sequence, a 115 Vac convenience outlet, and a -4 Vdc and +6 Vdc supply (T420) for the A2 logic board. The controller supply in the C2 Module consists of only the -4 Vdc and +6 Vdc supply (T420), which supplies the A2 logic board. The drive power supply for each module (A2, B2, or C2) uses two transformers (T531 and T532) and associated components to provide power for the A1 logic board, the servo power amplifiers, and the +24 Vdc Local for relay operation.

Power-on sequencing is initiated in the A2 Module and continues through the last module on the string.

### **POWER-ON SEQUENCE**

References are to the Power Supply Sequence diagram on PWR 307 and the sequence chart on PWR 308.

#### Controllers (A2 and C2)

- 1. Three-phase power is supplied from the customer's receptacle to active the +24 V Bootstrap Supply 1 and the 115 Vac outlets 2. The EPO relay (K203) must also be picked to provide 115 Vac at the outlets. K202 (Phase Rotation Detection) 3 picks if the phase is correct.
- 2. In the A2 Module, the Power Pick line or Power On switch 13 picks K601 (Subsystem Sequence Start) 5 if the Power Off/Enable switch is in the Enable position 4. The Controller AC contactor (K221) 8, Blower AC contactor (K222), and the Gate/Blower Thermal Sense relay (K606) are picked through CP Aux points and the gate thermal when K601 is picked.

- 3. With K601 picked, K201 (Subsystem Power) 6 is picked, the Power On lamp is on, and the +24 V BS Sequence line is active. The +24 V BS Sequence line picks two contactors and a relay in the C2 Module; Controller AC contactor (K221) 11, Blower AC contactor (K222), and Gate/Blower relay (K606). K201 makes ac power available through the K222 relays of both modules to their blowers, and through the K221 relays of both modules to the power supplies for each A2 logic board 9 and 12.
- 4. The +24 V Power Sequence line is also activated by K601 to pick the AC Power Drives contactor (K331) 23 and start the one-second delay in the pick of Power Sequence Delay relay (K611) 16.
- 5. The controller power-on sequence is now complete except for picking the String Power Sequence Complete relay (K603) 14 by the Power Sequence Complete line. This line is activated through a jumper (T4 to T3) 27 in the last module of the string when its Power Sequence Delay relay (K611) is picked. K603 signals the controlling storage control to advance to the next subsystem string. If the Service Bypass switch 19 of any module is on, the K611 does not need to be picked for string power sequencing.

#### Drives

The drive power section components, labels, and numbers of each module are identical. This means that K351 24 is the drive motor contactor for Drive A whether it is located in an A2, B2, or C2 Module. There are two exceptions, however. The first is that the blower 10 in the A2 Module receives power when contactor K201 is picked while contactor K331 activates the blower **22** in the B2 Module. The C2 blower also receives power when  $\overline{K}201$  is activated. The second exception is the application of the series of auxiliary CP points 20 and 21 that pick K331. Both exceptions result because blowers must be turned on when power is applied to the logic boards. The arive power-on sequence for each module is:

- 1. The +24 V Power Sequence line picks the AC Power Drives contactor (K331) 23 through the Off position of the Service Bypass switch and through the CP auxiliary point and Logic Gate Thermal points.
- 2. Contactor K331 activates the dc power supplies and starts the blower motor in the B2 Module. Three-phase power is also available to the drive motor contactors (K351 and K361) 24.
- 3. DC power from the supplies is distributed to the drive logic panel 28 through CPs, the +6 V Regulator, and the Drive DC Power switch 25. The three-position Drive DC Power switch permits removal of dc power to one drive while the other continues to operate.

4. The Power Sequence Delay relay (K611) 16 picks one second after K331 is picked and from the same source of voltage. With K611 picked, the Power Sequence Complete (LED) 17 is turned on and +24 V Power Sequence is sent to the next module.

In the next module, drive power sequencing begins by picking K331 and K611. In the last module of the string, a jumper between T4 and T3 27 routes the +24 V Power Sequence Complete line to pick the String Power Sequence Complete relay (K603) 14. The K603 points signal the storage control to advance to the next string (if used). Other points of K603 provide +24 V Drive Sequence and +24 V Poll lines 29 that with the +24 V Bootstrap line, start and stop the spindle drive motors.

The Power Sequence Complete (LED) is turned on if the string is active even when the Service Bypass switch is in the On position. The module is not sequenced on but K611 16 is picked and K612 26 is not picked. With K612 (6 V Sense) dropped, the K612-1 points turn on the Power Check (LED) 18.

#### **POWER-OFF SEQUENCE**

#### String

The entire string is powered off if the hold to the Subsystem Sequence Start relay (K601) is removed.

- 1. The hold to K601 is through the Power Off/Enable switch in the Enable position 4, K603-1 points 14, K601-4 points, the Power Hold line to the ISC, from the ISC on the Unit Source line, and to CP204 in the +24 V BS Supply 1. K601 removes the hold to K201 6
- 2. With K201 dropped, power is removed from the drive motors, blowers, and power supplies in all modules of the string.
- 3. Circuits that remain active after the hold to K601 is lost are the Phase Rotation Detection relay 3, the +24 V Bootstrap Supply, and the convenience outlets.

#### Controller

Since either controller will operate the string, the type of power failure determines whether the drives in the same module will be available. An open CP in the controller power supply affects only the controller, but an open Logic Gate Thermal or tripped drive CP causes loss of power to the drives.

#### CONTROLLER (OPEN THERMAL)

1. When the Logic Gate Thermal or Blower Thermal opens, the Controller AC contactor (K221), the Blower AC con-

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tactor (K222), and the Gate/Blower Thermal Sense relay (K606) 8 or 11 are dropped. This removes power from the A2 logic board 9 or 12, from the blowers, and opens the hold for  $\overline{K331}$  ( $\overline{AC}$  Power Drives) 23.

2. The Power Sequence Complete (LED) 17 and Power Check (LED) 18 are both on. K611 (Power Sequence Delay) 16 is held from the +24 V Bootstrap supply and K612 (+6 V Sense) 26 is dropped because dc drive power is off.

#### **CONTROLLER (TRIPPED CP)**

- 1. A tripped CP in the power circuit for the controller (A2 or C2) logic board drops the Controller AC contactor (K221) 8 or 11. The hold circuit to K221 is through CP420 Aux points and CP421 Aux points.
- 2. The modules (A2 and C2) maintain blower and drive power while the Power Sequence Complete (LED) is on and the Power Check (LED) is off. After control is transferred to the other controller, full string operation is maintained.

#### Drives

When the drives section of an A2, B2, or C2 Module loses power because of a tripped CP, other modules of the string remain on.

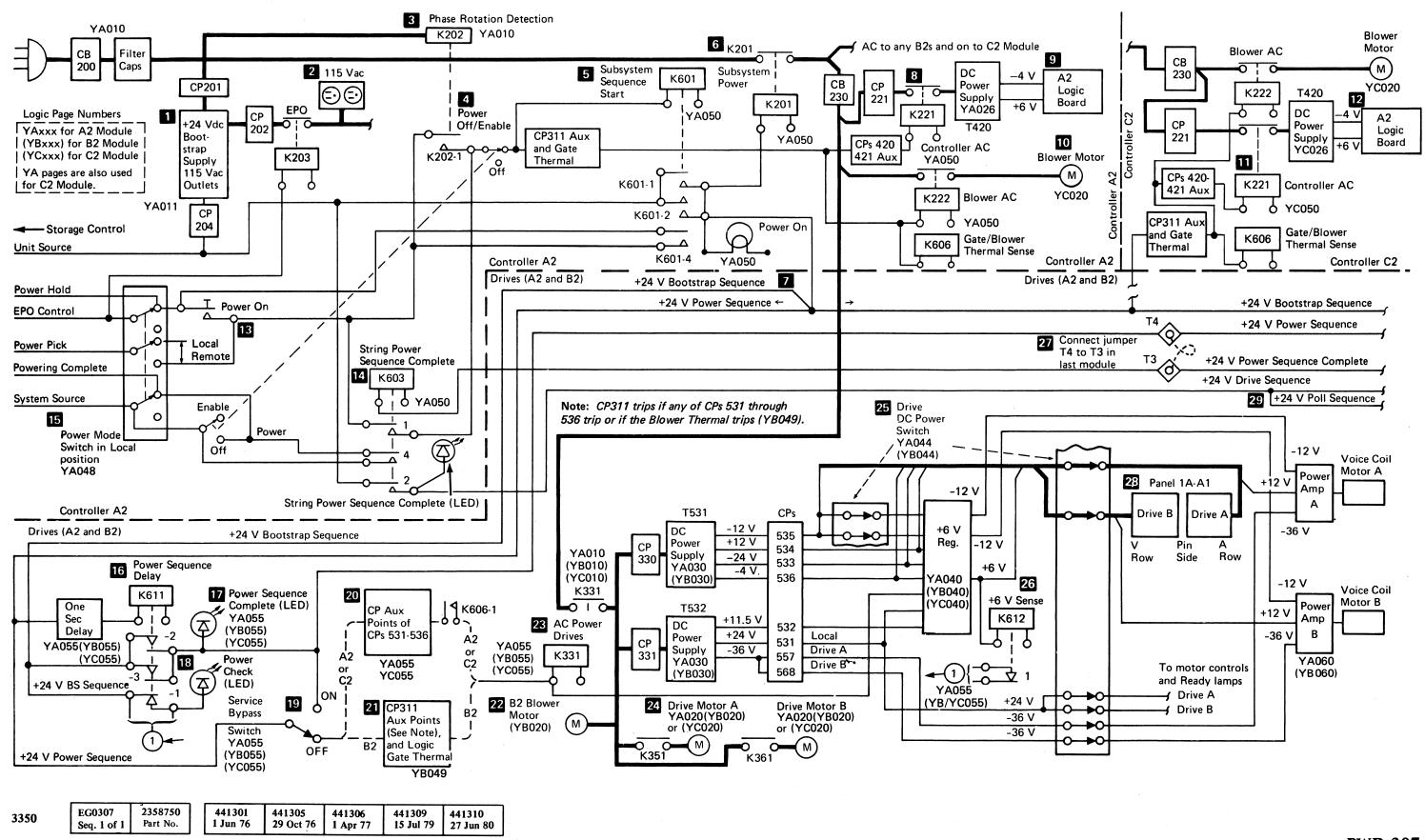
1. If contactor K331 23 is dropped, all power is removed from the dc power supplies and both drive motors in an A2, B2, or C2 Module. In an A2 or C2 Module, K331 is held activated through CPs 531-536 auxiliary points 20, through the Service Bypass switch, and through points of к606.

In a B2 Module, contactor K331 is held activated through the points of the Logic Gate Thermal, CP311 auxiliary points 21, and the Service Bypass switch. CP311 monitors the auxiliary points of CPs 531-536. When an auxiliary point in the series opens, the increased current trips CP311 which opens its auxiliary points to drop K331.

- 2. With K331 dropped in an A2, B2, or C2 Module, other modules of the string remain on because the Power Sequence Delay relay (K611) 16 is still picked to send +24 V Power Sequence to the next module. The Power Sequence Complete (LED) 17 is still on even though the drives are inactive.
- 3. The Power Check (LED) 18 is also turned on when K331 is dropped because there is no +6 V Regulator output to pick the 6 V Sense relay (K612). The normally closed points of K612-1 26 complete the Power Check (LED) circuit.

POWER SUPPLY SEQUENCE **PWR 306** 

## **POWER SUPPLY SEQUENCE**

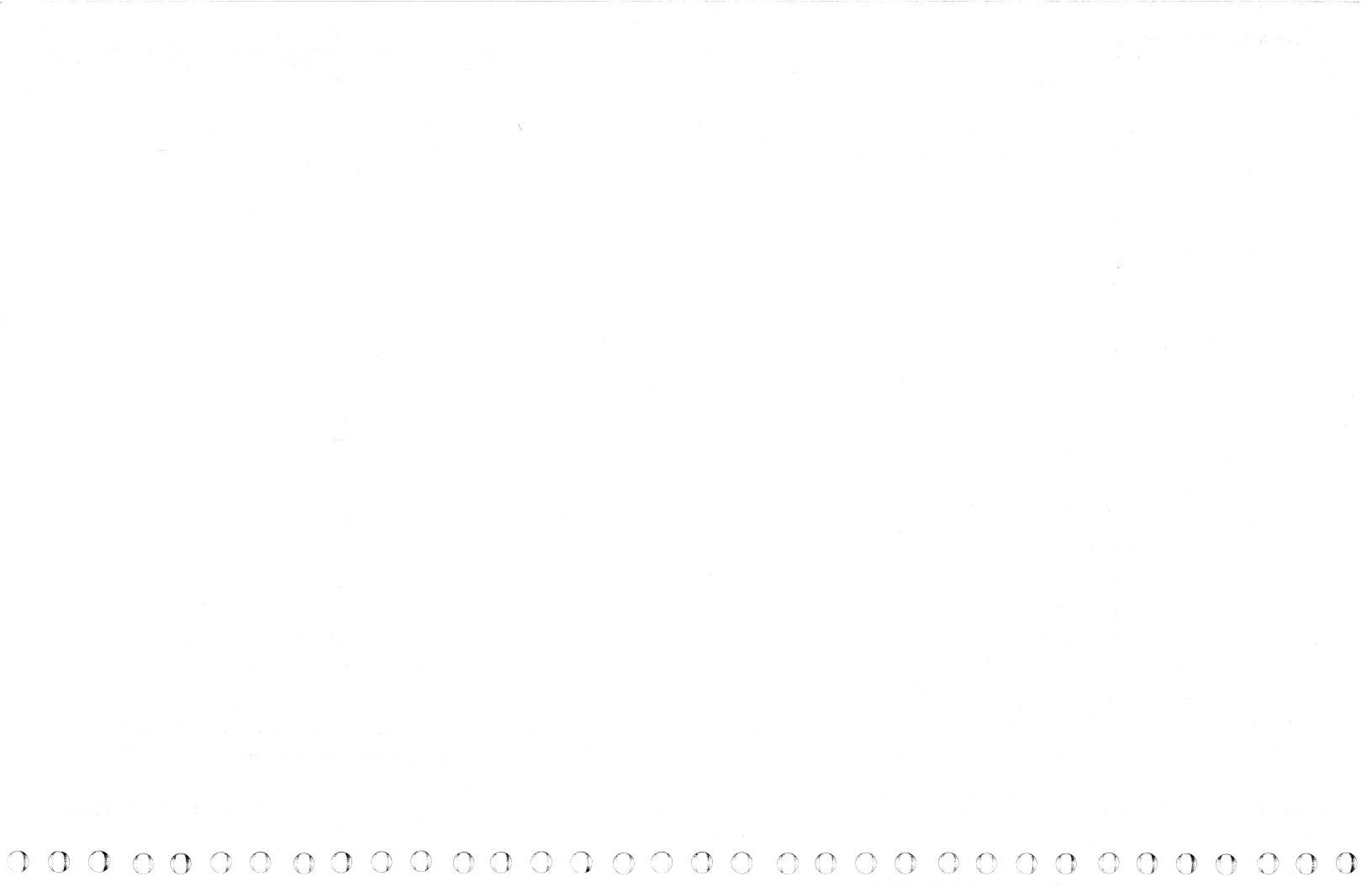


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#### POWER SUPPLY SEQUENCE

**PWR 307** 

### POWER SUPPLY SEQUENCE PWR 307



# **POWER ON SEQUENCE**

				Ă	Sequence Panel, Board				
			•	<b>B</b> =	Sequence Panel, Board			Contraction and contraction of the	
Chart Line No.	Line Name	ALD	Test Point		Press Power On	Both Contre DC Or		Driv	ve DC On (B2 or C2) Advance to next string
	Controller and Drive Power in A2 Modul	e and Controller in C2	Module			-Drive	e DC On (A2)		
1	K202 Phase Rotation	YA010							
2	K601 Subsystem Sequence Start K221 Controller AC (A2) K222 Blower AC (A2) K606 Gate/Blwr Thermal Sense (A2)	YA050	TP9 TB422-6 TB422-5 TP8	<b>A</b> <b>A</b>	V 1				
3	Power On Lamp	YA050	TP5	A	2				
4	K201 Subsystem Pwr On	YA050	TP5	A	2				
5	K221 Controller AC (C2) K222 Blower AC (C2) K606 Gate/Blwr Thermal Sense (C2)	YC050 (C2 Module)	TB422-6 TB422-5 TP8	A	2				
6	DC to Both Controllers (A2) first, followed by C2)	YA026(YC026)	TB101-11 (Logic +6 V Gate)			4			
7	A2 Blower Mtr On C2 Blower Mtr On	YA020(YC020)				4			
8	Power Check (LED)	YA055			2, 10, 11				
9	K331 AC Pwr Drives	YA055	TP9	₿	2				
10	K611 Pwr Seq Delay	YA055	T4 (Jumper terminal)	B		55	2 one s	econd	l delay
11	K612 +6 V Sense Drive	YA055	ТР7	€		9			
12	Power Seq Comp (LED)	YA055					10		
	Drive Power in B2 or C2 Module								
13	Power Check (LED)	YB055(YC055)			1		10, 15, 17		
14	K331 AC Pwr Drives	YB055(YC055)	TP9	0			10		
15	K611 Pwr Seq Delay	YB055(YC055)	T4 (Jumper terminal)	₿	Repeat lines 13 through 18 for each	ר <u>ו</u>			10 one second delay
16	B2 Blower Mtr On	YB020			B2 Module of the s and the C2 Module	tring	14		
17	K612 +6 V Sense Drive	YB055(YC055)	TP7	B				14	
18	Pwr Seq Complete (LED)	YB055(YC055)			/				15
	Setup to Start Spindles								
19	K603 String Power Seq Complete	YA050	TP10	A			· .		15
20	K631 Allow Start	YA055(YB055) (YC055)	TP1	8					19 (in all modules)
21	K632 Start Drives	YA055	TP17	3					20 (in A2 Module first)
22							A CONTRACTOR OF CO		

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POWER ON SEQUENCE **PWR 308** 

C

## **POWER SUPPLY FAILURE ANALYSIS**

#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering on machine.

An overall description of the power-on sequence is located on PWR 306 through PWR 308.

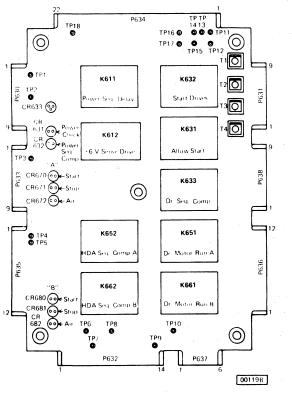
See PWR 391 and LOC pages for component locations.

See ZA100 for relay terminal numbering.

Located In
Controller AC Compartment
Drive AC Compartment
Controller DC Compartment
Drive DC Compartment
Sequence Panel

#### **SEQUENCE PANEL**





2358751

Part No.

441301

1 Jun 76

EG0308

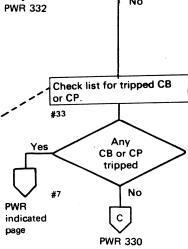
Seq. 2 of 2

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CP or CB	Function	Page En	try
CB200	Main AC Breaker	PWR 320,	A
CP201	AC to 24 V XFMR (Note 1)	PWR 322,	D
CP204	24 V Sequence (Note 2)	PWR 330,	Α



PWR 9

Α

Main Power On lamp off

Off/Enable switch in the Enable position, set Power

Mode switch to the Local

position. Press Power On

Main Power Or

lamp comes on nd remains on

No

PWR 307

switch.

#4

#5

Yes

E

With the Power

Main Power On lamp lights

the Power On switch.

#1

Note 1: When CP201 is tripped, the white button protrudes PWR about 1/4 inch. When reset, the button protrudes about 1/8 indicated inch.

**Note 2:** When CP204 is tripped, the red button protrudes about 1/2 inch. When reset, the button protrudes about 1/4 inch.



## POWER SUPPLY FAILURE ANALYSIS PWR 310

POWER SUPPLY FAILURE ANALYSIS PWR 310

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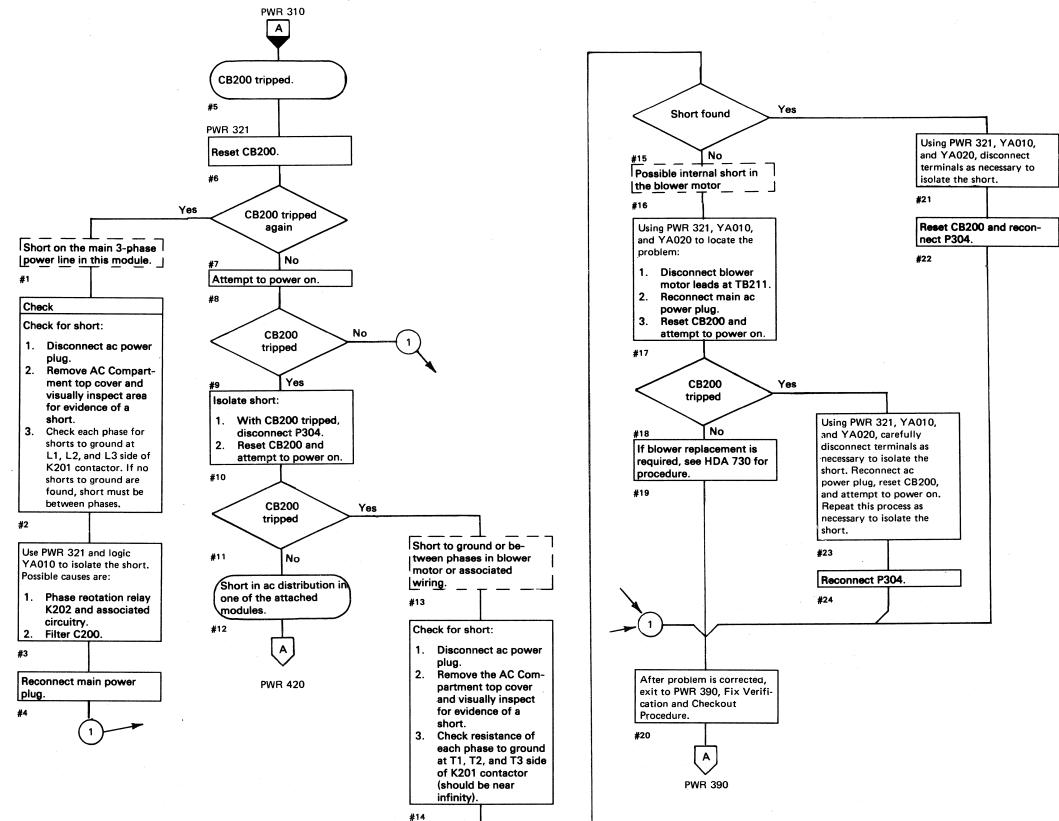
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## **AC CIRCUIT FAILURE ANALYSIS**

#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering on machine.



3350	EG0320 Seq. 1 of 2	2358752 Part No		441301 1 Jun 76	441306 1 Apr 77				
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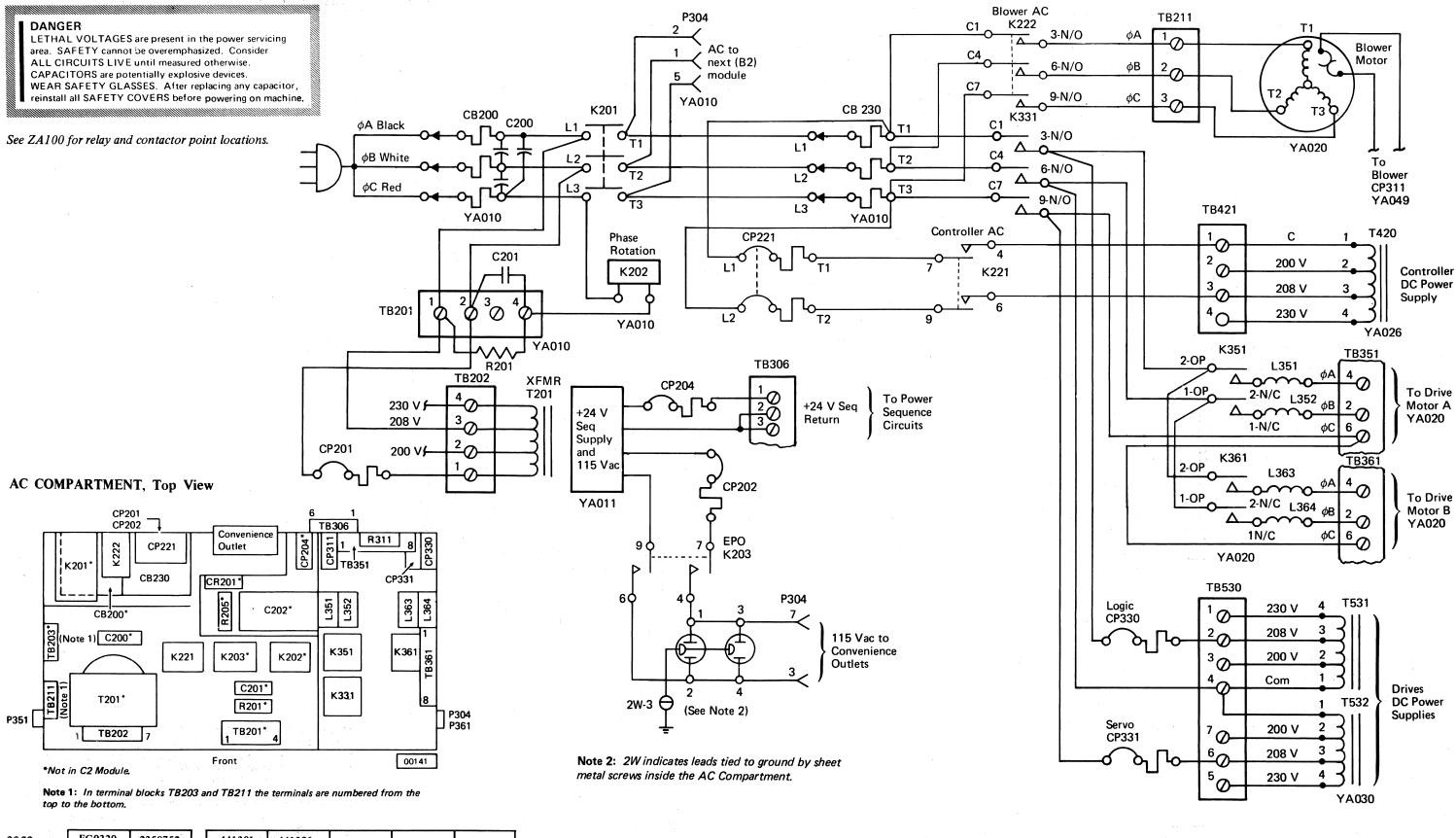
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#### AC CIRCUIT FAILURE ANALYSIS

**PWR 320** 

AC CIRCUIT FAILURE ANALYSIS **PWR 320** 

# AC CIRCUIT DIAGRAM (A2)



EG0320 2358752 3350 441301 441306 Seq. 2 of 2

1 Apr 77

1 Jun 76

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Part No.

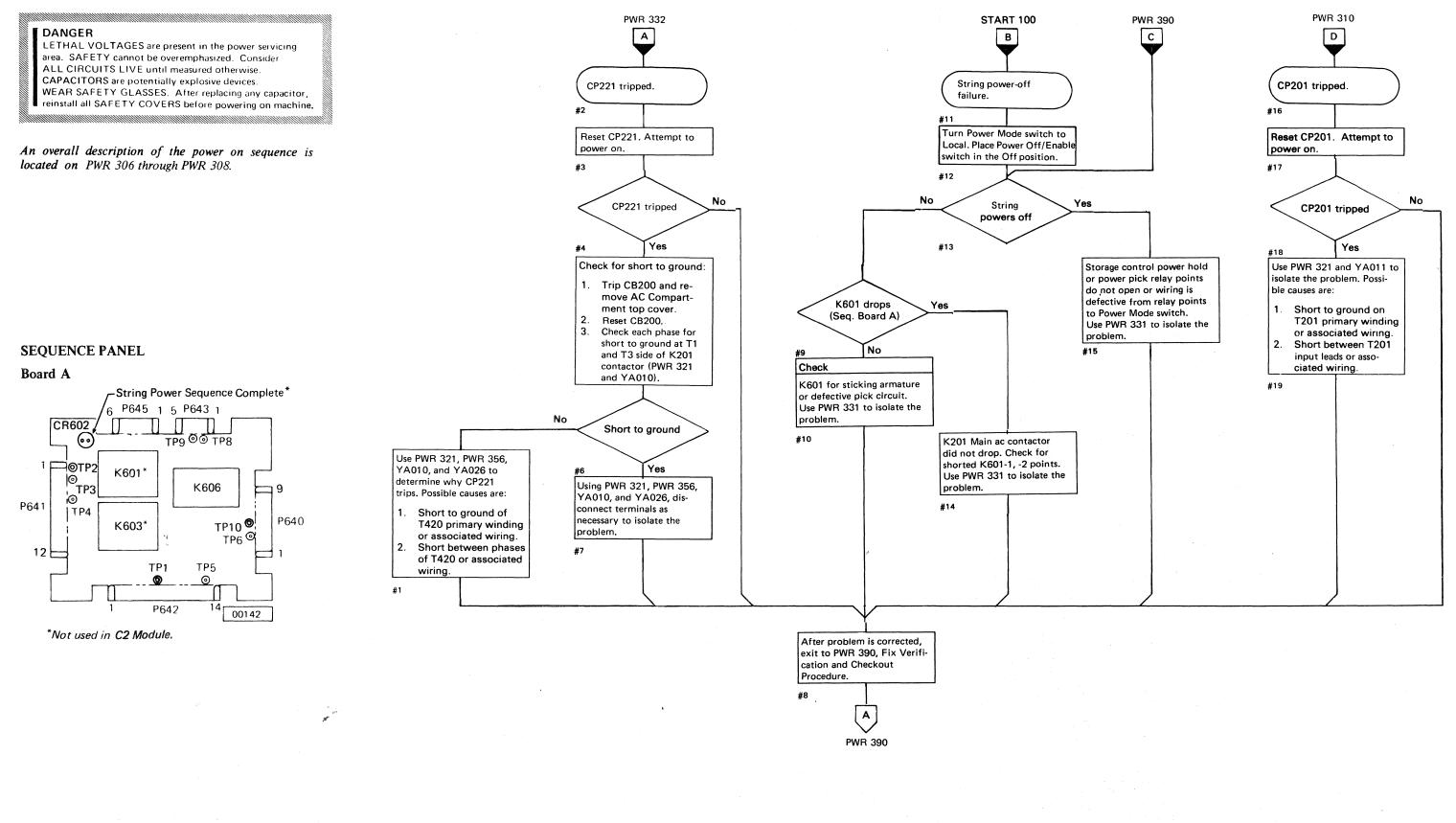
#### AC CIRCUIT DIAGRAM (A2)

**PWR 321** 

AC CIRCUIT DIAGRAM (A2) PWR 321

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## **AC CIRCUIT FAILURE ANALYSIS**



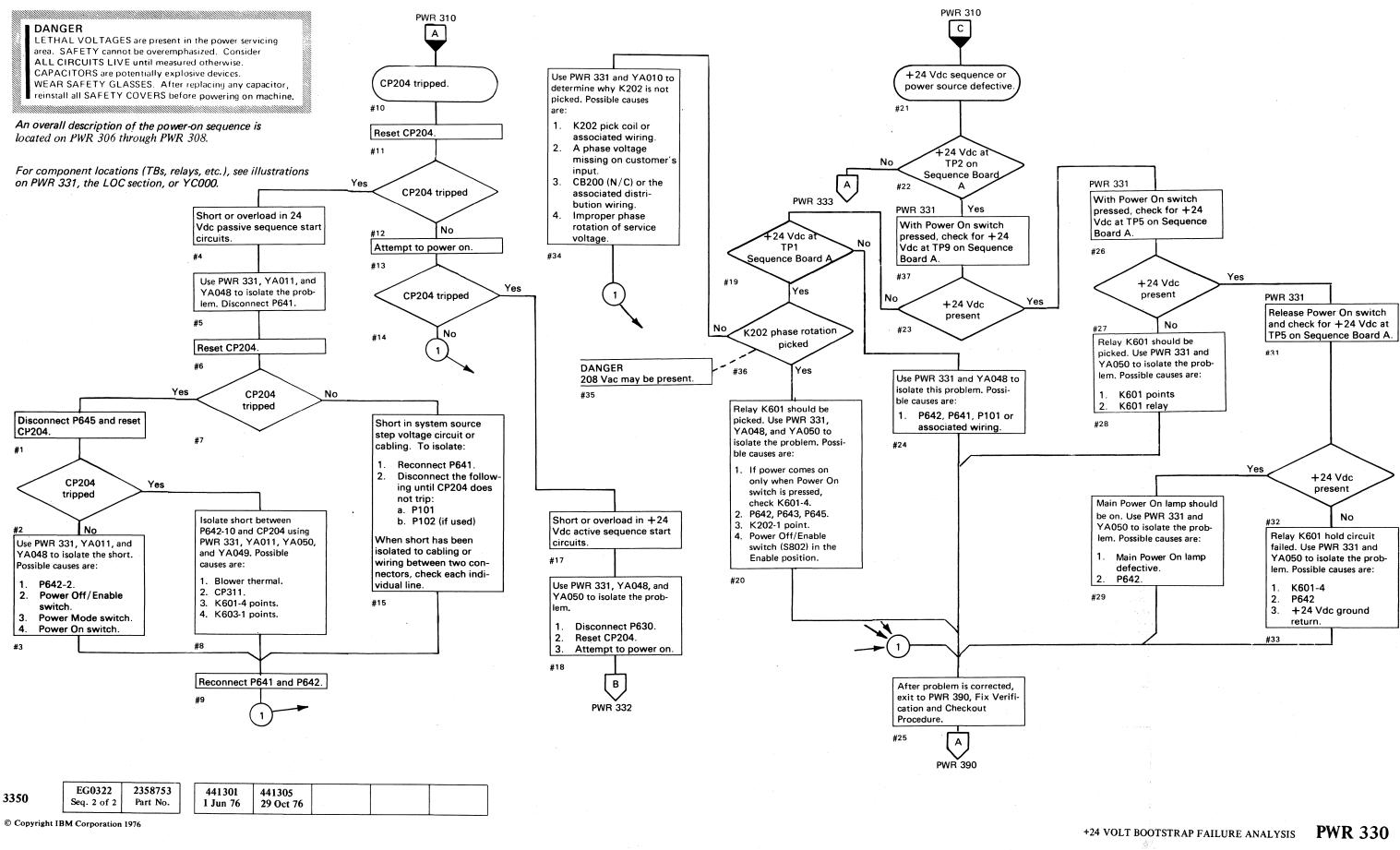
EG0322         2358753         441301         441305           Seq. 1 of 2         Part No.         1 Jun 76         29 Oct	6
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### AC CIRCUIT FAILURE ANALYSIS **PWR 322**

## AC CIRCUIT FAILURE ANALYSIS **PWR 322**

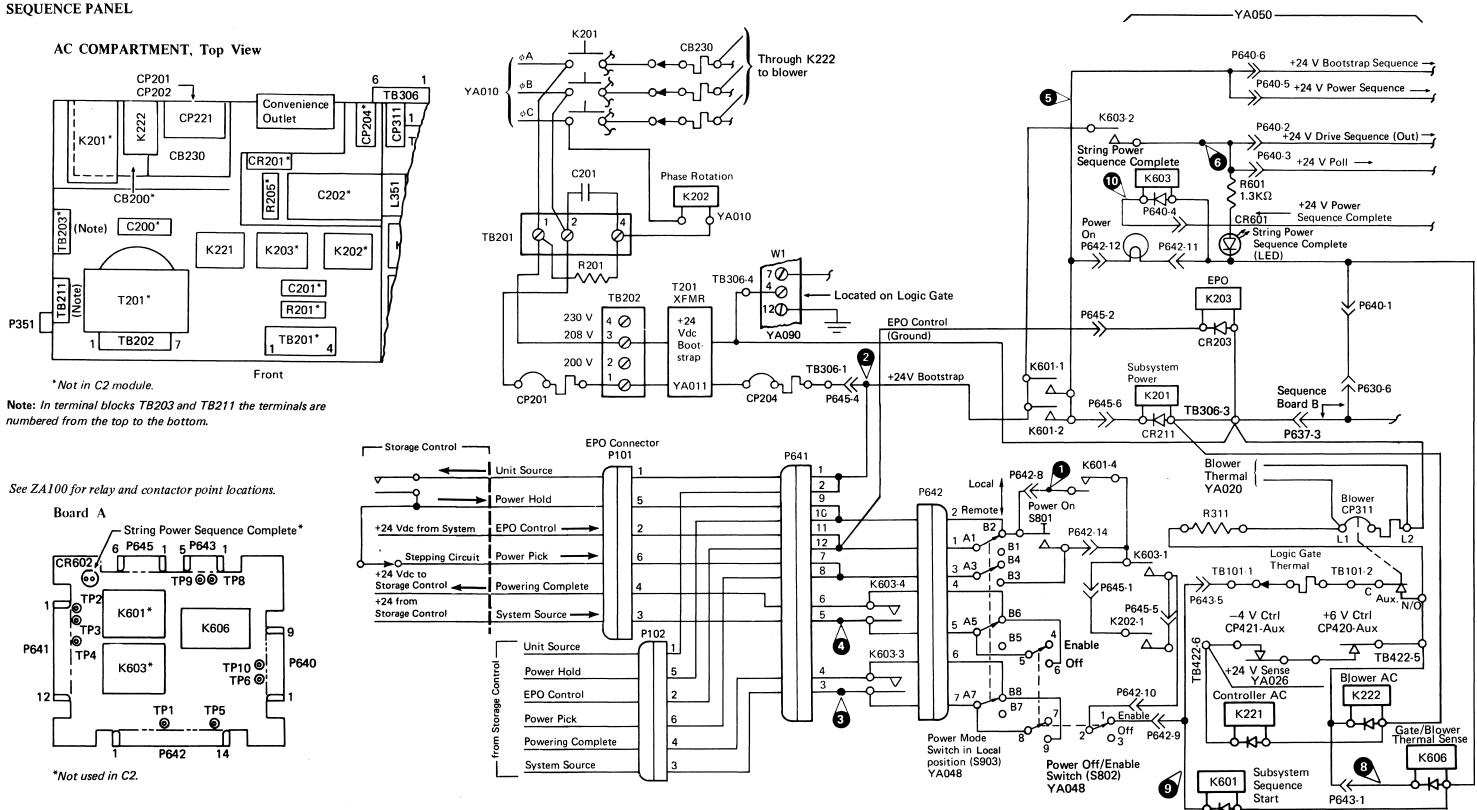
## +24 VOLT BOOTSTRAP FAILURE ANALYSIS



+24 VOLT BOOTSTRAP FAILURE ANALYSIS PWR 330

#### $\bigcirc$

## +24 VOLT BOOTSTRAP DIAGRAM



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3350	EG0331 Seq. 1 of 2	2358754 Part No.		441301 1 Jun 76	441309 15 Jul 79	441310 27 Jun 80	

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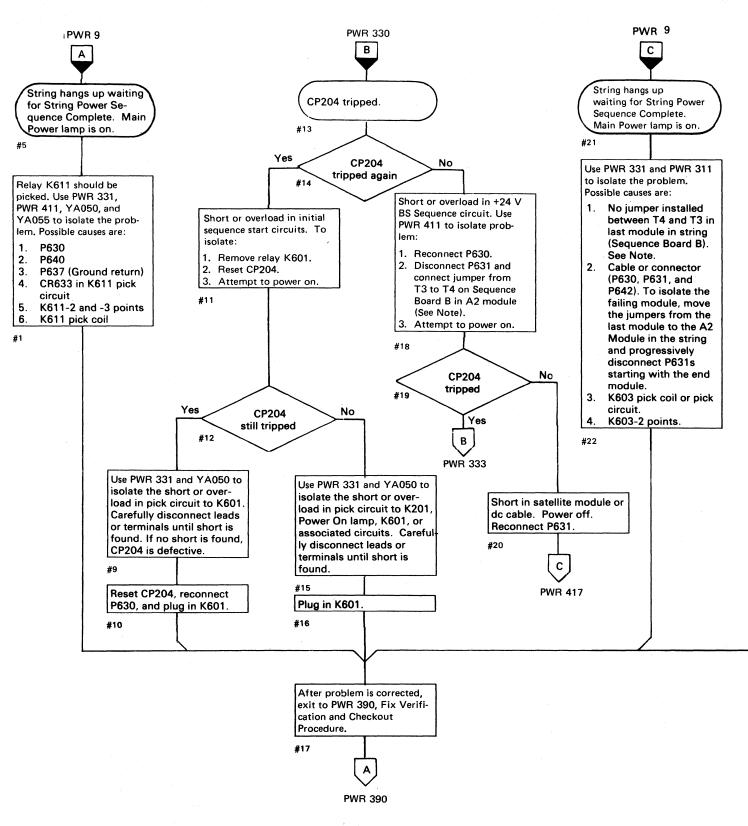
+24 VOLT BOOTSTRAP DIAGRAM

## +24 VOLT BOOTSTRAP FAILURE ANALYSIS

#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering-up machine.

An overall description of the power-on sequence is located on PWR 306 through PWR 308.



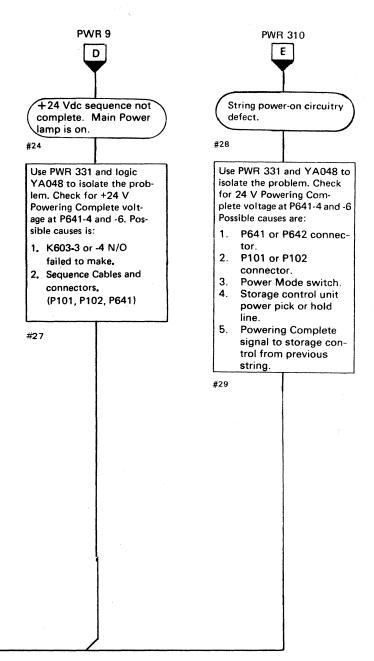
**Note**: The jumpers between T1 and T2 or between T3 and T4 are designed for installation in the last module of a string. The string of modules will work, however, if the jumpers are in any unit regardless of its position in the string.

	1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 - 1971 -					
3350	EG0331 Seq. 2 of 2	2358754 Part No.	441301 1 Jun 76	441309 15 Jul 79	441310 27 Jun 80	

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#### + 24 VOLT BOOTSTRAP FAILURE ANALYSIS

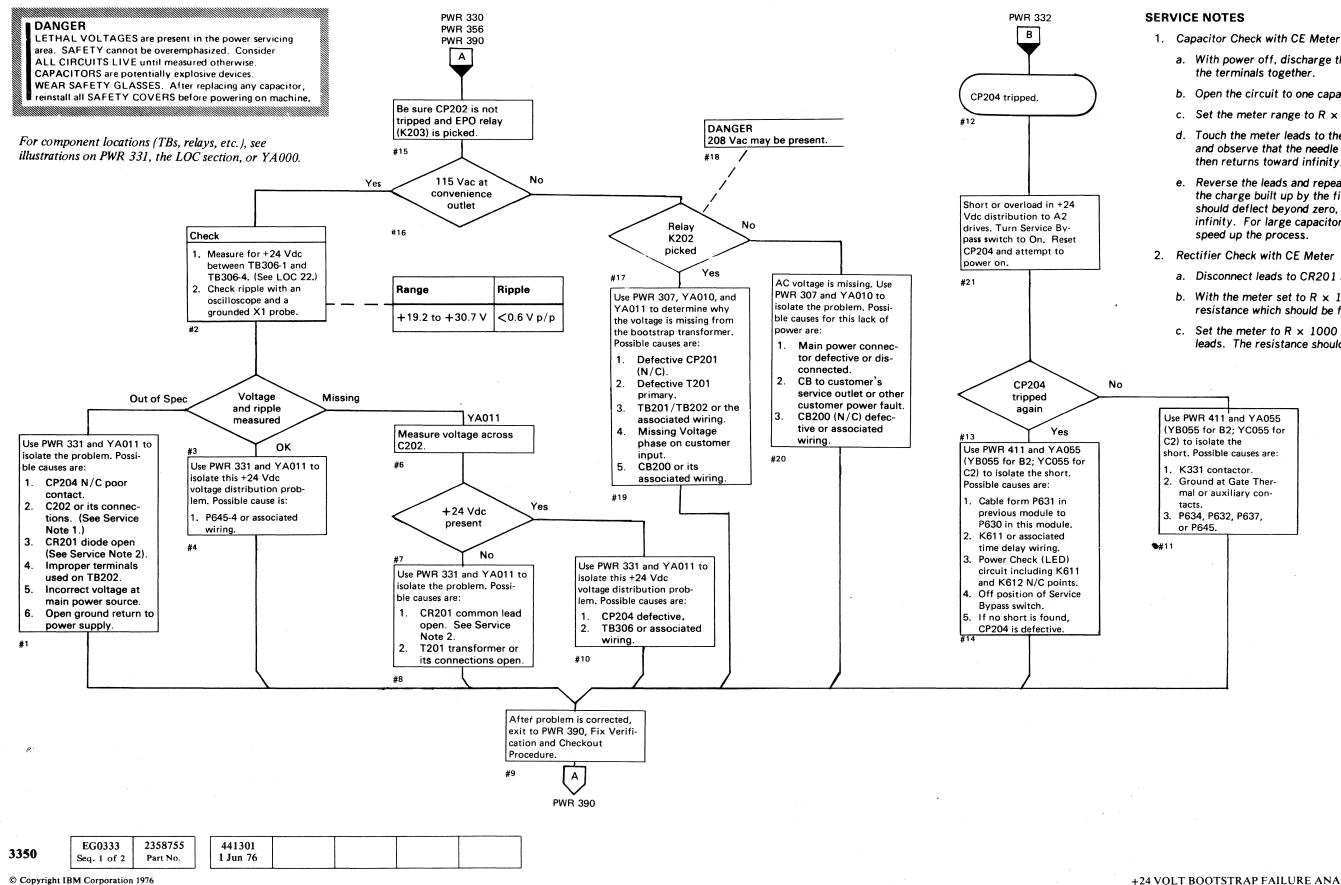
**PWR 332** 



+24 VOLT BOOTSTRAP FAILURE ANALYSIS PWR 332

 $\bigcirc$ 

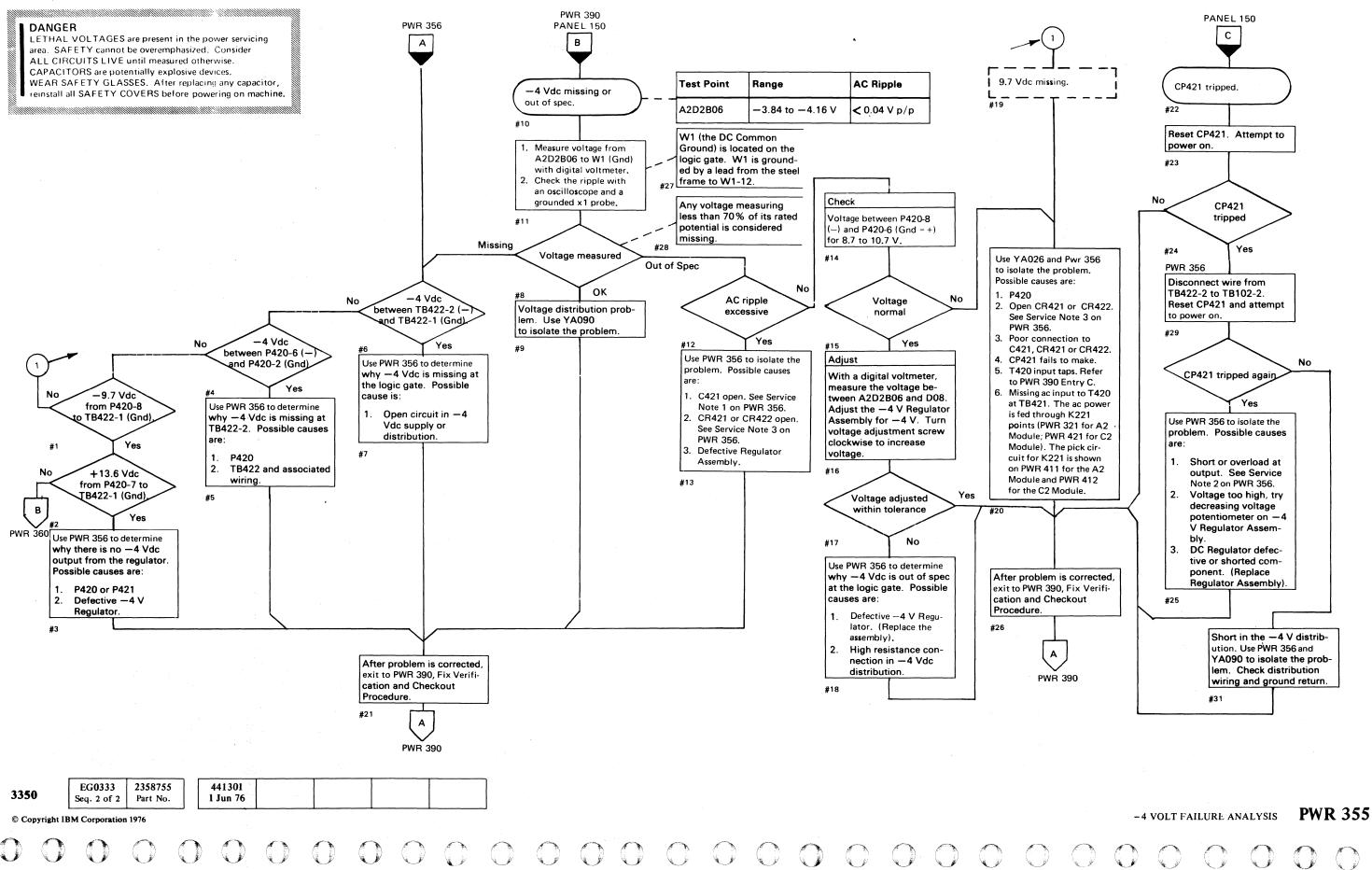
## +24 VOLT BOOTSTRAP FAILURE ANALYSIS



**PWR 333** 

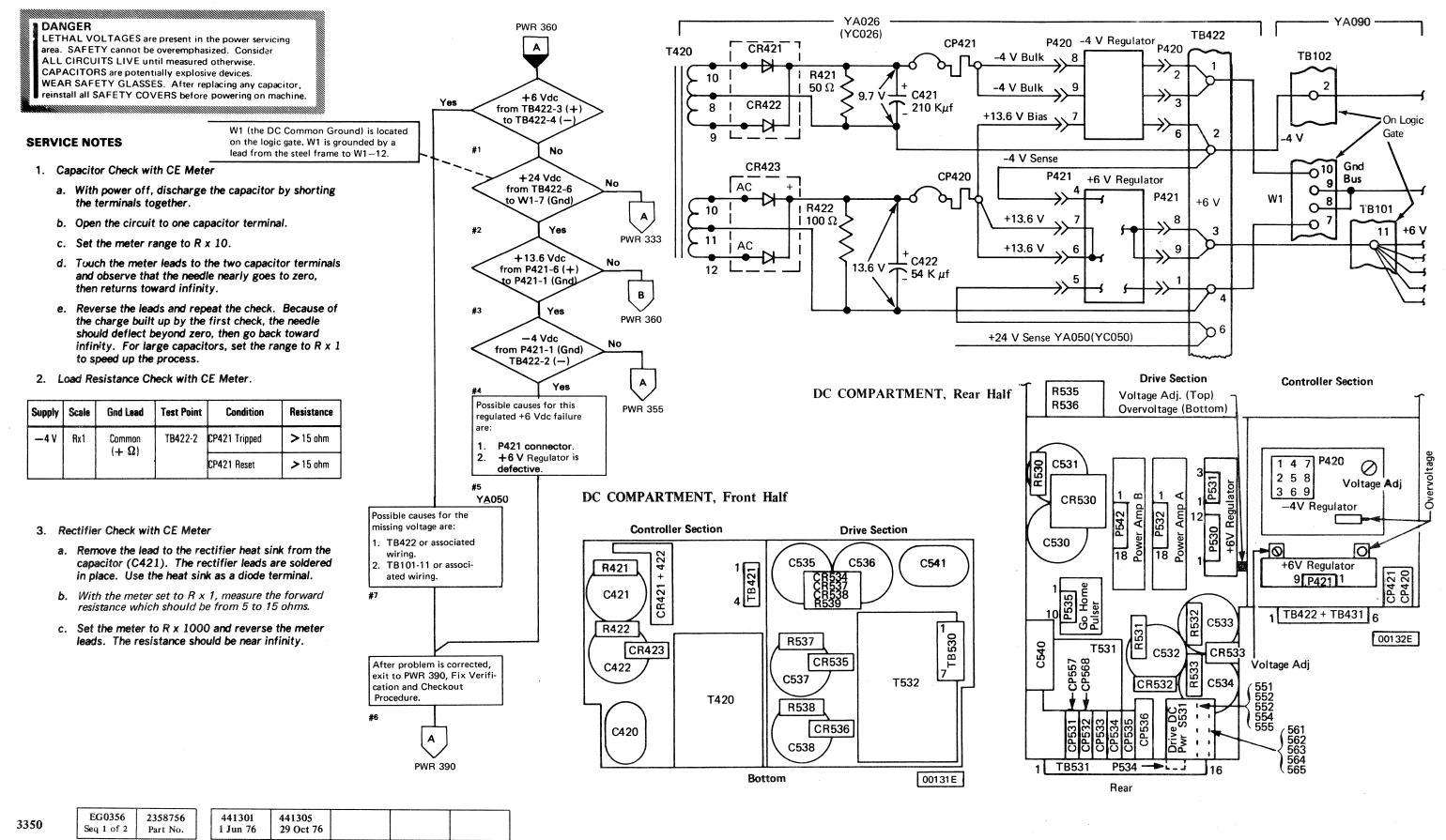
- - a. With power off, discharge the capacitor by shorting the terminals together.
- b. Open the circuit to one capacitor terminal.
- c. Set the meter range to  $R \times 10$ .
- d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
- e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to  $R \times 1$  to speed up the process.
- - a. Disconnect leads to CR201 assembly (PWR 31).
  - b. With the meter set to  $R \times 1$ , measure the forward resistance which should be from 5 to 15 ohms.
  - c. Set the meter to  $R \times 1000$  and reverse the meter leads. The resistance should be near infinity.

## -4 VOLT FAILURE ANALYSIS



#### -4 VOLT FAILURE ANALYSIS

## -4 V AND +6 V REGULATOR DIAGRAM

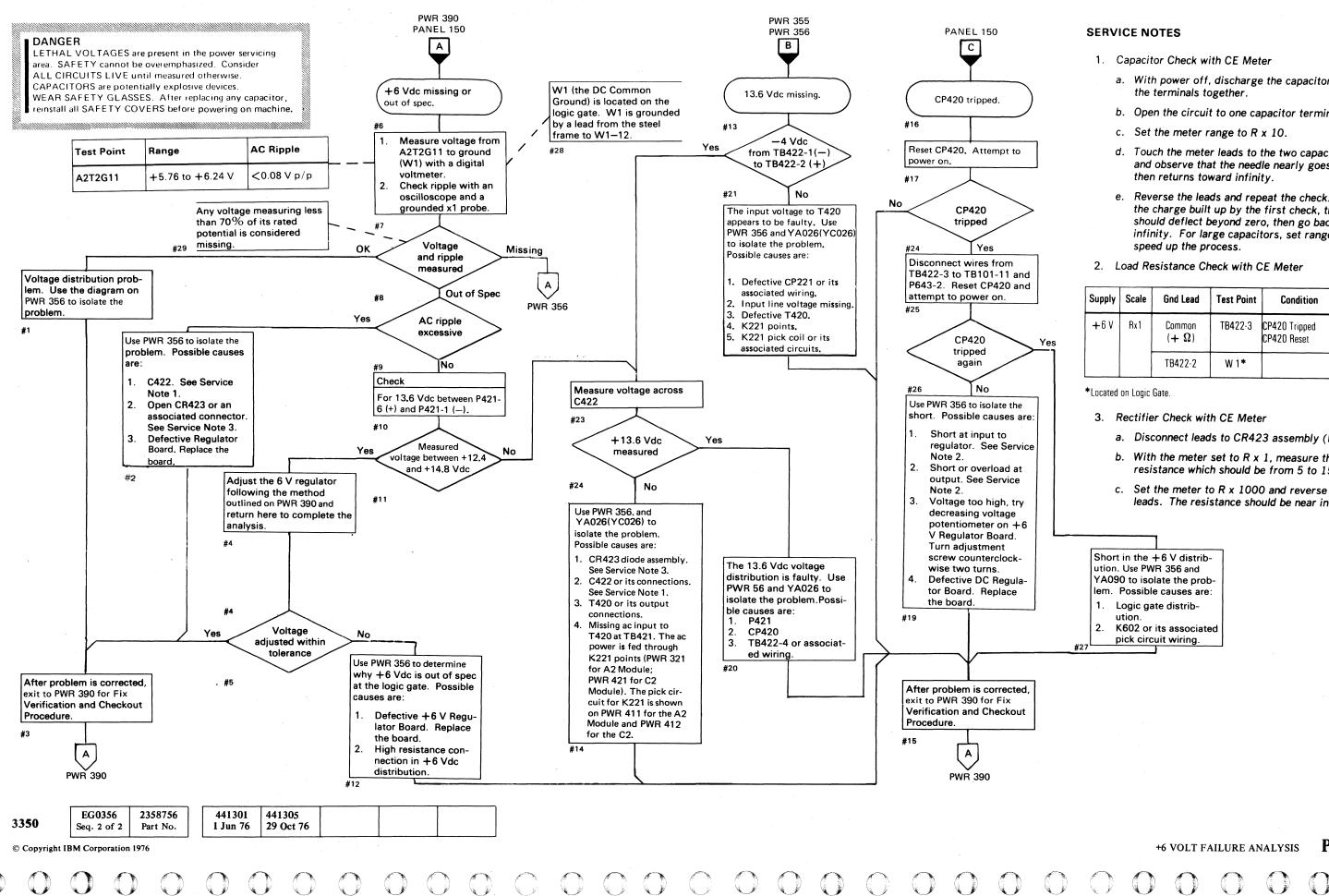


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### -4 VOLT AND +6 VOLT REGULATOR PWR 356

-4 VOLT AND +6 VOLT REGULATOR

## +6 VOLT FAILURE ANALYSIS



#### SERVICE NOTES

- 1. Capacitor Check with CE Meter
  - a. With power off, discharge the capacitor by shorting the terminals together.
  - b. Open the circuit to one capacitor terminal.
  - c. Set the meter range to R x 10.
  - d. Touch the meter leads to the two capacitor terminals and observe that the needle nearly goes to zero, then returns toward infinity.
  - e. Reverse the leads and repeat the check. Because of the charge built up by the first check, the needle should deflect beyond zero, then go back toward infinity. For large capacitors, set range to R x 1 to speed up the process.
- 2. Load Resistance Check with CE Meter

Supply	Scale	Gnd Lead	Test Point	Condition	Resistance
+6V	Rx1	Common $(+ \Omega)$		CP420 Tripped CP420 Reset	> 15 ohm > 15 ohm
		TB422-2	W 1*		<b>&gt;</b> 10 ohm

\*Located on Logic Gate.

- 3. Rectifier Check with CE Meter
  - a. Disconnect leads to CR423 assembly (PWR 56).
  - b. With the meter set to R x 1, measure the forward resistance which should be from 5 to 15 ohms.
  - c. Set the meter to R x 1000 and reverse the meter leads. The resistance should be near infinity.

	Short in the +6 V distrib- ution. Use PWR 356 and
	YA090 to isolate the prob- lem. Possible causes are:
	1. Logic gate distrib- ution.
	<ol> <li>K602 or its associated pick circuit wiring.</li> </ol>
‡27`	

+6 VOLT FAILURE ANALYSIS **PWR 360** 

<u>.</u>

## FIX VERIFICATION AND VOLTAGE CHECKS

PWR	
A	

#### FIX VERIFICATION AND CHECKOUT PROCEDURE

Complete the following checklist to ensure that the machine problem has been corrected. If a check cannot be completed, go to the referenced MIM page for aid in making a fix.

Note 1: It is not always necessary to check each step. Use your judgement for skipping all unneeded steps.

- 1. Set Power Mode switch to Local, then power off the string by placing the Power Off/Enable switch in the Off position. If the string does not power off, go to PWR 322, Entry C (controller).
- 2. Restore the string to normal operating conditions. (Remove all diagnostic jumpers and replace wiring, connectors, or parts that were removed.)
- 3. Power on the string, then set Power Mode switch to Remote.
- 4. Verify that the Power Sequence Complete (LED) and String Power Sequence Complete (LED) indicators and the blowers in each module all turn on. If not, go to PWR 9, Entry D.
- 5. Turn on the A and B Drive Start switches on the problem module(s). Verify that both Ready lamps turn on. If not, go to START 100, Entry B.
- 6. Check power supply voltages as shown in the Voltage Check Chart (this page). (See Note 2.)
- 7. Examine the DC Compartment air filter and clean or replace as necessary.
- 8. Replace all covers.
- 9. Run a string check. (See START 110.)
- 10. Go to START 500, Entry A.

PWR в

## **VOLTAGE CHECKS**

Note 2: The following checks should be made with the drives stopped or Ready but with no Seek or Read/Write operations in progress.

#### **DC Voltage Checks**

Measure each dc voltage in the order listed in the Voltage Check Chart. Only two voltages can be directly adjusted (-4 V and +6 V) for the controller board (A2). If adjustments are necessary, measure with a digital voltmeter. The adjustment potentiometers for -4 V and +6 V Regulators are accessible when the rear DC Compartment cover is removed. Be certain that only the voltage adjustment potentiometer on the regulator card is adjusted. (See PWR 356.) The overvoltage potentiometer on each card is adjusted at the plant and should not be changed. Turn the voltage adjustment potentiometer clockwise to increase the voltage.

If the voltage checks are not completed successfully, exit to the appropriate MAP indicated in the Voltage Check Chart.

If this page is entered because of a known dc voltage problem, and the voltage checks are correct, the problem must be in the voltage distribution. Use the appropriate diagram listed in the chart to isolate the problem.

### **AC Ripple Checks**

If the peak-to-peak ac ripple exceeds the maximum listed in the chart, it is likely that a power supply part has failed.

To measure the ac ripple, use the ac input on a scope having a 0.01 volt per centimeter range and a X1 probe placed on the test points shown in the chart. Place the probe ground on any convenient ground point.

If the ac component is greater than the maximum listed, exit to the appropriate MAP referenced in the chart to correct the problem.

> W1 (the DC Common Ground) is located on the logic gate. W1 is grounded by a lead from the steel frame to W1-12.

## **VOLTAGE CHECK CHART**

DC Supply	Test Points	/ Tolerance (Volts)	Adjustments	Logic Page	Maximum AC Ripple	Diagram	Page Entry
+24 V BS Seq.	TB301-6 to / W1 (Gnd)	+19.2 to +30.7	None*	YA050	0.6 V p/p	PWR 331	PWR 333, A
–4 V Reg	A2T2B06 to A2T2D08	-3.84 to -4.16 (Adiust to 4.0)	Turn screw clockwise to in- crease voltage	YA090 BV100	0.04 V p/p	PWR 356	PWR 355, B
+6 V Reg	A2TG11 to A2T2D08	+5.76 to +6.24 (Adjust to 6.0)	Turn screw clockwise to in- crease voltage	YA090 BV100	0.08 V p/p	PWR 356	PWR 360, A

\*Check transformer primary input taps and change to match available voltage. (See chart above.)

EG0390 2358757 441301 441305 441306 3350 Seq. 1 of 2 Part No. 1 Jun 76 29 Oct 76 1 Apr 77

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#### **TRANSFORMER PRIMARY INPUT TAP** WIRING CHART

Voltage	TB421 (YC026)
200 V	Phase C to TB421-2
208 V	Phase C to TB421-3
230 V	Phase C to TB421-4

FIX VERIFICATION AND VOLTAGE CHECKS

## **COMPONENT AND TEST POINT LOCATIONS**

#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering on machine.

#### See ZA100 for relay and contactor point location.

DC COMPARTMENT, Rear Half

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18 8

P532

<sup>+</sup> C532

CR532

IN A

P530

C533

🗲 CR53'3

C534

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R535

R536

C531

C530

C540

CR530

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557 568

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TB531

**T53**1

**Drive Section** 

Overvoltage (Bottom)

Voltage Adj. (Top)

**Controller Section** 

P420

Ο

CP421 CP420

00132E

-4V Regulator

+6V Regulator

9 P421 1

1 TB422 + TB431 6

0

Voltage Adj

1 4 7

258

369

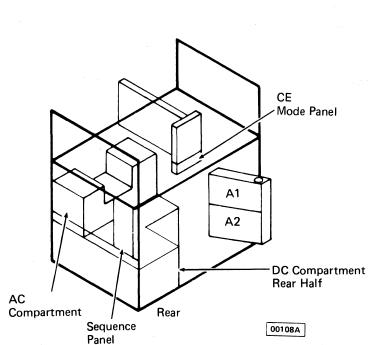
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Voltage Adj

551

552

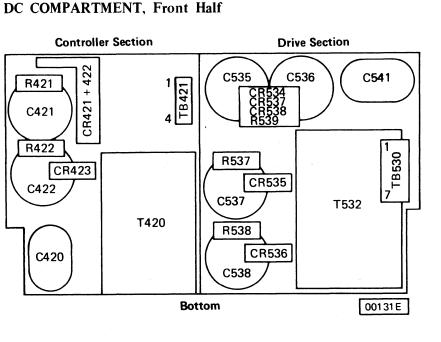
552 554 555

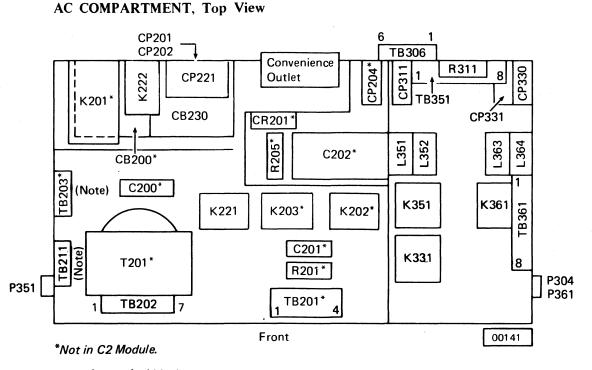


A2 MODULE

age

Overvol





Note: In terminal blocks TB203 and TB211, the terminals are numbered from top to bottom.

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3350	EG0390 Seq. 2 of 2	2358757 Part No.	441301 1 Jun 76	441305 29 Oct 76	441306 1 Apr 77	
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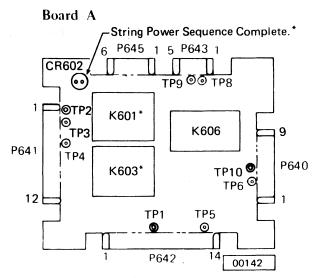
P534

Rear

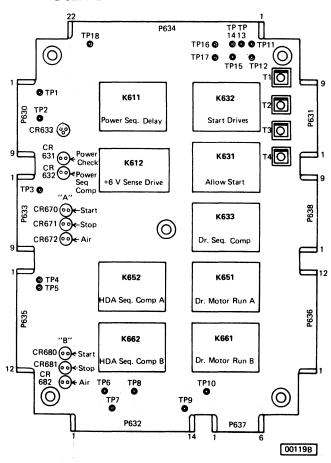
## COMPONENT AND TEST POINT LOCATIONS PWR 391

der.

### **SEQUENCE PANEL, A2 MODULE**



\*Not used in C2 Module.



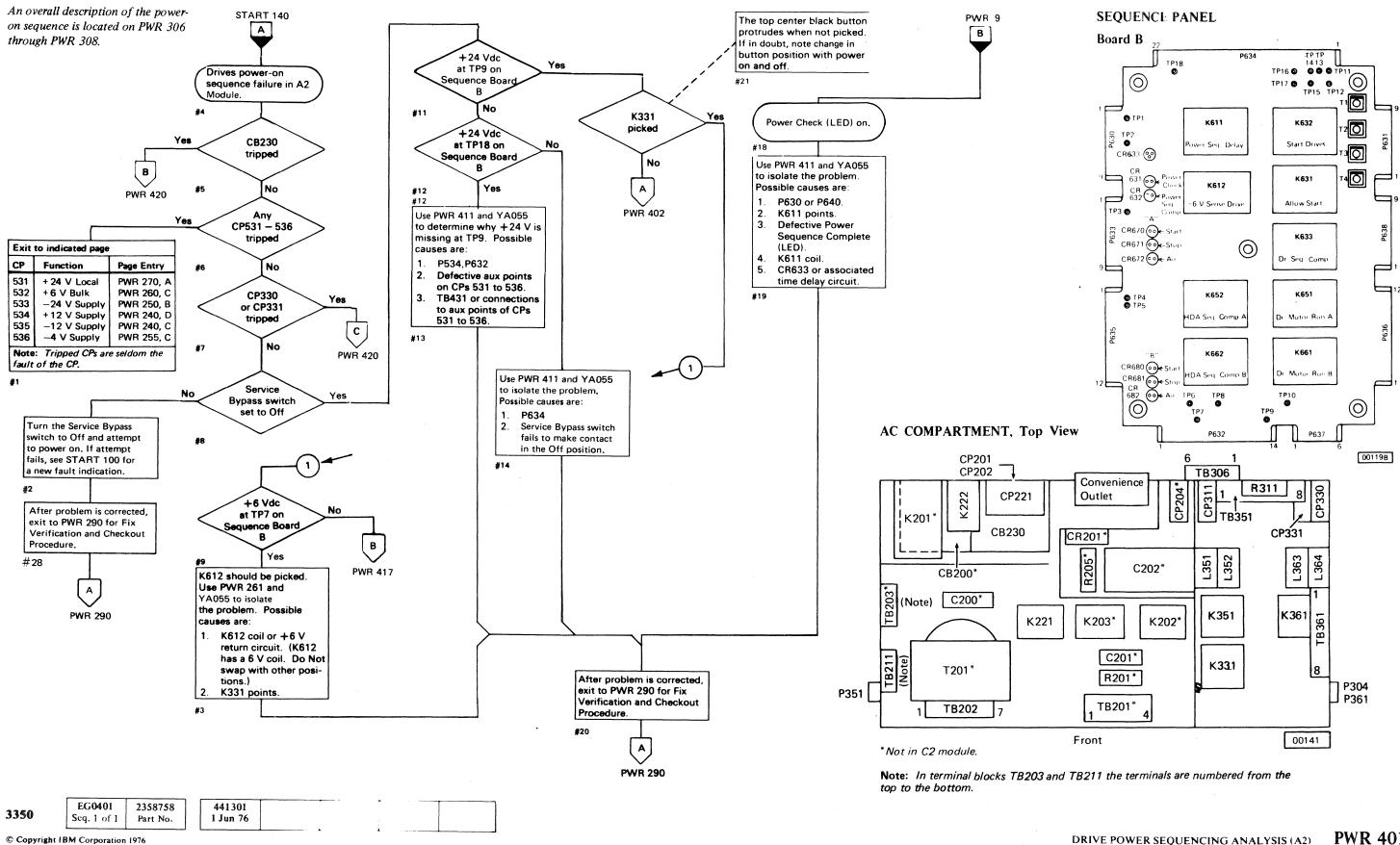
COMPONENT AND TEST POINT LOCATIONS

**PWR 391** 

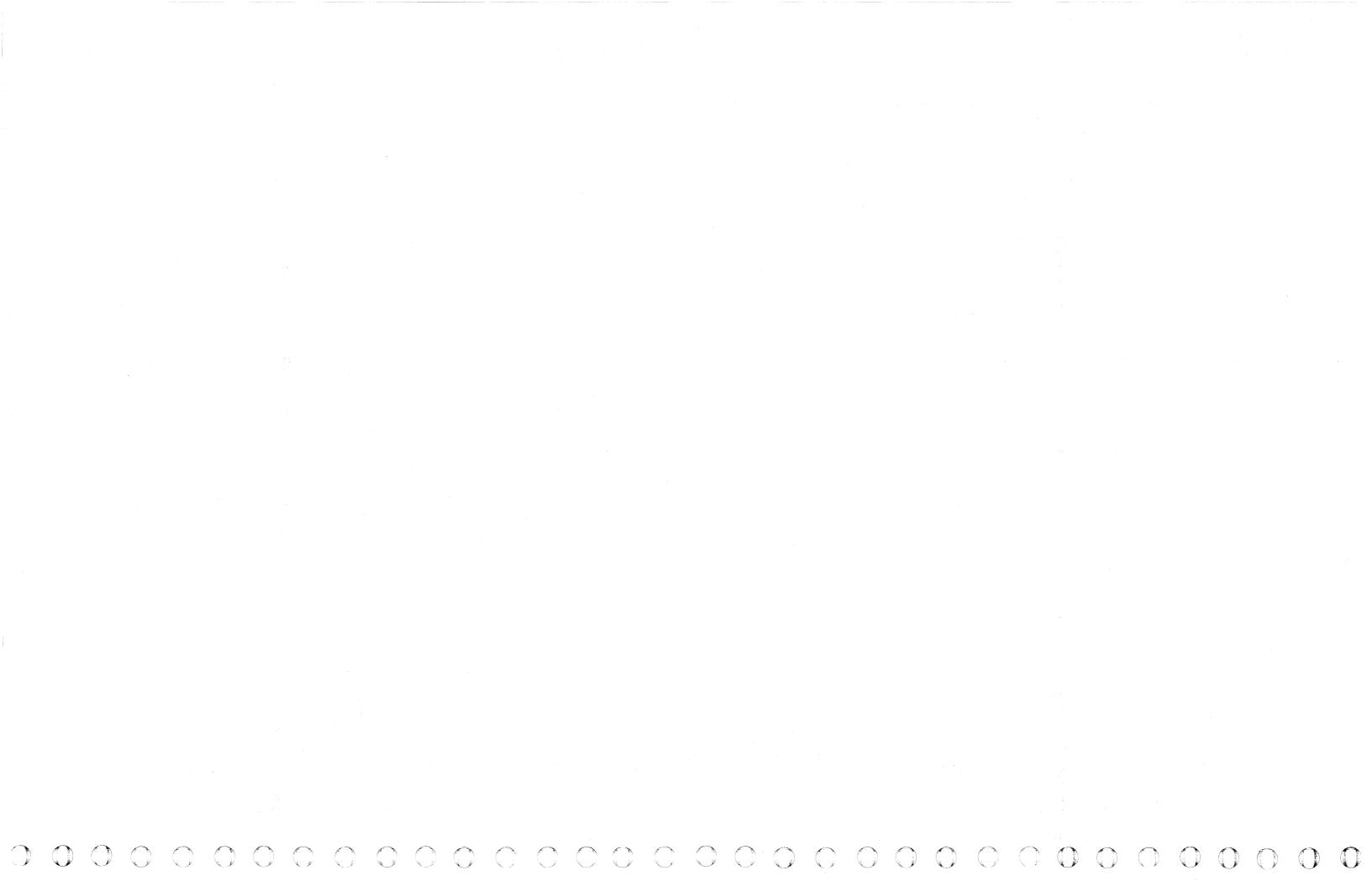
 $\bigcirc$ 

**Board B** 

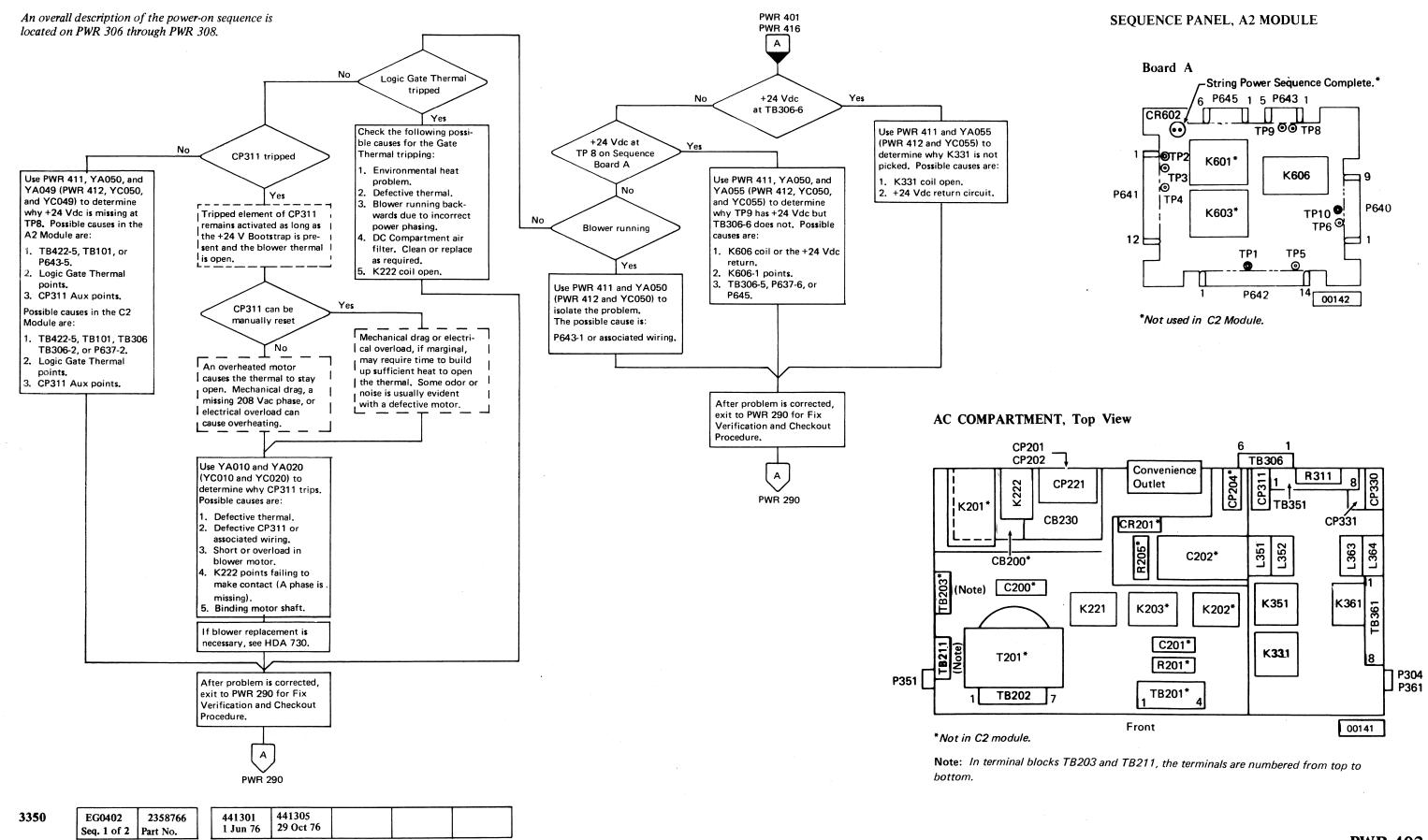
## **DRIVE POWER SEQUENCING ANALYSIS (A2)**



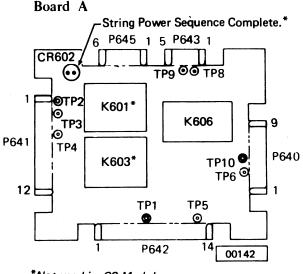
**PWR 401** DRIVE POWER SEQUENCING ANALYSIS (A2)



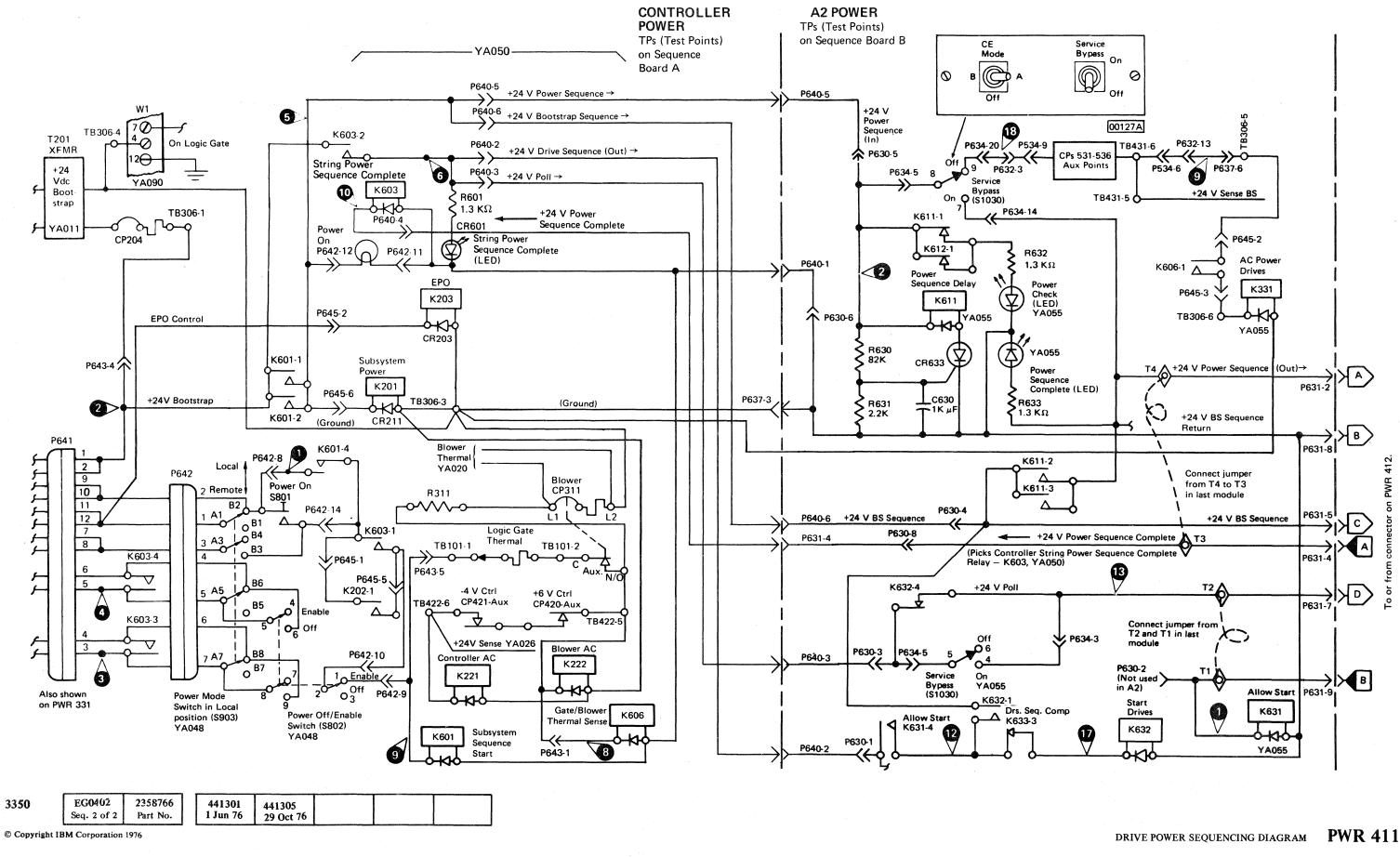
## **DRIVE POWER SEQUENCING ANALYSIS (A2 or C2)**



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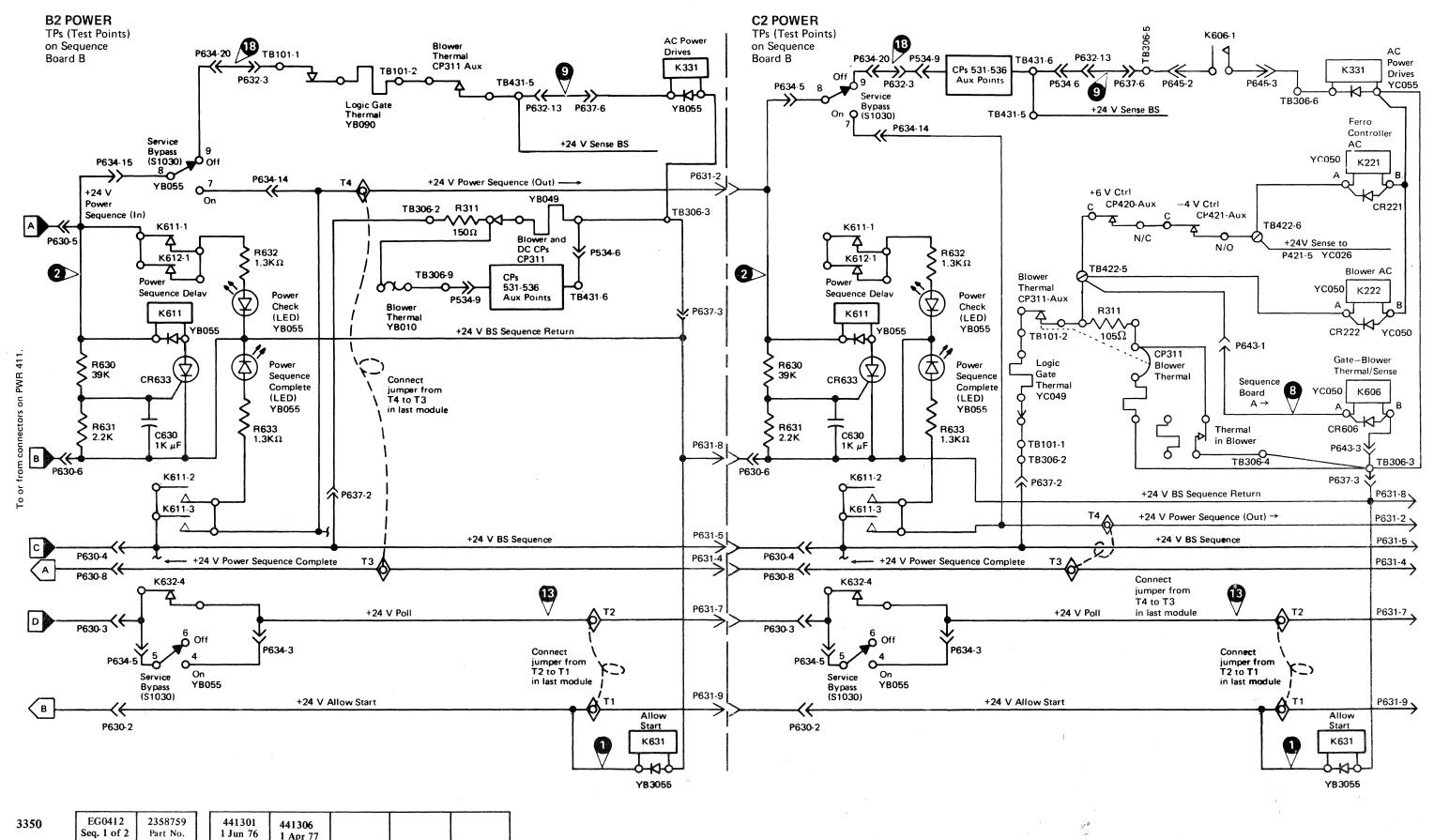
## DRIVE POWER SEQUENCING DIAGRAM



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#### DRIVE POWER SEQUENCING DIAGRAM

## **DRIVE POWER SEQUENCING DIAGRAM**



	1	
© Copyright IBM Corporatio	n 1976, 1977	

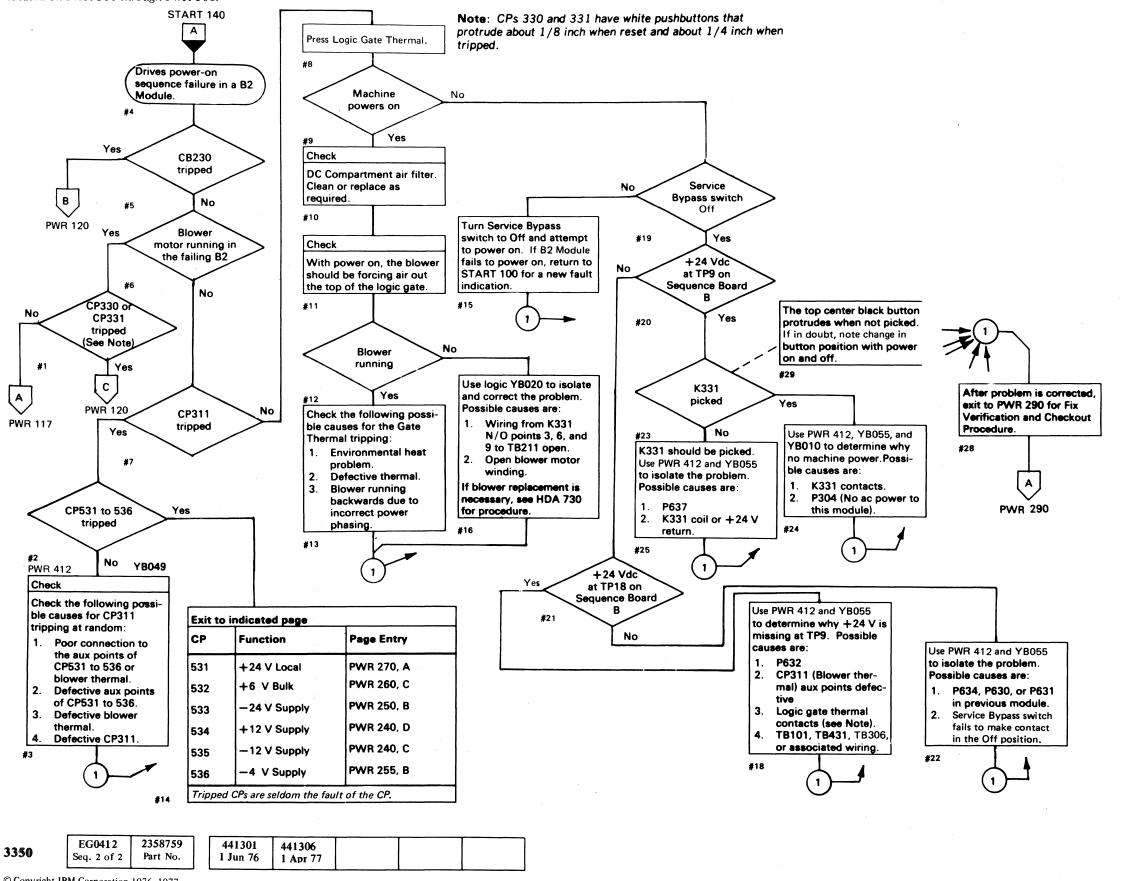
DRIVE POWER SEQUENCING DIAGRAM

**PWR 412** 

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## **DRIVE POWER SEQUENCING ANALYSIS (B2)**

An overall description of the power-on sequence is located on PWR 306 through PWR 308.



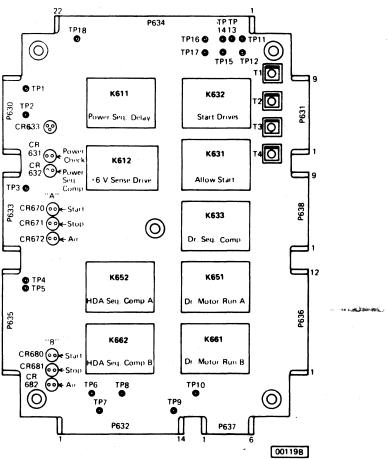
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DRIVE POWER SEQUENCING ANALYSIS (B2) PWR 415

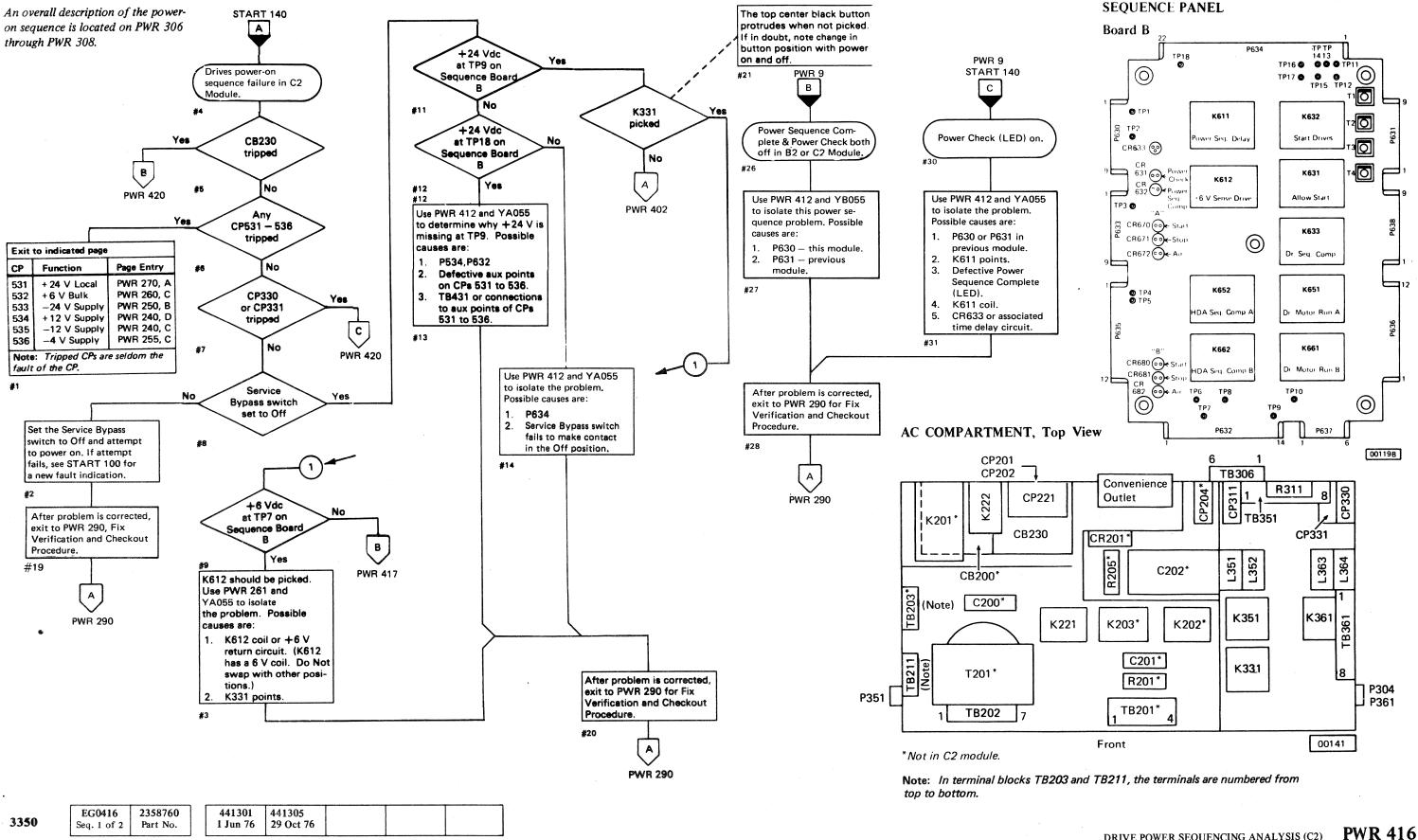
**PWR 415** 

### **SEQUENCE PANEL**

### **Board B**



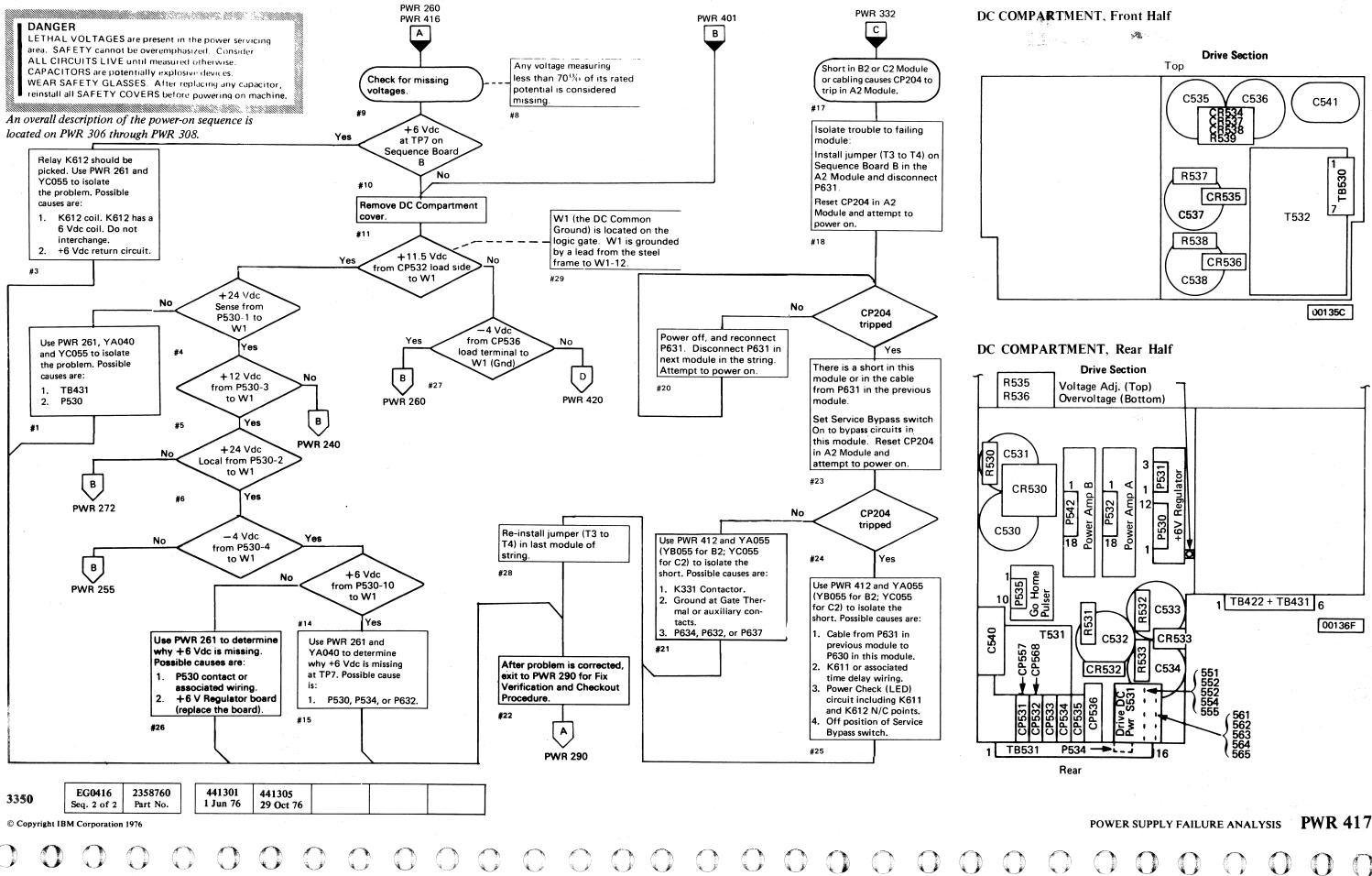
## **DRIVE POWER SEQUENCING ANALYSIS (C2)**



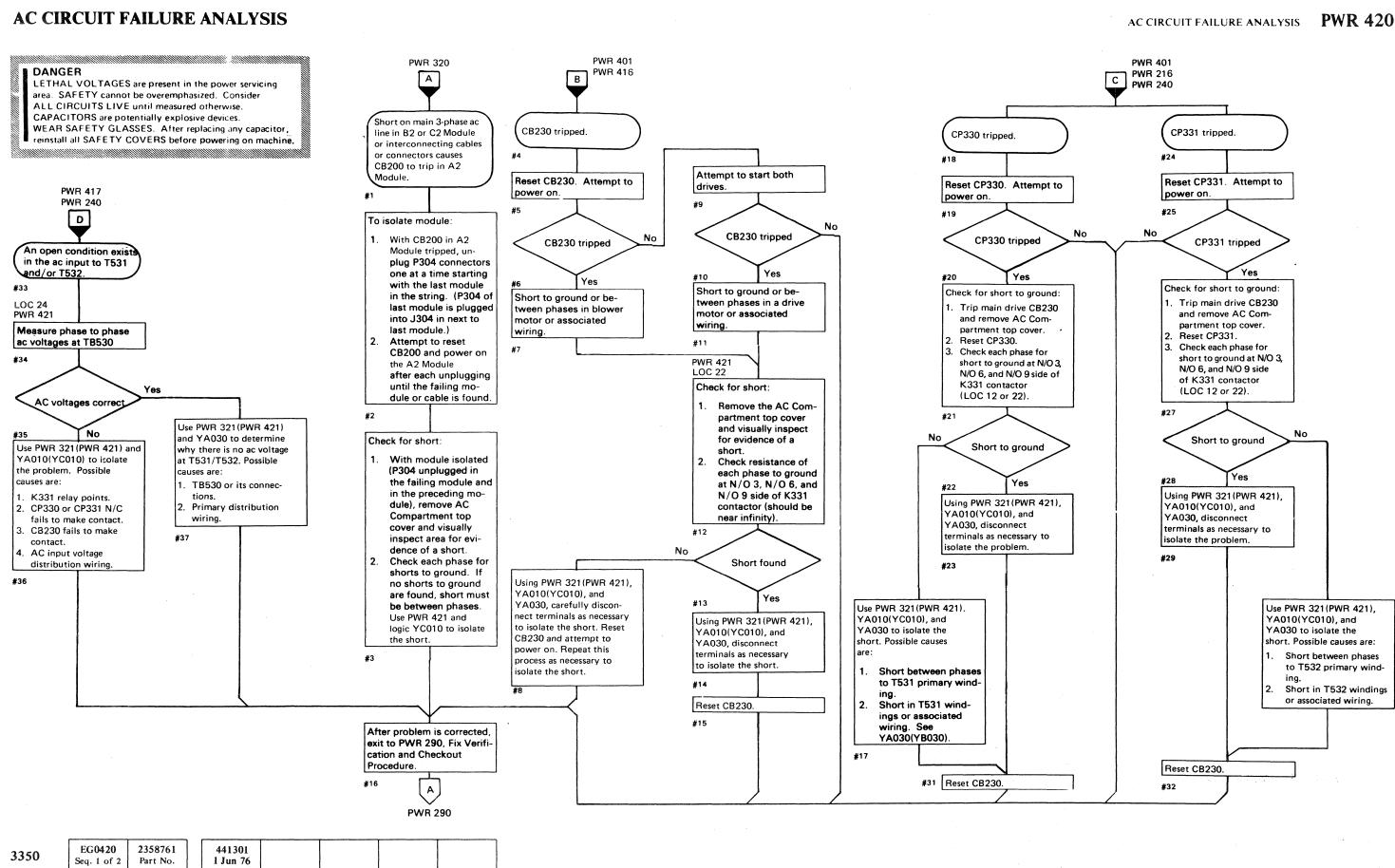
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DRIVE POWER SEQUENCING ANALYSIS (C2)

## **POWER SUPPLY FAILURE ANALYSIS**



#### POWER SUPPLY FAILURE ANALYSIS



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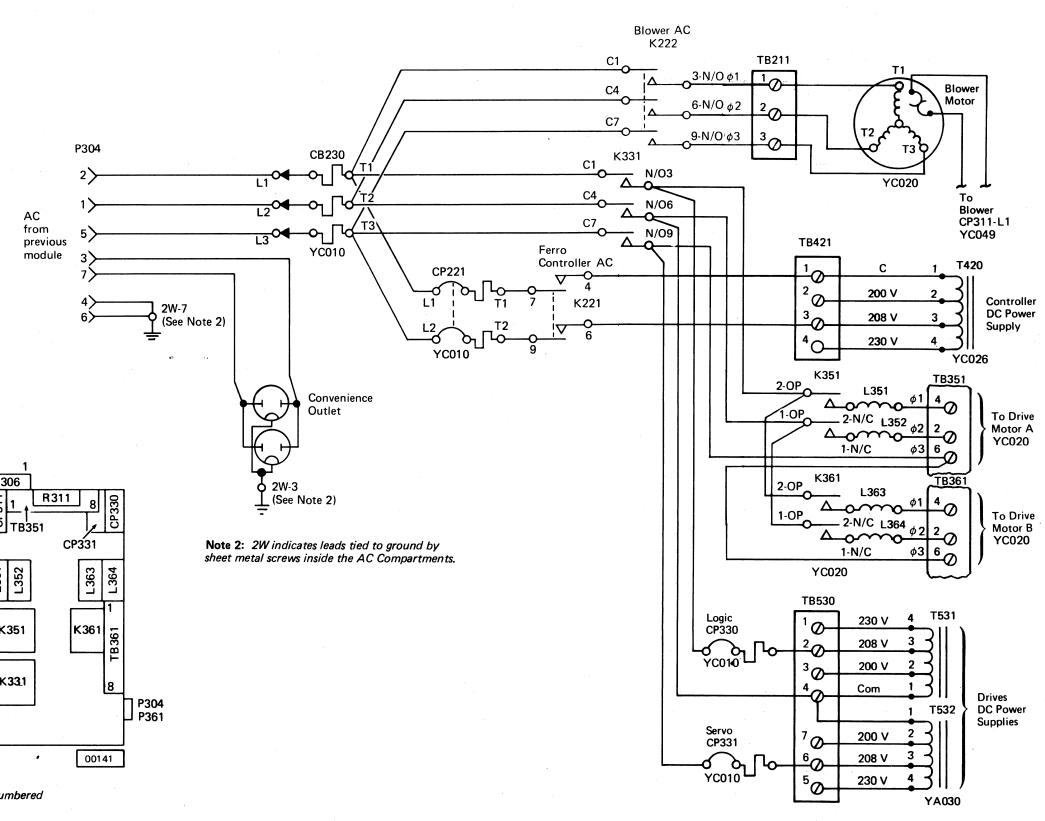
### AC CIRCUIT FAILURE ANALYSIS PWR 420

# AC CIRCUIT DIAGRAM (C2)

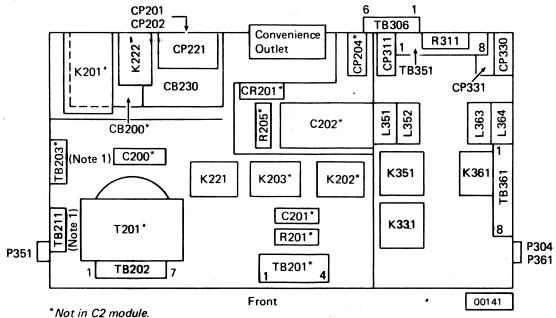
#### DANGER

LETHAL VOLTAGES are present in the power servicing area. SAFETY cannot be overemphasized. Consider ALL CIRCUITS LIVE until measured otherwise. CAPACITORS are potentially explosive devices. WEAR SAFETY GLASSES. After replacing any capacitor, reinstall all SAFETY COVERS before powering on machine.

#### See ZC100 for relay and contactor point location.



AC COMPARTMENT, Top View



Note 1: In terminal blocks TB203 and TB211 the terminals are numbered from the top to the bottom.

12.3

EG0420 2358761 441301 3350 Seq. 2 of 2 1 Jun 76 Part No.

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AC CIRCUIT DIAGRAM (C2) PWR 421

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0 0

#### **LOCATION INDEX**

LOC 2, 4, and 6 for A2 Module. LOC 12, 14, and 16 for B2 Module. LOC 22, 24, and 26 for A2 or C2 with a C2 Module attached.

#### Α

Absolute Filter LOC 2, 12, 22 AC Compartment LOC 2, 12, 22 Air Filters LOC 2, 12, 22 Air Switches LOC 6, 16, 26

#### B

Blower LOC 2, 12, 22 Boards A1 Logic LOC 2, 12, 22 A2 Logic LOC 2, 22 Sequence A LOC 4, 24 Sequence B LOC 4, 14, 24 Brake, Solenoid LOC 2, 12, 22

#### С

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#### F

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#### G

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#### Η

HDA Baseplate LOC 2, 12, 22 HDA Cables LOC 6, 16, 26

#### T

Inductors L1xx (Solenoid Brake) LOC 2, 12, 22 L3xx LOC 2, 12, 22 Solenoid Brake LOC 2, 12, 22 Interface A LOC 2, 22 Interface B LOC 2, 22 Interframe Connector (01E) LOC 12, 22

#### J

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Lights and Indicators Air A (LED) LOC 4, 14, 24 Air B (LED) LOC 4, 14, 24 Alternate (LED) LOC 26 Attention LOC 6, 16, 26 CE Dr Selection LOC 6, 26 Data (Lo Byte) LOC 6, 26 Execute Request LOC 6, 26 Parity Check CTL-I Bus Out LOC 6, 26 CTL-I Tag Bus LOC 6, 26 DEV-I Bus In LOC 6, 26 Power Check (LED) LOC 4, 14, 24 Power On LOC 6 Power Sequence Complete (LED) LOC 4, 14, 24 Primary (LED) LOC 26 Program Control (Hi Byte) LOC 6, 26 Ready LOC 6, 16, 26

Start A (LED) LOC 4, 14, 24 Start B (LED) LOC 4, 14, 24 Stop A (LED) LOC 4, 14, 24 Stop B (LED) LOC 4, 14, 24 String Power Sequence Complete (LED) LOC 4

#### N

Nipple with Cap LOC 2, 12, 22

#### 0

Operator Panel LOC 6, 16, 26

#### R

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#### S

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### LOCATION INDEX LOC 1

R/W Read LOC 6, 16, 26 Service Bypass LOC 6, 16, 26 Start/Stop, Drive LOC 6, 16, 26 S1xx LOC 6, 16, 26 S531 LOC 4, 14, 24 S7xx LOC 6, 16, 26 S8xx LOC 6, 26 S9xx LOC 6, 26 S10xx LOC 6, 16, 26

#### Т

Tailgate LOC 2, 22 **TBs** (Terminal Blocks) TB1xx LOC 2, 12, 22 TB2xx LOC 2, 12, 22 TB3xx LOC 2, 12, 22 TB4xx LOC 4, 14, 24 TB5xx LOC 4, 14, 24 Thermals Blower Motor, not shown (Thermal is internal to motor; resets as a result of cooling.) Logic Gate LOC 2, 12, 22 Transformers T2xx LOC 2 T4xx LOC 4, 24 T5xx LOC 4, 14, 24

#### V

VCM Terminals LOC 6, 16, 26

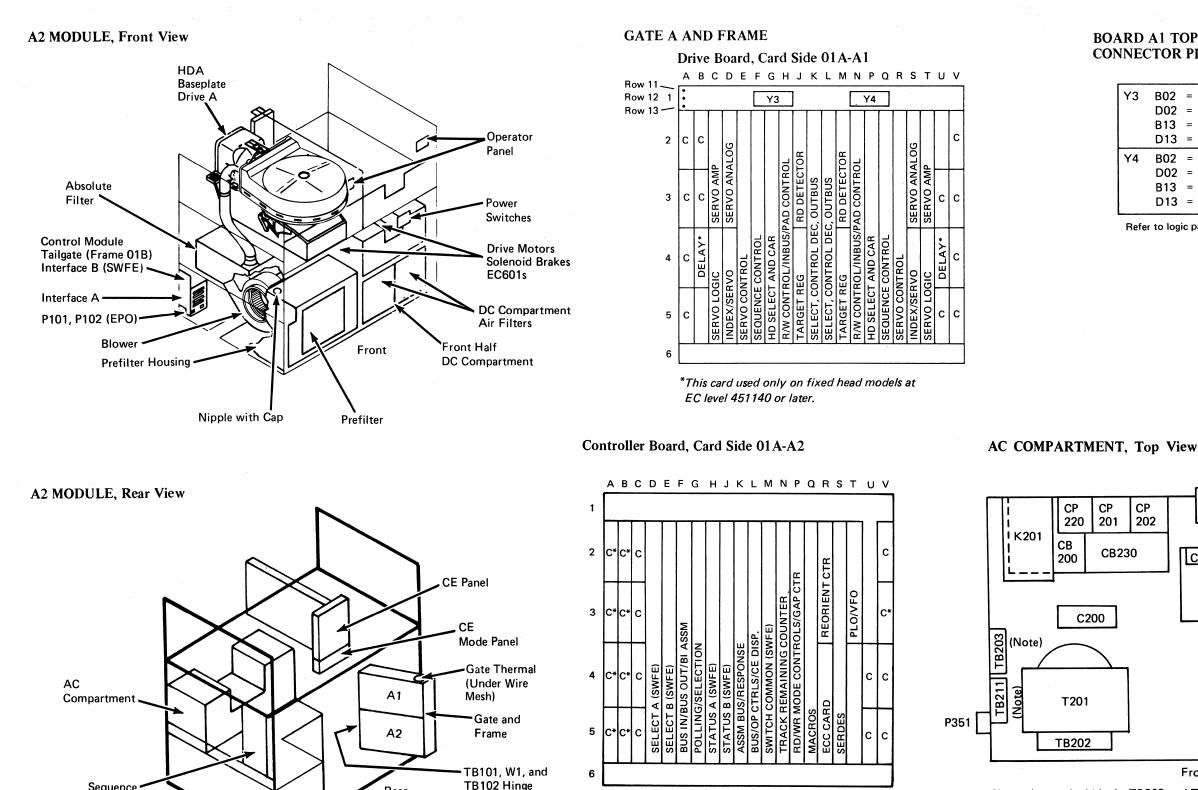
#### W

W1 LOC 2, 12, 22 2W not shown (2W indicates a lead grounded in the

AC Compartment by a sheet metal screw.)

#### LOCATION INDEX LOC 1

#### **CONTROL MODULE LOCATIONS**



Note: In terminal blocks TB203 and TB211, the terminals are numbered from top to bottom.

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3350

EH0001

Seq. 2 of 2

2358090

Part No.

441300

31 Mar 76

441301

1 Jun 76

Sequence

Panel

C indicates connector installed for basic machine.

C\* indicates connector installed for String Switch feature (SWFE).

End of Gate

Rear

**DC** Compartment

441310

27 Jun 80

Rear Half

441305

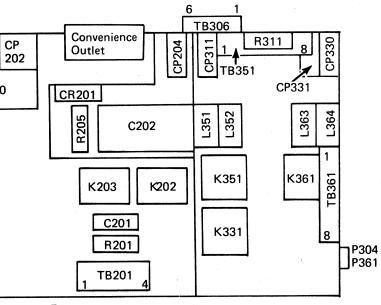
29 Oct 76

#### **BOARD A1 TOP ROW CONNECTOR PIN ALIGNMENT**

B02	=	A1H1 A13
D02	=	A1H1 A11
B13	=	A1K1 B13
D13	=	A1K1 B11
B02	=	A1L1 D13
		A1L1 D13 A1L1 D11
D02	=	
 D02 B13	=	A1L1 D11

Refer to logic page AA100.



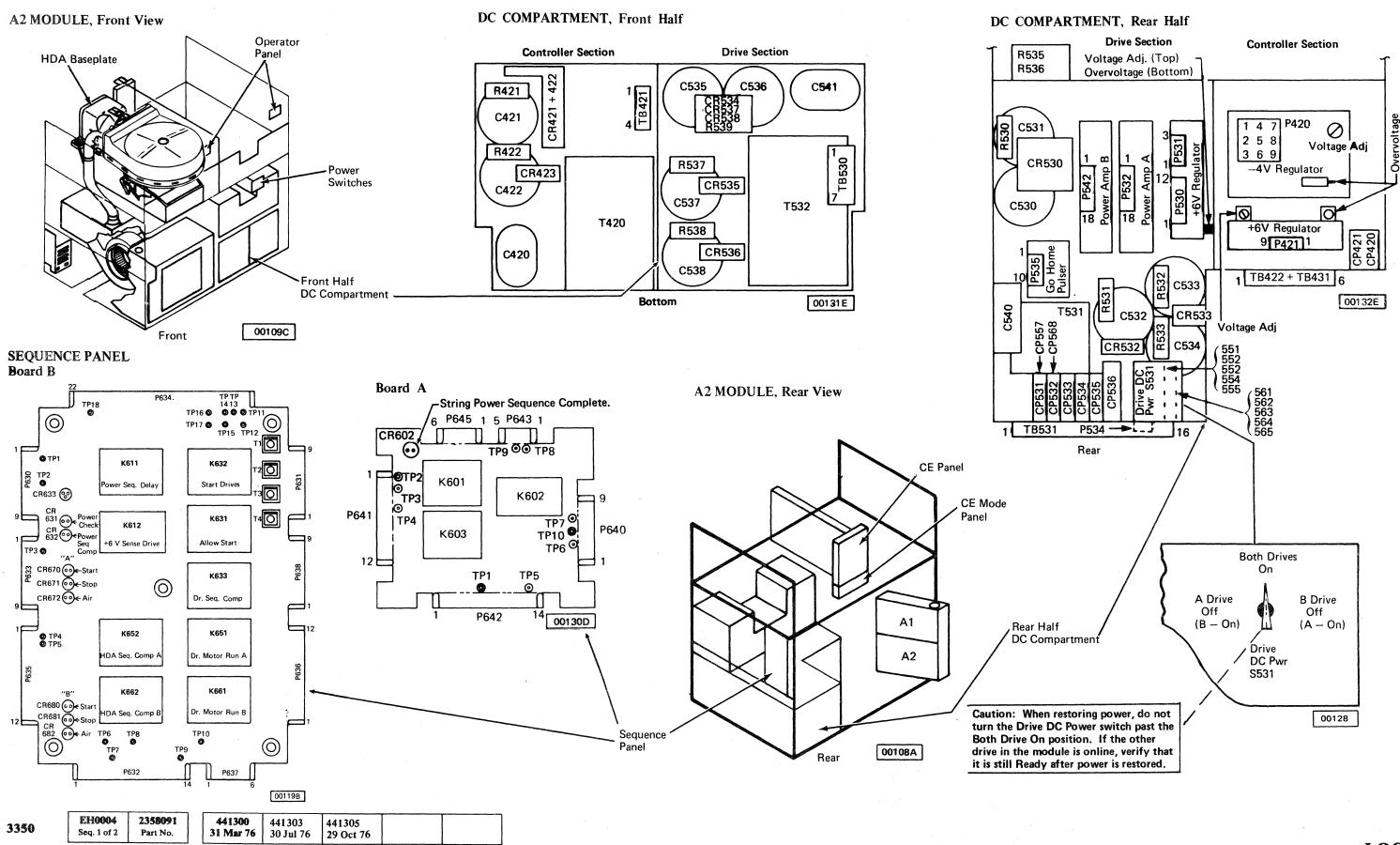


Front

CONTROL MODULE LOCATIONS LOC 2

()

## **CONTROL MODULE LOCATIONS**

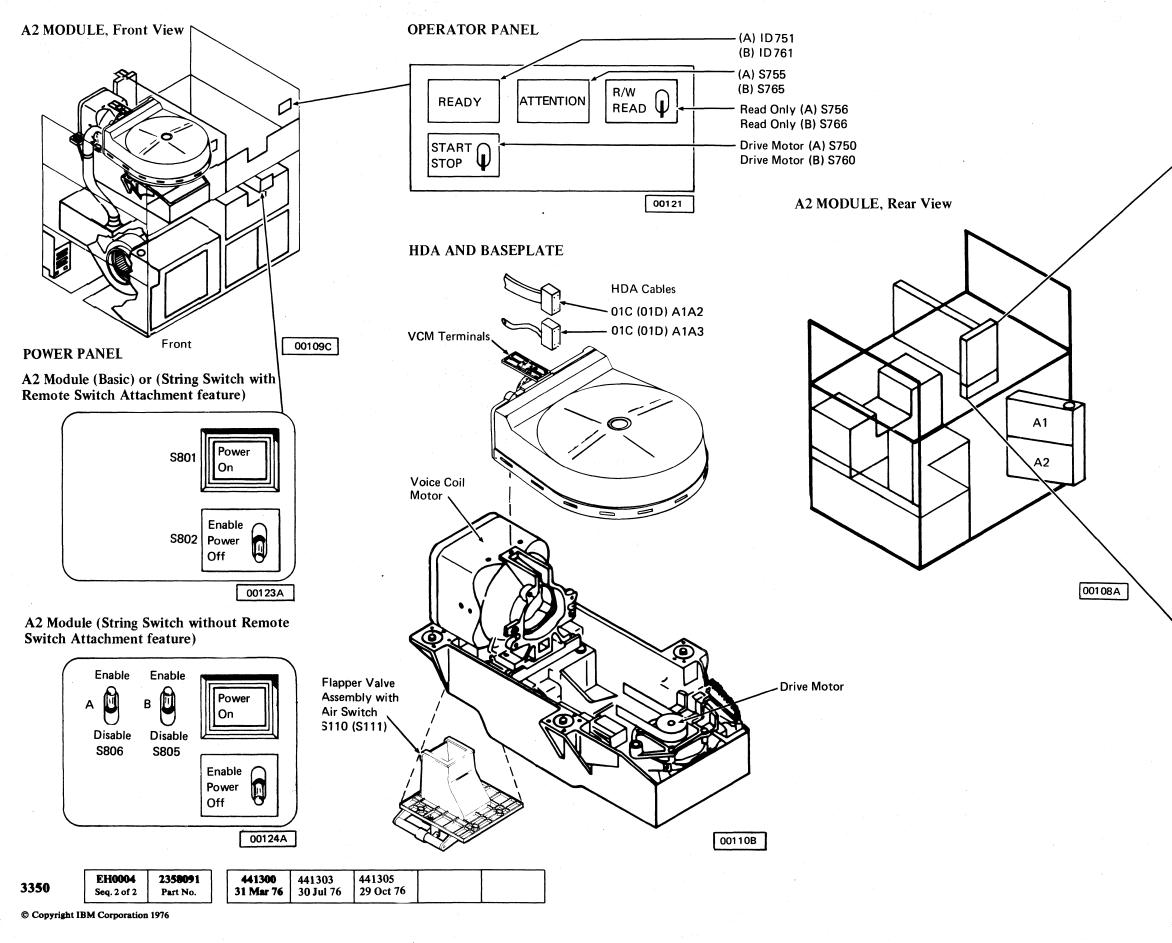


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CONTROL MODULE LOCATIONS LOC 4

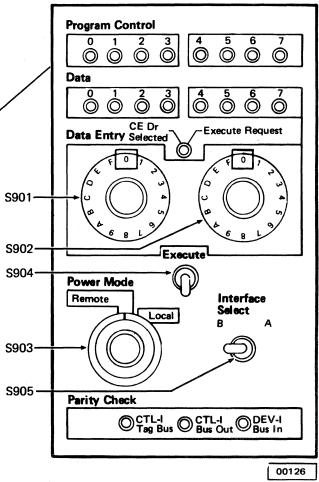
CONTROL MODULE LOCATIONS LOC 4

#### **CONTROL MODULE LOCATIONS**

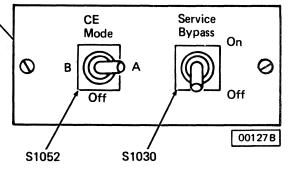


#### CONTROL MODULE LOCATIONS

#### **CE PANEL**



**CE MODE AND SERVICE BYPASS** 

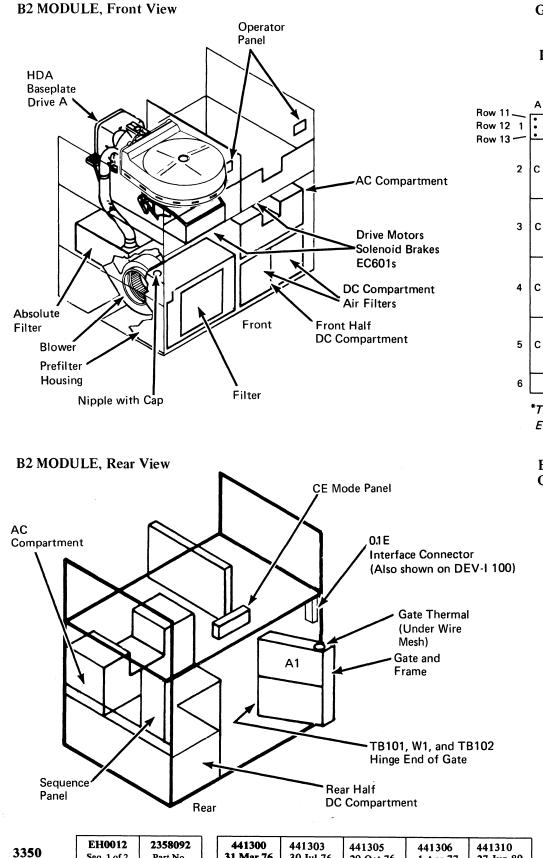


#### CONTROL MODULE LOCATIONS LOC 6

 $\bigcirc$ 

#### SATELLITE MODULE LOCATIONS

C



#### GATE A AND FRAME

Drive Board, Card Side 01A-A1

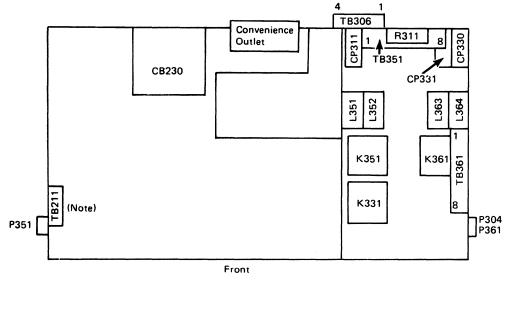
A B C D E F G H J K L M N P Q R S T U V Y3 ¥4 2 C C SERVO SERVO SERVO 1 5

\*This card used only on fixed head models at EC level 451140 or later.

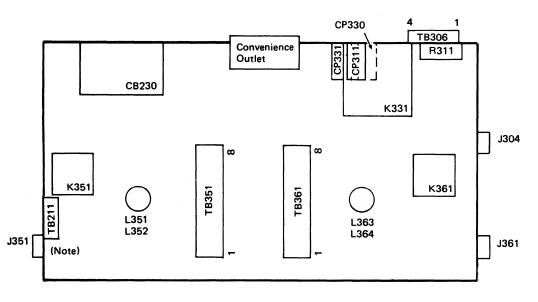
#### **BOARD A1 TOP ROW CONNECTOR PIN ALIGNMENT**

Y3	B02 =	= A1H1 A13
	D02 =	= A1H1 A11
	B13 =	= A1K1 B13
	D13 =	= A1K1 B11
Y4	B02 =	= A1L1 D13
	D02 =	= A1L1 D11
		= A1L1 D11 = A1N1 E13
	B13 =	

Refer to logic page AA100.



#### AC COMPARTMENT, Top View (later machines)



to bottom.

Seq. 1 of 2

Part No.

31 Mar 76

30 Jul 76

29 Oct 76

27 Jun 80

1 Apr 77

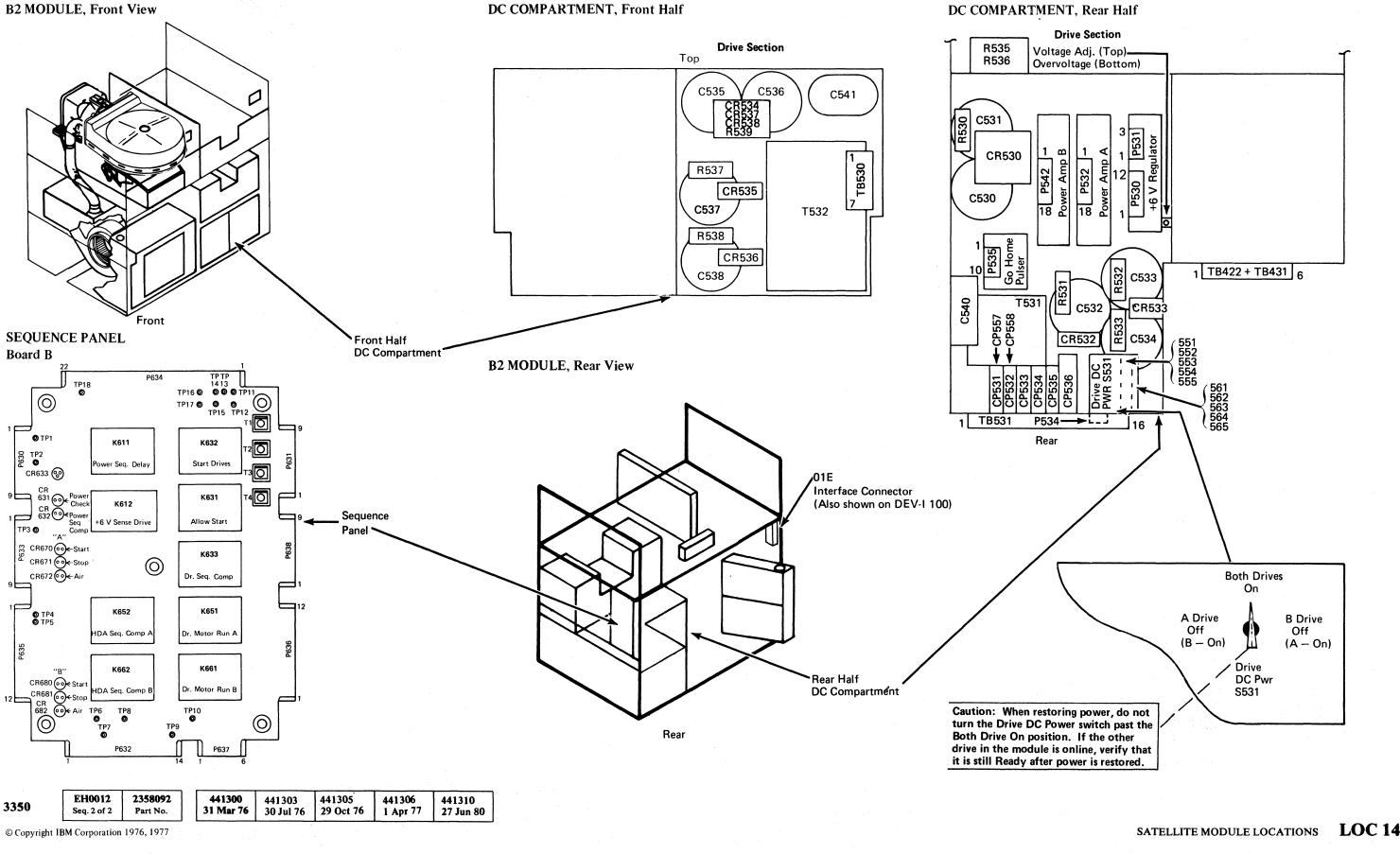
#### SATELLITE MODULE LOCATIONS LOC 12

#### AC COMPARTMENT, Top View (earlier machines)

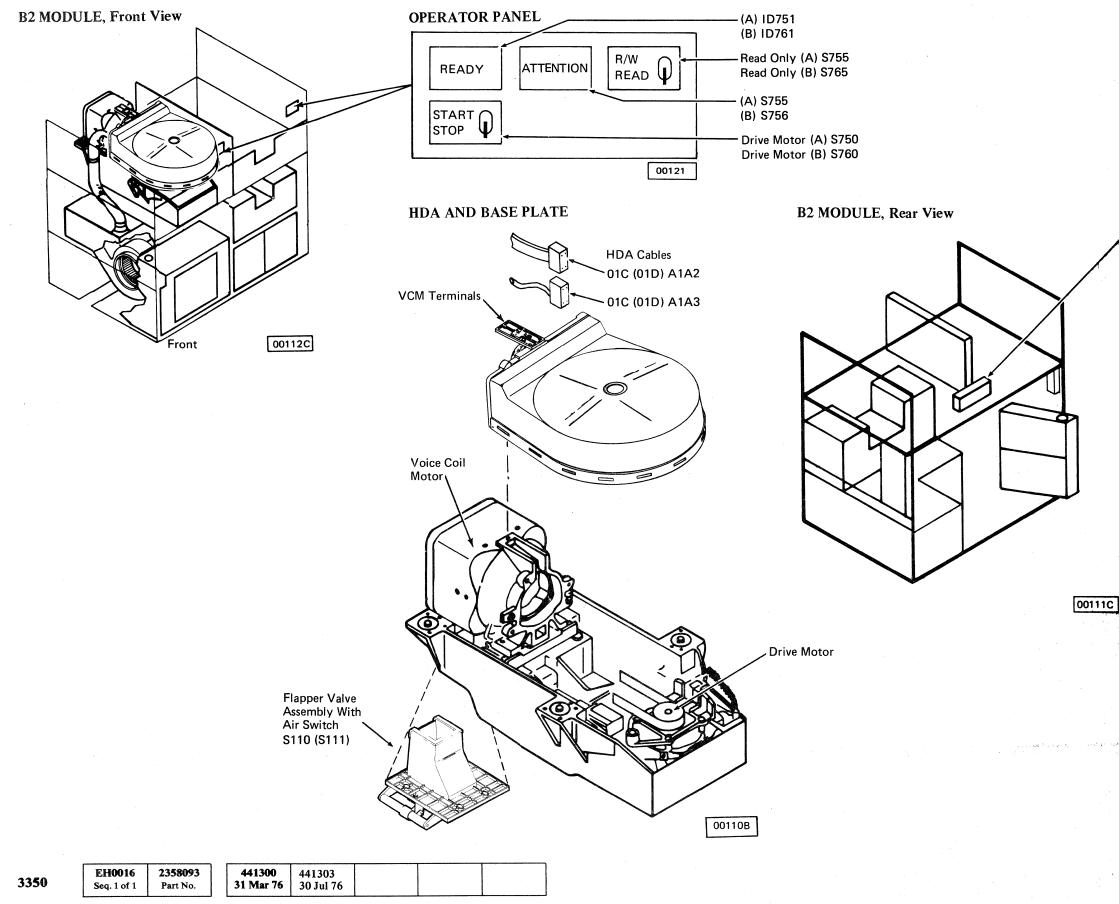
Note: In terminal block TB211, the terminals are numbered from top

#### SATELLITE MODULE LOCATIONS LOC 12

#### SATELLITE MODULE LOCATIONS



#### SATELLITE MODULE LOCATIONS



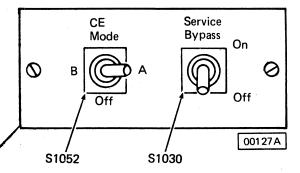
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演奏

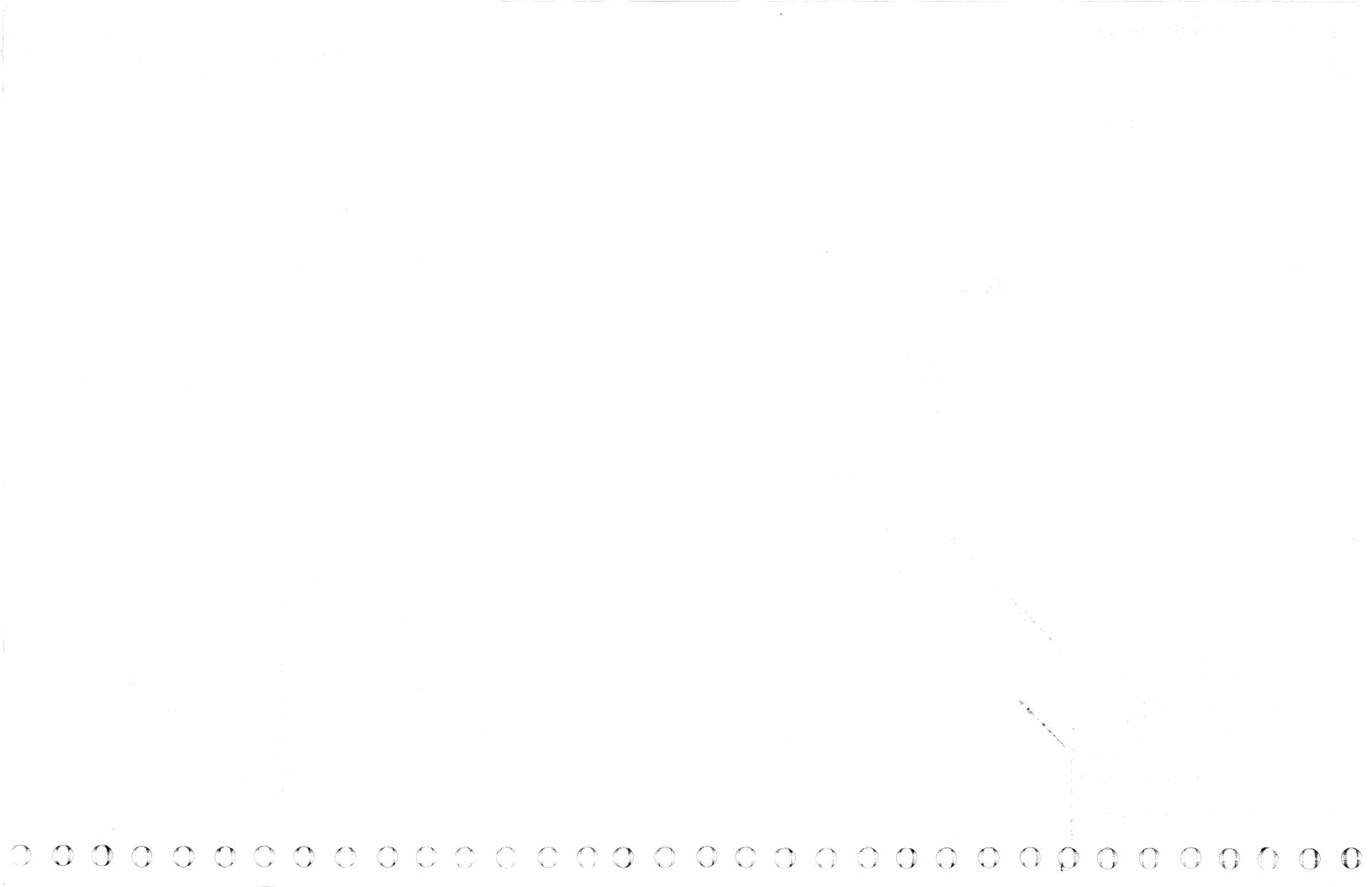
.

C

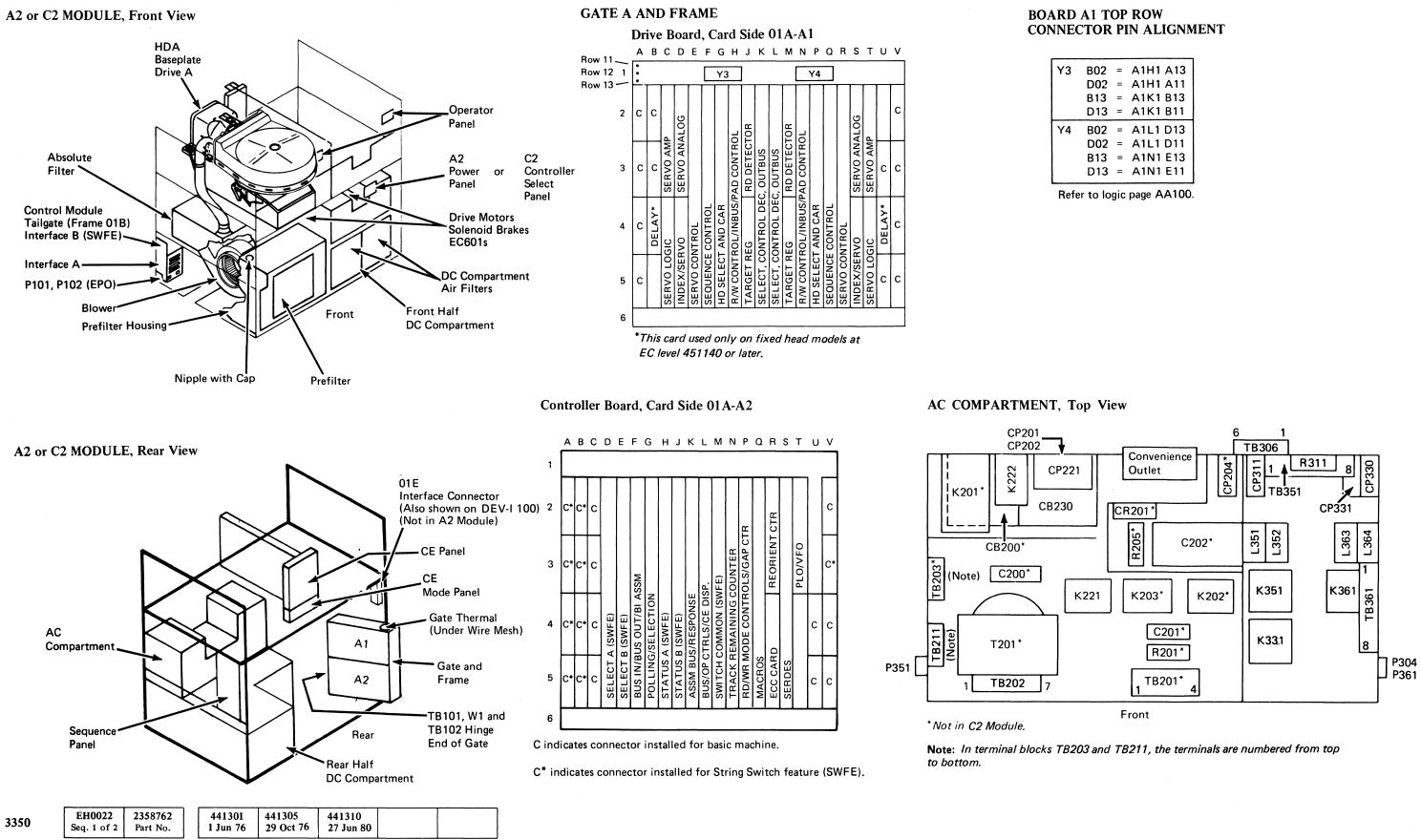
#### **CE MODE AND SERVICE BYPASS**



## SATELLITE MODULE LOCATIONS LOC 16



#### **CONTROL MODULE LOCATIONS (A2 or C2 Module)**



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LOC 22

13	B02	=	A1H1 A13
	D02	=	A1H1 A11
	B13	=	A1K1 B13
	D13	=	A1K1 B11
44	B02	=	A1L1 D13
	D02	=	A1L1 D11
	B13	=	A1N1 E13
	D13	=	A1N1 E11

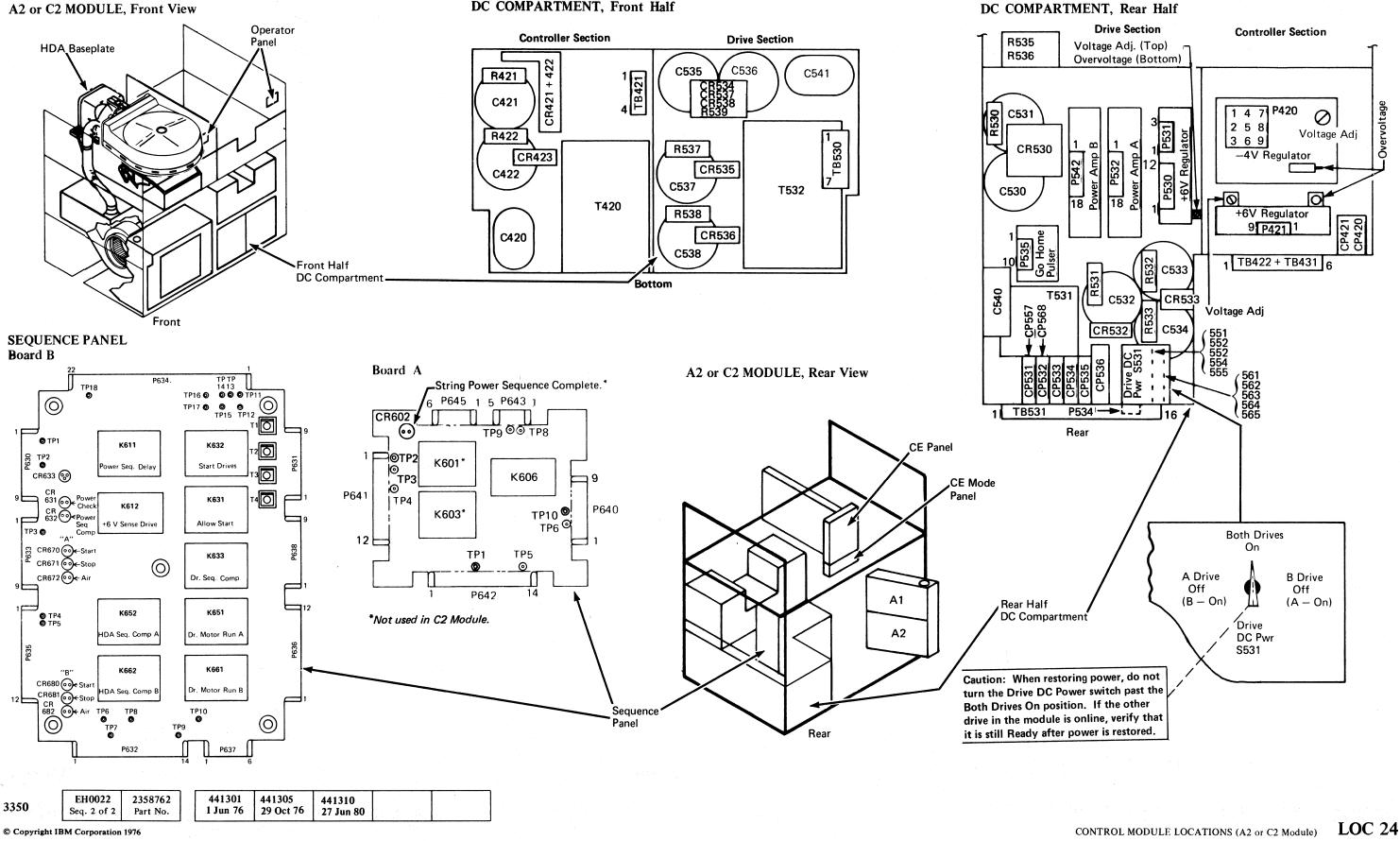


LOC 22

#### **CONTROL MODULE LOCATIONS (A2 or C2 Module)**



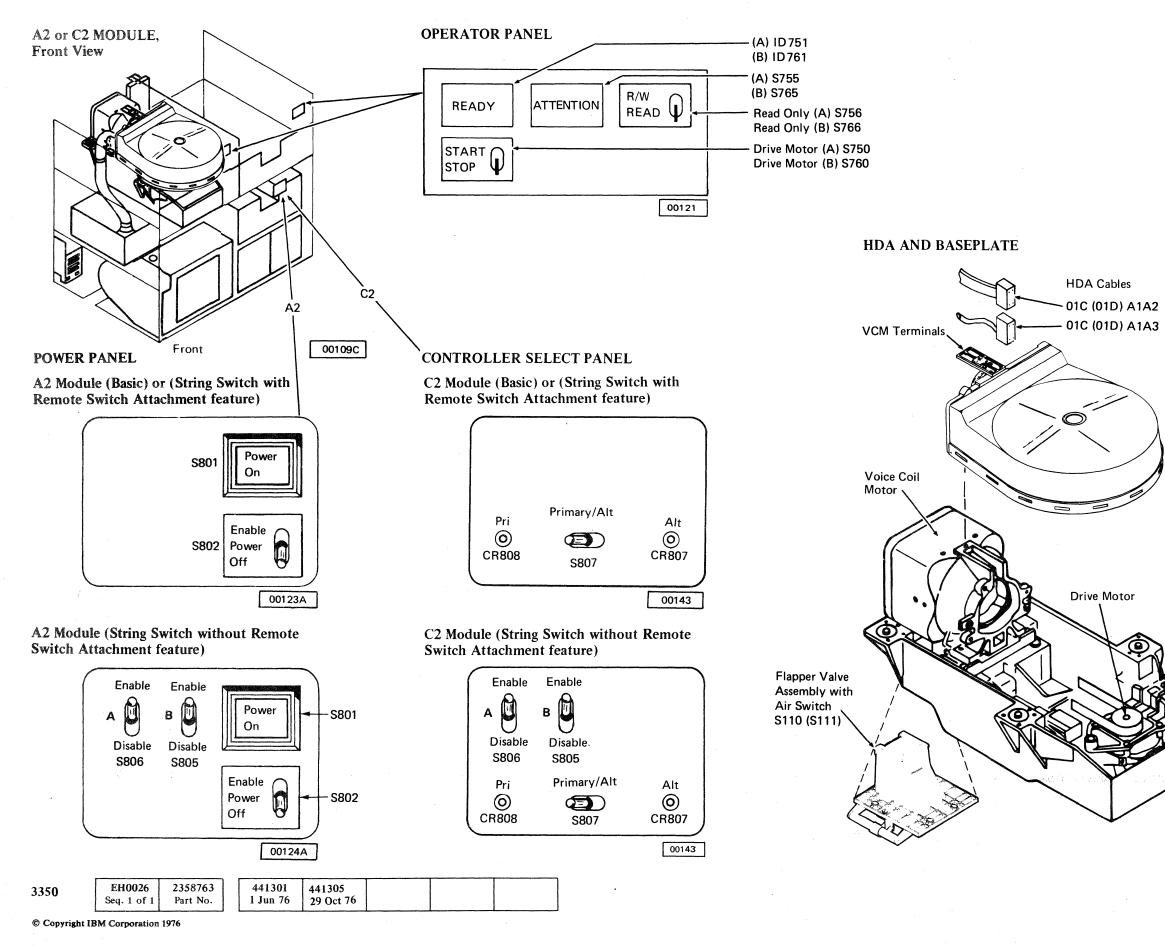
#### DC COMPARTMENT, Front Half



#### LOC 24

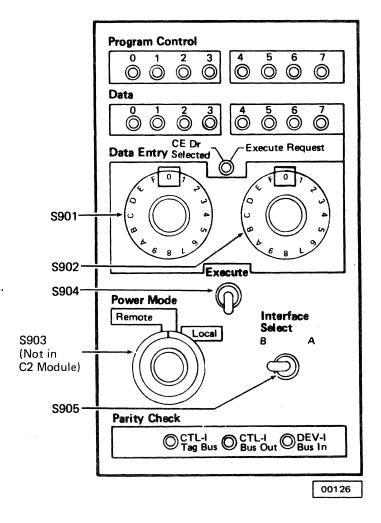
#### CONTROL MODULE LOCATIONS (A2 or C2 Module)

## **CONTROL MODULE LOCATIONS (A2 or C2 Module)**

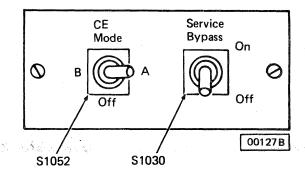


## CONTROL MODULE LOCATIONS (A2 or C2 Module) LOC 26

#### **CE PANEL**

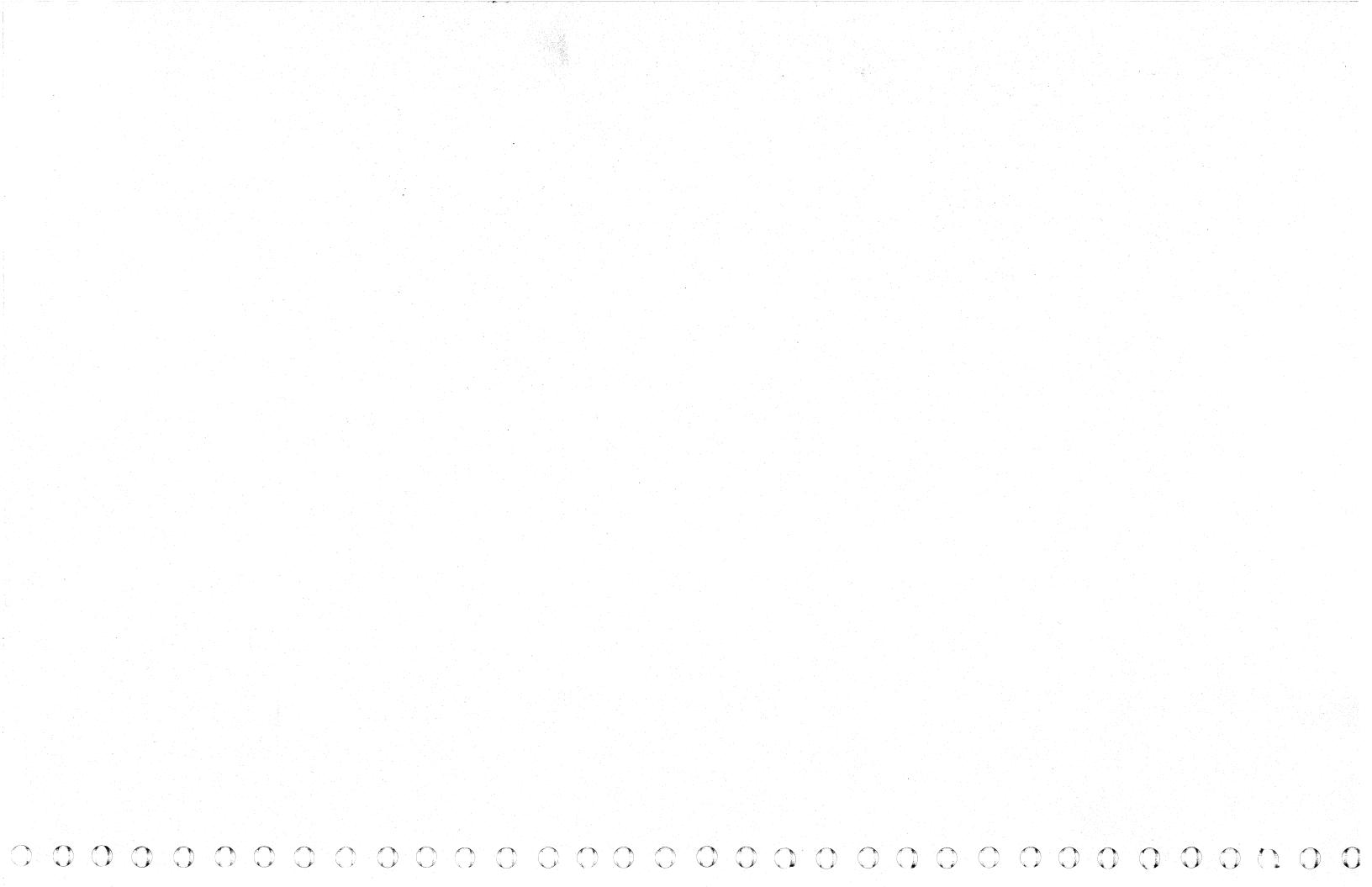


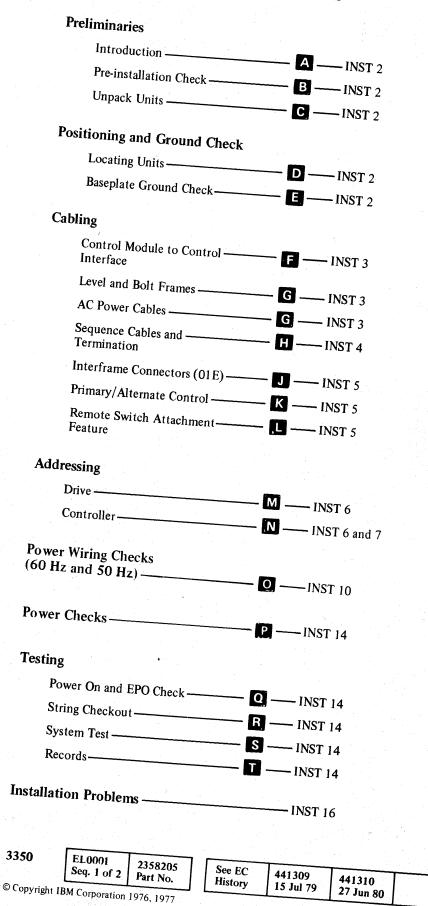
#### **CE MODE AND SERVICE BYPASS**



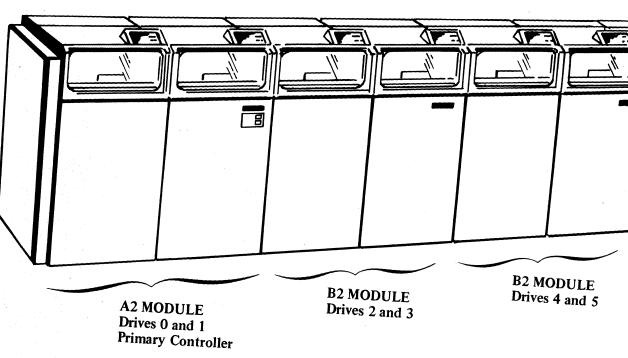
00110B

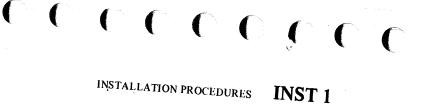
LOC 26





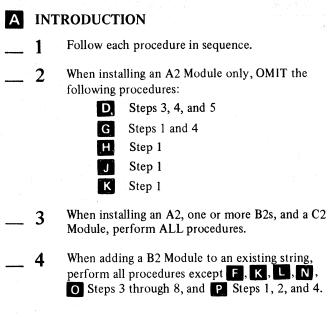
## 3350 DISK STORAGE





# 

**B2 MODULE** Drives 6 and 7 or C2 MODULE Drives 6 and 7 Alternate Controller



5 When adding a C2 Module to an existing string, perform ALL procedures.

#### SPECIAL TOOLS AND TEST EQUIPMENT

Required for installation:

Tools		Part Number
Digitec Voltmeter <sup>†</sup> (Branch office)		453585
Scope	453	453047
(Branch office)	or 454	453550
	or 475	453215
CTL-I Test Card (Branch office)		2758440
Bobbin Pushrod (A2 Shipping Group)		2758393
C2 Terminator Cards		
(C2 Shipping Group)		451(05)
Card (1 wide) Card (2 wide)		4516956 4516953

#### **B PRE-INSTALLATION CHECK**

Check with the IBM Branch Office or area Physical Planning Representative to ensure that installation planning requirements are met (service receptacle voltage, phase rotation, grounding, and cable lengths). When attaching a 3350 to an existing system Storage Control, check that the correct attachment features are installed. The attachment feature should be ordered on an MES by the responsible sales office before installation of the 3350.

The installation of a C2 Module requires the Primary Controller Adapter feature in the A2 Module. See Figure 1 for all 3350 Feature codes and Field Bill of Materials.

**Note:** If Primary Controller Adapter feature is required but not installed, the procedure in step K will allow for temporary installation of the C2.

#### **C** UNPACK UNITS

1 Use packing/unpacking instructions that are taped to the cover. Remove packing. Check for damage.

Do not remove the bobbin shipping rod from the rear of the voice coil motor at this time.

#### - 2 Inventory the parts in the shipping group. Use the Bill of Material listing:

BM 2758190 (A2) BM 2758191 (B2) BM 2758590 (C2)

#### **D** LOCATE UNITS

If installing an A2 Module only, OMIT Steps 3, 4, and 5.

- 1 Remove all covers, except the top.
- 2 Position the A2 Module.
- 3 For multiple module installation, remove the end cover and mounting hardware from the A2 Module for re-installation on the last B2 or C2 Module. See diagram on INST 1.
- 4 For multiple module installations, determine the operating mode of each spindle from the customer and locate the modules as required. Keep modules approximately 6 inches apart. Do not adjust leveling jacks yet.
  - 5 If installing a B2 or C2 Module, remove the end cover and mounting hardware from the previous last module on the string and re-install the end cover on the new last module.

Feature	Factory	Field Bill of Material Numbers								
Code	B/M		8150 w/o 1320	1320 w/o 8150	8150 w/1320	1320 w/8150	8150 + 1320			
8150	2757400 (Complete B/M)	To Add	2757395 (A02/A2F) or 2757424 (C02/C2F)		2757418		4516959			
String Switch	2757405 (FEALDs)	To Remove	2757396 (A02/A2F) or 2757426 (C02/C2F)		2757419		4516960			
1320 Primary Controller	2757392 (60 Hz) 2757856	To Add		2757394 (60 Hz) 2757850 (50 Hz)						
Adapter (50 Hz) without 8150 2757406 (FEALDs)	To Remove		2757404 (60 Hz) 2757851 (50 Hz)							
1320 Primary Controller	2757393 (60 Hz) 2757857	To Add				2757405 (60 Hz) 2757854 (50 Hz)	2757427 (60 Hz) 2757852 (50 Hz)			
Adapter (50 Hz) with 8150 2757632 (FEALDs)	To Remove				2757429 (60 Hz) 2757855 (50 Hz)	2757428 (60 Hz) 2757823 (50 Hz)				
6148	2757399 (8150 is	To Add	2757397 (For A2)	4517010 (For C2)						
Remote Switch	Prerequisite)	To Remove	2757398 (For A2)	2757398 (For C2 also)						

† Trademark of United Systems Corporation.

			_				
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#### **E BASEPLATE GROUND CHECK**

Modules must be separated and no cables connected between modules during this check.

- Remove the jumper from W1-12 to frame ground at the W1 end for each 3350 being installed. W1 is located on the logic gate (INST 4).
- 2 If installing an A2/C2 Module, pull the ribbon connectors from the following locations to remove ground connections at the tailgate:
  - On a basic machine without the string switch feature:

A2C2, A2C3, A2C4, A2C5

- With the string switch feature: A2A2, A2A3, A2A4, A2A5 A2B2, A2B3, A2B4, A2B5
- Check that the resistance between each baseplate and frame ground is at least 1 megohm.

Baseplates are connected through the servo and R/W matrix card cables and by leads to the dc common terminal block (W1) on the logic gate.

4 If resistance is less than 1 megohm, a grounding condition exists. Correct this problem first. For additional information, see the Power section of the Logics (YA/YB/YC) and the PWR pages in the MIM. (Check that HDA shipping blocks are removed, the Power Amp card in the DC compartment is not loose, and that the shock mounts are properly installed.)

5 Reconnect the jumper at the ground bus and reinstall the ribbon cables.

**Note:** If a ground check is required between the host system and the 3350, the interface cables should be disconnected.

#### INSTALLATION PROCEDURES

#### $O \cap O \cap O \cap O \cap O$

#### **INSTALLATION PROCEDURES**

#### F CABLING CONTROL MODULE (A2/C2) TO **CONTROL INTERFACE**

Connect EPO cable (P/N 5351178) from control module tailgate (A2 only) to Storage Control EPO. The EPO cable pigtail (ground) does not need to be connected at the 3350 end. It should be taped back against the cable body. Connect J101 to storage control 1 and J102 to storage control 2.

> Note: If it is inconvenient at this time to connect the EPO cable, use the shorting plug assembly (P/N 2282264 in A2 Shipping Group), but the EPO cable should be connected as soon as possible.-

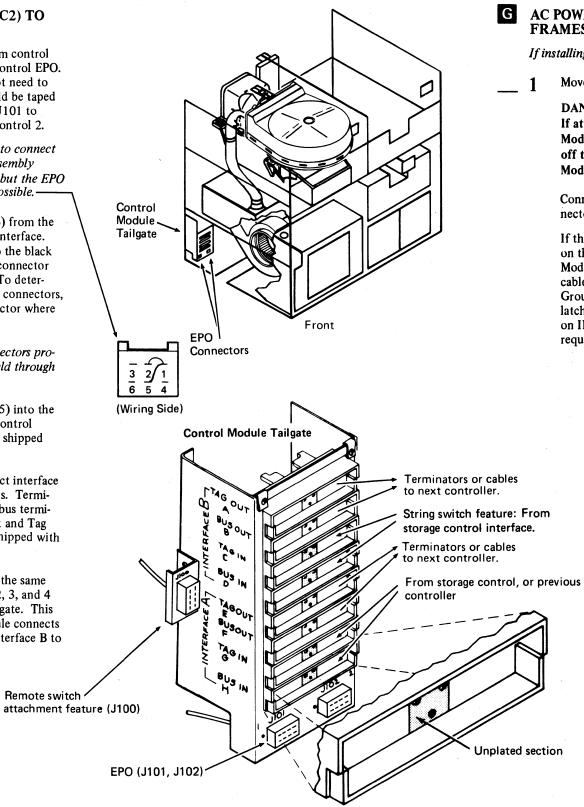
Connect interface cables (P/N 5466456) from the control module tailgate to the control interface. Plug the light grey cable connector into the black tailgate connector and the black cable connector into the light grey tailgate connector. To determine the color of the new style tailgate connectors, look at the center portion of the connector where it is not plated.

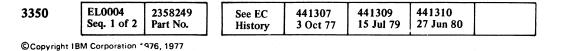
> Note: The plating on the tailgate connectors provides a ground path from the cable shield through the tailgate to the 3350 frame.

Plug two bus terminators (P/N 2282675) into the 3 Bus Out and Tag Out positions in the control module tailgate. These terminators are shipped with the storage control.

If installing multiple controllers, connect interface cables in Bus Out and Tag Out positions. Terminate at last controller by plugging two bus terminators (P/N 2282675) into the Bus Out and Tag Out positions. These terminators are shipped with the storage control.

If installing a C2 Module, connect it in the same way as an A2 Module. Perform Steps 2, 3, and 4 of this procedure at the C2 Module tailgate. This means that Interface A in the A2 Module connects to Interface A in the C2 Module and Interface B to Interface B.





AC POWER CABLES, LEVEL AND BOLT **FRAMES** 

If installing an A2 Module only, OMIT Steps 1 and 4.

Move all units together.

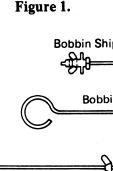
DANGER

If attaching to a previously installed A2 or B1/B2 Module, the AC power must be removed by turning off the main line disconnect (CB201) in the A2 Module.

Connect ac power cable from B2/C2 to the connector on A2 or B2 AC Compartment (P304).

If the last module is a C2 Module, relieve the strain on the AC power cable in the preceding B2 Module by using the screw (P/N 2181004) and cable clamp (P/N 350664) in the C2 Shipping Group. Place the screw in the upper tapped cover latch hole. This hole, shown in left hand module on INST 4, is available because the latch is not required in the last B2 Module





#### INSTALLATION PROCEDURES INST 3

- Verify with a CE meter that a direct short exists between the AC Compartments of the modules. (Check the green and yellow ground wire from AC Compartment to AC Compartment for 0.1 or less ohms.) If the reading is not within this range, investigate and correct the condition.
- Adjust leveling jacks for appearance and/or ease 3 of inserting frame tie bolts.

Caution: Before tightening bolts, check that no cables are caught between frame members.

Bolt frames together using:

3 bolts (P/N 59652 in B2/C2 Shipping Group) 3 washers (P/N 6935 in B2/C2 Shipping Group) 3 nuts (P/N 39600 in B2/C2 Shipping Group)

Remove the bobbin shipping rod (Figure 1) from the rear of the voice coil motor.

**Note:** Store the bobbin shipping rod in the clips located at the rear of the module on the VCM.

**Caution:** The tool must be re-installed whenever the machine is moved even for short distances.

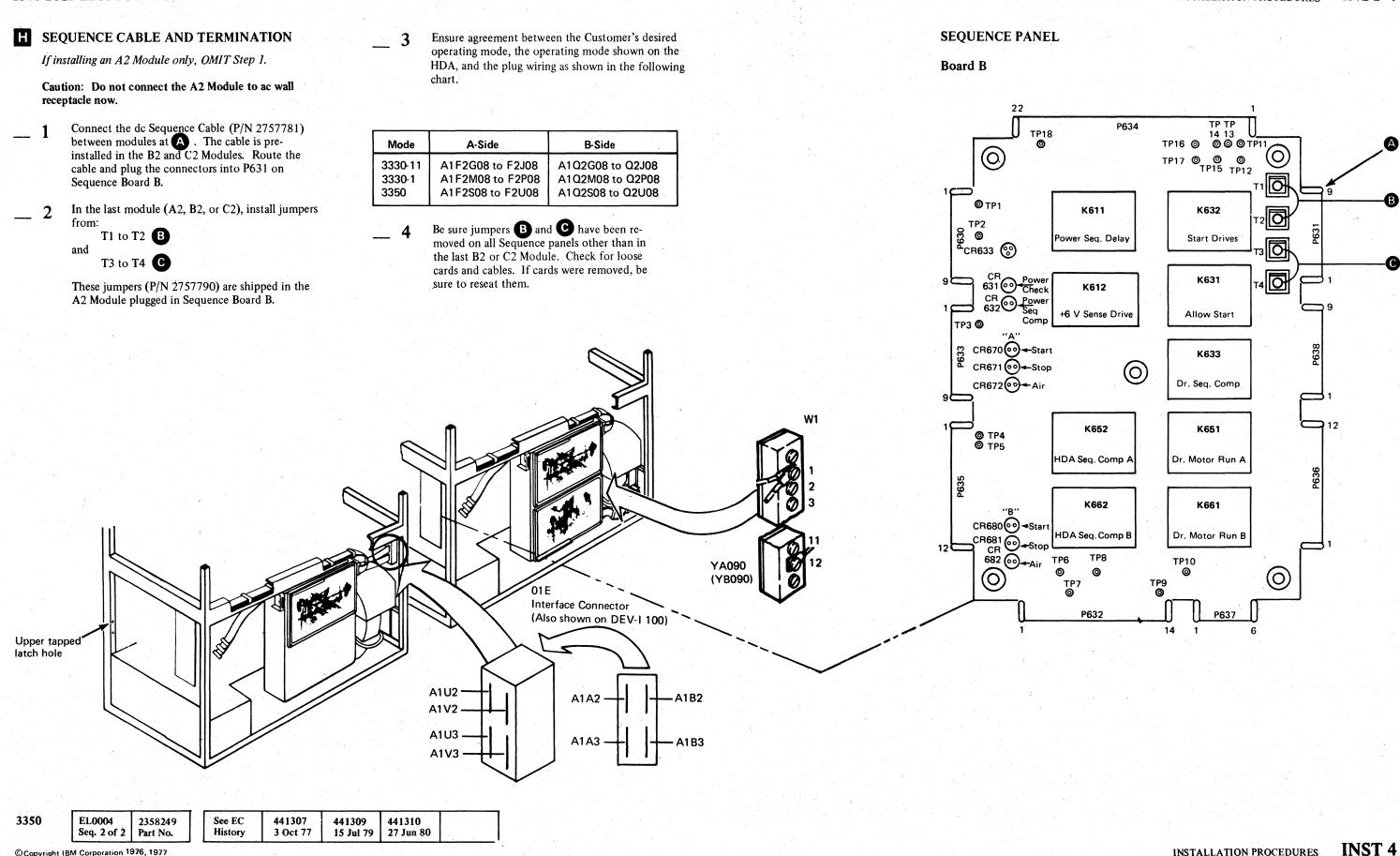
If at a later time the bobbin must be retrieved at the inner diameter (ID), thread the bobbin pushrod (P/N 2758393) into the shipping rod. Loosen the wingnut and washer and insert the combined tools. After the bobbin is returned to outer diameter (OD), slip the washer and wingnut back over the stud on the shipping rod and hand-tighten. Prevent the rod from turning by applying an open-end wrench to the stud at the end of the shipping rod, which has flats provided for this purpose.

Caution: Do not overtighten the rod or wingnut. Fingertight is tight enough.

Bobbin Shipping Rod (P/N 2758392)

Bobbin Pushrod (P/N 2758393)

**Combined Tools** Flats



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INSTALLATION PROCEDURES

INST 4

INSTALLATION PROCEDURES

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#### **INSTALLATION PROCEDURES**

#### J **CABLING INTERFRAME CONNECTORS**

If installing an A2 Module only, OMIT Step 1.

Plug the ribbon cables in the appropriate slot in the interframe connector.

Insert the 2-wide terminator (P/N 5863806) in the 2-wide card guide (P/N 811804). These items are supplied in the A2 Shipping Group. Install the assembly in A1A2 (Drive Board 01A) in place of the cables in the last module on the string.

> Insert the 1-wide terminator (P/N 8250634) in the 1-wide card guide (P/N 811802). These items are supplied in the A2 Shipping Group. Plug it into A1B3 (Drive Board 01A) in place of the cables in the last module on the string. Tie the three flat cables (from A1A2, A1A3, and A1B3) together on the outwide of the gate using cable tie P/N1159519 (in A2 Shipping Group).

If a B2 Module is being added to the string, move the terminators to the new last module, and replug the cables as marked on the cable-ends. Follow the procedure above for plugging the terminator cards.

If a C2 Module is being installed, the terminator cards are not needed; termination is done by the A2F2, A2G2, A2L2, and A2T2 cards. Replug the cables in the previous last module after removing the terminators.

CONTROL	SATELLITE	SATELLITE
MODULE	MODULE	MODULE
01A-A1 BOARD	01A-A1 BOARD	01A-A1 BOARD
U B 2 2 3 3 4 4 5 ( 5	$ \begin{array}{c}     U \\             B \\             \hline           $	U B 2 7 2 2 3 3 4 4 (P/N 825063

#### 534) 7. 7 Interframe Interframe 01E 01F Terminator (P/N 5863806) 5

	<u> </u>	N	1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1. 1	1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 - 1997 -		And the second second	
3350	EL0007 Seq. 1 of 2	2358765 Part No.	See EC History	441308 18 Aug 78	441309 15 Jul 79		
			 			the second s	

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#### CABLING PRIMARY/ALTERNATE CONTROL CABLE Κ

3350 A2 Module with Primary Control Adapter (PCA) feature or C2 Module only.

Route the cable (P/N 2758575), looped on the side of the C2 Module, through all B2 cable troughs and install at A2U3 in the A2 Module.

The following allows for temporary installation of A2 and C2 modules when either Primary Control Adapter (PCA) is not installed on A2 module or when the PCA is present and C2 module is not present. Action should be taken to restore the string to normal configuration as soon as possible. (See INST 2, Figure 1.)

- a. To install a C2 module on a 3350 A2 Module without the Primary Control Adapter feature (PCA - feature code1320):
- Install in the normal configuration.
- Do not plug the cable P/N 2758575 into A2U3 in the A2 module.

Note: The C2 module cannot be used as a controller until the PCA feature is installed on the A2 module and the cable plugged into A2U3 of A2 module.

- b. To install a 3350 A2 Module with PCA (feature code 1320) and shipped without a C2 Module:
- Install in the normal configuration.
- Connect the following to jumpers in the A2 module
  - A2M2M11 to ground A2M2P03 to ground

Terminate normally in the last B2 Module.

#### **CONNECT REMOTE SWITCH ATTACHMENT FEATURE PLUG**

3350 A2/C2 only.

This feature permits the selection of Channel A or B at the CPU Console instead of at the Power Panel on the A2 Module or at the Controller Select Panel on the C2 Module. Thus, if String Switch is installed with the Remote Switch Attachment feature, the A2/C2 Module has no Enable/Disable A or B switches.

The cable from the CPU connects to the A2/C2 Module at J100 located on the Control Module Tailgate (see INST 3). J100 is shown on ALD page ZA040.

#### **INSTALLATION PROCEDURES**

INST 5

#### INSTALLATION PROCEDURES

#### Μ **DRIVE ADDRESSING**

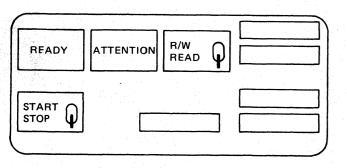
Install customer-assigned physical address labels (P/N 5412746 in A2 Shipping Group) in the recesses on the Operator Panel.

> When in 3330-1 Compatibility Mode, each spindle has a primary and a secondary address. The secondary address equals: Primary address + '20'.

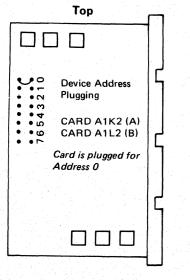
#### Examples:

Primary address	= 143
Secondary address = 143 + '20'	= 163
Primary address	= 18E
Secondary address = 18E + '20'	= 1 AE

#### **Operator Panel**



Establish each drive address by connecting jumper 2 points on card A1K2(A1L2). The drive addresses need not be in sequence, but no two can be plugged alike. The jumper (P/N 816645) is on the card.



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Copyright I	BM Corporation	976, 1977			

CONTROLLER ADDRESSING

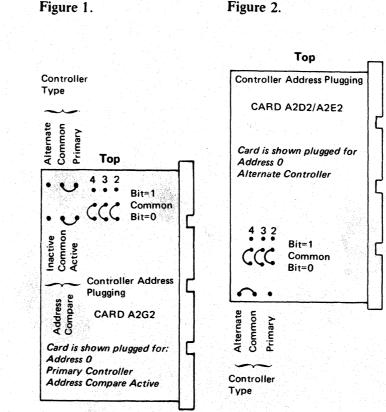
N

3350 A2 and/or C2 Module only.

Plug the address card(s) for the controller address(cs) assigned. Addresses are shown in Chart A, see Note. Plug the address cards (see Figures 1 and 2) by selecting the correct Controller Configuration in column one of the chart on INST 7 and following the plugging instructions to the right of that configuration.

Jumpers are included on the A2G2, A2D2, and A2E2 cards and may require re-plugging for correct addressing.

Check that Storage Control addresses are correct for this configuration.



#### Chart A

Controller	Plug	Addresses
	432	X00 – X07
0	• • •	X20 – X27
U	CCC	X40 - X47
	666	X60 - X67
		X80 – X87
		XA0 – XA7
		XC0 – XC7
		XE0 – XE7
	432	X08 - X0F
1	· · ·	X28 – X2F
	C	X48 — X4F
		X68 – X6F
		X88 – X8F
		XA8 – XAF
		XC8 – XCF
		XE8 – XEF
	432	X10 - X17
2	• • •	X30 – X37
۷	مام	X50 – X57
		X70 – X77
		X90 – X97
		XB0 - XB7
		XD0 – XD7
		XF0 - XF7
	4 3 2	X18 – X1F
3	La	X38 – X3F
•	66.	X58 – X5F
	•••	X78 – X7F
		X98 – X9F
		XB8 – XBF
		XD8 – XDF
		XF8 – XFF

If attached to 3880, see Note.

Note: If attachment is to a 3880 use the 3880 INST section to determine the correct controller for the given address range and string configuration. Plug A2G2 using chart A and INST 7 for the controller assigned.

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#### **CONTROLLER ADDRESS PLUGGING**

Figure 1, Figure 2, and Chart A, referenced in this chart, are located on INST 6.

Controller Configuration	Address Plugging	Address Compare	Primary/Alternate
Basic A2 Module Without String Switch feature Without a C2 Module	A2G2 (Figure 1) with address (0-3) from Chart A.	Common to Active on A2G2.	Common to Primary on A2G2.
A2 Module with String Switch feature Without a C2 Module Both A and B Interface addresses of A2 Module are identical	A2G2, A2D2, and A2E2 (Figures 1 and 2) with identical addresses (0-3) from Chart A.	Common to Active on A2G2.	Common to Primary on A2G2, A2D2, and A2E2.
A2 Module with String Switch feature Without a C2 Module Interface A and B addresses of A2 Module are different	A2D2 (Figure 2) with Interface A address (0-3) and A2E2 with Interface B address (0-3) from Chart A. (Plug A2G2 with either address.)	Common to Inactive on A2G2 (Figure 1). Addresses are compared by the A2D2 and A2E2 cards. (A2G2 must be plugged.)	Common to Primary on A2G2, A2D2, and A2E2.
A2 Module with a C2 Module Without String Switch feature on either A2 or C2 Module	A2G2 (Figure 1) in both A2 and C2 Modules are plugged with the same address (0-3). See Chart A.	Common to Active on A2G2 in both the A2 and C2 Modules.	Common to Primary on A2G2 in the A2 Module and Common to Alternate in the C2 Module.
A2 Module with a C2 Module With String Switch feature on either or both A2 or C2 Module Interface A and B addresses identical	A2G2 (Figure 1), A2D2 (Figure 2), and A2E2 with identical ad- dress (0-3). See Chart A. Address plugging must be performed in both A2 and C2 Modules if both Modules have the String Switch feature.	Common to Active on A2G2 in both the A2 and C2 Modules.	Common to Primary on all three cards in the A2 Module and Common to Alternate in the C2 Module.
A2 Module with a C2 Module With String Switch feature on either or both A2 or C2 Module Interface A and B addresses different	A2D2 (Figure 2) with Interface A address and A2E2 with Interface B address (0-3). See Chart A. Interface A in both the A2 and C2 Modules must have the same address, and Interface B in the A2 and C2 Modules must have the same address. (Plug A2G2 with either address.)	Common to Inactive on A2G2 (Figure 1) in the A2 and C2 Modules. Addresses are compared by the A2D2 and A2E2 cards in both the A2 and C2 Modules. (A2G2 must be plugged.)	Common to Primary on all three cards in the A2 Module and Common to Alternate in the C2 Module.

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INSTALLATION PROCEDURES INST 7

INSTALLATION PROCEDURES INST 7

#### **O** POWER WIRING CHECKS

Steps 3 through 8 are for A2 Modules only.

This procedure is for all A2, B2, and C2 Modules. Do not leave this page until all modules being installed are checked using this procedure.

- In all modules being installed, set the drive Start/ Stop switch to Stop.
- In all modules being installed, turn off the drive 2 disconnect circuit breaker (CB230).
- Turn the Power Mode switch on the CE Panel to -3 Local mode during installation.
- Turn off the main line disconnect (CB200).
- Verify with a CE meter that a direct short exists between the irregular size pin (GND) of the power plug or the green and yellow lead of the line cord and the control module frame ground (0.1 ohms or less). Investigate and correct this condition first if this is not the case.
- For 50 Hz machines only, see PWR 92 and verify 6 that the line cord neutral is connected properly on TB203 (YA010).
- Turn on wall receptacle CB and check ac voltage 7 at the receptacle.

#### DANGER Letal Voltage.

If the voltage measured at the wall receptacle agrees 8 with the voltage label located on the frame above the AC Compartment, go to step 9. For 50 Hz machines, see Figure 1.

If the voltage is different:

- For 60 and 50 Hz machines, see Figure 2 for transformer tap wiring changes.
- For 50 Hz machines only, go to PWR 92 for Delta/Wye jumper changes on the terminal boards (TBs) shown in Figure 3.

If a voltage conversion is made, record the change on the voltage label.

- If a 3350 B2 or C2 Module is also being installed, 9 perform the following steps. If not, go to step 12.
- Check that the voltage specified on the voltage \_\_\_\_ 10 label on the frame above the AC Compartment agrees with that specified on the A2 Module. If the voltage is the same, go to Step 11.

If the voltage is different:

- For 60 and 50 Hz machines, see Figure 2 for transformer tap wiring changes.
- For 50 machines only, go to PWR 92 for Delta/ Wye jumper changes on the terminal boards (TBs) shown in Figure 3.

If a voltage conversion is made, record the change on the voltage label.

- If more than one B2 Module is being installed, \_\_ 11 perform Step 10 for each B2 Module.
- **12** After each module being installed has been checked using this procedure, go to **P** on INST 14.

#### Figure 1. 3 Phase Table – 50 Hz

Delta Voltage	Wye Voltage
200 + 10% Line to	380 + 10% to Neutral
220 + 10% (1 inc)	= 220 V
235 + 10% <sup>) Line</sup>	408 + 10% to Neutral
	= 235 V

#### Figure 2. Transformer Primary Tap Wiring

	Voltage		Transformer Taps				
60 Hz	50	Hz	Bootstrap	Controller	Drive Ferro		
	Wye	Wye Delta TB202 (YA011) See Note.		Ferro TB421 (YB/YC026)	TB530 (YB/YB/YC030)		
·	-		A2	A2 and C2	A2, B2, and C2		
200 V		200 V	1 – 2	1 – 2	3 - 4 - 7		
208 V	380 V	220 V	1 – 3	1 – 3	2-4-6		
235 V	408 V	235 V	1 – 4	1 – 4	1 – 4 – 5		

Note: For Japan installations (60 Hz only), change the convenience outlet lead at TB202 if 110 V test equipment is issued (see YA011).

#### Figure 3. (50 Hz Machines Only) Delta/Wye Terminal Boards (TBs)

Module	TB Number									
	TB201 (YA/YB/YC010)	TB211 (YA/YB/YC020)	TB330 (YA/YB/YC010)	TB351 (YA/YB/YC020)	TB361 (YA/YB/YC020)					
A2	*	×	*	×	*					
B2		*	*	**************************************	*					
C2	*	*	*	* <b>*</b>	*					

\*To be checked

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#### INSTALLATION PROCEDURES

#### **INSTALLATION PROCEDURES**

#### **P** POWER CHECKS

If installing a 3350 B2 Module, OMIT Steps 1 and 3. If installing a 3350 C2 Module, OMIT Step 1.

Turn off wall receptacle CB and install power cable. Turn on wall receptacle CB, turn on CB200, place Power Off/Enable switch in the Enable position, and press the controller Power On switch. Assume that power is on when the controller Power On light and the drive Power Sequence Complete (LED) on Sequnce Panel Board B (LOC 4) are on. The Power Check (LED) is also on because CB230 is tripped. If power comes on, go to Step 2.

If power does not come on, phase rotation may be incorrect. K202 is picked if phase rotation is correct. Have customer maintenance personnel check the phase rotation at the wall receptacle. Contact the Branch Office Installation Planning Representative if assistance is needed.

If changing rotation at the wall receptacle is not possible, disconnect power cable from ac outlet. Correct the phasing by reversing any two input leads on the A2 Module, TB 203.

Repeat the beginning of Step 1. If phasing is correct and power does not sequence on, go to START 100, Entry B.

Turn on CB230 in all modules.

Check the controller voltages shown in Figure 1. Use a Digitec 251 Voltmeter<sup>†</sup> (P/N 453585). Set the +6.0 V to + 6 Vdc and -4.0 V to -4.0 Vdc to nominal at installation time. If adjustment is required see PWR 90 or 390, Entry B.

#### Figure 1: Controller Voltages

Supply	Range	Test Point		
		, A2	C2	
+24 Vdc Bootstrap	+ 19.2 V to +30.7 V (Not adjustable)	TB306-1		
-4 Vdc	-3.84 V to -4.16 V (Adjust to 4.0)	A2D2 B06	A2D2 B06	
+6 Vdc	+ 5.76 V to + 6.24 V (Adjust to 6.0)	A2T2 G11	A2T2 G11	
Note: Vol See INST 4	tages are measured with 1.	reference to	W1.	

#### Figure 2: Drive Voltages

DC Supply	Test Point	Tolerance (Volts)		
+24 V Local	CP531 Load Terminal	+ 21.6 to + 26.4 V (Not adjustable)		
-24 V	A1C2D03 (Dr A) A1T2D03 (Dr B)	-24.0 to -28.8 V (Not adjustable)		
+ 12 V	A1C2D05 (Dr A) A1T2D05 (Dr B)	+ 12.0 to + 14.4 V (Not adjustable)		
-12 V	A1C2D06 (Dr A) A1T2D06 (Dr B)	-12.0 to -14.4 V (Not adjustable)		
-4 V	A1C2B06 (Dr A) A1T2B06 (Dr B)	–3.85 to –4.50 V (Not adjustable)		
+6 V Reg	A1F2B11 (Dr A) A1Q2B11 (Dr B)	+ 5.76 to + 6.24 V (Adjust to 6.0)		
-36 V	TB431-4	–36.0 to –43.2 V (Not adjustable)		

Ensure that the Service Bypass switch is in the Off position in all modules being installed (LOC 6).

#### DANGER

Power off the drive before removing or replacing the DC Compartment cover. (Remove cover for adjustment only.)

Check the drive voltages in each drive as shown in Figure 2. Use the Digitec 251 Voltmeter<sup>†</sup> (P/N 453585). The +6.0 Vdc should be set at nominal during installation. If voltage is out of tolerance, see PWR 290.

If powering on problems are encountered, check the symptom list on INST 16 first. If trouble is not corrected, follow the normal maintenance procedure beginning on START 100.

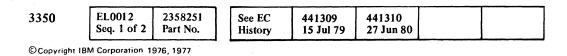
#### POWER ON SEQUENCE AND EPO CHECK Q

- With module power on, set the drive Start/Stop switch to Start.
  - a. Check that the disk rotates counter clockwise as viewed from the top. If the rotation is wrong use PWR 21 or 321 (A2 Module), PWR 121 (B2 Module) or PWR 421 (C2 Module) and ALD's to locate drive phase rotation problem.
  - b. The drive Ready lamp must come on within 30 seconds. If the lamp does not come on, go to START 100.

2 Perform these steps:

- a. Install back panel jumper between: C4D09 (T4D09) and ground to put servo in zero mode.
- b. Check for carriage binding by inserting the bobbin pushrod into the back of the VCM and threading it into the coupler. Move the carriage between the outer and inner stops with the pushrod. If resistance or binding is felt (over 100 grams), use the procedure on HDA 712 to correct the problem. Return here and continue once the trouble is corrected.
- c. Remove the bobbin pushrod and back panel jumper.

#### <sup>†</sup> Trademark of United Systems Corporation



#### INSTALLATION PROCEDURES INST 14

- Press the Attention pushbutton and verify the rezero function. The Ready lamp should go off as long as the Attention pushbutton is pressed.
- Repeat the above steps for each drive.
- Bring all drives to Ready.

9

Power off the subsystem at the storage control (check that controller Power Mode switch on the CE panel is in the Remote position). (LOC 6)

- Power on at the storage control and observe the 7 following:
  - a. Control module power comes on.
  - b. All drives start through the cycle within seconds from each other and should go to Ready.

If powering on problems are encountered, check 8 the symptom list on INST 16 first. If trouble is not corrected, follow the normal maintenance procedure beginning on START 100.

> Install all covers. Adjust hinges and cover latches for alignment, appearance, and ease of operation. The conductive rubber seals must be slightly compressed against the frame when the covers are latched to provide a path for electrostatic discharge. For top cover adjustment, see HDA 770.

#### INSTALLATION PROCEDURES

#### **R** STRING CHECKOUT

1 Make all drives Ready.

2 Use the microdiagnostic facility checkout procedure to check all drives (see MICRO 8). Recommended procedure is to run routine A0 once. Use Checklist below for procedure.

> If problems are encountered, check the symptom list on INST 16 first. If trouble is not corrected, follow the normal maintenance procedure beginning on START 100.

- **3** With String Switch feature, run routine B6 also (see MICRO 70).
- 4 If the Alternate Controller feature is installed, run microdiagnostic routines A1 to BB at least once, using the CE Panel in the C2 Module.

	Checklist for Microdiagnostics										
Drive	Α	В	С	D	Ε	F	G	Η	Remarks		
A0									Run once (See MICRO 20)		
A1-BB									Description (starts on MICRO 20)		
A7					1				See ACC 800, Entry B		
B1									See MICRO 56		
B2		2 2							See MICRO 60		
AB									See MICRO 28		

5 Execute the '30' option (Reset Diagnostic Control). See START 500 for additional information on loading the Fault Symptom Code Generator (3830-2 and ISC only) and on resetting the CE mode latch.

#### S SYSTEM TEST

- 1 Configure OLTEP, OLTSEP, and ST370 to include the 3350 string.
- 2 Check that the CE Mode switch is in the Off position (online). Push all Attention pushbuttons to rezero the HDA.
- **3** Run the following online tests from the CPU on at least one spindle (see OLT section) to check the test programs for proper configuration (PSB, TO 200A, and T3350 WT).
  - Run PSC in default mode on each spindle to build the SD (Skip Displacement) Directory.
  - **Note:** If an SD directory already exists on the HDA it is not necessary to rewrite the directory.
  - If PSC is not run because an SD directory already exists PSA must be run.

If the compatibility mode jumper was changed to run PSC, restore the jumper to customer configuration. See Figure 1 on HDA 711.

Misleading errors can occur if two control modules on the same channel have the same address. Refer to INST 6, Item N for proper plugging.

Ensure that the EPO cable is installed. Do not leave the shorting plug installed.

#### T RECORDS

1 Assist the customer with his checkout of each string.

- 2 Complete all installation records and report that the installation is complete to the Branch Office dispatcher. See Figure 1 for Installation Activity Document (IAD) codes.

**Note:** Machine serial tag is located on the lower frame member left front.

- 3 Insert these installation procedures in the Maintenance Information Manual for future reference.
- 4 Update the Account Management Plan book to include this installation.
- 5 If the String Switch feature is installed, a decal (P/N 2745548) is located on the A2 Module frame member below the CE Panel. Complete the information required on the decal to indicate the cabling route. Repeat this procedure at the C2 Module, if installed.

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#### Figure 1: Installation Activity Document Codes

# 3350 & 3830

		SITE READINESS/PROBLEMS	
1 1	0 5	<ul> <li>power/air cond.</li> <li>other - explain</li> </ul>	
		SHIPPING DAMAGES/PROBLEMS	
1 1	6 7	<ul> <li>(If S/C 39 is written on a regular IR; record activity code and 0 actual hrs. on IAD)</li> <li>bent covers, broken hardware, paint</li> <li>late arrival of cables and/or units</li> </ul>	
		FEATURES	
2 2	3 7	wrong, missing or extra features — machine does not match factory order – other - explain	
		DOCUMENTATION	
2	8	<ul> <li>incorrect or misleading - explain (PDP's, MAPS, installation instructions)</li> </ul>	
2	9	<ul> <li>missing - explain (e.g. parts catalog, MAPS, etc.)</li> </ul>	
3 3 3	4 5 9	INSTALLATION ACTIVITY	
Ū	0	TECHNICAL PROBLEMS/DEFECTS	
4	0	- voice coil, VCM, 5 5 - operator panel	
		hycraulic actuator 5 6 – brake assembly	
4	1	<ul> <li>drawer assembly</li> <li>5</li> <li>7</li> <li>pulley/belt</li> </ul>	
4	2	<ul> <li>disk brush unit</li> <li>6</li> <li>1</li> <li>sequence/distribution</li> </ul>	
4	3	– disk pack/data (power)	
		module/HDA 6 3 – AC compartment	
4	4	<ul> <li>spindle assembly</li> <li>6</li> <li>4</li> <li>power supply DC</li> </ul>	
4	5	– carriage 6 5 – cables, contact, CB,	
4	6	– heads relay	
4	7	- retract mech/DM 6 7 - logic board	
	-	load mech 6 9 - card-replaced/adjusted	
4	8	<ul> <li>bobbin/head load</li> <li>7 0 - signal cable</li> </ul>	
		linkage 7 3 - cable-RW/PLO/matrix	
4	9	- photo cell/transducer 7 4 - power amp	
5	0	- base/cooling/filters/ 7 6 - CE panel	
-		covers 8 0 – diskette drive	
5	1	- motor/drive 8 8 - diagnostics will not	
5	2	- wiring error run - explain	
5	3	- wrong EC level/ 8 9 - microcode	
_		part number 9 0 - other - (general technical	)
5	4	- air flow system	

#### INSTALLATION PROCEDURES

## **INSTALLATION PROCEDURES**

#### **INSTALLATION PROBLEMS**

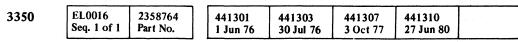
Use the Symptom Checklist to assist in isolating installation type problems. Do not spend a great deal of time. If a pass through the symptom list does not result in a fix, go to START 100 and follow the established maintenance procedure in the MIM.

The following is a list of general hints. Use it when problems are encountered during installation that do not have obvious symptoms:

- 1. Check interframe connector cables and terminators. See INST 5 and DEV-I 90 or DEV-I 100.
- 2. Check controller and drive addressing. See INST 6.
- 3. Check cables between controller (3350 A2/C2) and storage control. Verify cables are not reversed. See INST 3.
- 4. Check all voltages. Procedures are on PWR 90 (PWR 290). For 50 Hz, motor conversions are on PWR 92.
- 5. Verify that the correct Functional Microprogram disk is loaded in storage control, ISC, or IFA.
- 6. Verify that the correct Microdiagnostic disk is loaded in storage control, ISC, or IFA.
- 7. If the String Switch feature is installed, verify that both A and B Enable/Disable switches are in the Enable position.
- 8. Check Addressing cards, (A2G2; with String Switch feature, A2D2 and A2E2). Verify that Address Compare, Primary/ Alternate Controller, and Controller Addresses are plugged properly (see INST 7). See also the 3830-2/ISC Installation for address plugging.
- 9. Return to normal established maintenance procedures in the MIM. Go to START 100.

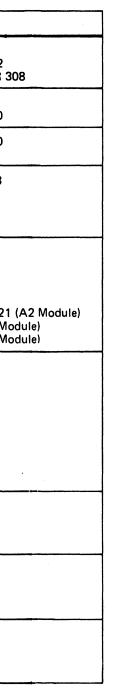
#### SYMPTOM CHECKLIST FOR INSTALLATION PROBLEMS

Failure	Symptom	Recommended Action	Reference
Power Sequence	Power sequences on but drive motors do not start.	Check that jumpers are between T1 and T2, and T3 and T4 in the last module only.	INST 3, E 2 YA/YB/YC052 PWR 8 or PWR 3
	Some drives power on, others do not.	Check that the ac power cable is plugged into P304 and properly seated.	INST 3, G 1 YA/YB/YC010
	Drive motors turn slowly.	Check that a pin is not pushed back into P304.	YA/YB/YC010
Ready Lamp not on	Drive never comes Ready. Drive motor starts and then stops.	1. Check that Mode jumper is installed correctly.	INST 4, 🖪 3
		2. Check for proper seating of Mode cable.	KF110, 120 (KQ110,120)
	Drive never comes Ready, but drive motor runs.	1. Check servo adjustment. Go to ACC 800, Entry A.	INST 14, O
		<ol> <li>Check for other servo problems or a missing voltage.</li> </ol>	PWR 290
		3. Check that disk rotates counter clockwise as viewed from the top. If not check drive phase rotation.	PWR 21 and 321 PWR 121 (B2 M PWR 421 (C2 M
Microdiagnostics	Microdiagnostics will not load. Execute Request LED on	Ensure that one of the following is not the failure:	INST 3, <b>F</b> ZA090
	continuously.	<ol> <li>Control Interface cables swapped; Bus In to Tag In connector.</li> </ol>	
		2. Wrong terminator is used.	
		3. The Switch Unit (for example, IBM 2914) not set up correctly.	
		4. Control Interface cables loose.	
	Microdiagnostic Error Codes: A158 A211 A220	Ensure correct plugging at the inter- frame connector.	INST 5, J DEV-I 100
	Microdiagnostics run slowly with the Alternate Controller only.	Ensure that card A2G2 (A2D2 and A2E2 with String Switch feature) is not wired for Primary Controller but installed in the C2 Module.	INST 6 6
Fault Symptom Code	Fault Symptom Code 9120.	Ensure that cards A1K2 and A1L2 are not wired with the same address (no two cards in a string can have the same address).	INST 6 M



#### INSTALLATION PROCEDURES

#### INST 16



#### INSTALLATION PROCEDURES INST 16

