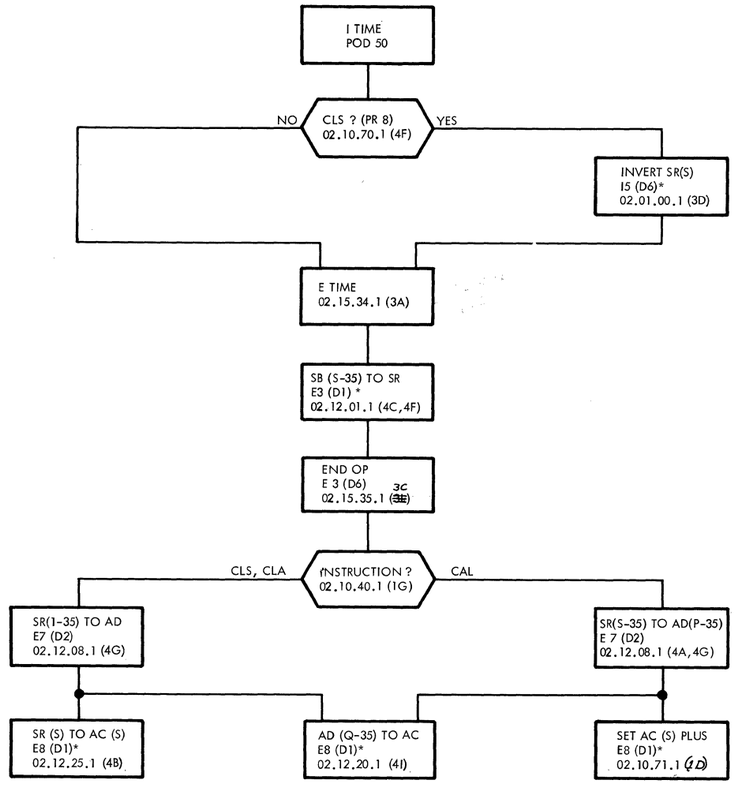
Contents by logic group on next page.

INDEX

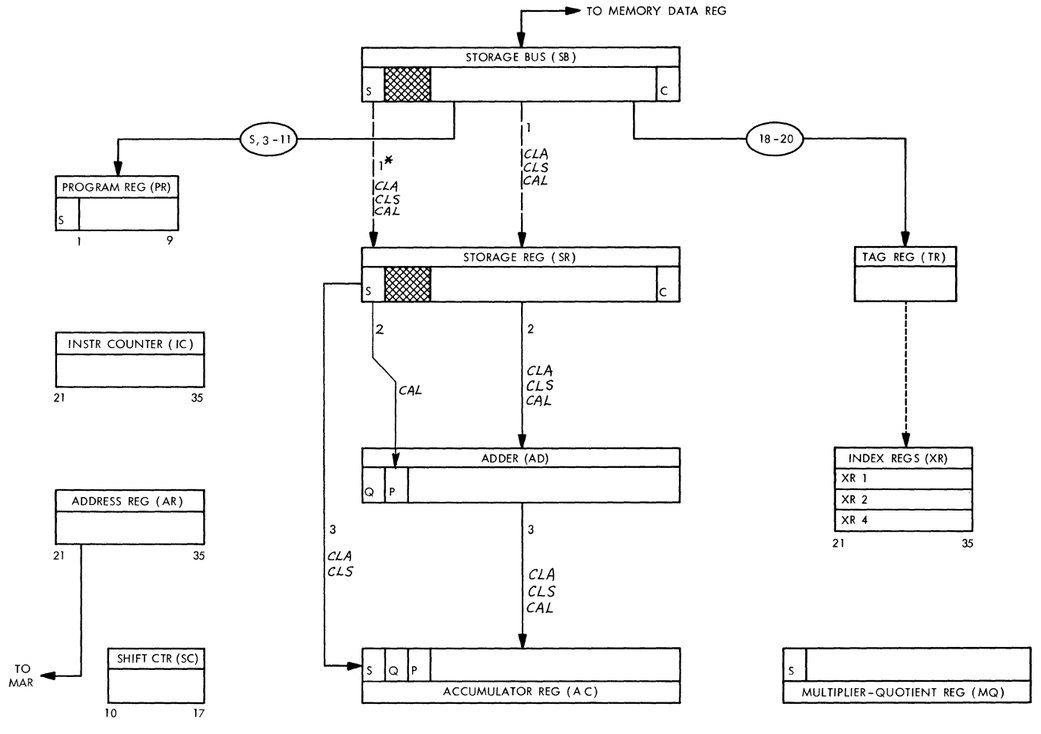
Clear and Add (CLA +0500)
Replaces the contents of the accumulator (S, 1-35) with the contents of the effective address. Bit positions P and Q of the accumulator are set to 0. The contents of memory are unchanged.

Clear and Subtract (CLS +0502)
Replaces the contents of the accumulator (S, 1-35) with the negative of the contents of the effective address. P and Q of the accumulator are set to 0. The contents of memory are unchanged.

Clear and Add Logical Word (CAL -0500)
Replaces the contents of the accumulator (P, 1-35) with the contents of the effective address. The sign of the memory word goes to bit P of the accumulator. Bits S and Q of the accumulator are set to 0's. The contents of memory are unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.



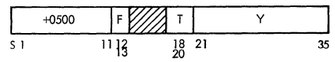
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0500 CLEAR AND ADD

ALPHA CODE: CLA CYCLES: I, E



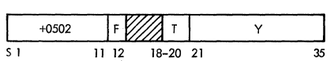
SEQUENCE NOTES:

THE C(AC) S,1-35 ARE REPLACED WITH C(Y). POSITIONS P AND Q OF AC ARE SET TO ZERO.

C(Y) ARE UNCHANGED.

INST +0502 CLEAR AND SUBTRACT

ALPHA CODE: CLS CYCLES: I, E



SEQUENCE NOTES:

THE NEG OF C(Y) REPLACES THE C(AC)S, 1-35.

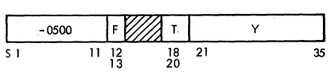
POSITIONS P AND Q OF THE AC ARE SET TO ZERO.

THE C(Y) ARE UNCHANGED.

*SB($\overline{S}$) ⟶ SR(S)

INST -0500 CLEAR AND ADD LOGICAL WORD

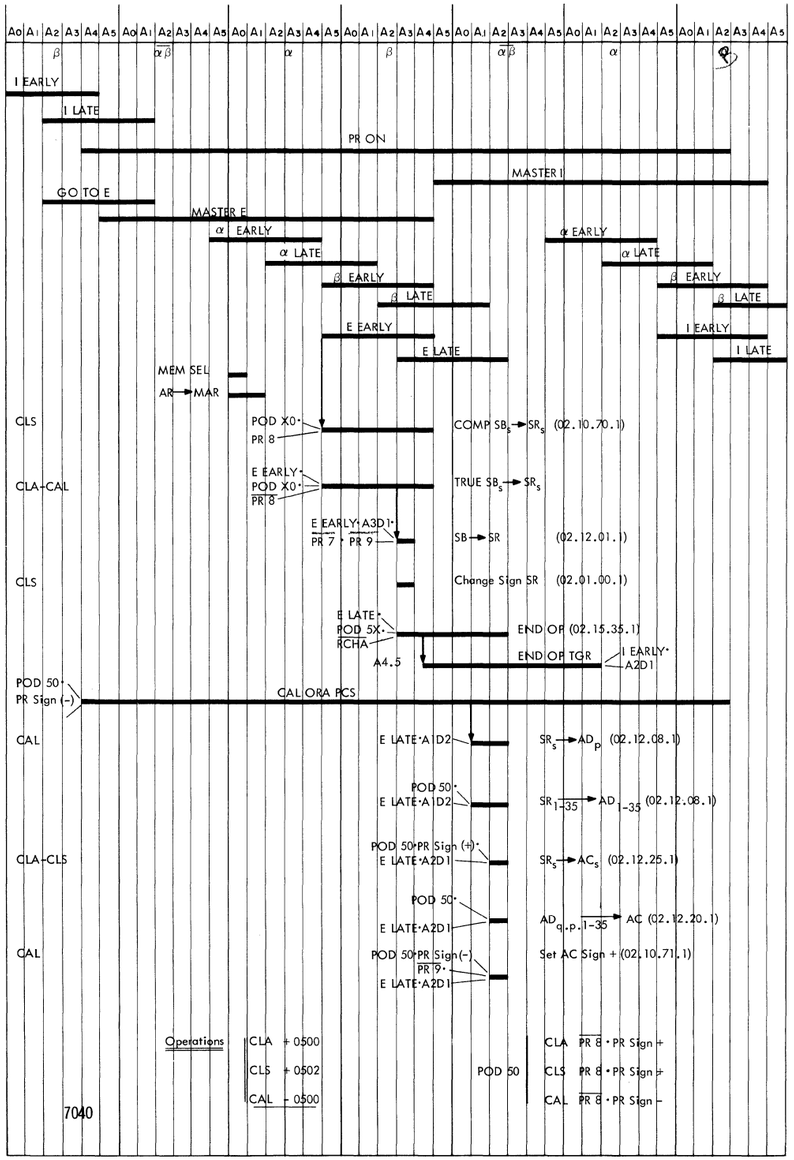
ALPHA CODE: CAL CYCLES: I, E



SEQUENCE NOTES:

THE C(Y) REPLACE THE C(AC)$_{P,1-35}$. THE SIGN OF Y APPEARS IN POSITION P OF THE AC. POSITIONS S AND Q ARE SET TO ZEROS. C(Y) ARE UNCHANGED.

FIGURE 1. CLA, CLS, CAL



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	CLA		00006	050000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			777777 777777
00006	Pattern			000000 000000

Clear and Add (CLA)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00005	050000000005	000000000000	00		
E	I	00001	+500	000	0	00001	777777777777	777777777777	00		
I	E	00002	+500	000	0	00006	050000000006	777777777777	00		
E	I	00002	+500	000	0	00002	000000000000	000000000000	00		
I	I	00003	+020	000	0	00000	002000000000	000000000000	00		

Location Switches	Inst	Tag	Address	Octal Equiv.
00000	CLS		00005	050200 000005
00001	CLS		00006	050200 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			777777 777777
00006	Pattern			000000 000000

Clear and Subtract (CLS)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+502	000	0	00005	050200000005	000000000000	00		
E	I	00001	+502	000	0	00001	377777777777	377777777777	00		
I	E	00002	+502	000	0	00006	050200000006	377777777777	00		
E	I	00002	+502	000	0	00002	400000000000	400000000000	00		
I	I	00003	+020	000	0	00000	002000000000	400000000000	00		
I	E	00001	+502	000	0	00005	050200000005	400000000000	00		

Location Switches	Inst	Tag	Address	Octal Equiv.
00000	CAL		00005	450000 000005
00001	CAL		00006	450000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			070707 070707
00006	Pattern			707070 707070

Clear and Add Logical Word (CAL)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	-500	000	0	00005	450000000005	000000000000	00		
E	I	00001	-500	000	0	00001	070707070707	070707070707	00		
I	E	00002	-500	000	0	00006	450000000006	070707070707	00		
E	I	00002	-500	000	0	00002	707070707070	307070707070	01		
I	I	00003	+020	000	0	00000	002000000000	307070707070	01		
I	E	00001	-500	000	0	00005	450000000005	307070707070	01		

Clear and Add Logical Word with Parity (CAP -1510)
Replaces the contents of bits S, P, 1-35 of the accumulator with bits C, S, 1-35 of the effective address. The sign of the memory location and the parity bit go to bits P and S, respectively, of the accumulator. Accumulator Q is reset to 0. The contents of the effective address are not checked for parity and do not cause a parity trap request. The contents of memory are unchanged.

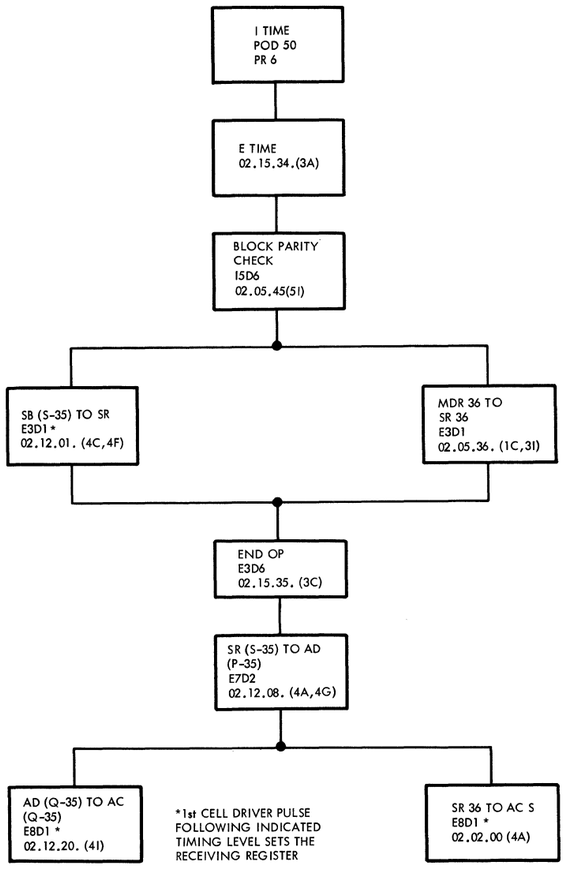
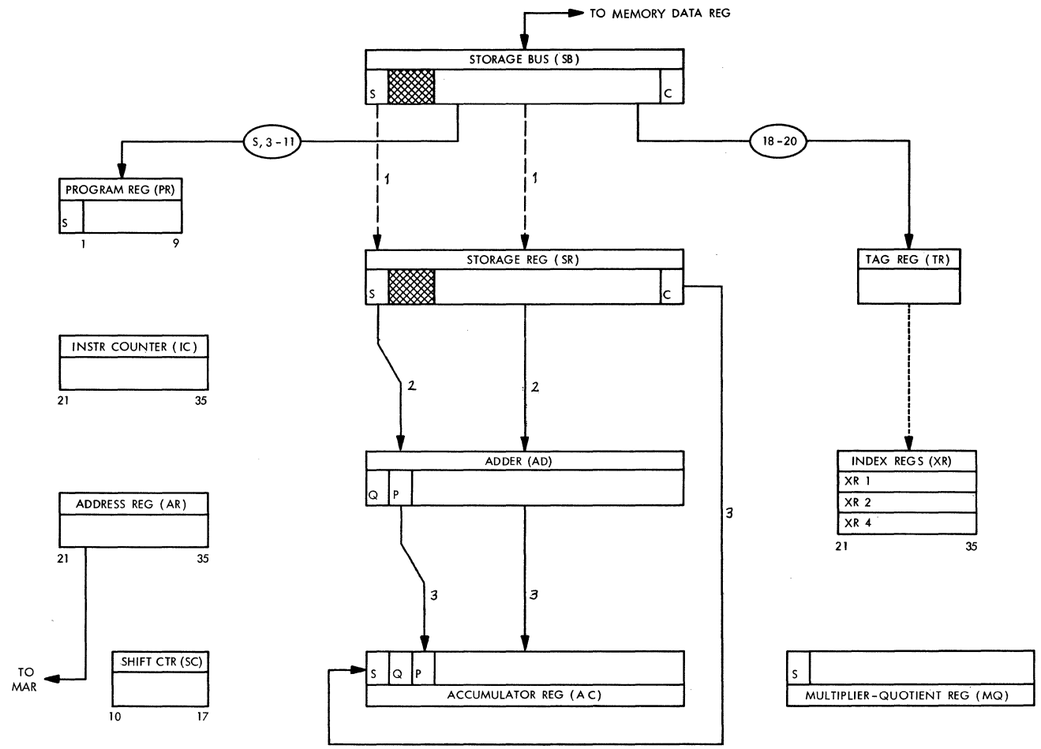


FIGURE 2. CAP



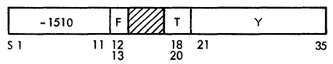
LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

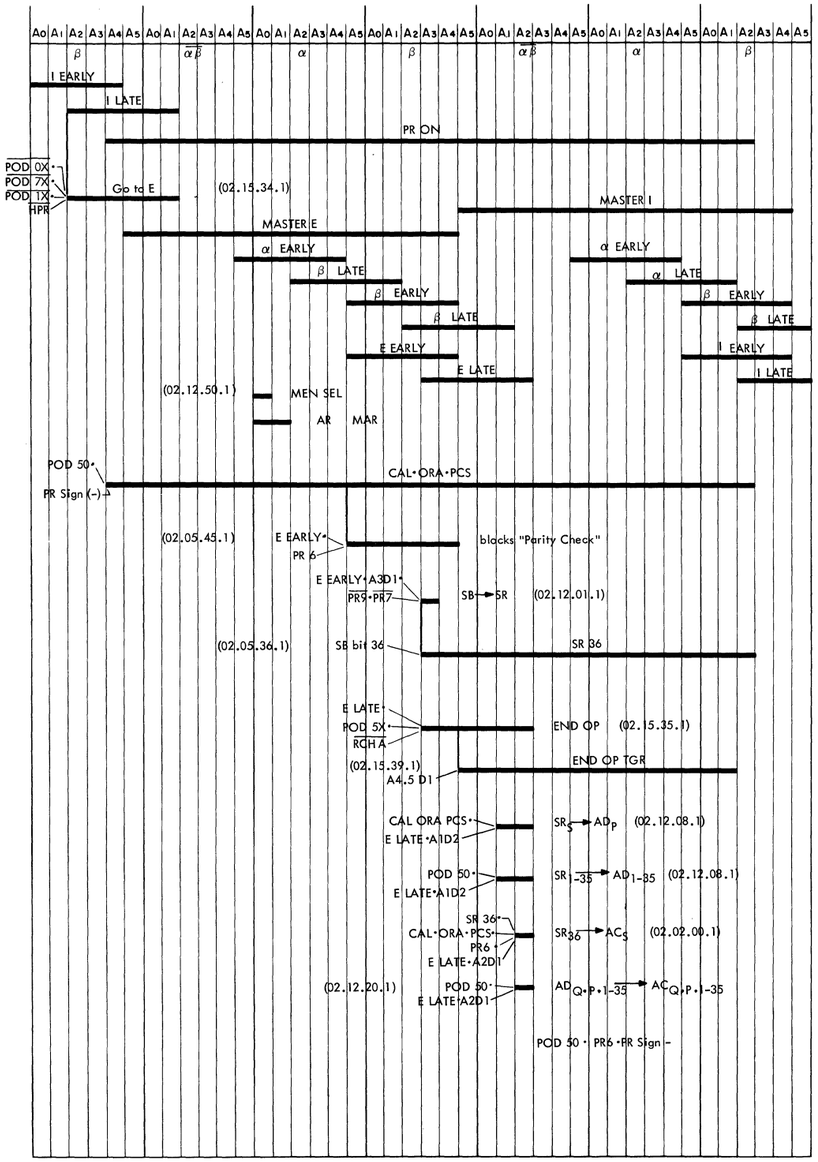
INST CLEAR AND ADD LOGICAL WORD WITH PARITY

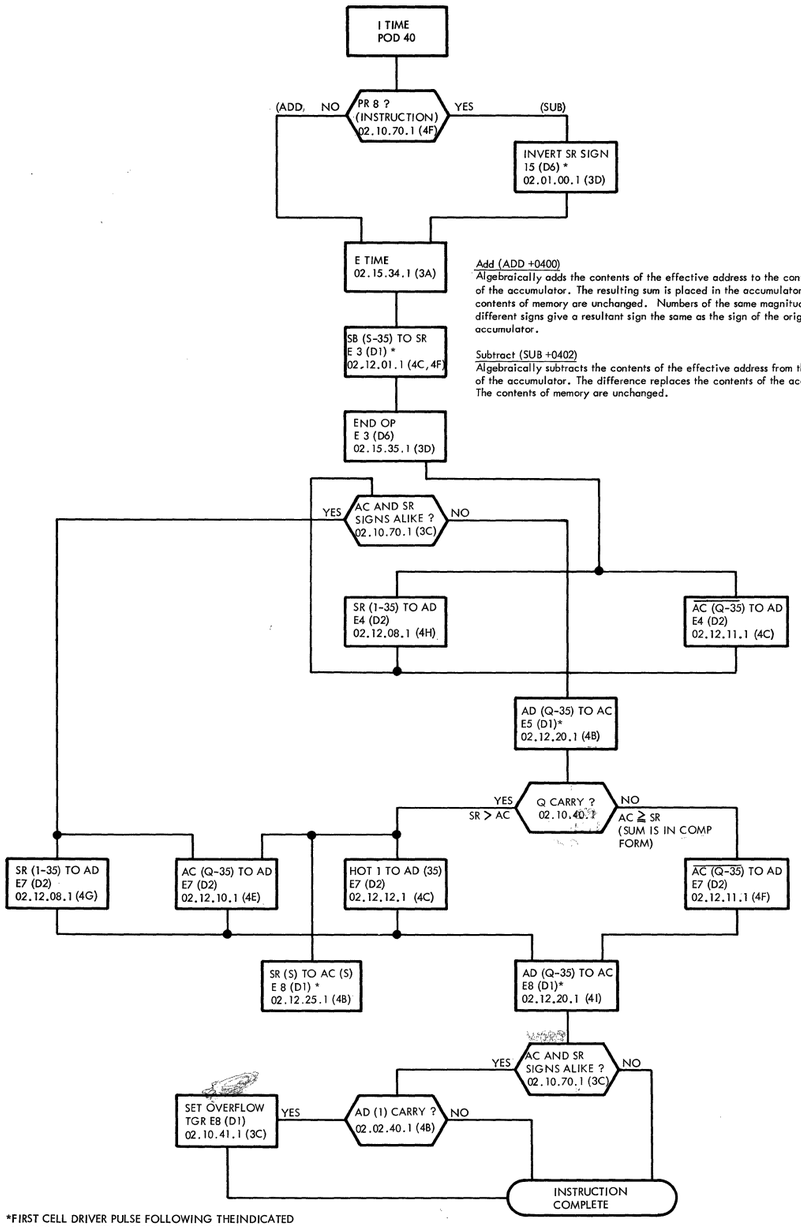
ALPHA CODE: CAP CYCLES: I, E



SEQUENCE NOTES:

THE $C(Y)_{C,S,1-35}$ REPLACE THE $C(AC)_{S,P,1-35}$. THE PARITY BIT OF LOC Y REPLACES S OF THE AC. AC(Q) IS SET TO A ZERO.


A0 A1 A2 A3 A4 A5
β
αβ
α
I EARLY
I LATE
PR ON
POD 0X
POD 7X
POD 1X
HPR
Go to E
(02.15.34.1)
MASTER I
MASTER E
α EARLY
β LATE
β EARLY
E EARLY
E LATE
I EARLY
I LATE
(02.12.50.1)
MEN SEL
AR MAR
POD 50
PR Sign (-)
CAL·ORA·PCS
(02.05.45.1)
E EARLY·PR 6
blocks "Parity Check"
E EARLY·A3D1·PR9·PR7
SB → SR
(02.12.01.1)
(02.05.36.1)
SB bit 36
SR 36
E LATE·POD 5X·RCH A
END OP
(02.15.35.1)
END OP TGR
(02.15.39.1) A4.5 D1
CAL ORA PCS·E LATE·A1D2
SR_S → AD_P
(02.12.08.1)
POD 50·E LATE·A1D2
SR_1-35 → AD_1-35
(02.12.08.1)
SR 36·CAL·ORA·PCS·PR6·E LATE·A2D1
SR_36 → AC_S
(02.02.00.1)
(02.12.20.1)
POD 50·E LATE·A2D1
AD_Q·P·1-35 → AC_Q·P·1-35
POD 50 · PR6 · PR Sign -

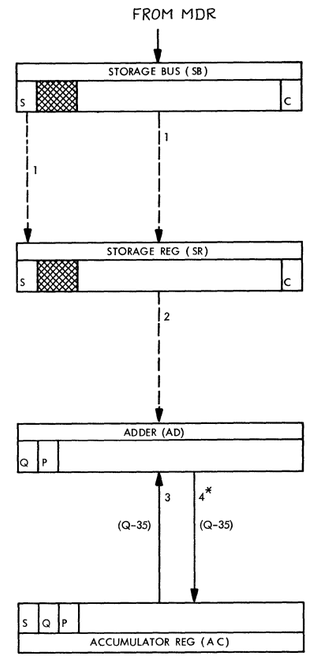


*FIRST CELL DRIVER PULSE FOLLOWING THEINDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

FIGURE 3. ADD, SUB

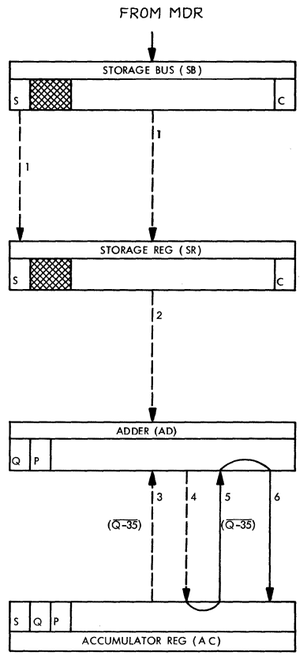
Add (ADD +0400)
Algebraically adds the contents of the effective address to the contents of the accumulator. The resulting sum is placed in the accumulator. The contents of memory are unchanged. Numbers of the same magnitude but different signs give a resultant sign the same as the sign of the original accumulator.

Subtract (SUB +0402)
Algebraically subtracts the contents of the effective address from the contents of the accumulator. The difference replaces the contents of the accumulator. The contents of memory are unchanged.

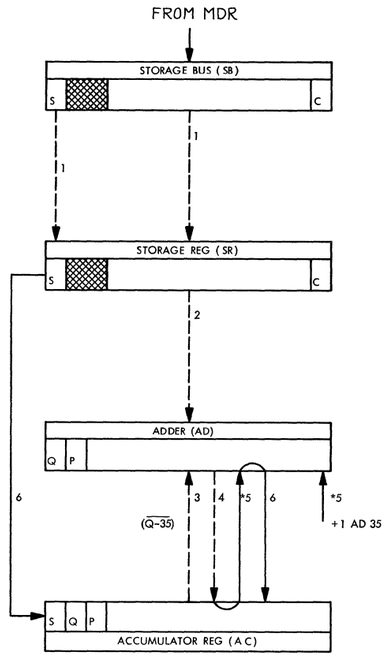


LIKE SIGNS

*4 AC OVFL TGR SET IF CARRY INTO P ON ADD, LIKE SIGNS



UNLIKE SIGNS, AC ≧ SR

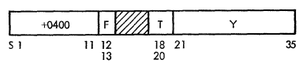


UNLIKE SIGNS, SR > AC

*5. $C(AC)_{Q-35}$ AND HOT 1 TO ADDER (CI 35)

INST +0400 ADD

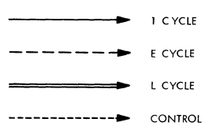
ALPHA CODE: ADD CYCLES: I, E



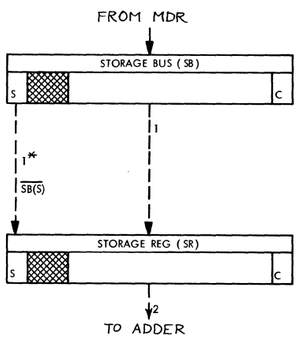
SEQUENCE NOTES:

THE C(Y) ARE ALGEBRAICALLY ADDED TO C(AC). THE RESULTING SUM IS PLACED IN THE AC. C(Y) ARE UNCHANGED. NUMBERS OF THE SAME MAGNITUDE BUT DIFFERENT SIGNS GIVE RESULTANT SIGN OF THE ORIGINAL AC.

LEGEND

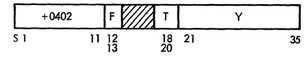


XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



INST +0402 SUBTRACT

ALPHA CODE: SUB CYCLES: I, E

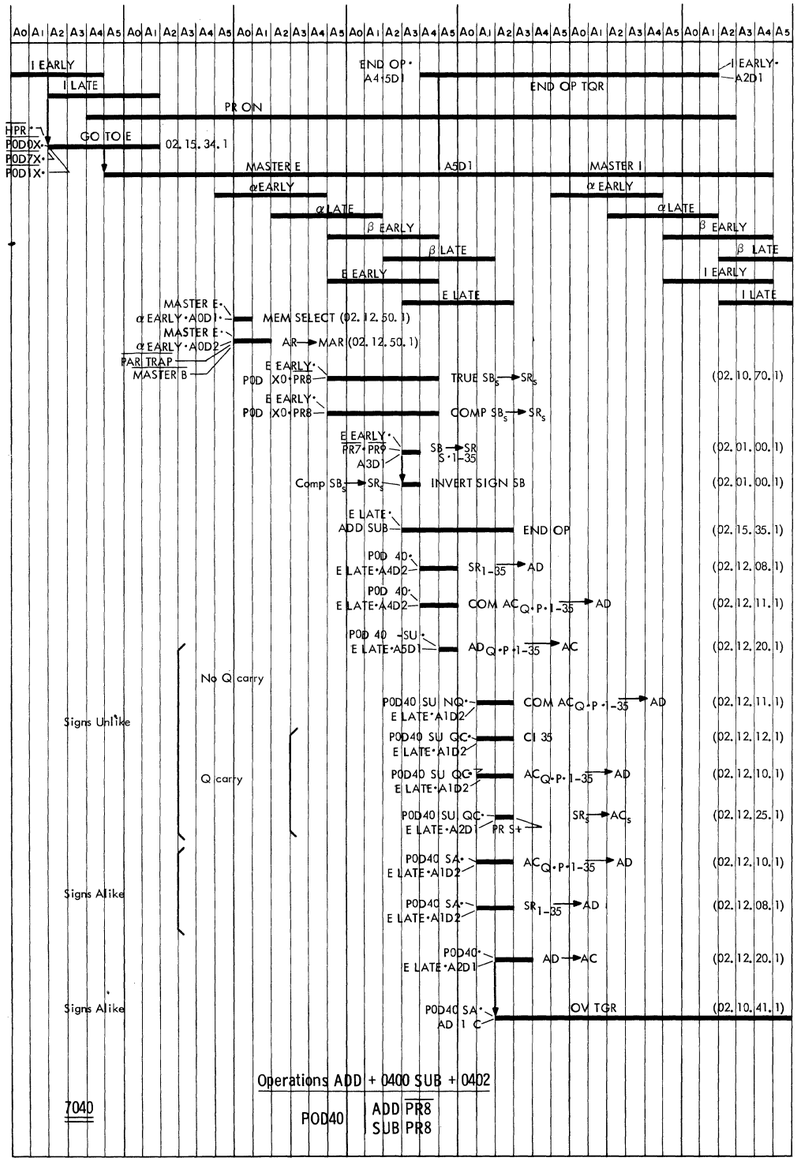


SEQUENCE NOTES:

*1 $C(\overline{SB})S \longrightarrow SR_S$.

REMAINDER OF SUB INSTRUCTION IS THE SAME AS "ADD".

OVERFLOW POSSIBLE WHEN SUBTRACTING VALUES WITH UNLIKE SIGNS.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	ADD		00006	040000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			000000 000001
00006	Pattern			377777 777777

Add (ADD)

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
CONSOLE INDICATORS																					
I	E	00001	+500	000	0	00005	050000000005	000000000000	00												
E	I	00001	+500	000	0	00001	000000000001	000000000001	00												
I	E	00002	+400	000	0	00006	040000000006	000000000001	00												
E	I	00002	+400	000	0	00002	377777777777	000000000000	01				1		1		1				
I	I	00003	+020	000	0	00000	002000000000	000000000000	01				1		0		0				
I	E	00001	+500	000	0	00005	050000000005	000000000000	01				1								
E	I	00001	+500	000	0	00001	000000000001	000000000000	00				1								
I	E	00002	+400	000	0	00006	040000000006	000000000000	00				1								

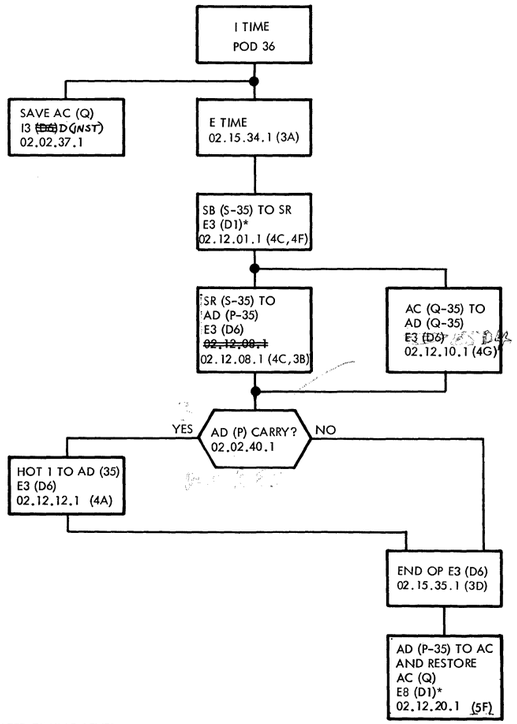
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	SUB		00006	040200 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			000000 000001
00006	Pattern			377777 777777

Subtract (SUB)

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
CONSOLE INDICATORS																					
I	E	00001	+500	000	0	00005	050000000005	000000000000	00												
E	I	00001	+500	000	0	00001	000000000001	000000000001	00												
I	E	00002	+402	000	0	00006	040200000006	000000000001	00												
E	I	00002	+402	000	0	00002	777777777777	777777777776	00						1		1				
I	I	00003	+020	000	0	00000	002000000000	777777777776	00						0		0				
I	E	00001	+500	000	0	00005	050000000005	777777777776	00						0		0				

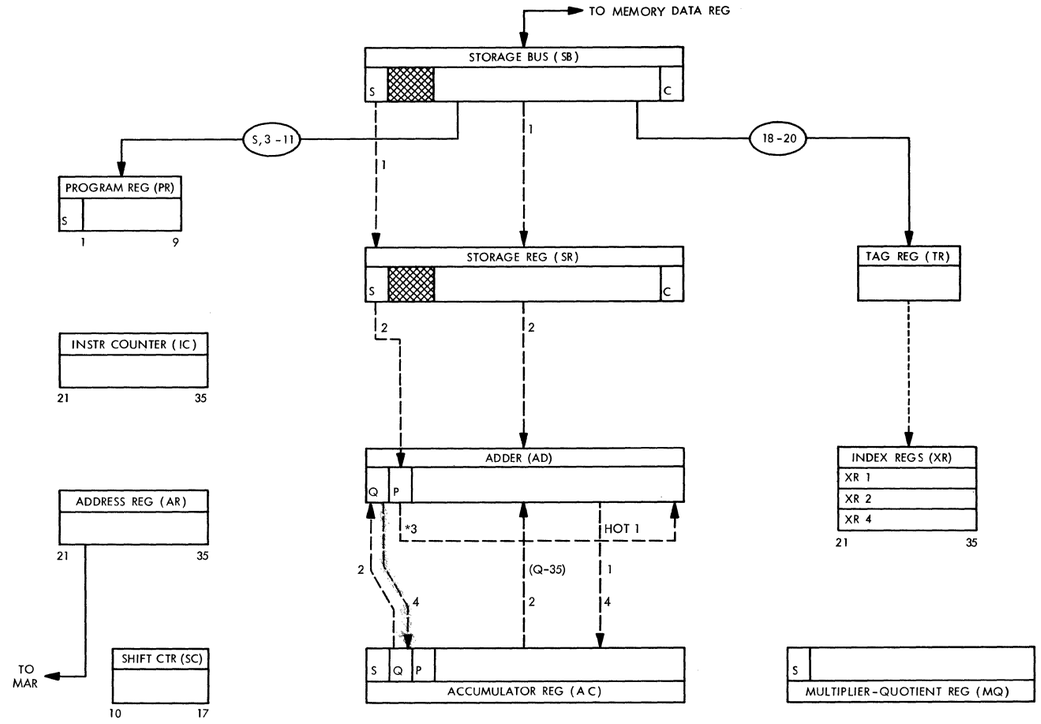
Add and Carry Logical Word (ACL +0361)

Adds the contents of the memory location (S, 1–35) to the contents of the accumulator (P, 1–35). The resultant sum replaces the contents of the accumulator (P, 1–35). The sign bit of the memory word is added to accumulator P bit; a carry out of P is added back to accumulator 35. Accumulator S and Q are not affected.



* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

FIGURE 4. ACL



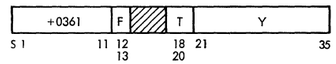
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0361 ADD AND CARRY LOGICAL WORD

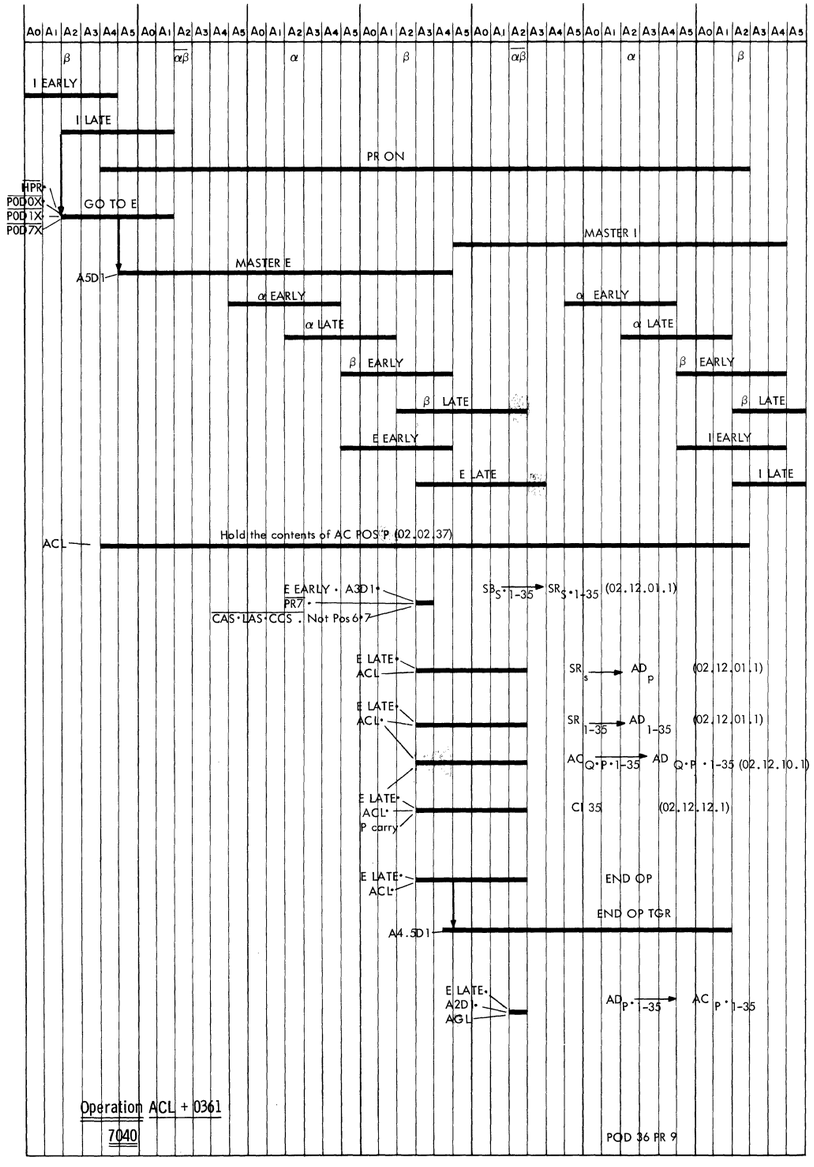
ALPHA CODE: ACL CYCLES: I, E



SEQUENCE NOTES:

THE C(Y) ARE ADDED TO THE $C(AC)_{P, 1-35}$. THE RESULTANT SUM REPLACES THE $C(AC)_{P, 1-35}$. THE SIGN OF Y IS ADDED TO POSITION P OF THE AC. A CARRY FROM AC(P) IS ADDED TO AD(35). POS S AND Q OF AC ARE NOT AFFECTED. C(Y) ARE UNCHANGED.

*3 P CARRY ⟶ CI 35.

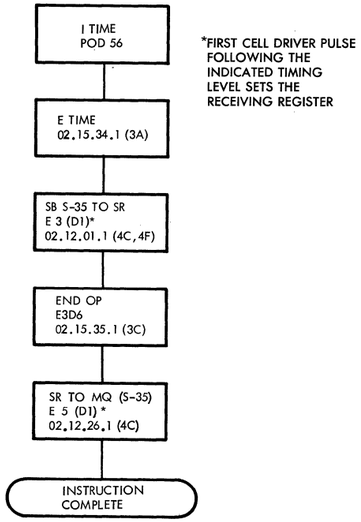


Location Switches	Inst	Tag	Address	Octal Equiv.
00000	CAL		00005	450000 000005
00001	ACL		00006	036100 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			525252 525252
00006	Pattern			252525 252525

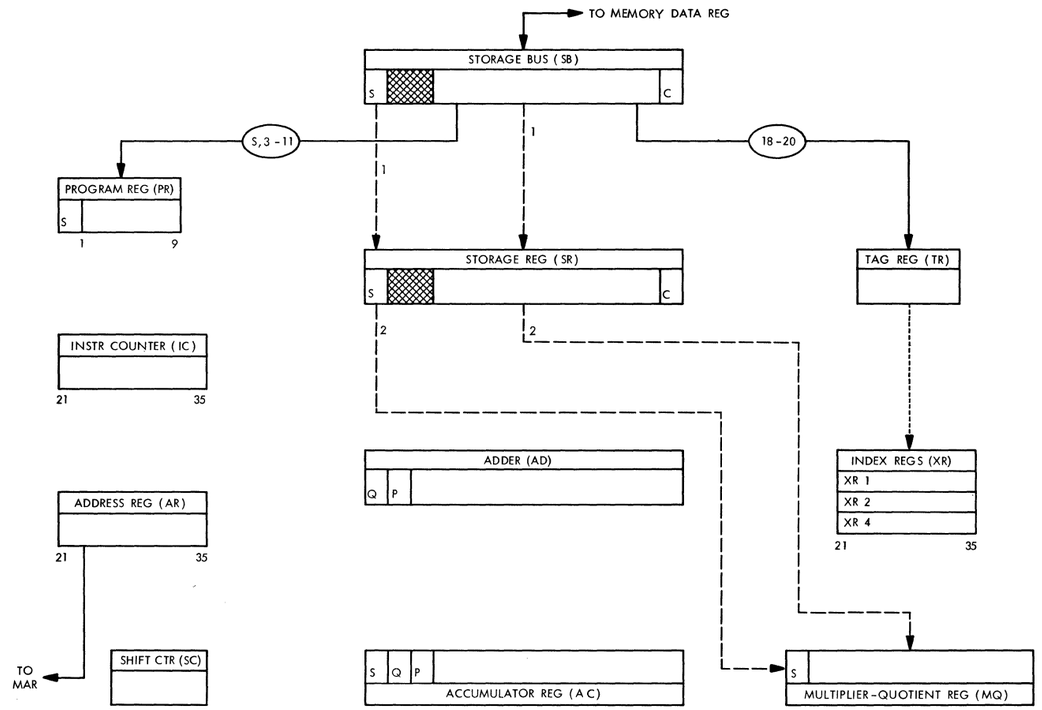
Add and Carry Logical Word (ACL)

CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCUM. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	-500	000	0	00005	450000000005	000000000000	00												
E	I	00001	-500	000	0	00001	525252525252	125252525252	01												
I	E	00002	+361	000	0	00006	036100000006	125252525252	01												
E	I	00002	+361	000	0	00002	252525252525	377777777777	01												
I	I	00003	+020	000	0	00000	002000000000	377777777777	01												
I	E	00001	-500	000	0	00005	450000000005	377777777777	01												

Load MQ (LDQ +0560)
The contents of the specified memory location to the MQ register (S,1-35).
The contents of memory are unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



LEGEND

1 CYCLE

E CYCLE

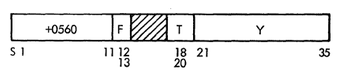
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0560 LOAD MQ

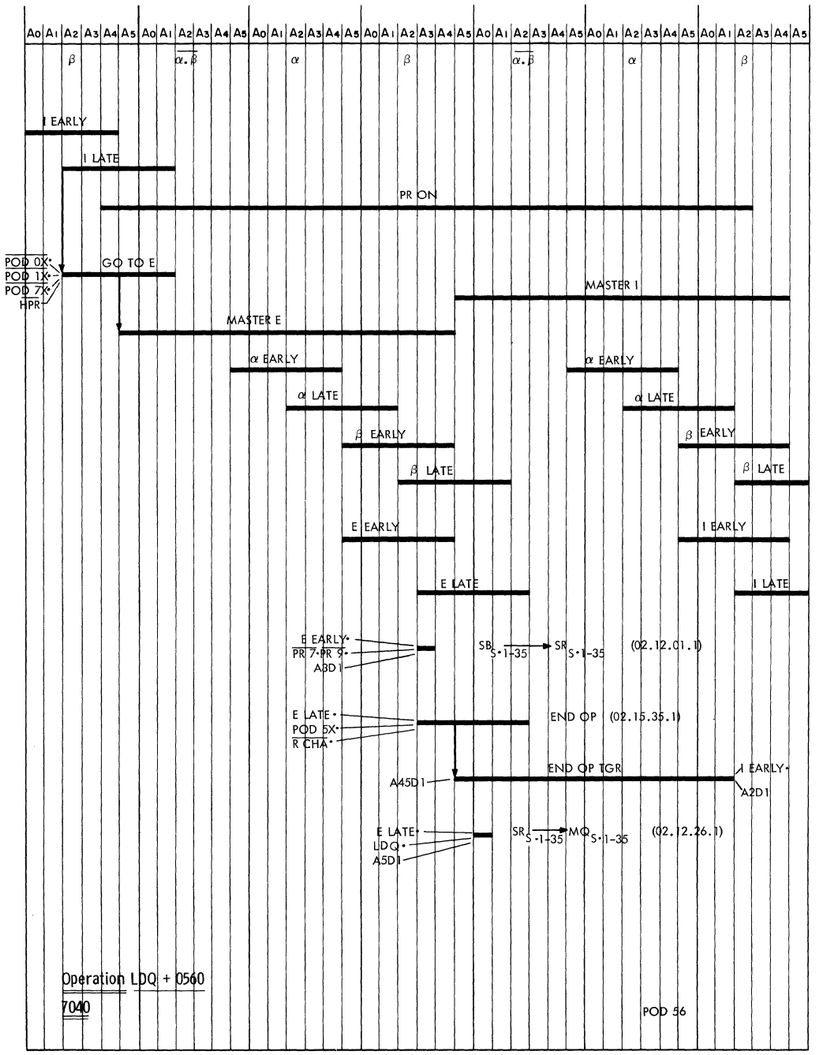
ALPHA CODE: LDQ CYCLES: I, E



SEQUENCE NOTES:

THE C(Y) IS LOADED INTO THE MQ. THE C(Y) ARE UNCHANGED.

FIGURE 5. LDQ



Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00005	056000 000005
00001	LDQ		00006	056000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			777777 777777
00006	Pattern			000000 000000

Load MQ (LDQ)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+560	000	0	00005	056000000005			000000000000											
E	I	00001	+560	000	0	00001	777777777777			777777777777											
I	E	00002	+560	000	0	00006	056000000006			777777777777											
E	I	00002	+560	000	0	00002	000000000000			000000000000											
I	I	00003	+020	000	0	00000	002000000000			000000000000											

Enter Keys (ENK +0760...0004)
Places the contents of the console word bank keys into the MQ register.
Address modification may change the operation.

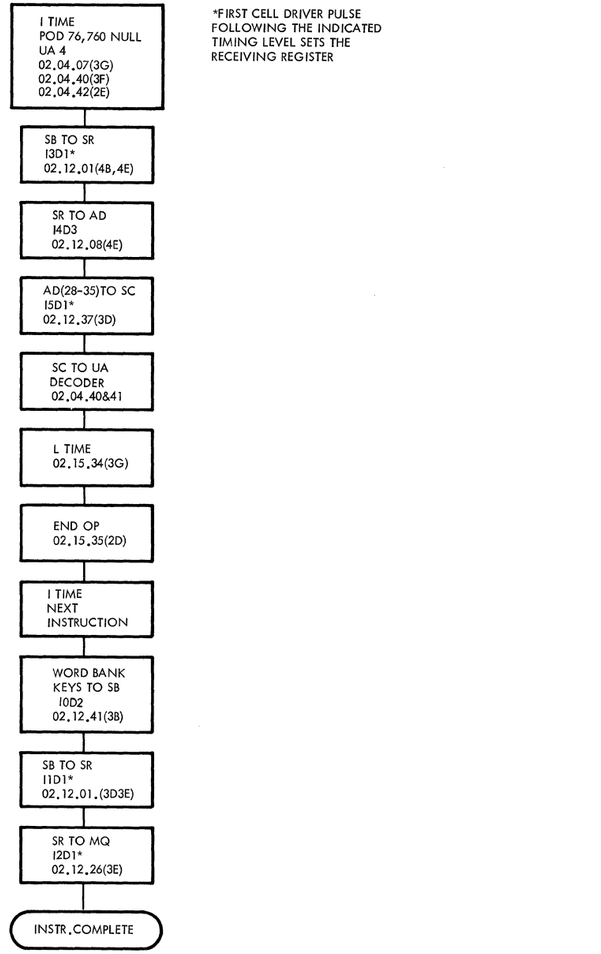
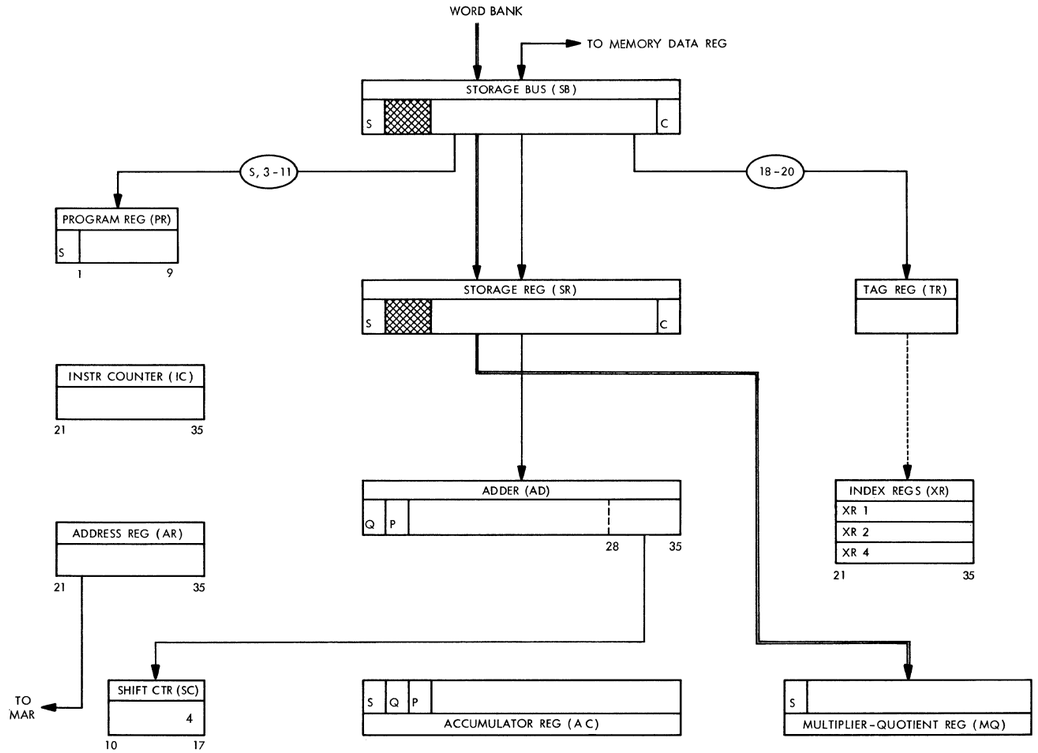


FIGURE 6. ENK



LEGEND

1 CYCLE

E CYCLE

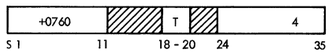
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

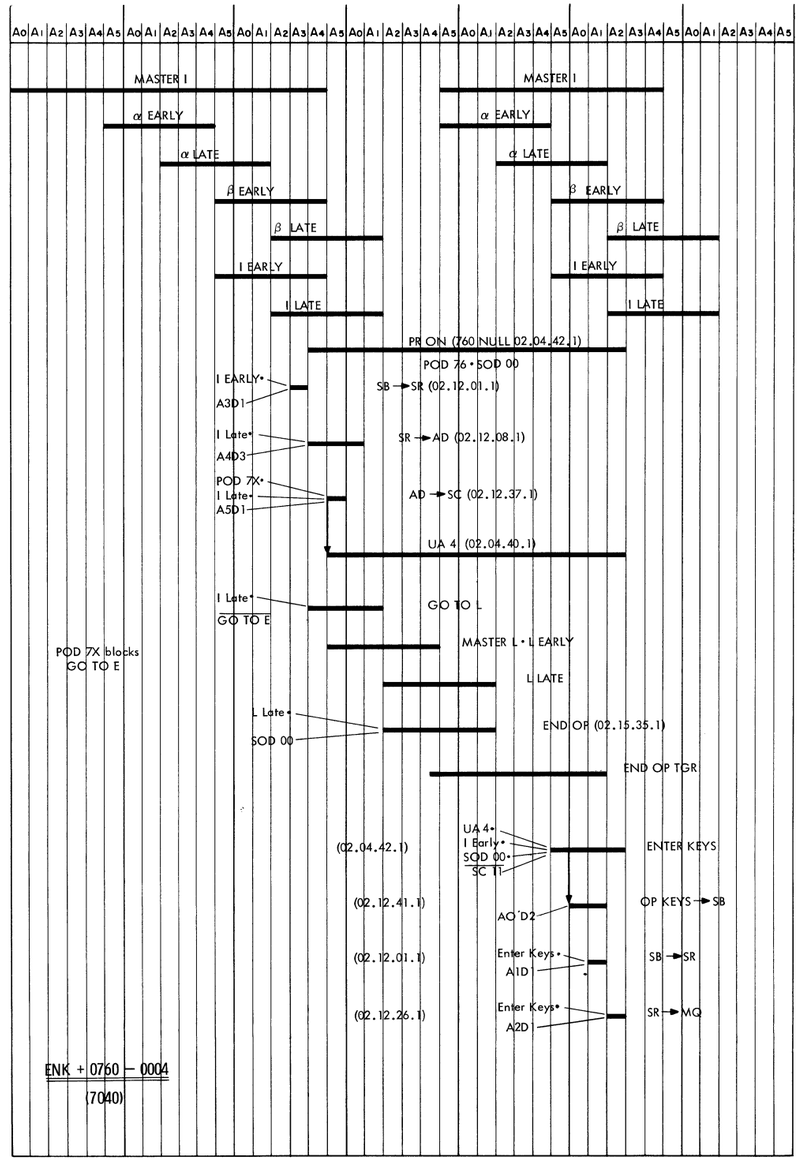
INST ENTER KEYS

ALPHA CODE: ENK CYCLES: I, L



SEQUENCE NOTES:

THE C(WORD BANK) IS PLACED IN THE C(MQ). ADDRESS MODIFICATION MAY CHANGE THE INSTRUCTION ITSELF.



* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

** THIS BLOCK IS INTERROGATED WITH CONSECUTIVE CELL DRIVER OUTPUT PULSES BEGINNING WITH THE PULSE THAT GENERATES THE FIRST L3 LEVEL. ONE PULSE WILL PERFORM ALL OF THE POSSIBLE OPERATIONS UNDER THE "NO" LINE.

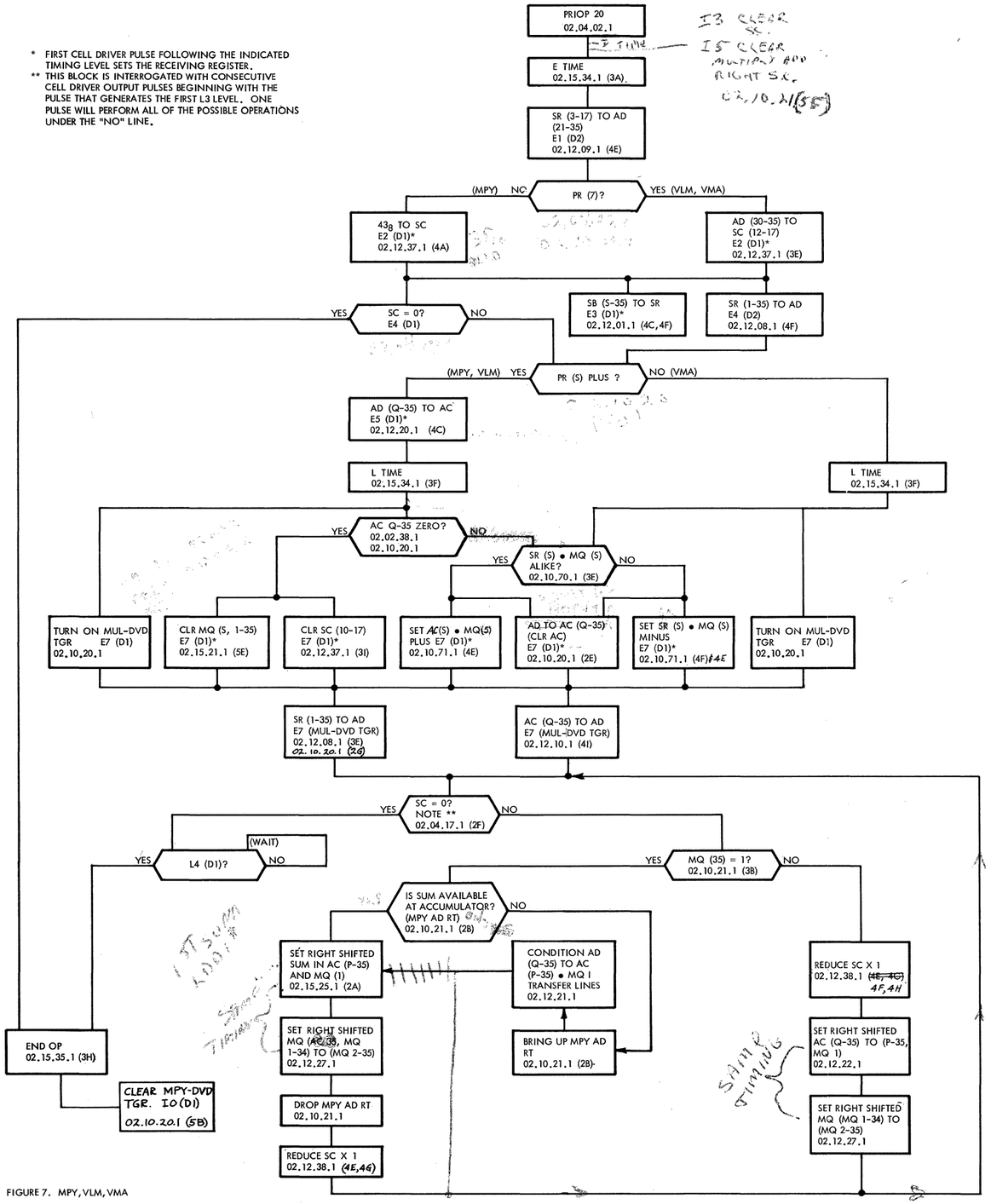
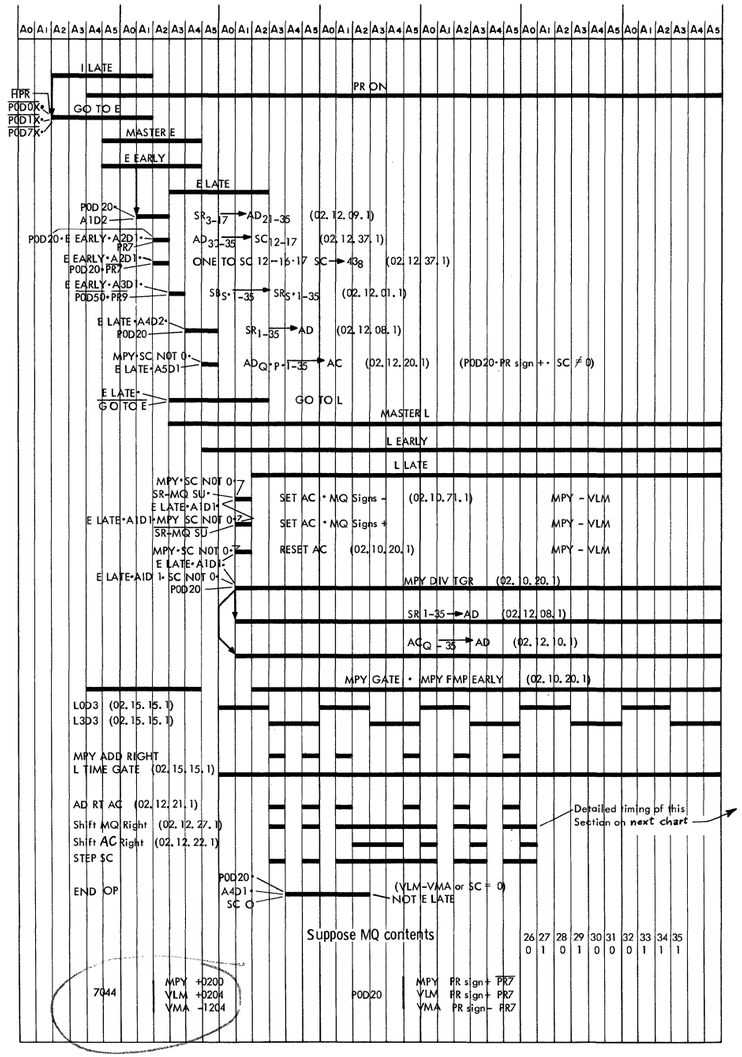


FIGURE 7. MPY, VLM, VMA

Multiply (MPY +0200)

Multiplies the contents of the specified memory location (multiplicand) by the contents of the MQ register (multiplier). The result is a 70-bit product that appears in the combined accumulator-MQ. The 35 most significant bits of the product replace the contents of the accumulator (1-35), and the least significant bits replace the contents of the MQ register (1-35). Accumulator P and Q are cleared. The signs of both the accumulator and the MQ register are set to the algebraic sign of the product. The number of bits to the right of the binary point of the first factor added to the number of bits to the right of the binary point of the second factor gives the total number of bits to the right of the binary point in the product.



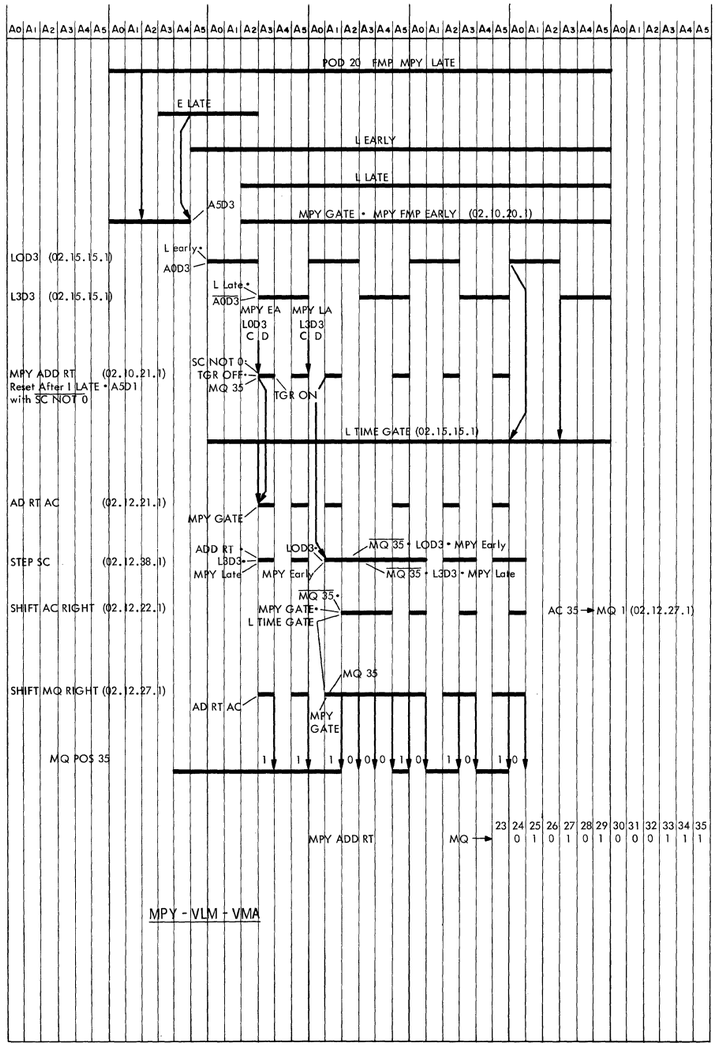
Variable-Length Multiply (VLM +0204)
Multiplies the contents of the specified memory location (multiplicand) by the C low-order bits of the MQ to produce a 35-plus-C bit product. C denotes the number of bits in the MQ to be used as the multiplier indicated by bits 12-17 in the instruction word. The 35 most significant bits of the product replace the contents of the accumulator (1-35), and the C least significant bits replace the contents of the MQ register (1-C). Accumulator positions Q and P are cleared. The remaining 35 minus C positions of the MQ register contain the original 35 minus C high-order bits of the MQ register. The signs of the accumulator and the MQ register are set to the algebraic sign of the product.

If C is 0, the instruction is interpreted as no-operation and the computer proceeds to the next instruction in sequence, leaving the accumulator unchanged.

If C is not 0,but the contents of the memory location are 0, the contents of the accumulator and the MQ register are cleared.

Variable-Length Multiply and Accumulate (VMA -1204)
VMA is similar to VLM except that the contents of the accumulator (Q, P, 1-35) are not cleared before the multiplication process begins. This results in adding the 35-plus-C bit product onto the original contents of the accumulator (Q, P, 1-35). If accumulator bit positions P and Q both originally contained 1's, a carry may be lost during the accumulation and the overflow indicator is not turned on. The C least significant bits of the result replace the contents of MQ 1-C. The 36 most significant bits replace the contents of the accumulator (P, 1-35). Accumulator bit position Q is cleared. The remaining 35 minus C positions of the MQ contain the original 35 minus C high-order bits. The signs of the accumulator and MQ are set according to the algebraic sign of the product.

If C is 0, the instruction is interpreted as no-operation and the computer proceeds to the next instruction in sequence, leaving the accumulator unchanged.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00005	056000 000005
00001	MPY		00006	020000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			400000 777777
00006	Pattern			000000 777777

Multiply (MPY)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+560	000	0	00005	056000000005	000000000000	00	000000000000	
E	I	00001	+560	000	0	00001	400000777777	000000000000	00	400000777777	
I	E	00002	+200	000	0	00006	020000000006	000000000000	00	400000777777	
E	L(1)	00002	+200	043	0	00006	000000777777	400000000000	00	400000777777	
L(1)	L(2)	00002	+200	040	0	00006	000000777777	400000677777	00	440000077777	
L(2)	L(3)	00002	+200	035	0	00006	000000777777	400000767777	00	404000007777	
L(3)	L(4)	00002	+200	032	0	00006	000000777777	400000776777	00	400400000777	
L(4)	L(5)	00002	+200	027	0	00006	000000777777	400000777677	00	400040000077	
L(5)	L(6)	00002	+200	024	0	00006	000000777777	400000777767	00	400004000007	
L(6)	L(7)	00002	+200	021	0	00006	000000777777	400000777776	00	400000400000	
L(7)	L(8)	00002	+200	013	0	00006	000000777777	400000007777	00	770000004000	
L(8)	L(9)	00002	+200	005	0	00006	000000777777	400000000077	00	777700000040	
L(9)	L(10)	00002	+200	000	0	00006	000000777777	400000000001	00	777776000001	
L(10)	I	00002	+200	000	0	00002	000000777777	400000000001	00	777776000001	
I	I	00003	+020	000	0	00000	002000000000	400000000001	00	777776000001	
I	E	00001	+560	000	0	00005	056000000005	400000000001	00	777776000001	
E	I	00001	+560	000	0	00001	400000777777	400000000001	00	400000777777	
I	E	00002	+200	000	0	00006	020000000006	400000000001	00	400000777777	

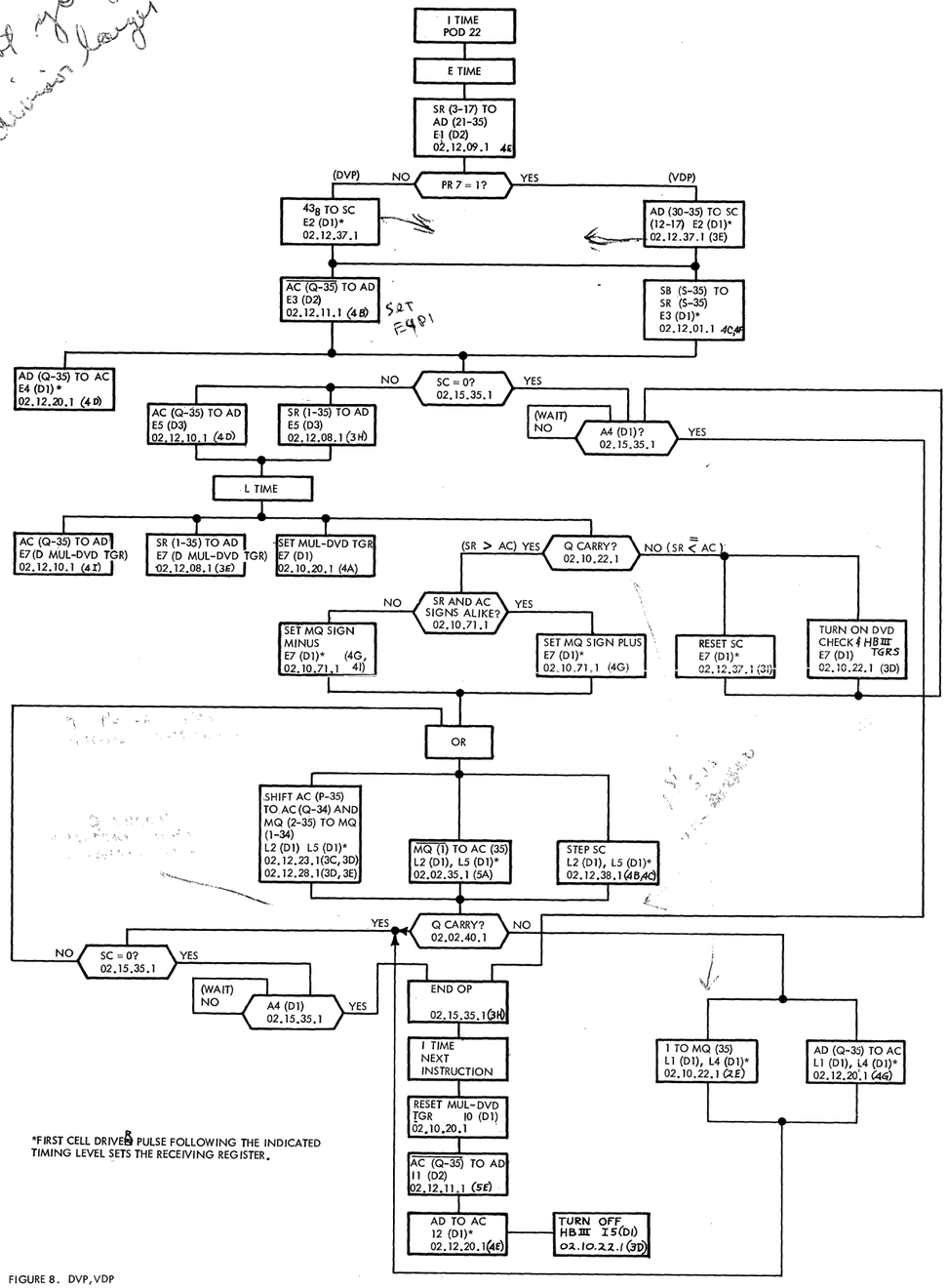
Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00005	056000 000005
00001	VLM (C=22)		00005	020422 000005
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			000000 777777

Variable Length Multiply (VLM)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVF
I	E	00001	+560	000	0	00005	056000000005	000000000000	00	000000000000				
E	I	00001	+560	000	0	00001	000000777777	000000000000	00	000000777777				
I	E	00002	+204	000	0	00005	020422000005	000000000000	00	000000777777			16	
E	L(1)	00002	+204	022	0	00005	000000777777	000000000000	00	000000777777			16	
L(1)	L(2)	00002	+204	017	0	00005	000000777777	000000677777	00	040000077777			16	
L(2)	L(3)	00002	+204	014	0	00005	000000777777	000000767777	00	004000007777			16	
L(3)	L(4)	00002	+204	011	0	00005	000000777777	000000776777	00	000400000777			16	
L(4)	L(5)	00002	+204	006	0	00005	000000777777	000000777677	00	000040000077			16	
L(5)	L(6)	00002	+204	003	0	00005	000000777777	000000777767	00	000004000007			16	
L(6)	L(7)	00002	+204	000	0	00005	000000777777	000000777776	00	000000400000			16	
L(7)	I	00002	+204	000	0	00002	000000777777	000000777776	00	000000400000			16	
I	I	00003	+020	000	0	00000	002000000000	000000777776	00	000000400000				
I	E	00001	+560	000	0	00005	056000000005	000000777776	00	000000400000				
E	I	00001	+560	000	0	00001	000000777777	000000777776	00	000000777777				
I	E	00002	+204	000	0	00005	020422000005	000000777776	00	000000777777			16	

SR must be > AC
if not you get Divide Check
divisor larger than dividend

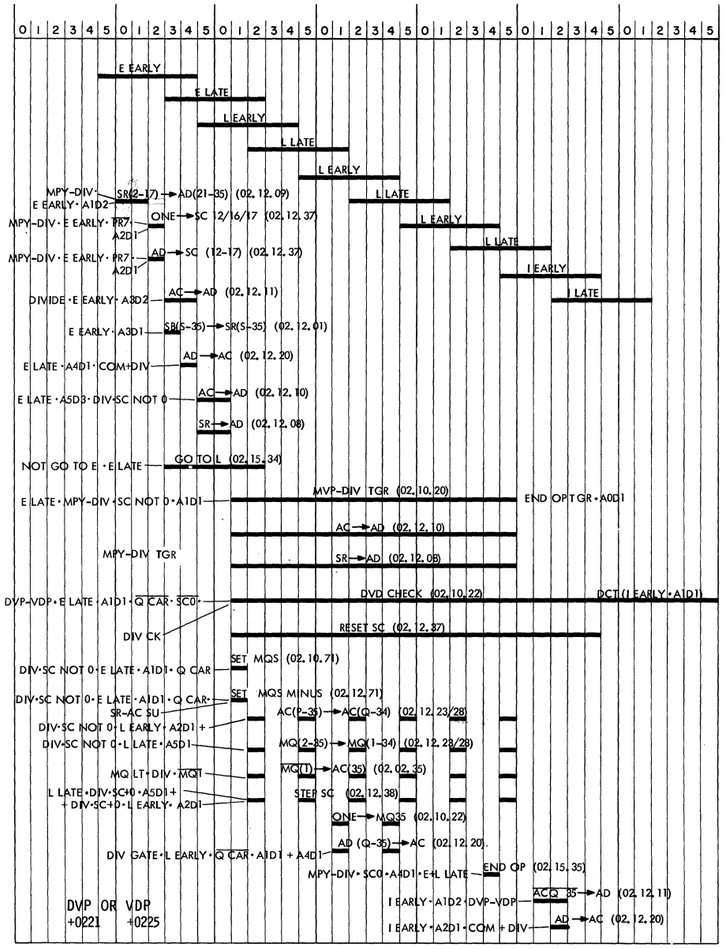


*FIRST CELL DRIVEN BY PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

FIGURE 8. DVP, VDP

Divide or Proceed (DVP +0221)
Treats the contents of the accumulator (Q,P,1-35) and the contents of the MQ register (1-35) as a 70-bit dividend, plus sign, and the contents of the memory location as a 35-bit divisor. If the memory word (divisor) is greater than the accumulator (high-order half of the dividend), division occurs. A 35-bit quotient replaces the contents of the MQ (1-35) and the remainder replaces the contents of the accumulator (1-35). The MQ sign is the algebraic sign of the quotient, and the accumulator sign is the sign of the dividend. If the memory word (divisor) is less than or equal to the accumulator (high-order half of the dividend), division does not occur and the divide-check indicator is turned on; the computer proceeds to the next instruction.

Variable-Length Divide or Proceed (VDP +0225)
Variable divide is the same as straight divide (DVP) except that bits 12-17 of the instruction word determine the number of partial divisions that are to occur. A C-length quotient (C determined by instruction word bits 12-17) with a sign replaces the C low-order positions of the MQ. The remainder replaces the contents of accumulator 1-35 and the 35 minus C high-order positions of the MQ. Initially, C rather than 43₈ is placed in the shift counter. If C is 0, the instruction is interpreted as no-operation and the computer proceeds directly to the next instruction in sequence.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00004	050000 000004
00001	LDQ		00005	056000 000005
00002	DVP		00006	022100 000006
00003	TRA		00000	002000 000000
00004	Pattern			000000 000000
00005	Pattern			007777 600001
00006	Pattern			000000 077777

Divide or Proceed (DVP)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	000000000000	000000000000	00	000000000000											
I	E	00002	+560	000	0	00005	056000000005	000000000000	00	000000000000											
E	I	00002	+560	000	0	00002	007777600001	000000000000	00	007777600001											
I	E	00003	+221	000	0	00006	022100000006	000000000000	00	007777600001											
E	L (1)	00003	+221	043	0	00006	000000077777	377777777777	11	007777600001								1	0		
L (1)	L (2)	00003	+221	041	0	00006	000000077777	377777777777	11	037777000004								1	1		
L (2)	L (3)	00003	+221	037		00006	000000077777	377777777777	11	177774000020								1	1		
L (3)	L (4)	00003	+221	035	0	00006	000000077777	377777777776	11	377760000100								1	1		
L (4)	L (5)	00003	+221	033		00006	000000077777	377777777770	11	377700000400								1	1		
L (5)	L (6)	00003	+221	031		00006	000000077777	377777777740	11	377400002000								1	1		
L (6)	L (7)	00003	+221	027		00006	000000077777	377777777600	11	376000010000								1	1		
L (7)	L (8)	00003	+221	025		00006	000000077777	377777777000	11	370000040000								1	1		
L (8)	L (9)	00003	+221	023		00006	000000077777	377777774000	11	340000200000								1	1		
L (9)	L (10)	00003	+221	021		00006	000000077777	377777760000	11	200001000000								1	1		
L (10)	L (11)	00003	+221	017		00006	000000077777	377777700001	11	000004000000								1	1		
L (11)	L (12)	00003	+221	015		00006	000000077777	377777600005	11	000020000002								1	1		
L (12)	L (13)	00003	+221	013		00006	000000077777	377777600021	11	000100000016								1	1		
L (13)	L (14)	00003	+221	011		00006	000000077777	377777600101	11	000400000076								1	1		
L (14)	L (15)	00003	+221	007		00006	000000077777	377777600401	11	002000000376								1	1		
L (15)	L (16)	00003	+221	005		00006	000000077777	377777602001	11	010000001776								1	1		
L (16)	L (17)	00003	+221	003		00006	000000077777	377777610001	11	040000007776								1	1		
L (17)	L (18)	00003	+221	001		00006	000000077777	377777640001	11	200000037776								1	1		
L (18)	I	00003	+221	000	0	00003	000000077777	377777777777	11	000000077777								1	0		
I	I	00004	+020	000	0	00000	002000000000	000000000000	00	000000077777								0	0		
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000077777								0	0		
E	I	00001	+500	000	0	00001	000000000000	000000000000	00	000000077777								0	0		
I	E	00002	+560	000	0	00005	056000000005	000000000000	00	000000077777								0	0		

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00004	050000 000000
00001	LDQ		00005	056000 000005
00002	VDP (C=24)		00006	022524 000006
00003	TRA		00000	002000 000000
00004	Pattern			000000 000000
00005	Pattern			007777 600001
00006	Pattern			400000 077777

Variable Length Divide or Proceed (VDP)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	000000000000	000000000000	00	000000000000											
I	E	00002	+560	000	0	00005	056000000005	000000000000	00	000000000000											
E	I	00002	+560	000	0	00002	007777600001	000000000000	00	007777600001											
I	E	00003	+225	000	0	00006	022524000006	000000000000	00	007777600001			15								
E	L (1)	00003	+225	024	0	00006	400000077777	377777777777	11	407777600001			15					1			
L (1)	L (2)	00003	+225	022	0	00006	400000077777	377777777777	11	437777000004			15					1	1		
L (2)	L (3)	00003	+225	020	0	00006	400000077777	377777777777	11	577774000020			15					1	1		
L (3)	L (4)	00003	+225	016	0	00006	400000077777	377777777776	11	777760000100			15					1	1		
L (4)	L (5)	00003	+225	014	0	00006	400000077777	377777777770	10	777700000400			15					1	1		
L (5)	L (6)	00003	+225	012	0	00006	400000077777	377777777740	10	777400002000			15					1	1		
L (6)	L (7)	00003	+225	010	0	00006	400000077777	377777777600	10	776000010000			15					1	1		
L (7)	L (8)	00003	+225	006	0	00006	400000077777	377777777000	10	770000040000			15					1	1		
L (8)	L (9)	00003	+225	004	0	00006	400000077777	377777774000	10	740000200000			15					1	1		
L (9)	L (10)	00003	+225	002	0	00006	400000077777	377777760000	10	600001000000			15					1	1		
L (10)	L (11)	00003	+225	000	0	00006	400000077777	377777700001	10	400004000000			15					1	1		
L (11)	I	00003	+225	000	0	00003	400000077777	377777700001	10	400004000000			15					1	1		
I	I	00004	+020	000	0	00000	002000000000	000000077776	00	400004000000											
I	E	00001	+500	000	0	00004	050000000004	000000077776	00	400004000000											
E	I	00001	+500	000	0	00001	000000000000	000000000000	00	400004000000											
I	E	00002	+560	000	0	00005	056000000005	000000000000	00	400004000000											
E	I																				

Floating Add (FAD +0300)
Adds the floating-point number in the specified memory location to the accumulator. The most significant portions of the result appear as a normalized floating-point number in the accumulator. The least significant portion of the result appears in the MQ register as a floating-point number with a characteristic 33_8 less than the accumulator characteristic. The signs of the accumulator and the MQ are set to the sign of the larger factor. The sum in the accumulator and MQ is always normalized whether the original factors are normalized or not. If the contents of the accumulator (1-35) contain 0's, the FAD instruction may be used to normalize an unnormalized floating-point number.

Unnormalized Floating Add (UFA -0300)
Same as FAD except that the sum is not normalized.

Floating Subtract (FSB +0302)
Algebraically subtracts the floating-point number in the specified memory location from the floating-point number in the accumulator. The results are normalized.

Unnormalized Floating Subtract (UFS -0302)
Same as FSB except that the difference is not normalized.

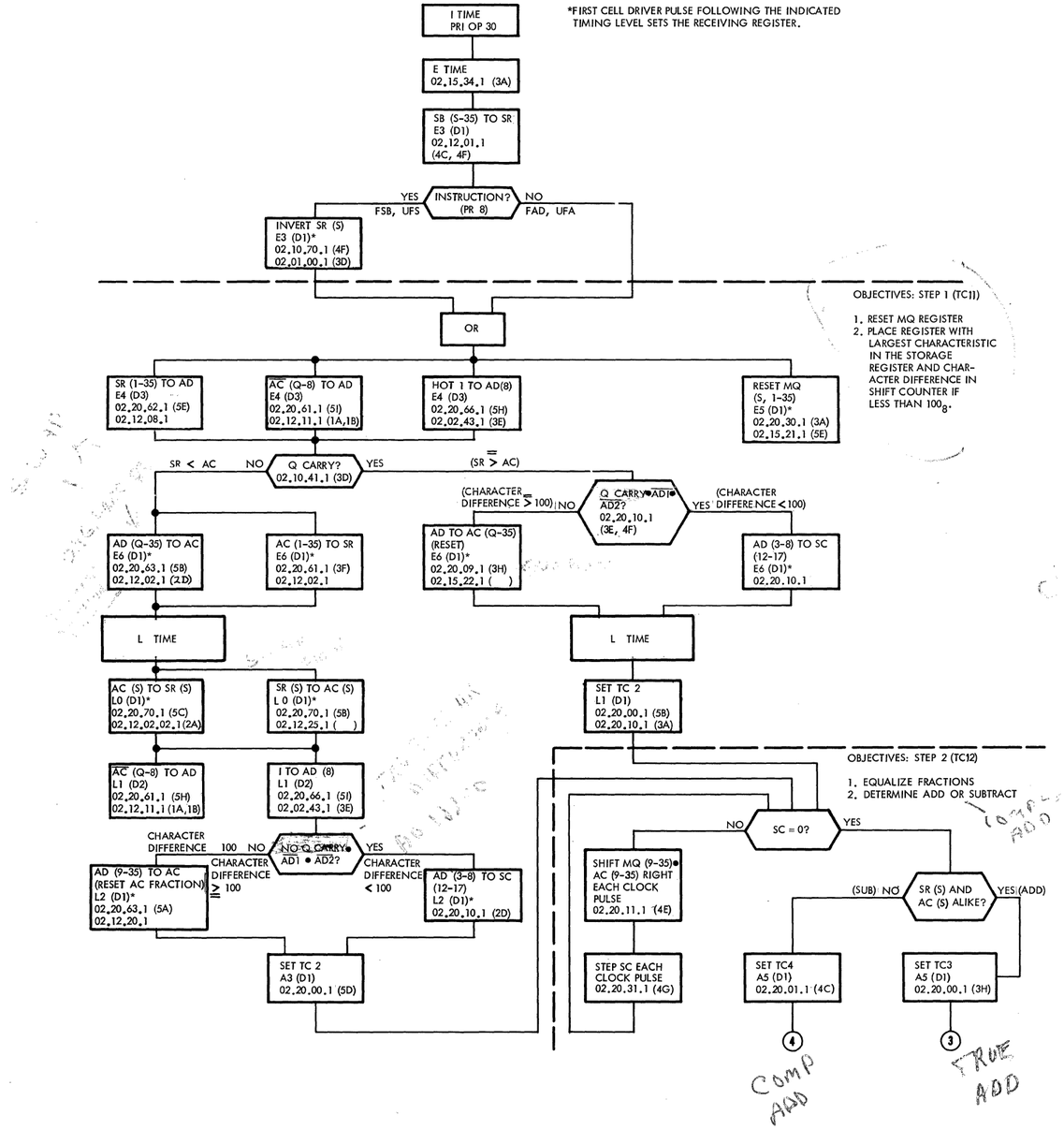
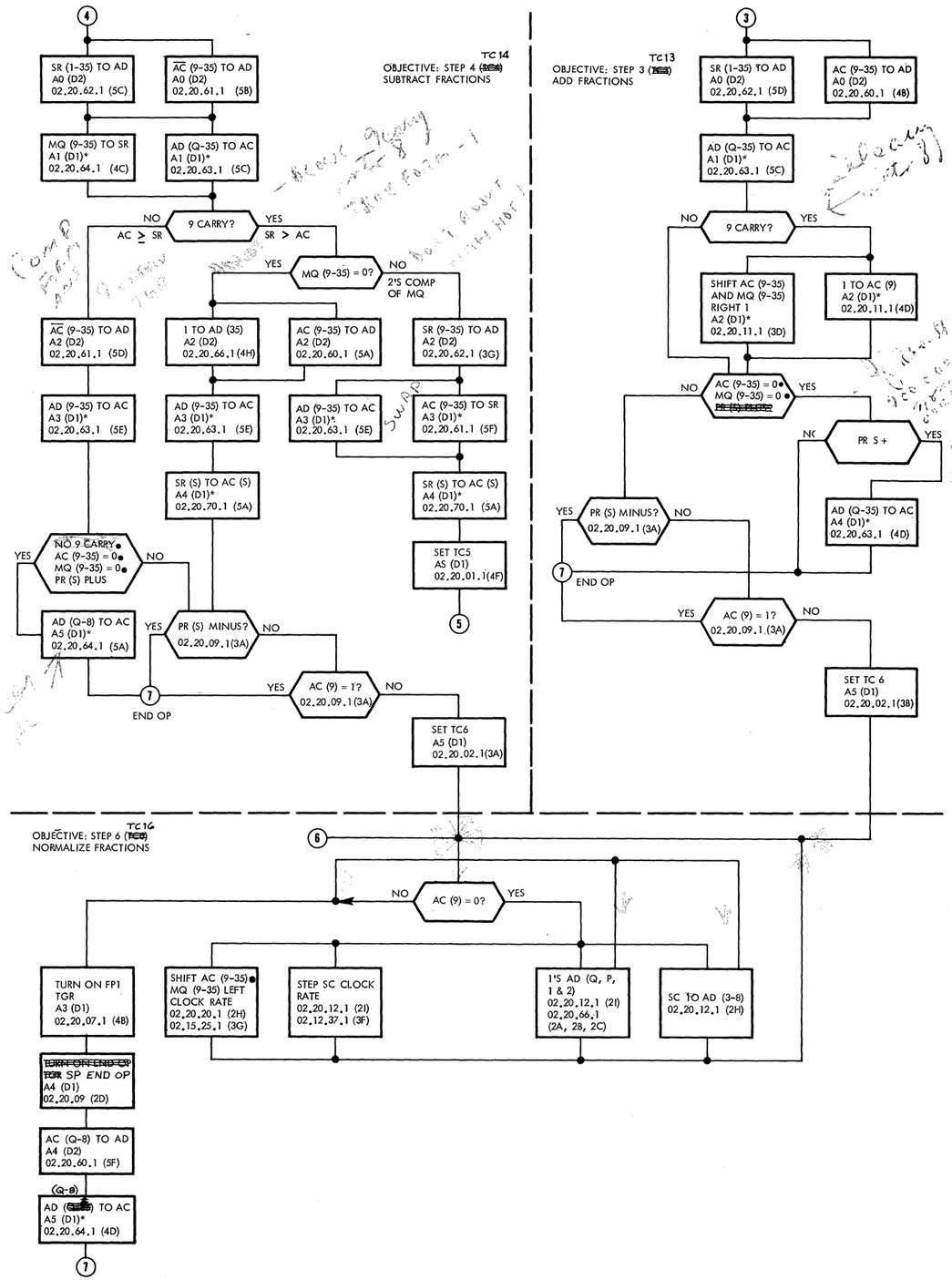
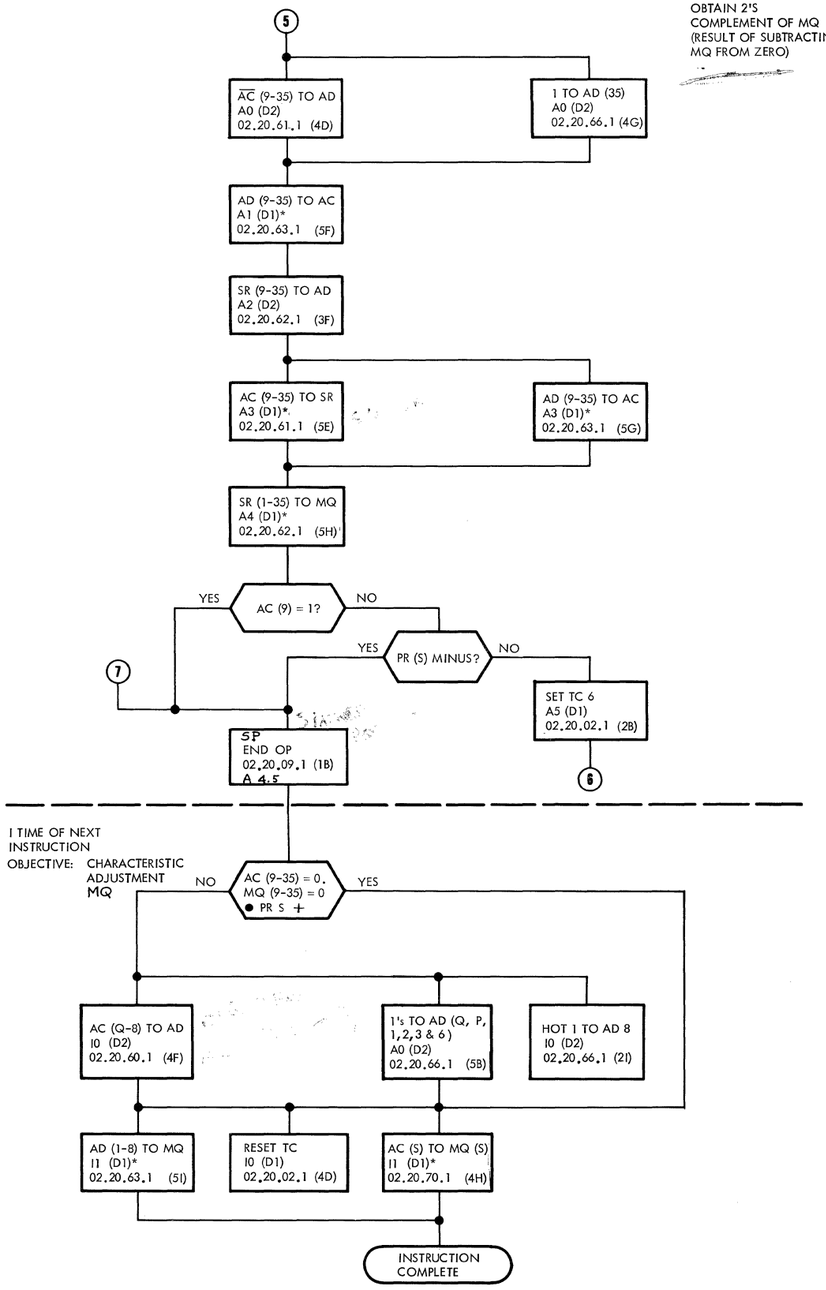


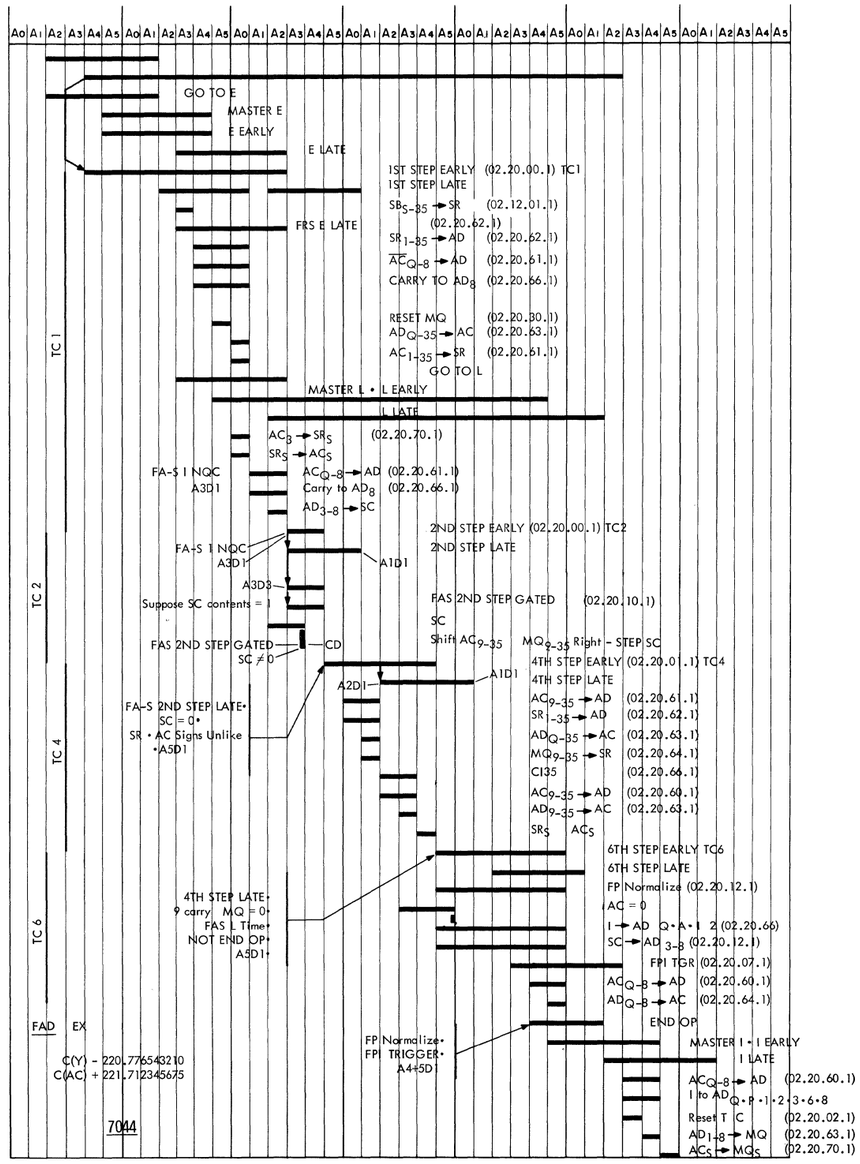
FIGURE 9. FAD, UFA, FSB, UFS



OBJECTIVE:

OBTAIN 2'S COMPLEMENT OF MQ (RESULT OF SUBTRACTING MQ FROM ZERO)





Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	FAD		00006	030000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			600012 334567
00006	Pattern			606065 443210

Floating Add(FAD)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	600012334567	600012334567	00	000000000000											
I	E	00002	+300	000	0	00006	030000000006	600012334567	00	000000000000	1 & 10										
E	L(1)	00002	+300	006	0	00006	606065443210	600012334567	00	000000000000	1 & 10					1					
L(1)	L(2)	00002	+300	001	0	00006	606065443210	600000246713	00	000560000000	2 & 10					1					
L(2)	L(3)	00002	+300	000	0	00006	606065443210	600000123345	00	000670000000	3 & 10					1					
L(3)	L(4)	00002	+300	377	0	00006	606065443210	606153355333	00	000560000000	6 & 10					1					
L(4)	I	00002	+300	375	0	00002	606065443210	603655665556	00	000700000000	6 & 10					1					1
I	I	00003	+020	000	0	00000	002000000000	603655665556	00	550700000000											
I	E	00001	+500	000	0	00005	050000000005	603655665556	00	550700000000											
E	I	00001	+500	000	0	00001	600012334567	600012334567	00	550700000000											
I	E	00002	+300	000	0	00006	030000000006	600012334567	00	550700000000											

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	UFA		00006	430000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			377777 777777
00006	Pattern			200000 000000

Unnormalized Floating Add (UFA)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	377777777777	377777777777	00	000000000000											
I	E	00002	-300	000	0	00006	430000000006	377777777777	00	000000000000	1&10										
E	L(1)	00002	-300	000	0	00006	377777777777	201000000000	11	000000000000	1 &10										
L(1)	L(2)	00002	-300	000	0	00006	377777777777	201000000000	11	000000000000	3 &10										
L(2)	I	00002	-300	000	0	00002	377777777777	377777777777	00	000000000000	3 &10										
I	I	00003	+020	000	0	00000	002000000000	377777777777	00	344000000000											
I	E	00002	+500	000	0	00005	050000000005	377777777777	00	344000000000											
E	I	00002	+500	000	0	00001	377777777777	377777777777	00	344000000000											
I	E	00002	-300	000	0	00006	430000000006	377777777777	00	344000000000											

FIGURE 9. FAD, UFA, FSB, UFS (CONTINUED)

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00004	050000 000004
00001	FSB		00005	030200 000005
00002	TRA		00000	002000 000000
00003				
00004	Pattern			606065 443210
00005	Pattern			600012 334567
00006				

Floating Subtract (FSB)

		CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	606065443210	606065443210	00	000000000000											
I	E	00002	+302	000	0	00005	030200000005	606065443210	00	000000000000	1 & 10										
E	L(1)	00002	+302	000	0	00005	606065443210	372012334567	11	000000000000	1 & 10										
L(1)	L(2)	00002	+302	003	0	00005	606065443210	372001233456	11	000700000000	2 & 10										
L(2)	L(3)	00002	+302	000	0	00005	606065443210	372000123345	11	000670000000	4 & 10										
L(3)	L(4)	00002	+302	000	0	00005	606065443210	606670000000	00	000670000000	5 & 10						1				
L(4)	L(5)	00002	+302	377	0	00005	606110000000	606152637504	00	206220000000	6 & 10						1				
L(5)	I	00002	+302	375	0	00002	606110000000	603653176421	00	206100000000	6 & 10						1				1
I	I	00003	+020	000	0	00000	002000000000	603653176421	00	550100000000											
I	E	00001	+500	000	0	00004	050000000004	603653176421	00	550100000000											
E	I	00001	+500	000	0	00001	606065443210	606065443210	00	550100000000											
I	E	00002	+302	000	0	00005	030200000005	506065443210	00	550100000000	1 & 10										

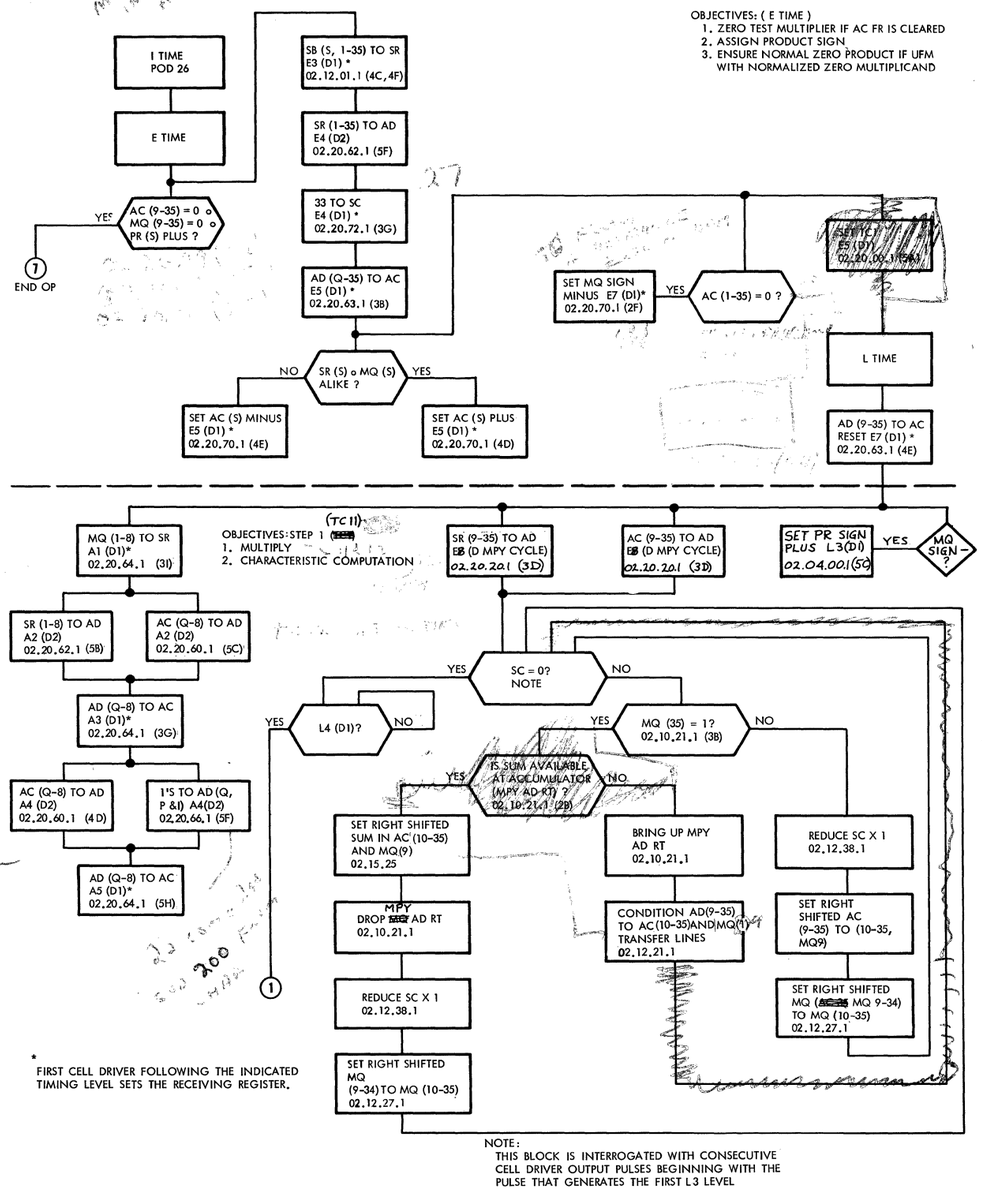
Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00004	056000 000004
00001	CLA		00005	050000 000005
00002	UFS		00006	430200 000006
00003	TRA		00000	002000 000000
00004	Pattern			777777 777777
00005	Pattern			200012 334567
00006	Pattern			206065 443210

Unnormalized Floating Subtract (UFS)

		CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+560	000	0	00004	056000000004	000000000000	00	000000000000											
E	I	00001	+560	000	0	00001	777777777777	000000000000	00	777777777777											
I	E	00002	+500	000	0	00005	050000000005	000000000000	00	777777777777											
E	I	00002	+500	000	0	00002	200012334567	200012334567	00	777777777777											
I	E	00003	-302	000	0	00006	430200000006	200012334567	00	777777777777	1 & 10										
E	L(1)	00003	-302	006	0	00006	606065443210	200012334567	00	000000000000	1 & 10					1					
L(1)	L(2)	00003	-302	001	0	00006	606065443210	200000246713	00	000660000000	2 & 10					1					
L(2)	L(3)	00003	-302	000	0	00006	606065443210	200000123345	00	000670000000	4 & 10					1					
L(3)	L(4)	00003	-302	000	0	00006	606065443210	606670000000	00	000670000000	5 & 10					1	1				
L(4)	I	00003	-302	000	0	00003	606110000000	606065317642	00	206110000000	5 & 10					1	1				
I	I	00004	+020	000	0	00000	002000000000	606065317642	00	553110000000											
I	E	00001	+560	000	0	00004	056000000004	606065317642	00	553100000000											
E	I	00001	+560	000	0	00001	777777777777	606065317642	00	777777777777											
I	E	00002	+500	000	0	00005	050000000005	606065317642	00	777777777777											

Floating Multiply (FMP +0260)
Multiplies the contents of the specified memory location by the contents of the MQ register. The most significant part of the product appears in the accumulator, and the least significant part appears in the MQ register. The product of two normalized numbers is in normalized form. If either number is not normalized, the product may or may not be in normalized form.

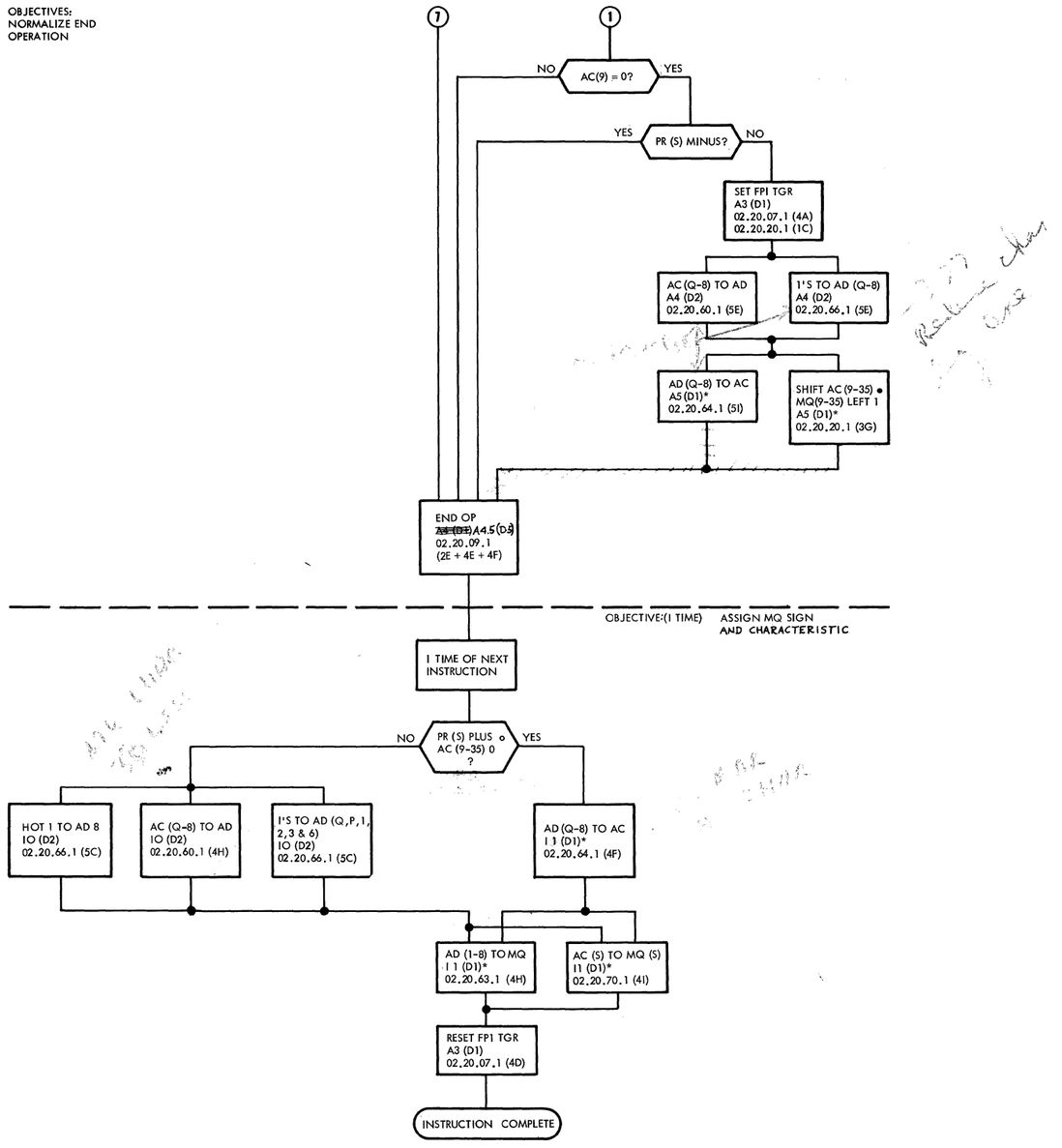
Unnormalized Floating Multiply (UFM –0260)
Multiplies the contents of the specified memory location by the contents of the MQ register. The result is not normalized.



* FIRST CELL DRIVER FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

FIGURE 10. FMP, UFM

OBJECTIVES:
NORMALIZE END OPERATION



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	LDQ		00005	056000 000005
00002	FMP		00006	026000 000006
00003	TRA		00000	002000 000000
00004				
00005	Pattern			611777 777777
00006	Pattern			600777 777777

Floating Multiply (FMP)

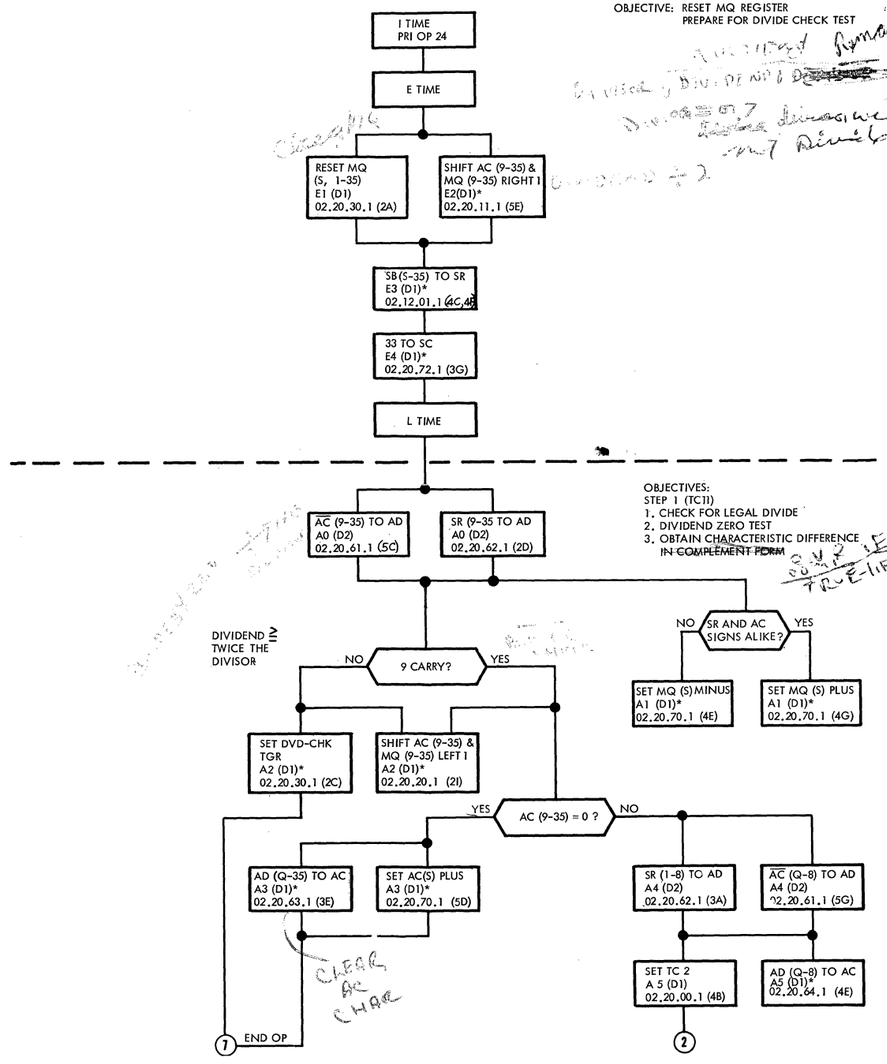
												CONSOLE INDICATORS										
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	611777777777	611777777777	00	000000000000											
I	E	00002	+560	000	0	00005	056000000005	611777777777	00	000000000000											
E	I	00002	+560	000	0	00002	611777777777	611777777777	00	611777777777											
I	E	00003	+260	000	0	00006	026000000006	611777777777	00	611777777777	1 & 10										
E	L(1)	00003	+260	033	0	00006	600777777777	200000000000	00	211777777777	1 & 10										
L(1)	L(2)	00003	+260	030	0	00006	611777777777	211677777777	00	211177777777	2 & 10									1	
L(2)	L(3)	00003	+260	025	0	00006	611777777777	211767777777	00	211077777777	2 & 10									1	
L(3)	L(4)	00003	+260	022	0	00006	611777777777	211776777777	00	211001777777	2 & 10									1	
L(4)	L(5)	00003	+260	017	0	00006	611777777777	211777577777	00	211000177777	2 & 10									1	
L(5)	L(6)	00003	+260	014	0	00006	611777777777	211777767777	00	211000017777	2 & 10									1	
L(6)	L(7)	00003	+260	011	0	00006	611777777777	211777776777	00	211000001777	2 & 10									1	
L(7)	L(8)	00003	+260	006	0	00006	611777777777	211777777677	00	211000000177	2 & 10									1	
L(8)	L(9)	00003	+260	003	0	00006	611777777777	211777777767	00	211000000017	2 & 10									1	
L(9)	L(10)	00003	+260	000	0	00006	611777777777	211777777776	00	211000000001	2 & 10									1	
L(10)	I	00003	+260	000	0	00003	611777777777	211777777776	00	211000000001	2 & 10									1	
I	I	00004	+020	000	0	00000	002000000000	211777777776	00	156000000001											
I	E	00001	+500	000	0	00005	050000000005	211777777776	00	156000000001											
E	I	00001	+500	000	0	00001	611777777777	611777777777	00	156000000001											
I	E	00002	+560	000	0	00005	056000000005	611777777777	00	156000000001											

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	LDQ		00005	056000 000006
00002	UFM		00006	426000 000006
00003	TRA		00000	002000 000000
00004				
00005	Pattern			200000 777777
00006	Pattern			200000 777777

Unnormalized Floating Multiply (UFM)

												CONSOLE INDICATORS										
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	200000777777	200000777777	00	000000000000											
I	E	00002	+560	000	0	00006	056000000006	200000777777	00	000000000000											
E	I	00002	+560	000	0	00002	200000777777	200000777777	00	200000777777											
I	E	00003	-260	000	0	00006	426000000006	200000777777	00	200000777777	1 & 10										
E	L(1)	00003	-260	033	0	00006	200000777777	200000000000	00	200000777777	1 & 10										
L(1)	L(2)	00003	-260	030	0	00006	200000777777	200000677777	00	200100077777	2 & 10										
L(2)	L(3)	00003	-260	025	0	00006	200000777777	200000767777	00	200010007777	2 & 10										
L(3)	L(4)	00003	-260	022	0	00006	200000777777	200000776777	00	200001000777	2 & 10										
L(4)	L(5)	00003	-260	017	0	00006	200000777777	200000777677	00	200000100077	2 & 10										
L(5)	L(6)	00003	-260	014	0	00006	200000777777	200000777767	00	200000010007	2 & 10										
L(6)	L(7)	00003	-260	011	0	00006	200000777777	200000777776	00	200000001000	2 & 10										
L(7)	L(8)	00003	-260	003	0	00006	200000777777	200000007777	00	200760000010	2 & 10										
L(8)	I	00003	-260	000	0	00003	200000777777	200000000777	00	200776000001	2 & 10										
I	I	00004	+020	000	0	00000	002000000000	200000000777	00	145776000001											
I	E	00001	+0500	000	0	00005	050000000005	200000000777	00	145776000001											
E	I	00001	+0500	000	0	00001	200000777777	200000777777	00	145776000001											
I	E	00002	+560	000	0	00006	056000000006	200000777777	00	145776000001											

Floating Divide or Proceed (FDP +0241)
Divides the contents of the accumulator (dividend) by the contents of the specified memory location (divisor). The quotient appears in the MQ register, and the remainder appears in the accumulator. If the dividend fraction is greater than or equal to twice that of the divisor fraction, or if the divisor fraction is 0, division does not occur and the computer takes the next instruction in sequence. The quotient is in normal form if both the dividend and the divisor are in normal form. The sign of the MQ is the algebraic sign of the quotient. If the dividend fraction is 0, the contents of the accumulator (Q, P, 1-35) are cleared and the sign is set plus.



* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.

OBJECTIVE: RESET MQ REGISTER
PREPARE FOR DIVIDE CHECK TEST

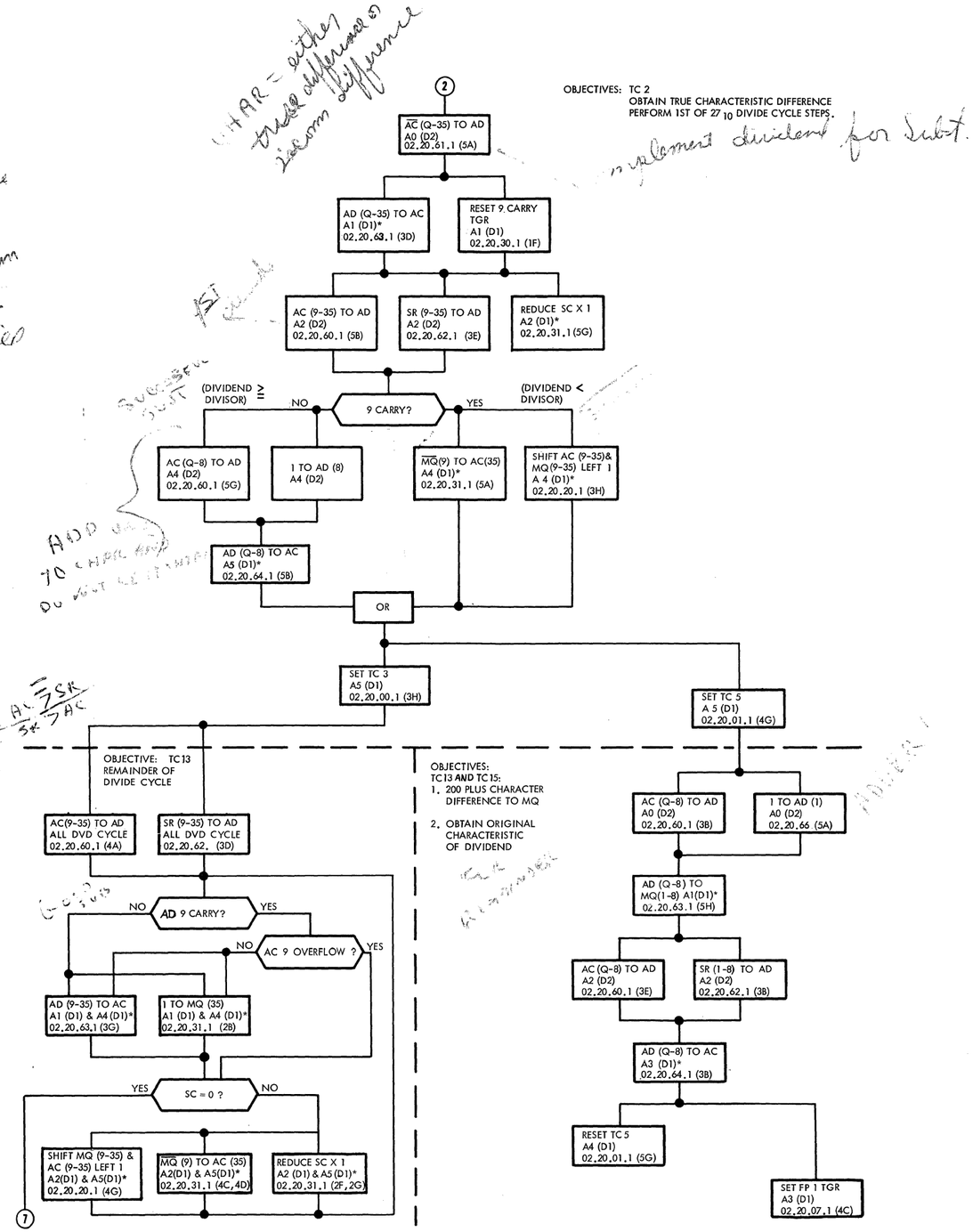
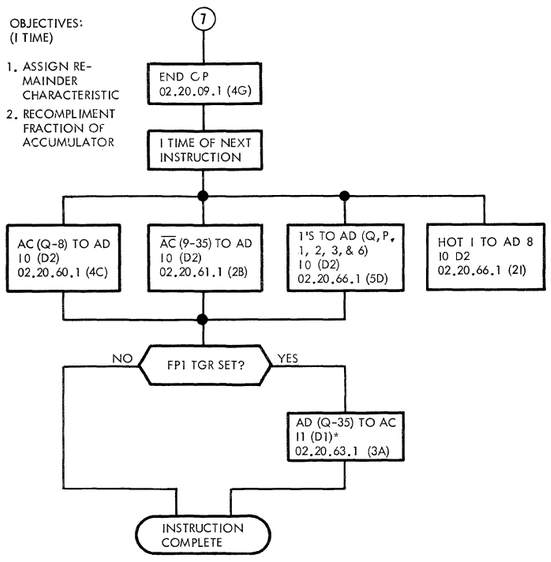


FIGURE 11. FDP



* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00007	056000 000007
00001	CLA		00005	050000 000005
00002	FDP		00006	024100 000006
00003	TRA		00000	002000 000000
00004				
00005	Pattern			173516 274051
00006	Pattern			176444 444445
00007	Live Reg			000000 000000

Floating Divide or Proceed (FDP)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+560	000	0	00007	056000000007														
E	I	00001	+560	000	0	00001	000000000000														
I	E	00002	+500	000	0	00005	050000000005														
E	I	00002	+500	000	0	00002	173516274051	173516274051	00												
I	E	00003	+241	000	0	00006	024100000006	173516274051	00		1&10										
E	L (1)	00003	+241	033	0	00006	176444444445	173247136024	00	000400000000	1&10										
L (1)	L (2)	00003	+241	033	0	00006	176444444445	002516274051	00	000000000000	2&10						1				
L (2)	L (3)	00003	+241	032	0	00006	176444444445	376261503726	11	000000000000	3,5,10										
L (3)	L (4)	00003	+241	030	0	00006	176444444445	174530641757	00	176000000004	3&10						1	1		1	
L (4)	L (5)	00003	+241	026	0	00006	176444444445	174654321011	00	176000000022	3&10						1	1		1	
L (5)	L (6)	00003	+241	024	0	00006	176444444445	174261504047	00	176000000110	3&10						1	1		1	
L (6)	L (7)	00003	+241	022	0	00006	176444444445	174560642463	00	176000000444	3&10						1	1		1	
L (7)	L (8)	00003	+241	020	0	00006	176444444445	174654323431	00	176000002222	3&10						1	1		1	
L (8)	L (9)	00003	+241	016	0	00006	176444444445	174261516147	00	176000011110	3&10						1	1		1	
L (9)	L (10)	00003	+241	014	0	00006	176444444445	174530713063	00	176000044444	3&10						1	1		1	
L (10)	L (11)	00003	+241	012	0	00006	176444444445	174654565431	00	176000222222	3&10						1	1		1	
L (11)	L (12)	00003	+241	010	0	00006	176444444445	174262726147	00	176001111110	3&10						1	1		1	
L (12)	L (13)	00003	+241	006	0	00006	176444444445	174535753063	00	176004444444	3&10						1	1		1	
L (13)	L (14)	00003	+241	004	0	00006	176444444445	174700765431	00	176022222222	3&10						1	1		1	
L (14)	L (15)	00003	+241	002	0	00006	176444444445	174403726147	00	176111111110	3&10						1	1		1	
L (15)	L (16)	00003	+241	000	0	00006	176444444445	174130641751	00	176444444442	3&10						1	1		1	
L (16)	I	00003	+241	000	0	00003	176444444445	174575306416	00	176444444443	3&10						1			1	
I	I	00004	+020	000	0	00000	002000000000	141202471361	00	176444444443											
I	E	00001	+560	000	0	00007	056000000007	141202471361	00	176444444443											
E	I	00001	+560	000	0	00001	000000000000	141202471361	00	000000000000											
I	E	00002	+500	000	0	00005	050000000005	141202471361	00	000000000000											

Double-Precision Floating Add (DFAD +0301)
Adds the double-precision number in the specified memory location and the next higher location to the number in the accumulator and MQ registers. The result is a normalized double-precision number with the major answer in the accumulator and the minor in the MQ. The sign of the accumulator and MQ is that of the algebraic sign.

Double-Precision Floating Subtract (DFSB +0303)
The same as DFAD except that the sign of the double-precision number in memory is inverted at the beginning of the operation.

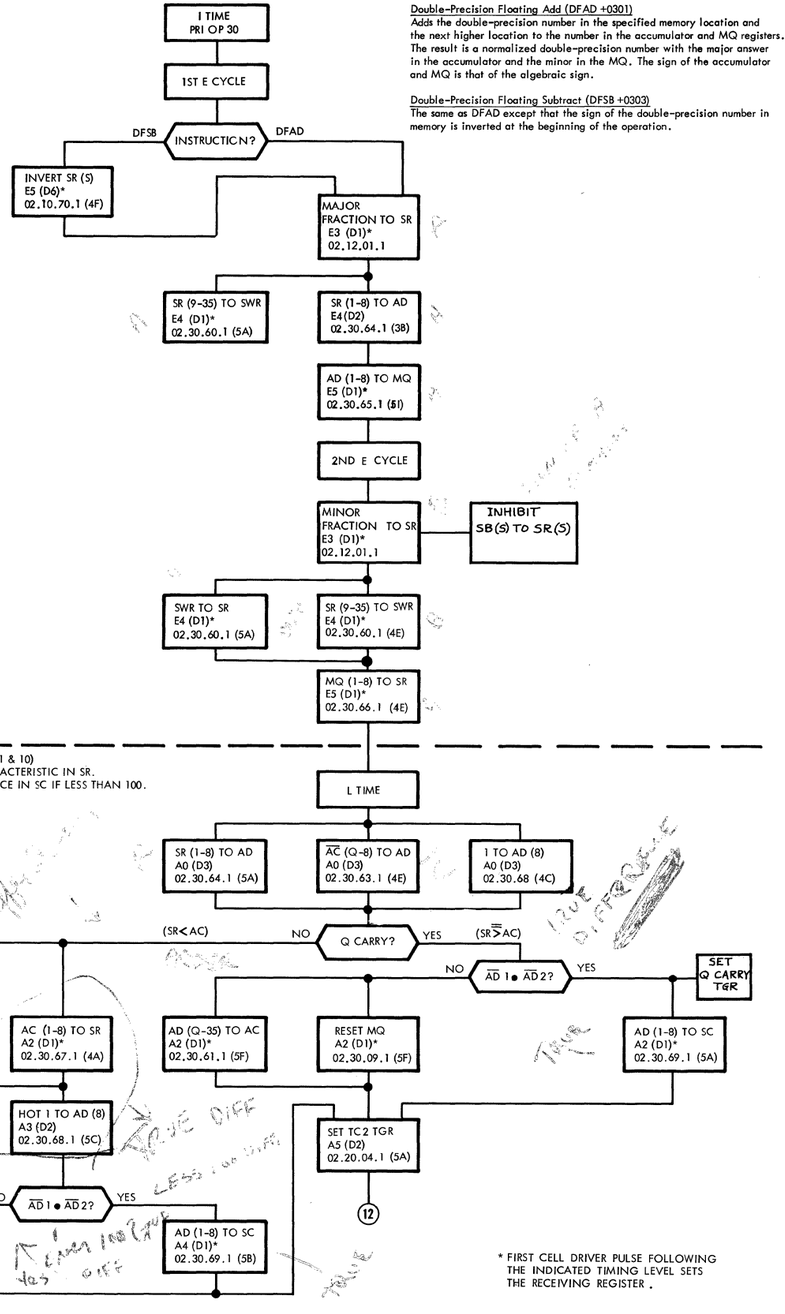
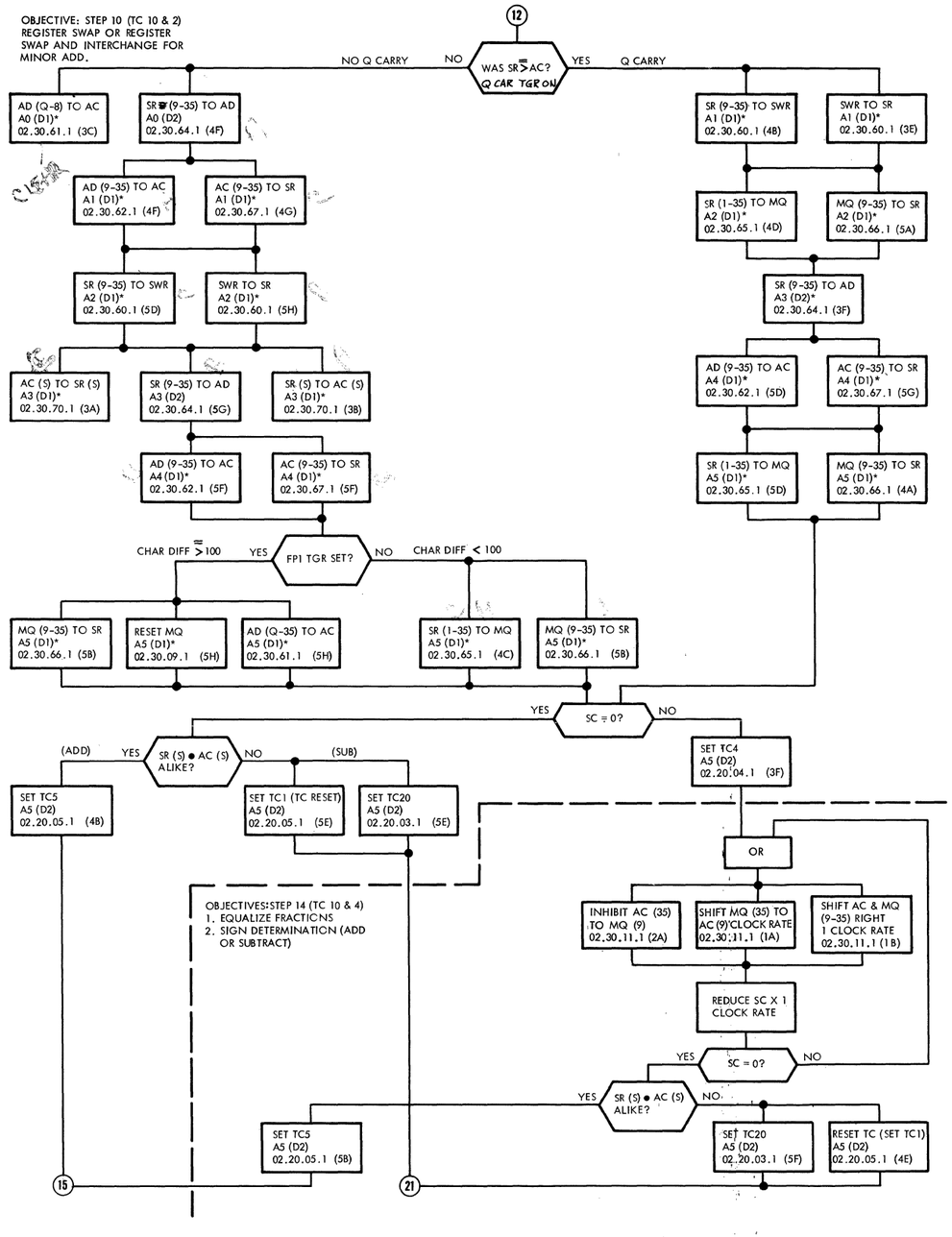
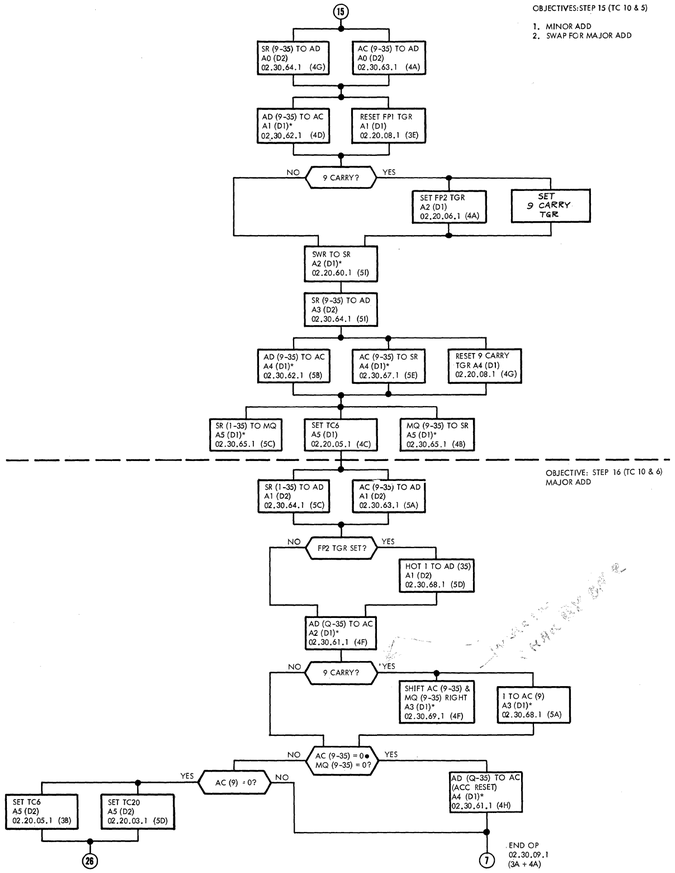
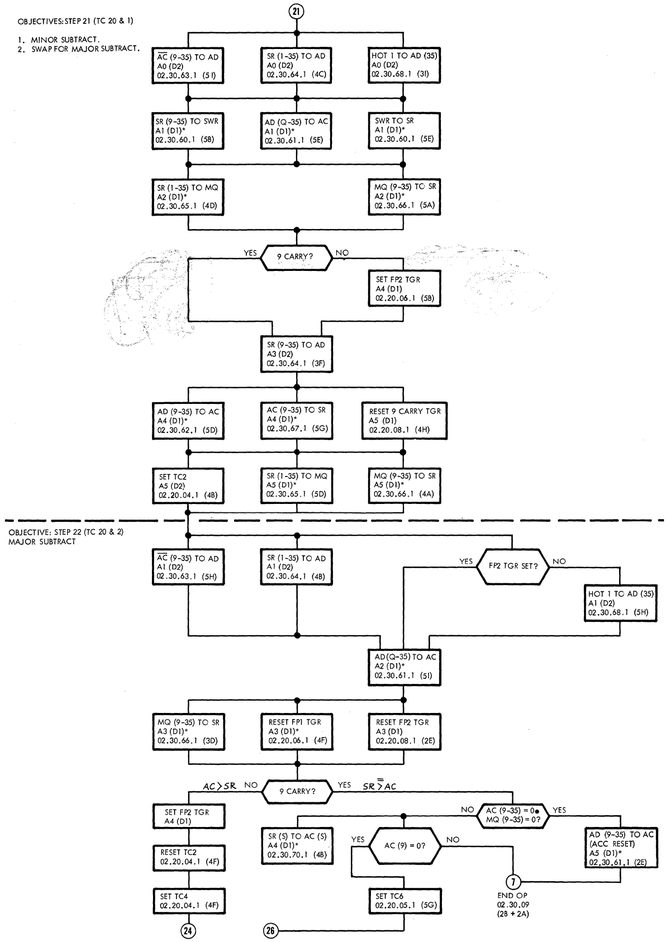
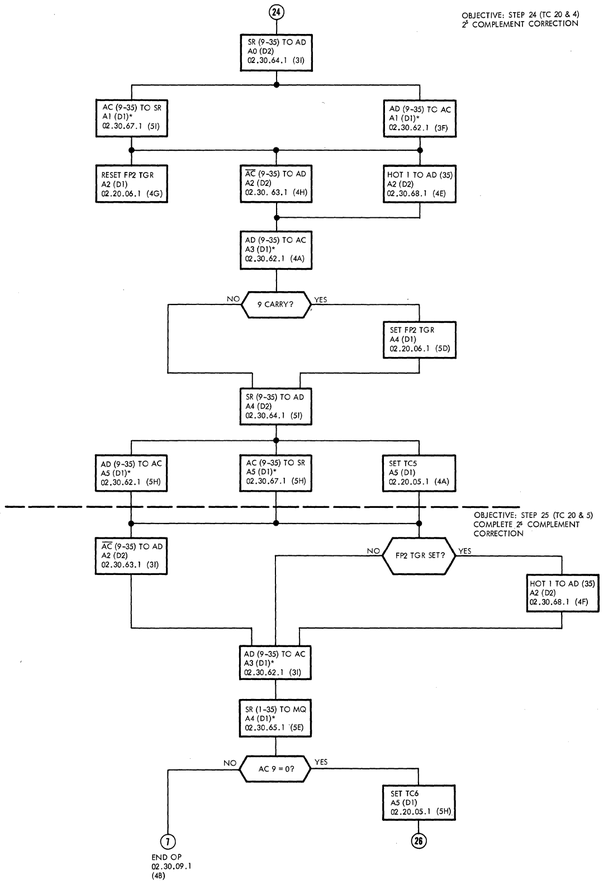


FIGURE 12. DFAD, DFSB




15
SR (9-35) TO AD
A0 (D2)
02,30,64,1 (4G)
AC (9-35) TO AD
A0 (D2)
02,30,63,1 (4A)
AD (9-35) TO AC
A1 (D1)*
02,30,62,1 (4D)
RESET FP1 TGR
A1 (D1)
02,20,08,1 (3E)
9 CARRY?
NO
YES
SET FP2 TGR
A2 (D1)
02,20,06,1 (4A)
SET
9 CARRY
TGR
SWR TO SR
A2 (D1)*
02,20,60,1 (5I)
SR (9-35) TO AD
A3 (D2)
02,30,64,1 (5I)
AD (9-35) TO AC
A4 (D1)*
02,30,62,1 (5B)
AC (9-35) TO SR
A4 (D1)*
02,30,67,1 (5E)
RESET 9 CARRY
TGR A4 (D1)
02,20,08,1 (4G)
SR (1-35) TO MQ
A5 (D1)*
02,30,65,1 (5C)
SET TC6
A5 (D1)
02,20,05,1 (4C)
MQ (9-35) TO SR
A5 (D1)*
02,30,65,1 (4B)
OBJECTIVES:STEP 15 (TC 10 & 5)
1. MINOR ADD
2. SWAP FOR MAJOR ADD
OBJECTIVE: STEP 16 (TC 10 & 6)
MAJOR ADD
SR (1-35) TO AD
A1 (D2)
02,30,64,1 (5C)
AC (9-35) TO AD
A1 (D2)
02,30,63,1 (5A)
FP2 TGR SET?
NO
YES
HOT 1 TO AD (35)
A1 (D2)
02,30,68,1 (5D)
AD (Q-35) TO AC
A2 (D1)*
02,30,61,1 (4F)
9 CARRY?
NO
YES
SHIFT AC (9-35) &
MQ (9-35) RIGHT
A3 (D1)*
02,30,69,1 (4F)
1 TO AC (9)
A3 (D1)*
02,30,68,1 (5A)
AC (9-35) = 0
MQ (9-35) = 0?
NO
YES
AC (9) < 0?
YES
NO
SET TC6
A5 (D2)
02,20,05,1 (3B)
SET TC20
A5 (D2)
02,20,03,1 (5D)
AD (Q-35) TO AC
(ACC RESET)
A4 (D1)*
02,30,61,1 (4H)
END OP
02,30,09,1
(3A + 4A)
26
7


21
AC (9-35) TO AD
A0 (D2)
02,30,63,1 (5I)
SR (1-35) TO AD
A0 (D2)
02,30,64,1 (4C)
HOT 1 TO AD (35)
A0 (D2)
02,30,68,1 (3I)
SR (9-35) TO SWR
A1 (D1)*
02,30,60,1 (5B)
AD (Q-35) TO AC
A1 (D1)*
02,30,61,1 (5E)
SWR TO SR
A1 (D1)*
02,30,60,1 (5E)
SR (1-35) TO MQ
A2 (D1)*
02,30,65,1 (4D)
MQ (9-35) TO SR
A2 (D1)*
02,30,66,1 (5A)
9 CARRY?
YES
NO
SET FP2 TGR
A4 (D1)
02,20,06,1 (5B)
SR (9-35) TO AD
A3 (D2)
02,30,64,1 (3F)
AD (9-35) TO AC
A4 (D1)*
02,30,62,1 (5D)
AC (9-35) TO SR
A4 (D1)*
02,30,67,1 (5G)
RESET 9 CARRY TGR
A5 (D1)
02,20,08,1 (4H)
SET TC2
A5 (D2)
02,20,04,1 (4B)
SR (1-35) TO MQ
A5 (D1)*
02,30,65,1 (5D)
MQ (9-35) TO SR
A5 (D1)*
02,30,66,1 (4A)
OBJECTIVES:STEP 21 (TC 20 & 1)
1. MINOR SUBTRACT.
2. SWAP FOR MAJOR SUBTRACT.
OBJECTIVE: STEP 22 (TC 20 & 2)
MAJOR SUBTRACT
AC (9-35) TO AD
A1 (D2)
02,30,63,1 (5H)
SR (1-35) TO AD
A1 (D2)
02,30,64,1 (4B)
FP2 TGR SET?
YES
NO
HOT 1 TO AD (35)
A1 (D2)
02,30,68,1 (5H)
AD (Q-35) TO AC
A2 (D1)*
02,30,61,1 (5I)
MQ (9-35) TO SR
A3 (D1)*
02,30,66,1 (3D)
RESET FP1 TGR
A3 (D1)*
02,20,06,1 (4F)
RESET FP2 TGR
A3 (D1)
02,20,08,1 (2E)
AC > SR
NO
9 CARRY?
YES
SR > AC
SET FP2 TGR
A4 (D1)
RESET TC2
02,20,04,1 (4F)
SET TC4
02,20,04,1 (4F)
SR (5) TO AC (5)
A4 (D1)*
02,30,70,1 (4B)
AC (9-35) = 0
MQ (9-35) = 0?
NO
YES
AC (9) = 0?
YES
NO
AD (9-35) TO AC
(ACC RESET)
A5 (D1)*
02,30,61,1 (2E)
SET TC6
02,20,05,1 (5G)
END OP
02,30,09
(2B + 2A)
24
26
7


24
SR (9-35) TO AD
A0 (D2)
02,30,64,1 (3I)
AC (9-35) TO SR
A1 (D1)*
02,30,67,1 (5I)
AD (9-35) TO AC
A1 (D1)*
02,30,62,1 (3F)
RESET FP2 TGR
A2 (D1)
02,20,06,1 (4G)
AC (9-35) TO AD
A2 (D2)
02,30,63,1 (4H)
HOT 1 TO AD (35)
A2 (D2)
02,30,68,1 (4E)
AD (9-35) TO AC
A3 (D1)*
02,30,62,1 (4A)
9 CARRY?
NO
YES
SET FP2 TGR
A4 (D1)
02,20,06,1 (5D)
SR (9-35) TO AD
A4 (D2)
02,30,64,1 (5I)
AD (9-35) TO AC
A5 (D1)*
02,30,62,1 (5H)
AC (9-35) TO SR
A5 (D1)*
02,30,67,1 (5H)
SET TC5
A5 (D1)
02,20,05,1 (4A)
OBJECTIVE: STEP 24 (TC 20 & 4)
2's COMPLEMENT CORRECTION
OBJECTIVE: STEP 25 (TC 20 & 5)
COMPLETE 2's COMPLEMENT
CORRECTION
AC (9-35) TO AD
A2 (D2)
02,30,63,1 (3I)
FP2 TGR SET?
NO
YES
HOT 1 TO AD (35)
A2 (D2)
02,30,68,1 (4F)
AD (9-35) TO AC
A3 (D1)*
02,30,62,1 (3I)
SR (1-35) TO MQ
A4 (D1)*
02,30,65,1 (5E)
AC 9 = 0?
NO
YES
SET TC6
A5 (D1)
02,20,05,1 (5H)
END OP
02,30,09,1
(4B)
26
7

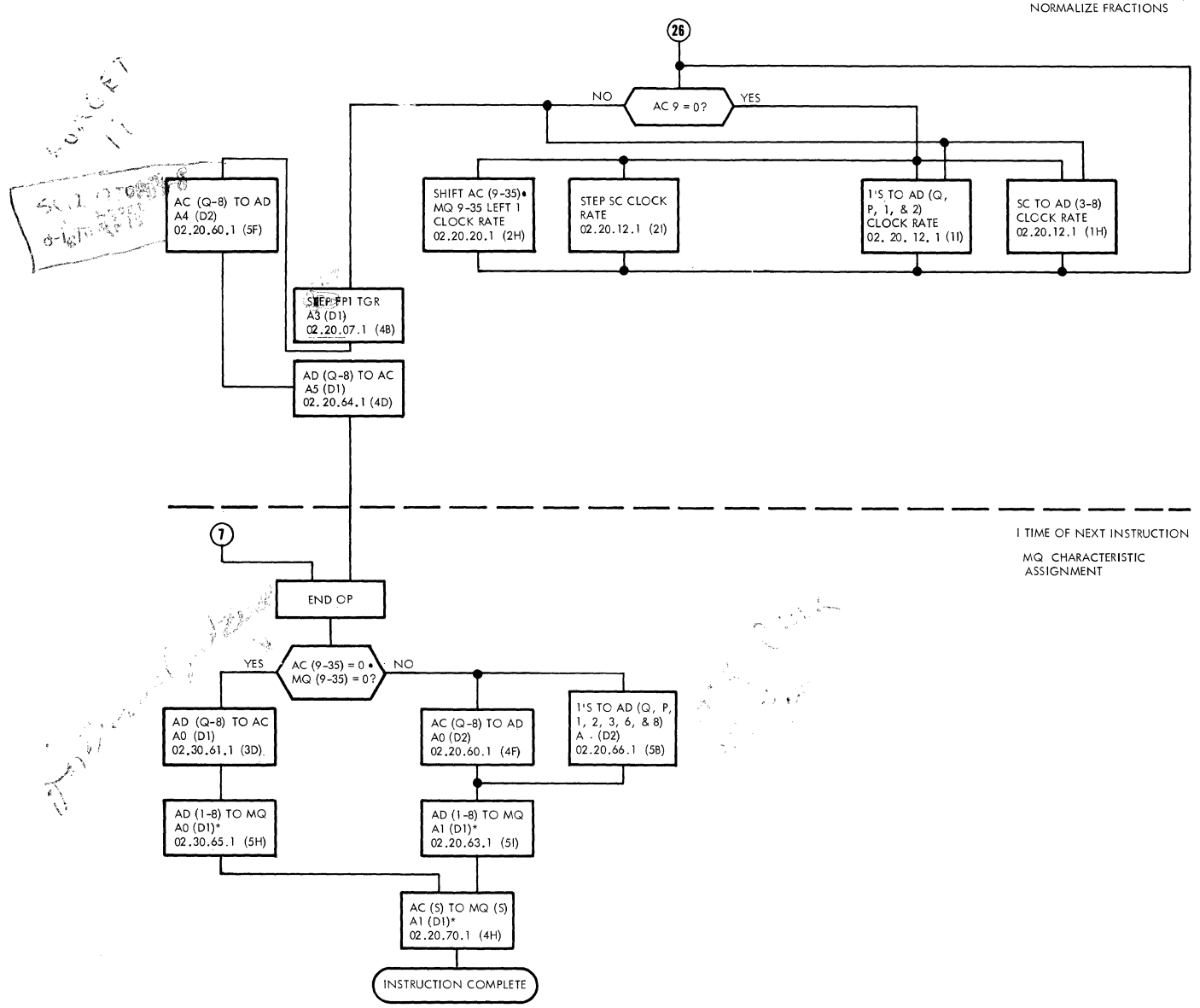
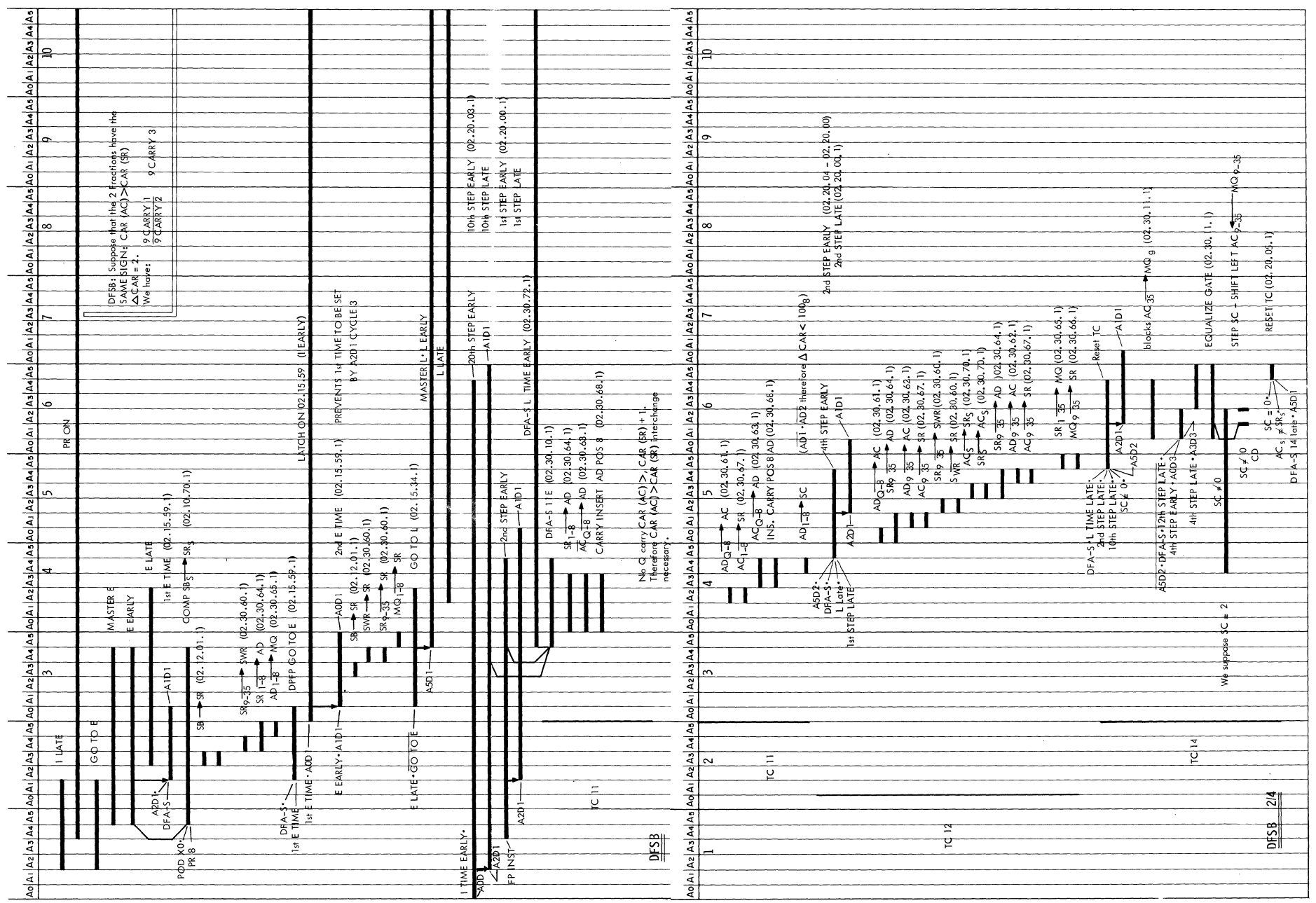
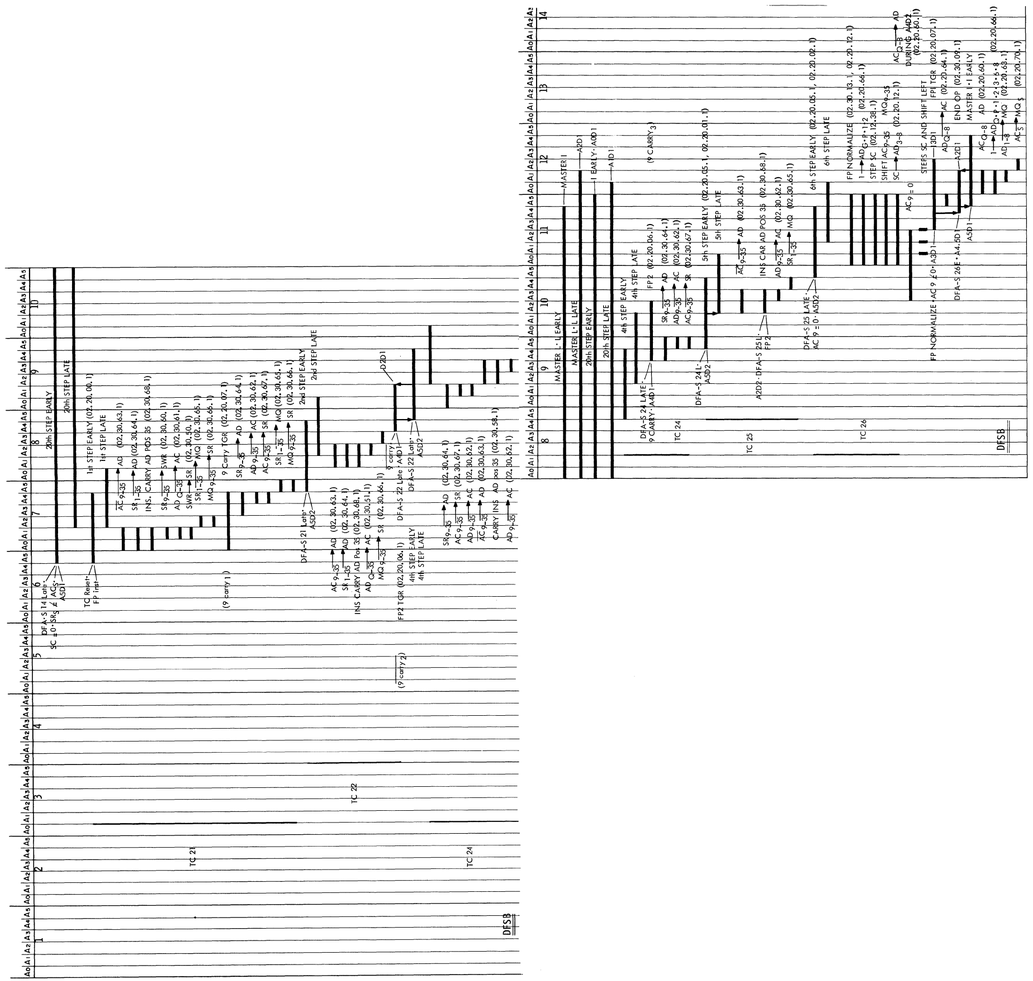


FIGURE 12. DFAD, DFSB (CONTINUED)





Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00005	056000 000005
00001	CLA		00004	050000 000004
00002	DFAD		00004	030100 000004
00003	TRA		00000	002000 000000
00004	Pattern			233012 345670
00005	Pattern			000654 321765
00006				

Double Precision Floating Add (DFAD)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR-EXT (S, 0)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	A CARRY	X CARRY	X OVERFLOW	FF1	FF2
I	F	00001	+560	000 0	00005	056000000005	000000000000	00	000000000000											
E	I	00001	+560	000 0	00001	000654321765	000000000000	00	000654321765											
I	F	00002	+500	000 0	00004	050000000004	000000000000	00	000654321765											
E	I	00002	+500	000 0	00002	233012345670	233012345670	00	000654321765											
I	E(1)	00003	+301	000 0	00004	030100000004	233012345670	00	000654321765	1 & 10										
E(1)	E(2)	00003	+301	000 0	00005	233012345670	233012345670	00	233654321765	1 & 10										
E(2)	L(1)	00003	+301	000 0	00005	233012345670	233012345670	00	233654321765	1 & 10										
L(1)	L(2)	00003	+301	000 0	00005	233012345670	233012345670	00	233654321765	2 & 10					1					
L(2)	L(3)	00003	+301	000 0	00005	233654321765	233654321765	00	233012345670	6 & 10					1					
L(3)	L(4)	00003	+301	000 0	00005	233012345670	233012345670	00	233530643752	6 & 10					1				1	
L(4)	L(5)	00003	+301	000 0	00005	233012345670	233024713561	00	233530643752	6 & 20					1				1	
L(5)	L(6)	00003	+301	374 0	00005	233012345670	233516273432	00	233615077240	6 & 20					1				1	
L(6)	I	00003	+301	374 0	00003	233012345670	227516273432	00	233615077240	6 & 20					1				1	1
I	I	00004	+020	000 0	00000	002000000000	227516273432	00	174615077240											
I	E	00001	+560	000 0	00005	056000000005	227516273432	00	174615077240											
E	I	00001	+560	000 0	00001	000654321765	227516273432	00	000654321765											
I	E	00002	+500	000 0	00004	050000000004	227516273432	00	000654321765											

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	LDQ		00004	056000 000004
00002	DFSB		00004	030300 000004
00003	TRA		00000	002000 000000
00004	Pattern			233123 456712
00005	Pattern			000543 210765
00006	Pattern			233543 210765

Double Precision Floating Subtract (DFSB)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR-EXT (S, 0)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	A CARRY	X CARRY	X OVERFLOW	FF1	FF2
I	F	00001	+500	000 0	00006	050000000006	000000000000	00	000000000000											
E	I	00001	+500	000 0	00001	233543210765	233543210765	00	000000000000											
I	E	00002	+560	000 0	00004	056000000004	233543210765	00	000000000000											
E	I	00002	+560	000 0	00002	233123456712	233543210765	00	233123456712											
I	E(1)	00003	+303	000 0	00004	030300000004	233543210765	00	233123456712	1 & 10										
E(1)	E(2)	00003	+303	000 0	00005	633123456712	233543210765	00	233123456712	1 & 10										
E(2)	L(1)	00003	+303	000 0	00005	633123456712	233543210765	00	233123456712	1 & 10										
L(1)	L(2)	00003	+303	000 0	00005	633123456712	233543210765	00	233123456712	2 & 10					1					
L(2)	L(3)	00003	+303	000 0	00005	633543210765	233123456712	00	233543210765	1 & 20					1					
L(3)	L(4)	00003	+303	000 0	00005	633123456712	233543210765	00	233417532053	2 & 20					1					
L(4)	L(5)	00003	+303	000 0	00005	633417532053	233360245725	00	233417532053	4 & 20					1				1	
L(5)	L(6)	00003	+303	000 0	00005	633360245725	233360245725	00	233417532053	5 & 20					1					
L(6)	I	00003	+303	000 0	00003	633360245725	233417532052	00	233360245725	5 & 20					1					
I	I	00004	+020	000 0	00000	002000000000	233417532052	00	200360245725											
I	E	00001	+500	000 0	00006	050000000006	233417532052	00	200360245725											
E	I	00001	+500	000 0	00001	233543210765	233543210765	00	200360245725											
I	E	00002	+560	000 0	00004	056000000004	233543210765	00	200360245725											

OBJECTIVES:(E TIME)
1. ZERO TEST MULTIPLIER
2. SAVE THE EFFECTIVE ADDRESS
3. SWAP FRACTION OF SR WITH MQ FOR 2ND E TIME
4. CHARACTER SR TO MQ

I TIME
PRI OP 26

1ST E TIME

AC (9-35) • MQ (9-35) = 0?
NO
YES

SET FPI TGR
E2 RE (D1)
02,20,08,1 (4B)

MAJOR MULTIPLICAND TO SR
E3 (D1)*
02,12,01,1

SR (9-35) TO SWR
E4 (D1)*
02,30,60,1 (5A)

SR (1-8) TO AD
E4 (D2)
02,30,64,1 (3B)

33 TO SC
E4 (D1)*
02,20,72,1 (3G)

MQ (9-35) TO SR
E5 (D1)*
02,30,66,1 (4C)

SR (5) TO MQ (5)
E5 (D1)*
02,30,70,1 (2D)

SR (1-35) TO MQ
~~SR-PRIS-CMD~~
E5 (D1)*
02,30,65,1 (5B)

AD (1-8) TO MQ
E5 (D1)*
02,30,65,1 (5I)

OBJECTIVES: (2ND E TIME)
1. ZERO TEST HIGH ORDER MULTIPLIER AND MULTIPLICAND
2. ORIGINAL FRACTION OF MQ BACK TO MQ
3. SWAP THE FRACTIONS OF THE EFFECTIVE ADDRESS AND EFFECTIVE ADDRESS + 1.
4. RESTORE SR CHARACTERISTIC
5. DETERMINE PRODUCT SIGN

2ND E TIME

AC (9-35) = 0 • MQ (9-35) = 0?
NO
YES

FPI TGR SET?
YES
NO

SR (1-35) TO MQ
E2 RE (D1)*
02,30,65,1 (5F)

SET FPI TGR
E2 RE (D1)
02,20,08,1 (2B)

MINOR MULTIPLICAND TO SR
E3 (D1)*
02,12,01,1

INHIBIT SB(S) TO SR(S)

AC (S) TO SR (S)
E4 (D1)*
02,30,70,1 (4A)

SR (9-35) TO SWR
E4 (D1)*
02,30,60,1 (5A)

SWR TO SR
E4 (D1)*
02,30,60,1 (4E)

MQ (1-8) TO SR
E5 (D1)*
02,30,66,1 (4E)

SR (S) • MQ (S) ALIKE?
NO
YES

SET AC (S) MINUS
E5 (D1)*
02,30,70,1 (4G)

SET AC (S) PLUS
E5 (D)*
02,30,70,1 (4H)

L TIME

FPI TGR SET?
NO
YES

(11)

END C P
02,30,09,1 (5D)
(7)

* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 13. DFMP

Double-Precision Floating Multiply (DFMP +0261)
Multiplies the double-precision number in the specified memory location and location plus 1 by the number in the accumulator and MQ registers. The result is a normalized double-precision number in the accumulator and MQ registers with an associated algebraic sign.

(15)

(11)

SR (9-35) TO AD
A0 (D2)
02,30,64,1 (5H)

AD (9-35) TO AC
A1 (D1)*
02,30,62,1 (4C)

AC (9-35) TO SR
A1 (D1)*
02,30,67,1 (4E)

SR (9-35) TO LR
A2 (D1)
02,30,66,1 (4F)

AC (9-35) TO SR
A3 (D1)*
02,30,67,1 (5D)

AD (9-35) TO AC
A4 (D1)* (RESET)
02,30,62,1 (5C)

MQ (9-35) = 0 ?
NO
YES

SET TC 2
A5 (D2)
02,20,04,1 (2B)

SET TC 4
A5 (D2)
02,20,04,1 (4E)

RESET TC 1
A5 (D2)
02,20,00,1 (1A)

MULTIPLY CYCLE
(AXD + BXC + AXC)

SR (9-35) TO AD MPY CYCLE

AC (9-35) TO AD MPY CYCLE

SC = 0? NOTE
YES
NO

SET FPI
A4 (D1)
02,20,08,1 (4C)

MQ (35) = 1?
YES
NO

MPY AD RT
YES
NO

SET AC & MQ
02,15,25,1

BRING UP MPY AD RT

REDUCE SC X1
02,12,38,1

SHIFT AC (9-35) o MQ (9-35) RIGHT WITH AC 35 TO MQ (9)
02,12,22,1

CONDITION AD(9-35) TO AC(10-35) and MQ 9 TRANSFER LINES

REDUCE SC X1
02,12,38,1

SHIFT AC (9-35) o MQ (9-35) RIGHT WITH AC 35 TO MQ (9)
02,12,22,1

DROP MPY AD RT

MULT AXD?
NO
YES
(STEP 12, AXD)

MULT (BXC)?
NO
YES
(FROM STEP 15, BXC)

FROM STEP 21 AXC
(21)

(18)

(14)

NOTE:
THIS BLOCK IS INTERROGATED WITH CONSECUTIVE CELL DRIVER OUTPUT PULSES BEGINNING WITH THE PULSE THAT GENERATES THE FIRST L3 LEVEL.

OBJECTIVES:STEP 11 (TC 10 & 1)
1. SWAP FRACTION OF AC AND FRACTION OF SR TO MULTIPLY.
2. SAVE FRACTION OF SR AND RESET AC IN PREPARATION TO MULTIPLY.

OBJECTIVES:STEP 14 (TC 10 & 4)
1 - SWAP FRACTION OF SR AND SWR
2 - SR TO MQ
3 - LR TO SR
4 - SWAP FRACTION OF AC AND SR
5 - SR TO LR
6 - CHARACTERISTIC OF AC AND FRACTION OF AC TO SR
7 - REGISTER SWAP IN PREPARATION FOR BXC

(14)

SWR TO SR
A0 (D1)*
02,30,60,1 (4F)

SR (9-35) TO SWR
A2 (D1)*
02,30,60,1 (4C)

SR (1-35) TO MQ
A1 (D1)*
02,30,65,1 (4F)

LR (9-35) TO SR
A1 (D1)*
02,30,66,1 (5H)

SR (9-35) TO AD
A2 (D2)
02,30,64,1 (5F)

AD (9-35) TO AC
A3 (D1)*
02,30,62,1 (4A)

AC (9-35) TO SR
A3 (D1)*
02,30,67,1 (4D)

SR (9-35) TO LR
A4 (D1)
02,30,66,1 (5F)

33 TO SC
A4 (D1)*
02,30,69,1 (3C)

AC (9-35) TO SR
A5 (D1)*
02,30,67,1 (5C)

SET TC 5
A5 (D2)
02,20,05,1 (4A)

SET FPI TGR
A5 (D1)
02,20,08,1 (2B)

AC (1-8) TO SR
A5 (D1)*
02,30,67,1 (5A)

AD (9-35) TO AC (ACC RESET)
A5 (D1)*
02,30,62,1 (4I)

OJECTIVES: STEP 15 (TC 10 & 5)
1. MULTPLY BXC
2. COMPUTE FINAL CHARACTERISTIC OF PRODUCT

SR(1-8) TO AD***
A0(D2)
02,20,64,1 (2B)

MULTIPLY CYCLE ** SAME AS STEP 12

AD(Q-8) TO AC ***
A1 (D1)*
02,20,64,1 (5G)

MQ(1-8) TO SR ** A1(D1)* ***
02,20,64,1 (3I)

SET TC 6
A5 (D2)
02,20,05,1

SR(1-8) TO AD***
A2(D2)
02,20,62,1 (5B)

AC(Q-8) TO AD***
A2(D2)
02,20,60,1 (5C)

AD (Q-8) TO AC***
A3 (D1)*
02,20,64,1 (3G)

AC(Q-8) TO AD***
A4 (D2)
02,20,60,1 (4D)

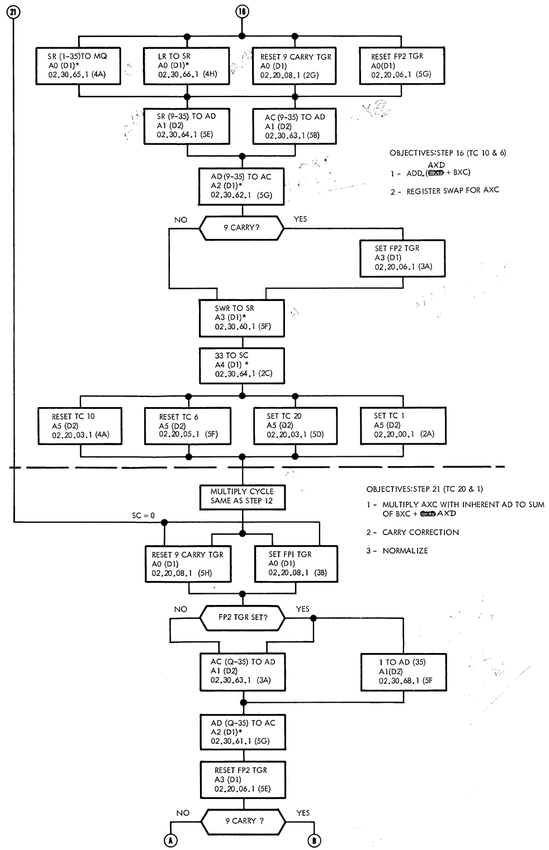
1'S TO AD (Q, P, & 1)***
A4 (D2)
02,20,66,1 (5F)

AC (Q-8) TO AC***
A5 (D1)*
02,20,64,1 (5H)

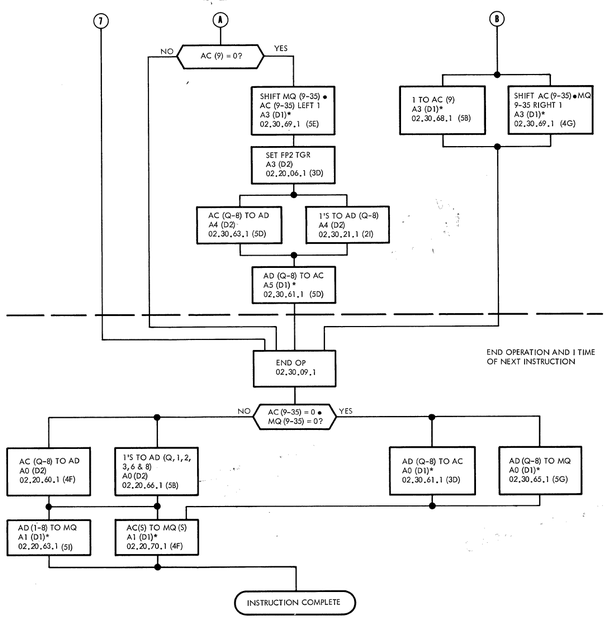
RESET FPI TGR
LT A0 (D1)
02,20,08,1 (5E)

(14)

** = SIMULTANEOUS OPERATION
*** = GATING OCCURS WITH FPI ON; IT ONLY OCCURS ONCE



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00004	050000 000004
00001	LDQ		00005	056000 000005
00002	DFMP		00004	026100 000004
00003	TRA		00000	002000 000000
00004	Pattern			211777 777777
00005	Pattern			200777 777777



Double Precision Floating Multiply (DFMP)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q) S	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP1	FP2	-
I	E	00001	+500	000	0	00004	050000000004	000000000000	00	000000000000												
E	I	00001	+500	000	0	00001	211777777777	211777777777	00	000000000000												
I	E	00002	+560	000	0	00005	056000000005	211777777777	00	000000000000												
E	I	00002	+560	000	0	00002	200777777777	211777777777	00	200777777777												
I	E (1)	00003	+261	000	0	00004	026100000004	211777777777	00	200777777777	1&10											
E (1)	E (2)	00003	+261	033	0	00005	211777777777	211777777777	00	211777777777	1&10											
E (2)	I (1)	00003	+261	033	0	00005	211777777777	211777777777	00	211777777777	1&10											
I (1)	I (2)	00003	+261	033	0	00005	211777777777	211000000000	00	211777777777	2&10											
I (2)	I (3)	00003	+261	030	0	00005	211777777777	211677777777	00	211177777777	2&10						1					
I (3)	I (4)	00003	+261	025	0	00005	211777777777	211767777777	00	211017777777	2&10						1					
I (4)	I (5)	00003	+261	022	0	00005	211777777777	211776777777	00	211001777777	2&10						1					
I (5)	I (6)	00003	+261	017	0	00005	211777777777	211777677777	00	211000177777	2&10						1					
I (6)	I (7)	00003	+261	014	0	00005	211777777777	211777767777	00	211000017777	2&10						1					
I (7)	I (8)	00003	+261	011	0	00005	211777777777	211777776777	00	211000001777	2&10						1					
I (8)	I (9)	00003	+261	006	0	00005	211777777777	211777777677	00	211000000177	2&10						1					
I (9)	I (10)	00003	+261	003	0	00005	211777777777	211777777767	00	211000000017	2&10						1					
I (10)	I (11)	00003	+261	000	0	00005	211777777777	211777777776	00	211000000001	2&10						1					
I (11)	I (12)	00003	+261	000	0	00005	211777777777	211777777776	00	211000000001	4&10						1				1	
I (12)	I (13)	00003	+261	033	0	00005	211777777777	211000000000	00	211777777777	5&10						1				1	
I (13)	I (14)	00003	+261	030	0	00005	211777777777	222677777777	00	211777777777	5&10						1					
I (14)	I (15)	00003	+261	025	0	00005	211777777777	222767777777	00	211017777777	5&10						1					
I (15)	I (16)	00003	+261	022	0	00005	211777777777	222776777777	00	211001777777	5&10						1					
I (16)	I (17)	00003	+261	017	0	00005	211777777777	222777677777	00	211000177777	5&10						1					
I (17)	I (18)	00003	+261	014	0	00005	211777777777	222777767777	00	211000017777	5&10						1					
I (18)	I (19)	00003	+261	011	0	00005	211777777777	222777776777	00	211000001777	5&10						1					
I (19)	I (20)	00003	+261	006	0	00005	211777777777	222777777677	00	211000000177	5&10						1					
I (20)	I (21)	00003	+261	003	0	00005	211777777777	222777777767	00	211000000017	5&10						1					
I (21)	I (22)	00003	+261	000	0	00005	211777777777	222777777776	00	211000000001	5&10						1					
I (22)	I (23)	00003	+261	000	0	00005	211777777777	222777777776	00	211000000001	6&10						1				1	
I (23)	I (24)	00003	+261	033	0	00005	211777777777	222777777774	00	211777777777	1&20						1				1	
I (24)	I (25)	00003	+261	030	0	00005	211777777777	222777777776	00	211577777777	1&20						1				1	
I (25)	I (26)	00003	+261	025	0	00005	211777777777	222777777776	00	211757777777	1&20						1				1	
I (26)	I (27)	00003	+261	022	0	00005	211777777777	222777777776	00	211775777777	1&20						1				1	
I (27)	I (28)	00003	+261	017	0	00005	211777777777	222777777776	00	211777577777	1&20						1				1	
I (28)	I (29)	00003	+261	014	0	00005	211777777777	222777777776	00	211777757777	1&20						1				1	
I (29)	I (30)	00003	+261	011	0	00005	211777777777	222777777776	00	211777775777	1&20						1				1	
I (30)	I (31)	00003	+261	006	0	00005	211777777777	222777777776	00	211777777577	1&20						1				1	
I (31)	I (32)	00003	+261	003	0	00005	211777777777	222777777776	00	211777777757	1&20						1				1	
I (32)	I (33)	00003	+261	000	0	00005	211777777777	222777777776	00	211777777775	1&20						1				1	
I (33)	I	00003	+261	000	0	00003	211777777777	222777777776	00	211777777775	1&20						0			0	1	
I	I	00004	+020	000	0	00000	002000000000	222777777777	00	167777777775												
I	E	00001	+500	000	0	00004	050000000004	222777777777	00	167777777775												
E	I	00001	+500	000	0	00001	211777777777	211777777777	00	167777777775												
I	E	00002	+560	000	0	00005	056000000005	211777777777	00	167777777775												
E	I	00002	+560	000	0	00002	200777777777	211777777777	00	200777777777												

FIGURE 13. DFMP (CONTINUED)

MULTIPLICATION
7
8
9
10
11
12
13
14
5th STEP EARLY (02.20.05.1)
DFMP 14L·A5D2
5th STEP EARLY
5th STEP LATE
FP1·5th St Early·10th St Early·DFMP L early
DFMP 15 FPI
DFMP 15L FPI
DFMP 15 FPI·A0D2
SR 1-8 → AD (02.30.64.1)
DFMP 15 FPI·A1D1
AD Q-8 → AC (02.30.61.1)
FMP 1E·A1D1·
MQ 1-8 → SR (02.20.64.1)
FMP 1E·A2D2·
SR 1-8 → AD (02.20.62.1)
FMP 1E·A2D2
AC Q-8 → AD (02.20.60.1)
FMP 1E·A3D1
AD Q-8 → AC (02.20.64.1)
FMP 1L·A4D2
AC Q-8 → AD
FMP 1L·A4D2
1 AD Q·P·1
FMP 1L·A5D1
AD Q-8 → AC
DFMP 15E·SC ≠ 0·DFMP 15L
DFMP 15L·A4D1·SC = 0·DFMP 15L·A5D2
DFMP 16E·A0D1
FP2 TGR (06.20.06.1)
6th STEP EARLY
6th STEP LATE
DFMP 16E·A0D1
SR 1-35 → MQ (02.30.65.1)
DFMP 16E·A0D1
LR → SR (02.30.66.1)
DFMP 16E·A0D1
RESET 9 CAR Tgr (02.20.08.1)
DFMP 16E·A1D2
SR 9-35 → AD (02.30.64.1)
AC 9-35 → AD (02.30.63.1)
DFMP 16E·A2D1
AD 9-35 → AC (02.30.62.1)
DFMP 16L·9 CARRY·A3D1
FP2 TGR (02.20.06.1)
DFMP 16L·A3D1
SWR → SR (02.30.60.1)
DFMP 16L·A4D1
33 → SC (02.30.69.1)
DFMP 16L·A5D1
TC RESET (02.20.05.1)
DFMP 16L·A5D1
20th STEP EARLY (02.20.03.1)
1 early·A0D1
TC RESET
1st STEP EARLY (02.20.00.1)
DFMP 21E·SC ≠ 0·DFMP 21L
FP MPY EARLY (02.30.21.1) (02.20.20.1)
FP MPY LATE (02.30.21.1) (02.20.20.1)
MULTIPLICATION π1 + π2 + (MDCS X MROS)
SC = 0·DFMP 21E·A0D1
FPI (02.20.08.1)
1 early·A3D1
DFMP 21E·
RESET 9 CA TGR (02.20.08.1)
DFMP 21L·FP1·FP2·A1D2
CI AD PCS 35 (02.30.68.1)
DFMP 21
DFMP 21E·FP1·A1D2
AC Q-35 → AD (02.30.63.1)
A2D1·DFMP 21E·FP1
AD Q-35 → AC (02.30.61.1)
DFMP 21E·FP1·9 CARRY·A3D1
1 → AC9 (02.30.68.1)
9 CARRY
Shift Right 1 AC 9-35 → MQ 9-35
DFMP 21E·FP1·9 CARRY·AC 9·A3D1
Shift Left 1 AC 9-35 ← MQ 9-35
9 CARRY·AC9 = 0
DFMP 21E·FP1·AC 9·9 CARRY·A3D2
FP2
1 EARLY·A3D2
(02.20.06.1)
AC Q-8 → AD (02.30.63.1)
DFMP 21·FP1·2·A4D2
1 → AD Q-8 (02.30.21.1)
DFMP 21·FP1·2·A5D1
AD Q-8 → AC (02.30.61.1)
FPI TGR·DFMP 21 FP1
FP END OP (02.30.09.1)
END OP TGR
MASTER 1
1 EARLY·DPFP·(AC 9-35 = 0)·(MQ 9-35 = 0)
DPFP 1 GATE (02.15.59.1)
(AC 9-35 = 0)·(MQ 9-35 = 0)
A0D1
AD Q-8 → AC (02.30.61.1)
AD Q-8 → MQ (02.30.61.1)
Cycle 1
DFMP (AC 9-35 ≠ 0)·1 Early
1 GATE (02.20.12.1)
(AC 9-35 ≠ 0)∠(MQ 9-35 ≠ 0)
A0D1
AC (Q-8) → AD (02.20.60.1)
1 GATE·A0D2
1 AD Q12368 (02.20.66.1)
1 GATE·A1D1
AD 1-8 → MQ (02.20.63.1)
FP·1 Early·A2D1
AC 5 → MQ 5 (02.20.70.1)

Double-Precision Floating Divide or Proceed (DFPD -0241)
Divides the double-precision number in the accumulator and MQ (dividend) by the double-precision number in the specified memory location and location plus 1 (divisor). The result is a double quotient in the accumulator and MQ registers with an associated algebraic sign.

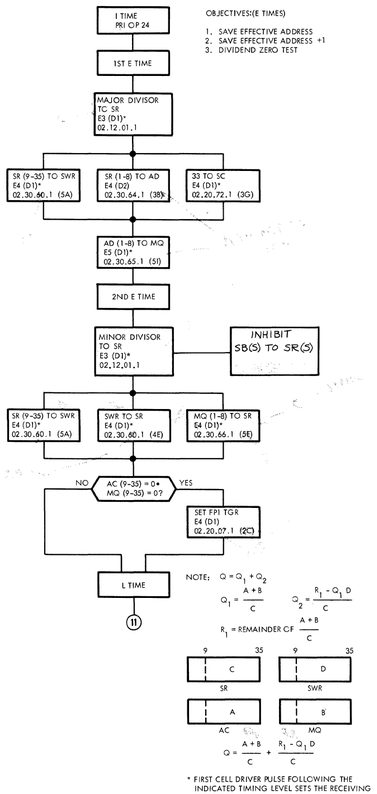
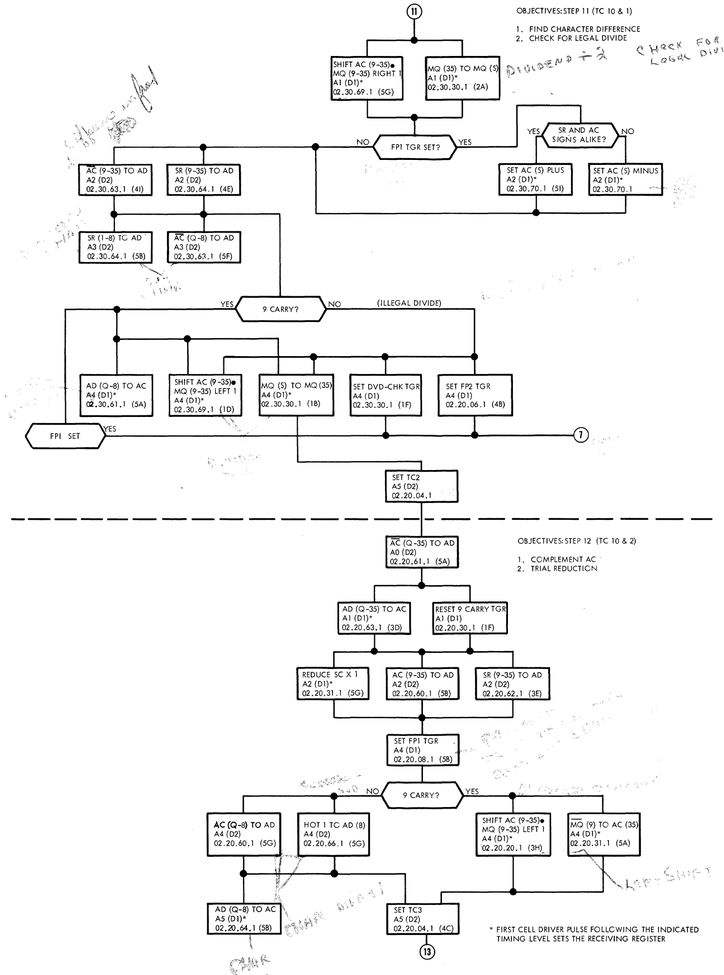
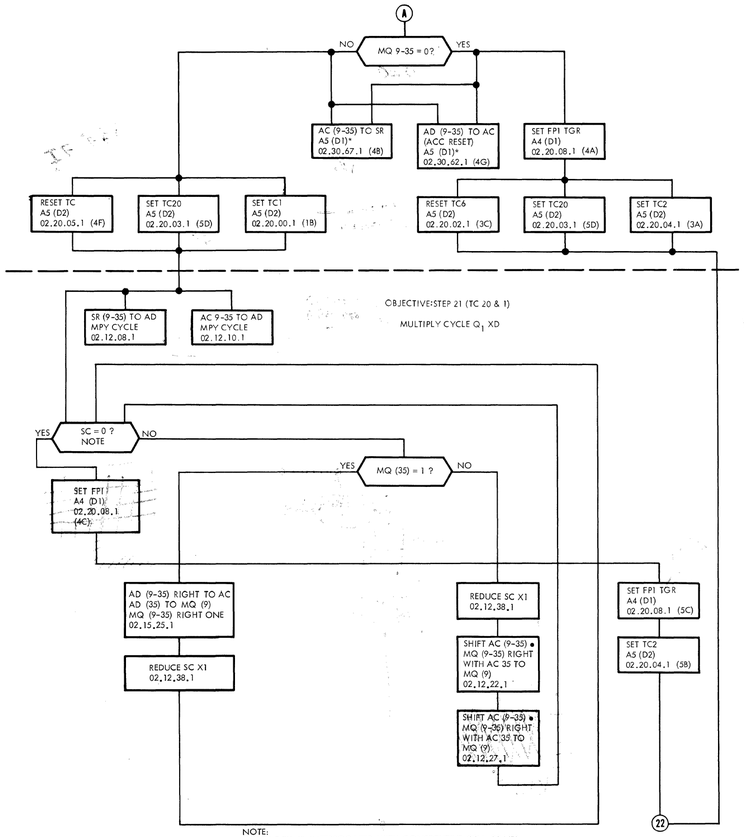
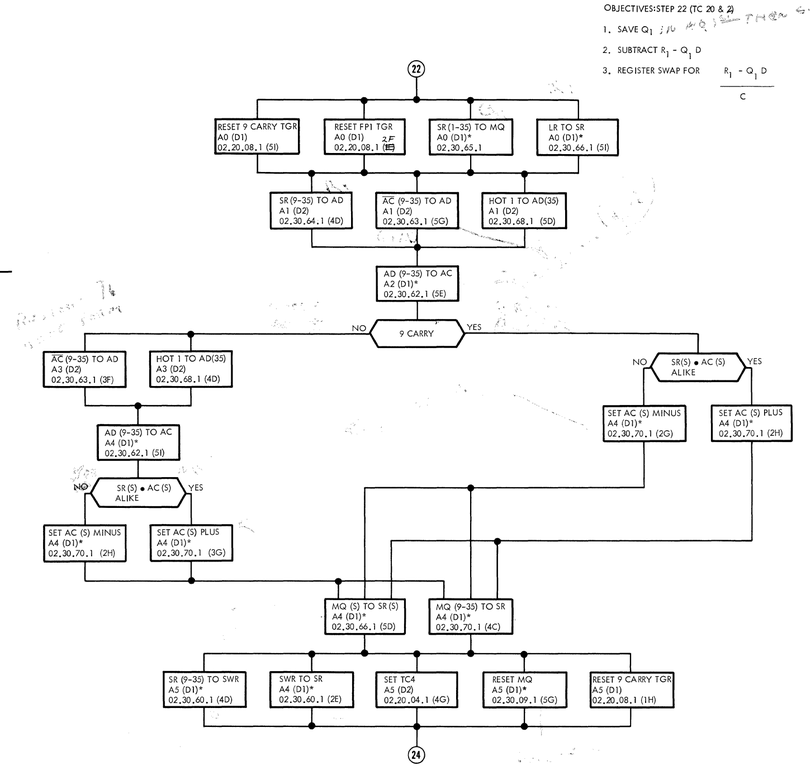
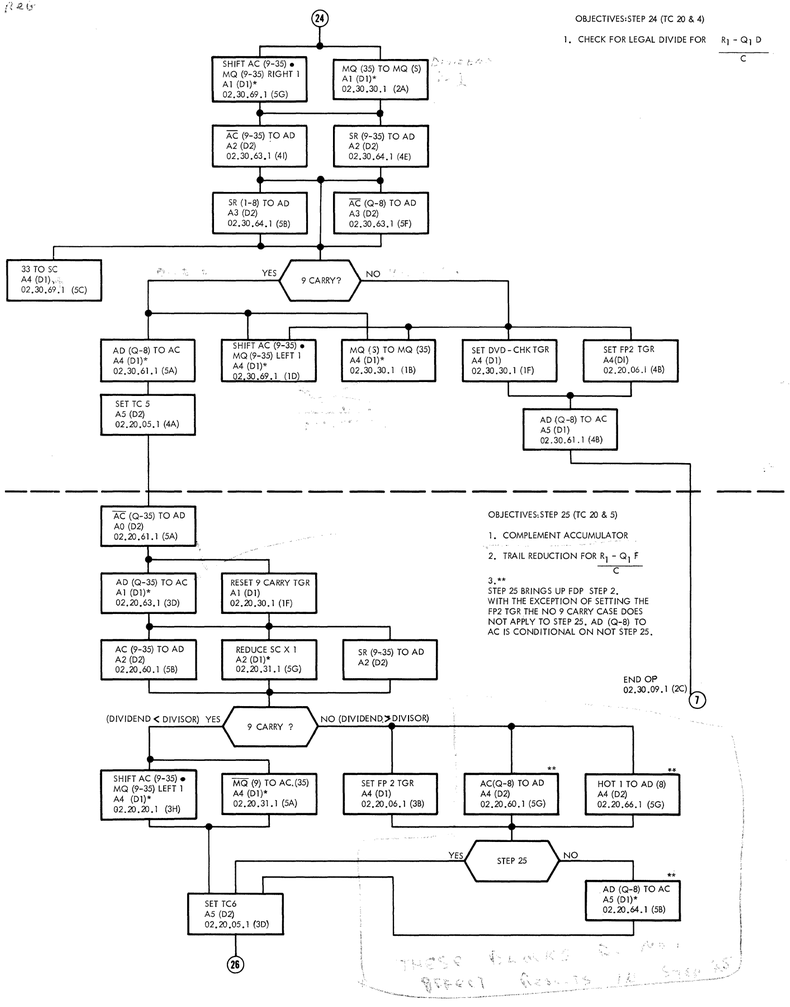


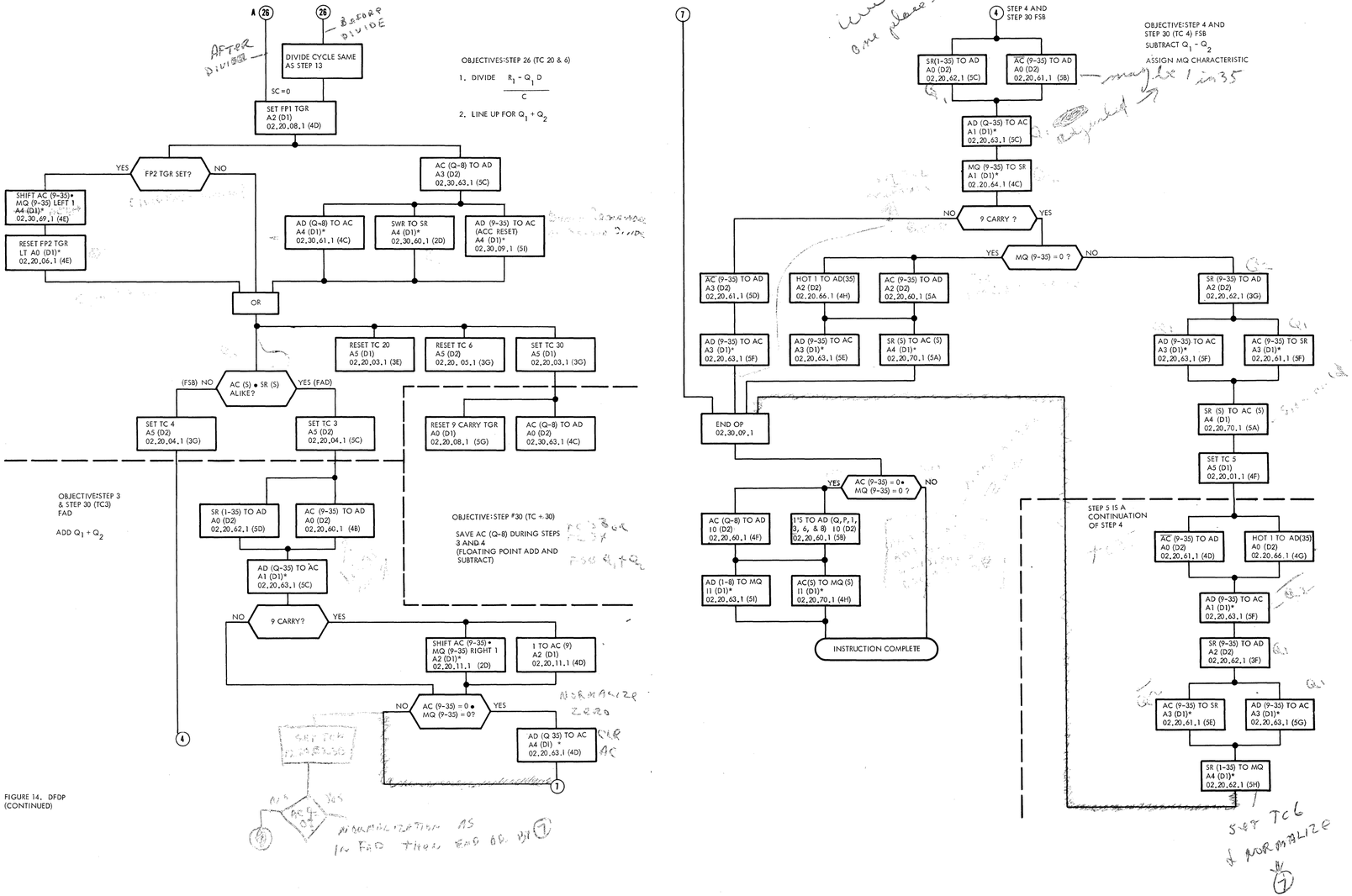
FIGURE 14. DFDP




A
MQ 9-35 = 0?
NO
YES
AC (9-35) TO SR
A5 (D1)*
02,30,67,1 (4B)
AD (9-35) TO AC
(ACC RESET)
A5 (D1)*
02,30,62,1 (4G)
SET FP1 TGR
A4 (D1)
02,20,08,1 (4A)
RESET TC
A5 (D2)
02,20,03,1 (4F)
SET TC20
A5 (D2)
02,20,03,1 (5D)
SET TC1
A5 (D2)
02,20,00,1 (1B)
RESET TC6
A5 (D2)
02,20,02,1 (3C)
SET TC20
A5 (D2)
02,20,03,1 (5D)
SET TC2
A5 (D2)
02,20,04,1 (3A)
SR (9-35) TO AD
MPY CYCLE
02,12,08,1
AC 9-35 TO AD
MPY CYCLE
02,12,10,1
OBJECTIVE:STEP 21 (TC 20 & 1)
MULTIPLY CYCLE Q1 XD
YES
SC = 0 ?
NOTE
NO
SET FP1
A4 (D1)
02,20,08,1
(4C)
YES
MQ (35) = 1 ?
NO
AD (9-35) RIGHT TO AC
AD (35) TO MQ (9)
MQ (9-35) RIGHT ONE
02,15,25,1
REDUCE SC X1
02,12,38,1
REDUCE SC X1
02,12,38,1
SHIFT AC (9-35) •
MQ (9-35) RIGHT
WITH AC 35 TO
MQ (9)
02,12,22,1
SHIFT AC (9-35) •
MQ (9-35) RIGHT
WITH AC 35 TO
MQ (9)
02,12,27,1
SET FP1 TGR
A4 (D1)
02,20,08,1 (5C)
SET TC2
A5 (D2)
02,20,04,1 (5B)
22
NOTE:
THIS BLOCK IS INTERROGATED WITH CONSECUTIVE CELL DRIVER
OUTPUT PULSES BEGINNING WITH THE PULSE THAT GENERATES
THE FIRST L3 LEVEL


OBJECTIVES:STEP 22 (TC 20 & 2)
1. SAVE Q1
2. SUBTRACT R1 - Q1 D
3. REGISTER SWAP FOR R1 - Q1 D / C
22
RESET 9 CARRY TGR
A0 (D1)
02,20,08,1 (5I)
RESET FP1 TGR
A0 (D1)
02,20,08,1 (1E)
SR(1-35) TO MQ
A0 (D1)*
02,30,65,1
LR TO SR
A0 (D1)*
02,30,66,1 (5I)
SR (9-35) TO AD
A1 (D2)
02,30,64,1 (4D)
AC (9-35) TO AD
A1 (D2)
02,30,63,1 (5G)
HOT 1 TO AD(35)
A1 (D2)
02,30,68,1 (5D)
AD (9-35) TO AC
A2 (D1)*
02,30,62,1 (5E)
NO
9 CARRY
YES
AC (9-35) TO AD
A3 (D2)
02,30,63,1 (3F)
HOT 1 TO AD(35)
A3 (D2)
02,30,68,1 (4D)
NO
SR(S) • AC (S)
ALIKE
YES
SET AC (S) MINUS
A4 (D1)*
02,30,70,1 (2G)
SET AC (S) PLUS
A4 (D1)*
02,30,70,1 (2H)
AD (9-35) TO AC
A4 (D1)*
02,30,62,1 (5I)
NO
SR(S) • AC (S)
ALIKE
YES
SET AC (S) MINUS
A4 (D1)*
02,30,70,1 (2H)
SET AC (S) PLUS
A4 (D1)*
02,30,70,1 (3G)
MQ (S) TO SR (S)
A4 (D1)*
02,30,66,1 (5D)
MQ (9-35) TO SR
A4 (D1)*
02,30,70,1 (4C)
SR (9-35) TO SWR
A5 (D1)*
02,30,60,1 (4D)
SWR TO SR
A4 (D1)*
02,30,60,1 (2E)
SET TC4
A5 (D2)
02,20,04,1 (4G)
RESET MQ
A5 (D1)*
02,30,09,1 (5G)
RESET 9 CARRY TGR
A5 (D1)
02,20,08,1 (1H)
24


24
OBJECTIVES:STEP 24 (TC 20 & 4)
1. CHECK FOR LEGAL DIVIDE FOR R1 - Q1 D / C
SHIFT AC (9-35) •
MQ (9-35) RIGHT 1
A1 (D1)*
02,30,69,1 (5G)
MQ (35) TO MQ (S)
A1 (D1)*
02,30,30,1 (2A)
AC (9-35) TO AD
A2 (D2)
02,30,63,1 (4I)
SR (9-35) TO AD
A2 (D2)
02,30,64,1 (4E)
SR (1-8) TO AD
A3 (D2)
02,30,64,1 (5B)
AC (Q-8) TO AD
A3 (D2)
02,30,63,1 (5F)
33 TO SC
A4 (D1)
02,30,69,1 (5C)
YES
9 CARRY?
NO
AD (Q-8) TO AC
A4 (D1)*
02,30,61,1 (5A)
SHIFT AC (9-35) •
MQ (9-35) LEFT 1
A4 (D1)*
02,30,69,1 (1D)
MQ (S) TO MQ (35)
A4 (D1)*
02,30,30,1 (1B)
SET DVD - CHK TGR
A4 (D1)
02,30,30,1 (1F)
SET FP2 TGR
A4(D1)
02,20,06,1 (4B)
SET TC 5
A5 (D2)
02,20,05,1 (4A)
AD (Q-8) TO AC
A5 (D1)
02,30,61,1 (4B)
AC (Q-35) TO AD
A0 (D2)
02,20,61,1 (5A)
OBJECTIVES:STEP 25 (TC 20 & 5)
1. COMPLEMENT ACCUMULATOR
2. TRAIL REDUCTION FOR R1 - Q1 F / C
3.**
STEP 25 BRINGS UP FDP STEP 2,
WITH THE EXCEPTION OF SETTING THE
FP2 TGR THE NO 9 CARRY CASE DOES
NOT APPLY TO STEP 25, AD (Q-8) TO
AC IS CONDITIONAL ON NOT STEP 25.
AD (Q-35) TO AC
A1 (D1)*
02,20,63,1 (3D)
RESET 9 CARRY TGR
A1 (D1)
02,20,30,1 (1F)
AC (9-35) TO AD
A2 (D2)
02,20,60,1 (5B)
REDUCE SC X 1
A2 (D1)*
02,20,31,1 (5G)
SR (9-35) TO AD
A2 (D2)
END OP
02,30,09,1 (2C)
7
(DIVIDEND < DIVISOR) YES
9 CARRY ?
NO (DIVIDEND ≥ DIVISOR)
SHIFT AC (9-35) •
MQ (9-35) LEFT 1
A4 (D1)*
02,20,20,1 (3H)
MQ (9) TO AC (35)
A4 (D1)*
02,20,31,1 (5A)
SET FP 2 TGR
A4 (D1)
02,20,06,1 (3B)
AC(Q-8) TO AD
A4 (D2)
02,20,60,1 (5G)
**
HOT 1 TO AD (8)
A4 (D2)
02,20,66,1 (5G)
**
YES
STEP 25
NO
AD (Q-8) TO AC
A5 (D1)*
02,20,64,1 (5B)
**
SET TC6
A5 (D2)
02,20,05,1 (3D)
26


A 26
26
DIVIDE CYCLE SAME AS STEP 13
SC = 0
SET FP1 TGR
A2 (D1)
02,20,08,1 (4D)
FP2 TGR SET?
YES
NO
SHIFT AC (9-35)* MQ (9-35) LEFT 1
A4 (D1)*
02,30,69,1 (4E)
RESET FP2 TGR
LT A0 (D1)*
02,20,06,1 (4E)
AC (Q-8) TO AD
A3 (D2)
02,30,63,1 (5C)
AD (Q-8) TO AC
A4 (D1)*
02,30,61,1 (4C)
SWR TO SR
A4 (D1)*
02,30,60,1 (2D)
AD (9-35) TO AC (ACC RESET)
A4 (D1)*
02,30,09,1 (5I)
OR
RESET TC 20
A5 (D1)
02,20,03,1 (3E)
RESET TC 6
A5 (D2)
02,20, 05,1 (3G)
SET TC 30
A5 (D1)
02,20,03,1 (3G)
(FSB) NO
AC (S) • SR (S) ALIKE?
YES (FAD)
SET TC 4
A5 (D2)
02,20,04,1 (3G)
SET TC 3
A5 (D2)
02,20,04,1 (5C)
RESET 9 CARRY TGR
A0 (D1)
02,20,08,1 (5G)
AC (Q-8) TO AD
A0 (D2)
02,30,63,1 (4C)
OBJECTIVE:STEP 3 & STEP 30 (TC3) FAD
ADD $Q_1 + Q_2$
SR (1-35) TO AD
A0 (D2)
02,20,62,1 (5D)
AC (9-35) TO AD
A0 (D2)
02,20,60,1 (4B)
AD (Q-35) TO AC
A1 (D1)*
02,20,63,1 (5C)
NO
9 CARRY?
YES
SHIFT AC (9-35)* MQ (9-35) RIGHT 1
A2 (D1)*
02,20,11,1 (2D)
1 TO AC (9)
A2 (D1)
02,20,11,1 (4D)
NO
AC (9-35) = 0 • MQ (9-35) = 0?
YES
AD (Q 35) TO AC
A4 (D1) *
02,20,63,1 (4D)
4
7
OBJECTIVE:STEP 26 (TC 20 & 6)
1. DIVIDE $\frac{R_1 - Q_1 D}{C}$
2. LINE UP FOR $Q_1 + Q_2$
OBJECTIVE:STEP #30 (TC + 30)
SAVE AC (Q-8) DURING STEPS 3 AND 4 (FLOATING POINT ADD AND SUBTRACT)
FIGURE 14. DFDP (CONTINUED)
STEP 4 AND STEP 30 FSB
SR(1-35) TO AD
A0 (D2)
02,20,62,1 (5C)
AC (9-35) TO AD
A0 (D2)
02,20,61,1 (5B)
AD (Q-35) TO AC
A1 (D1)*
02,20,63,1 (5C)
MQ (9-35) TO SR
A1 (D1)*
02,20,64,1 (4C)
NO
9 CARRY ?
YES
YES
MQ (9-35) = 0 ?
NO
AC (9-35) TO AD
A3 (D2)
02,20,61,1 (5D)
HOT 1 TO AD(35)
A2 (D2)
02,20,66,1 (4H)
AC (9-35) TO AD
A2 (D2)
02,20,60,1 (5A
SR (9-35) TO AD
A2 (D2)
02,20,62,1 (3G)
AD (9-35) TO AC
A3 (D1)*
02,20,63,1 (5F)
AD (9-35) TO AC
A3 (D1)*
02,20,63,1 (5E)
SR (S) TO AC (S)
A4 (D1)*
02,20,70,1 (5A)
AD (9-35) TO AC
A3 (D1)*
02,20,63,1 (5F)
AC (9-35) TO SR
A3 (D1)*
02,20,61,1 (5F)
END OP
02,30,09,1
SR (S) TO AC (S)
A4 (D1)
02,20,70,1 (5A)
SET TC 5
A5 (D1)
02,20,01,1 (4F)
YES
AC (9-35) = 0 • MQ (9-35) = 0 ?
NO
AC (Q-8) TO AD
10 (D2)
02,20,60,1 (4F)
1'S TO AD (Q, P, 1, 3, 6, & 8) 10 (D2)
02,20,60,1 (5B)
AD (1-8) TO MQ
11 (D1)*
02,20,63,1 (5I)
AC(S) TO MQ(S)
11 (D1)*
02,20,70,1 (4H)
INSTRUCTION COMPLETE
STEP 5 IS A CONTINUATION OF STEP 4
AC (9-35) TO AD
A0 (D2)
02,20,61,1 (4D)
HOT 1 TO AD(35)
A0 (D2)
02,20,66,1 (4G)
AD (9-35) TO AC
A1 (D1)*
02,20,63,1 (5F)
SR (9-35) TO AD
A2 (D2)
02,20,62,1 (3F)
AC (9-35) TO SR
A3 (D1)*
02,20,61,1 (5E)
AD (9-35) TO AC
A3 (D1)*
02,20,63,1 (5G)
SR (1-35) TO MQ
A4 (D1)*
02,20,62,1 (5H)
OBJECTIVE:STEP 4 AND STEP 30 (TC 4) FSB
SUBTRACT $Q_1 - Q_2$
ASSIGN MQ CHARACTERISTIC

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	LDQ		00006	056000 000006
00002	DFDP		00004	424100 000004
00003	TRA		00000	002000 000000
00004	Pattern			176777 777777
00005	Pattern			173777 777777
00006	Pattern			173777 777776

Double Precision Divide and Proceed (DFDP)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	173777777777	173777777777	00	000000000000											
I	E	00002	+560	000	0	00006	056000000006	173777777777	00	000000000000											
E	I	00002	+560	000	0	00002	173777777776	173777777777	00	173777777776											
I	E(1)	00003	-241	000	0	00004	424100000004	173777777777	00	173777777776	1 & 10										
E(1)	E(2)	00003	-241	033	0	00005	176777777777	173777777777	00	176777777776	1 & 10										
E(2)	L(1)	00003	-241	033	0	00005	176777777777	173777777777	00	176777777776	1&10										
L(1)	L(2)	00003	-241	033	0	00005	176777777777	002777777777	00	176777777776	2 & 10						1				
L(2)	L(3)	00003	-241	032	0	00005	176777777777	376000000000	11	176777777776	3 & 10						0				1
L(3)	L(4)	00003	-241	030	0	00005	000777777777	176777777774	00	000777777774	3 & 10						1	1			
L(4)	L(5)	00003	-241	026	0	00005	000777777777	176777777760	00	000777777760	3 & 10						1	1			
L(5)	L(6)	00003	-241	024	0	00005	000777777777	176777777700	00	000777777700	3 & 10						1	1			
L(6)	L(7)	00003	-241	022	0	00005	000777777777	176777777400	00	000777777400	3 & 10						1	1			
L(7)	L(8)	00003	-241	020	0	00005	000777777777	176777776000	00	000777776000	3 & 10						1	1			
L(8)	L(9)	00003	-241	016	0	00005	000777777777	176777770000	00	000777770000	3 & 10						1	1			
L(9)	L(10)	00003	-241	014	0	00005	000777777777	176777740000	00	000777740000	3 & 10						1	1			
L(10)	L(11)	00003	-241	012	0	00005	000777777777	176777600000	00	000777600000	3 & 10						1	1			
L(11)	L(12)	00003	-241	010	0	00005	000777777777	176777000000	00	000777000000	3& 10						1	1			
L(12)	L(13)	00003	-241	006	0	00005	000777777777	176774000000	00	000774000000	3 & 10						1	1			
L(13)	L(14)	00003	-241	004	0	00005	000777777777	176760000000	00	000760000000	3 & 10						1	1			
L(14)	L(15)	00003	-241	002	0	00005	000777777777	176700000000	00	000700000000	3 & 10						1	1			
L(15)	L(16)	00003	-241	000	0	00005	000777777777	176400000000	00	000400000000	3 & 10						1	1			
L(16)	L(17)	00003	-241	000	0	00005	000777777777	176400000000	00	000400000000	6 & 10						1	1	1		
L(17)	L(18)	00003	-241	033	0	00005	000400000000	176000000000	00	000777777777	1 & 20						1				
L(18)	L(19)	00003	-241	030	0	00005	000400000000	176340000000	00	000077777777	1 & 20						1				
L(19)	L(20)	00003	-241	025	0	00005	000400000000	176374000000	00	000007777777	1 & 20						1				
L(20)	L(21)	00003	-241	022	0	00005	000400000000	176377400000	00	000000777777	1 & 20						1				
L(21)	L(22)	00003	-241	017	0	00005	000400000000	176377740000	00	000000077777	1 & 20						1				
L(22)	L(23)	00003	-241	014	0	00005	000400000000	176377774000	00	000000007777	1 & 20						1				
L(23)	L(24)	00003	-241	011	0	00005	000400000000	176377777400	00	000000000777	1 & 20						1				
L(24)	L(25)	00003	-241	006	0	00005	000400000000	176377777740	00	000000000077	1 & 20						1				
L(25)	L(26)	00003	-241	003	0	00005	000400000000	176377777774	00	000000000007	1 & 20						1				
L(26)	L(27)	00003	-241	000	0	00005	000400000000	176377777777	00	000400000000	1 & 20						1				
L(27)	L(28)	00003	-241	000	0	00005	000400000000	176377777777	00	000400000000	2 & 20										1
L(28)	L(29)	00003	-241	000	0	00005	000777777777	176000000000	00	000000000000	4 & 20										
L(29)	L(30)	00003	-241	033	0	00005	000777777777	201000000000	11	000000000000	5 & 20						1				
L(30)	L(31)	00003	-241	032	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(31)	L(32)	00003	-241	030	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(32)	L(33)	00003	-241	026	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(33)	L(34)	00003	-241	024	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(34)	L(35)	00003	-241	022	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(35)	L(36)	00003	-241	020	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(36)	L(37)	00003	-241	016	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(37)	L(38)	00003	-241	014	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(38)	L(39)	00003	-241	012	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(39)	L(40)	00003	-241	010	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(40)	L(41)	00003	-241	006	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(41)	L(42)	00003	-241	004	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(42)	L(43)	00003	-241	002	0	00005	000777777777	176777777777	00	000000000000	6 & 20						1	1			
L(43)	L(44)	00003	-241	000	0	00005	000777777777	176777777777		000000000000	6 & 20						1	1			
L(44)	L(45)	00003	-241	000	0	00005	000400000000	176000000000	00	000000000000	3 & 30						1				1
L(45)	I	00003	-241	000	0	00003	000400000000	176400000000	00	000000000000	3 & 30										1
I	I	00004	+020	000	0	00000	002000000000	176400000000	00	143000000000											
I	E	00001	+500	000	0	00005	050000000005	176400000000	00	143000000000											
E	I	00001	+500	000	0	00001	173777777777	173777777777	00	143000000000											
I	E	00002	+560	000	0	00006	056000000006	173777777777	00	143000000000											

DIVISION
20th STEP EARLY
30th STEP EARLY
4th STEP EARLY DFDP 11-24 A-B (EARLY)
4th STEP LATE DFDP 11-24 L
SHIFT RIGHT AC → MQ (02.30.69.1)
MQ → MQS (02.30.30.1)
AC → AD (02.30.63.1)
SR → AD (02.30.64.1)
SET AC SIGN PLUS (02.30.70.1)
AD → AD (02.30.63.1)
SR → AD (02.30.64.1)
SET SC TO 33 (02.30.69.1)
SHIFT LEFT AC → MQ (02.30.69.1)
MQ → MQS (02.30.30.1)
TURN ON DIV CHECK TGR (02.30.30.1)
SET FP 2 TGR (02.20.06.1)
AD → AC (02.30.61.1)
AD → AC (02.30.61.1)
5th EARLY
5th STEP LATE
FDP 2E (02.20.30.1)
FDP 2L (02.20.30.1)
AD → AD (02.20.61.1)
AD → AC (02.20.63.1)
RESET 9 CAR TGR (02.20.30.1)
STEP SC (02.20.31.1)
AC → AD (02.20.60.1)
SR → AD (02.20.62.1)
AC → AD (02.20.60.1)
CI AD (02.20.66.1)
SET FP 2 TGR (02.20.06.1)
5th STEP EARLY (FDP 2E)
5th STEP LATE (FDP 2L)
MQ → AC (02.20.31.1)
SHIFT LEFT AC → MQ (02.20.20.1)
6th STEP EARLY
6th STEP LATE
DFDP DIVIDE EARLY (02.30.30.1)
DFDP DIVIDE LATE (02.30.30.1)
SR → AD (02.20.62.1) AC → AD (02.20.60.1)
AD(9-35) → AC (02.20.63.1)
1 → MQ (35) (02.20.31.1)
SHIFT LT AC (9-35) ← MQ (9-35)
MQ → AC
DFDP 26
STEP SC (02.20.31.1)
SC = 32
SC ≠ 0
(02.20.08.1) FPI TGR
(02.30.63.1) AC → AD
(02.30.60.1) SWR → SR
(02.30.61.1) AD → AC
(02.30.09.1) RESET AC
SHIFT LEFT AC → MQ (02.30.69.1)
RESET FP 2 TGR (02.20.06.1)
30th STEP (02.20.03.1)
(02.20.03.1) 30th STEP
3rd STEP EARLY
4th STEP EARLY
RESET 9 CARRY TGR (02.20.08.1)
AC → AD (02.30.63.1)
3rd STEP EARLY
FAS 3E (02.30.32.1, 02.20.11.1)
FAS 3L (02.30.32.1, 02.20.72.1)
AC → AD (02.20.60.1)
SR → AD (02.20.62.1)
AD → AC (02.20.63.1)
SHIFT RIGHT AC → MQ (02.20.11.1)
1 → AC0 (02.20.11.1)
AD → AC
(4th ST EARLY)
FAS 4E (02.30.32.1, 02.20.11.1)
FAS 4L
SR → AD (02.20.62.1)
AC → AD (02.20.61.1)
AD → AC (02.20.63.1)
MQ → SR (02.20.64.1)
AC → AD (02.20.61.1)
CI AD (02.20.66.1)
SR → AD (02.20.62.1)
AC → SR (02.20.61.1)
AD → AC (02.20.63.1)
SR → MQ (02.20.62.1)
FAS 5th STEP L Time LATE (02.30.32.1) (02.20.72.1) (02.20.12.1)
SP END OP (02.20.09.1)
FP END OP (02.30.09.1)
END OP TGR (02.15.39.1)
MASTER · I EARLY
I LATE
I GATE (02.30.13.1, 02.20.12.1)
AC(Q-8) → AD (02.20.60.1)
1 → AD (02.20.66.1)
AD → MQ (02.20.63.1)
AC → MQ
(02.20.70.1)
PR ON (DFDP)
MASTER L · I EARLY
L LATE
DFDP 24
DFDP 25
DFDP 33
DFDP 34
DFDP 35
COMPLETION OF DFDP 25
9 CARRY
FP 2 TGR ON

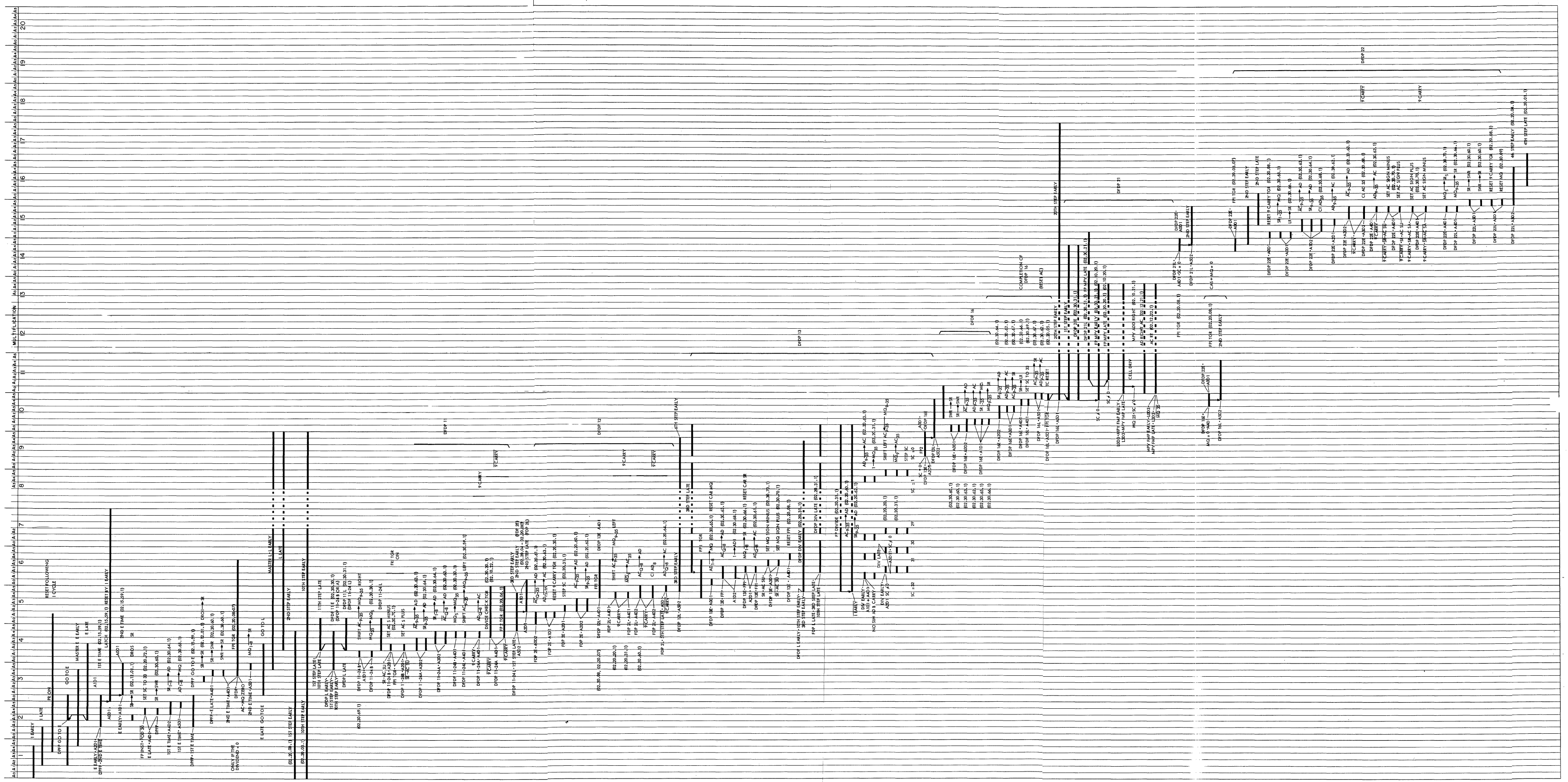


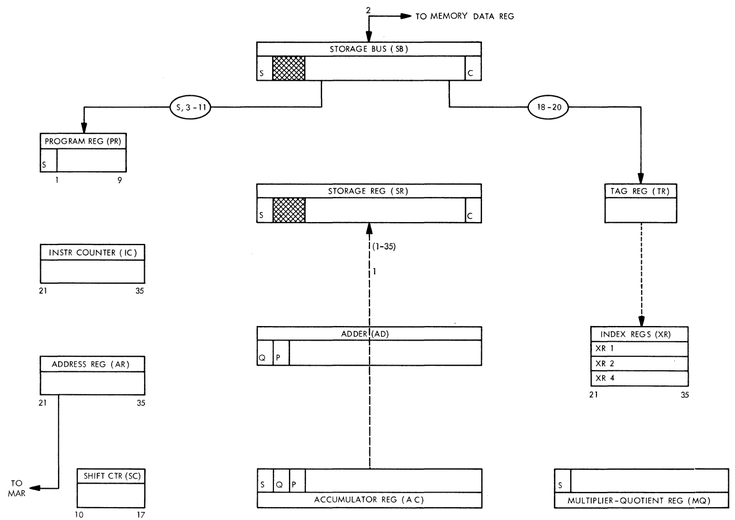
FIGURE 14. DFOP
(CONTINUED)

Store Zero (STZ +0600)
Stores all 0's into the specified memory location. The sign is made plus.

Store MQ (STQ -0600)
Stores the contents of the MQ register into the specified memory location (S, 1-35). The contents of the MQ remain unchanged.

Store (STO +0601)
Stores the contents of the accumulator (S, 1-35) into the specified memory location. The contents of the accumulator remain unchanged.

Store Logical Word (SLW +0602)
Stores the 36-bit logical word of the accumulator (P, 1-35) into the specified memory location (S, 1-35). The word in the accumulator remains unchanged.



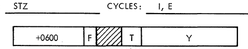
LEGEND

- I CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0600 STORE ZERO

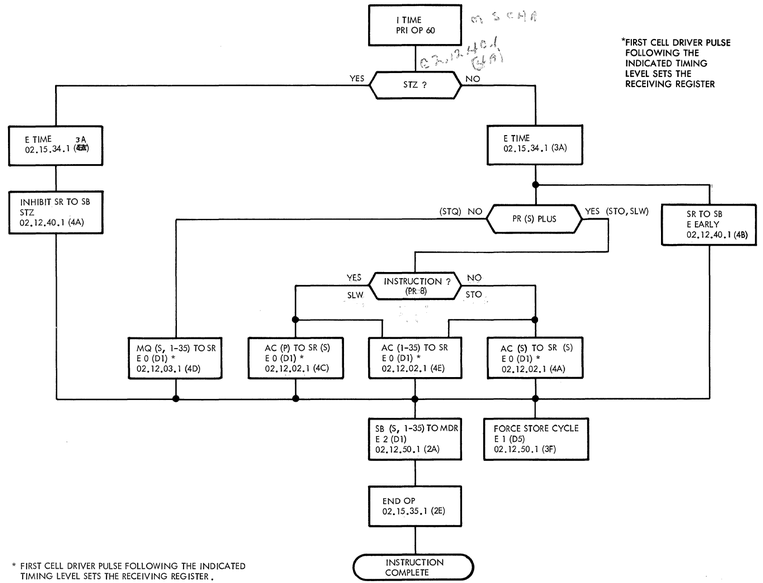
ALPHA CODE: STZ CYCLES: I, E



SEQUENCE NOTES:

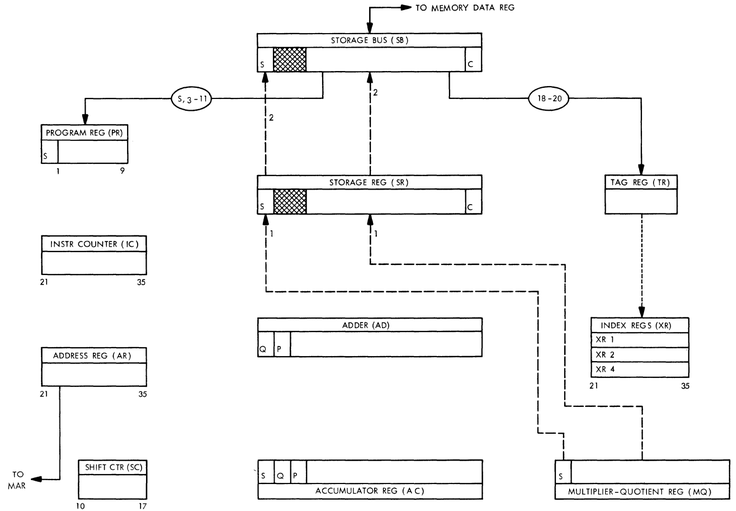
THE $C(Y)_{1-35}$ ARE REPLACED BY ZEROS AND THE SIGN OF Y IS MADE +.

FIGURE 15. STZ, STQ, STO, SLW



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

* FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER.



LEGEND

1 CYCLE

E CYCLE

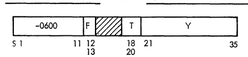
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0600 STORE MQ

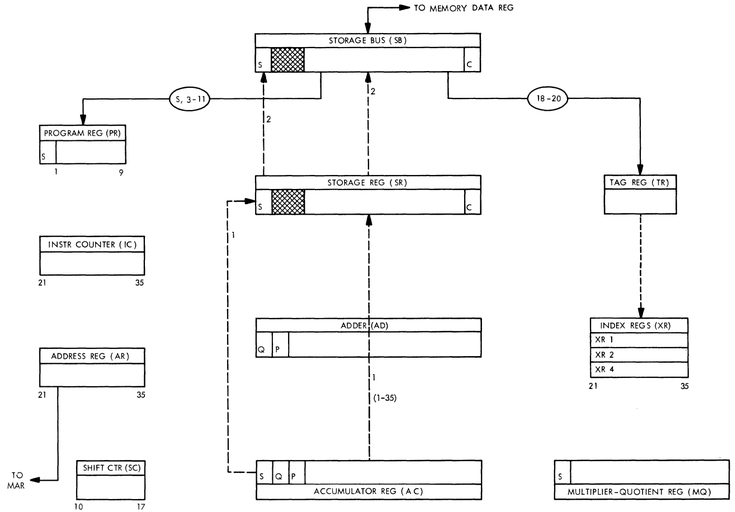
ALPHA CODE: STQ CYCLES: I, E



SEQUENCE NOTES:

THE $C(MQ)_{S-35}$ ARE PLACED INTO THE SPECIFIED Y LOCATION.

THE C(MQ) REMAIN UNCHANGED.



LEGEND

1 CYCLE

E CYCLE

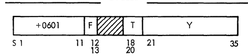
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0601 STORE

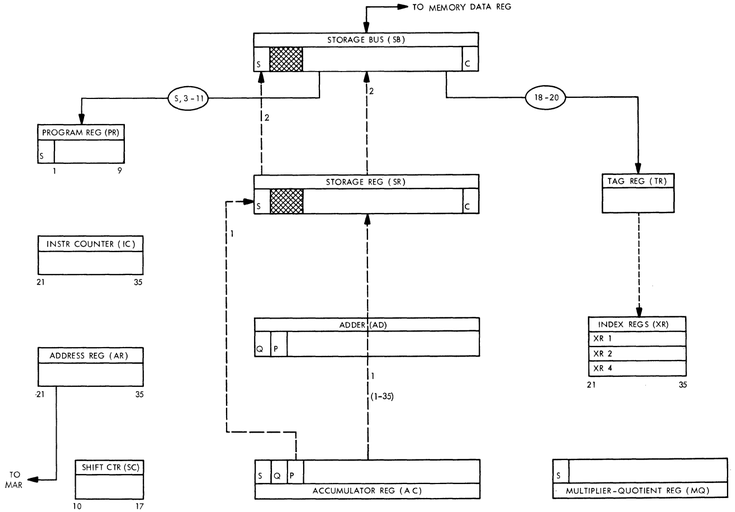
ALPHA CODE: STO CYCLES: I, E



SEQUENCE NOTES:

THE $C(AC)_{S, 1-35}$ ARE PLACED INTO LOCATION Y.

THE C(AC) ARE UNCHANGED.



LEGEND

1 CYCLE

E CYCLE

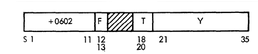
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0602 STORE LOGICAL WORD

ALPHA CODE: SLW CYCLES: I, E



SEQUENCE NOTES:

THE $C(AC)_{P, 1-35}$ ARE PLACED INTO LOCATION Y.

THE C(AC) ARE UNCHANGED.

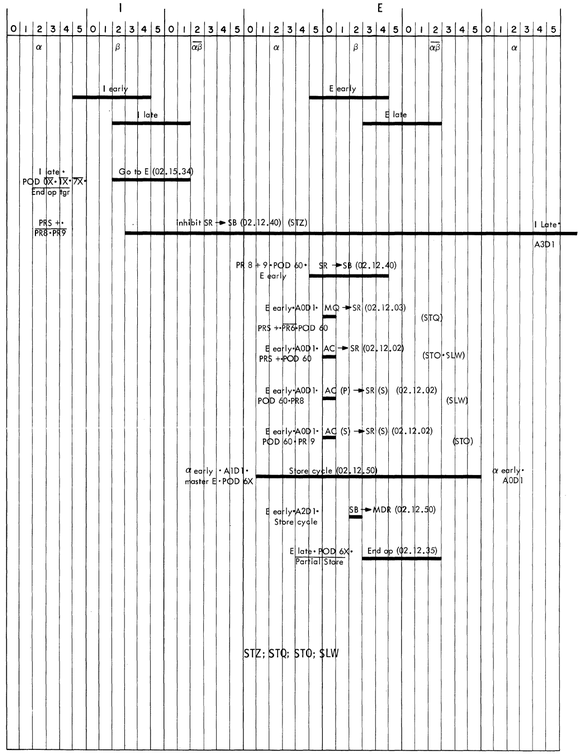


FIGURE 15. STZ, STQ, STO, SLW
(CONTINUED)

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	LDQ		00007	056000 000007
00003	STZ		00007	060000 000007
00004	LDQ		00007	056000 000007
00005	TRA		00000	002000 000000
00006	Pattern			777777 777777
00007	Live Reg			

Store Zeros (STZ)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	000000000000	
E	I	00001	+500	000	0	00001	777777777777	777777777777	00	000000000000	
I	E	00002	+601	000	0	00007	060100000000	777777777777	00	000000000000	
E	I	00002	+601	000	0	00002	777777777777	777777777777	00	000000000000	
I	E	00003	+560	000	0	00007	056000000007	777777777777	00	000000000000	
E	I	00003	+560	000	0	00003	777777777777	777777777777	00	777777777777	
I	E	00004	+600	000	0	00007	060000000007	777777777777	00	777777777777	
E	I	00004	+600	000	0	00004	000000000000	777777777777	00	777777777777	
I	E	00005	+560	000	0	00007	056000000007	777777777777	00	777777777777	
E	I	00005	+560	000	0	00005	000000000000	777777777777	00	000000000000	
I	I	00006	+020	000	0	00000	002000000000	777777777777	00	000000000000	
I	E	00001	+500	000	0	00006	050000000006	777777777777	00	000000000000	

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	LDQ		00007	056000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			777777 777777
00007	Live Reg			

Store Accumulator (STO)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS *	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	000000000000	
E	I	00001	+500	000	0	00001	777777777777	777777777777	00	000000000000	
I	E	00002	+601	000	0	00007	060100000007	777777777777	00	000000000000	
E	I	00002	+601	000	0	00002	777777777777	777777777777	00	000000000000	
I	E	00003	+560	000	0	00007	056000000007	777777777777	00	000000000000	
E	I	00003	+560	000	0	00003	777777777777	777777777777	00	777777777777	
I	I	00004	+020	000	0	00000	002000000000	777777777777	00	777777777777	
I	E	00001	+500	000	0	00006	050000000006	777777777777	00	777777777777	
E	I	00001	+500	000	0	00001	777777777777	777777777777	00	777777777777	
I	E	00002	+601	000	0	00007	060100000007	777777777777	00	777777777777	
E	I	00002	+601	000	0	00002	777777777777	777777777777	00	777777777777	
I	E	00003	+560	000	0	00007	050600000007	777777777777	00	777777777777	

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00006	056000 000006
00001	STQ		00007	460000 000007
00002	CLA		00007	050000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			777777 777777
00007	Live Reg			

Store MQ (STQ)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+560	000	0	00006	056000000006	000000000000	00	000000000000	
E	I	00001	+560	000	0	00001	777777777777	000000000000	00	777777777777	
I	E	00002	-600	000	0	00007	460000000007	000000000000	00	777777777777	
E	I	00002	-600	000	0	00002	777777777777	000000000000	00	777777777777	
I	E	00003	+500	000	0	00007	050000000007	000000000000	00	777777777777	
E	I	00003	+500	000	0	00003	777777777777	777777777777	00	777777777777	
I	I	00004	+020	000	0	00000	002000000000	777777777777	00	777777777777	
I	E	00001	+560	000	0	00006	056000000006	777777777777	00	777777777777	
E	I	00001	+560	000	0	00001	777777777777	777777777777	00	777777777777	
I	E	00002	-600	000	0	00007	460000000007	777777777777	00	777777777777	
E	I	00002	-600	000	0	00002	777777777777	777777777777	00	777777777777	
I	E	00003	+500	000	0	00007	050000000007	777777777777	00	777777777777	

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CAL		00006	450000 000006
00001	SLW		00007	060200 000007
00002	LDQ		00007	056000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			631463 146314
00007	Live Reg			

Store Logical Word (SLW)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	-500	000	0	00006	450000000006	000000000000	00	000000000000	
E	I	00001	-500	000	0	00001	631463146314	231463146314	01	000000000000	
I	E	00002	+602	000	0	00007	060200000007	231463146314	01	000000000000	
E	I	00002	+602	000	0	00002	231463146314	231463146314	01	000000000000	
I	E	00003	+560	000	0	00007	056000000007	231463146314	01	000000000000	
E	I	00003	+560	000	0	00003	631463146314	231463146314	01	631463146314	
I	I	00004	+020	000	0	00000	002000000000	231463146314	01	631463146314	
I	E	00001	-500	000	0	00006	450000000006	231463146314	01	631463146314	
E	I	00001	-500	000	0	00001	631463146314	231463146314	01	631463146314	
I	E	00002	+602	000	0	00007	060200000007	231463146314	01	631463146314	
E	I	00002	+602	000	0	00002	231463146314	231463146314	01	631463146314	
I	E	00003	+560	000	0	00007	056000000007	231463146314	01	631463146314	

Store Logical Word with Parity (SLP -1612)
Stores the 36-bit logical word of the accumulator (P, 1-35) into the specified memory location (S, 1-35). In addition, the sign bit of the accumulator is stored into the C bit position of the memory location. Unlike other store operations, parity is not generated on SLP.

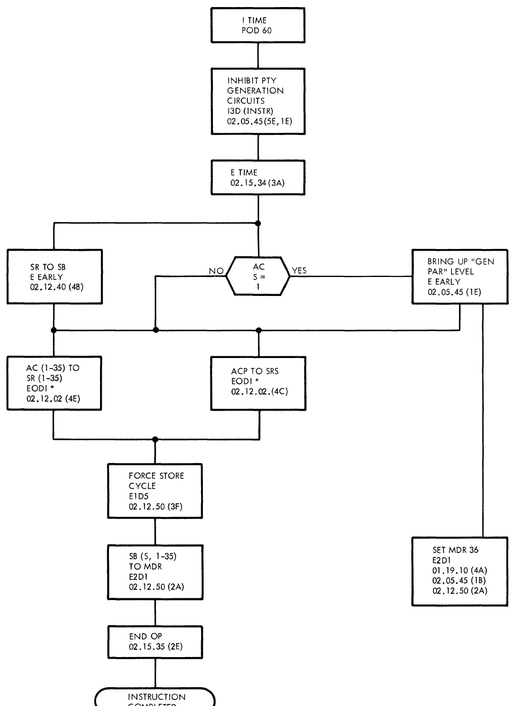
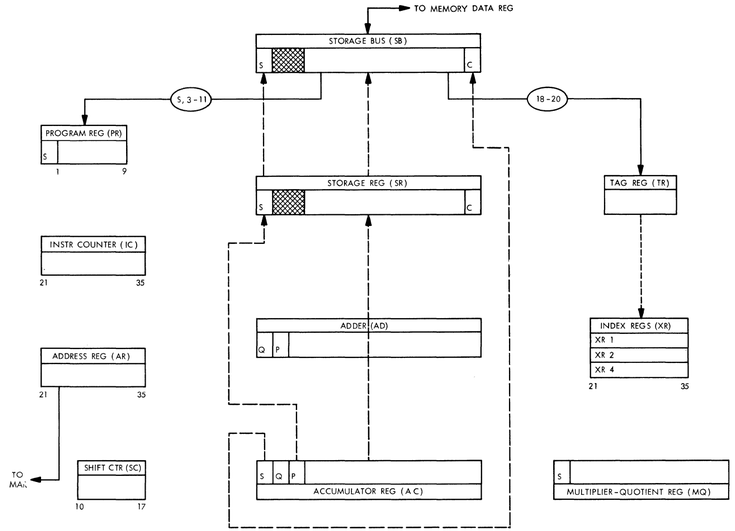


FIGURE 16. SLP



LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST STORE LOGICAL WORD WITH PARITY

ALPHA CODE: SLP CYCLES: I, E

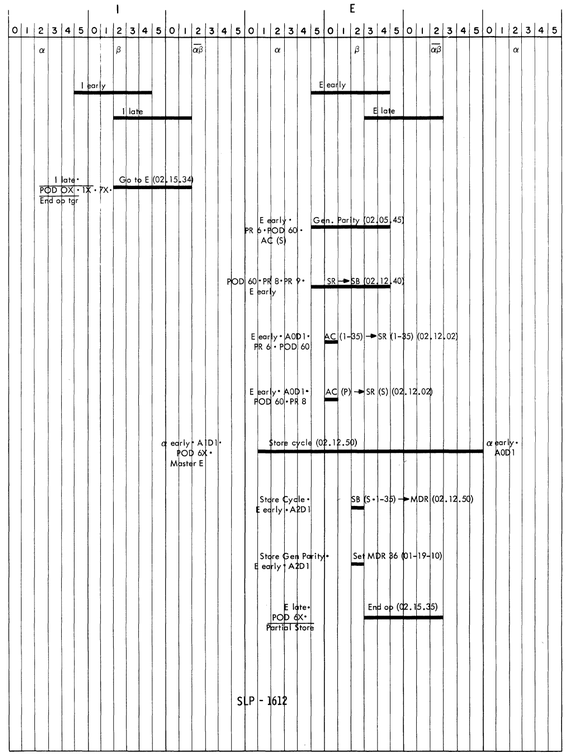
-1612	F	T	Y
S 1	11 12 13	18 20	21 35

SEQUENCE NOTES:

THE C(AC)S,P,1-35 ARE STORED INTO THE C(Y)C,S,1-35.

AC(P) ⟶ Y(S).

AC IS UNCHANGED AND PARITY IS NOT CHECKED.

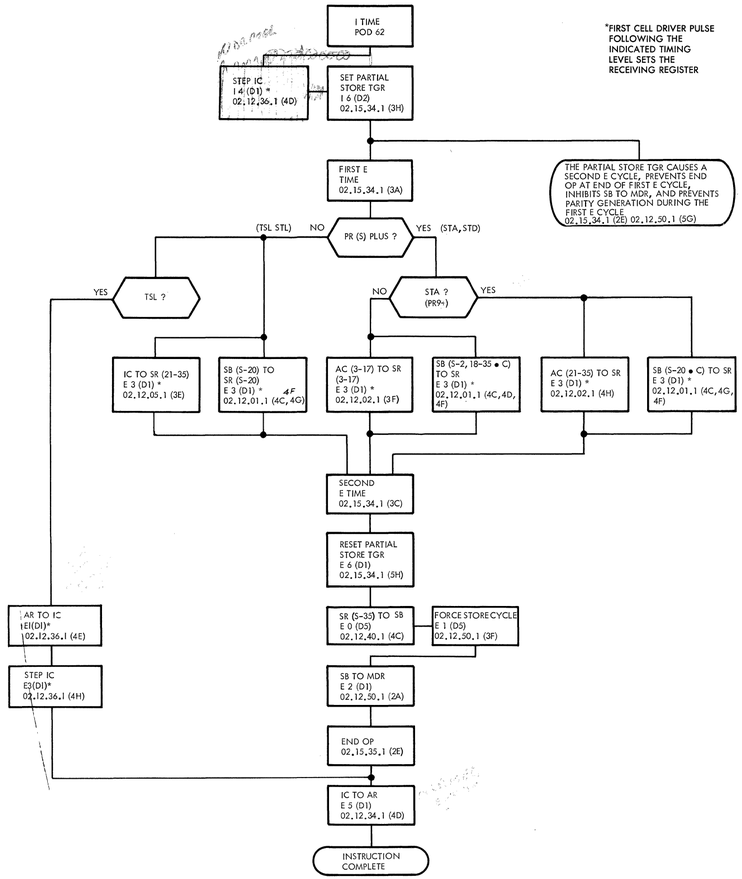


Store Address (STA +0621)
Stores the address portion of the accumulator (21-35) into positions 21-35 of the specified memory location. The rest of the memory word and the accumulator are unchanged.

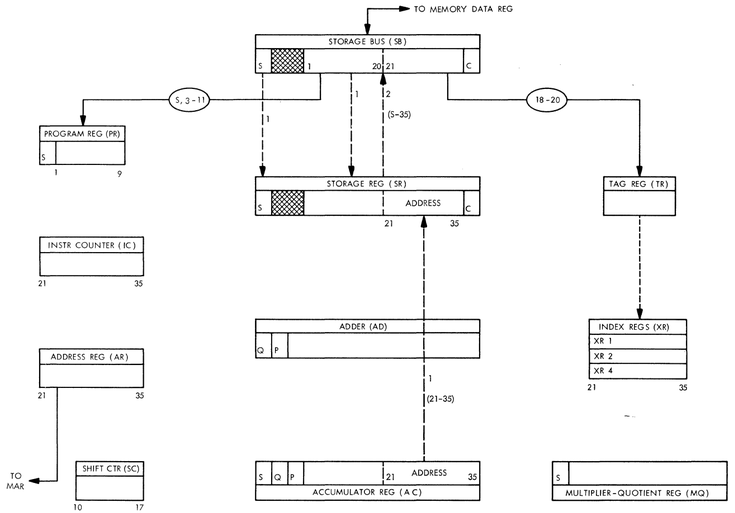
Store Decrement (STD +0622)
Stores the decrement portion of the accumulator (3-17) into positions 3-17 of the specified memory location. The rest of the memory word and the accumulator are unchanged.

Store Instruction Location Counter (STL -0625)
Stores the contents of the instruction counter (the location of the STL instruction plus 1) into positions 21-35 of the specified memory location. The rest of the memory word is unchanged.

Transfer and Store Instruction Counter (TSL -1627)
Stores the contents of the instruction counter (the location of the TSL instruction plus 1) into positions 21-35 of the specified memory location. The rest of the memory word is unchanged. The computer takes its next instruction from the specified memory location plus 1.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



LEGEND

- I CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0621 STORE ADDRESS

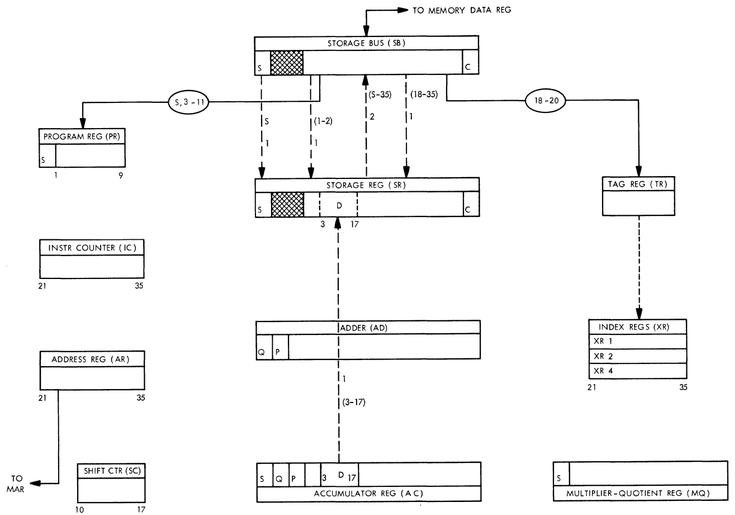
ALPHA CODE: STA CYCLES: I, E, E

SEQUENCE NOTES:

THE $C(AC)_{21-35}$ ARE PLACED INTO $C(Y)_{21-35}$.

THE $C(Y)_{S,1-20}$ AND THE C(AC) ARE UNCHANGED.

FIGURE 17. STA, STD, STL, TSL



LEGEND

1 CYCLE

E CYCLE

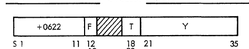
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0622 STORE DECREMENT

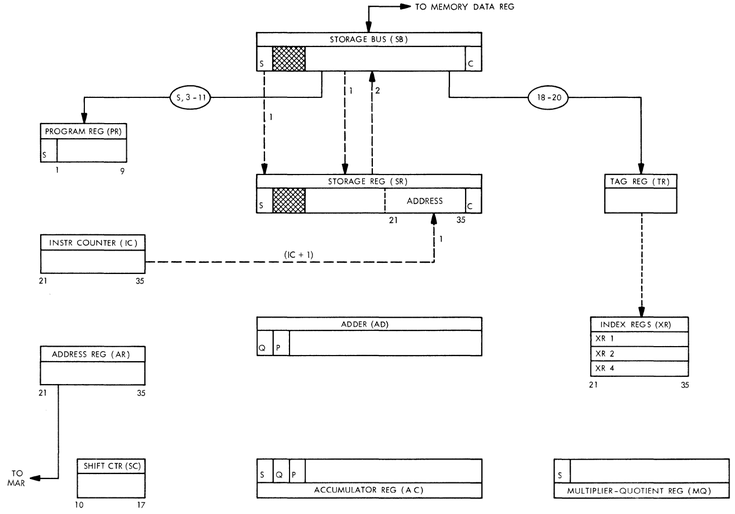
ALPHA CODE: STD CYCLES: I, E, E



SEQUENCE NOTES:

THE $C(AC)_{3-17}$ ARE PLACED INTO $C(Y)_{3-17}$.

THE $C(Y)_{S-2, 18-35}$ AND THE C(AC) ARE UNCHANGED.



LEGEND

1 CYCLE

E CYCLE

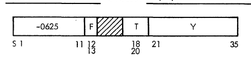
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0625 STORE INSTRUCTION LOCATION CTR

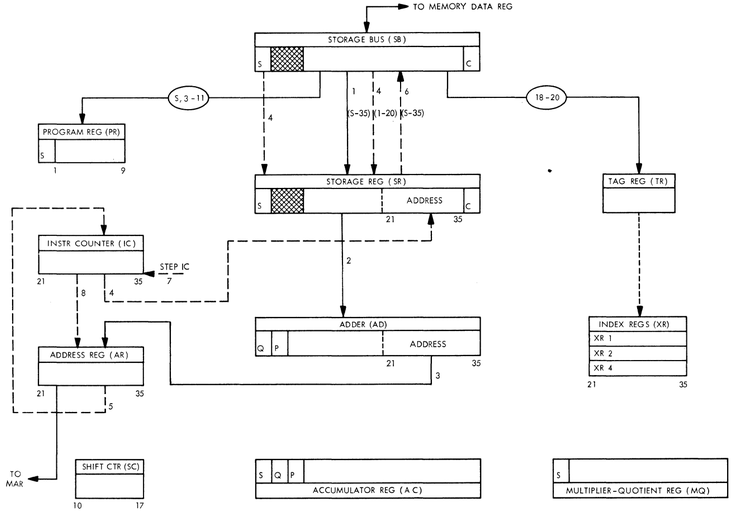
ALPHA CODE: STL CYCLES: I, E, E



SEQUENCE NOTES:

THE LOCATION OF THE STL INSTRUCTION +1 IS PLACED IN $C(Y)_{21-35}$.

THE $C(Y)_{S, 1-20}$ ARE UNCHANGED.



LEGEND

1 CYCLE

E CYCLE

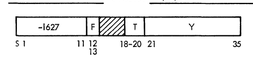
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -1627 TRANSFER AND STORE INSTRUCTION LOCATION COUNTER

ALPHA CODE: TSL CYCLES: I, E, E



SEQUENCE NOTES:

THE LOCATION OF THE TSL +1 IS STORED IN $C(Y)_{21-35}$.

POSITIONS S, 1-20 OF Y ARE UNCHANGED.

THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM Y+1.

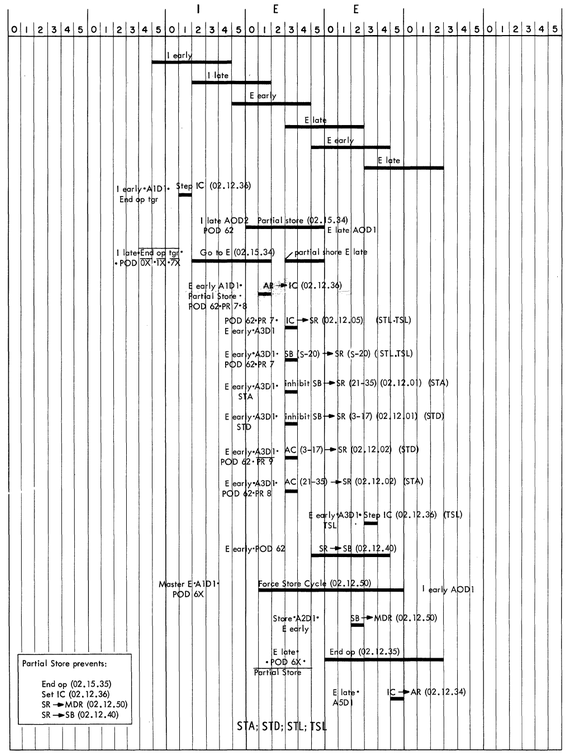


FIGURE 17. STA, STD, STL, TSL
(CONTINUED)

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STA		00007	062100 000007
00002	LDQ		00007	056000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			377777 777777
00007	Live Reg			

Store Address (STA)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S 1-35)	ACCUMULATOR (S, P)	MQ REGISTER (S 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	000000000000	
E	I	00001	+500	000	0	00001	377777777777	377777777777	00	000000000000	
I	E(1)	00002	+621	000	0	00007	062100000007	377777777777	00	000000000000	
E(1)	E(2)	00002	+621	000	0	00007	000000077777	377777777777	00	000000000000	
E(2)	I	00002	+621	000	0	00002	000000077777	377777777777	00	000000000000	
I	E	00003	+560	000	0	00007	056000000007	377777777777	00	000000000000	
E	I	00003	+560	000	0	00003	000000077777	377777777777	00	000000077777	
I	I	00004	+020	000	0	00000	002000000000	377777777777	00	000000077777	
I	E	00001	+500	000	0	00006	050000000006	377777777777	00	000000077777	
E	I	00001	+500	000	0	00001	377777777777	377777777777	00	000000077777	
I	E(1)	00002	+621	000	0	00007	062100000007	377777777777	00	000000077777	
E(1)	E(2)	00002	+621	000	0	00007	000000077777	377777777777	00	000000077777	
E(2)	I	00002	+621	000	0	00002	000000077777	377777777777	00	000000077777	
I	E	00003	+560	000	0	00007	056000000007	377777777777	00	000000077777	

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STD		00007	062200 000007
00002	LDQ		00007	056000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			377777 777777
00007	Live Reg			

Store Decrement (STD)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (S, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	000000000000	
E	I	00001	+500	000	0	00001	377777777777	377777777777	00	000000000000	
I	E(1)	00002	+622	000	0	00007	062200000007	377777777777	00	000000000000	
E(1)	E(2)	00002	+622	000	0	00007	077777000000	377777777777	00	000000000000	
E(2)	I	00002	+622	000	0	00002	077777000000	377777777777	00	000000000000	
I	E	00003	+560	000	0	00007	056000000007	377777777777	00	000000000000	
E	I	00003	+560	000	0	00003	077777000000	377777777777	00	077777000000	
I	I	00004	+020	000	0	00000	002000000000	377777777777	00	077777000000	
I	E	00001	+500	000	0	00006	050000000006	377777777777	00	077777000000	
E	I	00001	+500	000	0	00001	377777777777	377777777777	00	077777000000	
I	E(1)	00002	+622	000	0	00007	062200000007	377777777777	00	077777000000	
E(1)	E(2)	00002	+622	000	0	00007	077777000000	377777777777	00	077777000000	
E(2)	I	00002	+622	000	0	00002	077777000000	377777777777	00	077777000000	
I	E	00003	+560	000	0	00007	056000000007	377777777777	00	077777000000	

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STL		00007	462500 000007
00002	CLA		00007	050000 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			377777 777777
00007	Live Reg			

Store Instruction Location Counter (STL)

CONSOLE INDICATORS												
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00		
E	I	00001	+500	000	0	00001	377777777777	377777777777	00		
I	E(1)	00002	-625	000	0	00007	462500000007	377777777777	00		
E(1)	E(2)	00002	-625	000	0	00007	000000000002	377777777777	00		
E(2)	I	00002	-625	000	0	00002	000000000002	377777777777	00		
I	E	00003	+500	000	0	00007	050000000007	377777777777	00		
E	I	00003	+500	000	0	00003	000000000002	000000000002	00		
I	I	00004	+020	000	0	00000	002000000000	000000000002	00		
I	E	00001	+500	000	0	00006	050000000006	000000000002	00		

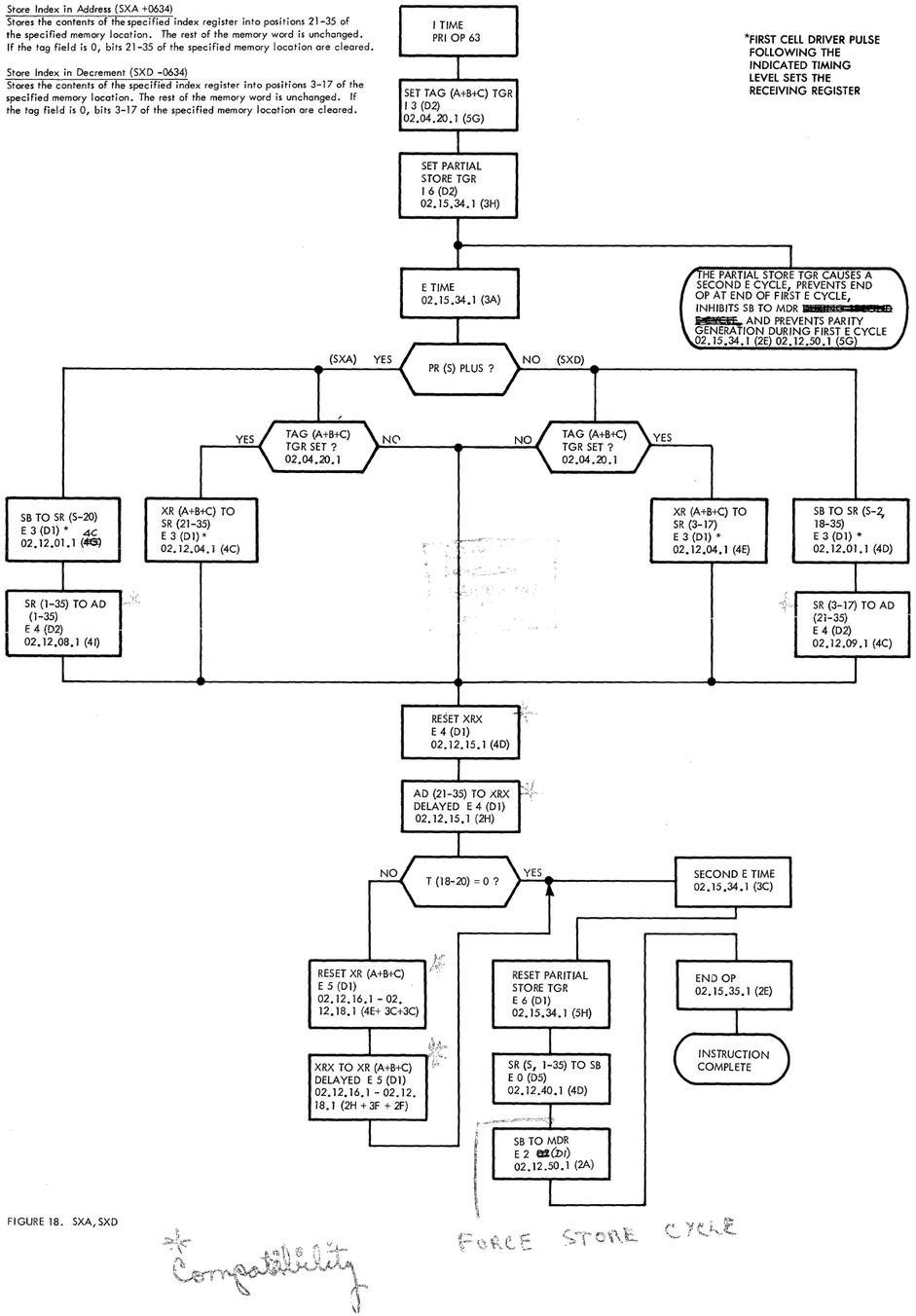
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TSL		00003	562700 000003
00002	TRA		00001	002000 000001
00003	TRA		00000	002000 000000
00004	ADD		00006	040000 000006
00005	TRA		00003	002000 000003
00006	Pattern			000000 000001

TRANSFER AND STORE INSTRUCTION COUNTER (TSL)

CONSOLE INDICATORS												
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00		
E	I	00001	+500	000	0	00001	000000000001	000000000001	00		
I	E(1)	00002	-627	000	0	00003	562700000003	000000000001	00		
E(1)	E(2)	00002	-627	000	0	00003	002000000002	000000000001	00		
E(2)	I	00004	-627	000	0	00004	002000000002	000000000001	00		
I	E	00005	+400	000	0	00006	040000000006	000000000001	00		
E	I	00005	+400	000	0	00005	000000000001	000000000002	00	*	
I	I	00006	+020	000	0	00003	002000000003	000000000002	00		
I	I	00004	+020	000	0	00002	002000000002	000000000002	00		
I	I	00003	+020	000	0	00001	002000000001	000000000002	00		
I	E(1)	00002	-627	000	0	00003	562700000003	000000000002	00		
E(1)	E(2)	00003	-627	000	0	00003	002000000002	000000000002	00		
E(2)	I	00004	-627	000	0	00004	002000000003	000000000002	00		
I	E	00005	+400	000	0	00006	050000000006	000000000002	00		
E	I	00005	+400	000	0	00005	000000000001	000000000003	00	*	
Note: *Increase accumulator by one for each program pass.											

Store Index in Address (SXA +0634)
Stores the contents of the specified index register into positions 21-35 of the specified memory location. The rest of the memory word is unchanged. If the tag field is 0, bits 21-35 of the specified memory location are cleared.

Store Index in Decrement (SXD -0634)
Stores the contents of the specified index register into positions 3-17 of the specified memory location. The rest of the memory word is unchanged. If the tag field is 0, bits 3-17 of the specified memory location are cleared.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

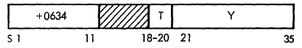
FIGURE 18. SXA, SXD

FORCE STORE CYCLE

Compatibility

INST +0634 STORE INDEX IN ADDRESS

ALPHA CODE: SXA CYCLES: I, E, E

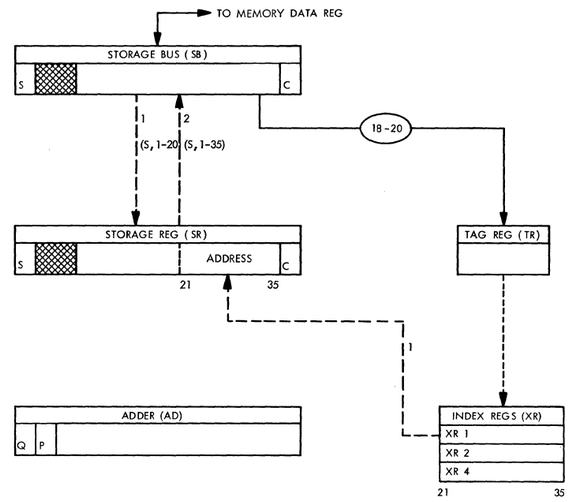


SEQUENCE NOTES:

THE CONTENTS OF THE SPECIFIED INDEX REGISTER(S) ARE STORED IN $C(Y)_{21-35}$.

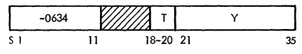
THE $C(Y)_{S,1-20}$ ARE UNCHANGED.

WITH A TAG OF ZERO, THE $C(Y)_{21-35}$ ARE CLEARED TO ZEROS.



INST -0634 STORE INDEX IN DECREMENT

ALPHA CODE: SXD CYCLES: I, E, E

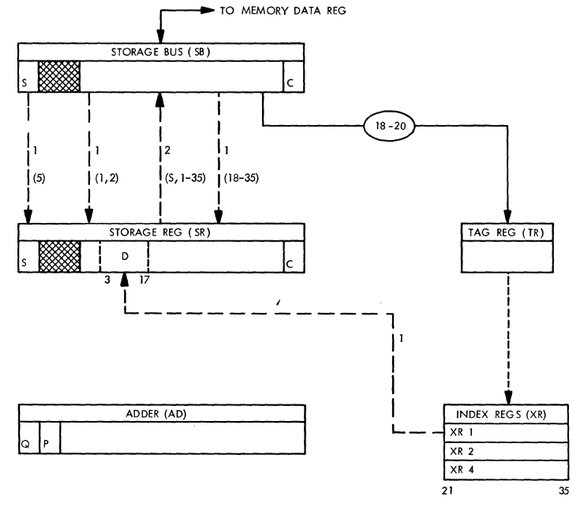


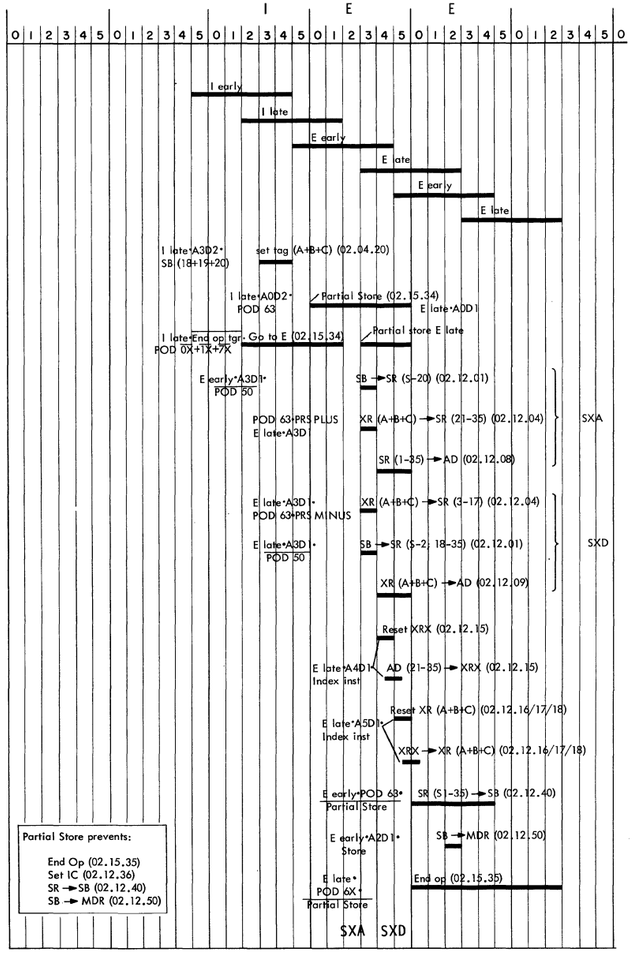
SEQUENCE NOTES:

THE CONTENTS OF THE SPECIFIED INDEX REGISTER(S) ARE STORED IN $C(Y)_{3-17}$.

THE $C(Y)_{S-2,\ 18-35}$ ARE UNCHANGED.

WITH A TAG OF ZERO, THE $C(Y)_{3-17}$ ARE CLEARED TO ZEROS.





Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	AXT	7	77777	077400 777777
00003	SXA	7	00007	463400 700007
00004	LDQ		00007	056000 000007
00005	TRA		00000	002000 000000
00006	Pattern			042077 700000
00007	Live Reg			

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	AXT	7	77777	077400 777777
00003	SXD	7	00007	463400 700007
00004	LDQ		00007	056000 000007
00005	TRA		00000	002000 000000
00006	Pattern			042000 777777
00007	Live Reg			

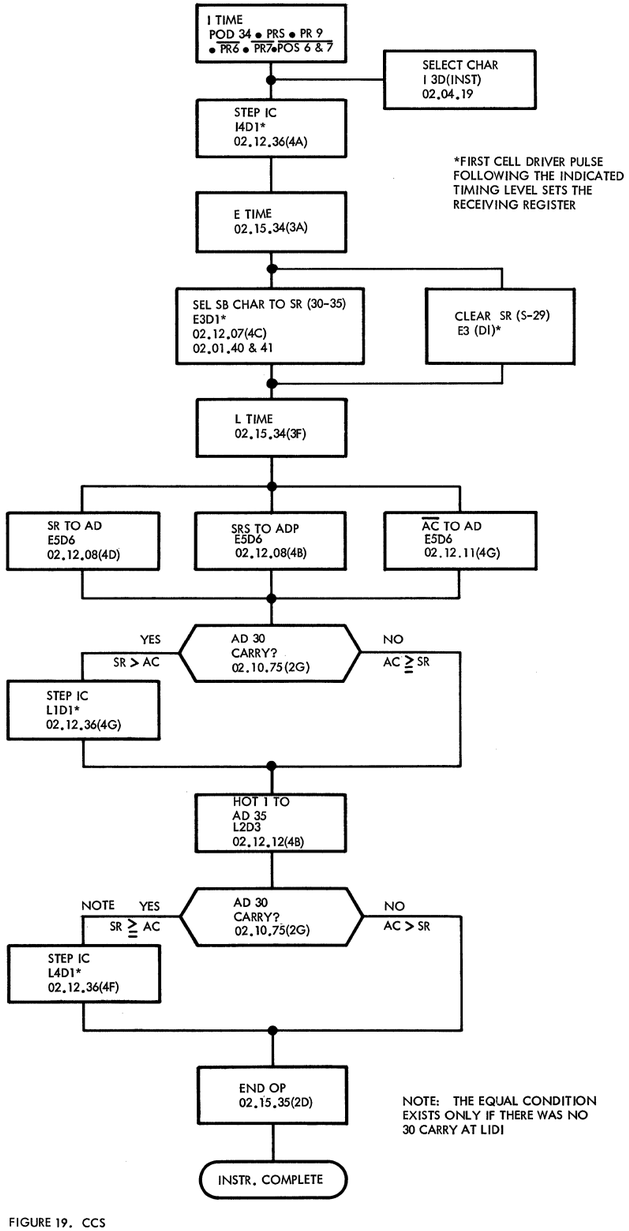
Store Index in Address (SXA)

CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	000000000000		00000									
E	I	00001	+500	000	0	00001	042077700000	042077700000	00	000000000000		00000									
I	E	00002	+601	000	0	00007	060100000007	042077700000	00	000000000000		00000									
E	I	00002	+601	000	0	00002	042077700000	042077700000	00	000000000000		00000									
I	I	00003	+774	377	7	00003	077400777777	042077700000	00	000000000000		77777									
I	E(1)	00004	+634	000	7	00007	063400700007	042077700000	00	000000000000		77777									
E(1)	E(2)	00004	+634	000	7	00007	042077777777	042077700000	00	000000000000		77777									
E(2)	I	00004	+634	000	7	00004	042077777777	042077700000	00	000000000000		77777									
I	E	00005	+560	000	0	00007	056000000007	042077700000	00	000000000000		77777									
E	I	00005	+560	000	0	00005	042077777777	042077700000	00	042077777777		77777									
I	I	00006	+020	000	0	00000	002000000000	042077700000	00	042077777777		77777									
I	E	00001	+500	000	0	00006	050000000006	042077700000	00	042077777777		77777									
E	I	00001	+500	000	0	00001	042077700000	042077700000	00	042077777777		77777									
I	E	00002	+601	000	0	00007	060100000007	042077700000	00	042077777777		77777									
E	I	00002	+601	000	0	00002	042077700000	042077700000	00	042077777777		77777									
I	I	00003	+774	377	7	00003	077400777777	042077700000	00	042077777777		77777									
I	E(1)	00004	+634	000	7	00007	063400700007	042077700000	00	042077777777		77777									
E(1)	E(2)	00004	+634	000	7	00007	042077777777	042077700000	00	042077777777		77777									
E(2)	I	00004	+634	000	7	00004	042077777777	042077700000	00	042077777777		77777									
I	E	00005	+560	000	0	00007	056000000007	042077700000	00	042077777777		77777									

Store Index in Decrement (SXD)

CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	000000000000		00000									
E	I	00001	+500	000	0	00001	042000777777	042000777777	00	000000000000		00000									
I	E	00002	+601	000	0	00007	060100000007	042000777777	00	000000000000		00000									
E	I	00002	+601	000	0	00002	042000777777	042000777777	00	000000000000		00000									
I	I	00003	+774	377	7	00003	077400777777	042000777777	00	000000000000		77777									
I	E(1)	00004	-634	000	7	00007	463400700007	042000777777	00	000000000000		77777									
E(1)	E(2)	00004	-634	000	7	00007	077777777777	042000777777	00	000000000000		77777									
E(2)	I	00004	-634	000	7	00004	077777777777	042000777777	00	000000000000		77777									
I	E	00005	+560	000	0	00007	056000000007	042000777777	00	000000000000		77777									
E	I	00005	+560	000	0	00005	077777777777	042000777777	00	077777777777		77777									
I	I	00006	+020	000	0	00000	002000000000	042000777777	00	077777777777		77777									
I	E	00001	+500	000	0	00006	050000000006	042000777777	00	077777777777		77777									
E	I	00001	+500	000	0	00001	042000777777	042000777777	00	077777777777		77777									
I	E	00002	+601	000	0	00007	060100000007	042000777777	00	077777777777		77777									
E	I	00002	+601	000	0	00002	042000777777	042000777777	00	077777777777		77777									
I	I	00003	+774	377	7	00003	077400777777	042000777777	00	077777777777		77777									
I	E(1)	00004	-634	000	7	00007	463400700007	042000777777	00	077777777777		77777									
E(1)	E(2)	00004	-634	000	7	00007	077777777777	042000777777	00	077777777777		77777									
E(2)	I	00004	-634	000	7	00004	077777777777	042000777777	00	077777777777		77777									
I	E	00005	+560	000	0	00007	056000000007	042000777777	00	077777777777		77777									

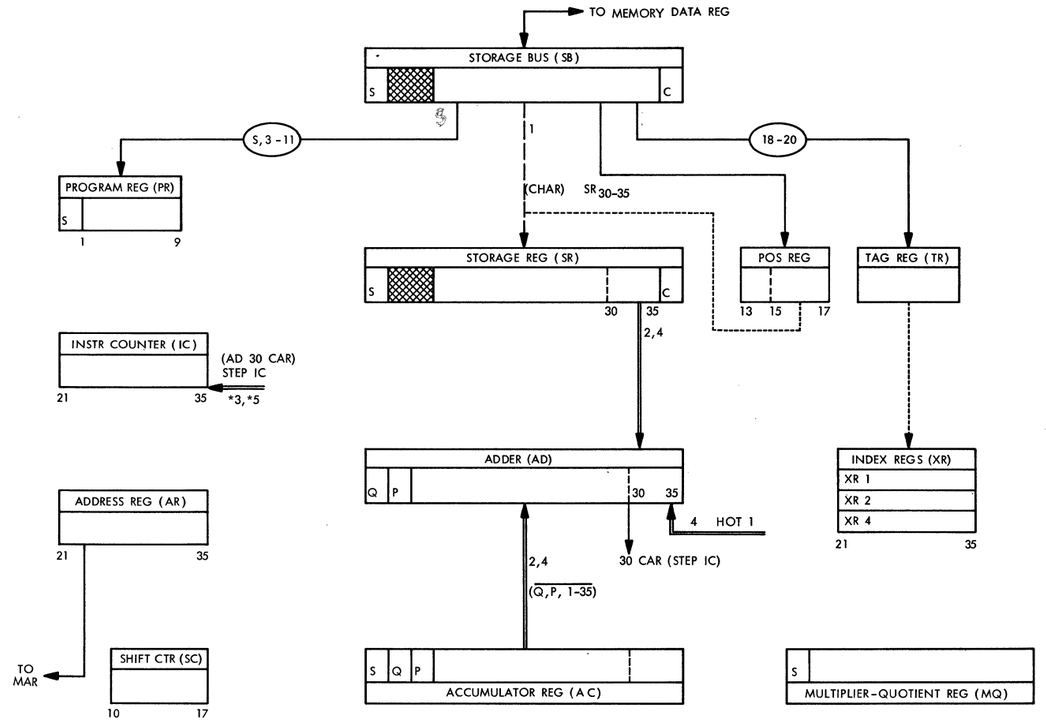
Compare Character with Storage (CCS -1341)
Compares the character in positions 30-35 of the accumulator with the character (specified by bits 15-17 of the instruction word) in the specified memory location. If the accumulator character bits are greater than the character in memory, the computer takes the next sequential instruction; if these bits are equal to the specified character, the computer skips the next instruction and proceeds from there; if they are less than the specified character, the computer skips the next two instructions. The contents of the accumulator and memory are unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

NOTE: THE EQUAL CONDITION EXISTS ONLY IF THERE WAS NO 30 CARRY AT L1D1

FIGURE 19. CCS



LEGEND

1 CYCLE

E CYCLE

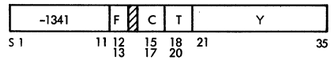
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -1341 -- C COMPARE CHARACTER WITH STORAGE

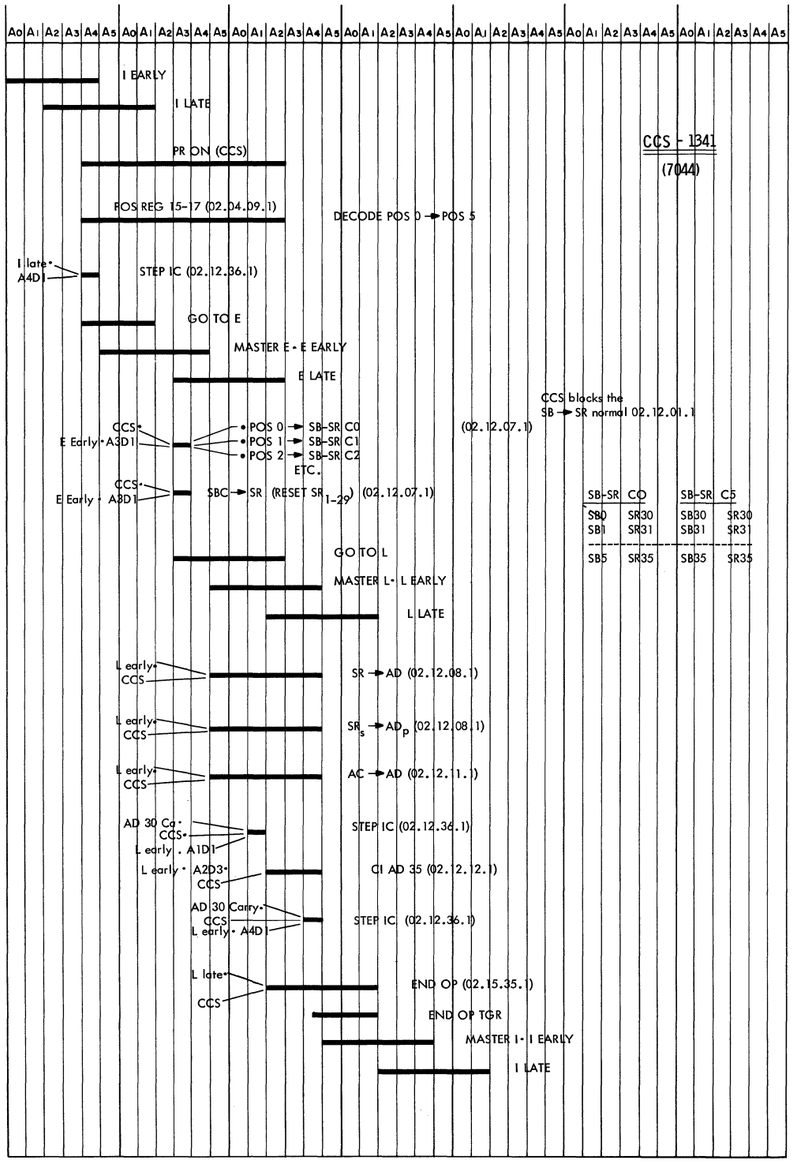
ALPHA CODE: CCS CYCLES: I, E, (L)



SEQUENCE NOTES:

THE CHARACTER IN LOCATION Y SPECIFIED BY THE "C" FIELD IS COMPARED WITH THE $C(AC)_{30-35}$. IF $C(AC)_{30-35} >$ CHARACTER IN Y, TAKE THE NEXT INSTRUCTION. IF $C(AC)_{30-35} =$ TO THE SPECIFIED CHAR, SKIP 1 INSTRUCTION. IF THE $C(AC)_{30-35} <$ CHAR, SKIP 2 INSTRUCTIONS.

CYCLES REQUIRED 7040: I, E
7044: I, E, L



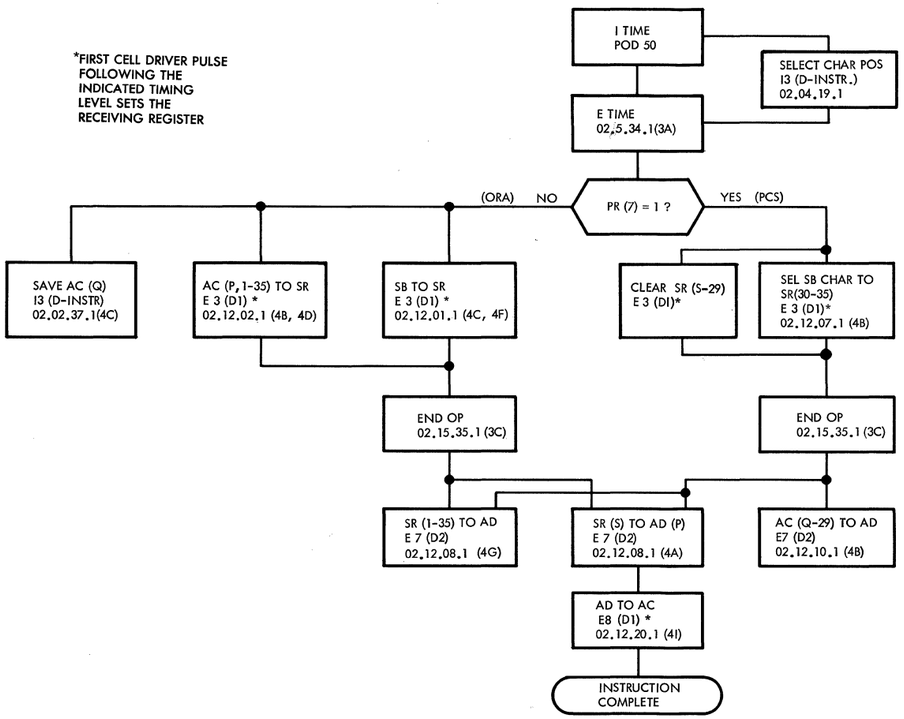
Compare Character with Storage (CCS)

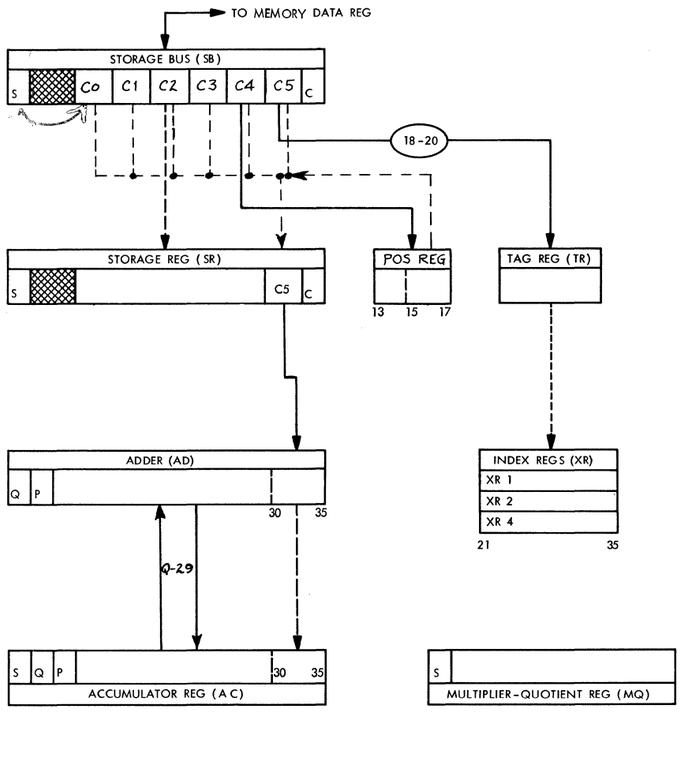
CONSOLE INDICATORS

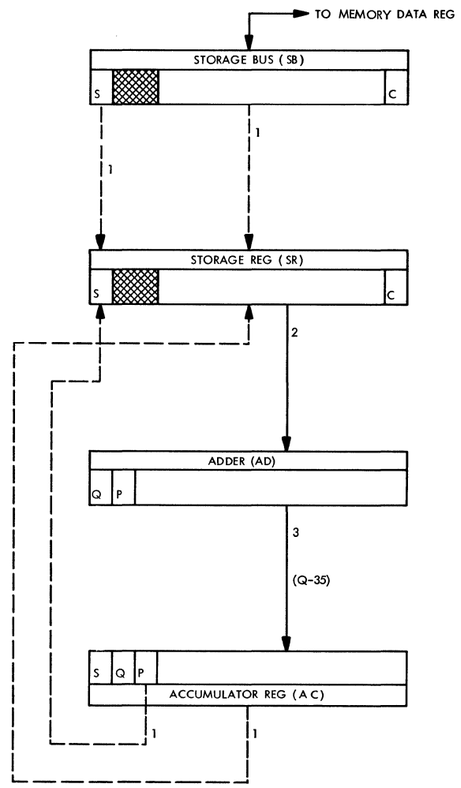
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	042000000076	042000000076	00												
I	E	00002	-341	000	0	00003	534105000003	042000000076	00				17 15&								
E	L	00002	-341	000	0	00003	000000000075	042000000076	00				17 15&								
L	I	00002	-341	000	0	00002	000000000075	042000000076	00				17 15&								
I	I	00003	+020	000	0	00000	002000000000	042000000076	00												
I	E	00001	+500	000	0	00006	050000000006	042000000076	00												

Place Character from Storage (PCS -1505)
Places the character (specified by bits 15-17 of the instruction word) of the specified memory location into positions 30-35 of the accumulator. The memory word and the rest of the accumulator are unchanged.

OR to Accumulator (ORA -0501)
Logically OR's each bit of the specified memory location with the corresponding bits of the accumulator. The result is placed in the accumulator. The sign bit of the memory word is OR'ed with the P bit of the accumulator. The contents of memory and bits S and Q of the accumulator are unchanged.
Logical OR'ing is as follows:
1,1 = 0
1,0 = 1
0,1 = 1
0,0 = 0

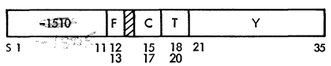






INST -1510--C PLACE CHARACTER FROM STORAGE

ALPHA CODE: PCS CYCLES: I, E



SEQUENCE NOTES:

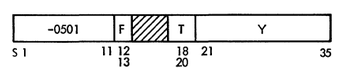
THE CHARACTER IN LOCATION Y SPECIFIED BY THE "C" FIELD OF THE INSTRUCTION REPLACES THE $C(AC)_{30-35}$.

THE $C(AC)_{S, Q, P, 1-29}$ ARE UNCHANGED.

THE C(Y) ARE UNCHANGED.

INST -0501 OR TO ACCUMULATOR

ALPHA CODE: ORA CYCLES: I

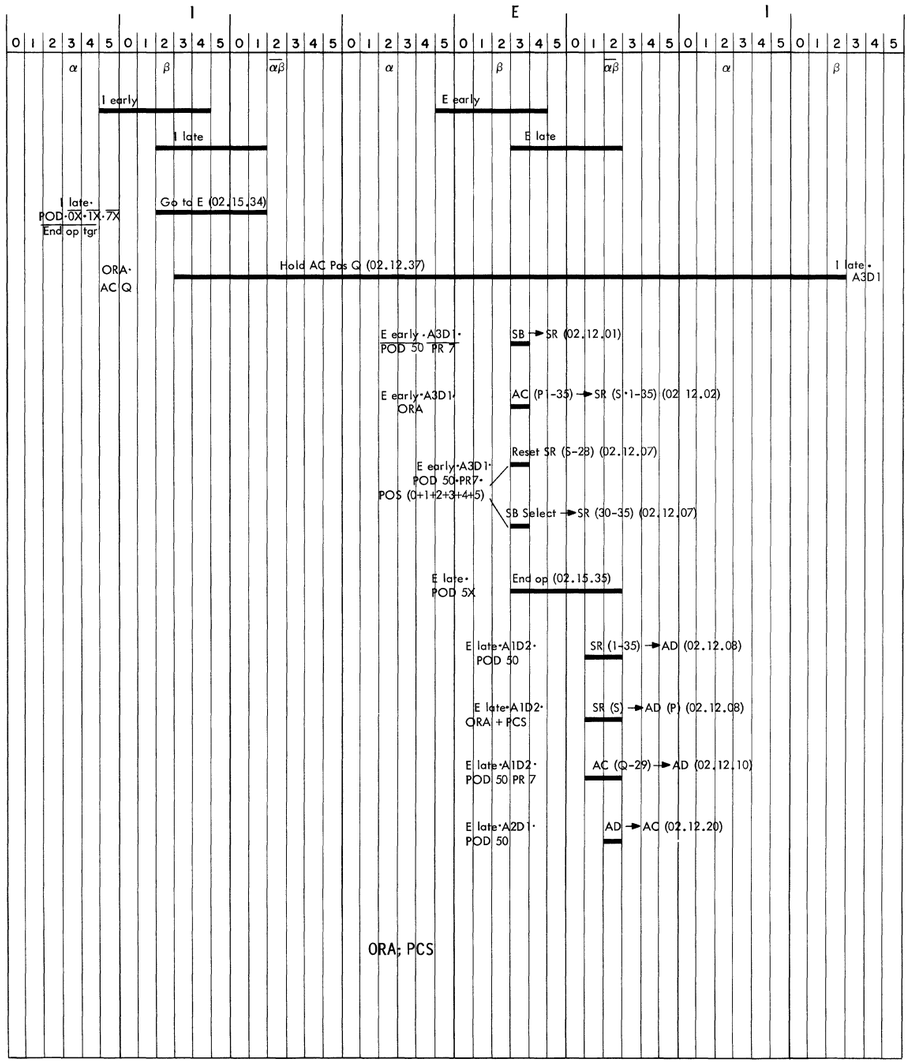


SEQUENCE NOTES:

LOGICAL ADDITION OF $C(AC)_{P-35}$ AND $C(Y)_{S-35}$.

THE AC(Q) AND AC(S) ARE UNCHANGED.

FIGURE 20. PCS, ORA



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	STO		00007	060100 000007
00002	CAL		00006	450000 000006
00003	ORA		00007	450100 000007
00004	TRA		00000	002000 000000
00005	Pattern			252525 252525
00006	Pattern			252525 525252

OR to Accumulator (ORA)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00												
E	I	00001	+500	000	0	00001	252525252525	252525252525	00												
I	E	00002	+601	000	0	00007	060100000007	252525252525	00												
E	I	00002	+601	000	0	00002	252525252525	252525252525	00												
I	E	00003	-500	000	0	00006	450000000006	252525252525	00												
E	I	00003	-500	000	0	00003	252525525252	252525525252	00												
I	E	00004	-501	000	0	00007	450100000007	252525525252	00												
E	I	00004	-501	000	0	00004	252525777777	252525777777	00												
I	I	00005	+020	000	0	00000	002000000000	252525777777	00												
I	E	00001	+500	000	0	00005	050000000005	252525777777	00												

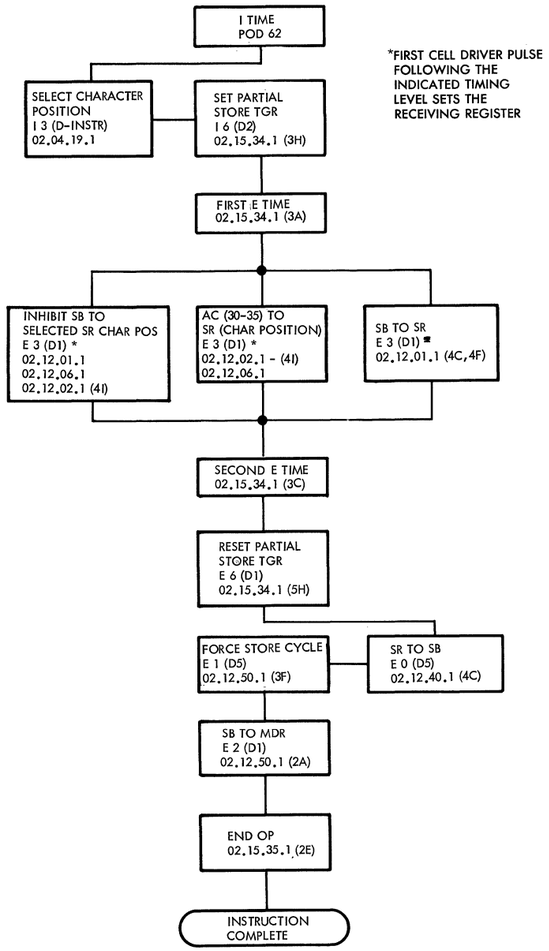
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	PCS (C=0)		00007	550500 000007
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			172737 475767
00007	Live Reg			

Place Character from Storage (PCS)

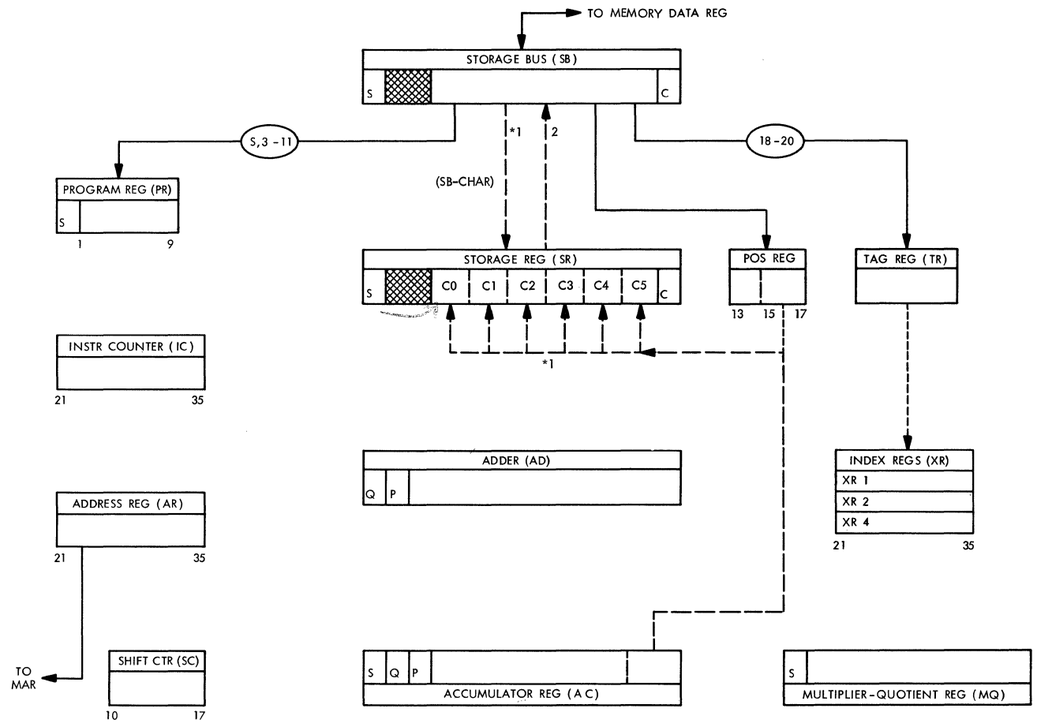
CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	172737475767	172737475767	00												
I	E	00002	+601	000	0	00007	060100000007	172737475767	00												
E	I	00002	+601	000	0	00002	172737475767	172737475767	00												
I	E	00003	-505	000	0	00007	550500000007	172737475767	00												
E	I	00003	-505	000	0	00003	000000000017	172737475717	00												
I	I	00004	+020	000	0	00000	002000000000	172737475717	00												
I	E	00001	+500	000	0	00006	050000000006	172737475717	00												

Store Accumulator Character (SAC -1623)
Stores the character in accumulator positions 30-35 into the specified memory location character position (specified by bits 15-17 of the instruction word). The contents of the accumulator and the rest of the memory word are unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



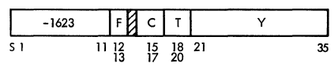
LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -1623---C STORE ACCUMULATOR CHARACTER

ALPHA CODE: SAC CYCLES: I, E, E



SEQUENCE NOTES:

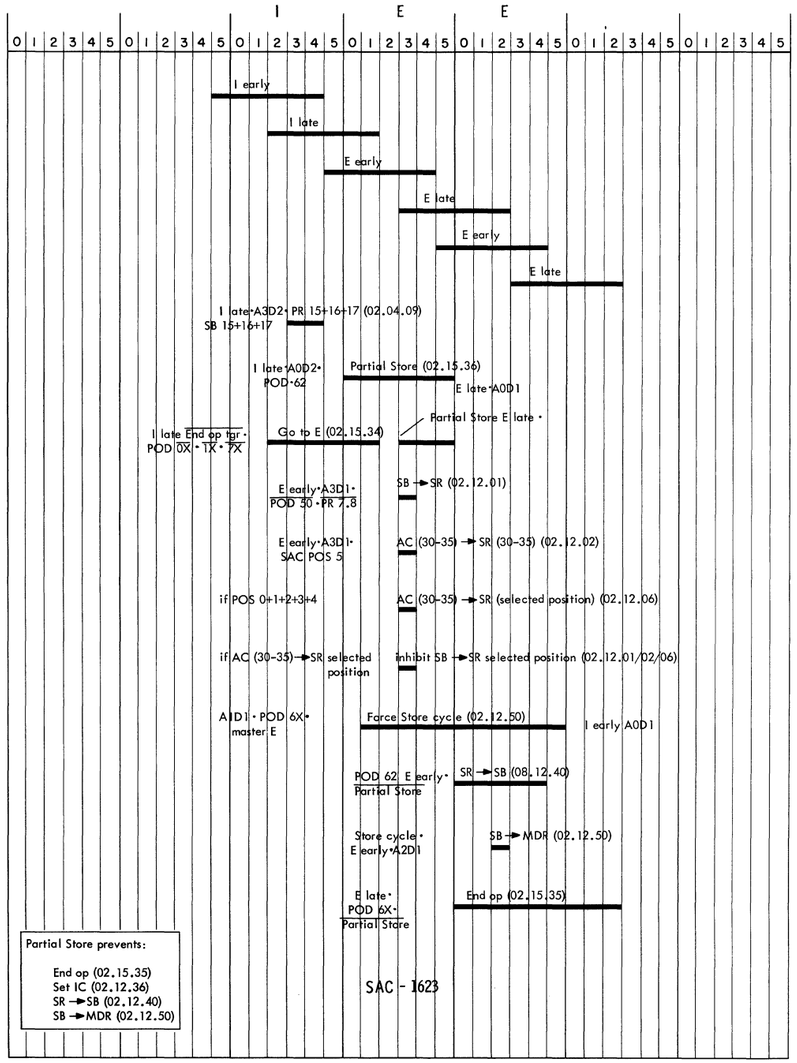
THE $C(AC)_{30-35}$ IS STORED IN LOCATION Y IN THE CHARACTER POSITION SPECIFIED BY C.

THE REMAINING BITS OF THE C(Y) ARE UNCHANGED.

THE C(AC) ARE UNCHANGED.

*1 $C(AC)_{30-35}$ → SB CHARACTER POSITION SPECIFIED BY POS REG

FIGURE 21. SAC



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	SAC (C=0)		00007	562300 000007
00003	LDQ		00007	056000 000007
00004	TRA		00000	002000 000000
00005				
00006	Pattern			675747 372717

Store Accumulator Character (SAC)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	675747372717	675747372717	00	000000000000											
I	E	00002	+601	000	0	00007	060100000007	675747372717	00	000000000000											
E	I	00002	+601	000	0	00002	675747372717	675747372717	00	000000000000											
I	E(1)	00003	-623	000	0	00007	562300000007	675747372717	00	000000000000											
E(1)	E(2)	00003	-623	000	0	00007	175747372717	675747372717	00	000000000000											
E(2)	I	00003	-623	000	0	00003	175747372717	675747372717	00	000000000000											
I	E	00004	+560	000	0	00007	056000000007	675747372717	00	000000000000											
E	I	00004	+560	000	0	00004	175747372717	675747372717	00	175747372717											
I	I	00005	+020	000	0	00000	002000000000	675747372717	00	175747372717											
I	E	00001	+500	000	0	00006	050000000000	675747372717	00	175747372717											
E	I	00001	+500	000	0	00001	675747372717	675747372717	00	175747372717											
I	E	00002	+601	000	0	00007	060100000007	675747372717	00	175747372717											
E	I	00002	+601	000	0	00002	675747372717	675747372717	00	175747372717											
I	E(1)	00003	-623	000	0	00007	562300000007	675747372717	00	175747372717											
E(1)	E(2)	00003	-623	000	0	00007	175747372717	675747372717	00	175747372717											
E(2)	I	00003	-623	000	0	00003	175747372717	675747372717	00	175747372717											
I	E	00004	+560	000	0	00007	056000000007	675747372717	00	175747372717											

AND to Accumulator (ANA -0320)

Logically AND's each bit of the specified memory location with the corresponding bits of the accumulator. The memory word sign bit is AND'ed with the accumulator P bit. The AND'ed result of the two words appears in the accumulator. Bits S and Q of the accumulator are cleared, and the contents of the memory word are unchanged. Logical AND'ing is as follows:

1,1 = 1
1,0 = 0
0,1 = 0
0,0 = 0

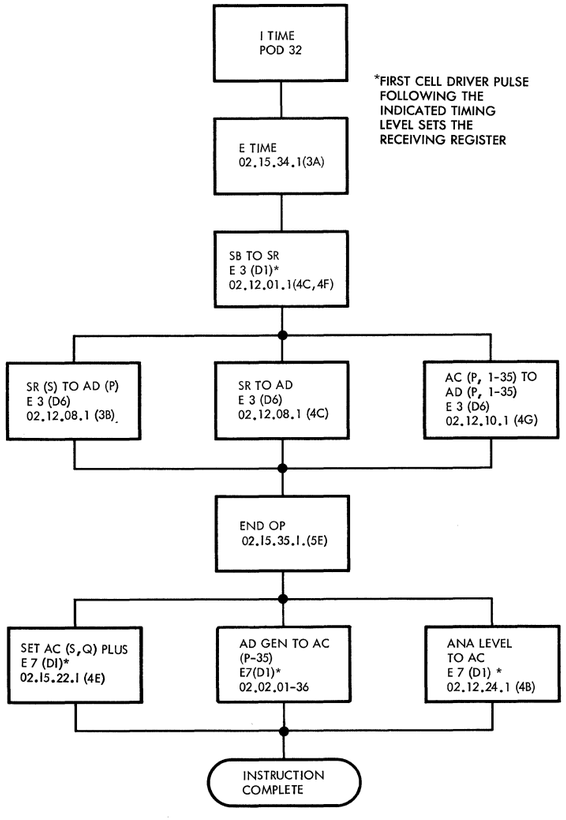
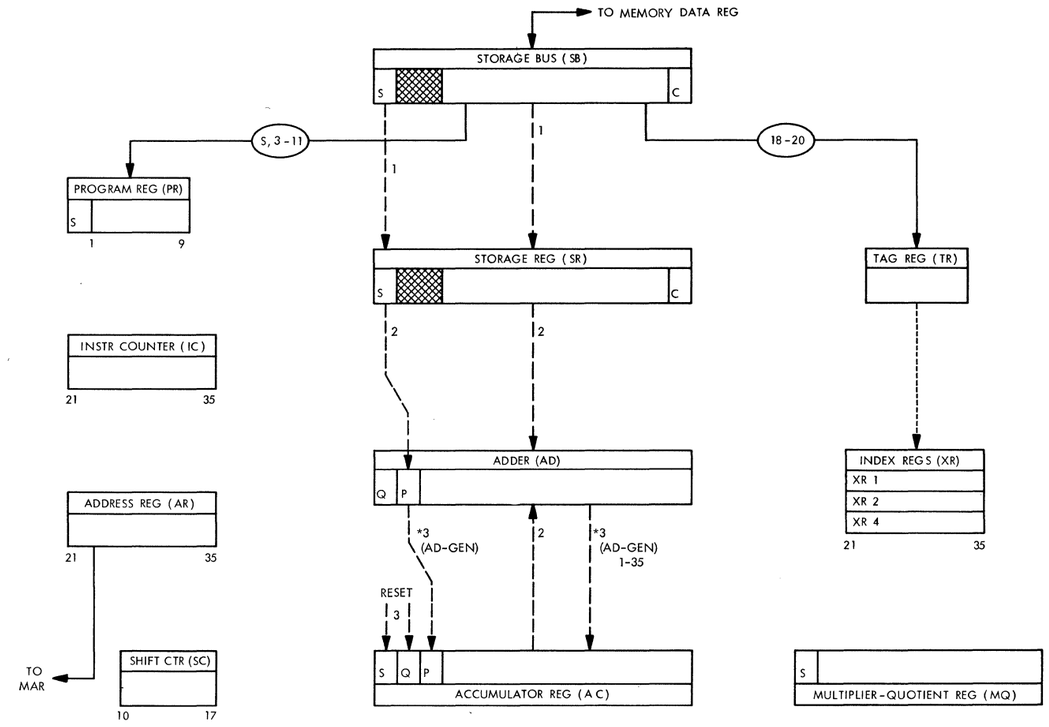


FIGURE 22. ANA



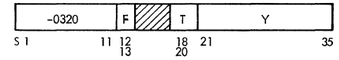
LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

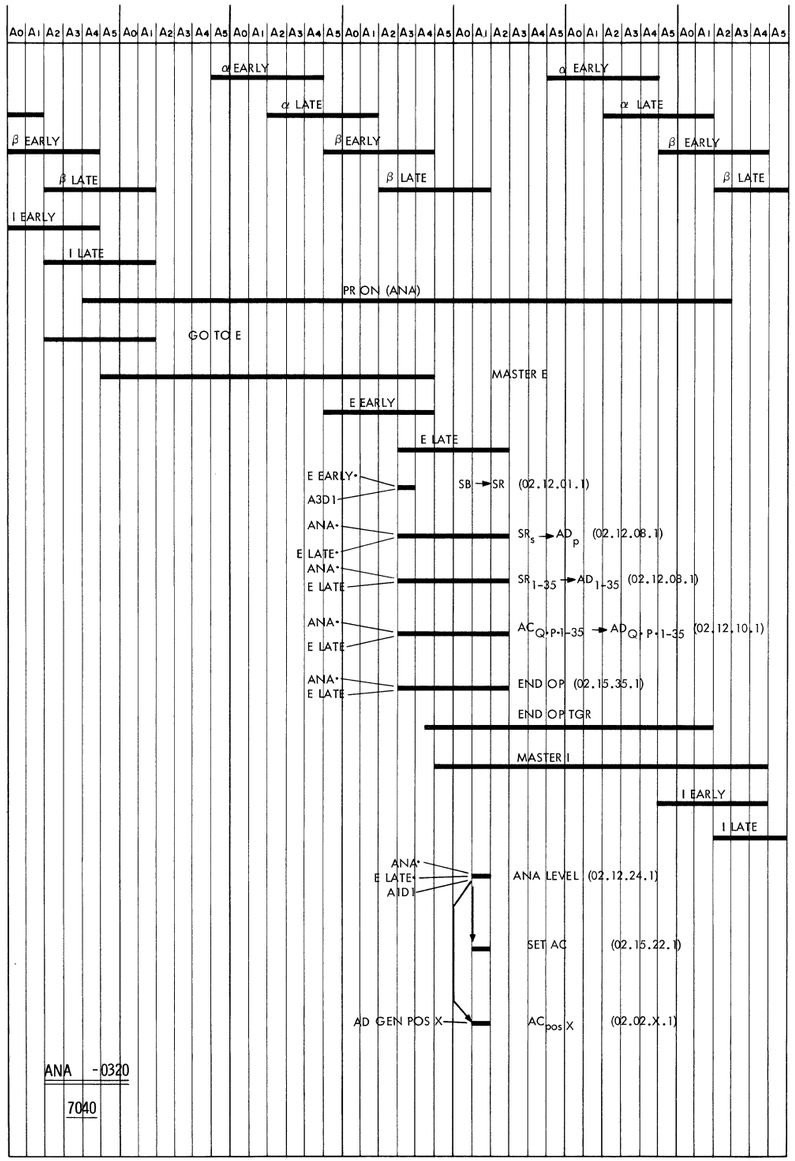
INST -0320 AND TO ACCUMULATOR

ALPHA CODE: ANA CYCLES: I, E



SEQUENCE NOTES:

LOGICAL MULTIPLICATION OF $AC_{P,1-35}$ AND $C(Y)_{S,1-35}$.
AC(S) AND AC(Q) ARE CLEARED. THE C(Y) ARE UNCHANGED.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	STO		00007	060100 000007
00002	CAL		00006	450000 000006
00003	ANA		00007	432000 000007
00004	TRA		00000	002000 000000
00005	Pattern			525252 252525
00006	Pattern			652525 252525

And to Accumulator (ANA)

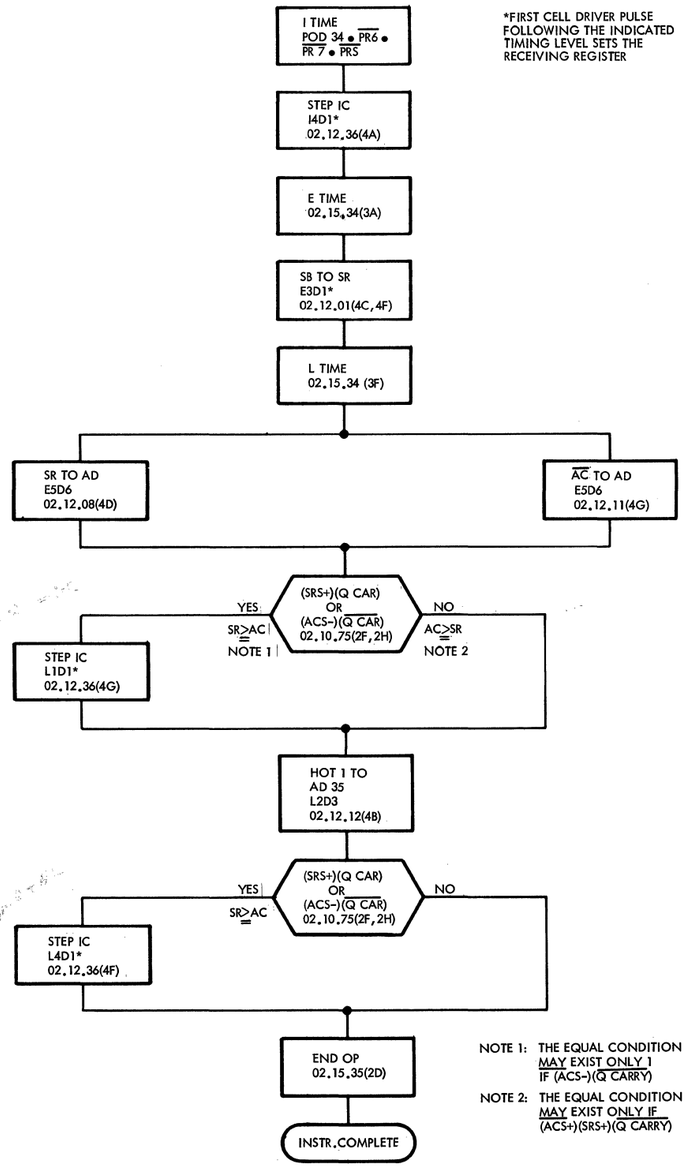
CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP1	FP2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00												
E	I	00001	+500	000	0	00001	525252252525	525252252525	00												
I	E	00002	+601	000	0	00007	060100000007	525252252525	00												
E	I	00002	+601	000	0	00002	525252252525	525252252525	00												
I	E	00003	-500	000	0	00006	450000000006	525252252525	00												
E	I	00003	-500	000	0	00003	652525252525	252525252525	01												
I	E	00004	-320	000	0	00007	432000000007	252525252525	01												
E	I	00004	-320	000	0	00004	525252252525	000000252525	01												
I	I	00005	+020	000	0	00000	002000000000	000000252525	01												
I	E	00001	+500	000	0	00005	050000000005	000000252525	01												

Compare Accumulator with Storage (CAS +0340)

Compares algebraically the contents of the accumulator and the specified memory location. If the accumulator is the greater, the computer takes the next sequential instruction. If the accumulator and memory are equal, the computer skips the next instruction and proceeds from there. If the accumulator is less than memory, the computer skips the next two instructions.

A +0 is considered greater than a -0

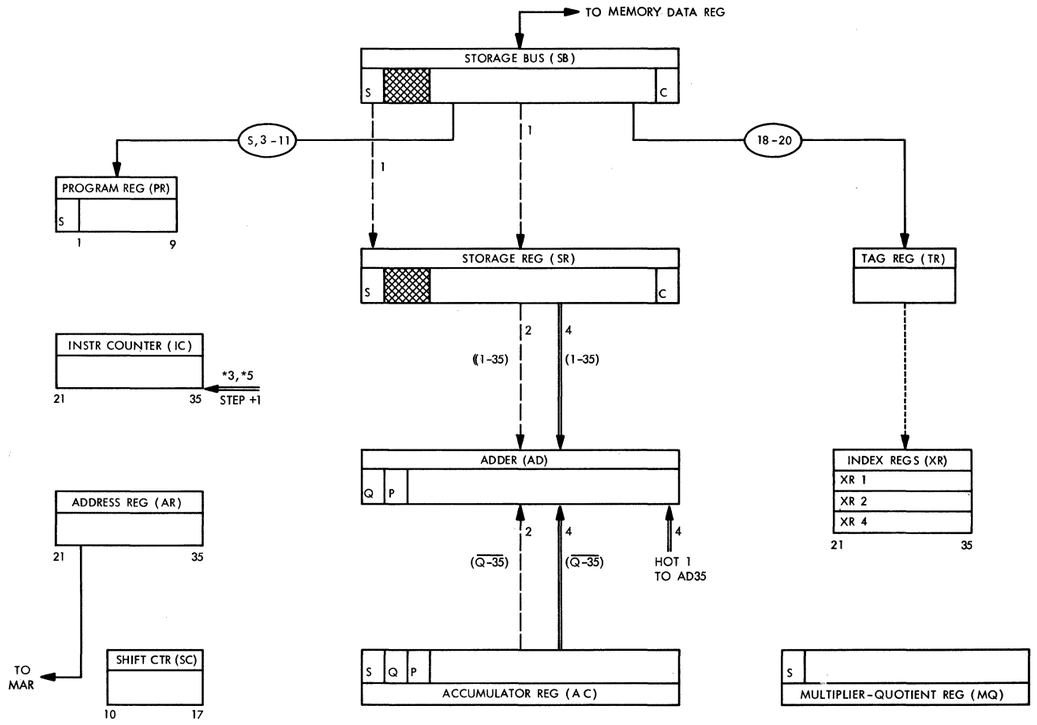


*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

NOTE 1: THE EQUAL CONDITION MAY EXIST ONLY 1 IF (ACS-)(Q CARRY)

NOTE 2: THE EQUAL CONDITION MAY EXIST ONLY IF (ACS+)(SRS+)(Q CARRY)

FIGURE 23. CAS



LEGEND

1 CYCLE

E CYCLE

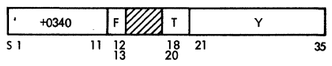
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0340 COMPARE ACCUMULATOR WITH STORAGE

ALPHA CODE: CAS CYCLES: I, E, (L)



SEQUENCE NOTES:

IF: C(AC) > C(Y), THE COMPUTER TAKES NEXT INSTRUCTION.

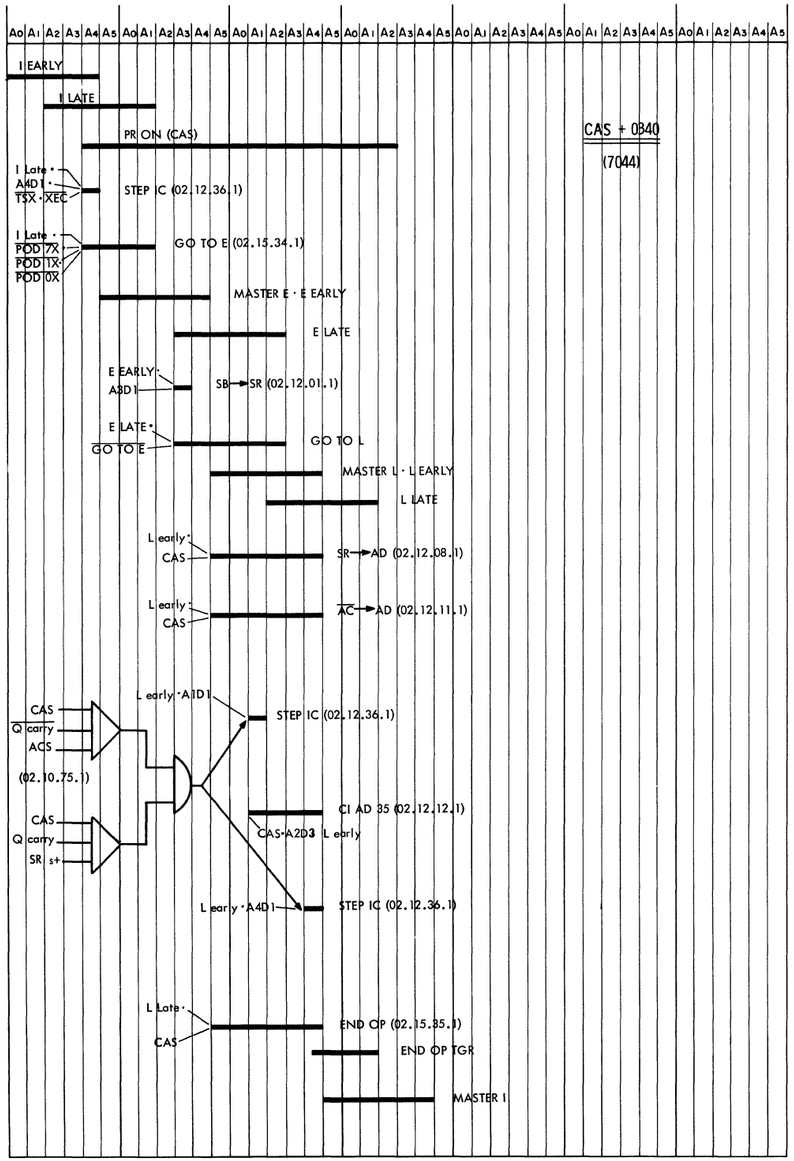
C(AC) = C(Y), THE COMPUTER SKIPS 1 INSTRUCTION.

C(AC) < C(Y), THE COMPUTER SKIPS 2 INSTRUCTIONS.

A PLUS ZERO (+0) IS CONSIDERED GREATER THAN A MINUS ZERO (-0).

CYCLES REQUIRED: 7040: I, E
7044: I, E, L

*3, *5 AC(S)-, Q CAR
SR(S)+, Q CAR



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	CAS		00006	034000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			177777 777777
00006	Pattern			777777 777777

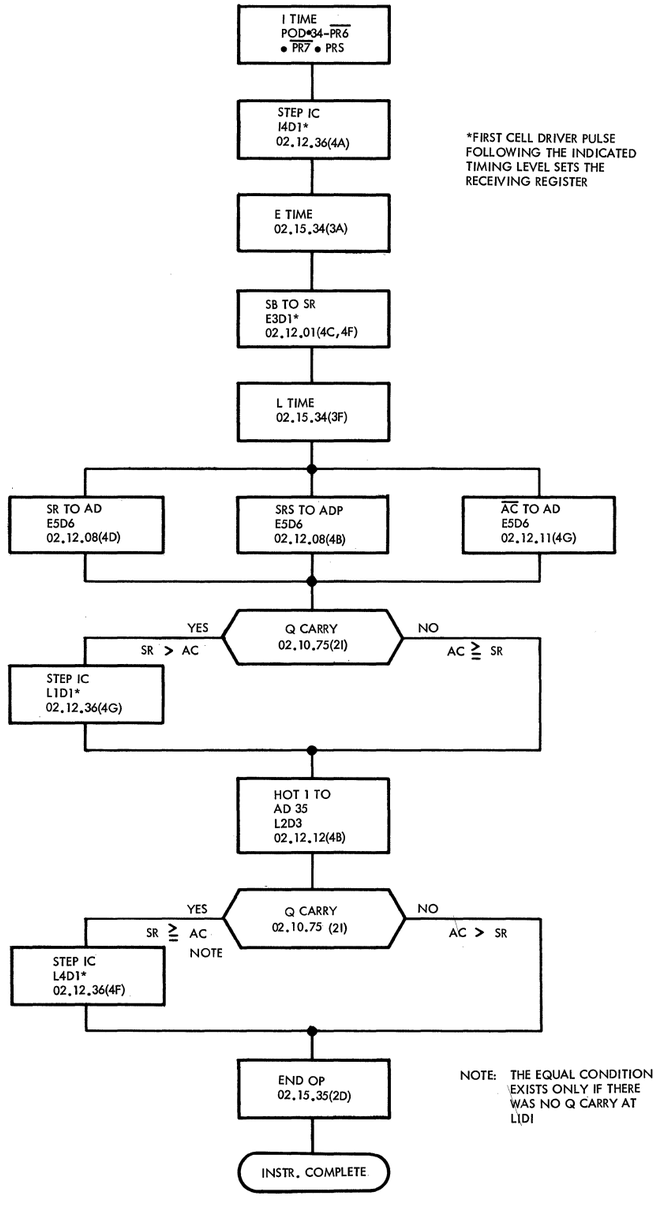
Compare Accumulator to Storage (CAS)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000									0				
E	I	00001	+500	000	0	00001	177777777777	177777777777									0				
I	E	00002	+340	000	0	00006	034000000006	177777777777									0				
E	L	00002	+340	000	0	00006	777777777777	177777777777									0				
L	I	00002	+340	000	0	00002	777777777777	177777777777									1				
I	I	00003	+020	000	0	00000	002000000000	177777777777									0				
I	E	00001	+500	000	0	00005	050000000005	177777777777									0				

Logical Compare Accumulator with Storage (LAS -0340)

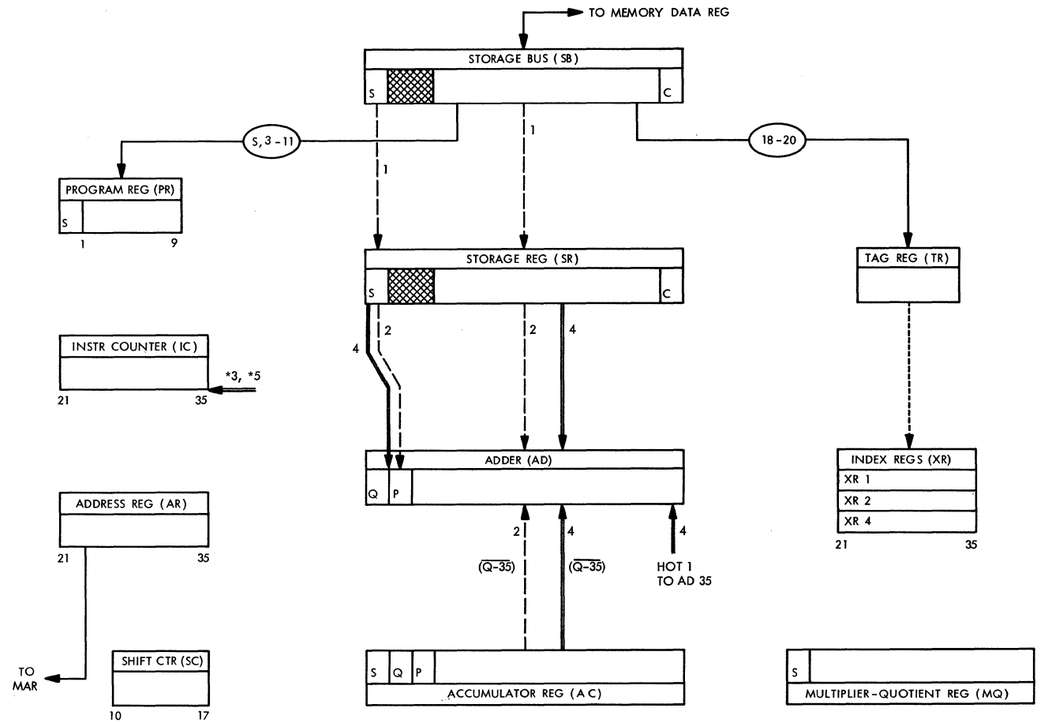
Compares the contents of the accumulator (Q,P,1-35) with the contents of the specified memory location (S,1-35). The accumulator is treated as an unsigned 37-bit number and the memory word is treated as an unsigned 36-bit number. If the accumulator is the greater, the computer takes the next sequential instruction. If the accumulator equals memory, the computer skips the next instruction and proceeds from there. If the accumulator is less than memory, the computer skips the next two instructions and proceeds from there.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

NOTE: THE EQUAL CONDITION EXISTS ONLY IF THERE WAS NO Q CARRY AT L1D1

FIGURE 24. LAS



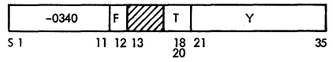
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0340 LOGICAL COMPARE ACCUMULATOR WITH STORAGE

ALPHA CODE: LAS CYCLES: I, E, (L)



SEQUENCE NOTES:

IF: $C(AC)_{Q, P, 1-35} > C(Y)_{S, 1-35}$, THE COMPUTER TAKES NEXT INSTRUCTION.

$C(AC)_{Q, P, 1-35} = C(Y)_{S, 1-35}$, THE COMPUTER SKIPS 1 INSTRUCTION.

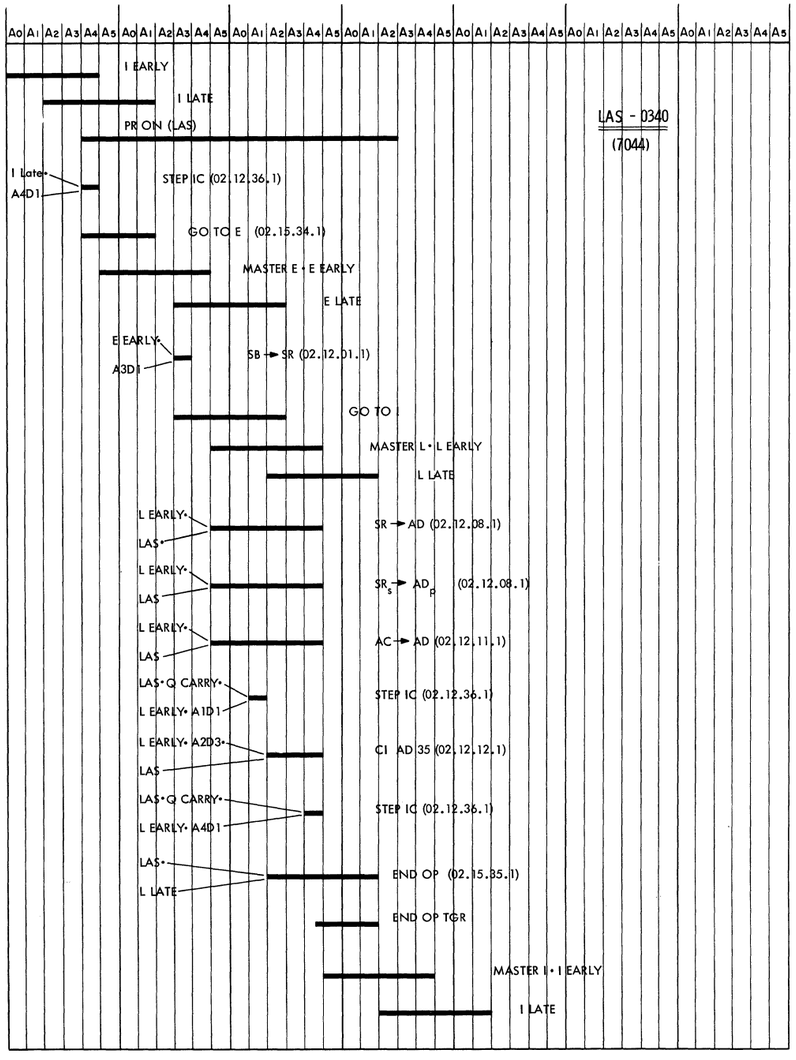
$C(AC)_{Q, P, 1-35} < C(Y)_{S, 1-35}$, THE COMPUTER SKIPS 2 INSTRUCTIONS.

THE AC IS TREATED AS AN UNSIGNED 37-BIT REGISTER.

THE C(Y) IS TREATED AS AN UNSIGNED 36-BIT REGISTER.

CYCLES REQUIRED: 7040: I, E
7044: I, E, L

*3, *5 (Q CAR)



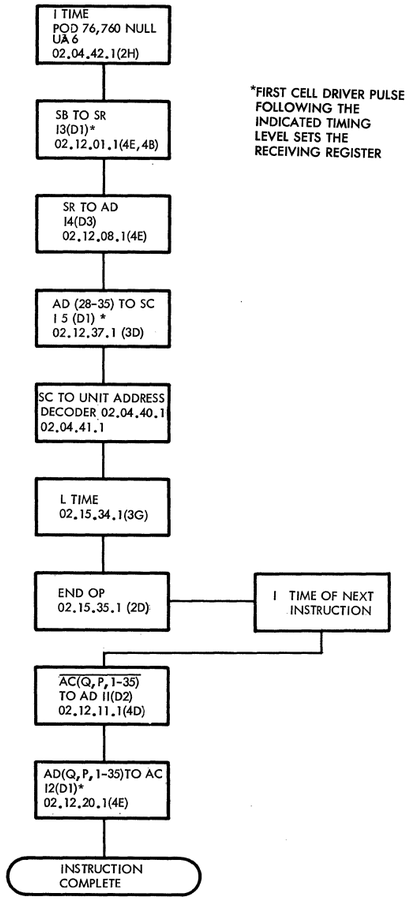
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	LAS		00006	434000 000006
00002	TRA		00000	002000 000000
00003				
00004				
00005	Pattern			377777 777777
00006	Pattern			377777 777776

Logical Compare Accumulator to Storage (LAS)

CONSOLE INDICATORS

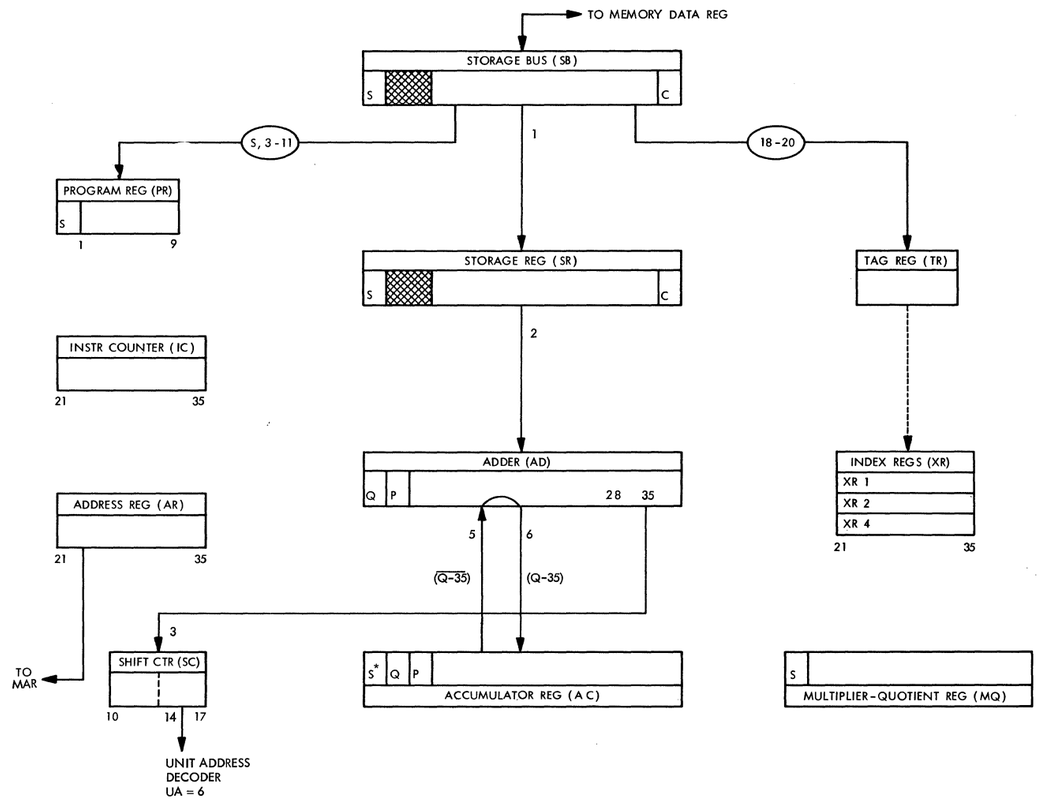
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00												
E	I	00001	+500	000	0	00001	377777777777	377777777777	00												
I	E	00002	-340	000	0	00006	434000000006	377777777777	00												
E	L	00002	-340	000	0	00006	377777777776	377777777777	00												
L	I	00002	-340	000	0	00002	377777777776	377777777777	00												
I	I	00003	+020	000	0	00000	002000000000	377777777777	00												
I	E	00001	+500	000	0	00005	0500u0000005	377777777777	00												

Complement Magnitude (COM +0760...0006)
Replaces all 1's with 0's, and all 0's with 1's, in the accumulator Q,P,1-35 positions. Accumulator sign is unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 25. COM



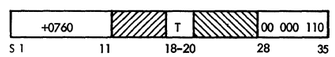
LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0760--6 COMPLEMENT MAGNITUDE

ALPHA CODE: COM CYCLES: I, (L)

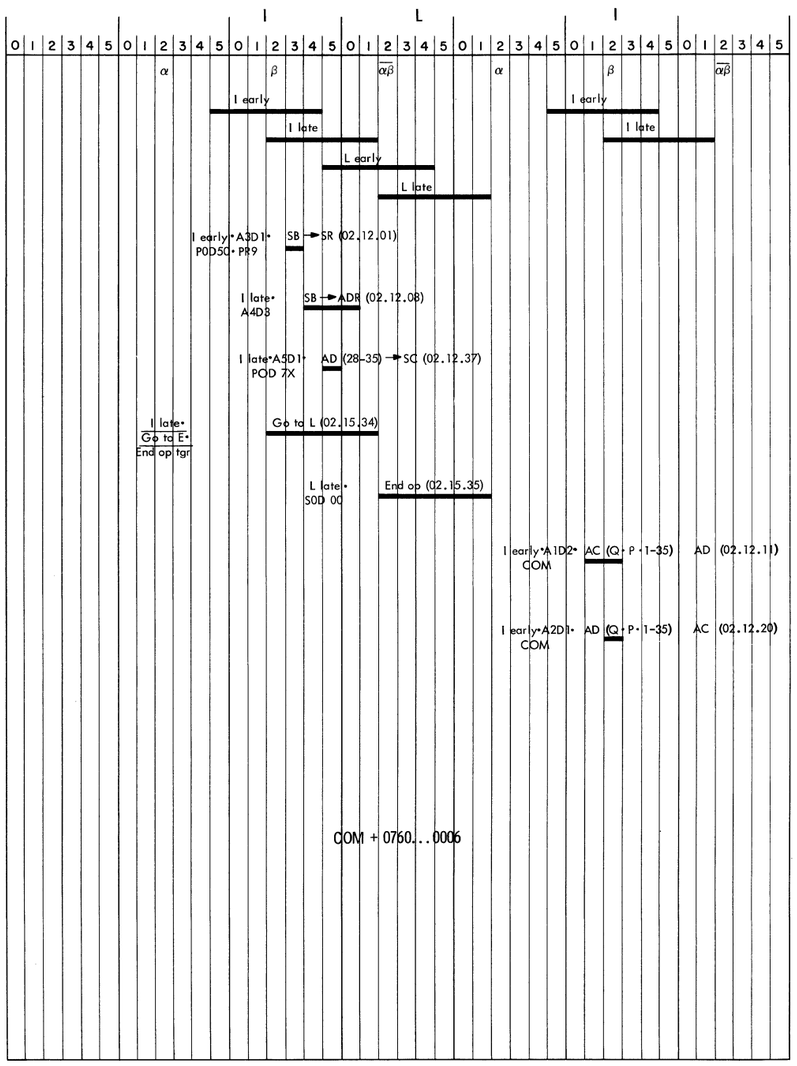


SEQUENCE NOTES:

THE $C(AC)_{Q,P,1-35}$ ARE COMPLEMENTED. THE AC(S) IS UNCHANGED.

INDEXING MAY CHANGE THE INSTRUCTION.

*SAVE AC(S)
CYCLES REQUIRED: 7040: I
7044: I, L



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	COM		00006	076000 000006
00002	TRA		00001	002000 000001
00003				
00004				
00005				
00006	Pattern			777777 777777

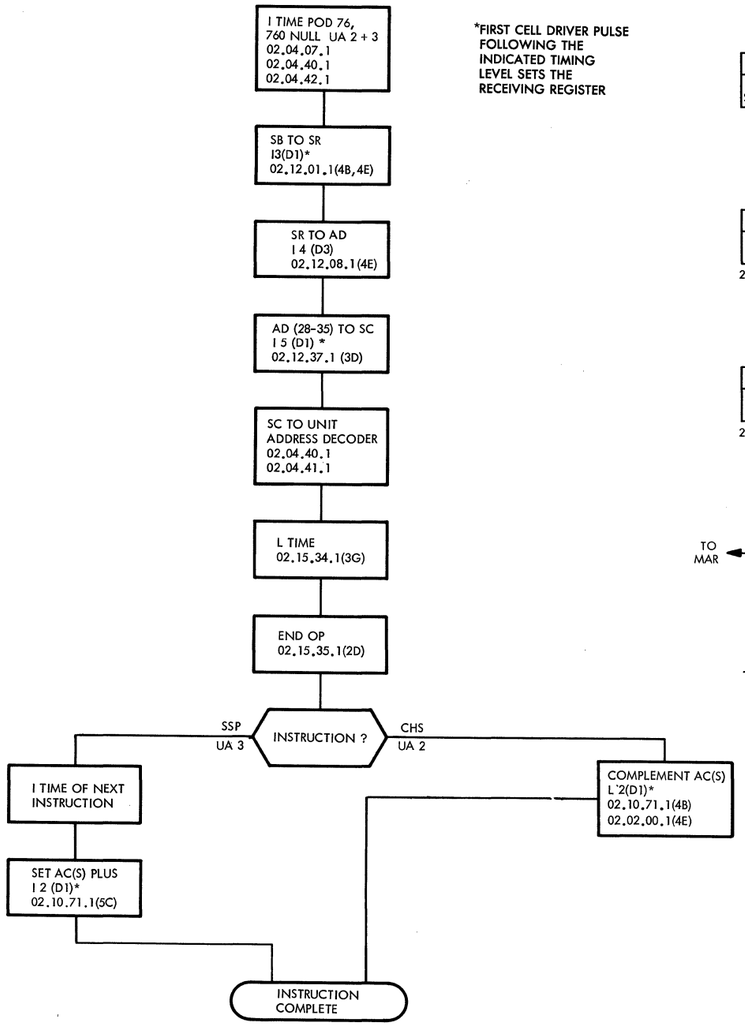
Complement Magnitude (COM)

CONSOLE INDICATORS

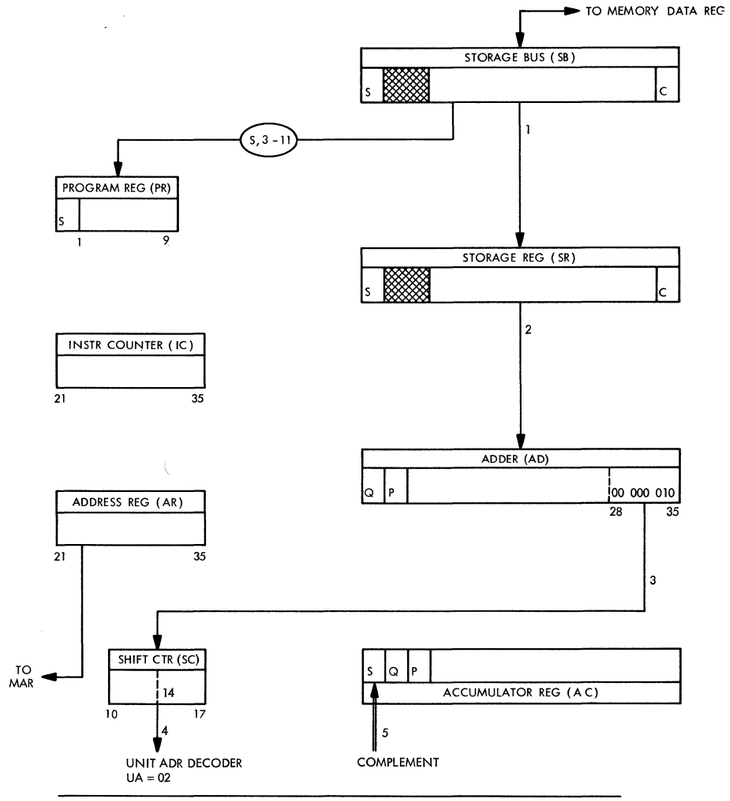
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9' OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000000	000000000000	00												
E	I	00001	+500	000	0	00001	777777777777	777777777777	00												
I	L	00002	+760	006	0	00006	076000000006	777777777777	00												
L	I	00002	+760	006	0	00002	076000000006	777777777777	00												
I	I	00003	+020	000	0	00001	002000000001	400000000000	11												
I	L	00002	+760	006	0	00006	076000000006	400000000000	11												
L	I	00002	+760	006	0	00002	076000000006	400000000000	11												
I	I	00003	+020	000	0	00001	002000000001	777777777777	00												
I	L	00002	+760	006	0	00006	076000000006	777777777777	00												
L	I	00002	+760	006	0	00002	076000000006	777777777777	00												

Change Sign (CHS +0760 ... 0002)
Makes the accumulator sign negative if it is plus, and plus if it is negative. The rest of the accumulator is unchanged.

Set Sign Plus (SSP +0760 ... 0003)
Sets the accumulator sign to plus.

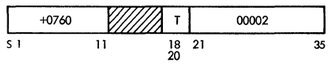


*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



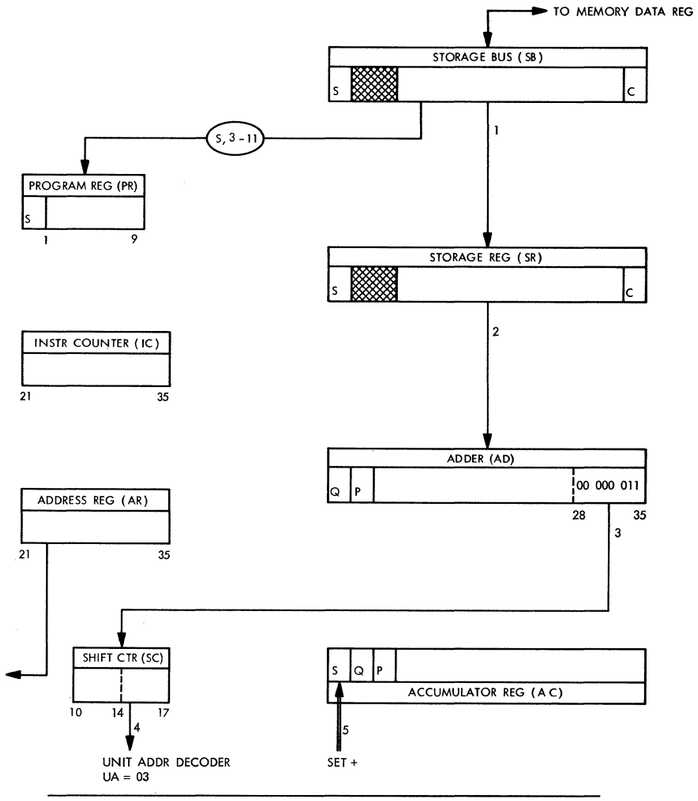
INST +0760--02 CHANGE SIGN

ALPHA CODE: CHS CYCLES: I (7040), I, L (7044)



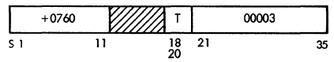
SEQUENCE NOTES:

CHANGE THE SIGN OF THE ACCUMULATOR. INDEXING MAY CHANGE THE OPERATION. THE $C(AC)_{Q,\ P,\ 1-35}$ ARE UNCHANGED.



INST +0760--03 SET SIGN PLUS

ALPHA CODE: SSP CYCLES: I (7040), I, L (7044)



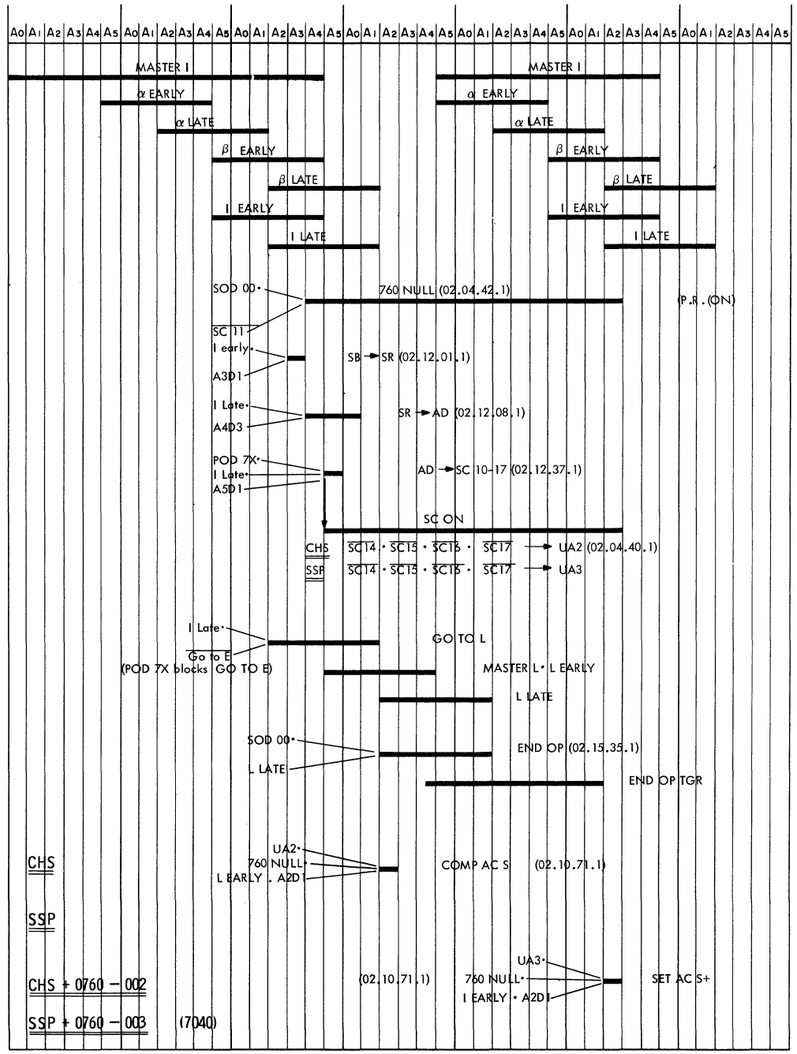
SEQUENCE NOTES:

THE SIGN OF THE AC IS SET TO PLUS (0).

INDEXING MAY CHANGE THE OPERATION.

THE $C(AC)_{Q,P,1-35}$ ARE UNCHANGED.

FIGURE 26. CHS, SSP



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	CHS		00002	076000 000002
00002	CHS		00002	076000 000002
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			377777 777777

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	SSP		00003	076000 000003
00002	SSP		00003	076000 000003
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			777777 777777

Change Sign (CHS)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00		
E	I	00001	+500	000	0	00001	377777777777	377777777777	00		
I	L	00002	+760	002	0	00002	076000000002	377777777777	00		
L	I	00002	+760	002	0	00002	076000000002	777777777777	00		
I	L	00003	+760	002	0	00002	076000000002	777777777777	00		
L	I	00003	+760	002	0	00003	076000000002	377777777777	00		
I	I	00004	+020	000	0	00000	002000000000	377777777777	00		
I	E	00001	+500	000	0	00006	050000000006	377777777777	00		

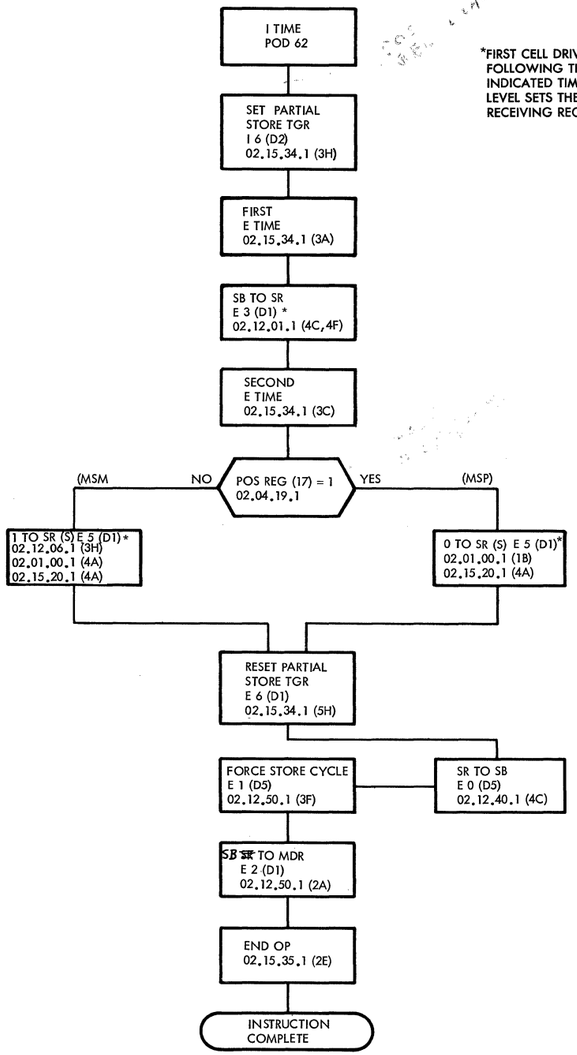
Set Sign Plus (SSP)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER
I	E	00001	+500	000	0	00006	050000000006	000000000000	00		
E	I	00001	+500	000	0	00001	777777777777	777777777777	00		
I	L	00002	+760	003	0	00003	076000000003	777777777777	00		
L	I	00002	+760	003	0	00002	076000000003	777777777777	00		
I	L	00003	+760	003	0	00003	076000000003	377777777777	00		
L	I	00003	+760	003	0	00003	076000000003	377777777777	00		
I	I	00004	+020	000	0	00000	002000000000	377777777777	00		
I	E	00001	+500	000	0	00006	050000000006	377777777777	00		

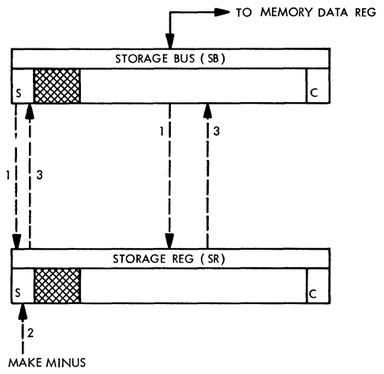
Make Storage Sign Minus (MSM -1623.6)
Makes the specified memory location sign minus. The rest of the memory word is unchanged.

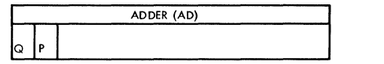
Make Storage Sign Plus (MSP -1623.7)
Makes the specified memory location sign plus. The rest of the memory word is unchanged.

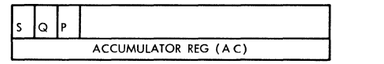


*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 27. MSM, MSP

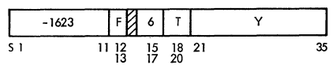






INST -1623--6 MAKE STORAGE SIGN MINUS

ALPHA CODE: MSM CYCLES: I, E, E

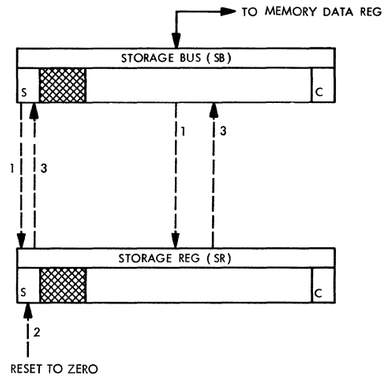


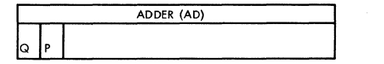
SEQUENCE NOTES:

THE SIGN BIT OF C(Y) IS REPLACED BY A 1 BIT (MINUS).

THE REMAINDER OF Y IS UNCHANGED.

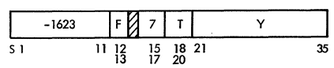
POSITIONS 15-17 MUST CONTAIN 6_8.





INST -1623--7 MAKE STORAGE SIGN PLUS

ALPHA CODE: MSP CYCLES: I, E, E

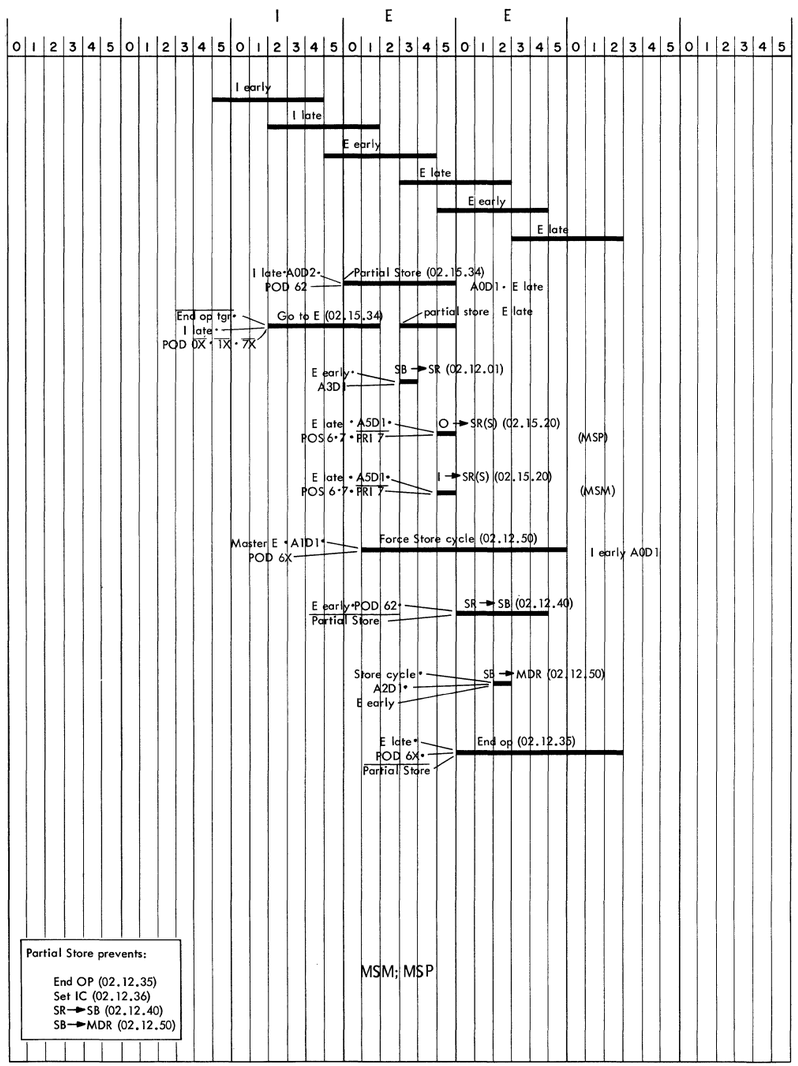


SEQUENCE NOTES:

THE SIGN BIT OF C(Y) IS REPLACED BY A ZERO BIT (PLUS).

THE REMAINDER OF Y IS UNCHANGED.

POSITIONS 15-17 MUST CONTAIN



Location Switches	Inst	Tag	Address	Octal Equiv
00000	MSM, 6		00007	562306 000007
00001	MIT, 6		00007	534106 000007
00002	HPR			042000 000000
00003	TRA		00000	002000 000000

Make Storage Sign Minus (MSM)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E(1)	00001	-623	000	0	00007	562306000007					15 16									
E(1)	E(2)	00001	-623	000	0	00007	400000000000					15 16									
E(2)	I	00001	-623	000	0	00001	400000000000					15 16									
I	E	00002	-341	000	0	00007	543106000007					15 16									
E	L	00002	-341	000	0	00007	400000000000					15 16									
L	I	00003	-341	000	0	00003	400000000000					15 16					1				
I	I	00004	+020	000	0	00000	002000000000														

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	MSP, 7		00007	562307 000007
00003	PLT, 7		00007	534107 000007
00004	HPR			042000 000000
00005	TRA		00000	002000 000000
00006	Pattern			400000 000000

Make Storage Sign Plus (MSP)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	400000000000	400000000000	00												
I	E	00002	+601	000	0	00007	060100000007	400000000000	00												
E	I	00002	+601	000	0	00002	400000000000	400000000000	00												
I	E(1)	00003	-623	000	0	00007	562307000007	400000000000	00				16 17 15								
E(1)	E(2)	00003	-623	000	0	00007	000000000000	400000000000	00				16 17 15								
E(2)	I	00003	-623	000	0	00003	000000000000	400000000000	00				16 17 15								
I	E	00004	-341	000	0	00007	534107000007	400000000000	00				16 17 15								
E	L	00004	-341	000	0	00007	000000000000	400000000000	00				16 17 15								
L	I	00005	-341	000	0	00005	000000000000	400000000000	00				16 17 15				1				
I	I	00006	+020	000	0	00000	002000000000	400000000000	00												
E	E	00001	+500	000	0	00006	050000000006	400000000000	00												

Low-Order Bit Test (LBT +0760 ... 0001)
If accumulator bit 35 is a 1, the computer skips the next instruction. If bit 35 is a 0, the computer takes the next sequential instruction.

P-Bit Test (PBT -0760 ... 0001)
If accumulator P-bit is a 1, the computer skips the next instruction. If the P-bit is a zero, the computer takes the next sequential instruction.

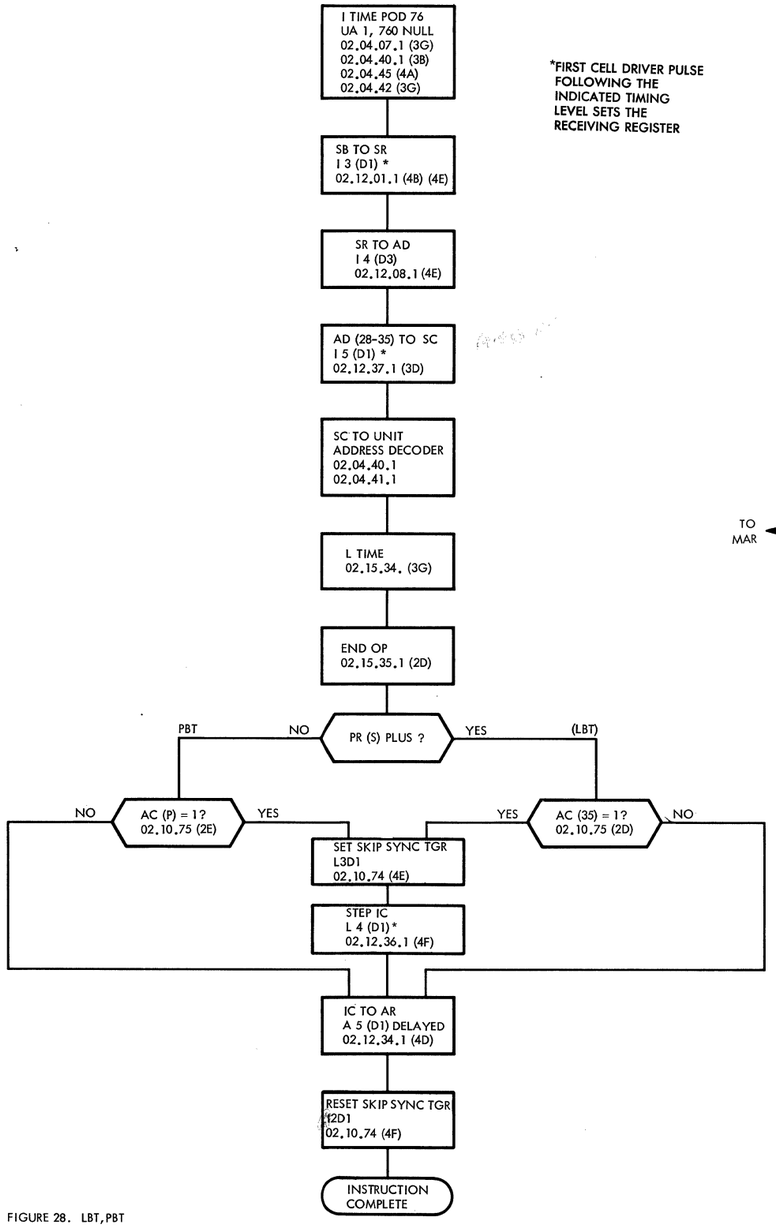
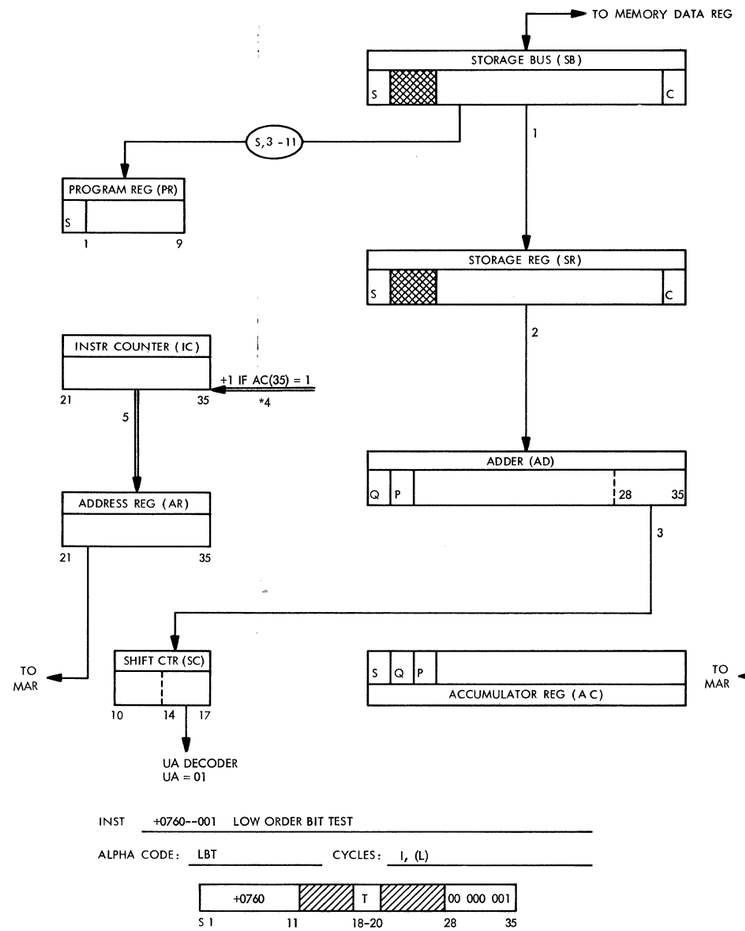


FIGURE 28. LBT, PBT

*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



INST +0760--001 LOW ORDER BIT TEST

ALPHA CODE: LBT CYCLES: I, (L)

SEQUENCE NOTES:

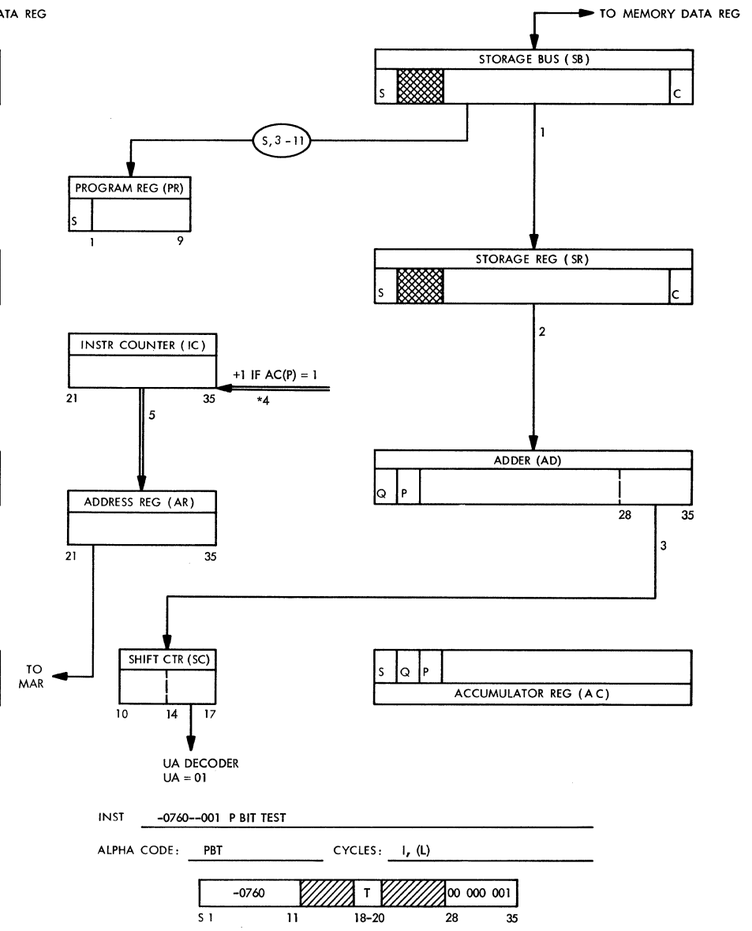
IF AC(35) = 1, THE COMPUTER SKIPS THE NEXT INSTRUCTION AND CONTINUES.

IF AC(35) = 0, THE COMPUTER TAKES THE NEXT SEQUENTIAL INSTRUCTION.

INDEXING MAY CHANGE THE INSTRUCTION.

*4 STEP I. C. BY 1 IF AC(35) = 1.

CYCLES REQUIRED: 7040: I
7044: I, L



INST -0760--001 P BIT TEST

ALPHA CODE: PBT CYCLES: I, (L)

SEQUENCE NOTES:

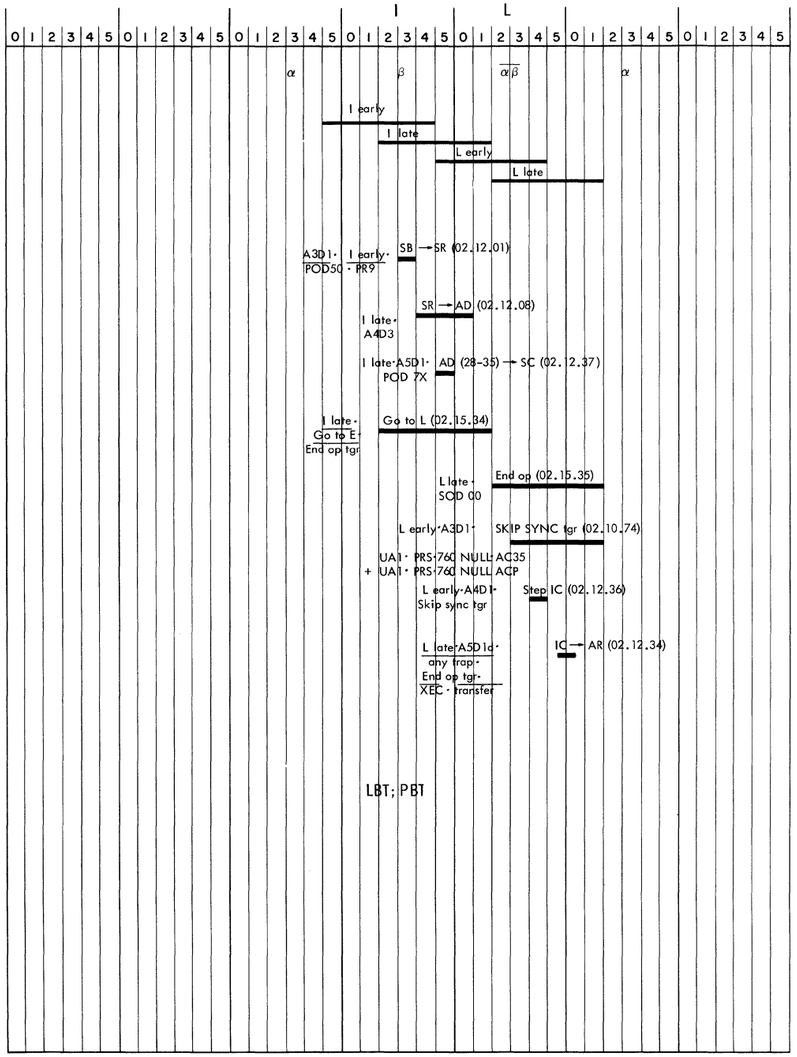
IF AC(P) = 1, THE COMPUTER SKIPS THE NEXT INSTRUCTION AND CONTINUES.

IF AC(P) = 0, THE COMPUTER TAKES THE NEXT SEQUENTIAL INSTRUCTION.

INDEXING MAY CHANGE THE INSTRUCTION.

*4. STEP I. C. BY 1 IF AC(P) = 1.

CYCLES REQUIRED: 7040: I
7044: I, L



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	LBT		00001	076000 000001
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			000000 000001

Low-Order Bit Test (LBT)

		CONSOLE INDICATORS																		
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	000000000001	000000000001	00												
I	L	00002	+760	001	0	00001	076000000001	000000000001	00												
L	I	00003	+760	001	0	00003	076000000001	000000000001	00												
I	I	00004	+020	000	0	00000	002000000000	000000000001	00												
I	E	00001	+500	000	0	00006	050000000006	000000000001	00												

NOTE: If Bit 35 in the accumulator equals zero, this routine hangs up with cycle time L Indicator ON.

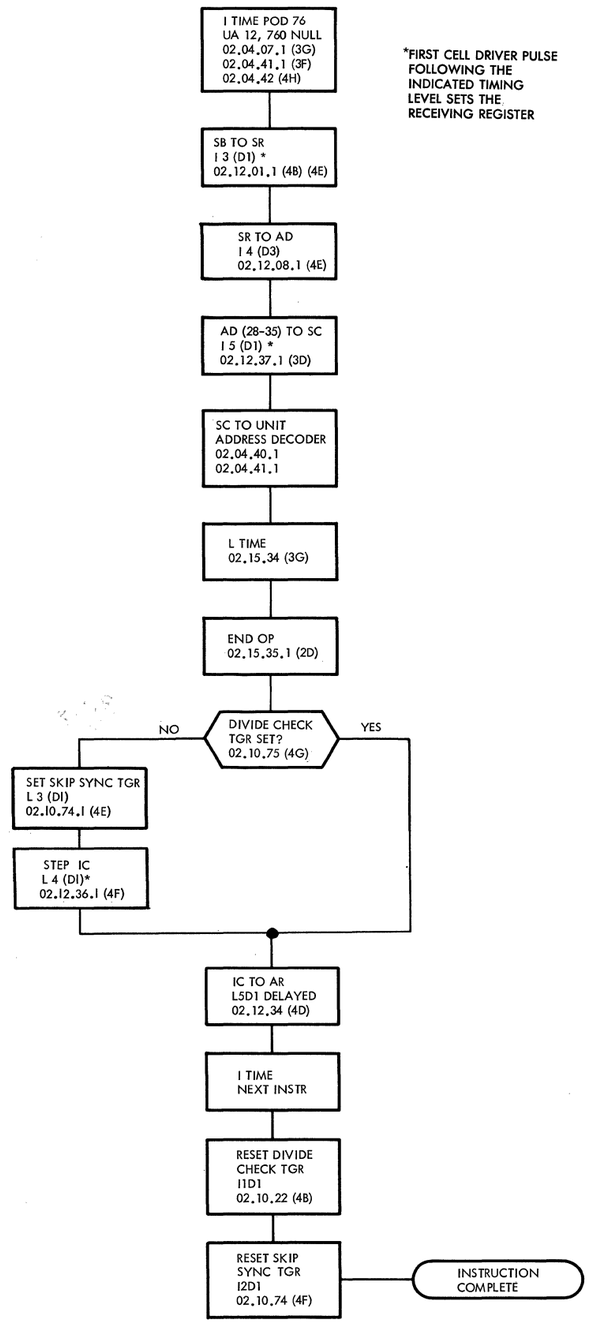
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CAL		00006	450000 000006
00001	PBT		00001	476000 000001
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			400000 000000

P-Bit Test (PBT)

		CONSOLE INDICATORS																		
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	-500	000	0	00006	450000000006	000000000000	00												
E	I	00001	-500	000	0	00001	400000000000	000000000000	01												
I	L	00002	-760	001	0	00001	476000000001	000000000000	01												
L	I	00003	-760	001	0	00003	476000000001	000000000000	01												
I	I	00004	+020	000	0	00000	002000000000	000000000000	01												
I	E	00001	-500	000	0	00006	450000000006	000000000000	01												

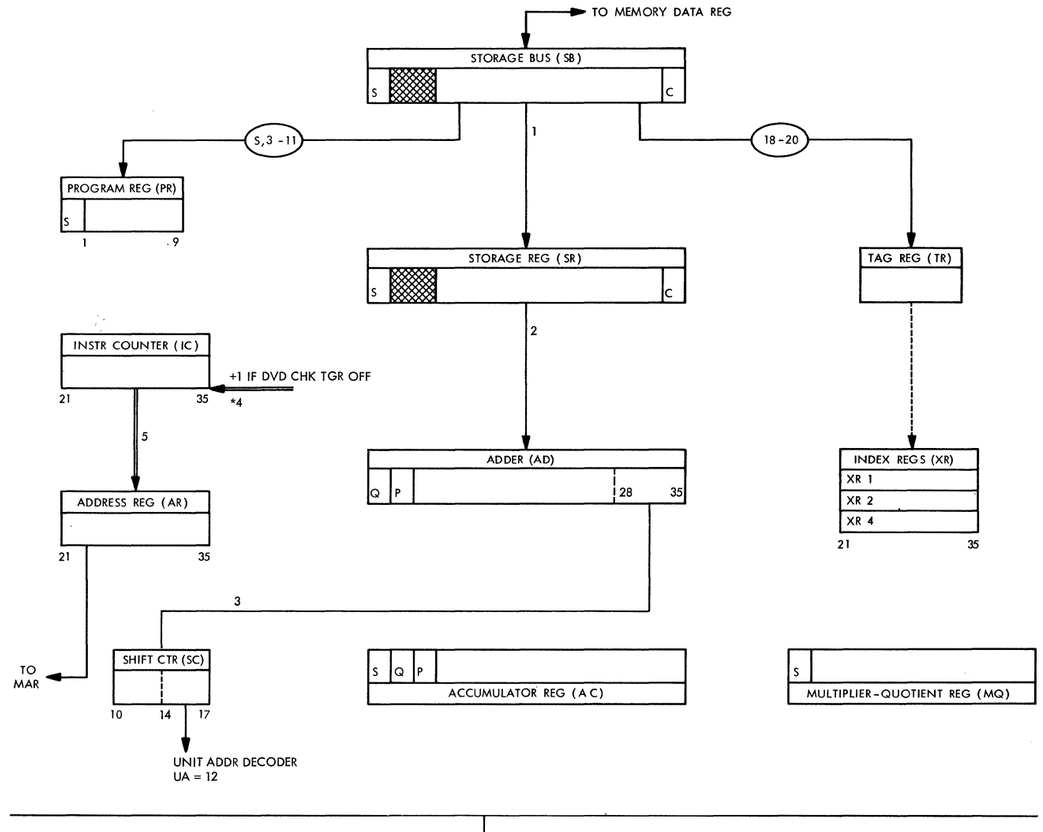
NOTE: If P-Bit equals zero, this routine hangs up with cycle time L indicator on.

Divide Check Test (DCT +0760 ... 0012)
If the divide check indicator is on, it is turned off and the computer takes the next sequential instruction. If the divide check indicator is off, the computer skips the next instruction.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 29. DCT



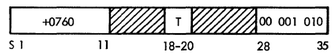
LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0760--012 DIVIDE CHECK TEST

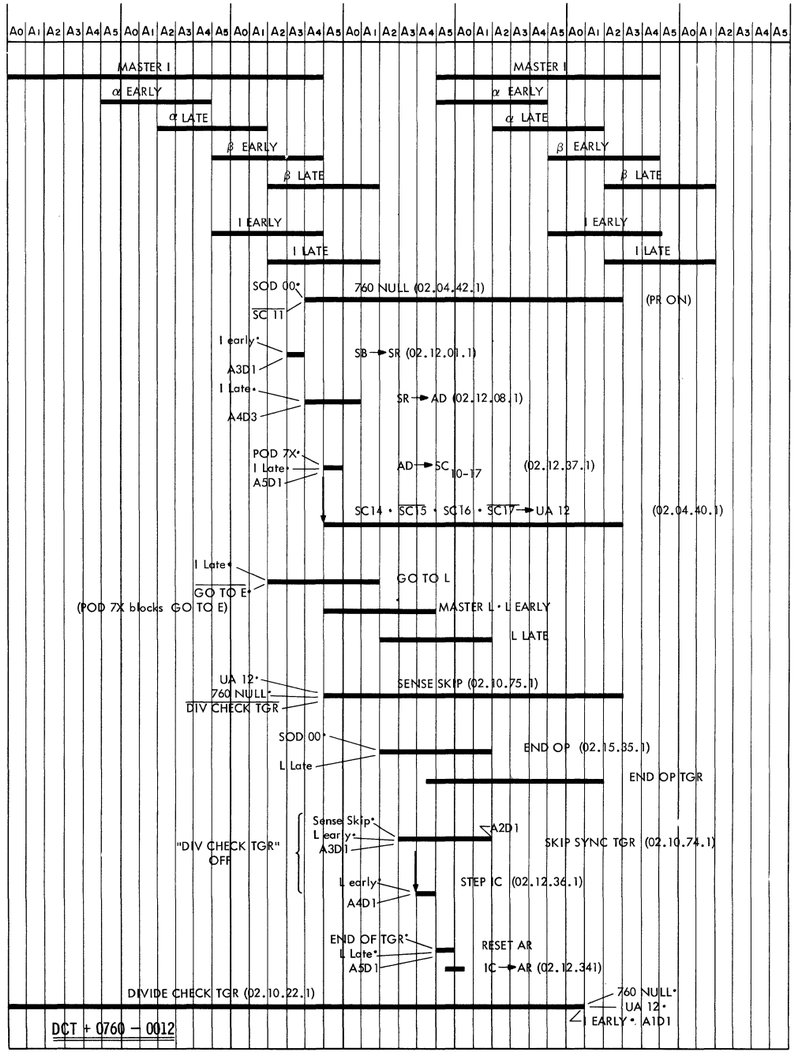
ALPHA CODE: DCT CYCLES: I, (L)



SEQUENCE NOTES:

IF THE DVD CHK INDICATOR IS ON, THE INDICATOR IS TURNED OFF AND THE COMPUTER TAKES THE NEXT SEQUENTIAL INSTRUCTION. IF THE INDICATOR IF OFF, THE COMPUTER SKIPS THE NEXT INSTRUCTION AND CONTINUES. INDEXING MAY CHANGE THE INSTRUCTION.

CYCLES REQUIRED: 7040: I
7044: I, L



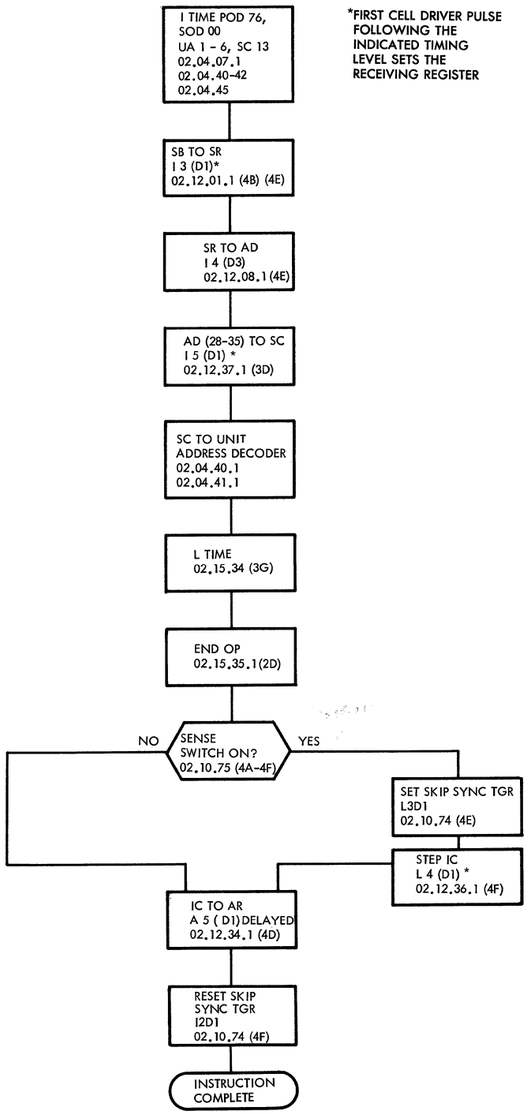
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	DVP		00006	022100 000006
00002	DCT		00012	076000 000012
00003	TRA		00000	002000 000000
00004	HPR		00000	042000 000000
00005	Pattern			200000 000000
00006	Pattern			100000 000000

Divide Check Test (DCT)

CONSOLE INDICATORS

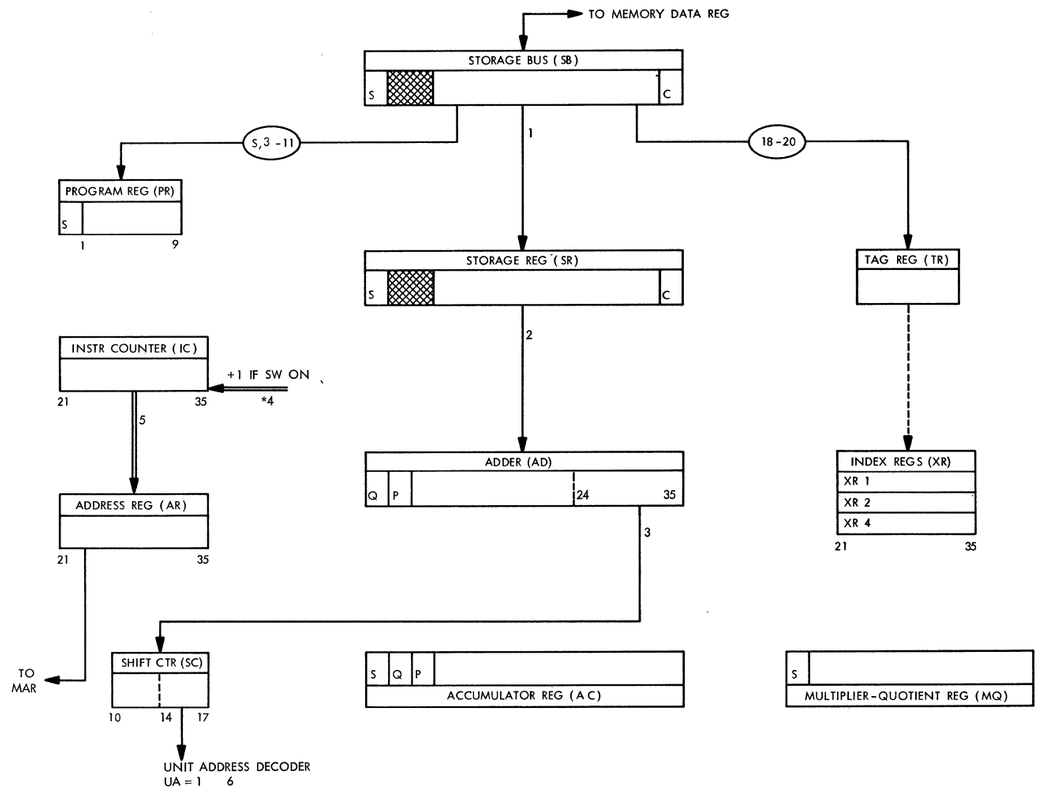
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	200000000000	200000000000	00	000000000000											
I	E	00002	+221	000	0	00006	022100000006	200000000000	00	000000000000											
E	L	00002	+221	000	0	00006	100000000000	177777777777	11	000000000000					1						
L	I	00002	+221	000	0	00002	100000000000	177777777777	11	000000000000					1						
I	L	00003	+760	012	0	00012	076000000012	200000000000	00	000000000000					1						
L	I	00003	+760	012	0	00003	076000000012	200000000000	00	000000000000					1						
I	I	00004	+020	000	0	00000	002000000000	200000000000	00	000000000000					0						
I	E	00001	+500	000	0	00005	050000000005	200000000000	00	000000000000					0						

Sense Switch Test (SWT +0760 ... 0161 to 0166)
If the switch tested is off, the computer takes the next sequential instruction.
If the switch is on, the computer skips the next instruction.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 30. SWT



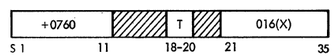
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST 0161 +0760--0166 SENSE SWITCH TEST

ALPHA CODE: SWT CYCLES: I, (L)



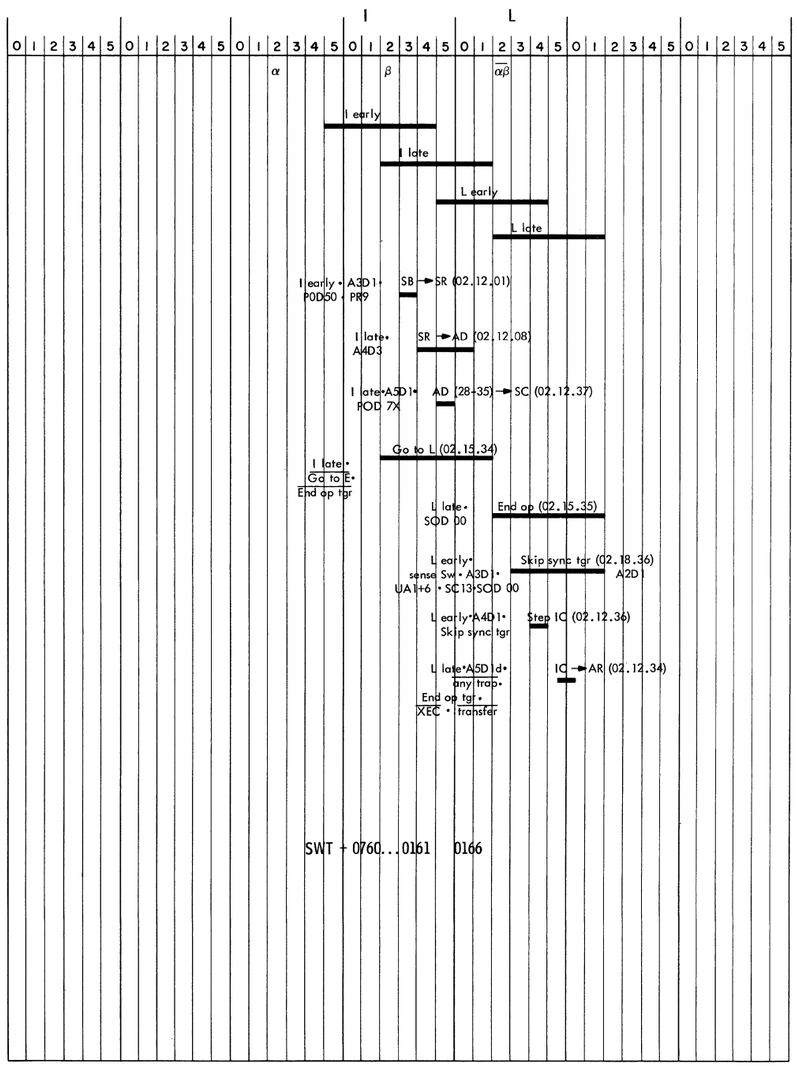
SEQUENCE NOTES:

IF SENSE SWITCH IS ON (1-6), THE COMPUTER SKIPS THE NEXT INSTRUCTION AND CONTINUES.

IF THE SWITCH IS OFF, THE COMPUTER TAKES THE NEXT SEQUENTIAL INSTRUCTION.

INDEXING MAY CHANGE THE INSTRUCTION.

CYCLES REQUIRED: 7040: I
7044: I, L



Location Switches	Inst	Tag	Address	Octal Equiv
00000	SWT		00161	076000 000161
00001	TRA		00000	002000 000000
00002	ADD		00004	040000 000004
00003	TRA		00000	002000 000000
00004	Pattern			000000 000001

Sense Switch Test (SWT)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	L	00001	+760	161	0	00161	076000000161														
L	I	00001	+760	161	0	00001	076000000161			SS#1 OFF											
I	I	00002	+020	000	0	00000	002000000000														
I	L	00001	+760	161	0	00161	076000000161	000000000000	*												
L	I	00002	+760	161	0	00002	076000000161	000000000000													
I	E	00003	+400	000	0	00004	040000000004	000000000000		SS#1 ON											
E	I	00003	+400	000	0	00003	000000000001	000000000001	*												
I	I	00004	+020	000	0	00000	002000000000	000000000000	*												

*Accumulator is increased by one for each pass.

Storage Minus Test (MIT -1341.6)
If the sign of the specified memory location is minus, the computer skips the next instruction. If the sign is plus, the computer takes the next instruction.

Storage Plus Test (PLT -1341.7)
If the sign of the specified memory location is plus, the computer skips the next instruction. If the sign is minus, the computer takes the next instruction.

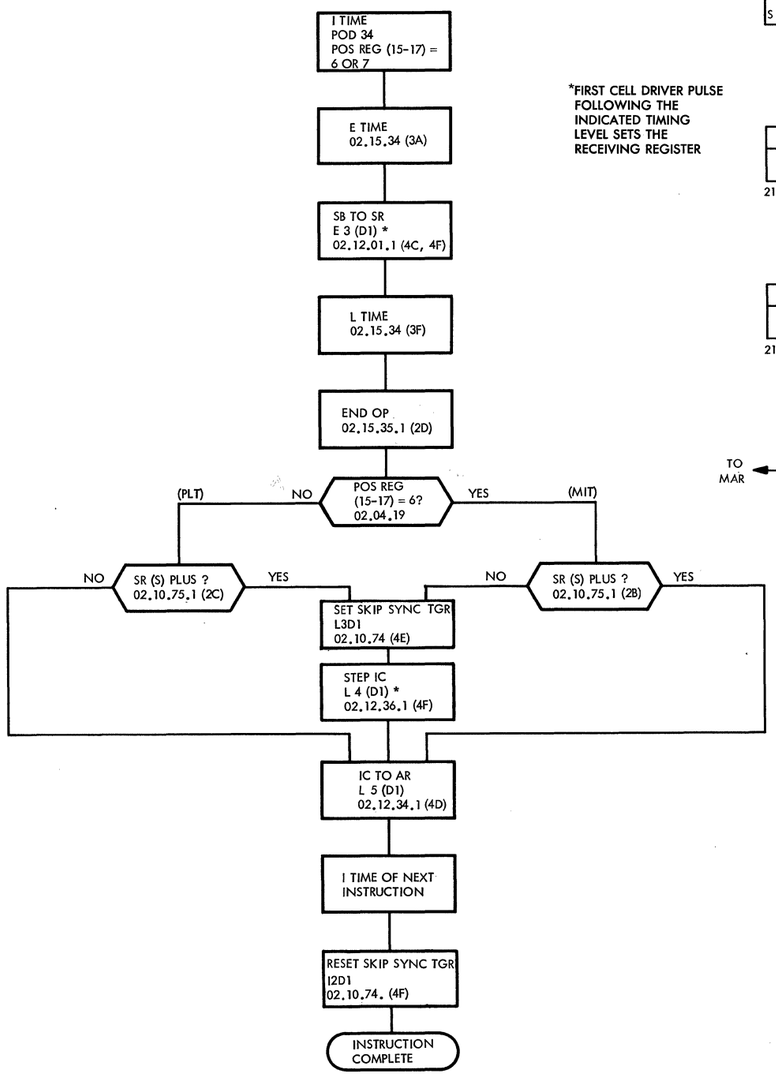
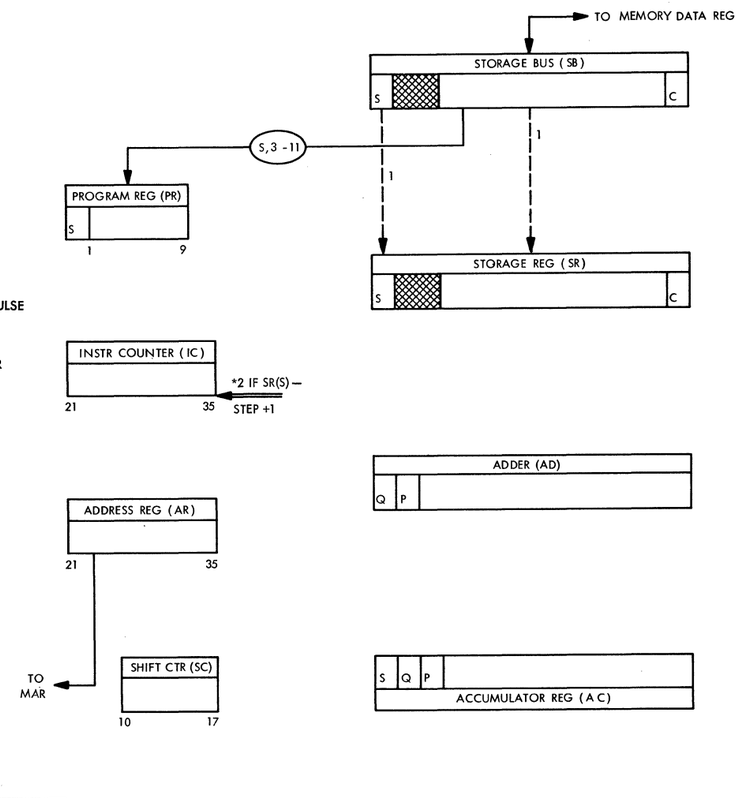


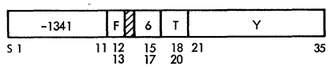
FIGURE 31. MIT, PLT

*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



INST -1341--6 STORAGE MINUS TEST

ALPHA CODE: MIT CYCLES: I, E, (L)

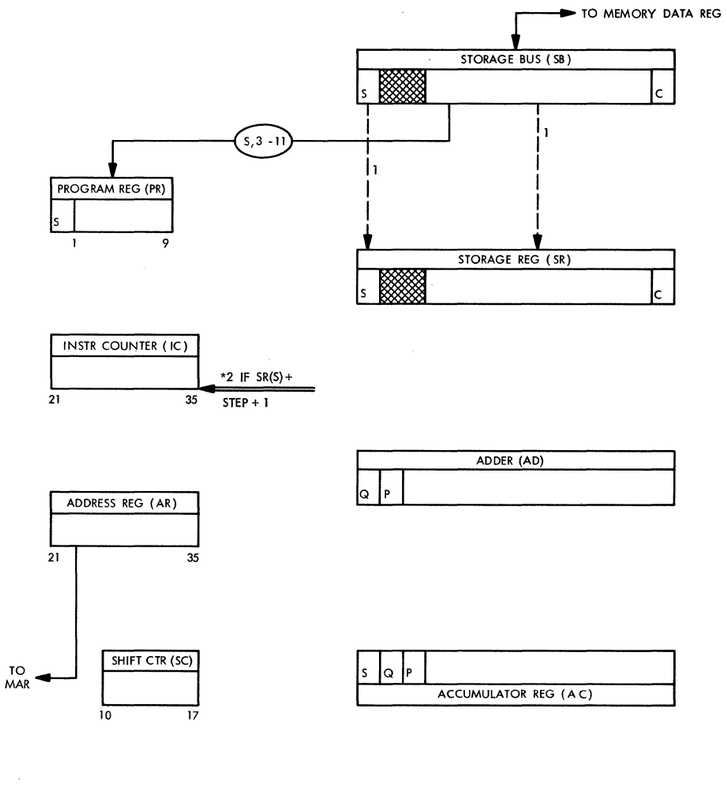


SEQUENCE NOTES:

IF THE SIGN OF LOCATION Y IS MINUS, THE COMPUTER SKIPS THE NEXT INSTRUCTION.

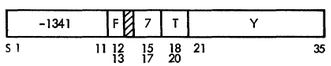
IF THE SIGN IS PLUS, TAKE THE NEXT INSTRUCTION.

CYCLES REQUIRED: 7040: I, E
7044: I, E, L



INST -1341--7 STORAGE PLUS TEST

ALPHA CODE: PLT CYCLES: I, E, (L)

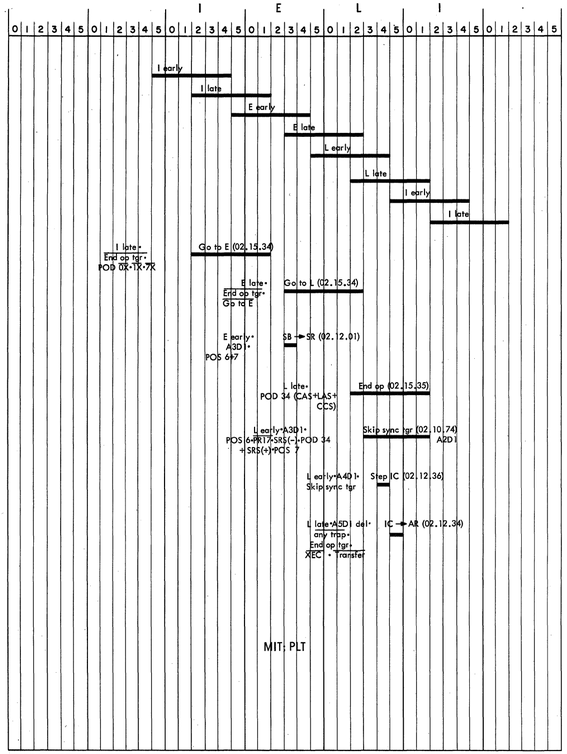


SEQUENCE NOTES:

IF THE SIGN OF LOCATION Y IS PLUS, THE COMPUTER SKIPS THE NEXT INSTRUCTION.

IF THE SIGN IS MINUS, TAKE THE NEXT INSTRUCTION.

CYCLES REQUIRED: 7040: I, E
7044: I, E, L



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	MIT		00007	534106 000007
00003	HPR			042000 000000
00004	TRA		00000	002000 000000
00005				
00006	Pattern			400000 000000

Storage Minus Test (MIT)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF1	FF2
E	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	400000000000	400000000000	00												
I	E	00002	+601	000	0	00007	060100000007	400000000000	00												
E	I	00002	+601	000	0	00002	400000000000	400000000000	00												
I	E	00003	-341	000	0	00007	534106000007	400000000000	00			16 15&									
E	L	00003	-341	000	0	00007	400000000000	400000000000	00			16 15&									
L	I	00004	-341	000	0	00004	400000000000	400000000000	00			16 15&					1				
I	I	00005	+020	000	0	00000	002000000000	400000000000	00								0				
I	E	00001	+500	000	0	00006	050000000006	400000000000	00												

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	STO		00007	060100 000007
00002	PLT		00007	534107 000007
00003	HPR			042000 000000
00004	TRA		00000	002000 000000
00005	TRA		00000	002000 000000
00006	Pattern			000000 000000

Storage Plus Test (PLT)

CONSOLE INDICATORS

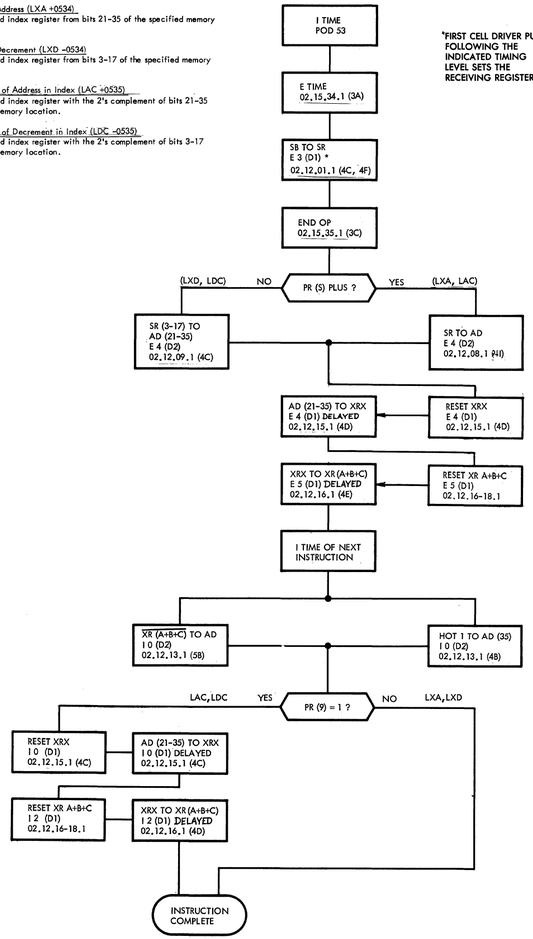
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF1	FF2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	000000000000	000000000000	00												
I	E	00002	+601	000	0	00007	060100000007	000000000000	00												
E	I	00002	+601	000	0	00002	000000000000	000000000000	00												
I	E	00003	-341	000	0	00007	534107000007	000000000000	00			16 17 15									
E	L	00003	-341	000	0	00007	000000000000	000000000000	00			16 17 15									
L	I	00004	-341	000	0	00004	000000000000	000000000000	00			16 17 15					1				
I	I	00005	+020	000	0	00000	002000000000	000000000000	00								0				

Load Index from Address (LXA +0534)
Loads the specified index register from bits 21-35 of the specified memory location.

Load Index from Decrement (LXD -0534)
Loads the specified index register from bits 3-17 of the specified memory location.

Load Complement of Address in Index (LAC +0535)
Loads the specified index register with the 2's complement of bits 21-35 of the specified memory location.

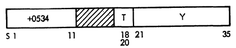
Load Complement of Decrement in Index (LDC -0535)
Loads the specified index register with the 2's complement of bits 3-17 of the specified memory location.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

INST +0534 LOAD INDEX FROM ADDRESS

ALPHA CODE: LXA CYCLES: I, E

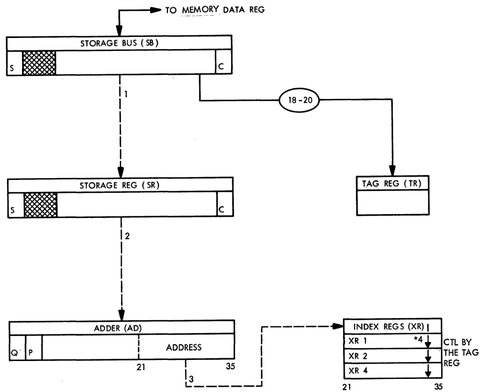


SEQUENCE NOTES:

THE SPECIFIED IX REGISTER(S) IS LOADED WITH THE $C(Y)_{21-35}$.

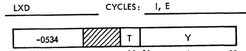
THE C(Y) ARE UNCHANGED.

A TAG OF ZERO RESULTS IN A NO-OP.



INST -0534 LOAD INDEX FROM DECREMENT

ALPHA CODE: LXD CYCLES: I, E

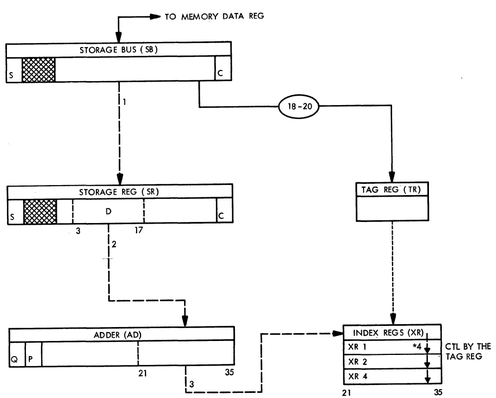


SEQUENCE NOTES:

THE SPECIFIED IX REGISTER(S) IS LOADED WITH THE $C(Y)_{3-17}$.

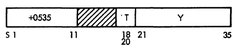
THE C(Y) ARE UNCHANGED.

A TAG OF ZERO RESULTS IN A NO-OP.



INST +0535 LOAD COMPLEMENT OF ADDRESS IN INDEX

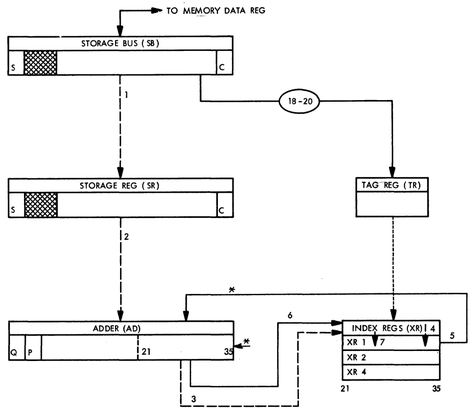
ALPHA CODE: LAC CYCLES: I, E



SEQUENCE NOTES:

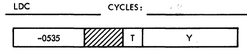
THE SPECIFIED INDEX REGISTER(S) IS LOADED WITH THE 2'S COMPLEMENT OF $C(Y)_{21-35}$. THE C(Y) ARE UNCHANGED. A TAG OF ZERO RESULTS IN A NO-OP.

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2'S COMPLEMENT



INST -0535 LOAD COMPLEMENT OF DECREMENT IN INDEX

ALPHA CODE: LDC CYCLES:



SEQUENCE NOTES:

THE SPECIFIED INDEX REGISTER(S) IS LOADED WITH THE 2'S COMPLEMENT OF $C(Y)_{3-17}$. THE C(Y) ARE UNCHANGED. A TAG OF ZERO RESULTS IN A NO-OP.

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2'S COMPLEMENT

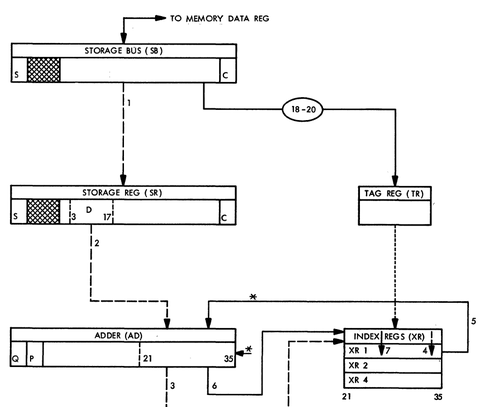
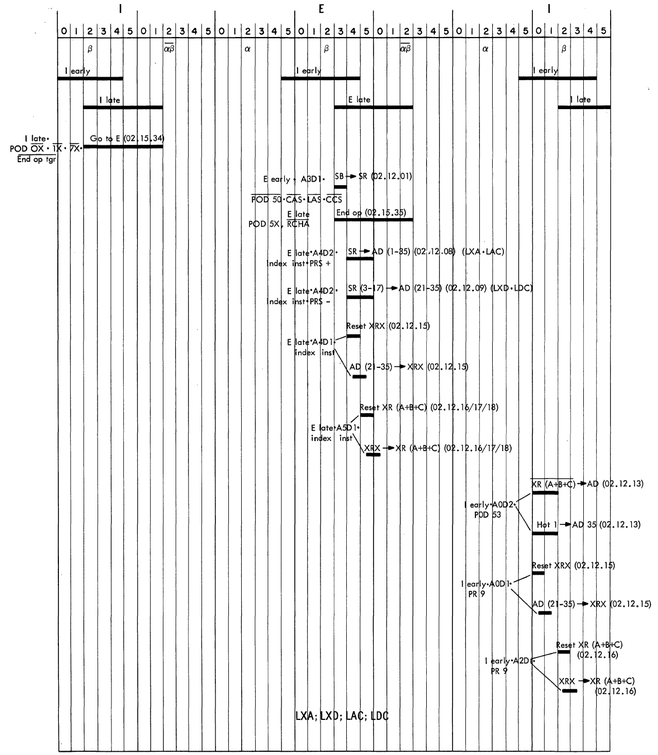


FIGURE 32. LXA, LXD, LAC, LDC



Location Switches	Inst	Tag	Address	Octal Equiv
00000	LXA	4*	00006	053400 400006
00001	LXA	4*	00007	053400 400007
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			000000 077777
00007	Pattern			000000 000000

*Change tag to test remaining index registers.

Load Index from Address (LXA)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER C	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF 1	FF 2
I	E	00001	+534	000	4	00006	053400400006					00000									
E	I	00001	+534	000	4	00001	000000077777					77777									
I	E	00002	+534	000	4	00007	053400400007					77777									
E	I	00002	+534	000	4	00002	000000000000					00000									
I	I	00003	+020	000	0	00000	002000000000					00000									

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LXD	3*	00006	453400 300006
00001	LXD	3*	00007	453400 300007
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006				077777 000000
00007				000000 000000

*Change tag to test remaining index register.

Load Index from Decrement (LXD)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A &B	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF 1	FF 2
I	E	00001	-534	000	3	00006	453400300006					00000									
E	I	00001	-534	000	3	00001	077777000000					77777									
I	E	00002	-534	000	3	00007	453400300007					77777									
E	I	00002	-534	000	3	00002	000000000000					00000									
I	I	00003	+020	000	0	00000	002000000000					00000									

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LAC	6*	00006	053500 600006
00001	TRA	0	00000	002000 000000
00002				
00003				
00004				
00005				
00006	Pattern			000000 000001

*Change tag to test remaining index register.

Load Complement of Address in Index (LAC)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS B & C	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF 1	FF 2
I	E	00001	+535	000	6	00006	053500600006					00000									
E	I	00001	+535	000	6	00001	000000000001					00001									
I	I	00002	+020	000	0	00000	002000000000					77777									
I	E	00001	+535	000	6	00006	053500600006					77777									

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDC	5*	00006	453500 000006
00001	TRA		00000	002000 000000
00002				
00003				
00004				
00005				
00006	Pattern			000001 000000

*Change tag to test remaining index register.

Load Complement of Decrement in Index (LDC)

CONSOLE INDICATORS

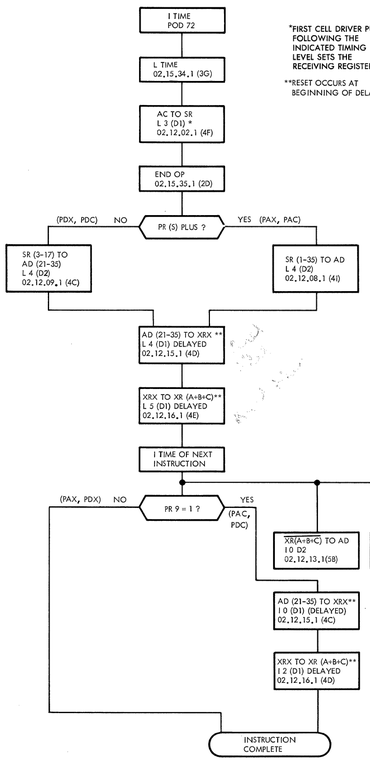
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A &C	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF 1	FF 2
I	E	00001	-535	000	5	00006	453500500006					00000									
E	I	00001	-535	000	5	00001	000001000000					00001									
I	I	00002	+020	000	0	00000	002000000000					77777									
I	E	00001	-535	000	5	00006	453500500006					77777									

Place Address in Index (PAX +0734)
Places accumulator bits 21-35 into the specified index register. The accumulator is unchanged.

Place Decrement in Index (PDX -0734)
Places accumulator bits 3-17 into the specified index register. The accumulator is unchanged.

Place Complement of Address in Index (PAC +0737)
Places the 2's complement of accumulator bits 21-35 into the specified index register. The accumulator is unchanged.

Place Complement of Decrement in Index (PDC -0737)
Places the 2's complement of accumulator bits 3-17 into the specified index register. The accumulator is unchanged.



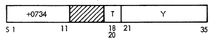
*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

**RESET OCCURS AT BEGINNING OF DELAY

FIGURE 33. PAX, PDX, PAC, PDC

INST +0734 PLACE ADDRESS IN INDEX

ALPHA CODE: PAX CYCLES: I, (L)



SEQUENCE NOTES:

THE $C(AC)_{21-35}$ ARE PLACED INTO THE SPECIFIED INDEX REGISTER(S).

THE C(AC) ARE UNCHANGED.

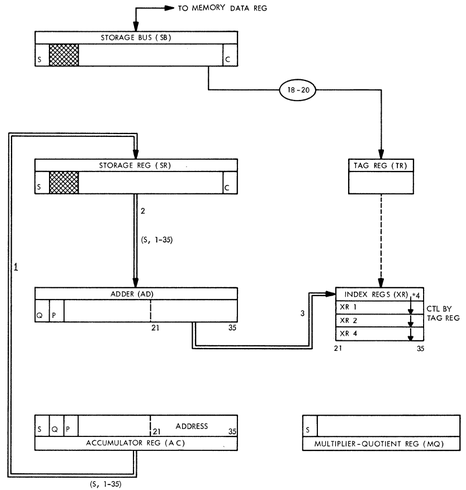
A TAG OF ZERO RESULTS IN A NO-OP.

CYCLES REQUIRED: 7040: I
7044: I, L

LEGEND

I CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.



INST -0734 PLACE DECREMENT IN INDEX

ALPHA CODE: PDX CYCLES: I,(L)

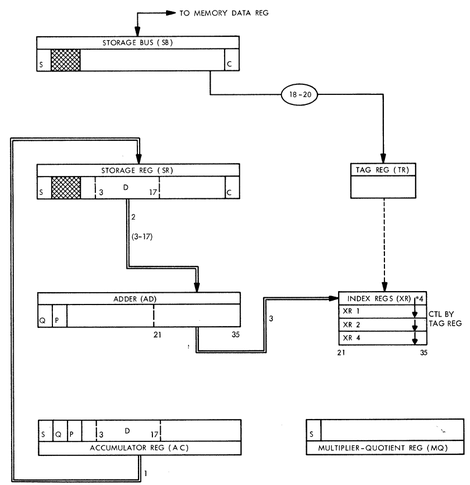
SEQUENCE NOTES:

THE $C(AC)_{3-17}$ ARE PLACED INTO THE SPECIFIED INDEX REGISTERS.

THE C(AC) ARE UNCHANGED.

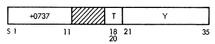
A TAG OF ZERO RESULTS IN A NO-OP.

CYCLES REQUIRED: 7040: I
7044: I



INST +0737 PLACE COMPLEMENT OF ADDRESS IN INDEX

ALPHA CODE: PAC CYCLES: I, (L)



SEQUENCE NOTES:

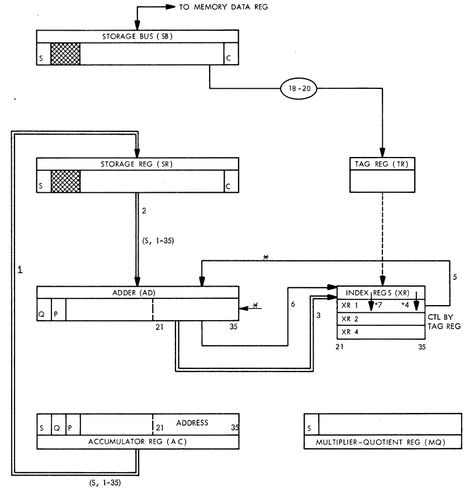
THE 2'S COMPLEMENT OF $C(AC)_{21-35}$ ARE PLACED INTO THE SPECIFIED INDEX REGISTER(S).

THE C(AC) ARE UNCHANGED.

A TAG OF ZERO RESULTS IN A NO-OP.

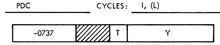
CYCLES REQUIRED: 7040: I
7044: I, L

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2'S COMPLEMENT.



INST -0737 PLACE COMPLEMENT OF DECREMENT IN INDEX

ALPHA CODE: PDC CYCLES: I, (L)



SEQUENCE NOTES:

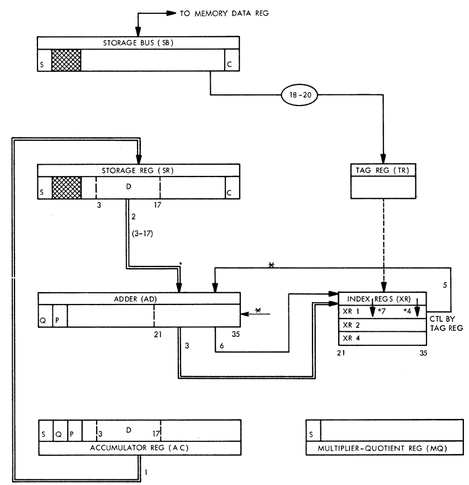
THE 2'S COMPLEMENT OF $C(AC)_{3-17}$ ARE PLACED INTO THE SPECIFIED INDEX REGISTER(S).

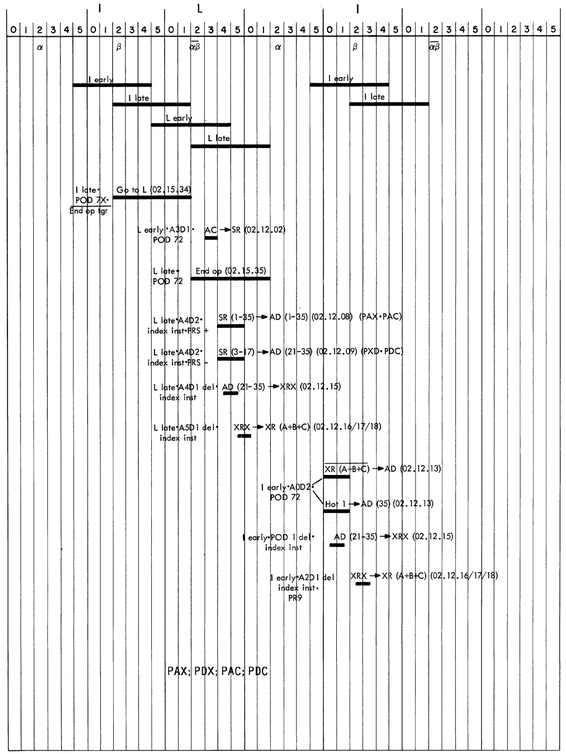
THE C(AC) ARE UNCHANGED.

A TAG OF ZERO RESULTS IN A NO-OP.

CYCLES REQUIRED: 7040: I
7044: I

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2'S COMPLEMENT.





Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	PAX	1*	00000	073400 100000
00002	CLA		00007	050000 000007
00003	PAX	1*	00000	073400 100000
00004	TRA		00000	002000 000000
00005				
00006	Pattern			000000 052525
00007	Pattern			000000 000000

*Change tag to test remaining index registers.

Place Address in Index (PAX)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER A	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF1	FF2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00			00000									
E	I	00001	+500	000	0	00001	000000052525	000000052525	00			00000									
I	L	00002	+734	000	1	00000	073400100000	000000052525	00			00000									
L	I	00002	+734	000	1	00002	000000052525	000000052525	00			52525									
I	E	00003	+500	000	0	00007	050000000007	000000052525	00			52525									
E	I	00003	+500	000	0	00003	000000000000	000000000000	00			52525									
I	L	00004	+734	000	1	00000	073400100000	000000000000	00			52525									
L	I	00004	+734	000	1	00004	000000000000	000000000000	00			00000									
I	I	00005	+026	000	0	00000	002000000000	000000000000	00			00000									

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	PDX	7	00000	473400 700000
00002	CLA		00007	050000 000007
00003	PDX	7	00000	473400 700000
00004	TRA		00000	002000 000000
00005				
00006	Pattern			025252 000000
00007	Pattern			000000 000000

Place Decrement in Index (PDX)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, AC	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF1	FF2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00			00000									
E	I	00001	+500	000	0	00001	025252000000	025252000000	00			00000									
I	L	00002	-734	000	7	00000	473400700000	025252000000	00			00000									
L	I	00002	-734	000	7	00002	425252000000	025252000000	00			25252									
I	E	00003	+500	000	0	00007	050000000007	025252000000	00			25252									
E	I	00003	+500	000	0	00003	000000000000	000000000000	00			25252									
I	L	00004	-734	000	7	00000	473400700000	000000000000	00			25252									
L	I	00004	-734	000	7	00000	400000000000	000000000000	00			00000									
I	I	00005	+020	000	0	00000	002000000000	000000000000	00			00000									

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	PAC	2*	00000	073700 200000
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			000000 025253

*Change tag to test remaining index registers.

Place Complement of Address in Index (PAC)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER B	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF1	FF2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00			00000									
E	I	00001	+500	000	0	00001	000000025253	000000025253	00			00000									
I	L	00002	+737	000	2	00000	073700200000	000000025253	00			00000									
L	I	00002	+737	000	2	00002	000000025253	000000025253	00			25253									
I	I	00003	+020	000	0	00000	002000000000	000000025253	00			52525									
I	E	00001	+500	000	0	00006	050000000006	000000025253	00			52525									
E	I	00001	+500	000	0	00001	000000025253	000000025253	00			52525									
I	L	00002	+737	000	2	00000	073700200000	000000025253	00			52525									

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	PDC	7	00000	473700 700000
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			052526 000000
00007	Pattern			000000 000000

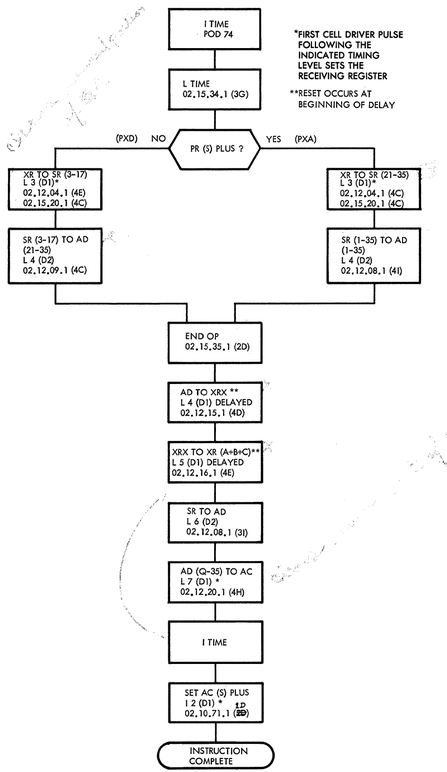
Place Complement of Decrement in Index (PDC)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, AC	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF1	FF2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00			00000									
E	I	00001	+500	000	0	00001	052526000000	052526000000	00			00000									
I	L	00002	-737	000	7	00000	473700700000	052526000000	00			00000									
L	I	00002	-737	000	7	00002	452526000000	052526000000	00			52526									
I	I	00003	+020	000	0	00000	002000000000	052526000000	00			25252									
I	E	00001	+500	000	0	00006	050000000006	052526000000	00			25252									
E	I	00001	+500	000	0	00001	052526000000	052526000000	00			25252									
I	L	00002	-737	000	7	00000	473700700000	052526000000	00			25252									

Place Index in Address (PXA +0754)
Places the contents of the specified index register into accumulator 21-35.
The rest of the accumulator is cleared. The index register is unchanged.

Place Index in Decrement (PXD -0754)
Places the contents of the specified index register into accumulator 3-17.
The rest of the accumulator is cleared. The index register is unchanged.

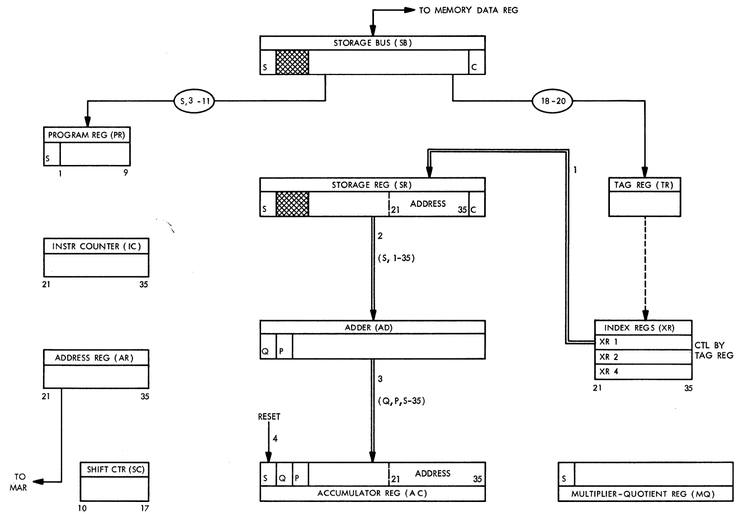


*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

**RESET OCCURS AT BEGINNING OF DELAY

FIGURE 34. PXA, PXD

* Providing 0 to effect for compatibility with previous machines



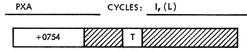
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0754 PLACE INDEX IN ADDRESS

ALPHA CODE: PXA CYCLES: I, (L)



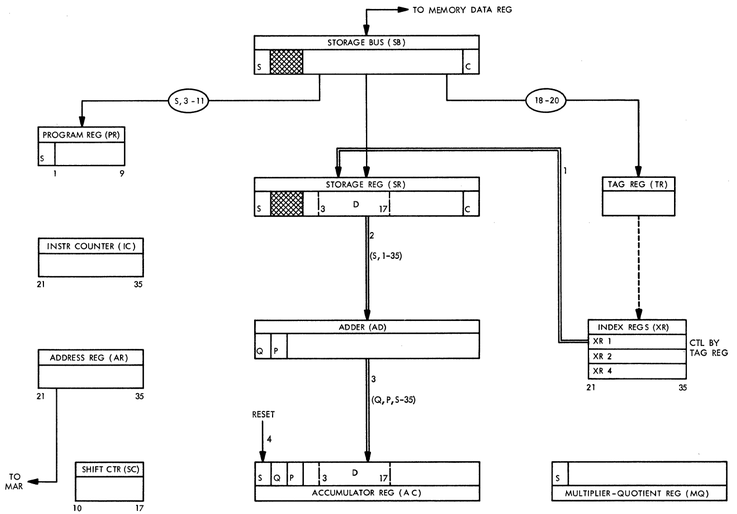
SEQUENCE NOTES:

THE ENTIRE ACCUMULATOR IS CLEARED AND THE CONTENTS OF THE SPECIFIED INDEX REGISTER(S) ARE PLACED IN THE $C(AC)_{21-35}$.

WITH A TAG OF ZERO, THE C(AC) ARE CLEARED.

THE INDEX REGISTER(S) IS UNCHANGED.

CYCLES REQUIRED: 7040: I
7044: I, L



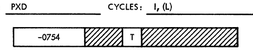
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0754 PLACE INDEX IN DECREMENT

ALPHA CODE: PXD CYCLES: I, (L)



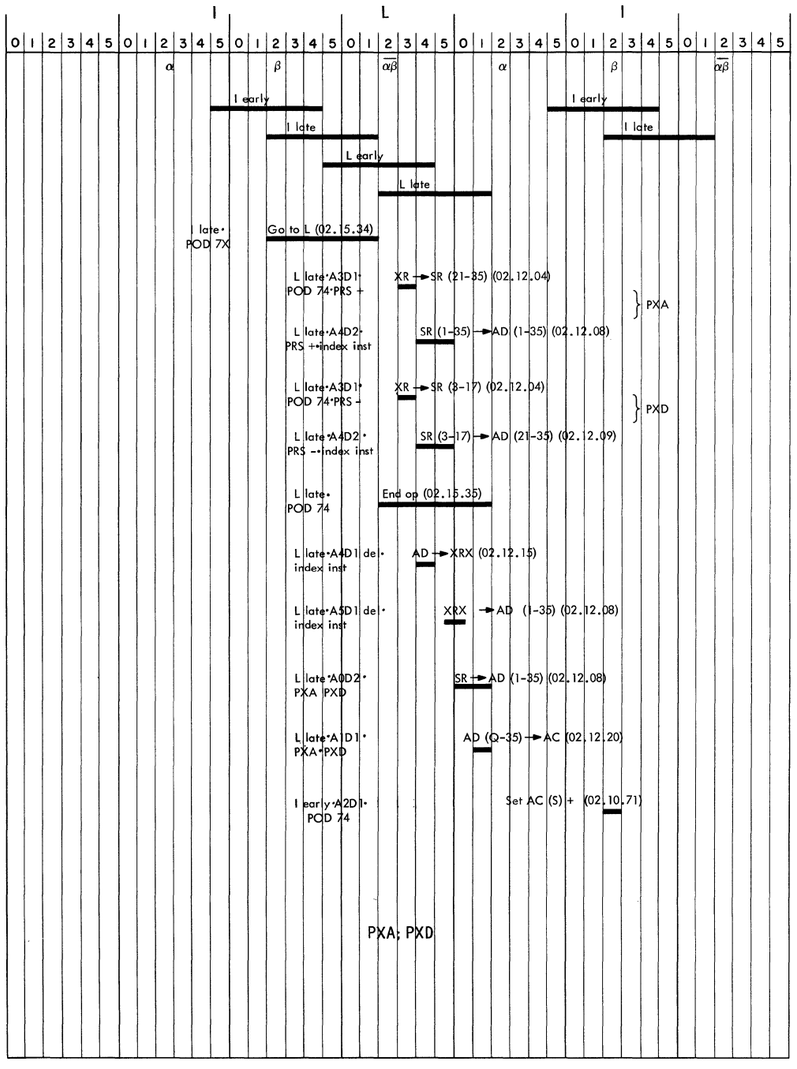
SEQUENCE NOTES:

THE ENTIRE ACCUMULATOR IS CLEARED AND THE CONTENTS OF THE SPECIFIED INDEX REGISTER(S) ARE PLACED IN THE $C(AC)_{3-17}$.

WITH A TAG OF ZERO, THE C(AC) ARE CLEARED.

THE INDEX REGISTER(S) IS UNCHANGED.

CYCLES REQUIRED: 7040: I
7044: I, L



Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	1*	77777	077400 177777
00001	CLA		00006	050000 000006
00002	PXA	1*	00000	075400 100000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			777777 700000

*Change tag to test remaining index registers.

Place Index in Address (PXA)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER A	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	I	00001	+774	377	1	00001	077400177777	000000000000	00			77777									
I	E	00002	+500	000	0	00006	050000000006	000000000000	00			77777									
E	I	00002	+500	000	0	00002	777777700000	777777700000	00			77777									
I	L	00003	+754	000	1	00000	075400100000	777777700000	00			77777									
L	I	00003	+754	000	1	00003	000000077777	000000077777	00			77777									
I	I	00004	+020	000	0	00000	002000000000	000000077777	00			77777									
I	I	00001	+774	377	1	00001	077400177777	000000077777	00			77777									
I	E	00001	+500	000	0	00006	050000000006	000000077777	00			77777									

Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	1*	77777	077400 177777
00001	CLA		00006	050000 000006
00002	PXD	1*	00000	475400 100000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			777777 777777

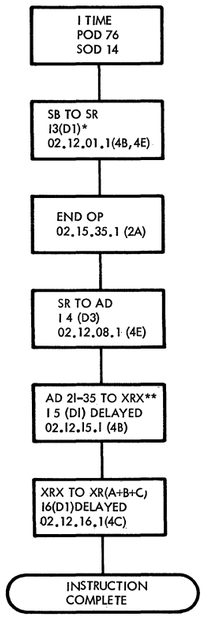
*Change tag to test remaining index registers.

Place Index in Decrement (PXD)

CONSOLE INDICATORS

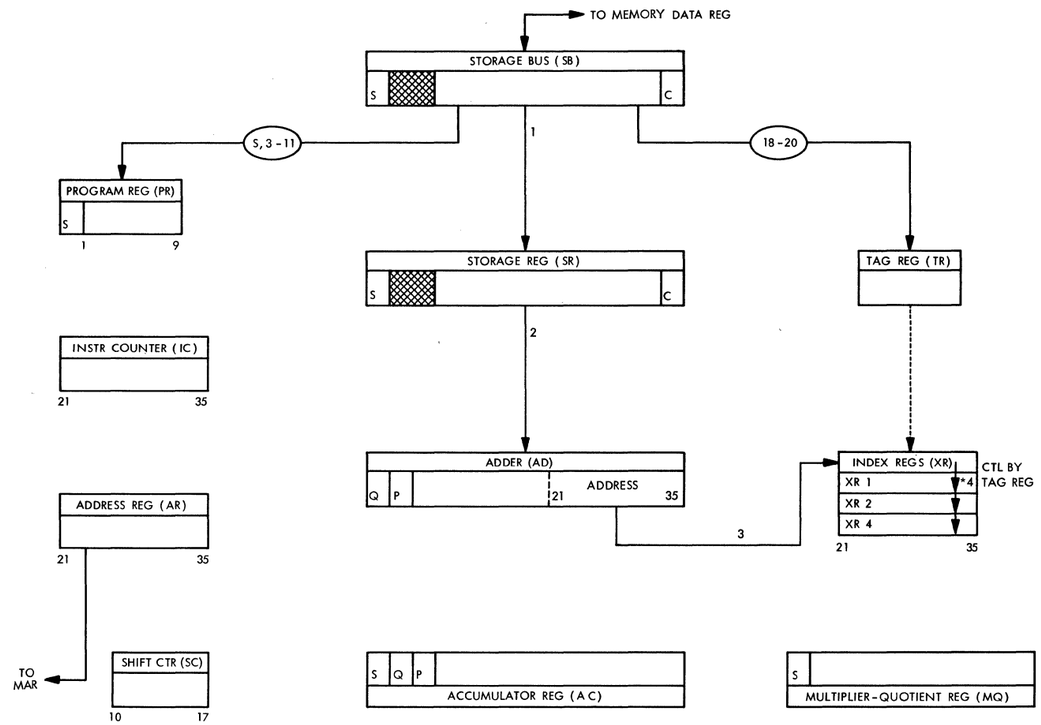
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER A	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	I	00001	+774	377	1	00001	077400177777	000000000000	00			77777									
I	E	00002	+500	000	0	00006	050000000006	000000000000	00			77777									
E	I	00002	+500	000	0	00002	777777777777	777777777777	00			77777									
I	L	00003	-754	000	1	00000	475400100000	777777777777	00			77777									
L	I	00003	-754	000	1	00003	077777000000	477777000000	00			77777									
I	I	00004	+020	000	0	00000	002000000000	077777000000	00			77777									
I	I	00001	+774	377	1	00001	077100177777	077777000000	00			77777									
I	E	00002	+500	000	0	00006	050000000006	077777000000	00			77777									

Address to Index True (AXT +0774)
Loads the specified index register from positions 21-35 of the instruction word.
The instruction is unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

**RESET OCCURS AT START OF DELAY



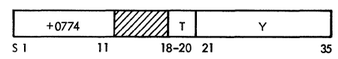
LEGEND

- I CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0774 ADDRESS TO INDEX TRUE

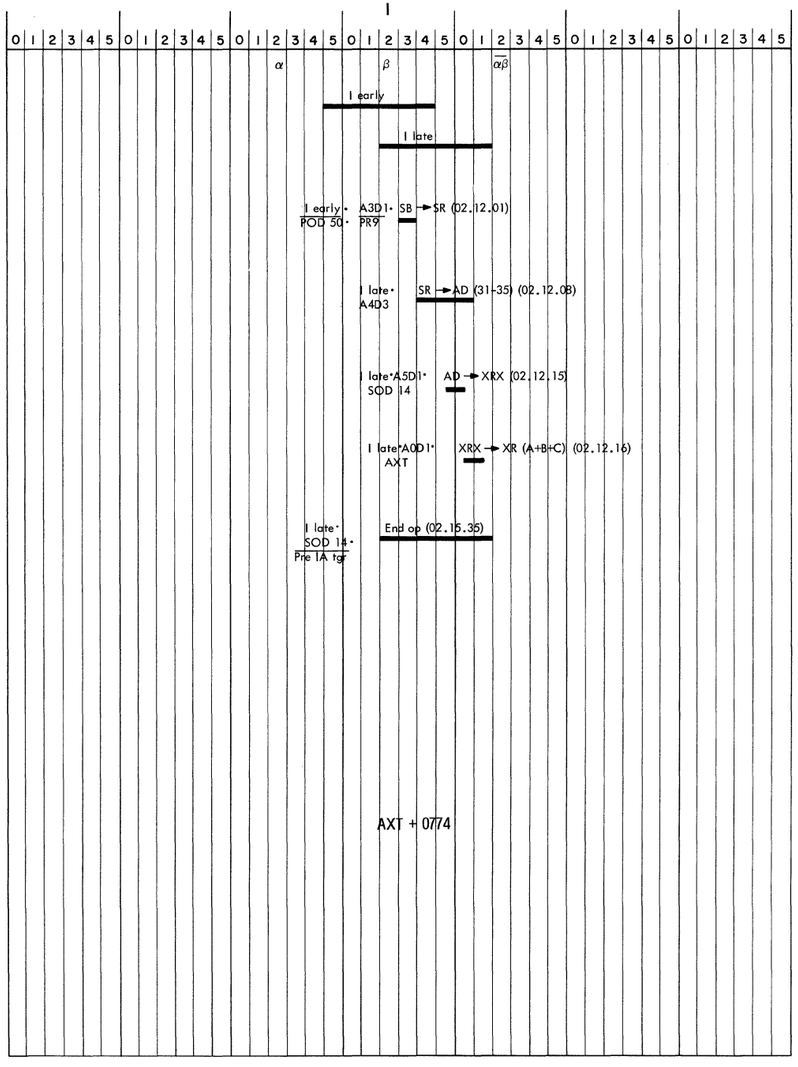
ALPHA CODE: AXT CYCLES: I



SEQUENCE NOTES:

THE SPECIFIED IX REGISTER(S) IS LOADED WITH THE VALUE CONTAINED IN 21-35 OF THE INSTRUCTION. A TAG OF ZERO RESULTS IN A NO-OP.

FIGURE 35. AXT

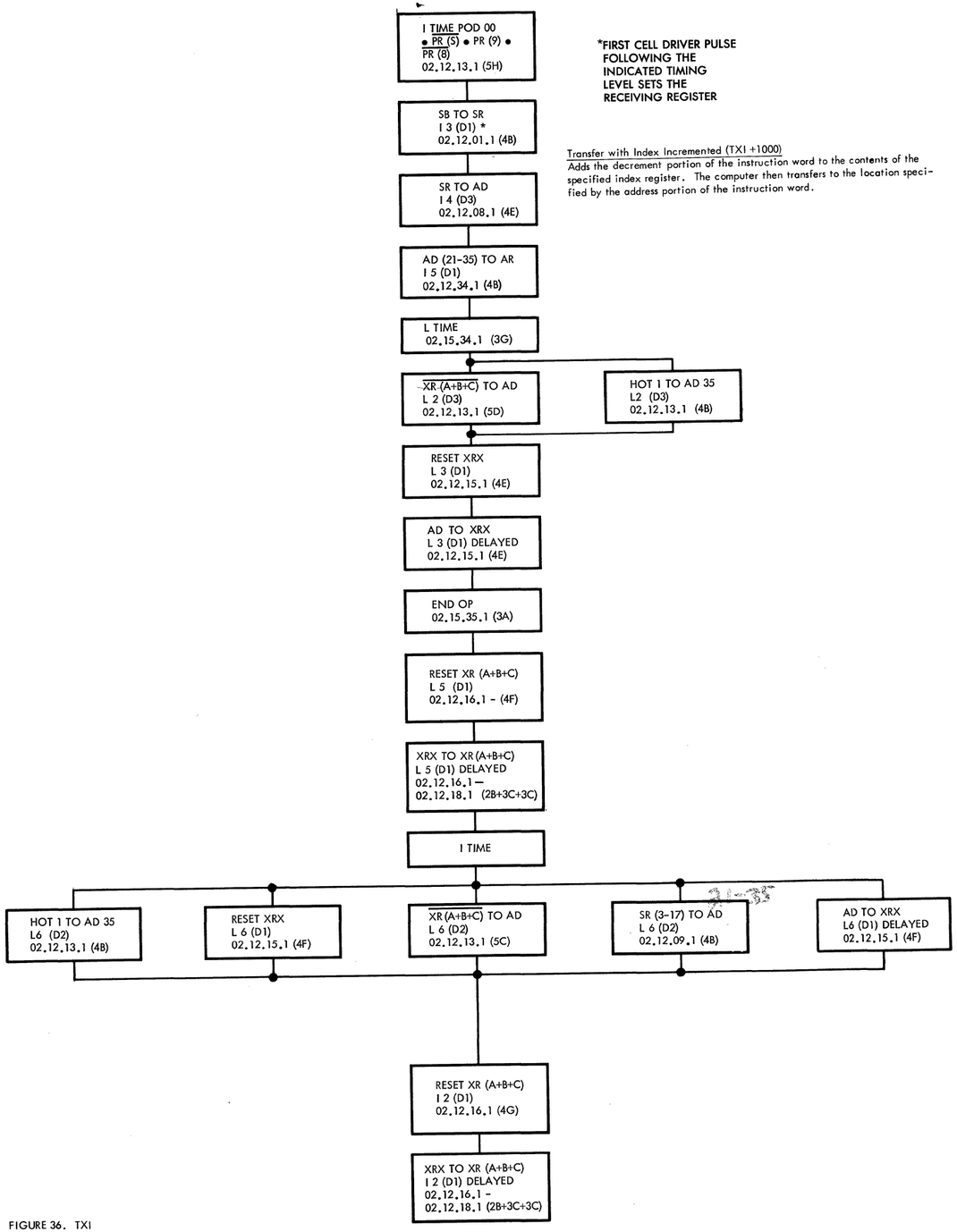


Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	77777	077400 777777
00001	AXT	7	00000	077400 700000
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006				

Address to Index True (AXT)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, &C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	I	00001	+774	377	7	00001	077400777777					77777									
I	I	00002	+774	000	7	00002	077400700000					00000									
I	I	00003	+020	000	0	00000	002000000000					00000									

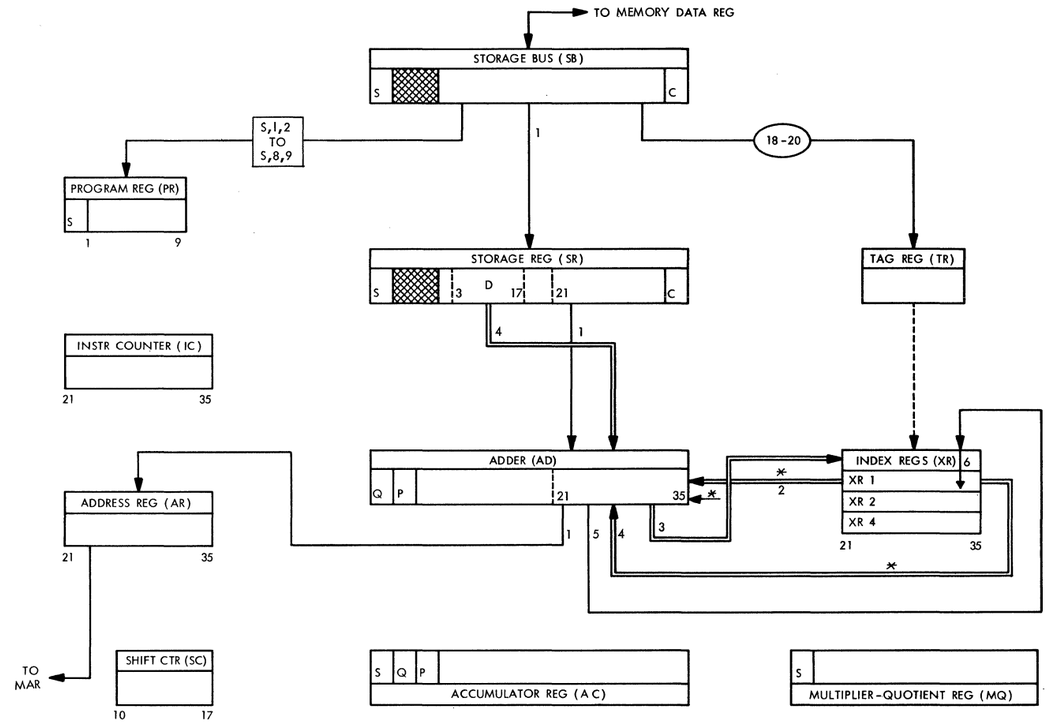


*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

Transfer with Index Incremented (TXI +1000)

Adds the decrement portion of the instruction word to the contents of the specified index register. The computer then transfers to the location specified by the address portion of the instruction word.

FIGURE 36. TXI



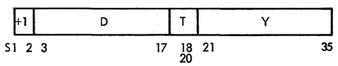
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +1 000 TRANSFER WITH INDEX INCREMENTED

ALPHA CODE: TXI CYCLES: I, (L)



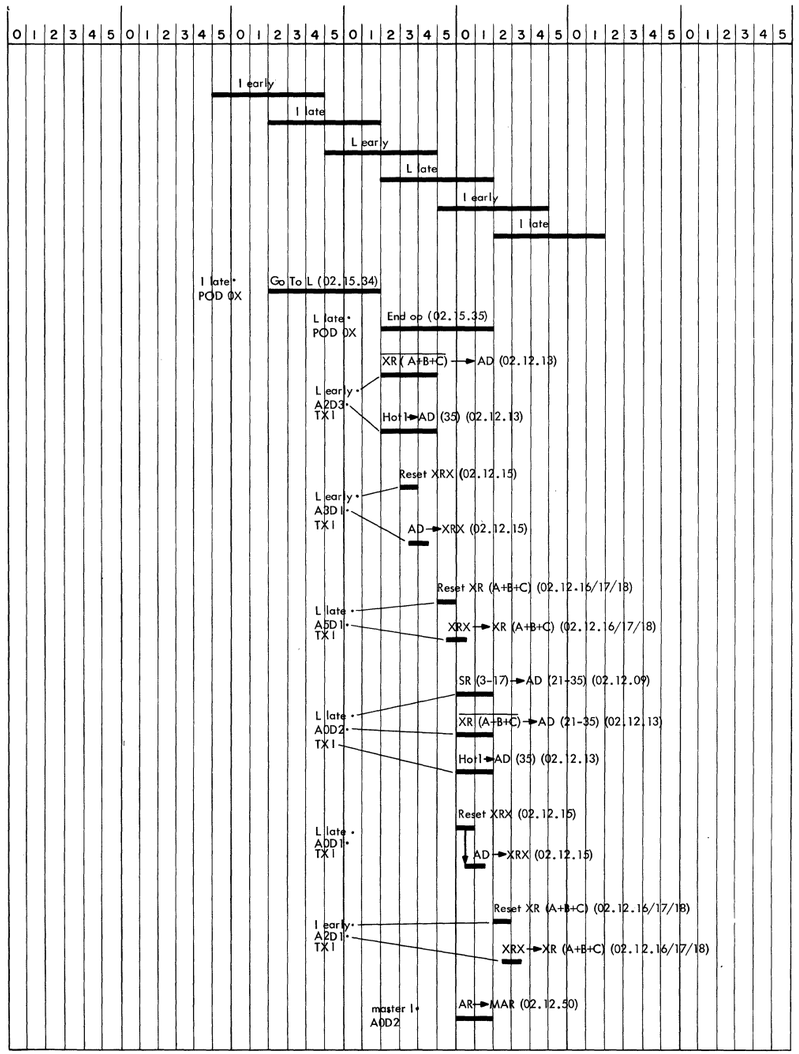
SEQUENCE NOTES:

THE DECREMENT PORTION OF THE INSTRUCTION WORD IS ADDED TO THE CONTENTS OF THE SPECIFIED XR(S).

THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y.

CYCLES REQUIRED: 7040: I
7044: I L

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2'S COMPLEMENT.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	TXI (D=7)	7	00002	100007 700002
00001	HPR			042000 000000
00002	TXI (D-70)	7		100070 700004
00003	HPR			042000 000000
00004	TXI (D=700)	7	00005	100700 700005
00005	AXT	7	00000	077400 700000
00006.	TRA		00000	002000 000000

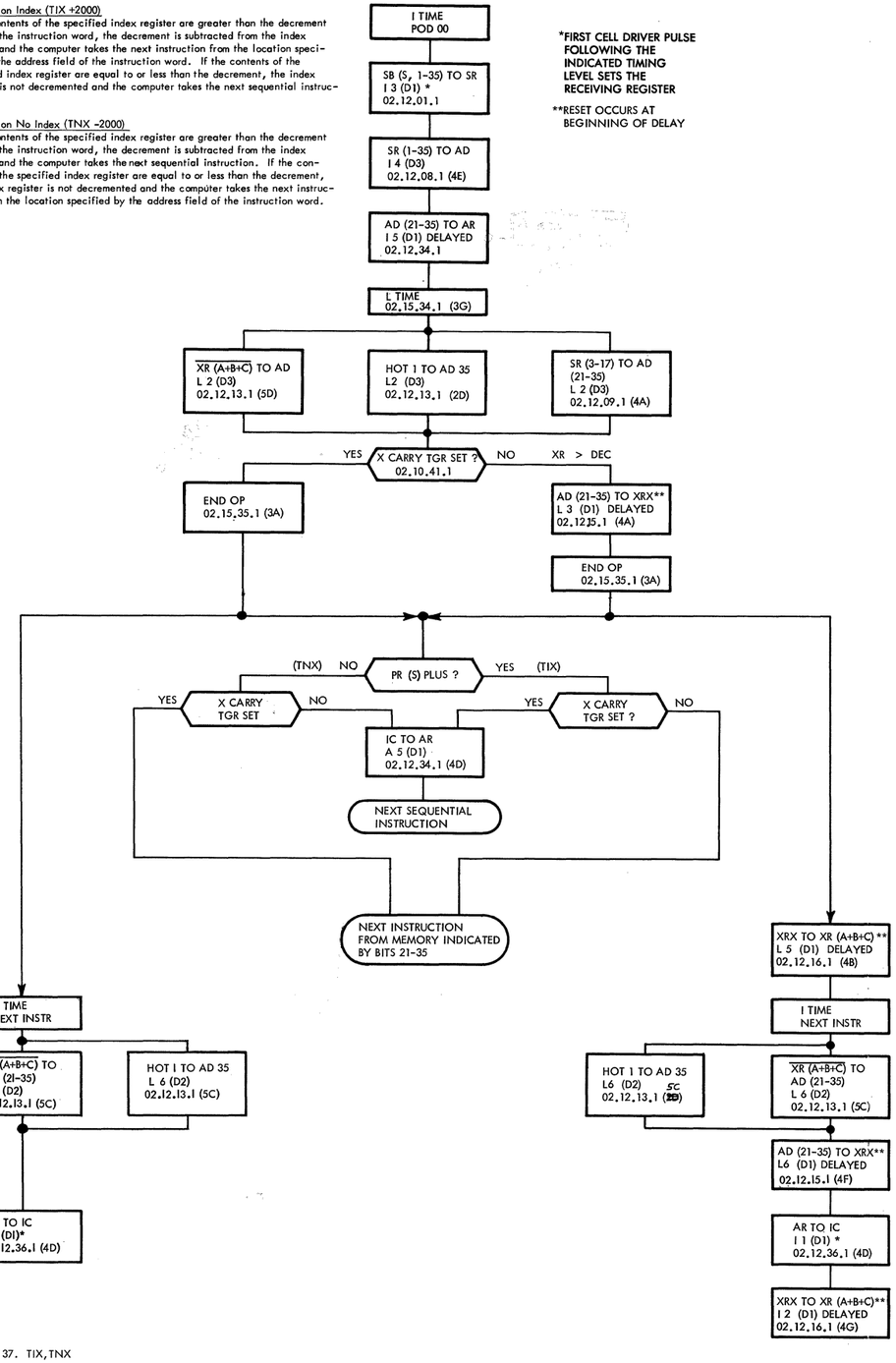
Transfer with Index Decremented (TXI)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, &C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	L	00001	+001	000	1	00002	100007700002					00000									
L	I	00001	+001	000	1	00002	100007700002					00000									
I	L	00003	+001	000	1	00004	100070700004					00007									
L	I	00003	+001	000	1	00004	100070700004					77771									
I	L	00005	+001	000	1	00005	100700700005					00077									
L	I	00005	+001	000	1	00005	100700700005					77701									
I	I	00006	+774	000	1	00006	077400700000					00000									
I	I	00007	+020	000	0	00000	002000000000					00000									

Transfer on Index (TIX +2000)
If the contents of the specified index register are greater than the decrement field of the instruction word, the decrement is subtracted from the index register and the computer takes the next instruction from the location specified by the address field of the instruction word. If the contents of the specified index register are equal to or less than the decrement, the index register is not decremented and the computer takes the next sequential instruction.

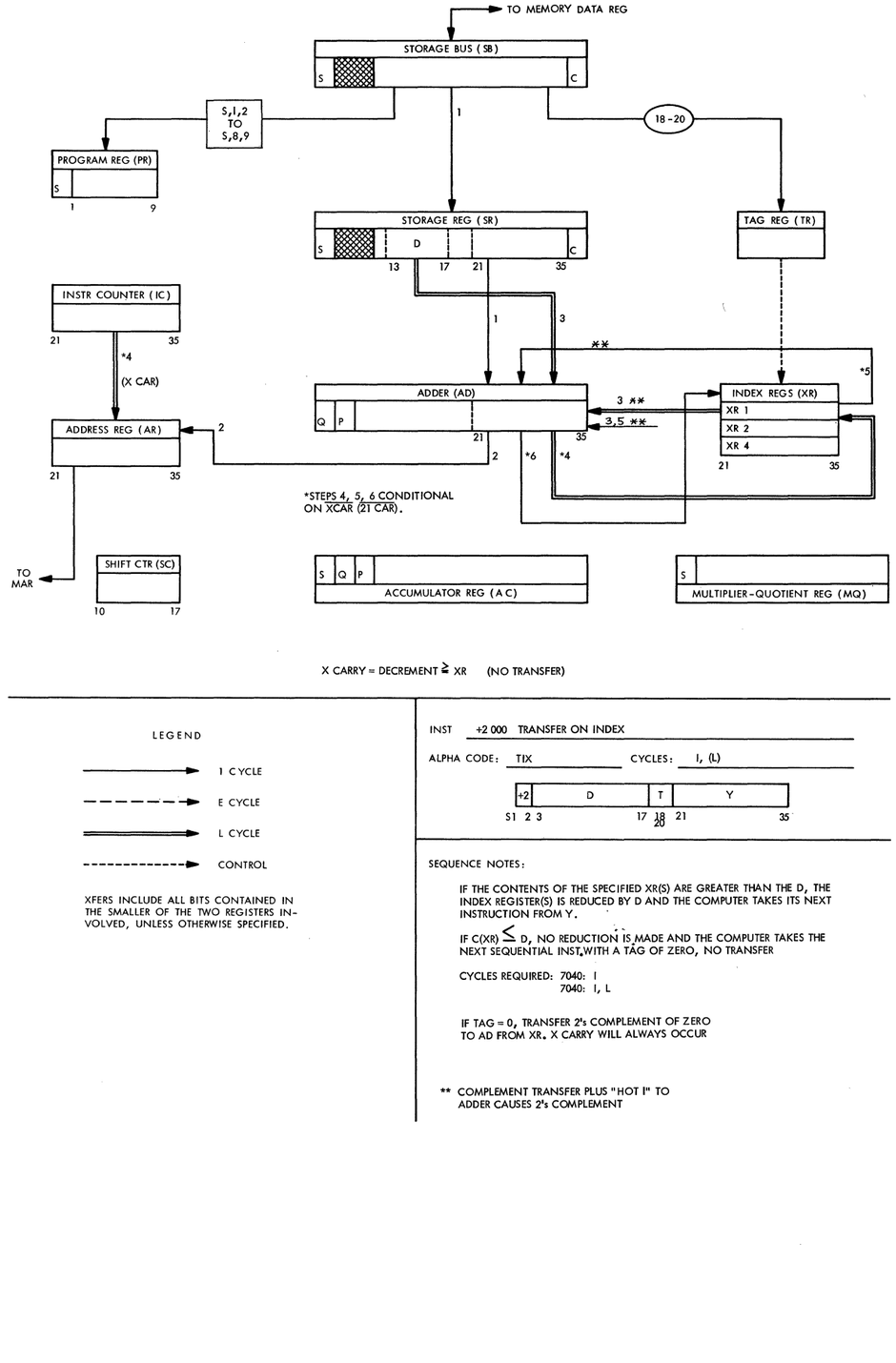
Transfer on No Index (TNX -2000)
If the contents of the specified index register are greater than the decrement field of the instruction word, the decrement is subtracted from the index register and the computer takes the next sequential instruction. If the contents of the specified index register are equal to or less than the decrement, the index register is not decremented and the computer takes the next instruction from the location specified by the address field of the instruction word.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

**RESET OCCURS AT BEGINNING OF DELAY

FIGURE 37. TIX, TNX



X CARRY = DECREMENT ≥ XR (NO TRANSFER)

LEGEND

- I CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +2 000 TRANSFER ON INDEX

ALPHA CODE: TIX CYCLES: I, (L)

SEQUENCE NOTES:

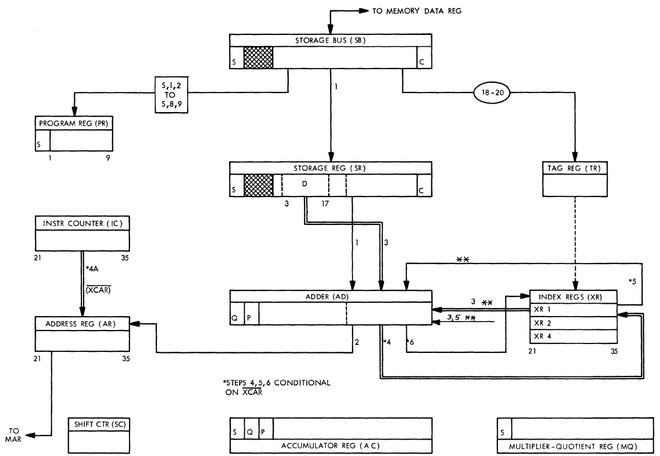
IF THE CONTENTS OF THE SPECIFIED XR(S) ARE GREATER THAN THE D, THE INDEX REGISTER(S) IS REDUCED BY D AND THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM Y.

IF C(XR) ≤ D, NO REDUCTION IS MADE AND THE COMPUTER TAKES THE NEXT SEQUENTIAL INST. WITH A TAG OF ZERO, NO TRANSFER

CYCLES REQUIRED: 7040: I
7040: I, L

IF TAG = 0, TRANSFER 2's COMPLEMENT OF ZERO TO AD FROM XR. X CARRY WILL ALWAYS OCCUR

** COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2's COMPLEMENT



$\overline{X\ CARRY}$ = XR > DECREMENT (NO TRANSFER)

LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -2 000 TRANSFER ON NO INDEX

ALPHA CODE: TNX CYCLES: I, (L)

-2	D	T	Y

S1 2 3 17 18 20 21 35

SEQUENCE NOTES:

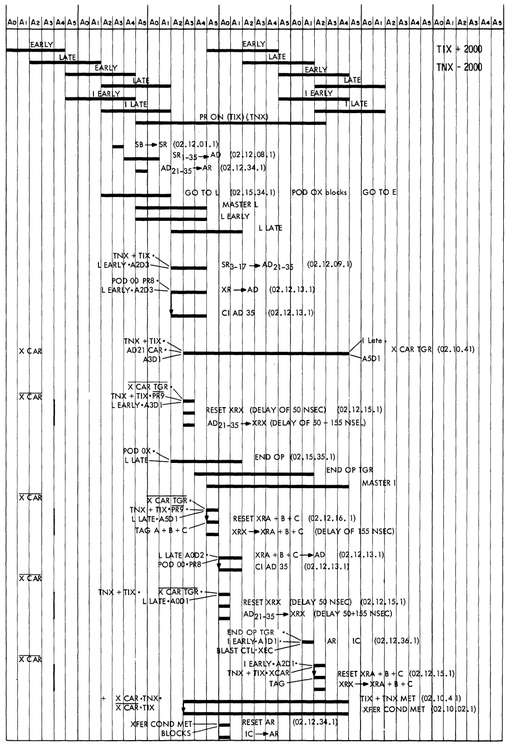
IF THE CONTENTS OF THE SPECIFIED XR(S) ARE GREATER THAN THE D, THE XR(S) IS REDUCED BY D, AND THE COMPUTER PERFORMS THE NEXT SEQ INST.

IF C(XR) $\leq$ D, NO REDUCTION IS MADE AND THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM Y.

A TAG OF ZERO WILL RESULT IN A TRANSFER.

CYCLES REQUIRED: 7040: I
7044: I, L

** COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2's COMPLEMENT



Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	00003	077400 000003
00001	TIX (D=1)	7	00001	200001 700001
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006				

Transfer on Index (TIX)

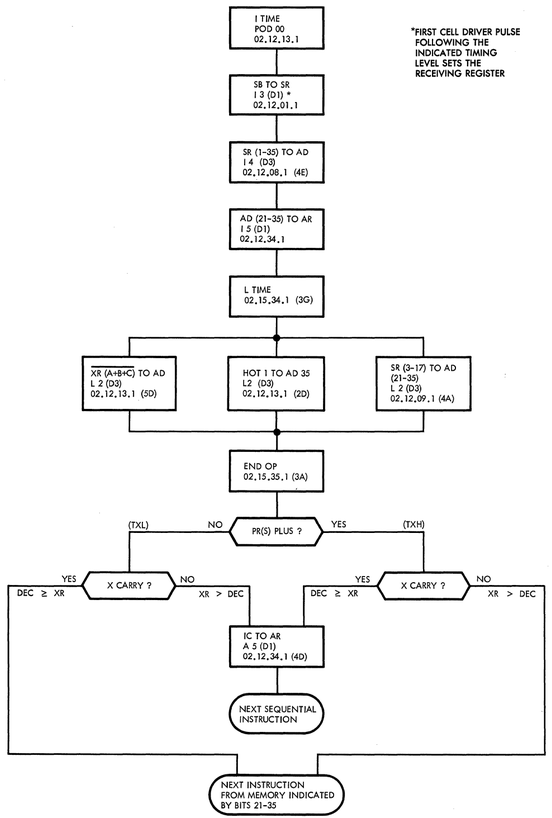
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	EXTENSION (S, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, AND C	POSITION REGISTER	ACCUM OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	Y CARRY	Z OVERFLOW	TP 1	TP 2
I	I	00001	+774	003	7	00001	077400700003					00003				0					
I	L	00002	+002	000	7	00001	200001700001					00003				0					
L	I	00002	+002	000	7	00001	200001700001					77776				0					
I	L	00002	+002	000	7	00001	200001700001					00002				0					
L	I	00002	+002	000	7	00001	200001700001					77777				0					
I	L	00002	+002	000	7	00001	200001700001					00001				0					
L	I	00002	+002	000	7	00002	200001700001					00001				1					
I	I	00003	+020	000	0	00000	002000000000					00001				0					

Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	00003	077400 700003
00001	TNX (D=1)	7	00000	600001 700000
00002	TRA	1	00001	002000 000001
00003				
00004				
00005				
00006				

Transfer on No Index (TNX)

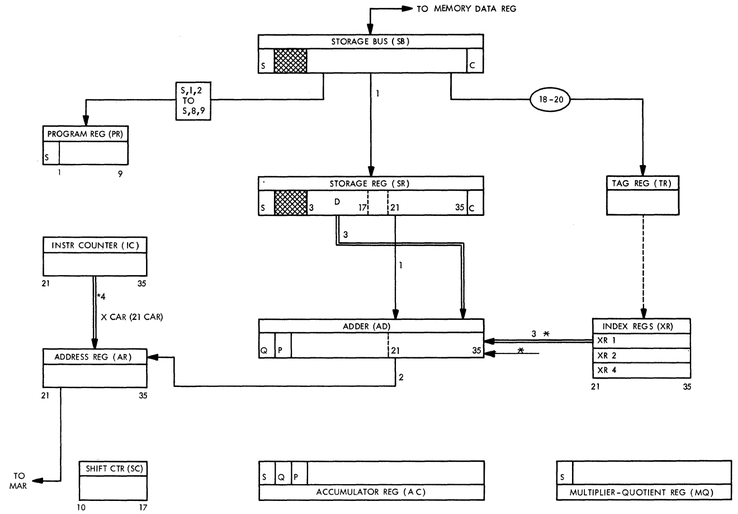
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	EXTENSION (S, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, AND C	POSITION REGISTER	ACCUM OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	Y CARRY	Z OVERFLOW	TP 1	TP 2
I	I	00001	+774	003	7	00001	077400700003					00003				0					
I	L	00002	-002	000	7	00000	600001700000					00003				0					
L	I	00002	-002	000	7	00002	600001700000					77776				0					
I	I	00003	+020	000	0	00001	002000000001					00002				0					
I	L	00002	-002	000	7	00000	600001700000					00002				0					
L	I	00002	-002	000	7	00002	600001700000					77777				0					
I	I	00003	+020	000	0	00001	002000000001					00001				0					
I	L	00002	-002	000	7	00000	600001700000					00001				0					
L	I	00002	-002	000	7	00000	600001700000					00001				1					

Transfer on Index Low or Equal (TXL -3000)
If the contents of the specified index register are less than or equal to the decrement field of the instruction word, the computer takes its next instruction from the location specified by the address field of the instruction. If the index register is greater than the decrement, the computer takes the next sequential instruction.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 38. TXH, TXL



X CARRY = DECREMENT ≧ XR (NO TRANSFER)

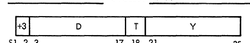
LEGEND

- I CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +3 000 TRANSFER ON INDEX HIGH

ALPHA CODE: TXH CYCLES: I, (L)



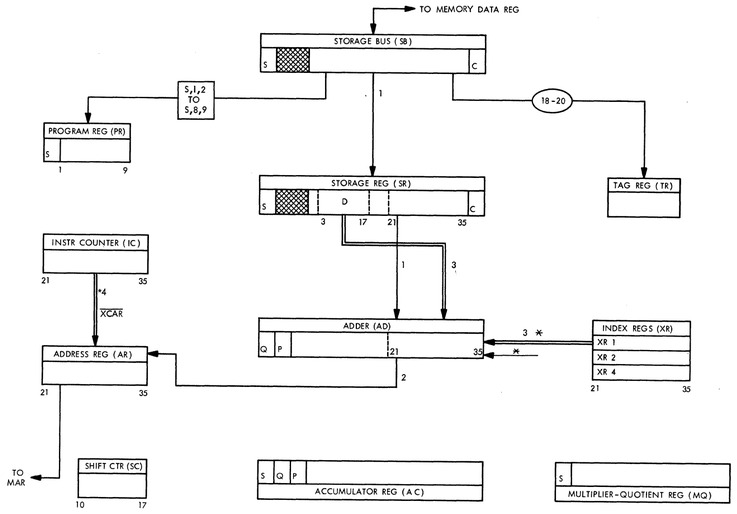
SEQUENCE NOTES:

IF THE CONTENTS OF THE SPECIFIED XR(S) ARE GREATER THAN D, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y.

IF C(XR) IS ≦ D, THE COMPUTER TAKES ITS NEXT SEQUENTIAL INSTRUCTION. WITH A TAG OF ZERO, NO TRANSFER OCCURS.

CYCLES REQUIRED: 7040: I
7044: I, L

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2's COMPLEMENT



$\overline{\text{X CARRY}}$ = XR > DECREMENT (NO TRANSFER)

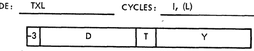
LEGEND

- I CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -3 000 TRANSFER ON INDEX LOW OR EQUAL

ALPHA CODE: TXL CYCLES: I, (L)



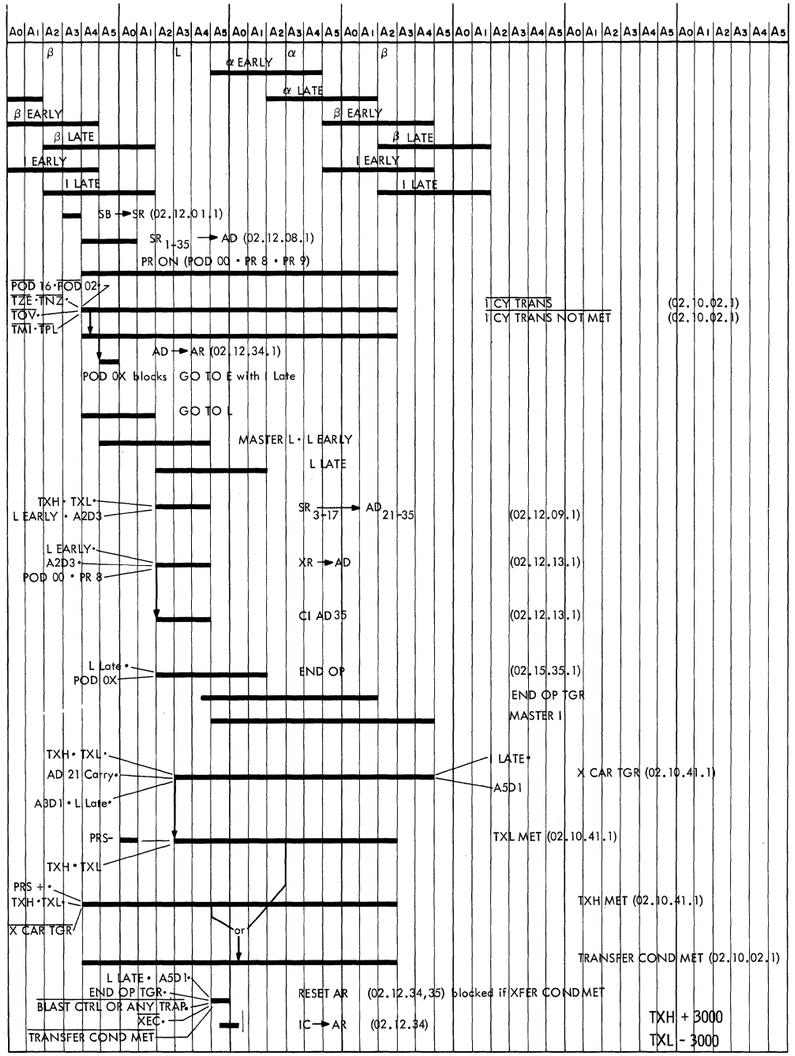
SEQUENCE NOTES:

IF THE CONTENTS OF THE SPECIFIED XR(S) ARE LESS THAN OR EQUAL TO D, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y.

IF C(XR) > D, THE COMPUTER TAKES ITS NEXT SEQUENTIAL INSTRUCTION. WITH A TAG OF ZERO, A TRANSFER OCCURS.

CYCLES REQUIRED: 7040: I
7044: I, L

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2's COMPLEMENT



Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	00077	077400 700077
00001	TXH (D=76)	7	00004	300076 700004
00002	HPR			042000 000000
00003	HPR			042000 000000
00004	AXT	7	00000	077400 700000
00005	TXH (D=0)	7	00004	300000 700002
00006	TRA		00000	002000 000000

Transfer on Index High (TXH)

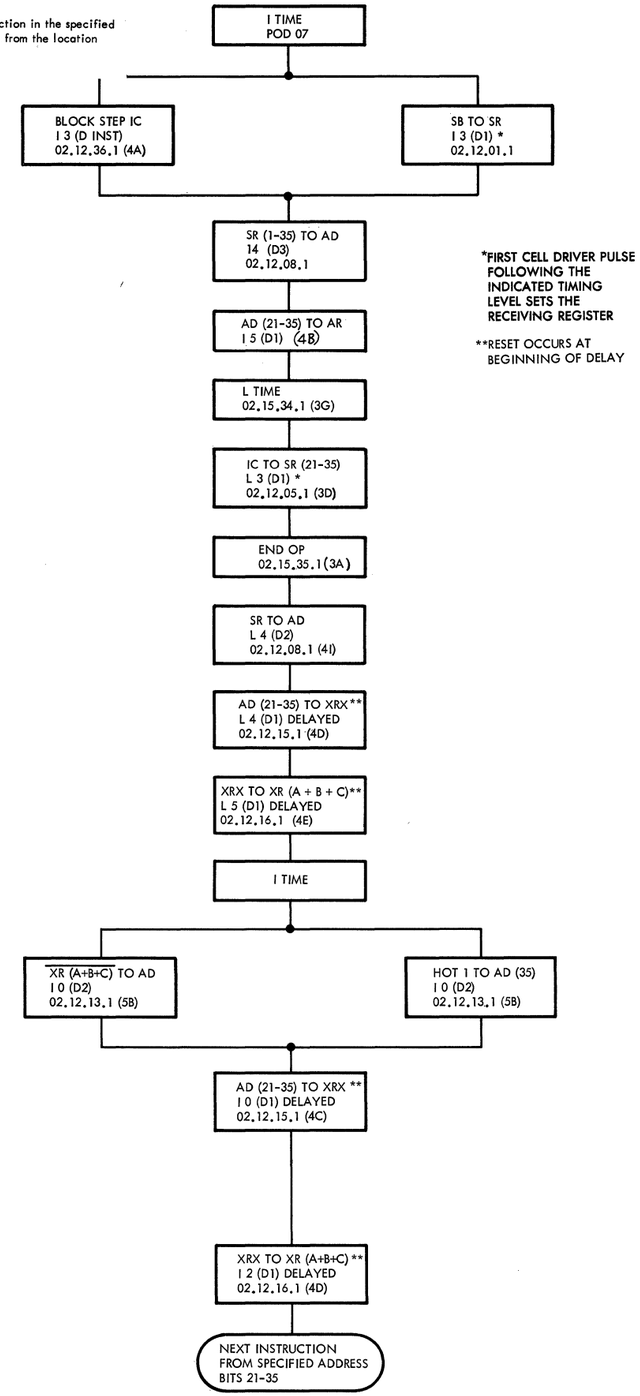
CONSOLE INDICATORS																								
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, &C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	I	00001	+774	077	7	00001	077400700077					00077				0					
I	L	00002	+003	000	7	00004	300076700004					00077				0					
L	I	00002	+003	000	7	00004	300076700004					00077				0					
I	I	00005	+774	000	7	00005	077400700000					00000				0					
I	L	00006	+003	000	7	00002	300000700002					00000				0					
L	I	00006	+003	000	7	00006	300000700002					00000				1					
I	I	00007	+020	000	0	00000	002000000000					00000				0					

Location Switches	Inst	Tag	Address	Octal Equiv
00000	AXT	7	00077	077400 700077
00001	TXL (D=76)	7	00005	700076 700005
00002	TXL (D=76)	7	00006	700076 700006
00003	AXT	7	00000	077400 700000
00004	TXL (D=0)	7	00006	700000 700006
00005	HPR		00000	042000 000000
00006	TRA		00000	002000 000000

Transfer on Index Low or Equal (TXL)

CONSOLE INDICATORS																								
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS A, B, &C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	I	00001	+774	077	7	00001	077400700077					00077				0					
I	L	00002	-003	000	7	00005	700076700005					00077				0					
L	I	00002	-003	000	7	00002	700076700005					00077				0					
I	L	00003	-003	000	7	00006	700076700006					00077				0					
L	I	00003	-003	000	7	00003	700076700006					00077				0					
I	I	00004	+774	000	7	00004	077400700000					00000				0					
I	L	00005	-003	000	7	00006	700000700006					00000				0					
L	I	00005	-003	000	7	00006	700000700006					00000				1					
I	I	00007	+020	000	0	00000	002000000000					00000				0					

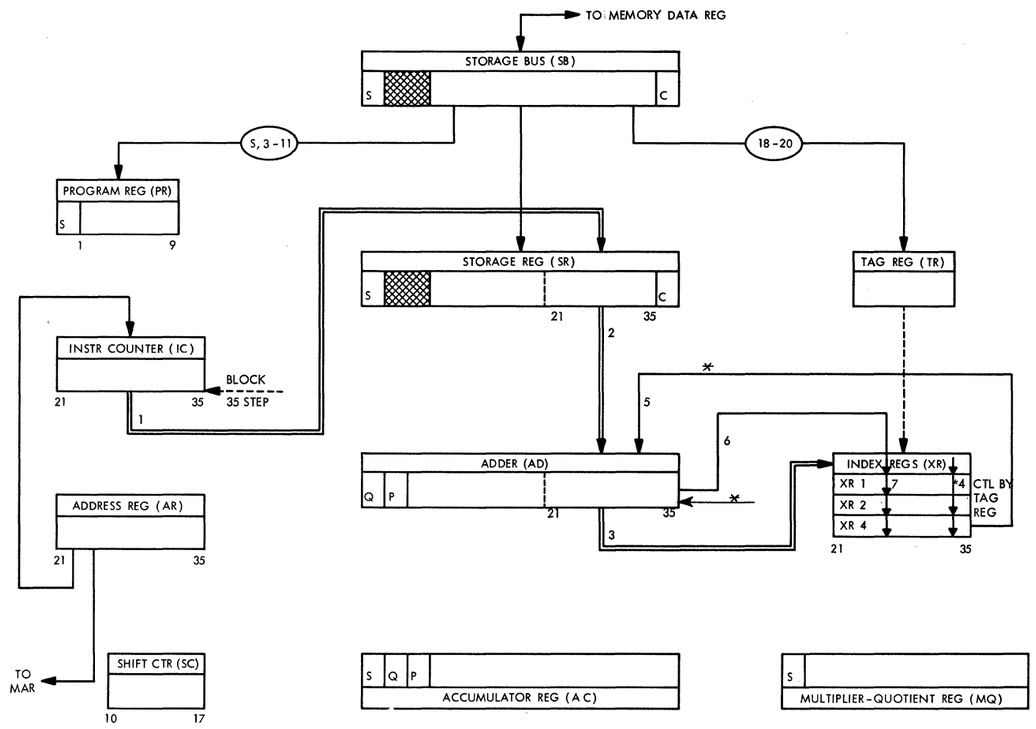
Transfer and Set Index (TSX +0074)
Places the 2's complement of the location of the instruction in the specified index register. The computer takes the next instruction from the location specified by the address field of the instruction word.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

**RESET OCCURS AT BEGINNING OF DELAY

FIGURE 39. TSX



LEGEND

1 CYCLE

E CYCLE

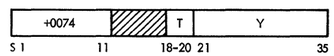
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0074 TRANSFER AND SET INDEX

ALPHA CODE: TSX CYCLES: I, (L)



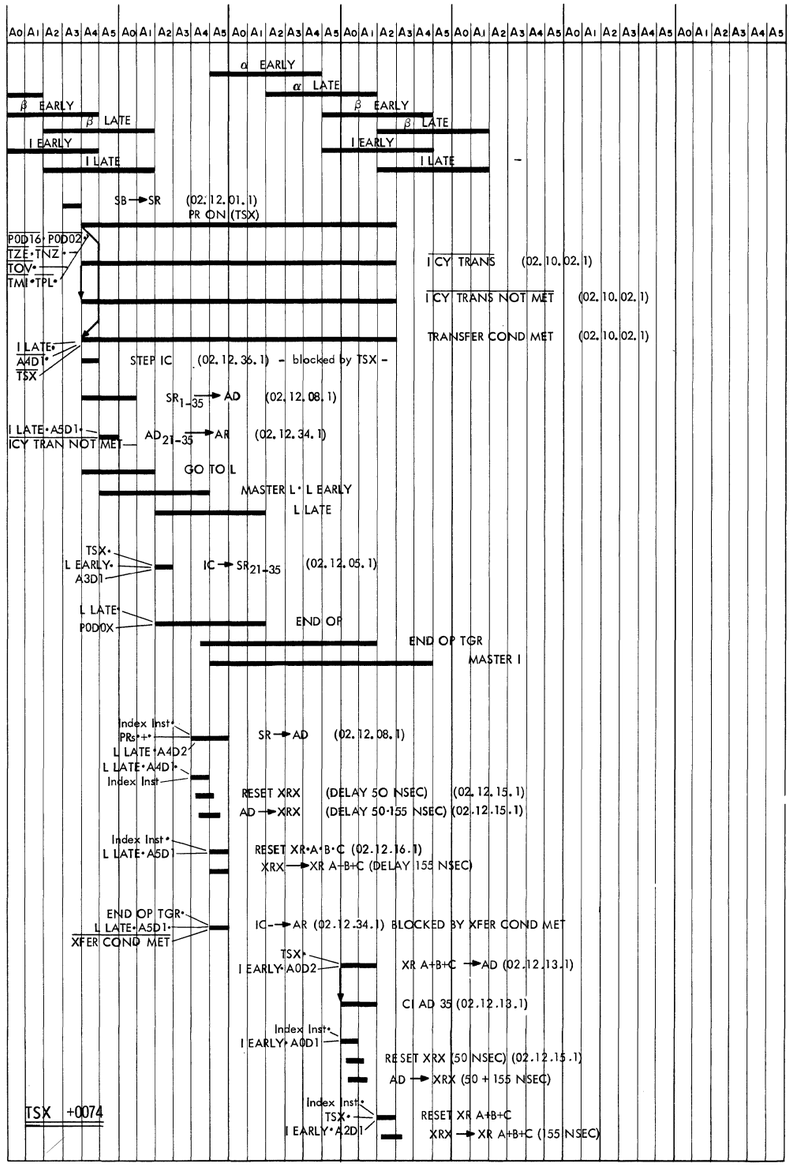
SEQUENCE NOTES:

THE 2'S COMPLEMENT OF THE LOCATION OF THE TSX IS STORED IN THE SPECIFIED INDEX REGISTER.

THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y.

CYCLES REQUIRED: 7040: I
7044: I, L

* COMPLEMENT TRANSFER PLUS "HOT I" TO ADDER CAUSES 2's COMPLEMENT



Location Switches	Inst	Tag	Address	Octal Equiv
00000	TSX	7	00003	007400 700002
00001	HPR			042000 000000
00002	HPR			042000 000000
00003	TSX	7	00005	007400 700005
00004	HPR			042000 000000
00005	TRA		00000	002000 000000

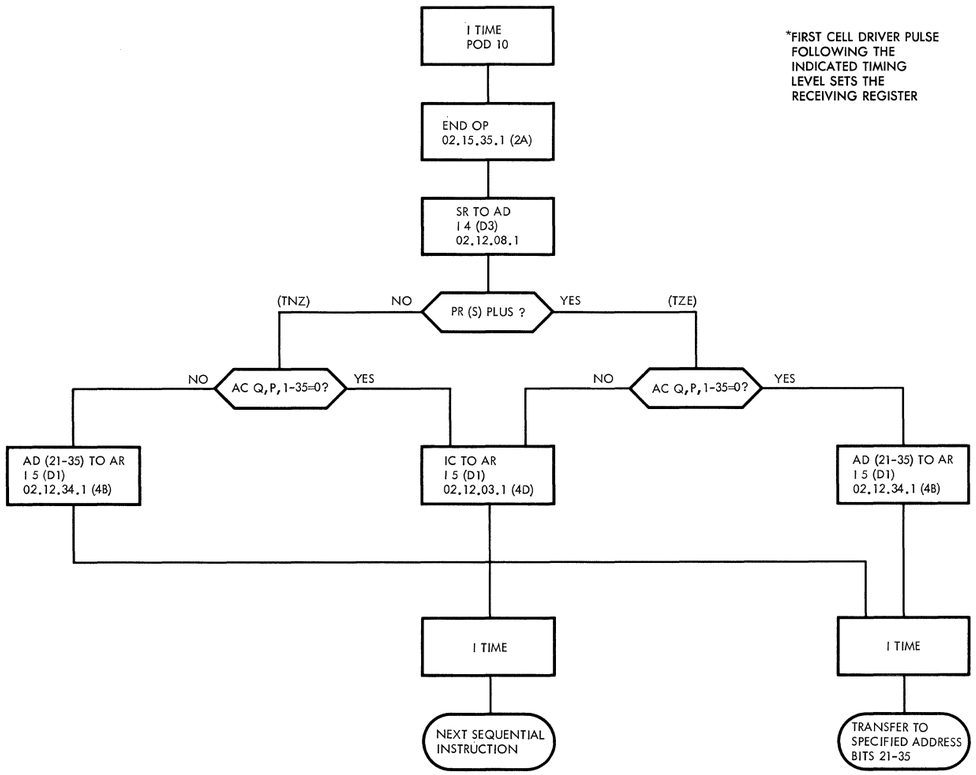
Transfer and Set Index (TSX)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTERS, A, B, &C	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	L	00000	+074	000	7	00003	007400700003														
L	I	00000	+074	000	7	00003	000000000000														
I	L	00003	+074	000	7	00005	007400700005														
L	I	00002	+074	000	7	00005	000000000003					00003									
I	I	00006	+020	000	0	00000	002000000000					77775									
I	L	00000	+074	000	7	00003	007400700003					77775									

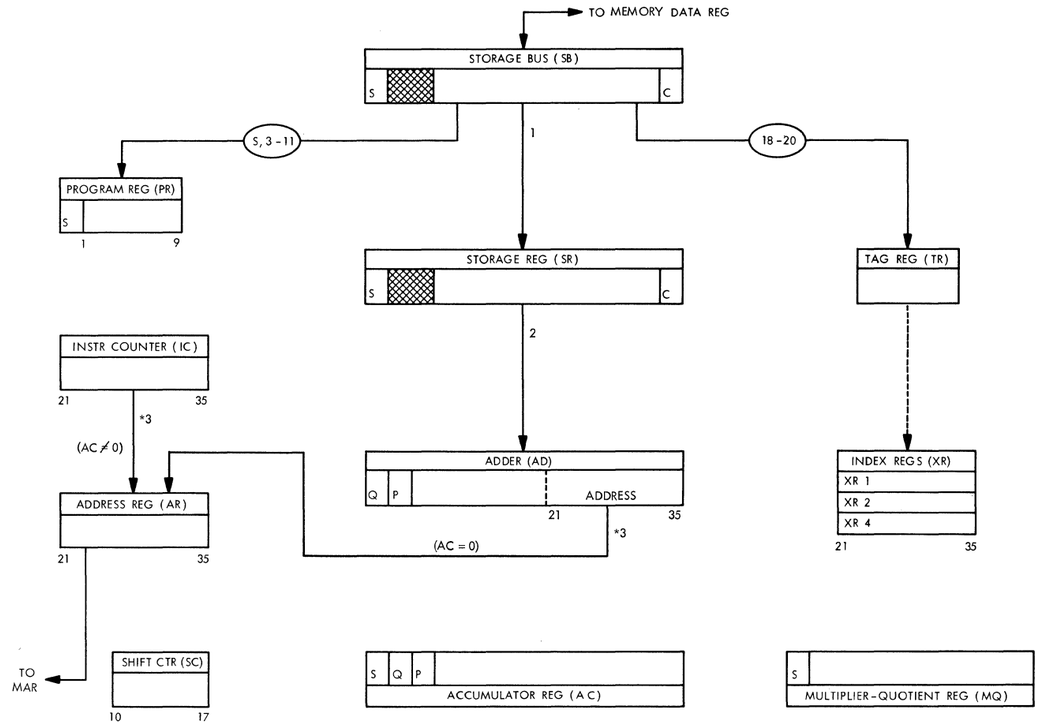
Transfer on Zero (TZE +0100)
If the accumulator is zero (Q,P,1-35), the computer takes its next instruction from the location specified by the address field of the instruction word. If the accumulator is not zero, the computer takes the next sequential instruction.

Transfer on No Zero (TNZ -0100)
If the accumulator is not zero (Q,P,1-35), the computer takes its next instruction from the location specified by the address field of the instruction word. If the accumulator is zero, the computer takes the next sequential instructions.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 40. TZE, TNZ



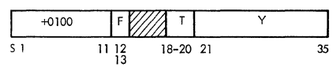
LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0100 TRANSFER ON ZERO

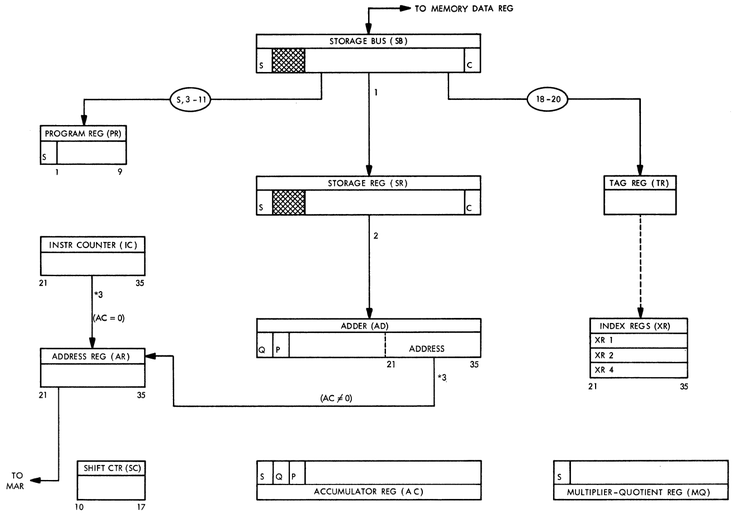
ALPHA CODE: TZE CYCLES: 1



SEQUENCE NOTES:

IF $C(AC)_{Q, P, 1-35}$ ARE ZERO, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y AND CONTINUES.

*3. AD_{21-35} ⟶ AR IF AC = 0.
IC ⟶ AR IF AC ≠ 0.



LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0100 TRANSFER ON NO ZERO

ALPHA CODE: TNZ CYCLES: 1

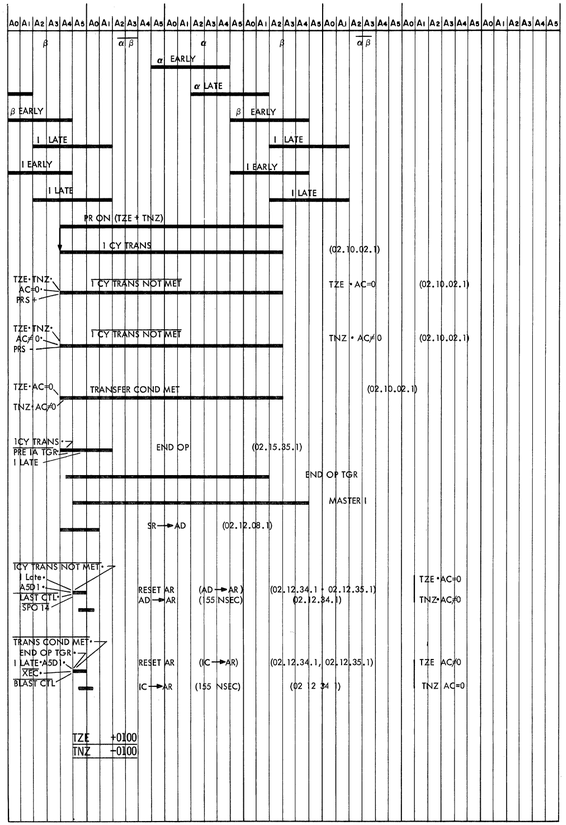
-0100	F	T	Y
S 1	11 12 13	18-20 21	35

SEQUENCE NOTES:

IF $C(AC)_{Q,\ P,\ 1-35}$ ARE NOT ZERO, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM LOCATION Y AND CONTINUES.

*3 AD_{21-35} ⟶ AR IF AC ≠ 0.

IC ⟶ AR IF AC = 0.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TZE		00003	010000 000003
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			000000 000000

Transfer on Zero (TZE)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	000000000000	000000000000	00												
I	I	00002	+100	000	0	00003	010000000003	000000000000	00												
I	I	00004	+020	000	0	00000	002000000000	000000000000	00												

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TNZ		00003	410000 000003
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			377777 777777

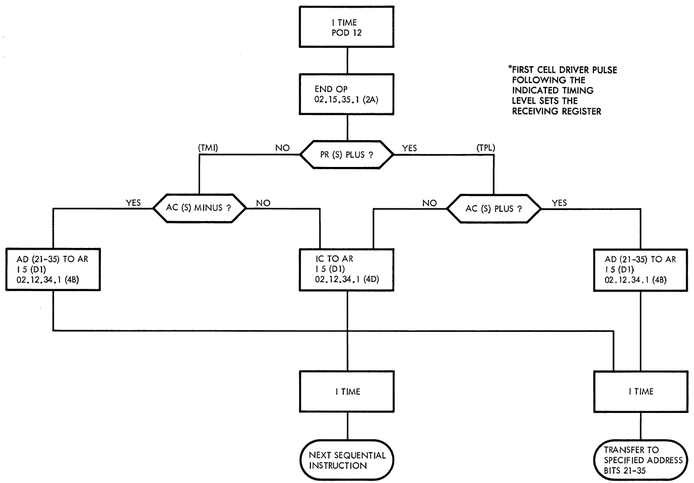
Transfer on No Zero (TNZ)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	377777777777	377777777777	00												
I	I	00002	-100	000	0	00003	410000000003	377777777777	00												
I	I	00004	+020	000	0	00000	002000000000	377777777777	00												
I	E	00001	+500	000	0	00006	050000000006	377777777777	00												

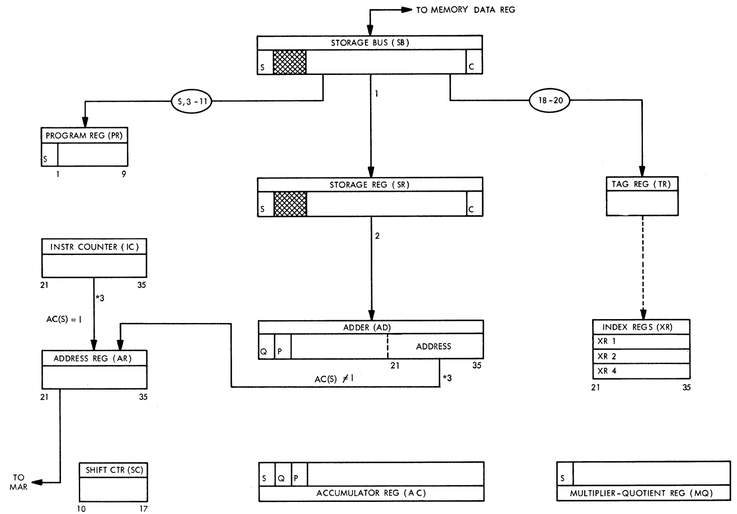
Transfer on Plus (TPL +0120)
If the sign of the accumulator is plus, the computer takes its next instruction from the location specified by the address field of the instruction word. If the sign is minus, the computer takes the next sequential instruction.

Transfer on Minus (TM1 -0120)
If the sign of the accumulator is minus, the computer takes its next instruction from the location specified by the address field of the instruction word. If the sign is plus, the computer takes the next sequential instruction.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 41. TPL,TM1



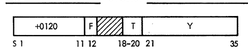
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0120 TRANSFER ON PLUS

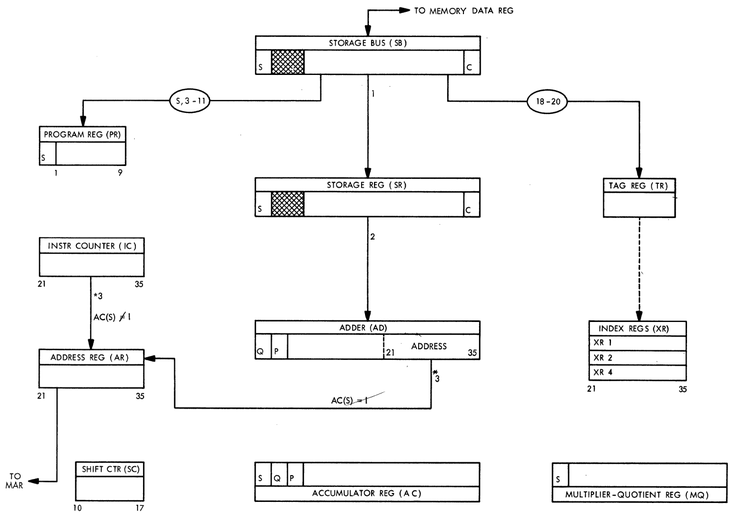
ALPHA CODE: TPL CYCLES: 1



SEQUENCE NOTES:

IF AC(S) IS +, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM Y AND CONTINUES.

*3 AD_{21-35} ⟶ AR IF AC(S) = +.
IC ⟶ AR IF AC(S) ≠ +.



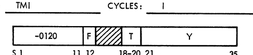
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0120 TRANSFER ON MINUS

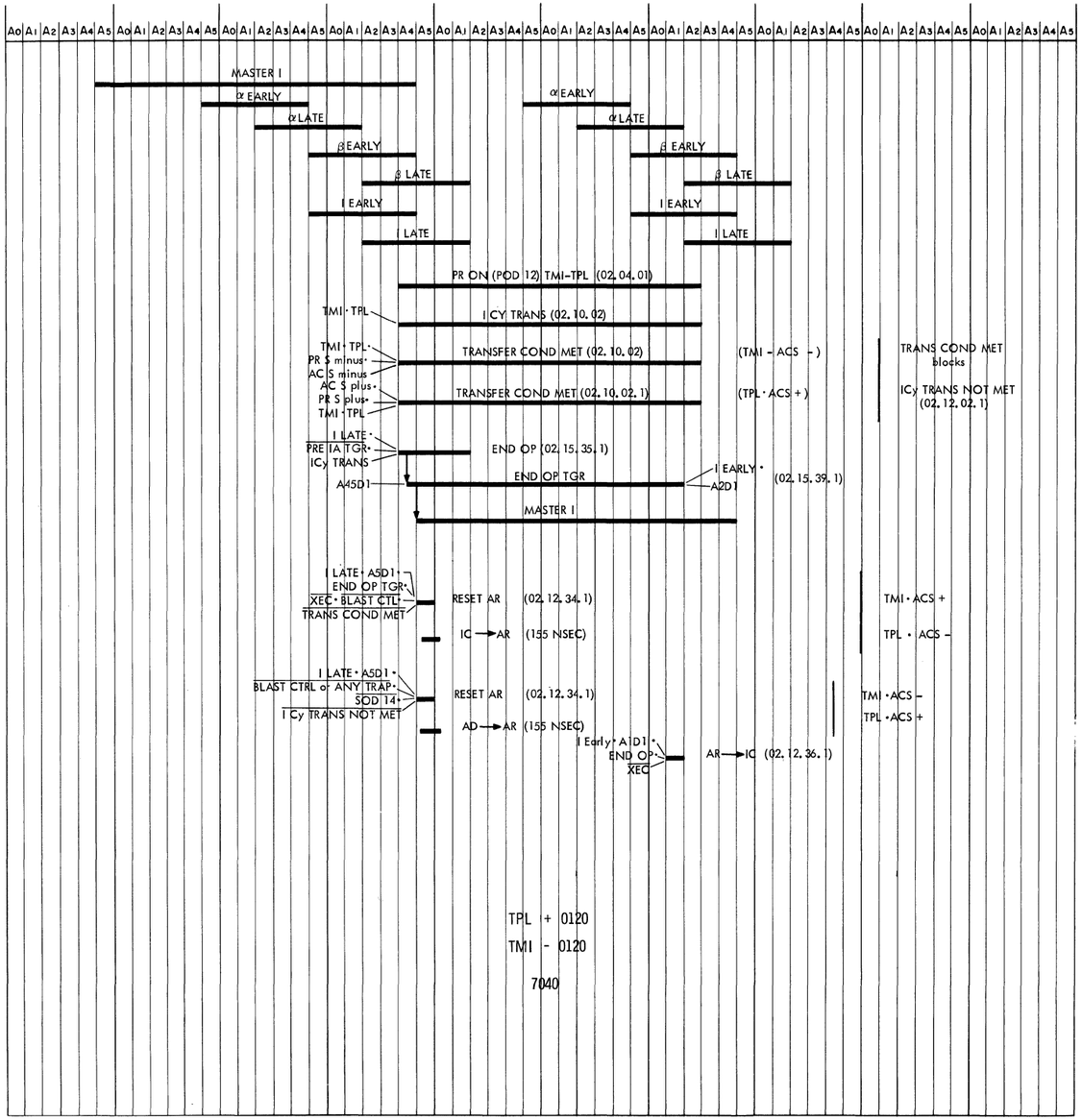
ALPHA CODE: TM1 CYCLES: 1



SEQUENCE NOTES:

IF AC(S) IS —, THE COMPUTER TAKES ITS NEXT INSTRUCTION FROM Y AND CONTINUES.

*3 AD_{21-35} ⟶ AR IF AC(S) IS —.
IC ⟶ AR IF AC(S) IS NOT —.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TPL		00003	012000 000003
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			377777 777777

Transfer on Plus (TPL)

CONSOLE INDICATORS																							
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	377777777777	377777777777	00												
I	I	00002	+120	000	0	00003	012000000003	377777777777	00												
I	I	00004	+020	000	0	00000	002000000000	377777777777	00												
I	E	00001	+500	000	0	00006	050000000006	377777777777	00												

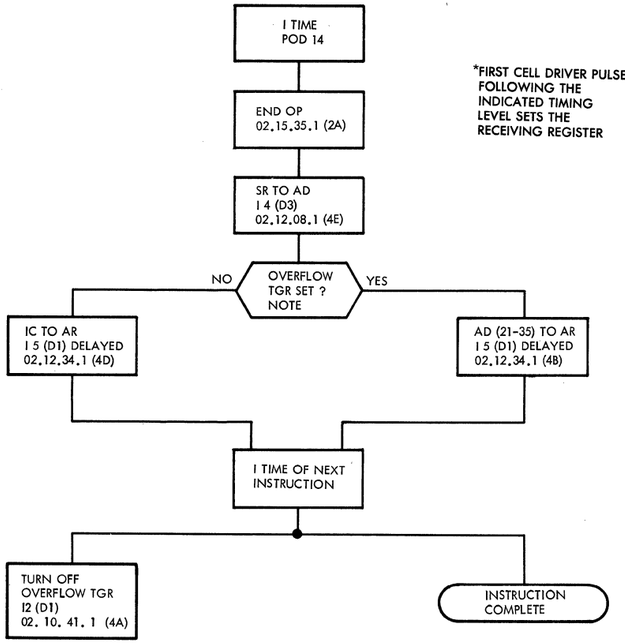
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	TMI		00003	412000 000003
00002	HPR		00000	042000 000000
00003	TRA		00000	002000 000000
00004				
00005				
00006	Pattern			400000 000000

Transfer on Minus (TMI)

CONSOLE INDICATORS																							
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	400000000000	400000000000	00												
I	I	00002	-120	000	0	00003	412000000003	400000000000	00												
I	I	00004	+020	000	0	00000	002000000000	400000000000	00												
I	E	00001	+500	000	0	00006	050000000006	400000000000	00												

NOTE: If the Sign of the accumulator is plus, this routine hangs up with the cycle Time L indicator on

Transfer on Overflow (TOV +0140)
If the overflow indicator is on, it is turned off and the computer takes its next instruction from the location specified by the address field of the instruction word. If the indicator is off, the computer takes the next sequential instruction.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

NOTE:
THE OVERFLOW TRIGGER IS SET BY :
1. AD-AC AND POD 40 AND SIGNS ALIKE *AND AD 1 CARRY.*
2. AC LEFT INSTRUCTION AND AC (1) = 1 AND SC $\neq$ 0 .

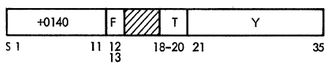
LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0140 TRANSFER ON OVERFLOW

ALPHA CODE: TOV CYCLES: 1



SEQUENCE NOTES:

IF AC OVERFLOW INDICATOR IS ON, THE COMPUTER TURNS OFF THE INDICATOR AND TAKES ITS NEXT INSTRUCTION FROM Y.

*3 AD_{21-35} → AR IF AC OVFLOW ON.
(TURN OFF INDICATORS)

IC → AR IF AC OVFLW NOT ON.

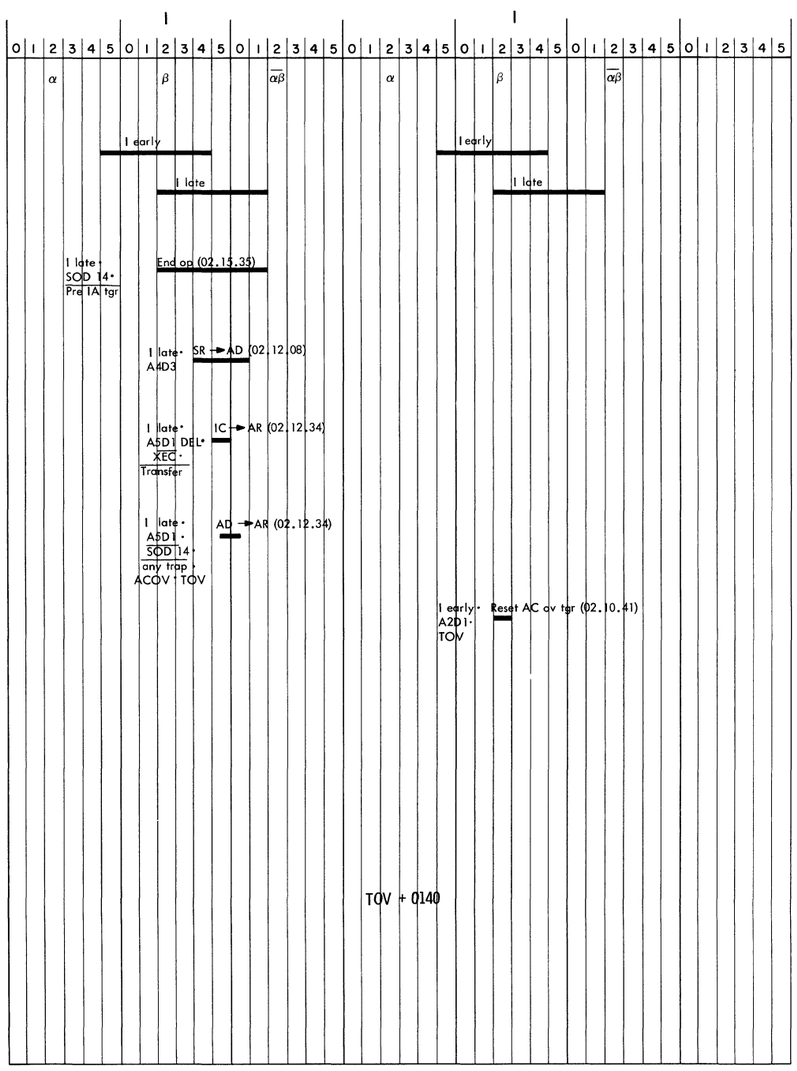


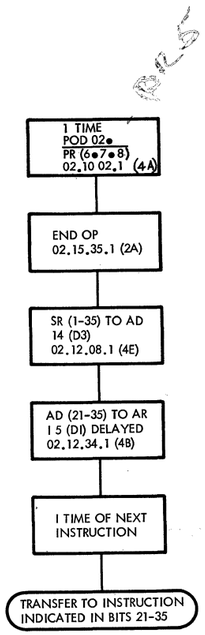
FIGURE 42. TOV

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00005	050000 000005
00001	ADD		00006	040000 000006
00002	TOV		00004	014000 000004
00003	HPR		00000	042000 000000
00004	TRA		00000	002000 000000
00005	Pattern			000000 000001
00006	Pattern			377777 777777

Transfer on Overflow (TOV)

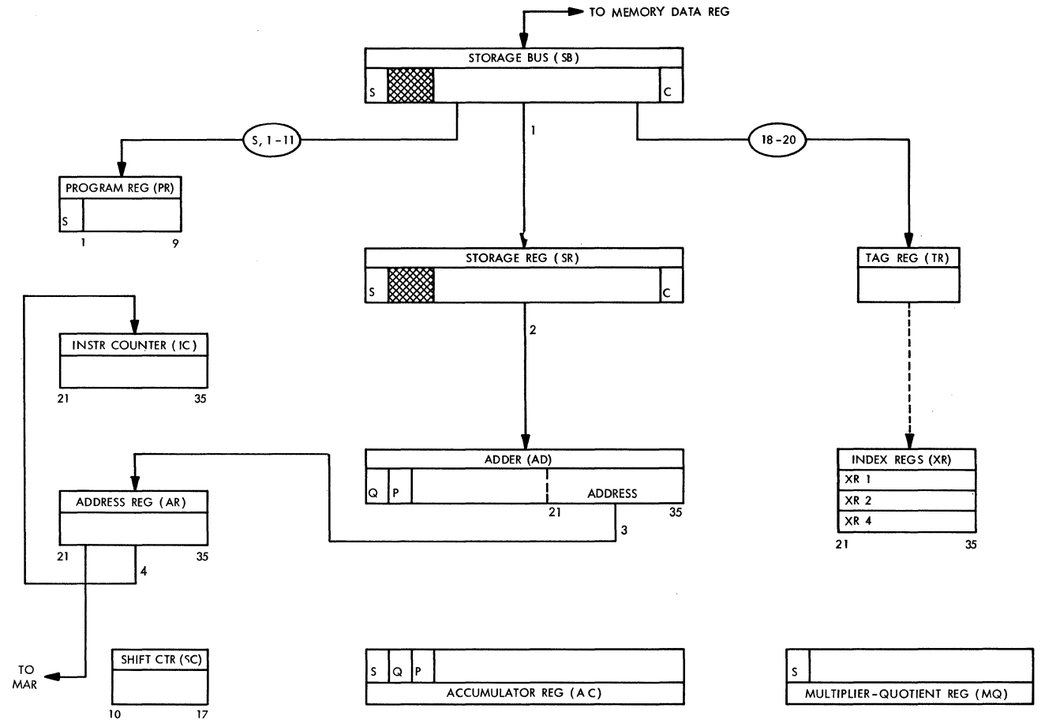
		CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00005	050000000005	000000000000	00												
E	I	00001	+500	000	0	00001	000000000001	000000000001	00												
I	E	00002	+400	000	0	00006	040000000006	000000000001	00												
E	I	00002	+400	000	0	00002	377777777777	000000000000	01				1		1		1				
I	I	00003	+140	000	0	00004	014000000004	000000000000	01				1		0		0				
I	I	00005	+020	000	0	00000	002000000000	000000000000	01				0		0		0				
I	E	00001	+500	000	0	00005	050000000005	000000000000	01				0		0		0				

Transfer (TRA +0020)
Causes the computer to take its next instruction from the location specified by the address field of the instruction word.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 43. TRA



LEGEND

1 CYCLE

E CYCLE

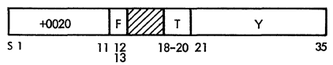
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

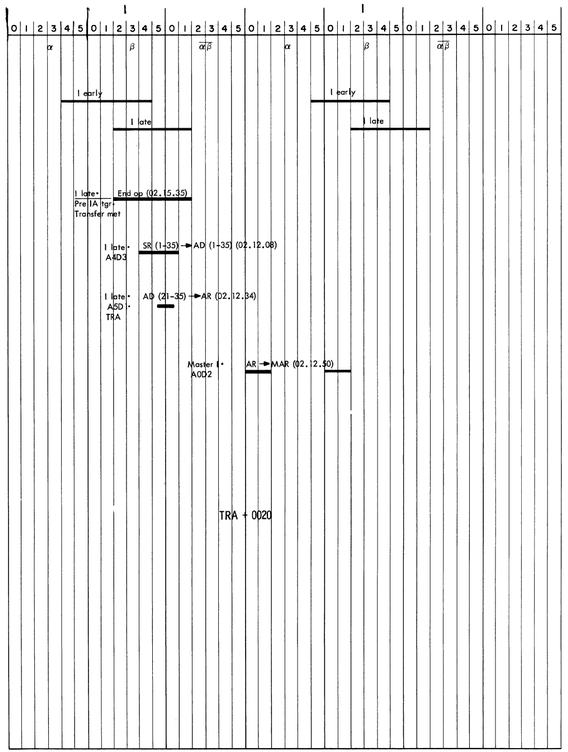
INST +0020 TRANSFER

ALPHA CODE: TRA CYCLES: 1



SEQUENCE NOTES:

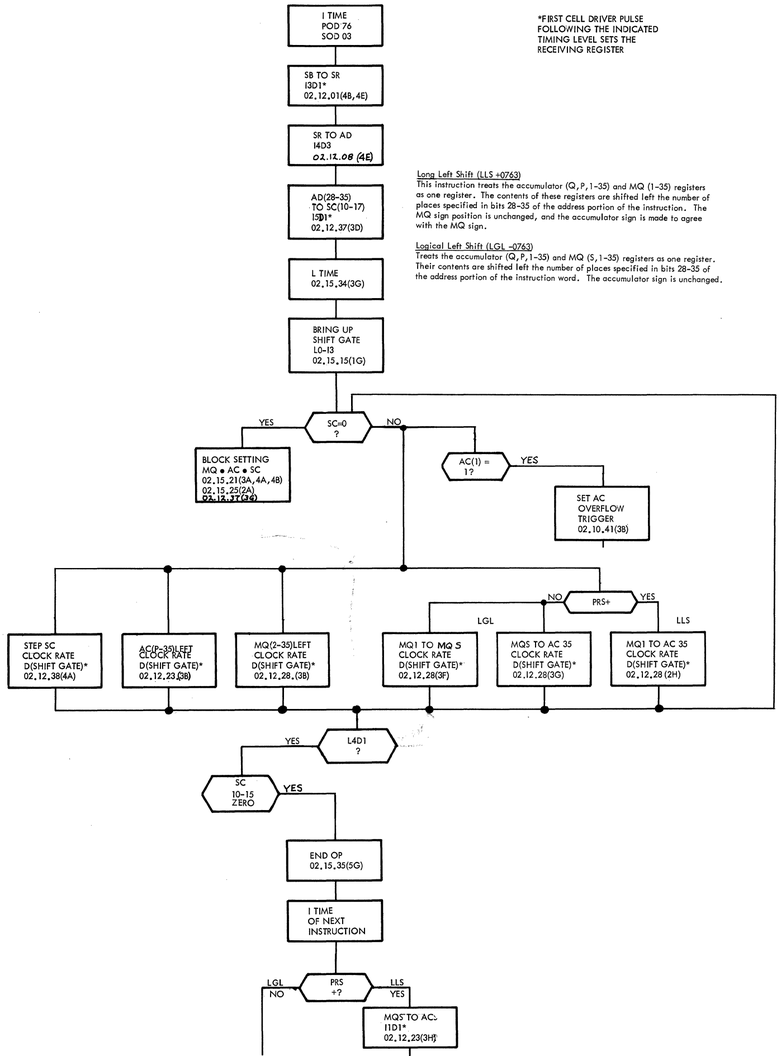
CAUSES THE COMPUTER TO TAKE ITS NEXT INSTRUCTION FROM LOCATION Y AND CONTINUE FROM THERE.



Location Switches	Inst	Tag	Address	Octal Equiv
00000	TRA		00002	002000 000002
00001	HPR		00000	042000 000000
00002	TRA		00005	002000 000005
00003	HPR		00000	042000 000000
00004	HPR		00000	042000 000000
00005	TRA		00000	002000 000000

Transfer (TRA)

CONSOLE INDICATORS																					
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF 1	FF 2
I	I	00001	+020	000	0	00002	002000000002														
I	I	00003	+020	000	0	00005	002000000005														
I	I	00006	+020	000	0	00000	002000000000														

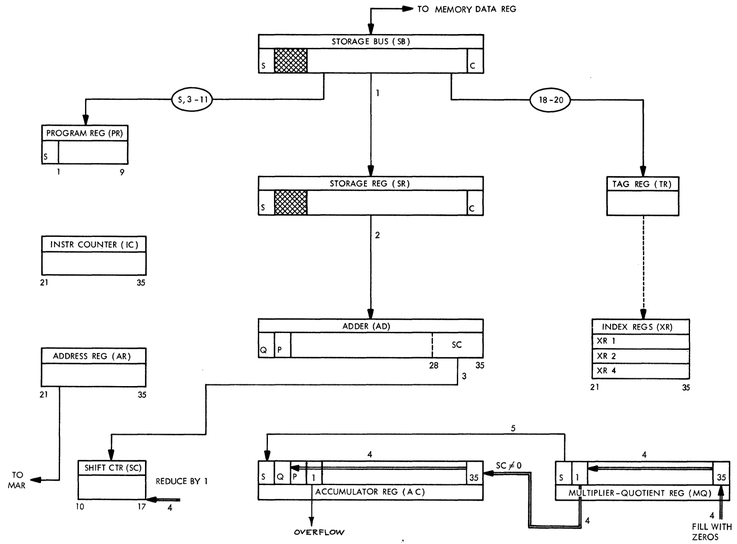


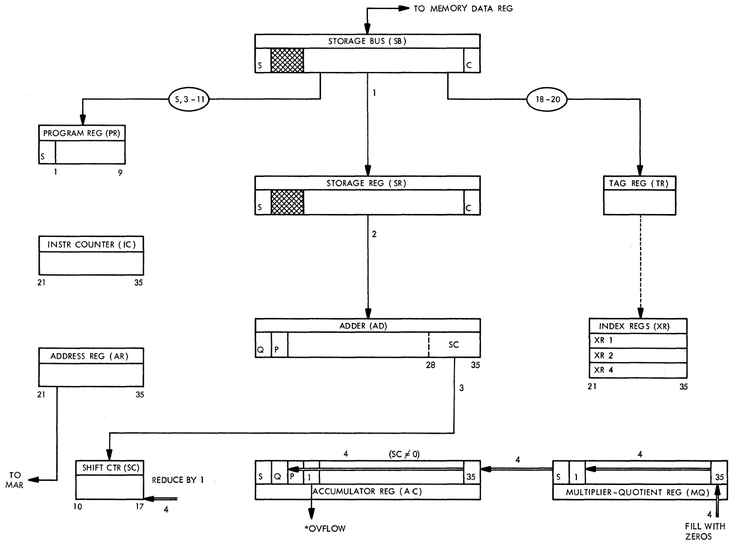
*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

Long Left Shift (LLS +0763)
This instruction treats the accumulator (Q,P,1-35) and MQ (1-35) registers as one register. The contents of these registers are shifted left the number of places specified in bits 28-35 of the address portion of the instruction. The MQ sign position is unchanged, and the accumulator sign is made to agree with the MQ sign.

Logical Left Shift (LGL -0763)
Treats the accumulator (Q,P,1-35) and MQ (5,1-35) registers as one register. Their contents are shifted left the number of places specified in bits 28-35 of the address portion of the instruction word. The accumulator sign is unchanged.

FIGURE 44. LLS,LGL





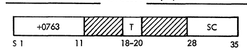
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0763 LONG LEFT SHIFT

ALPHA CODE: LLS CYCLES: I, L, ---



SEQUENCE NOTES:

THE $C(AC)_{Q, P, 1-35}$ AND $C(MQ)_{1-35}$ ARE TREATED AS ONE REGISTER.

THEIR CONTENTS ARE SHIFTED LEFT THE NUMBER OF PLACES INDICATED IN 28-35.

THE AC SIGN IS SET EQUAL TO THE MQ SIGN.

VACATED BITS ARE FILLED WITH ZEROS.

OVERFLOW POSSIBLE.

CYCLES REQUIRED: 7040: 1-4 2/3
7044: 2-13

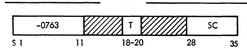
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0763 LOGICAL LEFT SHIFT

ALPHA CODE: LGL CYCLES: I, L, ---



SEQUENCE NOTES:

THE $C(AC)_{Q, P, 1-35}$ AND $C(MQ)_{S, 1-35}$ ARE TREATED AS ONE REGISTER.

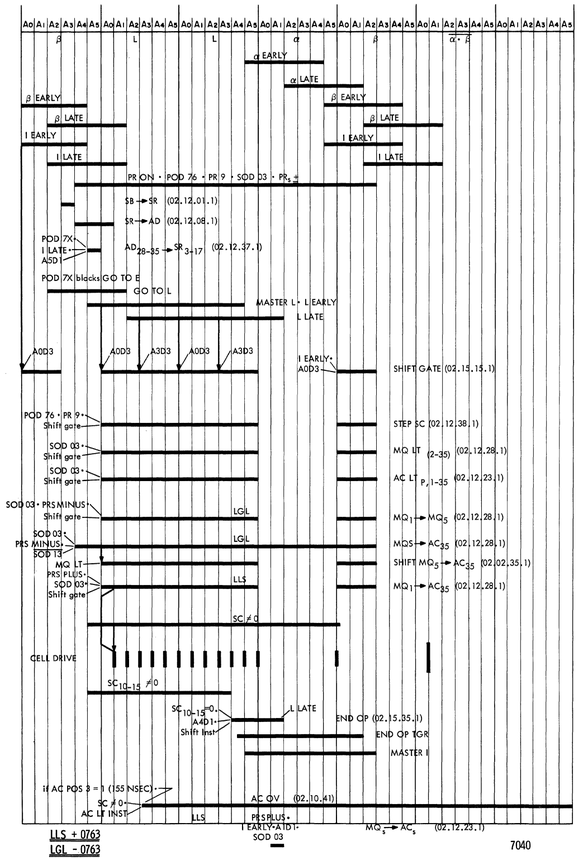
THEIR CONTENTS ARE SHIFTED LEFT THE NUMBER OF PLACES INDICATED IN 28-35.

THE SIGN OF THE AC IS UNCHANGED.

VACATED BITS ARE FILLED WITH ZEROS.

OVFLOW POSSIBLE.

CYCLES REQUIRED: 7040: 1-4 2/3
7044: 2-13



LLS + 0763

LGL - 0763

7040

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00006	056000 000006
00001	LLS		00043	076300 000043
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			377777 777777

Long Left Shift (LLS)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF 1	FF 2
I	E	00001	+560	000	0	00006	056000000006	0000000000	00	000000000000											
E	I	00001	+560	000	0	00001	377777777777	0000000000	00	377777777777											
I	L(1)	00002	+763	043	0	00043	076300000043	0000000000	00	377777777777											
L(1)	L(2)	00002	+763	035	0	00043	076300000043	0000000077	00	377777777700											
L(2)	L(3)	00002	+763	027	0	00043	076300000043	0000000777	00	377777770000											
L(3)	L(4)	00002	+763	021	0	00043	076300000043	0000077777	00	377777000000											
L(4)	L(5)	00002	+763	013	0	00043	076300000043	0000777777	00	377700000000											
L(5)	L(6)	00002	+763	005	0	00043	076300000043	0077777777	00	370000000000									1		
L(6)	I	00002	+763	000	0	00002	076300000043	3777777777	00	000000000000									1		
I	I	00003	+020	000	0	00000	002000000000	3777777777	00	000000000000									1		
I	E	00001	+560	000	0	00006	056000000006	3777777777	00	000000000000									1		
E	I	00001	+560	000	0	00001	377777777777	3777777777	00	377777777777									1		
I	L(1)	00002	+763	043	0	00043	076300000043	3777777777	00	377777777777			1						1		
L(1)	L(2)	00002	+763	035	0	00043	076300000043	3777777777	11	377777777700			1						1		
L(2)	L(3)	00002	+763	027	0	00043	076300000043	3777777777	11	377777770000			1						1		
L(3)	L(4)	00002	+763	021	0	00043	076300000043	3777777777	11	377777000000			1						1		
L(4)	L(5)	00002	+763	013	0	00043	076300000043	3777777777	11	377700000000			1						1		
L(5)	L(6)	00002	+763	005	0	00043	076300000043	3777777777	11	370000000000			1						1		
L(6)	I	00002	+763	000	0	00002	076300000043	3777777777	11	000000000000			1						1		
I	I	00003	+020	000	0	00000	002000000000	3777777777	11	000000000000			1						1		
I	E	00001	+560	000	0	00006	056000000006	3777777777	11	000000000000			1						1		
E	I	00001	+560	000	0	00001	377777777777	3777777777	11	377777777777			1						1		
I	L(1)	00002	+763	043	0	00043	076300000043	3777777777	11	377777777777			1						1		

Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00006	056000 000006
00001	LGL		00044	476300 000044
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			777777 777777

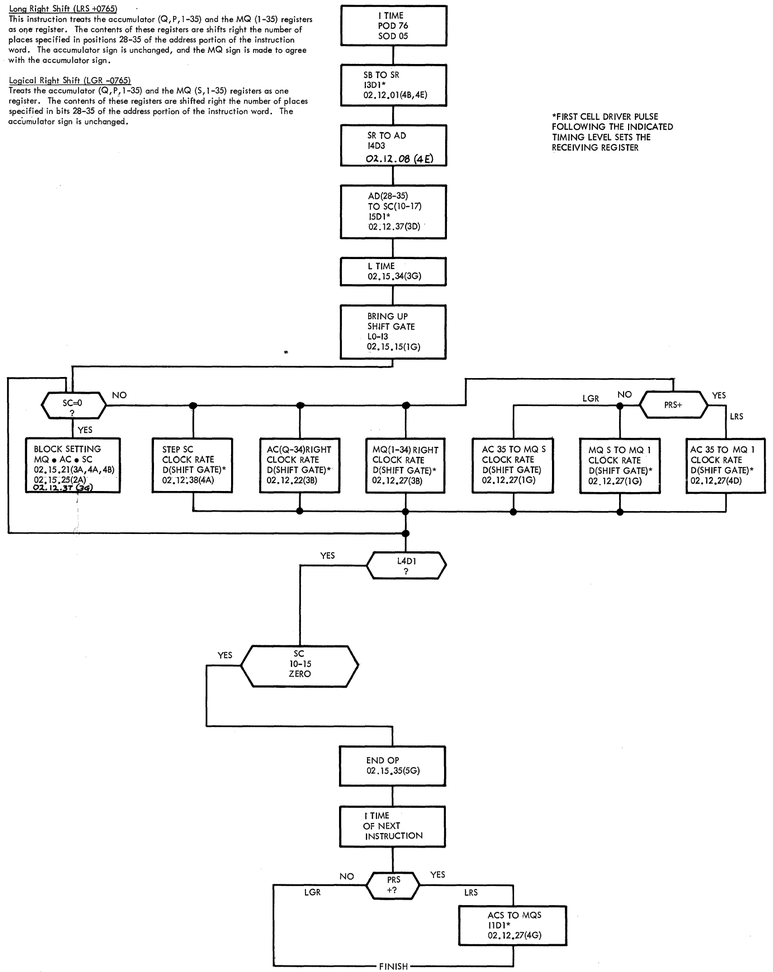
Logical Left Shift (LGL)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU. OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FF 1	FF 2
I	E	00001	+560	000	0	00006	056000000006	0000000000	00	000000000000											
E	I	00001	+560	000	0	00001	777777777777	0000000000	00	777777777777											
I	L(1)	00002	-763	044	0	00044	476300000044	0000000000	00	777777777777											
L(1)	L(2)	00002	-763	036	0	00044	476300000044	0000000077	00	777777777700											
L(2)	L(3)	00002	-763	030	0	00044	476300000044	0000000777	00	777777770000											
L(3)	L(4)	00002	-763	022	0	00044	476300000044	0000007777	00	777777000000											
L(4)	L(5)	00002	-763	014	0	00044	476300000044	0000077777	00	777700000000											
L(5)	L(6)	00002	-763	006	0	00044	476300000044	0077777777	00	770000000000										1	
L(6)	I	00002	-763	000	0	00002	476300000044	3777777777	01	000000000000			1							1	
I	I	00003	+020	000	0	00000	002000000000	3777777777	01	000000000000			1							1	
I	E	00001	+560	000	0	00006	056000000006	3777777777	01	000000000000			1							1	
E	I	00001	+560	000	0	00001	777777777777	3777777777	01	777777777777			1							1	
I	L(1)	00002	-763	044	0	00044	476300000044	3777777777	01	777777777777			1							1	
L(1)	L(2)	00002	-763	036	0	00044	476300000044	3777777777	11	777777777700			1							1	
L(2)	L(3)	00002	-763	030	0	00044	476300000044	3777777777	11	777777770000			1							1	
L(3)	L(4)	00002	-763	022	0	00044	476300000044	3777777777	11	777777000000			1							1	
L(4)	L(5)	00002	-763	014	0	00044	476300000044	3777777777	11	777700000000			1							1	
L(5)	L(6)	00002	-763	006	0	00044	476300000044	3777777777	11	770000000000			1							1	
L(6)	I	00002	-763	000	0	00002	476300000044	3777777777	11	000000000000			1							1	
I	I	00002	+020	000	0	00000	002000000000	3777777777	11	000000000000			1							1	
I	E	00003	+560	000	0	00006	056000000000	3777777777	11	000000000000			1							1	
E	I	00002	+560	000	0	00001	777777777777	3777777777	11	777777777777			1							1	
I	L(1)	00002	-763	044	0	00044	476300000044	3777777777	11	777777777777			1							1	

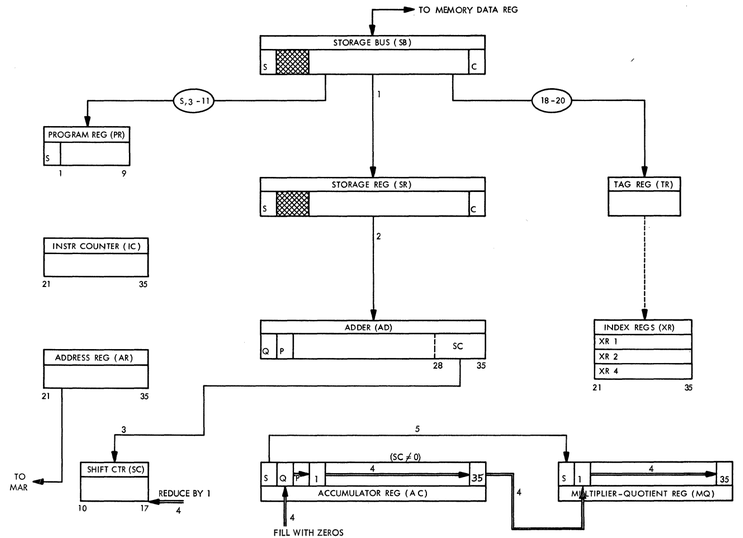
Long Right Shift (LRS +0765)
This instruction treats the accumulator (Q,P,1-35) and the MQ (1-35) registers as one register. The contents of these registers are shifts right the number of places specified in positions 28-35 of the address portion of the instruction word. The accumulator sign is unchanged, and the MQ sign is made to agree with the accumulator sign.

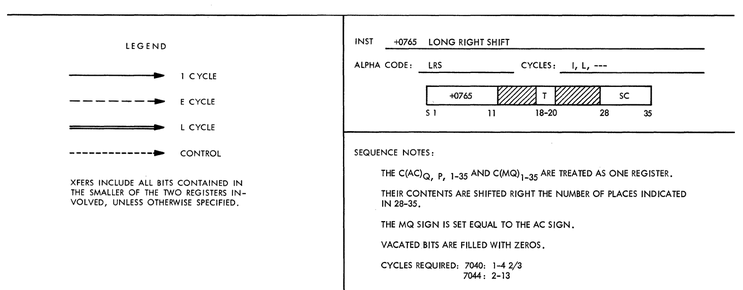
Logical Right Shift (LGR -0765)
Treats the accumulator (Q,P,1-35) and the MQ (S,1-35) registers as one register. The contents of these registers are shifted right the number of places specified in bits 28-35 of the address portion of the instruction word. The accumulator sign is unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

FIGURE 45. LRS,LGR





INST +0765 LONG RIGHT SHIFT

ALPHA CODE: LRS CYCLES: I, L, ---

SEQUENCE NOTES:

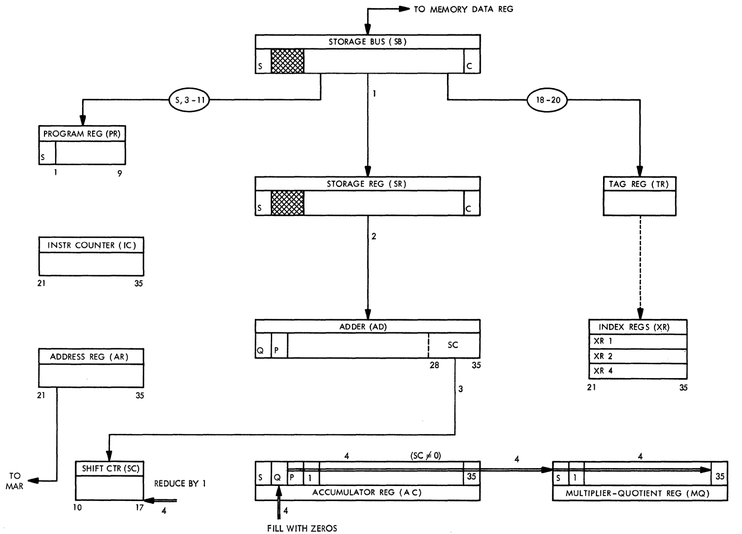
THE $C(AC)_{Q, P, 1-35}$ AND $C(MQ)_{1-35}$ ARE TREATED AS ONE REGISTER.

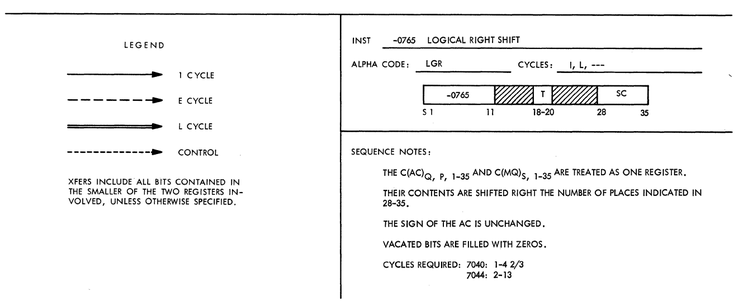
THEIR CONTENTS ARE SHIFTED RIGHT THE NUMBER OF PLACES INDICATED IN 28-35.

THE MQ SIGN IS SET EQUAL TO THE AC SIGN.

VACATED BITS ARE FILLED WITH ZEROS.

CYCLES REQUIRED: 7040: 1-4 2/3
7044: 2-13





INST -0765 LOGICAL RIGHT SHIFT

ALPHA CODE: LGR CYCLES: I, L, ---

SEQUENCE NOTES:

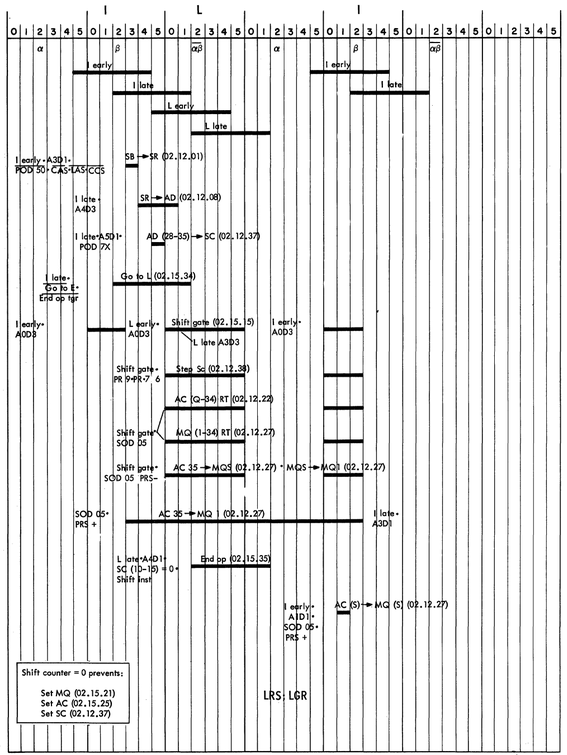
THE $C(AC)_{Q, P, 1-35}$ AND $C(MQ)_{S, 1-35}$ ARE TREATED AS ONE REGISTER.

THEIR CONTENTS ARE SHIFTED RIGHT THE NUMBER OF PLACES INDICATED IN 28-35.

THE SIGN OF THE AC IS UNCHANGED.

VACATED BITS ARE FILLED WITH ZEROS.

CYCLES REQUIRED: 7040: 1-4 2/3
7044: 2-13



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	LRS		00043	076500 000043
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			377777 777777

Long Right Shift (LRS)

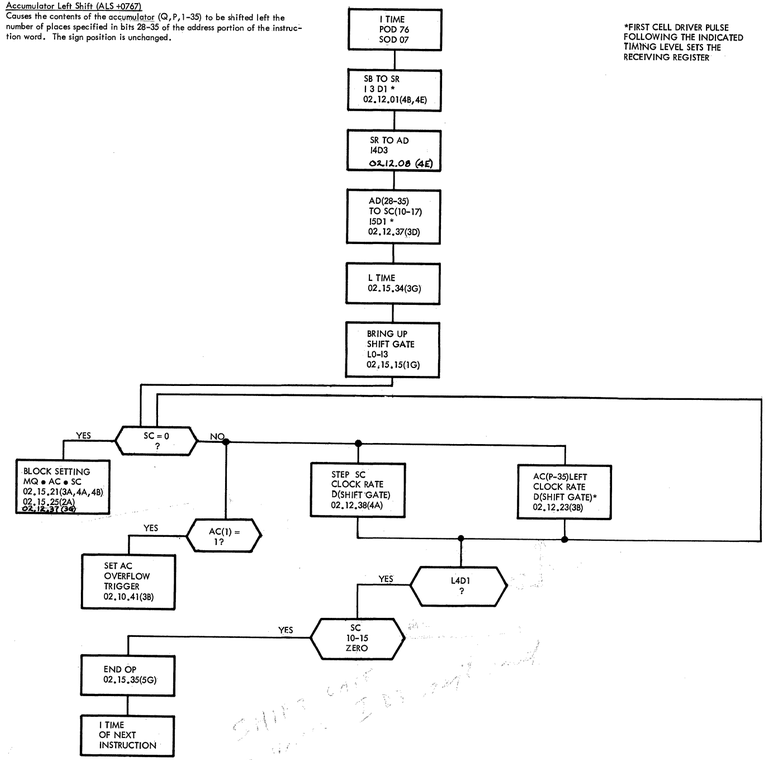
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	CONSOLE INDICATORS: INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	Y OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	000000000000											
E	I	00001	+500	000	0	00001	377777777777	377777777777	00	000000000000											
I	L(1)	00002	+765	043	0	00043	076500000043	377777777777	00	000000000000											
L(1)	L(2)	00002	+765	035	0	00043	076500000043	003777777777	00	374000000000											
L(2)	L(3)	00002	+765	027	0	00043	076500000043	000037777777	00	377740000000											
L(3)	L(4)	00002	+765	021	0	00043	076500000043	000000377777	00	377777400000											
L(4)	L(5)	00002	+765	013	0	00043	076500000043	000000003777	00	377777774000											
L(5)	L(6)	00002	+765	005	0	00043	076500000064	000000000037	00	377777777740											
L(6)	I	00002	+765	000	0	00002	076500000043	000000000000	00	377777777777											
I	I	00003	+020	000	0	00000	002000000000	000000000000	00	377777777777											
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	377777777777											
E	I	00001	+500	000	0	00001	377777777777	377777777777	00	377777777777											
I	L(1)	00002	+765	043	0	00043	076500000043	377777777777	00	377777777777											
L(1)	L(2)	00002	+765	035	0	00043	076500000043	003777777777	00	377777777777											
L(2)	L(3)	00002	+765	027	0	00043	076500000043	000037777777	00	377777777777											
L(3)	L(4)	00002	+765	021	0	00043	076500000043	000000377777	00	377777777777											
L(4)	L(5)	00002	+765	013	0	00043	076500000043	000000003777	00	377777777777											
L(5)	L(6)	00002	+765	005	0	00043	076500000043	000000000037	00	377777777777											
L(6)	I	00002	+765	000	0	00002	076500000043	000000000000	00	377777777777											
I	I	00003	+020	000	0	00000	002000000000	000000000000	00	377777777777											
I	E	00001	+500	000	0	00006	050000000006	000000000000	00	377777777777											

Location Switches	Inst	Tag	Address	Octal Equiv
00000	CAL		00006	450000 000006
00001	LGR		00044	476500 000044
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			777777 777777

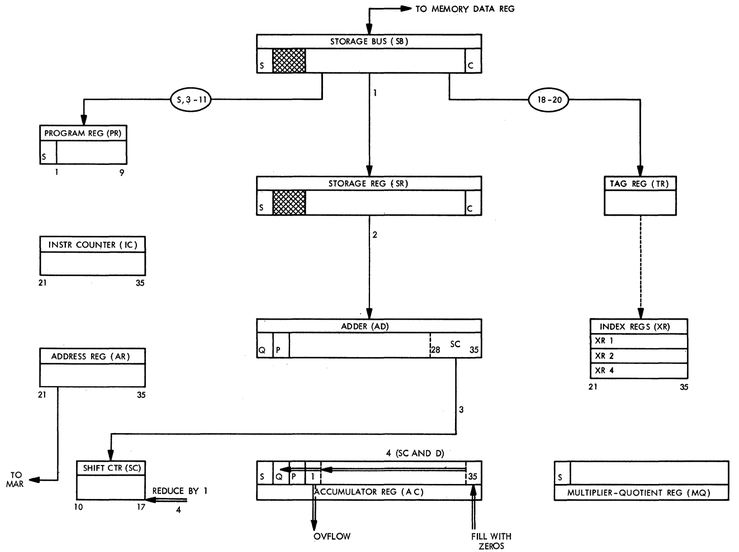
Logical Right Shift (LGR)

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	CONSOLE INDICATORS: INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	P CARRY	Y OVERFLOW	FP 1	FP 2
I	E	00001	-500	000	0	00006	450000000006	000000000000	00	000000000000											
E	I	00001	-500	000	0	00001	777777777777	377777777777	01	000000000000											
I	L(1)	00002	-765	044	0	00044	476500000044	377777777777	01	000000000000											
L(1)	L(2)	00002	-765	036	0	00044	476500000044	007777777777	00	770000000000											
L(2)	L(3)	00002	-765	030	0	00044	476500000044	000077777777	00	777700000000											
L(3)	L(4)	00002	-765	022	0	00044	476500000044	000000777777	00	777777000000											
L(4)	L(5)	00002	-765	014	0	00044	476500000044	000000007777	00	777777770000											
L(5)	L(6)	00002	-765	006	0	00044	476500000044	000000000077	00	777777777700											
L(6)	I	00002	-765	000	0	00002	476500000044	000000000000	00	777777777777											
I	I	00003	+020	000	0	00000	002000000000	000000000000	00	777777777777											
I	E	00001	-500	000	0	00006	450000000006	000000000000	00	777777777777											
E	I	00001	-500	000	0	00001	777777777777	377777777777	01	777777777777											
I	L(1)	00002	-765	044	0	00044	476500000044	377777777777	01	777777777777											
L(1)	L(2)	00002	-765	036	0	00044	476500000044	007777777777	00	777777777777											
L(2)	L(3)	00002	-765	030	0	00044	476500000044	000077777777	00	777777777777											
L(3)	L(4)	00002	-765	022	0	00044	476500000044	000000777777	00	777777777777											
L(4)	L(5)	00002	-765	014	0	00044	476500000044	000000007777	00	777777777777											
L(5)	L(6)	00002	-765	006	0	00044	476500000044	000000000077	00	777777777777											

Accumulator Left Shift (ALS +0767)
Causes the contents of the accumulator (Q,P,1-35) to be shifted left the number of places specified in bits 28-35 of the address portion of the instruction word. The sign position is unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



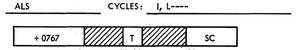
LEGEND

1 CYCLE
E CYCLE
L CYCLE
CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0767 ACCUMULATOR LEFT SHIFT

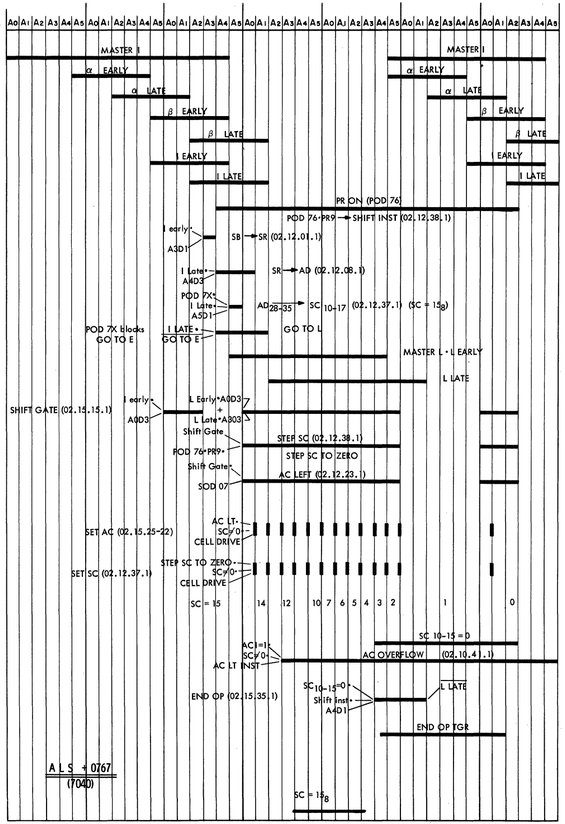
ALPHA CODE: ALS CYCLES: I, L----



SEQUENCE NOTES:

THE $C(AC)_{Q,P,1-35}$ ARE SHIFTED LEFT THE NUMBER OF PLACES INDICATED IN 28-35. SIGN POSITION IS UNCHANGED. VACATED BITS FILLED WITH ZEROS. A "1" SHIFTED OUT OF POS 1 TURNS ON AC OVFLOW.

CYCLES REQUIRED: 7040 1-2 2/3
7044 2-7



Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	ALS		00044	076000 000044
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			377777 777777

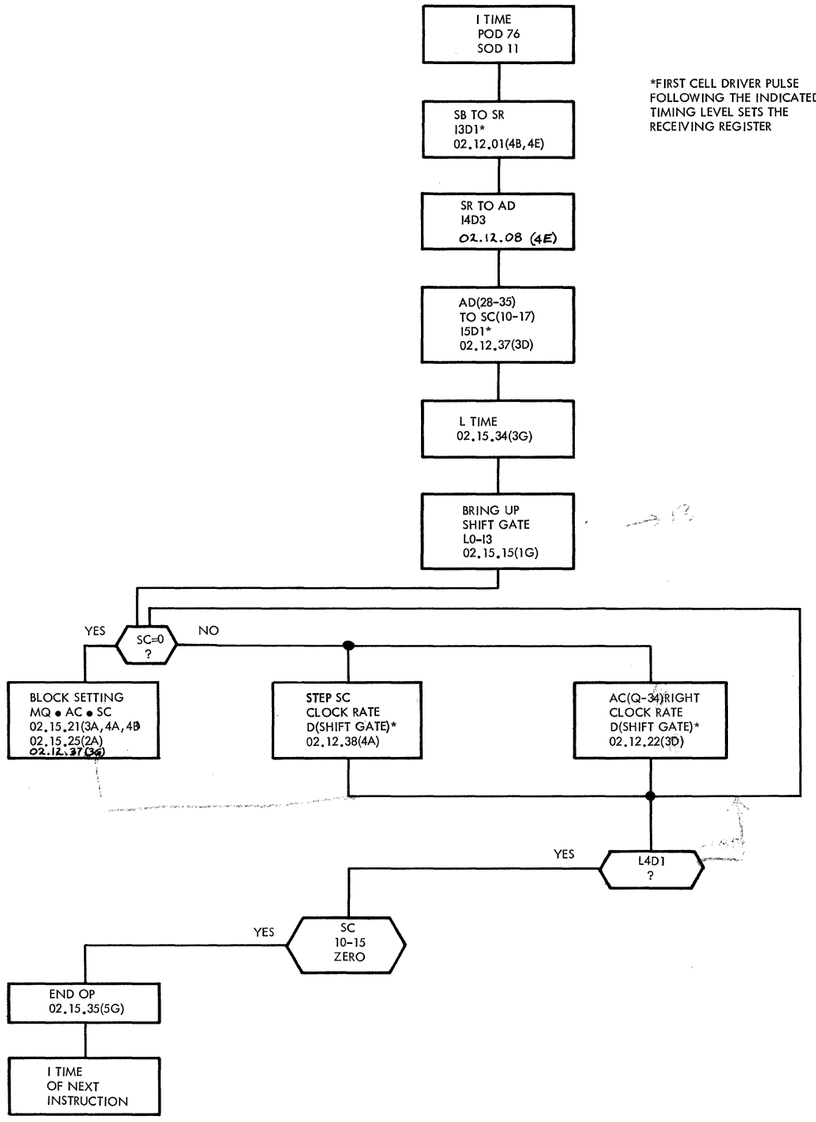
Accumulator Left Shift (ALS)

CONSOLE INDICATORS

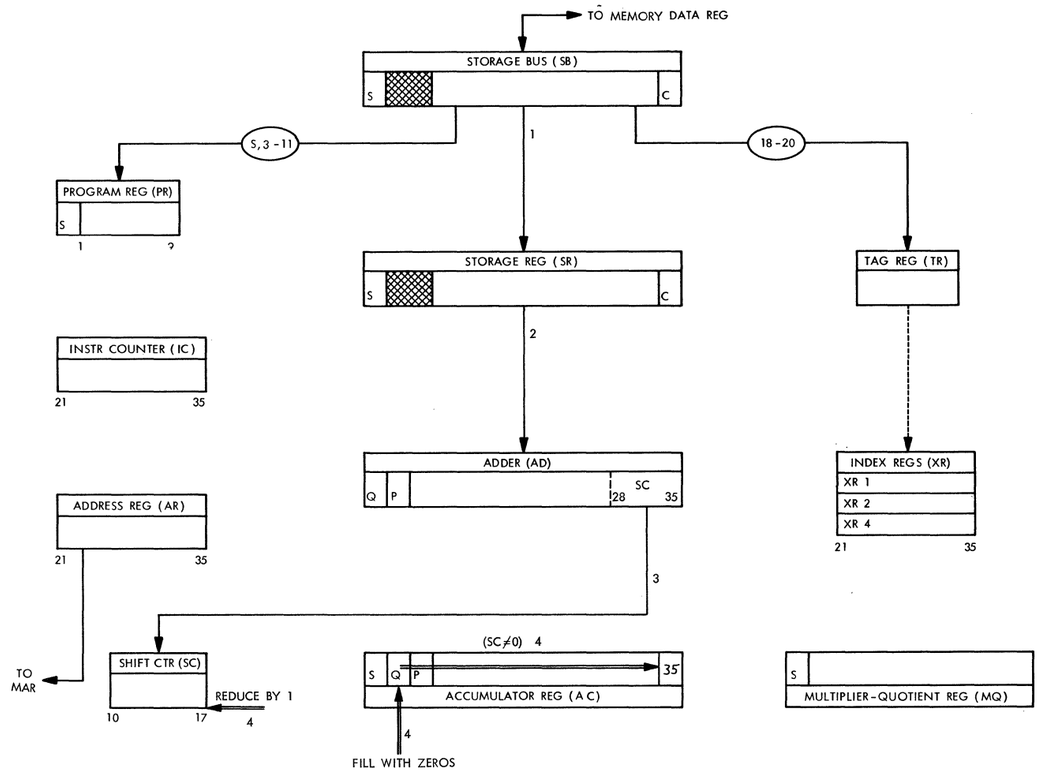
CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00				0						0		
E	I	00001	+500	000	0	00001	377777777777	377777777777	00				0						0		
I	L(1)	00002	+767	044	0	00044	076700000044	377777777777	00				1						0		
L(1)	L(2)	00002	+767	036	0	00044	076700000044	377777777700	11				1						1		
L(2)	L(3)	00002	+767	030	0	00044	076700000044	377777770000	11				1						1		
L(3)	L(4)	00002	+767	022	0	00044	076700000044	377777000000	11				1						1		
L(4)	L(5)	00002	+767	014	0	00044	076700000044	377700000000	11				1						1		
L(5)	L(6)	00002	+767	006	0	00044	076700000044	370000000000	11				1						0		
L(6)	I	00002	+767	000	0	00002	076700000044	000000000000	10				1						0		
I	I	00003	+020	000	0	00000	002000000000	000000000000	10				1						0		
I	E	00001	+500	000	0	00006	050000000006	000000000000	10				1*						0		

NOTE: To clear accumulator overflow, depress RESET.

Accumulator Right Shift (ARS +0771)
Causes the contents of the accumulator (Q, P, 1-35) to be shifted right the number of places specified in bits 28-35 of the address portion of the instruction word. The sign position is unchanged.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



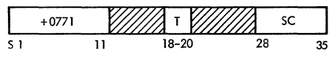
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST +0771 ACCUMULATOR RIGHT SHIFT

ALPHA CODE: ARS CYCLES: I, L,----

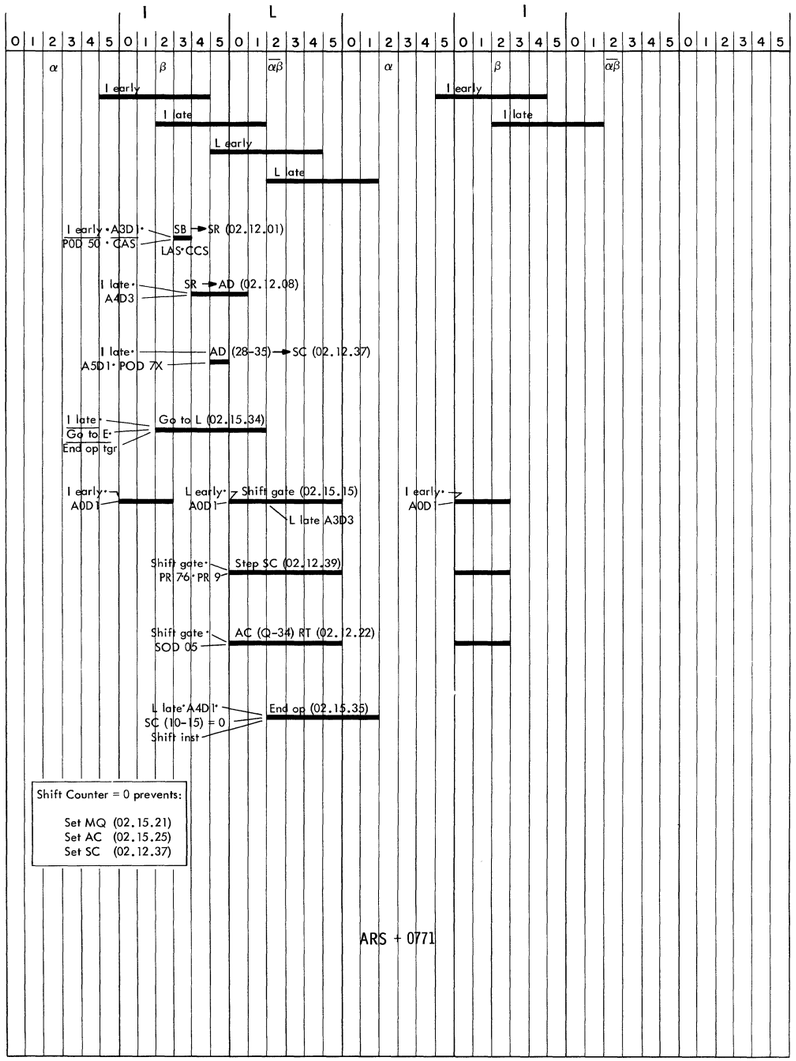


SEQUENCE NOTES:

THE $C(AC)_{Q, P, 1-35}$ ARE SHIFTED RIGHT THE NUMBER OF PLACES INDICATED IN 28-35. THE SIGN POSITION IS UNCHANGED. VACATED BITS ARE FILLED WITH ZEROS.

CYCLES REQUIRED: 7040 1-2 2/3
7044 2-7

FIGURE 47. ARS



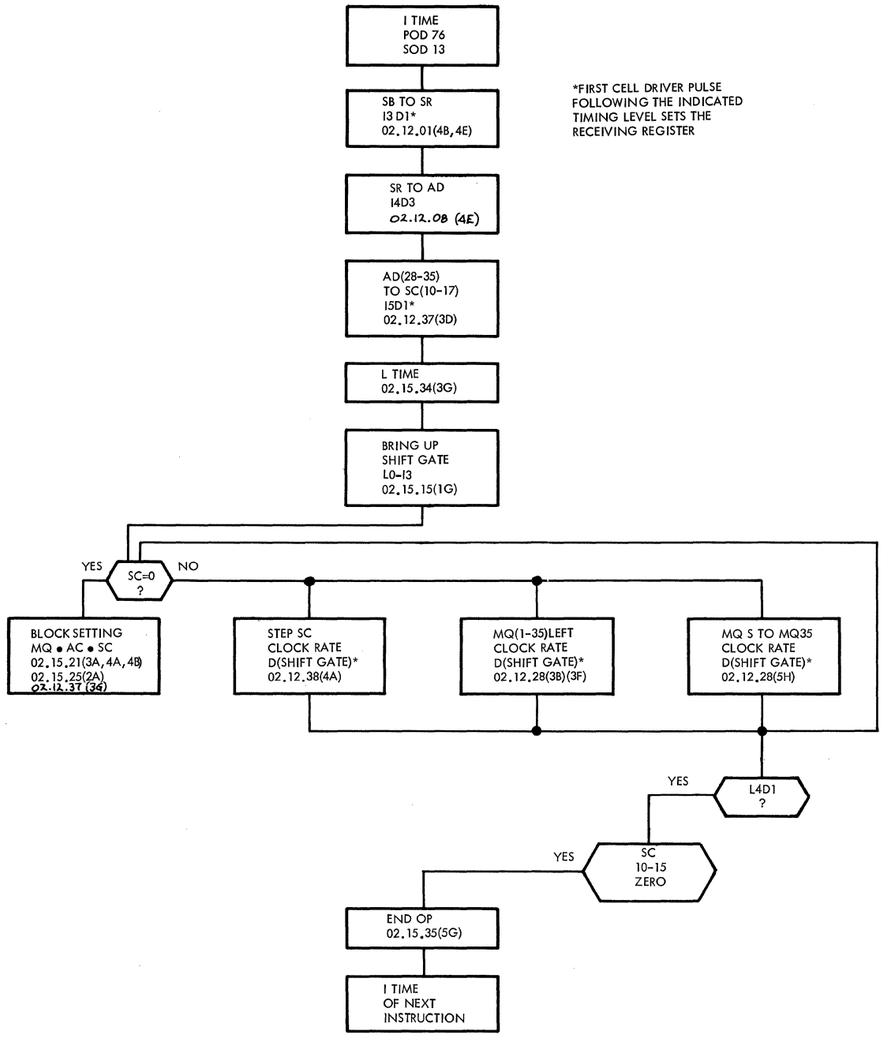
Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	ARS		00042	077100 000042
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			777777 777777

Accumulator Right Shift (ARS)

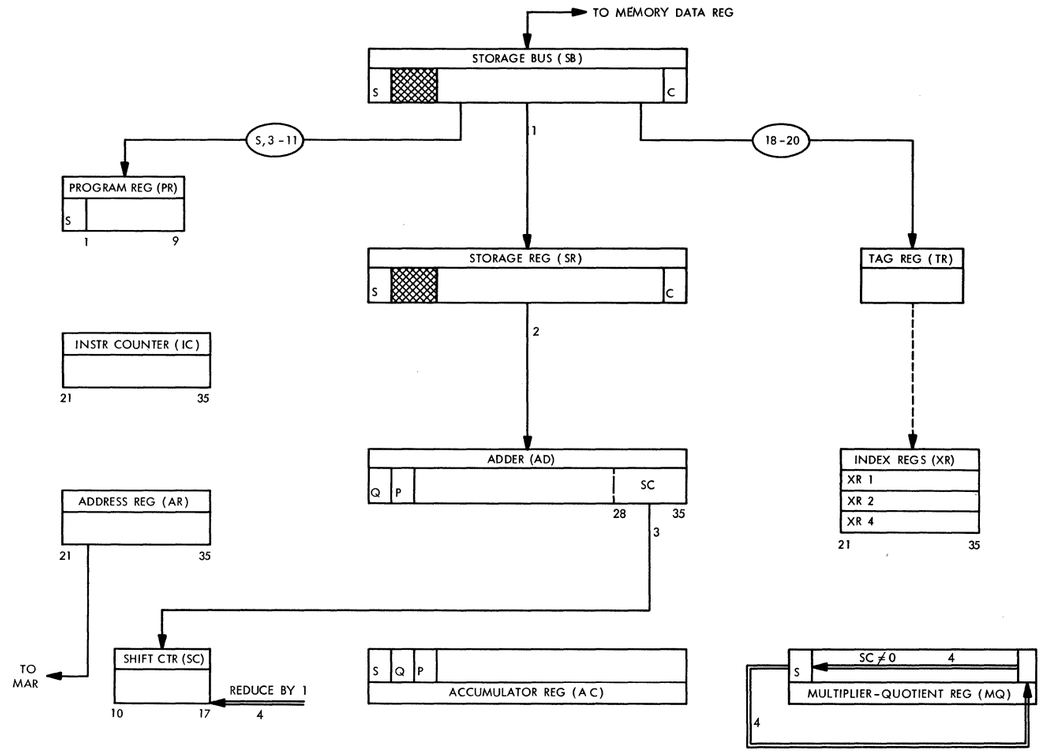
CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	E	00001	+500	000	0	00006	050000000006	000000000000	00												
E	I	00001	+500	000	0	00001	777777777777	777777777777	00												
I	L(1)	00002	+771	042	0	00042	077100000042	777777777777	00												
L(1)	L(2)	00002	+771	034	0	00042	077100000042	403777777777	00												
L(2)	L(3)	00002	+771	026	0	00042	077100000042	400037777777	00												
L(3)	L(4)	00002	+771	020	0	00042	077100000042	400000377777	00												
L(4)	L(5)	00002	+771	012	0	00042	077100000042	400000003777	00												
L(5)	L(6)	00002	+771	004	0	00042	077100000042	400000000037	00												
L(6)	I	00002	+771	000	0	00002	077100000042	400000000001	00												
I	I	00003	+020	000	0	00000	002000000000	400000000001	00												
I	E	00001	+500	000	0	00006	050000000006	400000000001	00												

Rotate MQ Left (RQL -0773)
The contents of the MQ register (S,1-35) are shifted left the number of places specified by the address portion of the instruction word. The sign position shifts into position 35; thus, the register becomes a closed loop.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



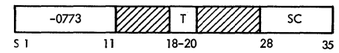
LEGEND

- 1 CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -0773 ROTATE MQ LEFT

ALPHA CODE: RQL CYCLES: I, L, ---



SEQUENCE NOTES:

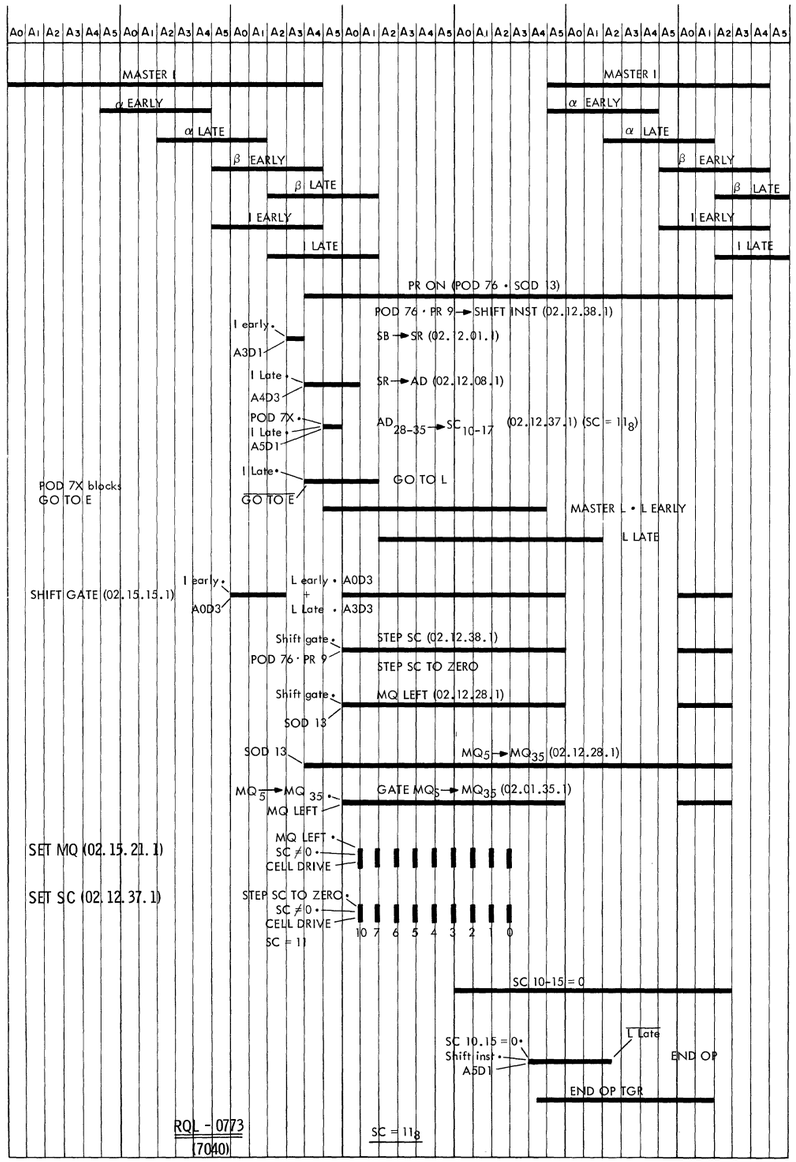
THE $C(MQ)_{S,1-35}$ ARE SHIFTED LEFT THE NUMBER OF PLACES INDICATED IN 28-35.

THE SIGN BIT IS CONNECTED TO THE 35 BIT FORMING A CLOSED SHIFTING LOOP.

NO BITS ARE LOST.

CYCLES REQUIRED: 7040: 1 - 2 2/3
7044: 2 - 7

FIGURE 48. RQL



Rotate MQ Left (RQL)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)
I	E	00001	+560	000	0	00006	056000000006			000000000000
E	I	00001	+560	000	0	00001	777777777776			777777777776
I	L(1)	00002	-773	377	0	00377	477300000377			777777777776
L(1)	L(2)	00002	-773	371	0	00377	477300000377			777777777677
L(2)	L(3)	00002	-773	363	0	00377	477300000377			777777767777
L(3)	L(4)	00002	-773	355	0	00377	477300000377			777776777777
L(4)	L(5)	00002	-773	347	0	00377	477300000377			777677777777
L(5)	L(6)	00002	-773	341	0	00377	477300000377			767777777777
L(6)	L(7)	00002	-773	333	0	00377	477300000377			777777777776
L(7)	L(8)	00002	-773	325	0	00377	477300000377			777777777677
L(8)	L(9)	00002	-773	317	0	00377	477300000377			777777767777
L(9)	L(10)	00002	-773	311	0	00377	477300000377			777776777777
L(10)	L(11)	00002	-773	303	0	00377	477300000377			777677777777
L(11)	L(12)	00002	-773	275	0	00377	477300000377			767777777777
L(12)	L(13)	00002	-773	267	0	00377	477300000377			777777777776
L(13)	L(14)	00002	-773	261	0	00377	477300000377			777777777677
L(14)	L(15)	00002	-773	253	0	00377	477300000377			777777767777
L(15)	L(16)	00002	-773	245	0	00377	477300000377			777776777777
L(16)	L(17)	00002	-773	237	0	00377	477300000377			777677777777
L(17)	L(18)	00002	-773	231	0	00377	477300000377			767777777777
L(18)	L(19)	00002	-773	223	0	00377	477300000377			777777777776
L(19)	L(20)	00002	-773	215	0	00377	477300000377			777777777677
L(20)	L(21)	00002	-773	207	0	00377	477300000377			777777767777
L(21)	L(22)	00002	-773	201	0	00377	477300000377			777776777777
L(22)	L(23)	00002	-773	173	0	00377	477300000377			777677777777
L(23)	L(24)	00002	-773	165	0	00377	477300000377			767777777777
L(24)	L(25)	00002	-773	157	0	00377	477300000377			777777777776
L(25)	L(26)	00002	-773	151	0	00377	477300000377			777777777677
L(26)	L(27)	00002	-773	143	0	00377	477300000377			777777767777
L(27)	L(28)	00002	-773	135	0	00377	477300000377			777776777777
L(28)	L(29)	00002	-773	127	0	00377	477300000377			777677777777
L(29)	L(30)	00002	-773	121	0	00377	477300000377			767777777777
L(30)	L(31)	00002	-773	113	0	00377	477300000377			777777777776
L(31)	L(32)	00002	-773	105	0	00377	477300000377			777777777677
L(32)	L(33)	00002	-773	077	0	00377	477300000377			777777767777
L(33)	L(34)	00002	-773	071	0	00377	477300000377			777776777777
L(34)	L(35)	00002	-773	063	0	00377	477300000377			777677777777
L(35)	L(36)	00002	-773	055	0	00377	477300000377			767777777777

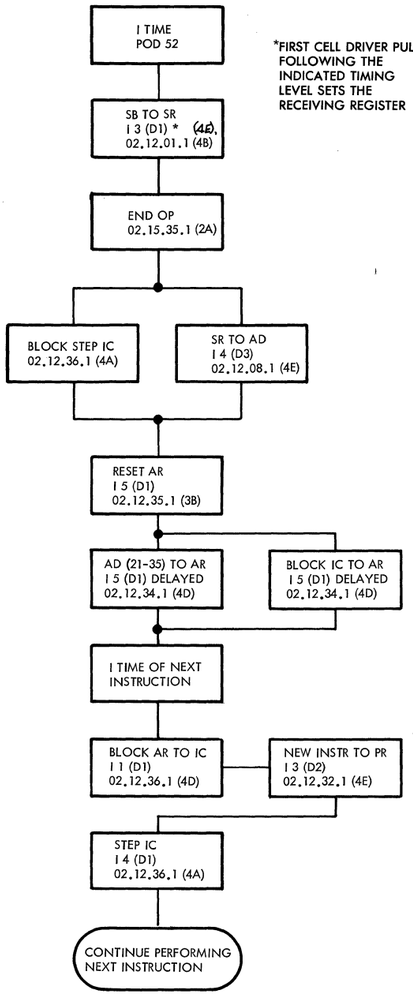
Location Switches	Inst	Tag	Address	Octal Equiv
00000	LDQ		00006	056000 000006
00001	RQL		00377	477300 000377
00002	TRA		00000	002000 000000
00003				
00004				
00005				
00006	Pattern			777777 777777

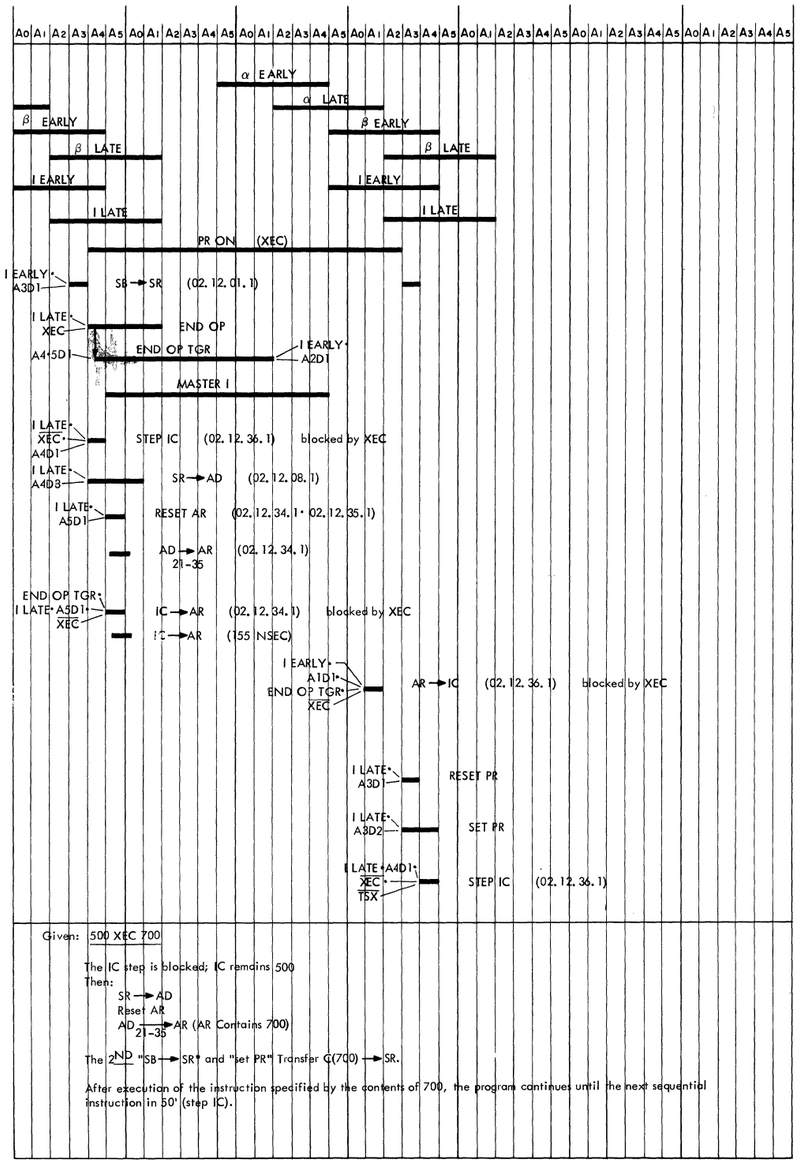
Rotate MQ Left (RQL)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)
L(36)	L(37)	00002	-773	047	0	00377	477300000377			777777777776
L(37)	L(38)	00002	-773	041	0	00377	477300000377			777777777677
L(38)	L(39)	00002	-773	033	0	00377	477300000377			777777767777
L(39)	L(40)	00002	-773	025	0	00377	477300000377			777776777777
L(40)	L(41)	00002	-773	017	0	00377	477300000377			777677777777
L(41)	L(42)	00002	-773	011	0	00377	477300000377			767777777777
L(42)	L(43)	00002	-773	003	0	00377	477300000377			777777777776
L(43)	I	00002	-773	000	0	00002	477300000377			777777777767
I	I	00003	+020	000	0	00000	002000000000			777777777767
I	I	00001	+560	000	0	00006	056000000006			777777777767

Execute (XEC +0522)
Causes the computer to execute the instruction at the location specified by the address portion of the instruction word. The computer then returns to the location plus 1 of the Execute instruction.





Location Switches	Inst	Tag	Address	Octal Equiv
00000	CLA		00006	050000 000006
00001	XEC		00005	052200 000005
00002	XEC		00005	052200 000005
00003	XEC		00004	052200 000004
00004	TRA		00000	002000 000000
00005	ADD		00006	040000 000006
00006	HPR		00000	042000 000000

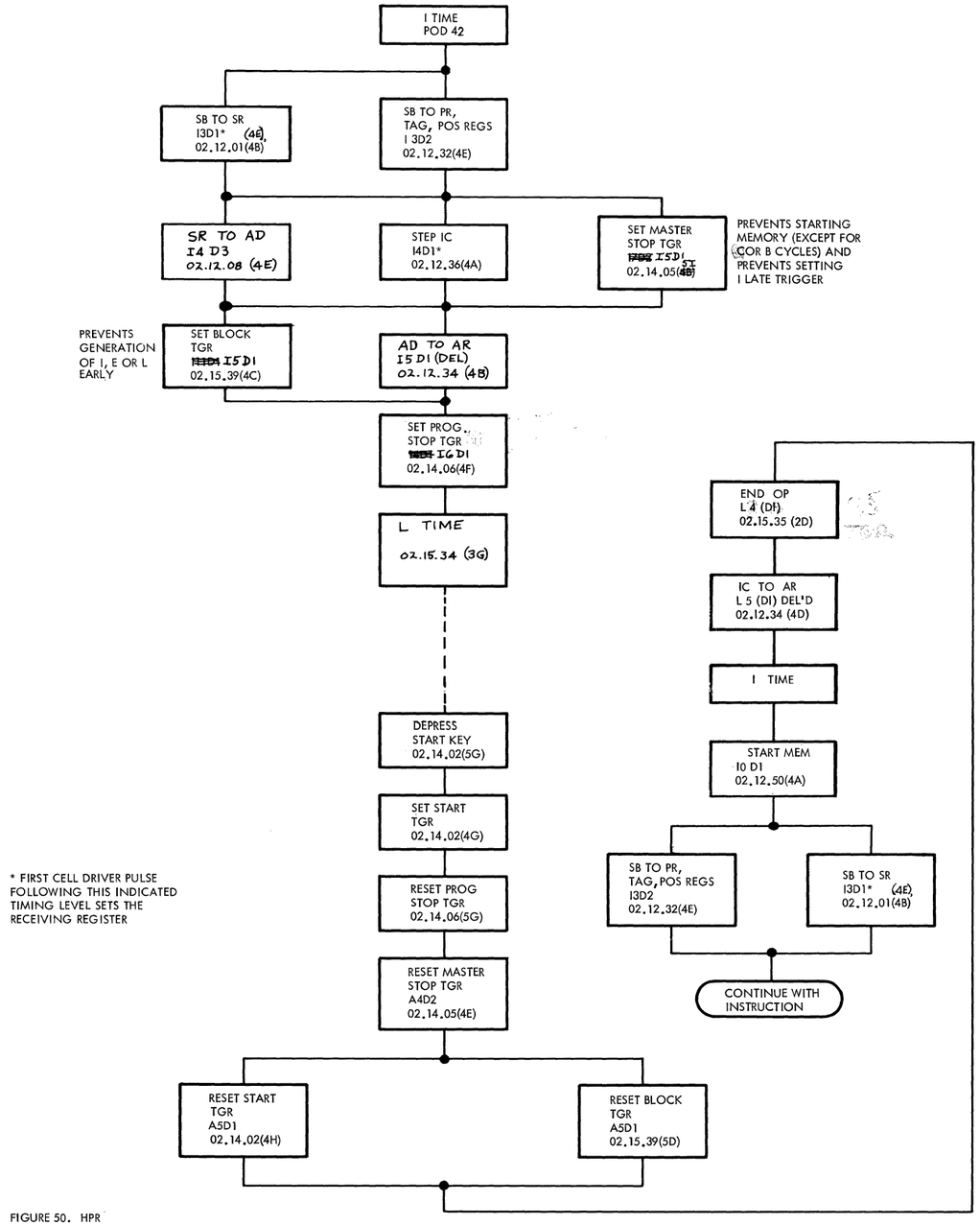
Execute (XEC)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TAI
I	E	00001	+500	000	0	00006	050000000006	000000000000	00		
E	I	00001	+500	000	0	00001	042000000000	042000000000	00		
I	I	00001	+522	000	0	00005	052200000005	042000000000	00		
I	E	00002	+400	000	0	00006	040000000006	042000000000	00		
E	I	00002	+400	000	0	00002	042000000000	104000000000	00		
I	I	00002	+522	000	0	00005	052200000005	104000000000	00		
I	E	00003	+400	000	0	00006	040000000006	104000000000	00		
E	I	00003	+400	000	0	00003	042000000000	146000000000	00		
I	I	00003	+522	000	0	00004	052200000004	146000000000	00		
I	I	00004	+020	000	0	00000	002000000000	146000000000	00		
I	E	00001	+500	000	0	00006	050000000006	146000000000	00		

FIGURE 49. XEC

Halt and Proceed (HPR +0420)
This instruction stops the computer. The instruction counter contains the location of the next instruction. When the start key is pressed, the computer proceeds with the next instruction.



* FIRST CELL DRIVER PULSE FOLLOWING THIS INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

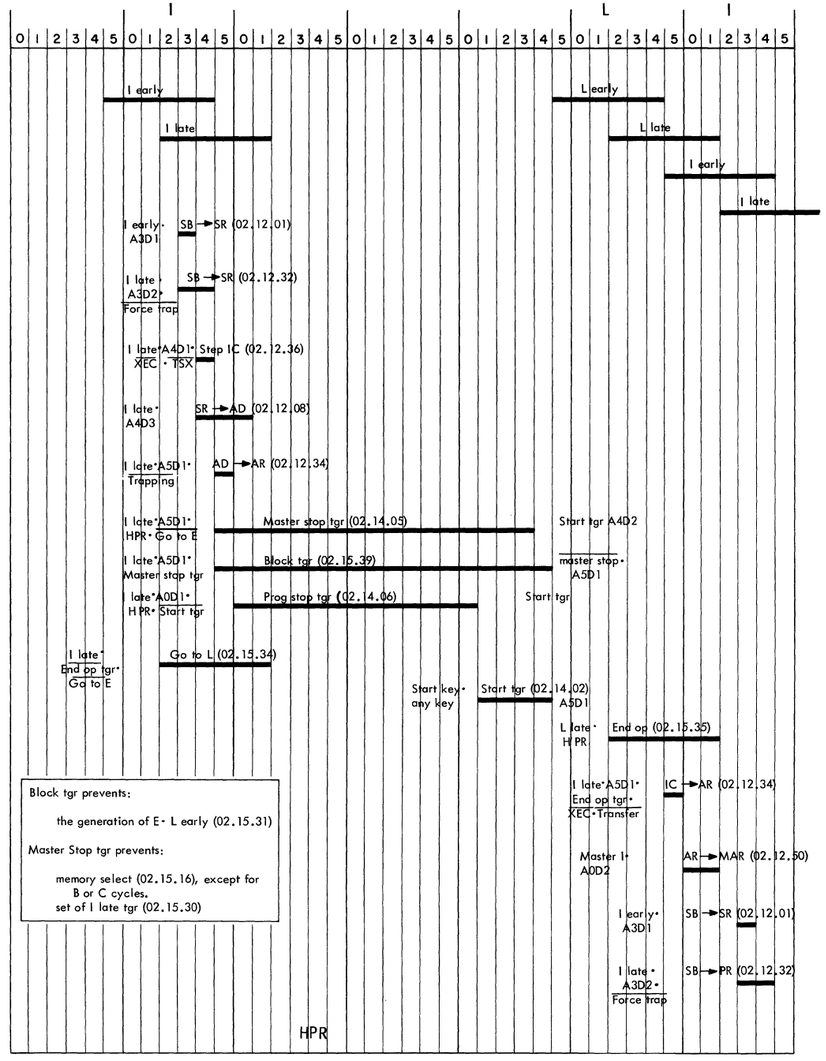


FIGURE 50. HPR

Transmit (TMT -1704)
This instruction moves words from one area of storage to another. Bits 28-35 of the address portion of the instruction word specify the number of words to be transmitted. Prior to executing the Transmit instruction, the accumulator must be set up so that bits 3-17 contain the starting "from" address, and bits 21-35 contain the starting "to" address. As each word is transmitted, the from and to addresses are incremented one, and the word count is decremented one. Words are transmitted until the word count (shift counter) reaches zero.

A maximum of 255 words can be transmitted by a single transmit instruction. At the completion of the transmission, AC 3-17 contains the address of the last word read, plus 1, and AC 21-35 contains the address of the last word stored, plus 1. Another TMT instruction can be given to transmit more words.

*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER

NOTE:
AFTER INITIAL L CYCLE, E CYCLE ARE REQUIRED UNTIL SC = 0.

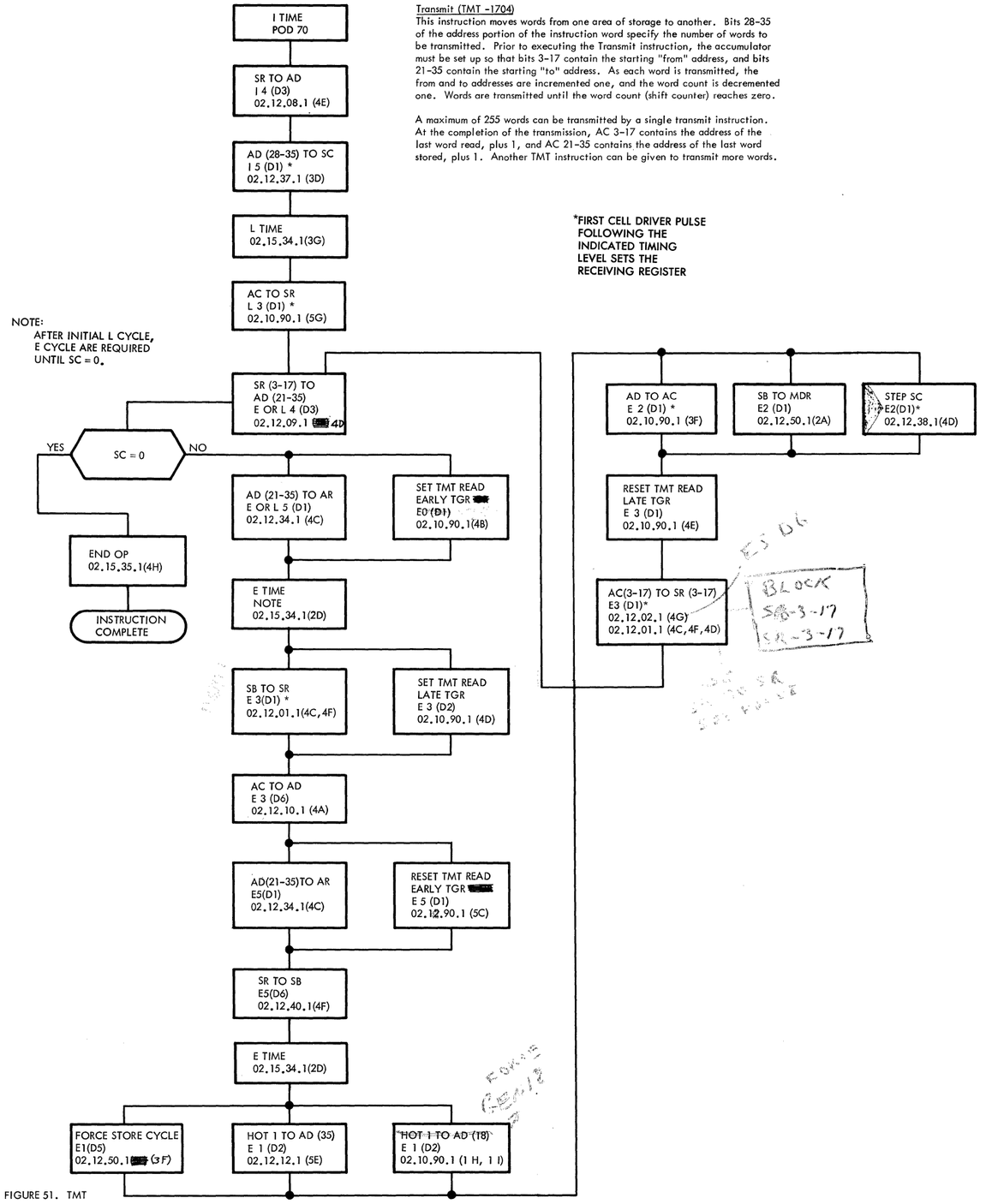
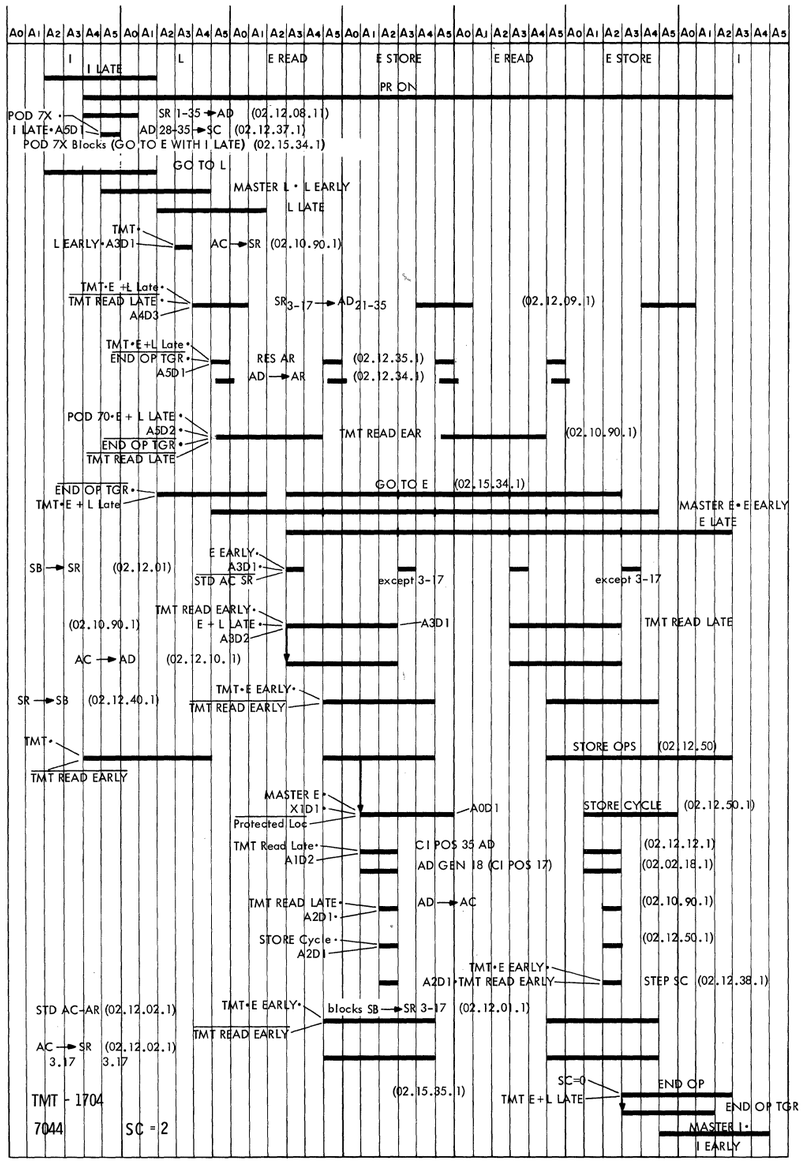
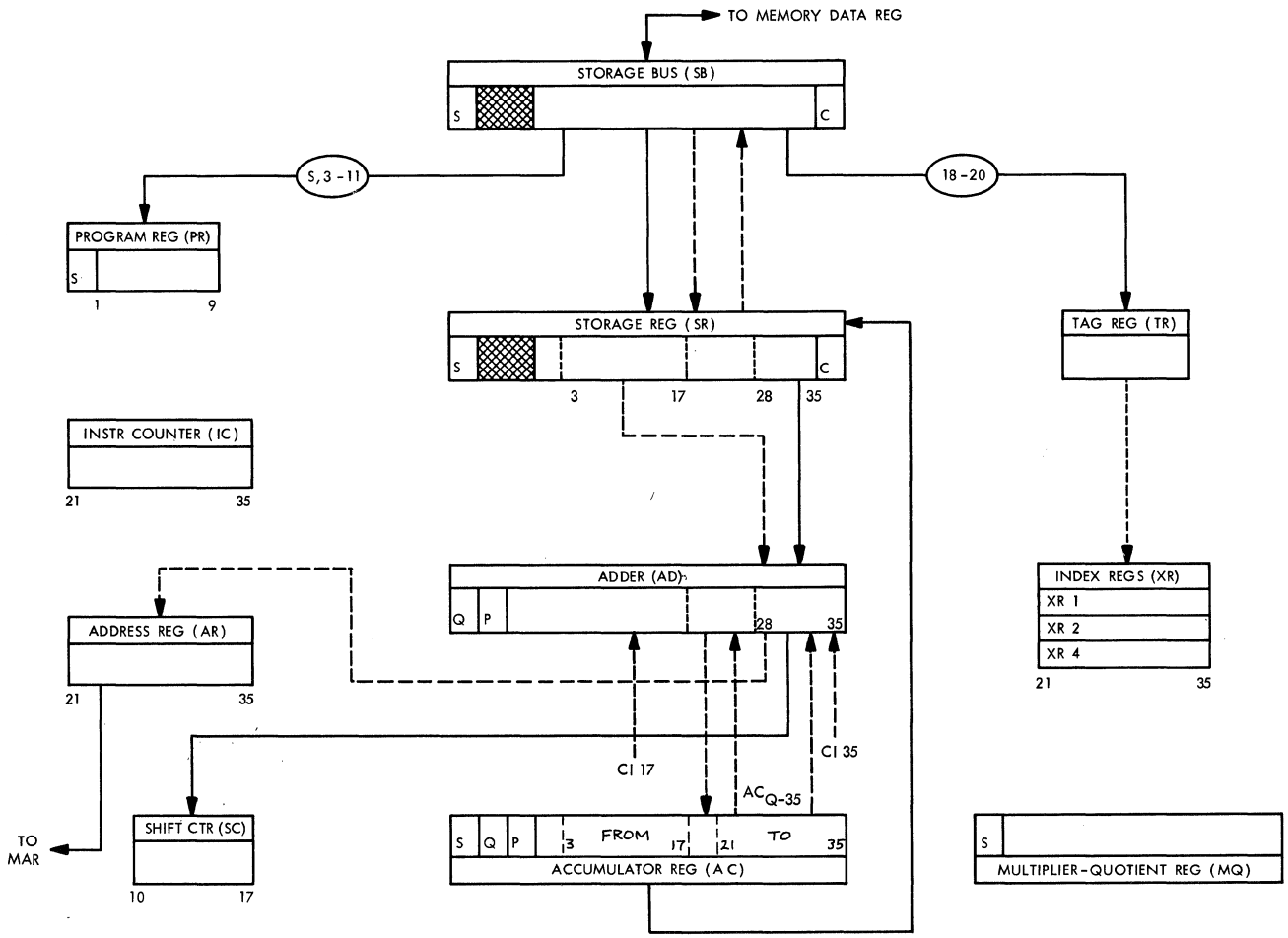


FIGURE 51. TMT





LEGEND

1 CYCLE

E CYCLE

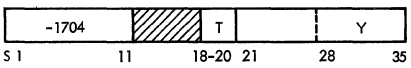
L CYCLE

CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -1704--C TRANSMIT

ALPHA CODE: TMT CYCLES: I, (L) + 2N



SEQUENCE NOTES:

Set Protect Mode (SPM -1160)

Causes the field register to be set to the high-order seven positions of instruction word 21-35, and the count register to be set to instruction word 32-35. Count register position 32 determines the mode of protection (1 for trap on equal, 0 for trap on unequal). Count register positions 33-35 determine the number of high-order positions of the field register that are to be compared with any store address. An attempt to store into a protected area of memory results in a memory protect trap.

If the computer is already in the memory-protect mode when the SPM instruction is given, an instruction trap results, placing the location of the SPM instruction plus 1 in the address part of location 32. Bit 16 is set on (indicating a violation), protect-mode is turned off, and the computer takes its next instruction from location 33.

If SPM is given on a machine that does not have the memory-protect option, a no-operation results and the computer takes its next instruction from the next sequential location.

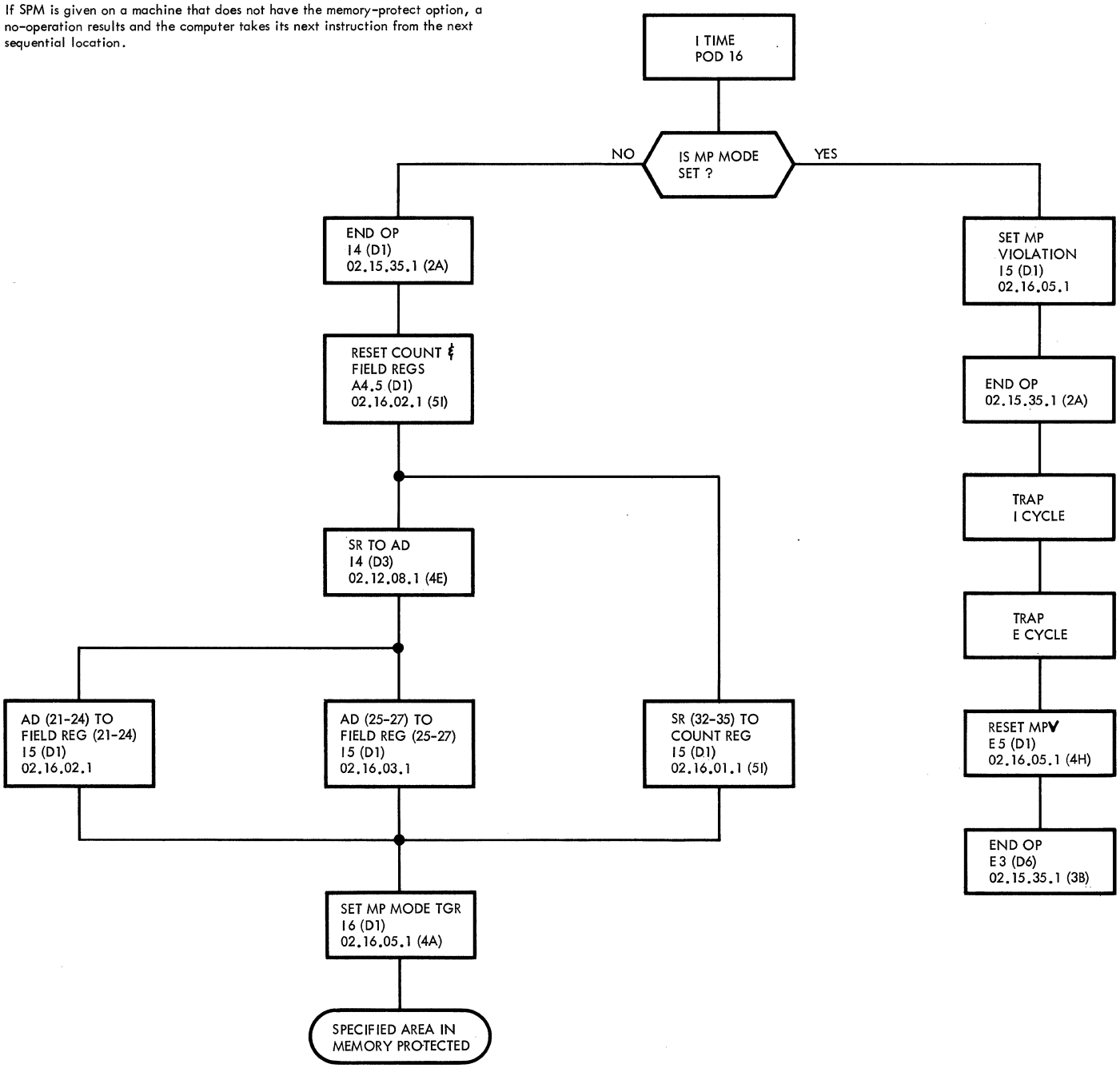
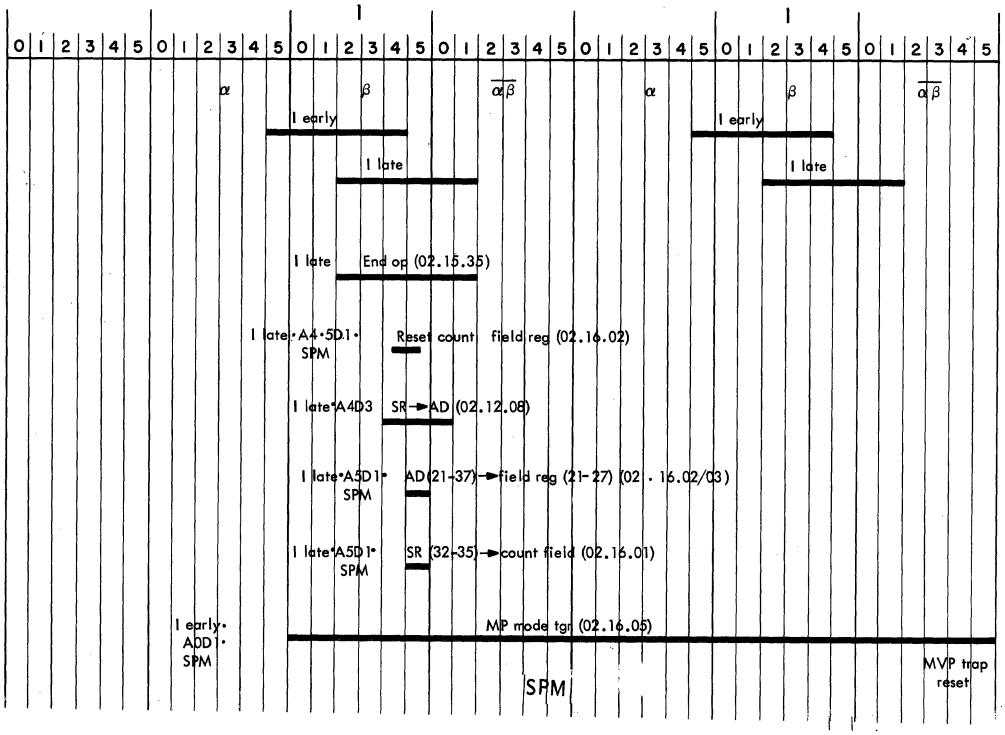


FIGURE 52. SPM



Location Switches	Inst	Tag	Address	Octal Equiv
00100	SPM		00000	516000 000000
00101	TRA		00104	002000 000104
00102				000000 000000
00103	TRA		00106	002000 000106
00104	SPM		00000	516000 000000
00105	HPR			042000 000000
00106	TRA		00100	002000 000100
00032				
00033	TRA		00106	002000 000106

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	MEMORY PROTECT	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	3 OVERFLOW	FP 1	FP 2
I	I	00100	+020	000	0	00100	002000000100															
I	I	00101	-160	000	0	00101	516000000000				0											
I	I	00102	+020	000	0	00104	002000000104				1											
I	I	00105	-160	000	0	00105	516000000000				1											
I	E	00105	000	000	0	00032	042000000000				1											
E	I	00105	000	000	0	00033	000002000105				0											
I	I	00034	+020	000	0	00106	002000000106				0											
I	I	00107	+020	000	0	00100	002000000100				0											

Release Protect Mode (RPM -1004)
If the computer is in memory-protect mode, this instruction turns the memory-protect mode off and traps to location 32 (sets bit 15). If the computer is not in memory-protect mode, this instruction traps to location 32 and sets bit 14. In either case, the computer takes its next instruction from location 33.

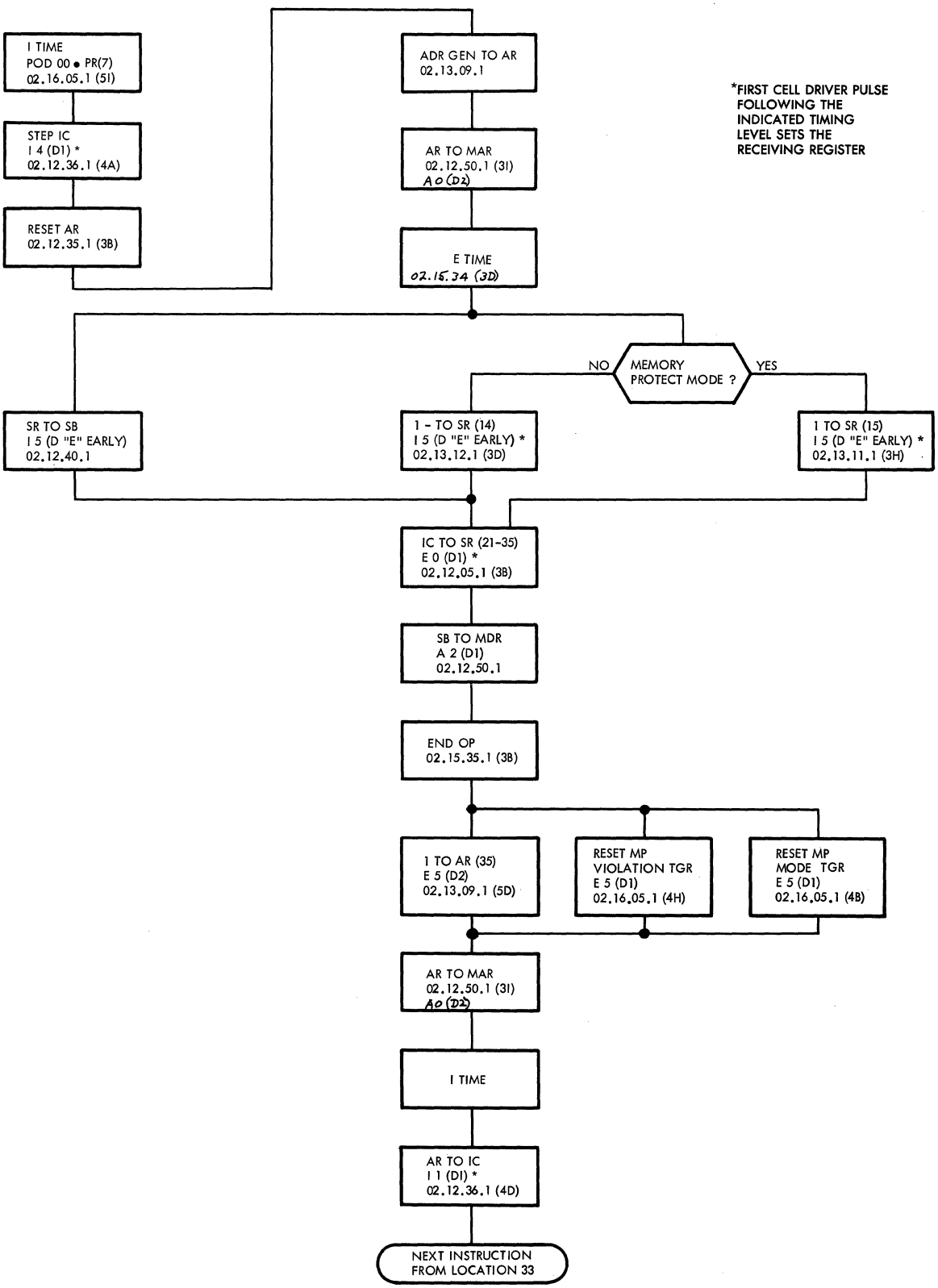
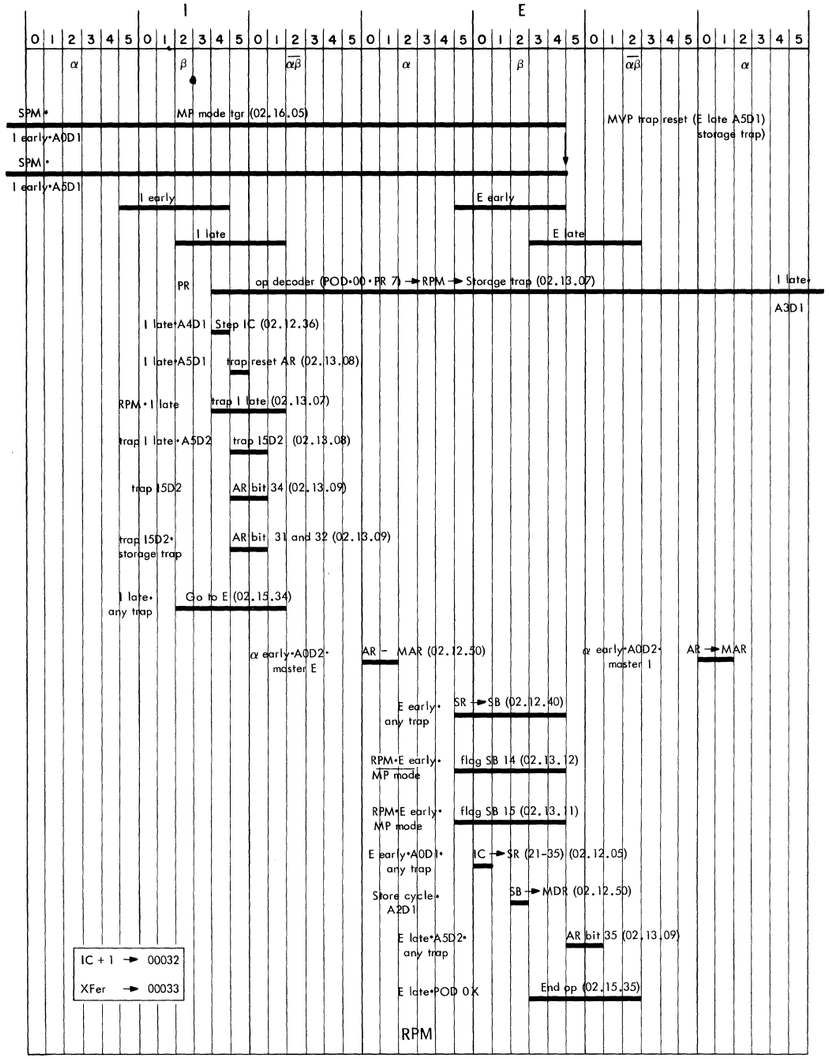


FIGURE 53. RPM



Location Switches	Inst	Tag	Address	Octal Equiv
00000	TRA		00100	002000 000100
00032				
0000	TRA		00104	002000 000104
00100	RPM		00000	500400 000000
00101				
00102				
00103				
00104	SPM		00000	516000 000000
00105	RPM		00000	500400 000000

Release Protect Mode (RPM)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	MEMORY PROTECT	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	I	00100	+020	000	0	00100	002000000100															
I	E	00101	-004	000	0	00032	500400000000															
E	I	00101	-004	000	0	00033	000010000101															
I	I	00034	+020	000	0	00104	002000000104															
I	I	00105	-160	000	0	00105	516000000000															
I	E	00106	-004	000	0	00032	500400000000					1										
E	I	00106	-004	000	0	00033	000004000106					0										
I	I	00034	+020	000	0	00104	002000000104					0										

End of Tape Test, Channel A (ETTA -0760)
This instruction is used to test the status of the end-of-tape trigger in Channel A. If the trigger is on, the computer resets the trigger and takes the next sequential instruction. If the EOT trigger is off, the computer skips the next instruction. The end-of-tape trigger is turned on when a write select, write end of file, or write blank tape causes the end-of-tape marker to be sensed.

An end-of-tape condition on any of the channels 8-E can be tested by executing ETT (-0760) with the proper channel selected.

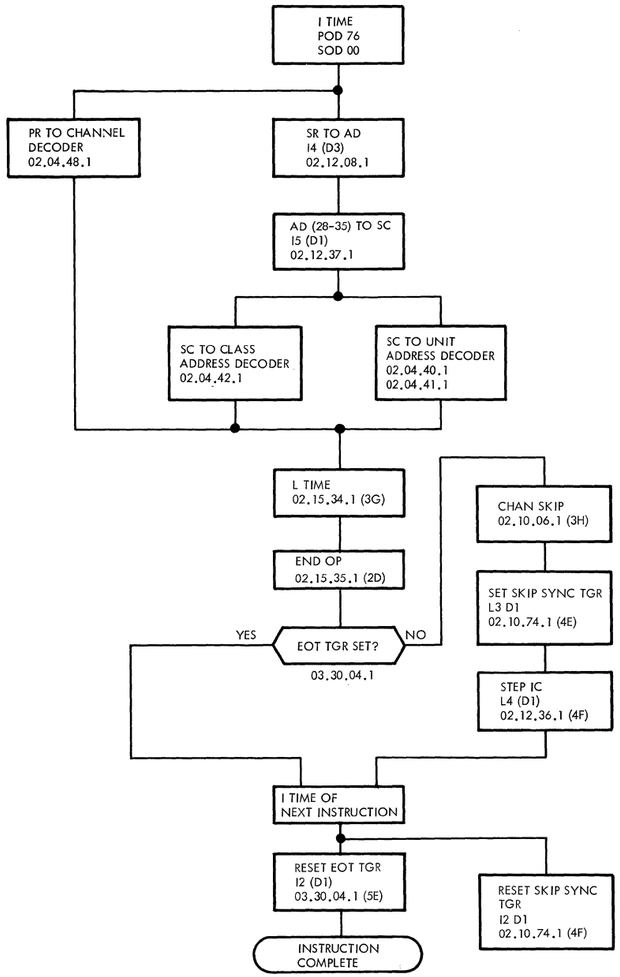
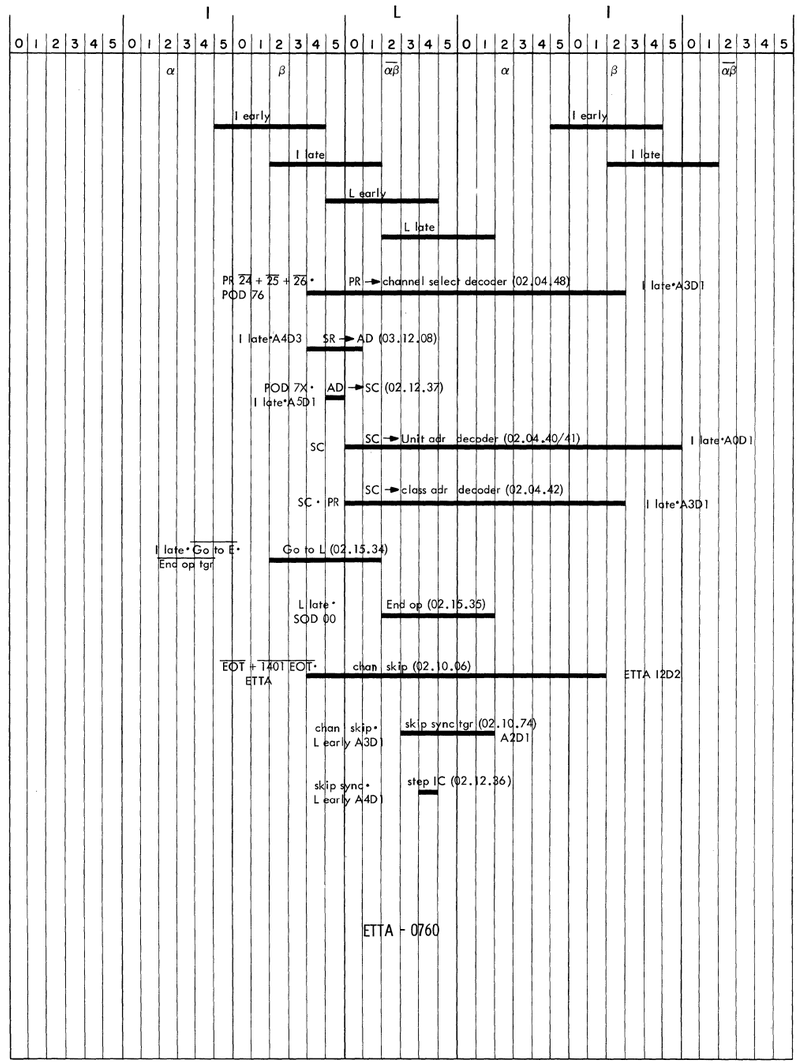
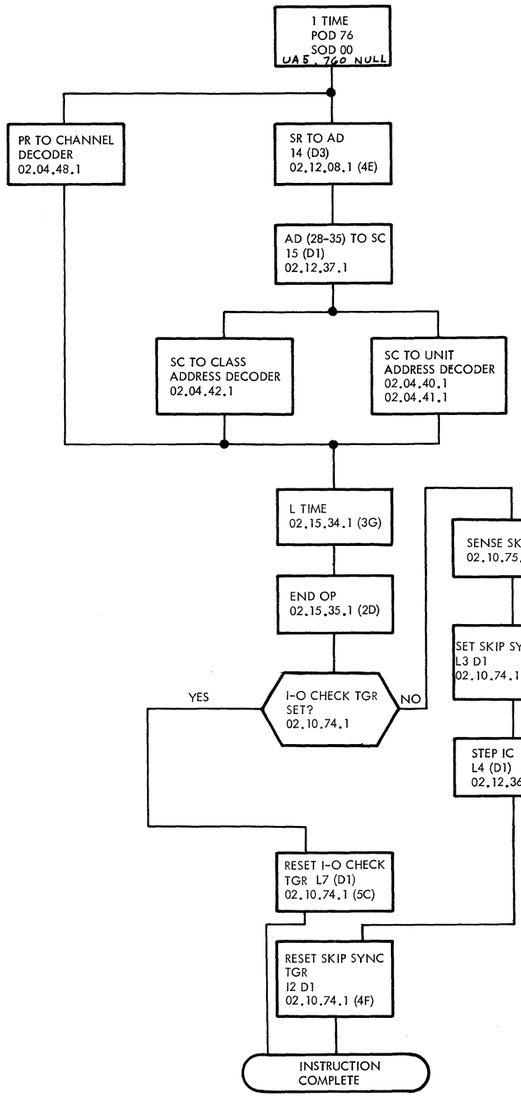


FIGURE 54. ETTA



Input-Output Check Test (IOT +0760 ... 0005)
If the I/O check indicator is on, the indicator is turned off and the computer takes the next sequential instruction. If the indicator is off, the computer skips the next instruction.



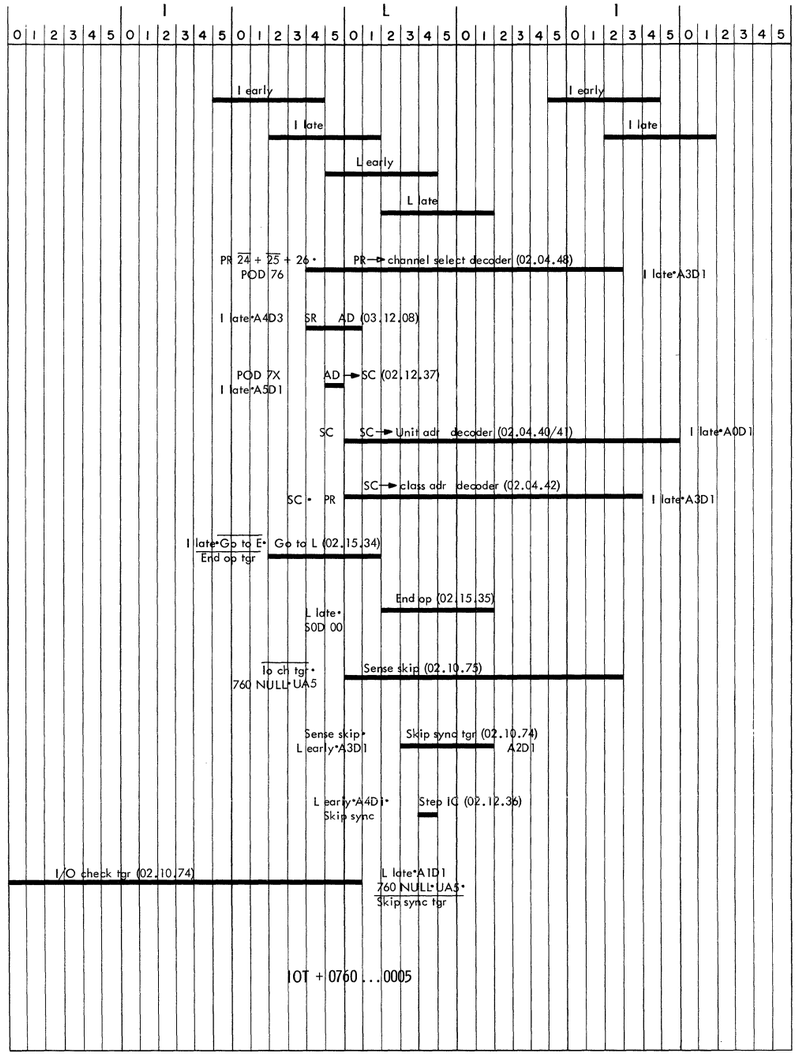


FIGURE 55. IOT

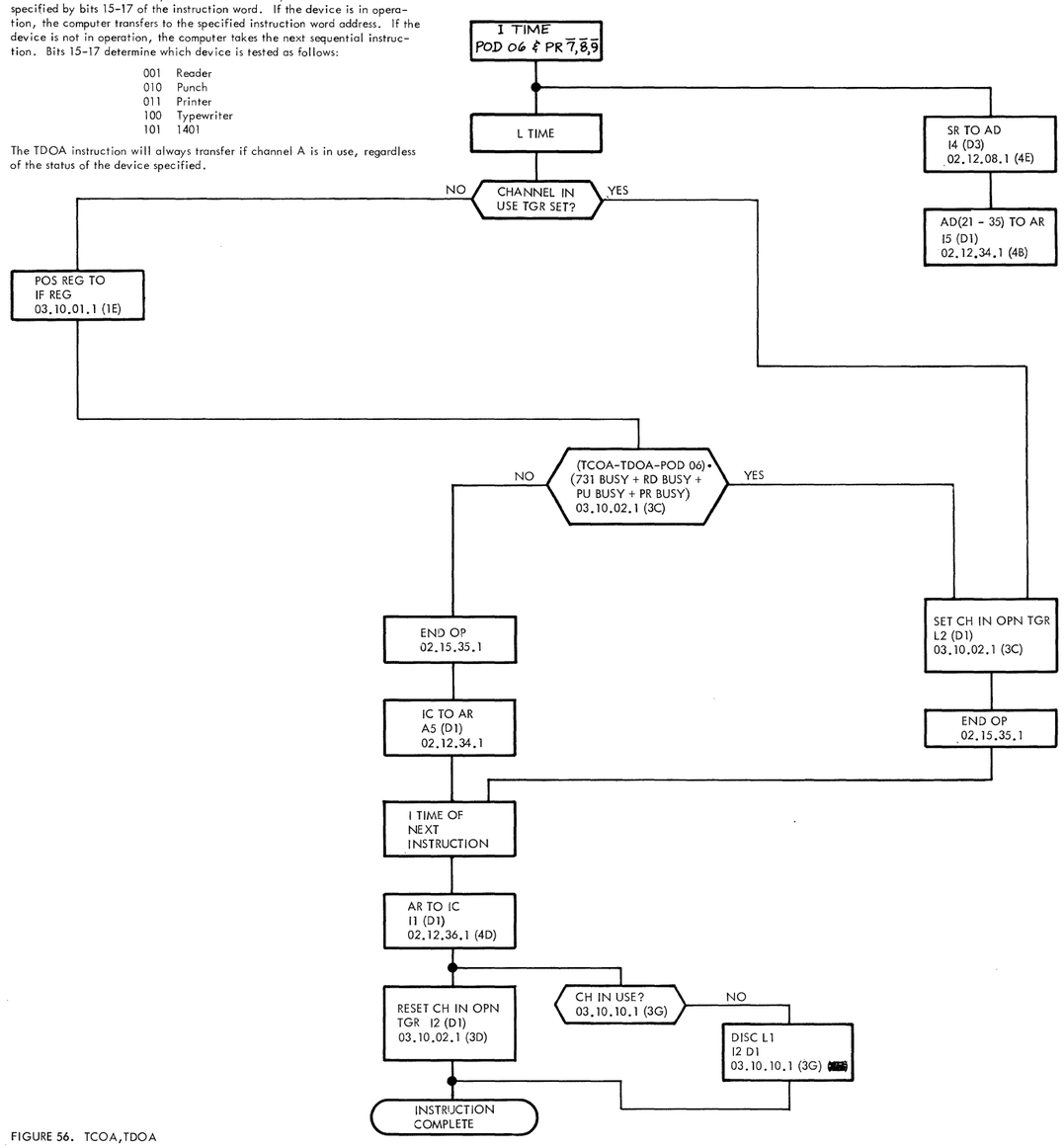
Transfer on Channel in Operation (TCOA +0060)
(TCOB +0061)
(TCOC +0062)
(TCOD +0063)
(TCOE +0064)

If the channel-in-use indicator is on for the specified channel, the computer takes its next instruction from the location specified by the address portion of the instruction word. If the channel-in-use indicator is off, the computer takes the next sequential instruction.

Transfer on Channel A Device in Operation (TDOA -1060)
This instruction tests the busy status of individual I/O devices on channel A specified by bits 15-17 of the instruction word. If the device is in operation, the computer transfers to the specified instruction word address. If the device is not in operation, the computer takes the next sequential instruction. Bits 15-17 determine which device is tested as follows:

001	Reader
010	Punch
011	Printer
100	Typewriter
101	1401

The TDOA instruction will always transfer if channel A is in use, regardless of the status of the device specified.



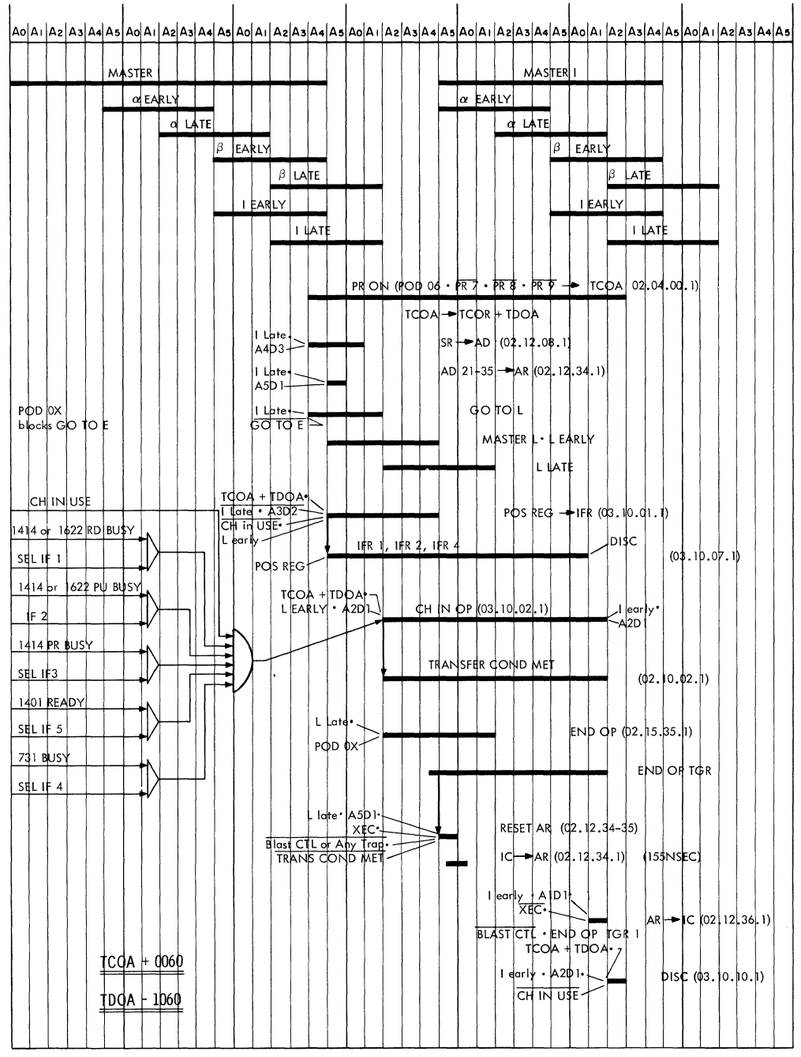


FIGURE 56. TCOA,TDOA

Transfer on Redundancy Check (TRCA +0022)
(TRCB -0022)
(TRCC +0024)
(TRCD -0024)
(TRCE +0026)

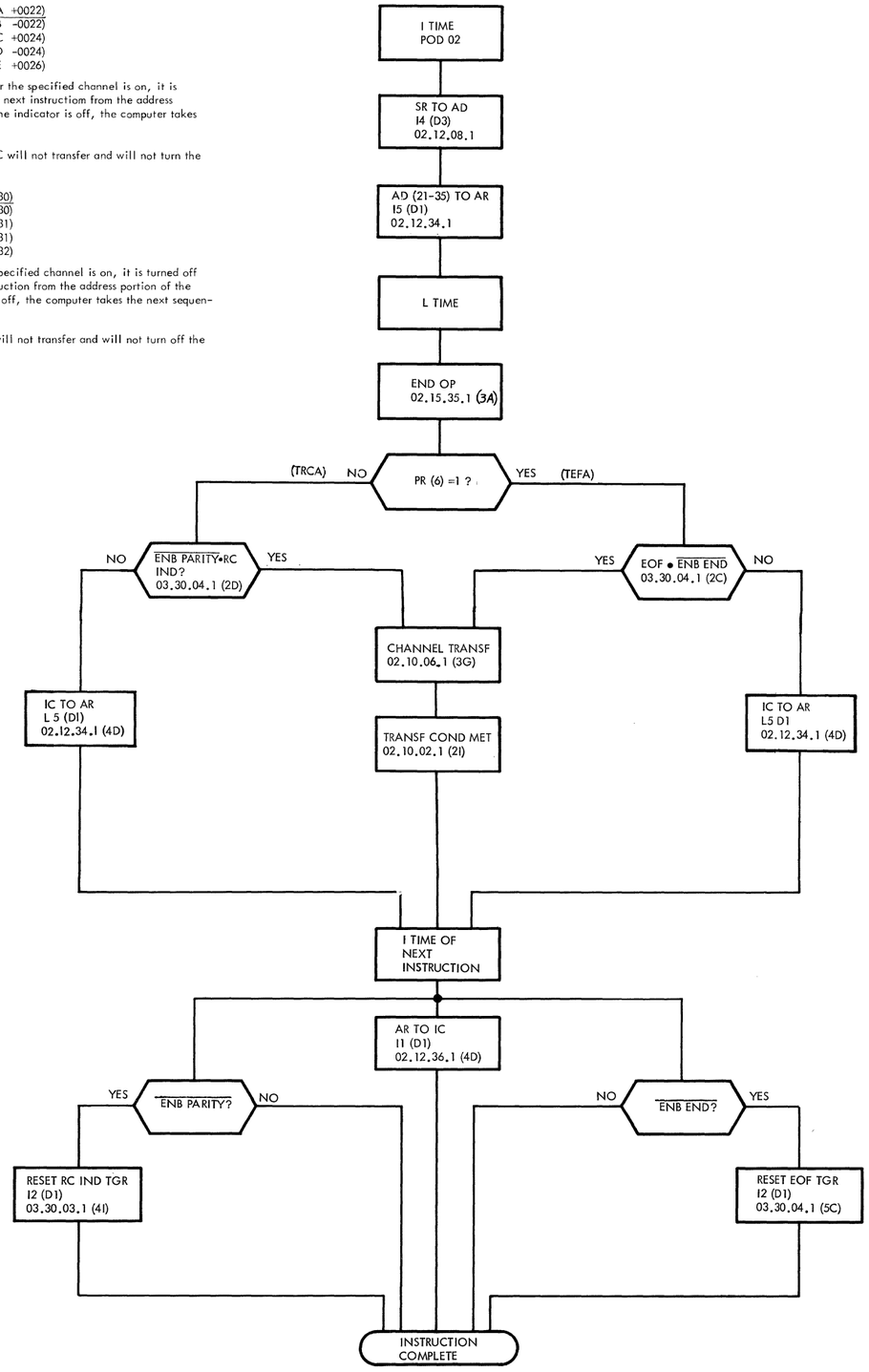
If the redundancy-check indicator for the specified channel is on, it is turned off and the computer takes its next instruction from the address portion of the instruction word. If the indicator is off, the computer takes the next sequential instruction.

If channel parity is enabled, the TRC will not transfer and will not turn the redundancy-check indicator off.

Transfer on End of File (TEFA +0030)
(TEFB -0030)
(TEFC +0031)
(TEFD -0031)
(TEFE +0032)

If the end-of-file indicator for the specified channel is on, it is turned off and the computer takes its next instruction from the address portion of the instruction word. If the indicator is off, the computer takes the next sequential instruction.

If channel end is enabled, the TEF will not transfer and will not turn off the end-of-file indicator.



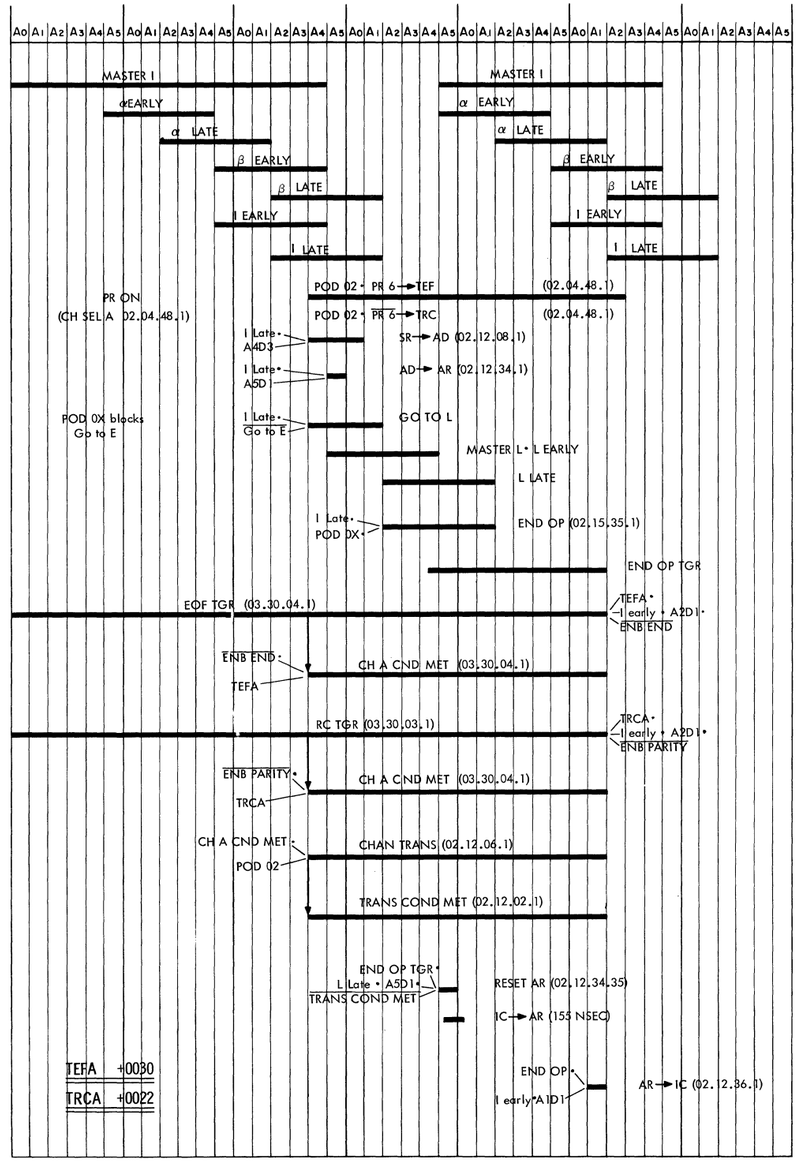
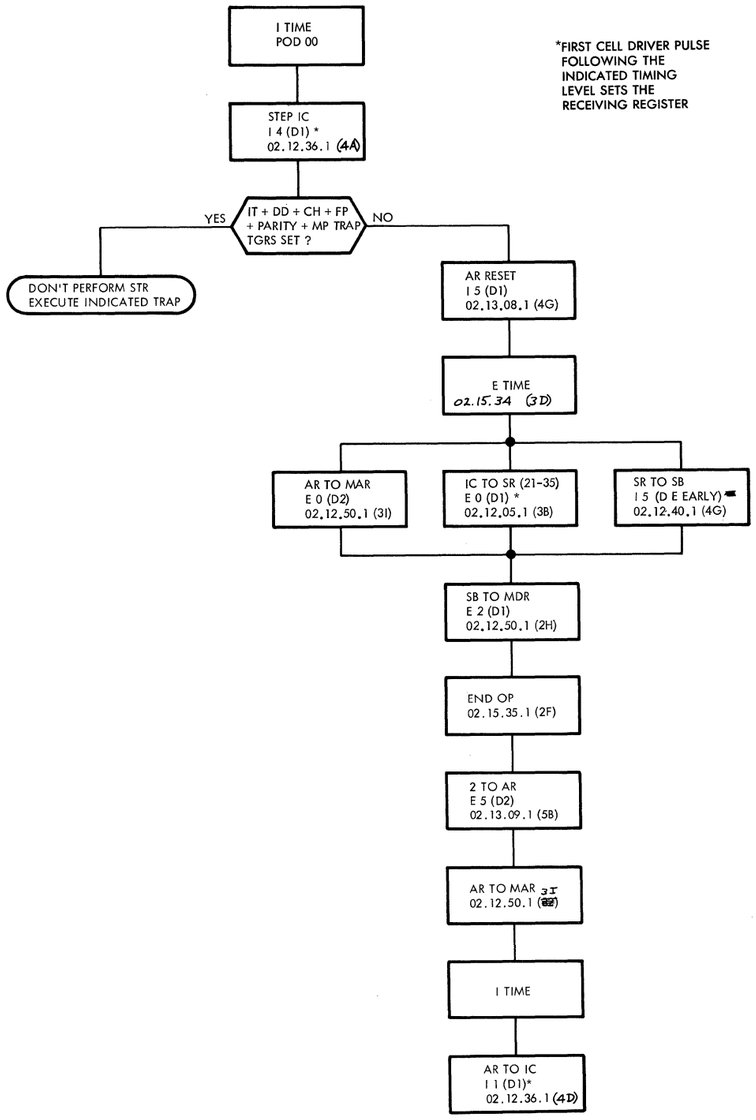


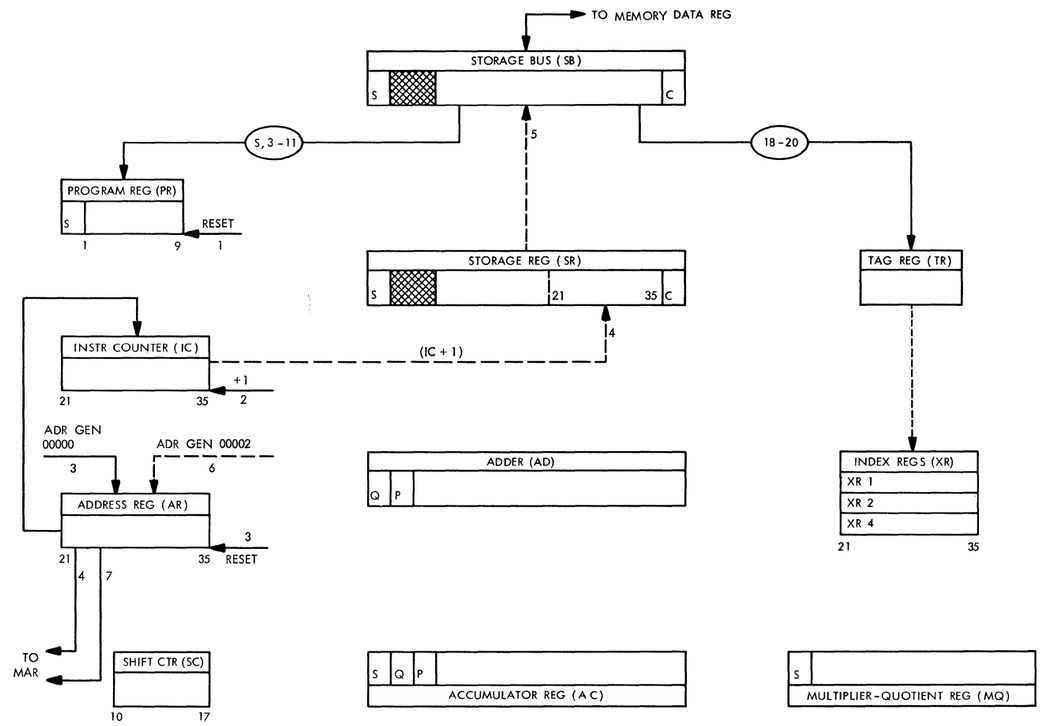
FIGURE 57. TRCA,TEFA

Store Location and Trap (STR -1000)

Execution of this instruction causes trapping to location 00000, where the instruction counter count (location of the STR plus 1) is stored in positions 21-35. The computer then transfers to location 00002. Bits 12-35 of the instruction word are not interpreted by the computer.



*FIRST CELL DRIVER PULSE FOLLOWING THE INDICATED TIMING LEVEL SETS THE RECEIVING REGISTER



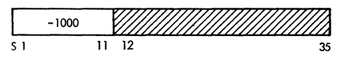
LEGEND

- I CYCLE
- E CYCLE
- L CYCLE
- CONTROL

XFERS INCLUDE ALL BITS CONTAINED IN THE SMALLER OF THE TWO REGISTERS INVOLVED, UNLESS OTHERWISE SPECIFIED.

INST -1000 (+0000) STORE LOCATION AND TRAP
(-0008)

ALPHA CODE: STR CYCLES: I, E



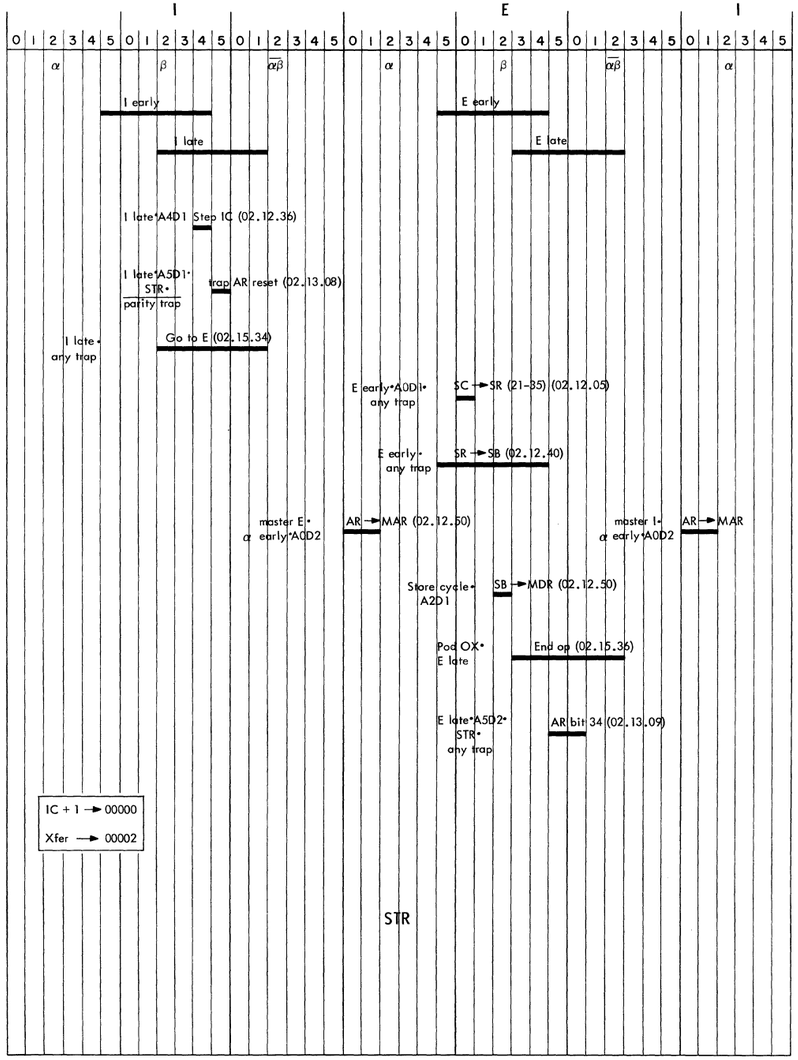
SEQUENCE NOTES:

THE LOCATION OF THE STR INSTRUCTION +1 IS PLACED IN $C(00000)_{21-35}$.

$C(00000)_{S-20}$ ARE CLEARED.

THE COMPUTER TRANSFERS TO LOC 00002.

FIGURE 58. STR



Location Switches	Inst	Tag	Address	Octal Equiv
00000				
00002	TRA		00100	002000 000100
00100	TRA		00103	002000 000103
00101				
00102				
00103	STR		00000	500000 000000

Store Location and Trap (STR)

CONSOLE INDICATORS

CYCLE EXECUTED	CYCLE TIME	INSTRUCTION COUNTER	INSTRUCTION	SHIFT COUNTER	TAG	ADDRESS	STORAGE REGISTER (S, 1-35)	ACCUMULATOR (S, 1-35)	ACCUMULATOR (Q, P)	MQ REGISTER (S, 1-35)	TALLY COUNTER	INDEX REGISTER	POSITION REGISTER	ACCU OVERFLOW	DIVIDE CHECK	Q CARRY	X CARRY	9 CARRY	9 OVERFLOW	FP 1	FP 2
I	I	00100	+020	000	0	00100	002000000100														
I	I	00101	+020	000	0	00103	002000000103														
I	E	00104	-000	000	0	00000	500000000000														
E	I	00104	-000	000	0	00002	000000000104														
I	I	00003	+020	000	0	00100	002000000100														

Transfer and Restore Traps (TRT -1164)
Turns on the trap-control trigger. The computer transfers to the location specified by the address portion of the instruction word.

Transfer and Restore Parity and Traps (TRP -1165)
Turns on the trap-control and parity-mode triggers. The computer transfers to the location specified by the address portion of the instruction word.

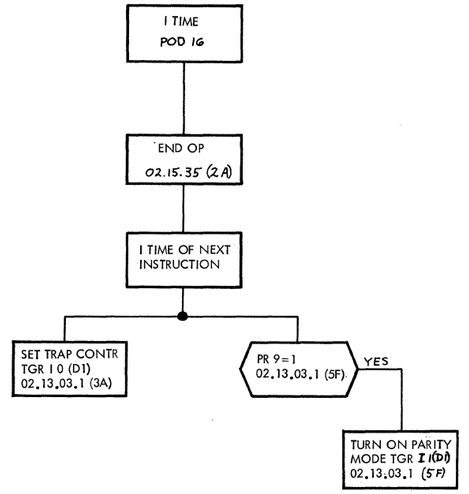
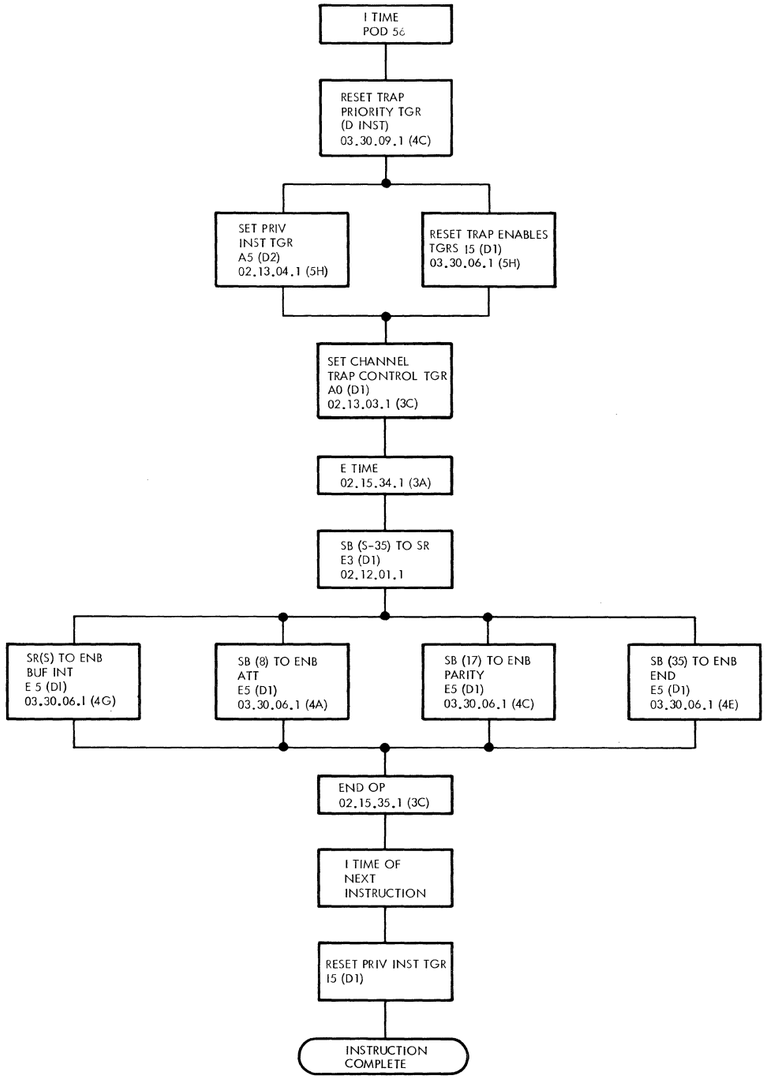


FIGURE 59. TRT,TRP

Enable from Y (ENB +0564)
The contents of Y (location specified by address portion of instruction word) are used to set the channel mask bits to 1 or 0. Execution of each enable instruction cancels the effect of previous enable instructions. The enable instruction turns on channel trap control.



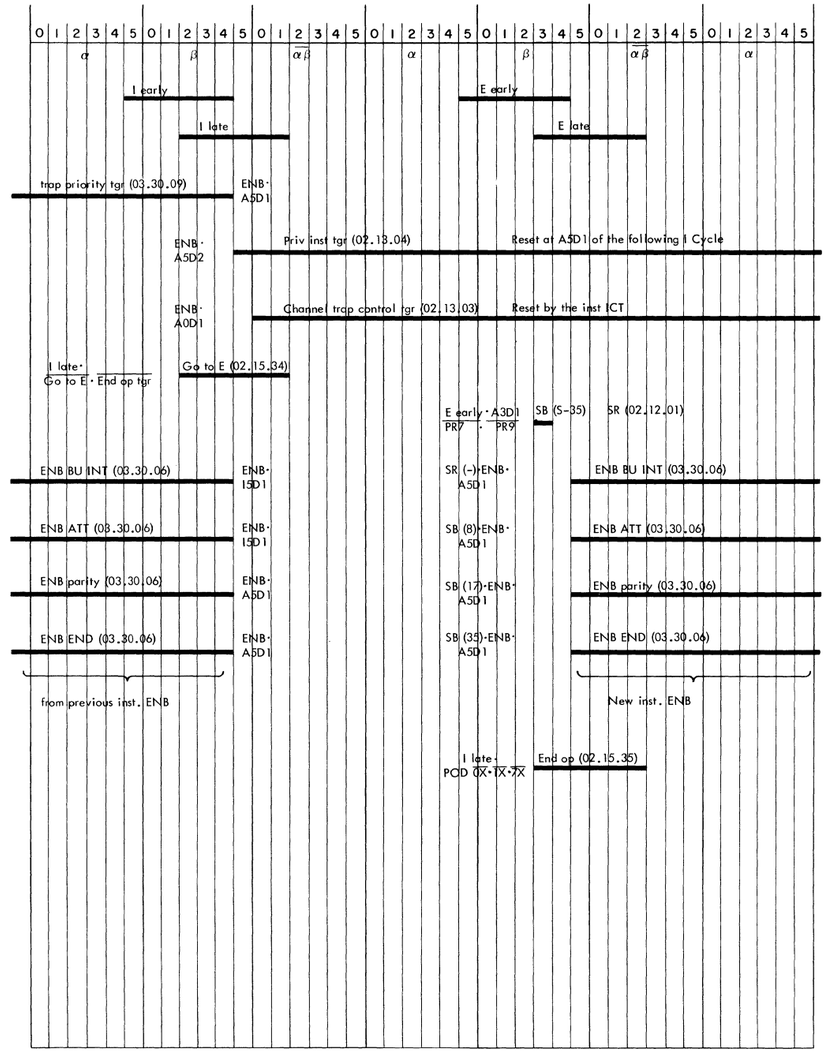
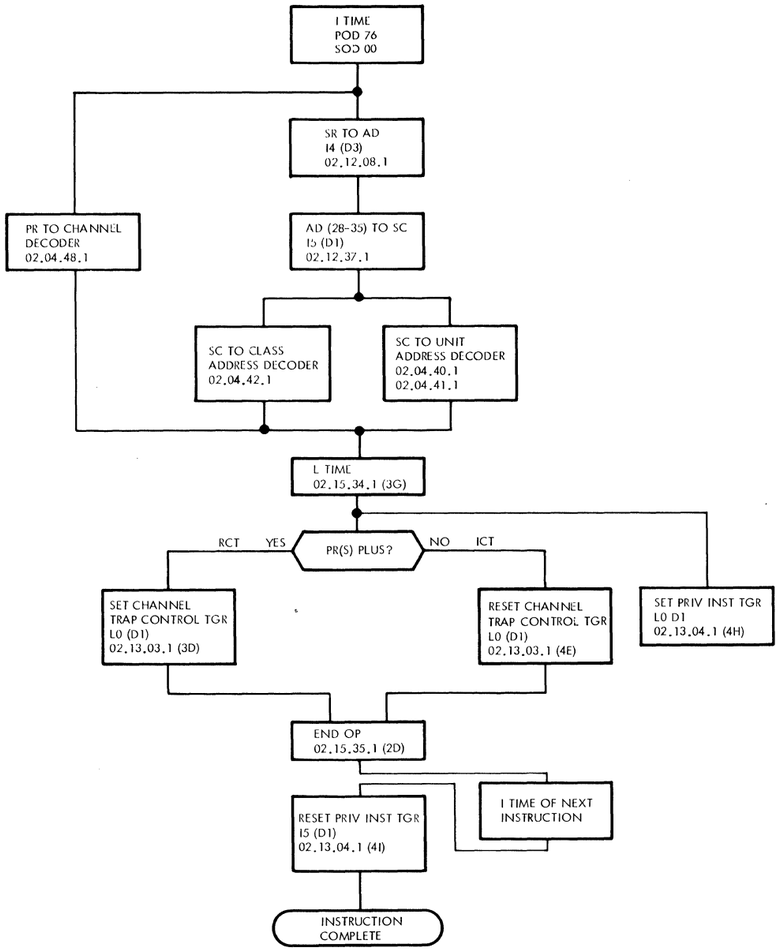


FIGURE 60. ENB

Restore Channel Traps (RCT 1760 ... 0014)
Turns on channel trap control. This allows traps to occur as specified by the previous enable instruction. It cancels the inhibiting effect of an executed trap or an ICT instruction.

Inhibit Channel traps (ICT 1760 ... 0014)
Turns off channel trap control. This inhibits all channel traps and direct data traps until an RCT instruction or a new ENB instruction is given.



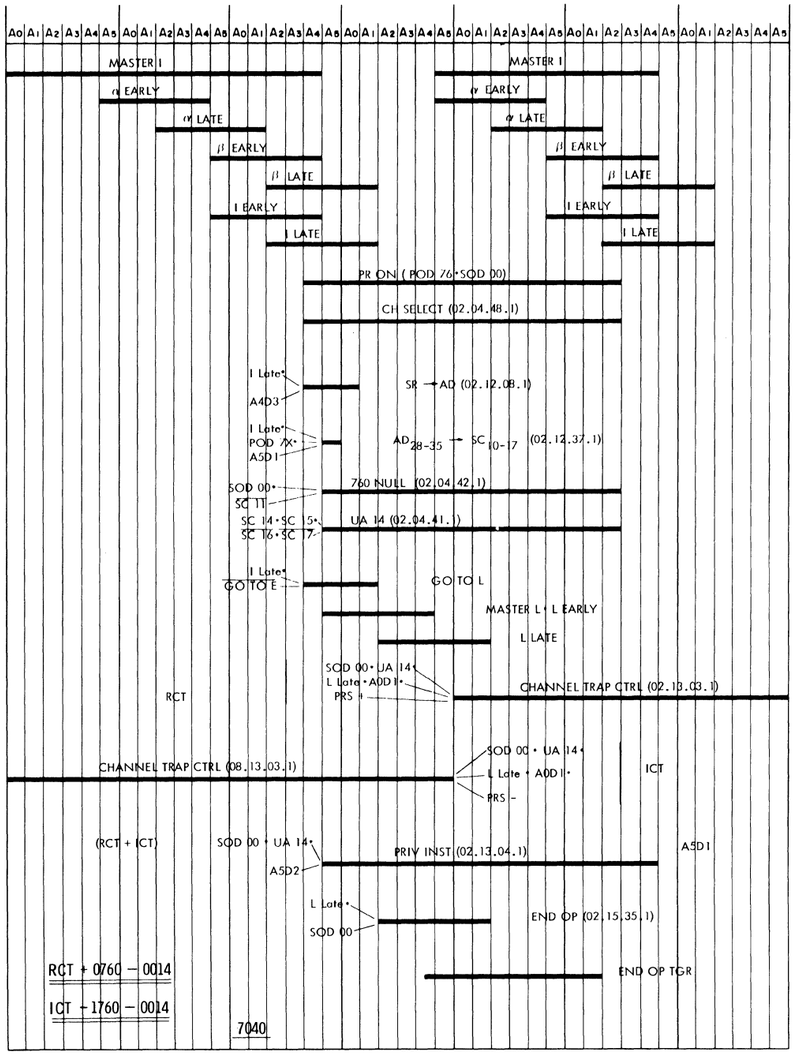


FIGURE 61. RCT, ICT

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Your comments regarding this manual will help Product Publications increase the value of future reference manuals. Please consider the following questions and mail this form.*

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2. Have the programs and their associated indicator charts helped you fix any troubles?

3. Have the timing charts helped you fix any troubles?

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