D99-3705E-09
D99-3705E-08

IBM MAINTENANCE DIAGNOSTIC PROGRAM

IBM 3705 COMMUNICATIONS CONTROLLER

INTERNAL FUNCTIONAL TEST SYSTEM INDEXES

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IBM/TECHNICAL NEWSLETTER D99-3705E-09

IBM MAINTENENCE DIAGNOSTIC PROGRAM
IBM 3705 COMMUNICATIONS CONTROLLER
INTERNAL FUNCTIONAL TEST SYMPTOM INDEXES

This TECHNICAL NEWSLETTER provides complete replacement for IBM 3705 Communications Controller Internal Functional Test Symptom Indexes, DOC. NO. DCL-3705E-08, previously released with OLT DIAGNOSTIC RELEASE 12.4.

RELEASE 13.0.

This change:
Corrects the running footer titles for CHAPTERS 1 and 2 of D99-3705E.

Adds description for new Type 4 Channel Adapter routine (Rtn 55), in Chapter 8.

Adds comments for Rtn X7A8 for manual intervention stops.

Adds second card call (A3D2) to Rtn X607, error stop 0X01.

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PREFACE

This manual contains the IBM 3705 Communications Controller Internal Functional tests symptom indexes. This manual should be used with its companion manual IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Loader, Diagnostic Control Module, Initial Test, and Panel Line Test, D99-3705D. The companion manual provides guidance in using the symptom indexes. The symptom refers to a 'suspected' card or cards for most error stops; these suspected cards have a high enough probability of causing the error to be singled out. However, the indicated card may not be the actual cause of the error. The suspected card serves only as a guide to assist in getting into the failing area and not as a sure fix for errors.

The material in this manual was previously published in IBM Maintenance Diagnostic Program 3705 Communications Controller On Line Tests and Internal Functional Tests, D99-3705A-05, which has been replaced by:

IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Channel Adapter And Wrap All Lines On-Line Tests, D99-3705C.

IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Loader, Diagnostic Control Module, Initial Test, and Panel Line Test, D99-3705D.

IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Symptom Indexes, D99-3705E.

The symptom indexes are arranged in IFT number order throughout this manual.

Companion Manuals that should be referred to are:

IBM 3705 Communications Controller Theory Maintenance Manual, SY27-0107.

IBM Maintenance Diagnostic Program IBM 3705 Communications Controller Internal Functional Test Loader, Diagnostic Control Module, Initial Test, and Panel Line Test, D99-3705D.

SUMMARY OF AMMENDMENTS FOR D99-3705E-01

Chapters 7.0 through 7.9 have been changed to include additional cards in the 'Suspected Card' column. Error stop 0X70 has been added to routine X718 in chapter 7.0.

Chapter 5.2 has been changed to include a manual intervention wrap routine X6P2. This routine provides for line set wrapping and modem wrapping with or without a wrap block. (Modem wrap cannot be done without a wrap block.)

Miscellaneous corrections have been made throughout this manual.

SUMMARY OF AMMENDMENTS FOR D99-3705E-02

This version of the manual was released as a DCL. Chapter 8 was changed to include support for multiple type 4 channel adapters (4).

SUMMARY OF AMMENDMENTS FOR D99-3705E-03

Chapter 1 was changed to include support for RPQ 858911.

Chapter 3 was changed to incorporate changes to routine 2.

Chapter 6 was changed to incorporate error stops for several routines that were inadvertently left out of the manual. Support for line sets 1T and 1U is included in this version.

Chapter 7 was changed to incorporate error stops for RPQs EH4100 and 858912. Support for line sets 1T and 1U is included in this version.

SUMMARY OF AMENDMENTS FOR D99-3705E-05

This edition incorporates DCL-3705E-04 and includes changes to support models J,K,L of the 3705.

Support for several RPQ's has been added.

A new error stop has been added to Chapter 4.

Support for line sets 1w and 1z is included in this version.

SUMMARY OF AMENDMENTS FOR D99-3705E-06

Chapters 6 and 7 have been changed to incorporate changes for the Type 3 High Speed Communication Scanner and the X.21 World Trade Line Interfaces. The X.21 support includes 2 new manual intervention routines X6F4 and X7B7.

SUMMARY OF AMENDMENTS FOR DCL-3705E-07

Chapter 7 has been changed to include symptom indexes for new manual intervention routines X7F1 - X7F3 (ICW Tests) and routines X7F4 - X7F6 (PDF Array Tests). In addition, section 7.1 has been changed from level 05 to level 06 which is the correct level.

Chapter 8 has been changed to include symptom indexes for new Type 4 Channel Adapter manual intervention routines X958 - X95C which enhance the diagnostic ability to isolate intermittent EBM failures. Routine X938 symptom index was changed and routine X939 symptom index was added to reflect changes in the EBM IFT's.

SUMMARY OF AMENDMENTS FOR DCL-3705E-08

Manual Intervention routine X6F6 added for RPQ S30254 on Type 2 scanner.

Comments added to Type 3 scanner IFT routine A8.

Comments reworded in Type 4 Channel adapter IFT routines 4C and 4E.

SUMMARY OF AMENDMENTS FOR D99-3705E-09

Routine 55 added to provide an inbound data address test to an odd address in Type 4 channel adapter tests.

Added card call for 'A3D2' in Type 2 Scanner Routine 7 (X607), ERROR CODE 0X01.

CHAPTERS 1 and 2 of D99-3705E had footer labels in error and are corrected in this release.

Comment added for manual intervention stops in type 3 scanner IFT routine A8.

Chapter 6.2 updated to correct column header alignment.

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CHAPTER 1.0: CENTRAL CONTROL UNIT IPT SYMPTOM INDEX

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	PETEM PAGE	COMMENTS
1102		If an error occurs in this routine, check bit 0.5 in Reg. x'79'. If: (a) the 900 nanosecond ccu oscillator is installed and bit 0.5 if off or, (b) the 1.0 microsecond ccu oscillator is installed and bit 0.5 is on, then hardware bit 0.5 is in error. Correct this fault and rerun the test. Otherwise, continue as specified in the error stops.						
	0X01	The interval timer level 3 interrupt should occur every 100 millseconds. This routine test for an accuracy of plus or minus three percent. Did L3 timer irpt occur prior to 97 ms.	The Timer L3 irpt occurred in less than 97 ms.	A-B3L2 A-B3J5	00FF	CP007 CC007	6-090	Reg X'15' indicates percent of error. If Register X'15' equals X'0004', the error is four percent which means the timer irpt occurred at 96 ms.
	0X02	Did L3 timer irpt occur after 103 ms.	The timer L3 irpt occurred later than 103ms.	A-B3L2 A-B3J5	00FF	CP007 CC007	6-090	Reg. X'15' contains per cent of error. X'0004' indicates 4 percent error. the interrupt occurred at 104ms.
	0X03	Default test - If an interrupt does not occur within 110 ms this routine will halt.	A timer L3 irpt did not occur within 110 ms.	A-B3L2 A-B3J5	N/A	CP007 CC007	6-090	Standard DCM display does not apply.
1103	0X01	Memory size test. Input X'70' is is compared with the 'BSM count' contained in the Configuration Data Set to verify that the two agree.	Input X'70' and CDS BSM count did not compare	A-B4E2 If CDS count is correct	N/A	CM002	4-070 6-770	Reg X'14' = CDS BSM Count Reg X'15' = Input X'70' converted into BSM Count Reg X'16' = Input X'70'
1104	0X01	Z bus parity checker Byte X, 0, and 1 bit 7 are complemented to forced bad parity. The CCU check register is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The actual CCU check register data is in error. The Z bus parity checked failed to detect bad parity. CCU CHK Reg is input X'7D'	See Note 5 A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See note 1
	0X02	Did the force error function produce the correct data	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001 CQ005	6-050	
1105	0X01	Z bus parity checker Byte X, 0, and 1 bit 6 are complemented to force bad parity. The CCU check register is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The actual CCU check register data is in error	See Note 5 A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001 CQ005	6-050	

POUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FRAME PAGE	FETCH PAGE	COMMENTS
1106	0X01	Σ bus parity checker Byte X, 0, and 1, bit 5 are complemented to force bad parity. The CCU check register is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The actual CCU check register data is in error.	See Note 5 A-B3N2 A-B3G2	FFFFF	CK003 CQ005	6-050	See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001-2 CQ005		
1107	0X01	Σ bus parity checker Byte X, 0, and 1, bit 4 are complemented to force bad parity. The CCU check register is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The actual CCU check register data is in error.	See Note 5 A-B3N2 A-B3G2	FFFF	CK003-7 CQ005		See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001 CQ005	6-050	
1108	0X01	Σ bus parity checker Byte 0 and 1 bit 3 are complemented to force bad parity. The CCU check register is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The actual CCU check register data is in error.	See Note 5 A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001 CQ005	6-050	
1109	0X01	Σ bus parity checker Byte 0 and 1 bit 2 are complemented to force bad parity. The CCU check register is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The actual CCU check register data is in error.	See Note 5 A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001 CQ005		
110A		Σ bus parity checker Byte 0 and 1 bit 1 are complemented to force bad parity.						
	0X01	The CCU check register is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The actual CCU check register data is in error.	See Note 5 A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001 CQ005	6-050	
110B		Σ bus parity checker Byte 0 and 1 bit 0 are complemented to force bad parity.						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X01	The CCU check register is tested for expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The actual CCU check register data is in error.	See Note 5 A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-050	See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001 CQ005	6-050	
110C		'A' register parity checker Output X'78' (force CCU checks) with mask X'0020' is used to force bad parity.						
	0X01	The CCU register is tested for the expected data. Routine makes 256 passes starting with data 00000 using an update value of X'10101'	The 'A' register parity checker failed to detect bad parity.	See Note 5 A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-920	See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	3FFFF	CK001 CQ005	6-920	
110D	0X01	'B' register parity checker Output X'78' with mask X'0040' is used to force bad parity. The CCU check register is tested for the expected data.	The 'B' register parity checker failed to detect bad parity.	See Note 5 A-B3N2 A-B3G2	FFFF	CK003 CQ005	6-920	See note 1
	0X02	Did the force error function produce the correct data.	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2	FFFFF	CK001 CQ005	6-920	
110E		SDR register parity checker test. Output X'78', force CCU checks, with data X'0040' is used in conjunction with a output instruction to force SDF errors. The output instruction that forces the error is Reg X'15' output to X'1A'. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.						
	0X01	The CCU Check Register is tested for the expected error bits.	The actual CCU Check Register data is in error.	See Note 6 A-B3N2 A-B3S2	FFFF	CK001 CU013 CU013	6-920	Register X'16' will contain the test data that was used to output to Reg X'1A'.
110F		Indata parity checker test. Output X'78', force CCU Checks, with data X'0010' is used in conjunction with an input instruction to force Indata Parity Errors. Routine makes 256 passes starting with data 00000 using an update value of X'10101'.						
	0X01	The CCU Check Register is tested for the expected error bits.	The actual CCU Check Register data is in error.	A-B3S2 A-B3N2	FFFF	CK001 CU013	6-920	Register X'16' will contain the test data that was in Reg X'1A' when the input from X'1A' was executed.
1110	0X01	SAR register parity checker test. Output X'78' (Force	The SAR register parity checker failed to detect bad parity.	See Note 7 A-B3N2	FFFF	CK003 DP993	6-920	See note 1

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMP PAGE	COMMENTS
		CCU Checks) with mask X'0040' is used to force bad parity. The CCU Check Register is tested for the expected error bits.		A-B4G2 A-B4H2		DR993		
	0X02	Did the force error function produce the correct data	The actual data produced by the force error function did not compare with the expected.	A-B3S2 A-B3G2 A-B3H2	FFFF	CK001 DP993 DR993	6-920	
1113	0X01	Level 4 interrupted by Level 3 via a PCI L3 irpt. irpt reg grp 2 (X'7F') is tested for a PCI L3 bit.	The PCI L3 interrupt failed to occur.	A-B3G2 A-B3M2 A-B3J2	FDFB	CQ005 CD001 CU015 CP002 CA003	6-090 6-860	
	0X02	Prior to forcing the L3 irpt, the L4 CZ latches are set to CZ = 10 on return to L4 the CZ latches are tested to ensure that L3 did not alter the preset L4 CZ ltch.	The level 4 CZ latches were affected by the PCI L3 irpt.	A-B3G2	0003	CZXXX	6-090	
1114	0X01	Level 4 is interrupted by Level 3 via a PCI L3 irpt. irpt reg grp 2 (X'7F') is tested for a PCI L4 bit.	The PCI L3 irpt failed to occur	A-B3G2 A-B3M2 A-B3J2	FDFB	CQ005 CD001 CU015 CP002 CA003	6-090 6-860	(See RTN. 1113)
	0X02	Prior to forcing the L3 irpt, the L4 CZ ltch are set to CZ = 01, on return to L4 the CZ ltch are tested to ensure that L3 did not alter the preset L4 CZ ltch.	The level 4 CZ ltch were affected by the PCI L3 irpt.	A-B3G2	0003	CZXXX	6-090	
1115	0X01	Level 2 masking and unmasking functions are tested. Level 2 is mask and then an attempt to force a L2 irpt, via "diag L2" function, is performed.	The Level 2 mask function failed to prevent a L2 irpt.	A-B3M2	FDFB	CP002 CD001 CQ001	6-090 6-940	
	0X02	Level 2 is unmasked and a L2 irpt is forced via "diag L2" function.	The Level 2 unmask function failed	A-B3M2	FDFB	CP002 CD001 CQ001	6-090 6-950	
1116		Level 4 is interrupted by Level 2 via the "diag L2" function.						
	0X01	Irpt reg grp 2 (X'7F') is tested for a "diag L2" bit.	The Diag L2 irpt failed to occur	A-B3M2	FDFB	CP002	6-860	
	0X02	Prior to forcing the L2 irpt the L4 CZ ltch are set to CZ = 10. On return to L4 the CZ ltch are tested to ensure that the L2 irpt did not alter the preset L4 CZ ltch.	The Level 4 CZ = 10 ltch were affected by the diag L2 irpt.	A-B3G2	0003	CZXXX	6-090	
1117	0X01	Level 4 is interrupted by Level 2 via the "diag L2" function.	The Diag L2 irpt failed to occur.	A-B3G2	FDFB	CP002	6-090	(See RTN. 1116)
	0X02	Prior to forcing the L2 irpt, the L4 CZ ltch are set to CZ = 01. On return to L4 the CZ ltch are tested to ensure that the L2 irpt did not alter the preset L4 CZ ltch.	The Level 4 CZ = 01 ltch were affected by the diag L2 irpt.	A-B3G2	0003	CZXXX	6-090	
1118	0X01	Level 4 is interrupted by a Level 1 irpt via a I/O check. The utility Reg (X'79') is tested to verify that L4	The utility Reg did not contain the 'prog level 4 interrupted' bit. (Level 1 failed to irpt)	A-B3M2 A-B3L2	00F0	CP004	6-830	Bypass trouble shooting this error until error code 0002 of this

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		was interrupted.						routine has run without error.
	0X02	Irpt req grp 1 (X'7E') is tested for the "in/out check L1" bit.	The in/out check L1 bit did not set. A Level 1 irpt did not occur.	N/A	FFFF	CU014	6-850	
	0X03	Prior to forcing the L1 irpt, the L4 CZ ltch are set to CZ = 10. On return to L4 the CZ ltch are tested to ensure that the L1 irpt did not alter the preset L4 CZ ltch.	The Level 4 CZ = 10 ltch were affected by the L1 irpt.	A-B3G2	0003	CZXXX	6-090	
1119		Level 4 is interrupted by a Level 1 irpt via a I/O check.						
	0X01	The utility Reg (X'79') is tested to verify if L4 was interrupted.	Level 1 failed to irpt.	A-B3L2 A-B3G2	00F0	CU014 CP002	6-803	(See RTN. 1118)
	0X02	Irpt req grp 1 (X'7E') is tested for the in/out check L1 bit.	The in/out check L1 bit did not set.		FFFF		6-050	
	0X03	Prior to forcing the L1 irpt, the L4 CZ ltch are set to CZ = 01.	The Level 4 CZ = 01 ltch were affected by the L1 irpt.	A-B3G2	0003	CZXXX	6-090	
111A		Level 3 is interrupted by Level 2 via diag L2 function.						(See RTN. 1113)
	1X01	Since the DCM runs under Level 4, a L3 irpt is forced via PCI L3 to allow this routine to test while in Level 3.	Pretest error				6-940	
	0X01	A L2 irpt is forced via diag L2. The irpt req grp 2 (X'7E') is tested to verify that diag L2 bit was set.	The diag L2 irpt failed to occur when running under Level 3.		FDFB		6-830	(See RTN 1116)
	0X02	Prior to forcing the L2 irpt, the L3 CZ ltch are set to CZ = 10.	The Level 3 CZ = 10 ltch were affected by the L2 irpt.		0003		6-090	
111B	1X01	Same as 1X01 above.						
	0X01	Same as 0X01 above.						
	0X02	Prior to forcing the L2 irpt, the L3 CZ ltch are set to CZ = 01.	The Level 3 CZ = 01 ltch were affected by the L2 irpt.		0003		6-830	
111C		Level 3 is interrupted by Level 1 via an in/out check L1.						(See RTN. 1113)
	1X01	Since the DCM runs under Level 4, a L3 irpt is forced via PCI L3 to allow this routine to test while in Level 3.	Pretest error.				6-940	
	0X01	The utility Reg (X'79') is tested to verify that L3 was interrupted.	The utility reg did not contain the prog level 3 interrupted bit.	A-B3M2	00F0	CP004	6-830	Bypass trouble shooting this error until error code 0002 of this routine has run without failure.
	0X02	The L1 irpt is forced via in/out check L1.	The in/out check L1 bit did not set. A Level 1 irpt did not occur when running under Level 3.		FFFF		6-050	(See RTN 1118)
	0X03	Prior to forcing the L1	The Level 3 CZ = 10 ltch were		0003		6-090	

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	PEALD PAGE	PETMM PAGE	COMMENTS
		irpt, the Level 3 CZ ltch are set to CZ = 10. On return to L3 the CZ ltch are tested to ensure that the L1 irpt did not alter the preset L3 CZ ltch.	affected by the L1 irpt.					
111D	1X01	Same as 1X01 above under routine 111C.						
	0X01	Same as 0X01 above under routine 111C.						
	0X02	Same as 0X02 above under routine 111C.						
	0X03	Prior to forcing the L1 irpt, the L3 CZ ltch are set to CZ = 01.	The Level 3 CZ = 01 ltch were affected by the L1 irpt.		0003		6-090	
111E		Level 2 is interrupted by Level 1 via an in/out check L1.					6-050	(See RTN. 1116)
	1X02	Since the DCM runs under Level 4, a L2 irpt is forced via diag L2 irpt. This will allow this routine to test while in Level 2.	Pretest error.				6-090	
	0X01	The utility Reg (X'79') is tested to verify that L2 was interrupted.	The utility reg did not contain the prog level 2 interrupted bit.	A-B3M2	00F0	CP004	6-830	Bypass trouble shooting this error until error code 0002 of this routine has run without failure.
	0X02	The L1 irpt is forced via an in/out check L1. irpt reg grp 1 (X'7E') is tested to verify.	The in/out check L1 bit did not set. A level 1 irpt did not occur when running under level 2.		FFFF		6-850	(See RTN 1118)
	0X03	Prior to forcing the L1 irpt, the level 2 CZ ltch are set to CZ = 10. On return to L2, the CZ ltch are tested to ensure that the L1 irpt did not alter the preset L2 CZ ltch.	The level 2 CZ =10) ltch were affected by the L1 irpt.		0002		6-090	
111F	1X02	Same as 1X02 above under routine 111E.						(See RTN 17)
	0X01	Same as 0X01 above under routine 111E.						(See RTN 19)
	0X02	Same as 0X02 above under routine 111E.						
	0X03	Prior to forcing the L1 irpt, the level 2 CZ ltch are set to CZ = 01. On return to L2, the CZ ltch are tested.	The level 3 CZ = 01 ltch were affected by the L1 irpt.		0003		6-090	
1120		This routine does an interrupt Daisy-Chain from L4 to L3 to L2 to L1 to L3 to L4. The CZ ltch latches for L4, L3, and L2 are preset to a known state prior to forcing the next irpt. Each is checked on return to its level.					6-080	(See RTNS. 1113-111F)
	1X01	Level 4 is interrupted by L3 via PCI L3.	Pretest error.				6-090	
	1X02	Level 3 is interrupted by L2 via Diag L2.	Diag L2 irpt failed to occur.		N/A		6-090	

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X01	Prior to forcing the L3 irpt, the level 4 CZ ltch are set to CZ = 10. On return to L4, the CZ ltch are tested to ensure that the L3, L2, and L1 irpt did not alter the preset L4 CZ ltch.	The level 4 CZ = 10 ltch were affected by the L3, L2, and L1 irpt Daisy-Chain.		0003		6-090	
	0X02	Prior to forcing the L2 irpt, the level 3 CZ ltch are set to CZ = 01. On return to L3, the CZ ltch are tested.	The level 3 CZ = 10 ltch were affected by the L2 and L1 irpt Daisy-Chain.		0003		6-090	
	0X03	Prior to forcing the L1 irpt, the level 2 CZ ltch are set to CZ = 10. On return to L2, the CZ ltch are tested.	The level 2 CZ = 10 ltch were affected by the L1 irpt.		0003		6-090	
1121	0X01	Level 4 masking and unmasking functions are tested. Since the DCM runs under PCI L4, this routine resets PCI L4 and waits for a level 3 interval timer L3 irpt. Level 4 is then masked and tested. On the next timer L3 irpt, level 4 is unmasked and tested.	The level 4 mask function failed to prevent a PCI L4 irpt from occurring.	A-B3M2 A-B3L2	N/A	CP002 CP006	6-090 6-940	
	0X02	Level 4 is unmasked and a PCI L4 irpt is set while in level 3. An exit from level 3 is performed and level 4 should irpt via PCI L4.	The level 4 unmask function failed. A PCI L4 irpt did not occur.	A-B3M2	N/A	CP002	6-090 6-950	
1122	0X01	Level 3 masking and unmasking functions are tested. level 3 is masked, an attempt is made to force a L3 irpt via a set PCI L3 irpt.	The level 3 mask function failed to prevent a PCI L3 irpt from occurring. If the level 5 mask function is not active, erroneous errors may occur. If so, run routine 1125 to test the level 5 mask function.	A-B3M2	N/A	CP002	6-940 6-950 6-940	
	0X02	Level 3 is unmasked, an attempt is made to force a L3 irpt via a set PCI L3 irpt.	The level 3 unmask function failed. A PCI L3 irpt did not occur.	A-B3M2	N/A	CP002	6-940	
1123		This routine test for a level 4 service interrupt (svc L4) when an exit from level 5 is performed.						
	0X01	In order to reach level 5 the PCI L4 irpt must be reset and an exit from L4 is performed.	Level 5 failed to become active or level 4 failed to exit (previously tested).	A-B3M2	N/A	CP003	6-090	
	0X02	The exit from level 5 should svc L4 irpt. The irpt req grp 2 (X'7F') will be tested to verify.	The level 5 exit failed to set svc L4 irpt bit.	A-B3M2	0001	CU015	6-860	
	0X03	The level 4 svc L4 irpt will be reset to verify that it can be reset.	svc L4 irpt failed to reset.	A-B3M2	0001	CU015	6-090	
	0X05	A level 5 exit is performed.	Level 5 failed to exit.		N/A		6-750	
1124		This routine tests that level 5 can be interrupted by level 1.						
	0X01	Level 5 is interrupted by level 1 via an in/out check. irpt reg grp 1 (X'7E') is tested to verify that a Level 1 irpt did occur.	The in/out check L1 bit did not set. Level 1 irpt failed to occur.		FFFF	CU014	6-850	
	0X02	The utility reg (X'79') is tested for a Prog level 5	The Prog level 5 Interrupted bit failed to set.	A-B3M2	0010	CP004	6-830	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETBM PAGE	COMMENTS
		interrupted bit. The L1 irpt should cause to utility reg to set the above mentioned bit.						
	0X03	Prior to forcing the L1 irpt the L5 CZ ltch are set to CZ = 01. On return to level 5 the CZ ltch are tested.	The L5 CZ = 01 ltch were affected by the L1 irpt.		0003		6-090	
	0X04	Upon return to level 4 the saved utility reg is tested to verify that the level 5 C and Z condition bits are correct.	The CZ = 01 bits of the utility reg are in error.	A-B3M2	0300	CP004	6-090	
	0X05	Upon return to level 4 and and after the above test have been run, the utility reg is tested to verify that the exit from L2, L5, and the L4 irpt did not affect the level 5 CZ = 01 latch.	The CZ = 01 bits of the utility reg are in error. The L5 exit or svc L4 irpt affected the L5 CZ latch.		0300	CP004	6-090	
1125	0X01	The masking and unmasking of level 5 is tested. Level 5 is masked and instruction execution is halted on Level 4 and an exit from L4 is performed. This should allow Level 5 to become active if the masking function failed.	The Level 5 masking function failed.	A-B3M2	N/A	CP002	6-940 6-950	
	0X02	Level 5 is unmasked to allow level 5 to become active.	The level 5 unmask function failed.		N/A		6-950	
112A	0X01	Invalid input register decode testing. An attempt is made to input an invalid register. An in/out check L1 irpt should result. Invalid register values are in a table. Irpt reg grp 1 (X'7E') is tested for an in/out check L1 bit.	The invalid input register failed to set in/out check.	A-B3L2 A-B3K2 A-B3H2	FFFF	CK007 CU014 CQ001 CD001	6-120 6-120 6-850	Reg X'16' will contain the value of the input register that produce the error. Errors in this RTN could be external to the CCU. (CSB's CA's). Byte 0 Bit 0-3 and byte 1 bits 0-3 are the two Hex values that define the register
	0X02	The LAG Register is tested to verify that the L1 irpt occurred at the invalid test slot.	LAG Register failed to track or the L1 irpt occurred at the wrong address.	A-B3M2	3FFFF	CS001	6-800	
112B	0X01	Invalid output register decode testing. An attempt is made to output an invalid register. An in/out check L1 irpt should result. Invalid register values are in a table. Irpt reg grp 1 (X'7F') is tested for an in/out check Irpt reg grp 1 (X'7E') is	The invalid output register failed to set in/out check.	A-B3L2 A-B3K2 A-B3H2	FFFF	CK007 CU014 CQ007 CD001	6-120 6-850	Reg X'16' will contain the value of the output register that produced the error Byte 0 bits 0-3 and byte 1 bits 0-3 are the two Hex values that define the reg.
	0X02	The LAG Register is tested to verify that the L1 irpt occurred at the invalid test slot.	LAG Register failed to track or the L1 irpt occurred at the wrong address.	A-B3M2	3FFFF	CS001	6-800	
112C		Invalid Op (Instruction) Testing.						
	0X01	An attempt is made to execute a half-word of code that is invalid. Invalid operations	The invalid oepration failed to set op check L1	A-B3L2	FFFF	CU014	6-050 6-850	Reg X'16' will contain the value of the OP that

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	PEALD PAGE	FETMM PAGE	COMMENTS
		are in a table. Irpt reg grp 1 (X'7E') is tested for a Op Check L1 bit.						produce the error.
	0X02	The LAG register is tested to verify that the L1 irpt occurred at the invalid test slot.	LAG register failed to track or the L1 irpt occured at the wrong address.	A-B3M2	3FFFF			
112D	0X01	Invalid Op (instruction) Testing. An attempt is made to execute a half-word of code that is invalid. The invalid Op's are formed from table data or'ed with a varying data field. This routine makes over 300 passes. Irpt reg grp 1 (X'7E') is tested for a Op check L1 bit.	The invalid operation failed to set op check L1	A-B3L2	FFFF	CU014	6-050 6-850	Reg X'16' will contain the value of the invalid Op that produce the error.
	0X02	The LAG register is tested.	LAG register failed to track or the L1 irpt occurred at the wrong address.	A-B3M2	FFFF	CS001	6-800	
112E	0X01	Same as 0X01 above under routine 112D. This routine makes over 600 passes.						
	0X02	Same as 0X02 above under routine 112D.						
112F	0X01	Same as 0X01 above under routine 112D This routine makes over 180 passes.						
	0X02	Same as 0X02 above under routine 112D.						
1130	0X01	Same as 0X01 above under routine 112D This routine makes over 50 passes.						
	0X02	Same as 0X02 above under routine 112D.						
1131	1X03	Test for a level 1 program check when an invalid OP is detected while in level 1. Since the DCM runs in level 4, an invalid in/out check will be used to force this routine to run in level 1.	In/out Check failed to force a L1 irpt (pretest error)		N/A		6-050	
	0X01	Once level 1 is active, an invalid op check is forced. irpt reg grp 1 (X'7E') is tested for an invalid op check.	The invalid op failed to force an error when operating under level 1.	A-B3H2	FFFF	CD004	6-050 6-850	(See RTN 112C or 112D)
	0X02	The invalid op in level 1 should set L1 prog check and CCU check. CCU check reg (X'7D') is tested.	The level 1 invalid OP failed to set the expected check bits.	A-B3N2	FFFF	CK007		
1132	1X03	Test for a level 1 program check when an invalid in/out check is detected while in level 1. Since the DCM runs in level 4, an invalid in/out check will be used to force this routine to run in level 1.	Initial in/out check failed to force a L1 IRPT. (pretest error)		N/A		6-050	
	0X01	Once level 1 is active, an in/out check is forced. irpt reg grp 1 (X'7E') is	The in/out check failed to force an error when operating under level 1		FFFF	CU014		

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		tested for an in/out check.						
	0X02	The in/out check in level 1 should set L1 prog check and CCU check. CCU check reg (X'7D') is tested.	The level 1 in/out check failed to set the expected check bits.	A-B3H2	FFFF	CK007	6-050 6-840	
1133		Address exception test. This routine attempts to load data from the first invalid address and expects an address exception check to occur. The address under test is then increased in increments of 4K until the maximum address is reached.						
	0X01	Test for address exception. Irpt reg grp (X'7E') is tested for address exception check L1 bit.	Address exception failed to occur.	A-B4E2 A-B3F2	0040	CS002 CM003	6-050 6-850	Register X'13' will contain address under test.
	0X02	LAR is tested to verify that it tracks and that the address exception occurred at the expected instruction.	LAR failed to track or address exception check above failed to occur.		FFFF		6-800	
1134	0X01	PCI L3 interrupt register unused bit testing. The data in reg X'11' is varied from 0000 to FFFF to verify that the value of the data does not matter. Cut R1, PCI L3	PCI L3 irpt failed to occur (don't care bits do care).		FDFB			Reg X'16' will contain the value of reg X'11' when error occurred.
1135		Level 4 instruction interaction test.						
	0X01	A given half-word instruction is inserted into an arithmetic sequence at three different points to test for any interaction. The test loop is repeated 48 times with different half-word instructions.	Data expected did not agree. Test instruction was between A 'LHR' and a 'OHR'.		FFFF		6-220	Reg X'16' contains the half-word instruction that caused the interaction.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	PEALD PAGE	FETMM PAGE	COMMENTS
		SPECIAL NOTE:	The purpose of this test is to produce a random sequence of instructions to verify any interaction that may exist. The following code is listed to illustrate the technique used to detect interaction.					
			LA R2,X'8421'	R2= 1000 0100 0010 0001				
			LA R4,X'1248	R4= 0001 0010 0100 1000				
			LHR R4,R4	R4= 0001 0010 0100 1000				
			**----------*					
			TEST SLOT	THE INSTRUCTION UNDER TEST IS STORED IN THIS SLOT				
			**----------*					
			OHR R2,R4	R2= 1001 0110 0110 1001				
			STH R2,SAVE1	SAVE R2 FOR ERROR CODE 0X01 ANALYSIS				
			LA R6,X'FFFF'	R6= 1111 1111 1111 1111				
			**----------*					
			TEST SLOT	THE INSTRUCTION UNDER TEST IS STORED IN THIS SLOT				
			**----------*					
			XHR R2,R6	R2= 0110 1001 1001 0110				
			**----------*					
			TEST SLOT	THE INSTRUCTION UNDER TEST IS STORED IN THIS SLOT				
			**----------*					
			LA R5,X'9669'	R5= 1001 0110 0110 1001				
			NHR R2,R5	R2= 0000 0000 0000 0000				
			STH R2,SAVE2	SAVE R2 FOR ERROR CODE 0X02 ANALYSIS				
	0X02	The final sum of the arithmetic sequence is tested.	Data expected did not agree. The test instruction was between a 'LA' and a 'XHR'.		FFFF		6-220 6-600	Same as above.
1136		Level 3 instruction interaction test. This routine is the same as 1135 above except the test is run under program level 3.						
	1X01	A PCI L3 irpt is used to force a level 3 irpt.	PCI I3 irpt failed. (Pretest error)		N/A		6-090	
	0X01	Same as 0X01 above under routine 1135.						
	0X02	Same as 0X02 above under routine 1135.						
1137		Level 2 instruction interaction test. This routine is the same as 1135 above except the test is run under program level 2.						
	1X02	Diag L2 irpt is used to force a level 2 irpt.	Diag L2 irpt failed. (Pretest error)		N/A		6-090	
	0X01	Same as 0X01 above under routine 1135.						
	0X02	Same as 0X02 above under routine 1135.						
1138		Level 1 instruction interaction test. This routine is the same as 1135 above except the test is run under program level 1.						
	1X03	An invalid output reg is used to force a L1 irpt.	Invalid output reg failed to produce a L1 irpt. (Pretest error)	N/A			6-090	
	0X01	Same as 0X01 above under routine 1135.						
	0X02	Same as 0X02 above under routine 1135.						
1139	0X01	Level 5 instruction interaction test. This routine is the same as 1135					6-090	

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	REALD PAGE	FETCH PAGE	COMMENTS
		above except the test is run under program level 5. Error is same as 0X01 above under routine 1135.						
	0X02	Same as 0X02 above under routine 1135.						
113C		Verify correct indication and operation of Reg X'7A'.						
	0X01	Input X'7A' byte 0 bit 0 not on - CUC instruction.	CDS definition indicates CUC installed, but hardware indicator bit is off.	A-B4T2				Verify CDS definition in Model/Flag byte.
	0X02	Input X'7A' byte 0 bit 0 is on - no CUC instruction.	CDS indicates CUC not installed, but hardware bit is on	A-B4T2				Verify Model/Flag byte of CDS.
	0X03	Cycle Utilization Counter value is not correct. Several passes are made using different values.		A-B4T2				Reg X'14' contains actual CUC value. Reg X'15' contains bits in error. Reg X'16' contains expected CUC value.
113F		BSC CRC polynomial test. This routine will test the hardware CRC circuitry to verify that the correct CRC character is developed.						
	0X01	Using input register X'7B'.	The developed and expected CRC characters did not compare.	A-B3S2	FFFF	CR001-3		See comment below for Routine 1140.
1140	0X01	8-Bit CRC polynomial test	The developed and expected CRC characters did not compare.	A-B3S2	FFFF	CR001-3		Register X'13' will contain an address pointer to the data table. To determine the old CRC, data character, and expected new CRC display the following storage addresses: Reg X'13' Adr= old CRC Reg X'13' Adr plus 2 = Data Reg X'13' Adr plus 4 = New CRC NOTE: Reg X'13' above implies the address contained in Reg X'13'
1141	0X01	7-Bit CRC Polynomial Test	The developed and expected CRC characters did not compare.	A-B3S2	FFFF	CR001-3		See comments for routine 1140.
1142		CRC Polynomial Test for ALC RPQ #858655	The developed and expected CRC characters did not compare. This routine should run only when RPQ 858655 is installed. If the failing 3705 does not have RPQ 858655 installed, check the CDS data.	A-B3C2	FFFF			See comments for routine 1140.
1143		ALC CS3 register Test. This routine should run only when RPQ 858911 is installed. If the failing 3705 does not						

RCUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FE/LI PAGE	FETMM PAGE	COMMENTS
	have RPQ 858911 installed, check the CDS data.						
	0X01 Test bits for RCV/Xmit direction and all CCC bits in input and output registers X'75'.	Input and Output regs X'75' do not compare.					R14 = data read from input reg x'75'. R15 = Bits in error. R16 = Data stored in output reg X'75'.
1144	ALC xmit test. This routine should run only when RPQ 858911 is installed. If the failing 3705 does not have RPQ 858911 installed, check the CDS data.						
	0X01 Test ALC L1 hardware by altering one instruction in the data processing sequence.	Altered instruction failed to produce a L1 inrpt.					Input reg X'7E' byte 1 bit 7 should be on to indicate ALC support L1 err.
	0X02 Test EOM remember part 1. Test if expected.	EOM remember was expected but was not detected. Bit tested is byte 0 bit 1.					R14 = actual data. R16 = Expected data.
	0X03 Test EOM remember part 2. Test if detected	EOM remember was detected but was not expected. Bit tested is byte 0 bit 1.					R14 = actual data. R16 = expected data.
	0X04 Test EOM expected.	EOM was expected but was not detected. Bit tested is byte 0 bit 2.					R14 = actual R16 = expected
	0X05 Test EOM detected.	EOM was detected but was not expected. Bit tested is byte 0 bit 2.					R14 = actual R16 = expected
	0X06 Test end character counter.	The actual end char. cntr. does not compare with the expected. Bits tested are byte 0 bits 5, 6, and 7.					R14 = actual R15 = bits in error R16 = expected
	0X07 Test CCC.	The act. CCC does not compare with the expected. Bits tested are byte 1 bits 2, 3, 4, 5, 6, and 7.					R14 = actual R15 = bits in error R16 = expected
	0X08 Test 1st 2 bytes of buffer.	First two bytes of buffer are in error.					R13 = addr. of buffer. R14 = act. data from buffer R15 = bits in error R16 = expected
	0X09 Test 2nd 2 bytes of buffer.	Second two bytes of buffer are in error.					R13 = addr. of buffer R14 = act. data from buffer R15 = bits in error R16 = expected
	0X0A Test 3rd 2 bytes of buffer.	Third two bytes of buffer are in error.					R13 = addr. of buffer R14 = act. data from buffer R15 = bits in error R16 = expected
	0X0C Test ALC L1 request bit.	ALC L1 request bit not set. Bit tested is byte 1 bit 7 of input reg X'7E'.					Reg X'03' = contents of input reg. X'7E'

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X0D	Test for correct L1 irpt. address.	Actual irpt. address does not compare with expected irpt. address.					LAR should point to irpt. addr. but does not. Reg X'04' = contents of LAR Reg X'05' = bits in error Reg X'06' = expected irpt. address.
	0X0E	Test reset of ALC L1 request bit.	ALC L1 request bit did not reset. Bit tested is byte bit 7.					Reg X'05' = contents of input reg X'7E'.
1145		ALC receive test. This routine should run only when RPQ 858911 is installed. If the failing 3705 does not have RPQ 858911 installed, check the CDS data.						
	0X01	Test ALC L1 hardware by Altering one instruction in the data processing sequence.	Altered instruction failed to produce a L1 interrupt.					Input reg X'7E' byte 1 bit 7 should be on to indicate ALC support L1 error
	0X02	Test EOM remember part 1. Test if expected.	EOM remember was expected but was not detected. Bit tested is byte 0 bit 1.					R14 = actual R16 = expected
	0X03	Test EOM remember part 2. Test if detected.	EOM remember detected but not expected. Bit tested is byte 0 bit 1.					R14 = actual R16 = expected
	0X04	Test GA part 1. Test if expected.	GA expected but not detected. Bit tested is byte 0 bit 2.					R14 = actual R16 = expected
	0X05	Test GA part 2. Test if detected.	GA detected but not expected. Bit tested is byte 0 bit 2.					R14 = actual R16 = expected
	0X06	Test CCC remember expected.	CCC remember expected but not detected. Bit tested is byte 0 bit 4.					R14 = actual R16 = expected
	0X07	Test CCC remember detected.	CCC remember detected but not expected. Bit tested is byte 0 bit 4.					R14 = actual R16 = expected
	0X08	Test end character counter.	The actual end char. CNTR. does not compare with the expected. Bits tested are byte 1 bits 5, 6, and 7.					R14 = actual R15 = bits in error R16 = expected
	0X09	Test CCC.	The actual CCC does not compare with the expected. Bits tested are byte 1 bits 2, 3, 4, 5, 6, and 7.					R14 = actual R15 = bits in error R16 = expected
	0X0A	Test first two bytes of buffer.	First two bytes of buffer are in error.					R13 = addr. of buffer R14 = act. data from buffer R15 = bits in error R16 = expected
	0X0B	Test second two bytes of buffer.	Second two bytes of buffer are in error.					R13 = addr. of buffer R14 = act. data from buffer R15 = bits in error R16 = expected
	0X0C	Test third two bytes of buffer.	Third two bytes of buffer are in error.					R13 = addr. of buffer R14 = act. data from buffer

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	PEALD PAGE	PETMM PAGE	COMMENTS
								R15 = bits in error R16 = expected
	0X0D	Test fourth two bytes of buffer.	Fourth two bytes of buffer are in error.					R13 = addr. of buffer R14 = act. data from buffer R15 = bits in error R16 = expected
	0X0E	Test ALC L1 request bit.	ALC L1 request bit did not set. Bit tested is byte 1 bit 7 of input reg X'7E'.					Reg X'03' = contents of input reg X'7E'
	0X0F	Test for correct L1 interrupt address.	Actual irpt. addr. does not compare with expected irpt. addr.					LAR should point to irpt addr but does not. Reg X'04' = contents of LAR Reg X'05' = Bits in error Reg X'06' = expected
	0X10	Test reset of ALC L1 request bit.	ALC L1 request bit did not reset. Bit tested is byte 1 bit 7.					Reg X'05' = contents of input reg X'7E'
1146	0X01	Storage protect test Set all storage keys to 000. The storage keys are first set and then read and compared for the correct key value. The setting and reading of keys is performed by a major subroutine (S.skFT1).	One of the storage block keys failed to set to 000.	A-B4D2	0007	CVXXX	6-040	See Note 2.
1147	0X01	Set all storage keys to 001.	One of the storage block keys failed to set to 001.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
1148	0X01	Set all storage keys to 010.	One of the storage block keys failed to set to 010.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
1149	0X01	Set all storage keys to 011.	One of the storage block keys failed to set to 011.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114A	0X01	Set all storage keys to 100.	One of the storage block keys failed to set to 100.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114B	0X01	Set all storage keys to 101.	One of the storage block keys failed to set to 101.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114C	0X01	Set all storage keys to 110.	One of the storage block keys failed to set to 110.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114D	0X01	Set all storage keys to 111.	One of the storage block keys failed to set to 111.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 3.
114E	0X01	Storage protect test. Set all protect keys to 000.	One of the protect keys failed to set to 000.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
114F	0X01	Set all protect keys to 001.	One of the protect keys failed to set to 001.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1150	0X01	Set all protect keys to 010.	One of the protect keys failed to set to 010.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1151	0X01	Set all protect keys to 011.	One of the protect keys failed ~~to~~ set to 011.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1152	0X01	Set all protect keys	One of the protect keys	A-B4D2	0007	CVXXX	6-040	See Note 2

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETHM PAGE	COMMENTS
		to 100.	failed to set to 100.					See Note 4.
1153	0X01	Set all protect keys to 101.	One of the protect keys failed to set to 101.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1154	0X01	Set all protect keys to 110.	One of the protect keys failed to set to 110.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1155	0X01	Set all protect keys to 111.	One of the protect keys failed to set to 111.	A-B4D2	0007	CVXXX	6-040	See Note 2. See Note 4.
1156		Special storage protect routine for problem definition mode.						
		This routine will run only if the problem definition mode and the manual intervention CE sense switches are set or if a single routine is requested and the routine requested is 1156. If the PDM sense switch is on, a manual intervention code will be displayed. The CE should then enter the desired 'key' data into switches B, C, D, and E (see Note 2 for layout out 'set key' data - also note that byte 0 bits 0-3 should be entered into switch B, etc). The data entered will determine if a storage key or protect key is set and/or read.						
		This test runs under program level 4.						
		CAUTION: Ensure that the block under test (for setting storage key) does not prevent this routine or the DCM for executing instructions.						
	FX0F	Manual intervention code - CE should enter the desired data into switches B, C, D, and E	N/A		N/A		4-080	For looping on error the DCM CE switch should be set. If not, routine will make only one pass.
	0X01	The 'key' set is tested to verify that it agrees with the expected key.	Key failed to set to the desired value		0007		6-040	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		Storage protection mechanism testing at program level 5. Section 1. The following seven routines test to verify that, if the protect key and storage key match, the user (level 5 is the user) is allowed to access storage for instruction execution. Since the protect keys for program levels 1, 2, 3, and 4 are fixed equal to 0, program level 5 is set up for the appropriate protect key and the actual test section of each routine is tested at program level 5.						
1158		Test that when the storage key is equal to 001 and the protect key (level 5) is equal to 001 that no storage protect errors occur, when an instruction execution is performed.						
	0X01	Irpt req grp 1 X'7E' is tested to verify that a protection check did not occur.	A protection check did occur	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest Error						
	1X21	Pretest Error						
1159		Test that when the storage key is eugal to 010 and the protect key (level 5) is equal to 010 that no storage protect errors occur, when an instruction execution is performed.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur	A protection check did occur	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X12	Pretest Error						
	1X22	Pretest Error						
115A		Test that when the storage key is equal to 011 and the protect key (level 5) is equal to 011 that no storage protect errors occur, when an instruction execution is performed.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X13	Pretest error						
	1X23	Pretest error						
115B		Test that when the storage key is equal to 100 and the protext key (level 5) is equal to 100 that no storage protect errors occur, when an instruction execution is performed.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X14	Pretest error						
	1X25	Pretest error						
115C		Test that when the storage key is equal to 101 and the protect key (level 5) is equal to 101 that no storage protect errors occur, when an instruction						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALR PAGE	FETMM PAGE	COMMENTS
		execution is performed.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X15	Pretest error						
	1X25	Pretest error						
115D		Test that when the storage key is equal to 110 and the protect key (Level 5) is equal to 110 that no storage protect errors occur, when an instruction execution is performed.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X16	Pretest error						
	1X26	Pretest error						
115E		Test that when the storage key is equal to 111 and the protect key (level 5) is equal to 111 that no storage protect errors occur, when an instruction execution is performed.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X17	Pretest error						
	1X27	Pretest error						
		Storage protection mechanism testing at program level 5. Section 2.						
		The following eight routines test to verify that, if protect key and storage key match or if the storage key is 111 (unprotected storage), the user (level 5 is the user) is allowed to modify storage without causing protection checks.						
115F		Test that when the storage key is equal to 001 and the protect key (level 5) is equal to 001 that no storage protect errors occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error						
	1X21	Pretest error						
1160		Test that when the storage key is equal to 001 and the protect key (level 5) is equal to 010 that no storage protect errors occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X12	Pretest error						
	1X22	Pretest error						
1161		Test that when the storage key is equal to 011 and the protect key (level 5) is equal						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		to 011 that no storage protect errors occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X13	Pretest error						
	1X23	Pretest error						
1162		Test that when the storage key is equal to 100 and the protect key (level 5) is equal to 100 that no storage protect errors occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X14	Pretest error						
	1X24	Pretest error						
1163		Test that when the storage key is equal to 101 and the protect key (level 5) is equal to 101 that no storage protect errors occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X15	Pretest error						
	1X25	Pretest error						
1164		Test that when the storage key is equal to 110 and the protect key (level 5) is equal to 110 that no storage protect errors occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X16	Pretest error						
	1X26	Pretest error						
1165		Test that when the storage key is equal to 111 and the protect key (level 5) is equal to 111 that no storage protect errors occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X17	Pretest error						
	1X27	Pretest error						
1166		Test that when the storage key is equal to 111 (unprotected storage) and the protect key (level 5) is some value other than 111 ((101 for this test)) that no storage protect errors occur, when an attempt is made to modify storage.						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did not occur.	A protection check did occur.	AB4D2	FFFF	CVXXX	6-040 6-850	
	1X15	Pretest error						
	1X17	Pretest error						
	1X27	Pretest error						
		Storage protection mechanism testing at program level 5. Section 3. The following four routines test to verify that if the protect key and the storage key are not equal, the user (level 5 is the user) is not allowed to execute an instruction. In addition, protection check should be set.						
116A		Test that when the storage key is equal to 001 and the protect key (level 5) is equal to 110 that storage protection checks will occur, when an attempt is made to execute an instruction.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error						
	1X16	Pretest error						
	1X26	Pretest error						
116F		Test that when the storage key is equal to 110 and the protect key (level 5) is equal to 001 that storage protection checks will occur, when an attempt is made to execute an instruction.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error						
	1X16	Pretest error						
	1X21	Pretest error						
1170		Test that when the storage key is equal to 000 and the protect key (level 5) is equal to 111 that storage protection checks will occur, when an attempt is made to execute an instruction.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X10	Pretest error						
	1X17	Pretest error						
	1X27	Pretest error						
1171		Test that when the storage key is equal to 111 and the protect key (level 5) is equal to 000 that storage protection checks will occur, when an attempt is made to execute an instruction.						
	0X01	Irpt req grp 1 (X'7F') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X10	Pretest error						
	1X17	Pretest error						
	1X20	Pretest error						
1172		Test that when the storage key is equal to 110 and the protect key (level 5) is equal to 111						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		that storage protection checks will occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X16	Pretest error						
	1X17	Pretest error						
	1X27	Pretest error						
		Storage protection mechanism testing at program level 5. Section 4.						
		The following six routines test to verify that, if the protect key and the storage key are not equal and if the protect key is not equal to zero, the user (level 5) is not allowed to modify storage. In addition, protection check should be set.						
1173		Test that when the storage key is equal to 100 and the protect key (level 5) is equal to 110 that storage protection checks will occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X14	Pretest error						
	1X16	Pretest error						
	1X26	Pretest error						
1174		Test that when the storage key is equal to 001 and the protect key (level 5) is equal to 101 that storage protection checks will occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error						
	1X15	Pretest error						
	1X25	Pretest error						
1175		Test that when the storage key is equal to 000 and the protect key (level 5) is equal to 100 that storage protection checks will occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X10	Pretest error						
	1X14	Pretest error						
	1X24	Pretest error						
1177		Test that when the storage key is equal to 011 and the protect key (level 5) is equal to 010 that storage protection checks will occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X12	Pretest error						
	1X13	Pretest error						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	READ PAGE	RETRN PAGE	COMMENTS
	1X22	Pretest error						
1178		Test that when the storage key is equal to 101 and the protect key (level 5) is equal to 001 that storage protection checks will occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 6-850	
	1X11	Pretest error						
	1X15	Pretest error						
	1X21	Pretest error						
1179		Test that when the storage key is equal to 100 and the protect key (level 5) is equal to 111 that storage protection checks will occur, when an attempt is made to modify storage.						
	0X01	Irpt req grp 1 (X'7E') is tested to verify that a protection check did occur.	A protection check did not occur.	A-B4D2	FFFF	CVXXX	6-040 1-040	
	1X14	Pretest error						
	1X17	Pretest error						
	1X27	Pretest error						
1190		The customer usage meter should run when an instruction is executed at program levels 1, 2, 4, 5, and level 3 if 8 ms has elapsed since the interval timer interrupt occurred or if an instruction is executed at level 3 and a non interval timer interrupt has occurred. A series of instructions totaling 24 seconds will be executed on each level for a total run time of 2 minutes (0.034 run time on meter) The CE will be requested to read and enter the meter at the start of the test and at the end. As a result, this routine will run only if the manual intervention CE sense switch is set.					1-040	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	FX01	Manual intervention code - CE should enter meter reading per the following procedure. Meter `* * * * * * * * * * * * * * * * * *` `*   *   *   *   *   *     -     *` `*   *   *   *   *   * 6 - -     *` `* 1 * 2 * 3 * 4 * 5 *     - * * *` `*   *   *   *   *   *     -     *` `*   *   *   *   *   *     -     *` `* * * * * * * * * * * * * * * * * *` 1- When this code is displayed, set the function switch to position (prepare to enter data). 2- Set the meter reading in the data switches B, C, D, and E. (For example, the above meter reading entered would be 4562. The thousandths position should be rounded-off to the next mark to reduce errors.) Press the start pushbutton. 3- After entering the first meter reading leave the function switch set to position 5, watch for display code FX02 and observe the meter. This meter value should then be entered into the data switches as outlined above. Press the start pushbutton.	Data switches = B C D E | | | | +---------- Reading in thousandths - for example at left the value would be 2 (must be 2, 4, 6, 8, or 0) | | | +---------- Reading in hundredths - for example at left the value would be 6 (digit 6 from the left) | | +---------- Reading of digit 5 | +---------- Reading of digit 4				
	EX01	Display code to indicate that this routine is running (2 min.).		N/A	N/A	N/A		
	FX02	Manual intervention code - CE should enter the meter value observed under No. 3 above.			N/A		1-040	
	0X01	The first meter reading is updated by 0.034 and compared with the second reading to verify that the run time is two minutes (0.034 in terms of meter reading).	The meter fail to run correctly or meter reading were not consistent.	A-B3 L2 A-B3 M2	FFFF	CP036 CP037	1-040	Warning: If meter reading entered under FX01 was between 9.966 and 9.999 inclusive a false error will be reported. Rerun the test again.
1191		Customer usage meter test 2 of 2 If no other program levels are active and a level 3 interval timer interrupt occurs, the customer usage meter should not run until after 8 ms has elapsed. This routine will mask off all execution except the interval timer and update a real time type of count. The customer usage meter should not run during this routine. Run time is one minute.					1-040	
	FX01	Same as FX01 above.						
	EX02	Display code to indicate this routine is running (1min.).		N/A	N/A	N/A		
	FX02	Same as FX02 above.						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X01	The first meter reading is saved and compared with the second since the meter should not run, the two meter readings should be equal.	The meter ran or meter readings were not consistent	A-B3 L2 A-B3 M2	FFFF	CP006 CP007	1-040	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	PEALD PAGE	PETME PAGE	COMMENTS
Routine PRETEST error codes 1Xkk								
		The following error codes define failures of functions previously tested by other routines. For each error code A cross reference will be given to point to the routine that originally tested the given function.						
11XX	1X01	Force a Level 3 interrupt via an output X'7C' to set PCI L3	Level 3 interrrupt failed to occur.		N/A		6-940	Routine 1113 previously tested this function. Request routine 1113 and verify if PCI L3 will force a L3 irpt.
11XX	1X02	Force a Level 2 interrupt via an output to set diag L2 irpt.	Level 2 interrupt failed to occur.		N/A		6-900	The DCM set the Level 2 mask prior to loading a given IPT. As a result, Level 2 must be unmasked before forcing a Level 2 irpt. Routine 1115 test both the Unmasking of L2 irpt and masking of L2 irpt via an output to set diag L2.
11XX	1X03	Force a Level 1 interrupt via an invalid output register X'2F'.	Level 1 interrupt failed to occur.		N/A		6-050	Routine 1118 previously tested this function. Request routine 1118 and verify if a Level 1 irpt can be forced via an in/out check.
11XX	1X10	Set a given Storage Key to 000.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 1146 previously tested this function. Run routine 1146 or 1156.
11XX	1X11	Set a given Storage Key to 001.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 1147 previously tested this function. Run routine 1147 or 1156.
11XX	1X12	Set a given Storage Key to 010.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 1148 tested this function. Run routine 1148 or 1156.
11XX	1X13	Set a given Storage Key to 011.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 1149 previously tested this function. Run routine 1149 or 1156.
11XX	1X14	Set a given Storage Key to 100.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 114A previously tested this function. Run routine 114A or 1156.
11XX	1X15	Set a given Storage Key to 101.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 114B

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								previously tested this function. Run routine 114E or 1156.
11XX	1X16	Set a given Storage Key to 110.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 114C previously tested this function. Run routine 114C or 1156.
11XX	1X17	Set a given Storage Key to 111.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 114D previously tested this function. Run routine 114D or 1156.
11XX	1X20	Set a given Protect Key to 000.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 114E tested this function. Run routine 114E or 1156
11XX	1X21	Set a given Protect Key to 001.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 114F previously tested this function. Run routine 114F or 1156.
11XX	1X22	Set a given Protect Key to 010.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 1150 previously tested this function. Run routine 1150 or 1156.
11XX	1X23	Set a given Protect Key to 011.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 1151 previously tested this function. Run routine 1151 or 1156.
11XX	1X24	Set a given Protect Key to 100.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 1152 previously tested this function. Run routine 1152 or 1156.
11XX	1X25	Set a given Protect Key to 101.	Key failed to set.		N/A		6-040 6-880	See notes 2 and 5. Routine 1153 previously tested this function. Run routine 1153 or 1156.
11XX	1X26	Set a given Protect Key to 110.	Key failed to set.		N/A		6-040	See notes 2 and 5. Routine 1154 previously tested this function. Run routine 1154 or 1156.
11XX	1X27	Set a given Protect Key to 111.	Key failed to set.		N/A		6-880	See notes 2 and 5. Routine 1155 previously tested this function. Run routine 1155 or 1156.
11XX	2X11	Subroutine to handle Level 1 interrupts.	A level 1 interrupt has occurred and there are no CCU bits on in either X'7D' CCU check reg or X'7Z' interrupt reg grp 1.	N/A	N/A	N/A	6-840 6-850	Register X'05' has a dummy bits-in-error data X'9999'.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			All level 1 interrupts should occur as a result of a CCU type error.					
11XX	2X12	Subroutine to handle Level 1 interrupts.	A level 1 interrupt has occurred due to some bit in either interrupt req grp 1 (X'7F) and/or adapter interrupt req grp 1 & 2 (X'76' & X'77') The CCUIFT level 1 subroutine resets all forced CCU interrupt conditions and determines that all bits cannot be reset.	N/A	N/A		6-810 6-820 6-860	Register X'05' will contain bits than cannot be reset. If any adapter 21 bits are on, they must be manually reset before pressing start to continue.
11XX	2X13	Subroutine to handle Level 1 interrupts.	A level 1 interrupt has occurred due to a CCU level 1 interrupt. The CCUIFT level 1 subroutine attempts to reset the level 1 interrupt conditions and determines that all bits cannot be reset.	A-B3L2 A-B4D2	N/A	CP005	6-090	Register X'05' will contain the 'or' of the CCU chk reg X'7D' and irpt req grp 1 X'7E'
11XX	2X14	Subroutine to handle Level 1 interrupts.	A level 1 interrupt has occurred and the routine under test did not expect to force a Level 1 irpt. The irpt occurred due to a CCU error.	N/A	N/A	CK006	6-090	Register X'05' will contain the 'or' of the CCU chk reg X'7D' and irpt req grp 1 X'7E'.
11XX	2X15	Subroutine to handle Level 1 interrupts.	A level 1 interrupt has occurred and the routine under test did not expect to force a level 1 irpt. There is not any CCU error bits on; as a result, the irpt must be due to either a channel adapter or CSB request.	N/A	N/A	N/A	6-090 6-810 6-820 6-860	Register X'05' has a dummy bits-in-error data X'9999' Display the following registers to determine the cause of the L1 irpt: X'7F' irpt req grp 2 X'76' adpt req grp 1 X'77' adpt req grp 2 If any adapter bits are on, they must be manually reset before pressing start to continue.
11XX	2X21	Subroutine to handle Level 2 interrupts.	"Diag L2" irpt req bit failed to reset	A-B3M2	N/A	CU014	6-050	
11XX	2X22	Subroutine to handle Level 2 interrupts.	A level 2 interrupt has occurred and the "diag L2" bit is not on in the interrupt req grp 2 (X'7F') - when running the CCUIFT's all level 2 interrupts should result from Diag L2 bit.	N/A	N/A	N/A	6-850	Register X'05' will contain irpt req grp 2 X'7F'
11XX	2X23	Subroutine to handle Level 2 interrupts.	A level 2 interrupt has occurred and either the Type 1 CSB L2 and/or Type 2 CSB L2 bits are on in adapter req grp 2 (X'77') - The CCUIFT level 2 subroutine has attempted to reset by resetting all forced CCU error conditions.	N/A	N/A	CX003	6-820	Register X'05' will contain adpt reg grp 2 X'77'
11XX	2X24	Subroutine to handle Level 2 interrupts.	A level 2 interrupt has occurred and the routine under test did not expect to force a level 2 irpt.	N/A	N/A	N/A	6-090	Register X'05' has a dummy bits-in-error data X'9999'.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								Display registers: X'77' adpt req grp 2 X'7F' irpt req grp 2 to determine the cause of the L2 irpt.
11XX	2X31	Subroutine to handle Level 3 interrupts.	A level 3 interrupt has occurred via a PCI L3 interrupt (X'7C'). The level subroutine attempts to reset the PCI L3 interrupt but fails	A-B3M2	N/A	CU015	6-940	
11XX	2X32	Subroutine to handle Level 3 interrupts.	A level 3 interrupt has occurred and neither the PCI L3, timer L3, nor pushbutton L3 bits are on. All Level 3 interrupts that occur should result from one of the above conditions.	N/A	N/A			Register X'0D' has a dummy bits-in-error data X'9999' Register X'0E' contains adpt req grp 2 X'77'.
11XX	2X33	Subroutine to handle Level 3 interrupts.	A level 3 interrupt has occurred and either the Type I CA L3 and/or Type 2 CA L3 bits are on in adapter req grp 2 (X'77') - The CCUIPT level 3 subroutine has attempted to reset by resetting all forced CCU error conditions.	N/A	N/A	CP005	6-820	Register X'05' will contain adpt req grp 2 X'77' If any adapter bits are on, they must be manually reset before pressing start to continue.
11XX	2X34	Subroutine to handle level 3 interrupts.	A level 3 interrupt has occurred and the routine under test did not expect to force a L3 irpt. The timer L3 and push-button L3 interrupts are expected at all times.	N/A	N/A	N/A	6-090	Register X'0D' has CCU irpt req grp X'7F' loaded. In addition display register X'77' adpt req grp 2 to determine if a channel adapter L3 irpt request occurred.
11XX	2X41	Subroutine to handle Level 4 interrupts	A PCI L4 or SVC L4 irpt has occurred. The SLV4 attempts to reset either or both but determines that one or both cannot be reset.	A-B2M2	N/A	CU015	6-090	Register X'15' contain the irpt req that cannot be reset Byte 0 Bit 7 = PCI L4 Byte 1 Bit 7 = SVC L4
11XX	2X42	Subroutine to handle Level 4 interrupts	A Level 4 irpt has occurred and neither the PCI L4 or SVC L4 bits are on in X'7F'.	N/A	N/A	CU015 CP005	6-860	Register X'15' has a dummy bits-in-error data X'9999'. If any adapter bits are on, they must be manually reset before pressing start to continue.

ROUT. CODE	ERROR	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	PEALD PAGE	PETMM PAGE	COMMENTS
11XX	2X43	Subroutine to handle Level 4 interrupts.	A Level 4 interrupt has occurred and the routine under test did not expect to force a L4 interpt.	N/A	N/A	N/A	6-090	Register X'15' has a dummy bits-in-error data X'0001'. Display register X'7F; CCU IRPT req grp 1. Byte 0 Bit 7 = PCI L4 Byte 1 Bit 7 = SVC L4

ROUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS

NOTE 1: Since the error forcing circuitry has not been previously tested, bypass this error code until code 0002 of the same routine has been run without failure.

NOTE 2: For all of the above Storage Protect Testing routines, register X'16' for error display has special meaning. Reg X'16' will contain the data that was used to output to Reg X'73' (SET KEY). This will allow the BLOCK Address to be displayed as illustrated below.
See routine 1156 for setting up a loop on a given storage or protect key.

For storage size of 256k or less use the following chart.

OUTPUT X'73'	SET KEY
BYTE 0, 0	SKA BIT 0 ----------(G)
1	SKA BIT 1 ----------(H)
2	SKA BIT 2 ----------(J)
3	SKA BIT 3 ----------(K)
4	SKA BIT 4 or PKA BIT 0--(L)
5	SKA BIT 5 or PKA BIT 1--(M)
6	SKA BIT 6 or PKA BIT 2--(N)
7	*
BYTE 1, 0	*
1	*
2	*
3	SELECT KEY ADR 1=SKA 0=PKA
4	SET KEY 1=SET
5	KEY - BIT 0
6	KEY - BIT 1
7	KEY - BIT 2

SAR

BYTE X	BYTE 0								BYTE 1							
67	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
||	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
GH	J	K	L	M	N	-	-	-	-	-	-	-	-	-	-	-

. . . Use this chart to convert block number into address range and vice versa.

Exp. If no key address bits are on, then the block number in question is zero and covers the address range of 0-4097 bytes.

For storage size greater than 256k use the following chart.

OUTPUT X'73'	SET KEY
BYTE 0, 0	SKA BIT 0 ----------Reserved
1	SKA BIT 1 ----------Reserved
2	SKA BIT 2 ----------Reserved
3	SKA BIT 3 ----------(G)
4	SKA BIT 4 or PKA BIT 0--(H)
5	SKA BIT 5 or PKA BIT 1--(J)
6	SKA BIT 6 or PKA BIT 2--(K)
7	SKA BIT 7 ----------(L)
BYTE 1, 0	SKA BIT 8 ----------(M)
1	SKA BIT 9 ----------(N)
2	SKA BIT 10 ----------(O)
3	SELECT KEY ADR 1=SKA 0=PKA
4	SET KEY 1=SET
5	KEY - BIT 0
6	KEY - BIT 1
7	KEY - BIT 2

SAR

BYTE X	BYTE 0								BYTE 1							
567	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
|||	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|	|
GHJ	K	L	M	N	O	-	-	-	-	-	-	-	-	-	-	-

. . . Use this chart to convert block number into address range and vice versa.

Exp. If no key address bits are on, then the block number in question is zero and covers the address range of 0-4097 bytes.

NOTE 3: The first two Storage Block Keys are not changed but are allowed to remain set to 000. This will allow the direct addressable areas, the DCM control module, and the CCUIFT interrupt and subroutine areas to be addressed without Protection checks.

NOTE 4: Only three of the available settable Protect Keys are currently used.

NOTE 5: Use the following chart to determine the first suspected card(s). The table should be keyed off of the failing bits in REG X'15' (Bits in error).

BIT IN ERROR REG X'15'	FAILURE	FUNCTION (Z-BUS)	CARD	LOGIC PAGE
Byte 0, Bit 0	Byte X 20 bit	ALU, AREG, BREG	A-B4S2	DE976
0, Bit 0	Byte X 18,20	ALU, AREG, BREG	A-B4J2	DF976
0, Bit 1	Byte 0	ALU, AREG, BREG	A-B4K2	DG976
0, Bit 2	Byte 1	ALU, AREG, BREG	A-B4M2	DK976

NOTE 6: Use the following chart to determine the first suspected card(s). Key off of the failing bits in Reg X'15' (bits in error).

BIT IN ERROR REG X'15'	FAILURE	FUNCTION	CARD	LOGIC PAGE
Byte 0, Bit 1	Byte 0	SDR	A-B432	DP993
0, Bit 2	Byte 1	SDR	A-B4A2	DR993

NOTE 7: Use the following chart to determine the first suspected card(s). Key off of the failing bits in Reg X'15' (bits in error).

ROUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION		SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	BITS IN ERROR REG X'15'	FAILURE	FUNCTION	CARD	LOGIC PAGE			
	Byte 0, Bit 0	Byte X	SAR	A-B4D2	CV001			
	0, Bit 1	Byte 0	SAR	A-B4D2	CV001			
	0, Bit 2	Byte 1	SAR	A-B4C2	DS001			

RCUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS

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CHAPTER 2.0: STORAGE IPT SYMPTOM INDEX

Routine 1: Addressability (Bridge only)
Routine 2: Address Analysis (Bridge only)
Routine 3: Address Capability (Bridge only)
Routine 4: Address Exception (Bridge only)
Routine 5: Random Addressing (Bridge only)
Routine 6: Complement/Recomplement (Bridge only)
Routine 7: Varied Timing Repetition (Bridge only)
Routine 8: Half Select Repetition (Bridge only)
Routine 9: Worst Case and Schmoo (Bridge only)
(See Special Purpose Routines)
Routine 10: Single Bit Error Correction (FET only)
Routine 11: Double Bit Error Detection (FET only)
Routine 12: Bus Out Parity Test (FET only)
Routine 13: Address Exception (FET only)
Routine 14: Double Bit Error Test (FET only)
Routine 15: Worst Card Analysis (FET only)
(See Special Puspose Routines)
Routine 16: Address Failure Analysis (FET only)
Routine 17: Addressing Capability (FET only)

SPECIAL PURPOSE ROUTINES DESCRIPTION

Routine 09: Can be used for schmoo test (Bridge only)

Routine 15: Worst card analysis, problem definition (FET only)

This description provides a reference to the IPT routines that have special purpose. These routines can be selected via a single routine request; they can also be selected in sequence with the other routines by setting the CE Sense switch to run the manual intervention routine (rtn. 09), or problem definition (rtn 15).
This description serves only as a guide into the more detailed symptom index and does not describe the error stops or manual intervention stops for these routines.

X215 Routine 15 can be run by setting the SSW for problem definition, or by making a single routine request for 15, at IPT select time. This rtn is designed to be run after rtn 14, when a double bit error was detected by rtn 14. This will cause only the 32K in which the double bit error resides to be tested. A 'worst card' in the address range being tested will be indicated if a double bit error was detected by rtn 14. This routine is for FET storage only.

Adapter Considerations

3705 storage routines are executed independently on each BSM (or adapter) except the BSM addressability routine which must be executed on all BSMs simultaneously for a valid test. Errors are detected and displayed by the DCM as established by DCM-IPT conventions.

If FET storage is installed, the entire storage array is considered one BSM.

Failure Analysis

Because a printed list of errors is not available, the recommended failure analysis procedure is to record the error conditions and continue to the next error until a failing pattern is established, such as, single data bit, BSM decode, address decode, etc. Refer to page 7-010 in the FETMM, SY27-0107, to assist in relating failing pattern to component location.

When FET is installed, errors in storage support circuits can appear as array card errors when diagnostics are run. If an array card error is indicated by diagnostics, suggested procedure is to swap the indicated card with another one and run the same diagnostics again. If the error indications remain the same, panel procedures should be used to test the support circuitry (FETMM, SY27-0107, page 7-260). Error indications are as follows unless noted otherwise in the Symptom Index:

Reg X'13' = failing Address
Reg X'14' = actual data received
Reg X'15' = failing data bits or
Reg X'16' = expected data

All routines except worst case routine set bypass CCU check stop mode during the test to allow an error display instead of a hardstop. A worst case routine does not set bypass CCU check stop because parity errors must be detected by a CCU check rather than data verification. Set the DIAGNOSTIC CONTROL switch to BYPASS CCU CHECK STOP position for an error display of data bits if desired.

RCUT. CODE	ERROR	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
Schmoo Test								

The schmoo test is accomplished by setting DIAGNOSTIC CONTROL switch to BYPASS CCU CHECK STOP and set DCM sense switches as follows:

1. Bypass New Error Stop - Byte 0, Bit 7
2. Bypass Error Stop - Byte 1, Bit 4
3. Cycle on Request - Byte 1, Bit 3

Errors can be detected by observing the CCU check light on the control panel.

X2XX	1X01	Initialize subroutine - Provides information needed in routine communication table and verifies correct CDS storage configuration on 1st execution after being loaded.	Configuration data is not equal to machine data. Verify BSM count in CDS. CDS data should agree with hardware Input X'70' storage size.			6-770 4-070	Reg X'14' = data derived from CDS. Reg X'16' = data from Input reg X'70'.
X2XX	2X01	L1 interrupt handler subroutine - Error 1 verifies that a level 1 interrupt has been caused by address exception condition in the address exception routine.	Unexpected L1 interrupt encountered. Address exception expected - other interrupt bit(s) also on. Flag stored by the address exception routine should = Input reg X'7E'. (Interrupt Request) Definition of Unexpected bits: 1.0 - Address compare 1.2 - In/out check 1.3 - Protection check 1.4 - Invalid op 1.6 - IPL level 1 request			6-090	Reg X'04' = interrupt request bits from Input X'7E'. Bit 1.1 expected. Reg X'06' = expected data.
X2XX	2X02	Level1 interrupt handler subroutine - Error 2	A level1 address exception did not occur at expected instruction in address exception routine.			6-050	Reg X'04' = adr of inst following the one causing the level 1 interrupt. Reg X'06' = adr of inst following the one that should have caused interrupt.
X2XX	2X03	L1 interrupt handler subroutine - Error 3 verifies that address exception condition can be reset.	Address exception bit failed to reset after the expected address exception condition.			6-050	Reg X'7E' bit 0 was set by address exception but could not be reset.
X201	0X01	BSM addressability Verifies that each BSM can be addressed properly. Complement of the data is tested to provide a basic sense amplifier test. This Routine runs on bridge storage only.	Incorrect BSM data in 1st half-word of last full-word address of BSM under test. BSM decode or sense amplifier failure. Byte 0 = number of BSMs in machine and byte 1 = BSM addressed.			7-010	Suspect the sense amp if error 0X02 does not occur, BSM decode if error 0X02 occurs.
	0X02	BSM addressability Ref to error code 0X01	Incorrect BSM complement data at last half-word address of BSM addressed. BSM decode or sense amplifier failure.			7-010	Byte 0 = complement of number BSMs in machine. Byte 1 = complement of BSM addressed.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X202		Address analysis test - solid address failure. This routine test the ability to store and display each address. The failing address bits are saved to provide a failing address pattern. Use the diagram below to form the failing pattern from the indications in both error code 0X01 and 0X02 as follows: 0X01 - Failing pattern bits on are saved as 1's in register X'15'. 0X02 - Failing pattern bits off are saved as 1's in register X'15'. X address bits that are not replaced in either error display were not consistently on or off at the time of failure. Y bits in the diagram do not affect the addressing within a BSM. This Routine runs on bridge storage only. Y Y Y X X X X X X X X X X X X X 16K Select / Low Y Decode / Low X Decode BSM Select / Hi Y Decode / Hi X Decode / Not Used					
	0X01	Address Analysis. Individual failures are not displayed, but the bits that were on at the time of the failure are saved for a composite display of the common bits that were on in the failing address pattern.	Solid address failure. Replace X's in the diagram with 1's for the bits in register X'15' that are on.					Register X'15' is a composite of the failing address. Ignore registers X'13' X'14', and X'16'.
	0X02	Address analysis. Individual failures are not displayed, but the bits that were off at the time of the failure are saved to form a composite display of the common bits that were off in the failing address pattern.	Solid Address failure. Replace X's in the diagram with 0's for the bits in register X'15' that are on. Ignore the low order bit in register X'15'.					Register X'15' is a composite of the failing address. Ignore registers X'13', X'14', and X'16'.
X203	0X01	Addressing capability. This Routine runs on bridge storage only.	Address data is not equal to the address. Can be data bit failure or address decode. Address decode failure causes an 'overlay' condition in which one of the affected addresses is not addressed.				7-010 7-030	Data should equal to 16 bit address. Establish pattern to determine whether data or address is failing.
X204	0X01	Address exception Verifies that address exception causes correct indications. This Routine runs on bridge storage only.	Failed to cause program L1 check interrupt in address exception routine. A level 1 interrupt should have occurred because an attempt to store data at an invalid address.				6-050	The invalid address is in reg X'13'.
X205	0X01	Random addressing Address is stored as data in non-sequential operation then verified. This Routine runs on bridge storage only.	Address data not equal to the 16 bit address.				7-010 7-030	Data should equal to the low order 16 bits of its address.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X206	0X01	Complement/recomplement This Routine Runs on bridge storage only.	Data pattern failure. Pattern is stored then verified. Data in reg X'14' should equal pattern in reg X'16'.				7-030	
	0X02	Complement/recomplement Above pattern is complemented, stored, then verified. Expected data= complement of pattern.,	Complement pattern failure. R14=Received R15=Bits in error R6=Expected				7-030	
	0X03	Complement/recomplement Above complemented pattern is re-complemented, stored, then verified. Should be equal to the pattern.	Recomplement pattern failure. R14=Received R15=Bits in error R6=Expected				7-030	
X207	0X01	Varied repetiton X'FFFF' is stored in the BSM being tested and varied after a 600 micro sec. delay. This Routine runs on bridge storage only.	Incorrect data--600 microsec delay after store.				7-030	
	0X02	Varied repetition Ref Error Code 0X01	Incorrect data -- 3 sec delay after store.					
X208	0X01	Continued repetition Addresses are selected diagonally in array to be beat 32 times with pattern. Half selected cores on the same X and Y drive lines as the selected addresses are tested. This Routine runs on bridge storage only.	Incorrect data - X Drive Line. Incrementing Y drive address to test X drive line cores. X drive line same as selected 'beat' address.				7-030 7-020	Refer to 7-010 for drive line relationship to failing addresses.
	0X02	Continued repetition Ref error code 0X01	Incorrect data - Y Drive Line. Incrementing X drive address to test Y drive line cores. Y drive line same as selected 'beat' address.				7-020	Same as error code 0X01.
X209	0X01	Worst case. Generates 'worst case' pattern in core then verifies data. Pattern is reversed to change parity. Test is run in check stop mode to detect parity bit failures. If DCM error codes are desired, set DIAGNOSTIC CONTROL Switch to BYPASS CCU CHECK STOP. For SCHMOO testing reference IFT heading. This Routine runs on bridge storage only.	Failed worst case pattern When CCU check occurs, set DISPLAY/FUNCTION switch to STATUS to determine failing data byte. Compare expected and actual data to determine failing bit. Note that parity is not indicated, but can cause failure.				7-020	Worst case pattern is generated on a core plane basis. Bits on a core plane = 11001100, complemented each 4096 bytes. Various data values are used to generate this pattern.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X210		Single bit error correction test This routine tests the ability to detect and correct a single bit or check bit error in storage. An error is forced via the diagnostic register for each of the data bits and check bits in both the on and off condition. The results are tested to verify that the bit was corrected. An error in this routine could be caused by storage support circuitry. See IBM 3705 COMMUNICATIONS CONTROLLER THEORY MAINTENANCE MANUAL, SY27-0107, page 7-260. This routine runs on FET storage only.						
	0X01	Single bit error correction.	Failed to correct single bit error. Error was forced via the diagnostic register.				7-220	R14=Actual data R15=Bit in error
	0X02	Single bit error correction.	Failed to correct single bit error in complement pattern. Error was forced via the diagnostic register.				7-220	R14=Actual data R15=Bit in error
	0X03	Data bit error. Error(s) already exists in storage.	Unable to verify single bit error correction due to error(s) already existing in storage at several addresses.				7-220	R14=Actual data R15=Bit in error
	0X04	Check bit error. Error(s) already exists in storage.	Unable to verify single bit error correction due to error(s) already existing in storage at several addresses.				7-220	R14=Actual data R15=Bit in error
X211		Double bit error detection test This routine tests the ability to detect a double bit error and provide the correct error indications. Double bit errors are forced via the diagnostic register. This routine runs on FET storage only.						
	0X01	Double bit error detection. Problem may be ECC card or other storage support logic.	Failed to detect a double bit error. CCU check register X'7D' should indicate SDB check.				7-220	R13=Data address R14=Actual bits from CCU check reg X'7D' R15=CCU check reg. bits in error. R16=Data stored

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X212		Bus out parity-store zero test This routine forces bad parity on CCU bus out via output reg. X'78' to verify that if a bus out check occurs, zeros are stored in storage and a double bit error condition is indicated to the CCU when that address is read. This routine runs on FET storage only.						
	0X01	Bus out parity	SDR check not indicated.				7-220	R13=Test address R14=Data Read from test address should=X'0000' R15=CCU check reg. bits received should contain SDR check.
	0X02	Bus out parity.	Stored data not equal to zero with forced bus out check.					R13=Test address R15=Received data should =X'0000' R6=Stored data
X213		Address exception test This routine tests ability to generate an address exception L1 interrupt or fold condition in which the data is stored in address zero. Flags are set to indicate to the L1 interrupt handler sub-routine that an address exception L1 Interrupt is expected. The interrupt or fold should occur during an attempt to store into an invalid address. This routine runs on FET storage only.						
	0X01	CDS,input X'70' compare	Number of 32K increments derived from CDS and input X'70' do not compare.					R14=Number of 32K increments, taken from CDS data, after one shift left and should compare with input X'70'. Ex: 64K in CDS=8200, after one shift left=0400. 64K in input X'70=0400. R15=Bits in error. R16= Input X'70'.
	0X02	Address exception or fold For 64K or 256K, max. addr. +2=addr. 0 or fold. For any other Storage size, max. addr. +2= addr. excep.	Failed to indicate address exception or fold. Address exception should occur except for 64K or 256K, in which cases the address should fold to zero.					R13=Maximum valid address determined from input X'70'. R14=Data Read from Address zero. Should be zero due to fold condition

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X214		Double bit error pattern test. This routine stores, loads and tests a pattern, its complement and its recomplement. Two patterns are used to provide bit variation. No errors are forced via the diagnostic register. If a double bit error occurs, a test is made to determine if both bits in error are on the same card, in which case the card is identified. If the bits in error are on both cards of a pair, information is saved for worst card analysis routine #15. Pattern 1 = 5555/AAAA Pattern 2 = 8001/7FFE This Routine runs on FET storage only.						
	0X01	Double bit error	A double bit error has occurred and both errors have been determined to be in a single array card as identified by reg X'15' displacement value.				7-220	R13=Failing addr. R15=Displacement into worst card table (See note 1 rtn #15)
	0X02	Double bit error If rtn. 14 was run as single rtn. request continue to termination and request rtn 15. If problem definition SSW was set at IFT select, continue. If it was not, set 9101 in data switches, function 1, and continue.	A double bit error has occurred, but cannot be isolated to a single array card. Suggested procedure is to set DCM sense switch for 'Problem Definition' to cause rtn #15 to be run, or run RTN as a single Routine. A flag is set to cause rtn #15 to test only the failing array cards.				7-220	R13=Failing Addr. at which the double bit error occurred.

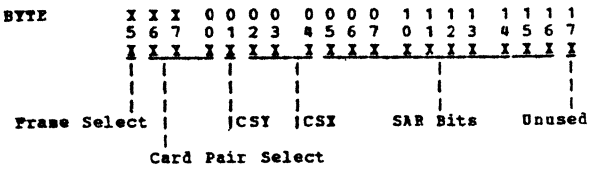
ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X215		Single bit error pattern Test. Note: This Routine runs in 'Problem Definition' mode and requires either the DCM sense switch or to be run as a single routine request. This routine stores, loads and tests a pattern, its complement and its recomplement. Two patterns are used to provide bit variation. ***Single Bit Error Forced*** Pattern 1 = 5555/AAAA Pattern 2 = 8001/7FFE This Routine runs on FET storage only.						
	0X01	Worst card analysis	The 'worst card' has been determined.			7-220		R15=Displacement into worst card table. See Note 1. If Reg 15=X'10', worst FET card= Pos. N2
	0X02	Worst card analysis Worst Card=card with greatest number of single bit errors.	Double bit error detected in Routine 14 has caused 'worst card' within the range of addresses where the double bit error exists to be determined.			7-220		R15=Displacement into worst card table. See Note 1. If Reg 15=X'10', worst FET card= Pos. N2

Note 1: Array card identification:

Frame 01 Gate 01B Address	Displacement/Card		Frame 02 Gate 02B Address	Displacement/Card	
00000 - 07FFE	00/J2	02/J4	40000 - 47FFE	20/J2	22/J4
08000 - 0FFFE	04/K2	06/K4	48000 - 4FFFE	24/K2	26/K4
10000 - 17FFE	08/L2	0A/L4	50000 - 57FFE	28/L2	2A/L4
18000 - 1FFFE	0C/M2	0E/M4	58000 - 5FFFE	2C/M2	2E/M4
20000 - 27FFE	10/N2	12/N4	60000 - 67FFE	30/N2	32/N4
28000 - 2FFFE	14/P2	16/P4	68000 - 6FFFE	34/P2	36/P4
30000 - 37FFE	18/Q2	1A/Q4	70000 - 77FFE	38/Q2	3A/Q4
38000 - 3FFFE	1C/R2	1E/R4	78000 - 7FFFE	3C/R2	3E/R4

	E0XX	This code is displayed because rtn. 15 takes longer than 20 sec. to run. It indicates only that the rtn. is running and not in a loop.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X216		Address Failure Analysis This Routine attempts to analyze a solid addressing failure by storing each address in its own location as data. Failures are saved for a composite error display, from which consistent address bits can be analyzed. Failing pattern can be determined by combining bits consistently ON from error code 0X01 and bits consistently OFF from error code 0X02. This routine runs on FET storage only. Bit definitions are as follows:						
	0X01	Address failure analysis	Address failure analysis - Part 1 of 2 - Address failure - Replace bits in address layout with a 1 for each bit on in Reg '15'. Continue to error code 0X02 to complete failing pattern.				7-220	R15=Bits consistently ON in all failures
	0X02	Address failure analysis	Address failure analysis - Part 2 of 2 - Addressing failure - Replace bits in address layout with a 0 for each bit on in Reg X'15'. Bits remaining as X after error code 0X01 and 0X02 were not consistent in the failures.				7-220	R15=Bits consistently OFF in all failures
X217		Addressing capability This routine checks addressing capability by storing each location with its own address as data and testing that the data was stored correctly. This routine runs on FET storage only.						
	0001	Addressing capability	Addressing failure. Compare expected and actual data to determine address bits in error.				7-230	R13=Failing address R14=Actual data R15=Bits in error R16=Expected Data



ROUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS

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CHAPTER 3.0: TYPE 1 CHANNEL ADAPTER SYMPTOM INDEX

The type "1" CA IFT symptom index is a listing of error codes relating to failures occurring during the operation of the IFT. All bits of the CA registers which have both input and output capability are tested with several patterns, including all ones, zeros, every other bit, growing-ones, and floating-zeros patterns. Interaction between these registers is also checked. In addition to verification of register operation, the function of program requested and suppress-out monitor level 3 interrupts are verified. Error codes are also given for unexpected and/or unknown level 1 and level 3 interrupts and if the CA interface was not disabled.

RTN	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1301	0X01	Disable CA Type 1 interface	Channel interface was not disabled	A4P2	0008	RC103		
1302	0X02	CA Diagnostic Reset	Did not clear reg X'60'	A4L2	FFFF	RC402	8-130	
1302	0X04	CA Diagnostic Reset	Did not clear reg X'62'	A4L2	FFFF	RC403	8-130	
1302	0X08	CA Diagnostic Reset	Did not clear reg X'66'	A4T2	FFFF	RC601	8-130	
1302	0X09	CA Diagnostic Reset	Did not clear reg X'67'	A4K2	00FF	RC505	8-130	
1303	0X0A	Set reg X'63' to X'0000'	Unable to set reg X'63' to X'0000'	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1304	0X0B	Set reg X'63' to X'FFFF'	Unable to set reg X'63' to X'FFFF'	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1305	0X0C	Set reg X'63' to X'5555'	Unable to set reg X'63' to X'5555'	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1305	0X0D	Set reg X'63' to X'AAAA'	Unable to set reg X'63' to X'AAAA'	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1306	0X0E	Set reg X'63' using floating zeros pattern	Unable to set reg X'63' using floating zeros pattern	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1307	0X0F	Set Reg X'63' using growing ones pattern	Unable to set reg X'63' using growing ones pattern	A4M2, A4P2 A4K2	FFFF	RC502	8-100	
1308	0X0A	Set reg X'64' to X'0000'	Unable to set reg X'64' to X'0000'	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
1309	0X0B	Set reg X'64' to X'FFFF'	Unable to set reg X'64' to X'FFFF'	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130A	0X0C	Set reg X'64' to X'5555'	Unable to set reg X'64' to X'5555'	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130A	0X0D	Set reg X'64' to X'AAAA'	Unable to set reg X'64' to X'AAAA'	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130B	0X0E	Set reg X'64' using floating Zeros pattern	Unable to set reg X'64' using floating zeros pattern	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130C	0X0F	Set reg X'64' using growing ones pattern	Unable to set reg X'64' using growing ones pattern	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130D	0X0A	Set reg X'65' to X'0000'	Unable to set reg X'65' to X'0000'	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130E	0X0B	Set reg X'65' to X'FFFF'	Unable to set reg X'65' to X'FFFF'	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130F	0X0C	Set reg X'65' to X'5555'	Unable to set reg X'65' to X'5555'	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
130F	0X0D	Set reg X'65' to X'AAAA'	Unable to set reg X'65' to X'AAAA'	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
1310	0X0E	Set reg X'65' using floating zeros pattern	Unable to set reg X'65' using floating zeros pattern	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
1311	0X0F	Set reg X'65' using growing ones pattern	Unable to set reg X'65' using growing ones pattern	A4M2, A4P2 A4K2	FFFF	RC502	8-110	
1312	0X0B	Set reg X'66' to X'CF00' by output of X'40CF' to reg X'66'	Unable to set reg X'66' to X'CF00'	A4T2	FFFF	RC601	8-120	

RTN	ERROR CODE	FUNCTION TESTED LOCATION(S)	ERROR DESCRIPTION	SUSPECTED CARD	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1313	0X0C	Set reg X'66' to X'4500' by output of X'0045' to reg X'66'	Unable to set reg X'66' to X'4500'	A4T2	FFFF	RC601	8-120	
1313	0X0D	Set reg X'66' to X'8A00' by output of X'008A' to reg X'66'	Unable to set reg X'66' to X'8A00'	A4T2	FFFF	RC601	8-120	
1314	0X0E	Set reg X'66' using floating zeros pattern	Unable to set reg X'66' using floating zeros pattern	A4T2	CF00	RC601	8-120	
1315	0X0F	Set reg X'66' using growing Zeros pattern	Unable to set reg X'66' using growing zeros pattern	A4T2	CF00	RC601	8-120	
1316	0X0A	Set reg X'62' to X'0000'	Unable to set reg X'62' to X'0000'	A4L2	FFFF	RC403	8-080	
1317	0X10	Set reg X'62' to X'8000' outbound transfer sequence	Unable to set reg X'62' to X'8000'	A4L2	FFFF	RC403	8-080	
1318	0X11	Set reg X'62' to X'4000' inbound transfer sequence	Unable to set reg X'62' to X'4000'	A4L2	FFFF	RC403	8-080	
1319	0X12	Set reg X'62' to X'2000' ESC final status transfer sequence	Unable to set reg X'62' to X'2000'	A4L2	FFFF	RC403	8-080	
131A	0X13	Set reg X'62' to X'1000' NSC channel end transfer sequence	Unable to set reg X'62' to X'1000'	A4L2	FFFF	RC403	8-080	
131A	0X14	Set Channel End status when setting reg X'62' to X'1000'	Unable to set reg X'66' to X'0800'	A4L2	FFFF	RC601	8-080	
131B	0X15	Set reg X'62' to X'0800' NSC final status transfer sequence	Unable to set reg X'62' to X'0800'	A4L2	FFFF	RC403	8-080	
131B	0X16	No bits are set in reg X'66' when setting reg X'62' to X'0800'	Reg X'66' not all zeros	A4T2	FFFF	RC601	8-080	
131C	0X0A	PRE-TEST. Set reg X'62' to X'0000'	Unable to set reg X'62' to X'0000'	A4L2	FFFF	RC403		Rerun Rtn 1316
131C	0X20	Set level 3 program requested interrupt	Level 3 interrupt did not occur	A4T2	0006	RC601	8-080	
131D	0X0A	PRE-TEST. Set reg X'62' to X'0000'	Unable to set reg X'62' to X'0000'	A4L2	FFFF	RC403		Rerun Rtn 1316
131D	0X21	Set suppress out monitor	Level 3 interrupt did not occur	A4T2	000A	RC602	8-080	
131E	0X0A	PRE-TEST. Set reg X'63' to X'0000'	Unable to set reg X'63' to X'0000'	A4M2	FFFF	RC403		Rerun Rtn 1303
131E	0X40	When X'0000' is set in reg X'63' it does not set reg X'64'	Reg X'64' set incorrectly	A4D2, A4K2	FFFF	RC502	8-100 8-110	
131E	0X41	When X'0000' is set in reg X'63' it does not set reg X'65'	Reg X'65' set incorrectly	A4D2, A4K2	FFFF	RC402	8-100 8-110	
131E	0X42	When X'0000' is set in reg X'63' it does not set reg X'66'	Reg X'66' set incorrectly	A4D2, A4K2	FFFF	RC502	8-100 8-120	
131F	0X0A	PRE-TEST. Set reg X'64' to X'0000'	Unable to set reg X'64' to X'0000'	A4M2	FFFF	RC502		Rerun Rtn 1308
131F	0X43	When X'0000' is set in reg X'64' it does not set reg X'65'	Reg X'65' set incorrectly	A4D2, A4K2	FFFF	RC502	8-110 8-120	
131F	0X44	When X'0000' is set in reg X'64' it does not set reg X'66'	Reg X'66' set incorrectly	A4D2, A4K2	FFFF	RC601	8-110 8-120	

RTN	ERROR CODE	FUNCTION TESTED LOCATION(S)	ERROR DESCRIPTION	SUSPECTED CARD	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
131F	0X45	When X'0000' is set in reg X'64' it does not set reg X'63'	Reg X'63' set incorrectly	A4D2, A4K2	FFFF	RC502	8-100 8-110	
1320	0X0A	PRE-TEST. Set reg X'65' to X'0000'	Unable to set reg X'65' to X'0000'	A4M2	FFFF	RC502		Rerun Rtn 130D
1320	0X46	When X'0000' is set in reg X'65' it does not set reg X'66'	Reg X'66' set incorrectly	A4D2, A4K2	FFFF	RC601	8-110	
1320	0X47	When X'0000' is set in reg X'65' it does not set reg X'63'	Reg X'63' set incorrectly	A4D2, A4K2	FFFF	RC502	8-110 8-100	
1320	0X48	When X'0000' is set in reg X'65' it does not set reg X'64'	Reg X'64' set incorrectly	A4D2, A4K2	FFFF	RC502	8-110	
1321	0X0B	PRE-TEST. Set reg X'63' to X'FFFF'	Unable to set reg X'63' to X'FFFF'	A4M2	FFFF	RC502		Rerun Rtn 1304
1321	0X4C	When X'FFFF' is set in reg X'63' it does not set reg X'64'	Reg X'64' set incorrectly	A4D2, A4K2	FFFF	RC502	8-100 8-110	
1321	0X4D	When X'FFFF' is set in reg X'63' it does not set reg X'65'	Reg X'65' set incorrectly	A4D2, A4K2	FFFF	RC502	8-100 8-110	
1321	0X4E	When X'FFFF' is set in reg X'63' it does not set reg X'66'	Reg X'66' set incorrectly	A4D2, A4K2	FFFF	RC601	8-100 8-120	
1321	0X4F	When X'FFFF' is set in reg X'63' it does not set reg X'60'	Reg X'60' set incorrectly	A4D2, A4K2	FFFF	RC402	8-100 8-120	
1321	0X51	When X'FFFF' is set in reg X'63' it does not set reg X'62'	Reg X'62' set incorrectly	A4D2, A4K2	FFFF	RC403	8-100 8-080	
1322	0X0B	PRE-TEST. Set reg X'64' to X'FFFF'	Unable to set reg X'64' to X'FFFF'	A4M2	FFFF	RC502		Rerun Rtn 1309
1322	0X52	When X'FFFF' is set in reg X'64' it does not set reg X'65'	Reg X'65' set incorrectly	A4D2, A4K2	FFFF	RC502	8-110	
1322	0X53	When X'FFFF' is set in reg X'64' it does not set reg X'66'	Reg X'66' set incorrectly	A4D2, A4K2	FFFF	RC601	8-110 8-120	
1322	0X54	When X'FFFF' is set in reg X'64' it does not set reg X'60'	Reg X'60' set incorrectly	A4D2, A4K2	FFFF	RC402	8-110 8-070	
1322	0X56	When X'FFFF' is set in reg X'64' it does not set reg X'62'	Reg X'62' set incorrectly	A4D2, A4K2	FFFF	RC403	8-080 8-110	
1322	0X56	When X'FFFF' is set in reg X'64' it does not set reg X'62'	Reg X'62' set incorrectly	A4D2, A4K2	FFFF	RC403	8-080 8-110	
1322	0X57	When X'FFFF' is set in reg X'64' it does not set reg X'63'	Reg X'63' set incorrectly	A4D2, A4K2	FFFF	RC502	8-100 8-110	
1323	0X0B	PRE-TEST. Set reg X'65' to X'FFFF'	Unable to set reg X'65' to X'FFFF'	A4M2	FFFF	RC502		Rerun Rtn 130E
1323	0X58	When X'FFFF' is set in reg X'65' it does not set reg X'66'	Reg X'66' set incorrectly	A4D2, A4K2	FFFF	RC601	8-120 8-110	
1323	0X59	When X'FFFF' is set in reg X'65' it does not set reg X'60'	Reg X'60' set incorrectly	A4D2, A4K2	FFFF	RC402	8-070 8-110	

RTN	ERROR CODE	FUNCTION TESTED LOCATION(S)	ERROR DESCRIPTION	SUSPECTED CARD	PROG	FEALD	FETMM	COMMENTS
			MASK PAGE PAGE					
1323	0X5B	When X'FFFF' is set in reg X'65' it does not set reg X'62'	Reg X'62' set incorrectly	A4D2, A4K2	FFFF	RC403	8-080 8-110	
1323	0X5C	When X'FFFF' is set in reg X'65' it does not set reg X'63'	Reg X'62' set incorrectly	A4D2, A4K2	FFFF	RC502	8-100 8-110	
1323	0X5D	When X'FFFF' is set in reg X'65' it does not set reg X'64'	Reg X'64' set incorrectly	A4D2, A4K2	FFFF	RC502	8-110	
1323	0X5E	When X'00CF' is set in reg X'66' it does not set reg X'60'	Reg X'60' set incorrectly	A4D2, A4K2	FFFF	RC402	8-120 8-070	
1324	0X0B	PRE-TEST. Output X'00CF' to reg X'66'	Input from reg X'66' not X'CF00'	A4T2	FFFF	RC601		Rerun Rtn 1312
1324	0X60	When X'00CF' is set in reg X'66' it does not set reg X'62'	Reg X'62' set incorrectly	A4D2, A4K2	FFFF	RC403	8-120 8-080	
1324	0X61	When X'00CF' is set in reg X'66' it does not set reg X'63'	Reg X'63' set incorrectly	A4D2, A4K2	FFFF	RC502	8-120 8-120	
1324	0X62	When X'00CF' is set in reg X'66' it does not set reg X'64'	Reg X'64' set incorrectly	A4D2, A4K2	FFFF	RC502	8-120 8-110	
1324	0X63	When X'00CF' is set in reg X'66' it does not set reg X'65'	Reg X'65' set incorrectly	A4D2, A4K2	FFFF	RC502	8-120 8-110	
13XX	1X01	Disable CA type 1 interface	Channel interface was not disabled	A4P2	0008	RC103	8-130	
13XX	1X0A	Set regs to X'0000'	Unable to set regs to X'0000'	A4M2, A4P2	FFFF	RC501	8-100 8-110	
13XX	1X0B	Set all used bit positions to 1's	Unable to set 1's to all used bit positions	A4M2, A4P2	FFFF	RC501	8-100 8-110	
13XX	2X00	Unexpected level 1 interrupt	Level 1 interrupt with no request bits on	A4K2	XXXX	RC505	8-340	
13XX	2X01	Unexpected level 3 interrupt	Initial selection level 3 interrupt bit on in reg X'77' (bit 1.4)	A4L2	XXXX	RC402		
13XX	2X02	Reset initial selection level 3 interrupt	Failed to reset initial selection level 3 interrupt	A4L2	XXXX	RC402	8-080	
13XX	2X03	Unexpected level 3 interrupt	Data/status level 3 interrupt bit on in reg X'77' (bit 1.3) without suppress out monitor or program requested interrupt bits on in reg X'67'	A4L2	XXXX	RC403	8-090	Reg X'62' should indicate cause interrupt
13XX	2X04	Reset data/status level 3 interrupt	Failed to reset data/status level 3 interrupt	A4L2	XXXX	RC602	8-080	
13XX	2X05	Unexpected suppress out level 3 interrupt	Suppress out interrupt bit on in reg X'77' (bit 0.6)	A4T2	XXXX	RC602		
13XX	2X06	Reset suppress out monitor level 3 interrupt	Failed to reset suppress out monitor	A4T2	XXXX	RC602	8-080	
13XX	2X07	Unexpected level 3 interrupt	Unexpected prog reg interrupt	A4T2	XXXX	RC602	8-090	
13XX	2X08	Reset program requested level 3 interrupt	Failed to reset program requested level 3 interrupt	A4T2	XXXX	RC602	8-080	
13XX	2X09	Unexpected level 3 interrupt from type 1 CA	No request bits on in reg X'62'	A4L2, A4T2	XXXX	RC407	8-090	
13XX	2X1X	Unexpected level 1 interrupt	Local store check	A4K2	XXXX	RC505	8-340	Combinations of more than one

RTN	ERROR CODE	FUNCTION TESTED LOCATION(S)	ERROR DESCRIPTION	SUSPECTED CARD	PROG MASK	FEALD PAGE	FETMH PAGE	COMMENTS
13XX	2X2X	Unexpected level 1 interrupt	CCU Outbus check	A4K2	XXXX	RC505	8-340	level 1 interrup cause will be
13XX	2X4X	Unexpected level 1 interrupt	In/Out instr accept check	A4K2	XXXX	RC505	8-340	indicated by Y in error code
13XX	2X8X	Unexpected level 1 interrupt	Channel Bus-in check	A4K2	XXXX	RC505	8-340	X'2XYX' and thes causes may be
13XX	2XFF	Reset unexpected level 1 interrupt	Failed to reset level 1 interrupt	A4K2	XXXX	RC505	8-130	separated into codes X'2X1X' - X'2X8X'

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CHAPTER 4.0: TYPE 2 AND TYPE 3 CHANNEL ADAPTER SYMPTOM INDEX

The type 2 channel adapter symptom index lists the error codes relating to failures occurring during the operation of the IPT. The CA is tested in diagnostic wrap mode, which wraps around the channel bus and tag interfaces. These interfaces are then controlled by 3705 instructions manipulating the diagnostic bus and tag registers to simulate the operation of the CA. This Symptom Index can be used to its maximum effectiveness to isolate channel faiures by continuing the current routine (DISPLAY/FUNCTION SELECT switch set to FUNCTION 5) or aborting the current routine (DISPLAY/FUNCTION SELECT switch set to FUNCTION 6) to locate additional error codes after the first error code is displayed. In the FEALD PAGE column, the pages are given for Type 2 CA. Look at the equivalent FEALD S-series pages for Type 3 CA.

RTN	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X401	0X01	Force level 3 interrupt (Reg X'57' bit 1.0)	No type 2 CA level 3 interrupt occurred	A4K2	X0008	QJ001	9-210	
	0X02	Select type 2 CA1 or CA2 (Reg X'57' bit 1.4)	Level 3 interrupt with no request bit (Reg X'77' bits 1.2, 1.4)	A4L2	XXXXX	QH001	9-210	
	0X03	Select type 2 CA1 or CA2 (Reg X'57' bit 1.4)	Level 3 interrupt from both type 2 CA's (Reg X'77' bits 1.2, 1.4)	A4L2	XXXXX	QH001	9-210	
	0X04	Select type 2 CA1 or CA2 (Reg X'57' bit 1.4)	Level 3 interrupt from other type 2 CA (Reg X'77' bits 1.2, 1.4)	A4L2	XXXXX	QH001	9-210	
	0X05	Program requested type 2 CA level 3 interrupt	Program requested type 2 CA level 3 bit off (Reg X'55' bit 0.4)	A4K2	X0008	QJ002	9-190	
	0X06	Reset type 2 CA level 3 request (Reg X'57' bit 1.3)	Program requested type 2 CA level 3 bit on (Reg X'55' bit 0.4)	A4K2	X0001	QJ001	9-190	
	0X07	CA selected bit for selected channel	CA selected bit off (Reg X'55' bits 1.6, 1.7)	A4L2	X0003	QH001	9-190	
X402	0X01	Set diagnostic mode (Reg X'57' bit 1.7)	Failed to set diagnostic mode (Reg X'55' bit 0.0)	A4L2	X8000	QH006	9-210	Routine has 60 second time out. Clock-out from CP may not have drop Test routine X402 to observe whethe the CA can be selected if clock out has dropped from the CPU.
X403	0X01	CA reset (Reg X'58' bit 1.7)	Failed to reset CASWSR (Reg X'53')	A4J2	XF300	QK003	9-220	
	0X02	CA reset (Reg X'58' bit 1.7)	Failed to reset CASTR (Reg X'54')	A4L2	XDF00	QK002	9-220	
	0X03	CA reset (Reg X'58' bit 1.7)	Failed to reset CTDR (Reg X'5B')	A4N2	XFCFD	QF003	9-220	
	0X04	CA reset (Reg X'58' bit 1.7)	Failed to reset CHDR (Reg X'5C')	A4K2	XFA01	QJ003	9-220	
	0X05	CA reset (Reg X'58' bit 1.7)	Failed to reset CBODR (Reg X'58')	A4H2	XFF80	QE001	9-220	
X404	0X01	Set all CADB bits on (Reg X'5A')	CADB bits not all on (Reg X'5A')	A4H2, A4G2	XFFFF	QL001	9-240	Byte 0=A4G2 Byte 1=A4G2
	0X02	Set all CADB bits off (Reg X'5A')	CADB bits not all off (Reg X'5A')	A4H2, A4G2	XFFFF	QL001	9-240	Same as above
	0X03	Set CADB to X'AAAA' (Reg X'5A')	Invalid bit pattern in CADB (Reg X'5A')	A4H2, A4G2	XFFFF	QL001	9-240	Same as above

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X04	Set CADB to X'5555' (Reg X'5A')	Invalid bit pattern in CADB (Reg X'5A')	A4H2, A4G2	XFFFF	QL001	9-240	Same as above
X405	0X01	Set all INCWAR bits on (Reg X'50')	INCWAR bits not all on (Reg X'50')	A4H2, A4G2	XFFFE	QL001	9-110	Same as above
	0X02	Set all INCWAR bits off (Reg X'50')	INCWAR bits not all off (Reg X'50')	A4H2, A4G2	XFFFE	QL001	9-110	Same as above
	0X03	Set INCWAR to X'AAAA' (Reg X'50')	Invalid bit pattern in INCWAR (Reg X'50')	A4H2, A4G2	XFFFE	QL001	9-110	Same as above
	0X04	Set INCWAR to X'5555' (Reg X'50')	Invalid bit pattern in INCWAR (Reg X'50')	A4H2, A4G2	XFFFE	QL001	9-110	Same as above
X406	0X01	Set all OUTCWAR bits on (Reg X'51')	OUTCWAR bits not all on (Reg X'51')	A4H2, A4G2	XFFFE	QL001	9-120	Same as above
	0X02	Set all OUTCWAR bits off (Reg X'51')	OUTCWAR bits not all off (Reg X'51')	A4H2, A4G2	XFFFE	QL001	9-120	Same as above
	0X03	Set OUTCWAR to X'AAAA' (Reg X'51')	Invalid bit pattern in OUTCWAR (Reg X'51')	A4H2, A4G2	XFFFE	QL001	9-120	Same as above
	0X04	Set OUTCWAR to X'5555' (Reg X'51')	Invalid bit pattern in OUTCWAR (Reg X'51')	A4H2, A4G2	XFFFE	QL001	9-120	Same as above
X407	0X01	Set CTDR byte 0 to all zeros (Reg X'5X' byte 0)	CTDR byte 0 not all zeros (Reg X'5B')	A4N2	XFC00	QF002	9-250	
	0X02	Set CTDR byte 0 to all ones (Reg X'5X' byte 0)	CTDR byte 0 not all ones (Reg X'5B')	A4N2	XFC00	QF002	9-250	
	0X03	Set CTDR Byte 0 to X'AA' (Reg X'5B')	Invalid bit pattern in CTDR (Reg X'5B')	A4N2	XFC00	QF002	9-250	
	0X04	Set CTDR Byte 0 to X'55' (Reg X'5B')	Invalid bit pattern in CTDR (Reg X'5B')	A4N2	XFC00	QF002	9-250	
X408	0X01	Set CBODR to all zeros (Reg X'58')	Invalid bit pattern in CBODR (Reg X'58')	A4R2	XFF80	QE001	9-220	
	0X02	Set CBODR to X'XFF80' (Reg X'58')	Invalid bit pattern in CBODR (Reg X'58')	A4R2	XFF80	QE001	9-220	
	0X03	Set CBODR to X'AA80' (Reg X'58')	Invalid bit pattern in CBODR (Reg X'58')	A4R2	XFF80	QE001	9-220	
	0X04	Set CBODR to X'5500' (Reg X'58')	Invalid bit pattern in CBODR (Reg X'58')	A4R2	XFF80	QE001	9-220	
X409	0X01	Set INCWAR, OUTCWAR valid latches (Reg X'55' bits 0.2, 0.3)	Failed to set INCWAR, OUTCWAR valid latches (Reg X'55' bits 0.2, 0.3)	A4L2	X3000	QH005	9-180	
	0X02	Reset INCWAR, OUTCWAR valid latches (Reg X'56' bits 0.2,0.3)	Failed to reset INCWAR,OUTCWAR valid latches (Reg X'55' bits 0.2, 0.3)	A4L2	X3000	QH005	9-180	
X40B	0X01	No response to 'op-out' (Reg X'5X', bit 0.4)	Invalid response to 'op-out' in CTDR (Reg X'5B')	A4N2, A4R2	X00FF	QF002	9-250	Display level 4, reg 5 to see error lines
X40C	0X01	No response to 'op-out' with device address on bus-out (Reg X'58')	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-220	Display level 4, reg 5 to see error lines
X40D	0X01	'Select-in' response to 'op-out' and 'sel/hold-out' (Reg X'5B')	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-250	Display level 4, reg 5 to see error lines

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X40E	0X01	'Op-in' response to 'op-out' and 'address-out' and 'sel/hold-out' and valid address on bus-out (Regs X'58', X'5B')	Op-in not set in CTDR (Reg X'5B')	A4N2	X0020	QF002	9-220	Cause of the failur may be a mismatch between CDS address and the plugged cha address.
X40F	0X01	'Select-in' response to 'op-out' and 'address-out' and 'sel/hold-out' and all invalid addresses on bus-out (Regs X'5B', X'58')	Invalid response in CTDR (Reg X'5B') or invalid address in CBODR (Reg X'58')	A4S2, A4N2	X00FF	QC007	9-220 9-250	
	0X11	PRE-TEST. CTDR Reset by CA reset	CA Reset did not reset CTDR	A4N2, A4Q2	X00FF	QF006	9-220	Rerun Rtn X40A
X410	0X01	'Select-in' response to 'op-out' and 'address-out' and 'sel/hold-out' and bad parity on channel bus-out	Invalid response in CTDR (Reg X'5B') or invalid address parity in CBODR (Reg X'58')	A4F2, A4N2	X00FF	QN001	9-250	Address is unit address of channel adapter.
X411	0X01	'Address-in' during initial selection sequence using CTDR (Reg X'5B')	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	
	0X11	PRE-TEST. 'Op-in' response to 'op-out', and 'address -out,' and 'sel/hold-out' and valid address on bus-in	Invalid response in CTDR	A4N2	X00FF	QF002	9-250	Rerun Rtn X40E
X412	0X01	Selective Reset from 'suppress-out' up and op-out down in CTDR (Reg X'5B')	Selective reset bit in CACR (Reg X'55' bit 1.3) did not set	A4N2	X0010	QF005	9-250	
	0X02	Reset of selective reset during level 3 interrupt	Selective reset bit in CACR (Reg X'55' bit 1.3) did not reset	A4N2	X0010	QF006	9-180	
	0X11	PRE-TEST. Selective reset bit off initially (Reg X'55' bit 1.3)	Selective reset bit initially on	A4N2	X0010	QF006	9-180	
X414	0X01	Write Break command decode	Write Break command bit in CMDR (Reg X'5C' bit 0.6) not set	A4K2	XFA01	QJ003	9-260	
	0X02	Channel Write Break remembrance latch	Channel Write Break Remembrance latch (Reg X'55' bit 1.1) not set		X0040		9-390 9-180	
	0X11	PRE-TEST. Reset of CMDR (Reg X'5C')	CMDR did not reset from a CA reset	A4K2	XFA01	QJ003	9-220	
X415	0X01	'Address-in' dropped after 'command-out' response to 'address-in' with a valid command on channel bus-out.	'Address-in' bit in CTDR (Reg X'5B') did not drop	A4N2	X00FF	QF003	9-250	
X416	0X01	'No-op' command decode	No-op command bit in CMDR (Reg X'5C' bit 0.3) not set	A4K2	XFA01	QJ003	9-260	
	0X11	PRE-TEST. Reset of CMDR (Reg X'5C')	CMDR did not reset from a CA Reset	A4K2	XFA01	QJ003	9-260	
X417	0X01	Test I/O command decode	Test I/O command bit in CMDR (Reg X'5C' bit 0.0) not set	A4K2	XFA01	QJ003	9-260	
	0X11	PRE-TEST. Reset of CMDR (Reg X'5C')	CMDR did not reset from a CA reset	A4K2	XFA01	QJ003	9-260	
X418	0X01	Sense command decode	Sense command bit in CMDR (Reg X'5C' bit 0.4) not set	A4K2	XFA01	QJ003	9-260 9-310	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X11	PRE-TEST. Reset of CHDR (Reg X'5C')	CHDR did not reset from a CA reset	A4K2	XFA01	QJ003	9-260	
X419	0X01	Write command decode	Write command bit in CHDR (Reg X'5C' bit 0.1) not set	A4K2	XFA01	QJ003	9-260 9-390	
	0X11	PRE-TEST. Reset of CHDR (Reg X'5C')	CHDR did not reset from a CA reset	A4K2	XFA01	QJ003	9-260	
X41A	0X01	Read command decode	Read command bit in CHDR	A4K2	XFA01	QJ003	9-260	
	0X11	PRE-TEST. Reset of CHDR (Reg X'5C')	CHDR did not reset from a CA reset	A4K2	XFA01	QJ003	9-260	
X41B	0X01	Channel Write IPL command decode	Channel Write IPL command bit in CHDR (Reg X'5C' bit 1.7) not set	A4K2	XFA01	QJ003	9-260 9-320	
	0X11	PRE-TEST. Reset of CHDR (Reg X'5C')	CHDR did not reset from a CA reset	A4K2	XFA01	QJ003	9-260	
X41C	0X01	Channel Command decode	Test decode of valid commands Bit 1.4 expected to be set in Reg 5C	A4K2	XFA01	QJ003	9-260	
	0X02	Valid cmd in reg 5A	Expected cmd in reg 15 Cmd rcvd from Reg 5A in Reg 14	A4K2	XFA09	QJ003	9-260	
	0X03	Check status reg 54	Channel end not set in reg 54 Results of input 54 in reg 14	A4K2	XFA01	QJ003	9-260	
	0X11	PRE-TEST. Reset of CHDR (Reg X'5C')	CHDR did not reset from a CA reset	A4K2	XFA01	QJ003	9-260	
X41D	0X01	Decode all invalid commands	Invalid command in CBODR (Reg X'58') decoded as valid command in CHDR (Reg X'5C')	A4K2	XFA01	QJ003	9-260	
	0X11	PRE-TEST. CTDR (Reg X'5B') reset by CA reset	CTDR did not reset from a CA Reset	A4N2, A4Q2	XFFFF	QF006	9-250	
X41E	0X01	No active inbound tag lines after selective reset	Active inbound tag line in CTDR (Reg X'5B') after selective reset	A4N2	X00FF	QF003	9-250	
X41F	0X01	'Command-out' dropping brings up 'status-in'	'Status-in' not up in CTDR (Reg X'5B' bit 1.4)	A4N2	X0008	QF003	9-250	
	0X11	PRE-TEST. Rtn X415 procedure	'Address-in' bit in CTDR (Reg X'5B') did not drop	A4N2	X0010	QF003	9-250	Rerun Rtn X415
X420	0X01	Zero initial status from a Test I/O command	Sense byte not zero in CASTR (Reg X'54' byte 0)	A4J2	XFF00	QK001	9-170	
	0X02	Zero initial status from Read command	Sense byte not zero in CASTE (Reg X'54' byte 0)	A4J2	XFF00	QK001	9-170	
	0X03	Zero initial status from Sense command	Sense byte not zero in CASTP (Reg X'54' byte 0)	A4J2	XFF00	QK002	9-170	
	0X04	Zero initial status from Write command	Sense byte not zero in CASTR (Reg X'54' byte 0)	A4J2	XFF00	QK001	9-170	
	0X11	PRE-TEST. Rtn X41F procedure	Invalid CTDR (Reg X'5B') response to dropping 'command-out'	A4N2	X000F	QF003	9-250	Expected: 'Status-in'; Rerun Rtn X41F
X421	0X01	CE and DE status to No-op command	Invalid status in CASTR (Reg X'54' byte 0)	A4J2	XFF00	QK002	9-170	
	0X11	PRE-TEST. Reset of CASTR	CASTR did not reset from a	A4J2	XFF00	QK002	9-170	

ROUT.	ERROR CODE	FUNCTION TESTED (Reg X'54')	ERROR DESCRIPTION CA reset	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X12	PRE-TEST. Rtn X41F procedure	Invalid CTDR (Reg X'5B') response to dropping 'command-out'	A4N2	XFFFF	QF003	9-250	Rerun Rtn X41F
X423	0X01	Asynchronous device end presentation after setting IPL prep device end	In-tags invalid in CTDR (Reg X'5B') initially	A4N2	X00FF	QF003	9-250	Expected: request -in
	0X02	Asynchronous device and presentation after setting IPL prep device end	In-tags invalid in CTDR (Reg X'5B') after raising select/hold out	A4N2	X00FF	QF003	9-250	Expected: Op-in & adr-in
	0X03	Asynchronous device end presentation after setting IPL prep device end	In-tags invalid in CTDR (Reg X'5B') after raising	A4N2	X00FF	QF003	9-250	Expected: Op-in only
	0X04	Asynchronous device end presentation after setting IPL prep device end	In-tags invalid in CTDR (Reg X'5B') after dropping command-out	A4N2	X00FF	QF003	9-250	Expected: op-in & status-in
	0X05	Asynchronous device end presentation after setting IPL prep device end	Invalid status in CASTR (Reg X'54' byte 0)	A4J2	XFF00	QK002	9-170	Expected: device-end
	0X11	PRE-TEST reset of CASTR (Reg X'54')	CASTR did not reset from a CA reset	A4J2	XFF00	QK002	9-170	
X424	0X01	Accept initial status from No-op command, part 1. 'Service-out' is raised	In-tags invalid in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	'Status-in' should drop when 'service-out' is raised leaving only 'op-in' tag
X425	0X01	Accept initial status from No-op command, part 2. 'Service-out' is dropped	In-tags invalid in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	Only 'op-in' should be up
X426	0X01	Accept initial status from No-op command, part 3. 'Op-out' is dropped	In-tags invalid in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-250	No in-tag should be up
X429	0X01	Stack status of No-op command, part 1. 'Status-in' drops with 'command-out' response to 'status-in'	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	Only 'op-in' tag valid
X42A	0X01	Stack status of No-op command, Part 2. 'Request-in' up when 'sel/hold-out' dropped	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Only 'request-in' tag valid
X42B	0X01	Stack status of No-op command, part 3. 'Request-in' up when 'command-out' and 'sel/hold-out' dropped	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Only 'request-in' tag valid
X42E	0X01	No in-tags after stacked status suppressed	In-tags in CTDR (Reg X'5B') not all zero	A4N2	X00FF	QF005	9-250	
	0X11	PRE-TEST. Rtn X42B procedure	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Exp 'request-in' Rerun Rtn X42B
X42F	0X01	Present stacked status-Part 1. 'Op-in' and	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Only 'op-in' and 'address-in' tags

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETHM PAGE	COMMENTS
		'address-in' with stack status after 'op-out' and 'sel/hold-out'						valid
	0X11	PRE-TEST. Rtn X42B procedure	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Exp 'request-in' Rerun Rtn X42F
X430	0X01	Present stacked status, Part 2. CA selected up through 'op-out', 'sel/hold-out', and 'command-out'	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Only 'op-in' tag valid
X431	0X01	Present stacked status of CE-DE on No-op command	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Only 'op-in' and 'status-in' tags valid
	0X02	Present stacked status of CE-DE on No-op command	Invalid status in CASTR (Reg X'54')	A4N2	XFF00	QF004	9-170	Only CE-DE status valid
	0X11	PRE-TEST. Rtn X42F procedure	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Exp 'op-in' and 'address-in': Rerun Rtn X42B
	0X12	PRE-TEST. Rtn X430 procedure	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Expected: 'op-in' Rerun Rtn X430
X432	0X01	Present zero stacked status on No-op command	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Only 'op-in' and 'status-in' tags valid
	0X02	Present zero stacked status on No-op command	Status in CASTR (Reg X'54') not all zeros	A4J2	XFF00	QK006	9-170	
	0X11	PRE-TEST. Rtn X42F procedure	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Expected: 'op-in' and 'addr-in'; Reru Rtn X42F
	0X12	PRE-TEST. Rtn X430 procedure	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Expected: 'op-in'; Rerun Rtn X430
X433	0X01	Command reject response to all invalid commands	Command reject bit in CASNSR (Reg X'53' bit 0.0) not set by invalid command	A4J2, A4K2	X8000	QK004	9-150	
	0X02	Unit check response to all invalid commands	Invalid status in CASTR (Reg X'54')	A4J2, A4K2	X0E00	QK003	9-170	Expected: UC
	0X11	PRE-TEST. Reset of CASNSR (Reg X'53') and CASTR (Reg X'54')	CASNSR or CASTR did not reset after CA reset	A4J2	XFFFF	QK003	9-220	
X434	0X01	Set Intervention required bit in CASNSR (Reg X'53' bit 0.1)	Intervention required bit in CASNSR not set or invalid status in CASTR (Reg X'54')	A4J2	XFFFF	QK004	9-140	Expected status: CE, and DE, and UC; byte 0 of mask sense and byte 1 of mask=status
	0X11	PRE-TEST. Reset of CASNSR (Reg X'53') and CASTR (Reg X'54')	CASNSR or CASTR did not reset after CA reset	A4J2	XFFFF	QK003	9-140	
X435	0X01	Set abort bit in CASNSR (Reg X'53' bit 0.7)	Abort bit in CASNSR not set or invalid status in CASTR (Reg X'54')	A4J2	XFFFF	QK005	9-140	Expected status: UC; byte 0 of mask= sense and byte 1 of mask=status
	0X11	PRE-TEST. Reset CASNSR (Reg X'53') and CASTR (Reg X'54')	CASNSR or CASTR did not reset after CA reset	A4J2	XFFFF	QK003	9-140	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X436	0X01	Bus-out Check caused by bad parity on Channel Test I/O command	Bus-out Check and Equipment Check bits in CASNSR (Reg X'53' bit 0.2) not set or invalid status in CASTR (Reg X'54')	A4J2	XFFFF	QK004	9-140	Expected: Bus-out Check and Equip Check and UC; Mask byte 0=sense and Mask byte 1=sta
	0X02	Bus-out check caused by bad parity on channel Write command	Same as above	A4J2	XFFFF	QK004	9-140	Same as above
	0X03	Bus-out check caused by bad parity on channel Read command	Same as above	A4J2	XFFFF	QK004	9-140	Same as above
	0X04	Bus-out Check caused by bad parity on channel No-op command	Same as above	A4J2	XFFFF	QK004	9-140	Same as above
	0X05	Bus-out Check caused by bad parity on channel Sense command	Same as above	A4J2	XFFFF	QK004	9-140	Same as above
	0X06	Bus-out check cuased by bad parity on Write Break command	Same as above	A4J2	XFFFF	QK004	9-140	Same as above
	0X07	Level 1 interrupt occurring due to bus-out check	Level 1 interrupt did not occur	A4K2	X2000	QJ001	9-500	
	0X08	Chan Bus Out Check bit (Reg X'56' bit 0.6) set because of bad parity on bus out lines	Chan Bus Out Check bit not set because of bad parity on bus out lines	A4F2	XFFFF	QN001		
	0X11	PRE-TEST. Reset of CASNSR (Reg X'53') and CASTR (Reg X'54')	CASNSR or CASTR did not reset after CA reset	A4J2	XFFFF	QK003	9-140	
X437	0X01	Unit Exception (UE) set by channel Write command with in and out CWAR valid latch not set	Unit Exception not set in CASTR (Reg X'54')	A4J2	XFFFF	QK003	9-170	Mask byte 0=sense Mask byte 1=status
	0X02	Unit Exception (UE) set by channel Read command with in and out CWAR valid latch not set	Unit Exception not set in CASTR (Reg X'54')	A4J2	XFFFF	QK003	9-170	Mask byte 0=sense Mask byte 1=status
	0X11	PRE-TEST. Reset CASNSR (Reg X'53') and CASTR (Reg X'54')	CASNSR or CASTR did not reset after CA reset	A4J2	XFFFF	QK003	9-160	
X438	0X01	Issue invalid command; stack and present stacked status	Command reject bit in CASNSR (Reg X'53' bit 0.0) not set or invalid status in CASTR (Reg X'54')	A4J2	XFFFF	QK004	9-160	Expected status: UC; Mask byte 0=sense Mask byte 1=status
X439	0X01	Issue valid command with bad parity; stack and present stacked status	Bus-out check and equipment check bits in CASNSR (Reg X'53' bit 0.2) not set or invalid status in CASTR (Reg X'54')	A4J2	XFFFF	QK004	9-160	Expected status: CE, DE, and UC status Mask byte 0=sense Mask byte 1=status
	0X02	Same as above	Level 1 interrupt from bus-out check did not occur	A4K2	X2000	QJ001	9-160	
X43A	0X01	Issue channel No-op command; stack, present and accept stacked initial status up through raising 'service-out'	Invalid tags in CTDR (Reg X'5B'): 'status-in' did not fall when 'service-out' was raised	A4N2	XFFFF	QF003	9-250	'Op-in' only in-tag expected
	0X11	PRE-TEST. Rtn X431 procedure	Invalid CASTR (Reg X'54') response	A4N2	XFF00	QF004	9-160	Expected: CE and DE; Rerun Rtn X431
X43B	0X01	Issue Channel No-op command; stack, present and accept stacked initial status	Invalid tags in CTDR (Reg X'5B'): 'status-in' failed to drop when 'service-out'	A4N2	XFFFF	QF003	9-250	'Op-in' only in-tag expected

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			came up					
	0X11	PRE-TEST. Rtn X431 procedure	Invalid CASTR (Reg X'54') response	A4N2	XFF00	QF004	9-160	Expected: CE and DE status; Rerun Rtn X431
	0X12	PRE-TEST. Rtn X43A procedure	Invalid CTDR (Reg X'5B') response	A4N2	XFFFF	QF003	9-250	Rerun Rtn X43A
X43D	0X01	Issue invalid command and accept initial status	Invalid in-tags in CTDR (Reg X'5B'): 'status-in' failed to drop when 'service-out' came up	A4N2	X00FF	QF003	9-250	'Op-in' only in-tag expected
	0X11	PRE-TEST. Rtn X433 procedure	Invalid CASTR (Reg X'54') response	A4J2, A4K2	XFF00	QK004	9-170	Rerun Rtn X433
	0X12	PRE-TEST. 'Status-in' response to dropping 'command -out'	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Rerun Rtn X433
X43E	0X01	Accept initial status from all valid commands with bad parity	Invalid in-tags in CTDR (Reg X'5B'): 'status-in' failed to drop when 'service-out' came up	A4N2	X00FF	QF003	9-250	'Op-in' only in-tag expected
	0X11	PRE-TEST. Level 1 interrupt on bus-out check	Level 1 interrupt did not occur	A4K2	X2000	QJ001	9-500	Rerun Rtn X436
	0X12	PRE-TEST. Rtn X436 procedure	Invalid CASTR (Reg X'54') response	A4J2	XFF00	QK004	9-170	Expected: UC statu Rerun Rtn X436
	0X13	PRE-TEST. Rtn X436 procedure	Invalid CTDR (Reg X'54') response	A4N2	X00FF	QF004	9-170	Expected: 'status-i and 'op-in'; Rerun Rtn X436
X440	0X01	Sense command does not reset CASNSR (Reg X'53')	CASNSR (Reg X'53') was reset by Sense command	A4J2	XFF00	QK006	9-150	
	0X02	No-op command does not reset CASNSR (Reg X'53')	CASNSR (Reg X'53') was reset by No-op command	A4J2	XFF00	QK006	9-150	
	0X03	Test I/O command does not reset CASNSR (Reg X'53')	CASNSR (Reg X'53') was reset by No-op command	A4J2	XFF00	QK006	9-150	
	0X11	PRE-TEST. Reset of CASNSR (Reg X'53')	CASNSR did not reset with CA reset	A4J2	XFF00	QK006	9-150	
X441	0X01	Issue channel Test I/O command after stacked status for No-op command	Invalid CASTR (Reg X'54') or CTDR (Reg X'5B')	A4J2, A4N2	XFFFF	QK006	9-170 9-250	'Status-in' should be up with CE, DE status; Mask byte 0=status Mask byte 1=tags in
X442	0X01	Issue a channel Test I/O command after stacked status for No-op command with bad parity	Invalid CASTR (Reg X'54') or CTDR (Reg X'5B')	A4J2, A4N2	XFFFF	QK004	9-170 9-250	Expected: 'status-in' and 'op-in' up with CE, DE, and UC Mask byte 0=status Mask byte 1=tags in
	0X11	PRE-TEST. Level 1 interrupt from valid command with bad parity	Level 1 interrupt did not occur	A4K2	X2000	QJ001	9-500	Rerun Rtn X439
	0X12	PRE-TEST. Rtn X439 procedure	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Expected: 'op-in' and 'status-in'; Rerun Rtn X439
	0X13	PRE-TEST. Rtn X439 procedure	Invalid CTDR (Reg X'5B') response	A4N2	X00FF	QF004	9-250	Expected: 'request-in' Rerun Rtn X439
	0X14	PRE-TEST. Level 1 interrupt from bus-out check	No level 1 interrupt	A4K2	X00FF	QJ001	9-500	Rerun Rtn X439

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	PEALD PAGE	FETMS PAGE	COMMENTS
X443	0X01	Issue a Chan Test I/O command after status stacked on No-op command and bring up 'service-out'	Inval in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	'Op-in' only tag in expected up
	0X11	PRE-TEST. Rtn X441 procedure	Invalid response in CASNSR (Reg X'53') or CASTR (Reg X'54')	A4J2, A4N2	XFFFF	QK004	9-140 9-160	Rerun Rtn X441
X444	0X01	Issue a channel Write command after status stacked on No-op command	Invalid CASTR (Reg X'54') or CTDR (Reg X'5B')	A4J2, A4N2	XFFFF	QK001	9-160 9-250	Expected: 'status-in' and 'op-in' tag up with busy, and CE and DE status; mask byte 0=status mask byte 1=tags-in
X445	0X01	Issue a channel Write command after status stacked on invalid command	Invalid CASTR (Reg X'54') or CTDR (Reg X'5B')	A4J2, A4N2	XFFFF	QK001	9-160 9-250	Expected: 'status-in' and 'op-in' tag up with Busy and UC status; mask byte 0=status mask byte 1=tags in
	0X11	PRE-TEST. Dropping 'command-out' brings up 'status-in'	In-tags invalid in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	Expected: 'op-in' and 'status-in. Rerun Rtn X41F.
	0X12	PRE-TEST. Initial selection up to 'command-out' up and 'sel/hold-out' down	In-tags invalid in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Expected: 'request-in'; Rerun Rtn X438
X447	0X01	Issue Channel Read and Write commands after intervention required and abort bits are set in CASNSR (Reg X'53')	CASNSR Reg X'53') not reset after channel Read or Write commands	A4J2	XFF00	QK004	9-140	
	0X11	PRE-TEST. Set abort and intervention required bits in CASNSR (Reg X'53')	Invalid CASNSR	A4J2	XFF00	QK004	9-140	Rerun Rtn X434 and X435
X448	0X01	Initial selection and selective-reset after intervention required and abort bits are set in CASNSR (Reg X'53')	CASNSR (Reg X'53') not reset after initial selection or selective reset	A4J2	XFF00	QK005	9-140	9-140
	0X11	PRE-TEST. Set abort and intervention required bits in CASNSR (Reg X'53')	Invalid CASNSR	A4J2	XFF00	QK005	9-140	Rerun Rtn X434 and X435
X44A	0X01	Selective reset after No-op command and initial status presented	Invalid in-tags in CTDR (Reg X'5B') or invalid CASTR (Reg X'54')	A4N2, A4J2	XFFFF	QF003	9-250 9-160	Expected: 'select-in' only; Mask byte 0=status Mask byte 1=tags in
X44B	0X01	Selective reset after No-op command with bad parity and status presented	Invalid in-tags in CTDR (Reg X'5B') or invalid CASNSR (Reg X'53')	A4N2, A4J2	XFFFF	QF003	9-250 9-140	Expected: 'select-in' only; Mask byte 0=status Mask byte 1=tags in
	0X11	PRE-TEST. Present status after No-op command with bad parity	Invalid CASNSR (Reg X'53') or no Level 1 interrupt	A4J2	XFFFF	QK004	9-500	Expected: Bus-out check and equipment check bits. Rerun Rtn X436.
	0X12	PRE-TEST. Present status after No-op command with bad parity	Invalid CASTR (Reg X'54') or invalid CTDR (Reg X'5B')	A4J2	XFFFF	QK004	9-160 9-250	Expected: UC and CE and DE stat (byte 0 and 'op-in' and 'st in' tags (byte 1). Rerun Rtn X436.
X44C	0X01	Selective reset after an invalid command and status	Invalid in-tags in CTDR (Reg X'5B') or invalid CASNSR	A4N2, A4J2	XFFFF	QF003	9-350 9-140	Expected: 'select-in' only;

ROUT.	ERROR CODE	FUNCTION TESTED presented	ERROR DESCRIPTION (Reg X'53')	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETCH PAGE	COMMENTS
								Mask byte 0=Sense Mask byte 1=tags in
	0X11	PRE-TEST. Present status after invalid command	Invalid CASNSR (Reg X'53') or invalid CASTR (Reg X'54')	A4J2, A4K2	XFFFF	QK003	9-160	Expected: Command reject bit in sense (byte 0) and UC status (byte 1). Rerun Rtn X43?
X44D	0X01	Sense command test, part 1: initial selection through raising 'service-out'	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-320	Expected: 'op-in' only
	0X11	PRE-TEST. Set intervention required in CASNSR (Reg X'53')	Invalid CASNSR	A4J2	XFF00	QK003	9-320	Expected: Intervention required bit. Rerun Rtn X434
	0X12	PRE-TEST. Set Intervention Required in CASNSR (Reg X'53')	Invalid CASNSR or invalid CASTR (Reg X'54')	A4J2	XFFFF	QK003	9-320	Expected: Intervention required bit in sense (byte 0) Rerun Rtn X434
	0X13	PRE-TEST. Tag check after dropping 'command-out'	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-320	Expected: 'op-in' a and 'status-in'. Rerun Rtn X41F
X44E	0X01	Sense command test, part 2: initial selection through dropping 'service-out'	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-320	Expected: 'op-in' a and 'service-in' on
X44F	0X01	Sense command test, part 3: initial selection through raising 'service-out' a second time	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-320	Expected: 'op-in' only
	0X11	PRE-TEST. Rtn X44E procedure	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-320	Expected: 'op-in' and 'service-in'. Rerun Rtn X44E
X450	0X01	Sense command test, part 4: initial selection through dropping 'service-out' second time	Invalid CASTR (Reg X'54') or invalid in-tags in CTDR (Reg X'5B')	A4N2, A4J2	XFFFF	QF003	9-320	Expected:'status--in' and 'op-in' wi CE and DE only; Mask byte 0=status Mask byte 1=in-tags
	0X11	PRE-TEST. Rtn X44E procedure	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-320	Expected: 'op-in' and 'service-in'. Rerun Rtn X44E.
	0X12	PRE-TEST. Rtn X44F procedure	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-320	Expected: 'op-in'. Rerun Rtn X44F
X451	0X01	Sense command test, part 5: initial selection through dropping 'sel/hold-out'	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-320	Expected:'status-in' and 'op-in' onl
	0X11	PRE-TEST. Rtn X44E procedure	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-320	Expected: 'op-in' and 'service-in'. Rerun Rtn X44E
	0X12	PRE-TEST. Rtn X44F procedure	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-320	Expected: 'op-in'. Rerun Rtn X44F
	0X13	PRE-TEST. Rtn X450 procedure	Invalid in-tags in CTDR (Reg X'5B')	A4N2, A4J2	X00FF	QF003	9-320	Expected: 'op-in' and 'status-in'. Rerun Rtn X450
X452	0X01	Sense command test, part 6: initial selection through raising 'service-out' a third	In-tags not all zero in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-320	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		time						
	0X11	PRE-TEST. Rtn X44E procedure	Invalid in-tags in CTDR (Reg X'5B')	A4M2	X00FF	QF003	9-320	Expected: 'op-in' and 'service-in'. Rerun Rtn X44E
	0X12	PRE-TEST. Rtn X44F procedure	Invalid in-tags in CTDR (Reg X'5B')	A4M2	X00FF	QF002	9-320	Expected: 'op-in'. Rerun Rtn X44F
	0X13	PRE-TEST. Rtn X450 procedure	Invalid in-tags in CTDR (Reg X'5B')	A4M2, A4J2	X00FF	QF003	9-320	Expected: 'op-in' and 'status-in'. Rerun Rtn X450
	0X14	PRE-TEST. Rtn X451 procedure	Invalid in-tags in CTDR (Reg X'5B')	A4M2	X00FF	QF003	9-320	Expected: 'op-in' and 'status-in'. Rerun Rtn X451
X453	0X01	Sense command test, part 7: initial selection through dropping 'service-out' a third time	In-tags not all zero in CTDR (Reg X'5B')	A4M2	X00FF	QF003	9-320	
	0X11	PRE-TEST. Rtn X44E procedure.	Invalid in-tags in CTDR (Reg X'5B')	A4M2	X00FF	QF003	9-320	Expected: 'op-in' and 'service-in'. Rerun Rtn X44E.
	0X12	PRE-TEST. Rtn X44F procedure	Invalid in-tags in CTDR (Reg X'5B')	A4M2	X00FF	QF002	9-320	Expected: 'op-in'. Rerun Rtn X44F
	0X13	PRE-TEST. Rtn X451 procedure	Invalid in-tags in CTDR (Reg X'5B')	A4M2	X00FF	QF003	9-320	Expected: 'op-in' and 'status-in'. Rerun Rtn X451
	0X14	PRE-TEST. Rtn X452 procedure	Invalid in-tags in CTDR (Reg X'5B')	A4M2	X00FF	QF003	9-320	Expected: no in-tags. Rerun Rtn X452
X454	0X01	CWCNT (Reg X'52') loading	CWCNT (Reg X'52') did not load X'03FF'(18 Bit) or X'00FF'(20 Bit)	A4L2	X03FF	QH002	9-130	
	0X02	CWCNT (Reg X'52') loading	CWCNT (Reg X'52') did not load X'0000'	A4L2	X03FF	QH002	9-130	
	0X03	CWCNT (Reg X'52') loading	CWCNT (Reg X'52') did not load X'02AA'(18 Bit) or X'00AA'(20 Bit)	A4L2	X03FF	QH002	9-130	
	0X04	CWCNT (Reg X'52') loading	CWCNT (Reg X'52') did not load X'0155'(18 Bit) or X'0055'(20 Bit)	A4L2	X03FF	QH002	9-130	
X455	0X01	OUTCWAR (Reg X'51') during channel Read command	OUTCWAR did not increment by 4 on a control word fetch	A4M2	XFFFF	QG003	9-430	
X456	0X01	INCWAR (Reg X'50') during Write command	INCWAR (Reg X'50') did not increment by 4 after control word fetch	A4M2	XFFFF	QG001	9-340	
X457	0X01	IN CW bit in CMDR (Reg X'5C' bit 0.2) during channel Write command	IN CW bit and/or channel Write command bit not found in CMDR (Reg X'5C' bits 1.2 and 0.1)	A4L2, A4M2	XFFF0	QH005	9-390	
X458	0X01	CSAR (Reg X'59') during Channel Write command with address of all ones	CSAR (Reg X'59') failed to set to all ones	A4H2, A4G2	XFFFE	QL005	9-400	Byte 0 and 1 only; byte 0 = A4H2; byte 1= A4G2
	0X02	CSAR (Reg X'59') during Write command with address of all zeros	CSAR (Reg X'59') failed to set to all zeros	A4H2, A4G2	XFFFE	QL005	9-400	Byte 0 and 1 only; byte 0 = A4H2; byte 1 = A4G2
	0X03	CSAR (Reg X'59') during Write command with address of X'AAAA'	CSAR (Reg X'59') failed to set to X'AAAA'	A4H2,A4G2	XFFFE	QL005	9-400	Byte 0 and 1 only; byte 0= A4H2; byte 1 = A4G2

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X04	CSAR (Reg X'59') during Write command with address of X'5554'	CSAR (Reg X'59') failed to set to X'5554'	A4H2, A4G2	XFFFE	QL005	9-400	Byte 0 and 1 only: byte 0 = A4H2; byte 1= A4G2
X459	0X01	CSAR (Reg X'59') during Write command with address of X'30000'	Byte X failure in CSAR (Reg X'58') 18 Bit (Reg X'53') 20 Bit	A4M2 A4T2(Mod J,K,L)	X0003	QG004 QB001	9-400	
	0X02	CSAR (Reg X'59') during Write command with address of X'00000'	Byte X failure in CSAR (Reg X'58') 18 Bit (Reg X'53') 20 Bit	A4M2 A4T2(Mod J,K,L)	X0003	QG004 QB001	9-400	
	0X03	CSAR (Reg X'59') during Write command with address of X'20000'	Byte X failure in CSAR (Reg X'58') 18 Bit (Reg X'53') 20 Bit	A4M2 A4T2(Mod J,K,L)	X0003	QG004 QB001	9-400	
	0X04	CSAR (Reg X'59') during Write command with address of X'10000'	Byte X failure in CSAR (Reg X'58') 18 Bit (Reg X'53') 20 Bit	A4M2 A4T2(Mod J,K,L)	X0003	QG004 QB001	9-400	
	0X05	CSAR (Reg X'59') during Write command with address of actual storage	Byte X failure in CSAR (Reg X'58') 18 Bit (Reg X'53') 20 Bit	A4M2 A4T2(Mod J,K,L)	X0003	QG004 QB001	9-400	
X45A	0X01	Initial status to sense command after setting sense prep unit exception	In-tags invalid in CTDR (Reg X'5B')	A4N2	XFFFF	QF003	9-250	Exp: op-in & sel/hold & status in
	0X02	Initial status to sense command after setting sense prep unit exception	Invalid status in CASTR (Reg X'54' byte 0)	A4J2	XFF00	QK002	9-170	Exp: Unit exception status
	0X03	Test Reset of CASTR(Reg X'54')	CASTR did not reset after the ending sequence	A4J2	XFF00	QK002		Exp: zero status
	0X04	Tag sequence, Sense UE latch on	In-tags invalid in CTDR (Reg X'5B')	A4N2	X0010	QF003		Exp: Addr.in drop
	0X05	Check for initial status	Invalid status in CASTR (Reg X'54' Byte 0)	A4J2	XFF00	QK002		Exp: Zero status
	0X06	Tag sequence	In-tags invalid in CTDR (Reg x'5B')	A4N2	X0008	QF003		Exp: status in up
	0X07	Tag sequence after raising service out	In-tags invalid in CTDR (Reg x'5B')	A4N2	X0008	QF003		Exp: status drop
	0X08	Tag sequence after dropping service out	In-tags invalid in CTDR (Reg x'5B')	A4N2	X0004	QF003		Exp: serv in up
	0X09	Tag sequence after raising service out	In-tags invalid in CTDR (Reg x'5B')	A4N2	X0004	QF003		Exp: serv drop
	0X0A	Check for final status	Invalid status in CASTR (Reg x'54')	A4J2	XFF04	QK002		Exp: CE,DE,UE
	0X0B	End sequence drop service out	In-tags invalid in CTDR (Reg x'5B')	A4N2	X0008	QF003		Exp: status in up
	0X0C	End sequence raise service out	In-tags invalid in CTDR (Reg x'5B')	A4N2	X0008	QF003		Exp: status in drop
	0X0D	End sequence drop sel out,svc out	In-tags invalid in CTDR (Reg x'5B')	A4N2	X0020	QF003		Exp: Op In drop
	0X0E	Reset Sense UE latch	Invalid status in CASTR (Reg X'54)	A4J2	XFF00	QK002		Exp: CE,DE
	0X0F	Set both latches on and verify IPL UE (Reg X'54) has precedence	Invalid status in CASTR	A4J2	XFF00	QK002		Exp: UF or
	0X11	PRE-TEST Reset of CASTR (Reg X'54')	CASTR did not reset from CA reset	A4J2	XFF00	QK002	9-170	
X45D	0X01	OUT CW bit in CMDR (Reg	Out CW bit and/or Read command	A4L2	XF0F0	QB005	9-440	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		X'5C' bit 1.0) during Read command	bit not found in CMDR (Reg X'5C' bits 1.0 and 0.2)					
X45E	0X01	Check Out Stop CW bit in CMDR (Reg X'5C' bit 0.1) during Read command	Out Stop CW bit and/or Read command bit not found in CMDR (Reg X'5C' bits 1.1 and 0.2)	A4L2	XF0F0	QH005	9-440	
X460	0X01	TIC CW bit in CMDR (Reg X'5C' bit 1.3) during write fetch	'Address in' INCWAR (Reg X'50') does not match address of CW to which TIC points	A4L2, A4M2	XFFFF	QH001	9-440	
X461	0X01	Chain bit in INCWAR (Reg X'50' bit 0.3) sets Valid latch in CACRS (Reg X'55' bit 0.2)	Chain bit in CW did not set valid latch	A4L2	X2000	QH005	9-440	
	0X02	No chain bit in INCWAR resets valid latch in CACRS	No chain bit in CW did not reset valid latch	A4L2	X2000	QH005	9-440	
X462	0X01	Chain bit in OUTCWAR (Reg X'51' bit 0.3) sets valid latch in CACRS (Reg X'55' bit 0.3)	Chain bit in CW did not set valid latch	A4L2	X1000	QH005	9-440	
	0X02	No chain bit in OUTCWAR resets valid latch in CACRS	No chain bit in CW did not reset valid latch	A4L2	X1000	QH005	9-440	
X463	0X01	Chain bit in Out Stop CW (Reg X'51' bit 0.3) sets valid latch in CACRS (Reg X'55' bit 0.3)	Chain bit in CW did not set valid latch	A4L2	X1000	QH005	9-440	
	0X02	No chain bit in OUTCWAR resets valid latch in CACRS	No chain in CW did not reset valid latch	A4L2	X1000	QH005	9-440	
X464	0X01	Transfer byte bits in CBODR (Reg. X'58' bits 1.2, 1.3) after Read command to 'service-out' is up in response to initial status	Transfer Byte 1 bit not on and/or transfer byte 2 bit not off	A4M2	X0030	QG001	9-440	
X465	0X01	Read 1023 bytes (18 Bits) or 255 Bytes (20 Bits)	CWCNT (Reg X'52') failed to decrement properly	A4L2	X03FF	QH002	9-440	CSAR (Reg X'59') contains failing address
	0X11	PRE-TEST. Chain bit in OUTCWAR (Reg X'51' bit 0.3) sets valid latch in CACRS (Reg X'55' bit 0.3)	Invalid CACRS (Reg X'55')	A4L2	X3000	QH005	9-440	Rerun Rtn X462
X466	0X01	Access all valid addresses with CSAR (Reg X'59')	CSAR (Reg X'59') did not properly increment +2 from last data fetch	A4F2, A4M2	3FFFF or 7FFFF	QN005	9-440	18 Bit 20 Bit
	0X11	PRE-TEST. Increment of CSAR (Reg X'59') after Out-CW fetch	CSAR did not increment	A4M2	3FFFF or 7FFFF	QG003	9-440	18 Bit 20 Bit
X467	0X01	Cycle steal from data address of progressive ones	Invalid address pattern in CSAR (Reg X'59')	A4M2,A4H2, A4G2	3FFFF or FFFFF	QL004	9-440	18 Bit Byte X =A4M2 Byte 0 =A4H2 20 Bit Byte 1 =A4G2
	0X02	Cycle steal from data address of floating zeros	Invalid address pattern in CSAR (Reg X'59')	A4M2,A4H2, A4G2	3FFFF or FFFFF	QL004	9-440	18 and 20 Bit Same as Above

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETEM PAGE	COMMENTS
X468	0X01	Fetch Out CW with flags = X'00'	Invalid CASTR (Reg X'54')	A4J2	XFF00	QK002	9-440	Only CE expected
	0X02	Fetch Out CW with flags = X'00'	Level 3 interrupt did not occur	A4F2, A4K2	X1000	QJ001	9-440	
X469	0X01	Fetch Out CW with flags = X'01'	Invalid CASTR (Reg X'54')	A4L2	XFF00	QK002	9-440	
	0X02	Fetch Out CW with flags = X'01'	Level 3 interrupt did not occur	A4F2, A4K2	X0010	QJ001	9-440	
	0X03	Fetch Out CW with flags = X'01'	Chaining to next CW failed	A4L2	X5104	QH005	9-440	
	0X04	Fetch Out CW with flags = X'01'	Invalid CACRS (Reg X'55') prior data transfer	A4L2	X51F4	QK002	9-440	
	0X05	Fetch Out CW with flags = X'11'	Invalid CASTR (Reg X'54')	A4L2	XFF00	QK002	9-440	
	0X06	Fetch Out CW with flags = X'11'	Level 3 interrupt did not occur	A4F2, A4K2	X0010	QJ001	9-440	
	0X07	Fetch Out CW with flags = X'11'	Chaining to next CW failed	A4L2	X5104	QH005	9-440	
	0X08	Fetch Out CW with flags = X'11'	Invalid CACRS (Reg X'55') prior data transfer	A4L2	XFF00	QK002	9-440	
X46A	0X01	Zero Ct Override bit in CACR (Reg X'55' bit 0.1)	Override bit not on with flag bits = X'10' during CW fetch	A4L2	X4000	QH005	9-440	
	0X02	Zero Ct Override bit in CACR (Reg X'55' bit 0.1)	Override bit on with flag bits = X'00' during CW fetch	A4L2	X4000	QH005	9-440	
X46B	0X01	Out CW with flag = '10'	Zero ccunt override bit did not cause Level 3 interrupt	A4K2, A4L2	X0010	QJ001	9-440	
	0X02	Out CW with flag = '10'	CASTR (Reg X'54') not set to all zeros by zero count override bit	A4J2, A4L2	XFF00	QK002	9-440	
X46C	0X01	Out Stop CW with flag = '00'	No Level 3 interrupt or CE status only not in CASTR (Reg X'54')	A4L2,A4K2, A4J2	XFF0F	QH005	9-440	Status = byte 0; Level 3 interrupt Byte 1
	0X02	Out Stop CW with flag = '10'	No Level 3 interrupt or CASTR (Reg X'54') not set to all zeros	A4L2,A4K2,	XFF0F	QH005	9-440	Status = Byte 0; Level 3 interrupt Byte 1
X46D	0X01	Out Stop CW with flag = '01'	Level 3 interrupt or CASTR (Reg X'54') not having CE + DE status only	A4L2,A4K2, A4J2	XFF01	QH005	9-440	Status = Byte 0; Level 3 interrupt Byte 1
	0X02	Out Stop CW with flag = '11'	No Level 3 interrupt or CASTR (Reg X'54') not set to all zeros	A4L2,A4K2, A4J2	XFF01	QH005	9-440	Status = Byte 0; Level 3 interrupt Byte 1
X46E	0X01	In CW with flag = '00'	No Level 3 interrupt or CASTR (Reg X'54') not having CE only status	A4L2,A4K2, A4J2	XFF01	QH005	9-440	Status = Byte 0; Level 3 interrupt Byte 1
X46F	0X01	In CW with flag = '01'	Level 3 interrupt or CASTR (Reg X'54') not set to all zeros	A4L2,A4K2, A4J2	XFF01	QH005	9-440	Status = Byte 0; level 3 interrupt Byte 1
	0X02	In CW with flag = '11'	No Level 3 interrupt or CASTR (Reg X'54') not set to all zeros	A4L2,A4K2, A4J2	XFF01	QH005	9-440	Status = Byte 0; Level 3 interrupt Byte 1
	0X03	INCWAR address=zero	INCWAR address not zero	A4L2,A4K2, A4J2	XFFFF	QH005	9-440	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETHR PAGE	COMMENTS
X470	0X01	In CW with flag = '10'	No Level 3 interrupt or CASTR (Reg X'54') not set to all zeros	A4L2,A4K2, A4J2	XFF01	QH005	9-440	Status = Byte 0; Level 3 interrupt = Byte 1
X471	XXXX	Verify that the CUC increments on cycle steal cycles	This test verifies proper incrementing of the CUC from cycle steal cycles by the adapter under test. CUC value represents a combination of cycle steal and instruction cycles. CCU operation of the CUC for I1, I2 and I3 cycles has been verified in the CCU diagnostic routines.					
X471	0X01	Verify that the CUC increments on cycle steal cycles	CUC value is not correct after cycle steal operation. Reg X'14' = Actual CUC value Reg X'15' = Bits in error Reg X'16' = exp'd. CUC value If a cycle steal error has previously occurred in the adapter under test, this test is invalid. If no previous errors have occurred, then error is in the CUC area of the CCU.	1AB4		CW001		
X472	0X01	Read with Out Stop CW with chain bit on, part 1	Invalid CTDR (Reg X'5B') after reading 2 bytes	A4N2	X00FF	QF003	9-440	'Status-in' and 'op-in' only expected
X473	0X01	Read with Out Stop CW with Chain bit on, part 2	Invalid CTDR (Reg X'5B') after bringing up 'service-out'	A4N2	X00FF	QF003	9-440	'Op-in' only expected
X474	0X01	Read with Out Stop CW with Chain bit on, part 3	Invalid CTDR (Reg X'5B') after ending status accepted	A4N2	X00FF	QF003	9-440	No in-tags expected
	0X11	PRE-TEST. Rtn X473 procedure	Invalid in-tags in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-440	Expected: 'op-in' only Rerun Rtn X473
X476	0X01	Chain 2 Read commands	Invalid CTDR (Reg X'5B') after suppress-out came up	A4N2	X00FF	QF003	9-270	
	0X02	Chain 2 Read commands	Chain bit in CACRS (Reg X'55' bit 1.0) set after Level 3 interrupt	A4N2	X0080	QF004	9-270 9-440	
X477	0X01	Chain 2 Read commands and end operation with chaining indicated	Chain bit in CACRS (Reg X'55' bit 1.0) not set	A4N2	X0080	QF004	9-270 9-440	
	0X02	Issue Read command again without chaining	Chain bit in CACRS (Reg X'55' bit 1.0) set	A4N2	X0080	QF004	9-440	
X479	0X01	Issue Read command and fetch TIC CW with address above 64K	Invalid CWAR address bit in CACHKR (Reg X'56' bit 0.0) did not set during level 1 interrupt or a level 1 interrupt did not occur	A4F2	X8020	QW002	9-440	Mask byte 0=CACHKR Mask byte 1=level 1 interrupt
	0X11	PRE-TEST. Initial status after Read command and fetch of TIC CW.	Invalid response in CTDR (Reg X'5B') or CASTR	A4N2	XFFFF	QF003	9-440	Expected: no status (byte 0), 'op-in' and 'status-in' (byte 1)
X47A	0X01	Issue Read command and fetch an In-type CW	Invalid CW Format bit in CACHKR (Reg X'56' bit 0.1) did not set during level 1 interrupt or level 1 interrupt did not occur	A4F2	X4020	QW002	9-440	Mask byte 0=CACHKR Mask byte 1=level 1 interrupt

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X02	Issue Read command and fetch an In-type CW	Invalid response in CASTR (Reg X'54')	A4L2	XFF00	QH002	9-440	Expected:CE, DE, and UC status
	0X03	Issue Read command and fetch an In-type CW	Invalid response in CASNSR (Reg X'53')	A4J2	X4000	QK005	9-400	Expected: Intervention required
X47B	0X01	Issue Write command and fetch an Out-type CW	Invalid CW Format bit in CACHKR (Reg X'56' bit 0.1) not set during level 1 interrupt or level 1 interrupt did not occur	A4F2	X4020	QN002	9-400	CACHKR = Byte 0 Level 1 interrupt = Byte 1 of mask
	0X02	Issue Write command and fetch an Out-type CW	Invalid response in CASTR (Reg X'54')	A4L2	XFF00	QH002	9-400	Expected: CE, DE, and UC status
	0X03	Issue Write command and fetch an Out-type CW	Invalid response in CASNSR (Reg X'53')	A4J2	X4000	QK005	9-400	Expected: Intervention required
X47C	0X01	Issue Read command and fetch CW with address of X'3FFFF'	Data address error bit in CACHKR (Reg X'56' bit 0.2) did not set during level 1 interrupt or level 1 interrupt did not occur	A4F2	X2040	QN002	9-440	Mask byte 0=CACHKR Mask byte 1=level 1 interrupt
X47D	0X01	Issue Read command; set abort bit after servicing initial status	Invalid CASNSR (Reg X'53') or invalid CASTR (Reg X'54')	A4J2	XFFFF	QK005	9-440	Expected; Abort bit and CE, DE, and UC; Mask byte 0=Sense Mask byte 1=Status
	0X02	Issue Read command; set abort bit after servicing initial status	Invalid CACRS (Reg X'55')	A4J2	X0700	QK005	9-440	Expected: CWAR valid bit reset; abort bit set
	0X03	Issue Read command; set abort bit after servicing initial status	Level 3 interrupt did not occur	A4K2	XXXXX	QJ001	9-440	
X47E	0X01	Halt I/O during Read command	Invalid in-tags in CTDR (Reg X'5B')	A4H2	X00FF	QJ004	9-480	Expected: 'request-in'
	0X02	Halt I/O during Read command	Invalid CASTR (Reg. X'54')	A4J2	XFF00	QK002	9-480	Expected: CE status
X47F	0X01	Cycle steal from data address of degressive ones	Invalid address pattern in CSAR (Reg X'59')	A4H2,A4H2 A4G2	3FFFF or FFFFF	QL004	9-230	18 Bit Byte X = A4H2 Byte 0 = A4H2 20 BIT Byte 1 = A4G2
	0X02	Cycle steal from data address of floating zero	Invalid address pattern in CSAR	A4H2,A4H2, A4G2	3FFFF	QL004	9-230	Same as above
	0X11	PRE-TEST. Valid address in CSAR (Reg X'59') from degressive ones address	Invalid CSAR	A4F2, A4H2	3FFFF or FFFFF	QN005		18 Bit Rerun Rtn X466 20 Bit
	0X12	PRE-TEST. Valid address in CSAR (Reg X'59') from floating zero address	Invalid CSAR	A4F2, A4H2	3FFFF or FFFFF	QN005		18 Bit Rerun Rtn X466 20 Bit
	0X13	PRE-TEST. CWCNT (Reg X'52')	CWCNT not = 2	A4L2	X03FF or X00FF	QH002		18 Bit Rerun Rtn X45B 20 Bit
	0X14	PRE-TEST. Read 2 bytes	Invalid response in CTDR (Reg. X'5B')	A4H2	X00FF	QF003		Expected 'op-in' an 'service-in'. Rerun Rtn. X472
	0X15	PRE-TEST. Read 2 bytes & raise 'service-out'	CWCNT not=1	A4L2	X03FF or X00FF	QH002		18 Bit Rerun Rtn X465 20 Bit

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X480	0X01	No duplication of next to last byte after issue of Write command with odd byte count	Invalid CASTR (Reg X'54')	A4J2	XFF00	QK002	9-390	Expected: CE status
	0X02	Same as above	First 2 bytes not written	A4L2	XFFFF	QH002	9-390	
	0X03	Same as above	Last 2 bytes incorrect	A4L2	XFFFF	QH002	9-390	
X481	0X01	Transfer byte bits in CBODR (Reg X'58' bits 1.2, 1.3) after read command and transferring one byte	Transfer byte 1 bit not off and/or transfer byte 2 bit not on	A4M2	X0030	QG001		
	0X11	PRE-TEST. Rtn X464 procedure	Transfer byte 1 bit not on and/or transfer byte 2 bit not off	A4M2	X0030			Rerun Rtn X464
X482	0X01	CTDR (Reg X'5B') after Halt I/O during Read command after transferring one byte of data	Invalid response in CTDR	A4N2	X00FF	QF004	9-430	Expected: 'request-in' only
	0X02	CTDR (Reg X'5B') after Halt I/O during Write command after transferring one byte of data	Invalid response in CTDR	A4N2	X00FF	QF004	9-390	Expected: 'request-in' only
	0X03	CASTR (Reg X'54') after Halt I/O during Read command after transferring one byte of data	Invalid response in CASTR	A4J2	XFF00	QK002	9-430	Expected: CE status only
	0X04	CASTR (Reg X'54') after Halt I/O during Write command after transferring one byte of data	Invalid response in CASTR	A4J2	XFF00	QK002	9-390	Expected: CE status only
	0X05	CWCNT (Reg X'52') after Halt I/O during Read command after transferring one byte of data	Invalid count in CWCNT	A4L2	XFFFF	QH002	9-430	Expected: count=1
	0X06	CWCNT (Reg X'52') after Halt I/O during Write command after transferring one byte of data	Invalid count in CWCNT	A4L2	XFFFF	QH002	9-390	Expected: count=1
X483	0X01	CTDR (Reg X'5B') after Halt I/O during Read command after even byte transfer	Invalid response in CTDR	A4N2	X00FF	QF004	9-430	Expected: 'request-in' only
	0X02	CASTR (Reg X'54') after Halt I/O during Read command after even byte transfer	Invalid response in CASTR	A4J2	XFF00	QK002	9-430	Expected: CE status only
	0X03	No level 3 interrupt after Halt I/O during Read command after even byte transfer	Unexpected level 3 interrupt before accepting status	A4K2	X1000	QJ001	9-430	
	0X04	CTDR (Reg X'5B') after Halt I/O during Write command after even byte transfer	Invalid response in CTDR	A4N2	X00FF	QF004	9-390	Expected: 'request-in' only
	0X05	CASTR (Reg X'54') after Halt I/O during Write command after even byte transfer	Invalid response in CASTR	A4J2	XFF00	QK002	9-390	Expected: CE status only
	0X06	No level 3 interrupt after Halt I/O during Write command after even byte transfer	Unexpected Level 3 interrupt occurred	A4K2	X1000	QJ001	9-390	
X484	0X01	CTDR (Reg X'5B') after Halt I/O during Read command after first 'service-in'	Invalid response in CTDR	A4N2	X00FF	QF004	9-430	Expected: 'request-in' only
	0X02	CASTR (Reg X'5B') after Halt I/O during Read command after first 'service-in'	Invalid response in CASTR	A4J2	XFF00	QK002	9-430	Expected: CE status only
	0X03	No Level 3 interrupt after Halt I/O during Read command after first 'service-in'	Unexpected level 3 interrupt before accepting status	A4K2	X1000	QJ001	9-430	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0X04	CTDR (Reg X'5B') after Halt I/O during Write command after first 'service-in'	Invalid response in CTDR	A4N2	X00FF	QF004	9-390	Expected: 'request-in' only
	0X05	CASTR (Reg X'5B') after Halt I/O during Write command after first 'service-in'	Invalid response in CASTR	A4J2	XFF00	QK002	9-390	Expected: CE status only
	0X06	No level 3 interrupt after Halt I/O during Write command after first 'service-in'	Unexpected Level 3 interrupt	A4K2	X1000	QJ001	9-390	
X485	0X01	CASTR (Reg X'54') after program abort during Read command after first 'service-in'	Invalid response in CASTR	A4J2	XFF00	QK002	9-430	Expected: CE, DE, and UC status
	0X02	CASNSR (Reg X'53') after program abort during Read command after first 'service-in'	Invalid CASNSR	A4J2	XFF00	QK003	9-430	Expected: Abort sense bit
	0X03	CASTR (Reg X'54') after program abort during Write command after first 'service-in'	Invalid response in CASTR	A4J2	XFF00	QK002	9-390	Expected: CE, DE, and UC status
	0X04	CASNSR (Reg X'53') after program abort during Write command after first 'service-in'	Invalid CASNSR	A4J2	XFF00	QK003	9-390	Expected: Abort sense bit
	0X08	CACRS (Reg X'55') after program abort during write command after first 'service-in'	Invalid CACRS	A4L2	X0400	QH006	9-390	Expected: Program requested abort bit
X486	0X01	CACRS (Reg X'55') after program abort with CA inactive.	Invalid CACRS or no level 3 interrupt.	A4L2	X0400	QH006	9-390	Expected: Program requested abort bit & level 3 interrupt.
X487	0X01	Attention status in CASTR (Reg X'54') after setting program attention bit in CACR (Reg X'55' bit 0.2)	Invalid response in CASTR	A4J2	XFF00	QK002	9-170	Expected: Attention status only
	0X02	Zero sense in CASNSR (Reg X'53') after setting Program Attention bit in CACR (Reg X'55' bit 0.2)	Invalid response in CASNSR	A4J2	XFF00	QK003	9-150	
	0X11	PRE-TEST. Reset CASTR (Reg X'54') and CASNSR (Reg X'53')	CASTR or CASNSR did not reset	A4J2	XFFFF	QK002	9-150 9-170	
X488	0X01	Busy status after initial selection with Intervention Required bit set in CASNSR (Reg X'53')	Invalid status in CASTR (Reg X'54')	A4J2	XFF00	QK002	9-150	Expected: CE, DE, UC, and Busy status
X4XX	1X01	SUBR-TEST. Configuration data	Invalid configuration data		XXXXX			Check Configuration Data Set (CDS).
	1X02	SUBR-TEST. Storage size in Reg X'70'	Invalid storage size in Reg X'70'		XXXXX			CDS may be incorrect.
	1X03	SUBR-TEST. Set diagnostic mode	Diagnostic mode not set in CACR (Reg X'55' bit 0.0)	A4L2	X8000	QH006	9-210	Run Rtn X402
	1X04	SUBR-TEST. Initial selection: 'op-out', 'address-out', and 'sel/hold-out'	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-250	Run Rtn X40E
	1X05	SUBR-TEST. Adr-in during	Invalid response in CTDR	A4N2	X00FF	QF003	9-250	Run Rtn X411

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		initial selection						
	1X06	SUBR-TEST. Adr-in dropped after 'command-out' during initial selection	Adr-in bit in CTDR (Reg X'5B') did not drop	A4N2	X0010	QF003	9-250	Run Rtn X415
	1X07	SUBR-TEST. Selective/system reset bit in CACR (Reg X'55' bit 1.3) off	Selective/system reset bit in CACR on	A4N2	X0010	QF005	9-190	Run Rtn X412
	1X08	SUBR-TEST. Selective/system reset	Selective/system reset bit in CACR (Reg X'55' bit 1.3) did not reset or level 3 interrupt did not occur	A4N2	X0010	QF005	9-190	Run Rtn X412
	1X09	SUBR-TEST. Selective/system reset	Selective/system reset bit in CACR (Reg X'55' bit 1.3) did not reset after level 3 interrupt	A4N2	X0010	QF006	9-190	Run Rtn X412
	1X0A	SUBR-TEST. Selective/system reset	Invalid CTDR (Reg X'5B') after selective/system reset	A4N2	X0020	QF003	9-250	Run Rtn X41E
	1X0B	SUBR-TEST. Dropping 'command-out' during initial selection	'Op-in' and 'status-in' not set in CTDR (Reg X'5B')	A4N2	X0028	QF003	9-250	Run Rtn X41F
	1X0C	SUBR-TEST. Status after dropping 'command-out' during initial selection	Invalid status in CASTR (Reg X'54')	A4J2	XFF00	QK001	9-170	Run Rtn X420
	1X0D	SUBR-TEST. Status after dropping 'command-out' during initial selection with No-op command	Invalid status in CASTR (Reg. X'54')	A4J2	XFF00	QK002	9-170	Run Rtn X421
	1X0E	SUBR-TEST. Initial selection and status stacked	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Run Rtn X42A
	1X0F	SUBR-TEST. Accept initial status	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	Run Rtn X425
	1X10	SUBR-TEST. Stack initial status	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF004	9-250	Run Rtn X42B
	1X11	SUBR-TEST. Drop 'command-out' during present stacked status	Invalid response in CTDR (Reg X'5B')	A4N2	XFFFF	QF003	9-250	Run Rtn X41F
	1X12	SUBR-TEST. Raise 'command-out' during present stacked status	Invalid response in CTDR (Reg X'5B')	A4N2	XFFFF	QF004	9-250	Run Rtn X42A
	1X13	SUBR-TEST. Drop 'command-out' during present stacked status	Invalid response in CTDR (Reg X'5B')	A4N2	XFFFF	QF004	9-250	Run Rtn X42B
	1X14	SUBR-TEST. Raise 'sel/hold-out' during present stacked status	Invalid response in CTDR (Reg X'5B')	A4N2	XFFFF	QF004	9-250	Run Rtn X42F
	1X15	SUBR-TEST. Raise 'command-out' during present stacked status	Invalid response in CTDR (Reg X'5B')	A4N2	XFFFF	QF004	9-250	Run Rtn X430
	1X16	SUBR-TEST. Drop 'command-out' during present stacked status	Invalid response in CTDR (Reg X'5B')	A4N2	XFFFF	QF004	9-250	Run Rtn X431
	1X17	SUBR-TEST. Drop 'sel/hold-out' during present stacked status	Invalid response in CTDR (Reg. X'5B')	A4N2	XFFFF	QF004	9-250	Run Rtn X431
	1X18	SUBR-TEST. 'Command-out' up during initial selection	CASTR (Reg X'54') or CASNSR (Reg X'53') not reset	A4J2	XFFFF	QK002	9-250	Run Rtn X421
	1X19	SUBR-TEST. Drop 'command-out' during initial selection	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	Run Rtn X41F
	1X1A	SUBR-TEST. Raise 'service-out' during initial selection	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF003	9-250	Run Rtn X425
	1X1B	SUBR-TEST. Drop 'command-out' during initial selection	Invalid response in CTDR (Reg X'5B')	A4N2	XFFFF	QF003	9-250	Run Rtn X41F
	1X1C	SUBR-TEST. Raise and drop 'service-out' during initial	Invalid response in CTDR (Reg X'5B')	A4N2	X00FF	QF002	9-250	Run Rtn X426

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		selection						
	1X1D	SUBR-TEST. Set CWAR Valid bits	CWAR valid bits not set in CACR (Reg X'55')	A4L2	X3000	QH005	9-250	Run Rtn X409
	1X1E	SUBR-TEST. Read 2 bytes	Invalid response in CTDR (Reg X'5B') after dropping 'service-out'	A4N2	X00FF	QF003	9-250	Run Rtn X472
	1X1F	SUBR-TEST. Read 2 bytes	Invalid response in CTDR (Reg X'5B') after raising 'service-out'	A4N2	X00FF	QF003	9-250	Run Rtn X473
	1X20	SUBR-TEST. Read 2 bytes and present ending status	Invalid response in CTDR (Reg X'5B') after presenting status	A4N2	X00FF	QF003	9-250	Run Rtn X474
	1X21	SUBR-TEST. Check that proper CA selected.	CA not properly selected		X0003		9-080	Run Rtn X402
	2X12	IPRT-TEST. Level 1 interrupt handling	Unexpected level 1 interrupt from channel adapter 1	A4K2	XXXXX	QJ001	9-500	
	2X13	IRPT-TEST. Level 1 interrupt handling	Unexpected level 1 interrupt from channel adapter 2	A4K2	XXXXX	QJ001	9-500	
	2X14	IRPT-TEST. Level 1 interrupt handling	Level 1 interrupt from wrong channel adapter	A4K2	XXXXX	QJ001	9-500	
	2X15	IRPT-TEST. Level 1 interrupt handling	Level 1 interrupt with no req bit on and not expected	A4K2	XXXXX	QJ001	9-500	
	2X16	IRPT-TEST. Level 1 interrupt handling	Level 1 interrupt expected, but no request bit on	A4K2	XXXXX	QJ001	9-500	
	2X31	IRPT-TEST. Level 3 interrupt handling	Unexpected level 3 interrupt	A4L2	XXXXX	QH001		Run Rtn X401
	2X32	IRPT-TEST. Level 3 interrupt handling	Level 3 interrupt from wrong channel adapter	A4L2	XXXXX	QH001		Run Rtn X401
	2X33	IRPT-TEST. Level 3 interrupt reset bit (Reg X'57' bit 1.3)	Level 3 interrupt did not reset	A4L2	XXXXX	QH001	9-210	

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1502 XXXX This routine checks the integrity of certain necessary data in the configuration data set. It issues no error stops, as such. Instead, it issues manual intervention stops to ensure that positive action is taken to correct the configuration data set. If any of these stops is encountered and the configuration data set is not corrected, the validity and reliability of all routines is in jeopardy. (See the manual intervention codes following the error code listings.) This routine will be run even if the DCM sense switch to include manual intervention routines is not set.

1504 XXXX Normal Static Conditions: Ensure that static conditions are normal after a scanner reset.

1504	0X01	Ensure that after an OUT X'45' with byte 0, bit 2 'scanner on (disable scanner), being CS is reset. resets the	One scanner pass (30 microseconds) after the OUT X'45', an IN X'44' indicated the CS was not reset. Reg. X'15' contains the IN X'44' bits that were in error:		FFFF			Test Since enabled' off
			Byte 0:					
			Bit 0-mode bit 'override' latch failed to reset.	Y4E2		RS104		others, if byte 0, bit 3 is on in error, ignore any others on until it is fixed. Reg. X'14' contains the result of the IN X'44'. Byte 0, bit 3 in error would most likely be caused by a problem in the latch itself or by a failure in power-on reset ("+reset" on ALD page RS105).
			Bit 2-'override remember' latch failed to reset.	Y4E2		RS104		
			Bit 3-'scanner enabled' latch failed to reset.	Y4E2		RS105	A-310	
			Bit 4-'character service pending' latch failed to reset.	Y4E2		RS105	A-210, A-220	
			Byte 1:					
			Bits 2 thru 5-bit clock check for LIBs 1,2,3, or 4 (respectively) failed to reset.	Y4F2		RS206	A-210 A-220	
			Bit 6-'LIB select check' failed to reset.	Y4F2		RS206	A-210, A-220	
			Bit 7-'outbus check' failed to reset.	Y4E2		RS102	A-210, A-220	

1506 XXXX Scanner Enable: Ensure that, after a successful scanner reset, the 'scanner enabled' latch can be set.

1506	0X01	Ensure that, after an OUT X'45' with byte 0, bit 2 on (disable scanner), the CS is reset.	One scanner pass (30 microseconds) after the OUT X'45', an IN X'44' indicated the CS was not reset. Reg. X'15' contains the IN X'44' bits that were in error:		FFFF			Pretest error. Rerun routine 1504. Since 'scanner enabled' being off resets the others, if byte 0, bit 3 is on in error, ignore any others that are on. Reg X'14' contains the results of the IN X'44'.
			Byte 0:					
			Bit 3-'Scanner enabled' latch failed to reset.	Y4E2		RS105	A-310	
			Bit 4-'Character service pending' latch failed to reset.	Y4E2		RS105	A-210, A-220	
			Byte 1:					
			Bits 2 thru 5-Bit clock check for LIBs 1,2,3, or 4 (respectively) failed to reset.	Y4F2		RS206	A-210, A-220	
			Bit 6-'LIB select check' failed to reset.	Y4F2		RS206	A-210, A-220	
			Bit 7-'Outbus check' failed to reset.	Y4E2		RS102	A-210, A-220	
1506	0X02	Ability of the 'scanner enabled' latch to be set by OUT X'45' with byte 0, bit 1 on.	'Scanner enabled' latch failed to set. (IN X'44', byte 0, bit 3).	Y4E2	1000	RS105	A-310	Test error. Reg X'14' contains the results of the IN X'44'.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1508	XXXX	Scanner Disable: Ensure that, after the CS has been enabled, it can again be disabled via OUT X'45'.						
1508	0X01	Ability of the 'scanner enabled' latch to be reset by OUT X'45' with byte 0, bit 2 on.	'Scanner enabled' latch failed to reset. (In X'44', byte 0, bit 3).	Y4E2	1000	RS105	A-310	Test error. Reg. X'14' contains the results of the IN X'44'. This failure is different from error 0X01 in routine 1504 in that the failure is most probably associated with the lines '-output 45' and '-outbus bit 0.2' on ALD page given.
150A	XXXX	Unwanted Level 1 Interrupts WITH LIBs Disabled: The CS is reset and enabled, adapter L1 interrupts unmasked for 30 milliseconds, and a check made to ensure that no level 1 interrupts occur without an error condition up in the CS.						
150A	0X01	If a level 1 interrupt occurred after unmasking, ensure that IN X'76' indicated a "type 1 CS level 1 check".	No indication was given, of which adapter caused the interrupt in IN X'76'.	Y4D2		RA102	6-082	Test error. Failure was most probably "-type 1 CS bid level 1" on ALD page given, failing to bring up "+ input type 1 CS level 1".
150A	0X02	If a level 1 interrupt occurred, ensure that no error conditions were present were present in the CS, before continuing.	A level 1 interrupt has occurred and IN X'44' did indicate an error condition. Reg. X'15' contains the error condition bits that were on in the IN X'44': Byte 1:		003F		A-210	Test error. Rerun routines 1504 thru 1508, since this error condition should have occurred in an
			Bits 2 thru 5-bit clock check for LIBs 1,2,3, or 4 (respectively).	Y4F2		RS206	A-210, A-220	earlier routine. Trouble is possibly
			Bit 6-LIB select check	Y4F2		RS206	A-210, A-220	intermittent. Reg. X'14'
			Bit 7-outbus check	Y4E2		RS102	A-210, A-220	contains the results of the IN X'44'.
150A	0X03	Ensure that no level 1 interrupts occur without an error condition in the CS.	A level 1 interrupt has occurred indicating that a bid for level 1 was present without any of the error conditions being present in IN X'44'.	Y4F2 Y4D2		RS206 RA102	6-082	Test error. If error code 0X02 in this routine occurred, this error stop will always occur.
150C	XXXX	Outbus Parity Error Detector: Ensure the validity and proper operation of the outbus parity error detection circuitry by forcing bad parity on the outbus (via OUT X'78') with various data patterns and ensuring that an outbus parity error does occur. Thirty-four passes through the routine are made, with different data, as follows: 1. All 16 bits off. 2. High-order bit on and then shifted right each pass until the low-order bit is on. 3. The two high-order bits on and shifted right each pass until the two low-order bits are on. 4. All 16 bits on. In addition, after forcing an outbus check, a check is made to ensure that it can be reset.						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
150C	0X01	Before continuing the test, ensure that no level 1 interrupts are already pending.	After unmasking adapter level 1 interrupts, a level one interrupt occurred. Reg. X'14' indicates the cause of the interrupt: Byte 1: Bit 0-Ignore					Pretest error. Rerun routines 1504 thru 150A. Additional comments:
			Bit 1-See Comment 1.	Y4D2		RA102	6-082	1. If this bit is off, IN X'76' failed to indicate which adapter caused the interrupt.
			Bit 2 thru 5-bit clock check for LIBs 1,2,3, or 4 (respectively).	Y4F2		RS206	A-210,	
			Bit 6-LIB address check.	Y4F2		RS206	A-210, A-220	
			Bit 7-outbus parity error.	Y4E2		RS102	A-210, A-220	
150C	0X02	Ability of the type 1 CS to detect bad parity on the CCU outbus.	After inverting the outbus parity bits (via OUT X'78') and putting bad data onto the outbus (via OUT X'41'), no level 1 check, indicating outbus check, occurred. Reg. X'15' describes the error: If byte 1=		00C1			Test error. Reg. X'13' contains the data pattern that was set onto the outbus with the parity bits inverted. If byte 1 of Reg.
			X'01' - level 1 interrupt occurred but IN X'44', byte 1,bit7, (outbus check bit) failed to set.	Y4E2		RS102	A-210 A-220	X'15' was X'81', record the contents of Reg. X'13' and continue the routine. (See General Comments, #4.) By continuing and recording the contents of Reg. X'13' each time this error stop occurs, a failing bit pattern may be detected.
			X'81' - outbus parity detector apparently failed to detect bad parity.	Y4E2		RS101, RS102		
			If byte 1, bit 1 is on, see comment 1.	Y4D2		RA102		Additional comments: 1. If this bit is on, IN X'76' failed to indicate which adapter caused the interrupt. Rerun routine 150A.
150C	0X03	Ability to reset the outbus check bit in IN X'44' (byte 1, bit 2).	After having forced and attempting to reset (via OUT X'45' with byte 1, bit 5 on) an outbus check, IN X'44' still indicated an outbus check.	Y4E2		RS102	A-210, A-220	Test error.
150C	0X04	Ensure that after resetting the source of a bid for level 1, no more level 1 interrupts occur.	After having reset the outbus check bit in IN X'44', level 1 interrupts were unmasked and another level 1 interrupt occurred.	Y4D2, Y4F2		RA102	A-210	Test error.
150D	XXXX	Unwanted Level 2 Interrupts With LIBs Disabled: The CS is reset and enabled. Level 2 interrupts are unmasked for 30 milliseconds, and a check made to ensure that no level 2 interrupts occur.						
150D	0X01	Ensure that, after only a scanner reset and enable, no level 2 interrupts are pending.	After unmasking level 2 interrupts for 30 milliseconds, at most, a level 2 interrupt occurred.	Y4F2, Y4G2		RS202, RS305	A-010, A-040	Test error. Display reg. X'14'. If it contains X'86F0',

OUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								an unwanted character service interrupt occurred. Try replacing Y4F2 first. If byte 0, bits 0 and 4 are on, an unwanted bit service occurred. Try replacing Y4G2 first. Display reg. X'42'. If either byte 0, bits 6 or 7 are on, the mode bits in local store (ALD page RS 304) have probably not been reset properly. If none of the above cases are true, the '+ bid level 2 interrupt' line on ALD page RS202 is hot.
150E	XXXX	Set Mode Bit Override: After resetting and enabling the scanner, ensure that both the 'mode bit override' and 'override remember' latches can be set via OUT X'40'.						
150E	0X01	Ensure that the 'mode bit override' latch can be set via OUT X'40'.	After resetting and enabling the scanner, and issuing an OUT X'40', and IN X'44' indicated the 'mode bit override' latch had not set (byte 0, bit 0 was off).	Y4E2	8000	RS104	A-230	Test error. Problem is in the CS itself. If needed, Reg X'14' contains the result of the IN X'44'.
150E	0X02	Ensure that the 'override remember' latch can be set via OUT X'40'.	The same in X'44' that followed the OUT X'40' in error code 0X01, above, indicated the 'override remember' latch failed to set (byte 0, bit 2 was off).	Y4E2	2000	RS104	A-230	Test error. Problem is in the CS itself. If needed, Reg X'14' contains the results of the IN X'44'.
150F	XXXX	Reset Mode Bit Override: After resetting the scanner and setting both the 'mode bit override' and 'override remember' latches, ensure that an OUT X'44' can reset the 'mode bit override' latch.						
150F	0X01	Ensure that an error. OUT X'40' can routine set the 'mode bit override' and reg. 'override remember' contains latches. actual	After having reset the scanner and issuing an OUT X'40', an IN X'44' indicated that one or both of the latches failed to set. If byte 0, bit 0 of Reg X'15' is IN on, the 'mode bit override' data. latch failed to set. If byte 0, bit 2 is on, the 'override remember' latch failed to set.	Y4E2	A000	RS104	A-230	Pretest Rerun 150E. If needed, X'14' the received X'43'
150F	0X02	Ensure that the error. 'mode bit is override' latch CS, can be reset	After setting 'mode bit override', an OUT X'44' with byte 1, bit 2 on was issued to	Y4E2	8000	RS104	A-230	Test Problem in the itself.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		If via OUT X'44'. Reg.	reset 'override'. An IN X'44' contains then indicated that actual 'mode bit override', received byte 0, bit 0, was still on.					needed, X'14' the data by the IN X'44'.
150F	0X03	Ensure that error. resetting 'mode bit override' does cause not reset 'override remember'. is	After resetting mode bit override, the same IN X'44' described in error code 0X02, above, indicated that 'override remember' outbus had reset also.. and	Y4E2		RS104	A-230	Test The only possible of this problem that bits 1.2 1.3 on ALD page given are tied together.
1510	XXXX	Reset Override Remember: After resetting the scanner and setting both the 'mode bit override' and 'override remember' latches, ensure that an OUT X'44' can reset the 'override remember' latch.						
1510	0X01	Ensure that an OUT X'40' can set the 'mode bit override' and 'override remember' latches.	After having reset the scanner and issuing an OUT X'40', an IN X'44' indicated that one or both of the latches failed to set. If byte 0, bit 0 of Reg X'15' is on, the 'mode bit override' latch failed to set. If byte 0, bit 2 is on, the 'override remember' latch failed to set.	Y4E2	A000	RS104	A-230	Pretest error. Rerun routine 150E. If needed. Reg X'14' contains the actual received IN X'43' data.
1510	0X02	Ensure that the 'override remember' latch can be reset via OUT X'44'.	After setting 'override remember' and 'mode bit override', an OUT X'44' with byte 1, bit 3 on was issued to reset 'override remember'. An IN X'44' then indicated that 'override remember', byte 0, bit 2, was still on.	Y4E2	2000	RS104	A-230	Test error. Problem is in the CS, itself. If needed, Reg X'14' contains the data received by the IN X'44'.
1510	0X03	Ensure that resetting 'override remember' does not reset 'mode bit override'.	After resetting override, the same IN X'44' described in error code 0X02, above, indicated that mode bit override had reset also.	Y4E2		RS104	A-230	Test error. The only possible cause of this problem is that OUTBUS bits 1.2 and 1.3 on ALD page given are tied together.
1511	XXXX	Unwanted Level 2 Interrupts With LIBs Enabled: The CS is reset and enabled, and a LIB is enabled, Level 2 interrupts are unmasked for 30 milliseconds, and a check made to ensure that no level 2 interrupts occur. The routine is run first with the first LIB enabled, then again, with the second LIB enabled, and so on.						
1511	0X01	Before starting the test, ensure that no level 2 interrupts are already	After resetting and enabling the scanner and unmasking level 2 interrupts for, at	Y4F2, Y4G2		RS202	A-060	Pretest error. Rerun routine 150D. If reg.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		pending, even with the LIBs disabled.	most, 30 milliseconds, a level 2 interrupt occurred.					X'14' contains X'86F0', a character service interrupt occurred. If byte 0, bits 0 and 4 are on, a bit service interrupt occurred.
1511	0X02	Knowing, now, that no level 2 interrupts have occurred with the LIBs disabled, ensure that after enabling a LIB, no more level 2 interrupts occur.	After enabling a LIB, a level 2 interrupt has occurred. (Byte 0, bits 6 and 7 of reg. X'11' indicate which LIB was enabled: 0, 1, 2, or 3.)	Y4G2		RS305, RS304	A-040	Test error. "Sampled bit service" from the LIB has probably been allowed to set the 'bit service level 2' latch. Display reg. X'42'. If either byte 0, bits 6 or 7 are on, the mode bits in local store (ALD page RS304) have probably not been reset properly, allowing the bit service to occur.
1512	XXXX	Force Bit Service Instruction (OUT X'47'): Test all 64 addresses, in turn, to ensure that forcing bit service to a given line will cause a bit service interrupt to occur from that line, and that line only, within one scanner pass. (LIBs are kept disabled.) Then check the ability to reset the forced bit service.						
1512	0X01	Ability of an OUT X'47' to cause a bit service level 2 interrupt.	After resetting and enabling the scanner (not the LIBs), an OUT X'47' failed to cause a bit service interrupt. Reg. X'11' contains line (BCB) address of line being tested.	Y4G2, Y4F2		RS305	A-330, A-040	Test error. Continue from error stop after recording the failing line address. (See General Comments, #4.) By recording the line address each time this error stop occurs, the trouble may be further isolated. If all line addresses fail; failure is probably near the 'bit service latch' on ALD page RS305 or the 'force bit service' line on ALD page RS201. If not, failure is probably near the scan counter.
1512	0X02	Ensure that the OUT X'47' (force bit service), which caused the interrupt just received, forced 'bit service' from the correct address.	The address received via an IN X"41" (input address) indicated that the scanner was forced to stop at the wrong address. Reg. X'11' contains the line (BCB) address of the line forced. Reg. X'14' contains the line (BCB) address received by the IN X'41'.	Y4F2, Y4G2		RS201	A-330	Test error. Either the scan counter is not stopping properly or the force bit service compare circuits failed. Continue from

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								(General Comments, #4.) to determine which addresses are failing.
1512	0X03	Ensure that trying to reset a forced bit service does not cause a feedback check.	An OUT X'41' (reset bit service) caused a feedback check to be indicated in an IN X'43'. Reg. X'11' contains the line (BCB) address of the line under test.	Y4F2, Y4G2	4000	RS202	A-240	Test error. This failure could be caused by a failure in the 'feedback check' latch itself or, most likely, a solid bit service condition present in a LIB or line adapter. See General Comments, #3.
1512	0X04	Ensure that OUT X'41' (reset 'bit service') can reset a forced bit service.	In X'77' still showed a bit service level 2 pending after the OUT X'41' was issued. (Reg. X'11' contains the line (BCB) address of address under test, if needed.)	Y4F2, Y4E2 Y4G2	4000	RS202	A-240	Test error. Either the 'start scanner' line failed to come up or the 'bit service' latch failed to reset.
1512	0X05	Ensure that after resetting the forced bit service, no other bit service interrupts occur.	After resetting the forced interrupt, unmasking level 2 interrupts again, and awaiting a scanner pass, another level 2 interrupt occurred. Reg. X'14' contains the modified results of an IN X'41' issued to determine the address of the line causing the second interrupt. (Ignore byte 0, bit 0.)	Y4F2		RS201	A-330	Test error. Most likely cause is failure to reset the OUT X'47' (force bit service) latch on ALD page given.
1514	XXXX	Reset Bit Service in Scanner: forced from that address, 'bit	Test each address to ensure that, after a bit service interrupt has been service' can be reset by both OUT X'41' and OUT X'46'.					
1514	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1514	0X02	Ability to reset (via OUT X'41' or OUT X'46') a bit service, level 2 request.	After having forced a bit service request from the line under test and attempting to reset it, an IN X'77' still showed an outstanding type 1 CS level 2 request (byte 0, bit 1 was on). Reg. X'11' contains the address to which bit service was forced. If byte 0, bit 3 is off, the reset attempted was an OUT X'41'. If it is on, the reset was an OUT X'46'.	Y4F2 Y4E2	4000	RS202, RS104	A-240, A-320	Test error. Failure is probably near the start scanner line on ALD page RS202. If failure occurs only when OUT X'46' is used, problem may be on card Y4D2, on ALD page RA101. (This routine checks only the capability of resetting a bit service in the scanner. It does not check the capability

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								of resetting a bit service in a line adapter.)
1516	XXXX	Reset All Bits in IN X'42': Test each line address, in turn, to ensure that, after a scanner reset and enable, all bits in an IN X'42' were reset to 0. (LIBs are enabled.)						
1516	0X02	Ensure that, following an OUT X'45' with byte 0, bit 2 on, the CS is reset.	After waiting 30 microseconds (one scanner pass), an IN X'44' indicated the scanner was not reset. Reg. X'15' contains the bits in IN X'44' in error:		FFFF		A-250	Pretest error. Rerun routine 1504. Since 'scanner enabled' being off resets the others, if byte 0, bit 3 is on in error, ignore any others that are on. Reg. X'14' contains the result of the IN X'44'.
			Byte 0:					
			Bit 0-'mode bit override' latch failed to reset.	Y4E2		RS104	A-210	
			Bit 2-'override remember' latch failed to reset.	Y4E2		RS104	A-210	
			Bit 3-'scanner enabled' latch failed to reset.	Y4E2		RS105	A-310	
			Bit 4-'character service pending' latch failed to reset.	Y4E2		RS105	A-210, A-220	
			Byte 1:					
			Bits 2 thru 5-bit clock check for LIBs 1,2,3, or 4 (respectively) failed to reset.	Y4F2		RS206	A-210, A-220	
			Bit 6-'LIB select check' failed to reset.	Y4F2		RS206	A-210, A-220	
			Bit 7-'outbus check' failed to reset.	Y4E2		RS102	A-210, A-220	
1516	0X04	Ensure that following an OUT X'45', with byte 0, bit 1 on, the CS can be enabled.	IN X'44' byte 0, bit 3 (scanner enabled latch) failed to set.	Y4E2	1000	RS105	A-210, A-220	Pretest error. Rerun routine 1506. Reg. X'14' contains the result of the IN X'44'.
1516	0X06	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1516	0X08	Ensure that after a scanner reset, all IN X'42' bits have been reset.	After having stopped on the line address under test, an IN X'42' had some bits on. Reg. X'11' contains the line (BCB) address of the line under test. Reg. X'15' contains the bits in the IN X'42' that were on:	Y4G2 Y4E2	03FF	RS107	A-150, A-190	Test error. If the failing bits are byte 0, bits 6 or 7, or byte 1, bit 0, the problem is within the CS, probably in the local store
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	array. If not,
			Bit 7-mode bit 2			RS304	A-170	the problem may
			Byte 1:					be in the CS,
			Bit 0-low priority			RS304	A-170	in a LIB or in
			Bit 1-diagnostic mode			RS306	A-160	a line adapter.
			Bit 2-data terminal ready			RS306	A-160	(See General
			Bit 3-synchronous mode			RS306	A-160	Comments, #3.)
			Bit 4-external clock			RS306	A-160	As indicated
			Bit 5-data rate select			RS306	A-160	in the FETMM
			Bit 6-oscillator select bit 1			RS306	A-160	pages referenced,
			Bit 7-oscillator select bit 2			RS306	A-160	a problem could also exist in the control-in signals. (This would be most likely if

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								multiple bits are in error.)
1518	XXXX	Reset All Bits in IN X'43': Test each line address, in turn, to ensure that, after a scanner reset and enable, byte 0, bits 4 thru 7, and byte 1, bit 5 of an IN X'43' were reset to 0. (LIBs are enabled.) (This test is not run on autocall lines).						
1518	0X02	Ensure that following an OUT X'45' with byte 0, bit 2 on, the CS is reset.	After waiting 30 microseconds (one scanner pass), an IN X'44' indicated the scanner was not reset. Reg. X'15' contains the bits in IN X'44' in error:		FFFF		A-310	Pretest error. Rerun routine 1504. Since 'scanner enabled' being off resets the others, if byte 0, bit 3 is on in error, ignore any others that are on. Reg. X'14' contains the result of the IN X'44'.
			Byte 0:					
			Bit 0-'mode bit override' latch failed to reset.	Y4E2		RS104		
			Bit 2-'override remember' latch failed to reset.	Y4E2		RS104		
			Bit 3-'scanner enabled' latch failed to reset.	Y4E2		RS105	A-310	
			Bit 4-'character service pending' latch failed to reset.	Y4E2		RS105	A-210, A-220	
			Byte 1:					
			Bits 2 thru 5-bit clock check for LIBs 1,2,3, or 4 (respectively) failed to reset.	Y4F2		RS206	A-210, A-220	
			Bit 6-'LIB select check' failed to reset.	Y4F2		RS206	A-210, A-220	
			Bit 7-'outbus check' failed to reset.	Y4E2		RS102	A-210, A-220	
1518	0X04	Ensure that following an OUT X'45' with byte 0, bit 2 on, the CS can be enabled.	IN X'44' byte 0, bit 3 (scanner enabled latch) failed to set.	Y4E2	1000	RS105	A-210, A-220	Pretest error. Rerun routine 1506. Reg. X'14' contains the result of the IN X'44'.
1518	0X06	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1518	0X08	Ensure that, after a scanner reset and enable, all bits in an IN X'43' that should be reset, are reset..	After having stopped the scanner at the line address under test, an IN X'43' had some bits on that should have been reset. Reg. X'11' contains the line (BCB) address of the line under test. Reg. X'15' indicates the bits in the IN X'43' that should have been reset but were on:	Y4E2	4F04	RS107	A-180 A-190	Test error. The problem may be in the CS, in a LIB, or in a line adapter. (See General Comments, #3.) As also indicated, FETMM pages referenced, the problem may be in the control-in signals. (This would be more likely if a number of bits are in error.)
			Byte 0:					
			Bit 1-feedback error	Y4F2		RS202	A-200	
			Bit 4-transmit mode	Y4G2		RS308	A-200	
			Bit 5-new sync	Y4G2		RS308	A-200	
			Bit 6-request-to-send	Y4G2		RS308	A-200	
			Bit 7-send data	Y4G2		RS308	A-200	
			Byte 1:					
			Bit 5-diagnostic mode	Y4G2		RS307	A-200	
1519	XXXX	Reset All Bits in IN X'43' (autocall): Test each autocall line address, in turn, to ensure that after a scanner reset and enable, all bits in IN X'43' that can be reset are reset. (LIBs are enabled.)						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1519	0X02	Ensure that, following OUT X'45' with byte 0, bit 2 on, the CS is reset.	After waiting 30 microseconds (one scanner pass), an IN X'44' indicated the scanner was not reset. Reg X'15' contains the bits in IN X'44' in error: Byte 0: Bit 0-'mode bit override' latch failed to reset. Bit 2-'override remember' latch failed to reset. Bit 3-'scanner enabled' latch failed to reset. Bit 4-'character service pending' latch failed to reset. Byte 1: Bits 2 thru 5-bit clock checks for LIBs 1, 2, 3, or 4 (respectively) failed to reset. Bit 6-'LIB select check' failed to reset. Bit 7-'outbus check' failed to reset.	 Y4E2 Y4E2 Y4E2 Y4E2 Y4E2 Y4F2 Y4E2	FFFF	 RS104 RS104 RS105 RS105 RS206 RS206 RS102	A-310 A-310 A-210 A-220 A-210, A-220 A-210, A-220 A-210, A-220	Pretest error. Rerun routine 1504. Since 'scanner enabled' being off resets the others, if byte 0, bit 3 is on in error, ignore any others that are on. Reg. X'14' contains the result of the IN X'44'.
1519	0X04	Ensure that following an OUT X'45' with byte 0, bit 2 on, the CS can be enabled.	IN X'44' byte 0, bit 3 ('scanner enabled' latch) failed to set.	Y4E2	1000	RS105	A-210, A-220	Pretest error. Rerun routine 1506. Reg. X'14' contains the result of the IN X'44'.
1519	0X06	Ensure that force bit service (OUT X'47') a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts, and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1519	0X08	Ensure that after scanner reset and enable, all bits in IN X'43' that should be off, are off.	After having stopped the scanner at the line address under test, an IN X'43' had on bits that should have been reset. Reg. X'11' contains the line (BCB) address of the line under test. Reg. X'15' indicates the bits in the IN X'43' that should have been reset but were on: Byte 0: Bit 3-digit present Bit 4-digit NBR 8 Bit 5-digit NBR 4 Bit 6-digit NBR 2 Bit 7-digit NBR 1 Byte 1: Bit 4-call request	Y4G2 Y4E2	1F08	RS308 RS107	A-190	Test error. The problem may be in the CS, in a LIB, or in a line adapter. (See General Comments, #3). As indicated, FETMM page referenced, the problem may also be in the control-in signals. (This would be the more likely if a number of bits are in error.)
151A	XXXX	Set Transmit Mode/NBR-8 Bit. After resetting and enabling the CS, then stopping the scanner on the tested line and ensuring a successful reset, ensure that the transmit mode/NBR-8 bit at that address can be set. (This test is run on all installed line adapters, in turn.)						
151A	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
151A	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/ NBR-8 Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.
151A	0X03	Ensure that the transmit mode/NBR-8 bit, and that bit only, can be set by issuing OUT X'43' with byte 1, bit 4 on.	Either the transmit mode/ NBR-8 bit failed to set or other bits in IN X'43' set in error. Reg. X'15' contains the bits in error. If byte 0, bit 4 is on, the transmit mode/NBR-8 bit failed to set. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. Problem is most likely in assoc-ated line adapter. (See General Comments, #3.) If bits other than byte 0, bit 4 are in error, some kind of inter-action occurred. Reg. X'14' contains the received IN X'43' data.
151C	XXXX	Reset Transmit Mode/NBR-8 Bit: After the CS has been reset, the scanner is stopped at the tested address, the transmit mode/NBR-8 bit is set, and a test is made to ensure that it can then be reset. (This test is run on all installed line adapters, in turn.)						
151C	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
151C	0X02	Ensure that the transmit mode/NBR-8 bit, and that bit only, can be set by issuing OUT X'43' with byte 1, bit 4 on.	Either the transmit mode/ NBR-8 bit failed to set or other bits in IN X'43' set in error. Reg. X'15' contains the bits in error. If byte 0, bit 4 is on, the transmit mode/NBR-8 bit failed to set. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Pretest error. Rerun routine 151A.
151C	0X03	Ensure that the transmit mode/NBR-8 bit can be reset via OUT X'43'.	After setting the transmit mode/NBR-8 bit and attempt-ing to reset it via OUT X'43' with all bits off, an IN X'43' still indicated it as being set (or other bits in IN X'43' were on in error). Reg. X'15' contains the bits in error. Byte 0, bit 4 on indicates that the transmit mode/NBR-8 bit failed to reset. Reg. X'11' contains the line	Y4G2 Y4E2		RS308 RS106	A-200, A-290	Test error. Problem is most likely in the associated line adapter. (See General Comments, #3.) If error bits other than the transmit mode/NBR-8 bit are on, some kind of inter-action occurred. Reg. X'14' con-

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			(BCB) address under test.					tains the data received by the IN X'43'.
151E	XXXX	Set New Sync/NBR-4 Bit: After resetting and enabling the CS, stopping the scanner on the tested line address, and ensuring a successful reset, an attempt is made to set the new sync/NBR-4 bit. (This test is run on all installed line adapters, in turn. It ensures that the bit can be set on all synchronous and autocall lines and ensures that the bit is not set on all others.)						
151E	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
151E	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/ NBR-8 Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.
151E	0X03	Ensure that the new sync/NBR-4 bit in IN X'43' can be set by issuing an OUT X'43' with byte 1, bit 5 on.	Either the new sync/NBR-4 bit failed to act correctly or other bits turned on in error in the IN X'43'. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 0, bit 5 indicates a new sync/NBR-4 bit error.) Reg. X'14' contains the actual data received by the IN X'43'.	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. The problem is probably in the associated line adapter. (See General Comment, #3.) If other bits are in error also, some kind of inter-action occurred. If byte 0, bit 5 is on in both Reg X'14' and X'15', the line address tested was a start stop adapter and the new sync/NBR-4 bit set and should not have.
1520	XXXX	Reset New Sync/NBR-4 Bit: After the CS has been reset, the scanner is stopped at the tested address, the new sync/NBR-4 is set, and a test is made to ensure that it can then be reset. (This test will be run on all installed line adapters, in turn, except start/stop.)						
1520	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
1520	0X02	Ensure that the new sync/NBR-4 bit in IN X'43'	Either the new sync/NBR-4 bit failed to act correctly	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Pretest error. Rerun routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		can be set by issuing an OUT X'43' with byte 1, bit 5 on.	or other bits turned on in error in the IN X'43'. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 0, bit 5 indicates a new sync/NBR-4 bit error.) Reg. X'14' contains the actual data received by the IN X'43'.					151E.
1520	0X03	Ensure that the new sync NBR-4 bit can be reset via OUT X'43'.	After setting the new sync/NBR-4 bit, an attempt was made to reset it via OUT X'43' with all bits off. An IN X'43' then indicated the bit as still being set (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 0, bit 5 on indicates that the new sync/NBR-4 bit failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If error bits other than the new sync/NBR-4 bit are on, some kind of interaction occurred. Reg. X'14' contains the actual data received by the IN X'43'.
1522	XXXX	Set Send Data/NBR-1 Bit: After the CS has been reset, the scanner is stopped at the tested address, and an attempt is made to set the send data/NBR-1 bit. (This test is run on all installed line adapters, in turn.)						
1522	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1522	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/ NBR-8 Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.
1522	0X03	Ensure that the send data/NBR-1 bit in IN X'43' can be set by issuing an OUT X'43' with byte 1, bit 7 on.	Either the send data/NBR-1 bit failed to set or other bits were set in error in the IN X'43'. Reg X'15' contains the bits in IN X'43' in error. (Byte 0, bit 7 on indicates a send data/NBR-1 bit set failure.) Reg X'11' contains the line (BCB) address under test.	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. The problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are in error, some kind of interaction problem exists. Reg. X'14' contains the actual

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								data received by the IN X'43'.
1524	XXXX	Reset Send Data/NBR-1 Bit: After the CS has been reset, the scanner is stopped at the tested address, the send data/NBR-1 bit is set, and a test is made to ensure that it can then be reset. (This test is run on all installed line adapters, in turn.)						
1524	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error, Rerun routine 1512.
1524	0X02	Ensure that the send data/ NBR-1 bit in IN X'43' can be set by issuing an OUT X'43' with byte 1, bit 7 on.	Either the send data/NBR-1 bit failed to set or other bits were set in error in the IN X'43'. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in IN X'43' in error. (Byte 0, bit 7 on indicates a send data/NBR-1 bit set failure.)	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Pretest error. Rerun routine 1522.
1524	0X03	Ensure that the send data/NBR-1 bit can be reset via OUT X'43'.	After having set the send data/NBR-1 bit, an attempt was made to reset it via OUT X'43' with all bits off. An IN X'43' then indicated the bit was still set (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 0, bit 7 on indicates that the send data/NBR-1 bit failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If error bits other than the send data/NBR-1 bit are on, some kind of interaction occurred. Reg. X'14' contains the actual data received by the IN X'43'.
1526	XXXX	Set Request-to-Send/NBR-2 Bit: After the CS has been reset, the scanner is stopped at the tested address, and an attempt is made to set the request-to-send/NBR-2 bit. (This test is run on all installed line adapters, in turn.)						
1526	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1526	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/ NBR-8	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	PEALD PAGE	FETMM PAGE	COMMENTS
			Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode					
1526	0X03	Ensure that the request to-send/NBR-2 bit can be set by issuing an OUT X'43' with byte 1, bit 6 on.	Either the request-to-send/ NBR-2 bit failed to set or other bits were set in error in the IN X'43'. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in IN X'43' in error. (Byte 0, bit 6 on indicates a request-to-send/NBR-2 bit set failure.)	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. The problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are in error, some kind of interaction problem exists. Reg. X'14' contains the actual data received by the IN X'43'.
1528	XXXX	Reset Request-to-Send/NBR-2 Bit: After the CS has been reset, the scanner is stopped at the tested address, the request-to-send/NBR-2 bit is set, and a test is made to ensure that it can then be reset. (This test is run on all installed line adapters, in turn.)						
1528	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305,	A-330, A-040	Pretest error. Rerun routine 1512.
1528	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/ NBR-8 Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode	Y4G2		RS308	A-200	Pretest error. Rerun routine 1526.
1528	0X03	Ensure that the request-to send/NBR-2 bit can be reset via OUT X'43'.	After having set the request-to-send/NBR-2 bit, an attempt was made to reset it via OUT X'43' with all bits off. An IN X'43' then indicated the bit was still set (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 0, bit 6 on indicates that the request-to-send/NBR-2 bit failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. The problem is probably in the associated line adapter. (See General Comments, #3.) If other error bits are on, some kind of interaction occurred. Reg. X'14' contains the actual data received by

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								the IN X'43'.
152A	XXXX	Set Synchronous Mode Bit: After the CS has been reset, the scanner is stopped at the tested address, and an attempt is made to set the synchronous mode bit. (This test is run on all installed line adapters, in turn. It ensures that the bit can be set on all synchronous lines and ensures that it is not set on all others.)						
152A	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2,Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
152A	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset:	Y4G2	FFFF		A-150	Pretest error. Rerun routine 1516.
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	
			Bit 7-mode bit 2			RS304	A-170	
			Byte 1:					
			Bit 0-low priority			RS304	A-170	
			Bit 1-diagnostic mode			RS306	A-160	
			Bit 2-data terminal ready			RS306	A-160	
			Bit 3-synchronous mode			RS306	A-160	
			Bit 4-external clock			RS306	A-160	
			Bit 5-data rate select			RS306	A-160	
			Bit 6-oscillator select 1			RS306	A-160	
			Bit 7-oscillator select 2			RS306	A-160	
152A	0X03	Ensure that the synchronous mode bit in IN X'42' can be set by issuing an OUT X'42' with byte 1, bit 3 on.	Either the synchronous mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 3 on indicates a synchronous mode bit error.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are in error, some kind of interaction occurred. If byte 1, bit 3 is on in both regs. X'14' and X'15', the line address tested was a start-stop adapter and the synchronous mode bit set and should not have.
152C	XXXX	Reset Synchronous Mode Bit: After the CS has been reset, the scanner is stopped at the tested address, the synchronous mode bit is set, and a test is made to ensure that it can then be reset. (This test is run on all installed synchronous line adapters, in turn.)						
152C	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
152C	0X02	Ensure that the synchronous mode bit in IN X'42' can be set by issuing an OUT X'42' with byte 1, bit 3 on.	Either the synchronous mode bit failed to set, or other bits in the IN X'42' turned on in error. Reg. X'11' contains the bits in error. (Byte 1, bit 3 on indicates a synchronous mode bit error.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 152A.
152C	0X03	Ensure that the synchronous mode bit can be reset via OUT X'42'.	After having set the synchronous mode bit, an attempt to reset it was made via OUT X'42' with all bits off. An IN X'42' then indicated the bit was still set (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 1, bit 3 on indicates that the synchronous mode bit failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are on in error, some kind of interaction occurred. Reg. X'14' contains the actual data received by the IN X'42'.
152E	XXXX	Set Data Rate Select Bit: After the CS has been reset, the scanner is stopped at the tested address, and an attempt is made to set the data rate select bit. (This test is run on all installed line adapters, in turn. This ensures that the bit can be set on all synchronous lines and ensures that it is not set on all others.)						
152E	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
152E	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset: Byte 0: Bit 6-mode bit 1 Bit 7-mode bit 2 Byte 1: Bit 0-low priority Bit 1-diagnostic mode Bit 2-data terminal ready Bit 3-synchronous mode Bit 4-external clock Bit 5-data rate select Bit 6-oscillator select 1 Bit 7-oscillator select 2	Y4G2	FFFF	 RS304 RS304 RS304 RS306 RS306 RS306 RS306 RS306 RS306 RS306	A-150 A-170 A-170 A-170 A-160 A-160 A-160 A-160 A-160 A-160 A-160	Pretest error. Rerun routine 1516.
152E	0X03	Ensure that the data rate select bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 5 on.	Either the data rate select bit failed to act correctly or other bits in IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 5 on indicates a data rate select bit failure.)	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are on in error, some kind of interaction

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Reg. X'14' contains the actual data received by the IN X'42'.					occurred. If byte 1, bit 5 is on in both regs X'14' and X'15', the line under test was a start-stop adapter and the data rate select bit set and should not have set
1530	XXXX	Reset Data Rate Select Bit: After the CS has been reset, the scanner is stopped at the tested address, the data rate select bit is set, and a test is made to ensure that it can then be reset. (This test is run on all installed synchronous line adapters, in turn.)						
1530	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1530	0X02	Ensure that the data rate select bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 5 on.	Either the data rate select bit failed to set or other bits in IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 5 on indicates a data rate select bit failure.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 152E.
1530	0X03	Ensure that the data rate select bit can be reset via OUT X'42'.	After having set the data rate select bit, an attempt to reset it was made via OUT X'42' with all bits off. An IN X'42' then indicated the bit was still set (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 1, bit 5 on indicates that the data rate select bit failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are on, in error, some kind of interaction occurred. Reg. X'14' contains the actual data received by the IN X'42'.
1532	XXXX	Set Data Terminal Ready (DTR) Bit: After the CS has been reset, the scanner is stopped at the tested address, and an attempt is made to set the data terminal ready (DTR) bit. (This routine is run on all installed non-autocall line adapters, in turn.)						
1532	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2,Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1532	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under	Y4G2	FFFF		A-150	Pretest error. Rerun routine 1516.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			test. Reg. X'15' indicates the bits in the IN X'42' that were not reset: Byte 0: Bit 6-mode bit 1 Bit 7-mode bit 2 Byte 1: Bit 0-low priority Bit 1-diagnostic mode Bit 2-data terminal ready Bit 3-synchronous mode Bit 4-external clock Bit 5-data rate select Bit 6-oscillator select 1 Bit 7-oscillator select 2			 RS304 RS304 RS304 RS306 RS306 RS306 RS306 RS306 RS306 RS306	 A-170 A-170 A-170 A-160 A-160 A-160 A-160 A-160 A-160 A-160	
1532	0X03	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are on in error, some kind of interaction has occurred.
1534	XXXX	Reset Data Terminal Ready (DTR) Bit: After the CS has been reset, the scanner is stopped at the tested address, the data terminal ready (DTR) bit is set, and a test is made to ensure that it can then be reset. (This test is run on all installed non-autocall line adapters, in turn.)						
1534	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1534	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.
1534	0X03	Ensure that the data terminal ready (DTR) bit can be reset via OUT X'42'.	After having set the data terminal ready bit, an attempt to reset it was made via OUT X'42' with all bits off. An IN X'42' then indicated the bit was still set (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 1, bit 2 on indicates that the data terminal ready bit failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are on in error, some kind of interaction occurred. Reg. X'14' contains the actual data received by the IN X'42'.
1536	XXXX	Set External Clock Bit: After the CS has been reset, the scanner is stopped at the tested address, and an attempt is made to set the external clock bit. (This routine is run on all installed line adapters, in turn. It ensures that the bit can be set on all synchronous lines and ensures that it is not set on all others.)						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1536	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
1536	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset:	Y4G2	FFFF		A-150	Pretest error. Rerun routine 1516.
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	
			Bit 7-mode bit 2			RS304	A-170	
			Byte 1:					
			Bit 0-low priority			RS304	A-170	
			Bit 1-diagnostic mode			RS306	A-160	
			Bit 2-data terminal ready			RS306	A-160	
			Bit 3-synchronous mode			RS306	A-160	
			Bit 4-external clock			RS306	A-160	
			Bit 5-data rate select			RS306	A-160	
			Bit 6-oscillator select 1			RS306	A-160	
			Bit 7-oscillator select 2			RS306	A-160	
1536	0X03	Ensure that the external clock bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 4 on.	Either the external clock bit failed to act correctly or other bits in IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 4 on indicates an external clock bit set failure.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are on in error, some kind of interaction occurred. If byte 1, bit 4 is on in both regs X'14' and X'15', the line under test was a start-stop or autocall adapter and the external clock bit set and should not have set.
1538	XXXX	Reset External Clock Bit: After the CS has been reset, the scanner is stopped at the tested address, the external clock bit is set, and a test made to ensure that it can then be reset. (This test is run on all installed synchronous line adapters, in turn.)						
1538	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts, and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1538	0X02	Ensure that the external clock bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 4 on.	Either the external clock bit failed to act correctly or other bits in IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 4 on indicates an external clock	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1536.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			bit set failure.) Reg. X'14' contains the actual data received by the IN X'42'.					
1538	0X03	Ensure that the external clock bit can be reset via OUT X'42'.	After having set the external clock bit, an attempt to reset it was made via OUT X'42' with all bits off. An IN X'42' then indicated the bit was still set (or other bits were set in error). Reg. X'15' contains the bits in error. Bytes 1, bit 4 on indicates that the external clock bit failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2	03FF	RS306 RS106	A-160, A-270	Test error. Problem is probably in associated line adapter. (See General Comments, #3.) If other bits are on, in error, some kind of interaction occurred. Reg. X'14'contains the actual data received by the IN X'42'.
153A	XXXX	Set Diagnostic Mode Bit in IN X'42': After the CS has been reset, the scanner is stopped at the tested address, and an attempt made to set the diagnostic mode bit. (This routine is run on all installed line adapters, in turn. It tests that the bit can be set on all non-autocall lines and that it is not set on all autocall lines.)						
153A	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
153A	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabline the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset: Byte 0: Bit 6-mode bit 1 Bit 7-mode bit 2 Byte 1: Bit 0-low priority Bit 1-diagnostic mode Bit 2-data terminal ready Bit 3-synchronous mode Bit 4-external clock Bit 5-data rate select Bit 6-oscillator select 1 Bit 7-oscillator select 2	Y4G2	FFFF	 RS304 RS304 RS304 RS306 RS306 RS306 RS306 RS306 RS306 RS306	 A-170 A-170 A-170 A-160 A-160 A-160 A-160 A-160 A-160 A-160	Pretest error. Rerun routine 1516.
153A	0X03	Ensure that the diagnostic mode bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 1 on.	Either the diagnostic mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 1 on indicates a diagnostic mode bit failure.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are on in error, some kind of interaction occurred. If byte 1, bit 1 is on in both Regs. X'15' and X'14', the line adapter tested was an autocall adapter and the diagnostic

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								mode bit set and should not have.
153C	XXXX	Reset Diagnostic Mode Bit in IN X'42': After the CS has been reset, the scanner is stopped at the tested address, the diagnostic mode bit is set, and a test made to ensure that it can then be reset. (This test is run on all installed line adapters, in turn, except autocall.)						
153C	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
153C	0X02	Ensure that the diagnostic mode bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 1 on.	Either the diagnostic mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 1 on indicates a diagnostic mode bit failure.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 153A.
153C	0X03	Ensure that the diagnostic mode bit can be reset via OUT X'42'.	After having set the diagnostic mode bit, an attempt to reset it was made via OUT X'42' with byte 1, bit 1 off. An IN X'42' then indicated the bit was still set (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 1, bit 1 on indicates that the diagnostic mode bit failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in associated line adapter. (See General Comments, #3.) If other bits are on in error, some kind of interaction occurred. Reg. X'14' contains the actual data received by the IN X'42'.
153E	XXXX	Set Diagnostic Mode Bit in IN X'43': After the CS has been reset, the scanner is stopped at the tested address and after ensuring that the diagnostic mode bit in IN X'43' is not on, the diagnostic mode latch in the line adapter is set via OUT X'42'. The scanner is then started and stopped again to allow the diagnostic mode bit in IN X'43' to be set by control-in-B and a check made to ensure that it has set. (This test is run on all installed line adapters, in turn, except autocall.)						
153E	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
153E	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabline the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/ NBR-8	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode					
153E	0X03	Ensure that the diagnostic mode bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 1 on.	Either the diagnostic mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 1 on indicates a diagnostic mode bit failure.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 153A.
153E	0X04	Ensure that the diagnostic mode bit in IN X'43' can not be set by the OUT X'42' just issued until the scanner has again been started.	After having set the diagnostic mode bit in IN X'42' and not starting the scanner, the diagnostic mode bit in IN X'43' was on (byte 1, bit 5). Reg. X'11' contains the line (BCB) address under test.	Y4G2	0004	RS307	A-200	Pretest error. Problem is probably in the CS. (See General Comments, #3.) The 'B in 6' latch on the ALD given should not be set until the next '53 time'. Since the scanner is stopped, '53 time' should not occur again until the scanner is started.
153E	0X05	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
153E	0X06	Ensure that once the diagnostic mode latch in a line adapter has been set and the scanner has been started and stopped again, the diagnostic mode bit in IN X'43' can be set.	After having set the diagnostic mode bit in IN X'42', starting the scanner and stopping it again, an IN X'43' failed to indicate diagnostic mode as being set (Byte 1, bit 5 on). Reg. X'11' contains the line (BCB) address under test.	Y4G2	0004	RS307	A-200	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) Reg. X'14' contains the actual data received by the IN X'43'. If byte 0, bit 1 is on, a feedback check has occurred. Ignore the diagnostic mode bit failure and rerun routines 1512 and 1514.

1540 XXXX Reset Diagnostic Mode Bit in IN X'43': After the CS has been reset, the scanner is stopped at the tested address and the diagnostic mode latch in the line adapter is set. The scanner is started and stopped again, and a check made to ensure that diagnostic mode is on in IN X'43'. OUT X'42' is issued to reset the diagnostic mode latch, the scanner is again started and stopped, and a check made to ensure that the diagnostic mode bit in IN X'43' is now off. (This test is run on all installed line adapters, in turn, except autocall.)

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1540	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1540	0X03	Ensure that once the scanner is stopped, it can be started again via OUT X'41' and then stopped again by forcing a bit service (OUT X'47') interrupt.	Either the scanner could not be started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000			Pretest error. Rerun routine 1512.
			X'E000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - The OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330, A-040	
1540	0X04	Ensure that once the diagnostic mode latch in a line adapter has been set and the scanner has been started and stopped again, the diagnostic mode bit in IN X'43' can be set.	After having set the diagnostic mode bit in IN X'42', starting the scanner and stopping it again, an IN X'43' failed to indicate diagnostic mode as being set (Byte 1, bit 5 on). Reg. X'11' contains the line (BCB) address under test.	Y4G2	0004	RS307	A-200	Pretest error. Rerun routine 153E.
1540	0X05	Ensure that once the scanner is stopped, it can be started again via OUT X'41' and then stopped again by forcing a bit service (OUT '47') interrupt.	Either the scanner could not started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000			Pretest error. Rerun routine 1512.
			X'E000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - The OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330, A-040	
1540	0X06	Ensure that resetting the diagnostic mode latch in	After issuing OUT X'42' (with byte 1, bit 1 off) to reset	Y4G2	0004	RS307	A-200	Test error. Problem is

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		the line adapter (via OUT X'42') resets the diagnostic mode bit in IN X'43'.	the diagnostic mode latch in the line adapter and starting and stopping the scanner again, an IN X'43' still indicated that diagnostic mode was set (Byte 1, bit 5 on). Reg. X'11' contains the line (BCB) address under test.					probably in the CS; however, see general comments, #3. Apparently, once the 'B in 6' latch, on ALD page given, is set, it cannot be reset.
1542	XXXX	Set Oscillator Select Bit 1: After the CS has been reset, the scanner is stopped at the address under test, and an attempt is made to set oscillator select bit 1. (This test is run on all installed line adapters, in turn. It tests to ensure that the bit sets on all adapters except autocall.)						
1542	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1542	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset:	Y4G2	FFFF		A-150	Pretest error. Rerun routine 1516.
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	
			Bit 7-mode bit 2			RS304	A-170	
			Byte 1:					
			Bit 0-low priority			RS304	A-170	
			Bit 1-diagnostic mode			RS306	A-160	
			Bit 2-data terminal ready			RS306	A-160	
			Bit 3-synchronous mode			RS306	A-160	
			Bit 4-external clock			RS306	A-160	
			Bit 5-data rate select			RS306	A-160	
			Bit 6-oscillator select 1			RS306	A-160	
			Bit 7-oscillator select 2			RS306	A-160	
1542	0X03	Ensure that oscillator select bit 1 (IN X'42', byte 1, bit 6) can be set by issuing OUT X'42' with that bit on.	Either oscillator select bit 1 failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 6 on indicates the oscillator select bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2	03FF	RS306 RS106	A-160 A-270	Test error. Failure is probably in the associated line adapter. (See General Comments, #3.) If other bits are in error, some kind of interaction occurred. If byte 1, bit 6 is on in both regs. X'15' and X'14', the line adapter under test was an autocall adapter and oscillator select bit 1 was on and should not have been.
1544	XXXX	Reset Oscillator Select Bit 1: After the CS has been reset, the scanner is stopped at the tested address, oscillator select bit 1 is set, and a test made to ensure that it can be reset. (This test is run on all installed line adapters, in turn, except autocall.)						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1544	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1544	0X02	Ensure that oscillator select bit 1 (IN X'42', byte 1, bit 6) can be set by issuing OUT X'42' with that bit on.	Either oscillator select bit 1 failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 6 on indicates the oscillator select bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1542.
1544	0X03	Ensure that oscillator select bit 1 can be reset via OUT X'42'.	After having set oscillator select bit 1, an attempt to reset it was made via OUT X'42' with byte 1, bit 6 off. An IN X'42' then indicated the bit was still on (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 1, bit 6 on indicates that oscillator select bit 1 failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are in error, some kind of interaction occurred. Reg. X'14' contains the actual data received by the IN X'42'.
1546	XXXX	Set Oscillator Select Bit 2: After the CS has been reset, the scanner is stopped at the address under test, and an attempt is made to set oscillator select bit 2. (This test is run on all installed line adapters, in turn. It tests to ensure that the bit sets on all adapters except autocall.)						
1546	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1546	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset: Byte 0: Bit 6-mode bit 1 Bit 7-mode bit 2 Byte 1: Bit 0-low priority Bit 1-diagnostic mode Bit 2-data terminal ready Bit 3-synchronous mode Bit 4-external clock Bit 5-data rate select Bit 6-oscillator select 1 Bit 7-oscillator select 2	Y4G2	FFFF	 RS304 RS304 RS304 RS306 RS306 RS306 RS306 RS306 RS306 RS306	A-150 A-170 A-170 A-170 A-160 A-160 A-160 A-160 A-160 A-160 A-160	Pretest error. Rerun routine 1516.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1546	0X03	Ensure that oscillator select bit 2 (IN X'42' byte 1, bit 7) can be set by issuing OUT X'42' with that bit on.	Either oscillator select bit failed to act correctly or other bits in IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 7 on indicates the oscillator select bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2	03FF	RS306 RS106	A-160 A-270	Test error. Failure is probably in the associated line adapter. (See General Comments, #6.) If other bits are in error, some kind of interaction occurred. If byte 1, bit 7 is on in both regs X'14' and X'15', the line adapter under test was an autocall adapter and oscillator select bit 2 was set and should not have been.
1548	XXXX	Reset Oscillator Select Bit 2: After the CS has been reset, the scanner is stopped at the tested address, oscillator select bit 2 is set, and a test made to ensure that it can then be reset. (This test is run on all installed line adapters, in turn, except autocall.)						
1548	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1548	0X02	Ensure that oscillator select bit 2 (IN X'42' byte 1, bit 7) can be set by issuing OUT X'42' with that bit on.	Either oscillator select bit 2 failed to act correctly or other bits in IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 7 on indicates the oscillator select bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1546.
1548	0X03	Ensure that oscillator select bit 2 can be reset via OUT X'42'.	After having set oscillator select bit 2, an attempt to reset it was made via OUT X'42' with byte 1, bit 7 off. An IN X'42' then indicated the bit was still on (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 1, bit 6 on indicates that oscillator select bit 2 failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are in error, some kind of interaction occurred. Reg. X'14' contains the actual data received by the IN X'42'.
154A	XXXX	Set Low Priority Bit: After the CS has been reset, the scanner is stopped at the tested address and a test made to ensure that the low priority bit for that address can be set. (This test is run on all addresses, in turn.)						
154A	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11',	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
154A	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset:	Y4G2	FFFF		A-150	Pretest error. Rerun routine 1516.
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	
			Bit 7-mode bit 2			RS304	A-170	
			Byte 1:					
			Bit 0-low priority			RS304	A-170	
			Bit 1-diagnostic mode			RS306	A-160	
			Bit 2-data terminal ready			RS306	A-160	
			Bit 3-synchronous mode			RS306	A-160	
			Bit 4-external clock			RS306	A-160	
			Bit 5-data rate select			RS306	A-160	
			Bit 6-oscillator select 1			RS306	A-160	
			Bit 7-oscillator select 2			RS306	A-160	
154A	0X03	Ensure that the low priority bit (IN X'42', byte 1, bit 0) can be set by issuing OUT X'42' with that bit on.	Either the low priority bit failed to set or other bits turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 0 on indicates the low priority bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS304 RS107	A-170, A-260	Test error. Problem is probably in the CS. If failure is unique to one address only, problem is probably associated with address selection in the interface control stack. If other bits are on in error, some kind of interaction occurred.
154C	XXXX	Reset Low Priority Bit: After the CS has been reset, the scanner is stopped at the tested address, the low priority bit is set, and then a test made to ensure that it can then be reset. (This test is run on all addresses, in turn.)						
154C	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
154C	0X02	Ensure that the low priority bit (IN X'42', byte 1, bit 0) can be set by issuing OUT X'42' with that bit on.	Either the low priority bit failed to set or other bits turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 0 on indicates the low priority bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS304 RS107	A-170, A-260	Pretest error. Rerun routine 154A.
154C	0X03	Ensure that the low priority bit can be reset via OUT X'42'.	After having set the low priority bit, an attempt to reset it was made via OUT	Y4G2	03FF	RS304	A-170 A-260	Test error. Problem is probably in

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			X'42' with byte 1, bit 0 off. An IN X'42' then indicated the bit was still on (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 1, bit 0 on indicates that the low priority bit failed to reset. Reg. X'11' contains the line (BCB) address tested.					the CS.
154E	XXXX	Set Mode Bit 1: After the CS has been reset, the scanner is stopped at the tested address and a test made to ensure that mode bit 1 for that address can be set. (This test is run on all addresses, in turn.)						
154E	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
154E	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset: Byte 0: Bit 6-mode bit 1 Bit 7-mode bit 2 Byte 1: Bit 0-low priority Bit 1-diagnostic mode Bit 2-data terminal ready Bit 3-synchronous mode Bit 4-external clock Bit 5-data rate select Bit 6-oscillator select 1 Bit 7-oscillator select 2	Y4G2	FFFF	 RS304 RS304 RS304 RS306 RS306 RS306 RS306 RS306 RS306 RS306	A-150 A-170 A-170 A-170 A-160 A-160 A-160 A-160 A-160 A-160 A-160	Pretest error. Rerun routine 1516.
154E	0X03	Ensure that mode bit 1 (IN X'42', byte 0, bit 6) can be set by issuing OUT X'42' with that bit on.	Either mode bit 1 failed to set or other bits turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 0, bit 6 on indicates mode bit 1 failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS304 RS107	A-170, A-260	Test error. Problem is probably in the CS. If other bits are on in error, some kind of interaction occurred.
1550	XXXX	Reset Mode Bit 1: After the CS has been reset, the scanner is stopped at the tested address, mode bit 1 is set, and then a test is made to ensure that it can then be reset. (This test is run on all addresses, in turn.)						
1550	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1550	0X02	Ensure that mode bit 1 (IN X'42', byte 0, bit 6) can be set by issuing	Either mode bit 1 failed to set or other bits truned on in error. Reg. X'11' contains	Y4G2 Y4E2	03FF	RS304 RS107	A-170, A-260	Pretest error. Rerun routine 154E.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		OUT X'42' with that bit on.	the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 0, bit 6 on indicates mode bit 1 failed.) Reg. X'14' contains the actual data received by the IN X'42'.					
1550	0X03	Ensure that mode bit 1 can be reset via OUT X'42'.	After having set mode bit 1, an attempt to reset it was made via OUT X'42' with byte 0, bit 6 off. An IN X'42' then indicated the bit was still on (or other bits were on in error). Reg. X'15' contains the bits in error. Byte 0, bit 6 on indicates mode bit 1 failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2	03FF	RS304	A-170, A-260	Test error. Problem is probably in the CS. If other bits are in error, some kind of interaction occurred.
1552	XXXX	Set Mode Bit 2: After the CS has been reset, the scanner is stopped at the tested address and a test made to ensure that mode bit 2 for that address can be set. (This test is run on all addresses, in turn.)						
1552	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1552	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset: Byte 0: Bit 6-mode bit 1 Bit 7-mode bit 2 Byte 1: Bit 0-low priority Bit 1-diagnostic mode Bit 2-data terminal ready Bit 3-synchronous mode Bit 4-external clock Bit 5-data rate select Bit 6-oscillator select 1 Bit 7-oscillator select 2	Y4G2	FFFF Rerun routine 1516.	 RS304 RS304 RS304 RS306 RS306 RS306 RS306 RS306 RS306 RS306	A-150 A-170 A-170 A-170 A-160 A-160 A-160 A-160 A-160 A-160 A-160	Pretest error.
1552	0X03	Ensure that mode bit 2 (IN X'42', byte 0, bit 7) can be set by issuing OUT X'42' with that bit on.	Either mode bit 2 failed to set or other bits were set in error. Reg. X'11' contains the line (BCB) address under test. Reg X'15' contains the bits in error. (Byte 0, bit 7 on indicates mode bit 2 failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS304 RS107	A-170 A-260	Test error. Problem is probably in the CS. If other bits are on in error, some kind of interaction occurred.
1554	XXXX	Reset Mode Bit 2: After the CS has been reset, the scanner is stopped at the tested address, mode bit 2 is set, and then a test is made to ensure that it can then be reset. (This test is run on all addresses, in turn.)						
1554	0X01	Ensure that force bit service (OUT X'47') causes	After attempting to force a bit service level 2 interrupt	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		a bit service interrupt from the line address under test.	(via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.					1512.
1554	0X02	Ensure that mode bit 2 (IN X'42', byte 0, bit 7) can be set by issuing OUT X'42' with that bit on.	Either mode bit 2 failed to set or other bits were set in error. Reg. X'11' contains the line (BCB) address under test. Reg X'15' contains the bits in error. (Byte 0, bit 7 on indicates mode bit 2 failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS304 RS107	A-170 A-260	Pretest error. Rerun routine 1552.
1554	0X03	Ensure that mode bit 2 can be reset via OUT X'42'.	After having set mode bit 2, an attempt to reset it was made via OUT X'42' with byte 0, bit 7 off. An IN X'42' then indicated the bit was still on (or other bits were set in error). Reg X'15' contains the bits in error. Byte 0, bit 7 on indicates mode bit 2 failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2	03FF	RS304	A-170, A-260	Test error. Problem is probably in the CS. If other bits are in in error, some kind of interaction occurred.
1556	XXXX	Set Call Request Bit: After the CS has been reset, the scanner is stopped at the tested address and a test made to ensure that call request can be set. (This test is run on all installed autocall adapters only, in turn.)						
1556	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1556	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/NBR-8 Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.
1556	0X03	Ensure that the call request bit in IN X'43' can be set by issuing OUT X'43' with byte 1, bit 2 on.	Either call request failed to set or other bits in IN X'43' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 4 on indicates call request	Y4G2 Y4E2	1F08	RS308 RS106	A-200 A-290	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			failed to set.) Reg. X'14' contains the actual data received by the IN X'43'.					bits are on in error, some kind of interaction problem occurred.
1558	XXXX	Reset Call Request Bit: After the CS has been reset, the scanner is stopped at the tested address, the call request bit is set, and then a test made to ensure that it can be reset. (This test is run on all installed autocall adapters only, in turn.)						
1558	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1558	0X02	Ensure that the call request bit in IN X'43' can be set by issuing OUT X'43' with byte 1, bit 2 on.	Either call request failed to set or other bits in IN X'43' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 4 on indicates call request failed to set.) Reg. X'14' contains the actual data received by the IN X'43'.	Y4G2 Y4E2	1F08	RS308 RS106	A-200 A-290	Pretest error. Rerun routine 1556.
1558	0X03	Ensure that the call request bit can be reset via OUT X'43' with byte 1, bit 2 off.	After having set the call request bit and attempting to reset it, an IN X'43' still indicated the bit was set (or other bits were set in error.) Reg. X'15' contains the bits in error. Byte 1, bit 4 on indicates call request failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2	1F08	RS308 RS106	A-200 A-290	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits were in error, some kind of interaction occurred.
155A	XXXX	Set Digit Present Bit: After the CS has been reset, the scanner is stopped at the tested address and a test made to ensure that digit present can be set. (This test is run on all installed autocall adapters only, in turn.)						
155A	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
155A	0X02	Before attempting to set the tested bit, ensure thatthe CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/NBR-8 Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
155A	0X03	Ensure that the digit present bit in IN X'43' can be set by issuing OUT X'43' with byte 1, bit 3 on.	Either digit present failed to set or other bits in IN X'43' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 0, bit 3 on indicates digit present failed to set.) Reg. X'14' contains the actual data received by the IN X'43'.	Y4G2 Y4E2	1F08	RS308 RS106	A-200 A-290	Test error. Problem is most likely in the associated line adapter. (See General Comments, #3.) If other bits are in error, some kind of interaction occurred.
155C	XXXX	Reset Digit Present Bit: After the CS has been reset, the scanner is stopped at the tested address, digit present is set, and then a check made to ensure it can be reset. (This test is run on all installed autocall adapters only, in turn.)						
155C	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
155C	0X02	Ensure that the digit present bit in IN X'43' can be set by issuing OUT X'43' with byte 1, bit 3 on.	Either digit present failed to set or other bits in IN X'43' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 0, bit 3 on indicates digit present failed to set.) Reg. X'14' contains the actual data received by the IN X'43'.	Y4G2 Y4E2	1F08	RS308 RS106	A-200 A-290	Pretest error. Rerun routine 155A.
155C	0X03	Ensure that the digit present bit can be reset via OUT X'43' with byte 1, bit 3 off.	After having set digit present and attempting to reset it an IN X'43' still indicated the bit was set (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 0, bit 3 on indicates digit present failed to reset. Reg. X'11' contains the line (BCB) address under test.	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits were in error, some kind of interaction occurred.
155E	XXXX	Output X'42' Interaction Test: After ensuring that all IN X'42' bits are off at two line addresses, all possible bits are turned on at one of them. A check is then made by doing an IN X'42' at the other to ensure that no interaction occurred (that is, that no bits were set). This test will be run on all installed line adapters. It is designed to run all possible address combinations. (Example: Assume line adapters are installed in addresses 0-5. The first pass through the test will set all bits on at line 0 and then ensure that no bits were set at line 1. The second pass will again set all bits on at line 0 but this time check line 2. This continues until line 5 has been checked. The sixth pass will set all bits at line 1 and check line 2. This pattern is continued until all addresses have been checked with all others.)						
155E	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11',	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
155E	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset:	Y4G2	FFFF		A-015	Pretest error. Rerun routine 1516.
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	
			Bit 7-mode bit 2			RS304	A-170	
			Byte 1:					
			Bit 0-low priority			RS304	A-170	
			Bit 1-diagnostic mode			RS306	A-160	
			Bit 2-data terminal ready			RS306	A-160	
			Bit 3-synchronous mode			RS306	A-160	
			Bit 4-external clock			RS306	A-160	
			Bit 5-data rate select			RS306	A-160	
			Bit 6-oscillator select 1			RS306	A-160	
			Bit 7-oscillator select 2			RS306	A-160	
155E	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
155E	0X04	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits in the IN X'42' that were not reset:	Y4G2	FFFF		A-150	Pretest error. Rerun routine 1516.
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	
			Bit 7-mode bit 2			RS304	A-170	
			Byte 1:					
			Bit 0-low priority			RS304	A-170	
			Bit 1-diagnostic mode			RS306	A-160	
			Bit 2-data terminal ready			RS306	A-160	
			Bit 3-synchronous mode			RS306	A-160	
			Bit 4-external clock			RS306	A-160	
			Bit 5-data rate select			RS306	A-160	
			Bit 6-oscillator select 1			RS306	A-160	
			Bit 7-oscillator select 2			RS306	A-160	
155E	0X05	To check for interaction, set all possible bits in an OUT X'42' on at one line address before checking the other address.	An IN X'42' following the OUT X'42' indicated a bit or bits failed to set. Reg. X'11' contains the line (BCB) address of the line being set. Reg. X'15' indicates which bits failed to set.	Y4G2			A-150	Test error. Although this has been designated as a test error, the capability to set the individual bits has been previously tested. Rerun routines 152A through 1554 to attempt further isolation. If necessary, refer to FETMM page given to

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								determine failing bit or bits. If only one line address fails, problem is probably in the associated line adapter. (See General Comments, #3.)
155E	0X06	Ensure that once the scanner is stopped, it can be started again via OUT X'41' and then stopped again by forcing a bit service (OUT X'47') interrupt.	Either the scanner could not started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000		A-240	Test error. Rerun routine 1512.
			X'E000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - The OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330, A-040	
155E	0X07	Ensure that no problem exists in address selection such that interaction occurs between two lines when issuing an OUT X'42'.	After setting all bits in OUT X'42' at one address and stopping the scanner at a second address, bits were found on in an IN X'42' at the second address. Reg. X'15' indicates the bits that were found on. Reg. X'13' contains the second line (BCB) address and Reg. X'11' contains the first.	Y4G2	03FF	RS301 RS302 RS304	A-010	Test error. If byte 0, bits 6 or 7, or byte 1, bit 0 are in error, problem is in the CS. If not, try to determine the pattern of failure by recording the line addresses and continuing from the error stop. (See General Comments, #4.) Failure may be restricted to line selection within a LIB (replace LIB cards). If not, failure is probably in line and LIB select circuitory within the CS. (Replace card indicated.)
1560	XXXX	Output X'43' Interaction Test: After ensuring that all bits that can be set by OUT X'43' are off in IN X'43' at two line addresses, all possible bits are turned on at one of them. A check is then made by doing an IN X'43' at the other to ensure that no interaction occurred (that is, that no bits were set). This test will be run on all installed line adapters. (See routine 155E, XXXX for description of the order in which lines are tested.)						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1560	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1560	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an IN X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/NBR-8 Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.
1560	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1560	0X04	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the scanner and forcing the scanner to stop at the tested address, bits in an in X'43' that should have been reset, were not. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' indicates the bits that were not reset in the IN X'43': Byte 0: Bit 3-digit present Bit 4-transmit mode/NBR-8 Bit 5-new sync/NBR-4 Bit 6-request to send/ NBR-2 Bit 7-send data/NBR-1 Byte 1: Bit 4-call request Bit 5-diagnostic mode	Y4G2		RS308	A-200	Pretest error. Rerun routines 1518 and 1519.
1560	0X05	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1560	0X06	To check for interaction, set all possible bits in an OUT X'43' on at one line address before checking the other address.	An IN X'43' following the OUT X'43' indicated a bit or bits failed to set. Reg. X'11' contains the line (BCB) address of the line being set.	Y4G2			A-180	Test error. Although this has been designated as a test error, the capability

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Reg. X'15' indicates which bits failed to set.					to set the individual bits has been previously tested. Rerun routines 151A through 1528 to attempt further isolation. If necessary, refer to FETMM page given to determine failing bit or bits. If only one line address fails, problem is probably in the associated line adapter. (See General Comments, #3.)
1560	0X07	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1560	0X08	Ensure that no problem exists in address selection such that interaction occurs between two lines when issuing an OUT X'43'.	After setting all possible bits in OUT X'43' at one address, one or more if those same bits were found on in an IN X'43' at the second address. Reg. X'15' indicates the bits that were found on. Reg. X'13' contains the second line (BCB) address and Reg. X'11' contains the first.	Y4G2		RS301 RS302	A-010	Test error. Try to determine the pattern of failure by recording the line addresses and continuing from the error stop. (See General Comments, #4.) Failure may be restricted to line selection within a LIB (replace LIB cards). If not, failure is probably in the line and LIB select circuitory in the CS. (Replace card indicated.)
1570	XXXX	Force Bit Service on Low Priority Lines: Each line address is tested, in turn, to ensure that after setting the address to low priority via OUT X'42', a bit service interrupt from that line can be forced via OUT X'47'.						
1570	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1570	0X02	Before attempting to set the tested bit, ensure that the CS reset was successful.	After resetting and enabling the CS and forcing the scanner to stop at the tested address, all bits in an IN X'42' should have been off (reset) and were not. Reg. X'11' contains the line (BCB) address under	Y4G2	FFFF		A-150	Pretest error. Rerun routine 1516.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			test. Reg. X'15' indicates the bits in the IN X'42' that were not reset:					
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	
			Bit 7-mode bit 2			RS304	A-170	
			Byte 1:					
			Bit 0-low priority			RS304	A-170	
			Bit 1-diagnostic mode			RS306	A-160	
			Bit 2-data terminal ready			RS306	A-160	
			Bit 3-synchronous mode			RS306	A-160	
			Bit 4-external clock			RS306	A-160	
			Bit 5-data rate select			RS306	A-160	
			Bit 6-oscillator select 1			RS306	A-160	
			Bit 7-oscillator select 2			RS306	A-160	
1570	0X03	Ensure that the low priority bit (IN X'42', byte 1, bit 0) can be set by issuing OUT X'42' with that bit on.	Either the low priority bit failed to set or other bits turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 0 on indicates the low priority bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS304 RS107	A-170, A-260	Pretest error. Rerun routine 154A.
1570	0X04	Ensure that a bit service interrupt occurs within one scanner pass after issuing OUT X'47' to a line address set to low priority.	By the time the OUT X'47' was issued, the allow low priority latch should have set and allowed the forced bit service. No interrupt occurred. Reg. X'11' contains the line (BCB) address from which bit service was forced.	Y4G2		RS305	A-040	Test error. Problem is probably in the CS near the allow low priority latch on ALD and FETMM pages given. (If byte 0, bit 1 of reg. X'43' is on, rerun routines 1512 and 1514. A feedback error has occurred and this error is invalid.)
1572	XXXX	Diagnostic Bit Service (Test #1): Test all addresses individually to ensure that diagnostic bit service causes a bit service level 2 interrupt from each. This is accomplished by stopping the scanner (via OUT X'47') at the address just preceding the one tested, setting diagnostic bit service, and resetting the forced interrupt. The address under test should interrupt immediately.						
1572	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1572	0X02	Ensure that setting diagnostic bit service (Byte 1, bit 0 of OUT X'44') will cause a level 2 interrupt as soon as the scanner is started from a previous stop.	A level 2 interrupt failed to occur after setting diagnostic bit service.	Y4E2 Y4G2		RS105 RS305	A-300 A-040	Test error. Problem is probably failure of the diagnostic bit service latch to set. (If needed, reg. X'13' contains the address of the line expected to interrupt.)

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1572	0X03	Ensure that the interrupt which just occurred was from the address expected.	The address received by an IN X'41' indicated the scanner stopped at the wrong address. Reg. X'13' contains the line (BCB) address expected. Reg. X'14' contains the address received by the IN X'41'. (Not valid if byte 0, bit 0 is off.)	Y4G2		RS301, RS302	A-140	Test error. Display reg. X'43'. If byte 0, bit 1 is on, a feedback check has occurred. Rerun routines 1512 and 1514. If not, the scan counter is probably not incrementing properly.
1574	XXXX	Diagnostic Bit Service (#Test #2): Ensure that after diagnostic bit service has been set, all line addresses present a bit service interrupt in address order. This is accomplished by forcing bit service (via OUT X'47') from line (BCB) address X'0BF0' and then setting diagnostic bit service. All addresses should then interrupt in address order from 0 thru to 64. (This allowed to occur twice.)						
1574	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1574	0X10 thru 0X8F	Ensure that after setting diagnostic bit service, all addresses interrupt in address order through two successive passes of the scanner. (To facilitate a scope loop, the error code is incremented just before each interrupt is expected.)	A line did not interrupt in address order. Reg. X'13' contains the line address expected to interrupt. (If byte 0, bit 5 is on, this was the second pass.) Byte 0, bit 0 of reg. X'15' describes the error. If on, no interrupt was received at all. If off, the wrong address interrupted. (See reg. X'14' for interrupting address.)	Y4G2		RS305 RS301, RS302		Test error. Problem is within the CS, probably in the scan counter. (However, if interrupt was received from wrong address, display reg. X'43'. If byte 0, bit 1 is on, a feedback check has occurred and stopped the scanner from incrementing. Rerun routines 1512 and 1514.)
1576	XXXX	High-Low Priority Test: Ensure the proper operation of the priority counter and control circuits. This is accomplished in two ways after having set all lines to low priority. First, a check is made to ensure that with all lines set to low priority and utilizing the diagnostic bit service function, each address interrupts in address order. Secondly, after the first pass, as each line interrupts, its priority is changed to high. This should cause the next interrupt to be from the same address. The address's priority is then changed back to low to allow the next address to interrupt. This is done through all 64 addresses. (Note: To determine at an error stop which of the above tests was in progress, display reg. X'13'. If contents are X'0000', first test was in progress. If not, the second test was.)						
1576	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1576	0X02	Ensure that the low priority bit (IN X'42', byte 1, bit 0) can be set by issuing OUT X'42' with that bit on.	Either the low priority bit failed to set or other bits turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in	Y4G2 Y4E2	03FF	RS304 RS107	A-170, A-260	Pretest error. Rerun routine 154A.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			error. (Byte 1, bit 0 on indicates the low priority bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.					
1576	0X03	Ensure a bit service level 2 interrupt occurs from each line as it is expected (described in the description for this routine, see 1576, XXXX, above.)	No interrupt was received from the expected address. Reg. X'15' describes the error. If byte 0, bit 0 is on, no interrupt was received at all. If off, the wrong address interrupted. Reg. X'11' contains the address expected to interrupt. Reg. X'14' contains the interrupting address.	Y4G2		RS305	A-040	Test error. Priority counter is probably at fault. (However, if interrupt occurred from the wrong address, display reg. X'43'. If byte 0, bit 1 is on, a feedback check has occurred and stopped the scanner from incrementing. Rerun routines 1512 and 1514.)
1576	0X04	Ensure that the low priority bit (IN X'42', byte 1, bit 0) can be set by issuing OUT X'42' with that bit on.	Either the low priority bit failed to set or other bits turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 0 on indicates the low priority bit failed.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS304 RS107	A-170, A-260	Test error. Rerun routines 154A and 154C.
1576	0X05	Ensure that the low priority bit can be reset via OUT X'42'.	After having set the low priority bit, an attempt to reset it was made via OUT X'42' with byte 1, bit 0 off. An IN X'42' then indicated the bit was still on (or other bits were set in error). Reg. X'15' contains the bits in error. Byte 1, bit 0 on indicates that the low priority bit failed to reset. Reg. X'11' contains the line (BCB) address tested.	Y4G2	03FF	RS304	A-170 A-260	Test error. Rerun routines 154A and 154C.
1578	XXXX	Set Data Set Ready, Carrier Detect, and Clear-to-Send (via diagnostic mode): Ensure that after setting a line to diagnostic mode and setting on request-to-send, data set ready, carrier detect, and clear-to-send are on. This test is run on all installed adapters except autocall, in turn. (This test can only ensure that these lines have been set. Due to the actual hardware, it cannot determine if diagnostic mode or the actual presence of the signal on the communications line set them.)						
1578	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1578	0X02	Ensure that the diagnostic mode bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 1 on.	Either the diagnostic mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 1 on indicates a diagnostic mode bit failure.) Reg. X'14'	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Test error. Problem is probably in the associated line adapter. (See General Comments, #3.) If other bits are on in error, some kind

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			contains the actual data received by the IN X'42'.					of interaction occurred. If byte 1, bit 1 is on in both Regs. X'15' and X'14', the line adapter tested was an autocall adapter and the diagnostic mode bit set and should not have.
1578	0X03	Ensure that the request-to-send/NBR-2 bit can be set by issuing an OUT X'43' with byte 1, bit 6 on.	Either the request-to-send/NBR-2 bit failed to set or other bits were set in error in the IN X'43'. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in IN X'43' in error. (Byte 0, bit 6 on indicates a request-to-send/NBR-2 bit set failure.)	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. The problem probably is in the associated line adapter. (See General Comments, #3.) If other bits are in error, some kind of interaction problem exists. Reg. X'14' contains the actual data received by the IN X'43'.
1578	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Test error. Rerun routine 1512.
1578	0X05	Ensure that setting diagnostic mode sets clear-to-send in IN X'43' (byte 1, bit 0 off) if request-to-send is already on.	After setting diagnostic mode and request-to-send, and forcing the scanner to again stop at the tested address, an IN X'43' indicated that clear-to-send was still off (or diagnostic mode or request-to-send had dropped). Reg. X'15' contains the bits in error. Byte 1, bit 0 on indicates clear-to-send failed to set. Reg. X'14' contains the data received by the IN X'43'.	Y4G2	0284	RS307	A-180, A-200	Test error. Failure is in the CS, however, if needed, reg. X'11' contains the line (BCB) address under test. If reg. X'15' indicates that diagnostic mode or request-to-send have dropped (byte 1, bit 5 or byte 0, bit 6, respectively), rerun routines 153E and 1526.
1578	0X06	Ensure that diagnostic mode sets data set ready in IN X'43' (byte 1, bit 2 off).	The same IN X'43' described in error 0X05, above, indicated that data set ready was not set by setting diagnostic mode. Reg. X'14' contains the received IN X'43' data.	Y4G2	0020	RS307	A-180	Test error. As above, failure is in the CS. Reg. X'11' contains the tested line address.
1578	0X07	Ensure that diagnostic mode sets carrier detect in IN X'43'.	Byte 1, bit 3 of the same IN X'43' in error 0X05, above, was off indicating that carrier detect was not set by diagnostic mode. Reg. X'14' contains the received IN X'43' data.	Y4G2	0010	RS307	A-180, A-200	Test error. As above, failure is in the CS. Reg. X'11' contains the tested line address, if needed.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
157A	XXXX	Feedback Error (Test #1): After the CS has been reset, the scanner is stopped at the tested line address and a check made to ensure that issuing an OUT X'43' with the transmit mode and send data bits on (transmit-mark) does not cause a feedback check. After testing all installed adapters except autocall, the entire test is run again but with send data off (transmit space).						
157A	0X02	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
157A	0X04	Before continuing the test, ensure that a feedback error is not already indicated.	After stopping the scanner at the tested address, an IN X'43' indicated a feedback error. (Byte 0, bit 1 was on.) (Reg. X'14' contains the result of the IN X'43'.)	Y4F2	4000	RS202	A-200	Pretest error. Rerun routine 1518.
157A	0X06	Before checking for feedback error, ensure via IN X'43', that the transmit mode and send data bits were properly set.	Either the transmit mode bit failed to set or the send data bit failed to act correctly. Reg. X'15' contains the bits in error. Byte 0, bit 4 on on indicates the transmit mode bit failed to set. Byte 0, bit 7 on indicates a send data bit failure. (Reg. X'14' contains the data received by the IN X'43'.)	Y4G2	0900	RS308	A-200	Test error. Rerun routine 151A if transmit mode bit failed and routines 1522 and 1524 if the send data bit failed.
157A	0X08	Ensure that issuing OUT X'43' with transmit-mark or transmit-space set, does not cause a feedback error.	After setting transmit mode and mark or space, the IN X'43' described in error 0X06, above, indicated a feedback check occurred. (Byte 0, bit 1 of the IN X'43' was on.) Reg. X'14' contains the received IN X'43' data. If byte 1, bit 7 of Reg. X'13' is on, send data was on (mark). If not, it was off (space).	Y4E2 Y4F2	4000	RS104 RS202	A-200	Test error. Problem is probably in the feedback error detection circuits in the CS. (See General Comments, #3.) If problem appears not to be in the CS, rerun routines 1522 and 1524 before proceding. If needed, Reg. X'11' contains the line address under test.
157C	XXXX	Feedback Error (Test #2): Ensure the ability of the feedback error detection circuitry to detect a feedback check thus preventing a bit service level 2 reset, and the ability to reset a feedback error. This is accomplished by resetting the scanner (keeping the LIBs disabled), forcing the scanner to stop at the tested address, attempting to set transmit mode and space via an OUT X'43' and checking that no feedback error occurs and that the bit service can be reset. The scanner is again stopped at the tested address and an attempt made to set transmit mode and mark. This time a feedback error should occur (since the LIB is disabled) and the level 2 interrupt should not reset. An attempt is then made to reset the feedback error and a check made that the level 2 interrupt can now be reset. (This test is run on all addresses.)						
157C	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
157C	0X02	Before continuing the test, ensure that attempting to set transmit mode and space, via OUT X'43', does not	After issuing an OUT X'43' to the line under test (Reg. X'11'), with only the transmit mode bit on (byte 1, bit 4)		4900		A-200	Pretest error. If Reg. X'15', byte 0, bits 4 or 7 are on,

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		cause a feedback error to occur.	(send data off=space), an IN X'43' indicated that either a feedback check occurred, transmit mode bit did set (it should not have since the LIBs were disabled), or send data erroneously set. Reg. X'14' contains the actual data received by the IN X'43'. Reg. X'15' contains the bits in error:					ignore bit 2. If rerunning the routines specified failes to locate the problem, a LIB may be enabled in error. Try replacing Y4F2, ALD page RS206, FETMM page A-310.
			Byte 0:					
			Bit 1-feedback check was on.	Y4F2		RS202	A-240	Rerun routine 157A.
			Bit 4-transmit mode bit set.	Y4G2		RS307		Rerun routine 151A.
			Bit 7-send data bit was set.	Y4G2		RS307		Rerun routine 1522.
157C	0X03	Ensure that with no feedback error present, the bit service level 2 interrupt that was forced can be reset.	An IN X'77' following an OUT X'41' to reset bit service, indicated a level 2 interrupt was still present.	Y4G2	4000	RS305	A-040	Pretest error. Rerun routine 1514.
157C	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
157C	0X05	Ensure that attempting to set transmit mode and mark (byte 1, bits 4 and 7 of an OUT X'43') on a line on a disabled LIB, causes a feedback check to occur.	After stopping the scanner and issuing the OUT X'43', an IN X'43' indicated that a feedback error failed to occur (or the transmit mode or send data bits set erroneously). Reg. X'15' contains the bits in error:		4900		A-200	Test error. If Reg. X'15', byte 0, bit 4 or 7 are on, ignore bit 1 and rerun the specified routines. (See error code
			Byte 0:					
			Bit 1-a feedback error failed to occur.	Y4F2		RS202		0X02, above.)
			Bit 4-the transmit mode bit set.	Y4G2		RS307		Rerun routine 151A.
			Bit 7-the send data bit set.	Y4G2		RS307		Rerun routine 1522.
157C	0X06	Ensure that after a feedback error has occurred, the bit service level 2 interrupt cannot be reset.	After forcing a feedback check (see above), an OUT X'41' was issued to attempt to reset the level 2 interrupt and start the scanner. A following IN X'77' no longer indicated a pending level 2 interrupt and should have.	Y4F2	4000	RS202	A-240	Test error. Feedback error has apparently failed to block the 'start scanner' line on ALD page given.
157C	0X07	Ensure that after a feedback error has occurred, an OUT X'44' with byte 1, bit 6 (reset feedback error) can reset it.	An IN X'43' following the OUT X'44' still indicated a feedback error. Reg. X'14' contains the results of the IN X'43'. Byte 0, bit 2 on indicates the feedback error reset failure.	Y4E2	4900	RS105	A-300	Test error.
157C	0X08	Ensure that now that the feedback error has been reset, an OUT X'41' can reset the level 2 interrupt.	After resetting the feedback, check an OUT X'41' (reset bit service) was issued and a following IN X'77' still indicated a level 2 interrupt present. Reg. X'14' contains the IN X'77' data.	Y4F2 Y4G2	4000	RS202 RS305	A-240	Test error. The 'start scanner' line on ALD pages given failed to come up.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
157E	XXXX	LIB Bit Clock Check: Enable a LIB and check to ensure that no LIB bit clock error is indicated for any LIB. (This test is run four times; once for each LIB.)						
157E	0X02	Before enabling any LIB, ensure that no bit clock is indicated.	After having reset and enabled the scanner, an IN X'44' indicated a LIB bit clock check even though all LIB's were disabled. Reg X'14' contains the results of the IN X'44': Byte 1: Bit 2-LIB 1 bit clock check Bit 3-LIB 2 bit clock check Bit 4-LIB 3 bit clock check Bit 5-LIB 4 bit clock check	Y4F2	003C	RS206	A210 A220	Pretest error. Rerun routines 1504 through 150A.
157E	0X04	Ensure that with any LIB enabled no bit clock check is indicated for the first LIB.	After enabling a LIB, the LIB 1 bit clock check bit was on in an IN X'44'. Reg. X'14' contains the results of the IN X'44'. Byte 0, bits 6 and 7 indicate which LIB was enabled; '00', '01', '10', and '11' for LIB's 1, 2, 3, and 4 respectively.	Y4F2	0020	RS206	A-210 A-220	Test error. If the first LIB was the one that was enabled, suspect a failure in that LIB's bit clock control card.
157E	0X06	Ensure that with any LIB enabled no bit clock check is indicated for the second LIB.	After enabling a LIB, the LIB 2 bit clock check bit was on in an IN X'44'. Reg. X'14' contains the results of the IN X'44'. Byte 0, bits 6 and 7 indicate which LIB was enabled; '00', '01', '10', and '11' for LIB's 1, 2, 3, and 4 respectively.	Y4F2	0020	RS206	A-210 A-220	Test error. If the second LIB was the one that was enabled, suspect a failure in that LIB's bit clock control card.
157E	0X08	Ensure that with any LIB enabled no bit clock check is indicated for the third LIB.	After enabling a LIB, the LIB 3 bit clock check bit was on in an IN X'44'. Reg. X'14' contains the results of the IN X'44'. Byte 0, bit 6 and 7 indicate which LIB was enabled; '00', '01' '10', and '11' for LIB's 1, 2, 3, and 4 respectively.	Y4F2	0020	RS206	A-210 A-220	Test error. If the third LIB was the one that was enabled, suspect a failure in that LIB's bit clock control card.
157E	0X0A	Ensure that with any LIB enabled no bit clock check is indicated for the fourth LIB.	After enabling a LIB, the LIB 4 bit clock check bit was on in an IN X'44'. Reg. X'14' contains the results of the IN X'44'. Byte 0, bit 6 and 7 indicate which LIB was enabled; '00', '01', '10', and '11' for LIB's 1, 2, 3, and 4 respectively.	Y4F2	0020	RS206	A-210 A-220	Test error. If the fourth LIB was the one that was enabled, suspect a failure in that LIB's bit clock control card.
1580	XXXX	Oscillator Interrupt Test (or Monitor Mode 11): By setting monitor mode 11 (allow normal bit service requests) and checking for a bit service level 2 interrupt from each installed adapter, ensure that all oscillators can cause a bit service interrupt from all installed adapters. (This test runs first with oscillator 0 and each line, first in receive and then in transmit mode. It then tests all other installed oscillators with each installed adapter except autocall.)						
1580	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11',	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
1580	0X02	Ensure that an OUT X'42' has set mode 11 and has properly selected an oscillator.	After stopping the scanner and issuing an OUT X'42', an IN X'42' indicated that mode 11 was not set or the proper oscillator select bits were not set (or other bits were set in error). Reg. X'14' contains the actual data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Rerun routines specified below. Reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode set in error.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select bit set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 failed to set or was set in error.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed to set or was set in error.			RS306	A-160	Rerun routines 1546 and 1548.
1580	0X03	Ensure that an OUT X'43' has set transmit or receive mode.	After issuing an OUT X'43' to the line under test, an IN X'43' indicated that the transmit mode bit failed to set or reset. Reg. X'14' contains the received IN X'43' data. The transmit mode bit (byte 0, bit 4) should have been the opposite of what it was.	Y4G2	0800	RS308	A-200	Pretest error. Rerun routines 151A and 151C.
1580	0X2X	The remaining error codes in this routine are basically the same, changing to indicate the oscillator selected at time of failure and to indicate whether the failure occurred while in transmit or receive mode. The majority of failures detected by this routine will be caused by a faulty line adapter, but may be caused by a LIB failure or the CS itself. (See general comments, #3.) If all lines fail in both transmit and receive modes and with all oscillators, suspect card at location Y4G2, ALD page RS305. If all lines fail with a given oscillator, regardless of mode, replace cards Y4H2 and Y4J2 for oscillators 0 or 1 and 2 or 3, respectively. If all lines fail on one LIB in transmit mode only, replace the LIB ISOLATION CARD. If all lines on one LIB fail in receive mode only, replace the LIB BIT CLOCK CONTROL CARD. If only one line fails, replace the line interface card for that address.					
1580	0X20	co off Ensure that the first error. oscillator can create a Reg. X'11' strobe in a line adapter the line set to receive mode, under causing a bit service (See level 2 interrupt. following the	After having set monitor oscillator 0, setting receive mode, starting the scanner, and waiting a maximum of 30 milliseconds for a bit for service interrupt from the code 0X03 line under test, none occurred. routine.)	Y4H2 mode 11 to allow normal bit service requests, selecting		RS401	Y4G2	Test RS305 A-040 contains address test. note description error of this

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1580	0X21	Ensure that the first error. oscillator can create a X'11' strobe in a line adapter the line set to transmit mode, under causing a bit service (See level 2 interrupt. following the	After having set monitor mode requests, selecting oscillator 0, setting transmit mode, starting the scanner, and waiting a maximum of 30 milliseconds for a bit service interrupt from for the line adapter under test, code 0X03 none occurred. routine.)	Y4H2 11 to allow normal bit service		RS401	A-040	Test Reg. contains address test. note description error of this
1580	0X22	Ensure that the second error. oscillator can create a X'11' strobe in a line adapter the line set to receive mode, service (See level 2 interrupt. following	After having set monitor mode requests, selecting oscillator 1, setting receive mode, starting the scanner, and waiting a maximum of 30 milliseconds for a bit service interrupt from description the line under test, none error code occurred. this	Y4H4 11 to allow normal bit service address under causing a bit		RS402	A-040	Test Reg. contains test. note the for 0X03 of routine.)
1580	0X23	Ensure that the second error. oscillator can create a X'11' strobe in a line adapter the line set to transmit mode, under causing a bit service (See level 2 interrupt. following	After having set monitor mode requests, selecting oscillator 1, setting transmit mode, starting the scanner, and waiting a maximum of 30 milliseconds for a bit service interrupt description from the line under test, error code none occurred. this	Y4H4 11 to allow normal bit service		RS402	A-040	Test Reg. contains address test. note the for 0X03 of routine.)
1580	0X24	Ensure that the third error. oscillator can create a X'11' strobe in a line adapter the line set to receive mode, under causing a bit service (See level 2 interrupt. following	After having set monitor mode requests, selecting oscillator 2, setting receive mode, starting the scanner, and waiting a maximum of 30 milliseconds for a bit service description interrupt from the line under error code test, none occurred. this	Y4J2 11 to allow normal bit service		RS403	A-040	Test Reg. contains address test. note the for 0X03 of routine.)
1580	0X25	Ensure that the third error. oscillator can create a X'11' strobe in a line adapter the line set to transmit mode, under causing a bit service (See level 2 interrupt. following	After having set monitor mode requests, selecting oscillator 2, setting transmit mode, starting the scanner, and waiting a maximum of 30 milliseconds for a bit description service interrupt from the error code line under test, none this occurred.	Y4J2 11 to allow normal bit service		RS403	A-040	Test Reg. contains address test. note the for 0X03 of routine.)
1580	0X26	Ensure that the fourth error. oscillator can create a X'11' strobe in a line adapter the line set to receive mode, under causing a bit service (See level 2 interrupt. following	After having set monitor service requests, selecting oscillator 3, setting receive mode, starting the scanner, and waiting a maximum of 30 milliseconds for a bit description service interrupt from the error code line under test, none this occurred.	Y4J4 11 to allow normal bit		RS404	A-040	Test Reg. contains address test. note the for 0X03 of routine.)

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1580	0X27	Ensure that the fourth error. oscillator can create a X'11' strobe in a line adapter service requests, selecting the line set to transmit mode, oscillator 3, setting transmit under causing a bit service mode, starting the scanner, and (See level 2 interrupt. waiting a maximum of 30 following milliseconds for a bit service description interrupt from the line under error code test, none occurred. this	After having set monitor mode	Y4J4 11 to allow normal bit		RS404	A-040	Test Reg. contains address test. note the for 0X03 of routine.)
1580	0X30	Ensure that after a bit error. service level 2 interrupt the has been caused by a strobe service in a line adapter, the 'bit was not service' bit in IN X'43' is onto the set. during the	After receiving a normal bit the actual data received by the IN X'43'.	Y4G2 service request from a line set to monitor mode 11, byte 1, bit 6 of an IN X'43' was not set. Reg. X'14' contains	0002	RS307	A-200	Test Apparently, bit bit gated inbus IN X'43'. (If needed, Reg. X'11' contains the line address under test.)
1582	XXXX	Reset Interface Bit Service Request: After the CS has been reset, the tested line address is set to mode 11, oscillator 0 selected, and a bit service level 2 interrupt caused by a strobe in the line adapter is allowed to occur. An OUT X'41' or X'46' is issued in an attempt to reset the interface bit service and a check made to ensure that it did. Also, if the bit service failed to reset, a check is made to ensure that a feedback occurs. (This test runs on each installed line adapter, first using OUT X'41' then OUT X'46', in turn.)						
1582	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1582	0X02	Ensure that an OUT X'42' has set mode 11 and has properly selected an oscillator.	After stopping the scanner and issuing an OUT X'42', an IN X'42' indicated that mode 11 was not set or the proper oscillator select bits were not set (or other bits were set in error). Reg. X'14' contains the actual data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Rerun routines specified below. Reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode set in error.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select bit set in error.			RS306	A-160	Rerun routines 152E and 1530.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 6-oscillator select bit 1 failed to set or was set in error.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed to set or was set in error.			RS306	A-160	Rerun routines 1546 and 1548.
1582	0X03	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner, and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-040	Pretest error. Rerun routine 1580.
1582	0X04	Ensure that if a reset bit service fails to do so, then a feedback check will occur.	After a failing attempt to reset an interface bit service request, an IN X'43' failed to indicate a feedback error. (Byte 0, bit 1 was off.)	Y4F2 Y4E2		RS202 RS104	A-240	Test error. Since feedback errors of this type cannot be forced, this problem should be fixed before the problem of the reset failing.
1582	0X05	Ensure that an OUT X'41' or X'46' can reset a bit service level 2 request.	After allowing a bit service level 2 request to cause an interrupt, an IN X'77' following an OUT X'41' or X'46' still indicated that a type 1 CS level 2 request was present. (Byte 0, bit 1 was on.) Reg. X'11', if needed, contains the line address under test. If byte 0, bit 3 of that Reg. is off, the reset attempted was an OUT X'41'. If not, it was an OUT X'46'.	Y4F2 Y4E2		RS202 RS104	A-240 A-320	Test error. Although this error code has been designated as a test error, the reset circuitry it tests has previously been tested. Rerun routine 1514.
1582	0X06	Ensure that in addition to resetting a bit service level 2 interrupt, an OUT X'41' or X'46' can reset the interface bit service request that caused the level 2.	After resetting the level 2 interrupt and thus starting the scanner, another bit service interrupt from the same line occurred within the next pass of the scanner. This indicated that the interface bit service request in the tested line adapter was not reset. Reg. X'11' contains the line (BCB) address under test. (If byte 0, bit 3 of that Reg. is off, the reset tried was an OUT '41'. If not, it was an OUT X'46'.)	Y4G2		RS308	A-240 A-320	Test error. Failure may be in the CS, the LIB, or line adapter. (See General Comments, #3.) However, if failure occurs with only one of the output instructions, problem is probably in instruction decode. Try rerunning routine 1514.
1584	XXXX	Disable Level 2 Interrupts (or via monitor mode 11, they can line adapters, in turn.)	Monitor Mode 00): Ensure that once normal bit service requests are allowed again be disabled via monitor mode 00. (This test is run on all installed					
1584	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1584	0X02	Ensure that an OUT X'42' has set mode 11 and has	After stopping the scanner and issuing an OUT X'42', an IN	Y4G2	03FF		A-150	Pretest error. Rerun routines

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		properly selected an oscillator.	X'42' indicated that mode 11 was not set or the proper oscillator select bits were not set (or other bits were set in error). Reg. X'14' contains the actual data received by the IN X'42'. Reg. X'15' contains the bits in error:					specified below. Reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode set in error.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select bit set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 failed to set or was set in error.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed to set or was set in error.			RS306	A-160	Rerun routines 1546 and 1548.
1584	0X03	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner, and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-040	Pretest error. Rerun routine 1580.
1584	0X04	Ensure that once monitor mode 11 has allowed normal bit service requests, they can again be disabled via monitor mode 00.	After having insurred that monitor mode 11 allowed at least one normal bit service request, an OUT X'42' was issued to set mode 00 (disable level 2 interrupts). Another bit service interrupt from the same line address then occurred. Reg. X'11' contains the line address under test.	Y4G2		RS305	A-040	Test error. Although this failure is designated as a test error, the separate functions have been previously tested. Display Reg. X'42'. If bits 6 or 7 of byte 0 are on, rerun routines 154E thru 1554. If not, rerun routine 1511.
1586	XXXX	Bit Overrun (Test #1): After the CS has been reset, the scanner is stopped at the tested address, and mode 11 (allow normal bit service requests) is set along with transmit or receive mode. The scanner is again started and when the next interrupt occurs from that line, a test is made to ensure that no bit overrun is present. (This test is run on all installed line adapters, in turn, in receive mode and then, in turn, in transmit mode.)						
1586	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
1586	0X02	Ensure that an OUT X'42' has set mode 11 and has properly selected an oscillator.	After stopping the scanner and issuing an OUT X'42', an IN X'42' indicated that mode 11 was not set or the proper oscillator select bits were not set (or other bits were set in error). Reg. X'14' contains the actual data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150 A-340	Pretest error. Rerun routines specified below. Reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode set in error.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select bit set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 failed to set or was set in error.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed to set or was set in error.			RS306	A-160	Rerun routines 1546 and 1548.
1586	0X03	Ensure that an OUT X'43' has set transmit or receive mode.	After issuing an OUT X'43' to the line under test, an IN X'43' indicated that the transmit mode bit failed to set or reset. Reg. X'14' contains the received IN X'43' data. The transmit mode bit (byte 0, bit 4) should have been the opposite of what it was.	Y4G2	0800	RS308	A-200 A-340	Pretest error. Rerun routines 151A and 151C.
1586	0X05	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner, and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-040	Test error. Although this failure is designated as a test error, this function has been previously tested. Rerun routine 1580.
1586	0X06	Ensure that no bit overrun is present after allowing a normal bit service request to cause a level 2 interrupt.	After setting mode 11 along with transmit or receive mode and allowing a level 2 interrupt to occur from the line under test, an IN X'43' indicated an overrun condition (byte 1, bit 7 was on) or did not indicate an interface bit service request (byte 1, bit 6 was off). Reg. X'14' contains the actual IN X'43' data received and Reg. X'15' indicates which bit was in error.	Y4G2	0003	RS308	A-200	Test error. Problem is probably in a line adapter. (See General Comments, #3.) If bit service bit failed to be set in IN X'43', rerun routine 1580.

1588 XXXX Bit Overrun (Test #2): After the CS has been reset, the scanner is stopped at the tested address, and mode 11 (allow normal bit service requests) is set along with receive or transmit mode. The scanner is then started and a normal bit service level 2 interrupt allowed to occur. After ensuring that no overrun was already present, the scanner is started again and no level 2 interrupts are allowed for at least 2 bit

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		times. Level 2 interrupts are then unmasked and a level 2 interrupt from the tested address is allowed. After checking that a level 2 from that line did occur, a check is made to ensure that bit overrun was set and that it can then be reset. (This test is run on all line adapters, in turn, first in receive and then in transmit mode.)						
1588	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
1588	0X02	Ensure that an OUT X'42' has set mode 11 and has properly selected an oscillator.	After stopping the scanner and issuing an OUT X'42', an IN X'42' indicated that mode 11 was not set or the proper oscillator select bits were not set (or other bits were set in error). Reg. X'14' contains the actual data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Rerun routines specified below. Reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode set in error.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select bit set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 failed to set or was set in error.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed to set or was set in error.			RS306	A-160	Rerun routines 1546 and 1548.
1588	0X03	Ensure that an OUT X'43' has set transmit or receive mode.	After issuing an OUT X'43' to the line under test, an IN X'43' indicated that the transmit mode bit failed to set or reset. Reg. X'14' contains the received IN X'43' data. The transmit mode bit (byte 0, bit 4) should have been the oppcsite of what it was.	Y4G2	0800	RS308	A-200	Pretest error. Rerun routines 151A and 151C.
1588	0X05	Ensure that the first oxcillator has created a strobe and caused a bit service level 2 interrupt.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner, and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-040	Pretest error. Rerun routine 1580.
1588	0X06	Ensure that no bit overrun is present after allowing a normal bit service request to cause a level 2 interrupt.	After setting mode 11 along with transmit or receive mode and allowing a level 2 interrupt to occur from the line under test, an IN X'43'	Y4G2	0003	RS308	A-200	Pretest error. Rerun routine 1586.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			indicated an overrun condition (byte 1, bit 7 was on) or did not indicate an interface bit service request (byte 1, bit 6 was off). Reg. X'14' contains the actual IN X'43' data received and Reg. X'15' indicates which bit was in error.					
1588	0X07	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner, and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-040	Test error. Although this failure is designated as a test error, this function has been previously tested. Rerun routine 1580.
1588	0X10	Ensure that after waiting more than two bit times and not allowing any level 2 interrupts, that when a level 2 interrupt is allowed, bit overrun has been set in the line adapter. (Line adapter was in receive mode.)	After allowing an interrupt, an IN X'43' indicated no bit overrun (or no interface bit service request). Reg. X'14' contains the received IN X'43' data. Reg. X'15' contains the bits in error. If byte 1, bit 7 is on, bit overrun failed to set. If byte 1, bit 6 is on, no interface bit service request was indicated. Reg. X'11' contains the line address under test.	Y4G2	0003	RS308	A-200	Test error. Failure is probably in the associated line adapter. (See General Comments, #3.) If no interface bit service request was present, rerun routine 1580.
1588	0X20	Ensure that after waiting more than two bit times and not allowing any level 2 interrupts, that when a level 2 interrupt is allowed, bit overrun has been set in the line adapter. (Line adapter was in transmit mode.	After allowing an interrupt, an IN X'43' indicated no bit overrun (or no interface bit service request). Reg. X'14' contains the received IN X'43' data. Reg. X'15' contains the bits in error. If byte 1, bit 7 is on, bit overrun failed to set. If byte 1, bit 6 is on, no interface bit service request was indicated. Reg. X'11' contains the line address under test.	Y4G2	0003	RS308	A-200	Test error. Failure is probably in the associated line adapter. (See General Comments, #3.) If no interface bit service request was present, rerun routine 1580.
1588	0X40	Ensure that bit overrun in a line adapter can be reset. (Line adapter set to receive mode.)	After forcing a bit overrun to occur, an OUT X'44' with byte 1, bit 7 on was issued to attempt to reset the overrun. An IN X'43' then indicated that bit overrun (byte 1, bit 7) was not reset (or bit service request erroneously was). Reg. X'14' contains the received IN X'43 data. Reg. X'15' contains the error bits. Byte 1, bit 7 on indicates a bit overrun reset failure and bit 6 on indicates bit service request was not set. Reg. X'11' contains the line address under test.	Y4E2	0003	RS105	A-300	Test error. Failure may also be in LIB or line adapter. (See General Comments, #3.) If bit service request was in error, rerun routine 1580 before attempting to isolate overrun reset failure.
1588	0X80	Ensure that bit overrun in a line adapter can be reset. (Line adapter set to transmit mode.)	After forcing a bit overrun to occur, an OUT X'44' with byte 1, bit 7 on was issued to attempt to reset the overrun. An IN X'43' then indicated that bit overrun (byte 1, bit 7) was not reset (or bit service request erroneously was). Reg. X'14' contains the received IN X'43' data. Reg. X'15'	Y4E2	0003	RS105	A-300	Test error. Failure may also be in LIB or line adapter. (See General Comments, #3.) If bit service request was in error, rerun routine 1580

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			contains the error bits. Byte 1, bit 7 on indicates a bit overrun reset failure and bit 6 on indicates bit service request was not set. Reg. X'11' contains the line address under test.					before attempting to isolate overrun reset failure.
158A	XXXX	Send Data From All Positions: Check the ability of all installed non-autocall line adapters to send both a mark and space to all others. The scanner is first stopped at one address, and it is set to diagnostic and receive modes and monitor mode 11. The scanner is then started and stopped at another address. This address is set to diagnostic mode and monitor mode 11. The scanner is again started and stopped at this address, transmit mode is set, and send data is set to mark or space. Since this time has already been set to diagnostic mode, setting transmit mode should set the test data latch in the CS to the same state as send data. The scanner is again started and two normal bit service requests from the receive line are allowed to interrupt. (The first interrupt is ignored and reset to clear out any pending bit service requests that may have occurred while setting up the transmit line.) A check is then made to ensure that the strobe that caused the second one set the receive data latch in the receive line adapter to the same state as the test data latch (which was set by the transmit line). This test is run first using the first installed non-autocall adapter as the transmit line and, one at a time, using all others to receive. It is then run using the second one as the transmit line, etc. Each receive line is first tested to receive a space and then again to receive a mark.						
158A	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
158A	0X02	Before continuing, ensure that the receive line has been set to diagnostic mode and monitor mode 11.	After stopping the scanner at the tested address and issuing an OUT X'42' to set the proper modes, an IN X'42' indicated a failure to do so. Reg. X'14' contains the data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150 A-340	Pretest error. Reg. X'11' contains line address under test. Rerun the appropriate routine.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 1516,154A, & 154C.
			Bit 1-diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1516,1532,&1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 1516,152A,&152C.
			Bit 4-external clock set in error.			RS306	A-160	Rerun routines 1516,1536,&1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 1516,152E,&1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1516,1542,&1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1516,1546,&1548.
158A	0X03	Before continuing, ensure that the receive line has been set to receive mode.	While the scanner was stopped at the tested address, an OUT X'43' was issued with all bits off to ensure the line to be in receive mode. An IN X'43' then indicated the line adapter was in transmit mode (byte 0, bit 4 was on).	Y4G2	0800	RS308	A-200 A-340	Pretest error. Rerun routine 151C. Reg. X'14' contains the received IN X'43' data and reg. X'11' contains the line address under test.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
158A	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
158A	0X05	Before continuing, ensure that the transmit line has been set to diagnostic mode and monitor mode 11.	After stopping the scanner at the tested address and issuing an OUT X'42' to set the proper modes, an IN X'42' indicated a failure to do so. Reg. X'14' contains the data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150 A-340	Pretest error. Reg. X'11' contains line address under test. Rerun the appropriate routine.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 1516,154A,&154C.
			Bit 1-diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1516,1532,&1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 1516,152A,&152C.
			Bit 4-external clock set in error.			RS306	A-160	Rerun routines 1516,1536,&1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 1516,152E,&1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1516,1542,&1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1516,1546,&1548.
158A	0X06	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
158A	0X07	Ensure that the transmit line has now been properly set to transmit mode and send data (and thus the test data latch) has been set to the proper state.	After having stopped the scanner at the transmit address for the second time and issuing an OUT X'43' to set send data to a mark or space and to set transmit mode, an IN X'43' indicated the transmit line had not been properly set up. Reg. X'11' contains the line address under test. Reg. X'14' contains the actual data received by the IN X'43'. Reg. X'15' contains the bits in error:	Y4G2, Y4F2	4904		A-200 A-350	Pretest error. Rerun the appropriate routine given.
			Byte 0:					
			Bit 1-a feedback check occurred when the OUT X'43' was issued.			RS202		Rerun routines 157A and 157C.
			Bit 4-transmit mode bit failed to set.			RS308		Rerun routines 151A and 151C.
			Bit 7-send data did not set to the proper state.			RS308		Rerun routines 1522 and 1524.
			Byte 1:					
			Bit 5-diagnostic mode failed to set in IN X'43'.			RS307		Rerun routines 153E and 1540.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
158A	0X08	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt from the receive line.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-040	Pretest error. Rerun routine 1580.
158A	0X09	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt from the receive line again.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner, and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-040	Pretest error. Rerun routine 1580.
158A	0X0A	Ensure that (now that the receive line has had a chance to strobe in the transmitted data) data can be sent from one line to another through the use of the test data latch in diagnostic mode.	After giving the receive line a chance to strobe in the data transmitted, an IN X'43' at the time the scanner stopped indicated the data transmitted was not received. Reg. X'14' contains the received IN X'43' data. Reg. X'15' contains the bits in error (ignore byte 0, bit 0 if any others are on): Byte 0: Bit 0-received data was not the same as the data transmitted. Byte 1: Bit 5-diagnostic mode has dropped. Bit 6-interface bit service request was not present.	Y4E2	8006	RS105	A-350	Test error. If diagnostic mode or interface service request were in error, rerun routines 153E and 1580, respectively. If not problem may be in the CS, a LIB, or line adapter. (See General Comments, #3.) If problem appears to be in a LIB, try replacing the LIB isolation card first. Reg. X'11' contains the line address of the receive line. If needed, Reg. X'16' contains the storage location of the line address of the transmit line.
158C	XXXX	Test Data Latch: Ensure that setting diagnostic mode causes the test data latch to be set to a mark. After the CS has been reset, the tested line address is set to diagnostic mode and transmit space (to set the test data latch to a space). The same line is then set to receive mode and a check made that it is now receiving a space (via the test data latch). Another OUT X'42' is then issued to set diagnostic mode again and a test made to ensure that the next time the scanner is stopped at that address, it will be receiving a mark. (Note that since sending the space, send data has never changed.) (This test is run on all installed non-autocall line adapters, in turn.)						
158C	0X02	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
158C	0X03	Ensure that the diagnostic mode bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 1 on.	Either the diagnostic mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 1 on indicates a diagnostic mode bit failure.) Reg. X'14'	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 153A.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			contains the actual data received by the IN X'42'.					
158C	0X04	Ensure that once the scanner is stopped, it can be started again via OUT X'41' and then stopped again by forcing a bit service (OUT X'47') interrupt.	Either the scanner could not started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000		A-240	Pretest error. Rerun routine 1512.
			X'E000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - The OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330, A-240	
158C	0X06	Ensure that, before continuing, diagnostic mode and transmit space have been able to be set in the line adapter under test.	After setting diagnostic mode via OUT X'42', setting transmit space via OUT X'43', and then forcing the scanner to stop again, an IN X'43' indicated something was not set up correctly. Reg. X'15' contains the bits in error:	Y4G2	0904		A-200	Pretest error. Reg. X'14' contains the data received by the IN X'43'. Reg. X'11' contains the line address under test. Rerun appropriate routine as shown below.
			Byte 0:					
			Bit 4-Transmit mode failed to set.			RS308	A-340	Rerun routine 151A.
			Bit 7-Send data was not a space.			RS308	A-340	Rerun routines 1522 and 1524.
			Byte 1:					
			Bit 5-Diagnostic mode was not set in IN X'43'.			RS307	A-340	Rerun routine 153E.
158C	0X08	Ensure that once the scanner is stopped, it can be started again via OUT X'41' and then stopped again by forcing a bit service (OUT X'47') interrupt.	Either the scanner could not started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000		A-240	Pretest error. Rerun routine 1512.
			X'E000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - the OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330, BF492	

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
158C	0X0A	Ensure that an OUT X'43' with data of all zeroes has set the tested address to receive mode.	One scanner pass after the OUT X'43', an IN X'43' indicated that the line was still set to transmit mode. (Byte 0, bit 4 was on.) Reg. X'14' contains the results of the IN X'43'. Reg. X'11' contains the tested line address.	Y4G2	0800	RS308	A-200	Pretest error. Rerun routine 151C.
158C	0X0C	Ensure that when a line is in receive and diagnostic modes, receive data reflects the status of the test data latch.	After having set the test data latch to a space and turning the line adapter around to receive mode, an IN X'43' indicated receive data was set to a mark, not a space. Reg. X'14' contains the actual data received by the IN X'43'. Reg. X'11' contains the tested line address.	Y4E2	0100	RS105	A-340 A-350	Pretest error. Rerun routine 158A.
158C	0X0E	Ensure that after issuing another OUT X'42' with the diagnostic mode bit set (byte 1, bit 1), the diagnostic mode bit remains set.	Now that the test data latch has been set, and the tested address set to receive mode, an OUT X'42' was issued with the diagnostic mode bit set in an attempt to reset the test data latch. An IN X'42' then indicated that diagnostic mode had dropped. (Byte 1, bit 1 was off.)	Y4G2	0040	RS306	A-160	Test error. Rerun routine 153A. Reg. X'14' contains the received IN X'43' data. If needed, reg. X'11' contains the tested line address.
158C	0X10	Ensure that once the scanner is stopped, it can be started again via OUT X'41' and then stopped again by forcing a bit service (OUT X'47') interrupt.	Either the scanner could not started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000		A-240	Test error. Rerun routine 1512.
			X'E000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - The OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330, A-040	
158C	0X12	Before checking to see if the test data latch was set to a mark, ensure that diagnostic mode was indeed set in the tested line adapter.	After allowing a scanner pass to latch up diagnostic mode in IN X'43', the diagnostic mode bit (byte 1, bit 5) in an IN X'43' was not on.	Y4G2	0004	RS307	A-200	Test error. Rerun routines 153E and 1540.
158C	0X14	Ensure that after setting the test data latch to a space, setting diagnostic mode on any line adapter will reset it to a mark.	After having set the test data latch to a space, turning the line arcund to receive mode, and checking that a space was being received, an OUT X'42' was issued with the diagnostic mode bit set. After stopping the scanner again at the	Y4E2	8000	RS105	A-340 A-350	Test error. Problem is most likely near the test data latch itself. If needed, reg. X'14' contains received IN X'43'

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			tested address, an IN X'43' indicated the test data latch was not reset to a mark (receive data, byte 0, bit 0 was still a space.)					data and reg. X'11' contains the tested line address.
15A0	XXXX	Oscillator Speed Test: By stopping the scanner at the tested address, allowing two bit overruns to occur, the average speed of each oscillator is determined and then examined to ensure that the tested oscillator has caused strobes to occur within 0.1% of the oscillator's bit rate. (The speed of all installed oscillators is checked on all installed line adapters in both transmit and receive modes, except autocall adapters. Autocall adapters are checked only with oscillator 0 and in receive mode.)						
15A0	0X02	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15A0	0X04	Ensure that an OUT X'42' has set the selected oscillator select bits (and has either set or reset diagnostic mode).	After issuing an OUT X'42' at the tested line address, an IN X'42' failed to reflect the OUT X'42'. Reg. X'14' contains the actual data received by the IN X'42' and reg. X'15' contains the bits in error:	Y4G2				Pretest error. Rerun appropriate routines as specified below. Reg. X'11' contains failing line address is needed.
			Byte 0:					
			Bit 6-mode bit 1 set in error.			RS304	A-170	Rerun 1550.
			Bit 7-mode bit 2 set in error.			RS304	A-170	Rerun 1554.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun 154C.
			Bit 1-diagnostic mode failed (it should have set on all but autocall adapters).			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun 1530.
			Bit 6-oscillator select bit 1 failed.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed.			RS306	A-160	Rerun routines 1546 and 1548.
15A0	0X06	Ensure that an OUT X'43' has set transmit or receive mode.	After issuing an OUT X'43' to the line under test, an IN X'43' indicated that the transmit mode bit failed to set or reset. Reg. X'14' contains the received IN X'43' data. The transmit mode bit (byte 0, bit 4) should have been the opposite of what it was.	Y4G2	0800	RS308	A-200	Pretest error. Rerun routines 151A and 151C.
15A0	0X08	Ensure that bit overrun can be set in the line adapter under test.	After waiting up to 60 milliseconds (the scanner is still stopped at the tested address) no bit overrun occurred. Reg. X'11' contains the line address under test.	Y4G2	0001	RS308	A-200	Pretest error. Rerun routine 1588.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15A0	0X0C	Ensure that bit overrun can be set in the line adapter under test.	After waiting up to 60 milliseconds (the scanner is still stopped at the tested address) no bit overrun occurred. Reg. X'11' contains the line address under test.	Y4G2	0001	RS308	A-200	Test error. Rerun routine 1588.
15A0	0X0E	Ensure that while measuring the oscillator speed, as each bit overrun occurs, it can be reset.	Following a bit overrun, OUT X'44' with byte 1, bit 7 on was issued to reset the overrun. An IN X'43' then indicated the overrun was not reset. Reg. X'11' contains the line address under test.	Y4E2		RS105	A-300	Test error. Rerun routine 1588.
15A0	0X10	Before checking the oscillator's average speed, ensure that all five overruns occurred.	After waiting a maximum amount of time, less than five bit overruns occurred.	Y4G2		RS308	A-200	Test error. Problem is probably intermittent. Rerun and loop on routine 1588. (If needed, byte 0 of reg. X'14' contains the number of overruns that were not received.)
15A0	0X12	Ensure that no oscillator is running too slow.	The amount of time it took five bit overruns to occur was greater than 0.1% more than what it should have taken. Reg. X'11' contains the tested line address. Byte 1, bits 6 and 7 of reg. X'16' indicate the oscillator under test (00, 01, 10, or 11 are the first, second, third, or fourth oscillators, respectively). If byte 0, bit 4 of reg. X'16' is on, the tested address was in transmit mode. If not, it was in receive mode.	Y4H2-for the first and second oscillators. Y4J2-for the third and fourth oscillators.		RS402 RS403		Test error. Problem may be in the CS, LIB, or line adapter. (See General Comments, #3.)
15A0	0X14	Ensure that no oscillator is running too fast.	The amount of time it took five bit overruns to occur was greater than 0.1% less than what it should have taken. Reg. X'11' contains the tested line address. Byte 1, bits 6 and 7 of reg. X'16' indicate the oscillator under test (00, 01, 10, or 11 are the first, second, third, or fourth oscillators, respectively). If byte 0, bit 4 of reg. X'16' is on, the tested address was in transmit mode. If not, it was in receive mode.	Y4H2-for the first and second oscillators. Y4J2-for the third and fourth oscillators.		RS402 RS403		Test error. Problem may be in the CS, LIB, or line adapter. (See general comments, #3.)
15A2	XXXX	Interrupt Mode 01 (Test #1): Ensure that interrupt mode 01 allows bit service level 2 interrupts from the tested line address when data set ready is active for at least one bit time by forcing data set ready up with diagnostic mode. (This test is run on all installed non-autocall line adapters, in turn. It does not check that mode 01 will prevent level 2 interrupts when data set ready and ring indicator are inactive.)						
15A2	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FRALD PAGE	FETMM PAGE	COMMENTS
			waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
15A2	0X02	Before continuing, ensure that the tested line has been set to diagnostic mode and monitor mode 11.	After stopping the scanner at the tested address and issuing an OUT X'42' to set the proper modes, an IN X'42' indicated a failure to do so. Reg. X'14' contains the data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Reg. X'11' contains line address under test. Rerun the appropriate routine.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 1516,154A, & 154C.
			Bit 1-diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1516,1532, & 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 1516,152A, & 152C.
			Bit 4-external clock set in error.			RS306	A-160	Rerun routines 1516,1536, & 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 1516,152E, & 1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1516,1542, & 1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1516,1546, & 1548.
15A2	0X03	Ensure that the first oscillator can create a strobe and cause a bit service level 2 interrupt from the tested line.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-Q40	Pretest error. Rerun routine 1580.
15A2	0X04	Ensure that the tested line, as a result of having been reset and of having set diagnostic mode, is in receive mode, diagnostic mode, and that data set ready is on.	After having reset the scanner, setting diagnostic mode, and allowing a bit service interrupt, an IN X'43' indicated that the expected conditions were not met. Reg X'14' contains the data received by the IN X'43' and reg. X'15' contains the bits that were in error:	Y4G2, Y4E2	0824		A-200	Pretest error. Rerun appropriate routines as given. If diagnostic mode was in error, ignore data set ready error. If needed, reg. X'11' contains line (BCB) address under test.
			Byte 0:					
			Bit 4-transmit mode bit was on.			RS308		Rerun routine 151C.
			Byte 1:					
			Bit 2-data set ready was not on (the bit in IN X'43' was on).			RS307		Rerun routine 1578.
			Bit 5-diagnostic mode was not on.			RS307		Rerun routine 153E.
15A2	0X05	Ensure that an OUT X'42' has set monitor mode 01, and has kept diagnostic mode set.	While the scanner was stopped for the prior bit service, an OUT X'42' was issued to set the proper modes. An IN X'42' then indicated that the proper bits were not set or other bits were set in error. Reg. X'14' contains the actual data received by the IN X'42' and	Y4G2	03FF		A-150	Pretest error. Rerun appropriate routines as specified below. If needed, reg. X'11' contains the line address under test.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			reg. X'15' indicates the bits in error: Byte 0:					
			Bit 6-mode bit 1 failed to reset.			RS304	A-170	Rerun routine 1550.
			Bit 7-mode bit 2 reset in error.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode reset.			RS306	A-160	Rerun routines 153A dna 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1546 and 1548.
15A2	0X06	Ensure that monitor mode 01 allows an interface service request to cause a level 2 interrupt when data set ready is active.	After having forced data set ready up via diagnostic mode, setting monitor mode 01, and waiting one bit time, no level 2 interrupt occurred from the tested line address.	Y4G2		RS305	A-040	Test error. Problem probably lies within the CS. (See General Comments, #3.) Reg X'11' contains the line address under test.
15A4	XXXX	Interrupt Mode 01 (Test #2): Ensure that interrupt mode 01 allows bit service level 2 interrupts from the tested line address if data set ready or ring indicator are active for at least one bit time. After setting monitor mode 11 and allowing a normal service request, a check is made to see if data set ready or ring indicator happen to be up on the tested address. If either is up, the tested line address is set to mode 01 and a test made to ensure that a bit service interrupt occurs from that line. If not, the test is bypassed on this address. (This test is run on all installed non-autocall line adapters, in turn.)						
15A4	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15A4	0X02	Ensure that an OUT X'42' has set mode 11 and has properly selected an oscillator.	After stopping the scanner and issuing an OUT X'42', an IN X'42' indicated that mode 11 was not set or the proper oscillator select bits were not set (or other bits were set in error). Reg. X'14' contains the actual data received by the IN X'42'. Reg. X'15' contains the bits in error: Byte 0:	Y4G2	03FF		A-150	Pretest error. Rerun routines specified below. Reg. X'11' contains the line address under test.
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode set in error.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready			RS306	A-160	Rerun routines

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			set in error.					1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select bit set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 failed to set or was set in error.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed to set or was set in error.			RS306	A-160	Rerun routines 1546 and 1548.
15A4	0X03	Ensure that the first oscillator can create a strobe and caused a bit service level 2 interrupt from the tested line.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401		Pretest error. Rerun routine 1580.
15A4	0X04	Ensure that monitor mode 01 has been set at the line address under test.	After finding data set ready or ring indicator on at the tested address, an OUT X'42' was issued to set mode 01. An IN X'42' then indicated mode 01 was not set. If byte 0, bit 6 of reg. X'15' is on, mode bit 1 failed to reset. If bit 7 is on, mode bit 2 failed to set.	Y4G2	0300	RS304	A-170	Pretest error. Rerun routines 154E through 1554. If needed, reg. X'11' contains the line address under test.
15A4	0X05	Ensure that ring indicator or data set ready are still active on the tested line address.	Caution: This may not actually indicate a hardware failure. Before waiting for an interrupt, data set ready or ring indicator was active. Now, after waiting for the interrupt, neither is active. Conditions on the line connected to the line adapter under test have changed. This invalidates error code 0X06 which you should get after this failure.	NONE		NONE	NONE	Test error. If it is desired to find out what conditions on the line have changed, display reg. X'15'. Byte 1, bit 1 on indicates ring indicator has dropped. Byte 1, bit 2 on indicates data set ready has dropped. Reg. X'11' contains the line address under test.
15A4	0X06	Ensure that monitor mode 01 allows an interface service request to cause a level 2 interrupt when data set ready or ring indicator are active.	After having found ring indicator or data set ready active, setting monitor mode 01, and waiting a bit time, no level 2 interrupt occurred from the tested line address.	Y4G2		RS305	A-040	Test error. Problem is most probably in the CS. (See General Comments, #3.) If needed, the tested line address may be found in reg. X'11'.
15A5	XXXX	Interrupt Mode 010: Ensure that monitor mode 010 prevents level two interrupts when either data set ready or ring indicator are active. After resetting the scanner, setting the tested line address to diagnostic mode and mode 011, and ensuring that an interrupt does occur (data set ready is active because of diagnostic mode), low priority is reset (thus mode 010 is set) and a test made to ensure that no more interrupts from that line occur. (This test will be run only on the first installed non-autocall adapter found.)						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15A5	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from the line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15A5	0X02	Ensure that an OUT X'42' has set mode 01 and has properly selected low priority and diagnostic mode.	After stopping the scanner at the tested address and issuing an OUT X'42' to set the proper modes, an IN X'42' indicated that bits failed to set or bits set in error Reg X'14' contains the data received by the IN X'42' Reg X'15' contains the bits in error:	Y4G2				Pretest error.
			Byte 0:					
			Bit 6 - mode bit 1 set in error.			RS304	A-170	Rerun routine 1550.
			Bit 7 - mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0 - low priority failed to set.			RS304	A-170	Rerun routine 154A and 154C.
			Bit 1 - diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A and 153C.
			Bit 2 - data terminal ready set in error.			RS306	A-160	Rerun routine 1532 and 1534.
			Bit 3 - synchronous mode set in error.			RS306	A-160	Rerun routine 152A and 152C.
			Bit 4 - external clock set in error.			RS306	A-160	Rerun routine 1536 and 1538.
			Bit 5 - data rate select set in error.			RS306	A-160	Rerun routine 152E and 1530.
			Bit 6 - oscillator select bit 1 set in error.			RS306	A-160	Rerun routine 1542 and 1544.
			Bit 7 - oscillator select bit 2 set in error.			RS306	A-160	Rerun routine 1546 and 1548.
15A5	0X03	Ensure that once the scanner is stopped, it can be started again via OUT X'41' and then stopped again by forcing a bit service (OUT X'47') interrupt.	Either the scanner could not started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000			Pretest error. Rerun routine 1512.
			X'E000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - The OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330, A-040	
15A5	0X04	Ensure that the tested line, as a result of having been reset and of having set	After having reset the scanner, setting diagnostic mode, and allowing a bit	Y4G2	0024	RS307	A-200	Pretest error. Rerun appropriate routines as given.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		diagnostic mode is in diagnostic mode, and that data set ready is on.	service interrupt, an IN X'43' indicated that the expected conditions were not met. Reg. X'14' contains the data received by the IN X'43' and reg. X'15' contains the bits that were in error: Byte 1: Bit 2 - data set ready was not set. Bit 5 - diagnostic mode was not set.					If diagnostic mode was in error, ignore data set ready error. If needed, reg. X'11' contains line address under test. Rerun routine 1578. Rerun routine 153E.
15A5	0X05	Ensure that monitor mode 01 allows an interface service request to cause a level 2 interrupt when data set ready is active.	After having forced data set ready active by setting diagnostic mode, setting monitor mode 01, and waiting a bit time, no level 2 interrupt occurred from the tested line address.	Y4G2		RS305	A-040	Pretest error. Problem is most probably in the CS. Rerun routine 15A2. If needed, the tested line address may be found in reg. X'11'.
15A5	0X06	Ensure that an OUT X'42' has set monitor mode 01, and has kept diagnostic mode set.	While the scanner was stopped for the prior bit service, an OUT X'42' was issued to set the proper modes. An IN X'42' then indicated that the proper bits were set or other bits were set in error. Reg. X'14' contains the actual data received by the IN X'42' and Reg. X'15' indicates the bits in error: Byte 0: Bit 6 - mode bit 1 set in error. Bit 7 - mode bit 2 failed to set. Byte 1: Bit 0 - low priority set in error. Bit 1 - diagnostic wrap mode reset in error. Bit 2 - data terminal ready set in error. Bit 3 - synchronous mode set in error. Bit 4 - external clock bit set in error. Bit 5 - data rate select set in error. Bit 6 - oscillator select bit 1 set in error. Bit 7 - oscillator select bit 2 set in error.	Y4G2	0140	 RS304 RS304 RS304 RS306 RS306 RS306 RS306 RS306 RS306 RS306	 A-170 A-170 A-170 A-160 A-160 A-160 A-160 A-160 A-160 A-160	Pretest error. Rerun appropriate routines as specified below. If needed, reg. X'11' contains the line address under test. Rerun routine 1552. Rerun routine 1550. Rerun routines 154A and 154C. Rerun routines 153A and 153C. Rerun routines 1532 and 1534. Rerun routines 152A and 152C. Rerun routines 1536 and 1538. Rerun routines 152E and 1530. Rerun routines 1542 and 1544. Rerun routines 1546 and 1548.
15A5	0X07	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line address in Reg. X'11' unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Test error. Rerun routine 1512.
15A5	0X08	Ensure that the line tested is still set to diagnostic mode and data set ready is still active.	With the scanner stopped at the tested address, an IN X'43' indicated one of the following conditions existed as described in reg. X'15': Byte 1: Bit 2 - data set ready failed to set.	Y4G2	0024	RS307	A-200	Test error. Rerun appropriate routines as indicated below. Rerun routine 1578.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 5 - diagnostic mode failed to set. Reg. X'14' contains the received IN X'43' data and reg. X'11' contains the tested address.					Rerun routine 1538.
15A5	0X09	Ensure that a bit service level 2 interrupt is prevented if mode 010 has been set and data set ready is active.	After having set mode 010 and data set ready, unmasking level 2 interrupts and waiting at least one bit time, an interrupt did occur and should not have.	Y4G2		RS305	A-040	Test error. Problem probably lies in the CS. If needed, reg. X'11' contains the line address under test.
15A6	XXXX	Interrupt Mode 10 (Test #1): Ensure that interrupt mode 10 prevents normal bit service requests from interrupting and that they are reset while receiving a mark. Also, ensure that as soon as a space is received, a normal bit service request can cause a bit service level 2 interrupt. After ensuring that the tested line address can cause a bit service interrupt while in monitor mode 11 and that diagnostic mode has forced data set ready up, monitor mode 10 is set. The routine then waits a total of two bit times. Since receive data has been a steady mark (via setting diagnostic mode) no interrupt should occur from the line under test and since mode 10 services bits while monitoring, no overrun should be indicated. The tested address is then set to transmit mode just long enough to set the test data latch to a space. The line is then set back to receive mode and a check made to ensure that mode 10 allows an interrupt as soon as a space is received. (This test is run on all installed line adapters, except autocall, in turn.)						
15A6	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15A6	0X02	Before continuing, ensure that the tested line has been set to diagnostic mode and monitor mode 11.	After stopping the scanner at the tested address and issuing an OUT X'42' to set the proper modes, an IN X'42' indicated a failed to do so. Reg. X'14' contains the data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Reg. X'11' contains line address under test. Rerun the appropriate routine.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 1516,154A, & 154C.
			Bit 1-diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1516,1532, & 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 1516,162A, & 152C.
			Bit 4-external clock set in error.			RS306	A-160	Rerun routines 1516,1536, & 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 1516,162E, & 1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1516,1542, & 1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1516,1546, & 1548.
15A6	0X03	Ensure that the first oscillator can create a strobe and caused a bit service level 2 interrupt from the tested line.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under	Y4H2		RS401		Pretest error. Rerun routine 1580.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			test, none occurred.					
15A6	0X04	That after having set the tested line address to diagnostic mode, the expected conditions have been set to continue the test.	After having done nothing but set diagnostic mode and allowed an interrupt from the tested line, an IN X'43' indicated other than the proper conditions. Reg. X'14' contains the received IN X'43' data and reg. X'15' contains the bits in error:		8824			Pretest error. Rerun appropriate routines as indicated below. (If diagnostic mode failed, ignore the receive data and data set ready failures.) If needed, reg. X'11' contains the tested line address.
			Byte 0:					
			Bit 0-receive data was not set to a mark.	Y4E2		RS105		Rerun routine 158C.
			Bit 4-the line was in transmit mode.	Y4G2		RS307	A-200	Rerun routine 151C.
			Byte 1:					
			Bit 2-data set ready was not set.	Y4G2		RS307	A-200	Rerun routine 1578.
			Bit 5-diagnostic mode failed to set.	Y4G2		RS307	A-200	Rerun routine 153E.
15A6	0X05	Ensure that an OUT X'42' has set monitor mode 10, and has kept diagnostic mode set.	While the scanner was stopped for the prior bit service, an OUT X'42' was issued to set the proper modes. An IN X'42' then indicated that the proper bits were not set or other bits were set in error. Reg. X'14' contains the actual data received by the IN X'42' and reg. X'15' indicates the bits in error:	Y4G2	03FF		A-150	Pretest error. Rerun appropriate routines as specified below. If needed, reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 1550.
			Bit 7-mode bit 2 set in error.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode reset.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1546 and 1548.
15A6	0X07	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15A6	0X08	Ensure that any overrun that may have existed before starting the test, have been reset by an OUT X'44'.	After an OUT X'44' with byte 1, bit 7 on, an IN X'43' still indicated a bit overrun. Reg. X'14' contains the results of the IN X'43' and reg. X'11' contains the line address	Y4E2	0001	RS105	A-300	Pretest error. Rerun routine 1588.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			under test.					
15A6	0X09	Ensure that while receiving a mark, a line set to monitor mode 10 does not cause any level 2 interrupts.	After having set the tested line to mode 10, and ensuring that a mark was being received, a level 2 bit service interrupt was received from that line.	Y4G2		RS305	A-040	Test error. Problem probably lies within the CS, however if needed, reg. X'11' contains the line address under test. (See General Comments, #3.)
15A6	0X0A	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15A6	0X0B	Ensure that the hardware services bits while in monitor mode 10 (i.e. as long as a mark is being received, bit service requests are reset.)	After waiting two bit times while in monitor mode 10 and receiving a mark, and no level 2 interrupt occurring, a bit service interrupt was forced. An IN X'43' should then have indicated no bit overrun (hardware should service the bits) but did (or other conditions were in error). Reg. X'14' contains the results of the IN X'43' and reg. X'15' contains the bits in error:	Y4G2	0025	RS305	A-040	Test error. Problem is probably in the CS, however if needed, reg. X'11' contains the line address under test. (See General Comments, #3.) If data set ready or diagnostic mode are in error, ignore the overrun failure and rerun routines 1578 and 153E, respectively.
			Byte 1:					
			Bit 2-data set ready erroneously dropped.					
			Bit 5-diagnostic mode has dropped.					
			Bit 7-a bit overrun has occurred.					
15A6	0X0C	Ensure that after attempting to set the test data latch to a space to continue the the test, the proper conditions have been set.	After setting the tested address to transmit mode, setting send data to a space, resetting transmit mode, and resetting any possible bit overruns, an IN X'43' indicated the proper conditions to continue had not been set. Reg. X'14' contains the results of of the IN X'43' and reg. X'15' contains the bits in error:		0925		A-200	Test error. Although this has been designated as a test error, each function has been previously checked. Rerun the appropriate routines as given below. If needed, reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 4-transmit mode bit was not reset.	Y4G2		RS308	A-180	Rerun routine 151C.
			Bit 7-send data latch (and thus the test data latch) was not reset (space).	Y4G2		RS308	A-180	Rerun routine 1524.
			Byte 1:					
			Bit 2-data set ready dropped (ignore if bit 5 is on).	Y4G2		RS307	A-180	Rerun routine 1578.
			Bit 5-diagnostic mode dropped.	Y4G2		RS307	A-180	Rerun routine 153E.
			Bit 7-any possible bit overrun was not reset.	Y4E2		RS105	A-180	Rerun routine 1588.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15A6	0X0D	Ensure that when a line adapter set to monitor mode 10 receives a space, a level 2 interrupt can occur.	The tested line address failed to interrupt while receiving a space in mode 10.	Y4G2		RS305	A-040	Test error. Problem probably lies in the CS. (See General Comments, #3.) If needed, reg. X'11' contains the line address under test. By continuing from this error stop, more information about the failure may be gathered from the data given at error 0X0F.
15A6	0X0E	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15A6	0X0F	Ensure that when the interrupt caused by receiving a space in mode 10 (see error code 0X0D) occurred, the line tested was indeed receiving a space and that the service request that caused the interrupt was the first since receiving a space (bit overrun was not set).	After receiving the interrupt (or forcing an interrupt if one failed to occur), an IN X'43' indicated conditions which invalidated the test. Reg. X'14' contains the received IN X'43' data and reg X'15' indicates the bits that were in error:		8927		A-280	Test error. If any bits other than byte 1, bit 7 are on, rerun appropriate routine as given below.** If not, problem is probably in the CS. (See General Comments, #3.)
			Byte 0:					
			Bit 0-receive data was not a space.	Y4E2		RS105	A-280	
			Bit 4-transmit mode erroneously set.	Y4G2		RS308	A-200	
			Bit 7-send data (thus the test data latch) was not a space (off).	Y4G2		RS308	A-200	
			Byte 1:					
			Bit 2-data set ready dropped.	Y4G2		RS307	A-200	
			Bit 5-diagnostic mode dropped.	Y4G2		RS307	A-200	
			Bit 6-bit service request not set.	Y4G2		RS307	A-200	
			Bit 7-bit overrun occurred indicating this was not the first interrupt.	Y4G2		RS305	A-040	
15AA	XXXX	Monitor Mode 10 (Test #3): By selecting the first two installed non-autocall line adapters, setting the first to transmit mode and the second to receive, and monitor mode 10, and sending 255 bits, alternating between mark and space, ensure that the receive line will interrupt no more or less than 127 times because of monitor mode 10. (This test runs only on the first two installed non-autocall line adapters found. If two are not found, the test is bypassed.)						
15AA	0X02	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15AA	0X04	Ensure that an OUT X'42'	While the scanner was stopped	Y4G2	03FF		A-150	Pretest error.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		has set monitor mode 10, and has set diagnostic mode.	for the prior bit service, an OUT X'42' was issued to set the proper modes. An IN X'42' then indicated that the proper bits were not set or other bits were set in error. Reg. X'14' contains the actual data received by the IN X'42' and reg. X'15' indicates the bits in error:					Rerun appropriate routines as specified below. If needed, reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 1550.
			Bit 7-mode bit 2 set in error.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode failed to set.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1546 and 1548.
15AA	0X06	Ensure that once the scanner is stopped, it can be started again via OUT X'41' and then stopped again by forcing a bit service (OUT X'47') interrupt.	Either the scanner could not started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000		A-240	Pretest error. Rerun routine 1512.
			X'E000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - The OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - The OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330, A-040	
15AA	0X08	Ensure that at this point of the test, the receive address has been set to the proper condition to continue.	After setting diagnostic mode and resetting any possible bit overruns, an IN X'43' indicated that conditions were not suitable for continuing the test. Reg. X'14' contains the received IN X'43' data and reg. X'15' indicates which bits were in error:		8825		A-180	Pretest error. Rerun appropriate routines as given below. If diagnostic mode failed to set, ignore the receive data and data set ready failures.
			Byte 0:					
			Bit 0-receive data was not a mark (should have been via test data latch and diagnostic mode).	Y4E2		RS105	A-180 A-200	Rerun routine 158C.
			Bit 4-line was in transmit mode.	Y4G2		RS308	A-200	Rerun routine 151C.
			Byte 1:					

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 2-data set ready was not forced up by diagnostic mode.	Y4G2		RS307	A-200	Rerun routine 1578.
			Bit 5-diagnostic mode failed to set.	Y4G2		RS307	A-200	Rerun routine 153E.
			Bit 7-overrun, if present, was not reset.	Y4G2		RS308	A-200	Rerun routine 1588.
15AA	0X0A	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the transmit address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15AA	0X0C	Before continuing, ensure that the transmit line has been set to diagnostic mode and monitor mode 11.	After stopping the scanner at the tested address and issuing an OUT X'42' to set the proper modes, an IN X'42' indicated a failure to do so. Reg. X'14' contains the data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Reg. X'11' contains line address under test. Rerun the appropriate routine.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 1516,154A, & 154C.
			Bit 1-diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1516,1532, & 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 1516,152A, & 152C.
			Bit 4-external clock set in error.			RS306	A-160	Rerun routines 1516,1536, & 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 1516,152E, & 1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1516,1542, & 1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1516,1546, & 1548.
15AA	0X0E	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt from the transmit line.	After setting monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401		Pretest error. Rerun routine 1580.
15AA	0X10	Ensure that at this point of the test, the transmit address has been set to the proper condition to continue.	After setting diagnostic mode, transmit mode, send data to a mark and resetting any possible bit overruns, an IN X'43' indicated that conditions were not suitable for continuing the test. Reg. X'14' contains the received IN X'43' data and reg. X'15' indicates which bits were in error:	Y4G2	0907		A-200	Pretest error. Rerun appropriate routine as shown below.
			Byte 0:					
			Bit 4-transmit mode failed to set.			RS308		Rerun routine 151A.
			Bit 7-send data failed to to set to a mark.			RS308		Rerun routine 1522.
			Byte 1:					
			Bit 5-diagnostic mode failed to set.			RS307		Rerun routine 153E.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 6-bit service request was not up.			RS307		Rerun routine 1580.
			Bit 7-bit overrun was not reset (if present).			RS308		Rerun routine 1588.
15AA	0X12	Ensure that after sending 255 bits (alternately mark and space) to a line (set to receive and diagnostic modes and interrupt mode 10), 127 bit service interrupts are received from that line.	During the process or end of sending the 255 bits an error occurred. The value contained in reg. X'16' is the storage location of the transmit line address. The value in reg. X'16' +2 is the storage location of the receive line address. The hex value in reg. X'15' describes the error:				A-340 A-350	Test error. Problem is probably in the CS near the 'reset bit service' line on ALD page given.
			X'8000' - No interrupt occurred from either the transmit or receive lines after a 30 millisecond wait.					Reg X'14', byte 0 contains the number of bits left to send at the time of failure. Rerun routine 1580.
			X'4000' - An interrupt from an address other than the two being run has occurred.					Reg. X'13' contains the address from which the interrupt occurred. Rerun routine 1511.
			X'2000' - OUT X'43' issued to transmit line failed. Display reg. X'13' for bits in error: Byte 0:					
			Bit 4-Transmit mode dropped.					Rerun routine 151A.
			Bit 7-Send data failed to set to proper state.					Rerun routines 1522 and 1524.
			X'1000' - Receive line interrupted too many times.					Rerun routines 15A6 and 158C.
			X'0800' - Monitor mode 10 did not allow a level 2 interrupt each time a space was received. Reg. X'14', byte 1 contains the received interrupt count in hex. This should have been 127 (X'7F').	Y4G2		RS308		
15AC	XXXX	Interface Check Summary (Test #1): Ensure that interface check summary is set whenever bit overrun is and that once the overrun is reset, so is it. After causing a bit overrun by ignore interface service requests, a check is made to ensure that interface check summary is on. Bit overrun is then reset and a check made to ensure that interface check summary is then off. (This test is run on the first installed non-autocall line adapter found.)						
15AC	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15AC	0X02	Before continuing, ensure that the tested line has been set to diagnostic mode and monitor mode 11.	After stopping the scanner at the tested address and issuing an OUT X'42' to set the proper modes, an IN X'42' indicated a failure to do so. Reg. X'14' contains the data received by the IN X'42'. Reg. X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Reg. X'11' contains line address under test. Rerun the appropriate routine.
			Byte 0: Bit 6-mode bit 1 failed			RS304	A-170	Rerun routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			to set.					154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 1516,154A, & 154C.
			Bit 1-diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A.
			Bit 2-data terminal ready set in error.			RS306	A-160	Rerun routines 1516,1532, & 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 1516,152A, & 152C.
			Bit 4-external clock set in error.			RS306	A-160	Rerun routines 1516,1536, & 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 1516,152E, & 1530.
			Bit 6-oscillator select bit 1 set.			RS306	A-160	Rerun routines 1516,1542, & 1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1516,1546, & 1548.
15AC	0X03	Ensure that the first oscillator can create a strobe and caused a bit service level 2 interrupt from the tested line.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401		Pretest error. Rerun routine 1580.
15AC	0X04	Ensure that diagnostic mode has forced data set ready up. (Data set ready being off will cause interface check summary to be on.)	After setting diagnostic mode, an IN X'43' indicated data set ready was off. (Byte 1, bit 2 of the IN X'43' was on.)	Y4G2	0020	RS307	A-200	Pretest error. Rerun routine 1578. If needed, reg. X'11' contains the tested line address.
15AC	0X05	Ensure that an OUT X'44' has reset any bit overrun condition. (Bit overrun being on will cause interface check summary to be on.)	After issuing an OUT X'44' with byte 1, bit 7 on to reset any possible overruns, an IN X'43' still indicated an overrun condition.	Y4G2	0001	RS308	A-200	Pretest error. Rerun routine 1588. If needed, reg. X'11' contains the tested line address.
15AC	0X06	Ensure that with bit overrun off and data set ready on, no interface check summary is present.	After ensuring that the conditions that can set interface check summary (except feedback error) were not present in an IN X'43', interface check summary was found on.	Y4F2	2000	RS202	A-200	Pretest error. Problem lies within the CS. Display reg. X'14'. If byte 0, bit 1 is on, ignore this error and rerun routine 157A (feedback error was present).
15AC	0X07	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner, and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-040	Test error. Although this failure is designated as a test error, this function has been previously tested. Rerun routine 1580.
15AC	0X08	Ensure that the only condition present to cause interface check summary to be on is bit overrun.	After attempting to cause a bit overrun by not allowing level 2 interrupts for 60 milliseconds and then allowing one, an IN X'43' indicated that the conditions needed were not		4021		A-200	Test error. Rerun appropriate routines as given below.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			present. Reg. X'14 contains the received IN X'43' data and reg. X'15' contains the bits in error: Byte 0: Bit 1-feedback check was present. Byte 1: Bit 2-data set ready dropped. Bit 7-Bit overrun was not set.	 Y4F2 Y4G2 Y4G2		 RS202 RS307 RS308	 A-180 A-180 A-180	 Rerun routine 157A. Rerun routine 1578. Rerun routine 1588.
15AC	0X09	Ensure that after having met the proper conditions for setting interface check summary (see error code 0X08, above) by bit overrun, interface check summary has been set.	With bit overrun on in an IN X'43', interface check summary was not on. (Byte 0, bit 2 of	Y4F2, Y4G2	2000	RS202	A-200	Test error. Problem is in the CS.
15AC	0X0A	Ensure that an OUT X'44' has reset any bit overrun condition. (Bit overrun being on will cause interface check summary to be on.)	After issuing an OUT X'44' with byte 1, bit 7 on to reset any possible overruns, an IN X'43' still indicated an overrun condition.	Y4G2	0001	RS308	A-200	Test error. Rerun routine 1588. If needed, reg. X'11' contains the tested line address.
15AC	0X0B	Ensure that after the bit overrun was reset, interface check summary is no longer on.	The IN X'43' that just indicated no bit overrun, still indicated interface check summary as being on. (Byte 0, bit 2 of the IN X'43'.)	Y4F2, Y4G2	2000	RS202	A-200	Test error. Problem lies within the CS.
15AE	XXXX	Interface Check Summary (Test #2): Ensure that after causing a feedback check error summary in IN X'43' is set and after resetting the feedback check, it is off. (This test is run only on the first installed non-autocall line adapter found.)						
15AE	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15AE	0X02	Ensure that the diagnostic mode bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 1 on.	Either the diagnostic mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 1 on indicates a diagnostic mode bit failure.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 153A.
15AE	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15AE	0X04	Ensure that none of the conditions that can cause interface check summary	After forcing data set ready up via diagnostic mode and disabling the LIB associated		4021		A-200	Pretest error. Rerun appropriate routines as

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		are on.	with the line under test to prevent a bit overrun condition, an IN X'43' indicated a condition that could set interface check summary. Reg. X'14' contains the received IN X'43' data and reg. X'15' contains the bits in error:					given below.
			Byte 0:					
			Bit 1-a feedback error was present.	Y4F2		RS202	A-180	Rerun routine 157A.
			Byte 1:					
			Bit 2-data set ready was off.	Y4G2		RS307	A-180	Rerun routine 1578
			Bit 3-a bit overrun was present.	Y4G2		RS308	A-180	Rerun routine 1588.
15AE	0X05	Ensure that with no condition present that should set interface check summary, interface check summary is indeed off.	The same IN X'43' that did not indicate bit overrun, data set ready off, or feedback error, did indicate interface check summary (byte 0, bit 2 of the IN X'43').	Y4F2, Y4G2	2000	RS202	A-200	Pretest error. Problem lies within the CS.
15AE	0X06	Ensure that after having forced a feedback error, the feedback error bit in IN X'43' has been set (and bit overrun is still off and data set ready is on).	After issuing an OUT X'43' with the send data and transmit mode bits on to the line adapter under test (the LIB is disabled), an IN X'43' indicated no feedback error occurred (or the other conditions were on in error). Reg. X'15' contains the bits in error:		4021		A-200	Test error. Rerun appropriate routine as given below.
			Byte 0:					
			Bit 1-no feedback check occurred.	Y4F2		RS202	A-180	Rerun routine 157C.
			Byte 1:					
			Bit 2-data set ready dropped.	Y4G2		RS307	A-180	Rerun routine 1578.
			Bit 7-bit overrun was on.	Y4G2		RS308	A-180	Rerun routine 1588.
15AE	0X07	Ensure that a feedback error has set interface check summary.	After having caused a feedback error to be indicated in an IN X'43', interface check summary in the same IN X'43' was not on.	Y4F2	2000	RS202	A-200	Test error. Problem is in the CS.
15AE	0X08	Ensure that issuing an OUT X'44' with byte 1, bit 6 on (reset feedback check) has reset the forced feedback check, that bit overrun is still off, and data set ready is still up.	An IN X'43' following the OUT X'44' still indicated a feedback error (or bit overrun was on, or data set ready dropped). Reg X'15' describes the error:		4021		A-200	Test error. Rerun routines as specified below.
			Byte 0:					
			Bit 1-feedback check failed to reset.	Y4F2		RS202	A-180	Rerun routine 157C.
			Byte 1:					
			Bit 2-data set ready dropped.	Y4G2		RS307	A-180	Rerun routine 1578.
			Bit 7-overrun was erroneously set.	Y4G2		RS308	A-180	Rerun routine 1588.
15AE	0X09	Ensure that resetting the feedback check that caused interface check summary to set, resets it.	The same IN X'43' that indicated that feedback check was reset also indicated that interface check summary was still on.	Y4F2	2000	RS202	A-200	Test error. Problem is in the CS.
15B0	XXXX	Interface Check Summary (Test #3): Ensure that data set ready being off sets interface check summary and that turning data set ready on, turns it off. (This test is run only on the first installed non-autocall line adapter found.)						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15B0	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15B0	0X02	Ensure that the diagnostic mode bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 1 on.	Either the diagnostic mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 1 on indicates a diagnostic mode bit failure.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 153A.
15B0	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15B0	0X04	Ensure that none of the conditions that can cause interface check summary are on.	After forcing data set ready up via diagnostic mode and disabling the LIB associated with the line under test to prevent a bit overrun condition, an IN X'43' indicated a condition that could set interface check summary. Reg. X'14' contains the received IN X'43' data and reg. X'15' contains the bits in error:		4021		A-200	Pretest error. Rerun appropriate routines as given below.
			Byte 0:					
			Bit 1-a feedback error was present.	Y4F2		RS202	A-180	Rerun routine 157A.
			Byte 1:					
			Bit 2-data set ready was off.	Y4G2		RS307	A-180	Rerun routine 1578.
			Bit 3-a bit overrun was present.	Y4G2		RS308	A-180	Rerun routine 1588.
15B0	0X05	Ensure that with no condition present that should set interface check summary, interface check summary is indeed off.	The same IN X'43' that did not indicate bit overrun, data set ready off, or feedback error, did indicate interface check summary (byte 0, bit 2 of the IN X'43').	Y4F2, Y4G2	2000	RS202	A-200	Pretest error. Problem lies within the CS.
15B0	0X06	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine. 1512.
15B0	0X07	Ensure that by starting and stopping the scanner and leaving the LIB disabled, data set ready is no longer latched up in the CS and that feedback error and bit overrun are still off.	After stopping the scanner again, an IN X'43' indicated that data set ready, feedback error, or bit overrun were on. Reg X'15' describes the error:		4021		A-200	Test error. Rerun routines specified below.
			Byte 0:					
			Bit 1-feedback error erroneously set.	Y4F2		RS202	A-180	Rerun routine 157A.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Byte 1: Bit 2-data set ready did not reset.	Y4G2		RS307	A-180	Rerun routine 1578.
			Bit 7-bit overrun erroneously set.	Y4G2		RS308	A-180	Rerun routine 1588.
15B0	0X08	Ensure that data set ready being off has caused interface check summary to be on.	After forcing data set ready down by keeping the LIB disabled, the same IN X'43' that indicated data set ready off, failed to indicate interface check summary on.	Y4F2	2000	RS202	A-200	Test error. Problem is within the CS.
15B0	0X09	Ensure that the diagnostic mode bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 1 on, now that the LIB has again been enabled.	Either the diagnostic mode bit failed to act correctly or other bits in the IN X'42' turned on in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 1 on indicates a diagnostic mode bit failure.) Reg. X'14' contains the actual data received by the IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 153A.
15B0	0X0A	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15B0	0X0B	Ensure that setting diagnostic mode has forced data set ready back up in IN X'43'.	After setting diagnostic mode (and disabling the LIB again) an IN X'43' indicated data set ready was off. (Byte 1, bit 2 of the IN X'43' was on.)	Y4G2	0020	RS307	A-200	Test error. Rerun routine 1578.
15B0	0X0C	Ensure that feedback error and bit overrun are still off in the IN X'43' (LIB is disabled).	The same IN X'43' that indicated that data set ready was back on also indicated bit overrun or feedback check as being on. Reg. X'15' says which:		4001		A-200	Test error. Rerun appropriate routine as indicated below.
			Byte 0: Bit 1-feedback error set in error	Y4F2		RS202	A-180	Rerun routine 157A.
			Byte 1: Bit 7-bit overrun was set in error.	Y4G2		RS308	A-180	Rerun routine 1588.
15B0	0X0D	Ensure that interface check summary is off, now that data set ready is back on.	The same IN X'43' that indicated that data set ready was back on, also indicated an interface check summary. (Byte 0, bit 2 of the IN X'43' was on.)	Y4F2	2000	RS202	A-200	Test error. Problem is in the CS.
15B3	XXXX	Character Service (test #0): Ensure that the character service pending latch can be set by an OUT X'46' and then reset by an OUT X'44'.						
15B3	0X01	Ensure that an OUT X'46' can set the character service pending latch.	After attempting to set the character service pending latch with an OUT X'46' an IN X'44' contained other than X'0800'. Reg. X'14' contains the received IN X'44' and Reg.	Y4E2		RS105	A-210, A-220	Test error. Problem is in CS.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			X'15' contains the bits in error.					
15B3	0X02	Ensure that the character service pending latch is reset after an OUT X'44' with the reset character service bit on (Byte 1, bit 4).	After an OUT X'44' with the reset character service pending bit on, an IN X'44' indicated that byte 0; bit 4 (character service pending) was not reset. Reg X'14' contains the received IN X'44' data.	Y4E2	0800	RS105	A-300	Test error. Problem is in CS.
15B4	XXXX	Character Service (Test #1)): Ensure that a character service interrupt can and does occur within 3 idle passes of the scanner after requesting a character service interrupt via OUT X'46'. This is accomplished by resetting the scanner, forcing a bit service interrupt to stop the scanner, and requesting a character service interrupt and starting the scanner via an OUT X'46'. Since no lines are enabled a character service interrupt should occur at the end of the third scanner pass.						
15B4	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15B4	0X02	Ensure that an OUT X'46' causes a level 2 interrupt.	After waiting, no level 2 interrupt occurred.	Y4E2 Y4F2		RS102 RS202 RS201	A-320	Test error. Problem is in the CS. Character service level 2 latch never set.
15B4	0X03	Ensure that the interrupt that occurred caused X'06F0' (the psuedo character control block address) to appear in IN X'41'.	After the level 2 interrupt occurred from requesting character service, an IN X'41' contained other than X'06F0'. Reg X'14' contains the results of the IN X'41' and reg. X'15' contains the bits in error:		0FF0		A-140 A-060	Test error. Problem is in the CS.
			Byte 0:					
			Bit 4 - was on	Y4G2		RS303		
			Bit 5 - was off	Y4F2		RS202		
			Bit 6 - was off	Y4G2		RS303		
			Bit 7 - was on	Y4G2		RS303		
			Byte 1:					
			Bit 0 - was off	Y4G2		RS303		
			Bit 1 - was off	Y4G2		RS303		
			Bit 2 - was off	Y4G2		RS303		
			Bit 3 - was off	Y4G2		RS303		
15B4	0X04	Ensure that the character service interrupt that occurred as a result of an OUT X'46' did so within exactly 3 idle passes of the scanner.	The character service interrupt occurred before or after the third pass. (It actually should occur right at the end of it.) Reg. X'15' indicates whether it was early or late. If the value in reg. X'15' is greater than X'7D' the interrupt was early (before the third pass) and if less than X'78' it was late (after it).	Y4F2		RS202	A-060	Test error. The counter in the character service circuitry is apparently counting wrong.
15B6	XXXX	Character Service (Test #2): Ensure that a bit service interrupt occurring within three scanner passes						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		of a requested character service interrupt can override the character service request.						
16B6	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15B6	0X02	Ensure that no interrupt occurs up to the end of the third idle pass of the scanner after requesting a character service interrupt.	Within 76.8 microseconds of an OUT X'46' (request character service) an interrupt occurred. (All lines were disabled.)	Y4F2		RS202	A-060	Test error. Rerun routine 15B4.
15B6	0X03	Ensure that if a bit service interrupt is requested within three idle passes of the scanner after requesting character service, it will override the requested character service.	A force bit service (OUT X'47') failed to cause a bit service level 2 interrupt. If byte 0, bit 0 of reg. X'15' is on, no interrupt was received at all. If byte 0, bit 5 is on, the character service interrupt requested was not overridden.	Y4F2		RS202	A-060	Test error. Problem is in the CS. If no interrupt was received at all, rerun routine 1512.
15B6	0X04	Ensure that no interrupt occurs up to the end of the third idle pass of the scanner after requesting a character service interrupt.	Within 76.8 microseconds of an OUT X'46' (request character service) an interrupt occurred. (All lines were disabled.)	Y4F2		RS202	A-060	Test error. Rerun routine 15B4.
15B6	0X05	Ensure that if a bit service interrupt is requested within three idle passes of the scanner after requesting character service, it will override the requested character service.	A force bit service (OUT X'47') failed to cause a bit service level 2 interrupt. If byte 0, bit 0 of reg. X'15' is on, no interrupt was received at all. If byte 0, bit 5 is on, the character service interrupt requested was not overridden.	Y4F2		RS202	A-060	The only difference between this error and error 0X03 of this routine, is that this error tests the reset capability of the 'allow character service counter'.
15B6	0X06	Ensure that an OUT X'46' causes a level 2 interrupt.	After waiting, no level 2 interrupt occurred.	Y4F2		RS202 RS201	A-320	Test error. Problem is in the CS. Character service level 2 latch never set.
15B6	0X07	Ensure that the interrupt that occurred caused X'06F0' (the psuedo character control block address) to appear in IN X'41'.	After the level 2 interrupt occurred from requesting character service, an IN X'41' contained other than X'05F0'. Reg. X'14' contains the results of the IN X'41' and reg. X'15' contains the bits in error:		0FF0		A-140	Test error. Problem is in the CS.
			Byte 0:					
			Bit 4 - was on	Y4G2		RS303		
			Bit 5 - was off	Y4F2		RS202		
			Bit 6 - was off	Y4G2		RS303		
			Bit 7 - was on	Y4G2		RS303		
			Byte 1:					
			Bit 0 - was off	Y4G2		RS303		
			Bit 1 - was off	Y4G2		RS303		
			Bit 2 - was off	Y4G2		RS303		
			Bit 3 - was off	Y4G2		RS303		

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15B8	XXXX	Character Service (Test #3): Ensure that a character service interrupt occurs after the scanner has passed four enabled high priority lines. This is accomplished by setting the first four line addresses to a mode other than 00, requesting a character service interrupt, waiting one scanner pass only, and ensuring that a character service interrupt does occur. (This test first sets the four addresses to mode 01, then mode 10, and then mode 11.)						
15B8	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15B8	0X02	Ensure that an OUT X'42' has set the proper mode bits.	After stopping the scanner at the tested address, an OUT X'42' was issued to set the mode bits. An IN X'42' then indicated the correct mode bits were not set. Reg. X'15' indicates which mode bit was in error. (Byte 0, bits 6 and 7 represent mode bits 1 and 2, respectively.)	Y4G2		RS304	A-170	Pretest error. Rerun routines 154E, 1550, and 1552, 1554 for mode bits 1 and 2, respectively. (If needed, reg. X'11' contains the line address under test.)
15B8	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15B8	0X04	Ensure that an OUT X'42' has set the proper mode bits.	After stopping the scanner at the tested address, an OUT X'42' was issued to set the mode bits. An IN X'42' then indicated the correct mode bits were not set. Reg. X'15' indicates which mode bit was in error. (Byte 0, bits 6 and 7 represent mode bits 1 and 2, respectively.)	Y4G2		RS304	A-170	Pretest error. Rerun routines 154E, 1550, and 1552, 1554 for mode bits 1 and 2, respectively. (If needed, reg. X'11' contains the line address under test.)
15B8	0X05	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.
15B8	0X06	Ensure that an OUT X'42' has set the proper mode bits.	After stopping the scanner at the tested address, an OUT X'42' was issued to set the mode bits. An IN X'42' then indicated the correct mode bits were not set. Reg. X'15' indicates which mode bit was in error. (Byte 0, bits 6 and 7 represent mode bits 1 and 2, respectively.)	Y4G2		RS304	A-170	Pretest error. Rerun routines 154E, 1550, and 1552, 1554 for mode bits 1 and 2, respectively. (If needed, reg. X'11' contains the line address under test.)
15B8	0X07	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and	Y4F2, Y4G2		RS305	A-330, A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
15B8	0X08	Ensure that an OUT X'42' has set the proper mode bits.	After stopping the scanner at the tested address, an OUT X'42' was issued to set the mode bits. An IN X'42' then indicated the correct mode bits were not set. Reg. X'15' indicates which mode bit was in error. (Byte 0, bits 6 and 7 represent mode bits 1 and 2, respectively.)	Y4G2		RS304	A-170	Pretest error. Rerun routines 154E, 1550, and 1552, 1554 for mode bits 1 and 2, respectively. (If needed, reg. X'11' contains the line address under test.)
15B8	0X0A	Ensure that an OUT X'46' (set character service request) will cause a character service level 2 interrupt after the scanner has passed four enabled high priority lines.	After having reset the scanner, setting four lines to other than mode 00, and waiting no more than one scanner pass, no character service interrupt occurred.	Y4G2 Y4F2		RS306 RS201	A-060	Test error. Problem is in the CS (probably near the '+ enabled hi pri intf' line).
15BA	XXXX	Character Service (Test #4): After ensuring that OUT X'46' will cause a character service interrupt, ensure that both OUT X'40' and scanner reset can reset the character service request such that no character service interrupt occurs again. (This test is first run using OUT X'46' and then using reset scanner.)						
15BA	0X01	Ensure that an OUT X'46' (request character service) causes a character service interrupt.	After waiting four scanner passes, no character service interrupt occurred.	Y4F2		RS202	A-320 A-060	Pretest error. Rerun routine 15B4.
15BA	0X02	Ensure that OUT X'46' or reset scanner can reset a character service interrupt.	After a character service interrupt occurred, an OUT X'40' or scanner reset (OUT X'45' with byte 0, bit 2 on) was issued. Another interrupt was then received. If reg. X'11' contains X'0000', the reset attempted was an OUT X'40'. If not, it was a reset scanner (after the reset scanner, the scanner is enabled again).	Y4F2		RS202	A-320	Test error. Problem is in the CS.
15BC	XXXX	Character Service (Test #5): Ensure that after a requested character service interrupt, an IN X'43' indicates all zeroes.						
15BC	0X01	Ensure that an OUT X'46' (request character service) causes a character service interrupt.	After waiting four scanner passes, no character service interrupt occurred.	Y4F2		RS202	A-320	Pretest error. Rerun routine 15B4.
15BC	0X02	Ensure that after a character service interrupt, IN X'43' is all zeroes.	After a character service interrupt and an IN X'41', IN X'43' was executed and the resultant data was not all zeroes. Reg. X'15' contains the bits in IN X'43' that were not 0, if needed.	Y4F2 Y4E2	FFFF	RS203 RS103	A-180	Test error. Problem is in the CS and caused by not degating the '+ input 43' signal on ALD page RS103.
15BE	XXXX	Level One Interrupts with LIBs Enabled: After ensuring that no level one interrupts occur when adapter level 1 interrupts are unmasked with the LIBs disabled, ensure that no level one interrupts						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		occur with each LIB enabled in turn.						
15BE	0X01	Ensure that with the LIBs disabled, no level 1 interrupts occur.	After resetting the scanner, level one interrupts were unmasked for 30 milliseconds and while they were unmasked, a type 1 CS level 1 check occurred.	Y4F2		RS206	A-220	Pretest error. Rerun routine 150A. (If needed, display reg. X'14' for the results of an IN X'44' to determine the source of the level one.)
15BE	0X02	If a level 1 interrupt occurred after unmasking, ensure that IN X'76' indicated "type 1 CS level 1 check".	No indication of which adapter caused the interrupt was given in IN X'76'.	Y4D2		RA102	6-082	Test error. Failure was most probably "-type 1 CS bit level 1" on ALD page given, failing to bring up '+ input type 1 CS level 1'.
15BE	0X03	Ensure that an OUT X'44' can reset a level one check.	After having found a level 1 check present, the LIBs were disabled and an OUT X'44' with byte 1, bit 5 on (reset level one checks) was issued. An IN X'44' then indicated a level one check as still being present. Reg. X'14' contains the results of the IN X'44' and reg. X'15' indicates the check bit that failed to reset: Byte 1: Bits 2 thru 5 - bit clock check for LIBs 1, 2, 3, or 4, respectively. Bit 6 - LIB select check.	Y4E2 Y4F2	003E	RS105 RS206	A-300 A-220	Test error. Problem is in the CS. Please note that there is no way to force a level one check of this type in the type 1 CS. Therefore, the cause of this error should be found before finding the cause of the level one check itself.
15BE	0X04	Ensure that no level one checks are present when a LIB is enabled.	After enabling a LIB and unmasking level 1 interrupts, a level 1 check occurred. Reg. X'11' byte 0, bits 6 and 7 indicate which LIB was enabled (0, 1, 2, or 3). Reg. X'15' indicates what check occurred: Byte 1: Bits 2-5 - bit clock check for LIBs one through 4, respectively. Bit 6 - LIB select check. Bit 7 - outbus check.	Y4F2		RS206	A-220	Test error. Problem is probably in the LIB that was enabled. Replace the LIB bit clock control card first. If failure is a LIB select check, first try to determine a failing pattern by continuing from this error stop and seeing which other LIBs fail.
15BF	XXXX	Mode Bit Override: Ensure that mode bit override can override all interrupt modes except mode 010. After resetting the scanner, setting all line addresses to mode 010, and then ensuring that a line set to mode 00 cannot interrupt, mode bit override is set and a test made to ensure that the only line that interrupts is the one set to mode 00. (The line set to mode 00 will be the first installed non-autocall line found.)						
15BF	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from a line set to mode 010.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line address in Reg. X'11'. unmasking level 2 interrupts and waiting the time of a	Y4E2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			scanner pass, no bit service interrupt occurred from that line					
		setting all lines to mode 010, the tested line address can now be set to mode 00 via an OUT X'42'.	with data of all zeroes, an IN X'42' indicated some bits were still set. Reg. X'14' contains the IN X'42' data (any bit on is in error):					Rerun appropriate routines as given. Reg X'11' contains tested line address if needed.
			Byte 0:					
			Bit 6 - mode bit 1			RS304	A-170	Rerun 1550.
			Bit 7 - mode bit 2			RS304	A-170	Rerun 1554.
			Byte 1:					
			Bit 0 - low priority			RS304	A-170	Rerun 154C.
			Bit 1 - diagnostic mode bit			RS306	A-160	Rerun 153C.
			Bit 2 - data terminal ready			RS306	A-160	Rerun 1534.
			Bit 3 - synchronous mode bit			RS306	A-160	Rerun 152C.
			Bit 4 - external clock bit			RS306	A-160	Rerun 1538.
			Bit 5 - data rate select bit			RS306	A-160	Rerun 1530.
			Bit 6 - oscillator select bit 1			RS306	A-160	Rerun 1548.
			Bit 7 - oscillator select bit 2			RS306	A-160	Rerun 1548.
15BF	0X03	Ensure that a bit service level 2 interrupt is prevented if mode 00 has been set and mode bit override is not set.	After having set monitor mode 00 and not setting mode bit override, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt, one occurred.	Y4G2		RS305	A-040	Pretest error. Rerun routine 1584.
15BF	0X04	Ensure that the mode bit override latch can now be set via OUT X'40'.	After having issued an OUT X'40', an IN X'44' indicated that mode bit override (byte 0, bit 0) had not set.	Y4E2	8000	RS104	A-230	Test error. Rerun routine 150E.
15BF	0X05	Ensure that setting mode bit override will allow level 2 interrupts from all lines but lines set to mode 010 (disable).	After having set mode bit override with one line set to mode 00 (normally disable), no level 2 interrupt occurred. (Mode bit override did not override the mode 00 setting.)	Y4G2		RS304	A-230	Test error. Problem is in the CS. Probably override control on ALD page given failed.
15BF	0X06	Ensure that the line address that caused the bit service interrupt was from the line that was set to mode 00.	After the interrupt, the address of the line under test did not compare with the line address that caused the interrupt. Reg X'11' contains the address expected to interrupt and Reg X'14' contains the address that did interrupt.	Y4G2		RS305	A-040	Test error. Apparently, since all other lines were set to mode 010 and yet one of them has caused an interrupt, mode 010 has failed to completely disable two interrupts from that line. Problem is probably in the CS.
15BF	0X07	Ensure that setting mode bit override will allow level 2 interrupts from all lines but lines set to mode 010 (disable).	After having set mode bit override with one line set to mode 00 (normally disable), no level 2 interrupt occurred. (Mode bit override did not override the mode 00 setting.)	Y4G2		RS304	A-230	Test error. Problem is in CS. Probably override control on ALD page given failed.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15BF	0X08	Ensure that the line address that caused the bit service interrupt was from the line that was set to mode 00.	After the interrupt, the address of the line under test did not compare with the line address that caused the interrupt. Reg X'11' contains the address expected to interrupt and Reg X'14' contains the address that did interrupt.	Y4G2		RS305	A-040	Test error. Apparently, since all other lines were set to mode 010 and yet one of them has caused an interrupt, mode 010 has failed to completely disable two interrupts from that line. Problem is probably in the CS.
15C0	XXXX	Data Set Ready and Clear to Send on IBM Integrated Modems (leased lines only). Ensure first that Data Set Ready is always active and then ensure that Clear to Send comes up within 300 milliseconds after setting Request to Send. (This routine is run on line types 5a, 5b, and 8a only.)						
		NOTE: All routines working with IBM integrated modems, autocall or answer units have been designed to attempt to functionally test the modems. In most cases, no suspected card locations are given since the maintenance procedures on C-440 provide a more thorough trouble isolation procedure. When any error occurs that indicates a possible modem, autocall or answer problem please refer to these procedures.						
15C0	0X02	Force a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUTX'47') from the line (BCB) address in Reg.X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-030 A-040	Pretest error. Rerun routine 1512
15C0	0X04	Ensure that data set ready is always active on the modem interface.	An IN X'43' failed to indicate that Data Set Ready was active (Byte 1, bit 2 was on and should not have been on.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.					Test error. If necessary, this failure can be scoped while stopped at this error. Run routine 15D0 to help isolate problem. Also, if LIB type 8, check DSR jumper on ALD page VQXXX.
15C0	0X08	Ensure that Request to send can be set with an OUT X'43'	Following an OUT X'43' with data of X'0002' to set Request to send bit, an IN'43' indicated it failed to set. Reg X'11' contains the line address under test and Reg X'14' contains the received IN X'43' data.	Y4G2	0200	RS308	A-180	Test error. A-200 Rerun routine 1526.
15C0	0X0A	Force a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-030 A-040	Test error. Rerun routine 1512.
15C0	0X0C	Ensure that Clear to Send comes up within 300 milliseconds after setting Request to Send.	Clear to send failed to set in IN X'43'. Reg X'11' contains the line address under test and Reg X'14' contains					Test error. Rerun routine 1578 to prove that clear to

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			the results of the IN X'43'.					send can be set via diagnostic mode. If that runs, run routine 15E0 (manual intervention Routine) to help diagnose the error further. Also, check both DSR and CTS delay jumpering.
15C2	XXXX	External Clock Test: By stopping the scanner at the tested address and allowing five bit overruns to occur, the average speed of each external clock in all integrated modems is determined and then examined to ensure that the tested clock has caused strobes to occur within 0.1% of the external clock's bit rate. This routine will be run on LIB types 5 through 7 only. Each line is run, first in receive and then in transmit mode, with data rate select off (1200 BPS). Then each line is run, as above, but with data rate select on (2400 BPS).						
		NOTE: All routines working with IBM integrated modems, autocall or answer units, have been designed to attempt to functionally test the modems. In most cases, no suspected card locations are given since the maintenance procedures on C-440 provide a more thorough trouble isolation procedure. When any error occurs that indicates a possible modem, autocall or answer problem, please refer to these procedures.						
15C2	0X02	Ensure that force bit service (Out X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-030 A-040	Pretest error. Rerun routine 1512.
15C2	0X04	Ensure that an OUT X'42' has properly set the external clock bit and data rates select bits.	After issuing an OUT X'42 at the tested line address, an IN X'42' failed to reflect the OUT X'42'. Reg. X'14' contains the actual data received by the IN X'42' and reg. X'15' contains the bits in error:	Y4G2	FFFF		A-150	Pretest error. Rerun appropriate routines as specified below. Reg. X'11' contains failing line address if needed.
			Byte 0: Bit 6-mode bit 1 set in error.			RS304	A-170	Rerun 1550.
			Bit 7-mode bit 2 set in error.			RS304	A-170	Rerun 1554.
			Byte 1: Bit 0-low priority set in error.			RS306	A-170	Rerun 154C.
			Bit 1-diagnostic mode bit set in error.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-Data Terminal Ready set in error.			RS306	A-160	Rerun 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun 152C.
			Bit 4-external clock bit failed to set.			RS306	A-160	Rerun 1538.
			Bit 5-data rate select failed to set to the proper state.			RS306	A-160	Rerun 1530.
			Bit 6-oscillator select bit 1 set in error.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 set in error.			RS306	A-160	Rerun routines 1546 and 1548.
15C2	0X06	Ensure that an OUT X'43' has set transmit or receive mode.	After issuing an OUT X'43' to the line under test, an IN X'43' indicated that the transmit mode bit failed to set or reset. Reg. X'14' contains the received IN X'43' data. The transmit mode bit (byte 0, bit 4) should have been the opposite	Y4G2	0800	RS308	A-200	Pretest error. Rerun routines 151A and 151C.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			of what it was.					
15C2	0X08	Ensure that bit overrun can be set in the line interface under test.	After waiting up to 60 milliseconds (the scanner is still stopped at the tested address) no bit overrun occurred. Reg. X'11' contains the line address under test.		0001			Pretest error. Display Reg. X'14'. If byte 0, bit 4 is on line is in TX mode. If not, it is in receive mode. NOTE: If in transmit mode, this error may be caused by loss of external clock. (In receive mode, overruns should occur anyway because of the internal backup clock.)
15C2	0X0C	Ensure that bit overrun can be set in the line interface under test.	After waiting up to 60 milliseconds (the scanner is still stopped at the tested address) no bit overrun occurred. Reg. X'11' contains the line address under test.		0001			Test error. Rerun routine 1588. Problem may be in overrun latch on line interface card. NOTE: If in transmit mode, this error may be caused by loss of external clock. (In receive mode, overruns should occur anyway because of the internal backup clock.)
15C2	0X0E	Ensure that while measuring the external clock speed, as each bit overrun occurs, it can be reset.	Following a bit overrun, OUT X'44' with byte 1, bit 7 on was issued to reset the overrun. An IN X'43' then indicated the overrun was not reset. Reg. X'11' contains the line address under test.	Y4E2		RS105	A-300	Test error. Rerun routine 1588.
15C2	0X10	Before checking the external clock's average speed, ensure that all five overruns occurred.	After waiting a maximum amount of time, less than five bit overruns occurred.					Test error. Problem is Probably intermittent. Rerun and loop on routine 1588. (If needed, byte 0 of reg. x'14' contains the number of overruns that were not received.) NOTE: If in transmit mode, this error may be caused by loss of external clock. (In receive mode, overruns should occur anyway because of the internal backup clock.)
15C2	0X12	Ensure that no external clock is running too slow.	The amount of time it took five bit overruns to occur was greater than 0.1% more than what is should have taken.					Test error. Problem is probably in the modems clock

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Reg. X'11' contains the tested line address. Byte 1, bit 5 on in reg X'16' indicates the 2400 BPS external clock was under test. Bit 5 off indicates the 1200 BPS external clock was under test. If byte 0, bit 4 of reg. X'16' is on, the tested address is on, the tested address was was in transmit mode. If not, it was in receive mode.					card, but may also be in the line interface whe the external clock is gated in. It should be possible to scope this failure while stopped at this error stop. Start scoping at the line interface card. NOTE: Because of the backup clock, in receive mode strobes will still be present even if the external clock is not there at all.
15C2	0X14	Ensure that no oscillator is running too fast.	The amount of time it took five bit overruns to occur was greater than 0.1% less than what it shold have taken. Reg X'11' contains the tested line address. Byte 1, bit 5 on in reg X'16' indicates the 2400 BPS external clock was under test. Bit 5 off indicates the 1200 BPS external clock was under test. If byte 0, bit 4 of reg X'16' is on, the tested address was in transmit mode. If not, it was in receive mode.					Test error. Problem is probably in the m modems clock card, but may also be in the line interface where the external clock is gated in. It should be possible to scope this failure while stopped at this error stop. Start scoping at the line interface card.
15C4	XXXX	Internal Modem Wrap: Insure that 255 marks can be internally wrapped through the IBM integrated modems in LIB types 5 through 7. This routine is run on all modems installed in LIB types 5 through 7. It is equivalent to test 2 of the 3872. Each line is run with the data rate selector bit off and then each line is run with it on. NOTE: All routines working with integrated modems, autocall or answer units have been designed to attempt to functionally test the modems. In most cases, no suspected card locations are given since the maintenance procedures on C-440 provide a more thorough trouble isolation procedure. When any error occurs that indicates a possible modem, autocall or answer problem, please refer to these procedures.						
15C4	0X02	Ensure that force bit service (out X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', ummasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4P2, Y4G2		RS305	A-030 A-040	Pretest error. Rerun routine 1512.
15C4	0X04	Ensure that the external clock and diagnostic mode bits in IN X'42' can be set by issuing OUT X'42' with byte 1, bits 1 and 4 on.	Either the external clock bit failed to set or the diagnostic mode bit failed to set or other bits in the IN X'42' turned on in error. Reg X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 2, bit 4	Y4G2		RS306	A-150 A-160	Pretest error. Rerun routines 1536 and 1538

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			on indicates an external bit failure.) Reg. X'14' contains the actual data received by the IN '42'.					
15C4	0X06	Ensure that the external clock can create a strobe and cause a bit service level 2 interrupt from the tested line.	After having set monitor mode 11 to allow normal bit service requests, selecting the external clock, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.					Pretest error. Rerun routine 15C2. (Remember that in receive mode, the internal backup clock should be causing strobes.)
15C4	0X08	Ensure that request to send has been set by issuing an OUT X'43' with byte 1, bit 6 on.	Either the Request to Send bit failed to set or other bits were set in error in the IN X'43'. Reg. X'11' contains the line (BCB) address under test. Reg X'15' contains the bits IN X'43' in error.	Y4G2	0AB4	RS308	A-180 A-200	Pretest error. Rerun routine 1578. Reg. X'14' contains the actual data received by the IN X'43'. Also, remember that diagnostic mode should force up RLSD, DSR and (if RTS is up) CTS.
15C4	0X10	Ensure that the line under test interrupts at least once every 30 milliseconds.	During the process of sending 255 bits no interrupt occurred from the line under test within 30 milliseconds of the previous interrupt.					Test error. Reg X'16' contains the storage address of a byte in core which contains the residual bit count left. Reg X'13' contains the OUT 42 data. Reg X'11' contains the line under test. Rerun routine 15C2.
15C4	0X12	Ensure as each interrupt occurs, that the tested line is receiving a mark and that no error conditions are present.	During the process of sending 255 bits an IN '43' indicated that conditions were not sutiable for continuing the test. Reg. X'14' contains the received IN X '43' data and reg X'15' indicates which bits were in error:			8215		Test error. Reg X'16', contains the storage address of a byte in core which contains the residual count left. Reg. X'11' contains the line under test.
			Byte 0: Bit 0-receive data was a space.					(See note, below)
			Bit 3-receive data lead set to a space					(See note, below)
			Bit 4-transmit mode erroneously set					Rerun routine. 151A and 15aC rerun routine.
			Bit 6-Request to send latch not set					1526 and 1528
			Byte 1: Bit 0-Clear to Send was not up					Rerun routine. 1578
			Bit 5-diagnostic mode not set					Rerun routine 153E and a540
			Bit 7-bit overrun/underrun set in error.					

NOTE: If receive data was in error but receive data lead was not, problem is probably in line interface. If not, problem probably exists in modem. It should be possible to scope a problem in the modem while stopped at this error stop. The modem should still be wrapping the all marks pattern. Also please see note following the routine description.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15C6	XXXX	Internal Modem Wrap (LIB's 8 and 9): Insure that 254 alternate marks and spaces can be wrapped through the integrated modems of LIB types 8 and 9 utilizing the modems self-wrap capability. The routine finds the highest allowable speed oscillator installed and uses it to run the test. The first installed non-autocall interface is used as the transmit line to set the test data latch in the CS. 254 bits are then wrapped through each installed modem in turn.						
		NOTE: Throughout the error descriptions for this routine, reference will be made to "the transmit line" and "the receive line." Remember that the transmit line is not associated with the modem that is being tested. It is nothing more than a vehicle used to set the test data latch in the CS. The line interface for LIB types 8 and 9 is designed such that if the line interface is in diagnostic and receive modes with data terminal ready on, the test data latch in the CS is gated into the send data trigger in the line interface. Send data is then wrapped through the modem and back into the receive buffer of the same line interface. Thus "the transmit line" refers to the interface being used to set the test data latch and "the receive line" refers to the interface and modem through which the data is actually being wrapped.						
		NOTE: All routines working with integrated modems, autocall or answer units have been designed to attempt to functionally test the modems. In most cases, no suspected card locations are given since the maintenance procedures on C-440 provide a more thorough trouble isolation procedure. When any error occurs that indicates a possible modem, autocall or answer problem, please refer to these procedures.						
15C6	0X02	Force a bit service level 2 interrupt from the receive line.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4P2,Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512
15C6	0X04	Set the receive diagnostic and monitor mode 11 with Data Terminal Ready on and select an oscillator.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg. X'11' contains the line address of the receive line. Reg X'14' contains the received IN X'42' data and reg X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Rerun the appropriate routine as given below.
			Byte 0:					
			Bit 6 - mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7 - mode bit 2 failed to set.					Rerun routine 1552.
			Byte 1:					
			Bit 0 - low priority set in error.			RS304	A-170	Rerun routine 1540.
			Bit 1 - diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A.
			Bit 2 - data terminal ready failed to set.			RS306	A-160	Rerun routine 1532.
			Bit 3 - synchronous mode bit set in error.			RS306	A-160	Rerun routine 152A.
			Bit 4 - external clock bit set in error.			RS306	A-160	Rerun routine 1538.
			Bit 5 - data rate select bit set in error.			RS306	A-160	Rerun routine 1530.
			Bit 6 - oscillator select bit 1 failed.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7 - oscillator select bits 2 failed.			RS306	A-160	Rerun routines 1546 and 1548.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15C6	0X06	Wait 300 milliseconds then start the scanner and force another bit service level 2 interrupt from the receive line.	Either the scanner could not be started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000			Pretest error. Rerun routine 1512.
			X'E000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-240	
			X'C000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4F2		RS202	A-240	
			X'8000' - the OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4F2, Y4G2		RS305	A-330 A-240	
15C6	0X08	Check that Clear to Send has now come up at the receive address. (Even though RTS has not been set, diagnostic mode in LIB types 8 and 9 forces RTS up in the modem. As a result, after the maximum CTS delay, CTS should come up.)	After waiting 300 milliseconds an IN X'43' executed while stopped at the receive address indicated either Clear to Send had not come up or other conditions were in error. Reg X'11' contains the receive line (BCB) address. Reg X'14' contains the results of the IN X'43'. Reg X'15' contains the bits in error:	Y4G2	4FB4		A-180 A-200	Pretest error. If CTS failed, problem is probably in modem. Try running routine 15E0. Also, if necessary, it should be possible to scope this failure while stopped at thi error stop. If other bits are in error, rerun routines as given below:
			Byte 0:					
			Bit 1 - a feedback check was present.			RS202		Rerun routine 157A.
			Bit 4 - transmit mode bit set in error.			RS308		Rerun routine 151C.
			Bit 5 - new sync bit set in error.			RS308		Rerun routine 1520.
			Bit 6 - RTS set in error.			RS308		Rerun routine 1528.
			Bit 7 - Send data mark set in error.			RS308		Rerun routine 1524.
			Byte 1:					
			Bit 0 - CTS failed to come up. (Ignore if byte 1, bit 5 in error also).			RS307		
			Bit 2 - DSR not forced up by diagnostic mode. (Ignore if byte 1, bit 5 in error also.)			RS307		Rerun routine 1578.
			Bit 5 - diagnostic mode bit failed.					
15C6	0X0A	Force a bit service level	After attempting to force a	Y4F2, Y4G2		RS305	A-330	Pretest error.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		2 interrupt from the transmit line.	bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.				A-040	Rerun routine 1512.
15C6	0X0C	Set the transmit line to diagnostic and monitor mode 11 and select an oscillator.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the actual IN X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Reg X'11' contains the selected line address. Rerun the appropriate routine as given:
			Byte 0:					
			Bit 6 - mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7 - mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0 - low priority bit set in error.			RS304	A-170	Rerun routine 1540.
			Bit 1 - diagnostic mode failed to set.			RS306	A-160	Rerun routine 153A.
			Bit 2 - data terminal ready set in error.			RS306	A-160	Rerun routine 1534.
			Bit 3 - synchronous mode bit set in error.			RS306	A-160	Rerun routine 152C.
			Bit 4 - external clock bit set in error.			RS306	A-160	Rerun routine 1538.
			Bit 5 - data rate select bit set in error.			RS306	A-160	Rerun routine 1530.
			Bit 6 - oscillator selected bit 1 failed.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7 - oscillator select bit 2 failed.			RS306	A-160	Rerun routines 1546 and 1548.
15C6	0X0E	Force another bit service level 2 interrupt from the transmit address.	After attempting to force a bit service level 2 interrupt (via an OUT X'47') from the line (BCB) address in reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error, Rerun routine 1512.
15C6	0X10	Set the transmit line to transmit mode and set send data to a mark.	After having set the selected address (found in reg. X'11') to diagnostic mode and issuing an OUT X'43' to set transmit mode and mark, an IN X'43' indicated one or more improper conditions. Reg X'14' contains the actual IN X'43' data and reg X'15' indicates the bits in error:		4904		A-180 A-200	Pretest error. Probably a bad line interface. Rerun routines as indicated below:
			Byte 0:					
			Bit 1 - a feedback check occurred.	Y4E2, Y4F2		RS202		Rerun routine 157A.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 4 - transmit mode bit failed to set.	Y4G2		RS308		Rerun routine 151A.
			Bit 7 - send data bit failed to set.	Y4G2		RS308		Rerun routine 1522.
			Byte 1:					
			Bit 5 - diagnostic mode failed to set.	Y4G2		RS307		Rerun routine 153E.
15C6	0X12	Allow 2 normal bit services from the transmit line to occur.	Although the transmit time has been set to mode 11, 2 level 2 bit service interrupts failed to occur from that line in 60 milliseconds. (Reg X'11' contains the transmit line's address.)	Y4G2		RS305	A-040	Pretest error. Probably an intermittent loss of strobe. Rerun routine 1580.
15C6	0X13	Forced bit SVC from xmit line to turn off all interface leads. Reg 14 contains the xmit line address.	The expected line did not interrupt. Reg 15 contains the bits in error.	A2P2		SB204	7-260 7-040	This is a break Feature test error.
15C6	0X14	Forced bit SVC from receive line to turn off all interface leads. Reg 14 contains the receive line address.	The expected line did not interrupt. Reg 15 contains the bits in error.	A2P2		SB204	7-260 7-040	This is a break feature test error.
15C6	0X15	Forced bit SVC from xmit line to set the send data to space. Reg 14 contains the xmit line address.	The expected line did not interrupt. Reg 15 contains the bits in error.	A2P2		SB204	7-260 7-040	This is a break feature test error.
15C6	0X16	Forced bit SVC from receive line to turn on the break feature. Reg 14 contains the receive line address.	The expected line did not interrupt. Reg 15 contains the bits in error.	A2P2		SB204	7-260 7-040	This is a break Feature test error.
15C6	0X17	Forced bit SVC from xmit line to begin sending Mark for 500ms. Reg 14 contains the xmit line address.	The expected line did not interrupt. Reg 15 contains the bits in error.	A2P2		SB204	7-260 7-040	This is a break feature test error.
15C6	0X18	Forced bit SVC from xmit line to begin sending space for 500ms. Reg 14 contains the xmit line address.	The expected line did not interrupt. Reg 15 contains the bits in error.	A2P2		SB204	7-260 7-040	This is a break feature test error.
15C6	0X19	Forced bit SVC from receive line to change mode bits. Reg 14 contains the receive line address.	The expected line did not interrupt. Reg 15 contains the bits in error.	A2P2		SB204	7-260 7-040	This is a break feature test error.

At this point the Routine will start handling transmit and receive interrupts asynchronously. As each transmit interrupt occurs, the send data bit will be inverted. As each receive line interrupt occurs, receive data is checked to ensure that the alternating bits being sent are being received. This continues until 254 bits have been sent and received. Since there is approximately a 1.5 millisecond delay through the modem, the transmit line will always be a few bits ahead of the receive line.

At each of the remaining error stops in this routine, Reg X'16' contains the storage address (X) of additional error information. Check the break test flag when checking the following stops, if the break test flag is on, the break feature may be failing.

X = line address of the transmit line.
X+2 = line address of the receive (wrapped) line
X+4 = receive bit count (this count is decremented from X'FE' after each bit is received)
X+5 = expected receive data (receive data bit is bit 0)
X+6 = transmit bit count (this count is decremented from X'FF' before each bit is sent.)
X+7 = last transmitted data (send data bit is bit 7)
X+10 = Break test flag: 0001 indicates that a line set 12A or 12B is being tested with the alternate bit wrap; 0002 indicates that the break feature is being tested on the line set 12A or 12B.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15C6	0X22	Ensure that a bit service level 2 interrupt occurs from one of the lines under test at least once every 30 milliseconds.	After resetting the previous bit service interrupt, either no interrupt occurred within 30 milliseconds or a line other than the two being used interrupted. If byte 0, bit 0 of reg. X'13' is off, no bit service occurred. If it is on, a line other than the two being tested interrupted (its address is in the remainder of reg. X'13').	Y4G2		RS305	A-040	Test error. Rerun routine 1580. Probably an intermittent loss of strobe. (See the comment above this error description for additional information.)
15C6	0X24	As each transmit line interrupt occurs, check that each bit has been sent.	An IN X'43' executed following a bit service interrupt from the transmit line, indicated that the previous bit had not been properly sent. Reg X'13' contains the received IN X'43' data. Any of the following bits may have caused the error:		2900		A-200	Test error. Probably an intermittent problem in the associated line interface. Rerun routine 158A or as indicated below:
			Byte 0:					
			Bit 2 - interface check summary if on	Y4F2		RS202		Rerun routines 15AC, 15AE, or 15B0.
			Bit 4 - transmit mode bit if it dropped.	Y4G2		RS308		Rerun routine 152A.
			Bit 7 - send data bit if it was not the same as the last transmitted bit.	Y4G2		RS308		Rerun routines 1522 and 1524. Also, if diagnostic mode dropped (Byte 1, bit 5 of the IN X'43' data was off) rerun routine 153E. (See the comment preceding error code 15C6, 0X22 for additional information.)
15C6	0X26	After transmitting all 254 alternate marks and spaces, disable the transmit line.	After the transmit bit count went to 0, an OUT X'42' was issued with all zeroes. An in X'42' indicated a bit or bits still on. Reg X'13' contains the in X'42' data. Any Bit on is in error:	Y4G2	FFFF		A-150	Test error. Probably a bit intermittently failing in the Associated line interface. (See the comment preceding error code 15C6, 0X22 for additional information. Rerun:
			Byte 0:					
			Bit 6 - mode bit 1			RS304	A-170	Routine 1550.
			Bit 7 - mode bit 2			RS304	A-170	Routine 1554.
			Byte 1:					
			Bit 0 - low priority bit			RS304	A-170	Routine 154C.
			Bit 1 - diagnostic mode			RS306	A-160	Routine 153C.
			Bit 2 - data terminal ready bit.			RS306	A-160	Routine 1534.
			Bit 3 - synchronous			RS306	A-160	Routine 152C.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			mode bit.					
			Bit 4 - external clock bit.			RS306	A-160	Routine 1538.
			Bit 5 - data rate select bit (secondary wrap).			RS306	A-160	Routine 1530.
			Bit 6 - oscillator select bit 1.			RS306	A-160	Routine 1544.
			Bit 7 - oscillator select bit 2.			RS306	A-160	Routine 1548.
15C6	0X28	After transmitting all bits ensure that the receive line has received at least the first space bit.	Even after all bits were transmitted, the receive line had not yet received the first space. There should be no more than 1.2 milliseconds delay through the modem and since 254 bits were sent the receive line should have received the first one by the time the last one is transmitted.					Test error. Suspect a problem in the path of carrier through the modem. The entire modem receiver may be bad. Try adjusting modem TX level.
15C6	0X2A	As each receive line interrupt occurs, ensure that modem is wrapping data and operating properly.	After a receive line interrupt, an IN X'43' indicated that either incorrect data was received or an error condition was detected. Reg X'13' contains the received IN X'43' data. Any of the following bits could have caused the error:		A080			Test error. If CTS dropped or receive data did not compare, look for a modem problem (see comments preceeding 15C6, 0X22 for additional information.) If interface check summary was on, rerun routines 1586, 15AE, or 15B0.
			Byte 0:					
			Bit 0 - received data may not have been as expected (See the expected receive data field.)					
			Bit 2 - interface check summary was on.					
			Byte 1:					
			Bit 0 - if on, CTS dropped.					
15C6	0X2B	The routine has completed the normal data wrap and is now testing the break feature. The routine is holding the xmit line at mark level for 500ms.	The receive line was found at space rather than mark. check the modem card for the line set under test.					
15C6	0X2C	The routine has completed the normal data wrap and has transmitted all marks for 500ms with the secondary wrap turned on. The routine is sending space for 500ms and should receive space.	After a 10ms delay at the mark-to-space change, the receive line was found at mark rather than space. The address in register x'16' plus 2 bytes contains the address of the failing line. Check the modem for the failing line.					

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15C7	XXXX	Internal Modem Wrap (LIB 10 and line set X and Y): Insure that 254 alternate marks and spaces can be wrapped through the integrated modems of LIB types 10 and 11 utilizing the modems self-wrap capability. The routine finds the highest allowable speed oscillator installed and uses it to run the test. 254 bits are then wrapped through each installed modem in turn.						

NOTE: Throughout the error descriptions for this routine, reference will be made to "the transmit line" and "the receive line." Remember that the transmit line is the even numbered interface. the Receive Line is the even line associated with the modem that is being tested. The line interface for LIB types 10 and 11 is designed such that if the even line interface is in diagnostic mode with data terminal ready on, send data is then wrapped through the transmit modem and back into the receive modem of the odd line interface.

NOTE: All routines working with integrated modems, autocall or answer units have been designed to attempt to functionally test the modems. In most cases, no suspected card locations are given since the maintenance procedures in the FETMM, Chapter 8 provide a more thorough trouble isolation procedure. When any error occurs that indicates a possible modem, autocall or answer problem, please refer to these procedures.

15C7	0X01	After waiting 300 milliseconds for the modem to settle down because of any previous testing Data terminal Ready is set on, then the line is tested that RLSD is down, Rec. data is at a mark and that Data Set Ready is on.	After setting Data Terminal Ready a input 43 indicated that incorrect bits were set. Reg X'11' contains the line address under test. Reg X'14' contains the in 43 data and Reg X'15' contains the bits in error. Byte 0 Bit 3 - Received Data Byte 1 Bit 2 - not data set ready Bit 3 - received line signal detector.					Test error. Suspect a problem in the modem Rec Path
15C7	0X02	Force a bit service level 2 interrupt from the transmit line.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512
15C7	0X04	Set the transmit diagnostic and monitor mode 11 with Data Terminal Ready on and select an oscillator.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg. X'11' contains the line address of the receive line. Reg X'14' contains the transmit IN X'42' data and reg X'15' contains the bits in error: Byte 0: Bit 6 - mode bit 1 failed to set. Bit 7 - mode bit 2 failed to set. Byte 1: Bit 0 - low priority set in error. Bit 1 - diagnostic mode	Y4G2	03FF	 RS304 RS304 RS306	 A-170 A-170 A-160	Pretest error. Rerun the appropriate routine as given below. Rerun routine 154E. Rerun routine 1552. Rerun routine 1540. Rerun routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			failed to set.					153A.
			Bit 2 - data terminal ready failed to set.			RS306	A-160	Rerun routine 1532.
			Bit 3 - synchronous mode bit set in error.			RS306	A-160	Rerun routine 152A.
			Bit 4 - external clock bit set in error.			RS306	A-160	Rerun routine 1538.
			Bit 5 - data rate select bit set in error.			RS306	A-160	Rerun routine 1530.
			Bit 6 - oscillator select bit 1 failed.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7 - oscillator select bits 2 failed.			RS306	A-160	Rerun routines 1546 and 1548.
15C7	0X06	Wait 300 milliseconds then start the scanner and force another bit service level 2 interrupt from the transmit line.	Either the scanner could not be started again or after attempting to force the next bit service interrupt and waiting the time of a scanner pass, no bit service interrupt from the line under test occurred. Reg. X'11' contains the line (BCB) address from which bit service was to be forced. Value of Reg. X'15' describes the failure:		E000			Pretest error. Rerun routine 1512.
			X'E000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' (however, no feedback check was present).	Y4G2		RS305	A-040	
			X'C000' - the OUT X'41' failed to reset the type 1 CS level 2 bit in IN X'77' because a feedback check was present.	Y4G2		RS308	A-040	
			X'8000' - the OUT X'41' was successful but the OUT X'47' (force bit service) failed to cause a bit service interrupt.	Y4G2		RS305	A-330 A-040	
15C7	0X08	Check that Clear to Send has now come up at the transmit address. (Even though RTS has not been set, diagnostic mode in LIB types 10 forces RTS up in the modem. LIB type 11 RTS is set in the normal manner. As a result, after the maximum CTS delay, CTS should come up.)	After waiting 300 milliseconds an IN X'43' executed while stopped at the transmit address indicated either Clear to Send had not come up or other conditions were in error. Reg X'11' contains the transmit line (BCB) address. Reg X'14' contains the results of the IN X'43'. Reg X'15' contains the bits in error:	Y4G2	4FB4		A-180 A-200	Pretest error. If CTS failed, problem is probably in modem. Try running routine 15E0. Also, if necessary, it should be possible to scope this failure while stopped at this error stop. If other bits are in error, rerun routines as given below:
			Byte 0:					
			Bit 1 - a feedback check was present.			RS308		Rerun routine 157A.
			Bit 4 - transmit mode bit set in error.			RS308		Rerun routine 151C.
			Bit 5 - new sync bit set in error.			RS308		Rerun routine 1520.
			Bit 6 - RTS set in error.			RS308		Rerun routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								1528.
			Bit 7 - Send data mark set in error.			RS308		Rerun routine 1524.
			Byte 1:					
			Bit 0 - CTS failed to come up. (Ignore if byte 1, bit 5 in error also).			RS307		
			Bit 2 - DSR not forced up by diagnostic mode. (Ignore if byte 1, bit 5 in error also.)			RS307		Rerun routine 1578.
			Bit 5 - diagnostic mode bit failed.					
15C7	0X0A	Force a bit service level 2 interrupt from the receive line.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15C7	0X0C	Set the receive line to diagnostic and monitor mode 11 and select an oscillator.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the actual IN X'15' contains the bits in error:	Y4G2	03FF		A-150	Pretest error. Reg X'11' contains the selected line address. Rerun the appropriate routine as given:
			Byte 0:					
			Bit 6 - mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7 - mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0 - low priority bit set in error.			RS304	A-170	Rerun routine 1540.
			Bit 2 - data terminal ready set in error.			RS306	A-160	Rerun routine 1534.
			Bit 3 - synchronous mode bit set in error.			RS306	A-160	Rerun routine 152C.
			Bit 4 - external clock bit set in error.			RS306	A-160	Rerun routine 1538.
			Bit 5 - data rate select bit set in error.			RS306	A-160	Rerun routine 1530.
			Bit 6 - oscillator selected bit 1 failed.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7 - oscillator select bit 2 failed.			RS306	A-160	Rerun routines 1546 and 1548.
15C7	0X12	Allow 2 normal bit services from the transmit line to occur.	Although the transmit time has been set to mode 11, 2 level 2 bit service interrupts failed to occur from that line in 60 milliseconds. (Reg X'11' contains the transmit line's address.)	Y4G2		RS305	A-040	Pretest error. Probably an intermittent loss of strobe. Rerun routine 1580.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15C7	XXXX	NOTE: At this point the routine will start handling transmit and receive interrupts asynchronously. As each transmit interrupt occurs, the send data bit will be inverted. As each receive line interrupt occurs, receive data is checked to ensure that the alternating bits being sent are being received. This continues until 254 bits have been sent and received. Since there is approximately a 1.5 millisecond delay through the modem, the transmit line will always be a few bits ahead of the receive line.						
15C7	XXXX	NOTE: At each of the remaining error stops in this routine, reg X'16' contains the storage address (X) of additional error information: X = line address of the transmit line. X+2 = line address of the receive (wrapped) line X+4 = receive bit count (this count is decremented from X'FE' after each bit is received) X+5 = expected receive data (receive data bit is bit 0) X+6 = transmit bit count (this count is decremented from X'FF' before each bit is sent.) X+7 = last transmitted data (send data bit is bit 7)						
15C7	0X22	Ensure that a bit service level 2 interrupt occurs from one of the lines under test at least once every 30 milliseconds.	After resetting the previous bit service interrupt, either no interrupt occurred within 30 milliseconds or a line other than the two being used interrupted. If byte 0, bit 0 of reg. X'13' is off, no bit service occurred. If it is on, a line other than the two being tested interrupted (its address is in the remainder of reg. X'13').	Y4G2		RS305	A-040	Test error. Rerun routine 1580. Probably an intermittent loss of strobe. (See the comment above this error description for additional information.)
15C7	0X24	As each transmit line interrupt occurs, check that each bit has been sent.	An IN X'43' executed following a bit service interrupt from the transmit line, indicated that the previous bit had not been properly sent. Reg X'13' contains the received IN X'43' data. Any of the following bits may have caused the error: Byte 0:		2900		A-200	Test error. Probably an intermittent problem in the associated line interface. Rerun routine 158A or as indicated below:
			Bit 2 - interface check summary if on	Y4G2		RS308		Rerun routines 15AC, 15AE, or 15B0.
			Bit 4 - transmit mode bit if it dropped.	Y4G2		RS308		Rerun routine 152A.
			Bit 7 - send data bit if it was not the same as the last transmitted bit.	Y4G2		RS308		Rerun routines 1522 and 1524. Also, if diagnostic mode dropped (Byte 1, bit 5 of the IN X'43' data was off) rerun routine 153E. (See the comment preceding error code 15C7, 0X22 for additional information.)
15C7	0X26	After transmitting all 254 alternate marks and spaces, disable the transmit line.	After the transmit bit count went to 0, an OUT X'42' was issued with all zeroes. An IN X'42' then indicated a bit or bits still on. Reg X'13' contains the IN X'42' data. Any bit on is in error:	Y4G2	FFFF		A-150	Test error. Probably a bit intermittently failing in the associated line interface. (See the comment preceding

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								error code 15C7, 0X22 for additional information. Rerun:
			Byte 0:					
			Bit 6 - mode bit 1			RS304	A-170	Routine 1550.
			Bit 7 - mode bit 2			RS304	A-170	Routine 1554.
			Byte 1:					
			Bit 0 - low priority bit			RS304	A-170	Routine 154C.
			Bit 1 - diagnostic mode			RS306	A-160	Routine 153C.
			Bit 2 - data terminal ready bit.			RS306	A-160	Routine 1534.
			Bit 3 - synchronous mode bit.			RS306	A-160	Routine 152C.
			Bit 4 - external clock bit.			RS306	A-160	Routine 1538.
			Bit 5 - data rate select bit.			RS306	A-160	Routine 1530.
			Bit 6 - oscillator select bit 1.			RS306	A-160	Routine 1544.
			Bit 7 - oscillator select bit 2.			RS306	A-160	Routine 1548.
15C7	0X28	After transmitting all bits ensure that the receive line has received at least the first space bit.	Even after all bits were transmitted, the receive line had not yet received the first space. There should be no more than 1.2 milliseconds delay through the modem and since 250 bits were sent the receive line should have received the first one by the time the last one is transmitted.					Test error. Suspect a problem in the path of carrier through the modem. The entire modem receiver may be bad. Try adjusting modem TX level.
15C7	0X2A	As each receive line interrupt occurs, ensure that modem is wrapping data and operating properly.	After a receive line interrupt, an IN X'43' indicated that either incorrect data was received or an error condition was detected. Reg X'13' contains the received IN X'43' data. Any of the following bits could have caused the error:		A080			Test error. If CTS dropped or receive data did not compare, look for a modem problem (see comments preceeding 15C7, 0X22 for additional information.) If interface check summary was on, rerun routines 1586, 15AE, or 15B0.
			Byte 0:					
			Bit 0 - received data may not have been as expected (See the expected receive data field.)					
			Bit 2 - interface check summary was on.					
			Byte 1:					

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 0 - if on, CTS dropped.					

15C8 XXXX Autocall Dial and Transmit (Manual Intervention Routine): This multipurpose routine allows the operator to select 4 basic test functions to ensure the proper operation of integrated autocall units and modems. The description of each test function is as follows: (The 4 digit hexadecimal identifier is the code that is entered at the first manual intervention stop to select the test function desired.)

X'0000' - Autocall Dial only. This function allows the operator to enter the line address of an integrated autocall unit and a telephone number to be dialed. After testing the static conditions on the autocall interface, the number given is dialed. After dialing is complete, the routine goes to its ending manual intervention stop to indicate that the dialed number should be ringing.

X'0001' - Autocall Dial and Disconnect. This function allows the operator to enter the line addresses of an integrated autocall unit and its associated communications line interface, and a telephone number to be dialed. After testing the static conditions on the communications line interface and the autocall interface, the number given is dialed. After dialing and waiting for an answer tone, the routine insures that control of the telephone line can be turned over to the communications line interface and then insures that a successful disconnec t can be executed.

X'0003' - Autocall Dial, Transmit Mark, and Disconnect. This function provides for the same function as X'0001' (above) except that after having turned a control of the telephone line over to the communications line interface, a continuous mark is sent down line until the operator tells the routine to stop via the dynamic communications facility of the DCM. This test function was designed primarily to simulate the test 3 function of the 3872 modem on a switched network.

X'0006' - Transmit Mark Only. This function provides the facility of sending a continuous mark down line from a non-autocall line interface. This function was designed primarily to simulate the test 3 function of the 3872 modem on a leased line network. (This function may also be used to adjust the equalization meter).

X'0007' - Continuously transmit all ones down line in DLC mode (this test will simulate the zero bit insertion of the DLC hardware). The bit pattern being transmitted will be a space and then 5 marks.

NOTE: Functions '0000', '0001', and '0003' also allow for testing of the 'abandon call and retry' circuitry of the autocall unit. To do so, simply enter the telephone number of a nearby telephone that is off hook. This will present a busy signal to the autocall unit and ACR should come up and cause error code 0X18. If it does not come up within one minute, the routine should time out and give error code 0X1A.

Before running this routine, it is suggested that the reader review the function tested column of each of the following error codes to obtain a basic understanding of the routine and its flow. Because of the different options available, not all error conditions described will be tested. The digits immediately underneath each error code describe under which test function that particular error condition can occur. (0, 1, 3, and 6 for X'0000', X'0001', X'0003', and X'0006' respectively.)

NOTE: All routines working with integrated modems, autocall or answer units have been designed to attempt to functionally test the modems. In most cases, no suspected card locations are given since the maintenance procedures on C-440 provide a more thorough trouble isolation procedure. When any error occurs that indicates a possible modem, autocall or answer, problem, please refer to these procedures.

15C8	0X02 1,3,6	Force a bit service interrupt from the selected communications line interface	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2	RS305	A-330 A-040		Pretest error. Rerun routine 1512.
15C8	0X04	Set the selected communications line interface to interrupt mode 11 with Data Terminal Ready and the other selected line	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the actual IN X'15'	Y4G2	03FF	A-150		Pretest error. Reg X'11' contains the selected line address. Rerun the appro-

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		control bits on.	contains the bits in error:					priate routine as given:
			Byte 0:					
			Bit 6-mode bit 1 failed to set			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority bit set in error			RS304	A-170	Rerun routine 1540.
			Bit 1-diagnostic mode set in error			RS306	A-160	Rerun routine 153C.
			Bit 2-data terminal ready failed to set			RS306	A-160	Rerun routine 1532.
			Bit 3-synchronous mode bit failed			RS306	A-160	Rerun routines 152A & 152C.
			Bit 4-external clock bit failed			RS306	A-160	Rerun routines 1536 & 1538
			Bit 5-data rate selected bit failed			RS306	A-160	Rerun routines 152E & 1530
			Bit 6-oscialltor selected bit 1 failed			RS306	A-160	Rerun routines 1542 & 1544
			Bit 7-oscillator select bit 2 failed			RS306	A-160	Rerun routines 1546 & 1548
15C8	0X06 1,3,6	Allow a normal bit service interrupt from the selected communications line interface to occur.	After setting monitor mode 11 to allow normal bit service requests, starting the scanner, and waiting up to 30 milliseconds for a level 2 interrupt from the selected line, none occurred.	Y4G2		RS305	A-040	Pretest error. Rerun routines 1580 and 15C2. Reg X'11' contains the selected line (BCB) address.
15C8	0X08 1,3	Since the selected communications line interface is a switched line, ensure that Data Set Ready is not up until the call in progress is complete.	With the scanner stopped at the selected line address, an IN X'43' indicated that data set ready was already active. If needed reg. X'14' contains the IN X'43' data.		0020	RS307	A-180 A-200	Pretest error. Rerun routine 1578 and then run routine 15D2 to help isolate problem. The problem may lie in the autoanswer or associated autocall circuitry. If scoping is necessary it should be possible to scope this failure while stopped at this error stop. Reg X'11' contains the selected line address
15C8	0X0A 0,1,3	Force a bit service interrupt from the selected autocall interface.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512
15C8	0X0C 0,1,3	Set the selected autocall interface to interrupt mode 11.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg. X'14' contains the actual IN X'42' data and reg X'15' contains the bits in error:	Y4G2	0300		A-170	Pretest error. Reg X'11' contains the selected line (BCB) address. Rerun the appropriate routines as given:
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed			RS304	A-170	Rerun routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			to set.					1552.
			Byte 1:					
			Bit 0-low priority bit set in error			RS304	A-170	Rerun routine 154C.
15C8	0X0E 0,1,3	Allow a normal bit service interrupt from the selected autocall interface to occur.	After setting monitor mode 11 to allow normal bit service requests, starting the scanner, and waiting up to 30 milliseconds for a level 2 interrupt from the selected line, none occurred.	Y4G2		RS305	A-040	Pretest error. Rerun routines 1580 and 15C2. Reg X'11' contains the selected line (BCB) address.
15C8	0X10 1,1,3	Check the static conditions on the autocall interface (PWI should be the only active line.)	With the scanner stopped at the selected line address, an IN X'43' indicated that PWI was not on or other bits were on in error. Reg X'14' contains the results of the IN X'43' and reg. X'15' contains the bits in error:	Y4G2	9FFC		A-190 A-200	Pretest error. Problem probably lies in the autocall circuitry in the line adapter. Reg X'11' contains the selected line address. If scoping is necessary, it should be possible to scope this failure while stopped at this error. Rerun routines given:
			Byte 0:					
			Bit 0-should always be. zero.			RS307		
			Bit 3-DPR was on in error.			RS308		Rerun routine 155C
			Bit 4-NB8 bit was on in error			RS308		Rerun routine 151C
			Bit 5-NB4 bit was on in error			RS308		Rerun routine 1520
			Bit 6-NB2 bit was on in error			RS308		Rerun routine 1528
			Bit 7-NB1 bit was on in error.			RS308		Rerun routine 1524
			Byte 1:					
			Bit 0-ACR was on in error			RS307		
			Bit 1-PND was on in error			RS307		
			Bit 2-DLO was on in error			RS307		
			Bit 3-PWI was not on			RS307		
			Bit 4-CRQ was on in error			RS308		Rerun routine 1558.
			Bit 5=COS was on in error			RS307		
15C8	0X12 0,1,3	After setting CRQ at the autocall interface, allow another bit service interrupt to occur. (TO check status of line after setting CRQ)	With mode 11 set at the selected line address, the scanner was started, and after waiting up to 30 milliseconds for a level 2 interrupt from the selected line, none occurred.	Y4G2		RS305	A-040	Pretest error. Rerun routine 1580. Reg X'11' contains the selected line (BCB) address.
15C8	0X14 0,1,3	Check that CRQ has been set at the selected autocall interface and that DLO is now up also.	With the scanner stopped at the selected line address, an IN X'43' indicated that DLO had not come up or other conditions were in error. Reg X'14' contains the received IN X'43' data and reg X'15' contains the bits in error.	Y4G2	9FFC		A-190 A-200	Pretest error. Problem probably lies in the autocall circuitry in the line interface. Reg X'1 contains the selected line address. If scoping is necessary, it should be possible to scope this failure while stopped at this error stop. Rerun routine given:
			Byte 0:					
			Bit 0-should always be zero.			RS307		
			Bit 3-DPR was on in error			RS308		Rerun routine 155C
			Bit 4-NB8 bit was on in error.				RS308	Rerun routine a5aC
			Bit 5-NB4 bit was on in error			RS308		Rerun routine 1520
			Bit 6-NB2 bit was on in error			RS308		Rerun routine 1528

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 7-NB1 bit was on in error Byte 1:			RS308		Rerun routine 1524
			Bit 0-ACR was on in error			RS307		
			Bit 1-PND was on in error			RS307		
			Bit 2-DLO failed to come up			RS307		
			Bit 3-PWI dropped			RS307		
			Bit 4-CRQ failed to set			RS308		Rerun routine 1556
			Bit 5-COS was on in error			RS307		
15C8	0X15	Wait up to 30 seconds for Data Line Occupied (DLO) to come up on the selected auto-call line interface.	After setting Call Request and waiting 30 seconds, DLO failed to come up. Reg X'14' contains the received IN X'43' data.					Pretest error. Problem probably lies in the auto-call circuitry in the line interface. Reg X'11' contains the selected line address. If scoping is necessar it should be possible to scope this failure while stopped at this error stage.
15C8	XXXX	Note: At this point the selected telephone number is dialed by a subroutine Before each number is dailed, X'E03n' will be displayed, where 'n' is the digit to be dialed.						See the description of subroutine error codes '1X0C' through '1X1A' for a description of the 'dial-a-digit' subroutine and its error codes.
15C8	XXXX	Note: After dialing the selected number, the routine will wait up to one minute (or until ACR comes up) for an answer tone.						See the description of manual intervention stop code X'F01C' for more information.
15C8	0X16 1,3	While waiting for COS to come up, check to ensure that a bit service interrupt occurs from the auto-call interface at least once every 30 milliseconds.	Although the selected auto-call interface was set to mode 11, no level 2 bit service interrupt occurred from that line within 30 milliseconds of the previous one.	Y4G2		RS305	A-040	Test error. Probably caused by an intermittent loss of strobe. Rerun and loop on routine 1580. If needed, reg X'11' contains the selected line (BCB) address.
15C8	0X18 1,3	Also while waiting for COS, monitor ACR to insure that it never comes up on the autocall interface.	After a bit service interrupt from the selected autocall interface (reg X'11' contains its address), an IN X'43' indicated that ACR had come up. Reg X'13' contains the received IN X'43' data. If byte 1, bit 5 is off, ACR probably came up as it should, indicating that the autocall unit never received an answer tone from the called number. If that bit is on, some other improper condition in the autocall circuitry brought ACR up.					Test error. If it appears that an answer done was never received, be sure that the correct telephone number was entered. Also try dialing the number from a manual phone and ensure that the line is not busy or out-of-order.
15C8	0X1A 1,3	Ensure that either COS or ACR comes up within one minute after dialing the selected number.	After waiting one minute, neither came up. If an answer tone was received, COS should have come up. If not, the ACR counter in the autocall unit should have timed out and brought up ACR. Reg X'13' contains the last received IN X'43' data. Reg X'11' contains the selected					

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			line (BCB) address.					
15C8	0X1C 1,3	After receiving COS, indicating that the communications line interface now has control of the line, reset CRQ to free the autocall unit.	After issuing an OUT X'43' with data of all zeros to the selected autocall address to reset CRQ, an IN X'43' indicated CRQ was still active. Reg X'11' contains the line (BCB) address and reg. X'14' contains the received IN X'43' data.	Y4G2	0008		A-190 A-200	Test error. Problem is probably in the autocall line interface Rerun routine 1558.
15C8	0X1E 1,3,6	Start the scanner and allow a normal bit service interrupt from the selected communications line interface.	Since the selected communications line interface is set to mode 11, when the prior bit service interrupt was reset and the scanner started, an interrupt from that line should have occurred within 30 milliseconds and did not.	Y4G2		RS305	A-040	Test error. Rerun routines 1580 and 15C2 to try to find why a strobe was apparently lost. Reg X'11' contains the selected communications line (BCB) address.
15C8	0X20 1,3,6	Check that Data Set Ready is active on the communications line interface	After the scanner stopped at the selected line (BCB) (which is reg X'11'), an IN X'43' indicated that DSR was off. If this is a leased line, DSR should always be up. If this is a switched line, the call has been completed and DSR should now be up. (Reg X'14' contains the received IN X'43' data.)		0020	RS307	A-180 A-200	Test error. Rerun routine 1578 and then run routine 15D0 to help isolate problem may lie in the associated autocall circuitry. It should be possible to scope this error while stopped at this error stop.
15C8	0X22 3,6	Set transmit mode, request-to-send, and send data to a mark on the communications line interface.	With the scanner stopped at the selected communications line interface, an OUT X'43' was issued to set the transmit mode, RTS, and send data bits. On IN X'43' then indicated that one of the bits failed to set or the new sync bit set in error. Reg X'14' contains the IN X'43' data and reg X'15' contains the bits in error: Byte 0: Bit 4-transmit mode bit failed to set Bit 5-new sync bit set in error. Bit 6-RTS failed to set Bit 7-send data bit failed to set.	Y4G2	0F00	RS308	A-180 A-200	Test error. Rerun the appropriate routine as given below. If needed, reg. X'11' contains the selected communications line address. Rerun routine 151A Rerun routine 1520 Rerun routine 1526 Rerun routine 1522
15C8	0X24 3,6	While waiting for clear to send from the modem check to ensure that a bit service interrupt occurs from the selected communications line interface at lease once every 30 milliseconds.	Although the selected communications line interface was set to mode 11, no level 2 bit service interrupt occurred from that line within 30 milliseconds of the previous one.	Y4G2		RS305	A-040	Test error. Probably caused by an intermittent loss of internal or external clock. Rerun and loop on routine 15C2. If needed reg X'11' contains the selected line (BCB) address.
15C8	0X26 3,6	Write up to 30 seconds for Clear to Send to come up on the selected communications line interface.	After setting Request to Send and waiting 30 seconds, clear-to-send failed to come up. Reg X'13' contains the last received IN X'43' data. Reg. X'11' contains the selected	Y4G2		RS307	A-180 A-200	Test error. Rerun routine 1578 and then run routine 15E0 to help isolate problem. Problem

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETHM PAGE	COMMENTS
			line address.					may be in the modem. If scoping is required, it can probably be done while stopped at this error stop.
15C8	XXXX 3,6	Note: At this point the routine will start continuously sending marks until either an error occurs or the operator uses the dynamic communication facility to end the routine. While doing this, X'E000' and X'E0FF' will alternately be displayed every 255 bit times.						For more information on using the dynamic communication facility to end the routine, see the description of the informational displays under 15XX, E000 and 15XX, E0FF.
15C8	0X28 3,6	While transmitting the continuous mark, check to ensure that a bit service interrupt occurs from the communications line interface at least once every 30 milliseconds	Although the selected communi cations line interface was set to mode 11, no level 2 bit service interrupt occurred from that line within 30 milliseconds of the previous one.	Y4G2		RS305	A-040	Test error. Probably caused by an intermittent loss of internal or external clock. Rerun and loop on routine 1580 or external clock. Rerun and loop on routine 1580 or routine 15C2. If needed, reg X'11' contains the selected line (BCB) address. Note: If the 'loop on error' option is on instead of looping back to the very start of the routine, this error will cause a loop back to where the routine starts to continuously transmit a mark.
15C8	0X2A 3,6	While transmitting the continuous mark, each time a bit service interrupt occurs, an IN X'43' is executed to check for any error conditions line interface.	After a bit service interrupt, an IN X'43' indicated some kind of error. Reg X'13' contains the received IN X'43' data that was in error: Byte 0: Bit 1-a feedback error occurred Bit 2-the interface check summary bit was on Bit 4-the transmit mode bit dropped Bit 6-RTS dropped Bit 7-send data dropped from a mark. (Note: Bit 2, interface check summary may have been set by dropping Data Set Ready, getting a feedback check, or getting a bit overrun, none of which should have occurred)	 Y4E2, Y4F2 Y4F2 Y4G2 Y4G2 Y4G2	6B00	 RS202 RS202 RS308 RS308 RS308	A-180 A-200	Test error Problem is probably intermittent. Reg X'11' contains the selected line (BCB) address Rerun routines as given below: Rerun routine 157A Rerun routines 1586, 15AC, 15AE or 15B0 Rerun routine 151A Rerun routine 1526 Rerun routine 1522 If Data Set Ready dropped, scoping can be done while stopped at this error stop. As in error code 0X28 above, if the 'loop on error' option is on, instead of looping back to the very start of the routine,

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								this error will cause a loop back to where the routine starts to continuously transmit a mark.
15C8	0X2E 1,3	To disconnect the switched line from the communications line interface, reset data terminal ready.	After issuing an OUT X'42' with nothing but both mode bits on, an IN X'42' did not reflect the OUT X'42'. Reg X'14' contains the IN X'42' did not reflect the OUT X'42'. Reg X'14' contains the bits in error: Byte 0: Bit 6-mode bit 1 dropped Bit 7-mode bit 2 dropped Byte 1: Bit 2-Data Terminal Ready failed to reset	Y4G2	0320	 RS304 RS304 RS306	A-150 A-170 A-170 A-160	Test error. Rerun the appropriate routine as given. If needed, reg X'11' contains the selected communications line address. Rerun routine 154E Rerun routine 1552 Rerun routine 1534.
15C8	0X30 1,3	Start the scanner and allow a normal bit service interrupt from the selected communications line interface.	Since the selected communications line interface is set to mode 11, when the prior bit service interrupt was reset and the scanner started, an interrupt from that line should have occurred within 30 milliseconds and did not.	Y4G2		RS305	A-040	Test error. Rerun routines 1580 and 15C2 to try to find why a strobe was apparently lost. Reg X'11' contains the selected communications line (BCB) address.
15C8	0X32 1,3	Check that Data Set Ready has now dropped on the communications line interface.	After having dropped data terminal ready to disconnect the line interface, an IN X'43' indicated that Data Set Ready was still active. If needed, reg X'14' contains the received IN X'43' data.		0020			Test error. The associated autocall unit should have dropped data set ready. If needed, reg X'11' contains the selected line address. It should be possible to scope this failure while stopped at this error code.
15C8	0X34 1,3	Wait 2 seconds and then start the scanner and allow a bit service interrupt to occur from the selected autocall interface.	Since the selected autocall interface is set to mode 11, an interrupt from that address should have occurred within 30 milliseconds after the scanner was started and did not.	Y4G2		RS305	A-040	Test error. Rerun routines 1580 and 15C2 to attempt to find why a strobe did not occur. Reg X'11' contains the selected autocall line (BCB) address.
15C8	0X36 1,3	Now check to insure that the selected autocall interface is back to a reset condition. (Particularly that DLO is now off.)	After having waited 2 seconds from the time data terminal ready was dropped on the communications line interface, an IN X'43' executed while stopped at the associated autocall interface, indicated that the autocall interface was not back to normal. Reg X'14' contains the results of the IN X'43' and reg X'15' contains the bits in error: Byte 0: Bit 0-shoudl always be zero	Y4G2	9FFC	 RS307	A-190 A-200	Test error. Problem probably lies in the autocall circuitry in the line interface Reg X'11' contains the selected line address. If necessary, it should be possible to scope this failure while stopped at this error stop. Rerun routines as given below:

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 3-DPR was on in error			RS308		Rerun routine 155C
			Bit 4-NB8 bit was on in error			RS308		Rerun routine 151C
			Bit 5-NB4 bit was on in error			RS308		Rerun routine 1520
			Bit 6-NB2 bit was on in error			RS308		Rerun routine 1528
			Bit 7-NB1 bit was on in error			RS308		Rerun routine 1524
			Byte 1:					
			Bit 0-ACR was on in error			RS307		
			Bit 1-PND was on in error			RS307		
			Bit 2-DLO failed to drop			RS307		
			Bit 3-PWI was not on			RS307		
			Bit 4-CRQ was on in error			RS308		Rerun routine 1558
			Bit 5-COS was on in error			RS307		
15CA	XXXX	Autoanswer and Receive Test (Manual Intervention Routine): This multipurpose routine allows the operator to select 3 basic test options to insure the proper operation of integrated modems and autoanswer features. The description of each test function follows. (The 4 digit hexadecimal identifier is the code that is entered at the first manual intervention stop to select the test function desired.) X'0000' - Autoanswer only. This function allows the operator to enter the line address of an integrated switched line modem with autoanswer. After testing the static conditions on the communications interface and enabling the line to receive a call, the operator is instructed to call that line's phone number and wait for an answer tone. After doing so, the routine will check to ensure the connection has been made, then disconnect and ensure a successful disconnection. (Also, if the switched line interface also has autocall attached, LIB types 7 and 9, the routine will check the status of DLO on the autocall interface before, during, and after the test.) X'0001' - Autoanswer and Receive (no data checking). This function provides the same test capability as in X'0000' above, except that after having ensured the connection, the routine will check for carrier detect and then go into a continuous receive operation. (No data is checked) It will continuously receive until the operator tells it stop through use of the dynamic communications facility of the DCM. X'0003' - Autoanswer and Receive (check data for a mark). This function provides the same capability of X'0001', above, except that it will check the received data to ensure that it is a steady mark. This function was designed primarily to simulate the test 4 function of a 3872 modem. X'0007' - To enable a selected line, check for carrier, and then put the line into receive mode. The receive data will be checked for the DLC pattern of one space and 5 marks. Data errors will be counted and displayed with the error display of EXXX. NOTE 1: In all three of the above functions, the address entered by the operator can be that of a non-switched line, in which case all parts of the test which deal with autoanswer will be bypassed. In the case of function X'0000' this will virtually bypass all testing. (If the address entered is that of a switched line other than types 6a, 7, 8b, or 9a, only functions X'0001' and X'0003' may be selected, all testing is done as if the line were a leased line, and the switched connection must be completed before continuing from stop 'F044'.) NOTE 2: Before running this routine, it is suggested that the reader review the function tested column of each of the following error codes to obtain a basic understanding of the routine and its flow. Because of the different options available, not all error conditions described will be tested. The digits immediately underneath each error code describe under which test function that particular error condition can occur. (0, 1, and 3 for X'0000', X'0001', and X'0003' respectively.) NOTE 3: All routines working with integrated modems, autocall or answer units have been designed to attempt to functionally test the modems. In most cases, no suspected card locations are given since the maintenance procedures on C-440 provide a more thorough trouble isolation procedure. When any error occurs that indicates a possible modem, autocall or answer problem please refer to these procedures.						
15CA	0X02 0,1,3	Force a bit service interrupt from the associated autocall interface, if one is present. (LIB types 7 and 9 only).	After attempting to force a bit service level 2 interrupt (via an OUT X'47') from the line (BCB) address in reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512
15CA	0X04	Check that DLO (Data Line	An IN X'43', executed while		0020			Pretest error.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
	0,1,3	Occupied is off at the associated autocall interface, if one is present. (LIB type 7 and 9 only.)	stopped at the line (BCB) address in reg X'11', indicated that DLO was already on. Since a call has not yet been placed or received, DLO should have been off. Reg X'14' contains the actual IN X'43' data received.					Problem is probably in the associated line interfa or autocall unit. If necessary, it should be possible to scope this failure while stopped at this error stop
15CA	0X06 0,1,3	Force a bit service interrupt from the selected line address.	After attempting to force a bit service level 2 interrupt (via an OUT X'47') from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512
15CA	0X08 0,1,3	Set the selected line address to interrupt mode 11 with DTR and other selected control bits on.	After issuing an OUT X'42' while stopped at the line (BCB) address in reg X'11', an IN X'42' failed to reflect the OUT X'42. Reg X'14' contains the received IN X'42' data. Reg X'15' indicates which bits were in error:	Y4G2	FFFF		A-150	Pretest error. Rerun and loop on appropriate routines as given below:
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	Routine 154E
			Bit 7-mode bit 2			RS304	A-170	Routine 1552
			Byte 1:					
			Bit 0-low priority bit			RS304	A-170	Routine 154C
			Bit 1-diagnostic mode bit			RS306	A-160	Routine 153C
			Bit 2-Data Terminal Ready			RS306	A-160	Routine 1532
			Bit 3-synchronous mode bit			RS306	A-160	Routines 152A & 152C
			Bit 4-external clock bit			RS306	A-160	Routines 1536 & 1538
			Bit 5-data rate select bit			RS306	A-160	Routines 152E & 1530
			Bit 6-oscillator select bit 1			RS306	A-160	Routines 1542 & 1544
			Bit 7-oscillator select bit 2			RS306	A-160	Routines 1546 & 1548
15CA	0X0A 0,1,3	Start the scanner and allow a normal level 2 interrupt to occur from the selected address.	Although the selected line has been set to monitor mode 11, after starting the scanner no bit service level 2 interrupt occurred from that line within 30 milliseconds. (Reg X'11' contains the line's address.)	Y4G2		RS305	A-040	Pretest error. Probably an intermittent loss of strobe. Rerun and loop on routines 1580 and 15C2.
15CA	0X0C	If the line selected is a switched line, check that Data Set Ready is not up.	With the scanner stopped at the selected line address (in reg. X'11'), an IN X'43' indicated that Data Set Ready was up. On a switched line, DSR should not be up until a call has been made and the connection is complete. If needed, reg X'14' contains the results of the IN X'43'.		0020			Pretest error. Rerun routine 1578 and then run routine 15D2 to help try isolate the problem. It should be possible, if necessary, to scope this failure while stopped at this error stop.
15CA	0X0D 0,1, 3	Set the selected line address to monitor mode 011 to wait for Data Set Ready. (Switched lines only.)	After issuing an OUT X'42' to set mode 011, an IN X'42' failed to reflect the OUT X'42'. Reg. X'14' contains the results of the IN X'42' and reg. X'15' contains the bits in error:	Y4G2	FFFF		A-150	Pretest error. Rerun and loop on appropriate routines as given below:
			Byte 0:					
			Bit 6-mode bit 1 set in error.				RS304	A-170 Rerun 1550.
			Bit 7-mode bit 2 failed to set.				RS304	A-170 Rerun 1552.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Byte 1:					
			Bit 0-low priority bit failed to set.			RS304	A-170	Rerun 154A.
			Bit 1-diagnostic mode set in error.			RS306	A-160	Rerun 153C.
			Bit 2-DTR dropped			RS306	A-160	Rerun 1532.
			Bit 3-Synchronous mode bit failed			RS306	A-160	Rerun 152A and 152C.
			Bit 4-external clock bit failed			RS306	A-160	Rerun 1536 and 1538.
			Bit 5-data rate select bit failed			RS306	A-160	Rerun 152E and 1530.
			Bit 6-oscillator select bit 1 failed			RS306	A-160	Rerun 1542 and 1544.
			Bit 7-oscillator select bit 2 failed.			RS306	A-160	Rerun 1546 and 1548.
15CA	XXXX 0,1, 3	Note: At this point, if the line tested is a switched line, the routine will display X'E00A' in Display B to indicate that it is waiting for Data Set Ready. At this time, the operator should place a call to the tested address.						See the description of informational display X'E00A' for further information.
15CA	0X0F 0,1, 3	After having received the call, set the selected line address back to monitor mode 11.	After issuing an OUT X'42' to mode 11, an IN X'42' failed to reflect the OUT X'42'. Reg. X'14' contains the results of the IN X'42' and reg. X'15' contains the bits in error:	Y4G2	FFFF		A-150	Test error. Rerun and loop in the appropriate routines as given below:
			Byte 0:					
			Bit 6-mode bit 1 failed to set				RS304	A-170 Rerun 154E.
			Bit 7-mode bit 2 failed to set				RS304	A-170 Rerun 1552.
			Byte 1:					
			Bit 0-low priority bit set in error.			RS304	A-170	Rerun 154C.
			Bit 1-diagnostic mode set in error.			RS306	A-160	Rerun 153C.
			Bit 2-DTR dropped			RS306	A-160	Rerun 1532.
			Bit 3-Synchronous mode bit failed			RS306	A-160	Rerun 152A and 152C.
			Bit 4-External clock bit failed			RS306	A-160	Rerun 1536 and 1538.
			Bit 5-data rate select bit failed			RS306	A-160	Rerun 152E and 1530.
			Bit 6-oscillator select bit 1 failed			RS306	A-160	Rerun 1542 and and 1544.
			Bit 7-oscillator select bit 2 failed.			RS306	A-160	Rerun 1546 and 1548.
15CA	0X10	Check that Data Set Ready is up on the selected line address. (leased lines only)	With the scanner stopped at the selected address (found in reg X'11'), an IN X'43' indicated that DSR was not up. Since this is a leased line, it should be up all the time. Reg X'14' contains the results of the IN X'43'.		0020			Test error. This failure also can be scoped while stopped at the error stop.
15CA	0X12 0,1,3	Force a bit service interrupt from the associated autocall interface, if one is present. (LIB types 7 and 9 only).	After attempting to force a bit service level 2 interrupt (via an OUT X'47') from the line (BCB) address in reg. X'11', unmasking level two interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512
15CA	0X14	Check that DLO is now on at	An IN X'43', executed while		0020			Test error.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		the associated autocall interface, if one is present. (LIB types 7 and 9 only)	stopped at the line (BCB) address in reg X'11', indicated that DLO has not come on. Since a line connection has been made, DLO should be up. Reg X'14' contains the received IN X'43' data.					Problem is probably in the associated line interface or autocall unit. If necessary, it should be possible to scope this failure while stopped at the error stop.
15C	0X15 0,1,3	Start the scanner and allow a normal level 2 interrupt to occur from the selected address.	Although the selected line has been set to monitor mode 11, after starting the scanner no bit service level 2 interrupt occurred from that line within 30 milliseconds. (Reg. X'11' contains the address of the line.)	Y4G2		RS305	A-040	Test error. Probably an intermittent loss of strobe. Rerun and loop on routine 1580 and 15C2.
15CA	0XXX 1, 3	Note: At this point the routine displays X'E00B' in Display B to indicate that it is waiting for RLSD. It will automatically continue as soon as RLSD is present.						See the description of informational display X'E00B' for further information.
15CA	0XXX 1, 3	Note: At this point the routine will start to continuously receive and will do so until either one of the following errors occur or until stopped by the operator through use of the dynamic communication facility of the DCM.						For more information on how to stop this continuous receive function, see the writeup for the informational displays E000 thr E0FF
15CA	0X18 1,3	While continuously receiving, ensure that a bit service interrupt occurs from the selected address at least once every 30 milliseconds	No bit service level 2 interrupt from the selected line address (in reg X'11') occurred within 30 milliseconds of the previous one.	Y4G2		RS305	A-040	Test error. Probably an intermittent loss of strobe. Rerun routines 1580 and 15C2. Note" If the 'loop on error' option of the DCM has been set, this error will cause a loop back, to continuously receiving rather than back to the initial start of the routine.
15CA	0X1A 1,3	As each bit is received, check that no error conditions are present (and, if function 3 was selected, check that receive data is a mark.)	After a bit service level 2 interrupt from the selected line address (in reg. X'11'), an IN X'43' indicated one or more error conditions. Reg X'13' contains the received IN X'43' data (ignore bits not described):					Test error. Rerun routines given for byte 0, bits 1, 2 or 4 in error.
			Byte 0:					
			Bit 0-bit off indicates receive data was a space (ignore if function 1 was selected)					
			Bit 1-bit on indicates a feedback check occurred.	Y4E2, Y4F2		RS202	A-200 A-180	Rerun routine 157A.
			Bit 2-bit on indicates error summary was on.	Y4F2		RS202	A-200	Rerun routines 1586, 15AC, 15AE or 15B0.
			Bit 4-bit on indicates transmit mode bit set.	Y4G2		RS308	A-200	Rerun routine 151C

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Byte 1: Bit 2-bit on indicates DSR dropped Bit 3-bit off indicates RLSD dropped.					Note: If the 'loop on error' option of the DCM has been set, this error wil cause a loop back to continuously receiving rather than back to the initial start of the routine.
15CA	0X1C 0,1,3	Start the scanner and allow another normal bit service level 2 interrupt to occur from the selected line address. (Switched lines only)	Although the selected line had been interrupting every bit time after starting the scanner this time no level 2 interrupt occurred from that line within 30 milliseconds. (Reg. X'11' contains the address of the line.)	Y4G2		RS305	A-040	Test error. Problem is probably an intermittent loss of of strobe. Rerun and loop on routines 1580 and 15C2
15CA	0X1E 0,1,3	Reset Data Terminal Ready at the selected line address. (Switched lines only)	After issuing an OUT X'42' while stopped at the selected line address (in reg X'11'), an IN X'42' indicated that either data terminal ready failed to reset or one of the mode bits reset in error. Reg X'14' contains the received IN X'42' data and reg X'15' indicates which bit was in error:	Y4G2	0320		A-150	Test error. Rerun and loop on appropriate routine as given.
			Byte 0:					
			Bit 6-mode bit 1 reset			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 reset			RS304	A-170	Rerun routine 1552
			Byte 1:					
			Bit 2-Data Terminal Ready failed to reset.			RS306	A-160	Rerun routine 1534
15CA	0X20 0,1,3	Start the scanner and allow another normal bit service level 2 interrupt to occur from the selected line address. (Switched lines only)	Although the selected is still set to monitor mode 11, after starting the scanner no level 2 interrupt occurred from that line within 30 milliseconds (Reg X'11' contains the lines address.)	Y4G2		RS305	A-040	Test error. Problem is probably an intermittent loss of strobe Rerun and loop on routines 1580 & 15C
15CA	0X22 0,1,3	Ensure that DSR has now dropped at the selected line address. (Switched lines only)	After having dropped data terminal ready at the selected address and allowing another bit service to occur, in IN X'43' indicated that DSR did not drop. (Reg X'11' contains the selected line address and reg X'14' contains the received IN X'43' data.)		0020			Test error. Problem is probably in the associated autoanswer circuitry. It should be possible to scope this failure while stopped at this error stop.
15CA	0X24 0,1,3	Force a bit service interrupt from the associated autocall interface, if one is present. (LIB types 7 and 9 only.)	After attempting to force a bit service level 2 interrupt (via an OUT X'47') from the line (BCB) address in reg X'11' and waiting the time of a scanner pass, no bit service level 2 interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Test error. Rerun routine 1512
15CA	0X26 0,1,3	Check that DLO is not off again at the associated autocall interface, if one is present. (LIB types 7 and 9	After having dropped DTR on communications line interface to disconnect the line, an IN X'43' executed while stopped		0020			Test error. Problem is probably in the associated line interface or

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		only.)	at the associated autocall interface indicated that DLO was still up. It should have dropped. (Reg X'14' contains the received IN X'43' data. Reg X'11' contains the line address of the associated autocall interface.)					autocall unit. If necessary, it should be possible to scope this failure while stopped at this error stop.

15CE XXXX External Data Wrap (Manual Intervention Routine): This routine allows the operator to select virtually any two similar lines and through a wrap block (or any other means available to him) send data from one line to the other. The lines may be wrapped anywhere, even down line, and may be both leased or both switched. If switched lines are used, the wrap block is not necessary as the transmit line can call the receive line. The operator may elect to either utilize an autodial unit, if one is available, or to place a manual call. If leased lines are selected, all dialing is, of course, bypassed.

This routine is arranged somewhat differently than other routines in this IFT; indeed, its error looping and ending facilities are unique. The following is a brief outline of its composition and flow:

1. Request transmit line address.
2. Request receive line address.
3. Request telephone number to be dialed. (Only if switched lines present).
4. Request autocall interface address. (Only if switched lines present and not manual dialing).
5. Request line speed, etc.
6. Request data option (start-stop 10/7, etc.) and number of characters to wrap.
7. Request data characters to be wrapped.
8. Reset hardware.
9. Enable receive line.
10. Enable transmit line.
11. Dial the autocall interface. (Only if switched lines present and requested).
12. Wait for manual dial completion. (Only if switched lines present and necessary).
13. Set mode on transmit line and wait for CTS.
14. Initialize program control fields.
15. Initialize transmit line.
16. Initialize receive line and set mode.
17. Interrupt level 2 first stage interrupt handler.
18. Transmit line start-stop bit service handler.
19. Transmit line bisync bit service handler.
20. Receive line start-stop bit service handler.
21. Receive line bisync bit service handler.
22. Transmit character service handler.
23. Receive character service handler.
24. End routine (or restart).

After all needed information has been obtained from the operator, the hardware is reset, line connection made, and the hardware and program are initialized. (Prior to this point, if leased lines are to be wrapped, the operator must have wrapped the two lines.) (Up to this point any error that occurs will force a loop back to step 8, hardware reset.) Now the routine's second level interrupt handler is allowed to process all level 2 interrupts. As each bit service occurs, the appropriate bit service handler is given control, and it serializes/deserializes each character, checking for line errors, start and stop bits, etc. As each character is sent/received, a request for a character service level 2 interrupt is made. As each character service interrupt occurs the next character to send is buffered or the character just received is compared to the expected data. When the last character has been sent, the routine will start over at the start of the data, continuously wrapping the same data over and over. This continues until the operator makes use of the dynamic communications facility of the DCM. At this time he may elect to either end the routine or restart at certain points. (See the note under manual intervention code 15XX, F06B for details on ending or restarting the routine).

Most errors occurring during the test will be detected by one of the handlers in level 2. When such an error occurs, level 2 interrupts are masked off, and the routine exits level 2 leaving the scanner and line interface hardware as it was at the time of the error.

Any error that occurs while actually transmitting and receiving data will automatically force a loop back to step 14. There is no way of preventing this loop except to abort the routine. This loop was provided so that by setting the "bypass error stop" sense switch a good scoping loop would be available. (Note that this loop does not go back to hardware setup. This way it prevents any switched line connection from being broken and does not have to wait for CTS again.)

Please note that this routine provides more of a functional test than most routines do and was designed to be utilized as a debug and scoping tool rather than a trouble isolation routine. As such, no suspected card locations are given except in some of the early errors in setting up the hardware. In some cases, the comments may call out a routine to rerun to help isolate a failure but due to possible line problems these routines may not help.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15CE	0X02	Force a bit service level 2 interrupt from the receive line.	After attempting to force a bit service level 2 interrupt (via OUT X'47' from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2,Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15CE	0X04	Set data terminal and the other selected line control bits on at the selected receive line address.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the actual input. X'15' contains the bits in errors:	Y4G2	03FF		A-150	Pretest error. Reg X'11' contains the selected line address. Rerun the appropriate routine as given:
			Byte 0:					
			Bit 6-mode bit 1 set in error			RS304	A-170	Rerun routine 1550.
			Bit 7-mode bit 2 set in error			RS304	A-170	Rerun routine 1554.
			Byte 1:					
			Bit 0-low priority bit set in error			RS304	A-170	Rerun routine 1540.
			Bit 1-diagnostic mode set in error			RS306	A-160	Rerun routine 153C.
			Bit 2-data terminal ready failed to set			RS306	A-160	Rerun routine 1532.
			Bit 3-synchronous mode bit failed			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit failed			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate selected bit failed			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator selected bit 1 failed			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed			RS306	A-160	Rerun routines 1546 and 1548.
15CE	0X06	Force a bit service level 2 interrupt from the transmit line.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2,Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15CE	0X08	Set the selected transmit line interface to interrupt mode 11 with data terminal ready and the other selected line control bits on.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the actual IN X'42' data and reg X'15' contains the bits in errors:	Y4G2	03FF		A-150	Pretest error. Reg X'11' contains the selected line address. Rerun the appropriate routine as given:
			Byte 0:					
			Bit 6-mode bit 1 failed to set			RS304		Rerun routine 154E.
			Bit 7-mode bit 2 failed to set			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority bit set in error			RS304	A-170	Rerun routine 1540.
			Bit 1-diagnostic mode set in error			RS306	A-160	Rerun routine 153C.
			Bit 2-data terminal ready failed to set			RS306	A-160	Rerun routine 1532.
			Bit 3-synchronous mode			RS306	A-160	Rerun routines

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			bit failed					152A and 152C.
			Bit 4-external clock bit failed			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate selected bit failed			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator selected bit 1 failed			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed			RS306	A-160	Rerun routines 1546 and 1548
15CE	0X0A	Force a bit service interrupt from the selected autocall interface.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2,Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512
15CE	0X0C	Set the selected autocall interface to interrupt mode 11.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the actual IN X'42' data and reg X'15' contains the bits in error:	Y4G2	0300		A-170	Pretest error. Reg X'11' contains the selected line (BCB) address. Rerun the appropriate routines as given:
			Byte 0:					
			Bit 6-mode bit 1 failed to set			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.			RS304	A-170	Rerun routine 1552.
15CE	0X0E	Allow a normal bit service interrupt from the selected autocall interface to occur.	After setting monitor mode 11 to allow normal bit service requests, starting the scanner, and waiting up to 30 milliseconds for a level 2 interrupt from the selected line, none occurred.	Y4G2		RS305	A-040	Pretest error. Rerun routine 1580. Reg. X'11' contains the selected line (BCB) address.
15CE	0X10	Check the static conditions on the autocall interface (PWI should be the only active line.)	With the scanner stopped at the selected line address, an IN X'43' indicated that PWI was not on or other bits were on in error. Reg X'14' contains the results of the IN X'43' and reg. X'15' contains the bits in error:	Y4G2	9FFC		A-190 A-200	Pretest error. Problem probably lies in the autocall circuitry in the line adapter. Reg X'11' contains the selected line address. If scop is necessary, it should be possible to scope this failure while stopped at this error. Rerun routines given:
			Byte 0:					
			Bit 0-should always be zero					
			Bit 3-DPR was on in error.			RS308		Rerun routine 155C
			Bit 4-NB8 bit was on in error			RS308		Rerun routine 151C
			Bit 5-NB4 bit was on in error			RS308		Rerun routine 1520
			Bit 6-NB2 bit was on in error			RS308		Rerun routine 1528
			Bit 7-NB1 bit was on in error.			RS308		Rerun routine 1524
			Byte 1:					
			Bit 0-ACR was on in error			RS307		

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 1-PND was on in error			RS307		
			Bit 2-DLO was on in error			RS307		
			Bit 3-PWI was not on			RS307		
			Bit 4-CRQ was on in error			RS308		Rerun routine 1558.
			Bit 5-COS was on in error			RS307		
15CE	0X12	After setting CRQ at the autocall interface, allow another bit service interrupt to occur. (To check status of line after setting CRQ)	With mode 11 set at the selected line address, the scanner was started, and after waiting up to 30 milliseconds for a level 2 interrupt from the selected line, none occurred.	Y4G2		RS305	A-040	Pretest error. Rerun routine 1580. Reg X'11' contains the selected line (BCB) address.
15CE	0X14	Check that CRQ has been set at the selected autocall interface and that DLO is now up also. (CRQ should have been set via an OUT X'43' just after checking the static conditions of the autocall interface.)	With the scanner stopped at the selected line address, an IN X'43' indicated that DLO had not come up, CRQ was not set, or other conditions were in error. Reg X'14' contains the received IN X'43' data and reg X'15' contains the bits in error:	Y4G2	9FFC		A-190 A-200	Pretest error. Problem probably lies in the autocall circuitry in the line interface. Reg X'11 contains the selected line address. If scoping is necessary, it should be possible to scope this failure while stopped at this error stop. Rerun routine given:
			Byte 0:					
			Bit 0-should always be zero.			RS307		Rerun routine 155C
			Bit 3-DPR was on in error.			RS308		Rerun routine 151C
			Bit 4-NB8 bit was on in error			RS308		Rerun routine 1520
			Bit 5-NB4 bit was on in error			RS308		Rerun routine 1528
			Bit 6-NB2 bit was on in error			RS308		Rerun routine 1524
			Bit 7-NB1 bit was on in error			RS308		
			Byte 1:					
			Bit 0-ACR was on in error			RS307		
			Bit 1-PND was on in error			RS307		
			Bit 3-PWI dropped			RS307		
			Bit 4-CRQ failed to set			RS308		Rerun routine 1556
			Bit 5-COS was on in error			RS307		
15CE	0X15	Wait up to 30 seconds for Data Line Occupied (DLO) to come up on the selected auto-call line interface.	After setting Call Request and waiting 30 seconds, DLO failed to come up. Reg X'14' contains the received IN X'43' data.					Pretest error. Problem probably lies in the autocall circuitry in the line interface. Reg X'11' contains the selected line address. If scoping is necessar it should be possible to scope this failure while stopped at this error stage.
15CE	XXXX	Note: At this point the selected telephone number is dialed by a subroutine Before each number is dailed, X'E03n' will be displayed, where 'n' is the digit to be dialed.						See the description of subroutine error codes '1X0C' through '1X1A' for a description of the 'dial-a-digit' subroutine and its error codes.
15CE	XXXX	Note: After dialing the selected number, the routine will wait up to one minute (or until ACR comes up) for an answer tone.						
15CE	0X16	While waiting for COS to come up, check to ensure that a bit service interrupt occurs from the auto-	Although the selected autocall interface was set to mode 11, no level 2 bit service interrupt occurred from	Y4G2		RS305	A-040	Pretest error. Probably caused by an intermittent loss of

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		call interface at least once every 30 milliseconds.	that line within 30 milliseconds of the previous one.					strobe. Rerun and loop on routine 1580. If needed, reg X'11' contains the selected line (BCB) address.
15CE	0X18	Also while waiting for COS, monitor ACR to insure that it never comes up on the autocall interface.	After a bit service interrupt from the selected autocall interface (reg X'11' contains its address), an IN X'43' indicated that ACR had come up. Reg X'13' contains the received IN X'43' data. If byte 1, bit 5 is off, ACR probably came up as it should, indicating that the autocall unit never received an answer tone from the called number. If that bit is on, some other improper condition in the autocall circuitry brought ACR up.					Pretest error. If it appears that an answer done was never received, be sure that the correct telephone number was entered. Also try dialing the number from a manual phone and ensure that the line is not busy or out-of-order.
15CE	0X1A	Ensure that either COS or ACR comes up within one minute after dialing the selected number.	After waiting one minute, neither came up. If an answer tone was received, COS should have come up. If not, the ACR counter in the autocall unit should have timed out and brought up ACR. Reg X'13' contains the last received IN X'43' data. Reg X'11' contains the selected line (BCB) address.					
15CE	0X1C	After receiving COS, indicating that the communications line interface now has control of the line, reset CRQ to free the autocall unit.	After issuing an OUT X'43' with data of all zeros to the selected autocall address to reset CRQ, an IN X'43' indicated CRQ was still active. Reg X'11' contains the line (BCB) address and reg. X'14' contains the received IN X'43' data.	Y4G2	0008		A-190 A-200	Pretest error. Problem is probably in the autocall line interface Rerun routine 1558.
15CE	0X1D	Now, disable the autocall interface from interrupting.	While stopped at the autocall interface address (found in reg X'11') an OUT X'42' was issued with all bit off. An IN X'42' then indicated that one of the mode bits failed to reset. Reg X'14' contains the results of the IN X'42'	Y4G2	0300	RS304	A-170	Pretest error. Rerun routines 1550 and 1554.
15CE	0X1E	Start the scanner and allow a normal bit service interrupt from the selected transmit line.	Since the selected transmit line interface is set to mode 11, when the prior bit service interrupt was reset and the scanner started, an interrupt from that line should have occurred within 30 milliseconds and did not.	Y4G2		RS305	A-040	Pretest error. Rerun routine 1580 to try to find why a strobe was apparently lost. Reg X'11' contains the selected communications line (BCB) address.
15CE	0X20	Check that Data Set Ready is active on the transmit line interface.	After the scanner stopped at the selected line (BCB) (which is reg X'11', an IN X'43' indicated that DSR was off. If this is a leased line, DSR should always be up. If this is a switched line, the call has been completed and DSR should now be up. (Reg X'14' contains the		0020	RS307	A-180 A-200	Pretest error. Rerun routine 1578 and then run routine 15D0 to help isolate problem may lie in the associated autocall circuitry. It should be

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			received IN X'43' data.)					possible to scope this error while stopped at this error stop.
15CE	0X22	While waiting for a manual call to be placed, ensure that a bit service interrupt occurs from the selected transmit line at least once every 30 milliseconds.	Although the selected transmit address (found in reg X'11' was set to monitor mode 11, no level 2 interrupt occurred from that line within 30 milliseconds of the previous one.	Y4G2		RS305	A-040	Pretest error. Probably caused by an intermittent loss of strobe. Rerun and loop on routine 1580.
15CE	0X24	Set transmit mode, request-to-send, and send data to a mark on the transmit line interface.	With the scanner stopped at the selected transmit line interface, an OUT X'43' was issued to set the transmit mode, RTS, and send data bits. An IN X'43' then indicated that one of the bits failed to set or the new sync bit set in error. Reg X'14' contains the IN X'43' data and reg X'15' contains the bits in error: Byte 0; Bit 4-transmit mode bit failed to set. Bit 5-new sync bit set in error. Bit 6-RTS failed to set. Bit 7-send data bit failed to set.	Y4G2	0F00	RS308	A-180 A-200	Test error. Rerun the appropriate routine as given below. If needed, reg. X'11' contains the selected communications line address. Rerun routine 151A. Rerun routine 1520. Rerun routine 1526. Rerun routine 1522.
15CE	0X26	While waiting for clear to send, check to ensure that a bit service interrupt occurs from the selected transmit line interface at least once every 30 milliseconds.	Although the selected transmit line interface was set to mode 11, no level 2 bit service interrupt occurred from that line within 30 milliseconds of the previous one.	Y4G2		RS305	A-040	Pretest error. Probably caused by an intermittent loss of strobe. Rerun and loop on routine 1580. If needed reg X'11' contains the selected line (BCB) address.
15CE	0X28	Wait up to 30 seconds for Clear to Send to come up on the selected transmit line interface.	After setting Request to Send and waiting 30 seconds, clear-to-send failed to come up. Reg X'13' contains the last received IN X'43' data. Reg. X'11' contains the selected line address.	Y4G2		RS307	A-180 A-200	Pretest error. Rerun routine 1578 and then run routine 15E0 to help isolate problem. Problem may be in the modem. If scoping is required, it can probably be done while stopped at this error stop.
15CE	0X30	Set the selected transmit line interface to interrupt mode 11 with data terminal ready and the other selected line control bits on.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the actual IN X'42' data and reg X'15' contains the bits in errors: Byte 0:	Y4G2	03FF		A-150	Pretest error. Reg X'11' contains the selected line address. Rerun the appropriate routine as given:

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 6-mode bit 1 failed to set			RS304		Rerun routine 154E.
			Bit 7-mode bit 2 failed to set			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority bit set in error			RS304	A-170	Rerun routine 1540.
			Bit 1-diagnostic mode set in error			RS306	A-160	Rerun routine 153C.
			Bit 2-data terminal ready failed to set			RS306	A-160	Rerun routine 1532.
			Bit 3-synchronous mode bit failed			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit failed			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate selected bit failed			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator selected bit 1 failed			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed			RS306	A-160	Rerun routines 1546 and 1548.
15CE	XXXX	Note: The code associated with error codes 0X31 through 0X34 was inserted to prevent erroneous error indications when continuing from an error stop that occurred while wrapping data. When continuing from such an error stop, the routine will loop back to this point. The transmit line is set to a mark and the routine waits until the receive line sees a mark. This is done to ensure that if the transmit line was at a space at the time of failure, the delay time through any modem will not allow that space to get through as the test restarts and be detected as a start bit and thus cause an error.						
15CE	0X31	Force another bit service interrupt from the selected transmit line address.	After attempting to force a bit service level 2 interrupt (via OUT X'47' from the line (BCB) address in reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15CE	0X32	Ensure that the transmit line is still in transmit mode, with send data at a mark, and RTS and CTS still up. (This action is done this second time to allow for looping.)	After issuing an OUT X'43' (with the transmit mode, RTS, and send data bits) while stopped at the transmit line address, in IN X'43' indicated that one of those three bits had failed to set or CTS had dropped. Reg. X'14' contains the received IN X'43' data and reg X'15' indicates the bits in error:	Y4G2	0B20		A-180 A-200	Test error. Rerun and loop on routines given below;
			Byte 0:					
			Bit 4-transmit mode bit failed			RS308		Rerun routine 151A.
			Bit 6-RTS bit failed			RS308		Rerun routine 1526.
			Bit 7-Send data bit failed			RS308		Rerun routine 1522.
			Byte 1:					
			Bit 2-CTS had dropped			RS307		Rerun routine 1578.
15CE	0X33	Force a bit service interrupt from the selected receive line interface.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in reg. X'11'	Y4F2,Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
15CE	0X34	Check that Data Set Ready is up on the selected receive line address.	With the scanner stopped at the selected address (found in reg X'11'), an IN X'43' indicated that DSR was not up. If this is a switched line, completion of the autoanswer function should have brought it up. If this is a leased line, it should be up all the time. Reg X'14' contains the results of the IN X'43'.		0020			Pretest error. This failure also can be scoped while stopped at the error stop.
15CE	XXXX	Note: At this point the routine will display X'E00C' in Display B while waiting for the receive line to see a mark.						See the note preceding error code 0X31 and the description of informational display X'E00C' for more information.
15CE	0X36	Set the selected receive line interface to interrupt mode 11 with data terminal and the other selected line line control bits on.	After issuing an OUT X'42' at the selected line address, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the actual IN X'15' contains the bits in errors:	Y4G2	03FF		A-150	Pretest error. Reg X'11' contains the selected line address. Rerun the appropriate routine as given:
			Byte 0:					
			Bit 6-mode bit 1 failed to set			RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority bit set in error			RS304	A-170	Rerun routine 1540.
			Bit 1-diagnostic mode set in error			RS306	A-160	Rerun routine 153C.
			Bit 2-data terminal ready failed to set			RS306	A-160	Rerun routine 1532.
			Bit 3-synchronous mode bit failed			RS306	A-160	Rerun routines 152A & 152C.
			Bit 4-external clock bit failed			RS306	A-160	Rerun routines 1536 & 1538.
			Bit 5-data rate selected bit failed			RS306	A-160	Rerun routines 152E & 1530.
			Bit 6-oscillator selected bit 1 failed			RS306	A-160	Rerun routines 1542 & 1544.
			Bit 7-oscillator select bit 2 failed			RS306	A-160	Rerun routines 1546 & 1548.
15CE	0X38	Start the scanner and allow another normal bit service level 2 interrupt to occur from the selected receive line address.	Although the selected address is still set to monitor mode 11, after starting the scanner no level 2 interrupt occurred from that line within 30 milliseconds (Reg X'13' contains the lines address.)	Y4G2		RS305	A-040	Test error. Problem is probably an intermittent loss of strobe. Rerun and loop on routine 1580.
15CE	0X3A	Set the selected receive line address to interrupt mode 10 with DTR and other selected control bits on. (If wrap to be in start-stop mode).	After issuing an OUT X'42' while stopped at the line (BCB) address in reg X'13', an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the received IN X'42' data. Reg X'15'	Y4G2	FFFF		A-150	Test error. Rerun and loop on appropriate routines as given below:

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			indicates which bits were in error:					
			Byte 0:					
			Bit 6-mode bit 1			RS304	A-170	Routine 154E
			Bit 7-mode bit 2			RS304	A-170	Routine 1552
			Byte 1:					
			Bit 0-low priority bit			RS304	A-170	Routine 154C
			Bit 1-diagnostic mode bit			RS306	A-160	Routine 153C
			Bit 2-Data Terminal Ready			RS306	A-160	Routine 1532
			Bit 3-synchronous mode bit			RS306	A-160	Routine 152A and 152C.
			Bit 4-external clock bit			RS306	A-160	Routines 1536 and 1538.
			Bit 5-data rate select bit			RS306	A-160	Routines 152E and 1530.
			Bit 6-oscillator select bit 1			RS306	A-160	Routines 1542 and 1544.
			Bit 7-oscillator select bit 2			RS306	A-160	Routines 1546 and 1548.
15CE	0X3C	Start the scanner and allow a normal bit service interrupt from the selected transmit line interface	Since the selected communications line interface is set to mode 11, when the prior bit service interrupt was reset and the scanner started, an interrupt from that line should have occurred within 30 milliseconds and did not.	Y4G2		RS305	A-040	Test error. Rerun routine 1580 to try to find why a strobe was apparently lost. Reg X'11' contains the selected communications line (BCB) address.

15CE XXXX NOTE: All of the remaining errors are those which can occur at any time while continuously wrapping data. They are the result of checks that are made as each bit or character is transmitted or received. At any of these error stops reg X'11' contains the address of a common information and control area for the routine. Reg X'16' will contain the address of the individual transmit and receive lines buffers and control areas. It is hoped that these areas may provide additional helpful failure information. The following describes these areas:

Reg X'11' = address of a two byte common control area, where:

Byte 0:

Bit 0-error occurred while in level 2	Bit 4-ununsed
Bit 1-wrap running in ASCII mode	Bit 5-character service has been requested
Bit 2-wrap running in EBCDIC mode	Bit 6-Transmit line not running
Bit 3-leased lines are being used	Bit 7-receive line not running

Byte 1:

Total (in hex) number of characters in data string to be wrapped.

Reg X'16' = address of 2 byte transmit control field, where:

Byte 0:

Bit 0-BSC mode flag	Bit 4-unused
Bit 1-Pads sent flag	Bit 5-character service has been requested
Bit 2-Start bit sent flag	Bit 6 and
Bit 3-Sending stop bits flag	Bit 7-number of stop bits per character

Byte 1:

Total number of data bits per character.

Reg X'16' + 2 = address of 2 byte receive control field, where:

Byte 0:

Bit 0-BSC mode flag	Bit 4-unused
Bit 1-syn character received	Bit 5-character service has been requested
Bit 2-start bit received	Bit 6 and

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		Bit 3-receiving stop bits	Bit 7-number of stop bits per character					
		Byte 1:						
		Total number of data bits per character.						
		Reg X'16' + 4 = address of 2 byte transmit bit control field, where:						
		Byte 0: Character currently being sent (shifted right by number of bits sent so far)						
		Byte 1: Number of bits of this character sent thus far						
		Reg X'16' + 6 = address of 2 byte receive bit control field where:						
		Byte 0: That portion of the current character received thus far (left-justified)						
		Byte 1: Number of bits of this character receive thus far						
		Reg X'16' + 8 = address of 2 byte transmit character control field, where:						
		Byte 0: Transmit character buffer (next character to be sent)						
		Byte 1: Displacement into data string of that character						
		Reg X'16' + 10 (X'A') = address of 2 byte receive character control field, where:						
		Byte 0: Receive character buffer (last complete character received)						
		Byte 1: Displacement into data string of what that character should be						
		Reg X'16' + 34 (X'22') = address of data string (63 bytes long maximum)						
15CE	0X3E	As each character is received, ensure that it is equal to the expected receive character.	After having completed assembling a character, the character received (in reg. X'13', byte 0) was compared to the character expected (in reg X'15', byte 0) and the two were not identical.					Continuing from this error will always cause a loop back to wrapping data. See comments preceding error codes 0X02, and this one.
15CE	0X40	Ensure that a character service interrupt occurs from both the transmit and receive lines at least every 500 milliseconds.	For some reason, either the transmit or receive lines or both have stopped operating or never started. Look at the common control area to see which is not running. Analyze the transmit and receive control fields to find out why. Look at such things as the pads sent, syn received, start bit sent, etc., flags.					Continuing from this stop will always cause a loop back to wrapping data. See comments preceding error codes 0X02, and 0X3E.
15CE	0X42	Ensure that no bit service interrupts occur from lines other than those being wrapped.	An interrupt occurred from a line other than the transmit or receive lines. Reg X'14' contains the address that interrupted.					Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.
15CE	0X44	As each transmit bit service interrupt occurs, ensure that no line errors are present.	After a bit service interrupt from the transmit line, an IN X'43' indicated an error. Reg X'14' contains the results of the IN X'43'. Reg X'15' contains the bits in error:		2A88			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			Byte 0: Bit 2-interface check summary bit was on Bit 4-transmit mode bit reset in error Bit 6-RTS dropped Byte 1: Bit 0-CTS dropped Bit 4-TTY echo check occurred					(Check summary may be on because of a feedback check, DSR dropping, or a bit overrun)
15CE	0X46	Each time a start bit is transmitted, ensure that no error conditions are present. (Start-stop mode only)	After issuing an OUT X'43' to the transmit line (with data of X'000A') to send a start bit, an IN X'43' indicated a failing condition. Reg. X'14' contains the received IN X'43' data and reg. X'15' contains the bits in error as described in error code 0X48, below.		2B80			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.
15CE	0X48	Each time a data bit is transmitted, ensure that it was indeed sent. (Start-stop mode only)	After issuing an OUT X'43' to the transmit line to send a bit, an IN X'43' indicated a failure. Reg X'14' contains the results of the IN X'43' and reg. X'15' contains the error bits: Byte 0: Bit 2-interface check summary bit was on Bit 4-transmit mode dropped Bit 6-RTS dropped Bit 7-Send data failed Byte 1: Bit 0-CTS dropped		2B80			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E. (Interface check summary may be on because of a feedback check, DSR dropping, or a bit overrun.)
15CE	0X4A	Each time a stop bit is sent, ensure that no error conditions are present (Start-stop mode).	After issuing an OUT X'43' to the transmit line with data of X'000B' to send a stop bit, an IN X'43' indicated a failure. Reg X'14' contains the IN X'43' data and reg X'15' contains the error bits as described in error code 0X48, above.		2B80			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.
15CE	0X4C	As each pad bit is sent, ensure that no error conditions exist on the transmit line. (Bisync mode only)	After issuing an OUT X'43' to the transmit line to send a pad bit, an IN X'43' indicated a failure. Reg X'14' contains the results of the IN X'43' and reg X'15' contains the bits in error as described in error code 0X48.		2B80			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.
15CE	0X4E	As each data bit is sent, ensure that no error conditions are present on the transmit line. (Bisync only)	After issuing an OUT X'43' to the transmit line to send a data bit, an IN X'43' indicated a failing line condition. Reg X'14' contains the results of the IN X'43' and reg X'15' contains the bits in error as described in error code 0X48.		2B80			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15CE	0X50	As each receive bit service interrupt occurs, ensure that no line errors are present.	After a bit service interrupt from the receive line, an IN X'43' indicated an error on the line. Reg X'14' contains the results of the IN X'43' Reg X'15' contains the bits in error: Byte 0: Bit 2-Interface check summary bit was on Bit 4-Transmit mode bit was set in error. Byte 1: Bit 3-RLSD dropped		2810			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E. (Check summary may be on because of a feedback check, DSR dropping, or a bit overrun.)
15CE	0X52	As the first bit of each character comes in, ensure that it is a space (start) bit. (Start-stop mode only.)	After each start-stop character is received, the receive line is placed in monitor mode 10 to look for the next start bit. After the next interrupt, an IN X'43' indicated that receive data was not a space. Monitor mode 10 should allow an an interrupt only when receive data is a space or DSR drops. Reg X'14' contains the results of the IN X'43'.		8000			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.
15CE	0X54	After each start bit is received, set the receive line to monitor mode 11 to receive the rest of the character. (Start-stop mode only.)	After issuing an OUT X'42' to set the receive line to monitor mode 11, an IN X'42' failed to reflect the OUT X'42'. Reg X'14' contains the results of the IN X'42'. Reg X'15' contains the bits in error: Byte 0: Bit 6-mode bit 1 failed to set Bit 7-mode bit 2 failed Byte 1: Bit 0-low priority bit set in error. Bit 1-diagnostic mode set in error Bit 2-DTR dropped Bit 3-synchronous mode bit failed Bit 4-external clock bit failed Bit 5-data rate selector bit failed Bit 6-oscillator select bit 1 failed Bit 7-oscillator select bit failed		FFFF			Continuing from this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E. It may help to rerun routines indicated below. Rerun 154E Rerun 1552 and 1554. Rerun 1540 Rerun 153C Rerun 1532 Rerun 152A and 152C Rerun 1536 and 1538 Rerun 152E and 1530 Rerun 1542 and 1544 Rerun 1546 and 1548
15CE	0X56	After all data bits of each character have come in, check that the proper number of stop bits are received. (Start-stop mode only.)	After an entire character was received, one of the ensuing bits was not a mark (stop bit). Reg X'14' contains the data received by an IN X'43' from the receive control fields to determine which stop bit was not received. The receive		8000			Continuing from this error stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			control field contains the total expected stop bit count and the count portion of the receive bit control field contains the number of stop bits received thus far.					
15CE	0X58	After an entire character, including stop bits, has been received, set monitor mode 10 to wait for the start of the next character. (start-stop mode only.)	After issuing an OUT X'42' to set the receive line to monitor mode 10, an IN X'42' failed to reflect the OUT X'42'. Reg. X'14' contains the results of the IN X'42' and reg X'15' contains the bits in error as described in error code 0X54.		FFFF			Continuing from this error stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E.
15CE	0X5A	After having assembled an	Before requesting the character					Continuing from
15CE	0X5C	entire received character, request a character service interrupt. (0X5A is issued when in start-stop mode and 0X5C is issued when in bisync mode.)	service interrupt, a check found that the previous character received had not yet been serviced. Probably, the previous character service interrupt request was never honored.					this stop will cause a loop back to wrapping data. See comments preceding error codes 0X02 and 0X3E. Try rerunning routines 15B3 through 15BC.
15D0	XXXX	Data Set Ready - Active (Manual Intervention Routine): Ensure that when Data Set Ready is active on the communications line interface, it is indicated as being active in an IN X'43'. (The operator selects the particular line address to be tested.) After forcing a bit service interrupt from the tested address, Data Terminal Ready is set and a test is then made to ensure that an IN X'43' indicates that Data Set Ready is active.						
15D0	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D0	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.
15D0	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D0	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
15D0	0X05	Ensure that when data set ready is active on the communications line interface, it is so indicated in an IN X'43'.	An IN X'43' failed to indicate that Data Set Ready was active. (Byte 1, bit 2 was on and should have been off.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0020	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15D1	XXXX	Autocall EIA test (Manual Intervention Routine): Insure that all auto call EIA Receivers and drivers can be activated at the communications line interface. (The operator selects the particular line address to be tested.) After forcing a bit service interrupt from the line under test, each autocall interface line in turn is set on and one interface line is tested to see if it is up. If the line is up the program steps to the next pair of interface lines. If the interface line is not up, the program stops with a Manual Intervention code telling the operator which line to bring up. NOTE: Digits NB8, NB4, NB2, and NB81 are turned on each time except when that individual Digit is being tested. This keeps all the EIA lines down except the line being tested.						
15D1	0X01	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X02	Insure that Call Request can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X03	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X04	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15D1	0X05	Insure that Power Indicator can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X06	Insure that Digit Present can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X07	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X08	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X09	Insure that DLO can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X0A	Insure that Digit NBR 8 can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface.

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.					Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X0C	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X0E	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X10	Insure that PND can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X12	Insure that Digit NBR 4 can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	SB212	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X14	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15D1	0X16	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X18	Insure that Abandon Call can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X1A	Insure that Digt NBR 2 can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X1C	Insure that force bit service (OUT X'47') causes a bit service irterrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X1E	Insure that forse bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to forse a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	petest error Rerun routine 1512.
15D1	0X20	Insure that COS can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in

RCUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETHM PAGE	COMMENTS
								the associated line interface.
15D1	0X22	Insure that Digit NBR 1 can be set with a Out X'43'	An IN '43' indicated that bits set in error or failed to set because of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib, or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D1	0X24	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X26	Insure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D1	0X28	Insure that Data Line Occpied can be set with a	An IN '43' indicated that bits set in error or failed to set bexause of the Output X'43'. Reg X'15' contains the bits in error. Reg X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0F08	RS307	A-200	Test error. Problem may be in CS, lib or line interface. Try testing other lines. If failure appears to be isolated to a lib, try replacing the lib isolation card. If only one line fails failure is in the associated line interface.
15D2	XXXX	Data Set Ready - Inactive (Manual Intervention Routine): Ensure that when Data Set Ready is inactive on the communications line interface, it is indicated as being inactive in an IN X'43'. (The operator selects the particular line address to be tested.) After forcing a bit service interrupt from the tested address, Data Terminal Ready is set and a test is then made to ensure that an IN X'43' indicates that Data Set Ready is inactive.						
15D2	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D2	0X02	Ensure that the data terminal ready (DTR) bit	Either the DTR bit failed to set or other bits in IN X'42'	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.					1532.
15D2	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D2	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D2	0X05	Ensure that when data set ready is inactive on the communications line interface, it is so indicated in an IN X'43'.	An IN X'43' failed to indicate that Data Set Ready was inactive. (Byte 1, bit 2 was off and should have been on.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0020	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15D4	XXXX	Carrier Detect - Active (Manual Intervention Routine): Ensure that when carrier detect is active on the communications line interface, it is indicated as being active in an IN X'43'. (The operator selects the particular line address to be tested.) After forcing a bit service interrupt from the tested address, Data Terminal Ready is set and a test is then made to ensure that an IN X'43' indicates that carrier detect is active.						
15D4	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D4	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.
15D4	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11',	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
15D4	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D4	0X05	Ensure that when carrier detect is active on the communications line interface, it is so indicated in an IN X'43'.	An IN X'43' failed to indicate that carrier detect was active. (Byte 1, bit 2 was off and should have been on.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0020	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15D6	XXXX	Carrier Detect - Inactive (Manual Intervention Routine): Ensure that when carrier detect is inactive on the communications line interface, it is indicated as being inactive in an IN X'43'. (The operator selects the particular line address to be tested.) After forcing a bit service interrupt from the tested address, Data Terminal Ready is set and a test is then made to ensure that an IN X'43' indicates that carrier detect is inactive.						
15D6	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D6	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03ff	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.
15D6	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D6	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			pass, no bit service interrupt occurred from that line.					
15D6	0X05	Ensure that when carrier detect is inactive on the communications line interface, it is so indicated in an IN X'43'.	An IN X'43' failed to indicate that carrier detect was inactive. (Byte 1, bit 2 was on and should have been off.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0010	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15D8	XXXX	Receive Data - Space (Manual Intervention Routine): Ensure that when receive data is a space on the communications line interface, received data lead is on in an IN X'43'. (The operator selects the particular line address to be tested.) After forcing a bit service interrupt from the tested address, Data Terminal Ready is set and a test is then made to ensure that an IN X'43' indicates that received data lead is on.						
15D8	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D8	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.
15D8	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D8	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15D8	0X05	Ensure that when receive data is a space on the communications line interface, received data lead is on in an IN X'43'.	An IN X'43' failed to show received data lead on. (Byte 0, bit 3 was off and should have been on.) Reg. X'14' contains the received IN X'43' data and reg. X'11' contains the line address under test.	Y4G2	1000	RS307	A-200	Test error. Problem may be in the CS, LIB. or line interface Try testing other lines. If failur appears to be isolated to a LIB

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15DA	XXXX	Receive Data - Mark (Manual Intervention Routine): Ensure that when receive data is a mark on the communications line interface, received data lead is off in an IN X'43'. (The operator selects the particular line address to be tested.) After forcing a bit service interrupt from the tested address, Data Terminal Ready is set and a test is then made to ensure that an IN X'43' indicates that received data lead is off.						
15DA	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15DA	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.
15DA	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15DA	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15DA	0X05	Ensure that when receive data is a mark on the communications line interface, received data lead is off in an IN X'43'.	An IN X'43' failed to show received data lead off. (Byte 0, bit 3 was on and should have been off.) Reg. X'14' contains the received IN X'43' data and reg. X'11' contains the line address under test.	Y4G2	1000	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15DC	XXXX	Ring Indicator - Active (Manual Intervention Routine): Ensure that when ring indicator is active on the communications line interface, it is indicated as being active in an IN X'43'. (The operator						

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		selects the particular line address to be tested.) After forcing a bit service interrupt from the tested address, Data Terminal Ready is set and a test is then made to ensure that an IN X'43' indicates that ring indicator is active.						
15DC	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15DC	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routines 1532.
15DC	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15DC	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15DC	0X05	Ensure that when ring indicator is active on the communications line interface, it is so indicated in an IN X'43'.	An IN X'43' failed to indicate that ring indicator was active. (Byte 1, bit 1 was off and should have been on.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0040	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15DE	XXXX	Ring Indicator - Inactive (Manual Intervention Routine): Ensure that when ring indicator is inactive on the communications line interface, it is indicated as being inactive in an IN X'43'. (The operator selects the particular line address to be tested.) After forcing a bit service interrupt from the tested address, Data Terminal Ready is set and a test is then made to ensure that an IN X'43' indicates that ring indicator is inactive.						
15DE	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			waiting the time of a scanner pass, no bit service interrupt occurred from that line.					
15DE	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.
15DE	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15DE	0X04	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15DE	0X05	Ensure that when ring indicator is inactive on the communications line interface, it is so indicated in an IN X'43'.	An IN X'43' failed to indicate that ring indicator was inactive. (Byte 1, bit 1 was on and should have been off.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0040	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15E0	XXXX	Clear to Send (Manual Intervention Routine): Ensure that Clear to Send in IN X'43' correctly indicates the state of Clear to Send on the communications line interface. (The operator selects the line address to be tested.) After forcing a bit service interrupt from the tested line address, Data Terminal Ready, transmit mode, send data, and Request to Send are set. A test is then made to ensure that Clear to Send became active within 30 seconds. Request to send is then dropped, and a test made to ensure that Clear to Send drops within 5 seconds. send drops within 5 seconds.						
15E0	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E0	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.					
15E0	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E0	0X04	Ensure that transmit mode, send data (mark), and Request to Send have been set in the line interface under test.	After issuing an OUT X'43' with data of X'000B', an IN X'43' indicated that the expected bits were not set. Reg. X'14' contains the received IN X'43' data and reg. X'15' indicates the bits that were not set: Byte 0: Bit 4-transmit mode Bit 6-Request to Send Bit 7-send data	Y4G2	0B00	RS308	A-200	Test error. Rerun appropriate routine as shown below. Reg. X'11' contains the line address under test, if needed. Rerun routine 151A Rerun routine 1526 Rerun routine 1522
15E0	0X05	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E0	0X06	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E0	0X07	Ensure that when clear to send is active on the communications line interface, it is so indicated in an IN X'43'.	An IN X'43' failed to indicate that Clear to Send was active. (Byte 1, bit 0 was on and should have been off.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0080	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15E0	0X08	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E0	0X09	Ensure that force bit	After attempting to force a	Y4F2, Y4G2		RS305	A-330	Pretest error.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		service (OUT X'47') causes a bit service interrupt from the line address under test.	bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.				A-040	Rerun routine 1512.
15E0	0X10	Ensure that when clear to send is inactive on the communications line interface, it is so indicated in an IN X'43'.	An IN X'43' failed to indicate that Clear to Send was inactive. (Byte 1, bit 0 was off and should have been on.) Reg. X'14' contains the received IN X'43' data. Reg. X'11' contains the line address under test.	Y4G2	0080	RS307	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15E4	XXXX	New Sync Active (Manual Intervention Routine): This routine sets the new sync bit and leaves it active so that it can be checked externally on the communications line interface. (The operator selects the line address to be tested.)						
15E4	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E4	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.
15E4	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E4	0X04	Ensure that the new sync/NBR-4 bit in IN X'43' can be set by issuing an OUT X'43' with byte 1, bit 5 on.	Either the new sync/NBR-4 bit failed to act correctly or other bits turned on in error in the IN X'43'. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains the bits in error. (Byte 0, bit 5 indicates a new sync/NBR-4 bit error.) Reg X'14' contains the actual data	Y4G2 Y4E2		RS308 RS106	A-200 A-290	Test error. The problem is probably in the associated line interface. (See General Comment, #3.) If other bits are in error also, some kind of interaction occurred.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			received by the IN X'43'.					If byte 0, bit 5 is on in both Reg. X'14' and X'15', the line address tested was a start stop interface and the new sync/NBR-4 bit set and should not have.
15E6	XXXX	Telegraph Echo Check (Manual Intervention Routine): After the operator has selected the address to test and has indicated whether or not the telegraph communications line is connected to the interface or not, a test is made for the proper condition of telegraph echo check when a mark is transmitted.						
15E6	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E6	0X02	Ensure that an OUT X'42' has set mode 11 and has properly selected an oscillator.	After stopping the scanner and issuing an OUT X'42', an IN X'42' indicated that mode 11 was not set or the proper oscillator select bits were not set (or other bits were set in error). Reg. X'14' contains the actual data received by the IN X'42' Reg. X'15' contains the bits in error:		03FF		A-150	Pretest error, Rerun routines specified below. Reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.	Y4G2		RS304	A-170	Rerun routine 154E.
			Bit 7-mode bit 2 failed to set.	Y4G2		RS304	A-170	Rerun routine 1552
			Byte 1:					
			Bit 0-low priority set in error.	Y4G2		RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode set in error.	Y4G2		RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-Data Terminal Ready set in error.	Y4G2		RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.	Y4G2		RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.	Y4G2		RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select bit set in error.	Y4G2		RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 failed to set or was set in error.	Y4G2		RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 failed to set or was set in error.	Y4G2		RS306	A-160	Rerun routines 1546 and 1548.
15E6	0X03	Ensure that the transmit line has properly been set to transmit mode and that send data is a mark.	Following an OUT X'43' with data of X'000B' to set send data, Request to Send, and transmit mode, an IN X'43' indicated either one of them failed to set or a feedback check occurred. Reg. X'14' contains the received IN X'43' data and reg. X'15' contains the bits in error:	Y4G2	4900		A-200	Pretest error. Rerun appropriate routine as given below. (If needed, reg. X'11' contains line address under test.)
			Byte 0:					
			Bit 1-a feedback check occurred.			RS202	A-180	Rerun routines 157A and 157C.
			Bit 4-transmit mode			RS308	A-180	Rerun routines

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			failed to set.					151A and 151C.
			Bit 5-New sync was set in error			RS308	A-180	Rerun routines 1518 and 1520
			Bit 6-Request to send failed to set			RS308	A-180	Rerun routine 1526.
			Bit 7-send data failed to set.			RS308		Rerun routines 1522 and 1524.
15E6	0X04	Ensure that the first oscillator has created a strobe and caused a bit service level 2 interrupt from the tested line.	After having set monitor mode 11 to allow normal bit service requests, selecting oscillator 0, starting the scanner and waiting up to 30 milliseconds for a bit service level 2 interrupt from the line under test, none occurred.	Y4H2		RS401	A-250	Pretest error. Rerun routine 1580.
15E6	0X05	Ensure that carrier detect is up on the tested address and that none of the bits previously set have dropped.	After allowing an interrupt to stop the scanner, an IN X'43' indicated that carrier detect was not up on the line under test or other bits had dropped. Reg. X'14' contains the received IN X'43' data and reg. X'15' indicates which bits were in error:	Y4G2	0B10		A-200	Test error. Rerun appropriate routines as given below. (Reg. X'11' contains line address under test.)
			Byte 0:					
			Bit 4-transmit mode dropped.			RS308	A-180	Rerun 151A.
			Bit 6-Request to Send dropped.			RS308	A-180	Rerun 1526.
			Bit 7-send data was no longer a mark.			RS308	A-180	Rerun 1522.
			Byte 1:					
			Bit 3-carrier detect was not up.			RS307	A-180	Rerun 15D4.
15E6	0X06	Ensure that telegraph echo check reacts correctly to sending a mark.	After sending a mark to an installed telegraph line an echo check should not have occurred and did (or if the line was not installed, an echo check did not occur). Echo check is byte 1, bit 4 an IN X'43'. Reg. X'14' contains the expected condition of echo check.	Y4G2	0080	RS308	A-200	Test error. Problem may be in the CS, LIB, or line interface. Try testing other lines. If failure appears to be isolated to a LIB, try replacing the LIB isolation card. If only one line fails, failure is in the associated line interface.
15E8	XXXX	Monitor Mode 01 (Manual Intervention Routine): After the operator selects the line address to test, a test is made to ensure that monitor mode 01 (monitor for ring indicator or Data Set Ready) will allow a level 2 bit service interrupt when either Data Set Ready or ring indicator become active.						
15E8	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E8	0X02	Ensure that the data terminal ready (DTR) bit in IN X'42' can be set by issuing OUT X'42' with byte 1, bit 2 on.	Either the DTR bit failed to set or other bits in IN X'42' were set in error. Reg. X'11' contains the line (BCB) address under test. Reg. X'15' contains	Y4G2 Y4E2	03FF	RS306 RS106	A-160 A-270	Pretest error. Rerun routine 1532.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			the bits in error. (Byte 1, bit 2 on indicates a DTR bit failure.) Reg. X'14' contains the actual data received by IN X'42'.					
15E8	0X03	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15E8	0X04	Ensure that monitor mode 01 has been set at the line address under test.	After finding Data Set Ready or ring indicator on at the tested address, an OUT X'42' was issued to set mode 01. An IN X'42' then indicated mode 01 was not set. If byte 0, bit 6 of reg. X'15' is on, mode bit 1 failed to reset. If bit 7 is on, mode bit 2 failed to set.	Y4G2	0300	RS304	A-170	Pretest error. Rerun routines 154E through 1554. If needed, reg. X'11' contains the line address under test.
15E8	0X05	Ensure that ring indicator or Data Set Ready are still active on the tested line address.	Cuation: This may not actually indicate a hardware failure. Before waiting for an interrupt, Data Set Ready or ring indicator was active. Now, after waiting for the interrupt, neither is active. Conditions on the line connected to the line interface under test have changed. This invalidates error code 0X06 which you should get after this failure.	NONE		NONE	NONE	Test error. If it is desired to find out what conditions on the line have changed, display reg. X'15'. Byte 1, bit 1 on indicates ring indicator has dropped. Byte 1, bit 2 on indicates Data Set Ready has dropped. Reg. X'11' contains the line address under test.
15E8	0X06	Ensure that monitor mode 01 allows an interface service request to cause a level 2 interrupt when Data Set Ready or ring indicator are active.	After having found ring indicator or Data Set Ready active, setting monitor mode 01, and waiting a bit time, no level 2 interrupt occurred from the tested line address.	Y4G2		RS305	A-040	Test error. Problem is most probably in the CS. (See General Comments, #3.) If needed, the tested line address may be found in reg. X'11'.
15EA	XXXX	Interrupt Mode 10: After setting 'Data Terminal Ready' in an attempt to bring up 'Data Set Ready' from the communications line on the tested line address, the condition of Data Set Ready is determined. Monitor mode 10 is set, and a check is made for the presence of level 2 interrupts according to the state of 'Data Set Ready'. Monitor mode 10 should allow level 2 interrupts whenever Data Set Ready is inactive for at least one bit time. This test can be run on all installed non-autocall line interfaces. The CE must select the line address to be tested. The test is bypassed if the line happens to be receiving a space.						
15EA	0X01	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
15EA	0X02	Ensure that force bit service (OUT X'47') causes a bit service interrupt from the line address under test.	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the line (BCB) address in Reg. X'11', unmasking level 2 interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4P2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15EA	0X03	Ensure that LIBs that have Data Set Ready tied up, Data Set Ready is indeed up.	After forcing the scanner to stop at the tested address, an IN X'43' indicated data set ready was off (byte 1, bit 2 was on). (Reg. X'11' contains failing line address.)	Y4G2	0020	RS307	A-200	Pretest error. Problem is probably in the associated line interface or LIB.
15EA	0X04	Ensure that an OUT X'42' has set monitor mode 10, and has kept data terminal ready on.	While the scanner was stopped for the prior bit service, an OUT X'42' was issued to set the proper modes. An IN X'42' then indicated that the proper bits were not set or other bits were set in error. Reg. X'14' contains the actual data received by the IN X'42' and reg. X'15' indicates the bits in error:	Y4G2	03FF		A-150	Pretest error. Rerun appropriate routines as specified below. If needed, reg. X'11' contains the line address under test.
			Byte 0:					
			Bit 6-mode bit 1 failed to set.			RS304	A-170	Rerun routine 1550.
			Bit 7-mode bit 2 set in error.			RS304	A-170	Rerun routine 1552.
			Byte 1:					
			Bit 0-low priority set in error.			RS304	A-170	Rerun routines 154A and 154C.
			Bit 1-diagnostic wrap mode set.			RS306	A-160	Rerun routines 153A and 153C.
			Bit 2-Data Terminal Ready reset in error.			RS306	A-160	Rerun routines 1532 and 1534.
			Bit 3-synchronous mode set in error.			RS306	A-160	Rerun routines 152A and 152C.
			Bit 4-external clock bit set in error.			RS306	A-160	Rerun routines 1536 and 1538.
			Bit 5-data rate select set in error.			RS306	A-160	Rerun routines 152E and 1530.
			Bit 6-oscillator select bit 1 is set.			RS306	A-160	Rerun routines 1542 and 1544.
			Bit 7-oscillator select bit 2 set.			RS306	A-160	Rerun routines 1546 and 1548.
15EA	0X05	Dependent upon state of Data Set Ready (see routine description), ensure that monitor mode 10 allows or prevents level 2 bit service interrupts from the tested address.	After setting mode 10 and waiting one bit time for an interrupt, an interrupt did or did not occur in error. Reg. X'14' describes what occurred. If byte 0, bit 0 is off, Data Set Ready was off and therefore an interrupt should have occurred and did not. If on, Data Set Ready was on and an interrupt should not have occurred and did.	Y4G2		RS305	A-040	Test error. Problem is probably in the CS. If needed, reg. X'11' contains the tested line address. (See General Comments, #3.)

15F0 XXXX SDLC LINK TEST. This is a manual intervention routine and will not be run unless you set the CE sense switch to run manual intervention routines or unless you requested a single routine to be run.

This routine stops with manual intervention stop codes F070 through F07C waiting for you to enter options needed to run this routine. These stop code definitions are listed in the T1CS-MAN section in Chapter 9.2 of this manual.

This routine may be used for SDLC data link problem determination and repair verification when on-line tests (under host system control) are not available.

When using this routine for problem determination external to the 3705, all normal internal functional tests should run normally without internal hardware errors. Local interface problems, such as line set drivers and

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terminators, should be tested using routine 15CE with external local wrap options because that routine provides more detailed information about local failures.

This SDLC link test is basically an ECHO test. The primary SDLC station sends a SDLC link test command frame down the link and expects to receive the same test frame back; provided the remote end of the link received the test frame without errors. Some SDLC terminals only respond with a non-sequenced acknowledgement response rather then sending back the link-test frame received.

Options are provided to run as a SDLC primary station or as a SDLC secondary station. The primary station option initiates the link-test commands and expects to receive responses. The secondary SDLC station responds to test-frames received; if the test frame was received without errors, the secondary station sends back the same test frame as a response. If a test frame was received without block check errors and had either more data than could be buffered or did not have the poll bit on in the control field, the secondary station responds with a command reject frame. All frames received with block check errors or with abort detect conditions are counted as errors and no response is provided. All frames received with a SDLC station address other than the SDLC station address selected in the F078 manual intervention stop code are counted as an unexpected or non-supported frame and no response is provided. No response is provided for frames received with anything but a link-test command field.

The structure of the link-test command enables this test to also run a local external duplex modem wrap if you select the primary station option and connect the transmit and receive lines together properly. A remote wrap can be done if the remote end of the link can tie the transmit and receive duplex lines together with proper loading etc. Because the remote node (on half-duplex links) must store the received frame and send it back, this wrap option will not work on half-duplex lines.

This routine always stops on transmit errors such as modem check, timeout or overrun, but does not stop on receive errors except for modem check error unless an option is selected to stop on frames in error or stop on any frame.

Continuation (select function 5 and press START key) from the 0X20, 0X60, or 0X61 stops, the routine clears all error counts and summary statistics and restarts the test from the transmit/receive data portions. This allows continueing the test on a manual switched line connection without making a new connection. The same restart is used for the D000 dynamic restart option or the D000 restart option at stop code F07C. Any manual switched line connection is not broken until you abort the routine or use a restart option that goes through total hardware setup such as D002 restart code.

15F0 ---- The format of all transmissions from this LINK-TEST are:

Pad Pad F A C dd BC BC F ee

where-

Pad = Alternate data transitions characters for clock correction and will be X'AA' if NRZI mode is not being used or X'00' if NRZI mode is being used.

F = SDLC flag character composed of a zero bit followed by six one bits followed by another zero bit (X'7E').

A = SDLC station address.

C = SDLC control field and will either be X'F3' if a LINK-TEST command/response is being sent or X'97' if a command reject response is being sent.

dd = Optional transmit/receive data field when the LINK-TEST command is being used. When the command reject response is being sent the first byte of this field is the command field of the received frame that is being rejected, the second byte is set to zeros (it is defined as the send and receive sequence counts) and the third byte is set to X'04' if more data was received than could be buffered; or to X'01' if the LINK-TEST command was received without the poll bit on.

BC = Block check (CRC) characters. Two block check characters are always sent and their bit configuration vary according to the SDLC station address, control field and optional data fields.

ee = An ending transmission of X'FF' to make line go to an idle state and to allow time for bits to be sent before dropping the 'request to send' lead on transmit turnarounds.

This routine refers to a frame as that segment of transmitted or received data defined above and enclosed between two flag characters. If the frame above is being sent/received in NRZI mode, the actual bit configuration on the line and the ones shown above will be different. Also SDLC zero bit insertion/deletion will apply to all characters except the flags and ending sequence defined under ee.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS

Test statistics and error count are available while the test is running and at the F07C test completion code.
In addition, certain registers are used for current status indicators and may be displayed while the test is running or at the F07C stop code.
Following is the definition of the status indicators:

15F0 ---- X'1E' Register contains the current transmit and receive line status.

Byte 0 of reg X'1E' = last received frame type indicator and may contain one of the following indications:

X'00' = Timeout occurred on last receive completion.

X'80' = A good link test frame was received with no errors.

X'40' = A command reject response was received as the last frame received at this primary station.

X'20' = A non-sequenced acknowledgement was received as the last frame at this primary station.

X'10' = A block check (CRC error) was detected in the last received frame.

X'08' = An invalid or non-supported frame was received as the last received frame. This link test only supports the link-test response, the non-sequenced acknowledgement response and the command reject response if running as a primary station. The secondary station option will only accept a link-test command but may respond with a link-test response or a command reject response. This type indicator is also set if a partial frame was received followed by an 'abort detect' sequence of seven or more consecutive one bits.

X'04' = A valid link-test frame was received but it contained more data than could be buffered. If this is a secondary station, a command reject response will be sent for this frame. The maximum length of the receive (and transmit) data buffer is 1024 characters if this 3704 has more than 16K storage or 10 characters if 3704 has only 16K of storage.

X'02' = Invalid SDLC station address received or, for primary station option with optional transmit data, the received data did not compare with the SDLC station address or optional transmit data that was sent. The SDLC station address provided in the F078 stop code is used to make this comparison. If the secondary station option was selected, no response will be provided for this frame.

X'01' = A hardware detected error such as modem check or overrun has been detected. No response will be made to any frames received with this type of error.

Byte 1 of reg X'1E'= transmit line status and other information bits. Multiple bits may be on in this byte as opposed to byte 0 which never will have more than one bit on. The bits within this byte are defined as:

X'80' = A reply is pending to be sent to the last frame received at this secondary station.

X'40' = A command reject reply is now being sent or was the last frame transmitted from this secondary station.

X'20' = A link-test command (from primary station) or response (from secondary station) was the last frame sent or is being sent at this time.

X'10' = A 'transmit initial' operation is being done or was the last transmit operation done. This 'transmit initial' is done to set 'request to send' and wait for 'clear to send' from the modem interface for the first transmit operation of all primary station options and for secondary station options when 'request to send' should be on at all times. See manual intervention stop code F070 for this option.

X'08' = Transmit line is busy if this bit is on.

X'04' = Receive line is busy if this bit is on.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS

X'02' = Bit not defined. May be used as added indicator at later time.

X'01' = Bit not defined. May be used as added indicator at later time.

15F0 ---- X'1F' Register contains the accumulated transmit and receive line status indicators. The bits in this register have the same meanings as the bits defined in the register X'1E' except once these bit are set on they are not reset until the test is restarted. These bits serve as a summary of all the transmit and receive operations that have occurred up to the time this register is displayed.

15F0 ---- X'1D' Register is used to control the E0?? display code that is displayed in the panel display B lights (if function 4, 5 or 6 is selected). This register is cleared to zeros at approximately two second intervals and in between this clearing to zeros it is used as an accumulator of all the bits defined in the bits in register X'1E'.

15F0 ---- E0?? Display codes. While the link-test is running, various display codes are in the display B lights if the FUNCTION SELECT switch is set to function position 4, 5 or 6. These display codes (except E06F) are displayed approximately once every other second with the display B lights cleared to zero between each E0?? display. The E0?? display codes are defined as follows:

E000 Alternating with E0FF = waiting for 'data set ready' to come on before doing any transmit or receive operations. These codes will be continously displayed until 'data set ready' comes on via completing a manual switched connection or via connecting (or jumpering) the proper modem interface leads. On a leased line connection you will not see this display code if 'data set ready' is always on (as expected).

E060 = A good test frame was received within the last two seconds and no other error was detected (except a possible timeout) during that time.

E061 = Nothing was received (timeouts) during the last two seconds.

E062 = A block check error (CRC error) was detected during the last two seconds.

E063 = A non-supported or invalid frame was received during the last two seconds.

E064 = More data was received than could be buffered during the last two seconds.

E065 = A command reject response was received at this primary station during the last two seconds.

E066 = A non-sequenced acknowledgement was received at this primary station during the last two seconds.

E067 = Either of 3 conditions may exist:

1 - SDLC station address did not compare equal.
2 - Received data did not compare equal to the transmitted data.
3 - Secondary station received more data than could be buffered.
In all cases 'E067' indicates that the data received does not compare equal to the data transmitted.

E068 = A hardware detected error such as modem check or overrun has been detected during the last two seconds.

E06F = This code is displayed if you are using the dynamic communications option (function select 1 and switches B-E set to D0??) and have entered a D0?? code that is not defined. No action is taken if this code is displayed.

15F0 ---- D0?? Dynamic communications codes. These dynamic communications codes allow termination or restarting the link-test at various points within the test. Enter these codes while the program is running by setting (1) the FUNCTION SELECT switch to function 1, (2) the selected code in switches B-E, and (3) pressing the INTERRUPT key on the control panel. These dynamic communication options are the same as those defined in the F07C manual intervention stop code definition. They are repeated here in a summary form. For more details see the F07C stop code definition.

D000 = Restart link-test at transmit/receive data point (no line resets).

D001 = Restart routine from beginning including asking for options.

D002 = Restart link-test including hardware resets and enables.

D003 = Stop routine at F07C stop code and display statistics.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS

D004 = Terminate routine after hardware resets.

15F0 ---- STATISTICS at link test termination.

X'1C' Register contains the address of a statistics table in storage. At all times while the test is running and at the F07C and 0X?? stop codes, you may get the storage address of the statistics table from this register and display the storage locations for the following half-word counters. A list of the available statistics follows:

Hex displacement within statistics pointed to by reg X'1C'.

00 = Number of SDLC link-test frames transmitted successfully. This count does not include command reject responses sent from a secondary station.

02 = Number of SDLC link-test frames received with no errors. If this is a primary station then the received SDLC station address and (if used) the optional data must compare in order to have one added to this count. On a normal F07C completion at a primary station this count should match the number of test frames transmitted count if no errors have been detected. An exception is when the secondary station responds with non-sequenced acknowledgements to test frames then this count should be zero and the received non-sequenced acknowledgements count should match the number of test frames transmitted count.

04 = Number of frames received with block check errors (CRC errors).

06 = Number of command reject responses received at this primary station.

08 = Number of non-sequenced acknowledgements received at this primary station.

0A = Number of frames received that were not included in other receive counts. This count includes frames received with invalid SDLC station addresses, non-supported commands/responses, non-data compares with optional transmit data and frames terminated by an abort detection condition. Note that some of these conditions may have caused a block check error and be included in the block check error count and not this count.

0C = If primary station then this field contains number of test frames requested to be sent in the F072 stop code. If this field is all zeros and a primary station option was selected then test frames will be sent continously (allowing for receiving etc) without ever terminating the test.

0E = Number of hardware errors detected, such as modem check or overruns, on the transmit and receive operations.

10 = Number of command reject responses transmitted by this secondary station.

15F0 ---- The error stop codes that may occur in this test follow. Note that any error stop codes beginning with 1 or 2 in display B byte 0 bits 0-3 are defined in another section of this symptom index. The display B codes starting with F are defined in the manual intervention section of this document.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X6F0	0X07	Auto call failed to complete	An auto call error has been detected. Reg. X'15' byte 0 contains an error indicator number. Determine error indicator and see description below. ERROR INDICATOR 1 -- Error in auto call connection. Reg.X'15' byte 1 contains SDF bits in error. SDF bits 0-4 on, 5-7 off. Also an error, if LCD not=3, PCF not=4 (reg. X'45' byte 0). 2 -- Error in dialing. See error indicator 1 description. 4,566 -- If last digit dialed was not an EON digit, PND may come on an cause a L2 interrupt if the distant station does not answer immediately. The same thing will occur with EON, as last digit, on some EOM (non-IBM) and on IBM auto-call units that do not have the EON feature strapped on. On some					Reg.X'15' byte 1= SDF bits 0-7. SDF bit definitions for auto-call are: Bit 0= (IR) intrpt remember. Bit 1= (PWI) power indicator. Bit 2= (CRQ) call request. Bit 3= (DLO) data line occupied. Bit 4= (PND) presen next digit. Bit 5= (DPR) digit present. Bit 6= (COS) call originate status. Bit 7= abandon call and retry.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			EOM auto-call units the EON will cause the auto-call unit to transfere control to the modem/data set with DATA-SET-READY on immediately, even though no distant station has been connected and given an answer tone. 4 -- Error indicating PWI, CRQ or DLO not on. Reg. X'15' byte 1 bits 1,2 & 3 should be on. 5 -- No auto-call completion (timeout). Reg. X'15' byte 1 bit 6 (COS) should be on. 6 -- Abandon-call and retry came on. Reg. X'15' byte 1 bit 7 came on.					
15F0	0X20	Transmit line operations.	A transmit line error has been detected. Reg X'13'=accumulated simulated ICW bits 0-15 during this transmit operation. On each level 2 interrupt simulated ICW bits 0-7 are ORed together and saved for this error display. If reg X'15' byte 0 bit 3(X'10') is on then the transmit line has timed out due to 'clear to send' not coming on or due to some other transmit failure such as loss of transmit clock. Definition of the simulated ICW bits: Bit 0 = Abort Detect 1 = Normal char SVC L2 2 = Over/Under run 3 = Modem Check 4 = Receive Line Signal Det 5 = Flag Detect					See Rtn heading for more registers and error statistic If you continue fro this error stop by selecting FUNCTION and press START the test restarts at the transmit or receive part of the test without hard-ware reset enable. This error may be easier to find and correct with rtn 15CE.
15F0	0X60	Receive error completion.	This error stop occurs if a modem check has been detected (simulated ICW bit 3 on) while in receive mode or this stop occurs if you selected the options to stop on any frame or any frame in error. Reg X'13' contains the simulated ICW bits accumulated during this receive operating by ORing ICW bits 0-7 together and saving them on each level 2 interrupt. Note that program does not stop on receive timeouts but setups to transmit again if a primary station or to receive again if a secondary station. Reg X'16'= address of receive data buffer in storage and reg X'19'=adr+1 of last received character. Note that regs defined in routine heading provide more information.					See Rtn heading for test details, registers and test statistics. Continueing from this stop by selecting FUNCTION 5, press START the test restarts from the xmit or rec portion of the test without doing the hardware reset and enables.
15F0	0X61	Receiving frames.	This stop code occurred because you selected an option to stop on the type of frame just received. Reg X'1E' defines type of frame received and is defined in the routine heading. Reg X'16= adr of start of receive data buffer. Reg X'19'=adr+1 of last character received (less block check chars). Reg X'14'=accumulated block check (CRC) characters accumulated by this program and should = X'F0B8' if no errors occurred. Reg X'13'=last two received characters (prior to flag char) and should be the					See Rtn heading for registers, test statistics. continue from this stop select FUNCTIO 5 and press START, the program restarts at the transmit/ receive portion of the test without doing hardware reset enable operations but clears the statistics

ROUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		actual received block check (CRC) characters.					counters.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
Type 1 Communications Scanner Common Subroutine and Interrupt Handler Error Codes								
15XX	1XXX	The following error codes are error stops caused by a failure detected in one of two common subroutines. These failures may therefore occur in any routine. The first subroutine, error codes 1X01 and 1X02, attempts to reset and enable the scanner by disabling the scanner via OUT X'45', waiting 30 microseconds for the scanner to disable, and then enabling the scanner only (not the LIBs) via OUT X'45'. The second subroutine, error codes 1X04 through 1X0A, sets diagnostic bit service and attempts to set each of the 64 line addresses to mode 010 (disable) as each line interrupts. Error codes (1X0C through 1X1A) are error stops issued by the 'dial-a-digit' subroutine. This subroutine is used by any routine that wishes to dial a digit on an autocall interface. The dial digit is passed to the subroutine which then handles the dial operation from the time PND comes up on the autocall interface until DPR is dropped by the subroutine after the digit has been sent. By reviewing the 'function tested' column of each of the error stops, the reader should be able to follow the flow of the dial operation.							
15XX	1X01	Ensure that following an OUT X'45' with byte 0, bit 2 on, the CS is reset.	After waiting 30 microseconds (one scanner pass), an IN X'44' indicated the scanner was not reset. Reg. X'15' contains the bits in IN X'44' in error:		FFFF			Pretest error. Rerun routine 1504. Since 'Scanner enabled' being off resets the others, if byte 0, bit 3 is on in error, ignore any others that are on. Reg. X'14' contains the result of the IN X'44'.
			Byte 0:					
			Bit 3-scanner enabled latch failed to reset.	Y4E2		RS105	A-310	
			Bit 4-character service pending latch failed to reset.	Y4E2		RS105	A-210 A-220	
			Byte 1:					
			Bits 2 thru 5-bit clock check for LIBs 1,2,3, or 4 (respectively) failed to reset.	Y4F2		RS206	A-210 A-220	
			Bit 6-LIB select check failed to reset.	Y4F2		RS206	A-210 A-220	
			Bit 7-outbus check failed to reset.	Y4E2		RS102	A-210 A-220	
15XX	1X02	Ensure that following an OUT X'45' with byte 0, bit 2 on, the CS can be enabled.	IN X'44' byte 0, bit 3 (scanner enabled latch) failed to set.	Y4E2	1000	RS105	A-210 A-220	Pretest error. Rerun routine 1506. Reg. X'14' contains the result of the IN X'44'.
15XX	1X04	Ensure that force bit service (OUT X'47') can cause a bit service interrupt from the first line (BCB address X'0800').	After attempting to force a bit service level 2 interrupt (via OUT X'47') from the first line address, unmasking level two interrupts and waiting the time of a scanner pass, no bit service interrupt occurred from that line.	Y4F2, Y4G2		RS305	A-330 A-040	Pretest error. Rerun routine 1512.
15XX	1X06	Ensure that with diagnostic bit service set, each time a pending bit service interrupt is reset and the scanner is started, another level two interrupt is immediately pending.	With diagnostic bit service having been set and the previous bit service request being reset, an IN X'77' immediately following the previous reset failed to indicate a pending level two interrupt. (Byte 0, bit 1 of the IN X'77' was off.)	Y4G2, Y4E2		RS305 RS105	A-040, A-300	Pretest error. Display reg. X'43'. If byte 0, bit 1 is on, a feedback error has occurred; rerun routines 1512 and 1514. If not, rerun routines 1572 and 1574. If needed, reg. X'15' contains the address that should have caused the next level two interrupt.
15XX	1X08	Ensure that the level two interrupt condition just caused was caused by the	After having found a pending level 2 interrupt condition as expected, an IN X'41'	Y4G2		RS301	A-140	Pretest error. Rerun routines 1572 and 1574.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
		the next sequential address.	indicated that it was not caused by the next sequential address.					If needed, reg. X'15' contains the line address that caused the interrupt as determined by the IN X'41'. Also, reg. X'16' contains the address that should have caused it.
15XX	1X0A	Ensure that mode 010 can be set via an OUT X'42' with mode bit 2 (byte 0, bit 7) on only.	After issuing the described OUT X'42', with the scanner stopped at the line address found in reg. X'15', an IN X'42' did not reflect the OUT X'42'.	Y4G2	FFFF	RS304	A-170	Pretest error. Rerun routines 1552 and 1516. If needed, reg. X'14' indicates the bits in error, and reg. X'16' indicates what the IN X'42' should have contained.
15XX	1X0C	While waiting for PND (present next digit) to come up from the autocall unit, ensure that a bit service interrupt occurs at least once every 30 milliseconds	A bit service interrupt from the tested address (found in reg X'11') failed to occur within 30 milliseconds of the previous one.	Y4G2		RS305	A-040	Pretest error. Probably an intermittent loss of strobe. Rerun routine 1580.
15XX	1X0E	While waiting for PND, keep checking for ACR (abondon call and retry).	While waiting for PND, an IN X'43' indicated that ACR had come up from the autocall unit. Reg X'13' contains the results of the IN X'43'. (ACR coming up may not in itself be the of the failure but just a symptom of it. In example, when dialing the first digit, ACR should come up if dial tone was not detected within the proper amount of time).					Pretest error. If needed, reg X'16' contains a storage location address. The byte at this address contains the digit count to identify which digit of the number is being dialed. The last four bits of the next byte at this address contain the digit itself. Reg X'11' contains the autocall line (BCB) address. It may be possible to scope this failure while stopped at this error stop.
15XX	1X10	Wait up to 60 seconds for PND to come up.	After waiting 60 seconds from the beginning of this subroutine, PND failed to come up from the autocall unit. nor had it brought up ACR to indicate an error condition. (At the start of this subroutine, if this is the first digit being dialed, CRQ has been set. If this is not the first digit, DPR has been dropped after sending the previous digit. In either case, PND should have come up within 60 seconds.) Reg X'13' contains the result of the last IN X'43'.					Pretest error. If needed, reg X'16' contains a storage location address. The byte at this address contains the digit count to identify which digit of the number is being dialed. The last four bits of the next byte at this address contain the digit itself. Reg X'11' contains the autocall line (BCB) address. It may be possible to scope this failure while stopped at

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								this error stop.
15XX	1X12	Present the digit to be dialed to the autocall unit.	After issuing an OUT X'43' while stopped at the autocall line address (found in reg. X'11'), and IN X'43' did not reflect the OUT X'43' as it should have. Reg. X'14' contains the results of the IN X'43' and reg. X'15' contains the bits in error:	Y4G2	1F08	RS308	A-190 A-200	Pretest error. Rerun and loop on the appropriate routines as given below. Failure is probably in the associated line interface.
			Byte 0:					
			Bit 3 - DPR failed to set					Rerun routine 155A
			Bit 4 - NB8 bit failed					Rerun routines 151A and 151C.
			Bit 5 - NB4 bit failed					Rerun routines 151E and 1520.
			Bit 6 - NB2 bit failed					Rerun routines 1526 and 1528.
			Bit 7 - NB1 bit failed					Rerun routines 1522 and 1524.
			Bit 1:					
			Bit 4 - CRQ dropped					Rerun routine 1556.
15XX	1X14	While waiting for PND to drop, ensure that a bit service interrupt occurs at least once every 30 milli-seconds.	A bit service interrupt from the tested address (found in reg X'11') failed to occur within 30 milli-seconds of the previous one.	Y4G2		RS305	A040	Pretest error. Probably an intermittent loss of strobe. Rerun routine 1580.
15XX	1X16	While waiting for PND to fall, keep check for ACR.	After having presented DPR and the digit to be dialed to the autocall unit and while waiting for PND to fall, the autocall unit brought up ACR. Reg X'13' contains the results of the IN X'43' that indicated ACR. (ACR itself may not be the actual cause of failure but just a symptom of it. In example, the autocall unit will bring up ACR if it doesn't recognize the presented digit as a valid digit.)					Pretest error. If needed, reg. X'16' contains a storage location address. The byte at this address contains the digit count to identify which digit of the number is being dialed. The last four bits of the next byte at this address contain the digit itself. Reg X'11' contains the autocall line (BCB) address. It may be possible to scope this failure while stopped at this error stop.
15XX	1X18	Wait up to 60 seconds for PND to fall after having presented DPR and the dial digit.	After waiting 60 seconds, PND never dropped to indicate that the dial digit had been dialed, nor had ACR ever come up to indicate a failure. Reg X'13' contains the results of the					Pretest error. If needed, reg. X'16' contains a storage location address. The byte at thi

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
			last executed IN X'43'.					address contains the digit count to identify which digit of the number is being dialed. The last four bits of the next byte at this address contains the digit itself. Reg X'11' contains the autocall line (BCB) address. It may be possible to scope this failure while stopped at this error stop.
15XX	1X1A	Reset DPR to complete the dialing of the current digit.	After having seen PND drop, an OUT X'43' was executed with just the CRQ bit on to reset the digit bits and DPR. An IN X'43' then indicated that either the bits did not reset or CRQ had. Reg X'14' contains the results of the IN X'43'. Reg X'15 contains the bits in error:	Y4G2	1F08	RS308	A-190 A-200	Pretest error. Rerun and loop on the appropriate routines as given below. Failure is probably in the associated line interface.
			Byte 0:					
			Bit 3 - DPR failed to reset.					Rerun routine 155C.
			Bit 4 - NB8 bit failed to reset.					Rerun routine 151C.
			Bit 5 - NB4 bit failed to reset.					Rerun routine 1520.
			Bit 6 - NB2 bit failed to reset.					Rerun routine 1528.
			Bit 7 - NB1 bit failed to reset.					Rerun routine 1524.
			Byte 1:					
			Bit 4 - CRQ dropped					Rerun routine 1556.
15XX	2XXX	The following error codes are error stops caused by a failure detected in either the first or second level interrupt handlers. When a level one or two interrupt occurs, certain checking is done by the appropriate interrupt handler to ensure the validity of the interrupt. Since the interrupt handlers are common to all routines, these errors may occur in all routines and in either pretest or test.						
15XX	2X10	Ensure that the level 1 interrupt which has just occurred is expected by the routine running. (i.e. adapter level 1 interrupts have been unmasked).	An unexpected level 1 interrupt has occurred. (i.e. A level 1 interrupt has occurred with level 1 interrupts masked off.)	B3M2		CP002	6-082	Rerun IFT 11XX (CCU IFT). Reg. X'05' contains additional information. If byte 1, bit 1 is off, neither IN X"76" nor IN X"7E" contained an interrupt request bit. If this bit is on, the type 1 CS requested the level 1.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
								Note: Regardless of the source of the interrupt, remember that adapter level 1 interrupts were masked off and the interrupt should not have occurred.
15XX	2X21	Ensure that all level 2 interrupts are caused by the CS. (The only other possible level 2 is "Diagnostic Level 2" in IN X'7F' which is not used by this IFT).	A level 2 interrupt has occurred and IN X'77' did not show it as being from the CS.	Y4F2		RS202	A-060 A-040	Rerun IFT 11XX (CCU IFT). If it is desired to locate the failure by scoping, try starting with "Bid Program Level 2" on ALD page RA012. This is the line that actually requests the level 2 interrupt.
15XX	2X23	Ensure that the level 2 interrupt which has just occurred is expected by the routine running. (i.e. level 2 interrupts have been unmasked).	A level 2 interrupt has occurred while level 2 interrupts were masked off.	B3M2		CP002	A-060 A-040	Rerun IFT 11XX (CCU IFT). Failure is associated with interrupt masking circuitry in the CCU.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS

Type 1 Communications Scanner Informational Displays

15XX E0X0 This code is displayed while any routine that takes longer than 20 seconds is running. It is used only to indicate that the routine is running and is not in a loop. (The 'X' is usually changed whenever the line address under test is changed.)

15XX E000 This code is displayed alternately with display 'E0FF' while any manual intervention routine that provides a continuous function (such as continuously transmitting) is looping. It is used to indicate that the routine is functioning and has not simply gone into an unexpected program loop. When it is desired to cause such a routine to stop looping and go through to its normal completion, the operator must do so by entering X'D0FF' through the use of the dynamic communication facility of the DCM. Enter X'D0FF' in data switches B-E, put the DISPLAY/FUNCTION SELECT switch in FUNCTION 1, and press the interrupt pushbutton. (See the DCM section of this manual for a more detailed description of how to use this function.) (For routine 15CE, please see note under manual intervention code 15XX, F06B for further details).

15XX E008 This code is continuously displayed while a routine is waiting for Clear to Send to come up from a modem. Some modems may take up to 30 seconds to bring up Clear to Send. During this time, the program is looping. After the 30 seconds has elapsed, if Clear to Send is still not up, an error will occur.

15XX E009 This code is continuously displayed while the routine running is waiting for a manual switched line connection to be made. Please place the manual call. The routine will remain in a loop until DSR comes up on the line being tested. (If this is routine 15CE, the line being monitored for DSR is the transmit line. Also, if this is routine 15CE and it is desired to end or restart the routine, follow the directions given in the note under manual intervention code 15XX, F06B.)

15XX E00A This code is continuously displayed by routine 15CA while it is waiting for a call to be made. The selected line has now been enabled and is ready to receive the incoming call. Please dial the telephone number of the selected line. When the routine sees Data Set Ready as a result of the incoming call, it will automatically continue. Please note that if this code remains displayed after the audible ringing is heard, the auto-answer circuitry failed to answer the incoming call or a problem exists either in the path or Data Set Ready through the auto-answer unit and into the CS or in the monitor for Data Set Ready circuitry in the CS. (At this point, the selected address is in monitor mode 01 and the routine is waiting for a level 2 interrupt. If no level 2 interrupt occurs, the routine will never be able to check for Data Set Ready.)

15XX E00B This code is continuously displayed by routine 15CA while it is waiting for RLSD as an indication that carrier is now present on the line being tested. The routine automatically continues as soon as carrier becomes present. If this code remains displayed for an appreciable time, suspect a failure in the carrier detect circuitry of the modem being tested or in path of RLSD from the modem to the scanner.

15XX E00C This code is continuously displayed by routine 15CE while it is waiting for the receive line to see a mark. (See the note preceding 15XX, 0X31 for information regarding why the receive line is looking for a mark.) If this display is active for any appreciable time, a problem probably exits somewhere in wrap data path.

15XX E03n This code is displayed by any routine that is dialing an autocall interface. It is displayed just prior to dialing each digit. 'n' is the digit to be dialed. In some cases, this display may be active up to one minute while the routine is waiting for PND from the autocall interface.

15XX E0FF This code is displayed alternately with display 'E000' while any manual intervention routine that provides a continuous function is looping. (See the description of "E000' for more detail.)

CHAPTER 6.0: TYPE 2 COMMUNICATIONS SCANNER NOTES

TYPE 2 COMMUNICATIONS SCANNER INTERNAL FUNCTIONAL TEST - NOTES

The following notes are referred to either the error code description or error code comments to provide register contents and other information for that error code.

Note 1. The expected character service level 2 interrupt either did not occur or the character service level 2 interrupt was from the wrong line address. The contents of the following registers indicate the type of error and the expected data.

Reg X'11' = line address the character service level 2 interrupt was expected from. This line address in in the format used to set ABAR.
Reg X'14' = either the line address obtained from ABAR of the line that caused the character service level 2 interrupt or if reg X'14'=0000 the expected character service level 2 interrupt did not occur.

Note 2. The expected transmit line character service level 2 interrupt either did not occur or the character service level 2 interrupt was from the wrong line address. The character service level 2 interrupt should be from the transmit line address. The following registers indicate the type of error and the expected data.

Reg X'11' = transmit line address the character service level 2 interrupt was expected from. This line address in in the format used to set ABAR.
Reg X'14' = either the line address obtained from ABAR of the line that caused the character service level 2 interrupt or if reg X'14'=0000 the expected character service level 2 interrupt did not occur.
Reg X'13' = receive line address. There should be no receive line character service level 2 interrupt at this time. Error could be caused by a feedback check setting LCD to F on the transmit line, by the transmit or receive line selecting the wrong oscillator, by a clock correction failure in the BCC card of the LIB, or by some other line set, LIB or scanner problem.

Note 3. The expected receive line character service level 2 interrupt either did not occur or the character service level 2 interrupt was from the wrong line address. The character service level 2 interrupt should be from the receive line address. The following registers indicate the type of error and the expected data.

Reg X'13' = receive line address the character service level 2 interrupt was expected from. This line address in in the format used to set ABAR.
Reg X'14' = either the line address obtained from ABAR of the line that caused the character service level 2 interrupt or if reg X'14'=0000 the expected character service level 2 interrupt did not occur.
Reg X'11' = transmit line address. There should be no transmit line character service level 2 interrupt at this time. Error could be caused by a feedback check setting LCD to F on the receive line, by the transmit or receive line selecting the wrong oscillator, by a clock correction failure in the BCC card of the LIB, or by some other line set, LIB or scanner problem.

Note 4. The Test Data latch and its function in the diagnostic wrap tests is a major tool in problem determination for the Type 2 Communication Scanner Internal Functional Tests. Most of the routines that transmit and/or receive data depend on the proper setting of the Test Data latch in the Communication Scanner. The Test Data latch is set to a mark condition when an ICW is scanned and that ICW is for a line address that is in diagnostic mode, has a bit-service pending, and any of the following conditions apply:

a. Transmit state and next bit to be transmitted is a 1.
b. A set mode (PCF=1) is being done.
c. Disable Communication Scanner (power on reset) is active.

In 'a' above the next bit to be transmitted may be from SDF bit 9, PDF bit 7, or a 1 bit forced by some other conditions, such as transmit initial.

The Test Data latch may be set to a space condition when an ICW is scanned and that ICW is for a line address that is in diagnostic mode, has a bit service pending, is in transmit state and the next bit to be transmitted is a 0. The 0 bit to be transmitted may be from SDF bit 9, PDF bit 7, or a forced start bit, zero bit insert or zero bit break signal.

Line addresses in receive mode strobe data into the receive data bit buffer from the Test Data latch if, when the ICW is scanned the line is in diagnostic mode, a bit service is pending and 'Data Terminal Ready' is not on.

During diagnostic mode transmissions, the transitions between mark and space in the Test Data latch should follow the bit service requests caused by the transmit clock (oscillator). The ICW for the diagnostic transmit line must be scanned before the Test Data latch can be set or reset so there may be a delay of up to one full scan period before the Test Data latch is set or reset after the bit service request is made. The period differences between the scan cycles and bit service requests usually results in an average delay of one-half of a scan period between the bit services and the setting or resetting of the Test Data latch. An unstable trace appears on the Test Data latch during diagnostic transmit operation caused by this delay. This unstable trace also occurs at the send data bit buffers during normal line transmissions and unstable trace does not occur on the actual transmit line because the bit to be transmitted is not set into the transmit trigger until the next bit service request time.

There is an average delay of one-half of a scan period between the time when the receive line bit service occurs and the receive data bit is gated into the SDF or PDF of the receive lines ICW.

The above two delays on the diagnostic transmit and receive operations normally account for less than one-half of a bit time. This delay usually will have no affect on a diagnostic wrap operation except that the receive clock correction circuits will be forced into action to correct for the jitter on the Test Data latch. With the higher speed oscillators, this delay along with receive clock correction may add up to more than half of a bit time. When this delay exceeds half of a bit time, the sequence of transmit and receive line character service level 2 interrupts may be affected. This sequence of interrupts is explained in more detail in notes 5 and 6.

Note 5: The routine did a diagnostic wrap data using start/stop LCD's. The receive line address is expected to cause its character service level 2 interrupt with a character being received before the character is completely transmitted on the transmit line address. This occurs only in diagnostic mode when the Test Data latch is in use (see note 4). During the manual intervention external data wrap test and during normal line operation, this does not occur because there is an extra bit time delay between the send data bit buffer and the transmit trigger. The receive interrupt occurs before the transmit interrupt because the receive line strobes the received data bit and requests its character service level 2 interrupt near the middle of the first or only stop bit at the end of the received data character. The transmit line does not request its character service level 2 interrupt until the end of the last or only stop bit at the end of the character being transmitted. This does not apply to the transmission of a pad character (all one bits with no start bit) since the receive line, in start/stop mode, should not cause a character service level 2 interrupt when receiving pad characters. If the line addresses are interrupting out of sequence and if neither line has had a feedback check (LCD=F) then there are many possibilities that can cause the error. Some of them are:

a. Oscillator select bits are not selecting the correct oscillator or blocking the other oscillators causing extra or missing strobes.
b. Start, stop or tag bit recognition is not working.
c. LCD is not being recognized as a start/stop type.
d. Receive clock correction is working incorrectly.

See note 7 for aids in isolating problems to the Communication Scanner, LIB or line sets. Another possible failure is that the oscillator is running way too fast or that a oscillator above 1200 is installed but is configured as a slower speed oscillator in the CDS. If the oscillator is way too fast (or too many strobes are occurring from some other source) the interrupts can occur out of sequence due to the Test Data latch delays explained in note 4. This condition can be tested by running routine 167A which is the oscillator speed test. If the CDS indicates that the first installed oscillator exceeds 1200 BPS then some portions of a few routines are bypassed due to the delay times explained in note. 4

Note 6. The routine did a diagnostic wrap data using synchronous LCD's. The receive line address is expected to cause its character service level 2 interrupt with the character being received before the character is actually fully transmitted. The receive line should not interrupt until it detects a received data bit pattern that is recognized as a synchronizing character for the particular line control (LCD) in use. Therefore, the transmit line address normally has several character service level 2 interrupts to transmit pad and synchronizing characters before the receive line has any. The routines shift the transmit lines data characters by one or more bit position to cause the receive line to recognize the synchronizing character bit pattern one or more bit times before the end of the transmitted character. This was done to ensure that the sequence of interrupts would be predictable so that the line sets could be tested for clock correction or selection errors. Without this transmit character shifting, out of sequence interrupts could occur on high speed oscillators due to the Test Data latch jitter explained in note 4 and the different type clock correction done in synchronous mode over start/stop mode. If the line addresses are interrupting out of sequence and if neither line has had a feedback check (LCD=F), then there are many possibilities that can cause the error. Some of them are:

a. Oscillator select bits are not selecting the correct oscillator or blocking the other oscillators causing extra or missing strobe pulses.
b. Tag bit recognition is not working.
c. LCD is not recognized as a synchronous LCD.
d. Receive clock correction is not working properly.

See note 7 for aids in isolating problems to the Communication Scanner, LIB or line sets. Another possibility is that the oscillator is running way too fast or some other failure is causing too many strobe pulses. In this case the interrupts could occur out of sequence due to the TEST DATA Latch jitter and delays explained in note 4.

Note 7. This note is referenced by those routines that run on more than one line address(not necessarily at the same time) and allow you to use the continue function.

This routine allows using the continue function after an error stop to help isolate a problem to the Communication Scanner, LIB or line sets. When an error stop occurs, record the line address and other information about that error and then select function 5 and press the push button to continue from that error stop. Other error stops for the same line address will probably occur but they should be ignored since they were probably caused by the previous error or by over/under run. When the routine is done testing one line address or a pair of line addresses it does a reset to the scanner and then starts the test on the next line or pair of line addresses. Because of this the first error stop for each line address should be recorded to develop a failure pattern to use to isolate the failure to one line address, a pair of line addresses, all the line addresses in a LIB or all line addresses in the scanner. If only one line address or a pair of even-odd line addresses fail then the problem is probably with the line set card for that position. If all line addresses fail the problem could be with LIB or Communication Scanner addressing failures or bad cable connections between the scanner and LIB. A bad bit clock control card in the LIB could also cause all line addresses in a LIB to cause failures that look like line set failures.

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CHAPTER 6.1: TYPE 2 COMMUNICATIONS SCANNER IFT SYMPTOM INDEX

X602 XXXX CDS (Configuration Data Set) checking routine. This routine checks that certain necessary control data within the CDS is valid. You should reference chapter 2.0 in this manual for a complete CDS definition. The CDS is loaded into storage starting at X'0F00' when the DCM (Diagnostic Control Module) is loaded. Within the CDS is a control block for the Type 2 communications scanner. This control block defines the scanner type, scanner RPQs, scanner features, oscillator types, LIB types and line set types. Some of this data is validated in this routine. If you get errors in this routine and the configuration data is correct then it could be that the version/level of the diagnostics that you are running does not support that feature. While this routine is running you may get some display B error codes starting with 1. These are pretest errors and these errors can not be bypassed except by aborting this routine. These pretest errors are defined in section T2CS-COM near the end of the type 2 scanner IFT symptom index. See section T2CS-COM for details on these pretest error codes if they occur. A summary of the error codes is listed here:

Display B.	Meaning.
1X01	Scanner is not configured as a type 2 scanner.
1X06	An invalid LIB type code found in CDS.
1X07	An invalid line set type code found in CDS.

X602	0X01	Configuration Data Set (CDS).	Scanner not configured as a a type 2 communications scanner. Reg X'16'=storage address of data block within the CDS for the adapter (scanner number) under test.					Reg X'11' =line address of scanner LIB line interface address.
X602	0X02	Configuration Data Set (CDS)	Oscillator 0 not installed according to CDS data. Reg X'16'=storage address of data block within the CDS for the adapter(scanner number) under test. Reg X'11'= line address as used to set ABAR.					This error will als occur if an invalid oscillator type cod was found in the CD for oscillator 0(1s oscillator position
X602	0X03	Configuration Data Set (CDS)	Oscillator 0 not lowest speed according to CDS data. Reg X'16'=storage address of data block within the CDS for the adapter (scanner number) under test. Reg X'11'= line address(as used to set ABAR).					This error will als occur if an invalid oscillator code is in the CDS for oscillators 1,2 or (2nd, 3rd or 4th oscillator positions).
X602	0X04	Configuration Data Set (CDS)	No LIBs configured according to CDS data. Reg X'16'= storage address of data block within the CDS for the adapter under test. Reg X'11' has line adr.					
X602	0X05	Configuration Data Set (CDS)	No line sets installed according to CDS data. Reg X'16'=storage address of data block within the CDS for the adapter(scanner number) under test.					Reg X'11' = line address of scanner-LIB-line interface address.
X603	0X01	Test all valid inputs and outputs for type 2 scanner.	Input or output caused I/O check. Display reg X'14' which has been loaded with the actual failing In/Out instruction. Reg X'16' contains storage adr of instruction loaded into reg X'14'. Reg. X'11'=line adr.	A3D2 B3E2		TA921 CK0Q1	B-120 B-210	
X603	0X02	Test all valid inputs and outputs for type 2 scanner.	Adapter level 1 interrupt occurred. Reg X'14' contains error bits stored in L1 routine from reg X'43'. Reg X'16' has adr of In/Out instr. Reg X'11' = line adr.	A3C2		TB131	9-500 8-460	Level 1 inputs are to A3C2 card.
X605	0X01	Attachment buffer adr reg. ABAR is reg X'40'	Unable to write or read valid adr to or from ABAR. Display reg X'14' for failing adr input from ABAR. Reg X'11' is adr that was output to ABAR.	B3E2 B3D2		CX001 CX009	B-030	All valid addresse are written to and read from the ABAR with output and input X'40'.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X607	0X01	'CSB disable' on - turned on by Output X'43' with byte 0 bit 0 and byte 1 bit 6 on. Should clear PCF and display request bits in ICW.	'CSB disable' failed to force Primary Control Field (PCF) to zero. Reg X'11'= failing line adr.	A3F2 A3D2	TA811 TA921	B-170 B-120	Check that 'CSB disable' holds the PCF to zero and resets ICW bit 38, Reg X'47' byte 0 bit 6. Also checks that Output X'43' with byte 0 bit 1 and byte 1 bit 5 clears reg X'43'.
X607	0X02	'CSB disable' on - turned on by Output X'43' with byte 0 bit 0 and byte 1 bit 6 on. Should clear PCF and display request bits in ICW.	'CSB disable' failed to force PCF to zero when output X'45' is done to set PCF=7.	A3F2	TA811	B-190	reg X'11'=line addr set in ABAR.
X607	0X03	'CSB disable' on - turned on by Output X'43' with byte 0 bit 0 and byte 1 bit 6 on. Should clear PCF and display request bits in ICW.	Error reg bits remain on in reg X'43'. Display reg X'15' for error bits.	A3C2	TB131	B-130	Reg X'11'=line addr set in ABAR.
X607	0X04	'CSB disable' on - turned on by Output X'43' with byte 0 bit 0 and byte 1 bit 6 on. Should clear PCF and display request bits in ICW.	'CSB disable' did not reset display request ICW bit 38. Reg X'11'=line adr.	A3G2	TB061	B-140	ICW Bit 38 (display bit) is input reg X'47' byte 0 bit 6.
X60A	XXXX	ICW address test. This test checks for interaction between ICWs by storing a different pattern in the SDF of each ICW that is used and then to check each ICW that it contains the correct pattern in its SDF. The pattern used in the SDF of each ICW is byte 0 bits 6-7 and byte 1 bits 0-7 of the line address (as used to set ABAR) of that ICW. If the SDF portion of the ICW local storage is bad you should use routine X61D to help locate the problem.					
X60A	0X01	Check that all ICWs (interface control words) can be addressed by the program.	Incorrect bits in serial data field. Reg X'16' contains expected SDF. Reg X'14' byte 0, bits 6-7 = actual SDF Bits 0 & 1 (ICW bits 24 & 25); byte 1 bits 0-7 = actual SDF bits 2-9 (ICW bits 26-33). Reg X'11'=line adr with invalid SDF.	A3L2 A3J2 A3H2	TA621 TA545 TA221	B-190	Each ICW is address and a different bit pattern is stored i the SDF bits of eac ICW. Then each ICW addressed and the S is input and checke that the correct bi are on for that ICW Note: the program does Output X'46' to setup the SDF's of all ICW's then the routine sets 'scope sync 2' before checking each ICW with Input X'45' and X'47'.
X60C	0X01	'CSB disable' off (scanner enabled)	Primary Control Field (PCF) did not remain at zero. Reg X'11' contains line adr which should be in ABAR. ABAR is reg x'40'.	A3F2	TA811	B-170	'CSB disable' latch is turned off and the PCF is checked to see if it is zer
X60C	0X02	'CSB disable' off (scanner enabled)	PCF did not set or remain at state 7 with scanner enabled. Reg X'45' has PCF, reg X'11' has line adr.	A3F2	TA811	B-190	The 'CSB disable' b being off allows the PCF to be chang to 7. The display b (ICW bit 38) should still be off.
X60C	0X03	'CSB disable' off (scanner enable)	Bits are on in the error reg after 'CSB disable' turn off. See reg X'43'. Reg X'11' has line adr.	A3C2	TB131	B-130	No error bits are caused or expected.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X60C	0X04	'CSB disable' off (scanner enabled)	Display bit on after 'CSB disable' off. Reg X'47' byte 0, bit 6 should not be on. Reg X'11'=line adr.	A3G2	TB061	B-140	
X610	0X01	Unexpected level 1 interrupts--test 1	Unexpected level 1 interrupt occurred. Reg X'16' = scanner check register (saved from reg X'43' in the L1 interrupt handler). Reg X'14' contains adr input from ABAR when the L1 occurred. Reg X'11'=line adr. Reg X'43' should be all zeros at this time unless another L1 error condition has occurred.	A3C2	TB131	B-130	Scanner is reset via an output to se 'CSB Disable Latch'. The pgm waits for any unexpected level 1 interrupts.
X611	0X01	Unexpected level 1 interrupts--test 2	Unexpected level 1 interrupt occurred. Reg X'16'=scanner check reg X'43' (saved by the L1 interrupt handler). Reg X'14'=line adr obtained from ABAR when the L1 occurred. Note: reg X'43' should be all zeros at this time unless another L1 error condition has occurred.	A3C2	TB131	B-130	Reset scanners via setting 'CSB DISABL latch on. Enable scanner by turning the latch off. Pgm waits for unexpected L1 or L2 interrupts.
X613	0X01	Unexpected level 2 interrupts--test 1	Unexpected level 1 interrupt. Reg X'16' is saved scanner check reg X'43' (saved by the L1 interrupt handler). Reg X'14'= adr obtained from ABAR when the L1 occurred. Note: reg X'43' should be all zeros at this time unless another error occurred.	A3C2	TB131	B-130	When 'CSB disable' is on, program chec for unexpected leve 1 and level 2 interrupts.
X613	0X02	Unexpected level 2 interrupts--test 1	Unexpected level 1 and level 2 interrupt. Regs same as error 0X01.	A3C2 A3L2	TB131 TA611	B-130	See 0X01 comments.
X613	0X03	Unexpected level 2 interrupts--test 1	Unexpected level 2 interrupt. Reg X'14' contains adr obtained from ABAR by an Input X'40' when the L2 occurred.	A3L2	TA611	B-300	See 0X01 comments.
X614	0X01	Unexpected level 2 interrupts--test 2	Unexpected level 1 interrupt. Reg X'16'= scanner check reg (saved from reg X'43' in the L1 interrupt handler). Reg X'14'=ABAR (obtained by Input X'40' when the L1 occurred). Reg X'43' was reset when the L1 occurred and should now be all zeros unless another L1 error is pending.	A3C2	TB131	B-130	After 'CSB disable' is reset, the progr checks for unexpect level 1 and level 2 interrupts. No action is initiated in the scanner after it is enabled, and no L1 or L2 interrupts should occur.
X614	0X02	Unexpected level 2 interrupts--test 2	Unexpected level 1 and level 2 interrupt. Regs same as error 0X01.	A3C2 A3L2	TA131 TA611	B-130	See 0X01 comments.
X614	0X03	Unexpected level 2 interrupts--test 2	Unexpected level 2 interrupt. Reg X'14'=ABAR when unexpected L2 occurred.	A3L2	TA611	B-300	See 0X01 comments.
X616	0X01	Disable line intf base (LIB)	Primary control field (PCF) not set to zero on disable. Reg X'11'=line adr.	A3F2	TA811	B-170	each LIB is disabled and checked to see that PCF is forced to remain at 0. The LIB is disabled if its

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							mask bit is set on by an Output X'43'. Note: only LIBs indicated as being installed by the CDS are tested.
X616	0X02	Disable line interface base (LIB)	Disable LIB did not force PCF to zero. Reg X'11'= line adr. An Output X'45' was done to set PCF to 7. The PCF should have been forced to 0 since the LIB is disabled.	A3P2	TA811	B-170	See 0X01 comments.
X617	0X01	Enable line interface base (LIB)	Primary control field (PCF) not zero after the LIB is enabled. Reg X'11'=line address.	A3P2	TA811	B-170	The program disable each LIB.
X617	0X02	Enable line interface base (LIB)	Could'nt set PCF after enabling LIB. Reg X'11'=line adr. Output X'45' was done to set LCD=0, and PCF=7. PCF should remain at 7.	A3P2	TA811	B-170	See 0X01 comments.
X61B	0X01	Interface control word bits 6 thru 15 test. Reg X'44'	ICW bits 6-15 did not set to X'2AA'. Reg X'11'=line adr.	A3P2 A3M2	TA131 TA741	B-180	Program set ICW bit 6-15 to X'000', set scope sync 2, set I bits 6-15 to X'2AA' and checks that they are = to X'2AA'.
X61B	0X02	Interface control word bits 6 - 15 test. Reg X'44'	ICW bits 6-15 not set to X'155'. Reg X'11' = line adr.	A3P2 A3M2	TA131 TA741	B-180	Program set ICW bit 6-15 to X'000', scope sync 2, ICW bits 6-15 to X'155' and then inputs and checks that they are = to X'155'.
X61B	0X03	Interface control word bits 6 thru 15 test. Reg X'44'	ICW bits 6-15 did not set to X'3FF'. Reg X'11' = line adr.	A3P2 A3M2	TA131 TA741	B-180	Program sets ICW bi 6-15 to X'000', set scope sync 2, set I bits 6-15 to X'3FF' and checks that they=X'3FF'.
X61B	0X04	Interface control word bits 6 thru 15 test. Reg X'44'	ICW bits 6-15 did not set to X'000'. Reg X'11'=line adr.	A3P2 A3M2	TA131 TA741	B-180	Program sets ICW bi 6-15 to X'3FF', scope sync 2, ICW bits 6-15 X'000' and then inputs and checks that they =X'000'.
X61C	0X01	Interface control word bits 16 thru 19 (LCD check).	ICW bits 16-19 did not set to X'A'. Reg X'11'=line adr.	A3P2	TA111	B-190	Bit patterns X'A,5,F & 0' are set in and read from ICW bits 16-19(LCD) in this test. ICW bits 20-23 (PCF) are not tested and are always set to zeros in this test to prevent any scanner hardware

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							action that may occur if these bits are not zero. For this error stop (0X01) the program sets LCD to 0, sets scope sync 2, sets LCD to A and then inputs and checks that LCD=A.
X61C	0X02	Interface control word bits 16 thru 19 (LCD check)	ICW bits 16-19 did not set to X'5'. Reg X'11'=line adr.	A3P2	TA111	B-190	Program set LCD = 0, scope sync 2, LCD t 5 and inputs to check that LCD=5.
X61C	0X03	Interface control word bits 16 thru 19 (LCD check)	ICW bits 16-19 did not set to X'F'. Reg X'11'=line adr.	A3P2	TA111	B-190	Pgm sets LCD = 0, scope sync 2, LCD = F, inputs and checks that LCD=F.
X61C	0X04	Interface control word bits 16 thru 19 (LCD check)	ICW bits 16-19 did not set to X'0'. Reg X'11'=line adr.	A3P2	TA111	B-190	Pgm sets LCD to F, scope sync 2, LCD to 0 and checks that LCD is is still 0.
X61D	0X01	Interface control word bits 24-33; Out=reg X'46'; in=reg. X'45' & X'47' (serial data field).	ICW bits 24-33 did not set to X'2AA'. Reg X'11'=line adr.	A3H2	TA221	B-200	Pgm sets SDF to X'000', scope sync 2, SDF to X'2AA' and checks that SDF is = X'2AA'.
X61D	0X02	Interface control word bits 24-33; Out=reg X'46'; In=reg X'45' & X'47' (serial data field).	ICW bits 24-33 did not set to X'155'. Reg X'11'=line adr.	A3H2	TA221	B-220	Pgm sets SDF to X'000', scope sync 2, SDF to X'155' and inputs and checks that SDF is = to X'155'.
X61D	0X03	Interface control word bits 24-33; Out=reg X'46'; In=reg X'45' & X'47' (serial data field).	ICW bits 24-33 did not set to X'3FF'. Reg X'11'=line adr.	A3H2	TA221	B-200	Pgm sets SDF to X'000', scope sync 2, SDF to X'3FF' and inputs and checks that SDF is = to X'3FF'.
X61D	0X04	Interface control word bits 24-33; Out=reg X'46'; In=reg X'45' & X'47' (serial data field).	ICW bits 24-33 did not set to X'000'. Reg X'11'=line adr.	A3H2	TA221	B-200	Pgm sets SDF to X'3FF', scope sync 2, SDF to X'000' and then inputs and checks that SDF is = to X'000'.
X61E	0X01	Display request bit (ICW bit 38); Out reg X'43'; In reg X'47'.	ICW bit 38 did not turn on. Reg X'11'=line adr.	A3G2	TB061	B-170 B-140	Set ICW bit 38 on and reset via an output X'43'. Bit is tested via an input from reg X'47'.
X61E	0X02	Display request bit (ICW bit 38); Out reg X'43'; In reg X'47'	ICW bit 38 did not reset. Reg X'11'=line adr.	A3G2	TB061	B-170	See 0X01 comments.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X61F	0X01	'CSB disable' resets display request bit (ICW bit 38)	ICW bit 38 could not turn on when scanner and LIB are enabled. Reg X'11'= line address under test.	A3G2	TB061	B-170	Pgm attempts to set ICW bit 38 and 'CSB disable' to turn it off. Bit is set via output reg X'43' and tested via input reg X'47'
X61F	0X02	'CSB disable' resets display request bit (ICW bit 38)	'CSB disable' did not reset ICW bit 38. Reg X'11'=line adr.	A3G2	TB061	B-170	
X625	0X01	Primary control field (PCF) (No-op test) reg X'45'	PCF did not set to X'0'. Reg X'11'=line address. Reg X'40' should be same as X'11'.	A3F2	TA811		The Pgm set the PCF = 0 and expects no scanner action and no interrupts during a 25ms period for each line adr. The scanner and LIBs are enabled during this test.
X625	0X02	Primary control field (No-op test) reg X'45'	PCF did not remain at X'0' during a 25ms wait.	A3F2	TA811		See 0X01 comments.
X625	0X03	Primary control field (NOP test) reg X'45'	Level 2 interrupt occurred with line set to NOP. Reg X'14'=ABAR (obtained by Input X'40' when the unexpected L2 occurred). Reg X'40' should = reg X'14'. Reg X'11' is last line adr set in ABAR (Output X'40') just prior to Output X'45' to set LCD and PCF=0. No L2 interrupts are expected in this routine.	A3L2	TA611	B-310	See 0X01 comments.
X626	0X01	Upper scan limit X'00'. Reg X'41'	Did not get level 2 interrupt from line when ICW 41 was set on. Reg X'11' = line adr. Reg X'40' should = reg X'11'.	A3L2	TA621	B-300	Set ICW bit 41 on.
X626	0X02	Upper scan limit X'00'. Reg X'41'	Level 2 from wrong line adr. Reg X'11'=expected line adr. Reg X'14'=line address that caused the level 2.	A3L2	TA611	B-300	Adr in each scanner is checked.
X627	XXXX	Set Mode and scanner test. This is the first routine in the type 2 scanner internal functional tests that requires that the line sets and some LIB circuits to be operational. There are many possibilities for errors being detected in this routine but the most likely source of problems is in the line sets receive strobe circuits or in the bit clock control card circuits in the LIB. See note 7 in section T2CS-NOTES for some aid in determining if failures are in only one line set, in the LIB or in the scanner.					
X627	0X01	Set mode and scanner test	Level 2 interrupt did not occur for set mode. Display Reg X'45'. If byte 0 bits 0-3 (LCD) are all on, a feedback check occurred. Check oscillator 0 in the scanner. Check for bit service or a missing line set card for the failing addr. The most likely source of failure is in the line set card(s) for the failing line address. Reg X'11'=line adr under test. Reg X'40' should=reg X'11'. If no feedback check (LCD=F) occurred, the LCD should be 7 if the line runs in start/stop mode; the LCD should be 'C' if the line runs in BSC	A3E2	TA331	B-310	All S/S and B-260 BSC line sets (some RPQ line set are tested via a se mode operation. Thi checks some of the scanner, osc, LIB, line set circuits. A likely source of error is the lin set card in the failing line addr. Display bit is set while line addr is under test so that the display Reg (reg X'46') is valid for line adr under

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			mode. If PCF = 1 the set mode never completed for start/stop or BSC lines. If PCF=0 the set mode completed normally but the level 2 interrupt expected did not occur within 25 mili-seconds after it was issued. Register X'77' byte 0 bit 1 will be on if a L2 pending occurred after the 25 milli-sec. The SDF contains the bits used for set-mode. The card called is only a starting point to look for bit service.				test. The PCF is checked for 0 after a set mode. A set mode may cause a level 2 interrupt even if the oscillator is not working properly. See note in T2CS-NOTES for aid in isolatin the problem.
X627	0X02	Set mode and scanner test	Level 2 interrupt from wrong address. Check the line that caused the interrupt for faults. Reg X'11'=line address under test. Reg X'40' should=reg X'11'. Reg X'14' has line adr obtained from ABAR by Input X'40' when the L2 occurred.	A3L2	TA621	B-310 B-260	See error 0X01 for details.
X627	0X03	Set mode and scanner test	PCF field did not set to zero on set mode. Regs X'11' and X'14' setup same as errors 0X01 and 0X02.	A3F2	TA811	B-310 B-260	See error 0X01 for details.

X628 XXXX Feedback check test. All installed line sets are tested to insure that a feedback check will occur if an invalid bit is used during set mode and that a feedback check does not occur if a valid bit is used during a set mode. This routine will most likely produce error stops if the CDS (configuration data set) defining the LIB and line set types is not set up properly for the hardware that is installed. If the CDS is correct then the most likely source of the error is in the line set card(s) for the failing line address. See note 7 in section T2CS-NOTES for an aid to problem determination.

Each installed line set is tested in the following steps:

a. Reset then enable the scanner.
b. Set the display bit on in the line address under test.
c. Set the SDF via an output X'46' with the bits in reg X'13'.
d. Set scope sync 2.
e. Set LCD=0 and PCF=1 to initiate the set mode operation.
f. Unmask level 2 interrupts and wait until either a level 2 occurs or 25 mili-seconds have elapsed.
g. Verify that the LCD was set to F by the scanner if a feedback check should have occurred due to an invalid bit being used in the SDF during the set mode or verify that LCD was not set to F if a valid bit was used during the set mode.
h. Repeat steps a through g until all set mode bit positions have been tested.

On all error stops in this routine the following registers are setup:

Reg X'11'= line address of line under test(as used to set ABAR).
Reg X'13'= bit pattern being output to the SDF for this step of the test. The bit position that is a 1 is the bit being tested. Each bit of byte 1 is defined in more detail as:

Bit	ICW bit	SDF bit	Normal use if this bit is a 1 during set mode.
0	26	2	Not used.
1	27	3	Set diagnostic wrap mode.
2	28	4	Set Data Terminal Ready.
3	29	5	Set sync bit clock(synchronous clock correction).
4	30	6	Set external clock selected.
5	31	7	Set Data Rate Select(select high rate).
6	32	8	Set oscillator select bit 1.
7	33	9	Set oscillator select bit 2.

X628	0X01	Check that an invalid bit in the SDF during a set mode operation causes a feedback check.	Error if a feedback check did not occur setting the LCD to F. See reg X'13' bit definitions in the	A3E2	TA341	B-260	A feedback check should have occurre since CDS indicates a line set is

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			routine heading for more information.				installed without a latch for the bit position under test in the SDF.
X628	0X02	Check that a valid bit in the SDF during a set mode operation does not cause a feedback check.	Error if a feedback check occurred setting LCD to F. See reg X'13' bit definitions in routine heading for failing bit.	A3E2	TA341	B-260	A feedback check should not occur CDS indicates a line set is installed with a latch that could be set on for this SDF bit position during a set mode operation.
X629	XXXX	Diagnostic mode test. Each installed start/stop or synchronous line adr is set into diagnostic mode with a set mode operation. Then a check is made that Clear to Send, Data Set Ready and Diagnostic Mode bits are on. Auto call line sets are not checked. Each adr is tested in the following sequence: (1). Reset and then enable the CS. (2). Set display bit (ICW bit 38). (3). Set SDF bit on for Diagnostic mode and set bit on for Syn Bit Clock if line will run in synchronous mode only. (4). Set scope sync 2. (5). Set PCF=1 and LCD =7 for start stop lines or LCD =C for synchronous lines. (6). Wait for level 2 interrupt from the set mode and check the results. The most likely source of hardware failures detected in this routine are the line set card(s) for the line address under test. Reference note 7 in section T2CS-NOTES for aid in determining a failing pattern.					
X629	0X01	Diagnostic mode	Level 2 interrupt did not occur. See routine X627 error 0X01 for regs. Card called is only a starting point to look for bit service.	A3E2	TA331	B-310 B-260	See routine heading for more info.
X629	0X02	Diagnostic mode	Level 2 interrupt from wrong line address. Check the line address for faults.	A3L2	TA621	B-310 B-260	See routine X627 0X02 for regs. See rtn heading for more info.
X629	0X03	Diagnostic mode	PCF did not change to zero on set mode completion. See routine X627 error 0X03 for registers.	A3F2	TA811	B-310 B-260	See rtn heading for more informatio
X629	0X04	Diagnostic mode	Proper latches did not set. Display reg X'46' byte 0, bits 0,2 and 5 should be on. Reg X'14' contains input from reg X'46' at the time failure was detected. Reg X'15' has a bit on for each bit position in reg X'14' which is in error. Reg X'11'=line address under test.	A3E2	TA331	B-150	Reg X'46' bit 3 (RLSD) is ignored in this test; it may be on or off. Errors may be detected if an incoming call on a switched line brings up 'ring indicator' (Reg X'46' bit 0.1).
X62D	0X01	Service request (ICW bit 1) and level 2 interrupt	Level 2 interrupt did not occur for set mode. See routine 0X27 error 0X01 for regs and checks.	A3E2	TA331	B-130 B-260	Each installed S/S or BSC line set into diagnostic receive mode and SDF bit 9 set on. A L2 interrupt should occur and svc req bit (ICW bit 1) should turn on. The reset of the svc req bit is then checked.
X62D	0X02	Service request (ICW bit 1) and level 2 interrupt.	Level 2 interrupt was from the wrong line address. Check the line address that causes the interrupt for faults.	A3L2	TA621	B-300	See comments in err code 0X01.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)		FEALD PAGE	FETMM PAGE	COMMENTS
			Reg X'11'=line address under test. Reg X'40' should = reg X'11'. Reg X'14' has line adr obtained from ABAR by Input X'40' when the L2 occurred.					
X62D	0X03	SDF bit 9 was turned on and should cause a character service level 2 interrupt.	Level 2 interrupt did not occur. Check osc or scanner or missing line set card for that line. Reg X'11' = line adr of line under test. Reg X'40' should = reg X'11'.	A3E2		TA331	B-310 B-260	See comments in err code 0X01.
X62D	0X04	SDF bit 9 was turned on and should cause a character service level 2 interrupt.	L2 interrupt occurred from wrong line address. Reg X'14' =line address that caused the level 2. Reg X'11'=line address L2 was expected from.	A3E2		TA331	B-490 B-420	See comments in err code 0X01.
X62D	0X05	SDF bit 9 was turned on and should cause a char-service level 2 interrupt with ICW bit 1 on.	ICW bit 1(svc-request) is not on or ICW bits 0,2,3,5,6 or 7 are on. Reg X'44' byte 0= ICW bits 0-7 in bits 0-7.	A3P2		TA121	B-140	ICW bit 4 is ignore in this test since may be on or off.
X62D	0X06	SDF bit 9 was turned on and should cause a character service L2 interrupt	Service request did not reset (ICW bit 1). Reg X'44' byte 0, bit 1.	A3P2		TA121	B-180	
X62E	0X01	Priority bits 1 & 2 Reg X'47'	Priority bit 2 failed to set. Reg X'11'=line address of line under test. Reg X'40' should = reg X'11'.	A3G2		TB021	B-210	All combinations of the priority bits a checked that they c be set and reset.
X62E	0X02	Priority bits 1 & 2 Reg X'47'	Priority bit 1 failed to set. Reg X'11' =line address under test. Reg X'40' should = reg X'11'.	A3G2		TB021	B-210	
X62E	0X03	Priority bits 1 & 2 Reg X'47'	Priority bit 1 and 2 failed to set. Reg X'11' = line address under test.	A3G2		TB021	B-210	
X62E	0X04	Priority bits 1 & 2 Reg X'47'	Priority bit 1 and 2 failed to turn off. Reg X'11' = line address under test.	A3G2		TB021	B-210	
X632	0X01	Interrupt request pending bit (ICW 41). Reg X'47'	L2 interrupt request pending bit did not set in ICW 41, or reg X'47'. Check that 1st set mode caused the priority reg to be occupied. Reg X'13'=line address that should be in priority reg 3. Reg X'16'=line address that should have interrupt request pending bit on. Reg X'40' should = reg X'16'.	A3L2	0040	TA641	B-300	L2 interrupts are masked off and a se mode puts a line addr (ICW) in diag mode with priority select set to 3. A 2nd line addr is put into diag mode; priority select set to 3 by another. set mode operation. Then the on state of the interrupt pending bit is tested in the 2nd line. Level 2 interrupts are unmasked and checked that they occur in correct order
X632	0X02	Interrupt request pending bit (ICW 41). Reg X'47'	No level 2 interrupt. Should have had a L2 from line adr in reg X'13'. Reg X'16' = line adr of the next expected L2 interrupt.	A3L2		TA611	B-300	See in error code 0X01.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X632	0X03	Interrupt request pending bit (ICW 41). Reg X'47'	1st level 2 interrupt occurred but not from the expected line. Reg X'13' = line adr expected to interrupt first. Reg X'14' = line adr that caused the L2 interrupt. Reg X'16' = line adr expected to interrupt next.	A3L2	TA611	B-300	See in error 0X01.
X632	0X04	Interrupt request pending bit (ICW 41). Reg X'47'	No level 2 interrupt from 2nd line that had interrupt pending bit on. Reg X'13' = line adr of line that should have interrupted previously. Reg X'16' = line address expected to cause the L2 interrupt.	A3L2	TA611	B-300	Check scanner, oscillator, and LIB clock if no L2 interrupt occurred. See comments in error code 0X01.
X632	0X05	Interrupt request pending bit (ICW 41). Reg X'47'	2nd Level 2 interrupt occurred but from wrong adr. Reg X'13' =line adr of previous line that should have interrupted on previous error check. Reg X'14' = line adr of line causing L2 interrupt. Reg X'16' = line adr expected to cause L2 interrupt.	A3L2	TA611	B-300	See error code 0X01.
X634	0X01	Upper scan limit X'01' test (8 lines).	Did not get level 2 interrupt from one of the 1st 8 lines when ICW bit 41 was set on. Reg X'11' = line adr L2 expected to L2 interrupt Reg X'40' should = reg X'11'.	A3L2	TA621	B-220	Only 8 lines should interrupt when ICW bit 41 is set on; upper sc limits are setup to scan 8 line addrs.
X634	0X02	Upper scan limit X'01' test (8 lines).	Level 2 from wrong adr. Reg X'11' = line adr expected to L2 interrupt. Reg X'14' = line adr causing the L2 interrupt.	A3L2	TA621	B-300	
X634	0X03	Upper scan limit X'01' test (8 lines).	Got an unexpected L2 interrupt when ICW bit 41 was set in one of the ICWs beyond the 1st 8 lines. This interrupting ICW should not have been scanned to cause a L2 interrupt even though its L2 interrupt pending bit was set. Reg X'11' = line adr in which the ICW bit 41 was set. Reg X'14' is the line adr causing the L2 interrupt. If reg X'11'= reg X'14', the upper scan limit 01 is not working properly.	A3L2	TA621	B-220	If reg X'11' is not = to reg X'14', the unexpected L2 may be caused by a scan problem not related to the uppe scan limit controls
X635	0X01	Upper scan limit X'11' test (16 lines).	Did not get level 2 interrupt from one of the 1st 16 lines when ICW bit 41 was set on. Reg X'11' = line adr expecting a L2 interrupt.	A3L2	TA621	B-220	Only 16 line addrs should interrupt when ICW bit 41 set on with scan limit set for 16 lines.
X635	0X02	Upper scan limit X'11' test (16 lines).	Level 2 interrupt from wrong adr. Reg X'11' = expected adr; reg X'14' = line adr causing the L2 interrupt.	A3L2	TA611	B-300	
X635	0X03	Upper scan limit X'11' test (16 lines).	Got an unexpected level 2 interrupt when ICW bit 41 was set in one of the ICW's beyond the 1st 16. This line adr should not be scanned with scan limit bits = 11 so a L2 should not occur. Reg X'11' = line adr of ICW in which bit 41 was set. Reg X'14' = line adr causing the L2. If reg X'11' = reg X'14', the upper	A3L2	TA621	B-220	If reg X'11' is not equal to Reg X'14', the unexpected L2 interrupt may be caused by a scanner problem not related to the upper scan limit controls.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			scan limit 01 is not working properly.				
X636	0X01	Upper scan limit X'10' test (48 lines).	Did not get L2 from one of the 1st 48 lines when ICW bit 41 was set. Reg X'11' = line adr expected to L2 interrupt.	A3L2	TA621	B-220	Only 48 line addrs should interrupt when ICW bit 41 is set on when upper scan limit is set for 48 lines.
X636	0X02	Upper scan limit X'10' test (48 lines).	Level 2 from wrong adr. Reg X'11' = line adr expected to L2 interrupt. Reg X'14' = line adr on which the L2 interrupt occurred.	A3L2	TA611	B-300	
X636	0X03	Upper scan limit X'10' test (48 lines).	Unexpected L2 interrupt when ICW bit 41 was set in one of the ICW's beyond the 1st 48 line adrs. With scan limit 10 set, this line should not be scanned so no L2 should occur. Reg X'11' = line adr of ICW in which ICW bit 41 was set on. Reg X'14'=line address that caused the L2. If reg X'11' = reg X'14' then upper scan limit 01 is not working properly.	A3L2	TA621	B-220	If reg X'11' is not equal to Reg X'14', the unexpected L2 interrupt may be caused by a scanner problem not to the scan limit controls.
X63B	0X01	Interrupt priority register.	Level 2 interrupts did not occur after unmasking level 2. Reg X'13' = line adr L2 expected from.	A3L2	TA611	B-300	The 1st 4 ICW's are setup with priority settings of 3,2,1, and 0 in that order. ICW bit 41 (interrupt request pending) is set in the 1st four ICWs. Level 2 is unmasked and the ICWs are checked to ensure they interrupt in proper order (1st, 2nd, 3rd, & 4th ICW).
X63B	0X02	Interrupt priority register.	Level 2 interrupt is not from the expected address. Reg X'13' = line adr L2 expected from. Reg X'14' = line adr that caused L2.	A3L2	TA611	B-300	
X63D	0X01	Substitution control reg bit 1	Unexpected level 2 interrupt occurred. Reg X'14'=line adr of line causing the level 2 interrupt. Reg X'11' = line address that had ICW bit 41 (L2 pending) set. If reg X'11' does not equal reg X'14', there may be a LIB or scanner failure. If reg X'14' = reg X'11', subst ctrl reg bit 1 is not working and reg X'14' is the line address that should not have been scanned and therefore should not have caused a L2 interrupt.	B3E2 B3D2	CX001 CX009	B-220	Subst ctrl reg bit 1 is set on and an attempt is made to cause a L2 interrupt on lines E & F of all LIBs. These addresses should not be scanned.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X63E	0X01	Substitution control reg bit 2	Unexpected level 2 interrupt. Reg X'14' = line address of line causing the level 2. Reg X'11' = line adr of line that had ICW bit 41 (L2 pending) set. If reg X'11' does not equal reg X'14' there may not be a LIB or scanner failure. If reg X'14' = reg X'11', subst ctrl reg bit 2 is not working, and reg X'14' is the line adr that should not have been scanned and therefore should not have caused a level 2.	B3E2 B3D2	CX001 CX009	B-220	Subst ctrl reg bit 2 is set and an attempt is made to cause a L2 interrupt on lines C & D of all LIBs. These addresses should not be scanned.
X63F	0X01	Substitution control reg. bit 3	Unexpected level 2 interrupt. Reg X'14' =line adr causing the L2 interrupt. Reg X'11'= line addr that had ICW bit 41 (L2 pending) set on. If reg X'11' does not = reg X'14' then there may be a LIB or scanner failure. If reg X'14' =reg X'11' then the substit-ution control reg bit 3 is not working properly and reg X'11'= the line address that should not have been scanner and should not have caused a L2.	B3E2 B3D2	CX001 CX009	B-220	Subst ctrl reg bit 3 is set and an attempt is made to cause a L2 interrupt on lines A & B of all LIBs. These address should not be scann with the scan substitution contro bit 3 on.
X640	0X01	Substitution control reg bit 4	Unexpected level 2 interrupt. Reg X'14' = line adr causing the L2 interrupt. Reg X'11' = line adr that had ICW bit 41 (L2 pending) set. If reg X'11' does not equal reg X'14', there may be a LIB or scanner failure. If reg X'14'=reg X'11', the subst ctrl reg bit 4 is not working in which case reg X'14' is the line adr that should not have been scanned and therefore should not have caused a level 2 interrupt.	B3E2 B3D2	CS001 CX009	B-220	SCR bit 4 is set and an attempt is made to cause a L2 interrupt on lines 8 & 9 of all LIBs. These addresses should not be scanned.
X645	XXXX	Diagnostic transmit test for start/stop line sets. All installed line addresses that will run in start/stop mode are tested, one at a time. The test goes through transmit initial (PCF=8) to transmit data (PCF=9) through transmit turn-around (PCF=9 to PCF=7). The characters transmitted are a PAD character of X'FF' followed by two data characters of X'AA'. The start stop LCD of 7 (start bit, 8 data bits, 2 stop bits) is used in this test. You should reference notes 4 and 7 in section T2CS-NOTES for aid in problem determination if this routine detects any errors. Prior to setting transmit initial the program does a set mode with the 'diagnostic mode' bit on. If this set mode fails you will get pretest error stop codes in display B beginning with 1. These codes may be found in section T2CS-COM near the end of the symptom index. With 'diagnostic mode' set properly the scanner should force on the 'clear to send' condition so that when transmit initial is set the next bit time should result in PCF changing from 8 to 9 (transmit initial to transmit data). The most likely source of hardware failure for this routine is in the line set card(s) for the line address that is under test.					
X645	0X01	Diagnostic transmit test for start/stop.	L2 interrupt did not occur after transmit initial was set. Display reg. X'45' and check byte 0, bits 0-3 for feedback check (all bits on). LCD should =7, PCF should =9. (PCF was set to 8 by program). Reg X'11'=line address under test. See routine heading for more information.	A3L2	TA611	B-310 B-260	The scanner hardwar should change the P from 8 to 9 when it detects 'CTS' which should be forced on by the scanner if 'diagnostic mode latch' set on properly when the set mode was done. After scanne changes PCF to 9, it should serialize and transmit a bit every bit service time and cause a char-svc L2

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETHM PAGE	COMMENTS
							interrupt when the PAD char has been sent.
X645	0X02	Diag transmit test for start/stop.	Level 2 interrupt was not from expected line adr. Reg X'14'=line adr that caused the level 2 interrupt. Reg X'11'=line address that level 2 was expected from.	A3L2	TA611	B-300	Check scanner, osc. and LIB clock if no level 2 interrupt occurred or L2 was from the wrong line addr. See rtn heading for more information.
X645	0X03	Diag transmit test for start/stop.	Primary control field (PCF) did not change to X'9'. Reg X'11'=line address under test. See routine heading for more information.	A3F2	TA811	B-080	Scanner should chan PCF to 9 from 8 whe it detects 'clear t send' which should be forced by the scanner if diagnostic mode set properly.
X645	0X04	Diag transmit test for start/stop.	No level 2 interrupt after 2nd transmitted char. Reg X'11'=line address under test. If LCD=F a feedback check has occurred. LCD should = 7, PCF should = 9.	A3L2	TA611	B-310	
X645	0X05	Diag transmit test for start/stop.	2nd level 2 interrupt from wrong line address. See error stop 0X02 for regs.	A3L2	TA611	B-300	See rtn heading for more informatio
X645	0X06	Diag transmit test for start/stop.	No L2 for transmit turnaround. Reg X'11' =line address under test. Check reg X'45' for LCD. If LCD=F a feedback check occurred. LCD should = 7, PCF should = 7 since PCF was set to 'D' (transmit turnaround) on the previous character service level 2 interrupt.	A3L2	TA611	B-310 B-080	See rtn heading for more informatio
X645	0X07	Diag transmit test for start/stop.	3rd level 2 interrupt from wrong line adr. See error stop code 0X02 above for regs.	A3L2	TA611	B-310	See rtn heading for more informatio
X645	0X08	Diag transmit test for start/stop.	PCF did not change to X'7' (receive mode) after turn-around or LCD changed. Reg X'11'=line adr under test.	A3F2	TA811	B-080	Scanner should chan PCF to 7 on normal turn-around completion. LCD should be 7.
X645	0X09	Diag transmit test for start/stop.	SDF did not set to 0.	A3H2	TA221	B-480	SDF should be chang to 0 by scanner hardware on transmit turnaround. Reg X'15' byte 0, bits 6 and 7 contain SDF bits 0 and 1. Byte 1 contains SDF Bits 2-9.

X64A XXXX Diagnostic receive mode bit service and tag detection test. All line sets that will run in start/stop or synchronous mode are tested. After the set mode is completed a bit pattern of X'0301' for start/stop line sets or X'0201' for synchronous line sets is output to SDF via an output to reg X'46'. Then the PCF is set to 7 (receive mode) with a LCD=7 for start/stop line sets or LCD=C for a synchronous line set. For start/stop line sets this should cause a character service level 2 interrupt on the first scan cycle after the next bit service occurs in the line set. For a synchronous line set (due to LCD=C) the character service level 2 interrupt should occur after the second bit service and should strobe a one bit into PDF bit 0 from the Test Data Latch. In either case the result should be a character of X'C0' in the PDF when the character service occurs.

X64A	0X01	Diagnostic receive mode bit deserializing and bit service for all installed	PCF did not set to X'7' (receive mode) or LCD has changed. Reg X'11'=line	A3F2	TA811	B-190	Pgm did an output to reg X'45' to set LCD and PCF. Then a

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		line addresses in receive mode(PCF=7).	address of line set under test.				input X'45' is done to check LCD & PCF.
X64A	0X02	Diag receive mode, bit deserializing and bit service for all lines in receive mode.	Level 2 interrupt did not occur. Check oscillator, scanner limits, or LIB clock. Reg X'11' = line address expected to cause L2 interrupt.	A3L2	TA611	B-490	See rtn heading.
X64A	0X03	Diag receive mode, bit deserializing and bit service for all lines in rcv mode.	L2 interrupt from wrong adr. Reg X'14' = line adr that caused 12 interrupt. Reg X'11'= line adr expected to cause level 2 interrupt.	A3L2	TA611	B-300	See rtn heading.
X64A	0X04	Diag receive mode, bit deserializing and bit service for all lines in rcv mode.	Data byte in PDF (parallel data field) not expected data, or check flag on in ICW bits 0-3. Reg X'11'=line adr. Reg X'14'=flags and PDF input from Reg X'44'. Reg X'16'=expected bits that should be on in Reg X'14'.	A3E2 A3P2	TA311 TA131	B-490 B-420	See rtn heading.
X64C	XXXX	Diagnostic transmit test for synchronous lines. All installed line sets that will run in synchronous mode are tested from transmit initial (PCF=8) through transmit data (PCF=9) to transmit turnaround (PCF=D to PCF=5). Characters transmitted are two pad characters of X'AA' and the character X'32'. Prior to setting transmit initial the program does a set mode with the 'diagnostic mode' and 'sync bit clock' bits both on. If this set mode fails you will get pretest error stop codes in display B beginning with 1. These codes may be found in section T2CS-COM near the end of the symptom index. With 'diagnostic mode' set properly the scanner should force on the 'clear to send' condition so that when transmit initial is set the next bit time should result in PCF changing from 8 to 9 (transmit initial to transmit data).					
X64C	0X01	Diagnostic transmit test for BSC line sets.	Level 2 did not occur after transmit initial. LCD should= C. If LCD=F a feedback check occurred so line set or LIB is probably in error. If LCD=C check PCF. PCF was set to 8 but should have changed to 9 as the 1st character was transmitted. If the character was not transmitted check for oscillator/LIB clock error or scanner failure.	A3L2	TA611	B-310 B-260	See rtn heading and notes 4 and 7 i T2CS-NOTES for checks to make information to to aid problem determination. Reg X'11'=line addr of line set under test.
X64C	0X02	Diag transmit test for BSC	Level 2 from wrong line adr. Display reg X'14' for line adr that caused the level 2 interrupt: reg X'11' for the line adr expected to cause the level 2 interrupt.	A3L2	TA611	B-300	See notes 4 & 7 in T2CS-NOTES for problem determination. aids.
X64C	0X03	Diag transmit test for BSC	PCF did not change to X'9' (transmit data). Reg X'11'= line adr. LCD & PCF same as error 0X01.	A3F2	TA811	B-080	See rtn heading.
X64C	0X04	Diag transmit test for BSC	2nd L2 interrupt did not occur. See error 0X01 above for LCD & PCF.	A3L2	TA611	B-310 B-260	See rtn heading.
X64C	0X05	Diag transmit test for BSC	2nd L2 interrupt from wrong line address. Check failing line adr for cause of error. See routine heading.	A3L2	TA611	B-300	Reg X'14'=line addr that caused the L2 in error. Reg X'11' = line addr expected to cause L2.
X64C	0X06	Diag transmit test for BSC	L2 interrupt did not occur after setting PCF X'D' for transmit turnaround. Check if LCD=F(feedback check). PCF should=5 since on last char service it was set to 'D'. If PCF is not 5 then turn-around did not work. Reg X'11'=line adr under test.	A3L2	TA611	B-080	See rtn heading. LCD should =C. PCF should have changed to 5.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X64C	0X07	Diag transmit test for BSC	3rd L2 interrupt from wrong line address. Check failing line adr for cause of error. See routine heading.	A3L2	TA611	B-300	Reg X'14'=line addr that caused the L2 in error. Reg X'11' = line addr expected to cause L2.
X64C	0X08	Diag transmit test for BSC	PCF did not change to 5 on transmit turnaround or LCD is not=C. Reg X'11'=line address under test.	A3F2	TA811	B-080	PCF should change to 5 and LCD should have remained at C.

X650 XXXX Wrap data test for start stop line sets using LCD=7. All lines that run in start/stop mode (except telegraph line sets) are wrapped two at a time. The first installed S/S line is made the receive line and the next installed S/S line is made a transmit line. As each pair of lines completes its wrap, the lines are reset. The line that was the transmit line is now made the receive line and the next installed S/S line is made the transmit line. This is continued until the last installed S-S line has been used as a transmit line. The last installed S/S line is then made a receive line and the first installed line is made the transmit line for the last wrap performed in this routine. Data sent on the transmit line will be the PAD character (X'FF') and the characters X'AA', X'01' and X'FE'. The test is run with LCD=7 so the hardware should add a start bit and two stop bits to the character being transmitted. The receive line should receive the transmitted characters except for the PAD character.

Note 1 : See notes 4, 5 and 7 in section T2CS-NOTES for more information and for aid in problem determination and isolation.

Note 2: For all error stops in this routine, the following registers are setup:
reg X'11' = transmit line address (as used to set ABAR)
reg X'13' = receive line address (as used to set ABAR)
reg X'14' for errors that indicate level 2 interrupt occurred from wrong address and contains the line address that caused the L2 interrupt.

reg X'14' for errors that indicate the received data is bad, or indicates that ICW bits 0-7 are in error and contains ICW bits 0-15 from the receive line ICW obtained by executing Input X'44'. ICW bits 8-15 (the PDF) contain the received data. ICW bits 0-7 are check and control flags and are always expected to be set as follows:
ICW bit 0 = Stop bit check and should be off
ICW bit 1 = Service request and should be on
ICW bit 2 = Character overrun/underrun and should be off
ICW bit 3 = Modem check and should be off
ICW bit 4 = Receive line signal detector. This bit is ignored in this test.
ICW bit 5 = Reserved bit. This bit is ignored in this test.
ICW bit 6 = Program flag. This bit is ignored in this test.
ICW bit 7 = Pad flag. This bit is ignored in this test.
reg X'16' for errors that indicate the received data is bad, and contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'.

The receive line always has the display bit on in its ICW, so register X'46' is valid for the receive line under test. All lines are set to priority 3 and oscillator select 0. The following error codes are listed in the sequence that the actual test is run.

X650	0X01	First level 2 interrupt for transmit line address (not counting the set mode).	No level 2 interrupt occurred. Reg X'11' = transmit line adr. Reg X'13' = receive line adr.	A3L2	TA611	B-310 B-260	Should have char-service L2 interrupt from the transmit line address after the P char was transmitte See notes 4, 5 and in section T2CS-NOT for checks to make and aids in problem determination.
X650	0X02	First level 2 interrupt for transmit line address.	Level 2 interrupt from wrong line address. Reg X'11'= transmit line address and the line address expected to cause the L2 interrupt. Reg X'13'=receive line adr. Reg X'14'=line adr that caused the level 2 interrupt.	A3L2	TA611	B-300	See checks & commen in the Rtn heading.
X650	0X03	Transmit line PCF changed to 9 as the PAD character of X'FF' is transmitted.	Transmit line PCF did not change to 9 or LCD not = 7. Reg X'11' = transmit line address.	A3F2	TA811	B-080	See checks & commen in the Rtn heading. Character X'01' is output to the PDF

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							of transmit line after this error display. Previous PDF character of X'AA' should now be in process of transmission from SDF.
X650	0X04	Receive line receiving character X'AA'. (First receive line L2 interrupt after set mode).	No level 2 interrupt occurred. Reg X'11' = transmit lineadr. Reg X'13'=receive line adr and line address expected to cause the level 2 interrupt. sync 2.	A3L2	TA611	B-490	See checks & commen in the Rtn heading. This should be the 2nd L2 interrupt after prog set scope
X650	0X05	Receive line receiving character X'AA'.	Level 2 interrupt from wrong address. Reg X'11' = transmit line adr. Reg X'13' = receive line adr; the line expected to cause the level 2 interrupt. Reg X'14' = line adr causing the L2.	A3L2	TA611	B-300	See checks and comments in the routine heading.
X650	0X06	Receive linereceiving character X'AA'.	Recieve linePCF not = 7 or LCD not = 7. Reg X'13' = receive line address.	A3F2	TA811	B-080	Rec PCF was set to 7(rec mode) by t prog and should not have changed. See checks and comments in the routine heading.
X650	0X07	Receive line receiving character X'AA'.	Received data in receive line PDF not X'AA', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-490	See rtn heading for registers & checks.
X650	0X08	Transmit of X'AA' completed.	No level 2 interrupt occurred. Reg X'11' = transmit line adr expected to cause a L2.	A3L2	TA611	B-310 B-260	Should have completed the transmission of X'AA'. The X'01' that was in the PDF should have transferred to the SDF and be in the process of being transmitted. This is the 3rd L2 interrupt after firing scope sync 2. See checks & commen in routine heading.
X650	0X09	Transmit of X'AA' completed.	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr and the adr expected to cause the L2. Reg X'13'= receive line adr. Reg X'14' =line adr that caused the L2.	A3L2	TA611	B-300	See checks & commen in the Rtn heading. After this error display, the transmit lines PDF is set to X'FE' for the next transmit character.
X650	0X0A	Receive character X'01'	No level 2 interrupt occurred. Reg. X'13' = receive line address expected to cause a character-service level 2 interrupt.	A3L2	TA611	B-490	Should receive char X'01' in PDF a char-service L2 interrupt. This should be 4th L2 (2nd from receive line adr) after pro set scope sync 2. S routine heading for registers & checks.
X650	0X0B	Receive character X'01'.	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr. Reg X'13' = receive line adr and the adr expected to cause level 2 interrupt.	A3L2	TA611	B-300	See checks and comments in the routine heading.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			Reg X'14' = line adr causing L2 interrupt.				
X650	0X0C	Receiving character X'01'.	Data Received not X'01', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-490	See checks & commen in routine heading.
X650	0X0D	Transmit of X'01' completed.	No level 2 interrupt occurred. Reg X'11' = transmit line adr expected to cause the level 2 char-svc interrupt.	A3L2	TA611	B-310 B-260	Should have just completed transmission of char X'01'. X'FE' should have been transferred from the PDF to the SDF and be in the process of being transmitted. This is the 5th L2 (3rd from transmit line adr) after pro set scope sync 2. See checks & commen in routine heading.
X650	0X0E	Transmit of X'01' completed.	Level 2 interrupt from wrong line address. Reg X'11'= transmit line adr and adr expected to cause the L2. Reg X'13'=receive line adr. Reg X'14'=line adr that caused the level 2 interrupt.	A3L2	TA611	B-300	See checks & commen in the Rtn heading. After this error check is made, the transmit lines PCF is set to 'D' to cause transmit turnaround.
X650	0X0F	Receive character X'FE'.	No L2 interrupt occurred.	A3L2	TA611	B-490	This is the 6th L2 (3rd from receive line adr). Last L2 expected for receive line. See checks and comments in the routine heading.
X650	0X10	Receiving character X'FE'	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr. Reg X'13' = receive line adr and adr expected to cause level 2 interrupt. Reg X'14' = line adr causing the L2 interrupt.	A3L2	TA611	B-300	See checks and comments in the routine heading.
X650	0X11	Receiving character X'FE'.	Received data not X'FE', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-490	See comments in routine heading.
X650	0X12	Transmit of X'FE' completed and transmit turnaround.	No level 2 interrutp occurred. Reg X'11' = transmit line adr and adr expected to cause L2.	A3L2	TA611	B-310 B-260	7th L2 line 4th from rec addr) after prog set scope sync 2. Transmit turnaround (PCF=D) was set after the previous L2 interru for transmit line so transmit line should now be turned around to receive mode (PCF=7).
X650	0X13	Transmit of X'FE' completed and transmit turnaround.	L2 interrupt from wrong adr. Reg X'11' = transmit line adr & adr expected to cause the L2. Reg X'13'=receive line address. Reg X'14'=line address that caused the level 2 interrupt.	A3L2	TA611	B-300	See checks and comments in the routine heading.
X650	0X14	Transmit turnaround.	Transmit line PCF did not change to 7 on turnaround, or transmit SDF did not set to 0 or LCD not=7.	A3F2 A3H2	TA811 TA211	B-080	When transmit turnaround is completed the S should be x'000', P

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							should be 7, LCD should be 7. See checks and comments in the routine heading.
X651	XXXX	Wrap data test for telegraph line sets. All telegraph line addresses are wrapped, two at a time. The 1st telegraph line address is made the receive line then the next installed telegraph line is made a transmit line. As each pair of lines completes its wrap the lines are reset. The line that was the transmit line is now made the receive line and the next installed telegraph line is made the transmit line. This is continued until the last installed telegraph line has been used as a transmit line. The last installed telegraph line is then made a receive line and the first installed line is made the transmit line for the last wrap performed in this routine. Data sent on the transmit line will be the PAD character of X'FF' and the characters X'AA', X'01' and X'FE'. The test is run with LCD=7 so the hardware should add a start bit and two stop bits to the character being transmitted. The receive line should receive the transmitted characters except for the PAD character. Note: See notes 4, 5 and 7 in section T2CS-NOTES for more information and for aid in problem determination and isolation. Throughout this test, register X'11' contains the transmit line address and register X'13' contains the receive line address. The receive line will always have the display bit on in its ICW so register X'46' is valid for the receive line under test. All lines are set to priority 3 and oscillator select 0. Note: when telegraph lines are wrapped, an echo check will occur if there is no external current loop. This echo check sets modem error (ICW bit 3) that prevents service request interlock from being set. This routine ignores the modem error and all the ICW 0-7 error conditions. The following error codes are listed in the sequence that the actual test is run.					
X651	0X01	First level 2 for transmit line (not counting set mode).	No level 2 interrupt occurred. Reg X'11' = transmit line adr. Reg X'13' = receive line adr.	A3L2	TA611	B-310 B-260	Should have char-service L2 interrupt after the PAD character was transmitted. See notes 4, 5 & 7 T2CS-NOTES for checks and aids in problem determination.
X651	0X02	First level 2 interrupt for transmit.	Level 2 interrupt from wrong address. Reg X'11' = transmit line adr: the adr expected to L2 interrupt. Reg X'13' = receive line adr. Reg X'14' = line adr that caused the level 2.	A3L2	TA611	B-300	See checks and comments in the routine heading.
X651	0X03	Transmit line PCF changed to 9 as the PAD character X'FF' is transmitted.	Transmit line PCF did not change to 9. Reg X'11' = transmit line adr.	A3F2	TA811	B-080	See checks & commen in the Rtn heading. Character X'01' is set in transmit PDF after this error display. Previous PDF character of X'AA' should now be in process of transmission from SDF.
X651	0X04	Receive line receiving character X'AA'. (First receive line L2 interrupt after set mode.)	No level 2 interrupt occurred. Reg X'11' = transmit line adr. Reg X'13' = receive line adr and the line adr expected to cause L2.	A3L2	TA611	B-490	See checks & commen in the Rtn heading. This is the 2nd L2 after program se scope sync 2.
X651	0X05	Receive line receiving character X'AA'.	Level 2 interrupt from wrong address. Reg X'11' = transmit line adr. Reg X'13' = receive line adr; the line expected to L2 interrupt. Reg X'14' = line adr causing L2.	A3L2	TA611	B-300	See checks and comments in the routine heading.
X651	0X06	Receive line receiving character X'AA'.	Receive line PCF not = 7. Reg X'13' = receive line adr.	A3F2	TA811	B-080	Rec PCF was set to 7 (receive mode)

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							prog during initial setup and should have remained at 7. See checks and comments in the routine heading.
X651	0X07	Receiving X'AA'	Received data in PDF not X'AA'.	A3E2	TA311	B-490	See checks & commen in routine heading.
X651	0X08	Transmit of X'AA' completed.	No level 2 interrupt occurred. Reg X'11' = transmit line adr expected to cause the L2.	A3L2	TA611	B-310 B-260	Should have just completed transmission of X'AA'. The X'01' that was in the PDF should have transferred to the SDF and be in the process of being transmitted. This is the 3rd L2 interrupt after firing of scope sync 2. See checks and comments in routine heading.
X651	0X09	Transmit of X'AA' completed.	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr: the adr expected to cause L2. Reg X'13'=receive line address. Reg X'14'= line adr that caused L2.	A3L2	TA611	B-300	See comments in routine heading. After this check is made, the transmit PDF is set to X'FE' as next. char to transmit
X651	0X0A	Receive character X'01'	No level 2 interrupt occurred. Reg. X'13' = receive line addr expected to cause the level 2 interrupt.	A3L2	TA611	B-490	Should have receive char X'01' and had char-service L2 interrupt. This should be 4th L2 interrupt (2nd from receive line adr) after firing scope sync 2. See checks and comments under error 0X01.
X651	0X0B	Receive character X'01'.	Level 2 from wrong adr. Reg X'11' = transmit line adr. Reg X'13' = receive line adr, the adr expected to cause L2. Reg X'14' = adr line causing L2 interrupt.	A3L2	TA611	B-300	See comments in routine heading.
X651	0X0C	Receiving character X'01'.	Data Received in PDF not X'01'	A3E2	TA311	B-490	See checks and comments in routine heading.
X651	0X0D	Transmit of X'01' completed.	No level 2 interrupt occurred. Reg X'11' = transmit line address expected to cause the L2 interrupt.	A3L2	TA611	B-310 B-260	Should have just completed transmitting X'01'. Char X'FE' should have been transferred from th PDF to the SDF and in the process of being transmitted. This is the 5th (3rd from transmit) L2 interrupt after firing scope sync 2. See checks and

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							comments in Rtn heading.
X651	0X0E	Transmit of X'01' completed.	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr and the adr expected to L2 interrupt. Reg X'13' = receive line address. Reg X'14' = the line address that caused the L2 interrupt.	A3L2	TA611	B-300	See checks & commen in routine heading. After this display, set transmit PCF to 'D' for transmit turnaround.
X651	0X0F	Receive character X'FE'.	No L2 interrupt occurred.	A3L2	TA611	B-490	This is the 6th L2 (3rd from receive line addr) and last L2 interrupt for receive line adr. See checks and comments in error 0X01.
X651	0X10	Receiving character X'FE'	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr. Reg X'13' = receive line adr: the adr expected to L2 interrupt. Reg X'14' = line adr causing the L2 interrupt.	A3L2	TA611	B-300	See comments in routine heading.
X651	0X11	Receiving character X'FE'.	Data received in PDF not X'FE'	A3E2	TA311	B-490	See comments in routine heading.
X651	0X12	Transmit of X'FE' completed and transmit turnaround.	No level 2 interrupt occurred. Reg X'11'= transmit line address expected to cause a L2 interrupt.	A3L2	TA611	B-310 B-260	This is the 7th L2 (4th from transmit line addr) after set scope sync 2. Transmit turnaround (PCF=D) was set after previous L2 interrupt for transmit line so transmit line should now be turned around to receive mode (PCF=7).
X651	0X13	Transmit of X'FE' completed and transmit turnaround.	L2 interrupt from wrong adr. Reg X'11' = transmit line adr the L2 was expected from. Reg X'13' = receive line adr. Reg X'14' = line adr that caused the L2.	A3L2	TA611	B-300	See error 0X14 for expected LCD,PCF and SDF. See comments in Rtn heading for more info.
X651	0X14	Transmit turnaround.	Transmit line LCD not =7 or PCF did not change to 7 on turnaround or transmit SDF did not set to 0.	A3F2 A3H2	TA611 TA211	B-080	When transmit turnaround is completed SDF should=X'00', PCF should change to X'7'. See checks and comments in error stop 0X01.

X652 XXXX Wrap data test start/stop line sets with LCD's of 0, 2, 4, 5, and 6. All installed S/S line addresses, except telegraph, are wrapped two at a time. The first installed S/S line is made the receive line and the next installed S-S line is made a transmit line. As each pair of lines completes its wrap, the lines are reset. The line that was the transmit line is made the receive line and the next installed S/S line is made the new transmit line. Then the test is run on this pair of lines. This is continued until the last installed S-S line has been used as a transmit line. At this time, the last installed S/S line is made a receive line and the first installed line is made the transmit line and the test is run. After the above is done with LCD=0, the whole process is repeated for LCD=2, then for LCD=4, then for LCD=5, then for LCD=6. Note: LCD=7 is tested in routine X650. This test is not run if the 1st installed oscillator exceeds 1200 Bits Per Second.

Data to be transmitted and received for each LCD should be:

LCD=0 - Data= X'2A', X'01', and X'3E'

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			LCD=2 - Data= X'0A', X'01', and X'1E' LCD=4 - Data= X'2A', X'01', and X'7E' LCD=5 - Data= X'2A', X'01', and X'7E' LCD=6 - Data= X'AA', X'01', and X'FE'				

The hardware should add a start bit and one or two stop bits to the transmitted character according to LCD type. A PAD character (X'FF') is always transmitted before the data characters are transmitted. The receive line should receive the transmitted characters except for the PAD character.

Note : For all error stops in this routine, the following registers are setup:
reg X'11' = transmit line address (as used to set ABAR)
reg X'13' = receive line address (as used to set ABAR)
reg X'14' for errors that indicate level 2 interrupt occurred from wrong address and contains the line address that caused the L2 interrupt.

reg X'14' for errors that indicate the received data is bad, or indicates that ICW bits 0-7 are in error and contains ICW bits 0-15 from the receive line ICW obtained by executing Input X'44'. ICW bits 8-15 (the PDF) contain the received data. ICW bits 0-7 are check and control flags and are always expected to be set as follows:
ICW bit 0 = Stop bit check and should be off
ICW bit 1 = Service request and should be on
ICW bit 2 = Character overrun/underrun and should be off
ICW bit 3 = Modem check and should be off
ICW bit 4 = Receive line signal detector. This bit is ignored in this test.
ICW bit 5 = Reserved bit. This bit is ignored in this test.
ICW bit 6 = Program flag. This bit is ignored in this test.
ICW bit 7 = Pad flag. This bit is ignored in this test.

reg X'16' for errors that indicate the received data is bad, and contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'.
reg X'16' for errors that indicate LCD changed or PCF is bad - contains expected LCD and PCF in byte 0.

The receive line always has the display bit on in its ICW, so register X'46' is valid for the receive line under test. All lines are set to priority 3 and oscillator select 0. Reference notes 4, 5 and 7 in section T2CS-NOTES for aid in problem determination. The following error codes are listed in the sequence that the actual test is run.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X652	0X01	First level 2 interrupt for transmit line (not counting set mode).	No level 2 interrupt occurred. Reg X'11' = transmit line adr. Reg X'13' = receive line adr.	A3L2	TA611	B-310 B-260	Should have char-service L2 interrup after the PAD char was transmitted. Check LCD for feedback check. You may use the continue function to check if only this line set, this LIB, or all lines in the scanner are failing. If all lines are failing the first oscillator card or the scanner card are probably bad. If all lines in one LIB are failing, check the bit clock control card. If only 1 line or a pair of lines are failing, the problem is probably the line set card(s) for the failing line addresses.
X652	0X02	First level 2 interrupt for transmit.	Level 2 interrupt from wrong address. Reg X'11' = transmit line adr; the adr expected to L2 interrupt. Reg X'13' = receive line adr. Reg X'14'	A3L2	TA611	B-300	See checks and comments under error 0X01

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			= line adr that caused the level 2.				
X652	0X03	Transmit line PCF changed to 9 as the PAD character X'FF' is transmitted.	Transmit line PCF did not change to 9 or LCD changed. Reg X'11' = transmit line address.	A3F2	TA811	B-080	See checks & commen under error stop co 0X01. Set X'01' in transmit PDF after this error display. Previous PDF character of X'AA' should be in process of transmission from SDF now.
X652	0X04	Receiving first character.	No level 2 interrupt occurred. Reg X'13'=receive line adr and line adr expected to cause the L2. Reg X'11'= the transmit line address.	A3L2	TA611	B-490	See checks & commen under error stop co 0X01. This is the 2nd L2 after prog set scope sync 2.
X652	0X05	Receiving first character.	Level 2 interrupt from wrong line adr. Reg X'13'=receive line adr; the line expected to L2 interrupt. Reg X'11'=transmit line adr. Reg X'14'=line adr that caused L2.	A3L2	TA611	B-300	See checks and comments under error 0X01
X652	0X06	Receiving first character.	Receive line PCF not = 7 or LCD changed. Reg X'13'=receive line adr.	A3F2	TA811	B-080	Set Rec PCF to 7 (rec mode) during initial setup and should ha remained at 7. See the Rtn heading for registers and checks.
X652	0X07	Receiving first character.	Receive data in PDF not = expected receive data, or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-490	See rtn heading for registers. See comments under error stop co 0X01 for aid in determining the failing pattern.
X652	0X08	Transmit of X'AA' completed.	No level 2 interrupt occurred. Reg X'11' = transmit line adr expected to cause the L2 interrupt.	A3L2	TA611	B-310 B-260	Should have just completed the transmission of X'AA'. The X'01' that was in the PDF should have transferred to the SDF and be in the process of being transmitted. This is the 3rd L2 interrupt after firing scope sync 2. See checks and comments under error 0X01.
X652	0X09	Transmit of X'AA' completed.	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr; the adr expected to L2 interrupt. Reg X'13' = receive line adr. Reg X'14' = line address that caused the level 2 interrupt.	A3L2	TA611	B-300	See checks & commen under error stop code 0X01. After this error display the transmit lines PDF is set to X'FE'.
X652	0X0A	Receive character X'01'	No level 2 interrupt occurred. Reg X'13' = receive line adr expected to cause L2.	A3L2	TA611	B-490	Should have receive the char X'01' in the PDF and had a character-service L2 interrupt. This should be the 4th L2 interrupt

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							(2nd from the receive line) after firing scope sync 2. See checks and comments under error 0X01.
X652	0X0B	Receive character X'01'.	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr. Reg X'13' = receive line adr; the adr expected to L2 interrupt Reg X'14' = adr line causing L2 interrupt.	A3L2	TA611	B-300	See checks and comments under error 0X01.
X652	0X0C	Receiving character X'01'.	Data Received not X'01', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-490	See comments under error code 0X07.
X652	0X0D	Transmit of X'01' completed.	No level 2 interrupt occurred Reg X'11' = transmit line adr expected to cause the L2.	A3L2	TA611	B-310 B-260	Should have just completed transmitting character X'01'. Char X'FE' should have transferred from the PDF to the SDF and be in the process of being transmitted. This is the 5th L2 (3rd from transmit line adr) after setting scope sync 2. See checks and comments under error 0X01.
X652	0X0E	Transmit of X'01' completed.	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr the L2 was expected from. Reg X'13' = receive line adr. Reg X'14' = line adr that caused L2 interrupt.	A3L2	TA611	B-300	See checks & commen under error stop co 0X01. After this error set transmit PCF to 'D' for turnaround.
X652	0X0F	Receiving 3rd character.	No L2 interrupt occurred.	A3L2	TA611	B-490	This is the 6th L2 (3rd from receive line adr) and last L2 interrupt for receive line. See checks and comments under error 0X01.
X652	0X10	Receiving 3rd character.	Level 2 interrupt from wrong adr. Reg X'11' = transmit line adr. Reg X'13' = receive line adr; the line expected to L2 interrupt. Reg X'14' = line adr causing the L2 interrupt.	A3L2	TA611	B-300	See checks and comments under error 0X01.
X652	0X11	Receiving 3rd character.	Received data in PDF not = to expected data, or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-490	See comments under error 0X07 for ICW bits.
X652	0X12	Transmit of X'FE' completed and transmit turnaround.	No level 2 interrupt occurred. Reg X'11' = transmit line adr expected to cause the level 2 interrupt.	A3L2	TA611	B-310 B-260	This is the 7th L2 (4th from the transmit line addr) after prog se scope sync 2. Transmit turnaround (PCF=D) was set after previous L2 for transmit line so transmit line should now be turned around to receive mode. (PCF=7).

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X652	0X13	Transmit of X'FE' completed and transmit turnaround.	L2 interrupt from wrong adr. Reg X'11' = transmit line adr; the adr expected to L2 interrupt. Reg X'13' = receive line adr. Reg X'14' = line adr that caused the L2 interrupt.	A3L2	TA611	B-300	See checks and comments under error 0X01.
X652	0X14	Transmit turnaround.	Transmit line PCF did not change to 7 on turnaround, or transmit SDF did not set to 0 or LCD is not=7.	A3F2 A3H2	TA811 TA211	B-080	When transmit turnaround is completed the SDF should = 000, PCF should =7, LCD shou =7. See comments in error code 0X01.

X656 XXXX Synchronous line sets wrap data test. All installed line addresses that run in synchronous mode (even though they also run in start/stop mode and have been already tested in routine X650) are wrapped two at a time. The first installed synchronous line address is made the receive line and the next installed synchronous line address is made the transmit line address. The test is performed on this pair of lines. When the test is completed on this pair of lines, the lines are reset and the line that was the transmit line is now made the receive line and the next installed synchronous line address is made the new transmit line. This pair of lines is then wrapped. This stepping through the lines is continued until the last installed synchronous line has been the transmit line. Then the first installed line is made the transmit line and the last installed synchronous line is made the receive line and this pair of lines is wrapped. All the installed synchronous line sets are wrapped with LCD=C and then the above procedure is repeated using LCD=D.

A set mode is executed for both the transmit and receive line addresses with ICW bit 27 (diagnostic wrap mode) and ICW bit 29 (sync bit clock) on. Oscillator select bits are zeros to select the first oscillator. The priority bits are set to 3. The set mode is executed before the setting of scope sync 2 as each pair of lines is wrapped. The set mode must complete successfully for the wrap to function and any errors detected during the set mode are pre-test errors and all start with error code 1XXX. These error codes are located near the end of the symptom index following the routine error codes. References to level 2 interrupts in the following error code displays are the character service level 2 interrupts that occur after scope sync 2 is set and do not include the level 2 interrupts that occurred for the set modes that occur before scope sync 2.

Note 1: For all error stops in this routine, the following registers are setup:
reg X'11' = transmit line address (as used to set ABAR)
reg X'13' = receive line address (as used to set ABAR)
reg X'14' for errors that indicate level 2 interrupt occurred from wrong address and contains the line address that caused the L2 interrupt.

reg X'14' for errors that indicate the received data is bad, or indicates that ICW bits 0-7 are in error and contains ICW bits 0-15 from the receive line ICW obtained by executing Input X'44'. ICW bits 8-15 (the PDF) contain the received data. ICW bits 0-7 are check and control flags and are always expected to be set as follows:

ICW bit 0 = Stop bit check and should be off
ICW bit 1 = Service request and should be on
ICW bit 2 = Character overrun/underrun and should be off
ICW bit 3 = Modem check and should be off
ICW bit 4 = Receive line signal detector. This bit is ignored in this test.
ICW bit 5 = Reserved bit. This bit is ignored in this test.
ICW bit 6 = Program flag. This bit is ignored in this test.
ICW bit 7 = Pad flag. This bit is ignored in this tost.

reg X'16' for errors that indicate the received data is bad, and contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'.

Note 2: Checks to be made on all error stops:
a. Check LCD of failing line address. If LCD=F, a feedback check has occurred. If the configuration data set (CDS) erroneously indicates a line set is installed that will run in synchronous mode, a feedback check will occur.
b. You may use the continue function (except on pre-test errors starting with 1) to continue from this error to (1) see if just this line address is failing, (2) see if all line addreses in this LIB are failing, or (3) see if all synchronous lines are failing. You may get additional error stops on the same line pair being wrapped so you may have to use the continue function multiple times. If only one line set is failing, or a pair of even/odd addresses, then the line set card is probably bad. If all addresses fail in one LIB, the LIB's bit clock control card may be bad, or the terminators may be bad. If all synchronous line addresses fail, the scanner cards may be bad. If the line addresses are the type that run in both synchronous and start/stop mode, and if they run successfully in routine X652, then suspect LCD=C or LCD=D circuitry or the sync bit clock control line. Reference LIB card positions in section C-xxx (LIBs and line sets) because card locations

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		vary in location according to LIB types.					
		The transmitted data characters are shifted by one data bit position from the received data characters to generate a predictable interrupt sequence. See notes 4 and 6 in section T2CS-NOTES for more information about this shifting of transmitted data characters. Transmit Data - 55 55 19 19 50 7F 80 00 (when using EBCDIC LCD of C) Receive Data - 32 A0 FE 00 01 (when using EBCDIC LCD of C) Transmit Data - 55 55 0B 0B 50 7F 80 00 (when using USASCII LCD of D) Receive Data - 16 A0 FE 00 01 (when using USASCII LCD of D). The routine is run in the sequence of the following error codes.					
X656	0X01	Transmit of 1st PAD completed.	No level 2 interrupt occurred from transmit line address.	A3L2	TA611	B-310 B-260	1st char-service L2 interrupt after sco sync 2. See notes 1 2 in the heading of this routine for registers and checks.
X656	0X02	Transmit of 1st PAD completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks.
X656	0X03	Transmit PCF changes from 8 to 9.	Transmit PCF not = 9 or LCD changed.	A3F2	TA811	B-080	Transmit PCF was se to 8 by program during hardware setup. The scanner hardware should have changed the PCF to 9 and should now be in process of transmitting 2nd pad character. The transmit PDF is set to the 1st SYN character after this error display. See notes 1 & 2 in heading of this routine for registers & checks.
X656	0X04	Transmit of 2nd PAD completed.	No level 2 interrupt occurred from transmit line address.	A3L2	TA611	B-310 B-260	2nd level 2 interru after scope sync 2. See notes 1 & 2 in the heading of this routine for registers and checks.
X656	0X05	Transmit of 2nd PAD completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit PDF is set with the 2nd SYN character.
X656	0X06	Transmit of 1st SYN completed.	No level 2 interrupt occurred from transmit line address.	A3L2	TA611	B-310 B-260	3rd level 2 interru after scope sync 2. See notes 1 & 2 in Rtn heading for registers and checks.
X656	0X07	Transmit of 1st SYN completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit PDF is

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							set to character X'A0' to be transmitted next. Should now be in process of transmitting 2nd SYN character.
X656	0X08	Receive 1st SYN.	Receive line PCF not = 7 or LCD changed.	A3F2	TA811	B-080	Receive line PCF wa set to 5. When the 1st SYN. character is received and recognized the hardware should set the receive PCF=7. Note: this setting of PCF=7 from PCF=5 does not cause a level 2 interrupt. See notes 1 & 2 in heading of this routine for registers and checks.
X656	0X09	Receive 2nd SYN.	No level 2 interrupt occurred from receive line address.	A3L2	TA611	B-310 B-420	4th L2 (1st from th receive line addr) after scope sync 2. See notes 1 & 2 in heading of this routine for registers & checks.
X656	0X0A	Receive 2nd SYN.	Level 2 interrupt not from receive line address.	A3L2	TA611	B-300	See Rtn heading notes 1 and 2 for registers and checks.
X656	0X0B	Receive 2nd SYN.	Received data in PDF not a SYN character, or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-420	Received data in PD should = X'32' SYN if LCD=C or X'16' SYN char if LCD=D. See notes 1 & 2 in heading of this routine for registers, ICW bits 0-7, and checks to make.
X656	0X0C	Transmit of 2nd SYN completed.	No level 2 interrupt occurred for transmit line address.	A3L2	TA611	B-310 B-260	5th L2 (4th from th transmit line adr) after prog set scope sync 2. See notes 1 & 2 in heading of this routine for registers & checks.
X656	0X0D	Transmit of 2nd SYN completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks. After this error display the transmit PDF is set to character X'7F' as the next character to transmit. The character X'50' should now be in the

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							process of being transmitted.
X656	0X0E	Receive character X'A0'.	No level 2 interrupt occurred from the receive line adr.	A3L2	TA611	B-310 B-420	6th L2 (2nd from th receive line addr) after scope sync 2. See notes 1 & 2 in heading of this routine for registers & checks.
X656	0X0F	Receive character X'A0'.	Level 2 interrupt not from receive line adr.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks.
X656	0X10	Receive character X'A0'.	Received data in PDF not = X'A0', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-420	See rtn heading notes 1 and 2 for registers, ICW bits 0-7, and checks to make.
X656	0X11	Transmit of X'50' completed.	No level 2 occurred for transmit line address.	A3L2	TA611		7th L2 (5th from th transmit line addr). See notes 1 & 2 in heading of this routine for registers & checks.
X656	0X12	Transmit of X'50' completed.	Level 2 not from transmit line address.	A3L2	TA611		See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit PDF is set to X'80' as the next character to transmit. Should now be in process of transmitting the character X'7F'.
X656	0X13	Receive character X'FE'.	No level 2 interrupt occurred for receive line adr.	A3L2	TA611	B-310 B-420	8th L2(3rd from the receive line addr). See notes 1 & 2 in heading of this routine for registers and checks to make.
X656	0X14	Receive character X'FE'.	Level 2 interrupt not from receive line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks.
X656	0X15	Receive character X'FE'.	Received data in PDF not = X'FE', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-420	See rtn heading notes 1 and 2 for registers, ICW bits 0-7, and checks to make.
X656	0X16	Transmit of X'7F' completed.	No level 2 occurred for transmit line address.	A3L2	TA611		9th L2(6th from the transmit line addr). See notes 1 & 2 in heading of this routine for registers and checks.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X656	0X17	Transmit of X'7F' completed.	Level 2 not from transmit line address.	A3L2	TA611		See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit PDF is set to X'00' as the next character to transmit. Should now be in the process of transmitting X'80'.
X656	0X18	Receive character X'00'.	No level 2 interrupt occurred from receive line adr.	A3L2	TA611	B-310 B-420	10th L2 (4th from t receive line addr). See notes 1 & 2 in heading of this routine for registers and checks to make.
X656	0X19	Receive character X'00'.	Level 2 interrupt not from receive line adr.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks.
X656	0X1A	Receive character X'00'.	Received data in PDF not = X'00', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-420	See rtn heading notes 1 and 2 for registers, ICW bits 0-7, and checks.
X656	0X25	Transmit of X'80' completed.	No level 2 occurred from transmit line address.	A3L2	TA611		12th level 2 (7th from transmit.) See notes 1 & 2 in heading of this routine for registers and checks.
X656	0X26	Transmit of X'80' completed.	Level 2 not from transmit line address.	A3L2	TA611		See rtn heading notes 1 and 2 for registers & checks. After this error display, the transmit PCF is set to X'D' for transmit turn-around. Should now be in process of transmitting X'00' as last character to transmit.
X656	0X27	Receive character X'01'.	No level 2 occurred from receive line address.	A3L2	TA611		12th level 2 (7th from receive). See notes 1 & 2 in heading of this routine for registers and checks. Last L2 for receive.
X656	0X28	Receive character X'01'.	Level 2 not from receive line address.	A3L2	TA611		See rtn heading notes 1 and 2 for registers & checks.
X656	0X29	Receive character X'01'.	Received data in PDF not = X'11' or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131		See rtn heading notes 1 and 2 for registers, ICW bits 0-7, and checks. After this error display, the receive PCF is

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETHM PAGE	COMMENTS
							set to 0 so no further level 2 interrupts should occur from the receive line addr.
X656	0X2A	Transmit of X'00' completed and transmit turn-around.	No level 2 occurred from transmit line address.	A3L2	TA611		13th level 2 (10th from transmit) and should be the last level 2. See notes 1 & 2 in heading of this routine for registers and checks. At this time the transmit PCF should have turned around to PCF=5.
X656	0X2B	Transmit of X'00' completed and transmit turn-around.	Level 2 not from transmit line address.	A3L2	TA611		See rtn heading notes 1 and 2 for registers and checks. PCF should be turned around to PCF=5.
X656	0X2C	Transmit turn-around.	Transmit PCF did not turn around to PCF=5 or LCD changed.	A3F2	TA811		After previous transmit level 2 (see error 0X26) transmit PCF was set to X'D' to cause a turn-around. The hardware should have completed the transmission of the character X'00' and then set PCF=5. See notes 1 & 2 in heading of this routine for registers and checks.

X658 XXXX RPQ 10 bit time out test: Test will only run if the CDS block for the scanner under test has a bit on to define this RPQ. All lines that run in start/stop mode are wrapped two at a time. The first installed S/S line is made the receive line and the next installed S/S line is made a transmit line. As each pair of lines completes its wrap, the lines are reset. The line that was the transmit line is now made the receive line and the next installed S/S line is made the transmit line. This is continued until the last installed S/S line has been used as a transmit line. The last installed S/S line is then made a receive line and the first installed line is made the transmit line for the last wrap performed in this routine.

Data sent on the transmit line will be the PAD character (X'FF') and the characters X'7F', X'FF', X'FF', and X'FF'. The test is run with LCD=7 so the hardware should add a start bit and two stop bits to the character being transmitted.

Receive line will have ICW bit 39 set on to activate the RPQ. The ICW bit 7 pad flag is set to hold the start bit to a mark in place of the normal space. The receive line not seeing start bits will recognize the first space received as a start bit. This will cause the receive line to receive different data than was transmitted. Data received will be F5, 8 bit times of marks, FF, then 10 or more bit times of marks to give the RPQ time to time out.

Note : For all error stops in this routine, the following registers are setup:
reg X'11' = transmit line address (as used to set ABAR)
reg X'13' = receive line address (as used to set ABAR)
reg X'14' for errors that indicate level 2 interrupt occurred from wrong address and contains the line address that caused the L2 interrupt.

reg X'14' for errors that indicate the received data is bad, or indicates that ICW bits 0-3 are in error and contains ICW bits 0-15 from the receive line ICW obtained by executing Input X'44'. ICW bits 8-15 (the PDF) contain the received data. ICW bits 0-3 are check and control flags and are always

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			expected to be set as follows: ICW bit 0 = Stop bit check and should be off ICW bit 1 = Service request and should be on ICW bit 2 = Character overrun/underrun and should be off ICW bit 3 = Modem check and should be off ICW bit 4 = Receive line signal detect. This bit is ignored in this routine. ICW bit 5 = Reserved bit. This bit is ignored in the routine. ICW bit 6 = Program flag and should be off ICW bit 7 = Pad flag. This bit is ignored on the received data character ICW bits 0-15 tests. reg X'16' for errors that indicate the received data is bad, and contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'. Section T2CS-Notes is referenced by some of the error stops in this routine. These notes give more detailed information about the above regs. Section T2CS-Notes note 7 also give some information that you may use to help isolate the problem. The receive line always has the display bit on in its ICW, so register X'46' is valid for the receive line under test. All lines are set to priority 3 and oscillator select 0. The following error codes are listed in the sequence that the actual test is run.				
X658	0X01	First level 2 interrupt for transmit line (not counting set mode).	No L2 or L2 not from the transmit line address.	A3L2	TA611		Should have had a char service level interrupt after the PAD character was transmitted. See section T2CS-Notes notes 2, 5 & 7 for regs & checks.
X658	0X02	Transmit line PCF changed to 9 as the PAD character X'FF' is transmitted.	Transmit line PCF did not change to 9 or the LCD did remain at 7.	A3F2	TA811		See comments in the rtn heading X'FF' is set in PDF in transmit ICW after this error display. Previous PDF character of X'7F' should be in process of transmission from SDF now.
X658	0X04	Transmit of char X'7F' completed.	No L2 or L2 not from the transmit line address.	A3L2	TA611		Should have just completed the transmission of X'7F'. The X'FF' that was in the PDF should have transferred to the SDF and be in the process of being transmitted. This is the 3rd L2 interrupt after firing scope sync 2. See notes 2, 5 & 7 T2CS-NOTES for registers & checks.
X658	0X06	Receive character X'FF'.	No L2 or L2 not from the receive line address.	A3L2 A3F2	TA611		Should have receive char X'FF' and had a char-service L2. This should be the 2nd L2 interrupt 2 (1st from the receive line adr) after program set scope sync 2. See section T2CS-Notes notes 2, 5 & 7 for regs & checks.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X658	0X08	Receiving character X'FF'.	Data Received not X'FF', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131		See comments under error code 0X05.
X658	0X0A	Transmit of X'FF' completed.	No L2 or L2 not from the transmit line address.	A3L2	TA611		Should have just transmitted character X'FF'. Character X'57' should be transferred from the PDF to the SDF and be in the process of being transmitted. This is the 4th L2 (3rd from th transmit line adr) after program set scope sync 2. See notes 2, 5 and 7 in T2CS-NOTES for registers & checks.
X658	0X0C	Receive line is in a time out mode. LCD of 7, PCF of E.	Receive line PCF not = E or LCD not = 7. Reg X'13' = receive line adr.	A3F2 A3H2	TA811 TA211		Receive line PCF should change to E (receive timeout mode).
X658	0X10	Receive line is in a time out mode. ICW bit 39 set.	Receive line ICW bit 39 not on. Reg X'13'=receive line address.	A3J2 A3L2 A3G2	 TA611 TA021		Receive line ICW bi bit 39 was set on during the initial program setup and should have remained on.
X658	0X12	Transmit of char X'57' completed.	No L2 or L2 not from the transmit line address.	A3L2	TA611		Should have just completed the transmission of X'57'. The X'FF' that was in the PDF should have transferred to the SDF and be in the process of being transmitted. This is the 3rd L2 interrupt after firing scope sync 2. See section T2CS-Notes notes 2, 5 & 7 for regs & checks.
X658	0X14	Receive line receiving character X'F5'	Receive line PCF not = 7 or LCD not = 7. Reg X'13'= receive line address.	A3F2	TA811		Rec PCF was =E but should have changed to 7 when t start bit was received.
X658	0X16	Receive character X'F5'.	No L2 or L2 not from the receive line address.	A3L2	TA611		Should receive char X'F5' and had char-service level interrupt. This should the 6th L2 (2nd from the receive line adr) after program set scope sync 2. See notes 3, 5 and 7 in T2CS-NOTES for registers & checks.
X658	0X18	Receiving character X'F5'.	Data Received not X'F5', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131		See comments under error code 0X05.
X658	0X1A	Transmit of X'FF' completed.	No L2 or L2 not from the transmit line address.	A3L2	TA611		Should have transmitted

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETNM PAGE	COMMENTS
							character X'FF'. X'FF' should be transferred from the PDF to the SDF and is being transmitted. This is the 7th (5rd from transmit) L2 interrupt after firing scope sync 2. See section T2CS-Notes notes 2, 5 & 7 for regs & checks. After this error display, the transmit line PCF is set to D for transmit turnaround.
X658	0X1B	Receive Line time out	No L2 or L2 not from the receive line address.	A3L2	TA611		This is the 8th (3r from receive addr) and last L2 interru for receive line. See section T2CS-Notes notes 2, 5 & 7 for regs & checks.
X658	0X1C	Receive line time out.	Service request bit 0.1 should not be on but was.	A3P2 A2P2			SVC request bit should be blocked by the scanner because of the time-out.
X658	0X1E	Receive line timed out, test ICW	ICW bit 39 should have turned off because of the time out. Reg X'13' receive line addr Reg X'14' input 44 data Reg X'15' bits in error	A3P2 A3J2 A3L2			Receive line ICW bit 39 should have turned off because of the time out.
X658	0X20	Receive line time out.	Receive line PCF not = 7 or LCD not = 7. Reg X'13'= receive line address.	A3P2 A3H2			Receive line PCF wa = E but should have changed to 7 because of the time out.
X658	0X22	Transmit of X'FF' completed and transmit turnaround.	No L2 or L2 not from the transmit line address.	A3L2	TA611		This is the 9th L2 (6th from transmit line addr) after scope sync 2. Transmit turn-around (PCF=D) was set after the previous L2 from transmit line so transmit line should now be turned around to receive mode (PCF=7). See section T2CS-Notes notes 2,5 & 7 for regs an checks.
X658	0X24	Transmit turnaround.	Transmit line PCF did not change to 7 on turnaround, or transmit SDF did not set to 0 or LCD did not remain at 7.	A3P2 A3P2	TA811		When transmit turn-around is completed the SDF should = 000, PCF should = 7, LCD should remain at 7. See notes 2, & 7 in T2CS-NOTES for regs & checks.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

X65A **xxxx** DLC line sets wrap data test. All installed line sets that will run in DLC mode are wrapped two at a time. The first installed DLC line set is made the receive line and the next installed DLC line set is made the transmit line. The test is then performed on this pair of lines. When the test is completed on this pair of lines, the lines are reset and the line that was the transmit line is now made the receive line and the next installed DLC line set is made the new transmit line. Then this pair of lines is wrapped. This stepping up through the lines is continued until the last installed DLC line has been the transmit line. The first installed line is then made the transmit line and the last installed DLC line is made the receive line and this pair of lines is wrapped.

A set mode is done on both the transmit and receive lines with ICW bit 27 (diagnostic wrap mode) and ICW bit 29 (sync. bit clock) both on. Oscillator select bits are 0 so the first oscillator is selected. The priority bits are set to 3. The set mode is done before the setting of scope sync 2 as each pair of lines is wrapped. The set mode must be completed successfully for the wrap to function and any errors detected during set mode are pre-test errors and start with error code 1XXX. These error codes are near the end of the symptom index after all routine error codes. References to level 2 interrupts in the following error codes are the character service level 2 interrupts that occur after scope sync 2 is set and do not include level 2 interrupts that occurred for set mode before scope sync 2.

Note 1: On all error stops in this routine, the following registers are set up:

Reg X'11' = Transmit line set address (as used to set ABAR)
Reg X'13' = Receive line set address (as used to set ABAR)
Reg X'14' for errors that indicate no level 2 occurred or L2 from wrong address
= Line address that caused the L2 or = 0000 if no L2 occurred.

Reg X'14' for errors that indicate received data is bad or ICW bits 0-3 or 5 are in error
= What was obtained by an input X'44' from the receive line ICW (bits 0-15)
ICW bits 8-15 are the PDF and should contain the receive data
ICW bits 0-7 are error and control flags and are expected to be set as follows:

ICW bit 0 = Stop bit check, should be off
ICW bit 1 = Service request, should be on
ICW bit 2 = Character overrun, should be off except when misaligned flag character is detected.
ICW bit 3 = Modem check, should be off.
ICW bit 4 = Receive line signal detect(this bit is ignored in this test).
ICW bit 5 = DLC flag detect/disable stuffer remember, on when a flag character is detected
ICW bit 6 = Program flag(this bit is ignored.)
ICW bit 7 = Pad flag/disables stuffer bit, on only when a flag or pad char is set into the PDF for the transmit line address. This bit is ignored on the receive line address.

Reg X'14' for errors that indicate the LCD or PCF is bad, contain the LCD in byte 0 bits 0-3, and the PCF in byte 0 bits 4-7.
Reg X'16' for errors that indicate received data is bad, contains the expected ICW bits 0-15 that are being tested against the contents of Reg X'14' except bits 4,6 and 7 are ignored.

Note 2: Checks to be made on all error stops:

A. Check LCD of failing line set. If LCD=F, a feedback check has occurred. If the CDS indicates a line set that will run in synchronous mode is installed, but this is not the case, then a feedback check will occur.
B. Use the continue function (except on pre-test errors starting with 1) to continue from the error, to see if just this line set is failing, if all line sets in this LIB are failing, or if all DLC lines are failing. Multiple error stops on the same pair of wrapped lines may occur so the continue function may have to be used many times. If only one line set is failing or a pair of even/odd addresses, then the line set card is probably bad. If all addresses fail in one LIB, the LIB's bit clock control card or terminators may be bad. If all DLC line sets fail, the CS cards may be bad. If the line sets are the type that will run also in synchronous and start/stop mode and if they run successfully in routine X652 and X656 then suspect the LCD or DLC circuitry or sync bit clock control.

Note 3,

The transmitted characters are offset by 1 data bit so to cause receive data characters to be offset by 1 data bit from transmitted characters. See notes 4 and 6 in section T2CS-NOTES for more info.

Transmit data	-	AA	2A	3F	50	7F	00	7F
Receive data	-			flag	A0	FE	00	idle

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		All installed DLC line sets are tested in 8 bit mode(LCD=9). The routine is run in sequence of the following error codes.					
X65A	0X01	Transmit of 1st pad(X'AA') character completed.	No level 2 or L2 not from transmit line adr.	A3L2		TA611	1st level 2 char-service interrupt after program set scope scope sync 2. See notes 1 & 2 at heading of this routine for registers & checks.
X65A	0X02	Transmit of 1st pad(X'AA') character completed.	Transmit PCF not = 9 or LCD changed.	A3F2		TA811	Transmit PCF was se to 8 by prog in hardware setup. CS hardware should have changed it to 9. Should now be in process of transmitting 2nd pad. The transmit PDF is set to an offset flag char after this error. See notes in routine header.
X65A	0X03	Transmit of 2nd pad(X'2A') character completed.	No L2 or L2 not from transmit line address.	A3L2		TA611	2nd L2 after scope sync 2. See routine header for register & checks. After thi error display the the transmit PDF is set with X'3F' flag character.
X65A	0X04	Receive flag character X'7E'.	No level 2 or L2 not from transmit line address.	A3L2		TA611	3rd L2 after scope sync 2. See routine header for register & checks.
X65A	0X05	Receive flag character X'7E'.	Receive LCD not = 9 or PCF not = 6.	A3G2		TB021	Receiving a flag char should change PCF to 6.
X65A	0X06	Receive flag character	ICW bits 0-3 or 5 are in error.	A3G2		TB021	ICW bit 5 should be on; bits 0-3 should be off. Reg X'14' = ICW bits 0-15.
X65A	0X07	Transmit of flag (X'3F') character completed	No level 2 or L2 not from transmit line address.	A3L2		TA611	4th L2 after scope sync 2. See routine header for register & checks.
X65A	0X08	Receive data character 'A0'	No L2 or L2 not from receive line address.	A3L2		TA611	5th L2 after scope sync 2. See routine heading for registe & checks.
X65A	0X09	Receive data character 'A0'	The receive LCD was not=9 or PCF not=7	A3F2		TA811	Reg X'14' contains LCD in bits 0-3 and PCF in bits 4-7
X65A	0X0A	Receive data character 'A0'	The receive data not=X'A0' or ICW bits 0-3 or 5 in error	A3E2 A3P2		TA311 TA121	ICW bit 1 should be on. ICW bits 0,2,3 5 should be off.
X65A	0X0B	Transmit of data character '50' completed	No level 2 or L2 not from transmit line address.	A3L2		TA611	6th L2 after scope sync 2. See routine header for register & checks.
X65A	0X0C	Receive data character 'FE'	No level 2 or L2 not from receive line address.	A3L2		TA611	7th L2 after scope sync 2. See routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							header for register & checks.
X65A	0X0D	Receive data character 'FE'	The receive data not =X'FE' or ICW bits 0-3 or 5 in error	A3B2 A3P2	TA311 TA121		See routine header for regs.
X65A	0X0E	Transmit of data character '7F' completed	No level 2 or L2 not from transmit line address.	A3L2	TA611		8th L2. See routine header for register & checks.
X65A	0X0F	Receive data character '00'	No level 2 or L2 not from receive line address.	A3L2	TA611		9th L2 after scope sync 2. See routine header for register & checks.
X65A	0X10	Receive data character X'00'.	The receive data not=X'00' or ICW bits 0-3 or 5 in error	A3B2 A3P2	TA311 TA121		See routine header for regs.
X65A	0X11	Receive idle character	No level 2 or L2 not from receive line address.	A3L2	TA611		10th L2 after scope sync 2.
X65A	0X12	Receive idle character.	The receive LCD not =9 or PCF not=7.	A3P2	TA811		Reg X'14' byte 0 =L in bits 0-3 & PCF i in bits 4-7.
X65A	0X13	Receive idle character	ICW bits 0-3 or 5 are in error.	A3G2	TB011		ICW bit 0 should be on. ICW bits 1,2,3 5 should be off.
X65B	XXXX	DLC LCD B, A, 8 Test. The first two installed lines that will run in DLC mode will be wrapped and tested using the LCDs for 5,6 and 7 bit characters. The error stop checks to be made and the register contents to check are as indicated in Routine X65A header.					
		The transmitted characters are offset by 1 bit position to cause receive data characters to be offset by 1 data bit position from the transmitted characters. See notes 4 and 6 in section T2CS-NOTES for more info.					
		Transmit Data - 5 bit (LCD=B) - AA 2A 3F 00 0F 3F 3F Received Data - 5 bit (LCD=B) - flag 00 1E 1E flag					
		Transmit Data - 6 bit (LCD=A) - AA 2A 3F 00 1F 3F 3F Received Data - 6 bit (LCD=A) - flag 00 3E 3E flag					
		Transmit Data - 7 bit (LCD=8) - AA 2A 3F 00 3F 3F 3F Received Data - 7 bit (LCD=8) - flag 00 7E 7E flag					
		The routine is run in sequence of the following error codes, first in 5 bit mode, then in 6 bit mode and finally in 7 bit mode.					
X65B	0X01	Transmit of 1st pad character completed.	No level 2 or L2 not from transmit line adr.	A3L2	TA611		1st level 2 charact service interrupt after setting scope sync 2. See routine X65A header for registers & checks.
X65B	0X02	Transmit of 1st pad character completed.	The transmit PCF not=9	A3P2	TA811		Transmit PCF was se to 8 by prog in hardware setup. The CS hardware should have changed it to 9.
X65B	0X03	Transmit of 2nd pad character completed.	No level 2 or L2 was not from transmit line address.	A3L2	TA611		2nd L2 after scope sync 2. See routine X65A header for registers & checks.
X65B	0X04	Receive flag character.	No level 2 or L2 not from receive line address.	A3L2	TA611		3rd L2 after scope sync 2. See routine X65A header for registers & checks.
X65B	0X05	Receive flag character.	Receive LCD not=9 or PCF not=6 for receive line address.	A3G2 A3P2	TA111 TA121		See rtn X65A header for registers and checks.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X65B	0X06	Receive flag character	ICW bits 0-3 or 5 are in error.	A3G2	TB021		ICW bit 2 should be on(flag det). ICW bits 0,1,3 & 5 should be off.
X65B	0X07	Transmit of flag character completed.	No level 2 or L2 not from transmit line address.	A3L2	TA611		4th L2 after scope sync 2. See routine X65A header for registers & checks.
X65B	0X08	Receive data character X'00'	No level 2 or L2 not from receive line address.	A3L2	TA611		5th L2 after scope sync 2. See routine X65A header for registers & checks.
X65B	0X09	Receive data character X'00'	The LCD changed or the PCF is not=7.	A3F2	TA811		See rtn X65A note 1 for register and checks. The LCD was previously set for either 5, 6, or 7 bit mode. Reg X'16' byte 0 contains expected LCD and PCF.
X65B	0X0A	Receive data char X'00'	The received data is not=X'00' or ICW bits 0-3 or 5 are in error.	A3E2 A3P2	TA311 TA121		ICW bit 1 should be on. ICW bits 0,2,3 & 5 should be off. See routine X65A header for registers & checks.
X65B	0X0B	Transmit data character X'00' completely transmitted.	No level 2 or L2 not from transmit line address.	A3L2	TA611		6th L2 after scope sync 2. See routine X65A header for registers & checks. After this error display, the PDF is set with data character X'3F', the disable stuffer bit is set on, the LCD is set to 9 and the PCF is set to D. This should cause the transmit line to send constant DLC idle characters without causing any more L2 interrupts.
X65B	0X0C	Receive data char X'1E', X'3E', or X'7E'.	L2 interrupt did not occur or L2 not from the receive line address.	A3L2	TA611		7th L2 after scope sync 2. See Rtn X65A header for registers and checks.
X65B	0X0D	Receive data char X'1E', X'3E' or X'7E'	The received data char not as expected (X'1F' or X'3F' or X'7F') or ICW bits 0-3 or 5 are in error.	A3P2 A3N2	TA111 TA511		See routine X65A header note 1 for registers & checks. Reg X'16'= the expected ICW bits 0 through 15. ICW bit 1 should be on, bits 0,2, 3 & 5 should be off
X65B	0X0E	Receive data char X'1E', X'3E' or X'7E'.	No L2 or L2 not from the receive line address.	A3L2	TA611		8th L2. This is the 2nd time this char is received. This is actually a flag char but due to char boundry alignment on the 5,6 or 7 bit chars this is detected as a data char.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X65B	0X0F	Receive data char X'1E', X'3E' or X'7E'.	Receive PCF not=7 or the LCD changed.	A3F2	TA811		LCD & PCF should no have changed. See routine X65A header for registers and checks.
X65B	0X10	Receive data char X'1E', X'3E' or X'7E'	The received data char not as expected (X'1F' or X'3F' or X'7F') or ICW bits 0-3 or 5 are in error.	A3P2 A3N2	TA111 TA511		See routine X65A header note 1 for registers & checks. Reg X'16' contains the expected ICW bits 0 through 15. ICW bit 1 should be on,bits 0,2,3 & 5 should be off.
X65B	0X11	Receive flag character.	Level 2 interrupt did not occur or L2 was not from the receive line address.	A3L2	TA611		9th L2 after scope sync 2. See Rtn X65A header for register and checks.
X65B	0X12	Receive flag character.	The LCD not=9 or PCF not=6 for receive line address.	A3F2	TA811		See rtn X65A for registers and checks.
X65B	0X13	Receive flag character.	ICW bits 0-3 or 5 are in error	A3G2	TB011		ICW bits 0,1 & 3 should be off. ICW bits 2 and 5 (DLC flag detect) should be on. See routine X65A header.

X660 XXXX DLC DATA WRAP IN NRZI MODE. The routine header for routine X65A is valid for this routine except for note 3. All DLC lines in this routine are tested in 8 bit mode.

Transmitted Data -
- AA for clock correction.
- 2A for clock correction
- 3F a shifted flag character send with the 'disable stuffer' bit on.
- 01 after the low order bit(a one bit) is sent from this character the transmit SDF is cleared to zeros and the NRZI bit is set in the transmit ICW by doing an output X'46' with data of X'8000'. The 'last line state' bit is also set on when the one bit is being transmitted. From this point on all zero bits are serialized out of the SDF but due to the NRZI circuits alternate data bits should be transmitted.
- 00 see comments under the 01 character.
- 00 see comments under the 01 character.
- 00 see comments under the 01 character.

Received Data -
- flag recognized from the transmitted X'3F' plus the extra one bit.
- AA alternate data bits received. Note that the NRZI bit is not set on for the receive line address.
- AA alternate data bits received.
- AA alternate data bits received.
- AA alternate data bits received.
- AA alternate data bits received.

This routine tests ability of CS to transmit data in NRZI mode. The transmitted and received characters are offset to generate a predictable interrupt sequence. See notes 4 and 6 in section T2CS-NOTES for reason for this offset.

X660	0X01	Transmit of first character completed.	No level 2 character service interrupt occurred or level 2 was not from the transmit line address.	A3L2	TA611		First character service level 2 aft program set scope sync 2. See Rtn X65A header for registers and other checks.
X660	0X02	Transmit of first character completed.	The transmit PCF not=9 or LCD not =9.	A3F2	TA811		The PCF was set to 8 by the program during setup and should have been changed to 9 by CS.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X660	0X03	Transmit of 2nd character completed.	No level 2 or L2 not from transmit line address.	A3L2	TA611		2nd level 2 char-sv interrupt after program set scope sync 2. See routine X65A header for registers & checks.
X660	0X04	Receive flag character	No level 2 or L2 not from receive line address.	A3L2	TA611		3rd level 2 char-sv interrupt after program set scope sync 2. See routine X65A header for registers & checks.
X660	0X05	Receive flag character	Receive LCD not=9 or PCF not=6	A3P2 A3F2	TA111 TA811		Reg X'14' byte 0= LCD and PCF.
X660	0X06	Receive flag character	ICW bits 0-3 or 5 are in error.	A3G2	TB011		ICW bits 2(char overrun) and ICW bit 5 (flag detect) should be on. Bits 0,1 & 3 should be off.
X660	0X07	Transmit of character X'3F' completed.	No L2 interrupt occurred or L2 was not from the transmit line address.	A3L2	TA611		4th level 2 char-sv interrupt after program set scope sync 2. See routine X65A header for registers and checks.
X660	0X08	Wait for Transmit or receive line address to cause a L2 interrupt.	No L2 interrupt occurred from either transmit or receive line address.	A3L2	TA611		
X660	0X09	Receive data character X'AA'	L2 interrupt not from receive line address.	A3L2	TA611		Reg X'14' = interrupting line address.
X660	0X0A	Receive data character X'AA'	Receive LCD not=9 or PCF not=7	A3P2 A3F2	TA111 TA811		Reg X'14' byte 0 = LCD/PCF.
X660	0X0B	Receive data character X'AA'	Receive data not=X'AA' or ICW bits 0-3 or 5 are in error	A3G2 A3N2	TB021 TA511		Reg X'14' byte 1 = PDF data byte 0=ICW bits 0-7. ICW bit 1 should be on. ICW bits 0,2,3 & 5 should be off.
X660	0X0C	Wait for transmit or receive line address to cause a L2 interrupt.	No L2 interrupt occurred from either transmit or receive line address.	A3L2	TA611		
X660	0X0D	Receive data character X'AA'	The level 2 interrupt not from receive line address.	A3L2	TA611		Reg X'14' = interrupting line address.
X660	0X0E	Receive data character X'AA'	Receive LCD not=9 or PCF not=7	A3P2 A3F2	TA111 TA811		Reg X'14' byte 0 = LCD/PCF.
X660	0X0F	Receive data character X'AA'	Receive data not=X'AA' or ICW bits 0-3 or 5 in error	A3G2 A3E2 A3P2	TB021 TA311 TA511		Reg X'14' byte 1 = PDF DATA, BYTE 0= ICW bits 0-7. ICW bit 1 should be on. ICW bits 0,2,3 & 5 should be off.
X660	0X10	Wait for transmit or receive line address to cause a L2 interrupt.	No level 2 interrupt occurred from either transmit or receive line address.	A3L2	TA611		
X660	0X11	Receive data character X'AA' line address	Level 2 not from receive	A3L2	TA611		Reg X'14' = interrupting line address.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X660	0X12	Receive data character X'AA'	Receive LCD not=9 or PCF not=7	A3P2 A3P2	TA111 TA811		Reg X'14' byte 0 = LCD and PCF.
X660	0X13	Receive data character X'AA'	Receive data not=X'AA' or ICW bits 0-3 or 5 in error	A3E2 A3P2	TA511 TA121		Reg X'14' byte 1 = received data from PDF, byte 0 =ICW bits 0-7. ICW bit 1 should be on. ICW bits 0,2,3 & 5 should be off.
X660	0X14	Wait for transmit or receive line address to cause a L2 interrupt.	No L2 interrupt occurred from either the transmit or receive line address.	A3L2	TA611		
X660	0X15	Receive data character X'AA'	Level 2 not from receive line address	A3L2	TA611		Reg X'14' = interrupting line address.
X660	0X16	Receive data character X'AA'	Receive LCD not=9 or PCF not=7	A3P2 A3F2	TA111 TA811		Reg X'14' byte 0 = LCD/PCF.
X660	0X17	Receive data character X'AA'	Receive data not=X'AA' or ICW bits 0-3 or 5 in error.	A3E2 A3P2	TA511 TA121		Reg X'14' byte 1 = PDF data. ICW bit 1 should be on, ICW bits 0,2,3 & 5 should not be on.
X660	0X18	Wait for transmit or receive line address to cause L2 interrupt.	No L2 interrupt occurred from either the transmit or receive line address.	A3L2	TA611		See rtn heading for registers and check to be made.
X660	0X19	Receive data character X'AA'	Level 2 not from receive line address.	A3L2	TA611		Reg X'14' = interrupting. line address.
X660	0X1A	Receive data character X'AA'	Receive LCD not=9 or PCF not=7	A3P2 A3F2	TA111 TA811		Reg X'14' byte 0 = LCD/PCF.
X660	0X1B	Receive data character X'AA'	Receive data not=X'AA' or ICW bits 0-3 or 5 in error.	A3G2 A3N2	TB021 TA511		Reg X'14' byte 1 = received data (from PDF). ICW bit 1 (svc-req) should be on, bits 0,2,3 & 5 should be off.
X660	0X30	Transmit of data character X'00' complete.	The transmit LCD not=9 or PCF not=9.	A3F2	TA811		Reg X'14' byte 0 = LCD and PCF. This error is in a subroutine common to all transmit interrupts after initial transmit of X'00'.

X662 XXXX SYNCHRONOUS MONITOR TEST - When in synchronous monitor state (LCD=9, PCF=4 or 5) the scanner is sampling for an EBCDIC syn character, a USASCII syn character or an DLC flag character. This routine tests that when a EBCDIC syn character is detected in the receive data stream, the scanner sets the LCD to X'C', PCF to X'7' and that when a USASCII syn character is detected in the receive data stream, the scanner sets the LCD to X'D', PCF to X'7'. The first installed line set pair that will run in DLC mode is wrapped. The set mode is done before setting the scope sync 2 as the pair of lines is wrapped. Any errors detected during set mode are pretest errors and start with error code 1XXX. These error codes are near the end of the symptom index after all routine error codes.

Note 1 On all error stops in this routine the following registers are set up:
Reg X'11' = Transmit line set address
Reg X'13' = Receive line set address
Reg X'14' for errors that indicate receive data is bad or ICW bits 0-3 or 5 are in error
= What was obtained by an input X'44' from the receive line ICW
ICW bits 8-15 are the PDF and contains the receive data

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FAILD PAGE	RETRN PAGE	COMMENTS
			ICW bits 0-7 are error and control flags and are defined as follows: ICW bit 0 = Stop bit check/DLC idle detect. ICW bit 1 = Service request ICW bit 2 = Character overrun ICW bit 3 = Modem check ICW bit 4 = Receive line signal detect(this bit is ignored in this test.) ICW bit 5 = DLC flag detect/disable stuffer remember. ICW bit 6 = Program flag(this bit is ignored in this test). ICW bit 7 = PAD flag/disable stuffer(this bit is ignored on the received data ICW bits 0-15 testing) Reg X'14' for errors that indicate the LCD or PCF is bad, = The LCD in byte 0 bits 0-3, and PCF in byte 0 bits 4-7. The line is tested in 8 bit mode. The transmitted characters are offset from the received characters. See notes 4 and 6 in section T2CS-NOTES for the reason for this offset. Transmit Data AA 2A 19 19 0B 0B Receive Data 32 16			
X662	0X01	Transmit of 1st character X'AA' completed	No level 2 character service interrupt occurred from transmit line addr of L2 occurred but not from transmit line address.	A3L2		TA611	1st level 2 interru after scope sync 2. Reg X'14' = 00 if no L2 occurred; Reg X'14' equal interrupting addr in error. Reg X'11'= transmit line adr.
X662	0X02	Transmit of 1st character X'AA' completed.	Transmit PCF not=9 or LCD not = 9.	A3F2		TA611	After transmit initial, the scanner should have changed PCF to 9.
X662	0X03	Transmit of 2nd character X'2A' completed	No level 2 character service interrupt occurred from transmit line or L2 interrupt not from transmit line.	A3L2		TA611	2nd level 2 interru after scope sync 2. See comments for th 0X01 error stop cod
X662	0X04	Transmit of 1st EBCDIC syn character X'19' completed.	No level 2 interrupt or level 2 interrupt not from transmit address.	A3L2		TA611	3rd level 2 interru after scope sync 2. See comments for th 0X01 error stop cod
X662	0X05	Transmit of 1st EBCDIC syn character X'19' completed.	Transmit PCF not=9 or LCD not = 9.	A3F2		TA811	Reg X'14' byte 0 = actual transmit LCD and PCF.
X662	0X06	Receive EBCDIC syn character X'32'	No level 2 interrupt from receive line adr or interrupt from wrong line address.	A3L2		TA611	Reg X'14'= 0000 if no L2 occurred else reg X'14= line adr ICW interrupting in error. Reg X'13'=receive line address.
X662	0X07	Receive EBCDIC syn character X'32'	Receive LCD not=C or PCF not= 7.	A3F2		TA261	Reg X'14' byte 0 = LCD & PCF. The CS hardware should change LCD to X'C' when a EBCDIC SYN character is received.
X662	0X08	Receive EBCDIC syn character X'32'	ICW bits 0-3 are in error or data received in PDF is not = to X'32'.	A3B2 A3P2		TA511 TA121	ICW bit 1(svc-req) should be on and ICW bits 0, 2, & 3 should be off. See Rtn header note 1.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X662	0X09	Transmit of 2nd EBCDIC syn character X'19' completed.	No L2 interrupt occurred from transmit line or interrupt occurred from wrong line adr.	A3L2	TA611		See comment for error stop 0X01.
X662	0X0A	Transmit of 1st USACII syn character X'0B' completed.	No L2 interrupt occurred from transmit line or interrupt occurred from wrong line adr.	A3L2	TA611		See comment for error stop 0X01.
X662	0X0B	Transmit of 1st USACII syn character X'0B' completed.	Transmit LCD not=9 or PCF not=9	A3F2	TA811		Reg X'14' byte 0 contains actual LCD and PCF.
X662	0X0C	Receive USACII sync character X'16'.	No L2 interrupt occurred from receive line or interrupt occurred from wrong line adr.	A3L2	TA611		See comment for error stop 0X06.
X662	0X0D	Receive USACII syn character X'16'	Receive LCD not=D or PCF not=7.	A3F2	TA261		Reg X'14' byte 0= LCD & PCF. The CS hardware should change LCD to D when USACII syn character is received.
X662	0X0E	Receive USACII syn character X'16'	Receive line ICW bits 0-3 are in error or the received data character in the PDF is not = to X'16'.	A3N2	TA511		ICW bit 1 (svc-req) should be on, ICW bits 0, 2 and 3 should be off. See rtn heading note 1.
X663	0X01	Ensure that IPCA RPQ Bit 39 (OUT X'47' byte 1, bit 3) can be set by issuing OUT X'47' with that bit on.	IN X'47' byte 0, bit 7 failed to set.	A3G2			
X663	0X02	Ensure that IPCA RPQ Bit 39 (OUT X'47' byte 1, bit 3) can be reset by issuing OUT X'47' with that bit off.	IN X'47' byte 0, bit 7 failed to set.	A3G2			
X664	0X01	Ensure that IPCA RPQ bit 39 (OUT X'47' byte 1, bit 3) can be set by issuing OUT X'47' with that bit on.	IN X'47' byte 0, bit 7 failed to set.	A3G2			
X664	0X02	Ensure that disabling CSB under test will reset IPCA RPQ bit 39.	IN X47' byte 0, bit 7 failed to reset.	A3G2			

X665 XXXX Synchronous line sets wrap data test for IPCA RPQ. All installed line addresses that run in synchronous mode (even though they also run in start/stop mode and have been already tested in routine 50) are wrapped two at a time. The first installed synchronous line address is made the receive line and the next installed synchronous line address is made the transmit line. The test is performed on this pair of lines. When the test is completed on this pair of lines, the lines are reset and the line that was the transmit line is now made the receive line and the next installed synchronous line address is made the new transmit line. This pair of lines is then wrapped. This stepping through the lines is continued until the last installed synchronous line has been the transmit line. Then the first installed line is made the transmit line and the last installed synchronous line is made the receive line and this pair of lines is wrapped. All the installed synchronous line sets are wrapped with LCD=C and then the above procedure is repeated using LCD=D.

A set mode is executed for both the transmit and receive lines with ICW bit 27 (diagnostic wrap mode) and ICW bit 29 (sync bit clock) on. Oscillator select bits are zeros to select the first oscillator. The priority bits are set to 3. The set mode is executed before the setting of scope sync 2 as each pair of lines is wrapped. The set mode must complete successfully for the wrap to function and any errors detected during the set mode are pre-test errors and all start with error code 1XXX. These error codes are located near the end of the symptom index following the routine error codes. References to level 2 interrupts in the following error code displays are the character service level 2 interrupts that occur after scope sync 2 is set and do not include the level 2 interrupts that occurred for the set modes that occur before scope sync 2.

Note 1: For all error stops in this routine, the following registers are setup:
reg X'11' = transmit line address (as used to set ABAR)
reg X'13' = receive line address (as used to set ABAR)
reg X'14' for errors that indicate level 2 interrupt occurred from wrong address

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

and contains the line address that caused the L2 interrupt.

reg X'14' for errors that indicate the received data is bad, or indicates that ICW bits 0-7 are in error and contains ICW bits 0-15 from the receive line ICW obtained by executing Input X'44'. ICW bits 8-15 (the PDF) contain the received data. ICW bits 0-7 are check and control flags and are always expected to be set as follows:

- ICW bit 0 = Stop bit check and should be off
- ICW bit 1 = Service request and should be on
- ICW bit 2 = Character overrun/underrun and should be off
- ICW bit 3 = Modem check and should be off
- ICW bit 4 = Receive line signal detector. This bit is ignored in this test.
- ICW bit 5 = Reserved bit. This bit is ignored in this test.
- ICW bit 6 = Program flag. This bit is ignored in this test.
- ICW bit 7 = Pad flag. This bit is ignored in this test.

reg X'16' for errors that indicate the received data is bad, and contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'.

Note 2: Checks to be made on all error stops:

a. Check LCD of failing line address. If LCD=F, a feedback check has occurred. If the configuration data set (CDS) erroneously indicates a line set is installed that will run in synchronous mode, a feedback check will occur.

b. You may use the continue function (except on pre-test errors starting with 1) to continue from this error to (1) see if just this line address is failing, (2) see if all line addreses in this LIB are failing, or (3) see if all synchronous lines are failing. You may get additional error stops on the same line pair being wrapped so you may have to use the continue function multiple times. If only one line set is failing, or a pair of even/odd addresses, then the line set card is probably bad. If all addresses fail in one LIB, the LIB's bit clock control card may be bad, or the terminators may be bad. If all synchronous line addresses fail, the scanner cards may be bad. If the line addresses are the type that run in both synchronous and start/stop mode, and if they run successfully in routine X652, then suspect LCD=C or LCD=D circuitry or the sync bit clock control line. Reference LIB card positions in section C-xxx in FETMM (LIBs and line sets) because card locations vary in location according to LIB types.

The transmitted characters are offset by 1 data bit to cause receive data characters to be offset by 1 data bit from transmitted characters. See notes 4 and 6 in section T2CS-NOTES for more information.

Transmit Data - 55 55 FF FF FC 00 (EBCDIC)
55 55 E9 E9 FC 00 (SDLC-7)
55 55 16 16 7C 00 (SBT)

Receive Data - FF F9 01 (EBCDIC)
53 79 01 (SDLC-7)
2C 38 01 (SBT)

The routine is run in the sequence of the following error codes.

X665	0X01	Transmit of 1st PAD completed.	No level 2 interrupt occurred from transmit line address.	A3L2	TA611	B-310 B-260	1st level 2 char-service interrupt after program set scope sync 2. See notes 1 & 2 at heading of this routine for register and checks to make.
X665	0X02	Transmit of 1st PAD completed.	Level 2 interrupt not from transmit line adr.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks to make.
X665	0X03	Transmit PCF changes from 8 to 9.	Transmit PCF not = 9 or LCD changed.	A3F2	TA811	B-080	Transmit PCF was se to 8 by program during hardware setup. The scanner hardware should have changed the PCF to 9 and should now be in process of transmitting 2nd pad character. The transmit PDF is set to the 1st SYN character after

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							this error display. See notes 1 & 2 in heading of this routine for registers and checks to make.
X665	0X04	Transmit of 2nd PAD completed.	No level 2 interrupt occurred from transmit line adr.	A3L2	TA611	B-310 B-260	2nd L2 after scope sync 2. See notes 1 and 2 in heading of this routine for registers and checks to make.
X665	0X05	Transmit of 2nd PAD completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks to make. After this error display, the transmit PDF is set with the 2nd SYN character.
X665	0X06	Transmit of 1st SYN completed.	No level 2 interrupt occurred from transmit line address.	A3L2	TA611	B-310 B-260	3rd L2 after scope sync 2. See notes 1 and 2 in the rtn heading for registers and checks to make.
X665	0X07	Transmit of 1st SYN completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks to make. After this error display, the transmit PDF is set to character X'A0' to be transmitted next. Should now be in process of transmitting 2nd SYN character.
X665	0X08	Receive 1st SYN.	Receive line PCF not = 7 or LCD changed.	A3F2	TA811	B-080	Receive line PCF wa initially set to 5. When the 1st SYN character is received and recognized the hardware should changed the receive PCF=7. Note: this setting of PCF=7 from PCF=5 does not cause a level 2 interrupt. See notes 1 & 2 in heading of this routine for registers and checks to make.
X665	0X09	Receive 2nd SYN.	No level 2 interrupt occurred from receive line address.	A3L2	TA611	B-310 B-420	4th level 2 (1st fr receive line addr) after scope sync 2. See notes 1 & 2 in heading of this routine for registers and checks to make.
X665	0X0A	Receive 2nd SYN.	Level 2 interrupt not from receive line adr.	A3L2	TA611	B-300	See rtn heading notes 1 and 2

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							for registers and checks to make.
X665	0X0B	Receive 2nd SYN.	Received data in PDF not a SYN character, or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-420	Received data in PD should be X'32' if LCD=C or X'16' if LCD=D. See notes 1 & 2 in heading of this routine for registers, ICW bits 0-7, and checks to make.
X665	0X0C	Transmit of 2nd SYN completed.	No level 2 interrupt occurred for transmit line address.	A3L2	TA611	B-310 B-260	5th level 2 (4th fr transmit line adr) after scope sync 2. See notes 1 & 2 in heading of this routine for registers and checks to make.
X665	0X0D	Transmit of 2nd SYN completed.	Level 2 interrupt not from transmit line adr.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks to make. After this error display, the transmit PDF is set to the next character to transmit.
X665	0X0E	Second Receive character.	No level 2 interrupt occurred from the receive addr.	A3L2	TA611	B-310 B-420	6th level 2 interru (2nd from receive address) after scope sync 2. See notes 1 & 2 in heading of this routine for registers and checks to make.
X665	0X0F	Second Receive character.	Level 2 interrupt not from receive line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks to make.
X665	0X10	Second Receive character .	Received data in PDF not = X'A0', or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131	B-420	See rtn heading notes 1 and 2 for registers, ICW bits 0-7, and checks to make.
X665	0X11	Transmit of second character completed.	No level 2 occurred for transmit line address.	A3L2	TA611		7th level 2(5th fro transmit line addr). See notes 1 & 2 in heading of this routine for registers and checks.
X665	0X12	Transmit of second character completed.	Level 2 not from transmit line address.	A3L2	TA611		See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit PDF is set to X'80' as the next character to transmit. Should now be in process of transmitting the character X'7F'.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X665	0X27	Receive character X'01'.	No level 2 occurred from receive line address.	A3L2	TA611		12th level 2(7th fr receive line addr). See notes 1 and 2 in heading of this routine for registers and check Last I2 for receive.
X665	0X28	Receive character X'01'.	Level 2 not from receive line address.	A3L2	TA611		See rtn heading notes 1 and 2 for registers and checks.
X665	0X29	Receive character X'01'.	Received data in PDF not = X'11' or ICW bits 0-3 in error.	A3E2 A3P2	TA311 TA131		See rtn heading notes 1 and 2 for registers, ICW bits 0-7, and checks. After this error display, the receive PCF is set to 0 so no further level 2 interrupts should occur from the receive line addr.
X665	0X2A	Transmit of X'00' completed and transmit turn-around.	No level 2 occurred from transmit line address.	A3L2	TA611		13th L2 (10th from transmit addr) and is the last L2. See notes 1 & 2 in heading of this routine for registers and checks. At this time the transmit PCF should have turned around to PCF=5.
X665	0X2B	Transmit of X'00' completed and transmit turn-around.	Level 2 not from transmit line address.	A3L2	TA611		See rtn heading notes 1 and 2 for registers and checks. PCF should be turned around to PCF=5.
X665	0X2C	Transmit turn-around.	Transmit PCF did not turn around to PCF=5 or LCD changed.	A3F2	TA811		After previous transmit level 2 (see error 0X26) transmit PCF was set to X'D' to cause a turn-around. The hardware should have completed the transmission of the character X'00' and then set PCF=5. See notes 1 & 2 in heading of this routine for registers and checks.

X666 XXXX Stop bit error test for all start/stop lines. All start/stop line addresses are tested to see if a stop bit check can be detected. The lines are used in pairs with one line made the receive line. This is the line that should detect the stop bit check. The receive line is tested with LCD's of 0, 2, 4, 5, 6, and 7. The transmit line always is setup with LCD=7. A PAD character of X'03' is transmitted followed by the character X'02'. When the X'02' is being transmitted, the program loops checking transmit SDF bits 8 and 9 for 00, then the transmit SDF is set to X'180'. This should cause the transmit line to send extra bits of zero and cause the receive line to get a stop bit check. The sequence of operation in this routine is:

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		a. Reset scanner. b. Enable scanner. c. Set display bit in the receive lines ICW. d. Set receive line address in receive mode. e. Set mode on the transmit line address. f. Set transmit line SDF=X'03'.(2 bit times of pad) g. Set transmit line PDF=X'02'. h. Set transmit PCF=8. i. Set scope sync 2. j. Wait for level 2 interrupt on transmit PAD character completed. k. Wait for transmit SDF bits 8-9=0. l. Set transmit SDF=X'180'. m. Wait for receive line address character service level 2 interrupt. n. Check that 'stop bit check' bit is on in receive lines ICW. o. Reset the 'stop bit check' bit. p. Check that the bit reset. The above sequence is done for LCD's 0, 2, 3, 4, 6, and 7 on the receive line address and then the next start/stop line is setup and the whole test is run again. All lines use priority 3 and oscillator select 0. Note 1. The following registers are setup for all errors displayed in this routine: Reg X'11' = Transmit line adr. Reg X'13' = Receive line adr; the adr that should detect the stop bit errors. Reg X'16' = The LCD being tested on the receive line. (in byte 1, bits 0-3.) Note 2. On all error stops, the LCD's should be checked for LCD=F (feedback check). You can use the continue function (except for pre-test errors during the set modes) to continue from the error stop to see if (1) only one line set, (2) the whole LIB, or (3) all start/stop line sets in the scanner are failing, and if the failure is for one LCD setting or all LCD settings. If only one line or one pair of lines is failing, suspect the line set card as being bad. If all lines on a LIB fail, check LIB cards and terminators. If all of lines on scanner fail, or if only one LCD setting fails, suspect the scanner cards. Reference LIB card positions in section C-xxx in FETMM (LIBs and line sets) because card locations vary according to LIB type. Other possible failures are that oscillator 0 is failing or oscillator select is not working.				
X666	0X01	Transmit of PAD completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	Reg X'11' = transmit line addr expected to cause L2 interrupt. See notes 1 & 2 in heading of this routine for other registers & checks to be made.
X666	0X02	Transmit of PAD completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	Reg X'11' = transmit line addr expected to cause L2 interrupt. Reg X'14' = line adr that caused the L2 interrupt. See notes 1 & 2 in heading of this routine for other registers & checks to be made.
X666	0X03	Shifting of transmit SDF.	Transmit SDF bits 8 & 9 did not get zeros shifted into them within 200 milliseconds.	A3L2	TA611	B-480	See rtn heading notes 1 and 2 for registers and checks. If this failure occurs suggest you run routines X650 & X652 to test diagnostic wrap.
X666	0X04	Received character.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	Reg X'13' = receive line addr expected to cause L2 interrupt. See notes 1 & 2 in heading of this routine

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							for other registers and checks.
X666	0X05	Received character.	Level 2 interrupt not from receive line address.	A3L2	TA611	B-300	Reg X'13' = receive line addr expected to cause the L2 interrupt. Reg X'14'=line adr that caused the L2. See notes 1&2 in heading of this routine for other registers & checks.
X666	0X06	Stop bit check bit on.	Stop bit check (ICW bit 0) not on.	A3P2	TA121	B-140	Stop bit check should be on in the receive line ICW. See notes 1 & in heading of this routine for registers & checks.
X666	0X07	Stop bit check bit off.	Stop bit check did not reset.	A3P2	TA121	B-180	Program attempted to reset the stop bit check but it did not reset. See notes 1 & 2 in heading of this routine for registers and checks.
X668	XXXX	Pad flag test for start/stop lines. Check that while the PAD flag (ICW bit 7) is on and the transmit PDF=X'FF', no characters are received. Then turn the PAD flag off and check that characters can be received. A pair of lines are used in each run of the test with one line being the receive line and the other the transmit line. All start/stop lines are tested with LCD=2, priority 3, and oscillator select 0. A set mode is executed for both the receive and the transmit line. The receive line is set in receive mode, the transmit SDF is set to X'FF', the transmit PDF is set to X'05', the transmit PCF is set to X'8', and then scope sync 2 is set and the rest of the test runs in the same sequence as the following error codes. As each test is finished, the next start/stop line address is used with the previous transmit line and the test is run again. This continues until all installed start/stop lines in the scanner under test are run in both transmit and receive mode. Note 1: The following registers are setup for error displays: Reg X'11'=Transmit line (ICW) address as used to set ABAR. Reg X'13'=Receive line (ICW) address as used to set ABAR. Reg X'14' for errors indicating level 2 interrupts from wrong address = the line address of the line that caused the level 2. Reg X'14' for unexpected received data in the PDF or for errors that indicate ICW bits 0-7 are in error. Contains ICW bits 0-15 from the receive line ICW obtained by an Input X'44'. Reg X'16'=Expected receive lines ICW bits 0-15 for receive data PDF errors, or ICW bits 0-7 error. The receive ICW bits 8-15 are the PDF, and byte 1 of both reg X'14' and reg X'16' should always be equal on all received data tests. ICW bits 0-7 are normally expected to = X'4?' in reg X'14' (service request bit on, 'receive line signal detect' bit ignored, all other bits off). For telegraph LIB's, ICW bits 0-7 are not checked since an echo check may occur setting modem check if no external current loop is present. Note 2: For all error stops, the LCD's should be examined for a feedback check; LCD=X'F'. You can use the continue function (except for set mode pre-test errors) to see if only this line address, a pair of line addresses, all lines in a LIB, or all lines in the scanner are failing. If only one line, or a pair of lines is failing, suspect the line set card. If all lines in a LIB are failing, suspect the LIB bit clock control card or line terminators. If all lines in the scanner fail, suspect scanner cards or first oscillator card. See LIB card positions in section C-xxx in FETMM (LIBs and line sets) because they vary according to LIB type.						
X668	0X01	First PAD character completely transmitted.	No level 2 interrupt occurred. Expected from transmit line	A3L2	TA611	B-310 B-260	See rtn heading notes 1 and 2

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			address.				for registers and checks. This should be 1st L2 interrupt after scope sync 2.
X668	0X02	First PAD completely transmitted.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit line's pad flag is turned on and the PDF is set to X'FF'. X'05' is being transmitted.
X668	0X03	Receive first character of X'05'.	No level 2 interrupt occurred. L2 interrupt expected from receive line address.	A3L2	TA611	B-310 B-420	See rtn heading notes 1 and 2 for registers and checks. This should be the 2nd level 2 interrupt (1st from receive line adr) after scope sync 2.
X668	0X04	Receive first character of X'05'.	Level 2 interrupt not from receive line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks.
X668	0X05	Receive first character of X'05'.	Received data in PDF not = X'05', or ICW bits 0-7 in error.	A3E2 A3P2	TA311 TA131	B-420	See rtn heading notes 1 and 2 for registers, ICW bits 0-7, & checks.
X668	0X06	Transmit of X'05' completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	See rtn heading notes 1 and 2 for registers & checks. This should be 3rd level 2 interrupt, 2nd for transmit line address.
X668	0X07	Transmit of X'05' completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit line's pad flag is turned on and the PDF is set to X'FF'. Should now be transmitting the pad character setup after error display 0X02 and receive line should not be receiving any data bits.
X668	0X08	Transmit of 2nd PAD completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	See rtn heading notes 1 and 2 for registers and checks. This is the 4th L2 (3rd from transmit line address).
X668	0X09	Transmit of 2nd PAD completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300 B-420	See rtn heading notes 1 and 2

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETRN PAGE	COMMENTS
							for registers and checks. If the L2 interrupt was cause by the receive line ad suspect that the receive line was receiving data instead of the pad character that was supposed to be transmitted. After this error display, the pad flag is turned off and the transmit PDF is set to X'0E' as the next character to transmit. A pad character should now be in the process of transmission.
X668	0X0A	Pad flag reset.	Pad flag did not reset in transmit ICW.	A3E2	TA311	B-180	See rtn heading notes 1 and 2 for registers and checks.
X668	0X0B	Transmit of 3rd PAD completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	See rtn heading notes 1 and 2 for registers and checks. This should be the 5th level 2 interrupt (4th from transmit line adr).
X668	0X0C	Transmit of 3rd PAD completed.	Level 2 interrupt from wrong address. Expected a L2 from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit pad flag is turned on and the PDF is set to X'FF'. Should now be in the process of transmitting character X'0E'.
X668	0X0F	Receive character X'0E'.	No level 2 interrupt occurred. Should have level 2 interrupt from receive line address.	A3L2	TA611	B-310 B-420	See rtn heading notes 1 and 2 for registers and checks. This should be the 6th level 2 interru (the 2nd from receive line adr).
X668	0X10	Receive character X'0E'.	Level 2 interrupt not from receive line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks. If the level 2 interrupt was caused by the transmit line addr the transmit lines ICW may have failed to recognize the reset of the pad flag after error display 0X09.
X668	0X11	Receive character X'0E'.	Received data in PDF not X'0E', or ICW bits 0-7 in error.	A3E2 A3P2	TA311 TA131	B-420	See rtn heading notes 1 and 2 for registers, ICW

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							bits 0-7, and checks.
X669	XXXX	Scanner priority test. This routine tests that the priority between multiple scanners is correct. If level 2 interrupts are pending from multiple scanners at the same time then the 1st scanner should have the highest priority, the 2nd scanner the next priority, etc. In this test the 1st ICW of each installed scanner is setup to have a level 2 interrupt pending by setting ICW bit 41. Then the program checks that the scanners interrupt in the correct sequence. The test is run using priority select 3 for all tested scanners. This test is not run if only one scanner is installed. If this test detects failures you should make sure that all previous test routines have run on all scanners before you use this routine to try to isolate the problem.					
X669	0X01	Scanner priority test.	Did not get level 2 interrupt after all scanners were set to cause a level 2 interrupt.	A3L2	TA611	B-300	See routine heading Reg X'13'=line adr L2 is expected from
X669	0X02	Scanner priority test. Scanner 1 has highest priority, scanner 2 next, scanner 3 next, and scanner 4 the lowest priority.	Level 2 interrupt occurred from wrong adr. Reg X'13'= line adr expected to cause L2 interrupt. Reg X'14'= line address causing L2.	A3L2	TA611	B-300	See routine heading
X66E	XXXX	Character overrun and underrun test for start/stop lines. Check that character overruns on the receive line and character underruns on the transmit line can be detected and reset. All start/stop lines are tested except for telegraph lines which cause an echo check if no external current source is connected to the line. The echo check sets modem check that suppresses the setting of service request. Overrun cannot be set when the service request bit is off. A pair of start/stop lines are used in each run of the test with one line made the receive line and one the transmit line. As each test finishes, the next start/stop line is made the transmit line and the last transmit line is made the receive line. This continues until all start/stop lines have been both a transmit and a receive line in the scanner under test. All lines are tested with LCD=2, priority=3, and oscillator select=0. A set mode is executed for the receive line and then the transmit line. The receive line is set in receive mode. The transmit line's SDF is set to X'FF', PDF to X'0A', and PCF=X'8'. Scope sync 2 is set, then the routine runs in the sequence of the following error display codes. The scanner is reset then enabled and the above test is run on the next line. This continues until all start/stop lines except telegraph have been tested. Note 1: The following registers are setup for error displays: Reg X'11'=Transmit line (ICW) address as used to set ABAR. Reg X'13'=Receive line (ICW) address as used to set ABAR. Reg X'14' for errors indicating level 2 interrupts from wrong adr and contains the address of the line that caused the level 2 interrupt. Reg X'14' for unexpected received data in the PDF or for errors that indicate ICW bits 0-7 are in error. Contains ICW bits 0-15 from the receive line ICW obtained by an Input X'44'. Reg X'16'=Expected receive lines ICW bits 0-15 for received data, PDF errors, or ICW bits 0-7 error. The receive ICW bits 8-15 are the PDF, and byte 1 of both reg X'14' and reg X'16' should always be equal on all received data tests. ICW bits 0-7 are expected to be = to X'42' in reg X'14' (service request on, 'receive line signal detect' ignored, all other bits off). The exception to ICW bits 0-7 occurs when an overrun is created. The service request bit (ICW bit 1) should be off and character overrun bit (ICW bit 2) should be on. Note 2: For all error stops, the LCD's should be examined for a feedback check; LCD=X'F'. You can use the continue function (except for set mode pre-test errors) to see if only this line address, a pair of line addresses, all lines in a LIB, or all lines in the scanner are failing. If only one line, or a pair of lines, is failing, suspect the line set card. If all lines in a LIB are failing, suspect the LIB bit clock control card or line terminators. If all lines in the scanner fail, suspect the scanner cards or first oscillator card. See LIB card positions in section C-xxx (LIBs and line sets) because they vary according to LIB type.					
X66E	0X01	Completed transmit of PAD character.	No level 2 interrupt occurred. Should have had a L2 interrupt from the transmit line address.	A3L2	TA611	B-310 B-260	See rtn heading notes 1 and 2 for registers and checks. This should be the 1st L2 interrupt after program set scope sync 2.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETNM PAGE	COMMENTS
X66E	0X02	Completed transmit of PAD character.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks.
X66E	0X03	Completed transmit of PAD character.	Transmit line PCF did not change to 9.	A3F2	TA811	B-080	See rtn heading notes 1 and 2 for registers and checks. Program sets transmit PCF=8 during hardware setup. Hardware should have changed the PCF to 9 as 1st character is transmitted. After this error display, the transmit PDF is set to X'01' as the next character to be transmitted. Should now be in process of transmitting char X'0A'.
X66E	0X04	Receive character X'0A'.	No level 2 interrupt occurred.	A3L2	TA611	B-490	See notes 1 & 2 in heading of this routine for registers and checks. This should be the 2nd level 2 interrupt (1st from receive line address).
X66E	0X05	Receive character X'0A'.	Level 2 interrupt not from receive line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks.
X66E	0X06	Receive character X'0A'.	Received data in PDF not = X'0A', or ICW bits 0-7 in error.	A3E2 A3P2	TA311 TA131	B-490	See rtn heading notes 1 and 2 for registers and checks. Service- request bit is not reset after this error display, so next received character should cause a character overrun.
X66E	0X07	Completed transmission of X'0A'.	No level 2 interrupt occurred. Should have had a L2 interrupt from transmit line address.	A3L2	TA611	B-310 B-260	See rtn heading notes 1 and 2 for registers and checks This should be the 3rd L2 interrupt interrupt (2nd from transmit line address).
X66E	0X08	Completed transmission of X'0A'.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks. After this error display, the transmit PDF is set to X'0E' as the next charact to be transmitted. Service request bit

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							is not reset so the next transmit level 2 interrupt should set the character underrun bit. Should now be in the process of transmitting the character X'01'.
X66E	0X09	Receive character X'01' and get character overrun.	No level 2 interrupt occurred. Should have a L2 interrupt from receive line address.	A3L2	TA611	B-490	See rtn heading notes 1 and 2 for registers and checks. This should be 4th L2 (2nd from receive line adr). Check reg X'44'; ICW bit 2 (character overrun bit) should be on in receive line, ICW bit 1 (service request) should be off and PDF should contain X'01'. If you (1) display reg X'40', (2) store the receive line adr and (3) display reg X'44' (ICW bits 0-15), the PDF should now = X'0E' since the transmit line is still sending characters X'0E' and the receive line should be receiving the character and setting overrun.
X66E	0X0A	Receive character X'01' and get character overrun.	Level 2 interrupt not from receive line adr.	A3L2	TA611	B-300	See comments on previous error 0X09
X66E	0X0B	Received character X'01' & get character overrun.	Character overrun (ICW bit 2) not on, or service request (ICW bit 1) is on, or PDF (ICW bits 8-15) not = X'01'.	A3P2	TA611	B-490 B-140	Rec ICW bit 2 should be on. See error stop code 0X09. Reg X'14'= th receive ICW bits 0-15 obtained via a input X'44'.
X66E	0X0C	Reset of ICW bit 2.	ICW bit 2 (character overrun) did not reset.	A3P2	TA611	B-180	See rtn heading notes 1 and 2 for registers and checks.
X66E	0X0D	Transmit of X'01' completed and transmit underrun.	No level 2 interrupt occurred. Should have had a L2 interrupt from transmit line address.	A3L2	TA611	B-310 B-260	See rtn heading notes 1 and 2 for registers and checks. This should be 5th level 2 interrupt (3rd from transmit)
X66E	0X0E	Transmit of X'01' completed and transmit underrun.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading notes 1 and 2 for registers and checks.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X66E	0X0F	Transmit underrun.	Underrun (ICW bit 2) not on in transmit lines ICW. (Should be on.)	A3P2	TA121	B-310 B-140	See rtn heading notes 1 and 2 for registers and checks. After error display 0X08 on last transmit character service L2, the service request bit was not reset so when this transmit level 2 interrupt occurred, the character underrun bit should have been set on by hardware.
X66E	0X10	Reset of transmit underrun.	Underrun bit (ICW bit 2) did not reset in transmit lines ICW.	A3P2	TA121	B-180	

X672 XXXX Character overrun and underrun test for synchronous lines. All synchronous lines are checked to ensure that character overrun can be detected on receive lines and character underrun can be detected on transmit lines. All lines are tested with LCD=C, priority=3, and oscillator select=0. Each pair of lines is setup by (1) setting the display bit in the receive line, (2) executing set mode on the receive line, (3) setting the receive line PCF=5, (4) executing set mode on the transmit line, (5) setting transmit SDF and PDF to X'55', (6) setting transmit PCF=8, and (7) setting scope sync 2. The rest of the test is run in the same sequence as the error codes that follow. When the test is finished on a pair of lines, the scanner is disabled then enabled, the next synchronous line address is made the new transmit line and the last transmit line is made the new receive line and the whole test is run again. This is continued until all synchronous lines have been tested both as transmit and receive lines.

Note 1: The following registers are setup for error displays:
Reg X'11'=Transmit line (ICW) address as used to set ABAR.
Reg X'13'=Receive line (ICW) address as used to set ABAR.
Reg X'14' for errors indicating level 2 interrupts from wrong adr and contains the address of the line that caused the level 2 interrupt.
Reg X'14' for unexpected received data in the PDF or for errors that indicate that ICW bits 0-7 are in error. Contains ICW bits 0-15 from the receive line ICW obtained by an Input X'44'.
Reg X'16'=Expected receive lines ICW bits 0-15 for received data, PDF errors, or ICW bits 0-7 error. The receive ICW bits 8-15 are the PDF, and byte 1 of both reg X'14' and reg X'16' should always be equal on all received data tests. ICW bits 0-7 are expected to be: bit 1(svc-req) on, bits 0,2,3,5,6 & 7 off; bit 4 ignored. The exception to ICW bits 0-7 being as above is when an overrun is created. The service request bit (ICW bit 1) should be off and character overrun bit (ICW bit 2) should be on.

Note 2: For all error stops, the LCD's should be examined for a feedback check; LCD=X'F'. You can use the continue function (except for set mode pre-test errors) to see if only this line address, a pair of line addresses, all lines in a LIB, or all lines in the scanner are failing. If only one line, or a pair of lines, is failing, suspect the line set card. If all lines in a LIB are failing, suspect the LIB bit clock control card or line terminators. If all lines in the scanner fail, suspect the scanner cards or first oscillator card. See LIB card positions in in section C-XXX in FETMM (LIBs and line sets) because they vary according to LIB type.

Note 3: See note 6 in section T2CS-Notes for explanation for the shifted SYN and data chars.

X672	0X01	Transmit 1st pad (X'55') completed.	No level 2 interrupt occurred.	A3L2	TA611		See notes 1 & 2 in heading of this routine for registers and checks. 1st level 2 (from transmit) after scope sync 2.
X672	0X02	Transmit 1st pad (X'55') completed.	Level 2 not from transmit line adr.	A3L2	TA611		See rtn heading heading of

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							this routine for registers & checks.
X672	0X03	Transmit PCF went to 9.	Transmit PCF did not go to 9.	A3F2	TA811		See rtn heading heading of this routine for registers and checks. Program set PCF=8 in hardware setup and hardware should have changed the PCF to 9. After this error display, the transmit PDF is set to X'19' (shifted sync char) and service request is reset.
X672	0X04	Transmit 2nd pad (X'55') completed.	No level 2 interrupt occurred.	A3L2	TA611		See rtn heading heading of this routine for registers and checks. 2nd level 2 (2nd from transmit) after scope sync 2.
X672	0X05	Transmit 2nd pad (X'55') completed.	Level 2 not from transmit line adr.	A3L2	TA611		See notes 1 & 2 in heading of this routine for registers and checks. After this error display, the transmit PDF is set with the 2nd shifted sync char (X'19') and service request is reset. Should now be in process of transmitting the 1st sync character.
X672	0X06	Transmit 1st sync (X'19') completed.	No level 2 interrupt occurred.	A3L2	TA611		See rtn heading heading of this routine for registers and checks. 3rd level 2 (3rd from transmit).
X672	0X07	Transmit 1st sync (X'19') completed.	Level 2 not from transmit line adr.	A3L2	TA611		See notes 1 & 2 in heading of this routine for registers & checks. After this error display, the transmit lines PDF is set to character X'50' and service request is reset. Should now be in process of transmitting the 2nd sync character.
X672	0X08	Receive line detected 1st SYN.	Receive line's PCF not =7.	A3F2	TA811	B-080	Ther rec addr PCF was set to 5 by the program during

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							hardware setup but the 1st SYN character should have been received and detected by the hardware and caused the PCF to be changed to 7. Note: no level 2 interrupt should result from changing PCF=5 to PCF=7. See notes 1 & 2 in heading of this routine for registers & checks.
X672	0X09	Receive line received 2nd SYN.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-420	See rtn heading heading of this routine for registers and checks. 4th level 2 interrupt (1st from receive).
X672	0X0A	Receive line received 2nd SYN.	Level 2 interrupt not from receive line address.	A3L2	TA611	B-300	See rtn heading heading of this routine for registers & checks.
X672	0X0B	Receive line received 2nd SYN.	Received data in receive line PDF not a SYN character (X'32'), or ICW bits 0-7 in error.	A3E2 A3P2	TA311 TA131	B-240	See rtn heading notes 1 and 2 for registers, ICW bits 0-7 and checks to make. Service request bit is not set off in the receive line ICW so the next receive line level 2 interrupt should indicate character overrun.
X672	0X0C	Transmit of 2nd SYN completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	See rtn heading heading of this routine for registers and checks. 5th level 2 interrupt (4th from transmit)
X672	0X0D	Transmit of 2nd SYN completed.	Level 2 interrupt not from transmit line address.	A3L2	TA611	B-300	See rtn heading heading of this routine for registers and checks. After this error display, the transmit line's PDF is set to X'00'. The service request bit is not reset. On the next level 2 interrupt for the transmit line address a character underrun error should be indicated. Should now be in the process of transmitting the char X'50'.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X672	0X0E	Receive character X'A0' and get character overrun.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-420	See rtn heading heading of this routine for registers and checks. Reg X'44' contains the receive line's ICW bits 0-15. ICW bits 8-15 are the PDF and should=X'A0'. ICW bit 2 (character overrun) should be on since service request (ICW bit 1) was not reset on the last receive line level 2 interrupt. ICW bit 1 (service request) should be off since hardware should turn it off when it turns on ICW bit 2. This is the 6th level 2 interrupt (2nd from receive).
X672	0X0F	Receive character X'A0' and get character overrun.	Level 2 interrupt not from receive line adr.	A3L2	TA611	B-300	See notes 1 & 2 in heading of this routine for registers and checks. Reg X'44' contains the receive line's ICW bits 0-15. ICW bits 8-15 are the PDF and should=X'A0'. ICW bit 2 (character overrun) should be on since service request (ICW bit 1) was not reset on the last receive line level 2 interrupt. ICW bit 1 (service request) should be off since hardware should turn it off when it turns on ICW bit 2.
X672	0X10	Receive character X'A0' and get character overrun.	Character overrun (ICW bit 2) is not on, or service request (ICW bit 1) is on, or PDF not = X'A0' in receive line's ICW.	A3P2	TA121	B-420 B-140	See comments under error 0X0F.
X672	0X11	Character overrun reset.	Character overrun (ICW bit 2) did not reset.	A3P2	TA121	B-180	Program attempted to reset character overrun and then checked to make sure it was off. See notes 1 & 2 in heading of this routine for registers & checks.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X672	0X12	Transmit of X'50' complete and character underrun.	No level 2 interrupt occurred.	A3L2	TA611		See rtn heading notes 1 and 2 for registers and checks. Should have transmit line's ICW bit 2 on (underrun) since the service request bit was not reset on the last transmit level 2 interrupt. 7th level 2 (5th from transmit).
X672	0X13	Transmit of X'50' completed and character underrun.	Level 2 not from transmit line address.	A3L2	TA611		See notes 1 & 2 in the heading of this routine for registers and checks. The transmit line's ICW should have the character underrun bit on (ICW bit 2) since the service request bit was not reset on the last transmit level 2 interrupt.
X672	0X14	Transmit of X'50' completed and character underrun.	The character underrun bit (ICW bit 2) is not on but should be.	A3P2	TA121		See notes 1 & 2 in notes 1 and 2 for registers & checks. The transmit line's ICW should have the character underrun bit on (ICW bit 1) since the service request bit was not reset on the last transmit level 2 interrupt.
X672	0X15	Reset underrun.	The character underrun bit did not reset.	A3P2	TA121	B-180	See notes 1 & 2 in heading of this routine for registers and checks. The program attempted to reset the character underrun bit in the transmit ICW and then checked and found the bit was still on.
X675	XXXX	Force level 1 check test. Checks that an Output X'43' with byte 0, bit 0 and byte 1, bit 5 on forces the check bits on in the scanner check register (Input X'43'). Then checks that an Output X'43' with byte 0, bit 1 and byte 1, bit 5 on resets the check bits. The scanner is disabled ('CSB disable' latch is set) then enabled ('CSB disable' latch turned off). Then ABAR is set with an Output X'40', scope sync 2 is set and an Output X'43' is done with byte 0, bit 0 and byte 1, bit 5 on. The rest of the test is run in the same sequence as the following error codes.					
X675	0X01	Scanner check register bits on.	All check bits not on.	A3C2	TB131	B-170 B-130	Reg X'14'= the scanner check register bits obtained by an Input X'43'. Byte 0, bit 0-7 and byte 1, bits 0-3 should all be on. Note: level 1

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							adapter checks were masked off so the normal level 1 adapter check that should occur is blocked at this time. Reg X'11'= line adr of scanner under test as used to set ABAR. After thi error display, ABAR is set again and another Output X'43' executed with byte 0, bit 1 and byte 1, bit 5 on to reset the scanner check reg bits.
X675	0X02	Scanner check register reset.	All check bits not reset.	A3C2	TB131	B-140 B-130	All scanner check r bits should be rese Reg X'14' contains the scanner check reg obtained by an Input X'43'. Reg X'11'= line addr of scanner under test set in ABAR. After this error display, Output X'43' is executed again to set the scanner check reg bits on. Then adapter level 1 interrupts are unmasked and a check is made that a level 1 actually occurred.
X675	0X03	Scanner check register causes level 1 interrupt.	No level 1 interrupt occurred.	A3C2	TB131	B-130	A level 1 interrupt should have occurre for scanner under test. Reg X'11'= line addr set in ABAR.
X675	0X04	Scanner under test caused the L1 interrupt.	The Scanner under test was not the scanner that caused the level 1 interrupt.	A3C2	TB131	B-300	Reg X'14'=line addr causing the L1 interrupt. Reg X'11' equals line Addr of scanne under test.
X678	XXXX	Modem error bit test. This routine tests that the modem error bit (ICW bit 3) is set according to the modem interface lines of Data Set Ready (DSR) and/or Clear To Send (CTS). Only one error stop can occur in this routine with Register X'15' indicating the failure. If Reg X'15'=0001 then the error is that the modem check bit did not come on with DSR off and a PCF of 5, 7, 8, 9, A, B, C, or D. If Reg. X'15'=0002 the error is that the modem error bit is not on with CTS off and a PCF of 9, A, B, or D. Reg X'13' contains the contents of the display reg obtained by an input X'46' with bit 0.0 being CTS and 0.2=DSR. Reg. X'11' contains line (ICW) address of line under test. Reg. X'14' contains ICW bits 0-15 with bit 0.3 being the modem check bit. Reg. X'45' contains LCD and PCF with bits 0.4 - 0.7 being PCF now in ICW. Reg. X'16' bits 1.0 - 1.3 = LCD in use and bits 1.4 - 1.7 = PCF that was used. PCF now in ICW may be different than PCF that was used and this may be normal. Example: if PCF was set to D with an LCD of C, then the PCF would change to 5.					
X678	0X01	Modem error bit.	Modem error bit (ICW bit 3) is at wrong value.	A3P2	TA131	B-140	Regs defined in routine heading.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X67A	XXXX	Oscillator speed test. Each installed oscillator in the scanner under test is checked. The oscillator frequency is checked to ensure that there is no more than a plus or minus 0.25 percent variation from its expected frequency. The first installed line in the scanner is used to run the test. The test: 1. Resets and then enable the scanner. 2. Sets up the best possible upper scan limit for the line being used for the test. 3. Sets priority = 3. 4. Sets the display request bit so reg X'46' will be valid for the line in use. 5. Executes set mode with oscillator select 0 to ensure the line operates. (Pretest errors are indicated if set mode fails.) 6. Sets scope sync 2. 7. Executes a set mode with oscillator select bits for the oscillator position under test. 8. Masks off level 1, 2, and 3 interrupts. 9. Sets PDF to X'55' and the SDF to X'1D5'. 10. Sets PCF=8 (transmit initial). 11. Loops until SDF bit 3=0 (the 1st 3 bit times are not included in the speed test because the 1st 3 bit times are unpredictable. Examples: the 1st bit service is caused by the receive clock because transmit state is not active yet. Also when transmit state is set it may cause an extra strobe pulse if the oscillator is in a negative state at this time). 12. Reports an error if the SDF did not shift 3 times to set SDF bit 3 to 0 within 180 milliseconds. 13. Sets SDF=X'54'. 14. Loops for one second plus enough time to round bits per second count to a whole number, counts the number of bits that occur while in the loop, saves the loop count when and if the number of bits to be counted is actually counted, and alternately sets the SDF to X'54' and X'55' after each bit time to cause the TEST DATA LATCH (transmit data) to have alternate bits for a possible trouble shooting aid. 15. Calculates from the number of bits counted, the loop count and the tolerance whether the oscillator is running at the correct frequency. 16. Reports an error if the detected frequency is not within tolerance. The above is done for each of the 4 possible oscillators if the CDS entry for that oscillator position contains a valid oscillator type. Notes: This routine is dependent on the proper operation of the first installed line since the routine is designed to test the oscillators rather than the line sets. Also the oscillator type fields in the Configuration Data Set (CDS) must be right. If this routine fails, the oscillator card for the oscillator under test could be bad, the oscillator select bits could be bad, or the gating controls for the oscillators could be bad. Another possible failure is getting extra or missing strobe pulses not caused by the oscillator. The following registers are setup for all routine error displays except the set mode pretest errors beginning with 1: Reg X'11'=Line adr of line used in test (adr as used to set ABAR). Reg X'14'=Number of bits counted during the test. Reg X'15'=Relative oscillator position under test in byte 0, bits 0-7 with Hex 0 being 1st oscillator, 1 being 2nd oscillator, 2 being 3rd oscillator, and 3 being the 4th oscillator. Reg X'15'=Oscillator type in byte 1, bits 0-7. This type is as obtained from the CDS. Reg X'16'=Number of bits per second expected to be counted (rounded off to a whole number).					
X67A	0X01	Set mode with oscillator under test.	No level 2 interrupt occurred.	A3L2 A3T2 A3T4 A3U2 A3U4	TA611 TB411 TB412 TB413 TB414	C-020 C-160	See notes in heading of this routine for registers & checks.
X67A	0X02	SDF shifting.	SDF bit 3 did not set to 0 in the 180 millisecond wait time.	A3L2 A3T2 A3T4 A3U2 A3U4	TA611 TB411 TB412 TB413 TB414	C-020 B-480 B-410	SDF bits 1,2 & 3 were set via an output X'46' with X'01D5'. The SDF should have been shifted right, setting SDF bit 3 to a 0. See notes in heading of this routine for registers & checks.
X67A	0X03	Oscillator frequency.	Oscillator under test running too fast.	A3L2 A3T2 A3T4 A3U2 A3U4	TA611 TB411 TB412 TB413 TB414	C-020 C-040	Reg X'14' contains the number of bits actually counted. Reg X'16' contains the number of bits

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							expected to be counted. If reg X'14'=reg X'16', the oscillator is getting less than 1 bit time extra in the one second run but is still too fast (not within 0.25 percent of expected frequency). See notes in the heading of this routine for other registers and checks to be made.
X67A	0X04	Oscillator frequency.	Oscillator under test running too slow. Not enough bits counted in one second.	A3L2 A3T2 A3T4 A3U2 A3U4	TA611 TB411 TB412 TB413 TB414	C-020 C-040	Reg X'14' contains the number of bits actually counted and is less than reg X'16' which contains number of bits expected to be counted. See notes in the heading of this routine for other registers and checks to make.
X680	XXXX	IBM HDX Integrated Modem Test. This routine tests line set Types 5A, 5B, 6A, and LIB type 7. These are integrated versions of the 3872 modems. The test is equivalent to the Modem Test 2 defined in the 3872 Modem Maintenance Manual. The routine sets the test lead in the modem by setting both diagnostic mode and Data Terminal Ready during the set mode operation. Then it sets transmit initial and sends 1 bit to allow for Request To Send to be set. On 1st transmit Interrupt the PCF is set to X'D' for xmit turnaround leaving Request To Send on. Also PDF is set to FF to xmit a character of all 1 bits before the turnaround occurs. The program then waits 180 mili-seconds for the 'request to send' to 'clear to send' delays and then checks that the 'receive line signal detect' modem interface lead is on. The program then sets PCF to 7 (receive mode) and checks the received characters to insure an all mark character condition is received after a wrap is established through the modem scrambler circuits. An oscillator speed test is performed to check the modem clocks. The oscillator frequency is checked that there is no more than a plus or minus 0.5 percent variation from its expected frequency. An LCD of C is used through out this routine. Reg X'11' = Line address (ICW adr.) of line under test. (As used to set ABAR.)				
X680	0X01	Set Mode	No Level 2 interrupt occurred or Level 2 not from line in test. If display reg X'45' byte 0 bits 0-3 (LCD) are all on a feedback check occurred.				If reg X'14'=0000 no L2 occurred; Reg X'14'= line addr th caused the L2. Should have a L2 from set mode, the PCF should now = 0. If PCF = 0 the Set Mode completed OK but the L2 did not interrupt within 25 milli-seconds after it was issued. Reg X'13' = the bits used to set the SDF before Set Mode.
X680	0X02	Set Mode	The LCD is not C or PCF did not go to 0 after set mode.				Reg X'14'= LCD & PC in bits 0-7.
X680	0X03	Set Mode	ICW bits 0-3 are in error.				Reg X'14' contains ICW bits 0-3 in byte 0 and only bit 1 (service

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							request) should be on.
X680	0X11	Check modem and line set interface lines after the modem has been set into test mode via a set diagnostic mode and waiting 15 milli-seconds. This error will occur with 'receive line signal detect' bit being on if Type 2 scanner is not at or above EC 310284 or does not have REA 23-10645 installed.	Error if bits for 'data set ready', 'clear to send' or 'diagnostic mode' are not on or error if bits are on for 'receive line signal detect' or 'ring indicator'.				Reg X'14'= display reg(X'46') bits. Reg X'14' byte 0 Bits 0,2 & 5 should be on. Bits 1 & 3 should be off. other bits are not checked.
X680	0X14	Transmit initial.	No L2 occurred or L2 from wrong line address.				If PCF is still = 8 this indicates that 'CTS' did not occur. ('CTS' should be forced by the CS hardware since diagnostic mode is set). If the external (in the modem) clock is not running this error will occur. Also, check Reg. X'45' bits 0.0 to 0.3 and if they are all on, a feedback check has occurred. Reg. X'11' contains line addr of line under test. Reg. X'14' contains the line address that caused the L2 or Reg. X'14' = 0 if no L2 occurred. Reg. X'13' = bits output to SDF via output X'46' during the set mode.
X680	0X15	Transmit initial	ICW bits 0-3 in error.				Reg. X'14'=ICW bits 0-15. Bit 0.1 should be on (service request). Bits 0.0, 0.2 and 0.3 should be off. Reg. X'11' and X'13' sam as in error stop 0X14 comments.
X680	0X16	Transmit initial	LCD or PCF is bad.				Reg X'14' bits 0.0-0.3 are LCD and should be = X'C'. Bits 0.4-0.7 are PCF and should be X'9'. PCF was set to 8 and should have changed to 9. Regs. X'11', X'13' same as in error stop 0X14 comments.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X680	0X17	Transmit turn-around	No L2 occurred or L2 from wrong line address.				Reg X'11'=line addr under test. Reg X'14'= line address that caused the L2 if Reg X'14'= 0000 then no L2 occurred. On the previous character service interrupt the PCF was changed to X'D' to cause a transmit turn-aroun leaving 'RTS' on. The PCF should change to 5 when the last character of all 1 bits was serialized.
X680	0X18	Transmit turn-around	ICW bits 0-3 in error.				Reg X'11'=line address under test. Reg X'14'= ICW bits 0-15. Bits 0,2 and 3 should be off, bit 1 should be on.
X680	0X19	Transmit turn-around	LCD not=C or PCF not=5.				Reg X'11'=line address under test. Reg X'14' = LCD in bits 0-3 and PCF in bits 4-7. LCD should have remained at X'C'. PCF should have changed from X'D' to X'5'.
X680	0X22	Wait for 180 mili-seconds for the 'request to send' to 'clear to send' delay and check interface lines.	Error if modem interface or line set interface leads are not correct.				Reg X'14' = bits input from the display reg(X'46'). Reg X'14' byte 0 bits 0,2,3 & 5 should be on for 'clear to send', 'data set ready', 'receive line signa detect' (carrier detect) and 'diagnostic mode'. Bit 1 ('ring indicator') should off. Other bits are not checked.

At this point the PCF is set to 7 (receive data mode). The routine now loops for 300 character times to verify the steady mark condition. During this time the modem should be using its scrambler/descrambler circuits to transmit and receive a variable bit pattern generated by the modem. The output from the de-scrambler on the receive side should be all mark(one bits) if the modem is working correctly. The CS should serialize all 1 bits and every 8th bit time the routine should detect a character service interrupt with no error bits on and the PDF should be set to X'FF' each character interrupt time.

X680	0X3A	Continuous mark received from modem.	No L2 interrupt occurred or L2 interrupt occurred from the wrong line address.				If reg X'14' = 0000 no L2 occurred; reg X'14' = addr causing the L2. If LCD (input X'45' bits 0-3) is all ones, a feedback check has occurred. Reg. X'16' = the number

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							of all one bit characters received up to this error. Reg. X'13' = bits used to output X'46' to set the SDF when set mode was done. If Reg X'13' bit 1.5 is a 1, 'DRS' is on; if 0 'DRS' is off.
X680	0X3B	Continuous mark received from modem.	The LCD is not = C or the PCF is not = 7.				Reg X'45'. Byte 0 bits 0-3 are actual LCD and bits 4-7 are actual PCF. If the LCD is = F, a feedback check occurred. The program set LCD = C and PCF = 7 during routine test and they should remain thus till the program changes them. Regs X'13' and X'16' are same as error stop 0X3A.
X680	0X3C	Continuous mark received from modem.	ICW bits 0-4 are in error or the PDF is not = X'FF'.				Reg X'44' = ICW bit 0-7 in byte 0. ICW bit 1 (service request) and bit 4 (receive line signal detect) should be on. If ICW bit 3 (modem check) is on this indicates that the 'data set ready' line is inactive. Reg X'44' contains the PDF (received data char in byte 1. A zero bit is in this field for each bit failure of the modem. After each character service L the program resets this field to zeros to test the data on the next character service interrupt.

The routine now loops for 25 character times to test the speed of external clocks in the modem under test to a tolerance of 0.50 percent. Level 2 and 3 interrupts are masked during this test and the rate at which character service bits occur, compared with expected counts, form the basis of oscillator speed measurement. The slow speed oscillator(1200 BPS) is selected by having the 'data rate select' bit off during the set mode. The high speed(2400 BPS) oscillator is selected by having the 'data rate select' bit on during the set mode. In both cases the external clock bit was selected to select the modem clock.

X680	0X4D	External oscillator frequency	Oscillator under test is running too slow.				Reg X'13' byte 1 bit 5 is = 0 if low speed oscillator is

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							under test (Data Rate Select off), = 1 if high speed oscillator is under test (Data Rate Select on). The greater the difference between the contents of X'16' (expected count) and X'14' (actual count) the slower the oscillator is.
X680	0X4E	External oscillator Frequency.	Oscillator under test is running too fast.				Reg X'13' byte 1 bit 5 is = 0 if low speed oscillator is under test, = 1 if high speed oscillator is under test.

X681 XXXX IBM HDX Integrated Modem Wrap Test. This routine tests installed line set types 8A, 8B, 9A, 12A and 12B. The modems are wrapped with the fastest internal clock up to 1200 BPS. The test is run with an LCD of 6. An alternate 0 and 1 bit pattern is transmitted and received. The receive line will have Data Terminal Ready bit set along with diagnostic mode bit to cause the test lead to be activated in the modem. The transmit line will not have the Data Terminal Ready bit set so it will run in internal diagnostic mode and no errors should occur on the transmit line since it should have already been tested with internal wrap in previous routines. The adapters are not tested in synchronous mode since there is no difference in the modem operation than from start/stop mode.

Note 1: On all error stops in this routine, the following registers are set up

Reg X'11' = transmit line address which is used to set the 'test data' latch to provide the transmitted data bits. This is not the modem interface address that is being tested at this time.
Reg X'13' = receive line address which is the address of the modem interface that is being tested.

X681	0X01	1st level 2 for receive line set mode	No level 2 interrupt occurred or level 2 not from expected line address.				If reg X'14' = 0000 = 0, no L2 interrup occurred; reg X'14' line address of the interrupting line
X681	0X02	1st level 2 for receive line set mode	The LCD is not 6 or the PCF is not 0				Reg X'14' = LCD and PCF. When the set mode is completed, the CS should change PCF from 1 to 0.
X681	0X03	1st level 2 for transmit line set mode	No level 2 interrupt occurred or level 2 not from expected line address.				If reg X'14' = 0, no L2 interrup occurred; reg X'14' line address of the interrupting line.
X681	0X04	1st level 2 for transmit	The LCD is not 6 or the PCF is not 0.				Reg X'14' = LCD and PCF.

Setting diagnostic mode on the line sets under test causes the 'request to send' line to be activated to the modem interface. The program now waits 300 mili-seconds for the 'request to send' to 'clear to send' delays and for the 'receive line signal detect' circuits to function. Then transmit initial is set (PCF=8) to transmit a pad character of all one bits followed by a character of X'55' to cause alternate 0 and 1 bit (space and mark) transmission. From this point on the transmit and receive lines may interrupt in any order. When the 1st character is received, it and an additional 24 received characters are checked that they are alternate bits (X'55'). The transmit interrupts are accepted and the transmit LCD is validated on each transmit interrupt and the PDF is setup to send another alternate data bits character. The transmit line may be any type start/stop line set and is being run in internal diagnostic wrap mode and should cause no errors since it should have already been tested in previous internal wrap tests.

X681	0X05	Character transmitted.	No L2 interrupt occurred or L2 interrupt from wrong line address				If reg X'14' = 0, no L2 interrupt occurred; reg X'14'

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							interrupting line address.
X681	0X06	Character transmitted.	The transmit LCD is not 6 or the transmit PCF is not 9.				An expected interru occurred from transmit line address, however the LCD or PCF was not as expected. Reg X'14' contains the LCD and PCF in bits 0-7.
X681	0X07	1st character received	No L2 interrupt occurred from receive line address within 500 mili-seconds.				Carrier detect ('receive line signal detect') should be on in the modem and should be receiving alternate data bits.
X681	0X08	1st character received	The receive LCD is not 6 or the receive PCF is not 7				The expected L2 occurred from recei line address howeve the LCD or PCF was not as expected. Reg X'14' contains the LCD and PCF in bits 0-7.
X681	0X09	1st character received	ICW bits 0-4 are in error or the PDF is not =x'55'				Reg X'14' = ICW bits 0-7 in byte 0, bit 1(svc-req), bit 4 (RLSD) should be on. ICW bit 3 (modem check) is on indicates that 'DSR' line is inactive reg X'14' contains the PDF in byte 1 and this received data character should be X'55'
		The following errors were detected when the routine looped to count 24 additional receive line character service level 2 interrupts and verified the integrity of the received data characters.					
X681	0X10	Character received	No level 2 occurred or level 2 from wrong line address				If reg X'14' is all zeros no L2 interru occurred; reg X'14' = line addr of the interrupting line. Reg X'16' = the transmited characte count.
X681	0X11	Character transmitted	The transmit LCD is not=6 or transmit PCF not=9				See error code 0X06 Reg X'16'=received character count.
X681	0X12	Character received	The receive LCD is not=6 or receive PCF not=7				See error code 0X08 Reg X'16'= received character count.
X681	0X13	Character received	ICW bits 0-4 are in error or PDF is not=X'55'				See error code 0X09 Reg X'16' = receive character count.
X681	0X14	Check that 25 X'55' characters have been received.	Twenty-five X'55' characters were not received. Reg 16 contains the received character count.				
		The following errors were detected when the routine was testing the break feature. Check the line set cards for the receive line under test.					

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X681	0X20	Attempted to execute a set mode on the receive line (Reg 13).	Either the wrong line or no line interrupted. Reg 14 contains the interrupting line address.				See the routine heading for more information
X681	0X21	Attempted to execute a set mode on the receive line to Set the Break feature and Diag Wrap. Reg 13 contains the receive line address.	Either the wrong line or no line interrupted. Reg 14 contains the interrupting line address.				
X681	0X22	Transmitted and received X'FF'. Either the Xmit (Reg 11) or the receive line (Reg 13) should have interrupted.	Either the wrong line or no line interrupted indicating The data was not sent.				
x681	0X23	Transmitted X'FF' from the line address in Reg 11.	Either the LCD and/or the PCF changed. Reg 15 contains the incorrect LCDPCF.				
X681	0X24	Should have received from line address in Reg 13 X'00'.	The data received was not X'FF'. Reg 15 contains the bits in error.				
X681	0X25	Transmitted and received X'00'. Either the Xmit (Reg 11) or the receive line (Reg 13) should have interrupted.	Either the wrong line or no line interrupted indicating the data was not sent.				
X681	0X26	Transmitted X'00' from the line address in Reg 11.	Either the LCD and/or the PCF changed. Reg 15 contains the incorrect LCDPCF.				
X681	0X27	Should have received X'00' from the line address in Reg 13.	The data received was not X'00'.				

X683 XXXX IBM FULL DUPLEX MODEM WRAP TEST FOR LIB 11.
These modems are integrated versions of the 3872 full duplex modems.
The modem is connected to an even/odd pair of line interface addresses with the even address being the transmit line address and the odd address being the receive line address.
If errors are detected in this routine and routine X656 ran without errors, the modem cards for the failing line address are the most likely source of the problem.

Each pair of Full Duplex LIB 11 line sets are wrapped in the following sequence of steps:

1..... Reset and then enable the scanner and set the transmitted and received character counts to zero.
2..... Set the display bit in the transmit ICW.
3..... Wait 15 mili-seconds for the modem interface lines to settle down after the reset.
4..... Set the receive ICW bits for LCD, PCF, SDF and ICW bits 0-3 all to zero.
5..... Set scope sync 2.
6..... Input and check the display register bits (Input X'46').
These bits represent the transmit line modem interface leads after the interface has been reset and before diagnostic mode has been set.
If any of the transmit interface leads are in error then report the error with error code 0X11. Only the 'data set ready' lead should be on at this time.
See reg X'46' definition for the bits being tested.
7..... Set mode on the transmit line address.
Reg X'1D' byte 1 bits 0-7 are the bits output to SDF (ICW bits 26-33) prior to setting PCF to 1 for the set mode.
Reg X'1D' byte 1 bit 1 on is used to set the diagnostic mode latch on the transmit line interface and that diagnostic mode latch should cause the modem test lead to be activated to pick the modem test relay.
When the test relay is picked it should cause the transmit line interface to be connected to the receive line interface so that data may be wrapped from the transmit to the receive line address without an external wrap connection. This test relay should also disconnect the actual communications line while the wrap is being done to prevent data from going to the communications line.
Reg X'1D' byte 1 bit 2 is on to cause the 'data terminal ready' latch to be set on.
Bit 3 is on to cause the 'sync bit clock' latch to be set for synchronous clock correction.

ROUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

Bit 4 is on to cause the 'external clock' latch to be set to select the clock within the modem.
Bit 5 is off the first time through the test for this pair of lines so that the 'data rate select' latch will not be turned on and the 1200 BPS clock will be selected in the modem. The second time through the test this bit is on so that the 'data rate select' latch will be turned on to select the 2400BPS clock.
Bits 6 & 7 are off to select the first internal oscillator as the backup clock used for the set mode and setting transmit initial.
After the SDF is setup, the LCD is set to C and the PCF is set to 1 to initiate the set mode operation and then the program wait for 8 checks for a level 2 interrupt and normal completion of the set mode.

8..... Reset the display bit in the transmit ICW and then set the display bit in the receive ICW.

9..... Perform the set mode for the receive line interface address. The same bits are used as defined in step 7 except the diagnostic mode bit is not set on. Check for normal level 2 interrupt and normal LCD, PDF and ICW bits 0-4.

10....Reset the display bit in the receive ICW and then set the display bit in the transmit ICW.

11....Wait for 15 mili-seconds for the test relay to pick and for the modem interface leads to settle down.

12....Get the display register bits for the transmit line modem interface conditions. Check that bits are on for 'clear to send', 'data set ready' and 'diagnostic mode'. Note that the 'clear to send' and 'data set ready' bits are forced on by the scanner via diagnostic mode and do not reflect the actual modem interface conditions.
Also check that the 'ring indicator' and 'receive line signal detect' bits are off.

13....Reset the display bit in the transmit ICW and then set the display bit in the receive ICW.

14....Get the display register bits for the receive line modem interface conditions. Check that the 'data set ready' and 'receive data bit buffer' bits are on. Check that the bits for 'clear to send', 'diagnostic mode', 'ring indicator' and 'receive line signal detect' are all off.
Note that 'request to send' has not been set on the transmit line interface yet so that no carrier should be transmitted at this time so that the 'receive line signal detect'(carrier detect) bit should be off. If the 'receive line signal detect' bit is off then the modem should clamp the receive data to a mark(1 bit) and the 'receive data bit buffer' should be a one bit.

15....Reset the display bit in the receive ICW and then set the display bit in the transmit ICW.

16....Reset transmit ICW bits 0-3 & 5-7 and set PDF to X'FF'. Set transmit SDF to X'0003'. Set transmit LCD to C and PCF to 8 to set transmit initial which should bring up the 'request to send' interface lead to the modem and cause the modem to start sending carrier.

17....Wait for the level 2 from the transmit line to occurr and check the results including the display register contents for the transmit line modem interface leads.

18....Reset the display bit in the transmit ICW and then set the display bit in the receive ICW.

19....Wait for 180 mili-seconds to allow for the maximum 'request to send' to 'clear to send' delay in the modem and for 'receive line signal detect' to come on.
During this time the transmit lines SDF is constantly set to X'FF' to cause all one bits(mark) to be transmitted.

20....Get the receive line display register bits. Check that the 'data set ready', 'receive line signal detect'(carrier detect) and 'receive data bit buffer' bits are on. Check that the 'diagnostic mode', 'clear to send' and 'ring indicator' bits are all off. Note that the 'receive line signal detect' bit should be on now since the transmit line should have been transmitting carrier and then a scrambled data bit pattern after the 'clear to send' delay.
The receive side of the modem should be detecting the scrambled data pattern and resulting in an all one bits(mark) output to the 'receive data bit buffer'.

21....Set the receive LCD to C and PCF to 5 to cause the received data to be monitored for an EBCDIC SYNC character of X'32' which is used to establish character phase.

22....Wait for level 2 interrupt from transmit line which is sending a X'FF'. Check for normal completion.

23....Set the transmitted character count to zero.(In reg X'1F').

24....Reset the display bit in the transmit ICW, set the display bit in the receive ICW.

25....Check that the receive LCD is still equal to C, that the PCF is still equal to 5 and that SDF bits 2 through 5 are all on. Note that if SDF bits being tested are not all on then all one bits are not being received and the modem scrambler, de-scrambler or clock correction/selection circuits are not working properly.

26....Set transmit SDF to X'0355' to overlay the X'FF' that is now being sent. This is to allow for alternate data transitions for clock correction. Set transmit PDF to X'64' as the next data character to be sent after the alternate data transitions character in the SDF. This X'64' put into the PDF is an EBCDIC SYNC character shifted left one bit position. This shifting of the SYNC character is to insure that the receive line level 2 interrupts always occurrs after the transmit line level 2 character service interrupts even under worse case clock correction.

ROUT. CODE | ERROR FUNCTION TESTED | ERROR DESCRIPTION | SUSPECTED CARD LOCATION(S) | FEALD PAGE | FETMM PAGE | COMMENTS

27....Set the transmitted character count to 1.
28....Wait for and check results of the transmit line level 2 interrupt that should occurr after the alternate data bits character is completely transmitted and the shifted SYNC character is starting to be sent.
29....Setup to transmit another shifted SYNC character.
30....Set the transmitted character count to 2.
31....Will now enter a common wait sub-routine to wait for either a transmit or receive line level 2 character service interrupt.
32....If no level 2 interrupt occurred then set the error indicator to X'0001' and go to step 48 to report the error.
33....If the character service level 2 interrupt was not from the transmit or the receive line address then set the error indicator to X'0002' and go to step 48 to report the error.
34....If the level 2 was from the receive line address then go to step 41.
35....If here than level 2 was from the transmit line address. Check that the transmit LCD = C and that the PCF = 9 and if they are in error set error indicator to X'0003' and go to step 48 to report the error.
36....If transmit ICW bits 0-4 are bad then set error indicator to X'0004' and go to step 48 to report the error.
37....Add 1 to the transmitted character count. If count = 300 then set the error indicator to X'0000' to indicate no error and then go to step 48.
38....Compare the transmitted and received character counters. Note that the transmitted character count should always be 3 or 4 higher then the received character count due to no character service level 2 interrupts from the receive line until the second SYNC character is received. If too many characters have been received then set the error indicator to X'000A' and go to step 48 to indicate error has occurred. If too few characters have been received then set the error indicator to X'000B' and go to step 48 to indicate error has occurred.
39....Set the transmit PDF to X'AA' to cause alternate data bits to be transmitted. Note that this should be received as alternate data bits of X'55' in the receive PDF due to the shifted SYNC characters.
40....Go to step 31 to wait for next character service level 2 interrupt.
41....If here then just got a receive line character service level 2 interrupt.
42....Check that the receive line LCD = C and PCF = 7 and if not then set the error indicator to X'0008' and go to step 48 to indicate an error has occurred.
43....Check that the receive lines ICW bits 0-4 are good and that the received data in the PDF is good. If the received character counter is zero than the first received data character should be X'32' (an EBCDIC SYNC character). If the received character counter is not zero that the received data in the PDF should be X'55'. If the received data is bad or ICW bits 0-4 are bad then set the error indicator to X'0009' and go to step 48 to report the error.
44.... Add one to the received character counter.
45....Compare the transmitted and received character counters. If any errors then go to step 48 to report them. (See step 38 for error conditions).
46....Reset receive ICW bits 0-3, 5 and 8-15 to zeros.
47....Go to step 31 to wait for the next character service level 2 interrupt.
48.... If here and the error indicator is zero, then no error has occurred and the previous portion of the test has run ok. If the error indicator is not zero, then the type of error will be indicated by loading reg X'15' with the error indicator and displaying error code 0X60.
49....Will now mask off level 2 and level 3 interrupts and loop for 200 bit(25 character) times to test the speed of the external clock.
50....Report an error if clock is running too slow or too fast. These errors are based on counting the number of character service requests that were made by the scanner for the receive line during a program loop time based on the number of machine cycles per character time. If a failure is detected it could be the transmit or receive clock in the modem or the fact that the 'data rate select' function is not working on one of the line interfaces.
51....If the 'data rate select' bit was off for this test run then turn it on and go back to step 1 to repeat the test on the same pair of lines with 'data rate select' on.
52....Repeat all previous steps on the next pair of similar lines if any are installed.

Register usage within routine for all error stops:

reg X'11' = the transmit line interface address as used to set ABAR.
reg X'13' = the receive line interface address as used to set ABAR.
reg X'1D' = the set mode bits output to SDF on the transmit line during a set mode operation. The same bits are used to do the set mode for the receive line except byte 1 bit 1 is not set on so that diagnostic mode is not set on the receive line.
reg X'1E' = the received character count.
reg X'1F' = the transmitted character count.
reg X'46' = the display register modem interface lines for the ICW that has the display bit on. Following is the meaning of each bit in byte 0.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			Bit 0 = clear to send is on if this bit is on. Bit 1 = ring indicator is on if this bit is on. Bit 2 = data set ready is on if this bit is on. Bit 3 = receive line signal detect (carrier detect) is on if this bit is on. Bit 4 = receive data bit buffer and a one bit(mark) was the last data bit received if this bit is a one. Bit 5 = diagnostic mode latch is on if this bit is on. Bit 6 = bit service request latch was on if this bit is on. Note that this bit is turned on by the strobe pulse in the line set and is turned off by the scanner when the scanner processes the bit service. This bit may be on or off at any time and is ignored in this routine. Bit 7 = not used.				
X683	0X11	Transmit line modem interface leads after reset and before setting diagnostic mode.	Modem interface lines in error for transmit line. 'Data set ready' should be on. 'Clear to send', 'receive line signal detect', 'ring indicator' and 'diagnostic mode' bits should be off.				See rtn heading for registers. Reg X'14 reg x'46' bits (scanner display reg). Reg X'15' has a bit on for each b bit position in error in reg X'14'.
X683	0X20	Set mode level 2 interrupt.	No L2 or L2 not from the transmit line address. If reg X'14' = 0000 then no L2 occurred. If reg X'14' is not zeros then it is the address of the line that caused the L2.				See routine heading for more regs.
X683	0X21	LCD & PCF are valid after set mode.	Transmit lines LCD is not = C or PCF is not 0. Reg X'14' byte 0 = LCD & PCF input from transmit ICW via an input X'45'. If LCD is = F then a feedback check has occurred indication that one of the bits being used to do set mode did not set properly in the line set card or that some extra latch did set. If LCD is ok but PCF is still 1 then the set mode did not complete probably due to missing a bit service.				See routine heading for more regs.
X683	0X22	ICW bits 0-3 are valid after set mode has completed on the transmit line.	ICW bit 1(svc-req) is not on or ICW bits 0,2 or 3 are on. Reg X'14' = ICW bits 0-15 input via an input X'44' from the transmit line.				See routine heading for more regs.
X683	0X24	Set mode level 2 interrupt from the receive line.	No L2 or L2 not from the receive line address. If reg X'14' =0000 then no L2 occurred. If reg X'14' is not zero then it is the address of the line that caused the L2.				See routine heading for more regs.
X683	0X26	LCD & PCF are valid for receive line after set mode has been completed.	LCD not = C or PCF not = 0. Reg X'14' byte 0 = LCD & PCF obtained from receive ICW via an input X'45'. If LCD = F then a feedback check has occurred indicating some latch being set by the set mode did not come on or that some latch that should not come on did come on. If LCD = C but PCF is still 1 then the set mode did not complete normally which is usually caused by a missing bit service from the line set under test.				See routine heading for more regs.
X683	0X28	ICW bits 0-3 after set mode has completed on the receive line.	Error if ICW bits 0,2 or 3 are on or if ICW bit 1(svc-req) is not on. Reg X'14' = ICW bits 0-15 input from the receive ICW via an input X'44'. Reg X'15'				See routine heading for more registers.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	PETNM PAGE	COMMENTS
			has a bit on for each bit position in error in reg X'14'.				
X683	0X2A	Modem interface bits from display reg for the transmit line after set mode and a 15 mili-second wait.	Error if bits for 'clear to send', 'data set ready' and 'diagnostic mode' are not on or if bits are on for 'ring indicator' or 'receive line signal detect'. Reg X'14' = bits input via an input X'46' at the time the failure was detected.				See routine heading for more regs & display reg (X'46') bit definitions.
X683	0X2C	Modem interface bits from display register for receive line interface.	Error if bits for 'data set ready' & 'receive data bit buffer' are not on or if bits are on for 'clear to send', 'ring indicator', 'diagnostic mode' or 'receive line signal detect'(carrier detect). Reg X'14' = bits input from the display reg via an input X'46'. Note that 'request to send' has not been set on the transmit line yet so no carrier should be received and the 'receive line signal detect' line should not be active and the modem should be clamping the receive data lead to a mark(1 bit) which should cause the 'receive data bit buffer' to be a one bit.				See routine heading for more regs & for display reg(X'46') bit definitions.
X683	0X30	Level 2 character service interrupt after setting transmit initial(PCF=8).	No L2 or L2 not from the transmit line address. If reg X'14' = 0000 then no no L2 occurred. If reg X'14' is not zeros then it is the line address that caused the L2. If this error occurred you should display reg X'45' and check byte 0 bits 0-3 (LCD) and if LCD=F then the setting of 'request to send' and/or transmit mode may have caused a feedback check. LCD should be C and PCF should be 9(PCF was set to 8 for transmit initial and the scanner should have changed it to 9 at the first bit service time.)				See routine heading for more regs.
X683	0X32	ICW bits 0-4 from transmit ICW after L2 from transmit initial.	Error if ICW bits 0,2,3 or 4 are on or if ICW bit 1(svc-req) is off. Reg X'14' = transmit ICW bits 0-15 obtained via an input X'44'. Reg X'15' has a bit on for each bit position in error in reg X'14'.				See routine heading for more regs.
X683	0X34	LCD & PCF after transmit initial L2.	Error if transmit LCD not = C or PCF not = 9. Reg X'14' byte 0 = LCD & PCF input via an input X'45' from transmit ICW.				See routine heading for more regs.
X683	0X36	Modem interface bits from display register for transmit line after transmit initial.	Error if bits for 'data set ready', 'diagnostic mode' and 'clear to send' are not on or if bits are on for 'ring indicator' or 'receive line signal detect'. Reg X'14' = display reg bits input via an input X'46'.				See routine heading for more regs & display reg (X'46') bit definitions.
X683	0X3A	'Receive line signal detect' is on after a 180 mili-second wait during which time all one bits(mark) are being transmitted with 'request to send' on.	'Receive line signal detect' is not on or 'data set ready' is not on or 'receive data bit buffer' is not on or 'clear to send' is on or 'diagnostic mode' is on or 'ring indicator' is on.				See routine heading for more regs & display reg (X'46') bit definitions.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X683	0X40	L2 char-svc from transmit line sending a X'FF' char. Note: prior to checking for this L2 the receive PCF was set to 5 to monitor for an an EBCDIC SYNC character.	No L2 or L2 not from the transmit line address. If reg X'14' = 0000 then no L2 occurred. If reg X'14' is not zero then it is the address of the line that caused the L2.				See routine heading for more regs.
X683	0X42	ICW bits 0-4 from transmit of X'FF' char-service L2.	Error if ICW bits 0,2,3 or 4 are on or if ICW bit 1(svc-req) is off. Reg X'14' = ICW bits 0-15 obtained via an input X'44' from the transmit ICW. Reg X'15' has a bit on for each bit position that is in error in reg X'14'.				See routine heading for more regs.
X683	0X46	LCD & PCF from transmit of X'FF' char-svc L2.	Error if LCD not = C or if PCF not = 9. Reg X'14' byte 0 = transmit LCD & PCF obtained via an input X'45'.				See routine heading for more regs.
X683	0X48	Receive line LCD & PCF are valid and that the receive line is receiving all one bits.	Error if LCD not = C or if PCF not = 5 or SDF bits 2-5 are not all one bits. Reg X'14' byte 0 = receive LCD & PCF and byte 1 = SDF bits 0-7. Reg X'15' has a bit on for each bit position that is in error in reg X'14'.				See routine heading for more regs & display reg (X'46') bit definitions.
X683	0X4A	L2 from transmission of alternate data bits for clock correction. Prior to checking for this char-svc L2 the transmit SDF was set to X'0355' to overlay the X'FF' that was being sent and the PDF was set to X'64' as a shifted EBCDIC SYNC character.	No L2 or L2 not from the transmit line address. If reg X'14' = 0000 then no L2 occurred. If reg X'14' is not zeros then it has the line address that caused the character service level 2 interrupt.				See routine heading for more regs.
X683	0X4C	ICW bits 0-4 after L2 from transmission of alternate data bits.	Error if ICW bits 0,2,3 or 4 are on or if ICW bit 1(svc-req) is not on. Reg X'14' = ICW bits 0-15 input from transmit ICW via an input X'44'. Reg X'15' has a bit on for each bit position that is in error in reg X'14'.				See routine heading for more regs.
X683	0X4E	LCD & PCF after L2 from transmission of alternate bits for clock correction.	Error if transmit LCD is not = C or PCF not = 9. Reg X'14' byte 0 = LCD & PCF obtained via an input X'45' from transmit ICW.				See routine heading for more regs.
X683	0X60	Wrap 300 data characters checking for normal char-service level 2 interrupts and transmit/receive ICW bits including LCD,PCF,PDF and ICW bits 0-4.	Reg X'15' tells what type of error has occurred. If reg X'15' is 0000 then no error has occurred.				See routine heading for more regs.

If reg X'15' is not zero then the following table shows what the error was according to the contents of reg X'15'.

Register X'15'	Error indication.
0001 - - - -	No character service level 2 interrupt occurred for either the transmit or receive line addresses.
0002 - - - -	The character service level 2 interrupt was caused by some line address other than the transmit or receive line under test. Reg X'14' = the line address that caused the L2 interrupt.
0003 - - - -	Transmit line LCD is not C or PCF is not 9.
0004 - - - -	Transmit lines ICW bits 0-4 are in error. ICW bits 0,2 and 3 should be off, ICW bits 1(svc-req) should be on. ICW bit 4 is 'receive line signal detect' and should be off on the transmit line.
0008 - - - -	Receive line LCD is not C or PCF is not 7 on a receive line character service level 2 interrupt. Reg X'14' byte 0 = receive line LCD & PCF input via an input X'45'.
0009 - - - -	Received data in the PDF is bad or receive line ICW bits 0-4 are in error. Reg X'14' = receive lines ICW bits 0-15 with byte 1 (ICW bits 8-15) being the received data in the PDF.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			ICW bit 1(service request) should be on. ICW bit 4(receive line signal detect) should be on and it reflects the actual 'receive line signal detect' signal from the modem since the receive line is not in diagnostic mode. ICW bits 0,2 and 3 should be off. If the received character counter(reg X'1E') is zero then the received data in the PDF should = X'32'(an EBCDIC SYNC character). If the received character counter(reg X'1E') is not zero then the received data in the PDF should = X'55'. If the received character count = 0000 and the received data in the PDF = X'AA' then the first SYNC character was not recognized possibily due to a data bit error. Received data errors can be caused by clock correction or clock selection(data rate select) problems in the modem or by a scrambler/descrambler circuit failure in the modem.				
	000A - - - -		Too many characters have been received. Reg X'1E' = the received character counter, reg X'1F' = the transmitted character counter. The transmitted character counter should always be 3 or 4 higher then the received character counter due to line delay and the fact that the the alternate data bits character and the first SYNC character do not cause a receive line L2 interrupt and are not counted.				
	000B - - - -		Too few characters have been received. Reg X'1E' = the received character counter, reg X'1F'= the transmitted character counter. The ICW input register is loaded with the receive ICW bits at this time so you may display regs X'44',X'45' and X'47' to get information about the state of the receive line. Also the display bit is set in the receive lines ICW so the display reg(X'46') is valid for the receive line. If reg X'45' byte 0(LCD & PCF) = C5 then the receive line is still in monitor mode and has never recognized an EDCDIC SYNC character in which case you should look at reg X'45' byte 1(SDF bits 0-7) to see if an all one bits, all zero bits or varying data is being received. If SDF bits 2-7 are all one bits then the data is not being wrapped through the modem. If SDF bits 2-7 are alternate one and zero bits then the alternate data bits being transmitted at this time are being received but the two SYNC characters transmitted were not recognized.				
X683	0X70	Checking speed of the external modem clock.	Error if the external clock is too slow(not enough characters counted in what should have been 25(X'19') characters times). Reg X'14' = the number of chars counted. If reg X'1D' byte 1 bit 5 is off then the external clock in use should be 1200 BPS. If reg X'1D' byte 1 bit 5(data rate select) is on then the clock in use should be 2400 BPS.				See routine heading for more regs.
X683	0X71	Checking speed of the external modem clock.	Error if the external clock is too fast(25 characters were counted before the minimum loop count had been reached). If reg X'1D' byte 1 bit 5 (data rate select) is off the clock in use should be 1200 BPS. If the data rate select bit is on then the clock in use should be 2400 BPS.				See routine heading for more regs.

X684 XXXX IBM Full Duplex Modem wrap test for LIB 10.
These modems are similar to the Mini-12 full duplex modems.
The modem is connected to an even/odd pair of line interface addresses with the even address being the transmit line address and the odd address being the receive line address.
If errors are detected in this routine and routine X656 ran without errors then the modem cards for the failing line address are the most likely source of the problem.

Each pair of Full Duplex LIB 10 line sets are wrapped in the following sequence of steps:

1..... Reset and then enable the scanner and set the transmitted and received character counts to zero.
2..... Set the display bit in the transmit ICW.
3..... Wait 15 mili-seconds for the modem interface lines to settle down after the reset.

ROUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
4.....	Set the receive ICW bits for LCD, PCF, SDF and ICW bits 0-3 all to zero.					
5.....	Set scope sync 2.					
6.....	Input and check the display register bits (Input X'46'). These bits represent the transmit line modem interface leads after the interface has been reset and before diagnostic mode has been set. If any of the transmit interface leads are in error then report the error with error code 0X11. Only the 'data set ready' lead should be on at this time. See reg X'46' definition for the bits being tested.					
7.....	Set mode on the transmit line address. Reg X'1D' byte 1 bits 0-7 are the bits output to SDF (ICW bits 26-33) prior to setting PCF to 1 for the set mode. Reg X'1D' byte 1 bit 1 on is used to set the diagnostic mode latch on the transmit line interface and that diagnostic mode latch should cause the modem test lead to be activated to pick the modem test relay. When the test relay is picked it should cause the transmit line interface to be connected to the receive line interface so that data may be wrapped from the transmit to the receive line address without an external wrap connection. This test relay should also disconnect the actual communications line while the wrap is being done to prevent data from going to the communications line. Reg X'1D' byte 1 bit 2 is on to cause the 'data terminal ready' latch to be set on. Bit 3 is on to cause the 'sync bit clock' latch to be set for synchronous clock correction. Bit 4 is off so that external clock will not be selected. Bit 5 is off so that the 'data rate select' latch will not be set. Bits 6 & 7 are the oscillator select bits. These bit are setup to select the highest speed internal oscillator up to and including 1200 BPS.					
8.....	Reset the display bit in the transmit ICW and then set the display bit in the receive ICW.					
9.....	Perform the set mode for the receive line interface address. The same bits are used as defined in step 7 except the diagnostic mode bit is not set on. Check for normal level 2 interrupt and normal LCD, PDF and ICW bits 0-4.					
10.....	Reset the display bit in the receive ICW and then set the display bit in the transmit ICW.					
11.....	Wait for 15 mili-seconds for the test relay to pick and for the modem interface leads to settle down.					
12.....	Get the display register bits for the transmit line modem interface conditions. Check that bits are on for 'clear to send', 'data set ready' and 'diagnostic mode'. Note that the 'clear to send' and 'data set ready' bits are forced on by the scanner via diagnostic mode and do not reflect the actual modem interface conditions. Also check that the 'ring indicator' and 'receive line signal detect' bits are off.					
13.....	Reset the display bit in the transmit ICW and then set the display bit in the receive ICW.					
14.....	Get the display register bits for the receive line modem interface conditions. Check that the 'data set ready' and 'receive data bit buffer' bits are on. Check that the bits for 'clear to send', 'diagnostic mode' and 'ring indicator' are all off. The 'receive line signal detect' bit is not checked at this time since it may be on or off.					
15.....	Reset the display bit in the receive ICW and then set the display bit in the transmit ICW.					
16.....	Reset transmit ICW bits 0-3 & 5-7 and set PDF to X'FF'. Set transmit SDF to X'0003'. Set transmit LCD to C and PCF to 8 to set transmit initial which should bring up the 'request to send' interface lead to the modem and cause the modem to start sending carrier.					
17.....	Wait for the level 2 from the transmit line to occurr and check the results including the display register contents for the transmit line modem interface leads.					
18.....	Reset the display bit in the transmit ICW and then set the display bit in the receive ICW.					
19.....	Wait for 180 mili-seconds to allow for the maximum 'request to send' to 'clear to send' delay in the modem and for 'receive line signal detect' to come on. During this time the transmit lines SDF is constantly set to X'FF' to cause all one bits(mark) to be transmitted.					
20.....	Get the receive line display register bits. Check that the 'data set ready', 'receive line signal detect'(carrier detect) and 'receive data bit buffer' bits are on. Check that the 'diagnostic mode', 'clear to send' and 'ring indicator' bits are all off. Note that the 'receive line signal detect' bit should be on now since the transmit line should have been transmitting carrier and all one bits(mark) after the 'clear to send' delay. The receive side of the modem should be detecting the carrier and resulting in an all one bits(mark) output to the 'receive data bit buffer'.					
21.....	Set the receive LCD to C and PCF to 5 to cause the received data to be monitored for an EBCDIC SYNC character of X'32' which is used to establish character phase.					
22.....	Wait for level 2 interrupt from transmit line which is sending a X'FF'. Check for normal completion.					
23.....	Set the transmitted character count to zero.(In reg X'1F').					

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

24..... Reset the display bit in the transmit ICW, set the display bit in the receive ICW.

25..... Check that the receive LCD is still equal to C, that the PCF is still equal to 5 and that SDF bits 2 through 5 are all on. Note that if SDF bits being tested are not all on then all one bits are not being received and the modem or line set transmit and/or receive data circuits are not working properly.

26..... Set transmit SDF to X'0355' to overlay the X'FF' that is now being sent. This is to allow for alternate data transitions for clock correction. Set transmit PDF to X'64' as the next data character to be sent after the alternate data transitions character in the SDF. This X'64' put into the PDF is an EBCDIC SYNC character shifted left one bit position. This shifting of the SYNC character is to insure that the receive line level 2 interrupts always occurrs after the transmit line level 2 character service interrupts even under worse case clock correction.

27..... Set the transmitted character count to 1.

28..... Wait for and check results of the transmit line level 2 interrupt that should occurr after the alternate data bits character is completely transmitted and the shifted SYNC character is starting to be sent.

29..... Setup to transmit another shifted SYNC character.

30..... Set the transmitted character count to 2.

31..... Will now enter a common wait sub-routine to wait for either a transmit or receive line level 2 character service interrupt.

32..... If no level 2 interrupt occurred then set the error indicator to X'0001' and go to step 48 to report the error.

33..... If the character service level 2 interrupt was not from the transmit or the receive line address then set the error indicator to X'0002' and go to step 48 to report the error.

34..... If the level 2 was from the receive line address then go to step 41.

35..... If here than level 2 was from the transmit line address. Check that the transmit LCD = C and that the PCF = 9 and if they are in error set error indicator to X'0003' and go to step 48 to report the error.

36..... If transmit ICW bits 0-4 are bad then set error indicator to X'0004' and go to step 48 to report the error.

37..... Add 1 to the transmitted character count. If count = 300 or 3 seconds have elapsed then set the error indicator to X'0000' to indicate no error and then go to step 48.

38..... Compare the transmitted and received character counters. Note that the transmitted character count should always be 3 or 4 higher then the received character count due to no character service level 2 interrupts from the receive line until the second SYNC character is received. If too many characters have been received then set the error indicator to X'000A' and go to step 48 to indicate error has occurred. If too few characters have been received then set the error indicator to X'000B' and go to step 48 to indicate error has occurred.

39..... Set the transmit PDF to X'AA' to cause alternate data bits to be transmitted. Note that this should be received as alternate data bits of X'55' in the receive PDF due to the shifted SYNC characters.

40..... Go to step 31 to wait for next character service level 2 interrupt.

41..... If here then just got a receive line character service level 2 interrupt.

42..... Check that the receive line LCD = C and PCF = 7 and if not then set the error indicator to X'0008' and go to step 48 to indicate an error has occurred.

43..... Check that the receive lines ICW bits 0-4 are good and that the received data in the PDF is good. If the received character counter is zero than the first received data character should be X'32' (an EBCDIC SYNC character). If the received character counter is not zero that the received data in the PDF should be X'55'. If the received data is bad or ICW bits 0-4 are bad then set the error indicator to X'0009' and go to step 48 to report the error.

44..... Add one to the received character counter.

45..... Compare the transmitted and received character counters. If any errors then go to step 48 to report them. (See step 38 for error conditions).

46..... Reset receive ICW bits 0-3, 5 and 8-15 to zeros.

47..... Go to step 31 to wait for the next character service level 2 interrupt.

48..... If here and the error indicator is zero, then no error has occurred and the previous portion of the test has run ok. If the error indicator is not zero, then the type of error will be indicated by loading reg X'15' with the error indicator and displaying error code 0X60.

49..... Repeat all previous steps on the next pair of similar lines if any are installed.

Notes on register usage within this routine for all error stops:

reg X'11' = the transmit line interface address as used to set ABAR.
reg X'13' = the receive line interface address as used to set ABAR.
reg X'1D' = the set mode bits output to SDF on the transmit line during a set mode operation. The same bits are used to do the set mode for the receive line except byte 1 bit 1 is not set on so that diagnostic mode is not set on the receive line.
reg X'1E' = the received character count.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PEALD PAGE	PETMM PAGE	COMMENTS
		reg X'1F' = the transmitted character count. reg X'46' = the display register modem interface lines for the ICW that has the display bit on. Following is the meaning of each bit in byte 0. Bit 0 = clear to send is on if this bit is on. Bit 1 = ring indicator is on if this bit is on. Bit 2 = data set ready is on if this bit is on. Bit 3 = receive line signal detect (carrier detect) is on if this bit is on. Bit 4 = receive data bit buffer and a one bit(mark) was the last data bit received if this bit is a one. Bit 5 = diagnostic mode latch is on if this bit is on. Bit 6 = bit service request latch was on if this bit is on. Note that this bit is turned on by the strobe pulse in the line set and is turned off by the scanner when the scanner processes the bit service. This bit may be on or off at any time and is ignored in this routine. Bit 7 = not used.				
X684	0X11	Transmit line modem interface leads after reset and before setting diagnostic mode.	Modem interface lines in error for transmit line. 'Data set ready' should be on. 'Ring indicator', 'clear to send' & 'diagnostic mode' bits should be off.				See rtn heading for registers. Reg X'14' = bits from reg X'46'. (scanner display reg). Reg X'15' has a bit on for each bit position that is in error in Reg X'14'.
X684	0X20	Set mode level 2 interrupt.	No L2 or L2 not from the transmit line address. If reg X'14' = 0000 then no L2 occurred. If reg X'14' is not zeros then it is the address of the line that caused the L2.				
X684	0X21	LCD & PCF are valid after set mode.	Transmit lines LCD is not = C or PCF is not 0. Reg X'14' byte 0 = LCD & PCF input from transmit ICW via an input X'45'. If LCD is = F then a feedback check has occurred indication that one of the bits being used to do set mode did not set properly in the line set card or that some extra latch did set. If LCD is ok but PCF is still 1 then the set mode did not complete probably due to missing a bit service.				
X684	0X22	IC^W bits 0_{-3} are valid after set mode has completed on the transmit line.	IC^W bit $1(sv^{c-}r^eq)$ i_s not on or ICW bits 0,2 or 3 are on. Reg X'14' = ICW bits 0-15 input via an input X'44' from the transmit line.				
X684	0X24	Set mode level 2 interrupt from the receive line.	No L2 or L2 not from the receive line address. If reg X'14' =0000 then no L2 occurred. If reg X'14' is not zero then it is the address of the line that caused the L2.				
X684	0X26	LCD & PCF are valid for receive line after set mode has been completed.	LCD not = C or PCF not = 0. Reg X'14' byte 0 = LCD & PCF obtained from receive ICW via an input X'45'. If LCD = F then a feedback check has occurred indicating some latch being set by the set mode did not come on or that some latch that should not come on did come on. If LCD = C but PCF is still 1 then the set mode did not complete normally which is usually caused by a missing bit service from the line set under test.				

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X684	0X28	ICW bits 0-3 after set mode has completed on the receive line.	Error if ICW bits 0,2 or 3 are on or if ICW bit 1(svc-req) is not on. Reg X'14' = ICW bits 0-15 input from the receive ICW via an input X'44'. Reg X'15' has a bit on for each bit position in error in reg X'14'.				See routine heading for more registers.
X684	0X2A	Modem interface bits from display reg for the transmit line after set mode and a 15 mili-second wait.	Error if bits for 'clear to send', 'data set ready' and 'diagnostic mode' are not on or if bits are on for 'ring indicator' or 'receive line signal detect'. Reg X'14' = bits input via an input X'46' at the time the failure was detected.				See routine heading for more regs & display reg (X'46') bit definitions.
X684	0X2C	Modem interface bits from display register for receive line interface.	Error if bits for 'data set ready' & 'receive data bit buffer' are not on or if bits are on for 'clear to send', 'ring indicator' or 'diagnostic mode'. Reg X'14' = bits input from the display reg via an input X'46'.				
X684	0X30	Level 2 character service interrupt after setting transmit initial(PCF=8).	No L2 or L2 not from the transmit line address. If reg X'14' = 0000 then no no L2 occurred. If reg X'14' is not zeros then it is the address of the line that caused the L2. If this error occurred you should display reg X'45' and check byte 0 bits 0-3 (LCD) and if LCD=F then the setting of 'request to send' and/or transmit mode may have caused a feedback check. LCD should be C and PCF should be 9(PCF was set to 8 for transmit initial and the scanner should have changed it to 9 at the first bit service time.)				
X684	0X32	ICW bits 0-4 from transmit ICW after L2 from transmit initial.	Error if ICW bits 0,2,3 or 4 are on or if ICW bit 1(svc-req) is off. Reg X'14' = transmit ICW bits 0-15 obtained via an input X'44'. Reg X'15' has a bit on for each bit position in error in reg X'14'.				See routine heading for more regs.
X684	0X34	LCD & PCF after transmit initial L2.	Error if transmit LCD not = C or PCF not = 9. Reg X'14' byte 0 = LCD & PCF input via an input X'45' from transmit ICW.				See routine heading for more regs.
X684	0X36	Modem interface bits from display register for transmit line after transmit initial.	Error if bits for 'data set ready', 'diagnostic mode' and 'clear to send' are not on or if bits are on for 'ring indicator' or 'receive line signal detect'. Reg X'14' = display reg bits input via an input X'46'.				See routine heading for more regs & display reg (X'46') bit definitions.
X684	0X3A	'Receive line signal detect' is on after a 180 mili-second wait during which time all one bits(mark) are being transmitted with 'request to send' on.	'Receive line signal detect' is not on or 'data set ready' is not on or 'receive data bit buffer' is not on or 'clear to send' is on or 'diagnostic mode' is on or 'ring indicator' is on.				See routine heading for more regs & display reg (X'46') bit definitions.
X684	0X40	L2 char-svc from transmit line sending a X'FF' char. Note: prior to checking for this L2 the receive PCF was set to 5 to monitor for an an EBCDIC SYNC character.	No L2 or L2 not from the transmit line address. If reg X'14' = 0000 then no L2 occurred. If reg X'14' is not zero then it is the address of the line that caused the L2.				See routine heading for more regs.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X684	0X42	ICW bits 0-4 from transmit of X'FF' char-service L2.	Error if ICW bits 0,2,3 or 4 are on or if ICW bit 1(svc-req) is off. Reg X'14' = ICW bits 0-15 obtained via an input X'44' from the transmit ICW. Reg X'15' has a bit on for each bit position that is in error in reg X'14'.				See routine heading for more regs.
X684	0X46	LCD & PCF from transmit of X'FF' char-svc L2.	Error if LCD not = C or if PCF not = 9. Reg X'14' byte 0 = transmit LCD & PCF obtained via an input X'45'.				
X684	0X48	Receive line LCD & PCF are valid and that the receive line is receiving all one bits.	Error if LCD not = C or if PCF not = 5 or SDF bits 2-5 are not all one bits. Reg X'14' byte 0 = receive LCD & PCF and byte 1 = SDF bits 0-7. Reg X'15' has a bit on for each bit position that is in error in reg X'14'.				See routine heading for more regs & display reg (X'46') bit definitions.
X684	0X4A	L2 from transmission of alternate data bits for clock correction. Prior to checking for this char-svc L2 the transmit SDF was set to X'0355' to overlay the X'FF' that was being sent and the PDF was set to X'64' as a shifted EBCDIC SYNC character.	No L2 or L2 not from the transmit line address. If reg X'14' = 0000 then no L2 occurred. If reg X'14' is not zeros then it has the line address that caused the character service level 2 interrupt.				
X684	0X4C	ICW bits 0-4 after L2 from transmission of alternate data bits.	Error if ICW bits 0,2,3 or 4 are on or if ICW bit 1(svc-req) is not on. Reg X'14' = ICW bits 0-15 input from transmit ICW via an input X'44'. Reg X'15' has a bit on for each bit position that is in error in reg X'14'.				
X684	0X4E	LCD & PCF after L2 from transmission of alternate bits for clock correction.	Error if transmit LCD is not = C or PCF not = 9. Reg X'14' byte 0 = LCD & PCF obtained via an input X'45' from transmit ICW.				
X684	0X60	Wrap 300 data characters checking for normal char-service level 2 interrupts and transmit/receive ICW bits including LCD,PCF,PDF and ICW bits 0-4.	Reg X'15' tells what type of error has occurred. If reg X'15' is 0000 then no error has occurred.				

If reg X'15' is not zero then the following table shows what the error was according to the contents of reg X'15'.

Register X'15'	Error indication.
0001 - - - -	No character service level 2 interrupt occurred for either the transmit or receive line addresses.
0002 - - - -	The character service level 2 interrupt was caused by some line address other than the transmit or receive line under test. Reg X'14' = the line address that caused the L2 interrupt.
0003 - - - -	Transmit line LCD is not C or PCF is not 9.
0004 - - - -	Transmit lines ICW bits 0-4 are in error. ICW bits 0,2 and 3 should be off, ICW bits 1(svc-req) should be on. ICW bit 4 is 'receive line signal detect' and should be off on the transmit line.
0008 - - - -	Receive line LCD is not C or PCF is not 7 on a receive line character service level 2 interrupt. Reg X'14' byte 0 = receive line LCD & PCF input via an input X'45'.
0009 - - - -	Received data in the PDF is bad or receive line ICW bits 0-4 are in error. Reg X'14' = receive lines ICW bits 0-15 with byte 1 (ICW bits 8-15) being the received data in the PDF. ICW bit 1(service request) should be on. ICW bit 4(receive line signal detect) should be on and it reflects the actual 'receive line signal detect' signal from the modem since the receive line is not in diagnostic mode. ICW bits 0,2 and 3 should be off. If the received character counter(reg X'1E') is zero then the received data in the PDF should = X'32'(an EBCDIC SYNC character).

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			If the received character counter(reg X'1E') is not zero then the received data in the PDF should = X'55'. If the received character count = 0000 and the received data in the PDF = X'AA' then the first SYNC character was not recognized possibily due to a data bit error. Received data errors can be caused by clock correction or clock selection problems in the line set or by a transmit or receive data failure in the modem.				
	000A - - - -		Too many characters have been received. Reg X'1E' = the received character counter, reg X'1F' = the transmitted character counter. The transmitted character counter should always be 3 or 4 higher then the received character counter due to line delay and the fact that the the alternate data bits character and the first SYNC character do not cause a receive line L2 interrupt and are not counted.				
	000B - - - -		Too few characters have been received. Reg X'1E' = the received character counter, reg X'1F'= the transmitted character counter. The ICW input register is loaded with the receive ICW bits at this time so you may display regs X'44',X'45' and X'47' to get information about the state of the receive line. Also the display bit is set in the receive lines ICW so the display reg(X'46') is valid for the receive line. If reg X'45' byte 0(LCD & PCF) = C5 then the receive line is still in monitor mode and has never recognized an EDCDIC SYNC character in which case you should look at reg X'45' byte 1(SDF bits 0-7) to see if an all one bits, all zero bits or varying data is being received. If SDF bits 2-7 are all one bits then the data is not being wrapped through the modem. If SDF bits 2-7 are alternate one and zero bits then the alternate data bits being transmitted at this time are being received but the two SYNC characters transmitted were not recognized.				
X686	XXXX	SABRE line control RPQ test 1. RPQ's number 858655 and 858657 are the SABRE RPQ numbers. This routine test that PCF states 4,5 & 7 allow ICW bits 34 through 37 to be set and that other PCF states reset and hold all these bits to zero.					
X686	0X11	wait for bit service before setting LCD & PCF.	No bit service occurred.	A3Q2			Suspect bad line set card for line adr in reg X'11'.
X686	0X12	Check that all PCF states except 4, 5, & 7 reset ICW bits 34-37 to zero when in LCD state 'E' (SABRE mode RPQ).	Bits 34-37 not equal to zero.	A3Q2			Reg '15' bits 0.2-5 have a bit on for each bit found in error. Reg X'13' bits 1.4-1.7 = PCF in use.
X686	0X14	Check that PCF states 4, 5, & 7 allow ICW bits 34-37 to be set when in LCD state 'E' (SABRE mode RPQ).	Bits 34-37 not equal to one.	A3Q2			Reg '15' bits 0.2-0.5 indicate which bits did not set on. Reg X'13' byte 1 bits 4-7 are the PCF bits in use.
X687	0X01	Check that ICW bit 39 can be set and reset in LCD state 'E' (SABRE mode RPQ).	ICW bit 39 expected and actual results not equal.	A3Q2			Reg '13' bit 0.7 is expected results. R X'15' bit 0.7 is actual results.
X688	XXXX	Sabre RPQ line sets wrap data test. All installed line addresses that will run in Sabre mode are wrapped two at a time. The first installed Sabre line adr is made the receive line and the next installed Sabre line adr is made the transmit line. Then the test is performed on this pair of lines. When the test is completed on this pair of lines, the lines are reset and the line that was the transmit line is now made the receive line and the next installed Sabre line adr is made the new transmit line. Then this pair of lines is wrapped. This stepping up through the lines is continued until the last installed Sabre line has been the transmit line. Then the first installed line is made the transmit line and the last installed Sabre line is made the receive line and this pair of lines is wrapped. All the installed Sabre line sets are wrapped with LCD=E. A set mode is done on both the transmit and receive lines with ICW bit 27 (diagnostic wrap mode) and ICW bit 29 (sync bit clock) on. Oscillator select bits are 0 so the first oscillator is selected. The priority bits are set to 3. The set mode is done before the setting of scope sync 2 as each pair of lines is wrapped. The set mode must complete successfully for the wrap to function and any errors detected during the set mode are pre-test errors and all start with error code 1XXX. These error codes are near the end of the symptom index after all routine error codes. References to level 2 interrupts in the following error code displays are the character service level 2 interrupts that occur after scope sync 2 is set and do not include the level 2 interrupts that occurred for the set modes which occur before scope sync 2.					

ROUT. CODE	ERROR	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

Note 1: On all error stops in this routine, the following registers are setup:

reg X'11' = transmit line address (as used to set ABAR)
reg X'13' = receive line address (as used to set ABAR)
reg X'14' for errors that indicate level 2 occurred from wrong address = line address that caused the L2 or =0000 if no L2 occurred.

reg X'14' for errors that indicate received data is bad or ICW bits 0-7 in error = what was obtained by an input X'44' from the receive line ICW this is ICW bits 0-15. ICW bits 8-15 are the PDF which should contain the received data. ICW bits 0-7 are error and control flags and are always expected to be set as follows:

ICW bit 0 = Stop bit check and should be off
ICW bit 1 = Service request and should be on
ICW bit 2 = Character overrun and should be off
ICW bit 3 = Modem check and should be off
ICW bit 4 = Receive line signal detect and is not checked.
ICW bit 5 = Reserved bit and should be off
ICW bit 6 = Program flag and should be off
ICW bit 7 = Pad flag and should be off

reg X'16' for errors that indicate received data is bad, contains the expected ICW bits 0-15 that are being tested against the contents of reg X'14'.

Note 2: Checks to be made on all error stops:

a. Check LCD of failing line set. If LCD=F, a feedback check has occurred. Note that if the CDS indicates a line set that will run in Sabre mode is installed but this is not the case, a feedback check will occur.
b. You may use the continue function (except on pre-test errors starting with 1) to continue from this error to see if just this line set is failing, if all line sets in this LIB are failing, or if all Sabre lines are failing. You may get additional error stops on same line pair being wrapped so you may have to use the continue function multiple times. If only one line set is failing or a pair of even/odd addresses, then the line set card is probably bad. If all addresses fail in one LIB, the LIB's bit clock control card may be bad or the terminators may be bad. If all Sabre line sets fail, the CS cards may be bad. If the line sets are the type that will run in both Sabre and synchronous mode and if they run successfully in routine X656, then suspect LCD=E or the sync bit clock control line. Reference card location charts in the FETMM for the CS, LIB, and line set card locations which vary in location according to LIB types.

After the PAD characters of alternate data bits are sent for receive clock correction the synchronizing bit sequence of 11 consecutive zero bits and the transmitted data characters are shifted left by 1 data bit position. This is to cause the received data characters to be offset by 1 data bit from transmitted characters so that the interrupt sequence can be predictable and tested.

	Pad	Pad	Sync-char						
Transmit Data -	55	15	00	10	15	00	10	00	00	15	01	(Sabre)
Receive Data -					2A	00	20	00	00	2A		(Sabre)

The routine is run in the sequence of the following error codes.

ROUT. CODE	ERROR	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X688	0X01	Transmit of 1st pad completed.	No level 2 interrupt occurred from transmit line or L2 not from the transmit line address.	A3Q2			1st L2 char-svc after setting of scope sync 2. See rtn heading notes 1 and 2 for registe and checks to make.
X688	0X02	Transmit PCF went from 8 to 9.	Transmit PCF not = 9.	A3Q2			Transmit PCF set to 8 by program during hardware setup. The CS hardware should have changed the PCF to 9. Should now be in process of transmitting 2nd pad character. The transmit PDF is set to the 1st sync character after this error

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							display. See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X03	Transmit of 2nd pad completed.	No level 2 interrupt occurred or L2 was not from the transmit line address.	A3Q2			2nd char-svc L2 interrupt after sco sync 2. See notes a heading of this routine for registers and checks.
X688	0X04	Transmit of 1st 6 zero bits of synchronizing sequence completed.	No level 2 interrupt occurred.	A3Q2			3rd L2 interrupt after setting of scope sync 2.
X688	0X05	Transmit of 1st part of SYNC char sequence completed.	Level 2 not from transmit line address.	A3Q2			See rtn heading notes 1 and 2 for registers & checks. After this error display, the transmit PDF is set with X'15'.
X688	0X06	Transmit of 2nd part of SYNC char sequence completed.	No level 2 interrupt occurred from the transmit line address.	A3Q2			4th L2 after scope sync 2. See rtn heading notes 1 and 2 for registers & checks.
X688	0X07	Transmit of 2nd part of SYNC character sequence completed.	Level 2 not from transmit line address.	A3Q2	See rtn		heading notes 1 and 2 for registers and checks. After this error display, the transmit PDF is set to character X'00' to be transmitted next. Should now be in process of transmitting X'15'.
X688	0X08	Receive line recognized SYNC character.	Receive lines PCF not =7.	A3Q2			Receive line PCF wa initially set to 5 and as 2nd sync character is received and recognized, the hardware should set the receive PCF=7. Note that this setting of PCF=7 from PCF=5 does not cause a level 2 interrupt. See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X09	Receive 1st data char of X'2A'.	No level 2 occurred from receive line adr.	A3Q2			5th L2 (1st from receive line adr) after scope sync 2. See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X0A	Receive 1st data char of X'2A'.	Level 2 not from the receive line address.	A3Q2			See rtn heading notes 1 and 2

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							for registers and checks.
X688	0X0B	Receive 1st data char of X'2A'.	Received data in PDF is not X'2A' or ICW bits 0-7 are in error.	A3Q2			Received data in PDF should be 1st char of X'2A'. See notes 1 & 2 in heading of this routine for registers, ICW bits 0-7, & checks to make.
X688	0X0C	Transmit of X'15' char	No level 2 interrupt completed. line adr.	A3Q2 occurred for transmit			6th L2 (5th from transmit adr) aft scope sync 2. See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X0D	Transmit of X'15' char completed.	Level 2 not from transmit line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks. After this error display, the transmit PDF is set to the character X'10' which is the next character to transmit. The character X'00' should now be in the process of being transmitted.
X688	0X0E	Receive character X'00'.	No level 2 occurred from receive line adr.	A3Q2			7th L2 (2nd from receive addr) after scope sync 2. See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X0F	Receive character X'00'.	Level 2 not from receive line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks.
X688	0X10	Receive character X'00'.	Received data in PDF not = X'00' or ICW bits 0-7 in error.	A3Q2			See rtn heading notes 1 and 2 for registers, ICW bits 0-7, & checks.
X688	0X11	Transmit of X'00' completed.	No level 2 occurred for transmit line address.	A3Q2			8th L2 (6th from transmit addr). See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X12	Transmit of X'00' completed.	Level 2 not from transmit line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks. After this error display, the transmit PDF is set to X'00' as the next character to transmit. Should

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							now be in process o transmitting X'10'.
X688	0X13	Receive character X'20'.	No level 2 occurred for receive line adr.	A3Q2			9th L2(3rd from receive addr). See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X14	Receive character X'20'.	Level 2 not from receive line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks.
X688	0X15	Receive character X'20'.	Received data in PDF not = X'20' or ICW bits 0-7 in error.	A3Q2			See rtn heading notes 1 and 2 for registers, ICW bits 0-7, & checks to make.
X688	0X16	Transmit of X'10' completed.	No level 2 occurred for transmit line adr.	A3Q2			10th L2 (7th from transmit addr). See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X17	Transmit of X'10' completed.	Level 2 not from transmit line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks. After this error display, the transmit PDF is set to X'00' as the next character to transmit. Should now be in the process of transmitting X'00'.
X688	0X18	Receive character X'00'.	No level 2 occurred from receive line adr.	A3Q2			11th L2 (4th from receive line adr). See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X19	Receive character X'00'.	Level 2 not from receive line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks.
X688	0X1A	Receive character X'00'.	Received data in PDF not = X'00' or ICW bits 0-7 in error.	A3Q2			See rtn heading notes 1 and 2 for registers, ICW bits 0-7, & checks.
X688	0X1B	Transmit of X'00' completed.	No level 2 occurred from transmit line adr.	A3Q2			12th L2 (8th from transmit addr). See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X1C	Transmit of X'00' completed.	Level 2 not from transmit line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks. After this error display, the transmit PCF is set to X'D' for

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							transmit turn-around. Should now be in process of transmitting X'00'.
X688	0X1D	Receive character X'00'	No level 2 occurred from receive line adr.	A3Q2			13th L2 (5th from receive addr). See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X1E	Receive character X'00'	Level 2 not from receive line adr.	A3Q2			See rtn heading notes 1 and 2 for ICW bits 0-7, registers & checks be made.
X688	0X1F	Receive character X'00'	Received data in PDF not = X'00' or ICW bits 0-7 in error.	A3Q2			See rtn heading notes 1 and 2 for registers and checks, and ICW bits 0-7 should be.
X688	0X20	Transmit of X'00' completed.	No level 2 occurred for transmit line adr.	A3Q2			14th L2 (9th from transmit line adr.) See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X21	Transmit of X'00' completed.	Level 2 not from transmit line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks. After this error display, the transmit PDF is set to X'01' as the next character to transmit. Should now be in the process of transmitting X'15'.
X688	0X22	ICW bit 39 (reseq remember) should be turned on by the scanner because more than 11 consecutive zero bits should have been received at this time.	ICW bit 39 did not come on for the receive line.	A3Q2			See rtn heading notes 1 and 2 for registers and checks.
X688	0X25	Transmit of X'15' completed	No level 2 occurred for transmit line adr.	A3Q2			15th L2 (10th from transmit line adr). See notes 1 & 2 in heading of this routine for registers & checks.
X688	0X26	Transmit of X'15' completed	Level 2 not from transmit line adr.	A3Q2			See rtn heading notes 1 and 2 for registers & checks. After this error display, the transmit PDF is set to X'00' as the next character to transmit. Should now be in the process of transmitting X'01'.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X688	0X27	Receive character X'2A'.	No level 2 occurred from receive line adr.	A3Q2			16th L2 (6th from receive addr). See notes 1 & 2 in heading of this routine for registers & checks. Last L2 for receive.
X688	0X28	Receive character X'2A'.	Level 2 not from receive line adr.	A3Q2			
X688	0X29	Receive character X'2A'.	Received data in PDF not = X'2A' or ICW bits 0-7 in error.	A3Q2			See rtn heading notes 1 and 2 for registers and checks. ICW bit 1 (svc-req) and bit 7 (a synchronizing sequence has been detected) should be on. ICW bits 0 & 2 should be off. After this error display the receive PCF is set to 0 so no further level 2 interrupts should occur from the receive line addr.
X688	0X2A	Transmit of X'01' completed and transmit turn-around	No level 2 occurred from transmit line adr.	A3Q2			17th L2 (11th from transmit line adr.) and should be last level 2. See notes 1 & 2 in heading of this routine for registers & checks. At this time the transmit PCF should have turned around to PCF=5.
X688	0X2B	Transmit of X'01' completed and transmit turn-around.	Level 2 not from transmit line adr.	A3Q2			
X688	0X2C	Transmit turn-around.	Transmit PCF did not turn around to PCF=5.	A3Q2			After previous transmit level 2 (see error 0X26) transmit PCF was set to X'D' to cause a turn-around. The hardware should have completed the transmission of the character X'00' and then change PCF=5. See notes 1 & 2 in heading of this routine for registers & checks.

X689 xxxx Fractional Stop Bit RPQ: Insure that normal transmission of characters for Start-Stop interfaces with an 8/5 format are followed by fractional (1.4375) stop bits.

(Note: This RPQ is restricted to a 3705A with a Type II Communications Scanner, using a Type 2A (TTY) line set. The modified oscillator must be installed in Oscillator Position 1 and is modified to operate at 16 times normal speed. Oscillators are restricted to those whose normal operation is 45.5 bps, 50.0 bps, 56.89 bps, and 74.2 bps. Prior to running test, please insure that the proper RPQ bit is set in the Configuration

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		Data Set.)					
X689	0X01	Insure that bit service is occurring under Transmit Normal operation.	Error is flagged to indicate the character is not shifting out of the SDF.	01A3T4			Pretest error. Problem is probably in the card for oscillator Position 1.
X689	0X02	Insure that the SDLC Counter (ICW bits 34-37) cycles from 0 to 16 to initiate bit service.	Because of the modified oscillator operating 16 times its normal speed, gated bit service is dependent upon the counter which triggers bit service at the count of 16. The counter then resets to 0 and resumes count for the next bit service. An error will be flagged if this counter fails to reach the count of 16 or if bit service occurs prior to the count of 16.	01A-A3Q2	TB701		Pretest error. Check counter card.
X689	0X03	Checks transmission of first stop bit.	Error is flagged when SDF bit 8 does not go to 0. This indicates that the first stop bit has not been transmitted normally. Could indicate bit service is failing.	01A3T4 01A-A3Q2	TB701		Pretest error. Re-run routine for Error 1 ck. (Could indicate a time-out on loop count.)
X689	0X04	Checks transmission of second (last) stop bit.	Error is flagged when second stop bit in SDF 9 does not go to 0. This indicates either failing bit service or timeout on the loop count.	01A3T4 01A-A3Q2	TB701		Pretest error. Re-run routine for Error 1 ck.
X689	0X05	Insure that the last or fractional stop bit does not exceed .4375.	Error is flagged if the last stop bit does not transmit normally but the counter has exceeded 7. This will show if the counter as displayed in the low order of Reg. 5 exceeds 6 and the SDF bit 9 is still turned on.	01A-A3Q2 Q1A3T4	TB701		Error could indicate failing bit service.
X689	0X06	To insure that the last or fractional stop bit does not exceed .4375.	Error is flagged if the last stop bit in SDF position 9 transmits but the counter exceeds 7.	01A-A3Q2 01A3T4	TB701		The counter in ICW bits 34-37 should read 0 when the last stop bit transmits. The counter is to activate bit service and reset when the bits read 6.

X690 XXXX SABRE RPQ New Sync data lead test. This routine is a manual intervention routine and will not run unless you set the CE sense switch to run manual intervention routines or unless you request this routine as a single routine to run. This routine will run on SABRE RPQ line sets only. The output of this routine is a square wave on the 'New Sync' data lead for scoping. The routine will run for two minutes unless you abort it. This routine will stop with manual intervention stop codes of F0-- asking you for the needed information to run the test. These F0-- codes may be found near the end of this Type 2 CS symptom index.

There are no error stops in this routine but while the routine is running it will display a E0-- code in the display B lights indication that a square wave output should be available at the 'New Sync' data lead for the line under test.

X694 XXXX PCF state F disable test. This routine is a manual intervention routine and will not be run unless you set the CE sense switch to run manual intervention routines, or unless you requested a single routine to be run. This routine will stop with manual intervention codes of F0-- in display B, asking you to enter the information required to run this routine. These F0-- codes may be found at the end of this symptom index for the type 2 communication scanner IFT. This test routine does a PCF=F switched line interface disable to the line(s) you entered. The routine:

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		1. Disables ('CSB disabled' latch turned on) then enables the scanner under test. 2. Sets the display request bit in the line (ICW) under test. 3. Sets scope sync 2. 4. Sets the diagnostic mode bit, and if the line is only synchronous, sets the sync clock bit in the SDF. 5. Sets PCF=1 and LCD=7 for start/stop lines, or LCD=C for synchronous lines. 6. Waits for and validates that a level 2 interrupt occurred for the line under test. 7. Checks that the PCF went from 1 to 0. (Set mode completed ok.) 8. Sets PCF=F. 9. Waits for and validates that a level 2 interrupt occurred for the line under test. 10. Checks that the PCF went to 0. 11. Checks that the scanner display reg (X'46') byte 0, bits 0, 1, 2, 3, and 5 are all off that indicates the line interface has been reset. Notes: It should be noted that this routine will indicate failures on any line interface that has modem interface lines 'clear to send', 'ring indicator', 'data set ready' or 'receive line signal detector' tied up to active levels. For some modems, data sets and line set types, it is normal for some of these interface lines to be tied up to an active (on) level. If you requested all lines to be run, this routine will bypass LIB types 2, 3, and 4 since they always have some interface line active. If the test indicates failures due to modem interface lines being on when they should not be, you could have a bad interface converter on the line set for the line that failed or there could be a bad modem or data set connected to the line. If none of the lines completed the PCF=F portion of the test, the scanner cards may be bad. It is assumed that the other internal test routines have been run and that set modes and internal data wraps work properly. If this is not true, there could be a bad oscillator, a bad line set, a bad LIB, or some scanner failure. The following registers are valid for all error displays in this routine: Reg X'11'=line address that is under test. (As used to set ABAR.) Reg X'46'=The scanner display register for the line under test.				
X694	0X01	Set mode.	No level 2 interrupt occurred.	A3E2	TA331	B-310 B-260	This error should not occur if routines X627 and X629 ran successfully. Suggest you run those routines again. Should have had a level 2 interrupt from the set mode and PCF should now = 0. See notes in the heading of this routine for registers and more information.
X694	0X02	Set mode.	Level 2 interrupt not from the line under test.	A3E2	TA331	B-300	This error should not occur if routines X627 and X629 ran successfully. Suggest you run those routines again. Should have had a level 2 interrupt from the set mode and PCF should now = 0. See notes in the heading of this routine for registers and more information. Reg X'14'=line adr that caused the L2 interrupt.
X694	0X03	Set mode.	PCF did not go to 0 after set mode.	A3E2	TA331	B-080	See comments in error 0X01. Reg X'14' byte 0 =LCD and PCF obtained by an Input X'45' at the time of failure.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X694	0X04	PCF=F completed.	No level 2 interrupt occurred after PCF was set to F.	A3F2	TA811	B-310	No level 2 interrupt will occur if some modem interface lines did not reset. See notes in the heading of this routine for registers and more information.
X694	0X05	PCF=F completed.| the line under test.	Level 2 interrupt not from	A3E2	TA331	B-300	This error may have nothing to do with the PCF=F test since no other line should cause a level 2. See notes in the heading of this routine for registers and more information. Reg X'14' contains the line adr that caused the level 2 interrupt.
X694	0X06	PCF=F completed.	PCF did not change to 0.	A3F2	TA811	B-080 B-260	Hardware should hav changed PCF to 0 from PCF=F after the modem interface is reset. If 'Data Set Ready' and 'Receive Line Signal Detect' interface lines did not reset properly, PCF may still = F. See notes in the heading of this routine for more information.
X694	0X07	Modem interface reset.	All modem interface lines that should be reset are not reset.	A3E2	TA331	B-150	Reg X'14'= Reg X'46' at the time of failure. Note: reg X'46' is loaded every scan cycle so it may not be = to reg X'14' at this time. Reg X'15' has a bit on for each bit position that is bad in reg X'14'. See notes in heading of this routine for more information.

X698 XXXX Diagnostic transmit test for PCF=B. This routine is a manual intervention routine and will not be run unless you set the CE sense switch to run manual intervention routines, or unless you requested a single routine to be run. This routine will stop with manual intervention codes of F0-- in display B, asking you to enter the information required to run this routine. These F0-- codes may be found at the end of this symptom index for the type 2 communication scanner IFT. This routine transmits a PAD character (X'FF'), and 2 data characters (X'AA'). The routine sets PCF=B to transmit the second data character, then the scanner sets PCF=C & checks that the transmit line turned around. This is a manual intervention routine because PCF=C turnaround requires the 'clear to send' modem interface line to drop and this does not occur on some modem interfaces that have this line tied up to an active (on) level. This routine runs on start/stop lines only, and uses LCD=7.

Notes: This routine indicates a failure on any line interface that does not drop the 'clear to send' modem interface line. If 'clear to send' should not be on for this interface, you should suspect the line set card for the failing line. If all lines fail, there may be a bad scanner card. Errors 0X01 through 0X05 should not occur and if they do you should run routine X645

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	PEALD PAGE	FETMM PAGE	COMMENTS
		to try to find the failure. The following registers are setup for all error displays: Reg X'11'=Line address of line under test (as used to set ABAR). Reg X'46'=Scanner display register and is valid for the line under test. Reg X'14'=Line that caused the L2 interrupt for errors that say 'L2 interrupt not from the line under test'.					
X698	0X01	Transmit of PAD completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	
X698	0X02	Transmit of PAD completed.	Level 2 interrupt not from the line under test.	A3L2	TA611	B-300	
X698	0X03	Transmit of PAD completed.	PCF did not go to 9.	A3F2	TA811	B-080	PCF set to 8 by program for transmit initial. The scanner hardware should have changed it to 9. See notes in the heading of this routine.
X698	0X04	Transmit of 1st data (X'AA') completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	
X698	0X05	Transmit of 1st data (X'AA') completed.	Level 2 interrupt not from the line under test.	A3L2	TA611	B-300	See routine heading notes After this error display, the PCF is set to B.
X698	0X06	Transmit of 2nd data (X'AA') completed.	No level 2 interrupt occurred.	A3L2	TA611	B-080 B-310 B-260	If 'c-t-s' did not drop, this interrupt will not occur. PCF should have been changed to C if the last data character was transmitted ok. See notes in the heading of this routine for more information.
X698	0X07	Transmit of 2nd data (X'AA') completed.	Level 2 interrupt not from the line under test.	A3L2	TA611	B-300	
X698	0X08	PCF went to 7.	PCF did not set to 7 after transmit turn-around.	A3F2	TA811	B-080	PCF was changed to C by the hardware, an an additional bit time should occur and if 'clear to send' is off, PCF should be changed to 7 by the scanner hardware. See notes in the heading of this routine for more information.
X698	0X09	SDF = 0.	SDF bits 0-7 did not = 0.	A3H2	TA221	B-480	Turnaround should leave SDF=0. See notes in the heading of this routine for more information.
X698	0X0A	SDF = 0.	SDF bits 8-9 did not = 0.	A3H2	TA221	B-480	Turnaround should leave SDF=0. See notes in the heading of this routine for more information.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X699	XXXX	Diagnostic transmit test for PCF=C. This routine is a manual intervention routine and will not be run unless you set the CE sense switch to run manual intervention routines, or unless you requested a single routine to be run. This routine will stop with manual intervention codes of F0-- in display B, asking you to enter the information required to run this routine. These F0-- codes may be found at the end of this symptom index for the type 2 communication scanner IFT. This routine transmits a PAD character (X'FF'), and 2 data characters (X'AA'). The routine transmits the second data character, then sets PCF=C and checks the 'clear to send' modem interface line to drop and this does not occur on some modem interfaces that have this line tied up to an active (on) level. This routine runs on DLC line only, and uses LCD=9. This routine indicates a failure on any line interface that does not drop the 'clear to send' modem interface line. If 'clear to send' should not be on for this interface, you should suspect the line set card for the failing line. If all lines fail, there may be a bad scanner card. Errors 0X01 through 0X05 should not occur and if they do you should run routine X645 to try to find the failure. The following registers are setup for all error displays: Reg X'11'=Line address of line under test (as used to set ABAR). Reg X'46'=Scanner display register and is valid for the line under test. Reg X'14'=Line that caused the L2 interrupt for errors that say 'L2 interrupt not from the line under test'.					
X699	0X01	Transmit of 1st data (X'AA') completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	See notes in the heading of this routine.
X699	0X02	Transmit of 1st data (X'AA') completed.	Level 2 interrupt not from the line under test	A3L2	TA611	B-300	See notes in the heading of this routine.
X699	0X03	Transmit of 1st data (X'AA') completed.	PCF did not go to 9.	A3F2	TA811	B-080	PCF was set to 8 by program for transmit initial. The scanner hardware should have changed it to 9. See notes in the heading of this routine.
X699	0X04	Transmit of 2nd data (X'AA') completed.	No level 2 interrupt occurred.	A3L2	TA611	B-310 B-260	See notes in the heading of this routine.
X699	0X05	Transmit of 2nd data (X'AA') completed.	Level 2 interrupt not from the line under test.	A3L2	TA611	B-300	See notes in the heading of this routine. After this error display, the PCF is set to B.
X699	0X06	Transmit turn completed.	No level 2 interrupt occurred.	A3L2	TA611	B-080 B-310 B-260	If 'clear to send' did not drop, this interrupt will not occur. PCF should have changed to 5 if the last data character was transmitted ok. See notes in the heading of this routine for more information.
X699	0X07	Transmit turn completed.	Level 2 interrupt not from the line under test.	A3L2	TA611	B-300	See notes in the heading of this routine.
X699	0X08	PCF went to 5.	PCF did not set to 5 after transmit turn-around.	A3F2	TA811	B-080	After PCF was set to C, an additional bit time should occur and if 'clear

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	PETMM PAGE	COMMENTS
							to send' is off, PCF should be changed to 5 by the scanner hardware. See notes in the heading of this routine for more information.

X69C XXXX Modem interface check. This routine is a manual intervention routine and will not run unless you set the CE sense switch to run manual intervention routines, or unless you requested a single routine to be run. This routine stops with manual intervention codes of F0-- in display B asking you to enter the information required to run this routine. These F0-- codes may be found at the end of this symptom index for the type 2 communication scanner IFT. This routine checks that the modem interface lines 'clear to send' and 'receive line signal detector' are not on, and that the 'receive data bit' buffer is on. This test is run with 'request to send' off and diagnostic wrap mode off.

Notes: This routine will indicate failures on all modem interface and/or line sets that have 'clear to send' and 'receive line signal detector' ties up to active (on) levels. Example - all LIB type 2 telegraph line sets should have 'receive line signal detector' active all the time and should cause failures. If failures occur and the interface line in error should not have lines tied to active levels, suspect a bad line set card or modem interface problem. The following registers are setup for error displays:

Reg X'11'=Line address (as used to set ABAR) of the line under test.
Reg X'46'=The scanner display register which should be loaded by the scanner every scan cycle for the line under test.
Reg X'14'=What was in the display reg X'46' at the time the failure was detected. Reg X'14' may not = reg X'46' if you display reg X'46' since reg X'46' may be changed on each scan cycle.
Reg X'15' contains bits in error with each bit position that is on representing the bit position in reg X'14' that is in error.

X69C	0X01	Modem interface.	Interface lines not in expected condition.		B-150		Reg X'14' byte 0 bit 0 is the 'cts' bit and should be off; bit 3 is the 'receive line signal detector' bit and should be off; bit 4 is the receive data bit buffer bit and should be on.

X6CE XXXX Modem, auto-call-originate, DLC link test and external wrap test. This is a manual intervention routine and will not be run unless you set the CE sense switch to run manual intervention routines or unless you make a single routine request. See notes after step 18 writeup for restrictions on use of Full-Duplex modems, full-duplex line set interfaces and other wrap options. You should not have the 'loop on first error' or 'restart routine on first error' CE sense switches on while this routine is running since this routine always causes a repeat of previously executed steps if any errors are detected. If you get an error stop code, you may use the continue function(function 5) to cause the test to restart. The restart point varies according to the type of error and the step within the test. You may also use the dynamic communications function of the DCM to pass some restart or loop requests to this routine. The accepted dynamic communication codes are defined in step 18 of this routine heading. This routine will stop with manual intervention stop codes from F030 through F042 in sequence asking you for the test options and line addresses to be tested. Some of the F030 through F042 stop codes will be bypassed according to what options you have previously selected. These stop codes are defined near the end of the Type 2 Communication Scanner IFT Symptom Index. This routine is designed to test line set cards and/or IBM modems and/or IBM auto call originate or IBM local attachments. This routine may also be used with non-IBM modems/data sets and/or auto call originate equipment but is only intended as an IBM line driver and terminator test in the line set cards and not as a test of the non-IBM equipment. During the running of this routine the timer interrupt dependent functions within the DCM will not function properly due to the fact that this routine intercepts all timer interrupts. This means that the DCM utility functions to display or stop during timer interrupts and the scoping indicator in display B byte 0 bit 4 will not operate. You should not use the DCM utility function for address compare level 1 interrupt while this routine is running or overrun/underrun or other ICW bits 0-4 errors may occurr.

This routine is broken down into steps, each of which performs one or more functions. Each step is assigned a number. Each step number may be referenced as a restart point after an error stop code is displayed or as a dynamic communications option entered. All references to going to another step after an error stop, assume either that you used the continue function (select function 5 and press the start push button) or that the bypass error stop and bypass new error stop CE sense switches are on.

ROUT. CODE	ERROR	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

NOTE 1: No card calling is done within this routine. The IBM CE should refer to the Maintenance Procedures for IBM Integrated Modems in the FETMM for trouble shooting IBM integrated modems. The line set interface pages in the FETMM should be referenced for line interface drivers, terminators and cable connections to external interfaces.

NOTE 2: For external wrap options utilizing a wrap block an error may occur indicating ICW Bit 4 (Receive Line Signal Detect) is not on for the receive line. This may be attributed to carrier not being present at the wrap block. On EIA interfaces the 'request to send' interface pin should be jumpered via a 'Y' jumper to both the 'clear to send' interface pin on the same interface and to the 'receive line signal detect' pin on the other interface.

NOTE 3: For examples on using this routine, refer to examples with the manual intervention stop codes.

NOTE 4: Full-duplex line sets and modems should be tested with the following restrictions. You should always select option 0003 (wrap data) when you get manual intervention stop code F030. If you want to do a transmit only test then you should select the 'ignore receive interrupts' option when you get the F042 stop code. If you want to do a receive only test you should select the 'transmit all ones' option when you get the F040 stop code. The receive only test will work only for 'DLC link test', 'receive all ones', 'receive all zeros' or 'ignore receive interrupts' options. When you are asked for the transmit and receive line addresses you should select both the transmit and receive line addresses that are connected to the same full-duplex interface. The above restrictions are not program enforced since you may select to do an internal diagnostic wrap for modem self-test or to internally wrap between a single side of a full-duplex interface to a different interface.

X6CE	0X01	Auto Call originate.	SDF bits are in error or LCD is not =3 or PCF is not=0.				Reg. X'14' byte 0= LCD in bits 0-3 & PCF in bits 4-7: byte 1 bits 0-7 are SDF bits 0-7. Only bit 1 of the SDF, power indicator (PWI) should be on. SDF bit definitions for auto call are: Bit 0=Interrupt remember. Bit 1=Power indicator. Bit 2=call request. Bit 3=Data Line occupied. Bit 4=Present next digit. Bit 5=call orig status. Bit 7=Abandon call and retry.
X6CE	0X02	Auto Call originate.	No level 2 interrupt occurred after an auto call interface reset or level 2 interrupt was from the wrong line address.				If Reg. X'14'= 0 no L2 occurred; reg X'14'= addr causing the L2.
X6CE	0X03	Auto call originate	After attempted reset of auto call interface by setting the PCF to F, the LCD is not=3, PCF did not go to 0, or SDF bits are in error.				See comments in error code 0X01 for reg and SDF definition.
X6CE	0X04	Auto call originate.	Character service request bit (ICW Bit 1) is not on or PDF is not=0.				Reg X'14'=ICW bits 0-15 with the service-request bit in byte 0 bit 1 and the autocall interface PDF in byte 1 bits 0-7.
X6CE	0X06	Setup of switched receive line address.	No level 2 interrupt occurred after switched line reset				If reg X'14'=0000 no L2 occurred;

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			(PCF=F) or a level 2 interrupt occurred from the wrong line address.				reg X'14'= addr that caused the L2.
X6CE	0X07	Setup of switched receive line address.	The receive line LCD has changed or the PCF did not get changed to 0 from F when doing switched line reset.				Reg X'13' byte 0= expected LCD in bits 0-3. Reg X'14' byte 0 is the actual LCD in bits 0-3 & actual PCF in bits 4-7.
X6CE	0X08	Setup of switched receive line address.	The modem interface line bits in the display register are in error for the receive line address.				Reg X'14'= bits from X'46' (scanner display register.) Only bit 4 (receive data bit buffer) should be on for a switched line in reset condition. Bit 0=CTS. Bit 1=Ring ind. Bit 2=DSR. Bit 3=Rec line-signal det. Bit 4=Receive data bit buffer. Bit 5=Diagnostic wrap mode.
X6CE	0X09	Setup of switched receive line address.	Character service request bit (ICW bit 1) is not on, PDF is not=X'00' or any of ICW bits 0,2 or 3 are on.				Reg X'14'= PDF in byte 1 bits 0-7 and reg X'14' byte 0= ICW bits 0-7. ICW bits 1 (svc-req) should be on, ICW bits 0, 2,3,4,6 & 8 should be off. ICW bit definitions are: Bit 0=stop bit ck. Bit 1=Service request. Bit 2=Character overrun/ underrun. Bit 3=Modem check. Bit 4=Receive line-Signal detect Bit 5= is ignored Bit 6=Program flag Bit 7=Pad flag.
X6CE	0X0A	Set mode for switched receive line address.	Level 2 interrupt did not occur for set mode or a level 2 interrupt occurred from the wrong line address.				Reg X'14'=all zeros if no L2 occurred; reg X'14'=addr that caused the L2.
X6CE	0X0B	Set mode for switched receive line address.	The LCD changed or the PCF not=0 after set mode completion.				Reg X'13' bits 0.0-3 is the LCD used during set mode. Reg X'14' byte 0= LCD in bits 0-3 and PCF in bits 4-7 after set mode.
X6CE	0X0C	Set mode for switched receive line address.	The modem interface line bits in the display register are in error.				See comment for error stop 0X08

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X6CE	0X0D	Set mode for switched receive line address.	Character service request bit (ICW Bit 1) is not on, PDF is not=0 or any error bits on.				See comment for error stop 0X09
X6CE	0X12	Setup of switched or autocall transmit line	No level 2 occurred after a switched line reset (PCF=F) from the wrong line address.				If reg X'14' = 0000, no L2 X'14'= addr that caused the L2.
X6CE	0X13	Setup of switched or autocall transmit line address.	The switched line reset has changed the LCD or the PCF has not been forced to 0.				Reg X'13' byte 0 bits 0-3=LCD used before reset. Reg X'14' byte 0= LCD in bits 0-3 and PCF in bits 4-7 after line reset.
X6CE	0X14	Setup of switched or autocall transmit line address.	The modem interface line bits in the display register are in error.				See comment for error stop 0X08.
X6CE	0X15	Setup of switched or autocall transmit line address.	Character service request bit (ICW bit 1) is not set, PDF is not=0 or any error bit(s) on.				See comment for error stop 0X09
X6CE	0X16	Set mode for switched transmit line address.	No level 2 interrupt occurred after a set mode or a level 2 interrupt occurred from wrong line address.				Set mode done with the external-clock bit and the diagnostic mode bit off but with any other set mode bits selected except the 'data terminal ready' bit is always turned on. If reg X'14'= all zeros, no L2 occurred, else reg X'14' contains the address of the interrupting line.
X6CE	0X17	Set mode for switched transmit line address.	The LCD changed during a set mode or the PCF did not change to 0.				LCD in Reg X'13' bits 0.0-3 used for set mode. Reg X'14 byte 0 bit 0-3=LCD & bits 4-7 = PCF from ICW after set mode.
X6CE	0X18	Set mode for switched transmit line address.	The modem interface line bits in the display register are in error.				See comment for error stop 0X08
X6CE	0X19	Set mode for switched transmit line address.	Character service request bit (ICW bit 1) is not set, or PDF is not=00 or any other bit on in error.				See comment for error stop 0X09
X6CE	0X1F	Any type of switched and line connection established by CE by dialing.	No level 2 interrupt is pending after the program has looped for 3 minutes waiting for CE to press the START push button and program will loop, waiting for a L2 interrupt pending, for another 3 minutes.				

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X6CE	0X20	Dial on autocall originate line interface	A L2 interrupt occurred within 500 milliseconds				Set autocall PCF to 4 to cause the CRQ latch to be set on the next bit time. IBM autocall units have a minimum of 1.5 seconds delay before PND should be set. Reg X'15' contains address of line causing L2 interrupt.
X6CE	0X23	Dial on autocall originate line interface.	No L2 interrupt is pending within a maximum wait time of 20 seconds.				After a 1.5 milisecond delay to within 20 seconds an interrupt should have occurred from autocall unit. Both this and the previous error stop indicate a failure in autocall timing.
X6CE	0X24	Dial on autocall originate line interface.	While waiting for a L2 interrupt from auto call line interface a level 2 interrupt occurred from some other line address.				Reg X'11'= auto call line addr. Reg X'14'= addr that caused the L2.
X6CE	0X25	Dial on autocall originate line interface	The LCD is not=3 or PCF is not=4 or SDF bits are in error.				Reg X'14' byte 0 = LCD in bits 0-3 & P bits 4-7. Reg X'14' byte 1=SDF and should = X'F8'. The following bit definitions are SDF bit definitions for autocall interface: Bit 0=IR should be on Bit 1=PWI should be on Bit 2=CRQ should be on Bit 3=DLO should be on Bit 4=PND should be on Bit 5=DPR should be off Bit 6=COS should be off Bit 7=ACR should be off
X6CE	0X26	Dial on autocall originate line interface	Character service request bit (ICW Bit 1) is not on or PDF is not=00 or any other error bits on.				See comment in error stop 0X09 for register and ICW bit def.
X6CE	0X28	Dial on autocall originate line interface.	No L2 interrupt occurred from autocall or a L2 interrupt occurred from some other line address.				The dial digit was set in PDF, PCF was set to 8. If reg X'14'= 0000 no L2 occurred. If reg X'14' is not all zeros then reg X'14'= addr that caused the level 2.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FRALD PAGE	FETMM PAGE	COMMENTS
X6CE	0X29	Dial on autocall originate line interface	The autocall PCF is not=4 or LCD is not=3 or SDF bits in error.				Reg X'14' byte 0 contains LCD in bits 0-3 and PCF in bits 4-7. Byte 1 contains the SDF and should be =X'F8'. Bit 0=IR should be on Bit 1=PWI should be on. Bit 2=CRQ should be on Bit 3=DLO should be on Bit 4=PND should be on Bit 5=DPR should be off Bit 6=COS should be off Bit 7=ACR should be off
X6CE	0X2A	Dial on autocall originate line interface.	Character service request bit (ICW bit 1) is not on.				Reg X'14' byte 0 = ICW bits 0-7 obtained via an input X'44' from auto call ICW.

The last digit to dial is now in the process of being dialed. If the last digit was not an EON digit then PND may come on if the distant station does not answer immediately. The same thing will occur with EON as last digit on some OEM (non-IBM) and on IBM autocall units that do not have the EON feature strapped on. For some OEM autocall units the EON will cause the autocall unit to transfer control to the modem/data set with Data Set Ready set immediately even though no distant station has been connected and given an answer.

X6CE	0X2E	Dial on autocall originate line interface	SDF autocall interface bits power indicator (PWI), or call request (CRQ) or data line occupied (DLO) are not on.				Reg X'15' byte 1 contains PWI in bit 1 CRQ in bit 2 and DLO in bit 3.
X6CE	0X2F	Dial on autocall originate line interface.	No autocall completion.				Reg X'15' byte 1 bit 0 = 1 if PCF was set to 5. If bit 2=1 then a rec line level 2 interrupt has occurred. If bit 3=1 then the abandon call and retry (ACR) bit is set. If bit 4=1 then a L2 occurred on the autocall line.
X6CE	0X30	Dial on autocall originate line interface.	During 60 second wait for level 2 from auto call line interface after dialing last dial digit a L2 occurred from some line other the auto call line interface address.				Reg X'14'= addr causing the L2. Reg X'16' = addr of auto call line interface the L2 was expected from.
X6CE	0X40	Complete switched connections.	No L2 occurred from switched transmit line address.				'DSR' did not come on and cause a L2 interrupt properly. Reg X'11'= xmit line address L2 was expected from.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X6CE	0X41	Complete switched connections.	The L2 interrupt which occurred while waiting 60 seconds for 'data set ready' to come on was not from the transmit line address.				Reg X'14' = addr that caused the L2. Reg X'11'= transmit line addr the L2 was expected from.
X6CE	0X42	Complete switched connections.	The transmit line LCD and PCF are not valid.				Reg X'45' byte 0 = LCD in bits 0-3 & PCF in bits 4-7. Reg X'15' byte 0 has a bit on for each bit position that is in error in reg X'45' byte 0.
X6CE	0X43	Complete switched connections.	Character service request bit (ICW bit 1) is not on or error if ICW bits 0,2 or 3 are on.				Reg X'14' byte 0 = ICW 0-7. Bits 0-3 are: bit 0 - stop bit check - off Bit 1 - Service request - on Bit 2 - Char overrun/ underrun - off Bit 3 - Modem check - off.
X6CE	0X44	Complete switched connections	No level 2 interrupt occurred from switched receive line address.				Data Set Ready did not come on and cause a L2 interrupt request. Reg X'11'= receive line address.
X6CE	0X45	Complete switched connections.	The L2 interrupt which occurred while waiting 60 seconds for 'data set ready' to come on was not from the receive line address.				Reg X'14'=addr of line causing the level 2 interrupt. Reg X'11' =receive line address the L2 was expected from.
X6CE	0X46	Complete switched connections	The receive line LCD is not valid.				Reg X'45' byte 0= receive lines LCD in bits 0-3.
X6CE	0X47	Complete switched connections.	Character service request bit (ICW bit 1) is not on or ICW bits 0,2 or 3 are on.				See comment for error stop 0X43.
X6CE	0X50	Set mode on transmit line	No level 2 interrupt occurred from transmit line or L2 from wrong address.				If reg X'14'= 0 then no level 2 interrupt occurred. If reg X'14' is not 0000, reg X'14'= the addr that caused the L2. Reg X'45' byte 0= LCD in bits 0-3 and should be equal to what you optioned, and bits 4-7 contains the PCF.
X6CE	0X51	Set mode on transmit line	Transmit line LCD in error or PCF not=0.				Reg X'45' byte 0= LCD in bits 0-3 & PCF in bits 4-7.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X6CE	0X52	Set mode on transmit line	Character service request bit (ICW bit 1) is not on or ICW bits 0,2 or 3 are on.				See comment for error stop 0X43.
X6CE	0X53	Set mode on receive line	No level 2 interrupt occurred or level 2 interrupt was not from the receive line address.				
X6CE	0X54	Set mode on receive line	Receive line LCD in error or PCF not= 0.				Reg X'45' byte 0 = LCD in bits 0-3 & PCF in bits 4-7.
X6CE	0X55	Set mode on receive line	Character service request bit (ICW bit 1) is not on or ICW bits 0,2 or 3 are on.				See comments for error stop 0X43.
X6CE	0X60	Set transmit initial	No L2 interrupt was received from transmit line.				A L2 should occur within 30 seconds after 'CTS' has been brought up by the modem and the first character that was put in SDF is completely transmitted.
X6CE	0X61	Set transmit initial	The interrupt received was not from transmit line address.				Reg X'14' = addr of the interrupting line. Reg X'11' equal the transmit line the L2 was expected from.
X6CE	0X62	Set transmit initial	The transmit LCD is not valid or the PCF is not =9.				Reg X'45' byte 0= LCD in bits 0-3 & PCF in bits 4-7. Reg X'15' byte 0 has a bit on for each bit position is in error in Reg X'45' byte 0.
X6CE	0X63	Set transmit initial	Character service request bit (ICW bit 1) is not on or ICW bits 0,2 or 3 are on.				See comments under code 0X43 for more information.
X6CE	0X64	Wait for character service interrupts	No level 2 interrupt occurred from receive line.				
X6CE	0X66	Wait for character service interrupts	No level 2 interrupt occurred from receive line address.				Reg X'11'= receive line addr L2 was expected from. Reg X'14' = received character count.
X6CE	0X67	Wait for character service interrupts.	No L2 interrupt was received from transmit line address.				Reg X'11'= transmit line address L2 was expected from. Reg X'14' = the transmitted character count.
X6CE	0X68	Wait for character service interrupts	A L2 interrupt occurred from an address other than the transmit or receive line.				Reg X'14' = addr of the interrupting line caused the

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							level 2 interrupt.
X6CE	0X70	Transmit line interrupts	The transmit LCD or PCF is in error.				Reg X'11'= transmit addr. Reg X'15' byte 0= actual (bad) LCD and PCF. Byte 1= expected LCD and PCF.
X6CE	0X71	Transmit line interrupts	The transmit LCD or PCF is in error.				Reg X'15' byte 0= actual (bad) LCD & PCF. Byte 1= the expected LCD & PCF.
X6CE	0X72	Transmit line interrupts	Character service request bit (ICW bit 1) is not on or ICW bits 0,2 or 3 are on.				Reg X'15' byte 0=IC bits 0-7. Bits 0-3 are: Bit 0 = stop bit check. Bit 1 = SVC req Bit 2 = Char overru underrun Bit 3 = Modem check
X6CE	0X73	Transmit line interrupts	More characters have been received than were transmitted.				Reg X'14' =received character count. Reg X'15' = transmitted char count.
X6CE	0X74	Transmit line interrupts	20 more characters have been sent than were received.				See registers in error code 0X73.
X6CE	0X80	Receive line interrupts	Character service request bit(ICW bit 1) is not on or ICW bits 0,2,3 or 4 are in error.				Reg X'14' byte 0 = bits 0-7 of ICW. ICW bits 1 & 4 should be on, bits 0,2 & 3 should be off.
X6CE	0X81	Receive line interrupts	All ones were not received.				Reg X'14' byte 1= received data (PDF) and should be =FF.
X6CE	0X82	Receive line interrupts	More characters were received than was transmitted for wrap options.				Caution: this error will occur if ycu selected a start/ stop wrap option with the wrap all zeros option and with an LCD that causes two stop bits to be sent.
X6CE	0X83	Receive line interrupts	An all zeros character was not received.				Reg X'15' byte 1= actual received cha from PDF. Reg X'16'= received character count.
X6CE	0X84	Receive line interrupts	The wrong character was received				Reg X'15' byte 0= expected receive character. Reg X'15' byte 1= actual received character (PDF). Reg X16' = received character count.
X6CE	0X85	Receive line interrupts	Received a L2 for receive line with the receive all ones options. Should not get any L2 since a S/S LCD is in use and no start bit should be received to cause a level 2.				

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X6CE	0X86	Receive line interrupts for start/stop receive all zeros option.	ICW bit 0 (stop-bit-error) is not on and should be for this receive all zeros option in start/stop mode.				Reg X'16' =received char count. Reg X'14' byte 0 = ICW bits 0-7. Bits 0-4 should be; Bit 0 = Stop bit error on. Bit 1 = SVC req - off Bit 2 = O/U run - off Bit 3 = Modem check - off Bit 4 = Rec-LN-Sig-Det - on
X6CE	0X87	Receive line interrupts	ICW bits 0-4 are in error for DLC receive line.				Reg X'14' byte 0= ICW bits 0-7.
X6CE	0X88	Receive line interrupts	Flag detect bit was on and this is not the 1st character received (this error occurs only if an DLC LCD was selected and a previous flag or data character has been received. If a receive only option then the sending terminal may have sent more than 1 flag character.				Reg X'16'=received character count.
X6CE	0X89	Receive line interrupts	The DLC idle character not received or ICW bits 0-4 are in error.				Reg X'14' byte 0= ICW bits 0-7. Bits 1, 2, 3 should be off. Bits 0 (idle char rec) and 4 (rec-LN-sig-det) should be on. The PDF should = X'1F', X'3F', X'7F', or X'FF'.
X6CE	0X8A	Receive line interrupts	All ones not received using an DLC LCD.				Reg X'16'=received character counter. Reg X'14' byte 1 = PDF receive data.
X6CE	0X8B	Receive line interrupts	DLC LCD is not valid				Rec line LCD has changed to an inval value.
X6CE	0X90	Disconnect line	Autocall LCD not=3 or PCF not = F.				Reg X'45' byte 0 = LCD in bits 0-3 & PCF in bits 4-7. This may be a normal condition if the transmit line connected to the autocall unit has already disconnected and dropped Data Set Ready.
X6CE	0X91	Disconnect line	The scanner display register bits are in error for the transmit line interface.				After a reset the following reg X'46' bits should be off; Bit 0 - CTS. Bit 2 - DSR. Bit 3 - RLSD Bit 5 - DM.
X6CE	0X92	Disconnect line	The transmit LCD is in error or PCF not=0.				Reg x'14' byte 0 = LCD in

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
							bits 0-3 & PCF in bits 4-7.
X6CE	0X93	Disconnect line	The scanner display register bits are in error (receive)				See comment for error stop 0X91.
X6CE	0X94	Disconnect line	Th(receive LCD is in error or PCF not=0.				Reg X'14'= LCD in bits 0-3, PCF in bits 4-7.
X6CE	0X95	Disconnect line	The PCF is still=F after a maximum wait time. This indicates the bits in the SDF for DLO, COS, ACR, or PND did not reset) to cause a normal auto-call disconnect.				Reg X'14' byte 0 = LCD in bits 0-3 PCF in bits 4-7.
X6CE	0X96	Disconnect line.	The LCD is not=3 or PCF is not 0.				Reg X'14' byte 0= L in bits 0-3 & PCF in bits 4-7.

X6D0 XXXX PLOTTER ADAPTER RPQ TEST. This is a manual intervention routine and will not be run unless you set the CE sense switch to run all manual intervention routines or you request a single routine to be run.

Manual intervention stop codes F01E and F01F are used by this routine. These stop codes are listed in chapter 13.5 of this manual.

The diagnostic program will cause the adapter to generate commands for an IBM 1627 type plotter which uses either an encoded interface or an unencoded interface as defined by RPQ#1863250. The routine tests only the ability of the plotter adapter to output commands that will move the plotter properly. The diagnostic routine does not test the plotter, the plotter is only a convenience to the testing.

Plotter commands are issued and the adapter status is checked in the following sequence:

1. The command is transferred to the plotter by first placing the proper bit configuration into the SDF. Figure 1 in the IBM THEORY OF OPERATIONS for RPQ#1863250 shows the meaning and position of the bits that make up a command.
2. The LCD and the PCF are then set to X'3' and X'1' respectively.
3. When the data has been transferred from the scanner to the adapter a level 2 interrupt will occur and the PCF will be set to zero.
4. After the level 2 interrupt occurs, the status of the adapter is placed into SDF bits 1-7 as shown in figure 2 in the IBM THEORY OF OPERATIONS for RPQ#1863250.
5. Before issuing another instruction, the program will turn off the Service Request bit.
6. If no errors occur, the program will continue issuing instructions to draw the pattern shown in figure 3 until the routine is aborted.
7. Whenever an error occurs, register X'11' will contain the line address and the low order byte of register X'13' will contain the command that was issued to the plotter.

X6D0	0X03	Does level 2 interrupt occur after a set mode	A level 2 interrupt did not occur within 12 milli-seconds after issuing a set mode		VB901		
X6D0	0X04	Level 2 interrupt	Level 2 interrupt caused by incorrect line address. Reg X'14' contains address of line that caused the interrupt.				Probable scanner error.
X6D0	0X05	Adapter status	The condition of the adapter and several sense signals from the plotter are checked. Reg X'14' contains the data that was returned to the scanner. Reg X'15' contains the error bits. Reg X'16' contains the expected data.		VB904		See rtn header for a description of adapter status bits and the contents of other registers.
X6D0	0X06	PCF state zero	The PCF was not set to zero after a command was issued to the plotter. Reg X'14' contains				Probable scanner error.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			the current state of the PCF in bits 3-7 of byte 0. Reg X'15' shows the bits in error. Reg X'16' contains the expected data.				
X6D0	0X07	The condition of the adapter and plotter sense signals after the last instruction(X'00') is issued.	See error conditions for error code 0X05.		VB904		See error code 0X05.

X6F0 XXXX SDLC LINK TEST. This routine is a manual intervention routine and will not be run unless you set the CE sense switch to run manual intervention routines or unless you requested a single routine to be run.

This routine will stop with manual intervention stop code F020 through F02C asking you to enter options needed to run this routine. These stop code definitions are listed in the T2CS-MAN section in Chapter 13.5 of this manual.

This routine may be used for SDLC data link problem determination and repair verification when on-line tests (under host system control) are not available.

When using this routine for problem determination external to the 3705, all normal internal functional tests should run normally without internal hardware errors. Any local interface problems, such as line set drivers and terminators, should be tested using routine X6CE with external local wrap options because X6CE provides more detailed information about local failures.

This SDLC link test is basically an ECHO test with the primary SDLC station sending a SDLC link test command frame down the link. The primary station expects get the same test frame back if the remote end of the link received the test frame without errors. Some SDLC terminals only respond with a non-sequenced acknowledgement response rather than sending back the link-test frame it received.

Options are provided to run as a SDLC primary station or as a SDLC secondary station. The primary station option initiates the link-test commands and expects to receive responses. The secondary SDLC station responds to test-frames received; if the test frame was received without errors, the same test frame is sent back as a response. If a test frame was received without block check errors and had either more data than could be buffered or did not have the poll bit on in the control field, the secondary station responds with a test frame without optional data. All frames received with block check errors or with abort detect conditions are counted as errors and no response is provided. All frames received with a SDLC station address other than the SDLC station address selected in the F028 manual intervention stop code are counted as an unexpected or non-supported frame and no response is provided. No response is provided for frames with anything but a link-test command field.

The structure of the link-test command enables this test to also run a local external duplex modem wrap if you select the primary station option and connect the transmit and receive lines together properly. A remote wrap can be done if the remote end of the link can tie the transmit and receive duplex lines together with proper loading etc. Because the remote end of the link must store the test frame and send it back, the wrap option does not work on half-duplex lines.

This routine always stops on transmit errors such as modem check, timeout, or overrun, but does not stop on receive errors except for modem check error unless an option is selected to stop on frames in error or stop on any frame.

Continuation (select FUNCTION 5 and press START key) from the 0X20, 0X60 or 0X61 stops the routine clears all error counts and summary statistics and restarts the test from the transmit/receive data portions. This allows continuing the test on a manual switched line connection without making a new connection. The same restart is used for the D000 dynamic restart option or the D000 restart option at stop code F02C. Any manual switched line connection will not be broken until you abort the routine or use a restart option that goes through total hardware setup such as D002 restart code.

X6F0 ---- The format of all transmissions from this LINK-TEST are:

Pad Pad F A C dd BC BC F ee

where-

Pad = alternate data transitions characters for clock correction and will be X'AA' if NRZI mode is not being used or X'00' if NRZI mode is being used.

F = SDLC flag character composed of a zero bit followed by six one bits followed by another zero bit(X'7E').

A = SDLC station address.

C = SDLC control field and will always be X'F3' if a LINK-TEST command/response is being sent or X'97' if a command reject response is being sent.

ROUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

dd = Optional transmit/receive data field when the LINK-TEST command is being used. When the command reject response is being sent the first byte of this field is the command field of the received frame that is being rejected, the second byte is set to zeros (it is defined as the send and receive sequence counts) and the third byte is set to X'04' if more data was received then could be buffered or to X'01' if the LINK-TEST command was received without the poll bit on.

BC = block check(CRC) characters. Two block check characters are always sent and their bit configuration vary according to the SDLC station address, control field and optional data fields.

ee = an ending transmission of X'FF' to make line go to an idle state and to allow time for bits to be sent before dropping the 'request to send' lead on transmit turnarounds.

All the data defined above between the two flag characters is defined as a FRAME. All references in this document to the frame refers to this portion of each transmitted or received segment of data. Note that if the above is being sent/received in NRZI mode then the actual bit configuration on the line will differ from the ones shown above. Also, SDLC zero bit insertion/deletion applies to all characters except the flags and ending sequence defined under ee.

Test statistics and error count are available while the test is running and at the F02C test completion code. In addition certain registers are used for current status indicators and may be displayed while the test is running or at the F02C stop code. Following is the definition of the status indicators:

X6F0 ---- X'1E' register contains the current transmit and receive line status.

Byte 0 of reg X'1E' = last received frame type indicator and may contain one of the following indications:

X'00' = Timeout occured on last receive completion.

X'80' = A good link test frame was received with no errors.

X'40' = A command reject response was received as the last frame received at this primary station.

X'20' = A non-sequenced acknowledgement was received as the last frame at this primary station.

X'10' = A block check (CRC error) was detected in the last received frame.

X'08' = An invalid or non-supported frame was received as the last received frame. This link test only supports the link-test response, the non-sequenced acknowledgement response and the command reject response if running as a primary station. The secondary station option will only accept a link-test command but may respond with a link-test response or a command reject response. This type indicator is also set if a partial frame was received followed by an 'abort detect' sequence of seven or more consecutive one bits.

X'04' = A valid link-test frame was received but it contained more data than could be buffered. If this is a secondary station, a command reject response is sent for this frame. The maximum length of the receive(and transmit) data buffer is 1024 characters if this 3705 has more than 16K storage or 10 characters if 3705 has only 16K of storage.

X'02' = Invalid SDLC station address received or, for primary station option with optional transmit data, the received data did not compare with the SDLC station address or optional transmit data that was sent. The SDLC station address that you provide in the F028 stop code is used to make this comparison. If the secondary station option was selected, this frame will not be responded to.

X'01' = A hardware detected error such as modem check or overrun has been detected. No response is made to any frames received with this type of error.

Byte 1 of reg X'1E'= transmit line status and other information bits. Multiple bits may be on in this byte as opposed to byte 0 which never will have more than one bit on.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

The bits within this byte are defined as:

X'80' = A reply is pending to be sent to the last frame received at this secondary station.

X'40' = A command reject reply is now being sent or was the last frame transmitted from this secondary station.

X'20' = A link-test command(from primary station) or response(from secondary station) was the last frame sent or is being sent at this time.

X'10' = A 'transmit initial' operation is being done or was last transmit operation done. This 'transmit initial' is done to set 'request to send' and wait for 'clear to send' from the modem interface for the first transmit operation of all primary station options and for secondary station options when 'request to send' should be on at all times. See manual intervention stop code F020 for this option.

X'08' = Transmit line is busy if this bit is on.

X'04' = Receive line is busy if this bit is on.

X'02' = Bit not defined. May be used as added indicator at later time.

X'01' = Bit not defined. May be used as added indicator at later time.

X6F0 ---- X'1F' registers contains the accumulated transmit and receive line status indicators. The bits in this register have the same meanings as the bits defined in the register X'1E' except once these bit are set on they are not reset until the test is restarted. These bits serve as a summary of all the transmit and receive operations that have been done up to the time this register is displayed.

X6F0 ---- X'1D' register is used to control the E0?? display code that is put out to the panel display B lights (if function select switch is in positions 4, 5 or 6). This register is cleared to zeros at approximately two second intervals and in between this clearing to zeros it is used as an accumulator of all the bits defined in the register X'1E' bits.

X6F0 ---- X'46' register is the scanner display register. This program sets the display bit in the ICW for the receive line used in this test. For half-duplex lines this register gives you the current line interface conditions for both the transmit and receive operations. For duplex lines this register contains the receive line interface conditions. Following is bit definition for byte 0 of this register.

Bit	Hex	Meaning if bit is on.
0	80	'clear to send' is active. Should be on while in transmit mode and may be on while in receive mode. For duplex lines this bit probably will not be on since it reflects the status of the receive half of the duplex pair.
1	40	'ring indicator' is active.
2	20	'data set ready' is active. Should be on for leased lines and should come on after line is connected for switched lines.
3	10	'receive line signal detect'(carrier detect) is active. Should be on while receiving and may be on while transmitting.
4	08	'receive data bit buffer' is a one bit. Should vary as received data varies.
5	04	'diagnostic mode bit' is on. Should not be on in this test.
6	02	'bit service request bit' is . Should be on once each bit service.

X6F0 ---- E0?? display codes. While the link-test is running, various display codes are displayed in display B if you have the FUNCTION SELECT SWITCH in function position 4, 5 or 6 (except E06F). These display codes are displayed approximately once every other second with the display B lights cleared to zero between each E0?? display. These E0?? display codes are defined as:

E000 alternating with E0FF = waiting for 'data set ready' to come on before doing any transmit or receive operations. These codes will be continously displayed until 'data set ready' comes on via completing a manual switched connection or via connecting (or jumpering) the proper modem interface leads. On a leased line connection you will not see this display code if 'data set ready' is always on(as expected).

E060 = A good test frame was received within the last two seconds and no other error was detected (except a possible timeout).

E061 = Nothing was received(timeouts) during the last two seconds.

ROUT. CODE	ERROR FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

E062 = A block check error(CRC error) was detected in some frame during the last two seconds.

E063 = A non-supported or invalid frame was received during the last two seconds.

E064 = More data was received than could be buffered during the last two seconds.

E065 = A command reject response was received at this primary station during the last two seconds.

E066 = A non-sequenced acknowledgement was received at this primary station during the last two seconds.

E067 = Either of 3 Conditions may exist:
1 - SDLC Station Address did not compare.
2 - Received data did not compare with transmitted data.
3 - Secondary Station received more data than could be buffered.
In all cases 'E067' indicates that the data received does not compare with data transmitted.

E068 = A hardware detected error such as modem check or overrun has been detected during the last two seconds.

E06F = This code is displayed if you are using the dynamic communications option (function select 1 and switches B-E set to D0??) and have entered a D0?? code that is not defined. No action is taken if this code is displayed.

X6F0 ---- D0?? dynamic communications codes. These dynamic communications codes allow you to terminate or restart the link-test at various points within the test. You enter these codes while the program is running by setting the DISPLAY/FUNCTION SELECT SWITCH to function position 1, by setting the selected code in switches B-E and then pressing the interrupt key on the control panel. These dynamic communication options are the same as those defined in the F02C manual intervention stop code definition. They are repeated here in a summary form. For more details see the F02C stop code definition.

D000 = Restart link-test at transmit/receive data point(no line resets).

D001 = Restart routine from beginning including asking for options.

D002 = Restart link-test including hardware resets and enables.

D003 = Stop routine at F02C stop code and display statistics.

D004 = Terminate routine after hardware resets.

X6F0 ---- STATISTICS at link test termination.

X'1C' register contains the address of a statistics table in storage. At all times while the test is running and at the F02C and 0X?? stop codes you may get the storage address of the statistics table from this register and display the storage locations for the following half-word counters. Following is a list of what is available in these statistics:

Hex displacement
within statistics
pointed to by
reg X'1C'.

00 = Number of SDLC link-test frames transmitted successfully. This count does not include command reject responses sent from a secondary station.

02 = Number of SDLC link-test frames received with no errors. If this is a primary station then the received SDLC station address and(if used) the optional data must compare in order to have one added to this count. On a normal F02C completion at a primary station this count should match the number of test frames transmitted count if no errors have been detected. An exception is when the secondary station responds with non-sequenced acknowledgements to test frames then this count should be zero and the received non-sequenced acknowledgements count should match the number of test frames transmitted count.

04 = Number of frames received with block check errors(CRC errors).

06 = Number of command reject responses received at this secondary station.

08 = Number of non-sequenced acknowledgements received at this secondary station.

0A = Number of frames received that were not included in other receive counts. This count includes frames received with invalid SDLC station addresses,

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		non-supported commands/responses, non-data compares with optional transmit data and frames terminated by an abort detection condition. Note that some of these conditions may have caused a block check error and be included in the block check error count and not this count.					
		0C = If primary station then this field contains number of test frames requested to be sent in the F022 stop code. If this field is all zeros and a primary station option was selected then test frames will be sent continously (allowing for receiving etc) without ever terminating the test.					
		0E = Number of hardware errors detected, such as modem check or overruns, on the transmit and receive operations.					
		10 = Number of command reject responses transmitted by this secondary station.					
X6F0	----	Following are the error stop codes that may occur in this test. Note that any error stop codes beginning with 1 or 2 in display B byte 0 bits 0-3 are defined in another section of this symptom index. The display B codes starting with F are defined in the manual intervention section of this document.					
X6F0	0X07	Auto call failed to complete	An auto call error has been detected. Reg. X'15' byte 0 contains an error indicator number. Determine error indicator and see description below. ERROR INDICATOR 1 -- Error in auto call connection. Reg.X'15' byte 1 contains SDF bits in error. SDF bits 0-4 on, 5-7 off. Also an error, if LCD not=3, PCF not=4 (reg. X'45' byte 0). 2 -- Error in dialing. See error indicator 1 description. 4,5&6 -- If last digit dialed was not an EON digit, PND may come on an cause a L2 interrupt if the distant station does not answer immediately. The same thing will occur with EON, as last digit, on some EOM (non-IBM) and on IBM auto-call units that do not have the EON feature strapped on. On some EOM auto-call units the EON will cause the auto-call unit to transfere control to the modem/data set with DATA-SET-READY on immediately, even though no distant station has been connected and given an answer tone. 4 -- Error indicating PWI, CRQ or DIO not on. Reg. X'15' byte 1 bits 1,2 & 3 should be on. 5 -- No auto-call completion (timeout). Reg. X'15' byte 1 bit 6 (COS) should be on. 6 -- Abandon-call and retry came on. Reg. X'15' byte 1 bit 7 came on.				Reg.X'15' byte 1= SDF bits 0-7. SDF bit definitions for auto-call are: Bit 0= (IR) intrpt remember. Bit 1= (PWI) power indicator. Bit 2= (CRQ) call request. Bit 3= (DLO) data line occupied. Bit 4= (PND) present next digit. Bit 5= (DPR) digit present. Bit 6= (COS) call originate status. Bit 7= abandon call and retry.
X6F0	0X20	Transmit line operations.	A transmit line error has been detected. Reg X'13'=accumulated ICW bits 0-15 during this transmit operation. On each level 2 interrupt ICW bits 0-7 are stored together and saved for this error display. If reg X'15' byte 0 bit 3(X'10') is on then the transmit line has timed out due to 'clear to send' not coming on or due to some other transmit failure such as loss of transmit clock.				See routine heading for more registers and error stats. If continuing from this error stop by selecting FUNCTION 5 and press START the test restarts at the transmit/ receive portion without hardware reset and enable. This error may be found more easily in routine X6CE.
X6F0	0X60	Receive error completion.	This error stop occurs if a modem check has been detected (ICW bit 3 on) while in receive				See Rtn heading for test run details, registers and test

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
			mode or this stop occurs if you selected the options to stop on any frame or any frame in error. Reg X'13'=ICW bits accumulated during this receive operating by storing ICW bits 0-7 together and saving them on each level 2 interrupt. Note that program does not stop on receive timeouts but setups to transmit again if a primary station or to receive again if a secondary station. Reg X'16'= address of receive data buffer in storage and reg X'19'=adr+1 of last received character. Note that regs defined in routine heading provide more information.				statistics. To continue from this stop select FUNCTION 5 and press START, the test restarts at the transmit/receive portion of the test without the hardware resets and enables.
X6F0	0X61	Receiving frames.	This stcp code occurred because you selected an option to stop on the type of frame just received. Reg X'1E' defines type of frame received and is defined in the routine heading. Reg X'16= adr of start of receive data buffer. Reg X'19'=adr+1 of last character received (less block check chars). Reg X'14'=accumulated block check (CRC) characters accumulated by this program and should = X'F0B8' if no errors occurred. Reg X'13'=last two received characters(prior to flag char) and should be the actual received block check (CRC) characters.				See routine heading for regs. & test statistics. To continue , select FUNCTION 5, press START, program restarts at the transmit/ receive data portio of the test without hardware resets and enable operations but clears the stat counters.

X6F2 XXXX Wrap Data Test - BSC and SDLC. This is a manual intervention wrap routine and runs only if you set the CE sense switch to run manual intervention routines or request a single routine to be run.

At the first manual intervention stop X'F049' enter the desired options:

SWITCH
B C D E

0 - - - first oscillator
1 - - - second oscillator
2 - - - third oscillator
3 - - - fourth oscillator
4 - - - data rate select (turns on break if line set 12A or 12B)
8 - - - external clock
- 0 - - no request
- - 0 0 no request
- - 0 1 transmit without a receive line (no wrap)
- - 0 2 transmit and receive, swap lines and repeat
- - 0 3 transmit and receive same pair

At stop F050 enter a valid transmit line address and wrap type operator.

BSC SWITCHES B C D E	SDLC SWITCHES B C D E	
5 X X X	D X X X	Normal (DTR/NOT DM) An external wrap facility must be provided to wrap data with this option
6 X X X	E X X X	Line Set Wrap (DM/NOT DTR)
7 X X X	F X X X	Modem Wrap (DM/DTR) For modems that use the Modem Wrap signal

At stop F052 enter a valid receive line address and wrap type operator in the same format as in stop F050.

X6F2	0X01	A set mode was executed on the receive line (Addr in register X'13')	Either the expected L2 did not occur or the wrong line interrupted. Register X'14' contains the interrupting line address.				The reference data for this test is variable and is not given.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X6F2	0X02	The LCD of the receive line was checked for a feedback check.	A feedback check occurred in the setmode to the receive line.				
X6F2	0X03	A setmode was executed on the transmit line (Addr in register X'11')	Either the expected L2 did not occur or the wrong line interrupted. Register X'14' contains the interrupting line address.				
X6F2	0X04	The LCD of the transmit line was checked for a feedback check.	A feedback check occurred in the setmode to the transmit line.				
X6F2	0X06	The modem should cause clear to send to come up on the transmit line after approximately 300ms.	The transmit line display register did not contain the clear to send bit.				
X6F2	0X07	The modem should cause data set ready to come up on the transmit line.	The transmit line display register did not contain the data set ready bit.				
X6F2	0X10	An interrupt was expected from either the transmit or the receive line. The test is transmitting and receiving (if receive is selected).	Neither the transmit nor the receive line interrupted or an unexpected line interrupted. Register X'14' contains the address of the interrupting line address or zero if no line interrupted.				
X6F2	0X13	The transmit and receive should interrupt for service each character time.	The receive line has not interrupted after at least 20 transmit line interrupts.				
X6F2	0X15	Checking input X'44' for correct flags set.	Flags set in SCF during the receive were not set properly. Register X'15' contains the address of the flags and data received.				
X6F2	0X16	Checking data received against the data expected.	The data received is not equal that expected. Reg X'15' byte one is the data received, byte two is the data received. Reg X'17' points to the expected byte, Reg X'16' points to the received data; SCF flags in byte 1 at addr pointed to by Reg x'16'.				

X6F4 XXXX X.21 LINE SET TEST

This is a manual intervention routine and runs only if directly selected or the CE sense switch is set to run manual intervention routines.

This routine tests the X.21 Line Sets unique handling of Data Set Ready and Clear to Send. If the switch option is specified, the bit pattern generator and state generation circuits are also tested. The transmit and receive lines must be wrapped (transmit T and C signals connected to the receive R and I signals respectively) via an external facility. Refer to FETMM Page 1-330 for wrap test block information.

Most of the tests are performed on the transmit line with the results being checked on the transmit and/or receive lines. This routine should be run twice on a half duplex pair, reversing the addresses specified as the transmit and receive lines the second time.

Data is not explicitly wrap by this routine. Use routine X6F2 for this purpose and to further verify the line set and external wrap connection.

Refer to logic page VA017 for the jumper information. The following manual intervention stops occur.

At stop F055, enter the routine options as follows:

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS

SWITCH
B C D E

X Y Z 2 2400 BPS Jumpers are in delay position
X Y Z 3 2400 BPS Jumpers are in no delay position

X 8 Z 4 4800 BPS Jumpers are in delay position
X 8 Z 5 4800 BPS Jumpers are in no delay position

X 8 Z 6 9600 BPS Jumpers are in delay position
X 8 Z 7 9600 BPS Jumpers are in no delay position

X 8 Z 8 48K BPS Jumpers are in delay position
X 8 Z 9 48K BPS Jumpers are in no delay position

where x = 0 If the routine is not to be looped without respecifying the manual input.
= 1 If the routine is to be looped without respecifying the manual input.

y = 0 If internal 2400 BPS clock is to be used.
NOTE: This option is only valid for 2400 BPS.
= 8 If external clock is to be used.

z = 0 If the line set is jumpered for non switched half duplex operation.
= 1 If the line set is jumpered for switched opertion.
= 2 If the line set is jumpered for non switched full duplex operation.

At stop F056, enter the transmit line address.

SWITCH
B C D E

0 X X X XXX is the transmit line address as defined in the F001 manual intervention stop code.

At stop F057, enter the receive line address.

SWITCH
B C D E

0 X X X XXX is the receive line address as defined in the F001 manual intervention stop code.

At stop F059, disconnect the external wrap facility. This stop code will be bypassed if the loop option was specified in response to stop code F055.

Error stops in this routine, except for the set mode pretest errors (1X03 and 1X04), are most likely caused by failures in the line set cards, if the other type 2 scanner routines have run successfully. Refer to logic page VA000 for line set card locations. Any one of the three cards of the line set could be causing the error as no attempt is made by this routine to isolate failures any further.

X6F4	0005	DTE controlled not ready state.	12 bit times after the receive line was initialized an alternating bit pattern was not detected in the SDF.				

NOTE: Error 0005 will only occur if switched and external clock options are specified.

X6F4	0007	DTE ready state	10 bit times after DTR was set on the transmit line all 1's were not detected in the SDF of the receive line.				
X6F4	0008	DSR active on the transmit side.	DSR on the transmit side was not active.				

NOTE: Error 0008 will only occur if non switched duplex or switched option is specified.

X6F4	0009	DSR active on the receive side.	DST on the receive side was not active.				
X6F4	000B	DSR on the receive line stays active at least 12 bit times after diag mode is set on the transmit line	DSR became inactive on the receive line too soon after diagnostic mode was set on the transmit line.				
X6F4	000C	DSR on the receive line becomes	DSR on the receive line was still active				

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		inactive 22 bit times after diag mode is set on the transmit line	22 bit times after diagnostic mode on the transmit line should have forced C and T and therefore I and R on the receive side to 0's.				
X6F4	000D	A bit pattern for a SDLC flag is generated on the receive line after DSR becomes inactive.	A SDLC flag bit pattern was not detected in the SDF within 20 bit times after DSR became inactive.				
		NOTE: Error 000D will only occur if the switched option was specified.					
X6F4	000E	A bit pattern for an USASCII SYN is generated on the receive line after DSR became inactive.	An USASCII SYN bit pattern was not detected in the SDF within at least 20 bit times after the SDLC flag bit pattern was detected.				
		NOTE: Error 000E will only occur if the switch option was specified.					
X6F4	0012	All marks generated by the transmit line and received when diagnostic mode is reset and data terminal ready is set on the transmit line. Data rate select is also set at this time, but it should have no effect because Request to Send is off.	All marks were not detected in the receive line's SDF 10 bit times after the set mode interrupt from the transmit line.				
X6F4	0013	I is inactive on the receive line when Request to Send is inactive on the transmit line.	I is active on the line before Request to Send (T) has been activated on the transmit line.				
X6F4	0015	Clear to Send is inactive on the transmit line when Request to Send is inactive on the transmit line.	Clear to Send is active on the transmit line before Request to Send has been activated on the transmit line.				
X6F4	0018	I becomes active on the receive line when clear to Send is activated on the transmit line.	I did not become active on the receive line after Request to Send was activated on the transmit line.				
X6F4	0019	Clear to Send delay	Clear to Send became active less than 21 bit times after Request to Send was set in the line set (I detected on the receive line).				
		NOTE: Error 0019 will only occur if the delay option was specified.					
X6F4	0020	Clear to Send becomes active after Request to Send is activated	Clear to Send did not became active within one scan time with no delay, 31 bit times with delay after Request to Send was set in the line set (I detected on the receive side).				
X6F4	0021	Call Request state	All 0's were not detected in the receive line's SDF when Request to Send, Data Rate select, and Data Terminal Ready are on in the transmit line.				

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		NOTE: Error 0021 will only occur if the switch option was specified.					
X6F4	0022	Data Set Ready stays active on the transmit line when I is active and the receive data line is held at space for at least 20 bit times.	Data Set Ready became inactive on the transmit line while a continuous space was being received when I was active (Request to Send active on the transmit line).				
		NOTE: Error 0022 will only occur if the non switched duplex or switched option is specified.					
X6F4	0023	Data Set Ready stays active on the receive line when I is active and the receive data line is held at space for at least 20 bit times.	Data Set Ready becomes inactive on the receive line while a continuous space was being received when I was active (Request to Send active on the transmit line).				
X6F4	0025	DSR stays active on the transmit line at least 12 bit times after diag mode is set on the transmit line.	DSR became inactive on the transmit line too soon after diagnostic mode was set on the transmit line.				
		NOTE: Error 0025 will only occur if the non switch duplex or switch option is specified.					
X6F4	0026	DSR becomes inactive on the transmit line 22 bit times after diag mode is set on the transmit line	DSR on the transmit line was still active 22 bit times after diagnostic mode on the transmit line should have forced C and T and therefore I an R on the receive side to 0's.				
		NOTE: Error 0026 will only occur if the non switch duplex or switch option is specified.					
X6F4	0027	DSR becomes inactive on the transmit line when the external connection is broken	Data Set Ready did not become inactive on the transmit line when the external connection was unplugged.				
		NOTE: Error 0027 will only occur if the non switch duplex or switch option is specified.					
X6F4	0028	DSR becomes inactive on the receive line when the external connection is broken	Data Set Ready did not become inactive on the receive line when the external connection was unplugged.				

X6F5 XXXX High Speed Local Attachment Oscillator Speed Test. This manual intervention routine checks the 14.4KHZ/57.6KHZ high speed oscillator that is supplied for the High Speed Local Attachment Line features. The frequency to be checked must be jumpered on the LIB type 1 board in which the oscillator is installed. See the following switch entry specifications for the jumper information. The oscillator frequency is checked to ensure that there is not more than a plus or minus 0.1 percent variation from its expected frequency.

The oscillator frequency and the line that it is to be checked on are entered in the Address/Data switches at stop code F058 as follows:

SWITCH
B C D E

0 X X X 14.4KHZ test on line XXX (Jumper on pin side A2G4B07 to A2G4B05)
1 X X X 57.6KHZ Test on line XXX (Jumper on bin side A2G4B07 to A2G4B09)

Where XXX is the line address as defined in the F001 manual intervention stop code.

The oscillator frequency is determined by the number of bits shifted in the SDF versus the number of times through a program loop. The SDF is set to X'01FE' and a bit count and program loop count are initialized. Each time through the loop, the loop count is decremented by one and the low order SDF bit is checked. When the low order SDF bit is one, the SDF is reinitialize to X'01FE' and the bit count is decremented by one. If loop count is decremented to zero before the bit count, the residual bit count is compared to 0.1 percent of its initial value. If the bit count is decremented to zero before the program loop count, the residual program loop count is compared to 0.1 percent of its initial value.

This routine indicates failures if:

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
		1. The frequency selected in Address/Data switch B does not agree with the frequency selected by the jumper on A2G4. 2. The oscillator card is defective. 3. External Oscillator select bit in the line set fails to set. 4. Oscillator gating controls are defective.					
X6F5	0X01	Set mode to set external clock.	No level 2 interrupt occurred.	A3L2 A3T2 A3T4 A3U2 A3U4	TA611 TB411 TB412 TB413 TB414	C-020 C-160	Reg X'11' contains the line address the level 2 interrupt was expected from.
X6F5	0X02	SDF shifting.	SDF bit 9 did not set to 1 in the approximate 180 millisecond wait time.	A3L2 A2G4	TA611 VA070	C-020	SDF bits 1,2,3,4, and 5 were set via an output X'46' with X'01F0'. Regs X'14' and X'13' contain the state of the ICW bits 2.0-5.7 at the end ofthe wait time. Reg X'14' contains the SDF Bits 0-7 in byte 1. Reg X'13' contains SDF bits 8&9 in 0.0-0.1 and external clock bit in 1.7.
			X6F5 too fast. The bit count decremented to zero before the program loop count was decremented below 0.1 percent of its intial value.	0X03 A2G4	Oscillator frequency VA070		Oscillator under t the residual loop count. Reg X'16' contains the initial loop count.
X6F5	0X04	Oscillator frequency.	Oscillator under test running too slow. The program loop count decremented to zero before the bit count was decremented below 0.1 percent of its initial value.	A3L2 A2G4	TA611 VA070	C-020	Reg X'14' contains the residual bit count. Reg X'16' contains the initial bit count.

X6F6 Type 2 Scanner Modem CHECK test Routine.

ROUTINE DESCRIPTION

X6F6 XXXX Modem Check Test. This routine is a manual intervention routine and will not run unless you set the CE sense switch to run manual intervention routines, or unless you requested a single routine to be run. It is intended to test only lines attached to the scanner that has RPQ S30254 installed.

This routine checks that the modem check causes a level 2 interrupt. This test is run with 'request to send' off and diagnostic wrap mode off.
Refer to the 3705 PRINCIPLES OF OPERATION and/or 3705 FETMM for a detailed description of MODEM CHECK. (SCF bit 3).
This routine stops with manual intervention codes of F0-- in display B, asking you to enter the information required to run this routine.
These F0-- codes may be found at the end of this symptom index for the type 2 communication scanner IFT.

STOP CODE

X6F6 F001 This stop occurs at the beginning of the routine to allow input to the test routine the address of the line to be tested. See this manual intervention stop at the end of index for type 2 scanner.

X6F6 F00A This stop occurs at the beginning of the routine to allow input to the test routine the lcd of the line to be tested. See this manual intervention stop at the end of index for type 2 scanner.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X6F6 0X01 A3S2 TA881 B300 and RPQ S30254
Theory of Operation

An output of 00X1 was issued to reg 45. (x = lcd)
A level 2 Interrupt did not occur after set mode.

ERROR CODE	CARD	FEALD	FETMM LOCATION	PAGENO	PAGENO
X6F6	0X02	A3S2	TA881	B300 and RPQ S30254 Theory of Operation	

An output of 00X7 was issued to reg 45. (x = lcd)
A level 2 Interrupt did not occur after set receive operaton.

ERROR CODE	CARD	FEALD	FETMM LOCATION	PAGENO	PAGENO
X6F6	0X03	A3L2	TA611	B300	

An output of 00X7 was issued to reg 45. (x = lcd)
A level 2 Interrupt did not occur from address expected.
Reg 15 = address from reg 40.
Reg 14 = address expected.

ERROR CODE	CARD	FEALD	FETMM LOCATION	PAGENO	PAGENO
X6F6	0X04	A3S2	TA881	B300 and RPQ S30204 Theory of Operation.	

An output of 00X7 was issued to reg 45. (x = lcd)
A level 2 Interrupt occured, but either modem check was not set or service request interlock was set.
Reg 15 = bits in error from reg 44
Reg 14 = input from reg 44.

LAST PAGE OF TYPE 2 SCANNER IFT SYMPTOM INDEX

CHAPTER 6.2: TYPE 2 COMMUNICATIONS SCANNER COMMON ERROR STOPS

TYPE 2 COMMUNICATIONS SCANNER INTERNAL FUNCTIONAL TEST SYMPTOM INDEX -
COMMON SUB-ROUTINE AND LEVEL 1, 2 AND 3 CODES.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X6XX	1X01	Configuration Data Set	CDS indicates it is not for the Type 2 Communication Scanner, or has an invalid scanner number in its scanner type and number field.				Register X'16'= storage address of the scanner control block within the CDS that is in error.
X6XX	1X03	SET MODE.	THE L2 interrupt that occurred during set mode was not from the expected line address. This is a pretest error so if you use the continue function(function 5) then the set mode will be tried again.			TA611 B-260	Reg X'14'= line address (as used to set ABAR) of the ICW that interrupt in error. Reg X'11'= the line address that the level 2 was expected from. If reg X'14'=0000 no L2 occurred.
X6XX	1X04	SET MODE.	A feedback check occurred setting the LCD field of the ICW to X'F'. This is a pretest error so if you use the continue function(function 5) then the set mode will be tried again.	A3E2		TA341 B-260	REG X'11'= line address (as used to set ABAR) of the scanner-LIB-line interface address that the set mode is being done on at this time.
X6XX	1X05	SET MODE.	Missing the level 2 interrupt expected within 1 bit time after doing the set mode. This is a pretest error so if you use the continue function(function 5) the set mode will be tried again.	A3L2		TA611 B-310	REG X'11'= line address (as used to set ABAR) of the line set that the set mode is being done on.
X6XX	1X06	Configuration Data Set.	An invalid LIB type is defined for the scanner being tested.				Reg X'15' byte 0= the invalid LIB type found in the CDS. Reg X'11'=addr (as used to set ABAR) for the scanner/LIB interface address.
X6XX	1X07	Configuration Data Set.	An invalid line set type is defined for the line being tested. Reference the CDS description in the previous chapters of this document.				Reg X'15' byte 1= the invalid line set type found in the CDS. Reg X'11'=line address being checked.
X6XX	2X01	All functions not expecting or causing L1 interrupt.	Unexpected L1 interrupt occurred with no CCU or adapter L1 error bits on.	A3C2		TB131 6-082	
X6XX	2X02	All functions not expecting a L1 interrupt or causing a level 1 interrupt.	Unexpected L1 interrupt occurred indicating a type 2 scanner level 1 error.	A3C2		TB131 B-130	REG X'76' contains adapter interrupt group 1 error bits.
X6XX	2X03	All functions not expecting or causing a L1 interrupt.	L1 adapter (TYPE 2 SCANNER) interrupt occurred with no scanner error Reg X'43' bits on for the scanner causing this error.	A3C2		TB131 B-130	
X6XX	2X04	All functions allowing adapter L1 interrupts.	cannot reset type 2 scanner adapter L1 interrupt bits.	A3C2		TB131 B-130	Reg X'76' contains adapter interrupt error bits.
X6XX	2X05	ALL FUNCTIONS.	AN INPUT/OUTPUT CHECK CAUSED by a valid input or output instruction.	A3C2		TB131 B-290	REG X'74' CONTAINS address of the valid input or output instruction.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(S)	FEALD PAGE	FETMM PAGE	COMMENTS
X6XX	2X21	All functions not expecting L2 interrupts but allowing L2 interrupts to occur.	Unexpected level 2 interrupt occurred.	A3L2	TA611	6-082	
X6XX	2X33	All functions.	An unexpected level 3 interrupt occurred with no L3 interrupt request bits on.			6-082	
X6XX	2X44	ALL FUNCTIONS.	L4 UNEXPECTED REENTRANCE. The DCM gives control to all routines with L4 PCI bit on (Reg 7F byte 0 bit 7 on). This bit should never be turned off and should never exit L4 except to L1, L2, and L3 which are higher priority.			6-082	
X6XX	E0XX	Display information.	This display is for information only. The XX after the E0 is the LIB and line address now under test unless otherwise specified in the routine write up.				This E0XX display is to let you know that the routine is running.

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F001 Enter the line address to be tested. Set switches B, C, D and E to 0000 to test all addresses, and set to FFFF to bypass all testing. Otherwise, enter the line address as used to set ABAR. See IBM 3705 Communications Controller Theory Maintenance Manual, SY27-0107, Page B-330 for a chart on all valid line addresses. Some routines will not accept the 0000 switch settings to test all installed line addresses and in that case you will get another manual stop code saying an invalid line address was selected.

To continue from manual intervention stops set the required information into the STORAGE DISPLAY/DATA ADDRESS SWITCHES B, C, D and E: set the DISPLAY/FUNCTION SELECT SWITCH to function and press the start switch. Following is the format to enter the line address.

	Hex
Switch B =	0

	Hex
Switch C =	0 for 1st scanner address bits. 1 for 2nd scanner address bits. 2 for 3rd scanner address bits. 3 for 4th scanner address bits.

	Hex
Switch D =	4 for 1st LIB, lines 0-7 5 for 1st LIB, lines 8-F 6 for 2nd LIB, lines 0-7 7 for 2nd LIB, lines 8-F 8 for 3rd LIB, lines 0-7 9 for 3rd LIB, lines 8-F A for 4th LIB, lines 0-7 B for 4th LIB, lines 8-F C for 5th LIB, lines 0-7 D for 5th LIB, lines 8-F E for 6th LIB, lines 0-7 F for 6th LIB, lines 8-F
Switch E =	0 for lines 0 or 8 2 for lines 1 or 9 4 for lines 2 or A 6 for lines 3 or B 8 for lines 4 or C A for lines 5 or D C for lines 6 or E E for lines 7 or F

F002 Invalid scanner address bits were entered in switch C. Re-enter the line address as in stop code F001.

F003 The selected scanner is not installed or not configured properly in CDS. Reg X'16' contains the address of the scanner block for the requested scanner. If reg X'16'=X'0000', the scanner is not configured. Re-enter the request as in stop code F001.

F004 Invalid LIB address selected. Re-enter the request as in stop code F001. (Only 4 LIBs are allowed in the first scanner.)

F007 The selected line address is not installed according to data in the CDS. This routine requires a line adapter to be installed to run tests. Re-enter the line address as in stop code F001.

F008 This routine cannot run tests on the LIB or type of line adapter for the line address selected. Re-enter the line address as in stop code F001.

F00A Enter the LCD of the line to be tested. Set switches B, C, D and E to 000x where x is the lcd for the line to be tested.

See 3705 RPQ S30254 THEORY OF OPERATION P/N 7838753 for definition of lcd jumpered in card P/N 6173443.

F01E Enter the plotter type in the STORAGE ADDRESS/DATA SWITCHES B, C, D and E.

B	C	D	E	switches
0	5	0	0	For unencoded plotter attachment.
0	7	0	0	For encoded plotter attachment.

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F01F An invalid plotter type code was entered in stop code F01E. Re-enter plotter type code as defined in the F01E stop code.

F020 Enter the link test line type and control options. Primary station option initiates link-test, secondary station option only responds to link-test command received from a remote primary station.

'RTS'=on means that 'request to send' is to be left on at all times(even during receive operations) and is normally used for point-to-point four wire half-duplex and duplex leased lines for both primary and secondary stations. For multi-point primary station the 'RTS'=on option is usually used for four wire half-duplex and duplex lines. Two wire leased lines, switched lines and multi-point secondary stations usually use the 'RTS'=off option to drop 'Request to send' while not in transmit mode.

The 'external clock', 'data rate select'=on and oscillator select options are dependent on the type of modem connected and the type of internal and/or external clocks installed. If you select the 'external clock' option (with or without 'data rate select'=on) then the program will not use NRZI mode of transmission. If you select internal oscillators numbe. 0, 1,2 or 3 then the program uses NRZI mode. NRZI mode means (as implemented in the 3705) that if a zero bit is to be transmitted then complement the transmit line trigger, if a one bit is to be sent then do not change the state of the transmit line trigger. The combination of NRZI mode and SDLC 'zero bit insertion' operations always result in at least one data transition every six bit times so that modem or internal clocks can be kept in phase. NRZI mode is not used when external clock is selected from the modem since it is then the modems responsibility to provide clock correction and bit synchronizing. This automatic selection of NRZI mode according to type of line clocking is compatible to 3705/3704 NCP utilization.

The optional transmit data option can only be used with the primary station options to provide data characters to be sent within the SDLC link-test frames being transmitted. This optional data is sent after the SDLC station address and control fields and before the block check(CRC) characters. If the optional transmit data option is not selected for a primary station option then the minimum test frame of four characters (SDLC station address, SDLC link-test control field and two block check characters) preceded and followed by flag characters are transmitted. Note that 16 alternate bit transitions are transmitted before the first flag character of a frame so that the receive clock can be corrected.

To continue, set the STORAGE ADDRESS/REGISTER DATA switches B, C, D and E to the required settings, set DISPLAY/FUNCTION SELECT switch to FUNCTION 5 and PRESS the START pushbutton.

Switch B-E setting to enter line type and control options for F020 stop code are;

Switch B = line type options. Enter one of the following in switch B.

- 0= Primary station, half-duplex 2-wire leased line with 'RTS'=off option.
- 1= Secondary station, half-duplex 2 wire leased line with 'RTS'=off option.
- 2= Primary station, half-duplex 4-wire leased line with 'RTS'=on option (normally point-to-point).
- 3= Secondary station, half-duplex 4-wire leased line with 'RTS'=on option (normally point-to-point).
- 4= Secondary station, half-duplex 4-wire leased line with 'RTS'=off option (normally multi-point secondary).
- 5= Primary station, duplex 4-wire leased line with 'RTS'=on option. Note: requires duplex line set interface such as line set type 1H or LIB type 10.
- 6= Secondary station, duplex 4-wire leased line with 'RTS'=on option. Note: requires duplex line set interface such as line set type 1H or LIB type 10.
- 7= Secondary station, duplex 4-wire leased line with 'RTS'=off option(normally multi-point secondary). Note: requires duplex line set interface such as line set type 1H or LIB type 10.
- 8= Primary station, switched line with manual call, manual answer or auto answer with 'RTS'=off option. Note: half-duplex only for switched lines.
- 9= Secondary station, switched line with manual call, manual answer or auto answer with 'RTS'=off option. Note: Half-duplex only for switched lines.
- A= Primary station, switched line with auto-call. Note: Half-duplex only for switched lines.

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B= Secondary station, switched line with auto-call.
Note: Half-duplex only, for switched lines.

Switch C = clock control options. Enter one of the following in switch C.

0= Internal oscillator select 0 to use first internal oscillator.

1= Internal oscillator select 1 to use second internal oscillator.

2= Internal oscillator select 2 to use third internal oscillator.

3= Internal oscillator select 3 to use fourth internal oscillator.

4= Select external clock but do not select 'data rate select'.

5= Select external clock and also set 'data rate select' to use the highest of the two external clocking rates.

Switch D = NRZI Control with external clock.

0= External clock, non-NRZI, or internal clock NRZI

1= External clock NRZI

2= External clock, new sync, non-NRZI mode
Note: New sync is normally used with 4-wire multipoint leased-line modem equipment where the associated interface is designated as the master station (primary).

3= External clock, new sync, and NRZI mode.
See the note under 2= above.

Switch E = Transmit and receive data options. Enter one of the following in switch E.

0= No optional transmit data and no stopping on received frames.

1= Stop on any frame received with a bad block check(CRC) character.

2= Stop on any frame received other than a normal link-test command or response.

3= Stop on any frame received(good or bad).

4= Optional transmit data is required and will be requested in the F024 and F025 stop codes. This option is restricted to primary stations. This option does not include any stops on received frames.

5= Optional transmit data is required and will be requested in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes a 'stop on any frame received with a block check(CRC) error' option.

6= Optional transmit data is required and will be requested in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes the 'stop on any frame received other than a normal test frame' option.

7= Optional transmit data is required and will be requested in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes the 'stop on any frame received' option.

F021 Invalid or invalid combination of options entered for the LINK-TEST. Enter options again as defined in the F020 stop code.

F022 Enter number of test frames to be transmitted at this primary station for the link test. Set switches B through E to number (in hex) of times you want the test frame transmitted before the program terminates with the F02C completion code. If you enter 0000, the test will not terminate unless you use the dynamic communication options or abort the test.

F024 Enter first optional transmit data character for the primary station link test option. Set switches D and E to the hex character to be transmitted.

If only one optional data character is to be transmitted then set switches B or C to any non-zero value. If more than one optional transmit data character is to be sent then set switches B and C to 00.

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F025 Enter next optional transmit data character to be sent from this primary station of the SDLC LINK-TEST. Set switches D and E to the hex character that you want to use as the next data character to be transmitted.

If this is the last optional transmit data character you want to send, set switches B or C to any non-zero value. If you want to enter more optional transmit data then set switches B and C to 00 and the current data character in switches D and E will be stored when you select function 5 and press start. Then you will get this stop code again unless end of transmit buffer has been reached. If the machine this test is running in has over 16K of storage then you may enter up to 1022 character to be transmitted with the F024 and F025 stop codes. If the machine has only 16K of storage then you are limited to a 24 character maximum.

F026 Enter transmit line interface address. Enter line address in same format as defined in the F001 manual intervention stop code.

If selected an option using duplex lines enter the transmit line interface address of the duplex line interface pair. Note: duplex transmit line interface is always first line interface address of the even/odd line interface pair with the even line interface address being used as the transmit line and the odd line interface address being used as the receive line. Note also that this line interface address to be entered does not use the low order bit of byte 1 to set/input ABAR so that line addresses such as 0842 and 0846 are considered to be odd line interface addresses and line addresses such as 0840 and 0848 are even line interface addresses.

The line interface address you enter is used to get line set type and options according to what is found in the configuration data set(CDS). If you have selected a not-installed or invalid line address you will get stop code F027 asking for the line interface address again. If selected a duplex line option then the line set type must be a type that can run in duplex mode and the same applies for half-duplex, switched and internal/external clock selection.

If you enter FF in switches B and C and continue, the program will go back to the F020 stop code to ask for initial options again.

F027 Transmit line interface address entered in stop code F026 was invalid line set type for running with options selected. Enter transmit line interface address again as defined in stop code F026. If you enter FF in switches B and C and then continue the program will go back to the F020 stop code to ask for initial options again.

F028 Enter SDLC station address in switches D and E. This is the SDLC station address put into all test frames transmitted on the line and the SDLC station address that this station expects to receive from the remote secondary station if the primary station option was selected. If selected the secondary station option then this will be the SDLC station address searched for in all incoming frames and the SDLC station address put into the response test frames or command reject response sent back to the remote primary station.

If the secondary station receives a frame that has a different SDLC station address than the one you are entering then it will not respond to that frame but will count it in the statistics counters defined in routine X6F0 writeup.

After you continue from this code the program will reset and enable the scanner and start the LINK-TEST. See routine writeup for display codes you will get while test is running.

F029 Enter the line address of the auto call originate line interface to be used in this test. See stop code F001 for format to enter the line address.
Note:If the line address entered is either invalid or not configured
as an auto call originate line, this stop code will be displayed again.
Enter line address again as defined for this stop code.

F02A Enter the first digit to be dialed on the auto call originate line. Set switch D to 0 and switch E to the next digit to be dialed (Press START)

F02B Enter the next digit to be dialed. Set switch D to 0 and switch E to the next digit to be dialed (Press START) Continue entering digits in this manner and after last digit has been entered set switches D and E to FF and Press start.

The program will now reset and enable the scanner and start the link-test. Wait for normal connection or timeout (20 sec) to occur. If normal connection occurs each dial digit will be displayed in display B, BYTE 1, as it is dialed.

F02C LINK-TEST has terminated. Check statistics and register indicators defined in the routine heading if necessary. Then enter a link test restart or termination option.

The following list of options are acceptable with switches B and C set to D0 or 00 for the is F02C stop code. The same options may be used with the D0 settings when using the dynamic communications options defined in the routine writeup. Following is a list of the restart/termination options:

Set switches
B,C,D and E
To: For this restart/terminate option.

D000 Restart the link test at point where it setup initial transmit and receive operations without doing a scanner reset and enable operation. This option allows you to restart the test on a switched line without making a new dialed connection, but may be used on any type of restart except a scanner or LIB failure. If you use this restart option then all the statistic counters will be cleared(except number of frames to transmit) and run indicators will be reset to starting options.

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D001 Restart routine at stop code F020 asking for the link test options. This restart option will mask level 2 interrupts and mess up transmit and receive buffer pointers but will not modify any of the other link test statistics and will not reset the lines currently in use until after you have entered your new options. Therefore this option may be used to terminate the current test but still be able to look at test statistics or be able to respecify options.

D002 Restart the link test from hardware reset and enable in the scanner. This option will clear all run indicators and statistics as in option D000 but in addition it will disconnect any switched line connection due to the scanner reset and enable. This restart option should be used if a scanner or LIB failure occurred or if you did any outputs from the control panel that changed the current line conditions.

D003 Go to stop code F02C and wait for next selection of options. This stop code is used for dynamic communications(function select position 1 and D003 in switches B-E). If used at F02C stop code then it will just result in stop F02C again. This dynamic communications may be used to terminate the test before the transmit frame count is reached for the primary station or to terminate the secondary station when nothing is being received(indicated by E061 display code being displayed continously).

D004 Terminate routine after resetting scanner. This option should be used when you are done testing with the link test. This will terminate the link test routine and if you have not set the CE sense switches to cycle on request or if you are not running multiple IFT's or adapters then the DCM will come out with a display B stop code of 807? asking for your next test request.

F030 Enter transmit, receive, wrap or dial option.

Note: See examples on how to use stop codes F030 through F042 after the F042 stop code description at the end of the manual intervention stop codes.

Enter in switches B-E your selected option. Options are:

0001 - Transmit test on a non-switched leased line or local attachment.
0002 - Receive test on a non-switched leased line or local attachment.
0003 - Wrap a pair of non-switched or local lines.
0004 - Transmit test on a switched line using manual dialing and line connection.
0005 - Receive test on a switched line using manual dialing and line connection.
0006 - Wrap a pair of switched lines using manual dialing and line connection.
0007 - Dial numbers on an auto call originate line interface and then transmit on the attached switched line interface.
0008 - Wrap data on switched lines. This option will dial numbers on an auto call originate interface. Answer the call on a switched line interface. Go into receive mode on the line interface that answered the call. Then transmit on the line interface attached to the auto call originate line interface to the receive line.
0009 - Dial numbers continuously on an auto-call originate line interface.
000A - Dial numbers on an auto call originate line interface and then transmit an alternate all zeros and all ones character pattern for 128 characters, then disconnect the line address.

F031 Enter the line address of the auto call originate line interface to be used in this test. See stop code F001 for format to enter the line address.

F032 The line address entered is either invalid or not configured as an auto call originate line. Enter the line address again as defined in stop code F031.

F033 Enter the first digit to be dialed on the auto call originate line.

Set switch D to 0 and switch E to the digit to be dialed. The digit to be dialed may be 0 through 9 for dial digits, C for the end of numbers character or D for the separator character. It should be noted that the end of numbers and separator characters are not supported by most IBM and non-IBM auto call units in the U.S.A. and should be used with caution. At this time register X'13' points to a location in storage where you (as an option)

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may store up to 32 bytes of dial digits and then set switches C and D to FF and press the START push button to continue. If you select this option to store the dial digits,then the first 4 bits of each byte should be 0 and the last 4 bits should be the dial digit, and you should store a X'FF' character after the last digit to be dialed. If you make any errors in entering any dial digits you will be asked to enter the first dial digit again. If you used the end of numbers character, it must be the last digit entered.

F034 Enter the next digit to be dialed.

Set switch D to 0 and switch E to digit to dial or set switches D and E to FF if last digit to dial was entered previously. See stop code F033 for caution on dial digits and optional use of register X'13' storage address which you may still use as an option. After you have entered the dial digits,the digits will be validated, and if any digit is invalid, you will be asked to enter the first dial digit again. This manual intervention code may be repeated up to 31 times to get a total of 32 digits.

F035 Enter the transmit line address to be used in this test. See stop code F001 for format to use.

F036 The transmit line address entered is invalid or not configured as a line that can run in transmit mode. Enter the transmit line address again as defined in stop code F035.

F037 The transmit line address entered can not be used with the switched line and/or auto call originate test option you selected. Enter the transmit line address again as defined in stop code F035.

F038 Enter LCD and set mode bits for transmit line. Set switch B to the line control definer (LCD) wanted.

Set Hex:

0	for start/stop 9/6 line control which has one start bit, 6 data bits and 2 stop bits.
2	for start/stop 8/5 line control.
4	for start/stop 9/7 line control.
5	for start/stop 10/7 line control.
6	for start/stop 10/8 line control.
7	for start/stop 11/8 line control.
8	for DLC 7 bit character line control.
9	for DLC 8 bit character line control.
A	for DLC 6 bit character line control.
B	for DLC 5 bit character line control.
C	for BSC EBCDIC line control.
D	for BSC USASCII line control.

NOTE: Do not use LCD=0, 2,5 or 7 when transmit and receive(wrap) all zeros is selected else an error may occur indicating more characters were received than were transmitted. Do not use LCD= 4 or 6 when transmitting on a line set that can detect a receive break via the stop bit check since you may get error stops indicating ICW bits 0-3 are in error with the 'stop bit check' bit being on.

Set switch C to 0.

Set switch D and E to the hexadecimal sum of the following bit definitions.
The 8 bits obtained are used to set SDF bits 2-9 (ICW bits 26-33) during the set mode operation.

Switch D

hex 8 This bit is reserved and should be 0.

hex 4 Diagnostic mode latch is set if this bit is a 1.
This bit should normally be a 0 to test normal modem operation.
If this bit is a 1 and the set Data Terminal Ready bit is a 1, the modem test lead will be activated in IBM integrated modems.
When the diagnostic mode bit is set on, that CS hardware forces on a Data Set Ready and may force a Clear To Send indication according to the line status.
This bit should be 0 for all auto call originate and switched line test options.

hex 2 Set data terminal ready if this bit is a 1.
This bit should normally be a 1 to test modems.
If you select to do an internal transmit or wrap operation, this bit should be a 0 and the diagnostic mode bit should be a 1.

hex 1 Sync bit clock latch is set if this bit is a 1.
This bit should normally be a 0 for start/stop

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line control and a 1 for synchronous and BSC line control.
With some special features, this bit may control other than the clocking method.

Switch E

hex 8 External clock latch is set if this bit is a 1.
If this bit is 0, an internal clock is used.
For proper modem operation, some modems require that external clock be used.
If you set this bit to 1 to select external clock, then you should set the two oscillator select bits to 0.
If you set the diagnostic mode bit to a 1, this bit should be a 0 except for the case where IBM integrated modems that provide external clock are put in test mode by having both the diagnostic mode and Data Terminal Ready bits set to 1.

hex 4 Data rate select latch is set on if this bit is a 1.
On modems that provide two operational speeds, this bit being on should select the highest of the two speeds.
The data rate select latch may be used for other purposes on some line sets.
An example is the EIA local line set type 1F where it drives the local attachments Receive Line Signal Detect lead.

hex 2 and
hex 1 Oscillator select bits used to select one of 4 possible oscillators.
These bits may be set to 00, 01, 10, or 11 to select the 1st, 2nd,3rd, or 4th oscillator position.
The 1st oscillator is required to be the lowest speed oscillator.
You should use caution in selecting the 2nd, 3rd, or 4th oscillator since that oscillator may not be installed or may exceed the maximum allow operating speed of the line set under test.
The oscillator select bits should be set to 00 if you have the external clock bit set to 1.

F039 LCD entered for transmit line in invalid or the transmit line set type can not run with the LCD type selected. Enter LCD and set mode bits again as in stop code F038.

F03A Enter the receive line address to be used in this test. See stop code F001 for format to use to enter address.

F03B The receive line address entered is invalid or not configured as a line set type that can run in receive mode. Enter the receive line address again as in stop code F03A.

F03C The receive line address entered can not be used with the switched line and/or auto call originate test option selected. Enter the receive line address again as in stop code F03A. This error will also occur if a wrap option was selected and the receive line can not run with the transmit line LCD or set mode options.

F03D Enter LCD and set mode bits for receive line. See stop code F038 for format to enter LCD and set mode bits.

F03E LCD entered for receive line is invalid, or the receive line set type can not run with the LCD type selected, or for wrap options the LCD selected is not the same as the transmit LCD. Enter the LCD and set mode bits for the receive line again. See stop code F038 for format.

F040 Enter transmit data options and/or first data character to transmit.
All data characters are transmitted as entered with bit 7 transmitted first, then bit 6, then bit 5, etc.
The characters are transmitted from the first entered to the last entered and then the same character pattern is repeated continously until the test is terminated.
If you select the option to transmit all marks (one bits) or all space (zero bits) any data characters entered are ignored.

Set switch B to the hexadecimal sum of the following options:

hex 8 Transmit in NRZI mode if a DLC LCD is selected.

hex 4 All one bits (marks) are transmitted if this bit is a 1.
For start/stop the pad flag will be set on to suppress the start bit and data characters of all one bits will be transmitted. For DLC the 'disable Stuffer' bit will be set on to suppress the zero bit insert function and data characters of all one bits will be transmitted.
Note that this transmit all ones options is intended for modem

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equalization functions and can not detect a failure such as an open transmit data lead. You should wrap data using some character with both zero and one bits for a better exercise of the modem or communications line.

hex 2 Transmit all zeros. For start/stop LCDs two pad characters of all one bits are transmitted and then the transmit lines PCF is set to 'A' to suppress stop bits and all zero bits are transmitted.
For other LCDs all zero bits are transmitted without any syn or flag characters.

hex 1 Transmit all ones in DLC mode without setting the 'Disable Stuffer' bit so zero bit insert will operate. This option will work only if selected a DLC LCD.

Set Switch C to the hexadecimal sum of the following options:

hex 8 Ignore ICW 0-3 if this bit is a 1.
Otherwise, after every transmit line character service ICW bits 0-3 are checked, and if any of these bits are in error, an error code is displayed.

hex 4 Reserved. Set to 0.

hex 2 Transmit DLC Link Test. This bit is ignored unless selected a DLC LCD or if selected the transmit all ones, the transmit all zeros or the transmit DLC all ones options.

hex 1 Alternate data input option if this bit is a 1.
If you set this bit to 0, then set switches D and E to the 1st character to be transmitted, select FUNCTION 5 and press the START push button and you will get stop code F041 asking for next data character to transmit.
If you want to use the alternate data input option, do the following:

a. Get storage address from register X'13'.

b. Store the count of the number of characters to be transmitted as the first character.
The highest valid count is X'78' to transmit 120 characters.
The program will transmit this number of characters and then go back to the first character and repeat the same number of characters continously until the test is terminated.

c. Store up to 120 consecutive characters after the count byte.
The characters to be transmitted are put in the PDF in the same format that you store them except bit 0, bits 0 & 1 or bits 0,1 & 2 may be cleared.
If selected LCD 4, 5 or 8 the characters you store will all have the 0 bit set to 0 since these are all 7 bit character LCDs.
If selected LCD 0 or A, then bits 0 and 1 will be set to 00.
If selected LCD 2 or B then bits 0,1,and 2 will be set to 000.

d. Set switch B to 0.

e. Set switch C to 1 or 9 (according to the ignore ICW bits 0-3 option) to indicate this alternate data input is being used.

f. Select function 5 and press the start push button.

Set switches D and E to the first character to be transmitted unless selected the alternate data input format or the transmit all one or all zeros option in which case switches D and E are ignored.

F041 Enter next character to be transmitted.

Set switches B and C to 00 and switched D and E to the next character to be transmitted or set switch B or C to any non zero position if the last character has been entered previously.
At this time register X'13' contains an address pointing to a storage location that contains a

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byte that has the number of characters you have previously entered
followed by the characters you have entered.
You may (as an option) use the alternate data input steps a,b and c
defined in stop code F040 and
then set switch B or C to a non zero position, select function 5
and press the START push button.

F042 Enter receive data options.
If you are wrapping data then the received data characters are compared with the transmitted characters selected unless selected the receive all ones, all zeros, DLC link test or ignore receive interrupts options. If you are doing a receive only test and have not selected one of the above options then the received data characters are ignored but you may display the the last data character received by displaying reg X'44'(byte 1) while the program is running. If selected a synchronous LCD (8,9,A,B,C or D) and did not select one of the above options then there will be no indication of any data being received unless a valid synchronizing character for the LCD in use is received.

NOTE: For a wrap option transmitting all ones, all zeros, DLC all ones or DLC link test the same receive data option should be selected or error stops may occur.

Set switch B to the hexadecimal sum of the following options:

hex 8 Receive in NRZI mode if this bit is a 1 and if selected a DLC LCD.

hex 4 All one bits are expected to be received if this bit is a 1.
If this bit is a 1 and all one bits are not received, an error will be reported.
Note that this receive all ones option is intended to be used for modem equalization and can not detect a failure such as an open receive data lead or a receive data lead clamping problem.
You should wrap some data character containing both zero and one bits for a complete exercise of the modems or communications line.

hex 2 All zero bits are expected to be received. If this bit is a 1 and all zero bits are not received, then an error is reported.

hex 1 Ignore all receive character service interrupts. If this bit is a 0, and you have selected one of the wrap options, and all ones and all zeros options are 0, then a check is made that characters received are the same as characters transmitted.

Set switch C to the hexadecimal sum of the following options:

hex 8 Ignore ICW bits 0-4 if this bit is a 1.
If this bit is a 0 and the Ignore All Receive Character Service Interrupts bits is a 0, then ICW bits 0-4 are checked on every receive character service interrupt and an error is reported if they are in error.

hex 4 Reserved. Set to 0.

hex 2 Receive DLC Link Test. This bit is ignored unless you selected a DLC LCD or if selected the receive all ones or the receive all zeros options.
If you select this option then receive data errors are counted and displayed in the display B indicator lights as an X'E07?' code where the ?? is the low order byte of the received data error count. The total error count is always available in reg X'1B'. Note that it is common to get one or two errors when the routine first starts receiving due to clock correction time and the DLC ones bit counter circuit.

hex 1 Reserved. Set to 0.

Set switches D and E to 00.

F049 Enter options for routine X6F2; see routine heading for selections.

F050 Enter transmit line address for routine X6F2; see routine heading for selections.

F052 Enter the receive line address for routine X6F2; see routine heading for selections.

F055 Enter options for routine X6F4; see routine heading for selections.

F056 Enter the transmit line address for routine X6F4; see stop code F001 for format.

F057 Enter the receive line address for routine X6F4; see stop code F001 for format.

DISPLAY B STOP MANUAL INTERVENTION ACTION REQUIRED CODE

F058 Enter the high speed local attachment oscillator frequency and line address for routine X6F5; see routine heading for selections.

F059 Disconnect the external wrap facility for routine X6F4; see routine heading.

EXAMPLE OF USING ROUTINE X6CE:

EXAMPLE A: Transmit All ones.

This test may be used for equalization of transmit lines.
This test is equivalent to Modem Test 3.

PANEL INDICATION		TYPICAL CE SWITCH RESPONSE IN FUNCTION5	
F030	(Select Option)	0001	(Transmit Option. Press START.
F035	(Select Xmit Line)	0040	(1st LIB, 1st Line Address). Press START.
F038	(Select LCD and Mode Bits)	C038	(LCD for EBCDIC line control, Data Terminal Ready, Sync Bit Clock and External Clock.) Press START.
F040	(Select Data)	4000	(Transmit All ones). Press START.

Note: The scanner transmits all ones on the selected line address.
Successful transmission is indicated by an incrementing count
In Byte 1 of Display B.
Equalization tests can then be performed.
To restart on any error stop, press START pushbutton while in
FUNCTION 5.

EXAMPLE B: Receive All Ones.

This test may be used for equalization of receive lines when all ones
are being transmitted from another station to this station on a
selected line. This test is equivalent to MODEM TEST 4.

PANEL INDICATION		TYPICAL CE SWITCH RESPONSE	
F030	(Select Option)	0002	(Receive Option). Press START.
F03A	(Select Receive Line)	0044	(1st CS, 1st LIB, 3rd Line Address). Press START.
F03D	(Select LCD and Set Mode Bits)	C038	(EBCDIC LCD 8 Bit Line Control, Data Terminal Ready, Sync Bit Clock, External Clock). Press START.
F042	(Select receive data option)	4000	(Receive all ones). Press START.

Note; Reception of all ones successfully, in synchronous mode, is
indicated by an incrementing display in Byte 1 of Display B.
Equalization tests can then be performed.
To restart on any error stop, press start pushbutton while in Function 5.

EXAMPLE C: Dial number 6238 on an autocall originate line interface.
Answer the call on a switched line interface.
Go into Receive Mode on the line interface that answered the call.
Transmit data characters X'01' and X'02' continously from the line interface attached
to the auto call originate line interface to the receive line.

PANEL INDICATION		TYPICAL CE SWITCH RESPONSE5	
F03Q	(select Option)	0008	(Test autocall as described above). Press start.
F031	(Select Auto-call Originate Line Address)	004C	(1st CS, 1st LIB, Autocall Originate Line Address). Press start.
F033	(Select 1st Digit to be dialed)	0006	(6 is 1st dial digit). Press start.
F034	(select subsequent digit)	0002	(2 is 2nd dial digit). Press start.
F034	(Select subsequent digit)	0003	(3 is 3rd dial digit). Press start.
F034	(Select subsequent digit)	0008	(8 is 4th dial digit). Press start.
F034	(Select subsequent digit)	00FF	(FF to indicate last digit has been entered. Press start.
F035	(Select transmit line.)	0048	(1st CS, 1st LIB, 5th Line Address.) Press start.
F038	(Select LCD and Mode Bits for Transmit Line)	C03C	(BSC EBCDIC Line Control, Data Terminal Ready, Sync Bit Clock, External Clock, Data Rate Select). Press start.

F03A	(Select Receive Line)	0050	(1st CS, 1st LIB,9th Line Address). Press start.
F03D	(Select LCD and Mode Bits for Receive Line)	C03C	(BSC EBCDIC Line Control, Data Terminal Ready, Sync Bit Clock, External Clock, Data Rate Select). Press START.
F040	(Select Xmit Data)	0001	(Data characters 01). Press START.
F041	(Select subsequent data)	0002	(Data Characters 02). Press START.
F041	(Select subsequent data)	FF00	(Indicate last data character has been entered). Press START
F042	(Select Receive Data)	0000	(Indicate expected receive data same as Transmit data). Press START.

While in dialing process the dial digits are indicated in Byte 1 Bits 4-7 of Display B.
On reception of data successfully, an incrementing count is indicated in Byte 1 of Display B.

CHAPTER 7.0: TYPE 3 COMMUNICATIONS SCANNER SYMPTOM INDEX

X701 Configuration Data Set (CDS) Check Routine

ROUTINE DESCRIPTION

This routine verifies that necessary CDS control data is valid. Data validated is (1) scanner type, (2) scanner RPQs, (3) scanner features, (4) oscillator type, (5) LIB type, and (6) line set type.

ERROR CODE	
X701	0X01

The CDS is in error; the scanner is not configured as a type 3 communication scanner. Register X'16' contains the storage address of the CDS data block in the CDS for the adapter under test.

ERROR CODE	
X701	0X02

The CDS is in error; either no oscillators or an invalid oscillator type is coded in the CDS for oscillator number 0 (first oscillator position).

ERROR CODE	
X701	0X03

The CDS is in error; either the oscillator in the first oscillator position is not the lowest speed available, or an invalid oscillator type code was found in the CDS for the second, third, or forth position.

ERROR CODE	
X701	0X04

The CDS is in error; no LIBs are configured in the CDS data. Register X'16' contains the address of the CDS data block for the scanner under test.

ERROR CODE	
X701	0X05

The CDS is in error; no line sets are configured in the CDS data. Register X'16' contains the CDS data block for the scanner under test.

X703 Input/Output Register Test

ROUTINE DESCRIPTION

All valid input and output registers that are used with the type 3 communication scanner are tested by this routine. The first line address is used to setup the scanner and outputs X'40' through X'4F' are executed to verify that no level 1 interrupts occur for any of the output instructions.

Input instructions X'40' through X'4F' are tested in like manner to verify that no level 1 interrupts occur.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X703	0X01 E3R2	TE26X	6-090	
	E3S2	TE50X		
	E3Q2	TE52X		
	B3E2	CK001		

An I/O check occurred after an input or output instruction. Register X'14' contains the failing input/output instruction. Register X'16' contains the storage address of the instruction that caused the error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X703	0X02 E3E2	TE70X	6-090	
	E3Q2	TE52X		
	E3R2	TE26X		
	E3S2	TE50X		

A level 1 check occurred after an input or output instruction. Register X'14' contains the error bits stored in the level 1 routine from the input X'43' Register X'16' contains the address of the input/output instruction causing the level 1 check; Register X'11' contains the line address.

X705 Attachment Buffer Address Register (ABAR) Test

ROUTINE DESCRIPTION

All valid addresses are written into and read from the attachment buffer address register via an output and input X'40' instruction.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X705	0X04 E3H2	TE54X	F-180	
	E3S2	TE50X	F-250	
	B3E2	CX001		
	B3D2	CX009		

The address set via an output X'40' and the address read via an input X'40' are not equal. Register X'14' contains the address read via the input X'40' and Register X'11' contains the address used in the output X'40'.

X707 Power On Reset, Communication Scanner Disable, and ICW Array Reset Test

ROUTINE DESCRIPTION

The routine disables all LIBs followed by a power-on reset to the scanner. An output X'43' with bits 0.0 and 1.6 on is used to disable the scanner (Power on Reset). Beginning with the first line, all ICW bits are checked to verify that they are reset to the correct state. Each line address is checked in turn.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707	0X01 E3Q2	TE52X	F-270	
	E3L2	TE40X		
	E3S2	TE50X		
	E3K2	TE24X		
	E3F2	TE20X		
	E3H2	TE54X		
	E3M2	TE32X		
	E3R2	TE26X		
	E2J2	TF50X		
	E2U2	TF30X		
	E2T2	TF20X		
	E2V2	TF41X		

The PCF field read via an input X'45' was not zeros after the Communication Scanner disable. Register X'15' (bits 0.4-0.7) contains the bits in error; Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707	0X02 E3E2	TE70X	F-270	
	E2G2	TE21X		
	E3D2	TE34X		
	E3Q2	TE52X		
	E3F2	TE20X		
	E3R2	TE26X		
	E3S2	TE50X		

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF field read via an input X'45' was not zeros after the Communications Scanner disable. Register X'15' (bits 0.4-0.7) contains the bits in error; Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707	0X03	E3D2	TE34X	P-270
		E3L2	TE40X	
		E3E2	TE70X	
		E3K2	TE24X	
		E3S2	TE50X	
		E3Q2	TE52X	
		E2D2	TF62X	
		E2J2	TF50X	
		E2N2	TF22X	
		E2G2	TF40X	
		E2T2	TF20X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF did not remain at zero during an output X'45' attempting to set the PCF to X'7' with the communication scanner disabled. The bits in error (read via an input X'45') are contained in Register X'15' (bits 0.4-0.7); Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707	0X04	E3E2	TE70X	P-270
		E3M2	TE52X	
		E2J2	TF50X	
		E2M2	TF31X	
		E3L2	TE40X	
		E2V2	TF41X	
		E2C2	TF60X	

The PCF did not remain at zero during an output X'45' attempting to set the PCF to X'7' with the communication scanner disabled. The bits in error (read via an input X'45') are contained in Register X'15' (bits 0.4-0.7); Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707	0X05	E3E2	TE70X	P-270
		E3S2	TE50X	
		E3Q2	TE52X	
		E3M2	TE32X	

All check bits (input X'43') should have been reset by the communication scanner disable. Register X'15' contains the bits in error. Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707	0X08	E2J2	TF50X	P-270
		E2V2	TF41X	
		E2B2	TF81X	
		E2C2	TF60X	
		E2U2	TF30X	
		E3Q2	TE52X	
		E3H2	TE54X	

ICW 4.2-4.4 (ones counter) should have been reset by the communication scanner disable. Register X'15' contains the bits in error. Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707	0X09	E2C2	TF60X	P-270
		E3L2	TE40X	
		E3H2	TE54X	
		E3S2	TE50X	
		E3D2	TE34X	
		E3K2	TE24X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

ICW 4.5 (last line state) should be set on by the communication scanner disable.
Register X'15' contains the bits in error. Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707 0X0A	E2C2	TF60X	F-270	
	E2V2	TF41X		
	E3E2	TE70X		

ICW 4.6 (Display bit) should have been reset by the communication scanner disable.
Register X'15' contains the bits in error. Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707 0X0B	E2V2	TF41X	F-270	
	E2C2	TF60X		
	E2M2	TF31X		
	E3L2	TE40X		
	E3Q2	TE52X		
	E3M2	TE32X		
	E3G2	TE21X		
	E3E2	TE70X		

ICW 4.7-5.0 (ones counter) should have been reset by the communication scanner disable.
Register X'15' contains the bits in error. Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707 0X0C	E2N2	TF22X	F-270	
	E3Q2	TE52X		
	E3M2	TE32X		
	E3G2	TE21X		
	E3L2	TE40X		
	E3E2	TE70X		

ICW 5.1 (level 2 pending) should have been reset by the communication scanner disable.
Register X'15' contains the bits in error. Register X'11' contains the line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707 0X0E	E3L2	TE40X	F-270	
	E3D2	TE34X		
	E3K2	TE24X		
	E3F2	TE20X		
	E2N2	TF22X		

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

Cycle steal valid bit (ICW bit 6.5) should have been reset off via the communication scanner disable. Register X'11' contains the line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707 0X0F	E3S2	TE50X	F-270	
	E3D2	TE34X		
	E2F2	TF48X		
	E2G2			
	E2V2			
	E2C2			

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

All cycle steal array address and PDF array address bits (read via input X'4E') should have been set on via the communication scanner disable. Register X'15' (bits 0.0-0.7) contains the bits in error; Register X'11' contains the line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707 0X10	E2E2	TF80X	F-270	
	E2N2	TF22X		
	E2T2	TF20X		

The trace bit (ICW bit 0.7) was not reset to zero.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X707	0X11	E3N2	TE35X	

The CS PDF Array Pointer bit 16 and the PDF Array Pointer bit 16 (read via input X'41') should have been set on via the communication scanner disable. Register X'15' (bits 1.0-1.1) contains the bits in error; Register X'11' contains the line address under test.

X709 ICW Output, ICW Input, and Control Circuitry Test

ROUTINE DESCRIPTION

This routine checks for 'hot' or 'cold' bits in the ICW output/input data stream. An output X'43' with bits 0.0 and 0.6 on is issued to set Diagnostic Test mode (ICW Test Mode) prior to this test (see F-270). ICW Test Mode allows the ICW array to be tested as a storage unit.

Ouptut instructions to turn all bits off in the cycle steal address and BCC fields of the ICW are executed. Input instructions read the data back to CCU registers and the data is checked to see that all zeros was returned where expected and all bits were returned where expected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X01	E3S2	TE50X	F-320
		E3J2	TE22X	F-230
		E3G2	TE21X	
		E3F2	TE20X	
		E3H2	TE54X	
		E3Q2	TE32X	
		E3M2	TE52X	
		E3E2	TE70X	
		E3L2	TE40X	
		E2D2	TF62X	

The data read from the cycle steal address field of the ICW is not X'0000' as expected. Register X'15' contains the bit(s) in error. Register X'11' contains the line under test. This could be a failure caused by either the out register, ICW control circuits, or the in register.

If error stop 0X02 does not occur, suspect the ICW or work register for causing the failure.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X02	E3A2	Terminator	F-320
		E3K2	TE24X	F-230
		E3D2	TE34X	
		E3H2	TE54X	
		E3L2	TE40X	
		E3S2	TE50X	
		E3R2	TE26X	
		E3E2	TE70X	
		E2M2	TF31X	
		E2U2	TF30X	
		E2D2	TF62X	
		E2L2	TF46X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The data read from the BCC field of the ICW was not X'0000' as expected. Register X'15' contains the bit(s) in error. Register X'11' contains the line under test.

If error stop 0X01 did not occur, the failure is probably caused by the work register or the ICW. If error stop 0X01 occurred, the error is probably caused by the out register.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X03	E3Q2	TE52X	F-320
		E3S2	TE50X	F-230
		E3J2	TE22X	
		E3G2	TE21X	

The data read from the cycle steal address field of the ICW and from the BCC field contained identical 'hot' bits. Register X'15 contains the bit(s) in error. Register X'11' contains the line under test. Error stops 0X01 and 0X02 should have occurred. The error is probably caused by the out register.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X04	E2M2	TF31X	F-320	
		E2U2	TF30X	F-230	
		E3H2	TE54X		
		E3Q2	TE52X		
		E3S2	TE50X		
		E3J2	TE22X		
		E3G2	TE21X		

The data read from the BCC field of the ICW is not X'0000' as expected. Register X'15' contains the bit(s) in error. Register X'11' contains the line under test. This error could be caused by either the out register, ICW control circuits, or the work register. If error stop 0X05, 0X06, 0X07 or 0X08 do not occur, suspect the ICW control circuits or the work register.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X05	E2D2	TF62X	F-320	
		E3Q2	TE52X	F-230	
		E3R2	TE26X		
		E3F2	TE20X		
		E3A2	Terminator		Gate ICW Work Reg to In Reg
		E3L2	TE400		
		E3S2	TE50X		
		E3G2	TE21X		
		E3D2	TE34X		
		E3E2	TE70X		

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

ICW 8.0-8.4 bits are not X'F' as expected. Register X'15' contains the bits in error. If error stop 0X04 did not occur, suspect the ICW control circuits or the work register.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X06	E3J2	TE22X	F-320	
		E3Q2	TE52X	F-230	
		E3F2	TE20X		
		E2L2	TF46X		
		E2U2	TF30X		
		E2M2	TF31X		

ICW 8.5-8.7 bits are not X'F' as expected. Register X'15' contains the bits in error. If error stop 0X04 did not occur, suspect the ICW control circuits or the work register.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X07	E3J2	TE22X	F-320	
		E3G2	TE21X	F-230	
		E3Q2	TE52X		

ICW 9.0-9.4 bits are not X'F' as expected. Register X'15' contains the bits in error. If error stop 0X04 did not occur, suspect the ICW control circuits or the work register.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X08	E3J2	TE22X	F-320	
		E3G2	TE21X	F-230	
		E3Q2	TE52X		

ICW 9.5-9.7 bits are not X'F' as expected. Register X'15' contains the bits in error.

The data read from the CS address field of the ICW is not X'FFFF' as expected. Register X'15' contains the bit(s) in error. Register X'11' contains the line under test. If error stop 0X04 did not occur, suspect the ICW control circuits or the work register.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X709	0X0A	E3L2	TE40X	F-320
		E3S2	TE50X	F-230
		E2M2	TF31X	
		E2U2	TF30X	

The data read from the BCC field is not X'FFFF' as expected. Either stop 0X04 or 0X05 should have occurred. Register X'15 contains the bit(s) in error. Register X'11' contains the line under test.

This error is probably caused by the ICW control circuits or the work register if error stop 0X05, 0X06, 0X07 or 0X08 did not occur; The out register probably caused the error if error stop 0X04 occurred.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X0C	E3H2	TE54X	F-320
		E3Q2	TE52X	F-230
		E3S2	TE50X	

The data read from the cycle steal address and the data read from the BCC field of the ICW was missing identical bits. Register X'15' contains the bit(s) in error. Register X'11' contains the line under test. Error stops 0X05, 0X06, 0X07 or 0X08 should have occurred. This error is probably caused by the output register.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X709	0X0E	E2M2	TF31X	F-320
		E2R2	TF32X	F-230
		E2U2	TF30X	
		E3F2	TE20X	
		E3G2	TE21X	
		E3L2	TE40X	
		E3S2	TE50X	
		E3Q2	TE52X	
		E3J2	TE22X	

The data read from the cycle steal address field and the data read from the BCC field was missing different bits. Error stop 0X05, 0X06, 0X07 or 0X08 should have occurred. Register X'15' contains the bit(s) in error. Register X'11' contains the line under test. The ICW control circuitry or the work register probably caused this error.

X70C Power On Reset Off

ROUTINE DESCRIPTION

This routine sets the power on latch and waits for one scanner cycle. After the wait, the power on reset latch is set off and the PCF field is checked to verify that it contains X'00'. Power on reset is turned off with an output X'43' with bits 0.1, 1.5 and 1.6 on (see F-270). The PCF is set to X'7' and the LCD is set to X'0' and the PCF is again checked to verify that the X'7' set correctly. This routine also verifies that no error bits were set via an input X'43' and that the display bit did not set.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X70C	0X01	E2J2	TF50X	F-270
		E3E2	TE70X	
		E3H2	TE54X	

The PCF did not remain at X'0' after the disable latch was set off. Register X'11' contains the line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X70C	0X02	E3E2	TE70X	F-290
		E3D2	TE34X	
		E3S2	TE50X	
		E3Q2	TE52X	
		E2C2	TF60X	
		E2D2	TF62X	
		E2J2	TF50X	
		E2N2	TF22X	
		E2G2	TF40X	
		E2U2	TF30X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

With the scanner enabled, the PCF did not set to X'7', when an output X'45' with data=0007 was executed. Register X'11' contains the line address under test; register X'15' (bits 0.4-0.7) contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X70C	0X03 E3K2	TE24X	F-270	
	E3F2	TE20X	F-200	
	E3H2	TE544		ICW SEL LIB 1 or 4
	E2F2	TF48X		
	E2B2	TF81X		
	E2U2	TF30X		

Error register X'43' bits are on after setting the disable latch off and setting the PCF to X'7'. Register X'11' contains the line address under test; register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X70C	0X04 E2V2	TF41X	F-270	
	E2C2	TF60X	F-210	
	E3S2	TE50X		

The display bit should have been set off after setting the disable latch off. Register X'47' bit 0.6 contains the display bit. Register X'11' contains the line address.

X710 Unexpected Level 1 Interrupt Test # 1

ROUTINE DESCRIPTION

This routine disables via power on reset all installed communication scanners and waits a full scan cycle time for the power on reset to complete. Another power on reset (POR) is issued for the scanner under test. Then the program unmasks or allows level 1 interrupts to occur and waits one-hundred-eight miliseconds for unexpected level 1 interrupts to occur. An output X'43' with bits 0.0 and 1.6 on is issued to do the POR (see F-270). If a level 1 interrupt occurs, the routine displays an error stop; the routine terminates if no interrupts occur.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X710	0X01 E3E2	TE70X	F-190	
	E3H2	TE54X	F-200	

The scanner is reset with an output to set the 'CSB disable latch' and a level 1 interrupt occurred. Register X'11' contains the input data from ABAR (line address under test) when the interrupt occurred. Register X'13' contains the contents of the scanner check register (X'42') when the interrupt occurred. Register X'16' contains the contents of the scanner checks register (X'43') when the interrupt occurred. Register X'43' and X'42' should contain X'0000' unless another L1 interrupt error condition occurred.

X711 Unexpected Level 1 Interrupt Test # 2

ROUTINE DESCRIPTION

This routine disables all installed communication scanners with a power on reset (POR) and waits for a scan cycle time before reseting the POR. The POR is reset by issuing an output X'43' with bits 0.1, 1.5 and 1.6 on, (see F-270). The routine unmasks level 1 interrupts for 160 milliseconds and checks to see if any unexpected L1 interrupts occurred. No level 1 interrupts are expected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X711	0X01 E3H2	TE54X	F-190	
	E3E2	TE70X	F-200	

An unexpected level 1 interrupt occurred after the scanners were reset and enabled by setting the 'CSB disable latch' off.

Register X'11' contains the input data from ABAR (line address under test) when the interrupt occurred. Register X'13' contains the contents of the scanner check register (X'42') when the interrupt occurred. Register X'16' contains the contents from the

scanner check register (X'43') when the interrupt occurred. Register X'43' and X'42' should contain X'0000' unless another L1 error condition has occurred.

X713 Unexpected Level 2 Interrupt Test #1

ROUTINE DESCRIPTION

This routine disables all installed communication scanners via a power on reset (POR) and waits for a scan cycle for the POR to complete. Output X'43' is issued to each scanner with bits 0.0 and 1.6 on to disable scanners. The routine unmasks level 1 and level 2 interrupts and waits for 180 milliseconds for any unexpected level 1 or level 2 interrupts to occur.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X713	0X01	B3E2	TE70X	F-190	
		B3H2	TE54X	F-200	

An unexpected level 1 interrupt occurred after the scanners were reset and enabled by turning off the 'CSB disable latch'.

Register X'11' contains the input data from ABAR (line address under test) when the interrupt occurred. Register X'13' contains the contents of the scanner check register (X'42') when the interrupt occurred. Register X'16' contains the contents of the scanner check register X'43' when the interrupt occurred. Register X'43' and X'42' should contain X'0000' unless another level 1 error condition has occurred.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X713	0X02	B3E2	TE70X	F-190	
		B3F2	TE20X	F-200	
		B3H2	TE54X	F-550	
		B3L2	TE40X		

An unexpected level 1 and level 2 interrupt occurred after the scanners were reset and enabled by turning off the 'CSB disable latch'.

Register X'11' contains the input data from ABAR (line address under test) when the interrupt occurred. Register X'13' contains the contents of the scanner check register (X'42') when the interrupt occurred. Register X'16' contains the contents of the scanner check register X'43' when the interrupt occurred. Register X'43' and X'42' should contain X'0000' unless another level 1 error condition has occurred.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X713	0X03	B3F2	TE20X	F-550	
		B3L2	TE40X	F-560	
		B3E2	TE70X		

An unexpected level 2 interrupt occurred after the scanners were reset and enabled by turning off the 'CSB disable latch'.

Register X'11' contains the input data from ABAR (line address under test) when the interrupt occurred.

X714 Unexpected Level 2 Interrupt Test # 2

ROUTINE DESCRIPTION

This routine disables via a power on reset (POR) all installed communication scanners and waits a scan cycle time for the POR to complete. The routine resets the POR and allows level 1 and level 2 interrupts and verifies that none occur. An output X'43' with bits 0.1, 1.5 and 1.6 is issued to reset the POR (enable scanner).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X714	0X01	E3H2	TE54X	F-190	
		B3E2	TE70X	F-200	

An unexpected level 1 interrupt occurred after the scanners were reset and enabled by turning off the 'CSB disable latch'.

Register X'11' contains the input data from ABAR (line address under test) when the interrupt occurred. Register X'13' contains the contents of the scanner check register (X'42') when the interrupt occurred. Register X'16' contains the contents of the scanner check register X'43' when the interrupt occurred. Register X'43' and X'42' should contain X'0000' unless another level 1 error condition has occurred.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X714	0X02	E3E2	TE70X	F-190
		E3H2	TE54X	F-200
		E3L2	TE40X	F-550

An unexpected level 1 and level 2 interrupt occurred after the scanners were reset and enabled by turning off the 'CSB disable latch'.

Register X'11' contains the input data from ABAR (line address under test) when the interrupt occurred. Register X'13' contains the contents of the scanner check register (X'42') when the interrupt occurred. Register X'16' contains the contents of the scanner check register X'43' when the interrupt occurred. Register X'43' and X'42' should contain X'0000' unless another level 1 error condition has occurred.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X714	0X03	E3L2	TE40X	F-550
		E3S2	TE50X	F-560
		E3Q2	TE52X	
		E2J2	TF50X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2B2	TF81X	
		E2N2	TF22X	
		E2P2	TF82X	

An unexpected level 2 interrupt occurred after the scanners were reset and enabled by turning off the 'CSB disable latch'.

Register X'11' contains the input data from ABAR (line address under test) when the interrupt occurred.

X716 ICW Disable Test

ROUTINE DESCRIPTION

This routine verifies that all ICW bits that should be set or reset were, after disabling (power on reset) and enabling the type 3 scanner. An output X'43' with bits 0.1, 1.5 and 1.6 is issued to enable the scanner.

Each address is checked by using input and output instructions to read the ICWs.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X716	0X01	E2N2	TF22X	F-270
		E3L2	TE40X	
		E3E2	TE70X	

ICW bit 0.1 is on after an input X'44'. This bit (service request) should have been set off by the disable.

Register X'11' contains the line address under test and Register X'15' contains the bit in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X716	0X02	E3E2	TE70X	F-270
		E2C2	TF60X	
		E2J2	TF50X	
		E2E2	TF80X	
		E2B2	TF81X	

The PCF is verified via an Input X'45' to be set to X'0' after the scanner enable.

Register X'11' contains the line address under test and Register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X716	0X03	E2C2	TF60X	F-270
		E2M2	TF31X	
		E2V2	TF41X	
		E3E2	TE70X	

The ones counter and the display bit are checked via an Input X'47' and should have all bits off, (ICW bits 4.2-4.4 and 4.6 and 4.7). ICW bit 4.5 (last line state) should be on.

Register X'11' contains the line address under test and Register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X716	0X04	E3E2	TE70X	F-270
		E3F2	TE20X	
		E3K2	TE24X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The cycle steal valid bit (ICW 6.5) is checked via an Input X'48' to see that it was set off by the disable and enable operations.

Register X'11' contains the line address under test and Register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X716	0X05	E3D2	TE34X	F-270
		E3Q2	TE52X	
		E3H2	TE54X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2B2	TF81X	
		E2L2	TF46X	
		E2P2	TF82X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The cycle steal array address bits (ICW 12.0 - 12.3) and the PDF-1 array address bits (ICW 12.4 - 12.7) are checked via an Input X'4E' to see that they were set on by the disable and enable operation.

Register X'11' contains the line address under test and Register X'15' contains the bits in error.

X717 Force Level 1 Interrupt Errors Test

ROUTINE DESCRIPTION

This routine checks that a set function with level 1 request bit on (register X'43' bit 1.5) turns on all error bits in input X'42' and X'43'. DBAR address and the input X'40' address are compared.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X717	0X01	E3L2	TE40X	F-270
		E3D2	TE34X	F-200
		E3E2	TE70X	
		E3K2	TE24X	
		E3H2	TE54X	
		E3S2	TE50X	
		E3M2	TE32X	

E3Q2	TE52X	
E2J2	TF50X	
E2N2	TF22X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

All error bits in the input X'43' are tested to be set correctly.

Register X'11' contains the line address for the line under test. Register X'14' contains the scanner check register bits via an input X'43', and register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X717	0X02 E3E2	TE70X	F-270	
	E3S2	TE50X	F-190	

All error bits in the input X'42' are tested to be set correctly.

Register X'11' contains the line address for the line under test. Register X'14' contains the scanner check register bits via an input X'42', and register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X717	0X03 E3E2	TE70X	F-260	
	E3H2	TE544	F-190	ICW Address Lines
	E3P2	TE31X		
	E3N2	TE30X		
	E3M2	TE32X		
	E3L2	TE40X		
	E3S2	TE50X		

NOTE **** If the High Speed Scanner Feature (230KB) is installed;
E3P2 has been deleted.

The address in an input X'40' did not equal the address in an input X'42' byte 1, (this is a binary representation of the address).

Register X'11' contains the line address of the scanner under test,

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X717	0X04 E3Q2	TE52X	F-270	
	E3E2	TE70X	F-200	

After the L1 request bit was reset, all error bits in input X'43'did not reset. Error bits should have been reset with an output X'43' with bits 0.1 and 1.5 on.

Register X'11' contains the line address of the scanner under test; register X'14' contains the check register bits via an input X'43'; Register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X717	0X05 E3L2	TE40X	F-270	
	E3E2	TE70X	F-190	
	E2H2	TF42X		

After the L1 request bit was reset, all error bits in input X'42' did not reset. Error bits should have been reset via an output X'43' with bits 0.1 and 1.5 on.

Register X'11' contains the line address of the scanner under test;

Register X'14' contains the check register bits via an input X'42';

Register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X717	0X06	E3E2	TE70X	F-270

A level 1 interrupt should have occurred for the line under test, because an output X'43' with bits 0.0 and 1.5 was issued.

Ignore this stop and use the abort routine function (FUNCTION 6) if the service aid to mask L1 errors off is being used.

Register X'11' contains the line address expected to cause the interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X717	0X07	E3E2	TE70X	F-190
		E3R2	TE26X	F-200

A level 1 interrupt occurred from an unexpected line address.

Register X'11' contains the line address expecting the interrupt; register X'14' contains the line address causing the interrupt.

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X718 ICW Set and Reset

ROUTINE DESCRIPTION

This routine sets the diagnostic mode bit via an Output X'43' with bit 0.6 on. Diagnostic mode permits the program to use the ICW as if they were storage. Starting with the first line address and bit 0.0 of the ICW, all bits are set on using the applicable output instruction. Input instructions are used to verify that each bit did set properly. The operation is repeated until all ICW bits of all ICW have been checked.

The diagnostic program starts with the first line address and sets all the ICW bits off to verify that the ICW bits turn off correctly.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X01	E3S2	TE50X	F-210 Input 44
		E3D2	TE34X	F-280 Output 44, ICW 0.4
		E3Q2	TE52X	Encode for str
		E3E2	TE70X	Input 42 or 43 bits
		E2T2	TF20X	ICW 0.7
		E2B2	TF81X	ICW 0.7
		E2N2	TF22X	ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X02	E3S2	TE50X	F-210 Output 45
		E2J2	TF50X	F-290 ICW 2.0, 2-4
		E2E2	TF80X	ICW 2.0
		E2H2	TF42X	ICW 2.4,2.5
		E2K2	TF44X	ICW 2.0
		E2L2	TF46X	ICW 2.1-3
		E2N2	TF220	CCU Time
		E2Q2	TF34X	ICW 2.0
		E2R2	TF32X	ICW 2.0
		E2U2	TF30X	ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X03	E3S2	TE50X	F-210	Output 46
		E3Q2	TE52X	F-300	Out Reg bus A-0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X04	E3S2	TE50X	F-210	Output 46
		E2C2	TF60X	F-300	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X05	E2V2	TF41X	F-210	
		E3S2	TE50X	F-310	
		E2C2	TF60X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X07	E3R2	TE26X	F-210	ICW 5.1
		E3S2	TE50X	F-310	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X08	E2D2	TF62X	F-210	ICW 5.5
		E2C2	TF60X	F-300	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2F2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X09	E3L2	TE40X	F-230	ICW 6.5-6
		E3G2	TE21X	F-320	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19' contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X0A	E3F2	TE20X	F-230
		E3G2	TE21X	F-320

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19' contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X0B	E2U2	TF30X	F-230
		E2M2	TF31X	F-320

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X0C	E3S2	TE50X	F-240	ICW 12.0-7
		E3D2	TE34X	F-340	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7

E2F2	TF48X	ICW 12.0-7, 13.2-5
E2B2	TF81X	ICW 13.3
E2R2	TF32X	ICW 13.1-3
E2G2	TF40X	ICW 13.0-7
E2H2	TF42X	ICW 13.3
E2P2	TF82X	ICW 13.0
E2V2	TF41X	ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X0D	E3S2	TE50X	F-240	Output 4F
		E2E2	TF80X	F-350	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2B2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X0E	E3S2	TE50X	F-240	ICW 16.0-7
		E3Q2	TE52X	F-290	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.1
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X21	E3S2	TE50X	F-210	Input 44
		E3D2	TE34X	F-280	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7
		E2B2	TF81X		ICW 0.7
		E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X22	E3S2	TE50X	F-210	Output 45
		E2J2	TF50X	F-290	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0
		E2H2	TF42X		ICW 2.4,2.5
		E2K2	TF44X		ICW 2.0
		E2L2	TF46X		ICW 2.1-3
		E2N2	TF220		CCU Time
		E2Q2	TF34X		ICW 2.0
		E2R2	TF32X		ICW 2.0
		E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X23	E3S2	TE50X	F-210	Output 46
		E3Q2	TE52X	F-300	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF81¶		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF34¶		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X24	E3S2	TE50X	F-210	Output 46
		E2C2	TF60X	F-300	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X25	E2V2	TF41X	F-210	
		E3S2	TE50X	F-310	
		E2C2	TF60X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X27	E3R2	TE26X	F-210	ICW 5.1
		E3S2	TE50X	F-310	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X28	E2D2	TF62X	F-210	ICW 5.5
		E2C2	TF60X	F-300	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2F2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X29	E3L2	TE40X	F-230	ICW 6.5-6
		E3G2	TE21X	F-320	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19' contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X2A	E3F2	TE20X	F-230	
		E3G2	TE21X	F-320	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19' contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X2B	B2U2	TF30X	F-230
		B2M2	TF31X	F-320

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X2C	E3S2	TE50X	F-240	ICW 12.0-7
		E3D2	TE34X	F-340	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X		ICW 13.0
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X2D	E3S2	TE50X	F-240	Output 4F
		E2E2	TF80X	F-350	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X2E	E3S2	TE50X	F-240	ICW 16.0-7
		E3Q2	TE52X	F-290	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.1
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X718	0X70	TE706	F-190	

Unexpected L1 interrupt occurred indicating a type 3 scanner level 1 error.

Register X'1B' contains the input instruction. Register X'1A' contains the output instruction. Register X'19' contains the bits that were set via the output instruction. Register X'18' contains the bits expected in the input instruction. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

X719 ICW Address - Test ABAR

ROUTINE DESCRIPTION

This routine sets the diagnostic mode bit (see routine 18 description).

This routine checks for interaction between ICWs by storing a different data pattern in the BCC of each ICW. Each ICW is checked to verify that the correct data pattern is stored in the BCC. The pattern stored in each ICW is the line address of that ICW. (Data stored is the same as the address in ABAR).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X719	0X01 E2U2	TF30X	F-230	
	E2M2	TF31X	F-320	
	E3H2	TE54X		
	B3D2	CX007		
	B3E2	CX009		

The BCC of the ICW (address in register X'11') contained incorrect data.

Register X'14' contains the actual BCC bits; register X'11' contains the expected BCC data. Register X'15' contains the bits in errors.

X71A ICW Address and Interaction Test

ROUTINE DESCRIPTION

This routine sets the diagnostic mode bit (see routine 18 description).

This routine checks that all ICWs can be addressed correctly and that there is no interaction between ICWs. All ICW bits are set on and one ICW at a time is set off while the other ICWs are checked to verify that no interaction took place. Each ICW is tested in this fashion to verify correct operation.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X01 E3S2	TE50X	F-210	Input 44
	E3D2	TE34X	F-280	Output 44, ICW 0-4
	E3Q2	TE52X		Encode for str
	E3E2	TE70X		Input 42 or 43 bits
	E2T2	TF20X		ICW 0.7
	E2B2	TF81X		ICW 0.7
	E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71A	0X02	B3S2	TE50X	F-210	Output 45
		B2J2	TF50X	F-290	ICW 2.0, 2-4
		B2E2	TF80X		ICW 2.0
		B2H2	TF42X		ICW 2.4,2.5
		B2K2	TF44X		ICW 2.0
		B2L2	TF46X		ICW 2.1-3
		B2N2	TF220		CCU Time
		B2Q2	TF34X		ICW 2.0
		B2R2	TF32X		ICW 2.0
		B2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X03	B3S2	TE50X	F-210	Output 46
		B3Q2	TE52X	F-300	Out Reg bus A.0-7
		B2C2	TF60X		ICW 3.1
		B2D2	TF62X		SDF 0-7
		B2J2	TF50X		Output 46
		B2F2	TF48X		EPCF bit 0
		B2G2	TF40X		SDF field
		B2B2	TF811		Force Constant to SDF
		B2H2	TF42X		ICW 3.0-7
		B2K2	TF44X		ICW 3.0-7
		B2L2	TF46X		ICW 3.4,3.7
		B2P2	TF82X		Output 46
		B2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X04	B3S2	TE50X	F-210	Output 46
		B2C2	TF60X	F-300	ICW 4.0-1
		B2E2	TF80X		ICW 4.0
		B2V2	TF41X		SDF 8, 9
		B2H2	TF42X		ICW 4.0,4.1
		B2K2	TF44X		ICW 4.0,4.1
		B2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X05	B2V2	TF41X	F-210
		B3S2	TE50X	F-310
		B2C2	TF60X	

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71A	0X07	E3R2	TE26X	F-210	ICW 5.1
		E3S2	TE50X	F-310	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X08	E2D2	TF62X	F-210	ICW 5.5
		E2C2	TF60X	F-300	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2F2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X09	E3L2	TE40X	F-230	ICW 6.5-6
		E3G2	TE21X	F-320	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19' contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X0A	E3F2	TE20X	F-230
		E3G2	TE21X	F-320

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19' contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X0B	E2U2	TF30X	F-230
		E2M2	TF31X	F-320

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X0C	E3S2	TE50X	F-240	ICW 12.0-7
	E3D2	TE34X	F-340	Output 4E, ICW 12.0-7
	E3L2	TE40X		ICW 12.0-7, 13.0-7
	E2J2	TF50X		ICW 13.3, 1.0
	E2E2	TF80X		ICW 13.0-7
	E2F2	TF48X		ICW 12.0-7, 13.2-5
	E2B2	TF81X		ICW 13.3
	E2R2	TF32X		ICW 13.1-3
	E2G2	TF40X		ICW 13.0-7
	E2H2	TF42X		ICW 13.3
	E2P2	TF82X		ICW 13.0
	E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X0D	E3S2	TE50X	F-240	Output 4F
	E2E2	TF80X	F-350	ICW 14.5
	E2T2	TF20X		ICW 14.0-7
	E2F2	TF48X		ICW 15.6
	E2N2	TF22X		ICW 14.0-7
	E2S2	TF21X		ICW 15.0-7
	E2P2	TF82X		ICW 14.1 set
	E2Q2	TF34X		ICW 14.1,15.0-7
	E2R2	TF32X		ICW 15.7
	E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X0E	E3S2	TE50X	F-240	ICW 16.0-7
	E3Q2	TE52X	F-290	ICW 16.2,3
	E2E2	TF80X		ICW 16.4,5,7
	E2F2	TF48X		ICW 16.4-7
	E2S2	TF21X		ICW 16.0-7
	E2B2	TF81X		ICW 16.4-7
	E2H2	TF42X		ICW 16.0,16.1
	E2P2	TF82X		ICW 16.0-7
	E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71A	0X21	E3S2	TE50X	F-210	Input 44
		E3D2	TE34X	F-280	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7
		E2B2	TF81X		ICW 0.7
		E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X22	E3S2	TE50X	F-210	Output 45
	E2J2	TF50X	F-290	ICW 2.0, 2-4
	E2E2	TF80X		ICW 2.0
	E2H2	TF42X		ICW 2.4,2.5
	E2K2	TF44X		ICW 2.0
	E2L2	TF46X		ICW 2.1-3
	E2N2	TF220		CCU Time
	E2Q2	TF34X		ICW 2.0
	E2R2	TF32X		ICW 2.0
	E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X23	E3S2	TE50X	F-210	Output 46
	E3Q2	TE52X	F-300	Out Reg bus A.0-7
	E2C2	TF60X		ICW 3.1
	E2D2	TF62X		SDF 0-7
	E2J2	TF50X		Output 46
	E2F2	TF48X		EPCF bit 0
	E2G2	TF40X		SDF field
	E2B2	TF811		Force Constant to SDF
	E2H2	TF42X		ICW 3.0-7
	E2K2	TF44X		ICW 3.0-7
	E2L2	TF46X		ICW 3.4,3.7
	E2P2	TF82X		Output 46
	E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X24	E3S2	TE50X	F-210	Output 46
	E2C2	TF60X	F-300	ICW 4.0-1
	E2E2	TF80X		ICW 4.0
	E2V2	TF41X		SDF 8, 9
	E2H2	TF42X		ICW 4.0,4.1
	E2K2	TF44X		ICW 4.0,4.1
	E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X25	E2V2	TF41X	F-210	
		E3S2	TE50X	F-310	
		E2C2	TF60X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X27	E3R2	TE26X	F-210	ICW 5.1
		E3S2	TE50X	F-310	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X28	E2D2	TF62X	F-210	ICW 5.5
		E2C2	TF60X	F-300	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2F2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X29	E3L2	TE40X	F-230	ICW 6.5-6
		E3G2	TE21X	F-320	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19' contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X2A	B3F2	TE20X	F-230
		B3G2	TE21X	F-320

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19' contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X2B	B2U2	TF30X	F-230
		B2M2	TF31X	F-320

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X2C	B3S2	TE50X	F-240	ICW 12.0-7
		B3D2	TE34X	F-340	Output 4E, ICW 12.0-7
		B3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X		ICW 13.0
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X2D	B3S2	TE50X	F-240	Output 4F
		E2E2	TF80X	F-350	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		B3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71A	0X2E	B3S2	TE50X	F-240	ICW 16.0-7
		E3Q2	TE52X	F-290	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X31	B3S2	TE50X	F-210	Input 44
		E3D2	TE34X	F-280	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7
		E2B2	TF81X		ICW 0.7
		E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X32	B3S2	TE50X	F-210	Output 45
		E2J2	TF50X	F-290	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0
		E2H2	TF42X		ICW 2.4,2.5
		E2K2	TF44X		ICW 2.0
		E2L2	TF46X		ICW 2.1-3
		E2N2	TF220		CCU Time
		E2Q2	TF34X		ICW 2.0
		E2R2	TF32X		ICW 2.0
		E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X33	B3S2	TE50X	F-210	Output 46
		E3Q2	TE52X	F-300	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X34	E3S2	TE50X	F-210	Output 46
		E2C2	TF60X	F-300	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X35	E2V2	TF41X	F-210	
		E3S2	TE50X	F-310	
		E2C2	TF60X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'.

Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X37	E3R2	TE26X	F-210	ICW 5.1
		E3S2	TE50X	F-310	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X38	E2D2	TF62X	F-210	ICW 5.5
		E2C2	TF60X	F-300	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2F2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71A	0X39	E3L2	TE40X	F-230	ICW 6.5-6
		E3G2	TE21X	F-320	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF48B		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19' contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X3A	E3F2	TE20X	F-230
		E3G2	TE21X	F-320

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19' contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X3B	E2U2	TF30X	F-230
		E2M2	TF31X	F-320

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X3C	E3S2	TE50X	F-240	ICW 12.0-7
		E3D2	TE34X	F-340	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X		ICW 13.0
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X3D	E3S2	TE50X	F-240	Output 4F
		E2E2	TF80X	F-350	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6

E2N2	TF22X	ICW 14.0-7
E2S2	TF21X	ICW 15.0-7
E2P2	TF82X	ICW 14.1 set
E2Q2	TF34X	ICW 14.1,15.0-7
E2R2	TF32X	ICW 15.7
E3D2	TE34X	ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X3E	E3S2	TE50X	F-240	ICW 16.0-7
	E3Q2	TE52X	F-290	ICW 16.2,3
	E2E2	TF80X		ICW 16.4,5,7
	E2F2	TF48X		ICW 16.4-7
	E2S2	TF21X		ICW 16.0-7
	E2B2	TF81X		ICW 16.4-7
	E2H2	TF42X		ICW 16.0,16.1
	E2P2	TF82X		ICW 16.0-7
	E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X41	E3S2	TE50X	F-210	Input 44
	E3D2	TE34X	F-280	Output 44, ICW 0.4
	E3Q2	TE52X		Encode for str
	E3E2	TE70X		Input 42 or 43 bits
	E2T2	TF20X		ICW 0.7
	E2B2	TF81X		ICW 0.7
	E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A 0X42	E3S2	TE50X	F-210	Output 45
	E2J2	TF50X	F-290	ICW 2.0, 2-4
	E2E2	TF80X		ICW 2.0
	E2H2	TF42X		ICW 2.4,2.5
	E2K2	TF44X		ICW 2.0
	E2L2	TF46X		ICW 2.1-3
	E2N2	TF220		CCU Time
	E2Q2	TF34X		ICW 2.0
	E2B2	TF32X		ICW 2.0
	E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X43	E3S2	TE50X	F-210	Output 46
		E3Q2	TE52X	F-300	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X44	E3S2	TE50X	F-210	Output 46
		E2C2	TF60X	F-300	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X45	E2V2	TF41X	F-210	
		E3S2	TE50X	F-310	
		E2C2	TF60X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X47	E3R2	TE26X	F-210	ICW 5.1
		E3S2	TE50X	F-310	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X48	E2D2	TF62X	F-210	ICW 5.5
		E2C2	TF60X	F-300	ICW 5.4-7
		E2J2	TF50X		ICW 5.6

E2F2	TF48X	ICW 5.4
E2B2	TF81X	NRZI or XPar
E2E2	TF80X	ICW 5.4
E2H2	TF42X	ICW 5.4-7
E2M2	TF31X	ICW 5.4-7
E2N2	TF222	Test Mode
E2P2	TF82X	ICW 5.4
E2R2	TF32X	ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X49	E3L2	TE40X	F-230	ICW 6.5-6
		E3G2	TE21X	F-320	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2P2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19' contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X4A	E3F2	TE20X	F-230	
		E3G2	TE21X	F-320	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19' contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X4B	E2U2	TF30X	F-230	
		E2M2	TF31X	F-320	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X4C	E3S2	TE50X	F-240	ICW 12.0-7
		E3D2	TE34X	F-340	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3

E2P2	TF82X	ICW 13.0
E2V2	TF41X	ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X4D			
	E3S2	TE50X	F-240	Output 4F
	E2E2	TF80X	F-350	ICW 14.5
	E2T2	TF20X		ICW 14.0-7
	E2F2	TF48X		ICW 15.6
	E2N2	TF22X		ICW 14.0-7
	E2S2	TF21X		ICW 15.0-7
	E2P2	TF82X		ICW 14.1 set
	E2Q2	TF34X		ICW 14.1,15.0-7
	E2B2	TF32X		ICW 15.7
	E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71A	0X4E			
	E3S2	TE50X	F-240	ICW 16.0-7
	E3Q2	TE52X	F-290	ICW 16.2,3
	E2E2	TF80X		ICW 16.4,5,7
	E2F2	TF48X		ICW 16.4-7
	E2S2	TF21X		ICW 16.0-7
	E2B2	TF81X		ICW 16.4-7
	E2H2	TF42X		ICW 16.0,16.1
	E2P2	TF82X		ICW 16.0-7
	E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

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X71C Ripple Zeros Accross The ICWs

ROUTINE DESCRIPTION

This routine sets the diagnostic mode bit (see routine 18 description).

All ICWs are filled with one bits (all ICW bits set on), then starting with the first bit of the first ICW, the bits are turned off one at a time for each ICW in turn. All ICWs are checked in this manner.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X01			
	E3S2	TE50X	F-210	Input 44
	E3D2	TE34X	F-280	Output 44, ICW 0.4
	E3Q2	TE52X		Encode for str
	E3E2	TE70X		Input 42 or 43 bits
	E2T2	TF20X		ICW 0.7
	E2B2	TF81X		ICW 0.7
	E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X02	E3S2	TE50X	F-210	Output 45
		E2J2	TF50X	F-290	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0
		E2H2	TF42X		ICW 2.4,2.5
		E2K2	TF44X		ICW 2.0
		E2L2	TF46X		ICW 2.1-3
		E2N2	TF220		CCU Time
		E2Q2	TF34X		ICW 2.0
		E2R2	TF32X		ICW 2.0
		E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X03	E3S2	TE50X	F-210	Output 46
		E3Q2	TE52X	F-300	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X04	E3S2	TE50X	F-210	Output 46
		E2C2	TF60X	F-300	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71C	0X05	E2V2	TF41X	F-210
		E3S2	TE50X	F-310
		E2C2	TF60X	

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X07	E3R2	TE26X	F-210	ICW 5.1
		E3S2	TE50X	F-310	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X08	E2D2	TF62X	F-210	ICW 5.5
		E2C2	TF60X	F-300	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2P2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X09	E3L2	TE40X	F-230	ICW .5-6
		E3G2	TE21X	F-320	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19' contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X0A	E3F2	TE20X	F-230	
		E3G2	TE21X	F-320	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19' contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X0B	E2U2	TF30X	F-230	
		E2M2	TF31X	F-320	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X0C	E3S2	TE50X	F-240	ICW 12.0-7
		E3D2	TE34X	F-340	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X		ICW 13.0
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X0D	E3S2	TE50X	F-240	Output 4F
		E2E2	TF80X	F-350	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X0E	E3S2	TE50X	F-240	ICW 16.0-7
		E3Q2	TE52X	F-290	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7

E2B2	TF81X	ICW 16.4-7
E2H2	TF42X	ICW 16.0,16.1
E2P2	TF82X	ICW 16.0-7
E2R2	TF32X	ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X21	E3S2	TE50X	F-210	Input 44
		E3D2	TE34X	F-280	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7
		E2B2	TF81X		ICW 0.7
		E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X22	E3S2	TE50X	F-210	Output 45
		E2J2	TF50X	F-290	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0
		E2H2	TF42X		ICW 2.4,2.5
		E2K2	TF44X		ICW 2.0
		E2L2	TF46X		ICW 2.1-3
		E2N2	TF220		CCU Time
		E2Q2	TF34X		ICW 2.0
		E2R2	TF32X		ICW 2.0
		E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X23	E3S2	TE50X	F-210	Output 46
		E3Q2	TE52X	F-300	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X24	B3S2	TE50X	F-210	Output 46
		B2C2	TF60X	F-300	ICW 4.0-1
		B2E2	TF80X		ICW 4.0
		B2V2	TF41X		SDF 8, 9
		B2H2	TF42X		ICW 4.0,4.1
		B2K2	TF44X		ICW 4.0,4.1
		B2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X25	B2V2	TF41X	F-210	
		B3S2	TE50X	F-310	
		B2C2	TF60X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X27	B3R2	TE26X	F-210	ICW 5.1
		B3S2	TE50X	F-310	Output 47
		B2C2	TF60X		ICW 4.7, 5.0-3
		B2M2	TF31X		ICW 5.0-3
		B2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X28	B2D2	TF62X	F-210	ICW 5.5
		B2C2	TF60X	F-300	ICW 5.4-7
		B2J2	TF50X		ICW 5.6
		B2F2	TF48X		ICW 5.4
		B2B2	TF81X		NRZI or XPar
		B2E2	TF80X		ICW 5.4
		B2H2	TF42X		ICW 5.4-7
		B2M2	TF31X		ICW 5.4-7
		B2N2	TF222		Test Mode
		B2P2	TF82X		ICW 5.4
		B2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X29	B3L2	TE40X	F-230	ICW 6.5-6
		B3G2	TE21X	F-320	Input 48
		B3D2	TE34X		ICW 6.5
		B3J2	TE22X		ICW 7.0-7
		B3K2	TE24X		Write bytes 6, 7

E3S2	TE50X	Input 48
E3F2	TE20X	ICW 6.0-7
E2F2	TF488	Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19' contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C 0X2A	E3F2	TE20X	F-230	
	E3G2	TE21X	F-320	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19' contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C 0X2B	E2U2	TF30X	F-230	
	E2M2	TF31X	F-320	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C 0X2C	E3S2	TE50X	F-240	ICW 12.0-7
	E3D2	TE34X	F-340	Output 4E, ICW 12.0-7
	E3L2	TE40X		ICW 12.0-7, 13.0-7
	E2J2	TF50X		ICW 13.3, 1.0
	E2E2	TF80X		ICW 13.0-7
	E2F2	TF48X		ICW 12.0-7, 13.2-5
	E2B2	TF81X		ICW 13.3
	E2R2	TF32X		ICW 13.1-3
	E2G2	TF40X		ICW 13.0-7
	E2H2	TF42X		ICW 13.3
	E2P2	TF82XICW 13.0		
	E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C 0X2D	E3S2	TE50X	F-240	Output 4F
	E2E2	TF80X	F-350	ICW 14.5
	E2T2	TF20X		ICW 14.0-7
	E2F2	TF48X		ICW 15.6
	E2N2	TF22X		ICW 14.0-7
	E2S2	TF21X		ICW 15.0-7
	E2P2	TF82X		ICW 14.1 set
	E2Q2	TF34X		ICW 14.1,15.0-7

E2R2	TF32X	ICW 15.7
E3D2	TE34X	ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19' contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71C	0X2E	E3S2	TE50X	F-240	ICW16.0-7
		E3Q2	TE52X	F-290	ICW 16.2, 3
		E2E2	TF80X		ICW 16.4, 5, 7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.1
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'.

The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'.

Register X'18' contains the bits expected in the Input X'4B'.

Register X'15' contains the bits in error.

Register X'11' contains the ICW line address under test.

X71D Ripple Ones Across The ICWs

ROUTINE DESCRIPTION

This routine sets the diagnostic mode bit (see routine 18 for description).

All ICWs are zeroed (all ICW bits set off), then starting with the first bit of the first ICW, the bits are turned on one at a time for each ICW in turn. All ICWs are checked in this manner.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X01	E3S2	TE50X	F-280	Input 44
		E3D2	TE34X	F-210	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7
		E2B2	TF81X		ICW 0.7
		E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X02	E3S2	TE50X	F-290	Output 45
		E2J2	TF50X	F-210	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0
		E2H2	TF42X		ICW 2.4,2.5
		E2K2	TF44X		ICW 2.0
		E2L2	TF46X		ICW 2.1-3

E2N2	TF220	CCU Time
E2Q2	TF34X	ICW 2.0
E2R2	TF32X	ICW 2.0
E2U2	TF30X	ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X03	E3S2	TE50X	F-300	Output 46
		E3Q2	TE52X	F-210	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X04	E3S2	TE50X	F-300	Output 46
		E2C2	TF60X	F-210	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X05	E3S2	TE50X	F-310	
		E2C2	TF60X	F-210	
		E2V2	TF41X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X07	E3R2	TE26X	F-310	ICW 5.1
		E3S2	TE50X	F-210	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19" contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X08	E2D2	TF62X	F-300	ICW 5.5
		E2C2	TF60X	F-210	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2F2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32XICW 5.7		

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X09	E3L2	TE40X	F-320	ICW 6.5-6
		E3G2	TE21X	F-230	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19" contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X0A	E3P2	TE20X	F-320	
		E3G2	TE21X	F-230	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19" contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X0B	E2U2	TF30X	F-320	
		E2M2	TF31X	F-230	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X0C	E3S2	TE50X	F-340	ICW 12.0-7
		E3D2	TE34X	F-240	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X	ICW 13.0	
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X0D	E3S2	TE50X	F-350	Output 4F
		E2E2	TF80X	F-240	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X0E	E3S2	TE50X	F-290	ICW 16.0-7
		E3Q2	TE52X	F-240	ICW 16.2, 3
		E2E2	TF80X		ICW 16.4, 5, 7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.1
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X21	E3S2	TE50X	F-280	Input 44
		E3D2	TE34X	F-210	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7

E2B2	TF81X	ICW 0.7
E2N2	TF22X	ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X22	E3S2	TE50X	F-290	Output 45
		E2J2	TF50X	F-210	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0
		E2H2	TF42X		ICW 2.4,2.5
		E2K2	TF44X		ICW 2.0
		E2L2	TF46X		ICW 2.1-3
		E2N2	TF220		CCU Time
		E2Q2	TF34X		ICW 2.0
		E2R2	TF32X		ICW 2.0
		E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X23	E3S2	TE50X	F-300	Output 46
		E3Q2	TE52X	F-210	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X	ICW 3.4,3.7	
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X24	E3S2	TE50X	F-300	Output 46
		E2C2	TF60X	F-210	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71D	0X25	E3S2	TE50X	F-310
		E2C2	TF60X	F-210
		E2V2	TF41X	

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X27	E3R2	TE26X	F-310	ICW 5.1
		E3S2	TE50X	F-210	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19" contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X28	E2D2	TF62X	F-300	ICW 5.5
		E2C2	TF60X	F-210	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2F2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32XICW 5.7		

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X29	E3L2	TE40X	F-320	ICW 6.5-6
		E3G2	TE21X	F-230	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19" contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X2A	E3F2	TE20X	F-320
		E3G2	TE21X	F-230

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19" contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X2B	E2U2	TF30X	F-320
		E2M2	TF31X	F-230

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X2C	E3S2	TE50X	F-340	ICW 12.0-7
		E3D2	TE34X	F-240	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X		ICW 13.0
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X2D	E3S2	TE50X	F-350	Output 4F
		E2E2	TF80X	F-240	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71D	0X2E	E3S2	TE50X	F-290	ICW 16.0-7
		E3Q2	TE52X	F-240	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7

E2B2	TF81X	ICW 16.4-7
E2H2	TF42X	ICW 16.0,16.1
E2P2	TF82X	ICW 16.0-7
E2R2	TF32X	ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

X71E Ripple Zeros Vertically Through The ICWs

ROUTINE DESCRIPTION

This routine sets the diagnostic mode bit (see routine 18 description).

This routine checks for interaction between ICWs of different lines. All ICW bits for all lines are set on; the first ICW is set to all zeros and followed by the next ICW set to zero. The first ICW is then set to one's again and a check is made of the second (all zero) ICW to verify that no interaction occurred. The pattern is repeated using each ICW as the first in the test pair.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X01	E3S2	TE50X	F-280	Input 44
		E3D2	TE34X	F-210	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7
		E2B2	TF81X		ICW 0.7
		E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X02	E3S2	TE50X	F-290	Output 45
		E2J2	TF50X	F-210	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0
		E2H2	TF42X		ICW 2.4,2.5
		E2K2	TF44X		ICW 2.0
		E2L2	TF46X		ICW 2.1-3
		E2N2	TF220		CCU Time
		E2Q2	TF34X		ICW 2.0
		E2R2	TF32X		ICW 2.0
		E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X03	E3S2	TE50X	F-300	Output 46
		E3Q2	TE52X	F-210	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7

E2K2	TF44X	ICW 3.0-7
E2L2	TF46X	ICW 3.4,3.7
E2P2	TF82X	Output 46
E2Q2	TF341	Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X04	E3S2	TE50X	F-300	Output 46
	E2C2	TF60X	F-210	ICW 4.0-1
	E2E2	TF80X		ICW 4.0
	E2V2	TF41X		SDF 8, 9
	E2H2	TF42X		ICW 4.0,4.1
	E2K2	TF44X		ICW 4.0,4.1
	E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X05	E3S2	TE50X	F-310	
	E2C2	TF60X	F-210	
	E2V2	TF41X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X06				

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X07	E3R2	TE26X	F-310	ICW 5.1
	E3S2	TE50X	F-210	Output 47
	E2C2	TF60X		ICW 4.7, 5.0-3
	E2M2	TF31X		ICW 5.0-3
	E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19" contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X08	E2D2	TF62X	F-300	ICW 5.5
	E2C2	TF60X	F-210	ICW 5.4-7
	E2J2	TF50X		ICW 5.6
	E2F2	TF48X		ICW 5.4
	E2B2	TF81X		NRZI or XPar
	E2E2	TF80X		ICW 5.4
	E2H2	TF42X		ICW 5.4-7
	E2M2	TF31X		ICW 5.4-7
	E2N2	TF222		Test Mode

E2P2	TF82X	ICW 5.4
E2R2	TF32X	ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X09	E3L2	TE40X	F-320	ICW 6.5-6
	E3G2	TE21X	F-230	Input 48
	E3D2	TE34X		ICW 6.5
	E3J2	TE22X		ICW 7.0-7
	E3K2	TE24X		Write bytes 6, 7
	E3S2	TE50X		Input 48
	E3F2	TE20X		ICW 6.0-7
	E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19" contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X0A	E3F2	TE20X	F-320	
	E3G2	TE21X	F-230	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19" contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X0B	E2U2	TF30X	F-320	
	E2M2	TF31X	F-230	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X0C	E3S2	TE50X	F-340	ICW 12.0-7
	E3D2	TE34X	F-240	Output 4E, ICW 12.0-7
	E3L2	TE40X		ICW 12.0-7, 13.0-7
	E2J2	TF50X		ICW 13.3, 1.0
	E2E2	TF80X		ICW 13.0-7
	E2F2	TF48X		ICW 12.0-7, 13.2-5
	E2B2	TF81X		ICW 13.3
	E2R2	TF32X		ICW 13.1-3
	E2G2	TF40X		ICW 13.0-7
	E2H2	TF42X		ICW 13.3
	E2P2	TF82X		ICW 13.0
	E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE		CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X0D	E3S2	TE50X	F-350	Output 4F
		E2E2	TF80X	F-240	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE		CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X0E	E3S2	TE50X	F-290	ICW 16.0-7
		E3Q2	TE52X	F-240	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.1
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE		CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X21	E3S2	TE50X	F-280	Input 44
		E3D2	TE34X	F-210	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7
		E2B2	TF81X		ICW 0.7
		E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE		CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X22	E3S2	TE50X	F-290	Output 45
		E2J2	TF50X	F-210	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0

E2H2	TF42X	ICW 2.4,2.5
E2K2	TF44X	ICW 2.0
E2L2	TF46X	ICW 2.1-3
E2N2	TF220	CCU Time
E2Q2	TF34X	ICW 2.0
E2R2	TF32X	ICW 2.0
E2U2	TF30X	ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X23	E3S2	TE50X	F-300	Output 46
		E3Q2	TE52X	F-210	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X24	E3S2	TE50X	F-300	Output 46
		E2C2	TF60X	F-210	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X25	E3S2	TE50X	F-310	
		E2C2	TF60X	F-210	
		E2V2	TF41X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X27	E3R2	TE26X	F-310	ICW 5.1
		E3S2	TE50X	F-210	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3

E2M2	TF31X	ICW 5.0-3
E2V2	TF41X	ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19" contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X28	E2D2	TF62X	F-300	ICW 5.5
		E2C2	TF60X	F-210	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2P2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X29	E3L2	TE40X	F-320	ICW 6.5-6
		E3G2	TE21X	F-230	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 46
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19" contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X2A	E3F2	TE20X	F-320	
		E3G2	TE21X	F-230	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19" contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X2B	E2U2	TF30X	F-320	
		E2M2	TF31X	F-230	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X2C	E3S2	TE50X	F-340	ICW 12.0-7
		E3D2	TE34X	F-240	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X		ICW 13.0
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X2D	E3S2	TE50X	F-350	Output 4F
		E2E2	TF80X	F-240	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X2E	E3S2	TE50X	F-290	ICW 16.0-7
		E3Q2	TE52X	F-240	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.1
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X31	E3S2	TE50X	F-280	Input 44
		E3D2	TE34X	F-210	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7

E2B2	TF81X	ICW 0.7
E2N2	TF22X	ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X32	E3S2	TE50X	F-290	Output 45
	E2J2	TF50X	F-210	ICW 2.0, 2-4
	E2E2	TF80X		ICW 2.0
	E2H2	TF42X		ICW 2.4,2.5
	E2K2	TF44X		ICW 2.0
	E2L2	TF46X		ICW 2.1-3
	E2N2	TF220		CCU Time
	E2Q2	TF34X		ICW 2.0
	E2R2	TF32X		ICW 2.0
	E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X33	E3S2	TE50X	F-300	Output 46
	E3Q2	TE52X	F-210	Out Reg bus A.0-7
	E2C2	TF60X		ICW 3.1
	E2D2	TF62X		SDF 0-7
	E2J2	TF50X		Output 46
	E2F2	TF48X		EPCF bit 0
	E2G2	TF40X		SDF field
	E2B2	TF811		Force Constant to SDF
	E2H2	TF42X		ICW 3.0-7
	E2K2	TF44X		ICW 3.0-7
	E2L2	TF46X		ICW 3.4,3.7
	E2P2	TF82X		Output 46
	E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X34	E3S2	TE50X	F-300	Output 46
	E2C2	TF60X	F-210	ICW 4.0-1
	E2E2	TF80X		ICW 4.0
	E2V2	TF41X		SDF 8, 9
	E2H2	TF42X		ICW 4.0,4.1
	E2K2	TF44X		ICW 4.0,4.1
	E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71E	0X35	E3S2	TE50X	F-310
		E2C2	TF60X	F-210
		E2V2	TF41X	

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X37	E3R2	TE26X	F-310	ICW 5.1
		E3S2	TE50X	F-210	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19" contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X38	E2D2	TF62X	F-300	ICW 5.5
		E2C2	TF60X	F-210	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2P2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32XICW 5.7		

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X39	E3L2	TE40X	F-320	ICW 6.5-6
		E3G2	TE21X	F-230	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19" contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X3A	E3F2	TE20X	F-320
		E3G2	TE21X	F-230

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19" contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X3B	E2U2	TF30X	F-320	
	E2M2	TF31X	F-230	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X3C	E3S2	TE50X	F-340	ICW 12.0-7
	E3D2	TE34X	F-240	Output 4E, ICW 12.0-7
	E3L2	TE40X		ICW 12.0-7, 13.0-7
	E2J2	TF50X		ICW 13.3, 1.0
	E2E2	TF80X		ICW 13.0-7
	E2F2	TF48X		ICW 12.0-7, 13.2-5
	E2B2	TF81X		ICW 13.3
	E2R2	TF32X		ICW 13.1-3
	E2G2	TF40X		ICW 13.0-7
	E2H2	TF42X		ICW 13.3
	E2P2	TF82X		ICW 13.0
	E2V2	TF41X		ICW 12,0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X3D	E3S2	TE50X	F-350	Output 4F
	E2E2	TF80X	F-240	ICW 14.5
	E2T2	TF20X		ICW 14.0-7
	E2F2	TF48X		ICW 15.6
	E2N2	TF22X		ICW 14.0-7
	E2S2	TF21X		ICW 15.0-7
	E2P2	TF82X		ICW 14.1 set
	E2Q2	TF34X		ICW 14.1,15.0-7
	E2R2	TF32X		ICW 15.7
	E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X3E	E3S2	TE50X	F-290	ICW 16.0-7
	E3Q2	TE52X	F-240	ICW 16.2,3
	E2E2	TF80X		ICW 16.4,5,7
	E2F2	TF48X		ICW 16.4-7
	E2S2	TF21X		ICW 16.0-7

E2B2	TF81X		ICW 16.4-7
E2H2	TF42X		ICW 16.0,16.1
E2P2	TF82X		ICW 16.0-7
E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X41	E3S2	TE50X	F-280	Input 44
	E3D2	TE34X	F-210	Output 44, ICW 0.4
	E3Q2	TE52X		Encode for str
	E3E2	TE70X		Input 42 or 43 bits
	E2T2	TF20X		ICW 0.7
	E2B2	TF81X		ICW 0.7
	E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X42	E3S2	TE50X	F-290	Output 45
	E2J2	TF50X	F-210	ICW 2.0, 2-4
	E2E2	TF80X		ICW 2.0
	E2H2	TF42X		ICW 2.4,2.5
	E2K2	TF44X		ICW 2.0
	E2L2	TF46X		ICW 2.1-3
	E2N2	TF220		CCU Time
	E2Q2	TF34X		ICW 2.0
	E2R2	TF32X		ICW 2.0
	E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X43	E3S2	TE50X	F-300	Output 46
	E3Q2	TE52X	F-210	Out Reg bus A.0-7
	E2C2	TF60X		ICW 3.1
	E2D2	TF62X		SDF 0-7
	E2J2	TF50X		Output 46
	E2F2	TF48X		EPCF bit 0
	E2G2	TF40X		SDF field
	E2B2	TF811		Force Constant to SDF
	E2H2	TF42X		ICW 3.0-7
	E2K2	TF44X		ICW 3.0-7
	E2L2	TF46X		ICW 3.4,3.7
	E2P2	TF82X		Output 46
	E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X44	E3S2	TE50X	F-300	Output 46
		E2C2	TF60X	F-210	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X45	E3S2	TE50X	F-310
		E2C2	TF60X	F-210
		E2V2	TF41X	

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X47	E3R2	TE26X	F-310	ICW 5.1
		E3S2	TE50X	F-210	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19" contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X48	E2D2	TF62X	F-300	ICW 5.5
		E2C2	TF60X	F-210	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2F2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X49	E3L2	TE40X	F-320	ICW 6.5-6
		E3G2	TE21X	F-230	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7

B3S2	TE50X	Input 48
B3F2	TE20X	ICW 6.0-7
B2F2	TF48B	Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19" contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X4A	B3F2	TE20X	F-320	
	B3G2	TE21X	F-230	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19" contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X4B	B2U2	TF30X	F-320	
	B2M2	TF31X	F-230	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X4C	B3S2	TE50X	F-340	ICW 12.0-7
	B3D2	TE34X	F-240	Output 4E, ICW 12.0-7
	B3L2	TE40X		ICW 12.0-7, 13.0-7
	B2J2	TF50X		ICW 13.3, 1.0
	B2E2	TF80X		ICW 13.0-7
	B2F2	TF48X		ICW 12.0-7, 13.2-5
	B2B2	TF81X		ICW 13.3
	B2R2	TF32X		ICW 13.1-3
	B2G2	TF40X		ICW 13.0-7
	B2H2	TF42X		ICW 13.3
	B2P2	TF82X		ICW 13.0
	B2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X4D	B3S2	TE50X	F-350	Output 4F
	B2E2	TF80X	F-240	ICW 14.5
	B2T2	TF20X		ICW 14.0-7
	B2F2	TF48X		ICW 15.6
	B2N2	TF22X		ICW 14.0-7
	B2S2	TF21X		ICW 15.0-7
	B2P2	TF82X		ICW 14.1 set
	B2Q2	TF34X		ICW 14.1,15.0-7

B2R2	TF32X	ICW 15.7
B3D2	TE34X	ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X4E			
	B3S2	TE50X	F-290	ICW 16.0-7
	B3Q2	TE52X	F-240	ICW 16.2,3
	B2E2	TF80X		ICW 16.4,5,7
	B2F2	TF48X		ICW 16.4-7
	B2S2	TF21X		ICW 16.0-7
	B2B2	TF81X		ICW 16.4-7
	B2H2	TF42X		ICW 16.0,16.1
	B2P2	TF82X		ICW 16.0-7
	B2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X51			
	B3S2	TE50X	F-280	Input 44
	B3D2	TE34X	F-210	Output 44, ICW 0.4
	B3Q2	TE52X		Encode for str;
	B3E2	TE70X		Input 42 or 43 bits
	B2T2	TF20X		ICW 0.7
	B2B2	TF81X		ICW 0.7
	B2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
B3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X52			
	B3S2	TE50X	F-290	Output 45
	B2J2	TF50X	F-210	ICW 2.0, 2-4
	B2E2	TF80X		ICW 2.0
	B2H2	TF42X		ICW 2.4,2.5
	B2K2	TF44X		ICW 2.0
	B2L2	TF46X		ICW 2.1-3
	B2N2	TF220		CCU Time
	B2Q2	TF34X		ICW 2.0
	B2R2	TF32X		ICW 2.0
	B2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71E	0X53	E3S2	TE50X	F-300	Output 46
		E3Q2	TE52X	F-210	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X54	E3S2	TE50X	F-300	Output 46
	E2C2	TF60X	F-210	ICW 4.0-1
	E2E2	TF80X		ICW 4.0
	E2V2	TF41X		SDF 8, 9
	E2H2	TF42X		ICW 4.0,4.1
	E2K2	TF44X		ICW 4.0,4.1
	E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'10' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X55	E3S2	TE50X	F-310	
	E2C2	TF60X	F-210	
	E2V2	TF41X		

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X57	E3R2	TE26X	F-310	ICW 5.1
	E3S2	TE50X	F-210	Output 47
	E2C2	TF60X		ICW 4.7, 5.0-3
	E2M2	TF31X		ICW 5.0-3
	E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19" contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E 0X58	E2D2	TF62X	F-300	ICW 5.5
	E2C2	TF60X	F-210	ICW 5.4-7
	E2J2	TF50X		ICW 5.6
	E2F2	TF48X		ICW 5.4
	E2B2	TF81X		NRZI or XPar
	E2E2	TF80X		ICW 5.4

E2H2	TF42X	ICW 5.4-7
E2M2	TF31X	ICW 5.4-7
E2N2	TF222	Test Mode
E2P2	TF82X	ICW 5.4
E2R2	TF32X	ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X59	E3L2	TE40X	F-320	ICW 6.5-6
		E3G2	TE21X	F-230	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19" contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X5A	E3F2	TE20X	F-320	
		E3G2	TE21X	F-230	

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19" contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X5B	E2U2	TF30X	F-320	
		E2M2	TF31X	F-230	

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X5C	E3S2	TE50X	F-340	ICW 12.0-7
		E3D2	TE34X	F-240	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3, 1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X		ICW 13.0
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:

E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X5D	E3S2	TE50X	F-350	Output 4F
		E2E2	TF80X	F-240	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X5E	E3S2	TE50X	F-290	ICW 16.0-7
		E3Q2	TE52X	F-240	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.1
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X61	E3S2	TE50X	F-280	Input 44
		E3D2	TE34X	F-210	Output 44, ICW 0.4
		E3Q2	TE52X		Encode for str
		E3E2	TE70X		Input 42 or 43 bits
		E2T2	TF20X		ICW 0.7
		E2B2	TF81X		ICW 0.7
		E2N2	TF22X		ICW 0.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 0 bits 0 through 7 via an output X'44'. The bits read via an Input X'44' were not equal to those set.

Register X'19' contains the bits that were set via the output X'44'. Register X'18' contains the bits expected in the Input X'44'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71E	0X62	E3S2	TE50X	F-290	Output 45
		E2J2	TF50X	F-210	ICW 2.0, 2-4
		E2E2	TF80X		ICW 2.0
		E2H2	TF42X		ICW 2.4,2.5
		E2K2	TF44X		ICW 2.0
		E2L2	TF46X		ICW 2.1-3
		E2N2	TF220		CCU Time
		E2Q2	TF34X		ICW 2.0
		E2R2	TF32X		ICW 2.0
		E2U2	TF30X		ICW 2.0-7

One or more bits were set in the ICW byte 2 bits 0 through 7 via an output X'45'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X63	E3S2	TE50X	F-300	Output 46
		E3Q2	TE52X	F-210	Out Reg bus A.0-7
		E2C2	TF60X		ICW 3.1
		E2D2	TF62X		SDF 0-7
		E2J2	TF50X		Output 46
		E2F2	TF48X		EPCF bit 0
		E2G2	TF40X		SDF field
		E2B2	TF811		Force Constant to SDF
		E2H2	TF42X		ICW 3.0-7
		E2K2	TF44X		ICW 3.0-7
		E2L2	TF46X		ICW 3.4,3.7
		E2P2	TF82X		Output 46
		E2Q2	TF341		Force Constant to SDF

One or more bits were set in the ICW byte 3 bits 0 through 7 via an output X'46'. The bits read via an Input X'45' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'45'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X64	E3S2	TE50X	F-300	Output 46
		E2C2	TF60X	F-210	ICW 4.0-1
		E2E2	TF80X		ICW 4.0
		E2V2	TF41X		SDF 8, 9
		E2H2	TF42X		ICW 4.0,4.1
		E2K2	TF44X		ICW 4.0,4.1
		E2L2	TF46X		ICW 4.0,4.1

One or more bits were set in the ICW byte 4 bits 0 through 1 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X65	E3S2	TE50X	F-310
		E2C2	TF60X	F-210
		E2V2	TF41X	

One or more bits were set in the ICW byte 4 bits 2 through 5 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X71E	0X67	E3R2	TE26X	F-310	ICW 5.1
		E3S2	TE50X	F-210	Output 47
		E2C2	TF60X		ICW 4.7, 5.0-3
		E2M2	TF31X		ICW 5.0-3
		E2V2	TF41X		ICW 4.0-7

One or more bits were set in the ICW byte 4 bit 7 and byte 5 bits 0 through 3 via an output X'47'. The bits read via an Input X'47' were not equal to those set.

Register X'19" contains the bits that were set via the output X'47'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X68	E2D2	TF62X	F-300	ICW 5.5
		E2C2	TF60X	F-210	ICW 5.4-7
		E2J2	TF50X		ICW 5.6
		E2P2	TF48X		ICW 5.4
		E2B2	TF81X		NRZI or XPar
		E2E2	TF80X		ICW 5.4
		E2H2	TF42X		ICW 5.4-7
		E2M2	TF31X		ICW 5.4-7
		E2N2	TF222		Test Mode
		E2P2	TF82X		ICW 5.4
		E2R2	TF32X		ICW 5.7

One or more bits were set in the ICW byte 5 bits 4 through 7 via an output X'46'. The bits read via an Input X'47' were not equal to those set.

Register X'19' contains the bits that were set via the output X'46'. Register X'18' contains the bits expected in the Input X'47'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X69	E3L2	TE40X	F-320	ICW 6.5-6
		E3G2	TE21X	F-230	Input 48
		E3D2	TE34X		ICW 6.5
		E3J2	TE22X		ICW 7.0-7
		E3K2	TE24X		Write bytes 6, 7
		E3S2	TE50X		Input 48
		E3F2	TE20X		ICW 6.0-7
		E2F2	TF488		Set ICW 6.6 DLE ITB END

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 6 bits 0 through 7 and byte 7 bits 0 through 7 via an output X'48'. The bits read via an Input X'48' were not equal to those set.

Register X'19" contains the bits that were set via the output X'48'. Register X'18' contains the bits expected in the Input X'48'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X6A	E3F2	TE20X	F-320
		E3G2	TE21X	F-230

One or more bits were set in the ICW byte 8 bits 0 through 7 and byte 9 bits 0 through 7 via an output X'49'. The bits read via an Input X'49' were not equal to those set.

Register X'19" contains the bits that were set via the output X'49'. Register X'18' contains the bits expected in the Input X'49'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X6B	E2U2	TF30X	F-320
		E2M2	TF31X	F-230

One or more bits were set in the ICW byte 10 bits 0 through 7 and byte 11 bits 0 through 7 via an output X'4A'. The bits read via an Input X'4A' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4A'. Register X'18' contains the bits expected in the Input X'4A'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X6C	E3S2	TE50X	F-340	ICW 12.0-7
		E3D2	TE34X	F-240	Output 4E, ICW 12.0-7
		E3L2	TE40X		ICW 12.0-7, 13.0-7
		E2J2	TF50X		ICW 13.3,1.0
		E2E2	TF80X		ICW 13.0-7
		E2F2	TF48X		ICW 12.0-7, 13.2-5
		E2B2	TF81X		ICW 13.3
		E2R2	TF32X		ICW 13.1-3
		E2G2	TF40X		ICW 13.0-7
		E2H2	TF42X		ICW 13.3
		E2P2	TF82X		ICW 13.0
		E2V2	TF41X		ICW 12.0-7

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 12 bits 0 through 7 and byte 13 bits 0 through 7 via an output X'4E'. The bits read via an Input X'4E' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4E'. Register X'18' contains the bits expected in the Input X'4E'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X6D	E3S2	TE50X	F-350	Output 4F
		E2E2	TF80X	F-240	ICW 14.5
		E2T2	TF20X		ICW 14.0-7
		E2F2	TF48X		ICW 15.6
		E2N2	TF22X		ICW 14.0-7
		E2S2	TF21X		ICW 15.0-7
		E2P2	TF82X		ICW 14.1 set
		E2Q2	TF34X		ICW 14.1,15.0-7
		E2R2	TF32X		ICW 15.7
		E3D2	TE34X		ICW 14.2

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

One or more bits were set in the ICW byte 14 bits 0 through 7 and byte 15 bits 0 through 7 via an output X'4F'. The bits read via an Input X'4F' were not equal to those set.

Register X'19" contains the bits that were set via the output X'4F'. Register X'18' contains the bits expected in the Input X'4F'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X71E	0X6E	E3S2	TE50X	F-290	ICW 16.0-7
		E3Q2	TE52X	F-240	ICW 16.2,3
		E2E2	TF80X		ICW 16.4,5,7
		E2F2	TF48X		ICW 16.4-7
		E2S2	TF21X		ICW 16.0-7
		E2B2	TF81X		ICW 16.4-7
		E2H2	TF42X		ICW 16.0,16.1
		E2P2	TF82X		ICW 16.0-7
		E2R2	TF32X		ICW 16.0-7

One or more bits were set in the ICW byte 16 bits 0 through 7 via an output X'45'. The bits read via an Input X'4B' were not equal to those set. Register X'19' contains the bits that were set via the output X'45'. Register X'18' contains the bits expected in the Input X'4B'. Register X'15' contains the bits in error. Register X'11' contains the ICW line address under test.

X720 PDF Array Data Testing

ROUTINE DESCRIPTION

This routine sets the diagnostic mode bit (see routine 18 for description).

The PDF array for each line address is checked that it can be set to all ones and reset to all zeros. Also, alternate bits are set in the array to check that no interaction between bits occurs. The array address are checked to see that they do not change because of input instructions.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X720	0X01	E2F2	TF48X	F-330
		E3D2	TE34X	F-240
		E3S2	TE50X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The array address is set to X'0000' and an output X'4C' sets bits 0-10 in the array. An input X'4E' verifies that the PDF array address did not change because of the output X'4C'. Register X'15' contains the bits in error and register X'13' contains the expected PDF array address. Register X'11' contains the ICW line address and register X'18' contains the data set into the array.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X720	0X02	E3S2	TE50X	F-240
		E3D2	TE34X	
		E3N2	TE30X	
		E3M2	TE32X	
		E2C2	TF60X	
		E2H2	TF42X	
		E2K2	TF44X	
		E3L2	TE40X	
		E3P2	TE31X	
		E2E2	TF80X	
		E2R2	TF32X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3P2 has been deleted.

The PDF arrays are set with data and read to verify that the data set correctly. The input data from the array using an input X'4C' did not agree with the data set.

Register X'11' contains the ICW line address. Register X'15' contains the bits in error and register X'18' contains the expected data.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X720	0X03	E3N2	TE30X	F-210
		E3P2	TE31X	
		E3M2	TE32X	
		E3D2	TE34X	
		E2C2	TF60X	
		E2F2	TF48X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3P2 has been deleted.

After data was set into the array, the data is read to verify that the data set correctly. The data is read via an input X'44'; the data read did not agree with the data set.

Register X'11' contains the ICW line address and register X'13' contains the expected PDF array data. Register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X720	0X04	E3N2	TE30X	F-330
		E3P2	TE31X	
		E3M2	TE32X	
		E3D2	TE34X	
		E2C2	TF60X	
		E2F2	TF48X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3P2 has been deleted.

After reading the data from the PDF array via an input X'44' and input X'4C', the array address is checked to verify that it did not change.

Register X'11' contains the ICW line address and register X'13' contains the expected array address. Register X'15' contains the address bits in error.

X722 Array Addressing Test

ROUTINE DESCRIPTION

This routine sets the diagnostic mode bit (see routine 18 for description).

Data is set into the array using the cycle steal address pointer (ICW bits 12.0-12.3) along with an output X'4D'. The data is X'11' for address 1, X'22' for address 2, etc. Address 0 has data of X'88'. The PDF address pointer (ICW bits 12.4-12.7) is used with an input X'44' to read the data out of the array.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X722	0X01 E3S2	TE50X	F-330	
	E3D2	TE34X		
	E3P2	TE31X		
	E3N2	TE30X		
	E3M2	TE32X		
	E3Q2	TE52X		
	E3L2	TE40X		
	E2N2	TF22X		
	E2P2	TF82X		

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3P2 has been deleted.

The data read from the array using the PDF address did not agree with the data set into the array.

Register X'15' contains the bits in error and register X'18' contains in byte 1 the expected data. Byte 0 of register X'18' contains the PDF address used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X722	0X02 E3D2	TE34X	F-330	
	E3L2	TE40X		
	E3S2	TE50X		
	E3M2	TE32X		

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The data read from the array using the PDF address did not agree with the data set into the array.

Register X'15' contains the bits in error and register X'18' contains (in byte 1) the expected data. Byte 0 of register X'18' contains the PDF address used.

X726 Scan Limit Test Scan Limit=00

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

All lines successively have the level 2 Pending bit turned on and depending upon how the scan limit is set, the line is checked that it should or should not cause an interrupt.
With an upper scan limit of 00 set, all lines should interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X726	0X01 E3L2	TE40X	F-100	
	E3D2	TE34X		
	E3E2	TE70X		
	E3R2	TE26X		
	E3H2	TE54X		
	E3S2	TE50X		
	E3Q2	TE52X		
	E2D2	TF62X		

E2F2	TF48X	
E2B2	TF81X	
E2N2	TF22X	
B3D2	CX004	
E2G2	TF40X	

No level 2 interrupt occurred from the expected line address.

Register X'11' contains the line address of the line expecting the level 2 interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X726	0X02	E3L2	TE40X	F-550
		E3F2	TE20X	F-560
		E3R2	TE26X	
		E3H2	TE54X	
		E2D2	TF62X	
		B3D2	CX004	
		E3G2	TF21X	
		E2G2	TF40X	
		E2V2	TF41X	
		E2T2	TF20X	
		E2S2	TF21X	
		E2M2	TF31X	

A level 2 interrupt occurred from an unexpected line address.

Register X'14' contains the line address causing the unexpected level 2 interrupt.
Register X'11' contains the line address of the line expecting the level 2 interrupt.

X72B Scan Limit Test Scan Limit=01

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

Each line in turn has the level 2 pending bit set on and depending upon how the scan limit is set, the line is checked that it should or should not interrupt.

With a scan limit of 01 set, only the first eight lines should interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72B	0X01	E3H2	TE54X	F-100
		E3R2	TE26X	
		E2E2	TF80X	
		B3D2	CX004	
		E2F2	TF48X	
		E3L2	TE40X	

No level 2 interrupt occurred from the expected line address.

Register X'11' contains the line address of the line expecting the level 2 interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72B	0X02	E3R2	TE26X	F-550
		E3H2	TE54X	F-560
		E3F2	TE20X	
		E2E2	TF80X	
		B3D2	CX004	
		E2F2	TF48X	
		E3L2	TE40X	

A level 2 interrupt occurred from an unexpected line address.

Register X'14' contains the line address causing the unexpected level 2 interrupt.
Register X'11' contains the line address of the line expecting the level 2 interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72B	0X03	E3E2	TE70X	F-100
		E3H2	TE54X	

E3S2	TE50X
E3Q2	TE52X
E2E2	TF80X
B3D2	CX004
E2F2	TF48X
E3L2	TE40X

A level 2 interrupt occurred from a line address that should not have been scanned.

Register X'14' has the line address of the line causing the level 2 interrupt. Register X'11' contains the line address of the line under test.

X72C Scan Limit TestScan Limit=11

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present. Each line in turn has the level 2 pending bit turned on and dupending upon how the scan limit is set, the line is checked that it should or should not interrupt.

With a scan limit of 11 set, only the first 16 lines should interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72C 0X01	E3E2	TE70X	F-100	
	B3H2	TE54X		
	E2E2	TF80X		
	B3D2	CX004		
	E2F2	TF48X		
	E3L2	TE40X		

No level 2 interrupt occurred from the expected line address.

Register X'11' contains the line address of the line expecting a level 2 interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72C 0X02	B3R2	TE26X	F-550	
	E3H2	TE54X	F-560	
	E3E2	TE70X		
	E2E2	TF80X		
	B3D2	CX004		
	E3L2	TE40X		
	E2F2	TF48X		

A level 2 interrupt occurred from an unexpected line address.

Register X'14' contains the line address causing the unexpected level 2 interrupt.
Register X'11' contains the line address of the line expecting the interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72C 0X03	E3H2	TE54X	F-100	
	E2E2	TF80X		
	B3D2	CX004		
	E2F2	TF48X		
	E3L2	TE40X		

- A level 2 interrupt occurred from a line address that should not have been scanned.

Register X'14' contains the line address of the line causing the level 2 interrupt.
Register X'11' contains the line address of the line under test.

X72D Scan Limit TestScan Limit=10

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

Each line in turn has the level 2 pending bit turned on and depending upon how the scan limit is set, the line is checked that it should or should not interrupt.

With a scan limit of 10 set, only the first 32 lines should interrupt.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72D	0X01	E3H2	TE54X	F-100	
		E2E2	TF80X		
		B3D2	CX004		
		E2F2	TF48X		
		E3L2	TE40X		

No level 2 interrupt occurred from the expected line address.

Register X'11' contains the line address of the line expecting the interrupt.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72D	0X02	E3H2	TE54X	F-550	
		E3F2	TE20X	F-560	
		E2E2	TF80X		
		B3D2	CX004		
		E2F2	TF48X		
		E3L2	TE40X		

A level 2 interrupt occurred from an unexpected line address.

Register X'14' contains the line address causing the unexpected level 2 interrupt.
Register X'11' contains the line address of the line expecting the level 2 interrupt.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72D	0X03	E2E2	TF80X	F-100	
		B3D2	CX004		
		E2F2	TF48X		
		E3L2	TE40X		

A level 2 interrupt occurred from a line address that should not have been scanned.

Register X'14' contains the line address of the line causing the level 2 interrupt.
Register X'11' contains the line address of the line under test.

X72F Interrupt Priority Register Test

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

The first four ICW's are set up with priority settings of 3, 2, 1, and 0 in that order. ICW bit 5.1 (interrupt request pending) is set on in the four ICW's and level 2 interrupts are unmasked. The ICW's are checked to ensure that interrupts occur in the proper order. The proper order is for the first, second, third, and the fourth ICW to interrupt in sequence.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72F	0X01	E2E2	TF80X	F-020	
		B3D2	CX009	F-180	
		B3E2	CX001		
		E2F2	TF48X		
		E3L2	TE40X		
		E3R2	TE26X		

Level 2 interrupts did not occur after unmasking level 2. Register X'13' contains the line address of the line the level 2 was expected from.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X72F	0X02	B3D2	CX009	F-020	
		B3E2	CX001	F-180	
		E3R2	TE26X		
		E3F2	TE20X		
		E2E2	TF80X		
		E2F2	TF48X		
		E3L2	TE40X		

The level 2 interrupt occurred from the wrong line address. Register X'13' contains the line address the level 2 interrupt was expected from. Register X'14' contains the line address causing the interrupt.

X730 Substitution Control Register Test

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

The substitution control register bit one is set on and an attempt is made to cause a level 2 interrupt on lines E and F of all LIB's. These address should not be scanned.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X730	0X01 E3H2	TE54X	F-100	
	E3F2	TE20X	F-250	
	E2E2	TF80X		
	B3D2	CX009		
	B3E2	CX001		
	E2F2	TF48X		
	E3L2	TE40X		

An unexpected level 2 interrupt occurred. Register X'14' contains the line address of the line causing the interrupt. Register X'11' contains the line address of the line with ICW bit 5.1 (L2 pending) set on. If register X'11' does not equal register X'14', there may not be a LIB or scanner failure.

If register X'14' equals register X'11', substitution control register bit 1 is not working properly. The line addressed by register X'14' should not have been scanned and should not have interrupted.

X731 Substitution Control Register Test

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

The substitution control register bit two is set on and an attempt is made to cause a level 2 interrupt on lines C and D of all LIB's. These address should not be scanned.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X731	0X01 E3H2	TE54X	F-100	
	E3F2	TE20X	F-250	
	E2E2	TF80X		
	B3D2	CX009		
	B3E2	CX001		
	E2F2	TF48X		
	E3L2	TE40X		

An unexpected level 2 interrupt occurred. Register X'14' contains the line address of the line causing the interrupt. Register X'11' contains the line address of the line with ICW bit 5.1 (L2 pending) set on. If register X'11' does not equal register X'14', there may not be a LIB or scanner failure.

If register X'14' equals register X'11', substitution control register bit 1 is not working properly. The line addressed by register X'14' should not have been scanned and should not have interrupted.

X732 Substitution Control Register Test

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

The substitution control register bit three is set on and an attempt is made to cause a level 2 interrupt on lines A and B of all LIB's. These address should not be scanned.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X732	0X01 E3H2	TE54X	F-100	
	E3F2	TE20X	F-250	

	E2E2	TF80X
	B3D2	CX009
	B3E2	CX001
	E2F2	TF48X
	E3L2	TE40X

An unexpected level 2 interrupt occurred. Register X'14' contains the line address of the line causing the interrupt. Register X'11' contains the line address of the line with ICW bit 5.1 (L2 pending) set on. If register X'11' does not equal register X'14', there may not be a LIB or scanner failure.

If register X'14' equals register X'11', substitution control register bit 3 is not working properly. The line addressed by register X'14' should not have been scanned and should not have interrupted.

X733 Substitution Control Register Test

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

The substitution control register bit four is set on and an attempt is made to cause a level 2 interrupt on lines 8 and 9 of all LIB's. These address should not be scanned.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X733	0X01	B3H2	TE54X	F-100
		E3F2	TE20X	F-250
		E2E2	TF80X	
		B3D2	CX009	
		B3E2	CX001	
		E2F2	TF48X	
		E3L2	TE40X	

An unexpected level 2 interrupt occurred. Register X'14' contains the line address of the line causing the interrupt. Register X'11' contains the line address of the line with ICW bit 5.1 (L2 pending) set on. If register X'11' does not equal register X'14', there may not be a LIB or scanner failure.

If register X'14' equals register X'11', substitution control register bit 4 is not working properly. The line addressed by register X'14' should not have been scanned and should not have interrupted.

X736 High Speed Selection Register

ROUTINE DESCRIPTION

NOTE **** This routine is by-passed if the High Speed Scanner Feature (230.4 KBPS) is present.

All bits in the high speed selection register are set on and the corresponding line address is checked that it will or will not interrupt. The line address for each line is stored in the BCC field of input X'4A'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X736	0X01	E3R2	TE26X	F-090
		E3H2	TE54X	

The expected line address did not interrupt. Register X'11' contains the line address expected to interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X736	0X02	E3L2	TE40X	F-090
		E3H2	TE54X	

An unexpected line address caused the interrupt.

Register X'13' contains the line address expected to interrupt; register X'14' contains the address of the line causing the interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION

X736	0X03	E2B2	TF81X	F-090
		E3H2	TE54X	

The address stored in the BCC field (register X'4A') did not equal the ABAR (input X'40').

Register X'14' conatins the BCC field data; register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X736	0X04	E3H2	TE54X	F-090
		E3S2	TE50X	
		E3F2	TE20X	

An unscanned line caused an interrupt.

Register X'14' contains the address of the unscanned line causing the interrupt.

X738 Interrupt Request Pending

ROUTINE DESCRIPTION

This routine verifies that when a priority register is occupied, the interrupt pending bit is set. The level 2 interrupt should occur when the priority register is free.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X738	0X01	E2N2	TF22X	F-550
		E2E2	TF80X	
		E2F2	TF48X	
		E3L2	TE40X	

The level 2 interrupt request pending bit did not set in Register X'47'. Register X'13' contains the line address that should have priority 3 set. Register X'16' contains the line address that should have the interrupt request pending bit on. Register X'16' should equal Register X'40'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X738	0X02	E2N2	TF22X	F-550
		E3R2	TE26X	
		E2E2	TF80X	
		E2F2	TF48X	
		E3L2	TE40X	

No level 2 interrupt occurred. A level 2 interrupt should occur from the line address contained in Register X'13'. Register X'16' contains the line address of the next expected level 2 interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X738	0X03	E2N2	TF22X	F-550
		E2E2	TF80X	
		E2F2	TF48X	
		E3L2	TE40X	

The first level 2 interrupt occurred from an unexpected line. Register X'13' contains the line address the interrupt was expected from. Register X'14' contains the line address causing the level 2 interrupt and Register X'16' contains the line address of the next expected interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X738	0X04	E2N2	TF22X	F-550
		E2E2	TF80X	
		E2F2	TF48X	
		E3L2	TE40X	

No level 2 interrupt occurred from the second line with the interrupt pending bit set on. Register X'13' contains the line address of the line that should have interrupted previously. Register X'16' contains the line address expected to cause the interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X738	0X05 E2N2	TF22X	F-550	
	E3F2	TE20X		
	E2E2	TF80X		
	E2F2	TF48X		
	E3L2	TE40X		

The second level 2 interrupt occurred from the wrong line. Register X'13' contains the line address of the previous line that should have caused an interrupt. Register X'14' contains the line address of the line causing the level 2 interrupt. Register X'16' contains the line address expected to cause the level 2 interrupt.

X741 Line Select Problem Determination

ROUTINE DESCRIPTION

This routine must be selected via the problem determination mode selection.

This routine provides the ability to select the pair of line addresses to be used in the internal wrap routines of the type 3 communication scanner. However, this routine does not alter the adapter selection mechanism of the DCM. If routines are running on the first adapter, selecting an address for the second adapter forces the equivalent address for the first adapter.

The routines run normally on the first two even line addresses (0X40 and 0X44).

ERROR CODE	
X741	FX98

Enter the receive line wrap address to be used for all internal wrap testing.

ERROR CODE	
X741	FX99

Enter the transmit line wrap address to be used for all internal wrap testing.

X742 Basic BSC Wrap Test LCD=4 EBCDIC EP

ROUTINE DESCRIPTION

This routine tests:

Transmit PAD insertion on 8/0 to 9/C state transition, SDF shift of PAD, Tag detect and PDF to SDF shift, PDF pointer incrementing.
Receive SDF shift receive marks and first SYN character, first SYN causes change from 4/0 to 5/1, second SYN causes change to 5/C, data wraps correctly from transmit to receive. Diag 0=1 and Diag 1=1 is set for both lines. Cycle steal is not used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X01 E3C2	TE71X	F-220
	E3L2	TE40X	F-550
	E3Q2	TE52X	
	E3S2	TE50X	
	E2J2	TF50X	
	E2D2	TF62X	
	E2C2	TF60X	
	E2H2	TF42X	
	E2P2	TF82X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X02 E3F2	TE20X	F-220
	E3R2	TE26X	F-550
	E2J2	TF50X	
	E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X03 E3D2	TE34X	F-580
	E2B2	TF81X	F-590
	E2J2	TF50X	F-570
	E2D2	TF62X	
	E2C2	TF60X	
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	
	E2H2	TF42X	
	E2L2	TF46X	
	E2E2	TF80X	
	E2P2	TF82X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 9/C with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X04 E3D2	TE34X	F-410
	E3L2	TE40X	F-420
	E2B2	TF81X	
	E2N2	TF22X	
	E2D2	TF62X	
	E2Q2	TF34X	
	E2F2	TF48X	
	E2H2	TF42X	
	E2K2	TF44X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X05 E3G2	TE21X	F-410
	E3S2	TE50X	F-420
	E3L2	TE40X	
	E3F2	TE20X	
	E2J2	TF50X	
	E2D2	TF62X	
	E2C2	TF60X	
	E2H2	TF42X	
	E2L2	TF46X	
	E2G2	TF40X	
	E2T2	TF20X	
	E2S2	TF21X	
	E2U2	TF30X	

		E2M2	TF31X	
		E2V2	TF41X	

SDF is not shifting properly. SDF did not go to X'00AA'. Reg X'15' contains SDF at timeout (bits 0.6-1.7)

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X06	E2B2	TF81X	F-410
		E2J2	TF50X	F-420
		E2D2	TF62X	
		E2E2	TF80X	
		E2R2	TF32X	
		E2F2	TF48X	
		E3D2	TE34X	
		E2H2	TF42X	
		E2C2	TF60X	
		E2P2	TF82X	
		E2K2	TF44X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

Transmit tag bit was not detected. Either the PDF to SDF transfer failed or the SDF did not shift properly. Register X'11' is the line under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X07	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X08	E3R2	TE26X	F-380
		E3D2	TE34X	F-390
		E3L2	TE40X	
		E2N2	TF22X	
		E2B2	TF81X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF1 pointer did not increment properly with PDF to SDF shift. The expected PDF1 pointer value was ICW bits 12.4, 12.5, and 12.6 off and 12.7 on.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X09	E3K2	TE24X	F-480
		E3D2	TE34X	F-500
		E3L2	TE40X	
		E3Q2	TE52X	
		E2C2	TF60X	
		E2B2	TF81X	
		E2J2	TF50X	
		E2N2	TF22X	
		E2D2	TF62X	
		E2F2	TF48X	
		E2H2	TF42X	
		E2K2	TF44X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The receive line SDF should contain X'0080'. The incorrect SDF data is contained in register X'15' bit 0.6 through 1.7.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X742	0X0A	E2B2	TF81X	F-480
		E2C2	TF60X	F-500
		E2H2	TF42X	
		E3J2	TE22X	

Receive SDF did not shift properly or the wrap function was incorrect. The SDF should contain X'00FF'; the incorrect SDF data is contained in register X'15' bits 0.6 through 1.7.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X0B	E3K2	TE24X	F-480
		E3D2	TE34X	
		E3L2	TE40X	
		E2D2	TF62X	
		E2C2	TF60X	
		E2E2	TF80X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The receive line SDF should contain X'0165'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X0C	E2B2	TF81X	F-580
		E2J2	TF50X	F-600
		E2D2	TF62X	F-570
		E2Q2	TF34X	
		E2R2	TF32X	
		E3L2	TE40X	
		E2K2	TF44X	
		E2H2	TF42X	
		E2E2	TF80X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X0D	E2B2	TF81X	F-580
		E2J2	TF50X	F-590
		E2H2	TF42X	
		E2K2	TF44X	

The PCF/EPCF should be 7/C with sequence bit 13.0 undefined. Refer to BSC Receive state transition 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X0E	E2B2	TF81X	F-480
		E2J2	TF50X	F-500
		E2E2	TF80X	
		E2C2	TF60X	

Tag time was not detected on the receive line. Routine did not see ICW bit 4.1 turn on and then turn off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X0F	E2B2	TF81X	F-410
		E2J2	TF50X	F-420
		E2H2	TF42X	

Tag time was not detected on transmit line. ICW bit 3.2 (tag bit) either did not turn on after going off (tag bit set at tag time), or it never went off (SDF shifting).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X10 E2B2	TF81X	F-480
	E2C2	TF60X	F-500
	E2E2	TF80X	
	E2J2	TF50X	

Tag time was not detected on receive line. Routine did not see ICW bit 4.1 turn on and then turn off. Last character being received.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X742	0X11 E2B2	TF81X	F-480
	E2H2	TF42X	F-500
	E2F2	TF48X	
	E2C2	TF60X	
	E2E2	TF80X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X743 PCF=E; Continuous XMIT PDF 1 LCD=C Not EP BSC EBCDIC

ROUTINE DESCRIPTION

This routine tests PCF state X'E' in the BSC transmit mode. State transitions, continuous send of PDF 1, and timeout are tested. Transmit only - Diag 0=1. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X01 E3F2	TE20X	F-220
	E3R2	TE26X	F-550
	E2J2	TF50X	
	E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X02 E2B2	TF81X	F-580
	E2E2	TF80X	F-600
	E2R2	TF32X	F-570
	E2C2	TF60X	
	E2K2	TF44X	
	E2J2	TF50X	
	E2H2	TF42X	

The PCF/EPCF should be 9/1 with sequence bit 13.0 off. Refer to BSC transmit state transition 1, 2 and 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X743	0X03	E2B2	TF81X	F-580
		E2J2	TF50X	F-600
		E2E2	TF80X	F-570
		E3D2	TE34X	
		E2K2	TF44X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be E/0 with sequence bit 13.0 on. The program forced PCF/EPCF state E/0 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 92.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X04	E2C2	TF60X	F-210
		E2B2	TF81X	
		E2V2	TF41X	

The BSC timeout counter was not set for a 1 sec timeout. ICW bits 4.2, 4.3, and 4.7 on with 4.4 and 5.0 off give 1 sec timeout. Bits in error are on in register X'15' bits 0.2-0.4, 0.7 and 1.0. Refer to BSC Transmit state transition 92.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X05	E2B2	TF81X	F-480
		E2C2	TF60X	F-500
		E2H2	TF42X	
		E3J2	TE22X	
		E2J2	TF50X	

The receive line SDF should contain X'010F'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X06	E2B2	TF81X	F-410
		E2J2	TF50X	F-420
		E2H2	TF42X	

Tag time was not detected. ICW bit 3.2 (tag bit) either did not turn on after going off (tag bit set at tag time), or it never went off (SDF shifting). Refer to BSC transmit state transition 93.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X07	E2B2	TF81X	F-480
		E2C2	TF60X	F-500
		E2H2	TF42X	
		E3J2	TE22X	

The receive line SDF should contain X'01F6'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X08	E3J2	TE22X	F-240
		E3D2	TE34X	F-380
		E2N2	TF22X	F-390
		E2F2	TF48X	
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to BSC Transmit state transition 93.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X09 E3J2	TE22X	F-240
	E3D2	TE34X	F-380
	E2F2	TF48X	F-390
	E2C2	TF60X	
	E2N2	TF22X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to BSC Transmit state transition 93.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X0A E2B2	TF81X	F-480
	E2C2	TF60X	F-500
	E2H2	TF42X	
	E3J2	TE22X	

The receive line SDF should contain X'01F6'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X0C E3J2	TE22X	F-240
	E3D2	TE34X	F-380
	E2F2	TF48X	F-390
	E2C2	TF60X	
	E2N2	TF22X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to BSC Transmit state transition 94.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X0D E2B2	TF81X	F-480
	E2C2	TF60X	F-500
	E2H2	TF42X	
	E3J2	TE22X	

The receive line SDF should contain X'01F6'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X0E E2B2	TF81X	F-210
	E2J2	TF50X	
	E2C2	TF60X	
	E2E2	TF80X	

The BSC timeout counter was not set for 1 sec timeout. ICW bits 4.2, 4.3 and 4.7 on with 4.4 and 5.0 off give 1 sec timeout. Bits in error are on in reg X'15' bits 0. Refer to BSC Transmit state transition 94.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X743	0X0F E2E2	TF80X	F-550
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Refer to BSC transmit state 94. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

X744 Cycle Steal from and to main Storage on even Byte Boundary --- Even Byte Count
LCD=C Not EP EBCDIC BSC

ROUTINE DESCRIPTION

This routine verifies that cycle steal hardware moves data correctly from main storage into ICW PDF array. After cycle stealing data from storage, the routine moves data from the ICW PDF array into main storage (8 bytes). Cycle steal data X'5566778899AABBCC'. Diag 0=1 for both lines.

NOTE **** If High Speed Scanner Feature (230.4KBPS) is installed, 16 bytes of data are transferred from the PDF array. The cycle steal data pattern is X'5566778899AABBCCDDEEFF1021324354'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Register X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - register X'14' not equal to register X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Register X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - register X'14' not equal to register X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X03	E2C2	TF60X	F-580
		E2B2	TF81X	F-600
		E3K2	TE24X	
		E2R2	TF32X	
		E2J2	TF50X	
		E3M2	TE32X	
		E3L2	TE40X	
		E3D2	TE34X	
		E3H2	TE54X	
		E3S2	TE50X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 9/7 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X04	E3S2	TE50X	F-360
		E3K2	TE24X	F-560

E3E2	TE70X	
E3H2	TE54X	
E3J2	TE22X	
E3D2	TE34X	
E3L2	TE40X	
E3Q2	TE52X	
E2B2	TF81X	
E2N2	TF22X	
E2E2	TF80X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

No L2 occurred. A L2 should have occurred following a cycle steal transfer of 8 bytes of data (or 16 bytes for Hi-Speed Scanner) from main storage to an ICW PDF array; "Cycle Steal Fetch". The L2 should occur because Byte Count = 0 and Cycle Steal valid (input 48 bit 6.5) is reset. Register X'11' is line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X05	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. The interrupt was from the wrong line. Register X'14' contains the address of the line that interrupted. Register X'11' contains the address of the line the interrupt was expected from.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X06	E3K2	TE24X	F-360
		E3E2	TE70X	
		E3J2	TE22X	
		E3D2	TE34X	
		E3L2	TE40X	
		E3Q2	TE52X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The data fetched into ICW PDF array on a cycle steal function, does not equal expected data. Register X'14' contains the byte number in error. Register X'4C' contains actual byte in error. Register X'15' contains bits in error. Expected data = 5566778899AABBCC.

NOTE **** If High Speed Scanner Feature (230.4KBPS) is installed, the expected data pattern is 5566778899AABBCCDDEEFF1021324354.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X07	E2B2	TF81X	F-580
		E2R2	TF32X	F-590
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. The program set the PCF/EPCF to 7/4.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X0A	E2D2	TF62X	F-360
		E2C2	TF60X	F-560
		E3K2	TE24X	
		E3E2	TE70X	
		E3H2	TE54X	
		E3J2	TE22X	
		E3C2	TE71X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

No L2 interrupt occurred. A L2 interrupt should have occurred within 280/MSEC, following a Cycle Steal store function of 8 test Bytes of Data (or 16 bytes for Hi-Speed Scanner). The L2 interrupt should occur because the Byte Count = 0 and Cycle Steal valid (input 48 Byte 0 Bit 5) are reset.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X0B	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. The interrupt was from the wrong line. Register X'14' contains the address of the line that interrupted. Register X'11' contains the address of the line the interrupt was expected from.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X744	0X0C	E3K2	TE24X	F-450
		E3J2	TE22X	
		E3D2	TE34X	
		E2D2	TF62X	
		E2H2	TF42X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The data cycle stolen into the main storage on a cycle steal store function, does not equal the expected data. Register X'14' contains the address + 1 of the byte expected. Register X'16' contains address +1 of byte in error. Register X'15' contains bits in error. Expected data = 5566778899AABBCC.

NOTE **** If High Speed Scanner Feature (230.4KBPS) is installed, the expected data pattern is 5566778899AABBCCDDEEFF1021324354.

X745 Cycle Steal from and to main Storage on Odd Byte Boundary -- Odd Byte Count
LCD=C EBCDIC Not EP BSC

ROUTINE DESCRIPTION

This routine verifies that cycle steal hardware moves data correctly from main storage into ICW PDF array. After cycle stealing data from storage, the routine moves data from ICW PDF array into main storage (7 bytes), and (15 bytes for High Speed Scanner). Cycle steal test data --- X'55' - X'5B' (5C - 63 for High Speed Scanner) Diag 0=1 for both lines.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X01	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Register X'15' Description

0001	No set mode L2 occurred.
0002	Interrupt from wrong line - register X'14' not equal to register X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Register X'15' Description

0001	No set mode L2 occurred.
0002	Interrupt from wrong line - register X'14' not equal to register X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X03	E2C2	TF60X	F-580
		E2B2	TF81X	F-600
		E2J2	TF50X	
		E2R2	TF32X	

The PCF/EPCF should be 9/0 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X04	B3H2	TE54X	F-550
		E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

No L2 interrupt occurred. A L2 interrupt should have occurred following a cycle steal transfer of 7 bytes of data from main storage to an ICW PDF array. (fetch). The interrupt should have occurred from byte count = 0 and cycle steal valid reset (input 44, Byte 0, Bit 5)

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X05	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. The interrupt was from the wrong line. Register X'14' contains the address of the line that interrupted. Register X'11' contains the address of the line the interrupt was expected from.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X06	E3J2	TE22X	F-360
		E3K2	TE24X	
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The Data Fetched into the ICW PDF Array on a Cycle Steal Fetch function, does not equal the expected data. Register X'14' contains the Byte number in error. Register X'4C' contains actual byte in Error. Register X'15' contains Bits in Error. Expected Data = 55, 56,57, 58, 59, 5A, 5B (also 5C - 63 for Hi-Speed Scanner).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X07	E2K2	TF44X	F-580
		E2R2	TF32X	F-590
		E2B2	TF81X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 undefined. The program set the PCF/EPCF to 7/4.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X745	0X0A	E3J2	TE22X	F-550
		E3K2	TE24X	F-560
		E2E2	TF80X	
		E2F2	TF48X	
		E3L2	TE40X	

No L2 interrupt occurred. A L2 interrupt should have occurred within 280/MSEC following a Cycle Steal store function of 7 test data bytes. The L2 interrupt should have occurred from Byte Count = 0 and Cycle Steal valid reset (input 44, Byte 0, Bit 5).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X0B	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. The interrupt was from the wrong line. Register X'14' contains the address of the line that interrupted. Register X'11' contains the address of the line the interrupt was expected from.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X745	0X0C	E3K2	TE24X	F-450
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data cycle stolen into the main storage on a cycle steal store function does not equal the expected data. Register X'14' contains Byte Number in Error. Register X'16' contains Addr +1 of Byte in error. Register X'15' contains Bits in Error. Expected Data = 55, 56,57, 58, 59, 5A, 5B (also 5C - 63 for Hi-Speed Scanner).

X746 SDLC Transmit Test # 1 LCD=1 EP

ROUTINE DESCRIPTION

This routine test state transitions and associated functions for SDF shifting, PAD insertion, Flag insertion, PDF to SDF shifting, BCC insertions, and line turn around. The line is functioning in SDLC Non-NRZI mode with the PAD before Line Turn (ICW bit 15.6) bit on, RTS Turn control (ICW bit 13.2) bit off, and Line Turn after transmission (ICW bit 15.7) bit on. Diag 0=1 for the transmit line. Receive not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X01	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X02	E2C2	TF60X	F-580
		E2B2	TF81X	F-600
		E2J2	TF50X	
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 9/0 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X03		
	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X04		
	E3F2	TE20X	F-440
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The SDF is not shifting properly. The SDF is monitored for a X'0043' (PAD shifted one bit) for approximately 1 msec. Register X'15', (bits 0.6-1.7) contains the SDF value at time out.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X05		
	E2B2	TF81X	F-580
	E2J2	TF50X	F-600
	E2C2	TF60X	
	E2F2	TF48X	
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X06		
	E2B2	TF81X	F-440
	E2Q2	TF34X	
	E2F2	TF48X	
	E2E2	TF80X	
	E2K2	TF44X	

The Transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X07		
	E3H2	TE54X	F-580
	E2B2	TF81X	F-590
	E2J2	TF50X	
	E2K2	TF44X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X08		
	E3R2	TE26X	F-220
	E3S2	TE50X	
	E2D2	TF62X	
	E2C2	TF60X	
	E2E2	TF80X	
	E2H2	TF42X	
	E2V2	TF41X	

The display register was checked for XMIT and RTS to be on in Data Out 1-7, and NEW SYNC and SEND DATA to be off.

Register X'15' contains bits in error (0.3=XMIT, 0.4=NEW SYNC, 0.5=RTS and 0.6=SEND DATA). Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X09	E2B2	TF81X	F-440
		E2F2	TF48X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The Transmit line SDF should contain X'0101'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X0A	E2P2	TF82X	F-240
		B3Q2	TE52X	
		E3R2	TE26X	
		E2H2	TF42X	

ICW bit 16.0 should be off. ICW bit 16.0 should only be set if the PCF is X'B'; this routine runs with PCF equal to X'9'. Refer to SDLC Transmit state transition 15.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X0B	E2B2	TF81X	F-440
		E2L2	TF46X	F-230
		E2M2	TF31X	
		E2P2	TF82X	
		E2U2	TF30X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The BCC (input X'4A') should have been reset and accumulation made on the first character. The expected value of the BCC was X'B1F1'. Reset and/or BCC accumulation could be at fault. Register X'15' contains the bits in error. Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X11	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X12	E2B2	TF81X	F-580
		E2E2	TF80X	F-590
		E2R2	TF32X	F-570
		E2F2	TF48X	
		E3D2	TE34X	
		E2K2	TF44X	
		E2J2	TF50X	
		E2Q2	TF34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to SDLC Transmit state transition 11.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X13	E2L2	TF46X	F-440
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E2P2	TF82X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The Transmit line SDF should contain X'0104'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X14	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 off. Refer to SDLC Transmit state transition 16.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X15	E2L2	TF46X	F-440
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E2P2	TF82X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The transmit line SDF should contain X'0124'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X16	E2Q2	TF34X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	
		E2P2	TF82X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X746	0X17	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The Transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X18	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 off. Refer to SDLC Transmit state transition 9.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X19	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2Q2	TF34X	
		E2P2	TF82X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X20	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2C2	TF60X	
		E2H2	TF42X	
		E2E2	TF80X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 17.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X21	E2D2	TF62X	F-220
		E2C2	TF60X	
		E2E2	TF80X	
		E2H2	TF42X	

The display register was checked for RTS off in Data Out 1-7.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X22	E2E2	TF80X	F-550
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Refer to SDLC transmit state 17. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X746	0X23	E2N2	TF22X	F-160
		E2E2	TF80X	F-210
		E2F2	TF48X	F-240
		E3D2	TE34X	
		E2Q2	TF34X	
		E2P2	TF82X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The status posted in the transmit line ICW was expected to be X'0403'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X24	E2V2	TF41X	F-210
		E2C2	TF60X	
		E2P2	TF82X	

ICW bit 4.5 should have been set on. Refer to SDLC transmit state 17.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X25	E2N2	TF22X	F-240
		E2E2	TF80X	F-570

Input X'4E' was used to check the message count (ICW bits 13.6-13.7) for reset. Register X'15' bits 1.5 and 1.6 indicate the bits in error. Refer to SDLC Transmit state transition 17.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X746	0X26	E2C2	TF60X	F-210
		E2N2	TF22X	
		E2B2	TF81X	
		E3L2	TE40X	
		E2F2	TF48X	

Input X'47' was used to check the ones counter (ICW bits 4.2-4.4, 4.7, and 5.0) for reset. Register X'15' bits 0.2-0.4, 0.7, and 1.0 contain the bits in error. Refer to SDLC Transmit state transition 17.

X747 SDLC Transmit Test # 2 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests state transitions and associated functions with the line in SDLC NRZI mode, and with the PAD Before Line Turn (ICW bit 15.6) bit off, Line Turn after transmit (ICW bit 15.7) bit on, RTS Turn Control (ICW bit 13.2) bit on, and NEW SYN (PCF = A and B). Diag 0=1 for Transmit line. Receive not used. Cycle steal is used.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X01	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode I.2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X02	E2C2	TF60X	F-580
		E2B2	TF81X	F-600
		E3K2	TE24X	
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be B/0 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 24.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X03	E2F2	TF48X	F-440
		E3F2	TE20X	
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0100'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X04	E2E2	TF80X	F-580
		E2B2	TF81X	F-600
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be B/1 with sequence bit 13.0 on. Refer to SDLC Transmit state transition 6.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X05	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0100'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X06	E2E2	TF80X	F-580
		E2B2	TF81X	F-600
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be B/1 with sequence bit 13.0 off. Refer to SDLC Transmit state transition 7.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X07 E2E2	TF80X	F-440
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0100'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X08 E2B2	TF81X	F-600
	E2J2	TF50X	F-580
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be B/2 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 8.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X09 E2E2	TF80X	F-440
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X0A E2B2	TF81X	F-440
	E2J2	TF50X	
	E2E2	TF80X	

Tag time not detected while in state PCF=B/EPCF=2. The PDF array was empty and a Flag was to be inserted at tag time. Refer to SDLC Transmit state transition 10.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X0B E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X0C E3H2	TE54X	F-580
	E2B2	TF81X	F-590
	E2J2	TF50X	
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be B/4 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747 0X0D	E2P2	TF82X	F-240
	E3Q2	TE52X	
	E3R2	TE26X	
	E2H2	TF42X	

New Syn (ICW bit 16.0) was not set. Reference SDLC Transmit state transition 15.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747 0X0E	E2D2	TF62X	F-220
	E2C2	TF60X	
	E2H2	TF42X	
	E2P2	TF82X	

Error detected in Data Out 1-7 (Display Register). XMIT, NEW SYN, RTS and SEND DATA were expected to be on. Register X'11' contains the address of the line under test. Register X'15' (bits 0.3-0.6) contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747 0X0F	E2B2	TF81X	F-580
	E2J2	TF50X	F-590
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be B/6 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 11.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747 0X10	E2P2	TF82X	F-240
	E2H2	TF42X	
	E3R2	TE26X	

ICW bit 16.0 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747 0X11	E2J2	TF50X	F-220
	E2P2	TF82X	
	E2E2	TF80X	
	E2R2	TF32X	

The Display Register was checked for XMIT and RTS to be on and New Sync and Send Data to be off. (Date Out 1-7) Register X'15' contains the bits in error (0.3=XMIT, 0.4=New Sync, 0.5=RTS and 0.6=Send Data). Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747 0X12	E2B2	TF81X	F-580
	E2J2	TF50X	F-590
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be B/5 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747 0X13	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2J2	TF50X	F-570

E2R2	TF32X	
E2K2	TF44X	

The PCF/EPCF should be B/7 with sequence bit 13.0 off. Refer to SDLC Transmit state transition 4.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X14	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E2F2	TF48X	
		E2Q2	TF34X	

The transmit line SDF should contain X'0007'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X15	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 20.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X16	E2C2	TF60X	F-220
		E2D2	TF62X	

Error detected in Data Out 1-7, XMIT, RTS were expected to be on and NEW SYN off. Register X'15' contains the bits in error (0.3=XMIT, 0.4=NEW SYN, 0.5=RTS). Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X747	0X17	E2E2	TF80X	F-550
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Refer to SDLC transmit state 20. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

X748 SDLC Transmit Test # 3 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests state transitions and functions with the line in 'do-nothing' mode (diagnostic 1 - ICW bit 5.6 on). Data chain on is tested to cause a level 2 service interrupt, and RTS Turn Control (ICW bit 13.2) is on. Diag 0 and Diag 1=1 for transmit line. Receive not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X01	E3F2	TE30X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X02 E2B2	TF81X	F-580
	E2J2	TF50X	F-590
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 9/C with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X03 E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X04 E2C2	TF60X	F-440
	E3F2	TE20X	
	E3J2	TE22X	
	E2B2	TF81X	
	E2H2	TF42X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X06 E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0101'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X07 E3E2	TE70X	F-440
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X08 E3L2	TE40X	F-440
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0104'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X09	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0124'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X0A	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X0B	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0100'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X0C	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X0D	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X0E	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X0F	E2B2	TF81X	F-160
		E2N2	TF22X	F-210
		E2C2	TF60X	F-240

E2E2	TF80X
E2R2	TF32X
E2F2	TF48X
E2Q2	TF34X

The status posted in the transmit line ICW was expected to be X'2000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748 0X10	E2B2	TF81X	F-580
	E2J2	TF50X	F-600
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 23 and 17.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748 0X11	E2N2	TF22X	F-160
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748 0X12	E2E2	TF80X	F-550
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Refer to SDLC transmit state 17. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748 0X13	E2N2	TF22X	F-160
	E2B2	TF81X	F-210

	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X748	0X14 E2V2	TF41X	F-210
	E2C2	TF60X	
	E2P2	TF82X	

Last-Line-State (ICW bit 4.5) was not set on. Refer to SDLC Transmit state transition 17.

X749 SDIC Transmit Test # 4 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests state transitions and functions leaving Data Chain (ICW bit 6.6) on while the PDF goes empty, and with No Line Turn (ICW bit 15.7) off, and XMIT Idle After Transmission (ICW bit 15.5) off. Diag 0=1 for transmit line. Receive not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749	0X01 E3F2	TE20X	F-220
	E3R2	TE26X	F-520
	E2J2	TF50X	
	E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749	0X02 E2F2	TF48X	F-580
	E2C2	TF60X	F-600
	E3H2	TE54X	
	E2B2	TF81X	
	E2R2	TF32X	
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 21, 1, 15 and 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X749	0X03	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749	0X04	E2B2	TF51X	F-600
		E2N2	TF22X	F-580
		E2R2	TF32X	
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749	0X05	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749	0X06	E2E2	TF80X	F-550
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Refer to SDLC transmit state 2. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749	0X07	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Refer to SDLC Transmit state transition 15, 11, 16 and 12.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749	0X08	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X749 0X09 E2E2 TP80X F-550
E2F2 TP48X F-560
E3L2 TE40X

A L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749 0X10	E2E2	TP80X	F-160
	E2C2	TP60X	F-210
	E2N2	TP22X	F-240
	E2B2	TP81X	
	E2E2	TP80X	
	E2F2	TP48X	
	E2Q2	TP34X	

The status posted in the transmit line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.		
X749 0X11	E2B2	TP81X	F-440 E2J2	TP50X E2H2	TP42X

Tag time was not detected. ICW bit 3.2 (Tag bit) either did not turn on after going off (tag bit set at tag time), or it never went off (SDF shifting). Refer to SDLC Transmit state transition 13.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X749 0X12	E2B2	TP81X	F-440
	E2C2	TP60X	
	E2H2	TP42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

X74A SDLC Transmit Test # 5 LCD=1 EP

ROUTINE DESCRIPTION

This routine test Transmit Flag After Transmission (ICW bit 15.5) on with No Line Turn After Transmission (ICW bit 15.7) off. Diag 0=1 for transmit line. Receive not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74A 0X01	E3F2	TE20X	F-220
	E3R2	TE26X	F-550
	E2J2	TP50X	
	E2D2	TP62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74A	0X02	E2F2	TF48X	F-580
		E2E2	TF80X	F-590
		E2C2	TF60X	F-570
		E2B2	TF81X	
		E3K2	TE24X	
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 off. Refer to SDLC Transmit state transition 21, 1, 15, 18, 11 and 16.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74A	0X03	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74A	0X04	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74A	0X05	E2E2	TF80X	F-550
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Refer to SDLC transmit state 19. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74A	0X06	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0404'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2

0.3	Data Check	14.3
0.4	SDLC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X74B SDLC transmit test 6 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests state transitions and functions for the transmit two flags (ICW bit 15.4 and bit 15.5 on). State transition flow is 21, 29, 31, 15, 3, 32, level 2, 30, 31, 15, 11, 16, 33. Diag 0=1 for transmit line. Receive not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X02	E2C2	TF60X	F-580
	E3F2	TE20X	F-600
	E2B2	TF81X	
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/0 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X03	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X04	E2E2	TF80X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	F-570
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 on. Refer to SDIC Transmit state transition 29.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X05	E2E2	TF80X	F-440
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X06	E2E2	TF80X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	F-570
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to SDLC Transmit state transition 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X07	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15'. (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X08	E3H2	TE54X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to SDLC Transmit state transition 15,3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X09	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B 0X0A	E2E2	TF80X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	F-570
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 on. Refer to SDIC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X0B	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X0C	E2E2	TF80X	F-550
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Refer to SDLC transmit state 19. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X0D	E2E2	TF80X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	F-570
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/1, 13.0 off prior to this test. Refer to SDLC Transmit state transition 30 and 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X0E	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	F-570
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 off. Refer to SDLC Transmit state transition 15, 11, 16.

Register X'15' contains the incorrect PCF (bits 0|0-0|3), EPCF (bits 0|4-0|7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X0F	E2E2	TF80X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	F-570
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 on. Refer to SDLC Transmit state transition 33.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X10	E2B2	TF81X	F-440
		E2C2	TF60X	

E2H2	TF42X	
E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X11		
	E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X12		
	E2N2	TF22X	F-160
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'040C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits	
0.0	Abort Detect	0.0	
0.1	Format Exception	14.1	
0.2	Char Over/Under run		0.2
0.3	Data Check		14.3
0.4	BSC bad PAD flag	14.4	
0.5	EOM	0.5	
0.6	Leading DLE Error	14.6	
0.7	Length Check	14.7	
1.0-1.7	ICW byte 15	15.0-7	

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X13		
	E2B2	TF81X	F-440
	E2J2	TF22X	
	E2E2	TF80X	

Tag time was not detected. ICW bit 3.2 (Tag bit) either did not turn on after going off (tag bit set at tag time), or it never went off (SDF shifting). Refer to SDLC Transmit state transition 13.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74B	0X14		
	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'017E'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

X74C SDLC Receive Test # 1 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests state transitions and associated functions involved in receiving valid non-NRZI non-information frames with good CRC.

Bit shifting and SDF to PDF shift are checked. Also, a non-information frame with bad CRC is received and the level 2 interrupt and status bits are checked. Diag 0=1 for both lines. Diag 1=1 for transmit line. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X02	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X03	E2C2	TF60X	F-580
		E3H2	TE54X	F-600
		E2R2	TF32X	
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X04	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/2 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X05	E2N2	TF22X	F-570
		E2B2	TF81X	
		E3L2	TE40X	
		E2F2	TF48X	

ICW bit 13.1 was not reset. Refer to SDLC Receive state transition 22.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74C	0X06	E2B2	TF81X	F-520
		E2H2	TF42X	
		E2P2	TF82X	

Receive data byte in PDF array not correct. The expected data byte was X'01'. Input X'4C' will display actual byte in array. Register X'15' (byte 1) contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X07	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC (input X'4A') should have been reset and accumulation made on the first character. The expected value of the BCC is X'E1F1'. Reset and/or accumulation could be at fault.

Refer to SDLC Receive state transition 22.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X08	E2C2	TF60X	F-580
		E3E2	TE70X	F-600
		E2E2	TF80X	F-570
		E2B2	TF81X	
		E2J2	TF50X	
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 off. Refer to SDLC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X09	E2N2	TF22X	F-570
		E2B2	TF81X	
		E3L2	TE40X	
		E2P2	TF48X	

ICW bit 13.1 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X10	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2P2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74C	0X11	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 on. Refer to SDLC Receive state transition 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X12	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X13	E2P2	TF82X	P-580
		E2E2	TF80X	F-590
		E2B2	TF81X	
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 51.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X14	E2C2	TF60X	F-240
		E2E2	TF80X	F-570
		E2N2	TF22X	

This stop indicates an error in at least one of the following bits in input X'4E': either ICW bits 12.4-12.7 (PDF1 pointer) is not X'2'; ICW bit 13.1 (sequence bit 1) is on; or ICW bit 13.3 (sequence bit 2) is off. Register X'15' contains the bits in error.

Refer to SDLC Recieve state transition 23, 44, 45, and 51.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X15	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 51.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X16	E2B2	TF81X	F-590
		E2J2	TF50X	F-580

		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 52.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X17	E3C2	TE71X	F-570
		E2J2	TF50X	
		E2E2	TF80X	

This stop indictes an error in at least one of the following bits in an input X'4E': The expected values are: ICW bit 13.1 (sequence bit 1) on; ICW bit 13.3 (sequence bit 2) off; and ICW bits 13.6-13.7 (message count) '01'. Register X'15' contains the bits in error.

Refer to SDLC Receive state transition 52.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X18	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/2 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 48.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X19	E2N2	TF22X	F-570
		E2B2	TF81X	
		E3L2	TE40X	
		E2P2	TF48X	

ICW bit 13.1 was not reset. Refer to SDLC Receive state transition 48.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X1A	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC (input X'4A') should have been reset and accumulation made on the first non flag character after the flag. The expected value of the BCC was X'E1F1'. Refer to SDLC Receive state transition 48.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X20	E3D2	TE34X	F-560
		E3L2	TE40X	
		E2N2	TF22X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 52.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74C	0X21	E2N2	TF22X	F-230
		E3K2	TE24X	
		E2P2	TF82X	

ICW bit 6.5 (CSV) was not reset.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X22	E2B2	TF81X	F-160
		E2N2	TF22X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	14.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X23	E2B2	TF81X	F-590
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 23, 44, 45, 51 and 54.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X24	E2B2	TF81X	F-570
		E2N2	TF22X	F-240
		E2E2	TF80X	
		E2F2	TF48X	

This stop indicates that an error in at least one of the following bits in input X'4E' is in error. The expected values are: ICW bit 13.1 (sequence bit 1) on, ICW bit 13.3 (sequence bit 2) off, and ICW bit 13.6-13.7 (message count) equal to '01'. Register X'15' contains the bits in error.

Refer to SDLC Receive state transition 23, 44, 45, 51, and 54.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X25	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 37.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74C	0X26	E2N2	TF22X	F-230
		E3K2	TE24X	
		E2P2	TF82X	

ICW bit 6.5 (CSV) was not reset.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X27	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 54.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X28	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X29	E2N2	TF22X	F-380
		E2B2	TF81X	F-390
		E3L2	TE40X	
		E2F2	TF48X	
		E3D2	TE34X	
		E2C2	TF60X	
		E2P2	TF82X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PDF array pointers (ICW byte 12) were not correct. The expected value of byte 12 was X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74C	0X30	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

L2 pending bit is incorrectly set in the ICW. ICW bit 5.1 should be off.

X74D SDLC Receive Test # 2 LCD=1 EP

ROUTINE DESCRIPTION

This routine checks the receive 'do-nothing' (inhibit line control - Diagnostic bit 1 on) mode. Flag, Abort, and Idle are wrapped and checked in the receive buffer. State transition flow is: 12, 13, 14, 14, 14. Diag 0 and Diag 1=1 for both lines. Cycle steal is used.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74D	0X01	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74D	0X02	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74D	0X03	E2C2	TF60X	F-590
		E3H2	TE54X	F-580
		E2B2	TF81X	
		E2J2	TF50X	
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 7/C with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 12. The PCF/EPCF was originally set to 4/0.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74D	0X04	E2B2	TF81X	F-590
		E2J2	TF50X	F-580
		E3Q2	TE52X	
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 7/C with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 13. The program forced the PCF/EPCF to 5/0 prior to this transition.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74D	0X05	E2N2	TF22X	F-570
		E2B2	TF81X	
		E3L2	TE40X	
		E2F2	TF48X	

Input X'4E' was used to check the message count (ICW bits 13.6 and 13.7). The expected value was 13.6 off and 13.7 on. Register X'15' contains the bits in error. Refer to SDLC Receive state transition 13.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74D	0X06	E3K2	TE24X	F-550
		E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74D	0X07	E3K2	TE24X	F-520
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X74E SDLC Receive Test # 3 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests the valid control frame detection circuits. Invalid control frames (short frames) are wrapped to the receive line and state transitions and PDP array addresses are verified. Frames are prematurely terminated with Flags and Aborts. Both normal and two control character modes are checked. Diag 0=1 for both lines. Diag 1=1 for transmit line. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X01	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X02	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74E	0X03	E2C2	TF60X	F-600
		E3H2	TE54X	F-580
		E2B2	TF81X	
		E2J2	TF50X	
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X04	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Flag characters should not change the PDF array pointers.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X05	E2C2	TF60X	F-580
		E2J2	TF50X	F-600
		E2B2	TF81X	
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 29A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X06	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/2 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X07	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'01'. Refer to SDLC Receive state transition 22. The received character should have incremented the PDF pointer by one.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X09	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X0A	E2F2	TF48X	F-380
		E3D2	TE34X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 15.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X0D	E2E2	TF80X	F-580
		E2B2	TF81X	F-600
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 off. Refer to SDLC Receive state transition 22 and 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X0E	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X0F	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 25.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X10	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 23, 44 and 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X11	E2E2	TF80X	F-380
	E3D2	TE34X	F-390
	E2F2	TF48X	
	E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 26.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X12	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2J2	TF50X	F-570
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 22, 15, 22, 23, 44 and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X13	E3J2	TE22X	F-580
	E2B2	TF81X	F-600
	E3K2	TE24X	
	E2R2	TF32X	
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X14	E2B2	TF81X	F-600
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X15	E2B2	TF81X	F-600
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/2 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74E	0X16	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 22 and 4.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X17	E2C2	TF60X	F-380
		E3D2	TE34X	F-390
		E2F2	TF48X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 27, 2, 1, 22 and 4.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X18	E2E2	TF80X	F-580
		E2B2	TF81X	F-600
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 off. Refer to SDLC Receive state transition 1, 22 and 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X19	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 6.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X1A	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 6.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X1B	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 on. Refer to SDLC Receive state transition 1, 22, 23 and 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X1C	E2E2	TF80X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 7.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X1D	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 7.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X1E	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 22, 23, 44 and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X1F	E2B2	TF81X	F-600
		E2R2	TF32X	F-580
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 8.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X20	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 8.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74E	0X21	E2B2	TF81X	F-600
		E2J2	TF50X	F-580
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X22	E2E2	TF80X	F-580
	E2B2	TF81X	F-600
	E2J2	TF50X	F-570
	E2N2	TF22X	
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 on. Refer to SDLC Receive state transition 22 and 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X23	E2B2	TF81X	F-600
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 24.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X31	E3D2	TE34X	F-380
	E2F2	TF48X	F-390
	E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 24.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X32	E2B2	TF81X	F-600
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 22, 30 and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X33	E3D2	TE34X	F-380
	E2F2	TF48X	F-390
	E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 5.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X34	E2E2	TF80X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	F-570
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 off. Refer to SDLC Receive state transition 1, 22, 30 and 43.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X35	E3J2	TE22X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 44 and 7.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X36	E3D2	TE34X	F-380
	E2F2	TF48X	F-390
	E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 7.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X37	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	F-570
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 on. Refer to SDLC Receive state transition 1, 22, 30, 43 and 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E 0X38	E2B2	TF81X	F-680
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X39	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 26.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X3A	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 22, 30, 43, 44, 45 and 8.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X3B	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 8.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X3C	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 1, 22, 30, 43, 44, 45 and 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X3D	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers (ICW byte 12 - input X'4E') are incorrect. The expected value of byte 12 was X'00'. Refer to SDLC Receive state transition 27.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74E	0X3E	E2N2	TF22X	F-560
		E2B2	TF81X	

The not-L2-Bid bit (ICW 0.4) should be on. There should not be an outstanding L2 at this time.

X74F SDLC Receive Test # 4 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests SDLC functions checking for valid information frames. Frames are prematurely terminated via flag, abort, and idle. Diag 0=1 for both lines. Diag 1=1 for transmit line. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X02	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X03	E2E2	TF80X	F-580
	E2C2	TF60X	F-600
	E3H2	TE54X	F-570
	E2J2	TF50X	
	E2B2	TF81X	
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 off. Refer to SDLC Receive state transition 3, 22, and 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X04	E2N2	TF22X	F-380
	E2B2	TF81X	F-390
	E3L2	TE40X	
	E2F2	TF48X	

Either the PDF array pointers (ICW byte 12) are not correct (the expected value is X'02') or Sequence bit 1 (ICW 13.1) is not on. Refer to state transition 23. Register X'15' contains the bits in error. Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74F	0X05	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X06	E2B2	TF81X	F-520
		E2E2	TF80X	
		E2F2	TF48X	
		E2N2	TF22X	
		E2S2	TF50X	

The last entry in the PDF is not equal to X'40B' (control, EOM, leading graphics and L2 pending).

Register X'15' (bits 0.5-1.7) contains the bit/s in error.

Register X'11' contains the address of the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X07	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 32.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X08	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0500'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X09	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	F-570
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 on. Refer to SDLC Receive state transition 22, 23 and 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X10	E2N2	TF22X	F-380
		E2B2	TF81X	F-390
		E3L2	TE40X	F-570
		E2F2	TF48X	

Either the PDF array pointers (ICW byte 12) are not correct (the expected value is X'56') or Sequence bit 1 (ICW bit 13.1) is not on, or the message count (ICW bits 13.6 and 13.7) are not as expected. (The expected message count is 13.6 off and 13.7 on). Refer to SDLC Receive state transition 23. Register X'15' contains the bits in error. Register X'11' is the line under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X11	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 33.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X12	E2B2	TF81X	F-520
		E2E2	TF80X	
		E2F2	TF48X	
		E2N2	TF22X	
		E2S2	TF50X	

The last entry in the PDF is not equal to X'40B' (control, EOM, leading graphics and L2 pending).

Register X'15' (bits 0.5-1.7) contains the bit/s in error.

Register X'11' contains the address of the line under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X13	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 33.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X14	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0500'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6

	0.7	Length Check	14.7	
	1.0-1.7	ICW byte 15	15.0-7	

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X15	E2C2	TF60X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 22, 23 and 17.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X16	E2B2	TF81X	F-590
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X17	E2B2	TF81X	F-520
		E2E2	TF80X	
		E2F2	TF48X	
		E2N2	TF22X	
		E2S2	TF50X	

The last entry in the PDF is not equal to X'509' (control, abort detect, EOM and L2 pending).

Register X'15' (bits 0.5-1.7) contains the bit/s in error.

Register X'11' contains the address of the line under test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X18	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 37, 22, 23 and 17.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X19	E3L2	TE40X	F-380
		E2B2	TF81X	F-390
		E2N2	TF22X	F-570
		E2F2	TF48X	

Either the PDF array pointers (ICW byte 12 - input X'4E') are incorrect, (the expected value of byte 12 was X'AC') or the message count (ICW bits 13.6 and 13.7) are not as expected. (The expected message count is 13.6 off and 13.7 on) or sequence 1 (ICW 13.1) is not on. Register X'15' contains the bits in error. Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X20	E2C2	TF60X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 9.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X21	E3D2	TE34X	F-380
	E2F2	TF48X	F-390
	E2C2	TF60X	F-570

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

Either the PDF array pointers (ICW byte 12 - input X'4E') are incorrect, (the expected value of byte 12 was X'AD') or the message count (ICW bits 13.6 and 13.7) are not as expected. (The expected message count is 13.6 off and 13.7 on) or sequence 1 (ICW 13.1) is not on. Register X'15' contains the bits in error. Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X22	E2B2	TF81X	F-520
	E2E2	TF80X	
	E2F2	TF48X	
	E2N2	TF22X	
	E2S2	TF50X	

The last entry in the PDF is not equal to X'589' (control, abort detect, idle detect, EOM and L2 pending).

Register X'15' (bits 0.5-1.7) contains the bit/s in error.

Register X'11' contains the address of the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X23	E2E2	TF80X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	F-570
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 on. Refer to SDLC Receive state transition 1, 22 and 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F 0X24	E2B2	TF81X	F-600
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X74F	0X25	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	F-570

NOTE **** If the High Speed Scanner Feature (230KB) is installed; E3N2 (TE35X) is also a possible failing card.

Either the PDF array pointers (ICW byte 12) are incorrect (the expected value is X'A0') or the message count (ICW byte 13 bits 6 and 7) are incorrect (the expected value is 13.6 on and 13.7 off) or sequence 1 (ICW byte 13 bit 1) is not on. Register X'15' contains the bits in error. Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X26	E2N2	TF22X	F-520
		E2B2	TF81X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2S2	TF50X	

The last entry in the PDF is not equal to X'40B' (control, EOM, leading graphics and L2 pending).

Register X'15' (bits 0.5-1.7) contains the bit/s in error.

Register X'11' contains the address of the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X27	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/2 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X28	E2N2	TF22X	F-380
		E2B2	TF81X	F-390
		E3L2	TE40X	F-570
		E2F2	TF48X	

Either the PDF array pointers (ICW byte 12 - input X'4E') are incorrect, (the expected value of byte 12 was X'A1') or the message count (ICW bits 13.6 and 13.7) is incorrect, (The expected message count is 13.6 on and 13.7 off) or 13.1 (sequence 1) is not off. Register X'15' contains the bits in error. Register X'11' is the line under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X29	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 31.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X30	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'8400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X31	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 30 and 16.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X32	E2B2	TF81X	F-590
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X33	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 28.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X34	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'C400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6

0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X35	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X36	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0500'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X37	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X74F	0X38	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'8400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X750 SDLC Receive Test # 5 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests the receive actions when a flag off-boundry is received in an information frame or when trace is on. Diag 0=1 for both lines. Diag 1=1 for transmit line. Cycle Steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750 0X02	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750 0X03	E2C2	TF60X	F-580
	E3H2	TE54X	F-600
	E2E2	TF80X	F-570
	E2B2	TF81X	
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 off. Refer to SDLC Receive state transition 3, 22, and 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750 0X04	E2B2	TF81X	F-600
	E2K2	TF44X	F-580
	E2R2	TF32X	
	EJ2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 39.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0)..

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X750	0X05	E2F2	TF48X	F-560
		E2E2	TF80X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 39.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X06	E2E2	TF80X	F-160
		E2F2	TF48X	F-210
		E2B2	TF81X	F-240
		E2N2	TF22X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0D00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X07	E2N2	TF22X	F-230
		E2P2	TF82X	
		E3K2	TE24X	

ICW bit 6.5 should have been set off. Refer to SDLC Receive state transition 39.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X08	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	F-570
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 on. Refer to SDLC Receive state transition 22, 23, and 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X09	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 40.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X750	0X0A	E2F2	TF48X	F-560
		E2E2	TF80X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 40.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X0B	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0D00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X0C	E2N2	TF22X	F-230
		E2P2	TF82X	
		E3K2	TE24X	

ICW bit 6.5 should have been set off. Refer to SDLC Receive state transition 40.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X10	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	F-570
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 22, 23, 44, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X11	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 41.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X750	0X12	E2F2	TF48X	F-560
		E2E2	TF80X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 41.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X13	E2E2	TF80X	F-160
		E2N2	TF22X	F-210
		E2B2	TF81X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0D00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X14	E2N2	TF22X	F-230
		E2P2	TF82X	
		E3K2	TE24X	

ICW bit 6.5 should have been set off. Refer to SDLC Receive state transition 41.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X15	E2B2	TF81X	F-590
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 22, 23, 44, 45, and 49.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X16	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 42.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X17	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 42.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X18	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X19	E2P2	TF82X	F-230
		E2N2	TF22X	
		E3K2	TE24X	

ICW bit 6.5 should have been set off. Refer to SDLC Receive state transition 44.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X1A	E2E2	TF80X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	F-570
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/3 with sequence bit 13.0 on. Refer to SDLC Receive state transition 22 and 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X1B	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 38.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X1C	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC receive state 38.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X1D E2N2	TF22X	F-160
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0D00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X750	0X1E E2P2	TF82X	F-230
	E2N2	TF22X	
	E3K2	TE24X	

ICW bit 6.5 should have been set off. Refer to SDLC Receive state transition 38.

X751 SDLC Receive Test # 6 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests the receiving of an Abort after the third frame character, and after the fourth, sixth, and after the ending flag with bad CRC. Diag 0=1 for both lines. Diag 1=1 for transmit line. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X02 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X03	E2E2	TF80X	F-580
		E2C2	TF60X	F-590
		E3H2	TE54X	F-570
		E2B2	TF81X	
		E2R2	TF32X	
		E2K2	TF44X	
		E2J2	TF50X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 6/4 with sequence bit 13.0 on. Refer to SDLC Receive state transition 3, 22, 23, and 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X04	E2C2	TF60X	F-580
		E2P2	TF82X	F-600
		E2B2	TF81X	
		E2R2	TF32X	
		E2J2	TF50X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 18.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X05	E2B2	TF81X	F-600
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Program forced state 6/3 off. Refer to SDLC Receive state transition 44, 45, and 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X06	E2B2	TF81X	F-590
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 7/4 with sequence bit 13.0 undefined. Program forced state 6/4 off. Refer to SDLC Receive state transition 49.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X07 E2B2	TF81X	F-590
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	
	E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 7/4 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 47.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X08 E2B2	TF81X	F-600
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	
	E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X09 E2F2	TF48X	F-380
	E2N2	TF22X	F-390
	E2B2	TF81X	F-570
	E3L2	TE40X	
	E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

Either the PDF array pointers were not set to X'FF' or the message count was not 13.6 off and 13.7 on, or 13.1 was not on. Register X'15' contains the bits in error; byte 0 is the PDF array pointers, byte 1, bit 1 is sequence bit 1 and byte 1, bits 1.6-1.7 are the message count. If the Hi Speed Scanner Feature (230KB) is installed, bits 1.4 and 1.5 are the extended PDF pointer bits. Refer to SDLC receive state transition 10.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X10 E2B2	TF81X	F-600
	E2K2	TF44X	F-580
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Receiving non-flag and non-idle characters cause the scanner to remain in state 7/3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X11 E2B2	TF81X	F-590
	E2K2	TF44X	F-580

		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X12	E2B2	TF81X	F-590
		E2K2	TF44X	F-580
		E2R2	TF32X	
		E2J2	TF50X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 7/4 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 48, 23, 44, 45, and 49.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X13	E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 35.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X14	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to SDLC receive state 35. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X15	E2N2	TF22X	F-160
		E2E2	TF80X	F-210
		E2Q2	TF34X	F-240
		E2F2	TF48X	
		E2B2	TF81X	
		E2P2	TF82X	

The status posted in the receive line ICW was expected to be X'1480'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4

0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X16	E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 7/7 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 11.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X751	0X17	E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

X752 SDLC Receive Test # 7 LCD=1 EP

ROUTINE DESCRIPTION

This routine test the receive in control frame, end Flag/Abort idle sequence and receive idle while in monitor (PCF = 5) functions. Diag 0=1 for both lines. Diag 1=1 for transmit line. Cycle steal is used.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.

0002 Interrupt from wrong line - Reg X'14' equal to Reg X'11'.
0003 Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X03	E2E2	TF80X	F-580
		E3H2	TE54X	F-590
		E2J2	TF50X	F-570
		E2R2	TF32X	
		E2B2	TF81X	
		E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 3, 22, 23, 44, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X04	E2P2	TF82X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 46.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X05	E2E2	TF80X	F-570
		E2N2	TF22X	
		E2G2	TF40X	
		E3Q2	TE52X	

ICW bit 13.1 should have been set on. Refer to SDLC Receive state transition 46.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X06	E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 35.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X07	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 35.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X08	E3J2	TE22X	F-520
		E3K2	TE24X	
		E2C2	TF60X	

E2E2	TF80X
E2F2	TF48X
E2H2	TF42X

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X09	E2E2	TF80X	F-160
		E2B2	TF81X	F-210
		E2N2	TF22X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1490'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X0A	E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/2 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 48.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X0B	E2E2	TF80X	F-570
		E2N2	TF22X	
		E2G2	TF40X	
		E3Q2	TE52X	

ICW bit 13.1 should have been set off. Refer to SDLC Receive state transition 48.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X0C	E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 30, 43, 44, 45, 49, and 29.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X0D	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 29.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X0E	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0410'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X0F	E3K2	TE24X	F-520
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X10	E2C2	TF60X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/7 with sequence bit 13.0 undefined. Refer to SDLC receive state transition 11.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X11	E2N2	TF22X	F-380
		E2B2	TF81X	F-390
		E3L2	TE40X	F-570
		E2F2	TF48X	

ICW Byte 12 should be X'00' and ICW Byte 13, bits 6 and 7 should be off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X15	E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/7 with sequence bit 13.0 undefined. Refer to SDLC receive state transition N/A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X16	E2N2	TF22X	F-380
		E2B2	TF81X	F-390
		E3L2	TE40X	F-570
		E2F2	TF48X	

ICW Byte 12 should be X'00' and Byte 13, bits 6 and 7 should be off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X17	E2C2	TF60X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 11 and 20.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X18	E2N2	TF22X	F-380
		E2B2	TF81X	F-390
		E3L2	TE40X	F-570
		E2F2	TF48X	

ICW byte 12 should be X'01' and ICW 13.6 off and 13.7 on. (PDF and CS array pointers should be X'01' and message count should be 1).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X19	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 20.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X1A	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4410'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

Beg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X20		
	E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 21 (idle character detected).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X21		
	E2N2	TF22X	F-160
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4410'.

The status bits in error are in Register X'15'.

Beg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X22		
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 1. The program forced state 7/5 prior to this transition.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X23		
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Program forces state 7/5 prior to this test. Refer to SDLC Receive state transition 11 and 53.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X24		
	E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 53.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X752	0X25		
	E2N2	TF22X	F-160
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0410'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X753 SDLC Receive Test # 8 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests receiving Frame/Abort/Idle and Frame/Abort/Idle/Data with ICW bit 15.3 off (no program requested interrupt on line idle detect or flag) functions. Diag 0=1 for both lines. Diag 1=1 for transmit line. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X753	0X01		
	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X753	0X02		
	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14'

not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X753	0X03 E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/7 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 3, 22, 23, 44, 45, 49, 29, and 11.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X753	0X04 E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/7 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 11. Received idle and data characters with ICW bit 15.3 off; state should not change.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

X754 SDLC Receive Test # 9 LCD=1 EP

ROUTINE DESCRIPTION

This routine tests the following conditions when a flag is received in PCF/EPCF state 6/4 with sequence bit 13.0 off: (1) information frame/CRC good, (2) information frame/CRC bad, (3) non- information frame/CRC good, and (4) non-information frame/CRC bad. Diag 0=1 for both lines. Diag 1=1 for transmit line. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X02 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X03	E2E2	TF80X	F-580
		E3H2	TE54X	F-590
		E2J2	TF50X	F-570
		E2B2	TF81X	
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 3, 22, 23, 44, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X04	E2P2	TF82X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X05	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 34.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X06	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X07	E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	F-570
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 48, 23, 44, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X08	E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 36.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X09	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 36.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X0A	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF60X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 48, 23, 44, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X0C	E2C2	TF60X	F-580
		E2B2	TF81X	F-590

E2K2	TF44X	
E2R2	TF32X	
E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 51 and 52.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X0D	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 52.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X0E	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 6/4 with sequence bit 13.0 off. Refer to SDLC Receive state transition 48, 23, 44, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X10	E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 51 and 54.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X11 E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to SDLC Receive state transition 54.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X754	0X12 E2N2	TF22X	F-160
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X755 SDLC PDF1 Pointer Back-up Test Transmit LCD=C Receive LCD=9 Not EP

ROUTINE DESCRIPTION

This routine checks that the PDF array pointer is drecemented correctly when a valid frame is not detected. Diag 0=1 for both lines. Transmit PCF=E/0. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X02 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.

0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X03	E2B2	TF81X	F-520
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The receive line SDF should contain X'017F'. The incorrect SDF data is contained in X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X04	E2B2	TF81X	F-520
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The receive SDF did not shift properly or the wrap function did not work correctly. The routine is checking for an Abort in the receive SDF.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X05	E2C2	TF60X	F-380
		E3D2	TE34X	F-390
		E2F2	TF48X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers, ICW byte 12 - input X'4E' (also input X'41' for HSS), are incorrect. Register X'14' (bits 0.4-0.7) contains the expected value. Register X'15' (bits 0.4-0.7) contains the bit/s in error. Refer to SDLC Receive state transition 4. For HSS extended PDF ptr bit is contained in bit 1.5 of Register 14 and 15.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X06	E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Program forced state 6/2, 13.0 off before this test. Refer to SDLC Receive state transition 4.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X07	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers, ICW byte 12 - input X'4E' (also input X'41' for HSS), are incorrect. Register X'14' (bits 0.4-0.7) contains the expected value. Register X'15' (bits 0.4-0.7) contains the bit/s in error. Refer to SDLC Receive state transition 6. For HSS extended PDF ptr bit is contained in bit 1.5 of Register 14 and 15.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X08	E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Program forced state 6/3, 13.0 off before this thest. Refer to SDLC Receive state transition 6.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X09	E2F2	TF48X	F-380
		E3D2	TE34X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers, ICW byte 12 - input X'4E' (also input X'41' for HSS), are incorrect. Register X'14' (bits 0.4-0.7) contains the expected value. Register X'15' (bits 0.4-0.7) contains the bit/s in error. Refer to SDLC Receive state transition 8. For HSS extended PDF ptr bit is contained in bit 1.5 of Register 14 and 15.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X0A	E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Program Forced state 6/4, 13.0 off before this test. Refer to SDLC Receive state transition 8.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X0B	E2F2	TF48X	F-380
		E3D2	TE34X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers, ICW byte 12 - input X'4E' (also input X'41' for HSS), are incorrect. Register X'14' (bits 0.4-0.7) contains the expected value. Register X'15' (bits 0.4-0.7) contains the bit/s in error. Refer to SDLC Receive state transition 7. For HSS extended PDF ptr bit is contained in bit 1.5 of Register 14 and 15.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X0C	E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Program forced state 6/4, 13.0 on before this test. Refer to SDLC Receive state transition 7.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X0D	E3D2	TE34X	F-380
		E2F2	TF48X	F-390
		E2C2	TF60X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

PDF array pointers, ICW byte 12 - input X'4E' (also input X'41' for HSS), are incorrect. Register X'14' (bits 0.4-0.7) contains the expected value. Register X'15' (bits

0.4-0.7) contains the bit/s in error. Refer to SDLC Receive state transition 8. For HSS extended PDF ptr bit is contained in bit 1.5 of Register 14 and 15.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X755	0X0E	E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Program forced state 6/4, 13.0 off before this test. Refer to SDLC Receive state transition 8.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

X756 SDLC Zero Bit Insertion Test LCD=9 Not EP

ROUTINE DESCRIPTION

This routine checks that the SDLC transmit line inserts zero bits correctly. The transmit and receive lines have Diag 0=1 (scanner wrap) and the receive line has Diag 1=1 (PCF/EPCF=7/C). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X756	0X01	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2D2	TF62X	
		E2J2	TF50X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X756	0X02	E3F2	TE20X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X756	0X03	E2F2	TF48X	F-550
		E2E2	TF80X	F-560
		E3L2	TE46X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X756	0X04	E2E2	TF80X	F-520
		E2C2	TF60X	
		E3K2	TE24X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X757 SDLC Delete Inserted Zero Bit Test LCD=9 Not EP

ROUTINE DESCRIPTION

This routine checks that the SDLC receive line removes inserted zero bits correctly. The transmit and receive lines have Diag 0=1 (scanner wrap). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X757 0X01	E2D2	TF62X	F-220
	E2J2	TF50X	F-550
	E3F2	TE20X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X757 0X02	E2D2	TF62X	F-220
	E2J2	TF50X	F-550
	E3F2	TE20X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X757 0X03	E2F2	TF48X	F-550
	E2E2	TF80X	F-560
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X757 0X04	E2E2	TF80X	F-520
	E2C2	TF60X	
	E3K2	TE24X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X758 SDLC NRZI Test (Transmit) LCD=9 Not EP

ROUTINE DESCRIPTION

This routine checks that the NRZI transmit function is operating. The transmit and receive lines have Diag 0=1 (scanner wrap) and the receive line has Diag 1=1 (PCF/EPCF=7/C). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X758	0X01 E2D2	TF62X	F-220
	E2J2	TF50X	F-550
	E3F2	TE20X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X758	0X02 E2D2	TF62X	F-220
	E2J2	TF50X	F-550
	E3F2	TE20X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X758	0X03 E2E2	TF80X	F-550
	E2C2	TF60X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X758	0X04 E2C2	TF60X	F-520
	E3K2	TE24X	
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X759 SDLC NRZI Test (Receive) LCD=9 Not EP

ROUTINE DESCRIPTION

This routine checks that the NRZI receive function is operating. The transmit and receive line have Diag 0=1 (scanner wrap). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X759 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X759 0X02	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X759 0X03	E2F2	TF48X	F-550
	E2B2	TF81X	F-560
	E2E2	TF80X	
	E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X759 0X04	E2G2	TF40X	F-520
	E3K2	TE24X	
	E2C2	TF60X	
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X760 BSC Transmit Test LCD=C Not EP EBCDIC

ROUTINE DESCRIPTION

This routine tests state transitions and associated functions while in BSC, EBCDIC, not-EP, not-Transparent and internal clock. Two data bytes are sent with the status specifying STX-Data-ETX. The transmit line has Diag 0=1 (scanner wrap). Receive functions are not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760 0X02	E2B2	TF81X	F-580
	E2R2	TF32X	F-600
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be 9/0 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760 0X03	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760 0X04	E2E2	TF80X	F-580
	E2B2	TF81X	F-600
	E2R2	TF32X	F-570
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be 9/1 with sequence bit 13.0 on. Refer to BSC Transmit state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760 0X05	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X06	E2E2	TF80X	F-570
		E2K2	TF44X	F-580
		E2B2	TF81X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/1 with sequence bit 13.0 off. Refer to BSC Transmit state transition 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X07	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X08	E3E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2R2	TF32X	F-600
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 on. Refer to BSC Transmit state transition 4.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X09	E2B2	TF81X	F-410
		E2R2	TF32X	F-420
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E2Q2	TF34X	
		E2K2	TF44X	
		E2F2	TF48X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X0A	E2B2	TF81X	F-210
		E2Q2	TF34X	

ICW bit 5.4 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2R2	TF32X	F-600
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X0C	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X0D	E2B2	TF81X	F-570
		E2R2	TF32X	F-580
		E2E2	TF80X	F-590
		E2K2	TF44X	
		E2J2	TF50X	
		E2Q2	TF34X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X0E	E2B2	TF81X	F-410
		E2E2	TF80X	F-420
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X0F	E2C2	TF60X	F-210
		E2B2	TF81X	
		E2V2	TF41X	

The timeout counter was not properly set for 1 second timeout. Input 47 should have bits 0.2, 0.3, and 0.7 on, and 0.4 and 1.0 off. Reg X'15' (bits 0.2-0.4, 0.7 and 1.0) indicates bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X10	E2B2	TF81X	F-210
		E2Q2	TF34X	
		E2P2	TF82X	

ICW bit 5.4 should have been set off. Refer to BSC transmit state transition 45.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X11	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC field of the transmit line ICW should have reset to zero.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X760	0X13	E2E2	TF80X	F-410
		E2B2	TF81X	F-420
		E2J2	TF50X	
		E2H2	TF42X	

Tag time was not detected. ICW bit 3.2 (tag bit) either did not turn on after going off (tag bit set at tag time) or did not turn off (SDF shifting).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X14	E3E2	TE70X	F-410
		E2B2	TF81X	F-420
		E3K2	TE24X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01F0'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X15	E2B2	TF81X	F-570
		E2E2	TF80X	F-580
		E2R2	TF32X	F-590
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 29.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X16	E2E2	TF80X	F-410
		E2B2	TF81X	F-420
		E2J2	TF50X	
		E2H2	TF42X	

Tag time was not detected. ICW bit 3.2 (tag bit) either did not turn on after going off (tag bit set at tag time) or did not rurn off (SDF shifting).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X17	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X18	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2R2	TF32X	F-590
		E2K2	TF22X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X760	0X19	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X1A	E2E2	TF80X	F-570
		E2R2	TF32X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2J2	TF50X	
		E2Q2	TF34X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to BSC Transmit state transition 38.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X1B	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X1C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2R2	TF32X	F-590
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 off. Refer to BSC Transmit state transition 39.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X1D	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0152'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X1E	E2P2	TF82X	F-240
		E2S2	TF21X	
		E3Q2	TE52X	
		E3R2	TE26X	

ICW bit 16.0 (New Sync) should be off. The bit was detected on in state PCF=9, EPCF=6, and sequence bit 0=0, this bit should be off during execution of the entire routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X760	0X1F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2R2	TF32X	F-590
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Refer to BSC Transmit state transition 40.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X20	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0129'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X21	E2B2	TF81X	F-580
		E2R2	TF32X	F-600
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 35 and 35A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X22	E2E2	TF80X	F-550
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to BSC Transmit state transition 35A.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X760	0X23	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0432'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X760	0X24	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

Unexpected L2 occurred. Register X'15' contains line address of line causing L2 interrupt.

X761 BSC Transmit Test 2 LCD=C EBCDIC Not EP

ROUTINE DESCRIPTION

This routine tests state transitions and associated functions while in BSC, EBCDIC, External Clock, Leading Graphics, Data Chain and single character response (EOT). State transition flow is 1, 12, 5, 16, 13, 22, 28, 41. The transmit line uses Diag 0=1 (scanner wrap). Receive functions are not used (transmit only). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X02	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2R2	TF32X	F-600
	E2J2	TF50X	
	E2K2	TF44X	

The PCF/EPCF should be B/2 with sequence bit 13.0 on. Refer to BSC transmit state transition 1 and 12.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X03	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X04	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2R2	TF32X	F-600
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be B/2 with sequence bit 13.0 off. Refer to BSC transmit state transition 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X05	E2P2	TF82X	F-240
	E2S2	TF21X	
	E3Q2	TE52X	
	E3R2	TE26X	

ICW bit 16.0 (New Syn) failed to set. With PCF=B, transition to state EPCF=2/Seq Bit 0=0 should set 'New Syn' bit.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X06	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X07	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be B/2 with sequence bit 13.0 off. Refer to BSC transmit state transition 16.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X08	E3E2	TE70X	F-410
	E2B2	TF81X	F-420
	E2Q2	TF34X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	
	E2P2	TF82X	

The transmit line SDF should contain X'01F0'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X09	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2R2	TF32X	F-600
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be B/2 with sequence bit 13.0 off. Refer to BSC transmit state transition 13.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761 0X0A	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2R2	TF32X	F-590
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be B/5 with sequence bit 13.0 off. Refer to BSC transmit state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761	0X0B	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0137'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2R2	TF32X	F-590
		E2K2	TF44X	
		E2J2	TF50X	

The PCF/EPCF should be B/7 with sequence bit 13.0 on. Refer to BSC transmit state transition 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761	0X0D	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761	0X0E	E2P2	TF82X	F-240
		E2S2	TF21X	
		E3Q2	TE52X	
		E3R2	TE26X	

ICW bit 16.0, 'New Syn' failed to reset. Refer to BSC transmit state transition 28.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be B/7 with sequence bit 13.0 off. Refer to BSC transmit state transition 41.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X761	0X10	E2F2	TF48X	F-380
		E2C2	TF60X	F-390
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

ICW byte 12 should equal X'11'. Checks that one byte was transmitted.

X762 BSC Transmit Test 3 LCD=4 EP EBCDIC

ROUTINE DESCRIPTION

This routine tests getting to the 'do-nothing' state (Diagnostic bit 1) and checks that selected control characters do not cause state transitions from EPCF=C. State transition flow is 23, 10, 10, 10, 19, 31, 35A. The transmit line used Diag 0 and Diag 1 set to 1 (scanner wrap and PCF/EPCF=9/C). Receive functions are not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762 0X02	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/C with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762 0X03	E3K2	TE24X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	
	E2B2	TF81X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762 0X04	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0137'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762 0X05	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0101'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762	0X06 E2E2	TF80X	F-550
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the transmit line because the byte count went to zero. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762	0X07 E2J2	TF50X	F-560
	E2N2	TF22X	
	E3L2	TE40X	
	E3Q2	TE52X	

ICW bit 0.1 should have been set on. Register X'11' contains the line address under test.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762	0X08 E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/C with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762	0X09 E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762	0X0A E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 35A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762	0X0B E2E2	TF80X	F-550
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to BSC Transmit state transition 35A.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762	0X0C E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'2400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X762	0X0D E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

An unexpected L2 interrupt occurred. Register X'15' contains line address of line causing L2 interrupt.

X763 BSC Transmit EP Mode EBCDIC LCD=4

ROUTINE DESCRIPTION

This routine tests EP mode, first byte not control (leading graphics), DLE in data, SYN in data, control byte in data, PDF empty with data chain on, and PDF empty with data chain off. The transmit line uses Diag 0=1 (scanner wrap). Receive functions are not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X02 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCP/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X03	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF sho ld contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X04	E3E2	TE70X	F-410
		E3K2	TE24X	F-420
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01F0'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 62.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X06	E2B2	TF81X	F-240
		E2Q2	TF34X	
		E2P2	TF82X	

ICW bit 15.7 should have been set on. Refer to BSC Transmit state 62.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X07	E2B2	TF81X	F-580
		E2R2	TF32X	F-600
		E2K2	TF44X	
		E2J2	TF50X	
		E2Q2	TF34X	
		E2E2	TF80X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X08	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X0A E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X0B E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 58.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X0C E2B2	TF81X	F-570
	E2E2	TF80X	F-580
	E2R2	TF32X	F-600
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 54.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X0D E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0102'.

SDF SHOULD CONTAIN C1 INSTEAD OF 02 IF RPQ EH4100 IS INSTALLED.

The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X0E E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X0F E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 63.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X11	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01F1'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X12	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 57.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X14	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 81.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X15	E2B2	TF81X	F-410
		E2C2	TF60X	F-420

	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0102'.

SDF SHOULD CONTAIN C1 INSTEAD OF 02 IF RPQ EH4100 IS INSTALLED.

The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X16 E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X17 E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X18 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50x	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 82.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X19 E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X1A E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'2001'.

EXPECTED STATUS POSTED WILL BE X'2000' IF RPQ EH4100 IS INSTALLED.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X1B E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X763	0X3A E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

THIS STOP SHOULD OCCUR ONLY IF RPQ EH4100 IS INSTALLED.

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Receive State transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X1C E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Refer to BSC Transmit state transition 82 and 78.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X1D E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X763	0X1E E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X763 0X3A SEE ERROR STOP 0X3A FOLLOWING ERROR STOP 0X1B.

X764 BSC Transmit Not EP: Control In Data Stream LCD=C EBCDIC

ROUTINE DESCRIPTION

This routine checks various conditions of control characters in the data stream. DLE/data, DLE/STX (change to transparent), DLE/DLE. Status specifies SOH/data/ETX. The transmit line uses Diag 0=1 (scanner wrap). Receive functions are not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764 0X02	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, 5 and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764 0X03	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0101'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X05	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X07	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X08	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01F1'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 29.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X0A E2R2	TF82X	F-590
	E2J2	TF50X	F-580
	E2B2	TF81X	
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 9/8 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 47A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X0B E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X0C E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 48.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X0D E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X0E E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2R2	TF32X	F-590
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X0F E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 47.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X10	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X12	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Transmit state transition 52.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X14	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 59.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X764	0X15	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X16	E2B2	TF81X	F-210
		E2Q2	TF34X	
		E2P2	TF82X	
		E2K2	TF44X	

ICW bit 5.4 should have been set on. Refer to BSC Transmit state transition 59; DLE STX received should set transparent mode.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X17	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01F2'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X18	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E1R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X19	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X1A	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X1B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580

	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X1C E2B2	1F81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X1D E2B2	TF81X	F-230
	E2L2	TF46X	
	E2P2	TF82X	
	E2K2	TF44X	

The BCC bytes (input X'4A') were not correct. Register X'17' contains expected value.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X20 E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 38, 39, 40, 35, and 35A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X764	0X21 E2B2	TF81X	F-210
	E2Q2	TF34X	
	E2P2	TF82X	

ICW bit 5.4 should have been set off.

X765 BSC Transmit Test; Not EP, Transparent LCD=C EBCDIC

ROUTINE DESCRIPTION

This routine checks transparent operation and various conditions of control characters in the data stream. Data chain on with and without the last byte being a control character, and a control character in data with and without the byte count = 0 are tested. The transmit line uses Diag 0=1 (scanner wrap). Receive functions are not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X01 E3P2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X02	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 1, 2, 3, 4, 5 and 49.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X03	E3K2	TE24X	F-410
		E2B2	TF81X	F-420
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X05	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X06	E2R2	TF32X	F-580
		E2J2	TF50X	F-570
		E2E2	TF80X	F-590
		E2B2	TF81X	
		E2K2	TF44X	
		E2Q2	TF34X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Transmit state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X765	0X07	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X08	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 66.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X09	E2B2	TF81X	F-410
		E2P2	TF82X	F-420
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X0A	E2P2	TF82X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/8 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 73.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X0B	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 48.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X0D	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X0E	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

An L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X0F	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X11	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0126'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X12	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765 0X13	E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

An L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765 0X14	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'012D'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765 0X15	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765 0X16	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765 0X17	E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765 0X18	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X19 E2B2	TF81X	F-410
	E2C2	TF60X	F-420
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The transmit line SDF should contain X'0126'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X1A E2L2	*TF46X	F-230
	E2B2	TF81X	
	E2P2	TF82X	

The BCC bytes (input X'4A') were not correct. Register X'17' contains expected value.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X765	0X1B E2N2	TF22X	f-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0054'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X766 BSC XMIT; NOT-EP, XPARENT (ITB) LCD=C EBCDIC

ROUTINE DESCRIPTION

This routine checks the operation of the scanner when the status specifies DLE/STX - Data - DLE/ITB. The transmit line uses Diag 0=1 (scanner wrap). Receive functions are not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X766	0X02	E2E2	TF80X	F-570
		E2P2	TF82X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 1, 2, 3, 4, 5, 45, 50, 29 and 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X03	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 61.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X05	E2E2	TF80X	F-410
		E2F2	TF48X	F-420
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E2Q2	TF34X	

The transmit line SDF should contain X'011F'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X06	E2E2	TF80X	F-570
		E2G2	TF40X	
		E3Q2	TE52X	

ICW bit 13.1 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X07	E2E2	TF80X	F-550
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to BSC Transmit state transition 61.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X766	0X08	E2N2	TF80X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0448'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to BSC Transmit state transition 33.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X0A	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0105'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

Check input X'4A' for BCC byte 2. If the byte in the ICW is correct, the BCC to SDF shift was not correct. Otherwise, the BCC accumulation is in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X0C	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C8'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

Check input X'4A' for BCC byte 1. If the byte in the ICW is correct, the BCC to SDF shift was not correct. Otherwise, the BCC accumulation is in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X766	0X0D E2B2	TF81X	F-210
	E2Q2	TF34X	
	E2P2	TF82X	

ICW bit 5.4 (transparent mode) should have been set off. Refer to BSC transmit state transition 34.

X767 BSC Transmit - General LCD=C Not EP EBCDIC

ROUTINE DESCRIPTION

This routine tests the following conditions; ENQ in data while in not-EP and leading graphics; Time-out in text mode (9/4); RTS Turn Control in State 9/C. The transmit line uses Diag 0=1 (scanner wrap). Receive functions are not used. Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X767	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X767	0X02 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4 and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X767	0X03 E2Q2	TF34X	F-570
	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	
	E2P2	TF82X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X767	0X04 E2P2	TF82X	F-150
	E2N2	TF22X	F-210

E2B2	TF81X	F-240
E2E2	TF80X	
E2F2	TF48X	
E2Q2	TF34X	
E2K2	TF44X	

The status posted in the transmit line ICW was expected to be X'0007'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X767	0X05	E2J2	TF50X	F-570
		E2C2	TF60X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2E2	TF80X	

The PCF/EPCF should be 9/8 with sequence bit 13.0 undefined. Program forces state 9/4, 13.0 off before this test. Refer to BSC Transmit state transition 46.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X767	0X06	E2B2	TF81X	F-410
		E2C2	TF60X	F-420
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X767	0X07	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 off. The program forced state 9/C prior to this state change. Refer to BSC Transmit state transition 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X767	0X08	E2D2	TF62X	F-220
		E2C2	TF60X	
		E2E2	TF80X	

Request to Send (RTS) was not reset in Data Out 1-7 to LIB. Refer to BSC Transmit state transition 42.

X768 BSC Receive In Diagnostic Mode; 'Do-Nothing' Mode Transmit LCD=C Receive LCD=4 EBCIDIC

ROUTINE DESCRIPTION

This routine tests (1) that the receive line gets toPCF/EPCF state 7/C, (2) that control characters STX and ETX received do not cause a state change, and (3) that these control characters are placed in storage when received in this state. The transmit and Receive lines have Diag 0 and Diag 1=1 (scanner wrap and PCF/EPCF=to 9/C and 7/C) Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X768	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X768	0X02 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X768	0X04 E2E2	TF80X	F-570
	E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X768	0X05 E2J2	TF50X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 7/C with sequence bit 13.0 undefined. Refer to BSC Receive state transition 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X768	0X06 E2J2	TF50X	F-580
	E2B2	TF81X	F-590

E2K2	TF44X	
E2R2	TF32X	

The PCF/EPCF should be 7/C with sequence bit 13.0 undefined. Refer to BSC Receive state transition 4.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X768 0X07	E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X768 0X08	E3K2	TE24X	F-480
	E2C2	TF60X	
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received is not as expected. Register X'13' contains the data expected; Register X'16' contains the data received.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X768 0X0A	E3K2	TE24X	F-480
	E2C2	TF60X	
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received is not as expected. Register X'13' contains the data expected; Register X'16' contains the data received.

X769 BSC Receive Normal Text LCD=C EBCDIC Not EP

ROUTINE DESCRIPTION

This routine test for normal test received conditions. The data stream expected to be received is SYN/SYN/STX/data/SYN/data/ETX/BCC. The transmit and receive lines have Diag 0=1 (scanner wrap) and the transmit line has Diag 1=1 (PCF/EPCF=9/C). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X02	E3F2	TE20X	F-220
	E2D2	TF62X	F-550

E2J2	TF50X	
E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X04	E2E2	TF80X	F-570
	E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 1 and 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X05	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2G2	TF40X	

ICW bit 13.3 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X06	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X07	E2B2	TF81X	F-230
	E2L2	TF46X	
	E2P2	TF82X	

Input X'4A' was used to check for BCC reset. The BCC was not X'0000' as expected. Register X'15' contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X08	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X09	E3L2	TE40X	F-560
	E2N2	TF22X	
	E2B2	TF81X	
	E3R2	TE26X	

ICW bit 0.4 should be off. This bit should be reset when a level 2 interrupt is requested. Refer to BSC Receive state transition 26.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X0A	E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X0B	E2N2	TF22X	F-560
	E2J2	TF50X	
	E2T2	TF20X	
	E3L2	TE40X	
	E3Q2	TE52X	

ICW bit 0.1 (service request) is not on as expected. Input X'44' should indicate the bits on. Refer to BSC Receive state transtion 26.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X0C	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2G2	TF40X	

ICW bit 13.3 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X0D	E3L2	TE40X	F-560
	E3R2	TE26X	
	E2N2	TF22X	
	E2B2	TF81X	

ICW bit 0.4 (not-L2bid) is off indicating a L2 request which is not expected. Refer to BSC Receive state transition 26.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X0F	E2F2	TF82X	F-570
	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Refer to BSC Receive state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X10	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590

E2R2	TF32X	
E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769	0X11 E2B2	TF81X	F-570
	E2R2	TF32X	F-580
	E2E2	TF80X	F-590
	E2K2	TF44X	
	E2J2	TF50X	
	E2P2	TF82X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 51.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769	0X12 E2E2	TF80X	F-570
	E2K2	TF44X	

Input X'4E' was used to check for a reset of ICW bits 13.3 and 13.1. Register X'15' bits 1.1 and 1.3 indicate the bit(s) in error. Refer to BSC Receive state transition 51.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769	0X13 E2B2	TF81X	F-570
	E2R2	TF32X	F-580
	E2E2	TF80X	F-590
	E2K2	TF44X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 47.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769	0X14 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 33.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769	0X15 E2E2	TF80X	F-240
	E2F2	TF48X	
	E2G2	TF40X	

ICW bit 13.3 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X16	E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 53.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X17	E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X769 0X18	E2E2	TF80X	F-150
	E2F2	TF48X	F-210
	E2B2	TF81X	F-240
	E2N2	TF22X	
	E2Q2	TF34X	
	E2P2	TF82X	

The status posted in the receive line ICW was expected to be X'0432'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

CHAPTER 7.1:TYPE 3 COMMUNICATIONS SCANNER SYMPTOM INDEX

X76A BSC Receive Transparent Test LCD=C EBCDIC Not EP

ROUTINE DESCRIPTION

This routine tests receiving a SYN character in PCF/EPCF state 5/1 with sequence bit 13.1 off while in transparent mode.

The data expected to be received is DLE/STX, DLE/DLE, and DLE/ETX with good BCC received. This routine checks the following state transitions:

2, 14, 6, 22, 8, 68, 76, 72, 68, 67, 47, 33, and 53.

The transmit and receive lines have Diag 0=1 (scanner wrap) and the transmit line has Diag 1=1 (PCF/EPCF=9/C). Cycle steal is used.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X03	E2E2	TF80X	F-570
		E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X04	E2B2	TF81X	F-210
		E2C2	TF60X	
		E2V2	TF41X	

The BSC time-out counter was not set for 3-second time out. ICW bit 4.3 should be on and bits 4.2, 4.4, 4.7, and 5.0 should be off. Register X'15' contains the bits in error. Refer to BSC Receive state transition 2.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 2 and 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 6.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X07	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X08	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 8.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 76.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X0B	E2N2	TF22X	F-560
		E2J2	TF50X	
		E2T2	TF20X	
		E3L2	TE40X	
		E3Q2	TE52X	

Either 'not-L2-bid' (ICW bit 0.4) was on or 'service request' (ICW bit 0.1) was off. Register X'15' contains bits in error. Refer to BSC Receive state transition 76.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X0C	E2E2	TF80X	F-550
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to BSC Receive state transition 76.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X11	E2P2	TF82X	F-570
		E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 68 and 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A	0X12	E2E2	TF80X	F-570
		E2G2	TF40X	
		E2N2	TF22X	
		E3Q2	TE52X	

ICW bit 13.1 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A 0X13	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 47.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A 0X14	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2G2	TF40X	

ICW bit 13.3 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A 0X15	E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 53.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A 0X16	E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76A 0X17	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0452'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X76B BSC Receive Miscellaneous Conditions LCD=C EBCDIC Not EP

ROUTINE DESCRIPTION

This routine test (1) receive ITB/ETB/ETX as first non-SYN (ETX used), (2) reveive DLE/DLE/SYN ans first characters, (3) receive non-control leading DLE error - go into leading graphics mode, (4) receive SYN in leading graphics, (5) receive DLE/DLE/SYN (DLE in leading graphics), and (6) receive DLE/SYN (DLE in leading graphics state). The transmit and receive lines have Diag 0=1 (scanner wrap) and the transmit line has Diag 1=1 (PCF/EPCF=9/C). Cycle steal is used.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X02	E2F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X03	E2E2	TF80X	F-570
		E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2R2	TF32X	
		E2K2	TF44X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X04	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 42.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X05	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X06	E2E2	TF80X	F-240
		E2F2	TF48X	
		E2G2	TF40X	

ICW bit 13.3 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X07	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X08	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Program forces state 5/1, 13.0 off before this test. Refer to BSC Receive state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X09	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 49.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X10	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 62.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X11	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0201'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X12	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 16.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

X76B 0X13 See error stop after 0X17

X76B 0X14 See error stop after 0X17

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X15	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 7.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X16	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X76B	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 11.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X76B	0X13	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

This stop occurs only if RPQ EH4100 is installed.

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X76B	0X14	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

This stop occurs only if RPQ EH4100 ia installed.

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 49.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X18	E2J2	TF50X	F-580
		E2K2	TF44X	F-600
		E2B2	TF81X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 46.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X19	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 35.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X20 E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	
	E2H2	TF42X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 59.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X21 E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to BSC Receive state transition 59.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X22 E2Q2	TF34X	F-150
	E2N2	TF22X	F-210
	E2B2	TF81X	F-240
	E2E2	TF80X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'060E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X23 E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 2, 14, 22, and 56.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X24 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0201'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76B	0X25	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2H2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X76C BSC Receive LCD=C EBCDIC Not EP

ROUTINE DESCRIPTION

This routine tests (1) idle in PCF/EPCF state 7/8 -receive SYN-, (2) receive good LRC following ASCII ETX, and (3) receive bad LRC following ASCII ITB. The transmit and receive lines have Diag 0=1 (scanner wrap). and the transmit line has Diag 1=1 (PCF/EPCF=9/C). Cycle steal is used.

	ERRORCODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X03	E2E2	TF80X	F-570
	E2J2	TF50X	F-580
	E2B2	TF81X	F-590
	E2R2	TF32X	
	E2K2	TF44X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 2, 14, and 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X04	E2P2	TF82X	F-570
	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Refer to BSC Receive state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X05	E2C2	TF60X	F-210
	E2V2	TF41X	
	B2B2	TF81X	

ICW bit 4.3 should have been set on; ICW bits 4.2, 4.4, 4.7 and 5.0 should be off. Timeout counter set for 3 seconds. Register X'15' (bits 0.2-0.4, 0.7 and 1.0) contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X06	E2H2	TF42X	F-480
	E2E2	TF80X	F-500
	E2B2	TF81X	
	B2J2	TF50X	

Tag time was not detected. Refer to BSC Receive state transition 53A.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X07	E2E2	TF80X	F-570
	E2G2	TF40X	
	E3Q2	TE52X	

ICW bit 13.1 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X08	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Refer to BSC Receive state transition 70A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X76C	0X09	E2B2	TF81X	F-210
		E2C2	TF60X	
		E2V2	TF41X	

ICW bit 4.3 should be on; ICW bits 4.2, 4.4, 4.7, and 5.0 should be off. Timeout counter set for 3 seconds. Register X'15' (bits 0.2-0.4, 0.7 and 1.0) contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X0B	E2V2	TF41X	F-210
		E2C2	TF60X	
		E2B2	TF81X	

ICW bit 4.3 should be on; ICW bits 4.2, 4.4, 4.7, and 5.0 should be off. Timeout counter set for 3 seconds. Register X'15' (bits 0.2-0.4,0.7 and 1.0) contains the bits in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Refer to BSC Receive state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X0D	E2N2	TF22X	F-570
		E2E2	TF80X	
		E2G2	TF40X	
		E3Q2	TE52X	

ICW bit 13.1 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X0E	E2N2	TF22X	F-560
		E2J2	TF50X	
		E2T2	TF20X	
		E3L2	TE40X	
		E3Q2	TE52X	

ICW bit 0.1 should be on and ICW bit 0.4 should be off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X0F	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X10	E2B2	TF81X	F-570
	E2K2	TF44X	F-580
	E2E2	TF80X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF shoul. be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 53A and 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X11	E2B2	TF81X	F-570
	E2K2	TF44X	F-580
	E2E2	TF80X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Refer to BSC Receive state transition 63.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X12	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 40.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X13	E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 59.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X15	E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to BSC Receive state transition 59.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C 0X16	E2N2	TF22X	F-150
	E2E2	TF80X	F-210
	E2F2	TF48X	F-240
	E2Q2	TF34X	
	E2B2	TF81X	

The status posted in the receive line ICW was expected to be X'0426'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 2 and 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X1A	E2E2	TF80X	F-570
		E2F2	TF48X	F-580
		E2J2	TF50X	F-590
		E3Q2	TE52X	
		E2B2	TF81X	
		E2K2	TF44X	
		E2R2	TF32X	
		E2H2	TF42X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 53A and 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X20	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X21	E2E2	TF80X	F-210
		E2F2	TF48X	
		E2G2	TF40X	

ICW bit 13.3 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X76C	0X22	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 53.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X23	E3L2	TE40X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'15').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X24	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0412'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X27	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 53A and 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X28	E2E2	TF80X	F-570
		E2Q2	TF34X	
		E2G2	TF40X	
		E3Q2	TE52X	

ICW bit 13.1 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X29	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 12.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X2A	E2E2	TF80X	F-210
		E2F2	TF48X	
		E2G2	TF40X	

ICW bit 13.3 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X30	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 39.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X31	E3L2	TE40X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to BSC Receive state transition 39.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X33	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1402'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2

0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X76C	0X35. E2F2	TF48X	F-480
	E3K2	TE24X	
	E2E2	TF80X	
	E2C2	TF60X	
	E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X770 LRC Accumulation Test Transmit LCD=C Receive LCD=D Not EP

ROUTINE DESCRIPTION

This routine checks the LRC calculation circuitry. Data is wrapped internally and the LRC calculation is checked as the data bytes are received. The transmit and receive lines have Diag 0=1 (scanner wrap) and the transmit line has Diag 1=1 (PCF/EPCF=9/C). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X770	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X770	0X02 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X770	0X03 E2E2	TF80X	F-570
	E2J2	TF50X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	
	E2H2	TF42X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 1, 14 and 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X770	0X04	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

BCC accumulation was not correct. Reg X'16' contains expected BCC and input X'4A' has the actual accumulation.

X771 BSC CRC Accumulation Test LCD=C EBCDIC Not EP

ROUTINE DESCRIPTION

This routine checks the CRC accumulation as internal wrapped data bytes are received. The transmit and receive lines have Diag 0=1 (scanner wrap) and the transmit line has Diag 1=1 (PCF/EPCF=9/C). Cycle steal is used.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X771	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X771	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X771	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 1, 14 and 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X771	0X04 E2B2	TF81X	F-230
	E2L2	TF46X	
	E2P2	TF82X	

BSC BCC accumulation was not correct. Reg X'16' contains expected accumulation and register X'4A' contains the actual accumulation.

X772 SDLC Block Check Character Accumulation Test LCD=9 Not EP

ROUTINE DESCRIPTION

This routine checks the SDLC BCC accumulation circuitry. Data is wrapped internally and the BCC accumulation is verified. The transmit and receive lines have Diag 0=1 (scanner wrap). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X772	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X772	0X02 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X772	0X03 E2C2	TF60X	F-580
	E2J2	TF50X	F-590
	E2B2	TF81X	
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 undefined. Refer to SDLC Receive state transition 3, 22, 23, 44, 45, 49, and 47.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X772	0X04 E2F2	TF48X	F-230
	E3K2	TE24X	
	E2B2	TF81X	
	E2L2	TF46X	

SDLC CRC accumulation was not correct. Reg X'16' contains the expected accumulation and register X'4A' contains the actual accumulation.

X773 SDLC CRC Data Check Test LCD=9 Not EP

ROUTINE DESCRIPTION

This routine verifies that a data check occurs if the BCC accumulation is not X'F0B8'. The Transmit and Receive lines have Diag 0=1 (scanner wrap) and the transmit line has Diag 1=1 (PCD/EPCF=9/C). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X773 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X773 0X02	E3F2	TE20X	F-220
	E3R2	TE26X	F-550
	E2J2	TF50X	
	E2D2	TF62X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X773 0X03	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 6/1 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X773 0X04	E2E2	TF80x	F-560
	E2F2	TF48x	
	E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X773	0X05	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2P2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X774 LRC/VRC Data Check Test Transmit LCD=4, Receive LCD=D

ROUTINE DESCRIPTION

This routine verifies that a data check occurs if the BCC accumulation is not zero. A bit is rippled through the accumulation to verify that all bit positions can cause a check. The transmit and receive lines use Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). This routine also uses cycle steal.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X774	0X01	E3F2	TE30X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A Set Mode interrupt failed on the receive line (Address in Register X'11). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003	Feedback Check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X774	0X03	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCFshould be 5/1 with sequence bit 13.0 off. Refer to BSC Receive State transition 2 and 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3). EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X774	0X04	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 32,70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X774	0X05	E2E2	TF80x	F-560
		E2F2	TF48x	
		E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X774	0X06	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X774	0X10	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X775 BSC EBCDIC CRC Data Check Test LCD=C, Not EP

ROUTINE DESCRIPTION

This routine verifies that a data check occurs if the BCC accumulation is not zero. A bit is rippled through the accumulation to verify that all BCC bit positions can cause a data check. The transmit and receive lines use Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1. The PCF/EPCF is 9/C; this routine also uses cycle steal

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X775	0X01	E3F2	TE30X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A Set Mode interrupt failed on the receive line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003	Feedback Check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X775	0X03	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive State transition 2,70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X775	0X04	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X775	0X05	E2E2	TF80x	F-560
		E2F2	TF48x	
		E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X775	0X06 E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	00.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X779 BSC Transmit Test; Cycle Steal Ending Characters ETB, ETX, and ENQ - EBCDIC - EP

ROUTINE DESCRIPTION

This routine verifies that ending control characters (ETB, ETX, ENQ) in the cycle steal data reset the cycle steal valid bit (ICW bit 6.5) and set the decode bit (ICW bit 6.4). EP mode (LCD=4) is used in this routine. Diag 0=1 (scanner wrap) used for transmit line.

Cycle steal valid is turned on again after being set off if the byte count is not zero and the line is in transparent mode. Receive functions are not used in this routine (transmit only). Cycle steal is used.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X02 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2. 3, 4, and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X779	0X03	E3D2	TE34X	F-360
		E3K2	TE24X	
		E3L2	TE40X	
		E3Q2	TE52X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

An ETB should have been decoded during a cycle steal fetch operation.

Results:

ICW bit 6.4 on (end character decoded)

ICW bit 6.5 off (cycle steal valid off)

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X05	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 69 and 70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X06	E2P2	TF82X	F-210
	E2B2	TF81X	
	E2Q2	TF34X	

ICW bit 5.4 (transparent mode) should have been set on. Refer to BSC Transmit state transition 70.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X07	E3K2	TE24X	F-230
	E2N2	TF22X	
	E2P2	TF82X	
	E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

ICW bit 6.5 (cycle steal valid) should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X08	E2B2	TF81X	F-410
	E2E2	TF80X	F-420
	E2H2	TF42X	
	E2J2	TF50X	

A transmit tag was not detected. Either ICW bit 3.2 (tag bit) did not turn on after going off, or it did not go off (SDF shifting).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X09	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X10 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0048'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X12 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to BSC Transmit state transition 60, 60, 67, 61, and 33.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X13 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X14 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition (forced state).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X779	0X15	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X16	E3K2	TE24X	F-360
		E3L2	TE40X	
		E3Q2	TE52X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

An ETX should have been decoded during a cycle steal fetch operation.

The expected results are: ICW bit 6.4 (end character decoded) set, ICW bit 6.5 (cycle steal valid) reset and ICW bit 6.6 (data chain) set.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X17	E2J2	TF50X	F-380
		E3Q2	TE52X	F-390

The PDF array pointer (ICW byte 12) was not correct. The expected value of byte 12 is X'9X'. If register X'4E' contains X'7X', data character X'17' (ASCII ETB) was decoded as an EBCDIC ending character. If register X'4E' contains X'8X', data character X'05' (ASCII ENQ) was decoded as an EBCDIC ending character.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X20	E2B2	TF81X	F-410
		E2E2	TF80X	F-420
		E2H2	TF42X	
		E2J2	TF50X	

A transmit tag was not detected. Either ICW bit 3.2 (tag bit) did not turn on after being turned off, or it never turned off (SDF shifting)

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X21	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 29.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X23	E2N2	TF22X	F-560
		E2B2	TF81X	
		E2J2	TF50X	
		E3L2	TE22X	

The L2 pending bit is incorrectly set in the ICW. ICW bit 0.4 should be on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X779	0X24	E2E2	TF80X	F-570
		E2P2	TF82X	
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to BSC Transmit state transition 18 and 38.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X25	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0032'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition (forced state).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X27	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X28	E3K2	TE24X	F-360
		E3L2	TE40X	
		E3Q2	TE52X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

An ENQ should have been decoded during a cycle steal fetch operation.

The expected results are: ICW bit 6.4 (end character decoded) on and ICW bit 6.5 (cycle steal valid) off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X29	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X30	E2B2	TF81X	F-210
	E2Q2	TF34X	
	E2P2	TF82X	

ICW bit 5.4 (transparent mode) should have been set on. Refer to BSC Transmit state 70.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X31	E2N2	TF22X	F-230
	E3K2	TE24X	
	E3D2	TE34X	
	E2P2	TF82X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

ICW bit 6.5 (cycle steal valid) should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X33	E2E2	TF80X	F-410
	E2B2	TF81X	F-420
	E2H2	TF42X	
	E2J2	TF50X	

A transmit tag was not detected. Either ICW bit 3.2 (tag bit) did not turn on after being turned off or it did not turn off (SDF shifting).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X34	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779 0X35	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0048'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Chec	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X36	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to BSC Transmit state transition 60, 60, 67, 61, and 33.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X779	0X37	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

X77A BSC Transmit Test; Cycle Steal Ending Characters ETB, ETX, and ENQ - USASCII - Transparent - EP

ROUTINE DESCRIPTION

This routine verifies that ending control characters (ETB, ETX, ENQ) in the cycle steal data reset the cycle valid bit (ICW bit 6.5) and set the decode bit (ICW bit 6.4). EP mode (LCD = 6) is used in this routine. Diag 0=1 (scanner wrap) used for transmit line.

Cycle steal valid is turned on again after being set off if the byte count is not zero and the line is in transparent mode. Receive functions are not used in this routine (transmit only). Cycle steal is used.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X77A	0X02	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	
		E2P2	TF82X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2. 3, 4, and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X03	E3K2	TE24X	F-360
	E3L2	TE40X	
	E3Q2	TE52X	
	E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

An ETB should have been decoded during a cycle steal fetch operation.

Results:

ICW bit 6.4 on (end character decoded)

ICW bit 6.5 off (cycle steal valid off)

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X05	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 69 and 70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X06	E2B2	TF81X	F-210
	E2Q2	TF34X	
	E2P2	TF82X	

ICW bit 5.4 (transparent mode) should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X07	E2N2	TF22X	F-230
	E3K2	TE24X	
	E2P2	TF82X	
	E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

ICW bit 6.5 (cycle steal valid) should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X08	E2E2	TF80X	F-410
	E2B2	TF81X	F-420
	E2H2	TF42X	
	E2J2	TF50X	

A transmit tag was not detected. Either ICW bit 3.2 (tag bit) did not turn on after going off, or it did not go off (SDF shifting).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X10	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0048'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X12	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to BSC Transmit state transition 60, 60, 67, 61, and 33.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X14	E2E2	TF80X	F-570
		E2B2	TF81X	F-580

		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition (forced state).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X15	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X16	E3K2	TE24X	F-360
		E3L2	TE40X	
		E3Q2	TE52X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KE) is installed:
E3N2 (TE35X) is also a possible failing card.

An ETX should have been decoded during a cycle steal fetch operation.

The expected results are: ICW bit 6.4 (end character decoded) set and ICW bit 6.5 (cycle steal valid) reset.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X17	E2J2	TF50X	F-380
		E3Q2	TE52X	F-390

The PDF array pointer (ICW byte 12) was not correct. The expected value in ICW byte 12 is X'9X'. If register X'4E' byte 0 contains X'7X', data character X'26' (EBCDIC ETB) decoded as an ASCII ending character. If register X'4E' byte 0 contains X'8X', data character X'2D' (EBCDIC ENQ) decoded as an ASCII ending character.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X20	E2E2	TF80X	F-410
		E2B2	TF81X	F-420
		E2H2	TF42X	
		E2J2	TF50X	

A transmit tag was not detected. Either ICW bit 3.2 (tag bit) did not turn on after being turned off, or it never turned off (SDF shifting)

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X21	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X23	E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

An unexpected L2 interrupt occurred. ICW bit 0.4 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X24	E2E2	TF80X	F-570
	E2P2	TF82X	
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 off. Refer to BSC Transmit state transition 18 and 56.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X25	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0032'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X26	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition (forced state).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A 0X27	E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X28	E3K2	TE24X	F-360
		E3L2	TE40X	
		E3Q2	TE52X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

An ENQ should have been decoded during a cycle steal fetch operation.

The expected results are: ICW bit 6.4 (end character decoded) on and ICW bit 6.5 (cycle steal valid) off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X29	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X30	E2B2	TF81X	F-210
		E2Q2	TF34X	
		E2P2	TF82X	

ICW bit 5.4 (transparent mode) should have been set on.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X31	E2N2	TF22X	F-230
		E3K2	TE24X	
		E2P2	TF82X	
		E3D2	TE34X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

ICW bit 6.5 (cycle steal valid) should have been set on.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X33	E2E2	TF80X	F-410
		E2B2	TF81X	F-420
		E2H2	TF42X	
		E2J2	TF50X	

A transmit tag was not detected. Either ICW bit 3.2 (tag bit) did not turn on after being turned off or it did not turn off (SDF shifting).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X34	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X35	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0048'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X36	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to BSC Transmit state transition 60, 60, 67, 61, and 33.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77A	0X37	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

X77B BSC Transmit - EP - EBCDIC LCD=4

ROUTINE DESCRIPTION

This routine sets up a transmit ICW and transmits a string of characters without using the cycle steal mechanism. The characters in the data stream are arranged to cause specific state transitions and status bit posting. The state transitions and status posting is verified for correct operation. Receive functions are not used in this routine (transmit only). Cycle steal is not used. Diag 0=1 (scanner wrap) used for transmit line.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X02	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4 and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X04	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	
		E2P2	TF82X	

The status posted in the transmit line ICW was expected to be X'0060'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X06	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0020'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X07	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC field of the transmit ICW should have been reset to X'0000'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X08	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X0A	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	
		E2K2	TF44X	

The status posted in the transmit line ICW was expected to be X'000C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X0B	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X0D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'001C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X0E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/3, 13.0 off prior to this test. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X0F	B2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'001E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/3, 13.0 off prior to this test. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X11	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'001A'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X12	E2E2	TF80X	F-570
		E2B2	TF81X	F-580

	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/3, 13.0 off prior to this test. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B 0X13	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	
	E2P2	TF82X	

The status posted in the transmit line ICW was expected to be X'009C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B 0X14	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. The program forced state 9/4, 13.0 off piror to this test. Refer to BSC Transmit state transition 25 and 52.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B 0X17	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 14. Looks for state 9/4 with sequence bit off, state 14A if RPQ EH4100 installed.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B 0X10	E2D2	TF82X	F-150
	E2N2	TF22X	F-210
	E2B2	TF81X	F-240
	E2E2	TF80X	
	E2F2	TF40X	
	E2Q2	TF34X	

THIS STOP SHOULD NOT OCCUR IF RPQ EH4100 IS INSTALLED.

The status posted in the transmit line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B 0X19	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 15. Looks for state 9/4 with sequence bit off, state 15A if RPQ EH4100 installed.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B 0X1A	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B 0X1B	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X1C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 17.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X1D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0014'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X1E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 18.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X1F	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0012'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0

0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X20	E2C2	TF60X	
		E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X21	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 20.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X22	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 75.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X23	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'000E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6

0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X24	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

THIS STOP SHOULD NOT OCCUR IF RPQ EH4100 IS INSTALLED.

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X25	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

THIS STOP SHOULD NOT OCCUR IF RPQ EH4100 IS INSTALLED.

The status posted in the transmit line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X41	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

THIS STOP OCCURS ONLY IF RPQ EH4100 IS INSTALLED.

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Receive State transition 30a.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC transmit state transition 75.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X27	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0098'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X28	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 78.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X29	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF is in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X2A	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 underfined. The program forces state 9/2, 13.0 off prior to this test. Refer to BSC transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X2B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 76.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X2C	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0060'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X30	E2B2	TF81X	F-210
		E2Q2	TF34X	
		E2P2	TF82X	

ICW bit 5.4 (transparent mode) should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X31	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced state 9/3, 13.0 off prior to this test. Refer to BSC Transmit state transition 70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X32	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X33	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0040'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X34	E2B2	TF81X	F-210
		E2Q2	TF34X	
		E2P2	TF82X	

ICW bit 5.4 (transparent mode) should have been set on. Refer to BSC Transmit state transition 70.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X35	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 67 and 80.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X36	E2Q2	TF34X	F-410
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E2P2	TF82X	

The transmit line SDF should contain X'012D'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77B	0X37	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'4006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X77B 0X41 SEE ERROR STOP AFTER 0X25

X77C BSC Transmit - EP - USASCII LCD=5

ROUTINE DESCRIPTION

This routine sets up a transmit ICW and transmits a string of characters without using the cycle steal mechanism. The characters in the data stream are arranged to cause specific state transitions and status bit posting. The state transitions and status posting is verified for correct operation. Receive functions are not used in this routine (transmit only). Cycle steal is not used. Diag 0=1 (scanner wrap) used for transmit line.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C 0X02	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/0 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C 0X03	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C 0X04	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/1 with sequence bit 13.0 on. Refer to BSC Transmit state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X77C	0X05	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/1 with sequence bit 13.0 off. Refer to BSC Transmit state transition 3.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X07	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0155'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X08	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 on. Refer to BSC Transmit state transition 4.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X09	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0116'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X77C	0X0B	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0116'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X11	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0060'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X12	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X13	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0020'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X14	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X15	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X16	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'000C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X17	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C 0X18	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C 0X19	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'001C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C 0X20	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/3, 13.0 off prior to this test. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C 0X21	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'001E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6

0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X22	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/3, 13.0 off prior to this test. Refer to BSC Transmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X23	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'001A'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X24	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/3, 13.0 off prior to this test. Refer to BSC Trahsmit state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X25	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'009C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2

0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 25 and 52.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X27	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

If RPQ EH4100 is installed, the routine expects PCF/EPCF 9/4. Refer to BSC Transmit state transition 14A.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X28	E2P2	TF82X	F-150
		E2N2	TF22X	F-210
		E2B2	TF81X	F-240
		E2E2	TF80X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'. The routine should not stop at this error if RPQ EH4100 is installed.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X29	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequenco bit (bit 1.0).

The routine looks for PCF/EPCF to be 9/4 with sequence bit 13.0 off if RPQ EH4100 is installed. Refer to BSC Transmit State transition 15A.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X30	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'. The routine should not stop at this error if RPQ EH4100 is installed.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X31	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X32	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 17.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X33	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0014'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X34	E2C2	TF60X	
		E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 18.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X35	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF8QX	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0012'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X36	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X37	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 20.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X38	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 75.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X39	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'000E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X40	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The routine should not stop at this error stop if RPQ EH4100 is installed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X41	E2N2	TF81X	F-150
		E2B2	TF81X	F-240
		E2E2	TF80X	F-210
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'. The routine should not stop with this error code if RPQ EH4100 is installed.

Reg X'15' Bits	Description	ICW Bits

0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X50	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The routine will only stop at this error stop if RPQ EH4100 is installed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM CODE	LOCATION	PAGENO
X77C	0X42	E2E2	TF80X	F-570 E2B2	TF81X	F-580 E2K2
		TF44X	F-600 E2R2	TF32X E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 75.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

Program forced state 9/2, 13.0 off prior to making this test.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X43	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0098'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X44	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X45 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 76.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X46 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0060'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X4A E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced state 9/3, 13.0 off prior to this test. Refer to BSC Transmit state transition 70.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X4B E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X4C E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0040'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X4D	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 67 and 80.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X4E	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0185'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X4F	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'4006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77C	0X50	SEE ERROR STOP AFTER 0X41		

X77D BSC ASCII Transmit Misc. Conditions Not EP LCD=D

ROUTINE DESCRIPTION

This routine checks the following conditions: (1) ASCII lending SYN insertion, (2) ASCII STX insertion, (3) ITB in data while in ASCII not - Transparent state and BCC insertion (4) ITB in data while in ASCII Transparent state and (5) Time-out while in ASCII Transparent text. Cycle steal is used in this routine. Receive functions are not used (transmit only). Diag 0=1 (scanner wrap) used for transmit line.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X02	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4 and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X03	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0116'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X05	E3D2	TE34X	F-410
		E2E2	TF80X	
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 29 and 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X07	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'011F'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X08	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X09	E2B2	TF81X	F-410
		E2L2	TF46X	
		E2P2	TF82X	

The transmit line SDF should contain X'012F'. The incorrect SDF data is contained in Register X'15' (bits 0.6-1.7). Register X'11' is the address of the line under test.

Check input X'4A' (ICW byte '11') for correct byte. If the byte in the ICW is correct, the BCC to SDF shift was not correct. Otherwise, the BCC accumulation is in error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Transmit state transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X0B	E2B2	TF81X	F-410
		E2C2	TF60X	

		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 59.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X0D	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Transmit state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X0E	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 66.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X10	E2P2	TF82X	F-410
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D	0X11	E2C2	TF60X	F-580
		E2J2	TF50X	F-590

E2B2	TF81X	
E2K2	TF44X	
E2R2	TF32X	

The PCF/EPCF should be 9/8 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 59 and 71.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D 0X12	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D 0X13	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 48.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D 0X14	E2C2	TF60X	F-210
	E2B2	TF81X	
	E2V2	TF41X	

The BSC time out count was not reset for 1 sec timeout. ICW bits 4.2, 4.3 and 4.7 should be on and bits 4.4 and 5.0 should be off. Reg X'15' displays error bits from input X'47'.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77D 0X15	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0116'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

X77E BSC Receive Time-Out Test LCD=C BSC Not EP EBCDIC

ROUTINE DESCRIPTION

This routine tests the operation of time-out while in receive states (PCF/EPCF) 7/2, 7/4 and 7/8. The state transition flow is: 78, 79, 80, 81 and 82. Cycle steal, transmit and receive functions are used in this test. The transmit and the receive line are put in scanner wrap mode (Diag 0=1). The transmit line has Diag 1=1 (PCF/EPCF=9/C) for this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X03	E2C2	TF60X	F-580
		E2J2	TF50X	F-600
		E2B2	TF81X	
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 78.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X04	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 78. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X05	E3K2	TE24X	F-150
		E2N2	TF22X	F-210
		E2B2	TF81X	F-240
		E2E2	TF80X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X06	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. The program forced state 7/4, 13.0 on prior to this test. Refer to BSC Receive state transition 79.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X07	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 79. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X08	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X09	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. The program forced state 7/4, 13.0 off prior to this test. Refer to BSC Receive state transition 80.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X0A	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transtion 80. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X0B	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X0C	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. The program forced state 7/8, 13.0 on prior to this test. Refer to BSC Receive state transition 81.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X0D	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 81. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X0E	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X0F E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. The program forced state 7/8, 13.0 off prior to this test. Refer to BSC Receive state transition 82.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X10 E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 82. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X11 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X20 E2B2	TF81X	F-480
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The receive line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77E	0X21 E2C2	TF60X	F-210
	E2S2	TF21X	
	E2B2	TF81X	
	E2J2	TF50X	
	E3S2	TE50X	
	E2V2	TF41X	

The BSC timeout counter has the wrong value; the counter should have incremented. Register X'15' byte 0 contains the counter value; byte 1 contains the expected value.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X77E 0X22 B3L2 CP006 6-090
CP007

No level 3 interrupt occurred from the interval timer.

X77F BSC Transmit - Initial Status 0 EBCDIC - Not EP LCD=C

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with initial status 0 and verifies that for each final status, the correct ending characters are inserted in the SDF. Cycle Steal is not used. Receive functions are not used in this routine (transmit only). Diag 0=1 (scanner wrap) is used for transmit line.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A setmode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No setmode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F 0X0A	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F 0X0B	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F 0X0C	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 13.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F 0X0D	E2B2	TF81X	F-410
	E2C2	TF60X	

		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C1'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X77F	0X10 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X77F	0X11 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'012D'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X77F	0X20 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	
	E2Q3	TF34X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X77F	0X21 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X77F	0X22 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO

X77F	0X23	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0170'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X30	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE		CARD LOCATION	FEALD PAGEN	FETMM 0	PAGENO
X77F	0X31	E2B2	TF81X	F-410	
		E2C2	TF60X		
		E2H2	TF42X		
		E3J2	TE22X		

The transmit line SDF should contain X'013D'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X40	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X41	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X42	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X77F	0X43	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'017C'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X77F 0X50	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	LOCATION	CARD PAGENO	FEALD PAGENO	FETMM
X77F 0X51	E2B2	TF81X	F-410	
	E2C2	TF60X		
	E2H2	TF42X		
	E3J2	TE22X		

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F 0X52	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F 0X53	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0161'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F 0X60	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X61	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X62	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X63	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'016B'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X70	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 53.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X71	E2Q2	TF34X	F-410
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	
		E2F2	TF48X	
		E2P2	TF82X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X72	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	
		E2P2	TF82X	

The status posted in the transmit line ICW was expected to be X'40FF'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X73	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 37.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X74	E2P2	TF82X	F-410
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'012D'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X77F	0X75	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'4006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X780 BSC Transmit - Initial Status 1 EBCDIC - Not EP LCD=C

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with Initial status 1 and verifies that for each final status, the correct beginning and ending control characters are inserted in the SDF. Neither cycle steal nor receive functions are used. (Transmit only). Diag 0=1 (scanner wrap) is used for transmit line.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780 0X0B	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, 5, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780 0X0C	E2E2	TF80X	F-410
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780 0X0D	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780 0X0E	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'012D'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780 0X0F	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590

		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced state 9/2, 13.0 ofr prior to this test. Refer to BSC Transmit state transition 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X10	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X12	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'011F'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 33 and 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X15	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC field of the transmit line ICW should have reset to zero.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X16	E2B2	TF81X	F-410
		E2C2	TF60X	

		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C2'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X18	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X20	E2C2	TF60X	
		E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X21	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 33 and 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X23	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C2'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X780	0X24	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X25	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0126'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X28	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 33 and 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X29	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0143'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X2C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X2D E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X30 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced state 9/4, 13.0 off prior to this test. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X31 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 33 and 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X32 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0143'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X33 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X780	0X34 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0126'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

X781 BSC Transmit Test - Initial Status 2 EBCDIC - Not EP LCD=C

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with initial status 2 and verifies that for each final status, the correct control characters are inserted in the SDF. Neither Cycle Steal nor receive functions are tested. Diag 0=1 (scanner wrap) is used for transmit line.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781	0X0B	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781	0X0C	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 49.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781	0X0D	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781 0X0E	E2K2	TF44X	F-590
	E2B2	TF81X	F-580
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF shoul ! be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781 0X0F	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781 0X10	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781 0X11	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01C1'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781 0X12	E2P2	TF82X	
	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781 0X13	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is cqntained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781	0X14	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X781	0X15	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'012D'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

X782 BSC Transmit Test - Initial Status 3; Not EP EBCDIC LCD=C

ROUTINE DESCRIPTION

This routine sets up a transmit line ICW with initial status 3 and verifies that for each final status, the correct beginning and ending control. Neither cycle steal nor receive functions are used in this routine (transmit only). Diag 0=1 (scanner wrap) is used for the transmit line.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, 5, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X0C	E2E2	TF80X	F-410
		E2B2	TF81X	
		E2P2	TF82X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0101'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X0D	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X0E	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'012D'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/2 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X10	E2E2	TF80X	F-410
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0101'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X12	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'011F'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 33 and 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X15	E2L2	TF46X	F-230
		E2B2	TF81X	
		E2P2	TF82X	

The BCC field of the transmit line ICW should have reset to zero.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X16	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C2'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X18	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X20	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X21 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 33 and 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X23 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01C2'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X24 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X25 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0126'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X26 E2C2	TF60X	
	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X28 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590

E2R2	TF32X	
E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 33 and 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X29	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0143'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X2C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X2D	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0103'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X30	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X31	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 33 and 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X32 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0143'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X33 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X782	0X34 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0126'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

X783 BSC Transmit Test - Initial Status 4 EBCDIC - Not EP LCD=C

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with initial status 4 and verifies that for each final status, the correct beginning and ending control characters are inserted in the SDF. Receive functions are not used in this routine (transmit only). Cycle steal is used. Diag 0=1 (scanner wrap) is used for the transmit line.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X0A E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X0B E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0132'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X0C E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 43.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X0D E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0137'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X0E E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Refer to BSC Transmit state transition 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X0F E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0175'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X10 E2Q2	TF34X	
	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 36.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X11	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X12	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X13	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0137'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X14	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Refer to BSC Transmit state transition 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X783	0X15	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0175'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

X784 BSC Transmit - Initial Status 0 USASCII - Not EP LCD=D

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with initial status 0 and verifies that for each final status, the correct ending characters are inserted in the SDF. Cycle Steal is not used. Receive functions are not used in this routine (Transmit only). Diag 0=1 (Scanner wrap) for transmit line.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550

E2J2	TF50X	
E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 13.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X0D	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C1'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X11	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0185'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X20 E2B2	TF80X	F-570
	B2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. The program forced PCF/EPCF state 9/2 13.0 off prior to this test. Refer to BSC Transmit state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X21 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	B3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X22 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X23 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	B3J2	TE22X	

The transmit line SDF should contain X'01B0'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X30 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/2 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X31 E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	B3J2	TE22X	

The transmit line SDF should contain X'0115'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784 0X40	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. The program forced PCF/EPCF state 9/2 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 36.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784 0X41	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784 0X42	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784 0X43	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01BC'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784 0X50	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. The program forced PCF/EPCF state 9/2 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784 0X51	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X52	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X53	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0131'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X60	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. The program forced PCF/EPCF state 9/2 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X61	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X62	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/2 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X63	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'013B'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X70	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/2, 13.0 off prior to this test. Refer to BSC Transmit state transition 53.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X784	0X71	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in Register X'15', (bits 0.6-1.7).

X785 BSC Transmit - Initial Status 1 USASCII - Not EP LCD=D

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with Initial Status 1 and verifies that for each final status, the correct beginning and ending Control Characters are inserted in the SDF. Neither cycle steal nor receive functions are used in this routine (Transmit only). Diag 0=1 (Scanner wrap) for transmit line.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, 5 and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X0C	E2E2	TF80X	F-410
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X0D	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X0E	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0185'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X10	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 29 and 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X12	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'011F'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X14	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'011A'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X15	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC field of the transmit line ICW should have reset to zero.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X16	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C2'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X18	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0183'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X785	0X20	E2C2	TF60X	
		E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 29 and 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785 0X21	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785 0X22	E2E2	TF80X	F-410
	E2B2	TF81X	
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The transmit line SDF should contain X'015B'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785 0X23	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01C2'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785 0X24	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785 0X25	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0197'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 29 and 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X28	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X29	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0183'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X2C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X2D	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0183'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X30	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 29 and 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X31	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X32	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0197'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X33	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X785	0X34	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0197'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

X786 BSC Transmit Test - Initial Status 2 USASCII - Not EP LCD=6

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with initial status 2 and verifies that for each final status, the correct control characters are inserted in the SDF. Cycle Steal is used. Receive functions are not used in this routine (Transmit only). Diag 0=1 (Scanner wrap) for transmit line.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14'

not equal to Reg X'11'.
0003 Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X02	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4 and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X03	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0116'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X04	E2J2	TF50	F-580
		E2B2	TF81X	F-580
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 9/3 with sequence bit 13.0 undefined. Refer to BSC Transmit state transition 49.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X05	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X07	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0102'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X08	E2E2	TF80X	F-410
		E2B2	TF81X	
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C1'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X09	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0141'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X0A	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X0B	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0100'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 60, 60, 60, 60 and 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X12	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X13	E2B2	TF81X	F-230
	E2L2	TF46X	
	E2P2	TF82X	

The transmit line BCC field should be X'71FF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X14	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X15	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0185'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7)

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X1A	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X1B	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01C1'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X1C	E2E2	TF80X	F-570
	E2B2	TF81X	F-580

	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X1D E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X1E E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 61.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X1F E2B2	TF81X	F-410
	E2E2	TF80X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'011F'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X24 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786	0X25 E2C2	TF60X	F-410
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01C1'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X786	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X27	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X28	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X29	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0183'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X2E	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 60.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X2F	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'01C1'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X786	0X30	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X31	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X33	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X786 0X34	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0197'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

X787 BSC Transmit Test - Initial Status 3 USASCII - Not EP LCD=D

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with initial status 3 and verifies that for each final status, the correct beginning and ending control characters are inserted in the SDF. Neither cycle steal nor receive functions are tested. Diag 0=1 (Scanner wrap) for transmit line.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X787	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, 5, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787 0X0C	E2E2	TF80X	F-410
	E2B2	TF81X	
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0101'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787 0X0D	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787 0X0E	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0185'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787 0X0F	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. The Program forced PCF/EPCF state 9/2 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787 0X10	E2B2	TF81X	F-410
	E2C2	TF60X	
	E2H2	TF42X	
	E3J2	TE22X	

The transmit line SDF should contain X'0101'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X12	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'011F'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X14	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'011A'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X15	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC field of the transmit line ICW should have reset to zero.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X16	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C2'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590

		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X18	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0183'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X19	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 off. Refer to BSC Transmit state transition 56.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X1A	E2H2	TF42X	F-210
		E2L2	TF46X	F-230
		E2P2	TF82X	

The BCC was loaded into register X'14' via an input X'4A'. The BCC shifted into the SDF and the SDF was compared to the value in register X'14'. The actual SDF data is contained in Register X'15'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X20	E2C2	TF60X	
		E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X21	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X787	0X22	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'015B'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X23	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01C2'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X24	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X25	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0197'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X28	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X787	0X29	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0183'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X2C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X2D	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0183'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X30	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 9/4 with sequence bit 13.0 off prior to this change. Refer to BSC Transmit state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X31	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X32	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0197'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X787	0X33	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X34	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0197'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X35	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 off. Refer to BSC Transmit state transition 56.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X787	0X36	E2H2	TF42X	F-210
		E2L2	TF46X	F-230
		E2P2	TF82X	

The BCC was loaded into register X'14' via an input X'4A'. The BCC shifted to the SDF and the SDF was compared to the value in register X'14'. The actual SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

X788 BSC Transmit Test - Initial Status 4 USASCII - Not EP LCD=D

ROUTINE DESCRIPTION

This routine sets up a transmit ICW with initial status 4 and verifies that for each final status, the correct beginning and ending control characters are inserted in the SDF. Cycle Steal is used. Receive functions are not tested in this routine (Transmit only). Diag 0=1 (Scanner wrap) for transmit line.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X01	E3P2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580

		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, and 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X0B	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0116'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 43.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X0D	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0104'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X0E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Refer to BSC Transmit state transition 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X0F	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580

	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 on. Refer to BSC Transmit state transition 36.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X11	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0110'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X12	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X13	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0104'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X14	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Refer to BSC Transmit state transition 28.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X788	0X15	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01FF'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7)

X789 BSC Receive - EP - EBCDIC LCD=4

ROUTINE DESCRIPTION

This routine test the control character handling circuits in scanner. The transmit line ICW has bit 5.6 set on to prevent modification of the data stream. The receive line is checked to see that proper status bits are posted for control characters received; and to verify that correct control characters are stripped from the data stream. This routine uses Diag 0=1 (Scanner Wrap) and the transmit line uses Diag 1=1 (PCF/EPCF =9/C). Cycle Steal is used by both lines.

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) and E3D2 (TE34X) could also be possible failing cards at all error stops except 0X01,0X02,0X04,0X08 and 0X09.

This routine does not run if RPQ EH4100 is installed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 off. Refer to BSC Receive state transition 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 2 and 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X06	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X07	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X08	E2E2	TF80X	F-560
		E2F2	TF48X	F-240

ICW 0.4 (not L2 bid) should be on. ICW 13.3 (sequence bit 2) should be off. Register X'15' (bits 0.4 and 1.3) indicate bit/s in error. Refer to BSC Receive State Transition 56.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X09	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X0A	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 43 and 16.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X0C	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X0D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4201'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4

0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X0E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	
		E2Q2	TF34X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 18.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X10	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'420B'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The Program forced PCF/EPCF state 7/3 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X789	0X12	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X13	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 undefined. The Program forced PCF/EPCF state 7/3 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X14	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X15	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The Program forced PCF/EPCF state 7/3 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X16	32N2	TF22X	F-150
		32B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001A'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. The Program forced PCF/EPCF state 7/2 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X18	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 24.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X19	32N2	TF22X	F-150
		32B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0088'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6

0.7	Length Check 14.7
1.0-1.7	ICW byte 15 15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X1A E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The Progras forced PCF/EPCF state 7/3 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 36.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X1B E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'020F'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X1C E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The Progras forced PCF/EPCF state 5/1 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X1D E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2

0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X1E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The program forced PCF/EPCF state 5/1 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X1F	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0008'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X20	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The Program forced PCF/EPCF state 7/2 with sequence bit 13.0 undefined prior to this change. Refer to BSC Receive state transition 35.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X21	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X22	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. The Program forced PCF/EPCF state 7/2 with Sequence bit 13.0 undefined prior to this change. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X23	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 37.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X24	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 59.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X25	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'020E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X26 E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

An L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 59. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'13').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X27 E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

An L2 interrupt was expected from the transmit line because the cycle steal byte count went to zero. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X789	0X28 E3K2	TE24X	F-480
	E2C2	TF60X	
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X78A BSC Receive Test - EP Mode
USASCII Control Characters, LCD=5

ROUTINE DESCRIPTION

This routine tests BSC Receive control character deletion via the scanner internal wrap capability. Two ICW's are selected; one serves as a transmit line set in diagnostic mode with bit 5.6 on. The other line set in diagnostic mode views the wrapped data and deletes control characters. This routine looks for USASCII control characters. This routine uses Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

This routine does not run if RPQ EH4100 installed.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X01 E3F2	TF20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X02 E3F2	TF20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 off. Refer to BSC Receive state transition 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X07	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2P2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X08	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X09	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X0A	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 43, 43, 16, 43, 43, and 43.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X0B	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X0D	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X0E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 18.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X78A	0X10	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'420B'.

The status bits i error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The program forced PCF/EPCF state 7/3 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X12	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The program forced PCF/EPCF state 7/3 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X14	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X15	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The program forced PCF/EPCF state 7/3 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X16	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001A'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. The program forced PCF/EPCF state 7/2 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X18	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 24.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X19	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0088'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X1A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The program forced PCF/EPCF state 7/3 prior to this change. Refer to BSC Receive state transition 36.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X1B	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'020E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3

0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X1C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The program forced PCF/EPCF state 5/1 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X1D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X1E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The program forced PCF/EPCF state 5/1 with sequence bit 13.0 off prior to this test. Refer to BSC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X1F	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0008'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X20	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. The program forced PCF/EPCF state 7/2 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 35.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X21	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X22	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. The program forced PCF/EPCF state 7/2 prior to this test. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X23	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 37.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X24	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 59.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X25	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'020E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X26	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 59. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'13').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X27	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line. The byte count went to zero. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78A	0X28	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X78B BSC Receive - EP EBCDIC LCD=4

ROUTINE DESCRIPTION

This routine is a continuation of routine X789, and test LCD 4. This routine uses Diag 0=1 (Scanner wrap) and the transmit line used Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X02 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X03 E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 2, 14, and 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X04 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X78B	0X05	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC field of the receive line ICW should have reset to zero.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X07	E2P2	TF82X	F-210
		E2B2	TF81X	
		E2Q2	TF34X	

ICW bit 5.4 (transparent mode) should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X08	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4260'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X0B	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0014'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 7/4 with sequence bit 13.0 off prior to this change. Refer to BSC Receive state transition 10 and 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0)

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X0D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0012',

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X0E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. The program forced PCF/EPCF state 7/4 with sequence bit 13.0 off prior to this test. Refer to BSC Receive state transition 10 and 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X0F	E2N2	TF22X	F-150
		E2B2	TF81X	F-210

E2E2	TF80X	F-240
E2F2	TF48X	
E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0002'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X10	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 13.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X12	E2E2	TF80X	F-570
		E2F2	TF48X	
		E2G2	TF40X	

ICW bit 13.3 should have been set on.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 39 and 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X78B	0X14	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B 0X15	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B 0X16	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B 0X17	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 58.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	
X78B 0X18	E2N2	TF22X	F-150	F-150
	E2B2	TF81X	F-210	
	E2E2	TF80X	F-240	
	E2F2	TF48X		
	E2Q2	TF34X		

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B 0X19	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. The program forced PCF/EPCF state 7/4 with sequence bit 13.0 off prior to this test. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B 0X1A	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 57.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B 0X1B	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B 0X1C	E2P2	TF82X	F-570
	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. The program forced PCF/EPCF state 7/4 with sequence bit 13.0 off prior to this test. Refer to BSC Receive state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X1D E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X1E E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Refer to BSC Receive state transition 63.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78B	0X1F E3K2	TE24X	F-480
	E2C2	TF60X	
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X78C BSC Receive - EP, USASCII, LCD=5

ROUTINE DESCRIPTION

This routine is a continuation of routine X789. This routine uses Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X78C	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X03	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 2, 14, and 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X05	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC field of the receive line ICW should have reset to zero.

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X07	E2B2	TF81X	F-210
		E2Q2	TF34X	

ICW bit 5.4 should have been set off.

ERROR CODE		CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X08	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4260'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0

0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X09		
	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X0A		
	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X0B		
	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0014'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X0C		
	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Program forced state 7/4, 13.0 off. Refer to BSC Receive state transition 10 and 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X0D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0012'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X0E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Program forced state 7/4, 13.0 off. Refer to BSC Receive state transition 10 and 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 12.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X10	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0002'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6

	0.7	Length Check	14.7
	1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X12	E2F2	TF48X	F-240
		E2E2	TF80X	
		E2G2	TF40X	

ICW bit 13.3 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X14	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

An L2 interrupt was expected from the receive line. Refer to BSC Receive Transition 21. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X15	E2N2	TF22X	F-160
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C 0X16	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C 0X17	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 58.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C 0X27	E2E2	TF80X	
	E2G2	TF40X	

ICW bit 13.1 was expected to be on.

This error stop is possible only when RPQ EH4100 is installed.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C 0X18	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C06'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C 0X19	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X1A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 57.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X2A	E2E2	TF80X
		E2G2	TE40X

ICW bit 13.1 was expected to be on.

This error stop is possible only when RPQ EH4100 is installed.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X1B	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C06'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X1C	E2P2	TF82X	F-570
		E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Program forced state 7/4, 13.0 off. Refer to BSC Receive state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X1D	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Program forced state 7/4, 13.0 on. Refer to BSC Receive state transition 63.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X1E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (with bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78C	0X1F	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X78C 0X27 See error stop after 0X17.

X78C 0X2A See error stop after 0X1A.

X78D BSC Receive 'STICK' Characters With Bad BCC - EBCDIC EP LCD=4

ROUTINE DESCRIPTION

This routine verifies that when a receive line detects a 'STICK' character, the scanner sequences through the correct state transmitions and that incorrect BCC characters cause level 2 interrupts. This routine uses Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X03	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 2, 14, and 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 17.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X05	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000A'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Program forced state 7/4, 13.0 off. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X78D	0X07	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 7/2, 13.0 off. Refer to BSC Receive state transition 30 and 18.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X08	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000A'.

The status bits in error are in Register X'15'. The routine should not stop with this error code if RPQ EH4100 is installed.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Program forced state 7/4, 13.0 off. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 51.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X0D	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected. Refer to BSC Receive state transition 39. The interrupt did not occur (Register X'14' equal Zero).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X0E	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. The interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78D	0X0F	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1402'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

X78E BSC Transparency Receive - EP EBCDIC, Bit 5.4 on, LCD=4.

ROUTINE DESCRIPTION

This routine checks for correct control character deletion in transparency receive mode. No control characters should be removed from the data stream. This routine uses Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 22 and 8.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590

E2R2	TF32X	
E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X07	E2P2	TF82X	F-570
		E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 off. Refer to BSC Receive state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X08	E2C2	TF60X	F-210
		E2B2	TF81X	
		E2V2	TF41X	

The BSC time-out counter was not set for 3 second timeout as expected.

Refer to BSC Receive state transition 74. ICW 4.2, 4.4, 4.7 and 5.0 should be off and 4.3 should be on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 75.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 off. Refer to BSC Receive state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X0D	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 77.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X15	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0)

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X16	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X17	E2F2	TF48X	F-240
		E2E2	TF80X	
		E2G2	TF40X	

ICW bit 13.3 should have been set on. Refer to BSC receive state 13.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X18	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

An L2 interrupt was expected from the receive line. Refer to BSC receive state 21. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X19	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0442'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X20 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X21 E2B2	TF81X	F-210
	E2Q2	TF34X	

ICW bit 5.4 should have been set off. Refer to BSC receive state 21.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X22 E2L2	TF46X	F-230
	E2B2	TF81X	
	E2P2	TF82X	

The BCC (Input X'4A') was not reset to X'0000' as expected. Register X'15' contains the bits in error. Refer to BSC Receive state transition 21.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X23 E2F2	TF48X	F-240
	E2E2	TF80X	
	E2G2	TF40X	

ICW bit 13.3 should have been set off. Refer to BSC receive state 21.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X24 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X25 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 9.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X26	E2B2	TF81X	F-210
		E2Q2	TF34X	

ICW bit 5.4 (transparency) was not set as expected for a DLE/STX received.

Refer to BSC Receive state transition 10 and 9.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X27	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X28	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 71.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X29	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 73.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The routine expects PCF/EPCF state 7/4 with sequence bit 13.0 off if RPQ Eh4100 is installed. Refer to BSC Receive state transition xx.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X30	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C06'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2

0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X31	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

An L2 interrupt was expected from the receive line. Receive byte count went to zero. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78E	0X32	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X78F BSC Not Transparency Receive; EP USASCII - LCD = 6, Bit 5.4 Off

ROUTINE DESCRIPTION

This routine checks transmit and receive for BCC accumulation and no data checks on the receive end. This routine uses Diag 0=1 (scanner wrap). Cycle Steal is used by both lines.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
8F	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 12, 5, 72, 29, and 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X04	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC should be X'D305' for BSC transmit.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 on. Refer to BSC Transmit state transition 38.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X06	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'0105'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7). The first BCC character should be in the SDF.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X07	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/6 with sequence bit 13.0 off. Refer to BSC Transmit state transition 39.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X08	E2B2	TF81X	F-410
		E2C2	TF60X	
		E2H2	TF42X	
		E3J2	TE22X	

The transmit line SDF should contain X'01D3'. The incorrect SDF data is contained in Register X'15', (bits 0.6 thru 1.7). The second BCC character should be in the SDF.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X78F	0X09	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0032'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X0A	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 2, 14, 25, 26, 51, 47, and 53.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X0B	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0432'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X78F	0X1E	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X790 NCP BSC Receive EBCDIC, LCD = C

ROUTINE DESCRIPTION

This routine tests BSC receive control character deletion via the scanner internal wrap capability. The routine operates in NCP mode and looks for EBCDIC control characters. This routine uses Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

This routine does not run if RPQ EH4100 is installed.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790 0X01	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790 0X02	E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790 0X03	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790 0X04	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-600
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 off. Refer to BSC Receive state transition 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X790	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X07	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	Q.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X08	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X09	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X0A	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 43, 43, 16, 43, 43, and 43.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X0C	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X0D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4201'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6

0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X0E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 18.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X10	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000A'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0)

The program forced state 7/3 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X790	0X12	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X13		
	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off, Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/3 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X14		
	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'y001C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X15		
	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/3 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X16 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X17 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/3 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X18 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X19 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/3 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X20	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X21	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/3 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X22	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001A'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X790	0X23	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/2 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X24	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 24.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X25	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0088'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 36.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/3 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X27	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'020E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X28 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 5/1 with sequence bit 13.0 off prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X29 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X30 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 5.1 with sequence bit 13.0 off prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X790	0X31	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0008'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X32	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 35.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

Program forced state 7/2 prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X33	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X34	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/2 proir to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X35 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 37.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X36 E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 59.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X37 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'020E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X38 E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'13').

Refer to BSC Receive state transition 59.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X39 E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

A L2 interrupt was expected from the transmit line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

The interrupt occurred because the transmit byte count went to zero.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X790	0X40	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X791 BSC Receive - Not EP, USASCII, LCD = D

ROUTINE DESCRIPTION

This routine tests the control character handling circuits in the communication scanner. The transmit line has bit 5.6 set on to prevent modification of the data stream.

The receive line is checked to see that proper status bits are posted for control characters received; and to verify that correct control characters are stripped from the data stream. This routine uses Diag 0=1 (scanner wrap) and the receive line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

This routine does not run if RPQ EH4100 in installed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 on. Refer to BSC Receive state transition 2.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 5, 2, and 14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X05	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X06	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-600
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive state transition 6.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X07	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X08	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X09	E2N2	TF22X	F-560
		E2B2	TF81X	

ICW 0.4 (not L2 bid) should be off and 0.1 (service request) should be on. Register X'15' contains the bits in error.

Refer to BSC Receive state transition 15.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X0A	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X0B	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 7.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 43, 43, 16, 43....30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X0D	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 31.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X11	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4201'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791 0X12	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791 0X13	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 18.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791 0X14	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'420B'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791 0X15	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 7/3 before this test. Refer to BSC Receive state transition 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X16 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001C'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X17 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 7/3 before this test. Refer to BSC Receive state transition 49 and 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X18 E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X19 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 7/3 before this test. Refer to BSC Receive state transition 49 and 23.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X1A	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'001A'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X1B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Program forced state 7/2 before this test. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X1C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 11 and 24.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X1D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0088'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits

0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X1E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 7/3 before this test. Refer to BSC Receive state transition 36.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X1F	E2N2	TF80X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'020E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X20	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 5/1, 13.0 off before this test. Refer to BSC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X21	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X22	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 5/1, 13.0 off before this test. Refer to BSC Receive state transition 34.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X23	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0008'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X24	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 7/2 before this test. Refer to BSC Receive state transition 35.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X25	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'000E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X'791'	0X26	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 on. Program forced state 7/2 before this test. Refer to BSC Receive state transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X'791'	0X27	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 37.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X'791'	0X28	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 59.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X'791'	0X29	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'060E'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1

0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X2A E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

An L2 interrupt was expected from the receive line. Refer to BSC receive state 59. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X2B E2E2	TF80X	F-550
	E2F2	TF48X	F-560
	E3L2	TE40X	

An L2 interrupt was expected from the transmit line. Byte count went to zero. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'13').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X791	0X2C E3K2	TE24X	F-480
	E2C2	TF60X	
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X792 BSC Receive - NCP EBCDIC LCD=C

ROUTINE DESCRIPTION

This routine tests the control character handling circuits in the type 3 communications scanner in NCP mode. The transmit line has bit 5.6 set on to prevent modification fo the transmit data stream.

The receive line is checked to see that proper status bits are posted for control characters received and to verify that correct state transitions occur. The data received is checked to verify that correct control characters are stripped from the received data. This routine uses Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X03	E2J2	TF50X	F-580
		E2B2	TF81X	F-600
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 2, 14, and 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X04	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X05	E2B2	TF81X	F-230
	E2L2	TF46X	
	E2P2	TF82X	

The BCC field of the receive line ICW should have reset to zero. Refer to BSC receive state 34.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X06	E2F2	TF48X	F-240
	E2E2	TF80X	
	E2G2	TF40X	

ICW bit 13.3 should have been set on. Refer to BSC receive state 14.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X07	E2Q2	TF34X	F-210
	E2B2	TF81X	

ICW bit 5.4 should have been set off. Refer to BSC receive state 44.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X08	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4260'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X09	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X0A	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X0B E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0014'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X0C E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Program forced 7/4, 13.0 off before this test. Refer to BSC Receive state transition 10 and 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X0D E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0012'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X0E E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Program forced 7/4, 13.0 off. Refer to BSC Receive state transition 10 and 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X0F	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0002'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X10	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 27.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X11	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 13.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X12	E2F2	TF48X	F-240
	E2E2	TF80X	
	E2G2	TF40X	

ICW bit 13.3 should have been set on. Refer to BSC receive state 13.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X13	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 39,10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X14	E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC receive state 39. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X15	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X16	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X17	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 58.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792 0X18	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240

E2P2	TF48X	
E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X1A E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Program forced state 7/4, 13.0 off before this test. Refer to BSC Receive state transition 10,57.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X1B E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X1C E2P2	TF82X	F-570
	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Program forced state 7/4, 13.0 off before this test. Refer to BSC Receive state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X1D	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Program forced state 7/4, 13.0 on before this test. Refer to BSC Receive state transition 63.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X1E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X1F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X20	E2B2	TF81X	F-230
		E2L2	TF46X	
		E2P2	TF82X	

The BCC is not correct.
The BCC was zeroed prior to receiving a DLE (BSC receive state 45).
The accumulation after the transition was expected to be X'CC01'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X792	0X21	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X793 BSC Receive; Not EP, USASCII Transmit LCD=4 Receive LCD=D

ROUTINE DESCRIPTION

This routine is a continuation of routine X791, and checks USASCII control characters with LCD equal D. This routine uses Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X01 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X02 E3F2	TE20X	F-220
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X03 E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive state transition 2, 14, and 22.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X04 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X05	E2B2	TF81X	F-230
	E2L2	TF46X	
	E2P2	TF82X	

The BCC field of the receive line ICW should have been reset to zero. BSC Receive state transition 44 resets the BCC.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X06	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2G2	TF40X	

ICW bit 13.3 should have been set on. BSC Receive state transition 14 should have set ICW bit 13.3.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X07	E2B2	TF81X	F-210
	E2Q2	TF34X	

ICW bit 5.4 should have been set off. BSC Receive state transition 44 should have reset ICW bit 5.4.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X08	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4260'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X09	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X0A	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X0B	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0014'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 10 and 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/4 with sequence bit 13.0 off prior to this change.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X0D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0012'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X0F	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590

E2R2	TF32X	
E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 10 and 50.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/4 with sequence bit 13.0 off prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X10	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X11	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0002'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X13	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 39 and 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793 0X14	E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

An L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

Refer to BSC Receive state transition 39.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X15	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'1400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X16	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 58.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X27	E3B2	TE81X	F-440

ICW bit 13.1 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X18	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C06'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0

0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X1A E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive state transition 10 and 57.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/4, 13.0 off prior to this change.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X2A E3B2	TE81X	F-440

ICW bit 13.1 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X1B E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C06'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X1C E2P2	TF82X	F-570
	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Refer to BSC Receive state transition 64.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/4 with sequence bit 13.0 off prior to this change.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X1D	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 on. Refer to BSC Receive state transition 63.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

The program forced state 7/4 with sequence bit 13.0 on prior to this change.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X1E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 65.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X793	0X1F	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X793 0X27 See error stop after 0X17.

X793 0X2A See error stop after 0X1A.

X795 Full Storage Cycle Steal Test

ROUTINE DESCRIPTION

This Routine cycle steals fifty bytes of data into storage locations starting at a buffer in low storage and adding X'4000' to the address on each pass until maximum storage has been reached. This routine depends upon the operation of the scanner in internal wrap mode, thus most of the error stops can be better analyzed via routine X795.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X795	0X01	E3F2	TE20X	F-530
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'.

Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14'

not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X795 0X02	B3F2	TE20X	F-530
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A setmode interrupt failed on the transmit line (address in Register X'11').

Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No setmode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' Not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X795 0X03	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, 5 and 45.

Register X'15' contains the incorrect PCF (Bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X795 0X04	E2C2	TF60X	F-570
	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 1, 2, 14, 25, and 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X795 0X05	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X795 0X06	E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 78.

Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X795	0X07	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line.

Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X795	0X08	E3K2	TE24X	F-420
		E2C2	TF60X	F-480
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected.

Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 4 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 8 is the address of the next byte in the received data buffer.

A failure to compare the data correctly can result if the cycle steal operation did not function correctly. You should compare the results in the receive and send buffer.

If the receive buffer is clear, suspect the ICW cycle steal address byte X circuits.

X797 BSC Transparency Receive - USASCII EP Transmit LCD=4 Receive LCD=6

ROUTINE DESCRIPTION

This routine checks for correct control character deletion with an LCD of 6. This routine uses Diag 0=1 (scanner wrap) and the transmit line uses Diag 1=1 (PCF/EPCF=9/C). Cycle Steal is used by both lines.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X04 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 2, 14, 22, and 8.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X05 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X06 E2P2	TF82X	F-570
	E2E2	TF80X	F-580
	E2B2	TF81X	F-590
	E2K2	TF44X	
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 off. Refer to BSC Receive state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X07 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 75.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X08 E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 OFF. Refer to BSC receive state transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X09	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 72...68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X0A	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/8 with sequence bit 13.0 off. Refer to BSC Receive state transition 74.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X0B	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 77.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X0C	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X0D	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0042'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4

0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X0E	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 27, 13, and 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X0F	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

An L2 interrupt was expected from the receive line. Refer to BSC receive state 21. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X10	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X11	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 ON. Refer to BSC receive state transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X12	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 9.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X13	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive state transition 68.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X14	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/5 with sequence bit 13.0 off. Refer to BSC Receive state transition 67.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X15	E2N2	TF22X	F-150
		E2B2	TF81X	F-210
		E2E2	TF80X	F-240
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0012'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797	0X17	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 7/6 with sequence bit 13.0 on. Refer to BSC Receive state transition 47.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797 0X18	E2J2	TF50X	F-580
	E2B2	TF81X	F-600
	E2K2	TF44X	
	E2R2	TF32X	

The PCF/EPCF should be 5/0 with sequence bit 13.0 undefined. Refer to BSC receive state transition 33,53.

Register X'15' contains the incorrect PCF (bits 0.0-0.3) EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797 0X19	E2E2	TF80X	F-560
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11'). Refer to BSC receive state 53.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797 0X20	E2N2	TF22X	F-150
	E2B2	TF81X	F-210
	E2E2	TF80X	F-240
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0019'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X797 0X21	E3K2	TE24X	F-480
	E2C2	TF60X	
	E2E2	TF80X	
	E2F2	TF48X	
	E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X799 Wrap Data Test - BSC EBCDIC NOT EP LCD=C

ROUTINE DESCRIPTION

This routine transmits all data characters except control characters and expects to receive via internal wrap, the same data characters. This routine uses Diag 0=1 (scanner wrap). Cycle Steal is used by both lines.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X799	0X01	E3K2	TE24X	F-220
		E3F2	TE20X	F-550
		E2D2	TF62X	
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X799	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X799	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, 5, and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X799	0X04	E3J2	TE22X	F-410
		E2E2	TF80X	F-480
		E2C2	TF60X	

The transmit line was wrapped to the receive line for 245 different data characters. The transmit line PCF/EPCF should stay at 9/4 with sequence bit 13.0 off. Byte 0 of register X'14' contains the character being transmitted; byte 1 should equal X'01' for transmit and X'02' for receive. If no tag time was detected, register X'14' contains X'FFFF'. Register X'11' contains the line address being tested.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X799	0X07	E2F2	TF48X	F-480
		E2J2	TF50X	
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X79A EBCDIC To ASCII; ASCII to EBCDIC Translation BSC

ROUTINE DESCRIPTION

This routine first wraps all ASCII translatable non-control characters with the Transmit line in NCP ASCII mode (LCD=D) and the receive line in EP ASCII Transparent mode LCD=6 (no translation). When all characters are wrapped, the receive buffer is checked for the ASCII characters. The Receive line is then put into normal NCP-ASCII mode (LCD=D) and the same character string wrapped. The receive buffer is then checked for the correct EBCDIC characters. This routine uses Diag 0=1 (scanner wrap). Cycle Steal is used by both lines.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X79A	0X01	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X79A	0X02	E3F2	TE20X	F-220
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X79A	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	
		E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 12, 5 and 45.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X79A	0X04	E3D2	TE34X	F-570
		E2P2	TF82X	F-580
		E2E2	TF80X	F-590
		E2B2	TF81X	
		E2K2	TF44X	
		E2R2	TF32X	
		E2J2	TF50X	

NOTE **** If the High Speed Scanner Feature (230KB) is installed:
E3N2 (TE35X) is also a possible failing card.

The PCF/EPCF should be 9/7 with sequence bit 13.0 on. Refer to BSC Transmit state transition 29 and 51.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X79A	0X06	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Transmit LCD=D and receive LCD=6. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X79A	0X07	E3K2	TE24X	F-480
		E2C2	TF60X	
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected. Transmit LCD=D and receive LCD=D.

Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1).

The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer.

The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

ROUTINE DESCRIPTION

X7A0 Data Out 1-7 Set Mode Test

This routine tests the Data Out 1-7 Lines with a set mode, by sending a bit out on Data Out 7 and checking it coming back to the display register, and then shifting the bit to Data Out 6,5 etc. until Data Out 1 has been tested.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A0	0X01	E3F2	TE20X	F-550
		E2D2	TF62X	F-530
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Error Description

0001 No Set Mode L2 Occurred
0002 interrupt from wrong line -

Reg X'14' not equal Reg X'11'.
0003 Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A0	0X02	E2D2	TF62X	F-530
		E2C2	TF60X	
		E2H2	TF42X	

The bit sent out to the LIB on Data Out 1-7 did not compare with the data read back into the Display Register from the LIB.

Register X'13' (bits 1.1-1.7) contains the actual bit sent out to LIB.

Register X'15' (bits 0.1-0.7) contains the bit(s) in error.

Register X'11' contains the address of the line being tested.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A0	0X03	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X' ').

Register X'11' contains the address of the line under test.

X7A1 Disable LIB Test

ROUTINE DESCRIPTION

This routine checks to see if each installed LIB can be disabled. Only LIBs defined as installed in the CDS are tested.

Each LIB is disabled and an attempt is made to set the PCF; the PCF should remain at zero.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A1	0X01	E3H2	TE54X	F-270
		E2J2	TF50X	
		E3E2	TE70X	

The PCF was not set to zero on the LIB disable. Register X'11' contains the line address of the PCF not zeroed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A1	0X02	E2J2	TF50X	F-270
		E3E2	TE70X	
		E3H2	TE54X	

Disabling the LIBs did not force the PCF to zero. Register X'11' contains the line address. An Output X'45' set the PCF to 7 and the disable should have forced the PCF to zero. Register X'15' contains the bit(s) in error.

X7A2 LIB Enable Test

ROUTINE DESCRIPTION

This routine checks to see if each installed LIB can be enabled.

Each LIB was disabled, scope sync 2 was set, and each LIB was enabled. The PCF of each ICW should have been forced to zero as the ICW was scanned.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7A2	0X01	E3E2	TE70X	F-270
		E3H2	TE54X	
		E2J2	TF50X	

The PCF was not zero after the LIB was enabled. Regsiter X'11' contains the line address of the PCF not zeroed.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A2	0X02	E3E2	TE70X	F-270
			E3H2	TE54X
			E2J2	TF50X

The PCF could not be set after enabling the LIB. The LCD/PCF should have been set to 0/7.

X7A3 Setmode Test

ROUTINE DESCRIPTION

This is the first routine requiring that all line set and LIB circuits be operational. The most likely source of problems is the line set receive strobe circuits or the bit clock control circuits in the LIBs.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A3	0X01	E3H2	TE54X	F-550
		E3F2	TE20X	F-530
		E2D2	TF62X	
		E2J2	TF50X	
		E3R2	TE26X	

The expected level 2 interrupt did not occur after executing a set mode on the line addressed by Register X'11'. If the PCF is X'1', the setmode was not completed; if the PCf is X'0', the setmode completed but the level 2 interrupt did not occur within 25 milliseconds. If the LCD is X'F', a feed-back check occurred.

Register X'46' contains the bits used in the setmode.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A3	0X02	E3F2	TE20X	F-550
		E2D2	TF62X	
		E2J2	TF50X	
		E3R2	TE26X	

The level 2 interrupt that occurred was from the wrong line address (Register X'14' does not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A3	0X03	E3F2	TE20X	F-210
		E2D2	TF62X	
		E2J2	TF50X	
		E3R2	TE26X	

The PCF was not set to X'0' during the setmode. The setmode probably did not complete properly.

X7A4 Feedback Error Test

ROUTINE DESCRIPTION

All installed line sets are tested to ensure that a feed-back check occurs if an invalid bit is used during the setmode operation. All line sets are also checked to ensure that feed-back checks do not occur for valid setmode bits.

Register X'13' contains the bit patterns used in each step of this test. The bit patterns are defined as:

Reg X'13 Bit	ICW Bit	SDF Bit	Description
0	26	2	not used

1	27	3	set diagnostic wrap mode
2	28	4	set diata terminal ready
3	29	5	set sync bit clock
4	30	6	set external clock
5	31	7	set data rate select (select high rate)
6	32	8	oscillator select bit 1
7	33	9	oscillator select bit 2

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A4	0X01	E2D2	TF62X	F-530
		E2C2	TF60X	
		E2H2	TF42X	

A feed-back check should have occurred because the CDS indicates that a line set installed does not have a latch for the bit position of the SDF under test. Register X'15' contains the bits that failed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A4	0X02	E2D2	TF62X	F-530
		E2C2	TF60X	
		E2H2	TF42X	

A feed-back check should not have occurred because the CDS indicates that a line set is installed that has a latch that should be set on for this SDF bit position used in the setmode. Register X'15' contains the bits that failed (0.0-0.3=LCD, 1.0-1.7=latches that failed).

X7A5 ALL INSTALLED LINE SETS WRAP (LOW STORAGE BLOCK) WITH 256 BYTES

ROUTINE DESCRIPTION

This Routine cycle steals fifty bytes of data into storage locations starting at a buffer in low storage and adding X'4000' to the address on each pass until maximum storage has been reached. This routine depends upon the operation of the scanner in internal wrap mode, thus most of the error stops can be better analyzed via routine X7A5.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A5	0X01	E3F2	TE20X	F-530
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'.

Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A5	0X02	E3F2	TE20X	F-530
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A setmode interrupt failed on the transmit line (address in Register X'11').

Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No setmode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' Not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A5	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 1, 2, 3, 4, 5 and 45.

Register X'15' contains the incorrect PCF (Bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A5	0X04	E2C2	TF60X	F-570
		E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 1, 2, 14, 25, and 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A5	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A5	0X06	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 78.

Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A5	0X07	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line.

Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A5	0X08	E3K2	TE24X	F-420
		E2C2	TF60X	F-480
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected.

Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 4 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 8 is the address of the next byte in the received data buffer.

X7A6 Oscillator Speed Test

ROUTINE DESCRIPTION

Each installed oscillator in the scanner under test is checked. The oscillator frequency is checked to ensure that not more than a plus or minus .25 percent variation from the expected frequency occurs. The first installed line in the scanner is used to run the test.

This routine depends upon proper operation of the first installed line because the routine tests the oscillators rather than the lines. This routine can indicate failures because of:

Configuration data set configured wrong.

Oscillator card may be defective.

Oscillator select bits failing.

Oscillator gating controls failing.

The following registers are setup for error displays throughout this routine:

Register X'11' contains the line address used in this test.

Register X'14' contains the number of bits counted in this test.

Register X'15' byte 0 contains the relative oscillator position for the oscillator under test.

X'0' indicates the first oscillator.

X'1' indicates the second oscillator.

X'2' indicates the third oscillator.

X'3' indicates the fourth oscillator.

Register X'15'byte 1 contains the oscillator type as obtained from the configuration data set.

Register X'16' contains the number of bits per second expected to be counted.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A6	0X01	E3F2	TE20X	F-550
		E2D2	TF62X	F-530
		E2J2	TF50X	
		E3R2	TE26X	
		E3C2	TE71X	
		E3C4	TE72X	

After a set mode to select the oscillator to be tested, no level 2 interrupt occurred. Refer to the routine description to see the register definition for this routine.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A6	0X02			
		E2D2	TF62X	F-420
		E3C2	TX7A6	E71X
		E3C4	TE72X	

The SDF should have been shifted right to set SDF bit 3 to 0.

Refer to the routine description to see the register definition for this routine.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A6	0X03	E3C2	TE71X	C-020
		E3C4	TE72X	C-040
		E2D2	TF62X	

The oscillator being tested is running too fast.

Refer to the routine description to see the register definition for this routine.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A6	0X04	E3C2	TE71X	C-020
		E3C4	TE72X	C-040
		E2C2	TF60X	
		E2D2	TF62X	
		E3H2	TE54X	

The oscillator being tested is running too slow.

Refer to the routine description to see the register definition for this routine.

X7A7 High Speed Local Attachment Oscillator Speed Test

Routine Description

This manual intervention routine checks the 14.4KHZ/57.6KHZ high speed oscillator that is supplied for the High Speed Local Attachment Line features. The frequency to be checked must be jumpered on the LIB type 1 board in which the oscillator is installed. See the following switch entry specifications for the jumper information. The oscillator frequency is checked to ensure that there is not more than a plus or minus 0.1 percent variation from its expected frequency.

The oscillator frequency and the line that it is to be checked on are entered in the Address/Data switches at stop code F058 as follows:

SWITCH
B C D E

0 X X X 14.4KHZ Test on line XXX (Jumper on pin side A2G4B07 to A2G4B05)
1 X X X 57.6KHZ Test on line XXX (Jumper on bin side A2G4B07 to A2G4B09)

Where XXX is the line address as defined in the F001 manual intervention stop code.

The oscillator frequency is determined by the number of bits shifted in the SDF versus the number of times through a program loop. The SDF is set to X'01FE' and a bit count and program loop count are initialized. Each time through the loop, the loop count is decremented by one and the low order SDF bit is checked. When the low order SDF bit is one, the SDF is reinitialized to X'01FE' and the bit count is decremented by one. If loop count is decremented to zero before the bit count, the residual bit count is compared to 0.1 percent of its initial value. If the bit count is decremented to zero before the program loop count, the residual program loop count is compared to 0.1 percent of its initial value.

This routine indicates failures if:

1. The frequency selected in Address/Data switch B does not agree with the frequency selected by the jumper on A2G4.
2. The oscillator card is defective.
3. External Oscillator select bit in the line set fails to set.
4. Oscillator gating controls are defective.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
x7A7	0X01	E3F2	TE20X	F-550
		E2D2	TF62X	F-530
		E2J2	TF50X	
		E3R2	TE26X	
		E3C2	TE71X	
		E3C4	TE72X	

After a set mode to select external clock, no level 2 interrupt occurred. Register X'11' contains the line address the level 2 interrupt was expected from.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A7	0X02	E2D2	TF62X	F-420
		A2G4	VA070	

The SDF did not shift right 4 Bit times in a minimum of 180 milliseconds to set SDF bit 9 to 1 with an initial character of X'01F0'. Register X'14' and X'13' contain the state of the ICW bits 2.0-5.7 at the end of the wait time. Register X'14' contains the SDF bits 0-7 in byte 1. Register X'13' contains SDF bits 8 and 9 in 0.0-0.1 and the external clock bit in 1.7.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A7	0X03	A2G4	VA070	
		E2D2	TF62X	

The oscillator being tested is running too fast. The bit count decremented to zero before the program loop count was decremented below 0.1 percent of its initial value. Register X'14' contains the residual program loop count. Register X'16' contains the initial program loop count.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7A7	0X04	E3C2	TE71X	C-020
		A2G4	VA070	
		E2D2	TF62X	
		E3H2	TE54X	

The oscillator being tested is running too slow. The program loop count decremented to zero before the bit count was decremented below 0.1 percent of its initial value. Register X'14' contains the residual bit count. Register X'16' contains the initial bit count.

X7A8 Wrap Data Test - BSC and SDLC

ROUTINE DESCRIPTION

This is a manual intervention wrap routine and runs only if you set the CE sense switch to run manual intervention routines or request a single routine to be run.

Once started, this routine runs continuously. To stop, put the function switch to 6 and press INTERRUPT. While the routine is running, the 'A' lights have no meaning. The 'B' lights will show E0XX where XX is the line address being tested.

At the first manual intervention stop, X'F049' enter into switches B, C, D and E from the following options:

FIRST OPTION DISPLAY B = F049

SWITCHES B

0 = NO REQUEST 1ST OSC
8 = EXTERNAL CLOCK
4 = DATA RATE SELECT
3 = OSC SELECT BIT 4TH OSC
2 = OSC SELECT BIT 3RD OSC
1 = OSC SELECT BIT 2ND OSC

SWITCHES C

0 = NO REQUEST
4 = AUTO CALL

SWITCHES D AND E

00 = NO REQUEST
01 = TRANSMIT CONTINUOUSLY
(NO RECEIVE LINE)
02 = TRANSMIT AND RECEIVE
(ALTERNATING LINE ADDRESS)
03 = TRANSMIT AND RECEIVE
(CONTINUOUSLY SAME REC & XMIT LINES
ADDRESS)

DISPLAY B

F050 = TRANSMIT LINE ADDRESS - SEE EXAMPLE BELOW...

F051 = LINE NOT VALID OR NOT INSTALLED

F052 = RECEIVE LINE ADDRESS - SEE EXAMPLE BELOW...

F053 = LINE NOT VALID OR NOT INSTALLED

HIGH ORDER HEX DIGIT OF REQUESTED ADDRESSES SPECIFIES TYPE OF WRAP AS FOLLOWS -

SDLC	BSC
8XXX	0XXX = INTERNAL SCANNER WRAP
EXXX	6XXX = LINE SET WRAP (DM/NOT DTR)
FXXX	7XXX = MODEM WRAP (DM/DTR) FOR MODEMS THAT USE THE MODEM WRAP SIGNAL
DXXX	5XXX = Normal (DTR/NOT DM) an external wrap facility must

be provided to wrap the data with this option

(XXX = CHARACTER CONTROL BLOCK ADDRESS - EX. 5848 FOR BSC LINE ADDR 24)

Transmit data is:

55AA - Five times
CC66 - Five times
EE88 - Five times
F0F0 - Five times
F8E0 - Five times
FCC0 - Five times
FE80 - Five times
FF00 - Five times

Receive data is same as transmit. If failures occur in this routine using line set wrap, modem wrap or normal mode and all previous routines run error-free, the cause of the error stop is most probably in the LIB or Modem.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8 0X01	E3F2	TE20X	F-530
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the autocall line (address in Register X'11').

Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8 0X02	E2E2	TF80X	F-550
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the autocall line. Routine sets PCF/EPCF 2/0 and waits for DSR to cause change to 4/0. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8 0X04	E3F2	TE20X	F-530
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11').

Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8 0X06	E2E2	TF80X	F-550
	E2F2	TF48X	
	E3L2	TE40X	

A L2 interrupt was expected from the receive line. Routine sets PCF/EPCF 2/0 and waits for DSR to cause change to 4/0. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8 0X07	E3F2	TE20X	F-530
	E2D2	TF62X	F-550
	E2J2	TF50X	
	E3R2	TE26X	

A set mode interrupt failed on the transmit line (address in Register X'11').

Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8 0X08	E2D2	TF62X	F-530
	E2H2	TF42X	
	E2C2	TF60X	

Auto call failed to complete or an error has been detected. Reg X'15' byte 0 contains an error indicator number.

1 or 2 - Error in auto call connection. Reg X'15' byte 1 contains SDF bits in error. SDF bits 0-4 on, 5-7 off. Also, an error if LCD not=3, PCF not=4 (Reg X'45' byte 0).

4 - Error indicating PWL, CRQ or DLO not on. Register X'15' byte 1 bits 1, 2 and 3 should be on.

5 - No auto call completion (timeout). Register X'15' byte 1 bit 6 (COS) should be on.

6 - Abandon call and Retry came on. Register X'15' byte 1 bit 7 came on.

Reg '15' byte 1

bit 0=(IR) interrupt remember
bit 1=(PWI) power indication
bit 2=(CRQ) call request
bit 3=(DLO) data line occupied
bit 4=(PND) present next digit
bit 5=(DPR) digit present
bit 6=(COS) call originate status
bit 7=(ACR) abandon call and retry

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8 0X0A	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 undefined.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8 0X0B	E2E2	TF80X	F-570
	E2B2	TF81X	F-580
	E2K2	TF44X	F-590
	E2R2	TF32X	
	E2J2	TF50X	

The PCF/EPCF should be 7/4 with Sequence bit 13.0 undefined.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8	0X0C	E2E2	TF80X	P-550
		E2F2	TF48X	P-560
		E3L2	TE40X	

A L2 interrupt was expected from the transmit and receive lines. The byte count went to zero.

Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A8	0X0D	E3K2	TE24X	F-410
		E2C2	TF60X	F-480
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected.

Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X7A9 Wrap all LIB types 8, 9 and 10.

ROUTINE DESCRIPTION

This routine tests installed line set types 8A, 8B, 9A and 10A. The third installed oscillator (1200 bps) is used and the lines are in BSC mode. All Received data is compared to the sent data to verify correct operation. The data is a string of 55's followed by a string of 00's and a string of AA's. If failures are detected in this routine but not in previous routines, the problem is most probably in the LIB.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A9	0X01	E3F2	TE20X	F-530
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A set mode interrupt failed on the receive line (address in Register X'11'.

Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A9	0X02	E3F2	TE20X	F-530
		E2D2	TF62X	F-550
		E2J2	TF50X	
		E3R2	TE26X	

A setmode interrupt failed on the transmit line (address in Register X'11').

Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No setmode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' Not equal to Reg X'11'.
0003	Feedback check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A9	0X03	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Transmit state transition 48.

Register X'15' contains the incorrect PCF (Bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A9	0X04	E2C2	TF60X	F-570
		E2E2	TF80X	F-580
		E2B2	TF81X	F-590
		E2K2	TF44X	
		E2R2	TF32X	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive state transition 1, 2, 14, 25, and 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A9	0X05	E2E2	TF80X	F-570
		E2B2	TF81X	F-580
		E2K2	TF44X	F-590
		E2R2	TF32X	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Transmit state transition 32.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A9	0X06	E2E2	TF80X	F-560
		E2F2	TF48X	
		E3L2	TE40X	

A L2 interrupt was expected from the receive line. Refer to BSC Receive state transition 78.

Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A9	0X07	E2E2	TF80X	F-550
		E2F2	TF48X	F-560
		E3L2	TE40X	

A L2 interrupt was expected from the transmit line.

Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO
X7A9	0X08	E3K2	TE24X	F-420
		E2C2	TF60X	F-480
		E2E2	TF80X	
		E2F2	TF48X	
		E2H2	TF42X	

The data received and buffered does not equal the data expected.

Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the received data buffer.

X7AA Cycle Utilization Counter Test

ROUTINE DESCRIPTION

This test verifies proper incrementing of the Cycle Utilization Counter (CUC) from cycle steal cycles by the Type 3 Communication Scanner. Expected CUC value represents a combination of cycle steal and

instruction cycles. CCU operation of the CUC for I1, I2 and I3 cycles should have been verified in the CCU diagnostic routines.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7AA	0X01	01AB4T2	CN001

CUC value is not correct after cycle steal operation.

Register X'14' contains the actual CUC value. Register X'15' contains the bits in error. Register X'16' contains the expected CUC value.

If a cycle steal error has previously occurred in the adapter under test, this test is invalid. If no previous errors have occurred, then the error is in the CUC area of the CCU.

X7B1 RPQ EH4100 Transmit Test

ROUTINE DESCRIPTION

This routine test state transitions changed for this RPQ. The data stream in this routine is: ENQ DLE ENQ ENQ The state transitions tested are: 30 25 14, and 15.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X01	E3F2	TE30X F-220
		E3R2	TE26X F-550
		E2J2	TF50X
		E2D2	TF62X

A Set Mode interrupt failed on the transmit line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003	Feedback Check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X05	E2E2	TF80x F-570
		E2B2	TF81x F-580
		E2K2	TF44x F-600
		E2R2	TF32x
		E2J2	TF50x

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Receive State transition 1,2,3,4,5. PP Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X07	E2E2	TF80x F-570
		E2B2	TF81x F-580
		E2K2	TF44x F-600
		E2R2	TF32x
		E2J2	TF50x

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Receive State transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X09	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF2CX	

The transmit line SDF should contain X'012d'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X0B	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Receive State transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X0D	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'0110'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X0F	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Receive State transition 14,15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X11	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'012d'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X13	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/5 with sequence bit 13.0 off. Refer to BSC Receive State transition 15.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B1	0X15	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'012d'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

X7B3 RPQ EH4100 Transmit Test -- EP

ROUTINE DESCRIPTION

This routine test state transitions changed for RPQ Eh4100.

The data stream for this routine is: ENQ EOT A DLE SOH ENQ DLE ENQ.

The state transitions tested are:

30A 75 62 69 76 15A 25 and 14A.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X01	E3F2	TE30X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A Set Mode interrupt failed on the transmit line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003 Feedback Check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X05	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Receive State transition 1,2,3,4,5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X07	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Receive State transition 30a.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X09	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'012d'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X0B	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Receive State transition 75.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X0D	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'0137'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X0F	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the transmit line ICW was expected to be X'0098'.

Register X'15' contains the status bits in error.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X11	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Receive State transition 62.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3 0X13	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E2J2	TF22X	

The transmit line SDF should contain X'01c1'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3 0X15	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 9/3 with sequence bit 13.0 off. Refer to BSC Receive State transition 69.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3 0X17	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E2J2	TF22X	

The transmit line SDF should contain X'0110'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3 0X19	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 76.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3 0X21	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 15a.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3 0X23	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E2J2	TF22X	

The transmit line SDF should contain X'012d'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X27	E2B2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Receive State transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X29	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 14a.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B3	0X31	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'012d'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

X7B4 RPQ EH4100 Transmit Test -- EP Mode, EBCDIC

ROUTINE DESCRIPTION

This routine tests state transitions changed for this RPQ ICW bit 13.5.

The data stream used is: SOH ITB DLE ITB ITB DLE ITB.

The state transitions tested are: 72 29 25 44 (with ICW bit 13.5 on)
21 25 20 (with ICW bit 13.5 off).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4	0X01	E3F2	TE30X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A Set Mode interrupt failed on the transmit line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003	Feedback Check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X05	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 9/2 with sequence bit 13.0 off. Refer to BSC Receive State transition 1,2,3,4,5.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X07	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 72.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X09	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E2J2	TF22X	

The transmit line SDF should contain X'0101'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X0B	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 29.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X0C	E3B2	TE81X	F-440

ICW bit 13.1 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X0D	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E2J2	TF22X	

The transmit line SDF should contain X'011f'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4	0X0F	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2B2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 on. Refer to BSC Receive State transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4	0X11	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'0110'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4	0X13	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 44.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4	0X15	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'011f'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4	0X17	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 21.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X19	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 25.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X21	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 9/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 20.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B4 0X23	E2B2	TF81X	F-440
	E2C2	TF60X	
	E2H2	TF42X	
	E2J2	TF22X	

The transmit line SDF should contain X'011f'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

X7B6 RPQ EH4100 Receive Test -- EP Mode

ROUTINE DESCRIPTION

This routine tests the receive function changes for this RPQ.

The data stream used is: SYN SYN ITB STX ITB DLE ITB.

The state transitions tested are: 1 2 14 15 25A 26 10 19.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6 0X01	E3F2	TE30X	F-220
	E3R2	TE26X	F-550
	E2J2	TF50X	
	E2D2	TF62X	

A Set Mode interrupt failed on the receive line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003 Feedback Check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X02	E3F2	TE30X	P-220
		E3R2	TE26X	P-550
		E2J2	TF50X	
		E2D2	TF62X	

A Set Mode interrupt failed on the transmit line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003 Feedback Check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X03	E2E2	TF80x	P-570
		E2B2	TF81x	P-580
		E2K2	TF44x	P-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 5/1 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 1,2,14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X04	E3B2	TE81X	P-440

ICW bit 13.3 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X05	E2N2	TE81X	P-160
		E3B2	TE22X	P-210
		E2C2	TF60X	P-240
		E2R2	TF32X	
		E2F2	TF46X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X06	E3B2	TE81X	P-440

ICW bit 13.3 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6 0X08	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6 0X09	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 25a.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6 0X0B	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4020'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6 0X0C	E3B2	TE81X	F-440

ICW bit 13.3 should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X10	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 2/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 26.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X12	E3B2	TE81X	F-440

ICW bit 13.1 should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X20	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K1	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive State transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X30	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 19.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X40	E2K2	TE24x	F-480
		E2C2	TF60x	
		E2E2	TF80x	
		E2F2	TF48x	
		E2H2	TF42x	

The data received and buffered does not equal the data expected. Register X'15' contains the expected data.

Register X'13' contains the address of the receive buffer byte in error. Register X'14' contains the received data byte.

X7B7 X.21 LINE SET TEST

ROUTINE DESCRIPTION

This is a manual intervention routine and runs only if directly selected or the CE sense switch is set to run manual intervention routines.

This routine tests the X.21 Line Sets unique handling of Data Set Ready (DSR) and Clear to Send (CTS). The transmit and receive lines must be wrapped (the transmit line's Transmit (T) and Control (C) leads connected to the receive line's Receive (R) and Indicate (I) leads respectively) via an external facility. Refer to FETMM page 1-330 for wrap test block information.

Most of the tests are performed on the transmit line with the results being checked on the transmit and/or receive line. This routine should be run twice on a half duplex pair, reversing the addresses specified as the transmit and receive lines the second time.

The purpose of this routine is to verify control functions; no explicit testing is done on the data sent through the wrap connection. Use routine X7A8 for data analysis and to further verify the line set and external wrap connection.

Refer to logic page VA017 for the jumper information. The following manual intervention stops occur.

At stop F055, enter the routine options as follows:

SWITCH
B C D E

X Y Z 2 2400 BPS Jumpers are in delay position
X Y Z 3 2400 BPS Jumpers are in no delay position

X 8 Z 4 4800 BPS Jumpers are in delay position
X 8 Z 5 4800 BPS Jumpers are in no delay position

X 8 Z 6 9600 BPS Jumpers are in delay position
X 8 Z 7 9600 BPS Jumpers are in no delay position

X 8 Z 8 48K BPS Jumpers are in delay position
X 8 Z 9 48K BPS Jumpers are in no delay position

where x = 0 If the routine is not to be looped without respecifying the manual input.
= 1 If the routine is to be looped without respecifying the manual input.

y = 0 If internal 2400 BPS clock is to be used.
NOTE: This option is only valid for 2400 BPS.
= 8 If external clock is to be used.

z = 0 If the line set is configured for non-switched half duplex operation.
= 2 If the line set is configured for non-switched duplex operation.

At stop F056, enter the transmit line address.

SWITCH
B C D E

0 X X X XXX is the transmit line address as defined in the F001 manual intervention stop code.

At stop F057, enter the receive line address.

SWITCH
B C D E

0 X X X XXX is the receive line address as defined in the F001 manual intervention stop code.

At stop F059, disconnect the external wrap facility. This stop code will be bypassed if the loop option was specified in response to stop code F055. Press START to test the fail safe circuits.

Except for the set mode pretest errors (1X03 and 1X04), error stops are most likely caused by failures in the line set cards, if the other type 3 scanner routines have run successfully. Refer to logic page VA000 for line set card locations. Any one of the three cards of the line set could be causing the error. This routine makes no attempt to isolate failures any further.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B7	0X07		

All 1's were not detected in the SDF of the receive line. The transmit line should be transmitting all marks after initialization.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B7	0X08		

DSR on the transmit side was not active. DSR should be active on the transmit side of a duplex pair when all marks are being received.
NOTE: This stop occurs only if duplex operation was specified.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X09

DSR on the receive side was not active. DSR should be active on the receive side when all marks are being received.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X0B

DSR became inactive on the receive line too soon after diagnostic mode was set on the transmit line. DSR should stay active at least 12 bit times after diagnostic mode on the transmit line forced C and T off; and therefore, the receive line's I and R off through the external wrap facility.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X0C

DSR was still active on the receive line 22 bit times after diagnostic mode was set on the transmit line. DSR should have become inactive 17 bit times after I and R went to 0's.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X12

All marks were not detected in the receive line's SDF, 10 bit times after the set mode interrupt, which resulted from resetting diagnostic mode and setting DTR on the transmit line.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X13

The I lead is active on the receive line before RTS has been activated on the transmit line. The I lead should be connected to the C lead on the transmit line through the external wrap facility.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X15

CTS is active on the transmit line before RTS has been activated.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X18

The I lead did not become active on the receive line after RTS (C) was active on the transmit line. The I lead should be connected to the C lead through the external wrap facility.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X19

CTS became active less than 21 bit times after RTS was set in the line set (I was detected on the receive line).
NOTE: This stop occurs only if delay was specified.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X20

CTS did not become active within one bit time with not delay, 31 bit times with delay after RTS was set in the line set (I was detected on the receive line).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X22

DSR became inactive on the transmit line while a continuous space was being received for 22 bit times when I was active (CTS active on the transmit line).
NOTE: This stop occurs only if duplex operation was specified.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X23

DSR becomes inactive on the receive line while a continuous space was being received for 22 bit times when I was active (RTS active on the transmit line).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X25

DSR became inactive on the transmit line too soon after diagnostic mode was set on the transmit line. DSR should stay active at least 12 bit times after diagnostic mode forced C and T off; and therefore, the receive line's I and R off.
NOTE: This stop occurs only if duplex operation was specified.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X26

DSR was still active on the transmit line 22 bit times after diagnostic mode was set on the transmit line. DSR should have become inactive 17 bit times after I and R on the receive line went to 0's.
NOTE: This stop occurs only if duplex operation was specified.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X27

DSR did not become inactive on the transmit line when the external connection was unplugged.
NOTE: This stop occurs only if duplex operation was specified.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO

X7B7 0X28

DSR did not become inactive on the receive line when the external connection was unplugged.

X7B8 RPQ EH4100 BSC Receive Test -- EP Mode, EBCDIC Control

ROUTINE DESCRIPTION

This routine tests state transitions changed for this RPQ.

The state transitions tested are: 2 14 42 25A 58 73A 10 9 42 25A 73 42.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X01 E3F2	TE30X	F-220
	E3R2	TE26X	F-550
	E2J2	TF50X	
	E2D2	TF62X	

A Set Mode interrupt failed on the receive line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003	Feedback Check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8 0X02	E3F2	TE30X	F-220
	E3R2	TE26X	F-550
	E2J2	TF50X	
	E2D2	TF62X	

A Set Mode interrupt failed on the transmit line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003 Feedback Check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8 0X05	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive State transition 2,14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8 0X06	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8 0X07	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 42.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X08	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2B2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X09	E3B2	TE81X	F-440

ICW bit 0.4 should have been set on.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X0A	E3B2	TE81X	F-440

ICW bit 13.3 should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X10	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 25A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X11	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4060'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X12	E3B2	TE81X	F-440

ICW bit 13.3 should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X20	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive State transition 58.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X21	E3B2	TE81X	F-440

ICW bit 13.1 should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X22	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X30	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 73A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X31	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'0102'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X32	E2E2	TF80x	F-560
		E2F2	TF48x	
		E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X33 E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X40 E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive State transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X41 E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 9.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X42 E3B2	TE81X	F-440

ICW bit 5.4 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X43 E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 42.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X44	E3B2	TE81X	F-440

ICW bit 13.3 should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X45	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X50	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 25A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X51	E3B2	TE81X	F-440

ICW bit 5.4 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X52	E2M2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4020'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X60	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 73.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X61		

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X62	E2E2	TF80x	F-560
		E2F2	TF48x	
		E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X63	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X70	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 42.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X71	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B8	0X80	E2K2	TE24x	F-480
		E2C2	TF60x	
		E2E2	TF80x	
		E2F2	TF48x	
		E2H2	TF42x	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the ixpected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the rceived data buffer.

X7B9 BPQ EH4100 Receive Test -- NCP Mode

ROUTINE DESCRIPTION

This routine test state transitions changed for this RPQ.

The state transitions tested are: 2 14 42 25A 58 73A 10 9 42 25A 73 42.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X01	E3F2	TE30X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A Set Mode interrupt failed on the receive line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003 Feedback Check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X02	E3F2	TE30X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A Set Mode interrupt failed on the transmit line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003 Feedback Check error.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X05	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive State transition 2,14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X06	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X07	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 42.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X08	E2E2	TF80x	F-560
		E2F2	TF48x	
		E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X09	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X0A	E3B2	TE81X	F-440

ICW bit 13.3 should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X10	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 25A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X11	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X12	E3B2	TE81X	F-440

ICW bit 13.3 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X20	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/6 with sequence bit 13.0 off. Refer to BSC Receive State transition 58.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X21	E3B2	TE81X	F-440

ICW bit 13.1 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X22	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4006'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X30	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 73A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X31	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'0102'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X32	E2E2	TF80x	F-560
		E2F2	TF48x	
		E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X33	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X40	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 on. Refer to BSC Receive State transition 10.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X41	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 9.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X42	E3B2	TE81X	F-440

ICW bit 5.4 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X43	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 42.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X44	E3B2	TE81X	F-440

ICW bit 13.3 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X45	E2E2	TF80x	F-560
		E2F2	TF48x	
		E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X46	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X50	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/4 with sequence bit 13.0 off. Refer to BSC Receive State transition 25A.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X51	E3B2	TE81X	F-440

ICW bit 5.4 should have been set off.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X52	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4020'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X60	E2E2	TF80x	F-570
		E2B2	TF81x	F-580
		E2K2	TF44x	F-600
		E2R2	TF32x	
		E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 73.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X61	E2B2	TF81X	F-440
		E2C2	TF60X	
		E2H2	TF42X	
		E2J2	TF22X	

The transmit line SDF should contain X'010E'.
The incorrect SDF data is contained in Register X'15', (BITS 0.6-1.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9 0X62	E2E2	TF80x	F-560
	E2F2	TF48x	
	E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9 0X63	E2M2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0C00'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9 0X70	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 42.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9 0X71	E2E2	TF80x	F-560
	E2F2	TF48x	
	E3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B9	0X72	E2N2	TE81X	F-160
		E3B2	TE22X	F-210
		E2C2	TF60X	F-240
		E2R2	TF32X	
		E2F2	TF48X	
		E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4001'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7B6	0X80	E2K2	TE24x	F-480
		E2C2	TF60x	
		E2B2	TF80x	
		E2F2	TF48x	
		E2H2	TF42x	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the ixpected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the rceived data buffer.

X7BB RPQ EH4100 Recieve Test -- EP Mode,EBCDIC Control

ROUTINE DESCRIPTION

This routine tests BSC receive control character deletion VIA the scanner internal wrap capability. Two ICWs are selected;
one serves as a transmit line set in diagnostic mode with bit 5.6 on. The other line in diagnostic mode receives the wrapped data and deletes the control characters.

This routine looks for EBCDIC characters.

	ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB	0X01	E3F2	TE30X	F-220
		E3R2	TE26X	F-550
		E2J2	TF50X	
		E2D2	TF62X	

A Set Mode interrupt failed on the receive line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003	Feedback Check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X02	E3F2	TE30X	F-220
	E3R2	TE26X	F-550
	E2J2	TF50X	
	E2D2	TF62X	

A Set Mode interrupt failed on the transmit line (Address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from wrong line - Reg X'14' not equal Reg X'15'.
0003	Feedback Check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X03	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 5/1 with sequence bit 13.0 off. Refer to BSC Receive State transition 2,14.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X04	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0XA4	E3B2	TE81X	F-440

ICW bit 13.3 should have been set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X05	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 15.
Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0XA5	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X06	E3B2	TE81X	F-440

ICW bit 13.3 should have been set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X07	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 43.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X08	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2P2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X09	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X0A	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 56.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X0B	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0200'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X0C	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 43.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X0D	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'4000'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X0E	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/3 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 30.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X0F	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 62.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X10	E2N2	TE81X	F-160
	E3B2	TE22X	F-210
	E2C2	TF60X	F-240
	E2R2	TF32X	
	E2F2	TF48X	
	E2Q2	TF34X	

The status posted in the receive line ICW was expected to be X'0200'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort Detect	0.0
0.1	Format Exception	14.1
0.2	Char Over/Under run	0.2
0.3	Data Check	14.3
0.4	BSC bad PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE Error	14.6
0.7	Length Check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X11	E2E2	TF80x	F-570
	E2B2	TF81x	F-580
	E2K2	TF44x	F-600
	E2R2	TF32x	
	E2J2	TF50x	

The PCF/EPCF should be 7/2 with sequence bit 13.0 undefined. Refer to BSC Receive State transition 43.

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7), and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X13	B2E2	TF80x	F-560
	B2F2	TF48x	
	B3L2	TE40x	

A L2 interrupt was expected from the receive line. Either, the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7BB 0X14	B2K2	TE24x	F-480
	B2C2	TF60x	
	B2E2	TF80x	
	B2F2	TF48x	
	B2H2	TF42x	

The data received and buffered does not equal the data expected. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the ixpected data buffer. The contents of register X'16' plus 4 is the address of the next byte in the rceived data buffer.

X7BB 0XA4 See error stop after 0X04

X7BB 0XA5 See error stop after 0X05

X7BC AIRLINES LINE CONTROL -- RPQ 858912

ROUTINE DESCRIPTION

The RPQ modifies the CS3 to enable it to monitor for the synchronizing sequence, ending sequence and carrier of ALC.

This routine tests for sync character (X'80) recognition, the new state transitions generated by the ALC RPQ and the RPQ ending sequence (11-18 consecutive marks).

```
XMIT DATA = X' 81  82 84 88 90 A0 C0  (NON SYNC CHAR'S)
         SYNC (80) 7F 8E 9D AC BB CA D9 EF FE
                   55  E0 FF 80 FF FF'

RCV DATA  = X' 7F 8E 9D AC BB CA D9
               EF FE 55 E0 FF FF FF'
```

Error stop 0X34 is out of sequence, it appears after error stop 0X04 in the listing.
As and aid it appears in its proper place in this document and in the the proper sequence position.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X01	B2A5	TF890	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from the wrong line - Register 14 = wrong line addr.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X02	B2A5	TF890	

A set mode interrupt failed on the transmit line (address in REG X'11'). Display register X'15' to determine the cause of the error.

Reg X'15' Description

0001 No set mode L2 occurred.
0002 Interrupt from the wrong line - Register 14 = wrong line addr.
0003 Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X03	B2A5	TF890	

The PCF/EPCF should be 9/C. Refer to ALC transmit state transition (1).

Register 15 contains the incorrect PCF (bits 0.0-0.3), EPCF (Bits 0.4-0.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X04	B2A5	TF890	

The new sync bit (ICW bit 16.0) was set incorrectly. It should not have been set while in PCF=9.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X34	E2B2	TF81x	F-440
	E2C2	TF60x	
	E2H2	TF42x	
	E2J2	TF22x	

The SDF was expected to be X'1D5'. However, the SDF was not as expected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X05	B2A5	TF890	

The PCF/EPCF should be 7/C with sequence bit 13.0 off. Refer to ALC receive state transition (1).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X06	B2A5	TF890	

The PCF/EPCF should be 7/C with sequence bit 13.0 off. Refer to ALC receive state transition (3).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X07	B2A5	TF890	

The PCF/EPCF should be 7/C with sequence bit 13.0 on. Refer to ALC receive state transition (4).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC 0X08	B2A5	TF890	

The PCF/EPCF should be 7/C with sequence bit 13.0 on. Refer to ALC receive state transition (5).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X09	B2A5	TF890

The PCF/EPCF should be 7/C with sequence bit 13.0 off. Refer to ALC receive state transition (6).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X10	B2A5	TF890

The PCF/EPCF should be 7/C with sequence bit 13.0 on. Refer to ALC receive state transition (4).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X11	B2A5	TF890

The PCF/EPCF should be 5/0. Refer to ALC receive state transition (7).

Register 15 contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X12	B2A5	TF890

A L2 interrupt was expected from the receive line. Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal to Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X14	B2A5	TF890

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort detect	0.0
0.1	Format exception	14.1
0.2	char over/under run	0.2
0.3	Data check	14.3
0.4	BSC and PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE error	14.6
0.7	Length check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X15	B2A5	TF890

Check for correct tag bit insertion into SDF following L2 interrupt.

Expected SDF=X'0020'

Actual SDF in Register X'15' byte 1.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X16	B2A5	TF890

The PCF/EPCF should be 7/C with sequence bit 13.0 on. Refer to ALC receive state transition (2), (4).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X18	B2A5	TF890

The PCF/EPCF should be 5/0. Refer to ALC receive state transition (7).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X20	B2A5	TF890

A L2 interrupt was expected from the receive line. Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal to Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X22	B2A5	TF890

The status posted in the receive line ICW was expected to be X'0400'.

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort detect	0.0
0.1	Format exception	14.1
0.2	char over/under run	0.2
0.3	Data check	14.3
0.4	BSC and PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE error	14.6
0.7	Length check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X23	B2A5	TF890

A L2 interrupt was expected from the transmit line. Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal to Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BC	0X24	B2A5	TF890

The data received and buffered does not equal the expected data. Register X'15' byte 0 contains the expected data; byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of Register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of Register X'16' plus 4 is the address of the next byte in the received data buffer.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X7BC 0X34

See error stop after error stop 0X04.

X7BD AIRLINE LINE CONTROL -- RPQ 858912

ROUTINE DESCRIPTION

This routine tests the ALC RPQ XMIT lines ability to set the new sync bit (ICW 16.0) in PCF=A and to detect the loss of Data Carrier Detect (DCD) on the receive line.

XMIT data = X' 80 7F 8E 9D AC BB CA D9 EF FE 80 AA AA AA'

Data Carrier Detect (DCD) will be dropped following the X'FE' character and following the second X'AA' character.

Error stop 0X34 is out of sequence. It appears after error stop 0X04 in the listing and in this document. For clarity, it is listed in two places in this document so that the reader may find the error stop by looking at either place.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD 0X01	B2A5	TF890	

A set mode interrupt failed on the receive line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from the wrong line - Register 14 = wrong line address.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD 0X02	B2A5	TF890	

A set mode interrupt failed on the transmit line (address in Register X'11'). Display Register X'15' to determine the cause of the error.

Reg X'15'	Description
0001	No set mode L2 occurred.
0002	Interrupt from the wrong line - Register 14 = wrong line address.
0003	Feedback check error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD 0X03	B2A5	TF890	

The PCF/EPCF should be B/C. Refer to ALC transmit state transition (1).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD 0X04	B2A5	TF890	

The new sync bit (ICW 16.0) was not set following ALC transmit state transition (1) while in PCF=A.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X34	E2B2	TF81x	F-440
		E2C2	TF60x	
		E2H2	TF42x	
		E2J2	TF22x	

Checked to verify that the SDF was X'1D5' as expected. However, the SDF was not equal to the expected value. Register X'15' contains the actual value found in the SDF.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X05	B2A5	TF890	

The PCF/EPCF should be 7/C with sequence bit 13.0 off. Refer to ALC receive state transition (1).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X06	B2A5	TF890	

The PCF/EPCF should be 7/C with sequence bit 13.0 off. Refer to ALC receive state transition (3).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X07	B2A5	TF890	

The PCF/EPCF should be 7/C with sequence bit 13.0 on. Refer to ALC receive state transition (4).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X08	B2A5	TF890	

Receive tag not detected in SDF. Register X'15' contains receive line address.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X09	B2A5	TF890	

A L2 interrupt was expected from the receive line. Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal to Register X'11').

Interrupt should have been generated by the loss of (DCD). Receive state transition (9). DCD will be set back on on the next bit service cycle.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X11	B2A5	TF890	

The status posted in the receive line ICW was expected to be X'0400' (EOM and lost DCD).

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort detect	0.0
0.1	Format exception	14.1
0.2	Char over/under run	0.2
0.3	Data check	14.3

0.4	BSC and PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE error	14.6
0.7	Length check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X13	B2A5	TF890

The PCF/EPCF should be 5/0. Refer to ALC receive state transition (9).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X14	B2A5	TF890

The PCF/EPCF should be 7/C with sequence bit 13.0 off. Refer to ALC receive state transition (2).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7) and sequence bit (bit 1.0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X16	B2A5	TF890

Receive tag not detected in SDF. Register X'15' contains the receive line address.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X18	B2A5	TF890

A L2 interrupt was expected from the receive line. Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal to Register X'11').

Interrupt should have been generated by the loss of DCD. Receive state transition (8). DCD will be set back on on the next bit service cycle.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X20	B2A5	TF890

The status posted in the receive line ICW was expected to be X'0480' (EOM and lost DCD).

The status bits in error are in Register X'15'.

Reg X'15' Bits	Description	ICW Bits
0.0	Abort detect	0.0
0.1	Format exception	14.1
0.2	Char over/under run	0.2
0.3	Data check	14.3
0.4	BSC and PAD flag	14.4
0.5	EOM	0.5
0.6	Leading DLE error	14.6
0.7	Length check	14.7
1.0-1.7	ICW byte 15	15.0-7

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD	0X22	B2A5	TF890

The PCF/EPCF should be 5/0. Refer to ALC receive state transition (8).

Register X'15' contains the incorrect PCF (bits 0.0-0.3), EPCF (bits 0.4-0.7).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD 0X23	B2A5	TF890	

A L2 interrupt was expected from the transmit line. Either the interrupt did not occur (Register X'14' equal zero), or the interrupt was from the wrong line (Register X'14' not equal to Register X'11').

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD 0X24	B2A5	TF890	

The data received and buffered does not equal the expected data. Register X'15' byte 0 contains the expected data, byte 1 contains the received data.

Register X'16' contains the address of; the number of bytes tested (byte 0) and the number of bytes remaining to be tested (byte 1). The contents of register X'16' plus 2 is the address of the next byte in the expected data buffer. The contents of Register X'16' plus 4 is the address of the next byte in the received data buffer.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X7BD 0X34			

See error stop after 0X04.

X7F0 SDLC Link Test.

ROUTINE DESCRIPTION

This routine is a manual intervention routine and runs only if you set the CE sense switch to run manual intervention routines or request a single routine to be run.

This routine will stop with manual intervention stop code F020 through F02C requesting entry of options needed to run this routine.

This routine may be used for SDLC data link problem determination and repair verification when on-line tests (under host system control) are not available.

When using this routine for problem determination external to the 3705, all normal internal functional tests should run normally without internal hardware errors. Any local interface problems, such as line set drivers and terminators, should be tested using routine X7A8 or X7A9 with external local wrap options because X7A8 and X7A9 provide more detailed information about local failures.

This SDLC link test is basically an ECHO test with the primary SDLC station sending a SDLC link test command frame down the link. The primary station expects to get the same test frame back if the remote end of the link received the test frame without errors. Some SDLC terminals only respond with a non-sequenced acknowledgement response rather than sending back the link-test frame it received.

Options are provided to run as a SDLC primary station or as a SDLC secondary station. The primary station option initiates the link-test commands and expects to receive responses. The secondary SDLC station responds to test-frames received; if the test frame was received without errors, the same test frame is sent back as a response. If a test frame was received without block check errors and had either more data than could be buffered or did not have the poll bit on in the control field, the secondary station responds with a test frame without optional data. All frames received with block check errors or with abort detect conditions are counted as errors and no response is provided. All frames received with a SDLC station address other than the SDLC station address selected in the F028 manual intervention stop code are counted as an unexpected or non-supported frame and no response is provided. No response is provided for frames with anything but a link-test command field.

The structure of the link-test command enables this test to also run a local external duplex modem wrap if you select the primary station option and connect the transmit and receive lines together properly. A remote wrap can be done if the remote end of the link can tie the transmit and receive duplex lines together with proper loading etc. Because the remote end of the link must store the test frame and send it back, the wrap option does not work on half-duplex lines.

This routine always stops on transmit errors such as modem check, timeout, or overrun, but does not stop on receive errors except for modem check error unless an option is selected to stop on frames in error or stop on any frame.

Continuation (select FUNCTION 5 and press START key) from the 0X20, 0X60 or 0X61 stops, stops the routine, clears all error counts and summary statistics and restarts the test from the transmit/receive data portions. This allows continuing the test on a manual switched line connection without making a new connection. The same restart is used for the D000 dynamic restart option or the D000 restart option at stop code F02C. Any manual switched line connection will not be broken until you abort the routine or use a restart option that goes through total hardware setup such as D002 restart code.

X7F0 ---- The format of all transmissions from this LINK-TEST are:

Pad Pad F A C dd BC BC F ee

where-

Pad = alternate data transition characters for clock correction and will be X'AA' if NRZI mode is not being used or X'00' if NRZI mode is being used.

F = SDLC flag character composed of a zero bit followed by six one bits followed by another zero bit(X'7E').

A = SDLC station address.

C = SDLC control field and will always be X'F3' if a LINK-TEST command/ response is being sent or X'97' if a command reject response is being sent.

dd = Optional transmit/receive data field when the LINK-TEST command is being used. When the command reject response is being sent, the first byte of this field is the command field of the received frame that is being rejected, the second byte is set to zeros (it is defined as the send and receive sequence counts) and the third byte is set to X'04' if more data was received then could be buffered or to X'01' if the LINK-TEST command was received without the poll bit on.

BC = block check(CRC) characters. Two block check characters are always sent and their bit configuration varies according to the SDLC station address, control field and optional data fields.

ee = an ending transmission of X'FF' to make the line go to an idle state and to allow time for bits to be sent before dropping the 'request to send' lead on transmit turnarounds.

All the data defined above between the two flag characters is defined as a FRAME. All references in this document to the frame refers to this portion of each transmitted or received segment of data. Note that if the above is being sent/received in NRZI mode then the actual bit configuration on the line will differ from the ones shown above. Also, SDLC zero bit insertion/deletion applies to all characters except the flags and ending sequence defined under ee.

Test statistics and error count are available while the test is running and at the F02C test completion code. In addition certain registers are used for current status indicators and may be displayed while the test is running or at the F02C stop code. Following is the definition of the status indicators:

X7F0 ---- Register X'1E' contains the current transmit and receive line status.

Byte 0 of reg X'1E' = last received frame type indicator and may contain one of the following indications:

X'00' = Timeout occured on last receive completion.

X'80' = A good link test frame was received with no errors.

X'40' = A command reject response was received as the last frame received at this primary station.

X'20' = A non-sequenced acknowledgement was received as the last frame at this primary station.

X'10' = A block check (CRC error) was detected in the last received frame.

X'08' = An invalid or non-supported frame was received as the last received frame. This link test only supports the link-test response, the non-sequenced acknowledgement response and the command reject response if running as a primary station. The secondary station option will only accept a link-test command but may respond with a link-test response or a command reject response. This indicator is also set if a partial frame was received followed by an 'abort detect' sequence of seven or more consecutive one bits.

X'04' = A valid link-test frame was received but it contained more data than could be buffered. If this is a secondary station, a command reject response is sent for this frame. The maximum length of the receive(and transmit) data buffer is 1024 characters if this 3705 has more than 16K storage or 10 characters if 3705 has only 16K of storage.

X'02' = Invalid SDLC station address received or, for primary station option with optional transmit data, the received data did not compare with the SDLC station address or optional transmit data that was sent. The SDLC station address that you provide in the F028 stop code is used to make this comparison. If the secondary station option was selected, this frame will not be responded to.

X'01' = A hardware detected error such as modem check or overrun has been detected. No response is made to any frames received with this type of error.

Byte 1 of reg X'1E'= transmit line status and other information bits. Multiple bits may be on in this byte as opposed to byte 0 which never will have more than one bit on. The bits within this byte are defined as:

X'80' = A reply is pending to be sent to the last frame received at this secondary station.

X'40' = A command reject reply is now being sent or was the last frame transmitted from this secondary station.

X'20' = A link-test command(from primary station) or response(from secondary station) was the last frame sent or is being sent at this time.

X'10' = A 'transmit initial' operation is being done or was last transmit operation done. This 'transmit initial' is done to set 'request to send' and wait for 'clear to send' from the modem interface for the first transmit operation of all primary station options and for secondary station options when 'request to send' should be on at all times. See manual intervention stop code F020 for this option.

X'08' = Transmit line is busy if this bit is on.

X'04' = Receive line is busy if this bit is on.

X'02' = Bit not defined. May be used as added indicator at later time.

X'01' = Bit not defined. May be used as added indicator at later time.

X7F0 ---- Register X'1F' contains the accumulated transmit and receive line statns indicators. The bits in this register have the same meanings as the bits defined in register X'1E' except once these bit are set on they are not reset until the test is restarted. These bits serve as a summary of all the transmit and receive operations that have been done up to the time this register is displayed.

X7F0 ---- Register X'1D' is used to control the E0XX display code that is put out to the panel display B lights (if function select switch is in positions 4, 5 or 6). This register is cleared to zeros at approximately two second intervals and in between this clearing to zeros it is used as an accumulator of all the bits defined in the register X'1E' bits.

X7F0 ---- Register X'46' is used to control the E0XX display code that is put out to the panel display B lights (if function select switch is in positions 4, 5 or 6). This register is cleared to zeros at approximately two second intervals and in between this clearing to zeros it is used as an accumulator of all the bits defined in the register X'1E' bits.

X7F0 ---- Register X'46' is the scanner display register. This program sets the display bit in the ICW for the receive line used in this test. For half-duplex lines this register gives you the current line interface conditions for both the transmit and receive operations. For duplex lines this register contains the receive line interface conditions. Following is bit definition for byte 0 of this register.

Bit	Hex	Meaning if bit is on.
0	80	'clear to send' is active. Should be on while in transmit mode and may be on while in receive mode. For duplex lines this bit probably will not be on since it reflects the status of the receive half of the duplex pair.
1	40	'ring indicator' is active.
2	20	'data set ready' is active. Should be on for leased lines and should come on after line is connected for switched lines.
3	10	'receive line signal detect'(carrier detect) is active. Should be on while receiving and may be on while transmitting.
4	08	'receive data bit buffer' is a one bit, if the line interface receive data buffer contains a mark(1). Should vary as received data varies.
5	04	'diagnostic mode bit' is on. Should not be on in this test.
6	02	'bit service request bit' is on. Should be on once each bit service.

X7F0 ---- E0XX display codes. While the link-test is running, various display codes are displayed in display B if you have the FUNCTION SELECT SWITCH in function position 4, 5 or 6 (except E06F). These display codes are displayed approximately once every other second with the display B lights cleared to zero between each E0XX display. These E0XX display codes are defined as:

E000 alternating with E0FF = waiting for 'data set ready' to come on before doing any transmit or receive operations. These codes will be continously displayed until 'data set ready' comes on via completing a manual switched connection or via connecting (or jumpering) the proper modem interface leads. On a leased line connection you will not see this display code if 'data set ready' is always on(as expected).

E060 = A good test frame was received within the last two seconds and no other error was detected (except a possible timeout).

E061 = Nothing was received(timeouts) during the last two seconds.

E062 = A block check error(CRC error) was detected in some frame during the last two seconds.

E063 = A non-supported or invalid frame was received during the last two seconds.

E064 = More data was received than could be buffered during the last two seconds.

E065 = A command reject response was received at this primary station during the last two seconds.

E066 = A non-sequenced acknowledgement was received at this primary station during the last two seconds.

E067 = Either of 3 Conditions may exist: 1 - SDLC Station Address did not compare. 2 - Received data did not compare with transmitted data. 3 - Secondary Station received more data than could be buffered. In all cases 'E067' indicates that the data received does not compare with data transmitted.

E068 = A hardware detected error such as modem check or overrun has been detected during the last two seconds.

E06F = This code is displayed if you are using the dynamic communications option (function select 1 and switches B-E set to D0XX) and have entered a D0XX code that is not defined. No action is taken if this code is displayed.

X7F0 ---- D0XX dynamic communications codes. These dynamic communications codes allow you to terminate or restart the link-test at various points within the test. You enter these codes while the program is running by setting the DISPLAY/FUNCTION SELECT SWITCH to function position 1, setting the selected code in switches B-E and then pressing the interrupt key on the control panel. These dynamic communication options are the same as those defined in the F02C manual intervention stop code definition. They are repeated here in a summary form. For more details see the F02C stop code definition.

D000 = Restart link-test at transmit/receive data point(no line resets).

D001 = Restart routine from beginning including asking for options.

D002 = Restart link-test including hardware resets and enables.

D003 = Stop routine at F02C stop code and display statistics.

D004 = Terminate routine after hardware resets.

X7F0 ---- STATISTICS at link test termination.

Register X'1C' contains the address of a statistics table in storage. At all times while the test is running and at the F02C and 0XXX stop codes you may get the storage address of the statistics table from this register and display the storage locations for the following half-word counters. Following is a list of what is available in these statistics:

Hex displacement
within statistics
pointed to by
reg X'1C'.

00 = Number of SDLC link-test frames transmitted successfully. This count does not include command reject responses sent from a secondary station.

02 = Number of SDLC link-test frames received with no errors. If this is a primary station then the received SDLC station address and(if used) the optional data must compare in order to have one added to this count. On a normal F02C completion at a primary station this count should match the number of test frames transmitted count if no errors have been detected. An exception is when the secondary station responds with non-sequenced acknowledgements to test frames then this count should be zero and the received non-sequenced acknowledgements count should match the number of test frames transmitted count.

04 = Number of frames received with block check errors(CRC errors).

06 = Number of command reject responses received at this secondary station.

08 = Number of non-sequenced acknowledgements received at this secondary station.

0A = Number of frames received that were not included in other receive counts. This count includes frames received with invalid SDLC station addresses, non-supported commands/responses, non-data compares with optional transmit data and frames terminated by an abort detection condition. Note that some of these conditions may have caused a block check error and be included in the block check error count and not this count.

0C = If primary station, then this field contains number of test frames requested to be sent in the F022 stop code. If this field is all zeros and a primary station option was selected then test frames will be sent continously (allowing for receiving etc.) without ever terminating the test.

0E = Number of hardware errors detected, such as modem check or overruns, on the transmit and receive operations.

10 = Number of command reject responses transmitted by this secondary station.

X7F0 ---- Following are the error stop codes that may occur in this test. Note that any error stop codes beginning with 1 or 2 in display B byte 0 bits 0-3 are defined in another section of this symptom index. The display B codes starting with F are defined in the manual intervention section of this document.

X7F0 0X07 Auto call failed to complete. An autocall error was detected. Register X'15' byte 0 contains an error indicator which is described below.
Register X'15' byte 1 contains the sdf bits for autocall.
SDF bits for autocall are defined as; bit 0.0 = interrupt remember, bit 0.2 = call request, bit 0.3 = data line occupied, bit 0.4 = present next digit, bit 0.5 = digit present, bit 0.6 = call originate status, bit 0.7 = abandon call and retry.
ERROR INDICATOR.

1 -- Error in auto call connection. Reg.X'15' byte 1 contains SDF bits in error. SDF bits 0-4 on, 5-7 off. Also an error, if LCD not=3, PCF not=4 (reg. X'45' byte 0).

2 -- Error in dialing.

2 -- Error in dialing. See error indicator 1 description.

4,5&6 -- If last digit dialed was not an EON digit, PND may come on and cause a L2 interrupt if the distant station does not answer immediately. The same thing will occur with EON, as last digit, on some OEM (non-IBM) and on IBM auto-call units that do not have the EON feature strapped on. On some OEM auto-call units the EON will cause the auto-call unit to transfer control to the modem/data set with DATA-SET-READY on immediately, even though no distant station has been connected and given an answer tone.

4 -- Error indicating PWI, CRQ or DLO not on. Reg. X'15' byte 1 bits 1,2 & 3 should be on.

5 -- No auto-call completion (timeout). Reg. X'15' byte 1 bit 6 (COS) should bne on.

6 -- Abandon-call and retry came on. Reg. X'15' byte 1 bit 7 came on.

X7F0 0X20 Transmit line operations. A transmit line error has been detected. Reg X'13' contains the accumulated ICW bits 0-15 during this transmit operation. On each level 2 interrupt ICW bits 0-7 are stored together and saved for this error display. If register X'15' bit 0.3 is on, the transmit line has timed out because 'clear to send' did not come on or some other transmit failure such as loss of transmit clock.

See the routine heading for more registers and error statistics. Continuing from this stop by selecting FUNCTION 5 and pressing START restarts the test at the transmit/receive portion without doing a hardware reset and enable. Routines X7A8 or X7A9 may be more useful in isolating this error.

X7F0 0X60 Receive error completion. This error stop occurs if a modem check was detected (ICW bit 3 on) while in receive mode. This stop may also occur if options to stop on any frame of frame in error was selected. Register X'13' contains the ICW bits accumulated during this receive operation by ORing ICW bits 0-7 together and saving them on each level 2 interrupt. The program does not stop for receive timeouts; it sets up to transmit again if stop on any frame or any frame in error options were selected. Register X'16' contains the address of the receive data During each level 2 interrupt service, ICW bits 0-7 are ORed with the previous bits and saved; these bits are displayed in register X'13'. buffer in storage and register X'19' contains the address plus 1 of the last received character.

See the routine heading for test run details, more registers, and link test statistics. Continuing from this stop by selecting FUNCTION 5 and pressing START restarts the test at the transmit/receive portion of the test without doing a hardware reset and enable. Routines X7A8 and X7A9 may be more useful to locate this failure.

X7F0 0X61 Receiving frames. This stop code occurred because an option to stop on the type of frame just received was selected. Register X'1E' defines the type of frame received as explained in in the routine heading. Register X'16' contains the starting address of the receive buffer; register X'19' contains the address one byte past the last character received. Register X'14' contains the accumulated block check characters and should be X'F0B8'. If no errors occurred, register X'13' contains the last 2 characters received and should be the actual received block check (CRC) characters.

See the routine heading for test run details, test statistics, and more registers. Continuing from this stop by selecting FUNCTION 5 and Pressing START restarts the test at the transmit/receive portion without doing a hardware reset and enable but the statistics counters will be cleared.

X7F1 ICW Card Test 1

ROUTINE DESCRIPTION

This manual intervention routine writes various data patterns in ICW bytes according to cards containing the bytes.

To completely test for defective HDB modules, the -4.0 Vdc measured at any B06 pin on the E2 or E3 board must be varied to -3.6 Vdc and to -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

DO NOT attempt to loop on error in this routine. This routine loops in such a manner that looping on error produces extraneous indications.

All type 3 communication scanner IFTs should have been run prior to running this routine.

Approximate run time is 20 seconds.

STOP
CODE

X7F1 F060 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E2 or E3 Board. Adjust the voltage to -3.6 and run the routine several times, replace defective cards that cause errors. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace defective cards that cause errors. Restore the voltage to -4.0 before returning the controller to the customer.

The voltage is adjusted via the potentiometer on 0XD-H2/0XD-A1.

The routine will loop as long as ADDRESS/DATA Switch E is set to any value other than 0. Thus, if you wish to loop the routine, set switch E to any value other than 0 for as long as you wish to loop.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F1 0X01	E3G2	TE-210	F-320	Pass = 0000 ICW bytes 7 and 9

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E3G2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F1 0X02	E3F2	TE-200	F-320	Pass = 0100 ICW bytes 6 and 8

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E3F2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F1 0X03	E2T2	TF-200 TF-200	F-280 F-350	Pass = 0200 ICW bytes 0 and 14

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2T2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F1 0X04	E2U2	TF-300 TF-300	F-290 F-320	Pass = 0400 ICW bytes 2 and 10

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2U2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F1	0X05 E2G2	TF-400	F-300	Pass = 0800
		TF-400	F-340	ICW bytes 3 and 13

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2G2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F1	0X06 E2S2	TF-210	F-290	Pass = 1000
		TF-210	F-350	ICW bytes 15 and 16

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2S2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F1	0X07 E2M2	TF-310	F-300	Pass = 2000
		TF-310	F-310	ICW bytes 5 and 11
		TF-310	F-320	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2M2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F1	0X08 E2V2	TF-410	F-300	Pass = 4000
		TF-410	F-300	ICW bytes 4 and 12
		TF-410	F-340	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2V2. Do not attempt to loop on error in this routine.

X7F2 ICW Ping Pong Card Test 1

ROUTINE DESCRIPTION

This manual intervention routine writes X'00', X'08', X'FF', and X'F7' in ICW bytes according to cards containing the bytes.

To completely test for defective HDB modules, the -4.0 Vdc measured at any B06 pin on the E2 or E3 board must be varied to -3.6 Vdc and to -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

DO NOT attempt to loop on error in this routine. This routine loops in such a manner that looping on error produces extraneous indications.

All type 3 communication scanner IPTs should have been run prior to running this routine.

Approximate run time is 1.0 minutes.

STOP CODE	
X7F2 F060	This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E2 or E3 Board. Adjust the voltage to -3.6 and run the routine several times, replace defective cards that cause errors. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace defective cards that cause errors. Restore the voltage to -4.0 before returning the controller to the customer.

The voltage is adjusted via the potentiometer on 0XD-H2/0XD-A1.

The routine will loop as long as ADDRESS/DATA Switch E is set to any value other than 0. Thus, if you wish to loop the routine, set switch E to any value other than 0 for as long as you wish to loop.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F2	0X01	E3G2	TE-210	F-320	Pass = 0000 ICW bytes 7 and 9

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E3G2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F2	0X02	E3F2	TE-200	F-320	Pass = 0100 ICW bytes 6 and 8

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E3F2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F2	0X03	E2T2	TF-200 TF-200	F-280 F-350	Pass = 0200 ICW bytes 0 and 14

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2T2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F2	0X04	E2U2	TF-300 TF-300	F-290 F-320	pass = 0400 ICW bytes 2 and 10

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2U2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F2	0X05	E2G2	TF-400 TF-400	F-300 F-340	Pass = 0800 ICW bytes 3 and 13

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2G2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F2	0X06	E2S2	TF-210 TF-210	F-290 F-350	Pass = 1000 ICW bytes 15 and 16

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2S2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F2	0X07 E2M2	TF-310	F-300	Pass = 2000
		TF-310	F-310	ICW bytes 5 and 11
		TF-310	F-320	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2M2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F2	0X08 E2V2	TF-410	F-300	Pass = 4000
		TF-410	F-300	ICW bytes 4 and 12
		TF-410	F-340	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2V2. Do not attempt to loop on error in this routine.

X7F3 ICW Ping Pong Card Test 2

ROUTINE DESCRIPTION

This manual intervention routine writes X'00', X'08', X'FF', and X'F7' in ICW bytes according to cards containing the bytes.

To completely test for defective HDB modules, the -4.0 Vdc measured at any B06 pin on the E2 or E3 board must be varied to -3.6 Vdc and to -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

DO NOT attempt to loop on error in this routine. This routine loops in such a manner that looping on error produces extraneous indications.

All type 3 communication scanner IFTs should have been run prior to running this routine.

Approximate run time is 2.3 minutes.

STOP CODE

X7F3 F060 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E2 or E3 Board. Adjust the voltage to -3.6 and run the routine several times, replace defective cards that cause errors. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace defective cards that cause errors. Restore the voltage to -4.0 before returning the controller to the customer.

The voltage is adjusted via the potentiometer on 0XD-H2/0XD-A1.

The routine will loop as long as ADDRESS/DATA Switch E is set to any value other than 0. Thus, if you wish to loop the routine, set switch E to any value other than 0 for as long as you wish to loop.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F3	0X01 E3G2	TE-210	F-320	Pass = 0000
				ICW bytes 7 and 9

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E3G2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F3	0X02	B3F3	TE-200	F-320	Pass = 0100 ICW bytes 6 and 8

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card B3F3. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F3	0X03	E2T2	TF-200	F-280	Pass = 0200 ICW bytes 0 and 14
			TF-200	F-350	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2T2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F3	0X04	E2U2	TF-300	F-290	Pass = 0400 ICW bytes 2 and 10
			TF-300	F-320	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2U2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F3	0X05	E2G2	TF-400	F-300	Pass = 0800 ICW bytes 3 and 13
			TF-400	F-340	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2G2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F3	0X06	E2S2	TF-210	F-290	Pass = 1000 ICW bytes 15 and 16
			TF-210	F-350	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2S2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F3	0X07	E2M2	TF-310	F-300	Pass = 2000 ICW bytes 5 and 11
			TF-310	F-310	
			TF-310	F-320	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2M2. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F3	0X08 E2V2	TF-410	F-300	Pass = 4000
		TF-410	F-300	ICW bytes 4 and 12
		TF-410	F-340	

Either a level 1 interrupt occured or the data did not equal that expected.

Replace card E2V2. Do not attempt to loop on error in this routine.

X7F4 PDF Array Data Test

ROUTINE DESCRIPTION

This routine writes X'000', X'008' X'FFF', and X'FF7' throughout the 512 PDF array bytes and then compares each byte of each HDB module to expected data while changing every other byte in the module. Both operations are executed both forward and reverse.

To thoroughly test the PDF array for defective HDB modules, the -4.0 Volts dc must be varied to -3.6 and -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-1017 Page D-230/D-580 to vary the -4.0 Volts.

DO NOT attempt to loop on error in this routine. This routine loops in such a manner that looping on error produces extraneous indications.

All type 3 communication scanner IFTs should have been run prior to running this routine. DO NOT attempt to loop on error in this routine.

Approximate run time is 2.0 seconds.

STOP CODE

X7F4 F060 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E2 or E3 Board. Adjust the voltage to -3.6 and run the routine several times, replace defective cards that cause errors. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace defective cards that cause errors. Restore the voltage to -4.0 before returning the controller to the customer.

The voltage is adjusted via the potentiometer on 0XD-H2/0XD-A1.

The routine will loop as long as ADDRESS/DATA Switch E is set to any value other than 0. Thus, if you wish to loop the routine, set switch E to any value other than 0 for as long as you wish to loop. Do not attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7F4	0X01 E3N2	TE30X	F-240

Replace card E3N2. DO NOT attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7F4	0X02 E3P2	TE31X	F-240

Replace card E3P2. DO NOT attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7F4	0X03 E3M2	TE32X	F-240

Replace card E3M2. DO NOT attempt to loop on error in this routine.

X7F5 PDF Array Ping Pong Test # 1

ROUTINE DESCRIPTION

This routine writes X'000', X'008' X'FFF', and X'FF7' throughout the 512 PDF array bytes and then compares each byte of each HDB module to expected data while changing every other byte in the module. Both operations are executed both forward and reverse.

To thoroughly test the PDF array for defective HDB modules, the -4.0 Volts dc must be varied to -3.6 and -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual SY27-0107 Page D-230/D-580 to vary the -4.0 Volts.

DO NOT attempt to loop on error in this routine. This routine loops in such a manner that looping on error produces extraneous indications.

All type 3 communication scanner IFTs should have been run prior to running this routine.

Approximate run time is 1.75 minutes.

STOP
CODE

X7F5 F060 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E2 or E3 Board. Adjust the voltage to -3.6 and run the routine several times, replace defective cards that cause errors. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace defective cards that cause errors. Restore the voltage to -4.0 before returning the controller to the customer.

The voltage is adjusted via the potentiometer on 0XD-H2/0XD-A1.

The routine will loop as long as ADDRESS/DATA Switch E is set to any value other than 0. Thus, if you wish to loop the routine, set switch E to any value other than 0 for as long as you wish to loop.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7F5 0X01	E3N2	TE30X	F-240

Replace card E3N2. DO NOT attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7F5 0X02	E3P2	TE31X	F-240

Replace card E3P2. DO NOT attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7F5 0X03	E3M2	TE32X	F-240

Replace card E3M2. DO NOT attempt to loop on error in this routine.

X7F6 PDF Array Ping Pong Test # 2

ROUTINE DESCRIPTION

This routine writes X'000', X'008', X'FFF', and X'FF7' throughout the 512 PDF array bytes and then compares each byte of each HDB module to expected data while changing every other byte in the module. Both operations are executed both forward and reverse writing various data pattern into the PDF array. To thoroughly test for defective HDB modules, the -4.0 Volts dc must be varied to -3.6 and -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

All type 3 communication scanner IFTs should have been run prior to running this routine.

Approximate run time is 2.0 minutes.

STOP CODE	
X7F6	F060 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E2 or E3 Board. Adjust the voltage to -3.6 and run the routine several times, replace defective cards that cause errors. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace defective cards that cause errors. Restore the voltage to -4.0 before returning the controller to the customer. The voltage is adjusted via the potentiometer on 0XD-H2/0XD-A1. The routine will loop as long as ADDRESS/DATA Switch E is set to any value other than 0. Thus, if you wish to loop the routine, set switch E to any value other than 0 for as long as you wish to loop.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	ADDITIONAL INFORMATION
X7F6	0X01	E3N2	TE30X	F-240

Replace card E3N2. DO NOT attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7F6	0X02	E3P2	TE31X	F-240

Replace card E3P2. DO NOT attempt to loop on error in this routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X7F6	0X03	E3M2	TE32X	F-240

Replace card E3M2. DO NOT attempt to loop on error in this routine.

COMMON ERROR STOP SYMPTOM INDEX

ROUT.	ERROR CODE	FUNCTION TESTED COMMENTS	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	
X7XX	1X01	Configuration Data Set	CDS indicates it is not for the type 3 communication scanner, or has an invalid scanner number in its scanner type and number field.					Register X'16'= addr of the scanner control block CDS in error.
X	1X03	Set mode.	The L2 interrupt that occurred during set mode was not from the expected line address. This is a pretest error so if you use the continue function(function 5) then the set mode will be tried again.	E3L2		TE401	F-550	Reg X'14'=addr (set into ABAR) that interrupted in error. Reg X'11' is the addr that the l2 was expected from. Reg X'14'=0 if no L2 occurred.
X7XX	1X04	Set mode.	A feedback check occurred setting the LCD field of the ICW to X'F'. This is a pretest error so if you use the continue function(function 5) then the set mode will be tried again.	E2D2		TF620	F-220 F-530	Reg X'11'=line addr (set into ABAR) of the scanner-LIB-line addr the set mode is done on.
X7XX	1X05	Set mode.	Missing the level 2 interrupt expected within 1 bit time after doing the set mode. This is a pretest error so if you use the continue function(function 5) the set mode will be tried again.	E2J2		TF502	F-550	Reg X'11'=addr set into ABAR; this line set was setup via the setmode.
X7XX	1X06	Configuration Data Set.	An invalid LIB type is defined for the scanner being tested.					Reg X'15' byte 0= an invalid LIB type found in the CDS. Reg X'11'=addr set into ABAR for the scanner -LIB- line addr.
X7XX	1X07	Configuration Data Set.	An invalid line set type is defined for the line being tested. Reference the CDS description in the previous chapters of this document.					Reg X'15' byte 1= invalid line set type in the CDS. Reg X'11'=addr being checked.
X7XX	2X01	All functions not expecting or causing L1 interrupt.	Unexpected L1 interrupt occurred with no CCU or adapter L1 error bits on.	E3E2		TE706	6-090	
X7XX	2X02	All functions not expecting a L1 intrpt or causing a level 1 interrupt.	Unexpected L1 interrupt occurred indicating a type 3 scanner level 1 error.	E3E2		TE706	F-190 F-200	Reg X'76' contains adpt intr gp 1 error bits.
X7XX	2X03	All functions not expecting or causing a L1 interrupt.	L1 adapter (type 3 scanner) interrupt occurred with no scanner error Reg X'42' or X'43' bits on for the scanner causing this error.	E3E2		TE706	F-190 F-200	Using the service aid for masking L1 interrupts.
X7XX	2X04	All functions allowing adapter L1 interrupts.	Cannot reset type 3 scanner adapter L1 interrupt bits.	E3E2		TB700	F-270	Reg X'76' contains adapter interrupt error bits.
X7XX	2X05	All functions.	An Input/Output check caused by a valid input or output instruction.	E3R2 E3E2		TE263	6-981	Reg X'74' contains addr of the valid input or output instruction.

ROUT.	ERROR CODE	FUNCTION TESTED	ERROR DESCRIPTION	SUSPECTED CARD LOCATION(s)	PROG MASK	FEALD PAGE	FETMM PAGE	COMMENTS
X7XX	2X21	All functions not expecting L2 interrupts but allowing L2 interrupts to occur.	Unexpected level 2 interrupt occurred.	E3L2		TE401	F-550 F-560	
X7XX	2X33	All functions.	An unexpected level 3 interrupt occurred with no L3 interrupt request bits on.				6-090	
X7XX	2X44	All functions.	L4 unexpected reentrance. The DCM gives control to all routines with L4 PCI bit on (Reg 7F byte 0 bit 7 on). This bit should never be turned off and should never exit L4 except to L1, L2, and L3 which are higher priority.				6-090	
X7XX	E0XX	Display information.	This display is for information only. The XX after the E0 is the LIB and line address now under test unless otherwise specified in the routine write up.					This E0XX display indicates that the routine is running.

MANUAL INTERVENTION STOP CODES AND EXAMPLES.

Display
B Stop Code — Manual Intervention Action Required.

F001 Enter the line address to be tested. Set switches B, C, D and E to 0000 to test all addresses, and set to FFFF to bypass all testing. Otherwise, enter the line address as used to set ABAR. See FETMM page B-330 for a chart on all valid line addresses. Note- some routines will not accept the 0000 switch settings to test all installed line addresses and in that case you will get another manual stop code saying an invalid line address was selected.

To continue from this manual intervention stop(and all manual intervention stops) set the required information into the STORAGE DISPLAY/DATA ADDRESS SWITCHES B, C, D and E: set the DISPLAY/FUNCTION SELECT SWITCH to function position 5: and then press the START switch.
Following is the format to enter the line address.

	Hex
Switch B =	0

	Hex
Switch C =	0 for 1st scanner address bits. 1 for 2nd scanner address bits. 2 for 3rd scanner address bits. 3 for 4th scanner address bits.

	Hex
Switch D =	4 for 1st LIB, lines 0-7 5 for 1st LIB, lines 8-F 6 for 2nd LIB, lines 0-7 7 for 2nd LIB, lines 8-F 8 for 3rd LIB, lines 0-7 9 for 3rd LIB, lines 8-F A for 4th LIB, lines 0-7 B for 4th LIB, lines 8-F
Switch E =	0 for lines 0 or 8 2 for lines 1 or 9 4 for lines 2 or A 6 for lines 3 or B 8 for lines 4 or C A for lines 5 or D C for lines 6 or E E for lines 7 or F

F002 Invalid scanner address bits were entered in switch C. Re-enter the line address as in stop code F001.

F003 The selected scanner is not installed or not configured properly in CDS. Reg X'16' contains the address of the scanner block for the requested scanner. If reg X'16'=X'0000', the scanner is not configured. Re-enter the request as in stop code F001.

F004 Invalid LIB address selected. Re-enter the request as in stop code F001. (Only 3 LIBs are allowed in the first type 3 scanner and 4 Libs in each additional Type 3 scanner).

F007 The selected line address is not installed according to data in the CDS. This routine requires a line adapter to be installed to run tests. Re-enter the line address as in stop code F001.

F008 This routine cannot run tests on the LIB or type of line adapter for the line address selected. Re-enter the line address as in stop code F001.

F020 Enter LINK-TEST line type and control options. Notes: primary station option initiates link-test, secondary station option only responds to link-test command received from a remote primary station.

'RTS'=on means that 'request to send' is to be left on at all times(even during receive operations) and is normally used for point-to-point four wire half-duplex and duplex leased lines for both primary and secondary stations. For multi-point primary station the 'RTS'=on option is usually used for four wire half-duplex and duplex lines. Two wire leased lines, switched lines and multi-point secondary stations usually use the 'RTS'=off option to drop 'Request to send' while not in transmit mode.

The 'external clock', 'data rate select' and 'oscillator select' options are dependent on the type of modem connected and the type of internal and/or external clocks installed. If you select the 'external clock' option (with or without 'data rate select'=on) then the program will not use NRZI mode of transmission. If you select internal oscillators number 0, 1,2 or 3 then the program uses NRZI mode. NRZI mode means (as implemented in the 3705) that if a zero bit is to be transmitted then complement the transmit line trigger, if a one bit is to be sent then do not change the state of the transmit line trigger. The combination of NRZI mode and SDLC 'zero bit insertion' operations always result in at least one data transition every six bit times so that modem or internal clocks can be kept in phase. NRZI mode is not used when external clock is selected from the modem since it is then the modems responsibility to provide clock correction and bit synchronizing. This automatic selection of NRZI mode according to type of line clocking is compatible to 3705/3704 NCP utilization.

The optional transmit data option can only be used with the primary station options to provide data characters to be sent within the SDLC link-test frames being transmitted. This optional data is sent after the SDLC station address and control fields and before the block check(CRC) characters. If the optional transmit data option is not selected for a primary station option then the minimum test frame of four characters (SDLC station address, SDLC link-test control field and two block check characters) preceded and followed by flag characters are transmitted. Note that 16 alternate bit transitions are transmitted before the first flag character of a frame so that the receive clock can be corrected.

To continue from this stop code (and all manual intervention stop codes) set the STORAGE ADDRESS/REGISTER DATA switches B, C, D and E to the required settings, set the DISPLAY/FUNCTION SELECT switch to function position 5 and then press the start key.

Switch B-E setting to enter line type and control options for F020 stop code are;

Switch B = line type options. Enter one of the following in switch B.

0= Primary station, half-duplex 2-wire leased line with 'RTS'=off option.

1= Secondary station, half-duplex 2 wire leased line with 'RTS'=off option.

2= Primary station, half-duplex 4-wire leased line with 'RTS'=on option (normally point-to-point).

3= Secondary station, half-duplex 4-wire leased line with 'RTS'=on option (normally point-to-point).

4= Secondary station, half-duplex,4-wire leased line with 'RTS'=off option (normally multi-point secondary).

5= Primary station, duplex 4-wire leased line with 'RTS'=on option. Note: requires duplex line set interface such as line set type 1H or LIB type 10.

6= Secondary station, duplex 4-wire leased line with 'RTS'=on option. Note: requires duplex line set interface such as line set type 1H or LIB type 10.

7= Secondary station, duplex 4-wire leased line with 'RTS'=off option(normally multi-point secondary). Note: requires duplex line set interface such as line set type 1H or LIB type 10.

8= Primary station, switched line with manual call, manual answer or auto answer with 'RTS'=off option. Note: half-duplex only for switched lines.

9= Secondary station, switched line with manual call, manual answer or auto answer with 'RTS'=off option. Note: Half-duplex only for switched lines.

A= Primary station, switched line with auto-call. Note: Half-duplex only for switched lines.

B= Secondary station, swithced line with auto-call. Note: Half-duplex only, for switched lines.

Switch C = clock control options. Enter one of the following in switch C.

0= Internal oscillator select 0 to use first internal oscillator.

1= Internal oscillator select 1 to use second internal oscillator.

2= Internal oscillator select 2 to use third internal oscillator.

3= Internal oscillator select 3 to use fourth internal oscillator.

4= Select external clock but do not select 'data rate select'.

5= Select external clock and also set 'data rate select' to use the highest of the two external clocking rates.

Switch D = NRZI Control with external clock.

0= External clock, non-NRZI, or internal clock NRZI

1= External clock NRZI

2= External clock, new sync, non-NRZI mode
Note: New sync is normally used with 4-wire multipoint leased-line modem equipment where the associated interface is designated as the master station (primary).

3= External clock, new sync, and NRZI mode.
See the note under 2= above.

Switch E = Transmit and receive data options. Enter one of the following in switch E.

0= No optional transmit data and no stopping on received frames.

1= Stop on any frame received with a bad block check(CRC) character.

2= Stop on any frame received other than a normal link-test command or response.

3= Stop on any frame received(good or bad).

4= Optional transmit data is wanted and will be asked for in the F024 and F025 stop codes. This option is restricted to primary stations. This option does not include any stops on received frames.

5= Optional transmit data is wanted and will be asked for in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes a 'stop on any frame received with a block check(CRC) error' option.

6= Optional transmit data is wanted and will be asked for in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes the 'stop on any frame received other than a normal test frame' option.

7= Optional transmit data is wanted and will be asked for in the F024 and F025 stop codes. This option is restricted to primary stations. This option includes the 'stop on any frame received' option.

F021 Invalid or invalid combination of options entered for the LINK-TEST. Enter options again as defined in the F020 stop code.

F022 Enter number of test frames to be transmitted at this primary station for the LINK-TEST.

Set switches B through E to number (in hex) of times you want the test frame transmitted before the program terminates with the F02C completion code. If you enter 0000 then the test will never terminate unless you use the dynamic communication options or unless you abort the test.

F024 Enter first optional transmit data character for the primary station LINK-TEST option.

Set switches D and E to the hex character to be transmitted.

If only one optional data character is to be transmitted then set switches B or C to any non-zero value. If more than one optional transmit data character is to be sent then set switches B and C to 00.

F025 Enter next optional transmit data character to be sent from this primary station of the SDLC LINK-TEST.

Set switches D and E to the hex character that you want to use as the next data character to be transmitted.

If this is the last optional transmit data character you want to send then set switches B or C to any non-zero value. If you want to enter more optional transmit data then set switches B and C to 00 and the current data character in switches D and E will be stored when you select function 5 and press start. Then you will get this stop code again

unless end of transmit buffer has been reached. If the machine this test is running in has over 16K of storage then you may enter up to 1022 character to be transmitted with the F024 and F025 stop codes. If the machine has only 16K of storage then you are limited to a 24 character maximum.

F026 Enter transmit line interface address. Enter line address in same format as defined in the F001 manual intervention stop code.

If you selected an option using duplex lines then you must enter the transmit line interface address of the duplex line interface pair. Note: duplex transmit line interface is always first line interface address of the even/odd line interface pair with the even line interface address being used as the transmit line and the odd line interface address being used as the receive line. Note also that this line interface address to be entered does not use the low order bit of byte 1 to set/input ABAR so that line addresses such as 0842 and 0846 are considered to be odd line interface addresses and line addresses such as 0840 and 0848 are even line interface addresses.

The line interface address you enter is used to get line set type and options according to what is found in the configuration data set(CDS). If you have selected a not-installed or invalid line address you will get stop code F027 asking for the line interface address again. If you selected a duplex line option then the line set type must be a type that can run in duplex mode and the same applies for half-duplex, switched and internal/external clock selection.

If you enter FF in switches B and C and then continue the program will go back to the F020 stop code to ask for initial options again.

F027 Transmit line interface address you entered in stop code F026 was invalid line set type for running with options you selected. Enter transmit line interface address again as defined in stop code F026. If you enter FF in switches B and C and then continue the program will go back to the F020 stop code to ask for initial options again.

F028 Enter SDLC station address in switches D and E.

If you selected the primary station option then this will be the SDLC station address put into all test frames transmitted on the line and the SDLC station address that this station expects to receive from the remote secondary station. If you selected the secondary station option then this will be the SDLC station address searched for in all incoming frames and the SDLC station address put into the response test frames or command reject response sent back to the remote primary station.

If the secondary station receives a frame that has a different SDLC station address than the one you are entering then it will not respond to that frame but will count it in the statistics counters defined in routine X6F0 writeup.

After you continue from this code the program will reset and enable the scanner and start the LINK-TEST. See routine writeup for display codes you will get while test is running.

F029 Enter the line address of the auto call originate line interface to be used in this test. See stop code F001 for format to enter the line address.
Note:If the line address you entered is either invalid or not configured
as an auto call originate line, this stop code will be displayed again.
Enter line address again as defined for this stop code.

F02A Enter the first digit to be dialed on the auto call originate line. Set switch D to 0 and switch E to the next digit to be dialed (Press Start)

F02B Enter the next digit to be dialed. Set switch D to 0 and switch E to the next digit to be dialed (Press Start) Continue entering digits in this manner and after last digit has been entered set switches D and E to FF and Press START.

The program will now reset and enable the scanner and start the link-test. Wait for normal connection or timeout (20 sec) to occur. If normal connection occurs each dial digit will be displayed in display B, BYTE 1, as it is dialed.

F02C LINK-TEST has terminated. Check statistics and register indicators defined in the routine heading if necessary. Then enter a link test restart or termination option.

The following list of options are acceptable with switches B and C set to D0 or 00 for theis F02C stop code. The same options may be used with the D0 settings when using the dynamic communications options defined in the routine writeup. Following is a list of the restart/termination options:

Set switches
B,C,D and E
To: For this restart/terminate option.

D000 Restart LINK-TEST at point where it setup initial transmit and receive operations without doing a scanner reset and enable operation. This option allows you to restart the test on a switched line without making a new dialed connection, but may be used on any type of restart except a scanner or LIB failure. If you use this restart option then all the statistic counters will be cleared(except number of frames to transmit) and run indicators will be reset to starting options.

D001 Restart routine at stop code F020 asking for LINK-TEST options. This restart option will mask level 2 interrupts and mess up transmit and receive buffer pointers but will not modify any of the other link test statistics and will not reset the lines currently in use until after you have entered your new options. Therefore this option may be used to terminate the current test but still be able to look at test statistics or be able to respecify options.

D002 Restart LINK-TEST from hardware reset and enable in the scanner. This option will clear all run indicators and statistics as in option D000 but in addition it will disconnect any switched line connection due to the scanner reset and enable. This restart option should be used if a scanner or LIB failure occurred or if you did any outputs from the control panel that changed the current line conditions.

D003 Go to stop code F02C and wait for next selection of options. This stop code is used for dynamic communications(function select position 1 and D003 in switches B-E). If used at F02C stop code then it will just result in stop F02C again. This dynamic communications may be used to terminate the test before the transmit frame count is reached for the primary station option or to therminate the secondary station option when nothing is being received(indicated by F061 display code being displayed continously).

D004 Terminate routine after resetting scanner. This option should be used when you are done testing with the LINK-TEST. This will terminate the LINK-TEST routine and if you have not set the CE sense switches to cycle on request or if you are not running multiple IFT's or adapters then the DCM will come out with a display B stop code of 80?? asking for your next test request.

F030 Enter transmit, receive, wrap or dial option.

Note: See examples on how to use stop codes F030 through F042 after the F042 stop code description at the end of the manual intervention stop codes.

Enter in switches B-E your selected option. Options are:

0001 - Transmit test on a non-switched leased line or local attachment.
0002 - Receive test on a non-switched leased line or local attachment.
0003 - Wrap a pair of non-switched or local lines.
0004 - Transmit test on a switched line using manual dialing and line connection.
0005 - Receive test on a switched line using manual dialing and line connection.
0006 - Wrap a pair of switched lines using manual dialing and line connection.
0007 - Dial numbers on an auto call originate line interface and then transmit on the attached switched line interface.
0008 - Wrap data on switched lines. This option will dial numbers on an auto call originate interface. Answer the call on a switched line interface. Go into receive mode on the line interface that answered the call. Then transmit on the line interface attached to the auto call originate line interface to the receive line.
0009 - Dial numbers continuously on an auto-call originate

line interface.

000A - Dial numbers on an auto call originate line interface and then transmit an alternate all zeros and all ones character pattern for 128 characters, then disconnect the line address.

F031 Enter the line address of the auto call originate line interface to be used in this test. See stop code F001 for format to enter the line address.

F032 The line address you entered is either invalid or not configured as an auto call originate line. Enter the line address again as defined in stop code F031.

F033 Enter the first digit to be dialed on the auto call originate line.

Set switch D to 0 and switch E to the digit to be dialed. The digit to be dialed may be 0 through 9 for dial digits, C for the end of numbers character or D for the separator character. It should be noted that the end of numbers and separator characters are not supported by most IBM and non-IBM auto call units in the U.S.A. and should be used with caution. At this time register X'13' points to a location in storage where you (as an option) may store up to 32 bytes of dial digits and then set switches C and D to FF and press the start push button to continue. If you select this option to store the dial digits,then the first 4 bits of each byte should be 0 and the last 4 bits should be the dial digit, and you should store a X'FF' character after the last digit to be dialed. If you make any errors in entering any dial digits you will be asked to enter the first dial digit again. If you used the end of numbers character, it must be the last digit entered.

F034 Enter the next digit to be dialed.

Set switch D to 0 and switch E to digit to dial or set switches D and E to FF if last digit to dial was entered previously. See stop code F033 for caution on dial digits and optional use of register X'13' storage address which you may still use as an option. After you have entered the dial digits,the digits will be validated, and if any digit is invalid, you will be asked to enter the first dial digit again. This manual intervention code may be repeated up to 31 times to get a total of 32 digits.

F035 Enter the transmit line address to be used in this test. See stop code F001 for format to use.

F036 The transmit line address you entered is invalid or not configured as a line that can run in transmit mode. Enter the transmit line address again as defined in stop code F035.

F037 The transmit line address you entered can not be used with the switched line and/or auto call originate test option you selected. Enter the transmit line address again as defined in stop code F035.

F049 Options for running wrap

Switch B enter the following options

0=1st installed oscillator (150 BPS)
1=2nd installed oscillator (600 BPS)
2=3rd installed oscillator (1200 BPS)
3=4th installed oscillator (optional)
4=Data Rate select
8=external clock
C=external clock and data rate select

Switch C

0=no request
4=auto call

Switches D and E

00=No request
01=Transmit Continuously - no receive line
02=Transmit on one line; Receive on another, then swap transmit and receive and report
03=Transmit and Receive continuously from one line to another

F050 Enter transmit line address

High order Hex digit of requested address specifies type of wrap as follows:

SDLC - Switches
BCDE
8XXX Internal Scanner Diagnostic Wrap
EXXX Line Set Diagnostic Wrap(DM/Not DTR)
FXXX Modem Wrap(DM/DTR) For modems that use the Modem Wrap signal
DXXX Normal (DTR/Not DM) An external wrap facility must be provided to wrap data with this option

BSC - Switches
BCDE
0XXX Internal Scanner Diagnostic Wrap

6XXX Line Set Diagnostic Wrap(DM/Not DTR)
7XXX Modem Wrap(DM/DTR) For modems that use the Modem Wrap signal
5XXX Normal (DTR/Not DM) An external wrap facility must be provided to wrap data with this option

Note: Refer to manual intervention stop code F001 for switches C, D and E settings.

F051 Line not valid or not installed.

F052 Enter Receive Line address

Enter address in same format as defined in the F050 manual intervention stop code.

F053 Line not valid or not installed.

F055 Enter options for routine X7B7; see routine heading for selections.

F056 Enter the transmit line address for routine X7B7; see stop code F001 for format.

F057 Enter the receive line address for routine X7B7; see stop code F001 for format.

F058 Enter the high speed local attachment oscillator frequency and line address for routine X7A7; see routine heading for selections.

F059 Disconnect the external wrap facility for routine X7B7; see routine heading for selections.

F060 Connect a precision Volt meter across any B06 pin and any D08 pin on the E2 board to measure -4.0 Volts dc. Run the routine, it should run successfully. Adjust the -4.0 Volts to -3.6 Volts with the potentiometer on the H2 card on the 01D gate (refer to Page D-230/D-580 in IBM 3705 Communications Controller Theory Maintenance Manual, SY27-0107.) The routine should run with the voltage adjusted to -3.6 Vdc, replace defective cards causing error stops. When the routine runs successfully at -3.6 Vdc, adjust the voltage to -4.4 Vdc, again the routine should run without errors. Replace any cards causing error stops.

Routine X7F1 through X7F6 will loop as long as ADDRESS/DATA switch E is set to any value other than 0. If you do not wish for the routine to loop, ensure that this switch is set to 0.

CHAPTER 8.0: TYPE 4 CHANNEL ADAPTER SYMPTOM INDEX

ROUTINE DESCRIPTION

This routine ensures that the adapter being tested can be selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X901	0X01 E4F2	PA108	H-120

Attempt to select type 4 channel adapter under test failed. Register X'14' contains the results of the IN X'67' executed following selection.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X901	0X02 E4F2	PA108	H-120

Attempt to select type 4 channel adapter under test failed. Register X'14' contains the results of the IN X'77' executed following selection.

X902 Channel Adapter Disable Test

ROUTINE DESCRIPTION

Ensures that the channel adapter can be disabled

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X902	0X01 E4P2	PB103	H-120

Channel interface was not disabled.

X903 Clear Adapter With Diagnostic Reset

ROUTINE DESCRIPTION

Ensures that Diagnostic Reset clears the Channel Adapter. Program does an Output X'67' with bit 0.4 on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X903	0X02 E4Q2	PH107	H-120	any bits
	E4K2	PF103	H-050	bit 0.6
	E4N2	PC105		bits 0.1, 0.2, 0.7
	E4L2	PE102		bits 0.0, 0.3, 0.5

Register X'60' did not clear.

EFROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X903	0X04 E4Q2	PH107	H-120	any bits
	E4L2	PE103	H-070	bits 0.0-0.4, 1.0, 1.5-1.7
	E4T2	PG102		bits 0.6, 0.7
	E4N2	PC104		bits 0.5, 1.1, 1.3
	E4K2	PF104		bits 1.2, 1.4

Register X'62' did not clear.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X903	0X08 E4Q2	PH107	H-120	any bits
	E4M2	PD108	H-100	bits 0.0, 0.1, 0.4, 0.5
	E4T2	PG102		bits 0.6, 0.7

Register X'66' did not clear.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X903	0X09	E4Q2	PH107	H-120	any bits
		E4K2	PF104	H-110	bits 1.1-1.5
		E4F2	PA108		bits 1.6, 1.7

Register X'67' did not clear. Bits 1.0-1.6 are checked.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X903	0X0A	E4Q2	PH107	H-120	any bits
		E4H2	PL102	H-130	bit 0.0
		E4E2	PQ104		bit 0.1

Register X'6C' did not clear. Bits 0.0 and 0.1 are checked.

X904 Register X'63' (SSAR) All Zeros Test

ROUTINE DESCRIPTION

This routine verifies that all Zeros can be loaded into register X'63'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X904	0X0A	E4M2	PD107	H-080
		E4P2	PB106	
		E4K2	PF102	

Unable to set register X'63' to X'0000'.

X905 Register X'63' (SSAR) All Ones Test

ROUTINE DESCRIPTION

This routine verifies that all bits can be set on in register X'63'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X905	0X0B	E4M2	PD107	H-080
		E4P2	PB106	
		E4K2	PF102	

Unable to set register X'63' to all ones.

X906 Register X'63' (SSAR) Alternate Bits Test

ROUTINE DESCRIPTION

This routine verifies that alternate bits can be set on in register X'63' via a X'5555' bit pattern followed by a X'AAAA' bit pattern.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X906	0X0C	E4M2	PD107	H-080
		E4P2	PB106	
		E4K2	PF102	

Unable to set register X'63' to X'5555'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X906	0X0D	E4M2	PD107	H-080
		E4P2	PB106	
		E4K2	PF102	

Unable to set register X'63' to X'AAAA'.

X907 Register X'63' (SSAR) Increasing Bits Test

ROUTINE DESCRIPTION

This routine tests register X'63' using a pattern of incrementing bits. The routine loops adding a bit to the pattern on each interaction.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9070X0E	E4M2	PD107	H-080
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'63' using a increasing bits pattern.

X908 Register X'63' (SSAR) Floating Zeros Test

ROUTINE DESCRIPTION

Register X'63' is tested using a floating zero pattern to ensure that extraneous bits are not set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X908 0X0F	E4M2	PD107	H-080
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'63' using the floating zeros pattern.

X909 Register X'64' (Data Register 1 and 2) All Zeros Test

ROUTINE DESCRIPTION

Register X'64' is tested with an all zero bit pattern to ensure that all bits can be set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X909 0X0A	E4M2	PD107	H-090
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'64' to X'0000'.

X90A Register X'64' (Data Register 1 and 2) All Ones Test

ROUTINE DESCRIPTION

Register X'64' is tested with an all bit pattern to ensure that all bits can be set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X90A 0X0B	E4M2	PD107	H-090
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'64' to X'FFFF.

X90B Register X'64' (Data Register 1 and 2) Alternate Bits Test

ROUTINE DESCRIPTION

Register X'64' is tested with X'5555' followed by X'AAAA' to ensure that no interaction between bits occurs.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X90B 0X0C	E4M2	PD107	H-090
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'64' to X'5555'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X90B 0X0D	E4M2	PD107	H-090
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'64' to X'AAAA'.

X90C Register X'64' (Data Register 1 and 2) Floating Zeros Test

ROUTINE DESCRIPTION

Register X'64' is checked with a floating zero bit pattern to verify that extraneous bits are not set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X90C 0X0E	E4M2	PD107	H-090
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'64' using the floating zero pattern.

X90D Register X'64' (Data Register 1 and 2) Increasing Bits Test

ROUTINE DESCRIPTION

Register X'64' is tested using a bit pattern with an increasing number of bit.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X90D 0X0F	E4M2	PD107	H-090
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'64' when using the increasing bits pattern.

X90E Register X'65' (Data Register 3 and 4) All Zeros Test

ROUTINE DESCRIPTION

Register X'65' is tested with an all zero bit pattern to ensure that all bits can be set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X90E 0X0A	E4M2	PD107	H-090
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'65' to X'0000'.

X90F Register X'65' (Data Register 3 and 4) All Bits Test

ROUTINE DESCRIPTION

Register X'65' is tested with an all bit pattern to ensure that all bits can be set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X90F 0X0B	E4M2	PD107	H-090
	E4P2	PB106	
	E4K2	PF102	

Unable to set register X'65' to X'FFFF'.

X910 Register X'65' (Data Register 3 and 4) Alternate Bits Test

ROUTINE DESCRIPTION

Register X'65' is tested with X'5555' followed by X'AAAA' to ensure that no interaction between bits occurs.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X910	0X0C	E4M2	PD107	H-090
		E4P2	PB106	
		E4K2	PF102	

Unable to set register X'65' to X'5555'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X910	0X0D	E4M2	PD107	H-090
		E4P2	PB106	
		E4K2	PF102	

Unable to set register X'65 to X'AAAA'.

X911 Register X'65' (Data Register 3 and 4) Floating Zero Test

ROUTINE DESCRIPTION

Register X'65' is tested with a floating Zero bit pattern to ensure that extraneous bits are not set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X911	0X0E	E4M2	PD107	H-090
		E4P2	PB106	
		E4K2	PF102	

Unable to set register X'65' when using the floating zeros pattern.

X912 Register X'65' (Data Register 3 and 4) Increasing Bits Test

ROUTINE DESCRIPTION

Register X'65' is tested using a bit pattern with an increasing number of bits on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X912	0X0F	E4M2	PD107	H-090
		E4P2	PB106	
		E4K2	PF102	

Unable to set register X'65' when using a growing bits pattern.

X913 NSC Status Register All Bits Test

ROUTINE DESCRIPTION

This routine verifies that all bits in byte 1 of Register X'66' (NSC Status Register) can be set on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X913	0X0B	E4T2	PG101	H-100

Unable to set register X'66' to X'CF00' using output X'40CF' to register X'66'.

X914 NSC Status Register Alternate Bits Test

ROUTINE DESCRIPTION

This routine verifies that no interaction occurs between bits in byte one of register X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X914	0X0C	E4T2	PG101	H-100

Unable to set register X'66' to X'4500' using output of X'0045' to register X'66'.

ERROR CARD	FEALD	FETMM

	CODE	LOCATION	FAGENO.	FAGENO.
X914	0X0D	E4T2	PG101	H-100

Unable to set register X'66' to X'8A00' using output of X'008A' to register X'66'.

X915 NSC Status Register Floating Zeros Test

ROUTINE DESCRIPTION

This routine verifies that extraneous bits are not set on in byte 1 of register X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X915	0X0E	E4T2	PG101	H-100

Unable to set register X'66' when using the floating zero pattern.

X916 NSC Status Register Increasing Bits Test

ROUTINE DESCRIPTION

This routine tests register X'66' with bit patterns containing an increasing number of bits.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X916	0X0F	E4T2	PG101	H-100

Unable to set register X'66' using a increasing bits pattern.

X917 Data/Status Control Register All Zero Bits Test

ROUTINE DESCRIPTION

Register X'62' is tested with an all zero bit pattern to ensure that all bits can be set off.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X917	0X0A	E4L2	PE103	H-060
		E4T2	PG102	
		E4N2	PC104	

Unable to set register X'62' to X'0000'.

X918 Outbound Transfer Sequence Test

ROUTINE DESCRIPTION

This routine verifies that Outbound Data transfer sequence can be set on in Register X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X918	0X10	E4L2	PE103	H-060

Unable to set register X'62' to X'8000' using outbound transfer sequence.

X919 Inbound Transfer Sequence Test

ROUTINE DESCRIPTION

This routine verifies that Inbound Data Transfer Sequence can be set on in register X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X919	0X11	E4L2	PE103	H-060

Unable to set register X'62' to X'4000' using the inbound transfer sequence.

X91A Status Transfer Sequence Test

ROUTINE DESCRIPTION

This routine verifies that Status Transfer Sequence can be set on in register X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91A 0X12	E4L2	PE103	H-060

Unable to set register X'62' to X'2000' using ESC final status transfer sequence.

X91B NSC Channel End Transfer Sequence

ROUTINE DESCRIPTION

This routine verifies that NSC Channel End Transfer Sequence can be set on in register X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91B 0X13	E4L2	PE103	H-060

Unable to set register X62 to X'1000' when using NSC channel end transfer sequence.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91B 0X14	E4L2	PE103	H-060
	E4T2	PG101	

Unable to set register X'66' to X'0800' when setting register X'62' to X'1000' to set Channel End.

X91C NSC Final Status Transfer Sequence Test

ROUTINE DESCRIPTION

This routine verifies that NSC Final Status Transfer Sequence can be set on in register X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91C 0X15	E4L2	PE103	H-060

Unable to set register X'62' to X'0800' when register X'62' is set to X'0800' to issue NSC Final Status transfer sequence.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91C 0X16	E4T2	PG101	H-060
	E4L2	PE103	

Register X'66' is not all zeros when setting register X'62' to X'0800'.

X91D Program Requested Level 3 Interrupt Test

ROUTINE DESCRIPTION

This routine verifies that a level 3 interrupt occurs when requested by the program and that the interrupt can be reset.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91D 0X0A	E4L2	PE103	H-060

Unable to set register X'62' to X'0000' during Pre-Test. Rerun routine X917.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91D 0X20	E4T2	PG102	H-120

Unable to issue a level 3 interrupt.

X91E Suppress Out Monitor with Level 3 Interrupt Test

ROUTINE DESCRIPTION

This routine verifies that Suppress Out Monitor can be set and will cause a level 3 interrupt with the Suppress Out Monitor bit on in register X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91E 0X0A	E4L2	PE103	H-060

Unable to set register X'62' to X'0000' during Pre-Test. Rerun routine X917.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91E 0X21	E4T2	PG102	H-120

Level 3 interrupt did not occur when issuing Suppress Out Monitor.

X91F Status Service and Address Register Addressibility Test

ROUTINE DESCRIPTION

This routine verifies that setting all bits off in register X'63' does not cause bits to bet set off in registers X'64', X'65' or X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91F 0X0A	E4M2	PD107	H-080

Unable to set register X'63' to X'0000' during Pre-Test. Rerun routine X904.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91F 0X40	E4F2	PA101	H-080
	E4K2	PF101	H-090

Register X'64' is set in error when attempting to set register X'63' to X'0000'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91F 0X41	E4F2	PA101	H-080
	E4K2	PF101	H-090

Register X'65' is set in error when attempting to set register X'63' to X'0000'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X91F 0X42	E4F2	PA101	H-080
	E4K2	PF101	H-100

Register X'66' is set in error when attempting to set register X'63' to X'0000.

X920 Data Register 1 and 2 Addressibility Test

ROUTINE DESCRIPTION

This routine verifies that setting all bits off in register X'64' does not cause bits to be set off in registers X'63', X'65' or X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X920	0X0A E4M2	PD107	H-090

Unable to set register X'64' to X'0000' during Pre-Test. Rerun routine X909.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X920	0X43 E4F2	PA101	H-090
	E4K2	PF101	H-090

Register X'65' is set in error when attempting to set register X'64' to X'0000'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X920	0X44 E4F2	PA101	H-090
	E4K2	PF101	H-100

Register X'66' is set in error when attempting to set register X'64' to X'0000'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X920	0X45 E4F2	PA101	H-080
	E4K2	PF101	H-090

Register X'63' is set in error when attempting to set register X'64' to X'0000'.

X921 Data Register 3 and 4 Addressibility Test

ROUTINE DESCRIPTION

This routine verifies that setting all bits off in register X'65' does not cause bits to be set off in registers X'63', X'64' or X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X921	0X0A E4M2	PD107	H-090
	E4P2	PB106	

Unable to set register X'65' to X'0000'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X921	0X46 E4F2	PA101	H-090
	E4K2	PF101	H-100

Register X'66' is set in error when attempting to set register X'65' to X'0000'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X921	0X47 E4F2	PA101	H-080
	E4K2	PF101	H-090

Register X'63' is set in error when attempting to set register X'65 to X'0000'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X921	0X48 E4F2	PA101	H-090
	E4K2	PF101	

Register X'64' is set in error when attempting to set register X'65 to X'0000'.

X922 Status Service and Address Register Addressibility Test

ROUTINE DESCRIPTION

This routine verifies that setting all bits on in register X'63' does not cause bit to be set on in registers X'60', X'62', X'64', X'65' or X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X922	0X0B E4M2	PD107	H-080
	E4P2	PB106	

Unable to set register X'63' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X922	0X4C E4F2	PA101	H-080
	E4K2	PF101	H-090

Register X'64' is set in error when attempting to set register X'63' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X922	0X4D E4F2	PA101	H-080
	E4K2	PF101	H-090

Register X'65' is set in error when attempting to set register X'63' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X922	0X4E E4F2	PA101	H-080
	E4K2	PF101	H-100

Register X'66' is set in error when attempting to set register X'63' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X922	0X4F E4F2	PA101	H-080
	E4K2	PF101	H-050

Register X'60' is set in error when attempting to set register X'63' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X922	0X51 E4F2	PA101	H-060
	E4K2	PF101	H-080

Register X'62' is set in error when attempting to set register X'63' to X'FFFF'.

X923 Data Register 1 and 2 Addressibility Test

ROUTINE DESCRIPTION

This routine verifies that setting all bits on in register X'64' does not cause bits to be set on in registers X'60', X'62', X'63', X'65' or X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X923	0X0B E4M2	PD107	H-090
	E4P2	PB106	

Unable to set register X'64' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X923	0X52 E4F2	PA101	H-090
	E4K2	PF101	

Register X'65' is set in error when attempting to set register X'64' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X923	0X53 E4F2	PA101	H-090
	E4K2	PF101	H-100

Register X'66' is set in error when attempting to set register X'64' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X923	0X54 E4F2	PA101	H-090
	E4K2	PF101	H-050

Register X'60' is set in error when attempting to set register X'64' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X923	0X56 E4F2	PA101	H-060
	E4K2	PF101	H-090

Register X'62' is set in error when attempting to set register X'64' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X923	0X57 E4F2	PA101	H-080
	E4K2	PF101	H-090

Register X'63' is set in error when attempting to set register X'64' to X'FFFF'.

X924 Data Register 3 and 4 Addressibility Test

ROUTINE DESCRIPTION

This routine verifies that setting all bits on in register X'65' does not cause bits to be set on in registers X'60', X'62', X'63', X'64' or X'66'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X924	0X0B E4M2	PD107	H-090
	E4P2	PB106	

Unable to set register X'65' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X924	0X58 E4F2	PA101	H-090
	E4K2	PF101	H-100

Register X'66' is set in error when attempting to set register X'65' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X924	0X59 E4F2	PA101	H-050
	E4K2	PF101	H-090

Register X'60' is set in error when attempting to set register X'65' to X'FFFF'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X924	0X5B E4F2	PA101	H-060
	E4K2	PF101	H-090

Register X'62' is set in error when attempting to set register X'65' to X'FFFF'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X924	0X5C	E4F2	PA101	H-080
		E4K2	PF101	H-090

Register X'63' is set in error when attempting to set register X'65' to X'FFFF'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X924	0X5D	E4F2	PA101	H-090
		E4K2	PF101	

Register X'64' is set in error when attempting to set register X'65' to X'FFFF'.

X925 NSC Status Register Addressibility Test

ROUTINE DESCRIPTION

This routine verifies that setting X'00CF' into register X'66' does not cause any bits to be set on in registers X'60', X'62', X'63', X'64' or X'65'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X925	0X0B	E4T2	PG101	H-100

Data from register X'66' was not X'CF00' when X'00CF' was set into register X'66.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X925	0X5E	E4F2	PA101	H-100
		E4K2	PF101	H-050

Register X'60' is set when attempting to set register X'66' to X'60CF'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X925	0X60	E4F2	PA101	H-060
		E4K2	PF101	H-100

Register X'62' is set when attempting to set register X'66' to X'00CF'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X925	0X61	E4F2	PA101	H-100
		E4K2	PF101	H-080

Register X'63' is set in error when attempting to set register X'66' to X'00CF'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X925	0X62	E4F2	PA101	H-100
		E4K2	PF101	H-090

Register X'64' is set in error when attempting to set register X'66' to X'00CF'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X925	0X63	E4F2	PA101	H-090
		E4K2	PF101	H-100

Register X'65' is set in error when attempting to set register X'66' to X'00CF'.

X92E E.B. and C.S. MODE RESET via OUT X'62'

ROUTINE DESCRIPTION

1. CS MODE is established via an output of X'4000' to Reg X'6C'
2. An output of X'0100' is made to Reg X'62' to reset the mode.

   An input from Reg X'6C' is made and verification is made. The Mode bits (0 and 1 of byte 0) are zero.

3. E. B. Mode is established via an output of X'8000' to Reg X'6C'
4. Step 2 is performed.
5. The routine ends when it recognizes that the E. B. mode has been tested.
6. Error code 01 defines inability to reset C. S. Mode
   Error code 02 defines inability to reset E. B. Mode

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X92E	0X01	E4H2	PL102	H-140
	0X02	E4J2	PL103	H-130

X930 EBM Control Register - All Zeroes

ROUTINE DESCRIPTION

After disabling and resetting the CA, bits 0.0, 0.1, 0.4, 0.5, 0.6 and 0.7 of the EBM Control Reg. are set via an output X'6C'. An attempt to reset them via an OUT X'6C' is then made and the results checked. Two passes are made. The first with Bit 0.1 reset and 0.0 set. The second pass is with bit 0.0 reset and bit 0.1 set.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X930	0X01	E4H2	PL102	H-140	Bit 0.0 - Extended Buffer Mode
	0X02	E4E2	PQ104	H-140	Bit 0.1 - CS Mode Bit

Error code 0X01 is for failure occurring when 0.0 was set. Error code 0X02 is for failure when 0.1 was set.

Following an output X'6C' with all bits off, an input X'6C' indicated that one or more of the tested bits were not zero. Register X'15' indicates the bit(s) in input X'6C' that were not zero: (The parenthesized numbers refer to the failure information above)
(1) Bit 0.0 - Extended Buffer Mode
(2) Bit 0.1 - CS Mode Bit
(3) Bit 0.4 - Syn Monitor Control Latch
(4) Bit 0.5 - DLE Remember Latch
(5) Bit 0.6 - USASCII Monitor Control Latch
(6) Bit 0.7 - EBCDIC Monitor Control Latch

X932 EBM Control Register - All Ones

ROUTINE DESCRIPTION

After disabling and resetting the CA, bits 0.0, 0.4, 0.5, 0.6, and 0.7 of the EBM and CS Control Register are all reset via an output X'6C'. An attempt to set them via an OUT X'6C' is then made and the results checked. Two passes are made. The first with 0.0 set and 0.1 reset. The second with 0.0 reset and 0.1 set.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	ADDITIONAL INFORMATION
X932	0X01	E4H2	PL102	H-140	Bit 0.0 - Extended Buffer Mode
	0X02	E4E2	PQ104	H-140	Bit 0.1 - CS Mode Bit
		E4H2	PL105	H-140	Bit 0.4 - Syn Monitor Control Latch
		E4H2	PL101	H-140	Bit 0.5 - DLE Remember Latch
		E4H2	PL101	H-140	Bit 0.6 - USASCII Monitor Control Latch
		E4H2	PL101	H-140	Bit 0.7 - EBCDIC Monitor Control Latch

Error code 0X01 is for failure occurring when 0.0 was set. Error code 0X02 is for failure occurring when 0.1 was set.

Following an output X'6C' with byte 0, bits 0, 1, 4, 5, 6 and 7 on, an input X'6C' indicated that one or more of the tested bits were not set. Register X'15' indicates the bit(s) in input X'6C' that were not set: (The parenthesized numbers refer to the failure information above.)

(1) Bit 0.0 - Extended Buffer Mode
(2) Bit 0.1 - CS Mode Bit
(3) Bit 0.4 - Syn Monitor Control Latch
(4) Bit 0.5 - DLE Remember Latch
(5) Bit 0.6 - USASCII Monitor Control Latch
(6) Bit 0.7 - EBCDIC Monitor Control Latch

X934 EBM Address Register Reset

ROUTINE DESCRIPTION

After disabling and resetting the CA, extended buffer (EB) mode is set and an output X'62' is executed. This should reset the EBM address reg.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X934 0X01	E4H2	PL102	H-140

After issuing an output X'62' with bit 0.0 on, an input X'6C' indicated EB mode had been reset. Register X'14' contains the results of the input X'6C'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X934 0X02	E4H2	PL103	H-140
	E4J2	PK103	H-130

The input X'6C' issued to verify that the EBM address reg. has been reset indicated it had not. Some value other than 0 was in the "Transferred Byte Count" bits. Reg X'15' indicates which of these bits were not 0. Register X'14' contains the results of the input X'6C'.

X935 EBM Address Register - Sequencing

ROUTINE DESCRIPTION

After disabling and resetting the CA, extended buffer (EB) mode is set and an output X'62' issued to reset the EBM address register and to initiate a service cycle.

Sequential output X'6D' instructions are then issued to step the EBM address reg. A diagnostic reset (via output X'67') is issued to reset service cycle, EB mode is again set, and an input X'6C' issued to obtain the transferred byte count. The transferred byte count should provide the value in the EBM address register and should be equal to twice the number of output X'6C' instructions issued plus two.

During the first pass through this routine, one output X'6D' is executed. On each succeeding pass the number of output X'6D' instructions is increased by one until 16 output X'6D' instructions are executed.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X935 0X01	E4H2	PL102	H-140
	E4J2	PK103	H-130

After issuing an output X'62' with bit 0.0 on to initiate a service cycle and to reset the EBM address reg, an input X'6C' indicated either EB mode had been reset or some value other than 0 was in the "Transferred Byte Count" bits. If bit 0.0 of register X'15' is on, EB mode has been reset. If any other bits are in, the EBM address register was not reset. Pre-Test Error. Rerun routine X'934'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X935 0X02	E4H2	PL102	H-140

Following the diagnostic reset issued to reset service cycle, an attempt is made to set EB mode. The input X'6C' which followed indicated EB mode had not been set. Setting EB mode was previously tested in routine X'932'. Rerun that routine.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X935 0X04	E4H2	PL103	H-160

After ensuring that EB mode has been set, the transferred byte count in the input X'6C' is checked to insure that the EBM address register has stepped properly. The value in the input X'6C' did not compare with the expected value. Register X'14' contains the results of the input X'6C'.

Reg X'13' contains the expected value. This value is twice the number of output X'6D' instructions issued +2. (The address register wraps around at a value of 32 so if 16 X'6D' instructions were issued, a value of 2 will be expected.)

X936 EBM Local Store - All Zeroes

ROUTINE DESCRIPTION

After disabling and resetting the CA, EB mode is set and 16 output X'6D' instructions are executed, turning on all bits in the EBM local store array. Then, 16 more OUT X'6D's are executed to ensure that all bits in the array have been set to zero.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X936 0X01-	E4J2	PK102	H-160
0X10	E4G2	PM101	H-160

After attempting to set all bits on in the EBM Local Store array and then attempting to reset them, a position of the array was found to be non-zero. The error code indicates which halfword (in hex) was found to be non-zero, e.g., error code 0X01 indicates the first halfword (bytes 0 and 1), error code 0X02 indicates the second (bytes 2 and 3), etc., up to error code 0X10 which indicates the sixteenth halfword (bytes 30 and 31). Reg. X'14' contains the results of the input X'6D' which obtained the halfword in error. All bits should have been off. (Continuing from this error stop causes the remaining positions of the array to be verified.)

X938 EBM Local Store - Interference Pattern Test

ROUTINE DESCRIPTION

After disabling and resetting the CA, the EBM local store array is cleared to zero. Then, 16 output X'6D' instructions are executed to set each halfword of the EBM array to selected bit patterns. Following an input X'6D' to prime the array in-buffer, 16 IN X'6D's are executed to verify that each halfword was properly set.

The first pass through the routine attempts to set all bits in the array on. Next each halfword is set to X'AAAA', X'5555', X'7A7A', X'8585', X'C3C3', X'3C3C', X'EFEF' and X'1010'. Each pattern is written in all array locations and read back for verification one pattern at a time.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X938 0X01-	E4J2	PK102	H-160
0X10	E4G2	PM101	H-160

After clearing the EBM local store array, 16 output X'6D's were executed to set each halfword of the array to the specified bit pattern. An input X'6D' then primed the array in-buffer, and 16 more input X'6D's were executed to verify that each halfword had been properly set. One of these input X'6D's indicated that a halfword had not been set as expected.

The error code indicates which halfword (in hex) failed, e.g., 0X11 indicates the first halfword (bytes 0 and 1), 0X12 indicates the second (bytes 2 and 3), up to 0X20 which indicates the sixteenth (bytes 30 and 31) halfword failed. Register X'14' contains the results of the input X'6D' and register X'15' indicates which bits were in error. (Continuing from this error stop will cause the remaining positions of the array to be checked and other data patterns to be used.)

X939 EBM Local Store - Variable Data

ROUTINE DESCRIPTION

After disabling and resetting the CA, the EBM local store array is cleared to zero. Then, 16 output X'6D' instructions are executed to set each halfword of the EBM array to a /certain bit pattern. Following an input X'6D' to prime the array in-buffer, 16 IN X'6D's are executed to verify that each halfword was properly set.

The first pass through the routine sets all locations in the array to X'FFFE' and reads to verify. The zero is then floated through the pattern until X'7FFF' is reached. Each pattern is stored in all array locations and read to verify. Next, growing ones patterns starting with X'0001' and ending with X'FFFF' are stored. Each pattern is written in all locations, read back, and verified.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X939 0X01-	E4J2	PK102	H-160
0X10	E4G2	PM101	H-160

After clearing the EBM local store array, 16 output X'6D's were executed to set each halfword of the array to the specified bit pattern. An input X'6D' then primed the array in-buffer, and 16 more input X'6D's were executed to verify that each halfword had been properly set. One of these input X'6D's indicated that a halfword had not been set as expected.

The error code indicates which halfword (in hex) failed, e.g., 0X11 indicates the first halfword (bytes 0 and 1), 0X12 indicates the second (bytes 2 and 3), up to 0X20 which indicates the sixteenth (bytes 30 and 31) halfword failed. Register X'14' contains the results of the input X'6D' and register X'15' indicates which bits were in error. (Continuing from this error stop will cause the remaining positions of the array to be checked and other data patterns to be used.)

X93A EBM Local Store - Addressing

ROUTINE DESCRIPTION

Following a disable and reset of the CA, the EBM local store array is cleared and 16 consecutive OUT X'6D's executed. Each output X'6D' places the number of each byte to be set into that byte of the EBM Local Store array. Thus, bytes 0 and 1 of the array should contain X'00' and X'01', bytes 2 and 3 should contain X'02' and X'03', etc. After all bytes have been set, an input X'6D' primes the array in-buffer and each halfword checked to ensure that its bytes contain their respective numbers.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X93A	0X01-0X10	E4J2	PK103 PK102	H-160

After storing each bytes number into that byte of the EBM local store array, an input X'6D' was executed to prime the array in-buffer. Sixteen consecutive X'6D's were executed to ensure each byte had its respective number in it. One of these input X'6D's indicated that one of the bytes was incorrect.

The error code indicates which halfword (in Hex) of the EBM array contained the failing byte, e.g., 0X01 indicates the first halfword (bytes 0 and 1), 0X02 indicates the second halfword (bytes 2 and 3), up to 0X10 which indicates the sixteenth halfword (bytes 30 and 31). Register X'11' contains the expected contents of the local store bytes, register X'14' contains the results of the input X'6D', and register X'15' indicates the bits in error. (Continuing from this error stop causes the remaining local store bytes to be checked.)

X93C EBM Addressing - Reset via input X'6C'

ROUTINE DESCRIPTION

Following a disable and reset of the CA, the EBM Local Store Array is cleared and 'n' (see below) X'6D's executed, storing each bytes number into the byte being set. An IN X'6C' is then executed to reset the EBM address register and then a X'FFFF' stored via an output X'6D'. This X'FFFF' should end up being stored into bytes 2 and 3 of the array, since an input X'6C' was used to reset the address reg.

Sixteen passes are made through this routine, the first pass executes one X'6D' instruction, the second executes 2, and so forth.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X93C	0X01	E4J2 E4H2	PK102 PL103	H-150 H-140

After storing X'FFFF' into bytes 2 and 3 of the EBM array, an output X'62' is executed to reset the address register (this reset function was previously tested in routine X934), and an input X'6D' obtains the first halfword (bytes 0 and 1) of the array. This halfword should contain X'0001' but did not. Register X'14' contains the results of the input X'6D'. The byte located at the address in reg X'12' plus X'64' indicates the number of bytes stored in the array before the input X'6C' reset was executed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X93C	0X02	E4J2 E4H2	PK102 PL103	H-150 H-140

After ensuring that the first two bytes of the array were not changed, another X'6D' obtains the second halfword of the array which should contain X'FFFF' stored following the input X'6C' to reset the address register. The data was incorrect. Reg X'14' contains the actual results of the input X'6D'. The byte located at the address in register X'12' plus X'64' indicates the number of bytes stored in the array before the input X'6C' reset was issued.

X93D EBM Address Register Reset and Prime via input X'6C'

ROUTINE DESCRIPTION

This routine verifies that an input X'6C' primes the EBM Local Store Array in-buffer with the first 2 bytes of the array. After disabling and resetting the CA, the EBM local store array is cleared and X'0001' stored in bytes 0

and 1 of the array. An input X'6C' is executed followed by an input X'6D' to verify that the first two bytes have been fetched.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X93D	0X01	E4H2	PL102 H-130

The input X'6D' executed to verify that the first 2 bytes of the array have been fetched, contained other than the X'0001' stored in the first 2 bytes. Register X'14' contains the results of the input X'6D'.

X93E EBM Address Register Reset via output X'62' and output X'6C'

ROUTINE DESCRIPTION

This routine verifies that the EBM address register is reset via an output X'62' or output X'6C'. After disabling and resetting the CA, the EBM local store array is cleared and 'n' (see below) X'6D's executed, storing each bytes number into the byte being set. An output X'62' or X'6C' is then executed to reset the EBM address register and a X'FFFF' stored via an output X'6D'. This X'FFFF' should end up being stored into the first 2 bytes of the array.

Sixteen passes are made through this routine using an output X'62' to reset the address reg and then 16 more using an output X'6C'. For each output instruction, the first pass does one output X'6D', the second does 2 and so forth.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X93E	0X24	E4H2	PL103 H-140

Following an output X'62' to reset the address register and storing X'FFFF' via an OUT X'6D', an input X'6C' was executed to reset the address register and an input X'6D' to get the first 2 bytes of the array. They did not contain X'FFFF'. Register X'14' contains the results of the IN X'6D'. The byte located at the address in register X'12' plus X'64' indicates the number of bytes stored before the output X'62' reset was executed.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X93E	0XC4	E4H2	PL103 H-140

Following an output X'6C' to reset the address register and storing X'FFFF' via an output X'6D', an input X'6C' was executed to reset the address register and an input X'6D' to get the first 2 bytes of the array. They did not contain X'FFFF'. Register X'14' contains the results of the input X'6D'. The byte located at the address in reg. X'12' plus X'64' indicates the number of bytes stored before the output X'6C' reset was executed.

X940 DATA/STATUS INTERRUPTS

ROUTINE DESCRIPTION

After disabling and resetting the CA, a test is made to ensure that each of the data/status level 3 interrupts can be forced. A separate pass through the routine is made for each type data/status transfer sequence. At any of the error stops within this routine, register X'11' indicates the type of data/status interrupt being tested. They are tested in the order listed, Priority Outbound Transfer Sequence being tested last:

Byte 0, Bit 4 - NSC Final Status Transfer Byte 0, Bit 3 - NSC Channel End Transfer Byte 0, bit 2 - ESC Final Status Transfer Byte 0, bit 1 - Inbound Data Transfer Byte 0, bit 0 - Outbound Data Transfer (If byte 1, bit 5 is on, a Priority Outbound Data Transfer)

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X940	0X01	E4G2	PM103 H-230

After issuing an output X'62' to set the tested type of transfer sequence, an OUT X'67' with data of all zero's is issued to force the selected type of interrupt. After unmasking level 3 interrupts, no interrupt occurred. (The output X'67' should have caused diagnostic hardware to force the selected type interrupt.) Register X'11' indicates the type of transfer sequence being tested. (See routine description.)

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X940	0X02	E4L2	PE103 H-070

Following the occurrence of the forced level 3 interrupt, an input X'62' indicated that the level 3 interrupt received was not the data/status level 3 expected. Register X'14' contains the results of the input X'62'. Reg. X'11' indicates the type of transfer sequence being tested. (See the routine description.)

X942 Data/Status Interrupts Reset

ROUTINE DESCRIPTION

After forcing each of the data/status level 3 interrupts, a check is made to ensure that each can be reset via an output X'62'. A separate pass through the routine is made for each type data/status transfer sequence. At any of the error stops within this routine, reg. X'11' indicates the type of data/status interrupt being tested. They are tested in the order listed, Priority Outbound Transfer Sequence being tested last:
Byte 0, bit 4 - NSC Final Status Transfer
Byte 0, bit 3 - NSC Channel End Transfer
Byte 0, bit 2 - ESC Final Status Transfer
Byte 0, bit 1 - Inbound Data Transfer
Byte 0, bit 0 - Outbound Data Transfer (If byte 1, bit 5 is on, a Priority Outbound Data Transfer)

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X942	0X01	E4G2	PM103	H-230

After issuing an output X'62' to set the tested type of transfer sequence, an OUT X'67' with data of all zero's is issued to force the selected type of interrupt. After unmasking level 3 interrupts, no interrupt occurred. (The output X'67' should have caused diagnostic hardware to force the selected type interrupt.) Register X'11' indicates the type of transfer sequence being tested. (See routine description.) Pre-Test Error. Rerun routine X940.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X942	0X02	E4L2	PE103	H-070

Following the occurrence of the forced level 3 interrupt, an input X'62' indicated that the level 3 interrupt received was not the data/status level 3 expected. Reg X'14' contains the results of the input X'62'. Reg. X'11' indicates the type of transfer sequence being tested. (See the routine description.) Pre-Test Error. Rerun routine X940.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X942	0X03	E4G2	PM103	H-230

After forcing the tested type data/status level 3 interrupt, an output X'62' with byte 1, bit 6 on was issued to reset the data/status level 3 interrupt request. Level 3 interrupts were then unmasked and a check made to ensure that no level 3 interrupt condition was still pending. A level 3 interrupt did occur. Reg X'14' contains the results of the input X'77' issued when the interrupt occurred. Continuing from this error stop will cause an input X'62' to be issued and a check made to ensure none of the transfer sequence bits are still set. (See error code 0X04.) If error 0X04 does not occur after continuing from this stop, then none of those bits were set. Register X'11' indicates the type of transfer sequence being tested. (See the routine description.)

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X942	0X04	E4L2	PE103	H-070

After ensuring that no level 3 interrupt occurs after resetting the tested type transfer sequence, another check is made to ensure that none of the sequence bits remain on. An input X'62' indicated that at least one of them was still on. Register X'14' contains the results of the input X'62'. Register X'11' indicates the type of transfer sequence being tested. (See the routine description.)

X944 Force Initial Select Interrupt

ROUTINE DESCRIPTION

A test is made to ensure that an Initial Select Level 3 interrupt can be forced via an output X'67'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X944	0X01	E4G2	PM103	H-120

After issuing an output X'67' with bit 0.0 on, another output X'67' with no bits on was issued to force an Initial Select interrupt. No level 3 interrupt occurred.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X944	0X02	E4G2 E4L2	PM103 PE102	H-120

Ensure that a Initial Select interrupt from the adapter under test was received. Reg. X'14' contains the results of the input X'77' issued when the interrupt was received. Reg. X'15' indicates the bits in error:
Bit 1.0: CA-4 level 3 interrupt bit not set.
Bit 1.3: Selected type 4 channel adapter data/status level 3 set in error.
Bit 1.4: Selected type 4 channel adapter level 3 initial select not set.

X945 Reset Forced Initial Select Interrupt

ROUTINE DESCRIPTION

An Initial Select level 3 interrupt is forced and a check made to ensure that it can be reset.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X945	0X01	E4G2	PM103	H-120

After issuing an output X'67' with bit 0.0 on, another output X'67' with no bits on is issued to force an Initial Select interrupt. No level 3 interrupt occurred. Pre-Test Error. Rerun Routine X944.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X945	0X02	E4G2 E4L2	PM103 PE102	H-120

After the level 3 interrupt is received, a check is made to ensure that it was an Initial Select Interrupt from the adapter under test. Register X'14' contains the results of the input X'77' issued when the interrupt was received. Register X'15' indicates the bits in error:

Bit 1.0: CA-4 level 3 interrupt bit not set.
Bit 1.3: Selected type 4 channel adapter data/status level 3 in error
Bit 1.4: Selected type 4 channel adapter level 3 initial select not set.

Pre-Test Error. Rerun routine X944.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X945	0X03	E4G2 E4L2	PM103 PE102	H-060 H-060

After having forced an Initial Select level 3 interrupt, an output X'62' with bit 0.5 on is issued in an attempt to reset the Initial Select Interrupt. After unmasking level 3 interrupts, another interrupt occurred. Register X'14' contains the results of an input X'77' issued when the interrupt occurred:

Bit 1.3: A data/status level 3 interrupt was present.
Bit 1.4: An Initial Select interrupt was still present.

X946 Dual type 4 channel adapter Immediate Select CA #1

ROUTINE DESCRIPTION

Ensure that with the second CA selected, an output X'67' can be issued to the first CA without changing the CA selection. Program Requested Interrupt is used as the test vehicle. This routine runs only on machines with a second type 4 channel adapter defined in the CDS.

The overall operation of this routine is:

1. After selecting and disabling the first CA-4, ensure that Program Requested Interrupt is off.

2. After selecting and disabling the second CA-4, ensure that Program Requested Interrupt is off.

3. Cause a Program Requested Interrupt on the first CA-4, leaving the second one selected.

4. Allow interrupts and ensure an interrupt occurs but that input X'77' indicates the second type 4 channel adapter is still selected and Program Requested Interrupt has not been set.

5. Select the first type 4 channel adapter and verify that Program Requested Interrupt has been set.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X01 E4F2	PA108	H-120

Following an output X'67' with bit 0.5 on to select CA #1, an input X'67' indicated that CA #1 was not selected. Reg. X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X02 E4T2	PG102	H-070

After having selected the first CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Reg X'14' contains the results of the input X'62' issued after the disable. Pre-Test Error. Rerun routine 1903.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X03 E4F2	PA108	H-120

Following an output X'67' with bits 0.5 and 0.7 on to select CA #2, an input X'67' indicated that CA #2 was not selected. Register X'14' contains the results of the IN X'67'. Pre-Test Error. Rerun routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X04 E4T2	PG102	H-070

After having selected the second CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was. Register X'14' contains the results of the input X'62' issued after the reset. Pre-Test Error. Rerun routine X903.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X05 E4G2	PM102	H-230

With CA #2 selected, an output X'67' with bits 0.3 and 1.1 on was issued to set Program Requested Interrupt on the first CA without changing CA selection. Level 3 interrupts were unmasked and a check made to ensure that a level 3 interrupt did occur but that CA #2 was still selected. If bit 0.0 of reg. X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, a level 3 interrupt occurred and reg. X'14' contains the results of an input X'77' issued when the interrupt occurred. Reg. X'15' contains the bits in error:

Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: Although a level 3 interrupt occurred, input X'77' did not indicate type 4 channel adapter level 3 interrupt.

Bit 1.3: A data/status level 3 interrupt was indicated. With CA #2 still selected and the interrupt condition set on CA #1, no data/status interrupt should be indicated.)

Bit 1.4: An initial select interrupt was indicated.

Bit 1.6: CA #2 was no longer selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X06 E4G2	PM102	H-230

While CA #2 is still selected, a check is made to ensure that an input X'62' does not indicate a Program Requested Interrupt. (The Program Requested Interrupt should have been set on CA #1). Reg. X'14' contains the results of the input X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X07 E4G2	PM102	H-230

Select CA #1. An output X'67' with bit 0.5 on is issued to select CA #1 again. An input X'67' which followed indicated CA #1 had not been selected. Register X'14' contains the results of the input X'67'. Though not a pretest error, this function has previously been tested. Try rerunning routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X08 E4G2	PM102	H-230

After reselecting CA #1, interrupts are again unmasked, and a check made to ensure that a data/status level 3 interrupt from CA #1 now occurs. (The Program Requested interrupt previously set has not been reset and should still be pending.) If bit 0.0 of reg. X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, an interrupt did occur and reg. X'14' contains the results of the input X'77' issued following the interrupt. Register X'15' contains the error bits:

Bit 0.0: No level 3 interrupt occurred.
(Ignore remaining error bits.)

Bit 1.0: IN X'77' did not indicate a CA-4 level 3.

Bit 1.3: A data/status interrupt was not indicated.

Bit 1.4: An initial select interrupt was indicated.

Bit 1.6: CA #2 was still selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X946	0X09 E4T2	PG102	H-070

Following the data/status interrupt from CA #1, an input X'62' did not indicate a Program Requested Interrupt. Register X'14' contains the results of the input X'62'.

X947 Dual type 4 channel adapter Immediate Select CA #2

ROUTINE DESCRIPTION

Ensure that with the third CA selected, an output X'67' can be issued to the first CA without changing the CA selection. Program Requested Interrupt is used as the test vehicle. This routine runs only on machines with a third type 4 channel adapter defined in the CDS.

The overall operation of this routine is:

1. After selecting and disabling the first CA-4, ensure that Program Requested Interrupt is off.
2. After selecting and disabling the third CA-4, ensure that Program Requested Interrupt is off.
3. Cause a Program Requested Interrupt on the first CA-4, leaving the third one selected.
4. Allow interrupts and ensure an interrupt occurs but that input X'77' indicates the third type 4 channel adapter is still selected and Program Requested Interrupt has not been set.
5. Select the first type 4 channel adapter and verify that Program Requested Interrupt has been set.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X947	0X01 E4F2	PA108	H-120

Following an output X'67' with bit 0.5 on to select CA #1, an input X'67' indicated that CA #1 was not selected. Reg. X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X947	0X02 E4T2	PG102	H-070

After having selected the first CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Reg X'14' contains the results of the input X'62' issued after the disable. Pre-Test Error. Rerun routine 1903.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X947	0X03	E4F2	PA108	H-120

Following an output X'67' with bits 0.5 and 0.6 on to select CA #3, an input X'67' indicated that CA #3 was not selected. Register X'14' contains the results of the IN X'67'. Pre-Test Error. Rerun routine X901.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X947	0X04	E4T2	PG102	H-070

After having selected the third CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was. Register X'14' contains the results of the input X'62' issued after the reset. Pre-Test Error. Rerun routine X903.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X947	0X05	E4G2	PM102	H-230

With CA #3 selected, an output X'67' with bits 0.3 and 1.1 on was issued to set Program Requested Interrupt on the first CA without changing CA selection. Level 3 interrupts were unmasked and a check made to ensure that a level 3 interrupt did occur but that CA #3 was still selected. If bit 0.0 of reg. X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, a level 3 interrupt occurred and reg. X'14' contains the results of an input X'77' issued when the interrupt occurred. Reg. X'15' contains the bits in error:

Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: Although a level 3 interrupt occurred, input X'77' did not indicate type 4 channel adapter level 3 interrupt.

Bit 1.3: A data/status level 3 interrupt was indicated. With CA #3 still selected and the interrupt condition set on CA #1, no data/status interrupt should be indicated.)

Bit 1.4: An initial select interrupt was indicated.

Bit 1.5: CA #3 was no longer selected.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X947	0X06	E4G2	PM102	H-230

While CA #3 is still selected, a check is made to ensure that an input X'62' does not indicate a Program Requested Interrupt. (The Program Requested Interrupt should have been set on CA #1). Reg. X'14' contains the results of the input X'62'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X947	0X07	E4G2	PM102	H-230

Select CA #1. An output X'67' with bit 0.5 on is issued to select CA #1 again. An input X'67' which followed indicated CA #1 had not been selected. Register X'14' contains the results of the input X'67'. Though not a pretest error, this function has previously been tested. Try rerunning routine 1901.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X947	0X08	E4G2	PM102	H-230

After reselecting CA #1, interrupts are again unmasked, and a check made to ensure that a data/status level 3 interrupt from CA #1 now occurs. (The Program Requested interrupt previously set has not been reset and should still be pending.) If bit 0.0 of reg. X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, an interrupt did occur and reg. X'14' contains the results of the input X'77' issued following the interrupt. Register X'15' contains the error bits:

Bit 0.0: No level 3 interrupt occurred.
(Ignore remaining error bits.)

Bit 1.0: IN X'77' did not indicate a CA-4 level 3.

Bit 1.3: A data/status interrupt was not indicated.

Bit 1.4: An initial select interrupt was indicated.

Bit 1.5: CA #3 was still selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X947	0X09	E4T2	PG102	H-070

Following the data/status interrupt from CA #1, an input X'62' did not indicate a Program Requested Interrupt. Register X'14' contains the results of the input X'62'.

X948 Dual type 4 channel adapter Immediate Select CA #3

ROUTINE DESCRIPTION

Ensure that with the fourth CA selected, an output X'67' can be issued to the first CA without changing the CA selection. Program Requested Interrupt is used as the test vehicle. This routine runs only on machines with a fourth type 4 channel adapter defined in the CDS.

The overall operation of this routine is:

1. After selecting and disabling the first CA-4, ensure that Program Requested Interrupt is off.
2. After selecting and disabling the fourth CA-4, ensure that Program Requested Interrupt is off.
3. Cause a Program Requested Interrupt on the first CA-4, leaving the fourth one selected.
4. Allow interrupts and ensure an interrupt occurs but that input X'77' indicates the fourth type 4 channel adapter is still selected and Program Requested Interrupt has not been set.
5. Select the first type 4 channel adapter and verify that Program Requested Ihterrupt has been set.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X948	0X01	E4F2	PA108	H-120

Following an output X'67' with bit 0.5 on to select CA #1, an input X'67' indicated that CA #1 was not selected. Reg. X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X948	0X02	E4T2	PG102	H-070

After having selected the first CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Reg X'14' contains the results of the input X'62' issued after the disable. Pre-Test Error. Rerun routine 1903.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X948	0X03	E4F2	PA108	H-120

Following an output X'67' with bits 0.5, 0.6 and 0.7 on to select CA #2, an input X'67' indicated that CA #4 was not selected. Register X'14' contains the results of the IN X'67'. Pre-Test Error. Rerun routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X948	0X04	E4T2	PG102	H-070

After having selected the fourth CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was. Register X'14' contains the results of the input X'62' issued after the reset. Pre-Test Error. Rerun routine X903.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X948	0X05	E4G2	PM102	H-230

With CA #4 selected, an output X'67' with bits 0.3 and 1.1 on was issued to set Program Requested Interrupt on the first CA without changing CA selection. Level 3 interrupts were unmasked and a check made to ensure that a level 3 interrupt did occur but that CA #4 was still selected. If bit 0.0 of reg. X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, a level 3 interrupt occurred and reg. X'14' contains the results of an input X'77' issued when the interrupt occurred. Reg. X'15' contains the bits in error:

Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: Although a level 3 interrupt occurred, input X'77' did not indicate type 4 channel adapter level 3 interrupt.

Bit 1.3: A data/status level 3 interrupt was indicated. With CA #4 still selected and the interrupt condition set on CA #1, no data/status interrupt should be indicated.)

Bit 1.4: An initial select interrupt was indicated.

Bit 1.6: CA #4 was no longer selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X948	0X06	E4G2	PM102	H-230

While CA #4 is still selected, a check is made to ensure that an input X'62' does not indicate a Program Requested Interrupt. (The Program Requested Interrupt should have been set on CA #1). Reg. X'14' contains the results of the input X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X948	0X07	E4G2	PM102	H-230

Select CA #1. An output X'67' with bit 0.5 on is issued to select CA #1 again. An input X'67' which followed indicated CA #1 had not been selected. Register X'14' contains the results of the input X'67'. Though not a pretest error, this function has previously been tested. Try rerunning routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X948	0X08	E4G2	PM102	H-230

After reselecting CA #1, interrupts are again unmasked, and a check made to ensure that a data/status level 3 interrupt from CA #1 now occurs. (The Program Requested interrupt previously set has not been reset and should still be pending.) If bit 0.0 of reg. X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, an interrupt did occur and reg. X'14' contains the results of the input X'77' issued following the interrupt. Register X'15' contains the error bits:

Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: IN X'77' did not indicate a CA-4 level 3.

Bit 1.3: A data/status interrupt was not indicated.

Bit 1.4: An initial select interrupt was indicated.

Bits 1.5 & 1.6: CA #4 was still selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X948	0X09	E4T2	PG102	H-070

Following the data/status interrupt from CA #1, an input X'62' did not indicate a Program Requested Interrupt. Register X'14' contains the results of the input X'62'. X949 Dual type 4 channel adapter Immediate Select CA #4

ROUTINE DESCRIPTION

Ensure that with the first CA selected, an output X'67' can be issued to the second CA without changing the CA selection. Program Requested Interrupt is used as the test vehicle. This routine is run only on machines with multiple CA-4's and only when the second CA-4 is defined in the CDS.
The overall operation of this routine is:

1. After selecting and disabling the second CA-4, ensure that Program Requested Interrupt is off.

2. After selecting and disabling the first CA-4, ensure that Program Requested Interrupt is off.

3. Cause a Program Requested Interrupt on the second CA-4, leaving the first one selected.

4. Allow interrupts and ensure an interrupt occurs but that input X'77' indicates the first type 4 channel adapter is still selected and Program Requested Interrupt has not been set.

5. Select the second type 4 channel adapter and verify that Program Requested Interrupt has been set.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X01 E4F2	PA108	H-120

Following an output X'67' with bits 0.5 and 0.7 on to select CA #2, an input X'67' indicated that CA #2 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X02 E4T2	PG102	H-070

After having selected the second CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Reg. X'14' contains the results of the IN X'62' issued after the disable. Pre-Test Error. Rerun routine X903.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X03 E4F2	PA108	H-120

Following an output X'67' with bit 0.5 on to select CA #1 an input X'67' indicated that CA #1 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X04 E4T2	PG102	H-070

After having selected the first CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Register X'14' contains the results of the input X'62' issued after the reset. Pre-Test Error. Rerun routine 1903.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X05 E4G2	PM102	H-230

With CA #1 selected, an output X'67' with bits 0.3, 0.7 and 1.1 on was issued to set Program Requested Interrupt on the second CA without changing CA selection. Level 3 interrupts were unmasked and a check made to ensure that a level 3 interrupt did occur but that CA #1 was still selected. If bit 0.0 of register X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, a level 3 interrupt occurred and register X'14' contains the results of an input X'77' issued when the interrupt occurred. Register X'15' contains the bits in error:

- Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)
- Bit 1.0: Although a level 3 interrupt occurred, input X'77' did not indicate type 4 channel adapter level 3 interrupt.
- Bit 1.3: A data/status level 3 interrupt was indicated. (With CA #1 still selected and the interrupt condition set on CA #2, no data/status interrupt should be indicated.)
- Bit 1.4: An initial select interrupt was indicated.
- Bit 1.6: CA #1 was no longer selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X06 E4G2	PM102	H-230

While CA #1 is still selected, a check is made to ensure that an input X'62' does not indicate a Program Requested Interrupt. (The Program Requested Interrupt should have been set on CA #2.) Register X'14' contains the results of the input X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X07 E4G2	PM102	H-230

Select CA #2. An output X'67' with bits 0.5 and 0.7 on is issued to select CA #2 again. An IN X'67' which followed indicated CA #2 had not been selected. Register X'14' contains the results of the input X'67'. Though not a pretest error, this function has previously been tested. Try rerunning routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X08 E4G2	PM102	H-230

After reselecting CA #2, interrupts are unmasked, and a check made to ensure that a data/status level 3 interrupt from CA #2 now occurs. (The Program Requested Interrupt previously set has not been reset and should still be pending.) If the interrupt bit 0.0 of register X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, an interrupt did occur and register X'14' contains the results of the input X'77' issued following the interrupt. Reg X'15' contains the error bits:

Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: IN X'77' did not indicate a type 4 channel adapter level 3.

Bit 1.3: A data/status interrupt was not indicated.

Bit 1.4: An initial select interrupt was indicated.

Bit 1.6: CA #1 was still selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X949	0X09 E4T2	PG102	H-070

Following the data/status interrupt from CA #2, an input X'62' did not indicate a Program Requested Interrupt. Register X'14' contains the results of the input X'62'.

X94A Dual type 4 channel adapter Immediate Select CA #5

ROUTINE DESCRIPTION

Ensure that with the first CA selected, an output X'67' can be issued to the third CA without changing the CA selection. Program Requested Interrupt is used as the test vehicle. This routine is run only on machines with multiple CA-4's and only when the third CA-4 is defined in the CDS.
The overall operation of this routine is:

1. After selecting and disabling the third CA-4, ensure that Program Requested Interrupt is off.
2. After selecting and disabling the first CA-4, ensure that Program Requested Interrupt is off.
3. Cause a Program Requested Interrupt on the third CA-4, leaving the first one selected.
4. Allow interrupts and ensure an interrupt occurs but that input X'77' indicates the first type 4 channel adapter is still selected and Program Requested Interrupt has not been set.
5. Select the third type 4 channel adapter and verify that Program Requested Interrupt has been set.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X01 E4F2	PA108	H-120

Following an output X'67' with bits 0.5 and 0.6 on to select CA #3, an input X'67' indicated that CA #3 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X02 E4T2	PG102	H-070

After having selected the third CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Reg. X'14' contains the results of the IN X'62' issued after the disable. Pre-Test Error. Rerun routine X903.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X03 E4F2	PA108	H-120

Following an output X'67' with bit 0.5 on to select CA #1 an input X'67' indicated that CA #1 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X04	E4T2	PG102	H-070

After having selected the first CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Register X'14' contains the results of the input X'62' issued after the reset. Pre-Test Error. Rerun routine 1903.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X05	E4G2	PM102	H-230

With CA #1 selected, an output X'67' with bits 0.3, 0.6 and 1.1 on was issued to set Program Requested Interrupt on the third CA without changing CA selection. Level 3 interrupts were unmasked and a check made to ensure that a level 3 interrupt did occur but that CA #1 was still selected. If bit 0.0 of register X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, a level 3 interrupt occurred and register X'14' contains the results of an input X'77' issued when the interrupt occurred. Register X'15' contains the bits in error:

Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: Although a level 3 interrupt occurred, input X'77' did not indicate type 4 channel adapter level 3 interrupt.

Bit 1.3: A data/status level 3 interrupt was indicated. (With CA #1 still selected and the interrupt condition set on CA #2, no data/status interrupt should be indicated.)

Bit 1.4: An initial select interrupt was indicated.

Bit 1.6: CA #1 was no longer selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X06	E4G2	PM102	H-230

While CA #1 is still selected, a check is made to ensure that an input X'62' does not indicate a Program Requested Interrupt. (The Program Requested Interrupt should have been set on CA #3.) Register X'14' contains the results of the input X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X07	E4G2	PM102	H-230

Select CA #3. An output X'67' with bits 0.5 and 0.6 on is issued to select CA #3 again. An IN X'67' which followed indicated CA #3 had not been selected. Register X'14' contains the results of the input X'67'. Though not a pretest error, this function has previously been tested. Try rerunning routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X08	E4G2	PM102	H-230

After reselecting CA #3, interrupts are unmasked, and a check made to ensure that a data/status level 3 interrupt from CA #3 now occurs. (The Program Requested Interrupt previously set has not been reset and should still be pending.) If the interrupt bit 0.0 of register X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, an interrupt did occur and register X'14' contains the results of the input X'77' issued following the interrupt. Reg X'15' contains the error bits:

Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: IN X'77' did not indicate a type 4 channel adapter level 3.

Bit 1.3: A data/status interrupt was not indicated.

Bit 1.4: An initial select interrupt was indicated.

Bit 1.6: CA #1 was still selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94A	0X09	E4T2	PG102	H-070

Following the data/status interrupt from CA #3, an input X'62' did not indicate a Program Requested Interrupt. Register X'14' contains the results of the input X'62'.

X94B Dual type 4 channel adapter Immediate Select CA #4

ROUTINE DESCRIPTION

Ensure that with the first CA selected, an output X'67' can be issued to the fourth CA without changing the CA selection. Program Requested Interrupt is used as the test vehicle. This routine is run only on machines with multiple CA-4's and only when the fourth CA-4 is defined in the CDS.
The overall operation of this routine is:

1. After selecting and disabling the fourth CA-4, ensure that Program Requested Interrupt is off.
2. After selecting and disabling the first CA-4, ensure that Program Requested Interrupt is off.
3. Cause a Program Requested Interrupt on the fourth CA-4, leaving the first one selected.
4. Allow interrupts and ensure an interrupt occurs but that input X'77' indicates the first type 4 channel adapter is still selected and Program Requested Interrupt has not been set.
5. Select the fourth type 4 channel adapter and verify that Program Requested Interrupt has been set.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X01	E4F2	PA108	H-120

Following an output X'67' with bits 0.5, 0.6 and 0.7 on to select CA #4, an input X'67' indicated that CA #4 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine X901.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X02	E4T2	PG102	H-070

After having selected the fourth CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Reg. X'14' contains the results of the IN X'62' issued after the disable. Pre-Test Error. Rerun routine X903.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X03	E4F2	PA108	H-120

Following an output X'67' with bit 0.5 on to select CA #1 an input X'67' indicated that CA #1 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X04	E4T2	PG102	H-070

After having selected the first CA-4, it was disabled and a check made to ensure that no Program Requested Interrupt was pending. One was Register X'14' contains the results of the input X'62' issued after the reset. Pre-Test Error. Rerun routine 1903.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X05	E4G2	PM102	H-230

With CA #1 selected, an output X'67' with bits 0.3, 0.6, 0.7 and 1.1 on was issued to set Program Requested Interrupt on the fourth CA without changing CA selection. Level 3 interrupts were unmasked and a check made to ensure that a level 3 interrupt did occur but that CA #1 was still selected. If bit 0.0 of register X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, a level 3 interrupt occurred and register X'14' contains the results of an input X'77' issued when the interrupt occurred. Register X'15' contains the bits in error:
Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: Although a level 3 interrupt occurred, input X'77' did not

indicate type 4 channel adapter level 3 interrupt.

Bit 1.3: A data/status level 3 interrupt was indicated. (With CA #1 still selected and the interrupt condition set on CA #4, no data/status interrupt should be indicated.)

Bit 1.4: An initial select interrupt was indicated.

Bit 1.6: CA #1 was no longer selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X06	B4G2	PM102	H-230

While CA #1 is still selected, a check is made to ensure that an input X'62' does not indicate a Program Requested Interrupt. (The Program Requested Interrupt should have been set on CA #4.) Register X'14' contains the results of the input X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X07	B4G2	PM102	H-230

Select CA #4. An output X'67' with bits 0.5 and 0.7 on is issued to select CA #4 again. An IN X'67' which followed indicated CA #4 had not been selected. Register X'14' contains the results of the input X'67'. Though not a pretest error, this function has previously been tested. Try rerunning routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X08	B4G2	PM102	H-230

After reselecting CA #4, interrupts are unmasked, and a check made to ensure that a data/status level 3 interrupt from CA #4 now occurs. (The Program Requested Interrupt previously set has not been reset and should still be pending.) If the interrupt bit 0.0 of register X'15' is on, no level 3 interrupt occurred. If bit 0.0 is off, an interrupt did occur and register X'14' contains the results of the input X'77' issued following the interrupt. Reg X'15' contains the error bits:

Bit 0.0: No level 3 interrupt occurred. (Ignore remaining error bits.)

Bit 1.0: IN X'77' did not indicate a type 4 channel adapter level 3.

Bit 1.3: A data/status interrupt was not indicated.

Bit 1.4: An initial select interrupt was indicated.

Bit 1.6: CA #1 was still selected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94B	0X09	E4T2	PG102	H-070

Following the data/status interrupt from CA #4, an input X'62' did not indicate a Program Requested Interrupt. Register X'14' contains the results of the input X'62'.

X94C Dual type 4 channel adapter Priority Selection Test #1

ROUTINE DESCRIPTION

This routine ensures that the Automatic Priority Selection circuitry selects the CA with the highest priority interrupt pending. This routine make 6561 passes with each pass forcing one of the 9 possible interrupt conditions on each of up to 4 CA's, until all possible combinations have been tested. If interrupts of the same priority are forced, this routine ensures that the next non-selected CA is the first selected when the auto-selection takes place.

The routine functions as follows:

Set up all CA's for the first priority sequence (PRIORITY OUTBOUND) shown in table above.

1. Select and disable CA #1.
2. Set tested interrupt condition.
3. Select and disable CA #2.
4. Set tested interrupt condition.
5. Select and disable CA #3.
6. Set tested interrupt condition.
7. Select and disable CA #4.
8. Set tested interrupt condition.

9. Perform output X'67' to allow auto CA selection.
10. Allow interrupts and ensure an interrupt occurred and that CA selection has taken place.
11. Determine which CA interrupted and verify that the type interrupt received from that CA was the type forced.
12. Reset the interrupting condition.
13. Repeat 9 - 12 for the 2nd interrupt.
14. Repeat 9 - 12 for the 3rd interrupt.
15. Repeat 9 - 11 for the 4th interrupt.
16. If different priority interrupts were forced, verify that the CA with the highest priority interrupt pending was the CA that interrupted prior to the other CA's.
17. If equal priority interrupts were forced, verify that the next logical C.A. interrupts when expected.
18. Advance CA sequence and return to 1.

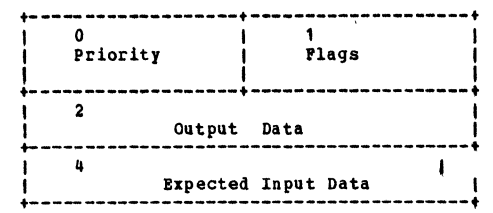
On the first pass, the priority sequence is tested on all Type 4 CAs defined in the CDS. After each pass the 1st CA is advanced to the next sequence. When the 1st CA has advanced and been tested on the last sequence, it is reset to the 1st sequence and the 2nd CA is advanced. When the 2nd CA has been tested on the last sequence the 1st and 2nd CAs are reset and the 3rd CA is advanced. In this manner all CAs are advanced through the 9 sequences. If 4 CAs are defined the test makes 6561 passes. This takes about 30 seconds. On each pass, E0XX is displayed in Display B; XX is the pass count reset at X'FF'. If the panel request is 0900, the above is run once for each CA defined.

INTERRUPT PRIORITY TABLE

NOTE: Some error stops in this routine are not listed in numerical order. They can be located as follows:

ERROR STOPS	LOCATED UNDER ERROR STOP
0X09	0X05
0X13	0X05
0X17	0X05
0X10	0X06
0X14	0X06
0X18	0X06
0X11	0X07
0X15	0X07
0X12	0X08
0X16	0X08

Used by Dual CA-4 Priority select routines.



Priority Assignments:

Priority outbound sequence	- 5
Outbound sequence	- 4
Initial select	- 3
Inbound data sequence	- 2
ESC status sequence	- 1
NSC channel end status sequence	- 1
NSC final status sequence	- 1
Program requested interrupt	- 1
Suppress out monitor interrupt	- 1

Flags

Bit 0 - 0 = Use out X'62' to set condition
1 = Use out X'67' to set condition
Bit 1 - 0 = Check register X'62'
1 = Do not check register X'62'
Bit 2 - 0 = Data/Status interrupt expected
1 = Initial selection interrupt expected
Bit 3 - 1 = Last table entry
Bits 4 - 7 - Unused

Priority Outbound Sequence

```
      DC    X'05'
      DC    X'00'
      DC    XL2'8004'
      DC    XL2'8000'

      Outbound Data Transfer Sequence

      DC    X'04'
      DC    X'00'
      DC    XL2'8000'
      DC    XL2'8000'

      Initial Selection Sequence

      DC    X'03'
      DC    X'E0'
      DC    XL2'8000'
      DC    XL2'0000'

      Inbound Data Sequence

      DC    X'02'
      DC    X'00'
      DC    XL2'4000'
      DC    XL2'4000'

      ESC Status Transfer Sequence

      DC    X'01'
      DC    X'00'
      DC    XL2'2000'
      DC    XL2'2000'

      NSC Channel End Status Transfer Sequence

      DC    X'01'
      DC    X'00'
      DC    XL2'1000'
      DC    XL2'1000'

      NSC Final Status Transfer Sequence

      DC    X'01'
      DC    X'00'
      DC    XL2'0800'
      DC    XL2'0800'

      Program Requested Interrupt

      DC    X'01'
      DC    X'80'
      DC    XL2'0040'
      DC    XL2'0400'

      Suppress Out Monitor Interrupt

      DC    X'01'
      DC    X'90'
      DC    XL2'0080'
      DC    XL2'0200'

      THROUGHOUT THIS ROUTINE REGISTER X'12' CONTAINS THE ADDRESS OF A
      SAVE AREA IN STORAGE.
      *
      X'54' BYTES INTO THE SAVE AREA IS A HALFWORD ADDRESS OF THE FIELD
      DESCRIBING THE TYPE OF INTERRUPT FORCED ON THE 1ST C.A.
      *
      X'56' BYTES INTO THE SAVE AREA IS A HALFWORD ADDRESS OF THE FIELD
      DESCRIBING THE TYPE OF INTERRUPT FORCED ON THE 2ND C.A.
      *
      X'58' BYTES INTO THE SAVE AREA IS A HALFWORD ADDRESS OF THE FIELD
      DESCRIBING THE TYPE OF INTERRUPT FORCED ON THE 3RD C.A.
      *
      X'5A' BYTES INTO THE SAVE AREA IS A HALFWORD ADDRESS OF THE FIELD
      DESCRIBING THE TYPE OF INTERRUPT FORCED ON THE 4TH C.A.
```

Byte	Description
0	Relative priority of this interrupt condition (5 being highest, 1 being lowest)
1	Flags:

Bit 0: 0=OUT X'62' used to set interrupt
1=OUT X'67' used to set interrupt

Bits 1-7: Ignore

2 & 3 Data to be used in output instruction to set interrupt (see byte 1, bit 0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94C	0X01	E4F2	PA108	H-120

Following an output X'67' with bit 0.5 on to select CA #1, an input X'67' indicated that CA #1 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94C	0X02	E4F2	PA108	H-120

Following an output X'67' with bits 0.5 and 0.7 on to select CA #2, an input X'67' indicated that CA #2 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94C	0X03	E4F2	PA108	H-120

Following an output X'67' with bit 0.5, 0.6 on to select CA #3, an input X'67' indicated that CA #3 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94C	0X04	E4F2	PA108	H-120

Following an output X'67' with bits 0.5, 0.6 and 0.7 on to select CA #4, an input X'67' indicated that CA #4 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94C	0X05			
	0X09			
	0X13			
	0X17	E4L2	PE102	H-070
		E4G2	PM103	H-120

After setting a pending interrupt condition on all 4 CA's, an output X'67' of all zeros was issued to cause auto-CA selection to occur. After unmasking level 3 interrupts, no interrupt occurred. (Refer to the routine description to determine what type interrupt was forced on each CA.)

0X05 is for the 1st interrupt expected
0X09 is for the 2nd interrupt expected
0X13 is for the 3rd interrupt expected
0X17 is for the 4th interrupt expected

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94C	0X06	E4G2	PM103	H-230
	0X10			
	0X14			
	0X18			

0X06 is for the 1st interrupt expected
0X10 is for the 2nd interrupt expected
0X14 is for the 3rd interrupt expected
0X18 is for the 4th interrupt expected

Although an interrupt occurred, see error code 0X05, neither bit 1.3 or 1.4 was on in input X'77'. This indicates that auto-selection has not taken place. (Refer to the routine description to determine the type interrupt forced on each adapter.) Register X'14' contains the results of the input X'77'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94C	0X19	E4L2	PE103	H-070
	0X21	E4G2	PM103	H-120

0X23
0X25

The interrupt occurring after auto-channel adapter selection was not the type interrupt expected. Register X'14' contains the results of the input X'77' executed at the time of the interrupt. Register X'15' indicates the bits in error in register X'14'. (Refer to the routine description to determine the type interrupt forced on each adapter.)

0X19 is for the 1st interrupt
0X21 is for the 2nd interrupt
0X23 is for the 3rd interrupt
0X25 is for the 4th interrupt

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94C	0X20	E4L2	PE103	H-070
	0X22			
	0X24			
	0X26			

If the type interrupt expected in codes 0X19, 21, 23 & 25 was a data/status interrupt, an input X'62' verifies that the interrupt was the expected type data/status interrupt. Register X'14' contains the results of the input X'62'. Reg X'15' indicates the bits in error in register X'14'. Refer to the routine description to determine the type interrupt forced on each CA. The halfword located at X'5C' plus the address in register X'12' contains the results of the input X'77' executed when the interrupt occurred. This can be used to determine the selected adapter.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94C	0X07	E4L2	PE103	H-070
	0X11			
	0X15			

After verifying that the interrupt received was the one expected, an output X'62' with bits 0.5 and 0.6 is executed to reset the interrupt condition. An input X'62' then indicated that a data/status transfer sequence was still set. Register X'14' contains the results of the input X'62'. Bits 0.4 through 0.7 should not have been on. The halfword located at X'5C' plus the address in register X'12' contains the results of the input X'77' executed when the interrupt was received. This can be used to determine which adapter is selected. Refer to the routine description to determine the type interrupt forced on each CA.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94C	0X08	E4G2	PM103	H-230
	0X12			
	0X16			

After verifying that the output X'62' reset any data/status transfer sequence bits, see error code 0X07, 0X11, or 0X15, an input X'77' is executed to verify that the received interrupt condition has been reset and that a type 4 channel adapter level 3 interrupt is still pending from the other CA. Register X'14' contains the results of the input X'77'. Either bits 1.3 or 1.4 were still on, indicating the present interrupt condition has not been reset, or bit 1.0 is no longer on indicating no other type 4 channel adapter level 3 interrupt is pending. Refer to the routine description to determine the type interrupt forced on each CA.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94C	0X27	E4G2	PM103	H-230

The 1st and 2nd interrupts were not correct. X'8000' in Reg 15 means the priority for the CA interrupting 1st was lower than the priority of the 2nd C.A. X'4000' in Reg 15 means the priorities were equal but the order of interrupts should be reversed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94C	0X28	E4E2	PM103	H-230

The 2nd and 3rd interrupts were not correct. X'8000' in Reg 15 means the priority for the CA interrupting 2nd was lower than the priority of the 3rd C.A. X'4000' in Reg 15 means the priorities were equal but the order of interrupts should have been reversed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94C	0X29	E4G2	PM103	H-230

The 3rd and 4th interrupts were not correct. X'8000' in Reg 15 means the priority for the CA interrupting 3rd was lower than the priority of the 4th C.A. X'4000' in Reg 15 means the priorities were equal but the order of interrupts should have been reversed.

The priorities of each test are found in the 1st byte (Byte) at the address found in the save area for each interrupt.

The address for the 1st interrupt priority received is found at X'4C' past the address in Reg 12. The address for the 2nd interrupt priority received is found at X'4E' past the address in Reg 12. X'50' for the 3rd interrupt and X'52' for the 4th.

X94E Dual type 4 channel adapter Priority Selection Test #2

ROUTINE DESCRIPTION

This routine ensures that the Automatic Priority Selection circuitry selects the CA with the highest priority interrupt pending. This routine make 6561 passes with each pass forcing one of the 9 possible interrupt conditions on each of up to 4 CA's, until all possible combinations have been tested. On each pass E0XX is displayed in Display B; XX is the pass count reset at X'FF'. If interrupts of the same priority are forced, this routine ensures that the next non-selected CA is the first selected when the auto- selection takes place.

The routine functions as follows:

Set up all C.A.s for the 1st priority sequence (priority outbound) shown in table in Routine 4C.

1. Select and disable CA #1.
2. Set tested interrupt condition.
3. Select and disable CA #2.
4. Set tested interrupt condition.
5. Select and disable CA #3.
6. Set tested interrupt condition.
7. Select and disable CA #4.
8. Set tested interrupt condition.
9. Perform output X'67' to allow auto CA selection.
10. Allow interrupts and ensure an interrupt occurred and that CA selection has taken place.
11. Determine which CA interrupted and verify that the type interrupt received from that CA was the type forced.
12. Reset the interrupting condition.
13. Repeat 9 - 12 for the 2nd interrupt.
14. Repeat 9 - 12 for the 3rd interrupt.
15. Repeat 9 - 11 for the 4th interrupt.
16. If different priority interrupts were forced, verify that the CA with the highest priority interrupt pending was the CA that interrupted prior to the other CA's.
17. If equal priority interrupts were forced, verify that the next logical C.A. interrupts when expected.
18. Advance CA Sequence and return to 1.

This routine is the same as Routine 4C except the order of advancement through the priority table by the CAs is reversed. The last CA defined is advanced 1st--see table and comments in RTN 4C.

THROUGHOUT THIS ROUTINE REGISTER X'12' CONTAINS THE ADDRESS OF A SAVE AREA IN STORAGE.
*
X'54' BYTES INTO THE SAVE AREA IS A HALFWORD ADDRESS OF THE FIELD DESCRIBING THE TYPE OF INTERRUPT FORCED ON THE 1ST C.A.
*
X'56' BYTES INTO THE SAVE AREA IS A HALFWORD ADDRESS OF THE FIELD DESCRIBING THE TYPE OF INTERRUPT FORCED ON THE 2ND C.A.
*
X'58' BYTES INTO THE SAVE AREA IS A HALFWORD ADDRESS OF THE FIELD DESCRIBING THE TYPE OF INTERRUPT FORCED ON THE 3RD C.A.
*
X'5A' BYTES INTO THE SAVE AREA IS A HALFWORD ADDRESS OF THE FIELD DESCRIBING THE TYPE OF INTERRUPT FORCED ON THE 4TH C.A.

Byte	Description
0	Relative priority of this interrupt condition (5 being highest, 1 being lowest)
1	Flags: Bit 0: 0=OUT X'62' used to set interrupt 1=OUT X'67' used to set interrupt Bits 1-7: Ignore
2 & 3	Data to be used in output instruction to set interrupt (see byte 1, bit 0).

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94E 0X01	E4F2	PA108	H-120	

Following an output X'67' with bit 0.5 on to select CA #1, an input X'67' indicated that CA #1 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94E 0X02	E4F2	PA108	H-120	

Following an output X'67' with bits 0.5 and 0.7 on to select CA #2, an input X'67' indicated that CA #2 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94E 0X03	E4F2	PA108	H-120	

Following an output X'67' with bit 0.5, 0.6 on to select CA #3, an input X'67' indicated that CA #3 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine 1901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94E 0X04	E4F2	PA108	H-120	

Following an output X'67' with bits 0.5, 0.6 and 0.7 on to select CA #4, an input X'67' indicated that CA #4 was not selected. Register X'14' contains the results of the input X'67'. Pre-Test Error. Rerun routine X901.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94E 0X05				
0X09				
0X13				
0X17	E4L2	PE102	H-070	
	E4G2	PM103	H-120	

After setting a pending interrupt condition on both CA's, an output X'67' of all zeros was issued to cause auto-CA selection to occur. After unmasking level 3 interrupts, no interrupt occurred. (Refer to the routine description to determine what type interrupt was forced on each CA.)

0X05 is for the 1st interrupt expected
0X09 is for the 2nd interrupt expected
0X13 is for the 3rd interrupt expected
0X17 is for the 4th interrupt expected

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94E 0X06	E4G2	PM103	H-230	
0X10				
0X14				
0X18				

0X06 is for the 1st interrupt expected
0X10 is for the 2nd interrupt expected
0X14 is for the 3rd interrupt expected
0X18 is for the 4th interrupt expected

Although an interrupt occurred, see error code 0X05, neither bit 1.3 or 1.4 was on in input X'77'. This indicates that auto-selection has not taken place. (Refer to the routine description to determine the type interrupt forced on each adapter.) Register X'14' contains the results of the input X'77'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.	
X94E 0X19	E4L2	PE103	H-070	
0X21	E4G2	PM103	H-120	
0X23				
0X25				

The interrupt occurring after auto-channel adapter selection was not the type interrupt expected. Register X'14' contains the results of the input X'77' executed at the time of the interrupt. Register X'15' indicates the bits in error in register X'14'. (Refer to the routine description to determine the type interrupt forced on each adapter.)

0X19 is for the 1st interrupt
0X21 is for the 2nd interrupt
0X23 is for the 3rd interrupt
0X25 is for the 4th interrupt

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94E	0X20	E4L2	PE103	H-070
	0X22			
	0X24			
	0X26			

If the type interrupt expected in codes 0X19, 21, 23 & 25 was a data/status interrupt, an input X'62' verifies that the interrupt was the expected type data/status interrupt. Register X'14' contains the results of the input X'62'. Reg X'15' indicates the bits in error in register X'14'. Refer to the routine description to determine the type interrupt forced on each CA. The halfword located at X'5C' plus the address in register X'12' contains the results of the input X'77' executed when the interrupt occurred. This can be used to determine the selected adapter.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94E	0X07	E4L2	PE103	H-070
	0X11			
	0X15			

After verifying that the interrupt received was the one expected, an output X'62' with bits 0.5 and 0.6 is executed to reset the interrupt condition. An input X'62' then indicated that a data/status transfer sequence was still set. Register X'14' contains the results of the input X'62'. Bits 0.4 through 0.7 should not have been on. The halfword located at X'5C' plus the address in register X'12' contains the results of the input X'77' executed when the interrupt was received. This can be used to determine which adapter is selected. Refer to the routine description to determine the type interrupt forced on each CA.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94E	0X08	E4G2	PM103	H-230
	0X12			
	0X16			

After verifying that the output X'62' reset any data/status transfer sequence bits, see error code 0X07, 0X11, or 0X15, an input X'77' is executed to verify that the received interrupt condition has been reset and that a type 4 channel adapter level 3 interrupt is still pending from the other CA. Register X'14' contains the results of the input X'77'. Either bits 1.3 or 1.4 were still on, indicating the present interrupt condition has not been reset, or bit 1.0 is no longer on indicating no other type 4 channel adapter level 3 interrupt is pending. Refer to the routine description to determine the type interrupt forced on each CA.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94E	0X27	E4G2	PM103	H-230

The 1st and 2nd interrupts were not correct. X'8000' in Reg 15 means the priority for the CA interrupting 1st was lower than the priority of the 2nd C.A. X'4000' in Reg 15 means the priorities were equal but the order of interrupts should be reversed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94E	0X28	E4E2	PM103	H-230

The 2nd and 3rd interrupts were not correct. X'8000' in Reg 15 means the priority for the CA interrupting 2nd was lower than the priority of the 3rd C.A. X'4000' in Reg 15 means the priorities were equal but the order of interrupts should have been reversed.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X94E	0X29	E4G2	PM103	H-230

The 3rd and 4th interrupts were not correct. X'8000' in Reg 15 means the priority for the CA interrupting 3rd was lower than the priority of the 4th C.A. X'4000' in Reg 15 means the priorities were equal but the order of interrupts should have been reversed.

The priorities of each test are found in the 1st byte (Byte) at the address found in the save area for each interrupt.

The address for the 1st interrupt priority received is found at X'4C' past the address in Reg 12. The address for the 2nd interrupt priority received is found at X'4E' past the address in Reg 12. X'50' for the 3rd interrupt and X'52' for the 4th.

X950 Cycle Steal Register 6F Test

ROUTINE DESCRIPTION

This routine ensures t at bits 1.4; 1.5; 1.6 and 1.7 of register X'6E' and all bits of register X'6F' can be set to ones.

The value of X'000F' is output to register X'6E'. Register X'6E' is then read and verification is made that X'000F' is received back.

The value of X'FFFF' is output to register X'6F'. Register X'6F' is then read and verification is made that X'FFFF' is received back.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X950	0X01 E4E2	PP103	H-180

Error indication upon INPUT of Cycle Steal Register 6E.

Bits expected to be set are 1.4; 1.5; 1.6 and 1.7.

Results of input should be in Register X'14'. Bit in error should be in Register X'15'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X950	0X02 E4D2	PP101	H-180

Error indication upon input of cycle steal register X'6F'.

All bits are expected to be set. Bits in error should be in Register X'15'. Results of the input are in Register X'14'.

X952 Cycle Steal Address and Outbound data transfer Test

ROUTINE DESCRIPTION

This routine tests for the proper functioning of the cycle steal address registers, X'6E' and X'6F', and for the transfer of data from memory to the Data Buffer register X'6D'.

On successive passes, cycle steal operation is executed in diagnostic mode. Starting with a 2 byte cycle steal each cycle steal is incremented by 2 until 256 bytes are transferred in the last pass.

On each pass, cycle steal operation is requested via an to register X'6C', the data out address is output to register X'6E' and register X'6F', Outbound transfer is requested via output X'62' and the cycle steal is initiated by outputs to register X'67'.

Output X'67' is executed on each pass once for each byte in the count in register X'6C'.

The resulting cycle steal address in registers X'6E' and X'6F', when in cycle steal mode, is 2 bytes higher than when in normal cycle steal mode. With this in mind, the cycle steal address is checked on each pass to be 2 bytes higher than normal, and the data in register 6D is compared with data that is 2 bytes passed that data normally expected.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X952	0X01 E4E2	PP103	H-180
	E4D2	PP101	H-180

Cycle steal addr error. Value obtained from register X'6F' is in Register X'14'. Address expected is in Register X'13'. Bit(s) in error in Register X'15'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X952	0X02 E4J2	PK102	H-160

Cycle steal data error. Value obtained from register X'6D' in register X'14'. Value expected from register X'6D' in register X'13'. Bits in error in register X'15'.

X954 Cycle Steal address and Inbound data transfer test

ROUTINE DESCRIPTION

This routine tests for the proper functioning of the cycle steal address registers X'6E' and X'6F' and for the transfer of data from the buffer register X'6D' to memory.

On successive passes, cycle steal operations are executed. The byte count of each cycle steal is incremented by 2, from 2 to 256 bytes.

On each pass, the cycle steal operation is requested via an output to register X'6C', the data in address is output to registers X'6F' and X'6E', Inbound transfer is requested via an output to register X'62' and outputs register X'67'. Register X'67' is output the number of times equal to the cycle steal count.

After each operation, the cycle steal address is verified to have incremented by the same value of the cycle steal count and the data in memory is verified to be that from the buffer register X'6D'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X954	0X01	E4E2	PP103	H-180
		E4D2	PP101	H-180

Cycle steal addr error. Value obtained from register X'6F' is in register X'14'. Address expected is in register X'13'. Bits in error are in register X'15'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X954	0X02	E4J2	PK102	H-180

Cycle steal data error value obtained from memory in register X'14'. Value expected in memory in register X'13'. Bits in error in register X'15'.

X955 CYCLE STEAL ADDRESS AND INBOUND DATA TRANSFER TEST (TO AN ODD ADDRESS)

ROUTINE DESCRIPTION

This routine tests for the proper functioning of the cycle steal address registers X'6E' and X'6F' and for the transfer of data from the buffer register X'6D' to an odd address in memory.

Only one pass is made for a one byte inbound data transfer to an odd address. Should odd addressing fail, a level 1 interrupt may occur. An indication of this would be X955 in the panel 'A' lights, and 0000 in the 'B' lights. If the above occurs, a failure did occur. Put the FUNCTION SELECT SWITCH to POSITION 5 and press START. This should cause one or more of the following error displays to be presented to the panel lights. If the error occurs without the level 1 interrupt, then one or more of the following displays will be the first failure indication.

This routine tests CSAR BYTE 1 BIT 7 (1.7). Should the card calls not prove to correct the problem, scoping the bit on the OUTBUS may be helpful. SEE THEORY-MAINTENANCE SY27-0107, PAGE H-340.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X955	0X01	E4E2	PP103	H-180
		E4D2	PP101	H-180

Cycle steal addr error. Value obtained from register X'6F' is in register X'14'. Address expected is in register X'13'. Bits in error are in register X'15'.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X955	0X02	E4J2	PK102	H-180

Cycle steal data error value obtained from memory in register X'14'. Value expected in memory in register X'13'. Bits in error in register X'15'.

X956 Cycle Steal Outbound Odd-Even Count and Address Test

ROUTINE DESCRIPTION

This test verifies proper performance of the cycle steal operation whether count or memory address is odd or even.

This test is mode up of 4 passes. The first is an outbound transfer of 3 bytes from an even address.

On the second pass, the address is made odd.

On the third pass, the count is made even, and of the fourth pass the address is made even.

On each pass, cycle steal registers X'6E' and X'6F' are verified to be incremented as expected. The anticipated data from memory is verified to be in register X'6D'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X956	0X01	E4D2	PP104 H-170

The cycle steal address from register X'6F' in error on a 3 byte transfer.

Register X'14' contains the data from register X'6F'. Register X'15' contains the bits of register X'14' that are in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X956	0X02	E4D2	PP104 H-170

The cycle steal address from register X'6F' in error on a 4 byte transfer.

Register X'14' contains the data from register X'6F'. Register X'15' contains the bits of register X'14' that are in error.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X956	0X03	E4D2	PP104 H-170

Data error on outbound 3 byte cycle steal transfer. Data expected is in register X'14'. Bits in error is in register X'15'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X956	0X04	E4D2	PP104 H-170

Data error on outbound 4 byte cycle steal transfer. Data expected is in register X'14'. Bits in error is in register X'15'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X957	0X01	1AB4-T2	CN001

CUC value is not correct after cycle steal operation.
Reg X'14' = Actual CUC value
Reg X'15' = Bits in error
Reg X'16' = Expected CUC value

X957 CYCLE UTILIZATION COUNTER TEST

This test verifies proper incrementing of the CUC from cycle steal cycles by the adapter under test. CUC value represents a combination of cycle steal and instruction cycles. CCU operation of the CUC for I1, I2 and I3 cycles has been verified in the CCU diagnostic routines.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X958 Type 4 Channel Adapter extended buffer test 1

ROUTINE DESCRIPTION

EBM LOCAL STORE _ DATA INTERFERENCE TEST NUMBER 1

In this test 1 position of the buffer is written into, and the remaining positions are read and verified to be unchanged. The position written is advanced on consecutive passes.

All type 4 channel adapter IFTs should have been run prior to running this routine.

If an error is detected, the channel adapter card E4J2 is assumed bad.

Do not attempt to loop on error. This routine is not designed to loop on error.

To thoroughly test the extended buffer for defective HDB modules, the -4.0 Volts dc must be varied to -3.6 and -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

Approximate run time is 1/2 second.

STOP
CODE

X958 F001 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E4 board. Adjust the voltage to -3.6 and run the routine several times. Replace channel adapter card if error is detected. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace channel adapter card if failure occurs. Restore the voltage to -4.0 before returning the controller to the customer.

TESTING RECOMMENDATION:

1. During the option step of routine selection, make the ROUTINE LOOP request VIA X'10' in the D and E switches.
2. At the Manual Intervention STOP, 'F001' IN THE 'B' LIGHTS;
   a. Adjust the -4 volts as desired.
      (NOTE: FAULT MAY OCCUR WITH OUT VARYING VOLTAGE)
   b. Enter CC in the D and E switches.
3. Put the Function switch to Function 5 position, and press START.

'CC' in the D and E switches causes the routine to BY-PASS subsequent M.I. stops.
Changing the D and E switches to anything other then 'CC' will cause the next M.I. stop to occur.

STOP
CODE

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X958 0X58	E4J2	PK102	H-130 through H-160

This error is because data compare did not result after an input x'6D'.

Reg x'14' has data, the results of an input x'6D'.
Reg x'15' has data bits in error. (PICKED OR DROPPED)
Reg x'16' has data expected.

X959 Type 4 Channel Adapter extended buffer test 2

ROUTINE DESCRIPTION

EBM LOCAL STORE _ DATA INTERFERENCE TEST NUMBER 2.

In this test 15 positions of the buffer are written into, and the remaining position is read and verified to be unchanged. The position read and verified is advanced on consecutive passes.

All type 4 channel ad pter IPTs should have been run prior to running this routine.

If an error is detected, the channel adapter card E4J2 is assumed bad.

Do not attempt to loop on error. This routine is not designed to loop on error.

To thoroughly test the extended buffer for defective HDB modules, the -4.0 Volts dc must be varied to -3.6 and -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

Approximate run time is 3 and 1/2 minutes.

STOP
CODE

X959 F001 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E4 board. Adjust the voltage to -3.6 and run the routine several times. Replace channel adapter card if error is detected. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace channel adapter card if failure occurs. Restore the voltage to -4.0 before returning the controller to the customer.

TESTING RECOMMENDATION:

1. During the option step of routine selection, make the ROUTINE LOOP request VIA X'10' in the D and E switches.
2. At the Manual Intervention STOP, 'F001' IN THE 'B' LIGHTS;
   a. Adjust the -4 volts as desired.
      (NOTE: FAULT MAY OCCUR WITH OUT VARYING VOLTAGE)
   b. Enter CC in the D and E switches.
3. Put the Function switch to Function 5 position, and press START.

'CC' in the D and E switches causes the routine to BY-PASS subsequent M.I. stops.
Changing the D and E switches to anything other then 'CC' will cause the next M.I. stop to occur.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X959 0X59	E4J2	PK102	H-130 through H-160

This error is because data compare did not result after an input x'6D'.

Reg x'14' has data, the results of an input x'6D'.
Reg x'15' has data bits in error. (PICKED OR DROPPED)
Reg x'16' has data expected.

X95A Type 4 Channel Adapter extended buffer test 3

ROUTINE DESCRIPTION

EBM LOCAL STORE DATA INTERENCE TEST NUMBER 3.

This routine writes X'0000' through x'FFFC' into consecutive positions of the extended buffer.

In this test 1 position of the buffer is written into, and the remaining positions are read and verified to be unchanged. The position written is advanced on consecutive passes.

All type 4 channel adapter IFTs should have been run prior to running this routine.

If an error is detected, the channel adapter card E4J2 is assumed bad.

Do not attempt to loop on error. This routine is not designed to loop on error.

To thoroughly test the extended buffer for defective HDB modules, the -4.0 Volts dc must be varied to -3.6 and -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

Approximate run time is 4 minutes.

STOP
CODE

X95A F001 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E4 board. Adjust the voltage to -3.6 and run the routine several times. Replace channel adapter card if error is detected. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace channel adapter card if failure occurs. Restore the voltage to -4.0 before returning the controller to the customer.

TESTING RECOMMENDATION:

1. During the option step of routine selection, make the ROUTINE LOOP request VIA X'10' in the D and E switches.
2. At the Manual Intervention STOP, 'F001' IN THE 'B' LIGHTS;
   a. Adjust the -4 volts as desired.
   b. Enter CC in the D and E switches.
3. Put the Function switch to Function 5 position, and press START.

'CC' in the D and E switches causes the routine to BY-PASS subsequent M.I. stops.
Changing the D and E switches to anything other then 'CC' will cause the next M.I. stop to occur.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X95A 0X5A	E4J2	PK102	H-130 through H-160

This error is because data compare did not result after an input x'6D'.

Reg x'14' has data, the results of an input x'6D'.
Reg x'15' has data bits in error. (PICKED OR DROPPED)
Reg x'16' has data expected.

X95B Type 4 Channel Adapter Extended Buffer Test 4

ROUTINE DESCRIPTION

EBM LOCAL STORE _ DATA INTERFERENCE TEST NUMBER 4.

PING PONG TEST NUMBER ONE:

Various data patterns are written and read in various positions of the extended buffer.

All Type 4 Channel Adapter IFTs should have been run prior to running this routine.

If an error is detected, the channel adapter card E4J2 is assumed bad.

Do not attempt to loop on error. This routine is not designed to loop on error.

To thoroughly test the extended buffer for defective HDB modules, the -4.0 Volts dc must be varied to -3.6 and -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

Approximate run time is 1/2 second.

STOP
CODE

X95B F001 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E4 board. Adjust the voltage to -3.6 and run the routine several times. Replace channel adapter card if error is detected. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace channel adapter card if failure occurs. Restore the voltage to -4.0 before returning the controller to the customer.

TESTING RECOMMENDATION:

1. During the option step of routine selection, make the ROUTINE LOOP request VIA X'10' in the D and E switches.
2. At the Manual Intervention STOP, 'F001' IN THE 'B' LIGHTS;
   a. Adjust the -4 volts as desired.
      (NOTE: FAULT MAY OCCUR WITH OUT VARYING VOLTAGE)
   b. Enter CC in the D and E switches.
3. Put the Function switch to Function 5 position, and press START.

'CC' in the D and E switches causes the routine to BY-PASS subsequent M.I. stops.
Changing the D and E switches to anything other then 'CC' will cause the next M.I. stop to occur.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO	
X95B	0X5B	U4J2	PK102	H-130 through H-160

This error is because data compare did not result after an input x'6D'.

Reg x'14' has data, the results of an input x'6D'.
Reg x'15' has data bits in error. (PICKED OR DROPPED)
Reg x'16' has data expected.

X95B	0X01	U4J2	PK102	H-130 through H-160

This error stop resulted because of a level 1 interrupt.

X95C Type 4 Channel Adapter Extended Buffer Test 5

ROUTINE DESCRIPTION

EBM LOCAL STORE _ DATA INTERFERENCE TEST NUMBER 5.

PING PONG TEST NUMBER TWO:

Various data patterns are written and read in various positions of the extended buffer.

All Type 4 Channel Adapter IFTs should have been run prior to running this routine.

If an error is detected, the channel adapter card E4J2 is assumed bad.

Do not attempt to loop on error. THIS ROUTINE is not designed to loop on error.

To thoroughly test the extended buffer for defective HDB modules, the -4.0 Volts dc must be varied to -3.6 and -4.4 Vdc. Refer to IBM 3705 Communications Controller Field Engineering Theory Maintenance Manual, SY27-0107 Page D-230/D-580.

Approximate run time is 1/2 second.

STOP
CODE

X95C F001 This stop occurs at the beginning of the routine to allow adjusting the -4.0 Volts dc measured at any B06 pin on the E4 board. Adjust the voltage to -3.6 and run the routine several times. Replace channel adapter card if error is detected. After running the routine with the voltage adjusted at -3.6 Vdc, adjust the voltage to -4.4 Vdc and run the routine several more times. Replace channel adapter card if failure occurs. Restore the voltage to -4.0 before returning the controller to the customer.

TESTING RECOMMENDATION:

1. During the option step of routine selection, make the ROUTINE LOOP request VIA X'10' in the D and E switches.
2. At the Manual Intervention STOP, 'F001' IN THE 'B' LIGHTS;
   a. Adjust the -4 volts as desired.
      (NOTE: FAULT MAY OCCUR WITH OUT VARYING VOLTAGE)
   b. Enter CC in the D and E switches.
3. Put the Function switch to Function 5 position, and press START.

'CC' in the D and E switches causes the routine to BY-PASS subsequent M.I. stops.
Changing the D and E switches to anything other then 'CC' will cause the next M.I. stop to occur.

ERROR CODE	CARD LOCATION	FEALD PAGENO	FETMM PAGENO
X95C 0X5C	E4J2	PK102	H-130 through H-160

This error is because data compare did not result after an input x'6D'.

Reg x'14' has data, the results of an input x'6D'.
Reg x'15' has data bits in error. (PICKED OR DROPPED)
Reg x'16' has data expected.

X95C	0X01	E4J2	PK102	H-130 through H-160

This error stop resulted because of a level 1 interrupt.

X9XX TYPE 4 CHANNEL ADAPTER COMMON ERROR STOPS

The following are common error codes that occur in common sub-routines.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	1X01	E4P2	PB103	H-120

Type 1 Channel Adapter interface was not disabled. Rerun routine X902.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	1X02	E4F2	PA108	H-120

Attempt to select type 4 channel adapter under test failed. Register X'14' contains results of input X'67'. Select bit should have been opposite to what it was. Rerun routine X901.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	1X03	E4F2	PA108	H-120

Attempt to select type 4 channel adapter under test failed. Register X'14' contains results of input X'77'. Select bit should have been opposite to what it was. Rerun routine X901.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	1X0A			

Unable to set registers to X'0000'. Rerun routines X904 through X925.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	1X0B			

Unable to set 1's in all used bit positions. Rerun routines X904 through X925.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	1X10			

Following an output instruction, an input instruction indicated requested bits were not set reset. Register X'16' contains the address of the output instruction. Reg. X'14' contains the results of the register X'15' indicates the bits in error.

The rerun routines are X904 through X925.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	1X11	E4H2	PL102	H-140

Following an output X'6C' with bit 0.0 on, an input X'6C' indicated EB mode had not been set. Reg X'14' contains the results of the input X'6C'.

The rerun routine is X932.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	1X21	E4J2	PK102	H-160
	1X30	E4G2	PM101	H-160

After setting all positions of the EB array to zeros, an input X'6D' indicated one of the positions did not contain zeros. Register X'14' contains the results of the input X'6D'. The error code indicates the failing halfword, i.e., 1X21 is the first, 1X22, the second and so on.

The rerun routine is X936.

	ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.
X9XX	2X00	E4K2	PF107	H-110

Received an unexpected Level 1 interrupt with no request bits on.

X9XX 2X01 B4L2 PM103 H-230

Received an unexpected level 3 interrupt, bit 1.4 in register X'77' was on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X02 B4L2 PE102 H-060

Unable to reset the level 3 Initial Select interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X03 E4L2 PE103 H-070

Unexpected level 3 interrupt, bit 1.3 in register X'77' was on. Neither the Suppress Out Monitor or the Program Request interrupt bits were on in register X'67'. Register X'62' should indicate the cause of interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X04 E4L2 H-060

Unable to reset the level 3 Data/Status interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X05 E4T2 PG102 H-070

Unexpected Suppress Out Monitor level 3 interrupt, bit 0.6 on in register X'77'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X06 E4T2 PG102 H-070

Unable to reset the level 3 Suppress Out Monitor interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X07 E4T2 PG102 H-070

Unexpected Program Request level 3 interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X08 E4T2 PG102 H-070

Unable to reset the level 3 Program Request interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X09 E4L2
E4T2 H-060

Unexpected level 3 interrupt from a type 1 channel adapter. There was no request bits on in register X'62'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X0A

Unknown level 3 interrupt occurred, neither input X'77' or input X'7F' indicated the source of the interrupt.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X0B

An unexpected type 4 channel adapter level 3 interrupt occurred. Reg X'09' contains the results of the input X'77'.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X1X E4K2 PF101 H-100

An unexpected level 1 interrupt occurred with the Local Store Check bit 1.3 in register X'67' on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X2X E4K2 PF101 H-100

An unexpected level 1 interrupt occurred with the CCU Outbuss Check bit 1.2 in register X'67' on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X4X E4K2 PF101 H-100

An unexpected level 1 interrupt occurred with the In/Out Instruction Accept Check bit 1.1 in register X'67' on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2X8X E4K2 PF101 H-100

An unexpected level 1 interrupt occurred with the channel. Bus-in check bit 1.0 in register X'67' on.

ERROR CODE	CARD LOCATION	FEALD PAGENO.	FETMM PAGENO.

X9XX 2XFF E4K2 PF101 H-100

Unable to reset the unexpected level 1 interrupt.

E4H2	PL105	H-140	Bit 0.4 - Syn Monitor Control Latch
E4H2	PL101	H-140	Bit 0.5 - DLE Remember Latch
E4H2	PL101	H-140	Bit 0.6 - USASCII Monitor Control Latch
E4H2	PL101	H-140	Bit 0.7 - EBCDIC Monitor Control Latch