Systems

**IBM System/360 and System/370
Direct Control and
External Interruption Features
Original Equipment
Manufacturers' Information**

IBM

Preface

This manual describes the specifications, timings, circuits and characteristics of the IBM System/360 and System/370 Direct Control and External Interruption features. The external interruption feature provides the means by which external devices may signal the CPU to gain its attention. The direct control feature includes the external interruption feature and provides an interface, exclusive of the channel, for the exchange of information between two central processing units, or between a central processing unit and external devices.

Contents

OPERATION

The direct control feature in System/360 and System/370 provides a means of communicating between two CPUs, or between a CPU and external devices. It is intended primarily for transmission of control information. A CPU communicates with external devices by using the external interruption mechanism and the write direct and read direct instructions. A byte of information and control signals are exchanged over the direct control interface lines (Figures 1 and 2).

Write Direct

The write direct instruction is used to place information on the direct control bus-out (dir-out) lines, and read direct is used to take information from the direct control bus-in (dir-in) lines. The write direct instruction causes the byte of information (8 bits) at the location designated by its operand address to be placed as static signals on the dir-out lines.

Write Direct

| 84		I_2		B_1	D_1	
0	7	8	15	16 19	20	31
Code		Immediate Operand		Operand Address		
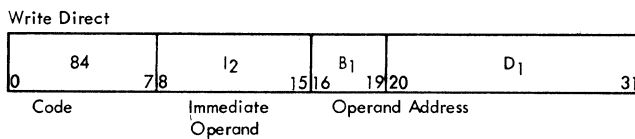
These signals may be changed at varying intervals by repeating the write direct instruction or they may be allowed to remain an indefinite period. No parity is presented with these eight bits of control information. The write direct instruction also causes the eight bits, contained in bit positions 8-15 of the instruction, to be sent out as eight timing pulses on the timing signal bus-out (sig-out) lines. Again no parity is presented. At the same time, a ninth and similar pulse is sent out on the write-out line. The leading edge of these timing pulses coincides (within skew limitations) with the leading edge of the write-out pulse, and the write-out pulse overlaps the change of the signal on the dir-out lines (Figure 3).

The timing signals and the write-out signal may be used to alert equipment to which data is to be sent. When communicating with another CPU, the timing pulses are used to cause an external signal interruption at the receiving CPU; the write-out pulse is used to ensure the validity of the control information.

Read Direct

The read direct instruction causes the information appearing on the eight dir-in lines to be placed as eight bits in the location in storage designated by the operand address (provided the hold-in signal is absent).

Read Direct

85		I_2		B_1		D_1	
0	7	8	15	16 19	20		31
Code		Immediate Operand		Operand Address			
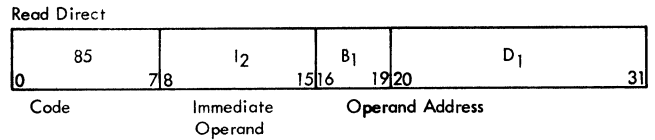
Information on the dir-in lines may not be valid while the hold-in signal is active. No parity is transmitted with the control information, however, a parity bit is generated by the CPU as the data is placed in storage.

Before accepting the control information, the read direct instruction causes the eight bits in positions 8-15 of the instruction to be sent out as eight timing pulses on the timing signal bus-out (sig-out) lines. At the same time, a ninth and similar pulse is sent out on the read-out line. The leading edges of the timing pulses and the read-out pulse must coincide within the skew limitations. (See Figure 3.)

The function of the hold-in signal is to allow the external device to inhibit (hold up) the read operation until current data has been placed on the dir-in bus. Hold-in also prevents a read operation while information on the dir-in lines is changing and therefore invalid. When communicating between CPUs, the write-out pulse of the sending CPU is received as the hold-in signal at the receiving CPU, and thereby prevents the reading of invalid information by the receiving CPU.

Devices connected to the CPU should be designed to respond quickly to the CPU's read-out signal by dropping (deactivating) the hold-in line. Note that hold-in overlaps the period when information is changing on the dir-in lines (Figure 4); therefore, time is allowed to complete a data-sending operation should the external device have one in progress.

External Interruption

The external interruption provides a means by which the CPU responds to signals from another CPU or from external equipment. These signal pulses appear on six external signal bus-in lines (sig-in-2 through sig-in-7). When these pulses occur, they are stored until honored by the CPU. The source of the signal is identified by the interruption code in bit positions 26-31 of the old program status word (PSW). See *IBM System/360 Principles of Operation*, GA22-6821, and *IBM System/370 Principles of Operation*, GA22-7000.
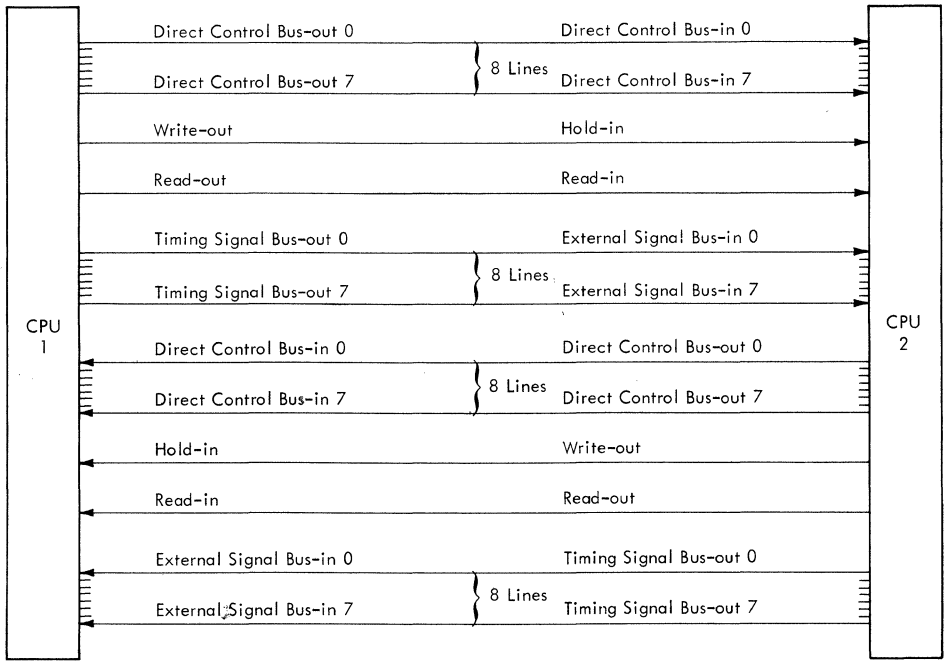
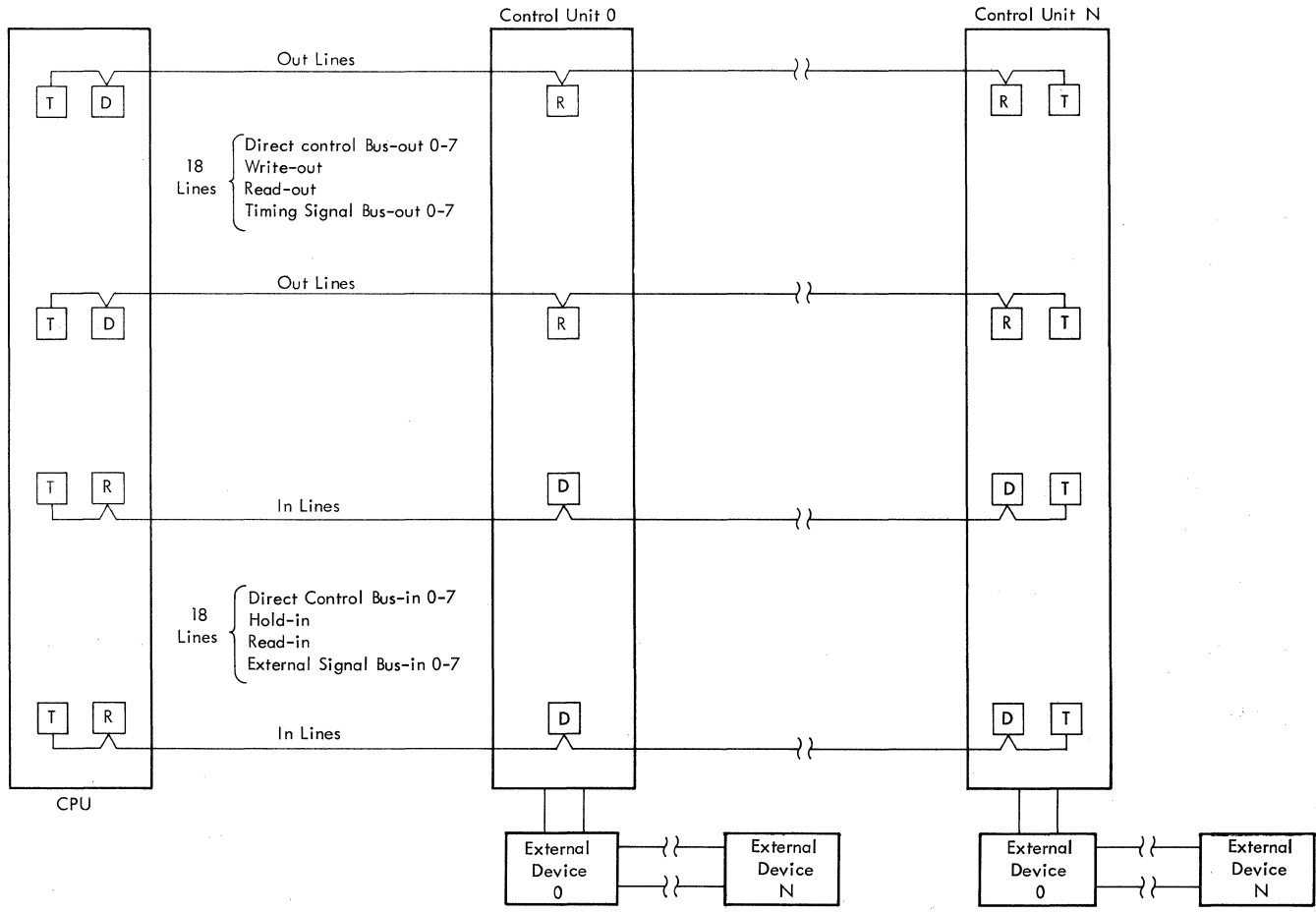Figure 1. Direct Control Interface, CPU to CPU

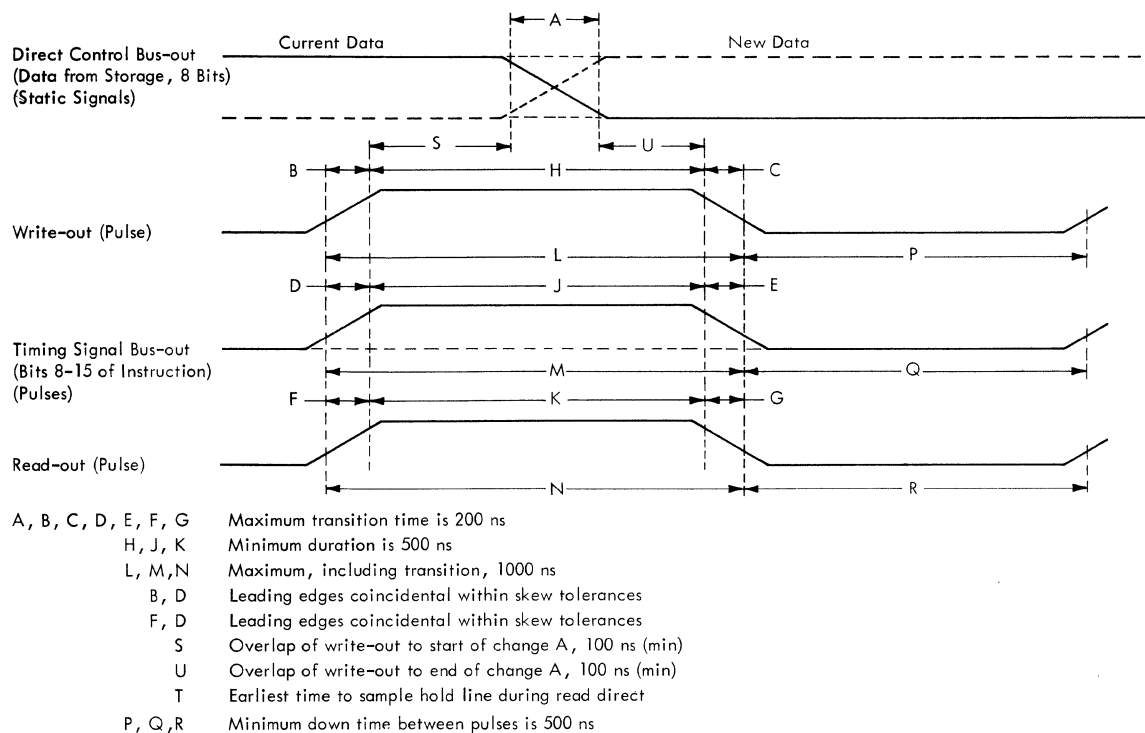Figure 2. Direct Control Interface, CPU to External Device

A, B, C, D, E, F, G   Maximum transition time is 200 ns
H, J, K   Minimum duration is 500 ns
L, M,N   Maximum, including transition, 1000 ns
B, D   Leading edges coincidental within skew tolerances
F, D   Leading edges coincidental within skew tolerances
S   Overlap of write-out to start of change A, 100 ns (min)
U   Overlap of write-out to end of change A, 100 ns (min)
T   Earliest time to sample hold line during read direct
P, Q,R   Minimum down time between pulses is 500 ns

Figure 3. Signals Originating Within the CPU

DEFINITIONS OF INTERFACE LINES

In the following signal description, the up-level is the active level; the down-level is the inactive level.

Direct Control Bus-out

The direct control bus-out is a set of eight lines from a CPU to the external equipment. The external equipment could be another CPU, in which case, direct control bus-out is connected to direct control bus-in of the other CPU.

Data on the direct control bus-out is placed only during the execution of the write direct instruction. The data on the lines represents the byte at the location designated by the operand address of the last write direct instruction. The data placed on the direct control bus-out remains valid until intentionally changed, as for example, at the execution of the next write direct. The write-out pulse overlaps a change on the direct control bus-out by 100 nanoseconds, i.e., data already on the dir-out lines is valid for at least 100 nanoseconds after the rise of the write-out pulse to its up-level and new data is valid at least 100 nanoseconds before the fall of the write-out pulse below its up-level (Figure 3).

Write-out

Write-out is a line from the CPU to external equipment. The external equipment could be another CPU, in which case, the write-out line is connected to the hold-in line of the other CPU.

The function of the write-out line is to signal the external equipment when the CPU is placing data on the dir-out lines, and to indicate that the data is, therefore, presently invalid. The down-level of write-out indicates that the data on the dir-out lines is valid. The up-level of the write-out pulse overlaps the transition of any signal on direct control bus-out by a minimum of 100 nanoseconds, and the leading edge of the write-out signal must coincide with the leading edge of the pulses on the timing signal bus-out (within skew limitations). See Figure 3.

Read-out

Read-out is a line that connects the CPU to the external equipment. The external equipment could be another CPU, in which case, the read-out line is terminated, but serves no function.

The purpose of the read-out line is to provide a means of signaling the external equipment that a read direct is being executed and that the external equipment must provide

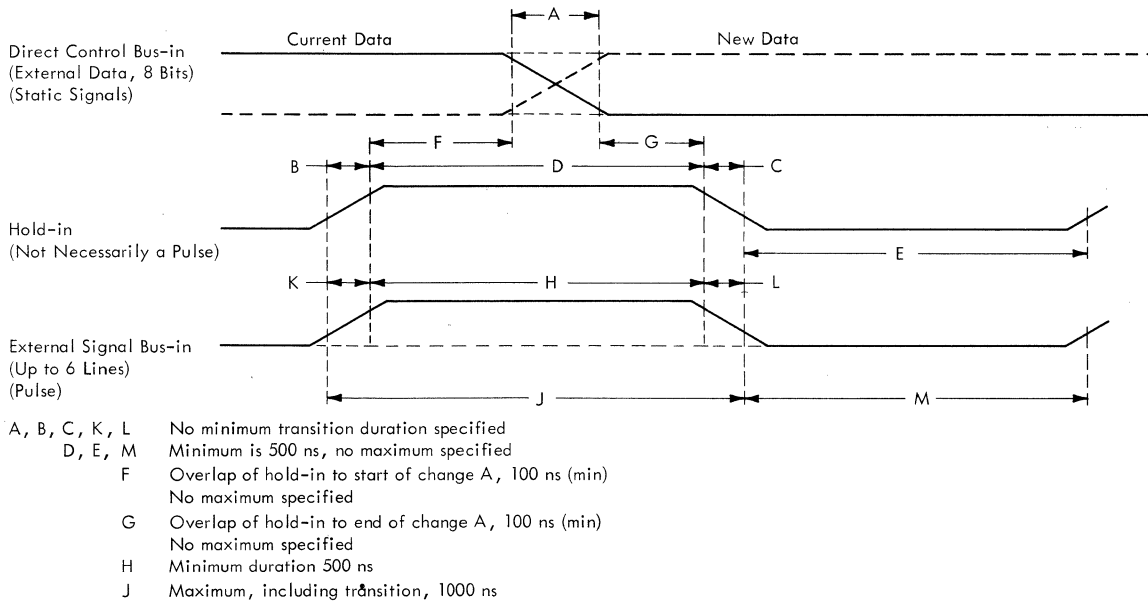|	
A, B, C, K, L	No minimum transition duration specified
D, E, M	Minimum is 500 ns, no maximum specified
F	Overlap of hold-in to start of change A, 100 ns (min)
	No maximum specified
G	Overlap of hold-in to end of change A, 100 ns (min)
	No maximum specified
H	Minimum duration 500 ns
J	Maximum, including transition, 1000 ns

Figure 4. Signals Originating Outside the CPU

valid data on the direct control bus-in, as indicated by the down-level of the hold-in signal.

Within skew limitations, the leading edge of the read-out signal must coincide with the leading edge of the pulses on the timing signal bus-out.

Timing Signal Bus-out

Timing signal bus-out is a set of eight lines from the CPU to the external equipment. The external equipment could be another CPU, in which case, the timing signal bus-out is connected to the external signal bus-in of the other CPU. The sig-out-0 and sig-out-1 lines are terminated, but serve no purpose. That is, the sig-out-0 and sig-out-1 lines of a CPU are usable with external devices but are terminated as sig-in-0 and sig-in-1 in a receiving CPU.

During a read direct or a write direct, the eight bits contained in the instruction (positions 8-15) are sent out as eight timing pulses, on the eight sig-out lines. The leading edge of the timing pulses must coincide, within skew limitations, with the leading edge of either the write-out or the read-out signal.

When the timing signal bus-out is connected to external signal bus-in of another CPU, the timing pulses on positions 2-7 cause an external signal interruption at the receiving CPU. (See "External Signal Bus-in.")

Direct Control Bus-in

The direct control bus-in is a set of eight lines from the external equipment to the CPU. The external equipment could be another CPU, in which case, the direct control

bus-in connects to the direct control bus-out of the other CPU.

The data appearing on the direct control bus-in is read by the CPU only during the execution of read direct. The data is stored in the location designated by the operand address of the read direct instruction. The CPU reads the direct control bus-in only when the direct control bus-in information is valid and after the read-out pulse occurs. The data already on the bus is valid for at least 100 nanoseconds after hold-in rises to its up-level; new data is valid at least 100 nanoseconds before hold-in falls below its up-level. When executing read direct, sampling of the hold line to determine validity of the data does not start until completion of the read-out pulse (Figure 3). Sampling of the direct control bus-in is completed within 100 nanoseconds of the time that both the read-out and hold-in lines are at a down-level.

Hold-in

Hold-in is a line from the external equipment to the CPU. The external equipment could be another CPU, in which case, the hold-in line is connected to the write-out line of the other CPU. The purpose of the hold-in signal is to prevent the CPU from reading the data from the direct control bus-in until such data is valid, or until the external device has replaced the information on direct control bus-in with current data.

The hold-in signal must be in the hold position (up-level) for at least 100 nanoseconds on either side of any signal transition on direct control bus-in; i.e., hold-in must be at

an up-level for at least 100 nanoseconds before data is invalid, and must remain up at least 100 nanoseconds after new data is valid on the direct control bus-in.

The hold-in signal must have a minimum up-level duration of 500 nanoseconds and, when at the down-level, must remain for a minimum duration of 500 nanoseconds (Figure 4).

After the read-out pulse is generated during the execution of read direct, the CPU senses for a down-level of the hold-in line so that reading of the direct control bus-in can be made, completing the instruction. Because the CPU will hang up waiting for hold-in to drop, devices connected to the CPU should be designed to respond quickly to the CPU's read-out signal by dropping (deactivating) the hold-in line. If the delay between the termination of read-out and the termination of hold-in is relatively long, serious interference with the computer program can occur.

The hold-in signal can occur at any time; it does not have to be synchronized with the read-out pulse. (It may occur before, during, after, or even as a result of either transition of the read-out pulse.)

Read-in

Read-in provides no function except as a termination for the read-out line in the CPU to CPU configuration.

External Signal Bus-in

Eight lines, sig-in-0 through sig-in-7, make up the external signal bus-in. Six of these lines provide access to the computer's external interruption mechanism. Two lines, sig-in-0 and sig-in-1, are terminated in the CPU but serve no other function. The external equipment could be another CPU, in which case, the external signal bus-in connects to the timing signal bus-out of the other CPU.

The purpose of the external signals bus is to provide a path to the external interruption mechanism of the CPU. The external interruption can occur only after the current instruction is completed and when system mask bit 7 is a one. The interruption causes the external old PSW to be stored at location 24 and an external new PSW to be fetched from location 88. As a result of an external interruption, the external signals are placed in bit locations 26-31 of the external old PSW.

The external signal requests (pulses) may occur at any time and have no relation to the timing of other signals on the direct control interface.

The requests are preserved until honored by the CPU. All pending requests are presented simultaneously when an external interruption occurs. Each request is presented only once. When several requests from one source are made before the interruption is taken, only one interruption

occurs. (Engineering Note: If a constant up-level, for any reason, appears on the external signal bus-in, it must not result in CPU hang up.)

Because of possible skew between pulses, CPU cannot guarantee that simultaneous pulses (requests) will be recognized as such. Skew may cause simultaneous requests to appear as separate requests and result in more than one interruption.

The external interruption may be used separately from the direct control and is available as a special feature on System/360 Models 30 and 44. The direct control cable, part 5372977, shown under "Direct Control Cabling" is also used for external interruption. See Figure 8.

Signal Duration

| Name | Duration (in ns) | | |
	Min Signal*	Max Signal**	Min Down Level
Write-out	500	1,000	500
Read-out	500	1,000	500
Timing Signal (Sig-out)	500	1,000	500
External Signal (Sig-in)	500	1,000	500
Hold-in	500	None	500

*Measured at up-level.
**Including transition time: from and to down-level.

Note: Transition of any signal originating in the CPU may not exceed 200 nanoseconds. See Figure 3.

Skew

Skew between any pair of pulses is expressed as a time interval between the leading edge of the leading pulse and the leading edge of the trailing pulse measured at the up-level.

The allowable skew between any pair of the eight signal-out pulses is less than 200 nanoseconds.

CONNECTOR PIN ASSIGNMENTS

Figure 5 shows the front (mating surface) view of tail-gate connectors on the CPU and the connector pin assignments. Figure 6 shows the Burndy connector pin assignments that correspond to the pin assignments shown on Figure 5. Consequently, Figures 5 and 6 indicate pin assignment of each signal at both ends of the cables (part 5372977 and 5372980) shown on Figures 8 and 9.

Some of the 40 signal lines are reserved. However, all 40 signal transmission lines, reserved and used, must be carried
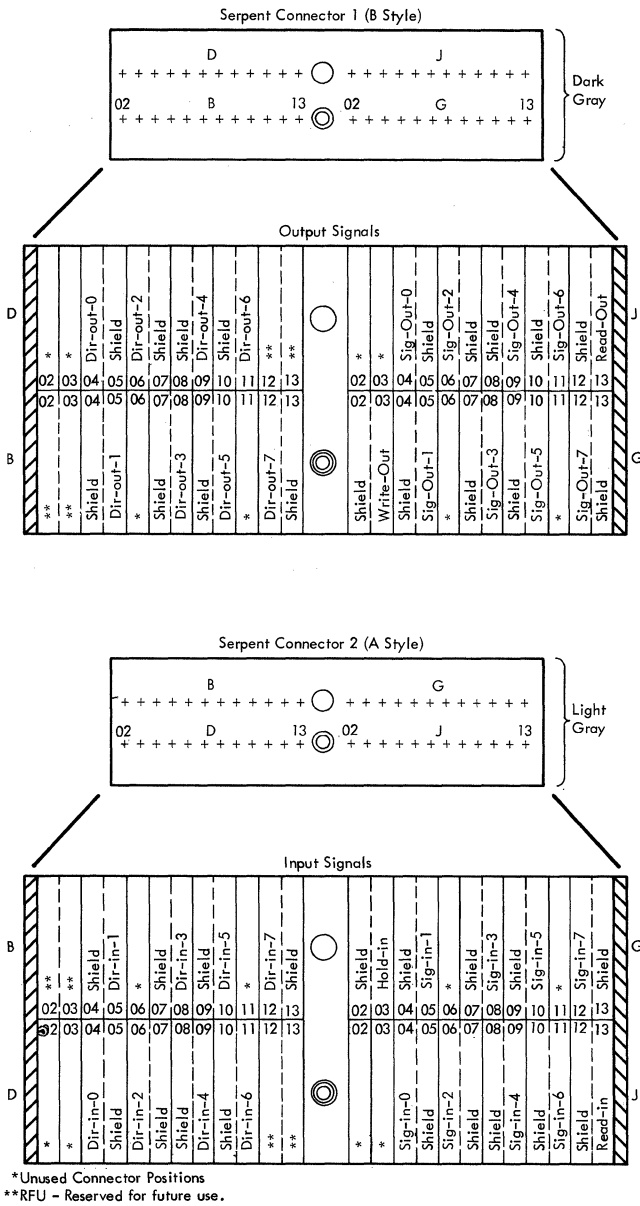
Figure 5

Serpent Connector 1 (B Style) — Dark Gray

Output Signals

Serpent Connector 2 (A Style) — Light Gray

Input Signals

*Unused Connector Positions
**RFU – Reserved for future use.

Figure 5. IBM Serpent Connector Pin Assignments

Figure 6

IBM Serpent Connector Pin Numbers	Corresponding Burndy Pin Numbers
B2 and 3	1
B4 and 5	2
B6	
B7 and 8	3
B9 and 10	4
B11	
B12 and 13	5
D2 and 3	
D4 and 5	6
D6 and 7	7
D8 and 9	8
D10 and 11	9
D12 and 13	10
G2 and 3	14
G4 and 5	15
G6	
G7 and 8	16
G9 and 10	17
G11	
G12 and 13	18
J2 and 3	
J4 and 5	19
J6 and 7	20
J8 and 9	21
J10 and 11	22
J12 and 13	23

Figure 6. Burndy Connector Pin Assignments

Power Effects

Steady State: The power-off state of a CPU or any external device must not affect any operations of other units on the interface.

Transient and Spurious Signals: Each external device must be designed so that, if proper procedures are followed, the process of individually powering up or down does not cause its interface driver or receiver circuits to generate noise on the interface signal lines.

Emergency Power Off: Refer to Systems Reference Library, *IBM Power Control Interface*, GA22-6906.

DIRECT CONTROL CABLING

Figures 7-9 illustrate possible configurations of IBM and non-IBM machines that use the direct control feature. If other configurations are desired, they may be obtained by Request Price Quotation (RPQ). Only direct control cabling is shown. All control units illustrated are non-IBM units. IBM cables supplied for the direct control feature are available in lengths up to 50 feet. Longer cables may be obtained on an RPQ basis.

Cable length may be limited by special conditions but is never to exceed a maximum line resistance of 33 ohms. The 33-ohm line resistance includes all contact resistance, internal cable resistance, and interunit cable resistance. The maximum allowable internal resistance, including all con-
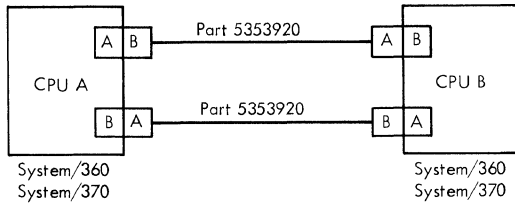
through the control units from the A (in) cable connector to the B (out) cable connector.

MAINTENANCE

For test purposes, the B (out) connector on the CPU may be connected to its A (in) connector. This allows testing of direct control operations without another CPU or an external device. Cable (part 5353920) may be used for this purpose.

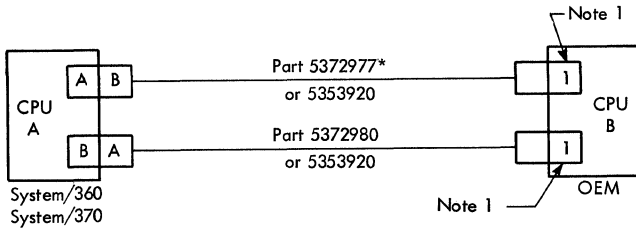Figure 7. Direct Control–CPU to CPU

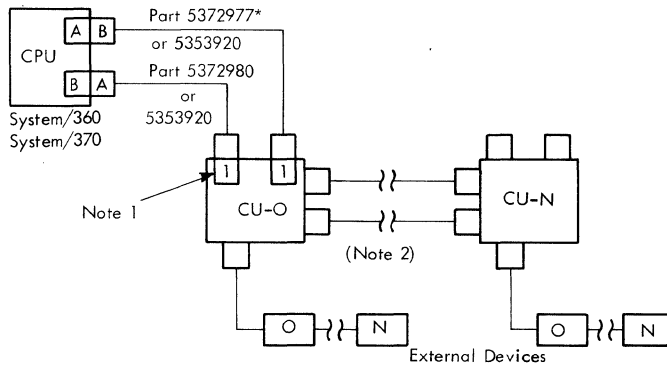Figure 8. Direct Control–CPU to OEM CPU

Figure 9. Direct Control–CPU to OEM External Devices

Notes for Figures 7-9:

1. For cables part 5372977 and 5372980, use Burndy connector ME23XR-1 on the OEM control unit. For cable part 5353920, use IBM serpent connectors. See Appendix B.

   Burndy connector No. ME23XR-1, mounted on the non-IBM unit, is supplied by the customer. If standard coaxial cable RG62A/U is used, the following parts for each ME23XR-1 connector will also be required:

Quantity	Burndy Part No.	Description
20	RC22W-6	Inner socket
20	RMX150-1	Outer male body
20	YOC180-L	Outer hyring
1	M8ND+N22RVT-2	Installation tool
1	RX4-1	Extraction tool

   Consult the local Burndy Corporation representative, or write Burndy Corporation, Richards Avenue, Norwalk, Connecticut, for terminal connector information required to use other types of cabling with the ME23XR-1 connector.

2. Only cables with part numbers shown are supplied by IBM.

   *Both part 5372977 and 5372980 are in B/M 5402263.

tact resistance, contributed by a control unit is specified as 1.5 ohms for each signal line. This resistance is measured between the incoming and the outgoing pins on the external connectors. The maximum allowable internal cable resistance offered by any CPU is 4.5 ohms.

The external interruption feature provides the means by which devices external to the system may signal the CPU to gain its attention. The external signals are transmitted to the CPU over six of the eight lines known as the external signal bus-in (Figure 10). The CPU stores the external signals until they are honored and indicates their source in the interruption code, bits 26-31, of the external old PSW.

In honoring the signals, the CPU takes an external interruption cycle. The current PSW is stored in location 24 as the external old PSW and the external new PSW from location 88 is made the current PSW. External devices are thus able to initiate the external interruption-handling routine, provided the system mask bit 7 is set to 1 in the current PSW.

An external signal request may occur at any time. Requests remain pending until honored by the CPU after the completion of the current instruction execution and before a new instruction is started. Pending requests are presented simultaneously when an external interruption occurs; each request is presented only once. When several requests from one source are made before the interruption is taken, only one interruption occurs.

SPECIFICATIONS

External signal bus-in 0 and 1 lines are terminated but are not used by the external interruption feature. The external signal bus-in 2-7 lines set bits 26-31 respectively in the external old PSW. The drivers, receivers, and terminators used are the same as those used by the direct control feature and are shown in Figures 11-13; specifications for these circuits are given in the direct control specifications, Appendix A.

Signals are described as they appear on the direct control/external interruption interface. All pulses are considered positive, the up-level being the minimum up-level defined to be a logical 1; the down-level being the maximum down-level defined to be a logical 0.

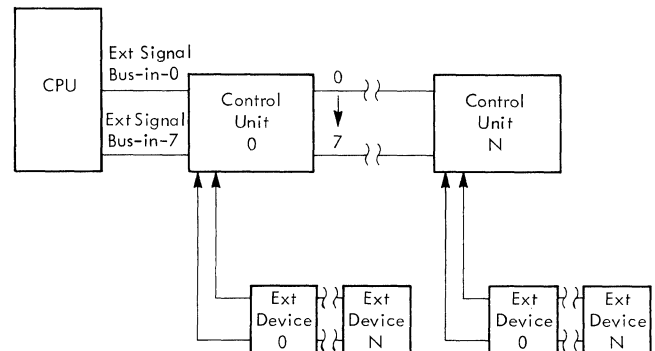The external interruption signals generated by external

Figure 10. External Interruption Feature

devices must have a minimum up-level duration of 500 nanoseconds (ns), a maximum up-level duration of 1,000 ns, and the down-level duration must be at least 500 ns. No maximum down-level is specified because external interruption signals are asynchronous and may occur at any time (see Figure 4).

No attempt should be made to use a pattern of bits or a bit configuration of external interruption signals to provide an identifiable interruption request, because CPU cannot guarantee that simultaneous pulses will be recognized as such. Possible skew between pulses may cause simultaneous pulses to be separated by sufficient time to cause the initiation of two separate but sequential interruption cycles.

CABLING

One cable, part 5372977, is required for the external interruption feature. It is supplied by the external device, and is available in lengths up to 50 feet. Longer lengths are available on an RPQ basis. See Figure 9. The signal pin assignments for the connector on the CPU and the corresponding assignments at the device end are shown on Figures 5 and 6. The external interruption signals are labeled sig-in-0 through sig-in-7. No other signals apply. See also "Power Effects" and "Direct Control Cabling" under "Direct Control Feature."

Appendix A. Electrical Specifications

PHYSICAL REQUIREMENTS

Multiple Drivers and Receivers

Up to ten receivers must be able to be driven by one driver. The driver must be located at one of the extreme ends. Up to ten drivers must be able to be dot-ORed to drive one receiver. The receiver must be located at one of the extreme ends.

Note: An end-of-line driver or receiver may be placed beyond the terminator. In this case, the distance between the end-of-line driver or receiver and the terminator must be less than 6 inches.

Receivers must be spaced at least 3 feet apart. No minimum requirement is set regarding the spacing between drivers. No minimum requirement is set regarding the spacing between a terminator and driver or receiver if the terminator is placed on the outermost end of the line.

The maximum stub length from the line to a driver or receiver on the circuit card is 6 inches.

ELECTRICAL REQUIREMENTS—GENERAL

Voltage Levels

There are two logical levels. A dc line voltage of +2.25 volts or more denotes a logical 1 state, and a dc voltage of +0.15 volt or less denotes a logical 0 state. These voltages are relative to the driver ground.

Cable

All lines must have a characteristic impedance of 92 ±10 ohms, and must be terminated at each extreme end in their characteristic impedance by a terminating network.

Cable length may be limited by special conditions but is never to exceed a maximum line resistance of 33 ohms. The 33-ohm line resistance includes all contact resistance, internal cable resistance, and interunit cable resistance.

Terminating Networks

The terminating network must present an impedance of 95 ohms ±2.5 percent between the signal line and ground, and must be capable of dissipating 390 milliwatts.

Ground Shift and Noise

The maximum noise (measured at the receiver input) coupled onto any signal line must not exceed 400 millivolts.

The maximum allowable ground shift, between any active driver and any receiver of the same interface line, is 150 millivolts. Therefore, the maximum shift (coupled noise plus ground shift) allowed on any line is 550 millivolts.

The logical levels defined in "Voltage Levels" under "Electrical Requirements—General" and the receiver threshold levels specified in "Receivers" under "Interface Circuit Requirements" allow for this 550-millivolt shift. That is, a negative noise pulse of 400 millivolts coupled with a positive receiver ground shift of 150 millivolts occurring during a 1 state (2.25 volts minimum) guarantees a receiver input of 1.7 volts or more. See Diagram A.
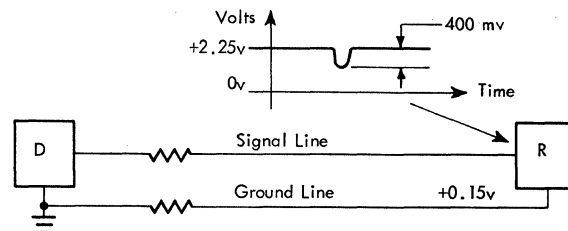

Diagram A. Negative Noise

Also, a positive noise pulse of 400 millivolts coupled with a negative receiver ground shift of 150 millivolts occurring during a 0 state (0.15 volt maximum) guarantees a receiver input of 0.7 volt or less. See Diagram B.

Note: The noise measurements are made at the input to the receiver. A combination of the dc level and ac noise must not exceed 0.7 volt for the down-level and must not be less than 1.7 volts for the up-level.
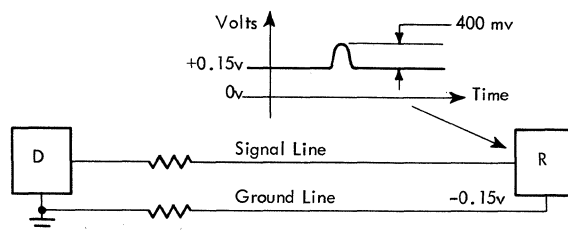

Diagram B. Positive Noise

Note: Noise may be generated by circulating currents in the grounding network if the proper grounding rules are not followed. In System/360 and System/370, the ground lead (green with yellow tracer) in the power source cable to the CPU is connected to the machine (frame) ground. All signal lead shields are connected to circuit (electronic) ground. In the CPU, these two grounds (circuit and machine) are connected at one point only.

Devices attached to the system should follow the same convention—signal shields connected to circuit ground, and power ground connected to machine frame. These two grounds should not be connected in the device. Excessive noise may be generated by circulating currents in the grounding network when circuit and machine grounds are commoned in both CPU and attached units.

INTERFACE CIRCUIT REQUIREMENTS

Receivers

An input voltage (relative to receiver circuit ground) of 1.7 volts or more is interpreted as a logical 1; an input of 0.70 volt or less is interpreted as a logical 0. An open-circuited input is interpreted as a logical 0.

The receiver should not be damaged by:
1. A dc input of 7.0 volts with power on in the receiver.
2. A dc input of 6.0 volts with power off in the receiver.
3. A dc input of -0.15 volt with power on or off.

The receiver input must not require a positive current (Diagram C) larger than +0.42 milliampere at an input voltage of +3.11 volts.

Negative receiver input current at +0.15 volt must not exceed -0.24 milliampere. In addition, receiver input impedance must be larger than 4.0 kilohms and less than 20 kilohms.

Receivers must be designed to ensure that no spurious noise is generated on the line during a normal power-up or power-down sequence.
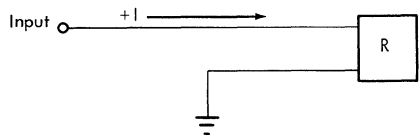
Diagram C. Receiver

Drivers

In the logical 0 state:
1. The output voltage must not exceed 0.15 volt at a load of +240 microamperes. See Diagram D for current polarity definition.
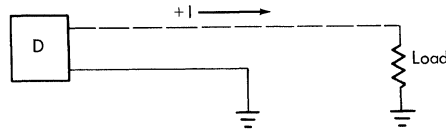
Diagram D. Current Polarity

In the logical 1 state:
1. The output voltage must be 3.11 volts or more at a load of +59.3 milliamperes (two terminators and ten receivers).
2. The output voltage must not exceed 5.85 volts at a load of +30 microamperes (one receiver and no terminator).
3. The output voltage must not exceed 7.0 volts at a load of +123.0 milliamperes during an overvoltage internal to the drivers.

Drivers must be designed to ensure that no spurious noise is generated on the line during a normal power-up or power-down sequence. For the driver, this may be accomplished by one of the following methods:
1. Sequencing the power supplies.
2. Building noise suppression into the circuit.
3. Providing an externally controlled gate. See Diagram E.
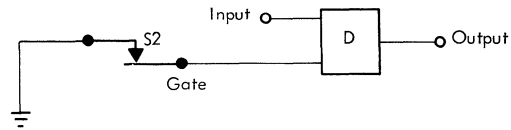

Diagram E. Driver Gate

For a normal power-down sequence:
1. Logically ensure that the driver is in the 0 state.
2. Close contact S2. See Diagram E.
3. Turn power off.
For a normal power-up sequence:
1. Ensure that contact S2 is closed.
2. Turn power on.
3. Logically ensure that the input level will cause the driver output to be in the 0 state.
4. Open contact S2.

Fault Conditions

A grounded signal line must not damage drivers, receivers, or terminators.

With one driver transmitting a logical 1, loss of power in any single circuit driver, receiver, or terminator on the line must not cause damage to other components.

With both terminators connected, line operation must not be affected by power off in any drivers or receivers on the line.

Circuits

Figures 11-13 show representative circuits used to drive, receive, and terminate the lines between the CPU and attached control units.
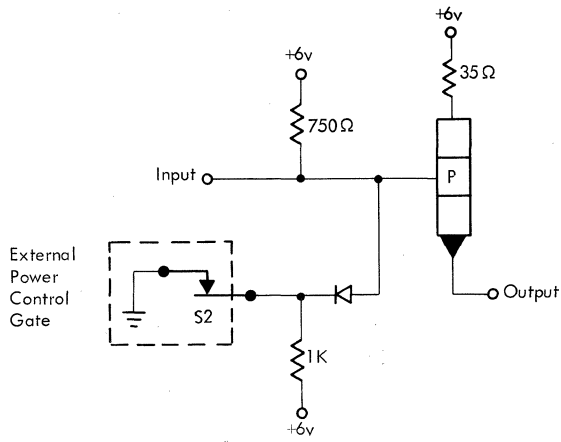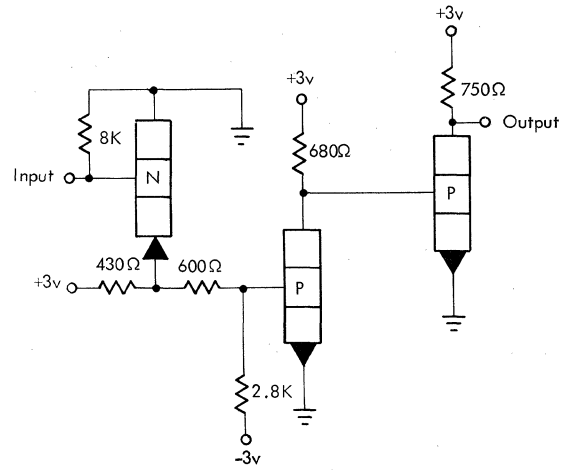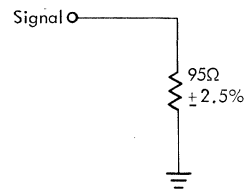

Figure 11. Line Driver

Figure 12. Line Receiver

Figure 13. Line Terminator

CABLING

Cable Halves

A screwdriver is required to join the cable halves. The connecting screw is spring-loaded to prevent damage to mating block contacts. Blocks should be aligned to ensure proper parallel contact mating. After the blocks are keyed, push the screw forward to engage the insert; then tighten securely. For assistance in removing individual contacts, field personnel should use tool, part 450540 (available from IBM Field Engineering) or a No. 12 crocheting needle.

Mounting

In normal applications, the blocks are mounted in the horizontal plane to provide a smoother bend into the coaxial cables. See Figure 14. Vertical mounting produces unusual bending configurations, requiring careful routing and strain relieving of the external cables.

Figure 15 shows an exploded view of the panel mounting.

OFFLINE UTILIZATION

This cable connector has the unique feature of being able to mate "cable half" to "cable half" for offline use or for the physical bypassing of machine units. See Figure 16.

When mating cable halves, it is only necessary to use the screw on the "B-" style connector. This allows the "A" style connector's screw to fall within the empty insert location in the "B-" style block and provides an easier connection.

Typical connections are shown on Figures 16 and 17. (Information concerning the EPO cable shown on Figure 17 is in Systems Reference Library, *IBM System/360 and System/370 Power Control Interface, Original Equipment Manufacturers' Information*, GA22-6906.)

CONNECTORS

Connector Blocks

Three styles of connector blocks are available: "A," "B," and "B-." The "A" and "B" designations identify proper mating arrangements since the physical hardware is identical. The two styles are differentiated by the color coding
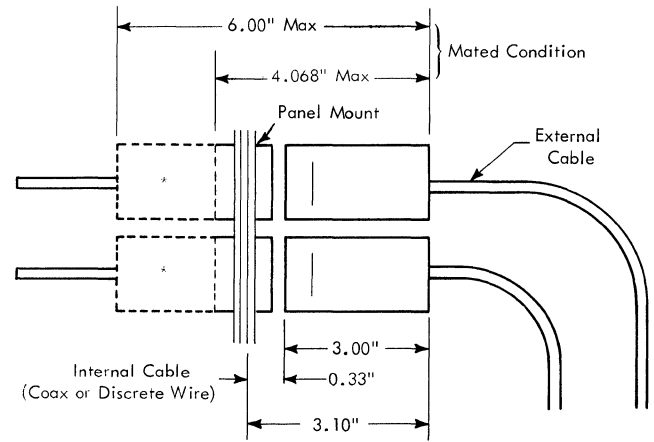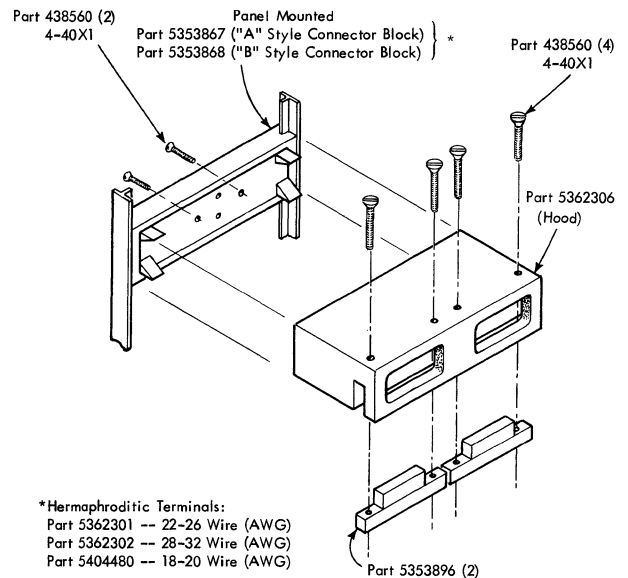

Figure 14. Mounted Cable Halves

Figure 15. Panel Mount with Optional Strain Relief

of the blocks: the "A" style is light gray and the "B" style is dark gray. See Figure 18.

The "B-" style block is the same as the "B" style but does not have a threaded insert.

When mating connectors, care should be taken to prevent accidental mismating of two "A" or two "B" style connectors since letter positions would be transposed. Connectors of the same color must never be mated.
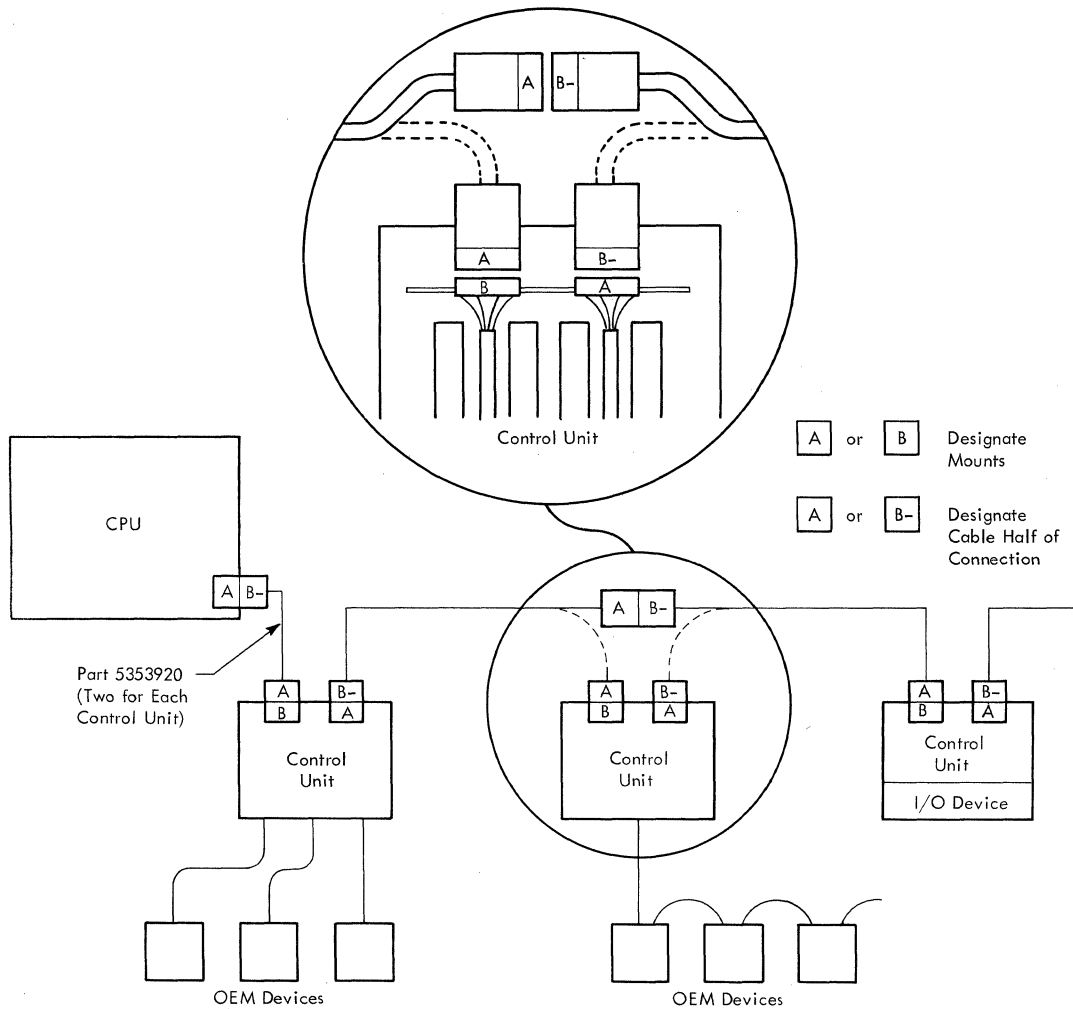
Figure 16. Offline Utilization

Both the "A" and the "B" style blocks are used for panel mounts. The "A" style may also be used for a cable end. The "B-" style is used only as a cable end. See "Offline Utilization."

Capacity

Forty-eight individual positions (serpent contacts) are provided for in the connector blocks. Application of the connector is limited only by the number of coaxial wires (shielded wires or twisted pairs) used and the method used to ground the shields of the coaxial wires. In the direct control interface, 40 serpent contacts are required on each connector to terminate individually the shield and signal wires of the 20 coaxial wires.

Terminators

The System/360 and System/370 direct control interface line termination is provided by the assembly (part 5440649) shown in Figure 19. This assembly, used with serpent connectors, is inserted into the out connectors (2) of the last control unit on the line.

Serpent Contacts

Description

The serpent contact is a hermaphroditic, gold-plated phosphor bronze, dual-mating surface contact. See Figure 20.

Wire Termination

Termination is accomplished by the bare-wire crimp method. Three contacts are available to cover the range of solid or stranded wire sizes required:

IBM Part	Wire Size (AWG)	Insulation Range
5404480	18-20	0.042 to 0.103
5362301	22-26	0.028 to 0.103
5362302	28-32	0.026 to 0.090

EPO Cable (Part 5351178)

Connector
(Part 523269)
Ground Tab
(Part 5271288)

System/360
System/370

OEM
Control Unit

| A | B |

| A | B | A | B |

| B- | | A |

| B- | | A |

A -- Panel Mount (Part 5353867)

B -- Panel Mount (Part 5353868)

Signal Cable
(Part 5353920)

Terminals:
EPO Cable Connector (6 Required)	14-18 AWG -- Part 523267
	20-22 AWG -- Part 5351177
Signal Cable Panel Mount (40 Required per Connector)	22-26 AWG -- Part 5362301
	28-32 AWG -- Part 5362302
	18-20 AWG -- Part 5404480

Figure 17. Typical Connection

Part 5808325

Part 5808325

Bus Assembly (Part 5440649)

Figure 19. Terminator Assembly

4.00"

Mating Surface
(Front)

*0.140"x 0.068" wide
(Both ends)

B   G

2 3 4 5 6 7 8 9 10 11 12 13   2 3 4 5 6 7 8 9 10 11 12 13

D   J

1.00"

"A" Style Block -- Light Gray (Part 5353867)

0.333"

0.068"

0.311"

0.546"

0.857"

Mating Surface
(Front)

D   J

2 3 4 5 6 7 8 9 10 11 12 13   2 3 4 5 6 7 8 9 10 11 12 13

B   G

"B" Style Block -- Dark Gray with Threaded Insert (Part 5353868)
"B-" Style Block -- Dark Gray, No Threaded Insert (Part 5353869)

*Mounting Slots

Figure 18. Connector Blocks and Contact Location

A. Part Identification

Retaining
Tab

Ski

Insulation
Support

Latch Tab

Crimp
Barrel

B. Dimensions

0.684"

0.028 ± 0.004"

0.025 + 0.015"
-0.000"

C. Mating Configuration

Two Point Contact

Two Point Contact

Figure 20. Serpent Contact

Appendix B. Signal Cabling and Connectors   19

Electrical Specifications

Voltage Ratings: The maximum voltage rating of this connector is 24 volts ac or dc. For applications above 24 volts, contact the local IBM representative.

Current Rating: The maximum continuous current rating of each contact is 6 amperes. The contacts are not intended for interrupting current.

Resistance: The termination-to-termination resistance (includes two crimps and mated contacts) will not exceed:
1. 0.020 ohms when installed on #22 AWG and larger wire.
2. 0.030 ohms when installed on #24-#26 AWG wire.
3. 0.040 ohms when installed on #28-#32 AWG wire.

Insulation Resistance: The contact-to-contact insulation resistance is 100 megohms (minimum) measured at a test potential of 100 volts dc, after exposure of 1 hour at a temperature of 38° C and 85-90 percent relative humidity.

Grounding: All surfaces of the connectors are nonconductive plastic; therefore, no grounding is necessary.