File No. S360-01
Form A22-6875-5

IBM Systems Reference Library

IBM System/360 Model 44

Functional Characteristics

This manual describes the system structure, features, instruction timings and formulas, channels, device addressing, and operator controls unique to System/360 Model 44.

It is assumed the reader has a knowledge of the System/360 as defined in the *IBM System/360 Principles of Operation,* Form A22-6821 and the *IBM System/360 System Summary,* Form A22-6810.

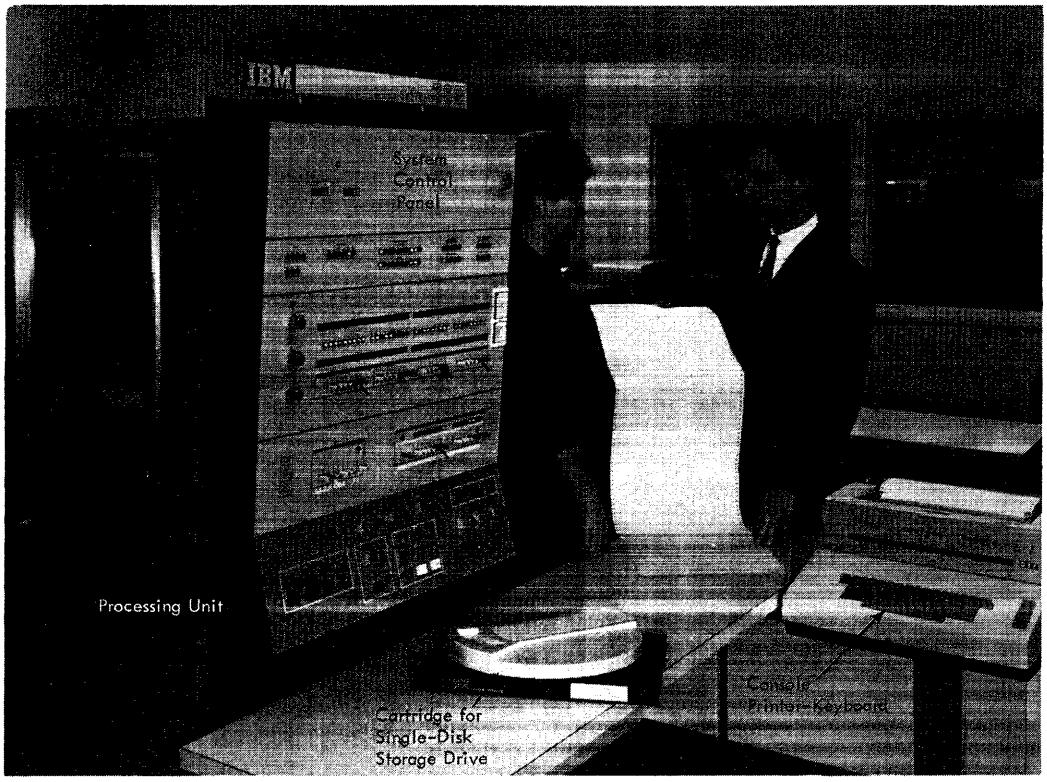
For installations using the direct word, direct data channel, or priority interrupt features, a companion publication is *Data Acquisition Special Features for the IBM System/360 Model 44,* Form A22-6900. Other related literature is described in *IBM System/360 Bibliography,* Form A22-6822.

SIXTH EDITION

This is a major revision of, and obsoletes, A22-6875-3 and -4 and Technical Newsletter N22-0253. The section "Instruction Timing Formulas" has been added. Other changes to the text are indicated by a vertical line to the left of the change; new and revised illustrations are denoted by the symbol ● to the left of the caption.

This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. B98, P.O. Box 390, Poughkeepsie, N.Y. 12602. A form is provided at the back of this publication for readers' comments. If the form has been removed, comments may be sent to the above address.

Contents



IBM System/360 Model 44

Model 44, a new member of the IBM System/360, is tailored to handle all relatively small to medium-sized scientific applications and advanced data acquisition and process control applications. Although the Model 44 is thus specialized, its inclusion within the context of System/360 philosophy provides for a very large addressing capability, a wide range of high-speed storage capacities, and I/O multiplexing on channels of low and high data-transfer rates.

The basic Model 44 is unilaterally compatible with System/360 Models 30 through 91. That is, a program written for the Model 44 can be executed on any of these other models if the compatibility constraints of System/360 are observed. However, programs that depend on special features available for only the Model 44 cannot be run on any other System/360 model. These features are: the selection of less than eight bytes for long-precision floating-point arithmetic (to be discussed) and three features (direct word, direct data channel, and priority interrupt) described in *Data Acquisition Special Features for the IBM System/360 Model 44*, Form A22-6900.

Model 44 was derived from standard System/360 architecture by including only those capabilities and instructions that are required for a binary and scientific model. The Model 44 therefore excludes 19 instructions that are normally included in the standard instruction set; those excluded are decimal arithmetic and other variable-field-length instructions.

One or more multiplexer channels, providing a choice of two data transfer rates, can be included in the Model 44 system. (Model 44 cannot be equipped with selector channels; however, a multiplexer channel in which one of its subchannels is operating in burst mode performs very similarly to a selector channel.)

Model 44 uses conventional high-speed sequential logic control instead of read-only storage.

Although the Model 44 processing unit is about the same in physical size (Figure 1) as that of its nearest neighbor, the Model 50, its performance on problems for which it is optimized is 30 to 60 per cent faster than that of a Model 50. Performance figures depend much on the specific applications and optional equipment selected, namely: storage size, number and speed of channels, and quantity and speed of I/O devices supporting the CPU.

The Model 44 processing unit contains, as standard equipment, a single-disk storage drive (capacity 1,171,200 bytes) used for programming systems residence; the necessary disk storage adapter; and an adapter for the console printer-keyboard that is located on the processor table. A second single-disk storage drive, of equal capacity to the first, may be added within the processing unit as a special feature. (See Figure 2.)

All the I/O devices that can be attached to the Model 44 are listed, with channel and control-unit data, in Figure 9.

Processing Unit

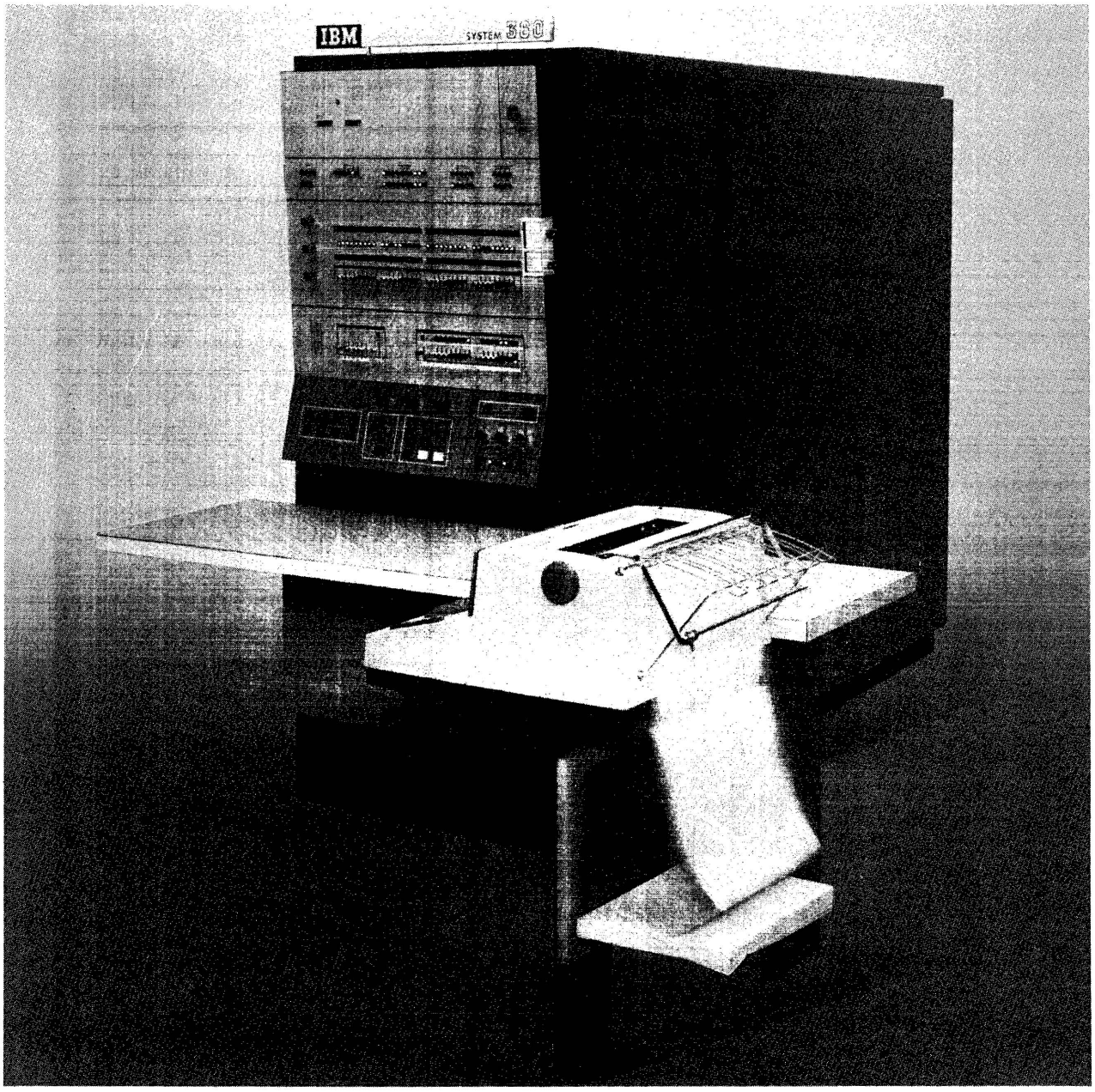
As in all other models of the System/360, the smallest addressable data unit is the byte, consisting of eight bits. A ninth bit, called the parity bit (not available to the program), is associated, for checking purposes, with each byte. Because of the optimization of Model 44 toward scientific work, however, the common units of data are the 32-bit binary word and the 16-bit binary halfword, composed of four and two bytes, respectively. Parity is checked upon each data fetch from processor storage and each transfer of data to or from channels.

Floating-point arithmetic uses the 32-bit word for short operands and a 64-bit double word for long operands. Model 44 introduces a new feature, variable long-precision floating-point arithmetic, in which different selections can be made for the length of the fraction when long operands are used. (See "Variable Long-Precision Floating Point.")

Processor storage speed for the Model 44 is 1 microsecond. Four bytes (one word or two halfwords) are stored or fetched in each access. Processor storage, always housed within the CPU, is available in the four capacities shown at the top of Figure 3.

Data paths throughout the CPU are one word wide. Because variable-length fields are not used in Model 44, bytes are handled in groups of two or four; however, they can be manipulated singly by the INSERT CHARACTER, STORE CHARACTER, TEST UNDER MASK, or the five immediate instructions:

AND (NI)
COMPARE LOGICAL (CLI)
EXCLUSIVE OR (XI)
MOVE (MVI)
OR (OI)

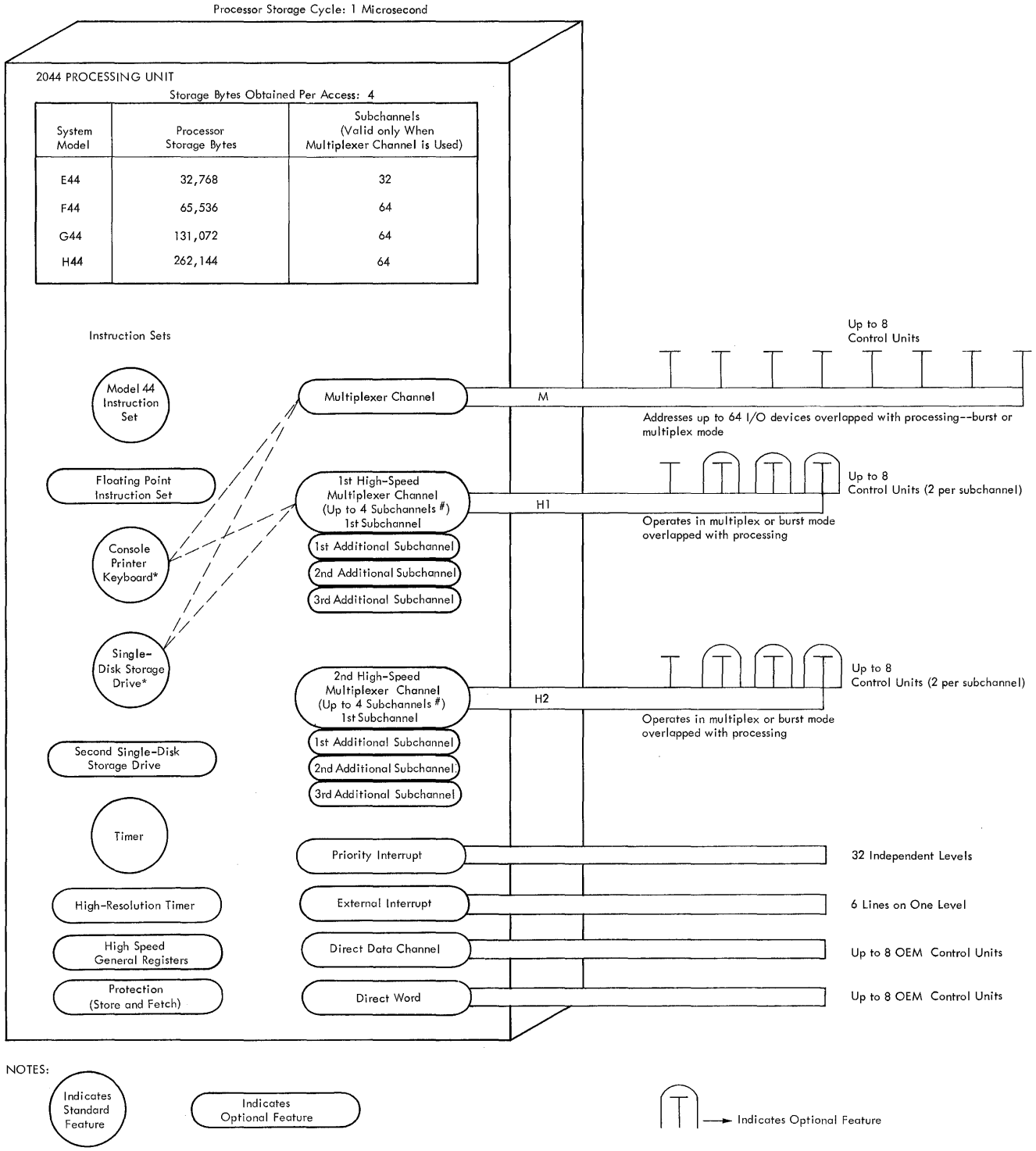


• Figure 1. Processing Unit and Console Printer-Keyboard

The 16 general registers of the basic Model 44 are in a normally-unaddressable extension of the 1-microsecond processor storage. (This extension is often called "bump" storage or "core extension.") If the optional high-speed general registers feature (sometimes called "accelerator" feature) is installed, the 16 general registers are provided instead in solid logic technology (SLT) circuitry having 0.25 microsecond read/write time. This quartering of the access periods substantially reduces address generation time as well as the basic execution time of all fixed-point instructions in particular. (See Figures 3 and 7.)

Arithmetic and logical operations are performed between the A and B registers; the results are usually formed in the B register. The Bx register, coupled to the B register with left and right shifting ability, is used in multiply and divide operations and as an auxiliary address register.

If the floating-point feature is installed, the Ax register extends the A register to the 64-bit width needed for long-operand floating-point arithmetic. For long operands, the high-order halves of the floating-point registers are contained in SLT circuitry and the low-order halves are contained in the extension of processor



A system must have either the Multiplexer or the 1st High-Speed Multiplexer Channel; a system may have either, or both, plus the 2nd High-Speed Multiplexer Channel or the two High-Speed Multiplexer Channels.

To each subchannel may be assigned:
Two shared-path control units, or
Two devices of a multipath control unit, or
One shared-path control unit and one device of a multipath control unit.

* Requires: Multiplexer or 1st High-Speed Multiplexer Channel, subchannel, and Control Unit position.

• Figure 2. IBM System/360 Model 44 Configurator

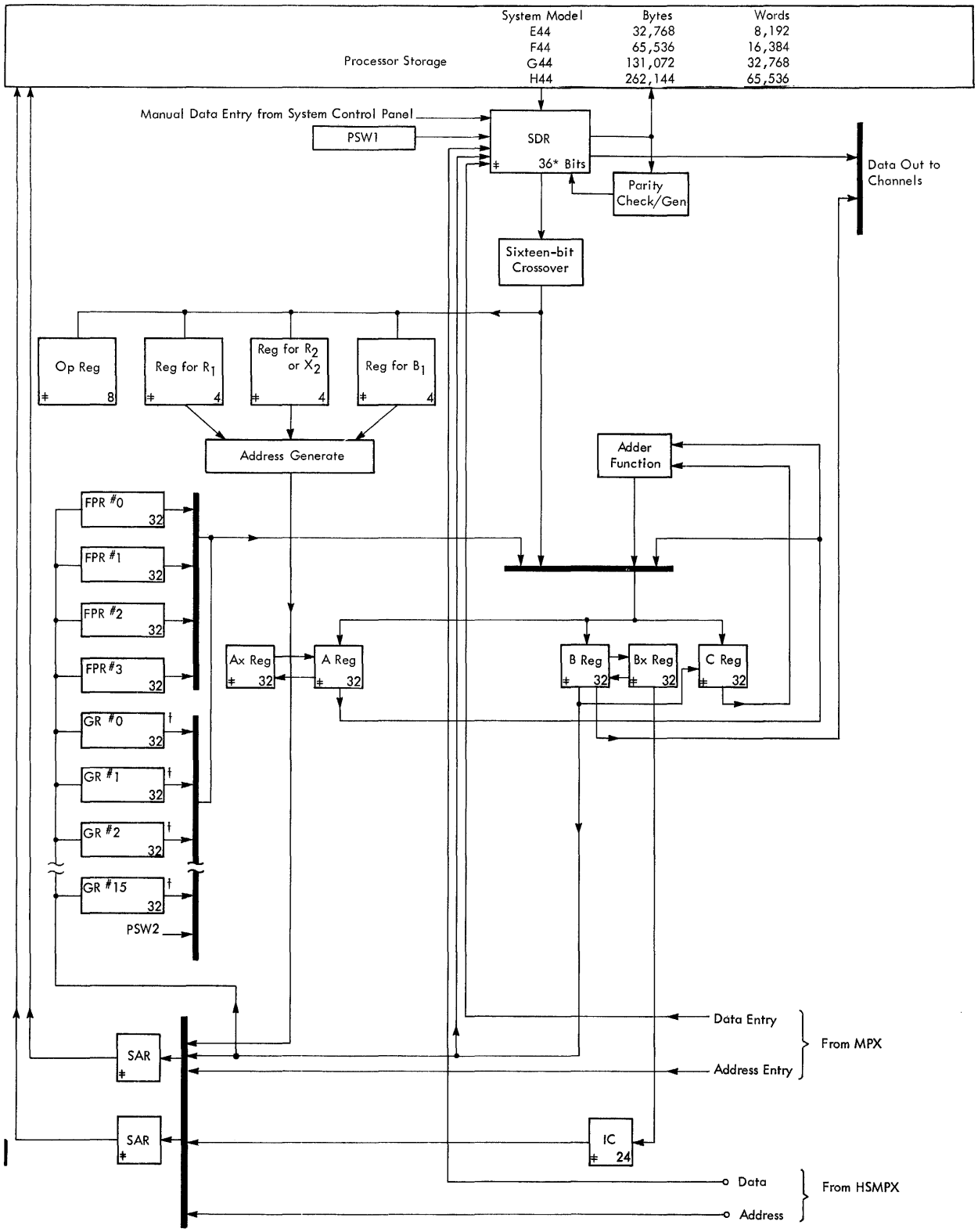


Figure 3. Data Flow in Model 44 CPU

storage. For short operands, only the high-order (SLT) halves of the floating-point registers are used.

An optional feature provides six lines for external interrupts. The source of the external interrupts is identified by bits 26-31 of the interruption code in bit positions 16-31 of the old program status word (old PSW). These interrupts are independent of channel operations or of the direct-control feature required to provide external-interrupt capabilities for most System/360 models. Figure 14 shows the PSW.

Timer

Model 44 has either a line-frequency timer as a standard capability or a high-resolution timer as a special feature. Either type can be used as an interval timer to measure elapsed time, or programmed to tell the time of day for program completions, etc. The standard timer is counted down every 1/60th or 1/50th of a second, and is fully described in *IBM System/360 Principles of Operation,* Form A22-6821. The special-feature timer is mentioned therein also; for this, the least significant bit of the 32-bit timer word is decremented and the resolution is 13 microseconds.

The low-order eight bits of the high-resolution timer lie in an SLT-circuit counter rather than in core storage. The contents of the storage address register are monitored for any reference to byte 83, whether addressed directly, or as part of the halfword at 82, or as part of the fullword at 80. When any such reference to 83 is detected, a substitution occurs that causes the contents of the eight-bit counter to participate in the operation in place of the storage byte 83. This eight-bit counter includes the decrementing and parity-generating circuits and acts for all purposes as the low-order byte of the timer word. Byte 83 in the storage array becomes unaddressable either by CPU instructions or by channels, and its bits cannot be displayed.

A 76.8-KC oscillator causes the low-order bit of the counter to be decremented at approximately 13-microsecond intervals. Decrementing the counter does not interfere with CPU processing. The decrementing is prevented by any of the following conditions:

1. The initial program is being loaded
2. The CPU is in the stopped state
3. The rate switch is set to INSN STEP
4. The disable interval timer switch is turned on. This switch is for the use of customer engineering (CE) personnel.

Every 1/300th of a second the counter becomes all 1's, and bit 23 is updated whenever access to storage permits. Specifically, when the counter becomes all 1's, a timer step trigger turns on (while the decrementing continues); if the timer step trigger is on at end-operation time, instruction sequencing is stopped to permit the timer word to be updated by the subtraction of 1 from bit position 23, at which time the timer step trigger is turned off. Updating takes 1.75 microseconds, and the fetching of the next instruction is delayed for that time.

If the timer step trigger is on when the CPU is fetching from the timer word in storage, bits 24-31 of the fetched word are made zero; that is, the fetch gets only zeros in the fourth byte instead of the contents of the counter. This ensures a correct relationship between the value fetched from the counter and the value fetched from the main storage portion of the timer at this instant; the counter is prevented from appearing as all 1's when timer bit position 23 is not yet decremented. The value of the fetched timer word may appear to be off by no more than the execution time of the instruction (after allowing for cycle-stealing by channels).

If, during the course of an instruction that addresses the timer word, an interruption is requested, this interruption may be delayed until the end of the next instruction. Only machine-check and program interruptions are not delayed. If only the standard timer is installed, however, the delay does not occur for any class of interruption.

When decrementing causes the entire timer word to pass from a positive value (including zero) to a negative value, a standard timer interrupt occurs in the form of an external interruption request. The full cycle time, from all 1's in bit positions 0-23 to the time when the interruption signal is generated, is the standard 15.5 hours.

Programming Note

When the timer is used as a real-time clock and the CPU is to be instructed to read the current timer value and set the clock to some other value, successive fullword LOAD and STORE instructions must be used to simulate the MVC move which is absent from the Model 44 instruction set. It is possible for a timer updating to occur between the LOAD and STORE instructions; thus, the real-time clock may "creep" forward by 13 microseconds, and in the worst case this creep takes place whenever the clock value is changed.

Protection Feature

The protection feature makes it possible to protect the contents of main storage from destruction or misuse. When the protection is added, as a special feature, to the Model 44, it includes both the store and the fetch protection features defined in *IBM System/360 Principles of Operation,* Form A22-6821. Neither store nor fetch protection is available alone. The protection key

in storage can be changed by the SET STORAGE KEY instruction and inspected by the INSERT STORAGE KEY instruction. Note that these two instructions are added to the Model 44 instruction set only when the protection feature is installed. The instruction timings are included in Figure 7.

In the INSERT STORAGE KEY instruction, bit 28 of the register designated by the first operand is the fetch protection bit and is set to one for both store and fetch protection or to zero for store protection only.

It is possible for the Model 44 to access in one cycle a storage word that straddles a 2,048-byte protection boundary. This can happen only in instruction fetching, at which time a fetch protection violation may cause the instruction to be suppressed. However, Model 44 has time to fetch and compare both storage keys during the one main storage access with no increase in the instruction time.

Standard Supporting Equipment

Console Printer-Keyboard

The console printer-keyboard (Figure 4) permits communication between the operator and the system. Facilities are provided for interrupting the processing unit and for signalling the end of a data transmission.

•Figure 4. Console Printer-Keyboard

The printer-keyboard has a stationary carriage and a replaceable, interchangeable printing sphere. Its typewriter-style keyboard and the printing function can be used independently: the keyboard for system input and the printer for computer output. The font of each printing sphere is specified by the customer.

The functions and operations of the console printer-keyboard are the same as those described for the IBM 1052 Printer-Keyboard Model 7 in *IBM System/360 System Summary,* Form A22-6810. Operating procedures and details are the same as those in *IBM 1052 Printer-Keyboard Model 7 with IBM 2150 Console,* Form A22-6877.

The console printer-keyboard is attached to one of the system channels via an adapter which is physically located within the CPU as a standard feature. The installation of the console printer-keyboard is also standard and takes up either one control-unit position and one subchannel of a multiplexer channel or one control-unit position and half a subchannel on a high-speed multiplexer channel.

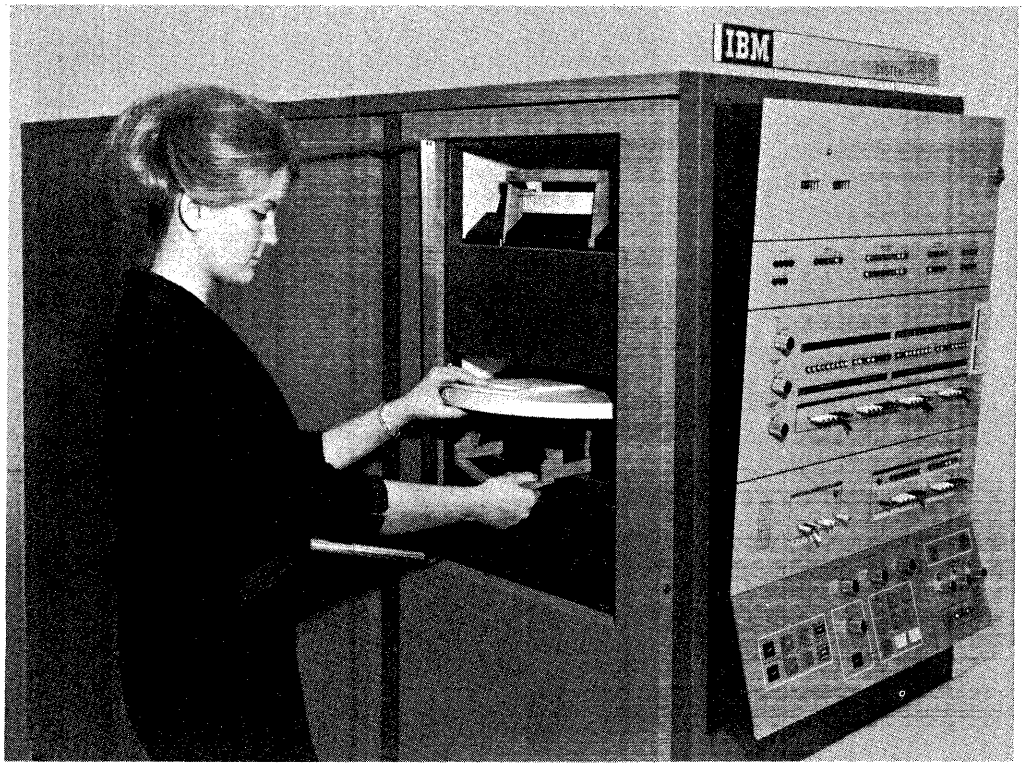
Single-Disk Storage Drive

The single-disk storage drive provides direct access auxiliary storage for a minimum of 1,171,200 bytes on a single disk permanently enclosed in an IBM 2315 Disk Cartridge and housed within the CPU, with side access for replacement of cartridges (Figure 5.) Each cartridge must be purchased separately, but the drive is a standard feature of Model 44.

The data rate of the disk storage is 90,000 bytes per second, necessitating operation in burst mode. Average time to seek a track is 70 milliseconds; the subsequent rotational delay to a particular record ranges from 0 to 40 milliseconds and averages 20 milliseconds.

Information is written on or read from the disk by a pair of magnetic read/write heads, one head for each surface. The disk is organized in 200 cylinders and three spare cylinders; a cylinder consists of a pair of tracks, one track per disk surface. Each cylinder contains 16 sectors (eight per track and surface). Each sector has a fixed length of 366 bytes. The three spare cylinders ensure that the stated capacities are maintained for the life of the cartridge. The read/write heads move, under a single seek command, directly to the track addressed. Error detection is accomplished on reading data from the disk.

No programming compatibility exists between the single-disk storage drive and disk storage drives controlled through the IBM 2841 Storage Control.



•Figure 5. Removing an IBM 2315 Disk Cartridge from a Single-Disk Storage Drive

The drive is attached to one of the system channels only via an adapter, which is also installed in the CPU as a standard feature. A second drive may be installed in the CPU, as a special feature, to double the storage capacity. The two drives use the same shared-path adapter and operate on one shared subchannel, requiring one control-unit position on either a multiplexer or a high-speed multiplexer channel. Seek overlap is permissible when both drives are installed.

Commands

Control Seek — 00001011: One byte is transferred to the adapter. The byte contains the required cylinder address (0 through 202). The channel is free after the transfer of this byte, and the drive is free at the end of the seek.

Read Data — HSSS1010: Reading begins with the head for track H, sector SSS, and continues to the end of the track. If SSS=0, the entire track of 2,928 bytes is read. If the CCW count goes to zero at the end of sector 7 (end of track) or before the end of any other sector, the drive is free at the end of the sector being read. If the CCW count goes to zero at the last byte of a sector 0-6, however, the device end is delayed until the end of the following sector.

Write Data — HSSS1001: Writing begins at track H, sector SSS, and continues to the end of the track. If the CCW count goes to zero before the end of the track, the remainder of the sector being written is filled with zeros by the adapter and the drive is then free.

Other Commands: The adapter also recognizes read IPL (00000010), control no-op (00000011), and sense commands (00000100).

Programming Notes

The formal record length of the single-disk storage drive is 2,928 bytes (one full track); for all correct but shorter records, "incorrect length" is a normal indication. The CCW for a read or write command must therefore contain the SLI flag (suppress-length-indication, bit 34) unless the operation is to end with the 366th byte of the eighth sector.

Command chaining to the next sector may take place at a sector boundary without rotational delay unless a read operation ends with the 366th byte of sectors 0-6.

Keys and Lights

All keys and lights for the proper operation of each drive are on the lower left portion of the system control panel and are described under "Operator Control Section."

Instructions

The Model 44 executes the following instructions:

	MNEMONICS			
	RR	RX	RS	SI
INSTRUCTION	FORMAT	FORMAT	FORMAT	FORMAT
Add	AR	A	----	----
Add Halfword	----	AH	----	----
Add Logical	ALR	AL	----	----
AND	NR	N	----	NI
Branch and Link	BALR	BAL	----	----
Branch on Condition	BCR	BC	----	----
Branch on Count	BCTR	BCT	----	----
Compare	CR	C	----	----
Compare Halfword	----	CH	----	----
Compare Logical	CLR	CL	----	CLI
Divide	DR	D	----	----
Exclusive OR	XR	X	----	XI
Halt I/O	----	----	----	HIO
Insert Character	----	IC	----	----
Load	LR	L	----	----
Load Address	----	LA	----	----
Load and Test	LTR	----	----	----
Load Complement	LCR	----	----	----
Load Halfword	----	LH	----	----
Load Negative	LNR	----	----	----
Load Positive	LPR	----	----	----
Load PSW	----	----	----	LPSW
Move	----	----	----	MVI
Multiply	MR	M	----	----
Multiply Halfword	----	MH	----	----
OR	OR	O	----	OI
Set Program Mask	SPM	----	----	----
Set System Mask	----	----	----	SSM
Shift Left Double	----	----	SLDA	----
Shift Left Double Logical	----	----	SLDL	----
Shift Left Single	----	----	SLA	----
Shift Left Single Logical	----	----	SLL	----
Shift Right Double	----	----	SRDA	----
Shift Right Double Logical	----	----	SRDL	----
Shift Right Single	----	----	SRA	----
Shift Right Single Logical	----	----	SRL	----
Start I/O	----	----	----	SIO
Store	----	ST	----	----
Store Character	----	STC	----	----
Store Halfword	----	STH	----	----
Subtract	SR	S	----	----
Subtract Halfword	----	SH	----	----
Subtract Logical	SLR	SL	----	----
Supervisor Call	SVC	----	----	----
Test and Set	----	----	----	TS
Test Channel	----	----	----	TCH
Test I/O	----	----	----	TIO
Test Under Mask	----	----	----	TM

An optional feature provides the full complement of floating-point instructions for both long and short operands and the RR and RX formats:

	MNEMONICS			
	RR FORMAT		RX FORMAT	
INSTRUCTION	LONG	SHORT	LONG	SHORT
Add Normalized	ADR	AER	AD	AE
Add Unnormalized	AWR	AUR	AW	AU
Compare	CDR	CER	CD	CE
Divide	DDR	DER	DD	DE
Halve	HDR	HER	----	----
Load	LDR	LER	LD	LE
Load and Test	LTDR	LTER	----	----
Load Complement	LCDR	LCER	----	----
Load Negative	LNDR	LNER	----	----

INSTRUCTION	MNEMONICS RR FORMAT	RX FORMAT	RS FORMAT	SI FORMAT
Load Positive	LPDR	LPER	----	----
Multiply	MDR	MER	MD	ME
Store	----	----	STD	STE
Subtract Normalized	SDR	SER	SD	SE
Subtract Unnormalized	SWR	SUR	SW	SU

As already described under "Protection Feature," two more instructions are added when that special feature is installed:

INSTRUCTION	FORMAT	MNEMONICS
Set Storage Key	RR	SSK
Insert Storage Key	RR	ISK

A full description of each instruction (except for execution time) is in the *IBM System/360 Principles of Operation,* Form A22-6821. Full timing formulas, and bases for determining the average times given in Figures 7 and 8, are described in this manual under "Instruction Timing Formulas."

Variable Long-Precision Floating Point

Some floating-point problems need more than short precision but do not require the 56 bits of long precision. With the variable long-precision floating-point feature, the user can adjust long-precision instructions for execution with 32, 40, 48, or the full 56 bits of precision. The adjustment for variable long-precision floating point is made at program execution time by setting a rotary switch on the system control panel to one of four positions (Figure 6). Each successively lower setting truncates eight bits from the fraction length. Figure 8 shows the effects on execution time.

SWITCH SETTING (NO. OF HEXADECIMAL DIGITS IN FRACTION)	LONG PRECISION (FRACTION LENGTH IN BITS)
14	56
12	48
10	40
8	32

For maximum speed, the switch is set to 8; for maximum precision, it is set to 14. Setting the switch to 14 maintains complete compatibility with other System/360 models using long-precision floating point. At settings 8, 10, or 12, all floating-point operations fetch the operands (from storage or floating-point registers) truncated to the selected fraction length;

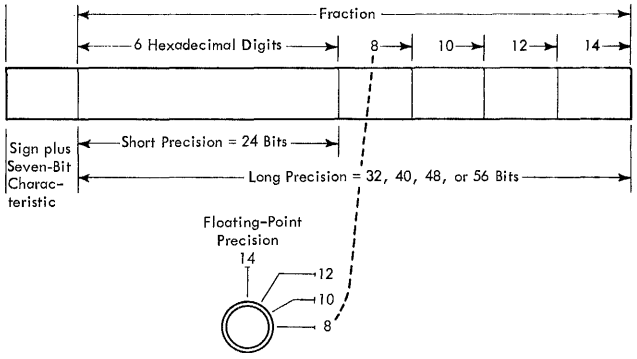


Figure 6. Variation of Fraction Length in Long Precision

low-order zeros are assumed to exist to the right of the truncation point. Model 44 always performs long-precision arithmetic with 56 bits. Therefore, when the truncated fraction is right-shifted for alignment during the performance of addition, subtraction, and comparison instructions, two, four, or six guard digits (depending on the selected precision) participate in the computation. With unnormalized addition and subtraction, the fraction in the result is tested for lost significance up to the selected fraction length.

Indexing Time

All Model 44 instruction timings (Figures 7 and 8) include the 1-microsecond I time and, for instructions that reference storage, the time to perform single indexing by one general register as referenced in the instruction (i.e., B ≠ 0).

For instructions in which double indexing is possible (i.e., all RX format instructions) the time required for the second indexing is 1 microsecond on the basic Model 44, or 0.75 microsecond when the high-speed general registers feature is installed. The times shown for the eight shift instructions assume no indexing (i.e., B = 0). For special timing calculations, the following adjustments may be made:

	BASIC MODEL 44	WITH HIGH-SPEED GENERAL REGISTERS
INSTRUCTION FETCH (included in all timings):	1.00	1.00
FIRST INDEXING (excluded for shift instructions):	1.00	0.25
SECOND INDEXING (excluded from all timings):	1.00	0.75

Instruction	Format	Mnemonic	Basic Model 44		Model 44 with High-Speed General Registers Feature (ms **)	
Add	RR	AR	3.75		1.75	
Add	RX	A	4.75		2.25	
Add Halfword	RX	AH	4.75		2.25	
Add Logical	RR	ALR	3.75		1.75	
Add Logical	RX	AL	4.75		2.25	
AND	RR	NR	3.75		1.75	
AND	RX	N	4.75		2.25	
AND	SI	NI	3.75		3.00	
Branch and Link	RR	BALR	3.25		2.25	
Branch and Link	RX	BAL	3.25		2.50	
Branch on Condition	RR	BCR	BR 2.50		1.75	
			No BR 1.00		1.00	
Branch on Condition	RX	BC	BR 2.75		2.00	
			No BR 2.00		1.25	
Branch on Count	RR	BCTR	3.75		2.50	
Branch on Count	RX	BCT	3.75		2.75	
Compare	RR	CR	3.00		1.75	
Compare	RX	C	4.00		2.25	
Compare Halfword	RX	CH	4.00		2.25	
Compare Logical	RR	CLR	3.00		1.75	
Compare Logical	RX	CL	4.00		2.25	
Compare Logical	SI	CLI	3.25		2.50	
Divide	RR	DR	31.75		28.75	
Divide	RX	D	32.75		29.00	
Exclusive OR	RR	XR	3.75		1.75	
Exclusive OR	RX	X	4.75		2.25	
Exclusive OR	SI	XI	3.75		3.00	
Halt I/O	SI	HIO	3.00 - 35.00		2.25 - 35.00	
Insert Character	RX	IC	4.00		2.50 EA, 2.25 OA	
*Insert Storage Key	RR	ISK	3.50		2.00	
Load	RR	LR	3.00		1.00	
Load	RX	L	4.00		2.25	
Load Address	RX	LA	3.00		1.25	
Load and Test	RR	LTR	3.00		1.00	
Load Complement	RR	LCR	3.00		1.75	
Load Halfword	RX	LH	4.00		2.25	
Load Negative	RR	LNR	3.00		1.75	
Load Positive	RR	LPR	3.00		1.75	
Load PSW	SI	LPSW	4.50		3.75	
Move	SI	MVI	3.75		3.00	
Multiply	RR	MR	18.39		16.14	
Multiply	RX	M	19.39		16.89	
Multiply Halfword	RX	MH	12.72		10.72	
OR	RR	OR	3.75		1.75	
OR	RX	O	4.75		2.25	
OR	SI	OI	3.75		3.00	
Set Program Mask	RR	SPM	2.00		1.50	
*Set Storage Key	RR	SSK	3.00		2.00	
Set System Mask	SI	SSM	3.50 EA,4.00 OA		2.75 EA,3.00 OA	
			$S \leq 3$	$S > 3$	$S \leq 1$	$S > 1$
Shift Left Double	RS	SLDA	5.50	5.50 + 0.25 (S-3)	3.00	3.00 + 0.25 (S-1)
Shift Left Double Logical	RS	SLDL	5.50	5.50 + 0.25 (S-3)	3.00	3.00 + 0.25 (S-1)
Shift Left Single	RS	SLA	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Left Single Logical	RS	SLL	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Right Double	RS	SRDA	5.50	5.50 + 0.25 (S-3)	3.00	3.00 + 0.25 (S-1)
Shift Right Double Logical	RS	SRDL	5.50	5.50 + 0.25 (S-3)	3.00	3.00 + 0.25 (S-1)
Shift Right Single	RS	SRA	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
Shift Right Single Logical	RS	SRL	3.50	3.50 + 0.25 (S-3)	2.25	2.25 + 0.25 (S-1)
			For single indexing of shift instructions, Add 1.00		For single indexing of shift instructions, Add 0.25	
Start I/O	SI	SIO	3.00 - 40.00		2.25 - 40.00	
Store	RX	ST	4.25		2.50	
Store Character	RX	STC	4.75 EA,4.25 OA		3.00 EA,2.50 OA	
Store Halfword	RX	STH	4.25		2.50	
Subtract	RR	SR	3.75		1.75	
Subtract	RX	S	4.75		2.25	
Subtract Halfword	RX	SH	4.75		2.25	
Subtract Logical	RR	SLR	3.75		1.75	
Subtract Logical	RX	SL	4.75		2.25	
Supervisor Call	RR	SVC	4.00		1.00	
Test and Set	SI	TS	3.50		2.75	
Test Channel	SI	TCH	4.00 - 20.00		3.25 - 20.00	
Test I/O	SI	TIO	3.00 - 38.00		2.25 - 38.00	
Test Under Mask	SI	TM	3.00 EA,3.25 OA		2.25 EA,2.50 OA	
			For double indexing of RX format instructions, add	1.00		0.75

NOTES: EA = Even Address
OA = Odd Address
S = Number of bits shifted
*Instruction added with protection feature
**All times except those for the eight shift instructions include single indexing; see "Indexing Time."

Figure 7. Execution Time for Standard Instructions and Protection-Feature Instructions

Instruction	Format	Mnemonic	Average Time in Microseconds *	
			Basic Model 44	Model 44 with High-Speed General Registers Feature
Add Normalized (long)	RR	ADR	6.28	6.28
Add Normalized (long)	RX	AD	8.28	7.53
Add Normalized (short)	RR	AER	3.81	3.81
Add Normalized (short)	RX	AE	5.31	4.56
Add Unnormalized (long)	RR	AWR	6.25	6.25
Add Unnormalized (long)	RX	AW	8.25	7.50
Add Unnormalized (short)	RR	AUR	3.79	3.79
Add Unnormalized (short)	RX	AU	5.29	4.54
Compare (Long)	RR	CDR	5.84	5.84
Compare (Long)	RX	CD	7.84	7.09
Compare (Short)	RR	CER	3.50	3.50
Compare (Short)	RX	CE	5.00	4.25
Divide (Long)				
Precision 14	RR	DDR	124.00	124.00
Precision 12	RR	DDR	108.50	108.50
Precision 10	RR	DDR	93.00	93.00
Precision 8	RR	DDR	32.75	32.75
Divide (Long)				
Precision 14	RX	DD	126.00	125.25
Precision 12	RX	DD	110.50	109.75
Precision 10	RX	DD	95.00	94.25
Precision 8	RX	DD	34.75	34.00
Divide (Short)	RR	DER	23.25	23.25
Divide (Short)	RX	DE	24.75	24.00
Halve (Long)	RR	HDR	3.25	3.25
Halve (Short)	RX	HER	1.50	1.50
Load (Long)	RR	LDR	3.00	3.00
Load (Long)	RX	LD	5.00	4.25
Load (Short)	RR	LER	1.00	1.00
Load (Short)	RX	LE	3.00	2.25
Load and Test (Long)	RR	LTDR	3.00	3.00
Load and Test (Short)	RR	LTER	1.00	1.00
Load Complement (Long)	RR	LCDR	3.00	3.00
Load Complement (Short)	RR	LCER	1.00	1.00
Load Negative (Long)	RR	LNDR	3.00	3.00
Load Negative (Short)	RR	LNER	1.00	1.00
Load Positive (Long)	RR	LPDR	3.00	3.00
Load Positive (Short)	RR	LPER	1.00	1.00
Multiply (Long)				
Precision 14	RR	MDR	61.39	61.39
Precision 12	RR	MDR	52.72	52.72
Precision 10	RR	MDR	44.06	44.06
Precision 8	RR	MDR	21.14	21.14
Multiply (Long)				
Precision 14	RX	MD	63.39	62.64
Precision 12	RX	MD	54.72	53.97
Precision 10	RX	MD	46.06	45.31
Precision 8	RX	MD	23.14	22.39
Multiply (Short)	RR	MER	14.06	14.06
Multiply (Short)	RX	ME	15.56	14.81
Store (Long)	RX	STD	5.25	4.50
Store (Short)	RX	STE	3.25	2.50
Subtract Normalized (long)	RR	SDR	6.28	6.28
Subtract Normalized (long)	RX	SD	8.28	7.53
Subtract Normalized (short)	RR	SER	3.81	3.81
Subtract Normalized (short)	RX	SE	5.31	4.56
Subtract Unnormalized (long)	RR	SWR	6.25	6.25
Subtract Unnormalized (long)	RX	SW	8.25	7.50
Subtract Unnormalized (short)	RR	SUR	3.79	3.79
Subtract Unnormalized (short)	RX	SU	5.29	4.54
For double indexing of RX format instructions, add			1.00	0.75

*All times include single indexing; see "Indexing Time."

Figure 8. Execution Time for Floating-Point Instructions

Instruction Timing Formulas

The timing formulas for the standard and protection-feature instructions and the floating-point instructions are given separately; all instructions are considered both in the presence and absence of the high-speed general registers feature.

Group 1: Standard and Protection Timings with High-Speed General Registers

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Add	AR	1.75	1.75
Add	A	2.0 + BX	2.25
Add Halfword	AH	2.0 + BX	2.25
Add Logical	ALR	1.75	1.75
Add Logical	AL	2.0 + BX	2.25
AND	NR	1.75	1.75
AND	N	2.0 + BX	2.25
AND	NI	2.75 + BX	3.00
Branch and Link	BALR	2.25	2.25
Branch and Link	BAL	2.25 + BX	2.50
Branch on Condition	BCR	$1.0 + 0.75F^1$	1.37
Branch on Condition	BC	$1 + BX + 0.75F^1$	1.63
Branch on Count	BCTR	2.5	2.50
Branch on Count	BCT	2.5 + BX	2.75
Compare	CR	1.75	1.75
Compare	C	2.0 + BX	2.25
Compare Halfword	CH	2.0 + BX	2.25
Compare Logical	CLR	1.75	1.75
Compare Logical	CL	2.0 + BX	2.25
Compare Logical	CLI	2.25 + BX	2.50
Divide	DR	28.75	28.75
Divide	D	28.75 + BX	29.00
Exclusive OR	XR	1.75	1.75
Exclusive OR	X	2.0 + BX	2.25

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Exclusive OR	XI	2.75 + BX	3.00
Halt I/O	HIO	HSMPX = 1 + BX + MM + 2BM + IFR (5 + SEL + CU) MPX = 1 + BX + MM + BM + IFR (7 + SEL + CU)	2.25 to 35.00
Insert Character	IC	2.0 + BX + 0.25EA	2.37
Insert Storage Key	ISK	2.0	2.00
Load	LR	1.0	1.00
Load	L	2.0 + BX	2.25
Load Address	LA	1.0 + BX	1.25
Load and Test	LTR	1.0	1.00
Load Complement	LCR	1.75	1.75
Load Halfword	LH	2.0 + BX	2.25
Load Negative	LNR	1.75	1.75
Load Positive	LPR	1.75	1.75
Load PSW	LPSW	3.5 + BX	3.75
Move	MVI	2.75 + BX	3.00
Multiply	MR	10.75 + 0.5A	16.14
Multiply	M	11.25 + BX + 0.5A	16.89
Multiply Halfword	MH	7.75 + BX + 0.5A	10.72
OR	OR	1.75	1.75
OR	O	2.0 + BX	2.25
OR	OI	2.75 + BX	3.00
Set Program Mask	SPM	1.50	1.50
Set Storage Key	SSK	2.0	2.00
Set System Mask	SSM	2.5 + BX + 0.25OA	2.87
Shift Left Double	SLDA	3.0 + BX + 0.25 (S − 1)	
Shift Left Double Logical	SLDL	3.0 + BX + 0.25 (S − 1)	
Shift Left Single	SLA	2.25 + BX + 0.25 (S − 1)	
Shift Left Single Logical	SLL	2.25 + BX + 0.25 (S − 1)	
Shift Right Double	SRDA	3.0 + BX + 0.25 (S − 1)	
Shift Right Double Logical	SRDL	3.0 + BX + 0.25 (S − 1)	
Shift Right Single	SRA	2.25 + BX + 0.25 (S − 1)	

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Shift Right Single Logical	SRL	$2.25 + BX + 0.25\,(S - 1)$	
Start I/O	SIO	$HSMPX = 1 + BX + MM + 2BM + IFR\ (12 + SEL + CU)$ $MPX = 1 + BX + MM + BM + IFR\ (12 + SEL + CU)$	2.25 to 40.00
Store	ST	$2.25 + BX$	2.50
Store Character	STC	$2.25 + BX + 0.5EA$	2.75
Store Halfword	STH	$2.25 + BX$	2.50
Subtract	SR	1.75	1.75
Subtract	S	$2.0 + BX$	2.25
Subtract Halfword	SH	$2.0 + BX$	2.25
Subtract Logical	SLR	1.75	1.75
Subtract Logical	SL	$2.0 + BX$	2.25
Supervisor Call	SVC	1.0	1.00
Test and Set	TS	$2.5 + BX$	2.75
Test Channel	TCH	$1 + BX + MM + 2$	3.25 to 20.00
Test I/O	TIO	$HSMPX = 1 + BX + MM + 2BM + IFR\ (6 + SEL + CU)$ $MPX = 1 + BX + MM + BM + IFR\ (10 + SEL + CU)$	2.25 to 38.00
Test under Mask	TM	$2.0 + BX + 0.25OA$	2.37

Group 2: Floating-Point Timings with High-Speed General Registers

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Add Normalized (long)	ADR	$5.75 + 0.25\ (EXP^{14} + 6T^{1} + H^{14})$	6.28
Add Normalized (long)	AD	$6.75 + BX + 0.25\ (EXP^{14} + 6T^{1} + H^{14})$	7.53
Add Normalized (short)	AER	$3 + 0.25\ (EXP^{1} + EXP^{7} + 2T^{1}AT^{1}H^{6} + H^{7})$	3.81
Add Normalized (short)	AE	$3.5 + BX + 0.25\ (EXP^{1} + EXP^{7} + 2T^{1} + T^{1}H^{6} + H^{7})$	4.56
Add Unnormalized (long)	AWR	$5.75 + 0.25\ (EXP^{14} + 6T^{1})$	6.25

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Add Unnormalized (long)	AW	$6.75 + BX + 0.25 (EXP^{14} + 6T^{1})$	7.50
Add Unnormalized (short)	AUR	$3 + 0.25 (EXP^{1} + EXP^{7} + 3T^{1})$	3.79
Add Unnormalized (short)	AU	$3.5 + BX + 0.25 (EXP^{1} + EXP^{7} + 3T^{1})$	4.54
Compare (long)	CDR	$5.5 + 0.25EXP^{14}$	5.84
Compare (long)	CD	$6.5 + BX + 0.25EXP^{14}$	7.09
Compare (short)	CER	$3.0 + 0.25 (EXP^{1} + EXP^{7})$	3.50
Compare (short)	CE	$3.5 + BX + 0.25 (EXP^{1} + EXP^{7})$	4.25
Divide (long)			
32 bits	DDR	$31.25 + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	32.75
40 bits	DDR	$39.25 + (49.75 + 5G^{7}) LS^{8} + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	93.00
48 bits	DDR	$44.75 + (59.75 + 5G^{7}) LS^{16} + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	108.50
56 bits	DDR	$50.25 + (69.75 + 5G^{7}) LS^{24} + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	124.00
Divide (long)			
32 bits	DD	$32.25 + BX + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	34.00
40 bits	DD	$40.25 + BX + (49.75 + 5G^{7}) LS^{8} + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	94.25
48 bits	DD	$45.75 + BX + (59.75 + 5G^{7}) LS^{16} + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	109.75
56 bits	DD	$51.25 + BX + (69.75 + 5G^{7}) LS^{24} + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	125.25
Divide (short)	DER	$21.75 + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	23.25
Divide (short)	DE	$22.25 + BX + 0.25 (H^{1} - 1) + 0.25 (H^{2} - 1) + 3G^{7}$	24.00
Halve (long)	HDR	3.25	3.25
Halve (short)	HER	1.5	1.50

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Load (long)	LDR	3.0	3.00
Load (long)	LD	4.0 + BX	4.25
Load (short)	LER	1.0	1.00
Load (short)	LE	2.0 + BX	2.25
Load and Test (long)	LTDR	3.0	3.00
Load and Test (short)	LTER	1.0	1.00
Load Complement (long)	LCDR	3.0	3.00
Load Complement (short)	LCER	1.0	1.00
Load Negative (long)	LNDR	3.0	3.00
Load Negative (short)	LNER	1.0	1.00
Load Positive (long)	LPDR	3.0	3.00
Load Positive (short)	LPER	1.0	1.00
Multiply (long)			
32 bits	MDR	$3.75 + [12.0 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	21.14
40 bits	MDR	$3.75 + [30.75 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	44.06
48 bits	MDR	$3.75 + [35.25 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	52.72
56 bits	MDR	$3.75 + [39.75 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	61.39
Multiply (long)			
32 bits	MD	$4.75 + BX + [12.0 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	22.39
40 bits	MD	$4.75 + BX + [30.75 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	45.31
48 bits	MD	$4.75 + BX + [35.25 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	53.97
56 bits	MD	$4.75 + BX + [39.75 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	62.64
Multiply (short)	MER	$3.0 + G^6 (7.0 + 0.5A + 0.25H^{12})$	14.06

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Multiply (short)	ME	$3.5 + BX + G^{6}$ $(7.0 + 0.5A + 0.25H^{12})$	14.81
Store (long)	STD	$4.25 + BX$	4.50
Store (short)	STE	$2.25 + BX$	2.50
Subtract Normalized (long)	SDR	$5.75 + 0.25$ $(EXP^{14} + 6T^{1} + H^{14})$	6.28
Subtract Normalized (long)	SD	$6.75 + BX + 0.25$ $(EXP^{14} + 6T^{1} + H^{14})$	7.53
Subtract Normalized (short)	SER	$3.0 + 0.25$ $(EXP^{1} + EXP^{7} + 2T^{1} + T^{1}H^{6} + H^{7})$	3.81
Subtract Normalized (short)	SE	$3.5 + BX + 0.25$ $(EXP^{1} + EXP^{7} + 2T^{1} + T^{1}H^{6} + H^{7})$	4.56
Subtract Unnormalized (long)	SWR	$5.75 + 0.25\ (EXP^{14} + 6T^{1})$	6.25
Subtract Unnormalized (long)	SW	$6.75 + BX + 0.25$ $(EXP^{14} + 6T^{1})$	7.50
Subtract Unnormalized (short)	SUR	$3.0 + 0.25$ $(EXP^{1} + EXP^{7} + 3T^{1})$	3.79
Subtract Unnormalized (short)	SU	$3.5 + BX + 0.25$ $(EXP^{1} + EXP^{7} + 3T^{1})$	4.54

Group 3: Standard and Protection Timings without High-Speed General Registers

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Add	AR	3.75	3.75
Add	A	$3.75 + BX$	4.75
Add Halfword	AH	$3.75 + BX$	4.75
Add Logical	ALR	3.75	3.75
Add Logical	AL	$3.75 + BX$	4.75
AND	NR	3.75	3.75
AND	N	$3.75 + BX$	4.75
AND	NI	$2.75 + BX$	3.75
Branch and Link	BALR	3.25	3.25
Branch and Link	BAL	$2.25 + BX$	3.25
Branch on Condition	BCR	$1.0 + 1.5F^{1}$	1.75
Branch on Condition	BC	$1 + BX + 0.75F^{1}$	2.37
Branch on Count	BCTR	3.75	3.75
Branch on Count	BCT	$2.75 + BX$	3.75

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Compare	CR	3.0	3.00
Compare	C	3.0 + BX	4.00
Compare Halfword	CH	3.0 + BX	4.00
Compare Logical	CLR	3.0	3.00
Compare Logical	CL	3.0 + BX	4.00
Compare Logical	CLI	2.25 + BX	3.25
Divide	DR	31.75	31.75
Divide	D	31.75 + BX	32.75
Exclusive OR	XR	3.75	3.75
Exclusive OR	X	3.75 + BX	4.75
Exclusive OR	XI	2.75 + BX	3.75
Halt I/O	HIO	HSMPX = 1 + BX + MM + 2BM + IFR (5 + SEL + CU) MPX = 1 + BX + MM + BM + IFR (7 + SEL + CU)	3.00 to 35.00
Insert Character	IC	3.0 + BX	4.00
Insert Storage Key	ISK	3.5	3.50
Load	LR	3.0	3.00
Load	L	3.0 + BX	4.00
Load Address	LA	2.0 + BX	3.00
Load and Test	LTR	3.0	3.00
Load Complement	LCR	3.0	3.00
Load Halfword	LH	3.0 + BX	4.00
Load Negative	LNR	3.0	3.00
Load Positive	LPR	3.0	3.00
Load PSW	LPSW	3.5 + BX	4.50
Move	MVI	2.75 + BX	3.75
Multiply	MR	13.0 + 0.5A	18.39
Multiply	M	13.0 + BX + 0.5A	19.39
Multiply Halfword	MH	9.0 + BX + 0.5A	12.72
OR	OR	3.75	3.75
OR	O	3.75 + BX	4.75
OR	OI	2.75 + BX	3.75

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Set Program Mask	SPM	2.0	2.00
Set Storage Key	SSK	3.0	3.00
Set System Mask	SSM	2.5 + BX + 0.5OA	3.75
Shift Left Double	SLDA	5.5 + BX + 0.25 (S − 3)	
Shift Left Double Logical	SLDL	5.5 + BX + 0.25 (S − 3)	
Shift Left Single	SLA	3.5 + BX + 0.25 (S − 3)	
Shift Left Single Logical	SLL	3.5 + BX + 0.25 (S − 3)	
Shift Right Double	SRDA	5.5 + BX + 0.25 (S − 3)	
Shift Right Double Logical	SRDL	5.5 + BX + 0.25 (S − 3)	
Shift Right Single	SRA	3.5 + BX + 0.25 (S − 3)	
Shift Right Single Logical	SRL	3.5 + BX + 0.25 (S − 3)	
Start I/O	SIO	HSMPX = 1 + BX + MM + 2BM + IFR (12 + SEL + CU) MPX = 1 + BX + MM + BM + IFR (12 + SEL + CU)	3.00 to 40.00
Store	ST	3.25 + BX	4.25
Store Character	STC	3.25 + BX + 0.5EA	4.50
Store Halfword	STH	3.25 + BX	4.25
Subtract	SR	3.75	3.75
Subtract	S	3.75 + BX	4.75
Subtract Halfword	SH	3.75 + BX	4.75
Subtract Logical	SLR	3.75	3.75
Subtract Logical	SL	3.75 + BX	4.75
Supervisor Call	SVC	1.0	1.00
Test and Set	TS	2.5 + BX	3.50
Test Channel	TCH	1 + BX + MM + 2	4.00 to 20.00
Test I/O	TIO	HSMPX = 1 + BX + MM + 2BM + IFR (6 + SEL + CU) MPX = 1 + BX + MM + BM + IFR (10 + SEL + CU)	3.00 to 38.00
Test under Mask	TM	2.0 + BX + 0.25OA	3.12

Group 4: Floating-Point Timings without High-Speed General Registers

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Add Normalized (long)	ADR	$5.75 + 0.25$ $(EXP^{14} + 6T^{1} + H^{14})$	6.28
Add Normalized (long)	AD	$6.75 + BX + 0.25$ $(EXP^{14} + 6T^{1} + H^{14})$	8.28
Add Normalized (short)	AER	$3 + 0.25$ $(EXP^{1} + EXP^{7} + 2T^{1} + T^{1}H^{6} + H^{7})$	3.81
Add Normalized (short)	AE	$3.5 + BX + 0.25$ $(EXP^{1} + EXP^{7} + 2T^{1} + T^{1}H^{6} + H^{7})$	5.31
Add Unnormalized (long)	AWR	$5.75 + 0.25\ (EXP^{14} + 6T^{1})$	6.25
Add Unnormalized (long)	AW	$6.75 + BX + 0.25$ $(EXP^{14} + 6T^{1})$	8.25
Add Unnormalized (short)	AUR	$3 + 0.25$ $(EXP^{1} + EXP^{7} + 3T^{1})$	3.79
Add Unnormalized (short)	AU	$3.5 + BX + 0.25$ $(EXP^{1} + EXP^{7} + 3T^{1})$	5.29
Compare (long)	CDR	$5.5 + 0.25EXP^{14}$	5.84
Compare (long)	CD	$6.5 + BX + 0.25EXP^{14}$	7.84
Compare (short)	CER	$3.0 + 0.25\ (EXP^{1} + EXP^{7})$	3.50
Compare (short)	CE	$3.5 + BX + 0.25$ $(EXP^{1} + EXP^{7})$	5.00
Divide (long)			
32 bits	DDR	$31.25 + 0.25\ (H^{1} - 1)$ $+ 0.25\ (H^{2} - 1) + 3G^{7}$	32.75
40 bits	DDR	$39.25 + (49.75 + 5G^{7})\ LS^{8}$ $+ 0.25\ (H^{1} - 1)$ $+ 0.25\ (H^{2} - 1) + 3G^{7}$	93.00
48 bits	DDR	$44.75 + (59.75 + 5G^{7})\ LS^{16}$ $+ 0.25\ (H^{1} - 1)$ $+ 0.25\ (H^{2} - 1) + 3G^{7}$	108.50
56 bits	DDR	$50.25 + (69.75 + 5G^{7})\ LS^{24}$ $+ 0.25\ (H^{1} - 1)$ $+ 0.25\ (H^{2} - 1) + 3G^{7}$	124.00
Divide (long)			
32 bits	DD	$32.25 + BX + 0.25\ (H^{1} - 1)$ $+ 0.25\ (H^{2} - 1) + 3G^{7}$	34.75
40 bits	DD	$40.25 + BX$ $+ (49.75 + 5G^{7})\ LS^{8}$ $+ 0.25\ (H^{1} - 1)$ $+ 0.25\ (H^{2} - 1) + 3G^{7}$	95.00

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
48 bits	DD	$45.75 + BX + (59.75 + 5G^7)\ LS^{16} + 0.25\ (H^1 - 1) + 0.25\ (H^2 - 1) + 3G^7$	110.50
56 bits	DD	$51.25 + BX + (69.75 + 5G^7)\ LS^{24} + 0.25\ (H^1 - 1) + 0.25\ (H^2 - 1) + 3G^7$	126.00
Divide (short)	DER	$21.75 + 0.25\ (H^1 - 1) + 0.25\ (H^2 - 1) + 3G^7$	23.25
Divide (short)	DE	$22.25 + BX + 0.25\ (H^1 - 1) + 0.25\ (H^2 - 1) + 3G^7$	24.75
Halve (long)	HDR	3.25	3.25
Halve (short)	HER	1.5	1.50
Load (long)	LDR	3.0	3.00
Load (long)	LD	$4.0 + BX$	5.00
Load (short)	LER	1.0	1.00
Load (short)	LE	$2.0 + BX$	3.00
Load and Test (long)	LTDR	3.0	3.00
Load and Test (short)	LTER	1.0	1.00
Load Complement (long)	LCDR	3.0	3.00
Load Complement (short)	LCER	1.0	1.00
Load Negative (long)	LNDR	3.0	3.00
Load Negative (short)	LNER	1.0	1.00
Load Positive (long)	LPDR	3.0	3.00
Load Positive (short)	LPER	1.0	1.00
Multiply (long)			
32 bits	MDR	$3.75 + [12.0 + 0.5A + 0.25\ (H^1 - 1) + 0.25\ (H^2 - 1)]\ G^6$	21.14
40 bits	MDR	$3.75 + [30.75 + 0.5A + 0.25\ (H^1 - 1) + 0.25\ (H^2 - 1)]\ G^6$	44.06
48 bits	MDR	$3.75 + [35.25 + 0.5A + 0.25\ (H^1 - 1) + 0.25\ (H^2 - 1)]\ G^6$	52.72
56 bits	MDR	$3.75 + [39.75 + 0.5A + 0.25\ (H^1 - 1) + 0.25\ (H^2 - 1)]\ G^6$	61.39

INSTRUCTION	MNEMONIC	TIMING FORMULA	AVERAGE TIME (microseconds)
Multiply (long)			
32 bits	MD	$4.75 + BX + [12.0 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	23.14
40 bits	MD	$4.75 + BX + [30.75 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	46.06
48 bits	MD	$4.75 + BX + [35.25 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	54.72
56 bits	MD	$4.75 + BX + [39.75 + 0.5A + 0.25 (H^1 - 1) + 0.25 (H^2 - 1)] G^6$	63.39
Multiply (short)	MER	$3.0 + G^6 (7.0 + 0.5A + 0.25H^{12})$	14.06
Multiply (short)	ME	$3.5 + BX + G^6 (7.0 + 0.5A + 0.25H^{12})$	15.56
Store (long)	STD	$4.25 + BX$	5.25
Store (short)	STE	$2.25 + BX$	3.25
Subtract Normalized (long)	SDR	$5.75 + 0.25 (EXP^{14} + 6T^1 + H^{14})$	6.28
Subtract Normalized (long)	SD	$6.75 + BX + 0.25 (EXP^{14} + 6T^1 + H^{14})$	8.28
Subtract Normalized (short)	SER	$3.0 + 0.25 (EXP^1 + EXP^7 + 2T^1 + T^1H^6 + H^7)$	3.81
Subtract Normalized (short)	SE	$3.5 + BX + 0.25 (EXP^1 + EXP^7 + 2T^1 + T^1H^6 + H^7)$	5.31
Subtract Unnormalized (long)	SWR	$5.75 + 0.25 (EXP^{14} + 6T^1)$	6.25
Subtract Unnormalized (long)	SW	$6.75 + BX + 0.25 (EXP^{14} + 6T^1)$	8.25
Subtract Unnormalized (short)	SUR	$3.0 + 0.25 (EXP^1 + EXP^7 + 3T^1)$	3.79
Subtract Unnormalized (short)	SU	$3.5 + BX + 0.25 (EXP^1 + EXP^7 + 3T^1)$	5.29

Symbols Used in Timing Formulas

All times are in microseconds. A negative value of any expression in parentheses should be treated as zero.

A = The number of addition-subtraction cycles required during multiplication. Its value is data-dependent as follows:

In fixed point, the second operand is used as the multiplier.

In short-precision floating point, the first operand fraction is used as the multiplier.

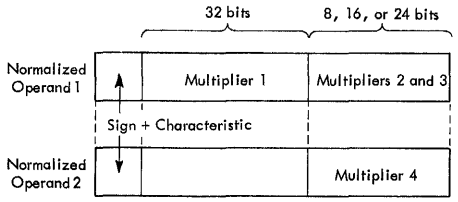
In 32-bit long-precision floating point, the normalized first operand fraction is used as the multiplier.

In 40-, 48-, and 56-bit long-precision floating point, four multipliers are used:

1. Multiplier 1 is the 32 most significant bits of the normalized first operand fraction.

2. Multipliers 2 and 3 are the 8/16/24 least significant bits of the normalized first operand fraction (used *twice* as multiplier).

3. Multiplier 4 is the 8/16/24 least significant bits of the normalized second operand fraction.



Proceeding from right to left through the multiplier or multipliers, underline from each two adjacent one bits (including these) to the next leftmost two adjacent zero bits (excluding these). For example:

10110010 10100110 11010110 01011101

Count 2 for each underline
plus 1 for each underlined zero
plus 1 for each non-underlined one
minus 1 if the leftmost bit is an underlined one.
For example:

3 underlines	6
5 underlined zeros	5
4 non-underlined ones	4
Leftmost underlined one	−1
	A = 14

A random pattern of n bits yields an average value of A equal to

$$\frac{(3n + 1 - (-0.5)^{n}),}{9}$$

or for specific word lengths:

	AVG VALUE OF A
Short precision	8.11
8 hex digits	10.77
10 hex digits	19.11
12 hex digits	27.44
14 hex digits	35.77
Fixed-point halfword	5.44
Fixed-point fullword	10.77

BM = 1 if the burst-mode state applies
= 0 if not*

BX = Base and indexing time

	SINGLE INDEXING	DOUBLE INDEXING
Basic Model 44	1.00	2.00
With HSGR feature	0.25	1.00

CU = Interface tag response delays in the addressed control unit. Minimum = 0 if fully overlapped with channel logic delays, maximum = 32 microseconds on HSMPX channel.**

EA = 1 if the effective storage address is even
= 0 otherwise

EXP^1 = 1 if the two exponents differ
= 0 otherwise

EXP^2 = the absolute value of the difference between the two exponents

$EXP^7 = EXP^2$ if $EXP^2 < 7$
$= 7$ if $EXP^2 \geq 7$

$EXP^{14} = 0$ if $EXP^2 = 0$ or 1
$= (EXP^2 - 1)$ if $1 < EXP^2 < 14$
$= 13$ if $EXP^2 \geq 14$

F^1 = 1 if the branch operation is successful
= 0 otherwise

G^6 = 1 if the second operand is non-zero
= 0 otherwise

G^7 = 1 if the absolute value of the normalized second operand fraction exceeds the absolute value of the normalized first operand fraction
= 0 otherwise

H^1 = the number of high-order hexadecimal zeros in the first operand fraction

H^2 = the number of high-order hexadecimal zeros in the second operand fraction

H^5 = the number of high-order hexadecimal zeros in the intermediate result fraction

$H^6 = 1$ if $H^5 \leq 1$
$= 0$ otherwise

$H^7 = 0$ if $H^5 = 0$ or 1
$= (H^5 - 1)$ if $1 < H^5 < 7$
$= 0$ if $H^5 \geq 7$ i.e., if the intermediate sum is zero

$H^{12} = 0$ if $H^5 = 0$ or 1
$= (H^5 - 1)$ if $1 < H^5 < 12$
$= 0$ if $H^5 \geq 12$

$H^{14} = 0$ if $H^5 = 0$ or 1
$= (H^5 - 1)$ if $1 < H^5 < 14$
$= 0$ if $H^5 \geq 14$ i.e., if the intermediate sum is zero

IFR = 1 if the interface-free state applies
= 0 if not*

LS^8 = 0 if the least significant 8 bits of the normalized 40-bit divisor are all zero
= 1 otherwise

LS^{16} = 0 if the least significant 16 bits of the normalized 48-bit divisor are all zero
= 1 otherwise

LS^{24} = 0 if the least significant 24 bits of the normalized 56-bit divisor are all zero
= 1 otherwise

MM = Delay while waiting for multiplex-mode state to end. Minimum = 0. Maximum = 100 for TCH, indefinite for HIO, SIO, or TIO.*

OA = 1 if the effective storage address is odd
= 0 otherwise

S = The number of bit positions of shifting called for

SEL = Time to propagate select-out to the addressed control unit. Minimum = 0, maximum = 17.5.**

T^1 = 1 if recomplementing is required
= 0 otherwise***

*See "Channel Architecture."
**See *Component Description* manual for the appropriate device/control unit.
***In short precision, if signs differ but exponents are equal, Model 44 complements the second operand. If signs differ and exponents differ, Model 44 complements the operand with the larger exponent.

In long precision, if signs differ but exponents are equal, Model 44 complements the first operand. If signs differ and exponents differ, Model 44 complements the operand with the smaller exponent.

Recomplementing is never required for a zero result.

Basis of Average Timings

Single indexing is assumed in all indexible instructions, except shift instructions; the variable BX is given the value 1.00 (basic) or 0.25usec (high-speed registers).

Successful and unsuccessful branches are assumed to have equal probability. Even and odd effective addresses in byte-handling instructions are assumed to have equal probability.

The operands in multiplication are assumed to have random bit patterns; the special effect of zero operands is ignored.

The average value of variables entering into floating-point formulas are based on trace information:

1. Frequency of alignment shifting for ADD, SUBTRACT, and COMPARE:

VALUE OF EXP^2	FREQUENCY
0	42.1
1	29.9
2	10.9
3	4.8
4-6	4.2
7-13	0.8
≥14	7.3
	100.0

2. Frequency of postnormalization shifting for ADD and SUBTRACT:

SHIFT	VALUE OF H^5	FREQUENCY
Overflow	0	4.35
0	0	81.70
1	1	6.95
2	2	3.05
3	3	1.15
≥4	≥4	2.00
Zero result	7 or 14	0.80
		100.00

3. Frequency of recomplementing in ADD and SUBTRACT (assuming that complementing occurs half the time):

Long precision: Because the shifted operand is complemented, recomplementing is assumed never to occur when exponents differ; from (1) above exponents are the same 42.1% of the time, complementing will occur 21% of the time, and recomplementing will occur 10.5% of the time.

Short precision: Because the unshifted operand is complemented, recomplementing is assumed on one quarter of the occasions when exponents are equal (10.5%) plus one half of the occasions when they differ (28.9%): total, 39.4%.

4. In floating-point MULTIPLY and DIVIDE, operands are assumed to be normalized, with post-shift required half the time.

The Model 44 uses the System/360 I/O interface. Command and data chaining are provided, as are all System/360 I/O instructions and channel commands and functions. All I/O operations overlap with processing.

The I/O control section consists of two parts, both physically integrated with the CPU: (1) the multiplexer (MPX) channel, and (2) the one or two high-speed multiplexer (HSMPX) channels. At least one channel must be installed, but the channel types are optional. The I/O equipment attachable to each channel is shown in Figure 9.

In the MPX channel, the information associated with a subchannel is kept in the extension of processor storage; in the HSMPX channels, this information is kept in the SLT registers associated with the high-speed channels. One set of SLT registers is provided for each HSMPX subchannel (see "Subchannels").

On any given channel operating in multiplex mode, the number of I/O devices that can transfer data simultaneously depends on:

1. The speed of the devices,
2. The maximum aggregate data transfer rate of the channel,
3. The use of chaining and transfer-in-channel (TIC) commands,
4. The number of subchannels composing the channel,
5. The number and type of I/O devices attached (via control units) to the channel.

Speed of Devices

Refer to the I/O device descriptions in *IBM System/360 System Summary,* Form A22-6810, or the I/O device publications listed in *IBM System/360 Bibliography,* Form A22-6822.

Data Transfer Rates

The data transfer rate of a single channel is not normally a limiting factor for devices operating in multiplex mode. However, the time available for data transfers on one channel (particularly the MPX) is decreased when any other channel is working. (See "Cross-Channel Interference.")

Chaining and TIC

The use of chaining and TIC commands increases the amount of cross-channel interference.

Subchannels

In the case of the MPX channel, the number of subchannels depends on the capacity of processor storage.

BYTES	WORDS	SUBCHANNELS
32,768	8,192	32
65,536	16,384	64
131,072	32,768	64
262,144	65,536	64

Each HSMPX channel equips the Model 44 with one high-speed subchannel; moreover, up to three additional high-speed subchannels can be installed in each HSMPX channel. Thus, the system maximum is eight HSMPX subchannels and 64 MPX subchannels.

Control Units and Devices

Up to eight control units can be attached to the MPX channel, and two control units can be attached for each HSMPX subchannel. The figure of two control units per HSMPX subchannel may vary as explained in item 5 in "Addressing" but the system maximum is 24 control units: 16 attached to high-speed subchannels (eight on each HSMPX channel) and eight attached to the MPX channel. In the following examples the console printer-keyboard and single-disk storage drive(s) require a total of two control-unit positions and two subchannels on the MPX channel, or two control-unit positions and one subchannel on the HSMPX channel.

Examples: If 63 MPX subchannels are in use for I/O devices or communication lines that are controlled via seven control units, the 64th subchannel is still available to attach a control unit (such as a tape control). To take another case, if an IBM 2702 Transmission Control that is to control 31 lines is attached, it would tie up 31 MPX subchannels. That would leave up to 33 subchannels or seven control units, whichever limit is reached first, for the use of other I/O devices attached via the MPX channel. In either case, the HSMPX channel capabilities remain available: up to eight control units for I/O devices per HSMPX channel. A system maximum of 72 devices (one for every MPX and HSMPX subchannel) may, if permitted by device and channel speeds, transfer data simultaneously.

Shared Subchannels

As in other models of the System/360, the first eight subchannels on the MPX channel are called shared subchannels. Thus, addresses 0 and 128-143 may refer to the same subchannel; however, devices cannot be in-

Device Name and Number with Exclusive Models			Attaches to Channel Via	Control Unit Type	Attaches to Model 44 Via (Channel Type)
No.	Model	Name			
1053	4	Printer	2848-1-3	---	M,H
1403	2,3,7,N1	Printer	2821-1,2,3,5	---	M,H
1442	N1	Card Read Punch	---	Single Path	M,H
1442	N2	Card Punch	---	Single Path	M,H
1443	N1	Printer	---	Single Path	M,H
1800	Data Acquisition and Control System		1827 or System/360 Adapter**	---	M,H
1827	Data Control Unit		---	Multipath	See 1800
2250	1	Display Unit	---	Single Path	M,H
2250	2	Display Unit	2840-1	---	M,H
2250	3	Display Unit	2840-2	---	M,H
2260	1	Display Station	2848-3	---	M,H
2260	2	Display Station	2848-1,2	---	M,H
2311	1	Disk Storage Drive	2841	---	M,H
2401	1-3	Magnetic Tape Unit	2803-1,2, or 2804-1,2, or 2403-1-6, or 2404-1-3	---	M,H
2401	4,5	Magnetic Tape Unit	2803-2, or 2804-2, or 2403-4-6	---	M,H
2401	6	Magnetic Tape Unit	2803-2, or 2804-2, or 2403-4-6	---	H
2402	1-3	Magnetic Tape Unit	2803-1,2 or 2804-1,2 or 2403-1-6, or 2404-1-3	---	M,H
2402	4,5	Magnetic Tape Unit	2803-2, or 2804-2, or 2403-4-6	---	M,H
2402	6	Magnetic Tape Unit	2803-2, or 2804-2, or 2403-4-6	---	H
2403	1-5	Magnetic Tape Unit and Control	---	Shared Path	M,H
2403	6	Magnetic Tape Unit and Control	---	Shared Path	H
2404	1-3	Magnetic Tape Unit and Control	---	Shared Path	M,H
2501	B1,B2	Card Reader	---	Single Path	M,H
2520	B1	Card Read Punch	---	Single Path	M,H
2520	B2,B3	Card Punch	---	Single Path	M,H
2540		Card Read Punch	2821-1,5	---	M,H
2671		Paper Tape Reader	2822	---	M,H
2701		Data Adapter Unit ***	---	Multipath	M,H
2702		Transmission Control ***	---	Multipath	M
2803	1	Tape Control	---	Shared Path	See 2401-1-3, 2402-1-3
2803	2	Tape Control	---	Shared Path	See 2401-1-6, 2402-1-6
2804	1	Tape Control	---	Shared Path	See 2401-1-3, 2402-1-3
2804	2	Tape Control	---	Shared Path	See 2401-1-6, 2402-1-6
2816	1	Switching Unit	2803-1,2 or 2403-1-6	---	See 2401-1-6, 2402-1-6, 2403-1-6
2821	1,5	Control Unit	---	Multipath	See 1403-2,3,7,N1, 2540
2821	2	Control Unit	---	Single Path	See 1403-2,3,7,N1
2821	3	Control Unit	---	Multipath	See 1403-2,3,7,N1
2822		Paper Tape Reader Control	---	Single Path	See 2671
2840	1	Display Control	---	Shared Path	See 2250-2
2840	2	Display Control	---	Shared Path	See 2250-3
2841		Storage Control	---	Shared Path	See 2311
2848	1-3	Display Control	---	Shared Path	See 2260-1,2
Channel-to-Channel Adapter			---	Single Path	See footnote****
Console Printer-Keyboard*			CPU Adapter	Single Path	M,H1
Single-Disk Storage Drive*			CPU Adapter	Shared Path	M,H
System/360 Adapter			---	Single Path	See 1800

* Standard feature of Model 44.

** System/360 adapter is installed in the 1826 Data Adapter Unit of the attached 1800 system. The 1827 permits attachment of 1800 process I/O equipment without use of an 1801 or 1802 Processor-Controller.

*** Used to attach a wide variety of teleprocessing systems or terminals, process control devices, and non-IBM communication equipment and (with 2701) data communication devices. See IBM System/360 Data Communications and Acquisition Configurator, Form A22-6824, also 2701 or 2702 in IBM System/360 Bibliography, Form A22-6822.

**** Channel-to-channel adapter, installed in Model 30, 40, or 50 CPU or in a 2860 Selector Channel, can provide high-speed intersystem communication.

M = Multiplexer channel
H = High-Speed Multiplexer Channel
H1 = First High-Speed Multiplexer Channel

Single Path = Only one device is associated with the control unit.
Shared Path = Only one attached device at a time is in a data-transferring operation. When attached to M, a shared subchannel may be used; where more than 16 devices can be attached (e.g., the 2848-3), a second shared subchannel is used. Where H is specified, the equivalent sharing capability of its subchannels is used.
Multipath = Attached devices are in data-transferring operations simultaneously. When attached to M, each device requires one nonshared subchannel.

• Figure 9. Device Attachment Data

stalled for both the single address and the set of 16 addresses in the same system. (Likewise, either 7 or 241-256, but not both in the same installation.) All I/O devices are attached to a channel via a control unit, or its equivalent in the form of an adapter in the CPU or a control section within the device; this control unit can be described as one of three types: "shared path," "single path," or "multipath." A shared subchannel may be assigned at the time of installation to only one of the three types:

1. *A "Shared-Path" Control Unit:* In this case, up to 16 devices can be addressed by the subchannel, of which one device at a time can be in a data-transferring operation, although all other devices attached through the same shared-path control unit can be engaged in free-running operations such as tape rewinding.

EXAMPLES OF SHARED-PATH CONTROL UNITS

IBM 2841 Storage Control
IBM 2803 Tape Control
Single-Disk Storage Drive Adapter (adapter acts as control)

2. *A "Single-Path" Control Unit:* The subchannel is associated with a single eight-bit device address.

EXAMPLES OF SINGLE-PATH CONTROL UNITS

IBM 1442 Card Read Punch Model N1 (has internal control)
IBM 2822 Paper Tape Reader Control

3. *One Path of a "Multipath" Control Unit:* The subchannel is associated with a single eight-bit device address. (Exceptionally, two or more addresses in a block of 16 addresses may be assigned to IBM 1827 Data Control Unit functions.)

EXAMPLES OF MULTIPATH CONTROL UNITS

IBM 2821 Control Unit Model 1, 3, or 5
IBM 1827 Data Control Unit
IBM 2701 Data Adapter Unit

Addressing

The addressing of shared and non-shared subchannels and devices is done within the general architectural rules defined in the "Input/Output Device Addressing" section of *IBM System/360 Principles of Operation,* Form A22-6821. Specifics for the Model 44 follow.

Of the 11 bits of addressing that specify the channel, subchannel, and device to be used in an I/O operation, the three high-order bits are assigned to specify the channel as follows:

000 — MPX channel
001 — HSMPX channel 1
010 — HSMPX channel 2

The eight low-order bits specify the subchannel and the device:

For Shared MPX Subchannels, indicated by 1 in the high-order position: 1 xxx yyyy (xxx specifies one of the eight subchannels that can be shared; yyyy specifies one of the 16 devices using subchannel and control unit xxx). If a shared subchannel is to be used as a non-shared subchannel and associated with a single device address instead of a set of 16, the subchannel address is at the right in the following table. Either address may be chosen, but the unused alternative *must* be left unassigned.

DEVICE ADDRESS FOR SHARED MPX		SUBCHANNEL
Shared Use	Non-Shared Use	
1000 yyyy	0000 0000	0
1001 yyyy	0000 0001	1
1010 yyyy	0000 0010	2
1011 yyyy	0000 0011	3
1100 yyyy	0000 0100	4
1101 yyyy	0000 0101	5
1110 yyyy	0000 0110	6
1111 yyyy	0000 0111	7

For Non-Shared MPX Subchannels, indicated by 0 in the high-order position: 0 0xx xxxx (xx xxxx specifies one of the non-shared subchannels and its control unit and device — up to 64 subchannels, depending on processor storage size, less the number of subchannels being used as shared subchannels).

DEVICE ADDRESS FOR NON-SHARED MPX		SUBCHANNELS
0000 1000 to 0001 1111	(All Model 44's)	8-31
0010 0000 to 0011 1111	(Not Model E44)	32-63

For HSMPX Subchannels, all having the shared capability: 1 hhc xxxx (hh specifies one of the four possible HSMPX subchannels on that channel and c distinguishes between the two control-unit data paths on that subchannel. Where 1 hhc identifies a shared-path control unit, xxxx is used to specify one of the 16 attached devices. Where 1 hhc identifies either a single-path control unit or one path of a multipath control unit, only one value of xxxx is significant because the unshared data path assumes a single eight-bit device address.)

DEVICE ADDRESS FOR ALL HSMPX	SUBCHANNEL	ASSIGNMENT EXAMPLE
1000 xxxx	A	1827 — 1st of two digital inputs*
1001 xxxx		2848 — 1st sixteen 2260's (1-16)
1010 xxxx	B	2701 — 1st of two adapters
1011 xxxx		1827 — 1st of three analog inputs**
1100 xxxx	C	2701 — 2nd adapter
1101 xxxx		1827 — 2nd analog input
1110 xxxx	D	2848 — remaining eight 2260's (17-24)
1111 xxxx		1827 — 3rd analog input
		1827 — 2nd digital input
		1827 — digital/analog output

*Requires more than one 1827 (only one digital input per 1827).
**A full analog input function requires three device assignments for the same analog input function.

The results or ramifications of several addressing facts are demonstrated by the last example:

1. Although the 1827 is not a shared-path control unit, a device attached to an 1827 may share a block of 16 addresses with other devices so attached, but not with any non-1827 device.

2. Analog input basic features, attached via 1827's, must be assigned to different subchannels.

3. If 1827 digital input or digital/analog output devices must operate at the same time as analog input, they must be assigned a different subchannel; however, if they need not operate simultaneously and independently, they may not only share a subchannel with one of the analog input devices, but they may also share a block of 16 addresses with one of the analog input devices.

4. Assignment of 2260 Display Stations 17-24 to a second HSMPX subchannel (rather than to the second control-unit position on the same subchannel) can be done to permit other devices to be spread over more subchannels. If all 2260's had been assigned to subchannel 0 in the preceding example, the 1827 devices could not have been assigned according to items 2 and 3.

5. On an HSMPX subchannel, each device address associated with a non-shared-path control unit falls in a separate and non-shared block of 16 addresses. Multipath control units such as the 2701 and 2821 usually need more than one such block of 16, reducing the number of attachable control units to less than two per subchannel. The 1827, however, is unique: two or more 1827's may share the same block of 16 addresses and increase the number of attachable control units to more than two per subchannel.

Burst Mode

Burst mode is a method of operation forced by many control units and adapters for high-speed synchronous devices; it is not under the control of the programmer. For example, magnetic tape control units, the IBM 2841 Storage Control, the single-disk storage drive adapter, and the IBM 2840 Display Control, all force burst mode.

In burst mode, either type of multiplexer channel (MPX or HSMPX) operates similar to a selector channel, which has only one subchannel. Only one device at a time communicates with the CPU via the particular channel, but communication is at a higher maximum data rate than in the multiplex mode and (in the case of the MPX channel) the interference with CPU operation, per byte of I/O data transferred, is reduced.

Control units (or equivalent adapters for devices) that force burst mode are listed under "Cross-Channel Interference" (see items 4 and 5 of "Type I Interference").

Multiplex Mode

In multiplex mode, each channel can concurrently sustain one data-transferring I/O operation per subchannel, provided that the aggregate data rate does not exceed the channel capacity. Thus:

1. The MPX channel may be capable of simultaneous communication with as many I/O devices as can be attached to it (up to 64, via no more than eight control units).

2. Each HSMPX channel may be capable of simultaneous communication with as many I/O devices as there are subchannels in that channel (up to four).

Channel Architecture

The following description of the interface states of Model 44 channels amplifies information in other IBM publications* but does not imply incompatibility with other models of the System/360.

For simplicity, the phrase "multiplexer channel" is used to apply equally, in this section, to the MPX and HSMPX channels.

States of the I/O Interface

The interface of a Model 44 channel is at any time in one of three states:

Interface free	IFR
Interface working in multiplex mode	MM
Interface working in burst mode	BM

Interface Free (IFR): In the basic Model 44, IFR is logically defined as: (not operational in) AND (not request in) AND (no channel-initiated communication sequence is taking place over the interface) AND (channel delay complete). Briefly, no control-unit selection or channel-initiated operation exists or is required on the interface and the channel's 400-nanosecond internal delay following a communication sequence is completed.

If the priority interrupt feature is installed, IFR is defined as: (not operational in) AND (no channel-initiated communication sequence is taking place over the interface) AND (channel delay complete) AND [(not request in) OR (priority interruption requested and enabled)]. The state IFR is created in two ways:

1. The same conditions exist as given for the basic Model 44, provided that no enabled priority interruption request exists.

IBM System/360 Principles of Operation, Form A22-6821, and *IBM System/360 I/O Interface — Channel to Control Unit, Original Equipment Manufacturers' Information*, Form A22-6843.

2. The CPU is attempting to select the channel to execute an I/O instruction, no control-unit selection or channel-initiated operation exists on the interface, the channel's internal delay is timed out, and a priority interruption request exists at any enabled level. Under these conditions, request in is ignored in an attempt to create IFR as soon as possible.

As a rule in the System/360 channel architecture, a new I/O operation can be started only after the channel has serviced all outstanding requests for data transfer from devices previously placed in operation. Installation of the priority interrupt feature causes Model 44 to differ only in this way: when a priority interruption is requested while the CPU is attempting to execute an I/O instruction, the I/O operation is started as soon as possible (in order to release the CPU for the interruption) even if there are outstanding requests for data transfer.

NOTE: The priority interrupt feature is described in *Data Acquisition Special Features for the IBM System/360 Model 44,* Form A22-6900.

Interface Working in Multiplex Mode (MM): This state is defined as the absence of states IFR and BM. Either one of the interface signals, request in or operational in, must be present, or the channel must be in the process of selecting a device. Because any of these conditions may also be present in state BM, they do not define state MM.

Interface Working in Burst Mode (BM): A multiplexer channel runs a timer whenever the operational in line is up or command chaining is in process after device end. The timer is reset on the fall of operational in, unless command chaining is indicated in response to the device end. The BM state exists when the value of the channel timer exceeds 100 microseconds (nominal). In other words, every selection of a control unit on the interface is monitored by the channel, and, for the first 100 microseconds of every selection, the channel is in the MM state but thereafter is in the BM state.

NOTE: For any multiplexer channel, a direct transition from state IFR to state BM cannot occur; all other transitions can occur.

Forcing Burst Mode

Devices such as tapes and disks "force burst mode." Such devices, having established a logical connection with a channel, usually stay connected for the duration of data transfer, thereby forcing the channel to reach the BM state. The BM state does not exist for multiplexer channels during the first 100 microseconds of an interface sequence, and does not necessarily extend until the device presents the ending status. The device may drop off for a time between data transfers before presenting ending status.

A multiplexer channel may appear to be in burst mode as a result of command chaining. More specifically, the channel keeps its timer running between the acceptance of device-end status, with command chaining indicated, and reselection for the chained command; and if the selection lasts for more than 100 microseconds, the channel enters the BM state.

The significant differences between a multiplexer channel and a selector channel are:

1. Selector channels have only the interface states IFR and BM.

   Multiplexer channels have the additional state MM.

2. Although all channels act to force burst mode, in effect, between device end and reselection for command chaining, a selector channel also creates the BM state (its only active state) by keeping the select-out interface line in the up state from the time of selection until channel end — and, if command chaining is indicated with channel end, from selection through channel end to device end.

   A multiplexer channel cannot do this.

3. A selector channel cannot be simultaneously in the interruption-pending state (as the result of status provided by the device) and in the BM state.

   A multiplexer channel can be.

NOTE: Both types of channels, while transferring data in burst mode, can be in the interruption-pending state if the PCI flag is set and signals for program-controlled interruptions.

Multiplexing Devices

"Multiplexing" devices cannot force burst mode; they are designed to complete an interface sequence in less than about 32 microseconds. It is possible, however, for several sequences of a multiplexing device to become joined by command chaining; and if the joined sequences last for 100 microseconds, the BM state is forced even though the device is of the multiplexing type.

Programming Aspects

The following points apply to overlapped Model 44 multiplexer channels.

1. The instructions START I/O, TEST I/O, and HALT I/O cannot be executed by a Model 44 channel in the MM state; if such an instruction is fetched by the CPU while the addressed channel is in the MM state, the CPU must wait until the state changes to IFR or BM. Unless an enabled priority interruption request is received, there is no logical limit to the duration of the MM state; but a duration of more than 100 microseconds is statistically improbable with any I/O configuration.

NOTE: An interruption request signal, whether from the priority interrupt feature or the standard interruption system, is often called an "interrupt." This provides a distinction between a request signal and (after the interrupt has been accepted) the actual performance by the CPU of the procedure known as the "interruption."

2. Because interface states can change unpredictably, the programmer aware of the present state of a channel cannot foresee its state in the immediate future. In particular, when a unit-check condition appears in a CSW, there is no warranty that the interface will immediately be free (IFR) for a sense command. A condition code 2 (channel or subchannel busy) is not an unusual response to a START I/O instruction where the first command is a sense.

3. A channel scheduler that queues an I/O request after receiving condition code 2 cannot rely on a channel-end I/O interrupt to signal the end of the BM state; the time when this interrupt will occur is not always predictable.

The generation of condition code 2 indicates that some device is working; therefore, that a channel-end interrupt must eventually occur unless a system reset occurs first. With most devices the channel-end interrupt occurs soon enough to avoid seriously delaying the CPU or causing the channel scheduler to appear inefficient. However, during a manual input operation the console printer-keyboard may take several seconds to present channel end; more importantly, a 2701 or 2702 executing an enable command can take an indefinite time before presenting channel end. Therefore, it is possible, though unlikely and entailing an unusual command chaining sequence, for the 2701, the 2702, or the printer-keyboard to (1) create the BM state, (2) cause an I/O request to be queued by the channel scheduler, then (3) delay channel-end status.

Channel Interference

The HSMPX subchannels delay the CPU about 0.5 microsecond per byte of data transferred. The following cause this figure to increase:

Use of data chaining
Use of TIC commands
Use of the PCI flag to cause program-controlled interruptions (PCI's).

The MPX channel operating in burst mode delays the CPU about 1.0 microsecond per byte of data transferred; data chaining, TIC commands, and PCI's increase this figure. The MPX subchannel operating in multiplex mode delays the CPU up to 5 microseconds per byte. This figure increases if data chaining, TIC commands, or PCI's are used; it decreases if the I/O device control unit sends more than one byte at a time in multiplex mode.

HSMPX data accesses to processor (main) storage are for halfwords, at 1 microsecond each, unless the specification of the channel command word (CCW) data address forces a 1-microsecond access for a single byte at the beginning or end of a logical record.

MPX data accesses to main storage are for single bytes at 1 microsecond each. As indicated in the following table, 4 microseconds are added when operation is in multiplex mode: this accounts for two 1-microsecond accesses when the control unit gains selection, and two more when the control unit disconnects from the interface.

Because a storage access by a channel does not stop the compute clock unless it causes the CPU to wait for a storage cycle, channel interference is slightly less than the following (in microseconds):

	MPX (MULTIPLEX MODE)	MPX (BURST MODE)	HSMPX
For Data			
Group of n bytes per selection	4 + n		
Per byte		1	
Per two bytes			1
Chaining (per link)			
Command chaining	8	4	4
Data chaining	4	4	4
TIC (per command)	2	2	2

Cross-Channel Interference

This is either intrachannel or interchannel interference, and is caused by contention among I/O devices. It is of two types:

TYPE	CAUSE
I	The devices are on the same MPX or HSMPX channel and are contending for use of the interface.
II	The devices are on different channels and are contending for access to storage.

Type II interference is significant, and type I interference is normally insignificant.

Type I Interference

Type I (interface) interference is insignificant when the devices' control units have the following normal priority arrangement:

1. Synchronous Unbuffered Multiplexing Devices: The devices in this group should be arranged in the order of increasing waiting time, with those having the fastest character rate placed first.

1442-N1 Card Read Punch used to read and punch concurrently
2501-B1, B2 Card Reader
2520-B1 Card Read Punch used to read and punch concurrently
2702 Transmission Control

2. Synchronous Buffered Multiplexing Devices: The devices in this group should be arranged in the order of increasing waiting time, with those having the fastest character rate placed first.

2520-B1 Card Read Punch used to punch only
2520-B2, B3 Card Punch

3. Asynchronous Buffered Multiplexing Devices: To permit the devices in this group to run at their maximum character rates, they should be arranged in the order of increasing waiting time, with those having the fastest character rate placed first.

1443-N1 Printer
1827 Data Control Unit
2821-1,2,3,5/1403-2,3,7,N1 Control Unit and Printer
2821-1,5/2540 Control Unit and Card Read Punch
2822/2671 Control Unit and Paper Tape Reader

4. Burst-Mode Devices Time-Dependent on Command Chaining:

2701 Data Adapter Unit
2841//2311-1 Storage Control and Disk Storage Drive

5. Other Burst-Mode Devices:

2250-1 Display Unit
2400-series Magnetic Tape Units and Controls
2840-1/2250-2 Display Control and Display Unit
2840-2/2250-3 Display Control and Display Unit
2848-1,2/2260-2 Display Control and Display Station
2848-3/2260-1 Display Control and Display Station
2848-1,2,3/1053-4 Display Control and Printer
Channel-to-Channel Adapter on other System/360
Single-Disk Storage Drive
System/360 Adapter on 1800 system

6. Asynchronous Unbuffered Multiplexing Devices:

1442-N1 Card Read Punch used to punch only
1442-N2 Card Punch
Console Printer-Keyboard

NOTE: Critical time (waiting time) directly concerns only the synchronous multiplexing devices (whether buffered or unbuffered) in priorities 1 and 2, but is also of indirect concern to the asynchronous buffered multiplexing devices in priority 3.

The critical time before overrun can occur is constant for any device, regardless of the channel to which it is attached; the shortest critical time (waiting time) for any device attachable to Model 44 is the 800 microseconds of the 1442 Card Read Punch.

The duration of multiplex-mode bursts on the channel interface is, however, much less than this shortest critical time. A sequence lasting more than 32 microseconds is exceptional, and will not occur under normal programming (see note).

For example, the interface time to transfer a burst of four bytes to a 1403 printer, with data chaining every byte, is unlikely to be more than 40 microseconds; and command chaining with NO-OP, command immediate, and TIC is unlikely to take more than 50 microseconds with any device. It is almost impossible to create enough type I interference to add up to 800 microseconds and cause overrun of a byte-multiplexing device on a Model 44 channel. Even with eight 1442's on a channel, all using TIC and data chaining, an overrun cannot be created.

NOTE: Normal programming is stipulated only because a sequence of 20 NO-OP commands, chained to each other, can be specified if an overrun must be forced. A channel program without unnecessary NO-OP's cannot cause type I overrun.

Type II Interference

Devices sensitive to type II interference (contention for storage) are the unbuffered burst-mode devices; multiplexing devices are affected only insignificantly.

Overrun occurs if a channel cannot obtain its required storage accesses in the time permitted by the device, or more specifically in the portion of that time left available by an interfering channel. The total time depends on the actual speed of the device, and the time required for data transfers by a given channel are shown under "Channel Interference." It is necessary to establish the probability of obtaining this time when there is contention for storage.

A channel may fail to obtain consecutive storage cycles because of contention. Even when there is no contention for storage, however, the channel may fail to obtain or even to request consecutive storage cycles; this can occur when the channel is transferring data (as opposed to fetching a CCW), and happens for one of the following reasons:

1. When operating with a relatively low-speed I/O device, the channel does not request consecutive storage cycles because it cannot go faster than the device.
2. When operating with an extremely high-speed device, the channel may be unable to obtain consecutive storage cycles for the simple reason that the channel (which in this case would logically be the HSMPX channel) cannot request its two-byte storage accesses more often than about once each 2 microseconds.

When consecutive storage cycles are demanded by the channel but are not obtained, the demands are always honored in subsequent cycles. In the high-speed case, excessive delay in obtaining the storage cycles may result in overrunning the device.

The amount of type II cross-channel interference depends on how often the interfering channel can demand storage cycles: its "demand rate."

The Demand Rate for steady-state data transfers in burst mode is set by the I/O device. The MPX channel, transferring one byte of data per storage access to or from a 90kb device such as the single-disk storage drive, demands a storage access every 11 microseconds

(or perhaps every 10 microseconds if the device operates well above its nominal speed). An HSMPX channel, transferring two bytes of data per storage access to or from a device of 90kb nominal speed, demands a storage access every 22 microseconds (for worst-case calculations, every 20 microseconds). If the device is indefinitely fast (e.g., a Model 65 connected via a channel-to-channel adapter), the demand rate of the Model 44 channel is limited only by interface and channel logic delays: the HSMPX can demand a storage cycle about every 2 microseconds (as stated previously), and the MPX can demand a storage cycle about every 2.5 microseconds. Contention for storage prevents any of these maximum demand rates from being sustained.

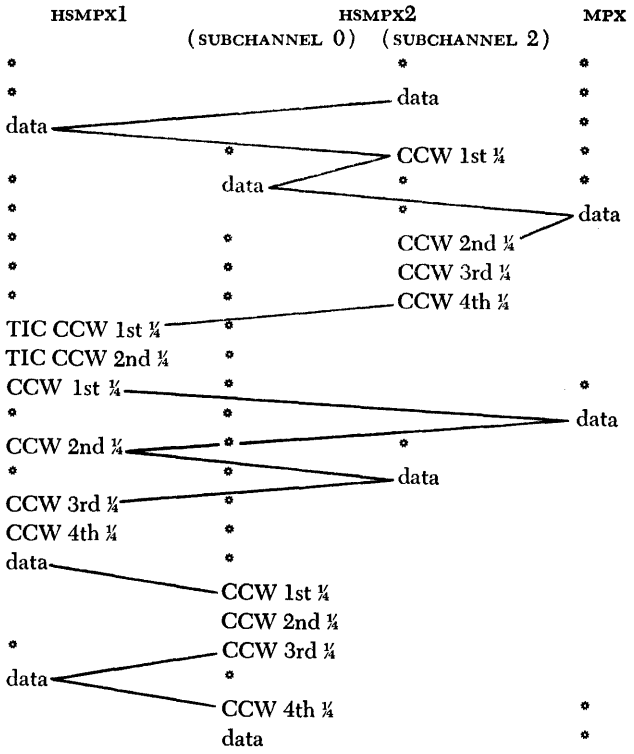
Effects of Data Chaining on Demand Rate: During a storage data cycle, a channel decrements its count. If the count reaches zero and data chaining is indicated, the channel demands four consecutive storage accesses to fetch a new CCW. (This demand becomes effective too late to obtain the first storage cycle that follows the data transfer cycle.) If a TIC CCW is detected, two additional cycles are demanded, for a total of six CCW cycles. Accordingly, the maximum demand rate of a channel during chaining is about 7.5 microseconds for seven cycles. (The extra 0.5 microsecond is the minimum time to obtain a storage access to fetch the new CCW.)

In multiplex mode, different subchannels may initiate data-chaining requests at 3-microsecond intervals; at the extreme, therefore, a single channel using data chaining with several devices can demand an indefinite number of consecutive storage cycles.

Priority Among Contending Channels: Only one HSMPX subchannel at a time can demand a CCW fetch cycle. The following priority scheme makes use of this fact to guarantee the MPX channel — if it is running in burst mode — a minimum frequency of storage accesses.

1. HSMPX1 and HSMPX2 data cycles (alternating in top priority).
2. HSMPX, cycles for bits 0-15, 32-47, and 48-63 of a CCW (first, third and fourth quarters).
3. MPX, data cycles in burst mode.
4. HSMPX, cycles for bits 16-31 of a CCW (second quarter).
5. MPX, data cycles in multiplex mode and MPX CCW cycles.

Demonstration of Priority: Let the first HSMPX channel be data chaining with TIC in burst mode. Let the second HSMPX channel be data chaining on two subchannels in multiplex mode. Let the MPX channel be operating in burst mode without data chaining. Then, with asterisks indicating when a subchannel is waiting for a storage cycle, a typical sequence of obtaining storage cycles is as follows:



Estimation of Storage Access Delay: It requires 0.5 microsecond to obtain a storage access when there is no contention. If storage is busy at the time of the request, it may take up to 2 microseconds longer; in particular, execution of the LPSW instruction involves a 2-microsecond use of storage during which channel break-in is not permitted.

HSMPX burst-mode data cycles can be held off for 2.5 microseconds, when two HSMPX channels make a simultaneous request of this type, one of them may be held off for 3.5 microseconds.

When a subchannel (either MPX or HSMPX) is fetching a CCW, or waiting for a CCW to be fetched, no data transfer for that subchannel is permitted. The channel does not accept input bytes from a device until the new CCW has been entirely fetched and checked for possible program errors (such as a zero count field). When both HSMPX channels request CCW fetching, one of them will obtain the four or six CCW cycles ahead of the other. The time for HSMPX data chaining is thus seriously limited, especially in multiplex mode, by the demand rate of other HSMPX subchannels.

In estimating the data-chaining performance of HSMPX1 in burst mode, a hold-off of 6 microseconds should be included if HSMPX2 is working, on the grounds that command chaining with TIC must be

allowed on HSMPX2. If MPX is working in burst mode, an allowance should also be added for MPX data cycles.

Several byte-multiplexing devices working on one HSMPX channel can hold off a burst-mode CCW fetch on the other HSMPX channel for an estimated 15 microseconds, but an overrun caused by this unusual duration would almost certainly be recoverable by a retry at the device associated with the overrun.

The MPX channel can be held off from multiplex-mode data cycles or CCW cycles (these having fifth and lowest priority) for extended periods by HSMPX activity. An MPX data request in burst mode has third priority, however, and cannot be held off for more than about 6 microseconds by HSMPX channels, as determined by the probable worst-case sequence of HSMPX demands:

CCW 2nd ¼
data
CCW 3rd ¼
CCW 4th ¼
CCW 1st ¼
data

MPX data chaining is heavily exposed to hold-off by HSMPX channels.

Channel Buffering: The MPX channel has no data buffering, and the entire time for a storage access, including hold-offs by HSMPX channels, must be allowed between adjacent bytes received from or sent to an I/O device via the MPX channel.

Each HSMPX subchannel has a two-byte data register and a single-byte interface register. These registers provide, in effect, one byte of data buffering during normal data transfer; therefore, the worst-case delay in obtaining a storage cycle can in practice be spread over two byte cycles of the device as in the following example.

DEVICE OFFERS DATA	SUBCHANNEL INTERFACE REGISTER CONTENTS	SUBCHANNEL DATA REGISTER CONTENTS	STORAGE ACCESS
byte 1			
	byte 1		
		byte 1	
		1	
		1	
byte 2		1	
	byte 2	1	
		bytes 1, 2	requested
		1, 2	
		1, 2	
byte 3		1, 2	
	byte 3	1, 2	
	3	1, 2	
	3	1, 2	
	3	1, 2	
byte 4	3	1, 2	
	3	1, 2	
byte 5		bytes 3, 4	requested
	byte 5		obtained
		byte 5	

NOTE: When data chaining is indicated, no further bytes are accepted into the interface register; hence, CCW accesses must be obtained between adjacent bytes from the device.

The HSMPX channels provide no buffering when data chaining is used; the time for data chaining, including any storage hold-offs, must be allowed between adjacent bytes at the interface.

In all cases, buffering in the I/O control unit can relieve the timing limitation at the channel.

Maximum Safe Data Rates: Figure 10 combines the above principles with I/O control-unit buffering information to estimate the types of I/O devices that are either safe from overrun or may overrun.

"Safe" means that overrun should not be expected; it is logically possible but abnormal, and should not recur on a retry.

NOTE: For the HSMPX channel, some combinations labelled safe can overrun if data chaining is used to link single-byte logical records: byte, chain, byte, chain, etc. — an inadvisable method of programming.

"May overrun" means that overruns should be expected; the frequency, and the likelihood of successful recovery on retry, can be estimated by using the principles described.

Multisystems

The channel-to-channel adapter is not presently available for the Model 44; multisystems composed exclusively of Model 44's permit communication among processing units via shared I/O devices only. However, Model 44 can be connected to any other model of the System/360 that has the channel-to-channel adapter feature or to an IBM 1800 Data Acquisition and Control System that has a System/360 adapter; either kind of adapter can then be brought into play to provide faster transmissions between systems. The adapter takes one control-unit position of an MPX or HSMPX channel.

The transmission rate from channel to channel is limited by the maximum data-transfer rate of the lower-speed channel.

The channel-to-channel adapter operates in burst mode; therefore, it cannot operate simultaneously with another unit on the same channel.

HSMPX CHANNEL

A magnetic tape (240x) or direct-access (2311 or SDSD*) operation is "Safe" from overrun or "May Overrun," depending on (1) whether the operation uses data chaining, and (2) the condition of the other channels.

Condition of Other Channels	No Data Chaining	Data Chaining Without TIC	Data Chaining With TIC
Not Working or Not Installed	Safe All attachable devices	Safe 240x-1,2,3,4 SDSD May Overrun 240x-5,6 2311	Safe 240x-1,2,3,4 SDSD May Overrun 240x-5,6 2311
MPX Only Working	Safe All attachable devices	Safe 240x-1,2,3,4 SDSD May Overrun 240x-5,6 2311	Safe 240x-1,2,4 SDSD May Overrun 240x-3,5,6 2311
Other HSMPX Only Working	Safe All attachable devices	Safe 240x-1,2,4 May Overrun 240x-3,5,6 2311 SDSD	Safe 240x-1 May Overrun 240x-2,3,4,5,6 2311 SDSD
Both MPX and Other HSMPX Working	Safe All attachable devices	Safe 240x-1 May Overrun 240x-2,3,4,5,6 2311 SDSD	Safe 240x-1 May Overrun 240x-2,3,4,5,6 2311 SDSD

MPX CHANNEL

A magnetic tape (240x) or direct-access (2311 or SDSD*) operation is "Safe" from overrun or "May Overrun," depending on (1) whether the operation uses data chaining, and (2) the condition of the HSMPX channel(s).

Condition of HSMPX Channel(s)	No Data Chaining	Data Chaining Without TIC	Data Chaining With TIC
Not Working or Not Installed	Safe All attachable devices	Safe 240x-1,2,3,4 SDSD May Overrun 240x-5 2311	Safe 240x-1,2,4 SDSD May Overrun 240x-3,5 2311
Only One Working	Safe 240x-1,2,3,4 SDSD May Overrun 240x-5 2311	Safe 240x-1,2 May Overrun 240x-3,4,5 2311 SDSD	Safe 240x-1 May Overrun 240x-2,3,4,5 2311 SDSD
Both Working	Safe 240x-1,2,3,4 SDSD May Overrun 240x-5 2311	Safe 240x-1 May Overrun 240x-2,3,4,5 2311 SDSD	Safe 240x-1 May Overrun 240x-2,3,4,5 2311 SDSD

*In the tabular notations:

SDSD refers to the Single-Disk Storage Drive(s).
240x-1,2,3 . . .refers to IBM 2401, 2402, 2403 Magnetic Tape Unit Models 1-6 (or 2404 Models 1-3). Model 6 is not attachable to the MPX channel.

Figure 10. I/O Activities Susceptible of Overrun

The system control panel (Figure 11) contains the switches and lights necessary to operate and control the system. The system consists of the CPU, storage, channels, on-line control units, and I/O devices. Off-line control units and I/O devices, although they may be part of the system environment, are not considered part of the system proper.

System controls are considered to be grouped in three classes, and are so physically oriented on the system control panel:

Operator control
Operator intervention
Customer engineering (CE) control

Figure 11 is divided into labeled areas for reference. The operator control section is virtually limited to areas B and G, and the left half of area F. The operator intervention controls appear on (but do not wholly occupy) areas D and E as well as the right half of area F. Operator interventions may also require the use of some of the CE controls and lights that occupy the remaining areas.

Area A contains the CPU usage meter, the CE usage meter, and the CE keylock switch. Area C contains lights primarily useful to customer engineers. Area H contains the two roller switches, both of which are set to position 1 during normal operations.

System Control Functions

Using the control panel, the operator can reset the system; store and display information in storage, in registers, and in the program status word (PSW); and perform initial program loading (IPL).

System Reset

This function suspends all instruction processing and timer updating, resets the channels, and resets on-line control units and I/O devices that are unshared by other CPU's.

The CPU is placed in the stopped state and all pending interruptions are eliminated. All error lights are turned off.

In general, the system is placed in such a state that processing can be initiated without the occurrence of machine checks, except for those caused by subsequent machine malfunction.

The reset state for a control unit or device is described in the appropriate System Reference Library (SRL) publication. A system-reset signal from a CPU resets only the functions in a shared control unit or device belonging to that CPU. Any function pertaining to another CPU remains undisturbed.

The system-reset function is performed when the system-reset key is pressed, when IPL is initiated, when a power-on sequence is performed, or when PSW restart is initiated (see "PSW Restart Key").

Programming Notes

If the system reset occurs in the middle of an operation, the contents of the PSW and of result registers or storage locations are unpredictable. If the CPU is in the wait state when the system reset is performed, and I/O is not operating, this uncertainty is eliminated.

A system reset does not correct parity in storage. Because a machine check occurs when information with incorrect parity is used, the incorrect information should be replaced by loading new information.

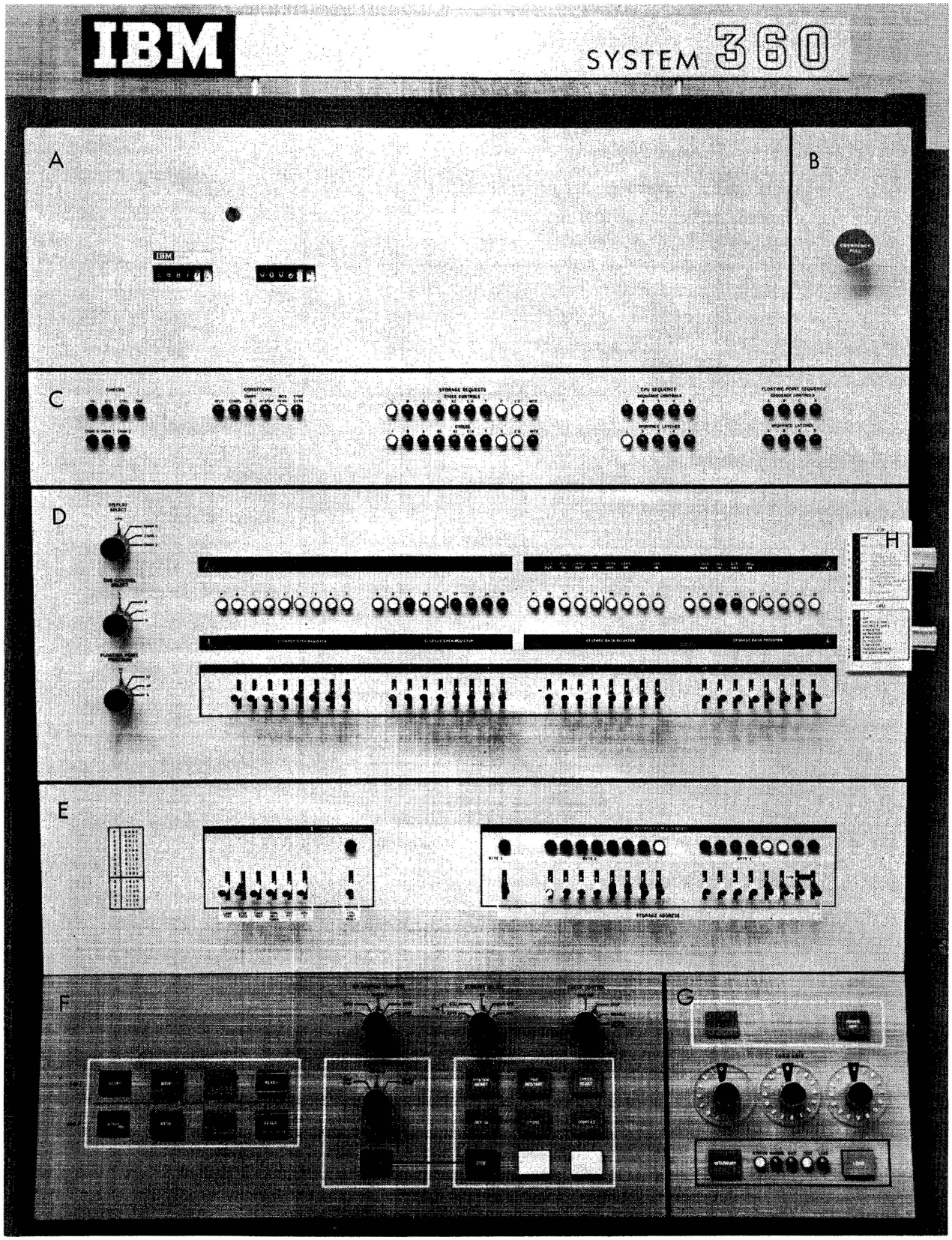
Store and Display

Certain controls in the operator intervention group permit storing and displaying data during manual intervention in the progress of a program. This manual intervention is begun by placing the CPU in the stopped state. The CPU enters the stopped state when the stop key is pressed, when single instruction execution is specified (by the rate switch setting of INSN STEP), or when a preset address is reached (see "MS Address Compare Switch").

The operator then uses the address switches, data switches, storage select switch, store key, and display key to store and/or display information in main storage, in general and floating-point registers, and in the PSW. Once the desired intervention is complete, the CPU can be started again.

The stopping and starting of the CPU does not in itself cause any alteration in program execution other than the time element involved in the transition from operating to stopped state.

Machine checks that occur during store or display operations do not interrupt or log immediately, but may create a pending interruption. This interrupt can be eliminated by a system reset. A pending interruption, when not disallowed, will be taken when the CPU is returned to the operating state.



• Figure 11. System Control Panel

Initial Program Loading

Initial Program Loading (IPL) is provided for the initiation of processing when the contents of storage or the PSW are not suitable for further processing.

IPL is started manually by using the load-unit switches to select the input device that contains the program and pressing the load key.

Pressing the load key causes a system reset, turns on the load light, and starts a read operation from the selected input device. The first 24 bytes read are placed in storage locations 0-23. If the selected input device is a disk, the IPL information is read from track 0. Storage protection, program-controlled interrupts, and a possible incorrect-length indication are ignored. The double word starting at location 8 is used as the channel command word (CCW) to continue the input operation under control of the channel. When chaining is specified in this CCW, the operation proceeds with the second CCW starting at storage location 16.

After the input operation ends, the I/O address is stored in bits 21-31 of the first word in storage. Bits 16-20 are made zero. Bits 0-15 remain unchanged. The CPU fetches the first two words in storage for a new PSW and proceeds under control of this new PSW. The load light is turned off.

At this point, the loader-portion of the first program is loaded. The IPL continues with the loading of programs or continuations of programs stored on the selected input device.

Programming Notes

Initial program loading resembles a START I/O that specifies the I/O device selected in the load-unit switches and a zero protection key. The CCW for this START I/O is simulated by CPU circuitry and contains a read command, zero data address, a byte count of 24, chain-command flag on, suppress-length-indication flag on, program-controlled-interruption flag off, chain-data flag off and skip flag off. The CCW has a virtual address of zero.

After the new information is read into the first six words of storage, the remainder of the IPL program may be placed in any desired section of storage.

The selected input device may be the channel-to-channel adapter connecting the channels of two CPU's. After a system reset is performed and a Read command is issued to the adapter by the requesting CPU, the adapter sends an attention signal to the addressed CPU. That CPU should then issue the write command necessary to load a program into main storage of the requesting CPU.

When the PSW starting at location 0 has bit 14 set to one, the CPU is in the wait state after the IPL procedure; the manual, the system, and the load lights are off, and the wait light is on. Interruptions that are requested during IPL are taken, if allowed, before instruction execution begins.

When the load light goes off, the loader portion of the first program is loaded. The continuing procedure for IPL varies slightly (but is nearly if not wholly automatic) if stand-alone programs are being loaded, with program execution to follow either immediately or, if the CPU is placed in the wait state at the end of IPL, upon receipt of the signal to exit from the wait state. If the control program is being loaded, additional procedures for the operator are required.

Operator Control Section

This section of the system control panel contains (except for the emergency pull switch) the only controls needed by the operator when the CPU is operating under full supervisor control.

The main functions provided by the operator control section (Figure 12) are:

Control and indication of system power
Indication of system status
Initial program loading
Control and status indication of single-disk storage drives

The operator controls and lights are (in alphabetical order):

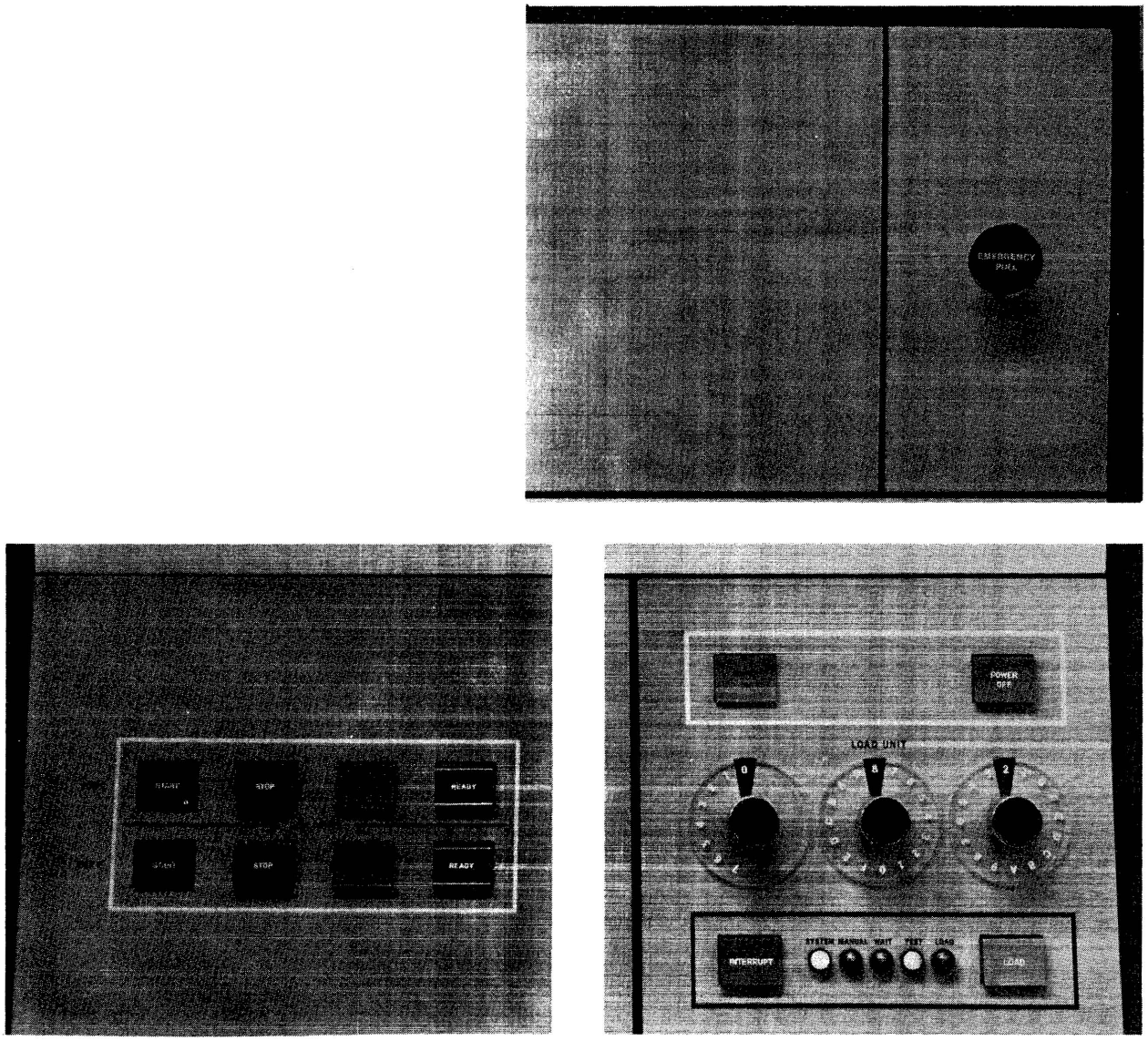
NAME	IMPLEMENTATION
Cartridge Unlocked (Disk)	Two lights
Emergency Pull	Pull switch
Interrupt	Key
Load	Key
Load	Light
Load Unit	Three rotary switches
Manual	Light
Power Off	Key
Power On	Key
Ready (Disk)	Two lights
Start (Disk)	Two keys
Stop (Disk)	Two keys
System	Light
Test	Light
Wait	Light

Cartridge-Unlocked Lights (Disk)

A light indicates that the associated single-disk storage drive is fully stopped and the operator is able to remove its cartridge. Neither this nor the ready light is on while the drive is decelerating; the drive slows to a stop in two minutes or less.

Emergency Pull Switch

Pulling this switch drops power at the primary power input to the CPU and all connected devices that are part of the system or can be switched onto the system, including I/O control units and devices that are off-line or shared by other CPU's. For emergency power



•Figure 12. Operator Controls (Areas B, F, and G)

off on multisystems, as many as six emergency pull switches are interconnected.

The switch latches in the out position and can be restored to its in position by maintenance personnel only.

When the emergency pull switch is in the out position, the power-on key is ineffective.

Interrupt Key

Pressing this key requests an external interruption. The interruption request remains pending if the interruption is disallowed or the CPU is stopped. Bit 25 in the interruption-code portion of the current PSW is made one to indicate that pressing the interrupt key is the cause of the external interruption.

The key is effective while power is on the system.

Load Key

Pressing this key starts IPL. The loading is from the input device selected by the three load-unit switches. Pressing the load key causes a system reset and loads the first 24 bytes of information from the input device into the first 24 bytes of main storage.

The key is effective while power is on the system.

Load Light

This light is on during IPL; it is turned on when the load key is pressed, and is turned off after the loading of the new PSW has been successfully completed.

Load-Unit Switches

Three rotary switches provide the 11-bit address of the channel and device to be used for initial program loading.

The leftmost rotary switch has eight positions, labeled 0-7, and is used to select the channel address. The other two are 16-position rotary switches, labeled with the hexadecimal characters 0-F, and are used to select the subchannel, control unit, and device (see "Addressing").

Manual Light

This light is on when the CPU is stopped. Several manual controls are effective only when the manual light is on. To exit from the stopped state, see "Start Key (CPU)."

Power-Off Key

The single-disk storage drive(s) must be individually turned off before this key is pressed. Pressing the power-off key initiates the power-off sequence of the system; about 5 seconds elapse between pressing the key and removal of power.

The contents of main storage (but not protection keys in storage) are preserved, provided that the CPU is in the stopped state. The general and floating-point registers may be affected.

Power-On Key

Pressing this key initiates the system power-on sequence and causes a system reset. After about 90 seconds, the sequence is complete; this is indicated when the power-on key lights up.

The system reset is performed in such a manner that the system executes no instructions or I/O operations until explicitly directed (the normal stopped state). The contents of main storage are preserved.

The power-on key is effective only when the emergency pull switch is in the normal (in) position.

Ready Lights (Disk)

A light turns on when the associated single-disk storage drive is up to full speed, operational, and ready for a seek command. Neither this nor the cartridge-unlocked light is on while the drive is accelerating; the drive achieves full rotational speed in 2 minutes or less.

Start Keys (Disk)

Pressing one of these keys starts the associated single-disk storage drive motor. If only one drive is installed, the disk 0 key is used; if both drives are installed and are to be started, the disk 0 and disk 1 keys are used.

Stop Keys (Disk)

Pressing one of these keys turns off the associated single-disk storage drive motor. If only one drive is installed, the disk 0 key is used. If both drives are installed and are to be turned off, the disk 0 and disk 1 keys are used.

If a cartridge is to be replaced, it is necessary to wait for the drive to come to a complete stop; this is indicated when the associated cartridge-unlocked light turns on.

System Light

This light is on when the CPU usage meter or CE usage meter is running.

When the CE keylock switch is turned off (counterclockwise, toward the CPU usage meter) and the system is doing productive work, the CPU usage meter accumulates time.

The manual light and wait light indications are independent of each other; the system light indication is a function of both the CPU and I/O states. The following table shows possible conditions when power is on:

SYSTEM LIGHT	MANUAL LIGHT	WAIT LIGHT	CPU STATE	I/O STATE
off	off	off	Rate switch on SINGLE CYCLE	
off	off	on	Wait	Not working
off	on	off	Stopped	Not working
off	on	on	Stopped, wait	Not working
on	off	off	Running	Undetermined
on	off	on	Wait	Working
on	on	off	Stopped	Working
on	on	on	Stopped, wait	Working

Test Light

This light is on when a manual control is not in its normal position or when a maintenance function is being performed for the CPU, including channels and storage.

Any abnormal switch setting on the system control panel that can affect the normal operation of a program causes the test light to be on.

The test light does not reflect the state of marginal voltage controls.

Wait Light

This light is on when the CPU is in the wait state. Exit is only by a new PSW, e.g. through external or I/O interruption or IPL.

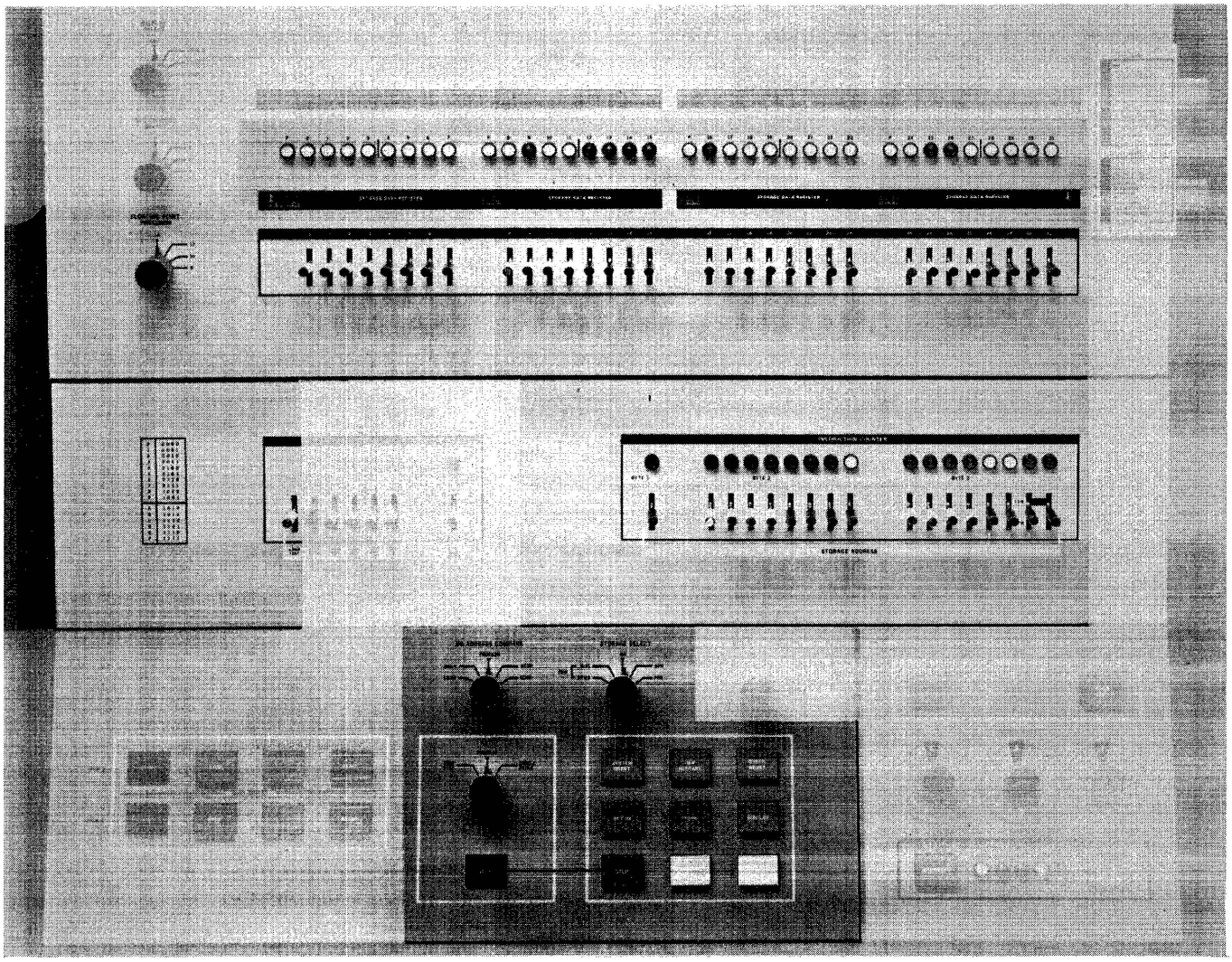
Operator Intervention Controls

Areas D, E, and F of the system control panel contain most of the controls required for the operator to intervene in normal programmed operation (Figure 13). These controls are intermixed with CE controls and lights that are located in the same areas.

Operator intervention provides the system-reset and the store-and-display functions.

The operator intervention controls are (in alphabetical order):

NAME	IMPLEMENTATION
Address	17 toggle switches (18 on H44)
Check Reset	Key
Data	32 toggle switches
Data	36 lights
Display	Key
Floating-Point Precision	Rotary switch
Instruction Counter	17 lights (18 on H44)
Lamp Test	Toggle switch
MS Address Compare	Rotary switch
PSW Restart	Key
Rate	Rotary switch
Set IC	Key
Start (CPU)	Key
Stop (CPU)	Key
Storage Select	Rotary Switch
Store	Key
System Reset	Key



•Figure 13. Operator Intervention Controls (Areas D, E, and F)

Address Switches

These switches provide a 17- or 18-bit address by means of 17 or (for H44) 18 toggle switches, of which the four rightmost, labeled GPR, are used to address a general (purpose) register; and the three labeled FPR are used to address halves of a floating-point register. The group of switches as a whole can be used to address any word in storage, or to stop the CPU at an equal address comparison. The 16 (or 17) high-order switches provide an address that can be loaded into the instruction counter. Correct address parity is generated.

Although enough switches are provided to address a single byte in a 262,144-byte storage, addresses are specified by word and not by byte. This means that switches 30 and 31 (rightmost) are ignored when the toggle switches are used to address storage.

The address switches can be manipulated without disrupting CPU operations and are normally used for:

Comparison by selecting a 17- (or 18-) bit address to be compared with any address in storage. Address switch 31 is ignored. The purpose is to stop the CPU when the comparison is equal. Example: processing a segment of a program to examine the results. This function is performed when the MS address compare switch is set at STOP.

Instruction-Counter Loading by selecting a 17- (or 18-) bit address to be loaded into the instruction counter when the set IC key is pressed. Address switch 31 is ignored. The purpose is to set in, or manually branch to, the instruction address where the program is to start.

Storage Addressing by selecting a 17- (or 18-) bit storage address to either store the word selected with the 32 data switches, or display (on the data lights in the center of the panel) the word of data at this address. Address switches 30 and 31 are ignored. The store or the display key initiates this function when the storage select switch is set at MS.

General Register Selection by selecting a four-bit address that identifies a general (purpose) register to either store the word selected with the 32 data switches, or display (on the data lights) the contents of this general register. The store or the display key initiates this function when the storage select switch is set at GPR.

GENERAL REGISTER	ADDRESS-SWITCH SETTING (0 = normal; 1 = down) 28	29	30	31
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Floating-Point Register Selection by selecting a two-bit address that identifies a floating-point register to either store the word selected with the 32 data switches, or display (on the data lights) the contents of this floating-point register. A third address bit, in the rightmost position, identifies which half of the 64-bit floating-point register is affected. The store or the display key initiates this function when the storage select switch is set at FPR.

FLOATING-POINT REGISTER	BITS	ADDRESS-SWITCH SETTING (0 = normal; 1 = down) 29	30	31
0	0-31	0	0	0
	32-63	0	0	1
2	0-31	0	1	0
	32-63	0	1	1
4	0-31	1	0	0
	32-63	1	0	1
6	0-31	1	1	0
	32-63	1	1	1

Check Reset Key

Pressing this key resets all error lights on the system control panel.

Data Switches

These 32 toggle switches (in area D) provide the data to be stored in main storage, in a general register, a floating-point register, or in the PSW. These switches are used in conjunction with the address switches, storage select switch, or store key, as described for those controls. The number of data switches is sufficient to permit storing of a fullword, with correct data parity being automatically generated.

Data Lights

These 36 lights display one of the following, as governed by the setting of the storage select switch and by pressing the display key:

1. The word of data at the main storage location specified by the address switches.
2. The contents of the general or floating-point register specified by the address switches.

3. Either half of the current PSW.

All 32 bits and the four associated parity bits are displayed, except as described for the PSW under "Storage Select Switch."

Display Key

Pressing this key causes the data lights to display one of the following, as selected by the storage select switch:

1. The word of data at the main storage location specified by the address switches.
2. The contents of the general or floating-point register specified by the address switches.
3. Either half of the current PSW. (For this function, see "Storage Select Switch.")

When the designated location is not available, the displayed information is unpredictable.

The key is effective only while the CPU is in the stopped state.

Floating-Point Precision Switch

This rotary switch enables the operator to select 4 degrees of precision (32-, 40-, 48-, or 56-bit fraction length) to be used in the processing of long-precision floating-point arithmetic (see Figure 6).

Instruction-Counter Lights

These 17 lights (18 for Model H44) automatically display the 17 (or 18) low-order bits of the instruction counter. These bits make up the instruction-address part of the current PSW.

Lamp Test Switch

Pushing this toggle switch down tests the ability of all panel lights to turn on.

MS Address Compare Switch

This rotary switch is used to stop the CPU on a successfull address comparison. It has two positions, PROCESS and STOP, for the use of operators; the other positions are for the use of customer engineers.

The switch has no effect on CPU operations when it is set at the PROCESS position. Setting the switch at the STOP position causes the address selected on the address switches to be compared with main storage addresses encountered as the program runs; when they match, the CPU enters the stopped state.

NOTE: Entering the stopped state means that the CPU will stop at the end of the current instruction, but any interruption allowed and pending will be taken before the CPU stops, and any current I/O operation will continue to completion.

The MS address compare switch can be switched between the PROCESS and STOP settings without disrupting CPU operation other than by causing the address-comparison stop. When it is set to any position except PROCESS, the test light is on.

PSW Restart Key

Pressing this key causes a system reset, which is followed by the loading of a PSW from location zero (bytes 0-7). Processing then starts, automatically, under control of the new PSW, using the instruction at the location in the instruction counter.

Rate Switch

This rotary switch indicates the manner in which instructions are to be performed. The position of the rate switch should be changed only while the CPU is in the stopped state. Otherwise, unpredictable results occur.

The switch has three positions: PROCESS, INSN STEP, and SINGLE CYCLE.

When the switch is in the PROCESS position, the system starts operating at normal speed when the start key is pressed. The test light is on when the rate switch is not set to PROCESS.

When the rate switch is set to INSN STEP and the CPU is in the stopped state, pressing the start key causes one complete instruction to be performed. All pending, allowed interruptions are subsequently taken. The CPU next returns to the stopped state. When the CPU is in the wait state, no instruction is performed but pending interruptions, if any, are taken before the CPU returns to the stopped state.

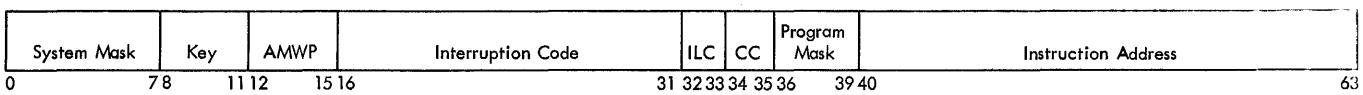
Any type of instruction can be executed with the rate switch set to INSN STEP and I/O operations are completed to the interrupt point. However, initial program loading is completed with the loading of the new PSW before any instruction is performed and the timer is not updated while the rate switch is set to INSN STEP.

The SINGLE CYCLE position is for the use of customer engineers.

Set IC Key

Pressing this key loads the instruction counter with the bits provided by the leftmost 16 (for H44, 17) address switches. The 17 (or 18) bits in the instruction counter make up the instruction-address part of the current PSW. The instruction address is entered in bits 47-63 (or 46-63) of the current PSW, as shown in Figure 14. Bit 63 must be zero; accordingly, the rightmost address switch is not used in this function and its information is ignored.

The key is effective only while the CPU is in the stopped state.



Bit Position	Displayed As	Indication
0,1,...	0,1,...	(For channel 0, 1, etc.) 1 = I/O interruption allowed, 0 = I/O interruption disallowed.
7	7	(For timer, interrupt key, other external) 1 = external interruption allowed, 0 = external interruption disallowed.
8-11	8-11	Protection key (0000 if no protection feature).
12	12	(A) 1 = USASCII-8 code, 0 = EBCDIC.
13	13	(M) 1 = machine-check interruption allowed, 0 = machine-check interruption disallowed.
14	14	(W) 1 = wait state, 0 = running state.
15	15	(P) 1 = problem state, 0 = supervisor state.
16-31	16-31	Interruption code.
32,33	0,1	Instruction length code.
34,35	2,3	Condition code for the instruction.
36-39	4-7	Each 1 = interruption results from the associated program exception, each 0 = no interruption results from the associated program exception. (The state of bit-position 39 also influences floating-point addition and subtraction.)
40-45	8-13	Inapplicable to Model 44.
46	14	High-order instruction address bit-position for H44.
47-63	15-31	Instruction address bit-positions for any Model 44.

•Figure 14. Bits in Program Status Word

Start Key (CPU)

Pressing this key starts instruction execution. The first instruction address used, when the CPU starts normal program execution, is that contained in the instruction counter when this key is pressed.

Pressing the start key after a normal stop causes instruction processing to continue as if no stop had occurred. Pressing the start key after system reset, without first introducing a new instruction address, yields unpredictable results.

The key is effective only while the CPU is in the stopped state.

Stop Key (CPU)

Pressing this key causes the CPU to enter the stopped state. The CPU will stop at the end of the current instruction, after all allowed and pending interruptions have been taken and all current I/O operations have continued to completion. The stop key is effective while power is on the system.

Programming Notes

Pressing the stop key has no effect when a continuous string of interruptions is performed or when the CPU is unable to complete an instruction because of machine malfunction. The effect of pressing the stop key is indicated by the turn-on of the manual light as the CPU stops.

Storage Select Switch

This rotary switch is used to select a register, storage, or PSW, for the purpose of either changing its information or displaying its contents. This switch has five positions:

MS — selects main storage.
GPR — selects general (purpose) registers.
FPR — selects floating-point registers.
PSW (0-31) — selects bits 0-31 of the current PSW.
PSW (32-63) — selects bits 32-63 of the current PSW.

The exact storage location or the particular register is identified under "Address Switches."

To store the 32 bits of data provided by the data switches into main storage or a register, the store key is pressed. All 32 bits in the location are affected. If the display key is pressed, the data lights display the word of data indicated by the storage address on the address switches, or the contents of the register indicated by the address switches.

Storing or displaying in the PSW positions does not involve the address switches.

On PSW 0-31, only bits 0-15 are affected. The interruption code in bits 16-31 is formed only at the time of an interruption and therefore cannot be displayed or stored. Also, in a store operation the correct protection key (or all zeros) must be selected on data switches 8-11 to avoid an interruption, even if the protection feature is not installed.

On PSW 32-63, bits 32-63 can be displayed but only bits 34-63 can be stored. On a store, the ILC bits (32 and 33) remain unchanged.

The storage select switch can be rotated without disrupting CPU operations.

Store Key

Pressing this key stores the data provided by the data switches into one of the following locations, as selected by the storage select switch:

1. The main storage location specified by the storage address on the address switches. (Storage protection is ignored.)
2. The general or floating-point register specified by the address switches.
3. Either half of the current PSW. (For this function, see "Storage Select Switch.")

The key is effective only while the CPU is in the stopped state.

System-Reset Key

Pressing this key causes a system reset. The CPU assumes the stopped state, error lights (if any) are reset, and all pending interruptions are eliminated. For other particulars, see "System Reset" as previously described.

The key is effective while power is on the system.

Index

READER'S COMMENT FORM

IBM System/360 Model 44
Functional Characteristics

A22-6875-5

- How did you use this publication?

  As a reference source ☐
  As a classroom text ☐
  As a self-study text ☐

- Based on your own experience, rate this publication...

As a reference source:	..... Very Good	..... Good	..... Fair	..... Poor	..... Very Poor
As a text:	..... Very Good	..... Good	..... Fair	..... Poor	..... Very Poor

- What is your occupation? .....

- We would appreciate your other comments; please give specific page and line references where appropriate. If you wish a reply, be sure to include your name and address.

- **Thank you for your cooperation. No postage necessary if mailed in the U.S.A.**

YOUR COMMENTS PLEASE . . .

This SRL bulletin is one of a series which serves as reference sources for systems analysts, programmers and operators of IBM systems. Your answers to the questions on the back of this form, together with your comments, will help us produce better publications for your use. Each reply will be carefully reviewed by the persons responsible for writing and publishing this material. All comments and suggestions become the property of IBM.

Please note: Requests for copies of publications and for assistance in utilizing your IBM system should be directed to your IBM representative or to the IBM sales office serving your locality.

fold fold

FIRST CLASS
PERMIT NO. 419
POUGHKEEPSIE, N.Y.

BUSINESS REPLY MAIL
NO POSTAGE NECESSARY IF MAILED IN THE UNITED STATES

POSTAGE WILL BE PAID BY . . .

IBM CORPORATION
P.O. BOX 390
POUGHKEEPSIE, N.Y. 12602

ATTENTION: CUSTOMER MANUALS , DEPT. B98

fold fold

IBM

International Business Machines Corporation
Data Processing Division
112 East Post Road, White Plains, N.Y. 10601
[USA Only]

IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
[International]

Printed in U.S.A. A22-6875-5

Printed in U.S.A. A22-6875-5

International Business Machines Corporation
Data Processing Division
112 East Post Road, White Plains, N.Y. 10601
[USA Only]

IBM World Trade Corporation
821 United Nations Plaza, New York, New York 10017
[International]