

**IBM** Field Engineering  
Diagram Manual

**IBM Confidential**

**System/360 Model 50  
2050 Processing Unit**

Z22-2833-4

Fifth Edition (July 1966)

This edition, Form Z22-2833-4, is a major revision of, and obsoletes, Form Z22-2833-3. All IDB's and the CLF's for I-Fetch have been updated to show the latest CAS pages and ROS addresses. The UDC's show additional logic and reference information. IOP pages 201 through 210 have been updated and ROS routines added where applicable.

A new system data flow diagram (SDF 000) shows the following:

1. Major data paths between logical units of the system.
2. Major control lines within the system.
3. Form numbers of manuals related to logical units and control functions within the system.

Changed or new diagrams are indicated by a vertical line in the table of contents and by the symbol ● to the left of the diagram title.

Significant changes or additions to the specifications contained in this publication will be reported in subsequent revisions or FE Supplements.

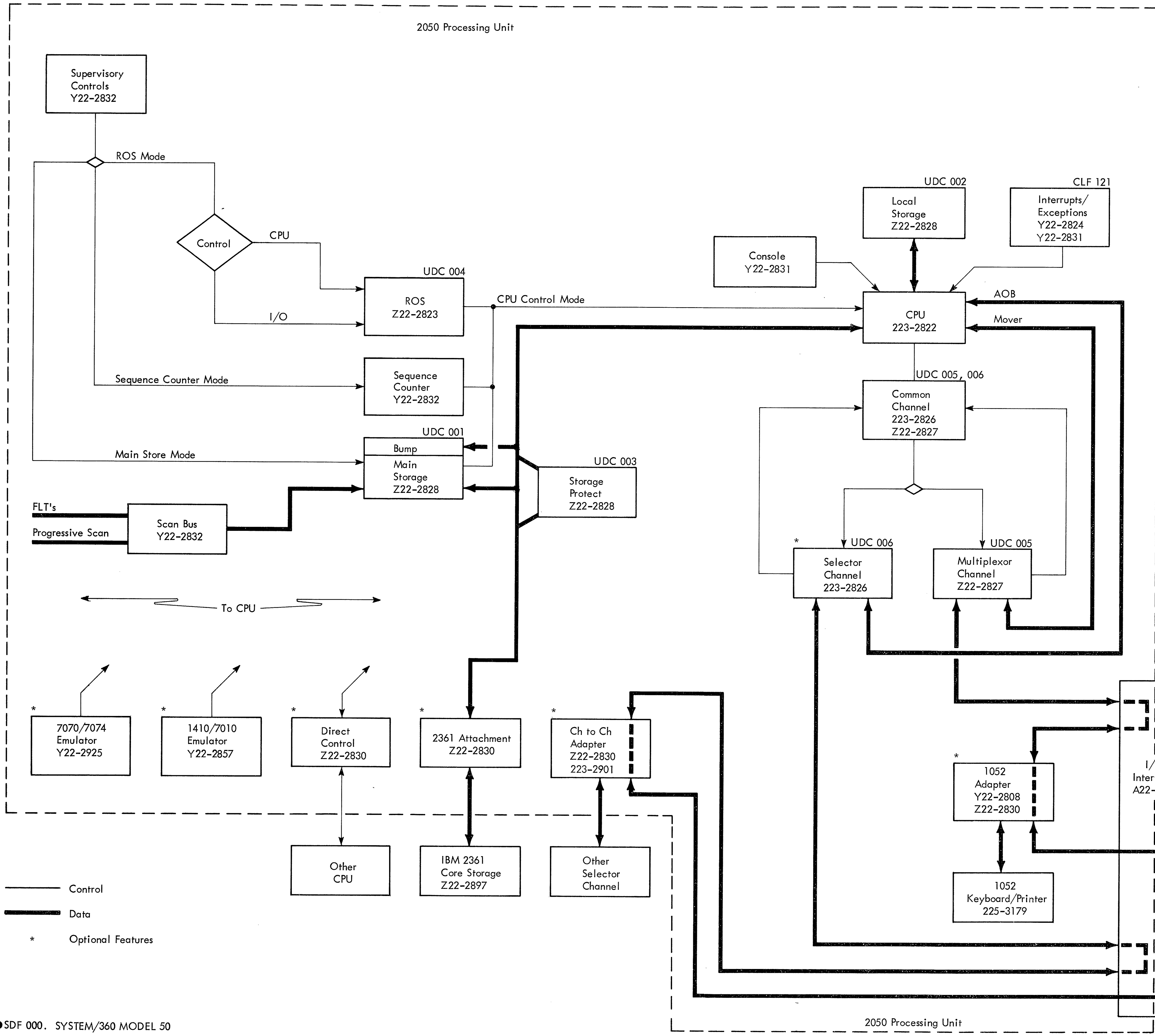
This manual has been prepared by the IBM Systems Development Division, Product Publications, Dept. B96, PO Box 390, Poughkeepsie, N. Y. 12602. A form is provided at the back of this publication for reader's comments. If the form has been removed, comments may be sent to the above address.

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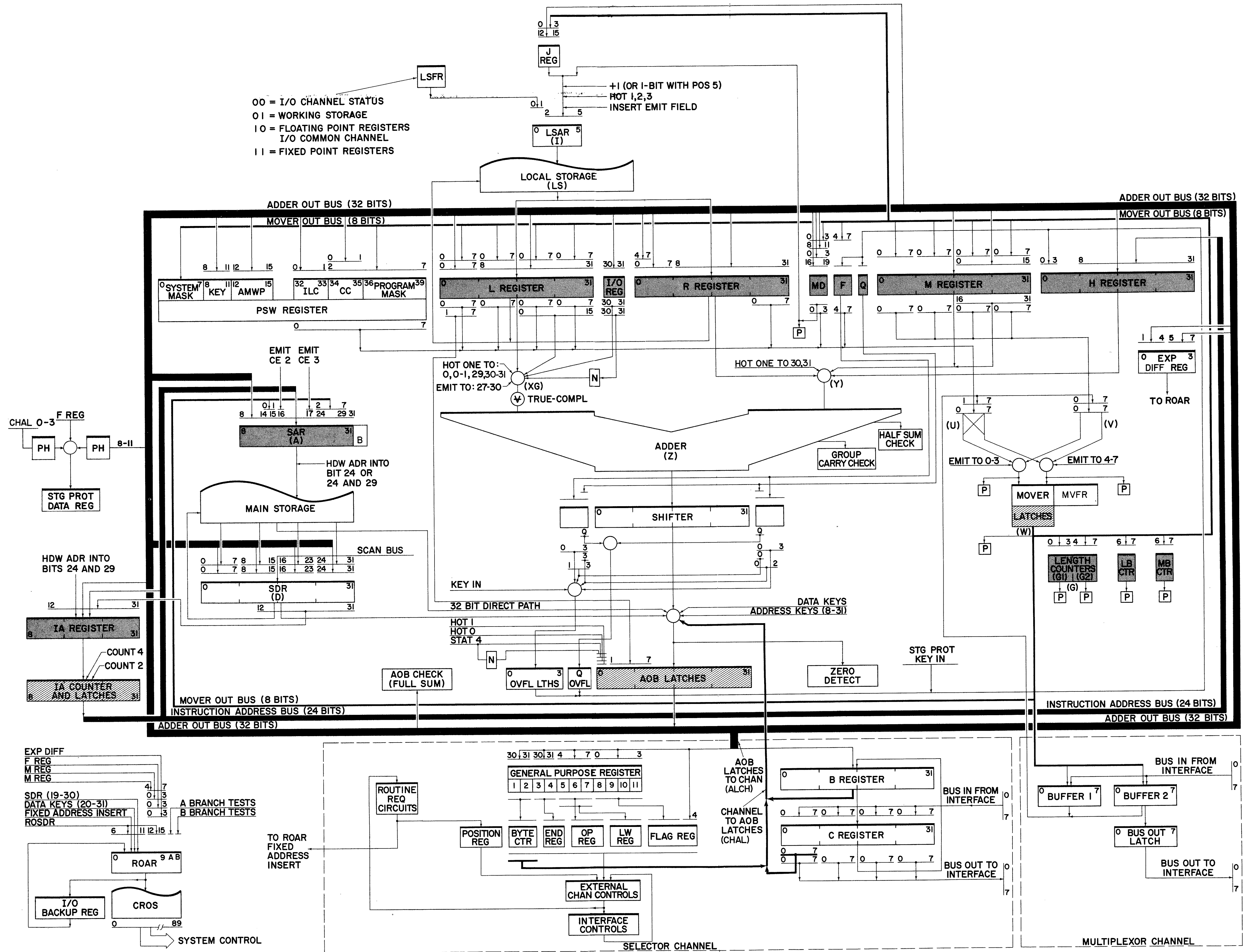
2050 Processing Unit Manuals

Comprehensive Introduction	223-2821
Functional Units	223-2822
CROS	Z22-2823
RR, RX Instructions	Y22-2824
RS, SI, SS Instructions	Z22-2825
Selector Channel	Z22-2826
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Features	Z22-2830
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Maintenance Manual	Y22-2832
Diagram Manual	Z22-2833
Model 50 Handbook	Z22-2855
1410/7010 Compatibility Feature	Y22-2857
7070/7074 Compatibility Feature	Y22-2925
Model 50 Installation Manual	123-9501

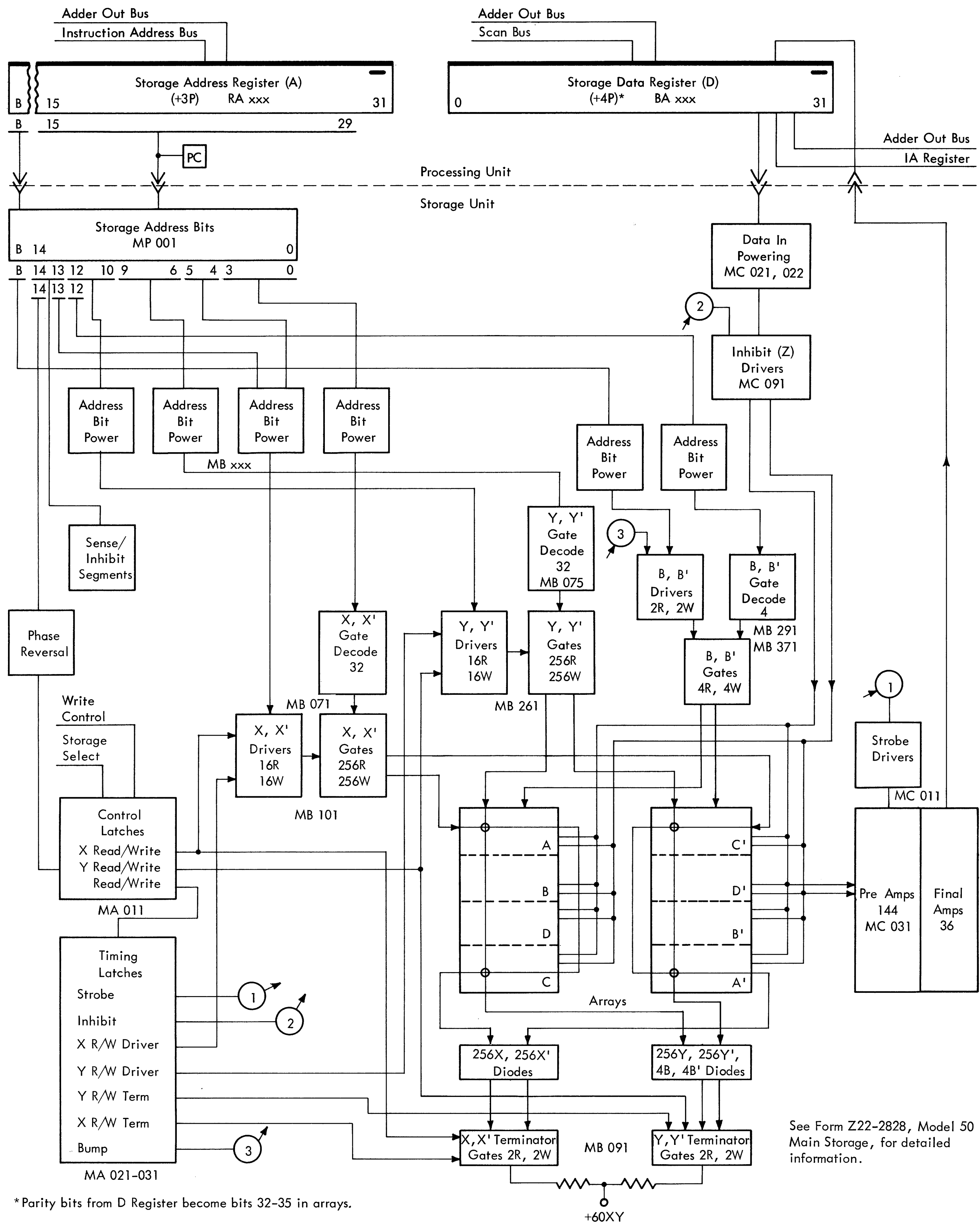
General Reference Manuals

System/360 Installation Manual - Physical Planning	C22-6820
System/360 Principles of Operation	A22-6821
System/360 I/O Interface	A22-6843
Model 50 Functional Characteristics	A22-6898
System/360 Handbook	Z22-2851
SLT Component Circuits	Z22-2798
SLT Power Supplies	Z22-2799
SLT Packaging, Tools and Wiring Change	Z22-2800

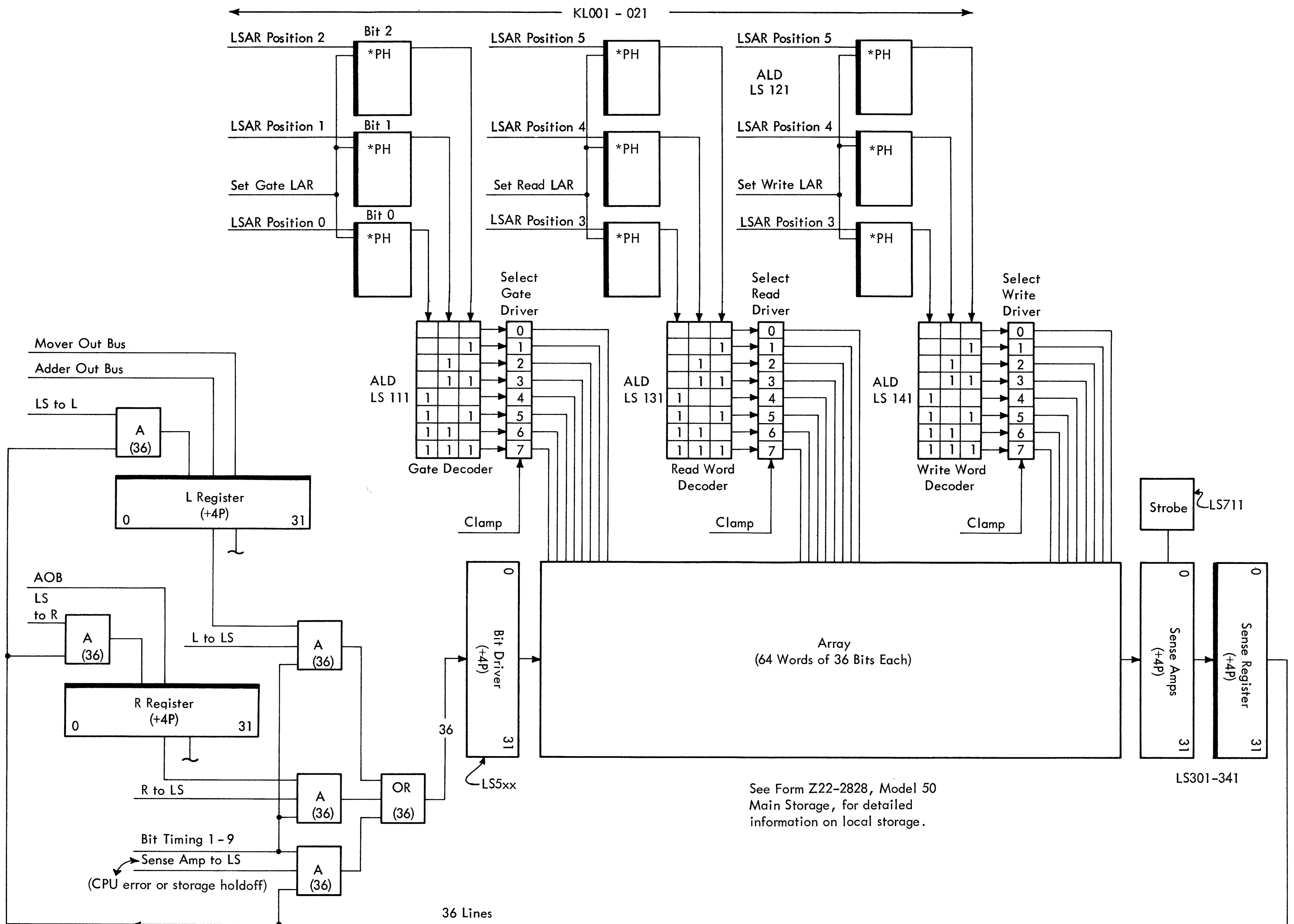
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SDF 001. 2050 PROCESSING UNIT DATA FLOW

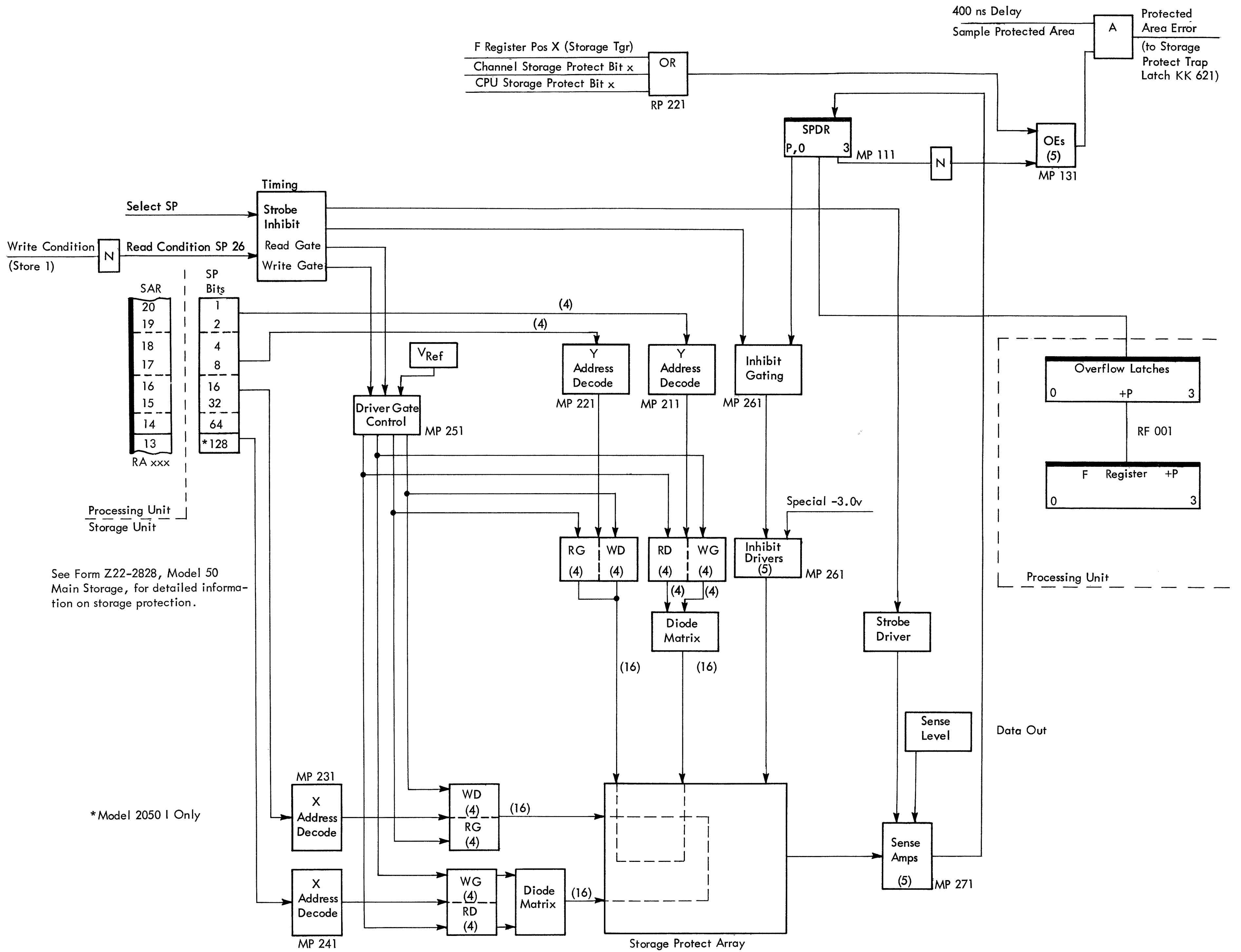


● UDC 001. MAIN STORAGE

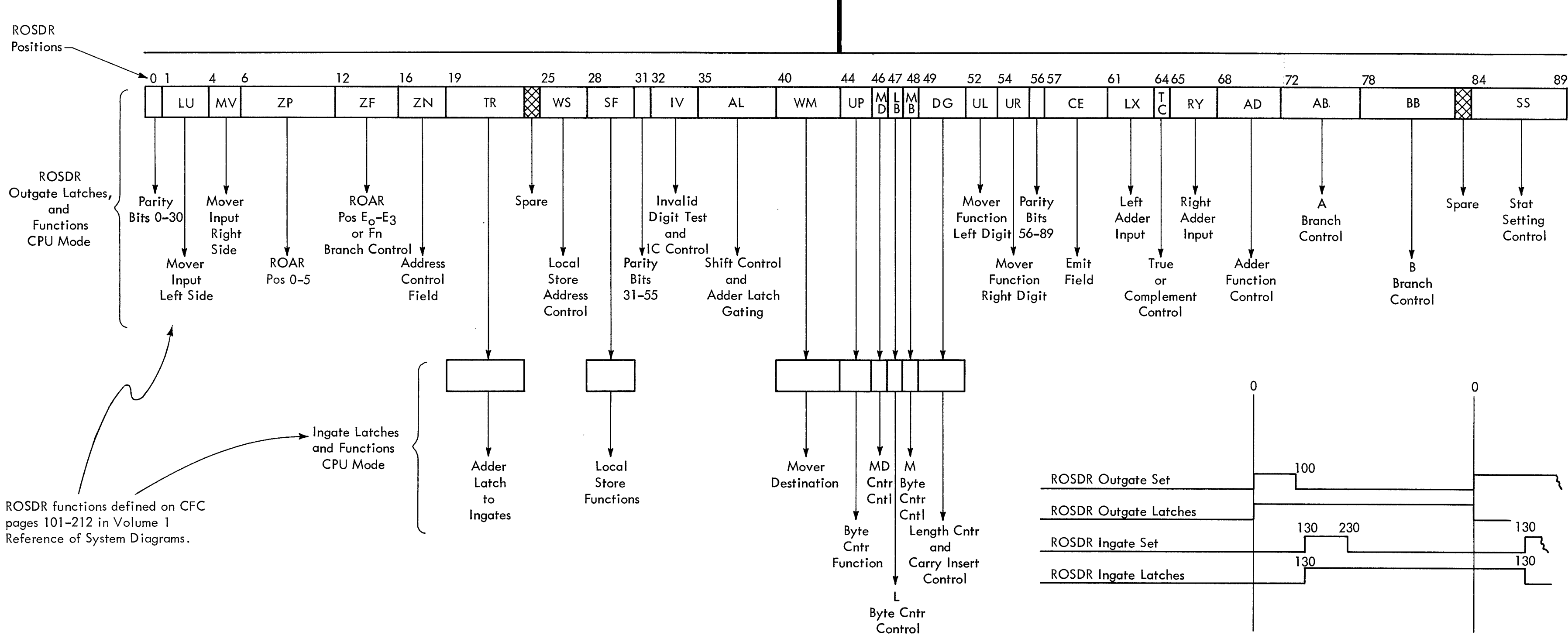
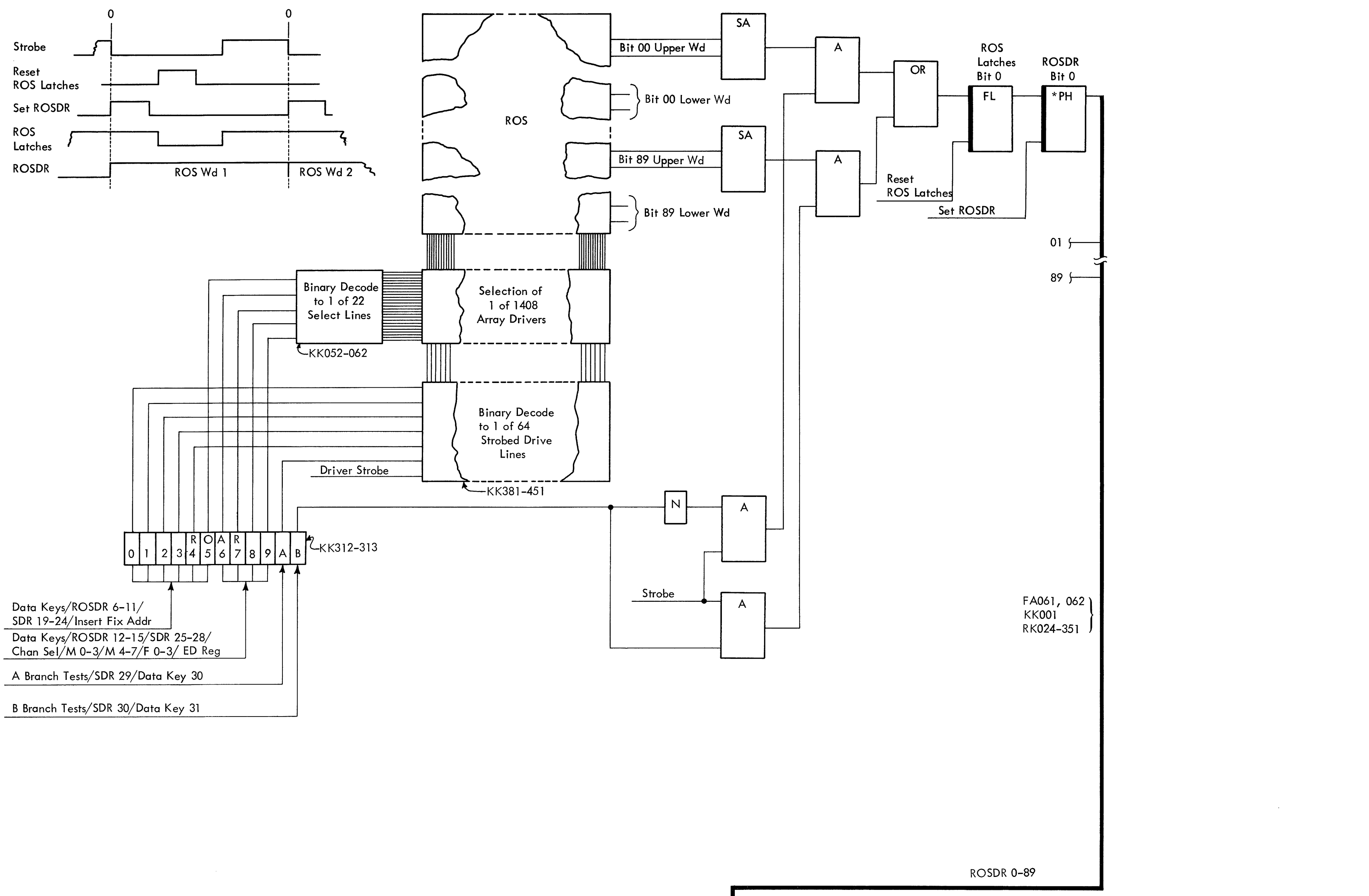


● UDC 002. LOCAL STORAGE





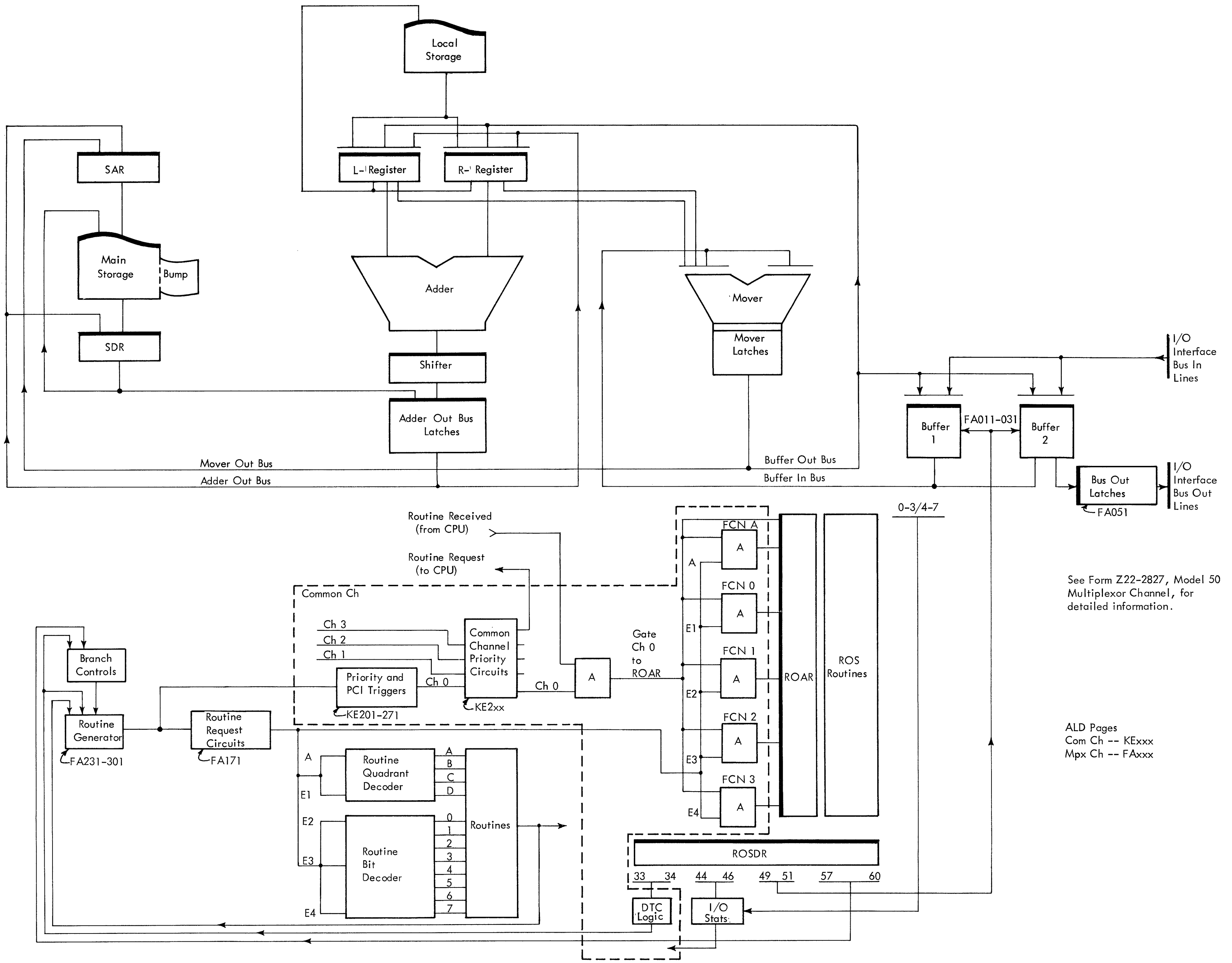
● UDC 003. STORAGE PROTECTION



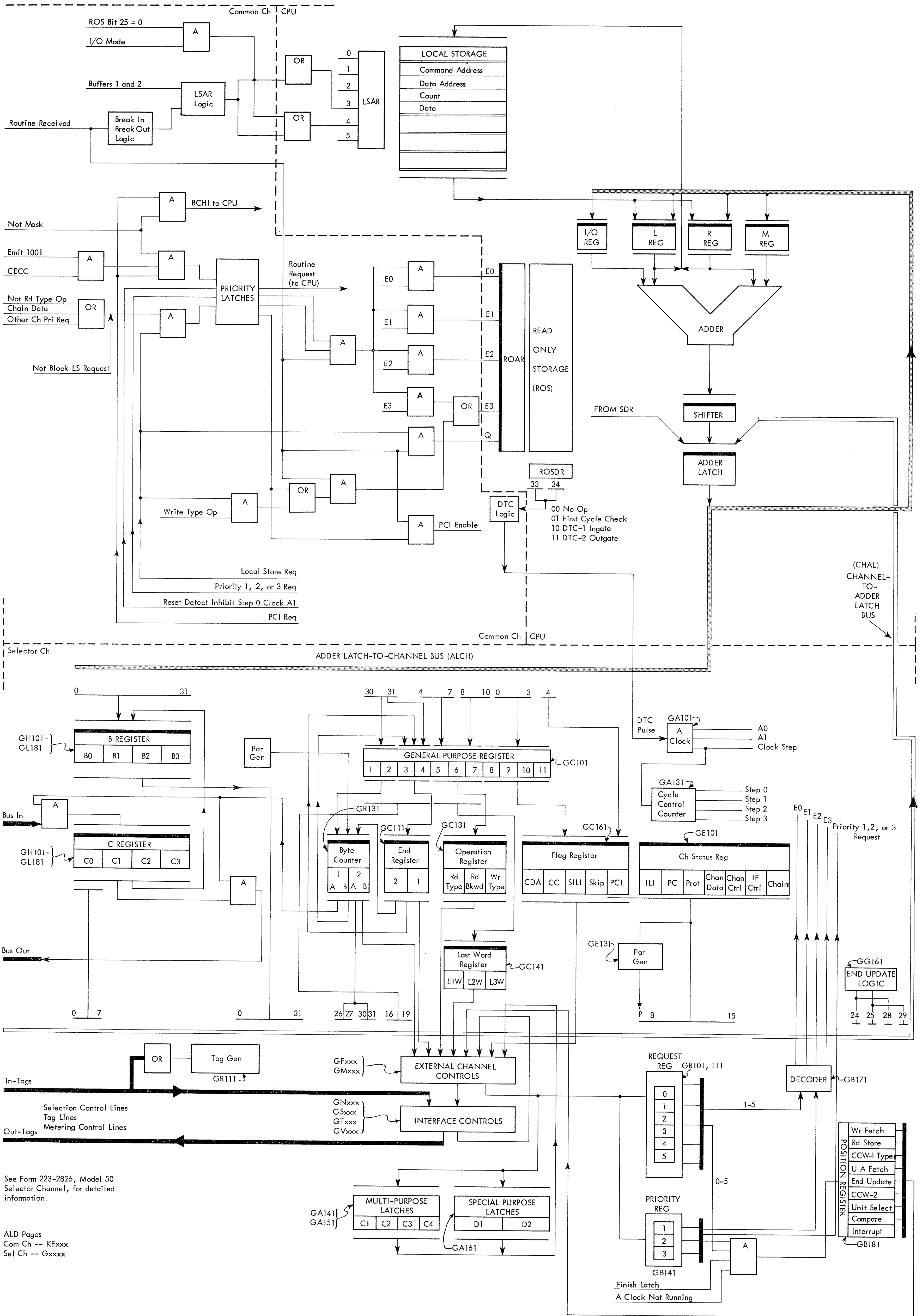
ROSDR functions defined on CFC pages 101-212 in Volume 1 Reference of System Diagrams.

See Form Z22-2823, Model 50 Capacitor Read-Only Storage for detailed information.

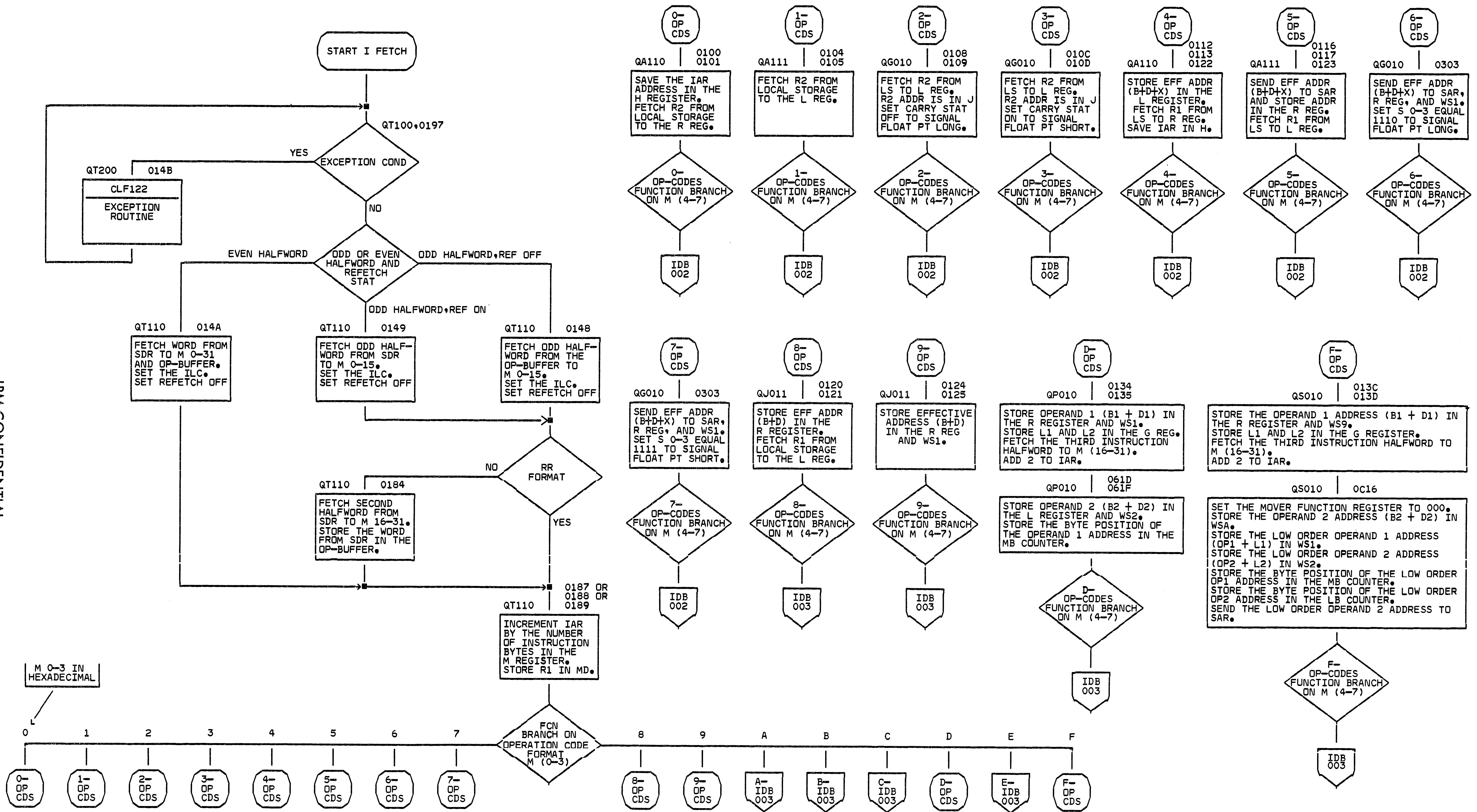
UDC 004. CAPACITOR READ ONLY STORAGE



● UDC 005. MULTIPLEXOR CHANNEL



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OP CODE IN M O-7	***0000	***0001	***0010	***0011	***0100	***0101	***0110	***0111	***1000	***1001	***1010	***1011	***1100	***1101	***1110	***1111	TYPE OF OPERATION
0000****	INVALID OP 0182 QM111 CLF 122	INVALID OP 0186 QM111 CLF 122	INVALID OP 018A QM111 CLF 122	INVALID OP 018E QM111 CLF 122	04 SPM SET PROGRAM MASK 0192 QA400 CLF 104	05 BALR BRANCH AND LINK 0196 QA500 CLF 102	06 BCTR BRANCH ON COUNT 019A QA700 CLF 102	07 BCR BRANCH ON CONDITION 019E QA700 CLF 102	08 SSK SET STORAGE KEY 01A2 QA800 CLF 104	09 ISK INSERT STORAGE KEY 01A6 QA800 CLF 104	0A SVC SUPERVISOR CALL 01AA QA400 CLF 122	INVALID OP 01AE QM111 CLF 122	INVALID OP 01B2 QM111 CLF 122	INVALID OP 01B6 QM111 CLF 122	INVALID OP 01BA QM111 CLF 122	INVALID OP 01BE QM111 CLF 122	BRANCHING AND STATUS SWITCHING
0001****	10 LPR LOAD POSITIVE 0280 QB100 CLF 110	11 LNR LOAD NEGATIVE 0284 QB100 CLF 110	12 LTR LOAD AND TEST 0288 QB100 CLF 110	13 LCR LOAD COMPLEMENT 028C QB100 CLF 110	14 NR AND 0290 QB400 CLF 104	15 CLR COMPARE LOGICAL 0294 QB500 CLF 105	16 OR OR 0298 QB400 CLF 104	17 XR EXCLUSIVE OR 029C QB400 CLF 104	18 LR LOAD 02A0 QB100 CLF 110	19 CR COMPARE 02A4 QB500 CLF 105	1A AR ADD 02A8 QB730 CLF 106	1B SR SUBTRACT 02AC QB730 CLF 106	1C MR MULTIPLY 02B0 QB800 CLF 113	1D DR DIVIDE 02B4 QB900 CLF 114	1E ALR ADD LOGICAL 02B8 QB750 CLF 105	1F SLR SUBTRACT LOGICAL 02BC QB750 CLF 105	FIXED POINT FULLWORD AND LOGICAL
0010****	20 LPDR LOAD POSITIVE 0300 QG100 CLF 108	21 LNDR LOAD NEGATIVE 0304 QG100 CLF 108	22 LTDR LOAD AND TEST 0308 QG100 CLF 108	23 LCDR LOAD COMPLEMENT 030C QG100 CLF 108	24 HDR HALVE 0310 QG200 CLF 107	INVALID OP 0314 QM112 CLF 122	INVALID OP 0318 QM112 CLF 122	INVALID OP 031C QM112 CLF 122	28 LDR LOAD 0320 QG300 CLF 107	29 CDR COMPARE 0324 QG400 CLF 118	2A ADR ADD NORMALIZED 0328 QG400 CLF 118	2B SDR SUBTRACT NORMALIZED 032C QG400 CLF 118	2C MDR MULTIPLY 0330 QG700 CLF 119	2D DDR DIVIDE 0334 QG500 CLF 120	2E AWR ADD UNNORMALIZED 0338 QG400 CLF 118	2F SWR SUBTRACT UNNORMALIZED 033C QG400 CLF 118	FLOATING POINT LONG
0011****	30 LPER LOAD POSITIVE 0300 QG100 CLF 108	31 LNER LOAD NEGATIVE 0304 QG100 CLF 108	32 LTER LOAD AND TEST 0308 QG100 CLF 108	33 LCER LOAD COMPLEMENT 030C QG100 CLF 108	34 HER HALVE 0310 QG200 CLF 107	INVALID OP 0314 QM112 CLF 122	INVALID OP 0318 QM112 CLF 122	INVALID OP 031C QM112 CLF 122	38 LER LOAD 0320 QG300 CLF 107	39 CER COMPARE 0324 QG400 CLF 115	3A AER ADD NORMALIZED 0328 QG400 CLF 115	3B SER SUBTRACT NORMALIZED 032C QG400 CLF 115	3C MER MULTIPLY 0330 QG700 CLF 116	3D DER DIVIDE 0334 QG500 CLF 117	3E AUR ADD UNNORMALIZED 0338 QG400 CLF 115	3F SUR SUBTRACT UNNORMALIZED 033C QG400 CLF 115	FLOATING POINT SHORT
0100****	40 STH STORE HALFWORD 0700 QE555 CLF 109	41 LA LOAD ADDRESS 0704 QE100 CLF 109	42 STC STORE CHARACTER 0708 QE100 CLF 109	43 IC INSERT CHARACTER 070C QE100 CLF 109	44 EX EXECUTE 0710 QE400 CLF 103	45 BAL BRANCH AND LINK 0714 QA500 CLF 102	46 BCT BRANCH ON COUNT 0718 QA700 CLF 102	47 BC BRANCH ON CONDITION 071C QA700 CLF 102	48 LH LOAD HALFWORD 0720 QE580 CLF 106	49 CH COMPARE HALFWORD 0724 QE580 CLF 106	4A AH ADD HALFWORD 0728 QE580 CLF 106	4B SH SUBTRACT HALFWORD 072C QE580 CLF 106	4C MH MULTIPLY HALFWORD 0730 QE580 CLF 113	INVALID OP 0734 QM112 CLF 122	4E CVD CONVERT TO DECIMAL 0738 QE800 CLF 111	4F CVB CONVERT TO BINARY 073C QE900 CLF 112	FIXED POINT HALFWORD AND BRANCHING
0101****	50 ST STORE 0281 QF100 CLF 109	INVALID OP 0285 QM112 CLF 122	INVALID OP 0289 QM112 CLF 122	INVALID OP 028D QM112 CLF 122	54 N AND 0291 QB400 CLF 104	55 CL COMPARE LOGICAL 0295 QB500 CLF 105	56 O OR 0299 QB400 CLF 104	57 X EXCLUSIVE OR 029D QB400 CLF 104	58 L LOAD 02A1 QF100 CLF 109	59 C COMPARE 02A5 QB500 CLF 105	5A A ADD 02A9 QB730 CLF 106	5B S SUBTRACT 02AD QB730 CLF 106	5C M MULTIPLY 02B1 QB800 CLF 113	5D D DIVIDE 02B5 QB900 CLF 114	5E AL ADD LOGICAL 02B9 QB750 CLF 105	5F SL SUBTRACT LOGICAL 02BD QB750 CLF 105	FIXED POINT FULLWORD AND LOGICAL
0110****	60 STD STORE 0302 QG300 CLF 107	INVALID OP 0306 QM111 CLF 122	INVALID OP 030A QM111 CLF 122	INVALID OP 030E QM111 CLF 122	INVALID OP 0312 QM111 CLF 122	INVALID OP 0316 QM111 CLF 122	INVALID OP 031A QM111 CLF 122	INVALID OP 031E QM111 CLF 122	68 LD LOAD 0322 QG300 CLF 107	69 CD COMPARE 0326 QG400 CLF 118	6A AD ADD NORMALIZED 032A QG400 CLF 118	6B SD SUBTRACT NORMALIZED 032E QG400 CLF 118	6C MD MULTIPLY 0332 QG700 CLF 119	6D DD DIVIDE 0336 QG500 CLF 120	6E AW ADD UNNORMALIZED 033A QG400 CLF 118	6F SW SUBTRACT UNNORMALIZED 033E QG400 CLF 118	FLOATING POINT LONG
0111****	70 STE STORE 0302 QG300 CLF 107	INVALID OP 0306 QM111 CLF 122	INVALID OP 030A QM111 CLF 122	INVALID OP 030E QM111 CLF 122	INVALID OP 0312 QM111 CLF 122	INVALID OP 0316 QM111 CLF 122	INVALID OP 031A QM111 CLF 122	INVALID OP 031E QM111 CLF 122	78 LE LOAD 0322 QG300 CLF 107	79 CE COMPARE 0326 QG400 CLF 115	7A AE ADD NORMALIZED 032A QG400 CLF 115	7B SE SUBTRACT NORMALIZED 032E QG400 CLF 115	7C ME MULTIPLY 0332 QG700 CLF 116	7D DE DIVIDE 0336 QG500 CLF 117	7E AU ADD UNNORMALIZED 033A QG400 CLF 115	7F SU SUBTRACT UNNORMALIZED 033E QG400 CLF 115	FLOATING POINT SHORT

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RR  
FORMAT

RX  
FORMAT

RR/RX OPERATION CODES  
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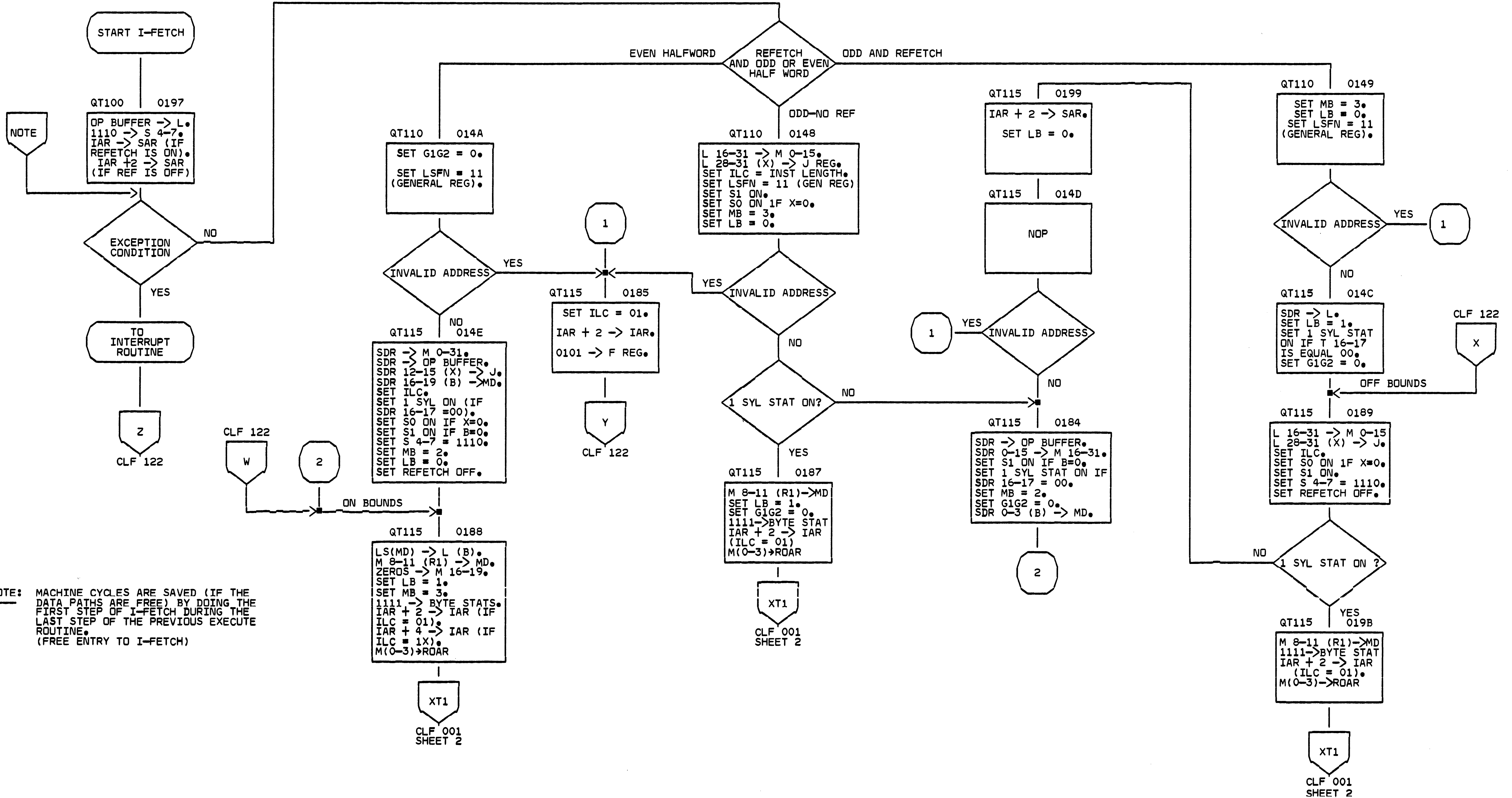
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	***0000	***0001	***0010	***0011	***0100	***0101	***0110	***0111	***1000	***1001	***1010	***1011	***1100	***1101	***1110	***1111			
RS/SI FORMAT	1000****	80 SSM INVALID OP SET SYSTEM MASK 0702 QJ200 CLF 209	INVALID OP 0706 QM111 CLF 122	82 LPSW LOAD PSW 070A QJ200 CLF 210	83 DIAG DIAGNOSE 070E QY110 CLF 213	84 WRD WRITE DIRECT 0712 QJ400 CLF 211	85 RDD READ DIRECT 0716 QJ400 CLF 212	86 BXH BRANCH ON INDEX HIGH 071A QJ600 CLF 214	87 BXLE BRANCH ON INDEX LOW OR EQUAL 071E QJ600 CLF 214	88 SRL SHIFT RIGHT SINGLE - LOGICAL 0722 QJ080 CLF 201	89 SLL SHIFT LEFT SINGLE - LOGICAL 0726 QJ090 CLF 202	8A SRA SHIFT RIGHT SINGLE 072A QJ100 CLF 203	8B SLA SHIFT LEFT SINGLE 072E QJ110 CLF 204	8C SRDL SHIFT RIGHT DOUBLE - LOGICAL 0732 QJ120 CLF 205	8D SLDL SHIFT LEFT DOUBLE - LOGICAL 0736 QJ130 CLF 206	8E SRDA SHIFT RIGHT DOUBLE 073A QJ140 CLF 207	8F SLDA SHIFT LEFT DOUBLE 073E QJ150 CLF 208	BRANCHING, STATUS SWITCHING, AND SHIFTING	
	1001****	90 STM STORE MULTIPLE 0902 QK666 CLF 224	91 TM TEST UNDER MASK 0906 QK555 CLF 222	92 MVI MOVE 090A QK222 CLF 220	93 TS TEST AND SET 090E QK300 CLF 220	94 NI AND 0912 QK222 CLF 220	95 CLI COMPARE LOGICAL 0916 QK555 CLF 223	96 OI OR 091A QK222 CLF 220	97 XI EXCLUSIVE OR 091E QK222 CLF 220	98 LM LOAD MULTIPLE 0922 QK666 CLF 224	INVALID OP 0926 QM111 CLF 122	INVALID OP 092A QM111 CLF 122	INVALID OP 092E QM111 CLF 122	9C SID START I O 0932 QK700 CLF 225	9D TIO TEST I O 0936 QK700 CLF 225	9E HIO HALT I O 093A QK700 CLF 225	9F TCH TEST CHANNEL 093E QK700 CLF 225	FIXED POINT LOGICAL AND I/O	
	1010****	INVALID FORMAT 0128 OR 0129 QN111 CLF 122	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	▶
	1011****	INVALID FORMAT 012C OR 012D QN111 CLF 122	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....
SS FORMAT	1100****	INVALID FORMAT 0130 OR 0131 QN111 CLF 122	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	▶
	1101****	INVALID OP 0600 QM112 CLF 122	D1 MVN MOVE NUMERIC 0604 QP800 CLF 232	D2 MVC MOVE 0608 QP800 CLF 232	D3 MVZ MOVE ZONE 060C QP800 CLF 232	D4 NC AND 0610 QP800 CLF 232	D5 CLC COMPARE LOGICAL 0614 QP100 CLF 230	D6 DC OR 0618 QP800 CLF 232	D7 XC EXCLUSIVE OR 061C QP800 CLF 232	INVALID OP 0620 QM112 CLF 122	INVALID OP 0624 QM112 CLF 122	INVALID OP 0628 QM112 CLF 122	INVALID OP 062C QM112 CLF 122	DC TR TRANSLATE 0630 QP900 CLF 233	DD TRT TRANSLATE AND TEST 0634 QP900 CLF 233	DE ED EDIT 0638 QP200 CLF 231	DF EDMK EDIT AND MARK 063C QP200 CLF 231	LOGICAL AND VFL	
	1110****	INVALID FORMAT 0138 OR 0139 QN111 CLF 122	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	▶
1111****	INVALID OP 0C00 QM111 CLF 122	F1 MVD MOVE WITH OFFSET 0C04 QS502 CLF 244	F2 PACK PACK 0C08 QS500 CLF 243	F3 UNPK UNPACK 0C0C QS600 CLF 245	INVALID OP 0C10 QM111 CLF 122	INVALID OP 0C14 QM111 CLF 122	INVALID OP 0C18 QM111 CLF 122	INVALID OP 0C1C QM111 CLF 122	F8 ZAP ZERO AND ADD 0C20 QS705 CLF 246	F9 CP COMPARE DECIMAL 0C24 QS200 CLF 241	FA AP ADD DECIMAL 0C28 QS110 CLF 240	FB SP SUBTRACT DECIMAL 0C2C QS110 CLF 240	FC MP MULTIPLY DECIMAL 0C30 QS400 CLF 242	FD DP DIVIDE DECIMAL 0C34 QS400 CLF 242	INVALID OP 0C38 QM111 CLF 122	INVALID OP 0C3C QM111 CLF 122	DECIMAL		

RS/SI/SS OPERATION CODES  
 DATE 3 JUN 66 MACH. 2050  
 FRAME  
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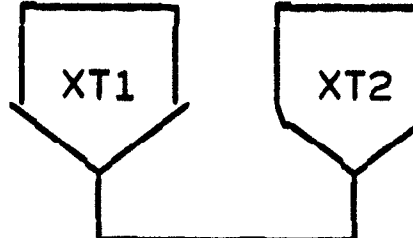


NOTE: MACHINE CYCLES ARE SAVED (IF THE DATA PATHS ARE FREE) BY DOING THE FIRST STEP OF I-FETCH DURING THE LAST STEP OF THE PREVIOUS EXECUTE ROUTINE. (FREE ENTRY TO I-FETCH)

1071 C



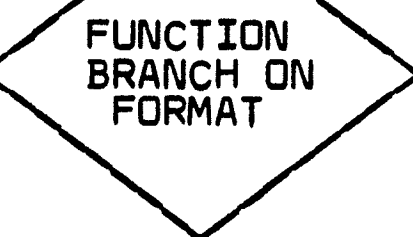
SHEET 1 CLF 103



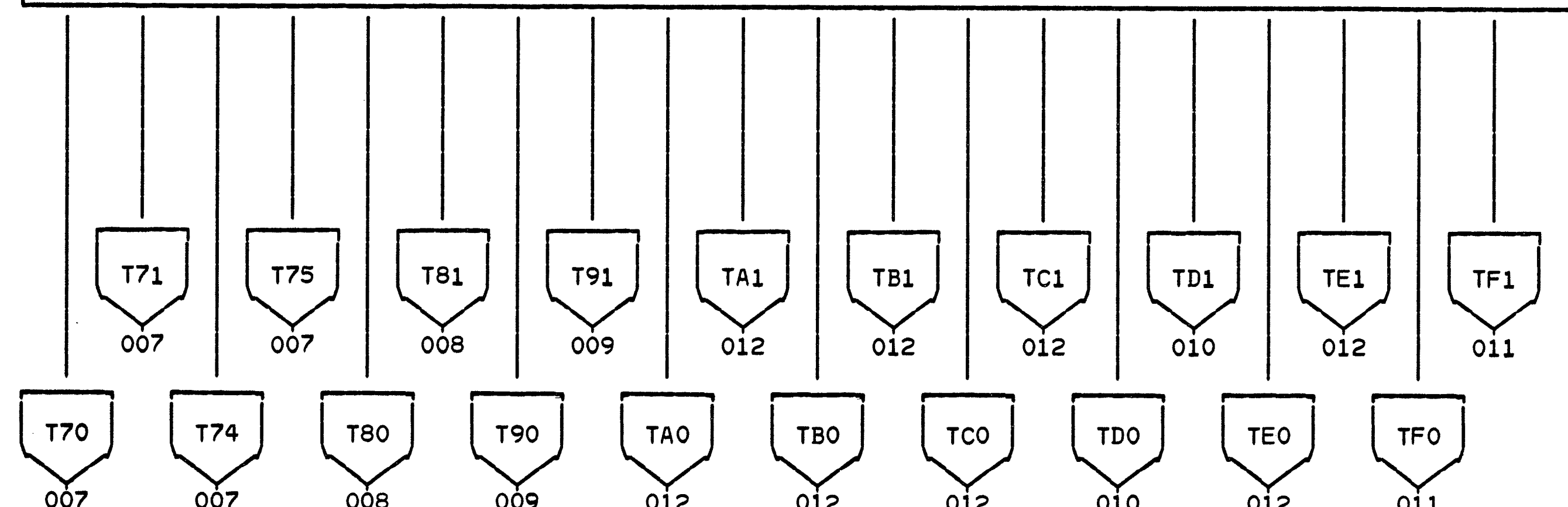
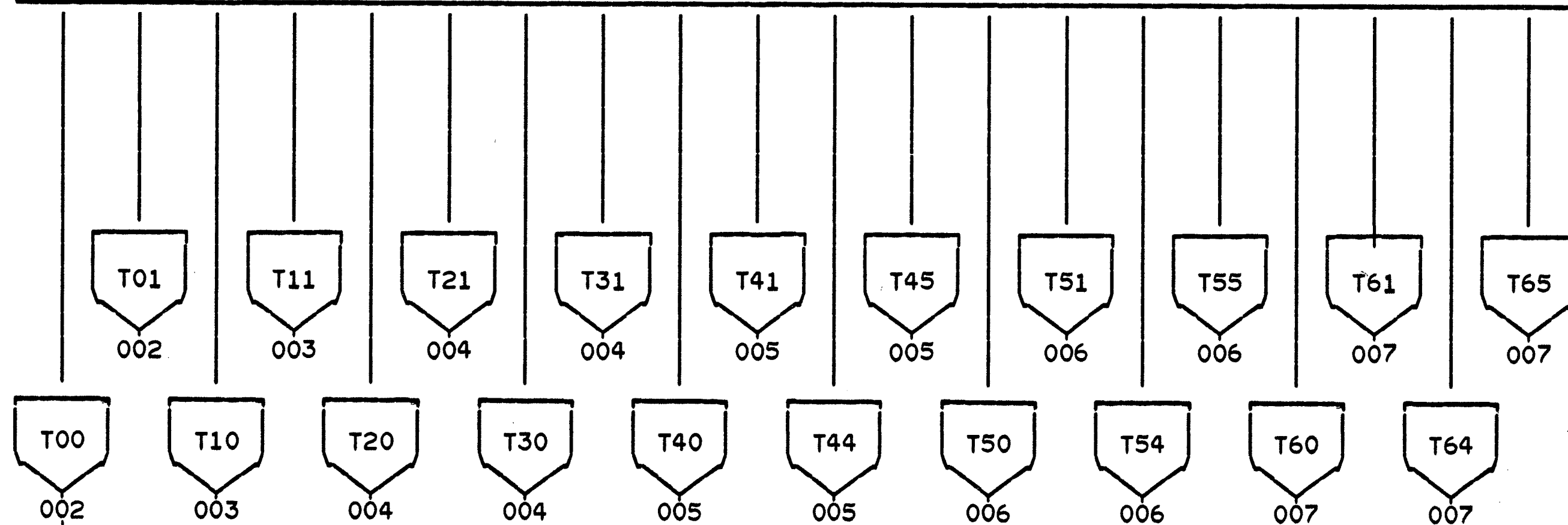
FUNCTION BR  
ON M 0-3.  
A BR ON SO(X=0)  
IF RX FORMAT.  
B BR ON S1  
(B=0).

M 0-3 IN HEX	B FIELD ADDRESS	X FIELD ADDRESS	BRANCH ADDRESS	INSTRUCTION FORMAT
1	0	NOT 0	---	0100 RR BRANCHING AND STATUS SWITCHING
2	0	B = 0	---	0101 RR BRANCHING AND STATUS SWITCHING
3	1	NOT 0	---	0104 RR FIXED POINT FULLWORD AND LOGICAL
4	1	B = 0	---	0105 RR FIXED POINT FULLWORD AND LOGICAL
5	2	NOT 0	---	0108 RR FLOATING POINT LONG
6	2	B = 0	---	0109 RR FLOATING POINT LONG
7	3	NOT 0	---	010C RR FLOATING POINT SHORT
8	3	B = 0	---	010D RR FLOATING POINT SHORT
9	4	NOT 0	NOT 0	0110 RX FIXED POINT HALFWORD AND BRANCHING
10	4	B = 0	NOT 0	0111 RX FIXED POINT HALFWORD AND BRANCHING
11	4	NOT 0	X = 0	0112 RX FIXED POINT HALFWORD AND BRANCHING
12	4	B = 0	X = 0	0113 RX FIXED POINT HALFWORD AND BRANCHING
13	5	NOT 0	NOT 0	0114 RX FIXED POINT FULLWORD AND LOGICAL
14	5	B = 0	NOT 0	0115 RX FIXED POINT FULLWORD AND LOGICAL
15	5	NOT 0	X = 0	0116 RX FIXED POINT FULLWORD AND LOGICAL
16	5	B = 0	X = 0	0117 RX FIXED POINT FULLWORD AND LOGICAL
17	6	NOT 0	NOT 0	0118 RX FLOATING POINT LONG
18	6	B = 0	NOT 0	0119 RX FLOATING POINT LONG
19	6	NOT 0	X = 0	011A RX FLOATING POINT LONG
20	6	B = 0	X = 0	011B RX FLOATING POINT LONG

M 0-3 IN HEX	B FIELD ADDRESS	X FIELD ADDRESS	BRANCH ADDRESS	INSTRUCTION FORMAT
21	7	NOT 0	NOT 0	011C RX FLOATING POINT SHORT
22	7	B = 0	NOT 0	011D RX FLOATING POINT SHORT
23	7	NOT 0	X = 0	011E RX FLOATING POINT SHORT
24	7	B = 0	X = 0	011F RX FLOATING POINT SHORT
25	8	NOT 0	---	0120 RS SI BRANCHING, STATUS SWITCHING, AND SHIFTING
26	8	B = 0	---	0121 RS SI BRANCHING, STATUS SWITCHING, AND SHIFTING
27	9	NOT 0	---	0124 RS SI FIXED POINT LOGICAL AND I O
28	9	B = 0	---	0125 RS SI FIXED POINT LOGICAL AND I O
29	A	NOT 0	---	0128 INVALID FORMAT
30	A	B = 0	---	0129 INVALID FORMAT
31	B	NOT 0	---	012C INVALID FORMAT
32	B	B = 0	---	012D INVALID FORMAT
33	C	NOT 0	---	0130 INVALID FORMAT
34	C	B = 0	---	0131 INVALID FORMAT
35	D	NOT 0	---	0134 SS LOGICAL
36	D	B = 0	---	0135 SS LOGICAL
37	E	NOT 0	---	0138 INVALID FORMAT
38	E	B = 0	---	0139 INVALID FORMAT
39	F	NOT 0	---	013C SS DECIMAL
40	F	B = 0	---	013D SS DECIMAL



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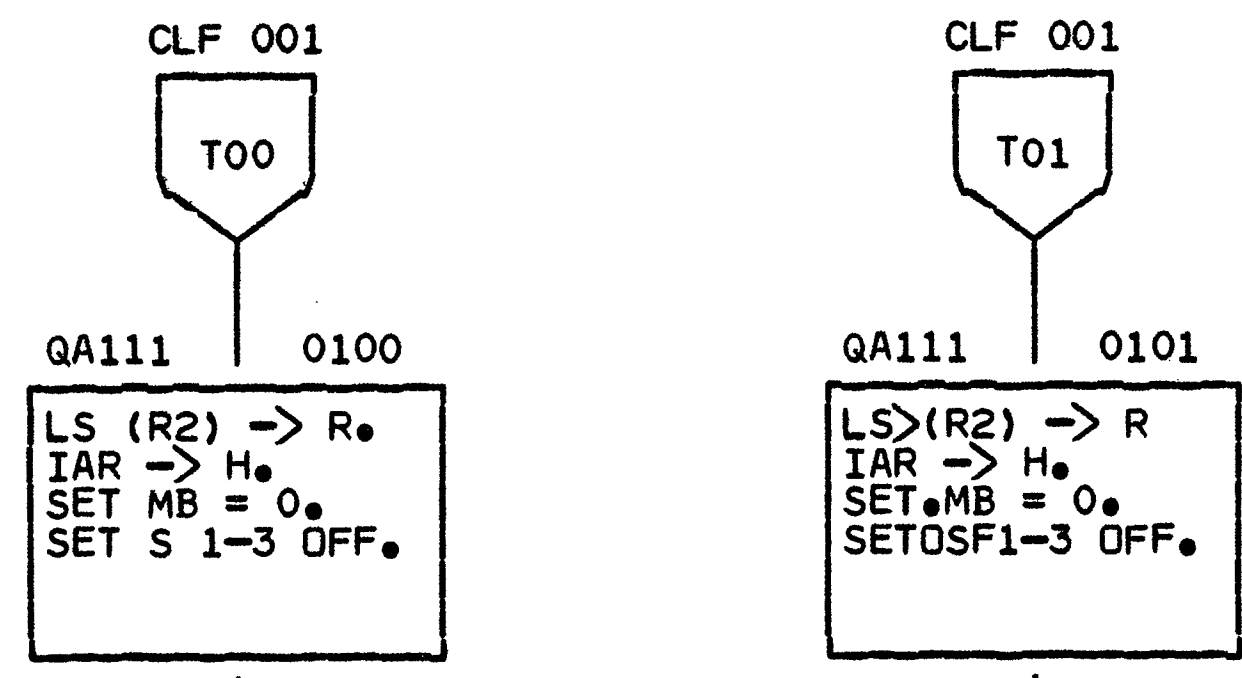
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FIRST LEVEL I-FETCH  
DATE 3 JUN 66 MACH. 2050  
FRAME  
P.#  
IBM CORP. SDD PAGE

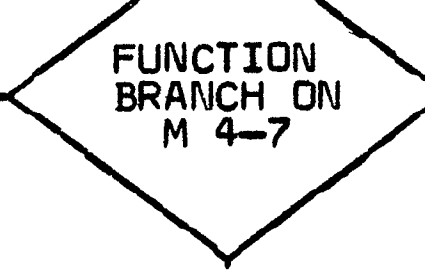
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M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
0	00	INVALID OPERATION CODE
1	01	INVALID OPERATION CODE
2	02	INVALID OPERATION CODE
3	03	INVALID OPERATION CODE
4	04	SET PROGRAM MASK
5	05	BRANCH AND LINK
6	06	BRANCH ON COUNT
7	07	BRANCH ON CONDITION

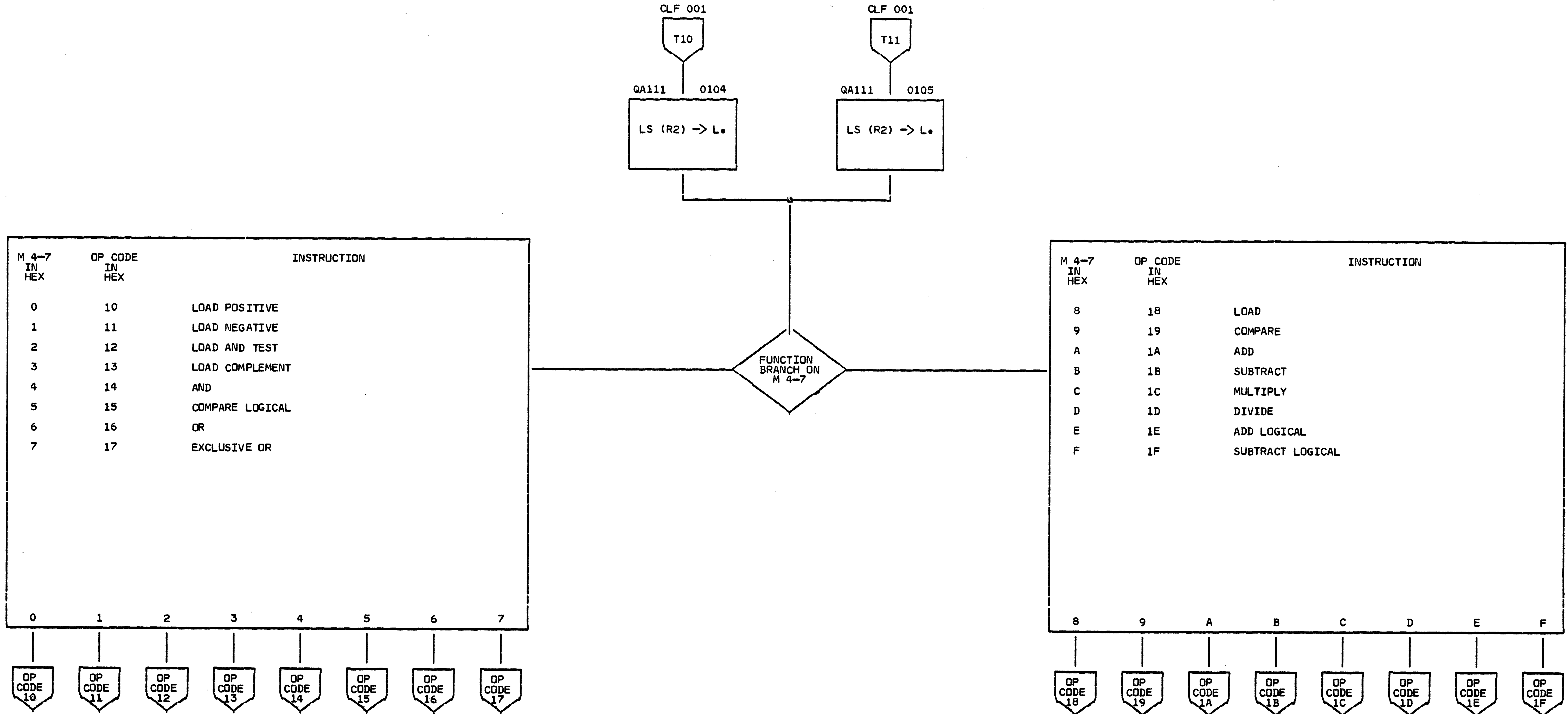
M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
8	08	SET KEY
9	09	INSERT KEY
A	0A	SUPERVISOR CALL
B	0B	INVALID OPERATION CODE
C	0C	INVALID OPERATION CODE
D	0D	INVALID OPERATION CODE
E	0E	INVALID OPERATION CODE
F	0F	INVALID OPERATION CODE



SEE IDB 002 FOR LOCATION OF ROUTINES

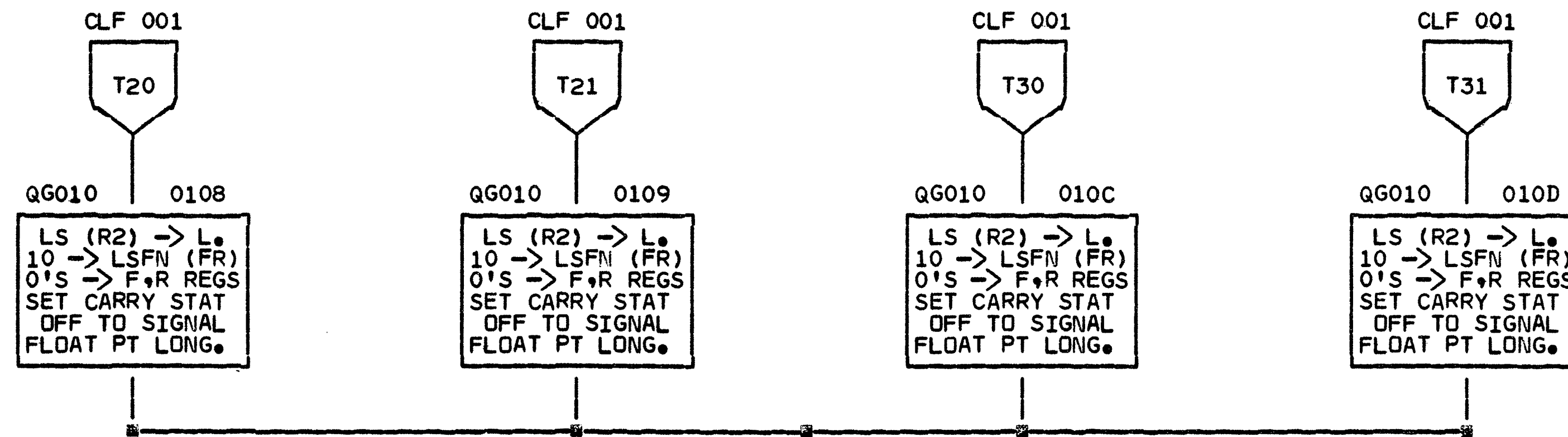
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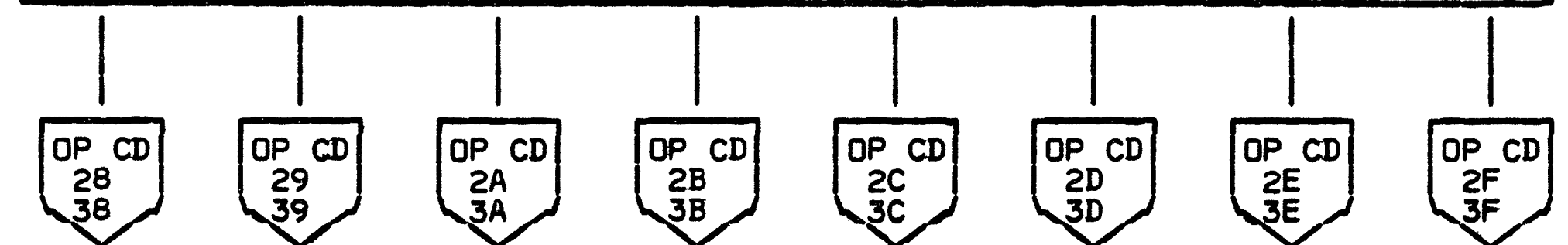
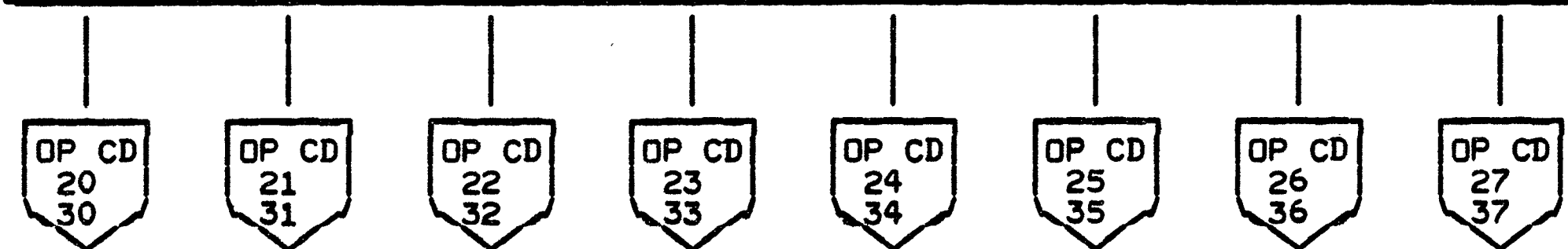
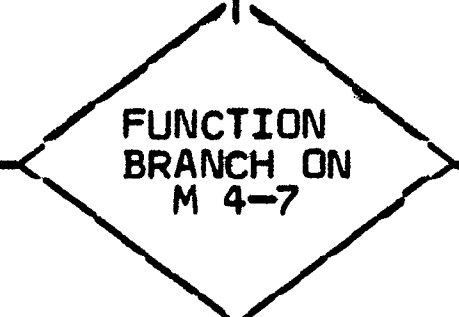
SEE IDB 002 FOR LOCATION OF ROUTINES

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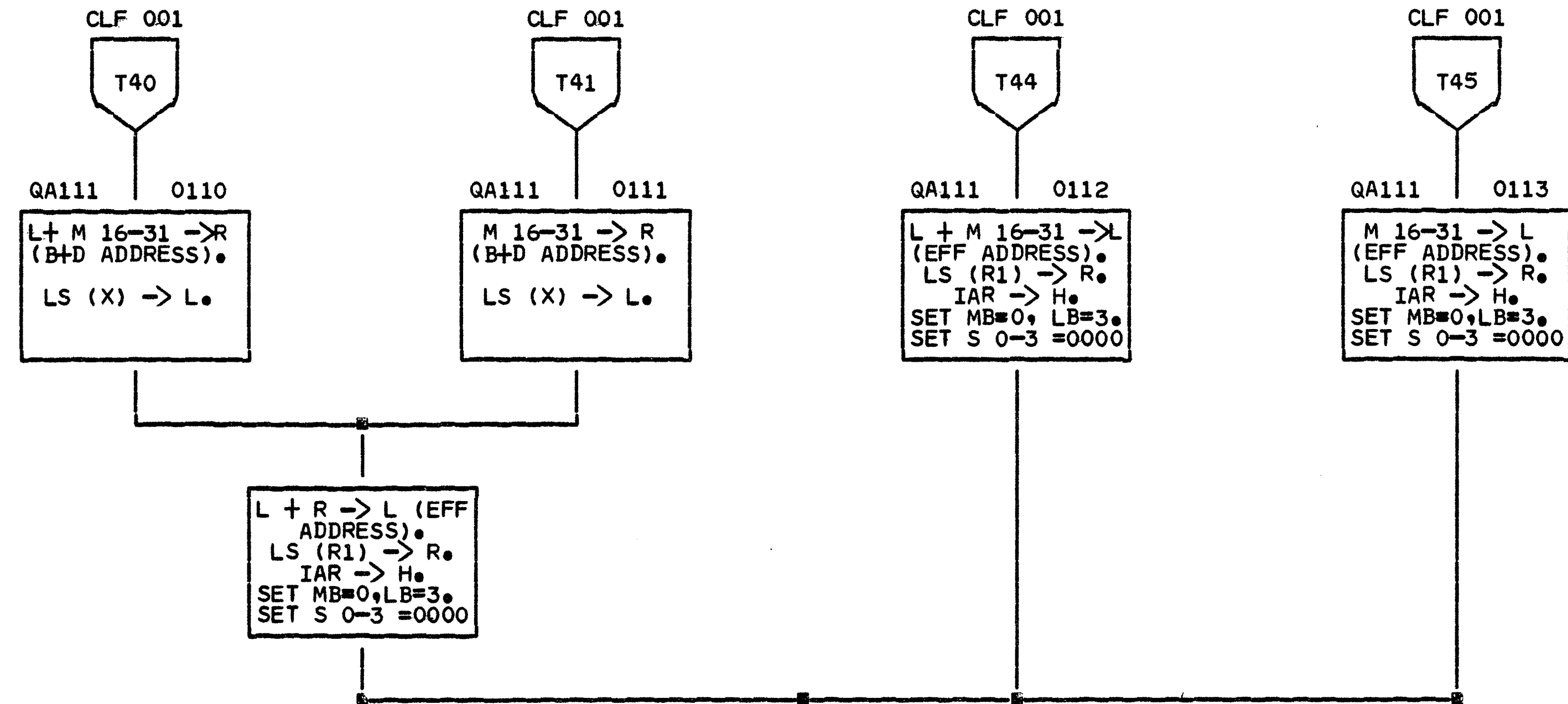


M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
0	20 30	LOAD POSITIVE - FLOATING POINT LONG LOAD POSITIVE - FLOATING POINT SHORT
1	21 31	LOAD NEGATIVE - FLOATING POINT LONG LOAD NEGATIVE - FLOATING POINT SHORT
2	22 32	LOAD AND TEST - FLOATING POINT LONG LOAD AND TEST - FLOATING POINT SHORT
3	23 33	LOAD COMPLEMENT - FLOATING POINT LONG LOAD COMPLEMENT - FLOATING POINT SHORT
4	24 34	HALVE - FLOATING POINT LONG HALVE - FLOATING POINT SHORT
5	25 35	INVALID INVALID
6	26 36	INVALID INVALID
7	27 37	INVALID INVALID

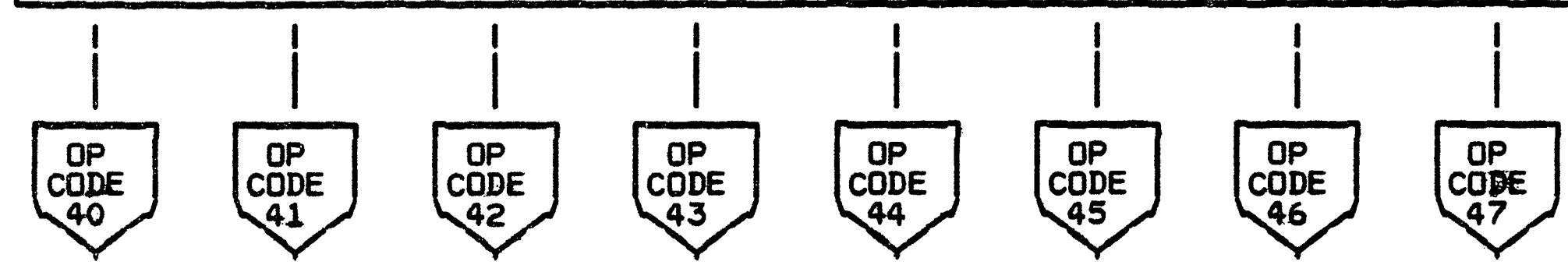
M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
8	28 38	LOAD - FLOATING POINT LONG LOAD - FLOATING POINT SHORT
9	29 39	COMPARE - FLOATING POINT LONG COMPARE - FLOATING POINT SHORT
A	2A 3A	ADD NORMALIZED - FLOATING POINT LONG ADD NORMALIZED - FLOATING POINT SHORT
B	2B 3B	SUBTRACT NORMALIZED - FLOATING POINT LONG SUBTRACT NORMALIZED - FLOATING POINT SHORT
C	2C 3C	MULTIPLY - FLOATING POINT LONG MULTIPLY - FLOATING POINT SHORT
D	2D 3D	DIVIDE - FLOATING POINT LONG
E	2E 3E	ADD UNNORMALIZED - FLOATING POINT LONG ADD UNNORMALIZED - FLOATING POINT SHORT
F	2F 3F	SUBTRACT UNNORMALIZED - FLOATING POINT LONG SUBTRACT UNNORMALIZED - FLOATING POINT SHORT DIVIDE - FLOATING POINT SHORT



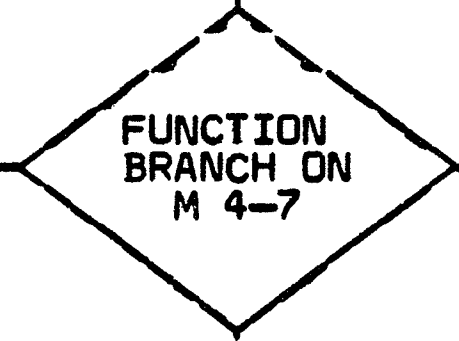
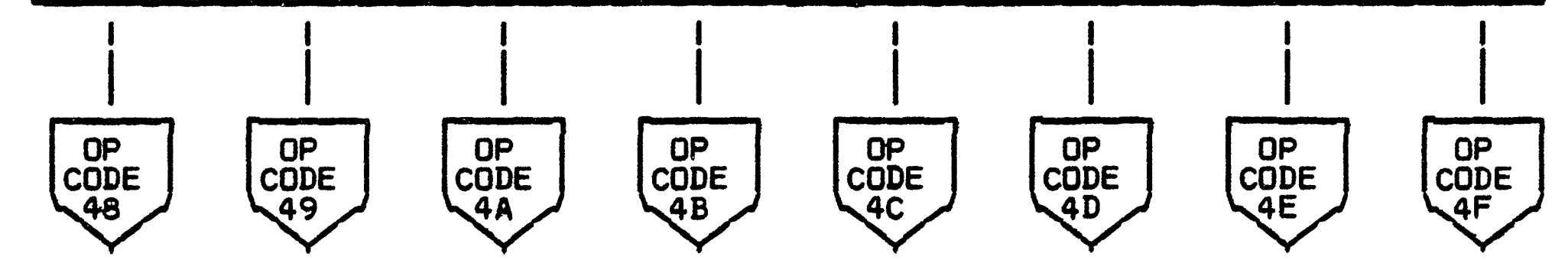
SEE IDB 002 FOR LOCATION OF ROUTINES



M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
0	40	STORE
1	41	LOAD ADDRESS
2	42	STORE CHARACTER
3	43	INSERT CHARACTER
4	44	EXECUTE
5	45	BRANCH AND LINK
6	46	BRANCH ON COUNT
7	47	BRANCT ON CONDITION



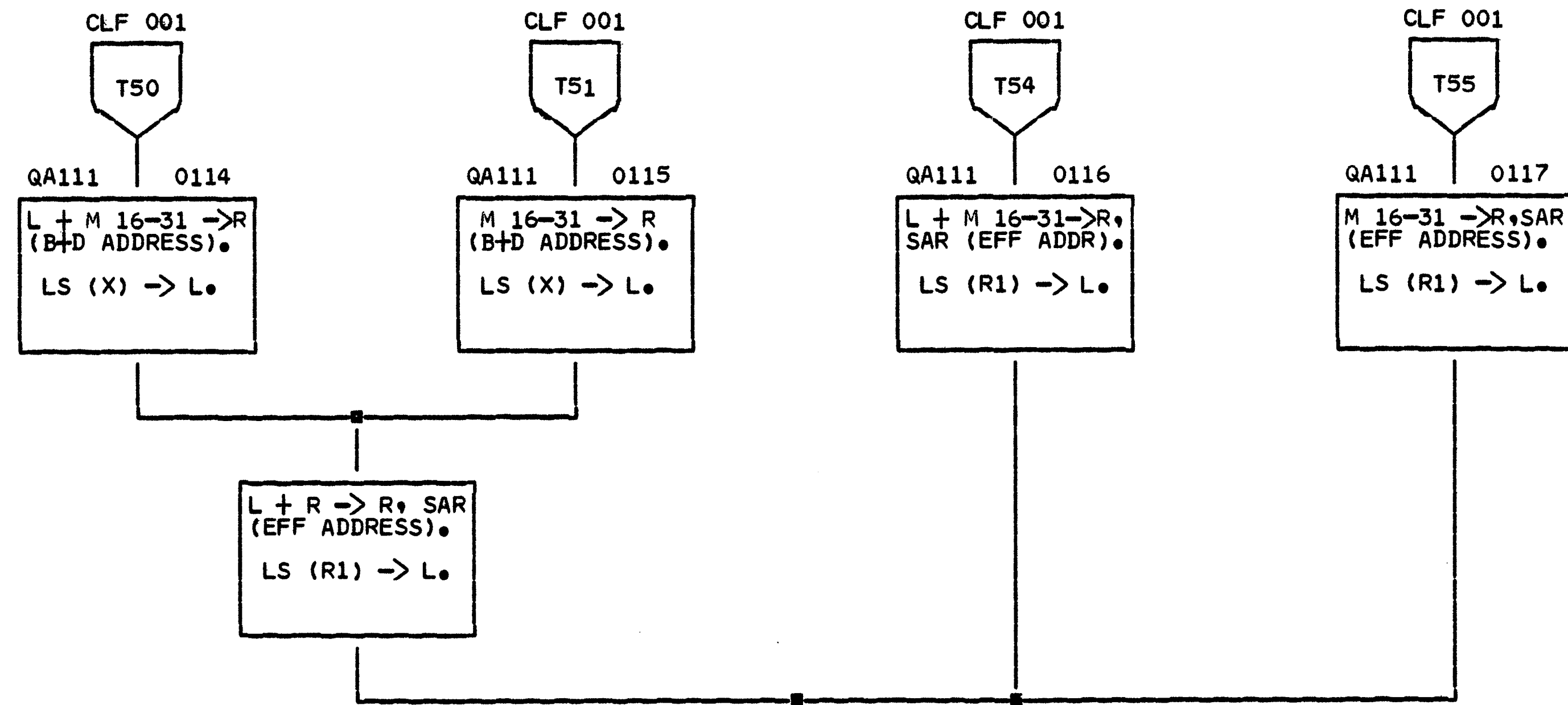
M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
8	48	LOAD
9	49	COMPARE
A	4A	ADD
B	4B	SUBTRACT
C	4C	MULTIPLY
D	4D	INVALID OP CODE
E	4E	CONVERT TO DECIMAL
F	4F	CONVERT TO BINARY



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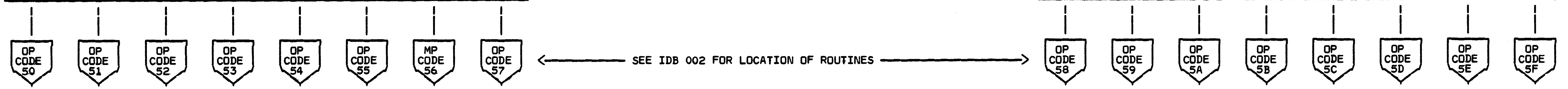
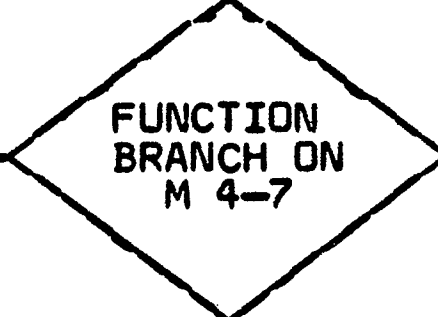
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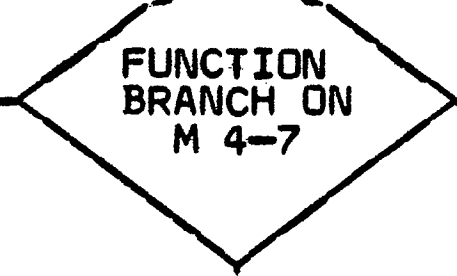
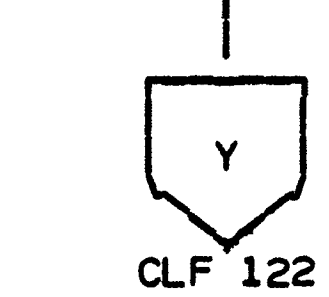
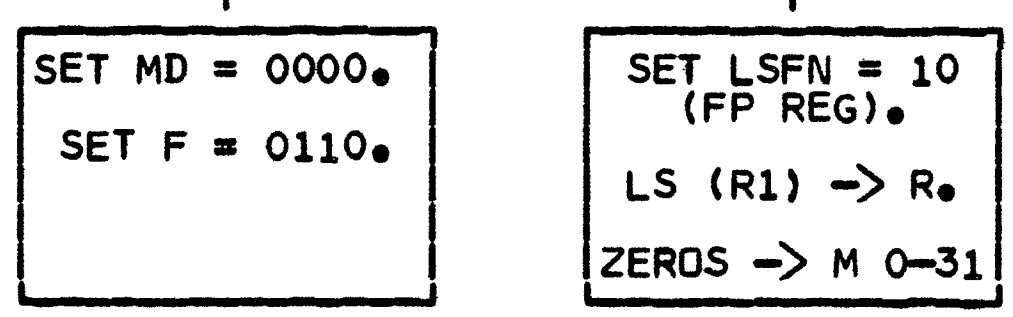
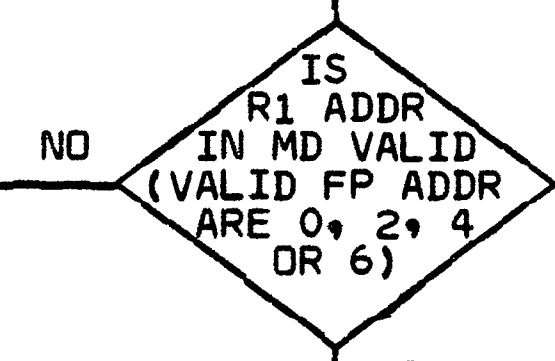
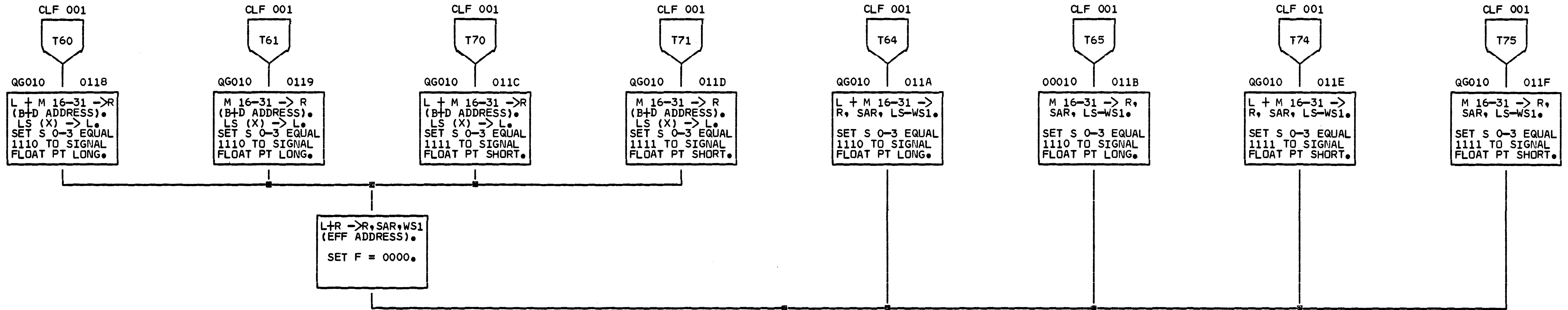
M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
0	50	STORE
1	51	INVALID OP
2	52	INVALID OP
3	53	INVALID OP
4	54	AND
5	55	COMPARE LOGICAL
6	56	OR
7	57	EXCLUSIVE OR

M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
8	58	LOAD
9	59	COMPARE
A	5A	ADD
B	5B	SUBTRACT
C	5C	MULTIPLY
D	5D	DIVIDE
E	5E	ADD LOGICAL
F	5F	SUBTRACT LOGICAL



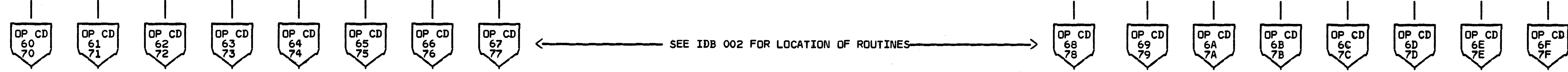
CLF 006  
 DATE 27 MAY 66 MACH. 2050  
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CLF 06



M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
0	60 70	
1	61 71	STORE - FLOATING POINT LONG STORE - FLOATING POINT SHORT
2	62 72	INVALID OP INVALID OP
3	63 73	INVALID OP INVALID OP
4	64 74	INVALID OP INVALID OP
5	65 75	INVALID OP INVALID OP
6	66 76	INVALID OP INVALID OP
7	67 77	INVALID OP INVALID OP

M 4-7 IN HEX	OP CODE IN HEX	INSTRUCTION
8	68 78	LOAD - FLOATING POINT LONG LOAD - FLOATING POINT SHORT
9	69 79	COMPARE - FLOATING POINT LONG COMPARE - FLOATING POINT SHORT
A	6A 7A	ADD NORMALIZED - FLOATING POINT LONG ADD NORMALIZED - FLOATING POINT SHORT
B	6B 7B	SUBTRACT NORMALIZED - FLOATING POINT LONG SUBTRACT NORMALIZED - FLOATING POINT SHORT
C	6C 7C	MULTIPLY - FLOATING POINT LONG MULTIPLY - FLOATING POINT SHORT
D	6D 7D	DIVIDE - FLOATING POINT LONG DIVIDE - FLOATING POINT SHORT
E	6E 7E	ADD UNNORMALIZED - FLOATING POINT LONG ADD UNNORMALIZED - FLOATING POINT SHORT
F	6F 7F	SUBTRACT UNNORMALIZED - FLOATING POINT LONG SUBTRACT UNNORMALIZED - FLOATING POINT SHORT

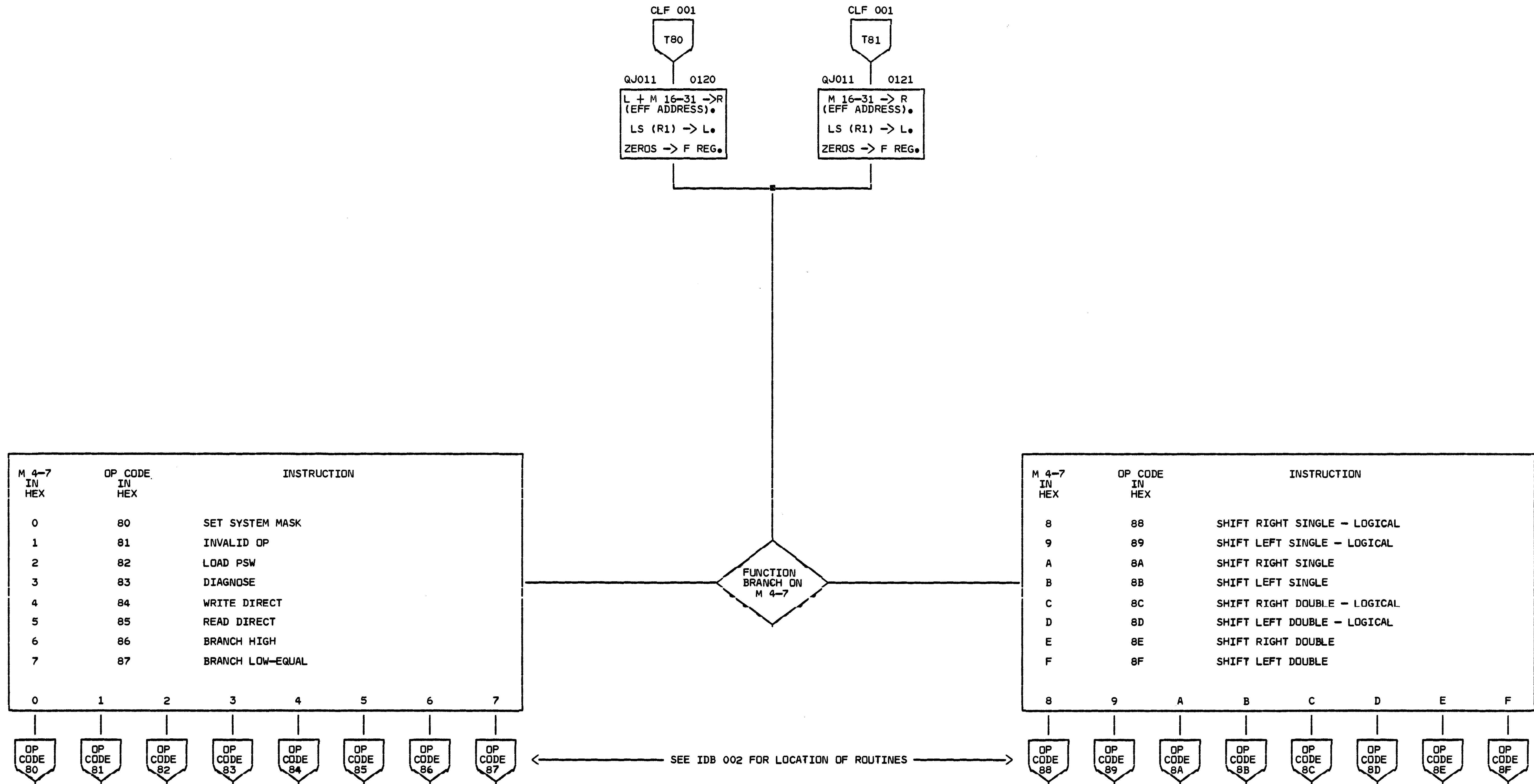


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DATE 27 MAY 66 MACH. 2050  
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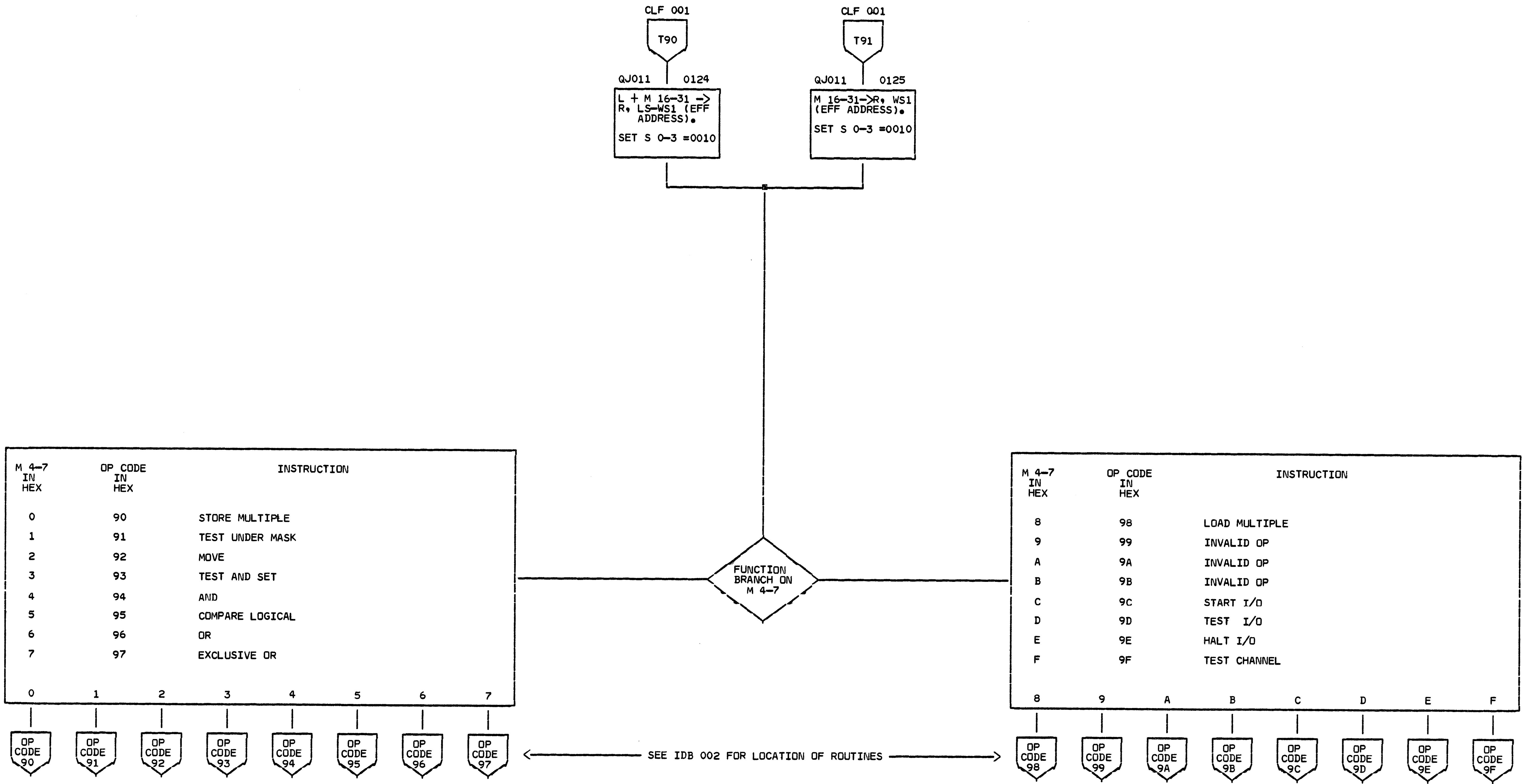
CLF07

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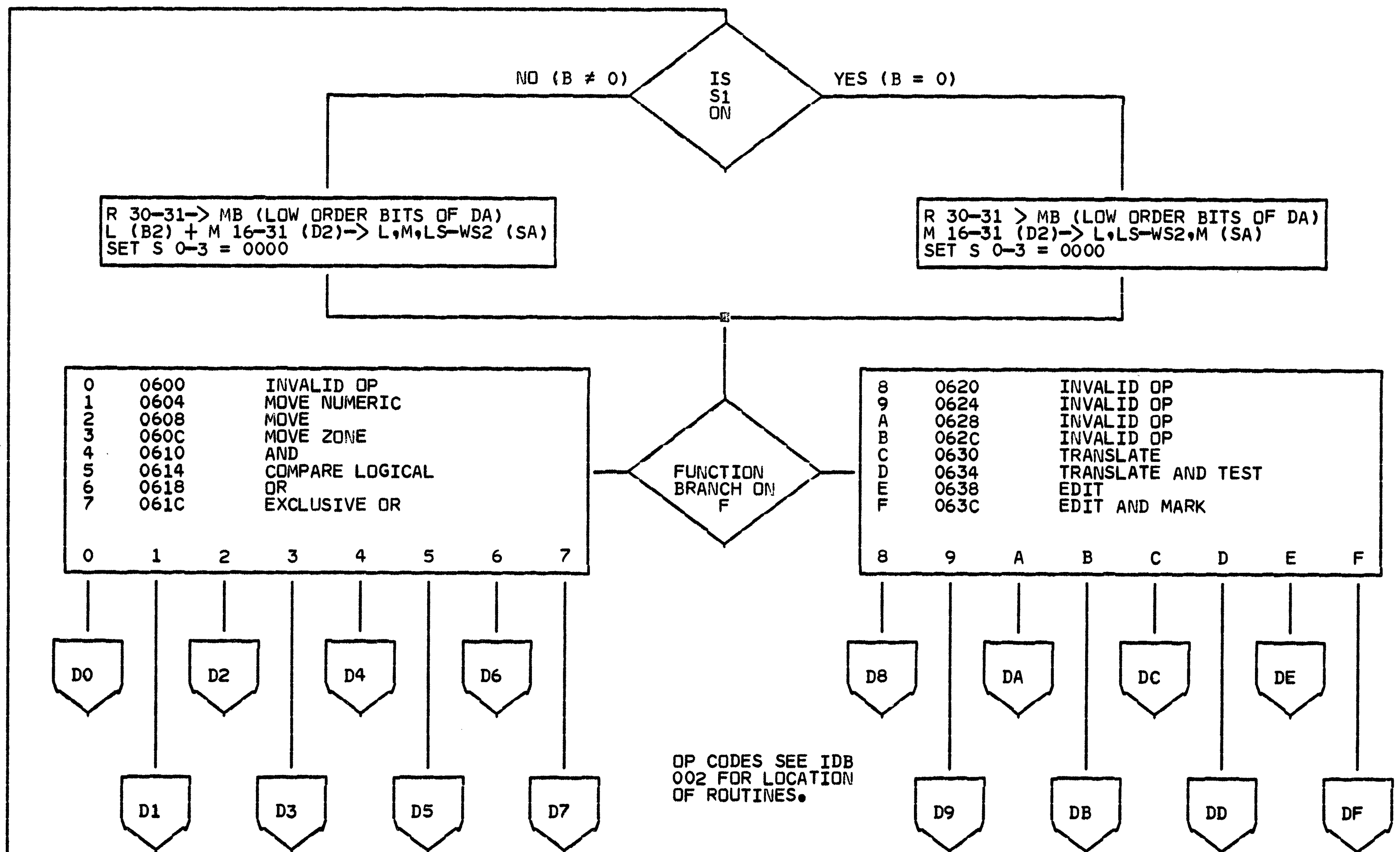
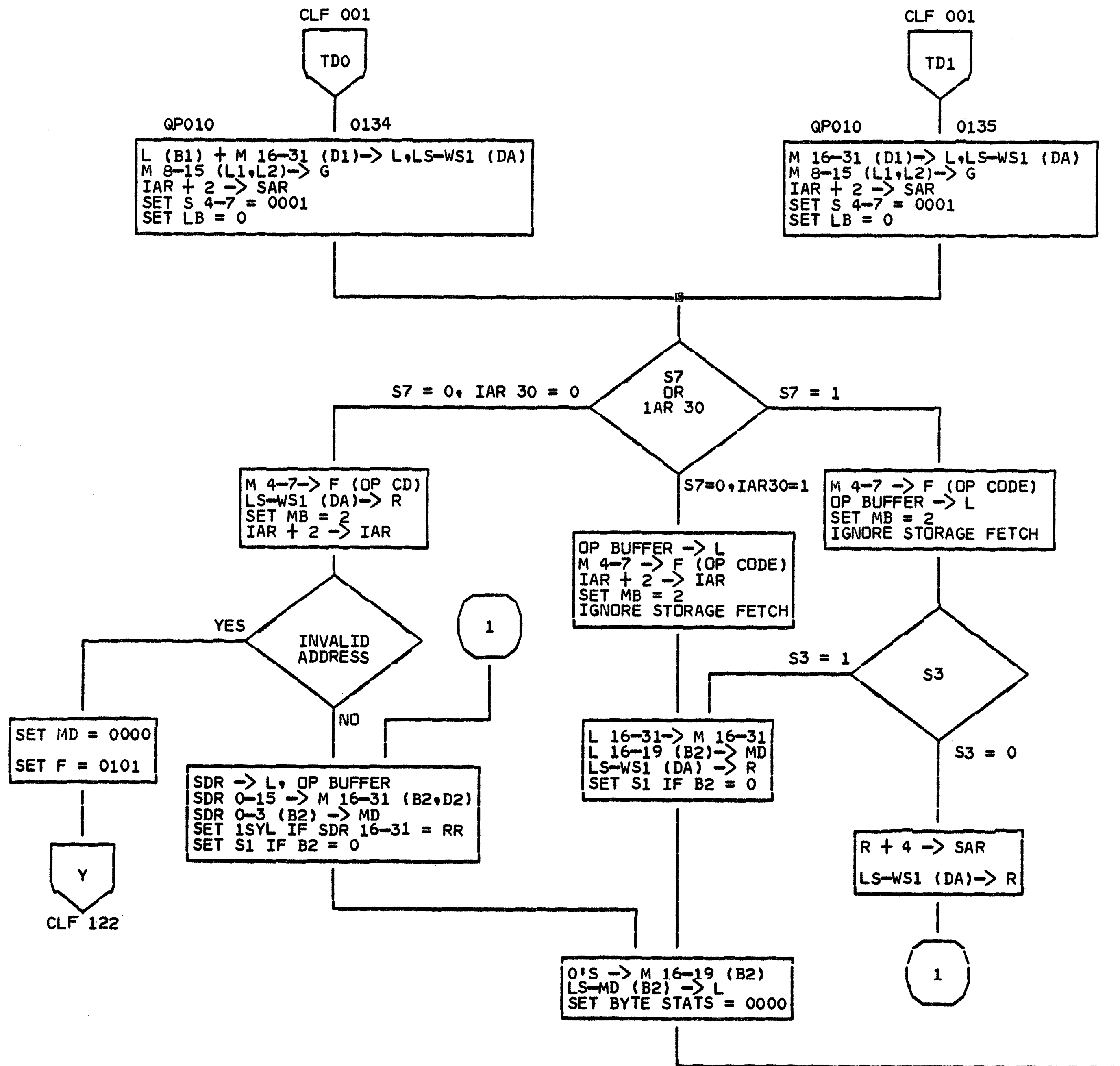
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CLF09

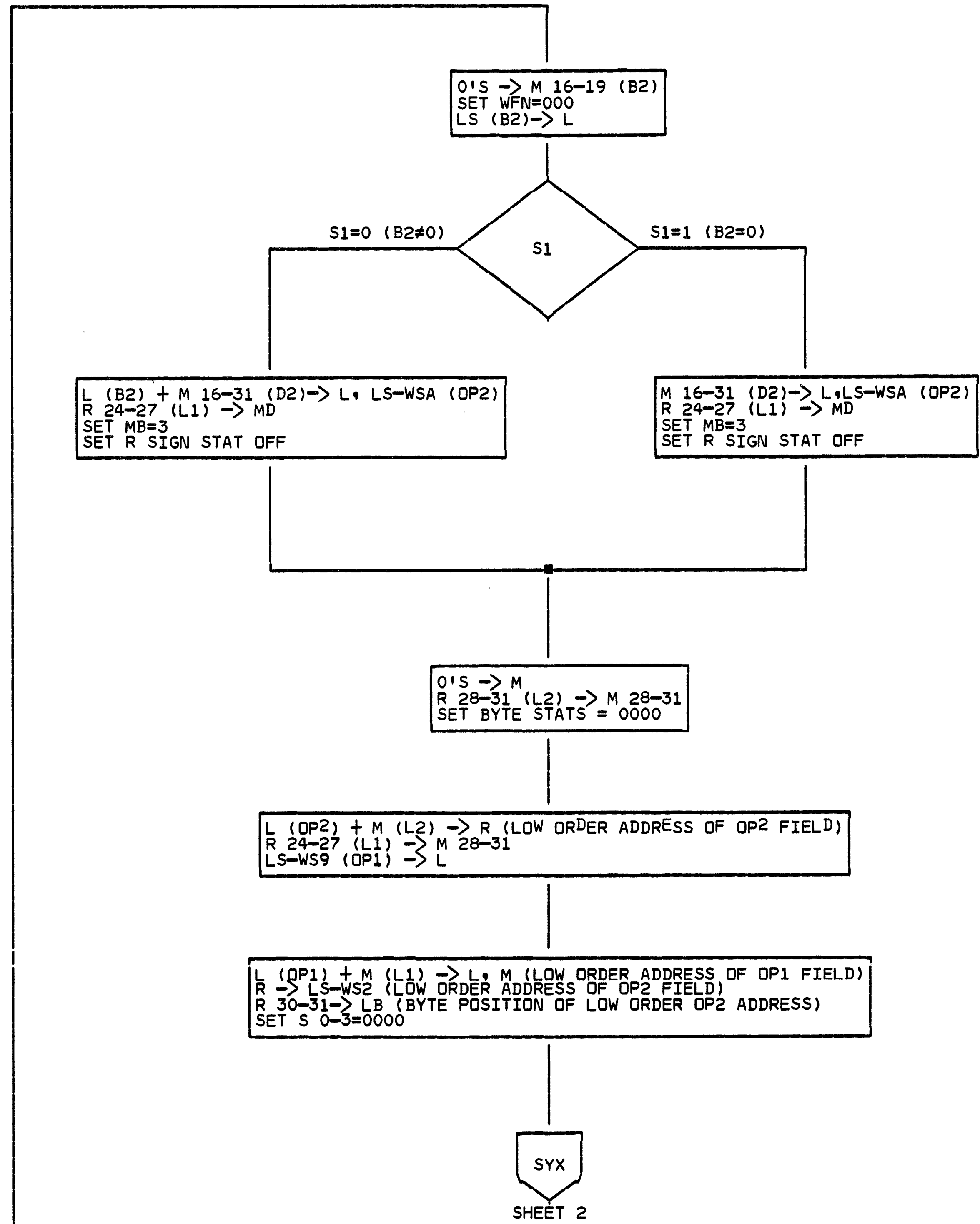
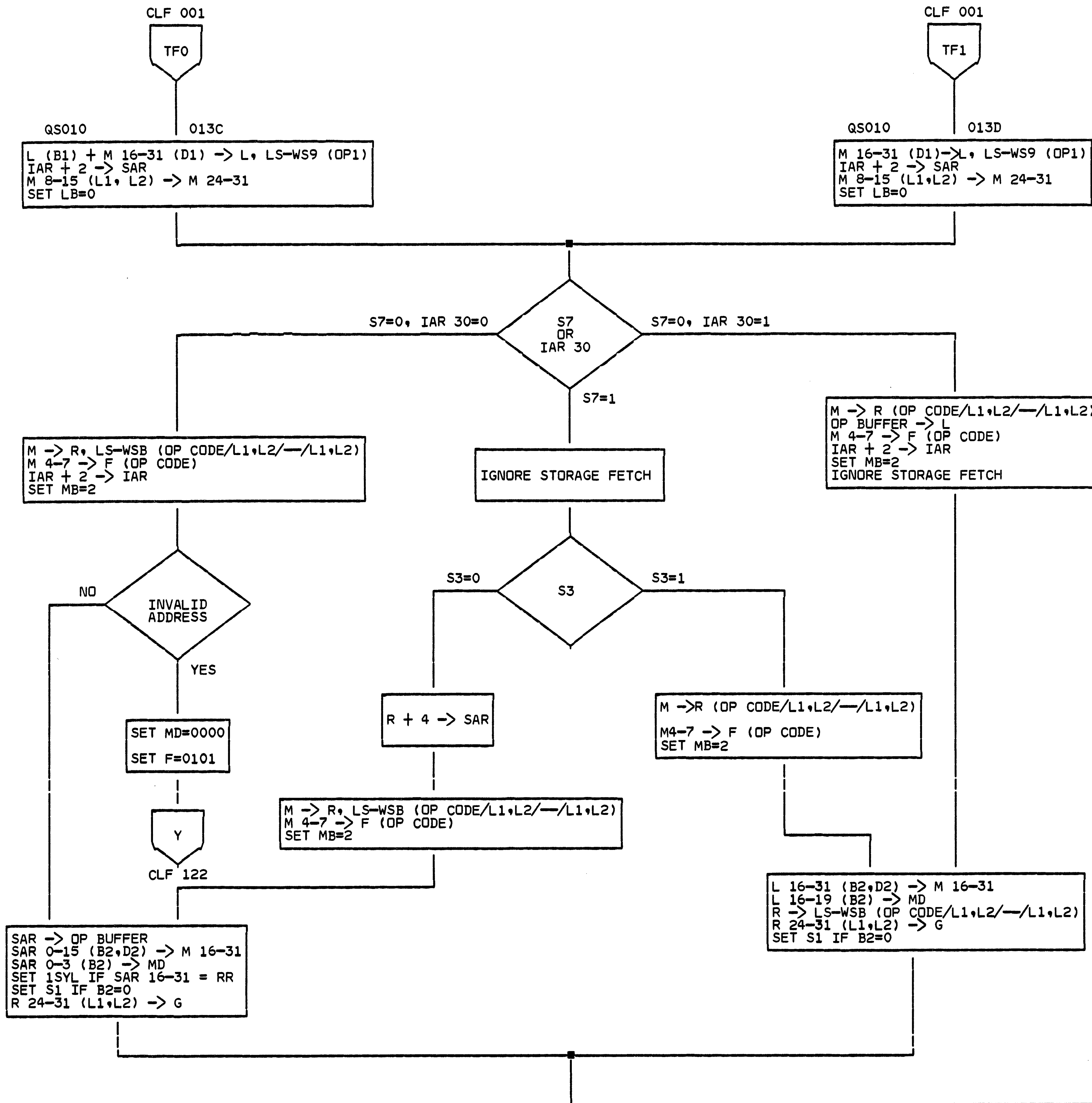


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OP CODES SEE IDB 002 FOR LOCATION OF ROUTINES.

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SHEET 2

CLF 011 (1 OF 2)  
 DATE 3 JUN 66 MACH. 2050  
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CLF 11

SHEET 1

SYX

R → SAR (LOW ORDER ADDRESS OF OP2 FIELD)

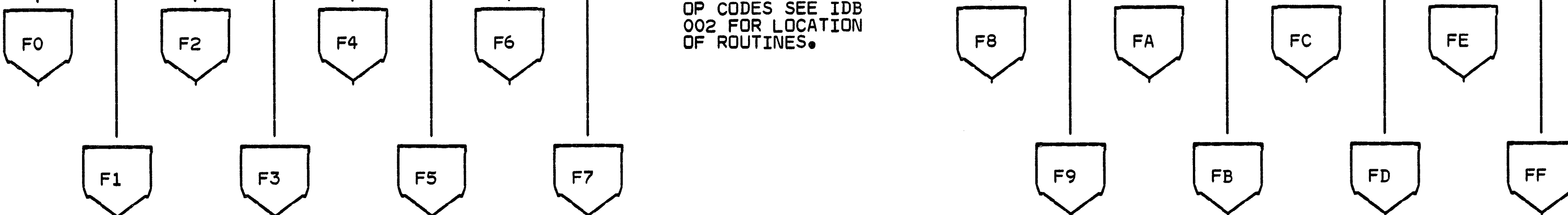
M 30-31 → MB (LOW ORDER BYTE POSITION OF OP1 FIELD)  
 M (L1 + OP1) → H (LOW ORDER ADDRESS OF OP1 FIELD)  
 L → LS-WS1 (LOW ORDER ADDRESS OF OP1 FIELD)  
 SET S4-7 = 0000

0	OC00	INVALID OP
1	OC04	MOVE WITH OFFSET
2	OC08	PACK
3	OC0C	UNPACK
4	OC10	INVALID OP
5	OC14	INVALID OP
6	OC18	INVALID OP
7	OC1C	INVALID OP

FUNCTION  
BRANCH ON  
F

8	OC20	ZERO AND ADD
9	OC24	COMPARE
A	OC28	ADD
B	OC2C	SUBTRACT
C	OC30	MULTIPLY
D	OC34	DIVIDE
E	OC38	INVALID OP
F	OC3C	INVALID OP

OP CODES SEE IDB  
002 FOR LOCATION  
OF ROUTINES.



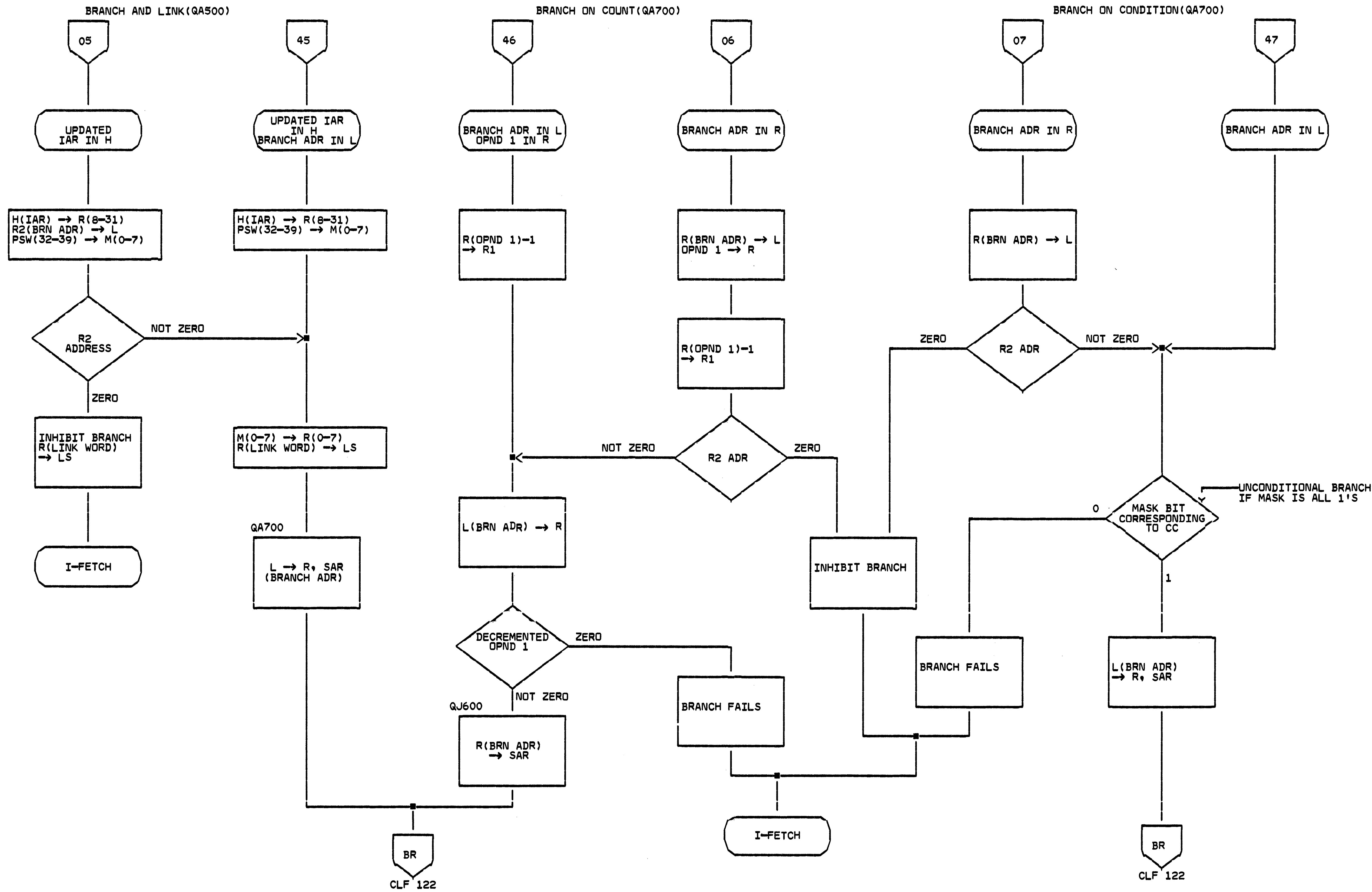
CONDITIONS AT END OF SECOND LEVEL I-FETCH

WS1 = ADDRESS OF LOW ORDER POSITION OF OP1 FIELD.  
 WS2 = ADDRESS OF LOW ORDER POSITION OF OP2 FIELD.  
 WS9 = OP1  
 WSA = OP2  
 WSB = OP CODE/L1, L2/—/L1, L2  
 H REG = ADDRESS OF LOW ORDER POSITION OF OP1 FIELD.  
 LB REG = LOW ORDER BYTE POSITION OF OP2 FIELD.  
 MB REG = LOW ORDER BYTE POSITION OF OP1 FIELD.  
 R SIGN STAT IS OFF.  
 STATS 0-7 ARE OFF.  
 MOVER FUNCTION REGISTER SET TO 000

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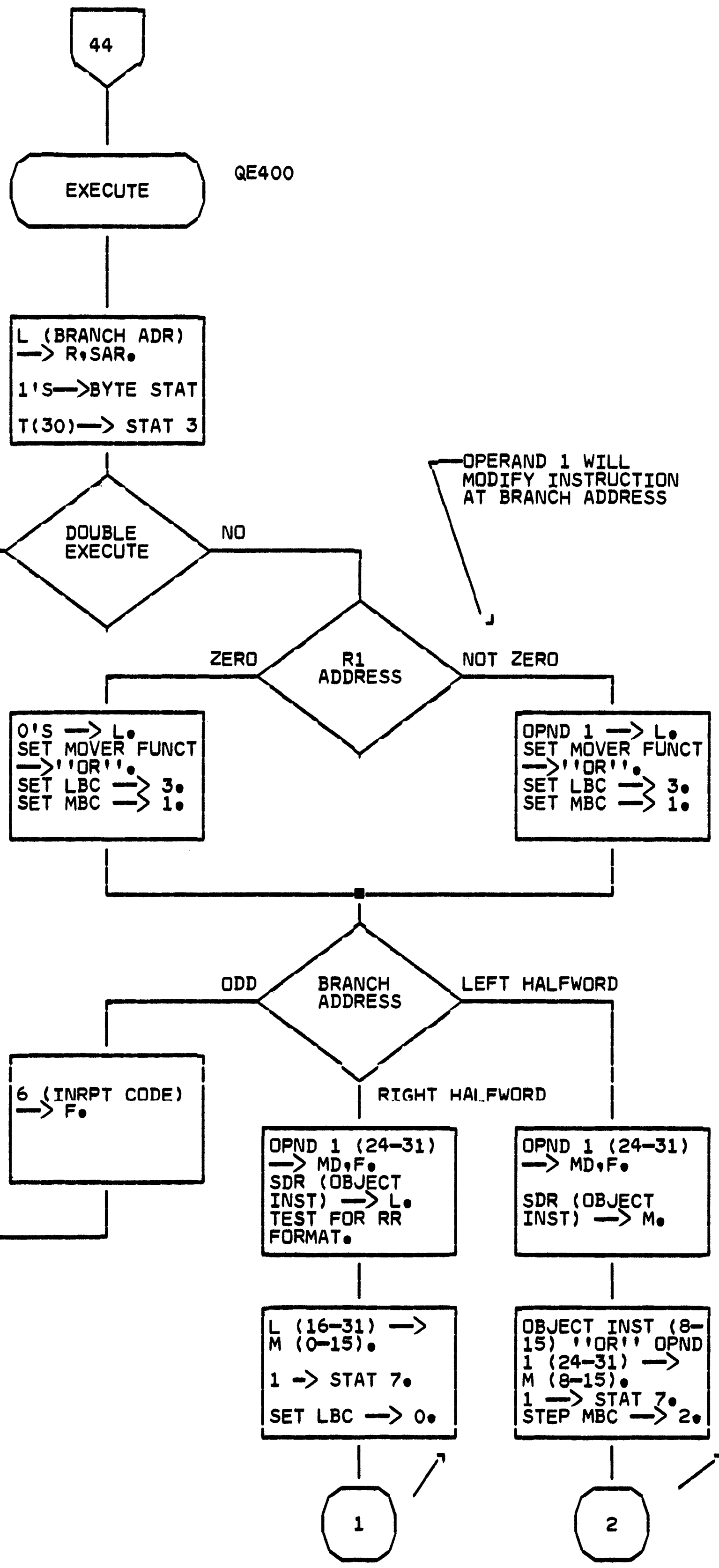


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BR  
CLF 122

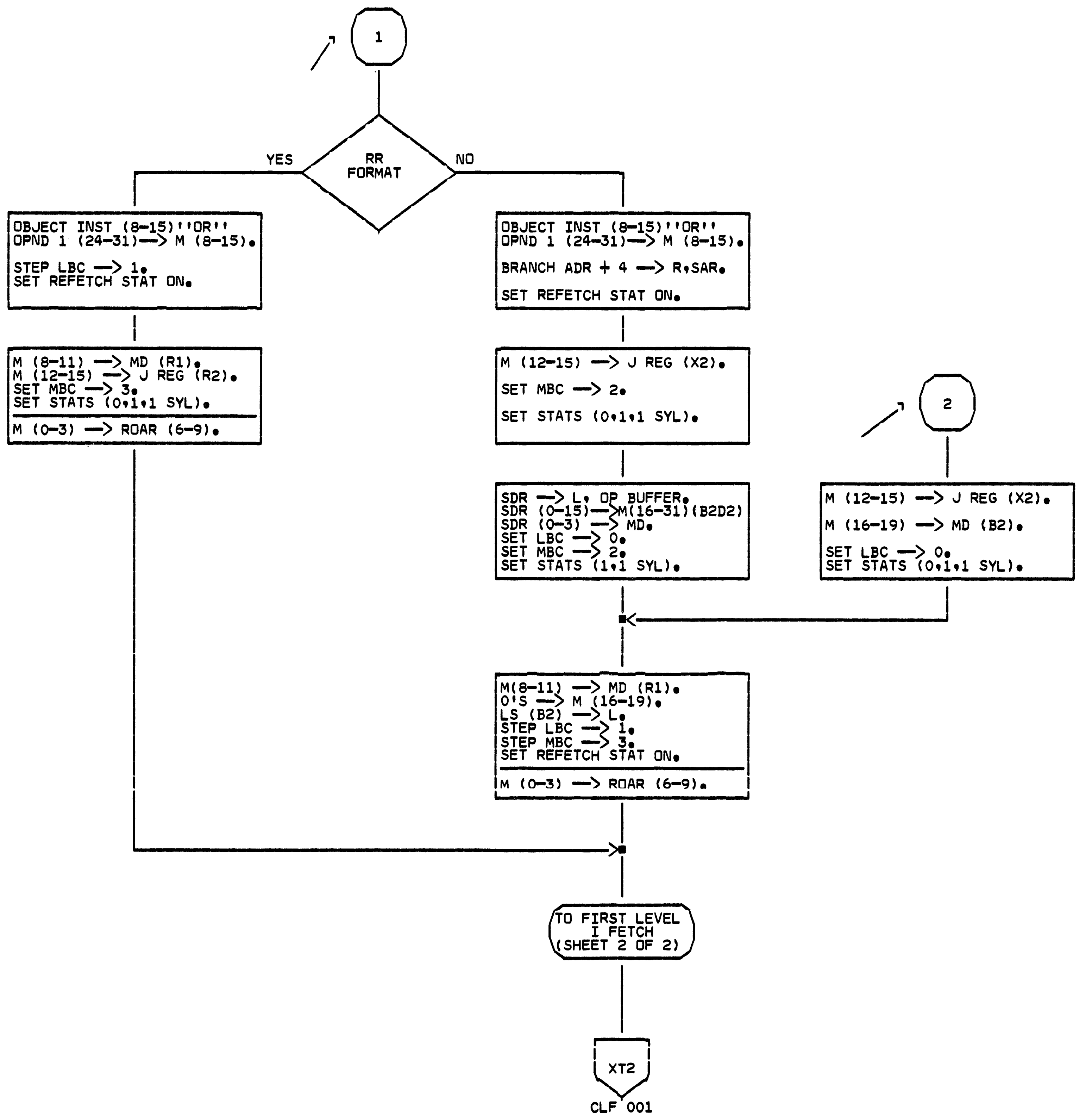
FIRST LEVEL I FETCH TURNS STAT 7 OFF. EXECUTE TURNS STAT 7 ON. STAT 7 IS ON IF THE INSTRUCTION IMMEDIATELY BEHIND EXECUTE (OBJECT INSTRUCTION) IS ALSO AN EXECUTE INSTRUCTION.

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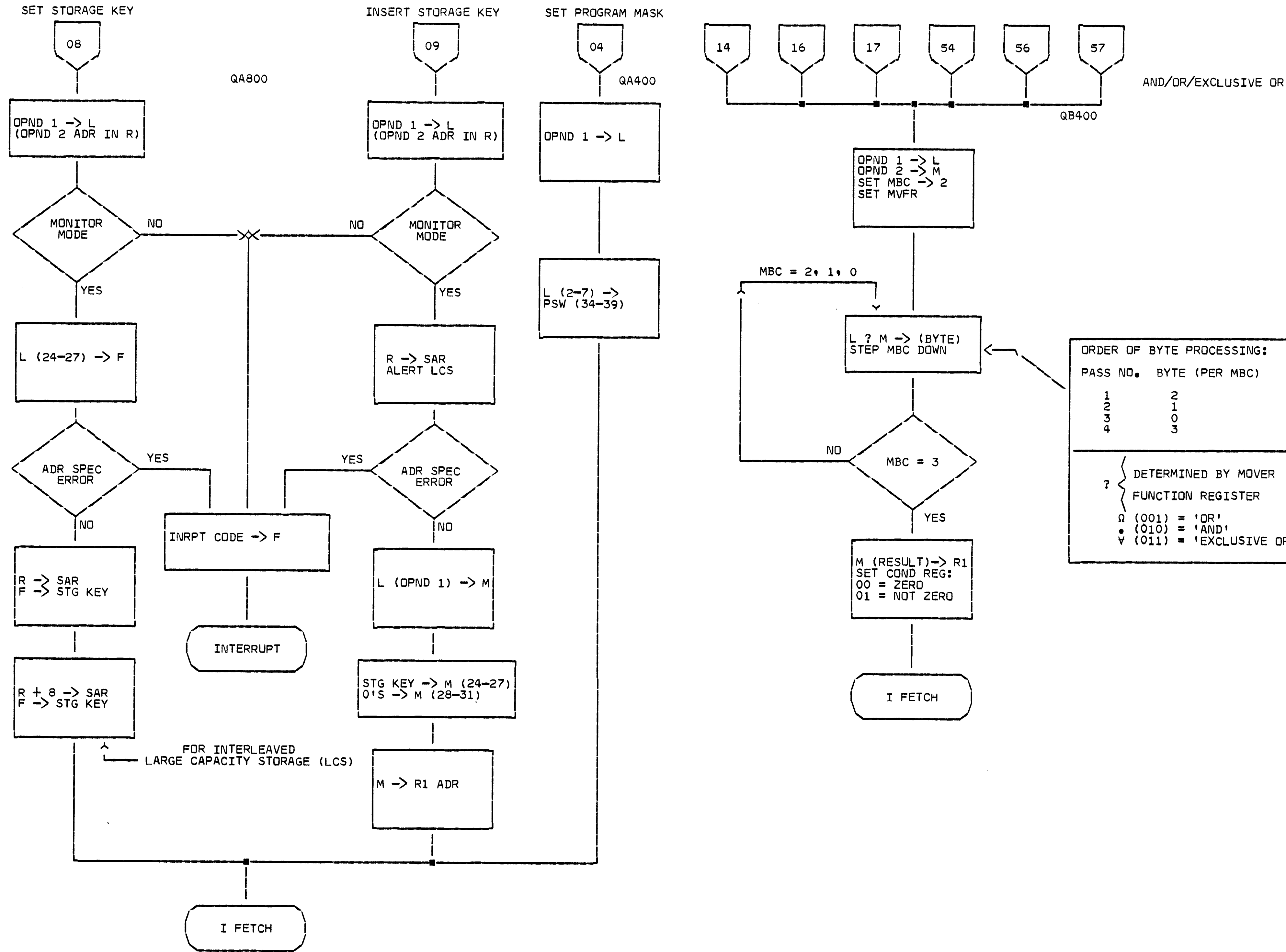


INTERRUPT

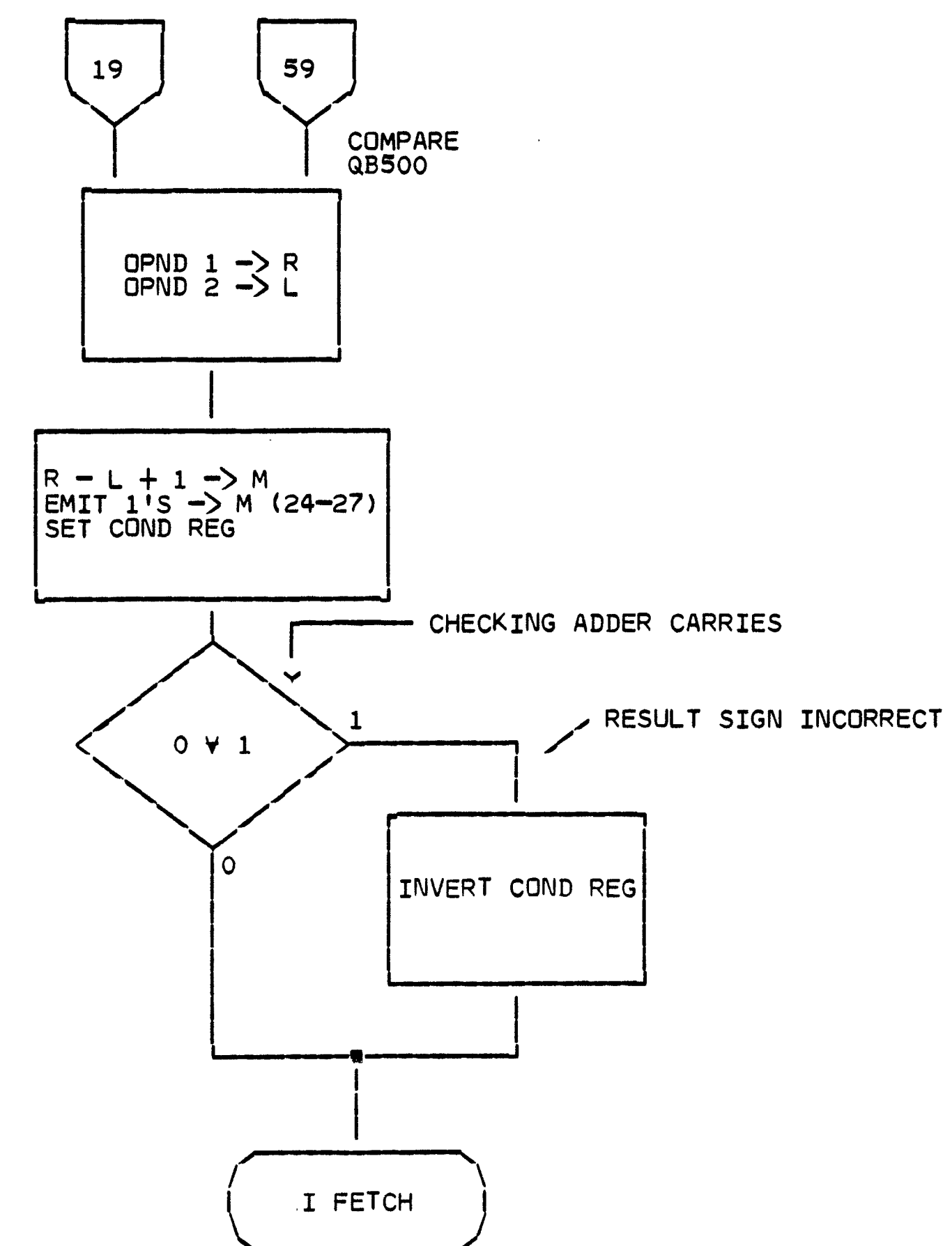
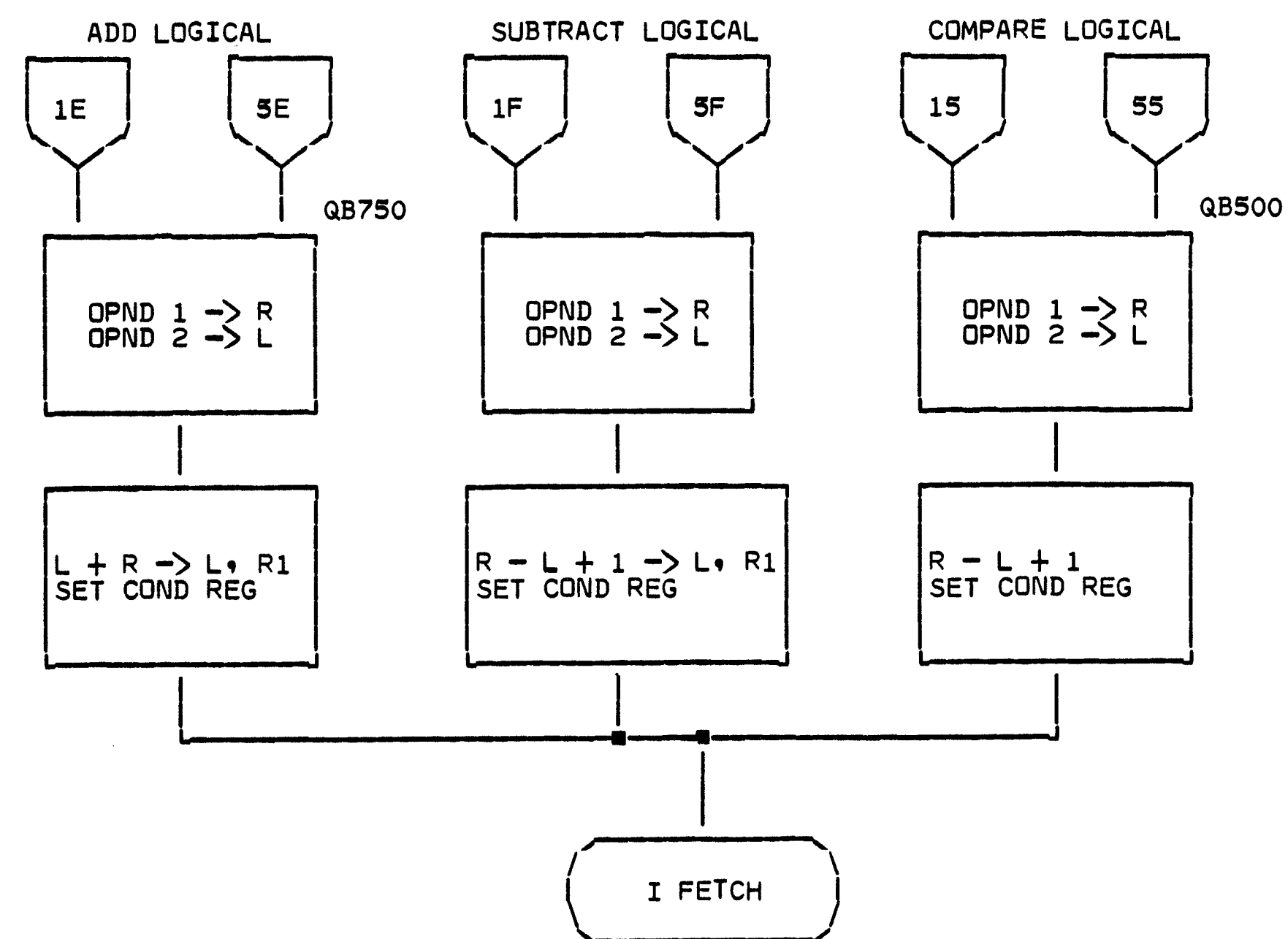
PROG  
CLF 122



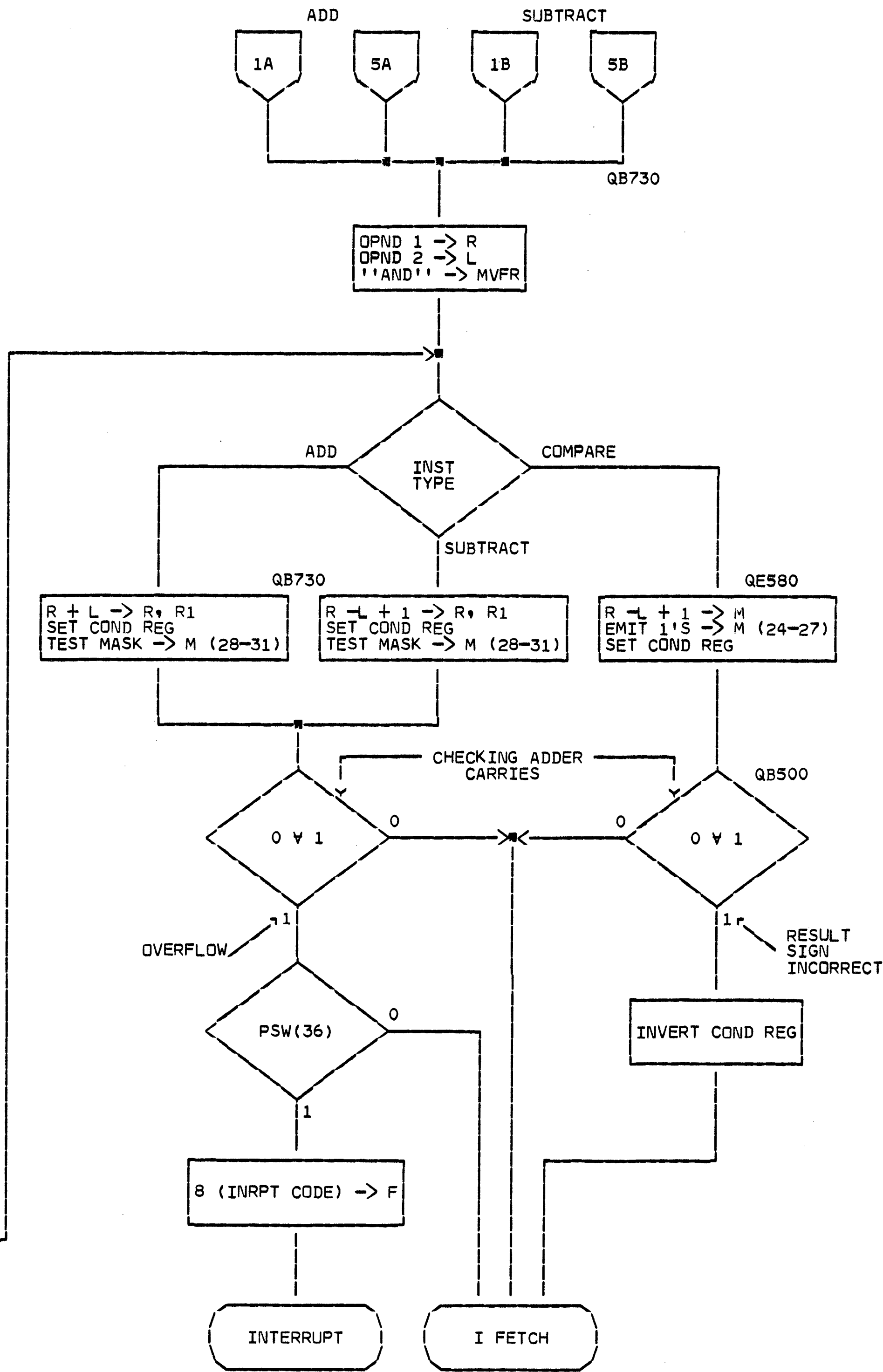
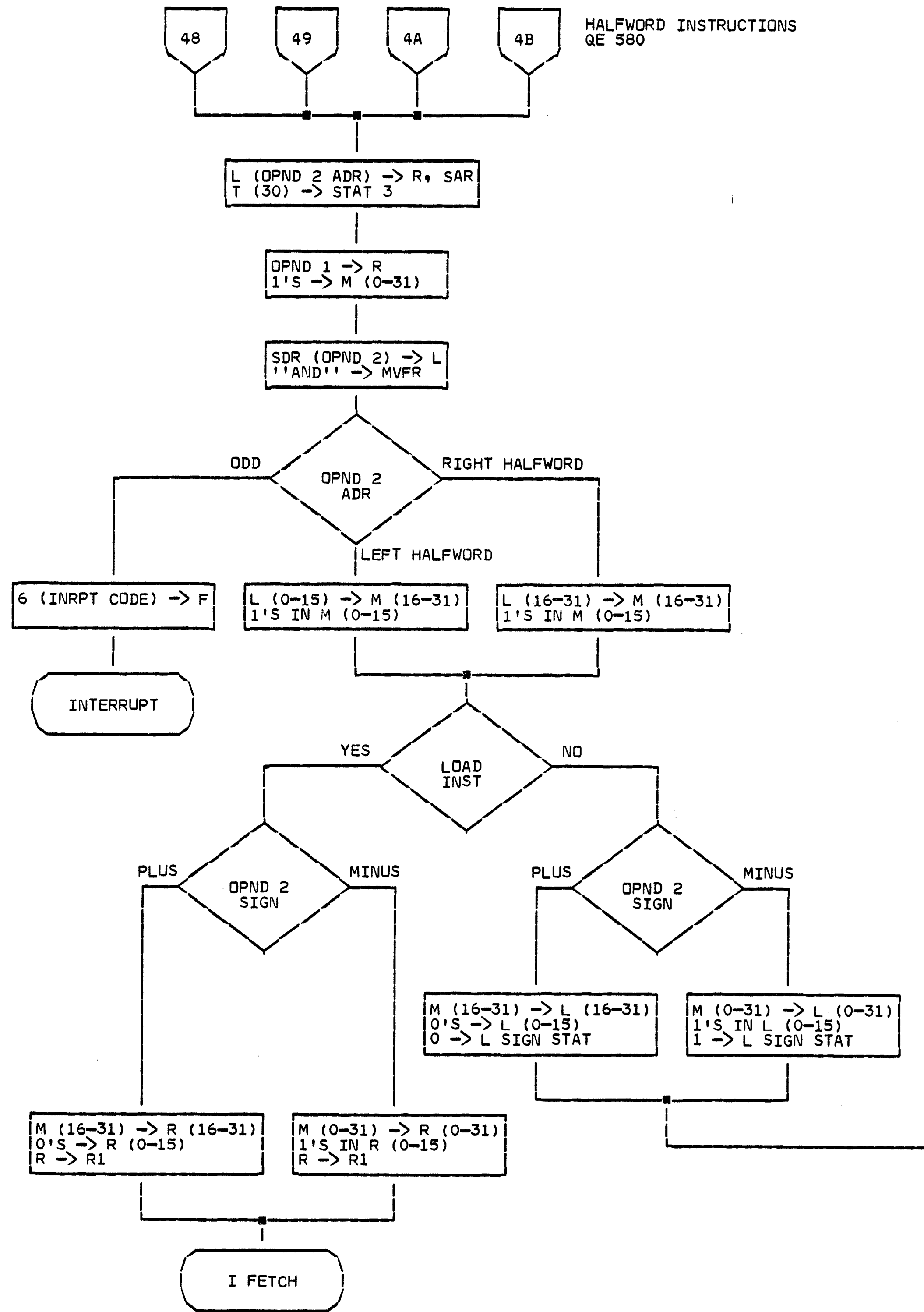




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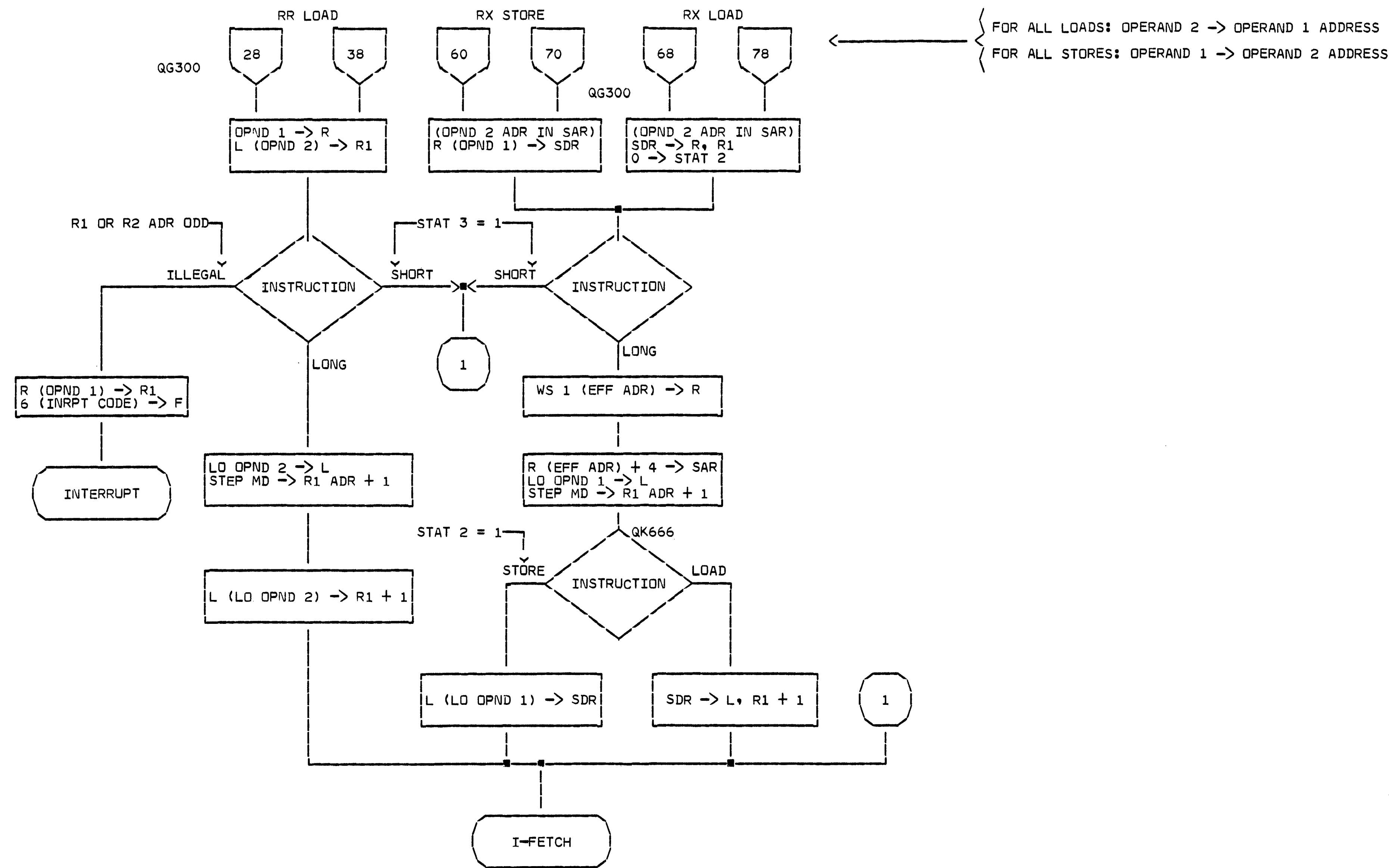
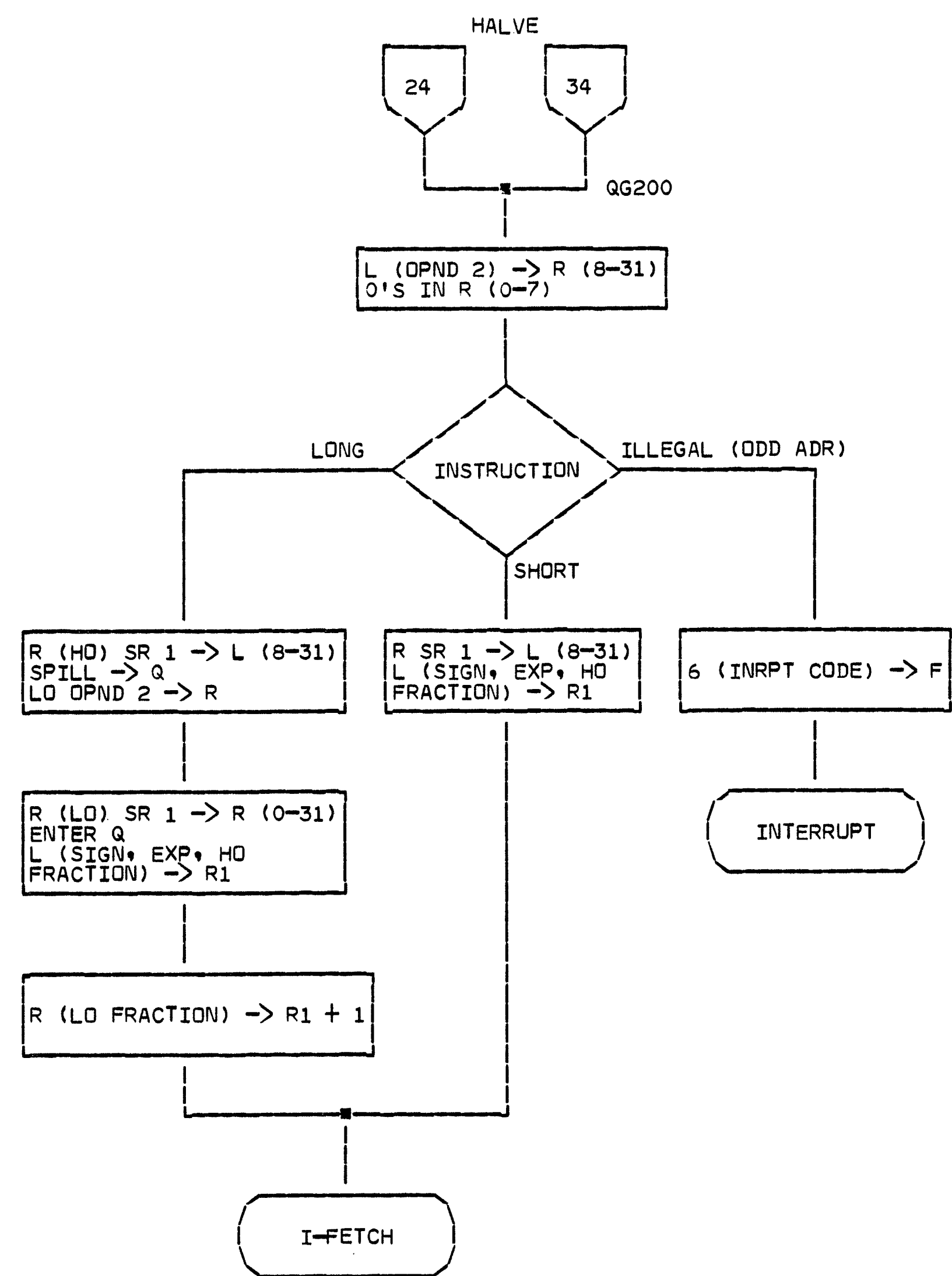
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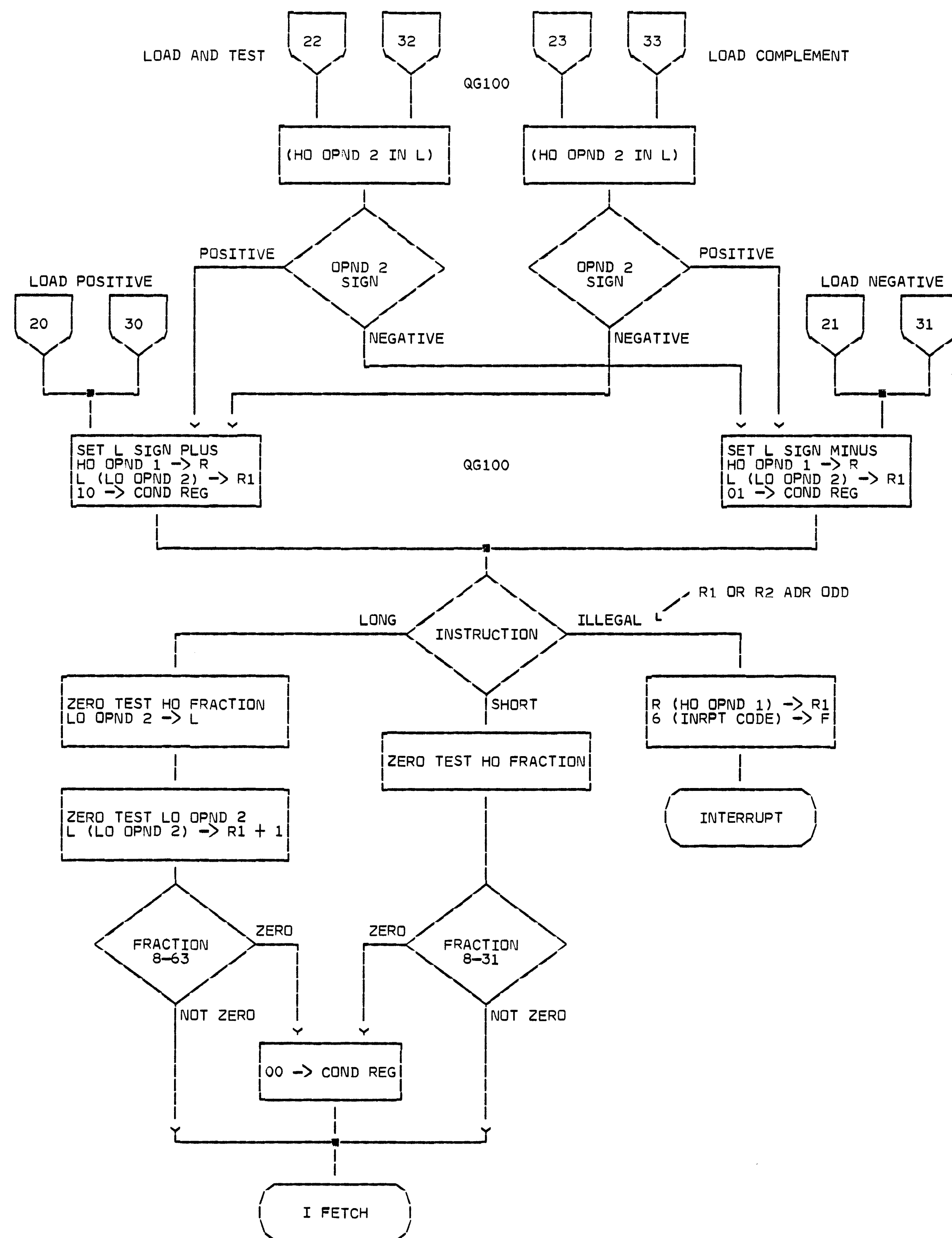
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DATE 23 MAR 65 MACH. 2050  
FRAME  
P. N.  
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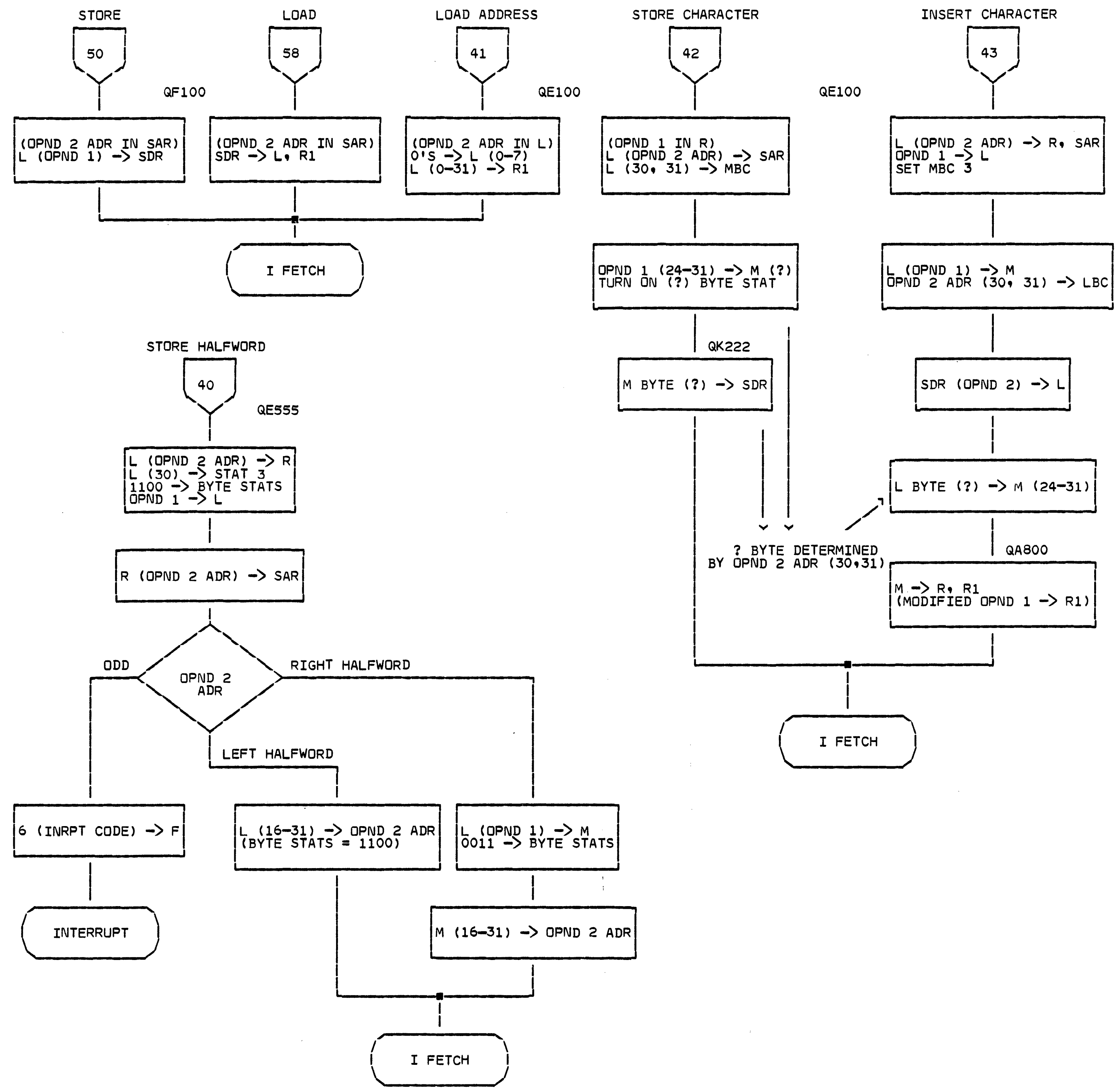
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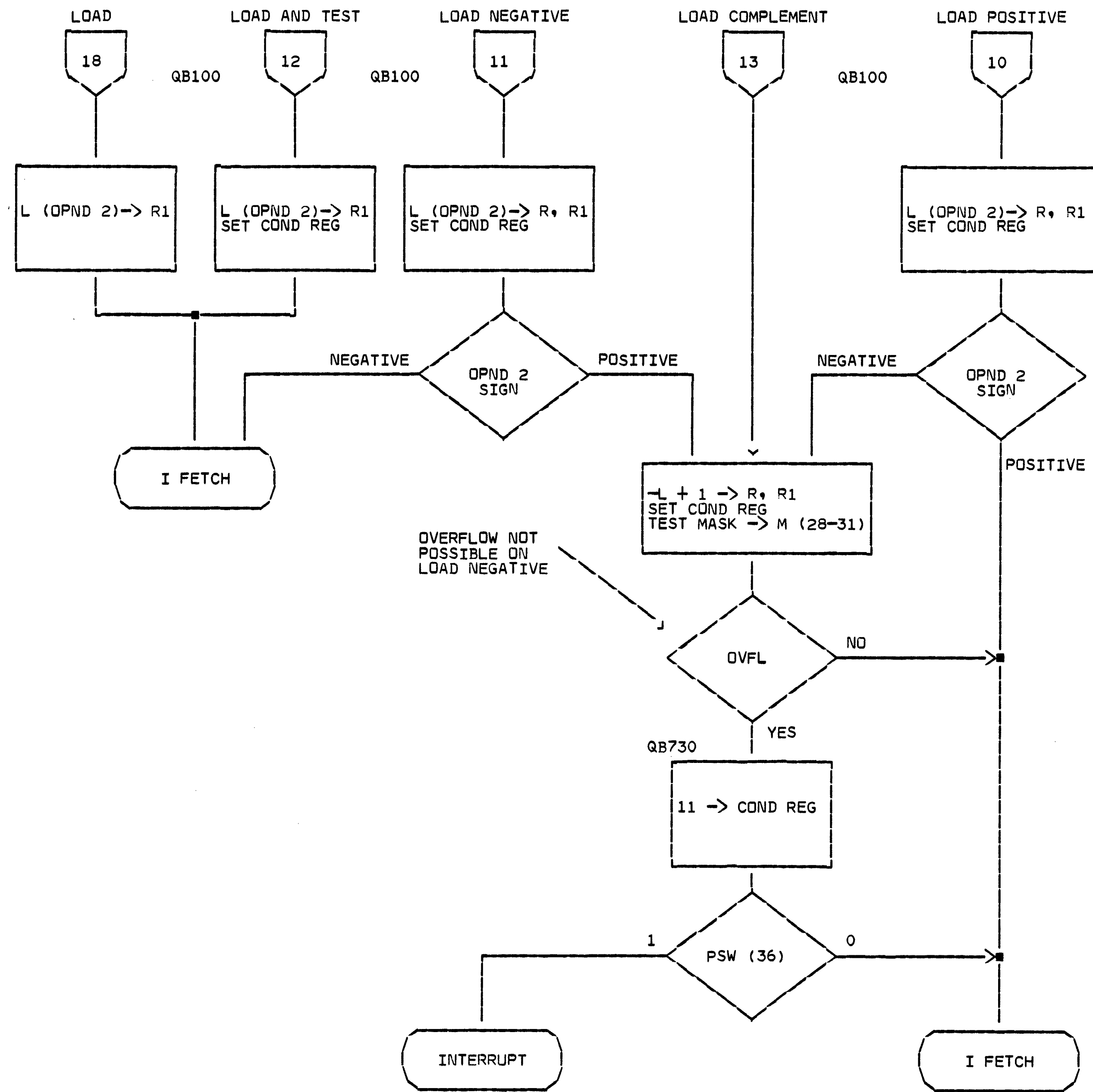
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 DATE 23 MAR 65 MACH. 2050  
 FRAME  
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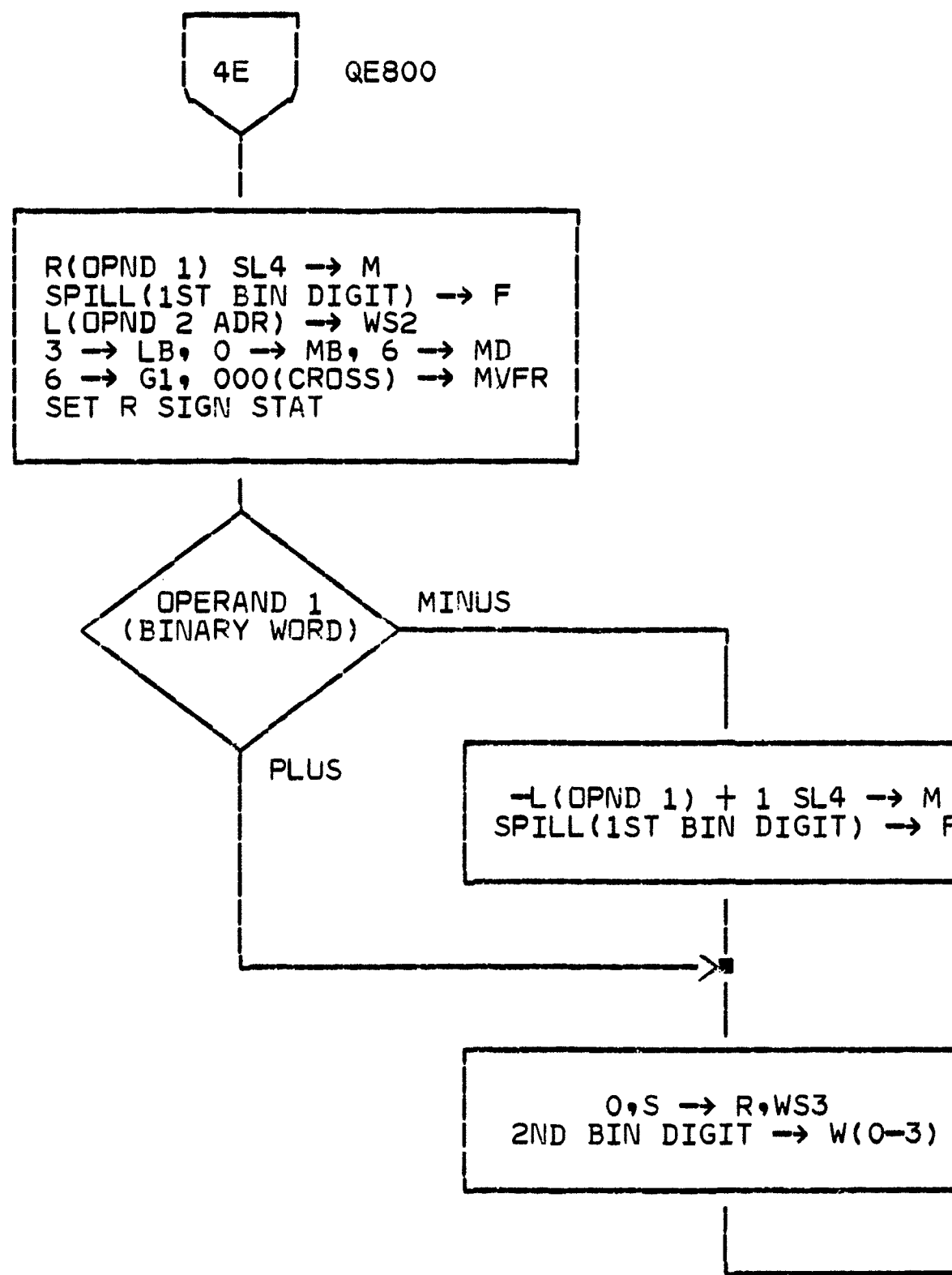
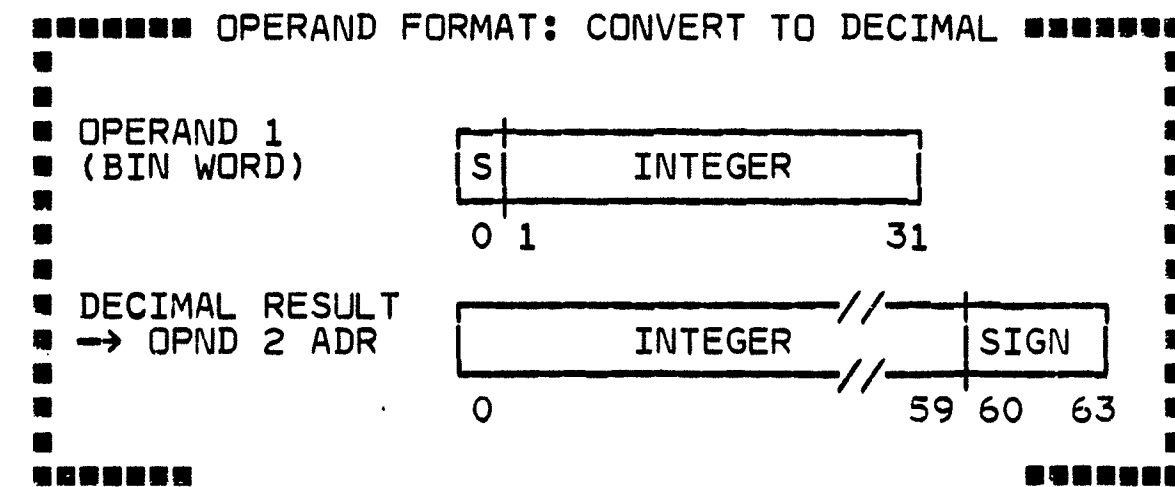


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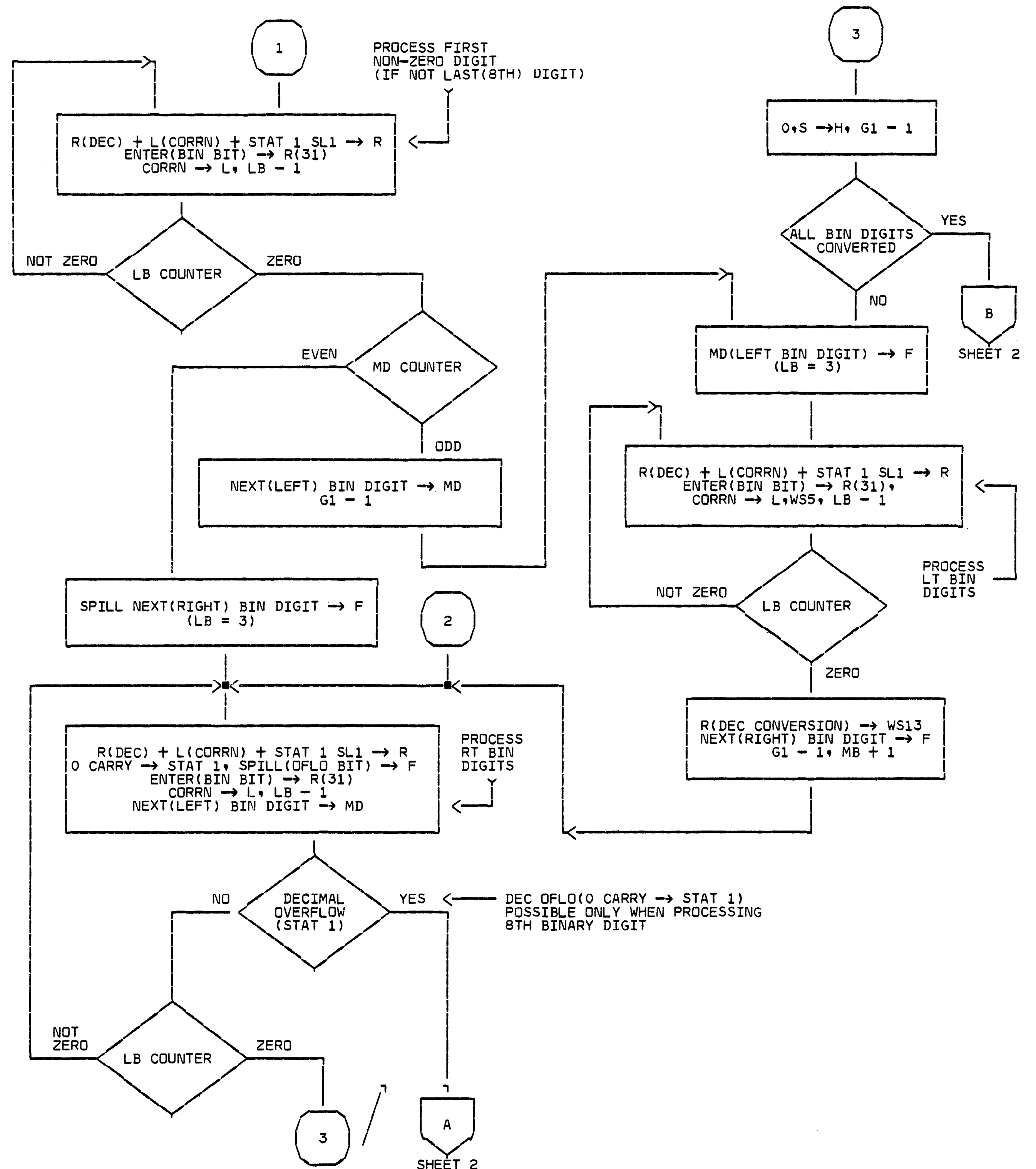
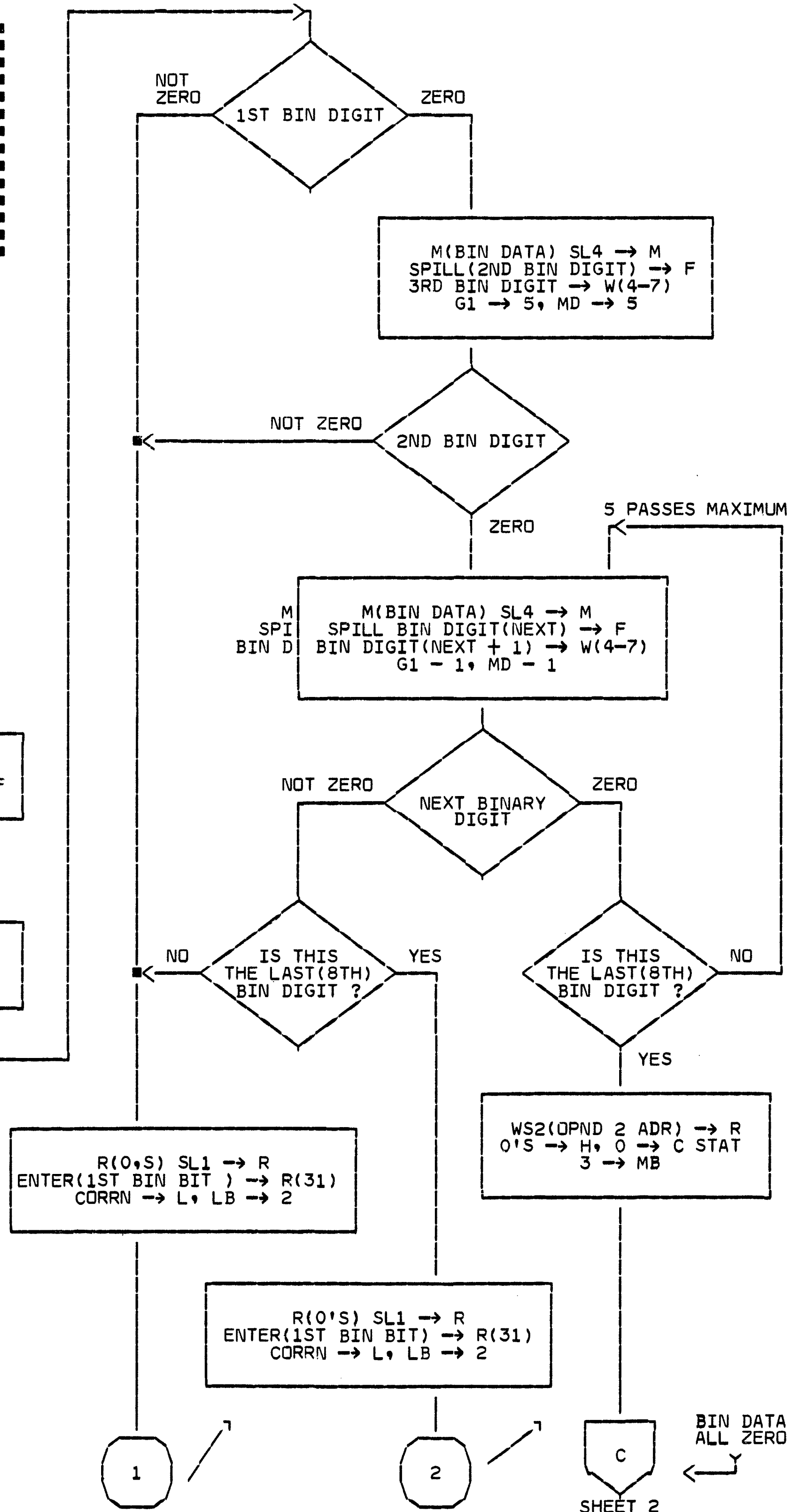
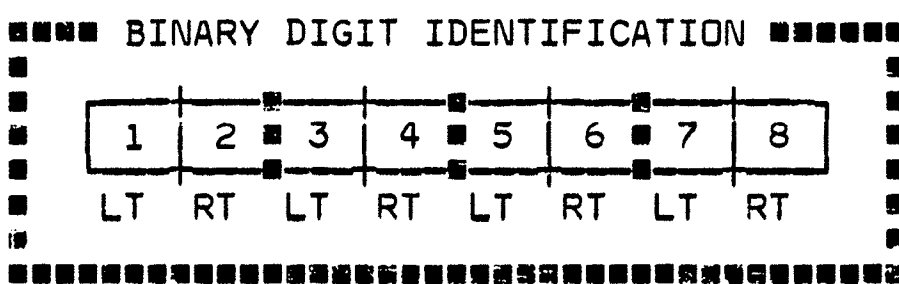


DECIMAL OVERFLOW POSSIBLE ONLY WHEN PROCESSING 8TH BINARY DIGIT. IF DECIMAL CONVERSION OVERFLOWS R REGISTER, RESTORE R AND L REGISTERS TO VALUES PRESENT AFTER PROCESSING THE PRECEEDING (7TH) DIGIT.

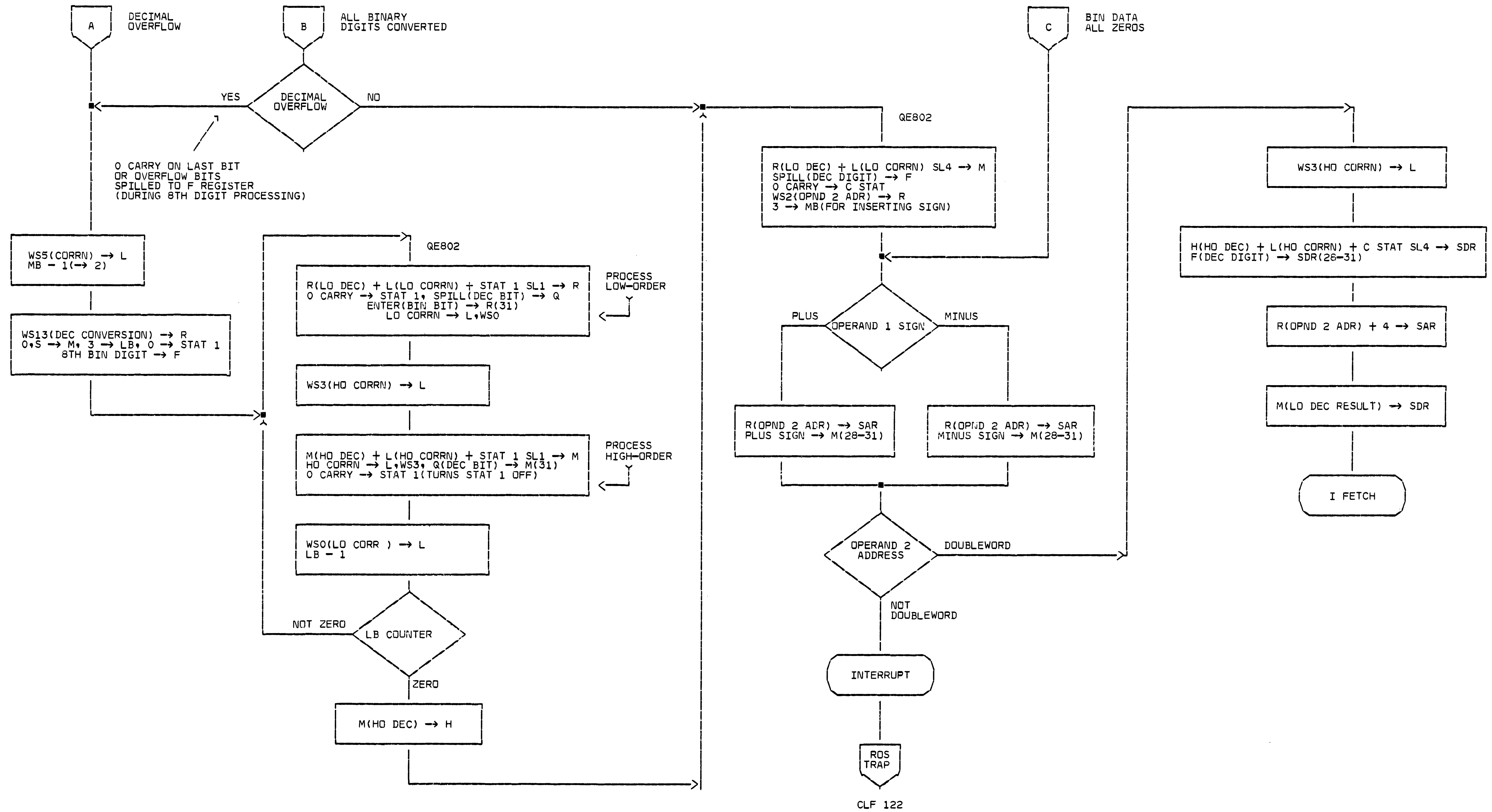
WORKING STORAGE LOCATIONS USED FOR DECIMAL OVERFLOW CONDITION(DEC RESULT > 1 FULLWORD):

WS0 LD CORRNL FOR DOUBLEWORD DEC RESULT  
WS3 HD CORRNL FOR DOUBLEWORD DEC RESULT

WS5 CORRNL FOR 7TH CONVERTED DIGIT  
WS13 DEC CONVERSION OF 7TH CONVERTED DIGIT

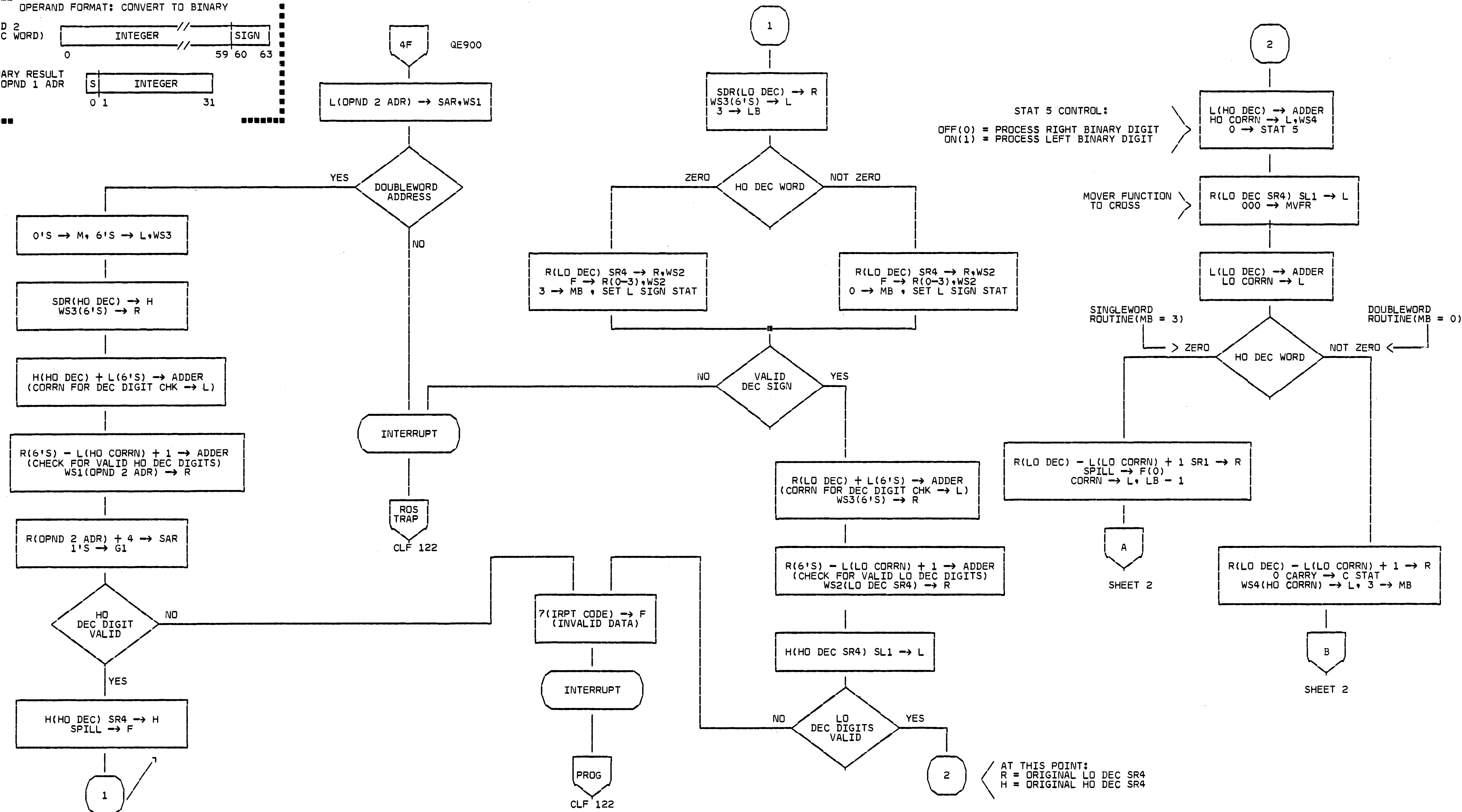
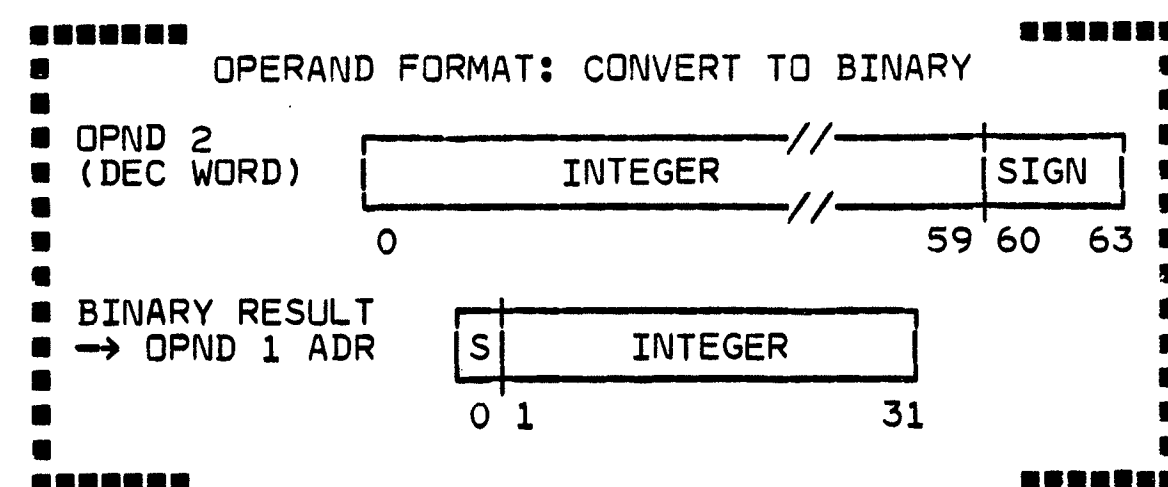






CLF 122

CL111



STAT 5 CONTROL:  
OFF(0) = PROCESS RIGHT BINARY DIGIT  
ON(1) = PROCESS LEFT BINARY DIGIT

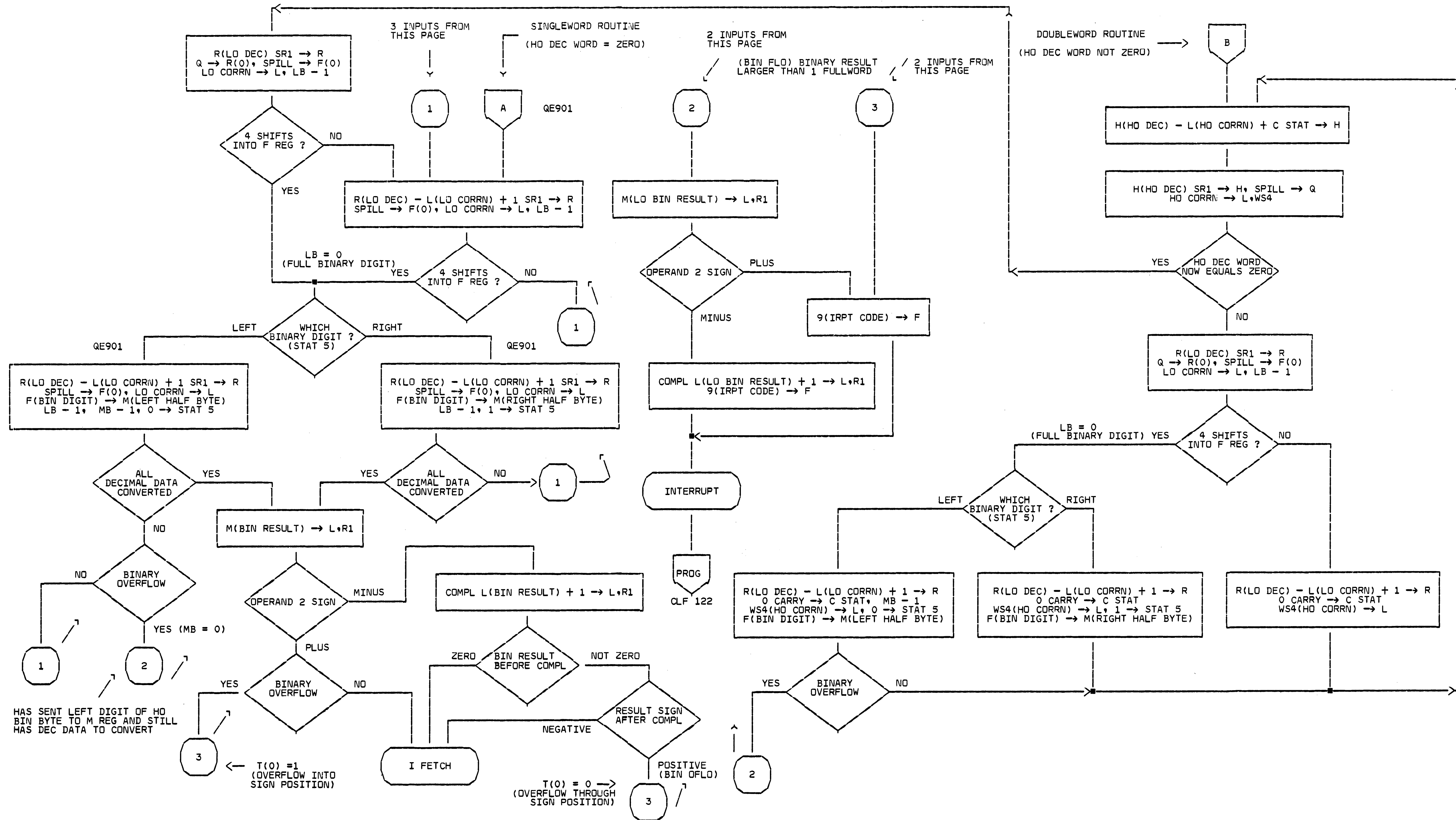
MOVER FUNCTION TO CROSS

SINGLEWORD ROUTINE (MB = 3)

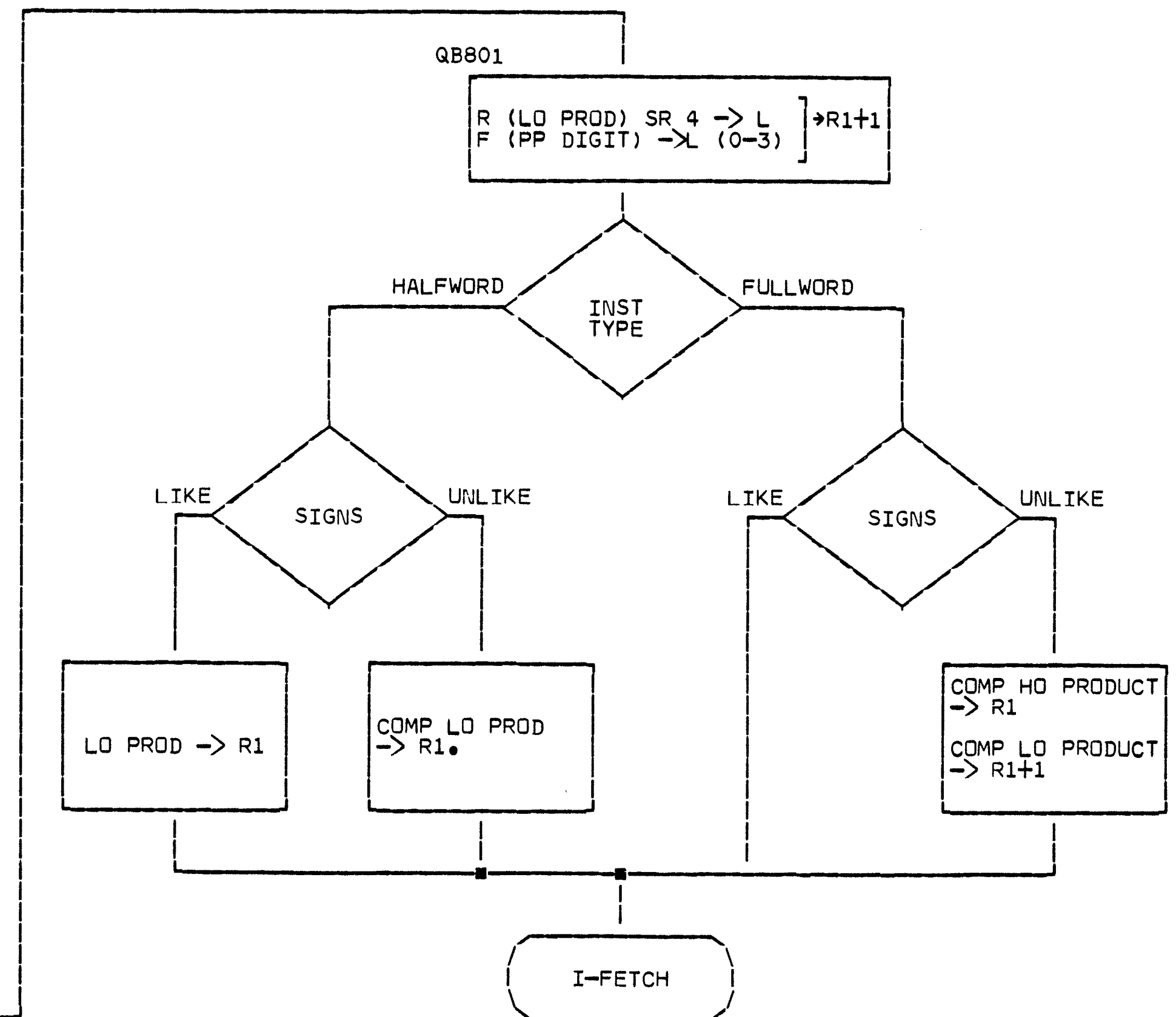
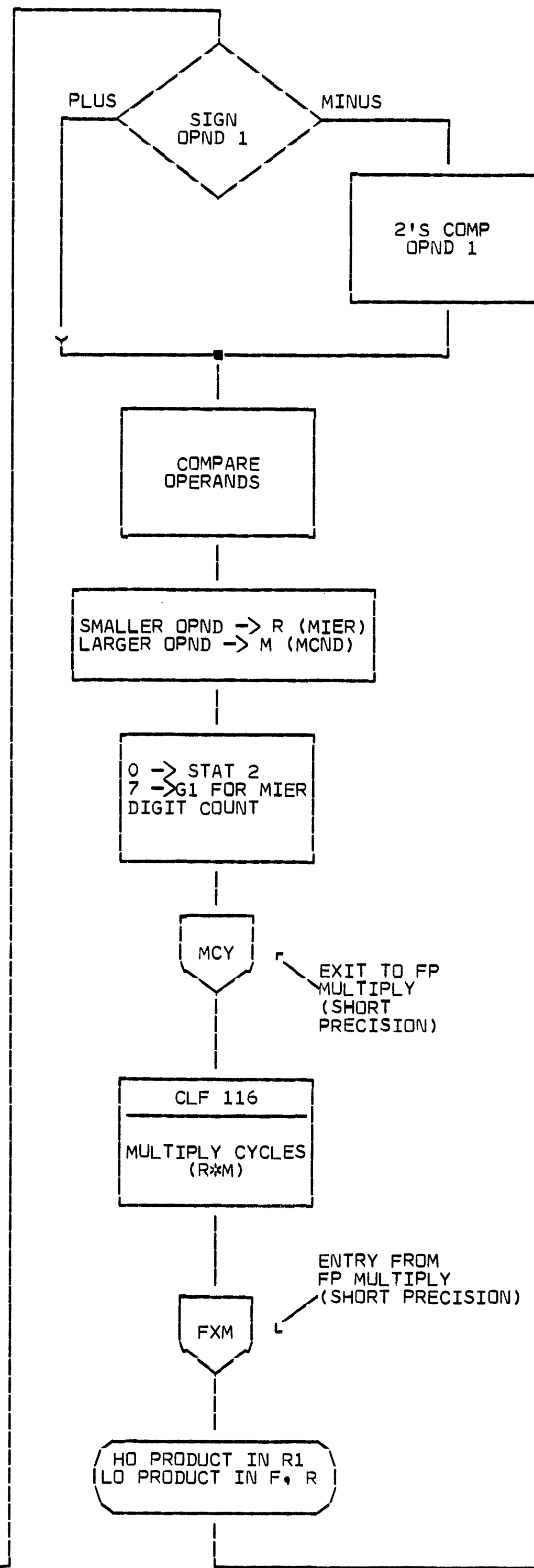
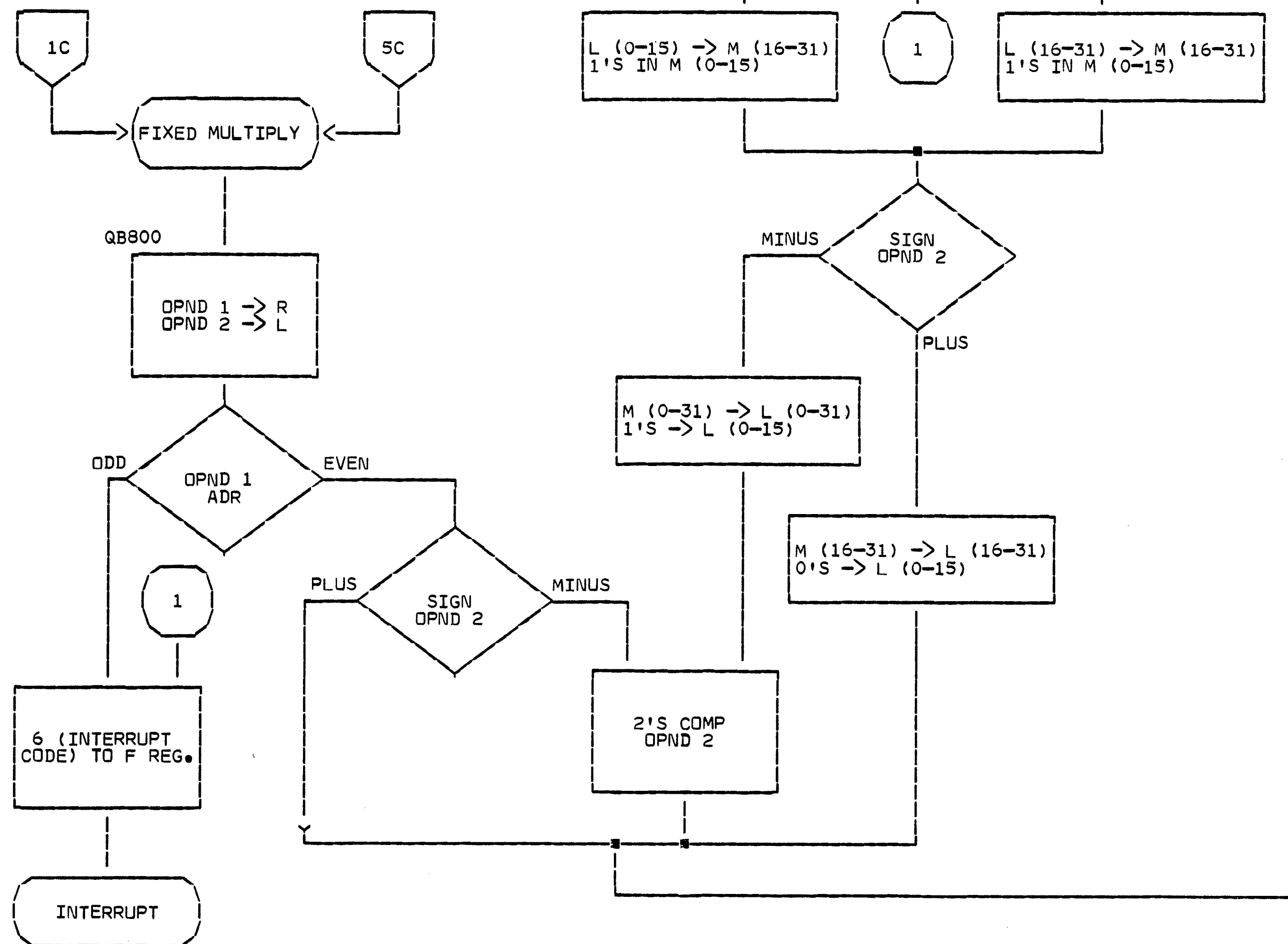
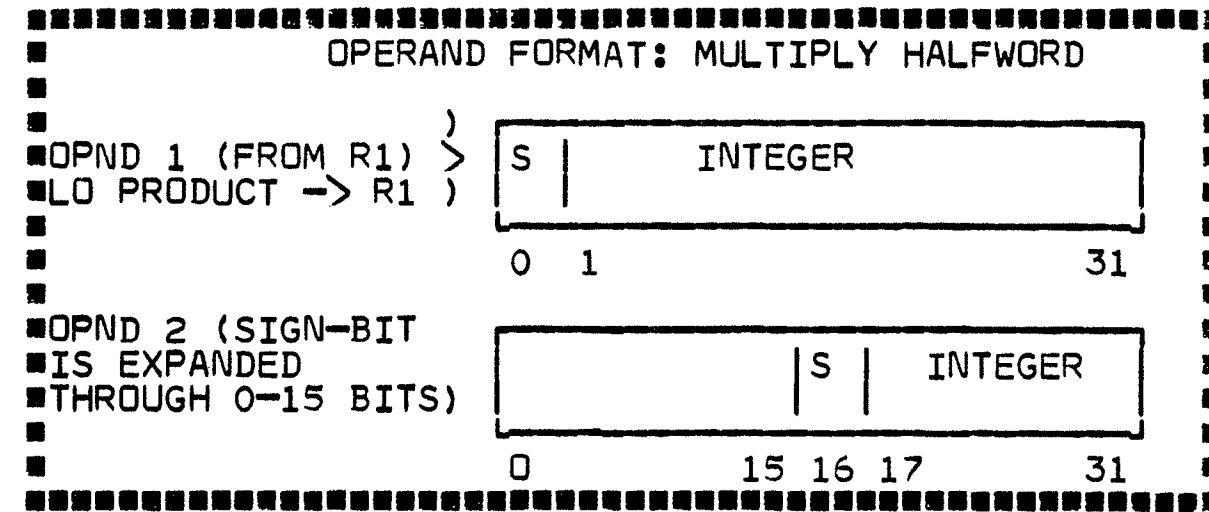
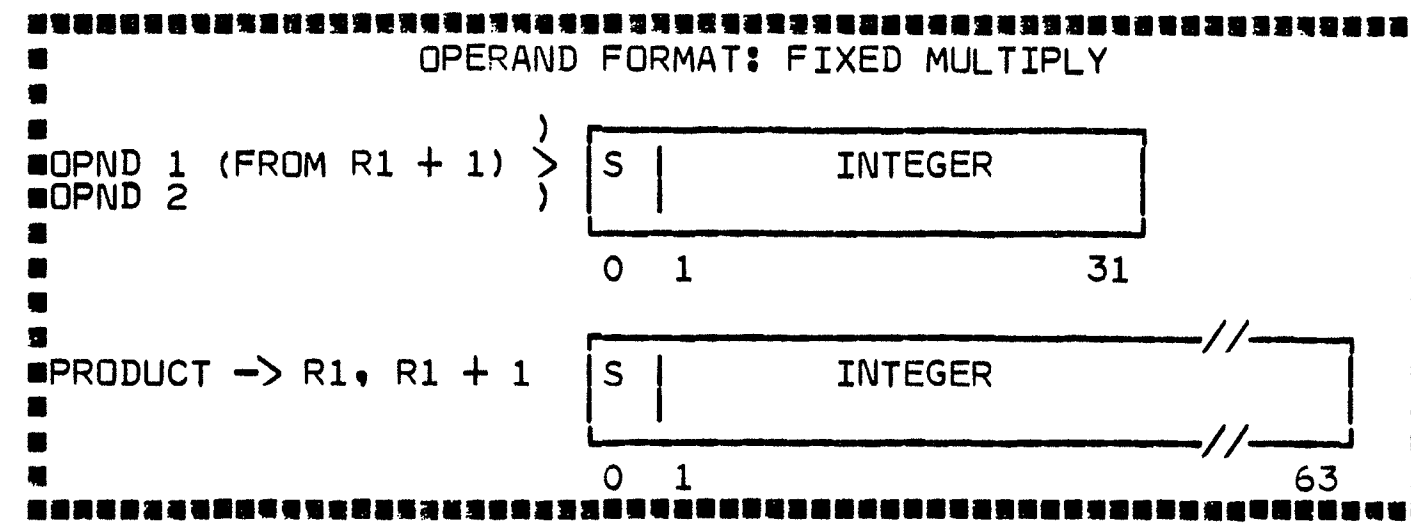
DOUBLEWORD ROUTINE (MB = 0)

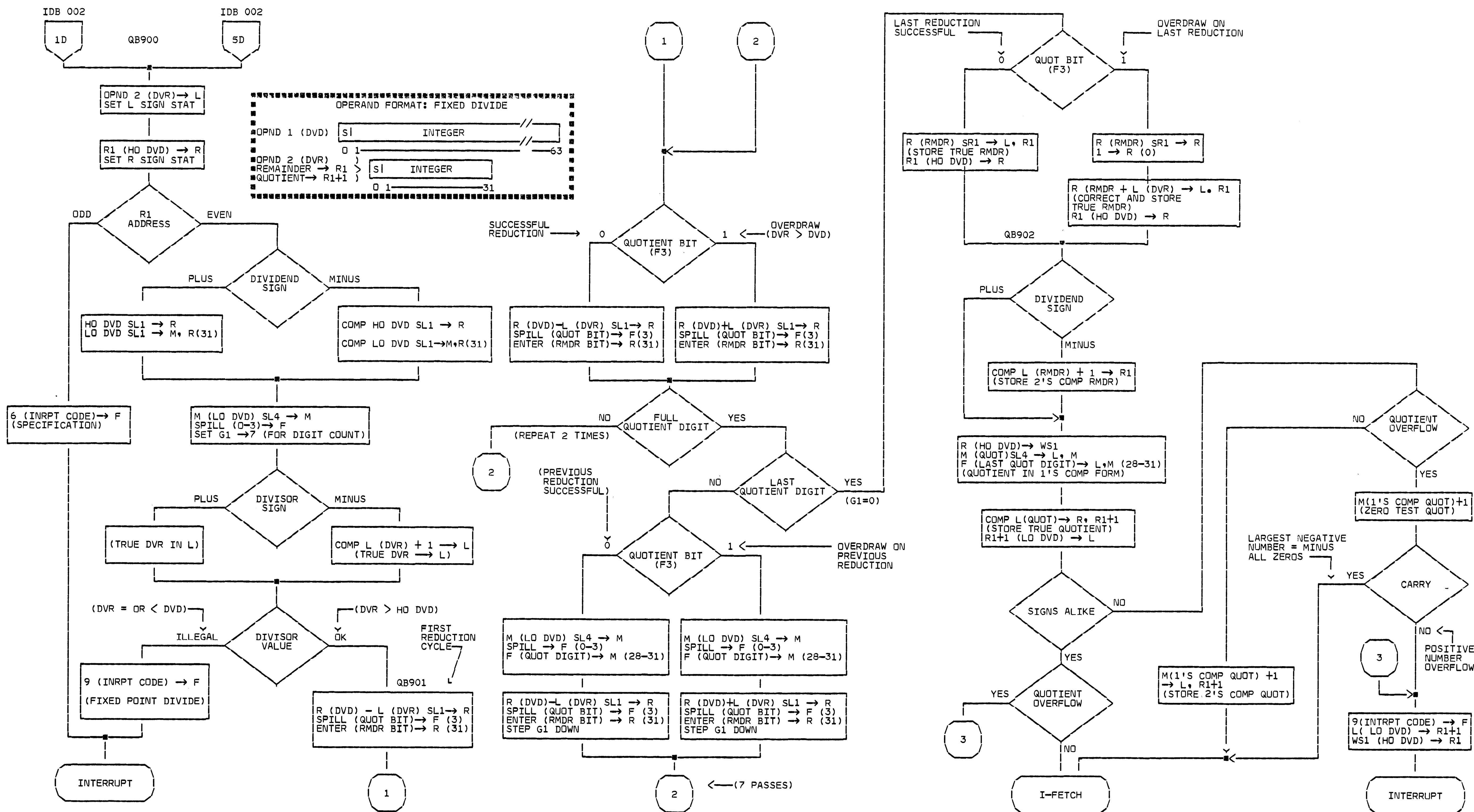
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CONVERT TO BINARY (1 OF 2)  
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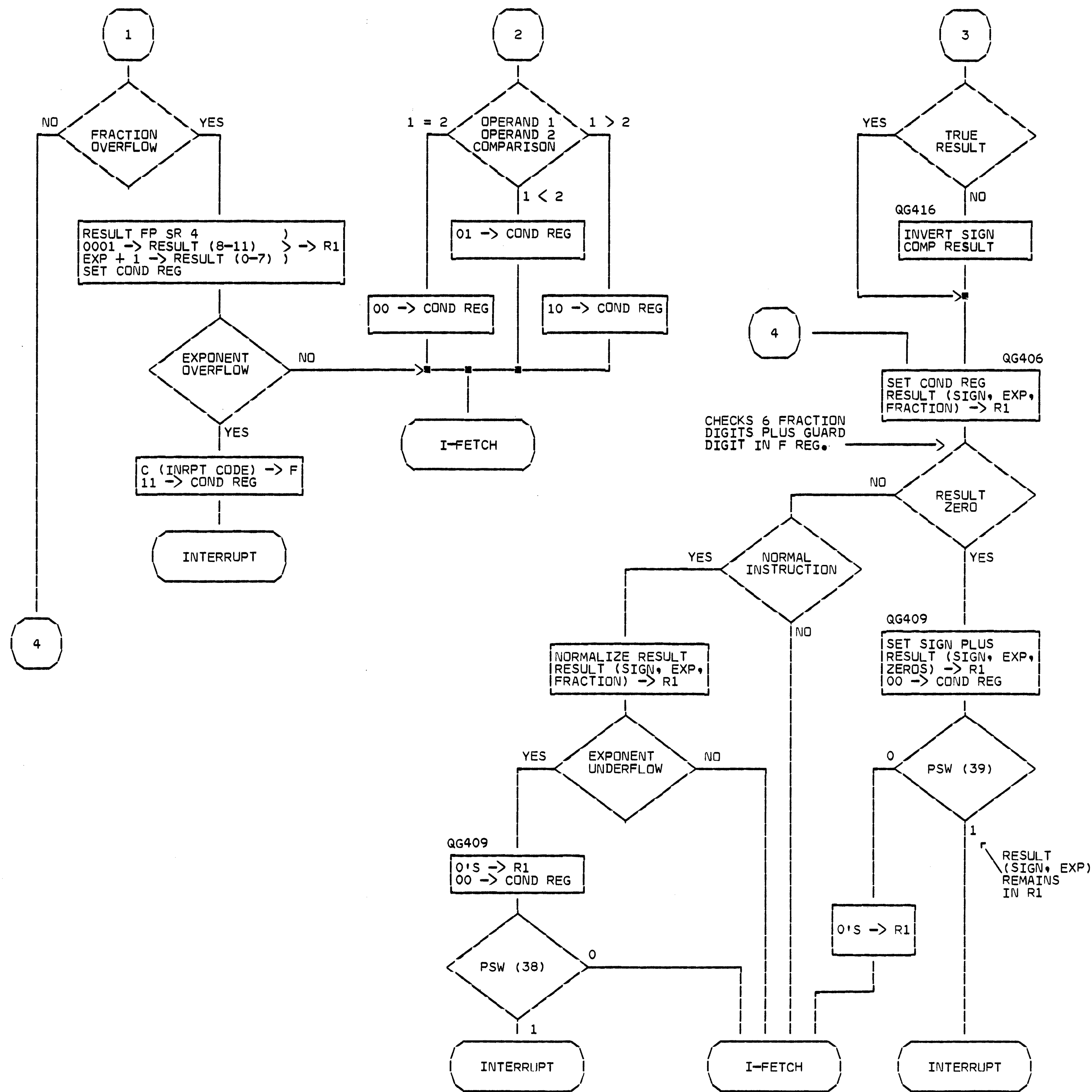
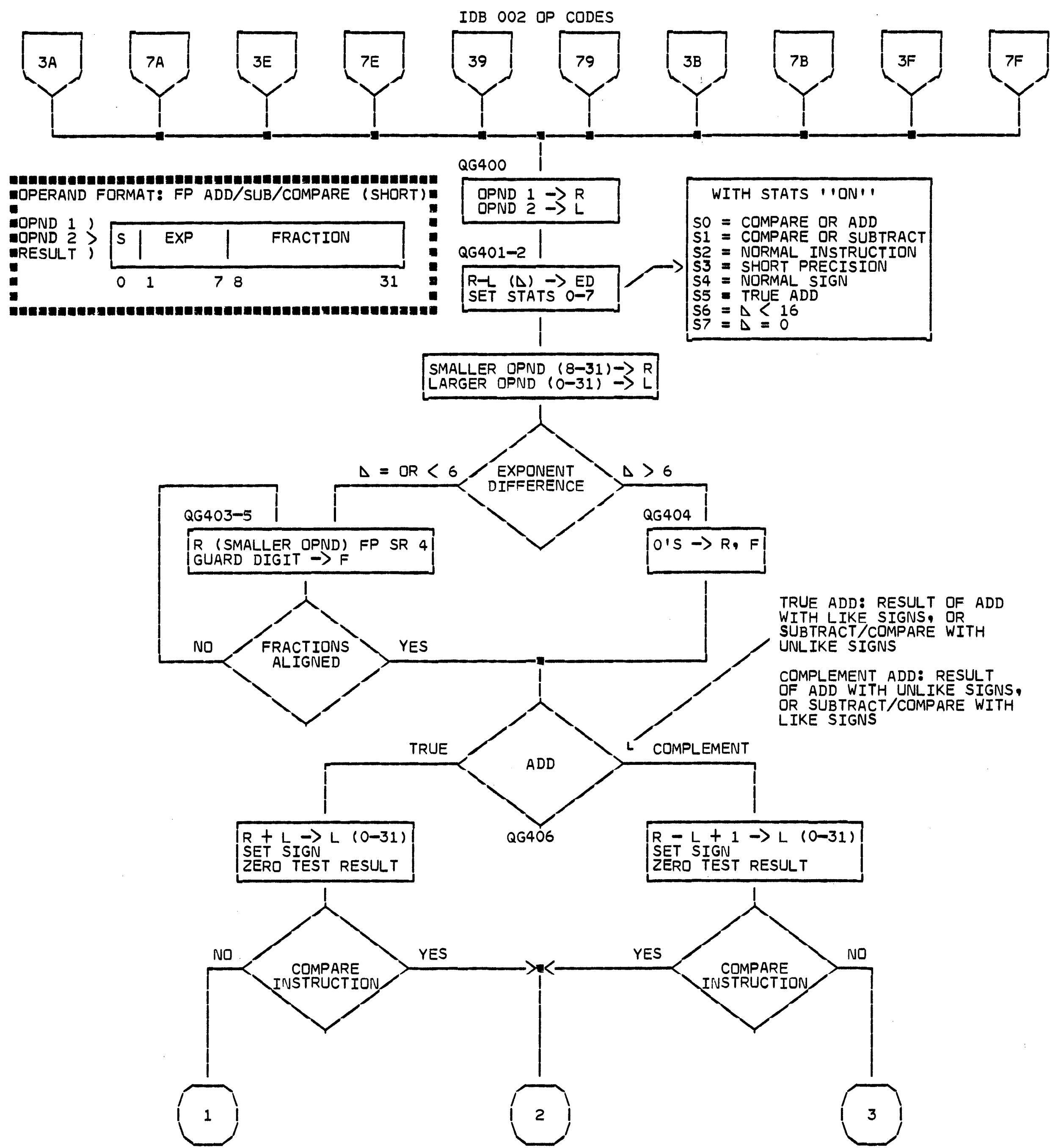


CL112

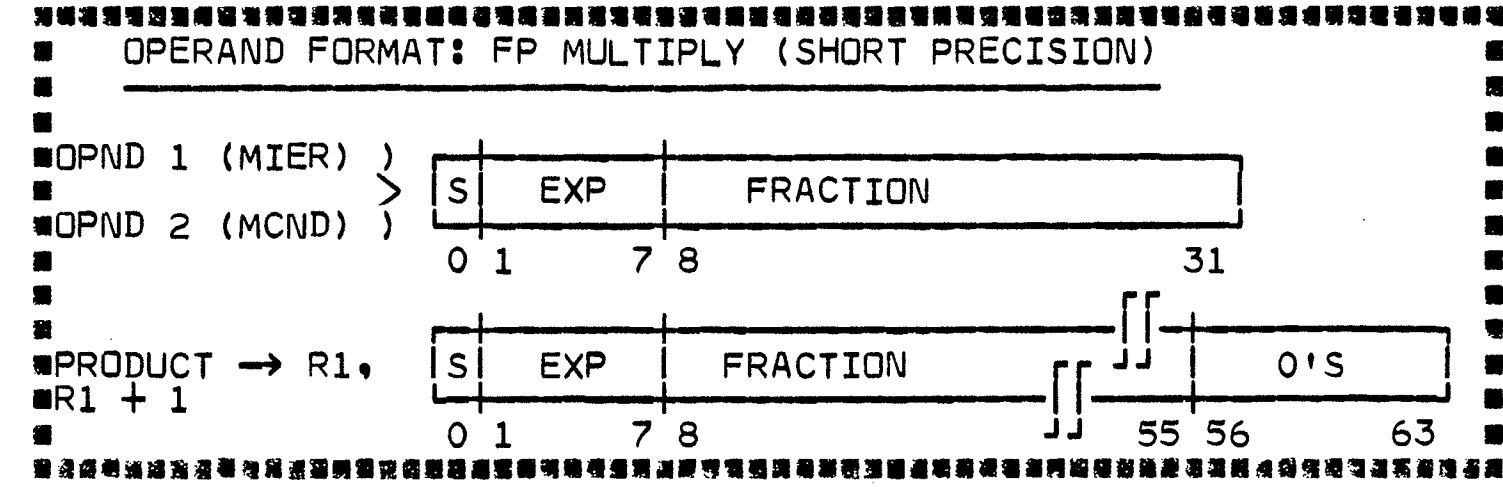
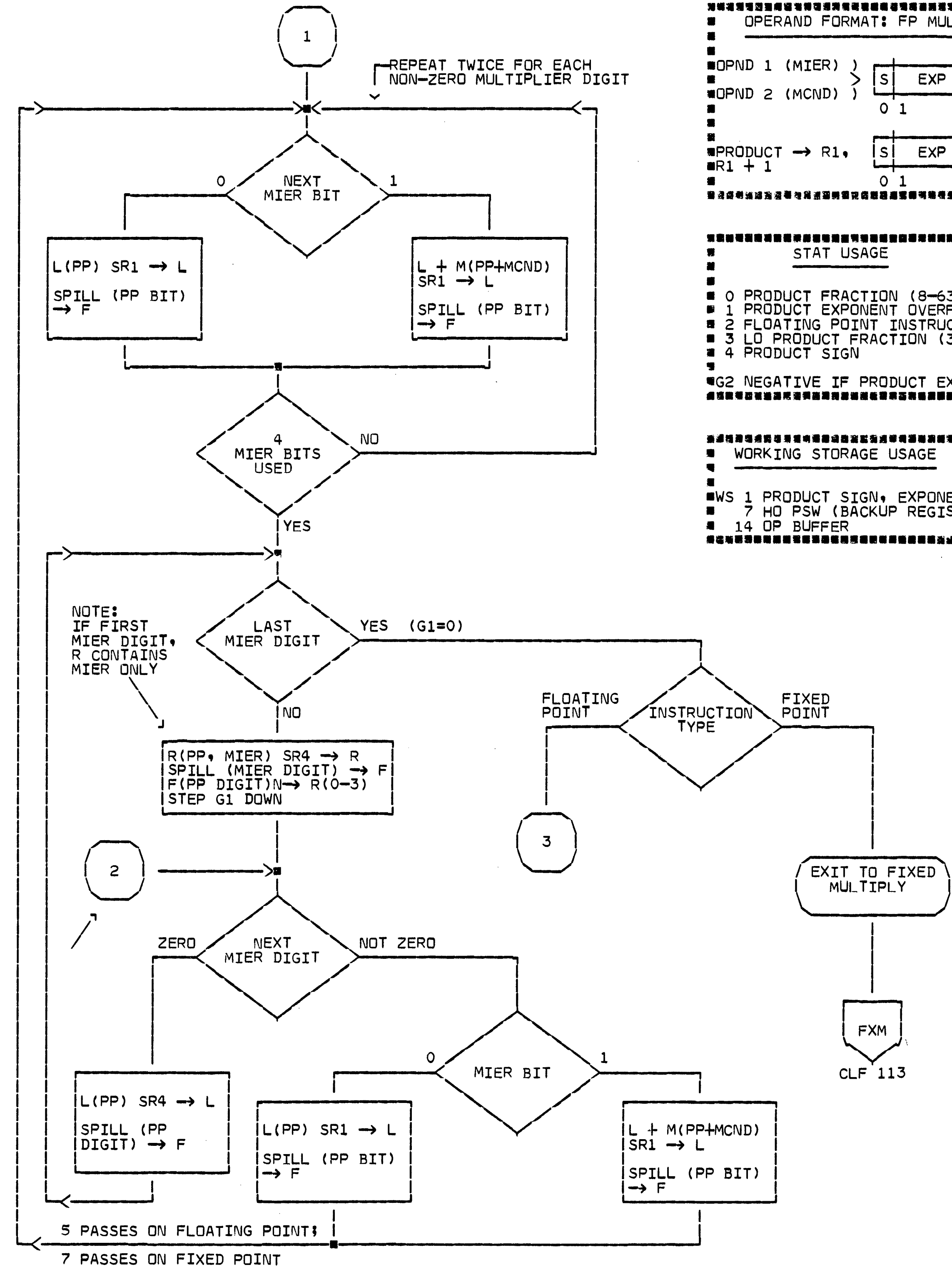
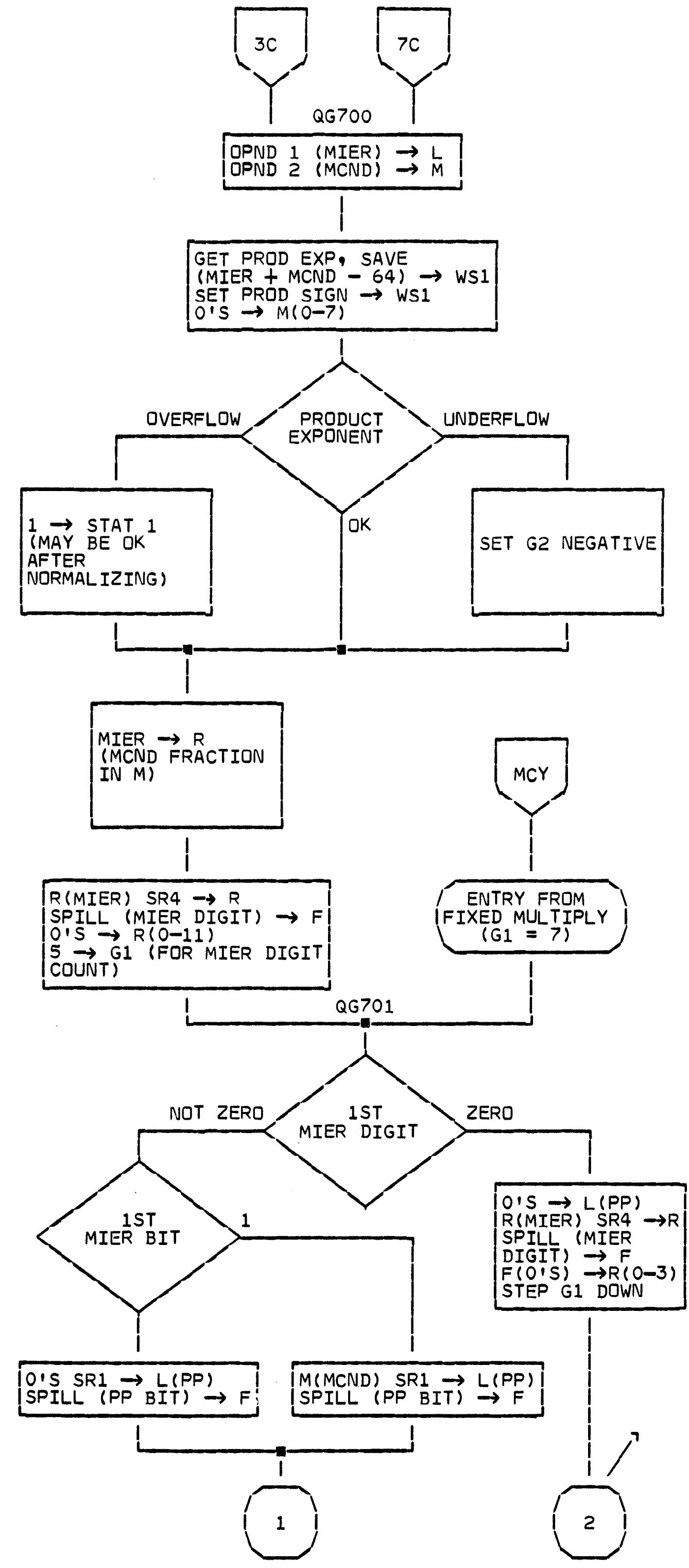




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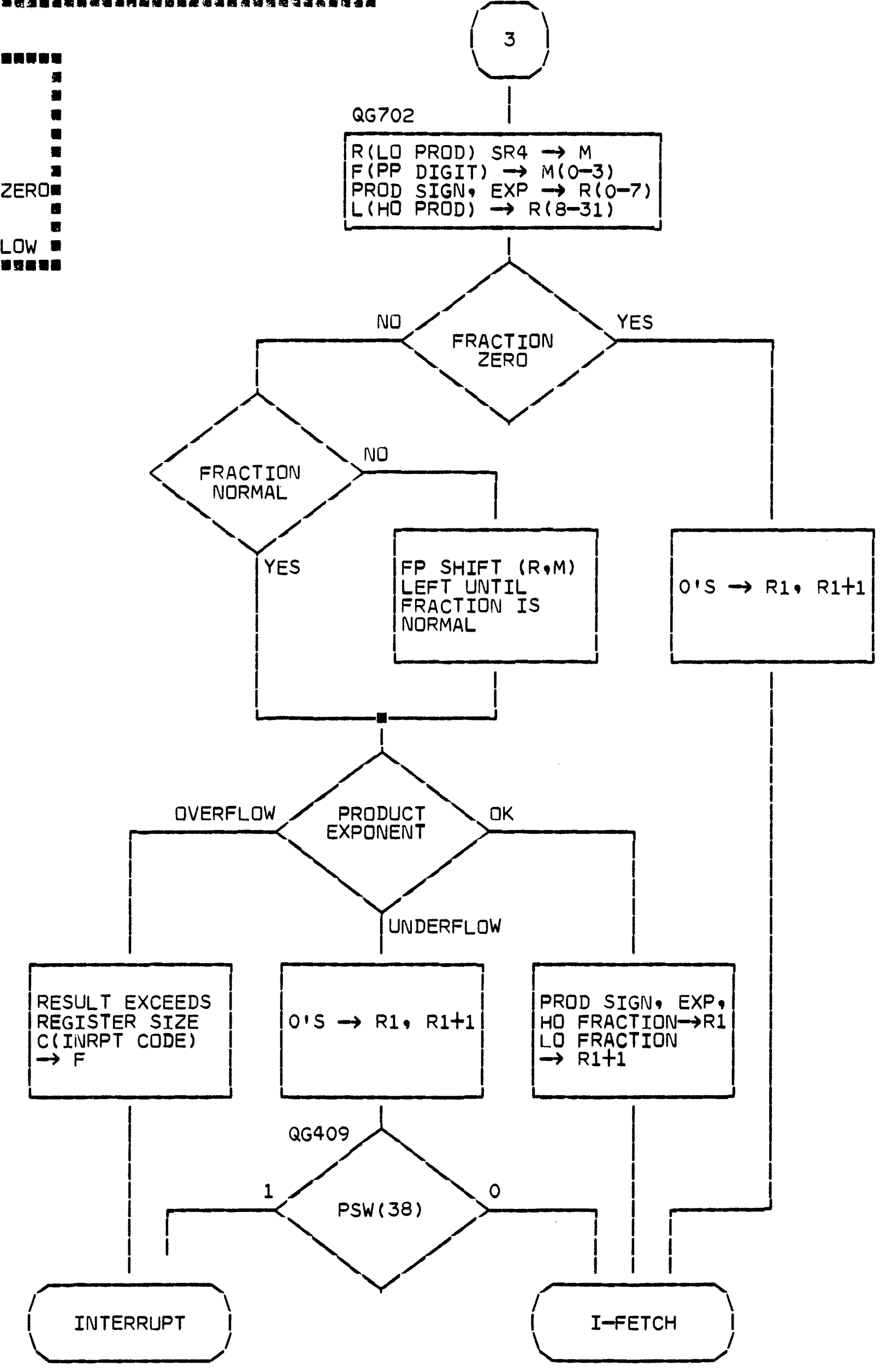


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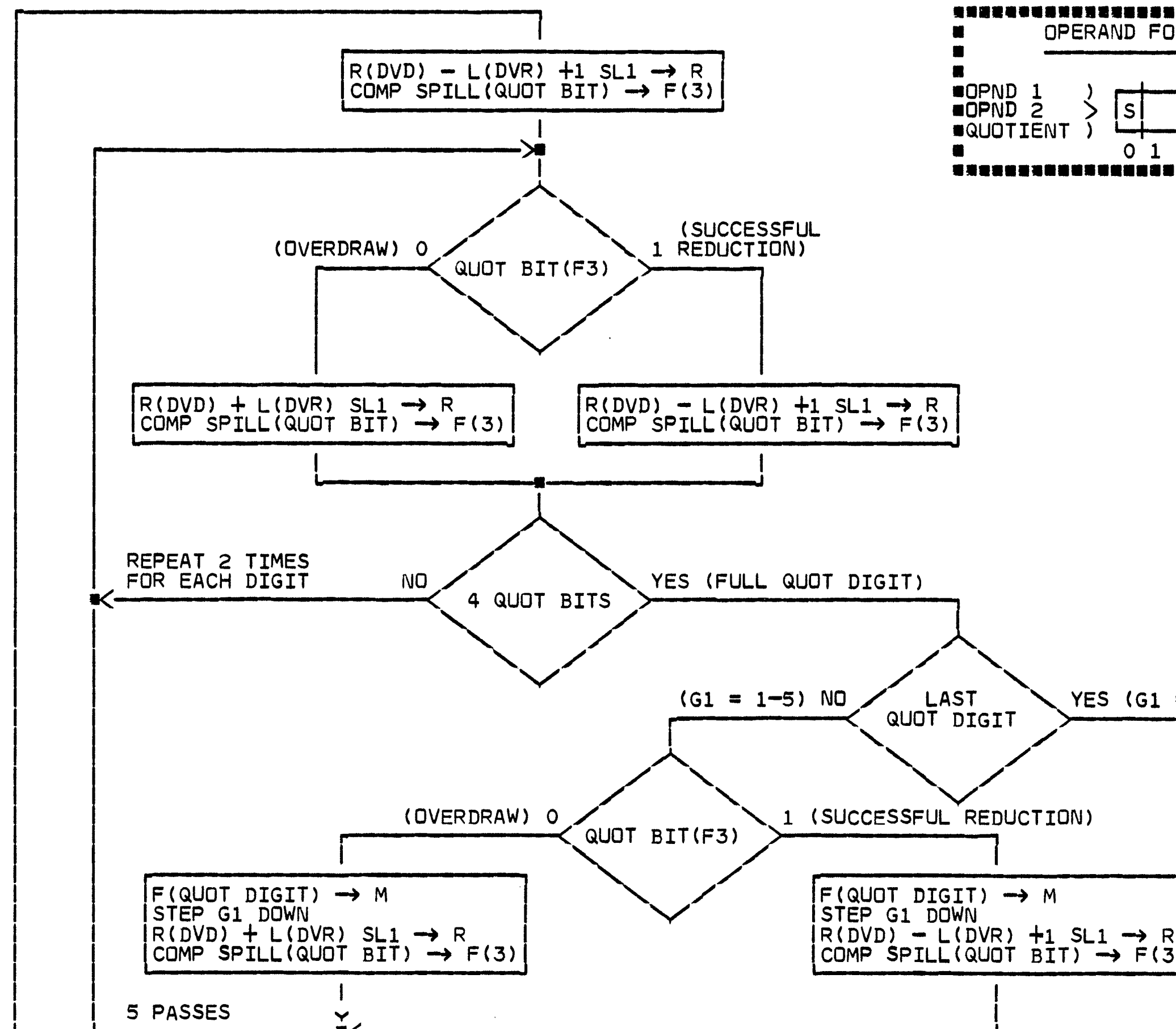
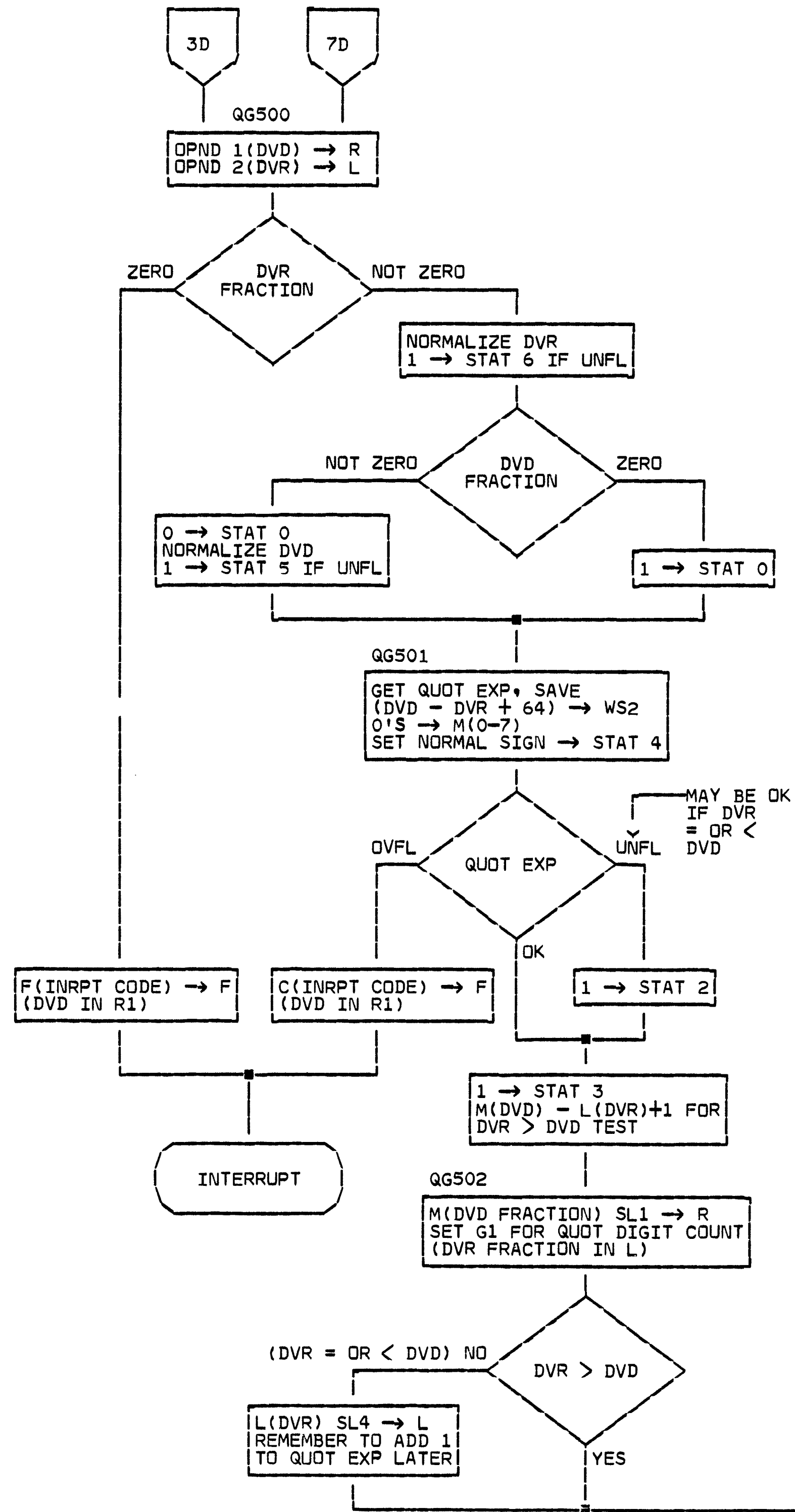
- STAT USAGE
- 0 PRODUCT FRACTION (8-63) = ZERO
  - 1 PRODUCT EXPONENT OVERFLOW
  - 2 FLOATING POINT INSTRUCTION
  - 3 LO PRODUCT FRACTION (32-63) = ZERO
  - 4 PRODUCT SIGN
- G2 NEGATIVE IF PRODUCT EXP UNDERFLOW

- WORKING STORAGE USAGE
- WS 1 PRODUCT SIGN, EXPONENT
  - 7 HD PSW (BACKUP REGISTER)
  - 14 OP BUFFER

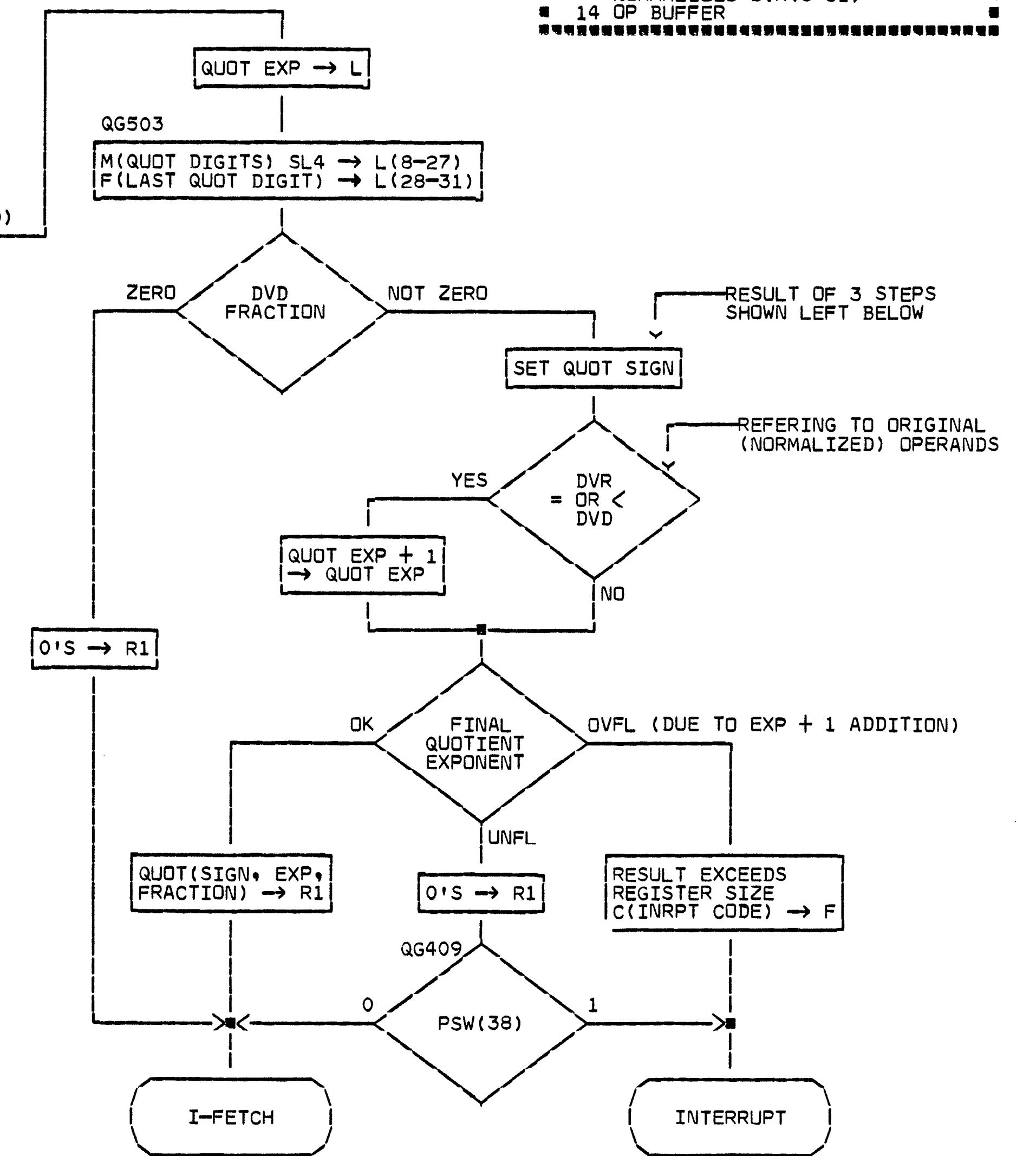
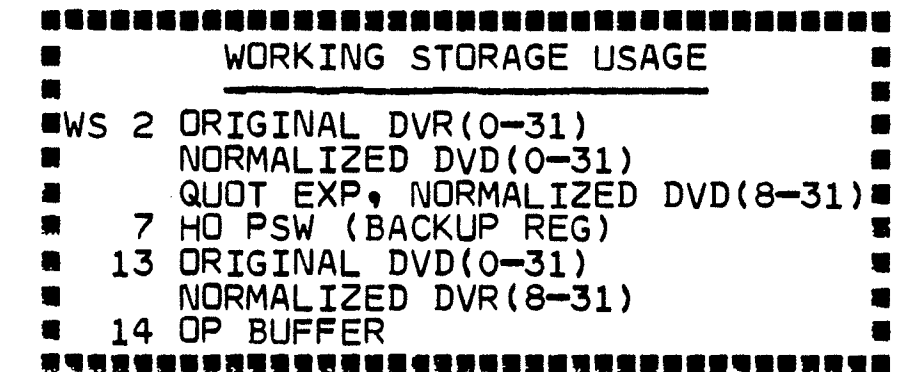
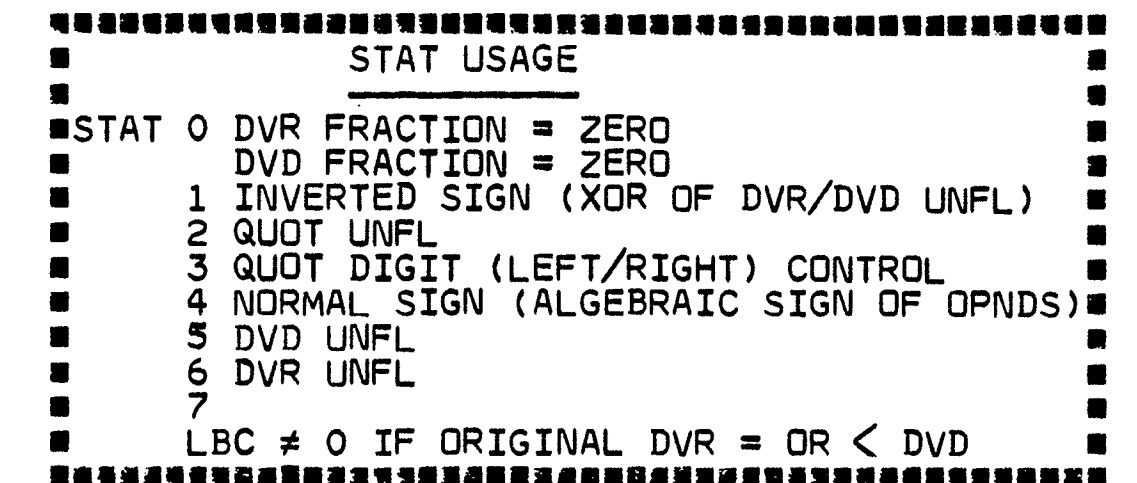
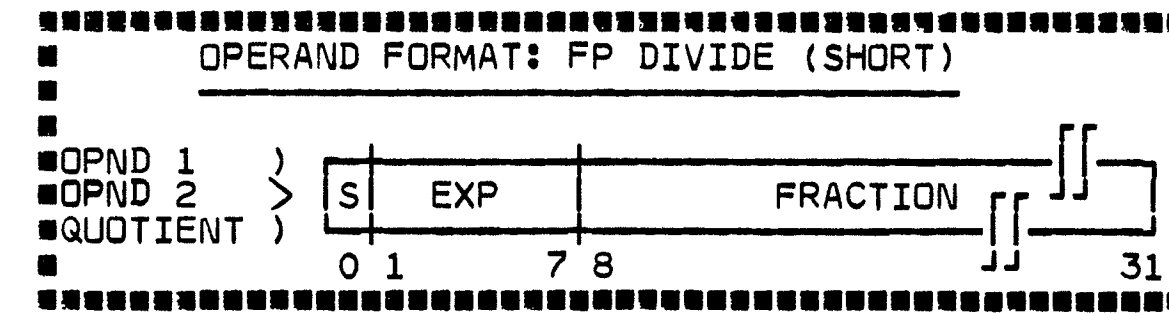
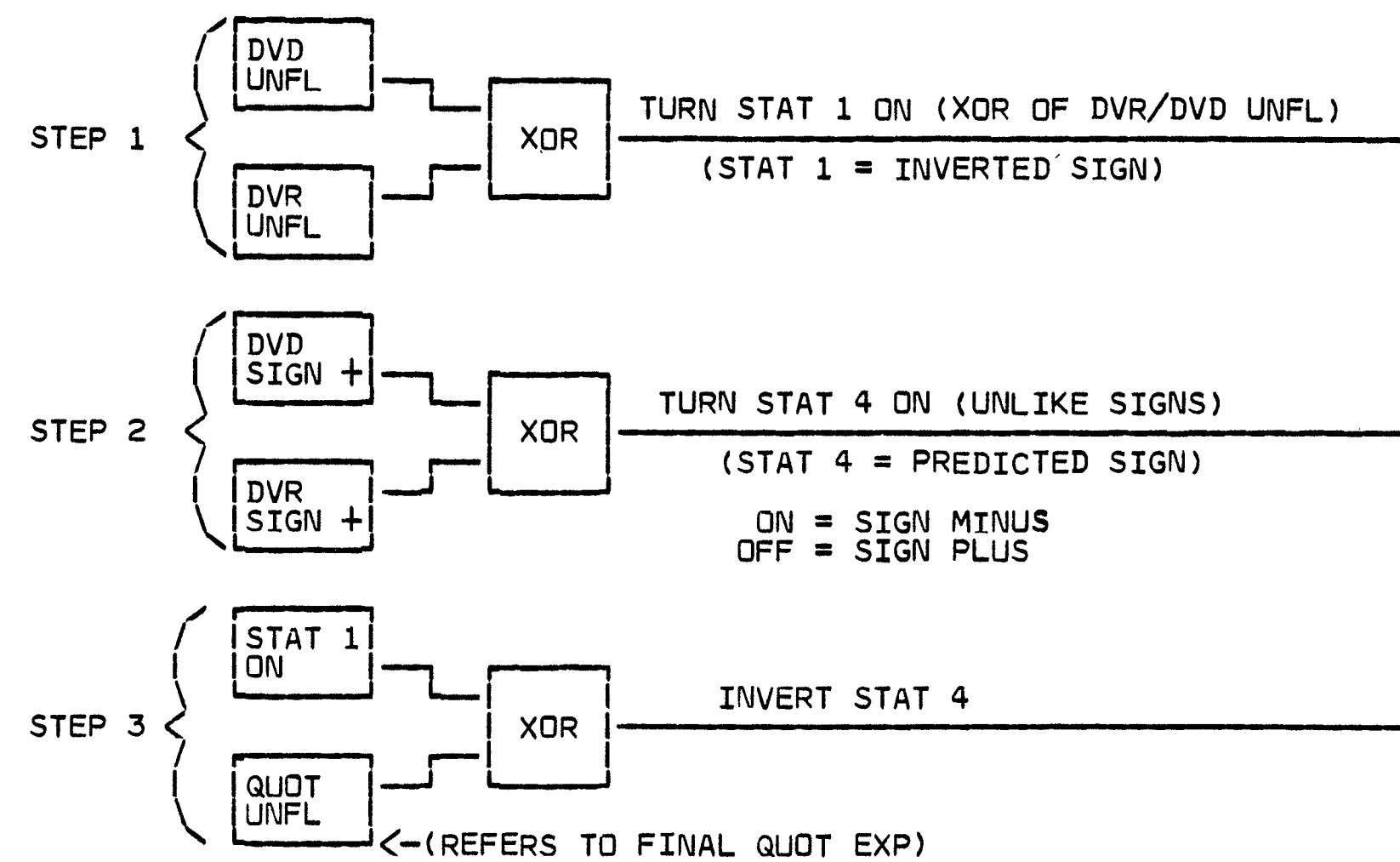


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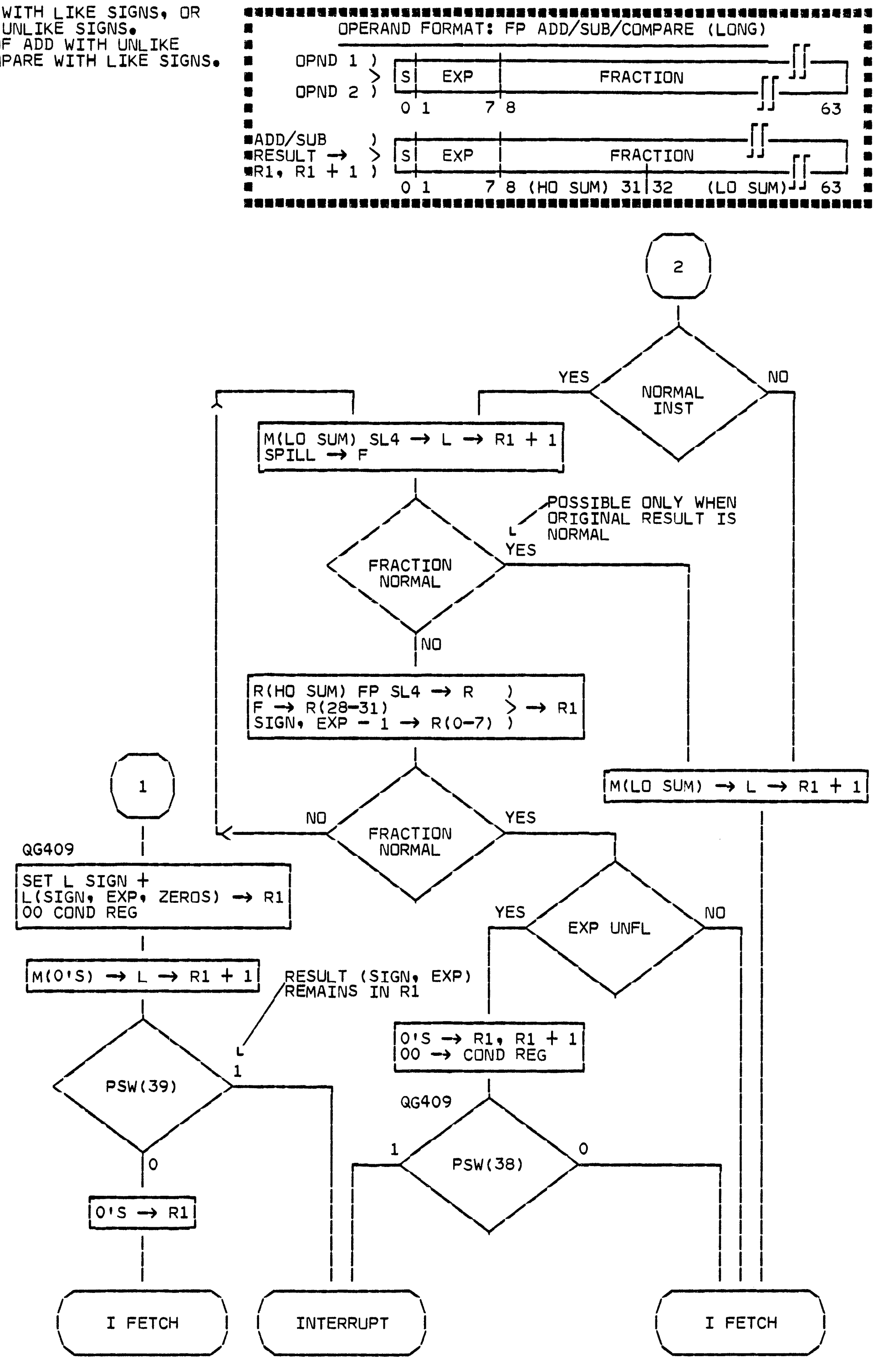
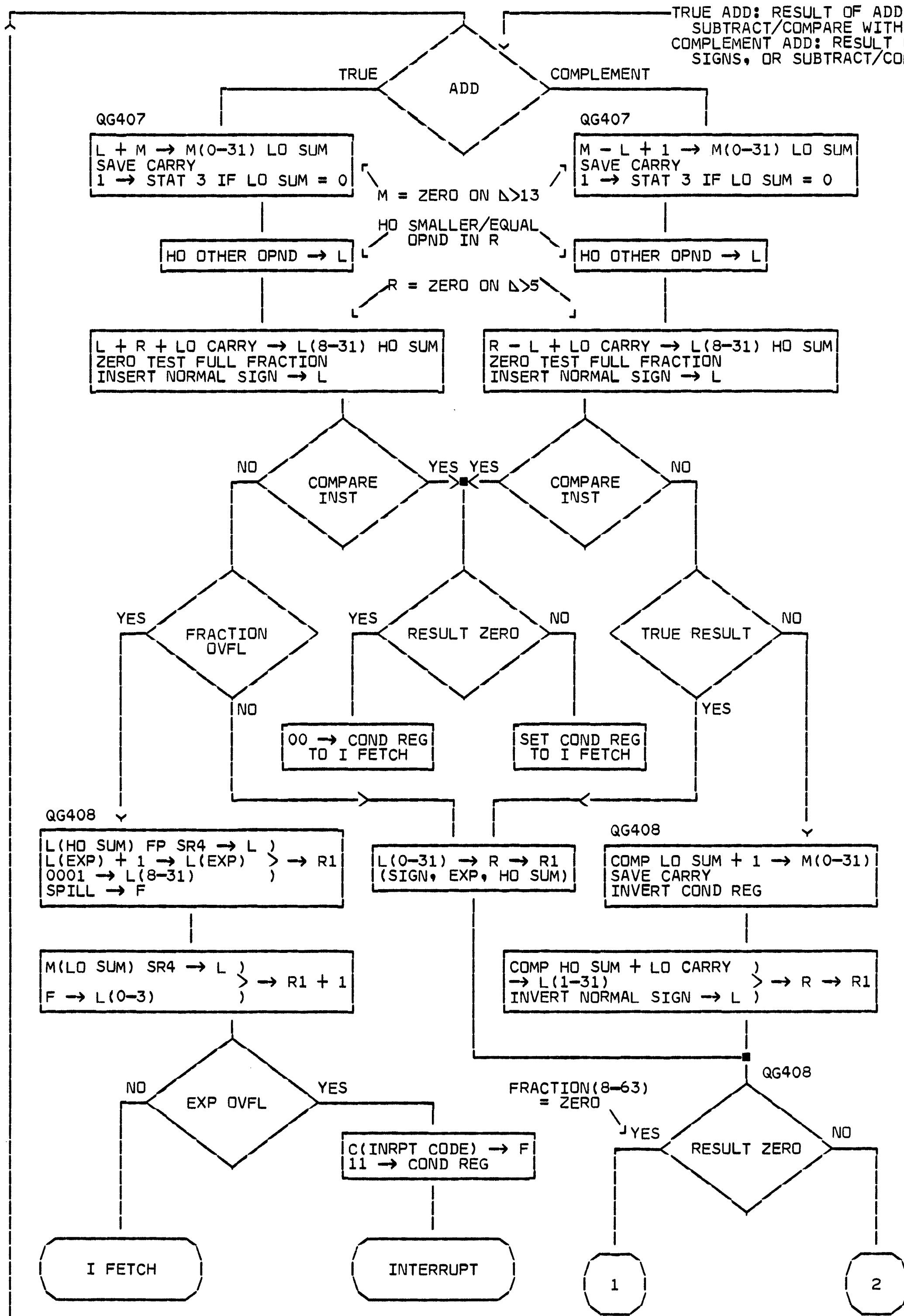
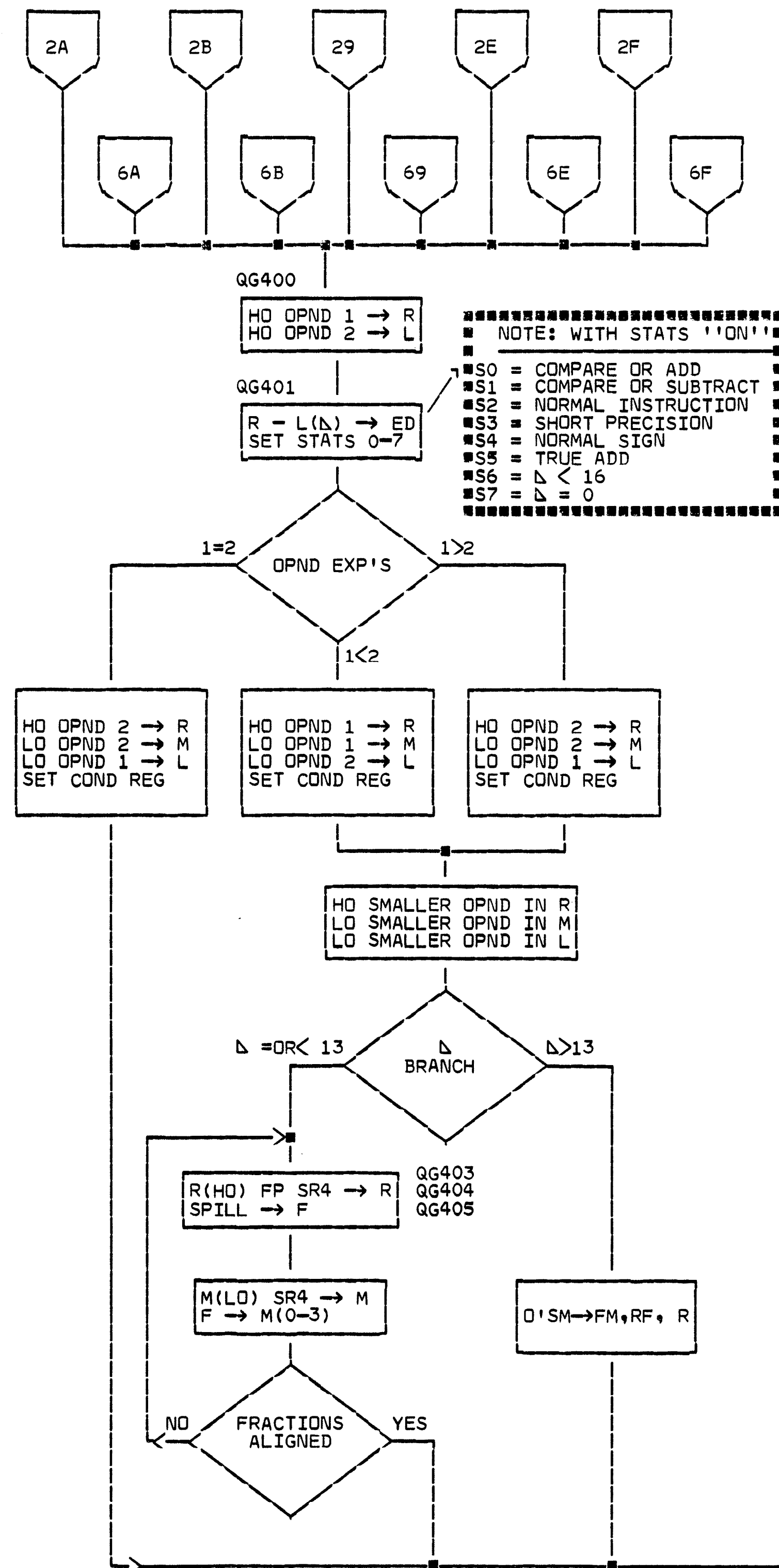
C  
 L  
 1  
 1  
 6

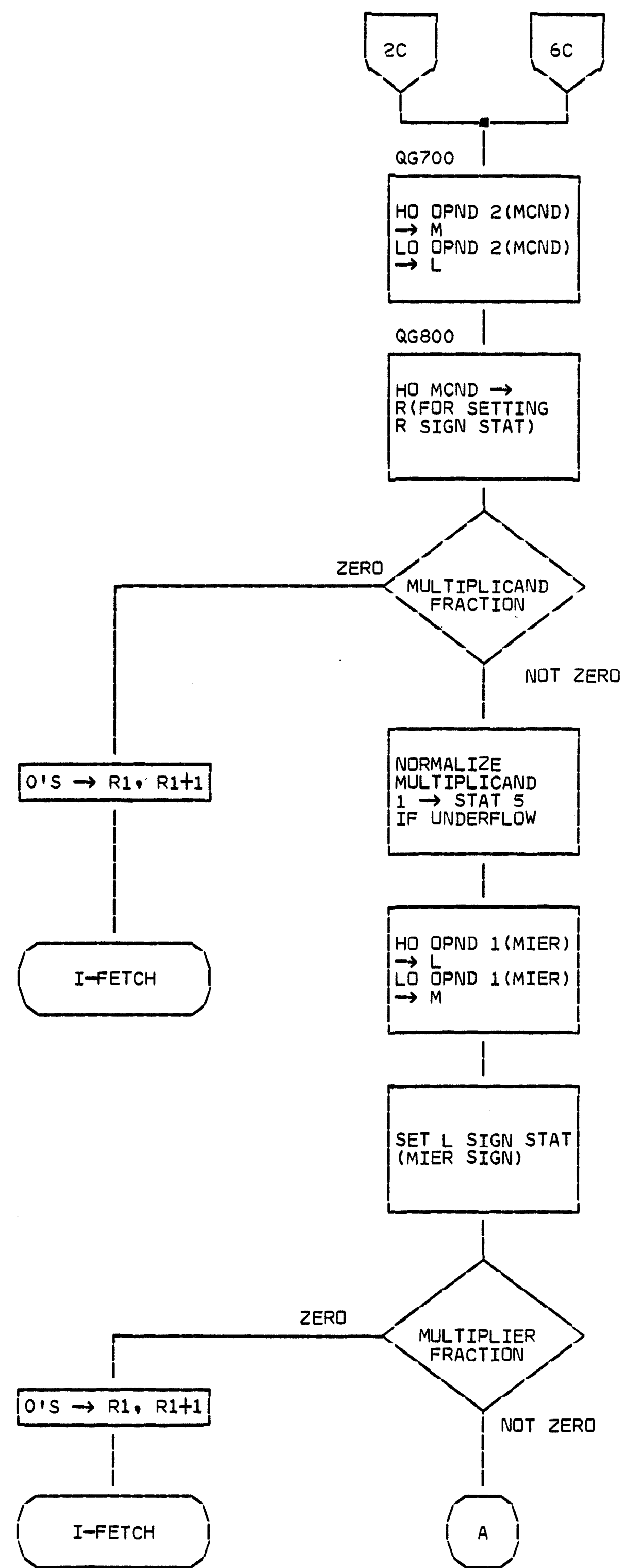


DETERMINING FINAL QUOTIENT SIGN (3 STEPS)

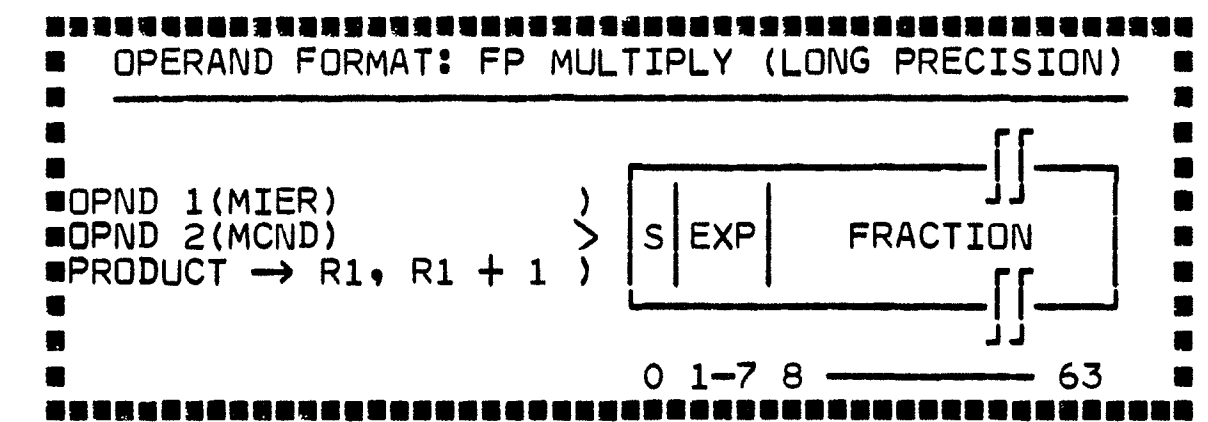
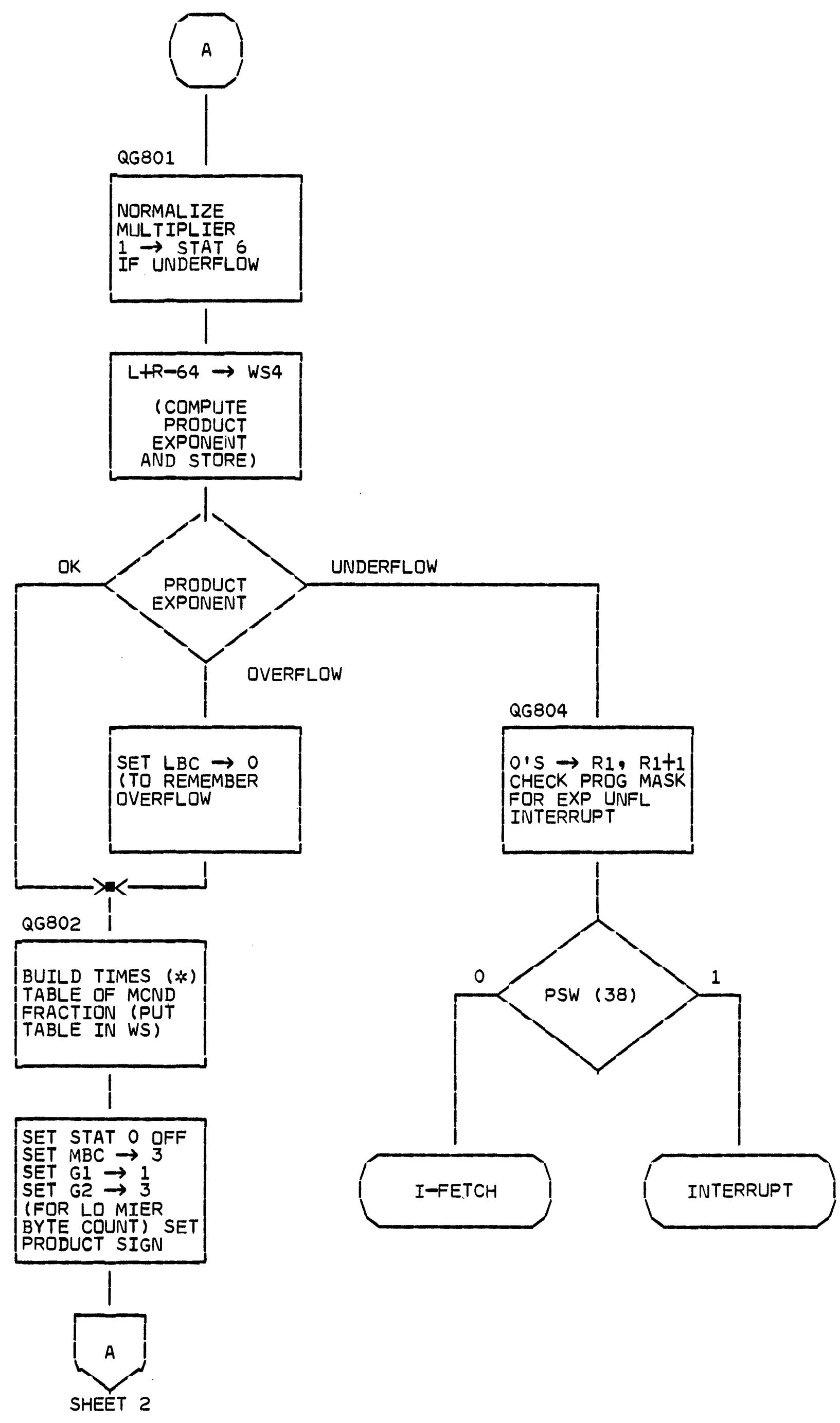








1\* = NORMAL MCND  
 2\* = NORMAL MCND SL1  
 6\* = (1\* + 2\*) SL1

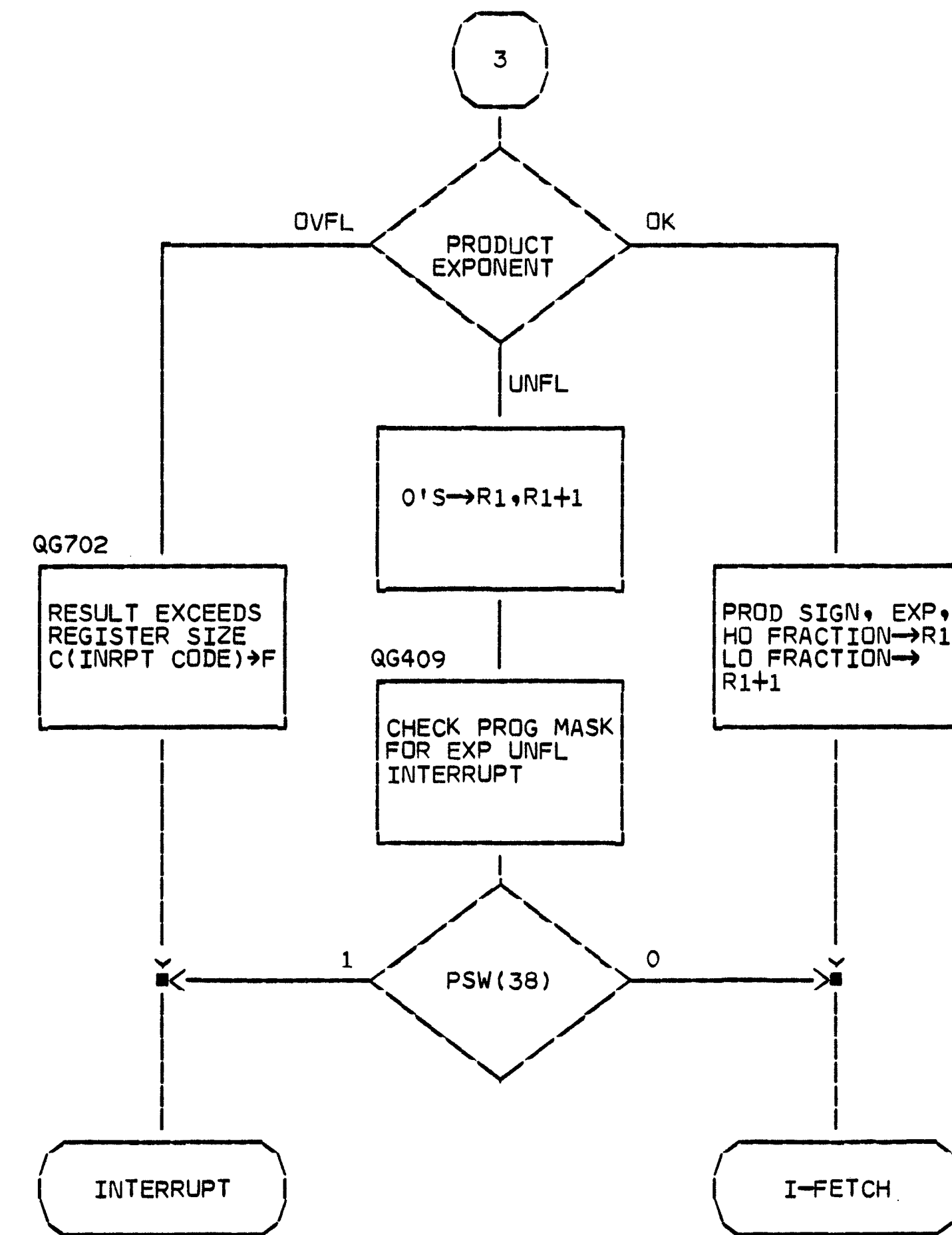
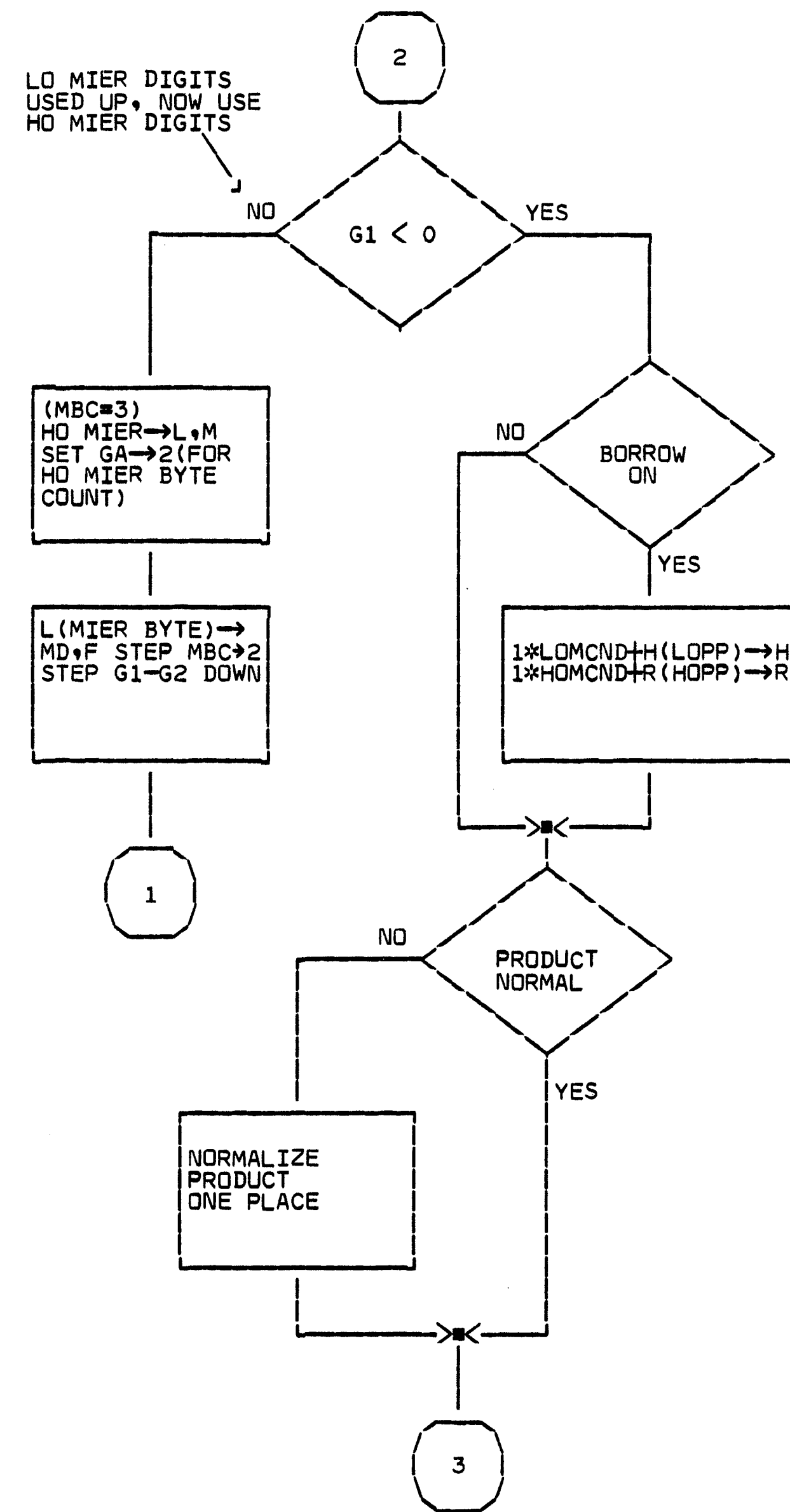
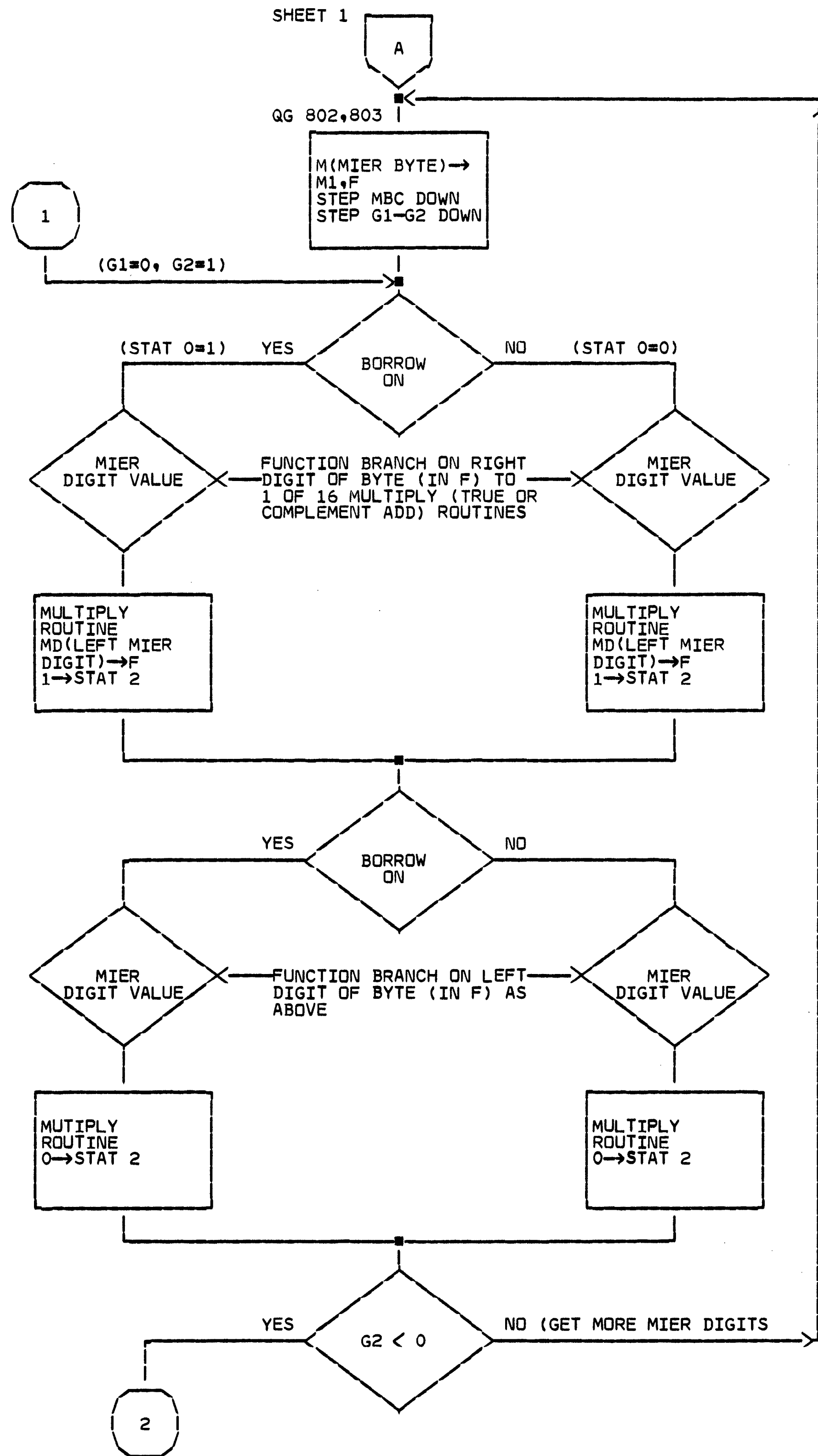


- WORKING STORAGE USAGE
- WS 0-R1 ADR (IN 8-11)
  - 1-LO 6\* MCND
  - 2-HO 6\* MCND
  - 3-HO MIER
  - 4-PRODUCT EXPONENT, HO MCND
  - 5-
  - 6-
  - 7-HO PSW BACKUP REGISTER
  - 8-LO 2\* MCND
  - 9-HO 2\* MCND
  - 10-
  - 11-ZERO'S
  - 12-LO 1\* MCND
  - 13-HO 1\* MCND
  - 14-OP BUFFER
  - 15-LO MCND

- STAT USAGE
- STAT 0 (BEFORE MIER PRENORMALIZATION)
    - HO MIER = ZERO (DURING MULTIPLY ROUTINES)
    - BORROW 'ON'
  - STAT 2 MULTIPLY WITH LEFT MIER DIGIT
    - 3 LO MIER = ZERO
    - 4 PRODUCT SIGN
    - 5 MCND UNDERFLOW
    - 6 MIER UNDERFLOW

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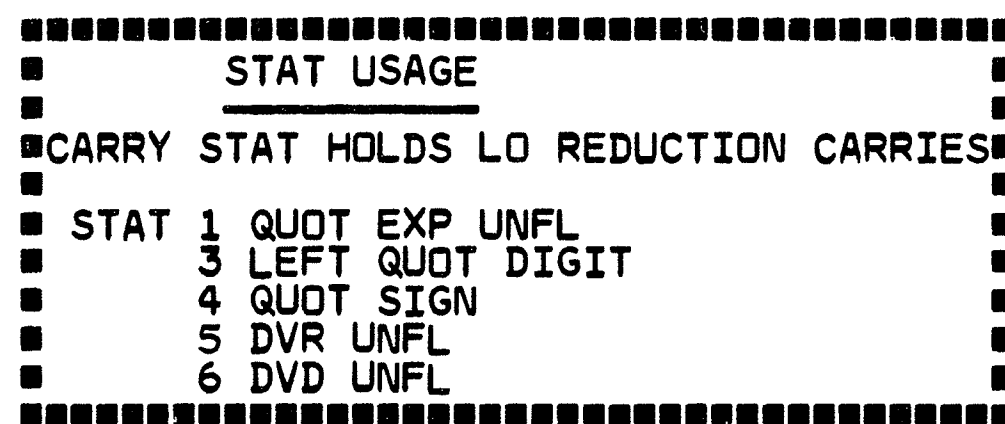
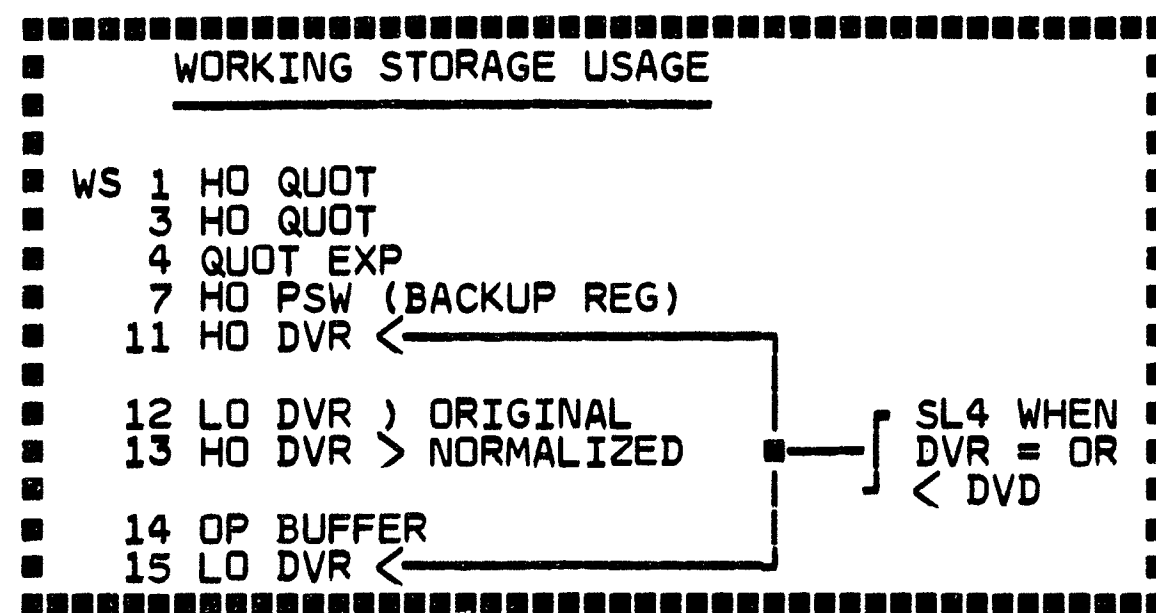
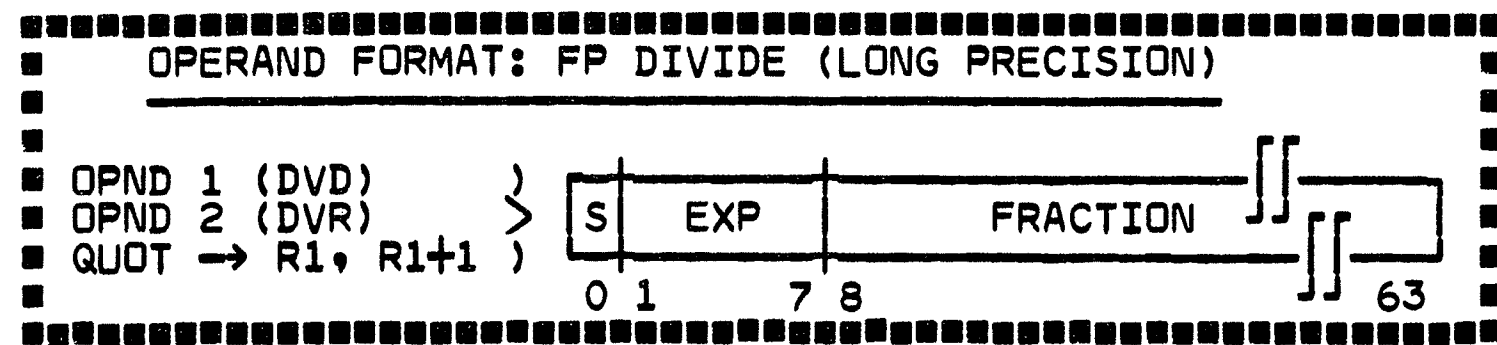
C  
 L  
 1  
 1  
 9



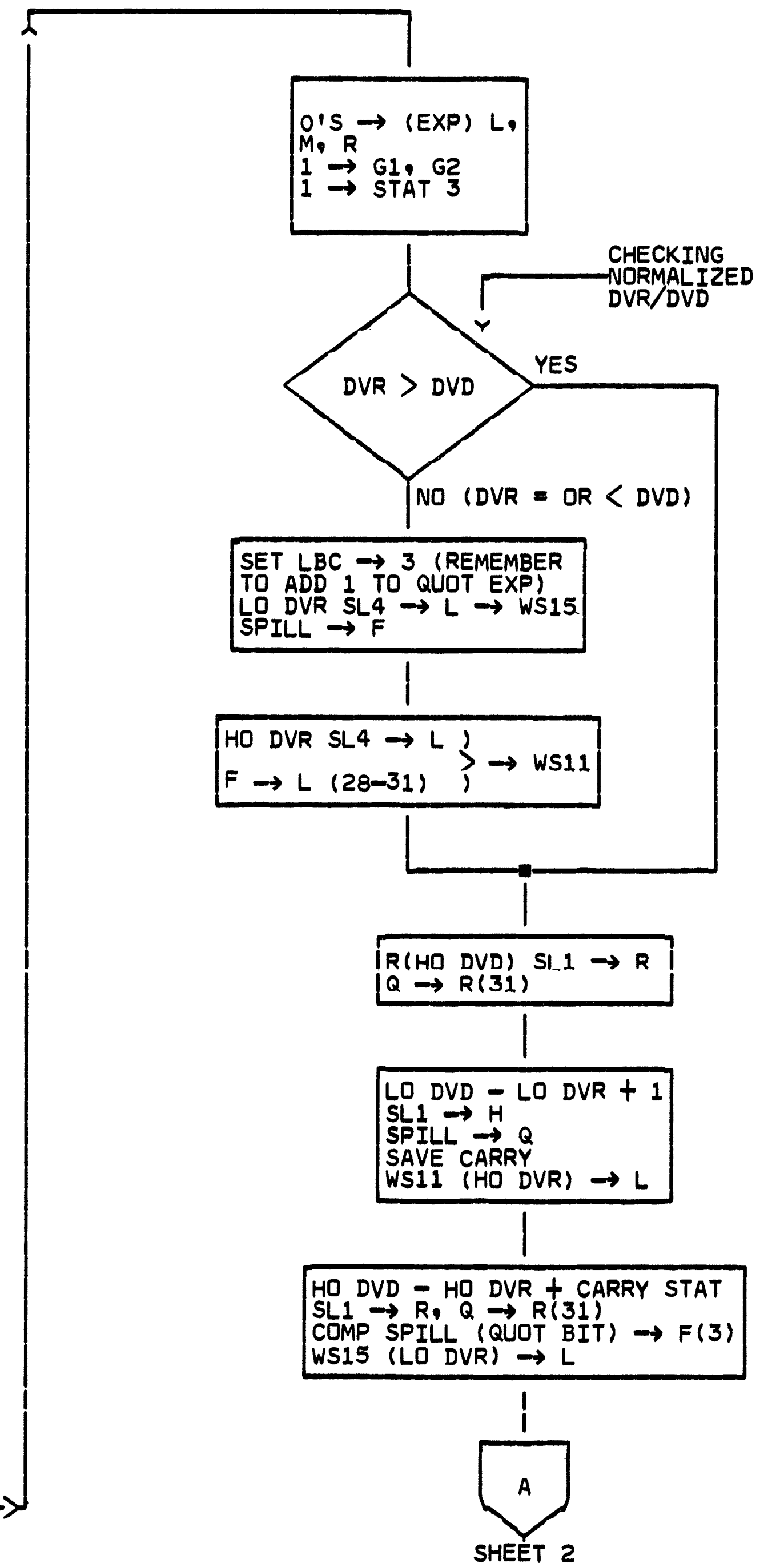
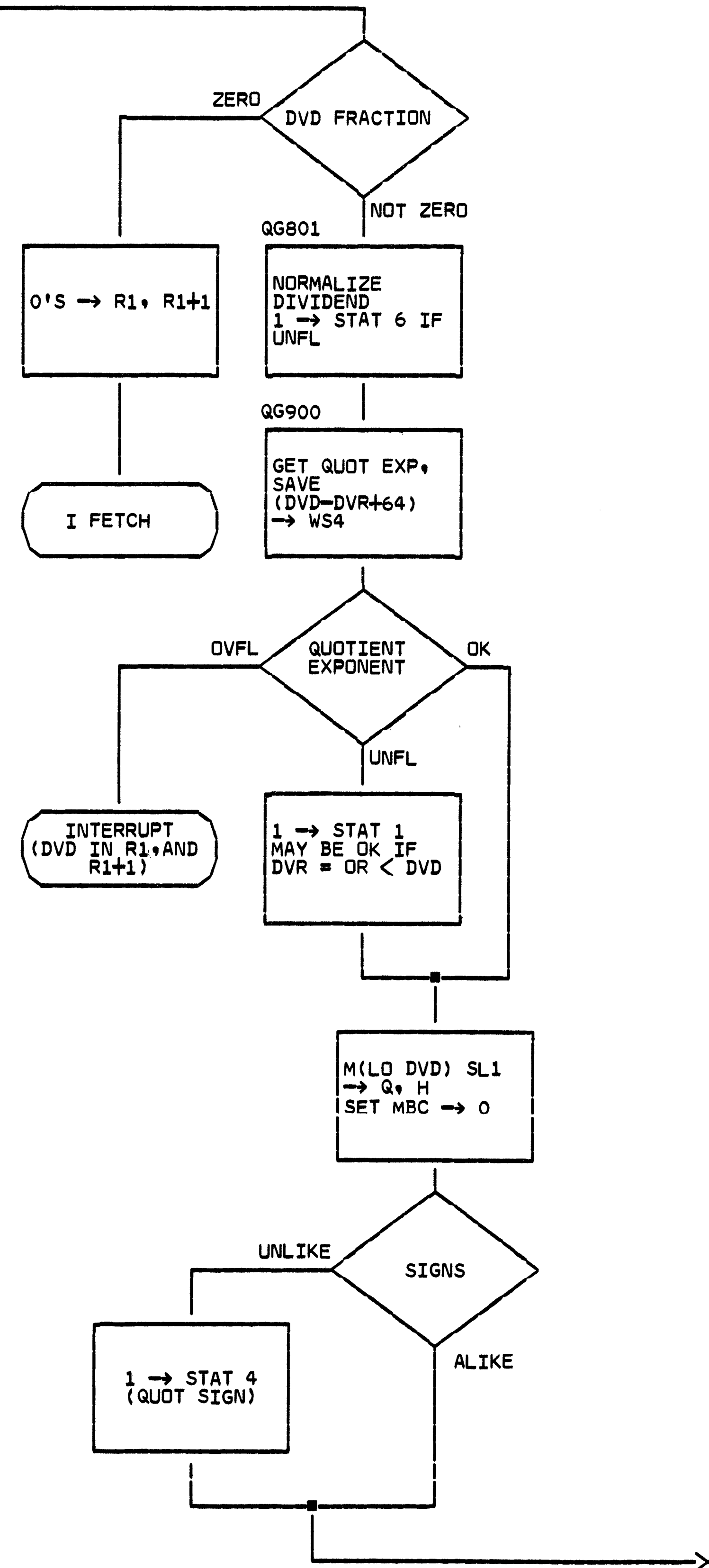
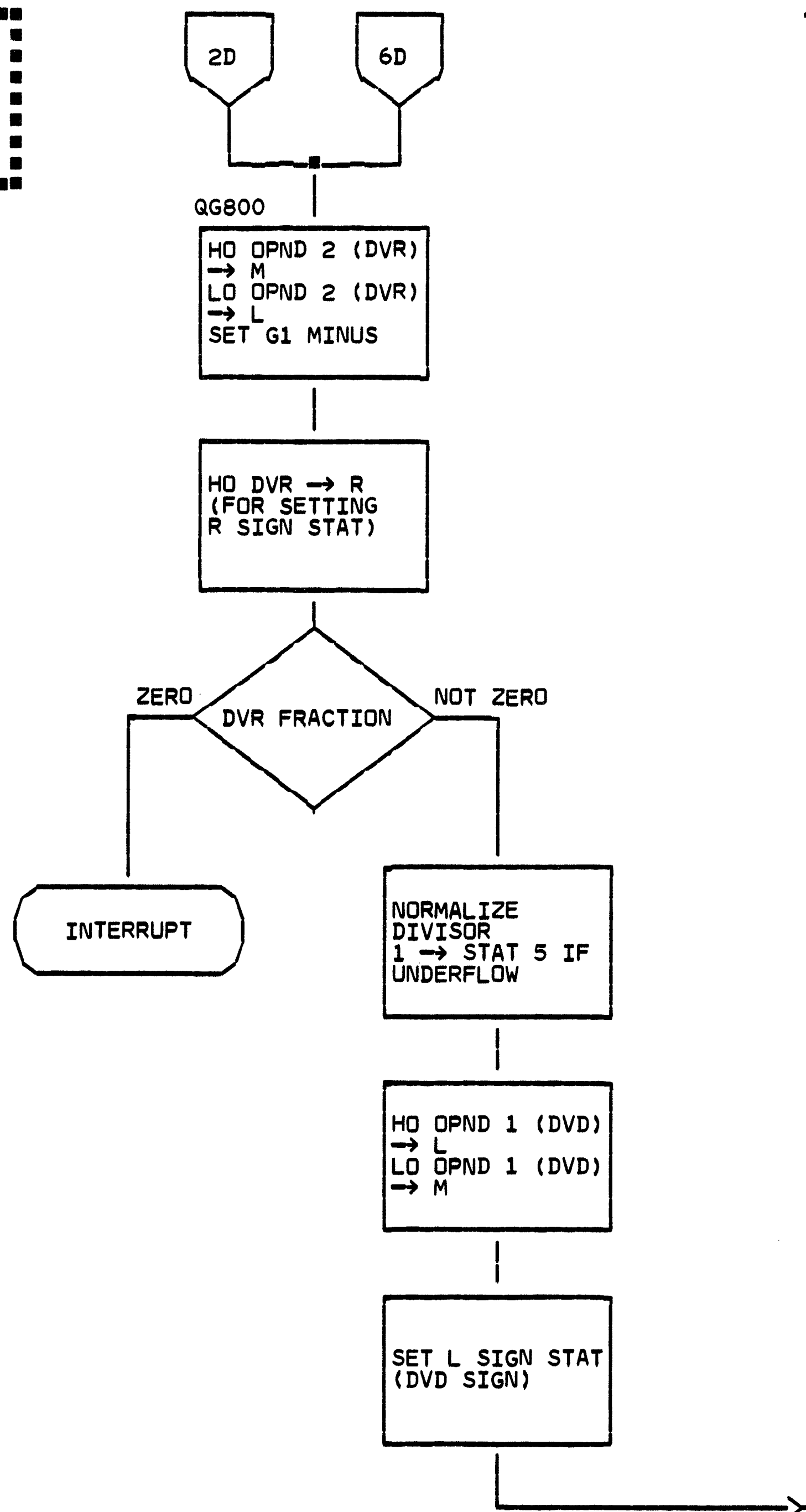
MIER DIGIT VALUES AND RESULTING ROUTINES

MIER DIGIT	BORROW OFF	BORROW ON
0	- - - -	+1
1	+1	+2
2	+2	+1, +2
3	+1, +2	+6, -2
4	+6, -2	+6, -1
5	+6, -1	+6
6	+6	+6, +1
7	+6, +1	+6, +2
8	+6, +2	+6, -1, B
9	+6, -1, B	+6, B
10	+6, B	+6, +1, B
11	+6, +1, B	+6, +2, B
12	+6, +2, B	+2, -1, B
13	+2, -1, B	-2, B
14	-2, B	-1, B
15	-1, B	B

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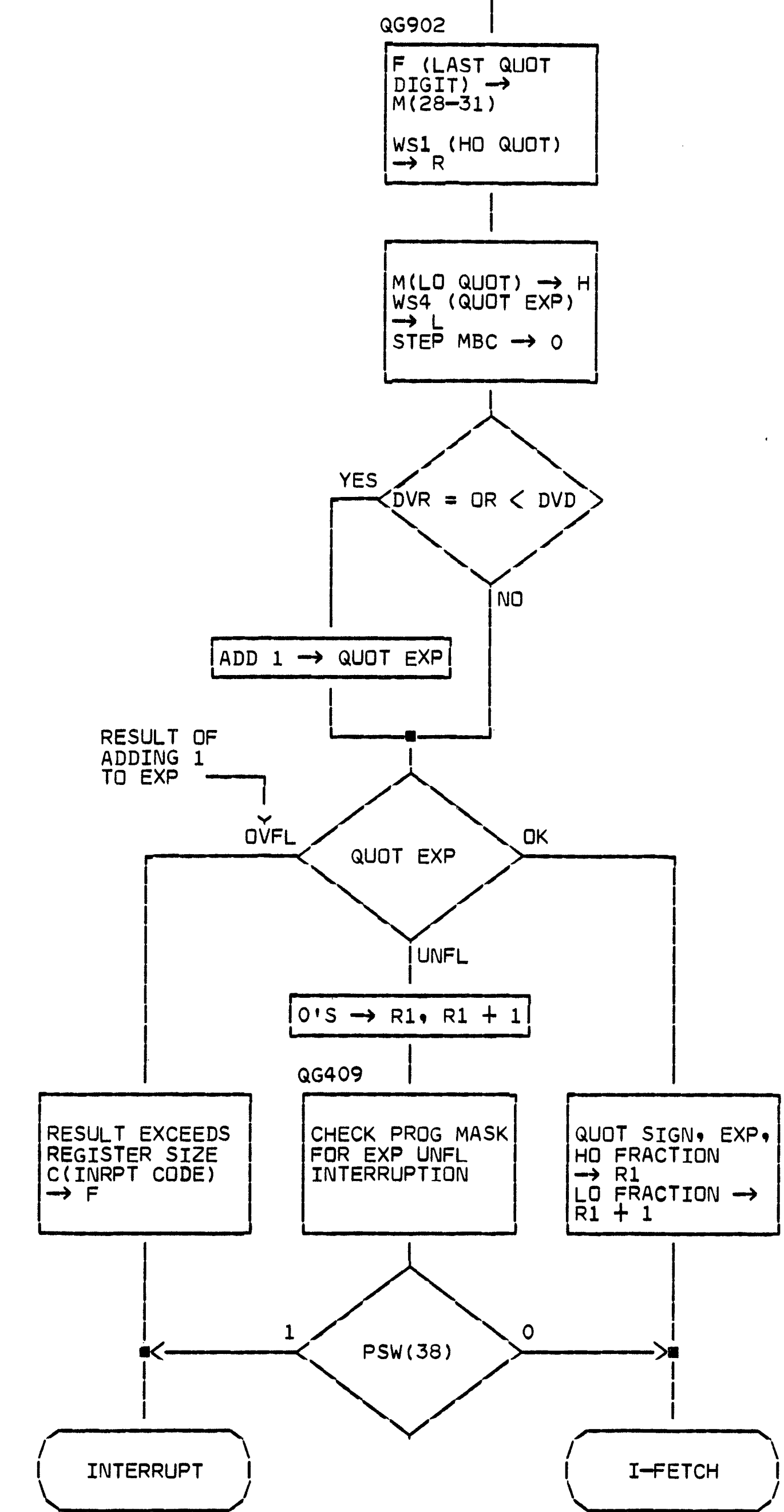
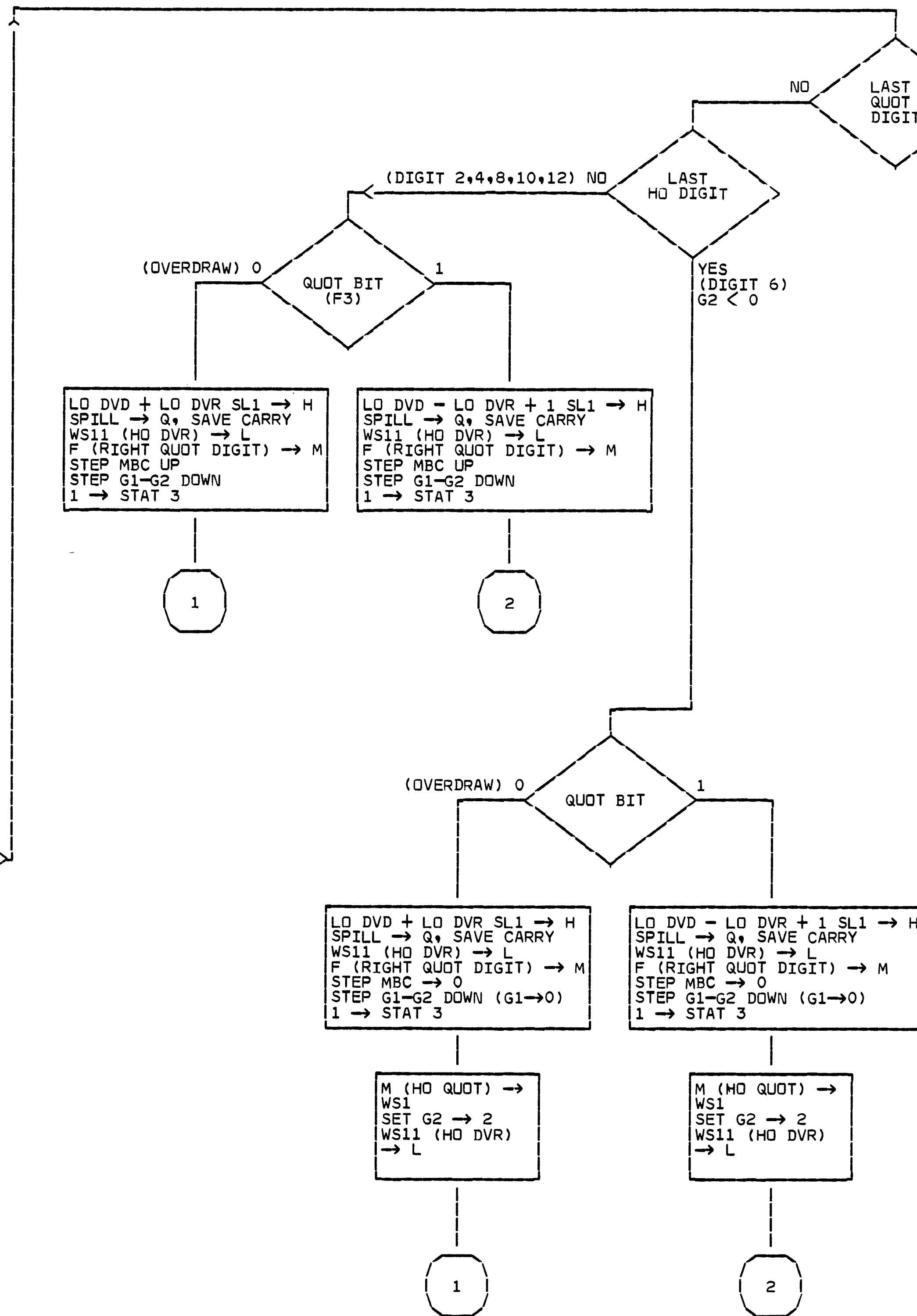
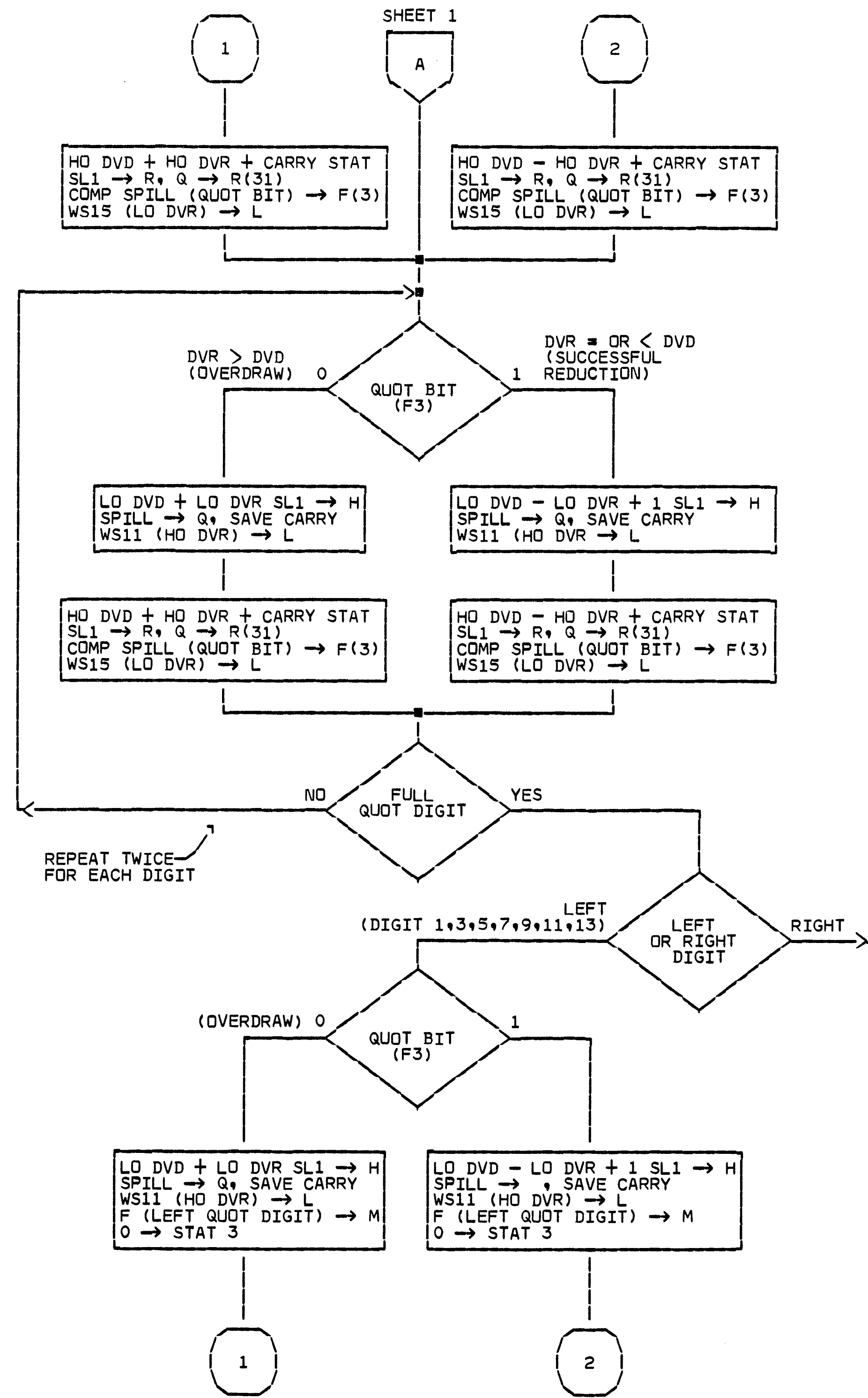


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FP DIVIDE (LONG PRECISION)  
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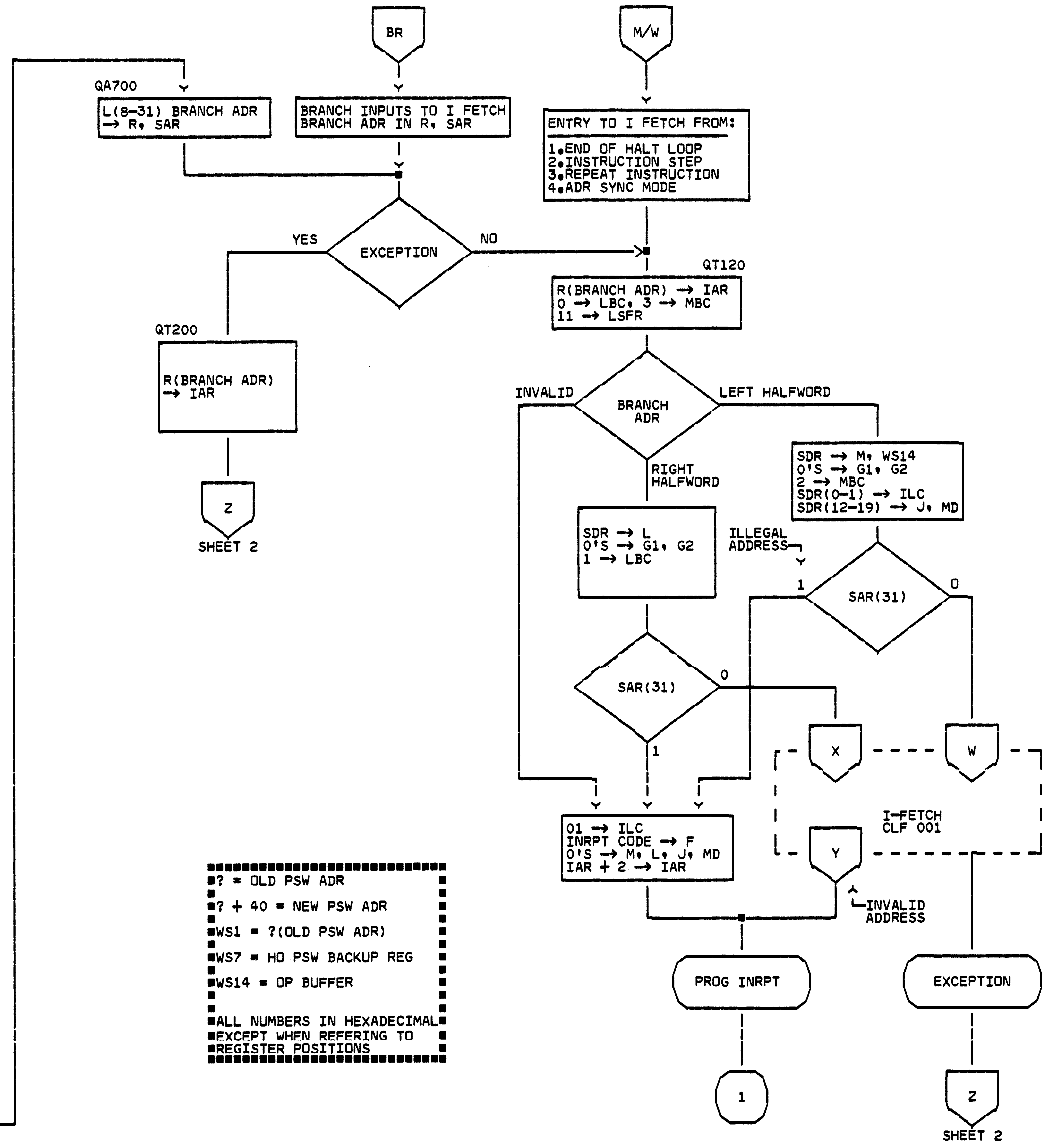
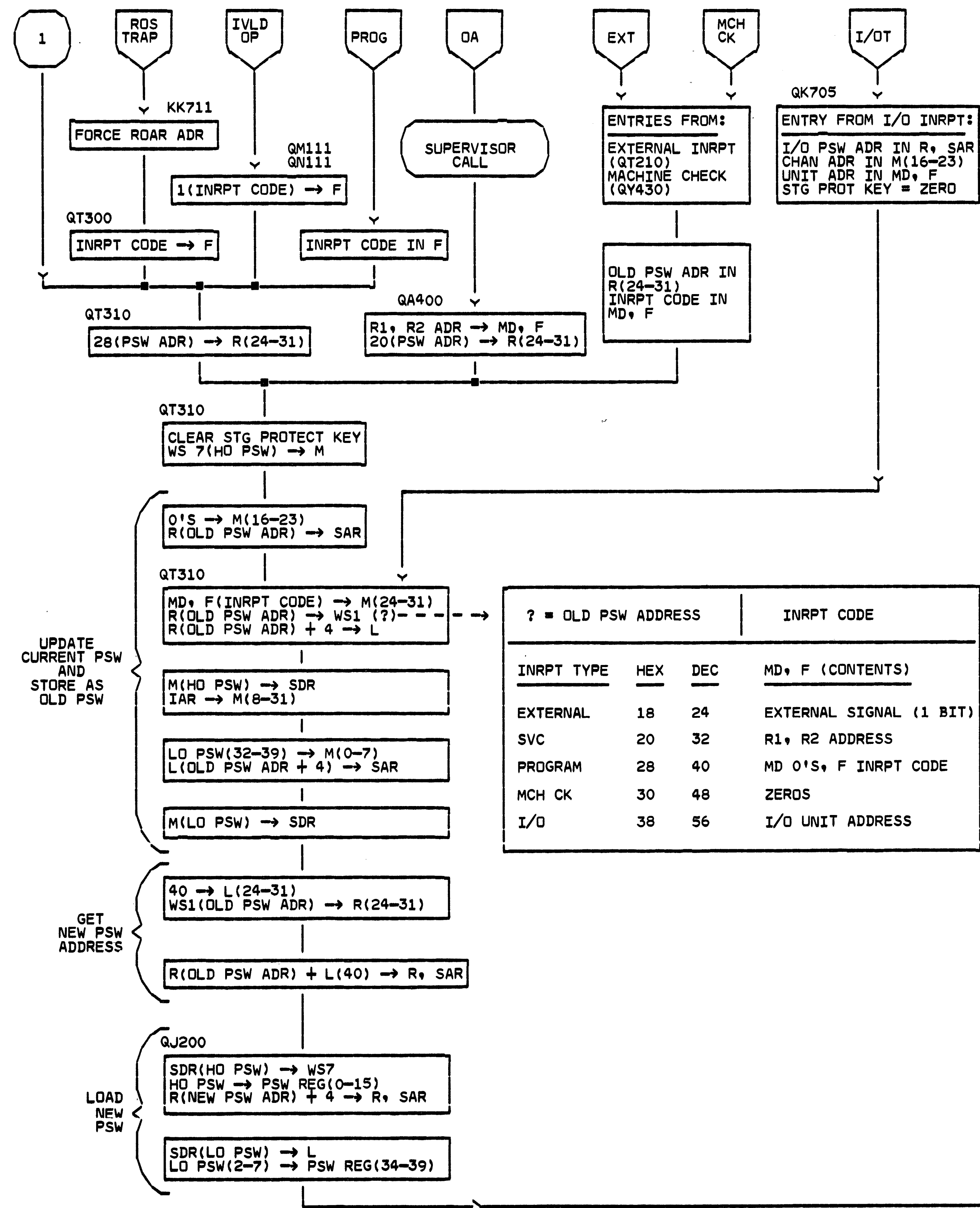
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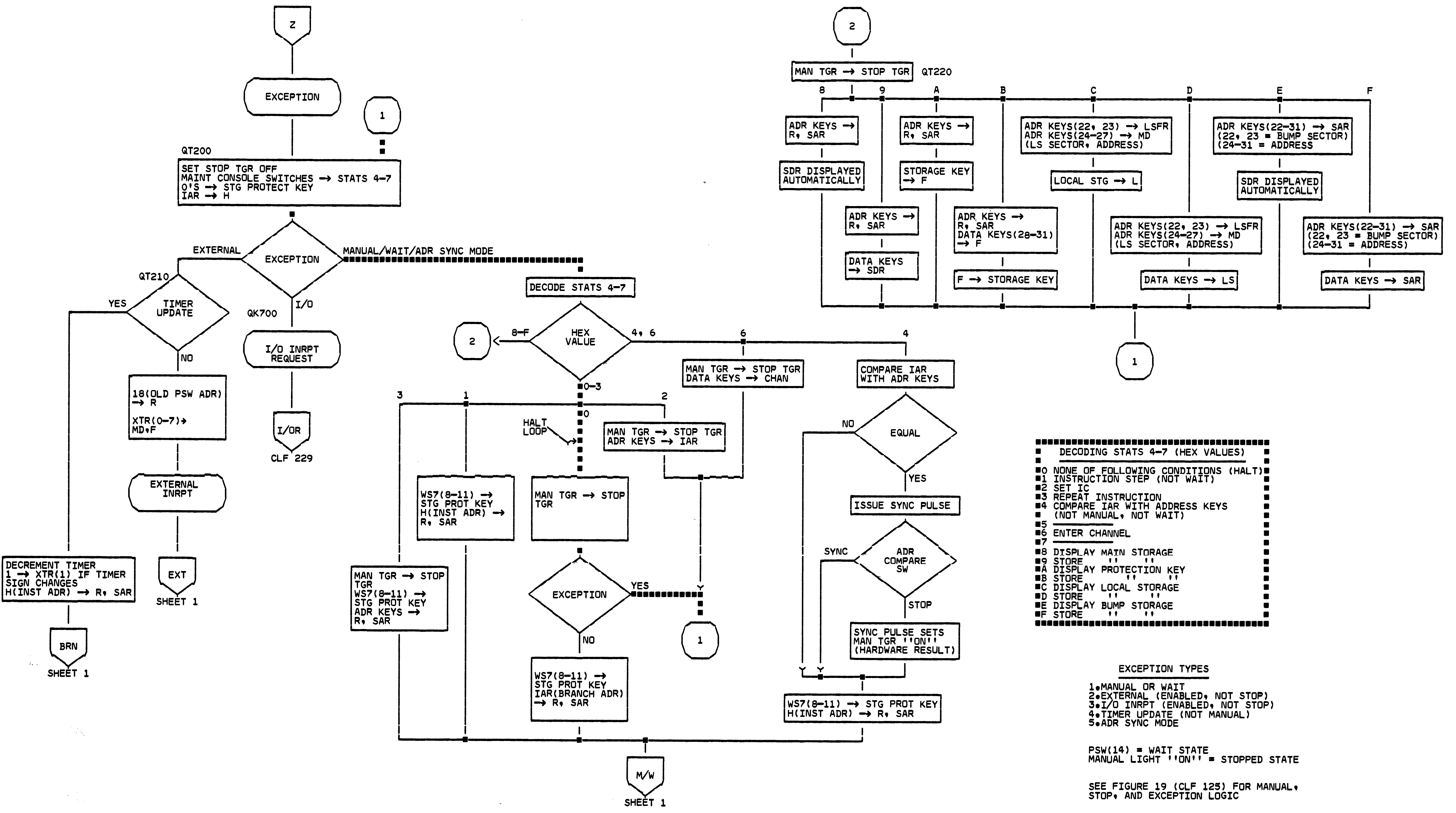
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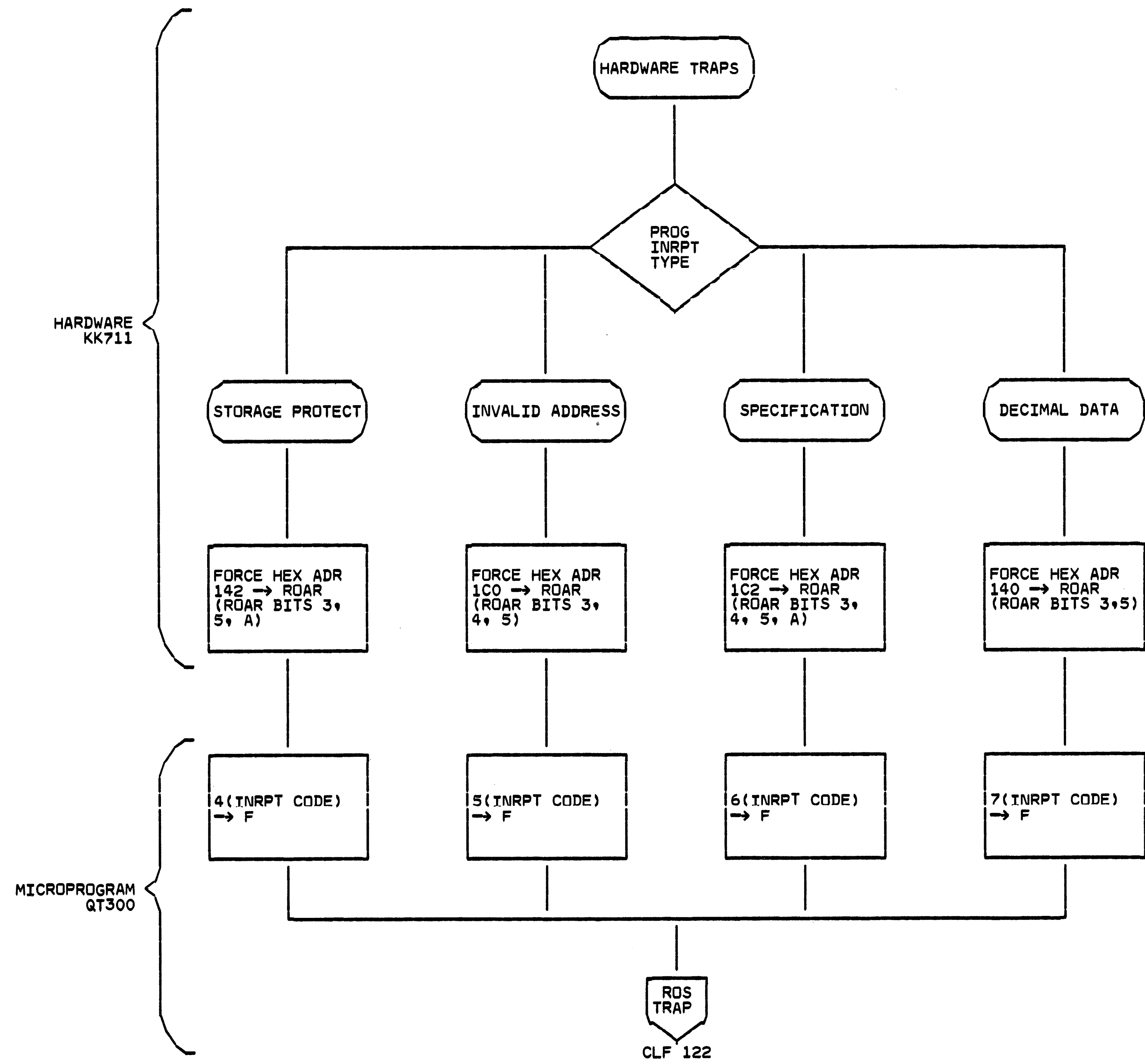


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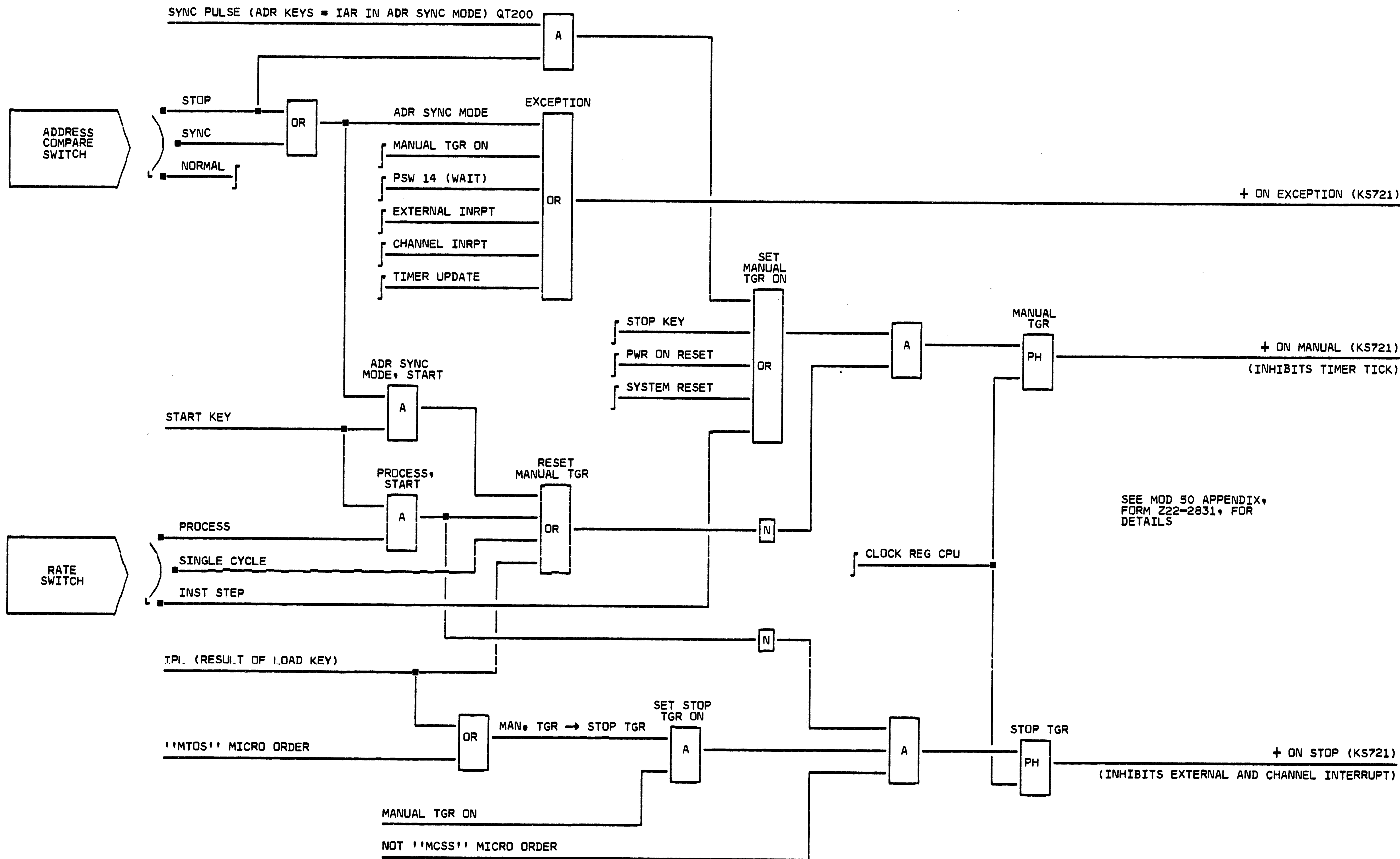


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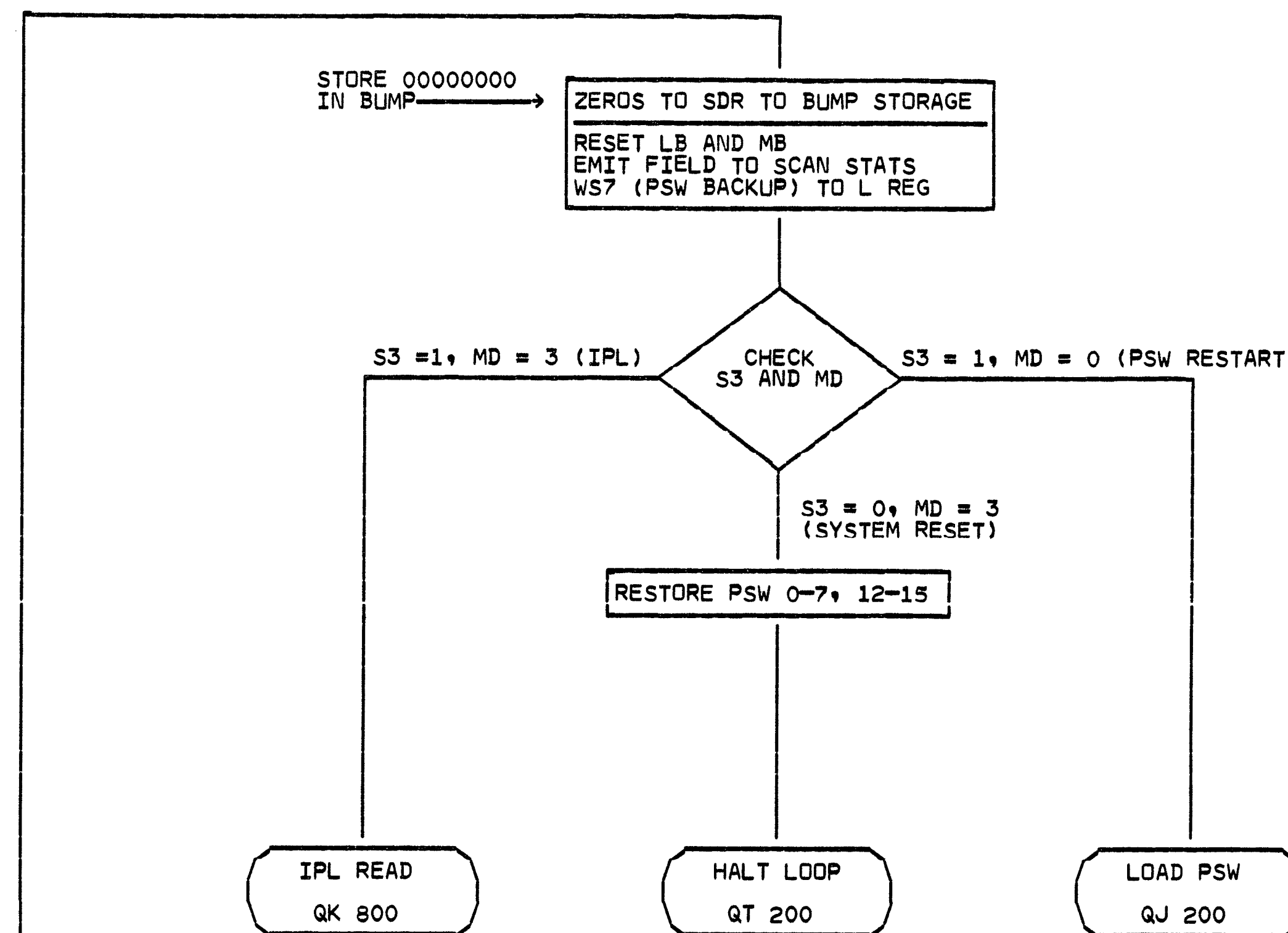
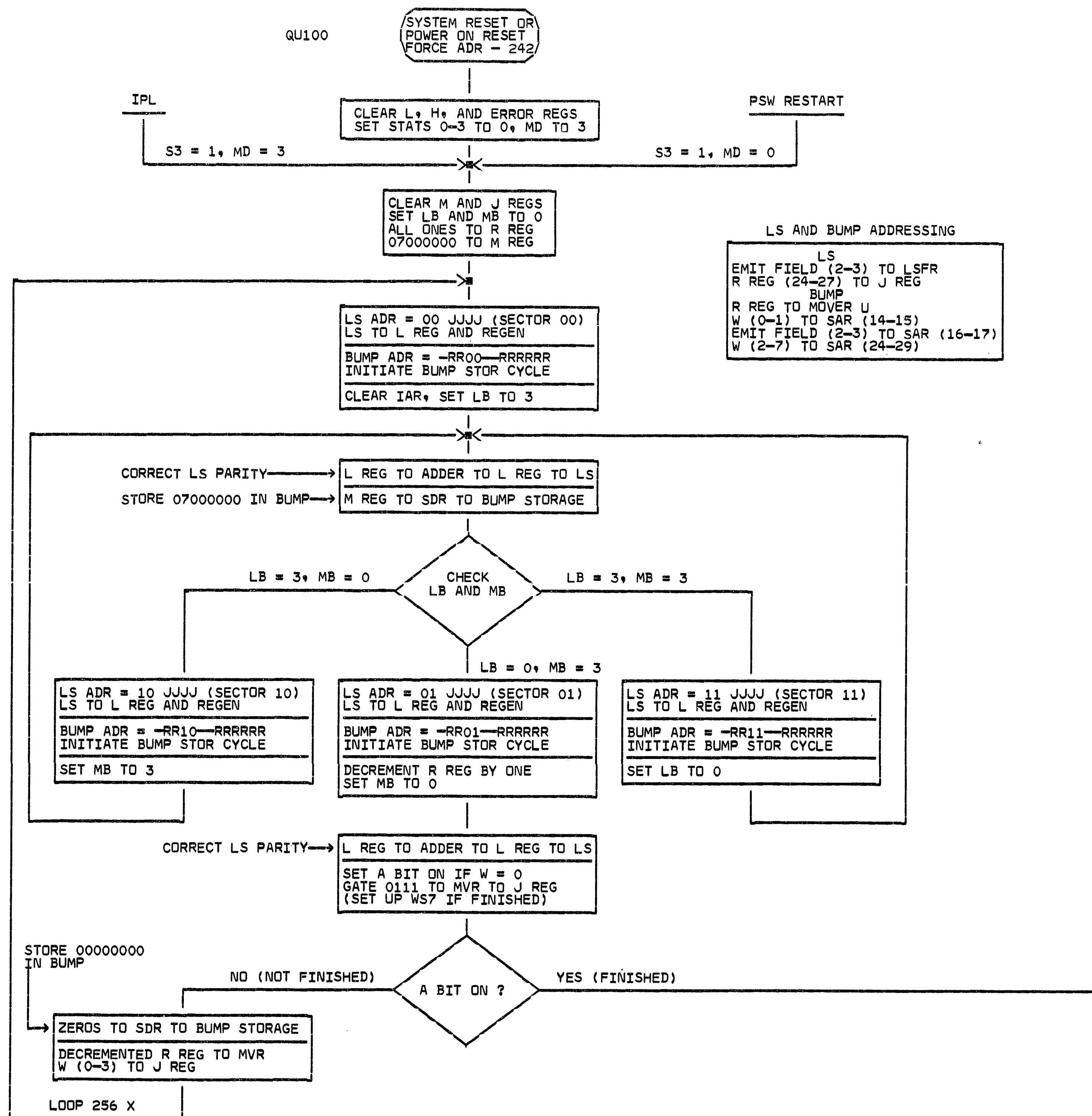
CLF 124  
 DATE 27 JUN 66 MACH. 2050  
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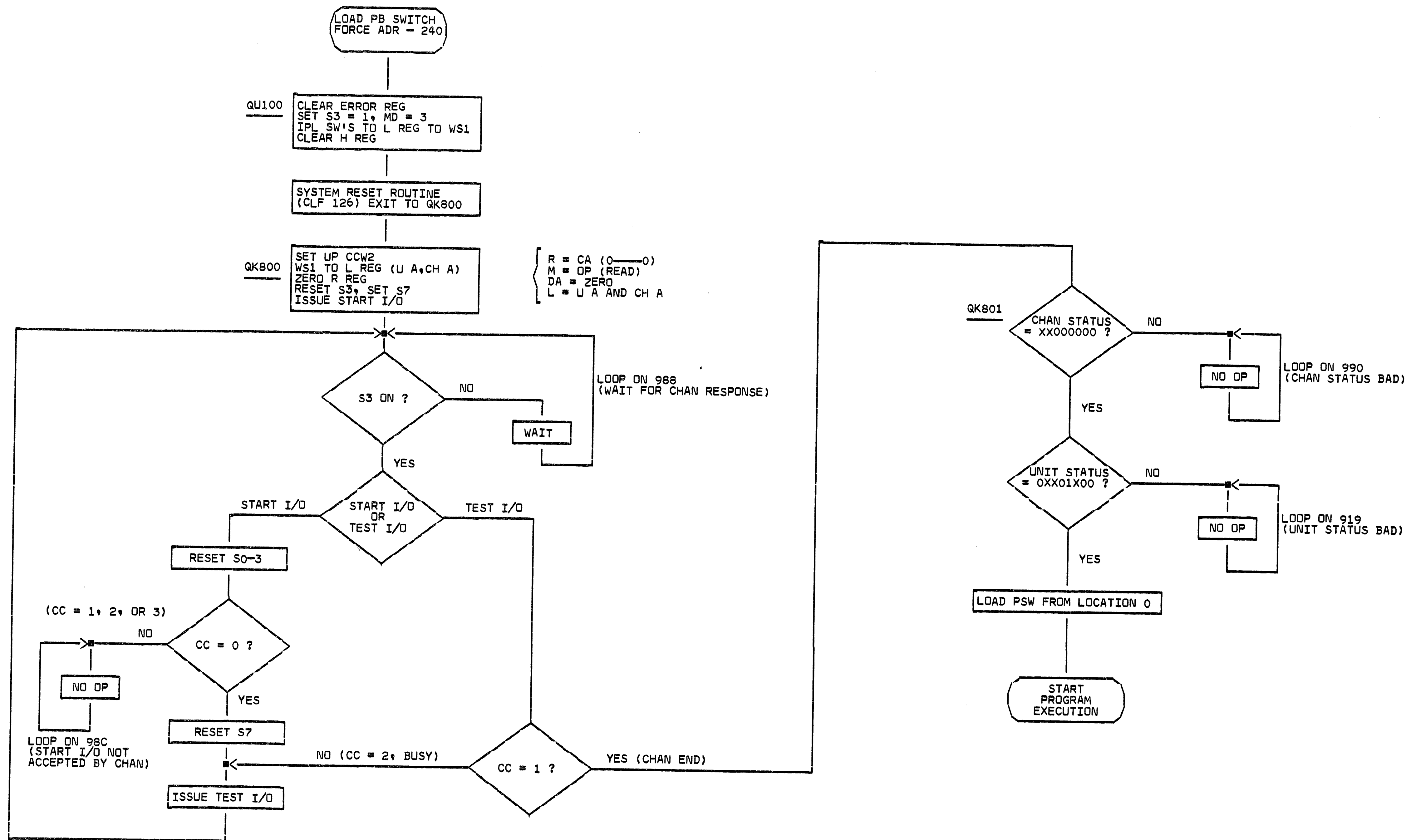
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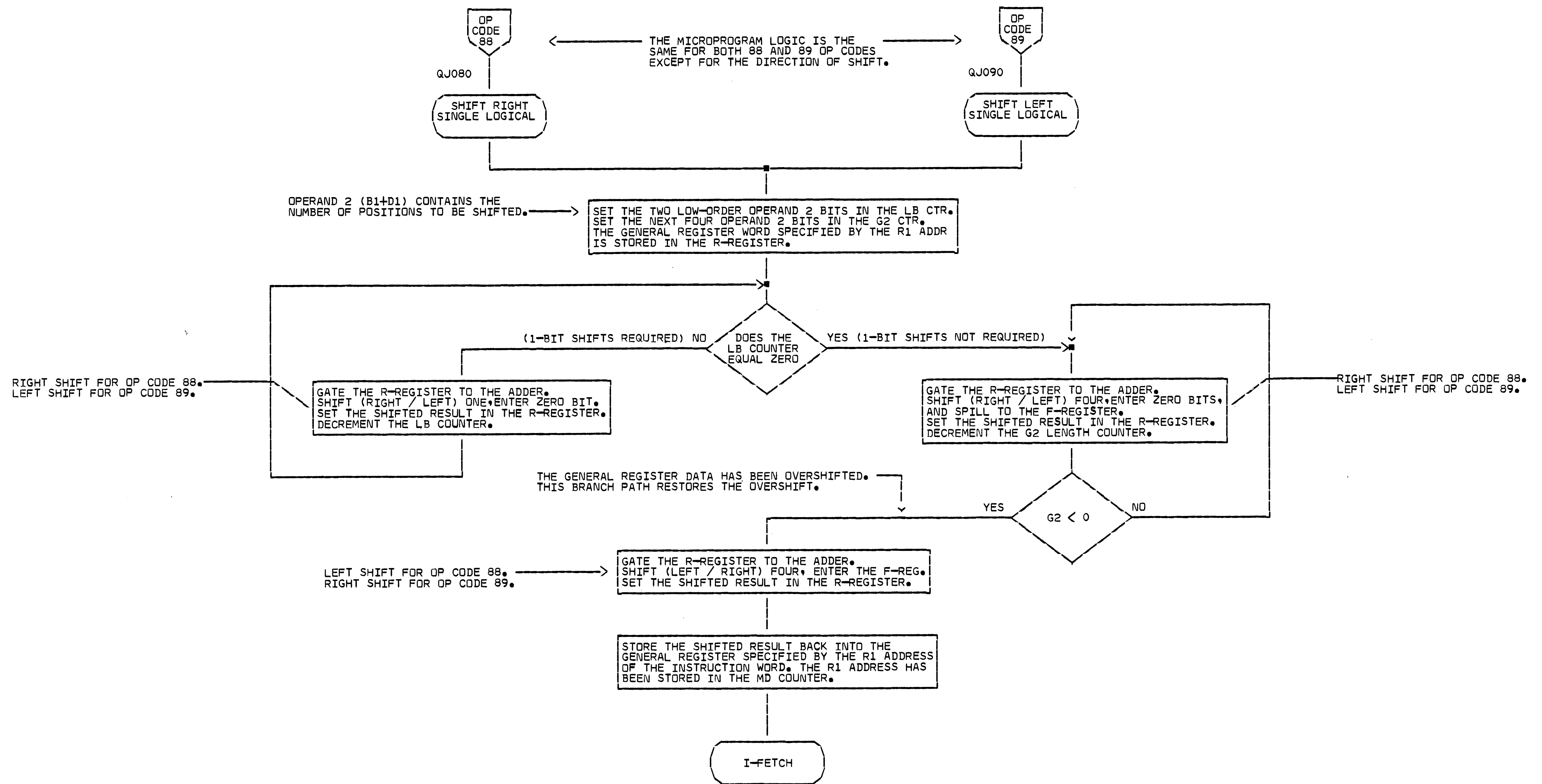


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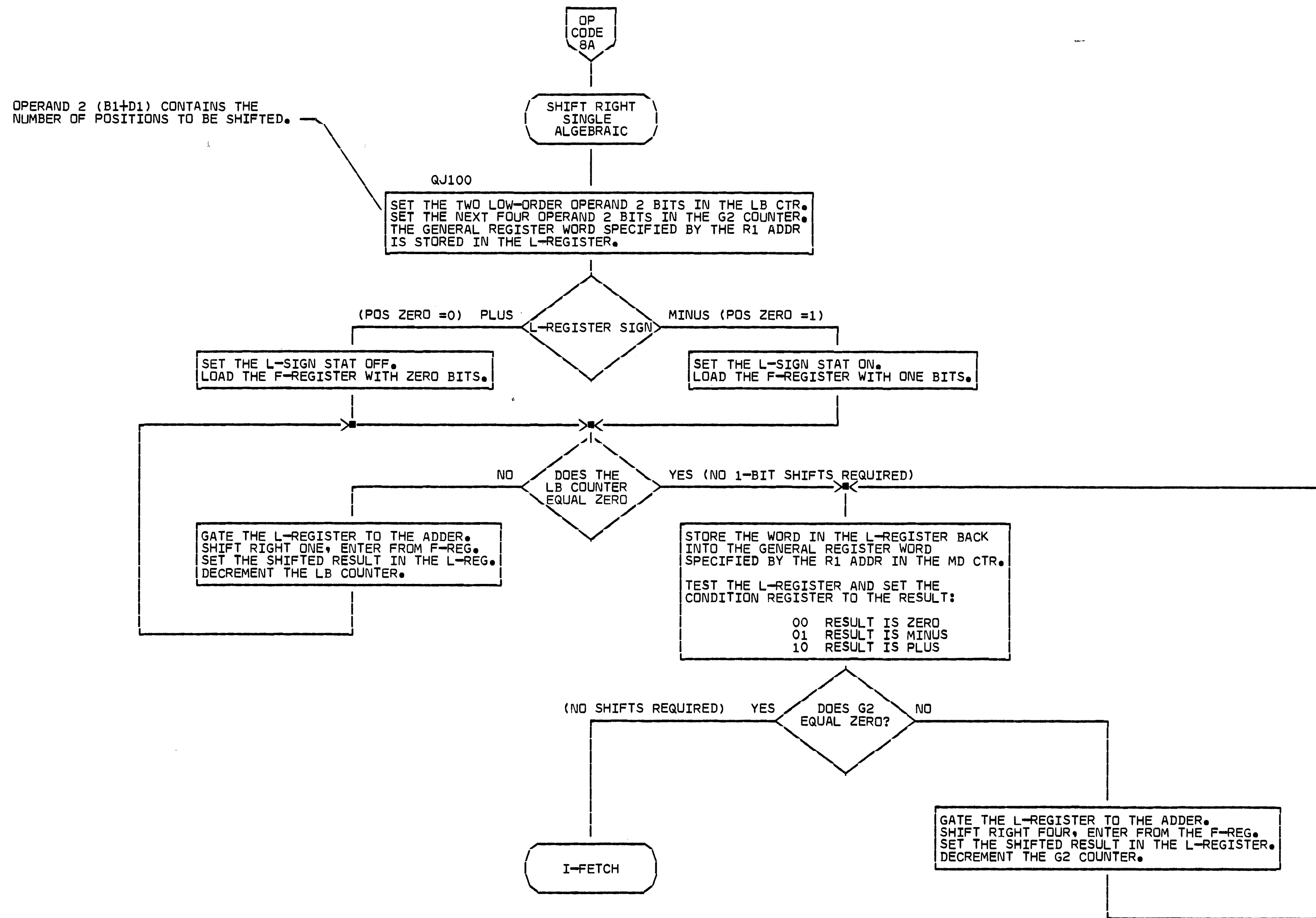


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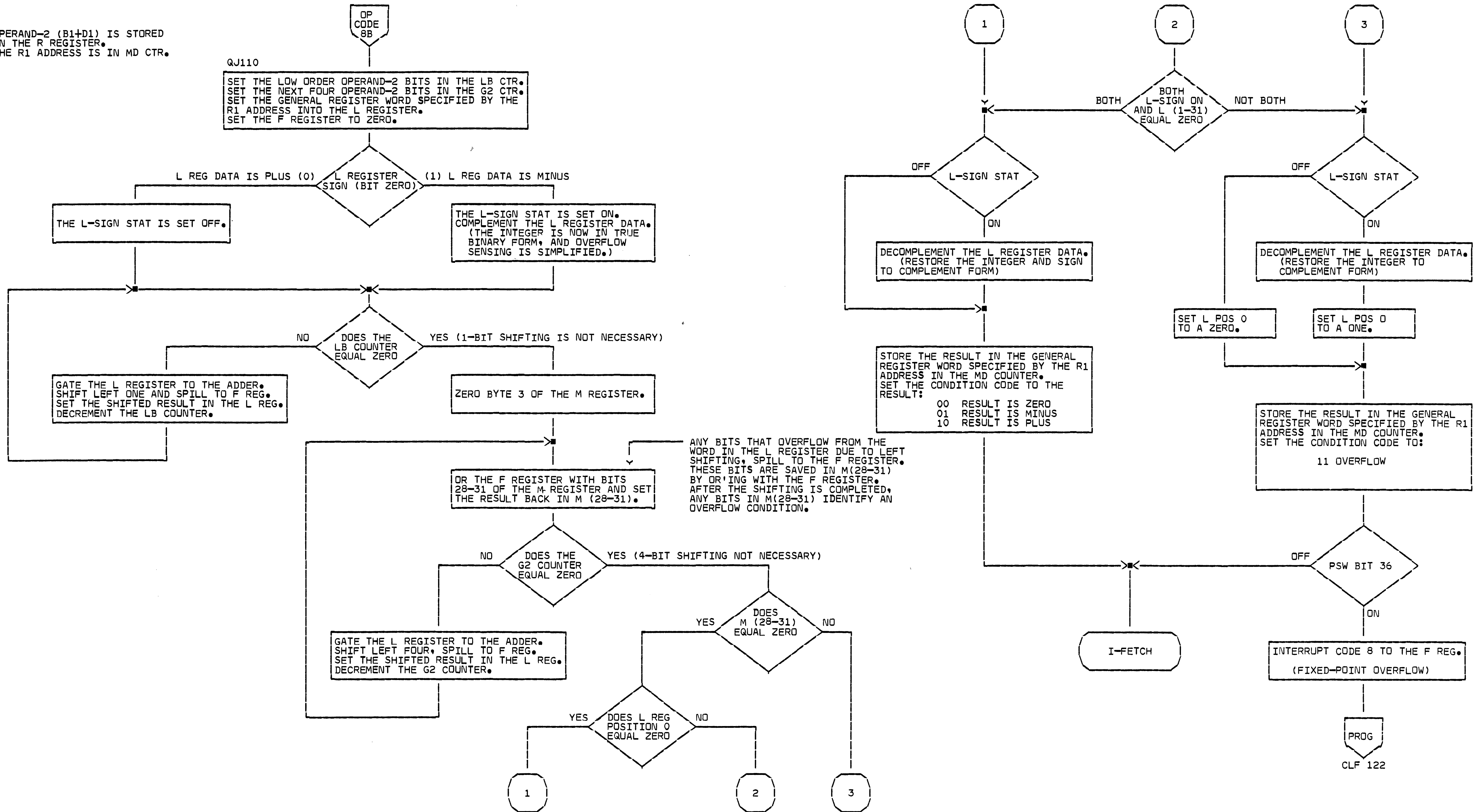


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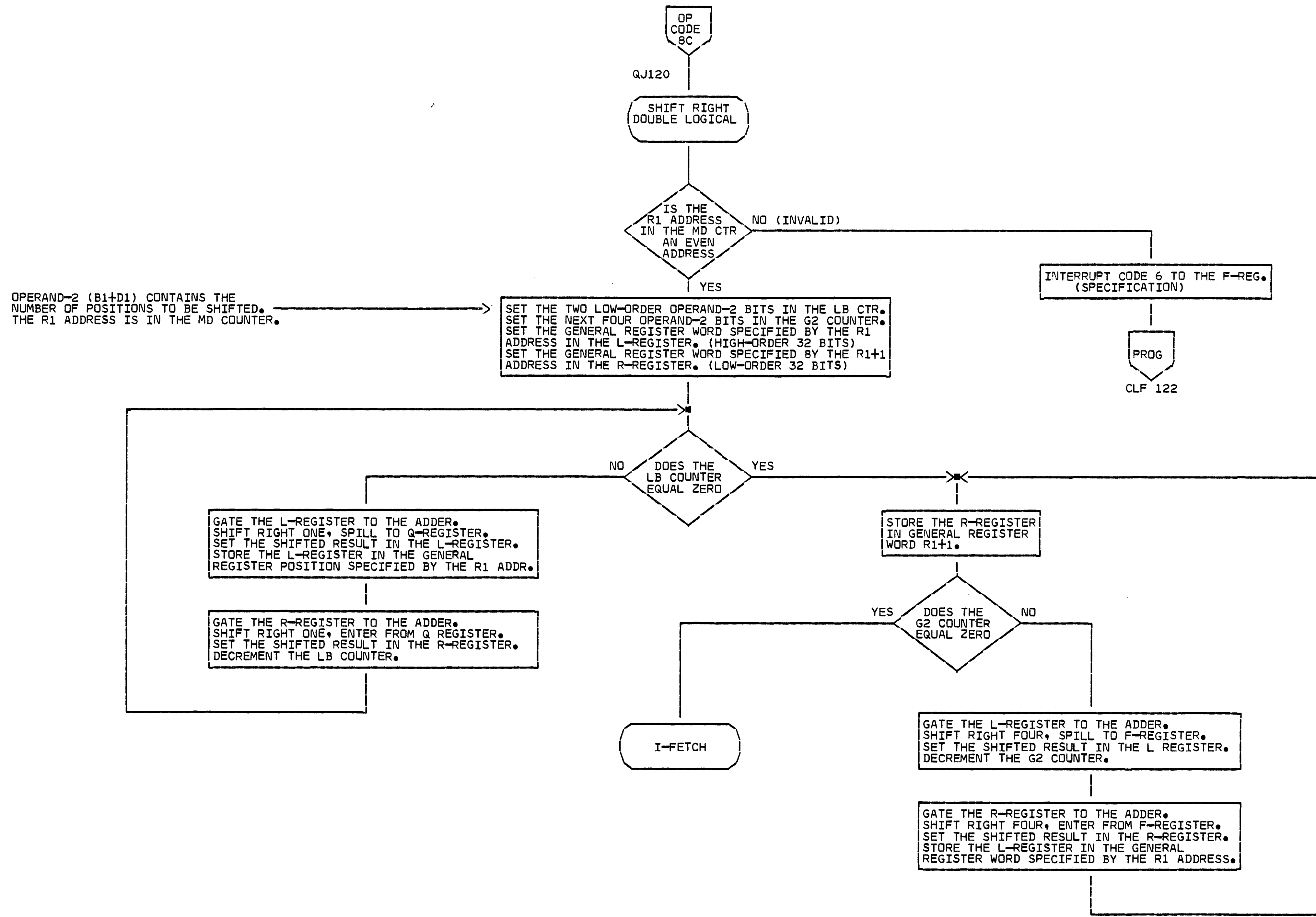
CLF 203

OPERAND-2 (B1+D1) IS STORED  
IN THE R REGISTER.  
THE R1 ADDRESS IS IN MD CTR.



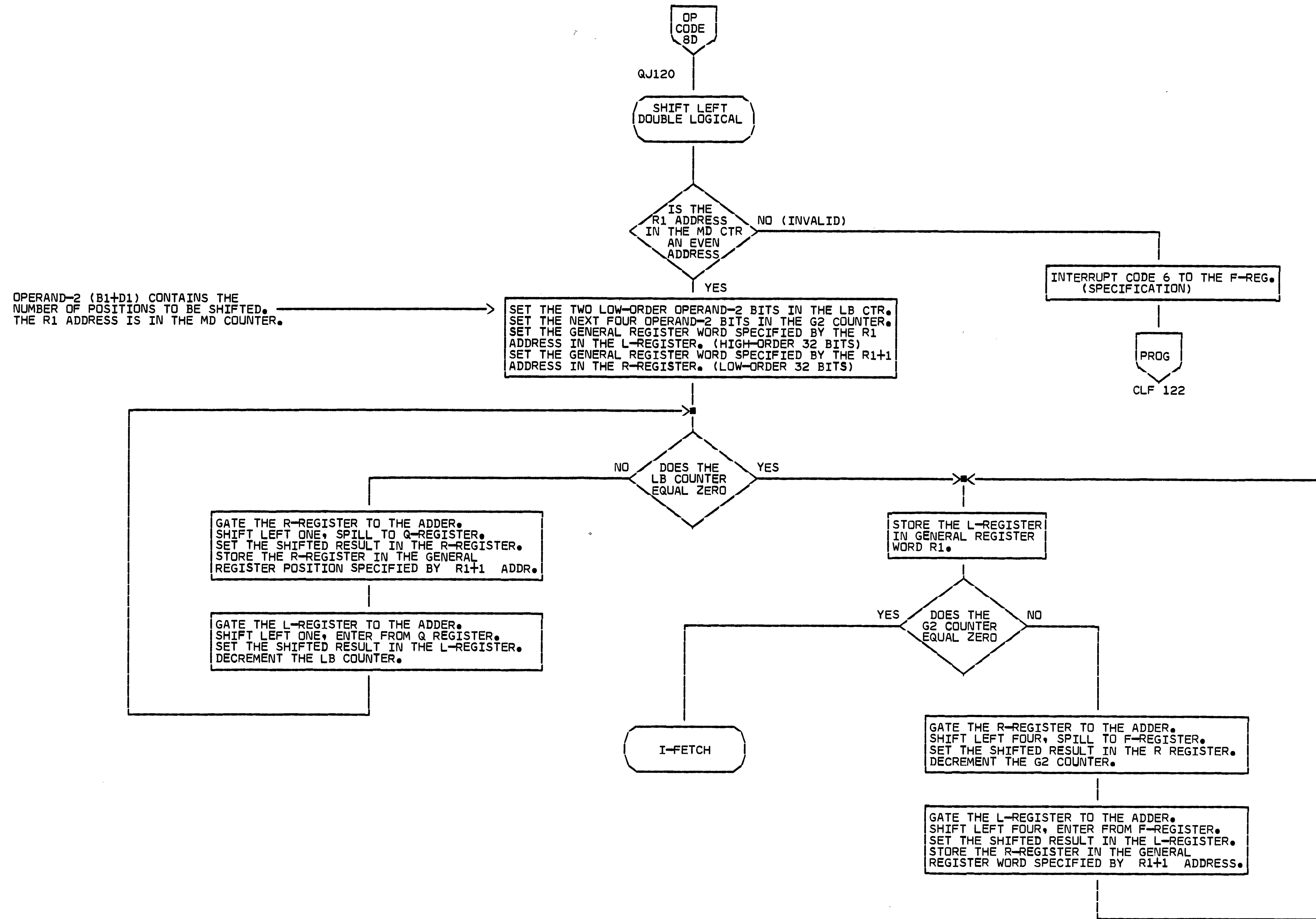
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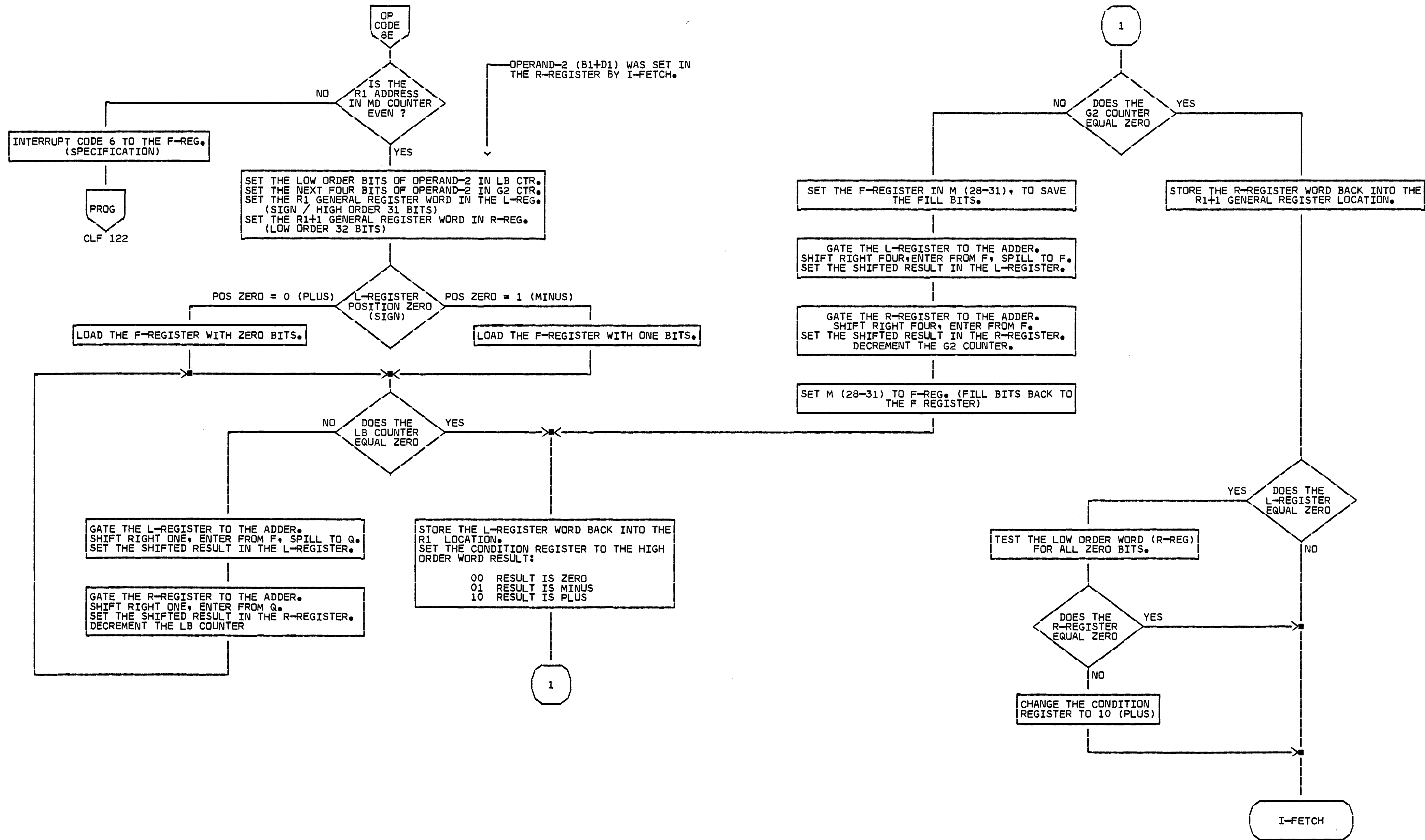


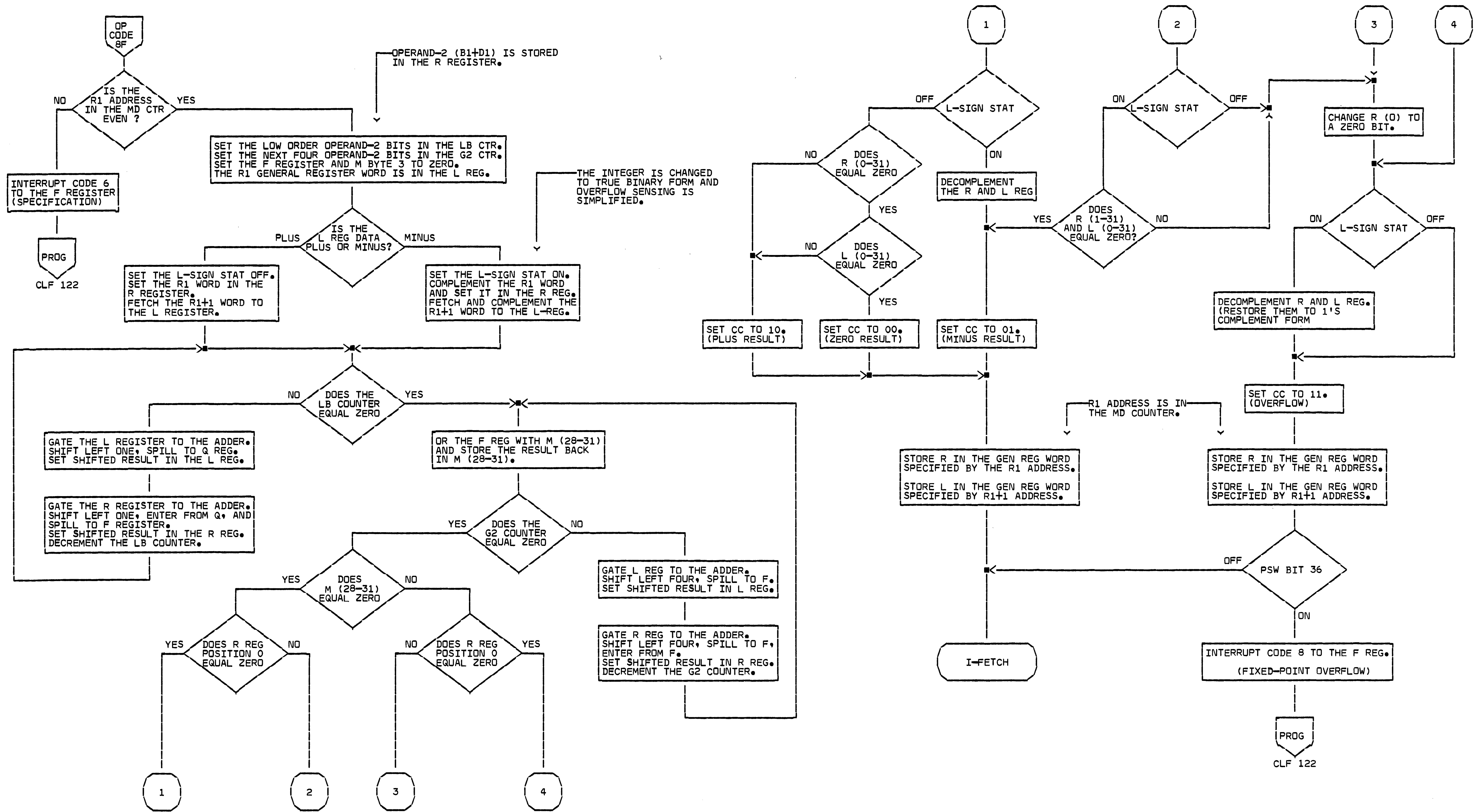
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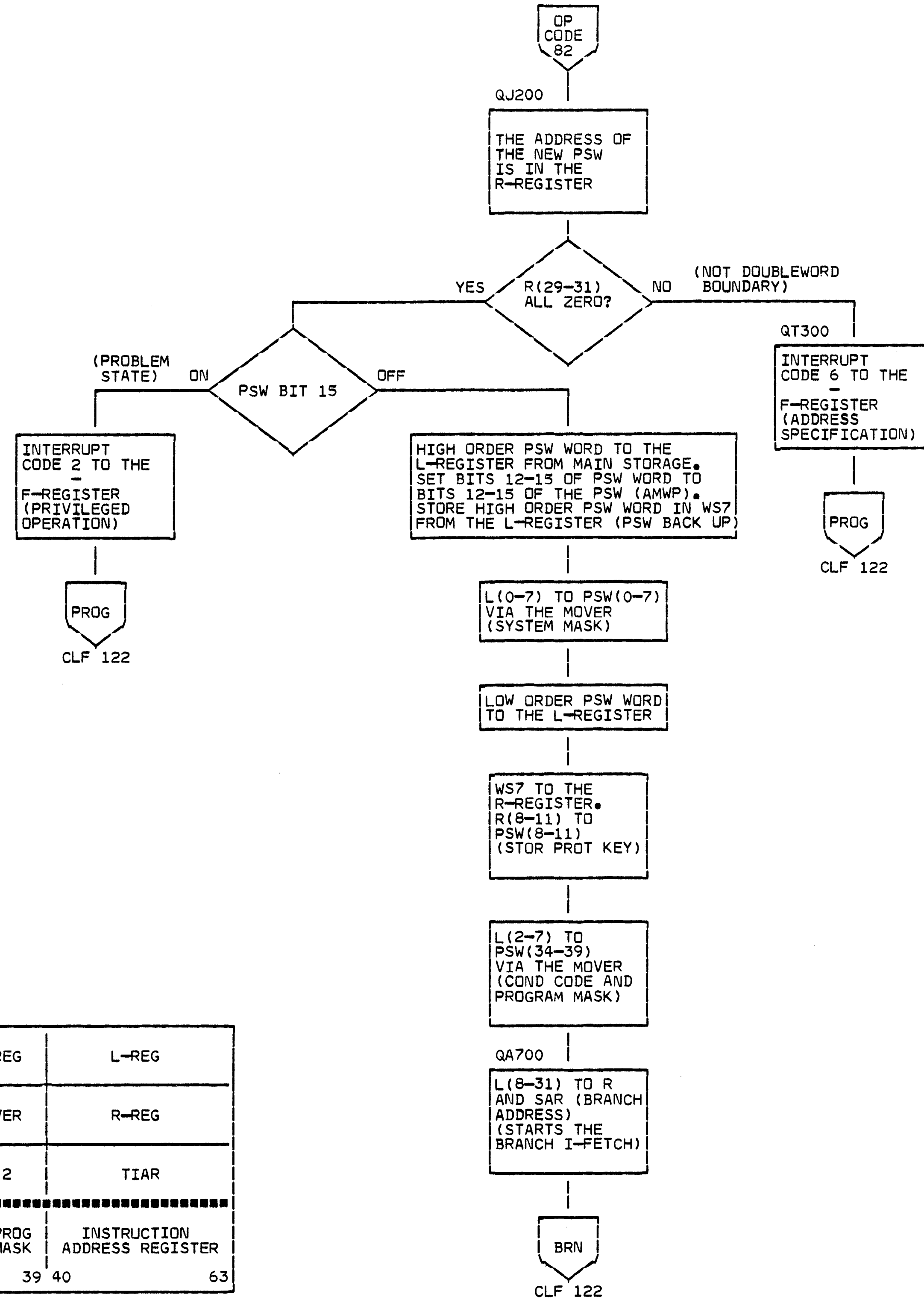
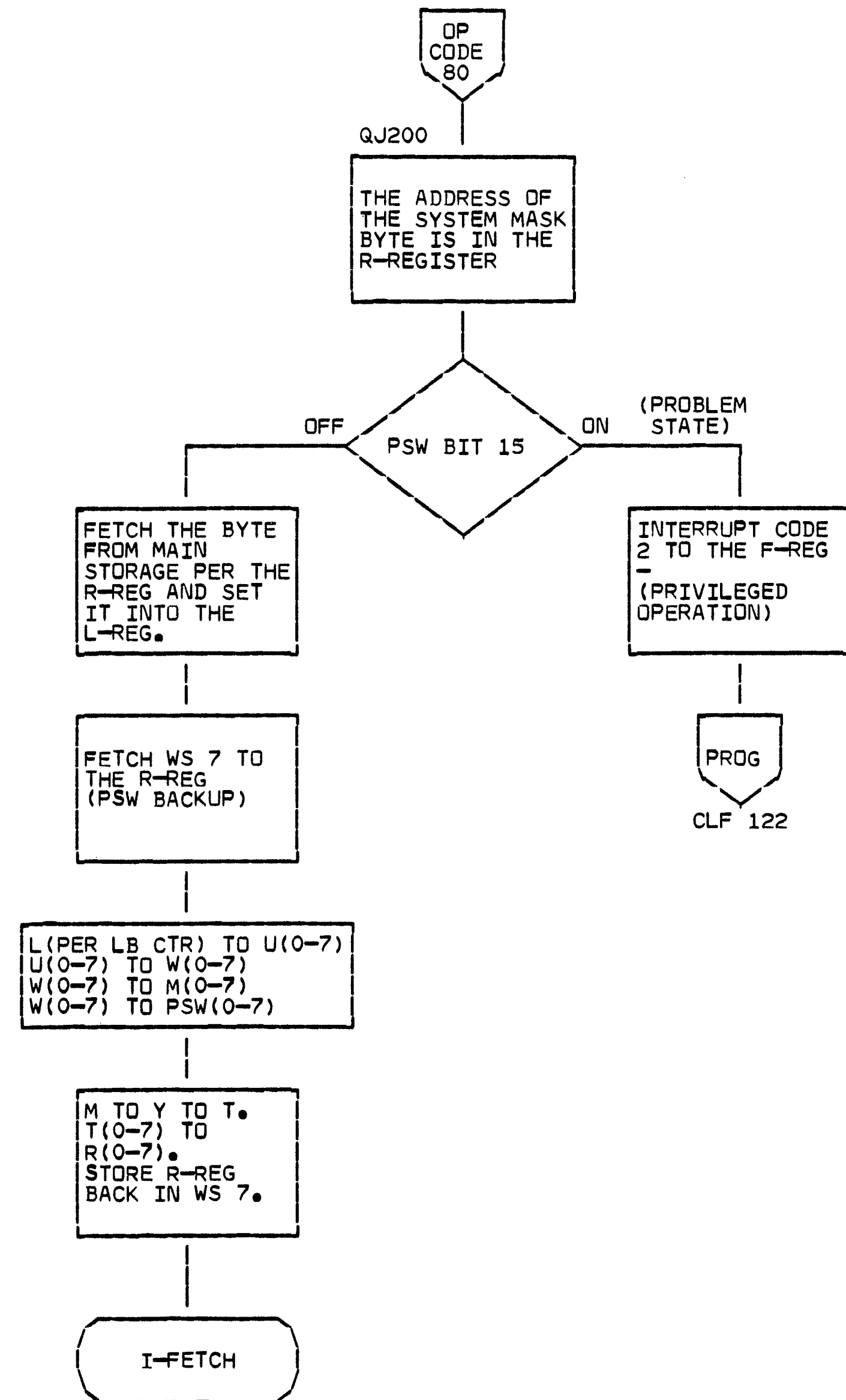
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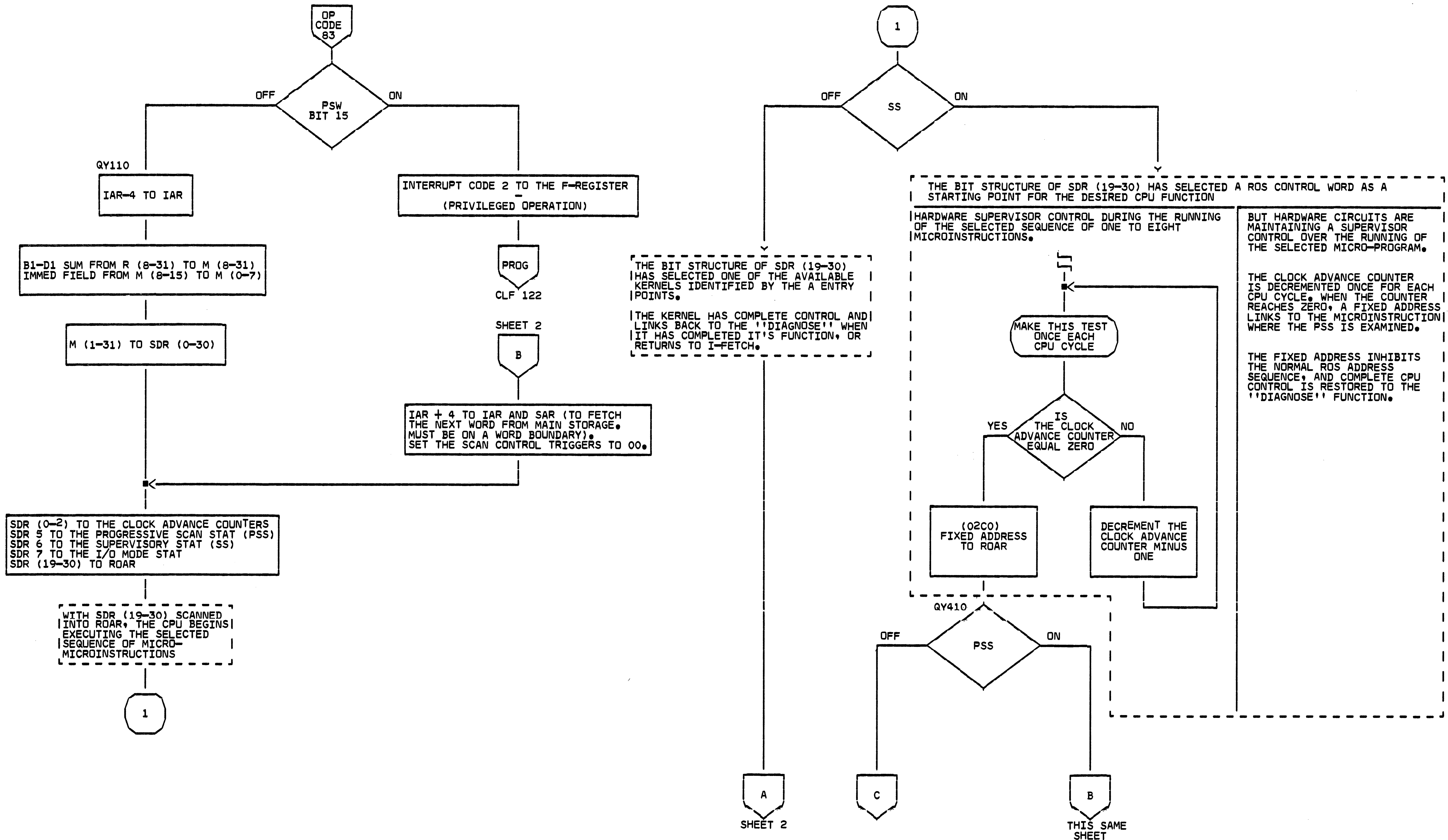


REGISTER	L-REG	R-REG	L-REG		L-REG	L-REG
PATH	MOVER	ADDER	ADDER		MOVER	R-REG
MICRO ORDER	WP 1	TSPM	TWS		WP 2	TIAR
PSW	SYSTEM MASK	SP KEY	AMWP		CC PROG MASK	INSTRUCTION ADDRESS REGISTER
	0 7 8	11 12 15			34 39 40	63

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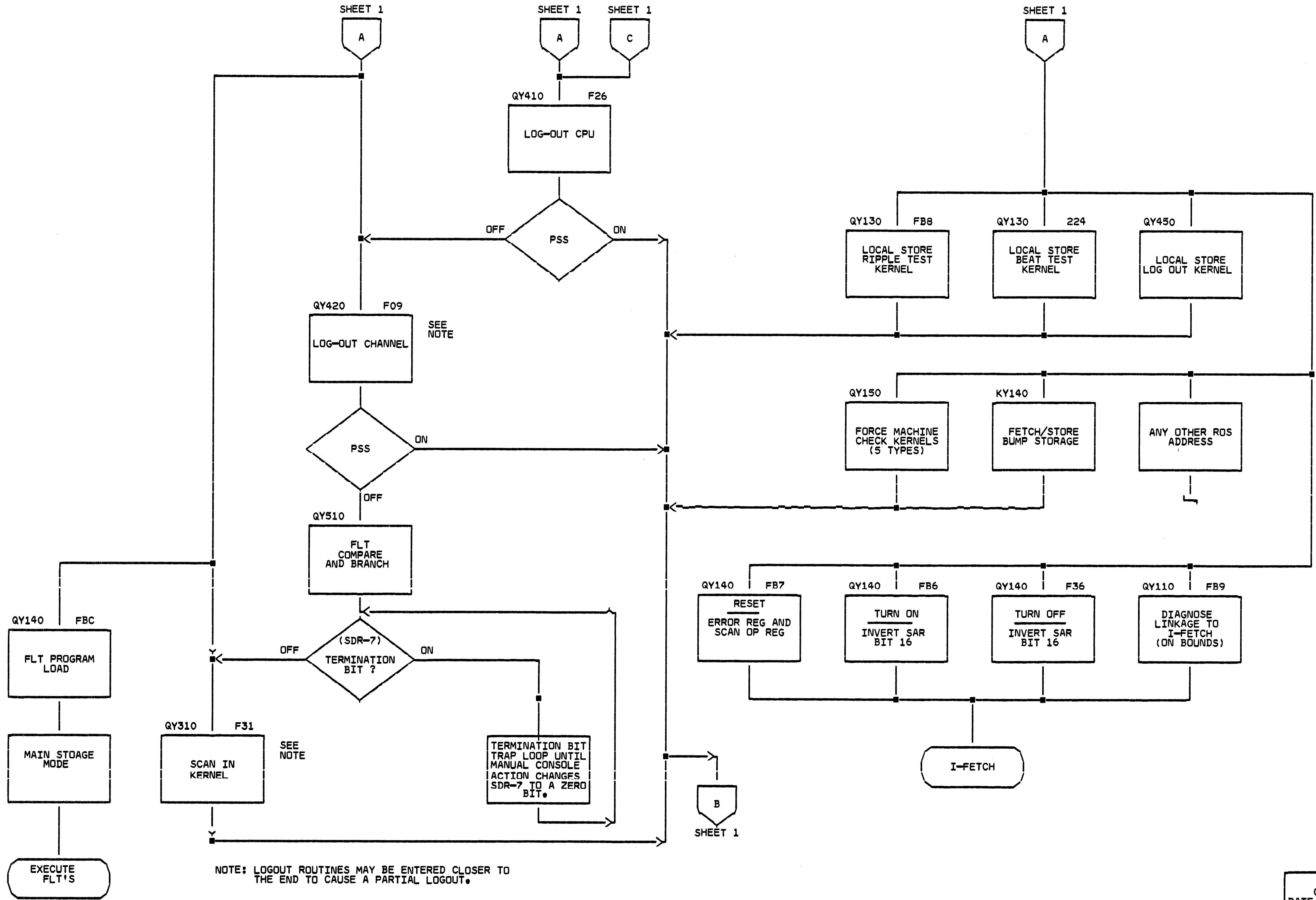
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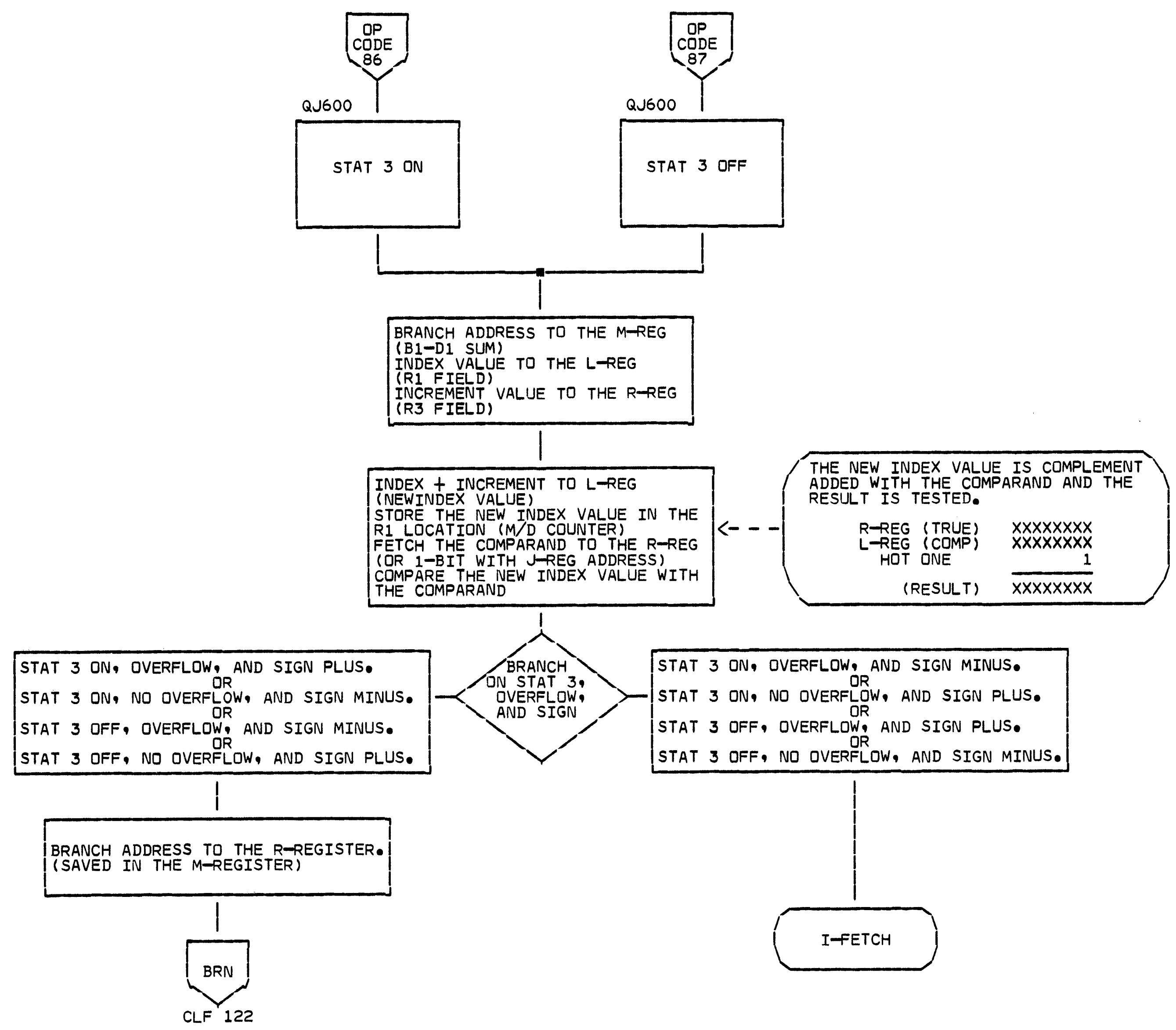
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NOTE: LOGOUT ROUTINES MAY BE ENTERED CLOSER TO THE END TO CAUSE A PARTIAL LOGOUT.

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DEFINITIONS

- STAT 3: IDENTIFIES THE INSTRUCTION BEING EXECUTED. BRANCH CONDITIONS FOR BXH (STAT 3 ON) ARE I-FETCH CONDITIONS FOR BXLE (STAT 3 OFF).
- OFLO: OVERFLOW IS IDENTIFIED BY AN EXCLOR OF THE CARRIES FROM POSITIONS ONE AND ZERO DURING THE COMPARE. IT OCCURS WHEN THE DIFFERENCE IS GREATER THAN THE CAPACITY OF A 31 BIT BINARY INTEGER.
- SIGN: THE HIGH ORDER BIT IS EXAMINED TO DETERMINE THE SIGN OF THE RESULT. A 0-BIT IS A PLUS SIGN AND A 1-BIT IS A MINUS SIGN.

EXAMPLE

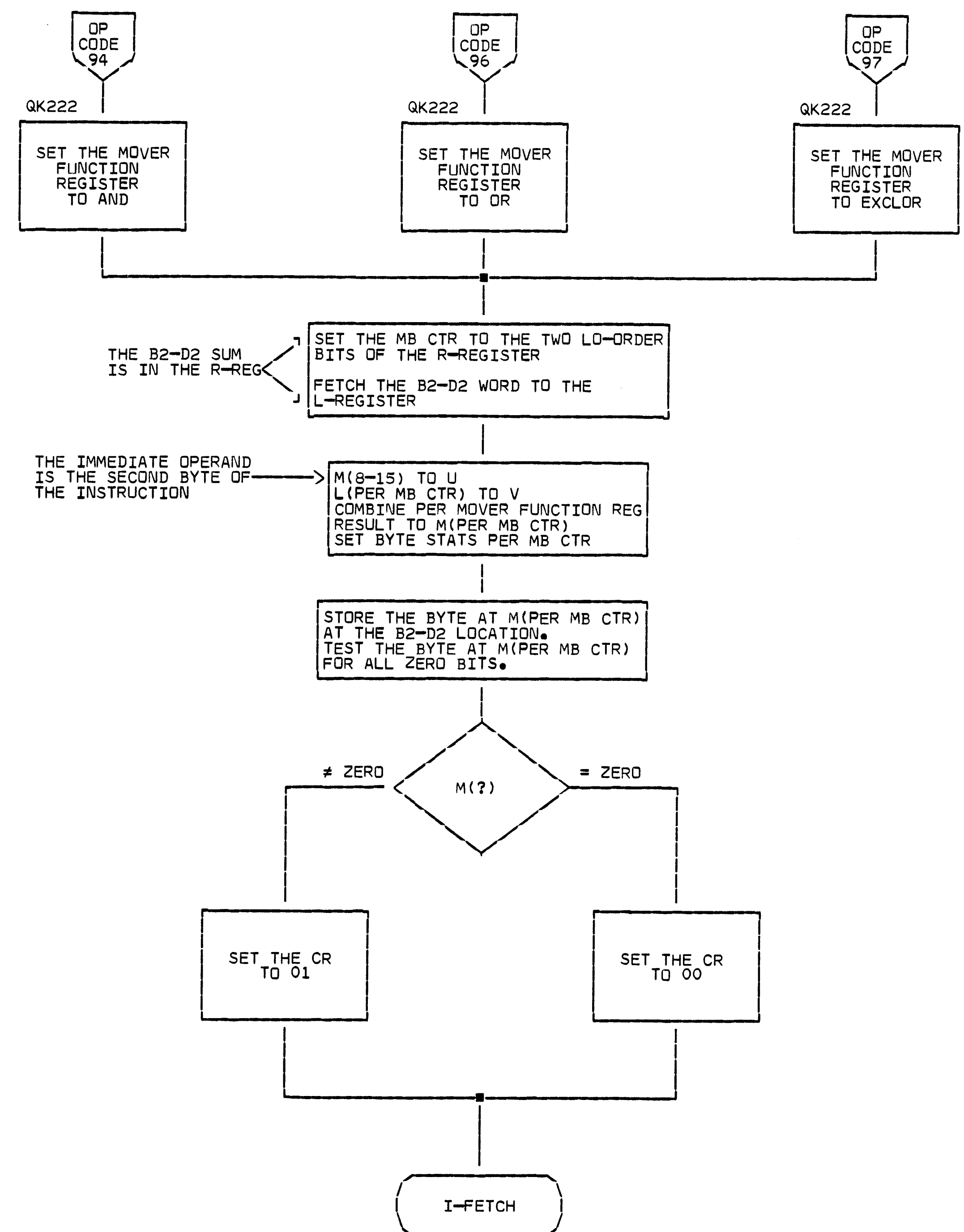
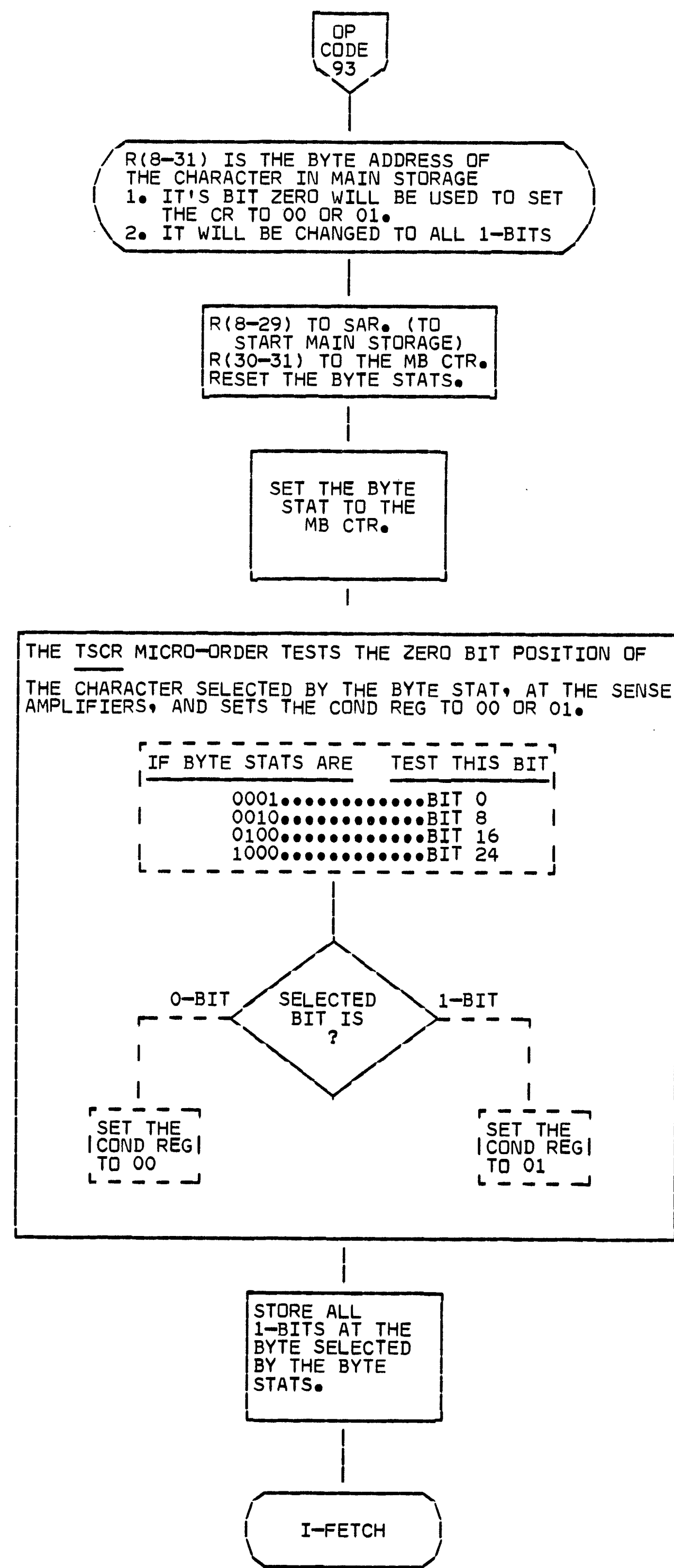
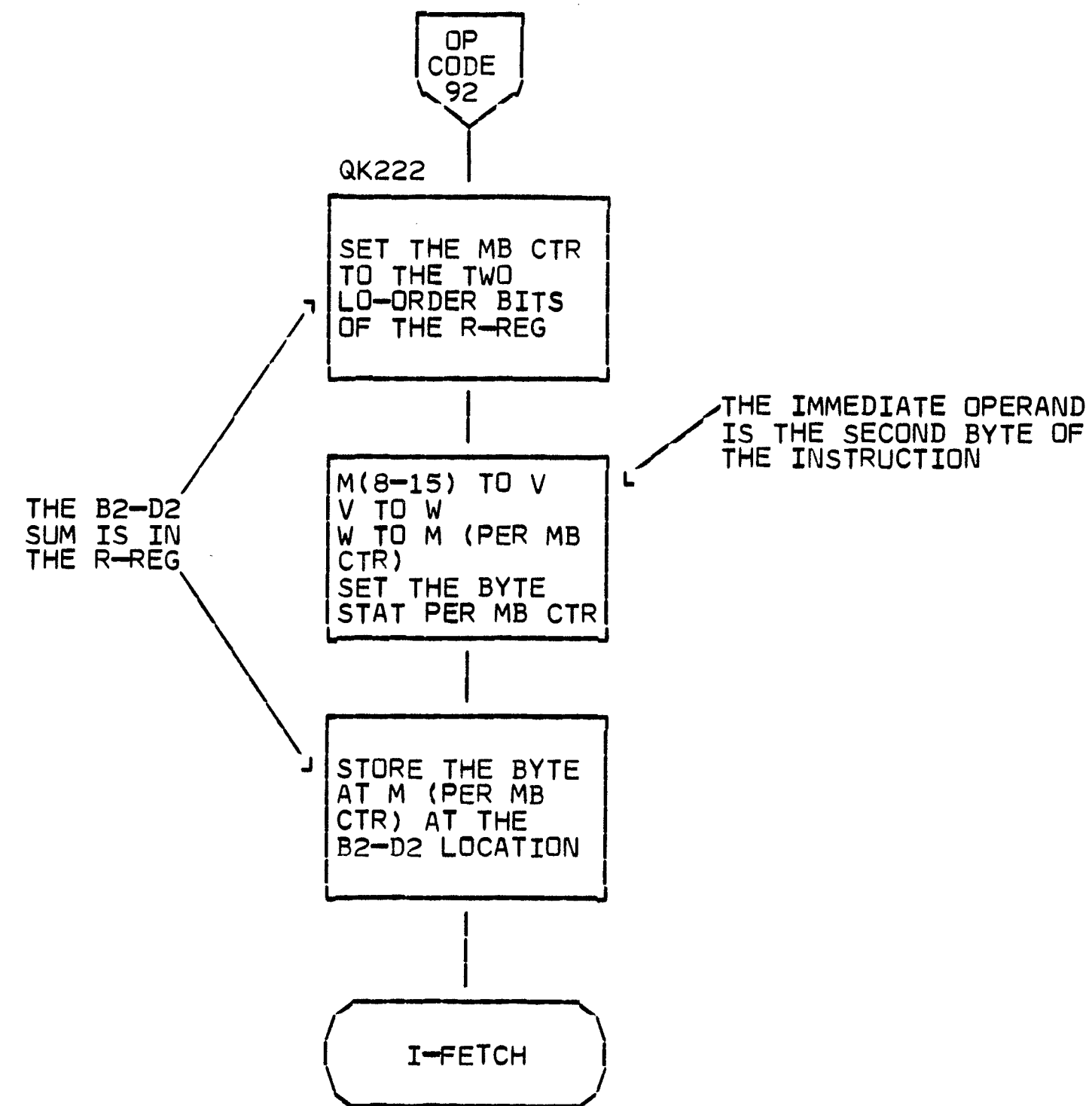
DURING THE COMPARE, THE NEW INDEX VALUE IS COMPLEMENTED. IF THE NEW INDEX VALUE IS HIGH, THE RESULT WILL HAVE A MINUS SIGN IF THERE IS NO OVERFLOW. AN OVERFLOW REVERSES THE EFFECT OF THE SIGN ANALYSIS ON THE BRANCH/I-FETCH CONDITIONS.

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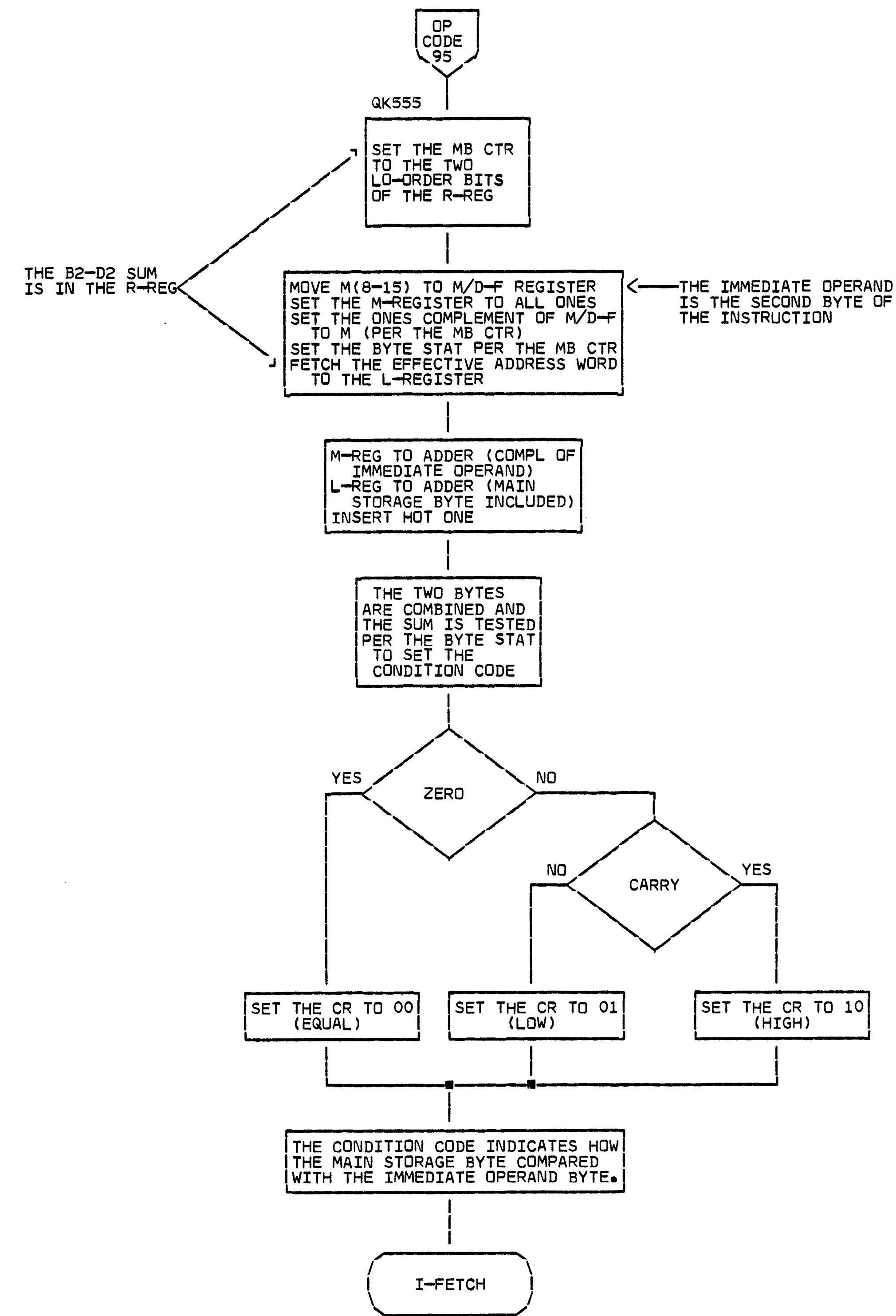
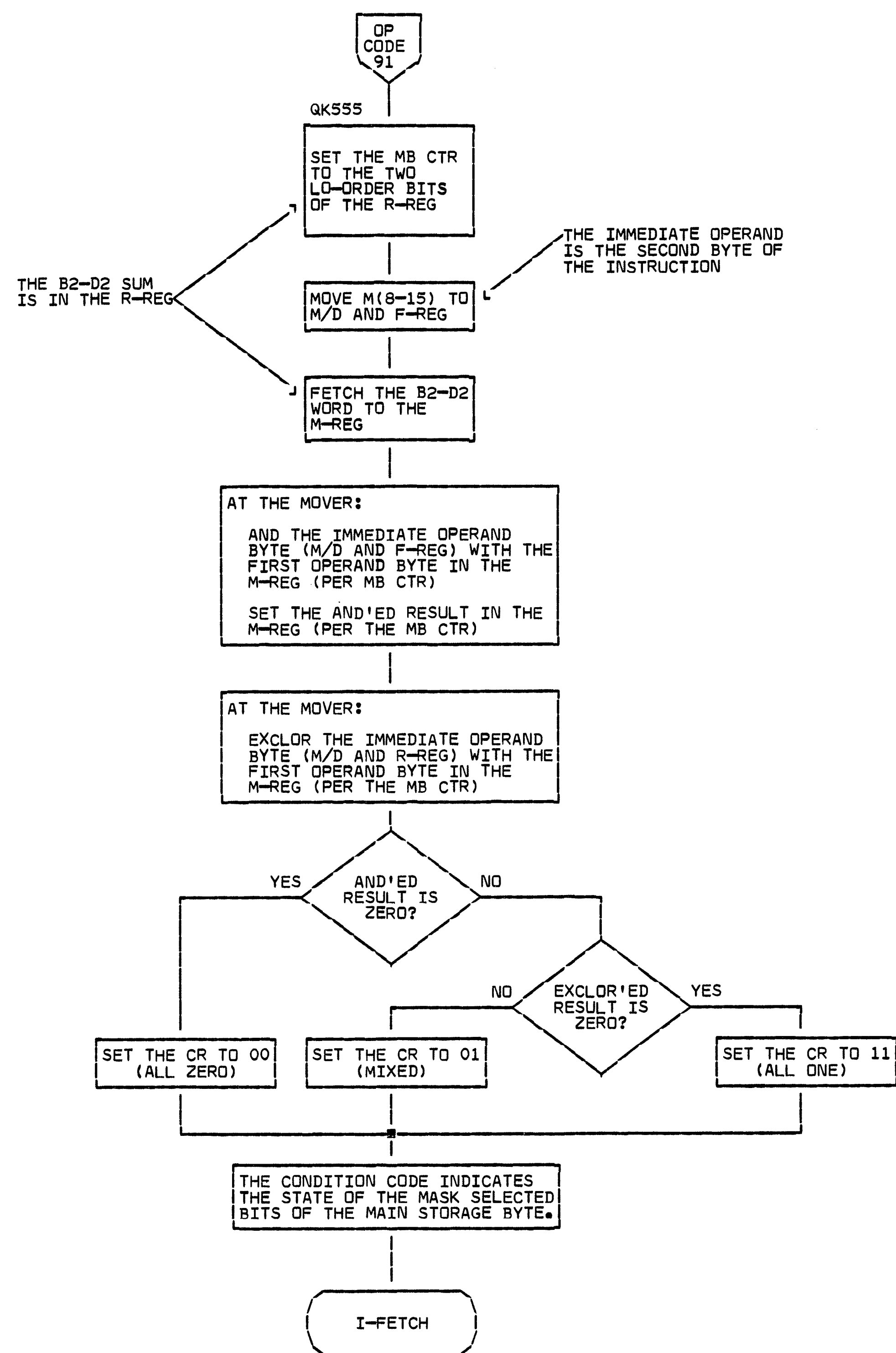
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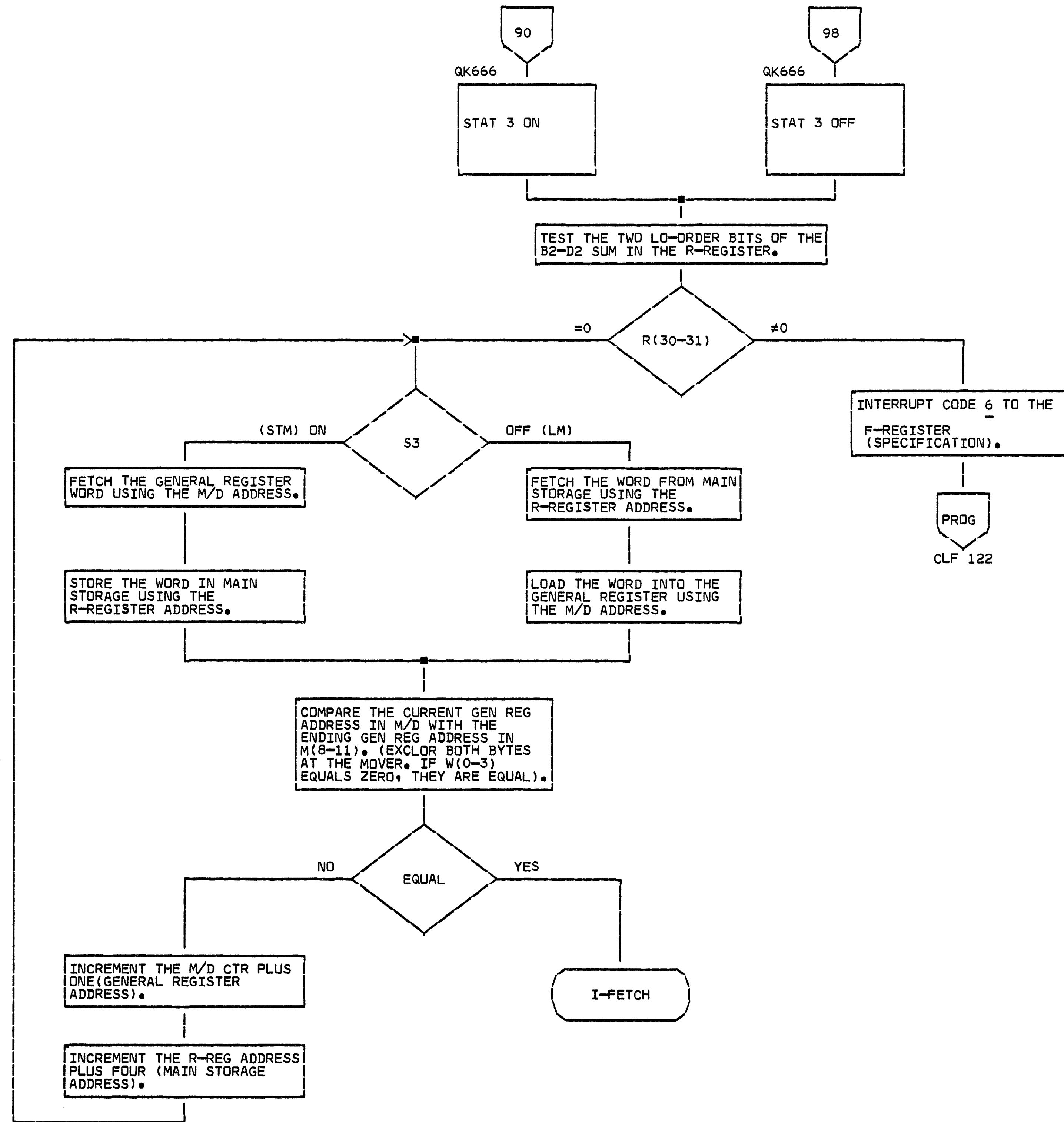




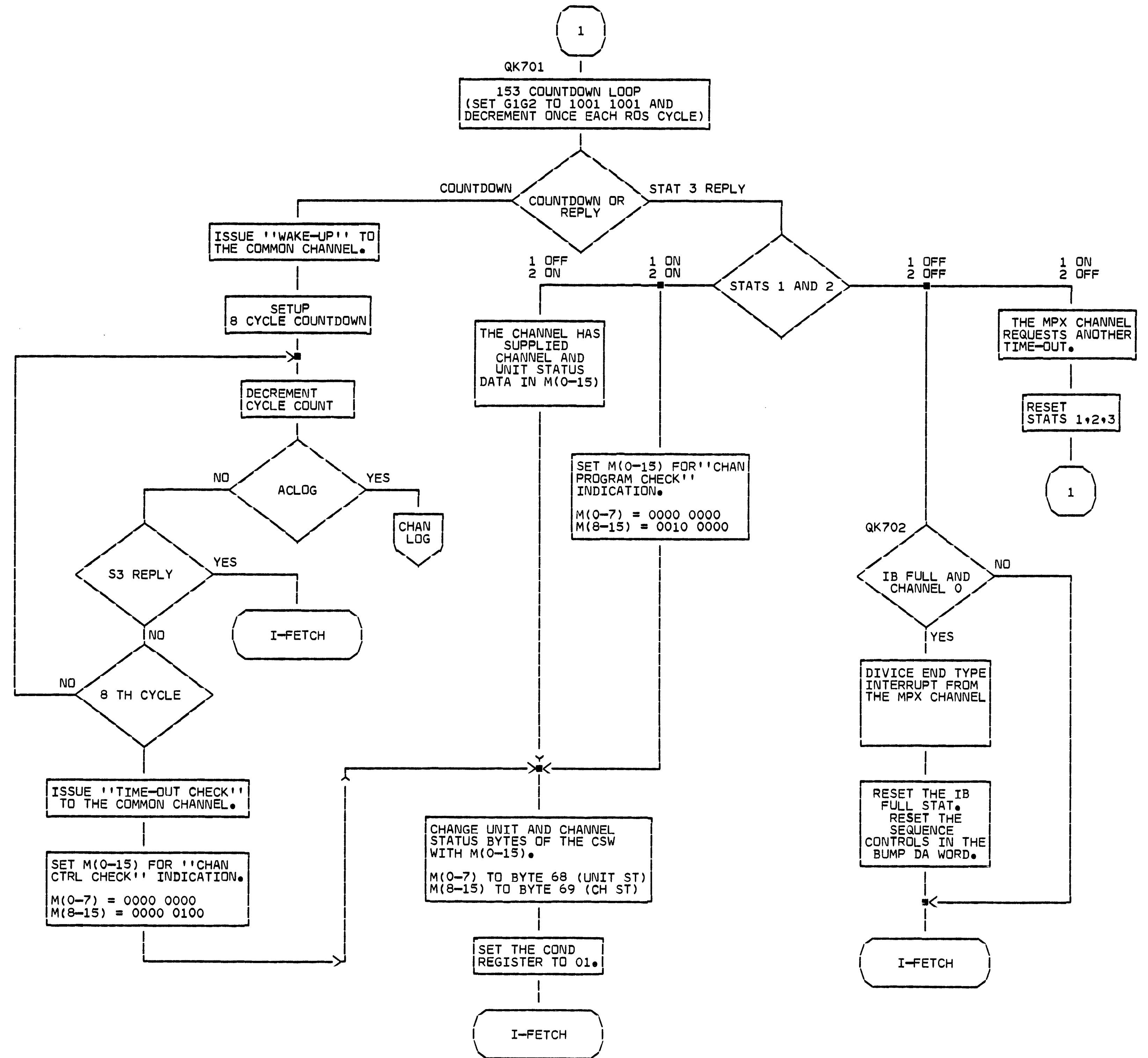
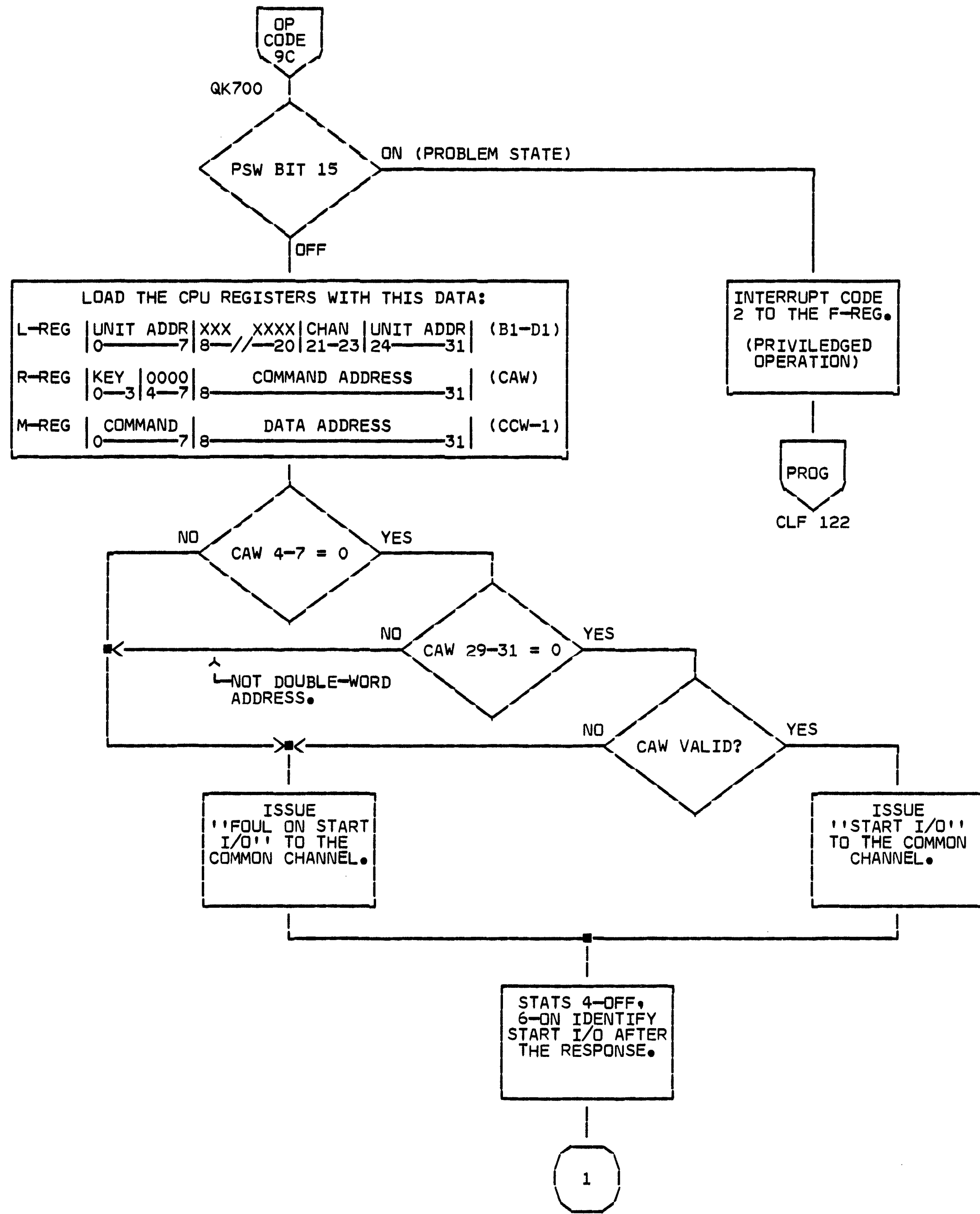
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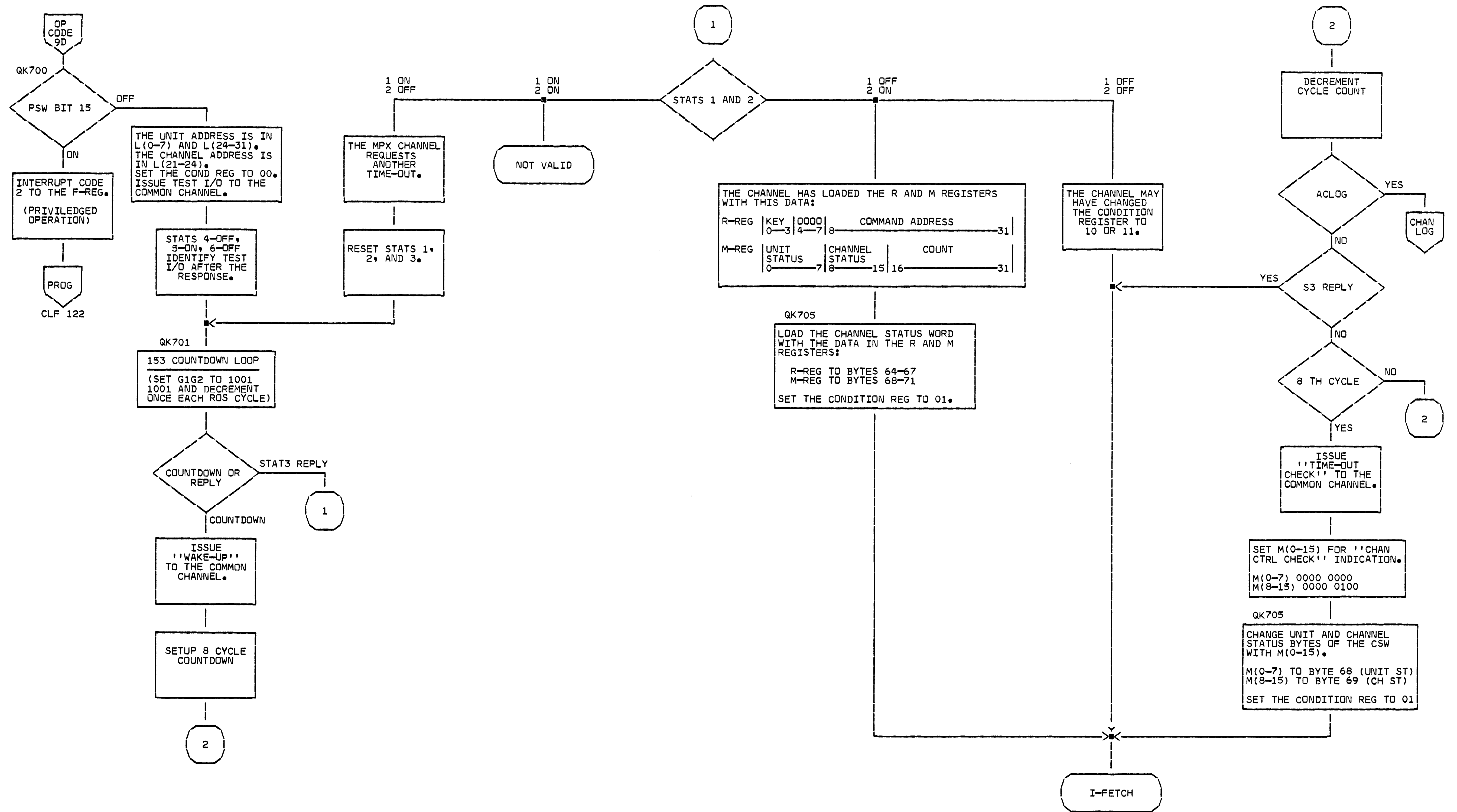


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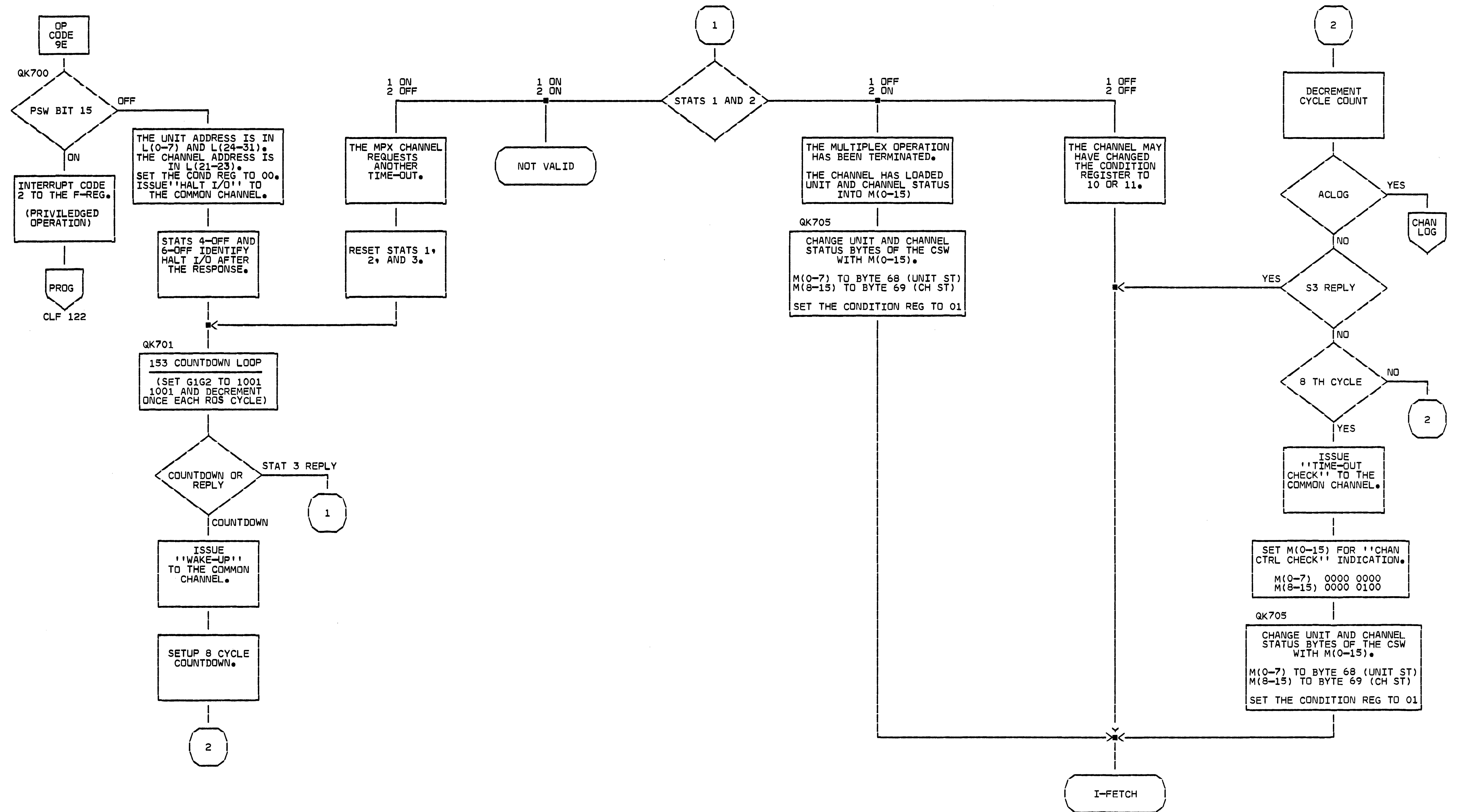
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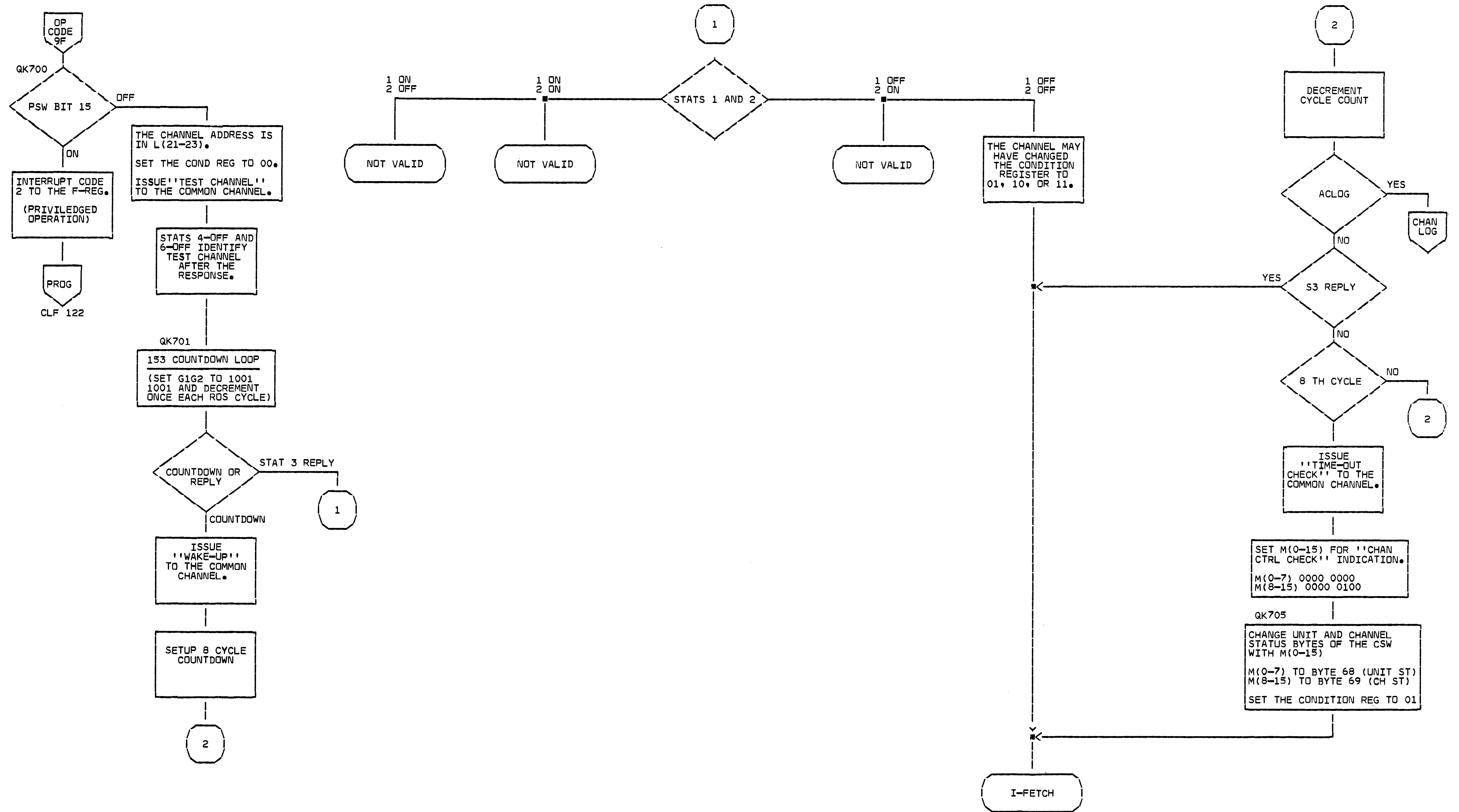
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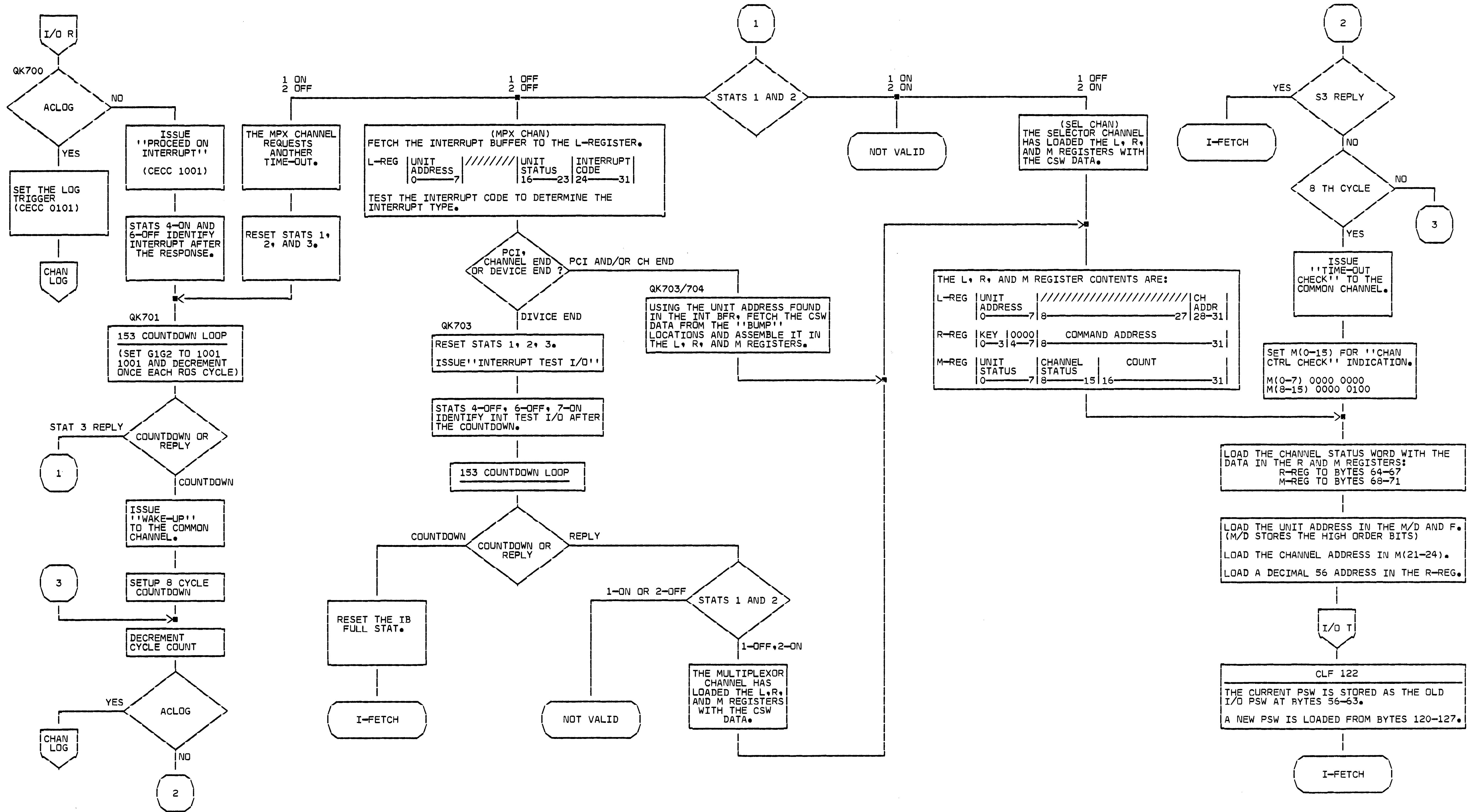
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(MPX CHAN)  
FETCH THE INTERRUPT BUFFER TO THE L-REGISTER.  
TEST THE INTERRUPT CODE TO DETERMINE THE INTERRUPT TYPE.

L-REG	UNIT ADDRESS	////////	UNIT STATUS	INTERRUPT CODE
	0-7		16-23	24-31

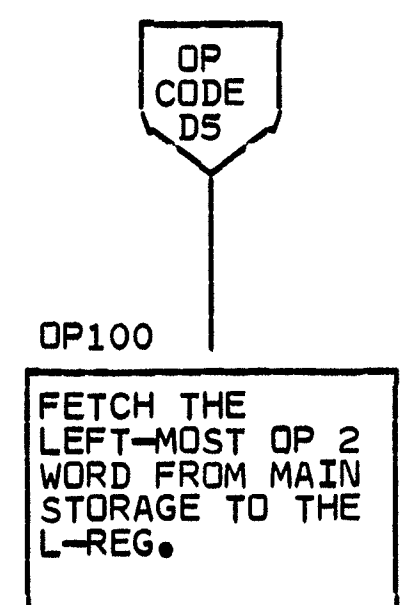
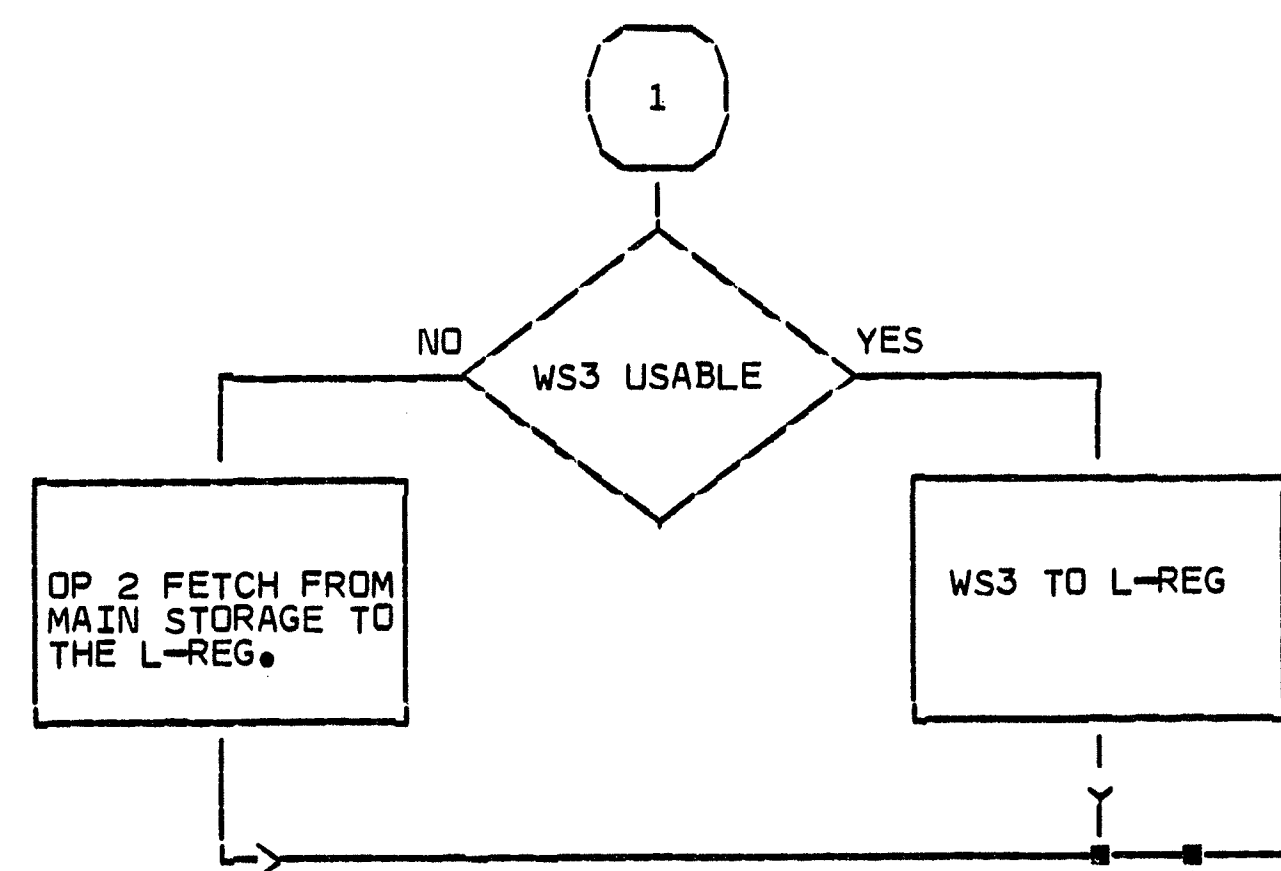
THE L, R, AND M REGISTER CONTENTS ARE:

L-REG	UNIT ADDRESS	//////////	CH ADDR
	0-7	8-27	28-31
R-REG	KEY	COMMAND ADDRESS	
	0-3	4-7	8-31
M-REG	UNIT STATUS	CHANNEL STATUS	COUNT
	0-7	8-15	16-31

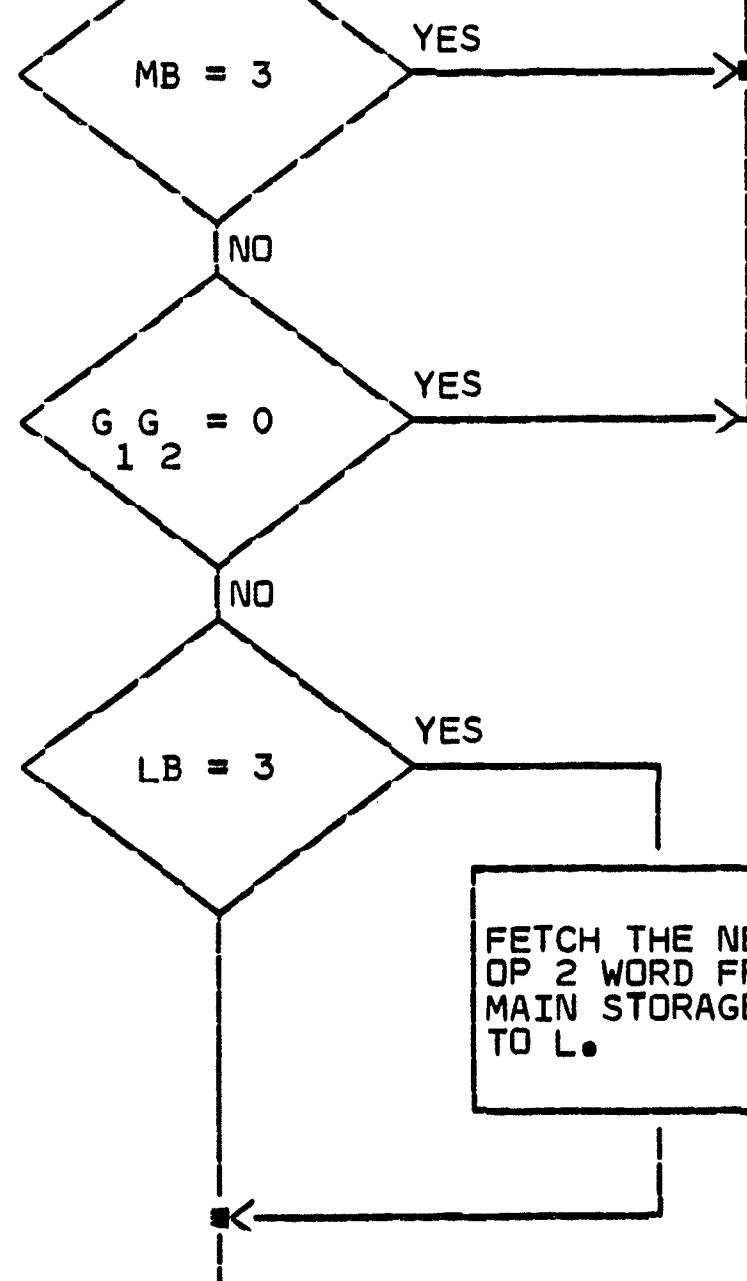
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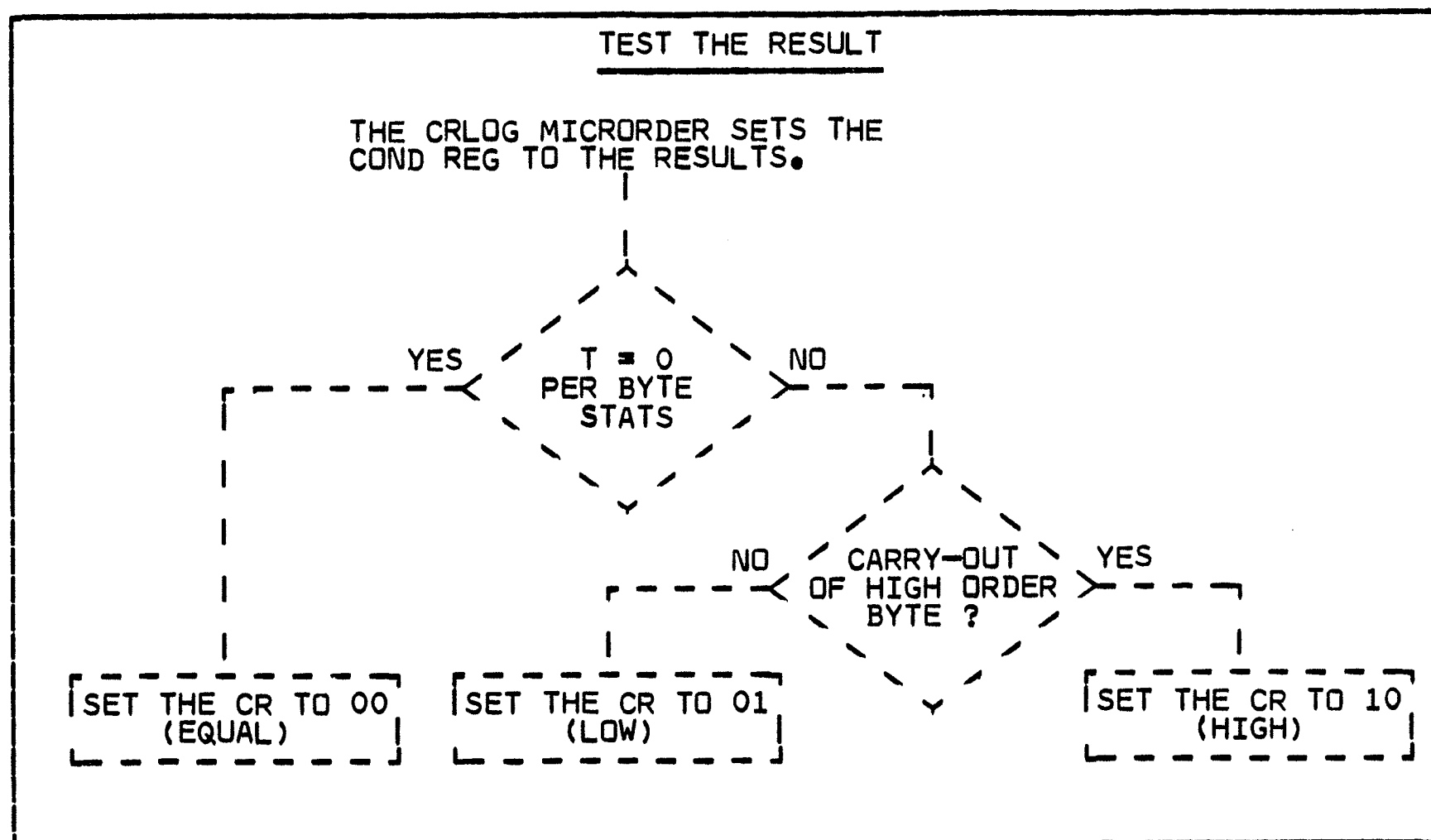
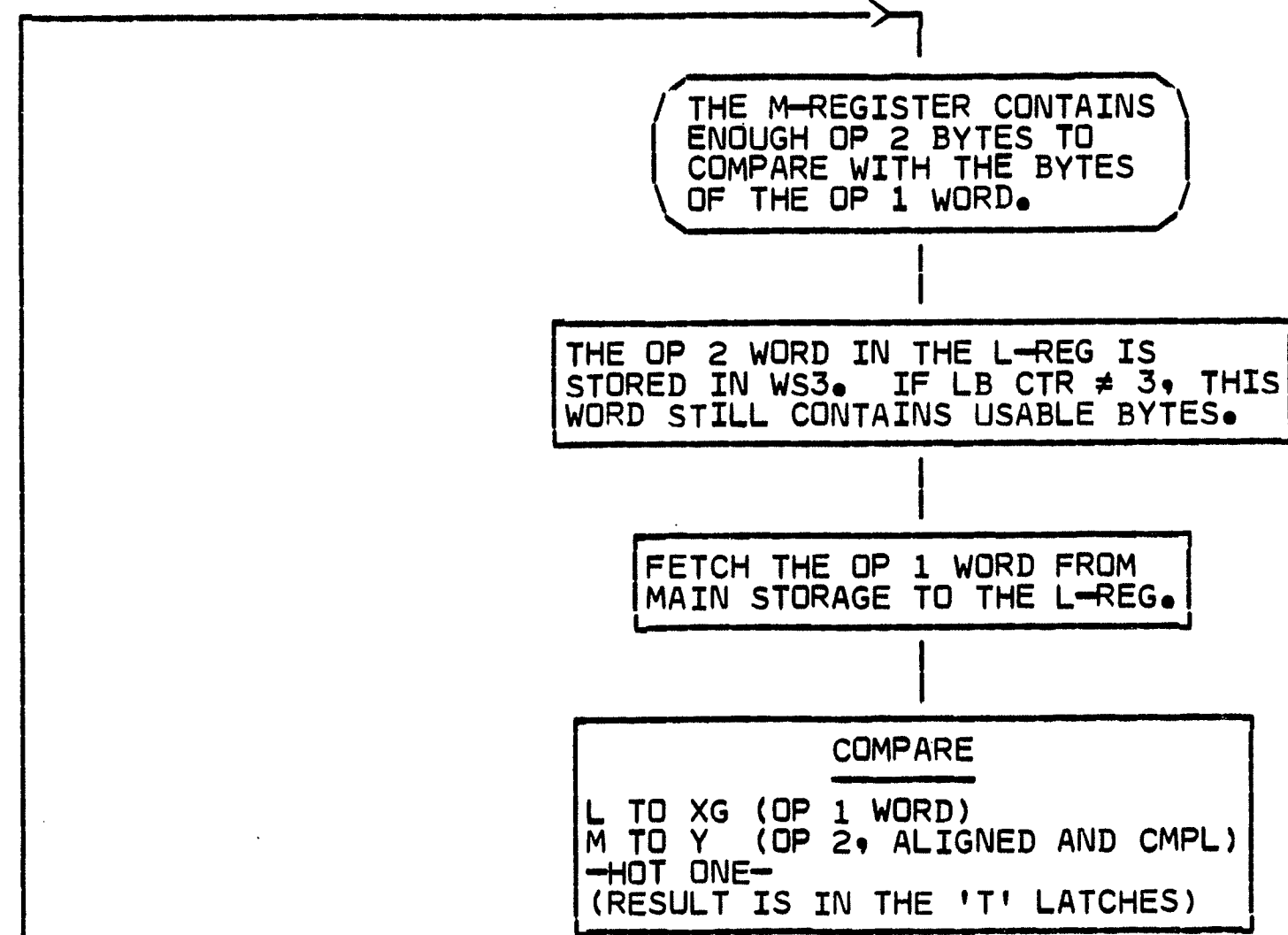




COMPLEMENT AND BYTE ALIGN THE OP 2 BYTE FROM THE L-REG. TO THE CORRESPONDING OP 1 BYTE POSITION IN THE M-REG.  
 L (PER LB CTR) TO U (OP 2 BYTE)  
 M (PER MB CTR) TO V (ALL 1-BITS)  
 -EXCLOR-  
 W TO M (PER MB CTR)



SET THE BYTE STAT PER THE MB CTR. INCREMENT LB AND MB CTRS BY +1. DECREMENT GG COUPLED BY -1.  
 1 2



COMPARE LOGICAL IS A BINARY COMPARE OF TWO FIELDS IN MAIN STORAGE. BOTH FIELDS ARE SCANNED FROM LEFT TO RIGHT UNTIL AN UNEQUAL (T 0) IS FOUND OR UNTIL BOTH FIELDS HAVE BEEN SCANNED (G 0).

LOW  
↓

SCAN →

OP 1	0000001010111000111000101001100
OP 2	000000101011100011100101000100

EACH FIELD MAY BE UP TO 256 BYTES LONG AND MAY NOT BE BYTE ALIGNED ON WORD BOUNDARIES.

IN MAIN STORAGE:

OP 1	0 1 5 C 7 1   4 C
OP 2	0 1 5 C 7 9 4 4

THE OP 1 WORD IS COMPARED A WORD AT A TIME JUST AS IT IS FOUND IN MAIN STORAGE. THE BYTES OF THE OP 2 FIELD ARE BYTE ALIGNED TO THE OP 1 FIELD.

OP 2 BYTE ALIGNED

	0 1 5 C 7 9	(BOTH WORDS HAD TO BE FETCHED FROM MAIN STORAGE)
--	-------------	--

OP 2 BYTES ARE COMPLEMENTED AND BYTE ALIGNED IN THE M-REG FOR COMPARISON WITH THE OP 1 WORD WHEN IT IS FETCHED FROM MAIN STORAGE.

OP 2 BYTE ALIGNED AND COMPL. IN THE M-REG

M-REG	FFFEA386 (OP 2 ALIGNED AND C)
L-REG	XX015C71 (OP 1 WORD)
	1 (HOT ONE)
RESULT	FFFFF8 (NOT ZERO) (NO CARRY OUT)

THE OP 1 BYTES WERE HI, LO, OR EQ TO THE OP 2 BYTES.

**COUNTERS AND REGISTERS**

**LB CTR:**  
 SET TO THE TWO LOW-ORDER BITS OF THE OP 2 ADDR. CONTROLS L-REG OUTGATES. PLUS ONE AS EACH BYTE IS ASSEMBLED.

**MB CTR:**  
 SET TO THE TWO LOW-ORDER BITS OF THE OP 1 ADDR. CONTROLS THE M-REG OUTGATING AND INGATING. PLUS ONE AS EACH BYTE IS ASSEMBLED.

**GG COUPLED:**  
 1 2

SET TO THE INSTRUCTIONS LENGTH FIELD. COUNTS THE NUMBER OF REMAINING BYTES. MINUS ONE AS EACH BYTE IS ASSEMBLED.

**BYTE STATS:**  
 SET FROM THE MB CTR. CONTROLS CRLOG ZERO/CARRY TESTING.

**WS 1:**  
 HOLDS THE CURRENT OP 1 ADDRESS.

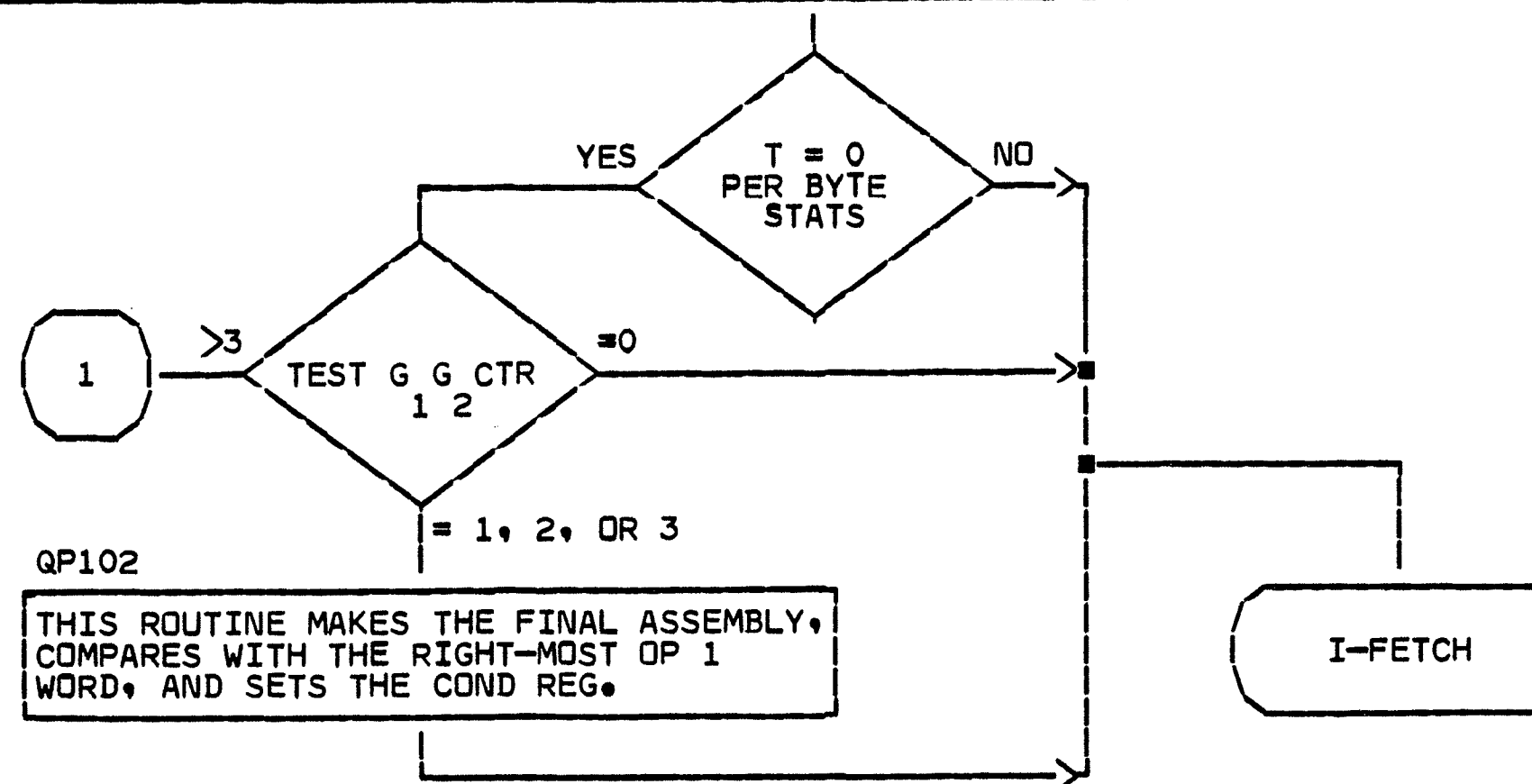
**WS 2:**  
 HOLDS THE CURRENT OP 2 ADDRESS.

**WS 3:**  
 TEMPORARY STORAGE FOR OP 2 WORD. IF LB CTR IS NOT THREE, THIS SAVES A MAIN STORAGE FETCH FOR THE REMAINING USABLE BYTES OF THIS WORD.

**L-REG:**  
 HOLDS THE OP 2 WORD DURING THE ASSEMBLY. HOLDS THE OP 1 WORD FOR THE COMPARE.

**M-REG:**  
 SET TO ALL ONES BEFORE THE ASSEMBLY. HOLDS THE BYTE ALIGNED/COMPLEMENTED OP 2.

**R-REG:**  
 USED AS AN ADDRESS REGISTER FOR OP 1/OP 2.

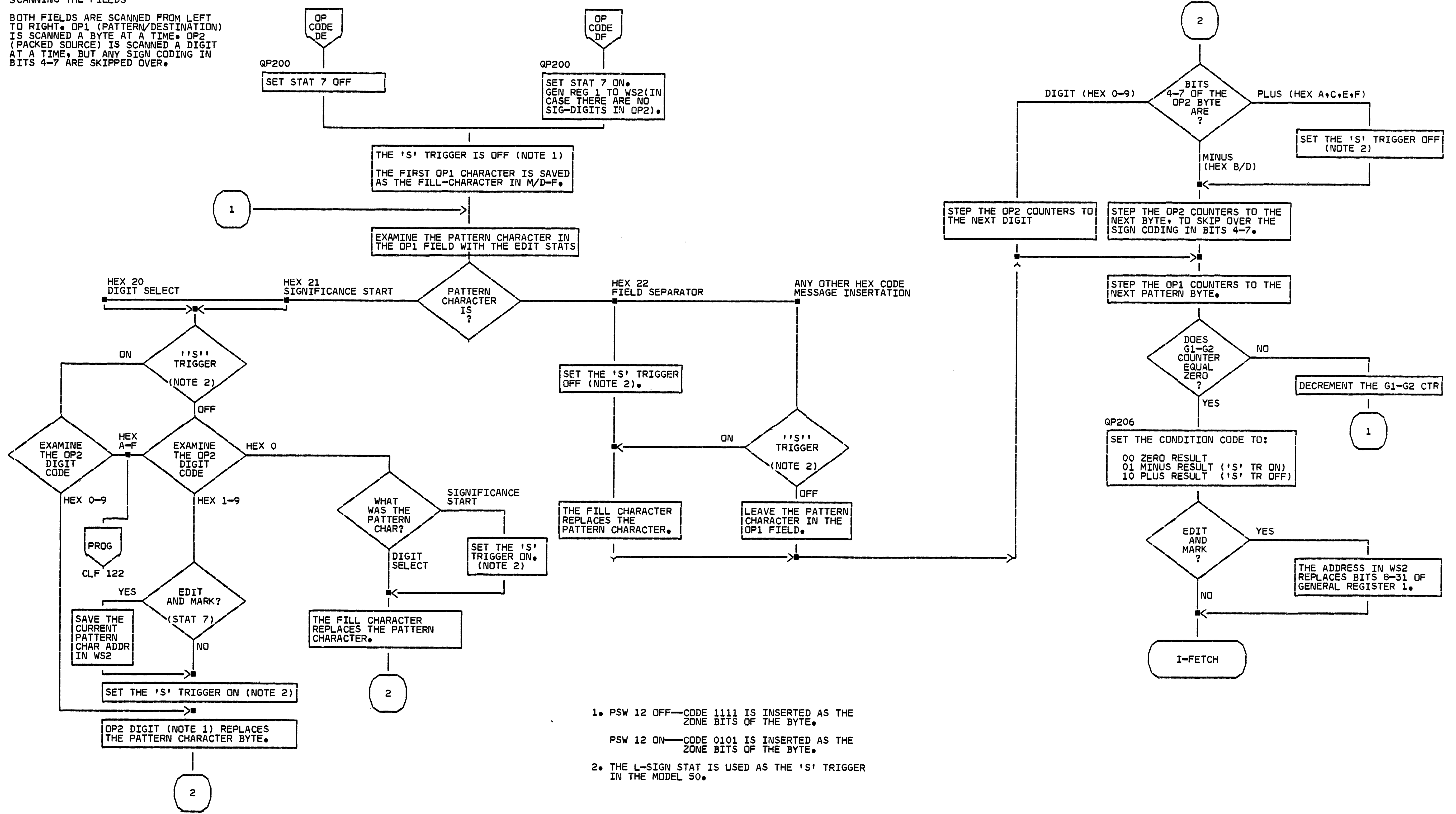


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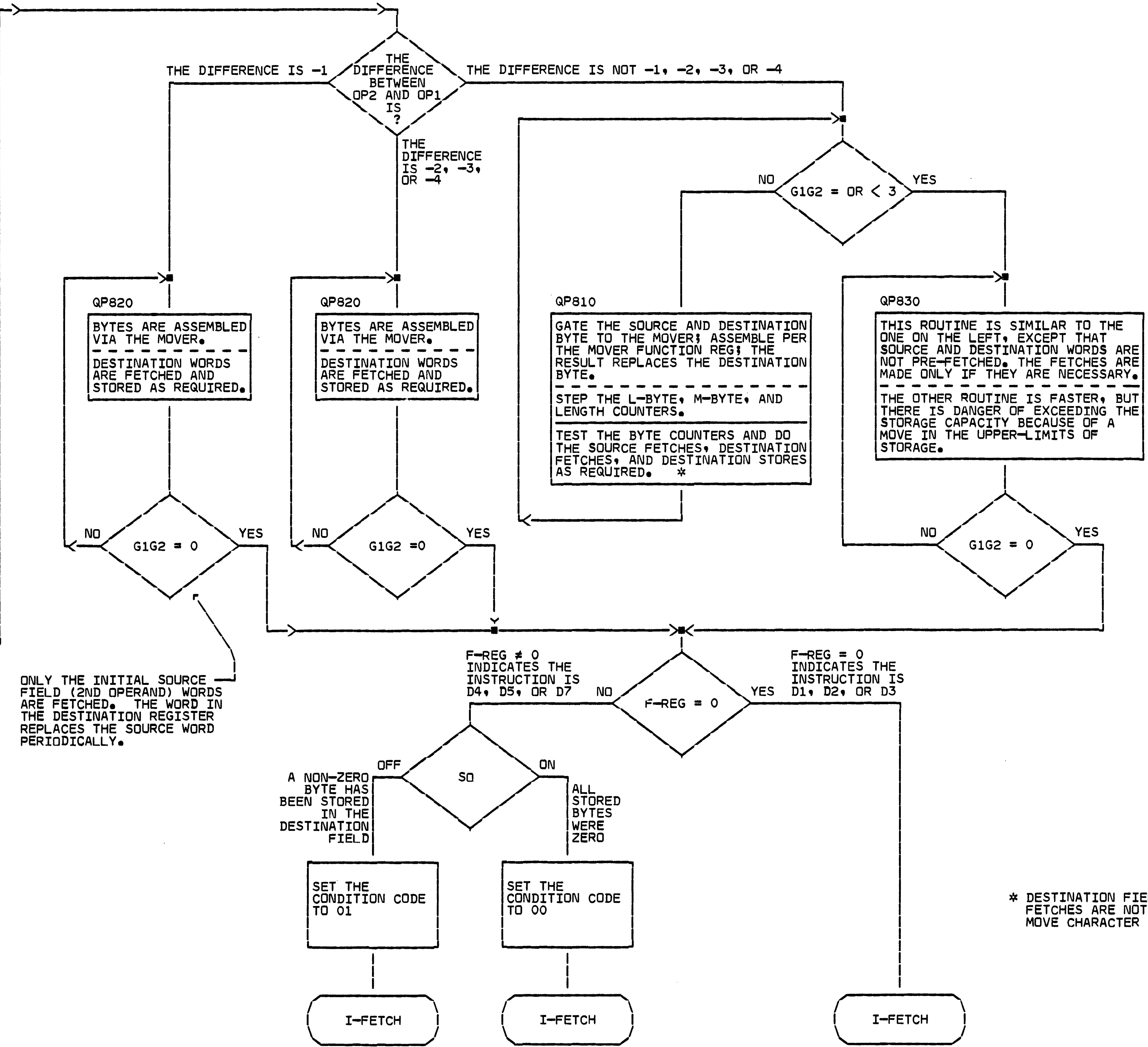
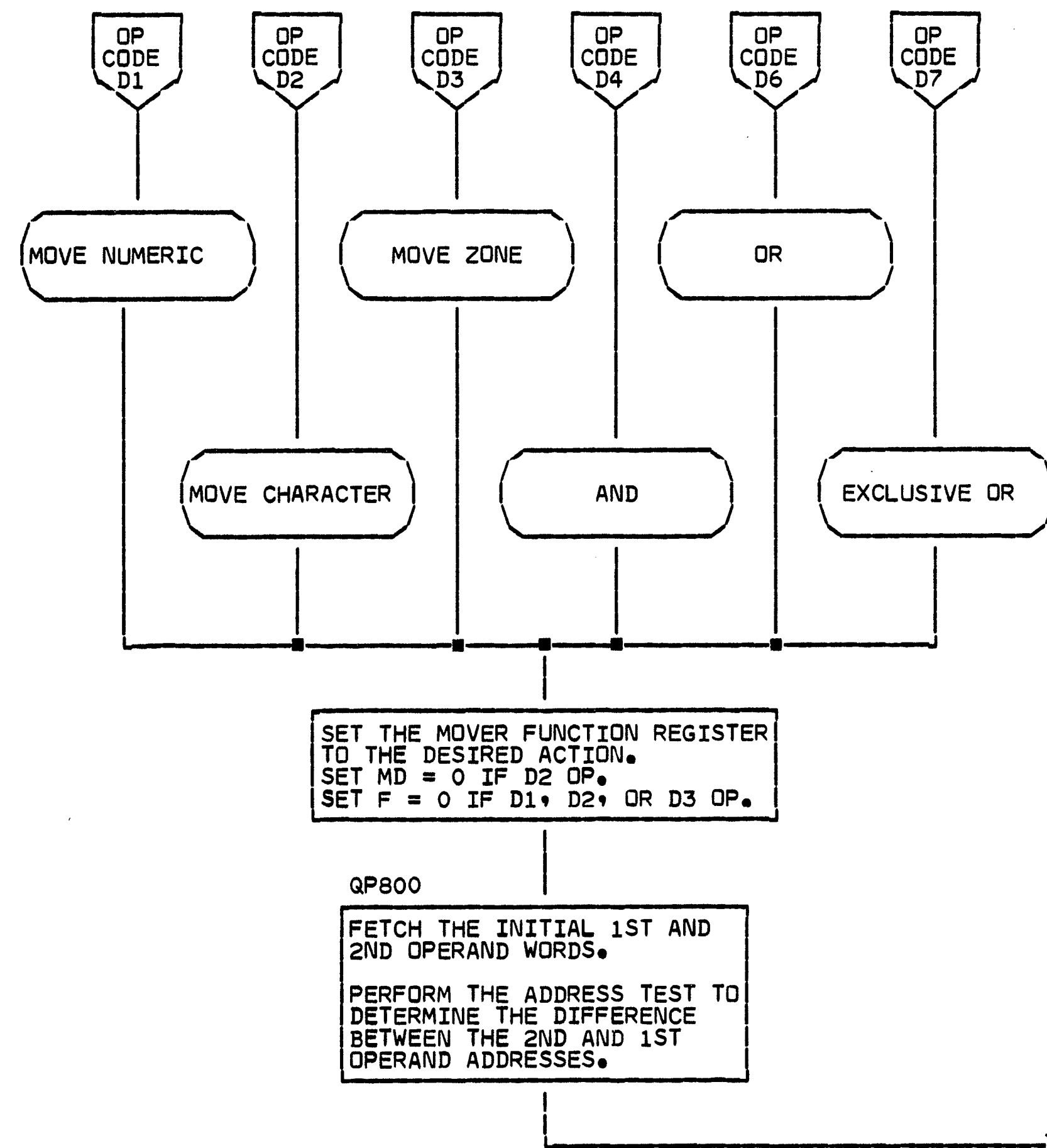
CLF 230  
 DATE 14 MAY 65 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE 2

SCANNING THE FIELDS

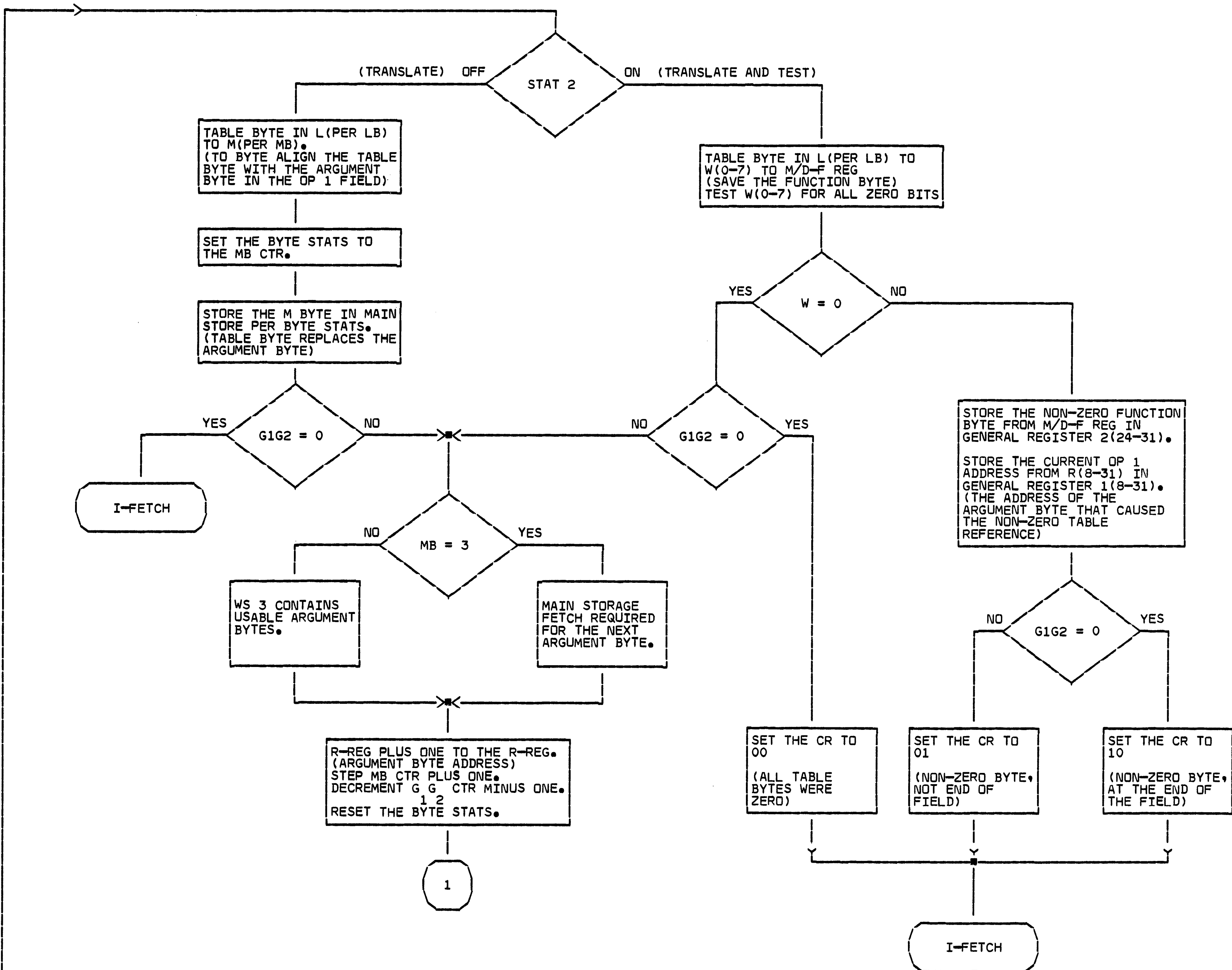
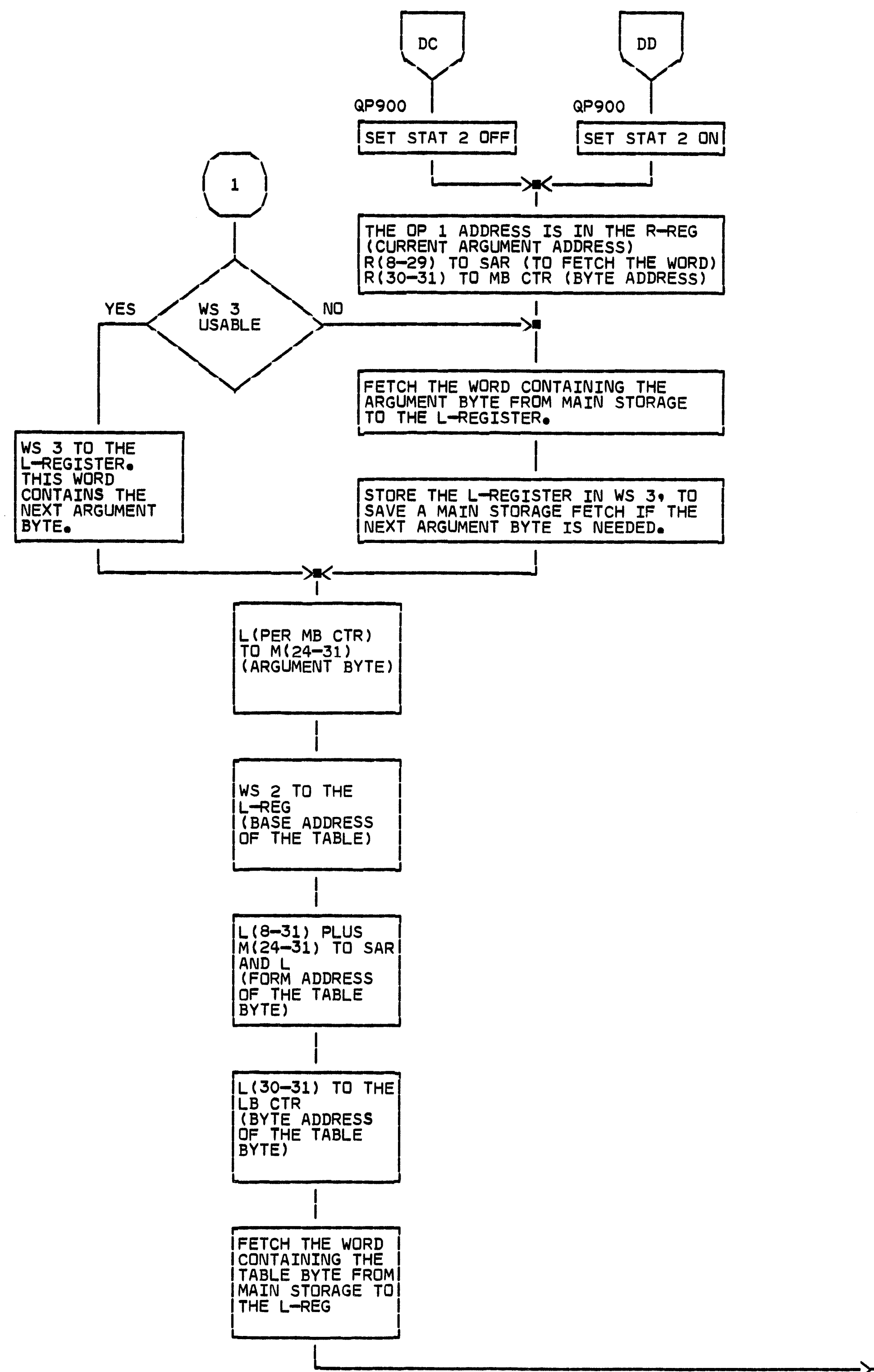
BOTH FIELDS ARE SCANNED FROM LEFT TO RIGHT. OP1 (PATTERN/DESTINATION) IS SCANNED A BYTE AT A TIME. OP2 (PACKED SOURCE) IS SCANNED A DIGIT AT A TIME, BUT ANY SIGN CODING IN BITS 4-7 ARE SKIPPED OVER.



- 1. PSW 12 OFF—CODE 1111 IS INSERTED AS THE ZONE BITS OF THE BYTE.  
PSW 12 ON—CODE 0101 IS INSERTED AS THE ZONE BITS OF THE BYTE.
- 2. THE L-SIGN STAT IS USED AS THE 'S' TRIGGER IN THE MODEL 50.

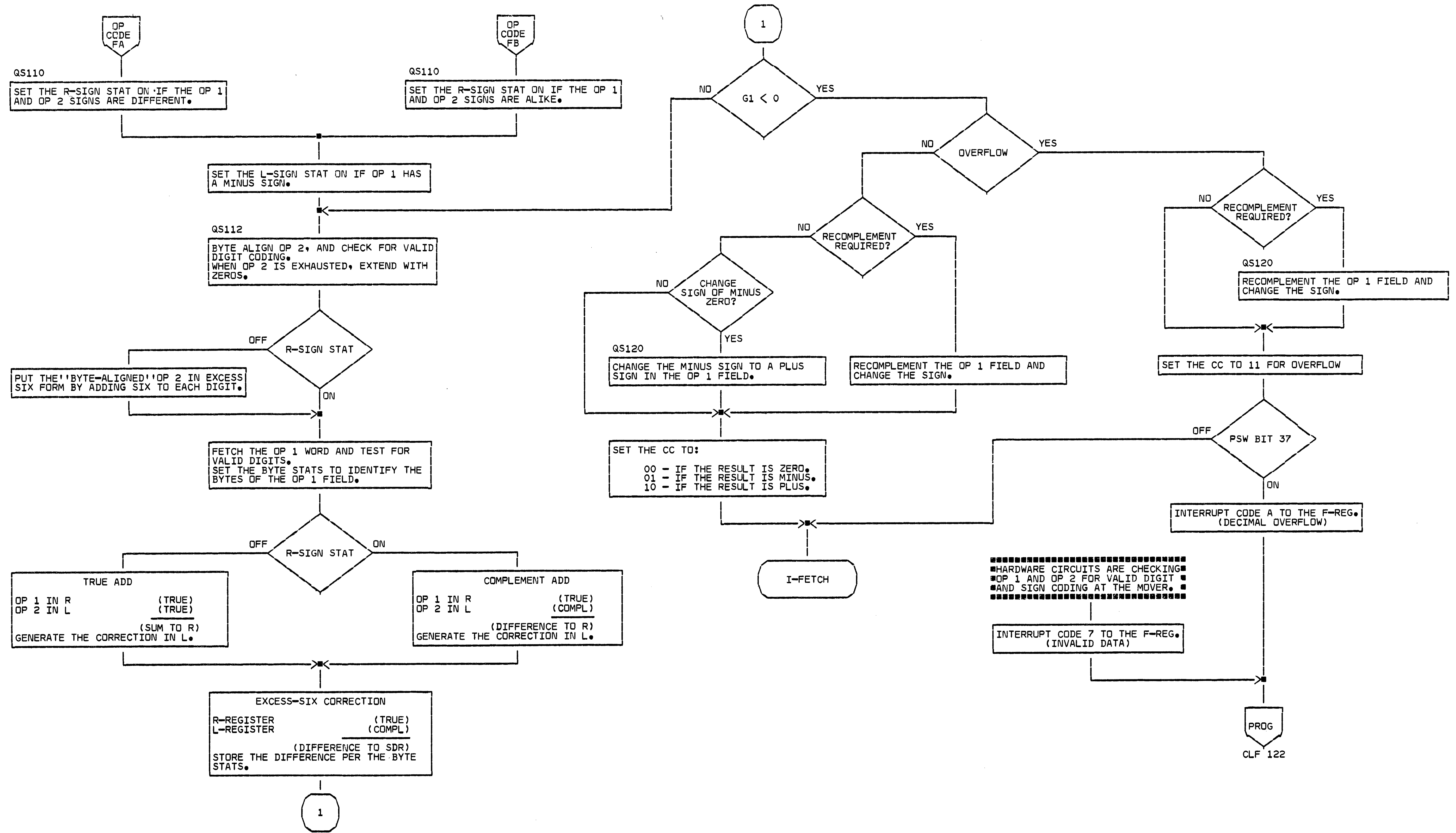


\* DESTINATION FIELD (1ST OPERAND) FETCHES ARE NOT REQUIRED FOR THE MOVE CHARACTER (D2) INSTRUCTION.



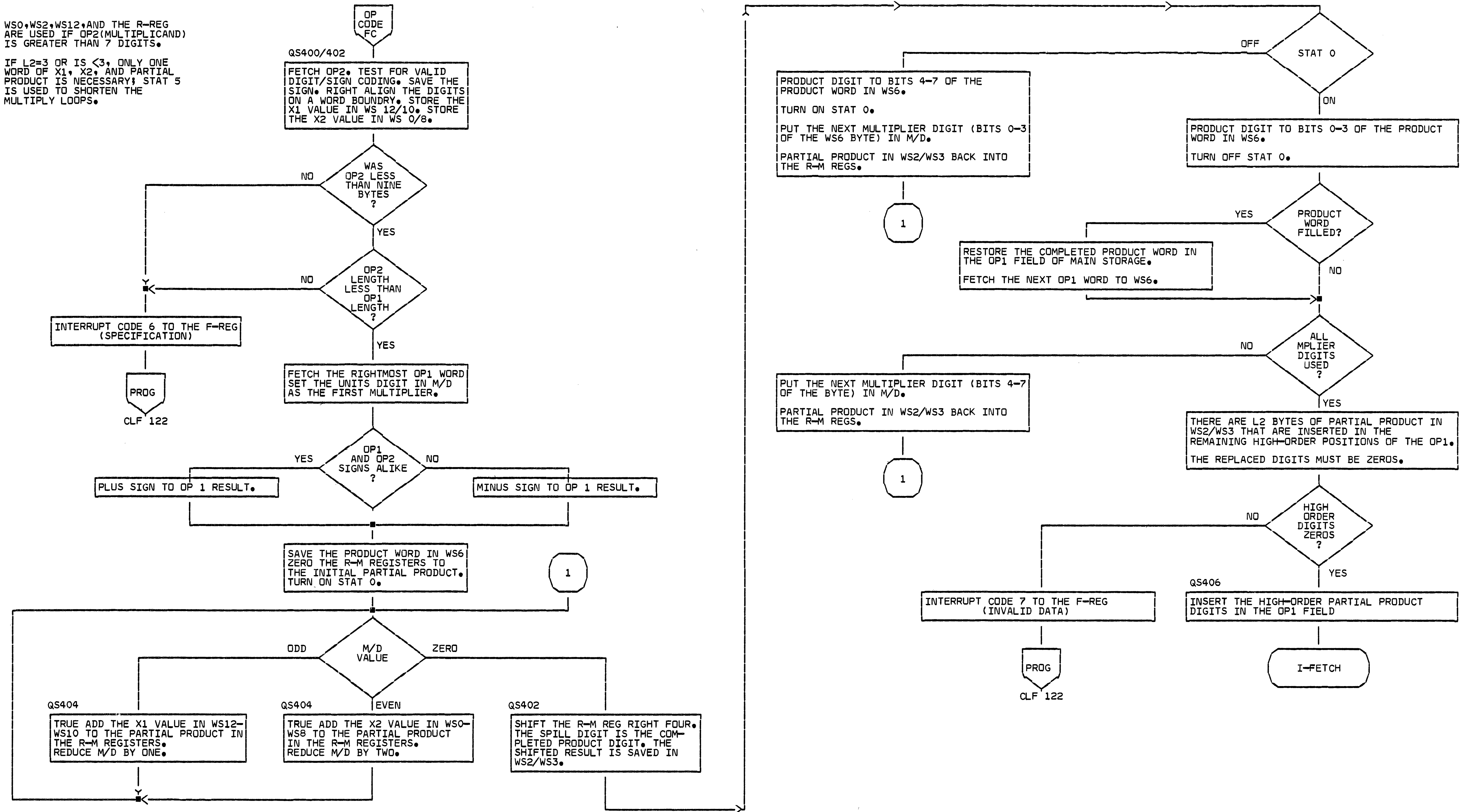
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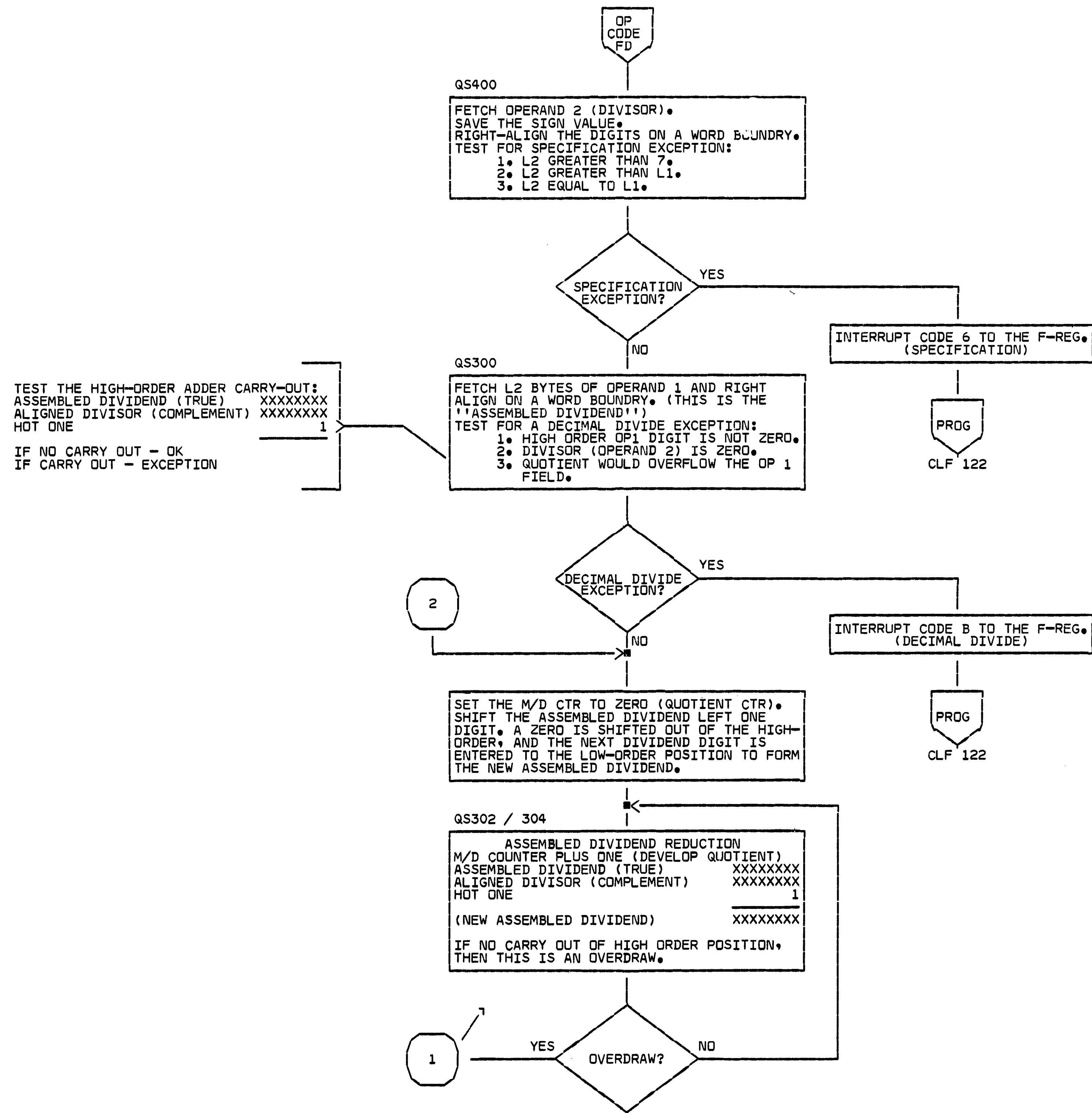
CLF 233  
 DATE 28 APR 65 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE 21



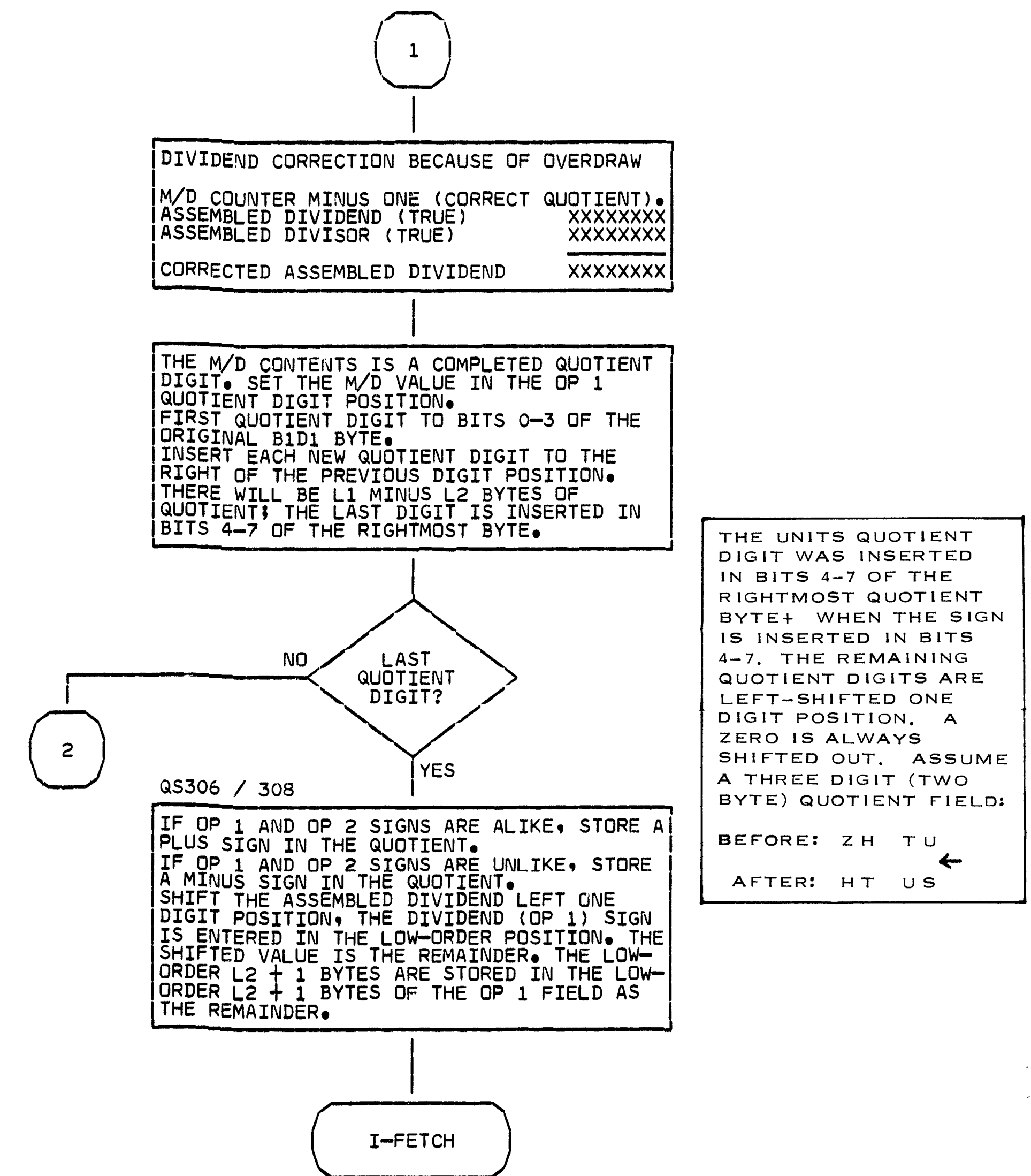
WS0, WS2, WS12, AND THE R-REG ARE USED IF OP2 (MULTIPLICAND) IS GREATER THAN 7 DIGITS.

IF L2=3 OR IS <3, ONLY ONE WORD OF X1, X2, AND PARTIAL PRODUCT IS NECESSARY; STAT 5 IS USED TO SHORTEN THE MULTIPLY LOOPS.



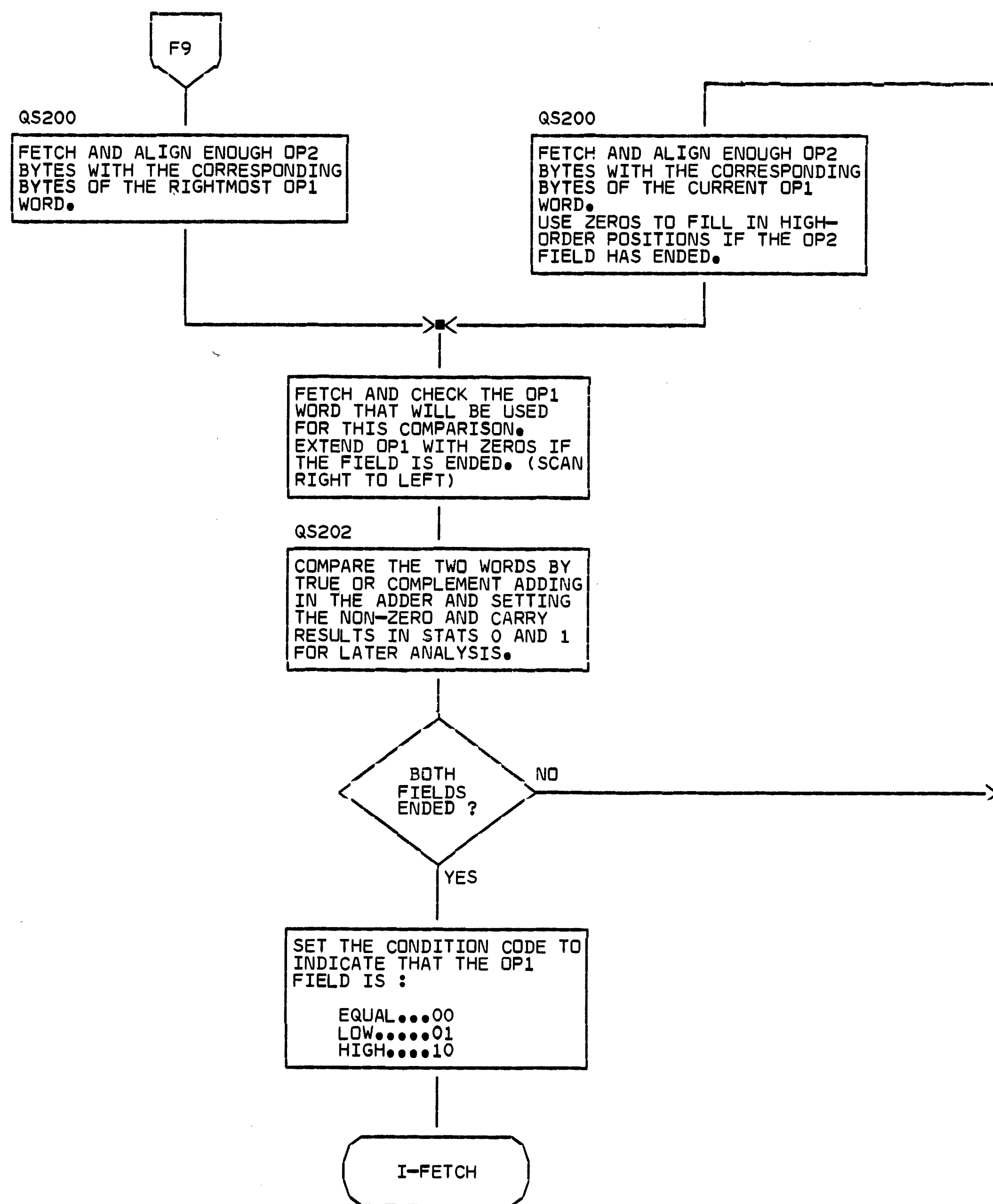


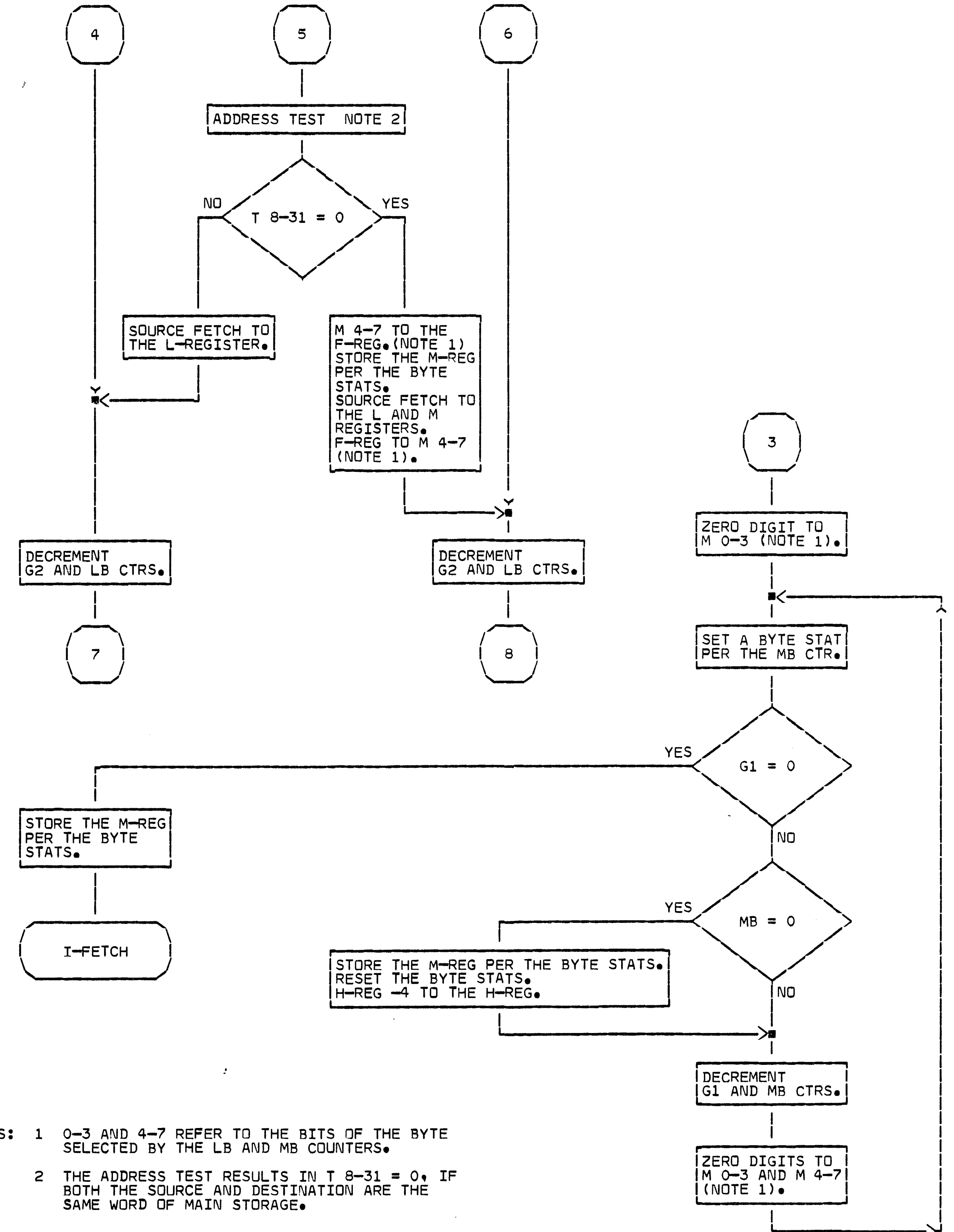
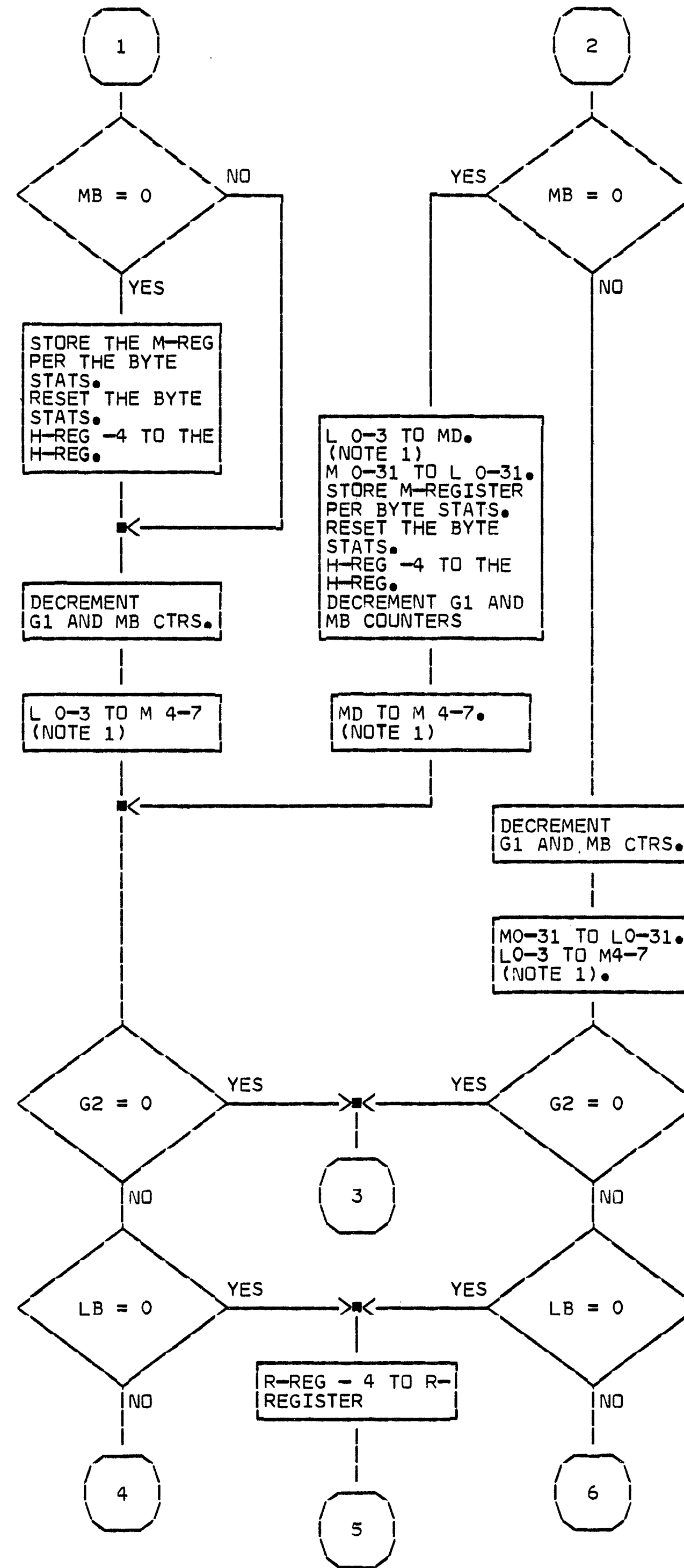
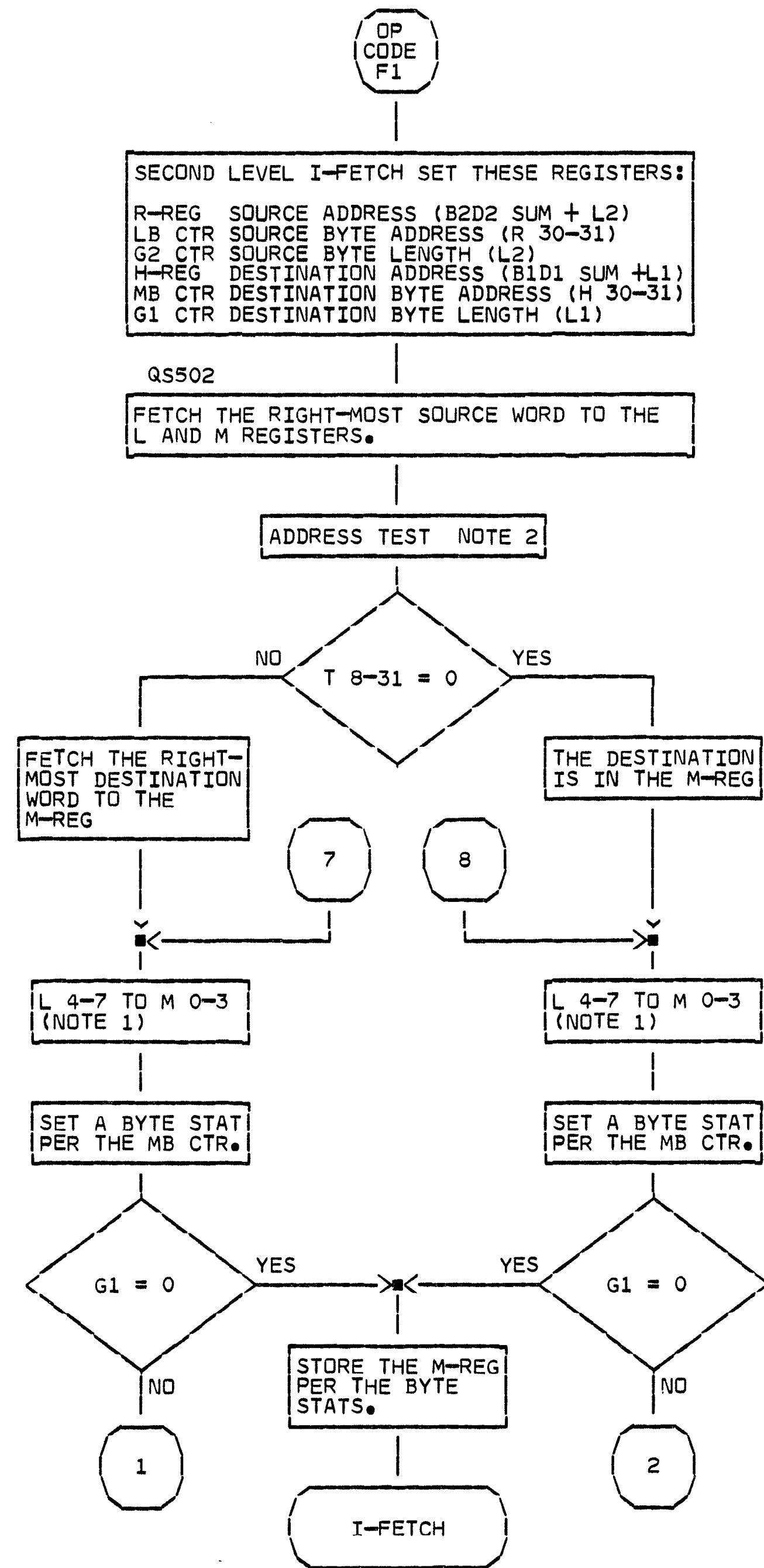
TEST THE HIGH-ORDER ADDER CARRY-OUT:  
ASSEMBLED DIVIDEND (TRUE) XXXXXXXX  
ALIGNED DIVISOR (COMPLEMENT) XXXXXXXX  
HOT ONE 1  
IF NO CARRY OUT - OK  
IF CARRY OUT - EXCEPTION



THE UNITS QUOTIENT  
DIGIT WAS INSERTED  
IN BITS 4-7 OF THE  
RIGHTMOST QUOTIENT  
BYTE+ WHEN THE SIGN  
IS INSERTED IN BITS  
4-7. THE REMAINING  
QUOTIENT DIGITS ARE  
LEFT-SHIFTED ONE  
DIGIT POSITION. A  
ZERO IS ALWAYS  
SHIFTED OUT. ASSUME  
A THREE DIGIT (TWO  
BYTE) QUOTIENT FIELD:  
BEFORE: ZH TU  
AFTER: HT US ←

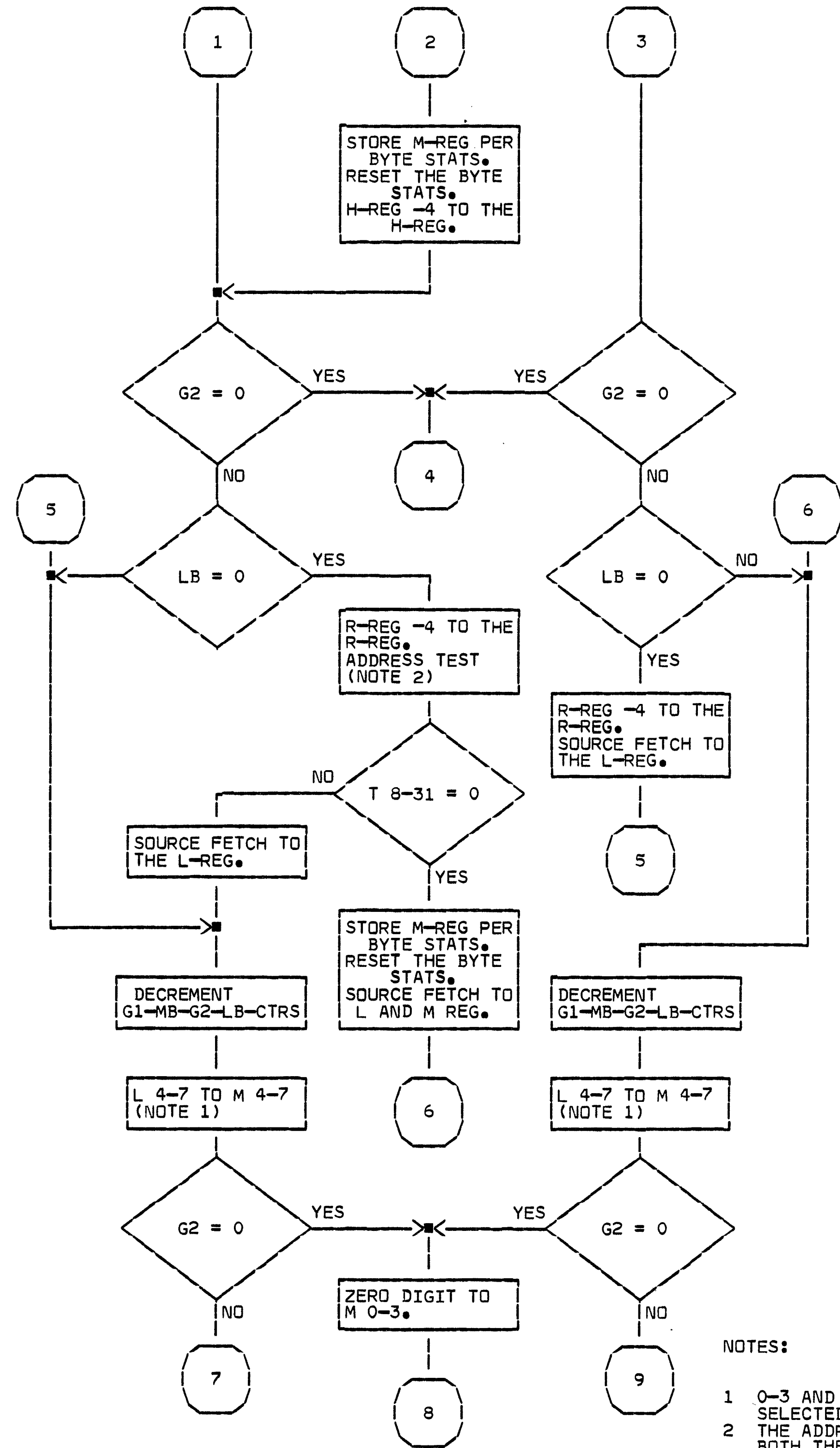
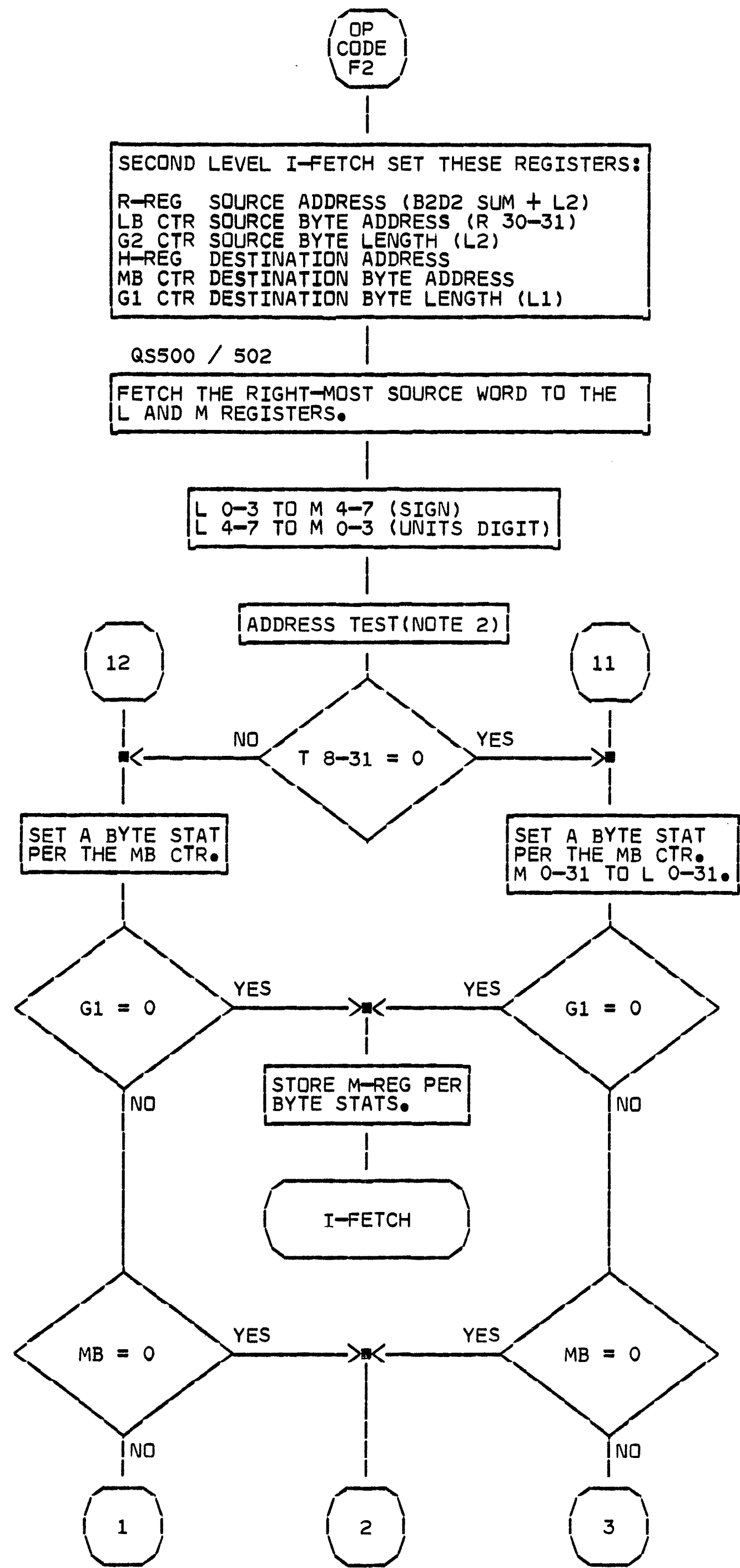




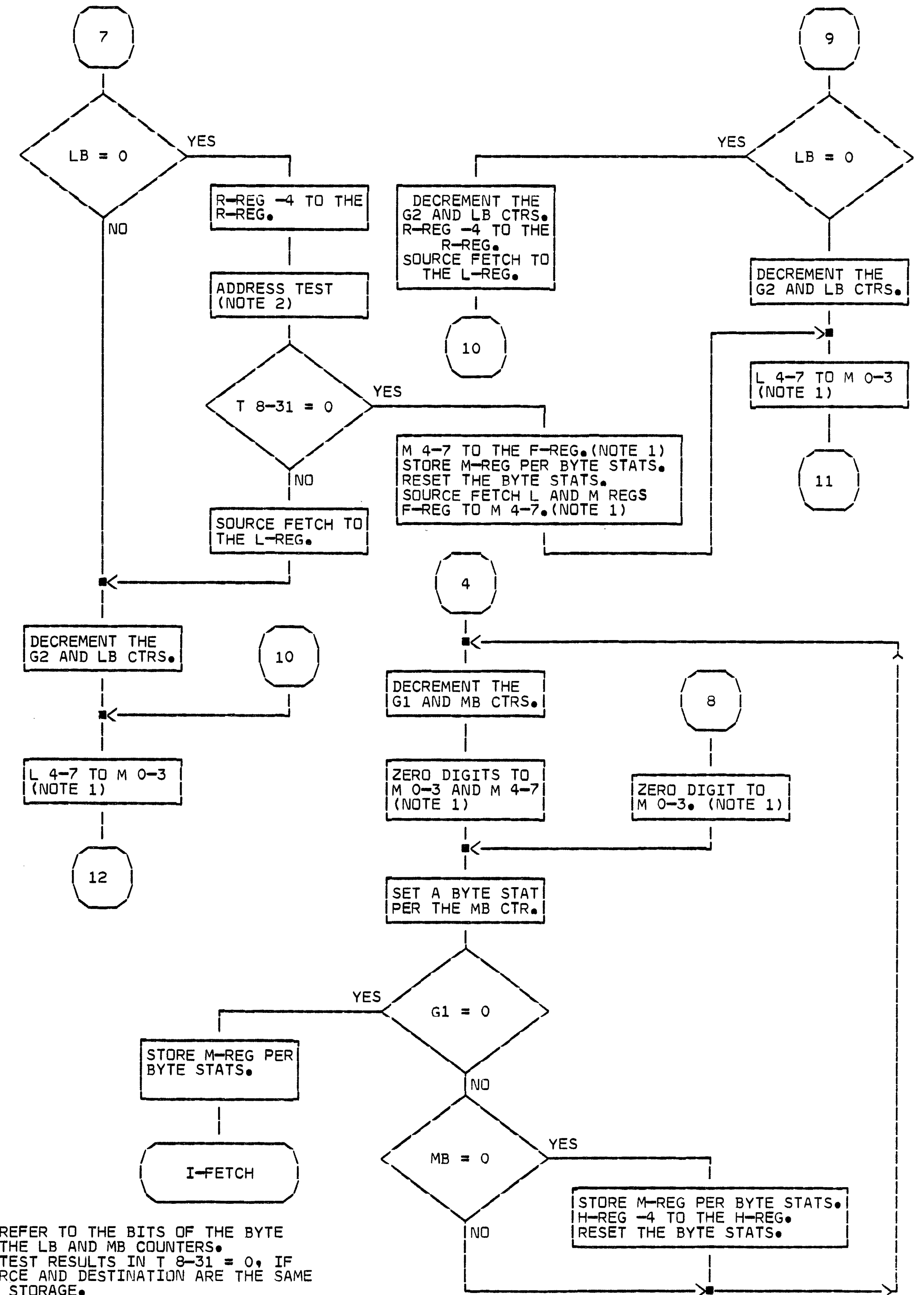


NOTES: 1 0-3 AND 4-7 REFER TO THE BITS OF THE BYTE SELECTED BY THE LB AND MB COUNTERS.  
 2 THE ADDRESS TEST RESULTS IN T 8-31 = 0, IF BOTH THE SOURCE AND DESTINATION ARE THE SAME WORD OF MAIN STORAGE.

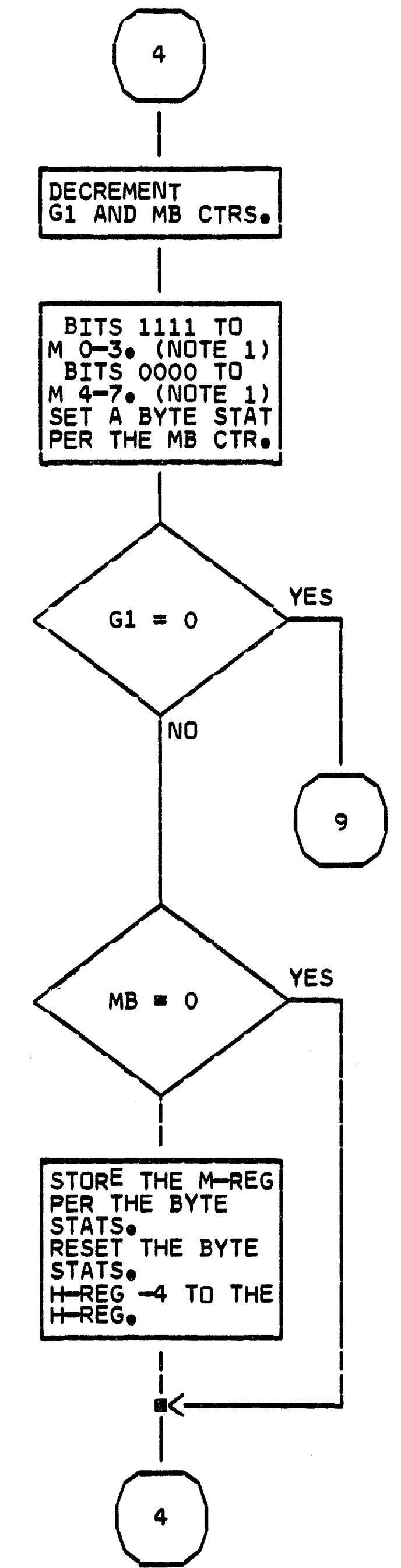
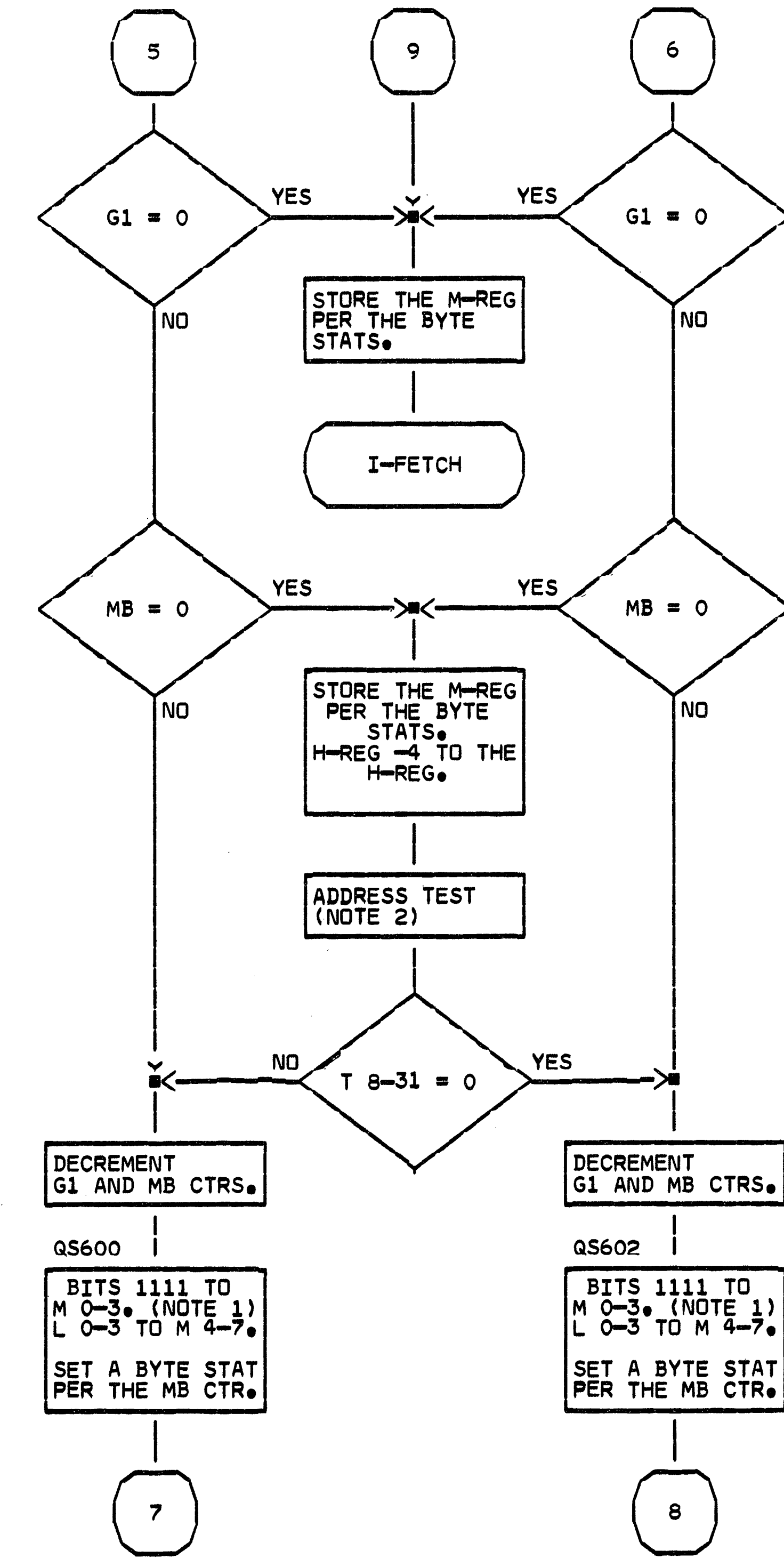
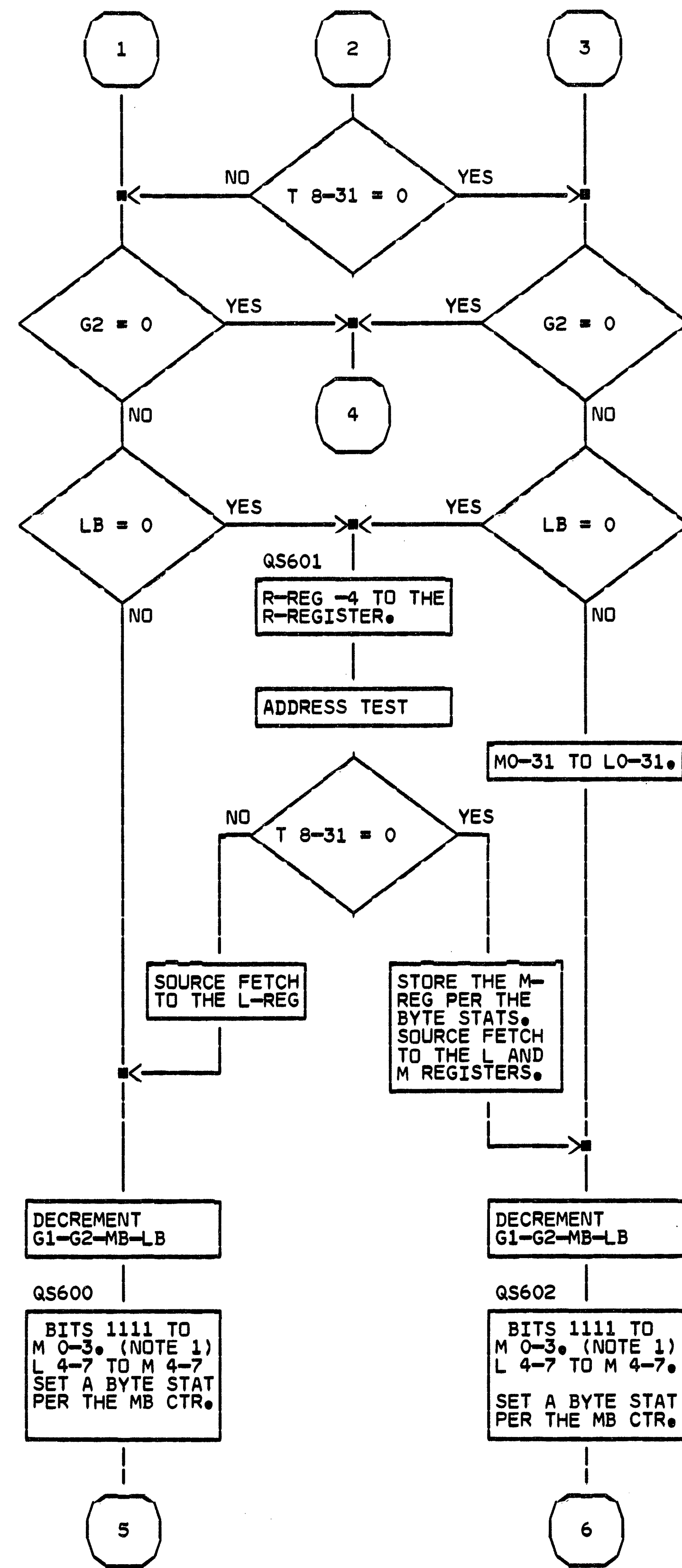
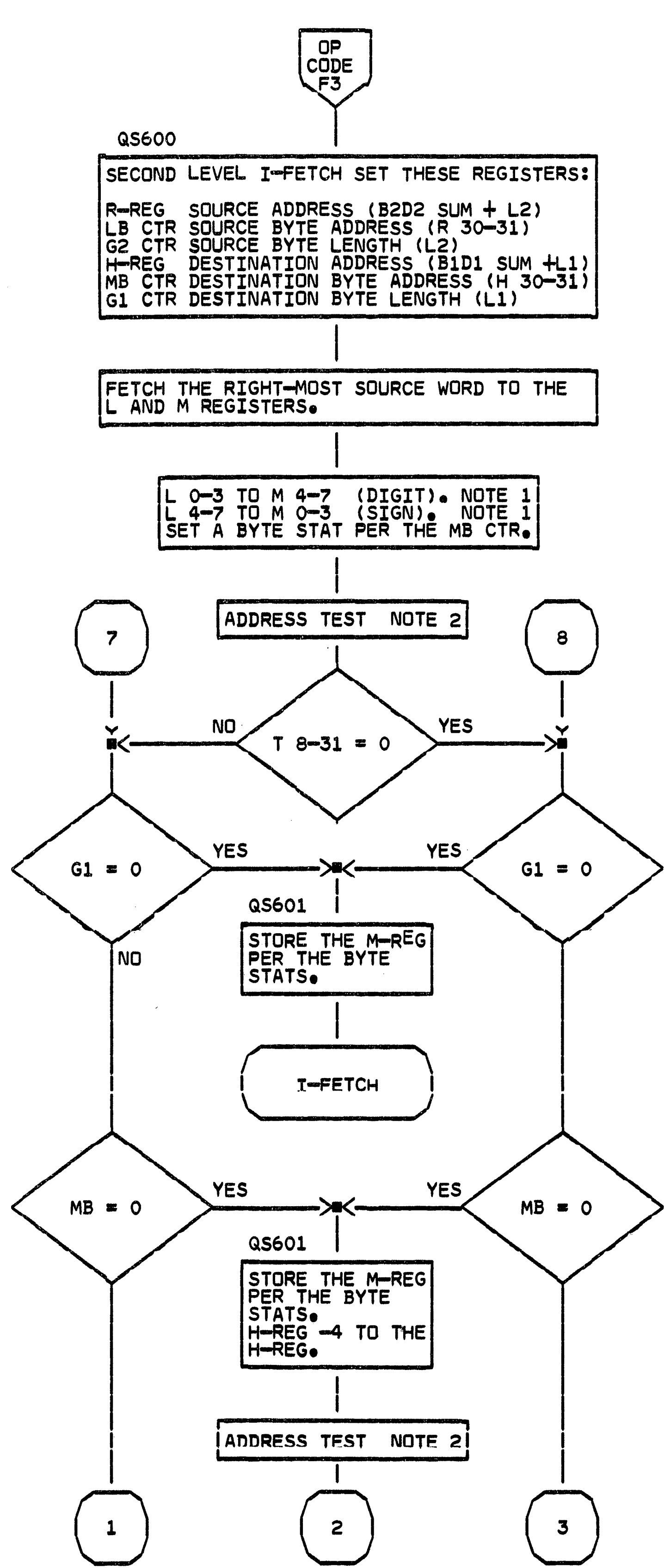
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NOTES:  
 1 0-3 AND 4-7 REFER TO THE BITS OF THE BYTE SELECTED BY THE LB AND MB COUNTERS.  
 2 THE ADDRESS TEST RESULTS IN T 8-31 = 0, IF BOTH THE SOURCE AND DESTINATION ARE THE SAME WORD OF MAIN STORAGE.



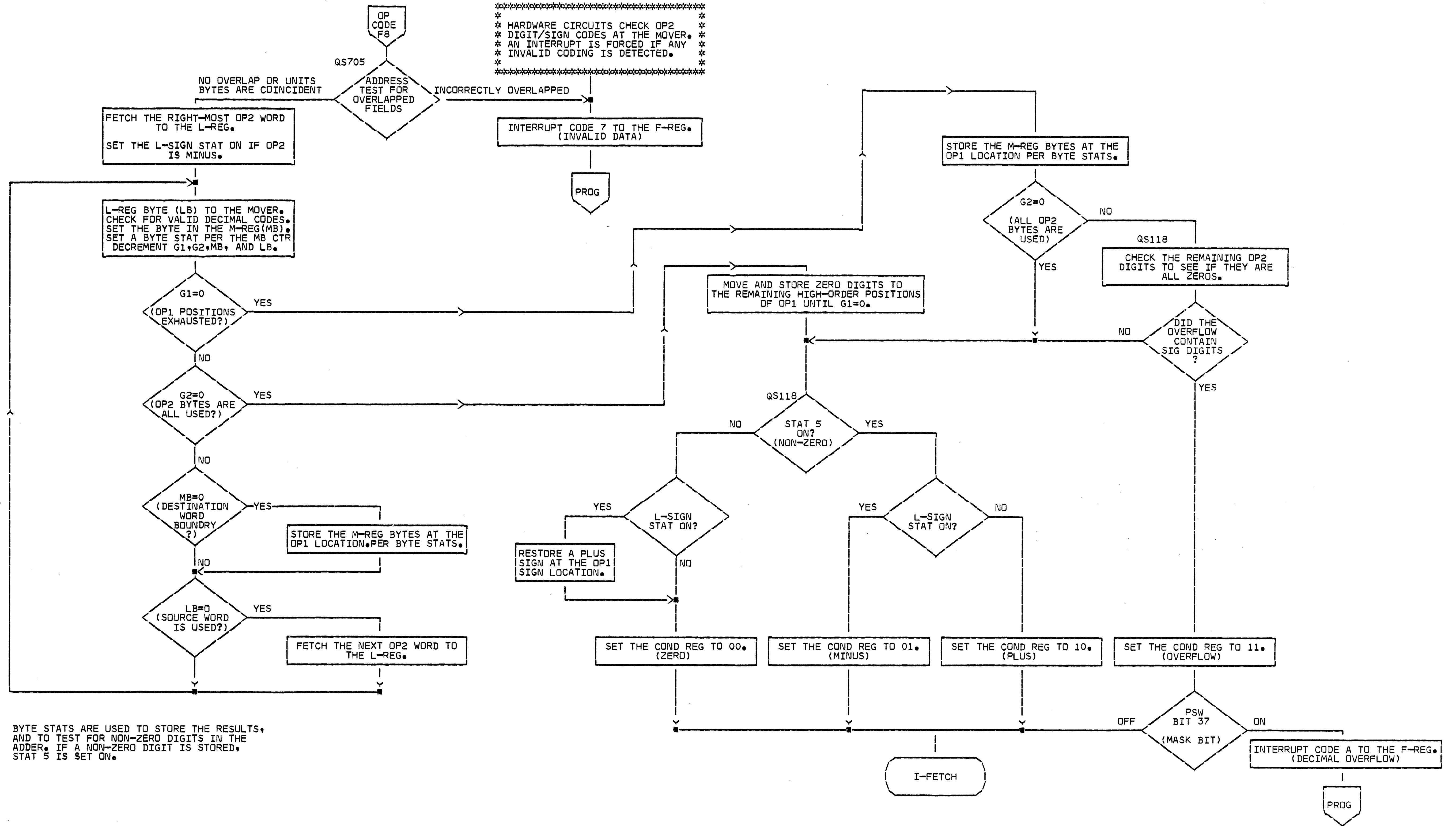
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NOTES: 1 0-3 AND 4-7 REFER TO THE BITS OF THE BYTE SELECTED BY THE LB AND MB COUNTERS. BITS 1111 ARE GENERATED FOR ZONE IF PSW 12 IS OFF (EBCDIC). BITS 0101 ARE GENERATED FOR ZONE IF PSW 12 IS ON (ASCII-8).

2 THE ADDRESS TEST RESULTS IN THE  $T_{8-31} = 0$ , IF BOTH THE SOURCE AND DESTINATION ARE THE SAME WORD OF MAIN STORAGE.

CL246



BYTE STATS ARE USED TO STORE THE RESULTS, AND TO TEST FOR NON-ZERO DIGITS IN THE ADDER. IF A NON-ZERO DIGIT IS STORED, STAT 5 IS SET ON.

\*\*\*\*\*  
 \* HARDWARE CIRCUITS CHECK OP2 \*  
 \* DIGIT/SIGN CODES AT THE MOVER. \*  
 \* AN INTERRUPT IS FORCED IF ANY \*  
 \* INVALID CODING IS DETECTED. \*  
 \*\*\*\*\*

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CLF 247  
 DATE 20 APR 65 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE 21

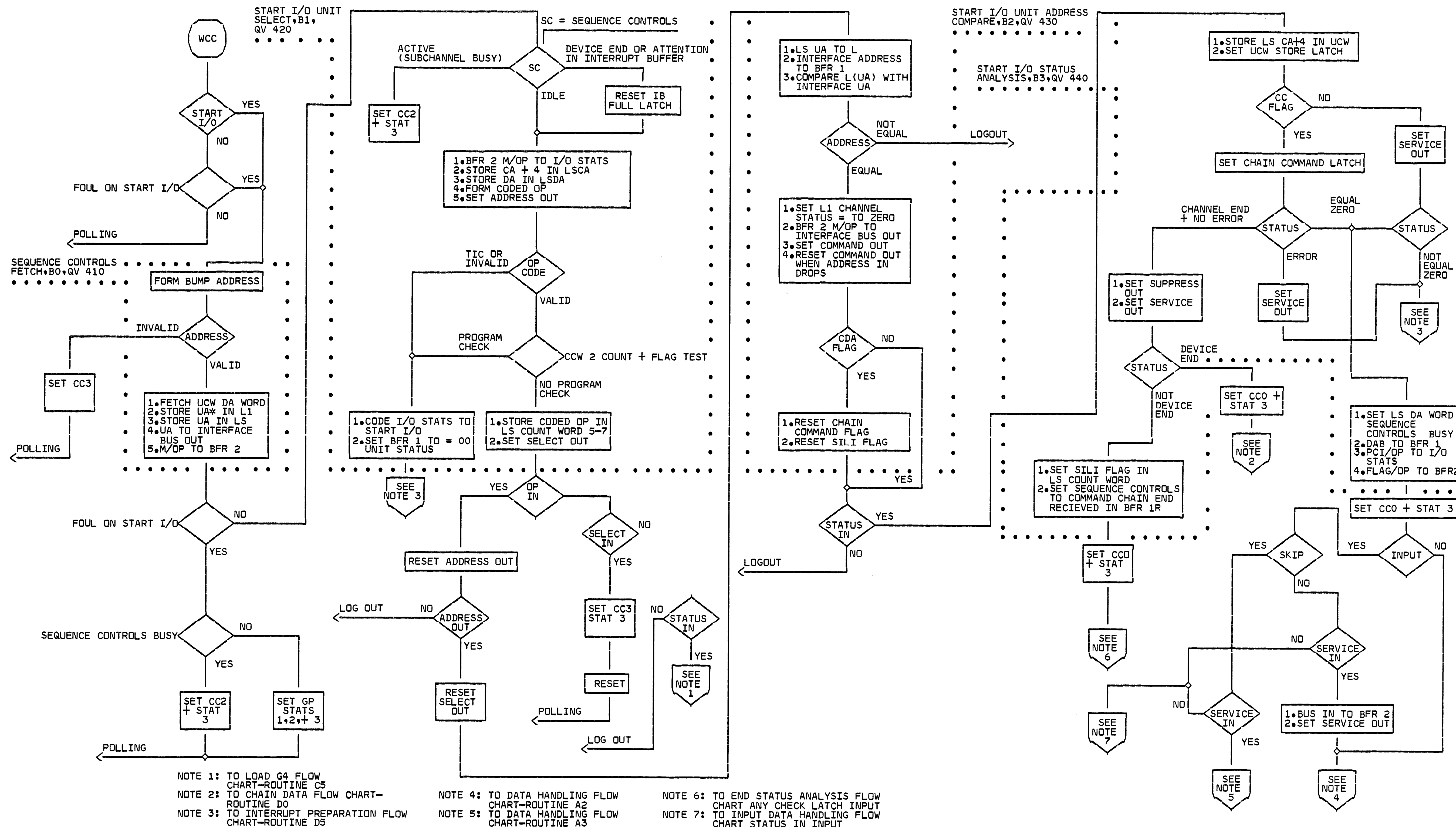
MPX ROUTINE	CAS QV-	HEX ADD	RDS ADDRESS			ROUTINE REQUEST BUFFER FUNCTION	ROUTINE NAME
			BASE	E			
			0123	4501	23AB		
			NOT 4 01	23A			
S A0	210	080	0000	1000	0000		COUNT FETCH AND UPDATE
S A1	220	084	0000	1000	0100		DATA ADDRESS FETCH AND UPDATE
S A2	230	088	0000	1000	1000		DATA HANDLING 1 (OUTPUT)
S A2	231		FROM	QV	230		DATA HANDLING 1 (INPUT)
S A3	240	086	0000	1000	1100		DATA HANDLING 2 (OUTPUT)
S A3	241		FROM	QV	240		DATA HANDLING 2 (READ FWD)
S A3	242		FROM	QV	240		DATA HANDLING 2 (STOP OR SKIP)
S A3	243		FROM	QV	240		DATA HANDLING 2 (READ BKWD)
S A4	250	090	0000	1001	0000		END STATUS ANALYSIS
S A5	350	094	0000	1001	0100		COMMAND CHAIN END STATUS ANALYSIS
S A5	351		FROM	QV	350		COMMAND CHAIN END STATUS ANALYSIS
S A5	352		FROM	QV	350		COMMAND CHAIN END STATUS ANALYSIS
A6	820	098	0000	1001	1000		INTERRUPT PREPARATION
A7	270	09C	0000	1001	1100		COUNT EQUALS ZERO ANALYSIS
B0	410	0A0	0000	1010	0000		SEQUENCE CONTROL FETCH
B1	420	0A4	0000	1010	0100		START IO UNIT SELECT
B2	430	0A8	0000	1010	1000		START IO UNIT ADDRESS COMPARE
B3	440	0AC	0000	1010	1100		START IO STATUS ANALYSIS
B5	460	0B4	0000	1011	0100		COUNT STORE
B6	470	0B8	0000	1011	1000		DA STORE
B7	840	0BC	0000	1011	1100		CHECK HANDLING
C0	260	002	0000	0000	0010		PCI
C1	520	086	0000	1000	0110		TEST IO UNIT SELECT 1
C2	540	08A	0000	1000	1010		TEST IO UNIT ADDRESS COMPARE
C3	550	08E	0000	1000	1110		TEST IO ACCEPT STATUS
C4	850	092	0000	1001	0010		CONTROL CHECK
C5	810	096	0000	1001	0110		CONTROL UNIT BUSY
C6	620	09A	0000	1001	1010		HALT IO UNIT SELECT
C7	530	09E	0000	1001	1110		TEST IO UNIT SELECT 2
D0	360	0A2	0000	1010	0010		COMMAND ADDR FETCH/STORE
D1	310	0A6	0000		0110		CHAN CONTROL WORD 1 FETCH
D2	330	0AA	0000		1010		COMMAND CHAIN UNIT ADDRESS COMPARE
D3	340	0AE	0000		1110		COMMAND CHAIN INITIAL STATUS ANAL
S D4	320	0B2	0000	1011	0010		FETCH 2ND HALF OF CHAN CTRL WORD
S D4	321		FROM	QV	320		CHAN CONTROL WORD 2 FETCH
S D5	830	0B6	0000	1011	0110		LOAD 64 PREP (ST IO OR TEST IO QED)
S D5	831		FROM	QV	830		LOAD 64 PREP (TEST IO NO END QED)
S D5	832		FROM	QV	830		LOAD 64 PREP (CU BUSY OR HALT IO)
D7	370	0BE	0000	1011	1110		DATA CHAINING

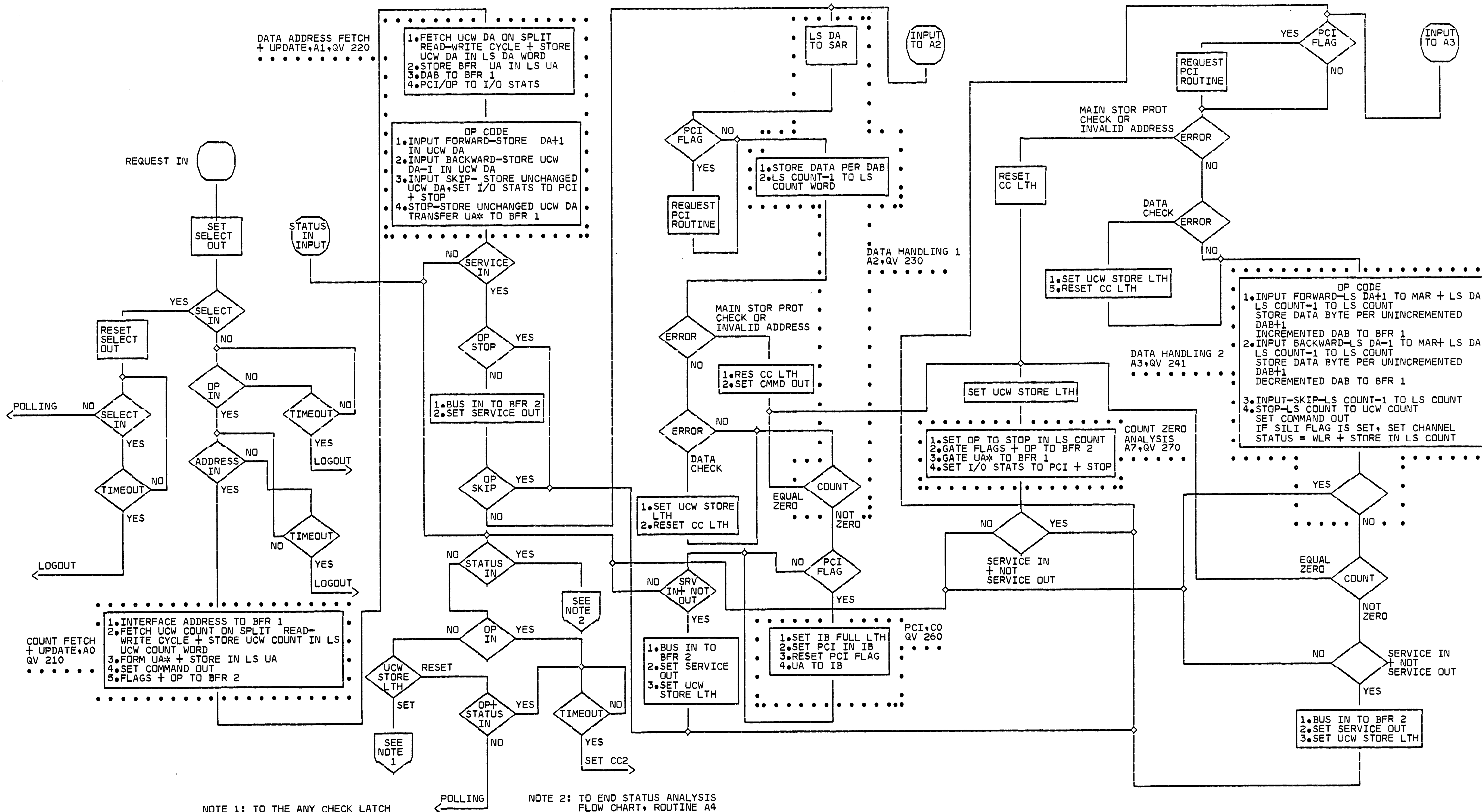
IOP 101 I-O ROUTINE STARTING ADDRESS

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DATE 9 SEP 65 MACH.  
 MULTIPLEXOR FRAME  
 FOR MODEL 50 P.No.  
 IBM CORP. SDD PAGE 1

J  
C  
M  
P  
X



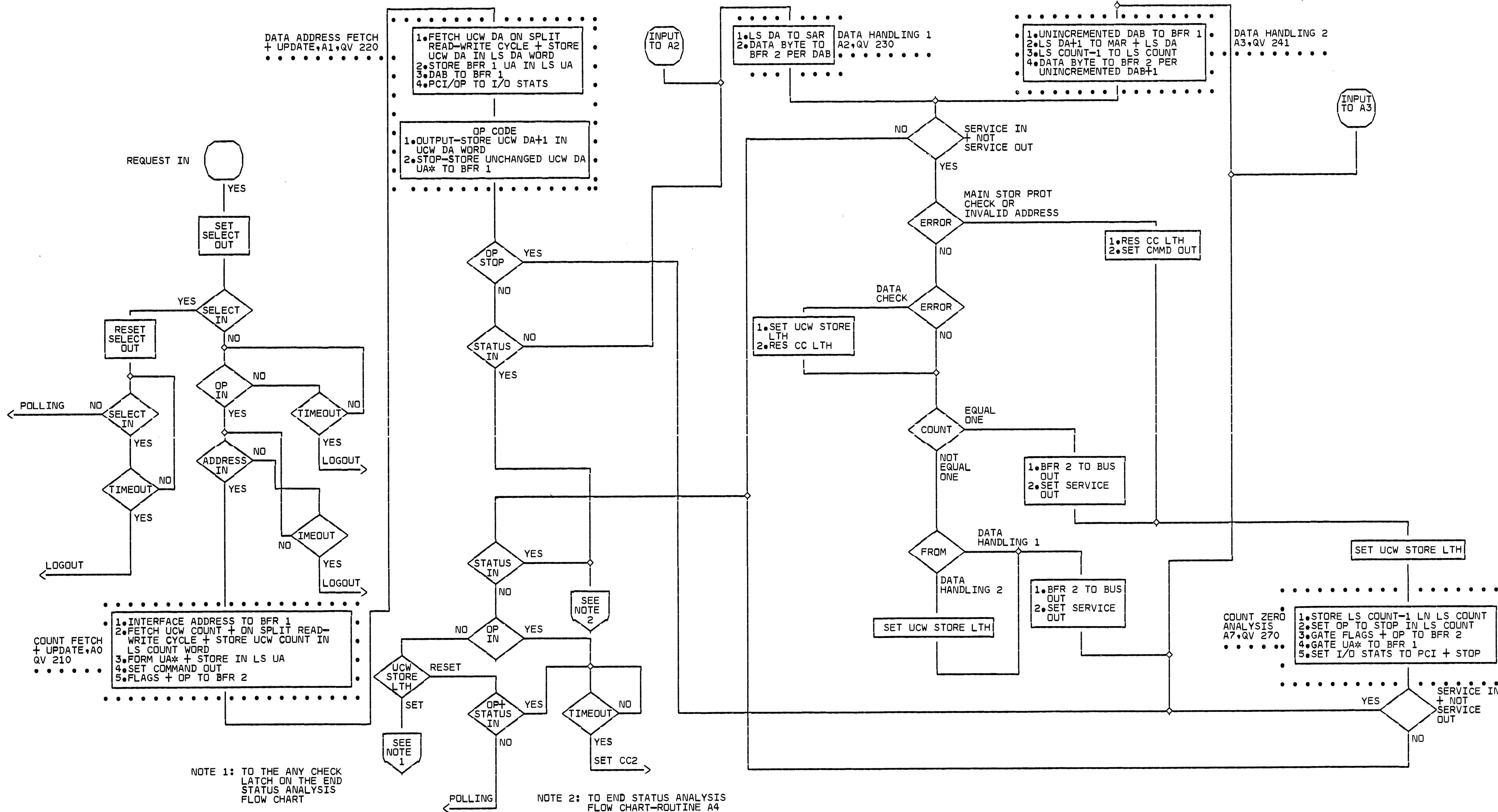


NOTE 1: TO THE ANY CHECK LATCH ON THE END STATUS ANALYSIS FLOW CHART

NOTE 2: TO END STATUS ANALYSIS FLOW CHART, ROUTINE A4

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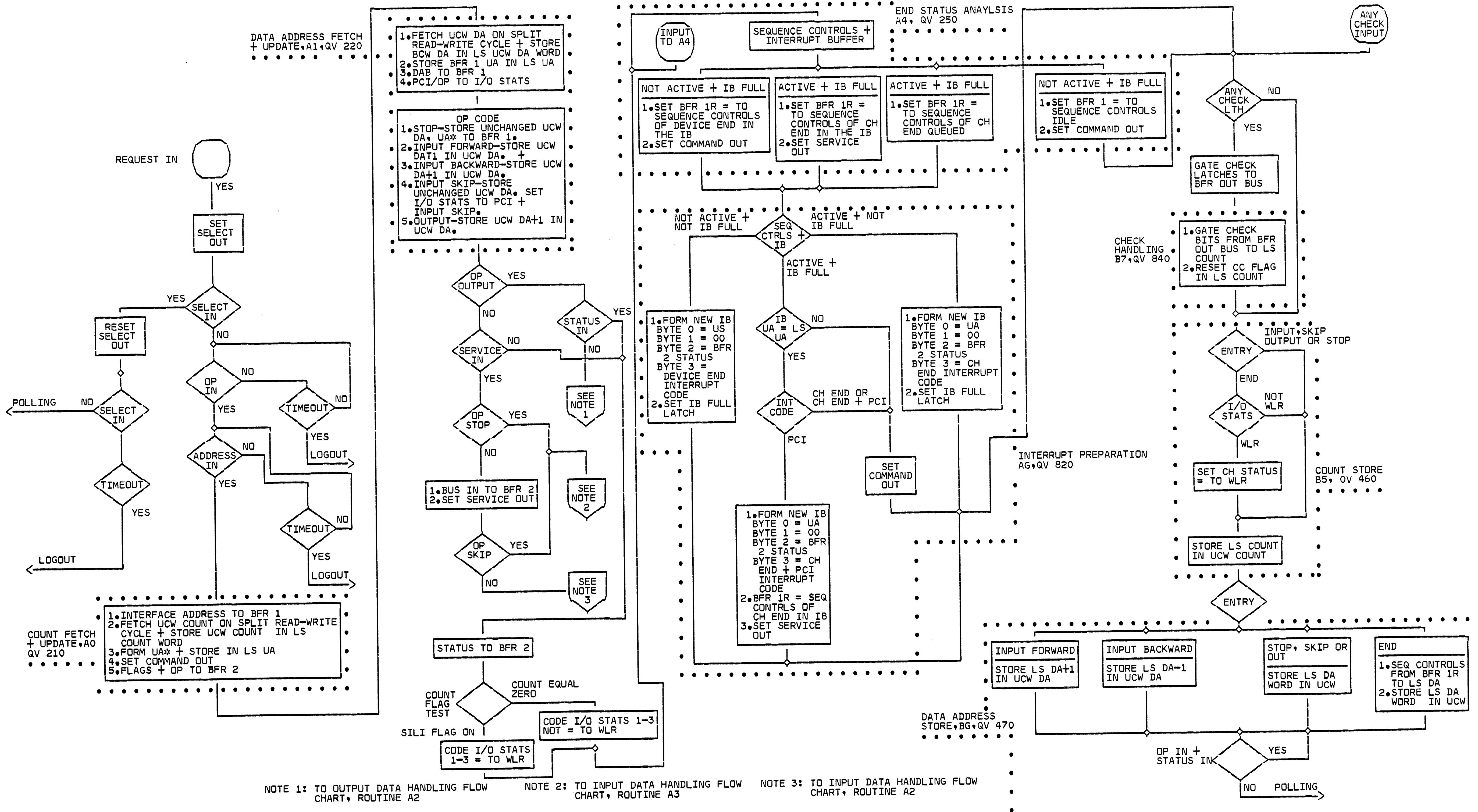


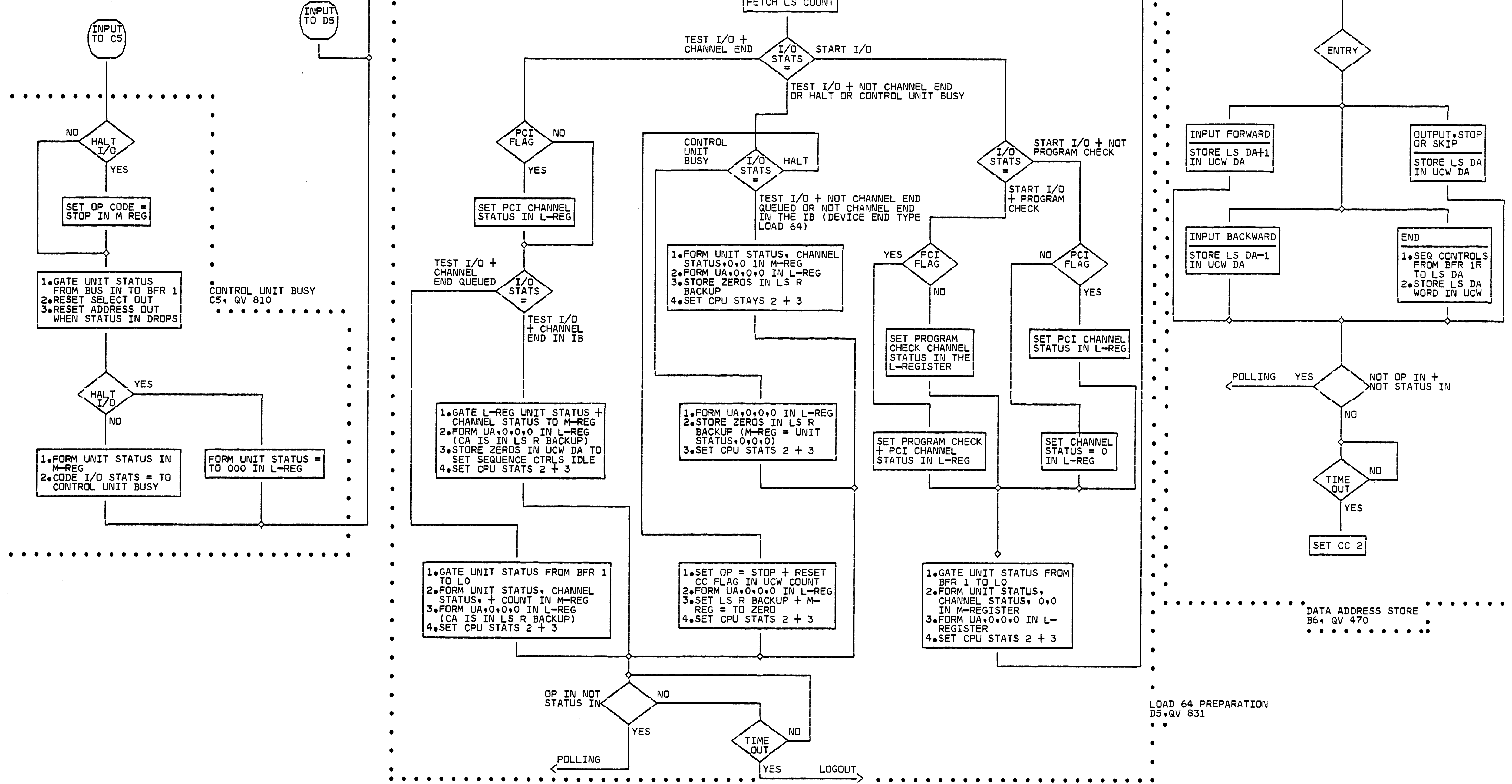


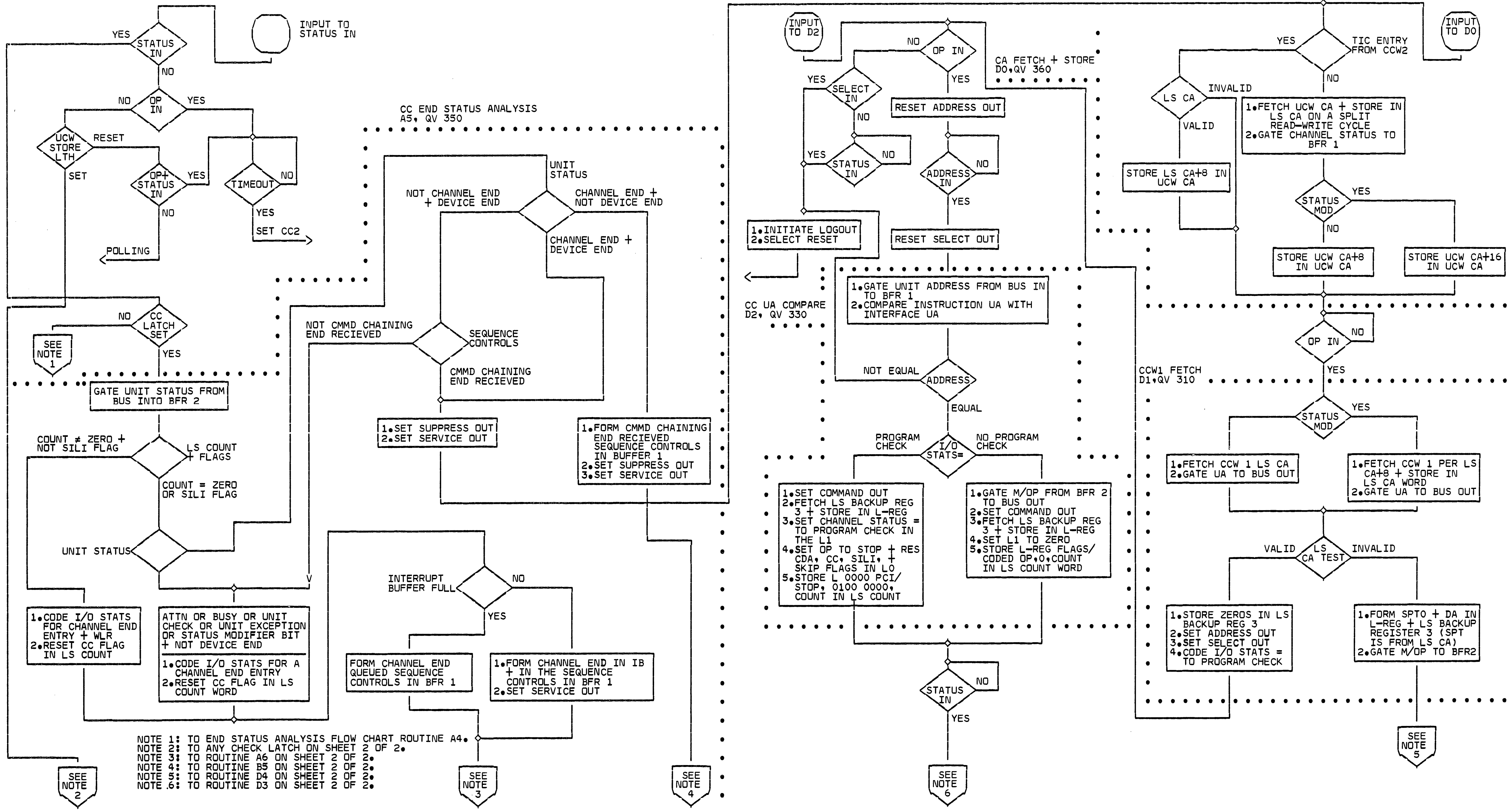
NOTE 1: TO THE ANY CHECK LATCH ON THE END STATUS ANALYSIS FLOW CHART

NOTE 2: TO END STATUS ANALYSIS FLOW CHART-ROUTINE A4

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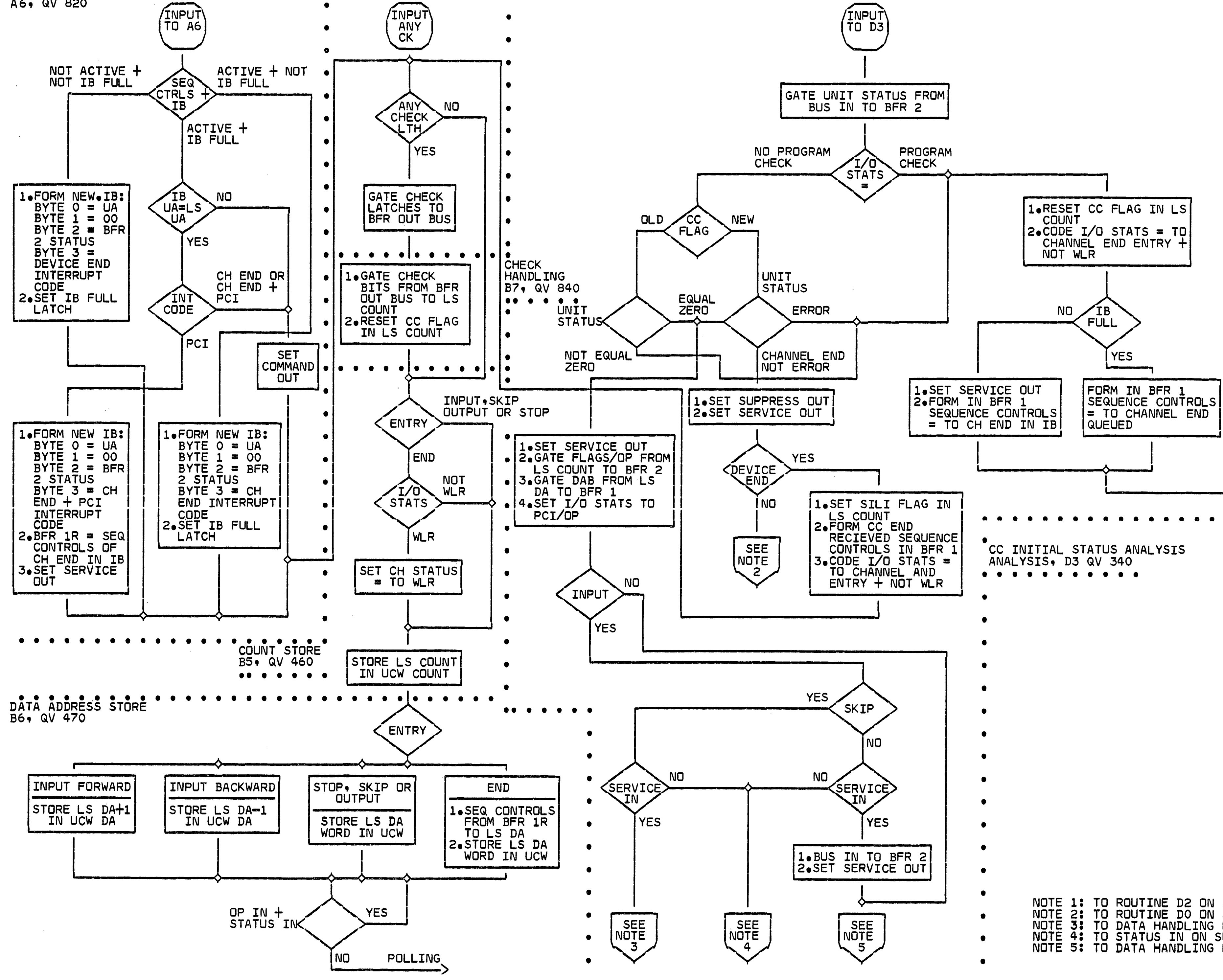


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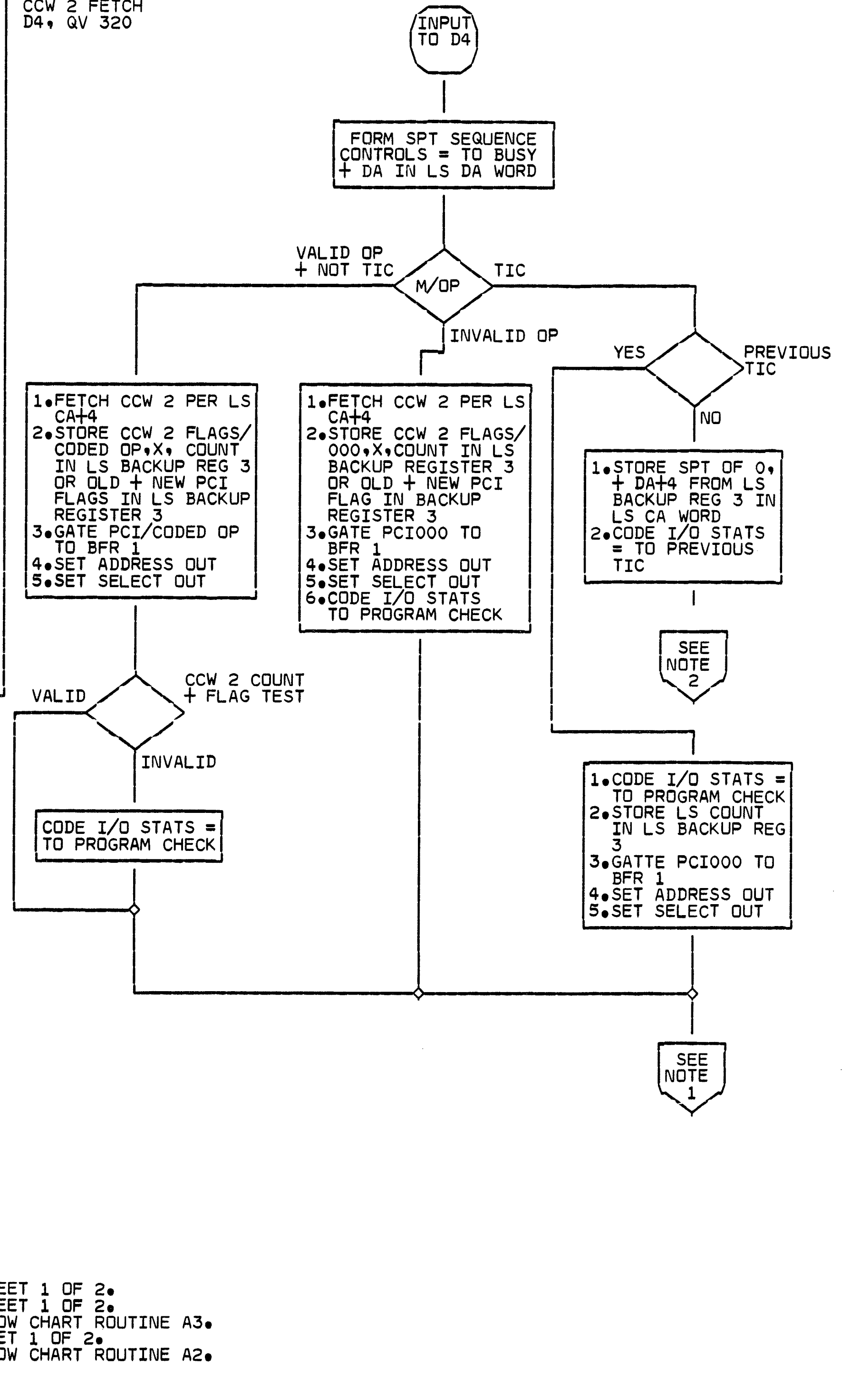
DATE 9 SEP 65 MACH.  
 MULTIPLEXOR FRAME  
 FOR MODEL 50 P.N.  
 IBM CORP. SDD PAGE 7

JCMPX

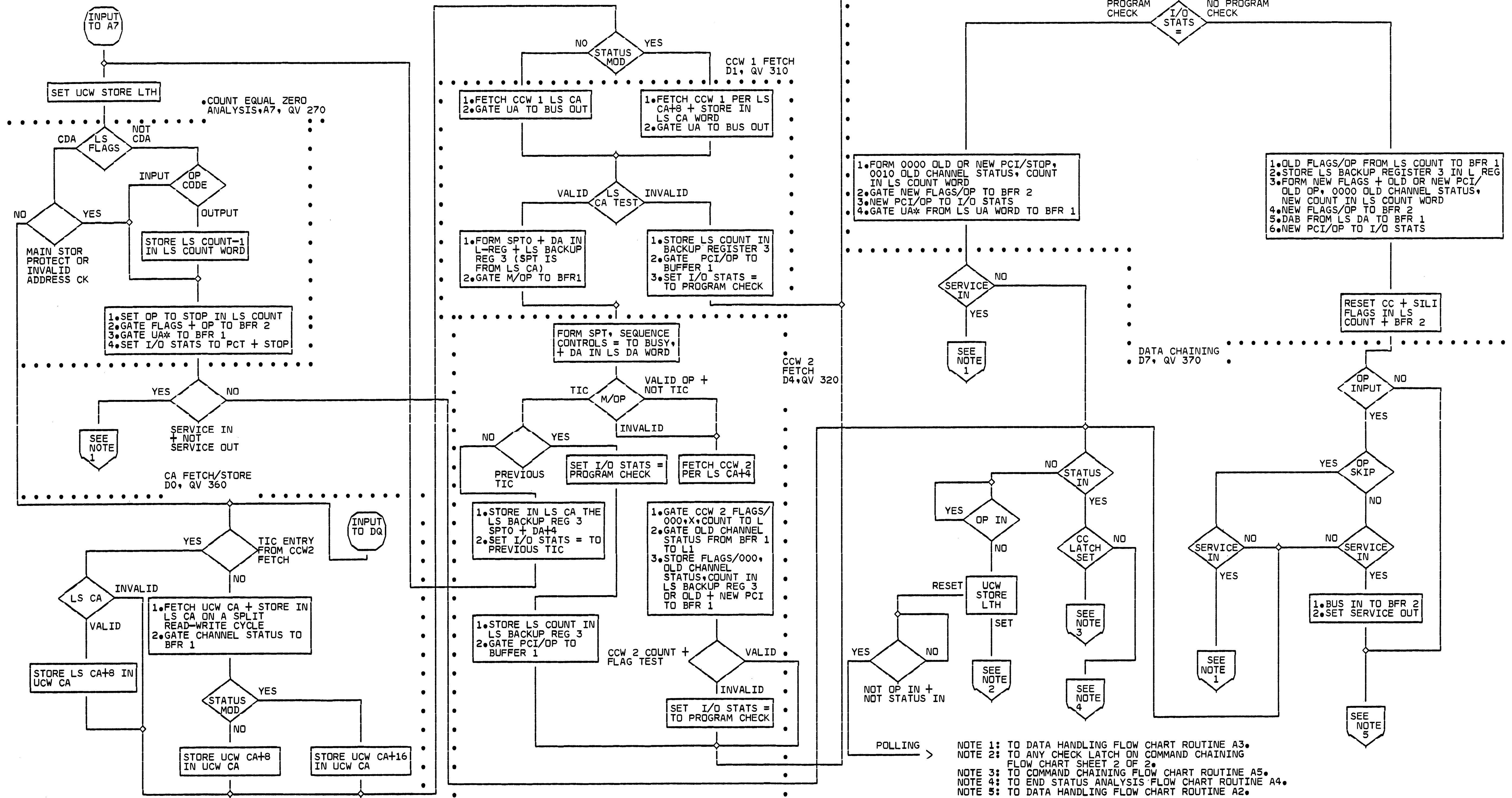
INTERRUPT PREPARATION  
A6, QV 820

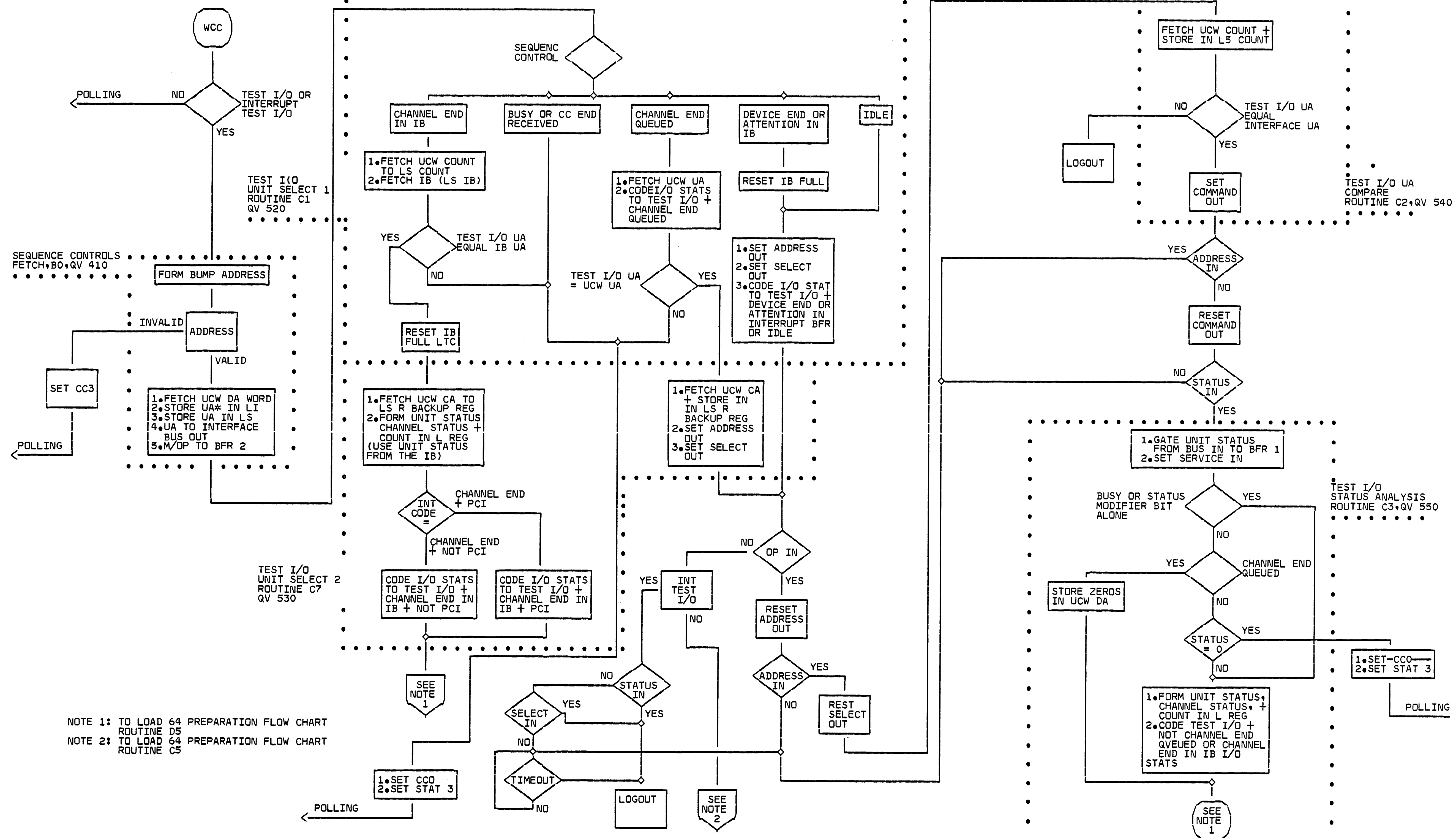


CCW 2 FETCH  
D4, QV 320



NOTE 1: TO ROUTINE D2 ON SHEET 1 OF 2.  
 NOTE 2: TO ROUTINE D0 ON SHEET 1 OF 2.  
 NOTE 3: TO DATA HANDLING FLOW CHART ROUTINE A3.  
 NOTE 4: TO STATUS IN ON SHEET 1 OF 2.  
 NOTE 5: TO DATA HANDLING FLOW CHART ROUTINE A2.



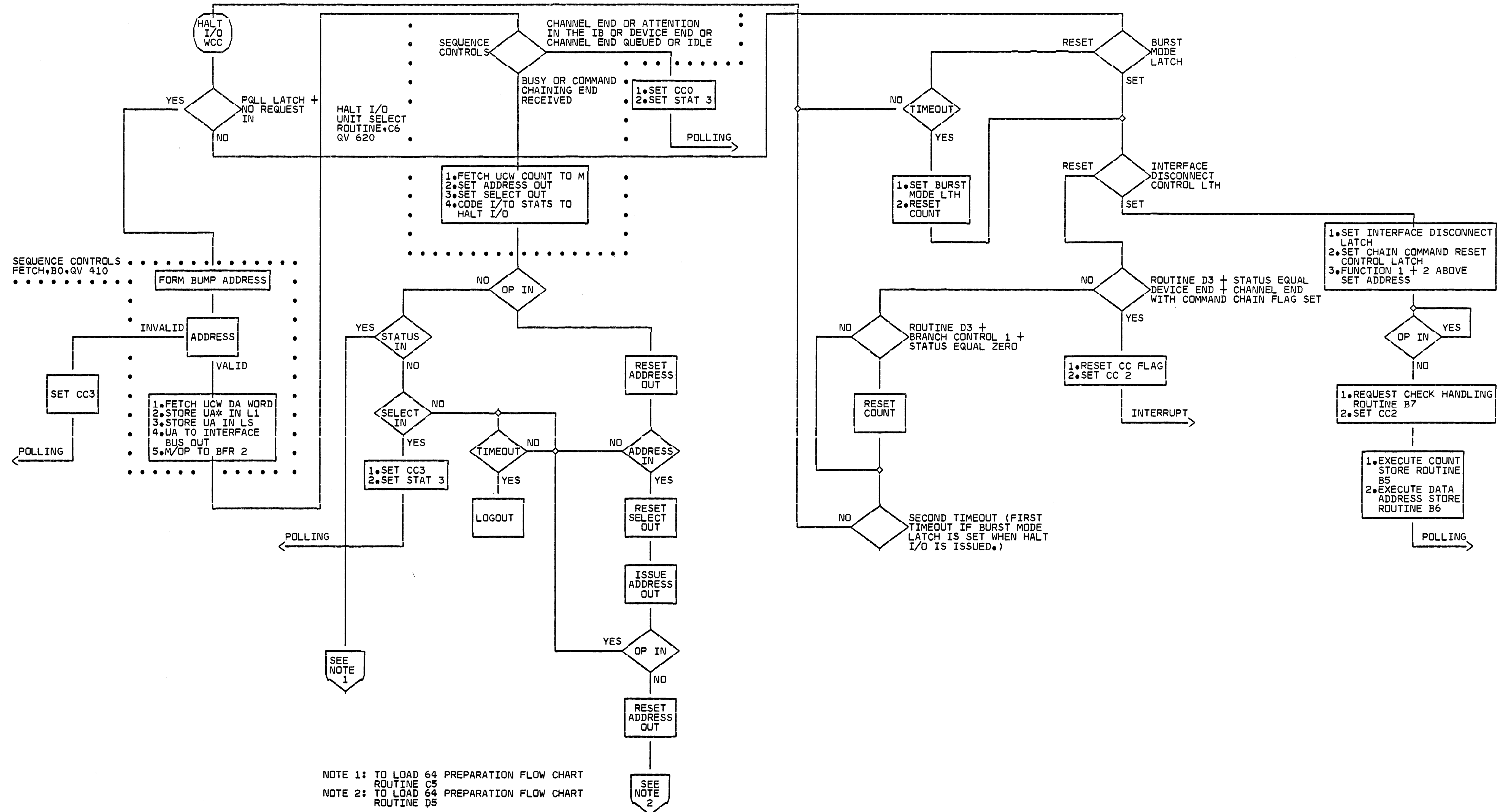


NOTE 1: TO LOAD 64 PREPARATION FLOW CHART ROUTINE D5  
 NOTE 2: TO LOAD 64 PREPARATION FLOW CHART ROUTINE C5

DATE 9 SEP 65 MACH.  
 MULTIPLEXOR FRAME  
 FOR MODEL 50 P.N.  
 IBM CORP. SDD PAGE 10

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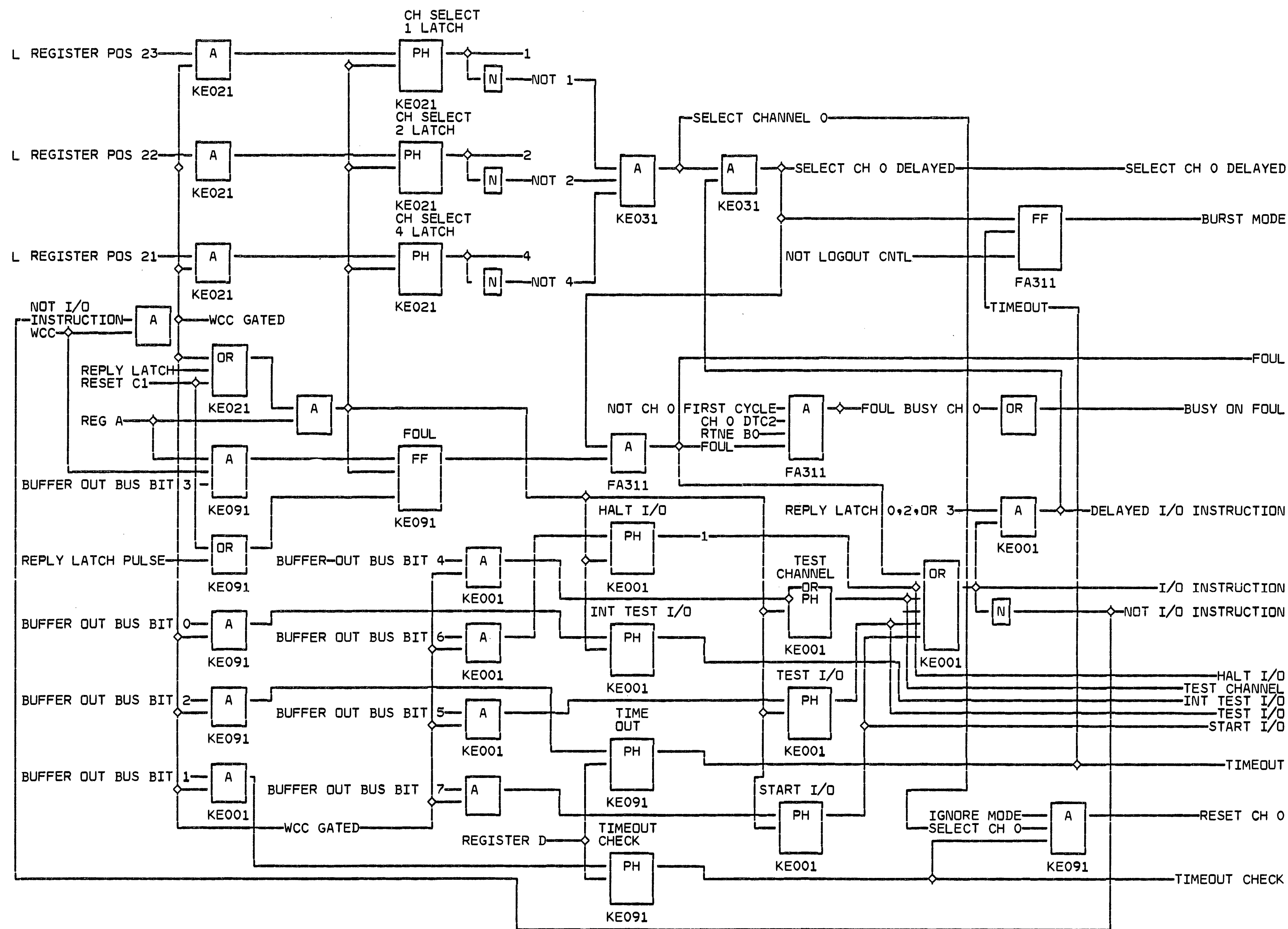
JCMAX



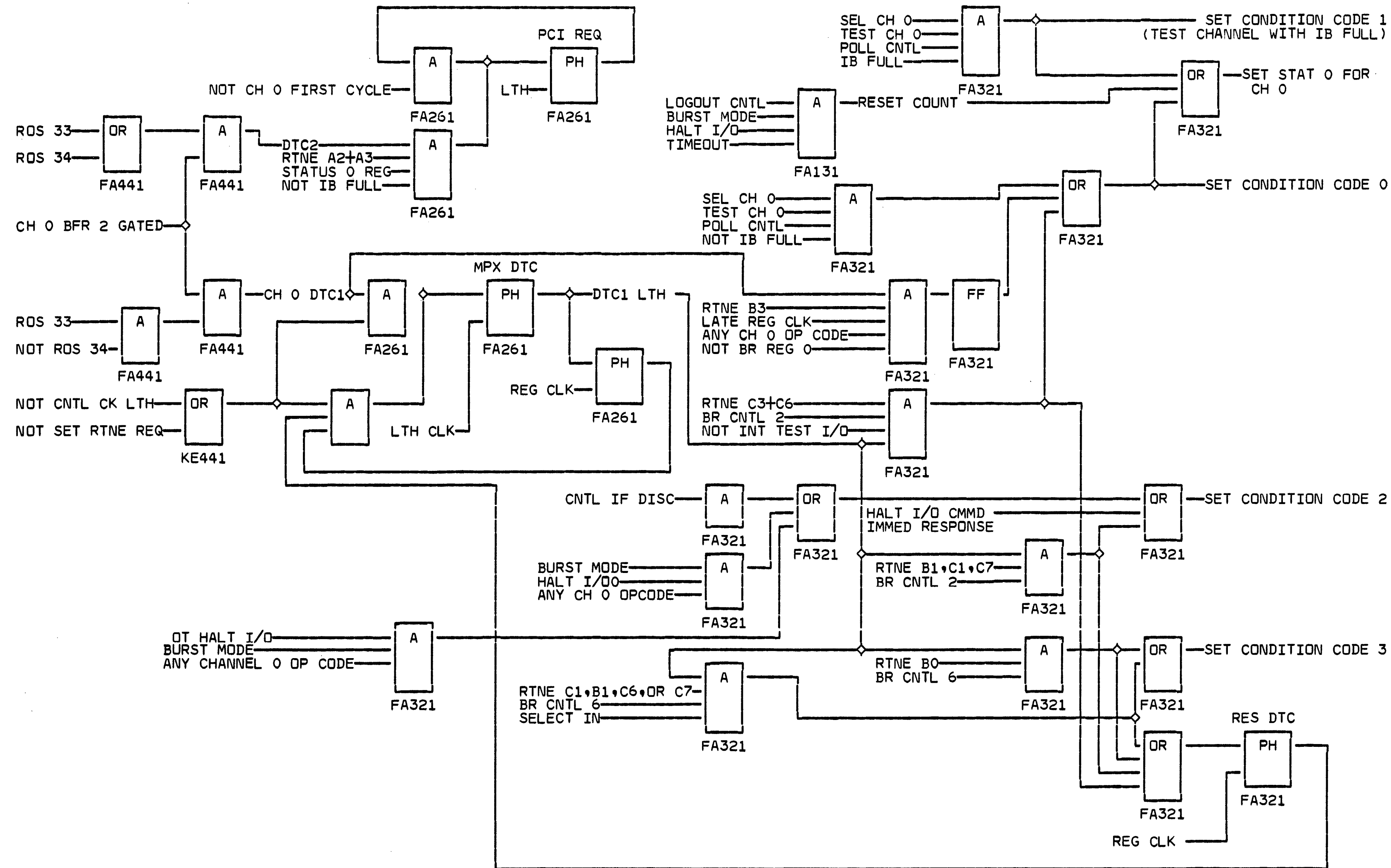
NOTE 1: TO LOAD 64 PREPARATION FLOW CHART  
 ROUTINE C5  
 NOTE 2: TO LOAD 64 PREPARATION FLOW CHART  
 ROUTINE D5

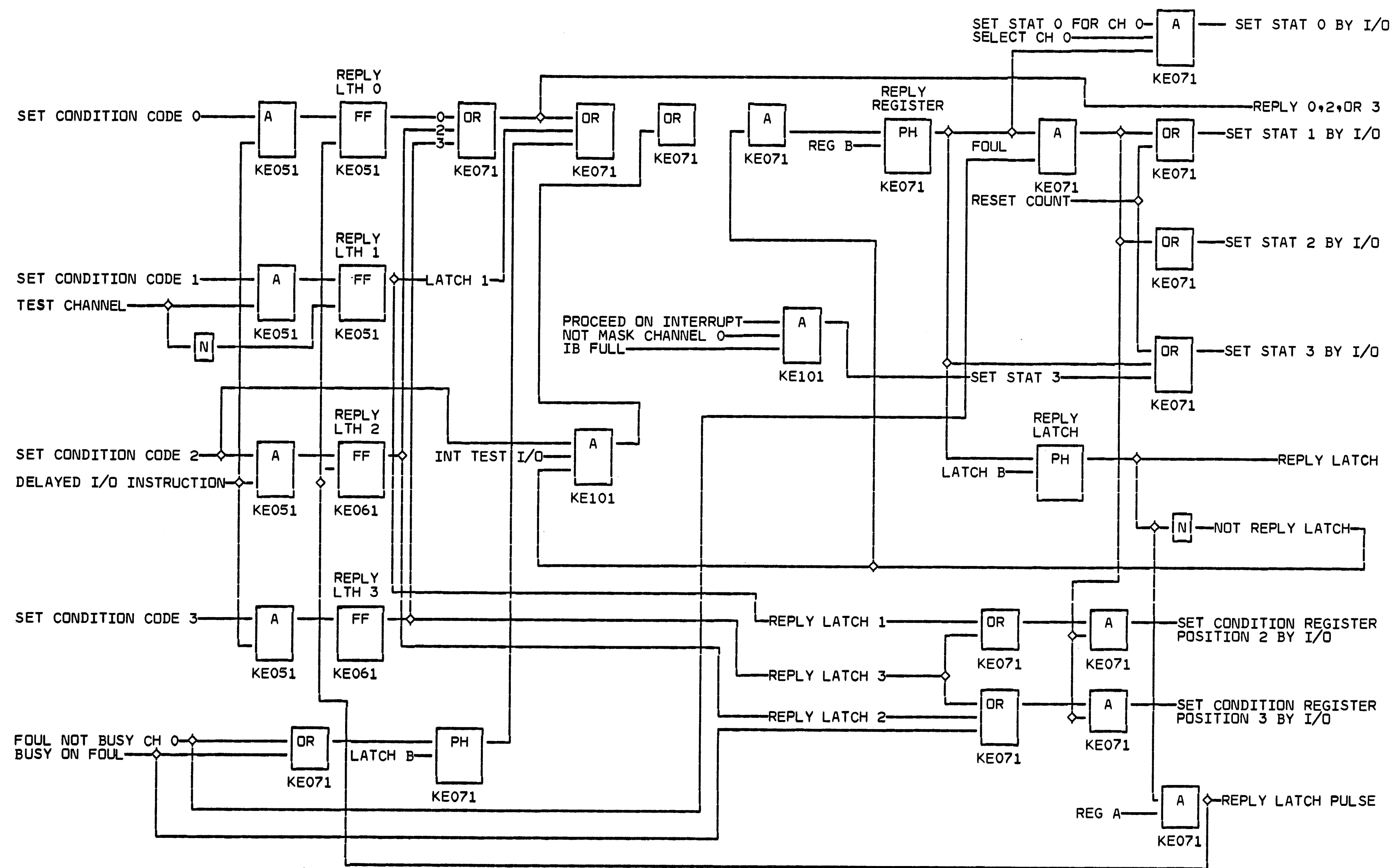
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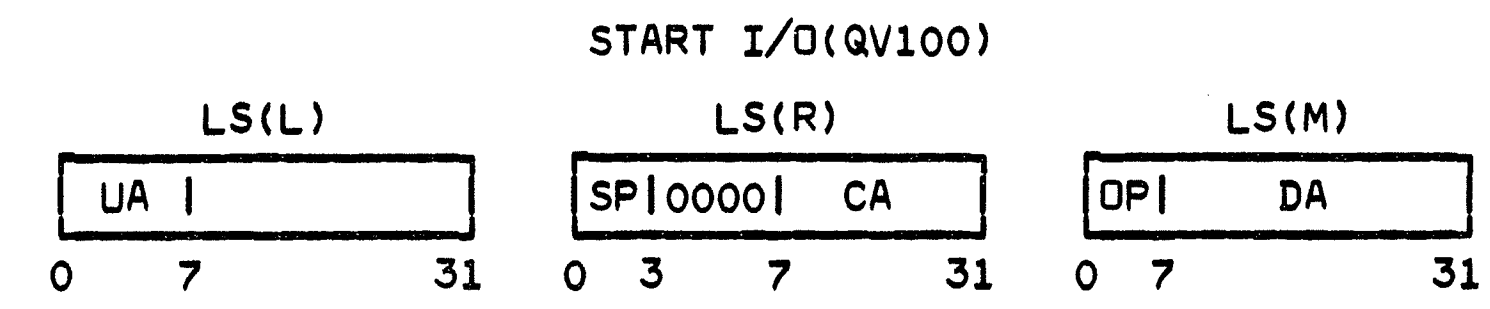
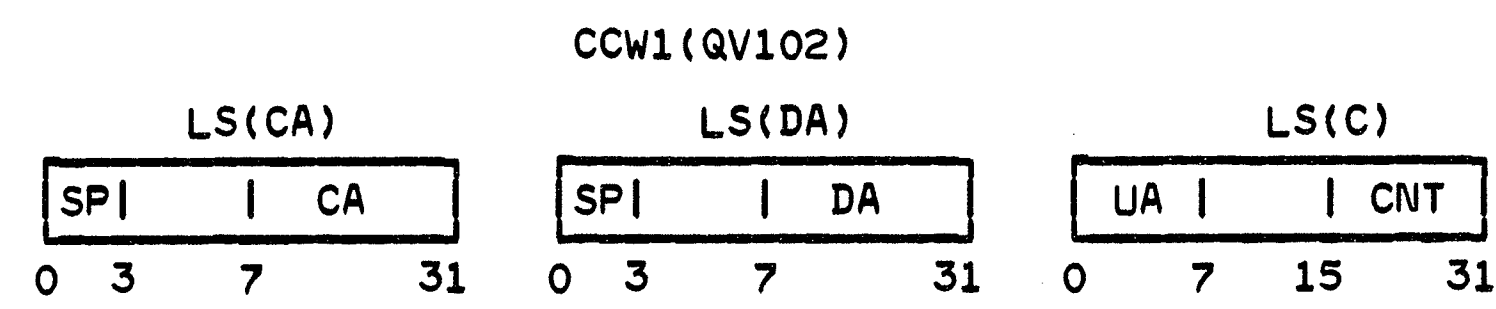
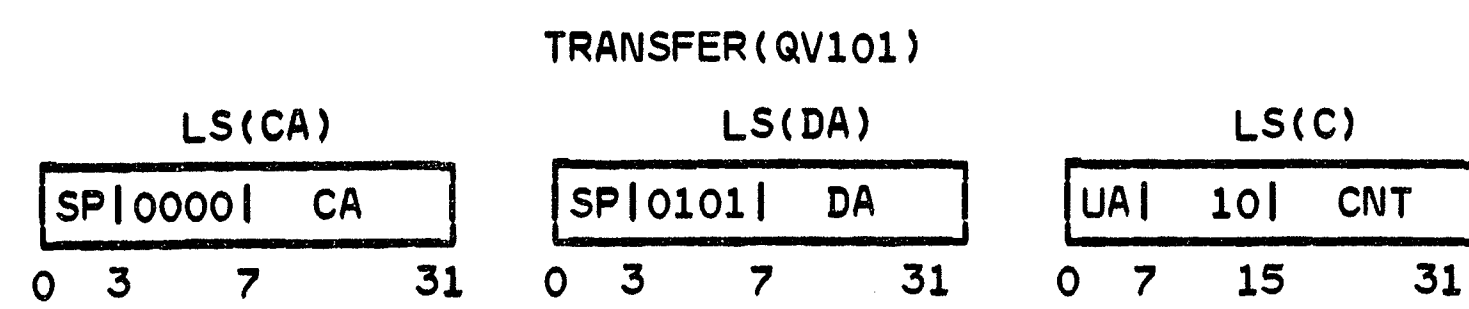




CONDITION REG	SET CONDITION CODE
2 OFF AND 3 OFF	0000000
2 ON AND 3 OFF	0000001
2 OFF AND 3 ON	0000010
2 ON AND 3 ON	0000011

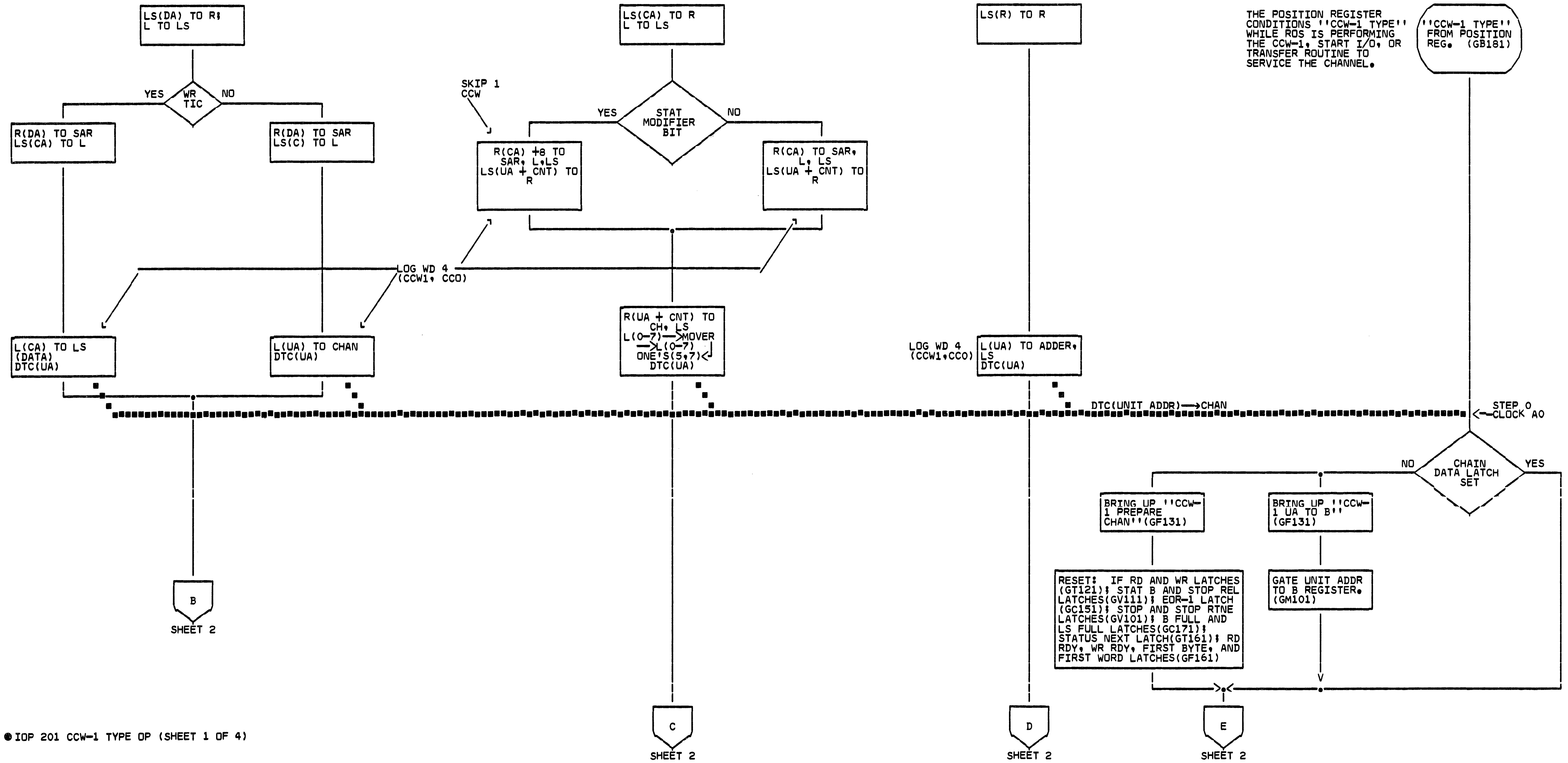
X P M C C J

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THE POSITION REGISTER CONDITIONS 'CCW-1 TYPE' WHILE RDS IS PERFORMING THE CCW-1, START I/O, OR TRANSFER ROUTINE TO SERVICE THE CHANNEL.

'CCW-1 TYPE' FROM POSITION REG. (GB181)



● IOP 201 CCW-1 TYPE OP (SHEET 1 OF 4)

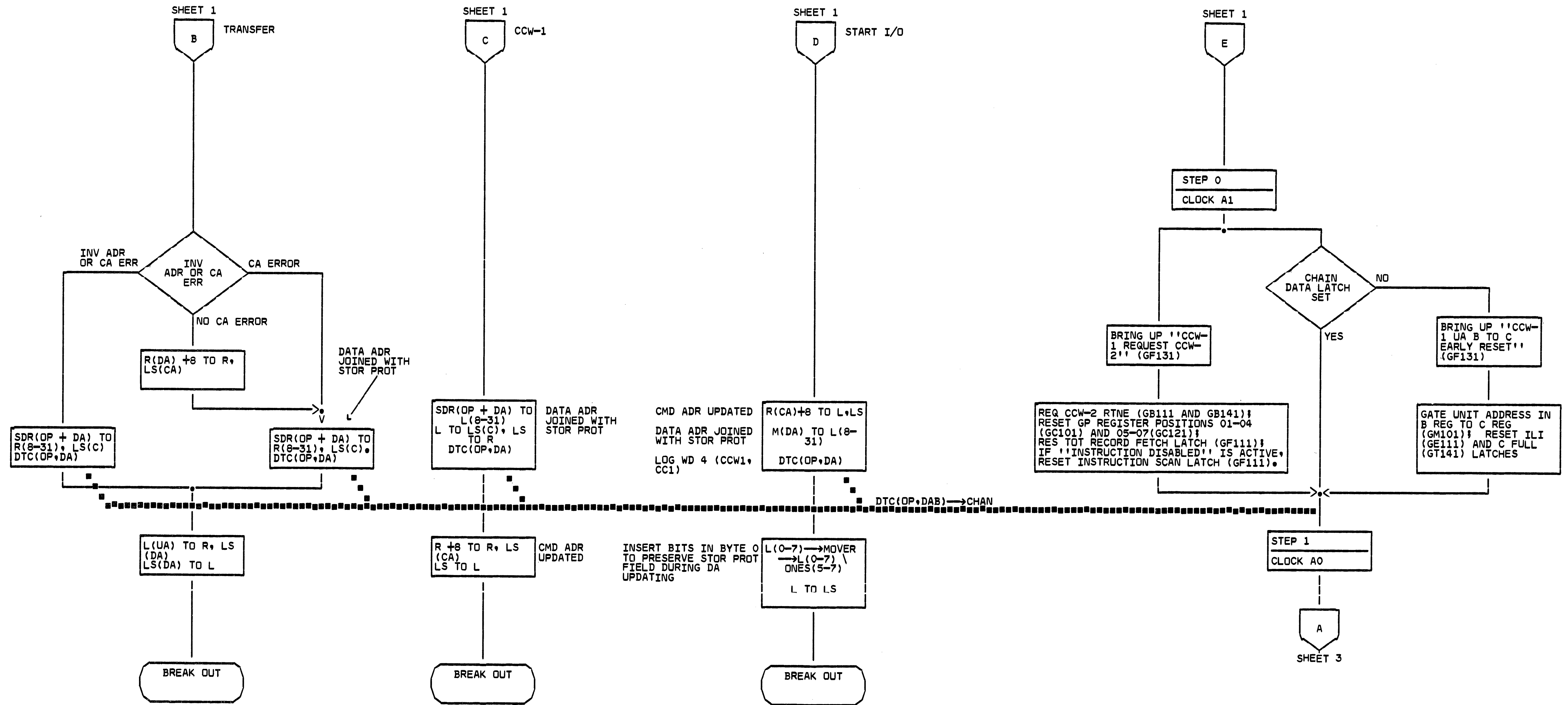
CCW-1 TYPE OP  
(SELECTOR CHANNEL)  
DATE 27 JUN 66 MACH. 2050

FRAME  
P.N.

IBM CORP. SDD PAGE 4

S4001

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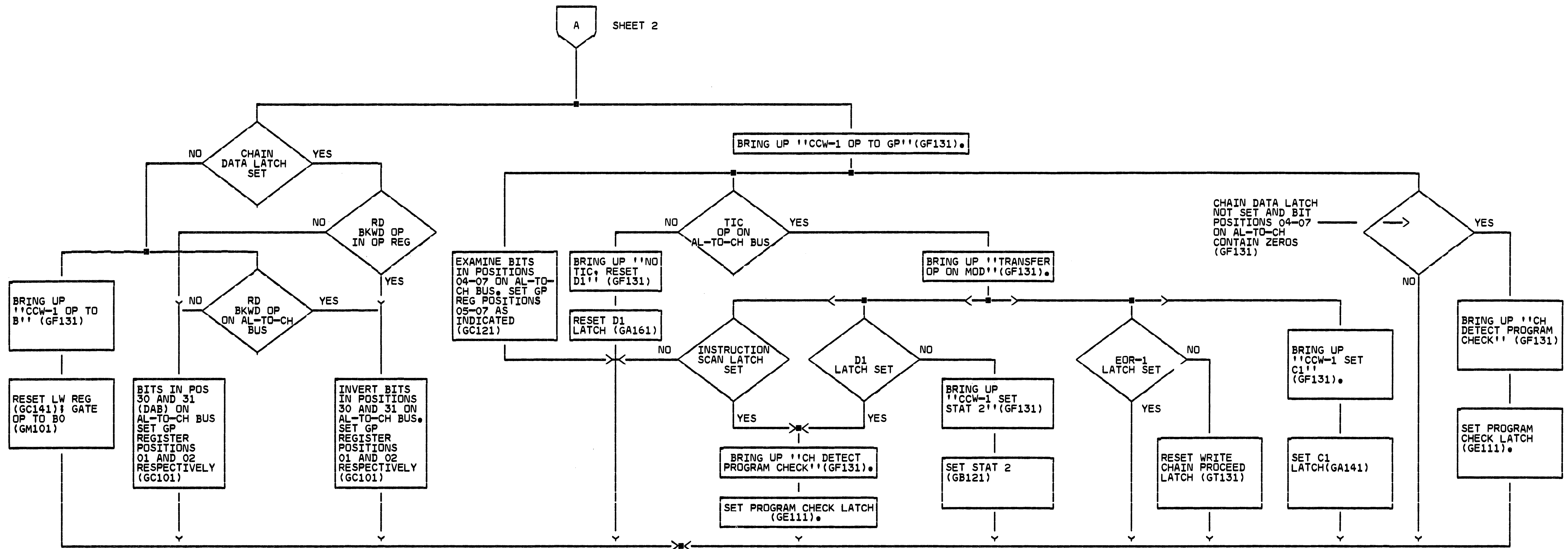


● IOP 201 CCW-1 TYPE DP (SHEET 2 OF 4)

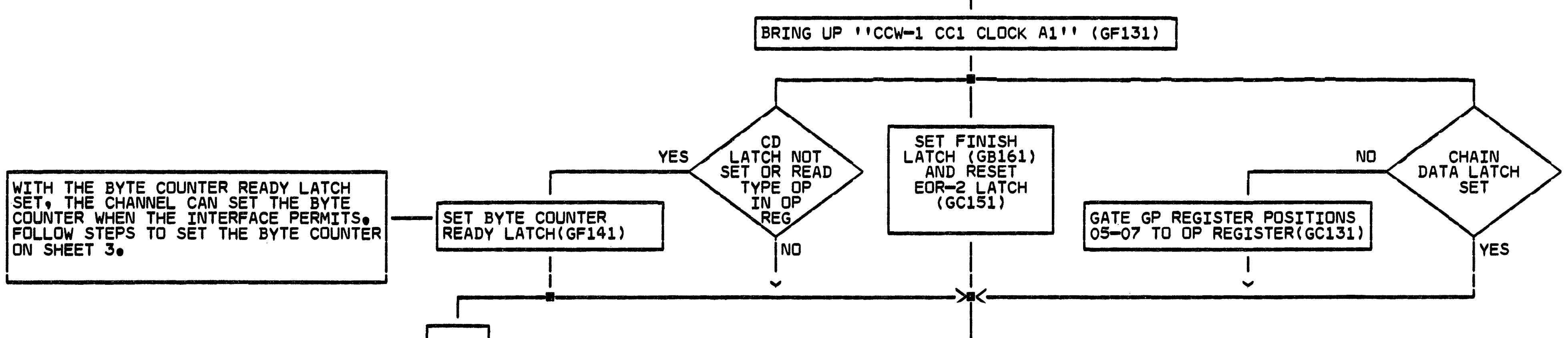
CCW-1 TYPE DP  
 (SELECTOR CHANNEL)  
 DATE 27 JUN 66 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE

S4001

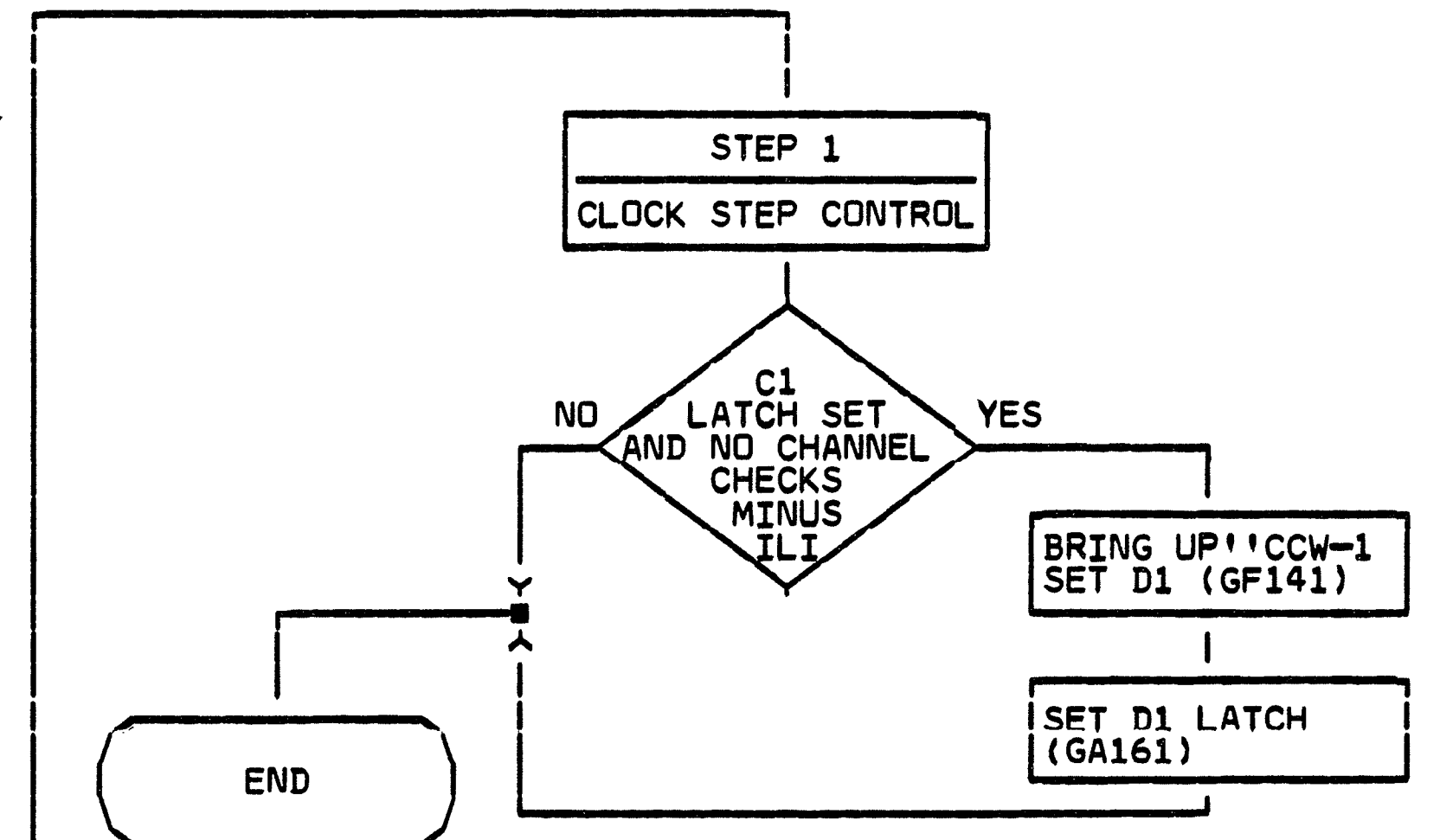
IBM CONFIDENTIAL



STEP 1  
CLOCK A1



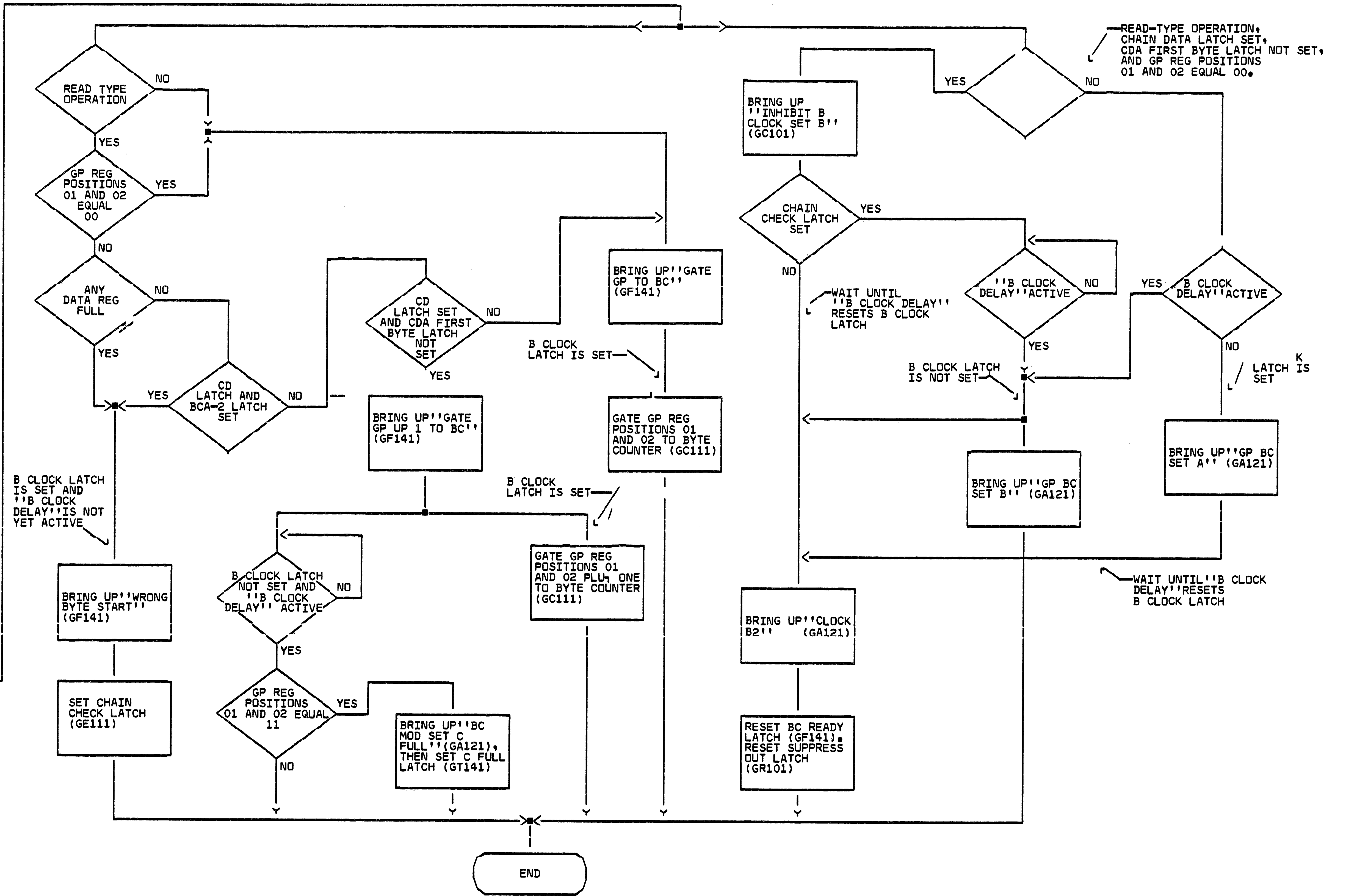
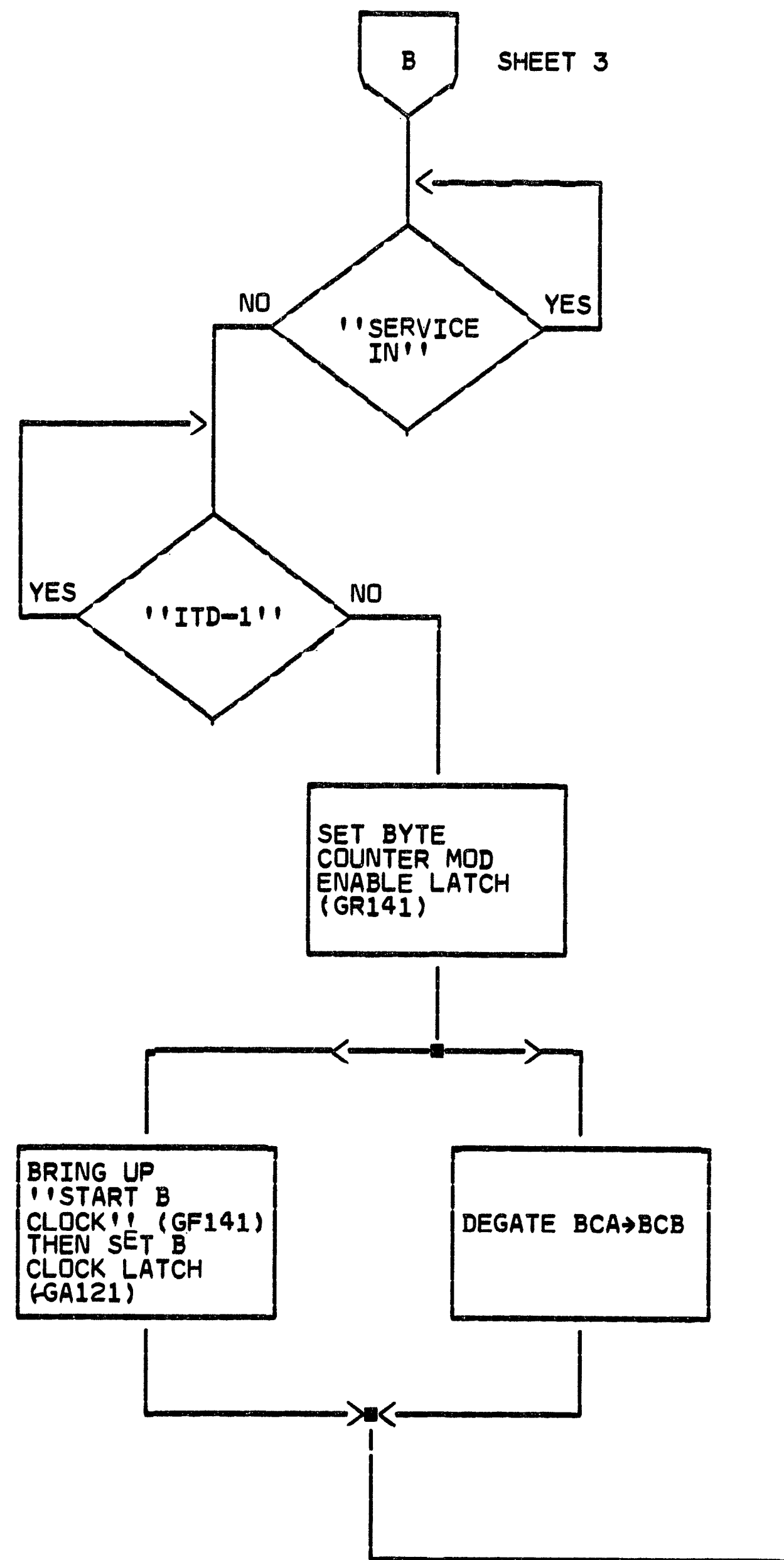
B SHEET 4



CCW-1 TYPE OP  
(SELECTOR CHANNEL)  
DATE 27 JUN 66 MACH. 2050  
FRAME  
P. No.  
IBM CORP. SDD PAGE 2

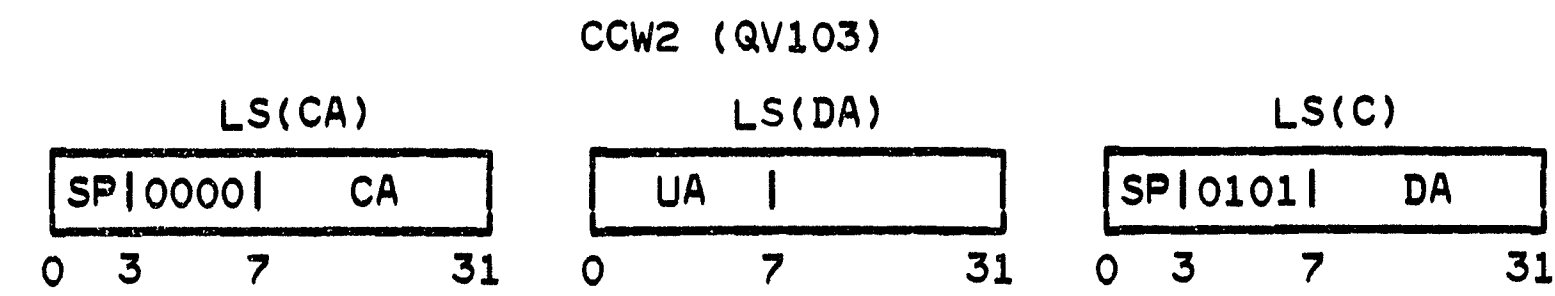
S4001

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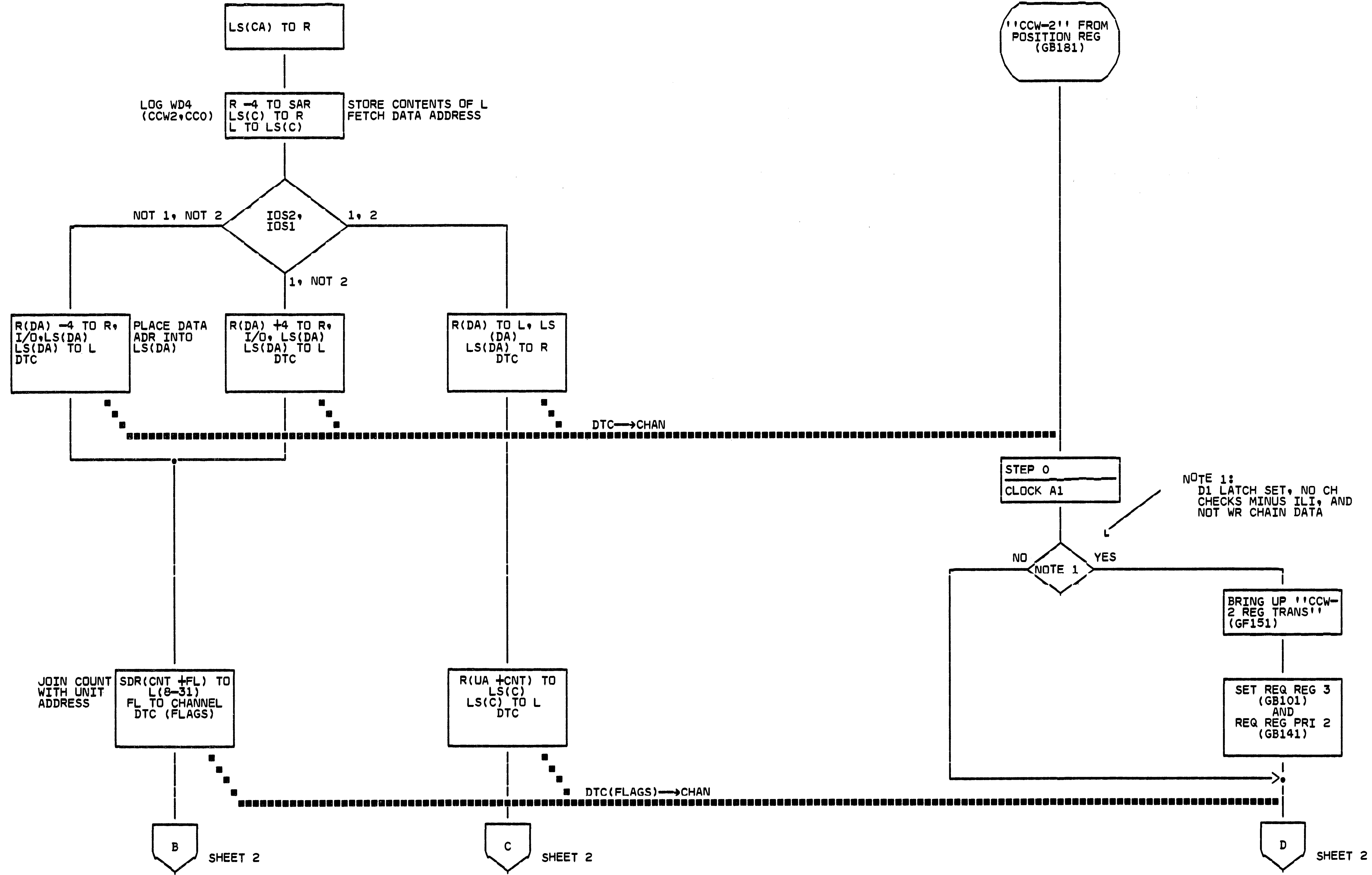


CCW-1 TYPE OP  
 (SELECTOR CHANNEL)  
 DATE 27 JUN 66 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE

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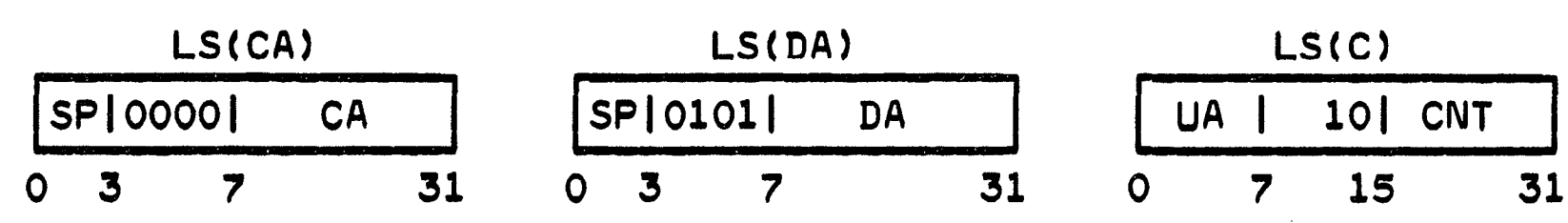
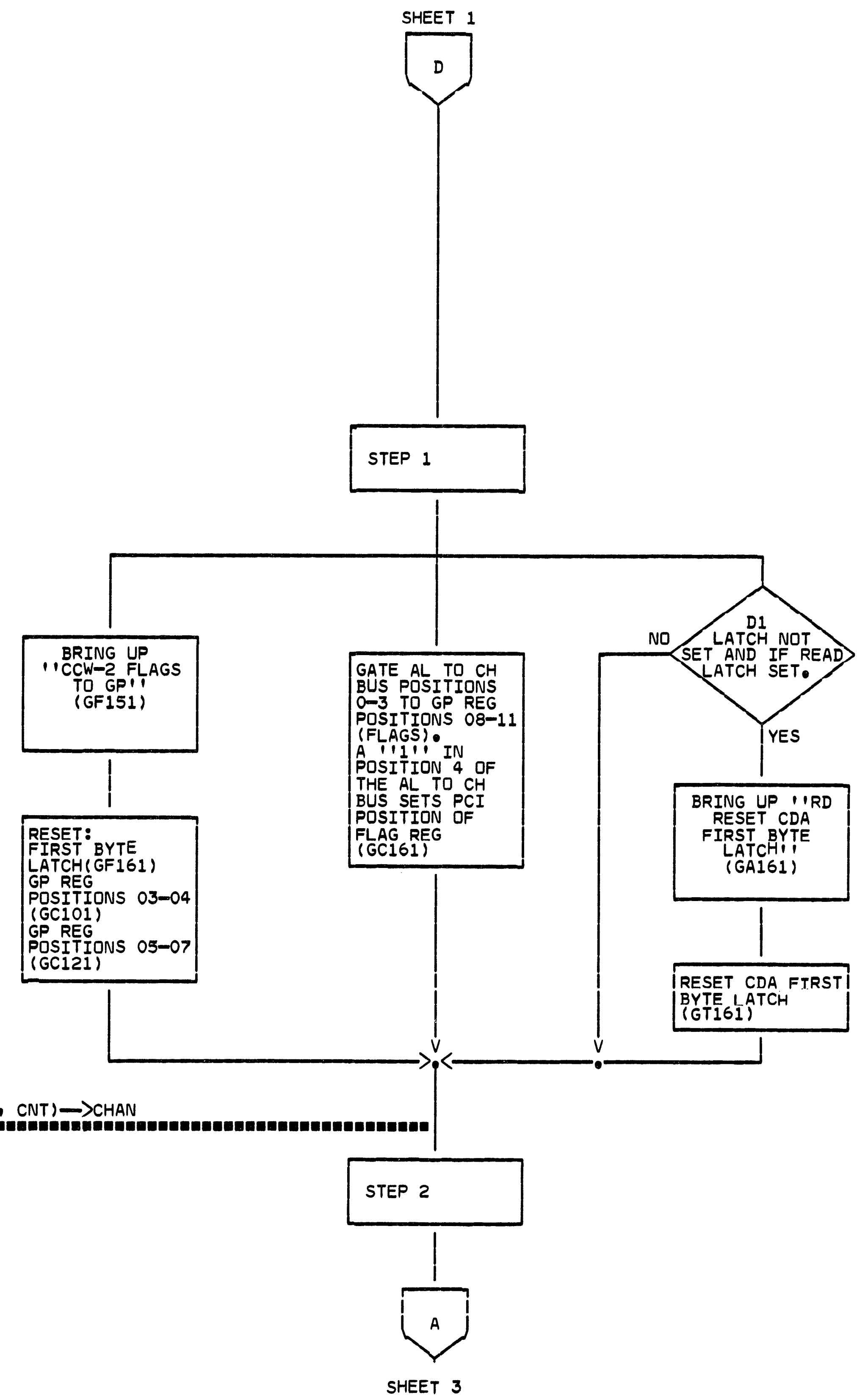
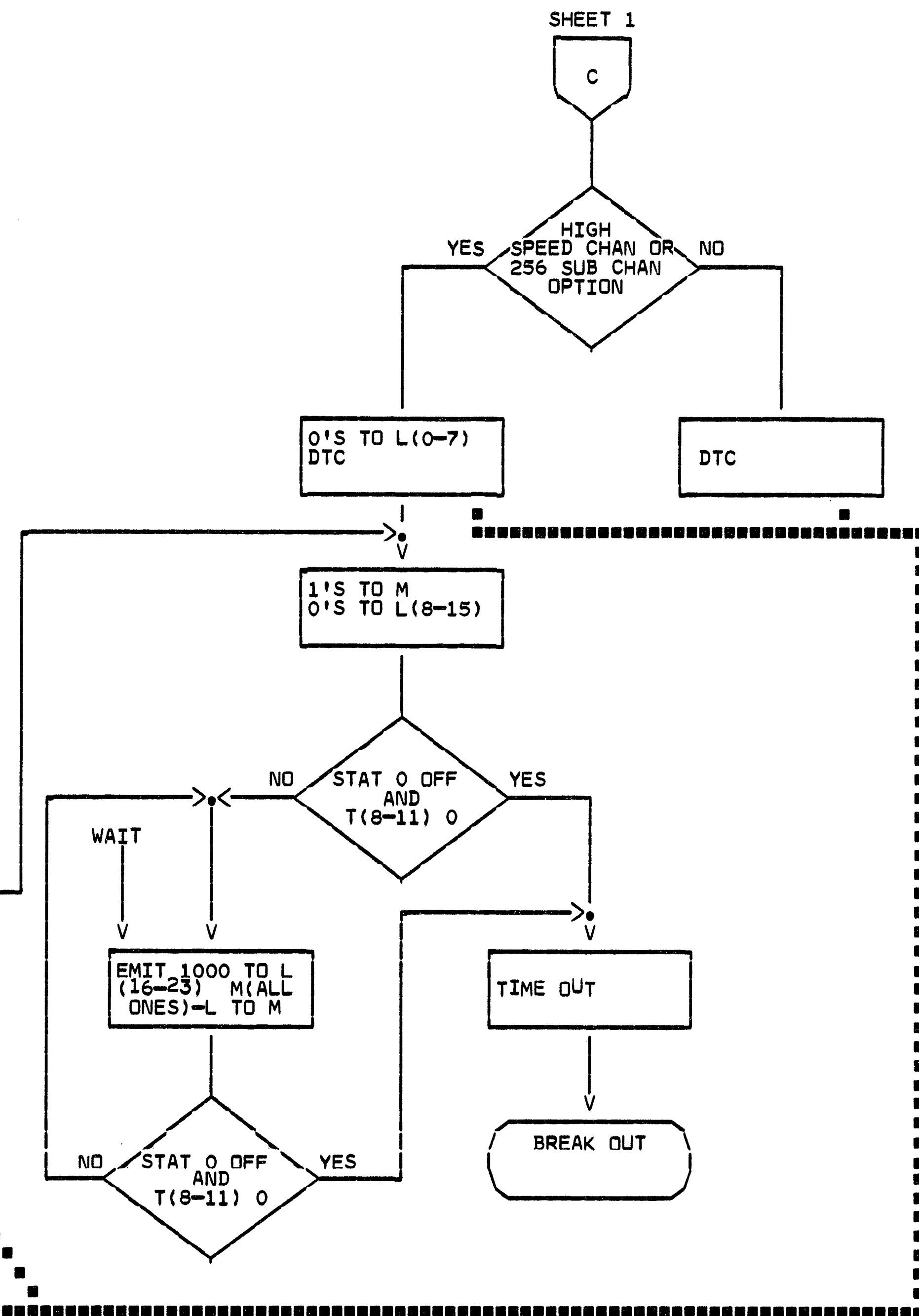
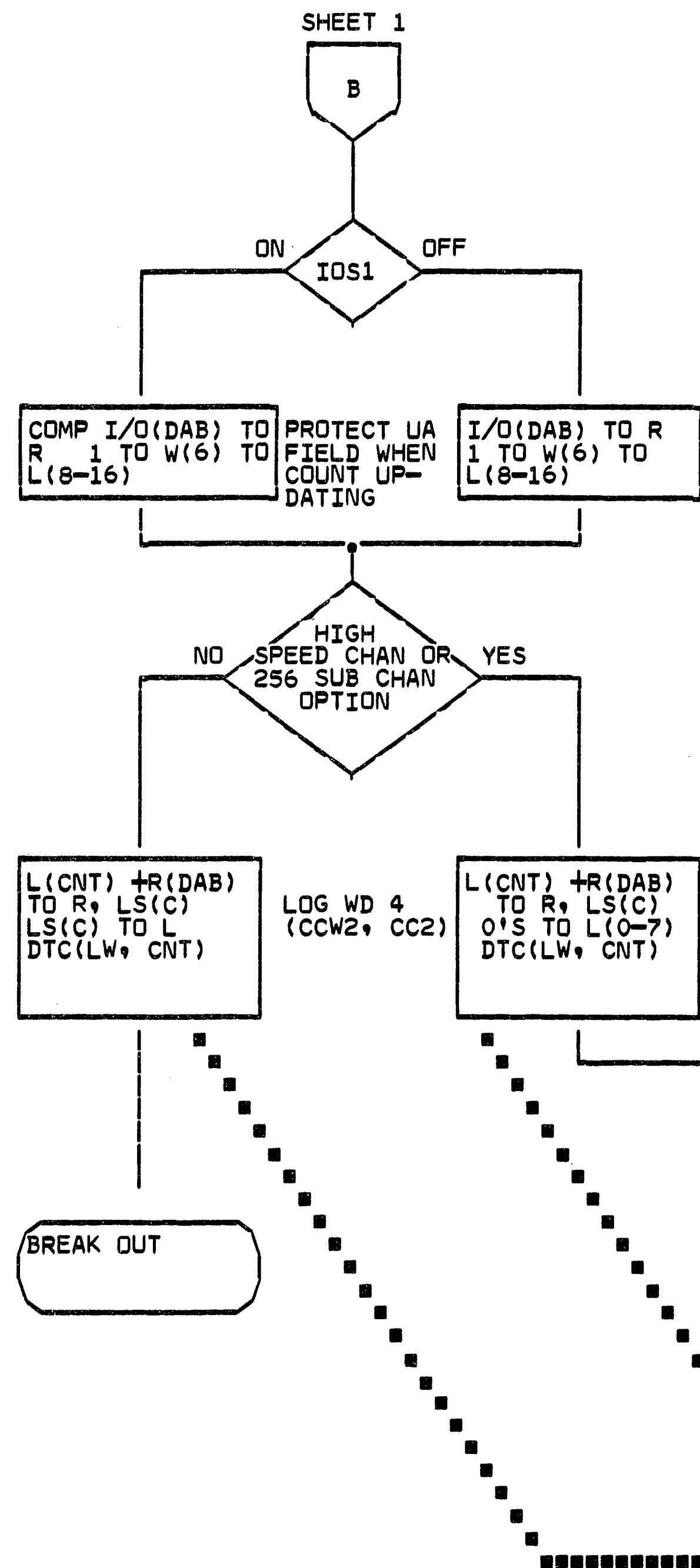


IBM CONFIDENTIAL

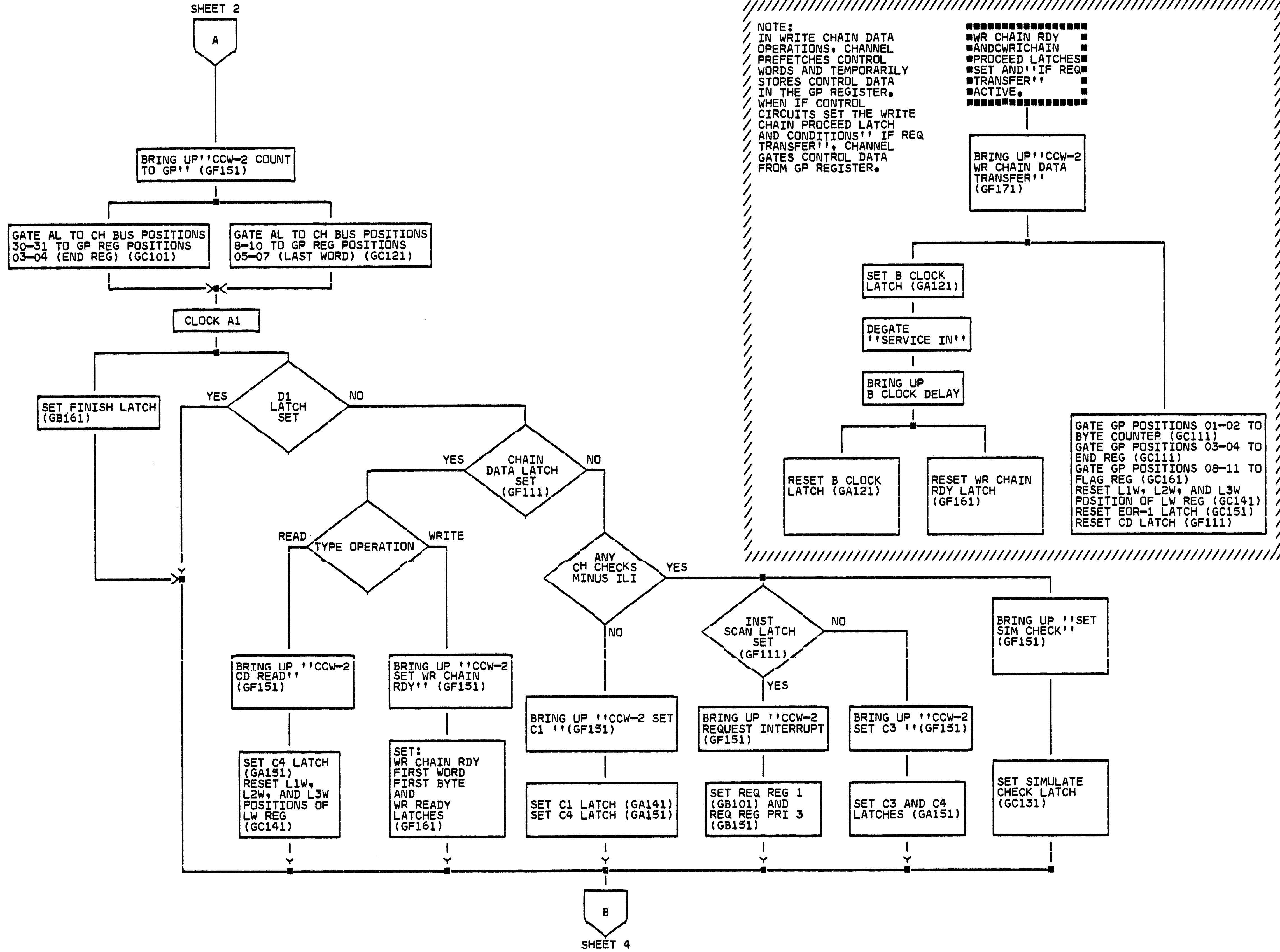




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SHEET 2



SHEET 4

IBM CONFIDENTIAL

IOP CCW-2 ROUTINE  
 (SELECTOR CHANNEL)  
 DATE 27 JUN 66 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE 5

S4002

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SHEET 3

B

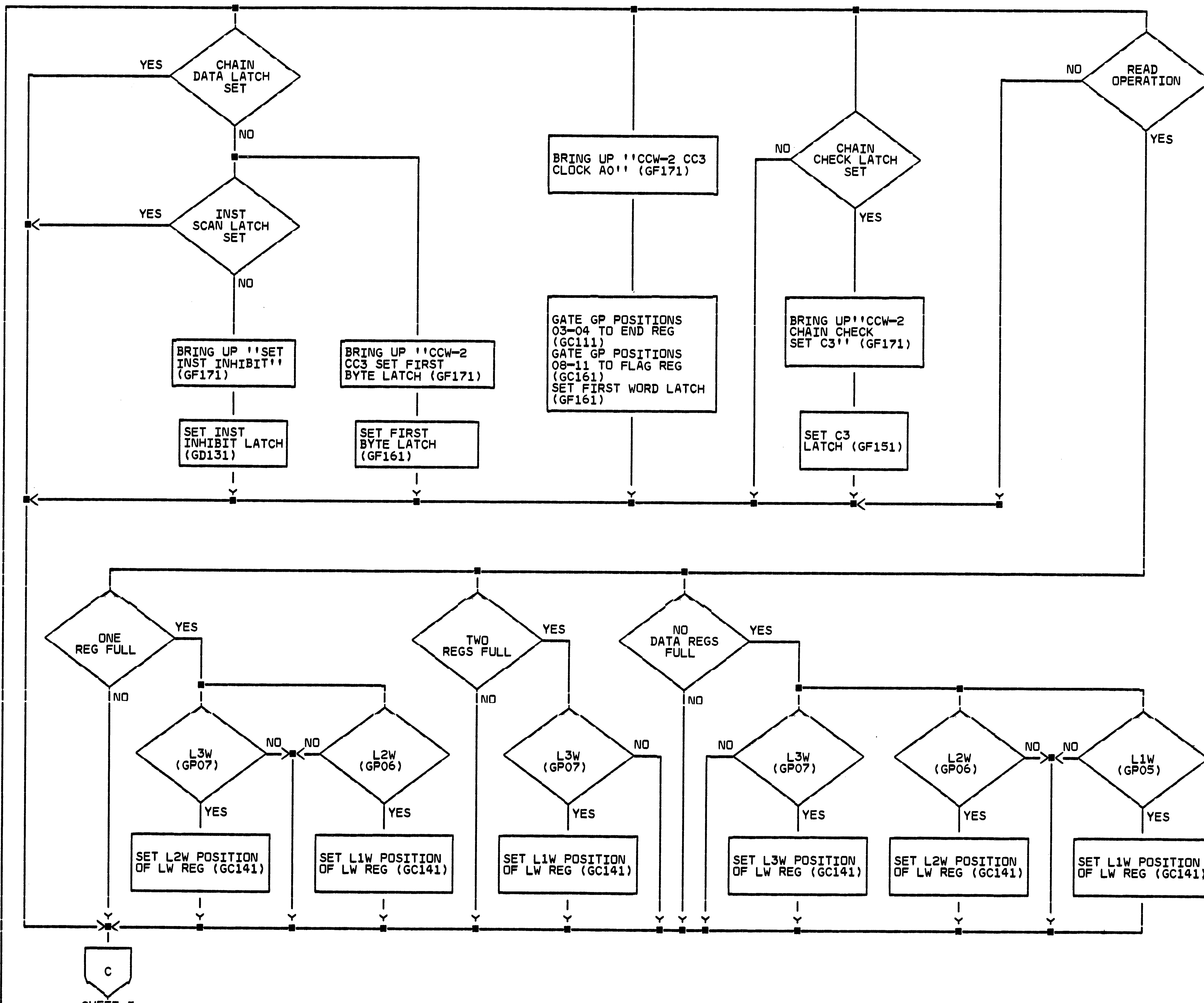
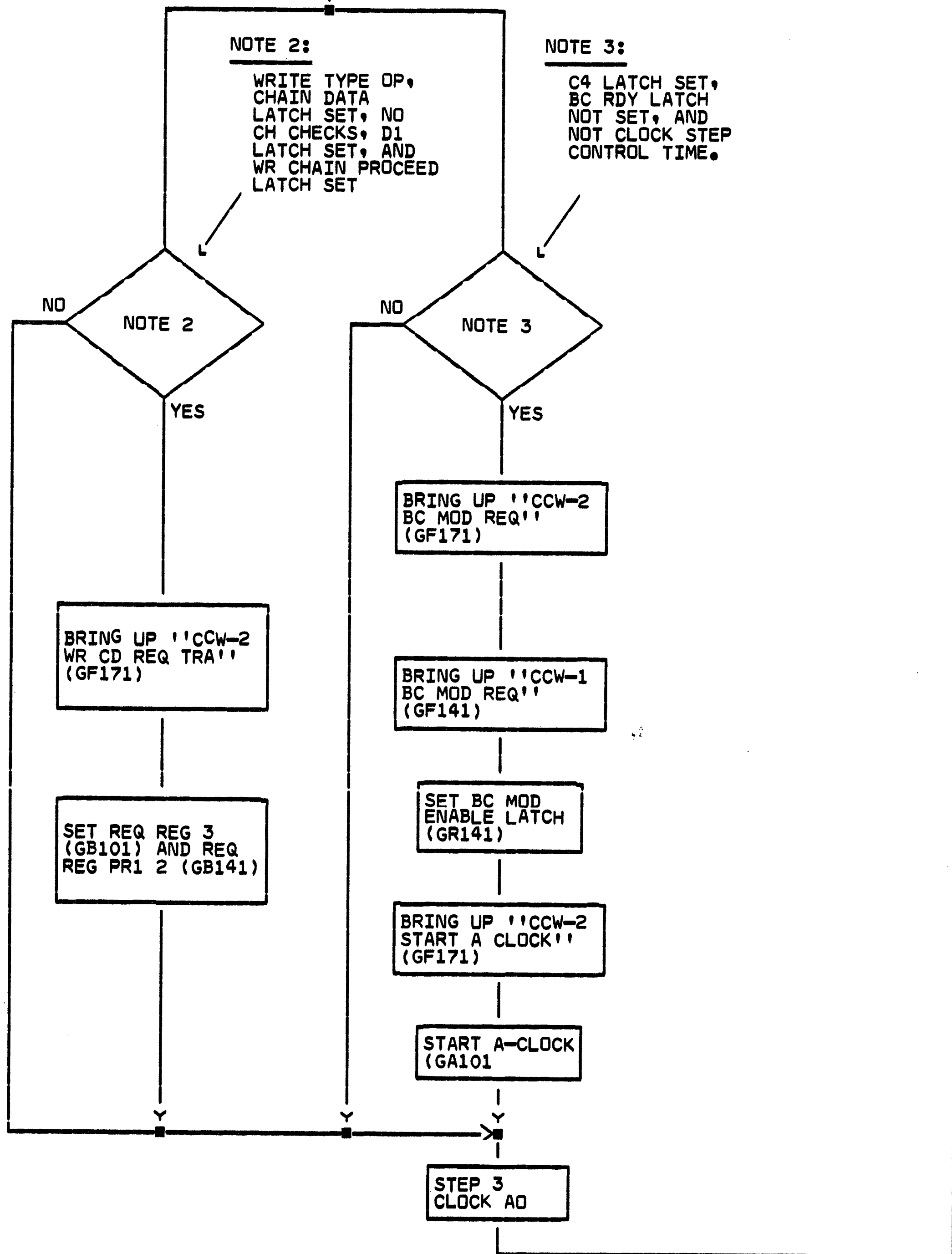
\*\*\*\*\*  
\* STEP 3 \*  
\*\*\*\*\*

NOTE 2:

WRITE TYPE OP,  
CHAIN DATA  
LATCH SET, NO  
CH CHECKS, D1  
LATCH SET, AND  
WR CHAIN PROCEED  
LATCH SET

NOTE 3:

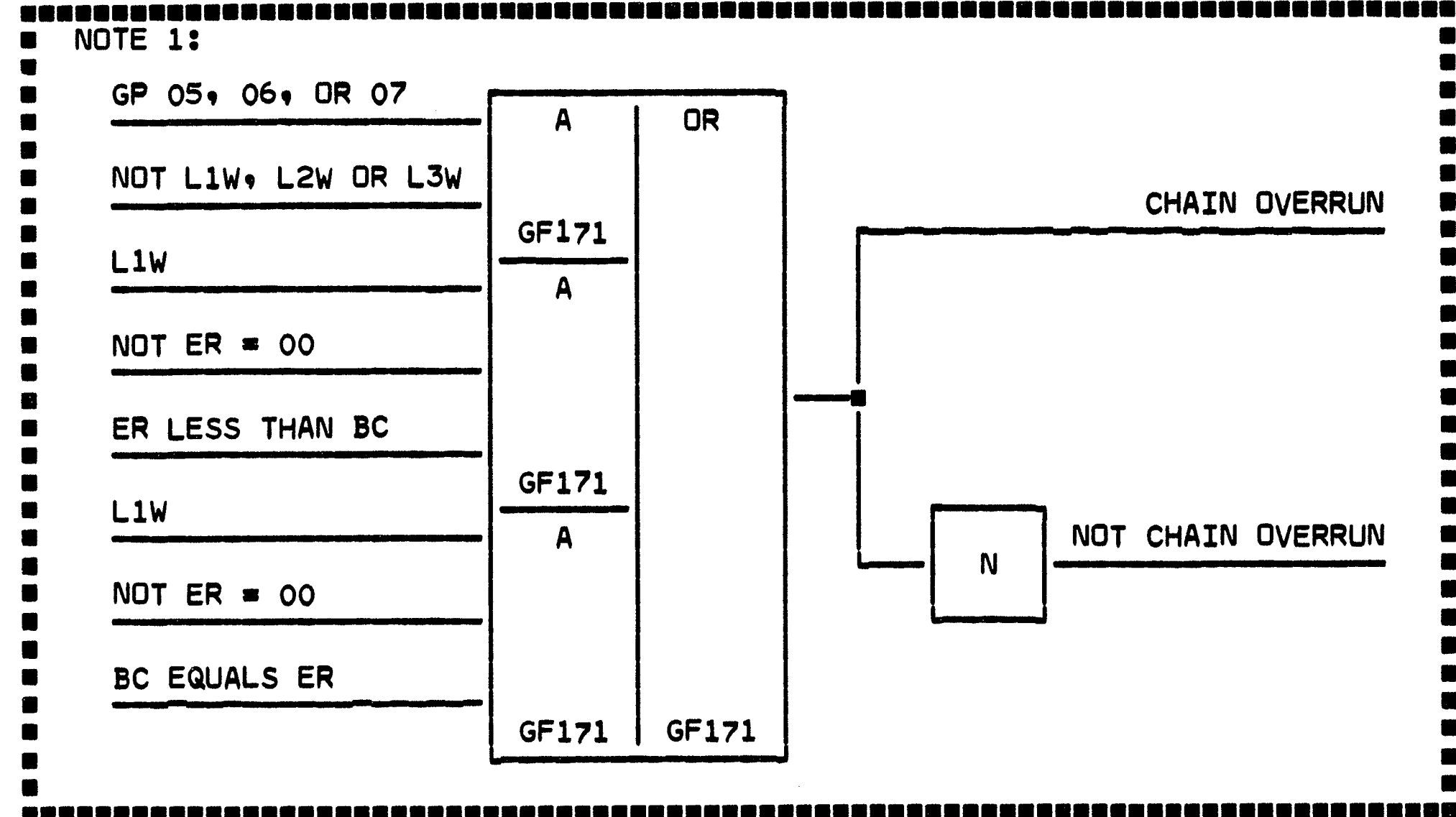
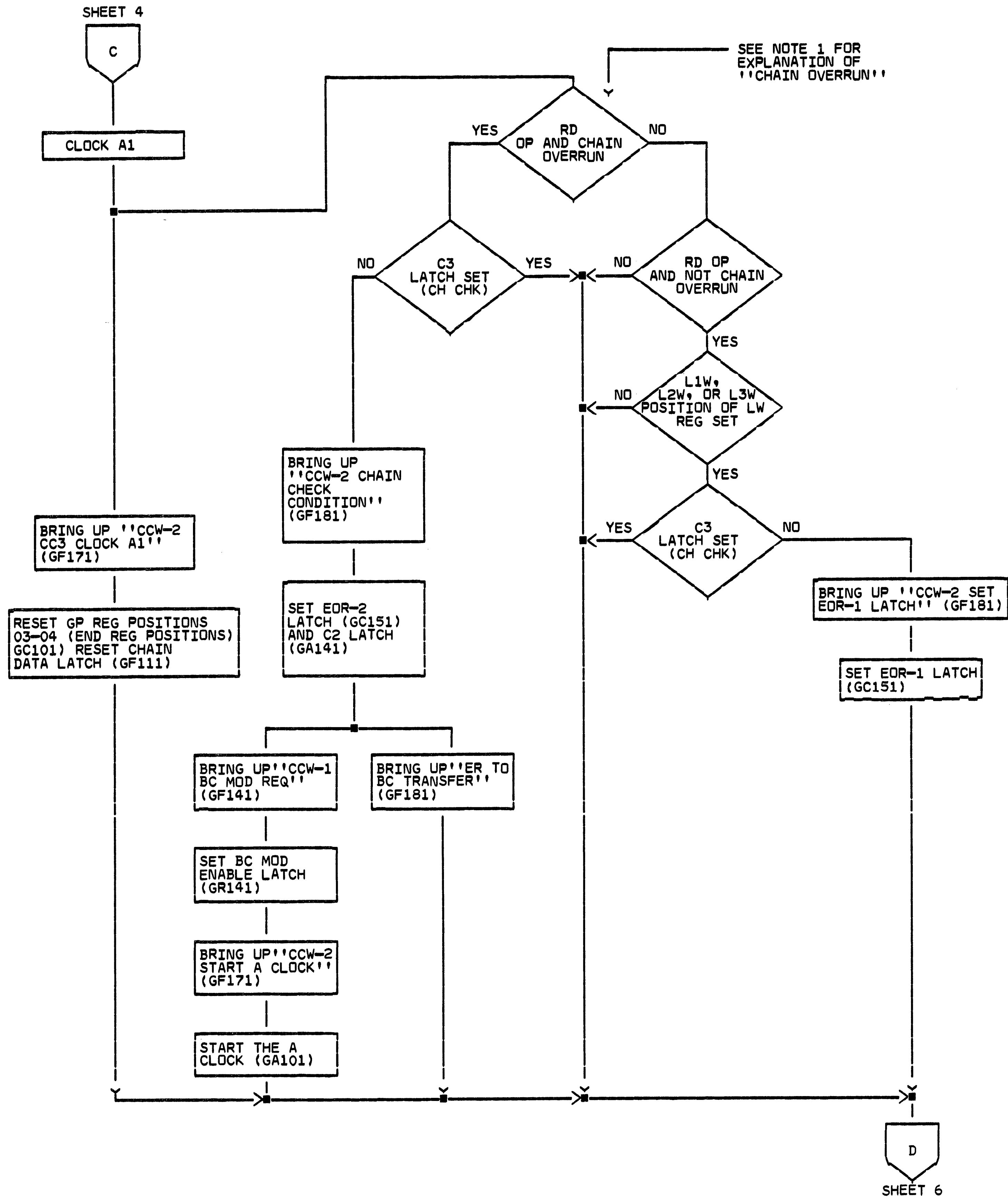
C4 LATCH SET,  
BC RDY LATCH  
NOT SET, AND  
NOT CLOCK STEP  
CONTROL TIME.



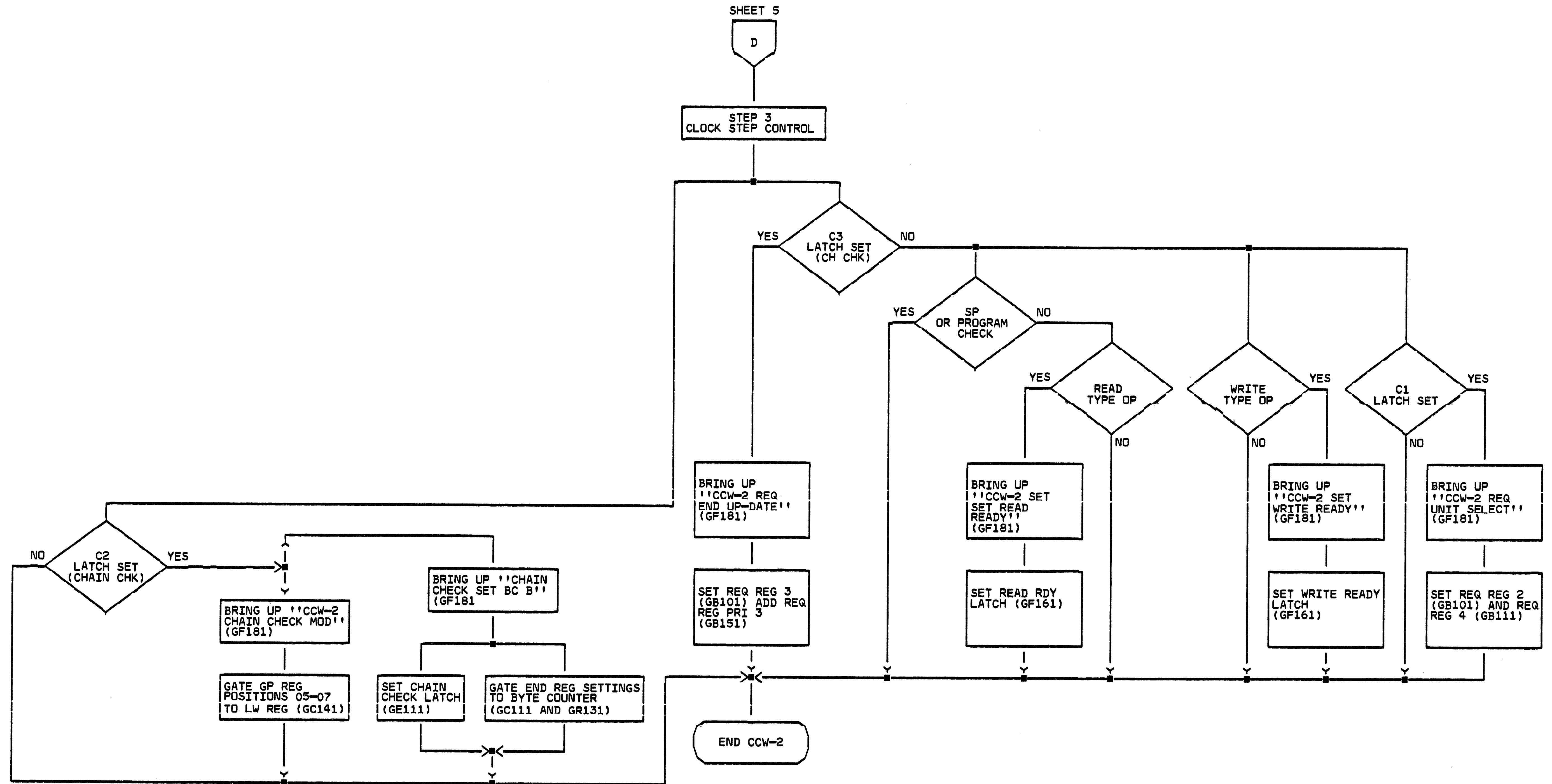
SHEET 5

C

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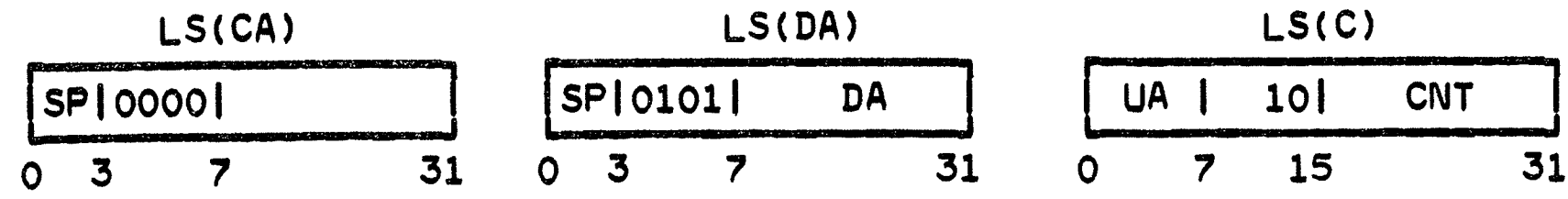
IBM CONFIDENTIAL



IOP CCW-2 ROUTINE  
 (SELECTOR CHANNEL)  
 DATE 27 JUN 66 MACH. 2050  
 FRAME  
 P. N.  
 IBM CORP. SDD PAGE 8

S4002

WRITE FETCH (OV104)



SHEET 3

LS(DA) TO R  
L TO LS(DA)

R(DA) +4 TO  
SAR, L, LS(C)  
LS(C) TO R  
DTC

LOG WD 4 (WR  
FETCH, CCD)  
DA UPDATE

T(8-11)=0  
HS CHAN

NOT T(8-11)=0,  
NOT HS CHAN

T(8-11)=0,  
HS CHAN

T(8-11)=0  
NOT HS CHAN

EMIT 000008XX  
TO L, M(ALL  
ONES) MINUS L  
TO M

TIME OUT

DTC → CHAN

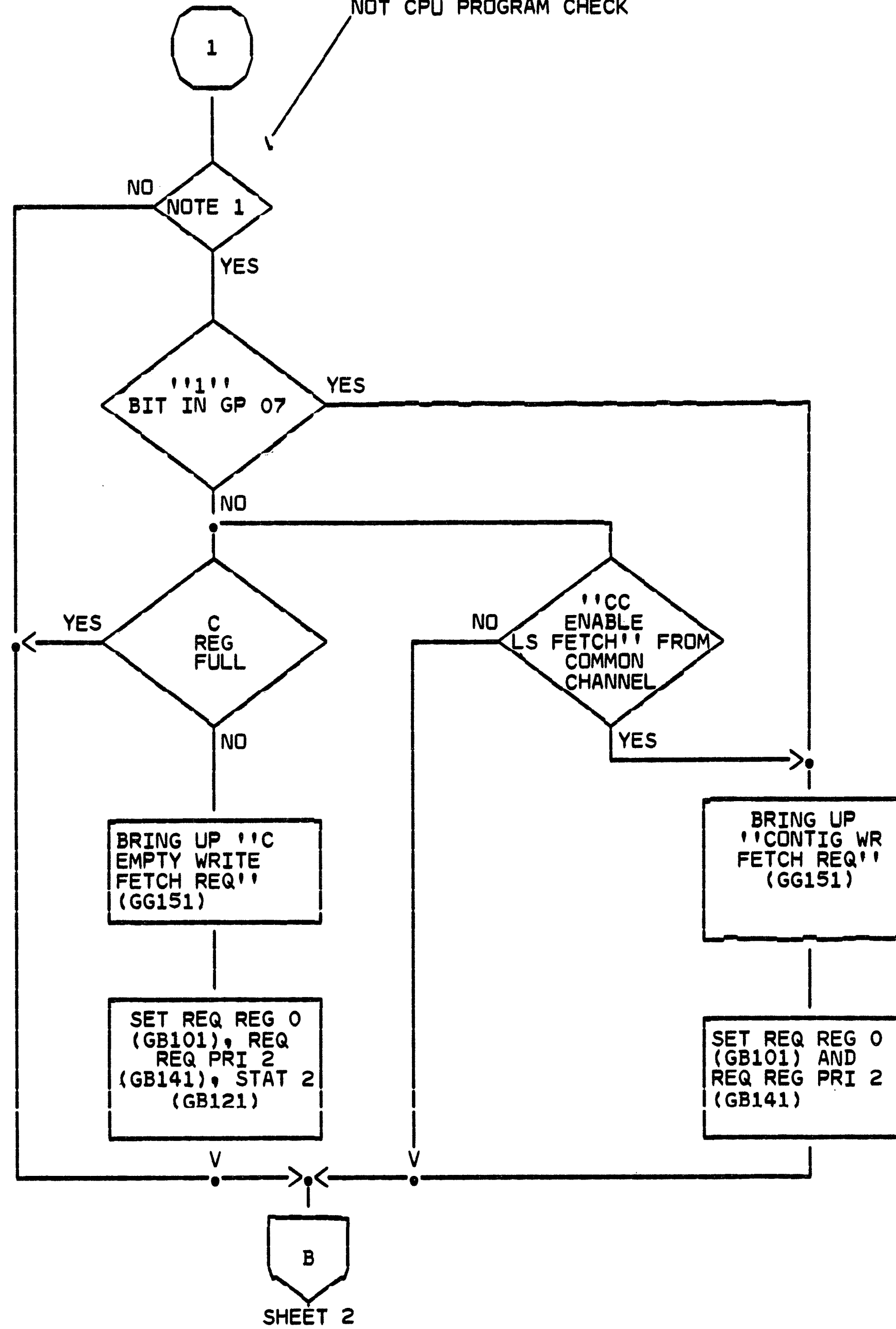
A  
SHEET 2

STEP 0  
PHASE B

1

'WRITE FETCH'  
(FROM POSITION  
REG) (GB181)

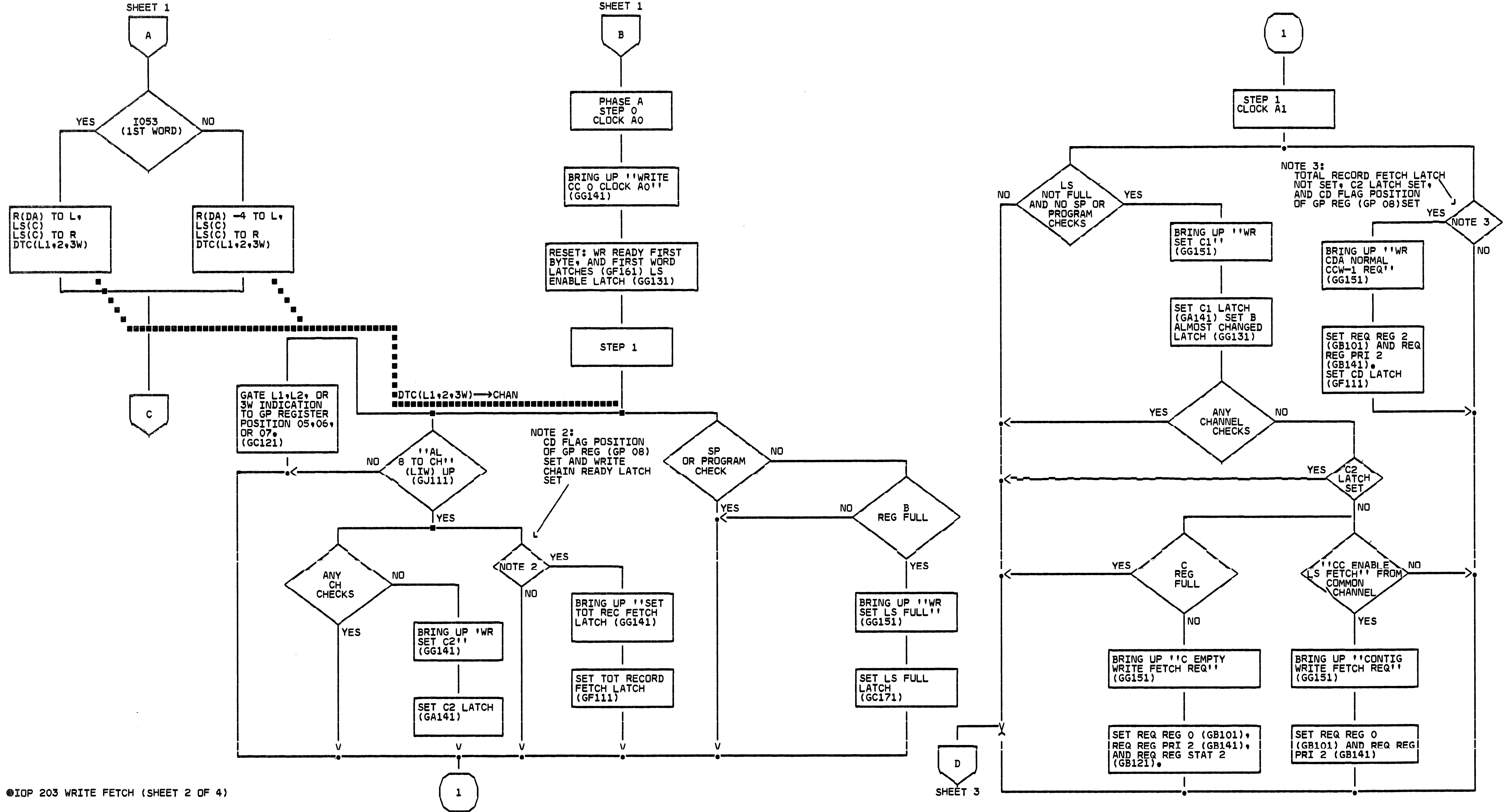
NOTE 1:  
NOT B REG FULL, PROGRAM  
CHECK LATCH NOT SET,  
NOT GP 05 OR 06, AND  
NOT CPU PROGRAM CHECK



B  
SHEET 2

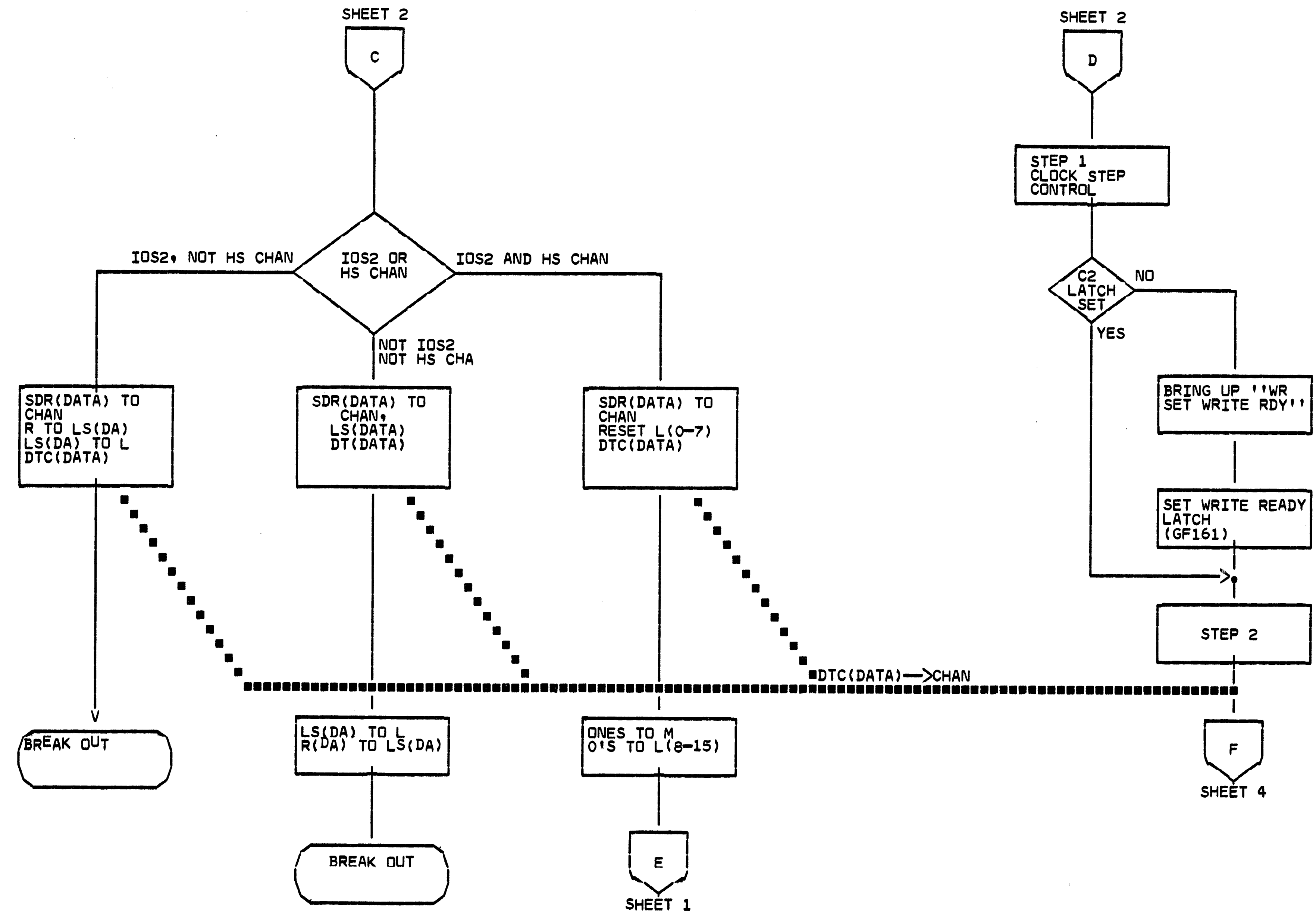
IBM CONFIDENTIAL

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WRITE FETCH  
(SELECTOR CHANNEL)  
DATE 27 JUN 66 MACH. 2050  
FRAME  
Page  
IBM CORP. PAGE 4

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● IOP 203 WRITE FETCH (SHEET 3 OF 4)

WRITE FETCH  
(SELECTOR CHANNEL)  
DATE 27 JUN 66 MACH. 2050

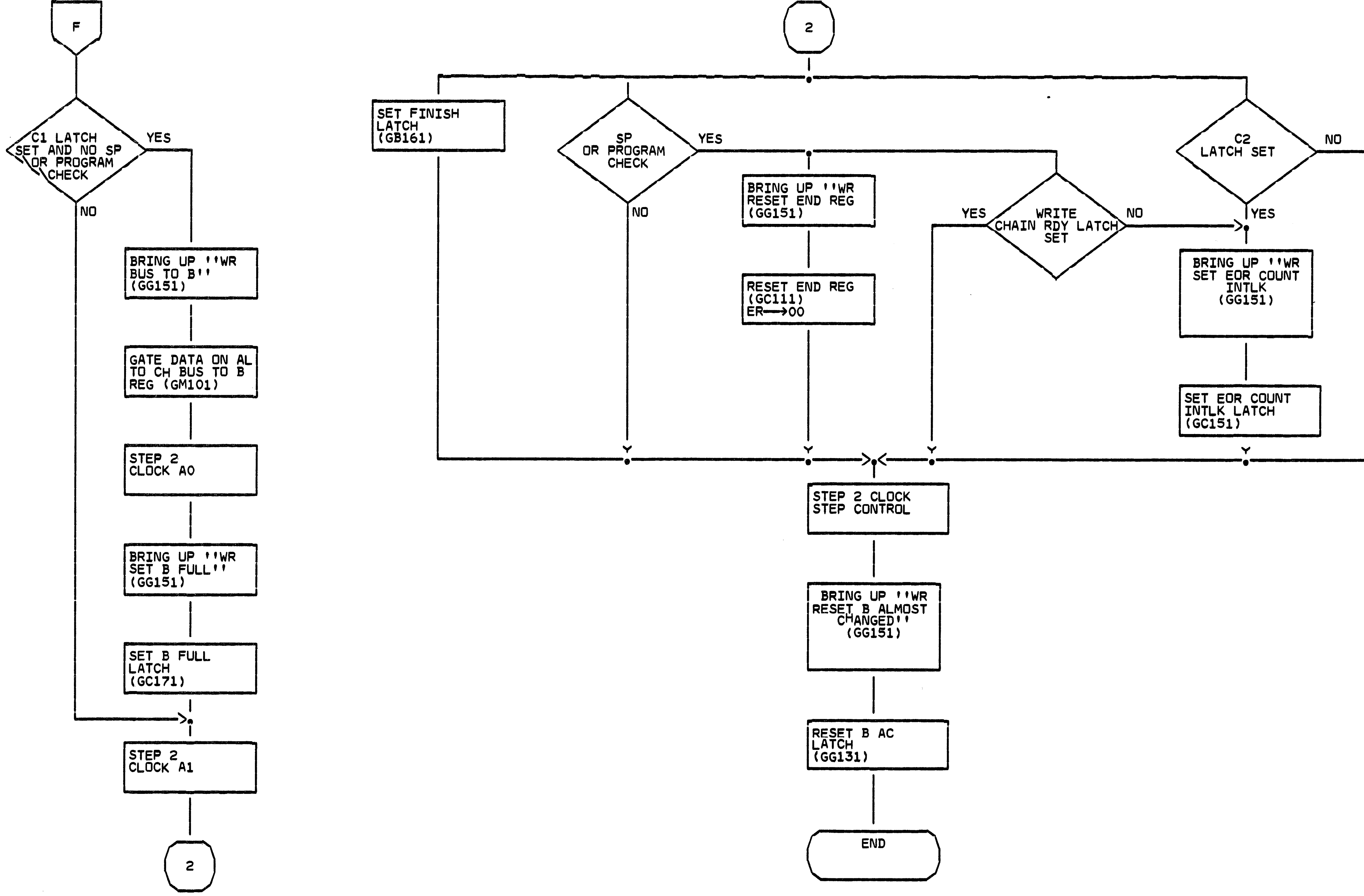
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PAGE

IBM CORP.

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3



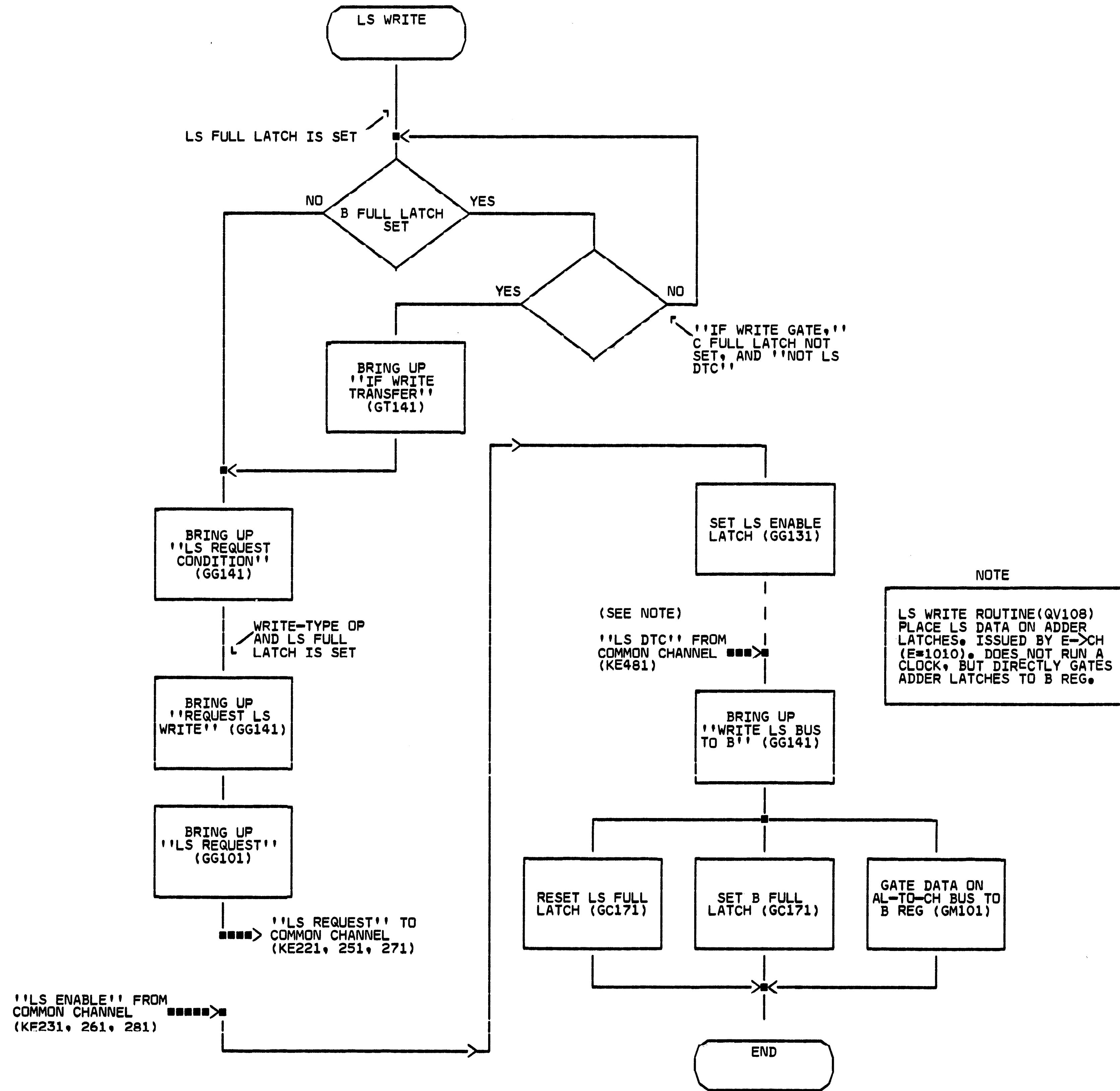
SHEET 3



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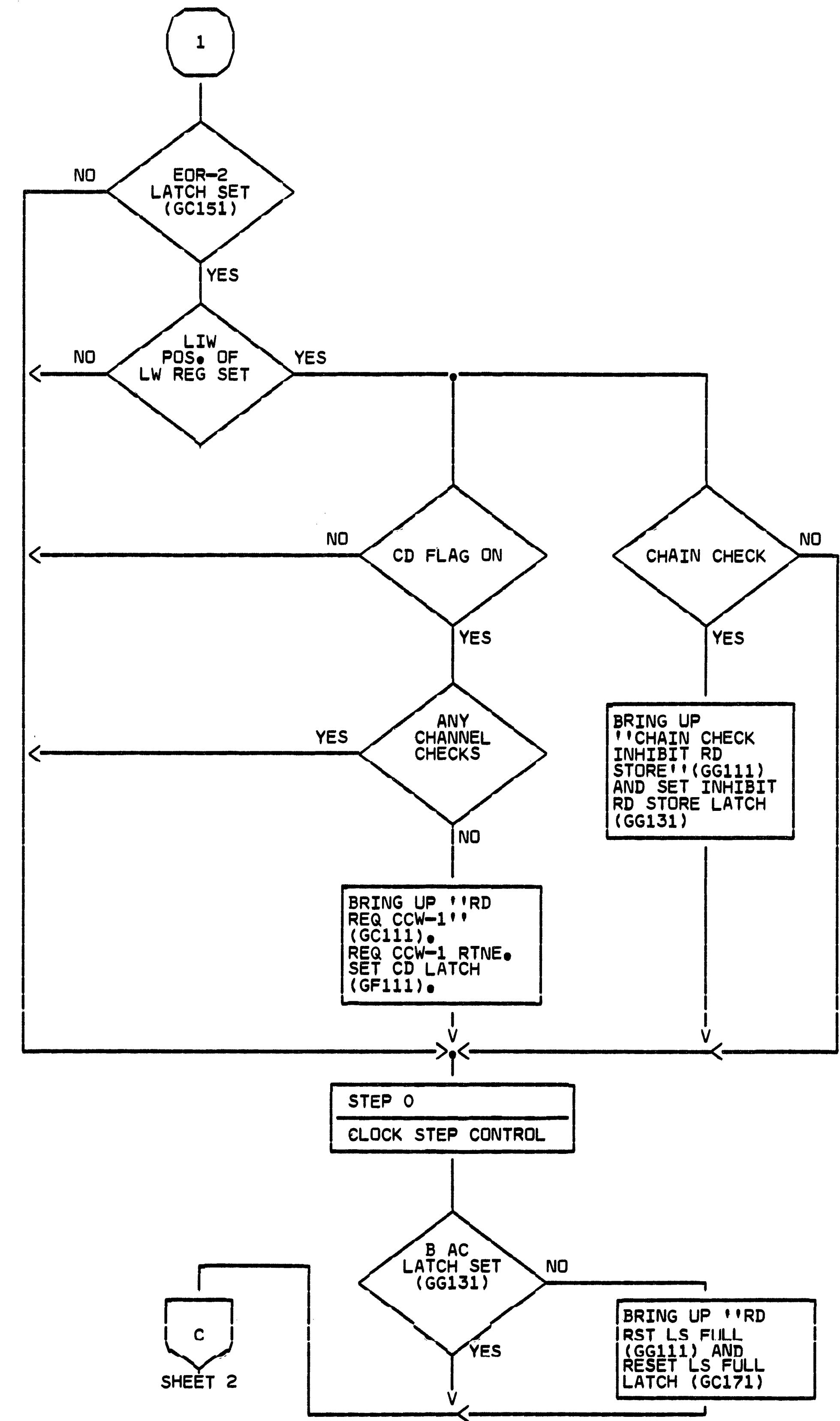
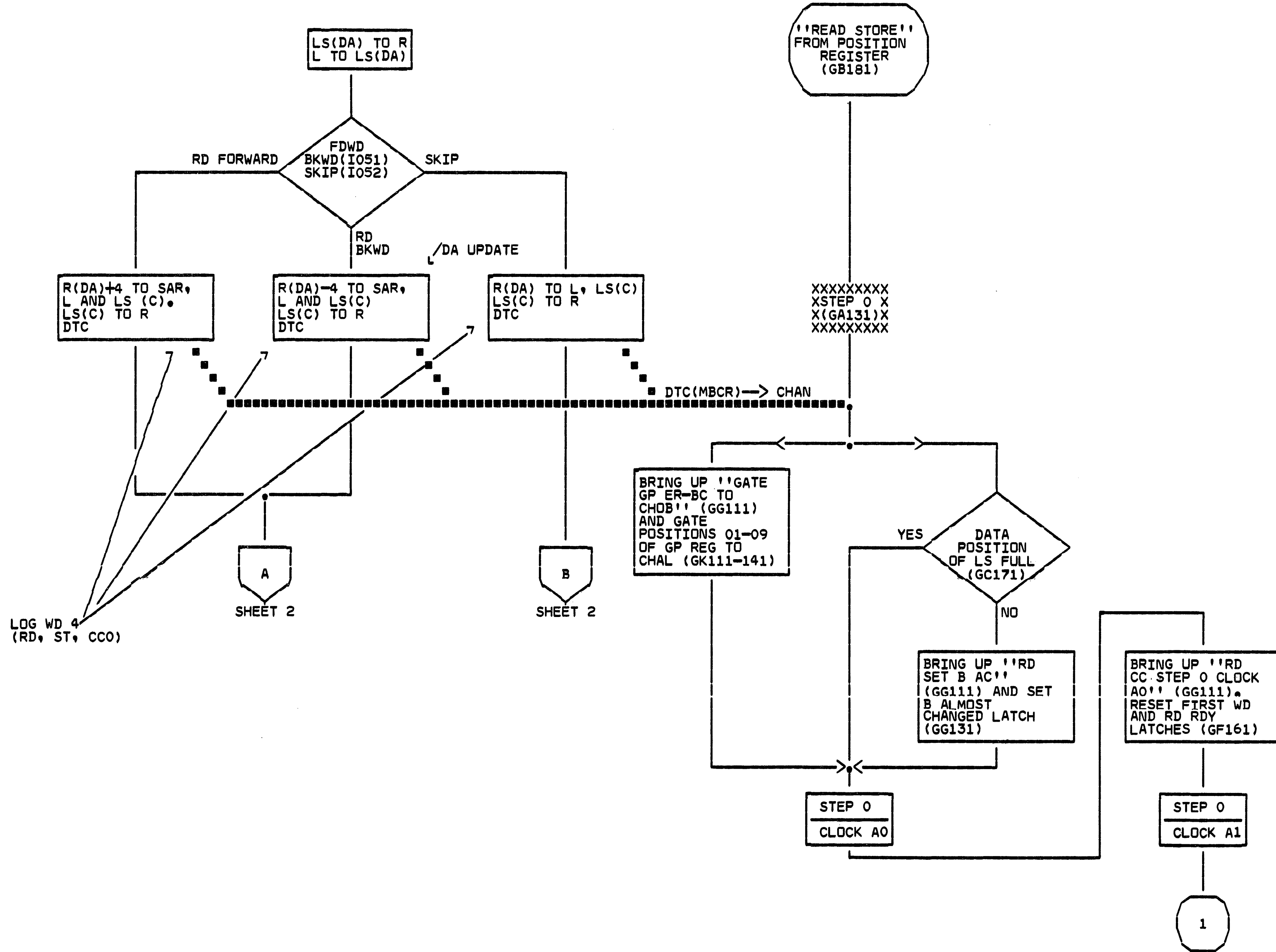
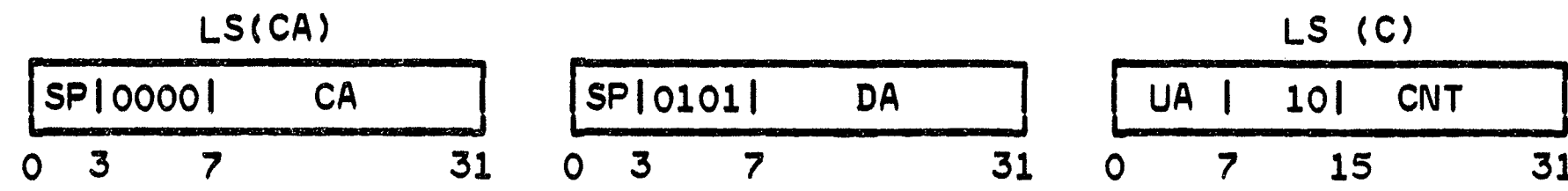


LOCAL STORE WRITE  
(SELECTOR CHANNEL)  
DATE 27 JUN 66 MACH. 2050

FRAME  
P.No.  
IBM CORP. SDD PAGE 2

S4004

READ STORE QV105



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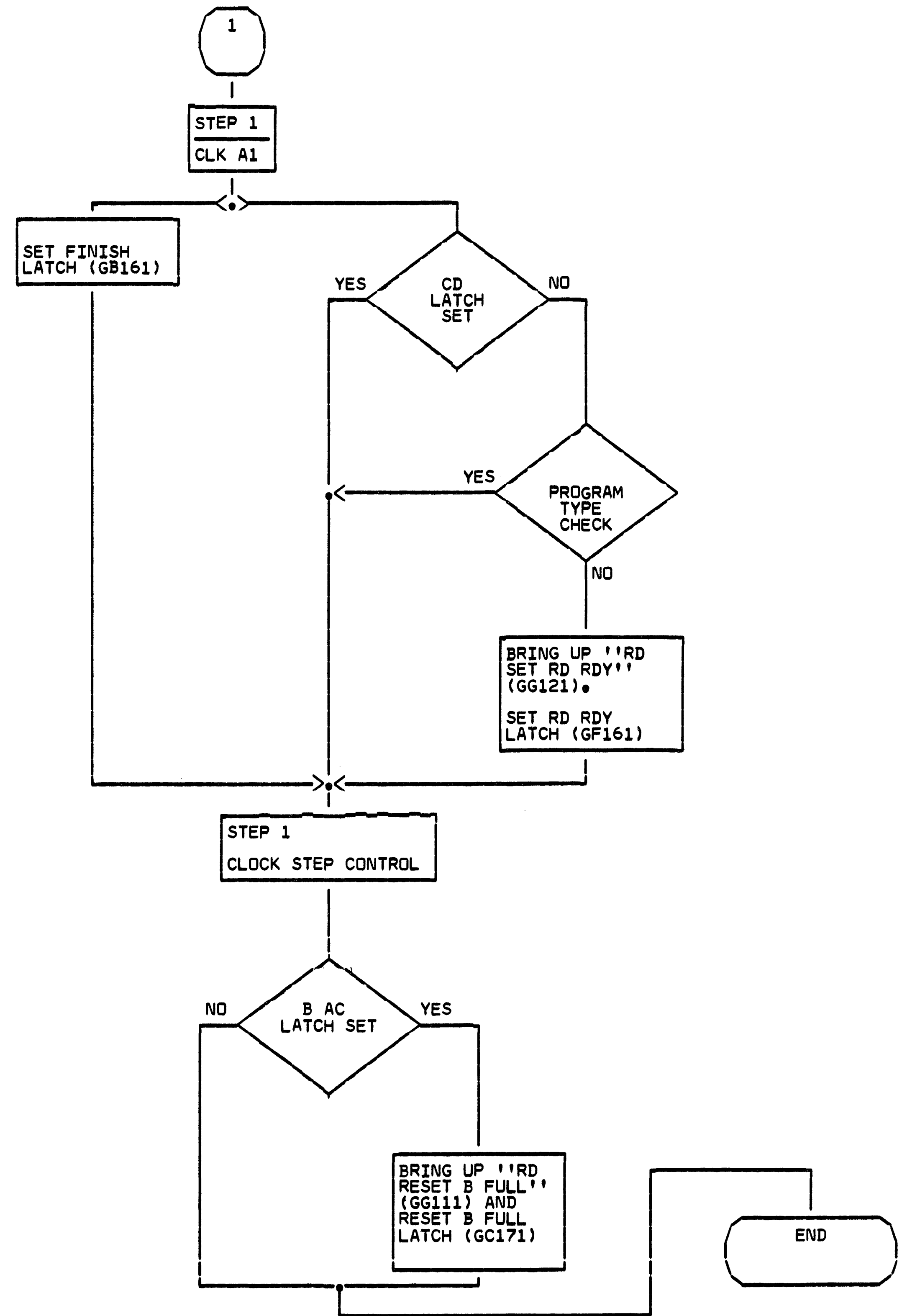
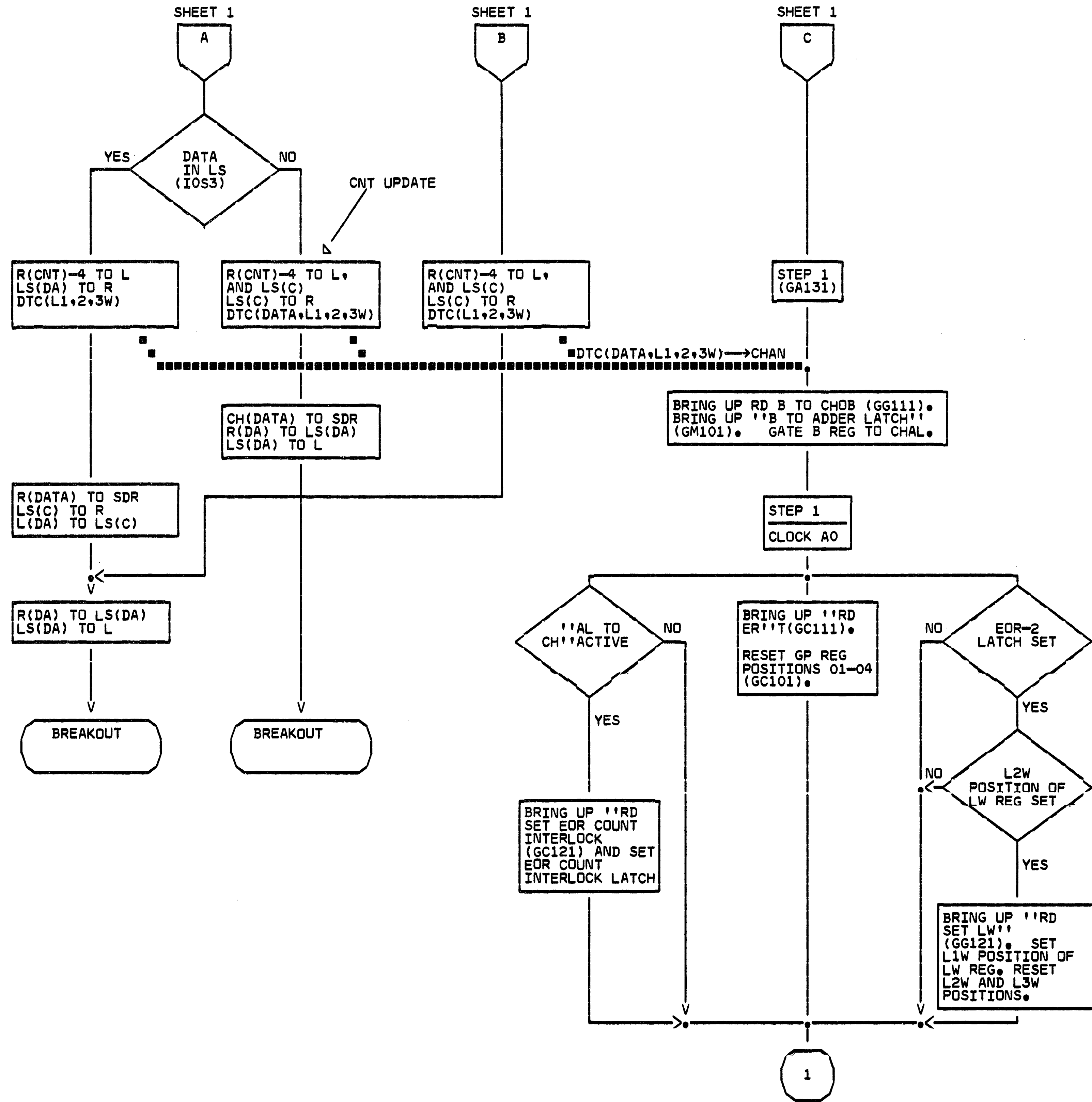
LOG WD 4 (RD, ST, CCO)

SHEET 2

SHEET 2

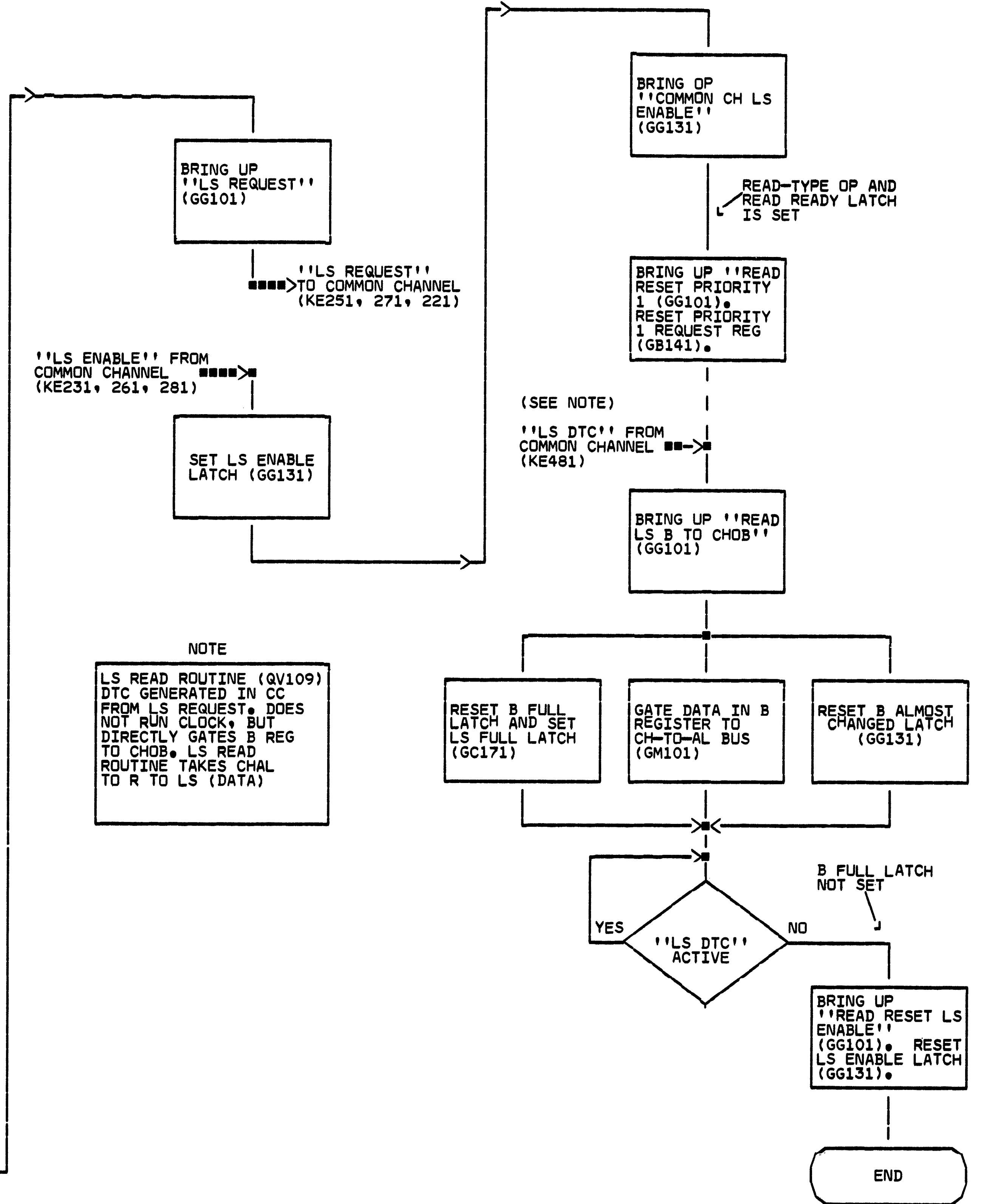
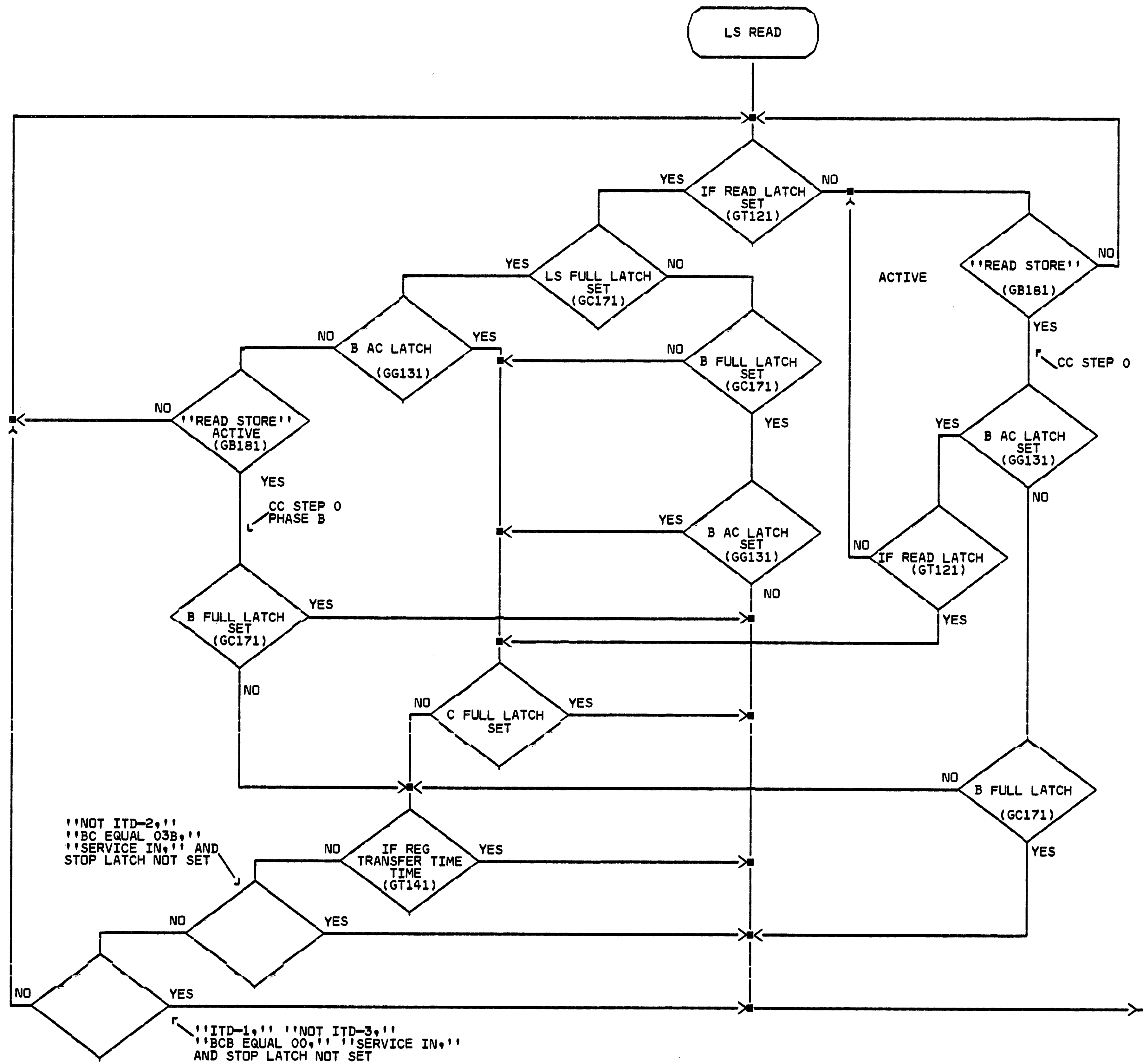
SHEET 2

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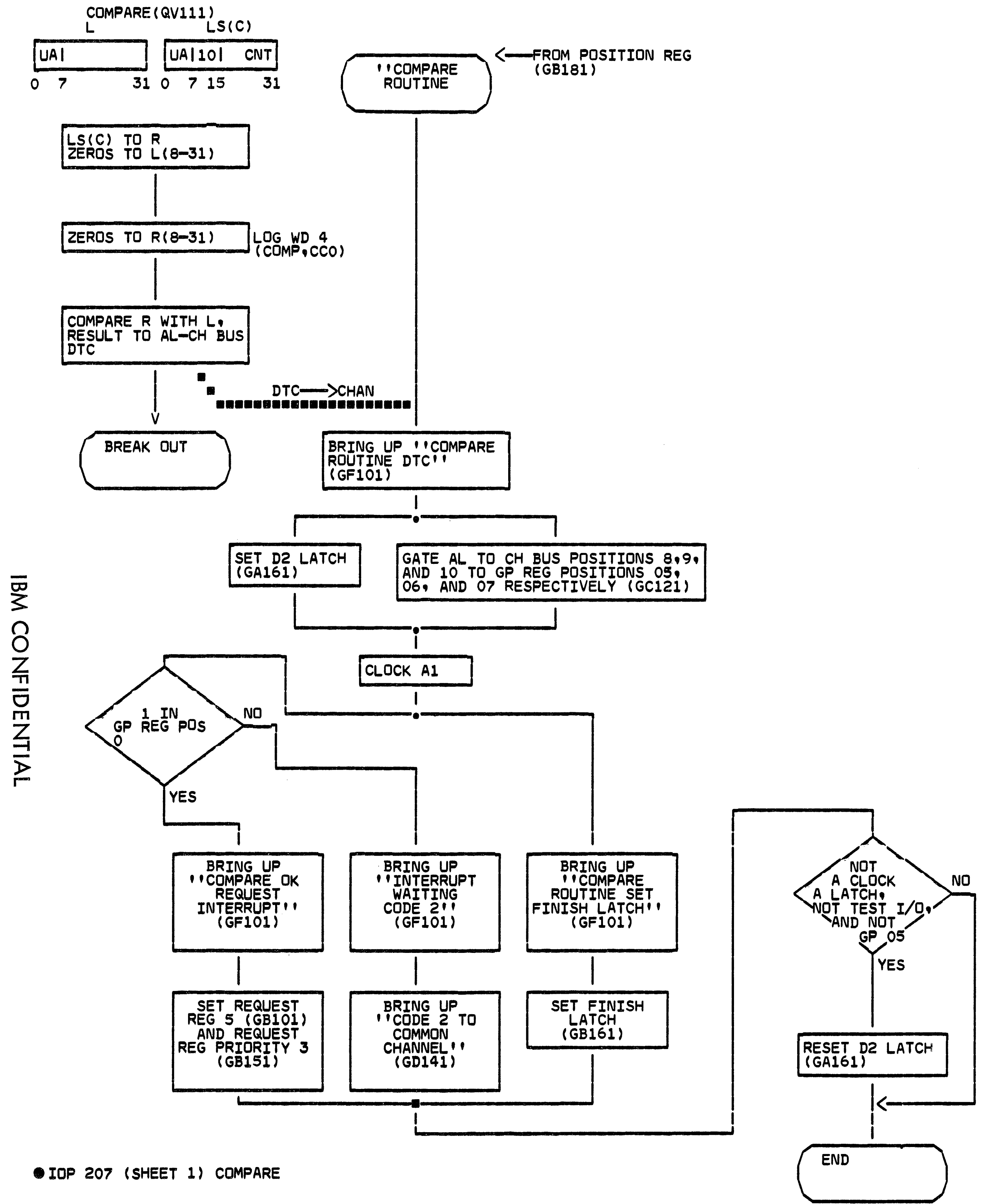
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NOTE  
 LS READ ROUTINE (QV109) DTC GENERATED IN CC FROM LS REQUEST, BUT DOES NOT RUN CLOCK, BUT DIRECTLY GATES B REG TO CHOB. LS READ ROUTINE TAKES CHAL TO R TO LS (DATA)

LOCAL STORE READ (SELECTOR CHANNEL)  
 DATE 27 JUN 66 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE 1

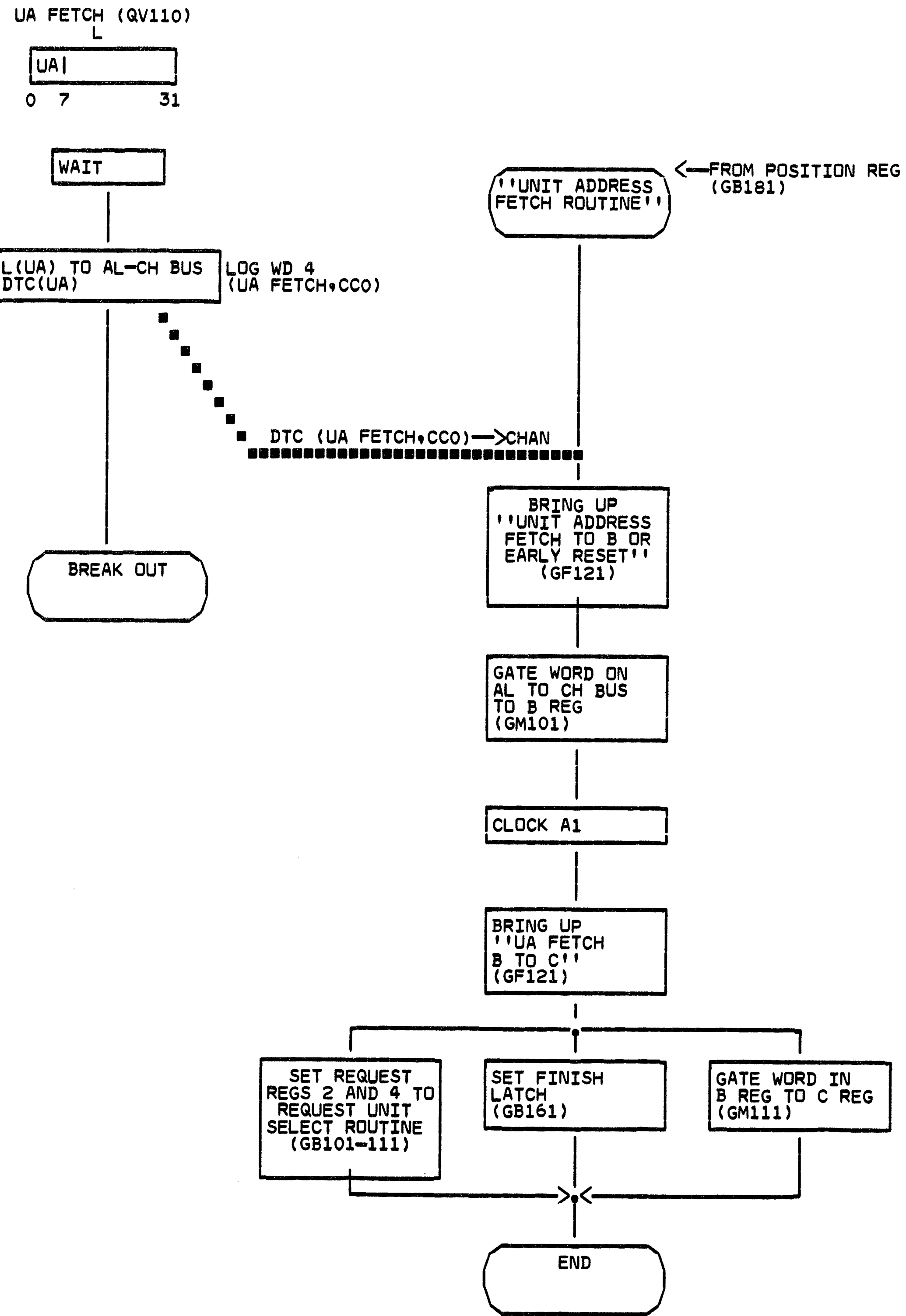
S4006



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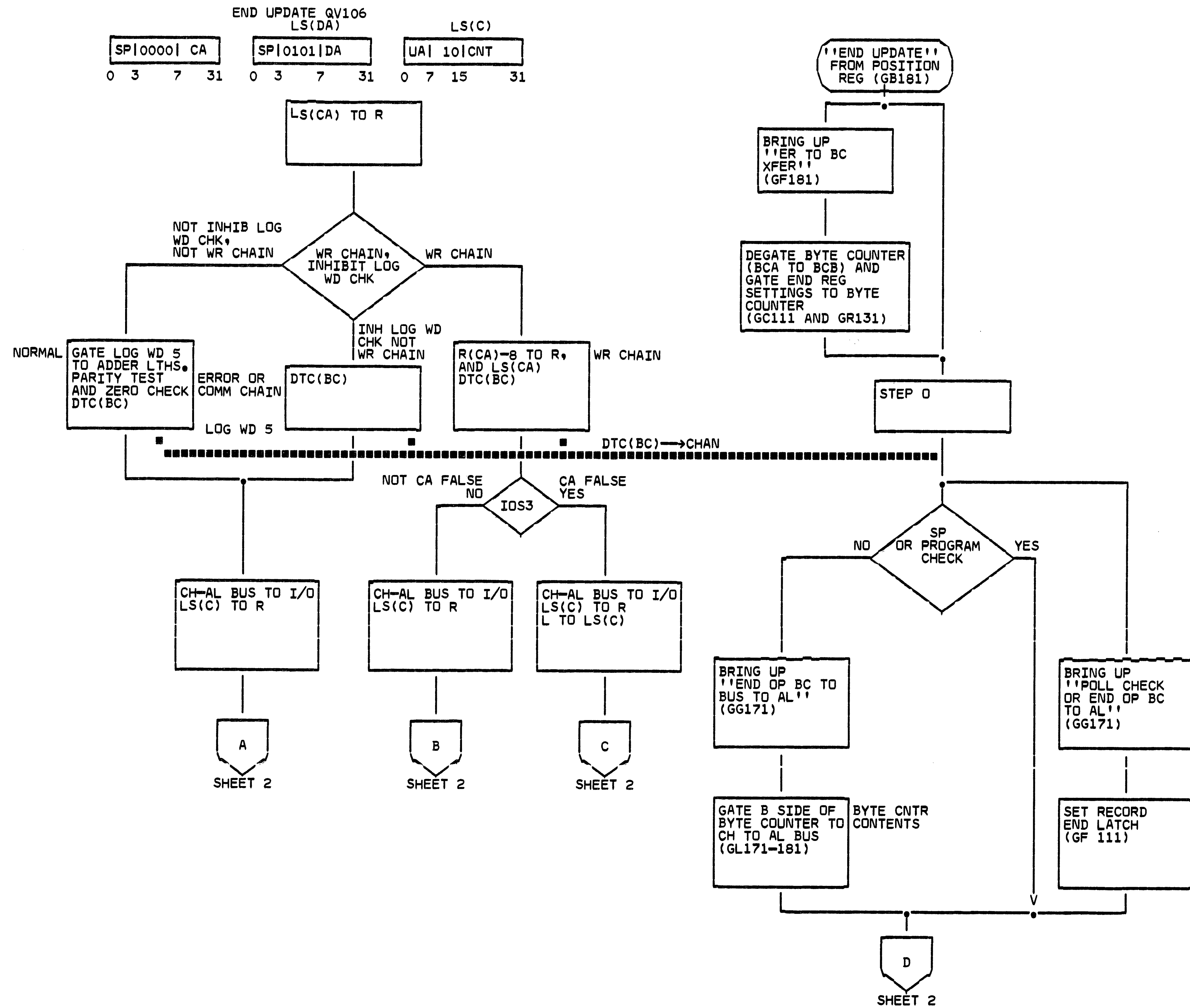
S4007





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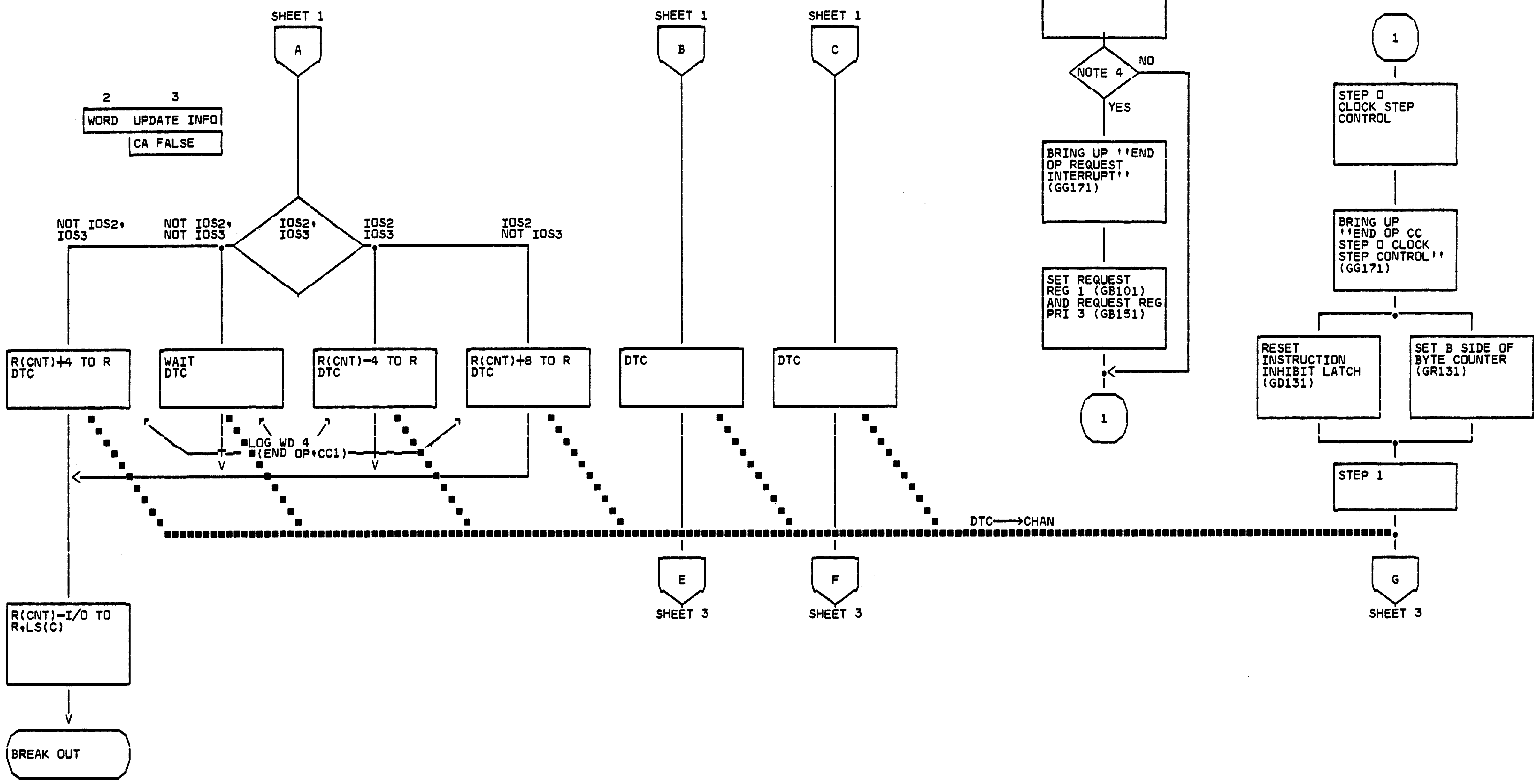




I/O STATS UPON ENTRY TO END UPDATE:  
 STAT 1 — WR CHAIN DATA AND NEW CCW NOT USED  
 STAT 2 — NOT 2 REGS FULL AND NOT 1 REG FULL  
 STAT 3 — NOT 1 REG FULL AND NOT 3 REGS FULL

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● IOP 208 END UPDATE (SHEET 2 OF 3)

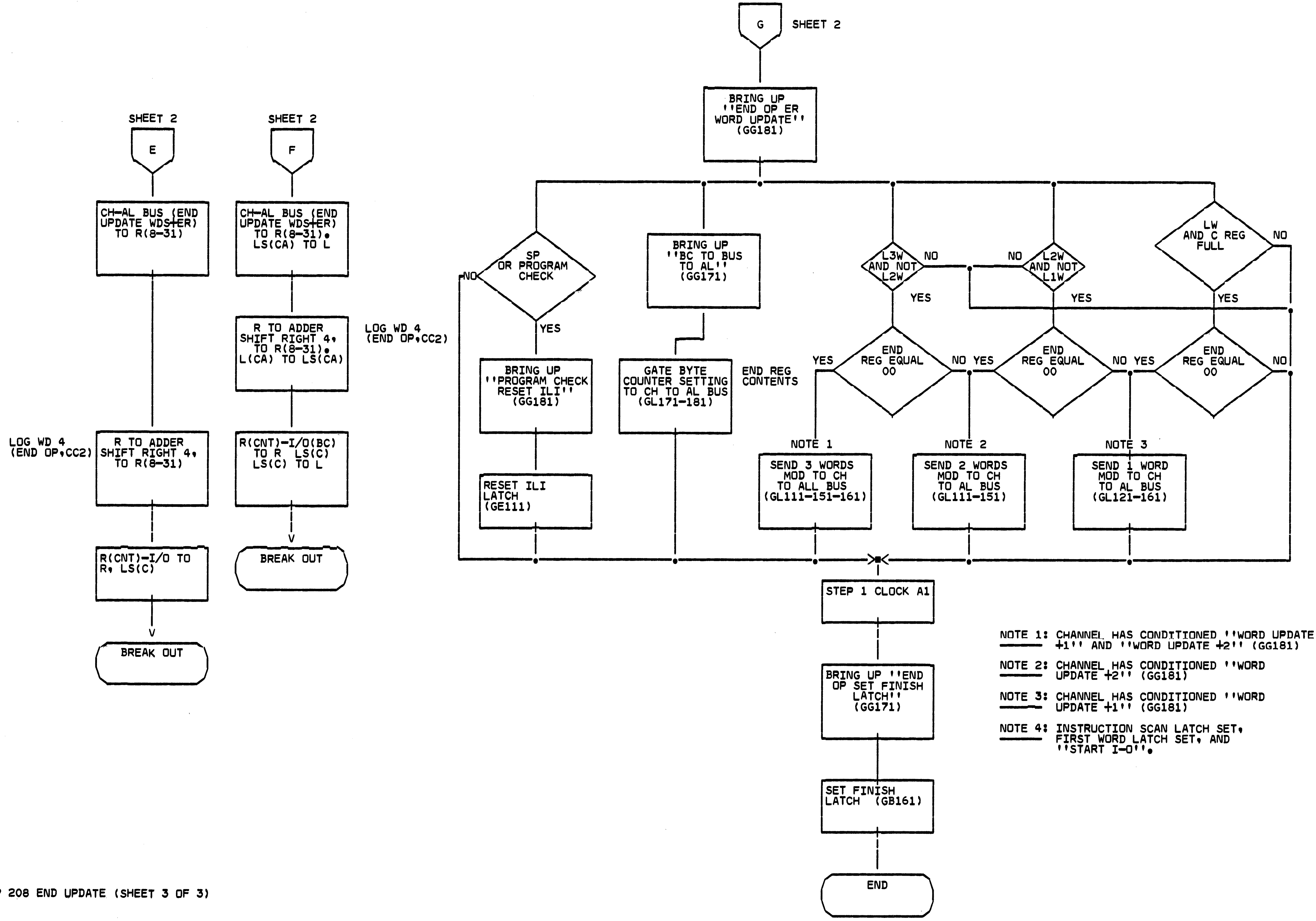
END UPDATE  
 (SELECTOR CHANNEL)  
 DATE 27 JUN 66 MACH. 2050

FRAME  
 P.No.

IBM CORP. SDD PAGE 3

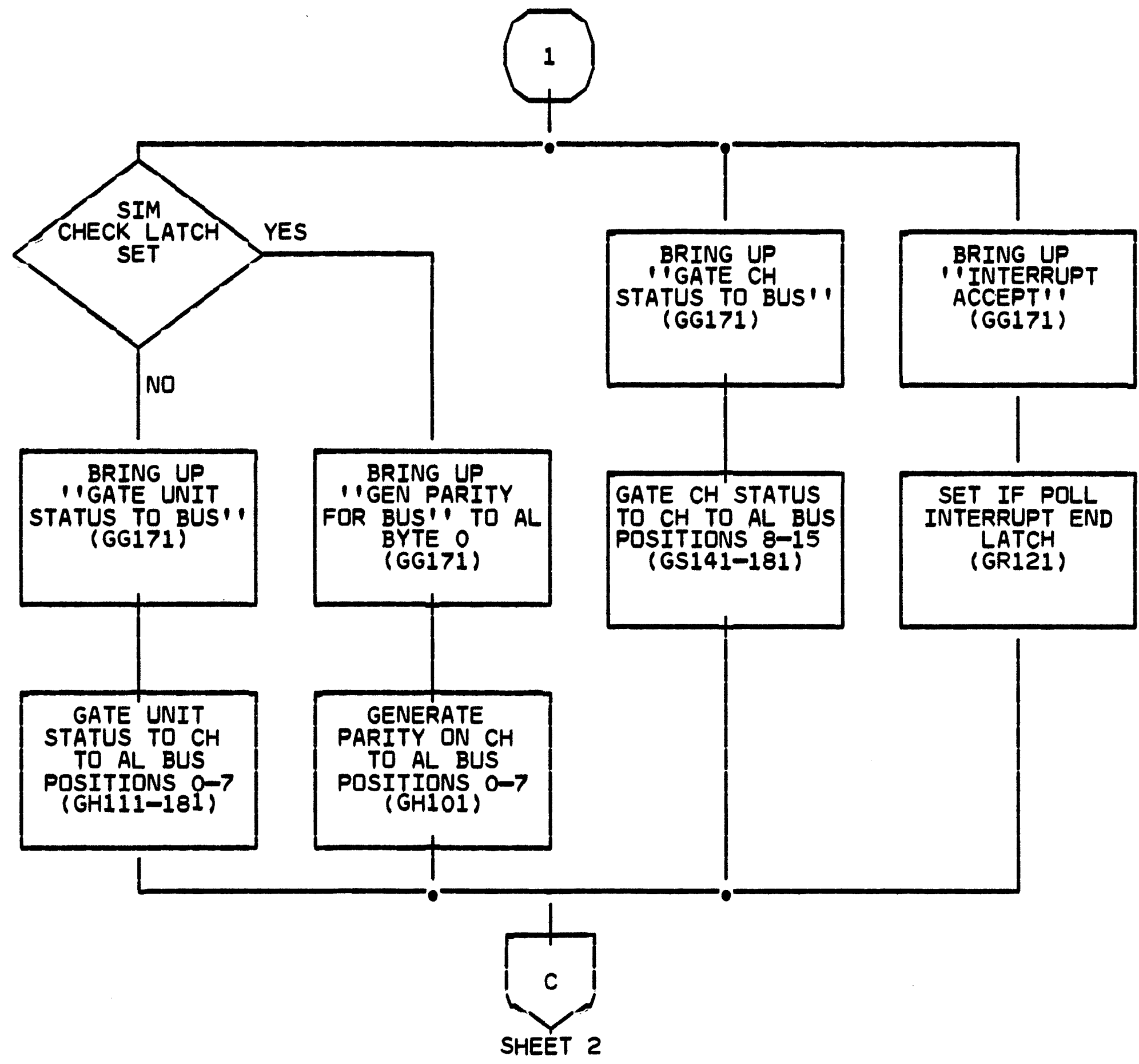
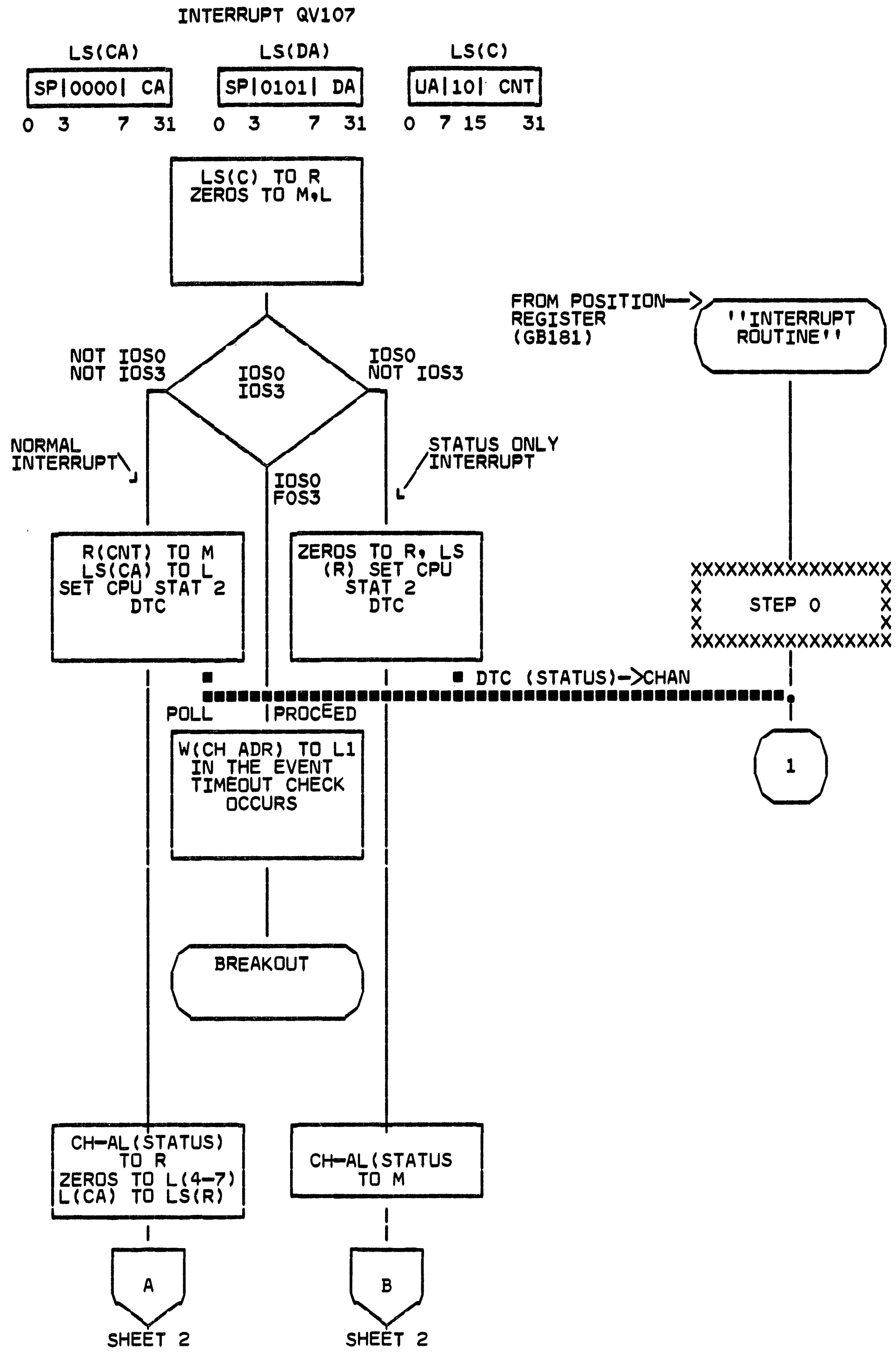
S4008

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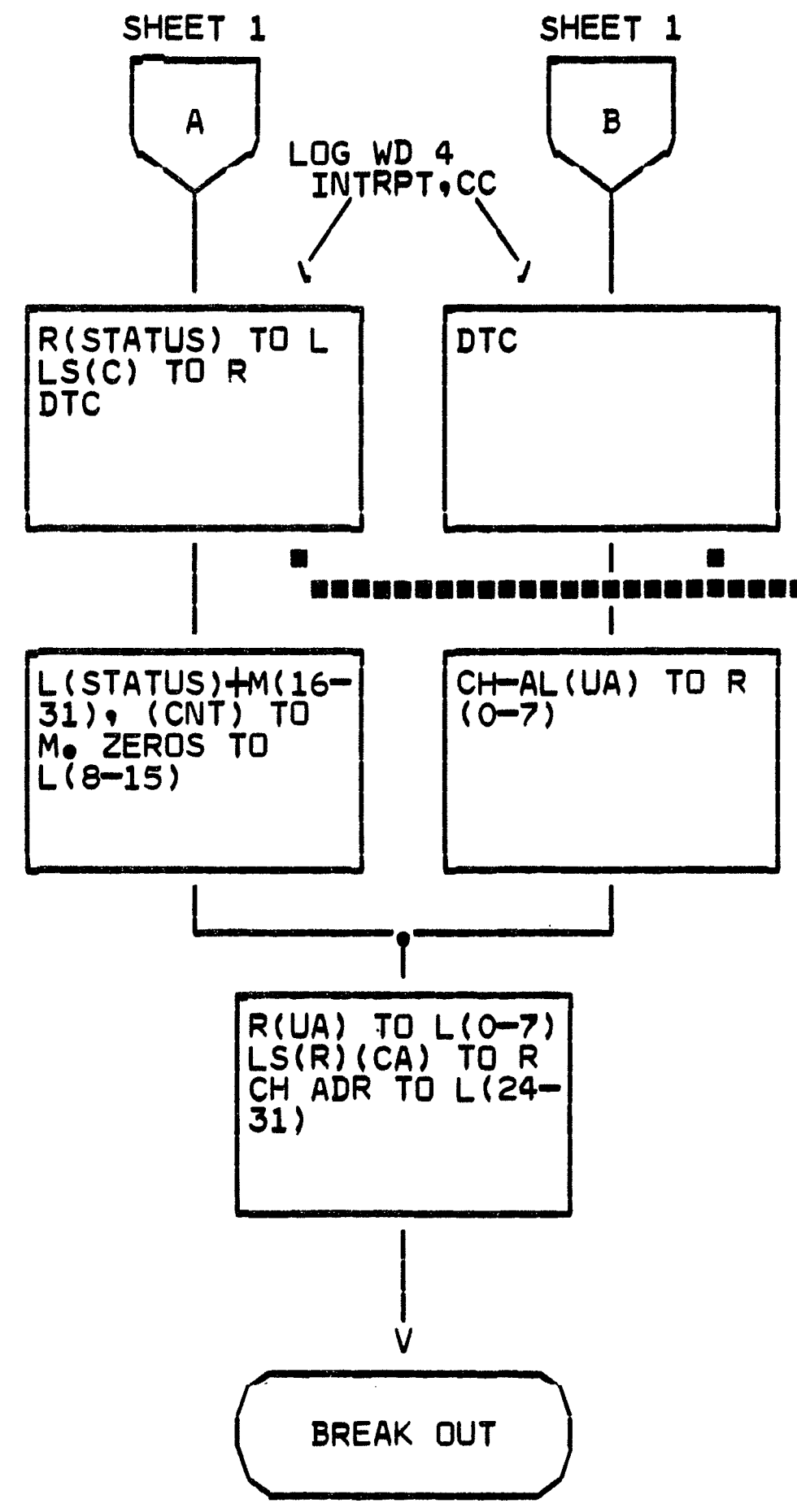


- NOTE 1: CHANNEL HAS CONDITIONED 'WORD UPDATE +1' AND 'WORD UPDATE +2' (GG181)
- NOTE 2: CHANNEL HAS CONDITIONED 'WORD UPDATE +2' (GG181)
- NOTE 3: CHANNEL HAS CONDITIONED 'WORD UPDATE +1' (GG181)
- NOTE 4: INSTRUCTION SCAN LATCH SET, FIRST WORD LATCH SET, AND 'START I-0'.

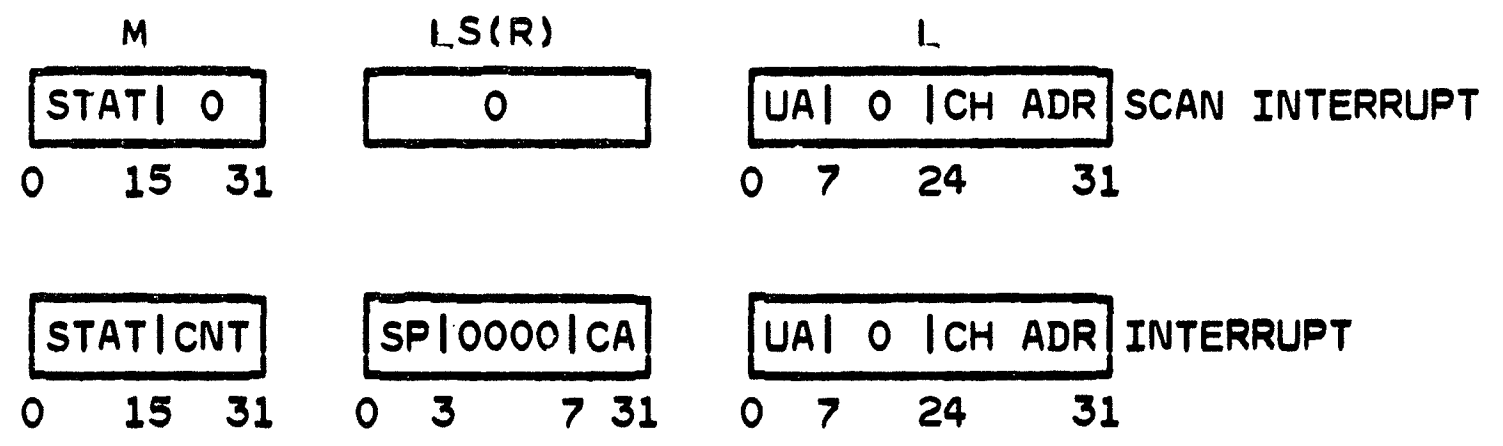
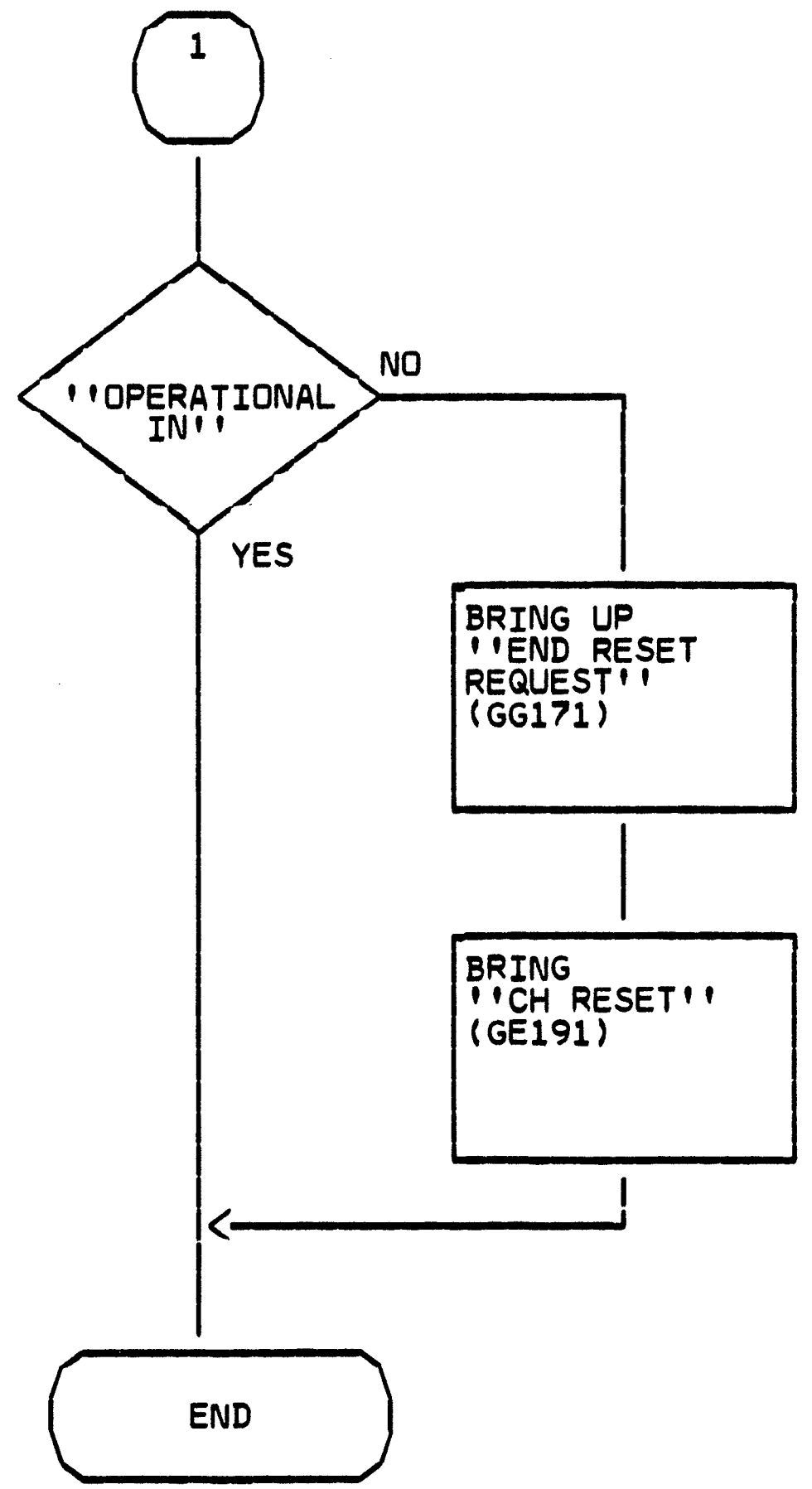
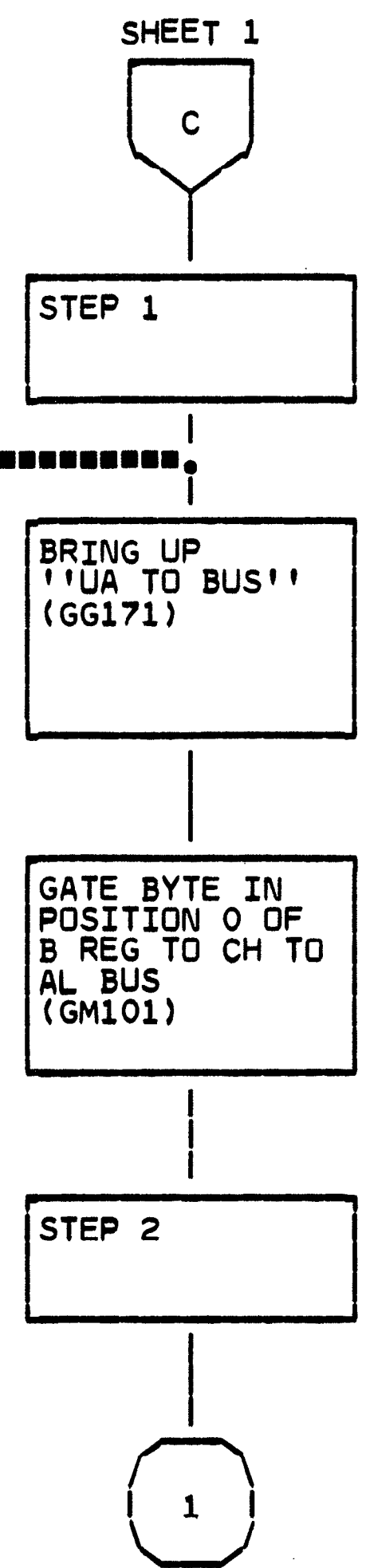
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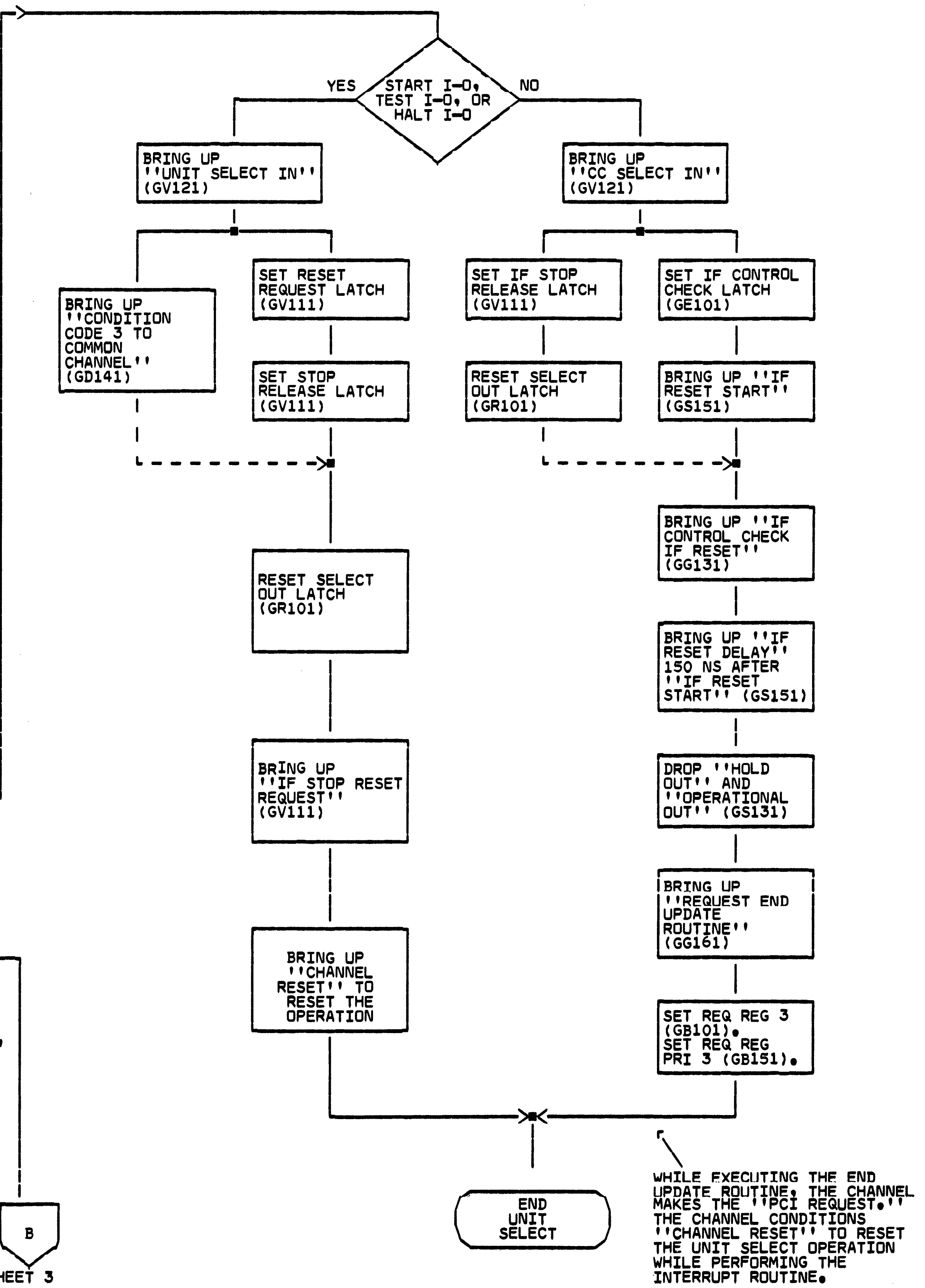
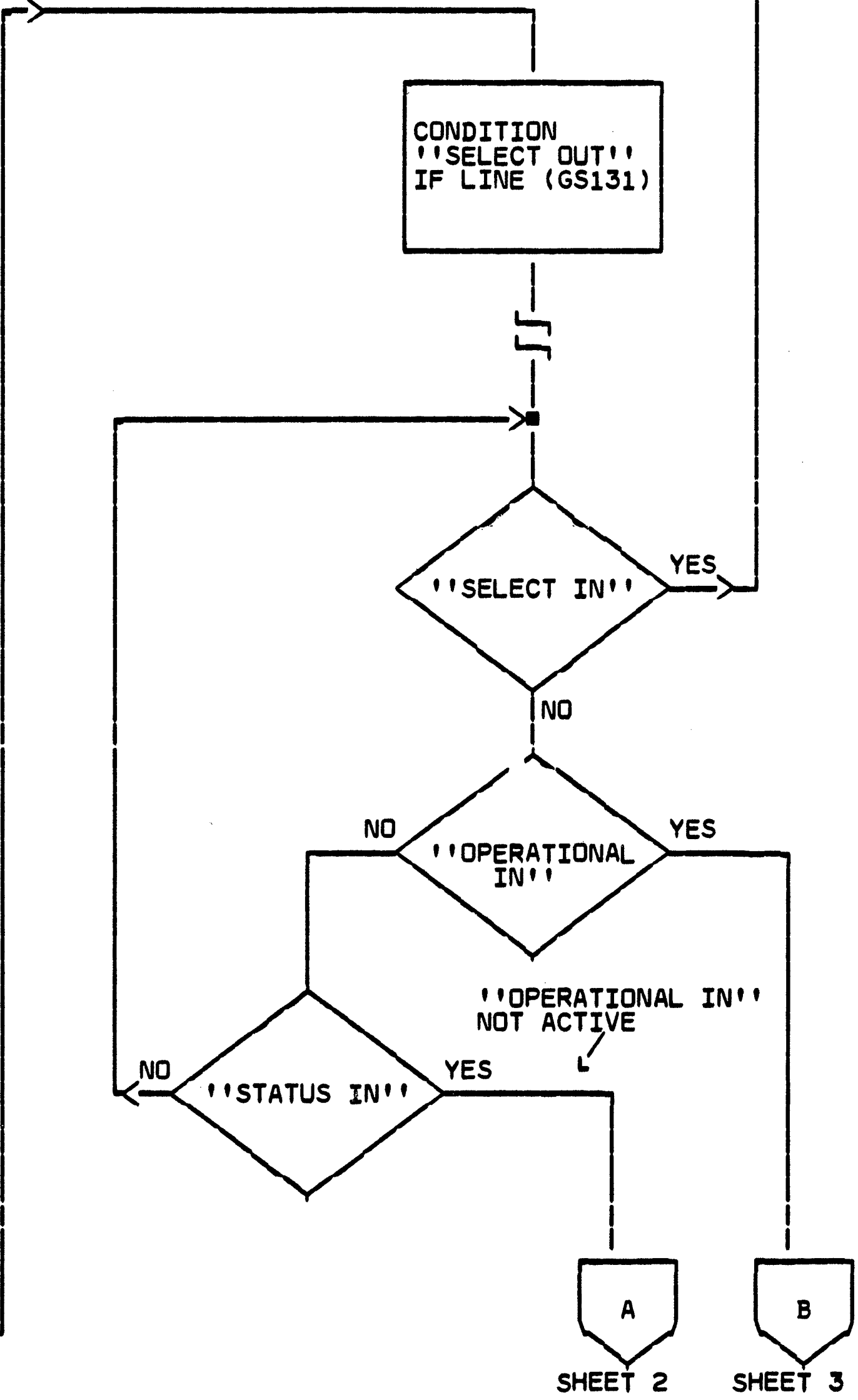
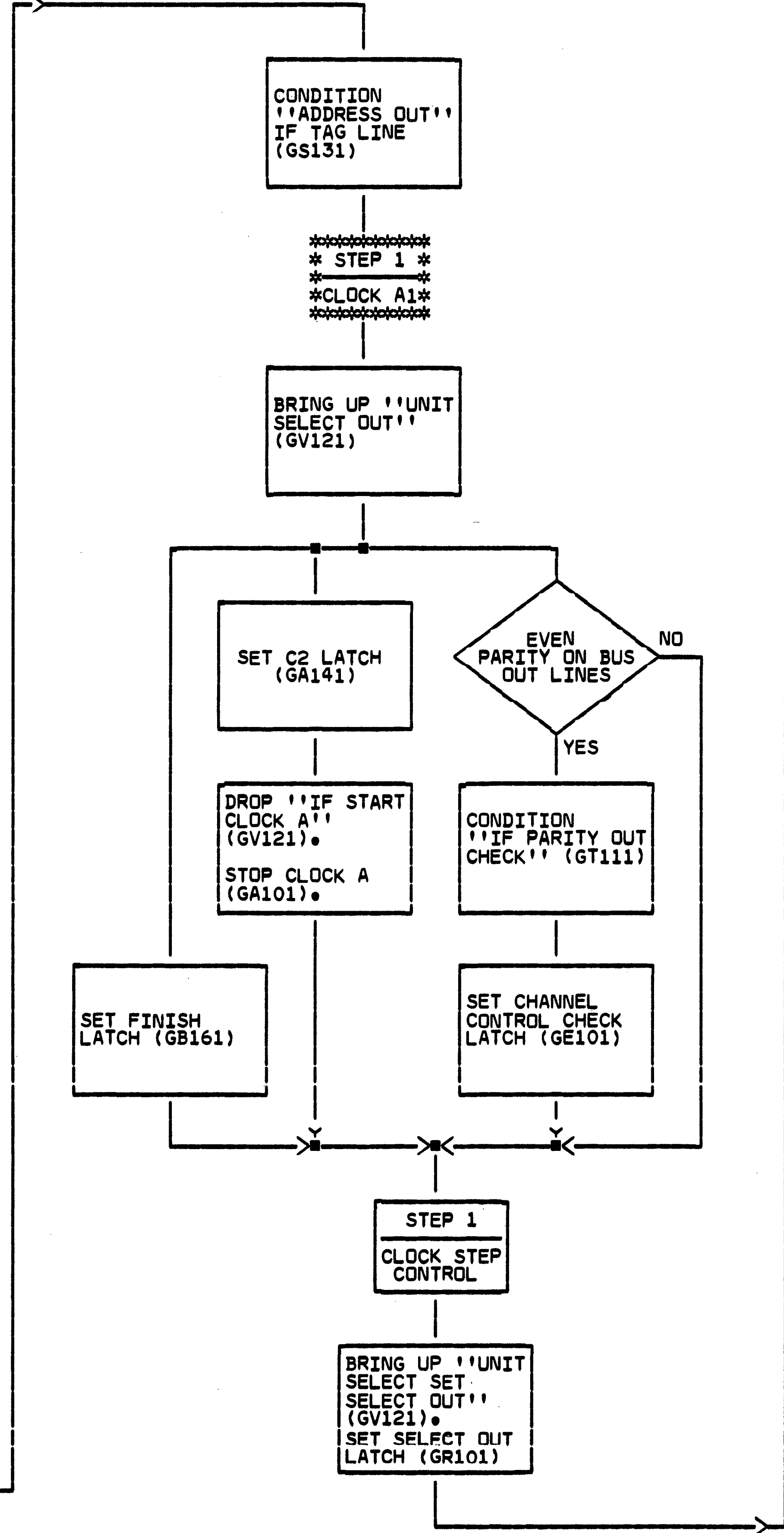
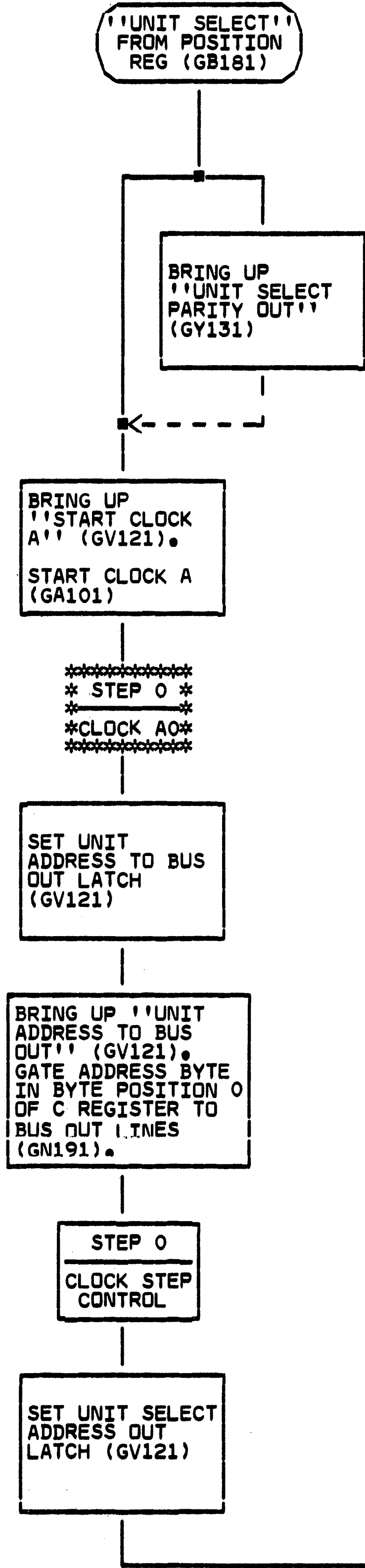


DTC(UA) → CHAN



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NO RDS ROUTINE INVOLVED



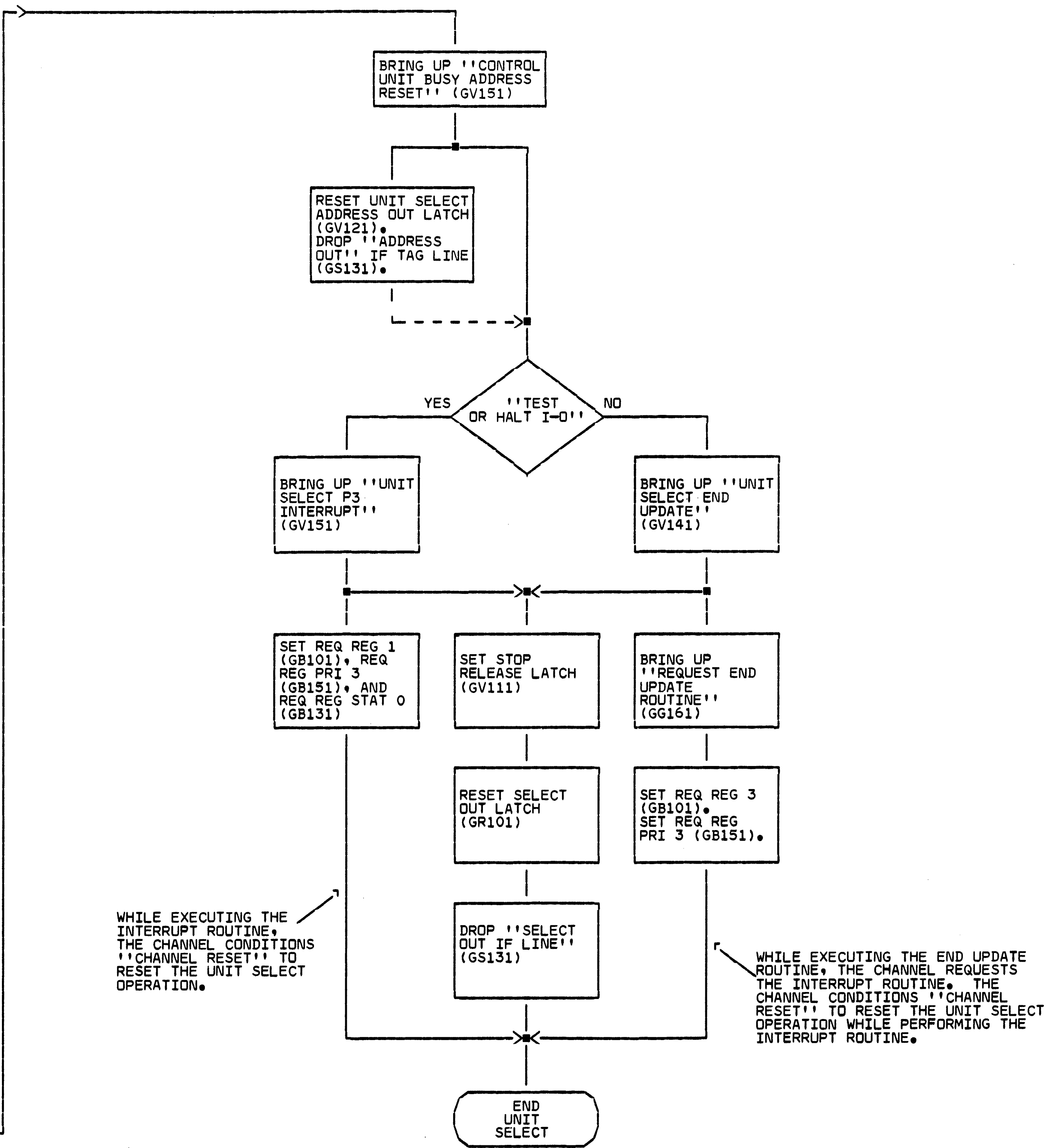
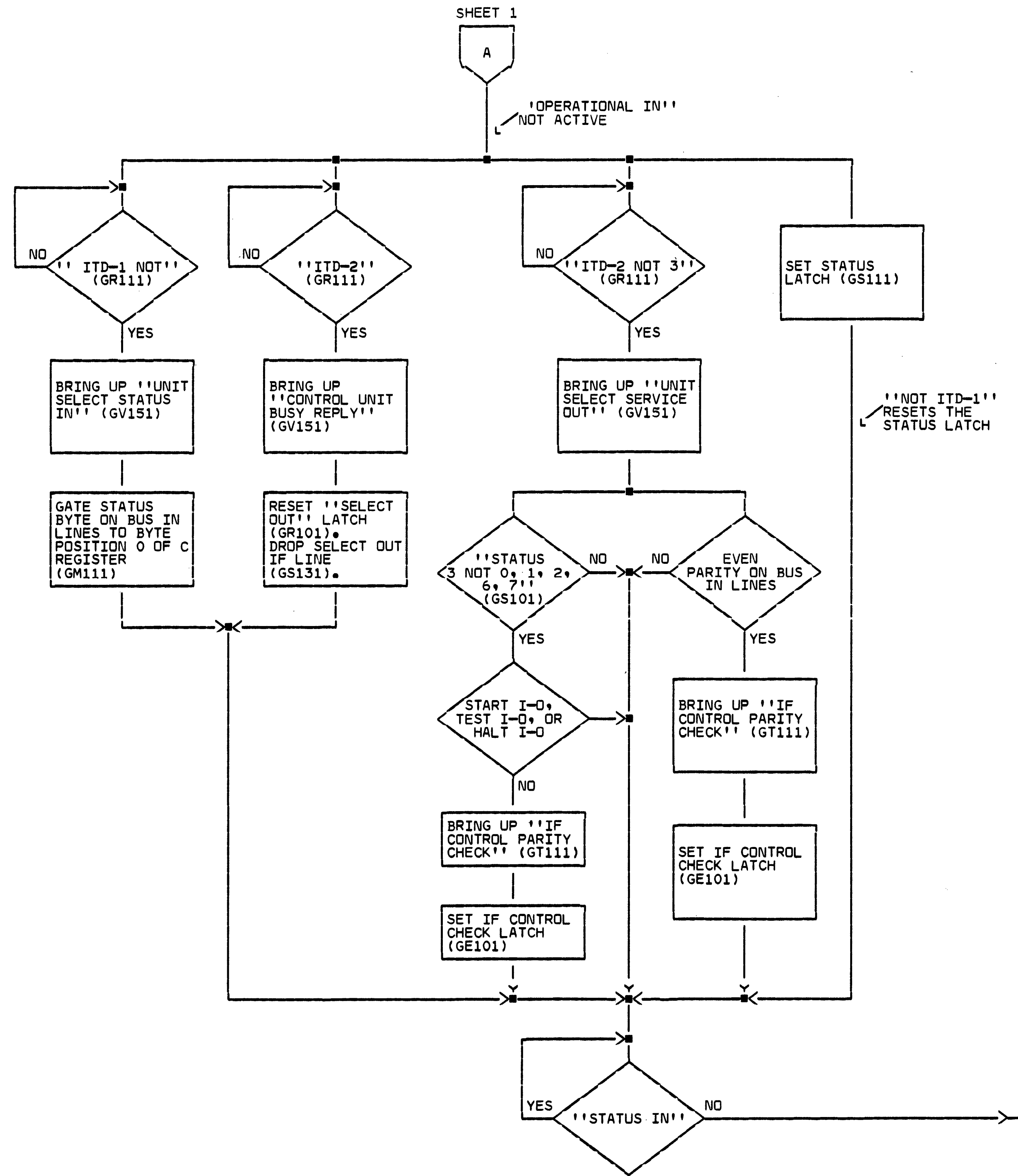
WHILE EXECUTING THE END UPDATE ROUTINE, THE CHANNEL MAKES THE "PCI REQUEST". THE CHANNEL CONDITIONS "CHANNEL RESET" TO RESET THE UNIT SELECT OPERATION WHILE PERFORMING THE INTERRUPT ROUTINE.

SHEET 2 SHEET 3

UNIT SELECT (SELECTOR CHANNEL)  
 DATE 27 JUN 66 MACH. 2050  
 FRAME  
 P.N.  
 IBM CORP. SDD PAGE 2

S4010

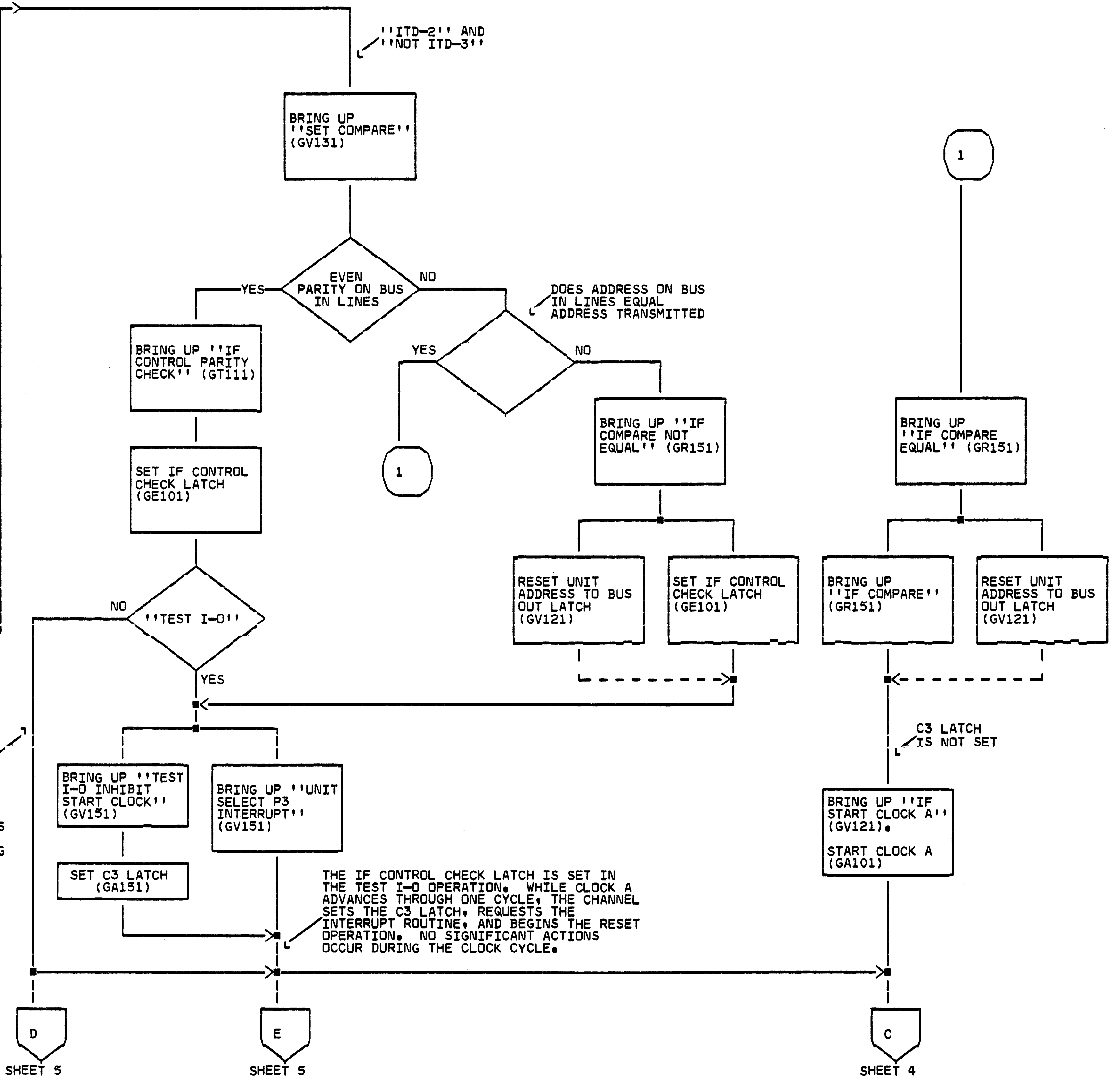
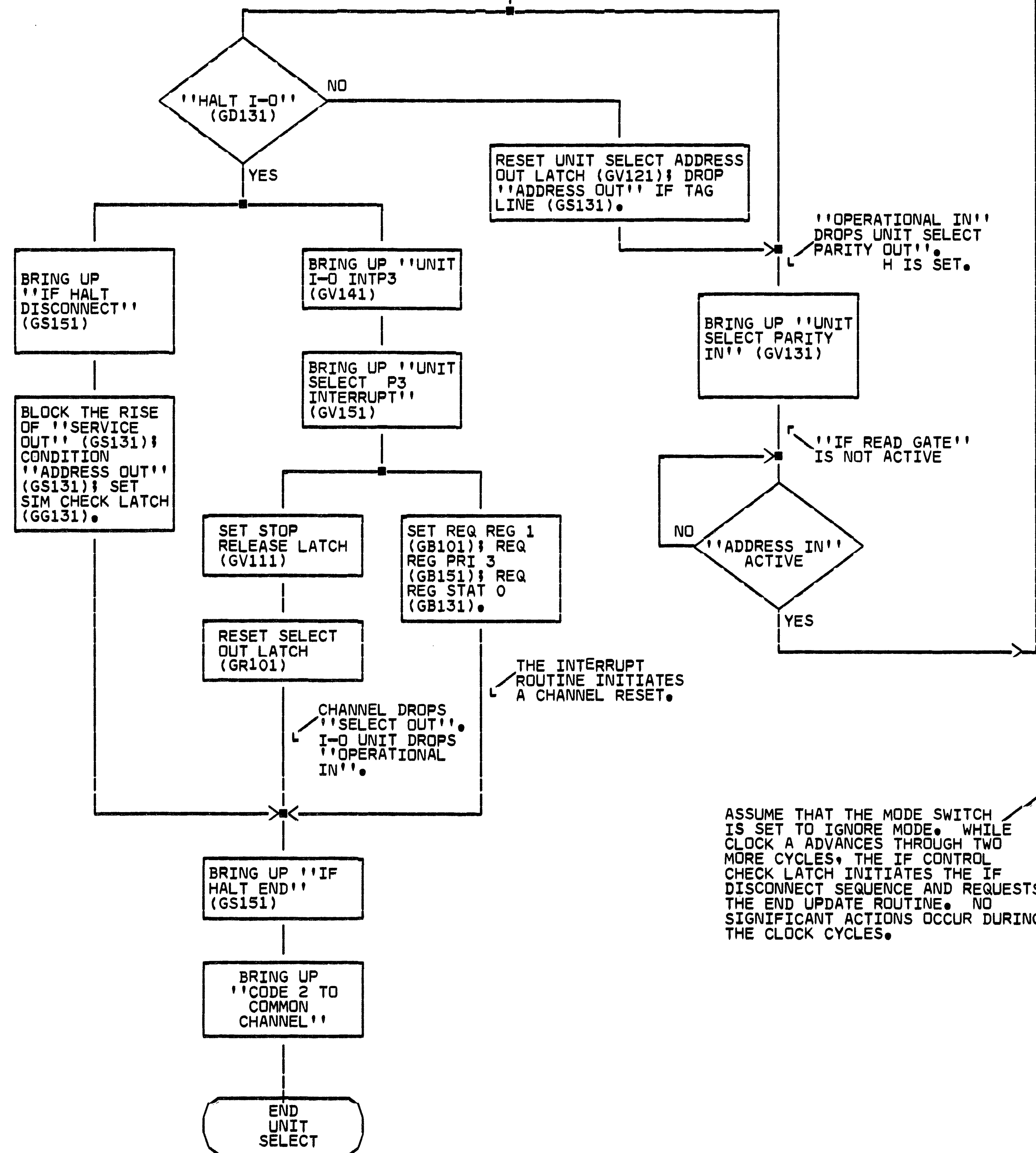




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SHEET 1

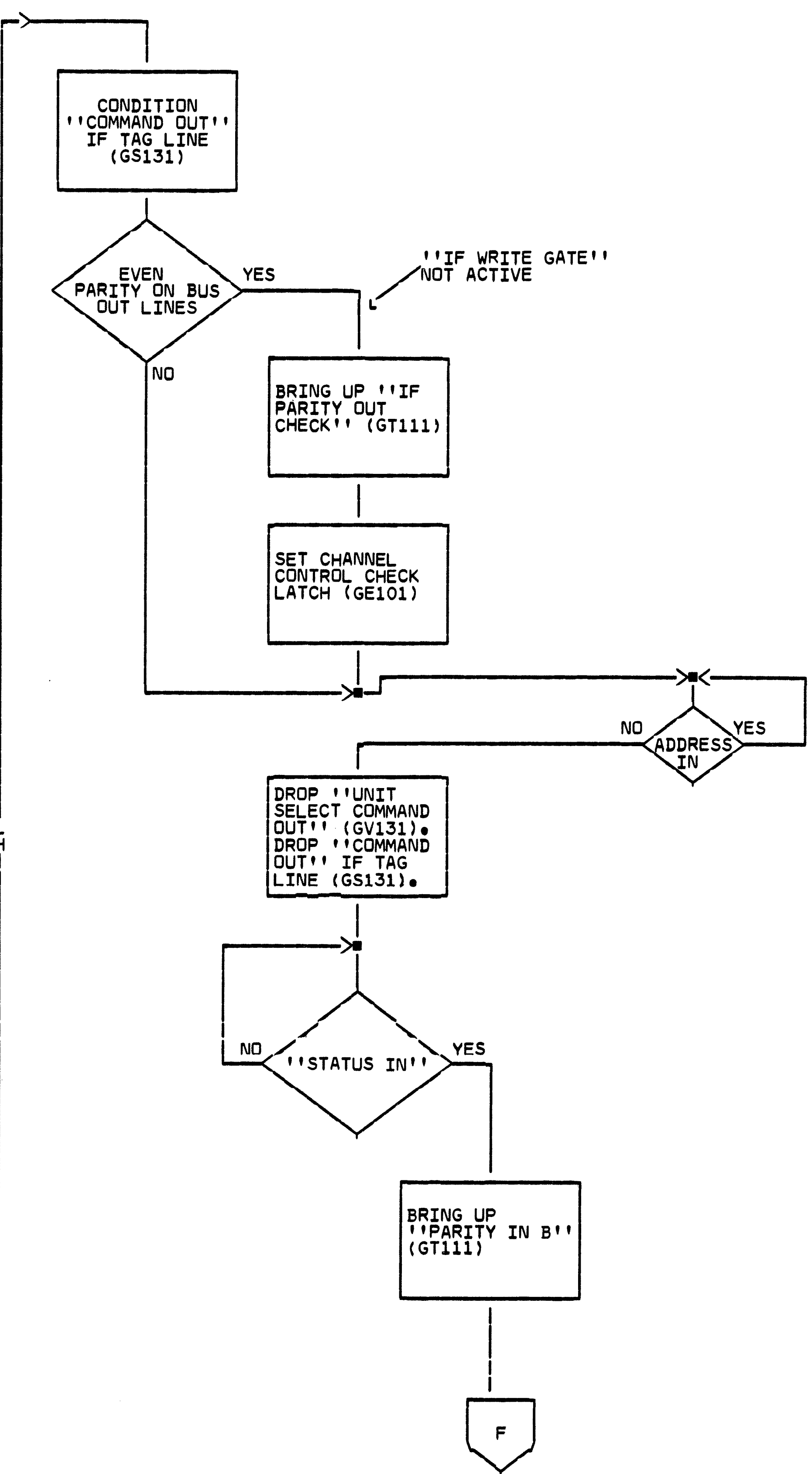
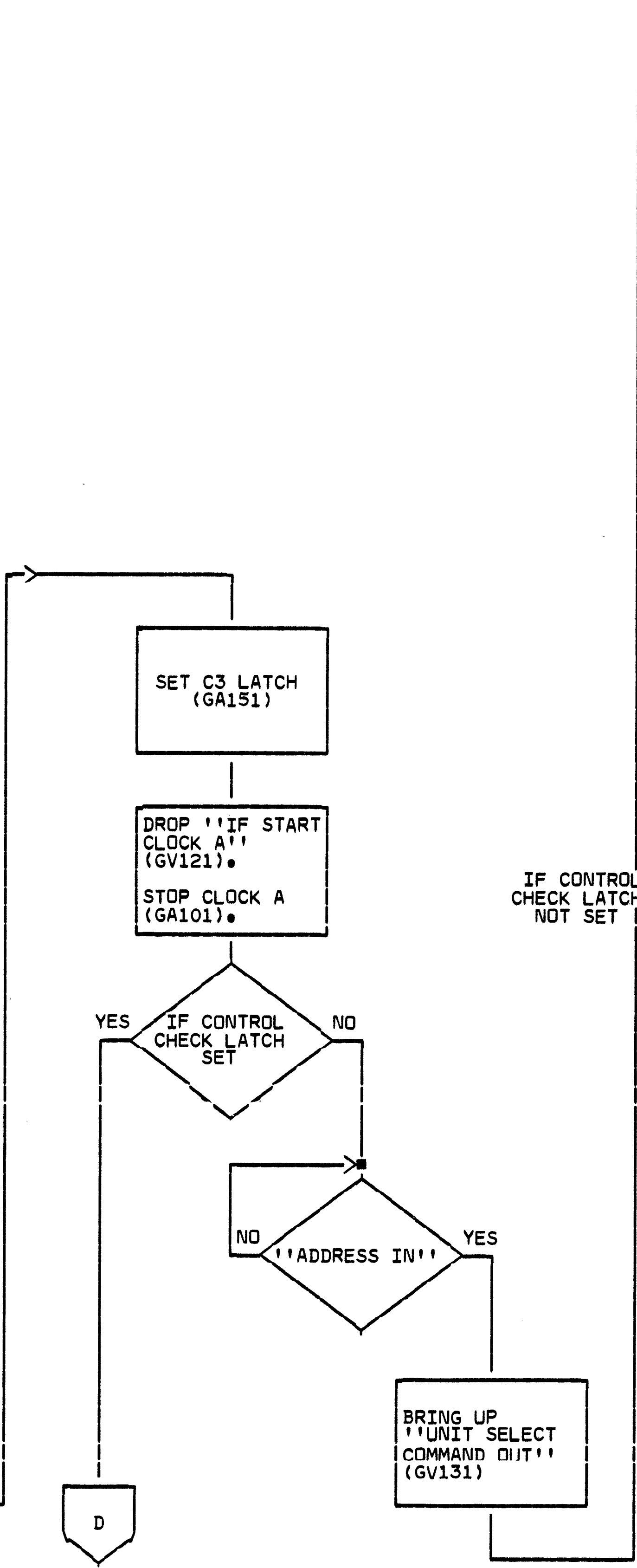
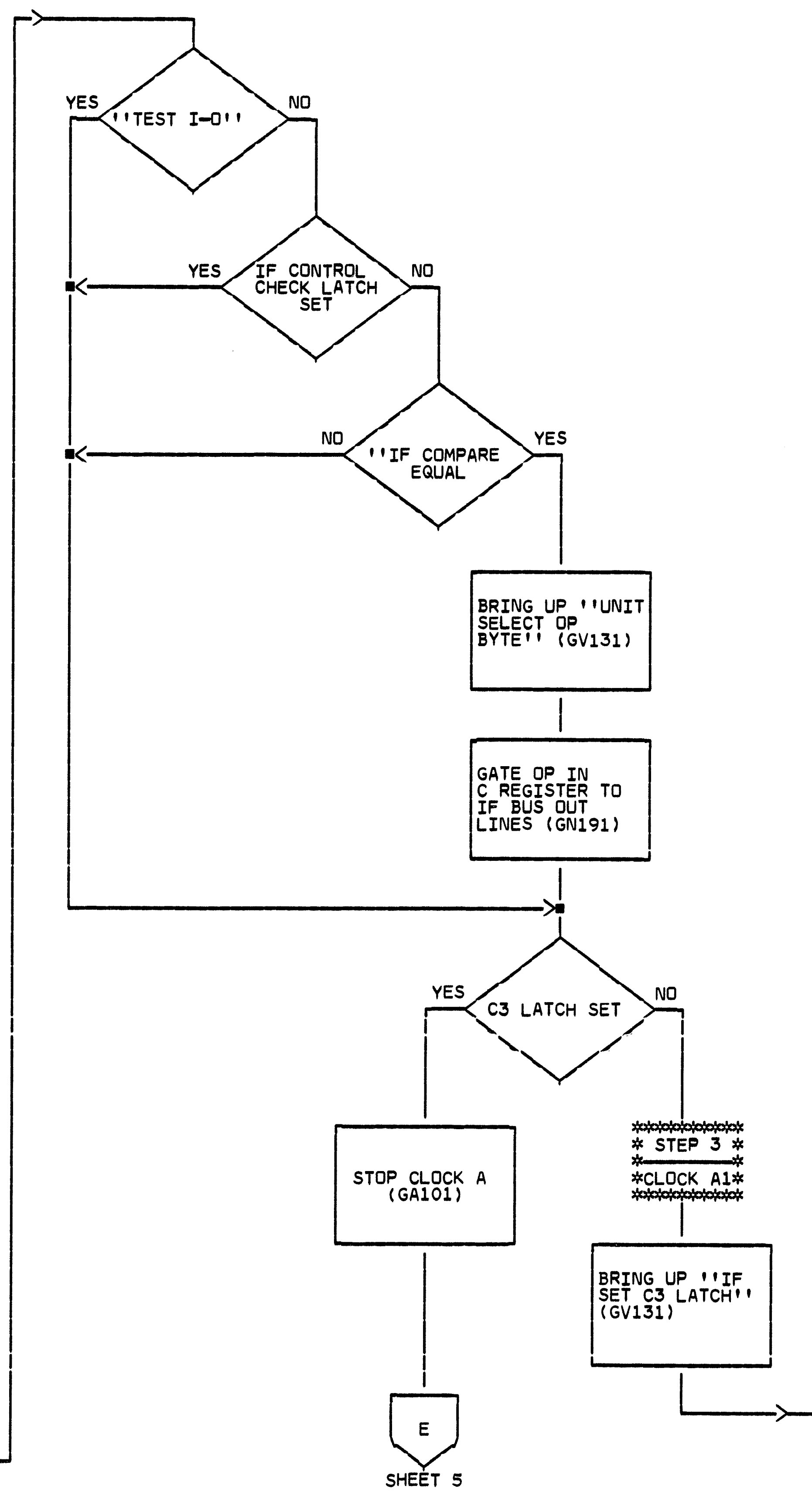
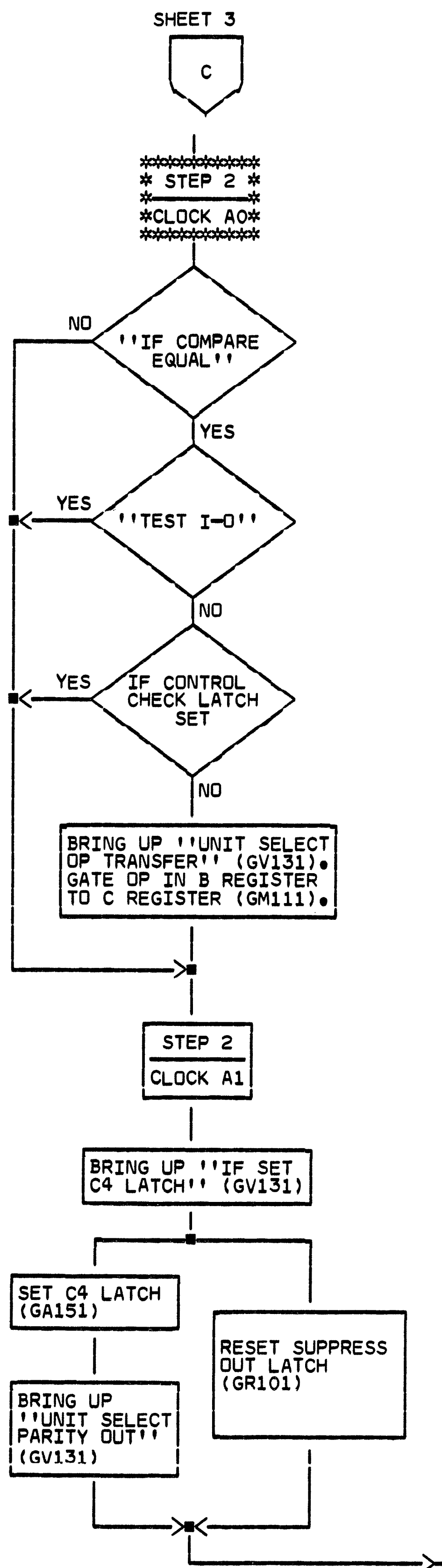
B



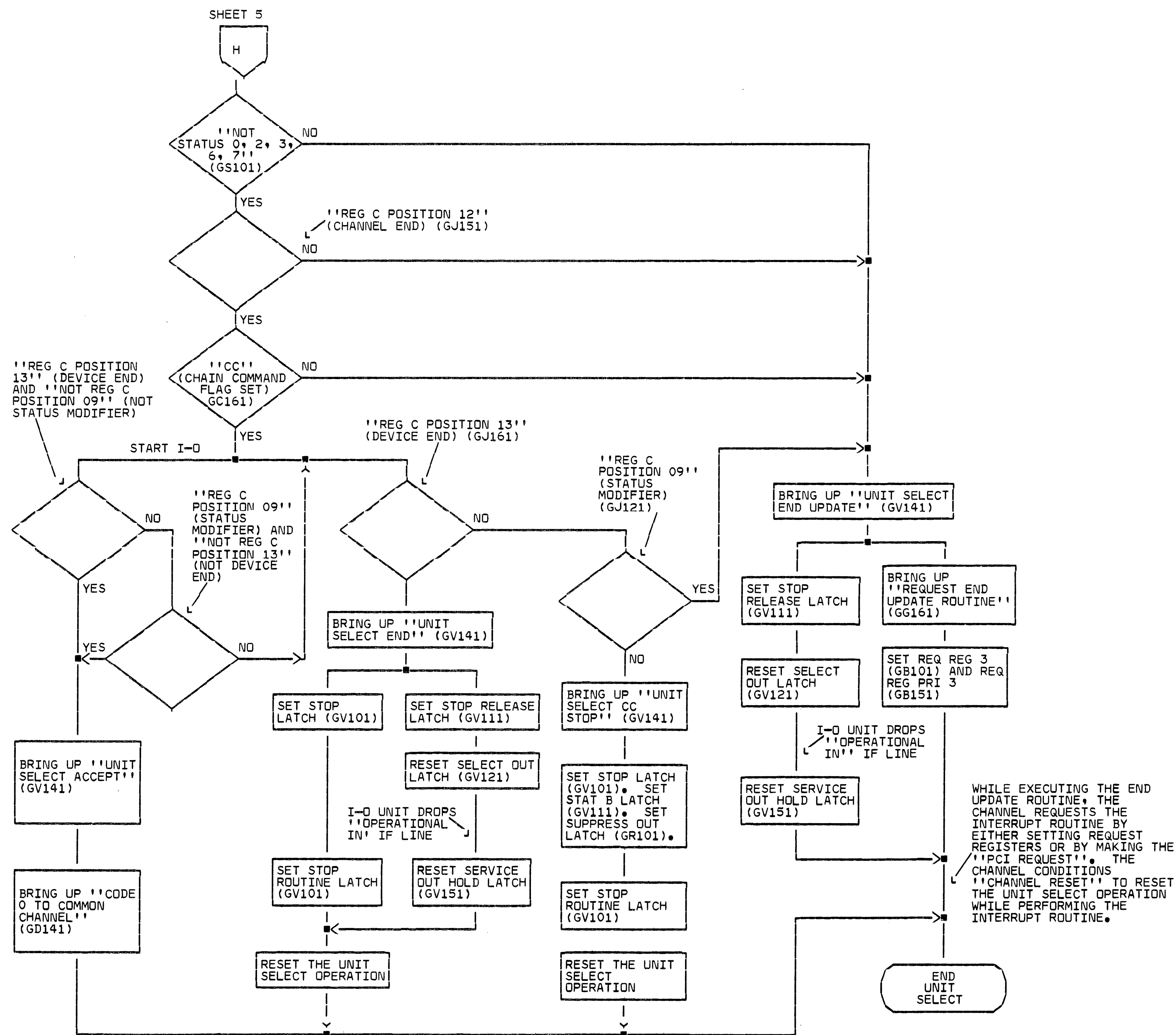
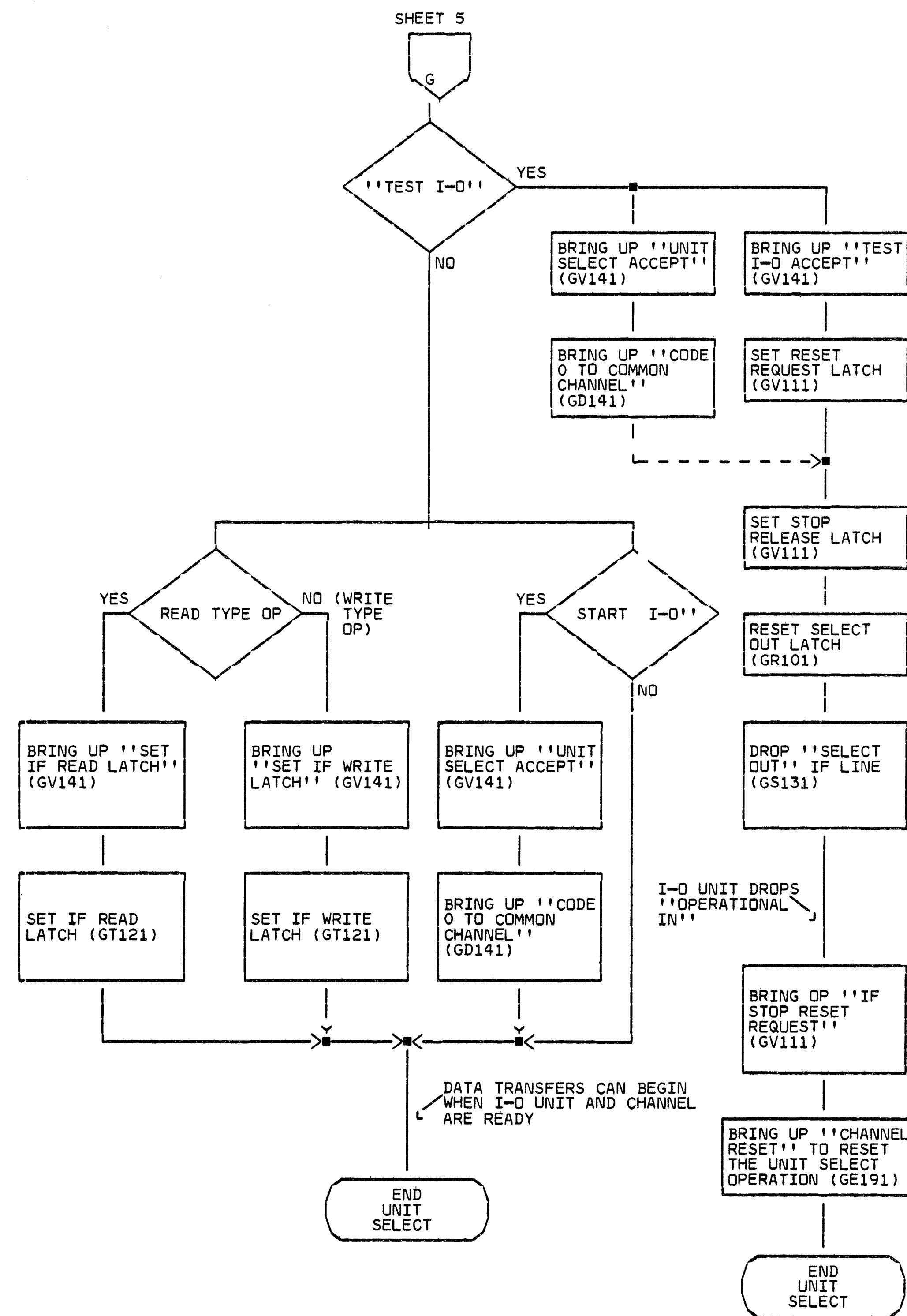
ASSUME THAT THE MODE SWITCH IS SET TO IGNORE MODE. WHILE CLOCK A ADVANCES THROUGH TWO MORE CYCLES, THE IF CONTROL CHECK LATCH INITIATES THE IF DISCONNECT SEQUENCE AND REQUESTS THE END UPDATE ROUTINE. NO SIGNIFICANT ACTIONS OCCUR DURING THE CLOCK CYCLES.

THE IF CONTROL CHECK LATCH IS SET IN THE TEST I-0 OPERATION. WHILE CLOCK A ADVANCES THROUGH ONE CYCLE, THE CHANNEL SETS THE C3 LATCH, REQUESTS THE INTERRUPT ROUTINE, AND BEGINS THE RESET OPERATION. NO SIGNIFICANT ACTIONS OCCUR DURING THE CLOCK CYCLE.

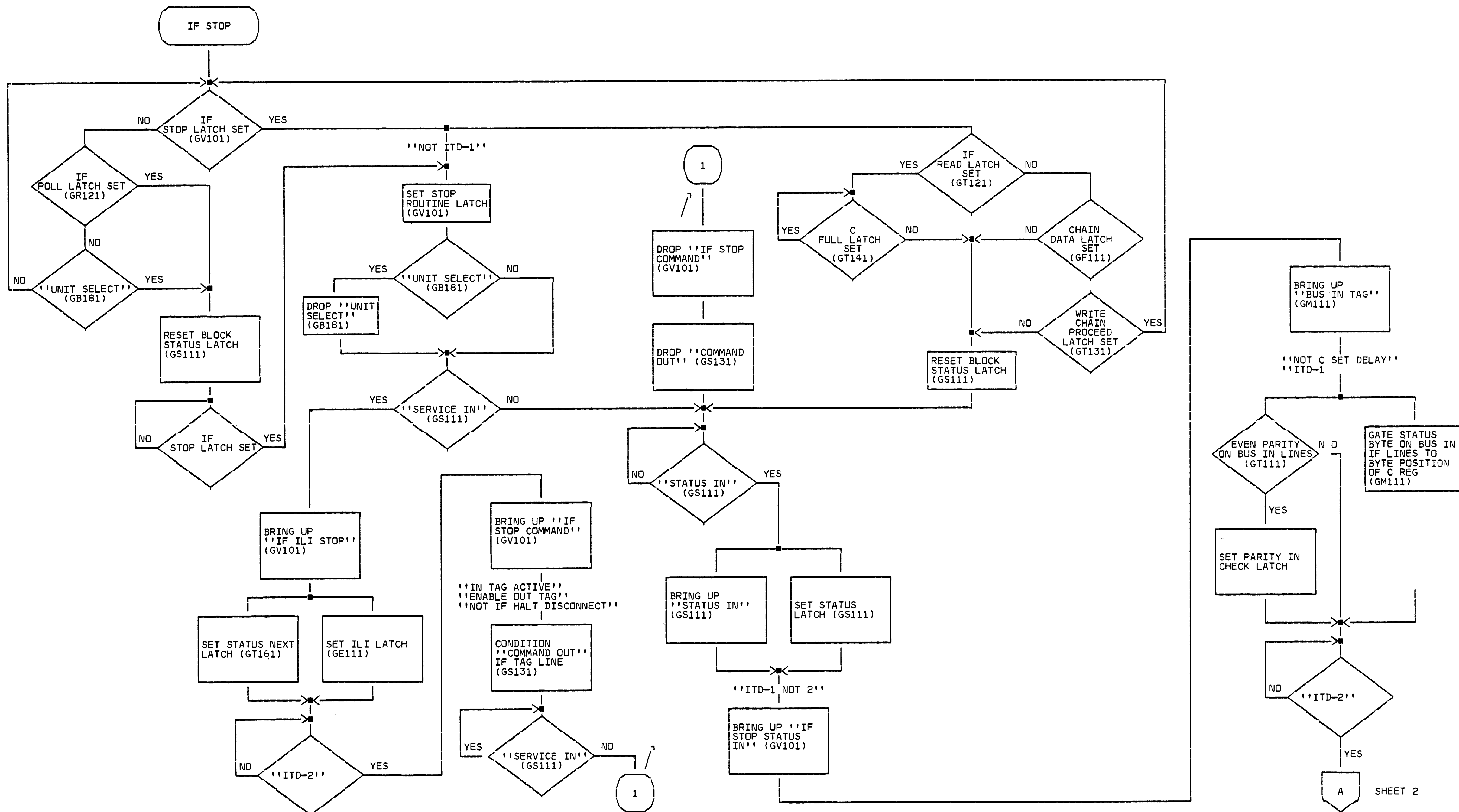
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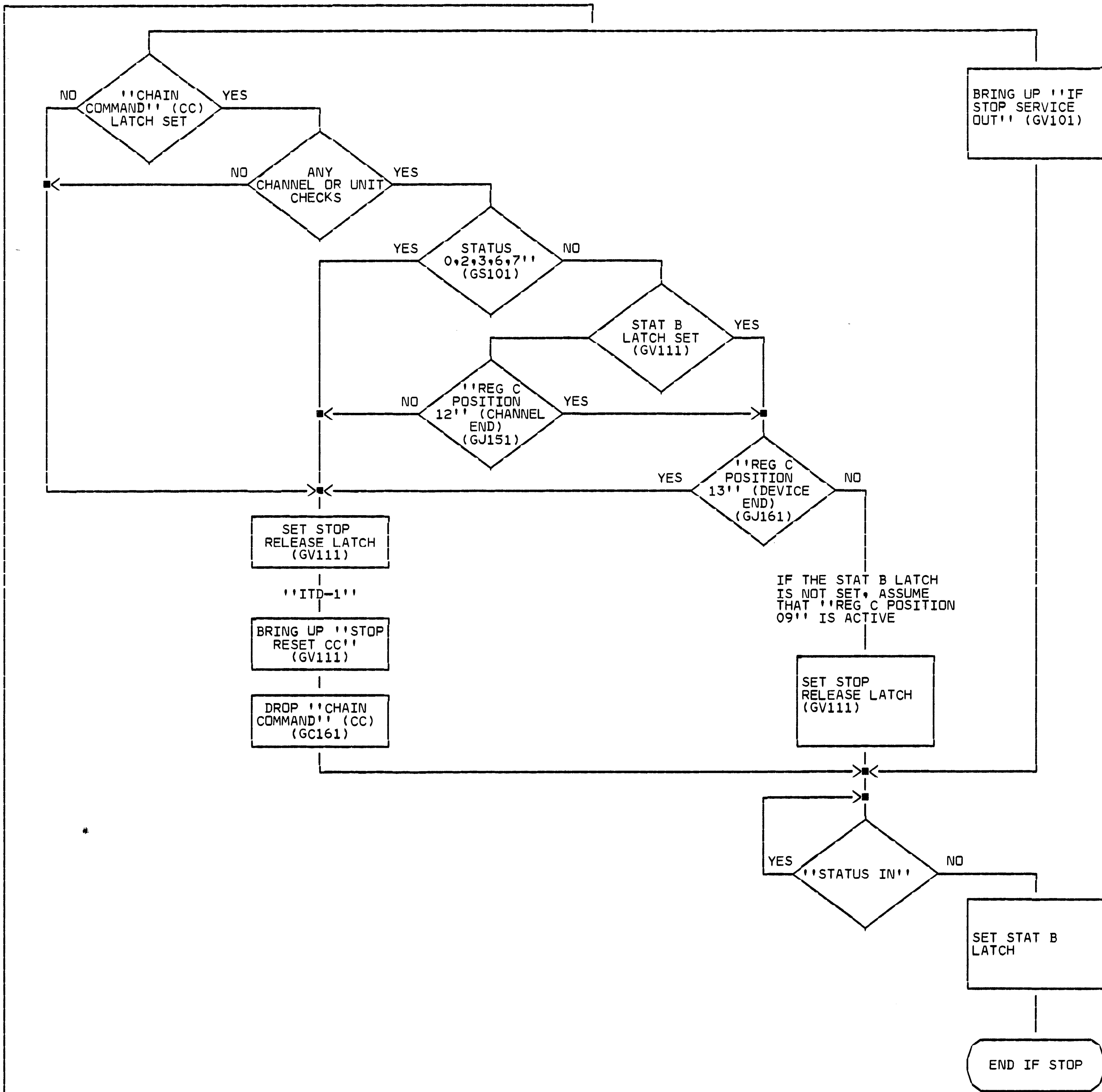
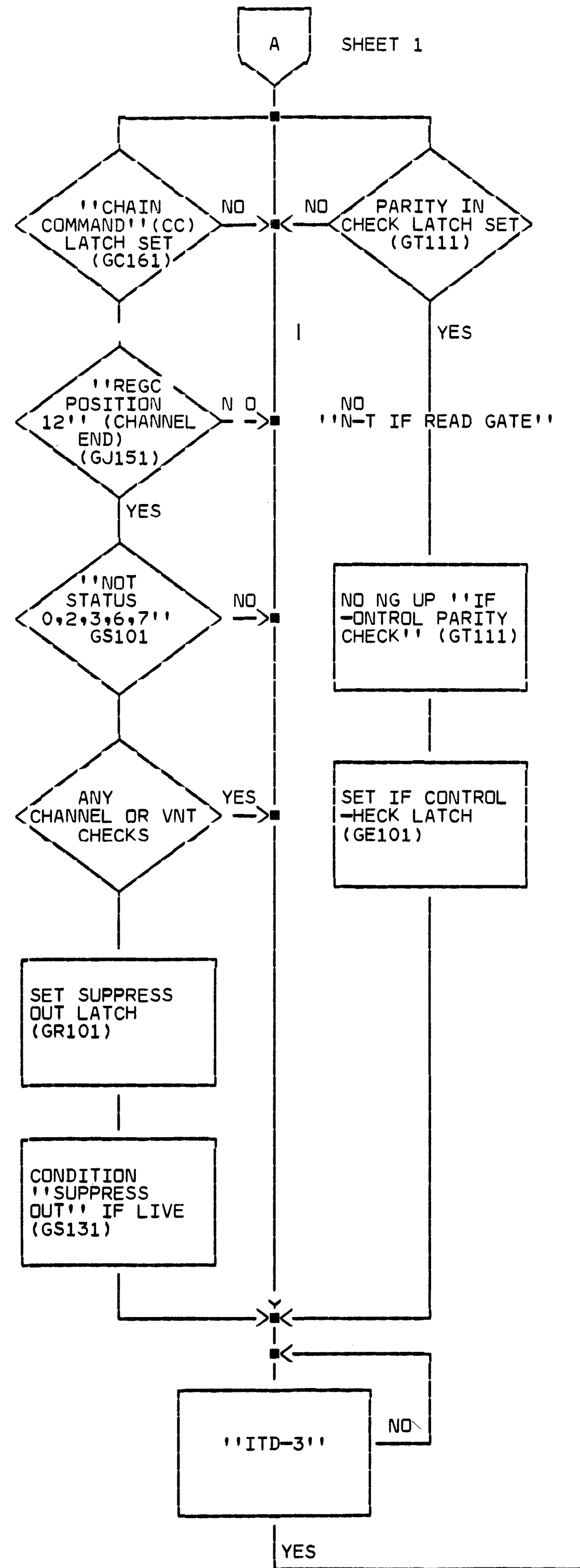
4010 UNIT SELECT  
(SELECTOR CHANNEL)  
DATE 16 JUL 65 MACH. 2050  
FRAME  
P.N.  
IBM CORP. SDD PAGE 6



4011 IF STOP  
 (SELECTOR CHANNEL)  
 DATE 16 JUL 65 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE 1

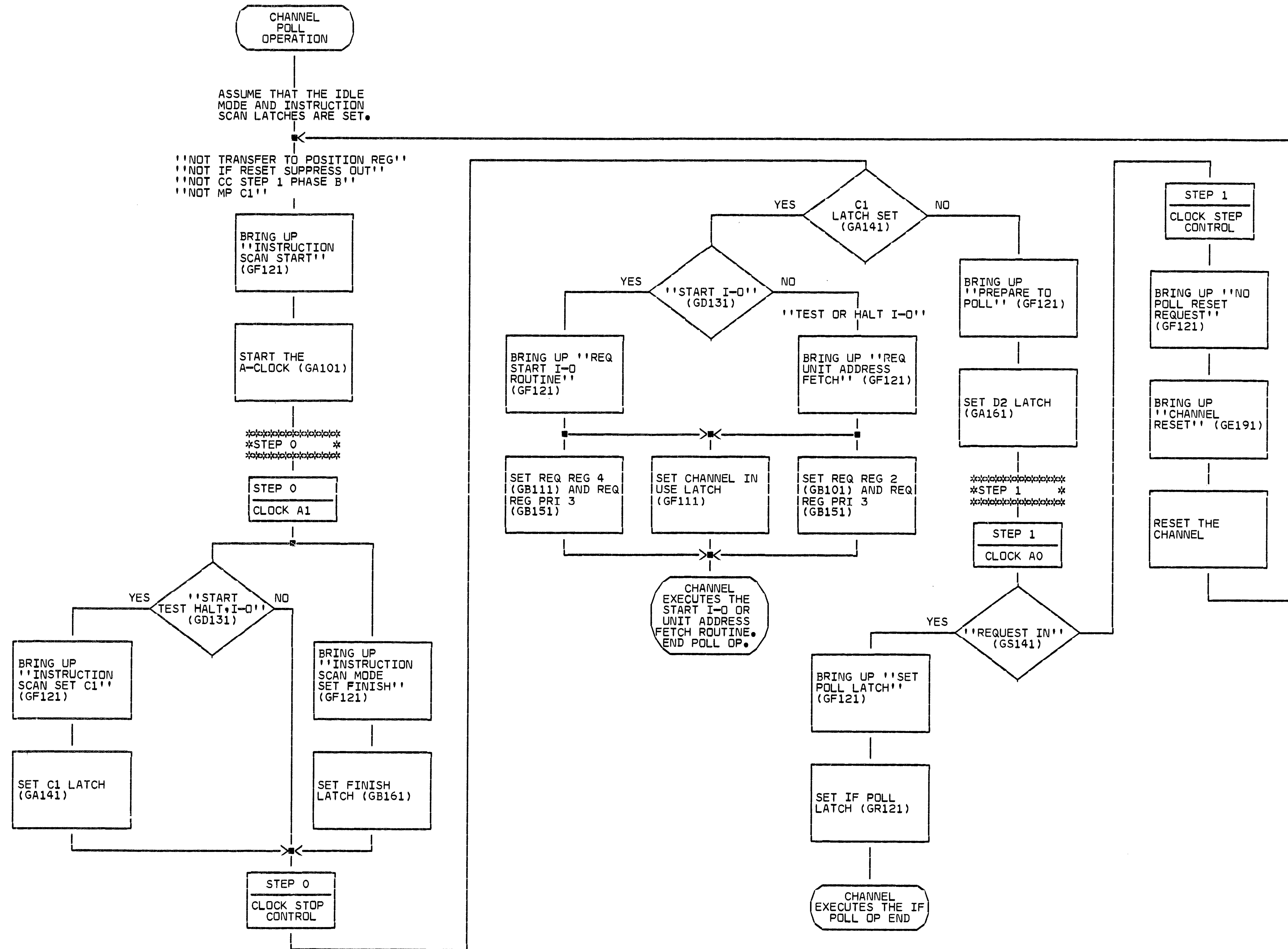
IBM CONFIDENTIAL

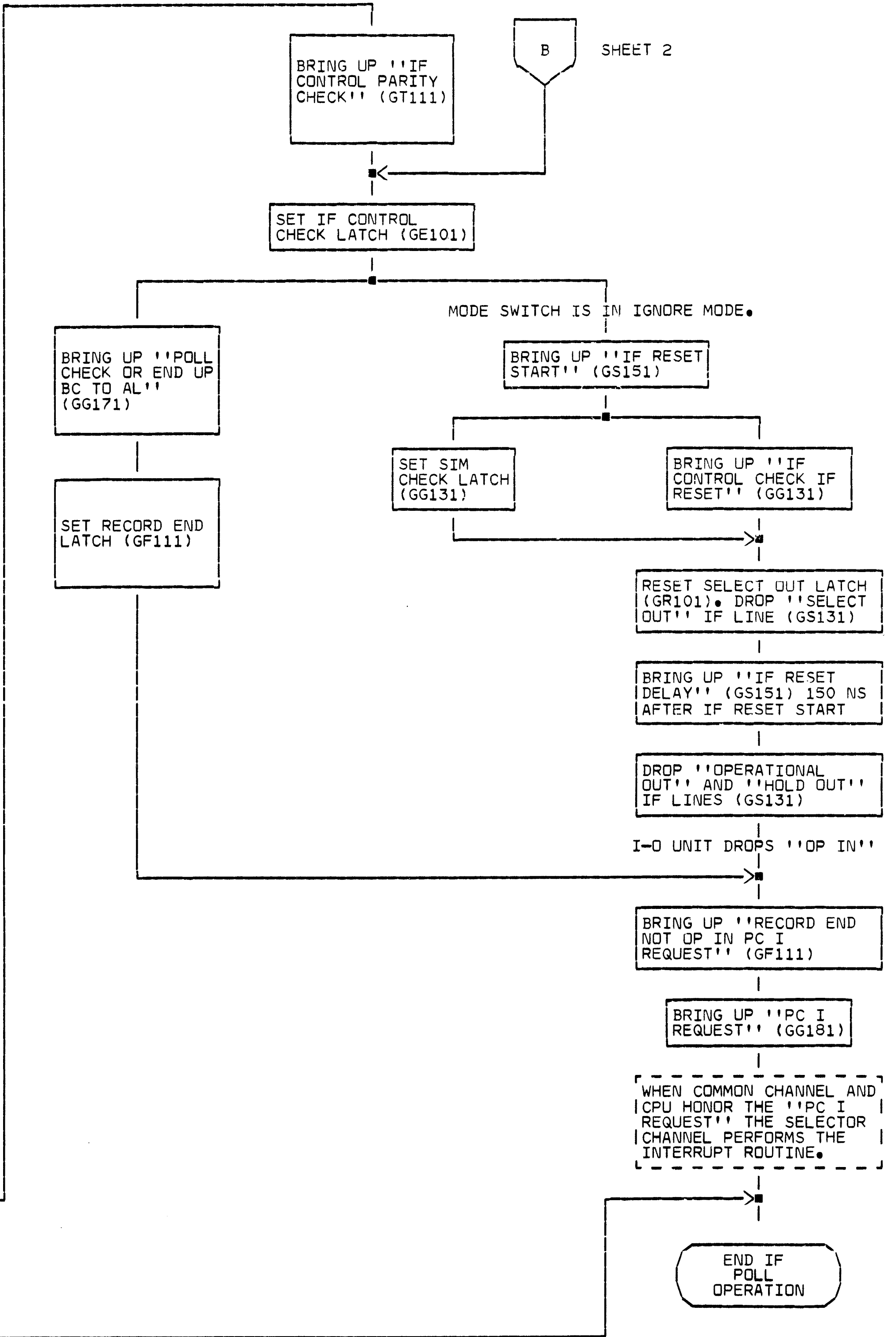
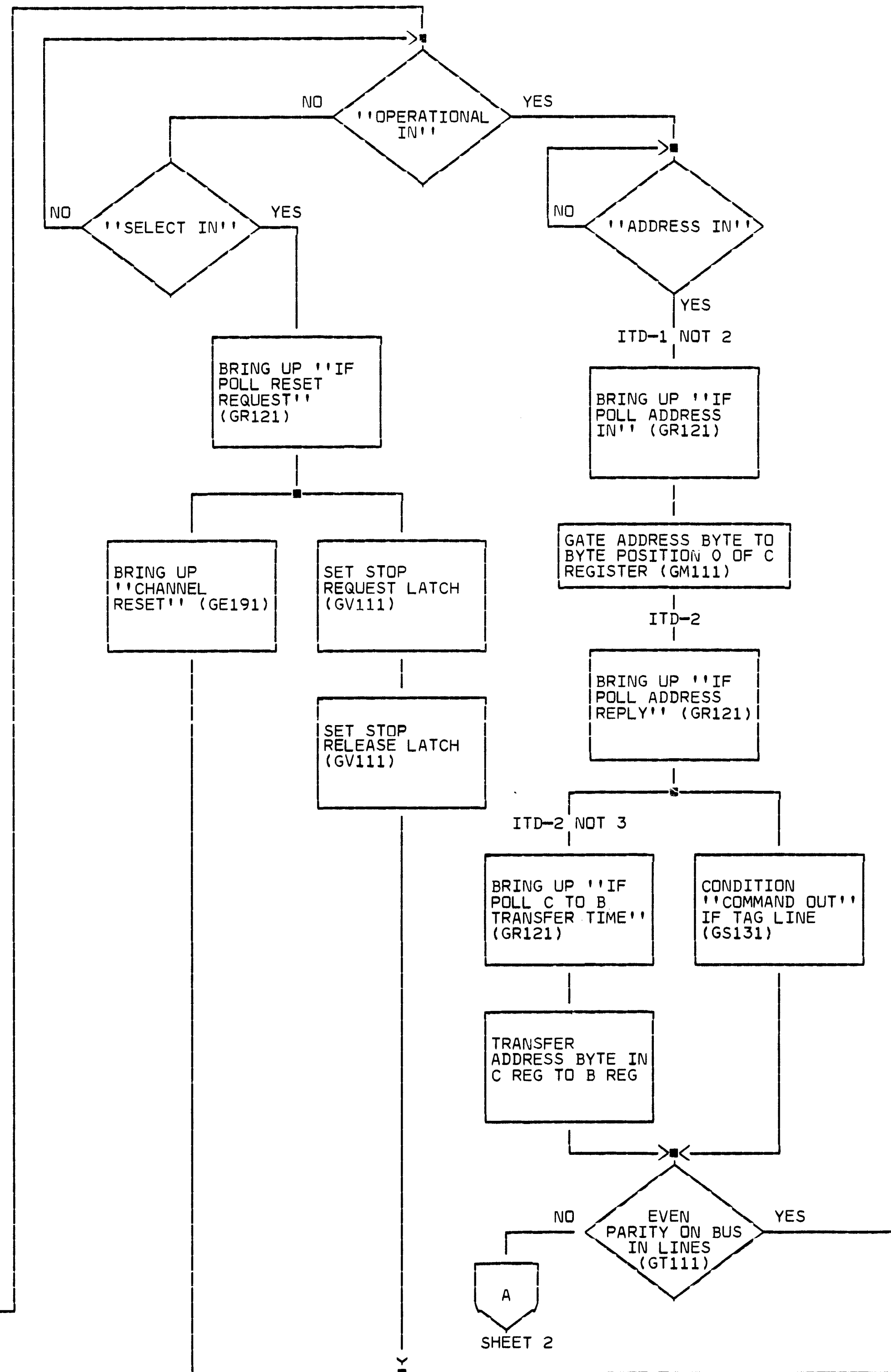
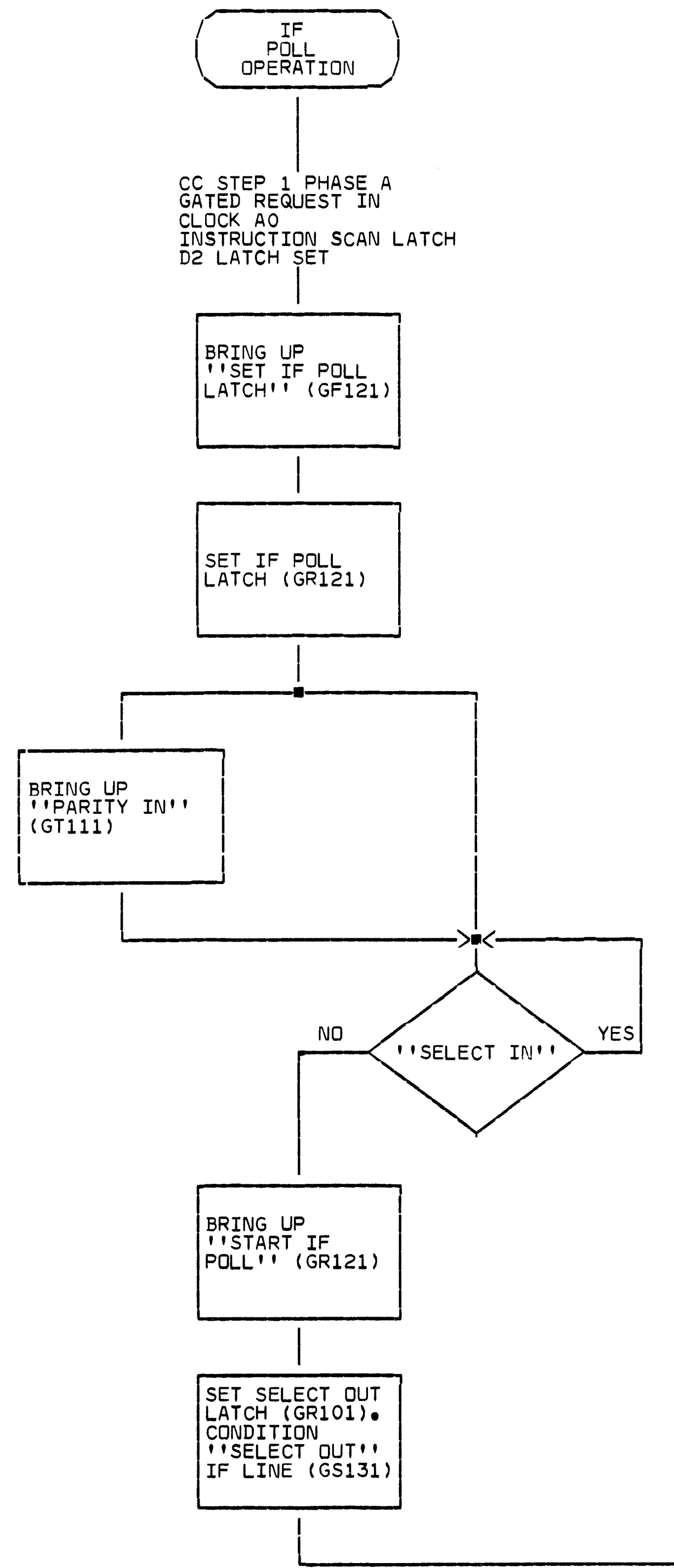
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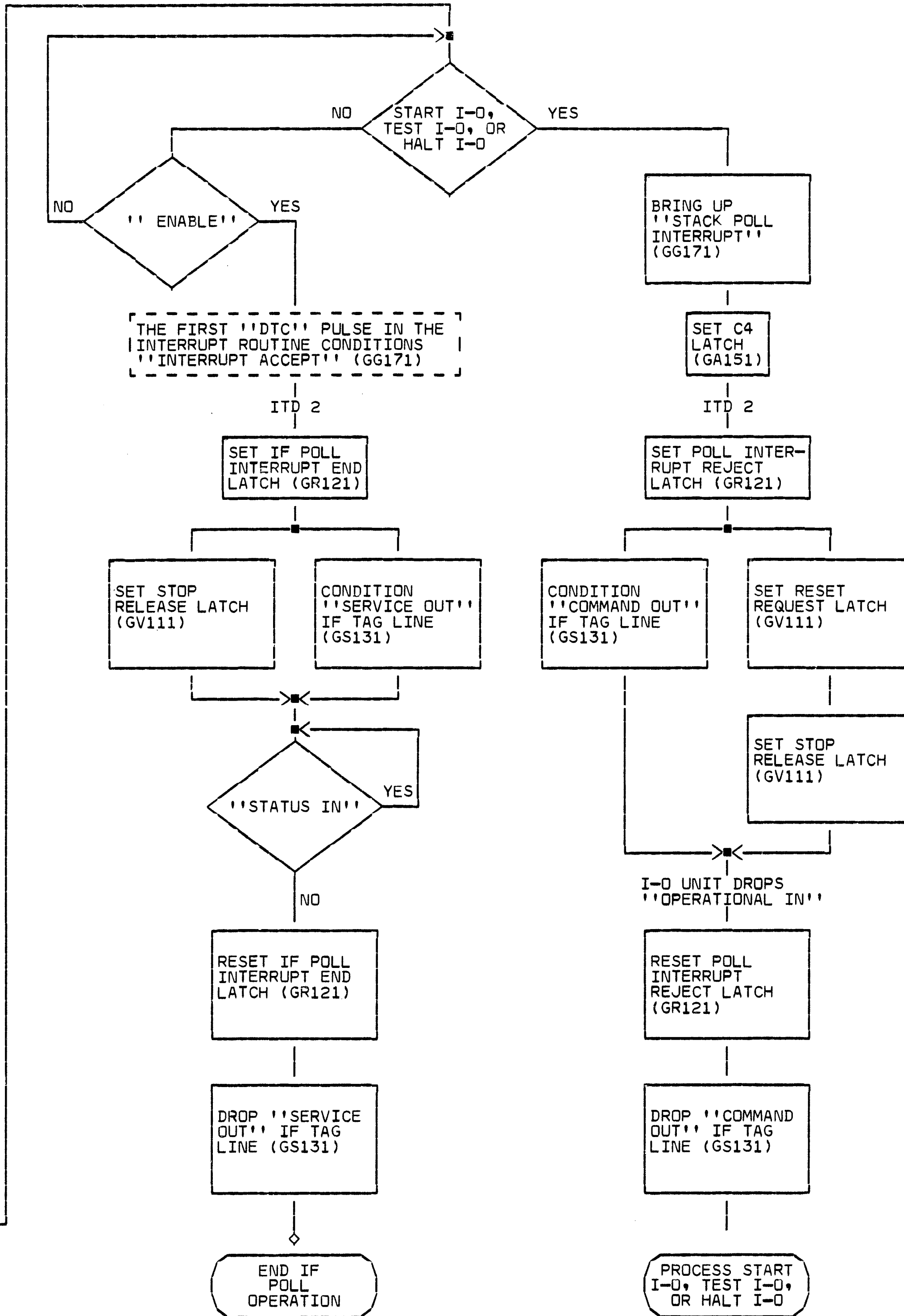
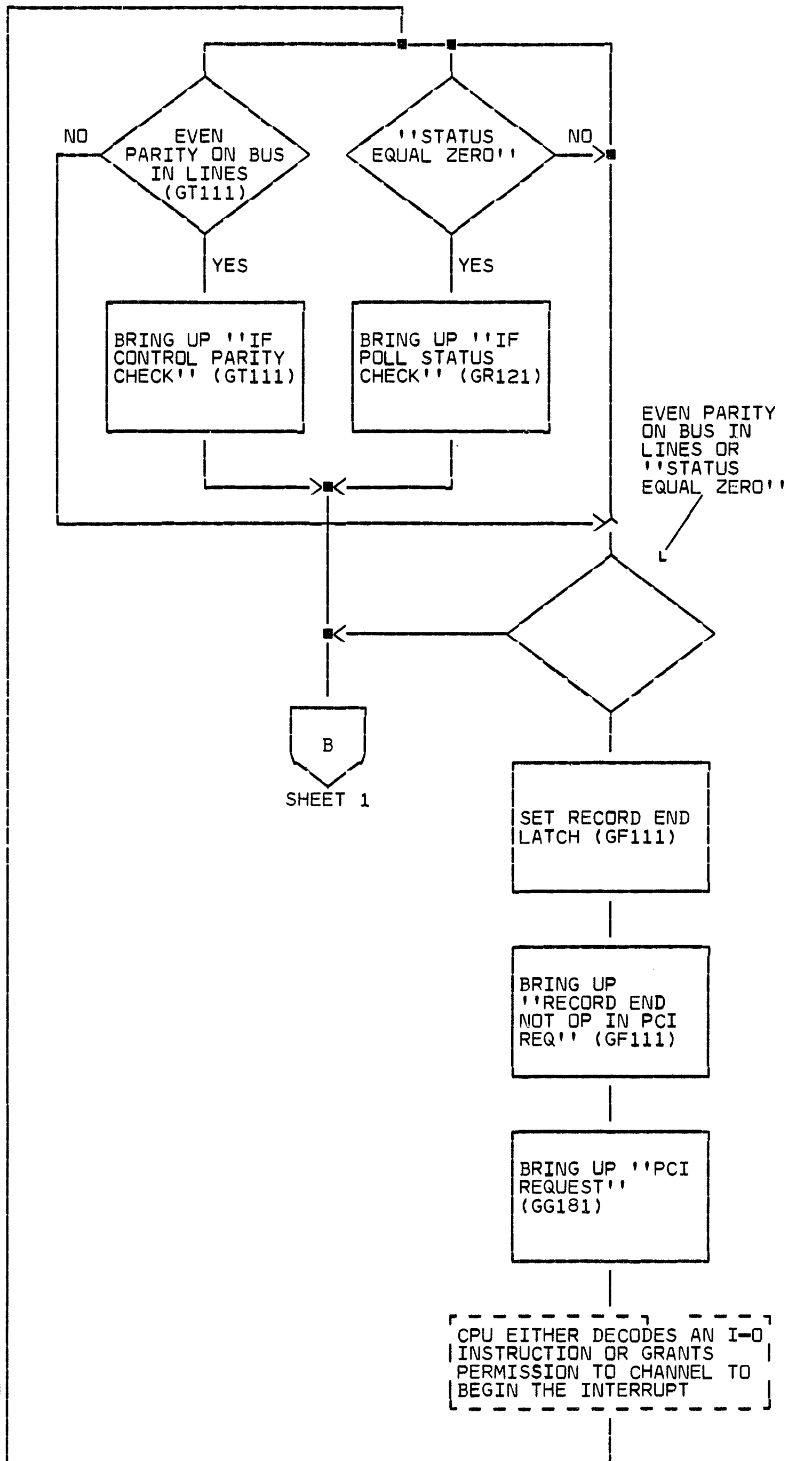
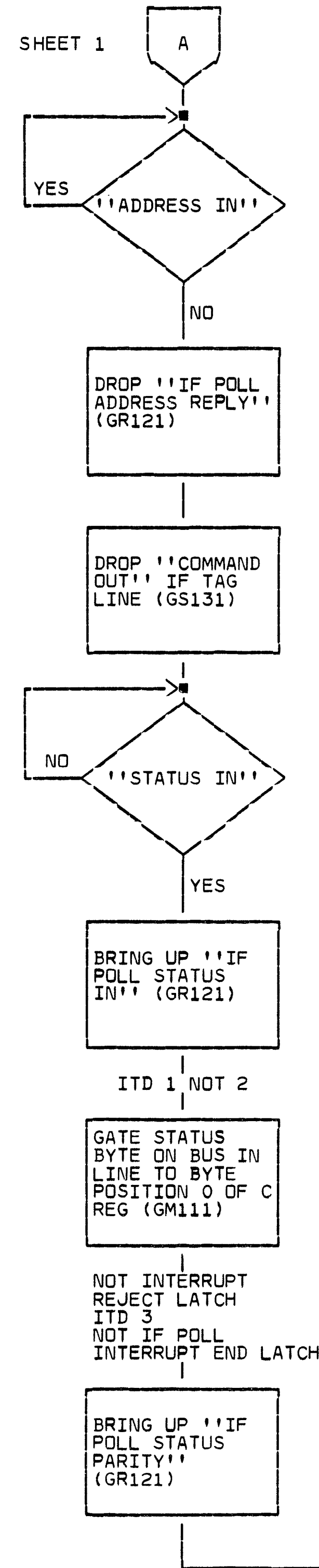




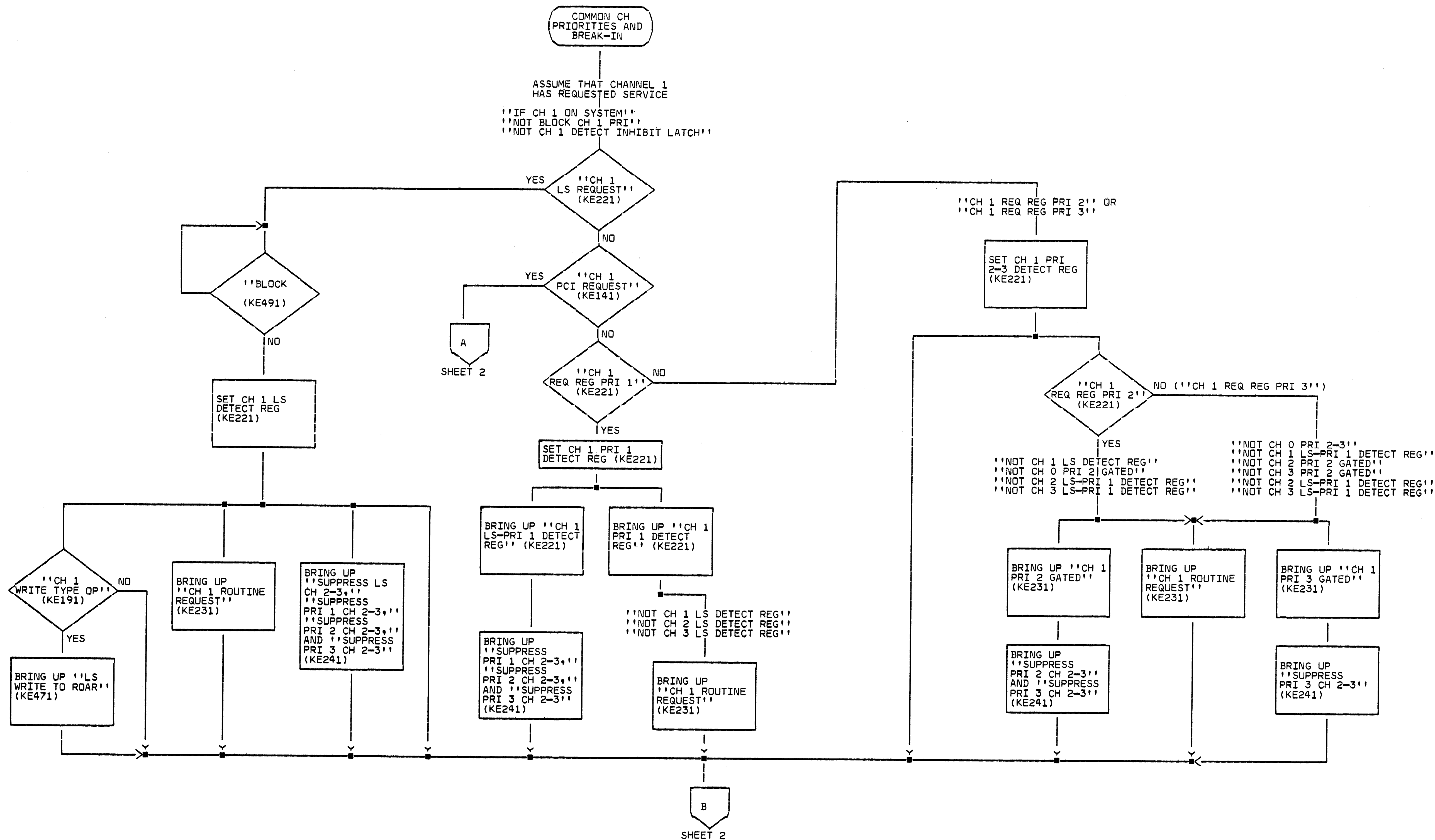










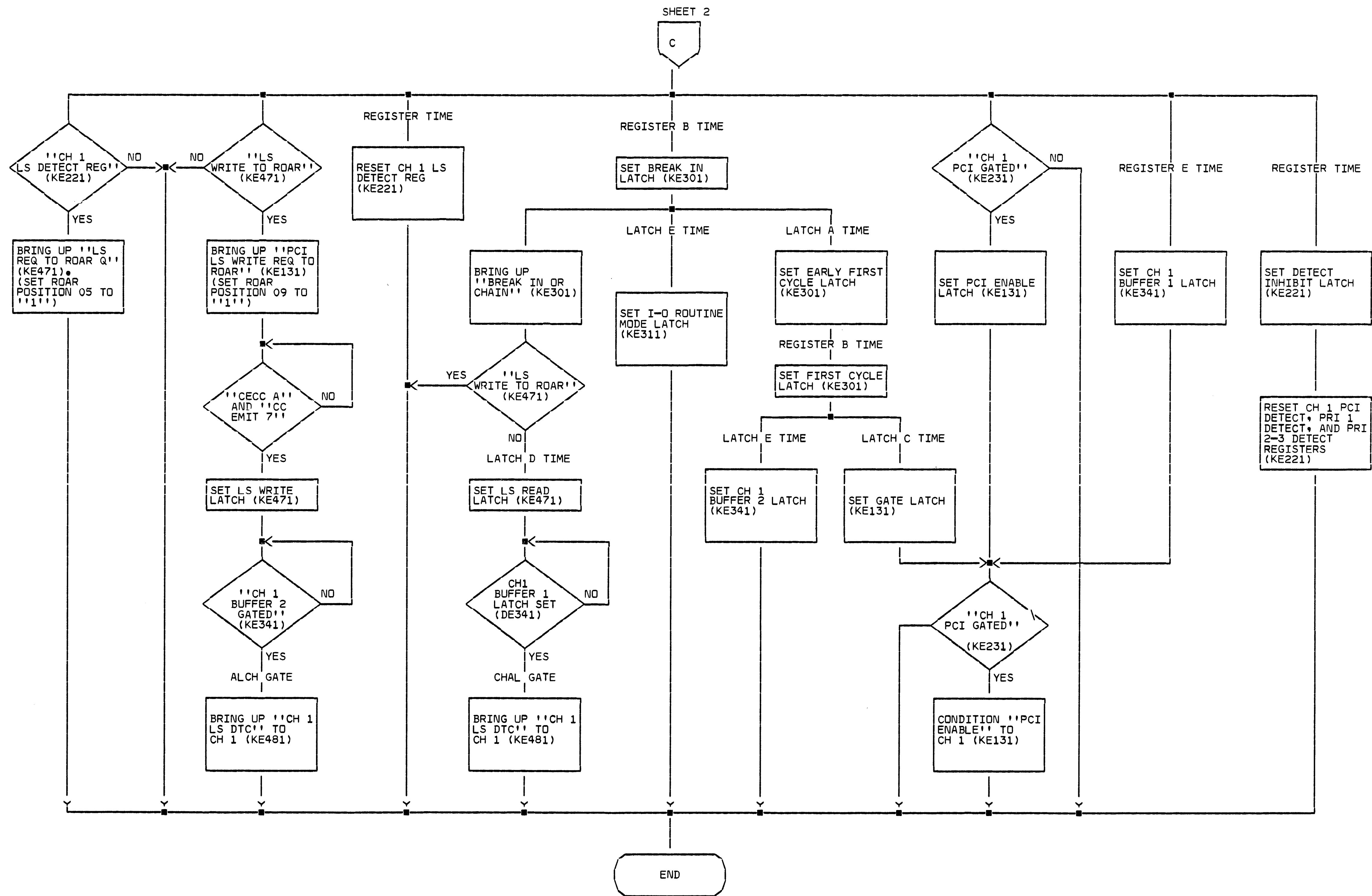


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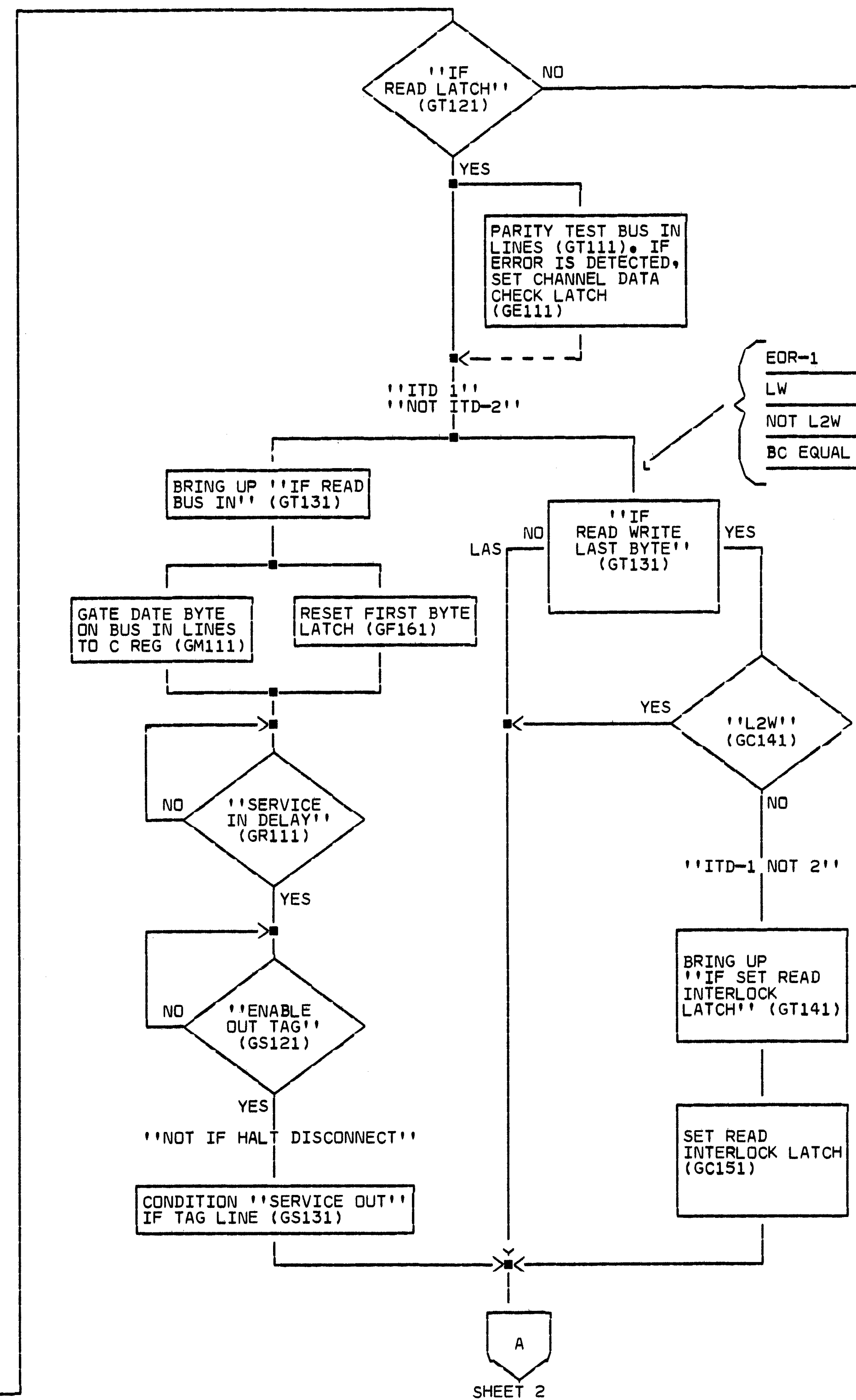
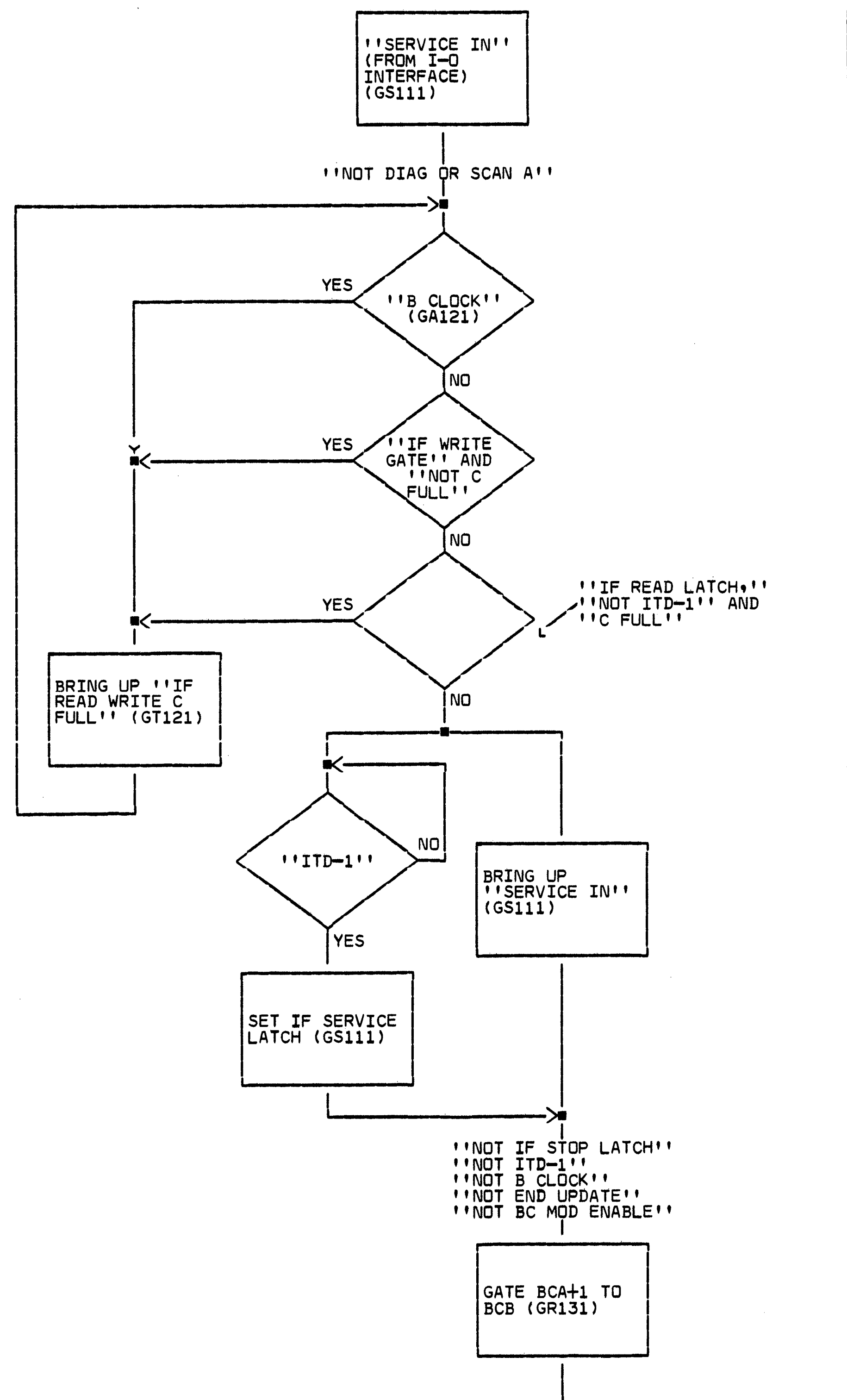
4014 COMMON CH PRIORITIES AND BREAK IN  
 DATE 16 JUL 65 MACH. 2050  
 FRAME  
 P.N.  
 IBM CORP. SDD PAGE 1

S4014





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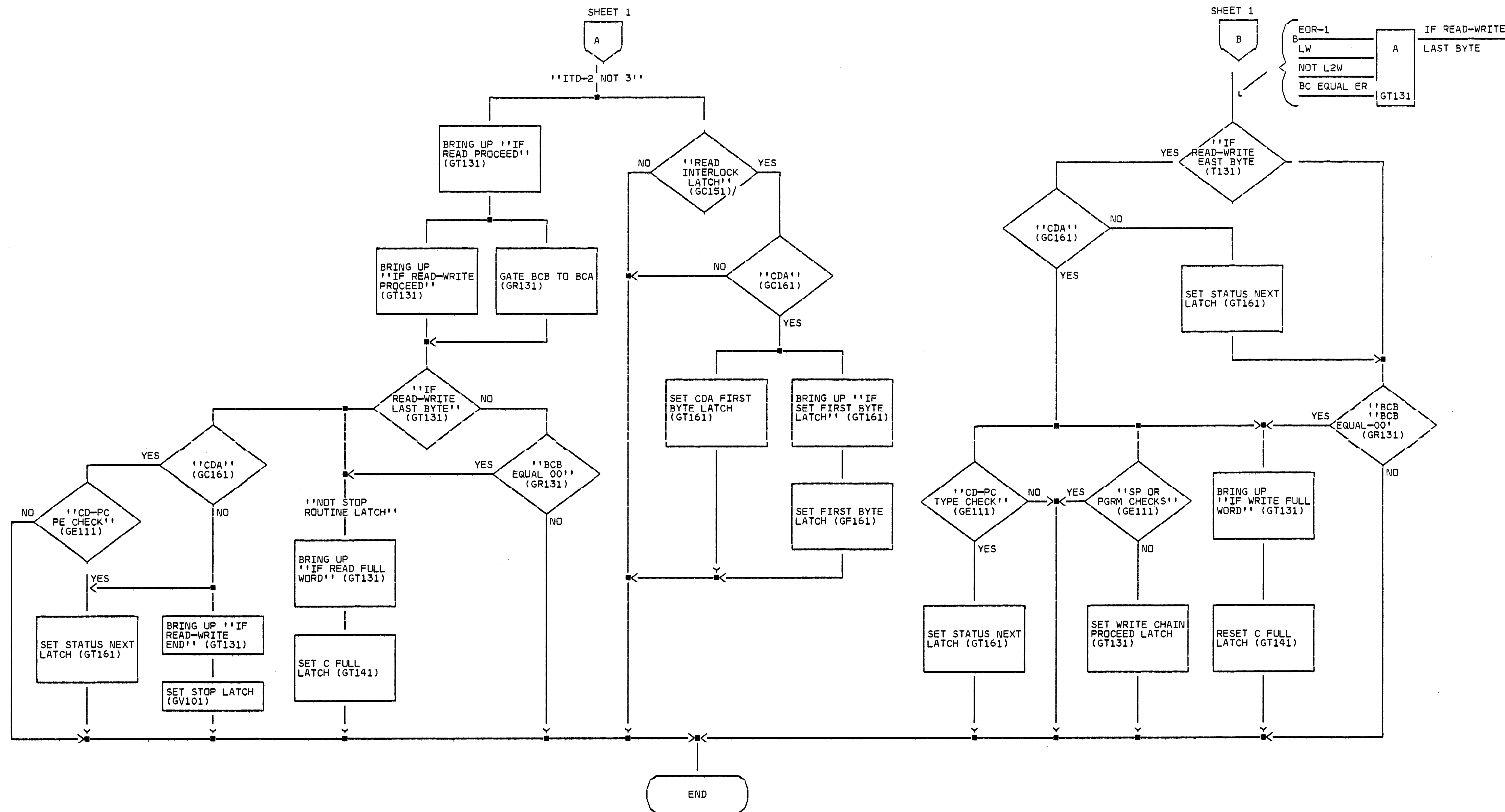
SHEET 2

SHEET 2

IBM CONFIDENTIAL

4015 SELECTOR CHANNEL RESPONSES TO SERVICE IN (SHEET 1 OF 2)  
 DATE 16 JUL 65 MACH. 2050  
 FRAME  
 P.N.  
 IBM CORP. SDD PAGE 1



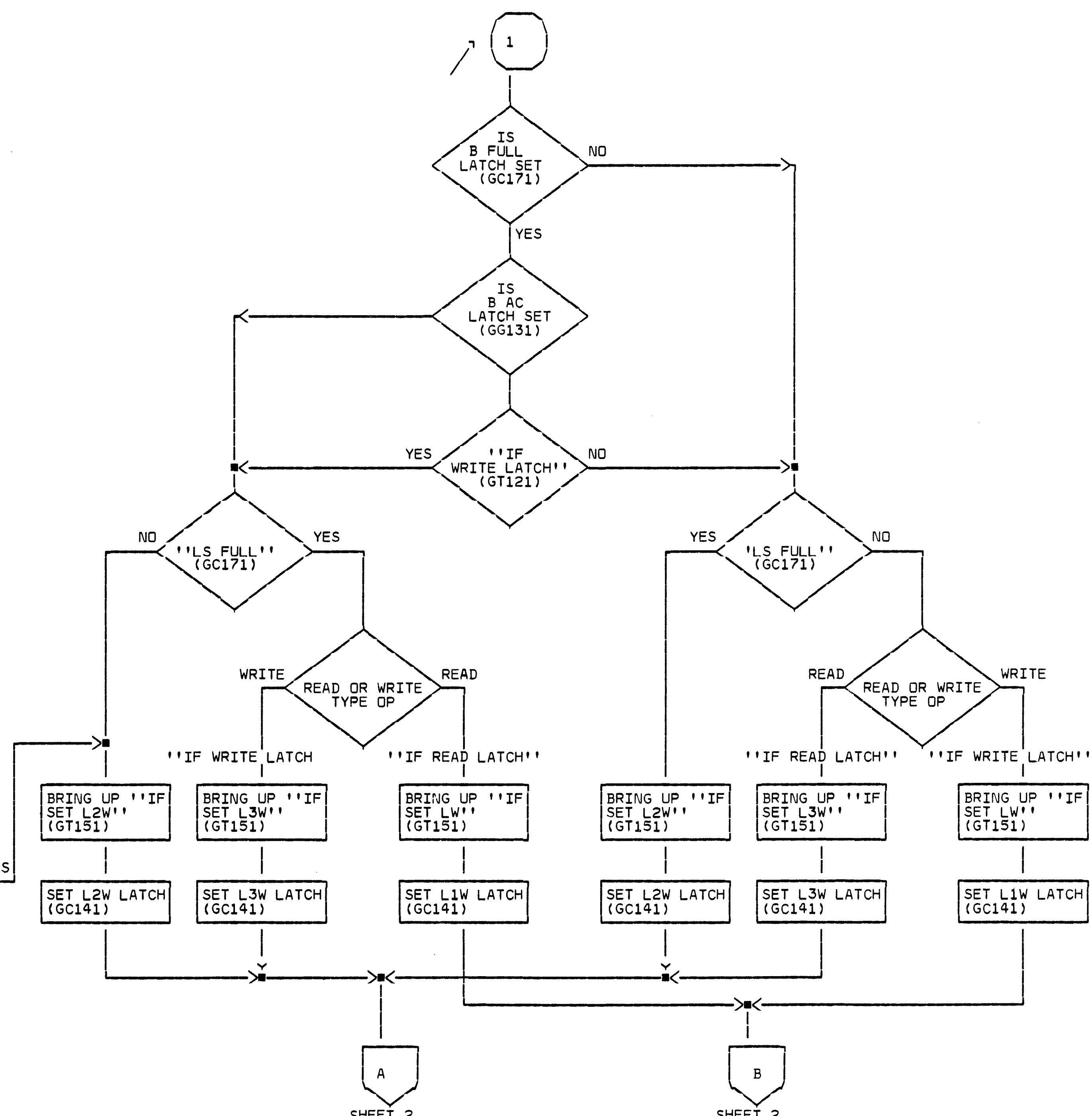
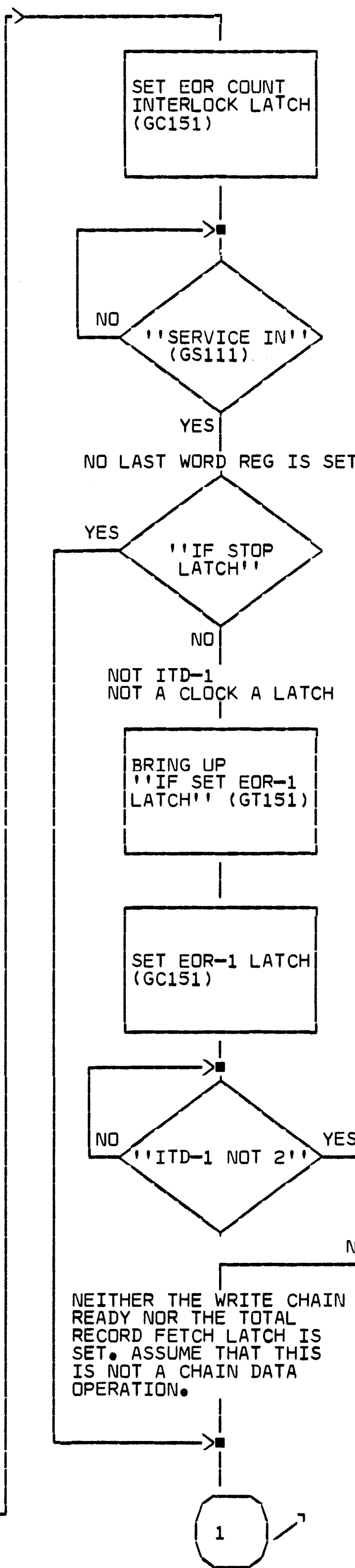
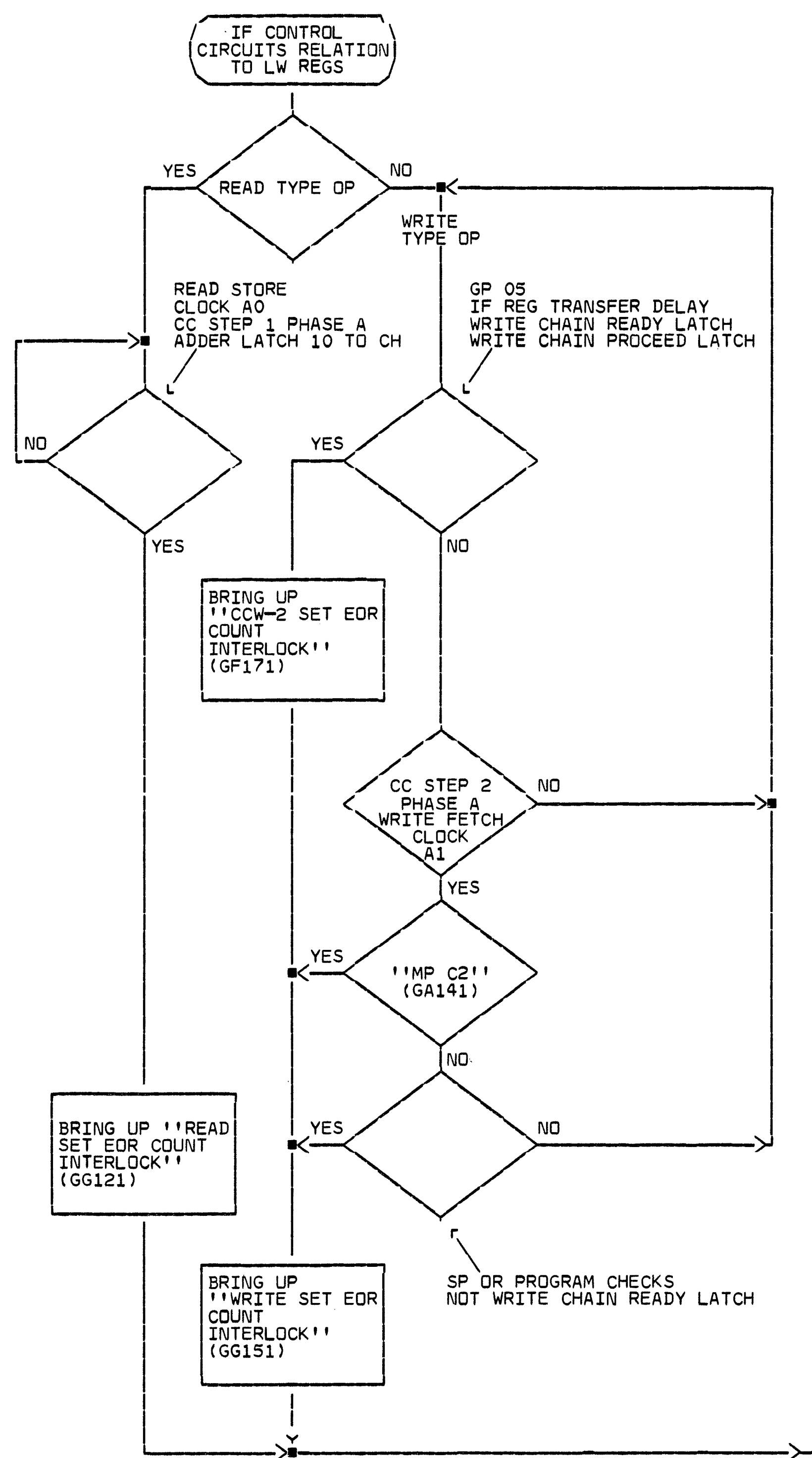


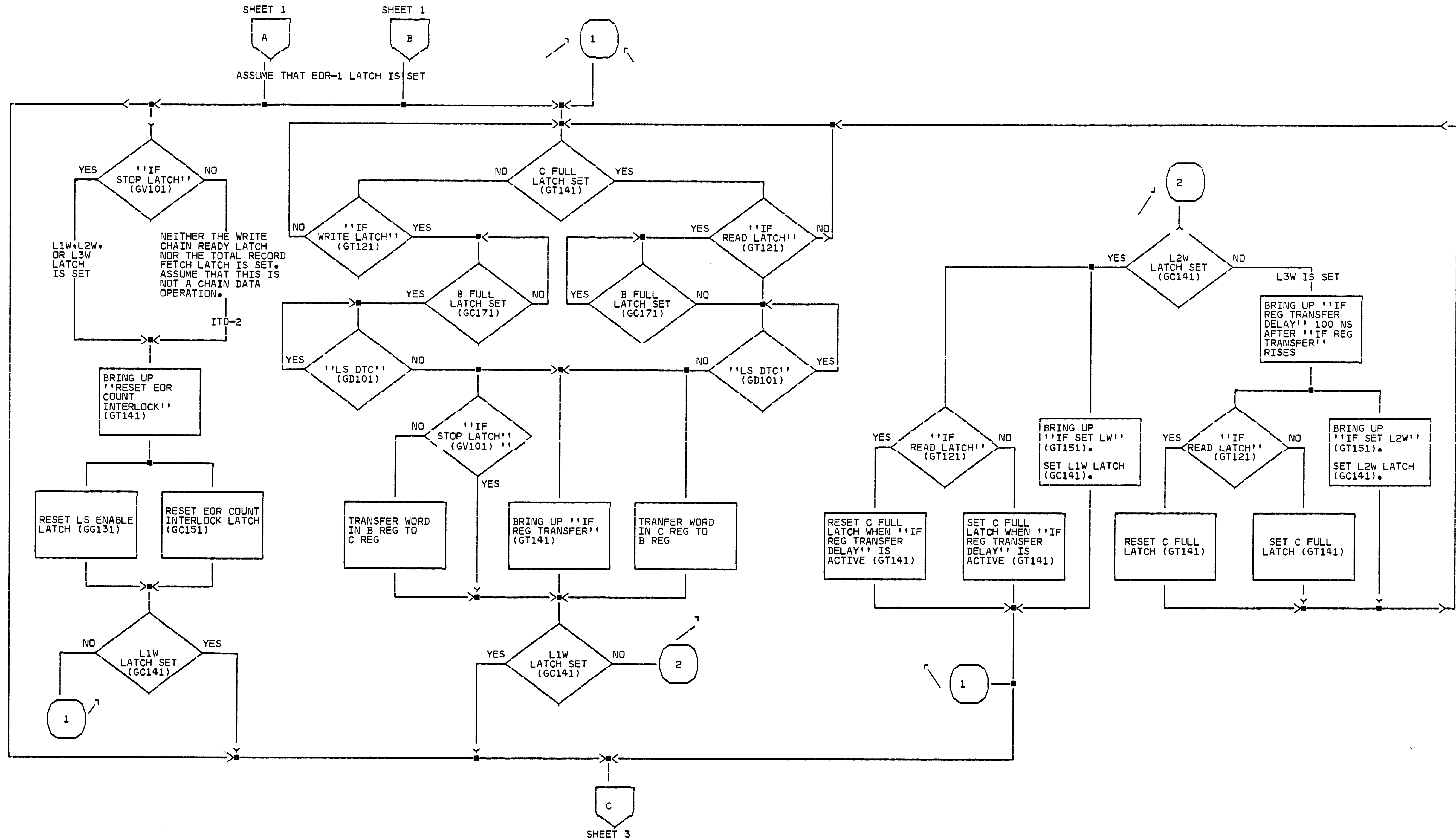
IBM CONFIDENTIAL

4015 SELECTOR CHANNEL  
 RESPONSES TO (L)AL)ASERVICE IN  
 DATE 16 JUL 65 MACH 2050

FRAME  
 P. N.  
 IBM CORP. SDD PAGE 2

S 4 0 1 5

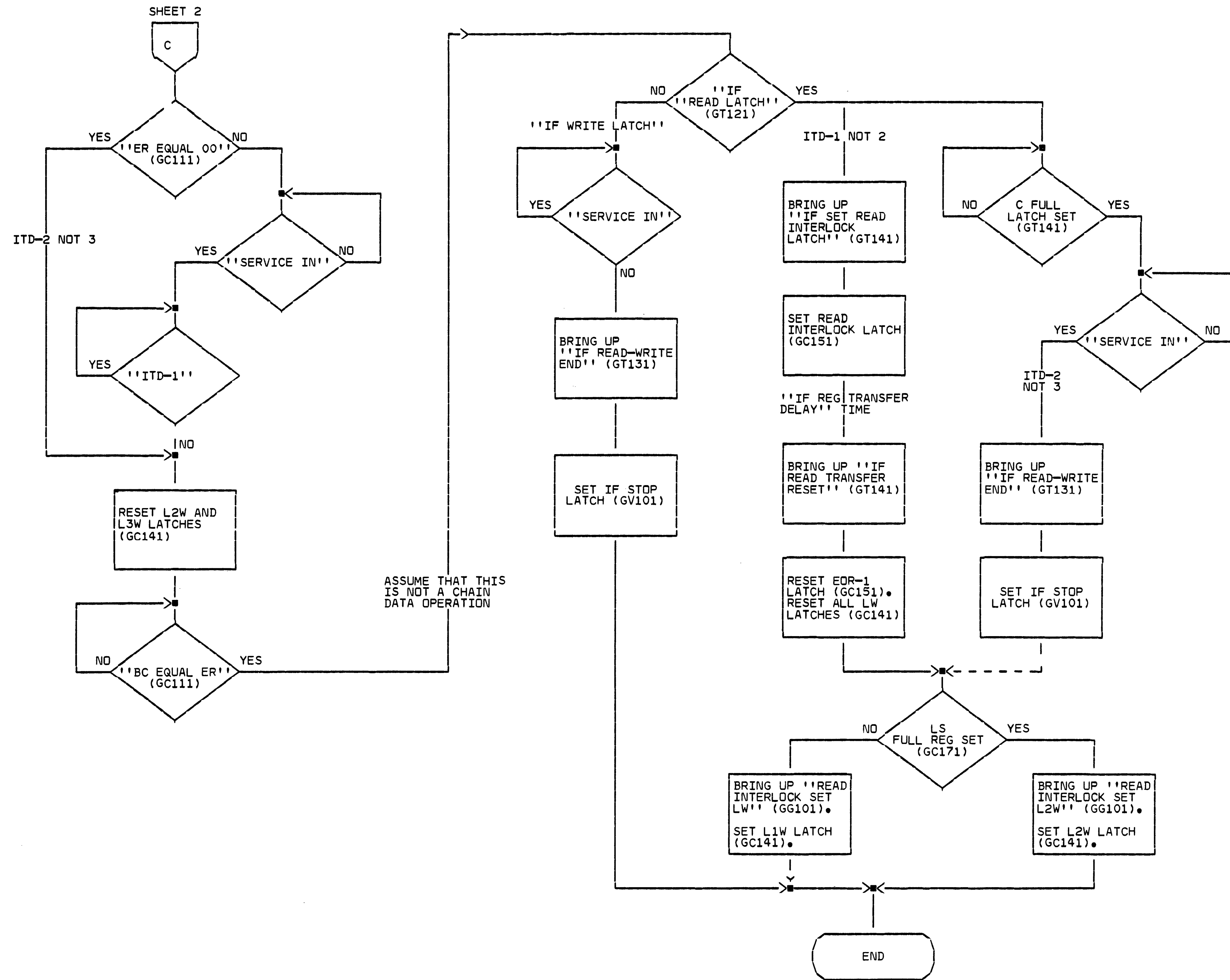


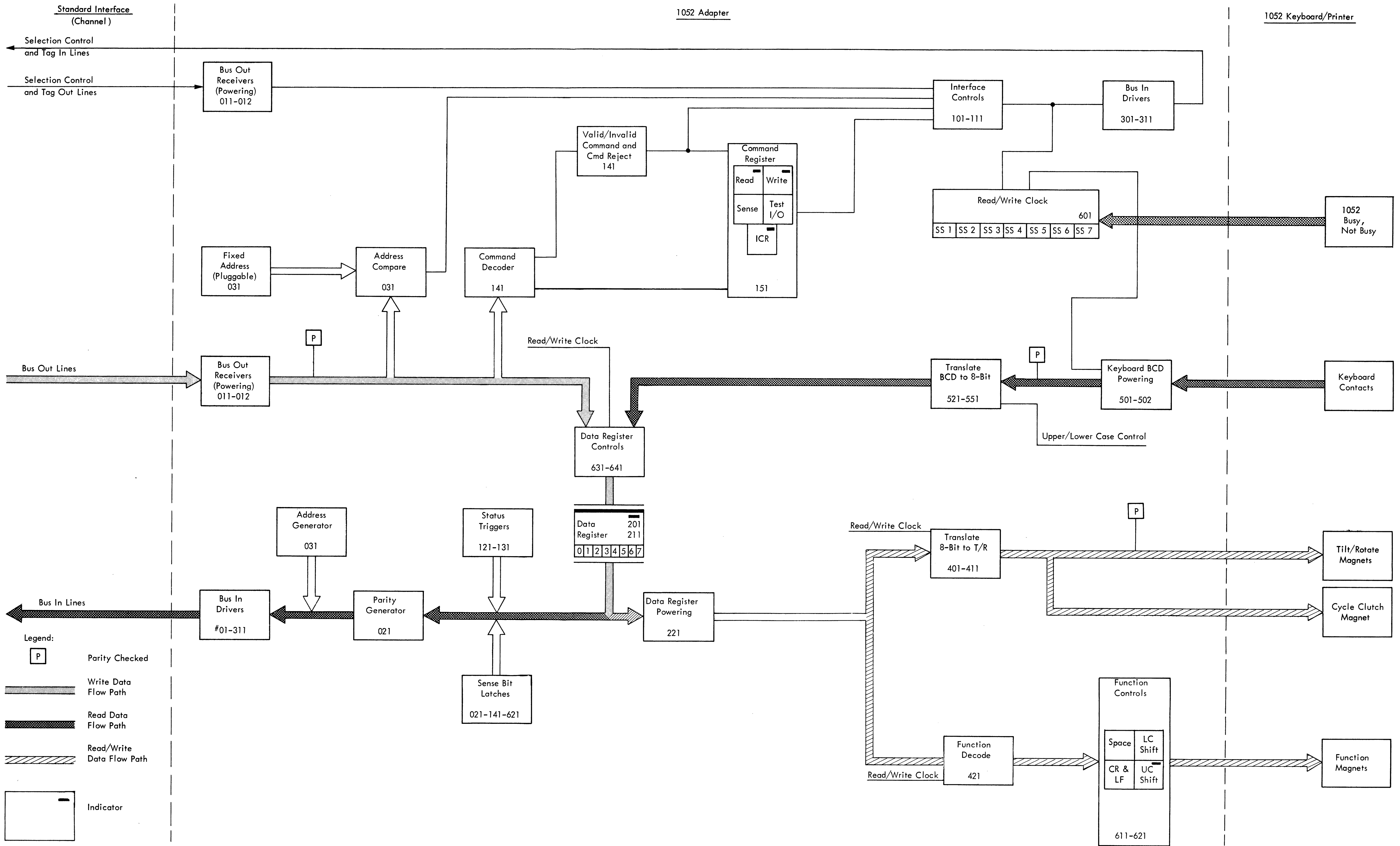


4016 IF CONTROL CIRCUITS  
 RELATION TO LW REGS  
 DATE 16 JUL 65 MACH. 2050  
 FRAME  
 P.No.  
 IBM CORP. SDD PAGE 2

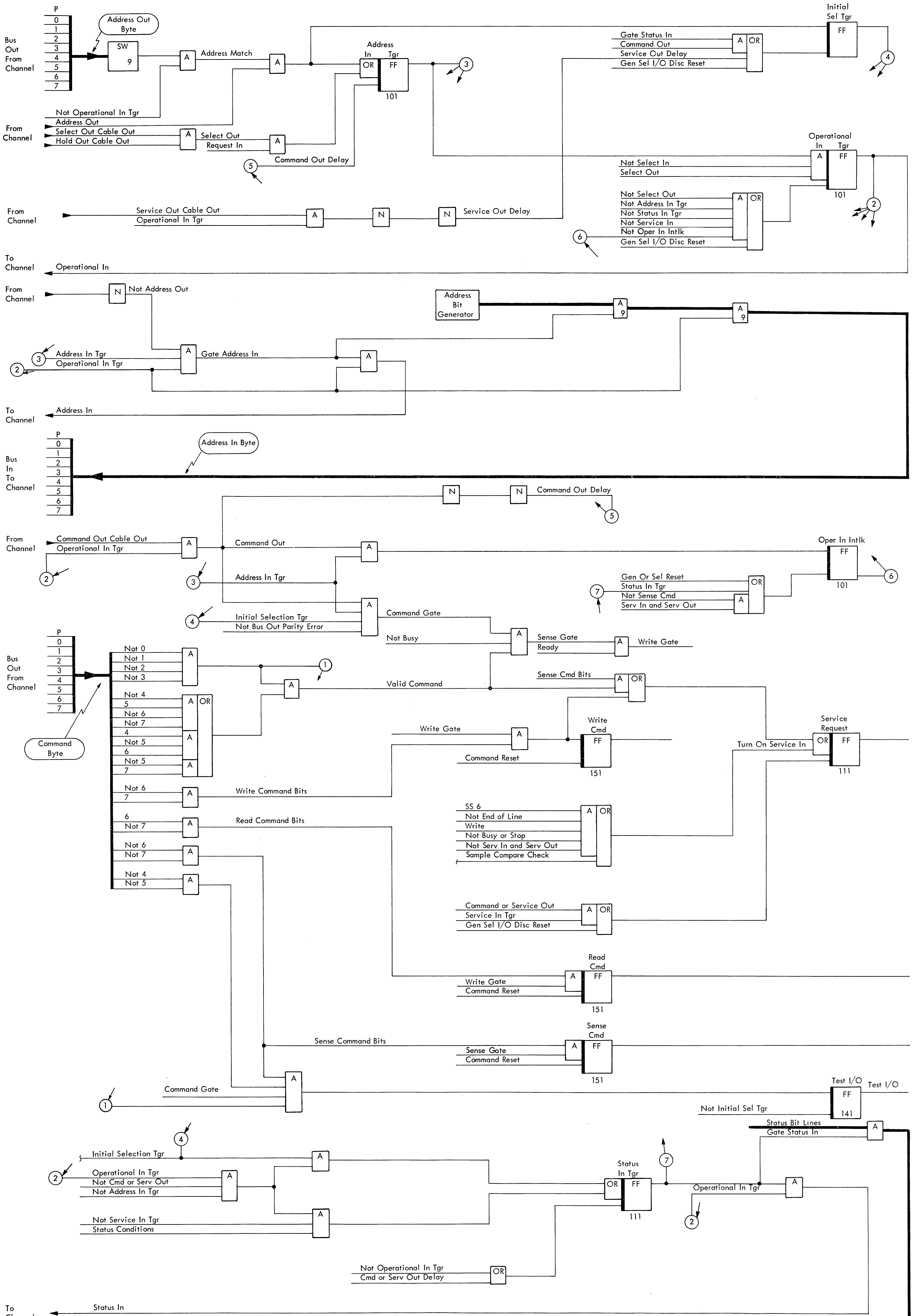
S  
4  
0  
1  
6

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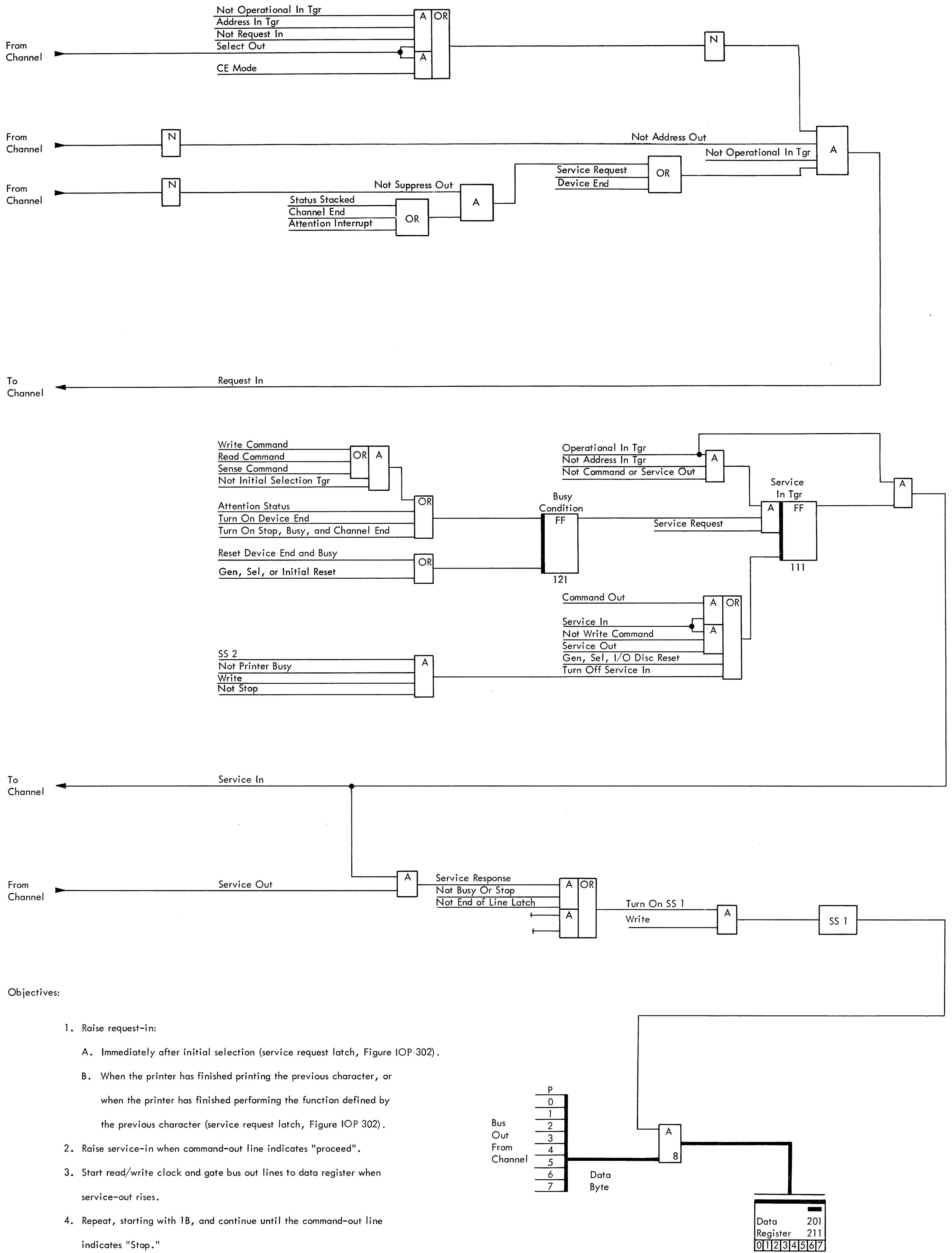
• FIGURE IOP 301. DATA FLOW--1052 ADAPTER UNIT



Objectives:

1. Match address-out byte with internally plugged address.
2. Raise Operational-in.
3. Raise address-in and gate address byte to bus-in lines when address-out falls.
4. Set command latches and drop address-in when command-out delay rises.
5. Raise status-in and gate status byte to bus-in lines when command-out falls.
6. Drop operational-in and status-in when service-out rises.

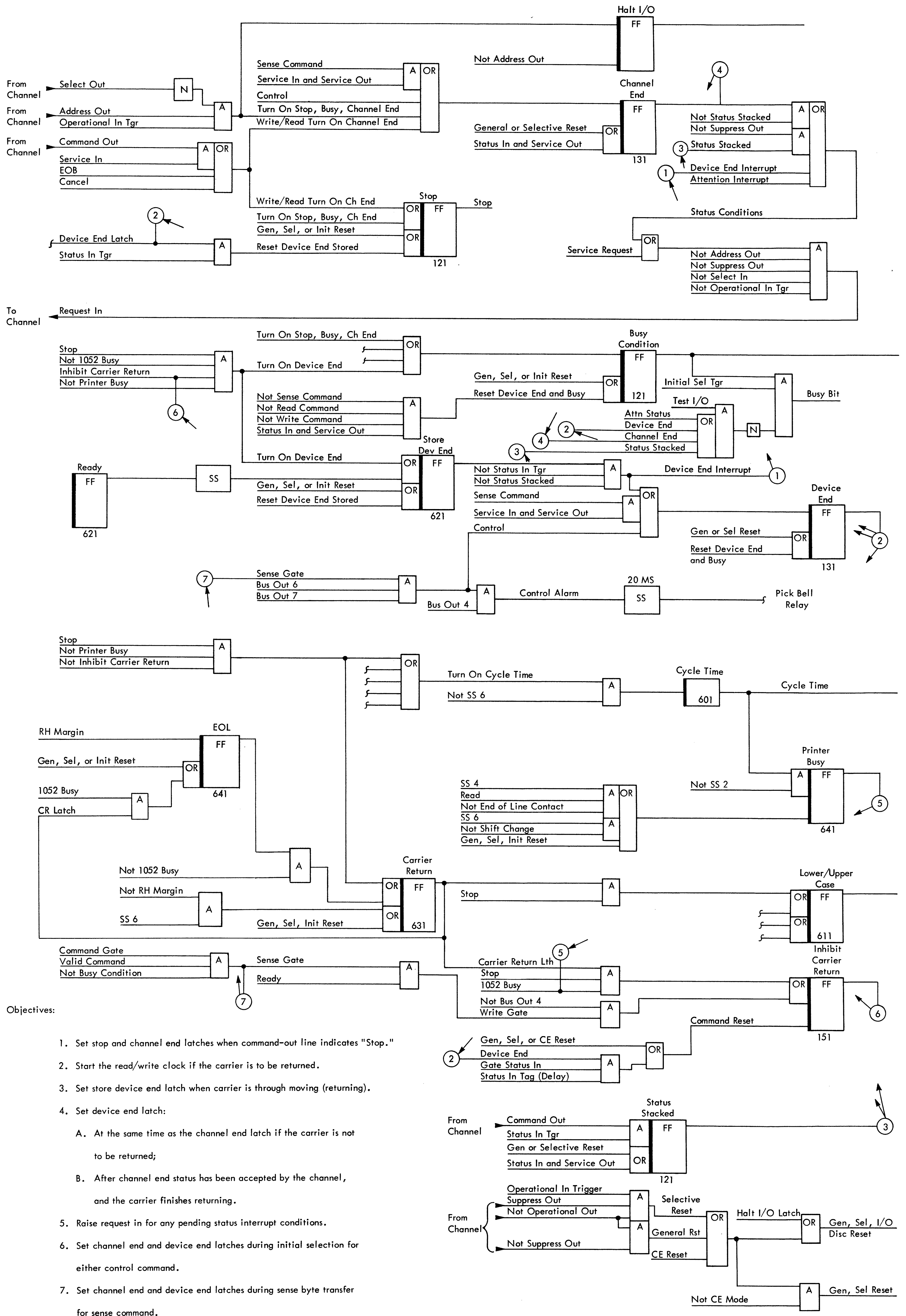
• FIGURE IOP 302. INITIAL SELECTION--READ, WRITE, SENSE (1052)



Objectives:

1. Raise request-in:
  - A. Immediately after initial selection (service request latch, Figure IOP 302).
  - B. When the printer has finished printing the previous character, or when the printer has finished performing the function defined by the previous character (service request latch, Figure IOP 302).
2. Raise service-in when command-out line indicates "proceed".
3. Start read/write clock and gate bus out lines to data register when service-out rises.
4. Repeat, starting with 1B, and continue until the command-out line indicates "Stop."

● FIGURE IOP 303. DATA TRANSFER--WRITE (1052)

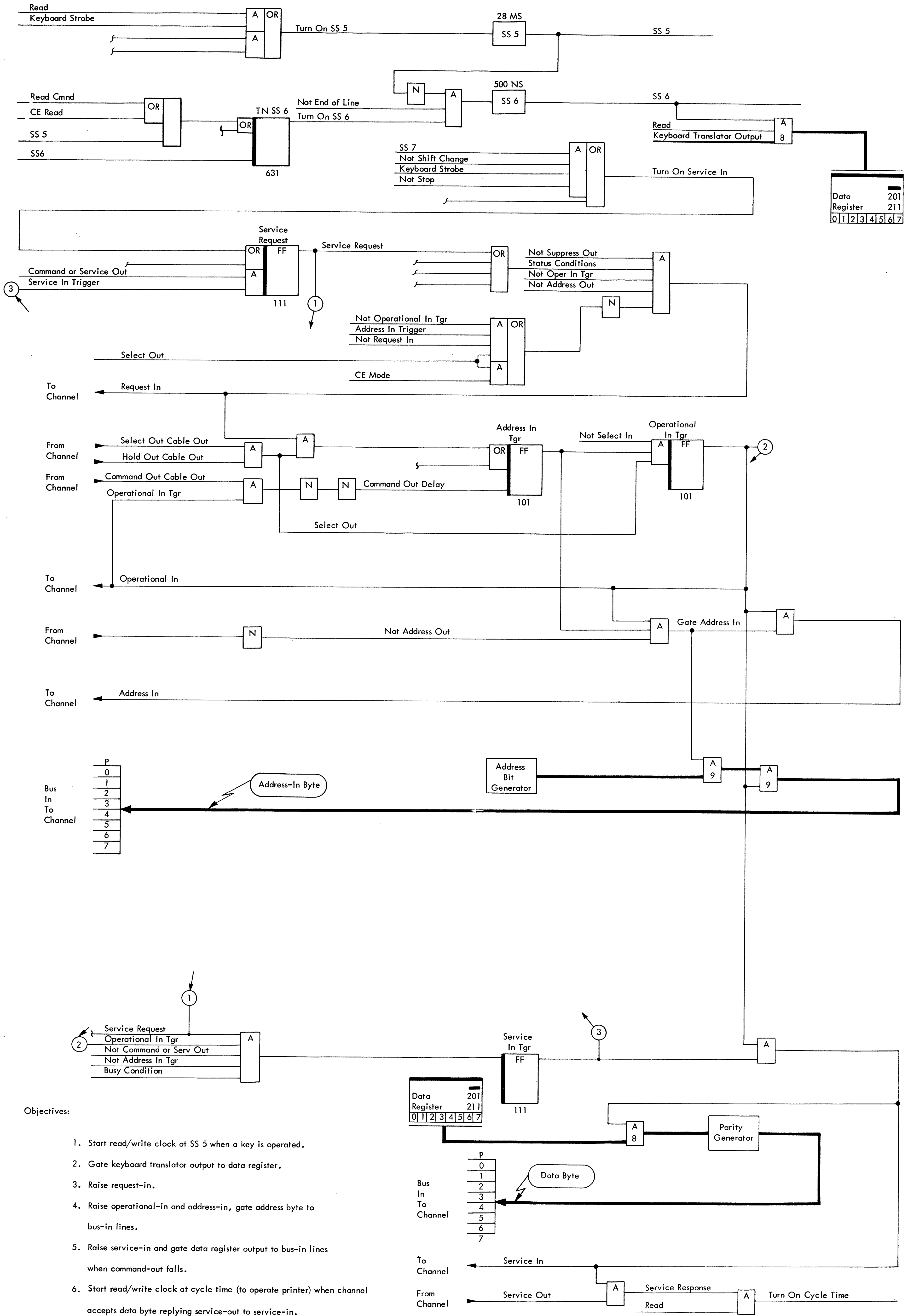


Objectives:

1. Set stop and channel end latches when command-out line indicates "Stop."
2. Start the read/write clock if the carrier is to be returned.
3. Set store device end latch when carrier is through moving (returning).
4. Set device end latch:
  - A. At the same time as the channel end latch if the carrier is not to be returned;
  - B. After channel end status has been accepted by the channel, and the carrier finishes returning.
5. Raise request in for any pending status interrupt conditions.
6. Set channel end and device end latches during initial selection for either control command.
7. Set channel end and device end latches during sense byte transfer for sense command.

● FIGURE IOP 304. ENDING SEQUENCE (1052)



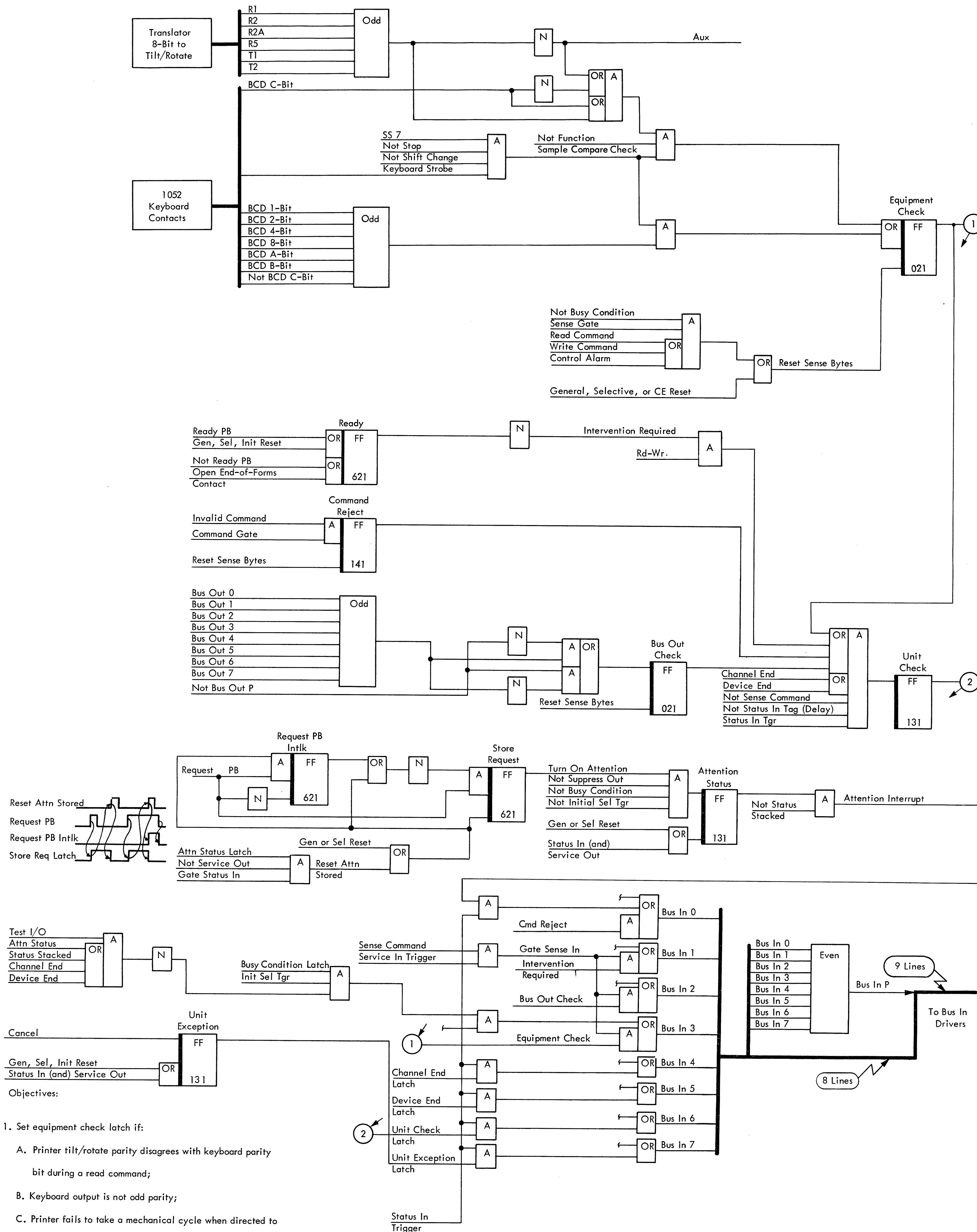


Objectives:

1. Start read/write clock at SS 5 when a key is operated.
2. Gate keyboard translator output to data register.
3. Raise request-in.
4. Raise operational-in and address-in, gate address byte to bus-in lines.
5. Raise service-in and gate data register output to bus-in lines when command-out falls.
6. Start read/write clock at cycle time (to operate printer) when channel accepts data byte replying service-out to service-in.

• FIGURE IOP 305. DATA TRANSFER--READ (1052)





- Objectives:
1. Set equipment check latch if:
    - A. Printer tilt/rotate parity disagrees with keyboard parity bit during a read command;
    - B. Keyboard output is not odd parity;
    - C. Printer fails to take a mechanical cycle when directed to print, up- or down-shift, tab, space, or backspace.
  2. Set unit check latch when status-in trigger is on for any of the following conditions:
    - A. Equipment check latch is on
    - B. Ready Latch is not on
    - C. Command reject latch is on
    - D. Bus-out check latch is on (even parity byte on bus-out lines).

• FIGURE IOP 306. SENSE AND STATUS BYTES (1052)

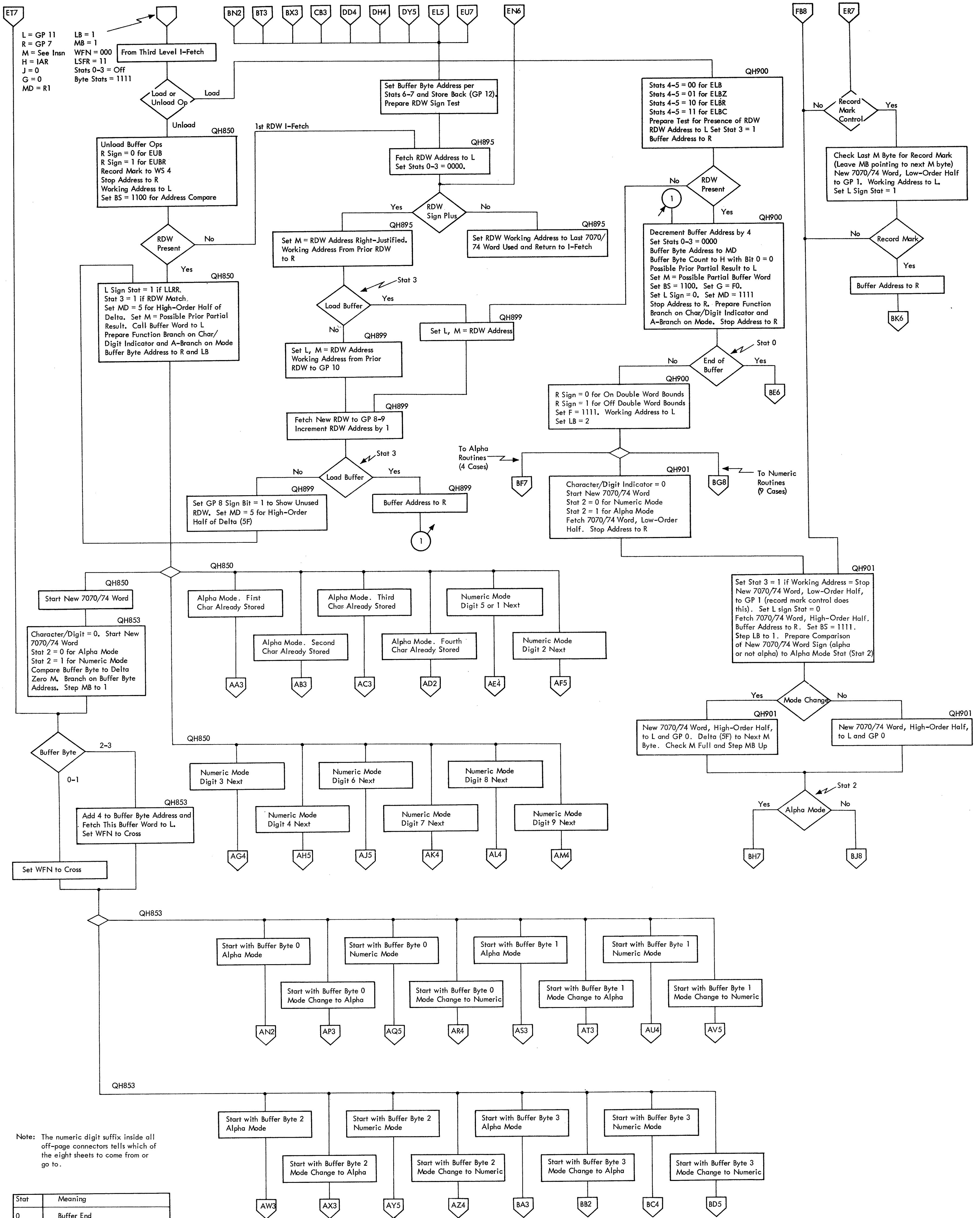
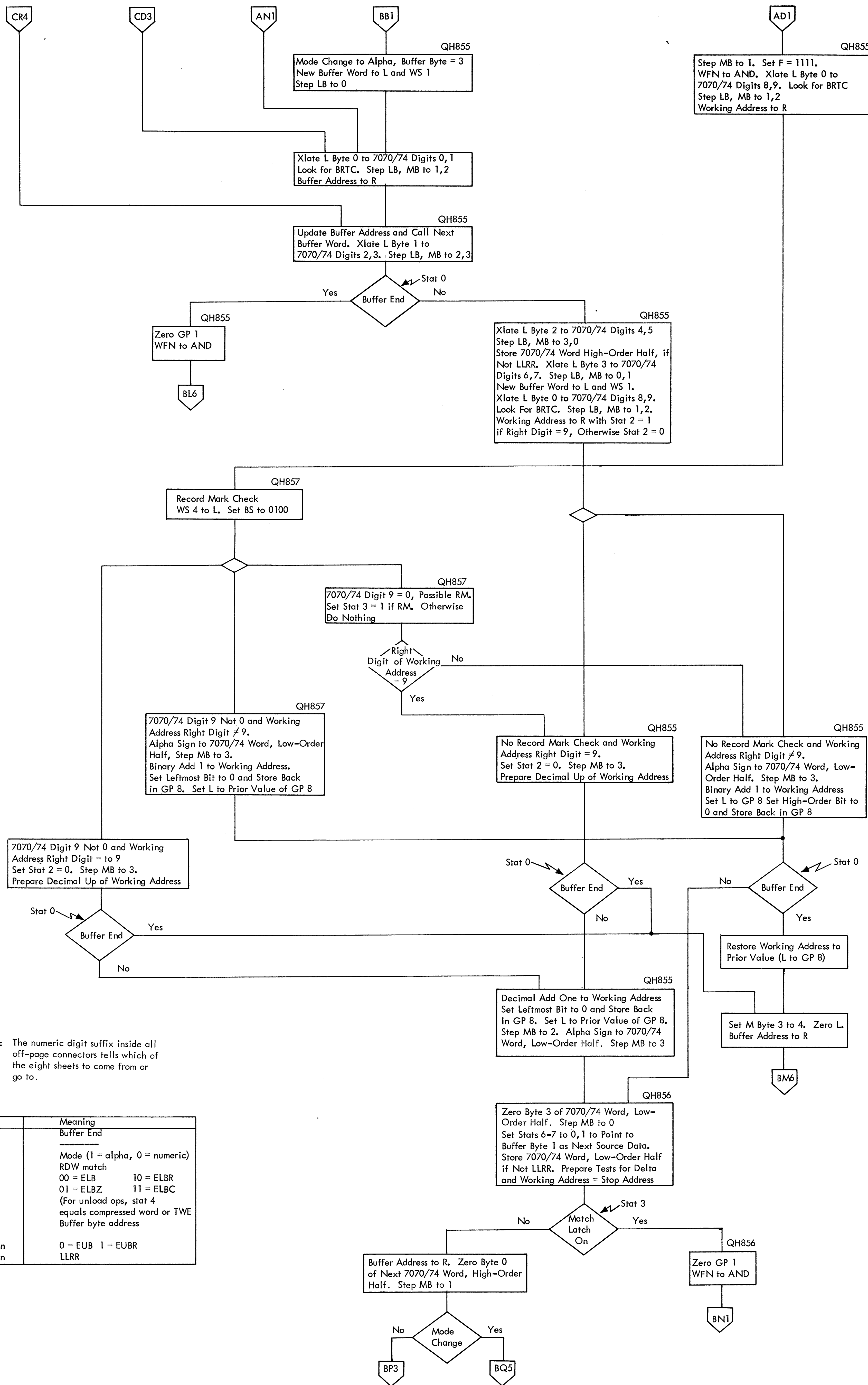


FIGURE CLF 800. BUFFER OPERATIONS -- INITIALIZE, START NEW 7070/74 WORD, RDW PROCESSING (SHEET 1 OF 8)



Note: The numeric digit suffix inside all off-page connectors tells which of the eight sheets to come from or go to.

Stat	Meaning
0	Buffer End
1	-----
2	Mode (1 = alpha, 0 = numeric)
3	RDW match
4	00 = ELB      10 = ELBR
5	01 = ELBZ     11 = ELBC
	(For unload ops, stat 4 equals compressed word or TWE)
6	Buffer byte address
7	
R Sign	0 = EUB 1 = EUBR
L Sign	LLRR

FIGURE CLF 800. BUFFER OPERATIONS -- UNLOAD BUFFER ALPHA MODE, BUFFER BYTE 0 (SHEET 2 OF 8)

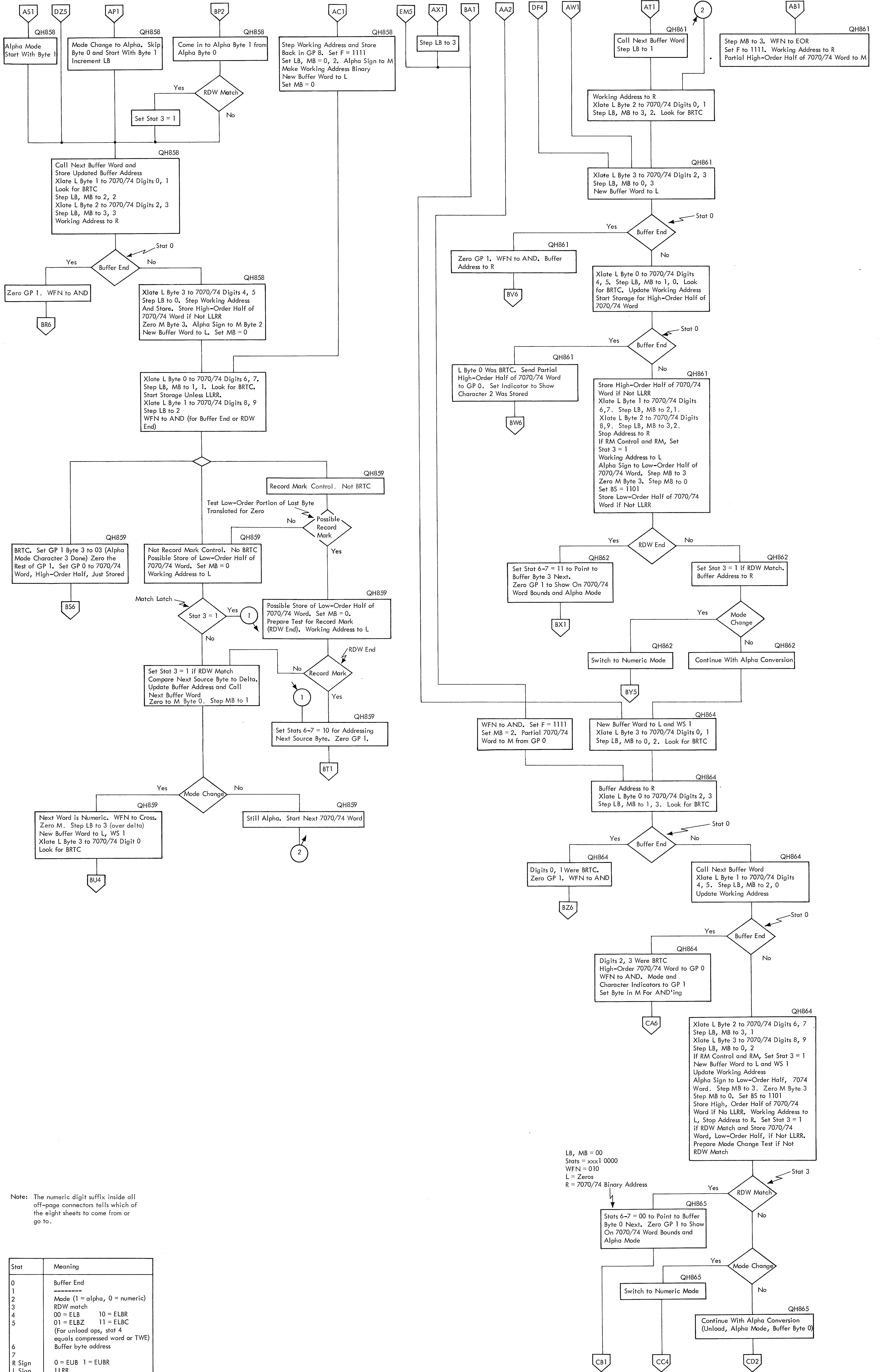
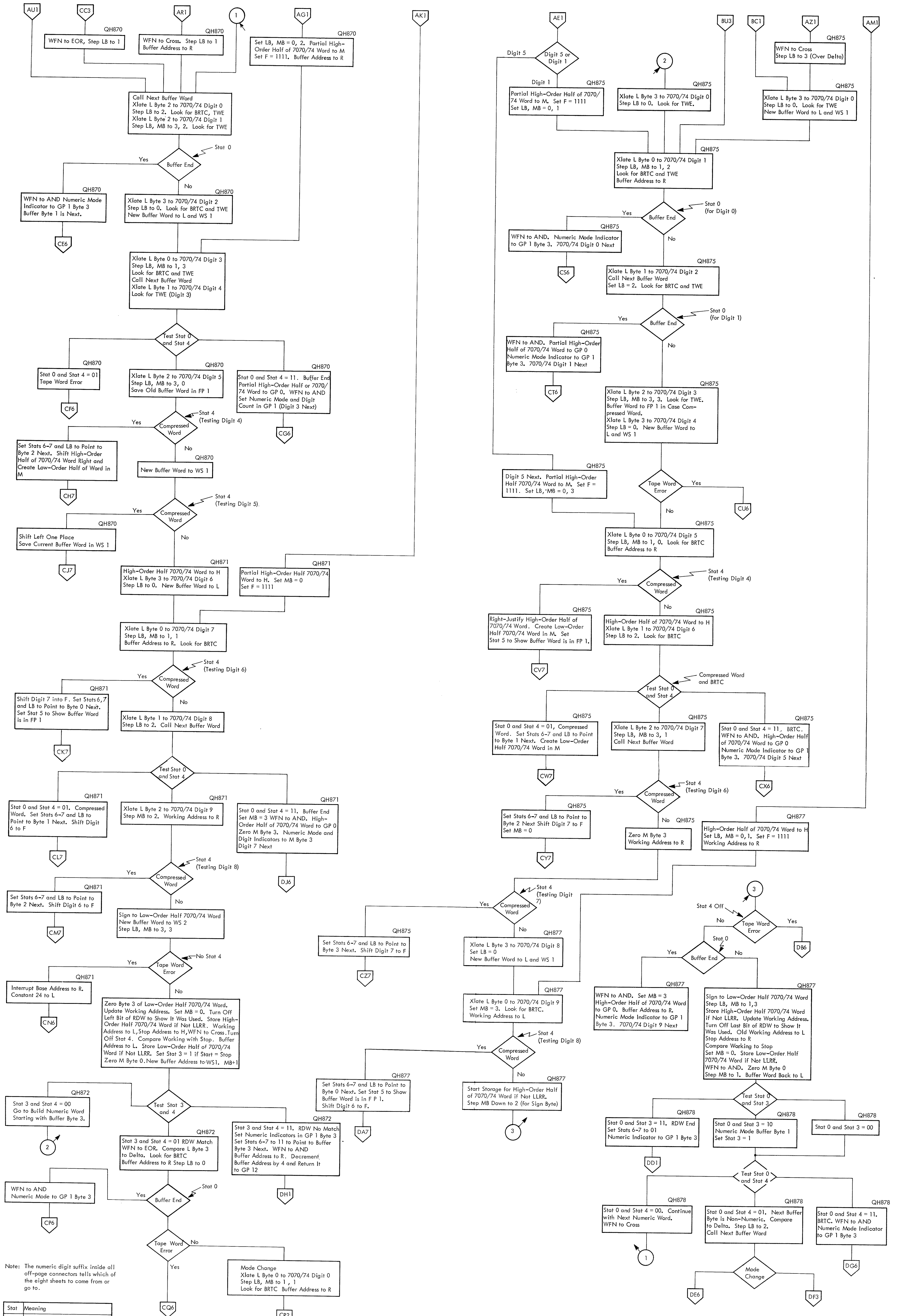


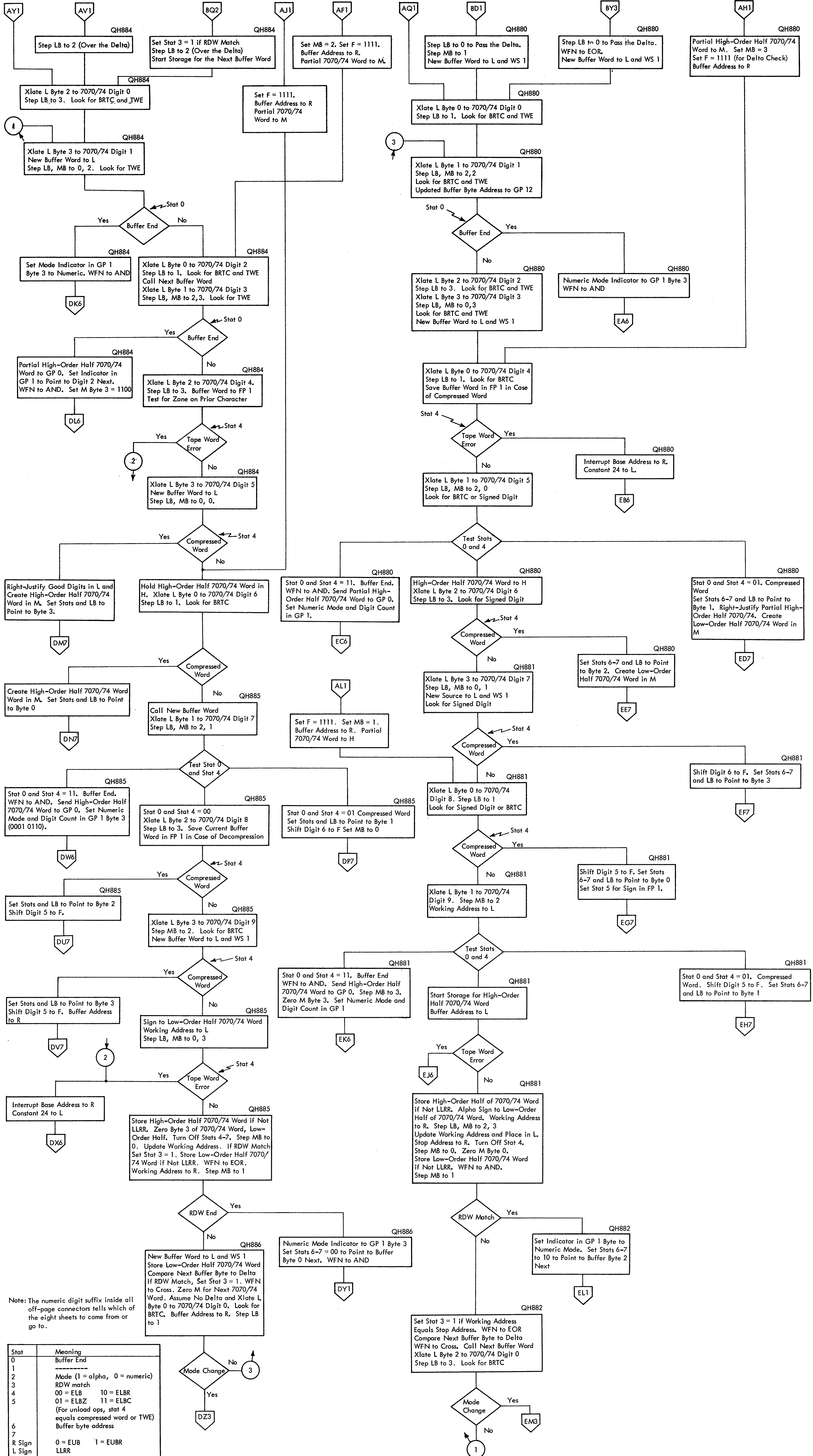
FIGURE CLF 800. BUFFER OPERATIONS -- UNLOAD BUFFER ALPHA MODE, BUFFER BYTES 1, 2, 3 (SHEET 3 OF 8)



Note: The numeric digit suffix inside all off-page connectors tells which of the eight sheets to come from or go to.

Stat	Meaning
0	Buffer End
1	-----
2	Mode (1 = alpha, 0 = numeric)
3	RDW match
4	00 = ELB 10 = ELBR
5	01 = ELBZ 11 = ELBC (for unload ops, stat 4 equals compressed word or TWE Buffer byte address)
6	7
R	Sign 0 = EUB 1 = EUBR
L	Sign LLRR

FIGURE CLF 800. BUFFER OPERATIONS -- UNLOAD BUFFER NUMERIC MODE, BUFFER BYTES 1 AND 3 (SHEET 4 OF 8)

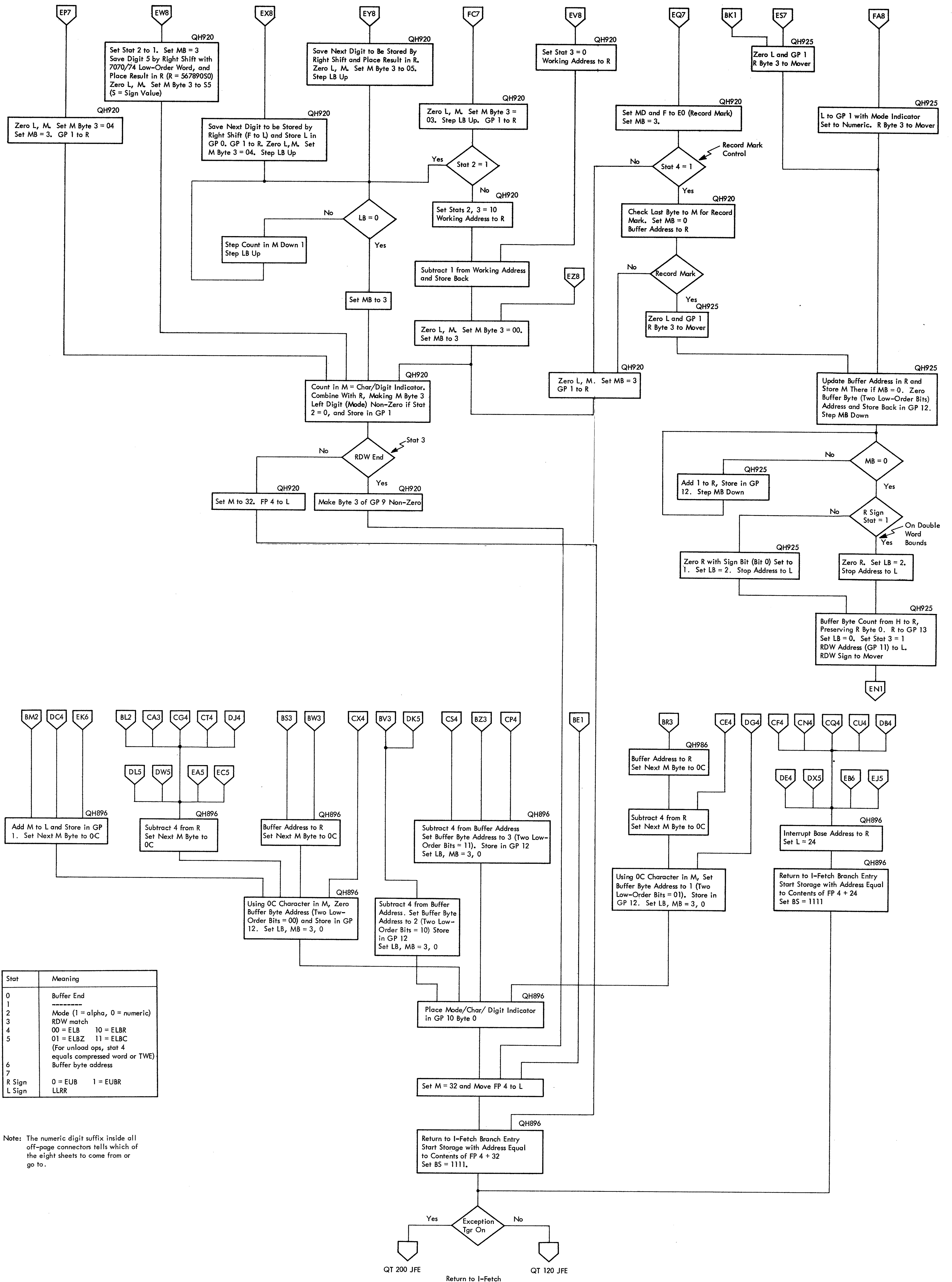


Note: The numeric digit suffix inside all off-page connectors tells which of the eight sheets to come from or go to.

Stat	Meaning
0	Buffer End
1	Mode Change
2	Mode (1 = alpha, 0 = numeric)
3	RDW match
4	00 = ELB 10 = ELBR
5	01 = ELBZ 11 = ELBC (For unload ops, stat 4 equals compressed word or TWE)
6	Buffer byte address
7	
R Sign	0 = EUB 1 = EUBR
L Sign	LLRR

FIGURE CLF 800. BUFFER OPERATIONS -- UNLOAD BUFFER NUMERIC MODE, BUFFER BYTES 0 AND 2 (SHEET 5 OF 8)

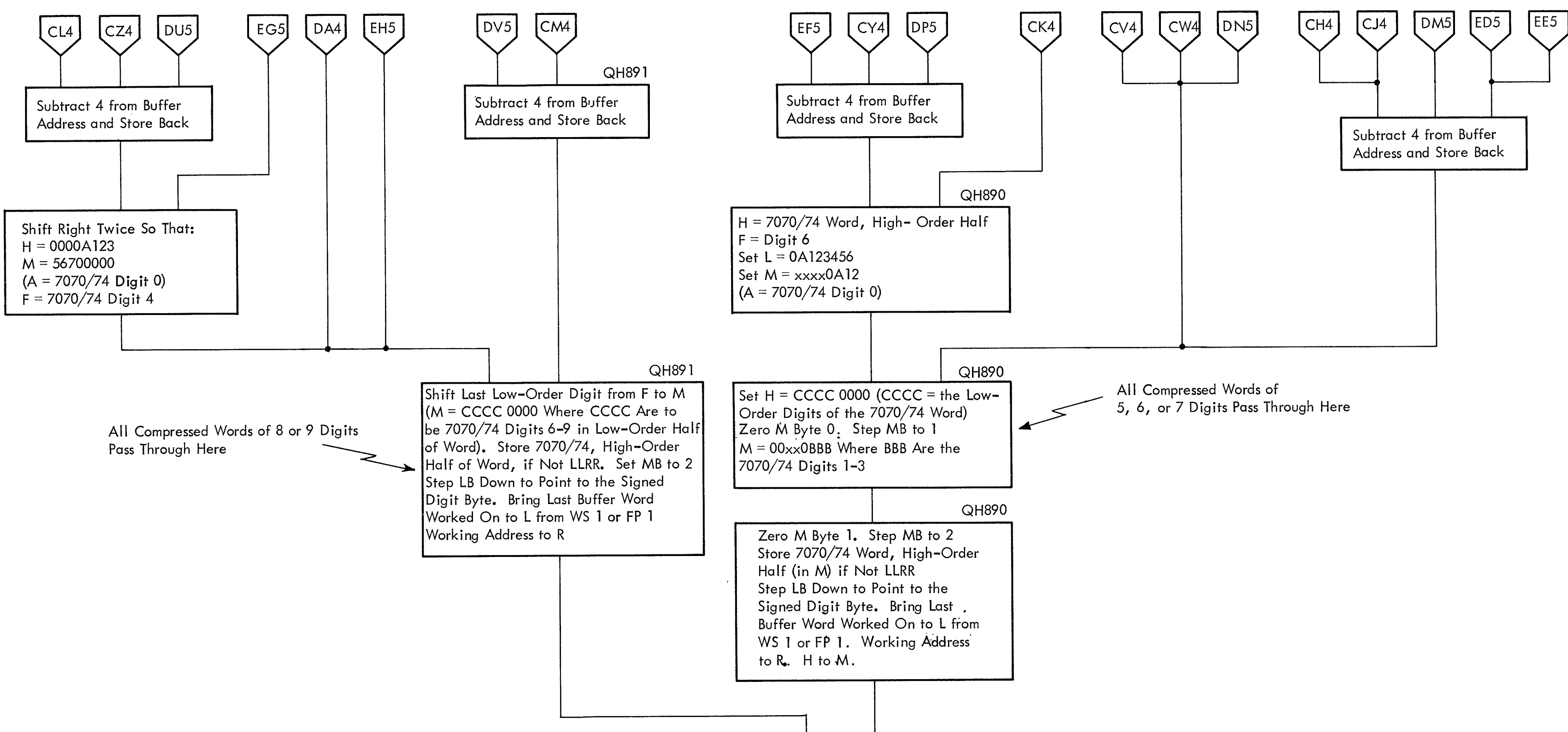
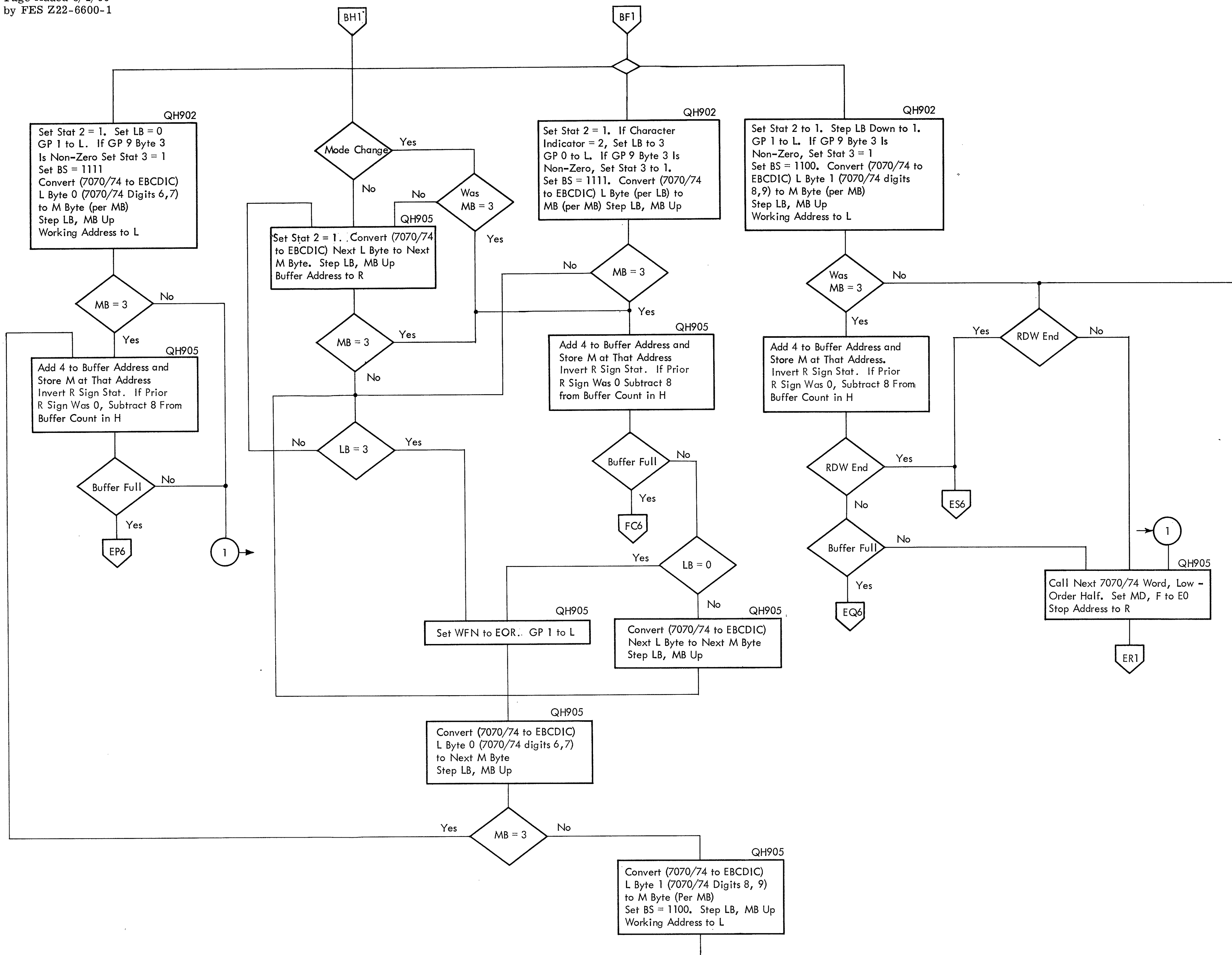




Stat	Meaning
0	Buffer End
1	-----
2	Mode (1 = alpha, 0 = numeric)
3	RDW match
4	00 = ELB 10 = ELBR
5	01 = ELBZ 11 = ELBC
	(For unload ops, stat 4 equals compressed word or TWE)
6	Buffer byte address
7	
R Sign	0 = EUB 1 = EUBR
L Sign	LLRR

Note: The numeric digit suffix inside all off-page connectors tells which of the eight sheets to come from or go to.

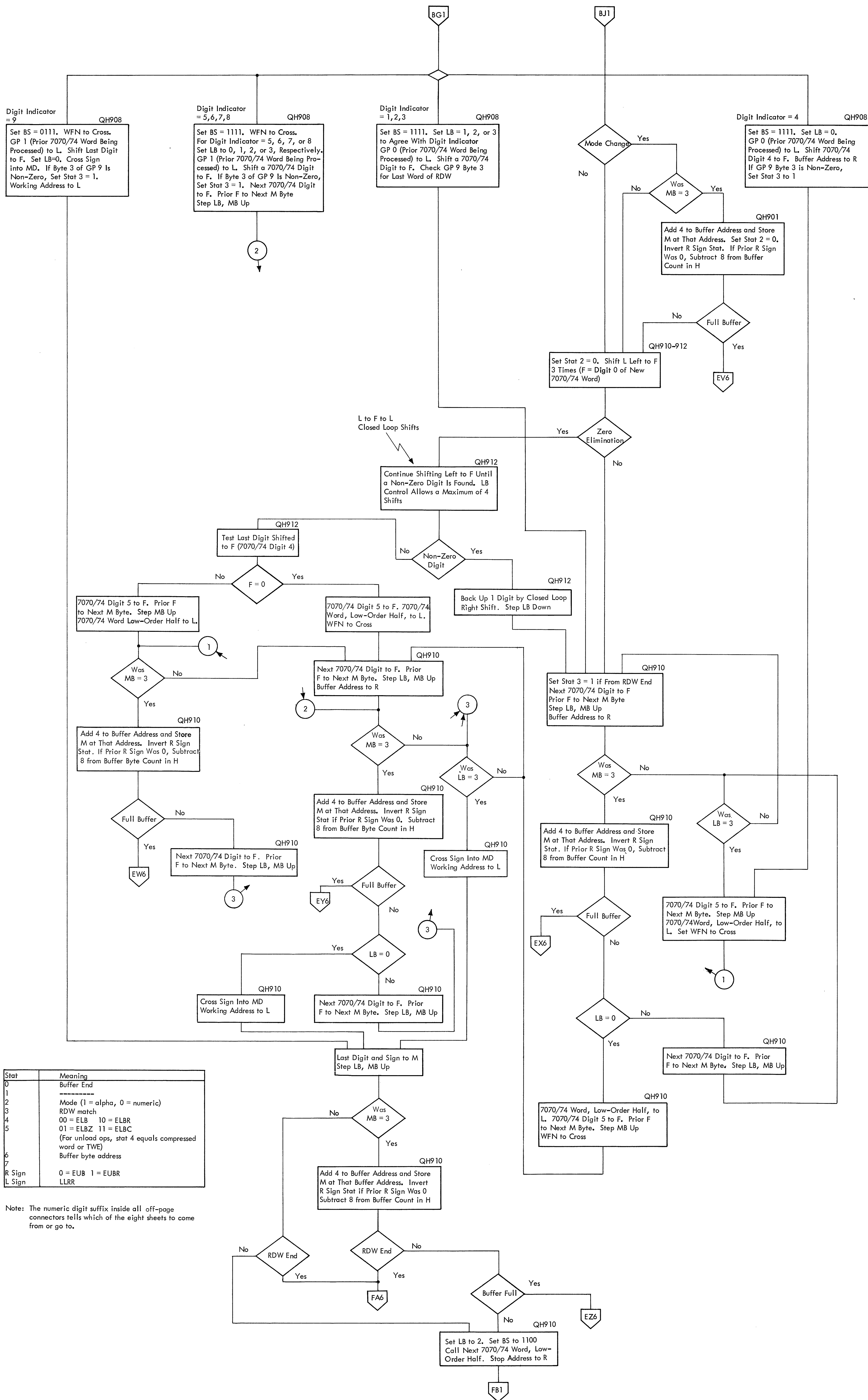
FIGURE CLF 800. BUFFER OPERATIONS -- UNLOAD BUFFER BRTC EXIT, LOAD BUFFER BUFFER END AND/OR RDW END (SHEET 6 OF 8)



Stat	Meaning
0	Buffer End
1	-----
2	Mode (1 = alpha, 0 = numeric)
3	RDW match
4	00 = ELB 10 = ELBR
5	01 = ELBZ 11 = ELBC (For unload ops, stat 4 equals compressed word or TWE)
6	Buffer byte address
7	
R Sign	0 = EUB 1 = EUBR
L Sign	LLRR

Note: The numeric digit suffix inside all off-page connectors tells which of the eight sheets to come from or go to.

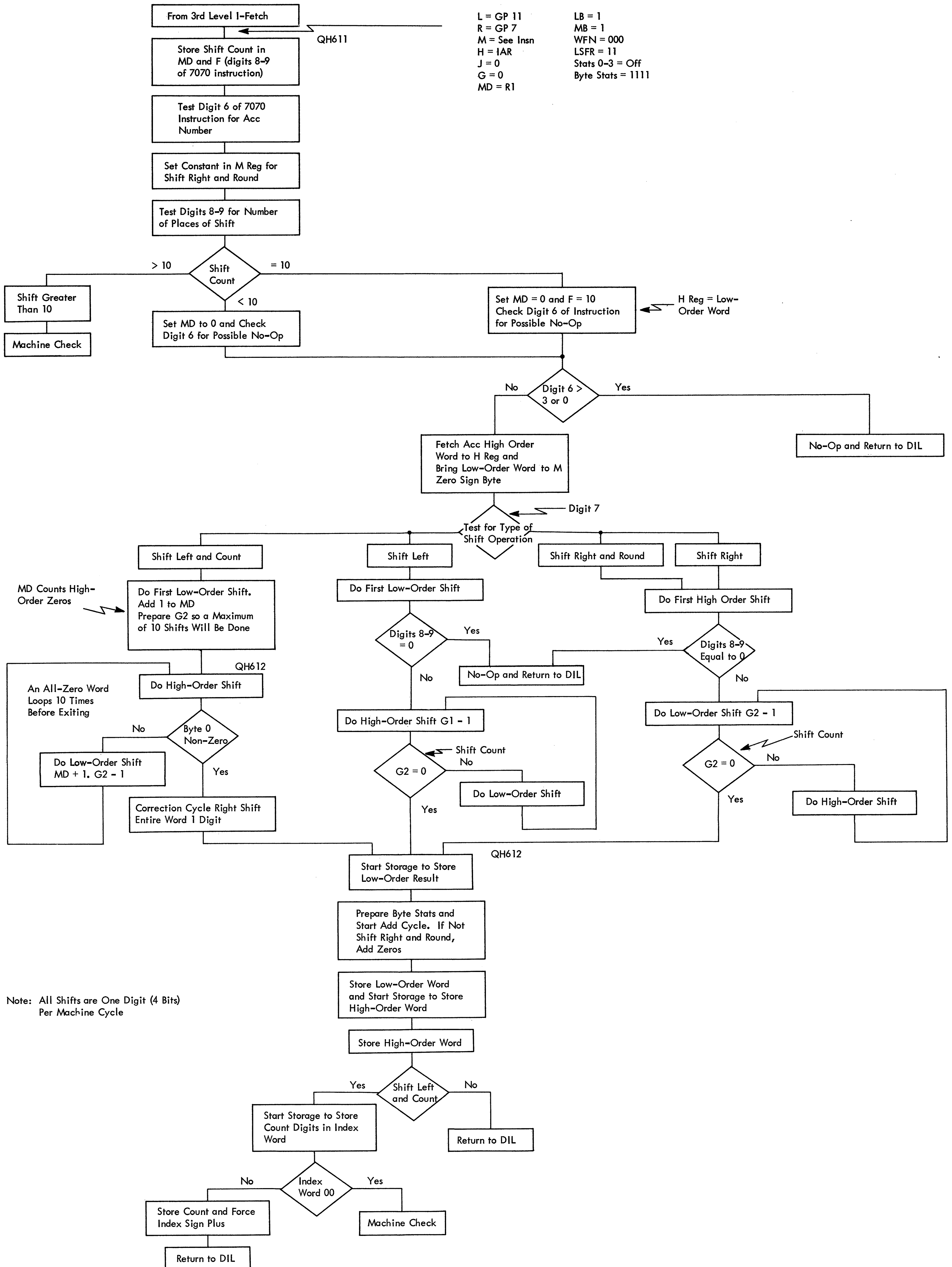
FIGURE CLF 800. BUFFER OPERATIONS -- LOAD BUFFER FROM ALPHA MODE AND UNLOAD BUFFER, DECOMPRESS NUMERIC DIGITS (SHEET 7 OF 8)



Stat	Meaning
0	Buffer End
1	-----
2	Mode (1 = alpha, 0 = numeric)
3	RDW match
4	00 = ELB 10 = ELBR
5	01 = ELBZ 11 = ELBC (For unload ops, stat 4 equals compressed word or TWE)
6	Buffer byte address
7	
R Sign	0 = EUB 1 = EUBR
L Sign	LLRR

Note: The numeric digit suffix inside all off-page connectors tells which of the eight sheets to come from or go to.

FIGURE CLF 800. BUFFER OPERATIONS -- LOAD BUFFER FROM NUMERIC WORD (SHEET 8 OF 8)



Note: All Shifts are One Digit (4 Bits) Per Machine Cycle

FIGURE CLF 802. SHIF CONTROL (ESC)

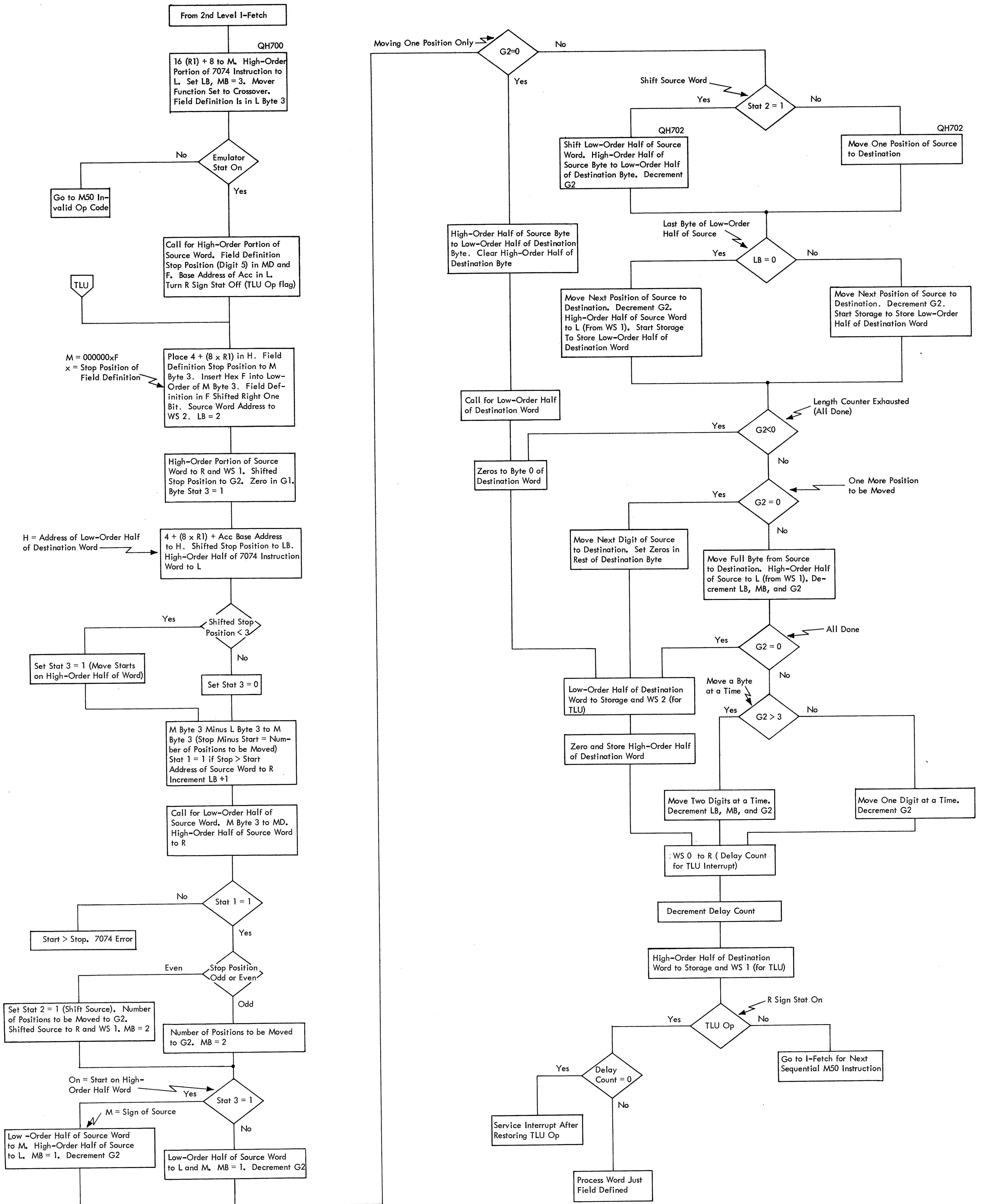
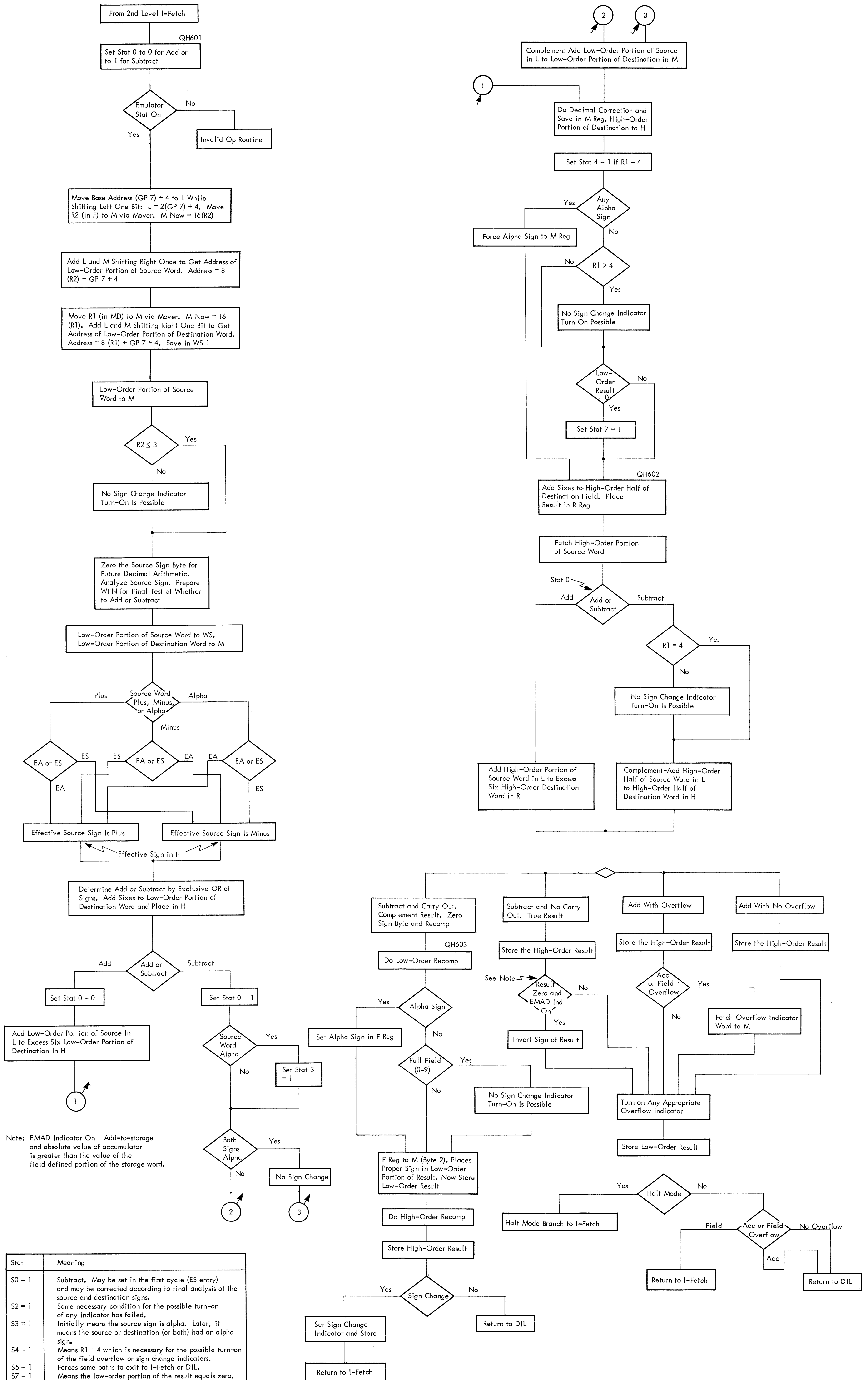


FIGURE CLF 804. FIELD DEFINITION (EFD)



Note: EMAD Indicator On = Add-to-storage and absolute value of accumulator is greater than the value of the field defined portion of the storage word.

Stat	Meaning
S0 = 1	Subtract. May be set in the first cycle (ES entry) and may be corrected according to final analysis of the source and destination signs.
S2 = 1	Some necessary condition for the possible turn-on of any indicator has failed.
S3 = 1	Initially means the source sign is alpha. Later, it means the source or destination (or both) had an alpha sign.
S4 = 1	Means R1 = 4 which is necessary for the possible turn-on of the field overflow or sign change indicators.
S5 = 1	Forces some paths to exit to I-Fetch or DIL.
S7 = 1	Means the low-order portion of the result equals zero.

FIGURE CLF 806. ADD/SUBTRACT (EA, ES)

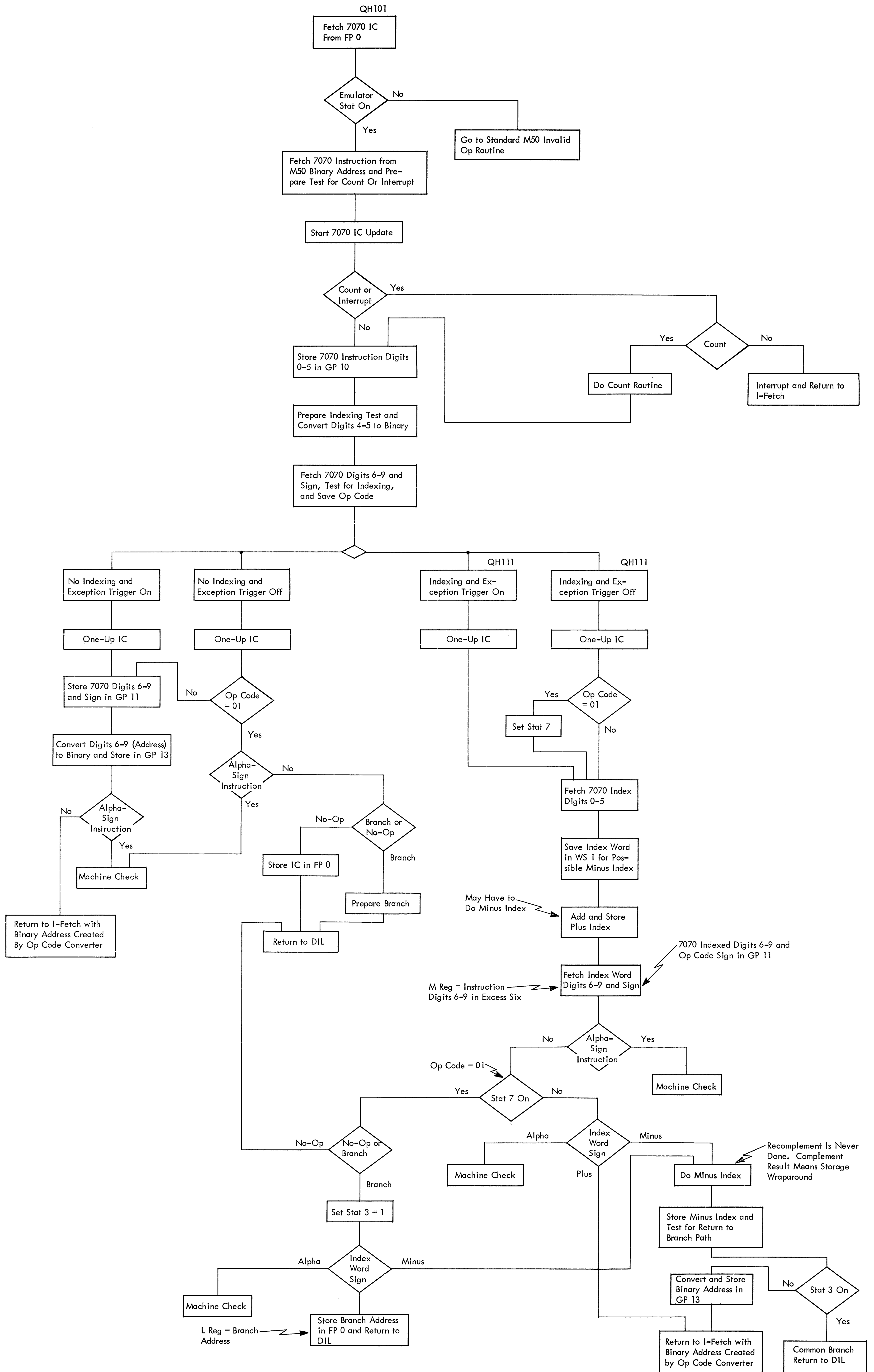
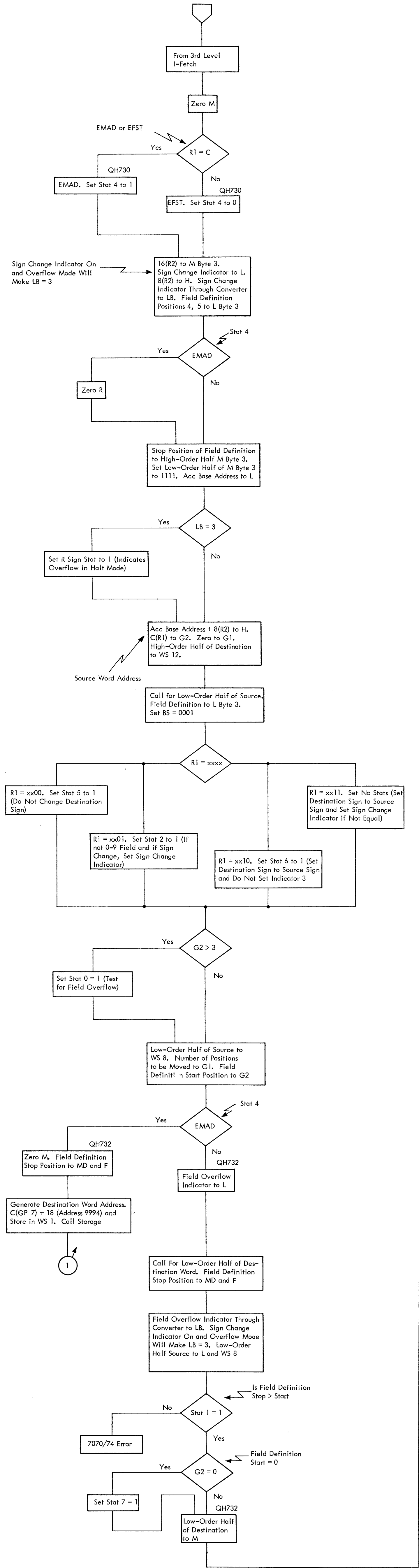


FIGURE CLF 808. DO INTERPRETIVE LOOP (DIL)



Stat	Usage
0	Test for field overflow.
1	Field definition stop position greater than the start position.
2	If sign change and not 0-9 field, set the sign change indicator.
3	Source byte not exhausted.
4	EMAD operation.
5	Inhibit sign change indicator turn-on.
6	Set the destination sign to the source sign but do not set the sign change indicator.
7	Field definition start position equal to zero.
G1	Number of positions to be moved.

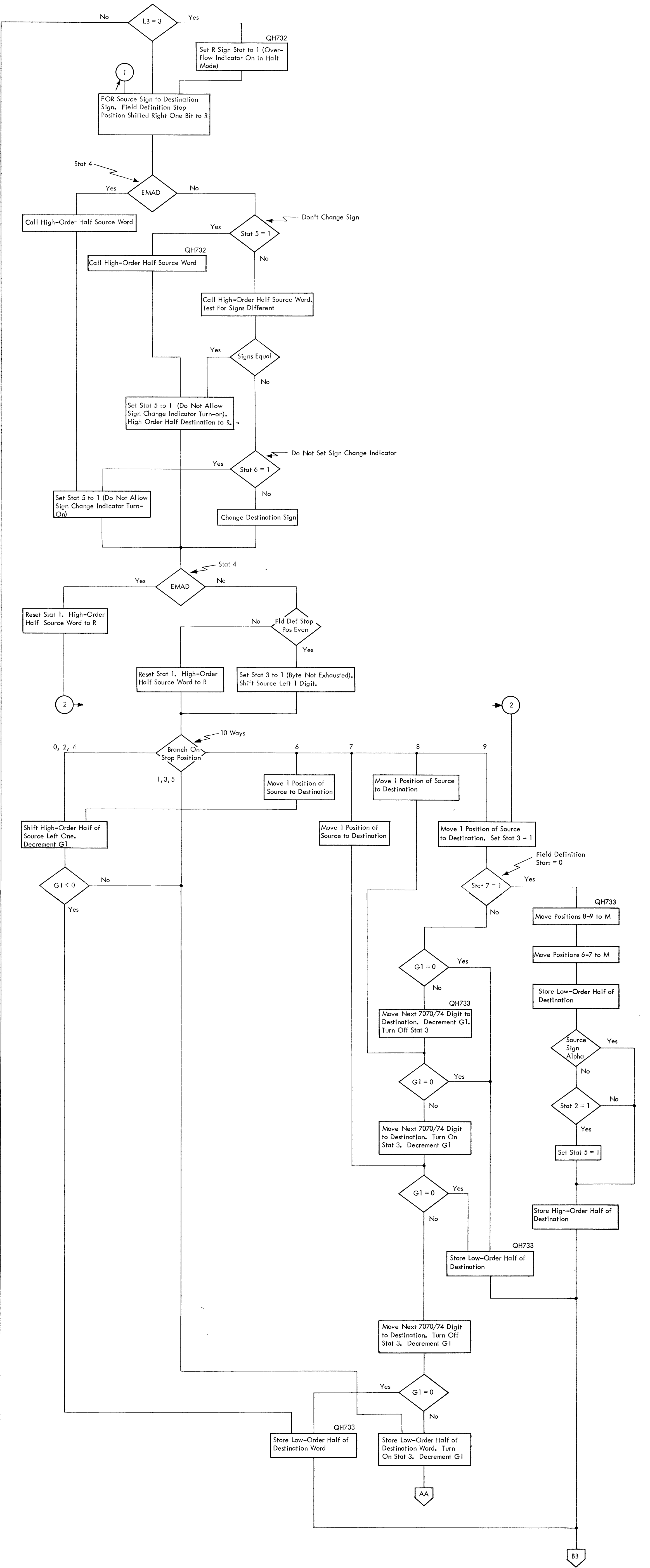


FIGURE CLF 810. FIELD STORE (EFST) AND MOVE ACCUMULATOR DIGITS (EMAD) (SHEET 1 OF 2)



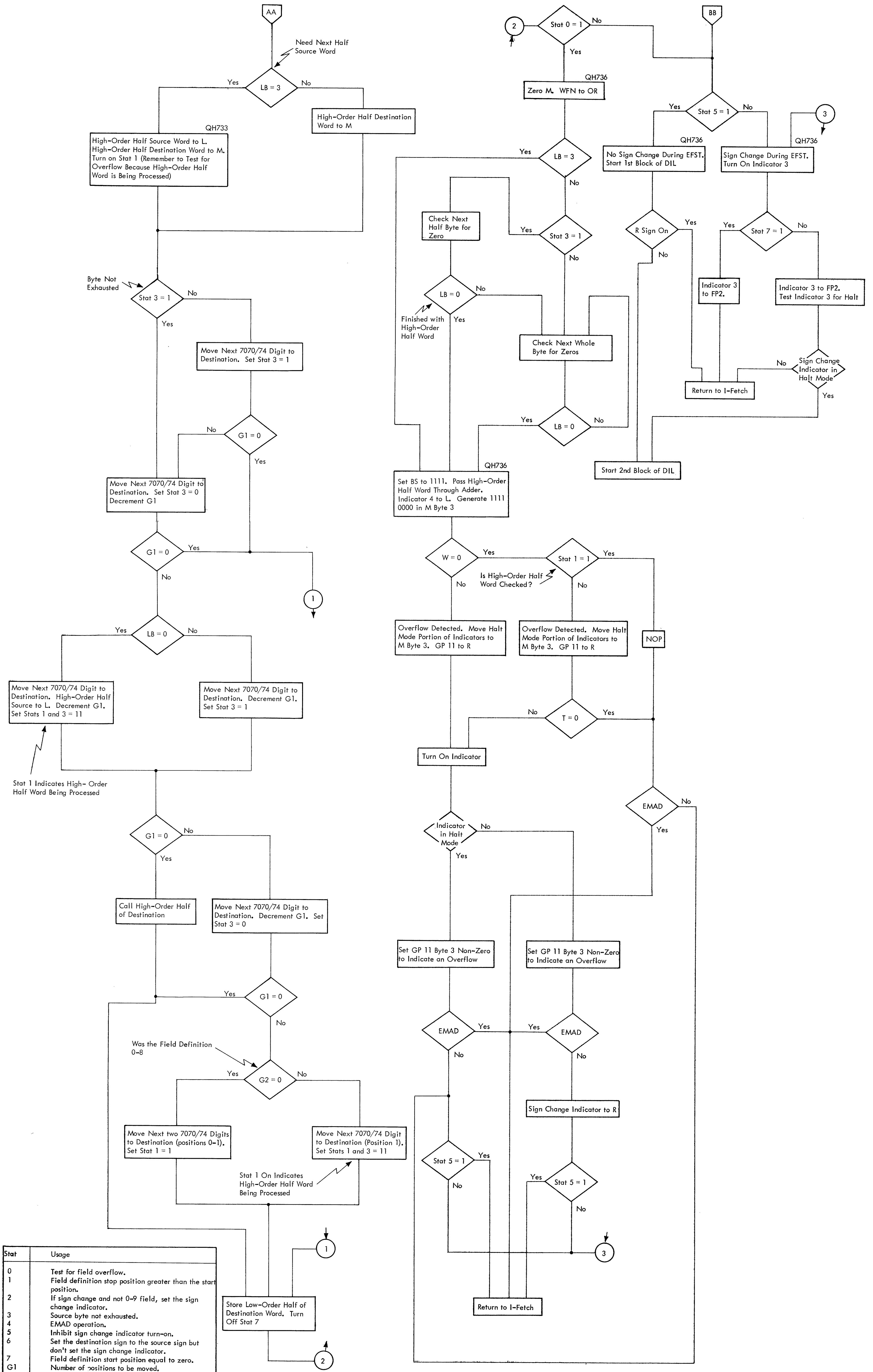


FIGURE CLF 810. FIELD STORE (EFST) AND MOVE ACCUMULATOR DIGITS (EMAD) (SHEET 2 OF 2)

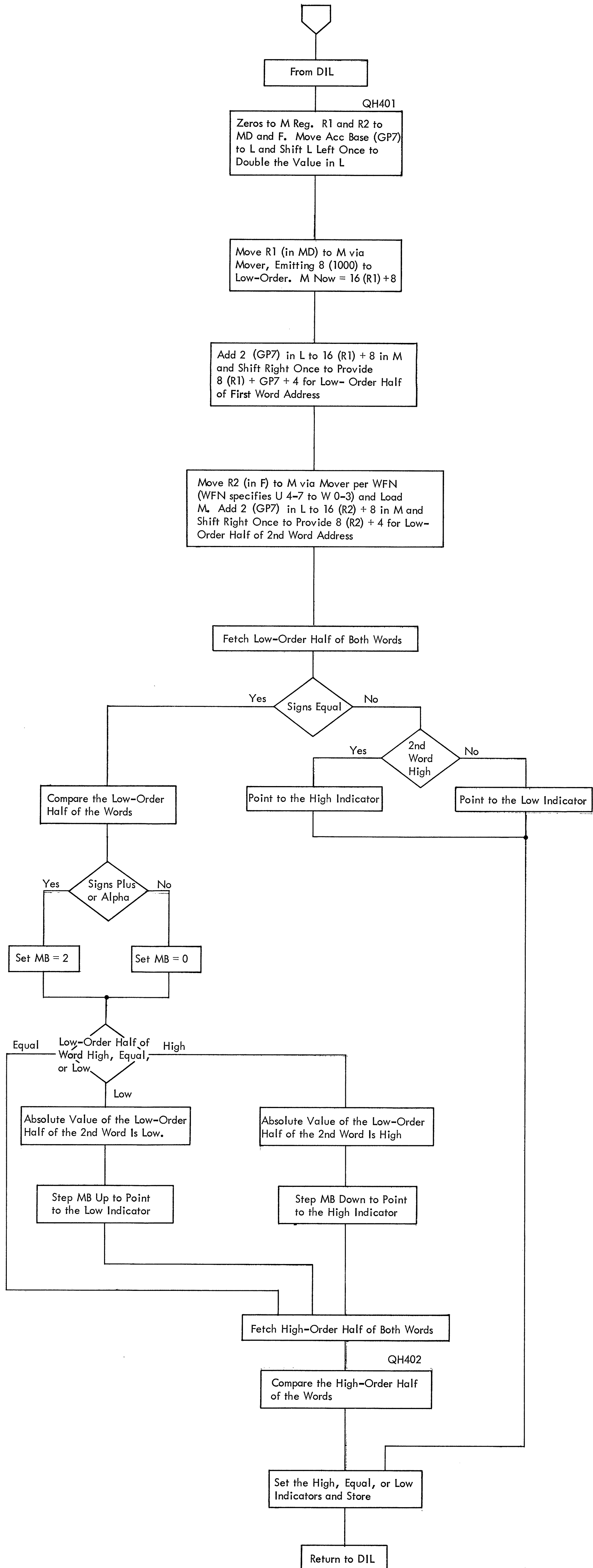


FIGURE CLF 812. COMPARE (EC)

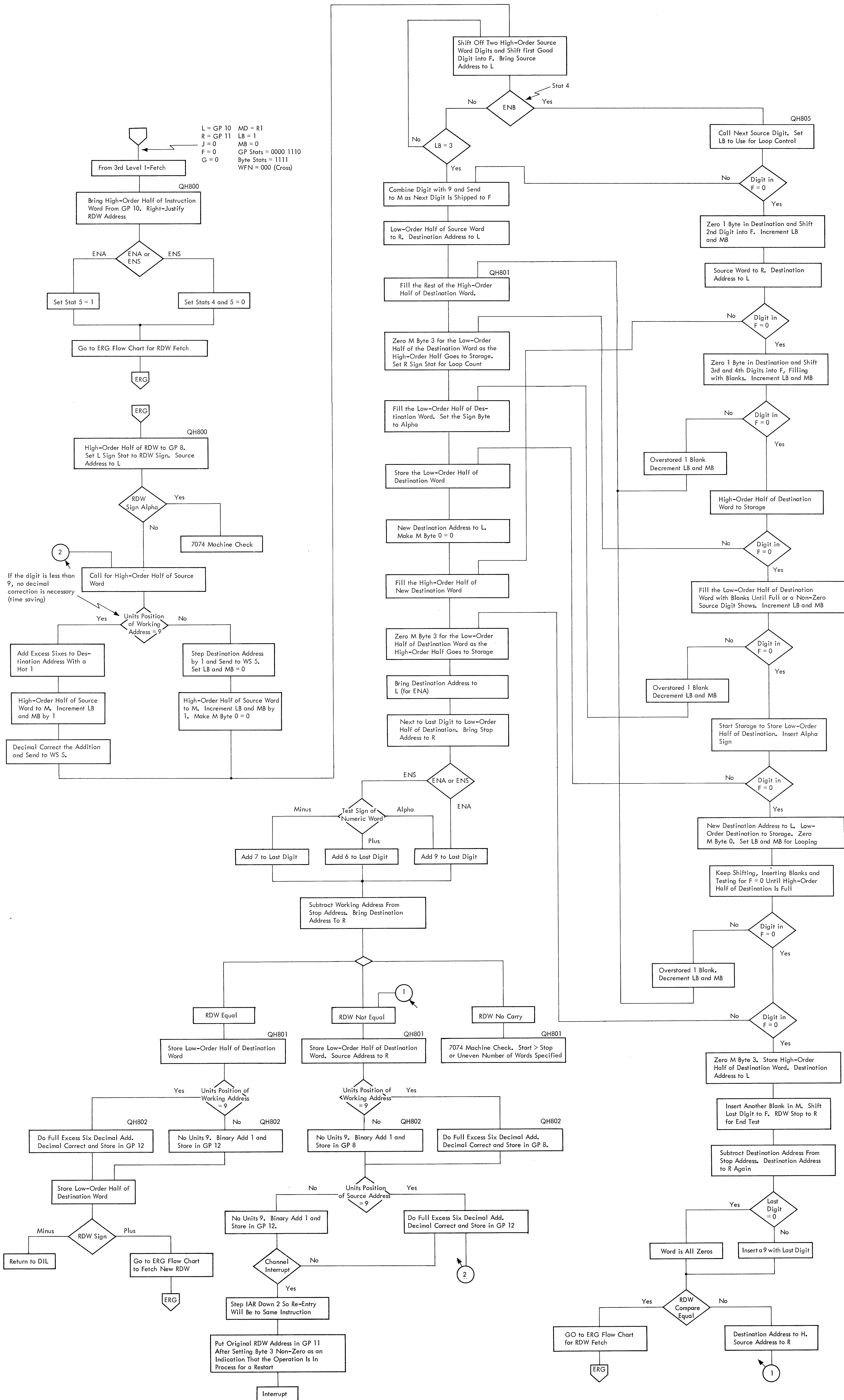


FIGURE CLF 814. EDIT NUMERIC TO ALPHA (ENA, ENS, ENB)

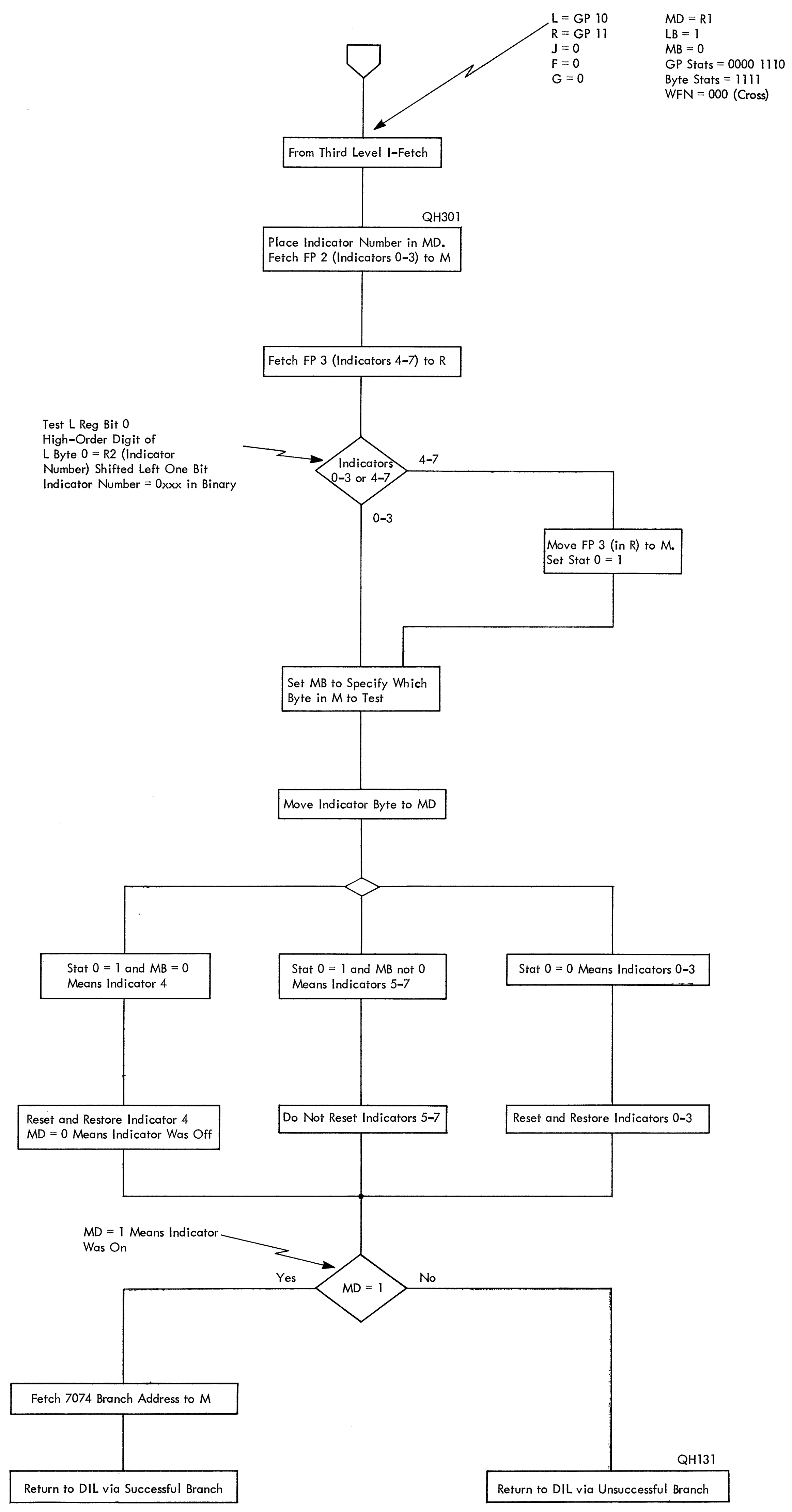


FIGURE CLF 816. BRANCH ON INDICATOR (EBI)

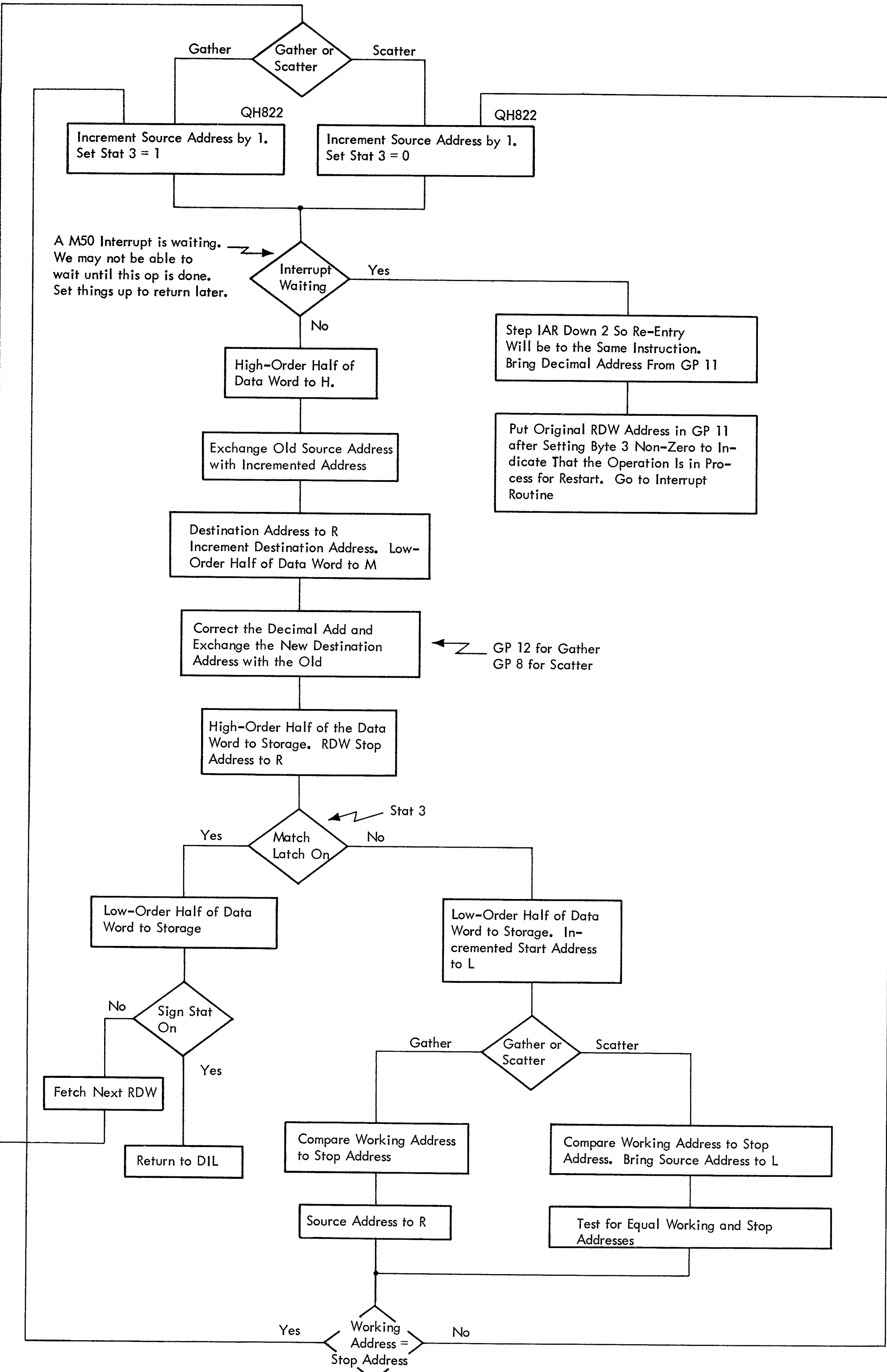
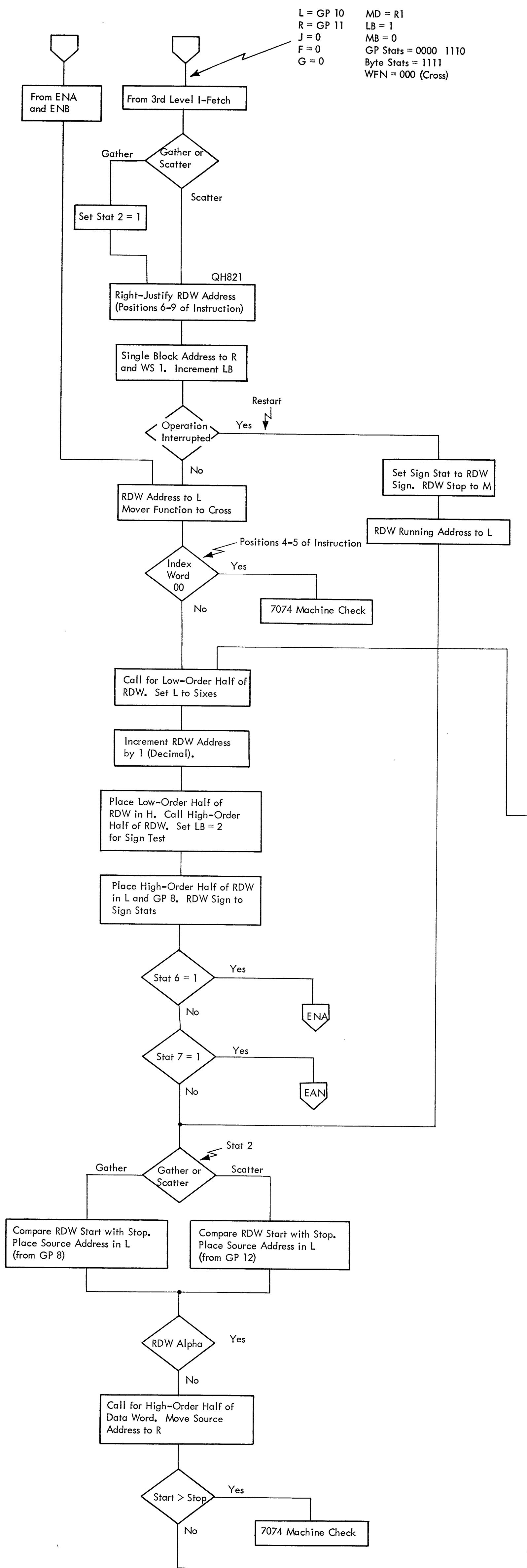


FIGURE CLF 818. RECORD GATHER/SCATTER (ERG, ERS)

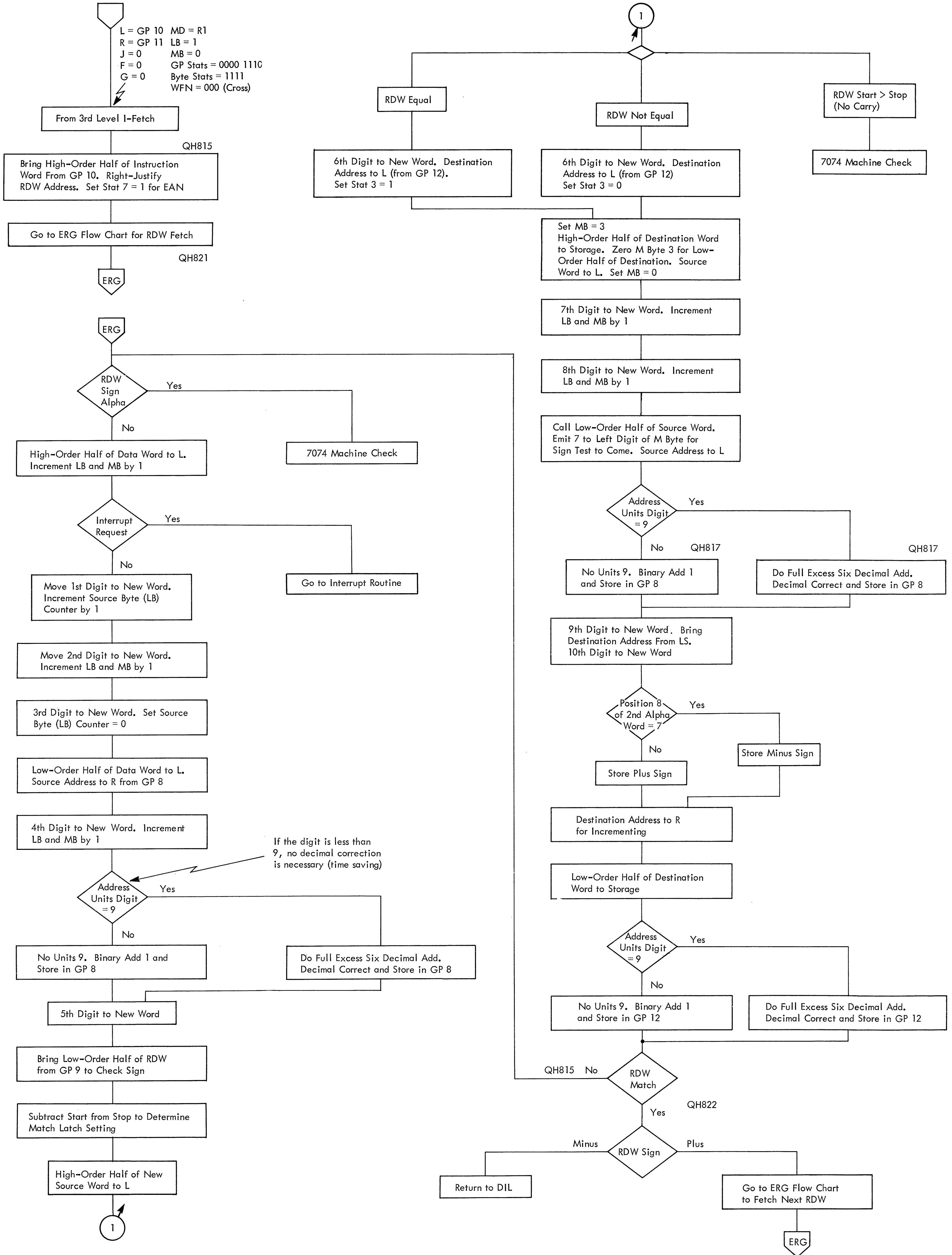
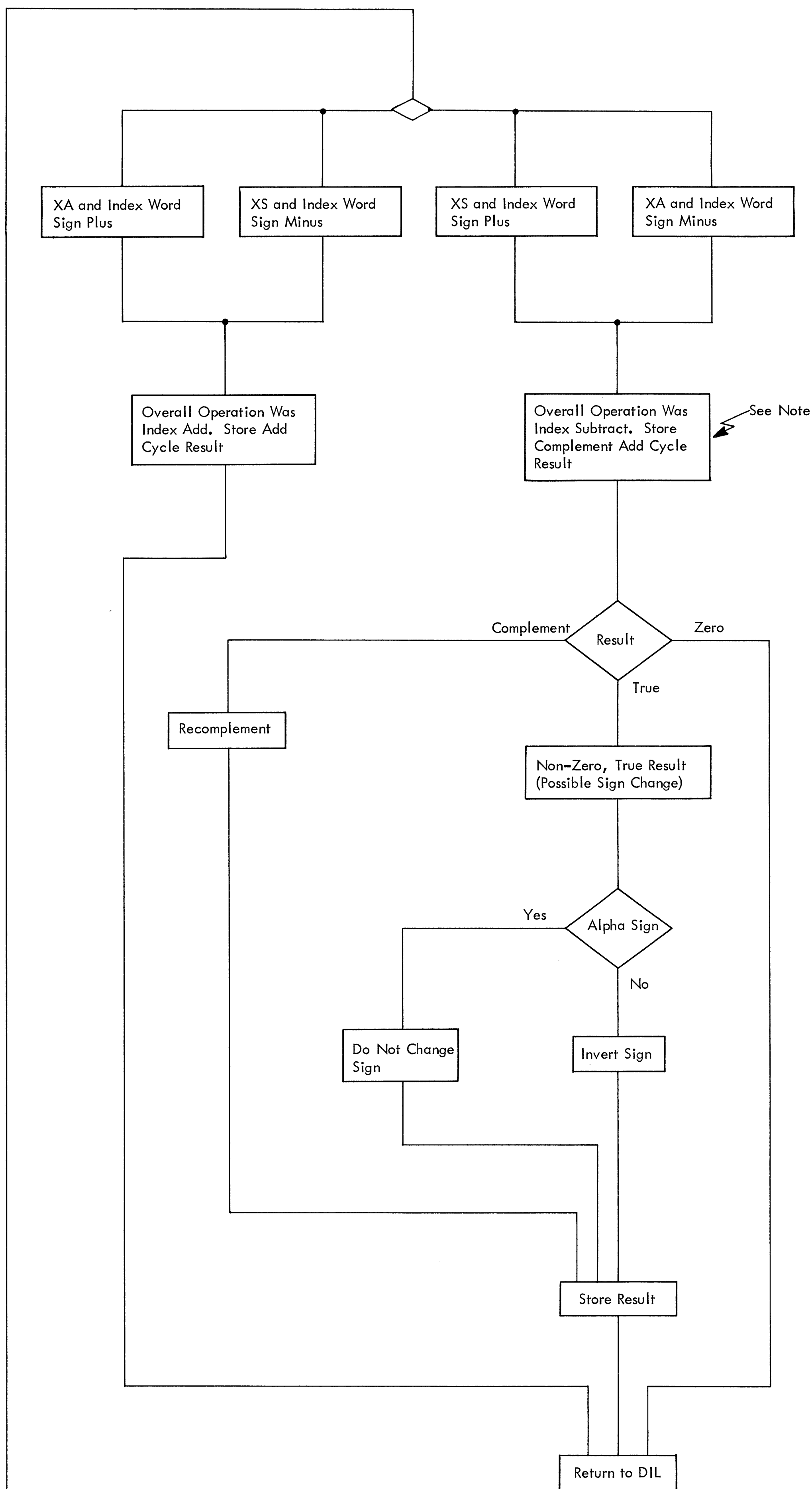
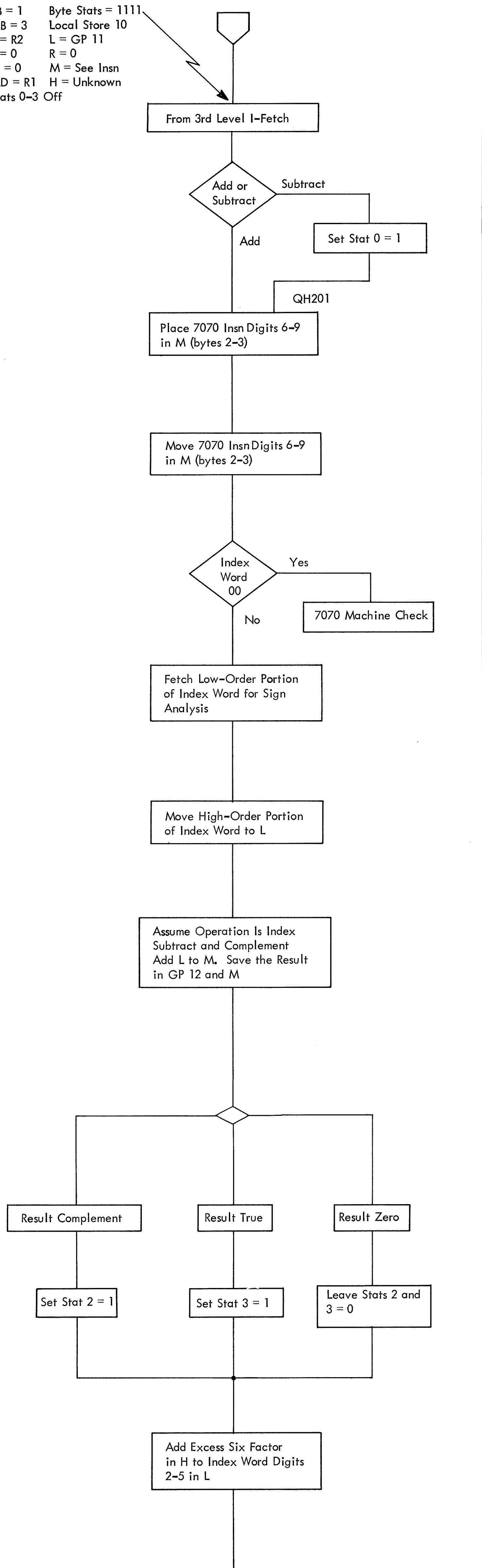


FIGURE CLF 820. EDIT ALPHA TO NUMERIC (EAN)

LB = 1 Byte Stats = 1111  
 MB = 3 Local Store 10  
 J = R2 L = GP 11  
 F = 0 R = 0  
 G = 0 M = See Insn  
 MD = R1 H = Unknown  
 Stats 0-3 Off



Note: The somewhat unusual sign manipulation is a result of the operands being reversed from the normal sense when the subtraction is done.

FIGURE CLF 822. INDEX WORD ADD/SUBTRACT (EXA, EXS)

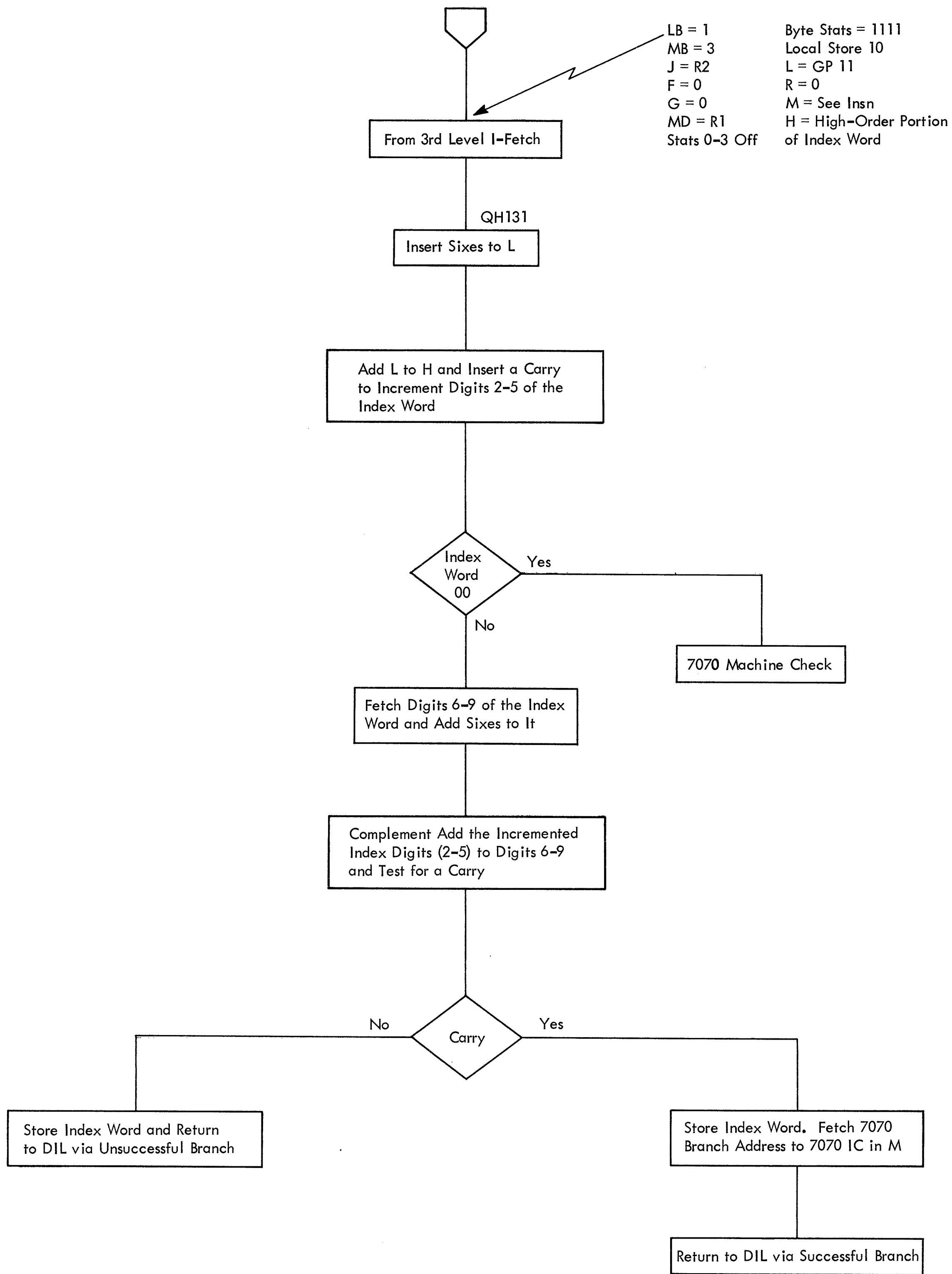


FIGURE CLF 824. BRANCH INCREMENTED INDEX WORD (EBIX)



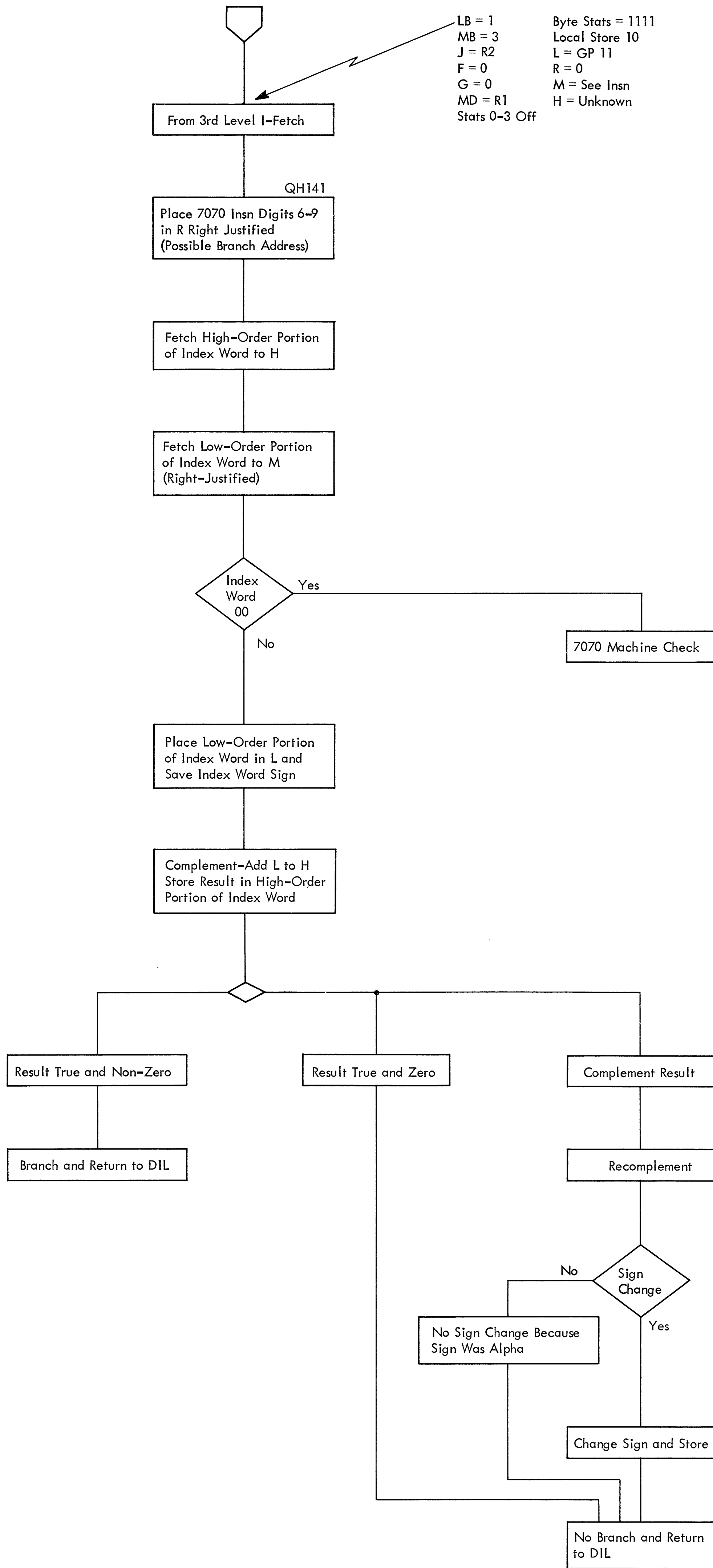


FIGURE CLF 826. BRANCH DECREMENTED INDEX WORD (EBDX)

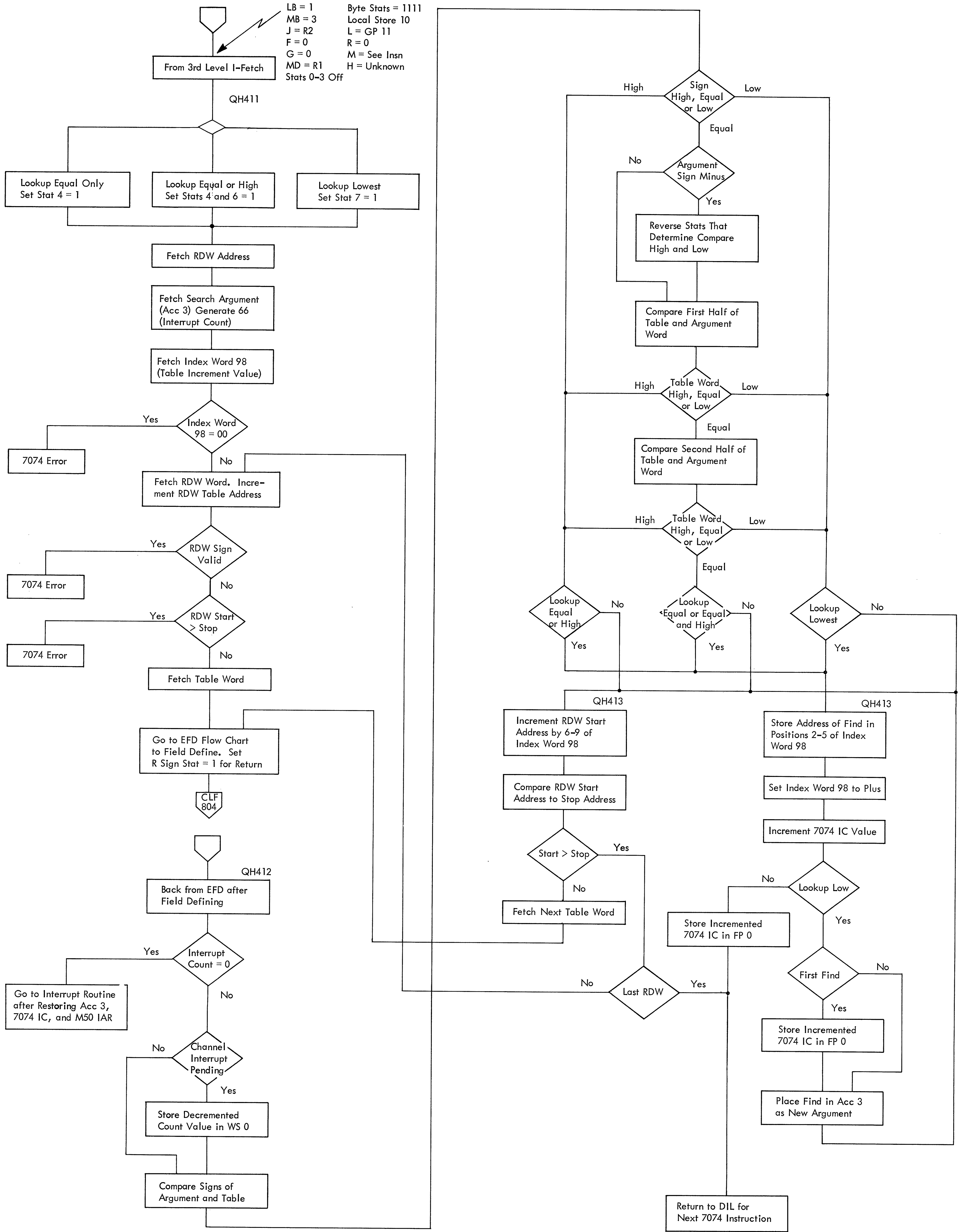
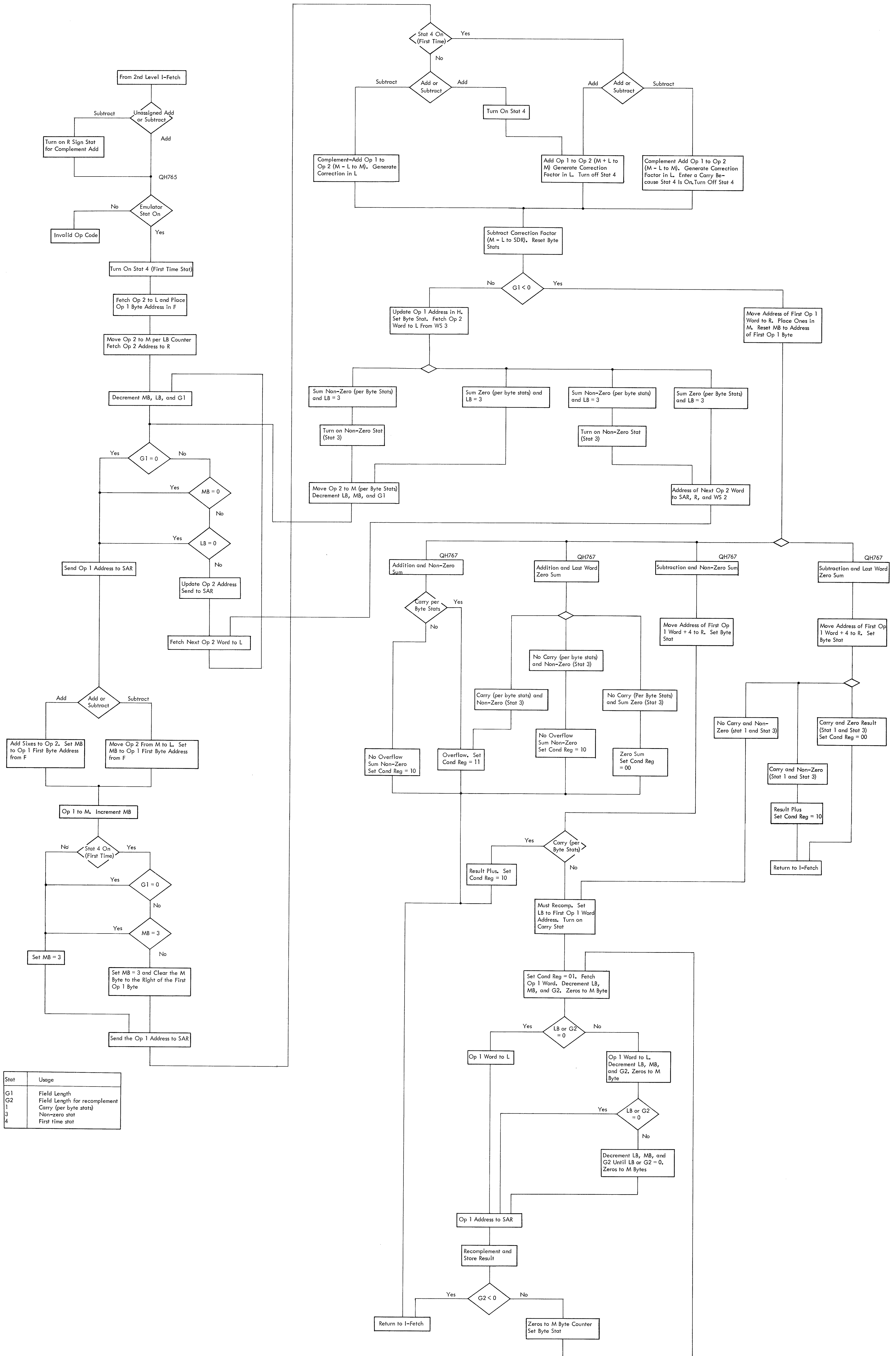


FIGURE CLF 828. TABLE LOOKUP OPERATIONS (ELE, ELEH, ELL)



Stat	Usage
G1	Field Length
G2	Field Length for recomplement
1	Carry (per byte stats)
3	Non-zero stat
4	First time stat

FIGURE CLF 830. UNSIGNED ADD/SUBTRACT (EUNA, EUNS)

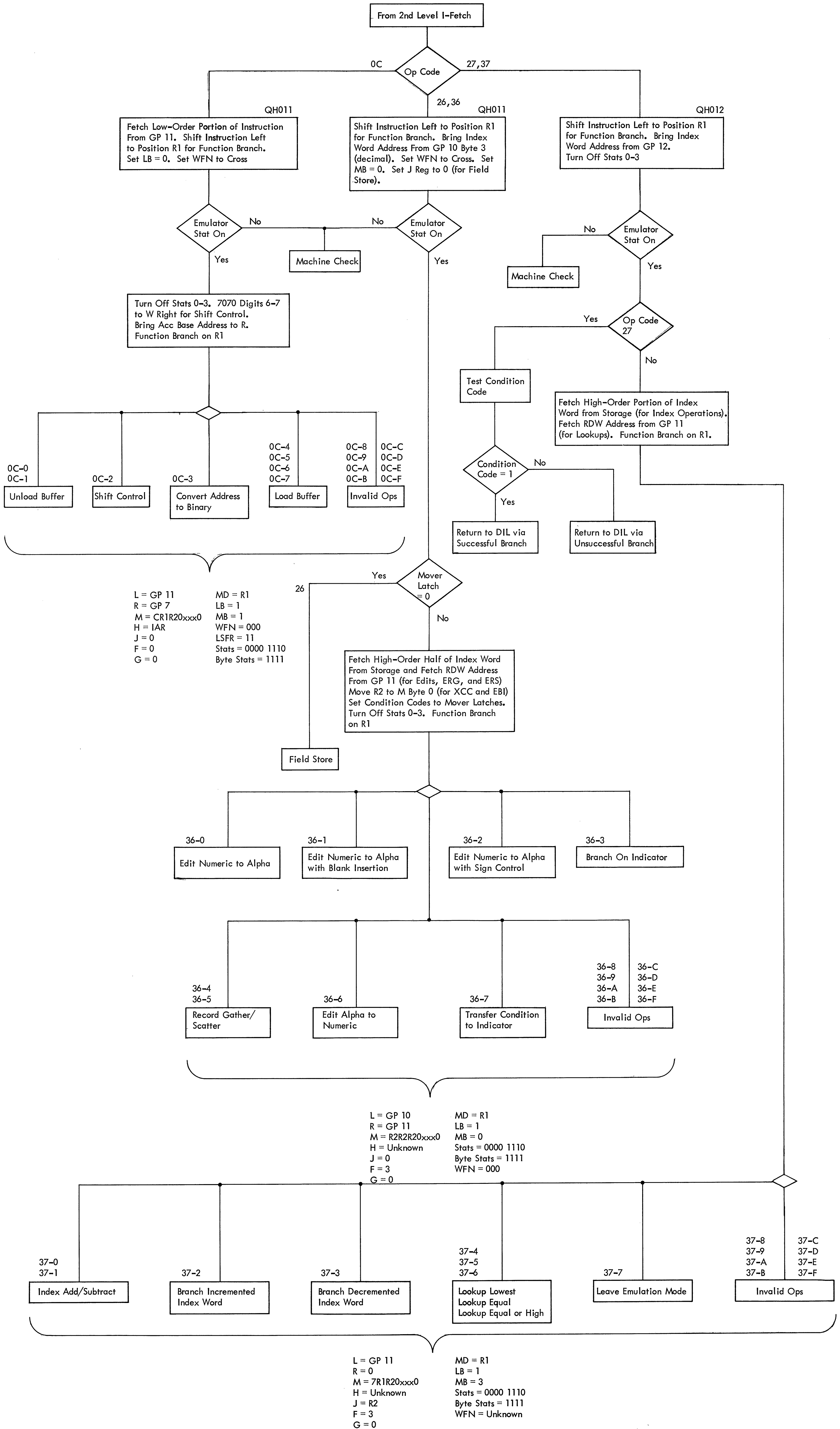
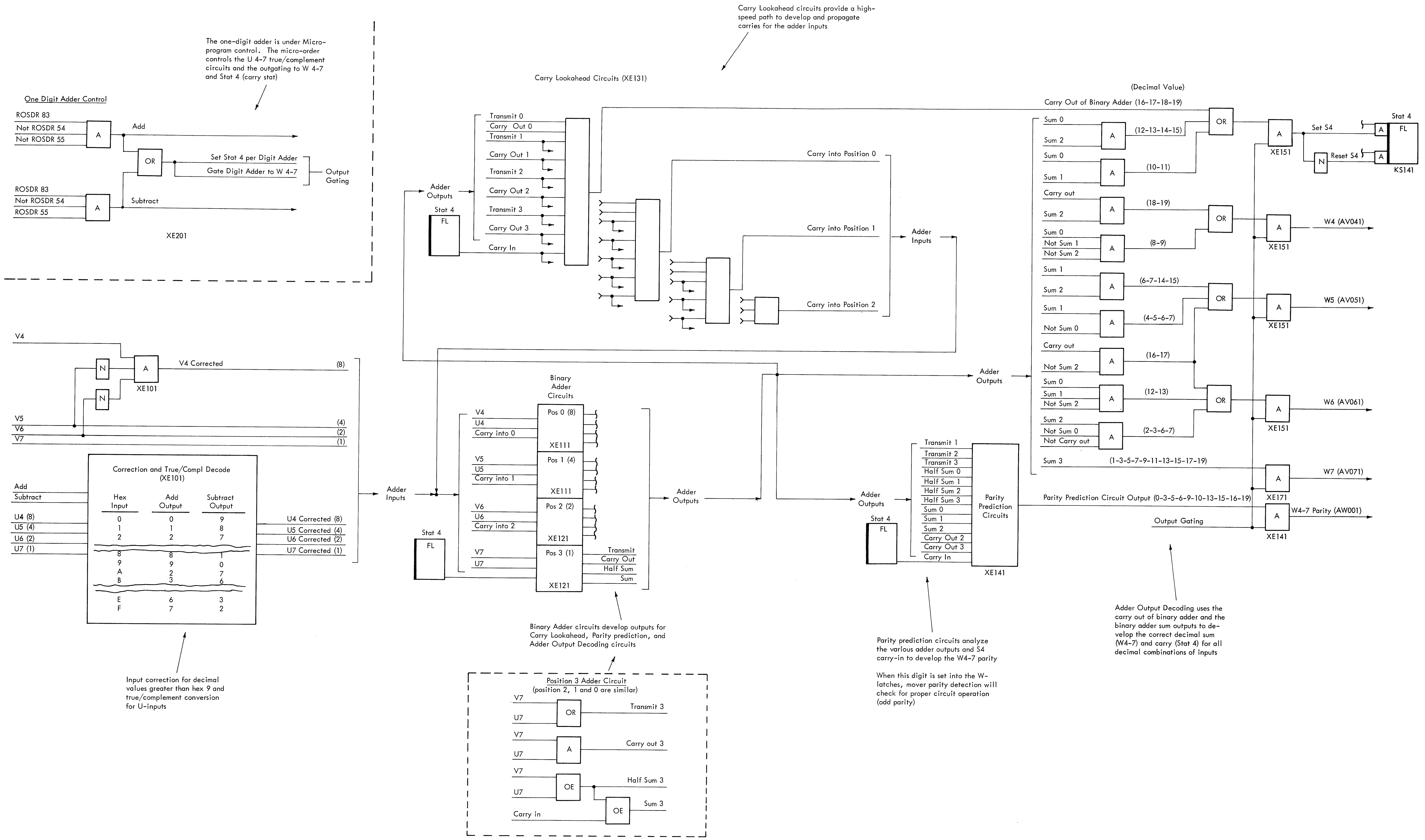


FIGURE CLF 832. THIRD LEVEL I-FETCH



The one-digit adder is under Micro-program control. The micro-order controls the U 4-7 true/complement circuits and the outgating to W 4-7 and Stat 4 (carry stat)

Carry Lookahead circuits provide a high-speed path to develop and propagate carries for the adder inputs

Binary Adder circuits develop outputs for Carry Lookahead, Parity prediction, and Adder Output Decoding circuits

Parity prediction circuits analyze the various adder outputs and S4 carry-in to develop the W4-7 parity

Adder Output Decoding uses the carry out of binary adder and the binary adder sum outputs to develop the correct decimal sum (W4-7) and carry (Stat 4) for all decimal combinations of inputs

Input correction for decimal values greater than hex 9 and true/complement conversion for U-inputs

When this digit is set into the W-latches, mover parity detection will check for proper circuit operation (odd parity)

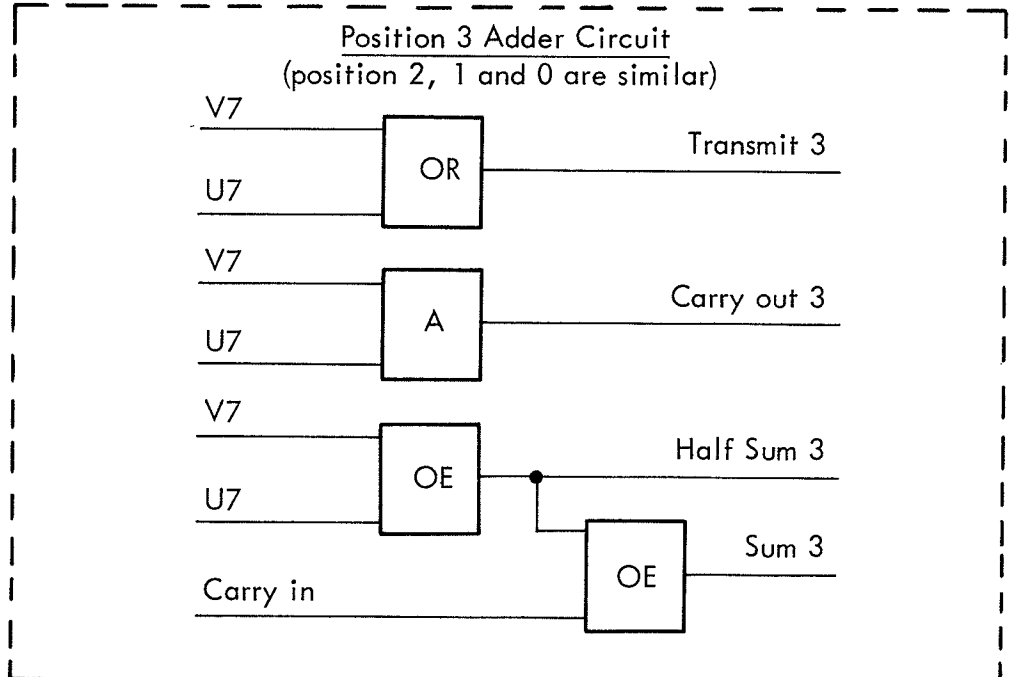


FIGURE UDC 900. ONE DIGIT ADDER

Function	Location		
	Channel 1	Channel 2	Channel 3
<u>TRANSLATE</u>			
File Latch } Load Latch } Odd Latch }	XE501	XE511	XE511
CAS Control	QR920	QR920	QR920
Translate Latch	XE521	XE521	XE521
CAS Control	QV103	QV103	QV103
<u>WM INSERT/DELETE</u>			
WS Control	XE621	-----XE801-----	*
<u>WM PRESERVATION</u>			
Sel Ch Read Store Routine		----- QR860 and QV105-----	
WM Stat Latch		-----XE401-----	
Split R/W Latch		-----KC511-----	
<u>INTERFACE LINES</u>			
(to the Sel Ch)			
Bus In Gating			
Bits			
P	XE561	-----XE741-----	} *
0-1	XE531	-----XE711-----	
2-3	XE541	-----XE721-----	
4-5-6-7	XE551	-----XE731-----	
Special Char Detection	XE571	-----XE751-----	
Service In	XE631	-----XE811-----	
(to the Interface Lines)			
Bus Out Gating			
Bits			
P-0	XE581	-----XE761-----	} *
1-2-3	XE591	-----XE771-----	
4-5-6-7	XE601	-----XE781-----	
Special Char Detection	XE611	-----XE791-----	
Service Out	XE621	-----XE801-----	

\* Selector channel 2 and 3 use ALD pages XE701 to XE841. They each have identical card and pin locations

The 'psuedo-location' shown in line 5 of the ALD logic block (gate-board-card) is Y-P4xx, and calls attention to the note that specifies the actual location for each channel

The note points out that the gate and board locations are:

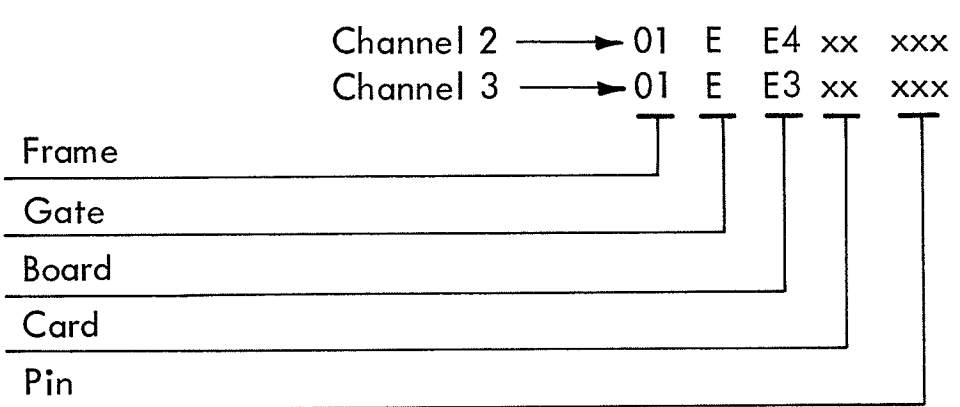


FIGURE IOP 900. 1410 I/O OPERATIONS - ALD/CAS LOCATIONS

	CAW Control			Table	Translation		Wordmark Considerations	
	Bit 7	Bit 6	Bit 4		(General Rule) Interface Code → EBCDIC II	Special Character Exceptions		
Read (Bus-in Lines Translation)	Tape	Move	Odd	1	00xx xxxx → 00xx xxxx 10xx xxxx → 01xx xxxx (IF bit one must be zero)	Yes	CCW 39 equal to a 1-bit activates the microprogramming during the sel ch read store routine, so that the wordmarks in 1410 core storage are preserved as the I/O byte is read into bits 1-7 of each location	
	Tape	Move	Even	1	01xx xxxx → 00xx xxxx 11xx xxxx → 01xx xxxx (IF bit one must be one)	Yes		
	Disk	Move	Even	1	01xx xxxx → 00xx xxxx 11xx xxxx → 01xx xxxx (IF bit one must be one)	Yes		
	Tape	Load	Odd	1	00xx xxxx → ?0xx xxxx 10xx xxxx → ?1xx xxxx (IF bit one must be zero)	Yes		Wordmark insert/delete circuits are active and block word separator characters on the bus in lines and insert bit zero on the next character (unless the 2nd character is also a word separator character)
	Tape	Load	Even	1	01xx xxxx → ?0xx xxxx 11xx xxxx → ?0xx xxxx (IF bit one must be one)	Yes		
	Disk	Load	Even	No	xx00 xxxx → xx11 xxxx xx01 xxxx → xx10 xxxx xx10 xxxx → xx01 xxxx xx11 xxxx → xx00 xxxx (IF bits 2 and 3 are inverted)	No		
Write (Bus-out Lines Translation)					EBCDIC II → Interface Code			
	Tape	Move	Odd	2	?0xx xxxx → 00xx xxxx ?1xx xxxx → 10xx xxxx	Yes	The EBCDIC II wordmark bit (bit zero) does not affect the translation	
	Tape	Move	Even	3	?0xx xxxx → 01xx xxxx ?1xx xxxx → 10xx xxxx	Yes		
	Disk	Move	Even	4	?0xx xxxx → 01xx xxxx ?1xx xxxx → 11xx xxxx	Yes		
	Tape	Load	Odd	2	?0xx xxxx → 00xx xxxx ?1xx xxxx → 10xx xxxx	Yes	Word separator characters are generated and precede each wordmarked character or a word separator character from core storage out to the interface bus out lines	
	Tape	Load	Even	3	?0xx xxxx → 01xx xxxx ?1xx xxxx → 11xx xxxx	Yes		
Disk	Load	Even	No	xx00 xxxx → xx11 xxxx xx01 xxxx → xx10 xxxx xx10 xxxx → xx01 xxxx xx11 xxxx → xx00 xxxx (EBCDIC II bits 2 and 3 are inverted)				

Table 1 Read (IF Bus In to EBCDIC II) Translation

	If Bus In Code			0-3															
	4-7	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F		
0	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	70		
1	01	11	61	31	01	11	61	31	41	51	61	71	41	51	61	71	71		
2	02	00	10	20	30	00	10	20	42	52	62	72	42	52	62	72	72		
3	03	11	23	33	03	13	23	33	43	53	63	73	43	53	63	73	73		
4	04	14	24	34	04	14	24	34	44	54	64	74	44	54	64	74	74		
5	05	15	25	35	05	15	25	35	45	55	65	75	45	55	65	75	75		
6	06	16	26	36	06	16	26	36	46	56	66	76	46	56	66	76	76		
7	07	17	27	37	07	17	27	37	47	57	67	77	47	57	67	77	77		
8	08	00	10	20	30	00	10	20	48	58	68	78	48	58	68	78	78		
9	09	19	29	39	09	19	29	39	49	59	69	79	49	59	69	79	79		
A	0A	0A	1B	2B	3B	0A	1B	2B	4A	5A	6A	7A	4A	5A	6A	7A	7A		
B	0B	1B	2B	3B	0B	1B	2B	3B	4B	5B	6B	7B	4B	5B	6B	7B	7B		
C	0C	1C	2C	3C	0C	1C	2C	3C	4C	5C	6C	7C	4C	5C	6C	7C	7C		
D	0D	1D	2D	3D	0D	1D	2D	3D	4D	5D	6D	7D	4D	5D	6D	7D	7D		
E	0E	1E	2E	3E	0E	1E	2E	3E	4E	5E	6E	7E	4E	5E	6E	7E	7E		
F	0F	1F	2F	3F	0F	1F	2F	3F	4F	5F	6F	7F	4F	5F	6F	7F	7F		

Table bytes are identified by dotted, striped or blank boxes. These serve to identify the translator outputs that are invalid parity and result in Channel Data Check during various types of 1410 I/O translations

Operation	Invalid Parity
tape-move-odd	no pattern
tape-move-even	striped or dotted pattern
disk-move-even	striped pattern
tape-load-odd	no pattern
tape-load-even	striped or dotted pattern
disk-load-even	(all bytes have correct parity)

Word Separator for tape-load-odd is hex 6D; for tape-load-even it is hex 2D

Table 2 Write Translation (tape-move/load-odd)

	EBCDIC II			0-3						
	4-7	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
0	00	10	20	3A	00	80	90	A0	B0	
1	01	11	21	31	81	91	21	B1		
2	02	12	22	3A	02	82	92	A2	B2	
3	03	13	23	33	83	93	A3	B3		
4	04	14	24	34	84	94	A4	B4		
5	05	15	25	35	85	95	A5	B5		
6	06	16	26	36	86	96	A6	B6		
7	07	17	27	37	87	97	A7	B7		
8	08	18	28	3A	08	88	98	A8	B8	
9	09	19	29	39	89	99	A9	B9		
A	0A	1A	2A	3A	0A	8A	9A	AA	BA	
B	0B	1B	2B	3B	8B	9B	AB	BB		
C	0C	1C	2C	3C	8C	9C	AC	BC		
D	0D	1D	2D	3D	8D	9D	AD	BD		
E	0E	1E	2E	3E	8E	9E	AE	BE		
F	0F	1F	2F	3F	8F	9F	AF	BF		

\* EBCDIC II codes 21, 2A, A1, and AA cause unit check because of a bad parity translator output  
EBCDIC II codes 2D, or AD are the word separator for tape-load write operations

Table 3 Write Translation (tape-move/load-even)

	EBCDIC II			0-3						
	4-7	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
0	00	50	60	40	C0	D0	E0	F0		
1	01	41	51	61	71	C1	D1	E1	F1	
2	02	52	62	42	C2	D2	E2	F2		
3	03	43	53	63	73	C3	D3	E3	F3	
4	04	44	54	64	74	C4	D4	E4	F4	
5	05	45	55	65	75	C5	D5	E5	F5	
6	06	46	56	66	76	C6	D6	E6	F6	
7	07	47	57	67	77	C7	D7	E7	F7	
8	08	58	68	48	C8	D8	E8	F8		
9	09	49	59	69	79	C9	D9	E9	F9	
A	0A	5A	6A	4A	CA	DA	EA	FA		
B	0B	4B	5B	6B	7B	CB	DB	EB	FB	
C	0C	4C	5C	6C	7C	CC	DC	EC	FC	
D	0D	4D	5D	6D	7D	CD	DD	ED	FD	
E	0E	4E	5E	6E	7E	CE	DE	EE	FE	
F	0F	4F	5F	6F	7F	CF	DF	EF	FF	

\* EBCDIC II codes 21 or A1 cause unit check because of a bad parity translator output  
EBCDIC II codes 2D or AD are the word separator for tape-load write operations

Table 4 Write Translation (disk-move-even)

	EBCDIC II			0-3						
	4-7	0/8	1/9	2/A	3/B	4/C	5/D	6/E	7/F	
0	00	50	60	7A	40	C0	D0	E0	F0	
1	01	41	51	61	71	C1	D1	E1	F1	
2	02	52	62	7A	42	C2	D2	E2	F2	
3	03	43	53	63	73	C3	D3	E3	F3	
4	04	44	54	64	74	C4	D4	E4	F4	
5	05	45	55	65	75	C5	D5	E5	F5	
6	06	46	56	66	76	C6	D6	E6	F6	
7	07	47	57	67	77	C7	D7	E7	F7	
8	08	58	68	7A	48	C8	D8	E8	F8	
9	09	49	59	69	79	C9	D9	E9	F9	
A	0A	5A	6A	7A	4A	CA	DA	EA	FA	
B	0B	4B	5B	6B	7B	CB	DB	EB	FB	
C	0C	4C	5C	6C	7C	CC	DC	EC	FC	
D	0D	4D	5D	6D	7D	CD	DD	ED	FD	
E	0E	4E	5E	6E	7E	CE	DE	EE	FE	
F	0F	4F	5F	6F	7F	CF	DF	EF	FF	

\* EBCDIC II codes 21, A1, 22, A2, 2B, or A8 cause unit check because of a bad parity translator output

FIGURE IOP 901. SELECTOR CHANNEL TRANSLATION FOR 1410 I/O OPERATIONS

Name	1410/7010 Graphic	EBCDIC II Code	Length	Hex ID for Fn Br to Execute	First Execute Page	After I-Fetch			
						Gen Purpose Stats 0-7	A Address	B Address	d Modifier
No Operation	N	D5	any	—	—	—	—	—	—
Add	A	C1	1, 6, 11 <sup>2</sup>	7	QR210	0000 ?001 (not Chained)	R-reg (GPR 6)	GPR 7	(None)
Subtract	S	E2	1, 6, 11 <sup>2</sup>	8	210				
Zero and Add	?	C0	1, 6, 11 <sup>2</sup>	5	250				
Zero and Subtract	!	D0	1, 6, 11 <sup>2</sup>	9	250				
Multiply	@	BC	1, 6, 11 <sup>2</sup>	2	300				
Divide	%	AC	1, 6, 11 <sup>2</sup>	0	335				
Compare	C	C3	1, 6, 11 <sup>2</sup>	4	510				
Set Wordmark	,	AB	1, 6, 11 <sup>2</sup>	3	375				
Clear Wordmark	≡	8C	1, 6, 11 <sup>2</sup>	1	375				
Clear Storage/Clear Storage and Branch	/	E1	1, 6, 11 <sup>2</sup>	D	361				
Edit	E	C6	1, 6, 11 <sup>2</sup>	6	180	0000 ?000 (BAR Chained)	R-reg (GPR 6)	GPR 7	(None)
Zero Suppress	Z	E9	1, 6, 11 <sup>2</sup>	8	180				
Branch if Character Equal	B	C2	1, 6, 11 <sup>2</sup>	3	QR545				
Branch if Bit Equal	W	E6	1, 6, 11 <sup>2</sup>	B	555				
Branch if WM and/or Zone Equal	V	E5	1, 6, 11 <sup>2</sup>	9	565				
Branch on C-bit	≡	E0	1, 6, 11 <sup>2</sup>	F	560				
Table Lookup	T	E3	1, 6, 11 <sup>2</sup>	7	510				
Move Data	D	C4	1, 6, 11 <sup>2</sup>	5	610				
Test and Branch	J	D1	1, 7 <sup>2</sup>	D	QR573				
Branch on Channel 1 Status	R	D9	7 <sup>2</sup>	8	593				
Branch on Channel 2 Status	X	E7	7 <sup>2</sup>	A	593				
Branch on Channel 3 Status	3	F3	7 <sup>2</sup>	C	593				
Priority Test and Branch	Y	E8	1, 7	6	582				
Store Address Register	G	C7	7	4	385				
Store or Restore Status	\$	9B	1, 7	2	405				
Halt/Halt and Branch	.	8B	1, 6	1	—	1xxx xxxx1	R-reg (GPR 6)	(None)	(None)
Read or Write without Wordmark	M	D4	10	1	QR800	0111 ?001	L-reg 8-31 (X Ch Field)	GPR 7	M-reg 0-7 (GPR 4 0-7)
Read or Write with Wordmark	L	D3	10	0	800				
Unit Control	U	E4	5	—	800	0111 0101	(None)	(None)	(None)
Stacker Select and Feed	K	D2	2	—	850	0000 0000	(None)	(None)	(None)
Carriage Control	F	C6	2	—	850	0100 0000	(None)	(None)	(None)

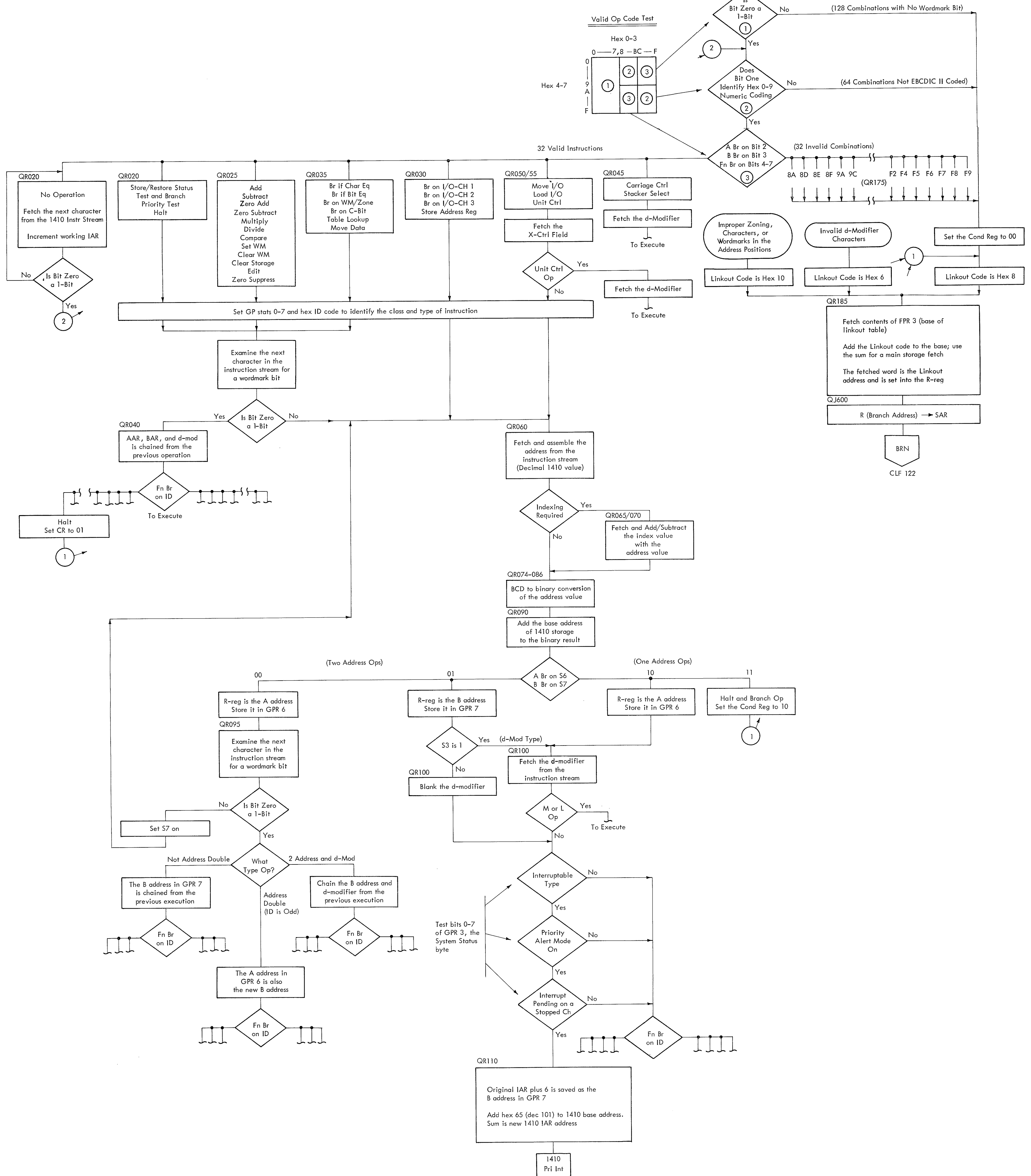
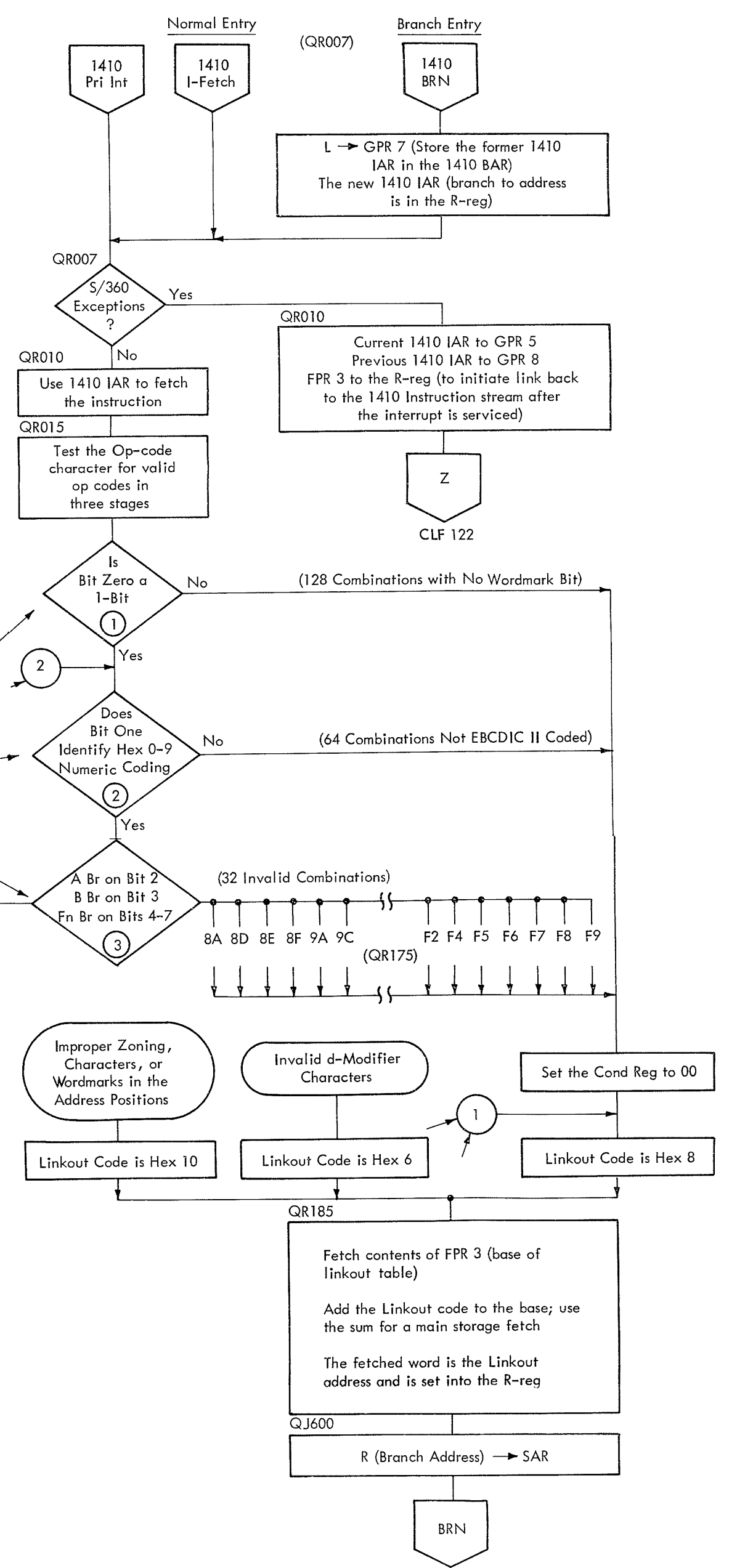


FIGURE CLF 900. 1410 I-FETCH



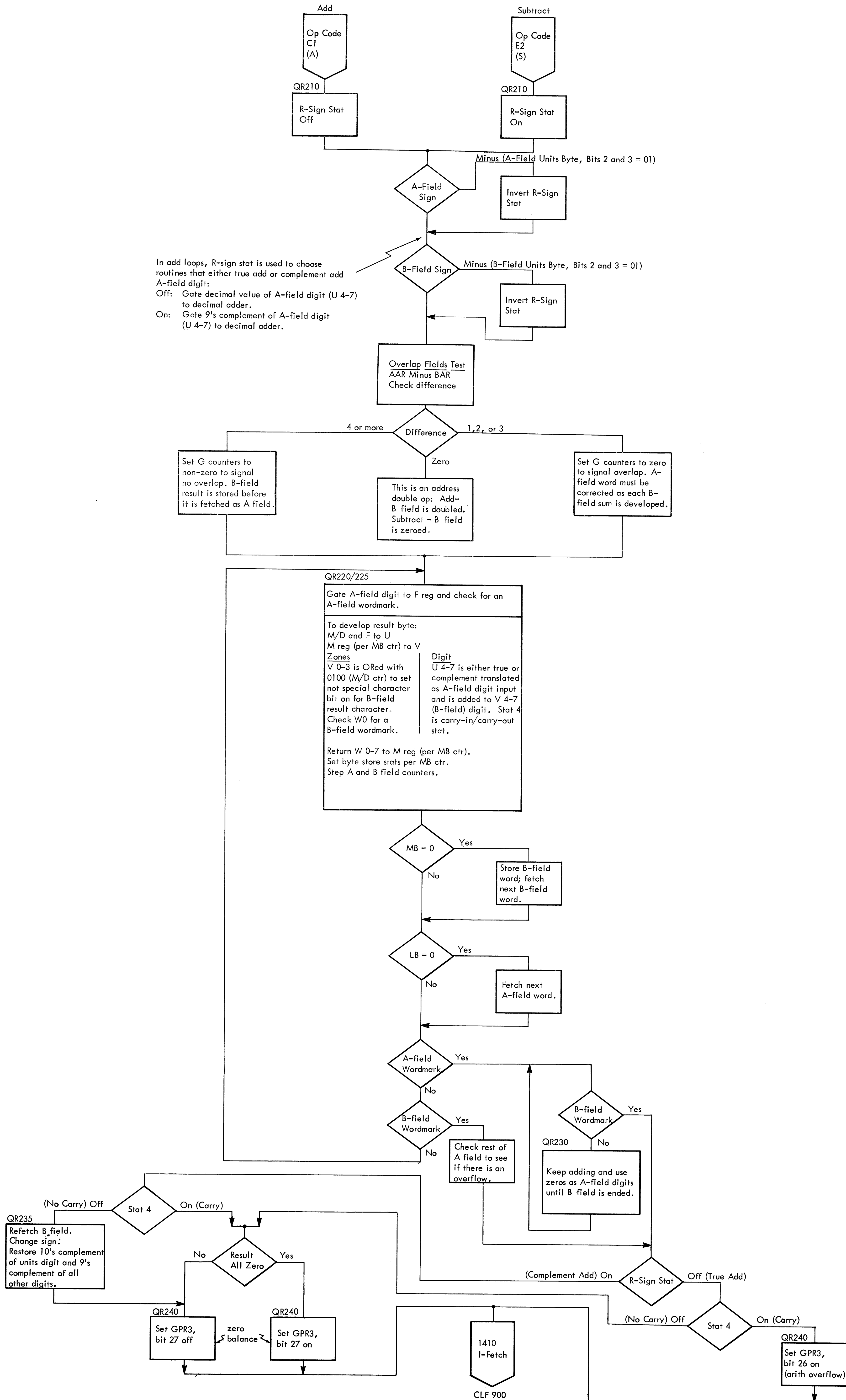


FIGURE CLF 901. ADD/SUBTRACT

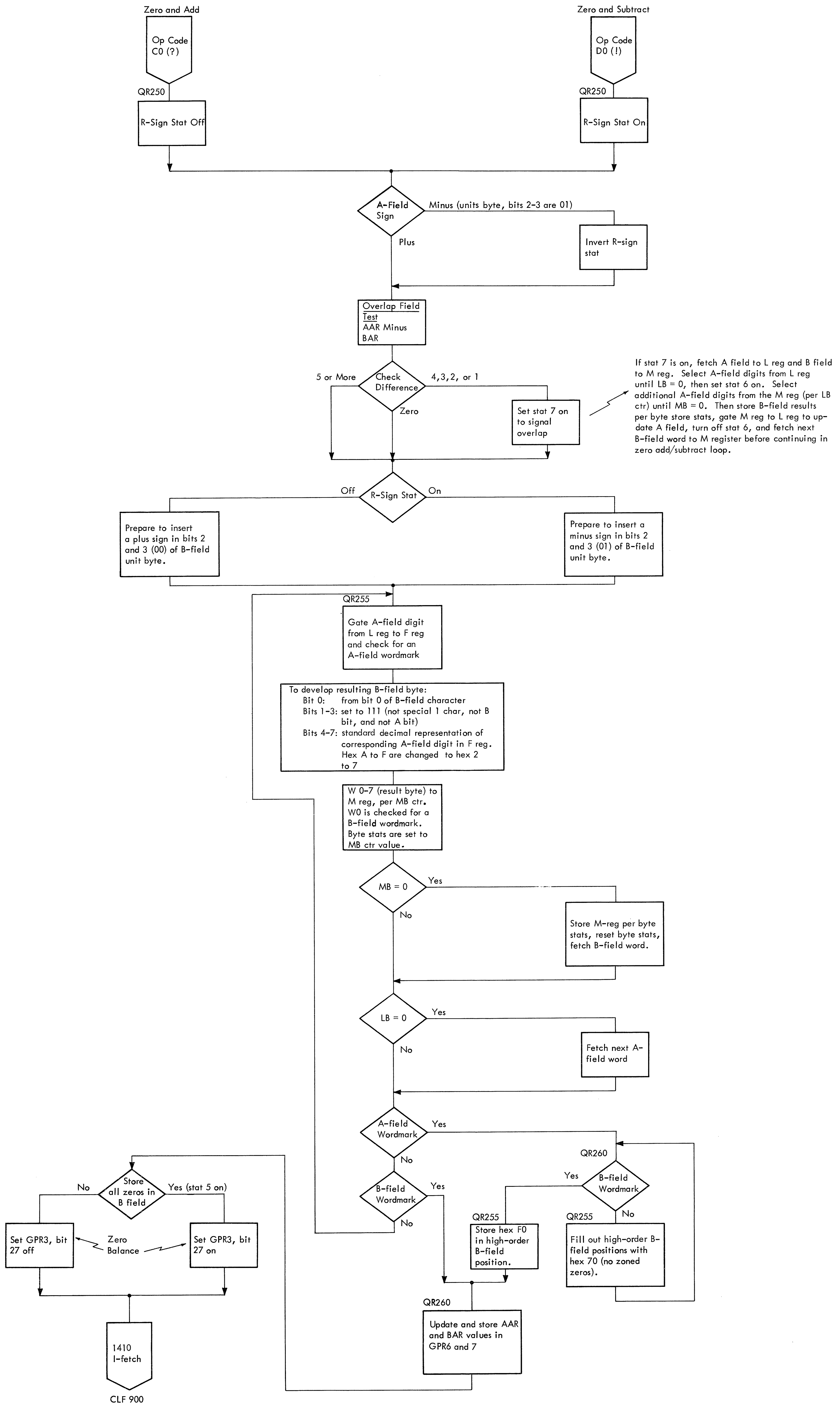
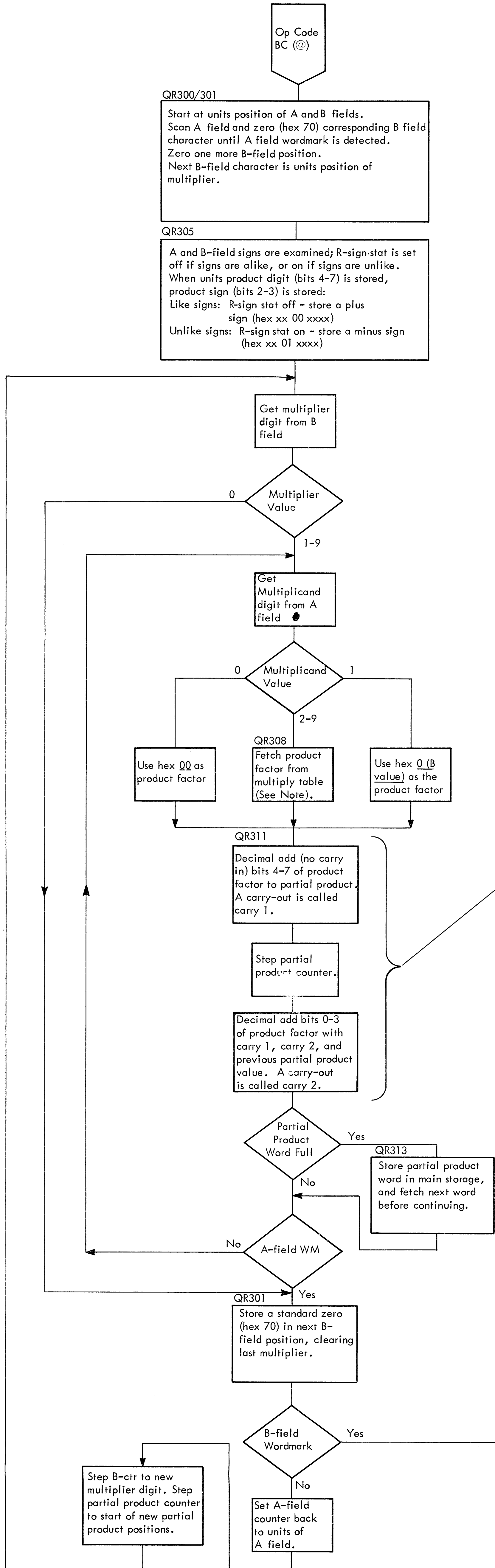


FIGURE CLF 902. ZERO AND ADD/ZERO AND SUBTRACT



Note:

To fetch product of B and A-field factors from multiply table.	Example: B factor is 7 A factor is 5
1. Emit from ROS → Y (Base Address of multiply table)	2100
2. Take B-field digit (not 0) Shift left four Shift right one Add to #1 result	0000 0111 0111 0000 0011 1000 → 0038 (binary add) 2138
3. Take 8 bit off A-field digit (not 0 or 1) Add to #2 result	0101 → 0005 (binary add) 213D
#3 sum is byte address of product byte of A and B-field factors.	byte at 213D is hex 35
Bits 4-7 are units digit of product.	
Bits 0-3 are tens digit of product.	

Example:

A field	623
B field (before)	65A0F5
B field (after clearing)	650000
Initial partial product	0000

B Factor	A Factor	Product
5	3	15
5	2	10
5	6	30

With first B factor, and with all A factors, fetch product factors, and decimal add them to partial product.

(decimal add)

00
15
015
10
011
30
31

Step to next B-field position and clear it.

603115
--------

Step again for next B factor Use it with all A factors to fetch another series of product factors; add them to partial product, properly aligned.

B Factor	A Factor	Product
6	3	18
6	2	12
6	6	36

(decimal add)

11
18
329
12
044
36
40

Step to next B-field position and clear it.

0
---

B and A-field wordmarks end multiply execution.

(final B field) 040495

Partial product is saved in main storage as it is developed.

FIGURE CLF 903. MULTIPLY

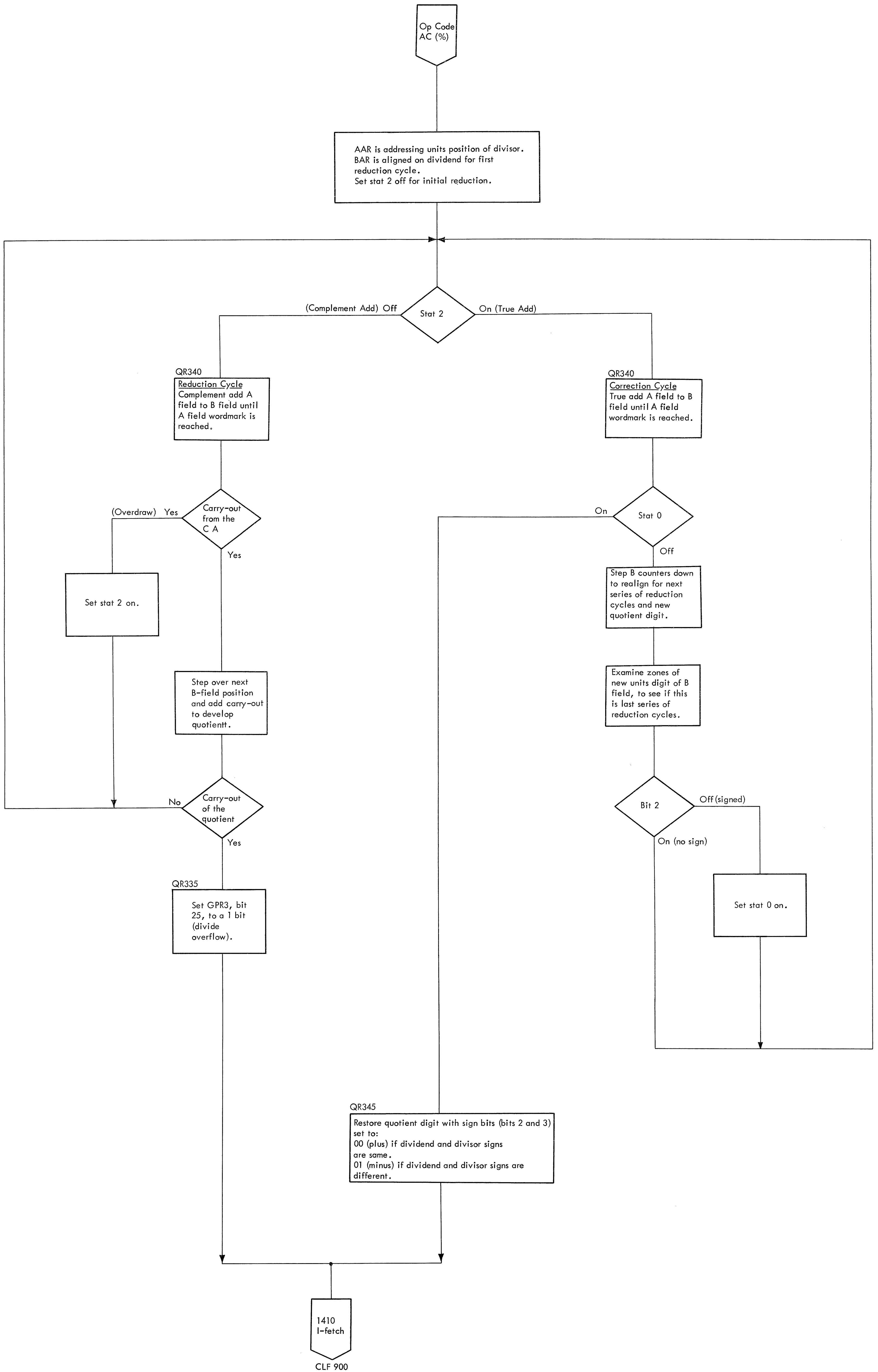


FIGURE CLF 904. DIVIDE.

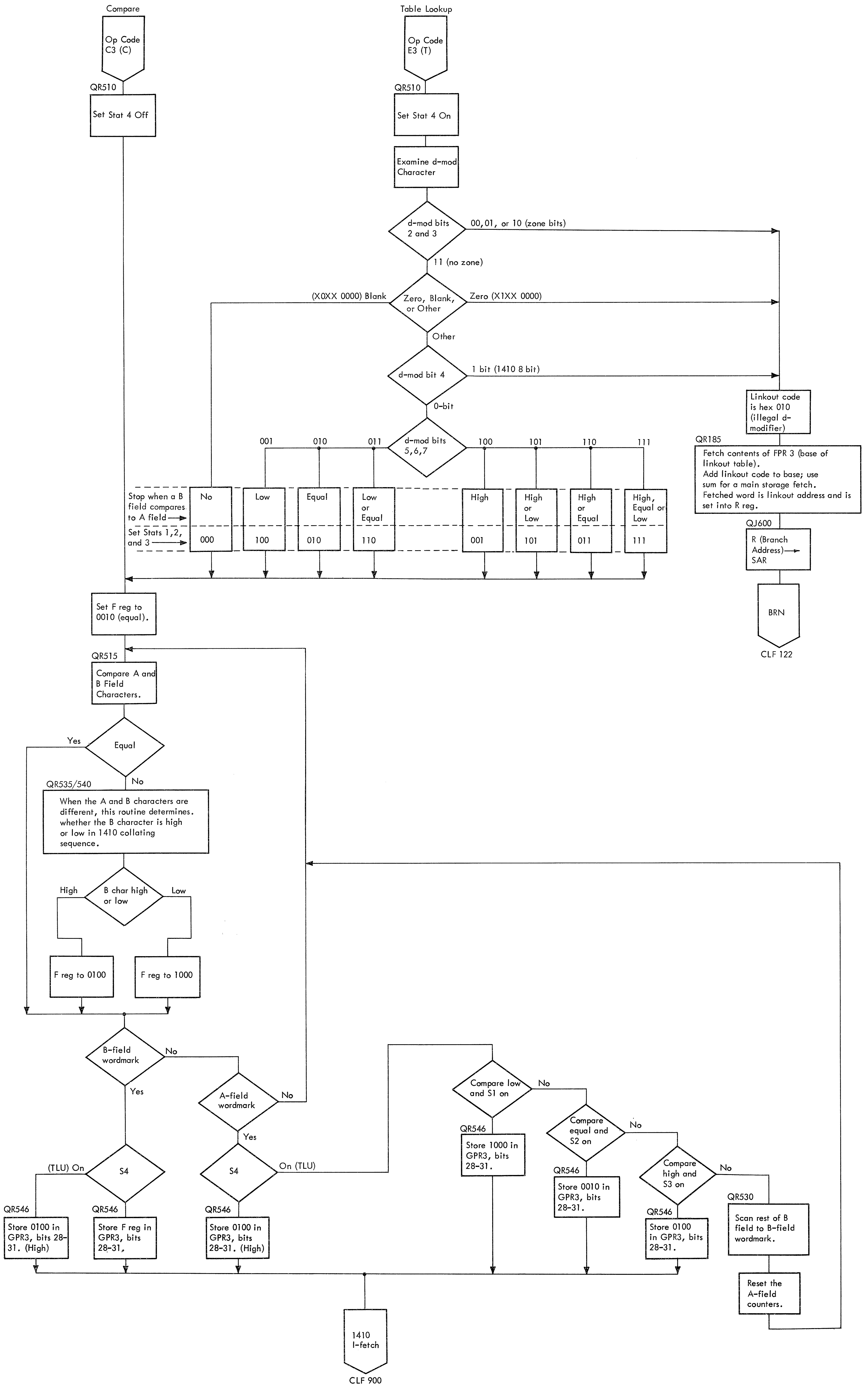


FIGURE CLF 905. COMPARE/TABLE LOOKUP

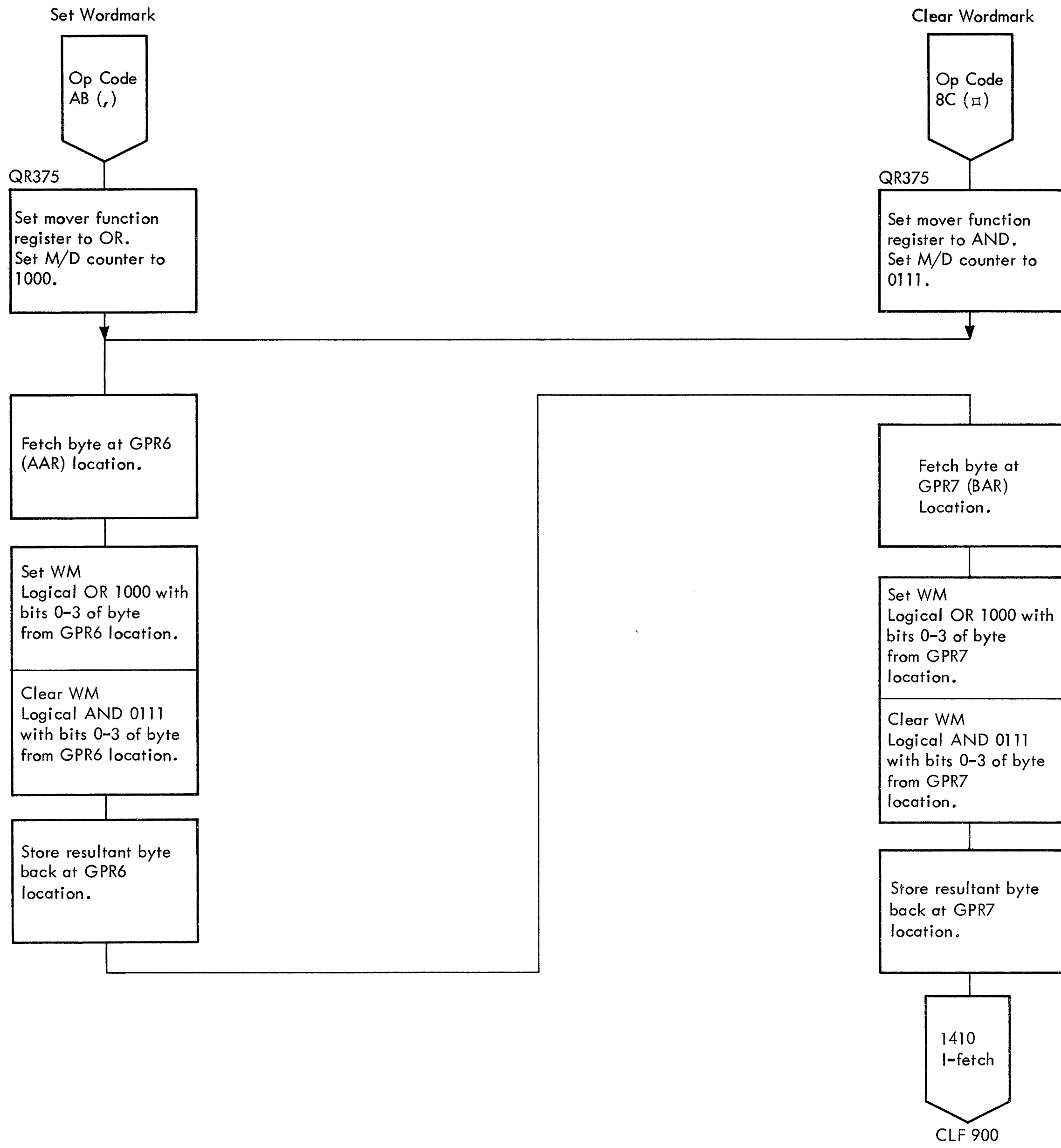


FIGURE CLF 906. SET WORDMARK/CLEAR WORDMARK

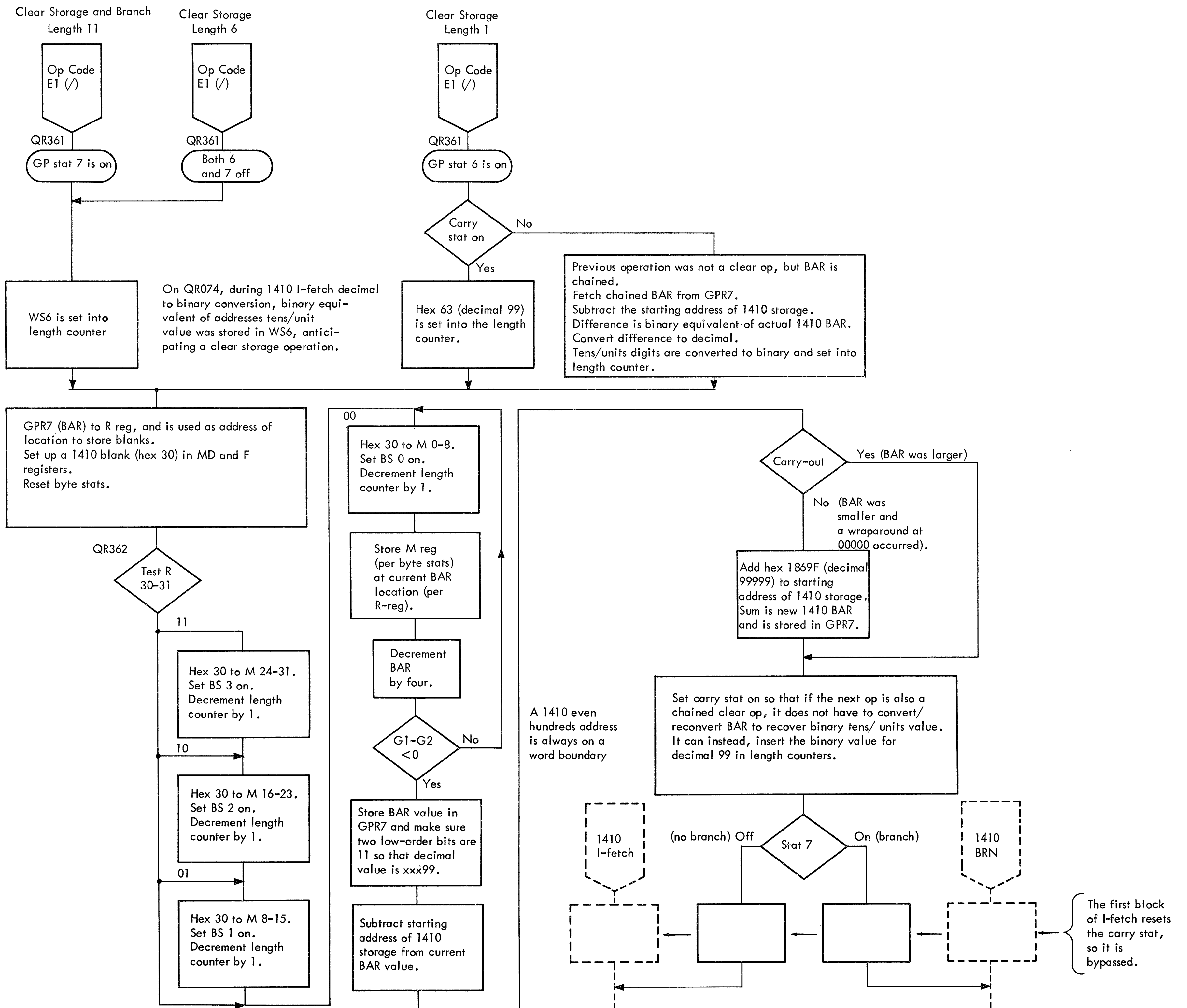


FIGURE CLF 907. CLEAR STORAGE/CLEAR STORAGE AND BRANCH

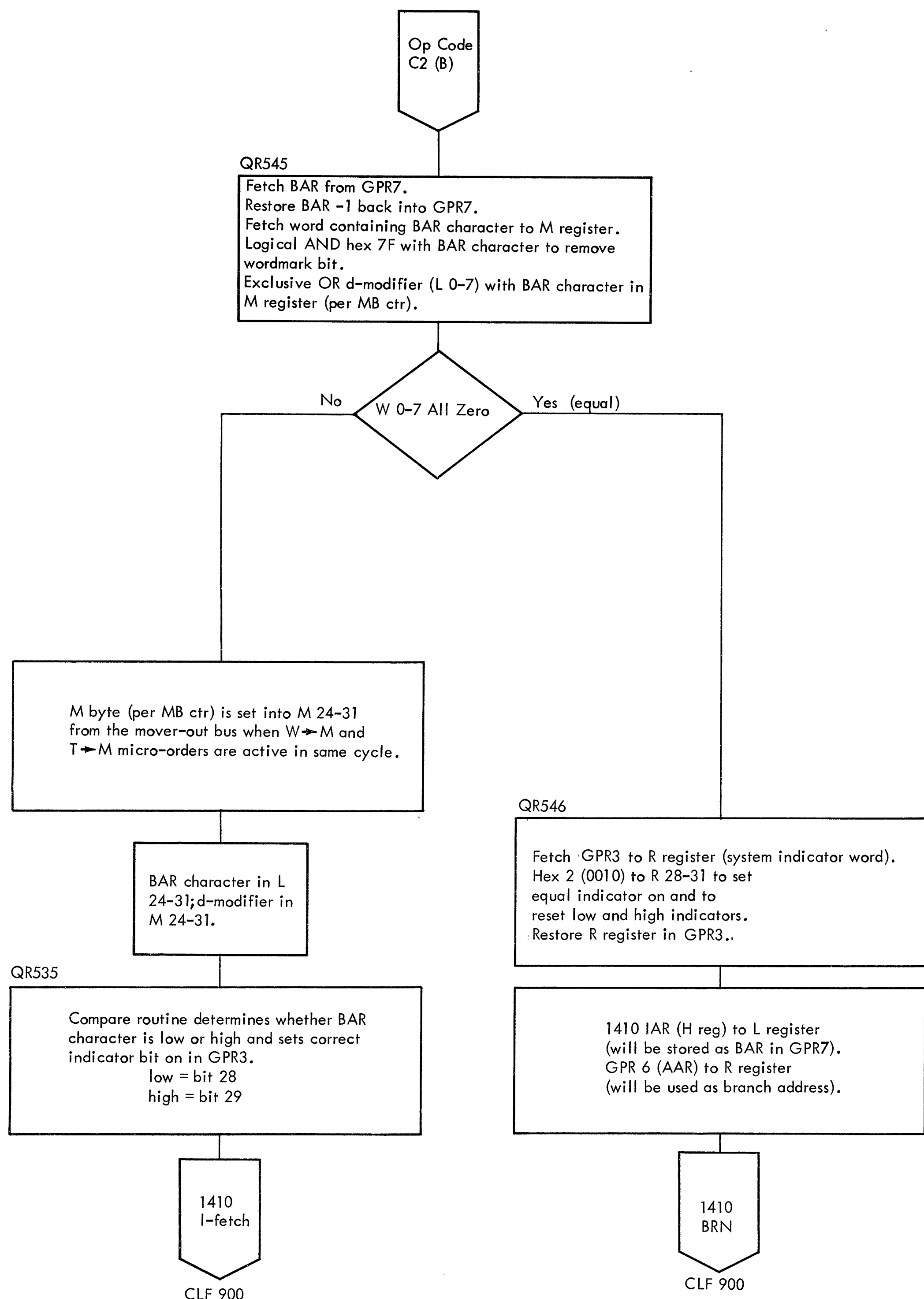


FIGURE CLF 908. BRANCH IF CHARACTER EQUAL

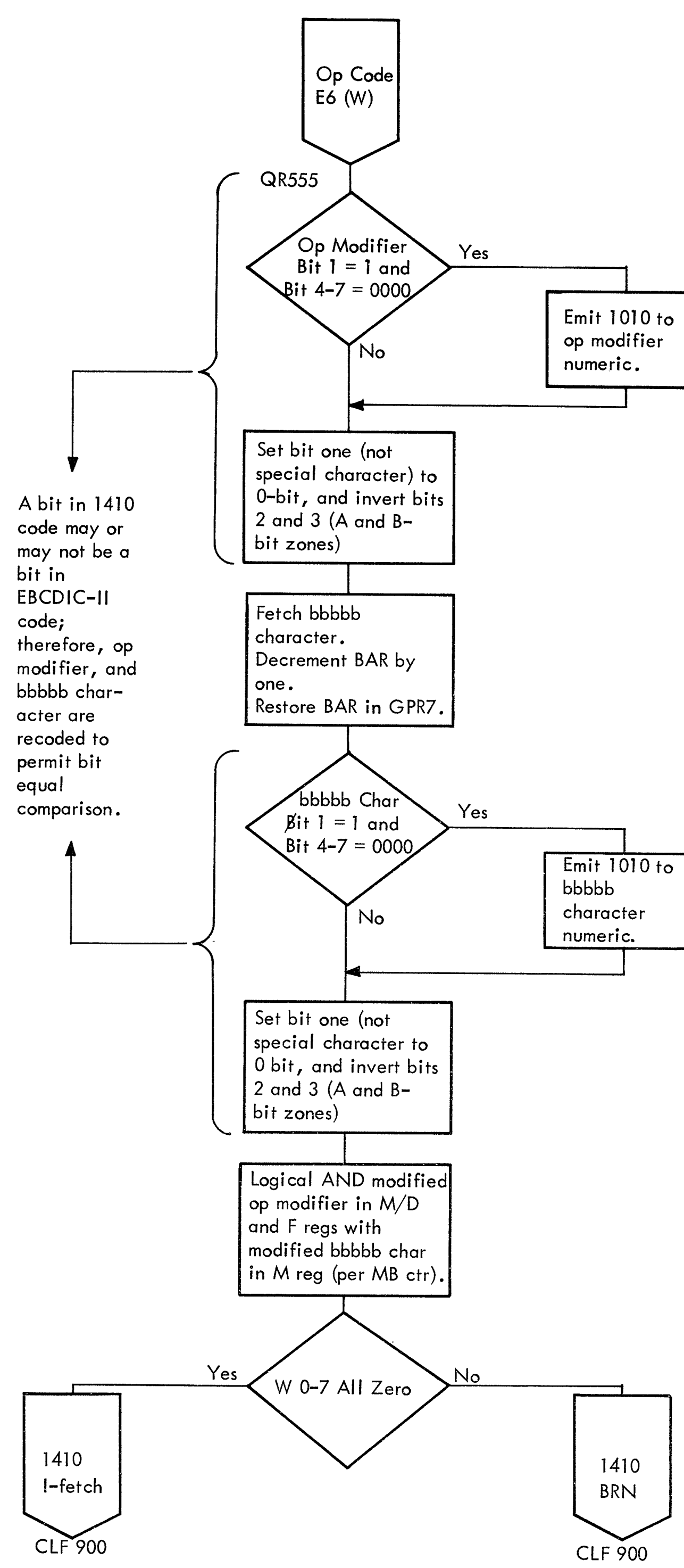


FIGURE CLF 909. BRANCH IF BIT EQUAL

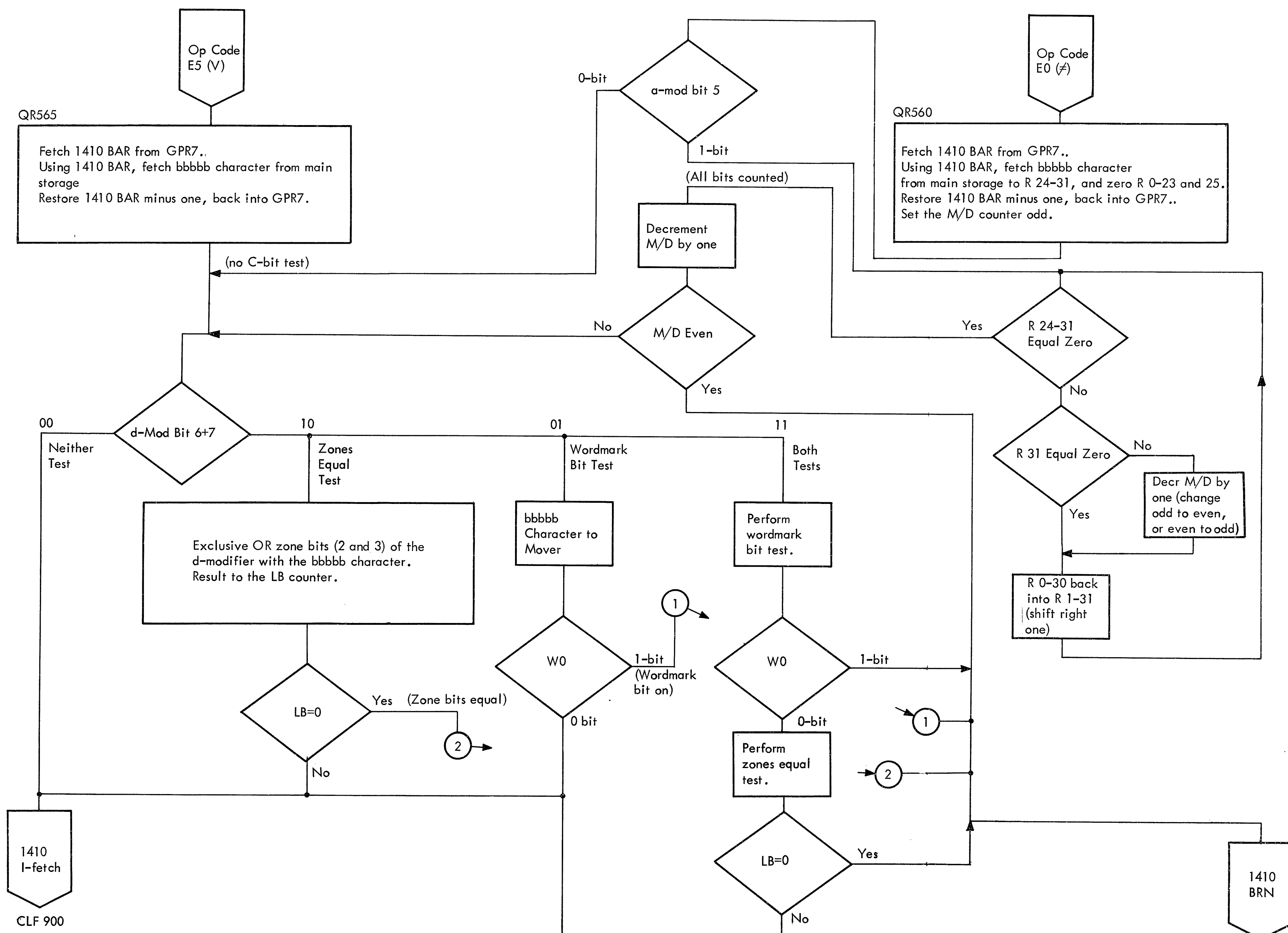
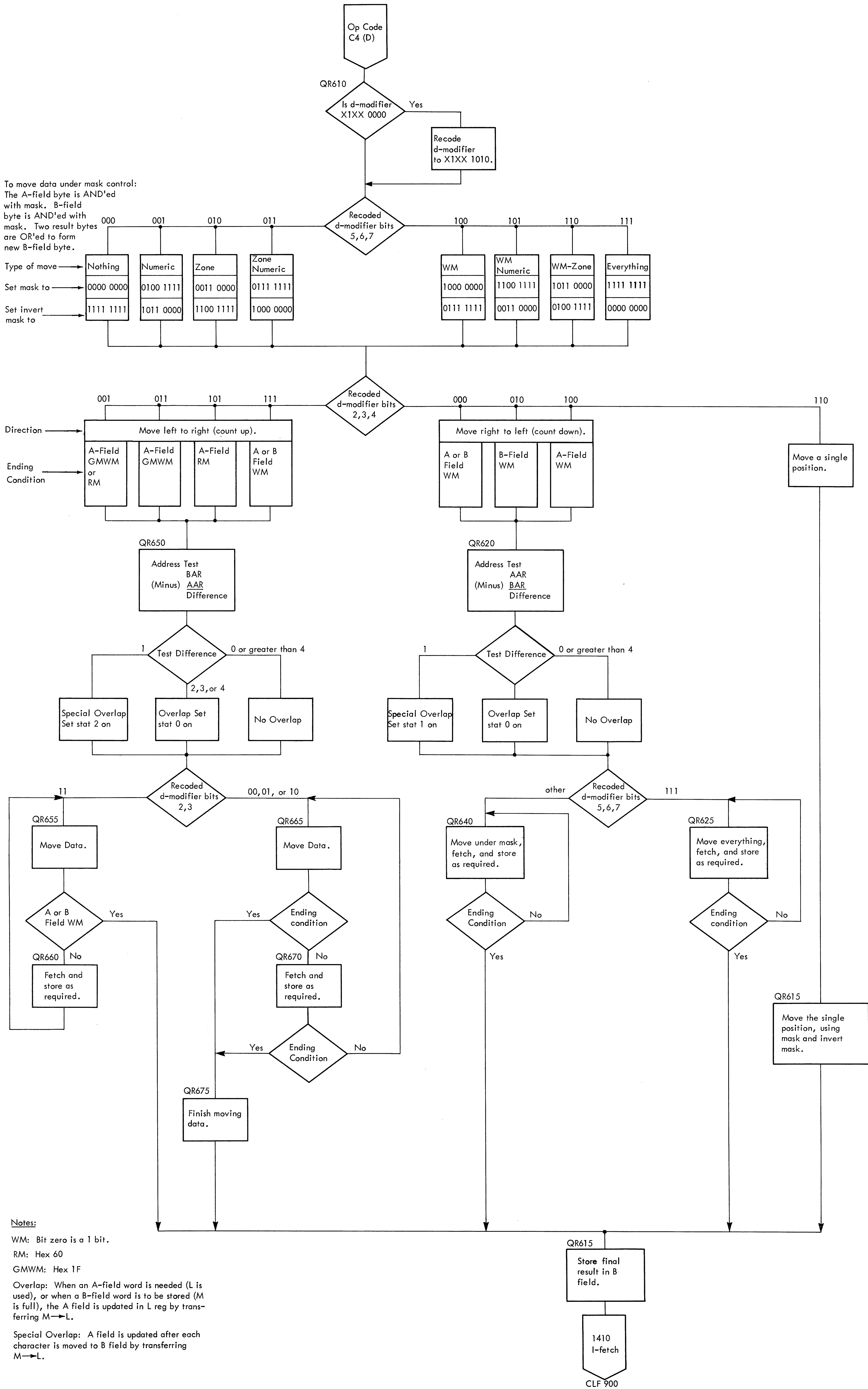


FIGURE CLF 910. BRANCH ON ZONES EQUAL/WORDMARK/C BIT



Notes:

WM: Bit zero is a 1 bit.  
 RM: Hex 60  
 GMWM: Hex 1F

Overlap: When an A-field word is needed (L is used), or when a B-field word is to be stored (M is full), the A field is updated in L reg by transferring M → L.

Special Overlap: A field is updated after each character is moved to B field by transferring M → L.

FIGURE CLF 911. MOVE DATA



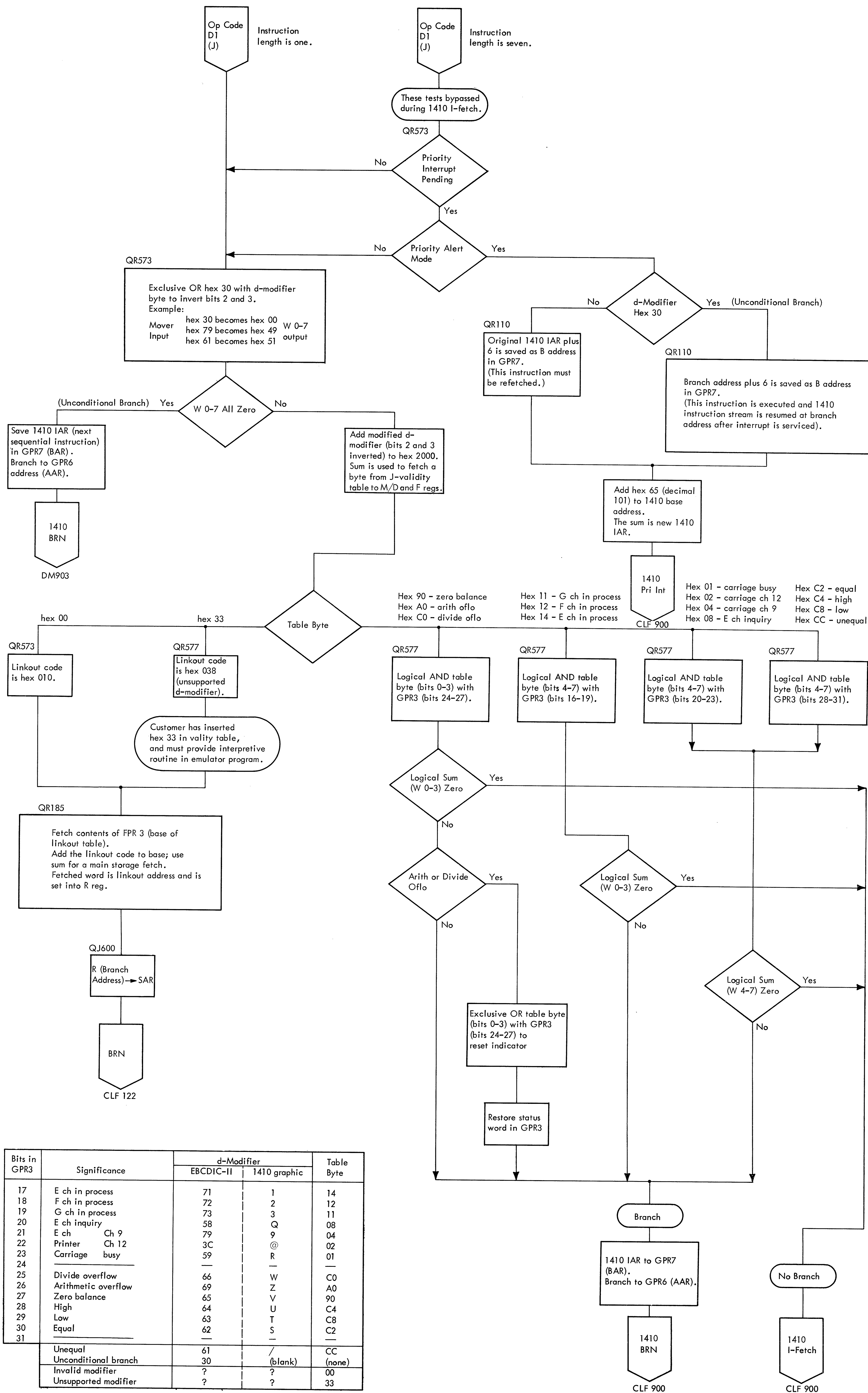
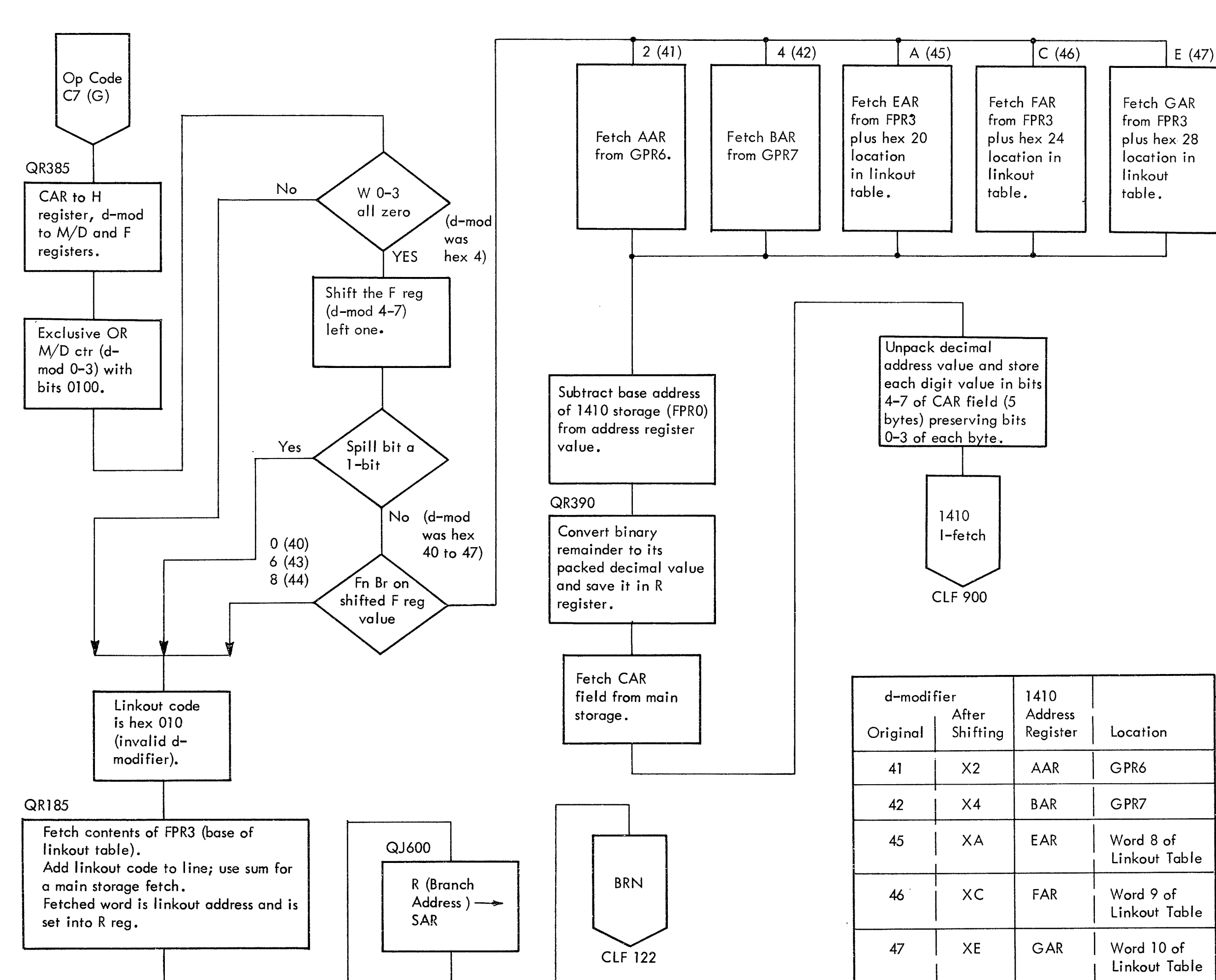
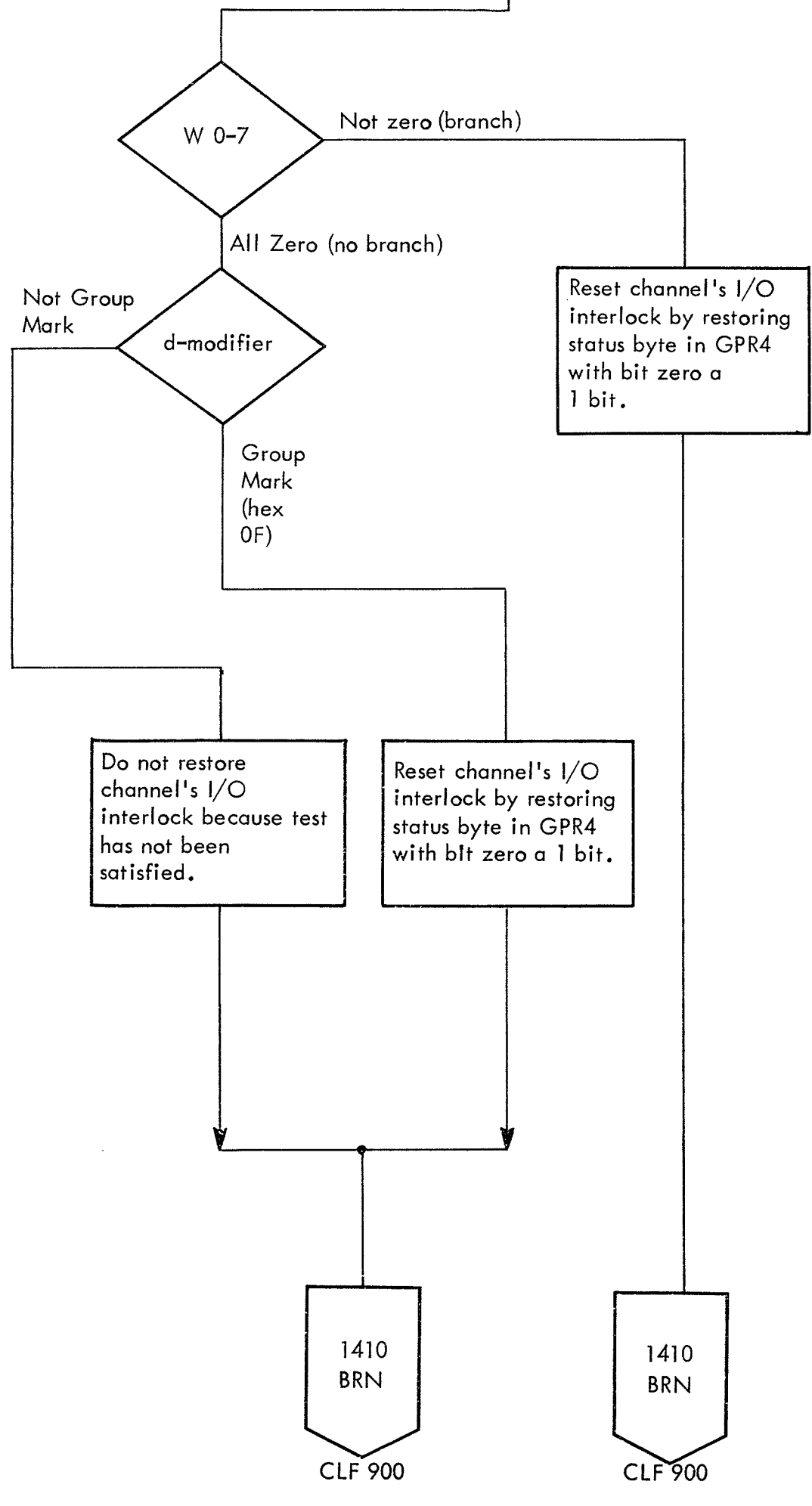
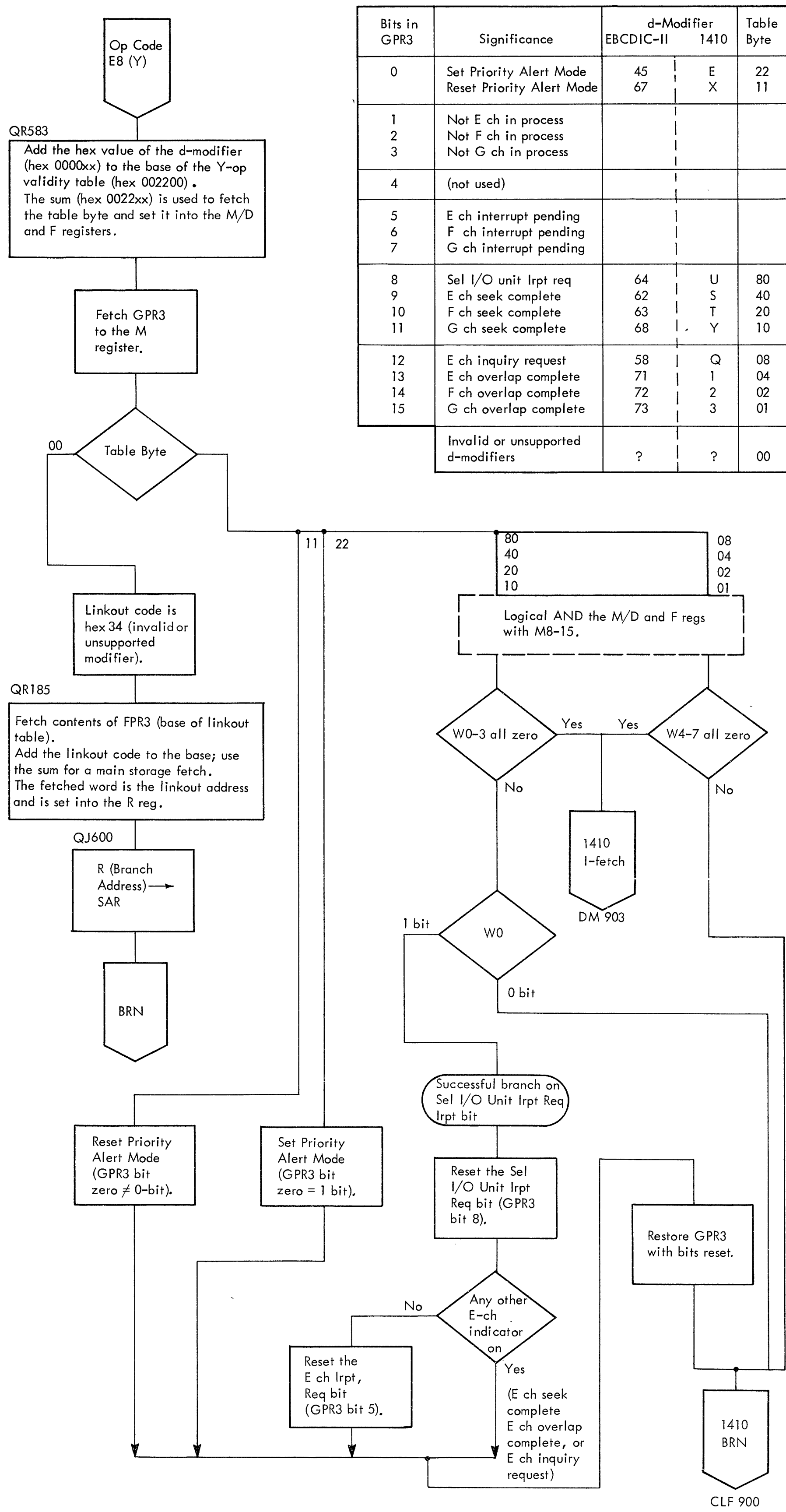
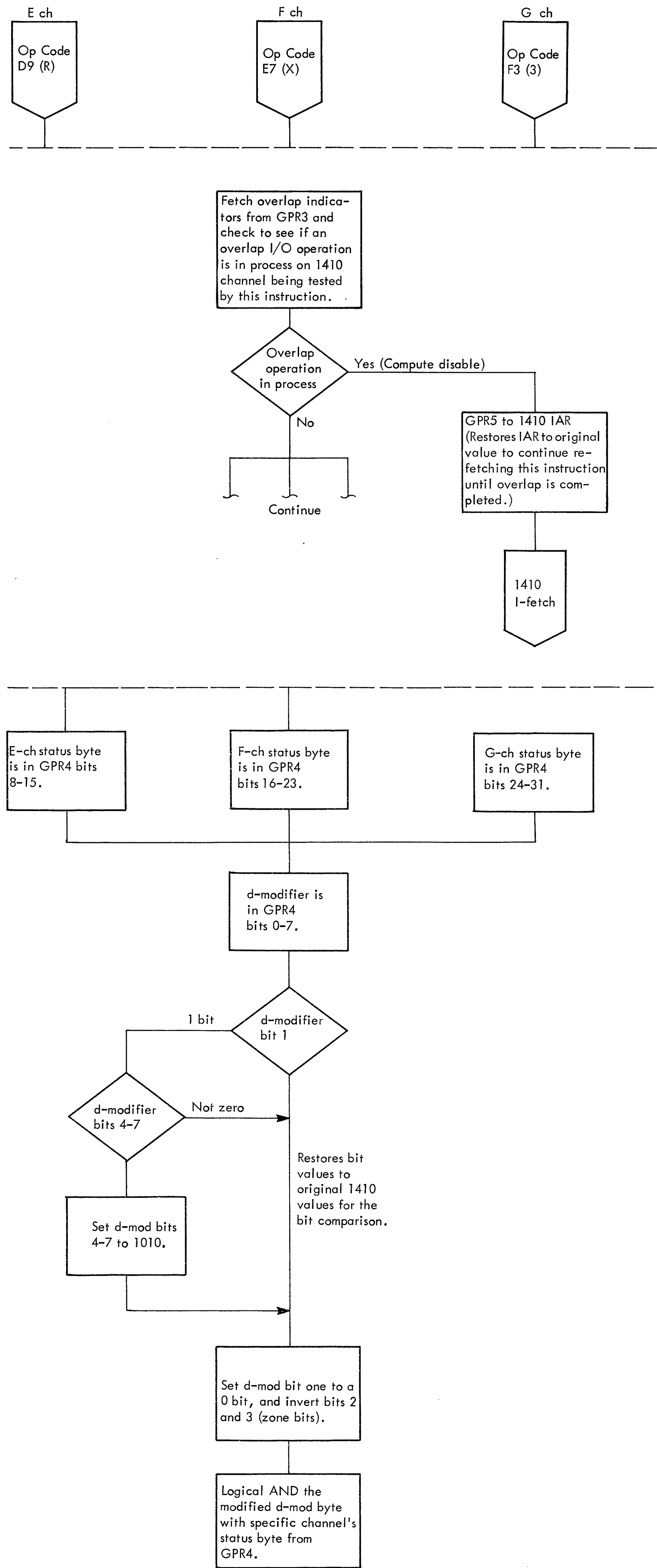


FIGURE CLF 912. TEST AND BRANCH



Bits in GPR3	Significance	d-Modifier EBCDIC-II	1410	Table Byte
0	Set Priority Alert Mode Reset Priority Alert Mode	45 67	E X	22 11
1	Not E ch in process			
2	Not F ch in process			
3	Not G ch in process			
4	(not used)			
5	E ch interrupt pending			
6	F ch interrupt pending			
7	G ch interrupt pending			
8	Sel I/O unit Irpt req	64	U	80
9	E ch seek complete	62	S	40
10	F ch seek complete	63	T	20
11	G ch seek complete	68	Y	10
12	E ch inquiry request	58	Q	08
13	E ch overlap complete	71	1	04
14	F ch overlap complete	72	2	02
15	G ch overlap complete	73	3	01
	Invalid or unsupported d-modifiers	?	?	00

FIGURE CLF 913. BRANCH ON E/F OR G CHANNEL STATUS

FIGURE CLF 915. STORE ADDRESS REGISTER

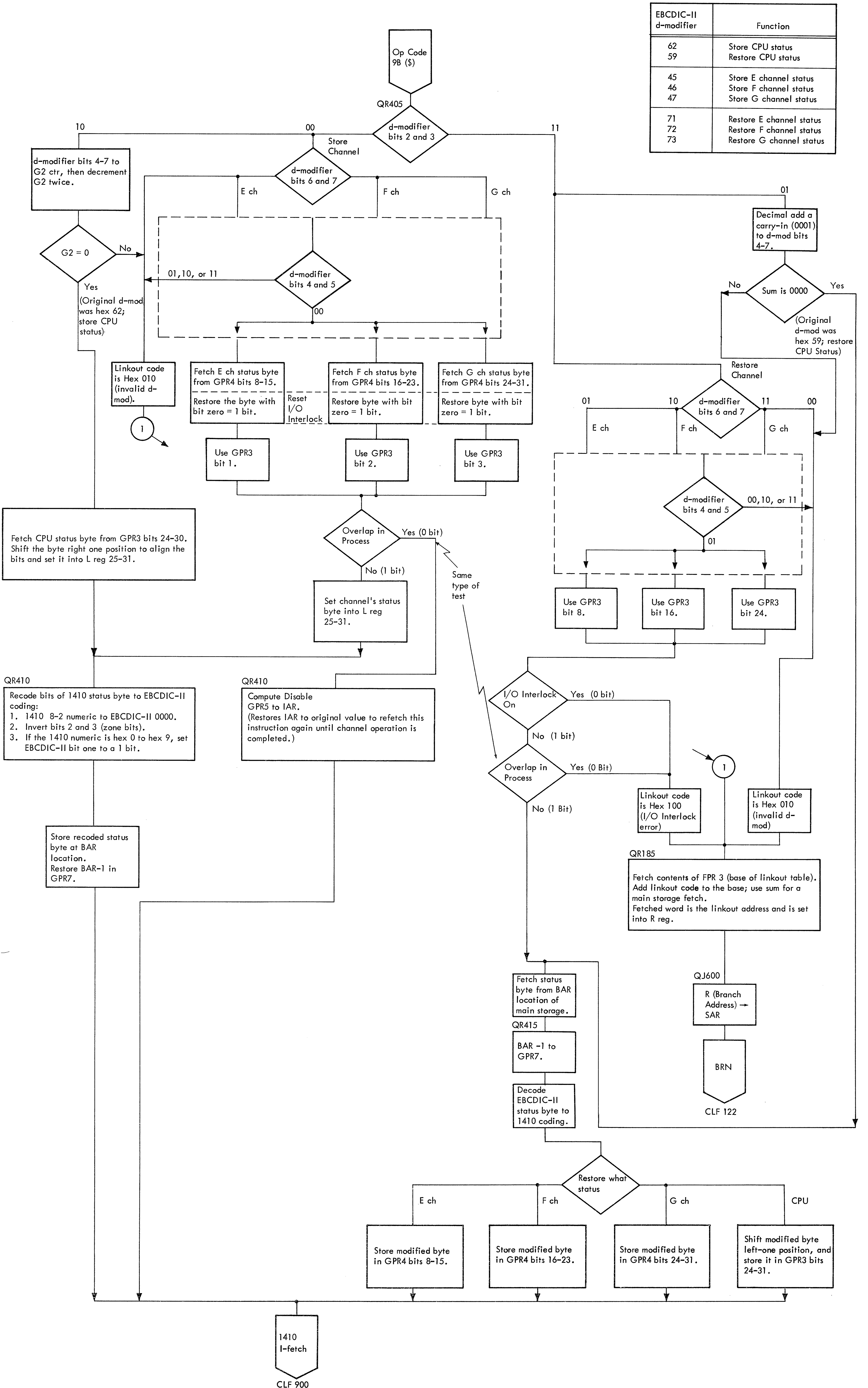


FIGURE CLF 916. STORE OR RESTORE STATUS

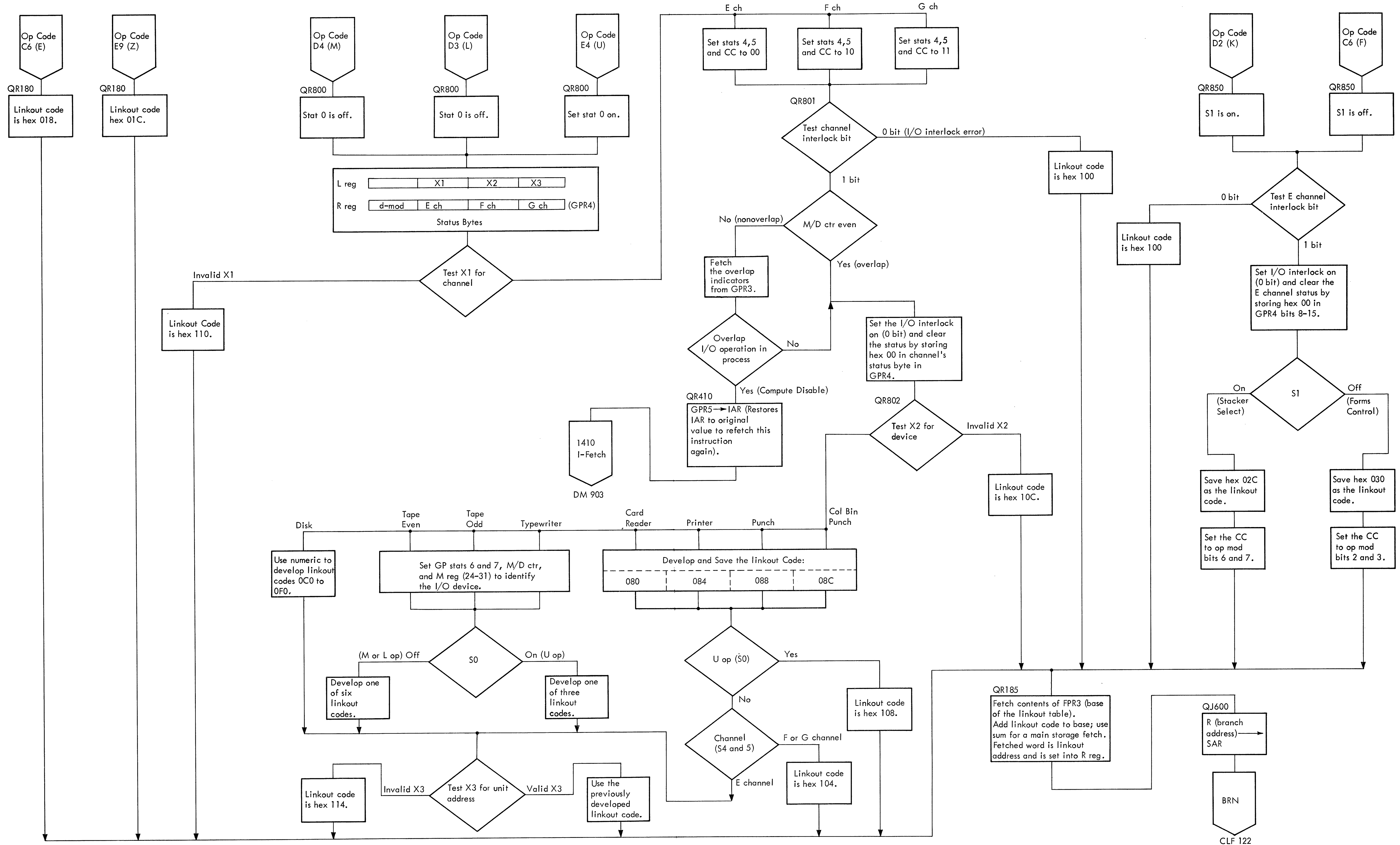
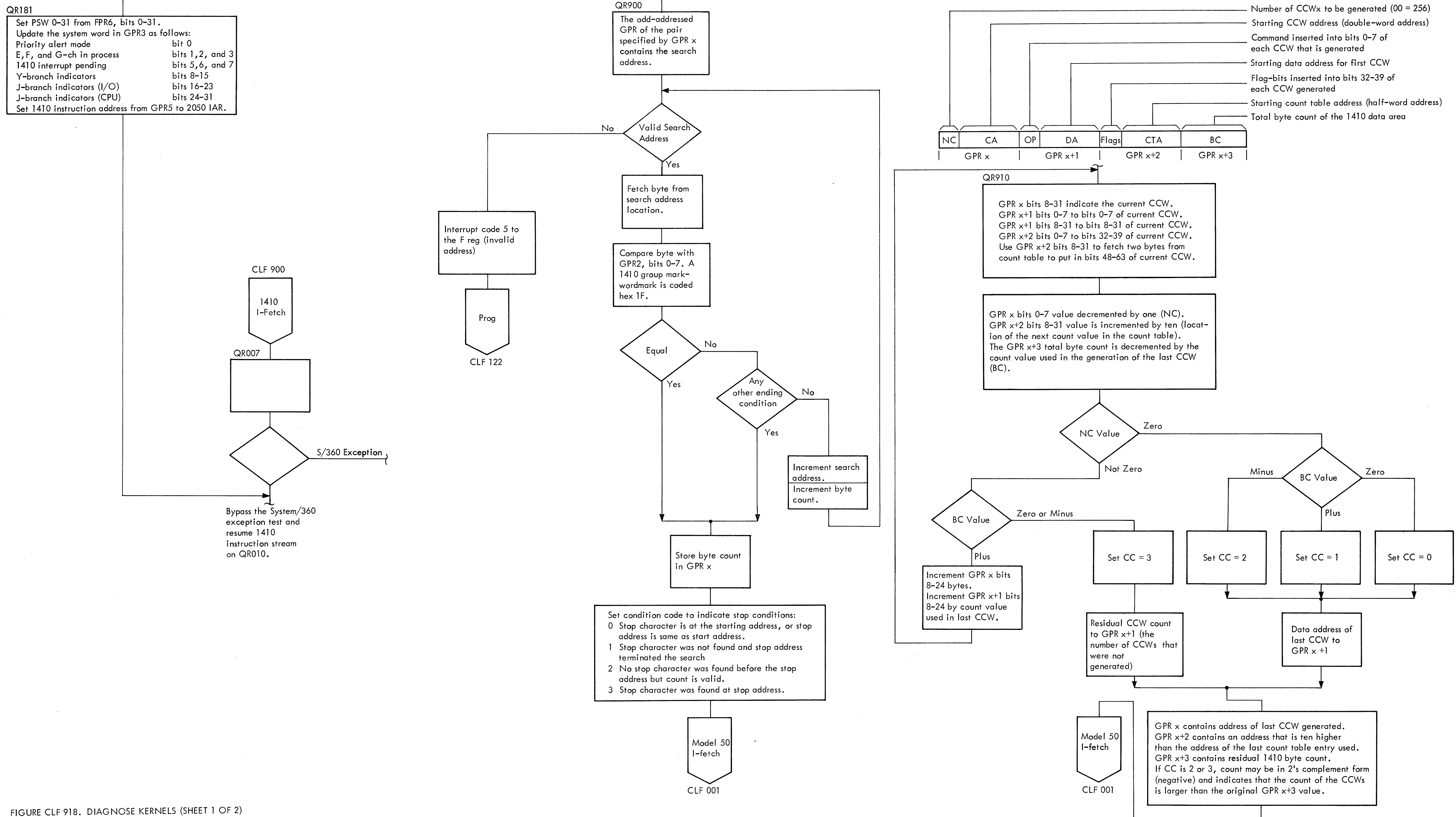


FIGURE CLF 917. EDIT/ZERO SUPPRESS/I/O INSTRUCTIONS

Linkback (8300 0AB1)  
This routine is the program linkage from the emulator program back to the 1410 instruction stream.

Special Scan (83x0 0A36)  
This routine scans the 1410 I/O data field and counts the number of bytes anticipated by the 1410 I/O instruction. The resulting count is used in the System/360 CCW count field.

CCW Generate (83x0 0AB5)  
This routine generates a string of CCWs for the disk emulation programs. Generated CCWs are stored in main storage, each one separated by two double words (room to insert two CCWs between the generated CCWs).

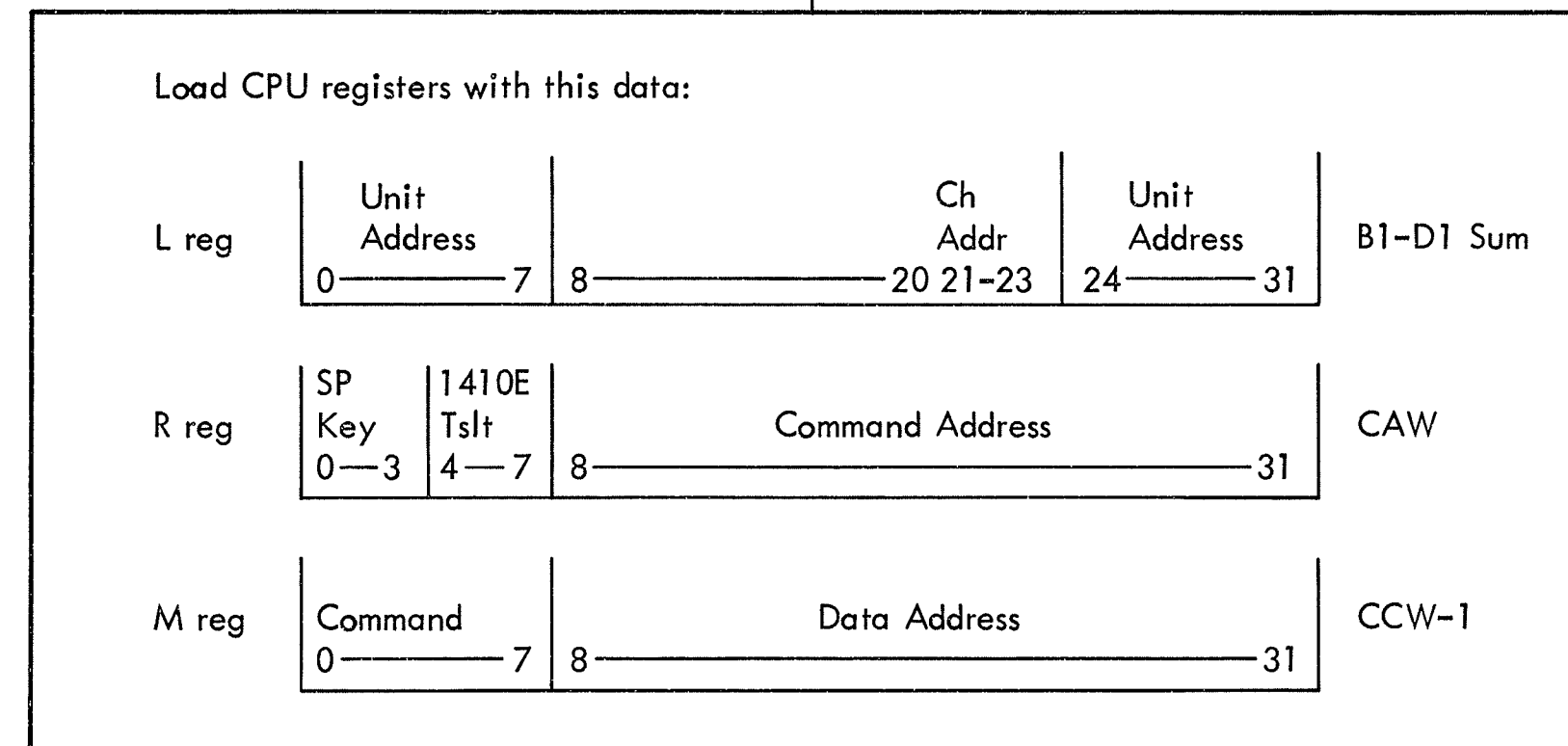


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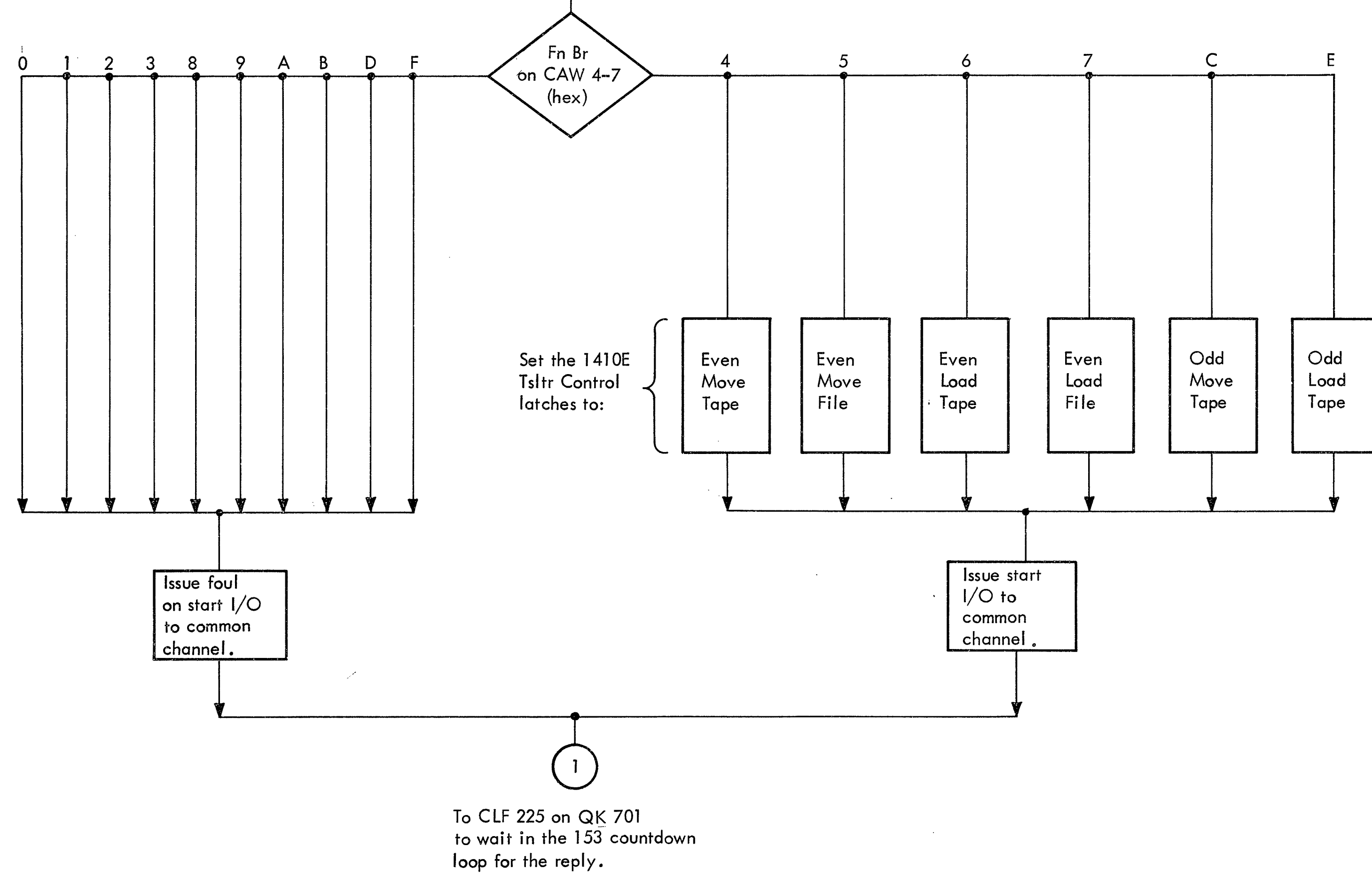
FIGURE CLF 918. DIAGNOSE KERNELS (SHEET 1 OF 2)

Start I/O (83x0 0AB8)  
 This routine initiates a System/360 I/O operation on a selector channel that is simulating a 1410 tape or file operation. It permits special control bits in CAW 4-7 and CCW 37-39 to modify the selector channel operation.

QR920

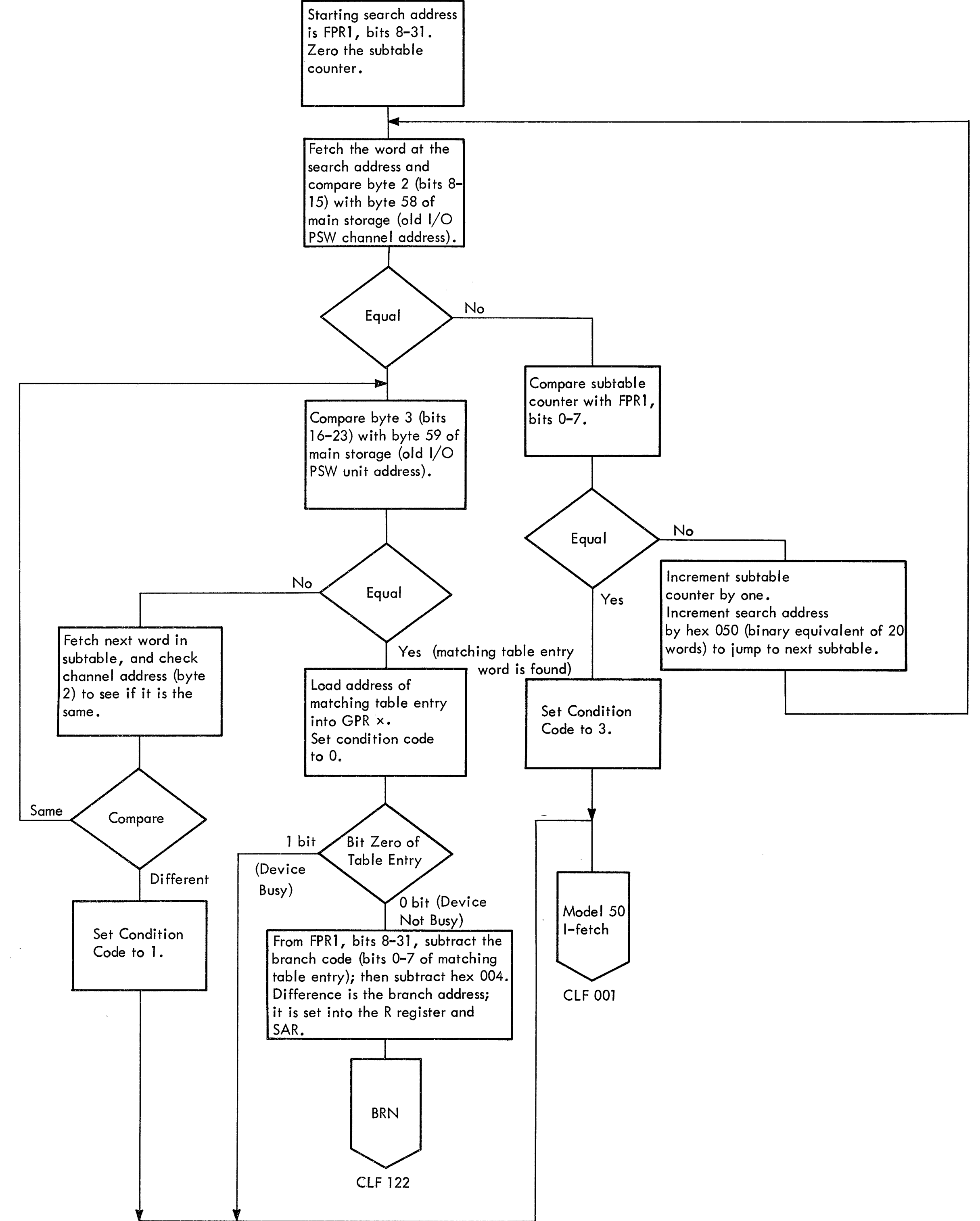


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Device Table Search (83x0 0AD5)  
 This routine searches through a table for the matching channel address; then, within the channel address portion of the table, the search continues for the matching unit address.

QR930



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 Page Added 8/1/66  
 by FFS Z22-6600-1

FIGURE CLF 918. DIAGNOSE KERNELS (SHEET 2 OF 2)







FIELD ENGINEERING DIAGRAM MANUAL, IBM SYSTEM/360  
MODEL 50--2050 PROCESSING UNIT, FORM Z22-2833-4

This supplement to the subject manual provides diagrams for the 7070/7074 Compatibility Feature, the 1410/7010 Compatibility Feature, system reset (CLF 126), and IPL (CLF 127). The system data flow diagram (SDF 000) has been updated to show new form numbers, and the 1052 Adapter diagrams (IOP 301-306) have been updated.

Changed or new figures are indicated by a vertical line in the table of contents and changed figures are indicated by the symbol (●) to the left of the figure title.

Substitute the attached table of contents, SDF pages, and revised IOP pages for respective pages in the manual. Insert CLF 126 and CLF 127 in the proper place, and add diagrams for the compatibility features at the back of the manual.

File this page at the back of the manual. It will provide a reference to changes, a method of determining that all amendments have been received, and a check that the publication contains the proper pages.

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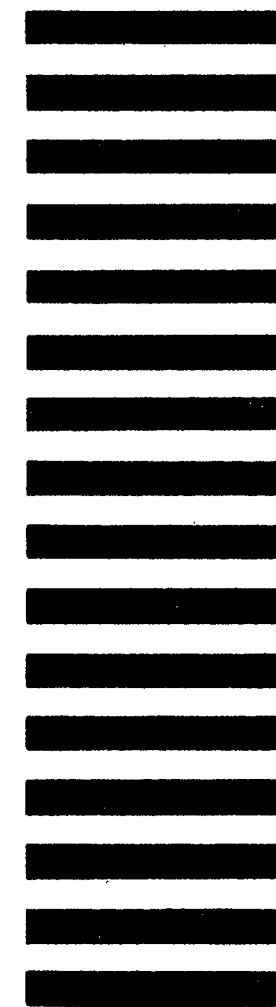
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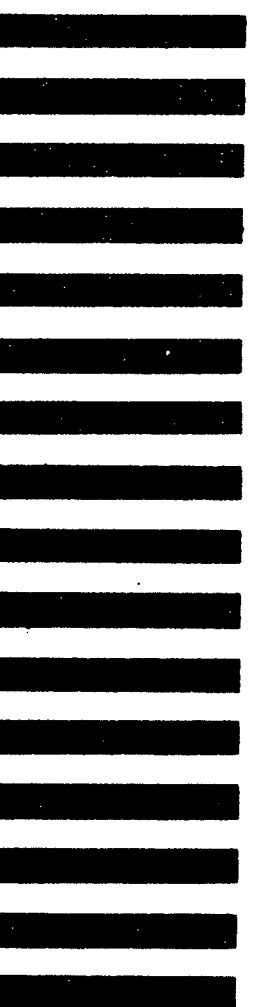
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