IBM

Field Engineering Education
Student Self-Study Course

2025 Processing Unit

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PREFACE

This manual is primarily intended for use by Field Engineering customer engineers enrolled in the 2025 Processing Unit Course 53232

Second Edition (February 1970)
This is a major revision of, and does make SR25-5414-0 obsolete.

Issued to: _____

Branch Office: _____ No: _____

Address: _____

_____

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Address any comments concerning the contents of this publication to: IBM, Field Engineering Education Media Development Center, Dept 927, Rochester, Minnesota 55901.

CONTENTS

GENERAL INFORMATION

FIS branch office self-study course administered via the FSS terminal. Follow-up lab to be administered at an education center.

MODE OF TRAINING

This course is a continuation of an overall training sequence which includes follow-on lab Course 13233. Because a total training sequence is involved, some of the topical objectives will not be completely supported in this FIS course. These objectives will be identified by an asterisk (*), which indicates that further activity will be required in the follow-on lab course.

If review of the training sequence is necessary, contact the FSS Monitor or your Field Manager.

The topic description and objectives for all sessions are included in this guide for your information. A table of contents for all topics is listed by session number, subject, teach mode and page number.

Answers to self-study questions for off-line sessions are included in each session. All text references to microfiche frames are on the following form numbers:

Teach material - SV31-0124
Quiz material - SV31-0126

TO INITIALLY BEGIN THIS COURSE, YOU MUST SIGN ON THE TERMINAL.

COURSE DESCRIPTION

This course teaches the operating principles and functional units of the Model 25 CPU and channel, including the standard interface for multiplexer and selector channels. The course prepares the student for a required follow-on lab and a subsequent Lecture/Lab course covering 2025 CPU attachments.

Prerequisites

For a complete list of the prerequisites and post-requisites, contact your local FSS monitor.

MATERIAL REQUIRED

For a complete list of all material required, contact your local FSS monitor.

TIME REQUIRED

For a complete list of times for each session and total course time, contact your local FSS Monitor.

INSTRUCTIONS TO THE STUDENT

This is a self-study text and will be used by you in conjunction with instructions and material from an FSS (Field Support System) terminal. This text (FEESSC - Field Engineering Education Student Self-Study Course) contains the assignments, questions and some of the answers on the material to be studied.

The FSS terminal will record your progress and provide you with the directions for the assignments that will best fit your learning requirements. After reading the introductory pages that follow, ask your monitor to assist you in signing on the FSS terminal. You will then receive instructions via the terminal which should start you on your way through the course.

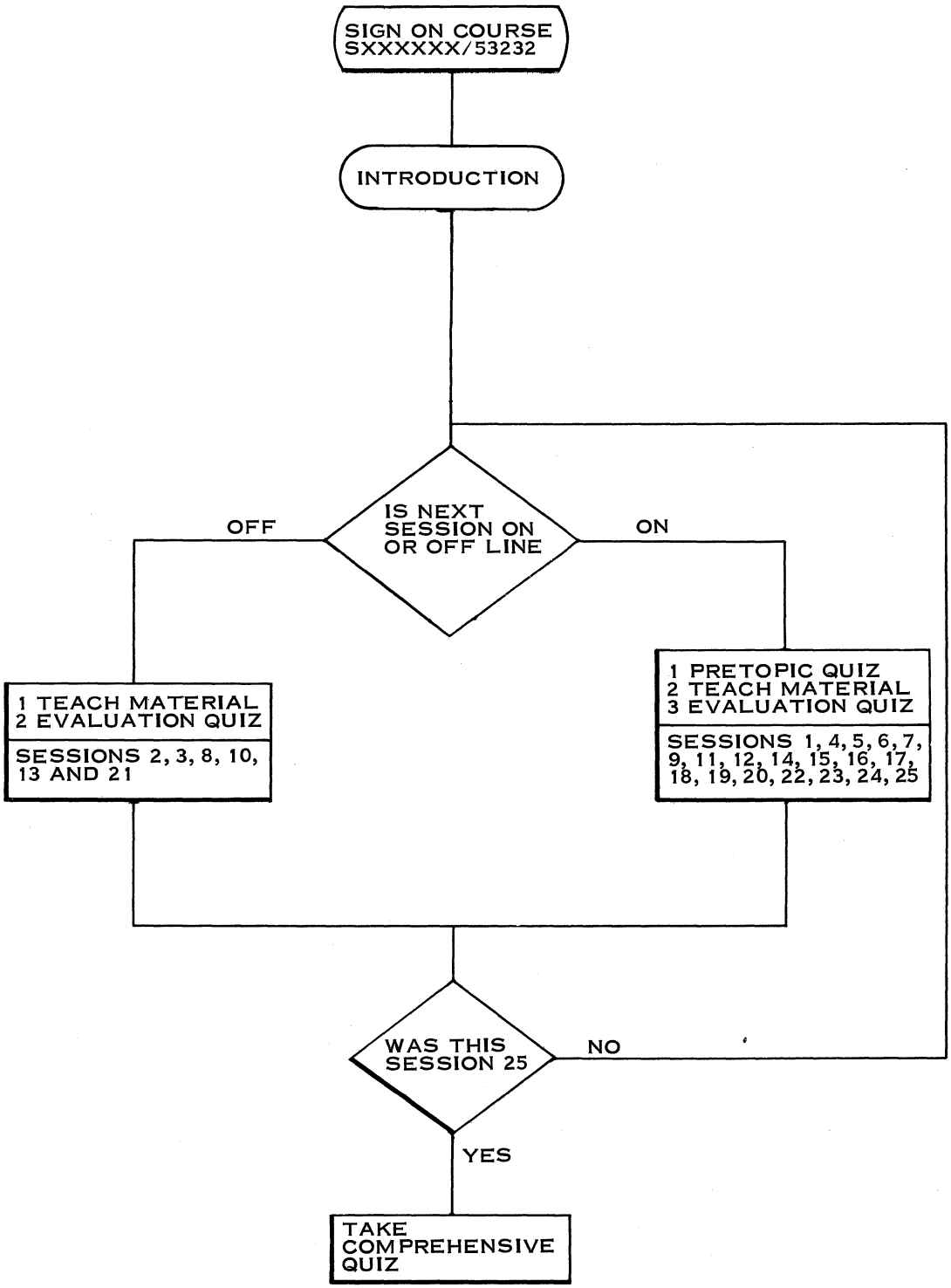
If you have never taken an FIS course, it is recommended that you have your monitor assist you in taking the FIS Orientation Course 50001 which may range in time from 0.5 hour to 2.0 hours. If you have taken an FIS course prior to this one, the basic operations are still the same.

The following is a brief summary of the important ground rules that you should keep in mind while you are working in this course:

1. Become familiar with your texts as soon as possible and try to associate their titles with their acronyms (FEMM, FETOM, etc.).
2. If studying at the terminal (not signed off), try to use one book at a time and keep the other texts stacked where you may reach them. This will allow you more space at the terminal.
3. When responding at the FSS terminal, try to remember to do the following:

    a. make entries in lower case typing.
    b. use numerals for numerical entries and avoid spelling the value.
    c. use no special characters or function keys such as tab, carrier return, line feed (index), $, ?, #, ., unless instructed to do so. Some entries, such as error corrections and comments, will require the use of special characters and are covered in the following pages.
    d. if you encounter any difficulty with the FSS terminal or the course and can not successfully continue, contact your monitor immediately.

4. Do not mark in any library copy books or forms since they will have to be used by others who follow you.



2025 Processing Unit, Course 53232 - Student Sequence

SESSION 1 - INTRODUCTION AND DATA FLOW

This topic will introduce the CE to the Model 25 and its relationship to the System/360 product line. General information, performance capabilities, major features and CPU data flow will be taught. The CE will also be introduced to basic controls, control words and some of the system internal functions.

Objective: Upon completion of this topic the student should be able to:

1. Given a list of I/O devices, identify the devices which can be natively attached to the Model 25.
2. Identify the memory readout time and the word length capability of the CPU.
3. Using the basic data flow diagram, identify the following:
   a. W-M register core loop.
   b. LS, A-and B-register, ALU data loop.
   c. I/O In, I/O Out data loop.
4. Identify the main purpose of the mode register.
5. Identify the main function of the MMSK register.
6. Differentiate between the effect of the mode register and the MMSK register on local storage selection.
7. Using the data flow diagram, identify the data path from local storage to memory.
8. Using the data flow diagram, identify the data path for control words.
9. Using the data flow diagram, differentiate between data input from 2311 compared to all other I/O.
10. * Given a sequential set of control words, enter a microprogram into control storage and execute it, tracing the data flow through the CPU functional units - ie, hardware registers, local storage, ALU, etc.

Sign on the terminal at this time.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

INTRODUCTION AND DATA FLOW

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____
11. _____
12. _____
13. _____
14. _____
15. _____
16. _____
17. _____
18. _____

SESSION 2 - INTRODUCTION TO MICROWORDS

This topic will contain the general information covering the various types of control words that direct all operations of the Model 25 CPU. An introduction to the MAS listing is also included.

Objective: Using the MAS testing and console indications to determine causes for system malfunctions, the student should be able to:

1. Given a list of control word types, match each control word with its associated hex word.
2. * Given a set of control words in hexadecimal, determine the operation to be performed by each, and write a microstatement for each control word. If the operation is arithmetic or logical, determine the outcome.
3. Locate the branch destination for a branch word.
4. Identify the A-source field (if applicable) for any given control word.
5. * Use the MAS cross reference listing to determine which microroutine detected an error when any control address is indicated in the M-register.

Highlights

- Control words are double byte (halfword) in length.
- Control words are located in the control storage section of main storage.
- Seven types of control words are available.
- Control words are gated from main core to the C0 and C1-registers.
- Each type of control word performs a different function and controls the overall flow of data within the CPU.
- Control register bit positions 0, 1, and 15 identify the control word type.
- The microprogram listings give a sequential and descriptive layout of the various routines of the E60 emulator program.

Activity

Read: The following material on microword introduction.

The Model 25 CPU data flow that was presented in the previous topic contains various registers, assemblers and core locations.

In order to move the data or control information from one place to another, some type of program or internal control is necessary. In the Model 25, the means of establishing this internal control is unique.

Remember that the Model 25 CPU will emulate a 1401, or a System/360 Model 20, or in fact, a strictly diagnostic machine, depending upon which emulator microprogram is initially loaded into main storage.

*Partially or totally supported in follow-on lab course.

Regardless of which emulator program is loaded into main storage, there is one consideration which will always be present. All of these microprograms are comprised of microwords and these microwords, upon execution, will determine the actual flow of data within the CPU.

In the Model 25, these microwords are referred to as control words and are located in the control storage section of main storage.

To learn more about these control words, first an exposure to the E60 (System/360 Model 25) Microprogram Listing is necessary because this listing will be one of your tools in troubleshooting system malfunctions.

Please turn to the contents page of the listing (Form R25-5402).

On this page you will find a table of contents of the various microroutines that comprise the total System/360 Model 25 emulator microprogram.

One of these microroutines is BDIA. Locate BDIA on this page and you will see that this is a resident CPU diagnostic routine.

The routine which is a System Reset microroutine is BSYS.

What routine controls Instruction Cycles?

The correct choice is CICY.

Perhaps you can see some similarity between the function of the microprogram and the last 3 characters of the routine name, for example:

Resident CPU Diagnostic	- B DIA
System Reset	- B SYS
Instruction Cycles	- C ICY

Also notice that the microroutines are located alphabetically in the listing. (BDIA would come before CICY.)

Please turn to the beginning of the BDIA microprogram routine.

If you are having some difficulty, look at the left-hand side of the pages in the listing. You will see the statement numbers for the particular routine you are looking at. These statements are numbered sequentially and are preceded by four alphabetic characters.

Look at the alphabetic characters and you can determine which direction in the listing that BDIA is located.

Locate BDIA statement 001.

Above BDIA 001 you can see descriptive text.

Under the descriptive text, you will see column headings such as ADDR, WORD, NEXTSEQ, NEXTLABEL, etc.

Under the heading ADDR, the first information is 08FE. This is the address in main storage for the statement BDIA008.

Under the heading WORD, you can see the control word that is in main storage at address 08FE.

If you look under the heading STATEMENT, you will see that the function of this control word is BR, which means branch.

BR means that when this control word (8240) located in main storage location (08FE) is executed, a branch will occur.

Where will the microprogram branch to, though?

This information is found under the headings NEXTSEQ and NEXTLABEL. If you will look under these headings, you will see that the branch goes to the address at BDIA018, which is the label START.

1. The control word at the label START is _____.

Take a look at the information under the COMMENTS heading. Where possible, these comments are available and do give some indication as to the operation to be performed by a given control word.

For a small exercise, please answer the following:

2. The last address in the BDIA microroutine is _____.
3. If the branch at statement BDIA163 is executed, the next control word encountered would be _____.
4. BDIA302 has a label name of _____.

The entire microprogram is made up of microroutines that perform different tasks. These tasks will be discussed in later topics.

Now that you have some idea of how to read the listings, the control words can now be introduced further.

Take a look at microroutine CICY statement 008.

As you can see, the control word for that statement is 5498. This is hex notation, so 5498 is two bytes or a halfword in length. All control words are halfword in length.

These control words are read out of the control storage section of main storage and placed in the control registers (C0 and C1).

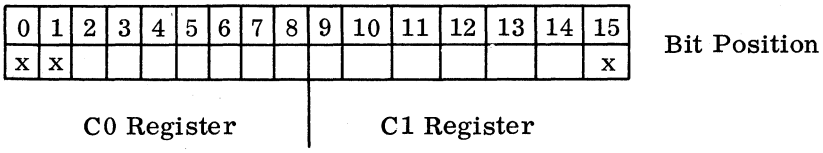
Once in the control register, any given control word will cause certain operations to occur. The kind of operation performed depends upon the type of control word being executed.

Seven different types of control word types are used in the model 25. These are:

Word Type 0
Word Type 1
Word Type 2
Word Type 3
Word Type 4
Word Type 5
Word Type 6 and 7 (combined function)

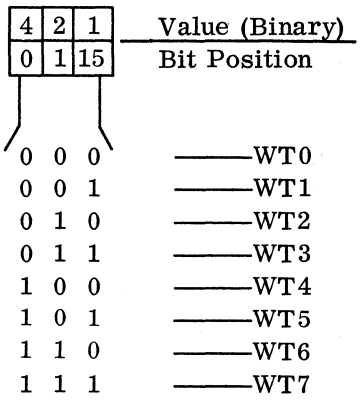
As was mentioned, each word type can perform a specific operation, but first you should be able to distinguish one word type from another.

Refer to the below figure.



When control words are called out of main storage and placed in the control register, there must be a means available for the CPU to distinguish the various word types.

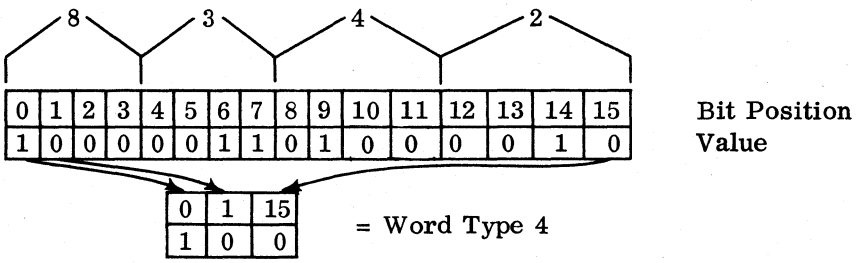
Bit positions 0, 1, and 15 of the control register are assigned the purpose of control word identification.



Depending on the bit positions that are active (1), seven different configurations can be represented.

Consider the following:

What type control word is 8342 (hex)?



Depending on the control word read into the control register; to determine the word type, the system simply looks at three bit positions.

Please answer the following study questions.

Match the following control words in hex notation with their associated word type.

5.	5438	_____	a.	WT0
6.	BBB2	_____	b.	WT1
7.	E161	_____	c.	WT2
8.	0080	_____	d.	WT3
9.	F228	_____	e.	WT4
10.	01E3	_____	f.	WT5
11.	AC67	_____	g.	WT6
12.	61E3	_____	h.	WT7

Now that the word types have been identified as to type, the basic function of each word type will be discussed.

Later in the course each word type will be covered in great detail.

Word Type - 0

Function - Set/Reset Word

1. Sets or resets bits of designated external registers.
2. Stores link address into local storage when used as a link word.
3. Retrieves link address from local storage when used as a return word.

In the front section of the microlistings, you will find bit significance charts for all word types.

Please turn to the chart for WT0.

As you can see on the chart, bit positions 0, 1, and 15 determine the word type as a WT0.

Other bit positions define the operation to be performed.

Bit 2 - If bit 2=0 the bits of the selected register are reset. If 2=1, the bits of the selected register are set.

Bits 4, 5, 6, 7 - Designate the register or external facility that will be set or reset; ie, 0000 would indicate the S-register.

Bits 3, 12, 13, 14 - Indicate the constant (K) that will be set or reset in the high order bit positions of the selected register, ie, K=84 The K high constant would be 8.

Bits 8, 9, 10, 11 - Indicate the constant (K) that will be set or reset in the low order bit positions of the selected register; ie, K=84 The K low constant would be 4.

Bits 8, 9, 10, 11 also perform other functions of link and return, but these will be covered later.

Some examples of WT0 follow:

	Word	Bit Structure															Comment
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
1.	3040	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	SET S K = 84
2.	0080	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	RST S4

Read the chapter Set/Reset Word in the FETOM, Form Y24-3527, and then return to this book.

Word Type 1

Function - Arithmetic Constant Word

1. Performs an arithmetic operation using a byte from local storage and a K (constant) value from the control word.

Please turn to the WT1 bit significance chart in the microlistings (Form R25-5402).

Bits 0, 1, 15 - Define the word type

Bits 2, 3, 12, 13, 14 - Compare the functional decode which determines the ALU operation, the A and B register gating and the destination of the ALU result.

Bits 4, 5, 6, 7 - Comprise the A-source field and indicate which byte of a designated local storage register is affected.

Bits 8, 9, 10, 11, - Comprise the K field.

Read the chapter in the FETOM entitled Arithmetic Constant Word and then return to this book.

Word Type 2

Function - Storage Word

1. Read data (byte of halfword) from program, control or auxiliary storage.
2. Store data (byte or halfword) into program, control, or auxiliary storage.
3. Do halfword updates of storage addresses or data counts.
4. Move halfwords from one local storage register to another.

To introduce the remainder of the word types, only the functions will be presented for WT3 - WT7.

Word Type 3

Function - Move/Arithmetic Word

1. Performs arithmetic and move operations on local storage data.
2. Moves local storage data to external facilities.
3. Moves data from external facilities to local storage.

Word Type 4

Function - Branch Unconditional Word

1. Branches unconditionally to some designated address.
2. Stores the next sequential address in the CPU backup register.

Word Type 5

Function - Branch on Mask Word

1. Performs 2, 4, 8, or 16 way branching.

Word Type 6 and 7

Function - Branch on Condition Word

1. Tests one of 8 bits of a designated byte source for a 0 or a 1 condition.
2. Branches if the condition of the bit tested compares to the condition indicated by the statement.

This has only been a brief introduction to control words, and, as you can see, many different operations can be performed.

Please answer the following study questions.

13. The word 368F is a set/reset word. _____ (True/False)
14. The word 0006 is an unconditional branch word. _____ (True/False)
15. Word types 8066, AC67, BBB2 deal with branching operations. _____ (True/False)

One more thing you should know about is the use of the microprogram address listing.

In the rear section of the microprogram listing is an address list showing the address of all control words that are located in main storage as a result of loading the E60 (System/360 Model 30 emulator program).

Occasionally, due to a malfunction, the microprogram may fail to execute properly. When this occurs, the CPU will stop and in the M-register lights on the console, the address of the failing microword will be visible.

It is possible, by using the address listing to locate the failing microroutine and microword.

You may already be familiar with the use of these cross references as a result of having Model 25 System I/O training. If so, please go to the heading of Evaluation Questions located at the end of this session.

Please display microfiche card 1 (Form V31-0124), frames A13 and A14, and you will see a section of the address listings.

To locate a control word for the address 0078 (C078 for a 48K system), first look on the left-hand side of the listing until you locate 0070.

Along the top of the frame, locate the last digit of the address, in this case an 8.

You can see by the marking on the listing that an address of 0078 indicates:

BCPL061
F0EE

This is to say statement number 061 of microroutine BCPL. Also, the control word that should reside at this address is given - F0EE.

To ensure that we are reading the reference correctly, please display frames A15 and A16 of card 1 (Form V31-0124).

As you can see, statement BCPL061 at address 0078 shows a control word of F0EE.

The statement says BR IF LZNZ or branch if the low order bits on the Z-bus are not at a value of 0.

As a troubleshooting aid, you now have a starting point to further investigate why this particular routine failed to operate correctly.

Let's try another one.

Turn to frames A17 and A18 of card 1 (V31-0124).

You can see that a control address of 1570 would yield statement 173 of the FILT microroutine.

Turn to frame B01 and B02 of card 1 (V31-0124) and answer the following study questions.

16. A control address of 304E would indicate statement number _____ of microroutine _____.

17. CSFT118 corresponds with what control address?
    a. 303C
    b. 300E
    c. 3062
    d. 3070
18. What is the control word located at control address 301E?
    a. 8F2C
    b. D961
    c. 4EEf
    d. 4FFF

Answers

1. 2810
2. 0F2A
3. F0B4
4. CKPASS
5. c
6. e
7. h
8. a
9. g
10. b
11. f
12. d
13. False
14. False
15. True
16. 108 CSFT
17. c
18. a

EVALUATION QUESTIONS

The evaluation questions for this topic are located on microfiche card V31-0126, frames A09 and A10.

Please display these frames and answer the questions.

Note: Keep these answers for input on the 2740 terminal at the completion of the next topic. The next topic to be covered will be Clock and Clock Control Circuits, which is Session 3 in this manual. When you have answered all the questions in Session 3, proceed to Session 4.

An answer sheet is provided on the next page for your use.

ANSWER SHEET FOR EVALUATION QUESTIONS ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

INTRODUCTION TO MICROWORDS

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____
11. _____
12. _____
13. _____
14. _____
15. _____
16. _____
17. _____
18. _____
19. _____
20. _____
21. _____
22. _____

SESSION 3 - CLOCK AND CLOCK CONTROL CIRCUITS

This topic will cover the Model 25 CPU time base, the system clock and available timing pulses for controlling the system hardware.

Objective: Upon completion of this topic, the student, using the maintenance documentation and equipment, should be able to:

1.* Determine if a clock or clock control failure exists, using console indications and switches.
2.* Localize and identify the failing component when a clock or clock control failure occurs.

Highlights

- The basic timing pulses for the 2025 CPU are generated by the CPU clock.
- The CPU clock operates as long as the clock start latch is on.
- During the CPU clock cycle, a pulse is available to cause a separate storage clock to operate.
- One CPU clock cycle is 900 nanoseconds long. During one CPU clock cycle local storage can be accessed up to four times.

Activity

Read: The following material on the clock and clock control circuits.

The Model 25 CPU, like any computer, has a need for a systematic flow of data and control information in order to perform operations with consistency and reliability.

This systematic data flow, as you saw in the previous topic, is partially controlled by the microprogram, which is located in storage.

In order for the microprogram to fulfill its duties, the CPU must first provide a method of being able to read out each control word, place it in the C-register, allow the control word to carry out its function, modify the contents of the M-register, read out the control word of the next main storage address, etc.

The necessary timing pulses to set and reset the various registers will be provided by the CPU clock.

Very briefly, the CPU clock is comprised of an oscillator and a five stage latch ring.

Please turn to page 4-11 of the FEMDM.

This page has two parts. One part contains a timing chart and the other contains clock circuitry.

*Partially or totally supported in follow-on lab course.

Looking at the circuit section, locate page coordinate B2 and you will see the free-running crystal oscillator which will provide the necessary pulses to drive the five stage latch ring, which you can see on the right-hand side of the page.

Located in the center of the page, you can see the Clock Off indicator. This indicator is physically located on the console in the CPU status indicator section.

Any time this indicator is on, the CPU clock is not running.

Now that you have familiarized yourself with the logic page, please read two sections in the FETOM entitled CPU Clock and Clock Control.

As you read these sections, follow the operation in the FEMDM that you already have open to page 4-11.

When you have finished the reading assignment, please answer the following study questions.

1. The clock is always stopped with the clock _____ latch on.
2. Each oscillator pulse is _____ nanoseconds in duration.
3. The clock off indicator glows whenever the clock is running. _____ (True/False)
4. In one CPU clock cycle, how many T pulses are generated? _____
5. How long in duration is one P pulse? _____

Now that the clock pulses are available, what can be accomplished?

To best answer that question, consider the following:

1. Depression of the Sys Reset Key causes the CPU to execute the resident micro-programs.
2. It is necessary to address various locations of main storage to place control words in the C-register.
3. The M and W-registers must have the ability to sequentially step through micro-program addresses.

As can be seen, the M, W, and C-registers have to be set and reset to properly execute any microroutine.

One of the functions of the CPU clock is to provide a means of controlling when these registers are set/reset.

Display frames B07 and B08 of microfiche card 1 (Form V31-0124).

This view shows a timing chart relationship of how the CPU clock affects CPU operation.

Notice that when the system reset key is depressed that an address is forced into the M register. This address must be predetermined and to properly execute the resident diagnostics, must always be the first address (C240 indicates a 48K machine).

Another function of depressing the system reset key is to cause the clock start latch to be turned on.

Once the CPU clock starts, it will run from T0 time to T0 time. For the purpose of determining overall clock operation, assume that two clock cycles will be taken.

At T5 time of the first CPU clock cycle, a memory clock cycle takes place. This memory clock is necessary to read out information from main storage and regenerate that data back into main storage. Another way of looking at it would be to say non-destructive read-out.

During this first memory clock cycle, the control word at address location C240 is read out and placed in the control register.

The contents of the control register are then analyzed and a particular operation takes place.

The CPU clock is still running, and, at T0 time, the contents of the M-register (C240) is modified by +2 and placed in the W-register, which will now contain C242.

The program steps sequentially and as can be seen, the W-register does contain the next sequential address.

In order to read out the control word at address C242, this value must first be placed into the M0 and M1-registers.

As the illustration shows, this takes place at P4 time.

Not too long after that, at T5 time of the second CPU cycle, the memory clock is started up again. This time as you will notice, the control word at address C242 is read out of main storage and placed in the control register.

This control word is executed and at T0 time the contents of the W-register are changed to C244; the next sequential address.

This sequential operation will take place as long as the CPU clock is allowed to run.

Other timing pulses of the CPU clock are used for various operations, but before continuing on, please answer the following study questions.

Referring to page 4-24 of the FEMDM or frames B07 and B08 of microfiche card 1 (V31-0124).

6. What clock time determines the set to the W-register? _____

Refer to page 4-21 of the FEMDM to answer question 7.

7. At what time are the M0 and M1-registers set? _____
8. The control register is set at every T0 time. _____ (True/False)
9. The CPU clock time is overlapped by the memory clock time. _____ (True/False)
10. The duration of one memory clock cycle is _____ (450/900) nanoseconds long. (See page 4-27 of the FEMDM.)

CPU clock to local storage relationship.

The local storage, as used in the Model 25, is separated from main storage (refer to the data flow illustration) and is composed of 64 one-byte registers. These locations are used for the intermediate storage of data to be operated on by the Arithmetic and Logic Unit (ALU).

It becomes necessary to move data in and out of local storage dependent upon the particular function of the decode of the microword located in the control register.

Local storage locations are loaded by control words so that required storage addresses and problem factors are made available without readdressing main storage.

During one CPU clock cycle, local storage can be accessed up to four times.

Refer to the timing chart on FEMDM page 4-30.

The timing chart shows a time cycle of P0 - P9 time or one CPU clock cycle.

The top two lines of the chart are labeled Read Line and Write Line.

11. Please notice that the possible read times are P1, P3, _____ and P7.
12. Also notice that the write line can be active during the times of P1, P3, _____ and P8.

These times are adaptable in any combination of four separate times for any basic cycle.

The CPU clock then, performs various functions. First, the main storage addressing of control words is accomplished by clock pulses.

Next, the storage clock(s) function as a result of CPU clock pulses.

Lastly, the accessing of local storage is controlled by the CPU clock.

Please turn to page 4-11 (part 1) in the FEMDM.

Find the Clock Off Latch at page coordinates 5C.

Notice that the Clock Off Latch can be turned on with the line Machine Reset Sw.

The Clock Start Latch, also on this page, can be turned off with the Machine Reset Sw.

With both latches in the above states, there is a circuit available to cause the Clock Off indicator to glow.

Whenever the Machine Reset Sw signal is active, the Clock Off indicator should be on.

The Machine Reset Sw signal is active any time one of the following keys is held depressed in the operated position:

System Reset
Load
Control Storage Load

Upon release of the depressed key, the clock is restarted and the Clock Off indicator should not be on.

From the above, it can be seen that through console switches and indications, it would be possible to detect some malfunction within the clock circuits.

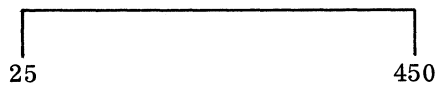
The Clock Off indicator is also on for the following conditions:

1. Hard Stop Latch on - (parity error)
2. Clock Stop Pulse
   a. Mode switch in any single cycle position
   b. A stop control word

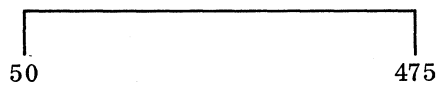
Other indications could also indicate a possible clock failure such as failing to set the M-register, W-register, C-register, etc. Console indications can be useful; do not overlook them.

Answers

1. 5
2. 90
3. False
4. 10
5. 90 nanoseconds
6. T0 Notice on FEMDM page 4-24 that to set the W0 or W1-register:
   1. The heavy dark line indicates the bits 0-7.
   2. The X in the heavy line indicates the set pulse is necessary to gate bits 0-7 to the register latches.
7. P4
8. True
9. True
10. 900 Page coordinates 8A and 8B on page 4-27 (Y24-3529) show the various timing pulses of the memory (storage) clock. 25/240 indicates a pulse that is active from



50/475 indicates a pulse that is active from



Once started, the TD (time delay) allows all pulses to ripple through and become available.

11. P5
12. P6

EVALUATION QUESTIONS

The evaluation questions for this topic are located on microfiche card V31-0126, frames A11 and A12.

Please display these frames and answer the questions. The next page includes space for your answers.

Note: Upon completing the evaluation questions, please follow the directions that are located on frame A13 of the microfiche card.

ANSWER SHEET FOR EVALUATION QUESTIONS ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time. (See frame A13 after completing the quiz.)

CLOCK AND CLOCK CONTROL CIRCUITS

1. _____

2. _____

3. _____

4. _____

5. _____

6. _____

7. _____

8. _____

9. _____

SESSION 4 - CONCEPTS AND PHYSICAL LAYOUT

This topic should give the CE information about physical locations, general layout and information about the speed and general operation of core storage.

Objective: Upon completion of this topic, the student should be able to:

1. Identify the important characteristics of magnetic cores and a core array.
2. Identify the number of BSMs for any given core size, using the FEMM or FEMDM.
3. Identify the starting address and address range for program, control, or auxiliary storage, using the FEMM or FEMDM and the customer core size.
4. State the number of auxiliary blocks available for any given core size, using the FETOM, FEMM, or FEMDM.
5. State the number of bits accessed in core for a normal read or write cycle.
6.* Determine all storage locations during the follow-on lab session.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

CONCEPTS AND PHYSICAL LAYOUT

1. _____

2. _____

3. _____

4. _____

5. _____

6. _____

SESSION 5 - X-Y DECODE

This topic should provide information on address bit breakdown selection of main and auxiliary storage and current drive and selection.

Objective: Upon completion of this topic the student, using the FETOM, FEMM or FEMDM, should be able to:

1. Given an address in program or control storage, identify the X and Y lines necessary to access that given address for a store or read operation.
2. Identify the X line or Y line decode pin entry and exit for a given address in program or control storage.
3. Identify the X and Y lines to access a given address in auxiliary storage for a store or read operation.
4. Identify the X line or Y line decode pin entry and exit for a given address in auxiliary storage.
5. Identify the number of diodes and drive lines on the array necessary to access a given address in program, control or auxiliary storage.
6.* Perform waveform scoping of the core array and be able to identify a bad wave-shape in a BSM during the follow-on lab.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

X-Y DECODE

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____

SESSION 6 - INTERFACE AND GATING

This topic should provide the tie-in between CPU and core storage. It will provide timing relationships and control lines between the CPU and memory.

Objective: Upon completion of this topic the student, using the FETOM, FEMM or FEMDM, should be able to:

1.* Define the timing relationship of the CPU to memory operation.
2. Identify the logical controls for byte operations.
3. Identify the CPU data source for memory on a store byte operation.
4.* Identify the control lines from CPU to memory.
5. State the CPU data source for memory on store halfword operations.
6.* Using oscilloscope and console indications locate and repair CPU memory control line failures.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

INTERFACE AND GATING

1. _____

2. _____

3. _____

4. _____

5. _____

SESSION 7 - SENSE INHIBIT

This topic will provide information on sense inhibit selection, peculiarities or circuits, and storage data register gating.

Objective: Upon completion of this topic the student should be able to:

1. Without documentation, identify how many wires provide sense and inhibit control for each core position in the array.
2. Using the FEMDM, identify the SAR bits controlling the sense amplifier gating to the SDR.
3. Using the FEMDM, identify the SAR bits controlling the inhibit drivers.
4. Using the FETOM, FEMM or FEMDM, state how many sense amps or inhibit drivers feed each bit position of the SDR.
5.* Using maintenance documentation, oscilliscope and console indications, diagnose and repair failures in address decoding.
6.* Using maintenance documentation, oscilliscope and console indications, diagnose and repair sense amplifier and/or inhibit drive failures.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

SENSE INHIBIT

1. _____

2. _____

3. _____

4. _____

SESSION 8 - MEMORY ADDRESSING

This topic will explain the normal storage address register operation, the storage address modifier, and the M-register gating conditions.

Objective: When the system fails to start or proceed from the desired micro operation, and resident diagnostics, non-resident diagnostics and fault locating lists do not isolate the failure, the student, using console indications, FEMM, FEMDM, and oscilliscope, should be able to:

1.* Detect and repair a failure in the M-register to storage address register circuits.
2.* Detect and repair a failure of the trap bits to storage address register circuits.
3.* Detect and repair a failure of the address modifier to modify the SAR bits.
4.* Detect and repair a failure of the W-register to receive an address from the address modifier circuits.
5.* Detect and repair a failure of the M-register assembler to receive data from the W-register.

Highlights

- The address in the M-register or the trap address is directed to the storage address register (SAR).
- The storage address register contains 15 bit positions and are referred to as SAR bits.
- SAR bits are decoded to select the basic storage module, and the necessary X and Y drive lines.
- For each address selected, two bytes are read out of main storage and placed in the C-register.

Activity

Read: The following material on memory addressing.

The ability to read-out or write-in data within main storage can be accomplished if the core locations are accessable.

Because you have already studied the topic on X-Y Decode, it should be clear that all core locations within a basic storage module (BSM) are accessable.

The following text will discuss how main storage core locations are accessed to retrieve the control words that reside there. This session will also explain the method by which the storage address register (SAR) controls the selection of the desired core locations.

*Partially or totally supported in follow-on lab course.

Memory addressing requires the usage of the:

M-register assembler
M-register
Trap address
Storage address assembler
Modify circuits
W-register

For a brief description of the usage of the above mentioned items, display frame B09 on microfiche card 1, V31-0124.

As you refer to the illustration, please read the following descriptions of the units involved.

M-Register

Main storage is addressed from the M-register, a 16 bit register in the processing unit. The M-register is composed of two single-byte registers, M0 and M1, which are fed from the M-register assembler where the actual addresses are constructed.

The M0 and M1-register outputs are gated to the storage-address assembler.

Storage-Address Assembler

The address received from the M-register is routed to the storage-address assembler. Once in the assembler, the information is passed through the storage address register lines. The storage address register (SAR) bits are comprised of 15 address lines which are routed to each basic storage module (BSM). These address lines are then decoded to control the correct X and Y drive lines to read out or write into the cores for a given address.

The storage-address assembler is also used for address substitution in the event of a trap (a forced address to execute a control word routine other than the next sequential word).

The contents of the assembler are replaced with the starting address of the trap routine.

The operation of a trap will be covered in detail in a later topic.

W-Register

The output of the storage-address assembler is presented to a modifier circuit for a modification of +2 and stored in the W-register.

The W-register is a 16 position register (W0 and W1) that holds an updated (+2) address of the control word presently being executed.

The modified output of the W-register is presented to the M-register assembler as the address of the next sequential word to be executed.

C-Register

The C-register is a 16 bit register that is fed from the main storage data-out lines (R0 and R1). This register contains the control word, which is being executed. The output decode circuitry of the C-register interprets the control word bits and conditions the gates, lines and data paths that determine the operation of the CPU for that particular control word.

The above descriptions outline the basic operation of the memory addressing circuits. Now, a detailed sequence of events will be presented, but before continuing on, please answer these self-study questions.

1. Of all the core locations in main storage, how many are accessable? _____ (all/some/none)
2. The modify circuits provide a (+2/-2) _____ update of the contents of the M-register.
3. The M-register contains _____ bits.
4. The SAR bits are only available from the M-register. _____ (True/False)
5. If for some reason, the CPU stopped during the execution of a control word, the address that would be visible in the W-register console indicators would be the _____ sequential address.

Address Generation

Please read the information under the heading M-Register Assembler located in the Functional Units (Chapter 2) Section of the FETOM.

Once you have finished reading, please turn to page 3-3 of the FEMDM.

This page shows the big picture of the data flow necessary for core storage and addressing.

At page coordinates 3B and 4B, you will find the M-register assembler and the M-register assembler gates, which are drawn in red.

As the FETOM mentioned, the M-register assembler can receive information (address) from the control register, A-register, W-register, local storage, console switches, and storage data-out lines.

Please verify that all of these sources have input to the M0 and M1 assembler.

All of these inputs will, at different times, control which address in main storage will be accessed. For this topic however, only be concerned with the inputs that come from the W0 and W1-registers.

As can be seen, the gates (drawn in red) are under control of word types, branch condition, control lines and time. For the purpose of this topic time will be the controlling factor.

If you look inside, the blocks M0, M1 Asm gates, M0 Asm, and M1 Asm, you will see a reference diag 4-20. This is the page number on which these portions of the machine are shown in greater detail.

Please turn to diag 4-20 at this time.

This page contains more detail, but is still recognizable as the M-register assembler gates, M1 assembler and M0 assembler.

Many inputs to the assemblers are shown, but in all cases a gate is necessary to allow any input to pass through.

Locate the M0 assembler. Notice the heavy black line which is drawn as an input to this assembler.

This line is labeled "W0-Reg Bits P-7" and these bits will be allowed through the assembler if the gate line "Gate W0 to M0" is active. Notice that the output of the M0 assembler would be the input for the M0-register.

Now locate the M1 assembler and find the input line which is labeled "W1-Reg Bits P-6." This is the input from the W1-register and it will be allowed to pass if the gate (Gate W1 to M1) line is active. The note inside the block states that bit 7 is forced to 0. The reason for this is that the model 25 reads out halfwords or another way of stating it would be to say that all address locations have an even address, ie, 4040, 32AE, 0042, etc, therefore, bit 7 is not needed.

Locate the large block labeled "M-Reg Assembler Gates" on the left-hand side of the page.

Most of the conditions shown, indicate that control word types determine which gate line is active.

One of the conditions to activate a gate line is shown with no input lines drawn. Instead, the note "When none of the above conditions exist, Gate W0, W1 to M0, M1." Please locate this note.

Notice that the output of this particular block will activate the two gate lines that were needed to allow the W-register information to be allowed to pass through the assembler.

Please answer the following self-study questions.

6. To reach the M-register from the W-register, an address must first pass through the M-register _____.
7. The M1 assembler causes the 7 bit to be forced _____ (on/off).
8. In order for any information to pass through the M-register assembler, a _____ line must be active.

M-Register Operation

Turn to page 3-3 in the FEMDM and locate the M0 and M1-registers at page coordinates 5B.

Notice that the output of the M0 and M1 assemblers directly feed the M0 and M1-registers. All that is required is a set line to each of the registers.

9. The set to the M-register occurs at _____ time.

The output of the M0 and M1-registers goes to the block labeled "Storage Address Asm."

10. As you can see, the output of the storage address assem. is labeled _____ Bits 0-14.

Another input to the storage address assembler is drawn in red and originates in the block labeled "Trap Controls and Addresses."

Normally to start the CPU, a trap address is forced into the storage address assembler. From this point on, all addresses are generated sequentially from the W-register - M-register loop until another trap occurs.

When you wish to take a more detailed look at this section of the circuitry, turn to diag 4-21.

The M0 and M1-registers are shown and as can be seen, the set pulse for both registers is available at P4 time of the CPU clock cycle.

11. The output of the M0-register, bits 0-7 become SAR bits _____.
12. The output of the M1-register, bits 0-6 become SAR bits _____.

Also shown on diag 4-21 is the block labeled "Trap Address." Notice that the trap bits do not use the M0 and M1-registers, but instead are routed directly to the storage address assembler.

Please read the section Storage Addressing, which is located in the Functional Units Section of the FETOM.

SAR Decode

Please turn to page 3-3 in the FEMDM.

Notice that when the SAR bits are avilable, a storage address decode will select the correct X and Y drive lines for the desired main storage core location.

The reference given for a more detailed view of this section is diag 4-27.

If you turn to diag 4-27, you will find that:

1. There are five sections to 4-27.
2. These pages are the same ones that were used during the topic of X-Y decode.

For you to have progressed this far in the course, you must have satisfied the objectives for the topic of X-Y Decode.

Therefore, the usage of these pages and the associated charts will not be covered again in this topic.

Please answer the following self-study questions. If you encounter any difficulty, please refer back to the topic on X-Y Decode.

13. Select the correct Y line pin to the core array which will be utilized for the SAR bits 1288 (HEX).
    a. 37 on A side
    b. 67-106 on D side
    c. 73 on A side
    d. 74 on C side
14. Select the sense amplifiers which will be conditioned for core address hex 1CFE.
    a. 0-8K A Adrs
    b. 0-8K B Adrs
    c. 8-16K A Adrs
    d. 8-16K B Adrs
15. Select the correct X line pin to the core array which will be utilized for the SAR bits 2068 (HEX).
    a. 74 on A side
    b. 37 on C side
    c. 67-106 on D side
    d. 31-142 on D side

Address Modifier

Please turn to page 3-3 in the FEMDM.

Notice that the output of the storage address assem feeds the storage address modifier located at page coordinate 3D.

It is at the modifier that the current address is updated by a value of +2 and this incremented address is directed to the W0 and W1-registers.

The W-register would then present this address to the M-register assembler circuits for the next sequential address.

All of these circuits are shown in greater detail on page diag 4-24.

At this time, please turn to that page.

The W0 and W1-registers are located on the right-hand side of the page.

Notice that bit 7 in the W1-register is always 0.

16. The W-register receives a set pulse at the CPU clock time of _____.

The data inputs to both the W0 and W1-registers originate at the block labeled Storage Address Modifier.

The heavy black line leading into the modifier block would be the SAR bits or Mem Addr Bits 0-14.

The note inside the modifier block states that a 0 modify operation could take place. This is correct, however, the only time a 0 modify is used is in the execution of special control words that require two CPU memory cycles to execute their function.

Also located on this page is the Modifier Parity Predict circuitry, which will simply insert the necessary parity to accommodate the new modified address.

Please answer the following self-study questions.

17. The correct source of data for the W-register is the:
    a. C-register
    b. M-register
    c. A-register
    d. Storage Address Modifier
18. The W0 and W1-registers transfer _____ (14, 15, 16) bits to the M-register assembler. (DO NOT INCLUDE PARITY.)

C-Register

Refer to page 3-3 of the FEMDM.

In the lower right-hand corner of the page, the storage data register (SDR) is shown. The SDR receives the desired control word from main storage and then places it on the storage data outlines (R0 and R1 bus).

Look at page 3-2 in the FEMDM and locate the control register.

Drawn as the input to the C-register is the storage data out bits 0-15.

19. The set line to the C-register is derived from the block labeled _____ cycle.
20. Control cycle includes the system clock timings which allow the C-register to be set at _____ time.

Once the control word is placed in the C-register, it becomes decoded and begins to perform its assigned task.

Looking at the various blocks drawn off the output of the C-register, it becomes apparent that the bit breakdown of the control word is extremely important.

Answers

1. all
2. +2
3. 16
4. False - Trap addresses can also be sent to the storage address register.
5. Next - The M-register would contain the current address of the control word being executed, however, the W-register contents would have been modified by +2.
6. Assembler
7. off
8. gate
9. P4 - Refer to frames B07 and B08 of microfiche card 1, Form V31-0124.
10. SAR
11. 0-7
12. 8-14
13. 37 on A side
14. 0-8K B Adrs
15. 31-142 on D side
16. T0
17. Storage Address Modifier
18. 15
19. Control
20. T0

EVALUATION QUESTIONS

The evaluation questions for this topic are located on microfiche card V31-0126, frames B09 and B10.

Please display these frames and answer the questions. The page after this one is provided for quiz answers.

Note: Upon completing the questions, please sign on the 2740, so that your answers may be checked. The next topic to be covered will be Local Storage, which will be presented via the 2740 terminal.

ANSWER SHEET FOR EVALUATION QUESTIONS ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

MEMORY ADDRESSING

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____

SESSION 9 - LOCAL STORAGE

This topic covers the local storage area of the CPU. It describes the characteristics and location of local storage and the addressing of this area. Console access to this area is also covered.

Objective: Using the FETOM, FEMM and FEMDM:

1.* Identify the physical characteristics and locate the local storage card in the CPU.
2. Identify the X and Y coordinates for any specific local storage register.
3. Given the X and Y lines and a local register, identify the zone the CPU is operating in.
4.* Given a specific hex value, use the console switch settings to display or alter a local storage register.
5.* Upon completion of this lab project, the student, using the maintenance documentation, should be able to:
    1. Identify correct or incorrect operation of local storage.
    2. Draw waveforms of correct signals to and from the local storage card.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

LOCAL STORAGE

1. _____

2. _____

3. _____

4. _____

5. _____

SESSION 10 - A-AND B-REGISTERS

This portion of the course describes the various functions, source inputs, outputs, timing considerations and operations performed by the A-and B-registers.

Objective: Using a combination of the following:

a. FEMDM
b. MAS Listings
c. Data Flowchart
d. Console display operation
e. ALD
f. Oscilliscope

the student should be able to:

1.* Determine if the A-and/or B-register(s) received data from the source specified by the contents of the control register.
2.* Determine if the A-and/or B-register(s) correctly performed the gating of data to ALU.
3.* Localize and replace the failing component when the A-and/or B-register(s) do not receive the correct data or fail to provide ALU with the necessary input to correctly execute any given control word.

Highlights

- The A-and B-registers provide the only input to the Arithmetic Logic Unit (ALU).
- A-register data can be gated to ALU seven different ways.
- B-register data can be gated to ALU five different ways.
- The A-and B-registers can receive data from five different sources.

Activity

Read: The following material on A-and B-registers.

The Model 25 CPU can perform many varied arithmetic operations. These operations are performed in the Arithmetic Logic Unit (ALU).

The only data input to ALU comes from the A-and B-registers.

Although the A-and B-registers can receive data from different sources and have the ability to gate data to ALU in various ways, it is the control register contents that control:

a. The source data for the A-and B-registers.
b. How the A-and B-register data will be gated to ALU.
c. The arithmetic operation to be performed on the data.
d. Where the resultant data will be stored.

*Partially or totally supported in follow-on lab course.

In short, the control word provides a means of arithmetic and logical operations and a control over data distribution gating.

In the FETOM, please read the section AB-Register Assembler, in Chapter 2. It may be helpful if you refer to the overall data flow illustration while reading.

1. The AB register assembler receives data from many sources and gates data to the A-and B-registers and to _____ circuits.

External facilities can be gated through the AB assembler to the A-and B-registers. The A-source decode of the control word determines which external will be gated.

2. Control words that have an A-source field are word types _____, _____, _____ and _____.
3. Whenever an unconditional branch word (Word Type 4) or a set/reset word (Word Type 0) with a link function is executed, the AB assembler receives data from the _____ register.
4. Local storage data can also be gated to the AB assembler. _____ (True/False)
5. Bits _____ through _____ of the control register are gated to the display circuits when a display control register operation is being executed.

Many of the control word operations furnish data to the AB-register. At this time, the specific operation of each type of control word has not been covered.

The most important fact to remember thus far is that for data to reach the A-and B-registers, the AB assembler must first be passed through.

At this time, open the Field Engineering Maintenance Diagram Manual to the diagram entitled AB-Register, ALU, EXT Facility in Data Flow.

On the left-hand side of the page is AB assembler.

Notice the AB asm gates (drawn in red). These conditions allow one of the data inputs (drawn in black) to be presented to AB assembler.

To see a more detailed illustration of the AB assembler, turn to diagram 4-35 (part 1 of 2).

On the right side of the page is the assembler and on the left side the various control gating circuits are shown.

Six gating conditions are shown and are labeled.

1 - Gate K to AB
2 - Gate LS to AB
3 - Gate M to AB
4 - Gate External to AB
6. 5 - Gate _____ to AB
7. 6 - Gate _____ to AB

Regardless of the gate that is active, the AB assembler will allow data to pass through to be presented to either the A-or B-register.

The A- and B-registers are located on part 2 of 2 of this same diagram.

Notice the data input to the A- or B-register is received directly from the AB assembler.

Of course, it is necessary to activate the set lines to the register before any data can be accepted.

Both the A- and B-registers can have their set lines activated manually (Man Set AB), but notice that when the system clock is running, specific times are set aside to allow the A- or B-register to receive data from the assembler.

8. The A-register has the ability to be set at _____ time and _____ time.
9. The B-register has the baility to be set at _____ time and _____ time.

Once data is available in the A- and/or B-registers, the manner by which the data is gated to ALU becomes quite important.

Read the sections entitled A-Register and B-Register in the FETOM.

The only source of input to ALU is from the A- and B-registers. To be able to send any data through ALU some specific conditions must be met.

10. Earlier in this session, it was pointed out that the _____ _____ controls how the A- and B-register data will be gated to ALU, or more specifically, the Adder.

A very good illustration of gating A- and B-register contents to ALU is on FEMDM diagram 4-36 (part 1 of 2). Please turn to that page now and locate the blocks entitled A-Reg Entry Gates to ALU and B-Reg Entry Gates to ALU.

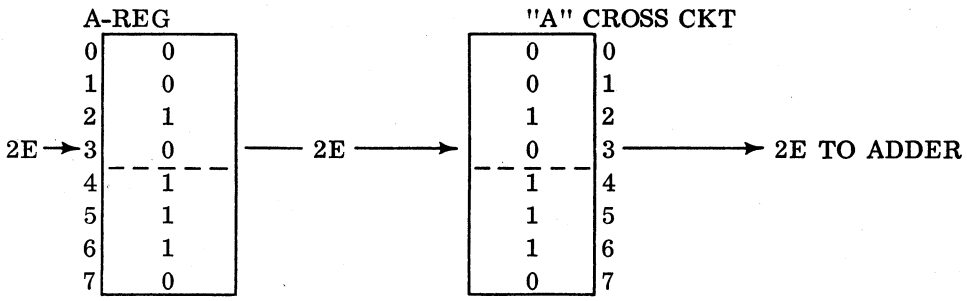
The inputs to these blocks are almost exclusively dependent upon control word types or control register bits.

Dependent upon the control register contents, the A- and B-registers can gate the data in many ways.

Referring to diagram 4-36 (part 1 or 2), please read the sections in the FETOM entitled A-Register Gating and B-Register Gating.

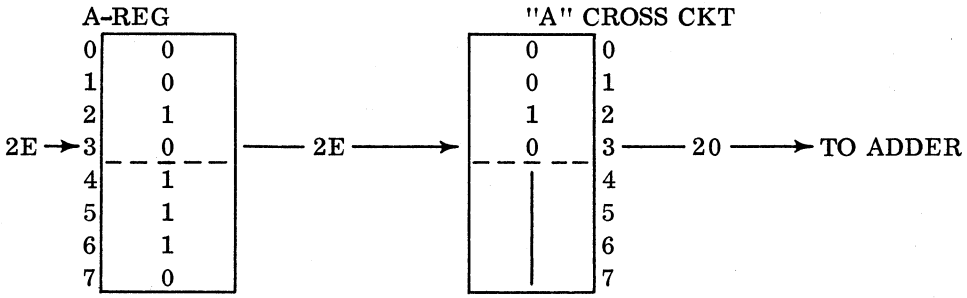
Examples of gating of A- and B-register contents to the adder follow.

A-Register Straight



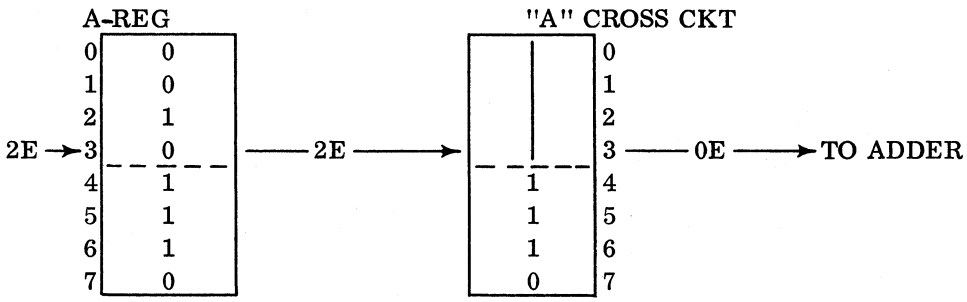
The Adder receives data exactly as it was contained in the A-register.

A-Register High



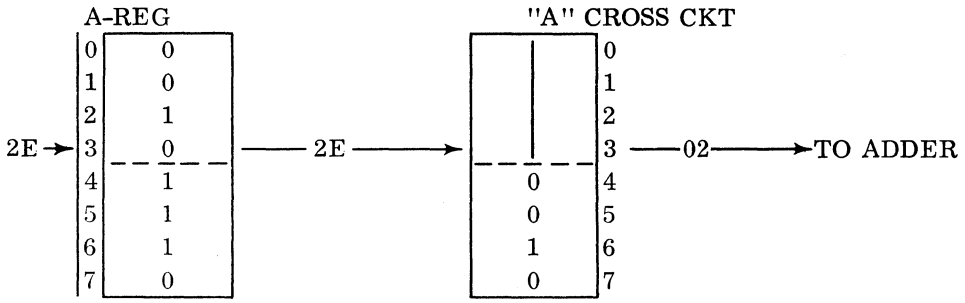
The high four bits of the A-register contents is allowed to pass to the adder, but the low four bits are blocked.

A-Register Low



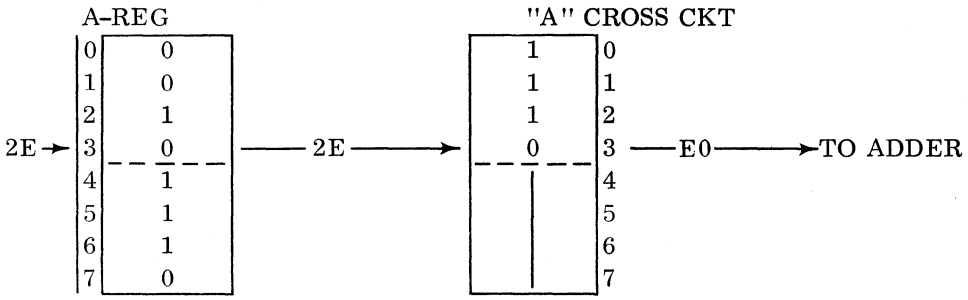
Gate low four bits of the A-register to the low four bits of the adder, block the high four bits.

A-Register Crossed Low



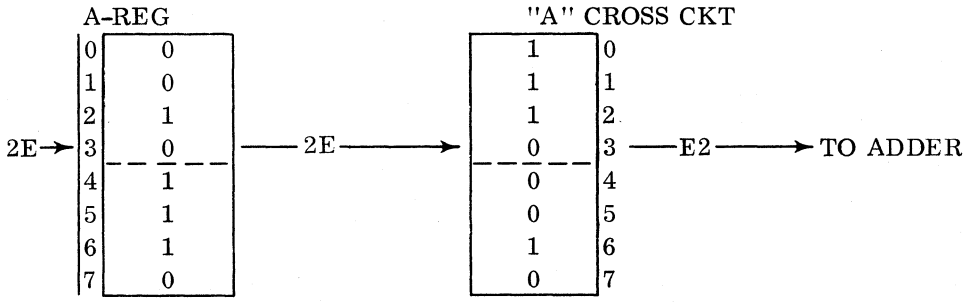
Gate the high four bits of the A-register to the low four bit input to the adder, block the high four bits.

A-Register Crossed High



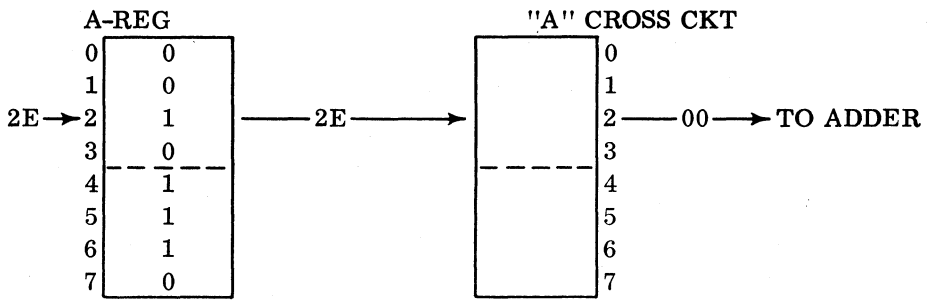
Gate the low four bits of the A-register to the high four bits of the adder, block the low four bits.

A-Register Crossed

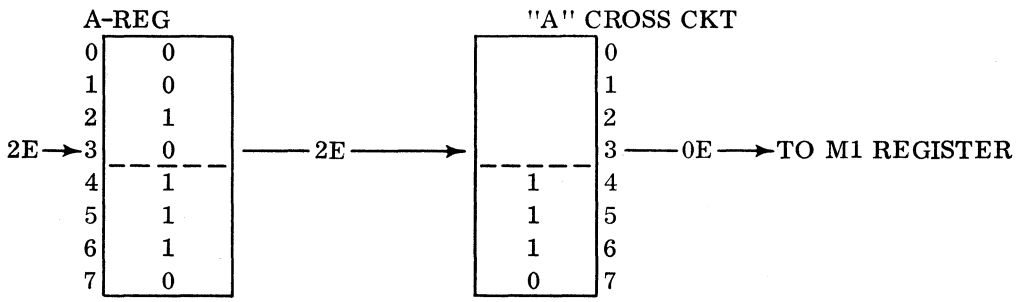


Gate the low four bits of the A-register to the high four bits of the adder, gate the high four bits of the A-register to the low four bits of the adder.

A-Register Blocked

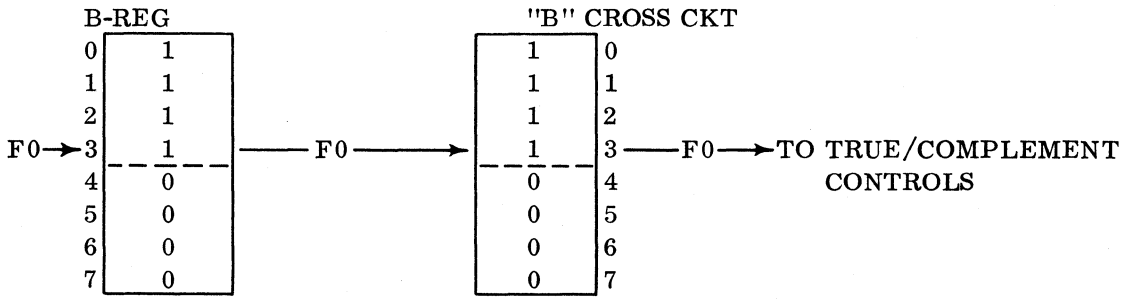


Block the A-register input to the adder.



The low four bits of the A-register are gated to the M1-register for "Branch on Mask" control word operations. (Word Type 5)

B-Register Straight



Gate bits 0-7 of the B-register to bits 0-7 of the true/complement controls.

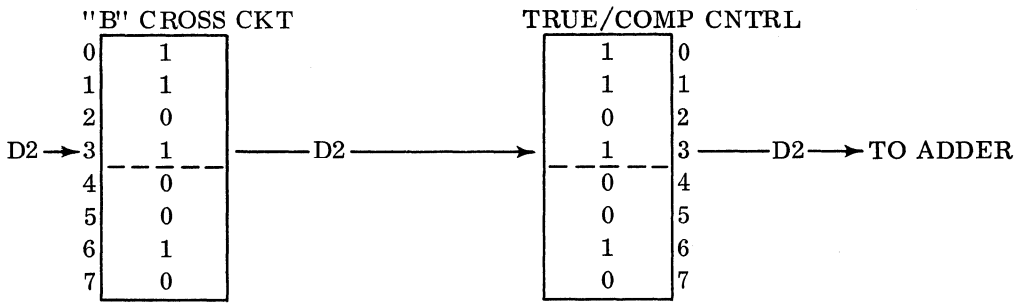
B-Register High

Same as A-register. (Data sent to true/complement controls.)

B-Register Low

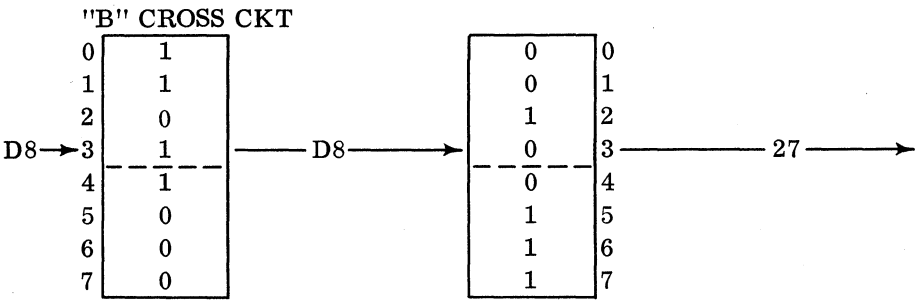
Same as A-register. (Data sent to true/complement controls.)

True/Complement Controls - True Control Active



Gate B-register contents undisturbed to the adder.

True/Complement Controls - Complement Control Active



Contents of the B-register are inverted and gated to the adder.

All of the preceding examples of gating A-and B-register data to ALU are dependent upon the content of the control register bits.

Later in the course, each word type will be explained in detail. At that time, a number of examples for each word type will be given and for each example, the motion of data through the AB assembler and AB-registers will be illustrated.

Answers

1. Display
2. 1, 3, 5 and 6 or 7
3. M1
4. True
5. 8, 15
6. Sw AB
7. Sw CD
8. T1, T5
9. T3, T7
10. Control register

EVALUATION QUESTIONS

The evaluation questions for this topic are located on microfiche card V31-0126, frames B15 and B16.

Please display the quiz and answer the questions. For your convenience, an answer sheet follows this page.

Note: Upon completing the questions, please sign on the 2740 so that your answers may be checked. The next topic to be covered is ALU which will be presented via the 2740 terminal.

ANSWER SHEET FOR EVALUATION QUESTIONS ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

A AND B REGISTERS

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____
11. _____
12. _____
13. _____
14. _____

SESSION 11 - ALU

This topic will introduce the CE to the arithmetic logic unit, the functions performed, and the external controls required.

Objective: Upon completion of this topic the student should be able to:

1. Using the FEMDM, identify the five bits in the control register that control an ALU function.
2. Using the FEMDM, identify which control lines are active for any given ALU function.
3. Using the FEMDM, locate the defective circuit or control for any given ALU failure.
4. Using the FEMDM, list the components used for the correction function during decimal addition.
5. Using the microprogram listing and given the incorrect result of an ALU operation, locate the failing microstep.
6. * Using the maintenance documentation during follow-on lab, diagnose and repair failures in the ALU logic of the 2025 involving binary and decimal operation.
7. * Enter a given microprogram which allows scoping of ALU when binary and decimal operations occur.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

ARITHMETIC LOGIC UNIT

1. _____

2. _____

3. _____

4. _____

5. _____

SESSION 12— EXTERNALS

This topic will describe external register access, addressing, locations and methods of data handling in the CPU.

Objective: Upon completion of this topic the student should be able to:

1. Using the FEMM, identify the external A-source decodes that can be tested with a branch-if microstatement.
2. Using the microprogram listing, identify the external registers which are displayable.
3. List the external registers which can be tested for branch in any external mode, using the FEMM.
4. Using the FEMDM, identify the external mode when given the contents of the mode register.
5. List the switch and its position to display any given external register, using the microprogram listing.
6. Given an I/O request condition and using the FEMDM, identify the conditions of the S7 and the BB1 bits.
7. Using the overall flow diagrams in the FEMDM, identify the busses which are parity checked.

This topic is an on-line topic presented via the FSS terminal.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

EXTERNALS

1. _____

2. _____

3. _____

4. _____

5. _____

6. _____

7. _____

SESSION 13 - WORD TYPE 0

This topic will introduce the microprogramming concepts and specific information about word type 0. Also included will be coding rules and functions.

Objective: Upon completion of this topic the student, using the maintenance documentation, should be able to:

1.* Using the FETOM, MAS listings, and console indications, the student should be able to identify and analyze the word type 0 when used as:
   a. a set/reset word.
   b. a link word.
   c. a RTN word.
2. Using the bit significance chart for a word type 0, the student should be able to convert a mnemonic statement (WT0) to its equivalent hex notation.
3. Using the bit significance chart for a word type 0, the student should be able to convert a hex control word (type 0) to its equivalent mnemonic statement.
4. Identify the assumed operands for a RTN word which has no coded operands.

Highlights

- Defined as a set/reset word (control bits 0, 1, 15 = 0).
- Sets or resets bits of a designated external facility.
- Stores a link address into local storage when used as a link word.
- Retrieves a link address from local storage when used as a return word.

Activity

Read: In the FETOM in Chapter 3, the following:

Microprogram Concepts
Microprogram Functions
Microlistings
Control Storage Load

Most of what was contained in the reading assignment was probably not new to you. The main purpose of reading those sections was to reorient you to the microlisting and microprogram terminology and basic operation.

Starting with this topic, the various types of control word types will be covered in detail. This topic will concern itself with word type 0, the set/reset word.

At this time, please turn to the Bit Significance Chart for Set/Rst Word (Word Type 0) located in the FETOM (Y24-3527).

This chart shows the 16 bit breakdown of a word type 0.

*Partially or totally supported in follow-on lab course.

In studying the chart, please answer the following self-study questions.

1. In determining the type of any control word, which bit positions are defined as the word-type field? _____
2. What would be the value of these bit positions if a word type 0 was identified?

   _____
3. The basic function of a WT0 (set/reset) is to set on or reset off bits in designated external registers. Which bit position determines if the set or reset function will be performed? _____
4. Bits 4, 5, 6, and 7 are designated as the _____ Source _____.
5. Dependent upon the configuration of bits 4-7, various external registers can be designated. Which external is designated with the bit structure of 0010 in the Set/Reset Source Field? _____
6. If the following bit structure was given for a WT0, the operation that would be identified would be:

Bit	0	1	2	3	4	5	6	7
Value	0	0	0	0	0	0	0	0

   a. set mode register.
   b. set DR register.
   c. reset MMSK register.
   d. reset S-register.

When a WT0 is being used as a set/reset word (instead of a link or RTN word), bit positions 8, 9, 10, and 11 are called by the K-low field.

Bits 3, 12, 13 and 14 are always referred to the K-high field.

What is K?

The symbol K simply means constant.

Notice on the bit significance chart that the K bits are not located in one group. These K bits, when referred to, are read in a special manner. Consider the illustration shown on frame C01 of microfiche card 2 of V31-0124.

In the illustration, the bits of the K-high and K-low fields combine to form a specific value. In this case, the high order value of the K-byte is C and the low order of the K-byte is 6.

In the mnemonic statement "SET SK = 84" would be defined as: set the S-register bits specified by the corresponding bits of the K field, whereas the K field is 84.

To elaborate on this for just a bit, consider the following.

The major function of the set/reset word is to set or reset specified bits of a designated external facility. The bits to be set or reset are designated by the corresponding bits of the K field.

For Example:

K field	=	3A (Hex)							
Source Bits Affected	=	0	1	2	3	4	5	6	7
				↑	↑	↑		↑	
K Bit Structure	=	0	0	1	1	1	0	1	0

Most external facilities that can be addressed by the WT0 are affected on a bit basis. That is to say, only the bits of the external for which there is a corresponding bit in the K field are set or reset.

Very good examples of this are shown in the figure entitled K Field Function Set/Reset Word in the FETOM.

Study that figure at this time.

7. Concerning bit sensitive external facilities; all bits in the register will be affected regardless of the value of the K field. _____ (True/False)

Not all external registers are bit sensitive. Some external facilities are affected on a byte basis.

If the statement "SET MODE K=22" was executed, the result would be as follows. Assume the mode register contains FF prior to execution of the above.

Since the mode register is affected on a byte basis, the entire register will assume the status indicated by the K field; in this case after execution, the mode register will contain 22.

Also included in the diagram K Field Function Set/Reset Word are examples of K field use with external register that are affected on a byte basis.

A question you might ask is, "How can I tell which external registers are affected by byte and which are affected by bit?"

That would be a very good question and for the answer, please turn to the figure entitled Set/Reset Word Source Mnemonics located in the FETOM.

Those registers that are preceded by an asterisk are affected on a byte basis. That is to say the K value is set directly into the facility addressed. All others shown in the chart are bit sensitive and only the corresponding bits of the K field are changed.

This figure brings to mind a few situations that should be mentioned at this time.

Across the top of the figure the various modes of the Model 25 are indicated.

8. As you recall, the operating mode of the CPU is designated by the contents of the _____.

Depending on the operating mode of the CPU, the Set/Reset Source Field of the control word has the ability to address a specific external facility.

If the CPU was operating in 1403 mode and the microprogram executed the control word, which had a source field decode of 0000, the S-register would be the addressed facility. In fact, with a source field decode of 0000, the S-register is always the addressed facility regardless of the CPU mode.

9. If, for example, the CPU was operating in channel mode, and the microprogram executed a control word with a source field decode of 1111, the addressed external facility would be the _____ register.

Notice that for a Set/Reset Source Field decode of 1111, the register that has its contents altered changes according to the operating mode of the CPU.

In order to determine if a set/reset word was executed properly (displaying the contents of the external register affected), it must first be determined which operating mode was active at the execution time of the control word.

The mode register determines the operating mode unless the MMSK register contents indicate a higher priority.

Once the operating mode is known, the external register being affected by a set/reset word can be determined.

10. What affect would the statement "RST BC K=11" have on the BC-register?
    a. BC-register will be set to a value of 11.
    b. BC-register will be reset to a value of 11.
    c. BC-register bits 3 and 7 will be set off; all other bits will be unaffected.
    d. BC-register bits 3 and 7 will be set on; all other bits will be unaffected.
11. The mnemonic statement "SET S K=84" converted to hex would be _____.
12. The mnemonic statement "RST R K=00" converted to hex would be _____.
13. To reset the R-register, what CPU operating mode is indicated?
    a. CPU mode
    b. 1052 mode
    c. 2311 mode
    d. 2540 mode

In the FETOM, locate the figure entitled Set/Reset Word External Bit Assignment.

This figure has seven parts and indicated on these charts is the manner by which the set or reset function of a WT0 will affect the various addressable registers.

These charts are very effective in quickly determining the status of the external facilities.

At this time, please turn to diagram 5-1 in the FEMDM.

As you know by now, the control register, when decoded, causes the control word to be executed. Shown on diagram 5-1 is the way by which the S-register is affected by the control word of 3040.

Please study this diagram and notice that the ALD page is shown under each of the blocks.

When you have studied diagram 5-1 and are satisfied, turn to diagram 5-3.

This diagram shows the operation of a WT0 upon a byte sensitive register.

This covers the major function of the set/reset word type 0. Two more functions can be performed by this word type and these will be covered at this time.

Please display frames C3 and C4 of microfiche card 2 (V31-0124).

What is shown here is an example of the CPU operating in a sequential manner upon control words stored in address 0000, then 0002, then 0004, etc. As can be seen, an alteration in normal continuous operation is shown when 0006 is reached. This change in operation shows the 2540 Punch interrupting the normal flow. This operation can occur because the 2540 has a higher priority than does the CPU. For example, a card moving along in the 2540 must be punched at the proper time. Since the card is under mechanical control, it would be impossible to stop the card in mid motion, hence the 2540 is allowed to cause a trap in order to cause specific microwords to be acted upon, ending in a resultant punching operation.

In the CPU mode program, however, it can be seen that the operation was interrupted prior to 0008.

When the trap is concluded, in order for the CPU to continue with its original operation, address 0008 somehow must be accessed.

What then is the purpose of control word type 0 in this type of trap routine?

To answer that question, consider these following points:

1. During an I/O trap routine, the MMSK register overrides the mode register.
2. The mode register contents are not disrupted during the trap.
3. Control of addressing is turned back to the mode register at the conclusion of the I/O trap and when the MMSK register latch(es) is/are reset.
4. Traps bypass the normal core storage addressing circuits.
5. A trap address is the starting address of a trap handling microroutine that operates on the particular trap allowed.
6. Traps are allowed on a priority basis.

Before continuing on too far, it should be pointed out that an entire topic is devoted to traps and will be presented at a later time.

The purpose of discussing traps in this topic is to show the relationship of the set/reset word when used under trap conditions.

When a trap or nonscheduled break in the normal operation of the system occurs, the control storage address of the microroutine designated to handle that trap is forced into the storage address assembler. The control word located at that forced address is read out and executed.

The first control word of a trap routine is usually the link word; a function of WT0.

Notice on the microfiche display the mnemonic statement shown as the first word of the trap routine is "LINK U MMSK 4=1."

14. If this mnemonic statement was shown in its equivalent hex notation, it would be 2208 which is a word type _____.

The statement LINK U MMSK 4=1 will cause certain operations to take place. These are:

1. The address contained in the M-register (0008) is caused to be stored in the U-register of local storage zone 4.
2. Set on bit 4 of the MMSK register.
3. Save the status of the dynamic condition register.

15. The reason 0008 is saved is because this is the address of the _____ control word that would have executed if the trap had not occurred.
16. Upon completion of the trap, the next address to be acted upon will be _____.
17. This address is being saved in the _____ register, which is located in LS zone 4, which is called the _____ zone.
18. To override the mode register, a bit in the _____ register must be set on.
19. The bit to be set on is the _____ bit.
20. What does this bit cause when set to a one? _____

The status of bit 3 of the dynamic condition register is stored in bit 7 of the U1-register. Also bits 6 and 7 of the DYN register are stored in bit positions 0 and 1 of the U0-register.

The status of these latches are thusly saved in the U-register and upon completion of the trap, the DYN register has the ability to have those same status conditions re-established.

Right about this time, a question should be in order.

In case the question that should be asked is not apparent, consider this; "How can status information be saved in the U-register if the address 0008 is also being stored in the U-register?"

Display frame C05 on microfiche card 2, V31-0124.

This illustration shows the address of 0008 being stored in the U-register.

Also shown is that U1-register bit position 7 is available to store the status of the DYN register bit 3. In fact, because all control words in the Model 25 are halfword (even) addresses, this particular bit position is free to use for any purpose on a temporary basis.

Bit positions 0 and 1 of the U0-register also may be used temporarily to store data (DYN bits 6 and 7) because these two high order bit positions are dependent upon the size of the storage available. For example, assuming that a 16K system was being used, the contents of these two bit positions would be forced to a value of 01 when its contents reached the M-register, 10 for a 24K machine and 10 for a 32K machine.

21. What would these bit positions be forced to (in the M-register) for a 48K machine?

_____

In summary, the usage of U0-register positions 0 and 1, and U1-register position 7 may temporarily be used to store or save the status of the DYN register when a trap occurs.

The address of the next control word (after the trap) to be executed is saved in the U-register, and the MMSK register has its contents changed to allow the correct LS zone and external gating controls to provide the necessary data paths for the execution of the trap routine.

Again, the statement "LINK U MMSK 4=1" indicates that the U-register is being used to save data. It is possible that more than one trap can cause an interruption in the CPU operation.

In this case, data (next address to be executed on completion of the trap) must be stored to allow for continuous system operation.

Please display frames C7 and C8 of microfiche card 2, V31-0124.

This illustration shows how the CPU is caused to detour from its original execution in order to honor a trap from a device.

This device causes what will be referred to as a "level 1 trap." The link statement shown is LINK U MMSK X=0 indicating that the U-register is used in this first level trap. Before the level 1 trap can complete its required operation, another trap of higher priority (level 2) occurs. At this point, the next sequential address of the level 1 trap must be saved. The statement LINK V MMSK X=0 is used. The U-register now contains backup address data. Before the level 2 trap can completely execute, a third trap takes place.

22. This would be referred to as a level _____ trap.
23. The register used for backup (the next sequential address of level 2 before the third trap occurred) in this case would be the _____ register.

In fact, certain registers are always used for saving address data when a link word is used.

Refer to the Bit Significance Chart for Set/Reset Word in the FETOM.

Bit positions 8, 9, 10 and 11 determine the register in LS that will be used in a save address operation.

To carry this one step further, the following table indicates the usage for each of the registers listed.

0000 = U-Register = Level 1 Backup
0010 = V-Register = Level 2 Backup
0100 = G-Register = Level 3 Backup
0110 = D-Register = Machine Check Backup
1000 = I-Register = CPU BAL Backup
1010 = T-Register = Spare
1100 = P-Register = Level 1 Working Area
1110 = H-Register = Level 1 Working Area

Refer back to the microfiche illustration. (Frames C06 and C07 of card 2)

Notice that the last statement of a trap routine are words RTN G MMSK X=0, RTN V MMSK X=0, RTN U MMSK X=0.

These words are the special return function of the set/reset word.

When executed, the return word causes the return to the interrupted microroutine in the following manner.

1. The address stored in the G-register of LS zone 4 is read out and placed in the M-register.
2. The status of bits 3, 6 and 7 of the dynamic condition (DYN) register, prior to the trap, is retrieved from the G-register (LS zone 4) and restored into the DYN register.
3. The MMSK register latch that was being used is reset, which returns the CPU to the mode of operation before the third level trap occurred.

Upon completing the level 2 trap requirements, the last control word encountered in that routine would be RTN V MMSK X=0. This causes the information in the V-register to be restored back to the M-register and DYN register. The MMSK bit used is also reset.

This operation continues until the MMSK register has no bits on and the machine is back under control of the mode register. This would place the operation back in CPU mode with no traps pending.

24. The mnemonic LINK G MMSK 1=1 converted to hex notation would be:
    a. 2208
    b. 0222
    c. 2242
    d. 0242
25. The hex word in hex of 0208 converted to a mnemonic statement would be:
    a. RTN G MMSK 0=0
    b. LINK G MMSK 0=1
    c. RTN U MMSK 4=0
    d. SET MODE K = 40
26. The _____ register is used for the level 2 backup register.
27. Bit positions _____, _____, _____ and _____ of the control word specify the LS register that will be used for backup.
28. When a trap is initiated, the status of the DYN register is last and possible arithmetic errors can result. (True/False) _____

Sometimes the statement RTN may be encountered in a microroutine. Upon first glance, it may seem that something is missing from the above statement. Something is missing and it is the operands. This statement causes the special function of the set/reset word to be performed.

The RTN word is generally used to return to a microroutine that had been branched to and linked from, using the address from the CPU backup register.

The branch and link (BAL function) will be covered in detail during the presentation of word type 4.

The operation is the same as for an exit from a trap routine except that the I-register is used as the backup of next address and reinstatement of DYN register status.

There is one more usage of the set/reset word.

In the FETOM, find and read the descriptive text given for the example statement of "SET MMSK K=31."

As shown, "SET MMSK K=31" or 2216, whichever is preferred, used the control word bit 11 for a specific purpose.

29. If the bit is off a _____ or _____ function is indicated.
30. Bit 11=1 is used to _____ the RTN or restore of the M-register.

In summary, the set/reset word can perform various functions. In the FETOM, read over all of the examples given for this word type.

At this time, please turn to diagram 5-2 in the FEMDM.

Shown on this page is a graphic circuit illustration of the WT0 statement "LINK U MMSK 4=1."

In the lower right-hand corner of the page, the objectives for this operation are shown; please read these objectives.

A timing chart is also shown indicating the events that occur during the CPU clock cycle time required for the execution of this word.

Study the circuit and its timing chart and answer the following self-study questions.

31. In the timing chart, it can be seen that the trap address is made available to the storage address register and at that time the M-register contains what would have been the next instruction or the _____ address.
32. The next thing to do is save the contents of the M-register. The M1-register contents (high link address) are sent to the _____ register after passing through the LS data assembler.
33. The DYN register bits _____ and _____ also pass through the LS data assembler during the first half of the clock cycle.
34. Shortly thereafter, the contents of the M1-register are directed through the _____ before reaching the LS data assembler.
35. The DYN bit _____ is also directed to the A-register through the AB Assembler.
36. About the middle of the clock cycle, the MMSK _____ latch becomes turned on to activate the _____ _____ trap lines.
37. Near the end of the cycle, the address that is contained in the M-register, which will be the next word to be executed is the trap address _____.

All of the functions for the objectives of this statement are shown on this page.

Using the information shown here should be of great assistance when trying to find a starting point if a link word is suspect of failing to execute properly.

Answers

1. Bits 0, 1 and 15
2. Bit 0=0, bit 1=6, bit 15=0
3. Bit 2
4. A-Source Field
5. MMSK register
6. Choice d is correct. A reset operation is defined because bit 2=0, the S-register is affected because bits 4, 5, 6, 7 = 0000.
7. False. Only the corresponding bit of the K field to external registers are affected.
8. Mode register
9. GC
10. Choice c is correct. Since the BC register is a bit sensitive register (see Figure 3-4, FETOM), only the corresponding bit positions in the K field will be reset.
    K field = 11 = 0001 0001
    All other bit positions remain unchanged.
11. 3040
12. 0B00
13. 2540 mode
14. Word type 0
15. Next
16. 0008
17. U, Backup
18. MMSK
19. 4
20. MMSK latch 4
    Significance = 2540 Punch Priority
    Forces LS zone 110 (2540) and external gating control 010 (2540 Punch mode)
21. 11 or C
22. 3
23. G
24. Choice c (2242). See the examples given in the FETOM for set/reset word.
25. Choice c (RTN U MMSK 4=0). See the examples given in the FETOM for set/reset word.
26. V
27. 8, 9, 10, 11
28. False, the DYN status is saved in the backup register in bit positions 0, 1 and 15.
29. Link, return
30. Suppress
31. Link
32. U0
33. 6 and 7
34. A-register
35. 3
36. 4, 2540 Punch
37. +2

This concludes the topic of the set/reset word phase.

EVALUATION QUESTIONS

The evaluation questions for this topic are located on frames C03, C04, and C05 of microfiche card V31-0126.

Please display those frames and answer the evaluation questions at this time. The following page is an answer sheet for your convenience.

Note: Upon completing the questions, please sign on the FSS terminal so that your answers may be checked. The next topic to be covered is Word Types 1, 3, and 4, which will be presented via the FSS terminal.

ANSWER SHEET FOR EVALUATION QUESTIONS ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

WORD TYPE 0

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____
11. _____
12. _____
13. _____
14. _____

SESSION 14 - WORD TYPE 1

This topic will cover the microprogramming concepts and specific information concerning word type 1. Also included will be coding rules and functions.

Objective: At the completion of this topic, the student should be able to:

1. * Using the FETOM, identify the specific function that a word type 1 performs.
2. * Given a list of control words, select all words which are word type 1.
3. Using no reference, identify the two operands of a word type 1.
4. Using the MAS listing, identify the mnemonic statements that allow for the three possible variations of data gating when executing a word type 1.

   Using the Bit Significance Chart for word type 1:

5. Convert a mnemonic statement for a word type 1 to its equivalent hex notations.
6. * Translate an arithmetic constant hex word to its mnemonic equivalent.
7. Create a hexword to perform any arithmetic function possible with a word type 1.
8. * Using the FEMDM and console error indications, analyze the operation of a word type 1 execution as it affects or is affected by:
   a. Timing conditions
   b. Data flow
   c. Storage utilization

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

WORD TYPE 1

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____
11. _____
12. _____
13. _____
14. _____

SESSION 15 - WORD TYPE 3

This topic will cover the microprogramming concepts and specific information concerning word type 3. Also included will be coding functions and rules.

Objective: At the completion of this topic, the student should be able to:

1.* Using the FETOM, identify the function that a word type 3 performs.
2.* Given a list of control words, select all words which are word type 3.
3. Using the Bit Significance Chart for a word type 3, identify:
   a. two operands for the arithmetic function of a word type 3.
   b. two operands for the move function of a word type 3.
4. Using the MAS listing, identify the mnemonic statements that allow for variations of data gating when executing the word type 3.
5. Convert a mnemonic statement for a word type 3 to its equivalent hex notation.
6.* Translate a move/arithmetic hexword to its mnemonic equivalent.
7. Create a hexword to perform any move/arithmetic function possible with a word type 3.
8.* Using the FEMDM and console error indications, analyze the operation of a WT3 execution as it affects or is affected by:
   a. Timing conditions
   b. Data flow
   c. Storage utilization
   d. S, DYN and MC registers

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

WORD TYPE 3

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____
11. _____
12. _____

SESSION 16 - WORD TYPE 4

This topic will cover the microprogramming concepts and specific information concerning word type 4. Also included will be coding functions and rules.

Objective: At the completion of this topic, the student should be able to:

1.* Using the FETOM, identify the function that a word type 4 performs.
2.* Given a list of control words, identify all words which are word type 4.
3. Convert a mnemonic statement for a word type 4 to its equivalent hex notation.
4.* Translate a branch/unconditioned hexword to its mnemonic equivalent.
5. Create an unconditional branch word for any address in control storage.
6.* Using the FEMDM and console indications, analyze the operation of a WT4 execution as it affects or is affected by:
    a. Timing conditions
    b. Data flow
    c. Storage utilization
    d. Backup register location and usage

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

WORD TYPE 4

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____

SESSION 17 - WORD TYPE 5

This topic will cover the microprogramming concepts and specific information concerning word type 5. Also included will be coding functions and rules.

Objective: At the completion of this topic, the student should be able to:

1. Using the FETOM, identify the function that a word type 5 performs.
2. Given a list of control words, identify all words which are word type 5 type hexwords.
3. Convert a mnemonic statement for a word type 5 to its hex equivalent.
4. Translate a word type 5 hexword to its equivalent mnemonic form.
5. Identify the difference between a 2 way branch (WT5) and an 8 way branch (WT5).
6. Identify the branchable locations for a word type 5, both in local storage registers or in external registers.
7. * Using the FEMDM and console error indications, analyze the operation of a word type 5 execution as it affects or is affected by:
   a. Timing conditions
   b. Data flow
   c. Storage utilization

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

WORD TYPE 5

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____

SESSION 18 - WORD TYPES 6 AND 7

This topic will cover the microprogramming concepts and specific information concerning word types 6 and 7. Also included will be coding functions and rules.

Objective: Upon completion of this topic the student, using the maintenance documentation, should be able to:

1. Using the FETOM, identify the function that word types 6 and 7 perform.
2. Given a list of control words, identify those words that are WT6 or WT7.
3. Convert a mnemonic statement for a word type 6 or 7 to its hex equivalent form.
4. Translate a given word type 6 or 7 hexword to its equivalent mnemonic form.
5. Identify the difference between a word type 6 and a word type 7.
6. Identify the branchable external registers and/or local storage registers when executing a WT6 or WT7.
7. * Using the FEMDM and console error indications, verify the operation of a WT6 or WT7 execution as it affects or is affected by:
   a. Timing conditions
   b. Data flow
   c. Storage utilization

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

WORD TYPES 6 AND 7

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____

SESSION 19 - WORD TYPE 2

This topic will explain the coding, use, timing and restrictions to be considered when using a word type 2. Also included will be the layout and usage of some of the auxiliary storage area.

Objective: At the completion of this topic, the student should be able to:

1. Using the FETOM, identify the functions of a word type 2.
2. Given a list of control words, identify all words that are WT2.
3. Using the Bit Significance Chart for a word type 2, convert a mnemonic statement for a WT2 to its hex equivalent.
4. Translate a WT2 hexword to its mnemonic equivalent.
5. Identify the main controls of a store operation when using a WT2.
6. Create a storage word to indirect access any area of addressable storage.
7.* Using the FEMDM and console error indications, verify the operation of a word type 2 as it affects or is affected by:
   a. Timing conditions
   b. Data flow
   c. Storage utilization

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

WORD TYPE 2

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____

SESSION 20 - TRAPS

This topic explains trapping, the reasons for traps, and the hardware and timings to accomplish the necessary functions.

Objective: Using the FETOM, FEMM and FEMDM:

1. Identify trap priorities by level.
2. Identify device priority within a given priority level.
3. Differentiate between trap level 0 and all other levels.
4. Identify the basic programming requirements for normal trap routines.
5. Identify the two major functions of the MMSK register.
6. Identify the significance of each MMSK bit position.
7. Identify the CPU status items that are saved on a trap.

This topic is an on-line topic presented via the FSS terminal.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

TRAPS

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____
10. _____
11. _____
12. _____

SESSION 21 - SELECTED ROUTINES AND SYSTEM RESET MICROPROGRAM

This topic introduces the CE to selected microprogram routines in the System/360 operational programs. It contains information on routine sequences, major functions and methods of using listings for diagnostic work. The diagnostic hardware will be defined as it is applied to CE resident diagnostic routine.

Objective: Upon completion of this topic, the student should be able to:

1.* Using console indications, the FEMDM and the microprogram listing, identify CSL failures and differentiate between:
   a. a hardware failure
   b. a microprogram failure
2.* Using the system reset function, identify correct or incorrect operation.
3. Using the FEMDM, identify the major objectives of a system reset function.
4. Using the microprogram listing, identify the operation and path for I-cycle decode of any given op code and its exit from I-cycles.
5.* Locate a failing CPU function with the use of the diagnostic register and console indications.
6.* Given a microword address and using the microprogram listing, determine the cause of a CSL check light.
7. Using the FEMDM, identify the CPU components set or reset during initial system reset.
8. Identify the function of each position of the diagnostic register using the FEMDM.
9. Given any microroutine and using the microprogram listings, identify the entry point to the routine.

SYSTEM RESET AND MICROPROGRAM AND DIAGNOSTIC HARDWARE

Highlights

- System reset key resets the CPU clock, all registers and controls in CPU and I/O units when the key is depressed.
- Release of system reset key causes microprogram trap to 0240.
- Address 0240 starts check of basic CPU functions.
- A diagnostic register is used for testing in the resident diagnostics and by the CE for test loops.

Activity

1. Read the section in the FETOM on System Reset in Chapter 6.
2. Read Resident Microdiagnostics in the FEMDM, diagram 1-1, part 2.

*Partially or totally supported in follow-on lab course.

The initial start of system operation, as defined in the System Reset section of the CPU FETOM, is the pressing of the system reset key after power has been turned on. Also, whenever the system is not running (MAN or TEST light is on) the CE can reset the system by depressing this switch. As shown on diagram 5-15 in the FEMDM, the system reset key starts a series of operations to first initialize (set or reset hardware components) and to then branch to a microprogram address which will test the various functions of the CPU.

To initialize the CPU hardware, many registers or latches must be either set or reset. Figure 5-15 lists these registers and latches and their condition before the system reset key is released.

Study diagram 5-15 in the FEMDM.

1. Which of the following set of registers and latches are reset when the system reset key is depressed?
   a. A-register check latch, clock 5 latch, soft stop latch, gate chan trap latch.
   b. Wait state latch, read call latch, S-register bit 6, display store latch.
   c. ALU check latch, diagram branch latch, M-register, mode register.
   d. Clock off latch, gate M to SAR latch, S-register, bit 6, system reset latch.

The text warned not to system reset when I/O devices are in mechanical motion. Notice on diagram 5-15, coordinates F and G2, the functions which are reset in the various attachment features.

On diagram 5-16, notice that the second block on the chart shows the clock being reset with depression of the system reset key, and the clock starting again when the key is released.

2. Clock latch _____ (No.) was set when the system reset key was pressed.

In addition, on diagram 4-11, part 1, it can be seen that the clock start interlock latch and the clock start latch are reset by the machine reset and the clock stop pulse lines respectively.

The clock off latch is set by the machine reset line. Follow these lines, on the FEMDM, back to the system reset key before proceeding.

How then was the clock restarted when the key was released? Read on for the answer.

Looking at the turn-on of the clock start latch on 4-11, B4, follow these lines or latches back to the system reset switch:

   a. clock start interlock latch (and with the negative going oscillator pulse).
   b. start clock pulse (ANDed with the positive going oscillator pulse).
   c. clock start latch on diagram 4-19A.
   d. system reset interlock turns on clock start latch (along with not clock start latch and not interlock latch).
   e. interlock latch was turned on by machine reset line (power on reset).

NOTE: Had system power been on and the read stop latch off, the start key would turn the clock start latch and start the clock.

Study these circuits and then continue with the following study questions.

3. When power is on, the clock start latch (diagram 4-1) turns on when:
   a. the start key is depressed.
   b. the system reset key is depressed.
   c. the system reset latch is on.
   d. the start key is released.
   e. the clock start interlock latch is on.
4. Is the M-register set or reset with system reset? _____
5. What must be the binary configuration to trap to hex address 0240? _____
6. Does system reset reset all positions of the MMSK register? _____
7. On what diagram is the MMSK register? _____

As the chart on diagram 5-16 shows, the trap address is generated if the system reset latch is on and positions 8 and 9 of the MMSK latch are off. Turning to the core storage and addressing data flowchart on diagram 3-3C5, take note that the "trap controls and addresses" block bypasses the actual M-register and goes directly to the storage address assembler.

Shown in more detail on the diagram 4-23C7, is the input from the system reset latch and the MMSK 8 and 9 positions. The correct output lines of M0-M1 are forced on and routed to the storage address assembler. Study the chart on this diagram before continuing.

Following the set line, "sample CPU trap req." back to its source, shows the set of the "gate M to SAR" latch by the system reset key.

Note: the following system sizes and their associated control program starting addresses:

System Size	Control Storage Starting Address
16K	Hex 4000
24K	Hex 8000
32K	Hex 8000
48K	Hex C000

The E60 listings for the 2025 systems, Form R25-5402, start with the lowest address at hex 0010. The CE must keep in mind the system size and the starting addresses involved. As can be seen from the above chart, the actual starting address for the 0240 BDIA routine is C240 for a 48K system. A tie-down page in the ALD (ZZ011), supplied with each system, will show the circuit prints necessary to force the correct storage addresses. (ALD pages are not included with your material.) (Manual selection of control storage is done with switch A in 0, 1, 2 or 3 position.)

Going back to diagram 5-16 in the FEMDM, the series of microlistings show BDIA, BCHK, BSYS, BPSW and BSWI as the necessary steps to complete the system reset operation.

BDIA

Turn to the System/360 Emulator (E60) microlisting, Form R25-5402, and find the BDIA routine. Read the descriptive text at the beginning of the section before continuing. (Page 33 in the listing.)

8. The resident BDIA microdiagnostic routine tests the CPU hardware for:
   a. Correct CSL operation
   b. Correct system reset operation
   c. Correct I/O operation
   d. Correct branching only
   e. Correct reader attachment operation

The microprogram routine is quite easy to follow if the correct next address, next sequence, label, next label, statement, comments and (sequence number) are used. (Check the heading at the top of each column.) Follow the first series of routines, as given here, and then the final address will be asked. Correct branching should result in the address given on the self-study answer page.

Starting at BDIA018, addresses 0240 and 0242 are executed twice; setting the diagnostic register 7 bit on to check for correct branching, and then setting the MMSK register to prevent further traps until this system reset routine is completed. After the second time through these two words, the program continues with address 0244. Please read the comments section before going on to the next paragraph. (Reading the line or lines of comments for each address used will make the whole routine understandable.)

The word at address 0246 checks to make sure the diagnostic register 7 bit was set.

> Had it not been set, the program would fall through to the next control word which branches the program to a hard stop at BDIA122.

Correct operation would branch, as indicated, to BDIA056 where DR7 is again set to a 1.

The next instruction sets G1-register to hex 0F to use its various bit positions to branch on. The G1 bit 0 should not be on so that the program falls through and sets DR7 again. The G1 bit 1 is then checked and should be off so that DR7 is again set.

9. What would have happened if G1 bit 1 would have been set when the program reached BDIA066?
   a. A branch to stop with the wait light on
   b. A one word branch loop with the system light on
   c. The system would stop with the manual light on
   d. A fall through to the next instruction

Falling through from BDIA067 to 072 now checks G1 bit 2 to be off. A correct branch to BDIA075 sets DR7. Bit 3 of G1 is checked to be off and another correct branch to BDIA083 again sets DR7. An unconditional branch from BDIA084 sends the program to BDIA087.

10. Continuing to test branching, the program will finally branch to BDIA _____ before going to the ALU test.

An address other than that given for this study question would be the result of an incorrect branch and the microprogram to this point should be reviewed until the correct address is reached.

One of the functions of the diagnostic branch register (FEMDM, diagram 4-13) is to check for correct branching during a diagnositc test. If a branch occurs to an address which does not set DR7, the diagnostic branch latch will stop the clock. Notice that the latch on the bottom right is set at T7 by a branch or a return word. It is reset at T2 time by a set DR function, which prevents the clock start latch (diagram 4-11, part 1, B4) from being reset. See frames D09 and D10 of microfiche card 2, V31-0124.

Going on to the ALU test beginning at address 2080, some of the operations should be familiar from previous sections.

The first instruction tests the Z-bus after an ALU operation.

11. Following the ALU (BDIA131) operation, what is the value on the Z-bus?

    _____

12. The dynamic condition (DC) register checks the ALU output. _____ (True/False)

A number of branch and link (BAL) operations plus checking for correct OR, exclusive OR, add, subtract, adder carry and complement AND functions are performed. The dynamic condition register is also checked, followed by more ALU operations to check for correct operation. Notice the use of the subroutine BDIA195 to BDIA203.

13. Follow the ALU test until it is complete. What is the last address in this test?

    _____

The microprogram following the ALU test checks the correct operation of the mode register, local storage, x-line addressing, local stroage set/reset, ALU error detection, main storage, A- and B- registers, parity detection and the dynamic condition register. Check the E60 listing for the start of these tests, defined by two rows of asterisks.

The main consideration when going through these steps is not necessarily to know what happens on every line, but to know how to decode the control words correctly. Each control word can be decoded to obtain the statement. Each statement is further defined by the comments and should need very little further comment.

From this point to the end of this section, questions will be labeled by the section (ie, BDIA) and, if necessary, by the function tested within the section (ie, BDIA - ALU Error). Please continue through the microprogram to the point of the question, and after answering the question, continue through the program to the next question. Some questions will point out changes to the program, which have not been changed on the listing. When in doubt about the statement and the comment, break down the control word using the bit significance charts for the word types at the beginning of the listing. The CPU FETOM will also be helpful.

14. BDIA208: What should be the receiving register of this move operation?

    _____

15. BDIA290: The second pass through the routine to check local storage register operation is a _____ (set/reset) operation.

16. BDIA328: How many times is the local storage subroutine executed? _____
17. BDIA379: The ALU error detection test depends on what register and bit position to prevent a clock stop? _____

The largest usage of the diagnostic register for resident testing is during this ALU error detection test and the tests starting at BDIA399. See frame D11 of microfiche card 2, V31-0124.

18. What is the control word which would force a trap? (Check all DR output lines; the answer is not found on the listing.)
    a. 28F2
    b. 2F14
    c. 20E2
    d. 27F2
    e. 38E8

This question took some investigation into the FEMDM. Following the output lines of the diagnostic register, the DR3 line is ANDed with various I/O requests (FEMDM figure 4-23) to cause a trap request. The control word, therefore, must have a definite configuration to set DR3.

19. Which control word allows a storage error to be created but also prevents the error from being recognized?
    a. 3804
    b. 38E8
    c. 3808
    d. 2804

BCHK

The completion of BDIA branches from BDIA432 to the BCHK routine. This check routine is used to verify that all of the control words in control storage are correct. Read the text at the beginning of the routine before proceeding.

20. Where is the check sum value stored for the Model 25?
    a. 0EC0
    b. 0002
    c. 0EC4
    d. 038E
21. BCHK045: The data 4E08 is obtained from:
    a. local storage location 8E.
    b. local storage D-register.
    c. control storage location 038E.
    d. program storage location 8E.

A normal system reset operation branches from BCHK047 to BCHK064 to prepare the P, T and V-registers for their use in the exclusive OR operation. The branch and link to BCHK083 allows a bypass of the CE trap area and starts the exclusive ORing subroutine at BCHK089.

22. What register is used for updating the CS addresses?
    a. P
    b. T
    c. V
    d. D

The subroutine mentioned above follows these sequence numbers:
BCHK - 068, 083, 084, 088, 089, 090, 091, 069, 070, 068 (repeat)
The subroutine of incrementing the P-register and exclusive ORing each successive control storage byte put into the V-register, with the previous data in the T-register, continues past 0EC4 where the check sum is stored. Step through and analyze this subroutine before proceeding.

23. What condition causes a branch out of this subroutine?
    a. An exclusive OR results in zero.
    b. The control storage address reaches 4000 hex.
    c. An exclusive OR does not result in zero.
    d. The control storage address reaches 16,385 binary.

If the result of exclusive ORing all of CS results in a zero, the program will branch from BCHK072 to label "OKSUM" and then go to BSYS002. This indicates that the control storage words are correct for this operation.

If the value put into the V-register (via the Z-bus) is not zero, one of two things happen:

1. The value in the V-register becomes the correction factor; if the CE key is on this factor is put into 0EC6 and a complete exclusive OR is done again resulting in a good (zero) check sum, or
2. The microprogram turns on the CSL check light and a hard stop.

BSYS

After studying the above routine, turn to the BSYS operation and read the descriptive text. Note that the BSYS routine can be entered by pressing the system reset key, the load key or the CSL key. Other than leaving this routine to branch to an IPL start routine if the load key had been used, the microprogram only sets and resets various I/O latches and auxiliary storage locations.

The branch from this system reset routine is from BSYS137 to the IPL and PSW load routines. Read the descriptive text and also refer to FEMDM diagram 5-16 before continuing to BPSW038.

BPSW

Entry from the system reset routine is to the NOT label at BPSW038. Notice the label LPSW at BPSW024. This would be an entry from a load key operation to load the initial PSW. If system problems point to PSW loading, addressing, machine check trap, the wait bit, protection errors, or any others listed in the descriptive text, analysis of this routine will help locate the trouble. Exit from this routine is from BPSW064 when system reset is initialized. Observe the general operation of this routine before moving to the last section of a system reset operation.

BSWI

Read: Read the descriptive text for the BSWI routine. Understanding of each step of the routine is not necessary. The ability to analyze the statements and the comments, and to correctly single cycle through the routine is important.

The entry from a system reset routine is to BSWI008. The final objective in this routine is to turn on the soft stop latch (BB0 = 0) and to branch on this condition. This branch is actually done at BSWI119 when the zero portion of the BB register is found to be zero. Branching back to BSWI105 puts the microprogram in a soft loop until BB1 = 1, BB4 = 1, or BB0 = 1. Any native request or set IC, or the start key will break the loop.

Summary

Refer back to the flowchart on diagram 5-16 in the FEMDM. This shows the major functions accomplished by the system reset key. Notice that a check for I/O requests is performed in this routine.

If the five routines performed correctly, the CPU enters a soft stop routine with only five lights lit on the console:

Byte 1 bit 2, 3, 6 and 7 lights are on.
Manual light is on.
All check lights are off.

This will indicate:

24. All registers and latches have been reset. _____ (True/False)
25. The check sum is correct. _____ (True/False)
26. The CPU functions checked in BDIA are working correctly. _____ (True/False)
27. B B-register zero position is on _____ (True/False)
28. The logout area printed out the check sum. _____ (True/False)
29. The system light is on while the microprogram loops. _____ (True/False)

Answers

1. c - the other answers all have at least one latch set.
2. 5 - see turn on of clock 5 from line 7 input.
3. d - the start key must be released (normal) to turn on clock start.
4. reset - check the left-hand column on diagram 5-15.
5. 0000001001000000
6. yes - see diagram for the MMSK register.
7. 4-15
8. a - check the description of BDIA.
9. b - check the next seq address.
10. 125
11. FF (binary 1111 1111)

12. True - check FEMDM 4-37
13. 20D8
14. 10 (I zero)
15. reset
16. 16
17. DRO
18. a - (control register bits 2, 4 and 14 allow a word type 0 to set diag register 3 bit).
19. a
20. b - check the BCHK descriptive text.
21. c
22. a - BCHK069
23. b - P0 bit 1 on = 4 (0100)
24. False
25. True
26. True
27. False
28. False
29. True

CONTROL STORAGE LOAD

Highlights

- The basic control program load routine of the (E60) System/360 Emulator Microprogram loads the resident microprogram.
- A hand load area is defined in case the program is altered or erased.
- The system reset routine is branched to, after the program is loaded.
- The check sum routine (BCHK) checks for correct loading of control storage.

Activity

Read: Control Storage Load (CSL) in the FETOM
Study diagram 5-20, FEMDM
Read CSL Check (Checksum) Routine in the FEMM

The diagram 5-20 shows a control storage load operation from an integrated 2540 and from the viewpoint of what happens in the CPU. Notice that after the CSL key is pressed, a trap is forced to 0010. This trap address is forced onto the storage address lines in the same way that the system reset trap was forced on diagram 4-23 of the FEMDM. Trace the set lines for the trap, back to the CSL key.

The 0010 address is the beginning of the basic control program load (BCPL) microprogram, which first checks the type of input device. The routine then waits for data from the input device before continuing to bootstrap the CSL deck into control storage. When the deck has been loaded, the routine branches to 08FE, which is the beginning of BDIA. BCHK follows and verifies that the CSL deck has entered correctly. The remainder of the system reset routine continues to the soft stop loop.

Read the BCPL descriptive text at the beginning of the BCPL routine.

1. The CSL deck is to be loaded from the native 2540. How are switches ABCD set?
   a. EEOD
   b. DDOC
   c. EEOC
   d. EEO6
   e. CCOD
2. The hand load address for Model 25 mode is:
   a. 0002
   b. 0004
   c. 0006
   d. 000A
3. The check sum figure is exclusive ORed for correction at control storage location 0002. _____ (True/False)

Turn to the hand load routine following the descriptive text of BCPL.

Notice that four hand load listings are shown, to be used depending on the type of input device. Using a native 2540, 20 addresses are shown which must be hand loaded before initial load, after control storage is wiped out, or if the CSL deck will not load correctly.

4. The CSL check light comes on if the deck loads incorrectly. _____ (True/False)
5. The logout area prints out for each CSL operation. _____ (True/False)

The CSL key has caused a trap to 0010, as described above. Address 0012 sets up the logout latch to allow printing of the EC level, the core load routine being used (in this case E60), the hand load data for the type of emulator deck (OBAD at 0002 for E60), and the correction factor, if any.

The address where the CSL cards begin loading (0100) is generated and the 2540 is readied for operation. When the first card has read, the program branches to a BNSR bootstrap routine which is common to the specific system being used. (The BNSR routine will be covered later. The E60 listing does not cover BNSR. The first section of the first ALD book with each system included BNSR for that system.)

Briefly, the BNSR bootstrap routine writes the data of each card into storage and forces reading of the following card. This continues until the end card is reached. The end card which is not read into storage, causes a branch to the last microstep of the BNSR. This instruction is an unconditional branch (statement XCTL '60F6') to BCPL118, where the overlay procedure begins.

The CSL cards had been read into hex 4000 of auxiliary storage and the data is now moved to 0100 of control storage. When the data is completely transferred to control storage, the CSL light is turned off. The program then branches to the beginning of BDIA and the normal system reset, BCHK, etc, routines will run.

Read the section Control Storage Load Failure Detection in the FEMM. After reading this section, answer the following self-study questions.

6. Cards 3, 4 and 5 of the CSL deck are:
   a. part of the bootstrap routine.
   b. data for the translate table.
   c. storage assignment cards.
   d. not used.
7. The check sum number is identified on the first bootstrap card and is loaded from the card to location 0002. _____ (True/False)
8. Two lines type out for the customer when a check sum error occurs. _____ (True/False)

The section of Procedure which was part of the reading assignment just given, describes the means of verifying the correct loading of data into storage. This procedure will indicate if the reader hardware is correct and if the CPU hardware receives the correct data.

Note the method of restarting CSL for intermittent reader checks.

Read the sections Checksum Routine -- BCHK and Initializing Procedure -- Checksum.

9. What location to be exclusive ORed has the check sum?
   a. 0EC4
   b. 0EC6
   c. 0002
10. The check sum figure is located:
   a. on the first bootstrap card.
   b. on the first CSL card.
   c. on the last bootstrap card.
   d. only on the first page of E60 listing.
11. An incorrect alteration to control storage is indicated (if the CE key is on) by four zeros printed out on the 1052 as follows:

    8226 0E60 0BAD 0000

    _____ (True/False)

Answers

1. c - see BCPL descriptive text
2. a - from BCHK
3. False - this is the check sum storage area
4. True - check FEMDM
5. True - check FEMDM
6. b
7. f - check sum is hand loaded
8. f - one line only
9. a
10. b
11. False - check FEMM

OPERATION CODE

Highlights

- The CICY routine analyzes the instruction cycles and determines the type of operation code.
- Op codes are fetched from main storage and decoded in CICY.
- Operands are fetched from storage, added, subtracted or compared, and replaced in storage, during the CBIN and CCOM routines.
- The effective storage address is developed, if data is in core, during instruction cycles.

Activity

Most activity for this section will be in the E60 listing, Form R25-5402.

The determination of the operation being performed by the problem program is done during instruction cycles, which is handled by the CICY routine. The objective of this section, then, is to analyze all op codes:

To set up some starting point, assume the following:

Instruction:	1A67 (add registers)
Instruction address:	0402
Operation:	PSW restart

A PSW restart is defined in the FETOM. Read this short section before proceeding.

Assuming a correct BDIA and BCHK operation, the microprogram branches to the beginning of the BSYS routine and proceeds through it. At what statement number will the program leave this routine? Determine the answer and then read on.

The normal sequence for a system reset would have branched at the point where the external DR register position 6 is tested. However, DR6 now equals 1 (BSYS124) and there is no branch. The program continues to BSYS128 where an unconditional branch to BPSW024 occurs.

Notice the layout of the PSW and the locations of each type, in the CE Handbook, Form 229-2178. Where is the location of the PSW for this operation?

The operation listed above is for a PSW restart, which uses the IPL-PSW located at HEX00. What is the address of the third halfword of the PSW?

The addressing of the PSW is done with the U-register, which had been reset to 00 back at BSYS127. The address of the third halfword would be 02 for the operation.

The PSW routine continues, as it did in a normal system reset until the PSW has been made the current PSW. The program then branches out from BPSW058 to check the op code starting at CICY008. Read the descriptive text for the CICY routine.

Looking at the read out of the first two bytes of the instruction, branching takes place depending on the value as placed in the G-register. What is the value in the G0-register?

There should be little difficulty in looking at a hex 1A value in the G-register and the fact that a branch to CICY016 occurs. The breakdown of this 16 way branch allows a further branch at what statement number?

A correct branch from the interrogation of the G0 high bits would be from CICY017, to allow a further breakdown of the op code.

The program now looks at G0 low and should branch to what label?

The listing for next address shows the first label for the branched-to location. The actual branch is determined by the A in G0 low, so that the program branches to OPIX A.

The type of op code has now been determined to be an add. The branch from here is to the CBIN routine, which covers the general objectives shown in the descriptive text for CBIN. Read the descriptive text before proceeding.

What objective is expected to be completed by CBIN for this operation?

Remember that the original operation is to add register 7 to register 6 with the answer in register 6. The overall objective then is the first one listed - add.

A branch to CCOM036 fetches the operands to be added together. The actual adding is done starting at what statement address?

Correct branching for the conditions involved would allow the adding of U0U1 to H0H1 and V0V1 to D0D1 starting at CCOM087.

This example problem started as a result of a PSW restart key depression, followed by pressing the system reset key. This branched the system reset program into the PSW routine after the normal entry for a program interrupt. The normal program interrupt would start at prog (BPSW003) and the instruction address would be stored and updated here.

The storage address for data was developed in CCOM.

EVALUATION QUESTIONS

The evaluation questions for this topic are located on microfiche card V31-0126, frames D09 and D10.

Please display these frames and answer the questions, keeping a record of these answers. When satisfied with all of your answers, sign on to the 2740 terminal and type in the answers.

When you have entered your answers, continue to the next topic, Console Controls, which is on the terminal.

This completes the information on selected routines.

ANSWER SHEET FOR EVALUATION QUESTIONS ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

SELECTED ROUTINES

1. _____
2. _____
3. _____
4. _____
5. _____
6. _____
7. _____
8. _____
9. _____

SESSION 22 - CONSOLE CONTROLS

This topic will familiarize the CE with the hardware which controls console operations.

Objective: Upon completion of this topic the student, using the maintenance documentation, should be able to:

1.* Define the purpose of the positions of the mode switch in relation to display and store functions.
2.* Differentiate between the mode switch positions which are single cycle and those which are not.
3.* Identify the major objectives for display of main storage.
4.* Identify the switch settings which allow the CPU clock to run.
5.* Define the use of each position of the diagnostic control switch and the purpose of the CE panel.
6.* Diagnose and repair failures to perform display or store functions.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

CONSOLE CONTROLS

1. _____

2. _____

3. _____

4. _____

5. _____

SESSION 23 - CHANNEL CONCEPTS

This topic introduces the CE to CPU channel concepts. It explains the channel data flow, CPU channel interface and channel to I/O interface. Basic performance specifications are also introduced.

Objective: Upon completion of this topic the student, using the maintenance documentation, should be able to:

1. Differentiate between integrated, channel zero and channel one operations.
2. Identify the data rate for byte or burst channel.
3. State the channel hardware required for byte or burst mode.
4. Identify the burst channel address.
5.* Diagnose and repair interface failures using the standard interface sequence chart and oscilloscope.
6.* Single cycle through the interface sequence using the pluggable indicators.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

CHANNEL CONCEPTS

1. _____

2. _____

3. _____

4. _____

5. _____

SESSION 24 - CHANNEL HARDWARE

This topic will define the channel hardware and describe its use for channel attachment operations.

Objective: Upon completion of this topic the student, using maintenance documentation, should be able to:

1. Idenfity the hardware registers and their relationship in channel operations.
2. Identify, using the microprogram listing, the failing register for a given failing channel operation.
3. Identify the channel latch that is automatically set by a storage word.
4. Differentiate between normal tag line operation and the tag line operation in CE diagnostic mode.
5.* Diagnose and repair failures in channel hardware, defined but not fault located by microdiagnostic programs.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

CHANNEL HARDWARE

1. _____

2. _____

3. _____

4. _____

5. _____

SESSION 25 - CHANNEL MICROPROGRAMS

This topic will provide information on the general flow and sequence of the microprograms that make up the channel.

Objective: Upon completion of this topic the student, using the maintenance documentation, should be able to:

1.* Using operational core load, define the cause of any interface check.
2. Trace logic flow through the microprogram for a normal start I/O.
3. State the purpose of any given section of code for the channel.
4. Given a channel trap address, identify the conditions that would cause that trap.
5. Identify the exit point from normal channel microprograms for any native device.
6. Trace the logic flow for a start I/O to any native device.
7. Identify the primary channel functions that are not used with native devices.
8. If a start I/O is issued to any device on the system, predict the resulting condition code.

This topic is an on-line topic presented via the FSS terminal.

*Partially or totally supported in follow-on lab course.

ANSWER SHEET FOR PRE-TOPIC QUIZ ON MICROFICHE

This sheet is provided as a convenience to the student. Record your answers in the space provided below. Save for insertion on the terminal at the appropriate time.

CHANNEL MICROPROGRAMS

1. _____

2. _____

3. _____

4. _____

5. _____

Self-Study Time/Page Log (SEE INSTRUCTIONS TO STUDENT PAGE)

DATE	ELAPSED TIME	ENDING PAGE	NOTES

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