



# **IBM**

**Field Engineering  
Theory of Operation**

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**2841** **Storage Control (Stage 2)**

## PREFACE

This manual describes the theory and operation of the IBM 2841 Storage Control Unit Stage 2, serial numbers 30101 (domestic) and 70-21147 or 73-21600 (W.T.C.) and above, with the IBM 2311 Disk Storage Unit.

Other manuals necessary for understanding the 2841 follow:

IBM Systems Reference Library Manual,  
System 360 Component Descriptions

(Order No. GA26-5988)\*

IBM Field Engineering Preschool Manuals,  
System/360

IBM Systems Reference Library Manual,  
System/360 Principles of Operation

(Order No. GA22-6821)

IBM Field Engineering Maintenance Manual, 2841  
Storage Control Stage 2 (Order No. SY26-3688)

IBM Field Engineering Manual of Instruction,  
SLT Packaging (Order No. SY22-2800)

IBM Installation Manual, 2841 Storage Control  
Unit (Included in System Diagram Manual)

IBM Maintenance Diagram Manual,  
2841 Storage Control, Order No. SY26-4137  
(FEMDM) (Included in System Diagram  
Manual Volume 8)

It is assumed that the CE has completed and understands IBM System/360 preschool; the 2311 Disk Storage Unit; a IBM System/360, Model 30 or larger; and channel operation.

Because the 2311 is the standard device used with the 2841, most of the references in Chapters 1 through 4 of this manual refer to operation with the 2311 interface.

This manual is based on version 007 of the system diagrams and information available as of July, 1969.

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\*Manuals referred to in this publication that have a form number with a four character prefix are identical in content to the same manual without the initial prefix character. (e.g., GA26-xxxx is the same in content as A26-xxxx.)

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LIST OF ABBREVIATIONS

Acc	-	Access	DL	-	Data field length
ac	-	Alternating current	DL	-	Data length low register
Addr	-	Address	DR	-	Data read register
Adv.	-	Advance	DW	-	Data write register
Adj.	-	Adjustment	E/C	-	Engineering change
ALD's	-	Automated logic diagrams	Ent	-	Entry
ALT	-	Alternate	ER	-	Error register
ALU	-	Arithmetic/logical unit	Err	-	Error
AM	-	Address mark			
BB	-	Burst byte register	FC	-	File control register
Bin	-	Binary	FCCHHR	-	Flag, cylinder number, head number, record number
BP	-	Bypass ALU control	FDD	-	Four double diode
BR	-	Bit ring	FDR	-	File data register
BX	-	Code check burst register	FF	-	Flip-flop
BY	-	Code check burst register	FL	-	Flip latch
			Fnd	-	Found
CA	-	TROS field - A register source	FR	-	Flag register
CAR	-	Cylinder address register	Freq	-	Frequency
CB	-	Circuit breakers	FS	-	File status
CB	-	TROS field - B register source	FT	-	File tag register
CC	-	Carry and ALU control			
CC	-	Code check	Gen	-	Generator
CCW	-	Command control word	GL	-	Gap length register
CD	-	D bus entry to registers	GP	-	General purpose register
CH	-	TROS field - branching control			
CK	-	TROS field - constant emit field	HA	-	Home address
CKD	-	Count - key-data	HD	-	Head
CL	-	TROS field - branching control	Hex	-	Hexadecimal
CLD	-	Control logic diagram	Hlt	-	Halt
CLK	-	Clock			
CN	-	TROS field - addressing control	ID	-	Identifier portion of the count field
CNT	-	Count field	IE	-	Gates in device interface
COMMO	-	Command out	IG	-	Register in the channel interface
CP	-	Circuit protectors	IH	-	Gates in the channel interface
CPU	-	Central process unit	Init	-	Initial
CS	-	Status register control	I/O	-	Input or Output
Ctr	-	Counter	IPL	-	Initial program load
Ctrl	-	Control	IS	-	Gates in device interface
CV	-	TROS Field - True complement control	IX	-	Index marker pulse
Cyl	-	Cylinder			
D	-	Data or D bus	K	-	Thousand
Dbl	-	Double	kc	-	Kilo-cycles
dc	-	Direct current	KD	-	Key-data
Del	-	Delay	KL	-	Key field length
Det	-	Detection	KL	-	Key length register
DH	-	Data length high register			
Diff	-	Difference	Mach	-	Machine
Dist	-	Destination	MAN	-	Manual



MLPX	-	Multiplex	S/D	-	Serializer/deserializer unit
Mod	-	Module	Sel	-	Select(ed)
MS	-	Module select	SELTO	-	Select out
$\mu$ sec	-	Microseconds	Sep	-	Separated
MSec	-	Milliseconds	SERDES	-	Serializer/deserializer unit
MT	-	Multi-track	SERVO	-	Service out
MTM	-	Multi-track-mode	SFM	-	Set file mask
			Sig	-	Signal
N/C	-	Normally closed	SLT	-	Solid logic technology
N/O	-	Normally open	Smpl	-	Sample
ns	-	Nanoseconds	SORSP	-	Service response
			Srch	-	Search
OA	-	Old address	SS	-	Single shot
OP	-	Operation code register	ST	-	Status register
Op-In	-	Operation in	Supp	-	Suppress
Osc	-	Oscillator	Svc	-	Service
			Sw	-	Switch
PA	-	TROS field-parity			
PC	-	TROS field-parity	T/C	-	True or complement
PN	-	TROS field-parity	Tgr	-	Trigger
PS	-	TROS field-parity	TIC	-	Transfer in channel
			TROS	-	Transformer read only storage
Rec	-	Record			
Ref	-	Reference	UR	-	Unit address register
Reg	-	Register			
Req	-	Request	vac	-	Volts alternating current
R0	-	Record zero	vdc	-	Volt direct current
ROS	-	Read only storage	VFO	-	Variable frequency oscillator
R/W	-	Read and/or write			
			W	-	TROS addressing register
SALS	-	Sense amplifier latches	Wrt	-	Write
SC	-	Seek complete			
SCU	-	Storage control unit	X	-	TROS addressing register

1.1 GENERAL INFORMATION

- The IBM 2841 Storage Control Unit provides a method of attaching serial direct access storage units to the IBM System/360.
- Up to eight 2841's may be attached to a channel.
- The basic 2841 can control up to eight 2311 Disk Storage Units.
- Types of units: 2311 (standard), 2302, 2303, and 2321 (optional).
- Any combination of units can be connected to one 2841.
- 2841 uses Solid Logic Technology.
- 2841 uses read only storage for control.

The IBM 2841 Storage Control Unit (SCU) is designed to attach serial direct access storage devices to the IBM System/360, Models 30 and above. The SCU provides all the buffering and control necessary to attach these devices to the I/O channels through the standard I/O interface (Figure 1-1).

The 2841 provides the ability to interpret and execute commands, to translate data as it moves between the serial-by-bit direct access device and the parallel-by-byte System/360 interface, to check the integrity of the information that is transmitted to and from the device, and to furnish status information to the using system.

The 2841 is designed so that circuits common to all direct access devices are housed in one section of the unit while circuits associated with a specific device are housed in a separate area.

The features available for the 2841 Storage Control are:

1. 2311 Attachment (standard part of 2841)
2. 2302 Attachment (optional)
3. 2303 Attachment (optional)
4. 2321 Attachment (optional)
5. Additional Storage 2302 (optional)
6. Two-Channel Switch (optional)
7. File Scan (optional)
8. Record overflow (optional)

2302 Attachment: This feature provides the circuitry required to attach a 2302 Disk Storage to a System/360 via the 2841. This feature is described in Chapter 5.

2303 Attachment: This feature provides the circuitry required to attach a 2303 Drum Storage to a System/360, Models 40, 50, 65, and 75 via the 2841. This feature is described in Chapter 5.

2311 Attachment: The IBM 2311 Disk Storage Unit is the standard unit for operation with the 2841. This manual is written primarily for 2311 operations.

2321 Attachment: The 2321 Attachment Feature provides the circuitry required to attach a 2321 Data Cell Drive to a system via the 2841. This feature is described in Chapter 5.

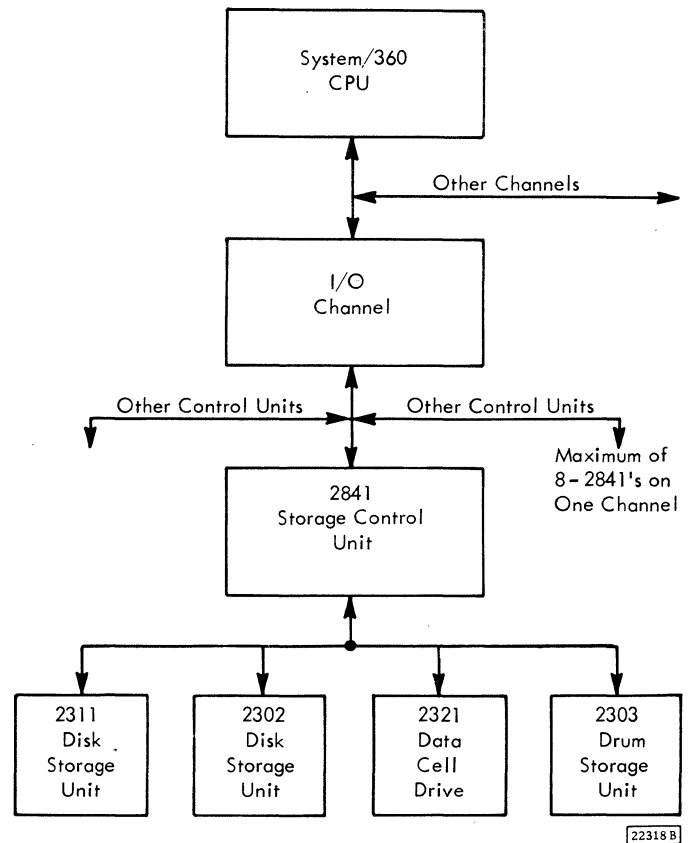


Figure 1-1. 2841 Storage Control Unit Configuration

**Two-Channel Switch:** The Two-Channel Switch Feature provides the switching circuitry required to attach the 2841 Storage Control Unit to a second channel. This feature is described in Chapter 5.

**Additional Storage:** The Additional Storage Feature provides circuitry to attach up to 16 access mechanisms to a 2841. The additional eight access mechanisms must be 2302 accesses. This feature is described in Chapter 5.

**File Scan:** The File Scan Feature provides an automatic rapid search for a specific identifier condition. This feature is described in Chapter 5.

**Record Overflow:** The Record Overflow Feature allows a record to overflow from one track to another. This feature is described in Chapter 5.

The 2841 utilizes Solid Logic Technology (SLT) and a Transformer Read Only Storage (TROS) to control its operations.

The use of disk storage provides the IBM System/360 with the ability to record and retrieve externally stored data either sequentially or randomly. It permits immediate access to specific areas of information without the need to sequentially examine all data recorded in the same file. Fast access to data storage locations enables the user to maintain up-to-the-minute files and to refer frequently and directly to data for the retrieval of stored data, regardless of the time of record insertion or the physical location of the data.

The extensive data storage capacity, swift access to recorded data, high data transmission rates, and broad flexibility of file maintenance and organization provided by disk storage devices introduce new and advanced data processing methods and allow simplification of procedures.

## 1.2 PHYSICAL DESCRIPTION

The physical characteristics of the 2841 are (Figures 1-2 through 1-10):

### 1.2.1 Dimensions

Height	60" (from floor)
Depth	30"
Width	44"
Weight	800 lbs.

The 2841 has two swinging covers on the right side and two swinging covers on the left side.

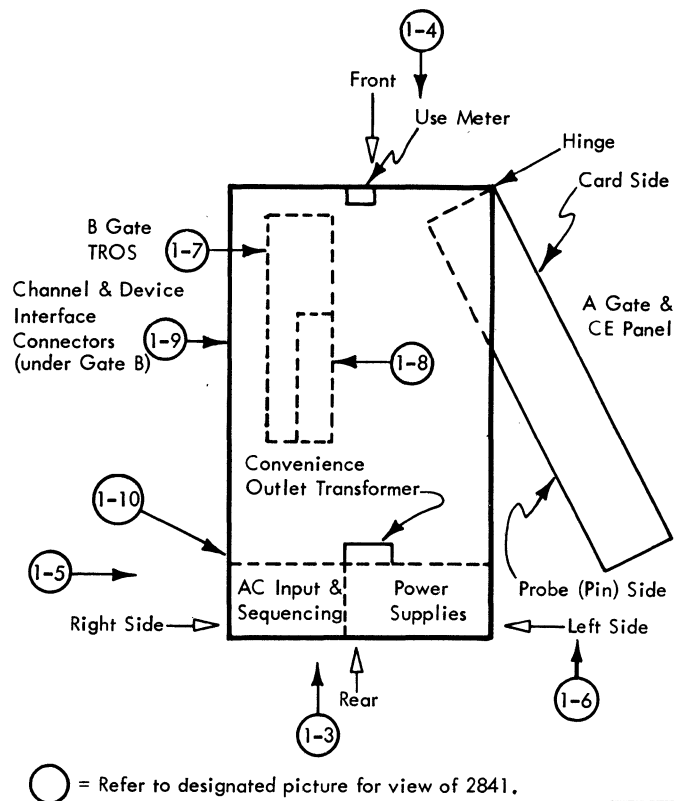


Figure 1-2. Top View

### 1.2.2 Power Requirements

Voltage:	3-phase 208 vac $\pm 10\%$ , 30 amp, 60-cycle, four wire cable (fourth wire is equipment ground)
Plug:	Russell & Stoll FS 3760
Mating Connector:	FS 3934
KVA:	1.9

NOTE: The 2841 can be adapted to operate on the following 50-cycle, 3 phase voltages in accordance with IBM Corporate Standard 3-2-5103-0:

1. 195 volts  $\pm 10\%$
2. 220/380 volts  $\pm 10\%$
3. 235/408 volts  $\pm 10\%$

### 1.2.3 Cable Entry

Power and signal cables enter the unit from underneath. A raised floor is desirable but not required.

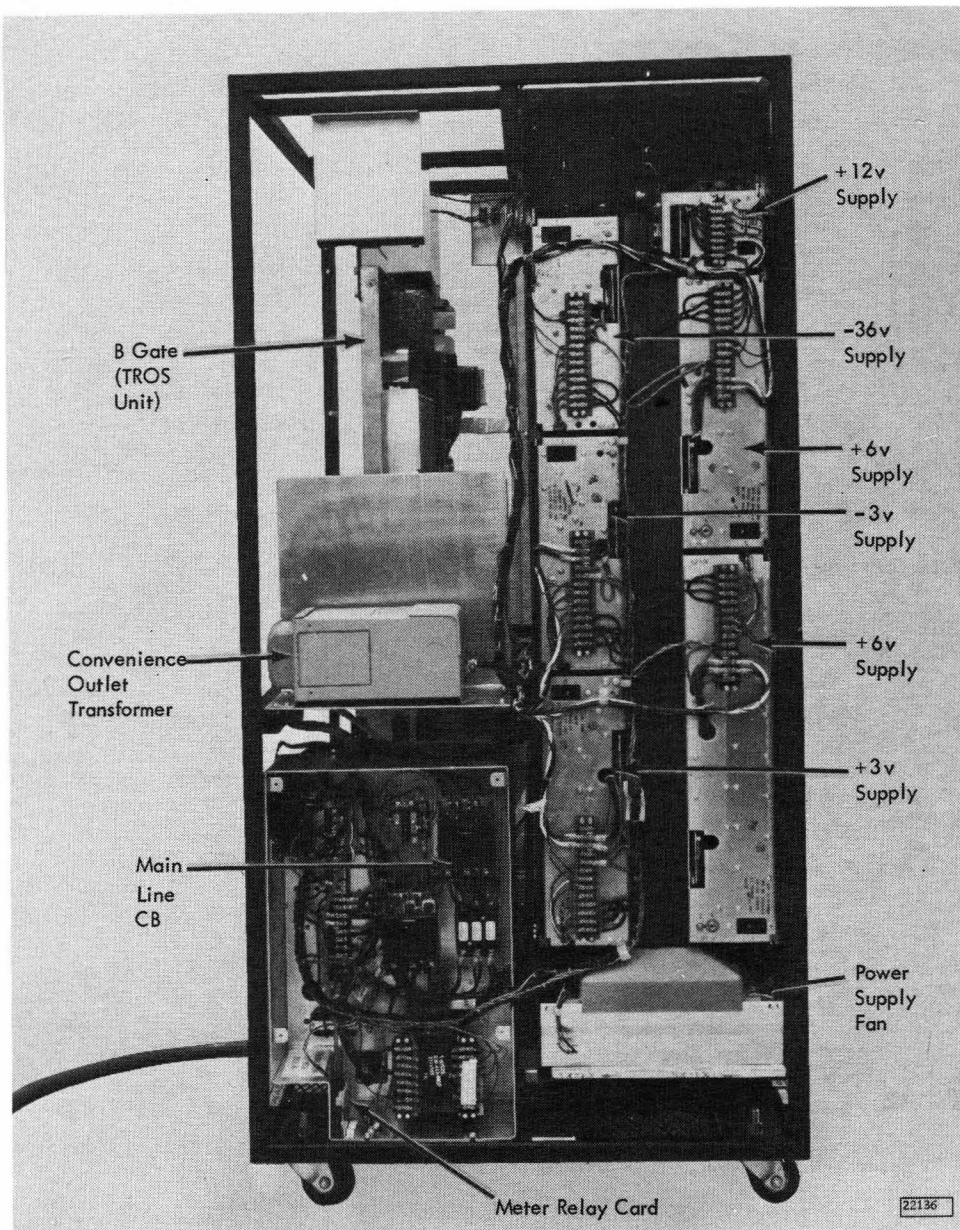


Figure 1-3. Rear View

1.2.4 Operator's Position

The control unit has no operator's position other than the meter-enable switch on the front of the 2841 (Figure 1-2).

1.2.5 Environmental Conditions

	<u>Operating</u>	<u>Non-Operating</u>
Temperature	60 - 90 <sup>o</sup> F	50 - 110 <sup>o</sup> F
Relative Humidity	8 - 80%	8 - 80%
Maximum Wet Bulb	78 <sup>o</sup>	80 <sup>o</sup>

1.2.6 Power Control

When power is present in the control unit, it is available to all devices attached to the unit. The control unit may be placed in one of its two modes, local mode or remote mode, by using a switch in the control unit. Normally the switch is in the remote position. In remote mode, power sequencing is controlled by the processor. In local mode, the power switches in the control unit must be operated. In local mode the processor cannot control sequencing.

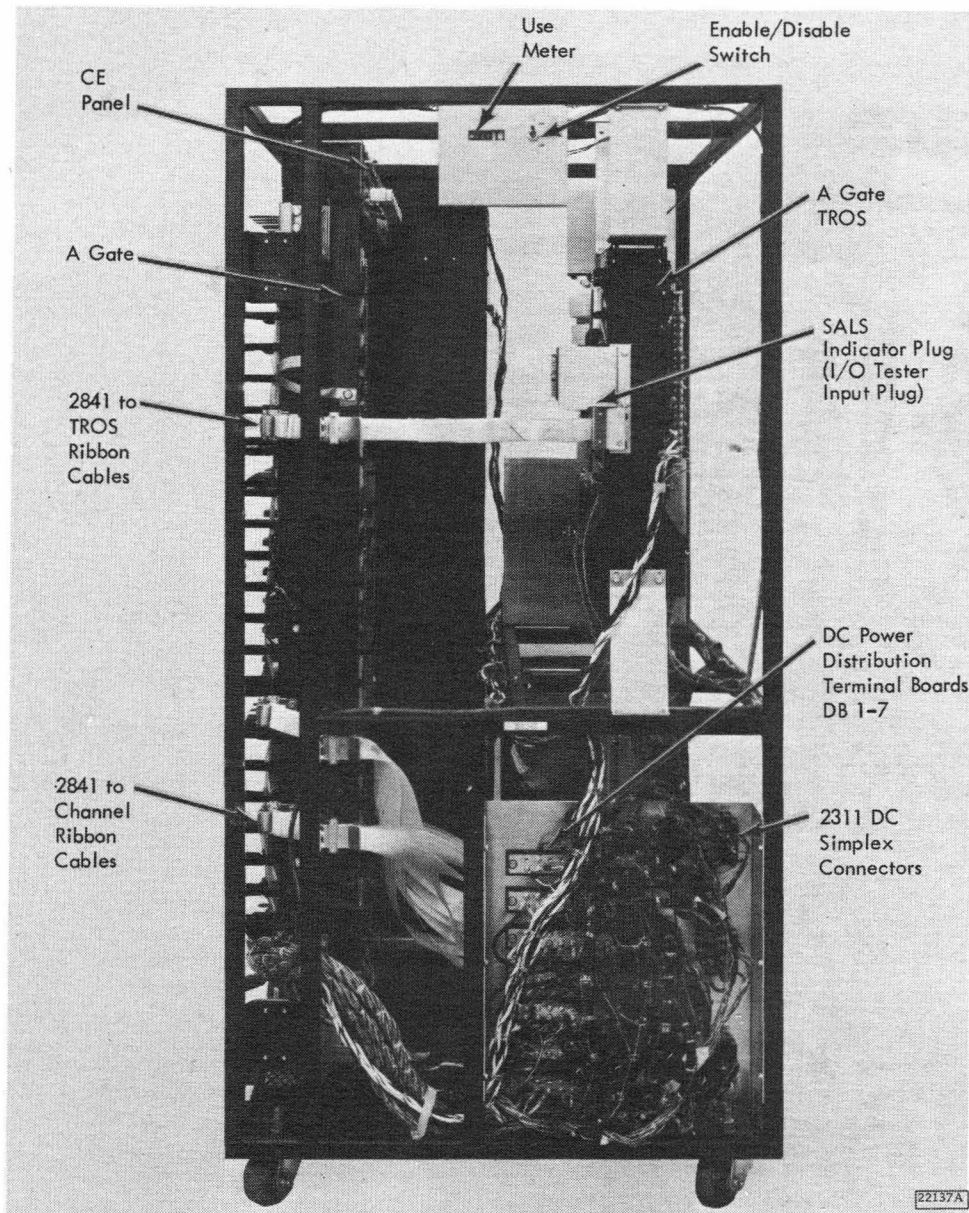


Figure 1-4. Front View

### 1.3 FUNCTIONAL DESCRIPTION

- The 2841 consists of six logical sections (Figure 1-11):
  1. System/360 Channel Interface
  2. Arithmetic/Logical Unit
  3. Serializer/Deserializer Unit
  4. Fourteen General Purpose Registers
  5. Transformer Read-Only Storage Unit
  6. Device Interfaces
    - a. 2311 Disk
    - b. 2302 Disk
    - c. 2303 Drum
    - d. 2321 Data Cell Drive

#### 1.3.1 System/360 Channel Interface

The System/360 Channel Interface provides a method for attaching I/O control units to System/360 channels.

#### 1.3.2 Arithmetic/Logical Unit

The Arithmetic/Logic Unit (ALU) can add, subtract, OR, AND, exclusive OR, and generate correct parity.

#### 1.3.3 Serializer/Deserializer Unit

The Serializer/Deserializer Unit (SERDES) converts parallel-by-byte data to serial-by-bit data when

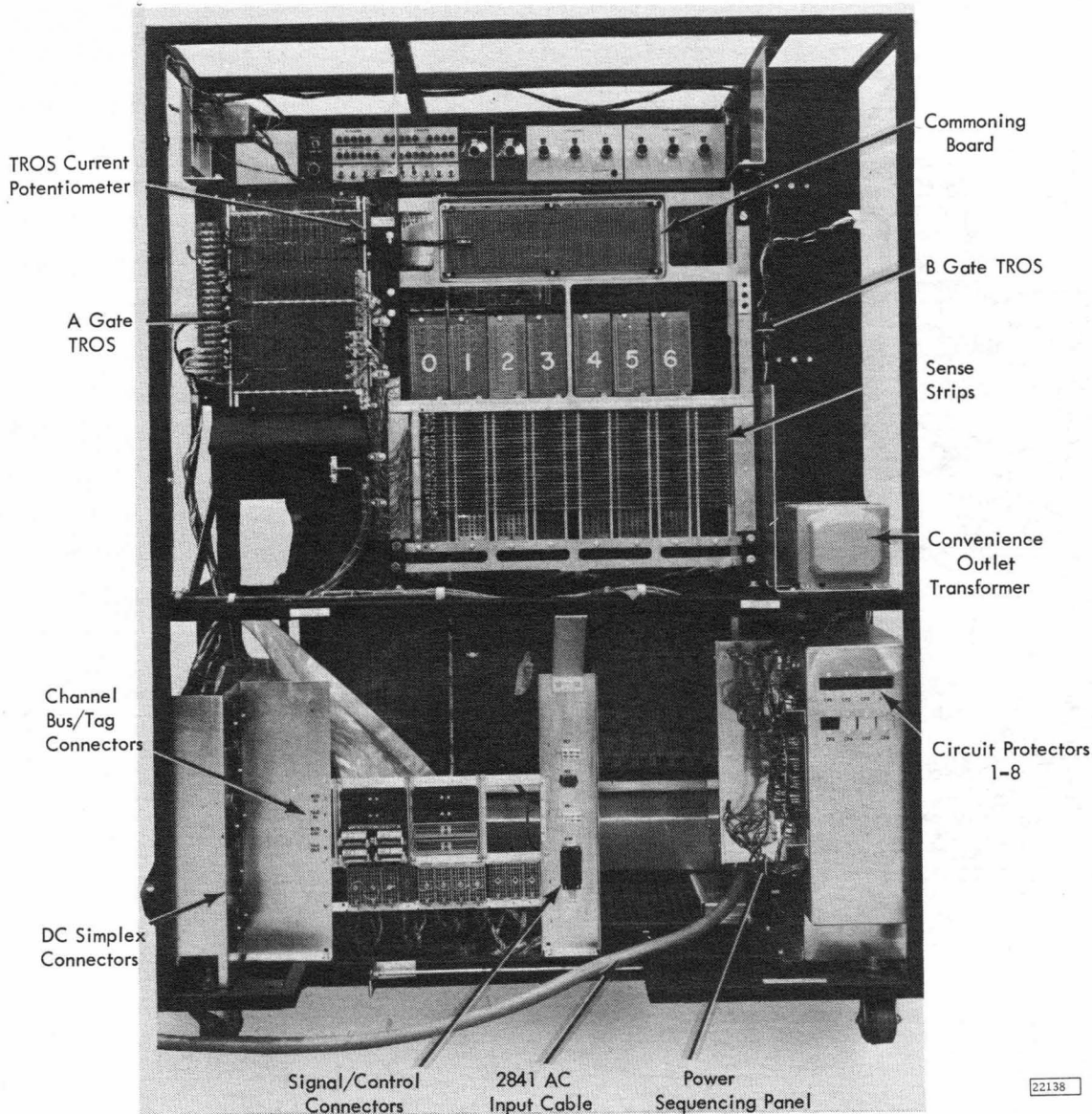


Figure 1-5. Right Side View

writing, and serial-by-bit data to parallel-by-byte data when reading.

#### 1.3.4 General Purpose Registers

There are 14 general purpose registers within the 2841. The microprogram uses the registers for various purposes. Chapter 3 includes a more detailed description of the usage of these registers.

#### 1.3.5 Transformer Read-Only-Storage

Transformer Read-Only Storage (TROS) consists of 2,048 addressable words. Each word is 48 bits in length and is one step in a sequence of words called a microprogram. The TROS storage cycle is 500 ns.

TROS furnishes control for all logical units within the 2841. Chapter 2 includes a more detailed description of TROS.

#### 1.3.6 Device Interfaces

The device interfaces contain data and control lines unique to a particular device type.

#### 1.3.7 Basic Write Data Flow

1. A byte of data is requested from a System/360 channel by the channel interface.
2. The channel places the byte on the bus-out lines and notifies the channel interface that the data is ready.

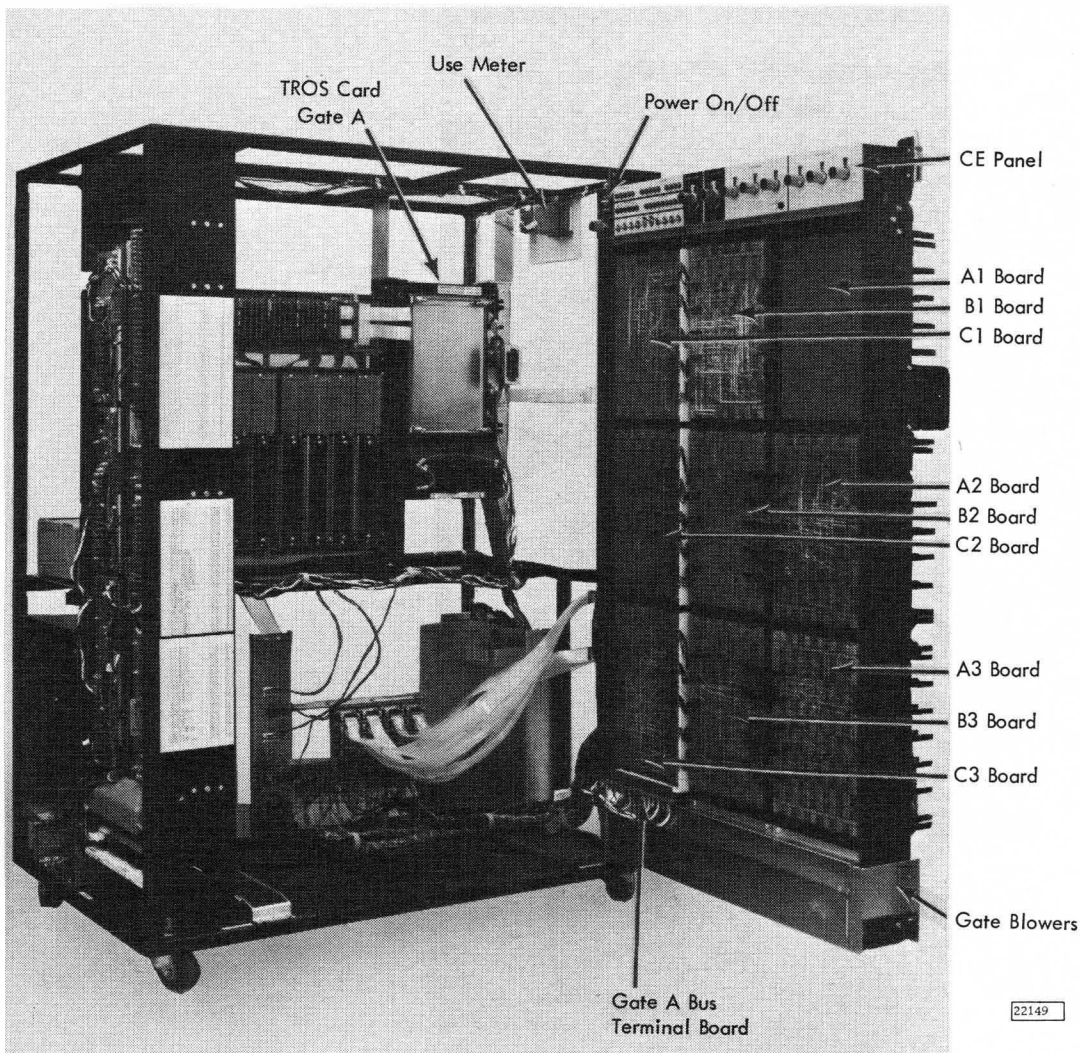


Figure 1-6. Gate A and CE Panel

3. The byte is transferred from the channel interface through ALU (No arithmetic operation is performed on it.) to one of the general purpose registers.
4. The byte is transferred from the general purpose register to SERDES.
5. SERDES converts the parallel-by-byte data to serial-by-bit data, and sends this data through the device interface to the device.
6. TROS controls each of these operations except for the parallel to serial conversion within SERDES.

#### 1.3.8 Basic Read Data Flow

1. Serial-by-bit data from the device is read in through the device interface and sent to SERDES.
2. SERDES converts the serial-by-bit data to parallel-by-byte data.
3. When SERDES has a complete byte (8 bits), the byte is transferred to one of the general purpose registers. TROS is notified of this transfer.
4. The byte is transferred from this general purpose register through ALU to another general purpose register. Correct parity is generated when the byte is transferred through ALU.
5. The channel interface notifies the channel that the 2841 has a byte ready for transfer.
6. When the channel is ready to receive the byte, the channel interface is notified and the byte is placed on the Bus In lines.
7. The channel takes the byte and notifies the 2841 of this action.

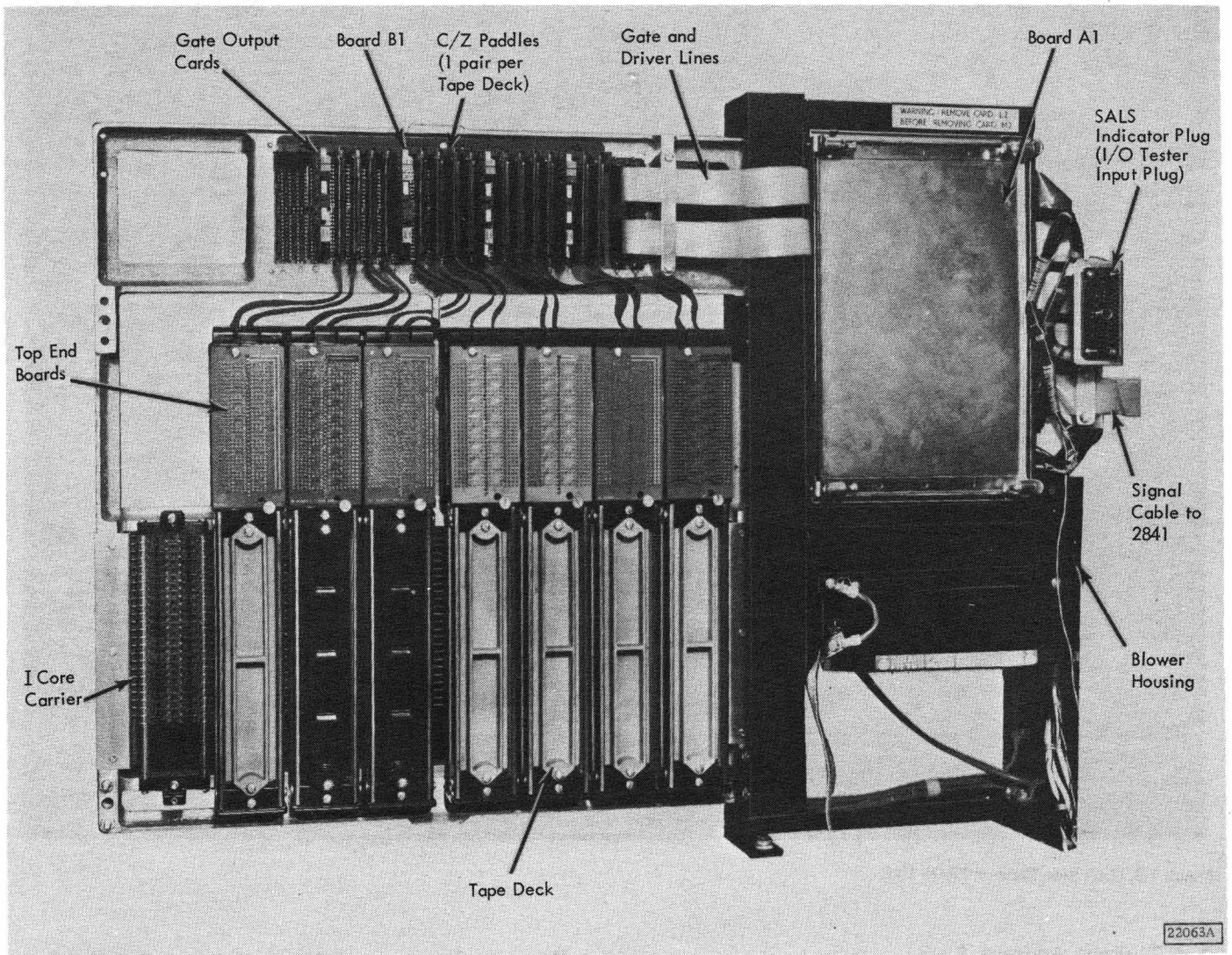


Figure 1-7. Right Side View of TROS Unit

#### 1.4 TRACK FORMAT

- A track consists of these areas and records:
  1. Home Address
  2. Record Zero
  3. One or more variable length data records.
- An index marker indicates the physical beginning of each track.
- Record zero (track descriptor record) has been designed for a special purpose, flagging.
- An address mark designates the beginning of data records.
- Each record is self-formatting. That is, it contains information defining the length of the records.

- Each record contains
  1. Count area
  2. Data area
  3. Possibly a key area.
- Two areas facilitate finding data: Identifier (part of count) and key area.

The following information concerning track format (Figure 1-12) pertains to the 2311 drive. However, all storage devices which attach to the 2841 use a common track format which differs from unit to unit mainly in the maximum capacity of an individual track.

##### 1.4.1 Index Marker

The index marker (IX) indicates the physical beginning of each track. All tracks use the same index marker.



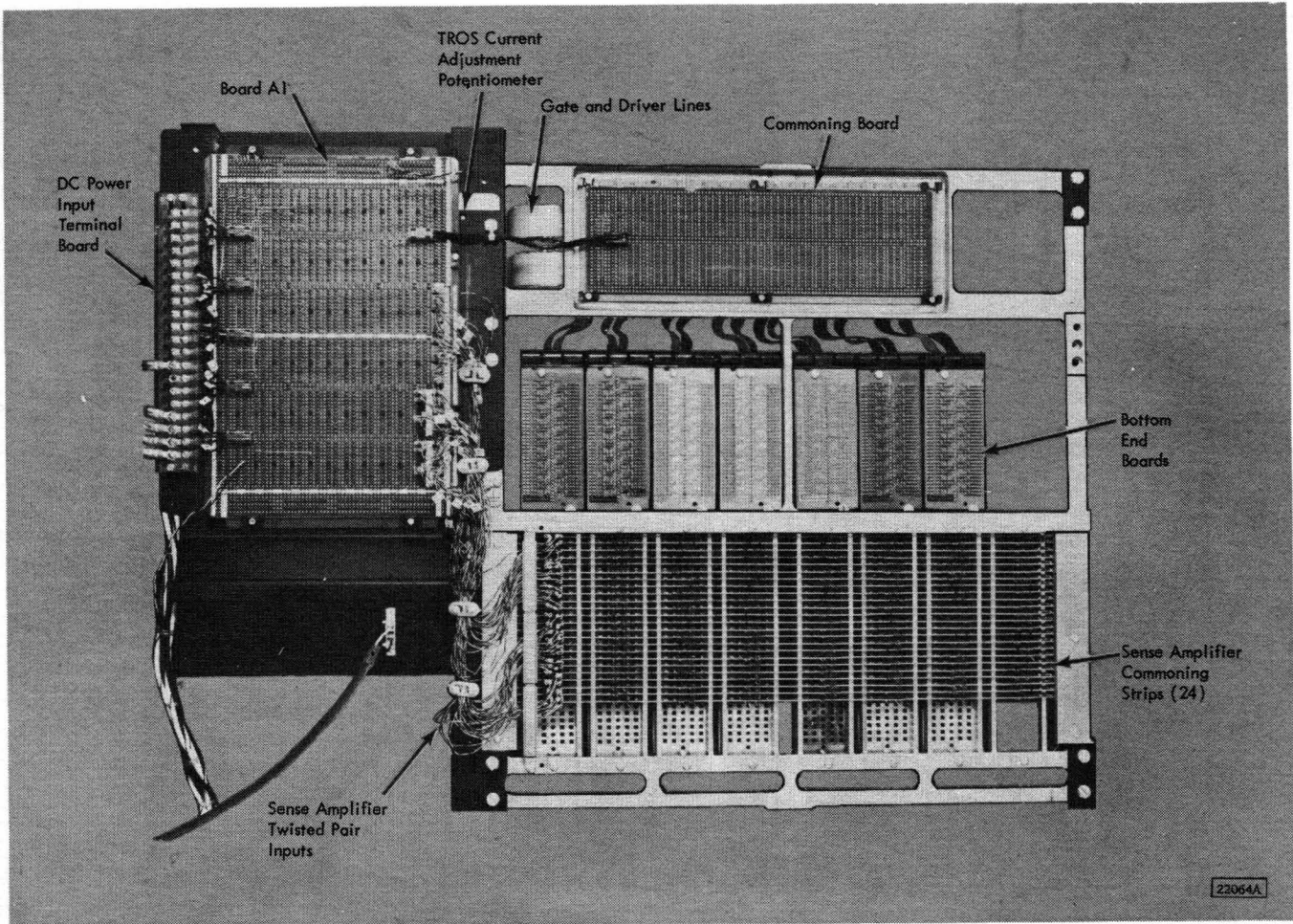


Figure 1-8. Left Side View of TROS Unit

### 1.4.2 Home Address Area

The home address area (HA) consists of seven bytes which define track condition and the physical location within the storage device. There is one HA area per track. This must be the first area written on each track and is created by a write HA operation. Contained within HA are five data bytes.

Byte	Name	Bits	Function
1	Flag	0 - 5	No purpose - always zero
		6	Track Condition 0 - good track 1 - defective track
		7	Track Use 0 - primary track 1 - alternate track

Byte	Name	Bits	Function
2, 3	Cylinder*	All	Specifies cylinder address
4, 5	Head*	All	Specifies head address
6, 7	Code Check	All	Error detection

\*The data recorded in the cylinder and head bytes must agree with the physical address of the track. The HH bytes must differ by one in ascending sequence from surface to surface. This format is followed because portions of these bytes are checked against the seek address on some operations.

Example: Assume the track is good, the cylinder is 173, the head is 3. Then the HA area equals:

F	C	C	H	H	CC	CC
0	0	173	0	3	**	**

\*\*Value assigned by microprogram during a write HA operation.

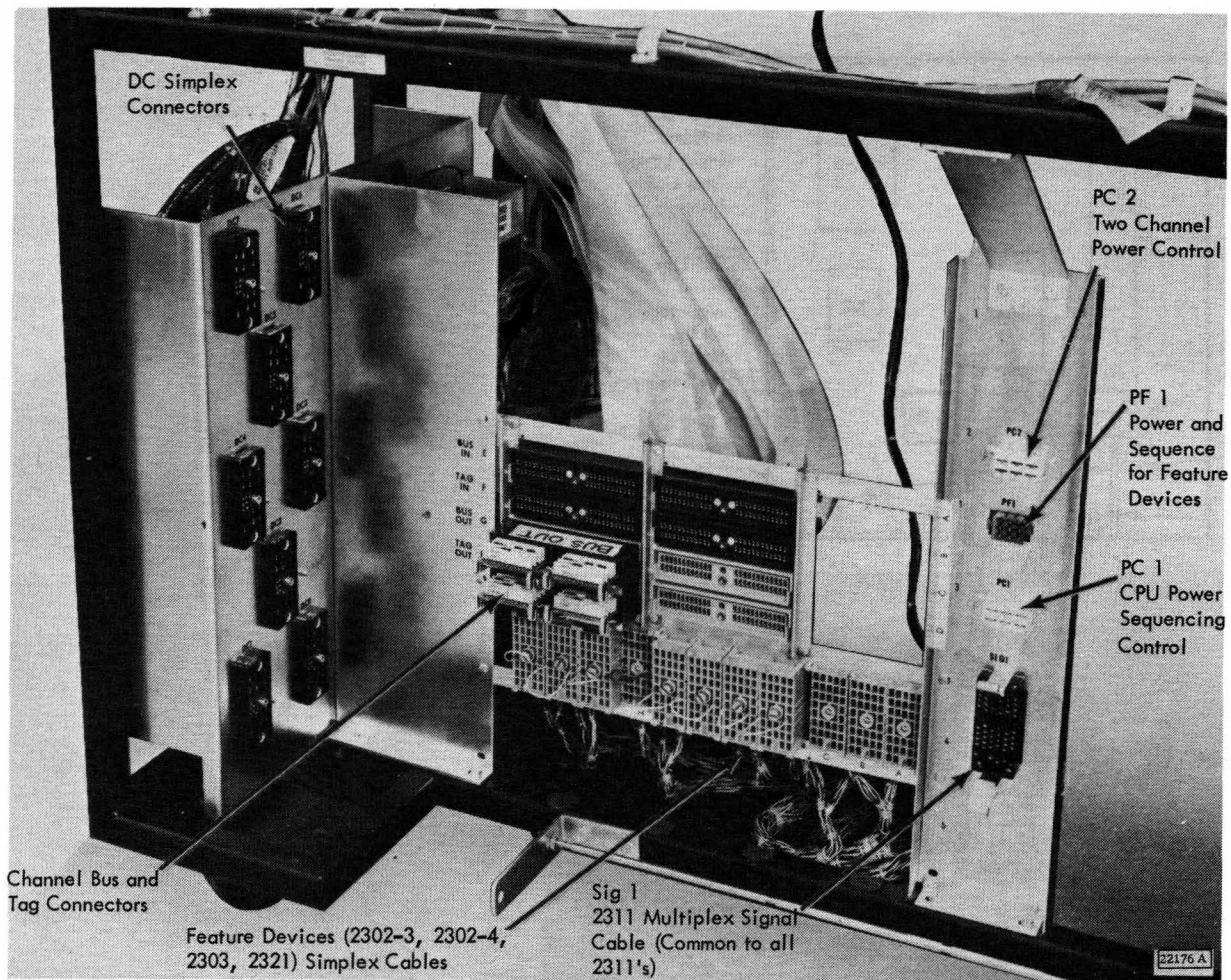


Figure 1-9. Device and Channel Cabling Area

### 1.4.3 Track Descriptor Record (R0)

The first record following home address on each track is the track descriptor record (record zero). Record zero is created by a write R0 operation. Although record zero may be used to store data, R0 is used by IBM Programming Systems to describe the track and to enable an entire track's data to be moved to an alternate track if a portion of the recording surface becomes defective. This process is called "flagging" and is described in Chapter 3. The description in this section is for normal R0 records only.

A count area and a data area are contained within R0. R0 may include a key area, but IBM Programming Systems does not require this.

#### 1.4.3.1 Count Area

This area is always 11 bytes in length. It can be divided into four logical sections.

1. Flag, Byte 1. This byte is generated by the

microprogram as R0 is written. Bits 0 - 5 equal zero. Bits 6 and 7 are propagated from bits 6 and 7 of the HA flag byte.

2. Identifier (ID), Bytes 2 - 6. This section is composed of five bytes - cylinder, cylinder, head, head, record number (CCHHR). (CCHH) is normally identical to the (CCHH) recorded in the HA area. (R) is the record number of this record. In the case of R0, the record byte is always zero.

Basically, the user can locate data in two ways. One way is to search for a particular ID, that is, a particular (CCHHR). Therefore, the purpose of the ID section of a count area is to furnish the user a method for locating the desired information. The second way is to search for a particular key area.

3. Format, Bytes 7 - 9. On some previous disk storage systems, records were of fixed length (1401-1311), or a separate track (format track) was used (7631-1301) to describe the length of a

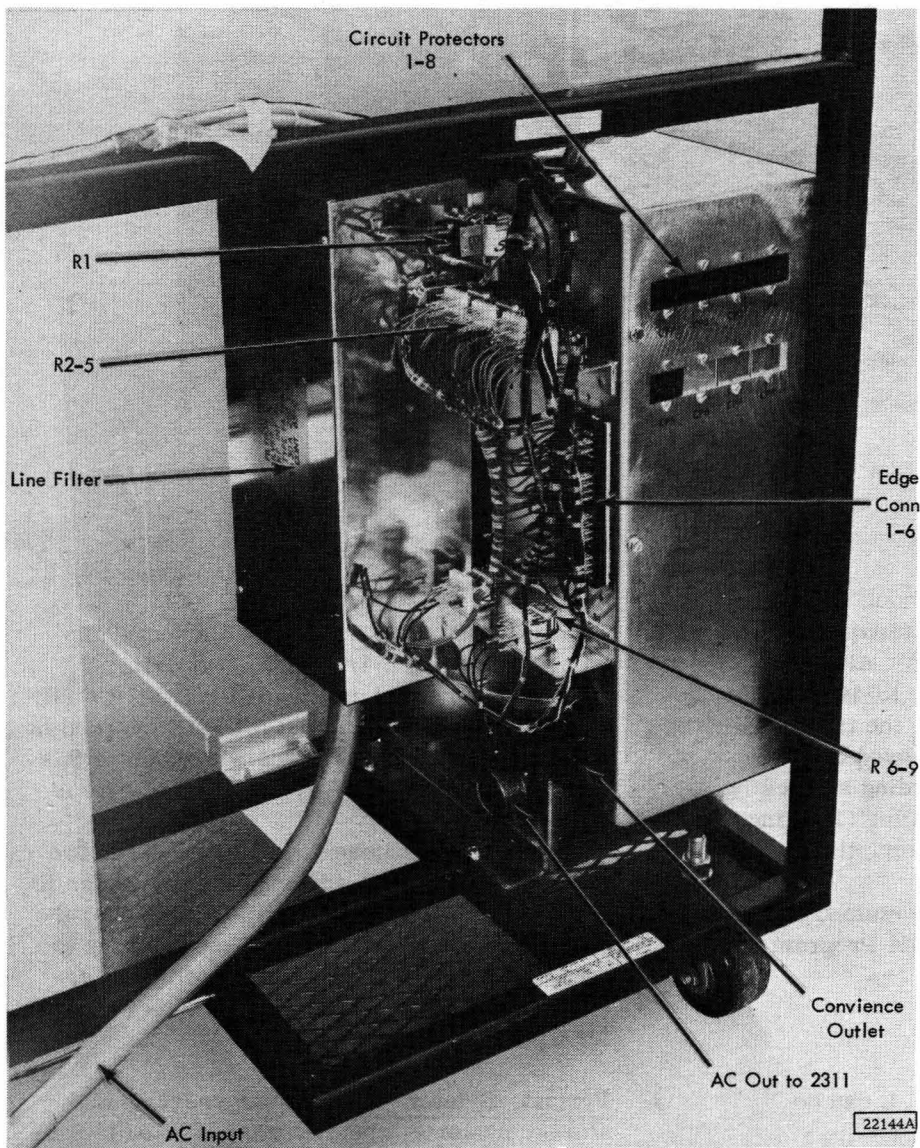
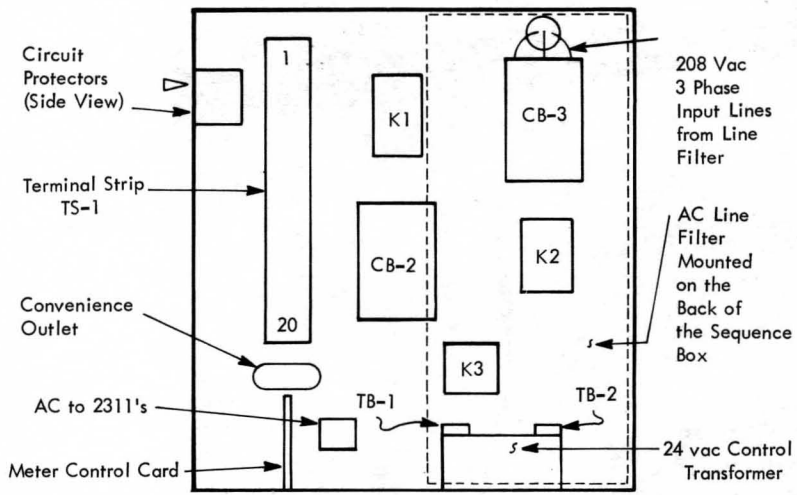


Figure 1-10. Power Sequencing Panel Area

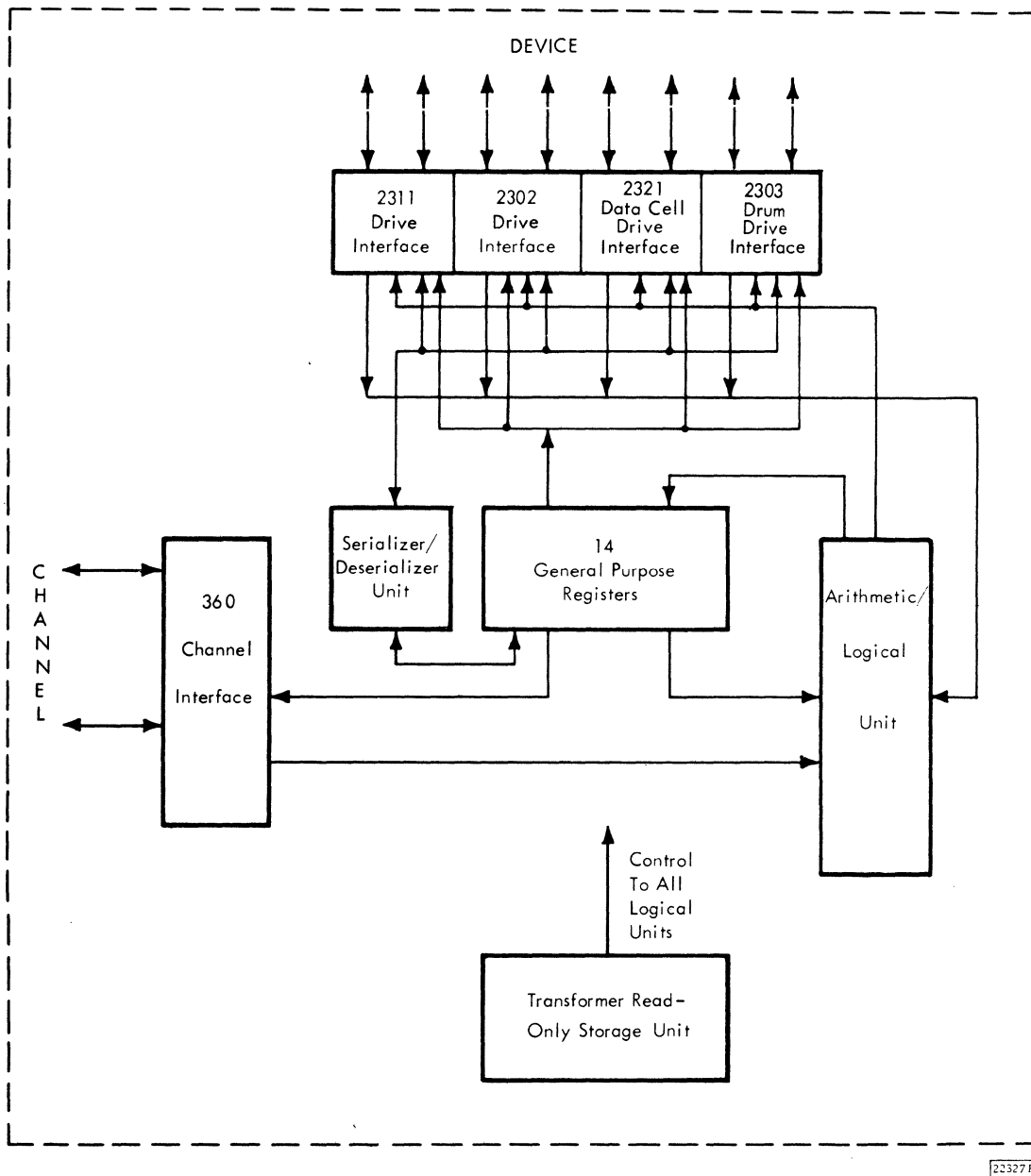


Figure 1-11. Functional Data Flow

record. Records on devices attaching to the 2841 can be of variable lengths. Therefore, some method was needed to define these record lengths. Bytes 7, 8 and 9 of each count field fully describe the record length as follows:

Byte 7 – Key Length (KL). This byte defines the number of bytes (excluding code check bytes) in the key area. If the record has no key area, the KL byte is zero. KL can indicate a key length of 0 to 255 bytes. Normally for R0, the byte is 0.

Bytes 8 and 9 – Data Length (DL). These two bytes define the number of bytes (excluding code check bytes) in the data area. Two bytes (16 bits) can indicate a data length of 0 to 65,535 bytes.

Zero data length indicates an end-of-file record. This may be used for any purpose by the user. The maximum quantity appearing in these two bytes for a 2311 is 3625.

4. Code Check – Bytes 10 and 11. Used for error detection.

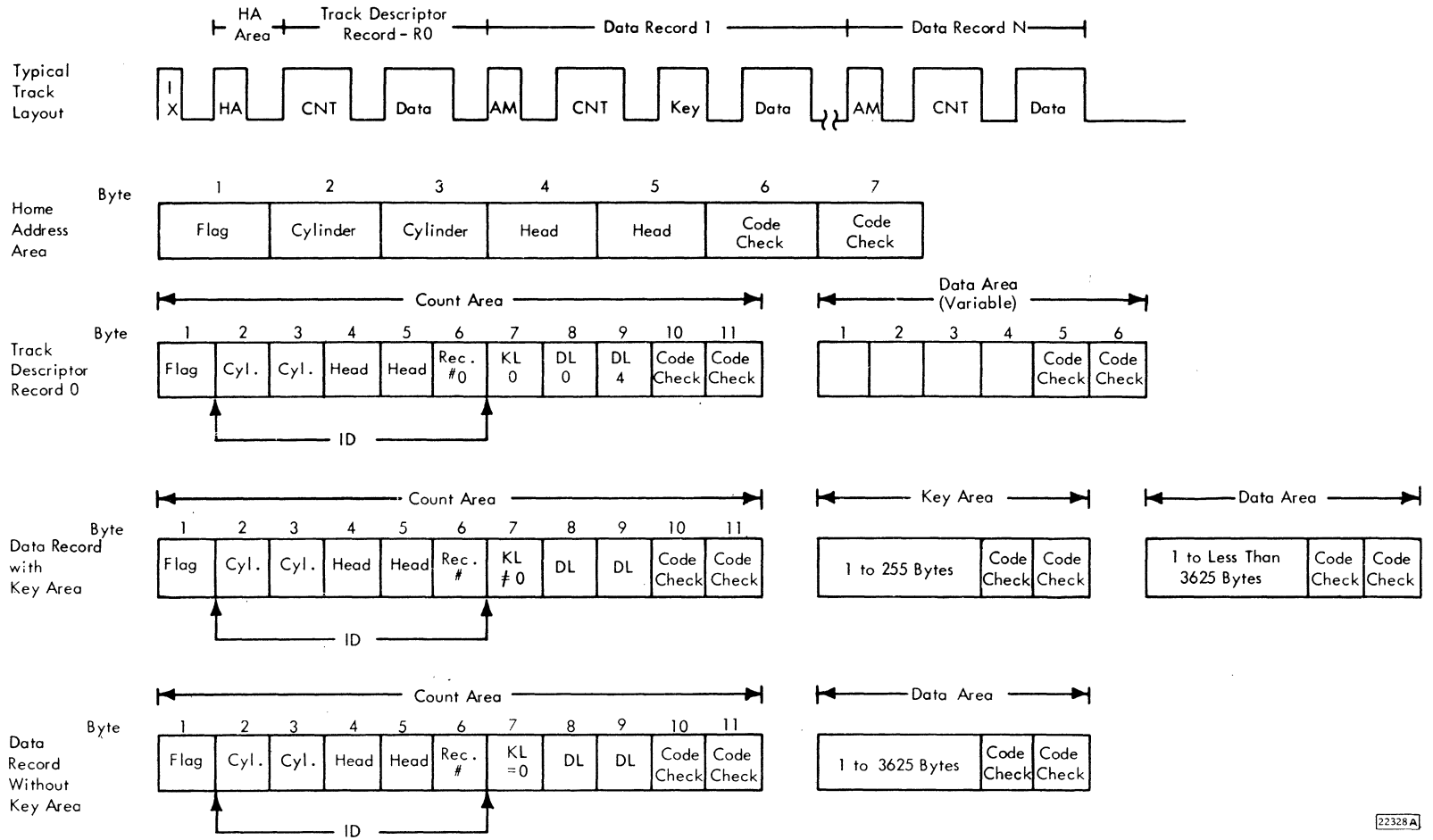


Figure 1-12. 2841 and 2311 Data Track Format

### 1.4.3.2 Key Area

The programmer decides whether or not to use a key area in R0. Refer to the Data Record Key Area section of this manual for a description of key area.

### 1.4.3.3 Data Area

Length and content of the data area of R0 depends on the type of programming used.

The IBM I/O Supervisor System/360 program uses this area to describe the balance of the track. The field will always be eight bytes in length. If the program is operating in direct access mode, the first five bytes contain the ID of the last record on the track, the next two bytes contain the byte count of the amount of track that is left to write on, and the last byte is not used. If the programmer has not called for this type of operation of the data field has no meaning.

Code check bytes are recorded at the end of the data area for error detection.

### 1.4.4 Data Record

One or more records may follow R0 on a track. Count areas make each record self-formatting for maximum data organization and flexibility. An address marker area and a count area are located before each data area. Depending upon the type of file organization, there may be a key area between count and data areas.

#### 1.4.4.1 Address Mark

This 3-byte area indicates the beginning of each data record. Address marks are written by the 2841 as data records are created. They are used by the 2841 to locate the beginning of a record for searching, writing, and reading operations. This allows the 2841 to begin an operation anywhere on the track instead of at index point.

#### 1.4.4.2 Count Area

This 11-byte area describes the key and data areas which follow. Bytes 2 - 9 are created in the CPU by the program used to write the record.

Flag: Byte 1 of the count area is generated by the 2841 as each record is written. It is not sent from the CPU.

Bit	Function
0	0 for even-count records (R <sub>0</sub> , R <sub>2</sub> , R <sub>4</sub> , R <sub>6</sub> ). 1 for add-count records (R <sub>1</sub> , R <sub>3</sub> , R <sub>5</sub> ). Used by the 2841 to ensure that all address marks (and records) are present. The 2841 signals a missing address mark when two consecutive, identical bits are encountered (unless an index point intervenes).
1	Used with Record Overflow feature. 0 for all non-overflow records and for the last record of an overflow chain. 1 for each record except the last segment of an overflow record.
2	Zero
3	Zero
4	Zero
5	Zero
6	Track Condition 0 indicates operative track 1 indicates defective track
7	Track Use 0 indicates primary track 1 indicates alternate track
Bits 6 and 7 are propagated from the flag byte of the preceding record.	

Cylinder - Bytes 2 and 3 contain the cylinder number of the track on which the data is stored.

Head - Bytes 4 and 5 contain the read/write head number of the track on which the data is stored. Generally the cylinder and head information are identical to the cylinder and head information recorded in the HA area.

Record Number - Byte 6 designates the sequential number of the record on the track.

Key Length - Byte 7 specifies the number of bytes in the key area. This may vary from 0 to 255 bytes (0 meaning no key area).

Data Length - Bytes 8 and 9 specify the number of bytes in the data area. This may vary from 0 to 3625 bytes for a 2311.

Cyclic Code Check - Bytes 10 and 11 are used for error detection. See Error Detection, 1.4.6.

### 1.4.4.3 Key Area

As mentioned previously, the user has two ways of locating his data. One way to locate data is to search for a particular ID (CCHHR).

Another way to locate data is to search for a particular key area. The key area length ranges from 1 to 255 bytes. The key area could contain identifying information about a record, such as serial number, social security number, policy number, etc.

Cyclic code check bytes are recorded at the end of the key area for error detection.

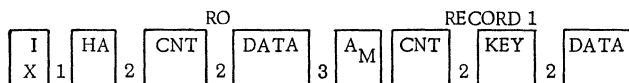
### 1.4.4.4 Data Area

This area contains the information identified by the count (ID) and key areas. This area may vary in length from 1 to 3625 bytes for a 2311.

Cyclic code check bytes are recorded at the end of the data area for error detection.

### 1.4.5 Gaps

Gaps are used to separate records and areas within records on the tracks. There are three types of gaps.



Gap 1 - The gap between index and the HA area. A fixed length - 36 bytes. This gap is referred to as the HA gap.

Gap 2 - The gap between the end of HA and RO count field. Also the gap between areas of a record. Fixed length - 18 bytes. This gap is referred to as the alpha ( $\alpha$ ) gap.

Gap 3 - The gap between the end of the data area of one record and the beginning of the count area of the next record. Variable length - 27 bytes plus 5% of the sum of the previous records key and data length. This gap is referred to as the beta ( $\beta$ ) gap. The beta gap also contains two address mark bytes.

A more detailed description of the contents of these gaps is in Chapter 2, under the heading - Serializer/Deserializer Unit.

Gap size and byte contents vary with the feature devices (refer to Chapter 5).

### 1.4.6 Error Detection

As information is being transferred from the parallel-by-bit using system to the serial-by-bit device (write), the 2841 strips off the parity bit associated with each byte. Parity bits are not recorded on the storage devices. For transfer to the channel (read), the 2841 assembles the serial-by-bit device data into a parallel-by-bit byte, adds a parity bit, and transmits the complete byte to the using system.

In the serial/direct access storage devices used with the 2841, the validity of the recorded information is maintained by adding a string of 16 bits (two bytes) to the end of each area. This type of checking is called cyclic code checking.

The 2841 accomplishes code checking by first filling two 1-byte registers with all bits. Each character read or written is exclusive ORed to one of the two registers. All even numbered characters go to the same register and all the odd characters go to the other. The final result is two "hash" total characters. These are used as the two code check characters.

For a write operation, the two bytes of cyclic check code are added to the end of the record and written on the track.

On a read operation, the process is continued until the cyclic code bytes on the end of the record are operated upon. If no error has occurred, the result is all zeros in the cyclic code check registers.

#### Example: Write

	Register 1
Set to ones	1 1 1 1 1 1 1 1
1st Char.	1 1 1 1 0 0 0 1
Result	0 0 0 0 1 1 1 0
3rd Char.	1 1 1 1 0 0 1 1
Result	1 1 1 1 1 1 0 1

#### Code Check byte one

	Register 2
Set to ones	1 1 1 1 1 1 1 1
2nd Char.	1 1 1 1 0 0 1 0
Result	0 0 0 0 1 1 0 1
4th Char.	1 1 1 1 0 1 0 0
Result	1 1 1 1 1 0 0 1

#### Code Check byte two

#### Example: Read

	Register 1
Set to ones	1 1 1 1 1 1 1 1
1st Char.	1 1 1 1 0 0 0 1
Result	0 0 0 0 1 1 1 0
3rd Char.	1 1 1 1 0 0 1 1
Result	1 1 1 1 1 1 0 1
Code Check one	1 1 1 1 1 1 0 1
Result	0 0 0 0 0 0 0 0

Register 2

Set to ones	1 1 1 1 1 1 1 1
2nd Char.	1 1 1 1 0 0 1 0
Result	0 0 0 0 1 1 0 1
4th Char.	1 1 1 1 0 1 0 0
Result	1 1 1 1 1 0 0 1
Code Check two	1 1 1 1 1 0 0 1
Result	0 0 0 0 0 0 0 0

The cyclic code check used in the 2841 has the following checking properties:

1. Detects all errors in which an odd number of bits is wrong.
2. Detects single bursts of errors that are 16 bits or less in length.

1.5 PROGRAMMING

Refer to SRL, Form Number A26-5988 for input/output operations and programming of the 2841.

A summary of the 2841 operation codes is included in Figure 1-13.

	0	1	2	3	4	5	6	7
	M/T	HI	=	C	K	D	CHANNEL	
Write Data	0	0	0	0	0	1	0	1
Write Key, Data	0	0	0	0	1	1	0	1
Write Count, Key, Data	0	0	0	1	1	1	0	1
Write Home Address	0	0	0	1	1	0	0	1
Write R0	0	0	0	1	0	1	0	1
Control Erase	0	0	0	1	0	0	0	1
Search Equal ID	-	0	1	1	0	0	0	1
Search Equal Key	-	0	1	0	1	0	0	1
Search Equal Home Address	-	0	1	1	1	0	0	1
Search Equal Key, Data	-	0	1	0	1	1	0	1
Search Hi ID	-	1	0	1	0	0	0	1
Search Hi Key	-	1	0	0	1	0	0	1
Search Hi Key, Data	-	1	0	0	1	1	0	1
Search Hi Equal ID	-	1	1	1	0	0	0	1
Search Hi Equal Key	-	1	1	0	1	0	0	1
Search Hi Equal Key, Data	-	1	1	0	1	1	0	1
Read Data	-	0	0	0	0	1	1	0
Read Key, Data	-	0	0	0	1	1	1	0
Read Count, Key, Data	-	0	0	1	1	1	1	0
Read Home Address	-	0	0	1	1	0	1	0
Read R0	-	0	0	1	0	1	1	0
Read Count	-	0	0	1	0	0	1	0
Read Initial Program Load (IPL)	0	0	0	0	0	0	1	0
Control Seek (BBCCHH)	0	0	0	0	0	1	1	1
Control Recalibrate	0	0	0	1	0	0	1	1
Control Restore	0	0	0	1	0	1	1	1
Control Space Count	0	0	0	0	1	1	1	1
Control No Op	0	0	0	0	0	0	1	1
Control Cyl. Seek (CCHH)	0	0	0	0	1	0	1	1
Control Head Seek (HH)	0	0	0	1	1	0	1	1
Control Set File Mask	0	0	0	1	1	1	1	1
Test I/O	0	0	0	0	0	0	0	0
Sense I/O	0	+	+	+	0	1	0	0
Write Spec-Count, Key, and Data (used with Record Overflow)	0	0	0	0	0	0	0	1
Reserved	0	0	1	0	0	0	1	1

Note: On Search and Read commands B0 can be either 0 or 1. If "0", head switching will not take place when Index Point is detected. If 1, head switching will take place when Index Point is detected. On a Sense Command Bits 1, 2, and 3 of the Code are "don't care" conditions (+).

22329A

Figure 1-13. Bit Structure of 2841 Operation Codes



## SYSTEM/360 I/O INTERFACE

### 1.6 CHANNEL INTERFACE INTRODUCTION

- The IBM System/360 Interface:
  1. Provides a method of attaching I/O units to the IBM System/360.
  2. Consists of 34 lines.
  3. Accommodates up to eight control units.

The input-output interface provides a uniform method of attaching input/output (I/O) control units to IBM System/360 channels. The interface can accommodate up to eight control units with addressing capabilities for up to 256 I/O devices.

The interface establishes requirements for signal transfers between control units and the servicing channel. Therefore, interface lines provide a common information format and signal sequence for all input/output devices. Figure 1-14 categorizes interface lines according to their general functions.

Except for signals that establish priority among control units, all interface signals are sent over a common bus. Any interface signal that the channel generates is available to all control units, but, only one control unit at a time is logically connected to the interface. After a control unit is selected, it remains logically connected to the interface until the control unit transmits or receives the required information or until the channel signals the control unit to disconnect.

The rise and fall of signals transmitted over the interface are interlocked with the corresponding responses. This interlocking makes the interface applicable to a wide variety of circuits and data rates, and permits the connection of control units of different circuit speeds.

Each control unit contains an address card that designates its interface address; no two control units on the same interface can have identical addresses. To begin an I/O operation, the channel must transmit the address of the desired unit.

Interface adapter circuits located in each control unit:

1. Convert interface line sequences and coded commands to the control lines necessary to operate the control unit.
2. Establish communication between the control circuits in the unit and the interface.

### 1.7 INTERFACE LINES

- Interface lines are divided into five types:
  1. Bus lines
  2. Scan controls

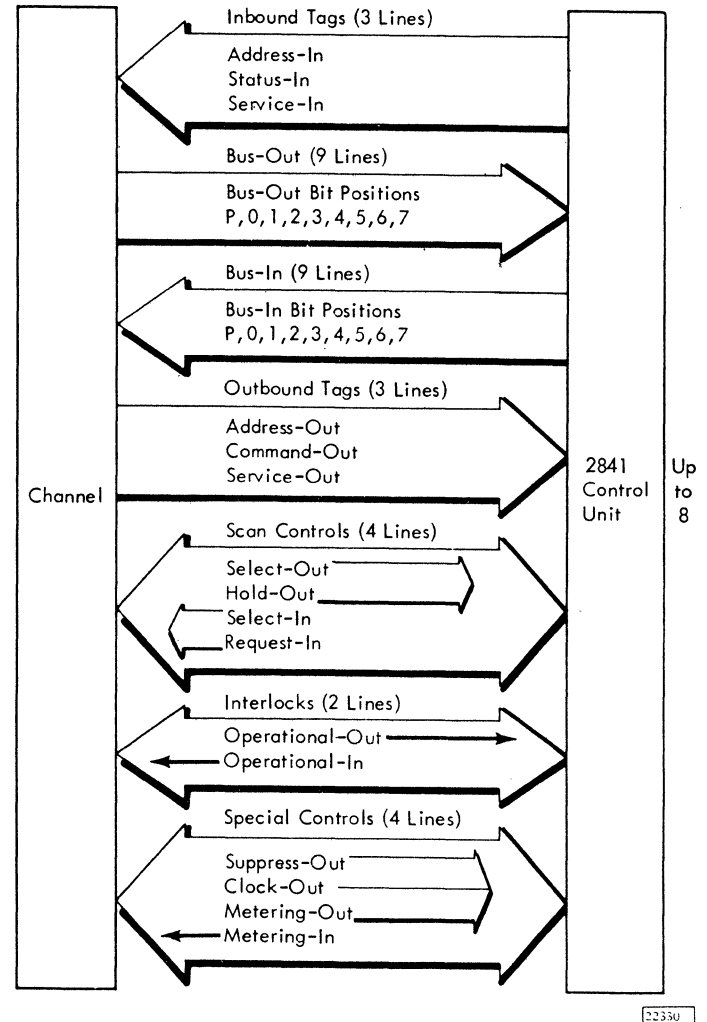


Figure 1-14. Interface Lines

3. Tag lines.
4. Interlock lines.
5. Special controls.

Figure 1-15 shows channel and control unit connections to the interface. Note that the select lines (select-out and select-in) connect serially through each control unit for the purpose of establishing priority; other lines connect in parallel.

#### 1.7.1 Bus Lines

- Bus lines carry information between the channel and control unit.
- There are nine bus-in lines and nine bus-out lines.

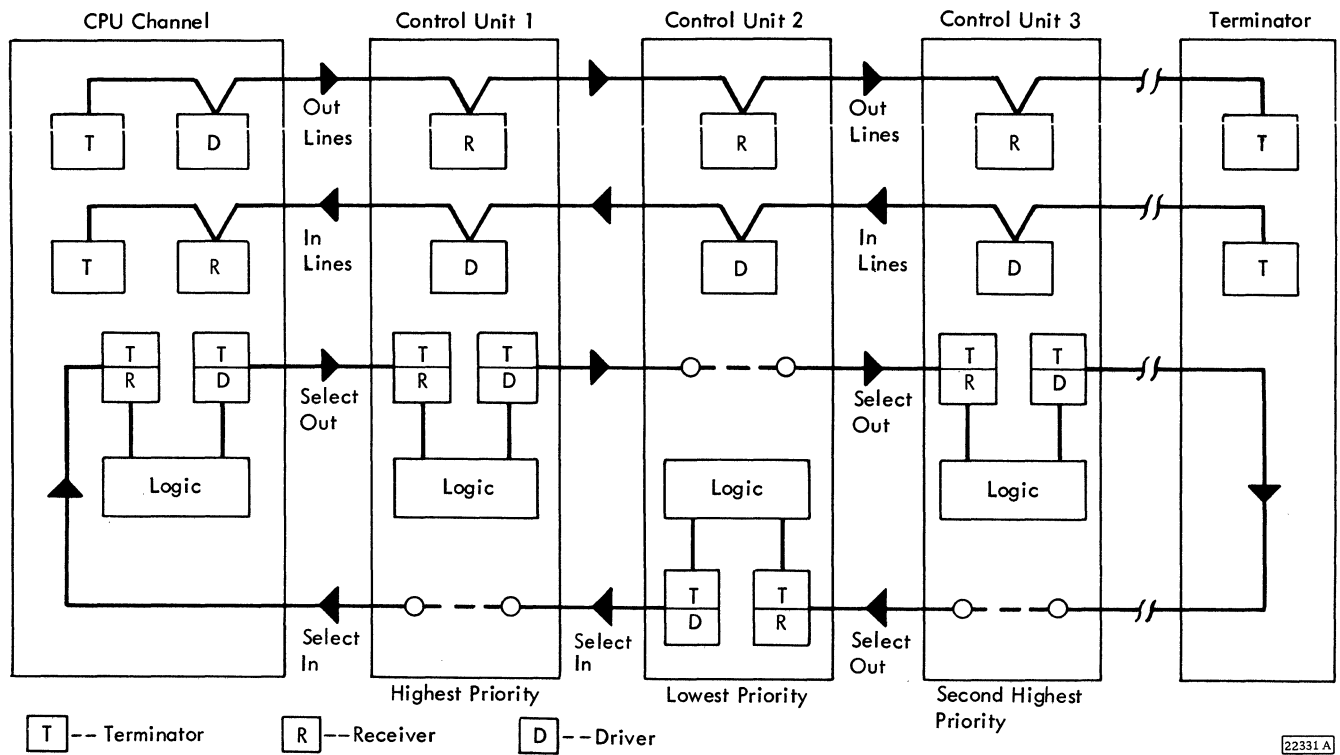


Figure 1-15. Interface Connections

Information is transmitted over the interface from the channel to the control unit on bus-out, and from the control unit to the channel on bus-in. Bus-in and bus-out each contain eight information lines and one line for odd parity.

Information on the in and the out bus is arranged so that bit position 7 of a bus always carries the lowest-order bit within an eight-bit byte. The highest-order bit is in position 0.

#### 1.7.1.1 Bus-Out

- Bus-out transfers information from the channel to the control unit.
- There are eight data lines and one parity line.

The nine bus-out lines transfer information from the channel to control units. The channel conditions an outbound tag line to identify the type of data transmitted on bus-out lines. For example, when the address-out tag and bus-out lines are active concurrently, information on bus-out lines designates an address.

Tag lines control the period during which bus-out lines contain valid information. When transferring the address of an I/O device, information on

bus-out lines is valid from the rise of address-out to the rise on one of the following: operational-in, select-in, or status-in. When transferring information other than an address, signals on bus-out lines are valid from the rise of the identifying outbound tag to the fall of the responding inbound tag.

#### 1.7.1.2 Bus-In

- Bus-in transfers information from the control unit to the channel.
- There are eight data lines and one parity line.

The nine bus-in lines transfer information from the selected control unit to the channel. The control unit conditions an inbound tag line to identify the type of information transmitted on bus-in lines. For example, when the status-in tag and bus-in lines are active concurrently, bus-in lines contain a status byte.

Tag lines control the period during which bus-in lines contain valid information. Signals on bus-in lines are valid 100 nanoseconds (ns) after the rise of the identifying inbound tag to the rise of the responding outbound tag.

### 1.7.2 Scan Controls

- Select-out, hold-out, and select-in are controlled by the channels. Request-in is controlled by the control unit.
- The scan controls are independent of CPU non-I/O operations.
- Scan controls enable the channel to contact control units attached to it.
- Scan controls permit control units to request service from the channel.
- Scan controls establish contact between the channel and the control units on a priority basis.

#### 1.7.2.1 Select-Out

- Select-out connects each control unit in series.
- It determines the priority of control units.

The select-out lines provide the loop that allows the channel to interrogate each control unit in priority sequence.

Logically, the select-out line connects serially through each control unit by connecting:

1. The channel to the control unit having the highest priority.
2. A control unit to the next control unit in descending priority sequence.

The physical location of a control unit (with respect to the channel) does not establish the unit's designated priority. For example, the control unit farthest from the channel might be the first unit to which select-out logically connects; this unit would then be the unit to which the highest priority is assigned.

When an I/O control unit receives the select-out signal it must either raise its operational-in line in response to it (request service) or immediately propagate the select-out signal to the next control unit in the series. Once a control unit has propagated select-out, it cannot raise its operational-in line until the next incoming select-out line to the control unit rises.

The channel must hold select-out active until it receives a signal on either the select-in or the address-in line. When select-out is transferred to the control unit with the lowest priority, the control unit either 1) raises its operation-in line, and later,

its address-in line, initiating a signal sequence with the channel, or 2) sends the incoming select-out to the channel. The signal on the select-out line's return path to the channel is called select-in.

If a control unit conditions operational-in when the incoming select-out is active, it does not transfer select-out to the next control unit (or select-in to the channel). By conditioning operational-in, the control unit interrupts the channel's scan loop. Then, the control unit transmits an address byte on bus-in lines and conditions address-in. The control unit must hold operational-in active until communication with the channel is complete. The channel can drop select-out after receiving address-in, or can hold select-out active through the complete I/O operation. In no case can the control unit cancel operational-in before the channel drops select-out.

#### 1.7.2.2 Select-In

- The select-out line's return path to the channel is select-in.

The control unit provides an option to connect its selection logic in series on either the select-out or select-in line (Figure 1-15). Descending-order priority from the channel can be established on the select-out line, and the remaining control units can maintain the descending-order priority from the channel on the select-in logic. For clarity, in this manual, the selection logic is assumed to be connected to the select-out line.

Select-in is a line from the lowest-priority control unit to the channel. It is the outgoing select-out line of that control unit and provides a return path to the channel for the select-out signal. The definition of the select-in line is the same as that of a select-out line coming from any control unit.

#### 1.7.2.3 Request-In

- This is a request for service from the control unit to the channel.
- May initiate a polling sequence at the channel.

A control unit conditions the request-in line to indicate that it will initiate a signal sequence when select-out polls that unit again. The channel need not condition select-out to scan the attached control units until the request-in line indicates that a control unit requires servicing. This operation allows the control unit with the highest priority to receive attention in a minimum amount of time after the request-in

line is conditioned. To illustrate the function of request-in, consider the following example:

Assume that the highest interface priority is assigned to the I/O device with the highest data rate and that the device with the slowest data rate has the lowest priority. The unit with the lowest priority can wait longest for service; so, each time that the request-in line is conditioned, that unit is the last to be polled. Because the I/O device with the highest priority can wait the least time for service, each request-in indication causes that unit to be polled first.

#### 1.7.2.4 Hold-Out

- Hold-out is used in conjunction with select-out.
- It allows the channel to cancel the effects of select-out and control polling.

The channel conditions the hold-out line to all control units in parallel to allow select-out to perform its designated function in a control unit. The hold-out line allows the channel to cancel the effects of select-out at each control unit at the same time. If the channel is holding select-out active and cancels hold-out, no control unit can make use of select-out; a unit can only propagate the incoming select-out to the next unit. Therefore, the channel receives select-in in the shortest possible time.

### 1.7.3 Outbound Tag Lines

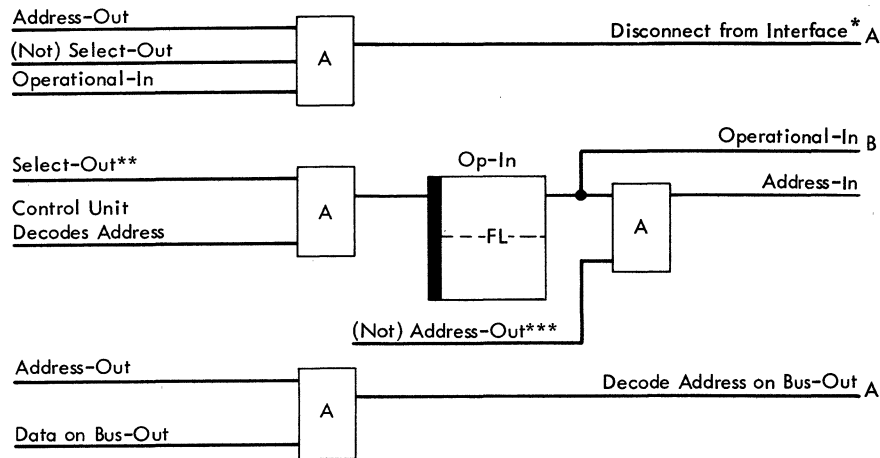
- These lines carry instructional signals to an attached control unit.
- They identify information on bus-out lines.
- Two out-tags cannot be active at the same time.
- Each line remains active until an inbound tag responds to it.

#### 1.7.3.1 Address-Out

- Address-out normally identifies information on bus-out as an address.
- On a halt-I/O instruction, address-out instructs the control unit on the interface to disconnect.

The channel transmits a signal over the address-out line (Figure 1-16) to indicate either of two conditions:

1. Address-out initiates selection of an I/O device causing all attached control units to attempt to decode the address on bus-out lines. Because each control unit address is different, only one unit can decode the address. If the control unit that recognizes the address is not busy, it must respond by conditioning operational-in when select-out is conditioned to that control unit.



\* Control Unit must drop Op-in within 6µsec.

\*\* Select-out rises a minimum of 400 ns after address-out

\*\*\* Rise of Op-in causes address-out to fall.

A Meaning to 2841

B Logical Circuit

22332 B

Figure 1-16. Address Out

Address-out precedes the rise of select-out by at least 400 nanoseconds. The channel must hold address-out active until it receives operational-in, select-in, or status-in. Select-in indicates that no control unit decoded the address. This occurs when the specified control unit is off line. Status-in indicates that the designated control unit is busy and cannot be interrupted to execute another operation. The channel responds to the status-in reply by canceling select-out. It then waits for status-in to fall and cancels address-out.

2. On a Halt I/O instruction, address-out instructs the control unit on the interface to disconnect. If the unit is selected, the channel will:
  - a. Condition the select-out line (may already be up).
  - b. Receive operational-in from a control unit, (will already be up).
  - c. Condition the address-out line.
  - d. Cancel select-out and hold address-out active until the control unit allows operational-in to fall.

The control unit must cancel operational-in within 6 microseconds ( $\mu\text{sec}$ ) after receiving the interface disconnect indication. The I/O operation proceeds to the normal end, but the data is not transferred across the interface.

### 1.7.3.2 Command-Out

- This indicates a command byte on bus-out in response to address-in during channel initiated selection.
- It means "proceed" in response to address-in during control unit initiated selection.
- It causes the control unit to stack the status in response to status-in.
- It means "stop" in response to service-in.

The channel conditions the command-out line (Figure 1-17) to respond to a signal on an inbound tag line. During the initial selection sequence, the channel activates command-out to reply to address-in, indicating that a command byte is on bus-out lines. This command byte specifies the I/O operation to be performed. Only at this point in the initial selection sequence does command-out cause the selected control unit to decode the byte on bus-out lines.

A command-out response to service-in means "stop" and causes the control unit to terminate the data transfer.

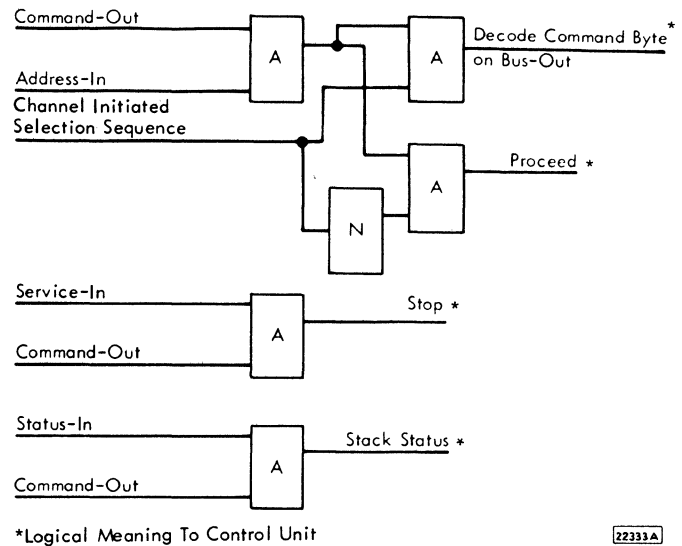


Figure 1-17. Command Out

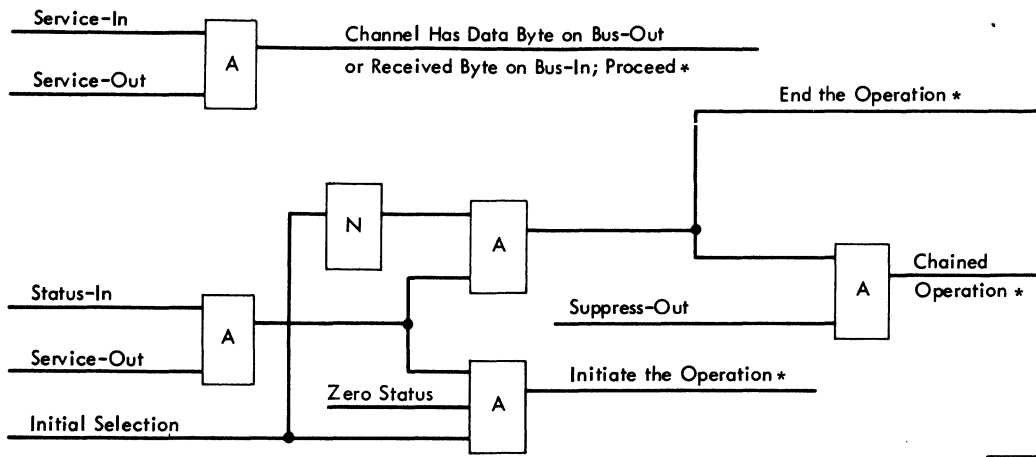
Whether during the initial selection sequence or at the end of the operation, the command-out reply to status-in causes the selected control unit to stack (hold) the status data. The control unit can present the stacked status only if suppress-out and address-out are down when select-out rises at the control unit.

### 1.7.3.3 Service-Out

- This identifies information on bus-out as data in response to service-in on write, search, and control operations.
- It indicates that the channel received data in response to service-in on read, and sense operations.
- It indicates that the channel accepted the status information in response to status-in.
- It indicates chaining in response to status-in with suppress-out active.

Service-out, a line from the channel to all attached control units, signals the selected device when the channel recognizes a signal on the service-in or status-in line (Figure 1-18). A signal on the service-out line indicates to the selected device that the channel has accepted the information on bus-in, or has provided on bus-out the data requested by service-in.

When service-out is sent in response to service-in during read or sense operations, or to status-in,



\*Logical Meaning at Control Unit

Figure 1-18. Service Out

the service-out signal must rise after the channel accepts the information on bus-in. In these cases, the rise of service-out indicates that the information is no longer required to be valid on bus-in. When service-out is sent in response to service-in during a write, search, or control operation, the rise of service-out indicates that the channel has provided the requested information on bus-out. In this case, the signal must rise after the information is placed on the bus. Service-out must stay up until the fall of the associated service-in or status-in signal.

Service-out cannot be up concurrently with any other "out" tag.

A service-out response to status-in while suppress-out is up indicates to the control unit that the operation is being chained. See Suppress-Out for further details. The status is accepted by the channel.

#### 1.7.4 Inbound Tag Lines

- These lines carry instruction signals from the control unit to the channel.
- They identify information on bus-in lines.
- They remain active until an outbound tag responds to it.
- Two "in" tags cannot be active at the same time.

Control units transmit instructional signals to the channel over inbound tag lines. Two or more inbound tag lines cannot be active concurrently. The control unit must hold the inbound tag line active until the channel responds by conditioning an

out-bound tag line. The control unit must then cancel the signal on the inbound tag line to allow the channel to drop the responding outbound tag line.

#### 1.7.4.1 Address-In

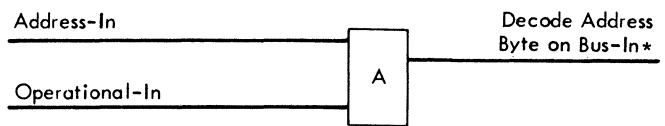
- This identifies information on bus-in as an I/O unit address.
- The channel responds with command-out.

Address-in is a line from all attached control units to the channel (Figure 1-19). It is used to signal the channel that the address of an I/O unit is on bus-in. The channel responds to address-in with command-out.

Address-in remains active until the rise of command-out. It must then fall in order that command-out can fall.

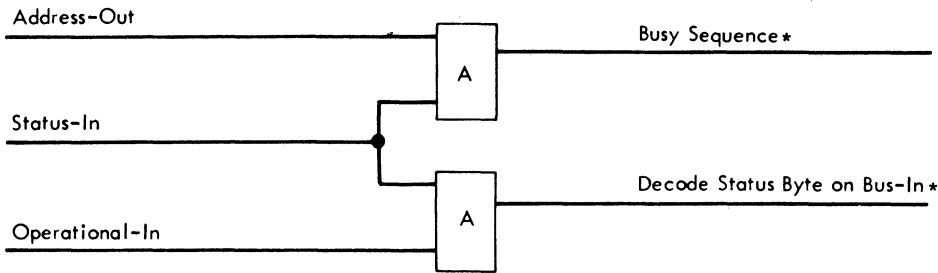
#### 1.7.4.2 Status-In

- This identifies information on bus-in as status information.
- It remains up until command-out or service-out rises, or until select-out falls if address-out is up.



\*Meaning to Channel

Figure 1-19. Address In



\*Meaning to Channel

22336

Figure 1-20. Status In

A control unit activates the status-in line to indicate to the channel that a status byte is on the bus-in lines (Figure 1-20). The status byte has a fixed format and contains bits describing the current status at the control unit.

Status-in must remain up until the channel responds with:

1. Service-out, indicating that the channel accepted the status.
2. Command-out, indicating that the channel has suppressed the status.

If status-in is the control unit's reply to address-out, during initial selection, it must remain up until select-out falls.

#### 1.7.4.3 Service-In

- This identifies information on bus-in on data read or sense operations.
- It indicates a control unit request for data on write and control operations.
- It remains up until command-out or service-out rises.

A control unit activates the service-in line (Figure 1-21) to:

1. Signal the channel that a data byte is on the bus-in lines (read, or sense operations).
2. Request that the channel transmit a data byte on the bus-out lines (write, search, or control operations).

The channel responds to service-in with:

1. Service-out, when data is accepted or transmitted.

2. Command-out, to stop data transfers and end the operation.

#### 1.7.5 Interlock Lines

- These lines permit only one control unit on the interface at a time.
- They gate the tag lines.
- They reset the control unit.

##### 1.7.5.1 Operational-Out

- Gates on all interface lines except suppress-out.
- Operational-out provides a reset to the control units.

Operational-out (Figure 1-22) originates at the channel, rising when the CPU is power-on reset. It stays up as long as the channel is operable. The fall of operational-out resets control units on the interface either selectively or concurrently depending on the status of suppress-out, a special control line (Figure 1-24). Operational-out is a gate on all outbound tag lines. Outbound tag lines have no effect if operational-out is down. If the channel drops operational-out while a control unit is operating on the interface, the operation must be reset. If the operational-out and the suppress-out lines are down concurrently for 6 microseconds, all control units operating in the on-line mode are reset.

##### 1.7.5.2 Operational-In

- This line signals the channel that a device is selected.
- It remains up until select-out falls and the signal sequence is completed.

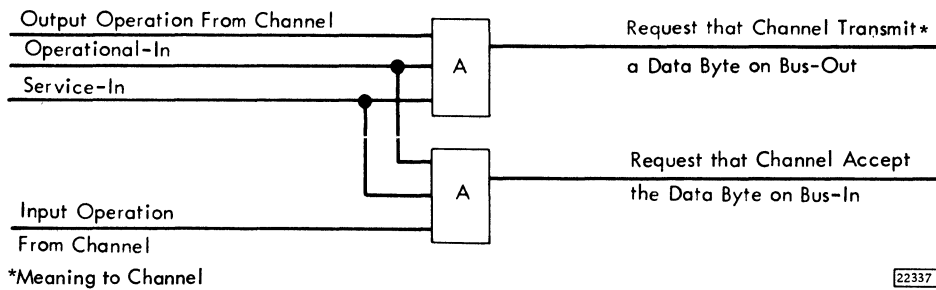


Figure 1-21. Service In

To initiate an interface signal sequence, a control unit conditions operational-in while the incoming select-out line to the control unit is up. The control unit must, at the same time, block select-out from reaching the next control unit. No other control unit can connect to the interface while operational-in is up.

When operational-in is raised for a particular signal sequence, it must stay up until all required information is transmitted between the channel and the device. Operational-in must drop at the same time, or after the rise of the outbound tag associated with the transfer of the last byte of information, if select-out is down. For burst-mode devices, operational-in can drop, if select-out is down or drops after receipt of the stop signal sequence.

Signals on bus-in and on the inbound tag lines are significant only when operational-in is up except in the case of the control-unit-busy selection sequence. When operational-in is down, the channel must disregard any signals on these lines. On the other hand, each control unit must provide interlocks to ensure that it does not place any signals on bus-in and the incoming tag lines unless its operational-in line is up.

### 1.7.6 Special Controls

- The four special-purpose lines are:
  1. Clock-out.
  2. Metering-out.
  3. Metering-in.
  4. Suppress-out.

#### 1.7.6.1 Clock-Out

- This indicates when the CPU is in a halt or wait condition.

- It designates when the control unit is free to change status.

The clock-out line (Figure 1-23) carries signals from the channel to indicate to each control unit that the processing unit is not in the halt or wait condition. Because a control unit can switch between the enable and disable states only when the processing unit is halted or waiting, clock-out designates the interval at which a control unit is free to change states. When the customer meter that registers processing unit time is disabled and the meter that indicates CE processing unit time is recording, the channel does not condition clock-out.

#### 1.7.6.2 Metering-Out

- This conditions customer meters to register time.

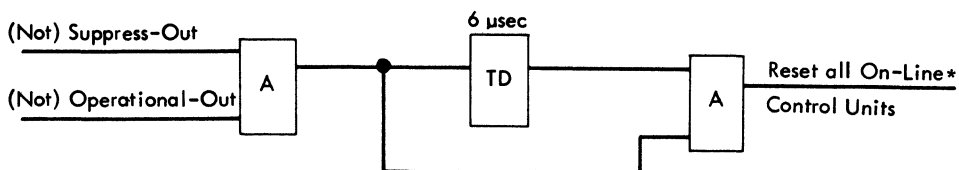
The channel transmits metering-out to each control unit when the customer meter is recording processing unit time. Metering-out causes customer meters to register time in each control unit that is not disabled.

#### 1.7.6.3 Metering-In

- This indicates to the channel that the customer meter is recording time.

A control unit transmits metering-in to the channel when the customer meter on the control unit is recording time. Metering-in causes the customer meter that records use of the processing unit to accumulate time even though the processing unit may be in the halt or wait condition.

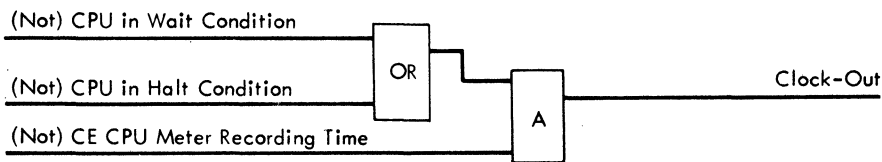




\*Meaning to Control Units

22338

Figure 1-22. Operational Out



22339

Figure 1-23. Clock Out

#### 1.7.6.4 Suppress-Out

- The suppress-out line has these functions:

1. Suppress status.
2. Suppress data transfer.
3. Chain command control.
4. Selective reset.

Suppress-out is used alone or with an outbound tag line to provide the following special functions (Figure 1-24).

**Suppress Status:** When a control unit ends an I/O operation, it transmits a status byte on bus-in lines and conditions the status-in tag line to the channel. The status byte indicates whether errors were encountered in performing the operation and signals the channel that the operation is complete. A channel may respond to status-in with command-out, causing the control unit to stack the status data.

The next time select-out rises at a control unit holding stacked status data, that control unit will not activate the interface to present the status byte if suppress-out is active. The channel must condition suppress-out at least 250 ns before the control unit receives select-out to ensure that the stacked status data is not transmitted. The rise of suppress out, after a control unit begins a status cycle, does not interfere with the transmission of the status byte. If a control unit conditions request-in to offer status data, and suppress-out rises before the control unit receives select-out, suppress-out drops request-in.

**Suppress Data Transfer:** For noncyclic I/O devices (buffered I/O devices, not applicable to 2841) that can wait for data transfers without indicating an overrun condition, suppress-out blocks service-in. The channel must condition suppress-out at least 250 nanoseconds before the previous service-out tag drops to ensure that the subsequent request for data or offer of data will be suppressed.

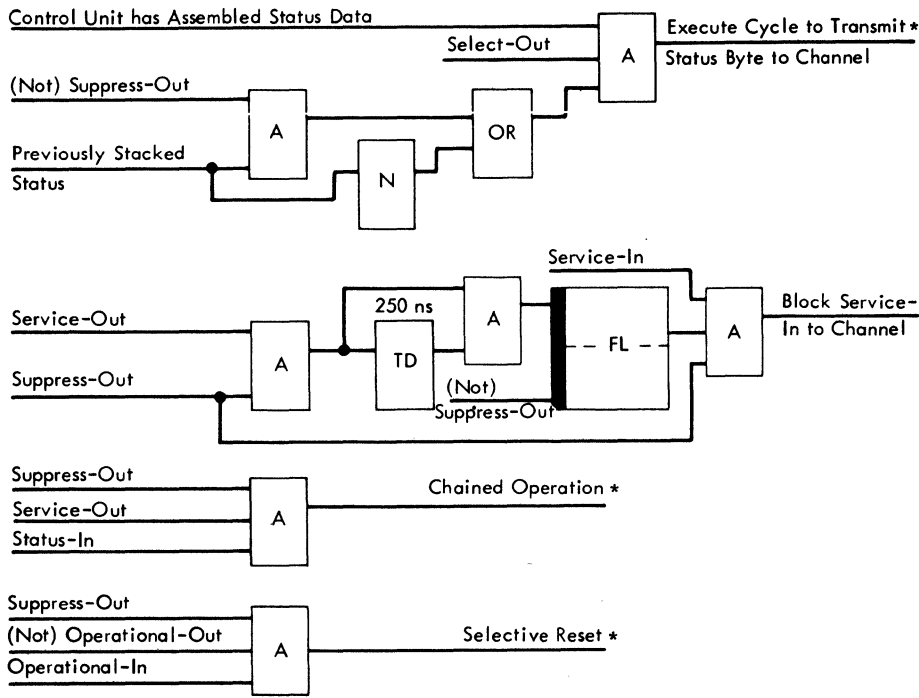
**Chain Command Control:** To indicate a chained command, the channel conditions suppress-out after the selected control unit begins the cycle to transfer the ending status byte and before the channel responds to status-in with service-out. The active state of the suppress-out line and the service-out response to status-in combine to hold selection of the control unit and the I/O device. The next command from channel must be directed to that control unit and I/O device.

**Selective Reset:** If the channel conditions suppress-out at least 250 nanoseconds before allowing operational-out to fall and holds suppress-out active until 250 ns after operational-out rises again, only the I/O device presently operating on the interface is reset.

### 1.8 INTERFACE OPERATIONS

#### 1.8.1 Initial Selection Sequence

- In this sequence the channel:
  1. Selects a control unit and device
  2. Specifies the operation to be performed.



\*Meaning to 2841  
 \*\*Not used by 2841

22340

Figure 1-24. Suppress Out

- The sequence is standard for all units and operations.

The interface signal sequence in which the channel selects a control unit and I/O device and specifies an operation to be performed is called the initial selection sequence (Figure 1-25). Regardless of the unit selected or the operation designated, the signal sequence in the initial selection is standard.

The channel begins the initial selection sequence by transmitting an address byte on bus-out lines and conditioning address-out. The address byte selects the unit to execute the operation. Each control unit attached to the interface attempts to decode the address, but, because all interface addresses are different, only one unit can interpret the coded byte.

When select-out is active at the control unit that successfully decodes the address byte, that control unit conditions either:

1. Status-in, indicating that the selected unit is busy and cannot execute another operation, or
2. Operational-in, indicating that the designated unit will complete the initial selection sequence.

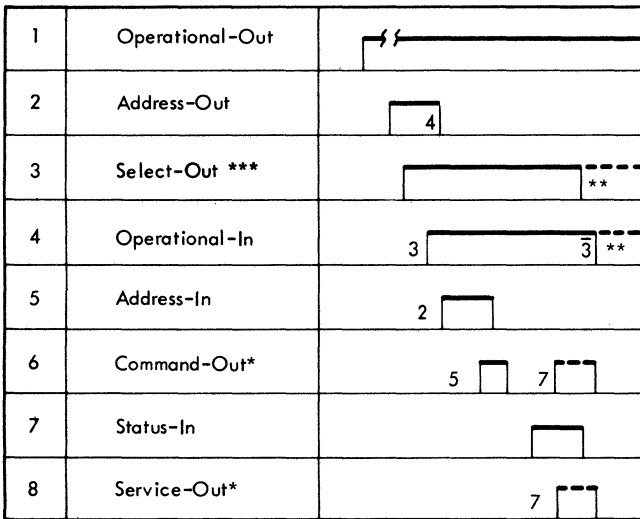
However, the operational-in response to address-out does not commit the control unit or the channel to perform an operation.

If no control unit decodes the address byte (specified control unit is off line, the address byte is invalid, etc), the control unit with the lowest priority propagates select-in to the channel when its incoming select-out is conditioned. The select-in or status-in reply to address-out causes the channel to cancel-out and terminate the selection sequence.

When operational-in causes the channel to drop address-out, the selected control unit transmits an address byte on bus-in lines and conditions the address-in line. The channel compares this address to the address it placed on the bus-out lines to ensure that the right device has answered.

After checking the address, the channel responds to address-in by transmitting a command byte and conditioning command-out to the control unit. The command byte designates one of the thirty-four operations and establishes conditions to control execution of the operation.

The control unit must then drop address-in, and after command-out falls, the control unit places its



\* A multiplex channel will respond to status-in with either command-out or service-out. Normally, a selector channel will respond to status-in with only service-out.

\*\* Depending on the channel controlling the operation, select-out might drop during the initial selection sequence or remain active after the sequence is complete. Operational-in cannot drop until select-out is inactive.

\*\*\* Select-Out and Hold-Out up together.

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Figure 1-25. Initial Selection Sequence

status information on bus-in and raises status-in. If the I/O device is available, the status byte is zero. If the channel accepts this status byte, it responds with service-out. The signal completes the initial selection sequence.

**Polling:** When a control unit that does not have operational-in up requires service, it raises its request-in line to the channel. The next time select-out rises at any control unit requiring service and no I/O selection is being attempted by the channel (address-out down), the control unit places the address of the device on bus-in. It then signals on both the address-in and the operational-in lines, and removes the request-in signals. When the channel recognizes the address, a command-out signal is sent to the control unit, indicating "proceed." After address-in drops, the channel responds by dropping the command-out signal. The remainder of the sequence is the same as a channel-initiated initial selection sequence.

### 1.8.2 Data Transfers

- A control unit can send data to, or request data from the channel.
- Service-in and service-out are the controlling tag lines.

Data transfer may be requested by a control unit after a selection sequence. To transmit to the channel, the control unit places a data byte on bus-in and raises service-in; the tag and the validity of bus-in must be held until an outbound tag is raised in response. To request data from the channel, service-in is raised. The channel places the data on bus-out and signals with service-out. The channel maintains the validity of bus-out until service-in falls. When service-in falls, the channel responds by dropping service-out.

### 1.8.3 End Operation

- An operation is completed when the control unit and device present ending status to the channel.
- The channel acknowledges receipt of the status byte with service-out or command-out.

When any I/O operation except test I/O and command immediates have proceeded to their normal end, the control unit assembles and transmits a second status byte to the channel. The meaning and format of this status byte are identical to the purpose and format of the status byte transmitted during the initial selection sequence.

To acknowledge receipt of the status byte, the channel conditions either service-out or command-out. Service-out indicates that the channel has accepted the status data and resets the operation. Command-out causes the control unit to stack the status.

If the channel conditions suppress-out 250 ns before select-out rises at the control unit holding stacked status data, the control unit does not transmit the status byte again until suppress-out drops. When the channel cancels suppress-out, and select-out to the unit is active, the control unit sends its address, and retransmits the status byte to the channel (Polling).

If the channel does not condition suppress-out before select-out rises at the control unit holding stacked status data, the control unit initiates another cycle to transmit the status byte again.

The ALD's for the 2841 stage 2 are drawn for full feature operation. This means that the ALD's show the blocks used by all of the special attachments even though on a given machine one or more of the features may not be installed.

A code name or number for one of the features appears in the block on the ALD under the card type (A, OR, N, etc.). This line is blank if the block is for the basic machine. If a code name appears in the block, the circuit is only in the machine if the feature is installed. In some cases jumpers are installed if the feature is not installed and is indicated on the card type line.

The codes are:

WCH2 = Two Channel Switch  
 WDRM = 2303 Drum Storage  
 DCDR = 2321 Data Cell Drive  
 DSKA = 2302/2321 Attachment  
 2302 = 2302 Attachment  
 NCH2 = Not Two Channel Switch  
 NDRM = Not 2302  
 NDCD = Not 2321  
 DSAS = 2302 Additional Storage  
 OPTA = Optional Features Gate A

The SLT large boards are wired for full feature operation. Features are added or removed by adding or removing cards and jumpers or in some cases large boards.

The ALD volumes include the Maintenance Diagram Manual (MDM's). The MDM includes: The unit data flow for the basic 2841 circuits, data flows of the channel and device attachments, logic flows of 2841 operations, error check analysis diagram, I/O operation diagrams, timing charts, and track format charts.

## 2.1 MACHINE CLOCK

- Provides basic timing pulses for 2841.

The machine clock consists of a four latch ring counter (Figure 2-1) which gives four equal timed output pulses of 250 ns duration each. These pulses are labeled clock 1, 2, 3, and 4 and are distributed to each board of logic within the machine.

Each board converts these pulses to form other pulses, clock A, B, C and D. Each one of these pulses is 125 ns in duration (Figure 2-2).

The clock is free running and is only stopped during a power-on-reset. This resets clock 1, 2, and 3 and turns on clock 4.

## 2.2 REGISTERS

- The basic 2841 contains 19 registers; A, Partial Sum, GP, ER, GL, BY, BX, FR, KL, DL, DH, OP, ST, UR, DW, DR, W, X, and IG (Figure 2-3).
- A, Partial Sum, W, X and IG registers have specific uses as explained later.
- All registers except ER, W and ST contain 8 bits.
- The abbreviation used to designate each register has a specific meaning during particular operations but no meaning at all during other operations. The use of these registers within a particular microprogramming sequence is covered in detail in Chapter 3.
- The A register and B bus are entry points to ALU.
- The DR register can be used as a general purpose register. In read or write sequences, it is used as a buffer to SERDES.
- The ST register is primarily used by the microprogram for branching decisions.
- The ER register is used to hold conditions that occur during an operation; write-data-error, halt I/O, bus-out-parity, control-unit-addressed while busy, ALU check, and address-out.
- The W and X registers are used for TROS addressing.
- The IG register is used for channel control.
- IG and IH are gates for bus-in and bus-out.

### 2.2.1 General Purpose Registers

The following 11 registers contain 8 bits plus parity and use polarity hold latches. The register abbreviations are explained, but it should be understood that

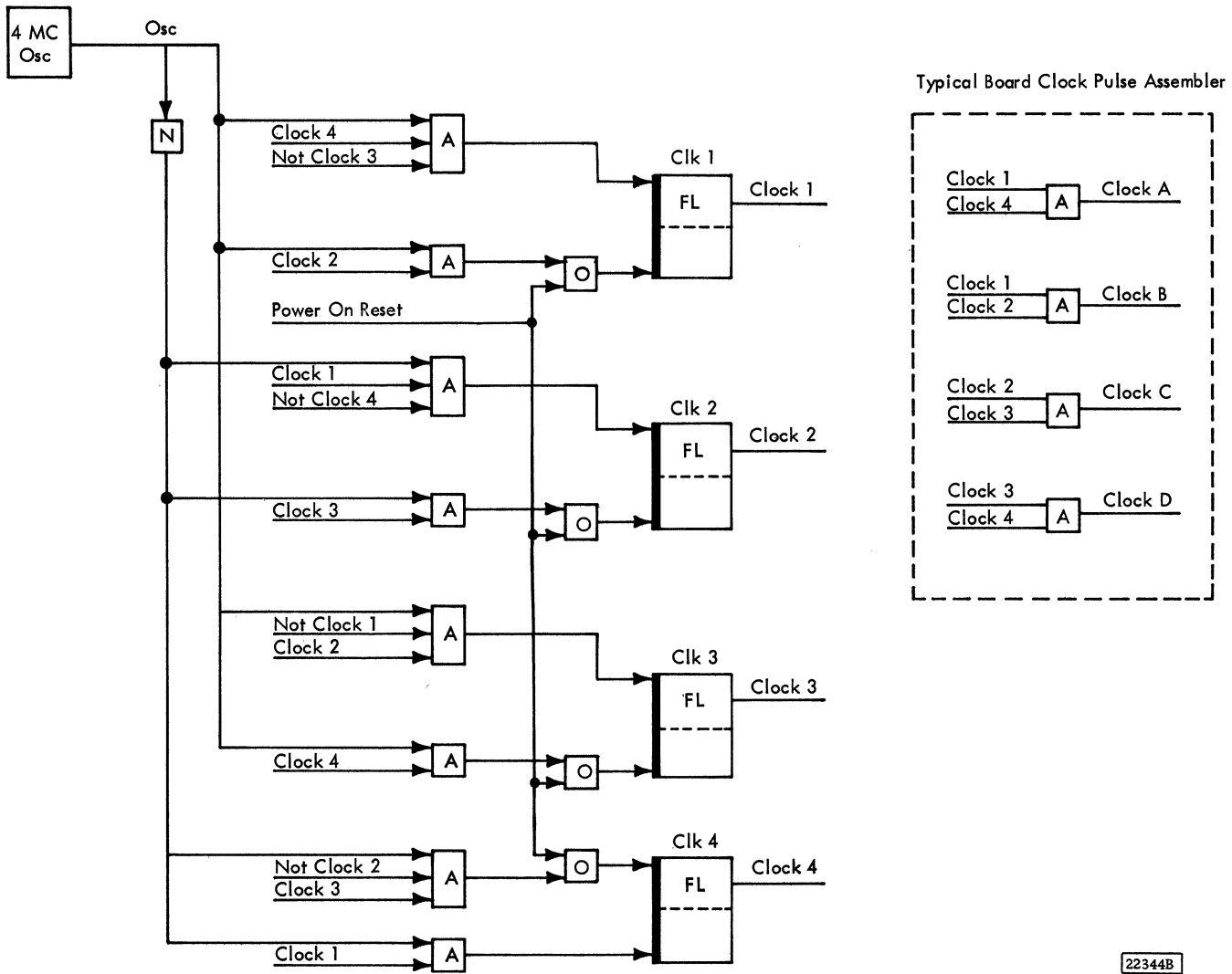


Figure 2-1. Machine Clock

these registers are general purpose registers and may or may not serve the particular function designated by their abbreviation. Chapter 3 contains a detailed explanation of the use of these registers in a particular microprogramming sequence.

1. GP - general purpose register
2. GL - gap length register (not used for this purpose)
3. BY - code check burst register
4. BX - code check burst register
5. FR - flag register
6. KL - key length register (not used for this purpose)
7. DL - data length low register
8. DH - data length high register
9. OP - operation code register

10. UR - unit address register
11. DW - data write register

All of the general purpose registers (Figure 2-3) have an output to ALU on the A-bus. In addition the BY Register may also be gated to ALU on the B bus. UR is also used to select a particular file.

### 2.2.2 A Register

This register serves as the common entry to the arithmetic/logic unit from the A-bus. It contains 8 bits plus parity and uses polarity hold latches (Figure 2-3).

### 2.2.3 Partial Sum Register

The partial-sum-register is one entry to the ALU. The partial-sum-register is set by the output of

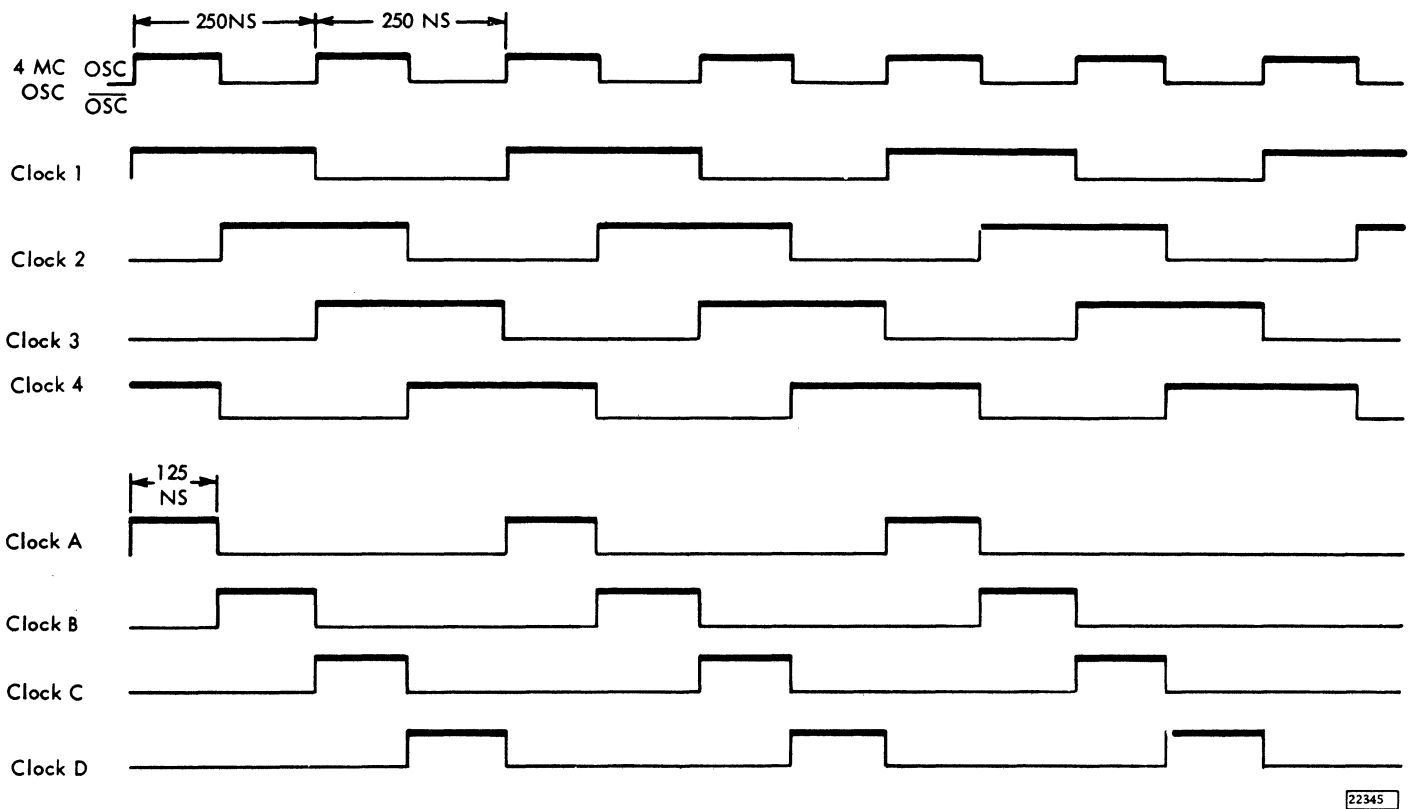


Figure 2-2. Machine Clock Timing

exclusive ORing the A register output with the B bus. The register contains 8 bits, 0-7, and uses polarity hold latches.

#### 2.2.4 DR Register - Data Read Register

The DR register consists of 8 bits plus parity and uses polarity hold latches (Figure 2-3). Inputs to DR are from CE switches, ALU (D-bus), or the file data register (in SERDES) when reading. Outputs of DR are to the A or B-register assemblers, or to FDR (in SERDES) when writing.

It should be noted that, when reading, DR may or may not contain good parity since parity is not assigned until the read byte is transferred from DR through ALU to one of the general purpose registers.

It should also be noted that the transfer of data from FDR to DR (Read) is not under microprogram control. Whenever FDR has a byte (8 bits), this byte will be transferred to DR. The microprogram is notified of this transfer by setting of status register bit 4 (means DR is full on a read). The microprogram must move this byte out of DR within approximately 6.4  $\mu$ sec (2311) or the next byte from the 2311 will destroy the original byte in DR. When writing, the

transfer of data from DR to FDR is also outside of microprogram control. Whenever FDR is empty, DR will be transferred to FDR. The microprogram will be notified of this transfer by the setting of status register bit 4 (DR has been used on a write). Unless the microprogram reloads DR with a new byte of data within approximately 6.4  $\mu$ sec (2311), the original byte will be retransferred to FDR and written on the disk storage again.

#### 2.2.5 ST Register - Status Register

The status register (ST) consists of 8 bits (no parity) and uses flip latches (Figure 2-3). The ST is used by the microprogram for branching control. That is, bits in the status register may be set and reset under microprogram control to indicate conditions within the machine; i. e., ST 6 on could mean write gate is on, ST 7 could mean erase gate is on. The microprogram can, at a later time, branch on status bits to the proper routine, i. e., ST 6 on and index - drop write gate.

The ST register has inputs from the D-bus (in CE mode only) and the status assembly logic (one bit at a time). It has outputs to the A-bus (in CE mode only) and the CH-CL branching circuits.

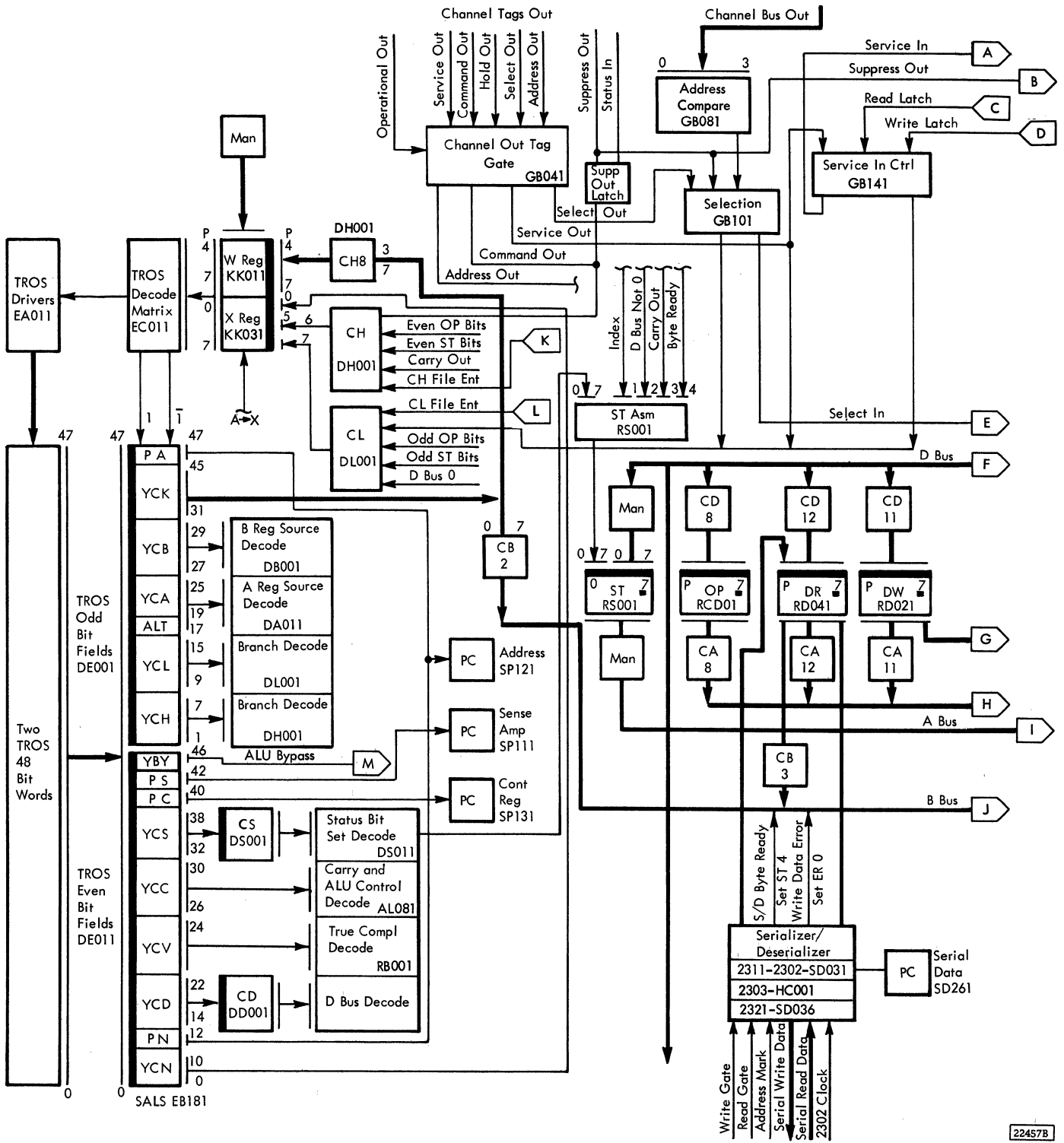
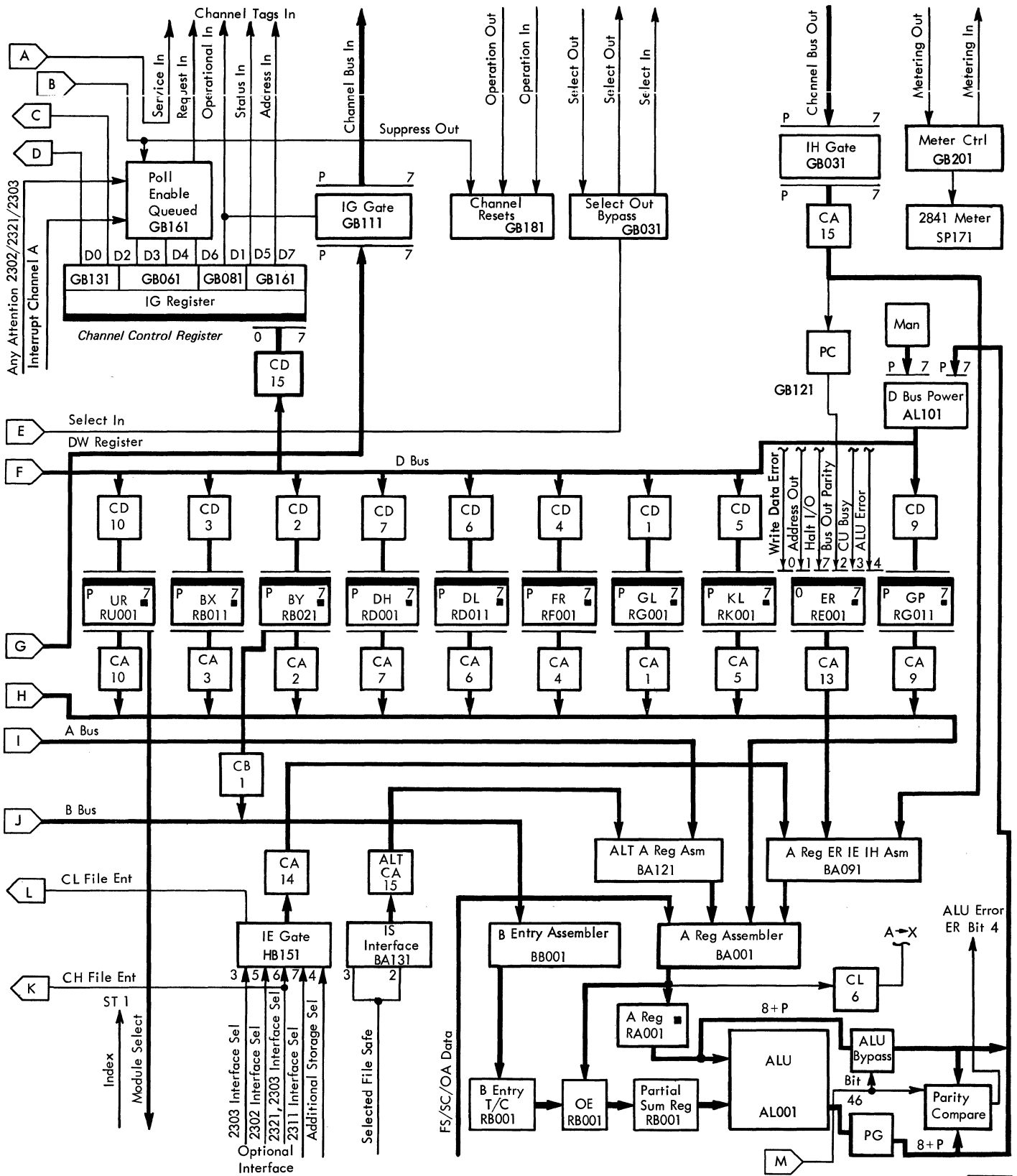


Figure 2-3a. Data Flow - Basic 2841 and Channel Attachment



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Figure 2-3b. Data Flow - Basic 2841 and Channel Attachment



The following status bits have definite meanings. ST(1) - Turned on with a selected index pulse after a microprogram statement of 1→ST(1). The statement 1→ST(1) turns on the allow index latch.

A CL decode of 14 (CL statement INDEX) allows the microprogram to branch on ST(1) after it is set by the index pulse.

ST(1) is reset by the statement 0→ST(1).

ST(4) - Read Operation - Turned on when FDR is transferred to DR. Means DR is full. Write operation - Turned on when DR transferred to FDR. Means DR has been used.

The other status bits are used by the microprogram for different meanings in different sequences. Chapter 3 has a more detailed discussion of the use of status bits within a particular microprogram sequence.

### 2.2.6 ER - Error Register

This register is used to hold conditions that occurred during an operation. It consists of six flip latches (Figure 2-3).

ER(0) is set on if there is a serial data error in SERDES during writing. ER(0) lights the data check lamp. Op In reset turns off the ER(0) flip latch and turns off the lamp.

ER(1) is not a latch. However, address out is gated into the ER(1) assembler for testing by the microprogram.

ER(2) is set on if bus out parity is detected on the command or data bytes. ER(2) lights the data check lamp. Op In reset turns off the ER(2) flip latch and turns off the lamp.

ER(3) is set on during the short control unit busy sequence. When the control unit goes not busy, the microprogram initiates a control unit end polling interrupt sequence. A more detailed description of the short control unit busy sequence is found under Channel Interface Attachment, 2.3.

ER(4) is set on under the following situation:

1. ALU bypass being used- (A register to D bus), and,
2. A register parity does not agree with parity computed by ALU, and
3. Bus-out parity did not occur on this byte.

ER(4) lights the data check lamp and the machine stops.

ER(7) is set on by a halt I/O command. It is also used in the short control unit busy sequence in setting of ER(3).

## 2.2.7 Miscellaneous Registers and Controls

### 2.2.7.1 TROS Addressing Registers

The W and X registers are used to address the transformer read only storage (Figure 2-3). W and X contain 12 bits giving the 2841 the ability to address 4096 individual TROS words. Since the 2841 has only 2048 words (2K), the high order bit of the W Register is not used.

### 2.2.7.2 Channel Control Register (IG Register)

The IG register (Channel Control Register) is used to raise and lower tag-in (i.e., address in, status in) line to the channel. IG consists of 8 latches (Figure 2-3).

IG0 - Write latch - Used to set up the service in/out controls for write, search, and control operations

IG1 - Operational In (Op In). Used to reset the operation-in latch.

IG2 - Read latch - Used to set up the service in/out controls for read and sense operations.

IG3 - Queued latch - Used for presenting any status other than device end through the polling interrupt sequence. Raises request-in if suppress-out is down.

IG4 - Poll enable latch - Allows any gated attention to initiate a polling interrupt sequence. Raises request-in if suppress-out is down.

IG5 - Status In.

IG6 - Used for presenting outstanding device end to a multiplexer channel when command word chaining is indicated. This is accomplished by means of a non-suppressible polling interrupt sequence. Raises request in (not gated by suppress-out).

IG7 - Address In. Also conditions operational in.

### 2.2.7.3 Service In/Out Controls

In addition to IG, five latches (transfer control 1, transfer control 2, service request, service in, and steering latch A) are used for controlling responses to the channel (Figure 2-3).

### 2.2.7.4 Bus Out Gates

IH is a set of 9 gates. It allows bus out to be gated to the A bus (Figure 2-3).

### 2.2.7.5 Bus in Gates (IG Gates)

IG gates (Bus In Gates) is a set of 9 gates. It is tied directly to the DW register and is used for gating data to the channel (Figure 2-3).

## 2.3 2311 INTERFACE ATTACHMENT

- The 2311 interface attachment (Figure 2-4) consists of:

1. Two registers (FC and FT).
2. Four gating networks (MS, SC, FS, OA).
3. Associated assemblers.

Assignment of device type (2311-2321-1302) to a module address is done by the CE, as requested by the customer, by changing constants in the microprogram. For the 2311, the microprogram sets FT register bit 7 to select the 2311 Interfaces.

Unit selection is done by decoding the three position field with the microprogram. A binary zero (000) decodes to UR register bit 0 and a binary seven (111) decodes to UR register bit 7.

### 2.3.1 FT - File Tag Register

The file tag register (Figure 2-4) consists of eight polarity-hold latches. It is used to raise and lower tag lines to the 2311, and to identify the file type (FT-7) to the 2841. Polarity hold latches are used so that individual bits in the register may be turned on or off without affecting the remainder of the register. The D bus output (Figure 2-5) is the control input to the polarity hold latch. CN-5 is the data input to the latch.

#### Example 1

Assume the following:

1. FT is equal to zero
2. ALU statement says  $128 \rightarrow FT$ . CN-5 equals a one.

All eight FT latches have a data input of one but only BIT 0 has control. Therefore bit 0 is the only latch affected and is turned on.

#### Example 2

Assume the following:

1. FT equals 128

2. ALU statement says  $128 \rightarrow FT$
3. CN-5 equals 0

All FT latches have a data input of zero. Bit 0 is the only latch that has control. Therefore bit 0 is the only latch affected and is reset.

### 2.3.2 FC - File Control Register

The file control register (Figure 2-4) consists of eight polarity-hold latches and is similar to FT in operation. It is used in conjunction with the FT register to define an operation to the device. For example:

1. FC2 = 1, FT0 = 1 - Return to zero
2. FC2 = 1, FT1 = 1 - Load CAR in 2311 with 2
3. FC2 = 1, FT2 = 1 - Select head 2 - go backward when you receive Seek Start
4. FC2 = 1, FT3 = 1 - Load the 2311 Difference Counter with 253 (ones complement of FC)

FC (Figure 2-5) uses polarity-hold latches and CN-5 so that individual latches may be affected without disturbing the remainder of the register. For example:

Assume:

- FT0 = 1 - Control tag
- 140 → FC - Head select, write and erase gates are on

The microprogram is operating on a write CKD command. When index is detected write gate is dropped.

Solution:

Index reached - ALU statement will say  $128 \rightarrow FT$  and CN-5 equal to zero. All latches have a zero data input. Only 0 has control, therefore, only bit 0 is affected and is turned off.

### 2.3.3 MS - Module Select Gates

MS is a set of gates (Figure 2-4) used in selecting a particular file. The unit address register (UR) (Figure 2-3) contains the module select number (one of the 8 bits on). This is fed to MS. If FT bit 7 is on, the contents of UR is gated through MS to the 2311.

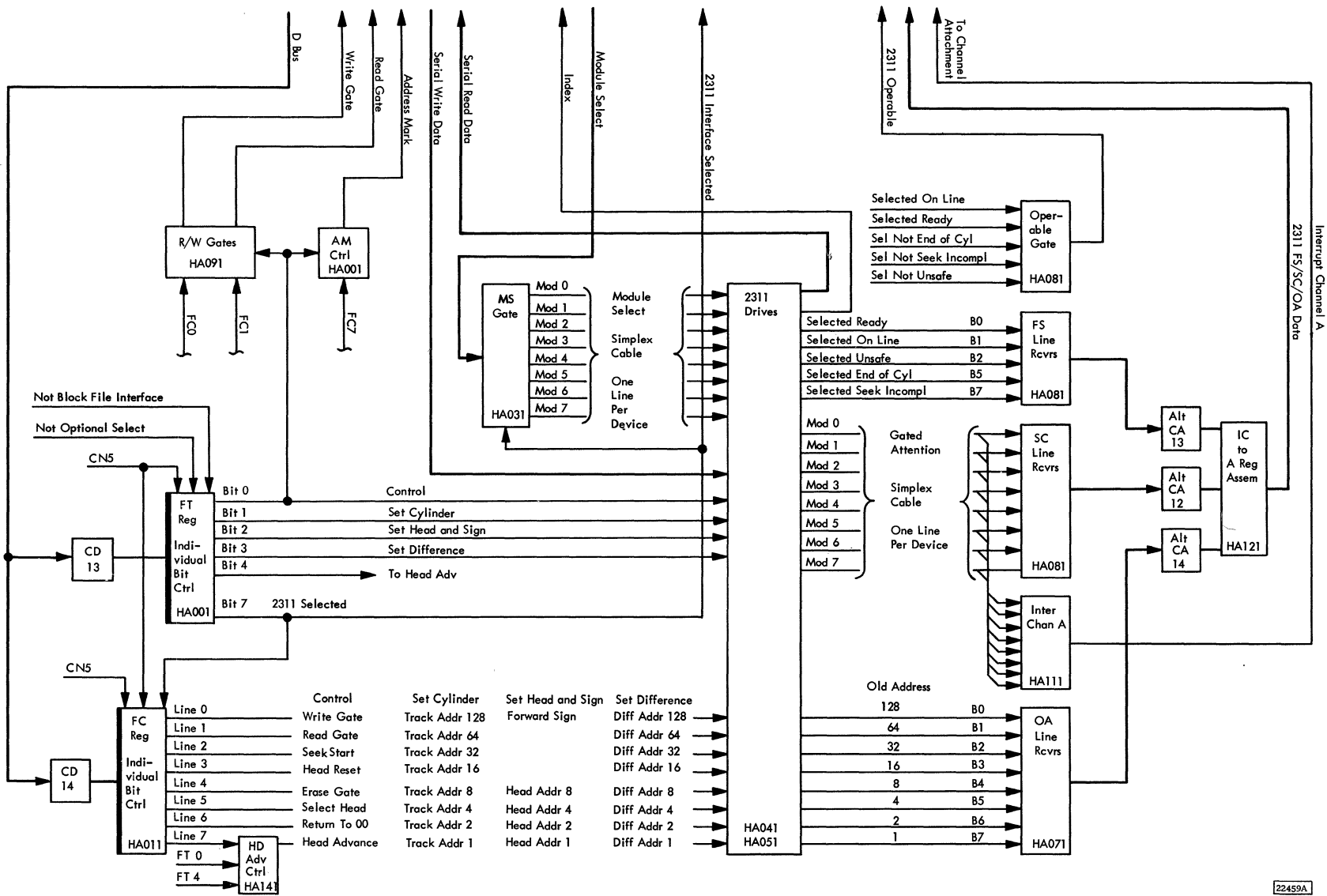


Figure 2-4. Data Flow - 2311 Attachment

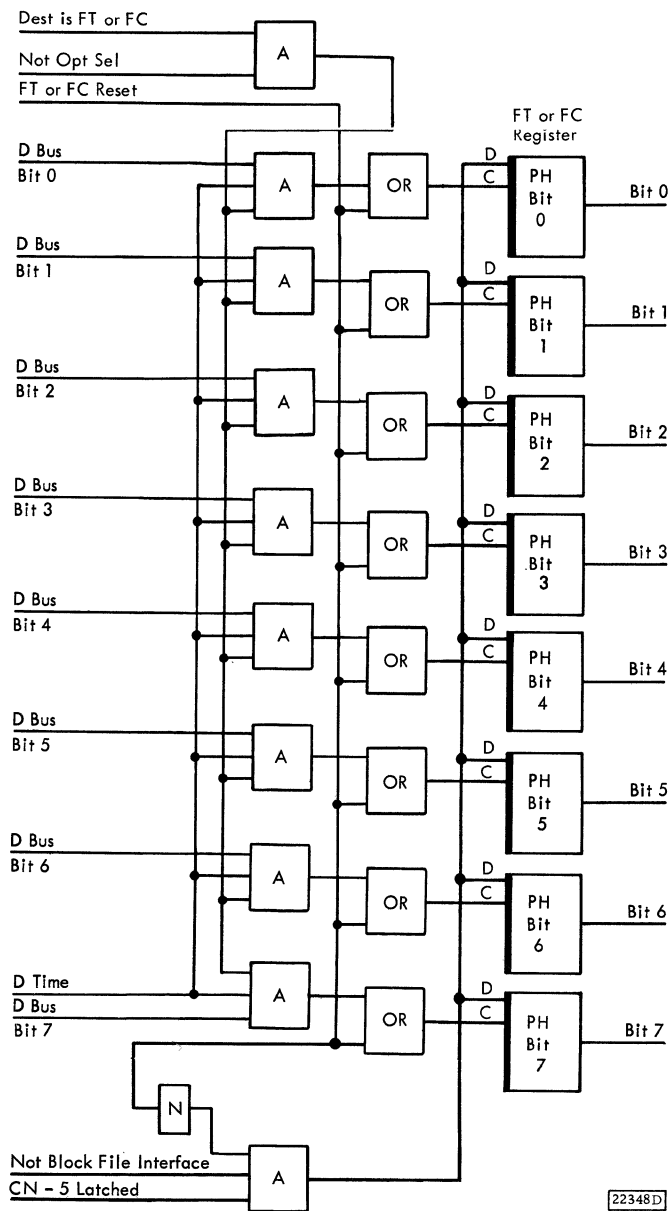


Figure 2-5. FT or FC Register

### 2.3.4 SC - Seek Complete Gates

SC is a set of gates (Figure 2-4) used in gating gated attention (Seek Complete) from a 2311 to the 2841 A bus.

All gated attentions are ORed together and develop the interrupt-channel-A line, interrupt-channel-A is sent to the channel interface. If the poll enable latch is on and the channel is not selected to some other control unit, interrupt-channel-A causes request-in to be raised. This initiates a polling interrupt sequence with the channel.

### 2.3.5 FS - File Status Gates

FS is a set of gates (Figure 2-4) used in gating file status from a selected 2311 to the 2841 A bus. Five status bits are transferred from the 2311 to the 2841.

Name	Bit Positions in FS
Ready	0
On Line	1
Unsafe	2
Strip Ready (Forced)	4
End-of-Cylinder	5
Seek Incomplete	7

Unsafe and seek incomplete are error conditions. End-of-Cylinder indicates that an attempt has been made to advance the head address register in the 2311 past 9.

Ready, on line, safe, not end-of-cylinder and not seek incomplete are ANDed together to develop file operable. File operable feeds IS bit 3. The microprogram can test this one bit to see if the file is functioning properly. If IS bit 3 is not on, then the microprogram can test FS to find out which condition caused the device to go not operable.

### 2.3.6 OA - Old Address Gates

OA is a set of gates (Figure 2-4) used in gating the cylinder address register in the selected 2311 to the 2841 A bus.

### 2.3.7 IE - Input Element Gates

The 2311 interface has a FT register. The 2302, 2303, and 2321 interfaces share another FT register. Particular bits in these registers are used to indicate to the microprogram (Figure 2-3) which type of device is selected. This is necessary since there are small differences in the internal operation of the 2841 for different devices. A summary of FT bits used and IE bit positions affected follows:

- 2311 FT-7 feeds IE-7
- 2302 FT-5 feeds IE-5
- 2303 FT-6 feeds IE-3 and IE-6
- 2321 FT-6 feeds IE-6

## 2.4 TRANSFORMER READ ONLY STORAGE - TROS

### 2.4.1 Purposes and Use of TROS

- Output of TROS controls machine functions.

- One output word of 48 bits is read out at a time.
- Output of word is called a micro-instruction.
- A chain of micro-instructions is called a micro-program.

The contents of any TROS word can be read out and stored in latches. This latched information is decoded and used to control machine functions. Part of the information read out of a particular TROS word is used to determine the next TROS word to be addressed.

The TROS words are addressed in a particular sequence, and this sequence of addresses is called a microprogram. To perform any operation in the machine, the various parts of the 2841 (ALU, registers, status bits, etc.) are controlled by the micro-program to perform certain functions in a given sequence.

#### 2.4.2 Characteristics and Capacity

- TROS contains fixed predetermined information.
- TROS can only be read out.
- A 12 bit address is used to select the next word to be read out.

TROS contains fixed, predetermined information which can only be read out. The stored information can be altered only by physically changing TROS.

TROS units can be built in various storage capacities. The 2841 stage 2 uses a 2K model of TROS-2 and a 4K model of TROS-2 if the 2303 feature is installed. Early models of the 2841 stage 2 with the 2303 feature use a 4K model of TROS-1. The TROS-1 and TROS-2 are functionally the same but differ in physical layout. There are 2,048 TROS words in the 2K model of TROS.

A 12 bit address register (W and X) is used to address the 2,048 words in the TROS unit. The TROS word in the 2841 is 48 bits long, and has a maximum possible length of 60 bits. The 12 additional bits are not presently used in any of the 2841 words.

TROS is built up of modular units, each having 256 addressable words, and each word having a length of 48 bits. The TROS for the 2841 contains 8 modules and has a capacity of 2,048 words.

#### 2.4.3 Principles of Operation

- TROS uses the current transformer principle.

- Sixty transformers are selectively linked with a drive line to provide one TROS word output (only 48 transformer positions are actually used).
- A drive line links with a transformer in positions where a 1-bit output is required.
- A drive line bypasses a transformer in positions where a 0-bit output is required.
- Each of two drive lines on one flexible plastic tape links the selected transformers.
- One of the two drive lines on each tape is selected to read out a TROS word.
- The TROS transformer consists of a U-core and an I-core.
- Etched copper drive lines on a plastic tape are selectively interrupted by punched holes to either link or not link transformers.

TROS Transformer Principle: When a current pulse is passed through the primary winding of a transformer (Figure 2-6), it induces a current pulse in the secondary winding. If no primary current pulse flows (or there is no primary winding), there is no output in the secondary winding.

Drive Line Linkage with Transformers: The primary of the transformer is an addressed drive line and the secondary of the transformer forms the sense winding. When a drive line links with a transformer core, a current pulse in this drive line induces a current pulse in the secondary winding. If the same drive line bypasses a transformer, no current pulse is induced in that particular sense winding. A pulse in the sense winding represents a 1-bit. No sense winding output represents a 0-bit. Additional drive lines could be used in a similar manner.

Example (Figure 2-6):

A current pulse in drive line A gives an output of 101.

A current pulse in drive line B gives an output of 011.

The 60 transformer cores associated with each TROS tape give an output of 60 bits (only 48 are used). Two drive lines for each set of 60 cores allow two different bit configurations depending on which drive line is selected.

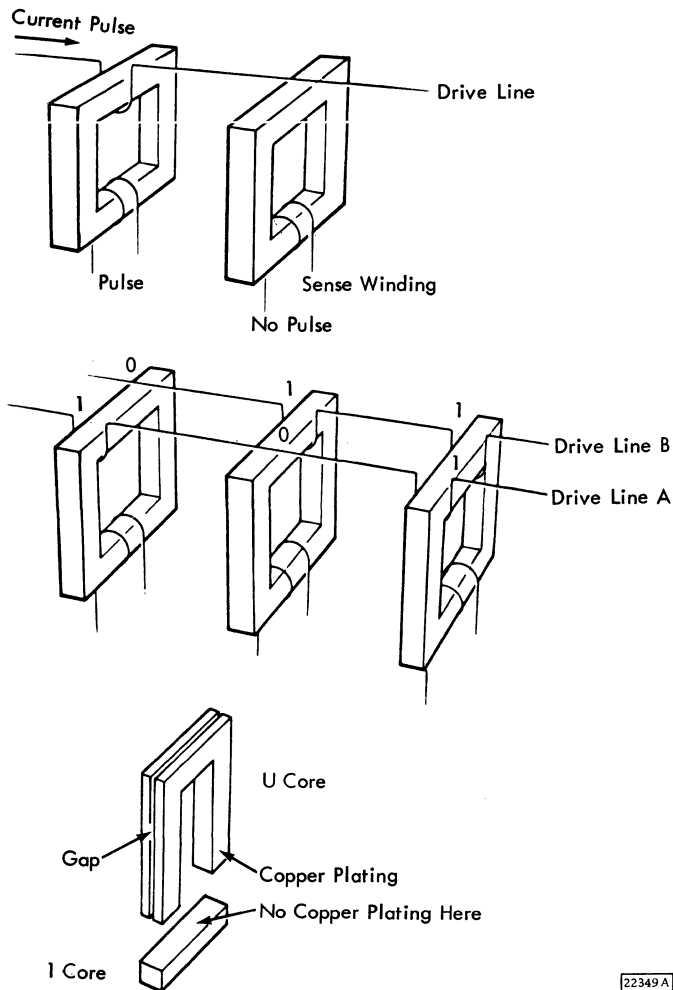


Figure 2-6. Principle of TROS

TROS drive lines are etched in copper on flexible plastic tapes. On each tape, two drive lines are printed, both in the form of a ladder network. Holes are punched between the rungs of the ladder so that U-cores can be inserted through the tapes to mate with the I-cores (Figure 2-7).

**Transformer Cores:** The core of a TROS transformer consists of two parts, a U-core and an I-core. Both the U-core and the I-core are made of soft, low-remanence ferrite. To reduce flux leakage, the U and I cores are first coated with an insulating material and then copper plated. A sense winding of 35 turns is wound on the I-core and the U-cores are gapped on their outside face to prevent the plating from acting as a short circuited turn.

**Interrupting the Drive Lines to Store a Logical 0 or 1:** Each leg of the U-core, when inserted in the tape, is encircled by the sides of the ladder network and

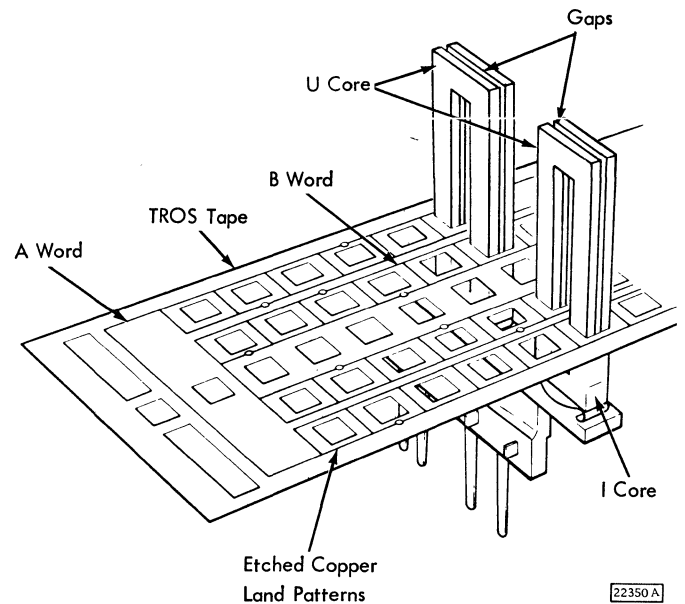


Figure 2-7. Tape with U and I Core

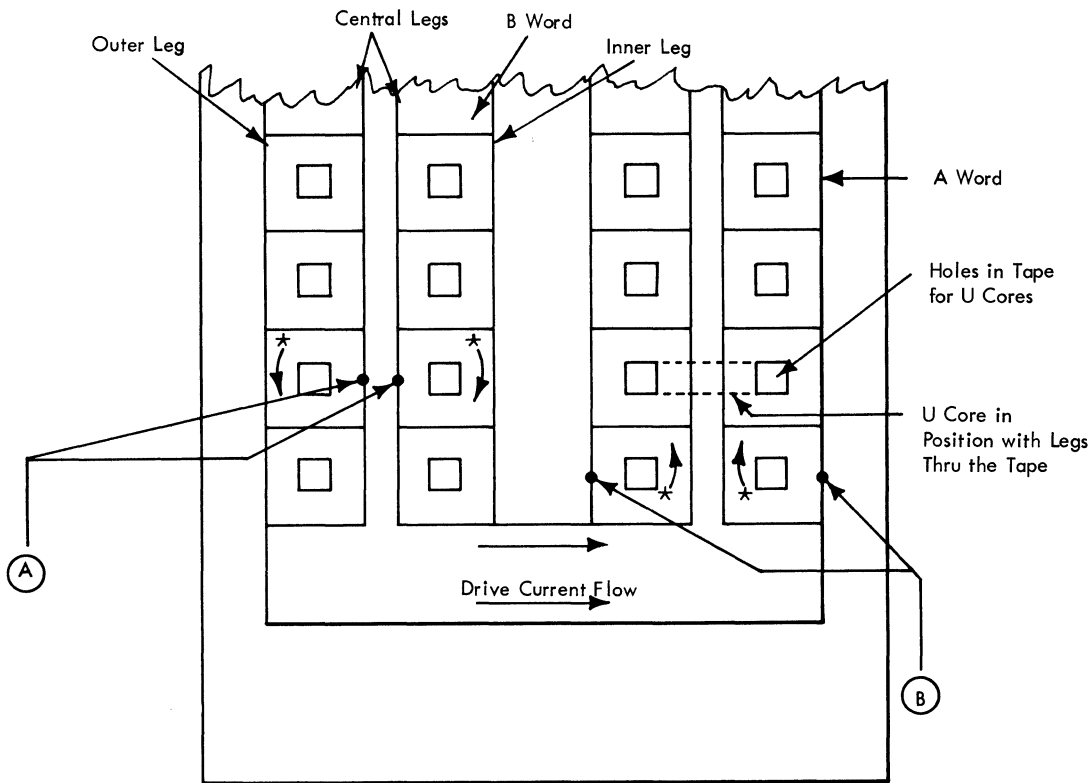
two of its rungs. By physically interrupting either side of the ladder, the conductor (drive line) may bypass or link with the core (Figure 2-8). In (A) of Figure 2-8, note where the sides of the ladder must be punched to obtain a logical 0 from a given bit position. In (B) of Figure 2-8, note where the sides of the ladder must be punched to obtain a logical 1 from a given bit position. The asterisked arrows in Figure 2-8 are intended to show the direction in which the current in the conductor tends to wrap, or link with the U-core. In both (A) and (B) of Figure 2-8, note that the currents for an A word and B word logical 1 wrap the U-core in the same direction, thus giving the same polarity signal to the sense amp for a logical 1. The currents for a logical 0 in both A and B words bypass the cores. However, a very small current noise signal is generated in the sense line. The logical 0 signal is blocked at the sense amplifier.

#### 2.4.4 Module Physical Construction

A TROS module is the building block for every TROS array. The following description refers to numbered references on both Figures 2-9 and 2-10.

**Plastic Tapes (Figure 2-9):** The 128 plastic tapes (18, 19) are contained in a tape deck carrying a total of 256 TROS words. Holes are punched between the ladder network of the tape to accept the U cores (21) which pass through the tapes to mate with the I-cores (4). The I cores (4) are held in a core carrier assembly consisting of parts (3), (5), and (6).

TROS Tape Section - Showing Punching for Logical 1 & Logical 0 in A & B Words



(A) Punching shown for a logical 0 in these bit positions.

(B) Punching shown for a logical 1 in these bit positions.

Note: To program a logical 0 in an A word the central leg must be punched. To program a logical 0 in a B word the central leg must be punched.

Note: To program a logical 1 in an A word the outer leg must be punched. To program a logical 1 in a B word the inner leg must be punched.

\* The arrows indicate direction of current flow as the conductor tends to wrap around the core. It will be noted that for a logical 1 the current wraps in one direction, while for a logical 0 the current wraps in the other direction.

22351A

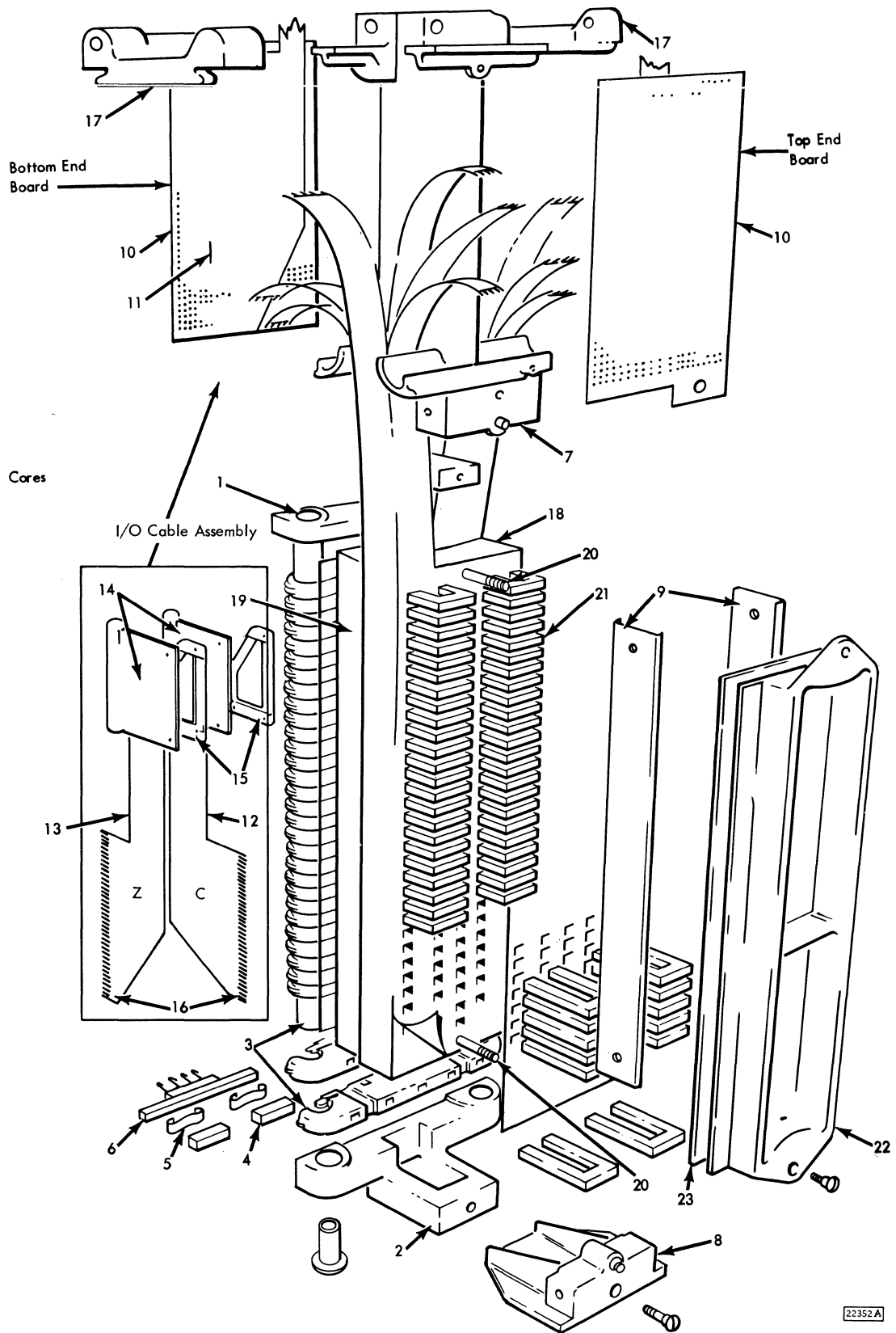
Figure 2-8. TROS Tape Section

Core Carrier Assembly (Figure 2-10): The core carrier assembly consists of a core carrier (1) into which the I-cores (2) are inserted. Springs (3) are placed behind the I-cores to ensure proper contact with the U-cores. The springs and the I-cores are held in position by clipping the strips (4) into the core carrier. The sense windings are wound round the core carrier, encircling the I pieces. The ends of the sense windings are connected to the pins on the

contact strip. On one end of the core carrier there is a boss (5) to enable correct visual orientation when placing the core carrier onto the support rods (1, Figure 2-9). If assembled incorrectly it would be impossible to connect the module to the TROS gate.

Module Assembly (Figure 2-9): The tapes are lifted on and off the module by the rails (9) and located by means of the aligning pins (20), screwed into the

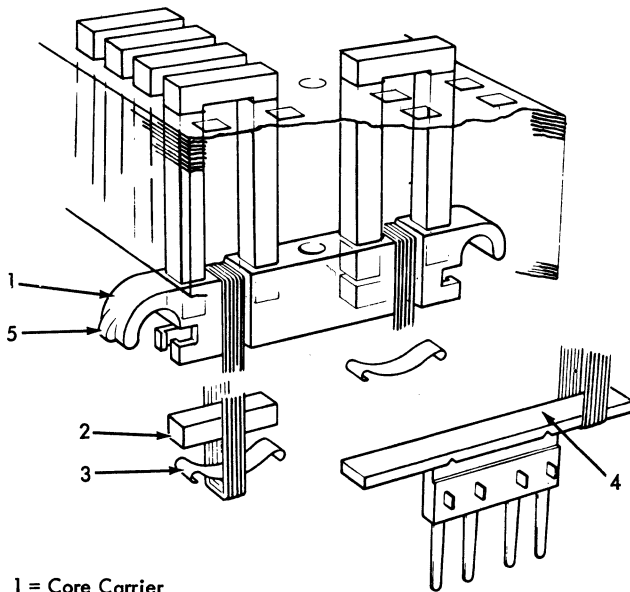
1. Rod
2. Block
3. Carrier
4. 1 Core
5. Spring
6. Strip
7. Chassis
8. Support
9. Rail
10. Diode Board
11. FDD Substrate
12. I/O Cables
13. I/O Cables
14. I/O Cable Card
15. Cable Clamp
16. Terminating Pins
17. Clamp
18. Tape Stack
19. Tape Stack
20. Alignment Pin
21. 2 Banks Of 24 U Cores
22. Retainer
23. Insulator



23352A

Figure 2-9. TROS Module





- 1 = Core Carrier
- 2 = I Core
- 3 = Compression Spring
- 4 = Contact Strip
- 5 = Locating Boss

22353

Figure 2-10. Core Carrier Assembly

support (8). The blocks (2) carry the two rods (1) for the core-carrier assemblies to clip onto. There are thirty carriers. The support (8) and chassis (7) screw into the blocks (2) and are spaced by the rails (9).

The U-cores (21) are held in the module by the retainer (22) and insulator (23). The retainer (22) screws into the support (8) and chassis (7), and forces the U-cores (21) against the I-cores.

**Connections to the Module:** Connected to the chassis are the module end boards (10) to carry the diodes (11) used for TROS word addressing and connections to the tapes in the tape deck. The diode board nearest the I-cores is defined as the bottom end board, and the diode board nearest the U-core retainer (22) as the top end board.

The connections to the TROS tape consist of pins placed in plated thru holes in the diode board on which the four tape terminal connections are pressed.

Input/output connections to the module end boards are made by the C and Z tapes and paddles (12), (13) and (14). The C and Z tapes have pins passing through plated holes in the diode boards (10) and soldered to printed circuitry on the diode boards. The C and Z tapes (12) (13) are clamped to the chassis (7) by the clamps (17) so as to relieve any strain in the connections to the diode boards (10).

**Laminar Bus (Figure 2-11):** When a number of modules have been assembled, the sense windings associated with each particular bit of a module are connected in parallel. In Figure 2-11 the sense windings for a particular bit in each of the 8 modules are shown connected in parallel with a 200 ohm terminating resistor. The terminating resistor is shown connected to the laminar bus. Each laminar bus consists of four conductors printed on a strip of non-conducting material. Each conductor has pins connected to it, coinciding with the pins on the core carrier. The pins of the core carrier are soldered to those of the laminar bus bars.

#### 2.4.5 TROS Tape Deck

- The TROS tape deck is numbered from top to bottom: 64-127, 63-0.
- Three types of tapes reduce inter-tape capacitance.
- A resistance tape isolates tape 127 from tape 63 and provides a resistance loop around each leg of each U-core to dampen resonance.

##### 2.4.5.1 Tape Numbering and Identification

The upper 64 tapes in the module are installed facing in the opposite direction from the lower 64 tapes (Figure 2-13). This creates more space for the connection of the tape ends to the module end boards. The bottom of the module is defined as the side nearer the I-cores. The tapes in the lower half of the tape deck are numbered 0 - 63 from the bottom up. The tapes in the upper half of the tape deck are numbered 64-127 from the top down.

On the end of the TROS tape there are two copper tabs which serve to identify the tape (Figure 2-14). The seven digit number represents the part number of the tape. The three high order positions of the part number will be 221 to identify the tape as belonging to the 2841. The fourth position of the part number represents the module where the tape is located.

The nine digit number is broken down as follows: the three high order digits represent the sequence number of the tape in the tape deck, the low order 6 digits represent the E/C level of the tape. Above the E/C level is a letter (A, B or C) to identify the type of tape for tape stagger purposes (Figure 2-12).

##### 2.4.5.2 Types of Tapes - A, B and C

To reduce the capacitance between the drive wires on adjacent tapes, three different types of tapes are

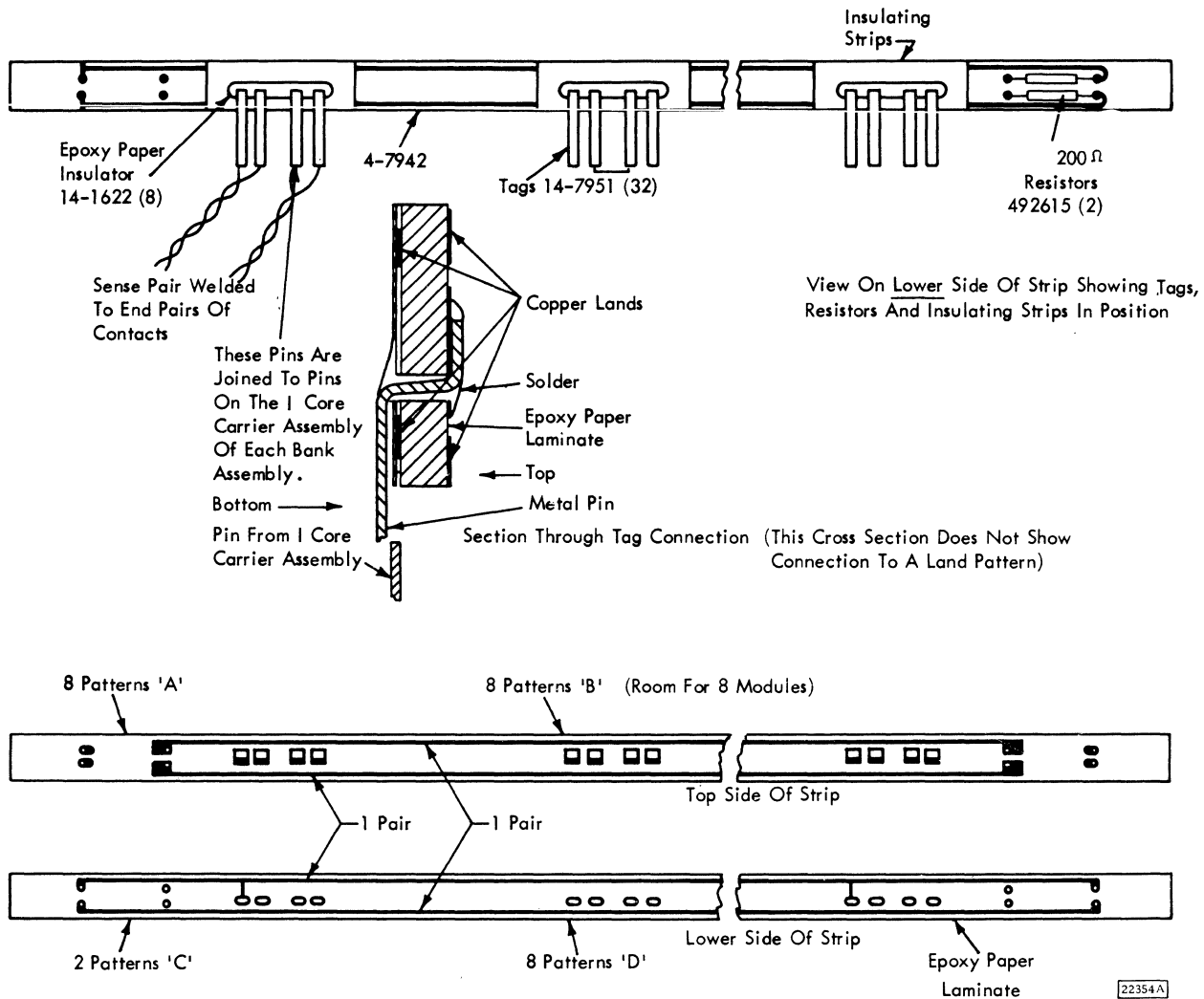


Figure 2-11. Laminar Bus

used. On each type, the conductor pattern is displaced from the U-core hole by a different amount. These three types are labelled A, B and C and are arranged sequentially throughout the deck of tapes.

2.4.5.3 Resistance Tape and Insulating Tape

To damp any resonance which might be caused by inter-tape capacity and flux leakage, a distributed loss is introduced. This is achieved by including in each module a plain plastic resistance tape (Figure 2-15) on which single turns of resistance foil are etched. These resistance loops are then covered with a plastic insulating tape. The single resistance loops encircle each leg of each U-core, and have an approximate resistance of 0.6 ohms.

The tapes in the tape deck are divided equally into sections, with end terminations passing on

either side of the chassis. Since all tapes are similar in their basic construction, the bottom set of tapes is completely reversed with respect to the top set. Therefore, to prevent the wiring on tape #63 and tape #127 from touching, the resistance tape is located between these two tapes.

2.4.6 Addressing TROS

- 12-bit address register is used to address TROS.
- Addressing of any of the 2,048 words of TROS is accomplished by the outputs of a 32 by 64 matrix; 32 gates and 64 drivers form the inputs to the matrix.

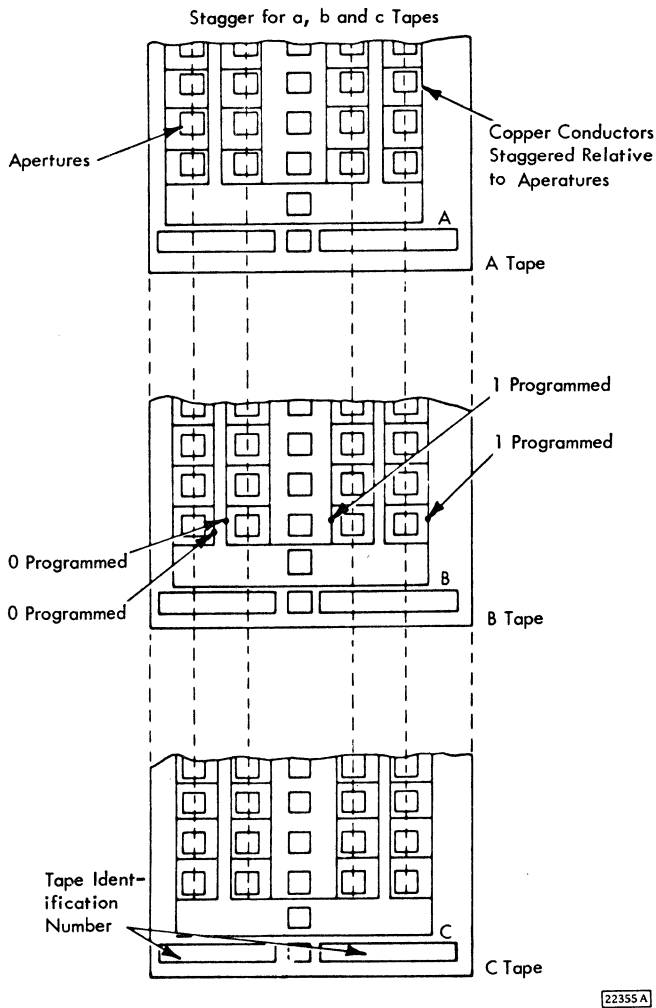


Figure 2-12. Tape Stagger

- Each of the eight TROS modules is addressed by a matrix made up of the 64 drivers and four of the 32 gates.
- One driver and one gate are required to address any of the 2,048 TROS words.

Addressing for the 256 word lines of a single module (Figure 2-16) is accomplished by a matrix made up of 64 drivers and four gates. The 64 drivers are common to all eight modules. Module 0 (Figure 2-16) is driven by 4 of the 32 gates (Gates 0 - 3). Module 1 is driven by gates 4 - 7, etc.

To address any word in TROS, a drive circuit is needed at one end of the drive line, and a gate circuit at the other end. For example (Figure 2-16), the drive line for word 5 is energized by turning on driver 1 and gate 0. The diodes on the driver side of the

drive line prevent back circuits through other drive lines and drivers.

**Module End Boards:** The 128 tapes in a module are terminated on two module end boards (Figure 2-17). The isolating diodes in the form of FDD (four double diode) substrate blocks are also mounted on the two module end boards. The commoning of lines on the module end boards follows:

**Drive Commoning:** Because 64 drivers are used for 256 word lines, four word lines from each module are commoned to one driver. The 4 word lines are the A and B lines on any particular tape together with A and B lines on the corresponding tape in the other (upper or lower) half of the module. For example, the A and B words on tape 95, together with the A and B words on tape 32 are common to driver 32 (Figure 2-17).

**Gate Commoning:** Each module has 256 word lines and 4 gates with 64 word lines commoned to each gate. In the upper half of the module, all the A lines are taken to one gate, all the B lines to another gate and similarly in the lower half of the module. The leads to the gates are numbered 0 - 31. Gates 0 - 3 are connected to module 0, gates 4-7 are connected to module 1 etc. For example, the B words of tapes 64 through 127 are commoned to gate 3 and the A words of tapes 64 through 127 are commoned to gate 2. In the lower deck all the A words are commoned to gate 0, all the B words to gate 1.

**Diode Substrate:** The diodes in series with the word lines of the driver are in FDD substrate blocks in the module end boards. Each board carries 16 substrate blocks, each containing eight diodes. Figure 2-18 shows the printed circuit on the ends of the boards, and the layout of the isolating diodes.

#### 2.4.7 Decoding the Address Register

- Bits 11-6 of the address register develop the gate address (Figure 2-19a).
- Bits 5-0 of the address register develop the driver address.
- The binary weight of the address register positions 10-6 gives the gate number.
- The binary weight of the address register positions 10, 9, 8 give the module number 0-7.
- The binary weight of the address register positions 7, 6 give the gate number (0, 1, 2, 3) on each module.

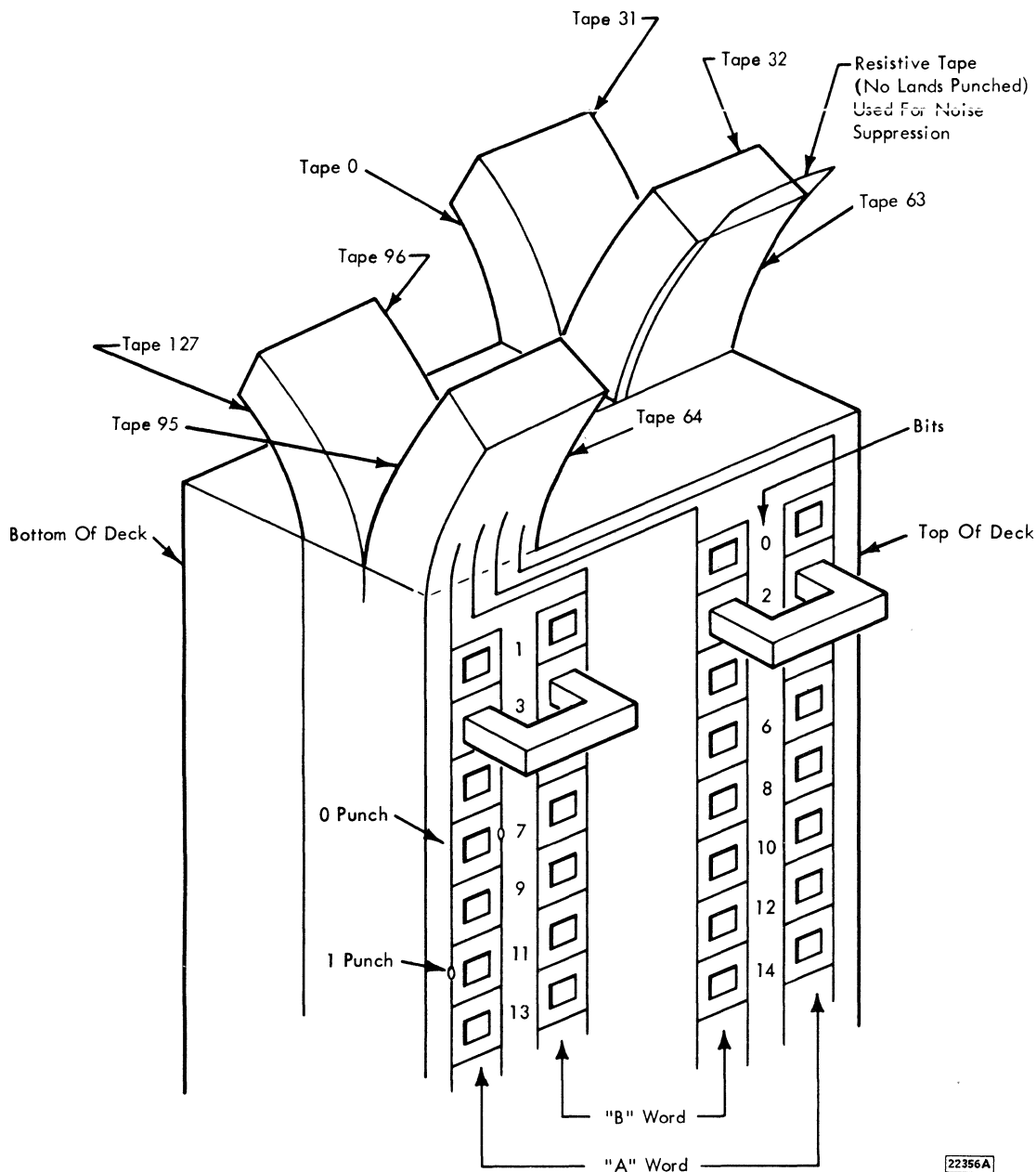


Figure 2-13. TROS Tape Deck

- The binary weight of the address register positions 5-0 gives the driver number.

**Gate Decoding:** The gate and module numbers can be determined by either of two methods. Once the gate and module numbers are known, the decoder circuit required to develop the module and gate can be found:

1. The binary weight of positions 10-6, gates only, (Figure 2-19b) gives the number of the gate.  
Example: 11001 = Gate 25. From Figure 2-19b,
2. The binary weight of positions 10, 9, 8 gives the module number. The binary weight of positions 7, 6 gives the gate number (0, 1, 2, 3) on each

gate 25 goes to module 6. Decoder outputs of 5 and 20 are required. The switching in the decoder required to give these outputs can now be determined. Note that the relation between gate 25 and decoder outputs 5 and 20 is not significant. Regard the decoder output line number as line labels only.

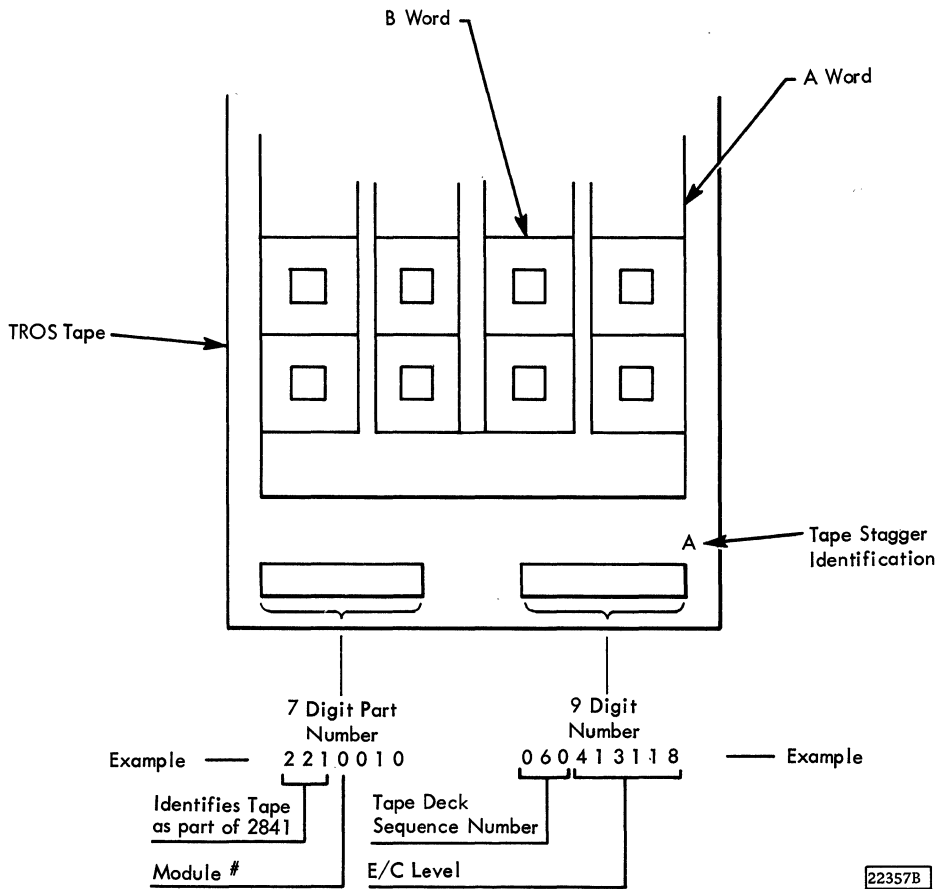


Figure 2-14. TROS Tape Identification

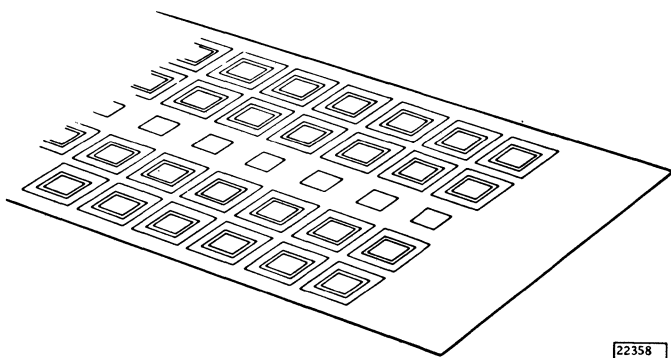


Figure 2-15. Resistance Tape

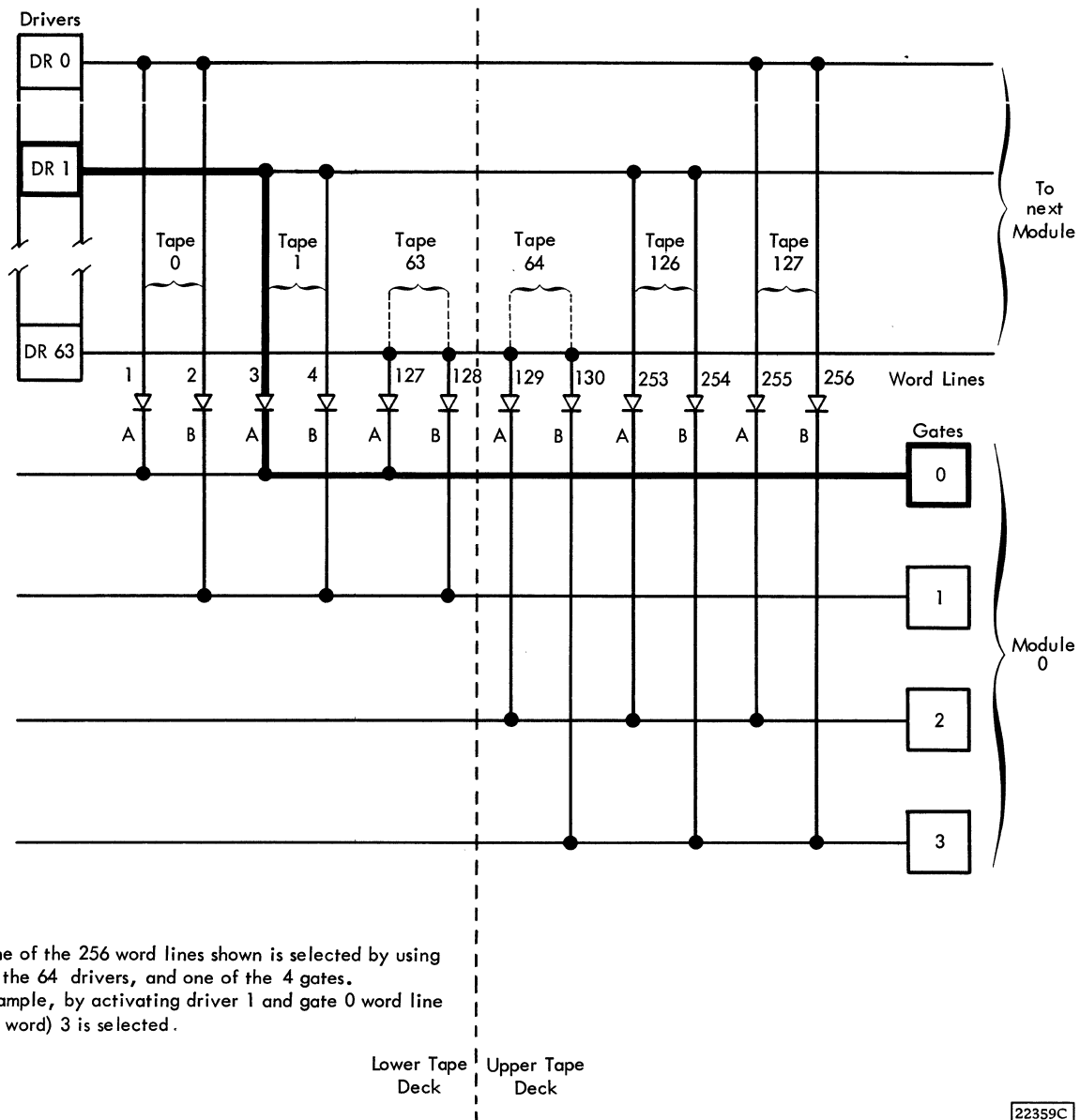
module (Figure 2-19a). For example, module 6 gate 0 is gate 24, module 6 gate 1 is gate 25, etc.

Once the module and gate are determined, the required switching can be found as noted in item 1.

**Driver Decoding:** The driver number and decoder switching can be determined by either of two methods.

1. The binary weight (address) of positions 5-0 gives the driver number (Figure 2-19c). A study of the matrix, once the driver is known, gives the required decoder output lines. For example, driver 16 requires decoder output lines 0 and 20. The example bit pattern of 010000 gives this decoder output.
2. Bits 2, 1, 0 can be decoded to give the decoder output low order octal digit. Bits 5, 4, 3 can be decoded to give the decoder high order octal digit. For example, in Figure 2-19c, the interaction of lines 0 and 20 in the matrix gives driver 16.

**Determining Tape Number:** After the driver is selected, the tape number can be determined by examining the bit in position 7 (X0). From Figure 2-17, gates 0 and 1 select tapes 0 to 63, and gates 2 and 3



**Note:**

Any one of the 256 word lines shown is selected by using one of the 64 drivers, and one of the 4 gates. For example, by activating driver 1 and gate 0 word line (TROS word) 3 is selected.

Figure 2-16. Principle of Driving and Gating

select tapes 64-127. If X0 is on, gate 2 or 3 is selected and the actual tape number is determined by subtracting the previously determined driver number from 127 (Figure 2-19a). If X0 is off, the driver number equals the tape number.

Determining A or B Word: A or B word on this tape is determined by examining the bit in position 6 (X1). From Figure 2-17, gates 1 and 3 are connected to B words. If X1 is on, gate 1 or 3 is developed and thus a B-word is addressed.

**2.4.8 TROS Functional Operation**

- TROS timing is developed from a 2841 clock pulse in a delay line.
- TROS cycle time is 500 ns.
- Voltage level at input to sense amplifier is restored so the sense amplifier can accept information to be read.
- The W and X address registers are decoded to select a gate and driver.

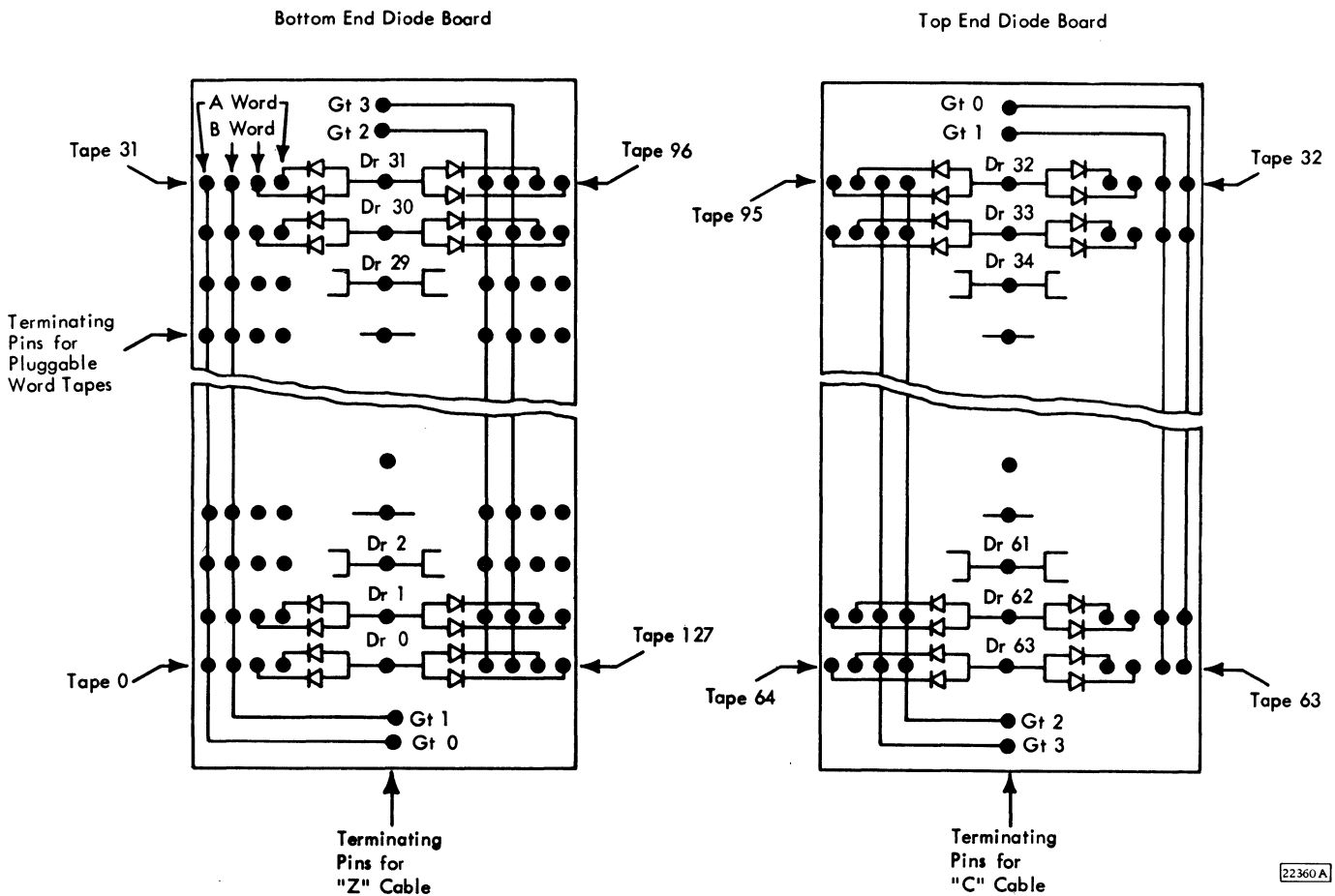


Figure 2-17. Diode Boards on Tape Modules

- The gate strobe switches on the selected gate.
- The driver is selected and when the driver strobe comes on, array current flows through the selected word line.
- The sense strobe samples the 48 sense line outputs to turn on the selected sense amplifier.
- Non-selected drivers are isolated by reverse biased diodes.

#### 2.4.8.1 TROS Timing

The timing for TROS is obtained by feeding a 2841 clock pulse to TROS every 500 ns (Figure 2-20), putting this clock pulse into a series of delay lines, and tapping the delay line at various points to obtain the required time pulses (Figure 2-21).

**NOTE:** These time pulses are interrelated and a failure at one point in the delay circuitry could alter the entire TROS timing. A procedure for checking the TROS timing is outlined in the IBM Field Engineering Maintenance Manual, 2481 Storage Control Unit.

The TROS cycles continually at a speed of 500 ns. Figure 2-21 shows the internal and external timing of TROS. The cycle starts when a 2841 clock pulse is fed into the delay line.

The sense amplifier is designed so that before a sense pulse appears at the input, the input of the threshold stage must be restored to a controlling level by applying a constant sense restore voltage for a time. The restore circuit is activated by the sense restore strobe.

While the sense amplifier threshold is being restored (Figure 2-21), the W and X address register is decoded to select a gate and driver as shown on Figure 2-20. When the gate strobe appears at the selected gate, the gate switches on.

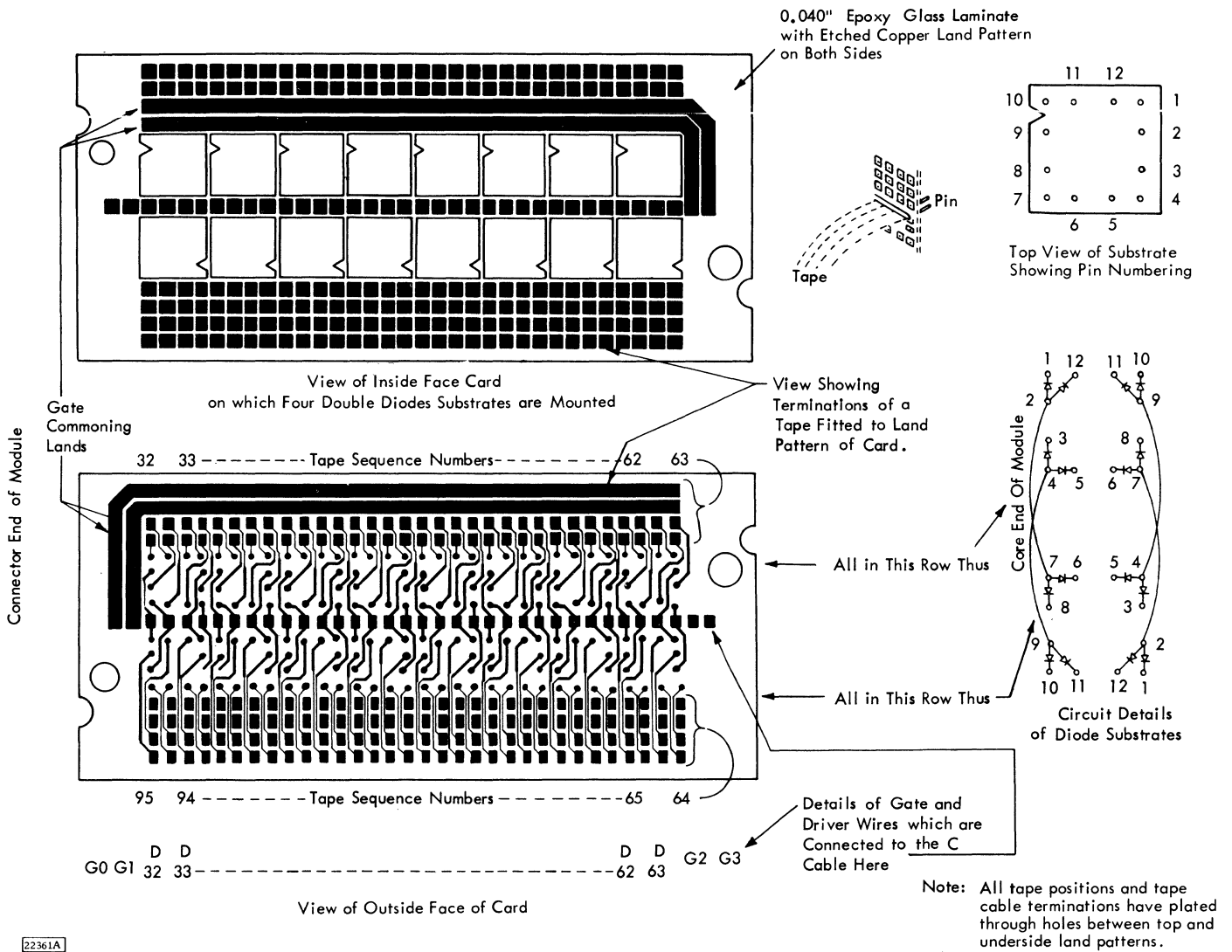


Figure 2-18. Module End Board Showing FDD Substrates

Until a driver is selected, no array current can flow. The selected gate has time to bring the 64 word lines connected to its output down to near ground potential, giving a quicker rise of the array current.

Simultaneously with the gate, the driver collector supply is turned on, the driver to be activated is selected, and after the driver strobe has activated the selected driver, the array current starts to flow.

The sense strobe appears at the input to the sense amplifiers about 100 ns after the start of the array current. In these 100 ns the noise of zeros being read dies away while the one's, which are much longer, are still present. The sense latches have been reset, and are now set with the new TROS word.

The driver collector supply is turned off, stopping the array current.

#### 2.4.8.2 Isolating Non-selected Drivers

The only forward biased diode at the driver collector supply output is the diode connected to the selected driver. The other seven diodes become reverse biased as soon as the array current starts to flow, isolating the other 56 not-selected drivers.

At this point, the function of the diodes in series with the word lines also becomes apparent; the 63 not-selected word lines connected to the driver have a not-selected gate at their other end. All these gate outputs are positive. When the current starts to flow through the selected word line, the voltage at the driver output drops to 1 to 2 volts, reverse biasing



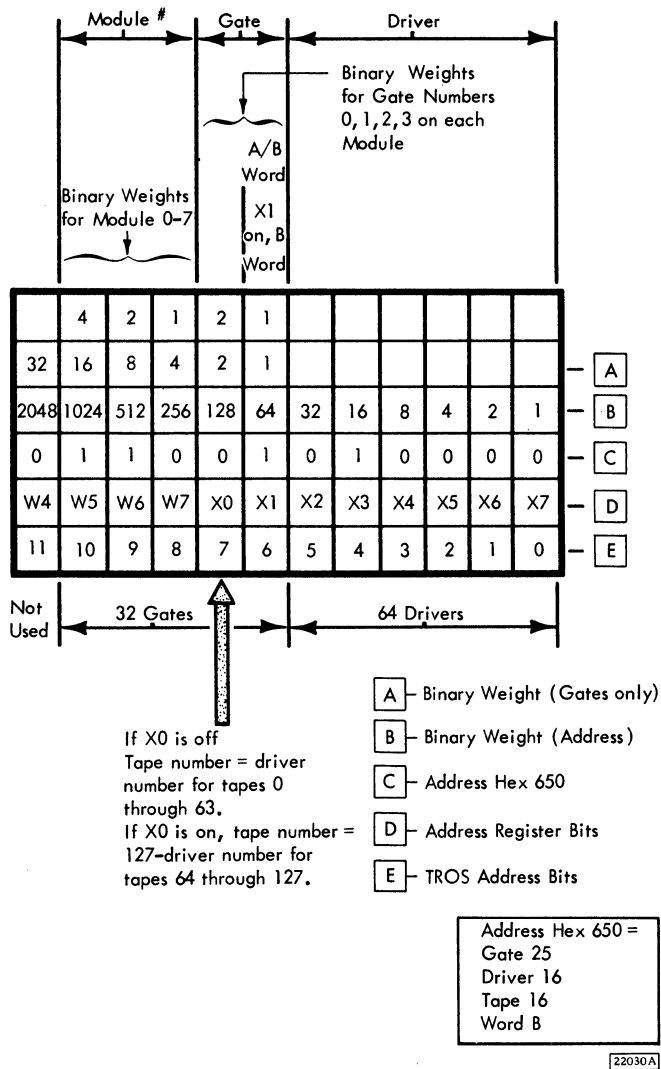


Figure 2-19a. TROS Address Decode

the 63 diodes of the not-selected word lines, which are at 3 to 4.5 volts. In this way, the load capacitance formed by the 63 not-selected word lines is isolated from the driver output, resulting in a faster rise of the array current.

#### 2.4.8.3 TROS Inhibit

TROS inhibit prevents the setting and resetting of the sense latches by inhibiting the generation of the sense reset and sense strobe pulses. The last word set into the sense latches before the rise of inhibit remains unchanged until the fall of inhibit.

#### 2.4.9 Array Layout

- TROS-1-4K logic carried on two large boards.
- TROS-2-2K logic carried on one large board.

- TROS-2-4K logic carried on two large boards.
- TROS-1 logic carried to TROS array(s) via two module connection (commoning) board.
- TROS-2 logic carried to TROS array(s) via one module connection (commoning) board.

The general layout of the TROS, as used in the 2841 stage 2 is shown on Figure 2-22. The entire TROS array is considered as C-gate in the 2841; however, the card locations in the automated logic diagrams (ALD's) do not reflect this C-gate notation. The decoders, drivers, timing cards, sense amplifiers and sense latches are on the large board(s) to the left of the TROS array. These boards are designated A1 and A2, and are considered the A-gate of the TROS.

The connection between the TROS modules and the large circuit boards (A1 and A2) is via the module connection or commoning board(s). These commoning boards are considered the B-gate of the TROS and will carry this notation in the ALD's. All necessary module interconnection wiring for drivers and gates is done on this board. The C and Z paddle connectors from the TROS module are plugged into the module connection boards that carry the gate circuit cards, and the gate strobe card. There is one gate circuit card for each module, and one gate strobe card for every eight modules.

#### 2.4.10 TROS Output Word

- Output word (48 bits long) split into 15 separate control fields.
- Each control field controls a separate part of the 2841 hardware.

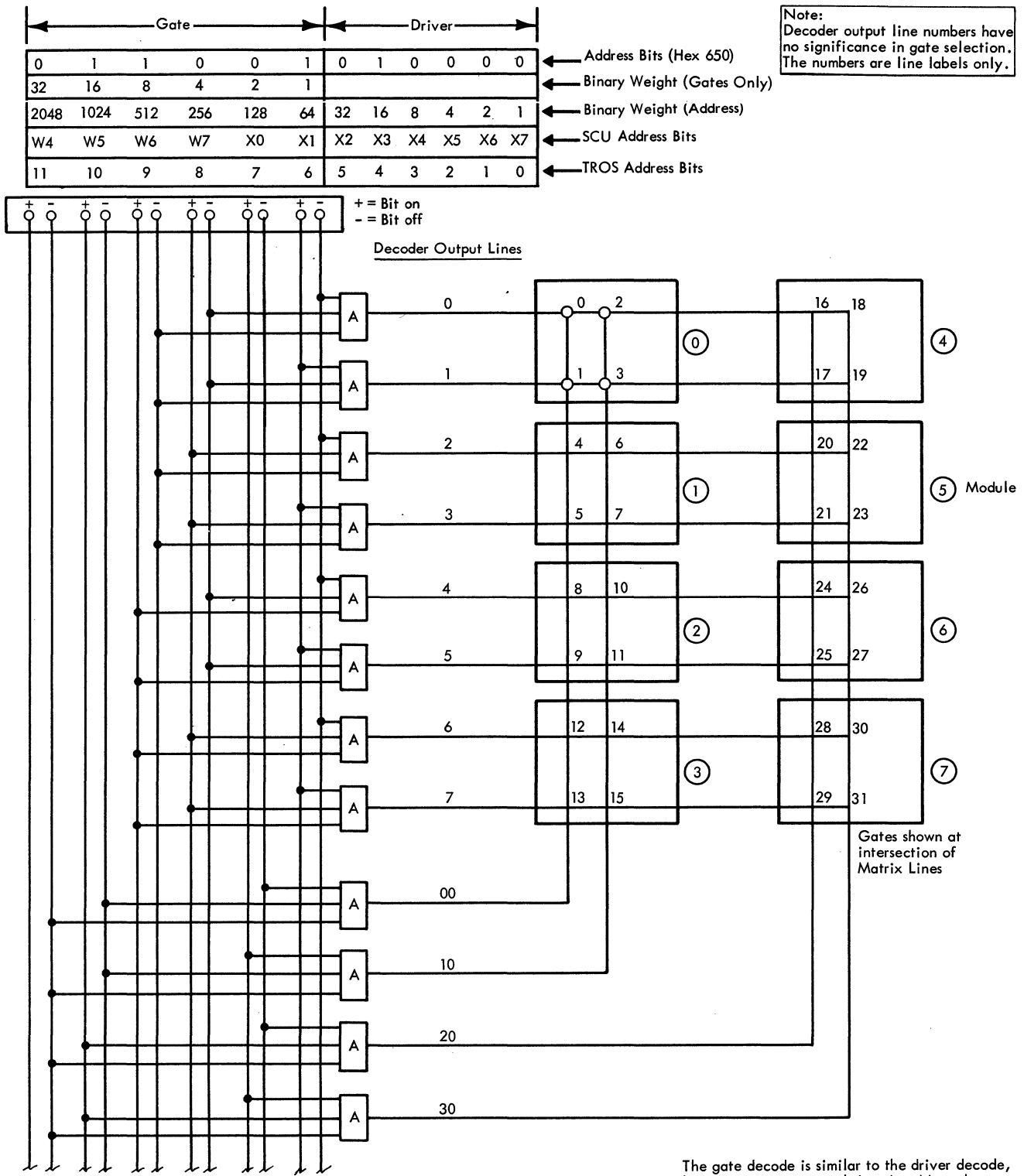
The 48 bit word is split into 15 control fields as follows (Figure 2-3):

Field CN - output bits 0, 2, 4, 6, 8, 10 - used to provide bits 0 - 5 of the X register for the next word to be addressed in the microprogram.

Field PN - output bit 12 - used to maintain odd parity in the CN field.

Field CD - output bits 14, 16, 18, 20, 22 - used to control the destination of the information on the D bus.

Field CV - output bit 24 - used to gate the B bus in true or complement form to the A or B entry exclusive OR's.



The gate decode is similar to the driver decode, but it is not a true octal decode, because the combination of bits used is different. Thus, two decoder outputs do not combine to give the gate in octal. However, by weighting the six binary bits as shown, the selected lines do give the indicated gate.

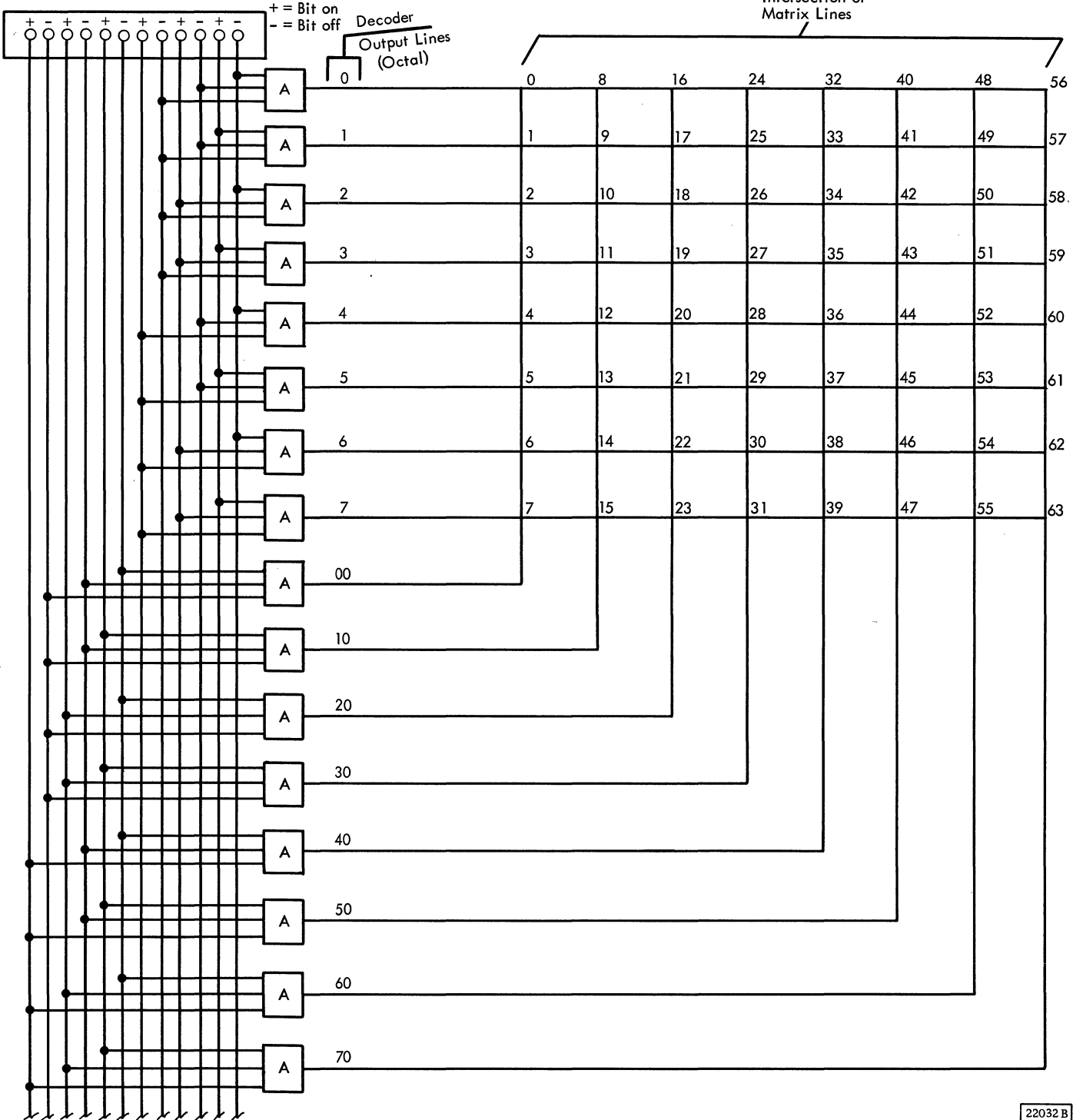
22031B

Figure 2-19b. Gate Decode

5		0				
0	1	0	0	0	0	
2			0			
32	16	8	4	2	1	
X2	X3	X4	X5	X6	X7	
5	4	3	2	1	0	

← Hex Address-650  
 ← Address Bits  
 ← Octal Value-20  
 ← Binary Weight  
 ← SCU Address Bits  
 ← TROS Address Bits

**Note:**  
 An octal decode scheme is used. Bits 0, 1, 2 are decoded into the low order octal digit. Bits 3, 4, 5 are decoded into the high order octal digit. The combination of two decoder outputs gives the driver in octal.



22032 B

Figure 2-19c. Driver Decode

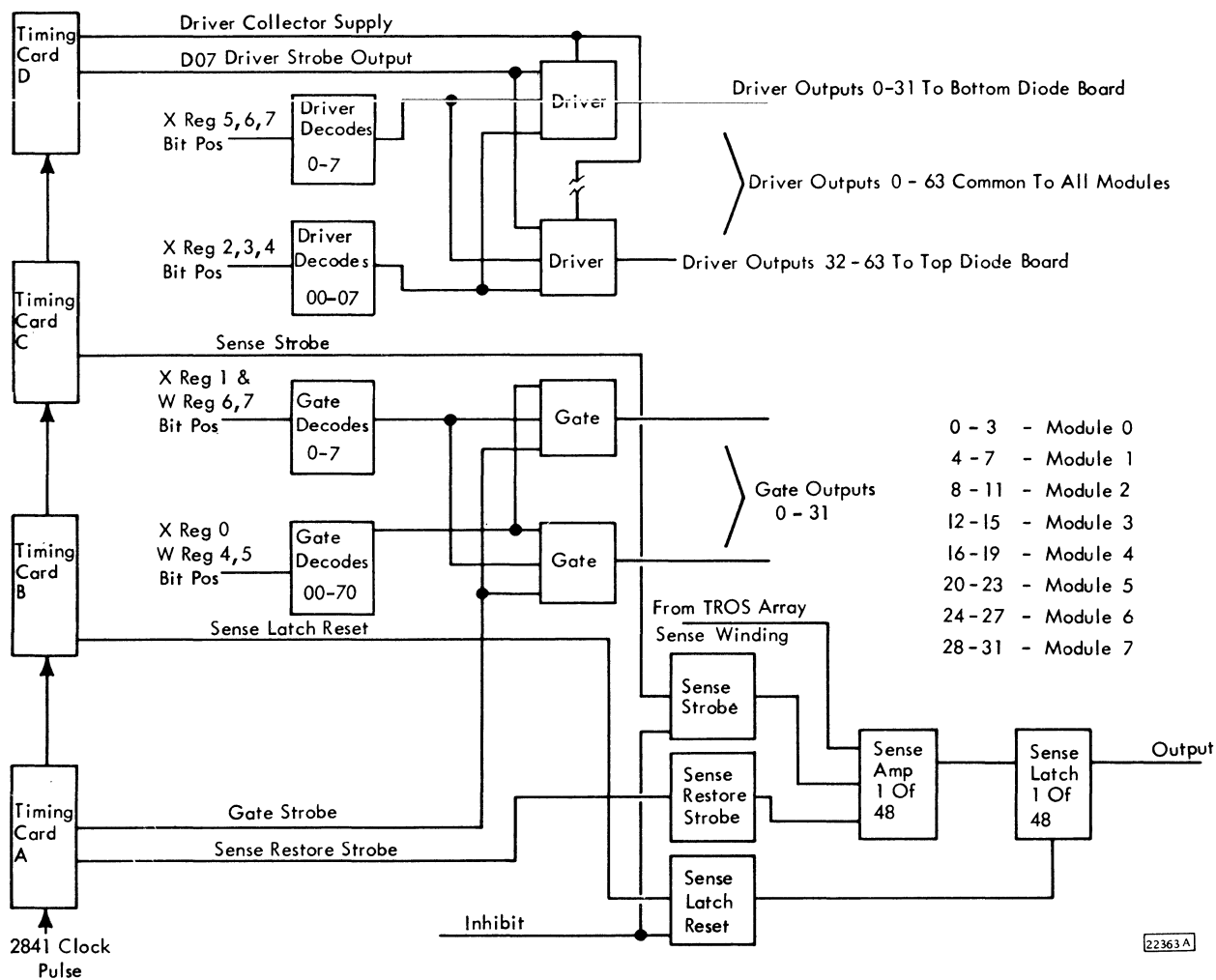


Figure 2-20. TROS Logic Layout

**Field CC** - output bits 26, 28, 30 - used to control carry functions and logical operation of ALU.

**Field CS** - output bits 32, 34, 36, 38 - used to control set and reset of the ST register.

**Field PC** - output bit 40 - used to maintain overall odd parity of the following fields CC, CD, CD ALT., CS, CV, BP, and PC fields.

**Field PS** - output bit 42 - used to maintain overall odd parity of the following fields, CA, CA ALT., CB, CK, CH, CL and PA fields.

**Field BP** - output bit 46 - when active (1-bit) the A register is presented directly to the D bus. The A register is also presented directly to the ALU for parity checking. If the output of the ALU parity bit

and the D register parity bit do not match, an ALU check is indicated.

**Field CH** - output bits 1, 3, 5, 7 - used to control the X register bit position 6 for branching purposes.

**Field CL** - output bits 9, 11, 13, 15 - used to control the X register bit position 7 for branching purposes.

**Field CA** - output bits 17, 19, 21, 23, 25 - used to control the A register data source.

**Field CB** - output bits 27, 29 - used to control the B register data source.

**Field CK** - output bits 31, 33, 35, 37, 39, 41, 43, 45, - used to provide a constant to the B bus or W register.

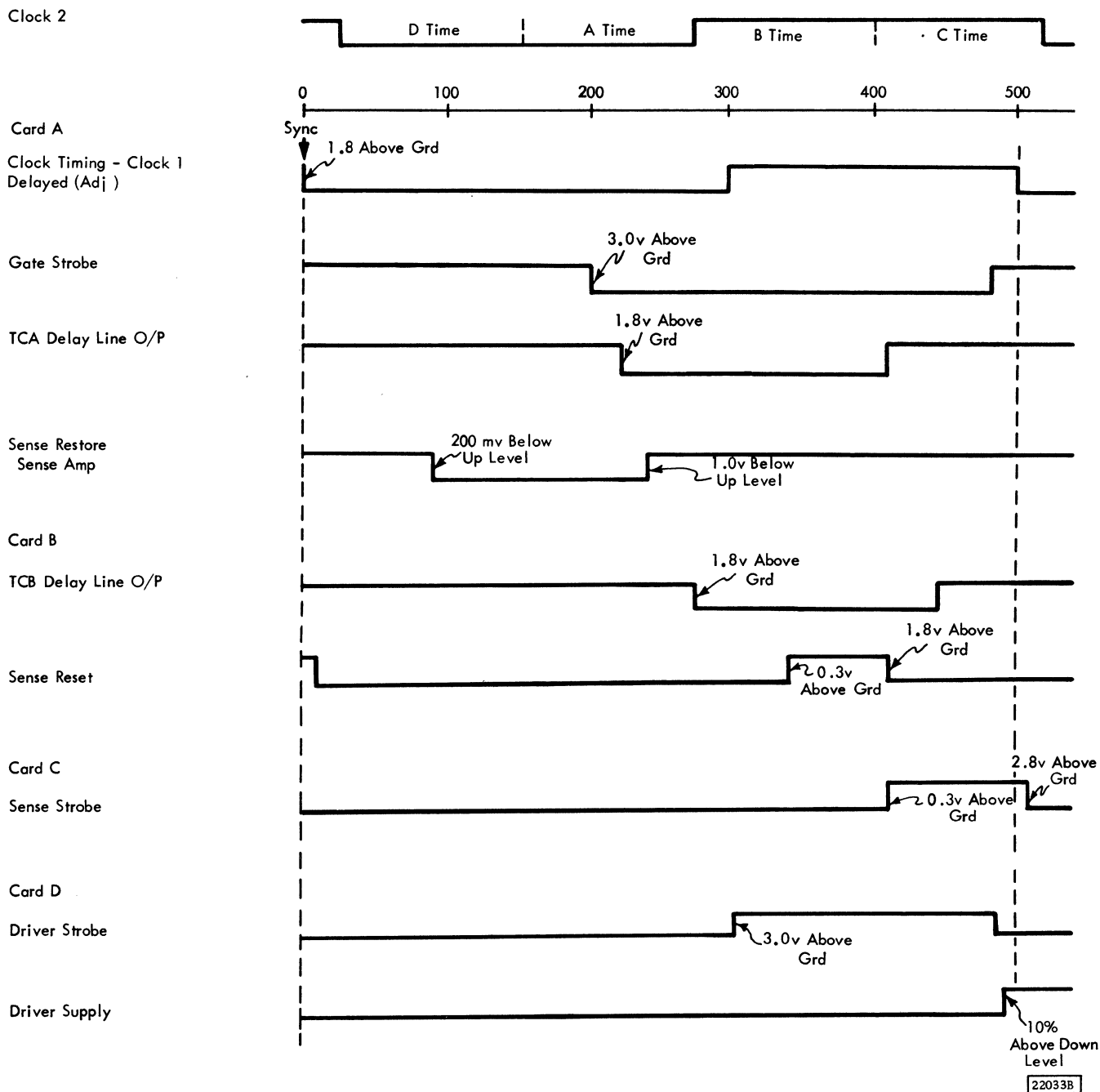


Figure 2-21. TROS Timing

**Field PA** - output bit 47 - used to check W and X register parity.

**Bit 44** - Not used.

#### 2.4.11 Control Latches

The following fields of the TROS word have control latches, set from the sense latches at Clock 1 time and reset at A time.

CD, CS, CN5

The purpose of the control latch is to have the control field output available for a whole cycle (500 nanoseconds) as the sense latch output is available from D to approximately C time.

#### 2.4.12 TROS Address Check

- Detects internal addressing failure.

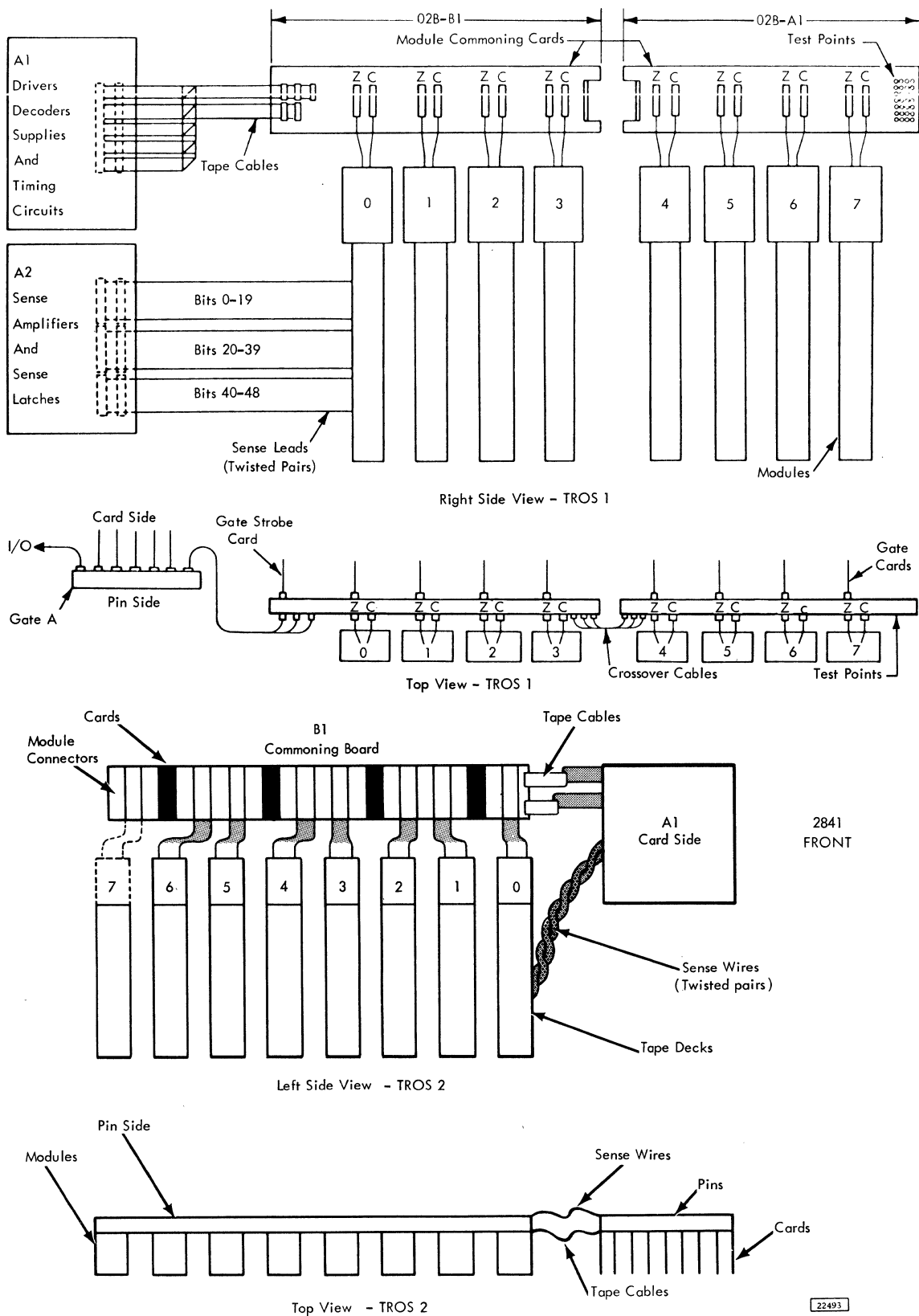


Figure 2-22. General Arrangement of TROS Hardware

- Causes an address check.
- 2841 stops with the control word information of the word in which the error occurred.
- 2841 stops with the SALS latches set with the data of the word addressed that was in error.

The W and X register parity bits are exclusive-ORed and the results set into a polarity hold latch at clock 2 time of every cycle. The output of the polarity hold latch is analyzed along with the PA bit and/or the CN field parity at A time of every cycle (SAL's will be good). If an address check condition is present, the address error latch is set and the 2841 comes to a hard stop.

Turning on the address error latch brings up three inhibit lines which have the following functions:

1. Inhibit 1 - comes up with address error and prevents the reset and setting of the SALS, the SAL's therefore contain the information from the word which was in error.
2. Inhibit 2 - comes up with inhibit 1 and clock 3 to block CA, CB and CD latch set and the W and X register set. Since the W and X registers are set at clock 4 time, it is too late to keep the address of the word that actually failed. Therefore, the W and X registers contain the address of the next word in the microprogram and under an address error condition they cannot be relied upon to be correct.
3. Inhibit 3 - comes up with Inhibit 2 and Clock 1 to block further ALU output.

#### 2.4.13 TROS Sense Amplifier Check

- Detects failure of SALS in certain fields of the TROS word.
- Even bit count causes a Sense Amp Error.

The CA, CA ALT., CB, CK, CL, CH, PS, and PA fields are checked for a total odd bit count at A time of every cycle. The PS bit is punched in the TROS tape to make the total bit count odd. A total even bit count causes the sense amp error latch to turn on at an A-time and the 2841 to come to a hard stop. Once the sense amp error latch is set, the sequence of bringing up the inhibit lines is the same as described for TROS address check. The sense amp error is indicated on the CE console, along with the address of the next word in the microprogram. The information in the SALS is that of the word in which the error occurred.

#### 2.4.14 TROS Control Register Check

- Detects failure of the SALS in those fields of the TROS word which feed the control register latches.
- Even bit count causes a control register check.

The CC, CD, CD ALT., CV, CS, PC, BP fields are checked for a total odd bit count at A time of every cycle. The PC bit is punched in the TROS tape to make the total bit count odd. A total even bit count causes the control register error latch to turn on at A time and the 2841 to come to a hard stop. Once the control register error latch is set, the sequence for bringing up the inhibit lines is the same as the sequence described for TROS address check. The control register error is indicated on the CE console, along with the address of the next word in the microprogram. The information in the SALS is that of the word in which the error occurred.

#### 2.5 ARITHMETIC/LOGICAL UNIT (ALU)

- ALU has inputs from the A and B entry assemblers and carry control.
- The B entry may be in true or ones complement form. This is controlled by the CV field decode.
- ALU can:
  - Add, subtract (add with one's complement input from B entry), AND, OR, and exclusive OR.
- The type of ALU function is controlled by the CC field decode.
- The output of ALU is placed on the D bus. It may be directed to any of the general purpose registers under microprogram control.
- ALU output may be tested for zero by the microprogram.
- ALU output of not zero may be used to turn on status register, bit 2.
- A carry out of the high order position may be used to turn on status register, bit 3.
- ALU generates correct odd parity any time it performs an operation.

- ALU may be bypassed by the bypass micro-program statement.

### 2.5.1 ALU General Description

The arithmetic/logic unit (ALU) is used to perform add, subtract, AND, OR, and exclusive OR operations within the 2841. It also assigns parity (odd) to data passing through it (Figure 2-23).

Inputs to ALU are from the A and B entry assemblers and the carry in latch. The input from the B Entry may be in true or one's complement form. This is determined by the CV 0 bit of the ROS word. The type of operation performed by the ALU is determined by the CC field decode section of the ROS word. There are eight different ALU (CC decode) operations (Figure 2-23).

Data from one of the B entry sources enters the true or complement exclusive ORs with the YCV 0 bit. When the YCV 0 bit is present the B entry is complemented. The output of the true-or-complement exclusive ORs, with the data from one of the A entry sources, enters the A-or-B-entry exclusive ORs. The output of the A or B entry exclusive ORs turn on or off the partial-sum-register latches to give the sum without carries.

The A and partial-sum register outputs enter the ALU with the control lines, from the YCC decodes, and the output of the carry-in latch where they are ANDed together to give the sum bits and carries to the next higher order bit during arithmetic operations.

The sum lines are gated to the D bus and the output sampled at clock 3 time after all carries have been propagated.

The output of ALU can be gated to the D bus. Two latches, D-equal-zero and carry-out, monitor the results of the ALU operations and may be tested by the microprogram.

The A register can be transferred to the D bus directly, thereby bypassing ALU. This operation is effected by placing bit 46 (bypass) of the ROS word On. When bypassing ALU, the ALU still receives the A and B inputs. The ALU computes parity for the byte. If the A register parity does not agree with the ALU computed parity (parity bits only are compared) the ALU check latch turns on, stopping TROS and lighting the data check lamp. The A to D transfer is negated if bus out parity occurred on the byte. In this case the byte goes through the ALU to the D bus. The ALU corrects the parity. The microprogram remembers that bus out parity occurred by means of the ER register, bit 2 latch.

Five symbols are used to represent the five arithmetic operations of ALU:

- + True Add/Positive
- Complement Add/Subtract
- AND - Logical
- Ω OR
- ⊕ Exclusive OR

### 2.5.2 Summary of ALU Statements

The following statements assume no bypass statement. Refer to CLD pages QA004 or Figure 2-39 for field layout.

CC Decode of 000: A CC decode of zero causes the ALU to add/subtract the A and B entry inputs with a carry in of zero from the carry in latch. The CC decode of 000 does not set the carry out in status register 3. This operation is represented symbolically as follows:

$A \pm B + 0 \rightarrow D$  Note: Carry in of zero does not always appear in ALU statement

For example:

$$DR = 163_{(10)}, KL = 29_{(10)}$$

ALU statement  $KL + DR \rightarrow GL$

A input (KL)	00011101	-	29	
B input (DR)	10100011	-	163	<sup>(10)</sup>
D bus output (GL)	11000000	-	192	<sup>(10)</sup>

CC decode of 001: A CC decode of one causes ALU to add/subtract the A and B entry inputs with a carry in of one from the carry in latch. The CC decode of 001 does not set status register 3. This operation is represented symbolically as follows:

$A \pm B + 1 \rightarrow D$

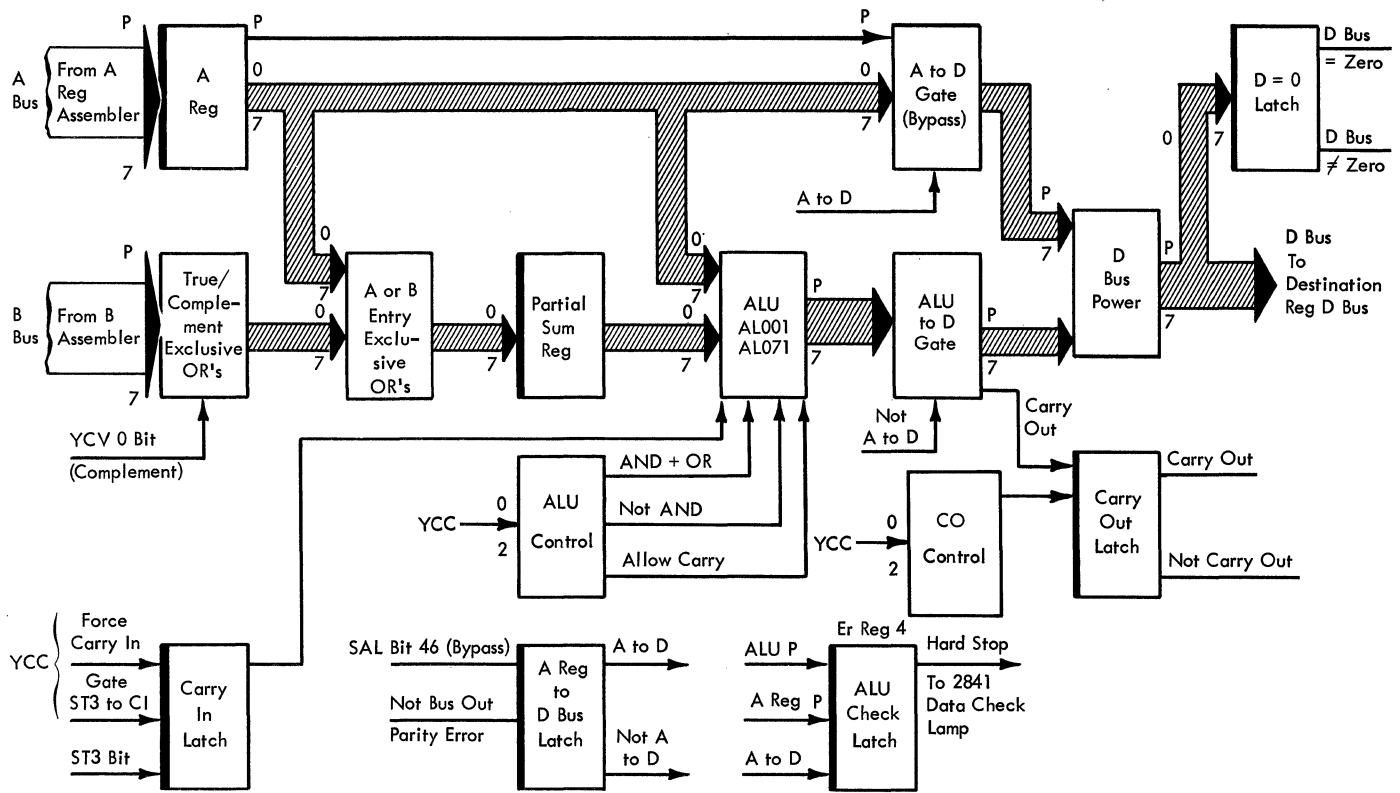
For example:

$$BY = 143_{(10)}, DH = 7_{(10)}$$

ALU statement  $DH + BY + 1 \rightarrow BX$

A input (DH)	10001111		143	
B input (BY)	00000111		7	<sup>(10)</sup>
Carry in			1	<sup>(10)</sup>
D bus output (BX)	10010111		151	<sup>(10)</sup>





CV Field 1 Bits	
Bit 0	
0	True B Entry Input
1	Complement B Input

Operation	ALU Control Lines		
	AND + OR	NOT AND	ALLOW CARRY
Add or Subtract	Off	On	On
Exclusive OR	Off	On	Off
And	On	Off	Off
OR	On	On	Off

C C FIELD 3 BITS			
Bit 0	Bit 1	Bit 2	
0	0	0	Add Operation - No Forced Carry In - No Carry Out to St 3
0	0	1	Add Operation - Force Carry In - No Carry Out to St 3
0	1	0	And Operation
0	1	1	OR Operation
1	0	0	Add Operation - No Forced Carry In - Latch Carry Out to St 3
1	0	1	Add Operation - Force Carry In - Latch Carry Out to St 3
1	1	0	Add Operation - Add in St 3 - Latch Carry Out to St 3
1	1	1	Exclusive OR

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Figure 2-23. ALU Block Diagram And Control

CC Decode of 010: A CC decode of two causes ALU to AND the A and B entry inputs. This operation is represented symbolically as follows:

$A \cdot B \rightarrow D$  Note: The B entry may be gated in complement form. In this case the statement symbolically would be:

$$A \cdot \bar{B} \rightarrow D$$

For example:

$$KL = 181_{(10)}, DR = 56_{(10)}$$

ALU statement  $KL \cdot DR \rightarrow GL$

A input (KL)	10110101	181	
B input (DR)	00111000	56	(10)
D bus output (GL)		00110000	48
			(10)

CC Decode of 011: A CC decode of three causes ALU to OR the A and B entry inputs. This operation is represented symbolically as follows:

$$A \cup B \rightarrow D$$

NOTE: The B entry may be gated in complement form. In this case the statement symbolically would be:

$$A \cup \bar{B} \rightarrow D$$

For example:

$$BY = 29_{(10)}, GP = 207_{(10)}$$

ALU statement  $GP \cup BY \rightarrow KL$

A input GP	11001111	207	
B input (BY)	00011101	29	(10)
D bus output (KL)		11011111	223
			(10)

CC Decode of 100: A CC decode of four causes ALU to add/subtract the A and B entry inputs with a carry in of zero from the carry in latch. The carry out from the high order position of ALU is stored in status register 3. This operation is represented symbolically as follows:

$$A \pm B + 0 \rightarrow DC$$

NOTE: The carry in of zero may not be shown. The C on the right side of the equal sign means store the carry out in status register, bit 3. This can be used on non arithmetic operations to reset ST 3.

For example:

$$\#1: DR = 19_{(10)}, BX = 128_{(10)}$$

ALU statement  $BX + DR \rightarrow GLC$

A input (BX)	10000000	128	
B input (DR)	00010011	19	(10)
D bus output (GL)		10010011	147
			(10)

(No carry out.  
Reset ST 3.)

$$\#2: DR = 93_{(10)}, BX = 204_{(10)}$$

ALU statement  $BX + DR \rightarrow GLC$

A input (BX)	11001100	204	
B input (DR)	01011101	93	(10)
D bus output (GL)		C←00101001	41
			(10)

(Carry Out of  
one. Set ST 3.)

CC Decode of 101: A CC decode of five causes ALU to add/subtract the A and B entry inputs with a carry in of one from the carry in latch. The carry out from the high order position of ALU is stored in status register 3. This operation is represented symbolically as follows:

$$A \pm B + 1 \rightarrow DC$$

For example:

$$BY = 223_{(10)}, OP = 32_{(10)}$$

ALU statement  $OP + BY + 1 \rightarrow BYC$

A input (OP)	00100000	32	
B input (BY)	11011111	223	(10)
Carry in (1)		1	1
D bus output (BY)		C←00000000	0

(Carry out of one.  
Set ST 3.)

CC Decode of 110: A CC decode of six causes ALU to add/subtract the A and B entry inputs with a carry in equal to the present condition of status register 3. The carry out from the high order position of ALU is stored in status register 3. This operation is represented symbolically as follows:

$$A \pm B + C \rightarrow DC$$

NOTE: A C in the carry in position of the ALU statement means to use the present condition of ST3 as the carry in to the low order position of the ALU.

For example:

$$DR = 28_{(10)}, KL = 36_{(10)}, ST\ 3 = 1$$

ALU statement  $KL + DR + C \rightarrow GPC$

A input (KL)	00100100	36
B input (DR)	00011100	28 <sup>(10)</sup>
Carry in (ST 3)	1	1 <sup>(10)</sup>
D bus output (GP)	01000001	65 <sup>(10)</sup>

(No carry out.  
ST 3 reset at  
end of operation.)

CC Decode of 111: A CC decode of seven causes the ALU to exclusive OR the A and B entry inputs. This operation is represented symbolically as follows:

$$A \nabla B \rightarrow D$$

NOTE: The B entry may be gated in complement form. In this case the symbolic statement is:

$$A \nabla -B \rightarrow D$$

For example:

$$BY = 53_{(10)}, GL = 150_{(10)}$$

ALU statement  $GL \nabla BY \rightarrow KL$

A input (GL)	10010110	150
B input (BY)	00110101	53 <sup>(10)</sup>
D bus output (KL)	10100011	163 <sup>(10)</sup>

Subtract Functions: The five different add/subtract functions can be made into subtract functions by transferring the complement of the B entry to the

ALU. This is accomplished by making the CV field decode equal to one.

For example:

$$GL = 38_{(10)}, BY = 24_{(10)}$$

ALU statement  $GL - BY \rightarrow KL$

A input (GL)	00100110	
B input (BY)	00011000 complement	11100111
D bus output (KL)	C ← 00001101	13 <sup>(10)</sup>

The answer is 13<sup>(10)</sup> and is off by one because one's complement subtraction is used. The carry out sets the carry out latch in the ALU. The carry out latch can be tested by the microprogram. The result in true form can be obtained by either adding one to the KL register, or by executing the ALU statement:

$GL - BY + 1 \rightarrow KL$

A input (GL)	00100110	
B input (BY)	00011000 complement	11100111
Carry in (1)	1	1
D bus output (KL)	C ← 00001110	14 <sup>(10)</sup>

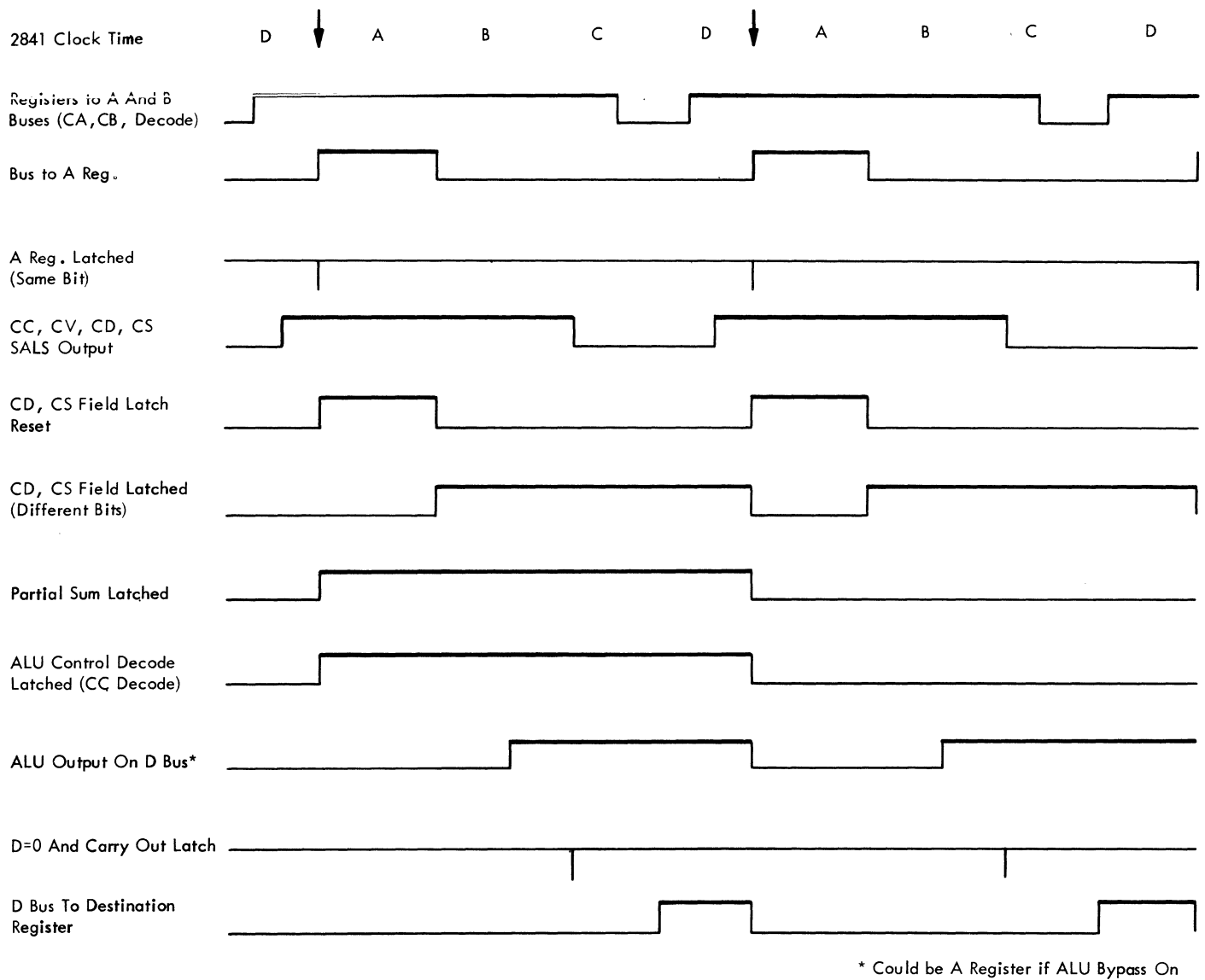
NOTE: Twos complement subtraction.

### 2.5.3 Functional Description and Basic Timing

Functionally the operation of the ALU (Figures 2-23 and 2-24) can be thought of as beginning in D time of the previous machine cycle (a machine cycle is A, B, C, and D time). During this time, CA and CB fields of ROS are decoded. They control the gating of information to the A and B buses.

#### A Time

1. A and B buses gated to ALU. The A register is latched up.
2. The CC, CV, and CD field decodes are reset and set. The set overrides the reset.
3. The A and B entries and CV decode turn on or off the partial-sum-register latches.
4. The applicable ALU control latches AND ± OR, Not AND, Allow Carry are set or reset and the ALU begins performing the function called for.



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Figure 2-24. ALU Basic Timing

### B Time

1. The CC, CV, CD reset is removed. These latches remain latched through D time.
2. ALU finishes the operation. The answer is now on the D bus.

### C Time

1. The D bus is sampled for zero. If it is zero, the D = 0 latch is set.
2. Carry out from the high order position of ALU is sampled. If there is a carry out, the carry out latch is set.

3. CA and CB decodes are reset.

### D Time

1. The register (if any) designated by the CD field is loaded with the output of ALU.
2. Status register 3 is set or reset if the operation was one which stored the carry out in ST 3 ( $\rightarrow$ DC).
3. Status register 2 is set now if the ROS word contained a DNST21 statement and the D bus did not equal zero.
4. The next ROS word is now available for field decoding.

## ALU Bypass

If the microprogram is using ALU Bypass, the ALU statement will appear as follows:

### A → D BYPASS

The word BYPASS appearing in the ALU statement means that bit 46 of the ROS word is a one. All ALU times remain the same with the exception that the A register is gated to the D bus.

If the ALU computed parity does not agree with A register parity, the ALU check latch is turned on, stopping the 2841 TROS unit.

Bypass statements appear only in blocks that do not have a B bus entry statement.

## 2.6 SERIALIZER/DESERIALIZER UNIT

- Changes parallel-by-byte data to serial-by-bit data when writing on the storage devices.
- Changes serial-by-bit data to parallel-by-byte data when reading from the storage devices.
- Generates clock pulses used in NRZI double frequency writing.
- Separates data from clock pulses when reading.
- Checks byte parity when writing.
- Finds address marks under control of the microprogram.

### 2.6.1 SERDES General Description

The serializer deserializer unit (SERDES) is used for the writing and reading of data on the storage devices.

SERDES is controlled externally by the microprogram with three lines (Figures 2-3 and 2-4).

1. Read gate.
2. Write gate.
3. Address-mark-search line.

The turning on of read-gate allows the data from the selected device to enter the SERDES unit. The SERDES unit synchronizes with the data by use of the VFO circuit. The serial data is placed into the file-data-register in the SERDES unit. When a full byte of data is in the file-data-register, the microprogram is notified by the setting of status register bit 4.

Read-gate and address-mark-search lines cause the SERDES to search for an address-mark in the data coming from the selected device. An address mark consists of two bytes of data with some missing clock bits and a byte called the sync byte. When SERDES has located the address-mark and read the sync byte, the microprogram is notified by the setting of status register bit 4.

The turning on of write-gate by the microprogram causes SERDES to write clock and data pulses on the selected device. Before the microprogram brings up write-gate the first byte of data to be written should be placed in the DR register. The SERDES transfers, automatically, the information in the DR register to the FDR register, takes this parallel byte of information and writes serial-by-bit information on the selected device.

The microprogram bringing up write-gate and address-mark lines causes SERDES to write an address-mark byte in the gap before the count field.

SERDES can be divided into three functional sections:

1. Write Section: This area contains a 2.5 megacycle crystal oscillator, write clock and data controls, write address-mark controls, and a write parity check circuit.
2. Read Section: This area contains a variable frequency oscillator (VFO), used in synchronizing the frequency of the 2841 read circuits to the frequency of the data coming in from the device selected. This section also contains read control circuits used in detecting address-marks.
3. Common Section: The read and write sections share some common circuits, namely:
  - a. Two bit rings ( $\Delta$  bit ring and bit ring)
  - b. The file-data-register (FDR).

The bit rings and the FDR perform parallel-to-serial conversion when writing and serial-to-parallel conversion when reading.

### 2.6.2 Write Operation:

- Write-oscillator, write-trigger, write-phase-X and write-phase-Y triggers are running all the time.
- Write operation begins with the microprogram bringing up write-gate.
- The 1600-ns-single shot is used to delay the turn on of the write-clock-gate for 1600 ns and to reset VFO-gate which in turn resets read-clock-gate if it is on.

- With both the read-clock-gate and the write-clock-gate off, delta-reset comes up, turning on the bit-ring-reset latch. The bit-ring-reset line is used to reset the bit ring latches all off by pulling them off. The delta bit ring latches are turned off except for  $\Delta 5$  which is pulled on.
- The allow-phase-Y latch insures that the bit-ring receives the first advance pulse (phase X).
- Coincidence of write-gate and not-write-clock-gate brings up the write-start line. The write-start line turns off the counter one flip-latch of the 4-position counter. Counter one is turned on or off by each data bit written.
- At the end of each byte, the counter one FL and the FDR parity bit are checked. Both FL's should be on or both FL's off to prevent an error.

The write operation sequence begins with the microprogram bringing up write-gate (Figures 2-25 and 2-26). Write-gate coming on starts the 1600 ns single shot timing to bring up  $\Delta$  reset. At the same time the 4-position-counter-reset is dropped. At the end of the 1600 ns single shot timing the write-clock-gate FL is turned on,  $\Delta$  reset is dropped and the bit-ring and delta-bit-ring are allowed to run. The  $\Delta$  bit-ring was held reset to delta 5 and the bit-ring reset to no count. The first drive pulse to the bit-ring sets the bit-ring to bit ring 5.

Each time the write-trigger is off a clock pulse is developed on the double-frequency-write-data line and sent to the selected device. At  $\Delta$ -bit-ring zero time the FDR register is reset and the information in DR is placed in the FDR register. At bit-ring zero time data is ready to be gated from the FDR register to the double-frequency-write-data line, if a bit is on in the FDR register. Each bit ring time gates the respective position of the FDR register. The write-trigger on allows data-pulses, if available, to be written on the device and the write-trigger being off allows the clock pulses to be written.

As data is being written on the device a check is made for proper parity in the attachment. Counter-one FL of the 4-position-counter and the FDR parity bit are used to make this check. When write gate comes on write-start turns the counter-one FL off. Each bit of data that is written on the device causes the counter-one FL to change states. At the end of each byte, the relative positions of FDR parity and the counter-one FL are checked. If the FDR parity bit and the counter-one FL are both on no error occurs or if both the FDR parity and counter-one are off no error occurs. If an error does occur, the

error register bit 0 is turned on so that the microprogram can check for this condition. Counter one is reset on at the start of each byte ( $\Delta$  zero, bit-ring zero).

At bit-ring 0 time of each byte after the FDR register has been set, the set-ST-4 latch is turned on. This latch then causes the ST4 bit to be set so that the microprogram may branch on this condition and know that the character has been moved from the DR register to the FDR register. The microprogram then must place a new character in the DR register before SERDES is ready to transfer the next character to FDR to prevent writing the same character over again.

When the microprogram wishes to write an address-mark it brings up the address-mark line. The address-mark line and write-gate and bit-ring zero time turns on the write-address-mark latch. The write-address mark FL on blocks the writing of clock pulses. The write-address-mark FL remains on until delta bit-ring 5 time when it is turned off and clock pulses can again be written.

When write gate comes up, the write FL is turned on. While in a write operation, if index is sensed, the index FL is turned on. If the write-gate is still on when the index pulse falls, the block-file-interface line is brought up to reset the FT and FC registers and prevent write operations of the devices past index.

To end a write operation, the microprogram drops write-gate. After write-gate falls, no more data can be gated to the devices. However, the serializer/deserializer circuits are still operating as if writing was taking place. The bit-rings operate, the write-triggers operate, and double-frequency-write-data is generated. The write serializer-deserializer circuits remain in this status until a new write operation is started or a read operation starts.

### 2.6.3 Read Operation

The 2841 uses a double frequency non return to zero (NRZI) method of recording. Due to variations in speed of the device from the time a record may be written to the time that a record may be read, the frequency at which it is received in the 2841 may vary. Also packs written on one drive may be read on a different drive. This is compensated for by the use of a variable frequency oscillator circuit which is described as a separate component in this section.

The 2841 track format of count, key, and data necessitates various types of gaps between portions of the record (Figures 2-30 and 2-33). All of the gaps have at least 4 bytes of zeros included in their format. These are used to synchronize the VFO with

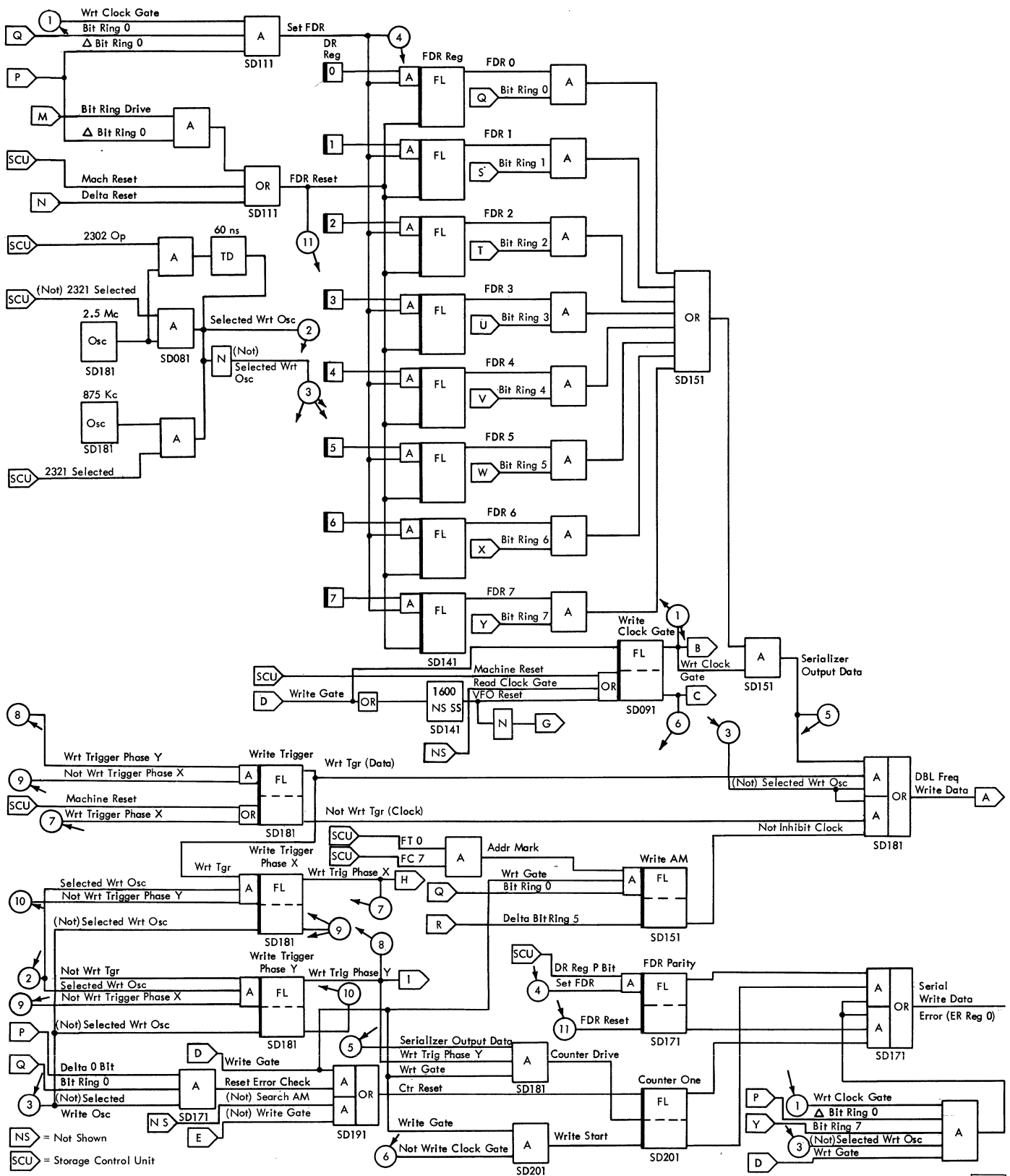


Figure 2-25a. SERDES Write Circuits

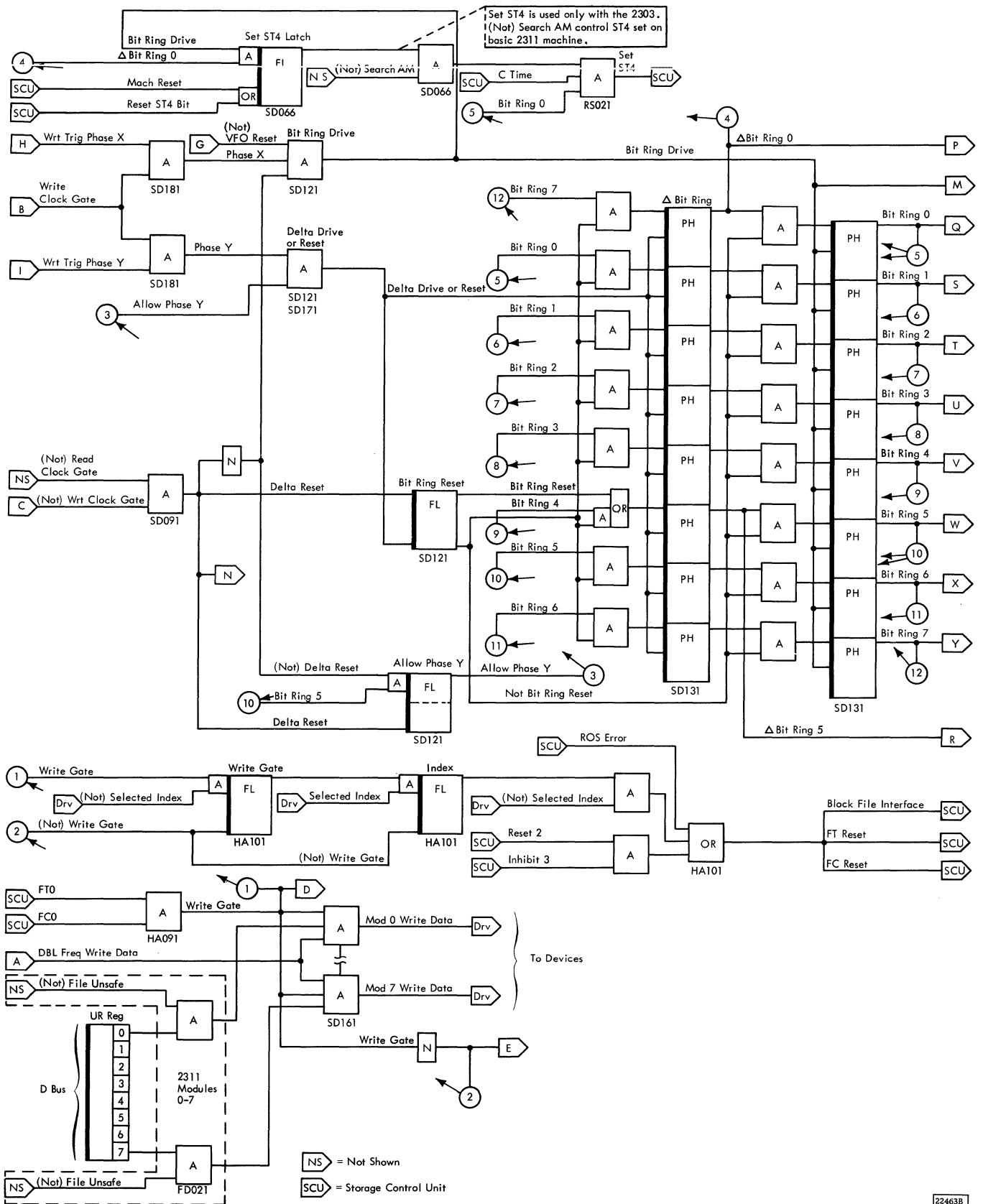
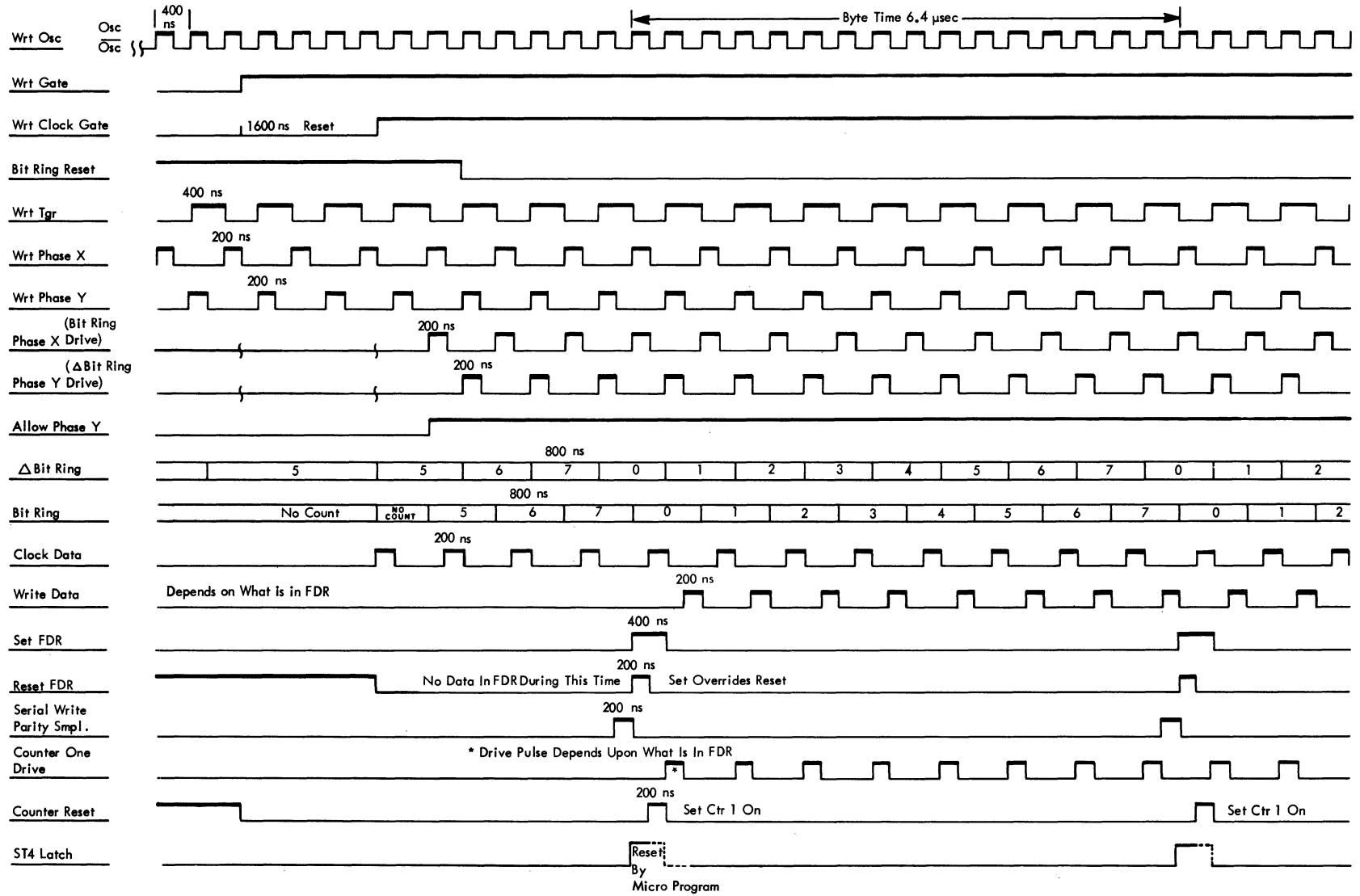


Figure 2-25b. SERDES Write Circuits



Figure 2-26. SERDES Write Timing



the clock pulses only. There are some variations in the number of bytes of one's and zero's between the gaps, however basically there are two types on gaps; home address or alpha gap, and the beta gap which includes the address mark. These two types are covered as a separate item in this section.

#### 2.6.3.1 Description of VFO Components

- Synchronize 2841 to device data.
- Separate clock and data pulses.
- Generate data or clock-gap sense.
- Determine if incoming data is a zero or one.

**Ramp Generator and VFO Trigger:** (Figures 2-29 and 2-28) The ramp-generator consists of a constant current source generating a linear ramp (5). The frequency of this ramp is normally 2.5 mc. The discharge (negative going portion of the sweep) complements the VFO-trigger. One state of this trigger is used as a clock pulse gate (6); the other for a data pulse gate (7).

The ramp generator is started with a VFO-Gate input. It is always running except:

1. During a write operation.
2. During VFO reset time in a read operation.

The frequency of the ramp is variable and is under control of the error signal (2) generated by the error-detector.

**Error Detector:** The error-detector controls the frequency of the ramp-generator. This is necessary since the frequency of the incoming data may not be the same as the normal frequency of the ramp. The read data and the 2841 are synchronized as follows:

1. A clock or data pulse (1) arrives from the device and samples the ramp output.
2. If the sample time is correct (the device and 2841 are in step), no error signal (2) is generated.
3. If the input pulse samples early or late on the ramp, an error level of negative or positive polarity is generated on the error signal line (2) and begins to correct the frequency output of the ramp-generator (5). When the 2311 and 2841 are in step again, the error signal will be minimal.

This frequency correction is continuously taking place whenever a device is selected. It is not designed to correct for an instantaneous frequency change, but rather a gradual change (i. e., speed of drive).

**Gate Generator:** The gate-generator is a differentiating network that converts the ramp to a non-symmetrical square wave (8). The gate-generator output develops separated data (10).

The circuit is adjusted for a 280 ns up level centered on the delayed-data-pulse (9) during the VFO adjustment procedure.

**Adjustable Delay Line and Single-Shot:** It is desirable to have the data (10) and clock (11) pulses centered on their respective outputs from the VFO-trigger. It is necessary, due to inherent delays in the other circuits (namely VFO-trigger), to introduce a fixed delay in the data line. The fixed delay is introduced by a tapped delay line (9), adjustable in increments of 5 ns, from 0 to 125 ns. During the VFO adjustment procedure, the delayed-data is centered on one of the outputs of the VFO-trigger.

The single-shot serves as a pulse shaping network for clock and data pulses.

**Gap Sensor:** This circuit is used to detect clock and data gaps.

If separated data pulses are absent for 2.4  $\mu$ sec, data-gap-sense rises (12).

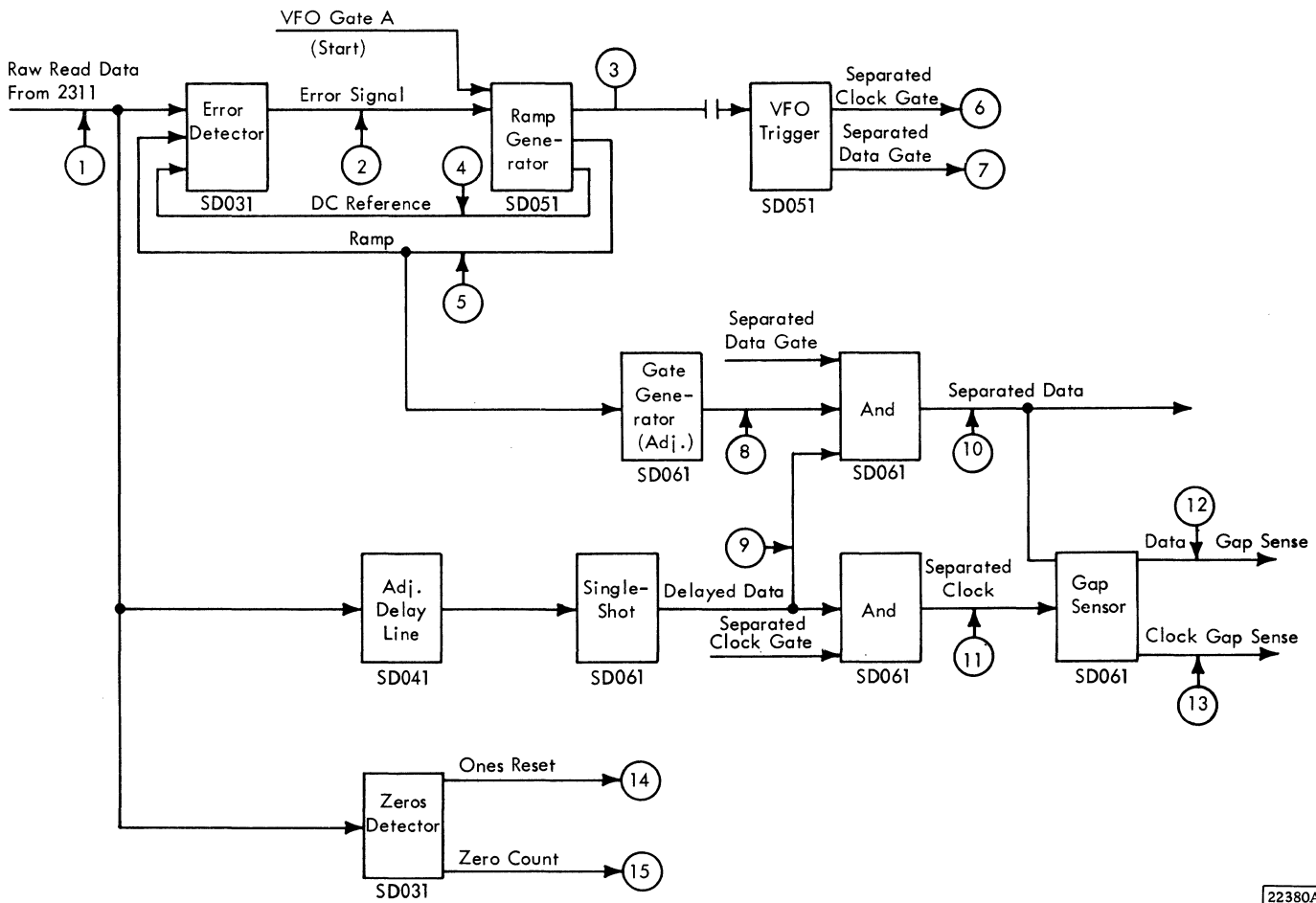
If separated clock pulses are absent for 2.8  $\mu$ sec, clock-gap-sense rises (13).

**Zeros Detector:** When looking for an address mark, the VFO may be 180° out-of-sync. Therefore, some type of circuit is needed to identify a particular area as having a zero or a one.

The zeros-detector identifies an area by looking at an 800 ns period without regard to which pulse is clock and which one (if any) is data. If it finds one pulse during the period, it raises the zero-count-line (15). Two pulses in the period raise the ones-reset line (14). Ones-reset remains up until the next zero is detected.

The zeros-detector is a special circuit that acts as a single shot on the zeros-count output and as a latch on the ones-reset output.

The voltage divider networks generate the ramps shown in Figure 2-28. When the pulses are 800 ns apart the zeros-ramp times the zeros-count single shot. When the pulses are 400 ns apart the zeros-ramp does not time the zeros-count single shot and



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Figure 2-27. Variable Frequency Oscillator Circuit Operation

the ones-reset ramp sets the ones-reset latch. The ones-reset latch is turned off by the next zeros count pulse.

### 2.6.3.2 HA or Alpha Gap Sequence

- The microprogram knows the orientation of the read heads to the track data when attempting to synchronize in an alpha or HA Gap.
- The operation is initiated with the raising of read-gate by the microprogram in the leading zeros area.
- The VFO synchronizes to the data in the remaining bytes of zeros.
- The bit rings are freed after the turning on of read-clock-gate.
- The allow-phase-Y latch insures that the bit-ring is stepped first.
- DR is loaded with the last three bits of the sync byte.

- ST 4 is set to indicate to the microprogram that SERDES has found a sync byte.

General (Figures 2-29, 2-30, and 2-31): The HA and alpha gaps are similar in content, except that HA has more bytes of leading zeros. This is necessary because of the time required for head switching that can occur at index. Key and data gaps have bytes of ones ahead of the bytes of zeros.

Synchronization of the VFO with read-data is initiated when the microprogram raises read-gate.

For a command which operates on HA, the microprogram branches on index, delays a fixed amount of time into the HA gap, and then raises read-gate.

When synchronizing in an alpha gap (i.e., between key and data areas), the microprogram must stay in a timing loop. During this loop, read-gate is down. When the timeout occurs (approximately 80  $\mu$ sec), the microprogram raises read-gate in the leading zeros area of the alpha gap. The dropping and raising of read-gate in this gap accomplishes two things:

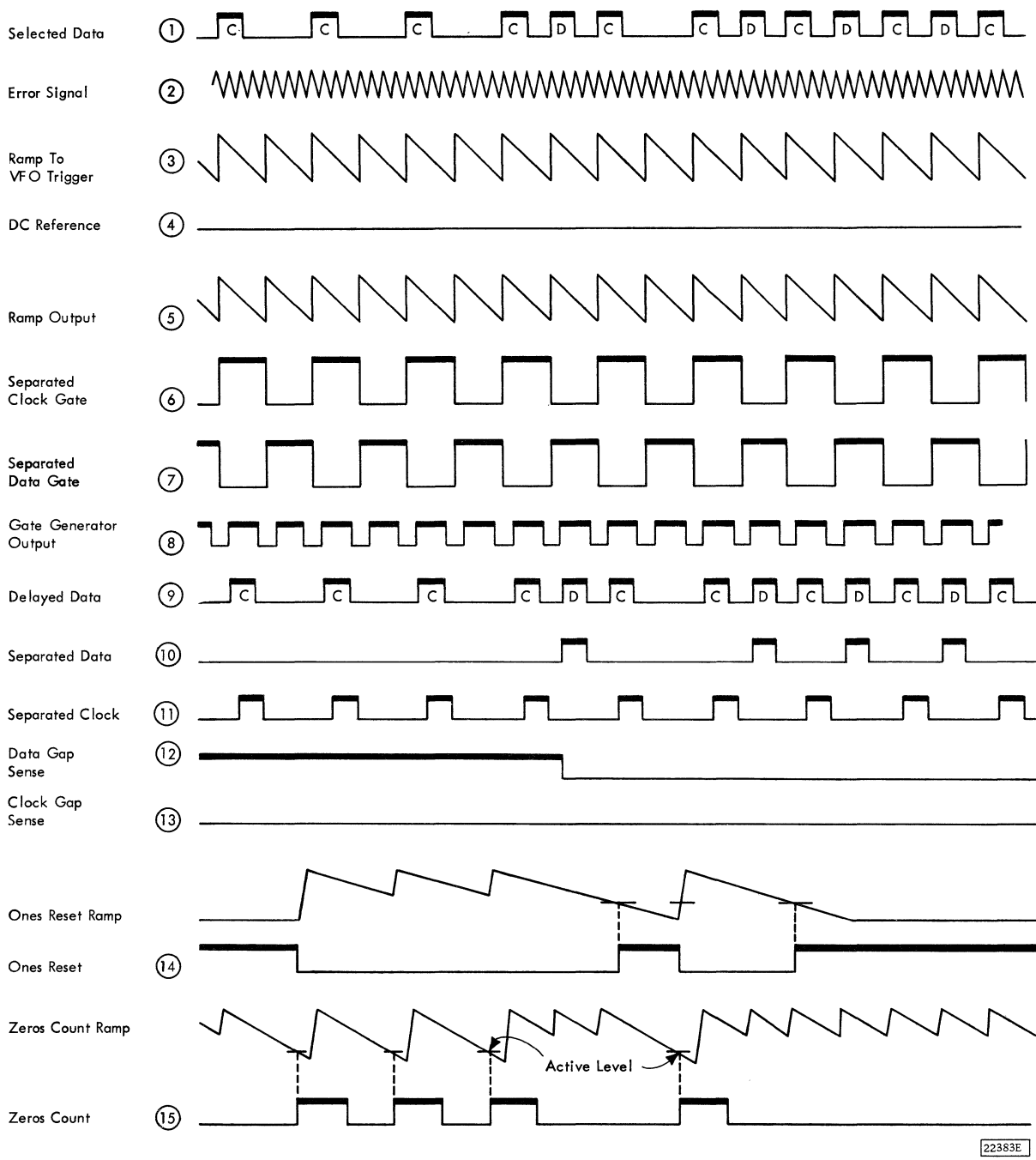


Figure 2-28. VFO Circuits Timing

1. The VFO and bit rings are resynchronized on the data from the data area. This is necessary since the key and data areas may not have been written with the same command and may even have been written on different drives.
2. The microprogram does not have to count the number of bytes in the gap. The microprogram is notified by SERDES when the sync byte is in DR by the setting of ST 4.

Description: Figure 2-31 shows the timing relationship of the circuitry in Figure 2-29.

Read-gate raising resets the VFO-sync latch and VFO-gate latch for 1600 ns. The VFO-sync latch allows the VFO-gate latch to turn on with the next clock pulse. The ramp-generator is started with VFO gate.

During the remaining bytes of zeros, the ramp's frequency is adjusted to the read-data frequency by the error-detector circuit. During this time the

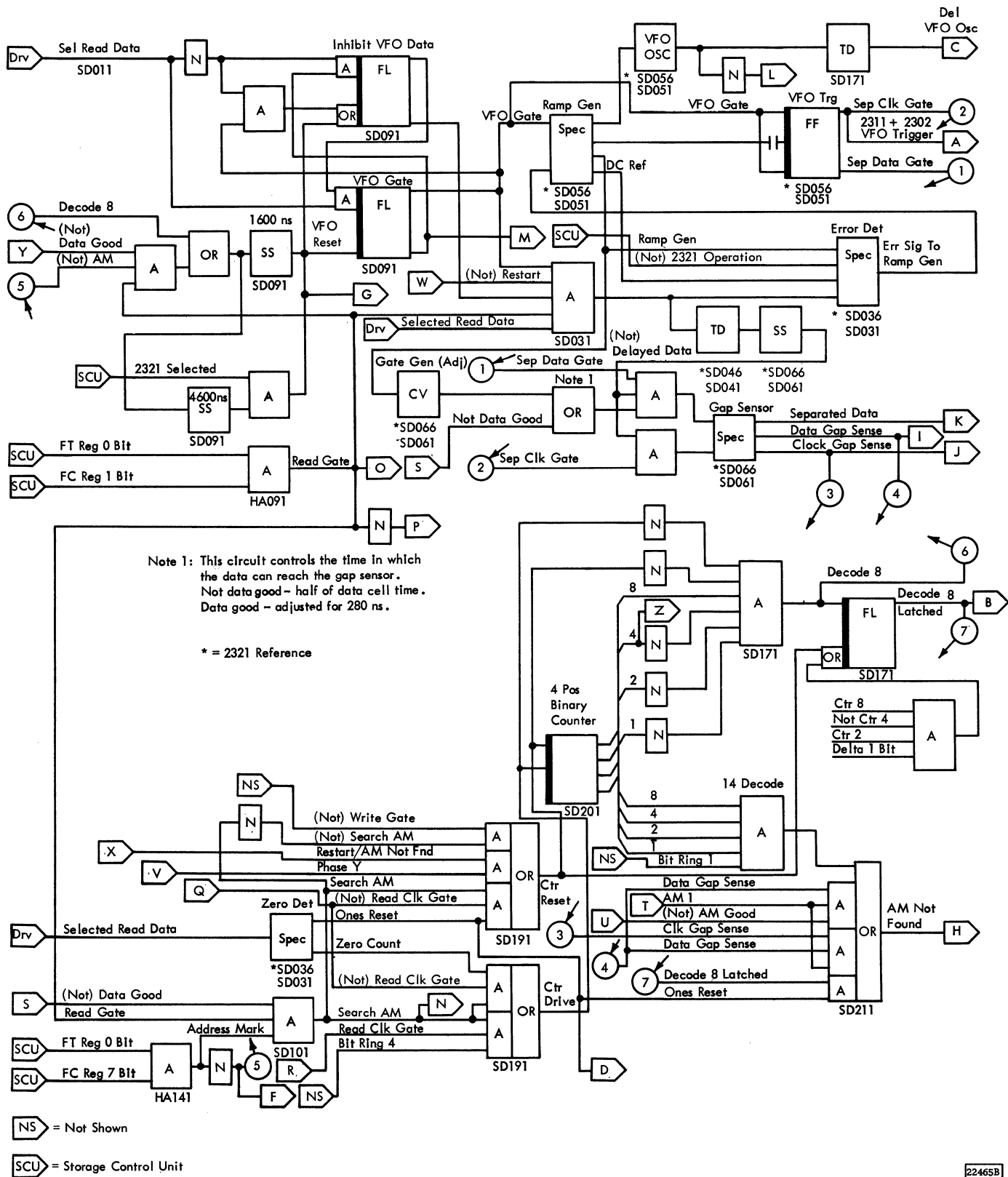


Figure 2-29a. SERDES Read Circuits

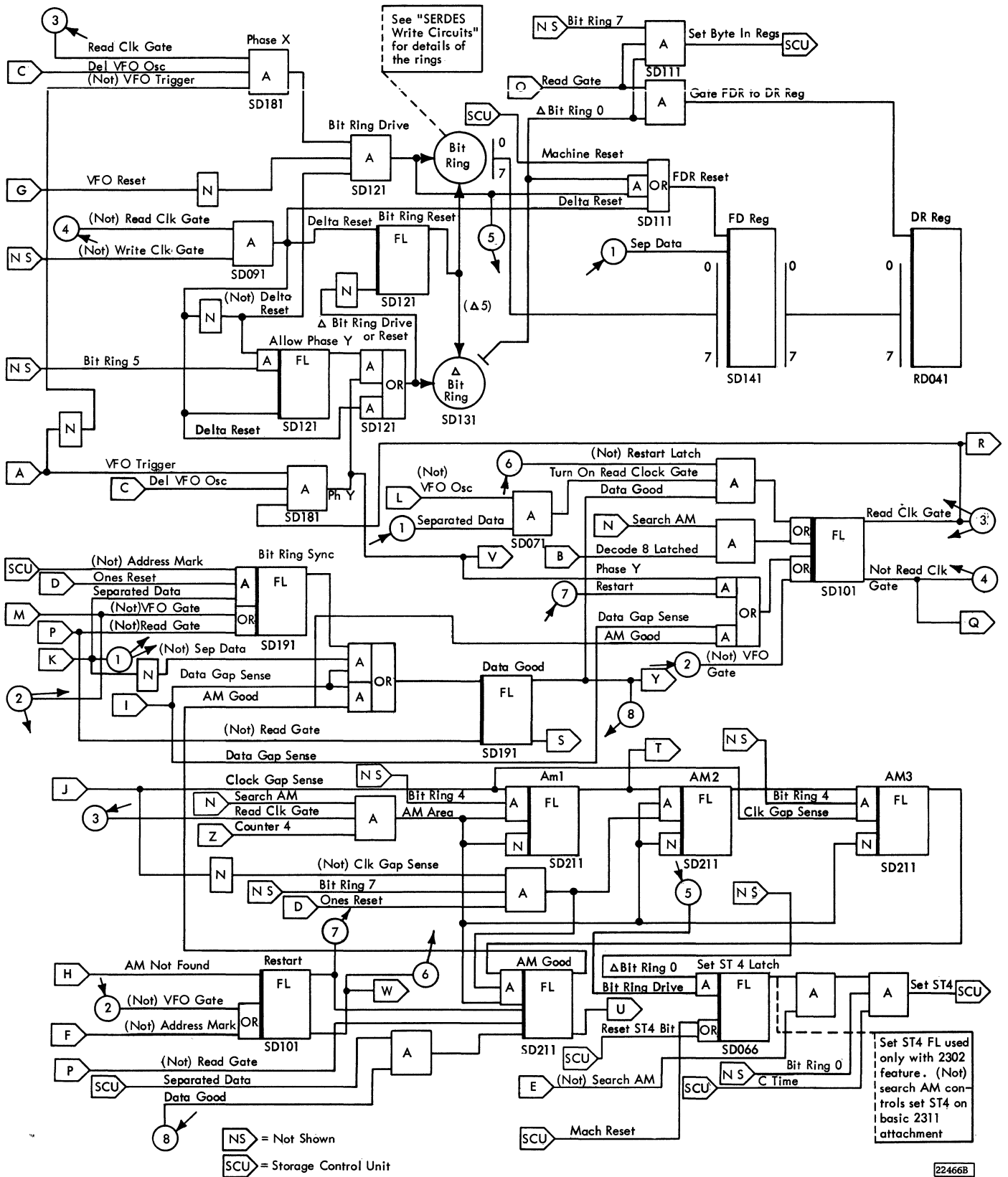
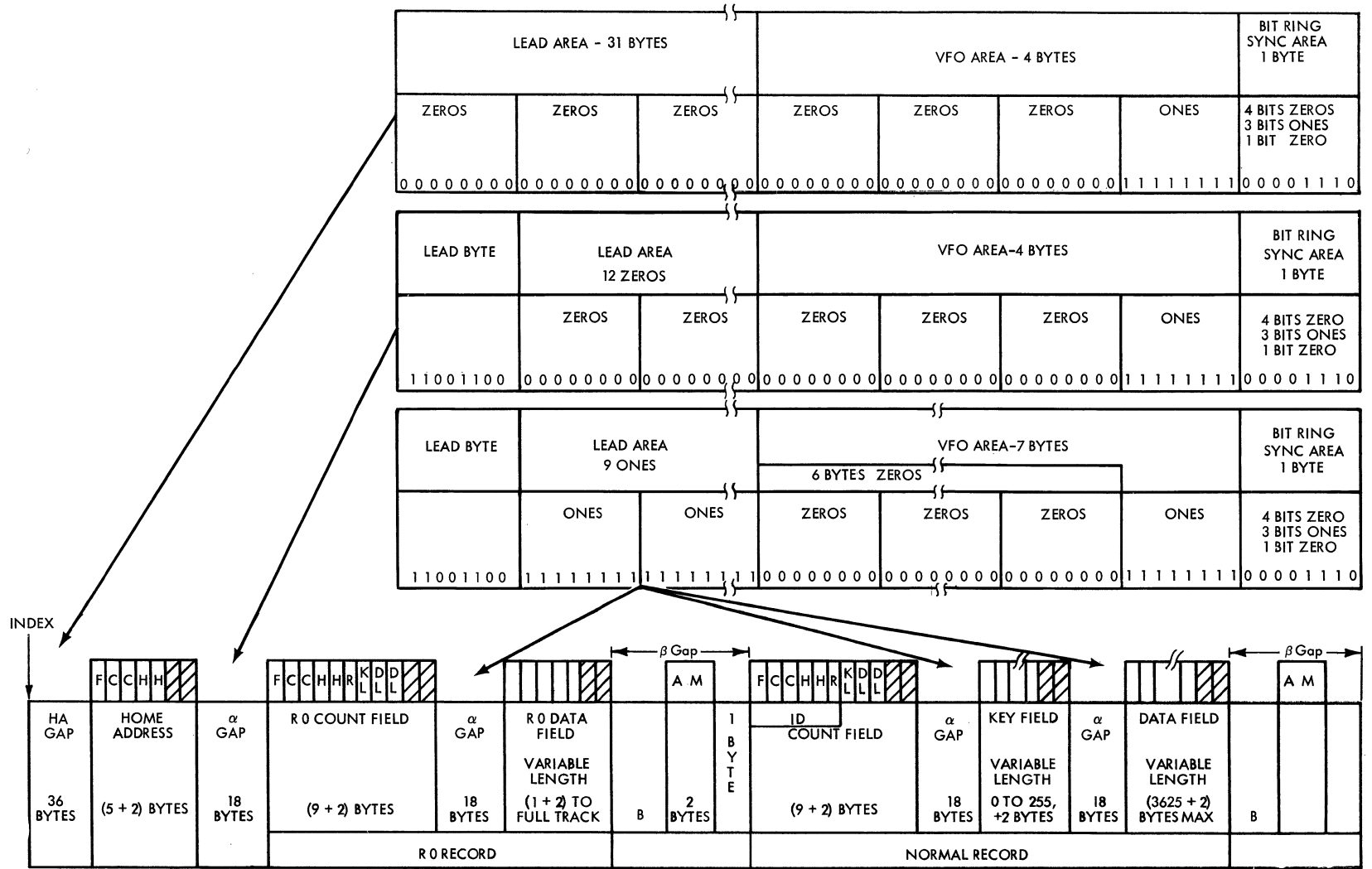
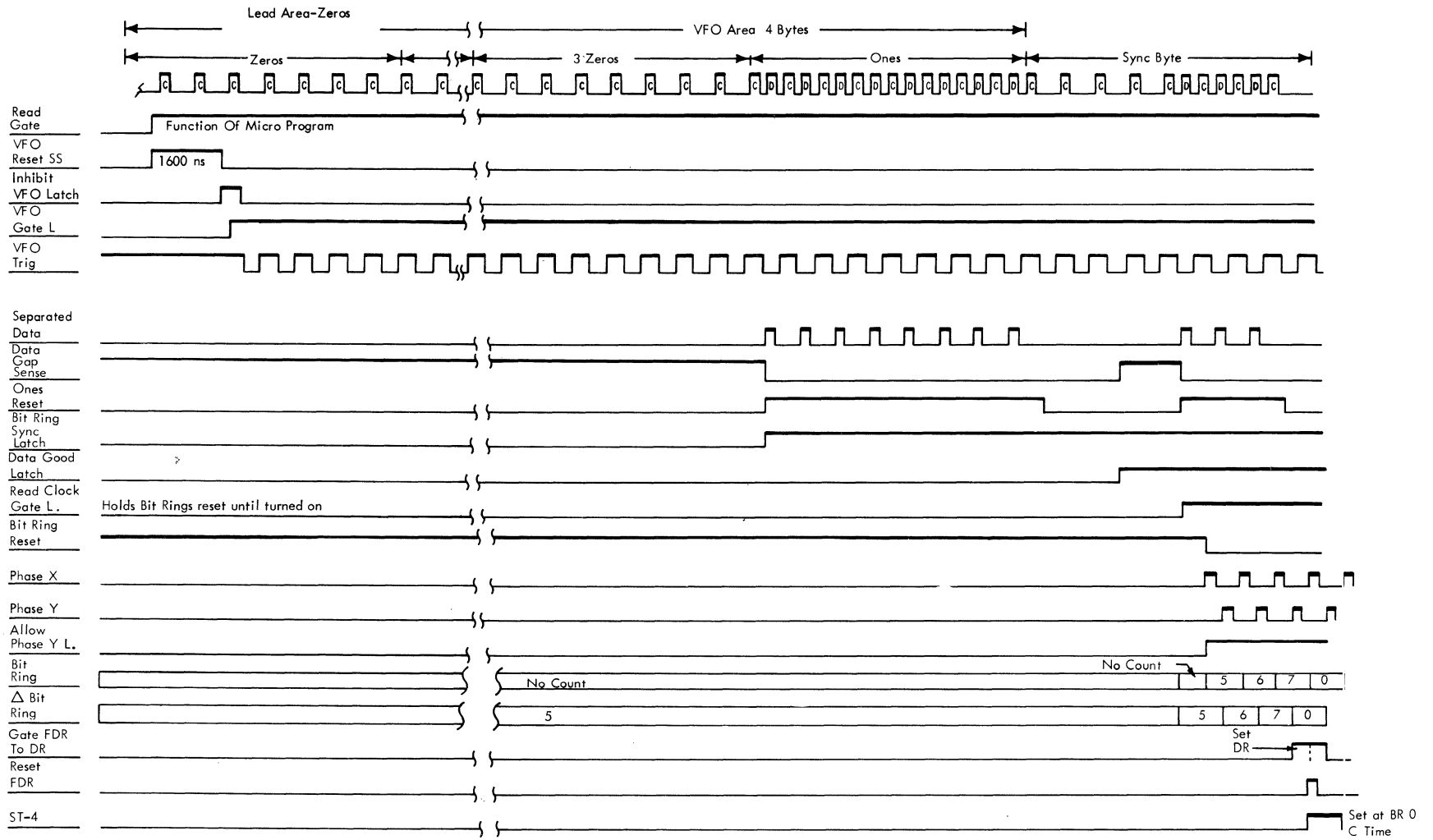


Figure 2-29b. SERDES Read Circuits

Figure 2-30. HA and Alpha Gap Bit Configurations





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Figure 2-31. HA or Alpha Gap Timing Diagram



bit-rings are held reset; bit-ring to no latches on, and delta-bit-ring to 5.

The bit-ring-sync latch is set with the first data bit in the gap.

Data-gap-sense sets data-good. The first data bit of the sync byte sets the read-clock-gate to drop delta-reset. The allow-phase-Y latch is off so that the first bit-ring advance is a phase-X pulse and steps the bit-ring to 5.

Bit-ring-5 turns on the allow-phase-Y latch and allows bit 5 of the sync byte to be set into FDR.

The bit rings continue to step, allowing separated data to be placed in FDR by the respective bit ring time. Although the sync byte equals 14(10) only the last three bits are gated into FDR and consequently to DR at bit ring 0 time. The microprogram is notified of this action by the setting of ST 4 (bit-ring-0, C time, and not-search-AM). DR should equal 6(10) and is checked by the microprogram. SERDES is now in step with the data of the field, and the sequence is continued by the microprogram until the count of the field has been read.

### 2.6.3.3 Beta Gap Sequence

- The microprogram does not know the orientation to the track of the read heads.
- The operation is started when the microprogram raises the read-gate and address-mark-search lines.
- The VFO synchronizes on the read data and looks for a particular combination of bits.
- If bits are incorrect, the operation is restarted.
- Eventually the proper bit configuration is found.
- DR is loaded with last three bits of the sync byte.
- ST 4 is turned on.

**General** (Figures 2-29, 2-32, and 2-33): The beta gap is unique in that it contains two address mark bytes. These should be the only bytes (on a track) that have missing clock bits.

The microprogram initiates the beta gap sequence by raising read-gate and the address-mark-search lines. The microprogram generally does not know where the heads are located in relation to the track data when it raises these lines. SERDES, therefore, looks for the beta gap (address mark),

and notifies the microprogram (by setting ST4) when it has found an address mark and read the sync byte.

**Description:** Figure 2-32 shows the timing relationship of the circuitry in Figure 2-29.

The microprogram raises read-gate and the address-mark-search lines. This can happen anywhere on the track. Figure 2-34 shows this happening in the last byte of ones in the beta gap.

The VFO sync latch is held reset for 1600 ns. The bit rings are held reset because the read-clock-gate is off. When the reset times out, the VFO is started with the incoming data. The timing chart shows a data pulse starting the VFO, therefore, the VFO is 180° out-of-sync.

The zeros-detector finds one bits (400 ns pulses) in the read data and raises the ones-reset-line. This holds the 4-position binary counter off.

The zeros-detector finds zero bits (800 ns pulses) in the read data, turns off ones-reset and raises zeros-count. Since the read-clock-gate is off at this time, each zeros-count pulse steps the 4-position counter until it reaches 8. If there are nine zeros in a row, this may be a beta gap.

A decode of count 8 resets the VFO circuits, and turns on the read-clock-gate latch. The VFO circuits are reset here so that they may resync in a zeros only area. After 1600 ns the VFO circuits have resynchronized. Read-clock-gate turning on removes the reset to the bit rings. The allow-phase-Y latch ensures that the bit-ring is stepped before the delta-bit-ring. The bit rings start stepping at bit-ring 5 time. Since read-clock-gate is on, bit-ring-4 is used to step the 4-position counter. During the remaining bytes of zeros, the ramp's frequency is adjusted to the read data frequency by the error-detector circuit.

The AM-1, -2, -3, and AM good latches are sequenced by clock-gap-sense, in AM bytes one and two. Data-gap-sense, occurring in the sync byte, resets the read-clock-gate latch and sets the data-good latch.

Read-clock-gate dropping:

1. Resets AM 1, 2, and 3 latches.
2. Delta-reset resets the bit rings so their count can be adjusted for bits 5, 6, and 7 of the sync byte.

Data-good turning on drops the search-AM line and allows the AM-good latch to turn on with the next separated-data pulse.

Read-clock-gate is turned on again with the first data pulse of the sync byte. The allow-phase-Y latch

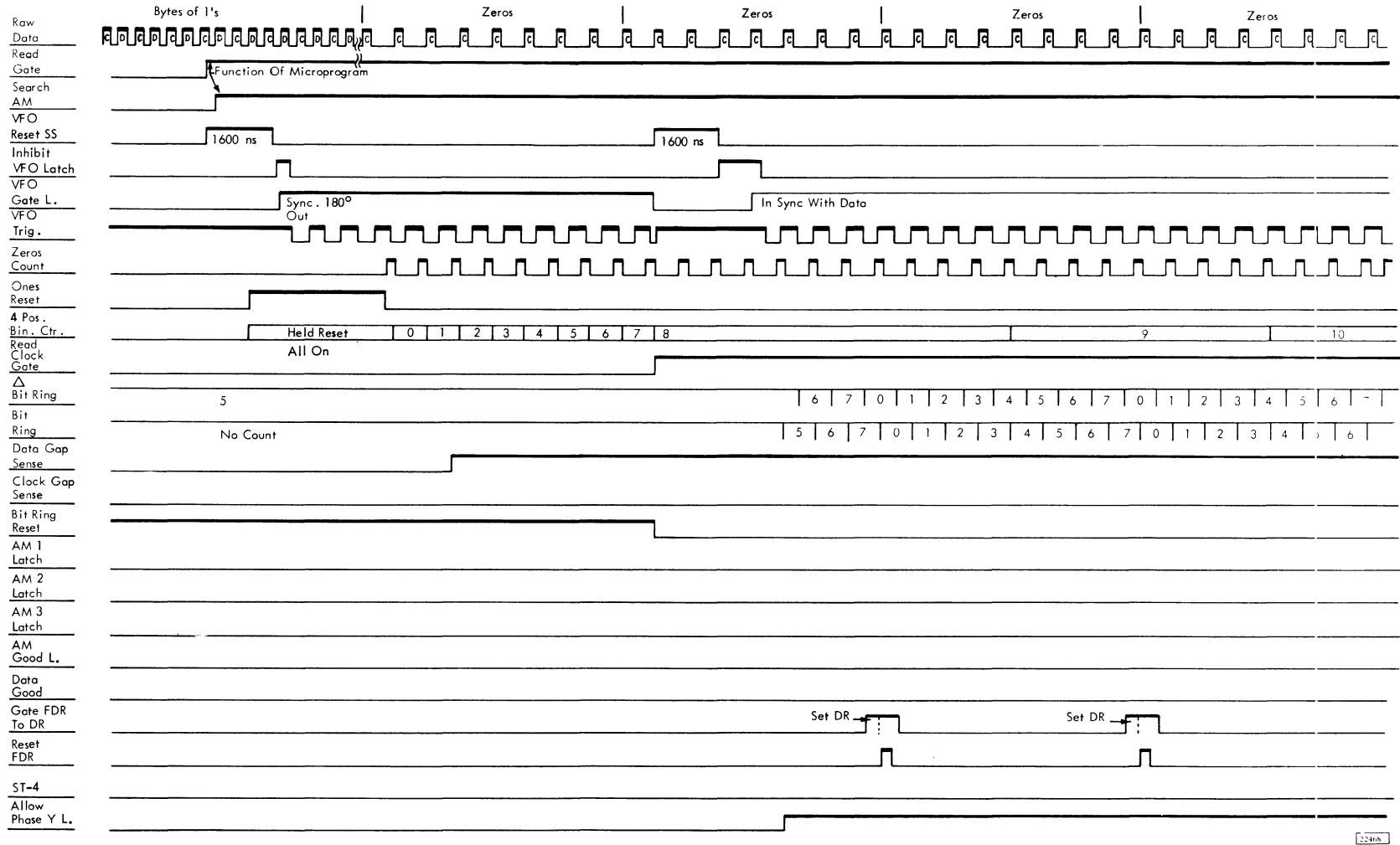


Figure 2-32a. Beta Gap Timing Diagram (Sheet 1 of 2)

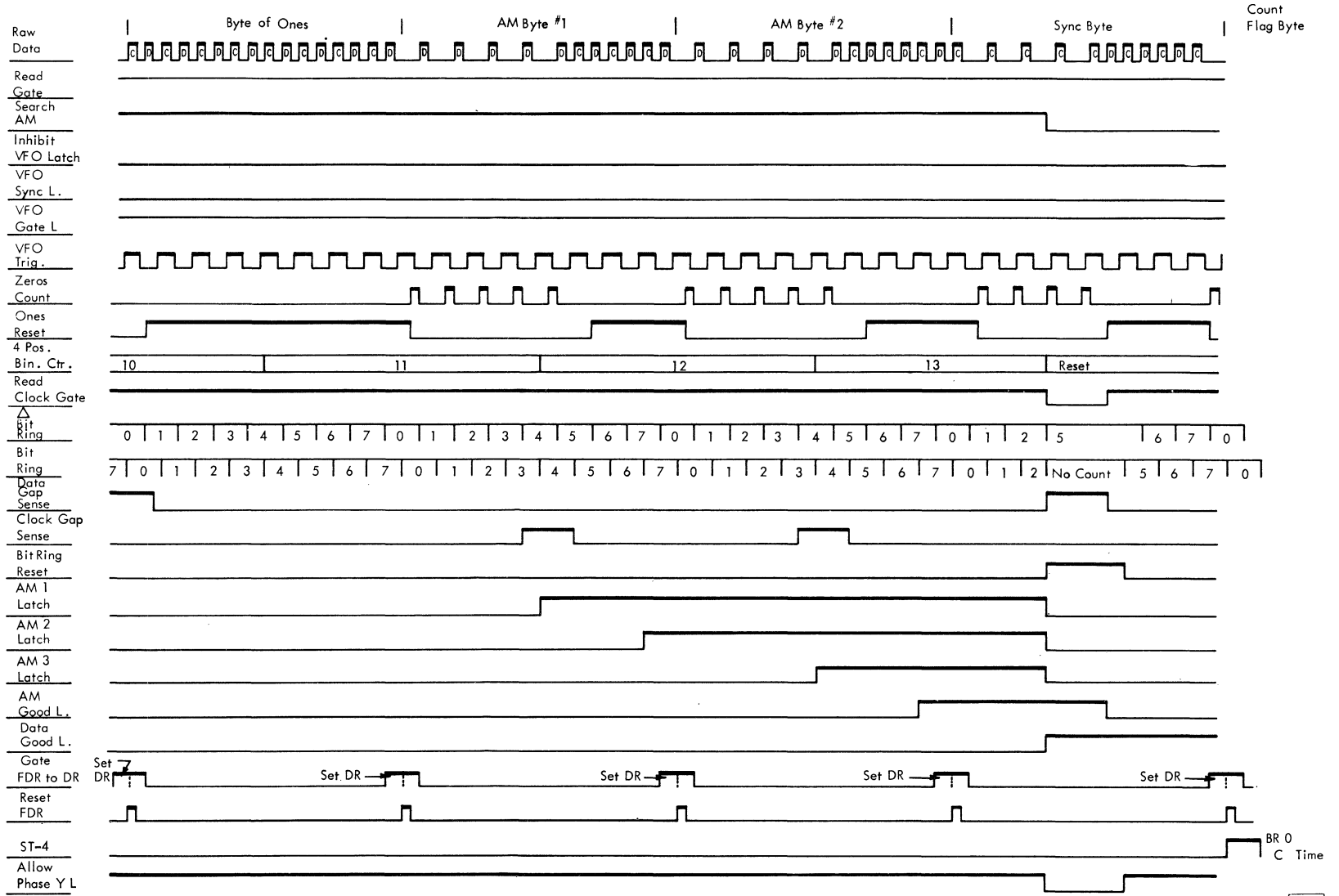
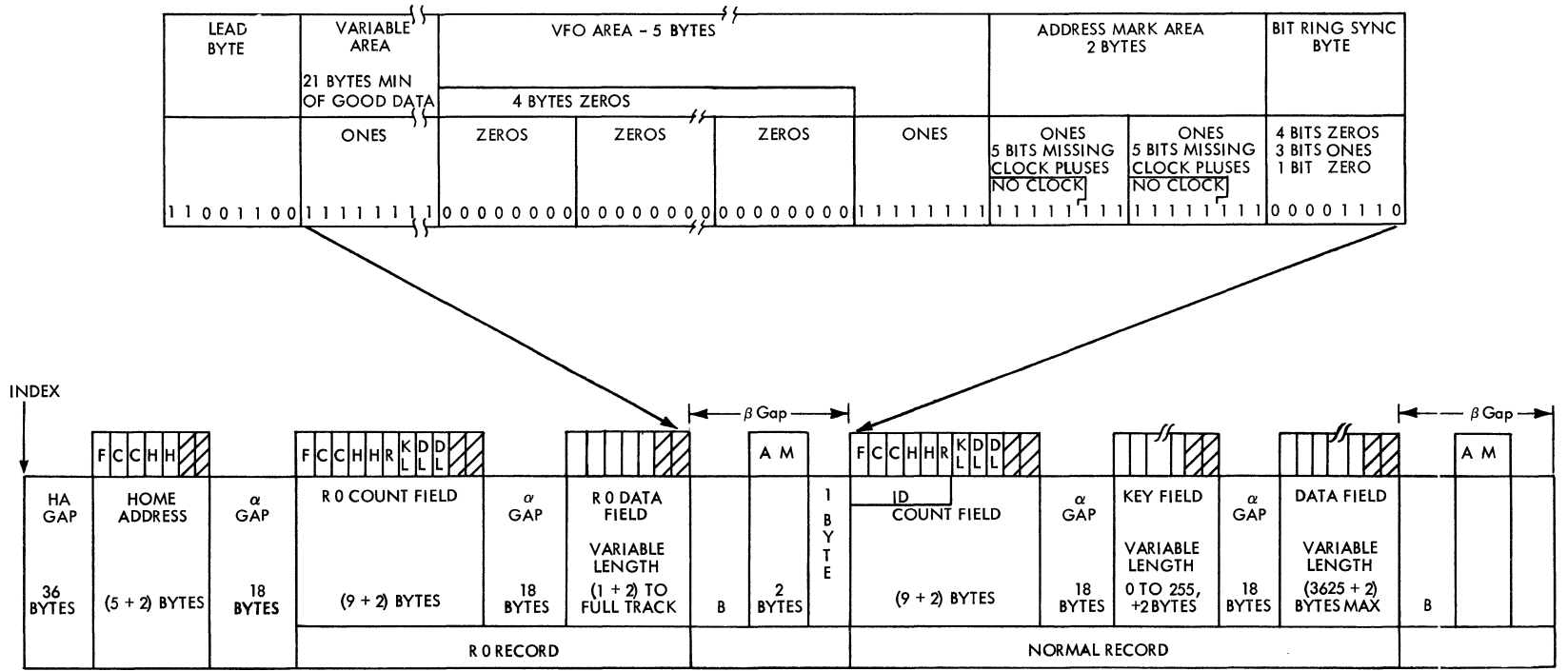


Figure 2-32b. Beta Gap Timing Diagram (Sheet 2 of 2)

Figure 2-33. Beta Gap Bit Configuration



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ensures that the bit-ring is stepped to bit-ring 5 before the delta-bit-ring steps to 6.

The bit rings step. Bits 5, 6, and 7 of the sync byte are gated into FDR, and subsequently into DR at bit-ring-0 time. The microprogram is notified that SERDES has found an address mark by the setting of ST 4 (bit-ring-0, C time, and not-search-AM).

The microprogram checks DR for 6. If it is 6, the operation continues. If it is not 6, the microprogram drops read-gate and AM-search, delays, and reinitializes the operation. If SERDES cannot find a good address mark, between index points, unit-check in the status byte and no-record-found in the sense data is indicated.

**Restart Conditions:**

1. Ones-reset, when the read-clock-gate is off, resets the 4-position counter. This means that fewer than 9 zeros in a row were read.
2. Decode-8 of the counter and ones-reset. This is the area where the VFO is resynced on clock pulses. If a one bit is here, the VFO is still out of sync with the read data.
3. AM-1 on, data-gap-sense, and not-AM-good. Checking for missing data bits in the two AM bytes.
4. AM-1 on, clock and data-gap-sense. This could occur in some area where no clock or data had been written.
5. Counter 14. No data-gap-sense in an area SERDES thought should have been the sync byte.

Restart conditions 2, 3, 4, and 5 reset:

1. The read-clock-gate latch.
2. The 4-position counter.
3. The AM-good latch.
4. AM 1, 2, and 3 latches when read-clock-gate drops.

**2.7 CHANNEL INTERFACE ATTACHMENT**

- The channel interface consists of seven sections (Figure 2-34).

1. Selection controls out.
2. Tags out.
3. Selection controls in.
4. Tags in.
5. Bus out.
6. Bus in.
7. Service in/out controls.

Due to the full feature drawing of the ALD's the channel attachment has line names for the two chan-

nel switch feature. The switched-to-A line is floating to give the active level and the switched-to-B line is jumpered to ground to hold it inactive, when the feature is not installed.

This section covers the basic attachment only.

The various sequences which the channel interface goes through are presented to tie together the seven sections. The microprogram philosophy is introduced where necessary to accomplish the sequence.

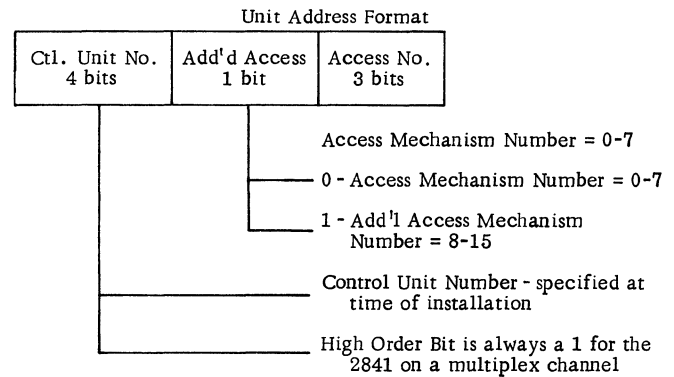
**2.7.1 Initial Selection Sequence**

- The initial selection sequence (Figure 2-34) is used to connect the channel to the 2841.
- Initial selection ends with the transfer of the initial status byte.

The initial selection sequence is as follows:

1. Initial condition – Steering-latch-A is off.
2. Channel places an address byte on bus-out and raises address-out.

The address byte contains the access and control unit number:



The control unit number may be any configuration selected by the customer at installation.

3. The 2841 compares bits 0, 1, 2, and 3 of the address out byte with its prewired address. It also checks parity (odd) of the entire byte. If the address is the same (address compare) and parity is good, the steering-latch-A is turned on. If the address doesn't compare or the byte has incorrect parity, the select out steering latch is left off.
4. Channel raises select out.

If the steering-latch-A is on (address compare and good parity), initial-select-A is raised in the

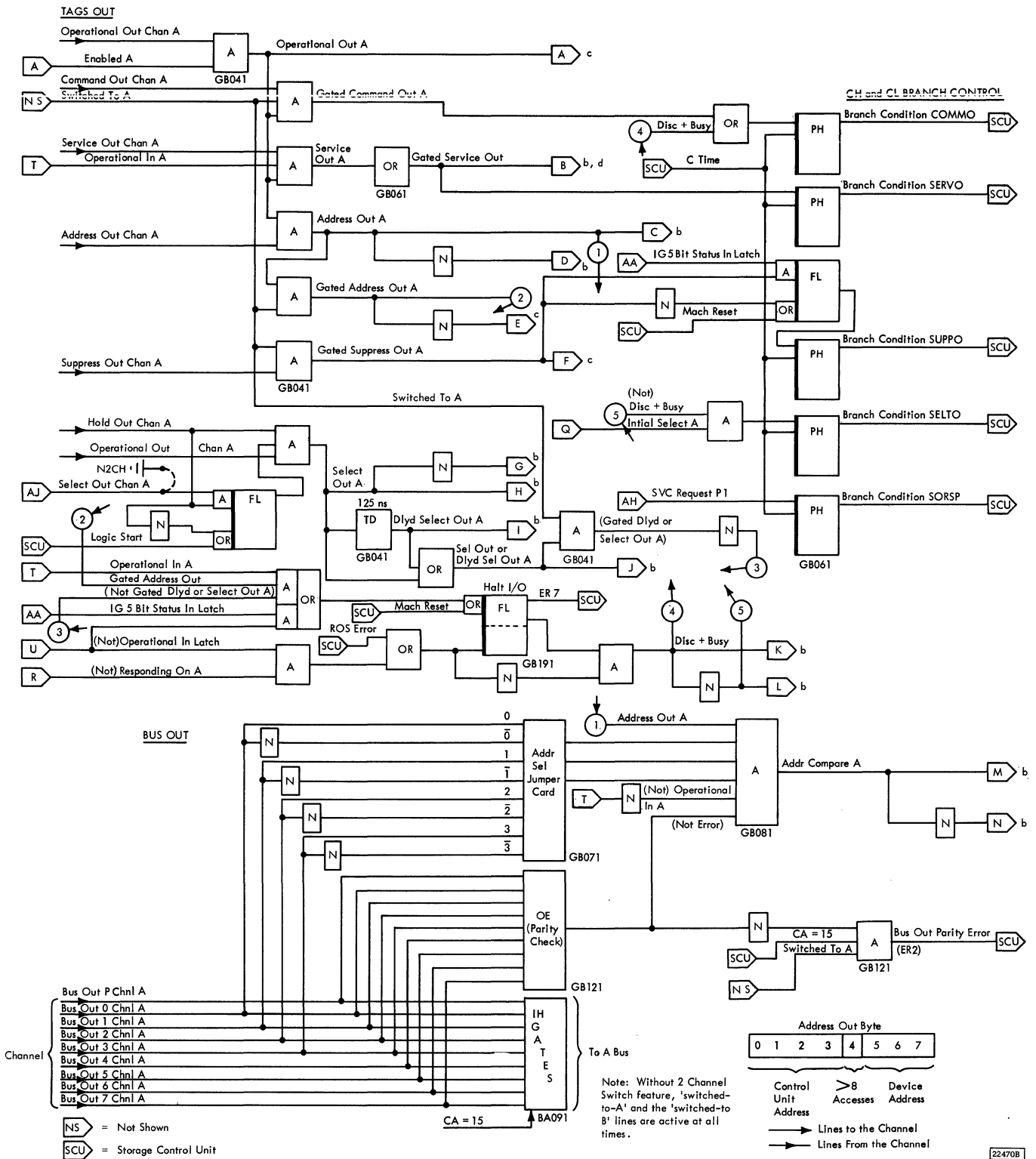


Figure 2-34a. Data Flow - Channel A Attachment

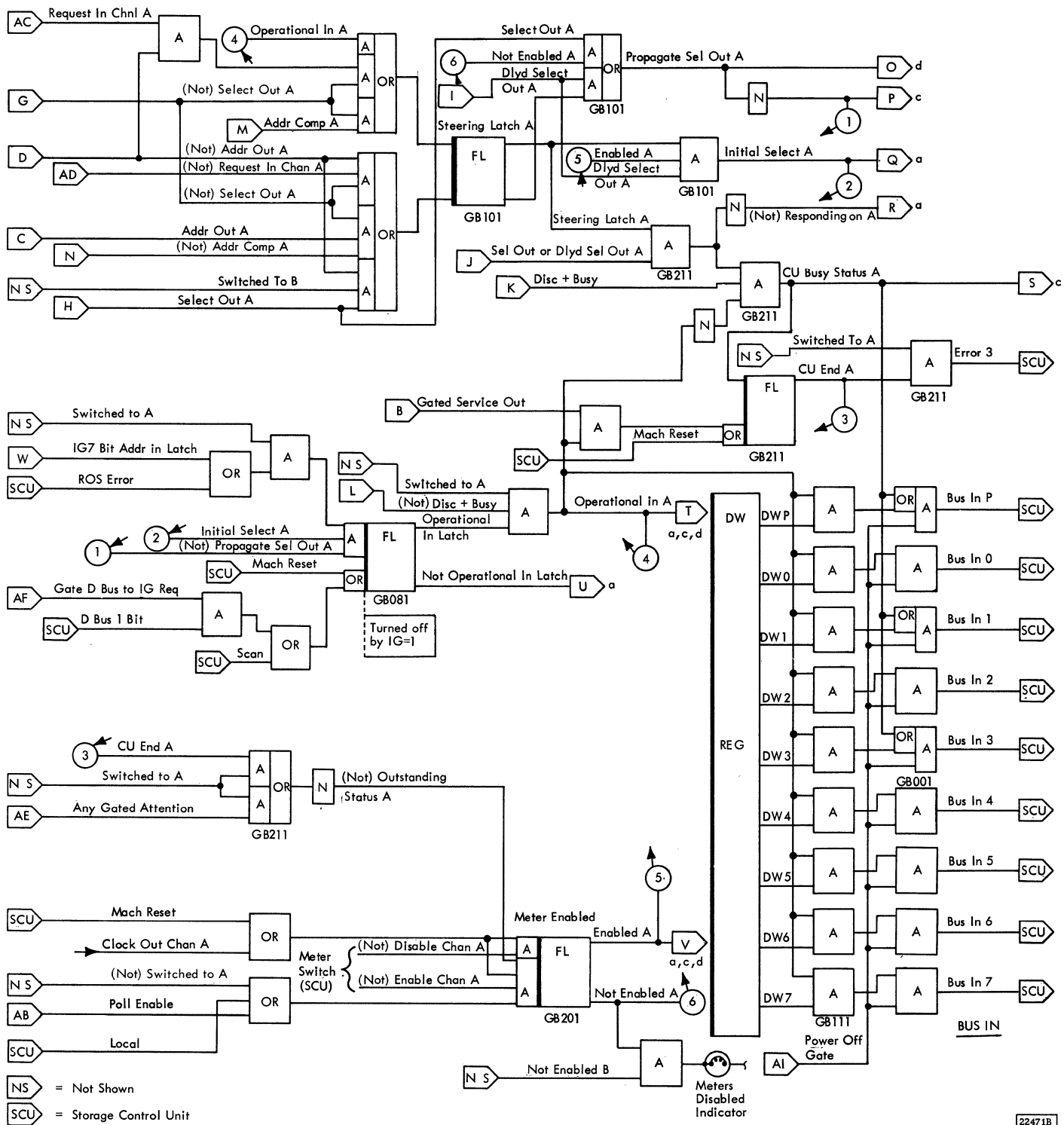
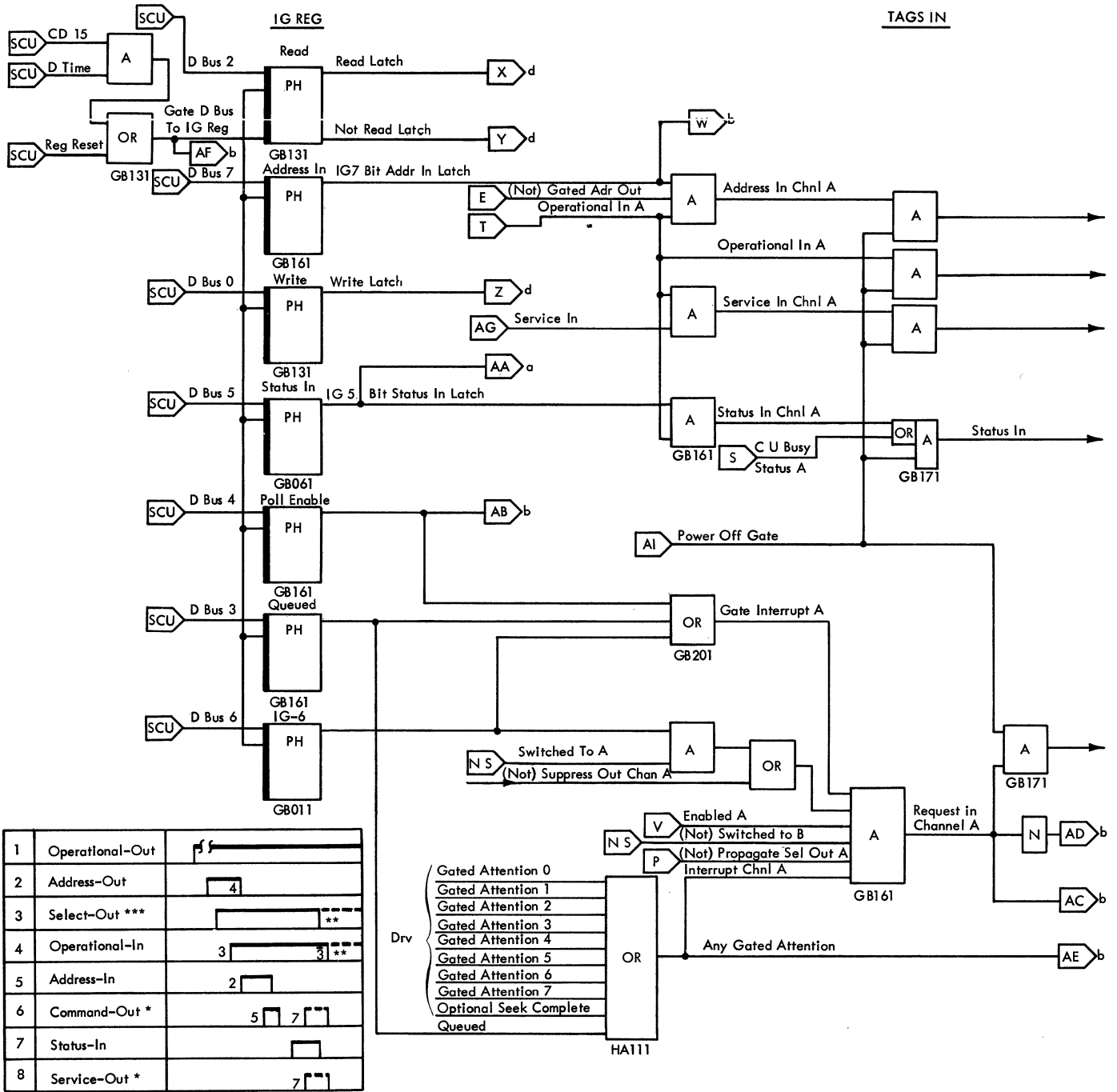


Figure 2-34b. Data Flow - Channel A Attachment



\* A multiplex channel responds to status-in with either command-out or service-out. Normally, a selector channel responds to status-in with only service-out.

\*\* Depending on the channel controlling the operation, select-out might drop during the initial selection sequence or remain active after the sequence is complete. Operational-in cannot drop until select-out is inactive.

\*\*\* Select-Out and Hold-Out up together.

NS = Not Shown  
SCU = Storage Control Unit

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Figure 2-34c. Data Flow - Channel A Attachment



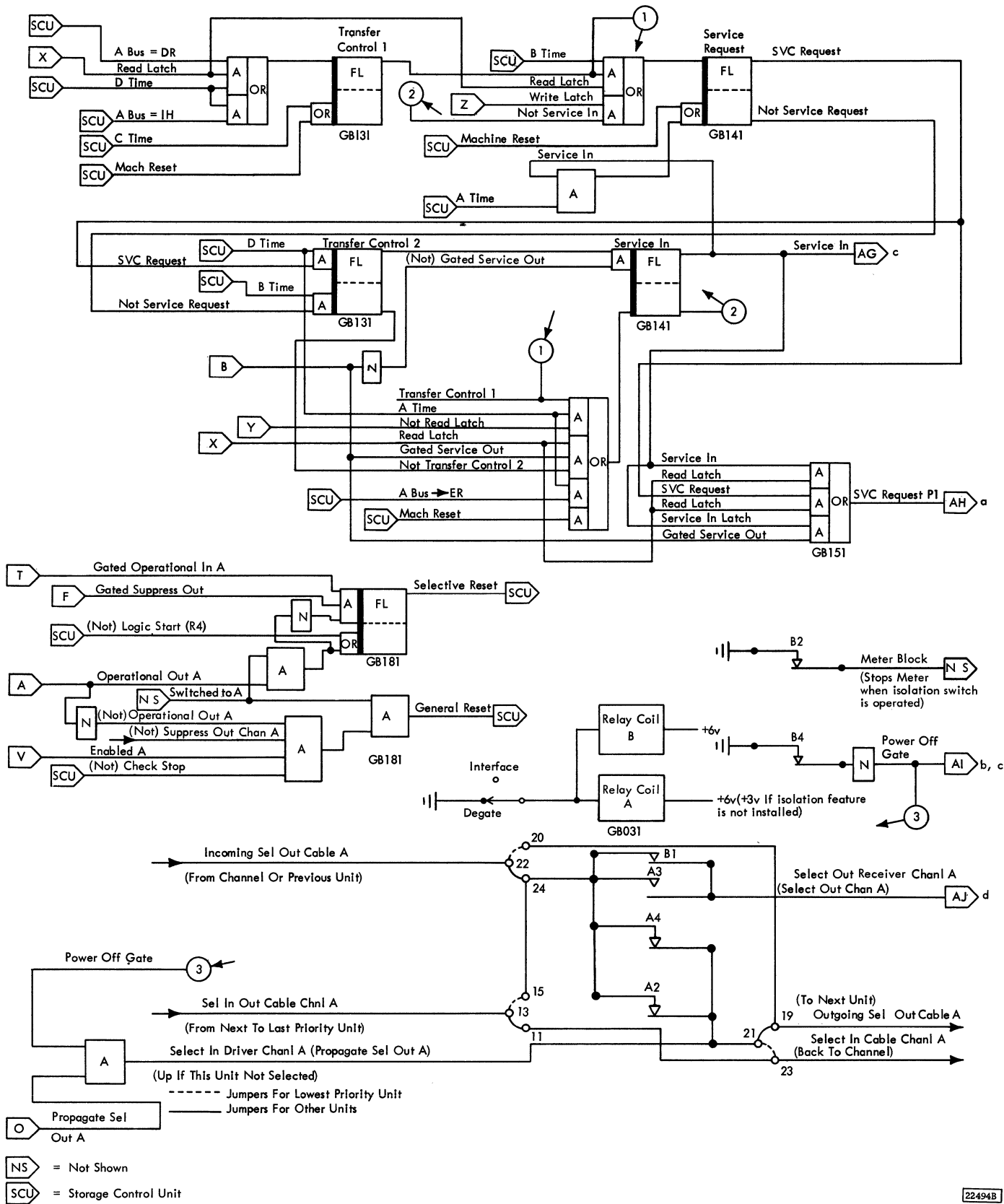


Figure 2-34d. Data Flow - Channel A Attachment

2841. Up to this time, the 2841 has been operating on channel timing. It is now necessary to get in step with the microprogram timing. The SELTO latch is turned on at the next 2841 clock C time. SELTO is a condition that can be tested by the microprogram.

NOTE: If the steering-latch-A is off (address did not compare or bad parity), select out is propagated to the next control unit.

5. The microprogram branches on SELTO, goes through several ROS words, and sets the address-in latch with the ALU statement  $1 \rightarrow IG$  (D bus bit 7).
6. The address-in latch on turns on the operational-in FL and causes the operational-in line to be sent to channel.
7. The operational-in line causes the channel to drop the address-out line.
8. The address-out line dropping causes the address-in line to be sent to channel. Before raising the address-in line, the 2841 microprogram places the address-in byte in the DW register.
9. The command-out line is sent from the channel. The COMMO latch is set on at the next C time. The microprogram branches on COMMO recognizing that command out has been sent.
10. The microprogram drops the address-in line with the ALU statement  $ER33 \rightarrow IG$ .
11. The channel drops the command out line.
12. The microprogram loads the DW register with the status byte and raises the status-in line with the ALU statement  $4 \rightarrow IG$  (D bus, bit 5).
13. The channel responds to the status in line by raising the service out line. The SERVO latch is turned on at the next C time.
14. The microprogram causes the status-in line to drop with the ALU statement  $0 \rightarrow IG$ .
15. The channel drops the service out line.
16. This completes the initial selection sequence.

### 2.7.2 Data Transfer Sequences

- The 2841 contains circuitry that controls the service in/service out responses to the channel (Figure 2-34).
- The controls are in read mode for read and sense commands.
- The controls are in write mode for write, search, and some control commands.

The service-in/out controls are used for two types of operations:

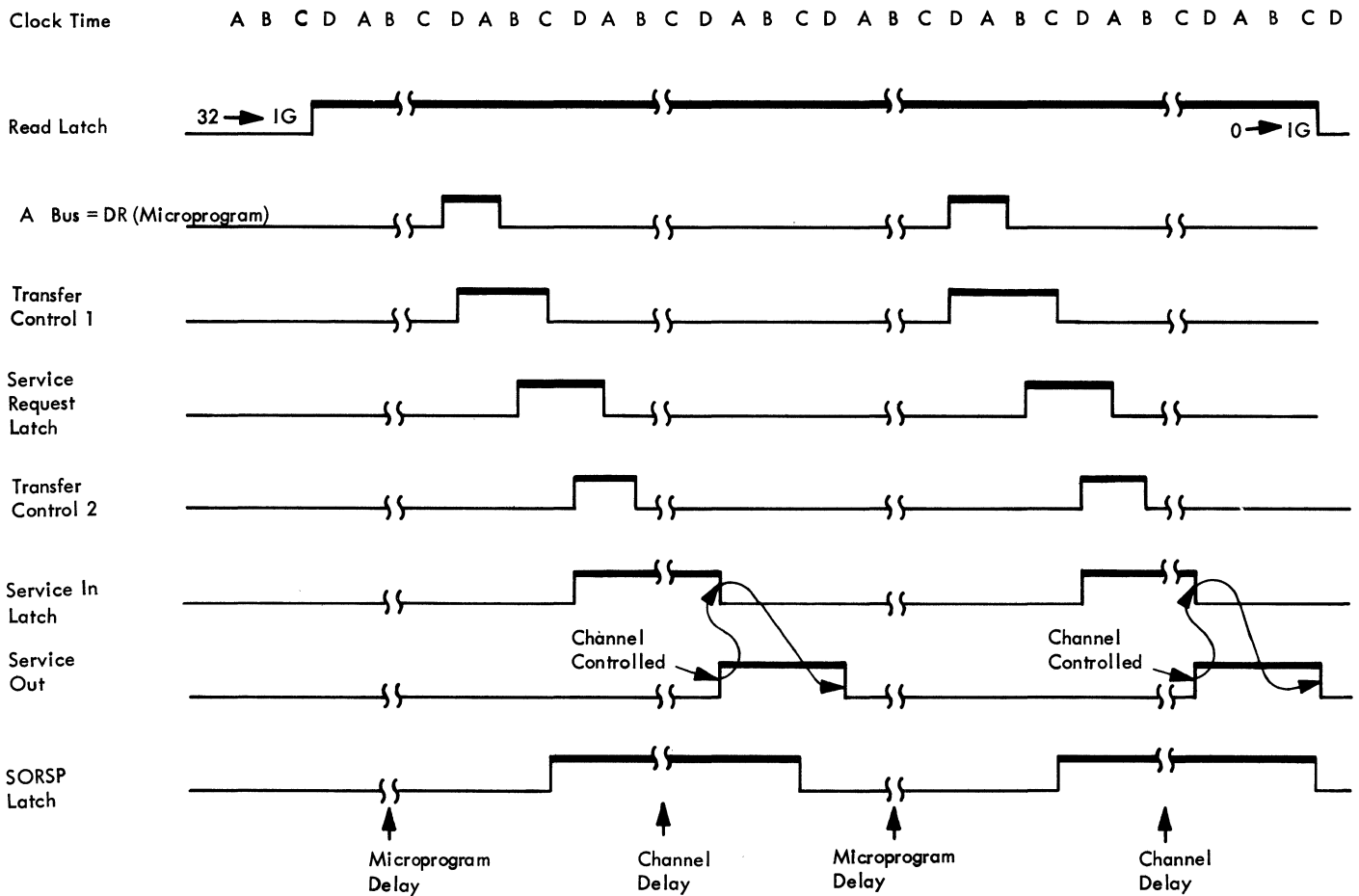
1. Data transferred to channel - read or sense.
2. Data transferred to the 2841 - write, search or control.

#### 2.7.2.1 Read Operation

1. The microprogram sets the read latch (Figures 2-34 and 2-35) with the ALU statement,  $32 \rightarrow IG$ .
2. When a byte of data is ready for transfer to the channel, the microprogram issues the ALU statement  $DR \rightarrow DW$  (DR is placed on the A bus).
3. This statement sets DW (bus in) with the byte of data and allows transfer control 1 FL to turn on at the following D time.
4. The service request latch turns on the following B time raising SORSP. SORSP is tested by the microprogram. In a read operation, it means that the channel has not yet responded to service-in with service-out.
5. The transfer control 1 FL is turned off at C time.
6. The transfer control 2 FL is turned on at D time.
7. The transfer control 2 FL turning on and not-service-out cause the service-in latch to be turned on, raising the service-in line to the channel.
8. The service-request latch is turned off at A time. SORSP is held up by the service-in latch.
9. The transfer control 2 FL is turned off at B time.
10. The channel responds with the service out line. (The byte has been transferred to the channel.)
11. The service-in FL is turned off by the service-out line.
12. The SORSP latch is turned off at C time. This indicates to the microprogram that the byte has been transferred to channel.
13. The microprogram and the service in/out controls repeat steps 2-12 for each byte.
14. When the microprogram is finished with the read operation, it turns off the read latch with the ALU statement  $0 \rightarrow IG$ .

#### 2.7.2.2 Write Operation (Figures 2-34 and 2-36)

1. The microprogram turns on the write latch with the ALU statement  $128 \rightarrow IG$ .
2. The service-request latch is turned on.



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Figure 2-35. Service In/Out Timing for Read and Sense Operations

3. The transfer control 2 FL turns on at the following D time.
4. Transfer control 2 FL and not-service-out set the service-in latch, raising the service-in line to the channel.

NOTE: The 2841 has requested a byte of data. The SORSP line is down and stays down until the channel raises the service-out line indicating a byte of data on the bus-out lines.

5. The channel raises the service out line.

NOTE: If the channel raises the command-out line instead of the service-out line, the microprogram recognizes this and resets the service-in latch with a ER → D ALU statement.

6. The SORSP latch turns on at the following C time.
7. The microprogram recognizes SORSP and performs the ALU statement, IH → register x. The byte of data is now stored within the 2841.

8. The transfer control 1 FL turns on the following D time.
9. The service-in latch is turned off the following A time dropping the SVC-request P1 line.
10. The SORSP latch turns off the following C time.
11. The transfer control 1 FL turns off the following C time.
12. Steps 2-11 are repeated for each byte of data.
13. When the write operation is finished, the microprogram turns off the write latch with the ALU statement 0 → IG.

### 2.7.3 Ending Sequence

- The ending sequence is used to present an ending status byte to the channel, and to disconnect from the channel (Figure 2-34).

The ending sequence is as follows:

1. The microprogram places the ending status byte in the DW register.

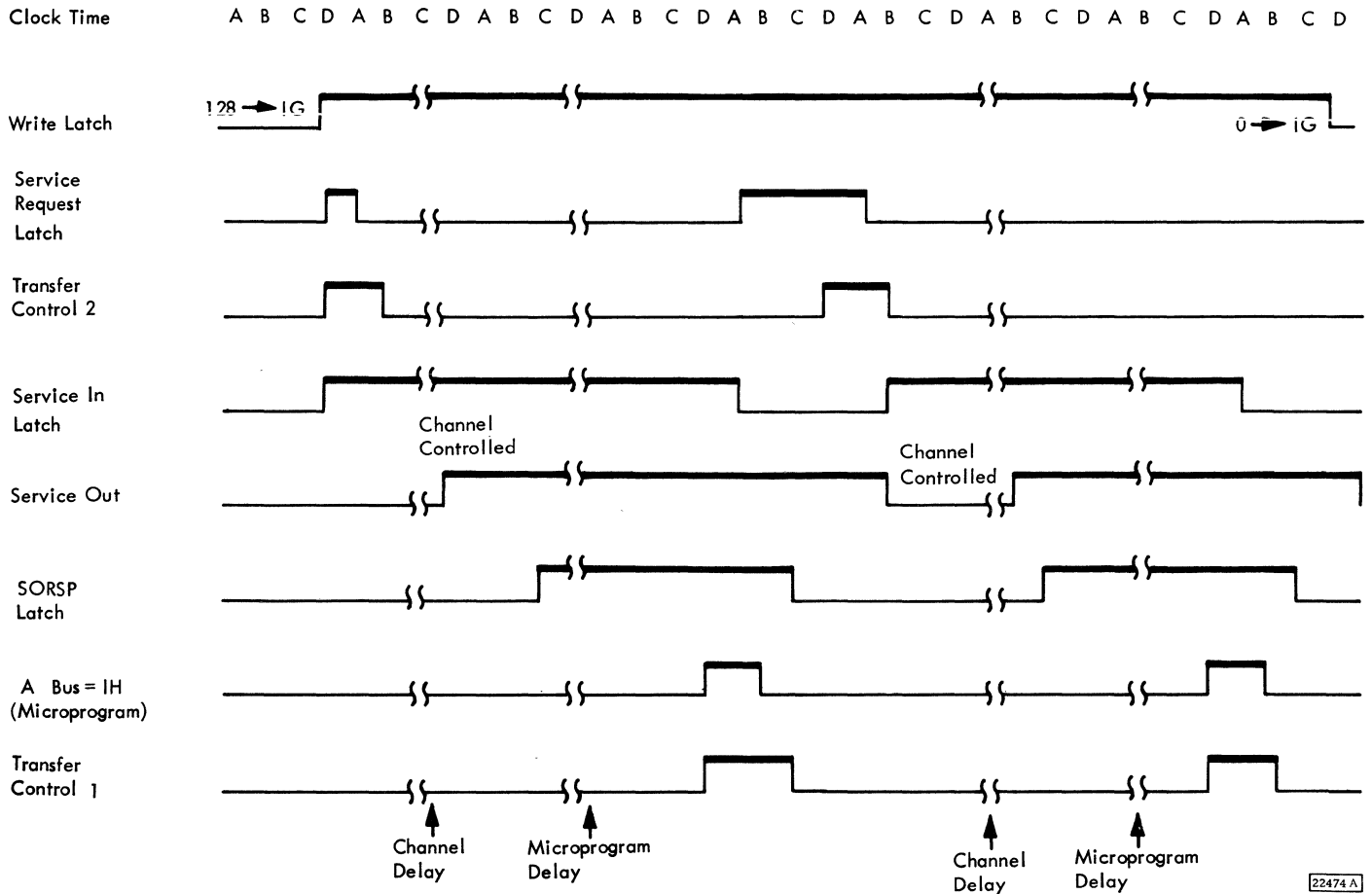


Figure 2-36. Service In/Out Timing for Write, Search, and Control Operations

2. The microprogram raises the status-in line with the ALU statement 4 → IG (D Bus, bit 5).
3. Channel responds with the service-out or command-out lines.
4. The microprogram drops the status-in line with the ALU statement 0 → IG.
5. The microprogram waits for the select-out line to fall (SELTO).
6. The microprogram turns off the Operational-In FL with the ALU statement 64 → IG (D Bus, bit 1).

#### 2.7.4 Short Control Unit Busy Sequence

The short control busy sequence indicates control-unit-status to the channel without going through the initial selection sequence (Figure 2-36).

- It is used when the 2841 is addressed with a new start or test I/O command and the 2841 is busy.

- If addressed while busy, the 2841 performs a polling interrupt sequence when it goes not busy. Control-unit-end is indicated in the status byte.

**Definition:** Indicates control-unit-status to the channel without going through the initial selection sequence. Presents the status-in line in response to the address-out line.

The short-control-unit-busy sequence is used by the 2841 in the following situations:

1. No chaining, and
2. The last command in the chain was a write, and
3. Channel-end and device-end have been transferred to the channel, and
4. Write gate or erase gate is on, and
5. A start or test I/O instruction is given to the 2841.

NOTE: During write-key-data and write-data operations, erase-gate is on for approximately 60  $\mu$ secs after channel-end and device-end were presented to the channel.

During write-HA, R0, CKD operations, write gate is on to index. Erase gate is on for approximately 60  $\mu$ secs past index.

Operation: (Figure 2-34)

1. After dropping the operational-in line at the end of a write command, and the program is not chaining, the 2841 sets the status-in latch. Status-in is not sent to channel since the Operational-in line is down.
2. The not-operational-in line and the status-in latch on raise the ER bit 7 line.
3. At this time, ER register, bit 7 is held reset.

NOTE: Assume the 2841 is addressed while busy.

4. The not-select-out line and the address-compare line turn on the steering-latch-A FL.
5. The channel raises the select-out line which brings up the responding-on-A line and blocks the reset to the ER register bit 7 FL to bring up the disc + busy line.
6. The disc + busy line brings up the CU-busy-status line and turns on the CU-end-A FL. The CU-busy-status line brings up the status-in line to the channel.
7. The CU-end-A FL brings up the Error 3 line and bits 1, 3, and parity of bus-in to the channel (status modifier, and busy bits).

NOTE: The 2841 does not go through the normal initial selection sequence.

8. The channel drops the select-out and address-out lines and turns off the steering-latch-A FL.
9. The steering-latch-A FL off drops the responding-on-A, and CU-busy-status lines. (status in drops)
10. The turn off of the responding-on-A line causes the ER register, bit 7 latch to turn off.

The only latch not in its original condition after this operation is the CU-end-A FL. When the microprogram finishes with the write operation, it tests ER register, bit 3. If ER register, bit 3 is on, the microprogram sets up to take a control-unit-end-polling-interrupt.

### 2.7.5 Halt I/O Instruction

- The halt I/O instruction causes the 2841 to release the channel immediately.
- The operation in progress continues to its ending point.
- When the operation in progress is finished, the 2841 initiates a polling-interrupt-sequence.

The halt I/O instruction causes the 2841 to release the channel immediately, stopping the transfer of data (Figure 2-34). The operation in progress when the halt I/O was given proceeds to its ending point.

When the operation reaches its ending point, the microprogram initiates a polling-interrupt-sequence.

#### 2.7.5.1 Halt I/O Sequence

Assume some operation in progress. Therefore, operational-in is up.

1. The channel drops the select-out line (may already be down on multiplexer channels).
2. The channel raises the address out line.
3. The ER register, bit 7 latch is turned on.
4. Operation-in to channel is degated by the disc + busy line.
5. Command-out is forced up within the 2841.
6. This completes the halt I/O line sequencing to channel.

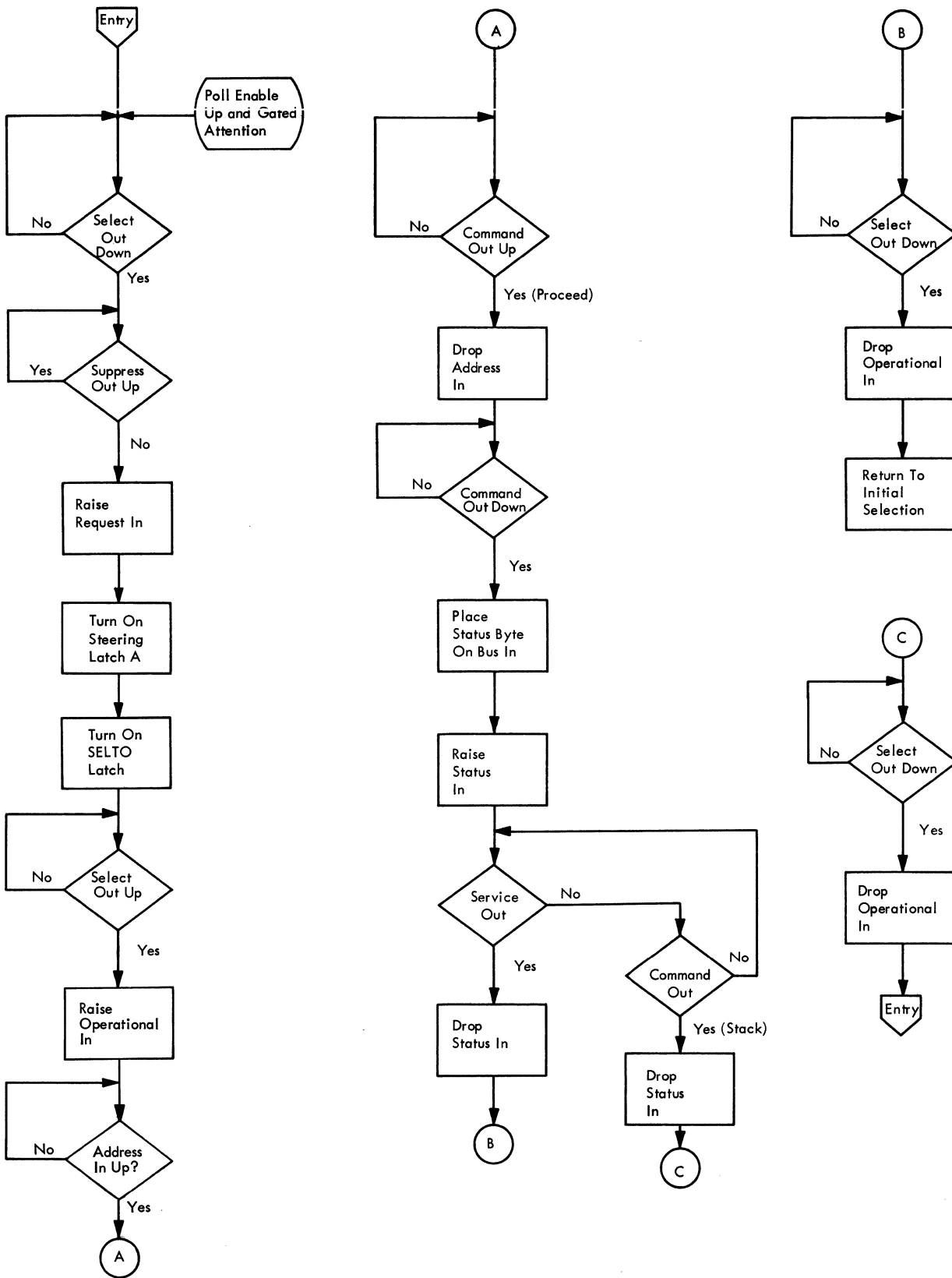
Command-Out is forced up so that the microprogram can branch on it. This normally means that the channel's byte count has gone to zero and tells the 2841 to stop the data transfer. However, the microprogram also finds ER register, bit 7 on. This indicates halt I/O to the microprogram and causes the microprogram to reset operational-in.

Operational-in dropping turns the ER register bit 7 latch off causing command-out to drop within the 2841.

If the 2841 is not working on any command when the halt I/O is given, the 2841 will ignore the halt I/O.

### 2.7.6 Polling Interrupts

- A polling interrupt is a means of connecting the 2841 to the channel without giving a start or test I/O command (Figures 2-34 and 2-37).



22475A

Figure 2-37. Channel and 2841 Interface Polling Interrupt Sequence

- The sequence is normally used to present a status byte after the channel and the 2841 have disconnected.
- A channel can tell the control unit to hold (stack) the interrupt by raising the command-out line in response to the status in-line.

#### 2.7.6.1 Polling Interrupt, Definition

Polling interrupt is a means of connecting the 2841 to the channel and of presenting an outstanding status byte without the channel giving a start or test I/O command to 2841.

#### 2.7.6.2 Polling Interrupt Routine

The 2841 uses the polling interrupt sequence in the following command word sequences to present outstanding status information to the channel.

1. Not chaining - A seek command to a different cylinder or a restore command is given. Channel-end is presented to the channel. The channel and the 2841 disconnect. Device-end is still outstanding. The microprogram turns on the poll enable latch. When gated attention occurs, a polling interrupt sequence is initiated to present a device-end status byte to the channel.
  2. The 2841 is addressed with a new start or test I/O command while busy (after a write command). The 2841 indicates control-unit-busy to the channel on the start or test I/O. When the 2841 goes not-busy it initiates a polling interrupt sequence with control-unit-end in the status byte.
  3. A halt I/O is given to the 2841 while it is operating on some command. The 2841 disconnects from the channel. When the original command reaches its logical ending point, a polling interrupt is initiated with the applicable status information in the status byte.
  4. Not chaining - The 2841 has presented channel-end and device-end after a write command. Write gate or erase gate is up because the field has not been completed. The 2311 drive goes inoperable for some reason (not ready, not on line or unsafe, etc.). The 2841 initiates a polling interrupt sequence with the control-unit-end and unit-check bits on in the status byte.
5. Assume:
    - a. Multiplexer channel.
    - b. Cylinder seek or restore command.
    - c. Command word chaining.
    - d. Channel-end presented to the channel.
    - e. Select-out line from the channel is down. The 2841 then drops the operational-in line, disconnecting from channel. The microprogram sets the IG-6 latch so that any gated-attention can raise request-in, thereby initiating a polling interrupt sequence with device-end in the status byte. During the time between channel-end and device-end, the channel has kept the suppress-out line up. This prevents any other control unit from initiating a polling interrupt. Note that when request-in is raised by means of IG-6 and gated-attention, the suppress-out line from the channel cannot suppress the polling interrupt request. This is the only type of 2841 polling interrupt that cannot be suppressed by the channel.
  6. Changing a 2311 from not-ready to ready initiates a polling interrupt sequence with device-end in the status byte.

#### 2.7.6.3 Stacked Status

Definition: When the channel brings up the command-out line in response to the status-in line, the 2841 must hold (stack) the status byte.

The channel and the 2841 disconnect. The 2841 attempts to transmit this stacked status byte to the channel by means of the polling interrupt sequence.

#### 2.7.7 Resets

##### General Reset

The channel is able to reset all on-line control units by dropping the operational-out line and not raising suppress-out line. This provides a general reset to the 2841 (Figure 2-34). All registers are reset and the microprogram restarts in TROS address zero.

##### 2.7.7.1 Selective Reset

The channel issues a selective reset by raising the suppress-out line and dropping the operational-out line (Figure 2-34). If the 2841 has operational-in up, all 2841 registers are reset (with the exception of

ST(7), reset on) and the microprogram restarts in TROS address zero.

An example of why the channel might issue a selective reset follows:

Assume: ROS error in the 2841 while not selected to channel.

A ROS error stops the microprogram and attempts to set the operational-in latch. When channel next addresses the 2841, initial select rises, setting the operational-in latch. No other lines are raised on the interface. The channel decides that something is wrong with one of the control units. Some channels may attempt a halt I/O routine first. Note that ROS error stops the ER register, bit 7 from being turned on; therefore halt I/O does nothing within the 2841 (operational-in is still on).

Eventually the channel gives a selective reset. This resets the error condition, drops operational-in, and allows the microprogram to begin operating at TROS address zero.

## 2.8 CE PANEL

- Allows Customer Engineer control of 2841 operations (Figure 2-38).
- Displays error checks.
- Displays read only storage address register.
- Displays A register output.
- Displays BX, BY, DH, DL, DR, DW, FR, GL, GP, KL, OP, UR, ST, ER, and SW registers by reading them into the A register.
- Allows setting of a byte of data into a selected register.
- Allows stopping on errors.
- Can stop at a preset address.
- Can start the microprogram at a preset address.
- Provides for single microprogram step operation.
- Provides a sync pulse at a preset address.
- Provides for recycling between two microprogram addresses.
- Provides for local power control.

### 2.8.1 CE Switches

#### 2.8.1.1 Normal/CE

The normal/CE switch in the NORMAL (on line) position allows power sequencing and signals from the

using system to control the 2841. The normal/CE switch in the CE (local) position degates signals to and from the using system if the enable-disable switch is in DISABLE. Power control is then under control of the 2841 power on/off switch. If the enable-disable switch is in ENABLE, the 2841 is in CE on line mode.

#### 2.8.1.2 Lamp Test

When pressed, in either CE or normal mode, lights all lamps.

#### 2.8.1.3 Interface Degate

When transferred drops power to the selection relay and blocks all in lines to the channel and turns off usage meter.

#### Caution:

Operating the interface degate switch out of the proper sequence can cause CPU problems.

### The Following Switches are Active Only in CE Mode.

#### 2.8.1.4 Register Select

Allows selection of certain registers for display or data entering.

#### 2.8.1.5 Display

Displays the selected register data in the A register lamps. The contents of the selected register are displayed only as long as the display button is pressed.

#### 2.8.1.6 Enter

Enters data, stored in the two low order start address switches, into the selected register.

#### 2.8.1.7 Set ADDR

Places the address contained in the start address switches into the W and X registers.

#### 2.8.1.8 Check Reset

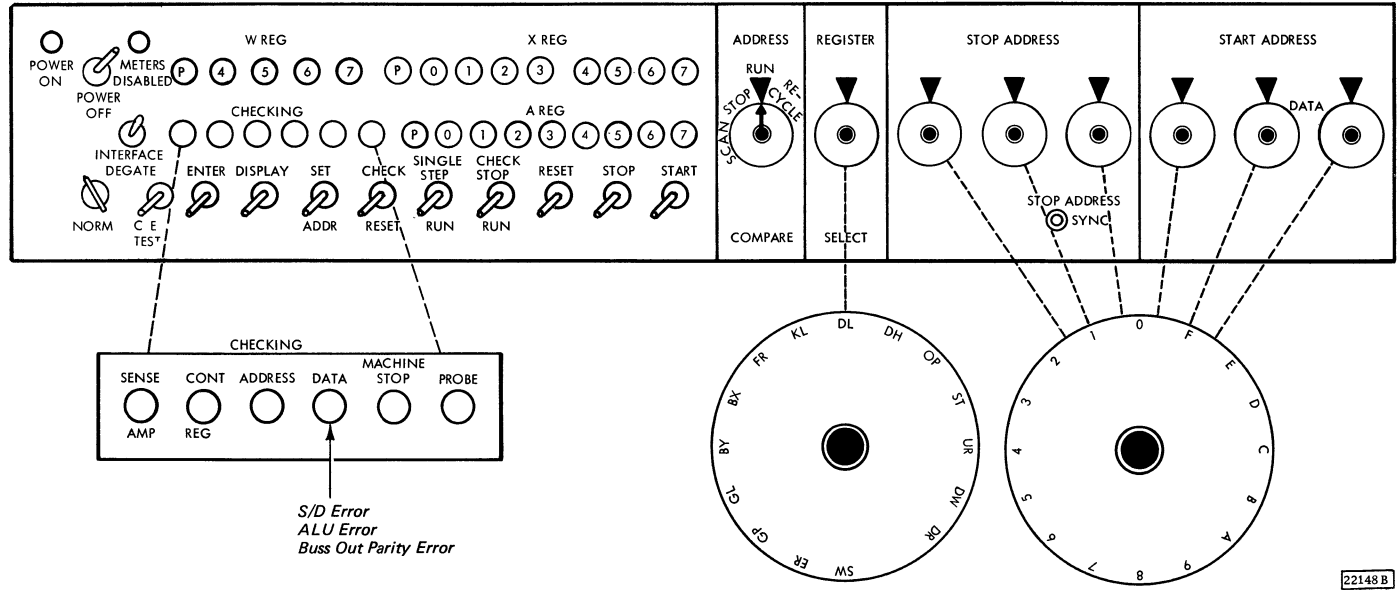
Resets sense amplifier, control register, address, and data check indicators.

#### 2.8.1.9 Reset

Resets all indicators and registers.



Figure 2-38. CE Panel



22148 B

#### 2.8.1.10 Stop

The sense latch reset and sense strobe lines are inhibited. The TROS continues to cycle internally. The 2841 is functionally stopped.

#### 2.8.1.11 Start

Starts TROS at the address sitting in the W and X registers.

#### 2.8.1.12 Single Step

Operate TROS for one machine cycle each time the start switch is pressed.

#### 2.8.1.13 Check Stop/Run

Check Stop Position - causes TROS to stop on a sense amplifier, control register, address, or data check error. The probe latch can also be jumpered into this circuit in order to stop the 2841 at a given point in the microprogram.

Run - Machine does not stop on errors. In normal mode TROS stops for four error conditions:

1. Sense Amplifier.
2. Control register.
3. Address.
4. Data Check (ALU - ER 4 bit).

#### 2.8.1.14 Address Compare

Run: The microprogram runs to its own ending point.

Stop: The microprogram runs to the address set in the stop-address switches.

Recycle: The microprogram runs to the address set in the stop-address switches. It then restarts at the address set in the start-address switches.

**NOTE:** Do not recycle on scan words, 004, 100, 200, etc.

Scan: A position of the switch, used in conjunction with micro diagnostic statements ( $GP + 0 + 1 \rightarrow GP, A \rightarrow X$ ), which allows one TROS module's 256 words to be read out repetitively for parity checking by the ROS parity checking circuits.

#### 2.8.1.15 Start Address

Two functions:

1. The two low order switches are used as a data source. When the enter switch is pressed, the selected register is loaded.
2. All three switches are used as a starting address for the microprogram. The switch output is loaded into W and X registers when the set-address switch is pressed.

#### 2.8.1.16 Stop Address

The Stop-address switch is used in conjunction with the address-compare switch to control the sequence of the microprogram. When the microprogram stops at the stop-address switch setting, that address has not yet been read out of TROS.

**NOTE:** The stop-address-sync hub furnishes a negative going pulse in either CE or normal mode. The sync pulse is 325 ns in duration. The sync pulse starts at D time of the cycle where the contents of the W and X registers are the same as the address in the three stop address switches. This sync pulse is useful in tracing an operational CAS microprogram through the CLD's.

### 2.8.2 CE Indicators

The W, X and A registers are normally displayed. In CE mode, the A register can be loaded with a selected register by pressing and holding the display switch.

#### 2.8.2.1 Sense Amp

When on, indicates a parity error in CA, CA Alt., CB, CK, CH, CL, PA, or PS control fields. Refer to 2.4.13 TROS Sense Amplifier Check.

#### 2.8.2.2 Control Register

When on, indicates a parity error in CV, CS, CD, CD Alt., CC, BP, or PC control fields. Refer to 2.4.14 TROS Control Register Check.

#### 2.8.2.3 Address

When on, indicates a parity error in X register P bit, W register P bit, CN, PN, or PA TROS fields. Refer to 2.4.12 TROS address check.

#### 2.8.2.4 Machine Stop

When on, indicates that the microprogram has stopped. The machine clock and TROS continue to run. The contents of the TROS sense amplifier latches (SALs) are frozen. The W and X registers display the next microprogram address that would have been executed.

#### 2.8.2.5 Probe

The probe indicator is used as a diagnostic tool. See check-stop/run switch.

#### 2.8.2.6 Data

The data indicator is on for three reasons:

1. Serial write data error.
2. Bus out parity error.
3. ALU error is developed when a bypass ALU statement is used and A register parity does not agree with ALU parity. ALU error also turns on the machine stop indicator in normal mode, or in CE mode if the check-stop/run switch is in the CHECK STOP position.

#### 2.8.2.7 Meters Disabled

Lights when both the channel A and channel B 'meter enabled' latches are off.

### 2.9 CAS MICROBLOCK

- 48 bits are read from TROS each 500 nanoseconds (ns).
- The 48 bits form one TROS word (bits 0-47).
- SAL 44 (TROS bit 47) is not used.
- The word is divided into 15 fields.
- Collectively, the fields define the 2841 operation for the next 500 ns.

48 bits are read out of the TROS array every 500 ns and are called a TROS word. The word is divided into 15 fields. Collectively, these fields define the operation of the 2841 for the next 500 ns.

This section of the manual defines these fields, shows how they are represented in a microblock, and includes a sample usage of several microblocks to perform a logical function (Seek).

#### 2.9.1 TROS Bit Assignment Chart

The TROS word is divided into 15 control fields (Figure 2-39). Each one of these fields performs a particular function during one machine cycle. A description follows:

#### 2.9.1.1 CN

The value contained in CN is loaded into the six high order bits of the X register. In addition, CN-5 is used as the data source when loading the FT register and FC register.

#### 2.9.1.2 PN

PN is a parity bit for the CN and PN fields. Total parity should be odd.

#### 2.9.1.3 CD

The value contained in this field gates the output of ALU (A register if bypass bit on) to one of seventeen destinations (i.e.,  $7 \rightarrow DH$  would gate the output of ALU to the DH register).

NOTE: Even though the data was loaded into a register, it is still on the D bus and can be tested by the microprogram.  $A + B \rightarrow D$  means to place the output of ALU on the D bus only.

#### 2.9.1.4 CV

The value contained CV determines if the B entry is gated in true or ones complement form to ALU.

#### 2.9.1.5 CC

The value contained in CC determines the ALU operation. There are eight different ALU statements. Five different symbols are used to indicate the arithmetic operation:

- + Add positive
- Complement add/subtract
- . AND
- $\Omega$  OR
- $\nabla$  Exclusive OR

CC=0: Add or subtract (CV) the A and B entry inputs. Carry In of zero to the low order ALU position. Example:  $KL+BY+0 \rightarrow DH$

CC=1: Add or subtract (CV) the A and B entry inputs. Carry In of one to the low order ALU position. Example:  $KL+BY+1 \rightarrow DH$

CC=2: AND the A and B entry inputs. Example:  $KL \cdot BY \rightarrow DH$

Figure 2-39. TROS Bit Assignment Chart

TROS Tape (SAL Bit)	19	21	23	25	27	29	31	33	35	37	39	41	43	45	09	11	13	15	01	03	05	07	47	42	00	02	04	06	08	10	12	14	16	18	20	22	24	26	28	30	32	34	36	38	40	17	46	44					
Word Bit Position	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47					
Field Name	CA Field				CB	CK Field								CL Field				CH Field				PA	PS	CN Field					PN	CD Field				CD <sup>A</sup>	CV	CC				CS				PC	CA <sup>A</sup>	BP	-						
Field Bit Position	1	2	3	4	0	1	0	1	2	3	4	5	6	7	-	-	-	-	-	-	-	-	0	0	0	1	2	3	4	5	0	0	1	2	3	0	0	1	2	0	1	2	3	0	0	0	-						
Binary Value	8	4	2	1	2	1	128	64	32	16	8	4	2	1	-	-	-	-	-	-	-	-	-	-	-	8	4	2	1	16	-	-	-	-	1	4	2	1	8	4	2	1	-	16	-	-							
Use	A Reg Entry				B Ent	W Reg or B Reg Entry								Branch X7				Branch X6				P	P	Next Address X0-5					P	Destination				ALU Control				ST Control															
	Normal	Alt																																																			
	None	SW			None																																																
16	0	GL	Stop	BY																																																	
17	1	BY		CK																																																	
2		BX		DR																																																	
3		FR																																																			
4		KL																																																			
5		DL																																																			
6		DH																																																			
7		OP																																																			
8		GP																																																			
9		UR																																																			
10		DW																																																			
11		DR	SC																																																		
12		ER	FS																																																		
13		IE	OA																																																		
14		IH	IS																																																		
15																																																					

- NOTE 1 DNST21 says set ST2 to 1 if D bus is non-zero. ST2 is never set to zero by this statement.
- NOTE 2 File branching is a hardware decode of the IE register; Where CH.CL 00 = 2302, 01 = 2311, 10 = 2303, 11 = 2321.
- NOTE 3 PA is parity bit for address of the word reading out PA.  
 PS is parity bit for CA,CB,CK,CL,CA ALT, PA,CH  
 PC is parity bit for CD,CD ALT, CV,CC,CS,BP  
 PN is parity bit for CN.
- NOTE 4 BP is set by bypass statement in line 3 of microprogram box. It Activates the ALU checking circuits.
- NOTE 5 CC decode of 4,5 or 6 sets ST3 with carry out (DC).  
 CC decode of 6 sets carry in with contents of ST3 (+C).

22391C

CC=3: OR the A and B entry inputs. Example:  
KLΩBY→DH

CC=4: Add or subtract (CV) the A and B entry inputs. Carry In of zero to the low order ALU position. If there is a Carry Out of the high order ALU position, set ST(3). Example: KL+BY+0→DHC

CC=5: Add or subtract (CV) the A and B entry inputs. Carry In of one to the low order ALU position. Carry Out, set ST(3). No Carry Out, reset ST(3). Example: KL+BY+1→DHC (C means set ST(3)).

CC=6: Add or subtract (CV) the A and B entry inputs. Use the present condition of ST(3) as a Carry In to the low order position of ALU. If there is a Carry Out, set ST(3). No Carry Out, reset ST(3). Example: KL+BY+C→DHC

CC=7: Exclusive OR the A and B entry inputs. Example: K~~Ω~~BY→DH

#### 2.9.1.6 CS

The value contained in this field controls the setting and resetting of individual bits in the status register; i. e., CS=6 (DN ST 21) means if the D bus does not equal zero set ST(2) to a one. The only way to turn ST(2) off is with a CS=5 (0→ST2) statement.

#### 2.9.1.7 PC

PC is the parity bit for CV, CS, CD, CD Alt., CC, BP and PC fields. Total parity should be odd.

#### 2.9.1.8 PS

PS is the parity bit for CA, CA Alt., CB, CK, CH, CL, PA and PS fields. Total parity should be odd.

#### 2.9.1.9 BP

The value contained in BP determines whether the ALU or A register output is placed on the D bus. With this bit on, a parity check of the A register P bit and the ALU generated P bit is made. An error stops the 2841 with the data-check lamp on. Example: KL+0→DH, BYPASS.

#### 2.9.1.10 CH

The value contained in CH (hex) allows a particular condition in the machine to be tested. X register bit

6 is set or reset depending upon the result of the test. A summary of CH branching conditions follows:

CH=0: Set X 6 off.

CH=1: Set X 6 on.

CH=3, D, E, or F - Test am OP register bit. If it is on, set X 6. If not, reset X 6.

CH=2, 4, 5 or 6 - Test a ST register bit. If it is on, set X 6. If not, reset X 6.

CH=7: Test 2321 Interface selected. If it is on, set X 6. If not reset X 6.

CH=8: Reset X 6. Gate bits, 3, 4, 5, 6, and 7 of the CK field to the W register if the microblock contains a CK→W statement.

CH=9: Test the ALU carry out latch. If on, set X 6. If not, reset X 6.

CH=A: Test command-out. If on, set X 6. If not, reset X 6.

CH=B: Test suppress-out. If on, set X 6. If not, reset X 6.

CH=C: Not used.

#### 2.9.1.11 CL

The value contained in CL (hex) allows a particular condition in the machine to be tested. X register bit 7 is set or reset depending upon the result of the test. A summary of CL branching conditions follows:

CL=0: Set X 7 off.

CL=1: Set X 7 on.

CL=2, 3, or 4: Test a ST register bit (3, 5 or 7). If on, set X 7. If off, reset X 7.

CL=5: Test the ALU, D=0 latch. If on, set X 7. If off, reset X 7.

CL=6: Do not gate CN 0-5 and the results of the CH and CL branch tests to the X register. Instead, gate

the contents of the A bus to the X register. This statement should be used only when the address compare switch is in SCAN, since it actually gives a 256-way branch.

CL=7: Test optional interface selected. If it is on, set X 7. If off, reset X 7.

CL=8: Test service-out. If it is on, set X 7. If off, reset X 7.

CL=9: Test service-out response. If it is on, set X 7. If off, reset X 7.

CL=A: Test select-out. If it is on, set X 7. If off, reset X 7.

CL=B, C, D, or F: Test an OP register bit. If on, set X 7. If off, reset X 7.

CL=E: Test for index. If index, set X 7, if not, reset X 7.

NOTE: Before index can be gated to the CL branching circuits, the microprogram must allow index by issuing the CS statement 1→ST1.

### 2.9.1.12 CA

The value contained in CA gates a particular source to the A bus, i. e. , CA=0 places zero on the A bus. CA=D places the contents of ER on the A bus.

CA=11, STOP, is a special use of the CA field. This statement is used in the microdiagnostics. Check stop/run switch in the CHECK STOP position and the stop statement stops the 2841. Refer to ALU microdiagnostic for examples of the stop statement.

### 2.9.1.13 CB

The value contained in CB gates a particular source to the B Bus, i. e. , CB=0 places zero on the B bus. CB=3 places the contents of DR on the B bus.

### 2.9.1.14 CK

The value in the CK field is used as a constant data source by the microprogram, i. e. , KL+9→DL. The nine is in the B entry position in the ALU statement. To gate CK to the B bus, it is necessary to make the CB field equal 2.

Bits 3, 4, 5, 6, and 7 may also be gated to the W register for module switching in TROS. This is accomplished by making the CH field 8 and issuing a

CK→W (i. e. 3→W) statement. CK 3 is used as W register parity bit.

### 2.9.1.15 PA

PA is the parity bit for the combined W and X registers.

W					X							Hex address 58B ↓	
P	4	5	6	7	P	0	1	2	3	4	5		6
1	0	1	0	1	1	1	0	0	0	1	0	1	1

The sum of the bits is even. Therefore, PA is punched for an output of one from TROS tape.

### 2.9.2 Microblock Symbology

- The microblock is divided into eight lines of information (Figure 2-40).
- Each line identifies a particular function of the machine.

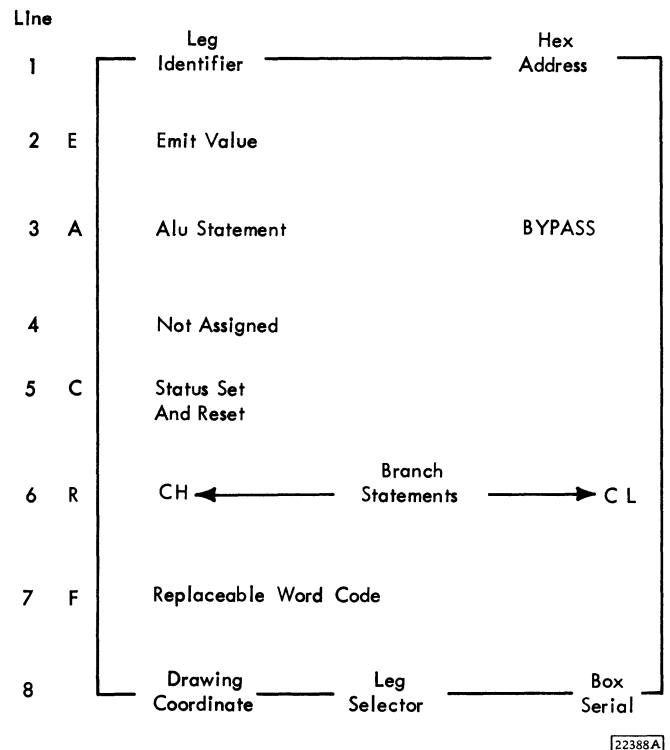


Figure 2-40. CAS Microblock

2.9.2.1 Line 1

Line 1 contains a leg identifier and the hexadecimal address of the microblock.

The leg identifier consists of two characters which are indicative of the setting of X register, bits 6 and 7 for this block. Valid symbols and their meanings follow:

- 0 Appropriate X bit is off
- 1 Appropriate X bit is on
- X Setting of appropriate X bit is not shown in leg identifier.

The hexadecimal address consists of three digits. The first one represents the value set in the W register. The other two represent the value set in the X register.

2.9.2.2 Line 2

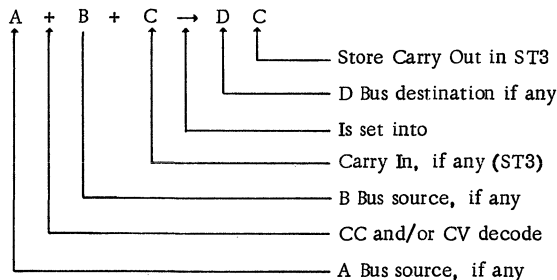
Line 2 contains an emit value. This represents a binary picture of the CK field when the CK field is used in ALU statements. It is identified by an E on the left side of the microblock, i. e.,  $KL+29 \rightarrow BY$ ; emit value = 00011101.

2.9.2.3 Line 3

Line 3 contains the ALU statement. It is identified by an A on the left side of the block. A summary of the line ALU arithmetic symbols follows:

- + Add Positive
- Complement Add/Subtract
- AND
- $\Omega$  OR
- $\nabla$  Exclusive OR

Symbolic ALU Statement:



A summary of the eight ALU statements follows. The DH, KL, and BY registers are used in the examples.

CC Decode

- 0  $KL \pm BY \rightarrow DH$
- 1  $KL \pm BY + 1 \rightarrow DH$
- 2  $KL \cdot BY \rightarrow DH$  or  $KL \cdot -BY \rightarrow DH$
- 3  $KL \Omega BY \rightarrow DH$  or  $KL \Omega -BY \rightarrow DH$
- 4  $KL \pm BY \rightarrow DHC$
- 5  $KL \pm BY + 1 \rightarrow DHC$
- 6  $KL \pm BY + C \rightarrow DHC$
- 7  $KL \nabla BY \rightarrow DH$  or  $KL \nabla -BY \rightarrow DH$

Line 3 also contains the BYPASS statement.

2.9.2.4 Line 4

Line 4 is not presently used.

2.9.2.5 Line 5

Line 5 contains the status register set/reset statement. The line is identified by a C on the left side of the microblock.

The status set/reset statement, if any, takes the format shown in the bit assignment chart (Figure 2-39).

2.9.2.6 Line 6

Line 6 is used for the branching test statements. It is identified by an R on the left side of the microblock. Refer to the bit assignment chart (Figure 2-39) for the conditions which may appear in this area.

NOTE:  $CK \rightarrow W$  statement appears in the CH position. It causes X register 6 to be reset.

2.9.2.7 Line 7

Line 7 contains replaceable word code information. The line is identified by an F on the left side of the block.

The replaceable word code is defined as follows: Every announced feature is assigned a code number, starting with 1 and progressing to 999. The basic machine has no number assigned.

When a location in the ROS is used by more than one option (basic or feature), each definition of the word, as shown by a CAS logic block, must contain the code of the feature which requires the word. If two or more features require the installation of the same word, all the feature numbers must appear in the block, with a comma (,) to indicate AND or a slash (/) to indicate OR. Only one type of symbol can appear in a block.

If a ROS word location is not assigned a basic or feature use, or is assigned only to a feature and the feature is not installed, the contents of that location is zero with correct parity in all fields, and the next address (CN field) is its own physical address.

**Examples:**

- F = 4,            Indicates that this word is installed if feature 4 is installed.
- F = 1, 2, 6.    Indicates that this word is installed only if feature 1 and 2 and 6 are installed at the same time.
- F = 1/2/12.    Indicates that this word is installed by either feature 1 or 2 or 12 or any combination of them.

**Initial replaceable word code assignment:**

2302	1
2321	2
2303	3
Additional Storage	5
File Scan	6
Record Overflow	7
2 Channel Switch	8

**2.9.2.8 Line 8**

Line 8 contains a drawing coordinate, leg selector, and box serial designation.

The drawing coordinate and box serial designation are used mainly by engineering and design automation in physically locating the blocks on a CAS sheet.

The leg selector consists of two or three characters. If there are three, the first one (leftmost) represents the condition of CN-5. It is used as a data input to the FT and FC registers, and is always a one or a zero.

The other two characters indicate X register, bits 6 and 7 settings for the next microblock. Valid characters and their meanings follow:

- 0    Set appropriate X bit to 0
- 1    Set appropriate X bit to 1
- X    Setting of the appropriate X bit is not shown in the leg selector (see C line)
- \*    Setting the appropriate X bit is under control of condition tested in CH or CL branching statement.

**2.9.3 Sample Usage of Microblocks**

This example (Figure 2-41) shows how several microblocks may be joined to perform a logical function.

Test B of the non-resident diagnostic module is used.

Test B restores and seeks head 00 from cylinder 00 to cylinder 198 and back. Test B also reads the HA at cylinders 00 and 198 to verify the seek operation.



Introduction to 2311 Diagnostic Test

(B) Seek/Restore. Head 00. From Cylinder 000 to Cylinder 198.

(1) This Program:

- (A) Returns the 2311 Access Arm to Zero.
  - (B) Reads and Checks Home Address.
  - (C) Seeks to Cylinder 198
  - (D) Reads and Checks Home Address.
  - (E) Repeats Step (A).
- (2) Install the C.E. Disk Pack on the 2311  
 (3) Place the Check Sw In Stop Position  
 (4) Place the Address Compare Sw In Run Position.

- (5) Press Reset Button.
- (6) Place All Files, Other Than The 2311 to be Selected. In Off Line Condition.
- (7) To Select the Desired Module Manually Set The Proper Bit Into The UR Register as Follows:

Module	Position	Data
0	0	080
1	1	040
2	2	020
3	3	010
4	4	008
5	5	004
6	6	002
7	7	001

- (8) Set Start Address Sw to .3A1 (QX260).
- (9) Press Set Address Button.
- (10) Press Start Button.
- (11) The Program May Be Stopped On Address 3A3 (QX250).
- (12) Index is Found In Word 032 (QX200).
- (13) Passing Through Word 060 (QX230) Means That the Byte of 14 in the Alpha Gap Preceding Home Address was Not Properly Read.
- (14) If Home Address is not Properly Read The Program will Stop On Either Word 0A9 or 0AA (QX300).

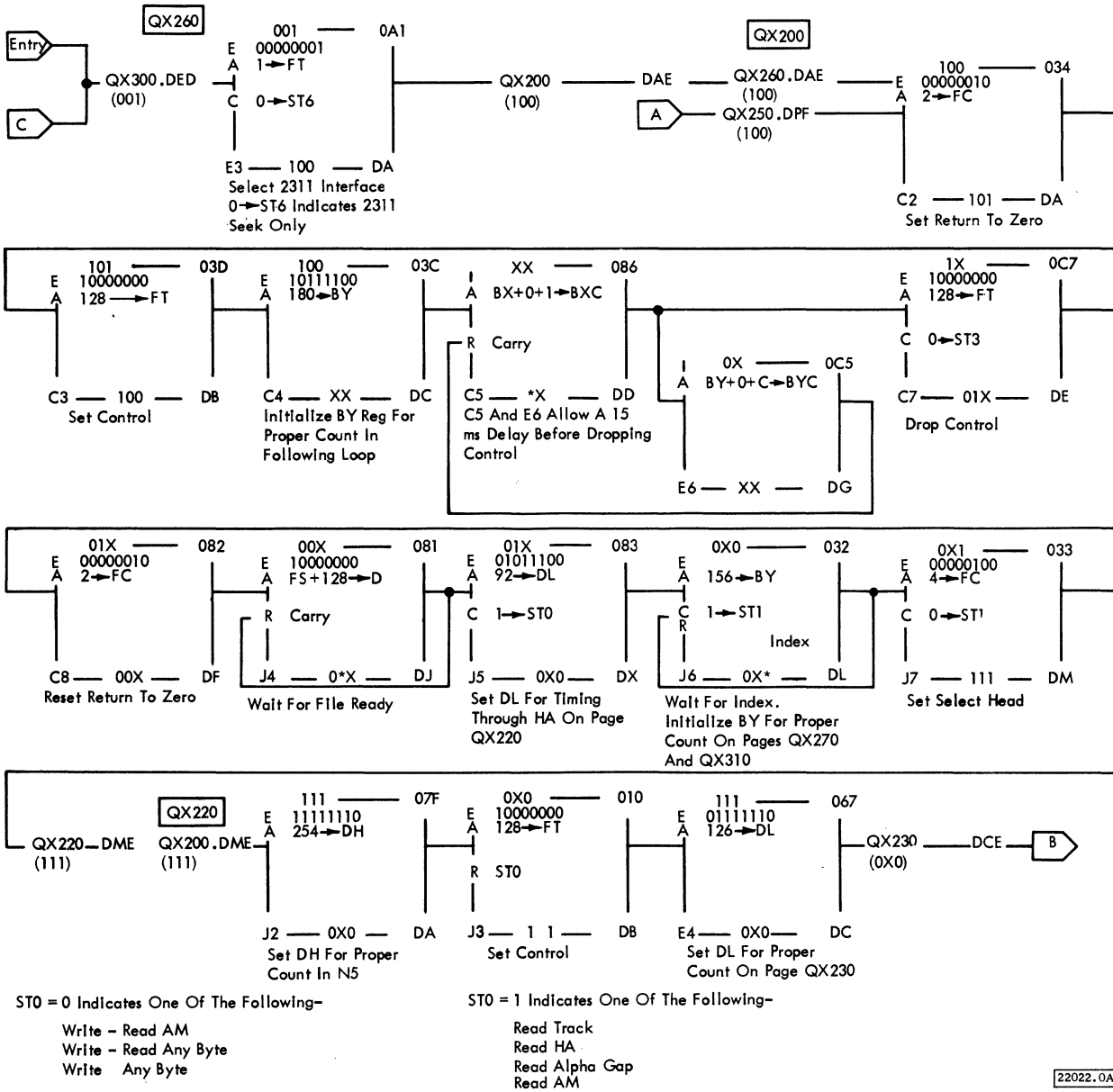


Figure 2-41a. Sample Usage of Microblocks

Introduction to 2311 Diagnostic Test

(B) Seek/Restore. Head 00. From Cylinder 000 to Cylinder 198.

(1) This Program:

- (A) Returns the 2311 Access Arm to Zero.
- (B) Reads and Checks Home Address.
- (C) Seeks to Cylinder 198
- (D) Reads and Checks Home Address.
- (E) Repeats Step (A).
- (2) Install the C.E. Disk Pack on the 2311
- (3) Place the Check Sw In Stop Position
- (4) Place the Address Compare Sw in Run Position.

(5) Press Reset Button.

- (6) Place All Files. Other Than The 2311 to be Selected. In Off Line Condition.
- (7) To Select the Desired Module Manually Set The Proper Bit Into The UR Register as Follows:

Module	UR Bit Position	Data Switches
0	0	080
1	1	040
2	2	020
3	3	010
4	4	008
5	5	004
6	6	002
7	7	001

(8) Set Start Address Sw to 3A1 (QX260).

- (9) Press Set Address Button.
- (10) Press Start Button.
- (11) The Program May Be Stopped On Address 3A3 (QX250).
- (12) index is Found in Word 032(QX200).
- (13) Passing Through Word 060 (QX230) Means That the Byte of 14 in the Alpha Gap Preceding Home Address was Not Properly Read.
- (14) If Home Address is not Properly Read The Program will Stop On Either Word 0A9 or 0AA (QX300).

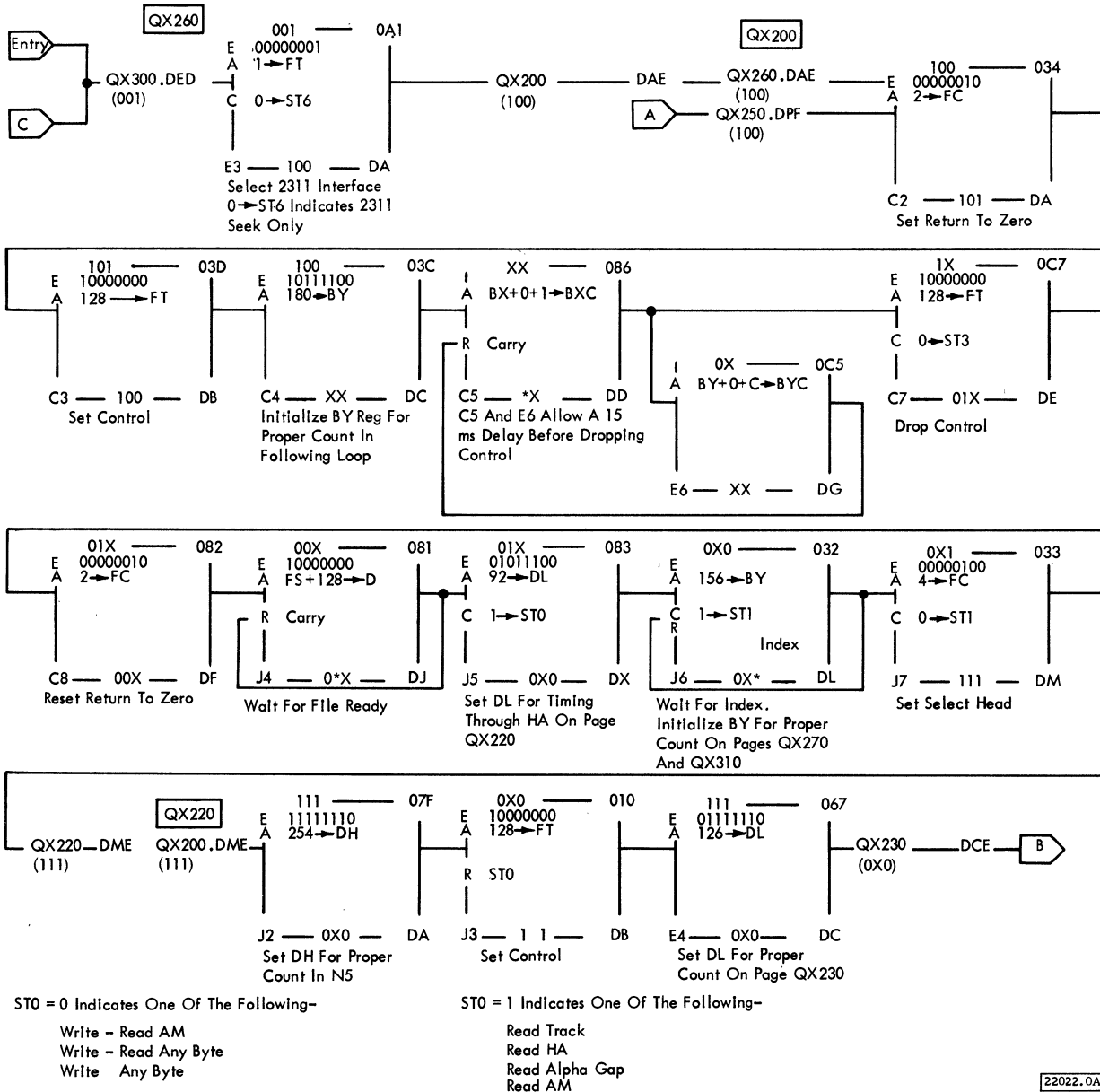


Figure 2-41a. Sample Usage of Microblocks

## 2.10 READING MICROPROGRAMS

The microprogram is a series of logical steps (instructions) used to control data flow and machine operations within and between machine elements of the 2841 Storage Control. Microprogram instructions are similar in function and purpose to the stored binary program instructions used by various digital computers. Unlike the stored binary program instructions for digital computers, which are stored in a read/write core storage, the microprogram instructions for the 2841 are stored in a transformer read-only storage (TROS) module. The TROS module is a combination of electronic circuits and programming.

The microprogram for the 2841 consists of a series of program routines similar in concept and function to the stored program routines for a digital computer. Each program routine performs a specific operation: reset, search, read, write, and so on. The program routines are divided into subroutines that alter the program routine. A subroutine can correct bad parity, sense machine conditions, modify the address to change routines or subroutines, and so forth. Thus, the 2841 microprogram is a subprogram (for the 2841) of the system to which the 2841 is attached. The using system instructs the 2841 to perform a specific program routine or series of routines. Upon completing the routine(s) (or determining that the routine cannot be completed) the 2841 signals the system that the routine is complete. The system can then accept data, transfer data, or initiate another operation.

Each microprogram instruction is represented by a 48-bit TROS word. The TROS word is punched into a flexible plastic tape called the TROS tape. Each TROS tape contains two words, designated A and B. A total of 126 tapes can be inserted over 256 U-shaped cores within a TROS module. The open end of each U core is capped by an I core, which contains a sense winding.

The selection of a TROS tape word is similar to the selection of a core storage word. The addressing scheme for the 2841 TROS consists of a four-bit module select code (W register) and an eight-bit tape word select code (X register). When the W and X register bits are decoded, a single tape drive line is selected and pulsed with a current. If the TROS tape was punched for a 1 bit, the drive links with the core (transformer action) and induces a current pulse into the sense winding; if the TROS tape was punched for a 0 bit, the drive pulse bypasses the core (no transformer action) and no

current pulse is detected in the sense winding. The current pulse in the sense winding is detected by and stored in a sense amplifier latch (SAL). A total of 48 SAL's are required to store the 2841 TROS tape word. Every 500 ns a new word is read into the SAL's.

Each 48-bit TROS word consists of 15 fields. Eleven of the 15 fields are used to control machine operations and to select the next TROS word. The remaining four fields are parity bits for the TROS tape word. The 11 fields used in controlling machine functions in the 2841 are:

1. CA field: A five-bit field which selects an A bus entry.
2. CB field: A two-bit field which selects a B bus entry.
3. CC field: A four-bit field which determines the arithmetic logic unit (ALU) control function (add, AND, and OR with the true value of the B entry).
4. CV field: A one-bit field which causes the B bus entry to be complemented.
5. CD field: A five-bit field which selects a register in which to store the data produced by the ALU control.
6. CK field: An eight-bit field which can be the B entry to ALU (selected by a CB field code) or can be used to modify the contents of the W register (selected by a CH field code).
7. CH field: A five-bit field which is used to sense machine conditions and cause a program branch by modifying bit 6 in the X register. This field can also cause the four low-order bits of the CK field to be gated to the W register.
8. CL field: A five-bit field which senses additional machine conditions and causes a program branch by modifying bit 7 in the X register. This field can also cause the eight bits of data on the A bus to be gated to the X register.
9. CN field: A six-bit field which is gated to A register bits 0-5. This field contains 0's when the A register is gated to the X register by the CL field.
10. CS field: A five-bit field which is used to set or reset specific bits in the status (ST) register.
11. BP field: A one-bit field which allows data from the A register to bypass ALU. If this field contains a 1 bit (bypass) the CB field must be coded with 0's.

The IBM document which contains the microprogram instruction listing is the Control Logic Diagram (CLD) manual. Each 48-bit microprogram instruction is shown pictorially in the CLD. The instruction pictorial is called a Control Automated System (CAS) microblock. Each CAS microblock depicts a 500 ns machine cycle and the machine operations that take place during the machine cycle.

Figures 2-42a through 2-52b illustrate the CAS microblock format, correlate the 11 TROS fields to the CAS microblock statements, briefly explain each statement that may be used within the CAS microblock, explain the TROS unit address decoding scheme, and illustrate and explain selected examples of CAS microblocks from the 2841 CLD's.

Figures 2-42a and 2-42b introduce the format of the CAS microblock and the format of the examples that are explained later. Observe that the figures consist of five parts. Four of them are numbered ①, ②, ③, and ④; the fifth is the CAS microblock example, located to the right of ③. (See Figure 2-42a.) The contents of the W and X registers are shown above and below the CAS microblock. The contents above represent the address for the illustrated CAS microblock; those below, the address for the next CAS microblock. Numbers ① and ② explain the addressing for the illustrated CAS microblock; ① relates to X register data shown in the upper left corner of the CAS microblock; and ② relates to the W and X register data

shown in the upper right corner of the CAS microblock. Number ③ explains data and operations shown on lines E, A, C, R, and F of the CAS microblock. (See left side of the CAS microblock shown in Figure 2-42a.) Number ④ explains how the address for the next CAS microblock is developed in the illustrated CAS microblock.

Figures 2-43a and 2-43b explain the significance of the characters used in addressing, and correlates the TROS fields to an example of a CAS microblock.

Figures 2-44a through 2-44d explain the use of the CK and CN fields and the modification of data in the W and X registers by the CK→W and A→X statements.

Figures 2-45a and 2-45b show CAS microblock arithmetic symbols, and show how to determine the module, gate, driver, tape number, tape word, and type of tape.

Figures 2-46a through 2-46e describe the function of each mnemonic used in the various TROS fields represented in the CAS microblock. In addition the hex and decimal value of each mnemonic are given.

Figures 2-47a through 2-52b are descriptions of the CAS microblocks taken from the CLD's. These examples start with the easily understood machine reset block and progress to the more difficult status set/reset, D = 0, DNST21, and counter blocks.

## 2.10 READING MICROPROGRAMS

### Leg Identifier

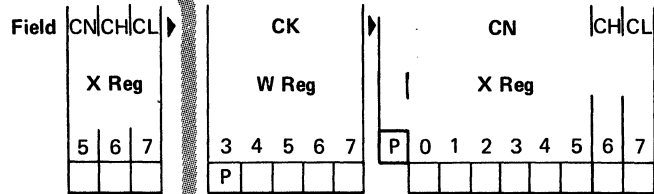
How You Got Here.....

- ① This portion of the following figures contains the Leg Identifier description.

### Hex Address

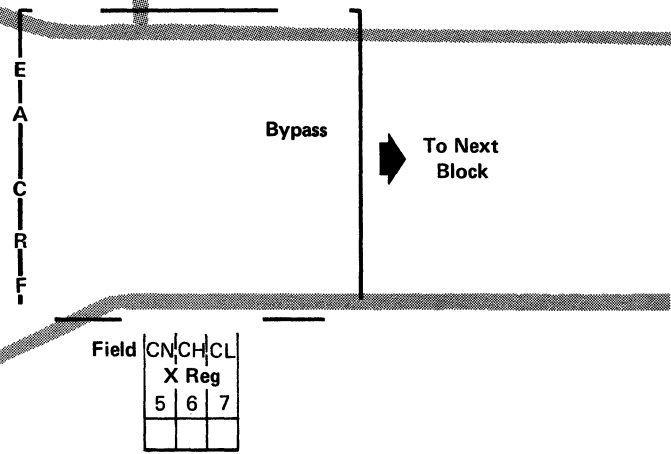
Where You Are.....

- ② This portion of the following figures contains the Hex Address description.



What You Do Here.....

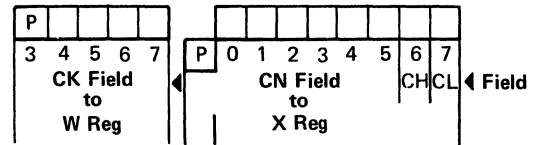
- ③ This portion of the following figures contains descriptions for the:
- E. Emit value (CK field)
  - A. ALU operations
  - C. Status conditions
  - R. Branching statements
  - F. Feature code



### Leg Selector

Where You Are Going.....

- ④ This portion of the following figures contains description for the:
- Leg Selector (X register bits 5, 6, and 7).
- E. Emit value for CK→W transfers
  - A. FC and FT register set/reset with CN 5 bit in Leg Selector
  - R. Set/Reset of X register 6 and 7



16413

Figure 2-42a. Introduction to Microblock Line Functions

**Leg Identifier**

**How You Got Here.....** Three low order X register bits controlled by the previous microblock. This is a repeat of the data in the Leg Selector of the previous microprogram block.

①

**Hex Address**

**Where You Are.....** Three hex characters controlled by the previous microblock.

②

Fields on this line represent address data developed in the previous microblock.

**What You Do Here.....**

③

- E. Data to use here ..... (Emit Value) .. E CK Field
  - A. The registers and arithmetic functions used here ..... (ALU Statement) .. A CA,CB,CV,CC,CD
  - C. Status conditions to set or reset ..... (Status) .. C CS Field
  - R. Address modification ..... (Branching Statement) .. R CH
  - F. *Caution:* Machine feature ..... (Feature Code) .. F
- BP Fields ..... Data bypasses ALU (Bypass).  
 To Next Block

Drawing Coordinate

Box Serial

**Leg Selector**

**Where You Are Going.....**

④

Branching statements on line R modify X6 and X7 bits. Thus, permitting 1, 2, and 4 way branches from a microprogram block. X5 bit (CN5) controls FC and FT set/reset when CK field is used as a B entry in line A statements.

Fields on this line represent address data developed in this microblock for the next microblock. W register data can be the existing data in this register or new data from the CK field. X register data (X0-X5) can be from the CN field or the A register. X6 and X7 are determined by the CH and CL fields except when the X register receives data from the A register.

16414

Figure 2-42b. Introduction to Microblock TROS Tape Fields

**Leg Identifier**

**How You Got Here.....**

① Indicates the branching conditions of the previous block.

If 2 bits, indicates X register 6 and 7.

If 3 bits, indicates CN5, (X register 5) and X register 6 and 7.

CN5 Bit	X Reg 6 and 7
0 = CN5 in Leg Selector of previous block was 0.	0 = Bit off in previous block.
1 = CN5 in Leg Selector of previous block was 1.	1 = Bit on in previous block.
	X = Bit not controlled in previous block.

(See Leg Sector)

**Hex Address**

**Where You Are.....**

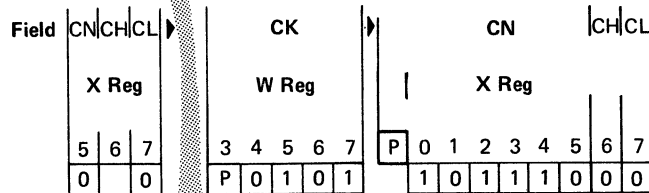
Indicates the address in TROS for this block.

Always 3 digits for 2841.

First digit is contents of the W register.

Second and third digits are the contents of the X register.

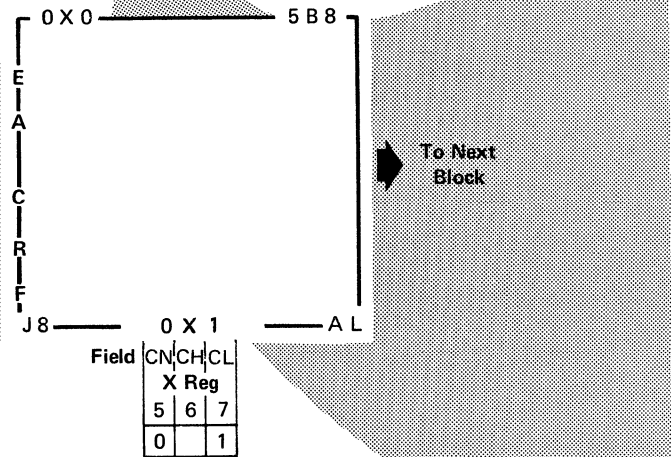
(Note the third digit in this address should agree with the X register bits in the Leg Identifier portion of this block).



See also 2-44b and 2-44c

**What You Do Here.....**

③



**Leg Selector**

**Where You Are Going.....**

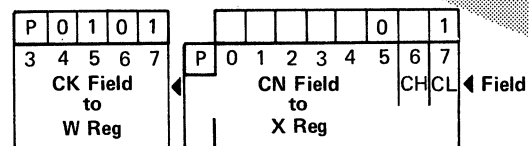
④ Indicates the branching conditions for this block.

If 2 bits, indicates X register 6 and 7.

If 3 bits, indicates CN5 (Xregister 5) and X register 6 and 7.

CN5 Bit	X Register 6 and 7
0 = Reset the bits in FC or FT register that correspond to the 1 bits in the Emit Field.	* = X bit is set if branching condition is met.
1 = Set the bits in the FC or FT register that correspond to the 1 bits in the Emit Field.	0 = X bit is a 0
	1 = X bit is 1.
	X = X bit is not controlled by branching statement.

See also 2-44a



See 2-44b

See 2-44b and 2-44c

16415

Figure 2-43a. Location of Address Data for the Microblock

Leg Identifier  
How You Got Here.....

Hex Address  
Where You Are.....

1

2

What You Do Here.....

3

- E. This line represents the CK field. The CK field consists of 1 byte of data which is used as a B entry for ALU operations.
- A. This line represents the CA, CA alternate, CB, CC, CD, CD alternate, CV, and BP fields. Each ALU statement requires codes in a minimum of 4 of these fields; the CA, CB, CC, and CD. The CA alternate field (CA A) extends the CA field; the CD alternate field (CD A) extends the CD field; the CV field (complement B entry) extends the CC field; the BP field causes A entry data to BYPASS ALU (the CB, CC, and CV fields are coded with zeros when the BP field is used).
- C. This line represents the CS field. The CS field is used to set or reset individual bits in the ST register (status).
- R. This line represents the CH and CL fields. These fields are used to sense various register bits and conditions within the 2841. When the designated bit or condition is sensed, the X6 or X7 bit is set and the microprogram branches to the desired microblock.
- F. This line is used to flag microprogram blocks that are NOT used by all storage devices that can be attached to the 2841

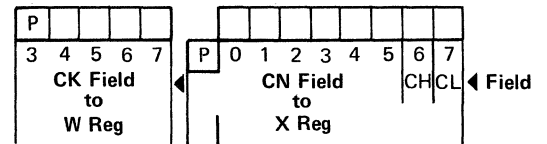
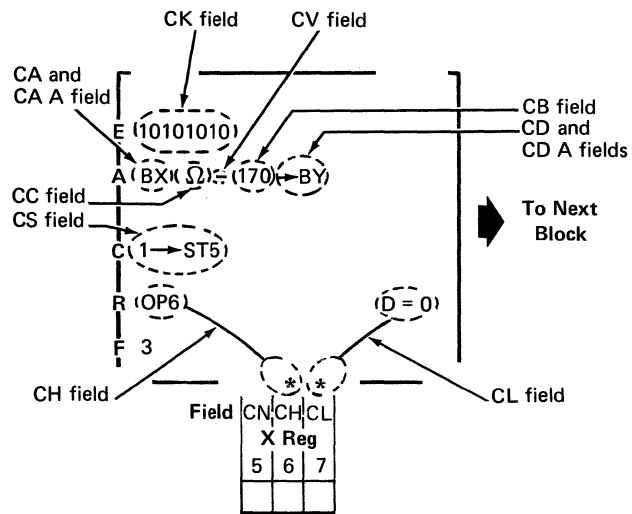
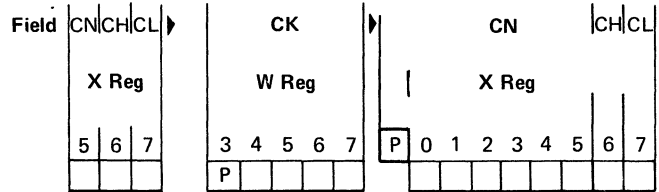


Figure 2-43b. Location of TROS Fields for a Typical Microblock Example

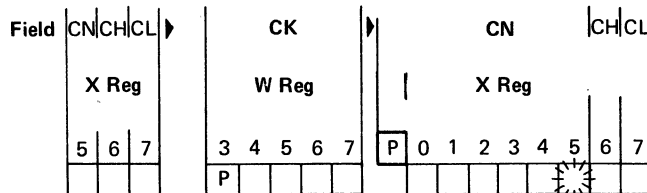
16416



Hex Address  
Where You Are.....

2

TROS Tape	31	33	35	37	39	41	43	45
	06	07	08	09	10	11	12	13
Field	CK Field							
Field Bit Position	0	1	2	3	4	5	6	7
Binary Value	128	64	32	16	8	4	2	1
	B Reg Entry							

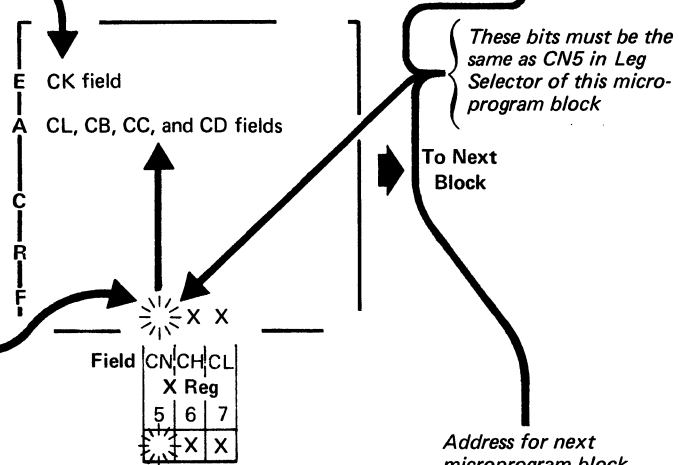


Address for this micro-program block

What you Do Here .....

3

- E. (1) } CN5 bit = 0, data in CK field and A
  - A. (1) } buss entry to FC or FT register.
  - 1 bits in the CK field reset the cor-
  - responding FC or FT bits. CN5 bit
  - for this and the next X address is a 0.
- 0
- E. (2) } CN5 bit = 1, data in CK field and A
  - A. (2) } buss entry to FC or FT register.
  - 1 bits in the CK field set the cor-
  - responding FC or FT bit. CN5 bit
  - for this and the next X address is a 1.
- 1 or



Line E of the microblock always shows the 8 bits of the CK field.

Line A of the microblock (ALU statement) is shown as a decimal value to the FC or FT register.

Examples:

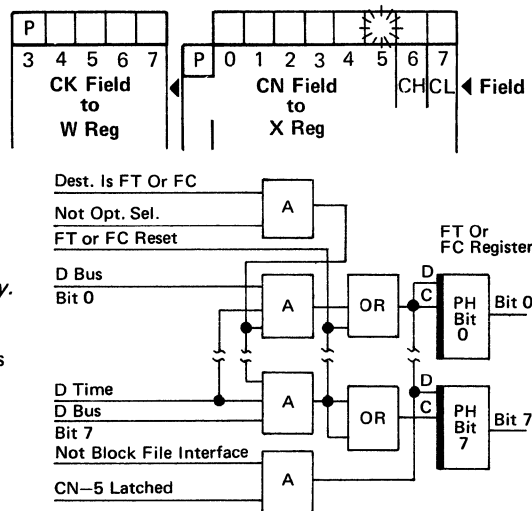
- 1. { E 10000000      3. { E 00000000
- A 128→FC        A 0-0→FT      5. A 0→FT
- 2. { E 10101100      4. A 0-0→FC
- A 172→FT

Examples 1 and 2 are coded on the TROS tape as (1.) 0 + 128→FT and (2.) 0 + 172→FT but are not written this way in the CAS micro-blocks. Examples 3 through 5 are valid operations and are used occasionally.

Normally the CK field is used with the CN5 bit to set or reset the FC or FT registers. However, the conditions which allow entry to the FC and FT registers are:

- 1. a destination of FC or FT      3. data on the D buss
- 2. CN5 equal to 0 or 1

Thus, FC and FT selective set/reset is initiated by a CD field decode of FC or FT (Hex D or E). See figure below. The CN5 bit is present each time a new X address is read from a TROS tape and all ALU operations place data on the D buss.



16417

Figure 2-44a. CK Field and CN5 Bit Used to Set or Reset Bits in the FC and FT Registers

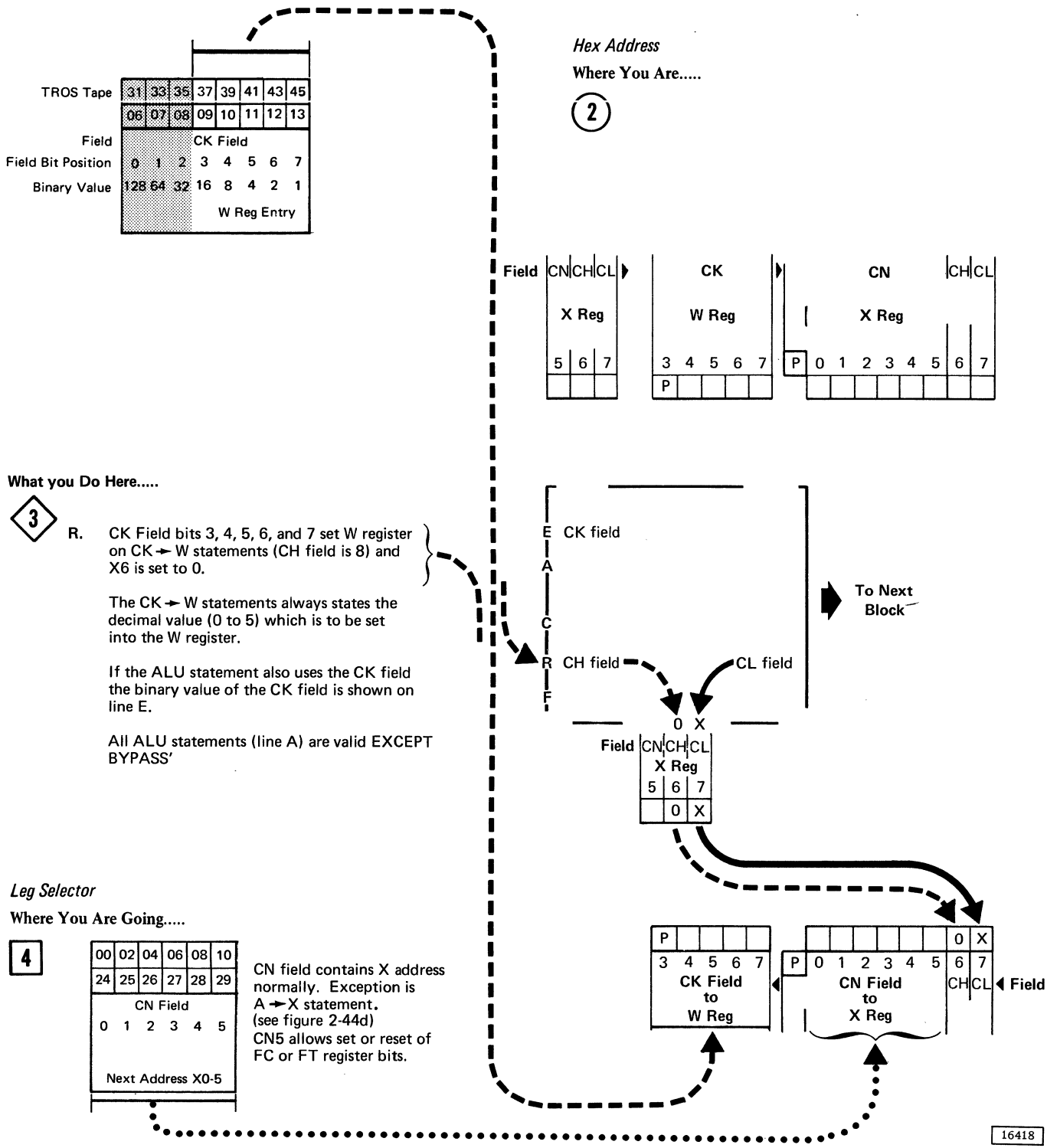
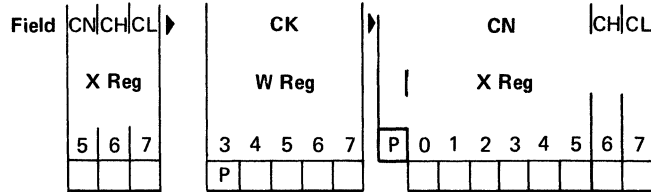


Figure 2-44b. CK Field Transfers to W Register and CN Field Transfers to X Register

TROS Tape	31	33	35	37	39	41	43	45
	06	07	08	09	10	11	12	13
Field	CK Field							
Field Bit Position	0	1	2	3	4	5	6	7
Binary Value	128	64	32	16	8	4	2	1
	B Reg Entry							

Hex Address  
Where You Are....

2



What You Do Here....

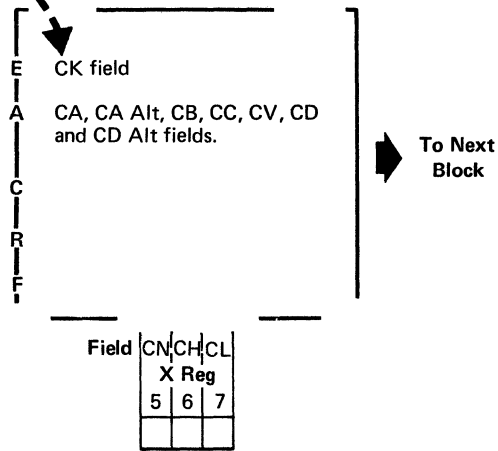
3

- E. } CK field is a data source
- A. } via the B buss for ALU statements.

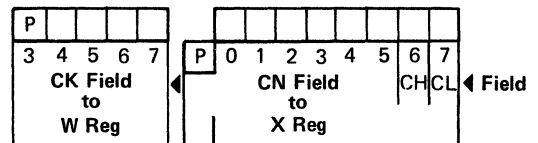
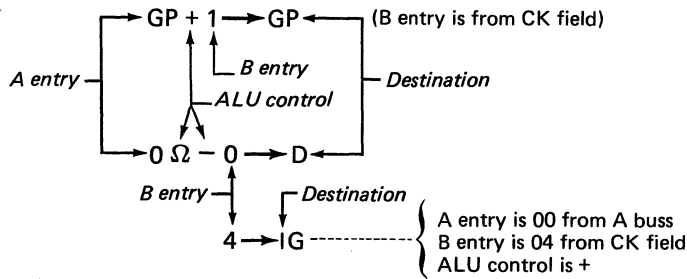
Line E of the microblock always shows the 8 bits of the CK field. Example: 10000000

Line A of the microblock (ALU statement) shows A entry, ALU control, B entry (decimal value) and destination (normal ALU statement)

The Bypass statement cannot be used because there is a B entry.



Examples:



This statement (4 → IG) is coded on the TROS tape as 0 + 4 → IG but is not written this way in the CAS microblocks.

16419

Figure 2-44c. CK Field Used as a Data Source for ALU

*Leg Identifier*  
How You Got Here.....

1

*Hex Address*  
Where You Are.....

2

What You Do Here.....

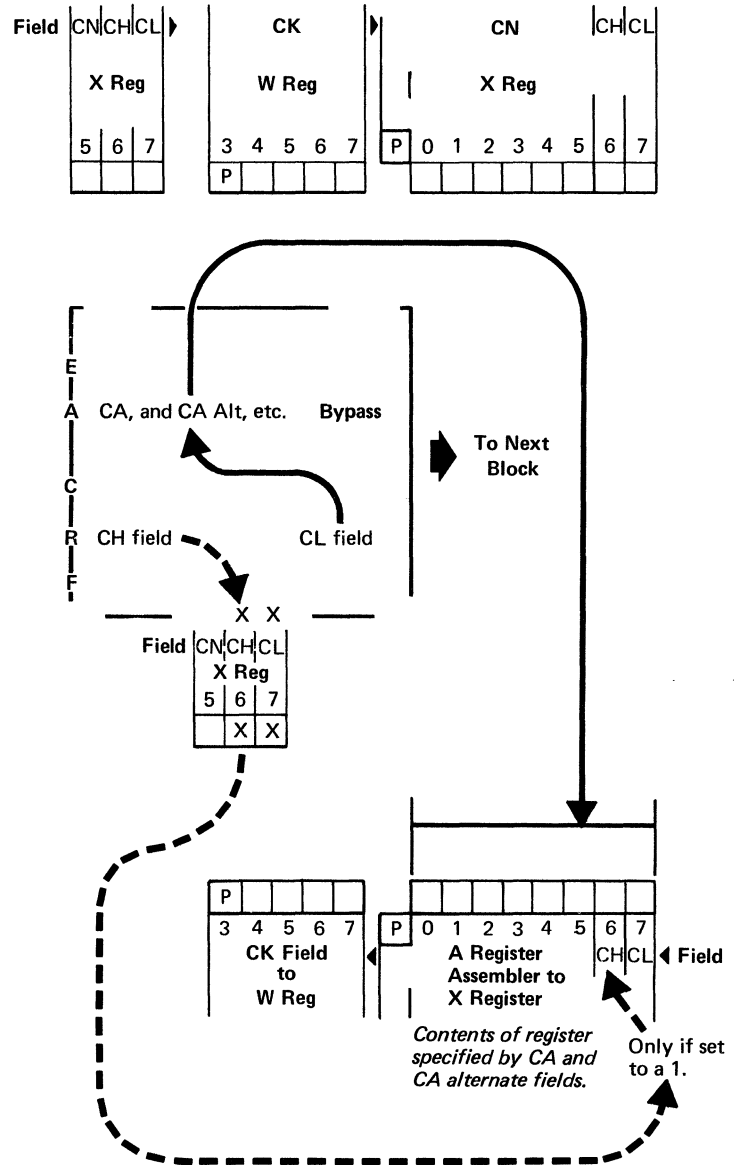
3

- A. } Data from the A register assembler is gated to the
- R. } X register on A → X statements (CL field is 6).

The A → X statement causes the contents of the A entry register specified by the CA and CA alternate fields to be transferred to the X register. The data going to the X register is NOT changed by the ALU control statement or data from the B entry register.

All valid ALU statements including Bypass are used with the A → X statement.

Normally a CH field branch is NOT used with the A → X (CL 6) statement. However, the 1 bit inputs to the X register are ORed and the absence of ALL 1 bit inputs to an X register bit position sets the X register bit position to a 0. Thus, any CH field branch that sets X6 to a 1 overrides a 0 bit from the A register assembler.



16420

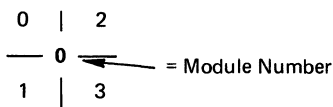
Figure 2-44d. A Register Assembler to X Register Transfers

**TO CONVERT HEX ADDRESS TO TROS GATE AND DRIVER DECODE:**

**GATE DECODE**

1. Use W register bits 4-7 and X register bits X0 and X1.
2. Convert W4, W5, and X0 bits to decode for the OCTAL tens position (00, 10, 20, and 30 normally, but to 50 in machines with 2303).
3. Convert W6, W7 and X1 bits to decode for the OCTAL units position (1-7).
4. Use the decodes from 2 and 3 with this table to determine the gate and module. *See examples on next page.*

Tens	00	10	20	30	40	50	Tape Word
0	0	2	16	18	32	34	A
1	1	3	17	19	33	35	B
2	4	6	20	22	36	38	A
3	5	7	21	23	37	39	B
4	8	10	24	26	40	42	A
5	9	11	25	27	41	43	B
6	12	14	28	30	44	46	A
7	13	15	29	Not used	47		B
Tapes	0-63		0-63		0-63		X0 = 0
		64-127		64-127		64-127	X0 = 1



**DRIVER DECODE**

1. Use X register bits 2-7.
2. Decode bits X2, X3 and X4 for the OCTAL tens position. (00, 10, 20 through 70).
3. Decode bits X5, X6 and X7 for the OCTAL units position (0, 1, 2, through 7).

4. Use the decodes from 2 and 3 with this table to determine the driver. *See examples on next page.*

Tens	00	10	20	30	40	50	60	70
0	0	8	16	24	32	40	48	56
1	1	9	17	25	33	41	49	57
2	2	10	18	26	34	42	50	58
3	3	11	19	27	35	43	51	59
4	4	12	20	28	36	44	52	60
5	5	13	21	29	37	45	53	61
6	6	14	22	30	38	46	54	62
7	7	15	23	31	39	47	55	63

5. OR; Convert the OCTAL decode to decimal for the driver line (0 through 63).

**TO CONVERT HEX ADDRESS TO TROS MODULE NUMBER AND TAPE NUMBER:**

1. W register is the TROS module number. *See examples.*
2. X0 = 0 the tape number is 0-63.  
X0 = 1 the tape number is 64-127.
3. Convert bits X2-X7 to decimal.  
If X0 = 0, X2-X7 is the tape number.  
If X0 = 1, Subtract the decimal value of X2-X7 from 127.  
The answer is the tape number. *See examples.*
4. If X1 = 0 the microblock is tape word A.  
If X1 = 1 the microblock is tape word B.  
*See examples on next page.*

**TO DETERMINE TYPE OF TAPE:**

1. Divide tape number by 3.
2. If the remainder is:
  - a. 0 the tape is an A type
  - b. 1 the tape is a B type
  - c. 2 the tape is a C type
3. Tape 00 is an A type.  
Tape 01 is a B type.  
Tape 02 is a C type.  
*See examples on next page.*

16421

Figure 2-45a. TROS Addressing: Driver and Gate, Tape Number and Tape Type

EXAMPLES

Address	65F	AA9	9FD
W Register	0110	1010	1001
X Register	0101 1111	1010 1001	1111 1101
W4, W5, X0	010=20 <sub>8</sub>	101=50 <sub>8</sub>	101=50 <sub>8</sub>
W6, W7, X1	101=5 <sub>8</sub>	100=4 <sub>8</sub>	011=3 <sub>8</sub>
Gate/Tape Word	25/B	42/A	39/B
X2-4	011=30 <sub>8</sub>	101=50 <sub>8</sub>	111=70 <sub>8</sub>
X5-7	111=7 <sub>8</sub>	001=1 <sub>8</sub>	101=5 <sub>8</sub>
Driver	31	41	61
W4-7	0110=6	1010=10	1001=9
Module	6	10	9
X0 (tape)	0=0-63	1=64-127	1=64-127
X1 (tape word)	1=B	0=A	1=B
X2-7	011 111=31	101 010=41	111 101=61
Tape Number	31	127-41=86	127-61=66
Octal/Decimal	37 <sub>8</sub> =31	51 <sub>8</sub> =41	75 <sub>8</sub> =61
Tape Type	31:3=10 R1 R1=B	86:3=28 R2 R2=C	66:3=22 R0 R0=A

ARITHMETIC SYMBOLS

Symbol	Definition	Example
+	True Add/Positive	A + B: B is added (true) to A.
-	Complement Add/Subtract, Negative	A - B: B is complement added to A.
→	Is Set Into (transferred to)	A → B: A is set into B (destructive read-in is implied).
•	Is ANDed With (logical)	A • B: A is ANDed with B.
Ω	Is ORed With (logical)	A Ω B → C: A is ORed with B and the result is set into C.
∇	Is Exclusive ORed With	A ∇ B → C: A is exclusive ORed with B and set into C.

16422

Figure 2-45b. Examples of TROS Addressing and Microblock Arithmetic Symbols

TROS FIELD CODE DESCRIPTIONS

TROS Tape	17	19	21	23	25	Hex	Decimal	Description	
Word Bit Position	45	00	01	02	03				
Field	CA CA Field								
Field Bit Position	A	0	1	2	3	4			
Binary Value	16	8	4	2	1				
Use	A Register Entry								
Alt	Normal								
	None					00	0	Gate Hex 00 from the A buss to the A register.	
	GL					01	1		
	BY					02	2		
	BX					03	3		
	FR					04	4		
	KL					05	5		
	DL					06	6		
	DH					07	7		
	OP					08	8		
	GP					09	9		
	UR					0A	10		
	DW					0B	11		
	DR					0C	12		
	ER					0D	13		
	IE					0E	14		
	IH					0F	15		
SW						10	16	Gate the contents of the specified register to the A register via the A buss.	
Stop						11	17		If CHECK STOP switch is on stop the 2841 microprogram.
SC						1C	28		
FS						1D	29	Gate the contents of the specified register to the A register via the A buss.	
OA						1E	30		
IS						1F	31		
								Codes 18 through 27 (Hex 12-1B) are not decoded.	
TROS Tape	27	29							
Word Bit Position	04	05							
Field	CB								
Field Bit Position	0	1							
Binary Value	2	1							
Use	B Ent								
	None		0	0	Gate Hex 00 from the B buss to the B entry assembler.				
	BY		1	1	Gate BY register to B entry assembler via B buss.				
	CK		2	2	Gate data in CK field latches to B entry assembler via B buss.				
	DR		3	3	Gate DR register to B entry assembler via B buss.				

TROS Tape	46	Description
Field	BP	
Field Bit Position	0	
	0	Data from ALU is gated to the D buss.
	1	A register data is gated to the D buss, bypassing ALU.

16423

Figure 2-46a. CA, CA A, CB and BP Fields: A and B Entry and Bypass

TROS Tape	22	14	16	18	20	Hex	Decimal	Description
Word Bit Position	35	31	32	33	34			
Field	CD	CD Field						
Field Bit Position	A	0	1	2	3			
Binary Value	16	8	4	2	1			
Use	Destination Reg							
Alt	Normal							
	D					00	0	Gate ALU to D buss.  Gate ALU to specified register via the D buss.
	GL					01	1	
	BY					02	2	
	BX					03	3	
	FR					04	4	
	KL					05	5	
	DL					06	6	
	DH					07	7	
	OP					08	8	
	GP					09	9	
	UR					0A	10	
	DW					0B	11	
	DR					0C	12	
	FT					0D	13	
	FC					0E	14	
	IG					0F	15	
	SW					10	16	

TROS Tape	24	26	28	30	Hex	Decimal	Description	Example
Word Bit Position	36	37	38	39				
Field	CV	CC						
Field Bit Position	0	0	1	2				
	1	4	2	1				
Use	ALU Control							
	A+B → D				0	0	B is added (true) to A.	BX + BY → GL
	A+B+1 → D				1	1	B is added (true) to A and a carry in of 1 is forced to ALU.	BX + BY + 1 → GL
	A . B → D				2	2	A is ANDed (logical) with B.	GL • CK → GP
	A ∩ B → D				3	3	A is ORed (logical) with B.	ER ∩ CK → UR
	A + B → DC				4	4	B is added (true) to A, and carry out is set in ST3.	BX + CK → GPC
	A+B+1 → DC				5	5	B is added (true) to A and a carry in of 1 is forced, any carry out is set into ST3. GL + BY + 1 → URC	
	A+B+C → DC				6	6	B is added (true) to A and ST3 is gated to carry in, and carry out is set into ST3. BX + CK + C → GPC	
	A ∨ B → D				7	7	A and B are Exclusive ORed.	BX ∨ BY → GP
	A - B → D				10	8	Same as above except that B is complemented.	
	A - B + 1 → D				11	9		
	A . - B → D				12	10		
	A ∩ - B → D				13	11		
	A - B → DC				14	12		
	A - B + 1 → DC				15	13		
	A - B + C → DC				16	14		
	A ∨ - B → D				17	15		

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Figure 2-46b. CD, CD A, CC, and CV Fields: Destination and ALU Control



TROS Tape Word Bit Position	32	34	36	38	Hex	Decimal	Description
	40	41	42	43			
Field	CS						
Field Bit Position	0	1	2	3			
Binary Value	8	4	2	1			
Use	ST Control						
	Not Used	0	0				Not used.
	0 → ST0	1	1				Set indicated bit position in the ST register to 0 or 1 as indicated. ----- Allow Index.
	1 → ST0	2	2				
	0 → ST1	3	3				
	1 → ST1	4	4				
	0 → ST2	5	5				
	DNST21	6	6				If D buss is non-zero (1 or more) set ST register Bit 2 to 1.
	0 → ST3	7	7				Set indicated bit position in the ST register to 0 or 1 as indicated.
	1 → ST3	8	8				
	0 → ST4	9	9				
	0 → ST5	A	10				
	1 → ST5	B	11				
	0 → ST6	C	12				
	1 → ST6	D	13				
	0 → ST7	E	14				
	1 → ST7	F	15				

16425

Figure 2-46c. CS Field: Status Control

TROS Tape Word Bit Position Field	09	11	13	15	Hex	Decimal	Description
	14	15	16	17			
Field Bit Position	CL Field						
Binary Value	0	1	2	3			
Use	Branch X7						
	0 → X7				0	0	Set X register bit 7 to 0.
	1 → X7				1	1	Set X register bit 7 to 1.
	ST3				2	2	} If indicated ST register bit is a 1, Set X register bit 7 to a 1. If ST register bit is 0 set X register 7 to 0.
	ST5				3	3	
	ST7				4	4	
	D = 0				5	5	If D buss is zero set X register bit 7 to a 1. If D buss is not zero set X 7 to 0.
	A → X				6	6	Gate the contents of the A register (0-7) to the X register (0-7).
	File				7	7	If optional interface is selected, set X 7 to a 1; if not selected set X 7 to 0.
	SERVO				8	8	If Service Out is up, set X 7 to 1; if Service Out is down set X 7 to 0.
	SORSRP				9	9	If Service Out Response is up, set X 7 to 1; if Service Out Response is down, set X 7 to 0.
	SELTO				A	10	If Select Out is up, set X 7 to 1; if Select Out is down set X 7 to 0.
	OP1				B	11	} If indicated OP register bit is a 1, set X 7 to a 1; if OP register bit is a 0, set X 7 to a 0.
	OP3				C	12	
	OP5				D	13	
	Index				E	14	If ST1 is a 1 and index is detected, set X 7 to 1; no index, set X 7 to 0.
	OP7				F	15	If OP register bit 7 is 1, set X 7 to 1; if OP register 7 is 0, set X 7 to 0.

TROS Tape Word Bit Position Field	01	03	05	07	Hex	Decimal	Description
	18	19	20	21			
Field Bit Position	CH Field						
Binary Value	0	1	2	3			
Use	Branch X6						
	0 → X6				0	0	Set X register bit 6 to 0.
	1 → X6				1	1	Set X register bit 6 to 1.
	ST0				2	2	} If indicated ST or Op register bit is 1, set X 6 to 1; if ST or OP register bit is 0 set X 6 to 0.
	OP6				3	3	
	ST2				4	4	
	ST4				5	5	
	ST6				6	6	
	File				7	7	If optional interface is selected, set X 6 to 1, if not selected, set X 6 to 0.
	CK ← W(0 → X6)				8	8	Set X 6 to 0 and gate CK Field bits 4, 5, 6 and 7 to the W register.
	Carry				9	9	If Carry Out latch is set, set X 6 to 1; if Carry Out is reset, set X 6 to 0.
	COMMO				A	10	If command Out is up, set X 6 to 1; if command Out is down, set X 6 to 0.
	SUPPO				B	11	If Suppress Out is up, set X 6 to 1; if Suppress Out is down, set X 6 to 0.
	Unused				C	12	Not used.
	OP0				D	13	} If indicated OP register bit is 1, set X 6 to 1; if OP register bit is 0, set X 6 to 0.
	OP2				E	14	
	OP4				F	15	

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Figure 2-46d. CH and CL Fields; Branch Control X6 and X7

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**Leg Identifier**

How You Got Here.....

① Previous TROS tape word.

**Hex Address**

Where You Are.....

② Previous TROS tape word.

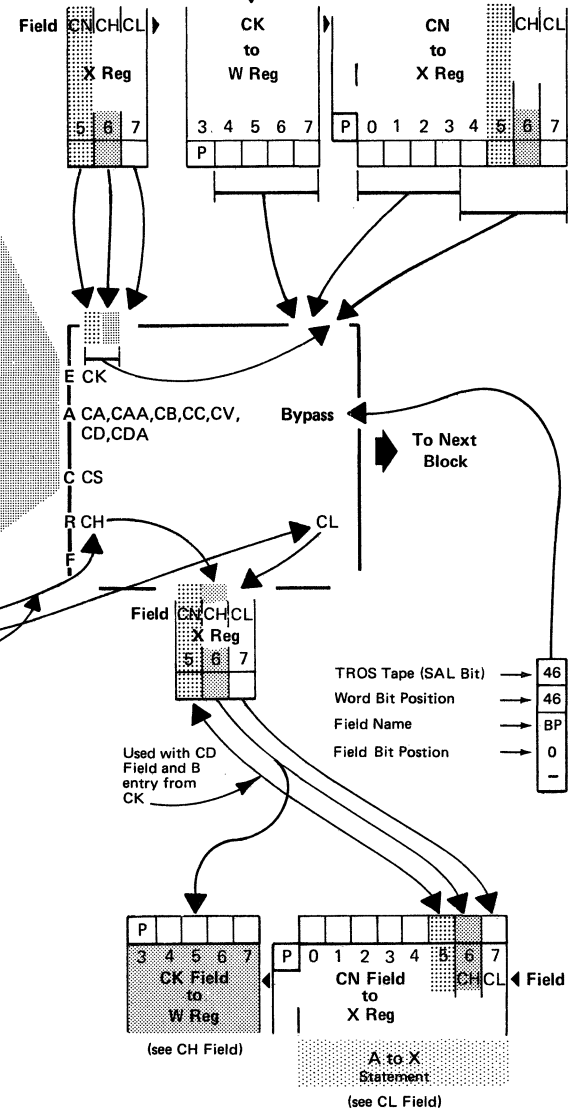
TROS Tape (SAL Bit)	31	33	35	37	39	41	43	45
Word Bit Position	06	07	08	09	10	11	12	13
Field Name	CK Field							
Field Bit Position	0	1	2	3	4	5	6	7
Binary Value	128	64	32	16	8	4	2	1
Use	W Reg Entry							

TROS Tape (SAL Bit)	00	02	04	06	08	10	12	
Word Bit Position	24	25	26	27	28	29	30	
Field Name	CN Field							PN
Field Bit Position	0	1	2	3	4	5	0	
Binary Value	-							-
Use	Next Address X0-5							P

**What You Do Here.....**

③ This TROS tape word.

TROS Tape (SAL Bit)	17	19	21	23	25	27	29	24	26	28	30	22	14	16	18	20	32	34	36	38
Word Bit Position	45	00	01	02	03	04	05	36	37	38	39	35	31	32	33	34	40	41	42	43
Field Name	CA	CA Field				CB	CV	CC	CD	CD Field				CS						
Field Bit Position	0	1	2	3	4	0	1	0	0	1	2	3	0	1	2	3				
Binary Value	16	8	4	2	1	2	1	4	2	1	16	8	4	2	1	8	4	2	1	
Use	A Register Entry				B Ent	ALU Control				Destination				ST Control						
	Alt	Normal					See Note 5				Normal	Alt								
16	0	SW	None				None	A+B → D				D	SW				Not Used			
17	1	Stop	GL				BY	A+B+1 → D				GL	0 → ST0							
	2		BY				CK	A.B → D				BY	1 → ST0							
	3		BX				DR	A.A.B → D				BX	0 → ST1							
	4		FR					A + B → DC				FR	1 → ST1							
	5		KL					A+B+1 → DC				KL	0 → ST2							
	6		DL					A+B+C → DC				DL	DNST21							
	7		DH					A ∅ B → D				DH	0 → ST3							
	8		OP					A - B → D				OP	1 → ST3							
	9		GP					A - B + 1 → D				GP	0 → ST4							
	10		UR					A . - B → D				UR	0 → ST5							
	11		DW					A.A.-B → D				DW	1 → ST5							
28	12	SC	DR					A - B → DC				DR	0 → ST6							
29	13	FS	ER					A - B + 1 → DC				FS	1 → ST6							
30	14	OA	IE					A - B + C → DC				FC	0 → ST7							
31	15	IS	IH					A ∅ B → D				IG	1 → ST7							



**Leg Selector**

Where You Are Going.....

④ This TROS tape word.

TROS Tape (SAL Bit)	01	03	05	07	09	11	13	15	31	33	35	37	39	41	43	45
Word Bit Position	18	19	20	21	14	15	16	17	06	07	08	09	10	11	12	13
Field Name	CH Field				CL Field				CK Field							
Field Bit Position	-				-				0 1 2 3 4 5 6 7							
Binary Value	-				-				128 64 32 16 8 4 2 1							
Use	Branch X6				Branch X7				W Register Entry							

0	0 → X6	0 → X7
1	1 → X6	1 → X7
2	ST0	ST3
3	OP6	ST5
4	ST2	ST7
5	ST4	D = 0
6	ST6	A → X
7	File	File
8	CK = W(0 → X6)	SERVO
9	Carry	SORSP
10	COMMO	SELTO
11	SUPPO	OP1
12	Unused	OP3
13	OP0	OP5
14	OP2	Index
15	OP4	OP7

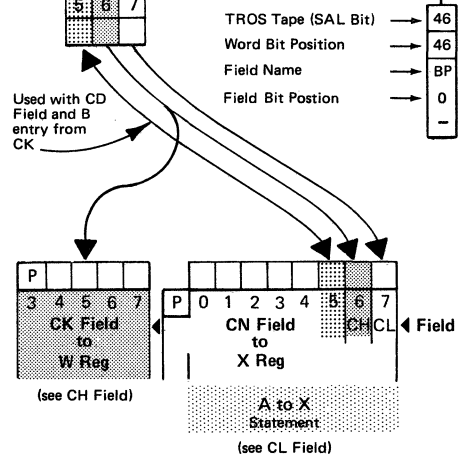


Figure 2-46e. Location of TROS Field Data in CAS Microblocks

**MICROBLOCK EXAMPLE, MACHINE RESET**

**Leg Identifier**

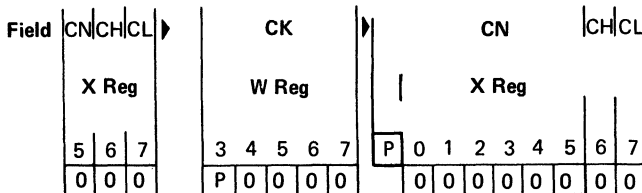
**How You Got Here.....**

- ① The RESET switch was pressed. This caused all registers and indicators to be reset. Thus the address 000 in the W and X registers.

**Hex Address**

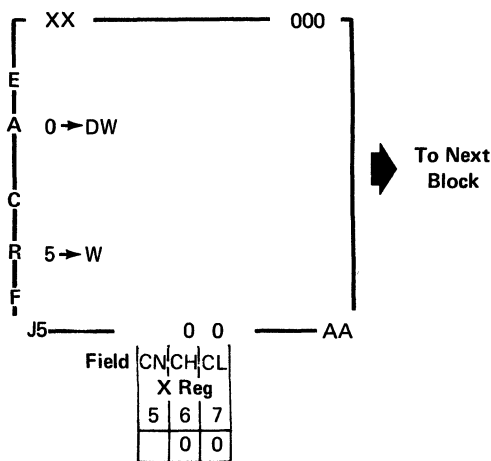
**Where You Are.....**

- ② This is module 0, tape word A, tape 00. Resetting the machine cleared the W and X registers. The internal clock in the machine causes TROS to read out address 000 and enter the Reset Entry block of the TROS.



**What You Do Here.....**

- ③ A. This statement says; transfer 0 from the A register to the DW register. The operation is valid but meaningless since the DW register was reset to 0 by the machine RESET.
- R. This statement performs 2 functions:
  1. Transfer 5 from the CK field to the W register.
  2. Set X register bit 6 to 0.
 Note that X6 can also be zeroed by the statement 0 → X6.

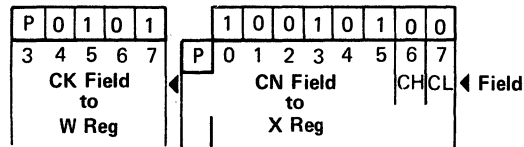


**Leg Selector**

**Where You Are Going.....**

- ④ This portion of the microblock indicates that the TROS tape contains 2 branching statements on line R. The CH field statement sets X6 to a 0. The CL field statement, which does not show on line R, says set X7 to a 0. It is typical in CAS logic to indicate the X6 and X7 set/reset statements in the Leg Selector. Thus 0 → X6, 1 → X6, 0 → X7, and 1 → X7 statements do not appear on the R line.

The address of the next microblock is W register 5, the contents of the CN field from this TROS tape, and X6 and X7 equal to 0. You determine the contents of the CN field by looking at the address shown in the next microblock.



16428

Figure 2-47a. CK to W Register Transfer

TROS Tape (SAL Bit) →	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	01	03	05	07	09	11	13	15	00	02	04	06	08	10	12	22	14	16	18	20	24	26	28	30	32	34	36	38	46	
Word Bit Position →	45	00	01	02	03	04	05	06	07	08	09	10	11	12	13	18	19	20	21	14	15	16	17	24	25	26	27	28	29	30	35	31	32	33	34	36	37	38	39	40	41	42	43	44	
Field Name →	CA CA Field				CB				CK Field							CH Field			CL Field			CN Field					PN	CD	CD Field			CV	CC	CS			BP								
Field Bit Position →	A	0	1	2	3	4	0	1	0	1	2	3	4	5	6	7	0	1	2	3	0	1	2	3	0	1	2	3	4	5	0	0	0	1	2	3	0	0	1	2	0	1	2	3	0
Binary value →	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	1	0	1	0	1	0	1	1	0	1	0	1	0	1	1
Use →	A Register Entry				B Ent				B Reg Entry							Branch X6			Branch X7			Next Address X0-5					P	Destination			ALU Control			ST Control											
Alt	Normal				None				CK3 becomes W Reg parity on CK→W statements.							0 → X6			0 → X7			Except on statements when the next address is the contents of the register defined by the CA field in the ALU statement. CN5 is shown as 1 or 0 in the legend when it is used as a control register.					Normal			Alt			Not Used												
SW	None				None											0 → X6			0 → X7								D			SW			A+B → D			Not Used									
16 0	Stop				GL				BY							ST0			ST3								GL			A+B → D			0 → ST0												
17 1					BY				CK							ST0			ST3								BY			A-B → D			1 → ST0												
2					BX				DR							OP6			ST5								BX			A-B → D			0 → ST1												
3					FR											ST2			ST7								FR			A → DC			1 → ST1												
4					KL											ST4			D = 0								KL			A+B → DC			0 → ST2												
5					DL											ST6			A → X								DL			A+B → DC			DNST21												
6					DH											File			File								DH			A → B → D			0 → ST3												
7					OP											CK←W(0→X6)			SERVO								OP			A → B → D			1 → ST3												
8					GP											Carry			SORSP								GP			A → B + 1 → D			0 → ST4												
9					UR											COMMO			SELTO								UR			A → B → D			0 → ST5												
10					DW											SUPPO			OP1								DW			A → B → D			1 → ST5												
11					SC											Unused			OP3								DR			+B → DC			0 → ST6												
28 12					FS											OP0			OP5								FT			-B → DC			1 → ST6												
29 13					OA											OP2			Index								FC			A-B-C → DC			0 → ST7												
30 14					IS											OP4			OP7								IG			A → B → D			1 → ST7												
31 15					IH																																								

2841 Clock Time	TROS Decode or 2841 Function
D	Select TROS tape addressed by W and X registers. Decode CA, CA alternate and CB Fields.
A	A and B busses gated to ALU. The A register is latched up. Set and Reset CC, CV, and CD Fields. ALU operation is started.
B	CC, CV and CD Field reset is removed and these fields are latched. ALU operation is completed and answer is on D buss.
C	Sample D buss for zero and set carry latch if there was a carry.
D	The register (if any) designated by the CD field is loaded with the output of ALU. Status register 3 is set or reset if the operation was one which stored the carry out in ST 3 (→DC).  Status register 2 is set now if the ROS word contained a DNST21 statement and the D buss did not equal zero. The next ROS word is now available for field decoding.
A-C	Same as above.

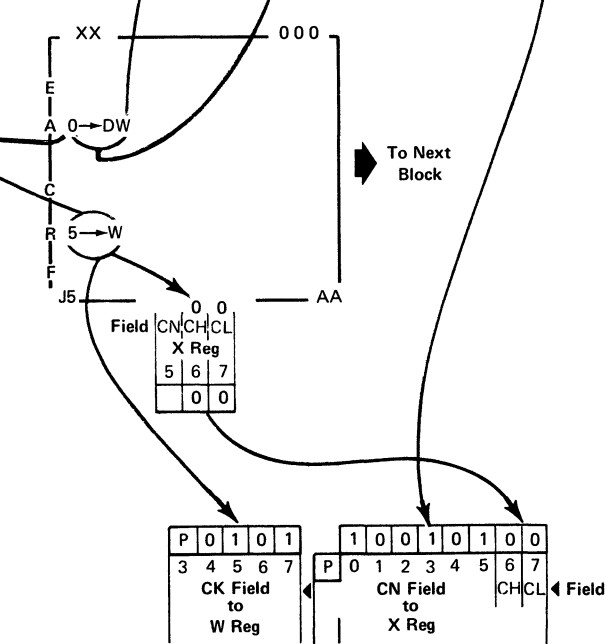


Figure 2-47b. CK to W Register Transfer: Timing and TROS Fields

# MICROBLOCK EXAMPLE, SCAN

## Leg Identifier

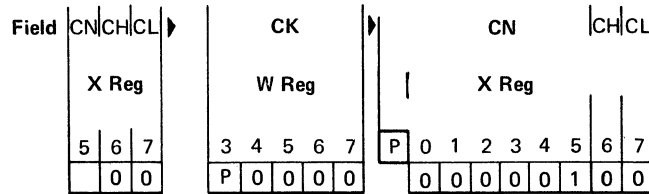
### How You Got Here.....

- 1 By resetting the machine, setting the ADDRESS COMPARE switch to SCAN and setting the START ADDRESS switch to 004 and starting the machine.

## Hex Address

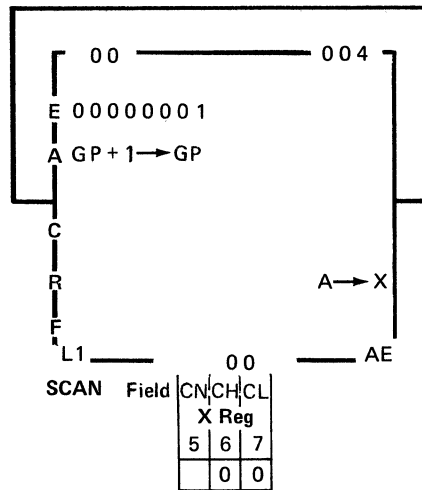
### Where You Are.....

- 2 This module 0 tape word A tape 04.



### What You Do Here.....

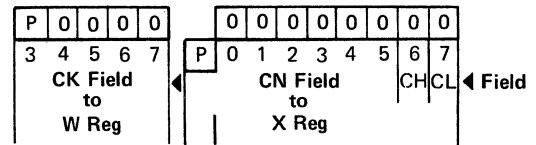
- 3
  - A. This statement says to transfer the GP register to the A register, add 1 to the A register and transfer the sum back to the GP register.
  - E. The CK field contains the value 1 which is to be added to the A register.
  - R. This statement says that the contents of the A register are to be transferred to the X register and used as the address for the next microblock.



## Leg Selector

### Where You Are Going.....

- 4 In this microblock the 00 in the Leg Selector is meaningless. The address for the second microblock (000) is transferred to the X register from the GP register(A→X). The address for the third microblock (004) is transferred to the X register from the START ADDRESS by the Recycle FL. The fourth microblock address is again transferred from the GP register to the X register. Remember that the GP register is incremented by 1 each time the program enters microprogram block 004. Thus, this block is a one block program (to check addressing) that alternates from address 004 to 000 back to 004 to 001, back to 004 to 002, back to 004 etc.



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Figure 2-48a. Module 0 Address Scan

TROS Tape (SAL Bit)	17	19	21	23	25	27	29	31	33	35	37	39	41	43	45	01	03	05	07	09	11	13	15	00	02	04	06	08	10	12	22	14	16	18	20	24	26	28	30	32	34	36	38	40	42	44	46
Word Bit Position	45	00	01	02	03	04	05	06	07	08	09	10	11	12	13	18	19	20	21	14	15	16	17	24	25	26	27	28	29	30	35	31	32	33	34	36	37	38	39	40	41	42	43	44	45	46	
Field Name	CA CA Field				CB	CK Field							CH Field			CL Field		CN Field					PN	CD Field			CV	CC		CS			BP														
Field Bit Position	A	0	1	2	3	4	0	1	2	3	4	5	6	7						0	1	2	3	4	5	0	0	1	2	3	0	0	1	2	0	1	2	3	0								
Binary value	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1									
Use	A Register Entry				B Ent	B Reg Entry							Branch X6			Branch X7		Next Address X0-5					P	Destination			ALU Control		ST Control																		

16	0	Alt SW	Normal	None	None	0 → X6	0 → X7	Except on A→X Statements when the next Address is the Contents of the Register Defined by the CA Field in the ALU Statement.	Normal D	Alt SW	A+B → D	Not Used	
17	1	Stop	GL	BY	ST0	ST3	1 → X6		1 → X7	GL	D	A+B+1 → D	0 → ST0
2			BY	CK	OP6	ST5				BY	D	A,B → D	1 → ST0
3			BX	DR	ST2	ST7				BX	D	A,B → D	0 → ST1
4			FR		ST4	D=0				FR	D	A+B → DC	1 → ST1
5			KL		ST6	A → X				KL	D	A+B+1 → DC	0 → ST2
6			DL		File	File				DL	D	A+B+C → DC	DNST21
7			DH		CK → WIO → X6	SERVO				DH	D	A → B → D	0 → ST3
8			OP		Carry	SORSR				OP	D	A-B → D	1 → ST3
9			GP		COMMO	SELTO				GP	D	A-B+1 → D	0 → ST4
10			UR		SUPPO	OP1				UR	D	A-B → D	0 → ST5
11			DW		Unused	OP3				DW	D	A → B → D	1 → ST5
28	12		SC	DR	OP0	OP5				DR	D	A-B → DC	0 → ST6
29	13		FS	ER	OP2	Index				FS	D	A-B+1 → DC	1 → ST6
30	14		OA	IE	OP4	OP7				FC	D	A-B+C → DC	0 → ST7
31	15		IS	IH					IG	D	A → B → D	1 → ST7	

- Machine Reset**  
2841 Clock 2
- D Select module 0, tape word A, tape 04 as indicated by START ADDRESS switch. Decode CA, CA alternate and CB fields.
  - A Gate A and B busses to ALU. Set and reset CC, CV and CB field latches. Start ALU operation.
  - B Remove reset from CC, CV and CB field latches complete ALU operation, Answer is now on the D buss.
  - C Sample D buss for zero. Set carry latch if a carry is detected.
  - D Perform CD, CH and CL field operations. Read next word from TROS. Decode CA, CA alternate and CB fields from new TROS word.
- A-C Same as above.

Note: The recycle latch causes the microprogram to alternate between this microblock and the GP register for the X address. 004, 000, 004, 001, 004, 002, 004 etc.

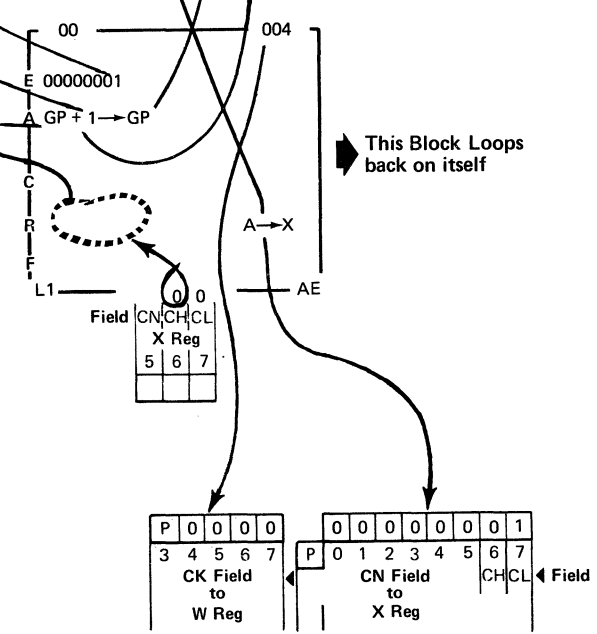


Figure 2-48b. Module 0 Address Scan Timing and TROS Fields

16431



TYPICAL MICROBLOCK STATEMENTS

Leg Identifier

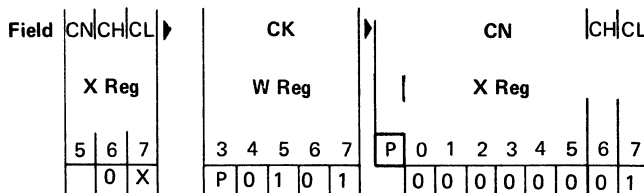
How You Got Here.....

- 1 The Leg Selector in the previous microblock contained a 0X branching condition. Since the X address for this block contains 01 the CL field in the previous tape contained a 1 → X7 statement.

Hex Address

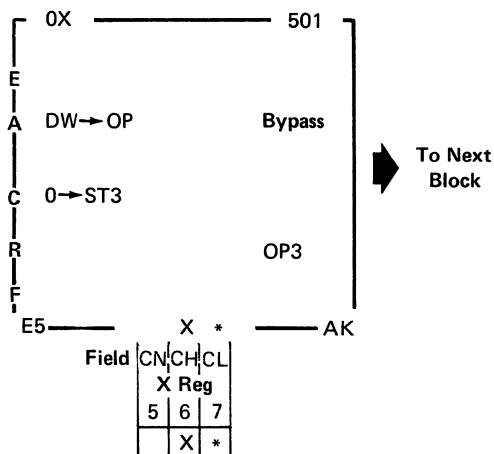
Where You Are.....

- 2 This is TROS module 5, tape word A, tape 01.



What You Do Here.....

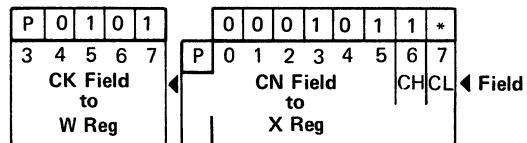
- 3 A. The DW → OP Bypass statement gates the contents of the DW register to the A register via the B buss. From the A register this data is gated to the Op register Via the D buss BYPASSing the ALU. ALU does perform the normal parity check.
- C. The 0 → ST3 statement resets the ST3 bit.
- R. If the OP3 bit is 1, set X7 to 1, If the OP3 bit is 0, set X7 to 0.



Leg Selector

Where You Are Going.....

- 4 The next microblock is located in module 5 (W register is unchanged). The X register is either 16 or 17 depending on the OP3 bit. Since X6 is a 1 this CH field contained a 1 → X6 statement.



16432

Figure 2-49a. ALU Bypass, ST3 Reset and X7 Branch

**Leg Identifier**

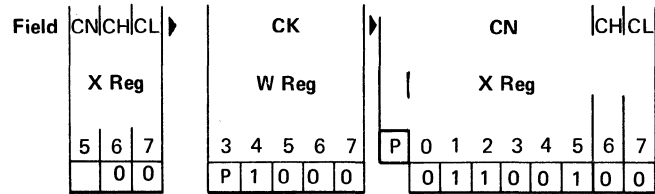
**How You Got Here.....**

- 1 The Leg Selector in the previous microblock contained a 00 branching condition.

**Hex Address**

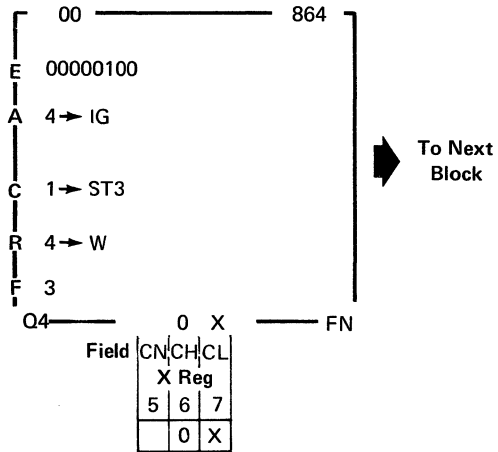
**Where You Are.....**

- 2 This is module 8, tape word A, tape 36.



**What You Do Here.....**

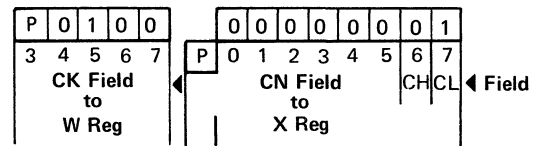
- 3 E. The CK field contains the value 4.
- A. The 4 → IG statement gates the contents of the CK field to ALU via the B buss, and transfers the data from ALU to the IG register.
- C. The 1 → ST3 statement sets bit 3 in the ST register to a 1. This condition can be used by a future microblock as a branching condition.
- R. The 4 → W statement transfers the CK field to the W register. This transfer causes the microprogram to go to module 4 for the next TROS tape. NOTE that the CK field was used twice by this microblock.



**Leg Selector**

**Where You Are Going.....**

- 4 The next microblock is located in module 4 and X6 must be a 0 (4 → W sets X6 to 0). The remainder of the X register (X0 through X5 and X7) is controlled by the CN and CL fields. By looking at the next microblock it can be determined that the CN field on this tape (864) contains zeros, and that the CL field contains a 1 → X7 statement. Thus, the 0X in the Leg Selector is not accurate. The actual condition is 01 which gives a truer indication of the address of the next microblock.



16433

Figure 2-49b. CK Field to IG and W Registers and ST3 Set

**Leg Identifier**

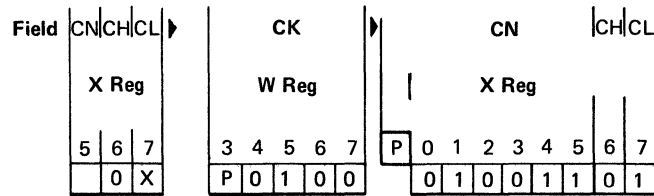
**How You Got Here.....**

- 1 The previous microblock contained a 0X branching condition. The 40 X address indicates that the CL field is the previous microblock contained a 1→X7 statement.

**Hex Address**

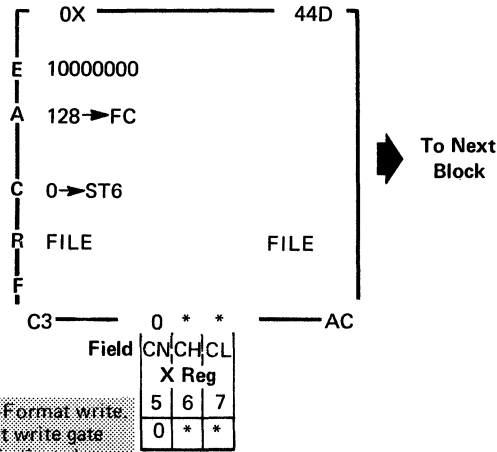
**Where You Are.....**

- 2 This is module 4, tape word B, tape 13.



**What You Do Here.....**

- 3 E. The CK field contains the value 128.
- A. The 128→FC statement and CN5 = 0 indicates that bit 0 in the FC register is reset.
- C. The 0→ST6 statement sets ST6 to a 0.
- R. The FILE, FILE statement is a 4-way branch depending on the selected file interface.
  - 000 = 2302
  - 001 = 2311
  - 010 = 2303
  - 011 = 2321



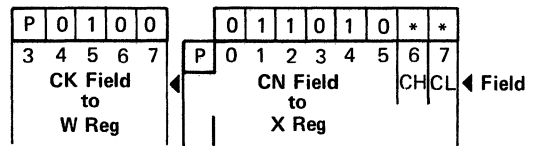
The note contains added information on the 128→FC and 0→ST6 statements.

Non-Format write  
Reset write gate  
and indicate by  
resetting ST6.

**Leg Selector**

**Where You Are Going.....**

- 4 The next microblock is in module 4. The X address can be 68, 69, 6A or 6B as determined by the FILE, FILE branch.



16434

Figure 2-49c. FC Register Reset, ST6 Reset and 4-Way Branch (X6 and X7)

**Leg Identifier**

**How You Got Here.....**

1

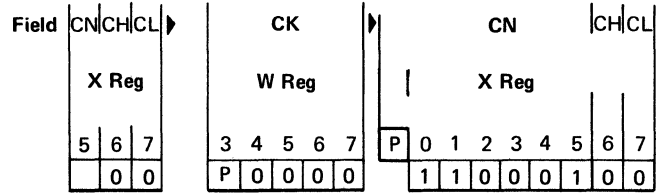
The Leg Selector of the previous block contained either a 00 branch or X register bits 6 and 7 were set to 00 by 0 →X6 and 0 →X7 statements.

**Hex Address**

**Where You Are.....**

2

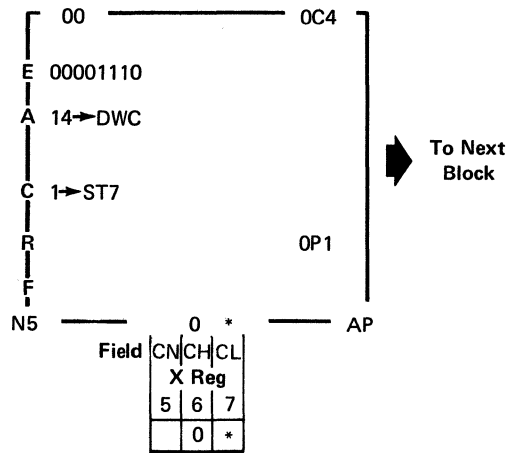
This is TROS module 0, tape word B, tape 123.



**What You Do Here.....**

3

- E. The CK field contains 14.
- A. The value in the CK field is to be transferred to the DW register. Since there is no carry from this operation, the C statement resets the ST3 bit.
- C. The 1 →ST7 statement causes the ST7 bit to be turned on. This function will be used as a branching condition later on in the microprogram.
- R. The OP1 statement causes the microprogram to branch if OP1 is set to a 1. This is one of the conditions that you must keep track of when using CAS logic.

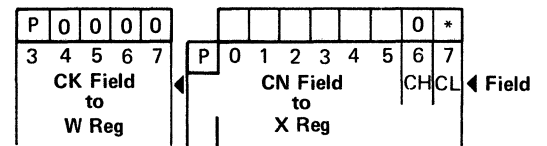


**Leg Selector**

**Where You Are Going.....**

4

If OP1 is set the microprogram branches to 01. If OP1 is zero (reset) the microprogram branches to 00. The X6 bit is a 0 as a result of a 0 →X6 statement in the CH field.



16435

Figure 2-49d. ST3 (Carry) Reset, ST7 Set and X7 Branch

*Leg Identifier*

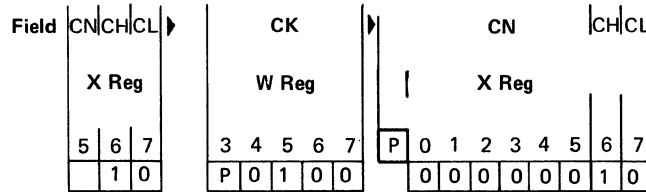
How You Got Here.....

- 1 The previous block contained a double branch in the Leg Selector. This block indicates that a branch was made on the CH field. (Remember that the branching statements could be 1→X6 and 0→X7 for this block.)

*Hex Address*

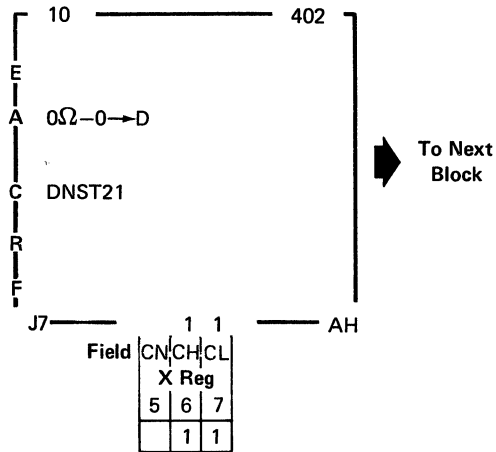
Where You Are.....

- 2 This is TROS module 4, tape word A, tape 02.



What You Do Here.....

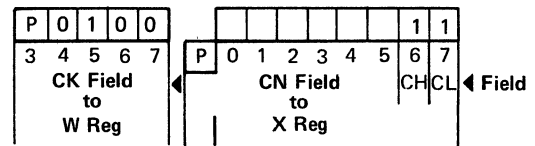
- 3 A. This statement indicates that the A buss is 0Red with the complement of the B buss. Since no registers are gated to these busses, both contain zeros. The complement of Hex 00 is Hex FF. Thus, the buss is non-zero.  
 C. This statement asks if the D buss is non-zero. Since the D buss contains Hex FF, ST2 is set to 1.



*Leg Selector*

Where You Are Going.....

- 4 The Leg Selector Bits indicate that the next address must be 3, 7, B or F. The CH and CL fields are punched with 1→X6 and 1→X7 statements.



16436

Figure 2-49e. DNST21: Forcing the D Bus to FF to Enable Setting ST2



**X ADDRESS MODIFICATION FROM A BUSS**

*Leg Identifier*

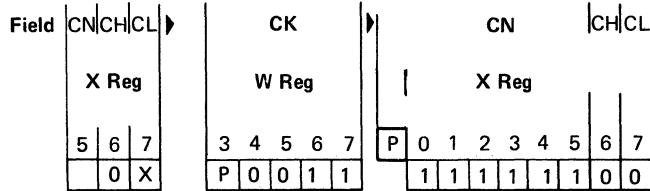
**How You Got Here.....**

- ① The previous microblock contained either an X6 branch or a 0→X6 statement.

*Hex Address*

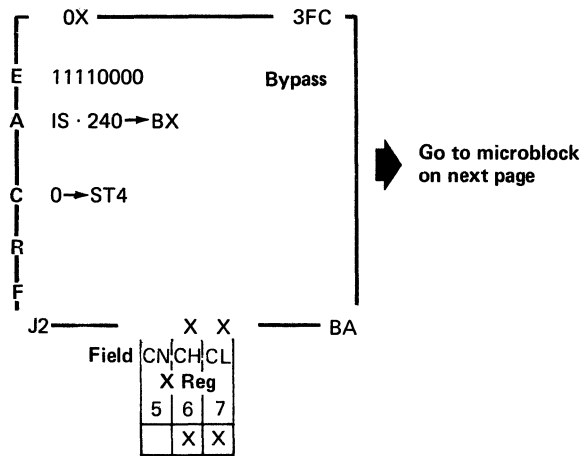
**Where You Are.....**

- ② This is TROS module 3, tape word B, tape 67.



**What You Do Here.....**

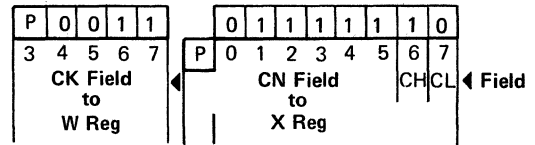
- ③ E. The CK field contains 240.
- A. The contents of the IS register are gated to the A buss (assume the IS is AA) and the contents of the CK field are gated to the B buss. ALU ANDs the A and B busses and transfers the answer to the BX register via the D buss.
  - IS = 10101010 = AA
  - CK = 11110000 = FG
  - 
  - BX = 10100000 = A0
- C. The 0→ST4 statement resets the ST4 bit.



*Leg Selector*

**Where You Are Going.....**

- ④ There are no branching conditions to be met in this microblock. The W register remains at 3 and the CN field in this tape contains new data for X register bits 0 through 5. X register bits 6 and 7 may or may not be changed by the CH and CL fields.



16438

Figure 2-50a. ANDing the IS Register and CK Field

**Leg Identifier**

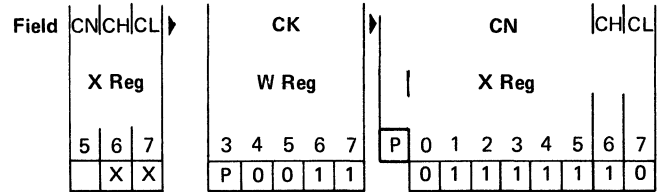
**How You Got Here.....**

- 1 The previous microblock modified the X register with the contents of the CN field and placed 10 (via CH and CL statements) in X6 and X7.

**Hex Address**

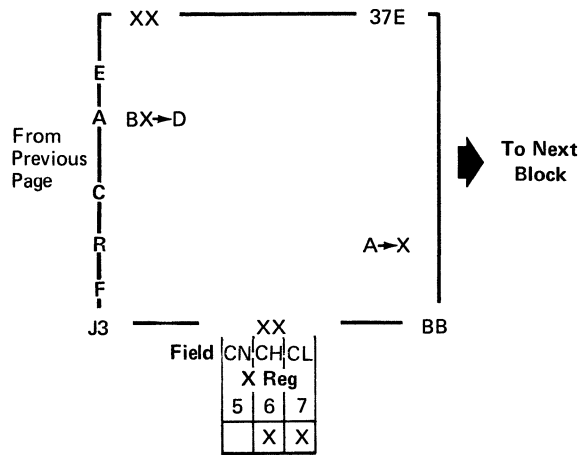
**Where You Are.....**

- 2 This is TROS module 3, tape word B, tape 62.



**What You Do Here.....**

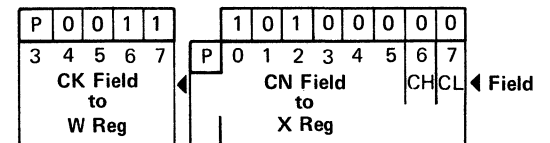
- 3 A. The BX→D statement gates the contents of the BX register (A0 as set in the previous microblock) to the D buss.
- R. The A→X statement transfers the contents of the A register to the X register. Because of the BX→D statement the A register contains A0. Thus, the address for the next microblock is Hex 3A0.



**Leg Selector**

**Where You Are Going.....**

- 4 The contents of the W register are unchanged and the X register contains the Hex address A0. Note that the A→X statement transfers A register bits 0 through 7 to X register bits 0 through 7.



16439

Figure 2-50b. A Bus to X Register Transfer



USING CN5 BIT TO SET FT REGISTER BITS

Leg Identifier

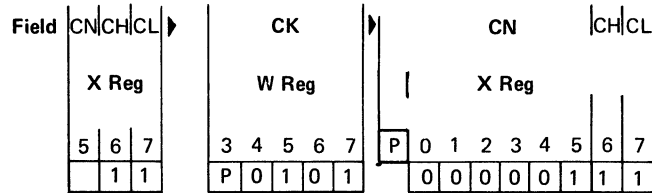
How You Got Here.....

- ① The Leg Selector in the previous microblock contained a 11 branching condition.

Hex Address

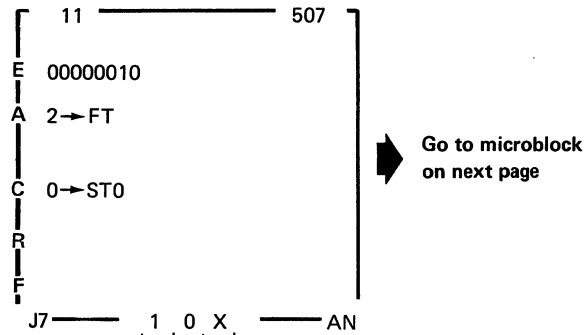
Where You Are.....

- ② This module 5, tape word A, tape 7.

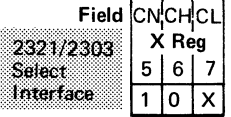


What You Do Here.....

- ③ E. The CK field contains the value 2.
- A. The 2→FT statement and CN5 = 1 indicates that bit 6 of the FT register is to be set.
- C. The 0→ST0 statement sets ST0 to a 0.



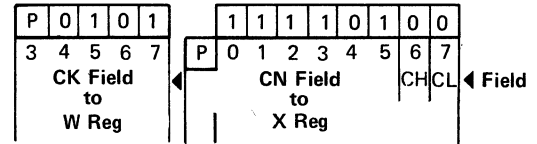
This note and the 2→FT statement indicate that the 2321 or 2303 interface is to be selected.



Leg Selector

Where You Are Going.....

- ④ The next microblock is in module 5, the X address is F4. The Leg Selector for this microblock shows that CN5 in the next microblock is a 1 and that the CH field for this block contains a 0→X6 statement. By looking at the address in the next block (next page) it can be determined that the CL field for this block contains a 0→X7 statement.



16440

Figure 2-5 1a. Selecting 2321 or 2303 Interface (FT2 Bit)

**Leg Identifier**

**How You Got Here.....**

1

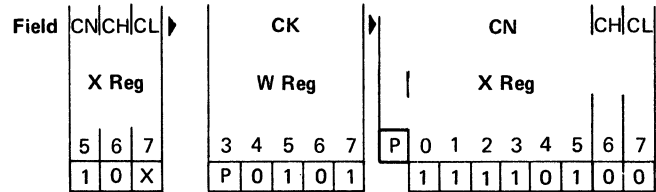
The Leg Selector in the previous microblock contained a 10X branching condition. Since the X address for this tape is 04 the CH field on the previous tape contained a 0 → X6 statement and the CL field contained a 0 → X7 statement.

**Hex Address**

**Where You Are.....**

2

This is module 5, tape word B, tape 75.

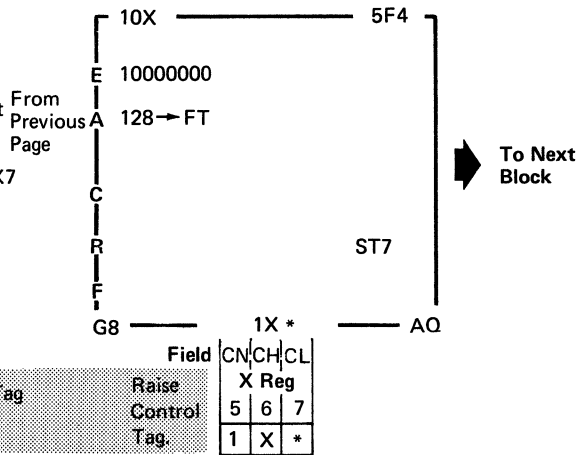


**What You Do Here.....**

3

E. The CK field contains the value 128.

- A. The 128 → FT statement and CN5 = 1 indicates that bit 0 of the FT register is to be set.
- R. The ST7 statement sets X7 to a 1 if ST7 is a 1, or sets X7 to a 0 if ST7 is a 0.



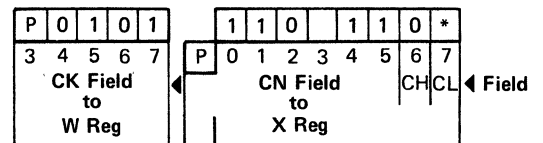
This note and the 128 → FT indicate that the Control Tag was raised by this microblock.

**Leg Selector**

**Where You Are Going.....**

4

The next microblock is located in module 5, the X address is CC or CD as determined by the ST7 branch.



16441

Figure 2-51b. Raising the Control Tag (FT0 Bit)

MACHINE SYNCHRONIZATION AND PROGRAM DELAYS

Leg Identifier

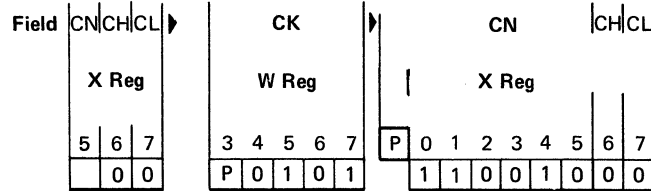
Hex Address

How You Got Here.....

Where You Are.....

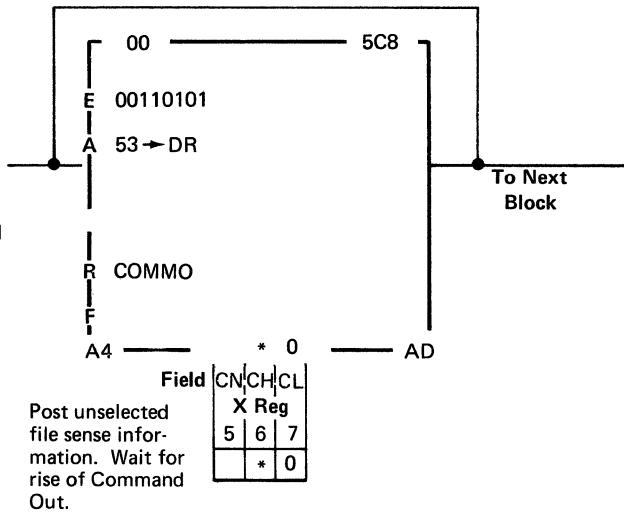
1 The previous microblock contained a 00 branch in the Leg Selector.

2 This is module 5, tape word B, tape 119.



What You Do Here.....

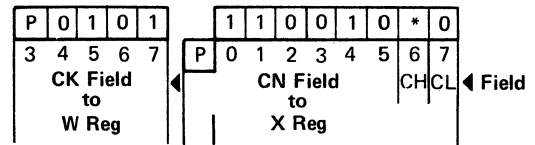
- 3 E. The CK field contains the value 53.
- A. The 53 → DR statement transfers the contents of the CK field to the DR register via the D bus. Note: Remember that this is a constant value.
- R. The COMMO statement checks for the rise of Command Out. If Command Out is detected, X6 is set to a 1, if not X6 is set to a 0.



Leg Selector

Where You Are Going.....

4 This microblock synchronizes the 2841 and CPU operations. The address of the next microblock is identical to the address of this block except for the X6 bit. As long as Command Out is not detected, the microprogram returns to this block. Command Out sets X6 to a 1 and allows the microprogram to branch to address 5CA. Observe that regardless of the number of times the microprogram loops on this block the contents of the DR register remain at 53 (see A. above).



16442

Figure 2-52a. Synchronizing 2841 Operations to Command Out from the CPU

**Leg Identifier**

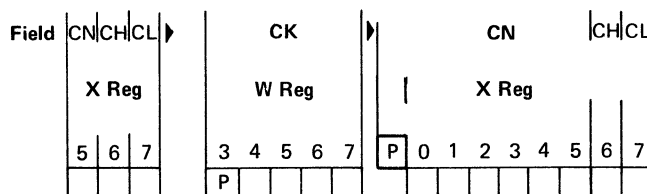
**How You Got Here.....**

- 1 The Leg Selector of the previous microblock contained a 11 branch.

**Hex Address**

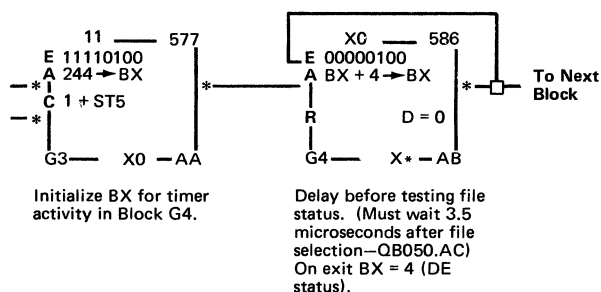
**Where You Are.....**

- 2 The first block is module 5, tape word A, tape 55. The second block is module 5, tape word A, tape 121.



**What You Do Here.....**

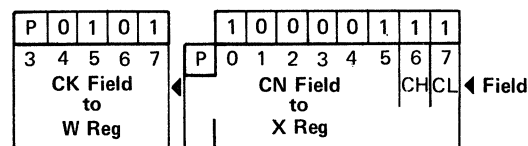
- 3 E. The CK field contains the value 244.
- A. The 244 → BX statement sets the BX register to 244 (F4).
- C. The 1 → ST5 statement sets the ST5 bit to a 1.
- E. The CK field contains the value 4.
- A. The BX + 4 → BX statement adds 4 to the contents (244) of the BX register.
- R. The D = 0 statement checks the D buss for 00. If D = 0 the program branches to address 587, if D ≠ 0 the program loops on address 586.



**Leg Selector**

**Where You Are Going.....**

- 4 The purpose of the 2 blocks shown above is to delay execution of the program for a specific period of time (3.5 us).. This is accomplished by using a register (BX) in the 2841 as a counter and incrementing the register each time the program makes a pass through the register. By presetting the register, the programmer can determine the length of the delay. Each pass through the microblock requires 500 ns. Thus 3.5 us requires 7 passes. On the 6th pass the BX register contains 00. This is detected by the D = 0 statement on the 7th pass, and the BX register is incremented by 4 for the last time. The X7 bit is set to 1 and the program branches address 587.



16443

Figure 2-42b. Timing a Delay with the BX Register, CK Field and D=0 Statement



3.1 STATUS INFORMATION

- The status byte consists of eight bits.
- It is used to notify channel of the conditions of the 2841.
- All 2841 commands, with the exception of Seeks and Command Immediates, transmit two (initial and ending) status bytes to channel.
- Cylinder seeks and the restore commands transmit three bytes (initial, channel end, device end) to channel.
- Command Immediates (No-Op and Release) transmit one status byte (channel and device end in initial) unless they are chained after a write command. In this case, they transmit two (initial and ending).

The status byte contains information which reflects the status of the 2841 and the selected device attached to the 2841. The significance of each bit in the status byte is listed below:

Bit	Name	Note
0	Attention	Not used.
1	Status Modifier	Used with Search and Control Unit Busy.
2	Control Unit End	The Control Unit has finished an operation.
3	Busy	Addressed Access Mechanism is moving or used in conjunction with Status Modifier to indicate Control Unit Busy.
4	Channel End	The Control Unit has received all the data from the channel needed to do the operation called for and the channel is freed.
5	Device End	Indicates that an access mechanism is free to be used.
6	Unit Check	Indicates that a Control Unit or programming error or device hardware check has been detected.
7	Unit Exception	End-of-File.

A more detailed description follows:

Attention (Bit 0): Not Used.

Status Modifier (Bit 1): This bit is set whenever a search high, search equal or a search high or equal command has been executed and the condition satisfied.

The status modifier is also set whenever the 2841 is busy. This bit in conjunction with the busy bit signifies control unit busy.

Control Unit End (Bit 2): This bit is set if a control unit busy status has been generated previously and the busy condition has been terminated. Bit 2 is also set with unit check when unit check occurs after device end.

Busy (Bit 3): The busy bit may indicate either device busy or control unit busy:

1. **Device Busy:** The busy bit indicates that the selected device is busy. It will be set when a new command chain is initiated while the selected access mechanism is still in motion due to a previous seek command. Busy is also included in the response to any command except Test I/O if there is outstanding status for the device.
2. **Control Unit Busy:** The busy bit in conjunction with the status modifier bit indicates the control unit is busy. It will be set when a new command chain is initiated while the 2841 is causing a track to be erased following a format write command or an erase command. It is also set if an attached 2321 is addressed while performing an automatic strip restore.

Channel End (Bit 4): This bit is set when the channel to control unit operation is completed.

Device End (Bit 5): This bit indicates that an access mechanism is free to be used. After a seek or a restore command, device end is presented to the channel together with the unit address to indicate a seek complete. It is generated simultaneously with channel end at the end of all other commands. Device End is also generated when an attached device goes from a not ready to a ready condition.

Unit Check (Bit 6): This bit is set whenever an unusual or error condition on the selected device is

detected in the 2841. Sense bytes 0, 1 and 2 provide detailed information as to the nature of the condition. Channel end and device End are always presented with unit check unless the unit check is presented in initial selection sequence.

Unit Exception (Bit 7): This bit indicates that an end-of-file has been detected during a read IPL, read R0, read CKD, read KD, read D, write KD, write D or search-key-data operation. It is not set for read count, write CKD or search key or ID commands. Unit exception results from a data length of zero. The key field, if any, is transferred.

All 2841 commands result in two status bytes (initial and ending) with the following exceptions:

1. Immediate Commands: No-op and release are processed as immediate commands only if the control unit is not writing or erasing at the time the command is received (chained). If not writing or erasing, channel and device end are indicated in the initial status byte (one status byte only). If writing or erasing, zero is transmitted in the initial status byte. Channel and device end are indicated in the ending status byte when the 2841 finishes writing or erasing.
2. SEEK type commands: A seek (CCHH, or BBCCHH) that causes the access to move or a restore command results in three status bytes:
  - a. Initial
  - b. Channel end after data transfer from the CPU.
  - c. Device end after the device has stopped seeking (gated attention).
3. A third status byte may occur on write commands if channel has already accepted device end. This could occur, i.e., if the device went unsafe while completing a formatting write. In this case a status byte containing control-unit-end and unit check would be transmitted to channel via the polling interrupt sequence.

### 3-2. SENSE INFORMATION

Six bytes of sense condition information are provided by the 2841 to completely identify the setting of the unit check bit in the status byte. These six bytes are transferred to the channel by issuing a sense command.

#### 3.2.1 Sense Byte 0

Command Reject (Bit 0): This bit indicates that the 2841 has received an invalid operation code, an invalid sequence of commands, or an invalid seek

address. Detection of a bus-out parity with a command does not set command reject. If a write-file mask is violated, command reject is set along with file protect.

Intervention Required (Bit 1): This bit indicates that the specified device is:

- a. Not physically attached to the system.
- b. The specified device is physically attached to the system, but it is not available for use because the motor is not on, a cover interlock is open, etc.

After this sense bit is set the program may try the same command again but not another command without causing other errors.

Bus Out Parity (Bit 2): This bit indicates that a data parity error has been detected during the transfer of information from the channel to the 2841. This check is an odd redundancy check that occurs on control, write and search operations. The check is done by the 2841. A parity error detected during command transfer is a bus out check and not a command reject.

Equipment Check (Bit 3): This bit indicates that an unusual condition is detected in the control unit or device unit. The conditions that are covered by the bit are defined in Sense Byte 2.

Data Check (Bit 4): This sense bit indicates that a data error has been detected in the data received from the device during a read, search, space or clocking operation.

Overrun (Bit 5): This bit indicates that a service out signal was not received in the 2841 within a specified time allowed after service in or that a chained CCW was issued but that it was received too late to be properly executed. Detection of an overrun during reading or writing immediately stops data transmission. When writing, the remaining portion of the record area is padded out with valid zeros.

Defective Track (Bit 6): (Flag Byte-Track Condition Bit 6 = 1) - A Track condition check is generated for a defective track whenever:

1. Any read or search (except search HA, read HA, read R0) is attempted on the track in either multi-track or single track mode. The interrupt occurs prior to transmission of any data to or from the channel.
2. An overflow record being read, written, or searched overflows to a track flagged as defective. The interrupt occurs after the last byte on the previous track has been operated on and before the first byte for the defective track is

requested from or sent to the channel. In this case, overflow incomplete is also set. Sense byte 5 is also set to define the operation in process at the time of the interrupt.

Alternate Track (Bit 6): (Flag Byte-Track Condition Bit B7 = 1) - A track condition check is generated when command chaining and multiple track mode signals indicate that operations are to continue on the next higher-order track or the record is not the last segment of an overflow record. The track condition check indication inhibits the incremental head switching.

Seek Check (Bit 7): This bit indicates that the device has been unable to successfully complete a Seek due to:

1. The transferred seek address is outside the valid address boundaries of the device. The unused bytes must contain zeros. This condition also sets command reject.
2. Less than six bytes of seek address is sent. This condition also sets command reject.
3. Failure of hardware which results in the access mechanism failing to detent correctly.
4. On multi-track operations, the home address of the track advanced to does not compare with the physical address.
5. Seek check bit and missing address marks (bit 6) set when a 2321 is addressed indicate that sub cell 0 of a ballast cell has been accessed.

### 3.2.2 Sense Byte 1

Data Check in Count Field (Bit 0): This bit indicates that a data error has been detected in a count field read from the device. Data check in byte 0 is also turned on. Error detection is the same as described for data check (Byte 0, Bit 4). The operation is terminated at the end of the count field.

Track Overrun (Bit 1): This bit indicates that writing has not been completed by the time index point is detected. This type of error is detected during write-R0, write-count, key and data, write-key-and data, write data or space count operations.

If the bad record is read with subsequent read commands, the track overrun condition is not set.

End-of-Cylinder (Bit 2): This bit indicates that the CCW command chain has not been completed, but that end-of-cylinder has been detected.

Invalid Sequence (Bit 3): This bit indicates that an attempt has been made to execute an invalid sequence of CCW's. Invalid sequences are normally related to write operations. Invalid sequences also occur if two set file mask CCW's operations are attempted in the same chain of CCW's, if head switching is attempted without prior seeking, or if a space count is preceded by a write command. Command reject (Byte 0 - Bit 0) is also turned on when an invalid sequence is encountered.

No Record Found (Bit 4): The no record found function is included in the 2841 so that the programmer may use a sequence such as:

Search ID (MTM Off)  
TIC\* - 8  
Read Data

without the possibility of the program getting trapped in an endless loop in the event that the desired record is not contained on the track being searched. The no record found function occurs as follows:

1. An index passed condition is turned on whenever index point is sensed on the device.
2. The index passed condition is turned off whenever the 2841 performs a read operation in a HA or data field area, any write command, a sense command or any control command.  
The index passed bit is also reset when chaining is broken.
3. No record found condition occurs whenever the 2841 senses index point while performing a single track read or search operation other than read 0, or read HA and the index passed latch is already on.
4. A no record found condition occurs when Index is sensed while executing a space count command following HA and no address mark is found. A no record found condition occurs with missing address mark when neither HA or R0 can be found on the track.
5. A no record found condition and missing address mark (bit 6) occurring when a 2321 is addressed indicate:
  - a. a missed strip,
  - b. a strip that has not been initialized,
  - c. or a ballast cell other than sub cell 0 has been accessed.

The following programming notes apply:

1. Read CKD, read-key-data and read-data reset the index passed bit at the time the data field is



read from the track. Hence, No record found may occur while one of these commands is being executed; most notably, No record found will occur when one of these commands is given and there is no address mark detected on the track.

2. The programmer should insure that spurious no record found conditions cannot occur. For example, in the sequence:

```
Read Count
Search Key
TIC* - 16
Search ID (of Count Field read above)
TIC* - 8
Read Key Data
```

the index passed bit is not reset prior to the read key data command and index point is passed once after the key is located prior to orienting on the desired ID. If the index passed latch is on at the time the desired key was found (this cannot be predicted if the sequence was started with random orientation), then no record found condition will occur. The sequence may be corrected by inserting a read HA or Read R0 immediately prior to the search ID command (this is the best method since the added command will also eliminate unnecessary search ID sequences between the located key and the end of the track) or a no-op may be inserted. Also a read HA or read R0 could be included at the beginning of the sequence.

File Protected (Bit 5): This bit indicates that a seek or write CCW or MTM read or search command was issued that violated the file mask. The command reject bit is also set on detection of this condition if a write file mask is violated.

Missing Address Marks (Bit 6): A missing address mark is detected during the execution of any command or chain of commands which operate on successive count fields on a track. The detection is accomplished by identifying that two successive records on a track have equal bit conditions in bit 0 of the flag bytes. Under normal conditions, bit 0 of the flag byte is always a zero for all even-numbered records and is always a one for all odd-numbered records.

Upon detection of a missing address mark, bit six of sense byte one (missing address mark) will be turned on for all commands or chained commands except search ID CCW's. The search ID CCW is

used to pass over the missing address mark so that the remaining data on the track can be retrieved.

Overflow Incomplete (Bit 7): This bit is used with the optional record overflow feature. It is set as follows:

1. Overflow to a bad track—Set overflow incomplete and track condition check.
2. Overflow from an alternate track—Set overflow incomplete and track condition check.
3. Overflow to file protected boundary—Set overflow incomplete, file protected.
4. Overflow to wrong track—Head number compares unequal—Set overflow incomplete and seek check.
5. Overflow to end of cylinder—Set overflow incomplete and end of cylinder.

### 3.2.3 Sense Byte 2

Unsafe (Bit 0): This bit is used to indicate that a device malfunction has been detected. Some of these malfunctions are:

- More than one head has been selected.
- The device is trying to read and write at the same time.
- The write gate is Off and write driver is On.
- The write gate is On and the writer driver is Off.
- The erase driver is Off and the erase gate is On.
- The erase driver is On and the erase gate is Off.
- One of the DC file voltages has been lost (2311 only).

Bit 1: Reserved

Serializer/Deserializer Check (Bit 2): This bit indicates that a bit has been either lost or gained when the parallel channel data is converted to serial data during a write operation.

Bit 3: Not Used

2841 ALU Check (Bit 4): The microprogram has detected an impossible condition, indicating an equipment malfunction. This check is made only on the BYPASS microprogram statement. The 4 bit is turned on if the A register P bit and the ALU P bit are not the same.

Unselected Status (Bit 5): This bit indicates that some bit in the file status lines is on without any module being selected. This indicates a device malfunction of some kind since no bit should be on prior to selection.

**Bit 6: Reserved**

**Bit 7: Reserved**

**3.2.4 Sense Byte 3**

Byte 3	2311	2321	2302	2303
0	Ready	Drive Ready	Access Ready	Drum Ready
1	On Line	Drive Operative	Access Operative	Drum Operative
2	Unsafe	Read Safety	Read Safety	Read Safety
3	-----	Write Safety	Write Safety	Write Safety
4	On Line*	Strip Ready	On Line*	On Line*
5	End of Cylinder	Invalid Address	-----	
6	-----	Auto Restore	-----	
7	Seek Incomplete	CE Cell Located	CE Cylinder Located	

\*Forced On Line

22452A

**3.2.5 Sense Byte 4**

This byte is all zeros. It is included for compatibility with other control units.

**3.2.6 Sense Byte 5**

This byte is zero at all times except when overflow incomplete occurs (Byte 1, Bit 7). Information on the bit meanings is given in Chapter 5 - Record Overflow.

Sense Information Summary (Continued)

Status Byte Condition	Sense Bit Condition	Sense Bit Position
Unit	Track Overrun, Indicated on Write	Bit 1
Check	End-of-Cylinder	Bit 2
(Cont)	Invalid Sequence-also causes Command Reject (Byte 0, Bit 0) to be turned on	Bit 3
	No Record Found	Bit 4
	File Protected-also causes Command Reject (Byte 0, Bit 0)	Bit 5
	Missing Address Marker	Bit 6
	Overflow Incomplete	Bit 7
Unsafe	Also turn on Equipment Check Byte 0, Bit 3	Byte 2, Bit 0
Not Used		Bit 1
Serializer/Deserialzer Check		Bit 2
Not Used		Bit 3
2841 ALU Check		Bit 4
Unselected Status		Bit 5

22454

Sense Information Summary

Status Byte Condition	Sense Bit Condition	Sense Bit Position
Unit	Command Reject-includes Invalid Command, Invalid Sequence, & File Protected	Byte 0, Bit 0
Check	Intervention Required	Bit 1
	Bus Out Parity	Bit 2
	Equipment Check	Bit 3
	Data Check	Bit 4
	Overrun	Bit 5
	Track Condition Check	Bit 6
	Seek Check	Bit 7
	Data Check in Count Field-also causes Byte 0, Bit 4 (Data Check) to be turned on	Byte 1, Bit 0

22453

**3.3 MISCELLANEOUS OPERATIONS**

**3.3.1 Multiple Track (M/T) Operation**

The 2841 can automatically select the next sequentially numbered head on an access mechanism under control of B0 of the command byte. Head switching will not take place at index point if B0 is a 0. Head switching will take place at index point if B0 is a 1. A seek CCW must be given in each chain of commands in which a M/T command is given.

The M/T bit is recognized on all read and search commands. Therefore, a certain amount of discretion should be used when making B0 a 1-bit. For example, if during a search operation the M/T bit is a 1 and index is encountered before the search condition is satisfied, the head is automatically switched to the next track. The operation continues

until the end-of-cylinder is detected. This condition can occur if the search was initiated beyond the point where the record was located on the track. On the other hand, by correctly utilizing the M/T bit, it is possible to search a complete cylinder of ID's or keys.

Each time head switching occurs, the units cylinder and head number (CHH) in the home address of the new track is read by the 2841. If the head number is incorrect, seek check is set.

### 3.3.2 End-of-File

The end-of-file indication is written by executing a write-count-key-and-data CCW that has a data length of zero indicated in the count area. Execution of the write-count-key-and-data CCW with a DL of zero, causes the 2841 to automatically write one byte of 0's in the data portion of the end-of-file record. The KL portion of the count area can either be zero or up to 255 bytes. If KL = 0, the end-of-file record contains the contents of the count area and the data area (one byte of 0's). If KL ≠ 0, the key whose length is specified by KL is written in the key area of the end-of-file record.

As a logical file is being read, the count area of the records is examined. Detection of a DL of zero in the count area causes a unit exception signal to be generated. The unit exception signal is always generated at the normal ending time of the read operation that was scheduled to be performed. No data from the data area is transferred.

NOTE: Key data is transferred.

The unit exception is possible during read IPL, read R0, read CKD, read KD, read D, write KD, write D, and search KD operations.

### 3.3.3 Defective Surfaces

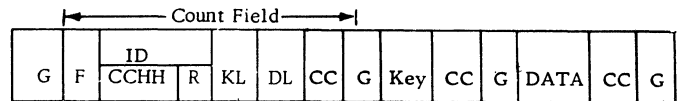
- Provision is made to continue a logical file of more than one track when a track with a defect is found.
- The defect must not be in the record zero area.
- The condition of the track and the alternate track are indicated in the flag bytes.
- The address of the alternate track is written in the record zero count field.

The 2841 has the ability to handle defective recording areas that may appear during the life of the storage

medium. The instrument that permits defective areas to be circumvented is the track descriptor record (R0). Implementation of the R0 concept is dependent upon the availability of a perfect recording area on each track that extends from the index point to the end of R0.

R0 is always the first record on the track following the home address. The schematic representation of R0 is:

#### Track Descriptor Record - R0



F = Flag Byte. Bits 6-7 of the flag byte are called the track condition bits and are used to determine the condition of the track. This condition code is propagated to all records on that track. The significance of the track condition bits is as follows:

- B6 = 0 = good track
- B6 = 1 = defective track
- B7 = 0 = not an alternate track
- B7 = 1 = alternate track

B0 of the flag byte is used internally by the 2841 to check for missing address marks. B1 is used for record overflow feature. B2 - B5 of the flag byte are not used.

ID = Identifier. The ID includes cylinder, head and record number. Cylinder number is two bytes in length. Head number is two bytes in length. Record number is 1 byte long and identifies the sequential position of the record on the track. The total ID is 5 bytes long.

KL = Key Length. The key length is 1 byte long and contains the length of the key area.

DL = Data Length. The data length specifies the number of bytes in the data portion of the record. DL is two bytes long.

CC = Code Check Bytes. This is a series of bits used for error detection purposes. CC is two bytes long.

G = Gap. The gap separates the various areas associated with the record.

K = Key. The key area is used to identify the data area.

D = Data. This is the information associated with the record. The data area can be variable in length.

Note that an R0 type record is not preceded by an address marker.

Read-R0 and write-R0 are special commands that are associated with the R0 function. Read-R0 operates the same as a read CKD with the exception that it never sets track condition. Write R0 operates the same as write CKD.

The R0 (alternate) approach to the defective area problem permits entire tracks to be repositioned independently of the way the file is organized, i. e. , random or sequential. In either case, the following conditions prevail:

1. Original track (good). In this case, the track condition bits (B6, B7) are set at 00.
2. Original track (defective). In this case the track condition bits are set to 10.
3. Alternate track (good). In this case the track condition bits are set to 01.
4. Alternate track (defective). In this case the track condition bits are set to 11.

The sequence of events that are required to move the data from a defective track to a good track is as follows:

1. Determine track is defective by repeated write and read-check operations.
2. If track is considered to be defective, assign alternate track.
3. Read as much information as possible from defective track into central processing unit.
4. In CPU change count portion of R0 of original track to address of alternate track.
5. Set flag byte to 10 and put flag byte and home address in core memory. Execute a write-home address command to change track condition bits. Chain to write R0.
6. Re-write new R0 on defective track. The balance of the track is erased.
7. Set ID (CCHH) of alternate track R0 count to equal the ID (CCHH) plus one of original defective track.
8. Set flag byte of alternate track home address to 01 to indicate alternate track.
9. Initiate seek to alternate track.
10. Command chain from seek to set file mask to write-HA to write-R0.

11. Copy data from original track onto alternate track. The count fields of records other than R0 are the same as they were on the defective track.

During normal processing runs, detection of a defective recording area and the selection of its alternate area could be accomplished in the following manner:

1. Assume access mechanism has been properly positioned and desired head selected.
2. Execution of a command causes the track condition bits to be examined.
3. If the track condition bits indicate that this track is defective, channel end, device end, and unit check (track condition check on sense) signals are generated.
4. The interrupt routine associated with R0 causes count (address of alternate track) to be read into core memory.
5. This address is used to select alternate track (seek operation).
6. At the completion of the seek operation, the access mechanism is positioned on the alternate track and the proper head selected.
7. It is now possible to process the sequence of instructions called for in item two.
8. If multiple track mode and command chaining operation is being used, channel end, device end and unit check occur at index time, and track condition occurs on a sense. The using system then issues a seek to the address of the original track plus one (found in R0 count field). Normal operation resumes when the desired track is reached.

The procedures described above apply when it is necessary to relocate an entire track and to process on a relocated track. It is also possible on sequentially organized data files, where the track is not preformatted, to handle defective areas as they are detected, thus eliminating the need to relocate an entire track unnecessarily.

One method that might be used in this instance is:

1. Write desired records on selected track.
2. Read-check track just written.
3. If error is detected, rewrite and read check several times to determine if defective area exists.
4. When defective area is found, search on last good ID or key and execute appropriate write commands. Execution of the last write command causes the remainder of the track to be erased.

### 3.3.4 Initial Program Load (00000010)

- Provides a method of setting a program into the CPU from an access mechanism.

An initial program loading (IPL) procedure is provided for the initiation of processing when power is turned On or when the contents of storage are not suitable for further processing.

The IPL procedure for random access devices is as follows:

1. The channel, control unit, and access mechanism from which the first IPL information is to be read are determined by setting the IPL load unit switches on the system console to the desired address.
2. Pressing the IPL key on the system console causes a complete system reset including all 2841 registers.
3. At the completion of the reset operation, the IPL hardware initiates a start I/O command and forms the initial CCW which is a read command (00000010) with the command chain bit on.
4. Execution of the read command causes the selected access mechanism to move to track zero (cylinder zero, head zero). A search for index point is initiated.
5. When index point is sensed, the microprogram causes home address and R0 to be skipped over and the data portion of record 1 to be read into core memory. This data is a PSW and two CCW's. The two CCW's that are read into core memory are used to control the progress of the read-in procedure.

### 3.3.5 File Protection

- Logical file areas are protected from inadvertent change by the use of set file mask commands.

File protection is accomplished by the logic circuits in the 2841 Storage Control and the checks within the control programs serving the system.

The 2841 portion of the file protection function utilizes set file mask commands and its associated controls.

The set file mask command is a control command whose bit structure is 00011111. Execution of a set file mask command causes one byte of data to be transferred from the channel to the 2841. At the completion of the transfer, channel end and device end signals are generated. The byte of data that is sent to the 2841 describes the write and seek functions that can be performed.

The significance of the file mask bits is:

B0	B1		
0	0	Inhibit Write Home Address and Write R0	
0	1	Inhibit <u>all</u> Write Commands	
1	0	Inhibit Write Home Address – Inhibit Write R0–Inhibit Write Count, Key, and Data	
1	1	Permit <u>all</u> Write Commands	
B3	B4		
0	0	Permit all Seek and Restore Commands	
0	1	Permit Seek CCHH & Seek HH CCW's	
1	0	Permit Seek HH CCW	
1	1	Inhibit <u>all</u> Seek Commands	
B2	B5	B6	B7
0	0	0	0

NOTE: For the 2841 Storage Control, B2, B5, B6 and B7 of the mask must be zero. If these bits are not zero, the mask is considered to be invalid and a unit check signal is generated. When a subsequent sense command is executed, a command reject is signaled.

A set-file-mask command can be issued any place within a CCW chain. At the completion of the CCW chain, the file mask is reset to all zeroes. A set-file mask command can only be issued once within any given CCW chain. If an attempt is made to issue more than one set-file-mask command with a given CCW chain, a unit-check signal is generated in the status byte. A subsequent sense command signals command reject and invalid sequence.

If a write command is issued that violates the file mask set, the write command is not executed, and a unit-check signal is generated in the status byte. A subsequent sense command signals command reject and file protect.

If a seek command that violates the file-mask set is issued, the seek command is not executed, and a unit-check signal is generated in the status byte. A subsequent sense command signals file protect.

A system reset or selective reset causes the file mask to be set to all zero's.

## 3.4 COMMAND FLOW CHARTS

Included in this section are 2841 command flow charts (Figures 3-1 thru 3-22). These charts present, in a logical fashion, the sequence which the 2841 goes through for a particular op code. Basic error checks are included. All op codes are not included, however, it should be realized that some

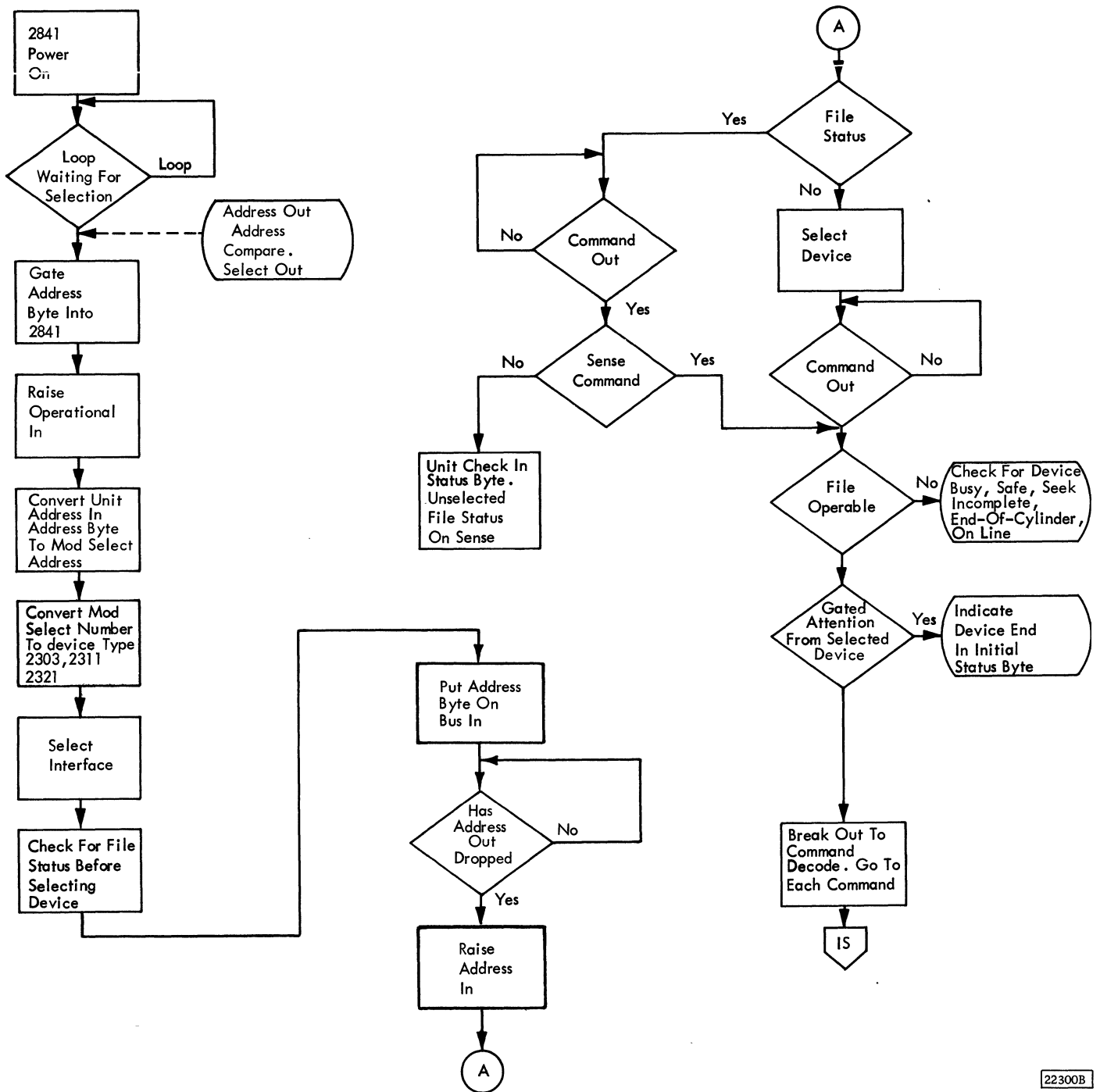


Figure 3-1. Initial Selection

commands differ only slightly, i. e. , a search-key-equal and a search-key-high command differ only in the area where the actual comparison occurs.

These charts are at a higher level than the individual microblocks on the CLD's.

To locate a routine in the CLD's refer to the Maintenance Diagram flow charts in the ALD's.

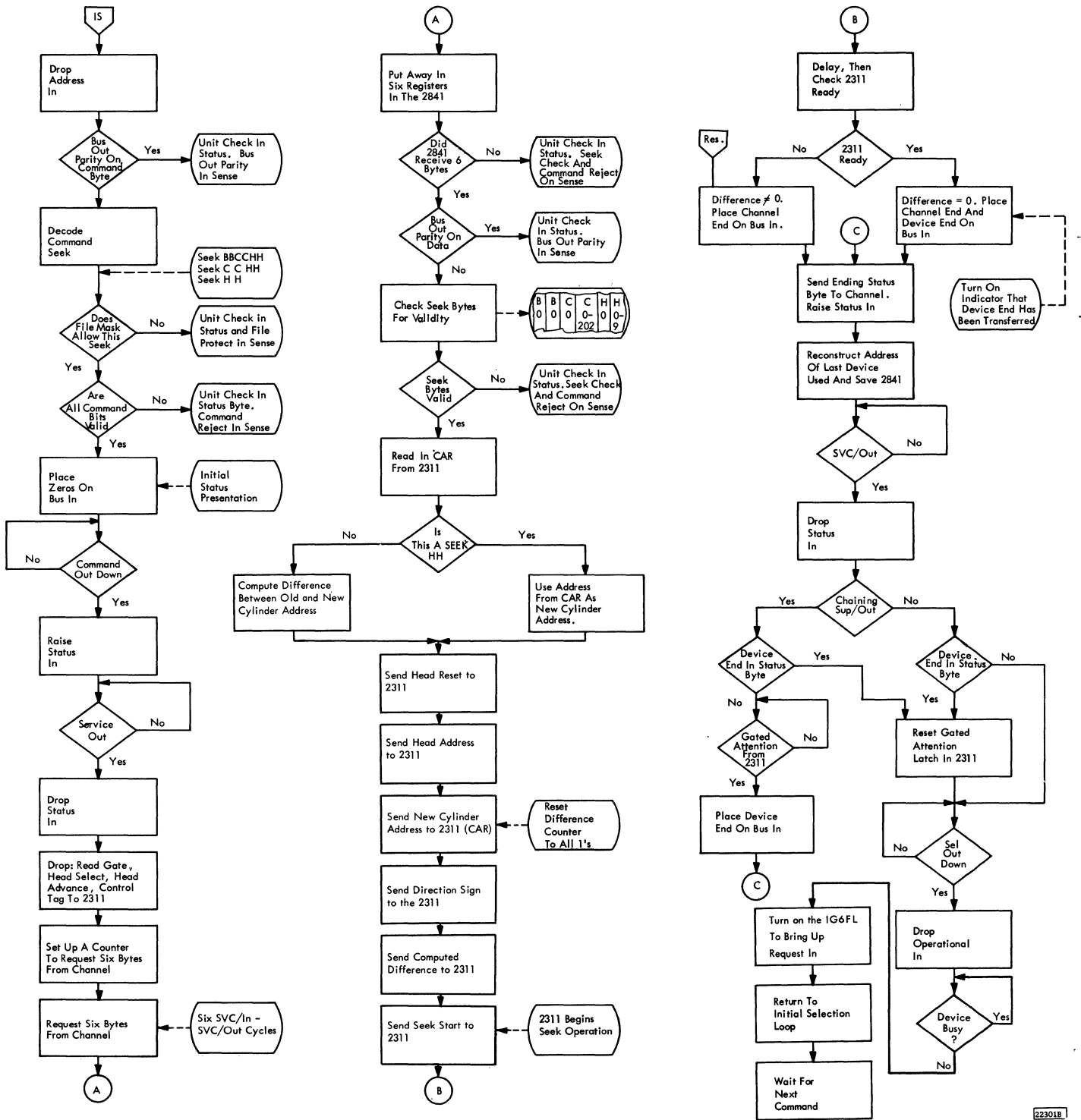


Figure 3-2. Seek - 2311

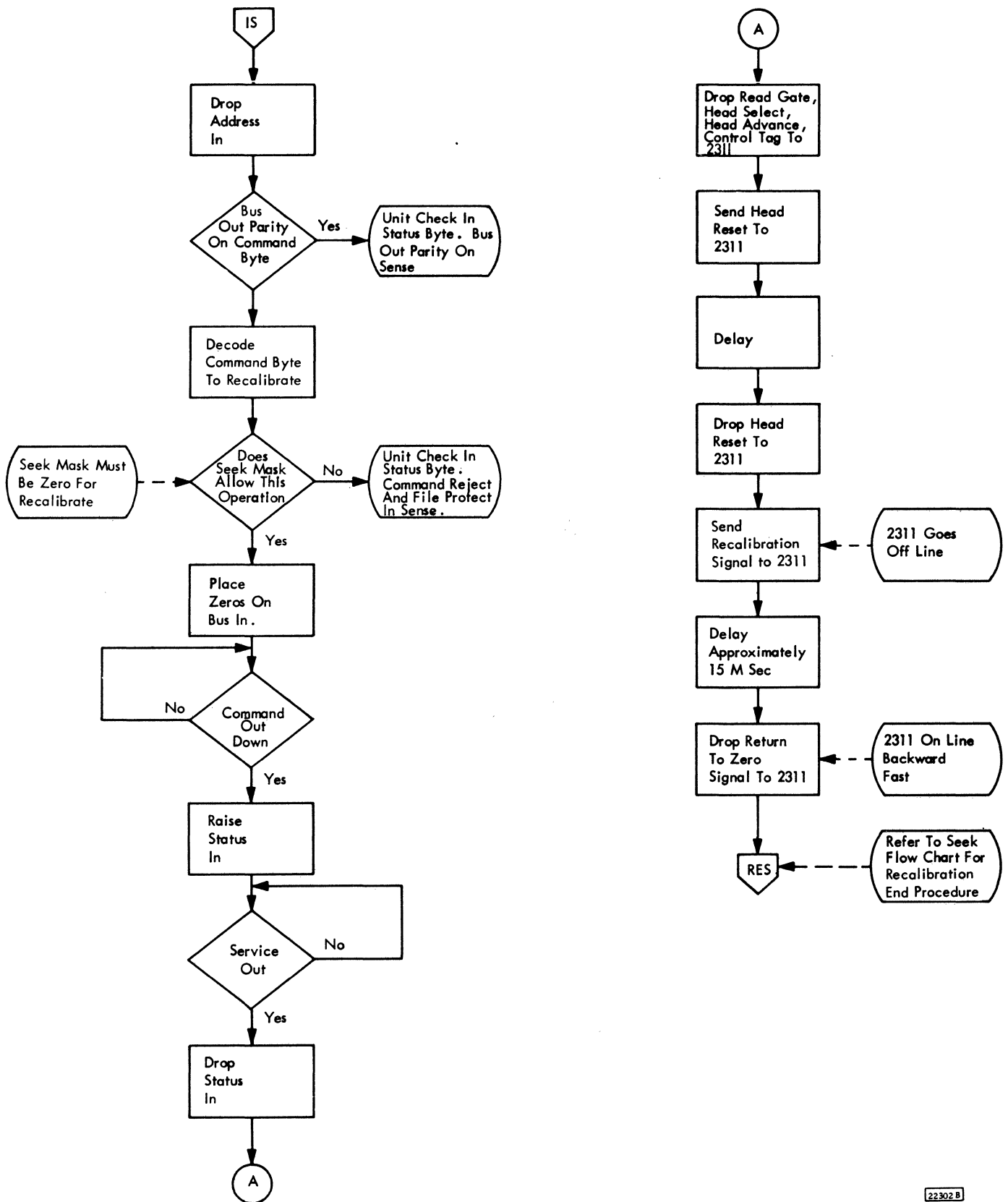
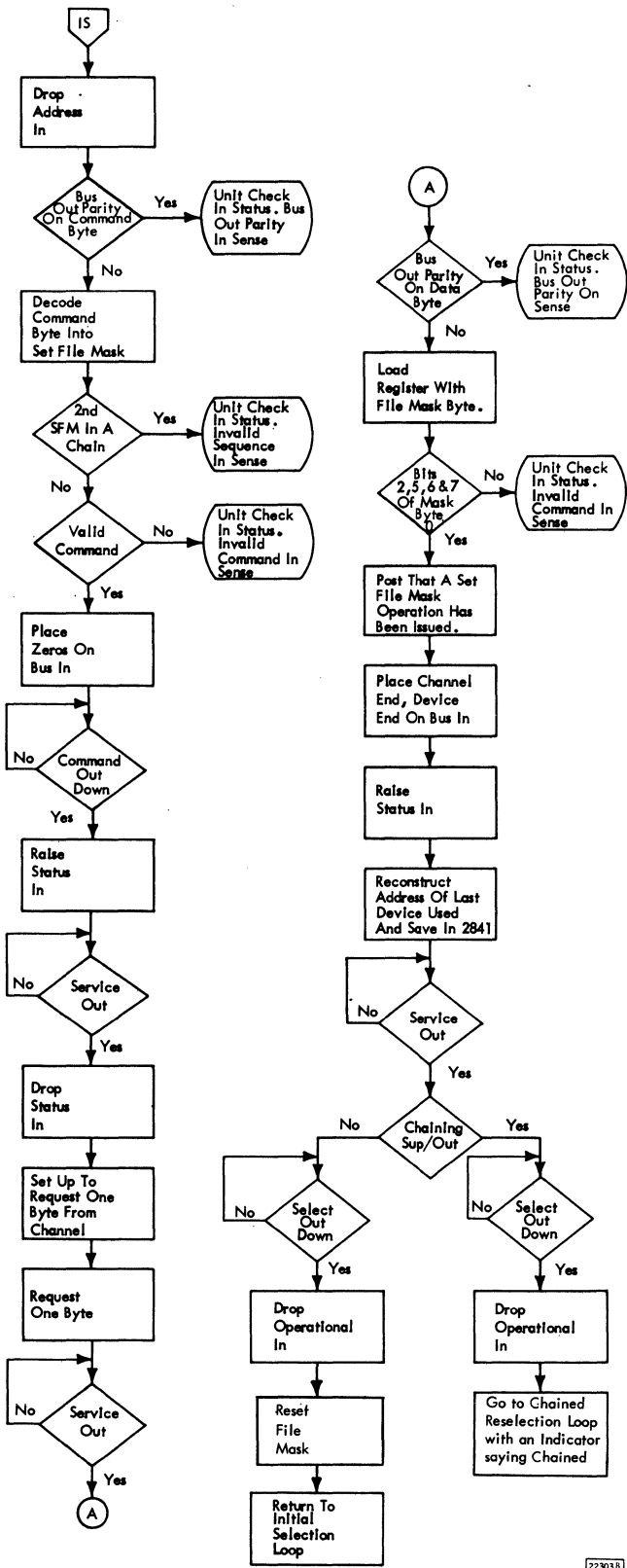


Figure 3-3. Recalibrate - 2311

22302 B





22303B

Figure 3-4. Set File Mask 2311

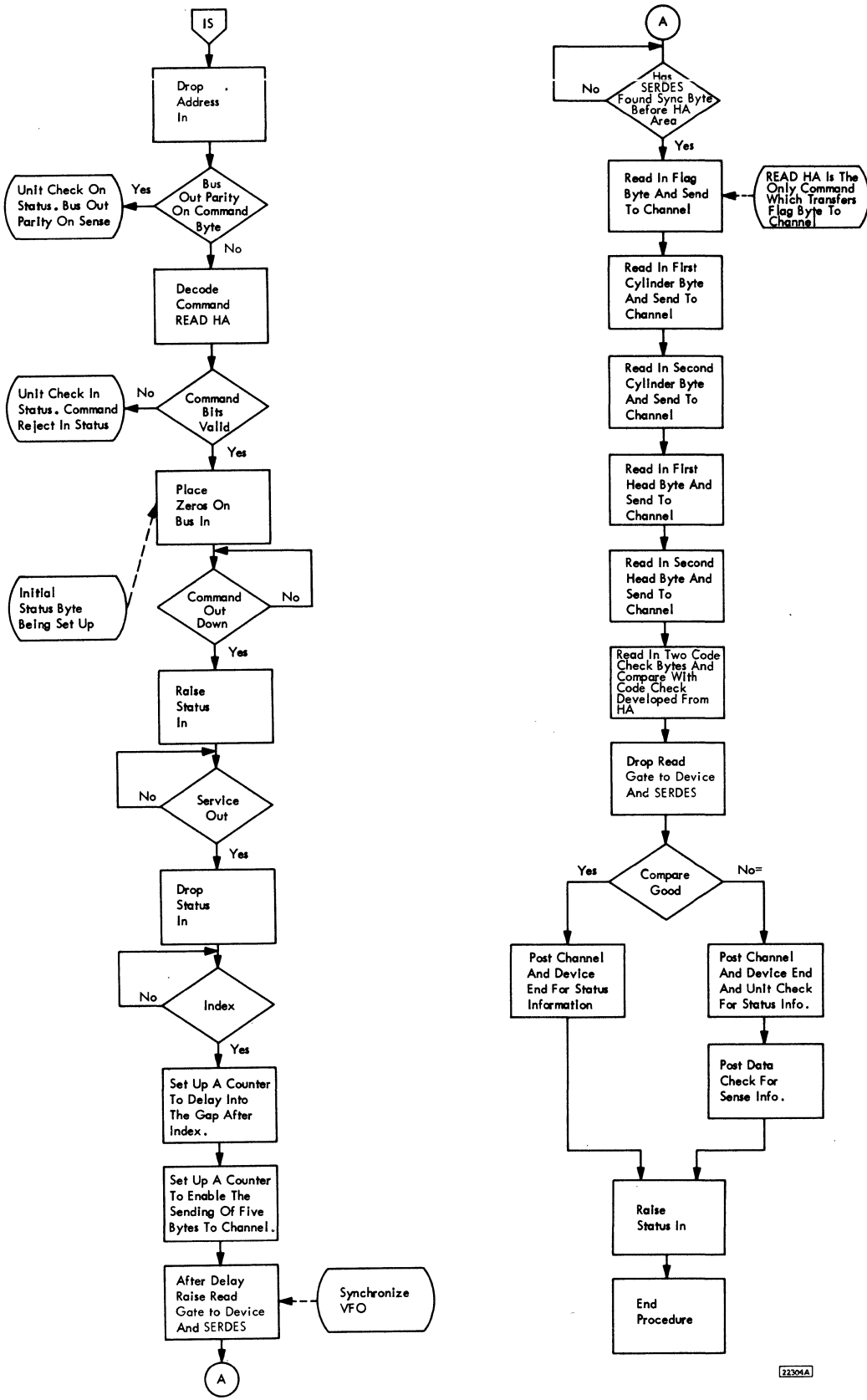
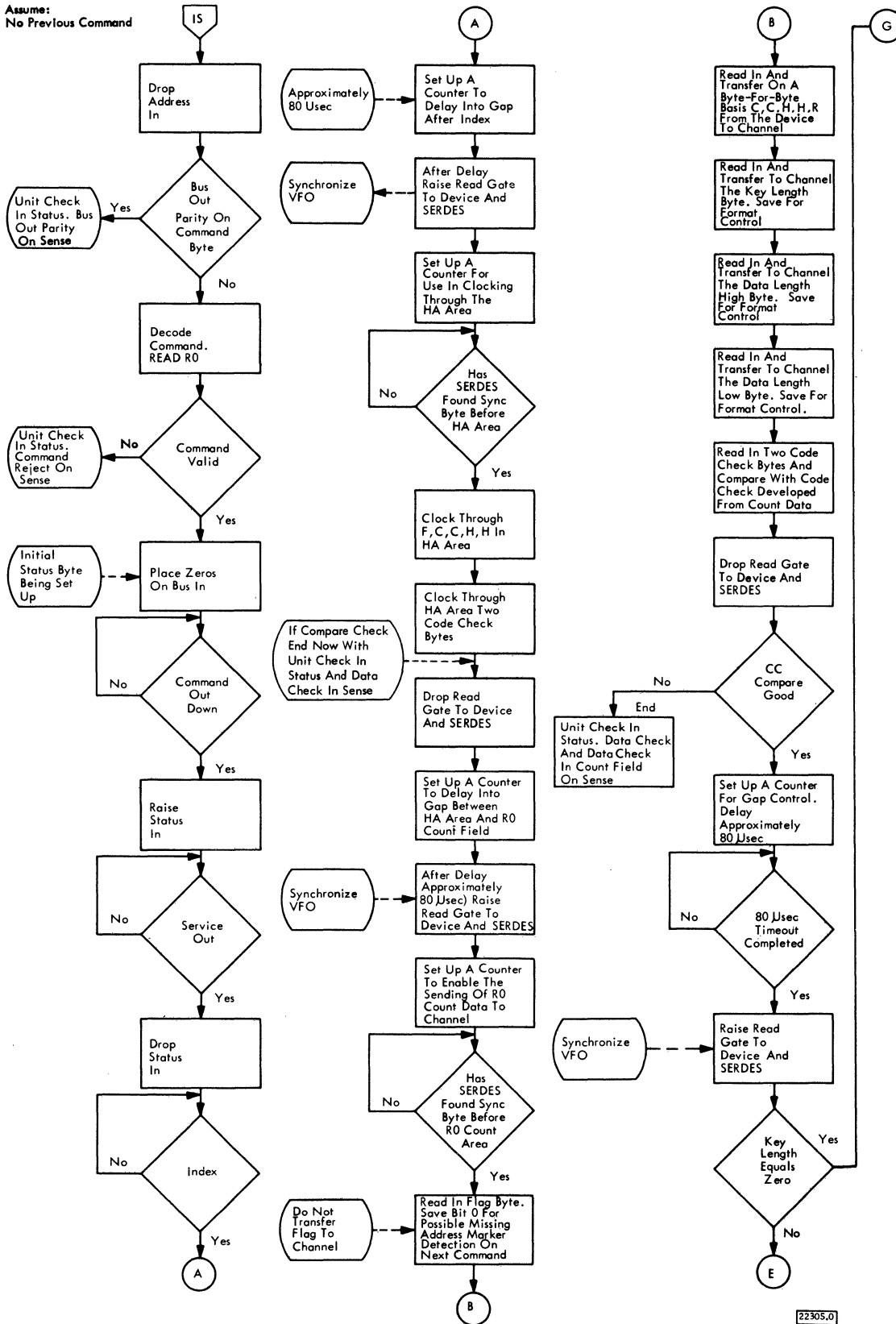


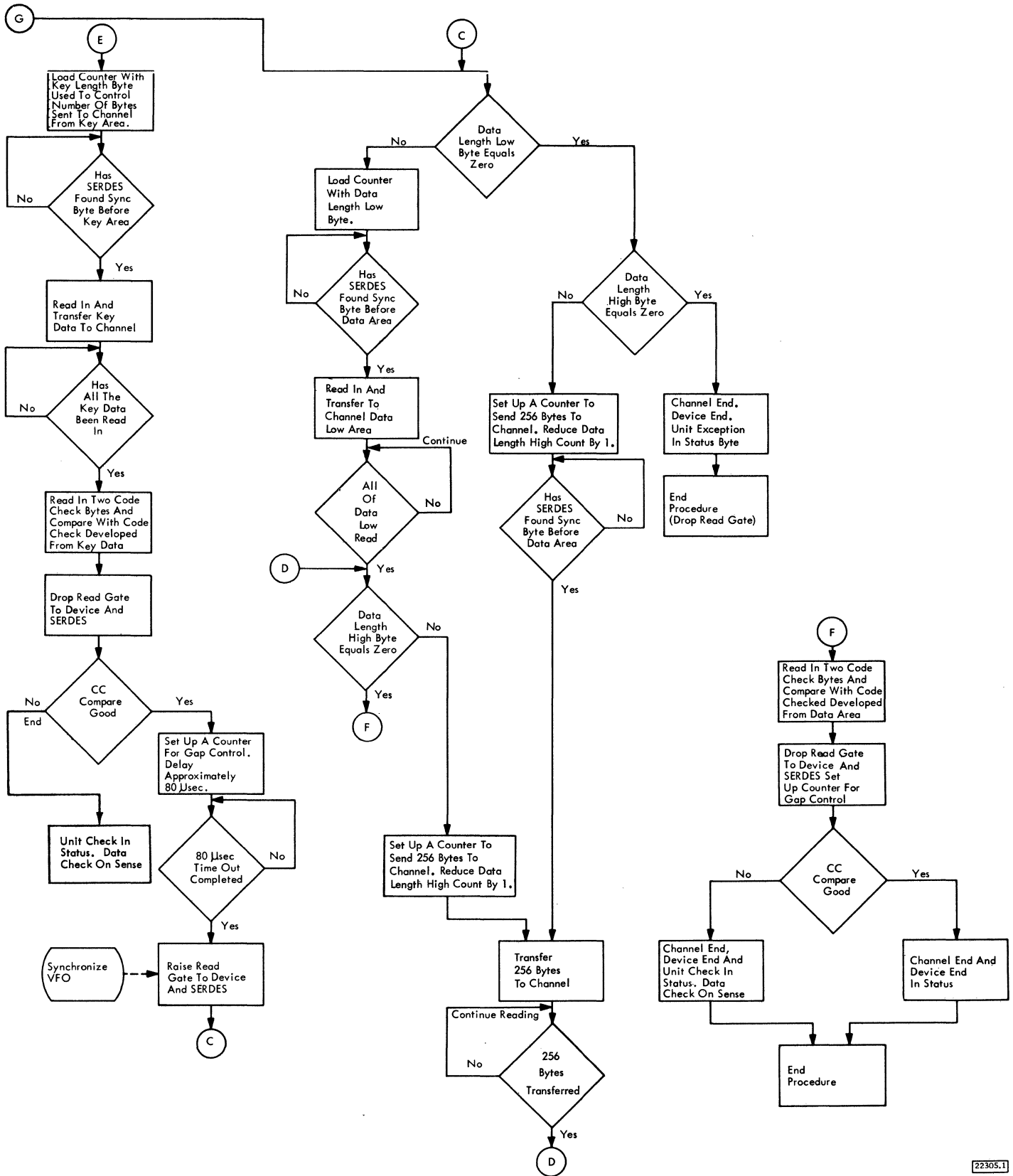
Figure 3-5. Read Home Address - 2311

Assume:  
No Previous Command



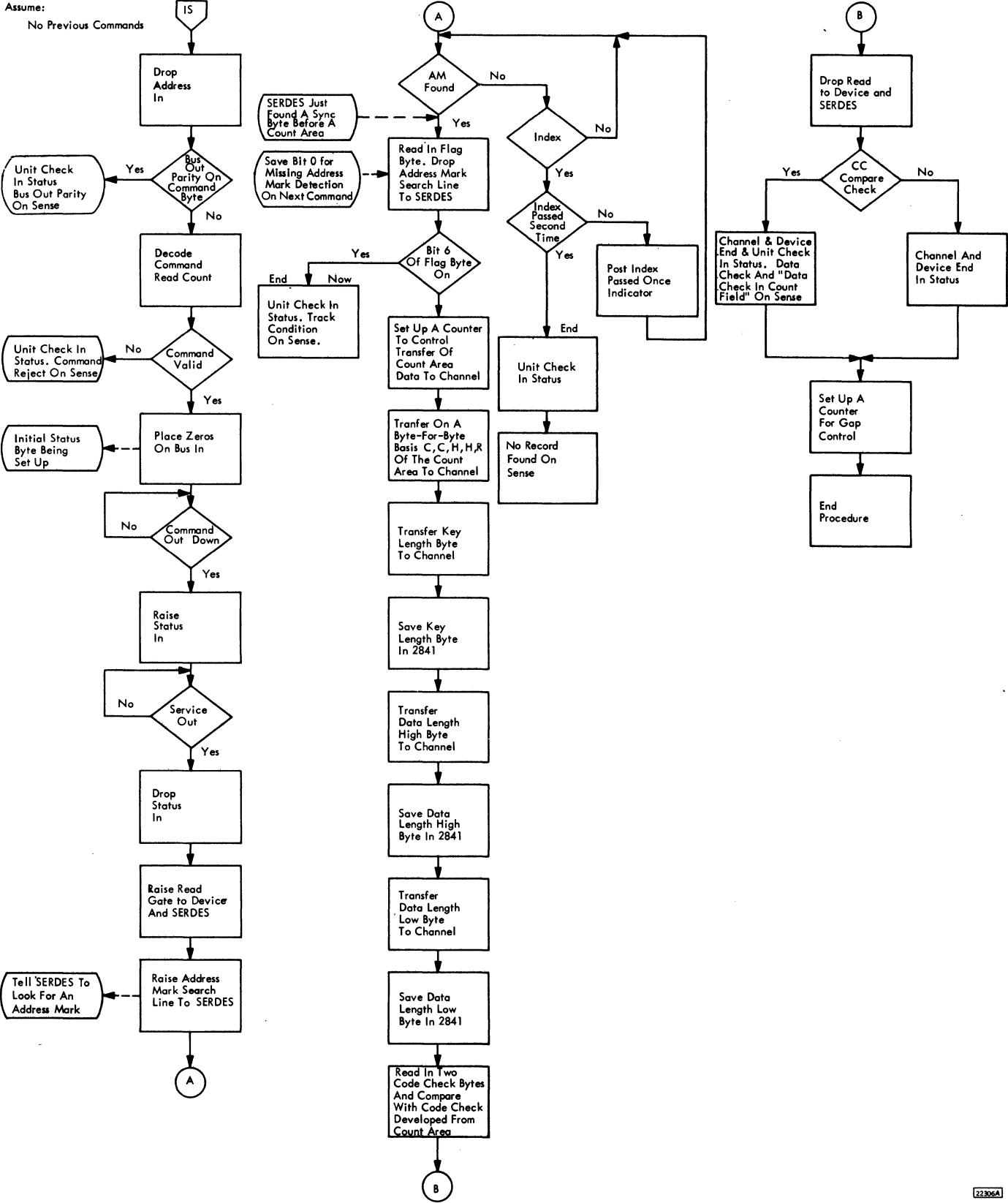
22305.0

Figure 3-6a. Read Record Zero - 2311



22305.1

Figure 3-6b. Read Record Zero - 2311

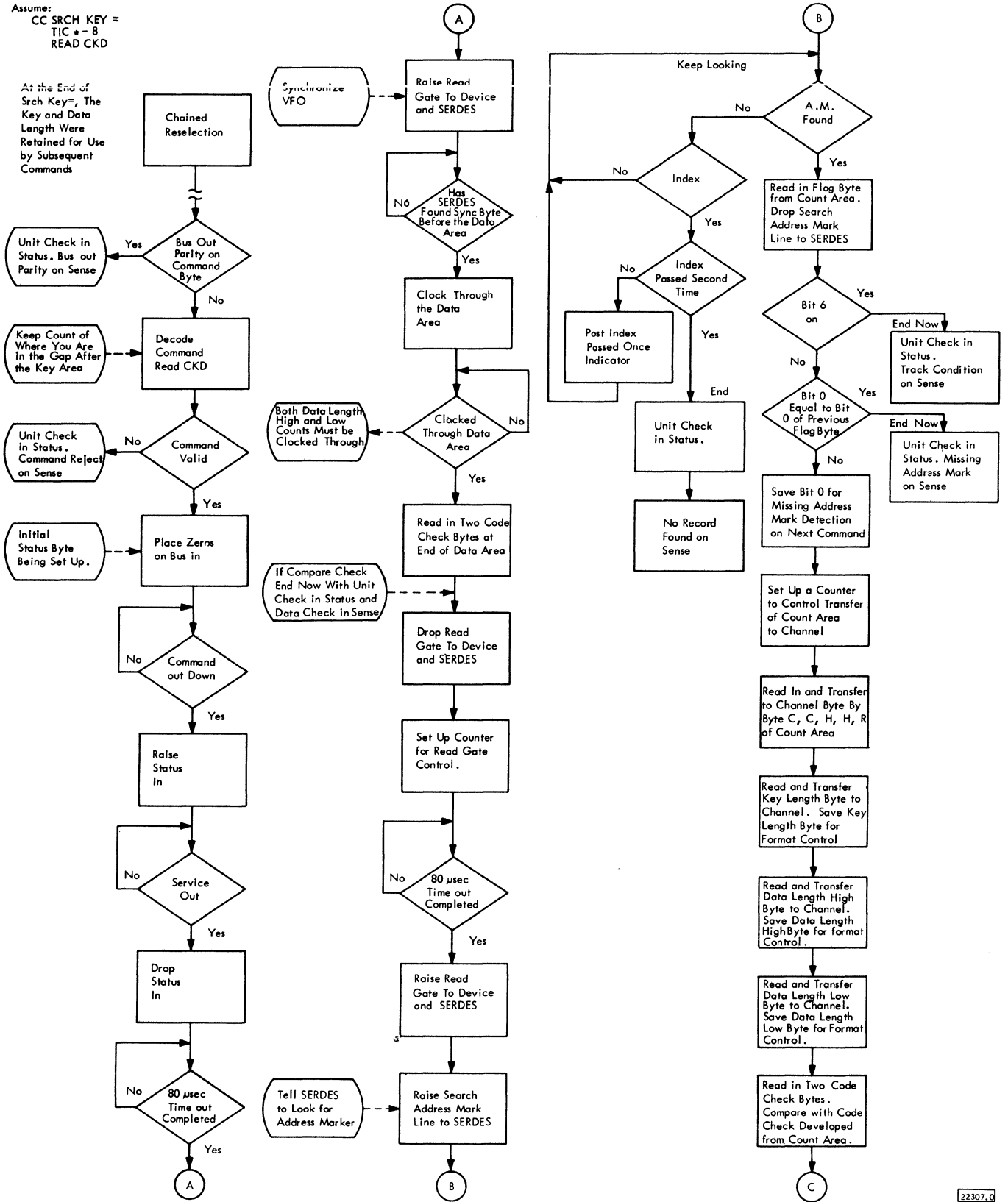


23306A

Figure 3-7. Read Count - 2311

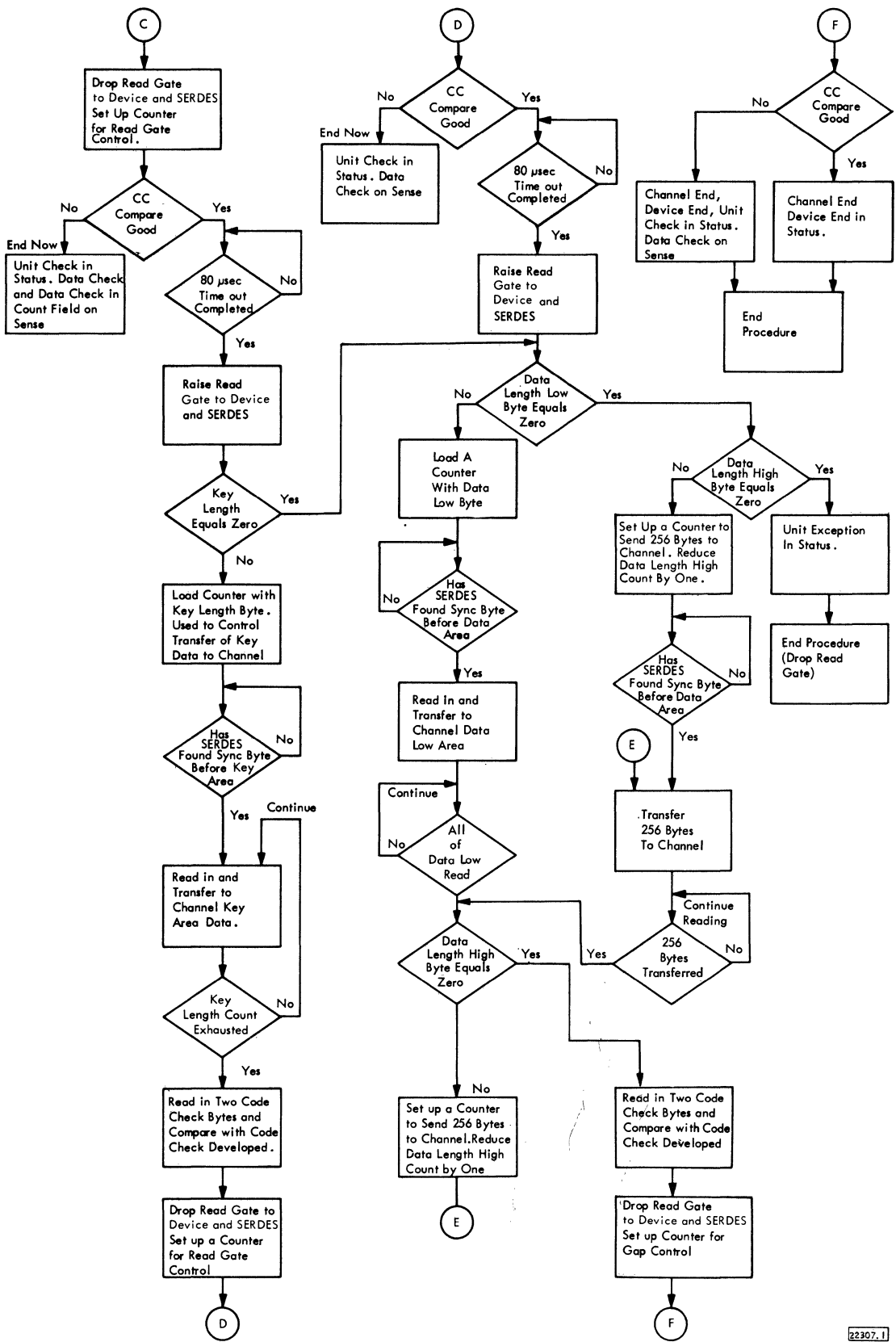
Assume:  
 CC SRCH KEY =  
 TIC \* - 8  
 READ CKD

At the End of  
 Srch Key, The  
 Key and Data  
 Length Were  
 Retained for Use  
 by Subsequent  
 Commands



22307.d

Figure 3-8a. Read Count - Key - Data - 2311



22307.1

Figure 3-8b. Read Count - Key - Data - 2311

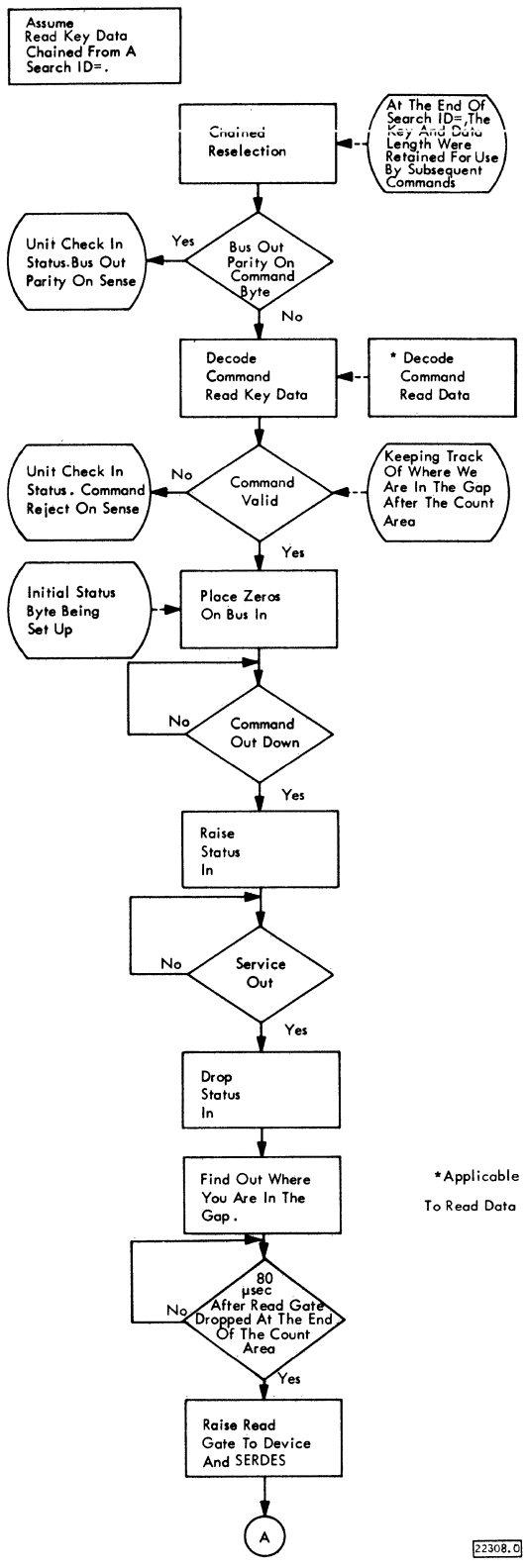


Figure 3-9a. Read Data and Read Key - Data - 2311



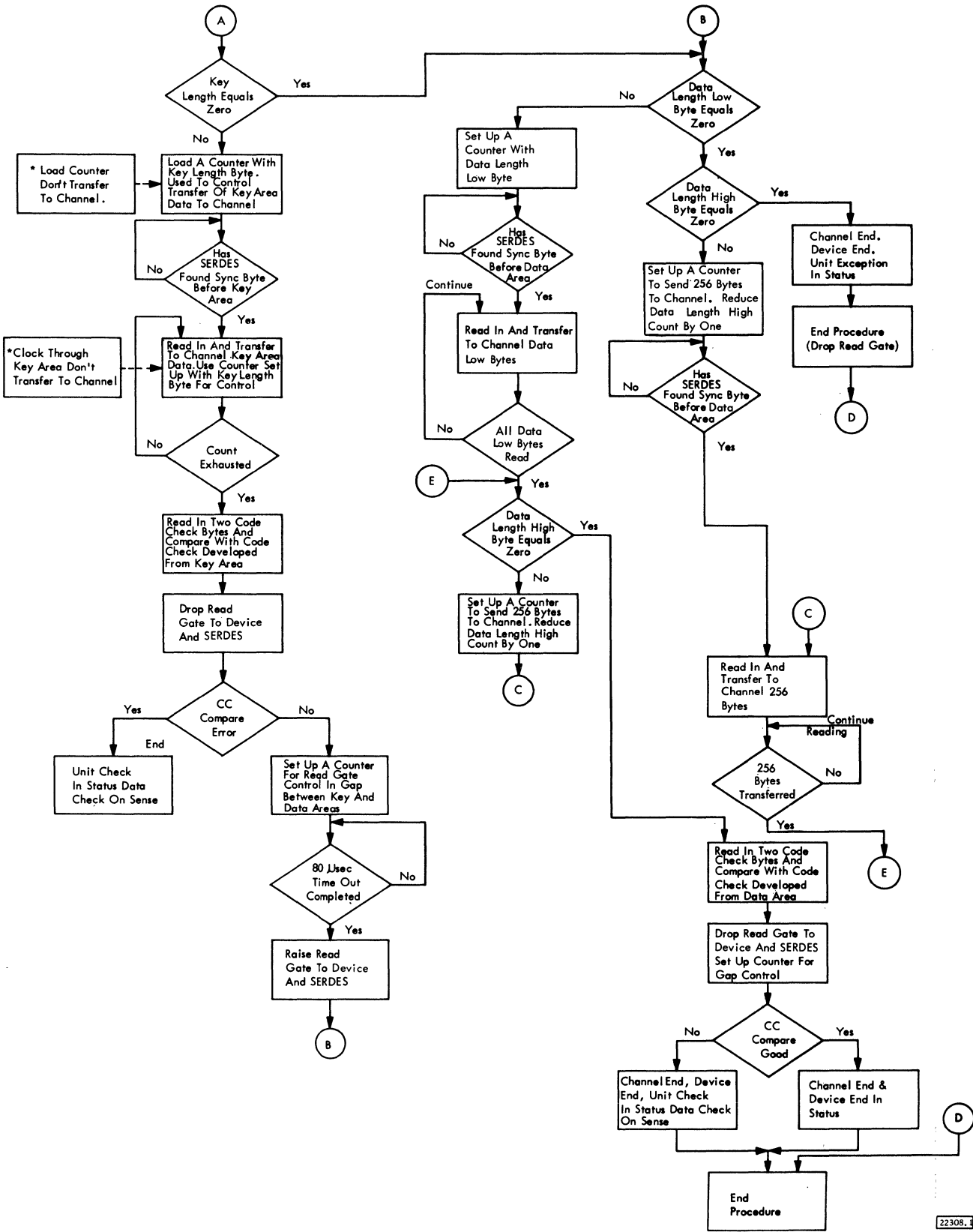
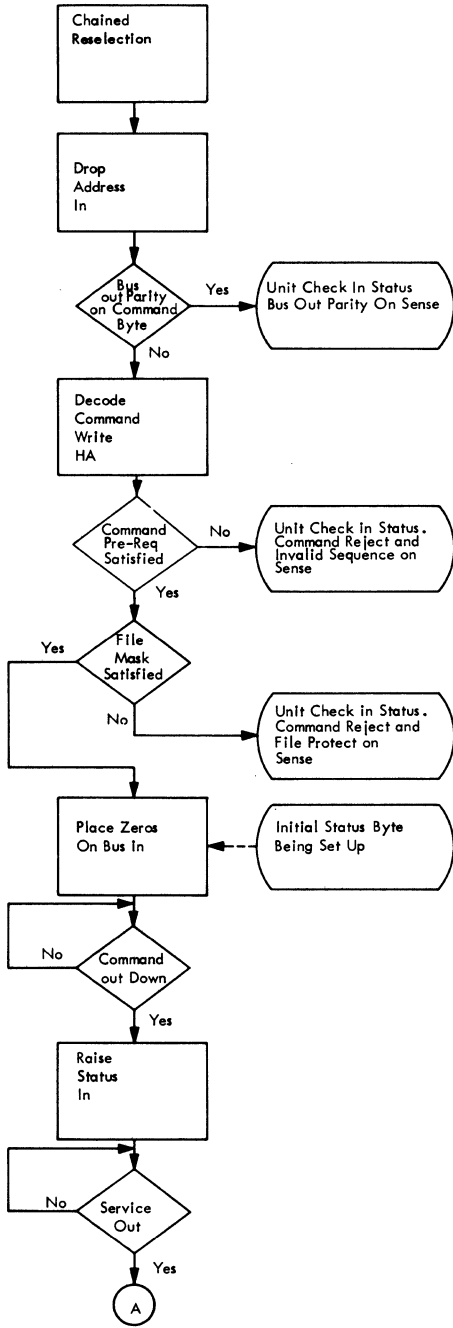
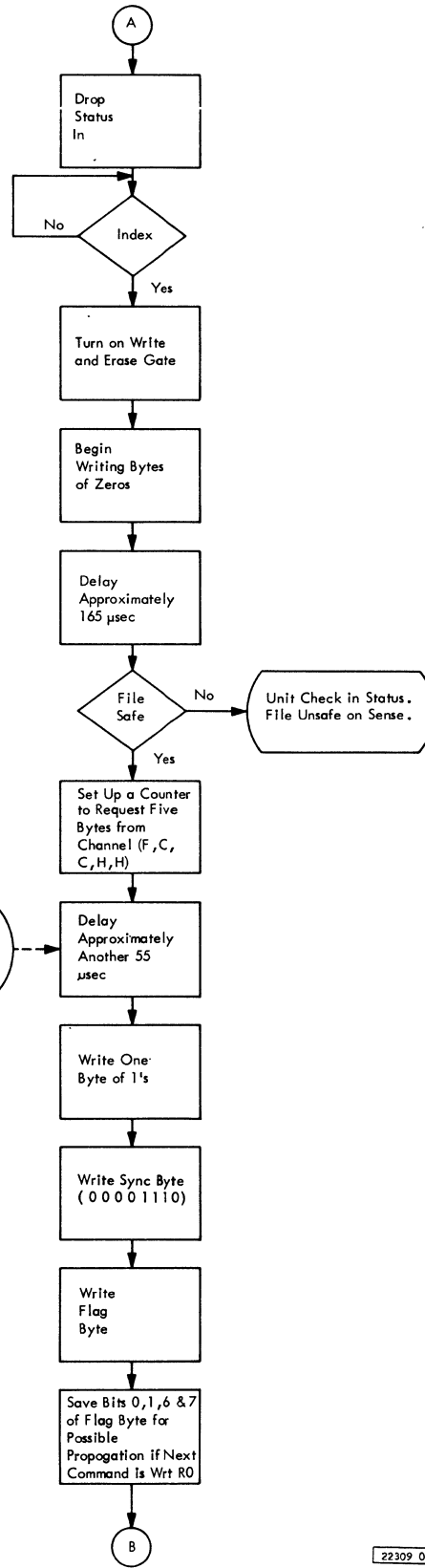


Figure 3-9b. Read Data and Read Key - Data - 2311

Program:SIO  
 CC Seek CCHH  
 CC SFM (To Allow  
 Wrt HA) Wrt HA

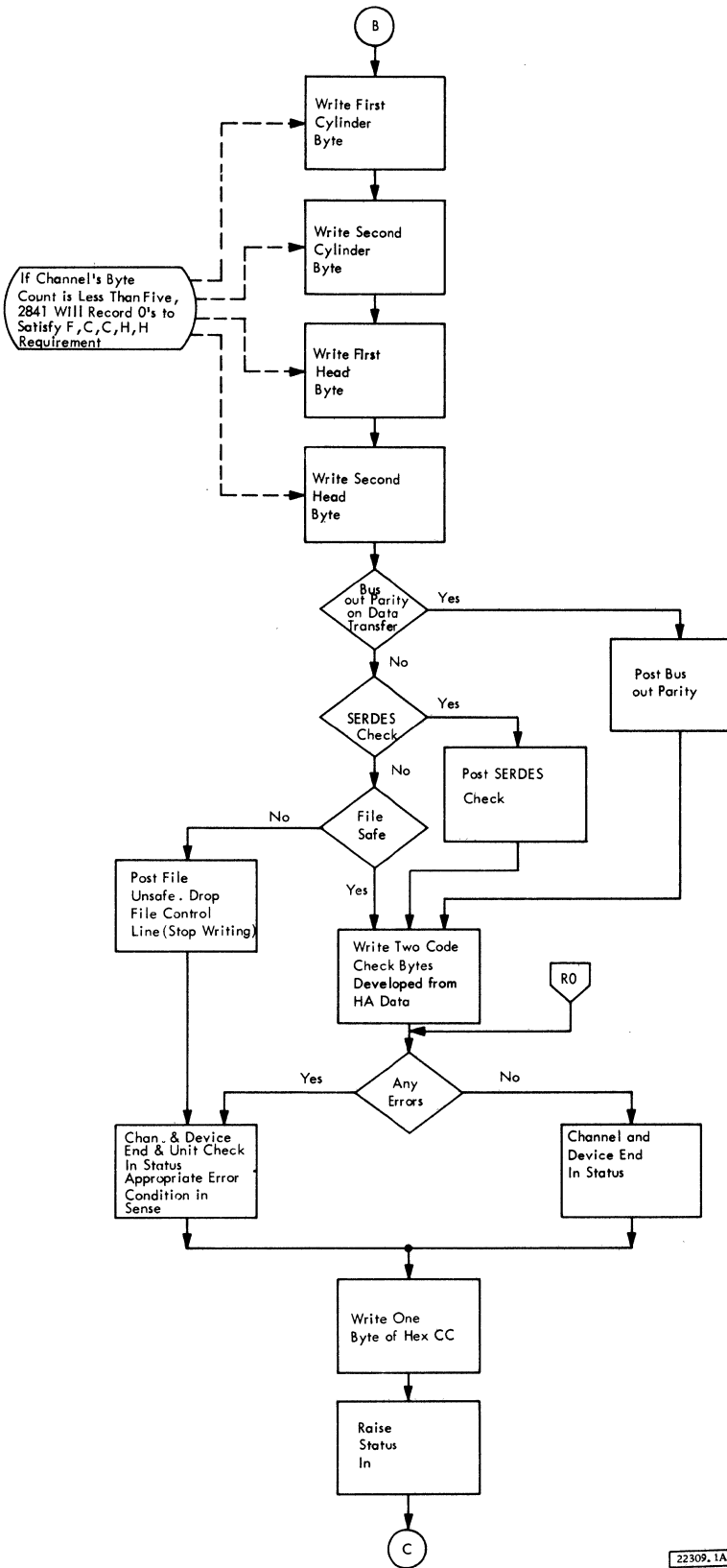


Still Writing Zeros



22309 0A

Figure 3-10a. Write Home Address - 2311



22309. 1A

Figure 3-10b. Write Home Address - 2311



Figure 3-1a. Write Record Zero - 2311

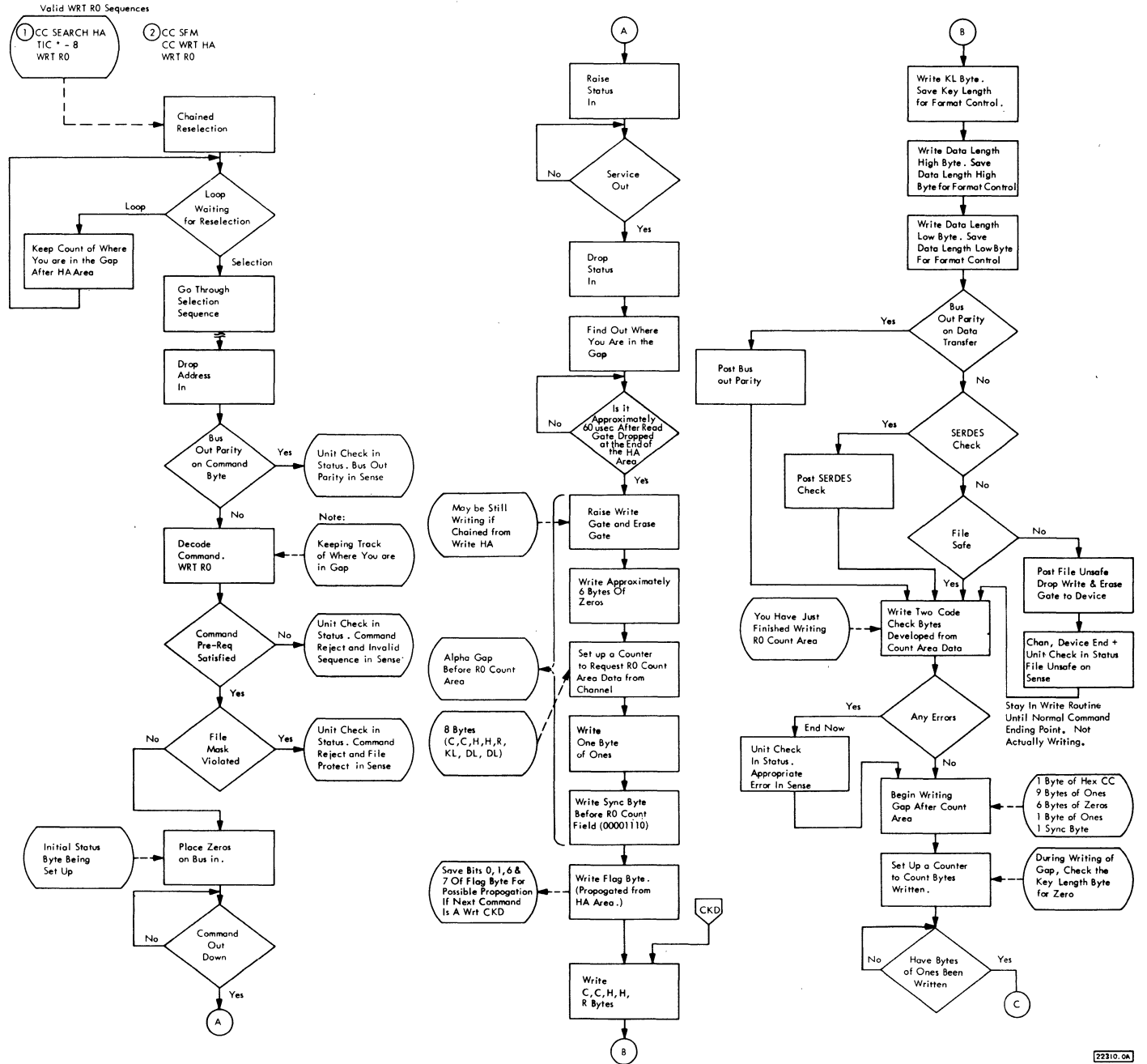
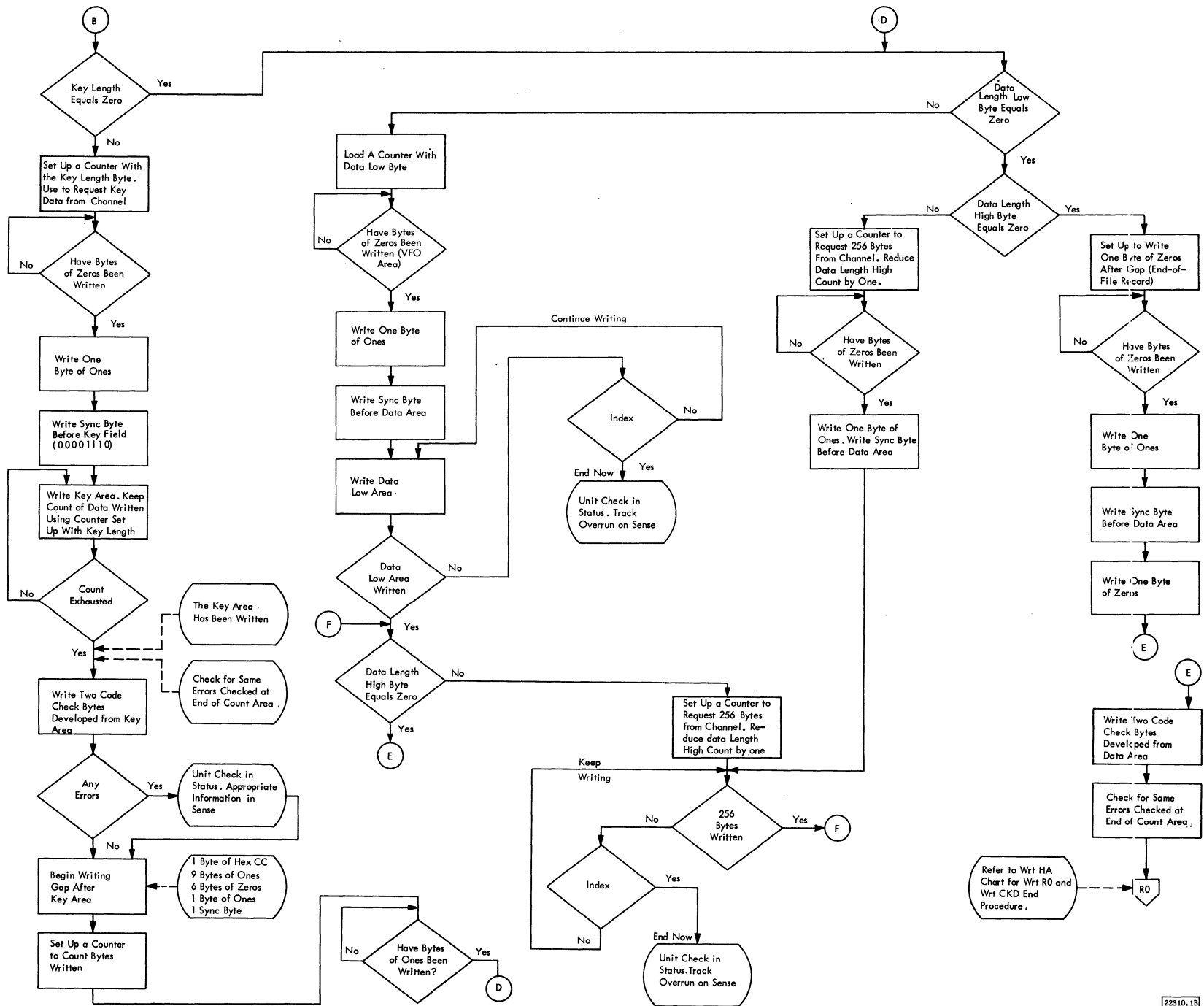


Figure 3-11b. Write Record Zero - 2311



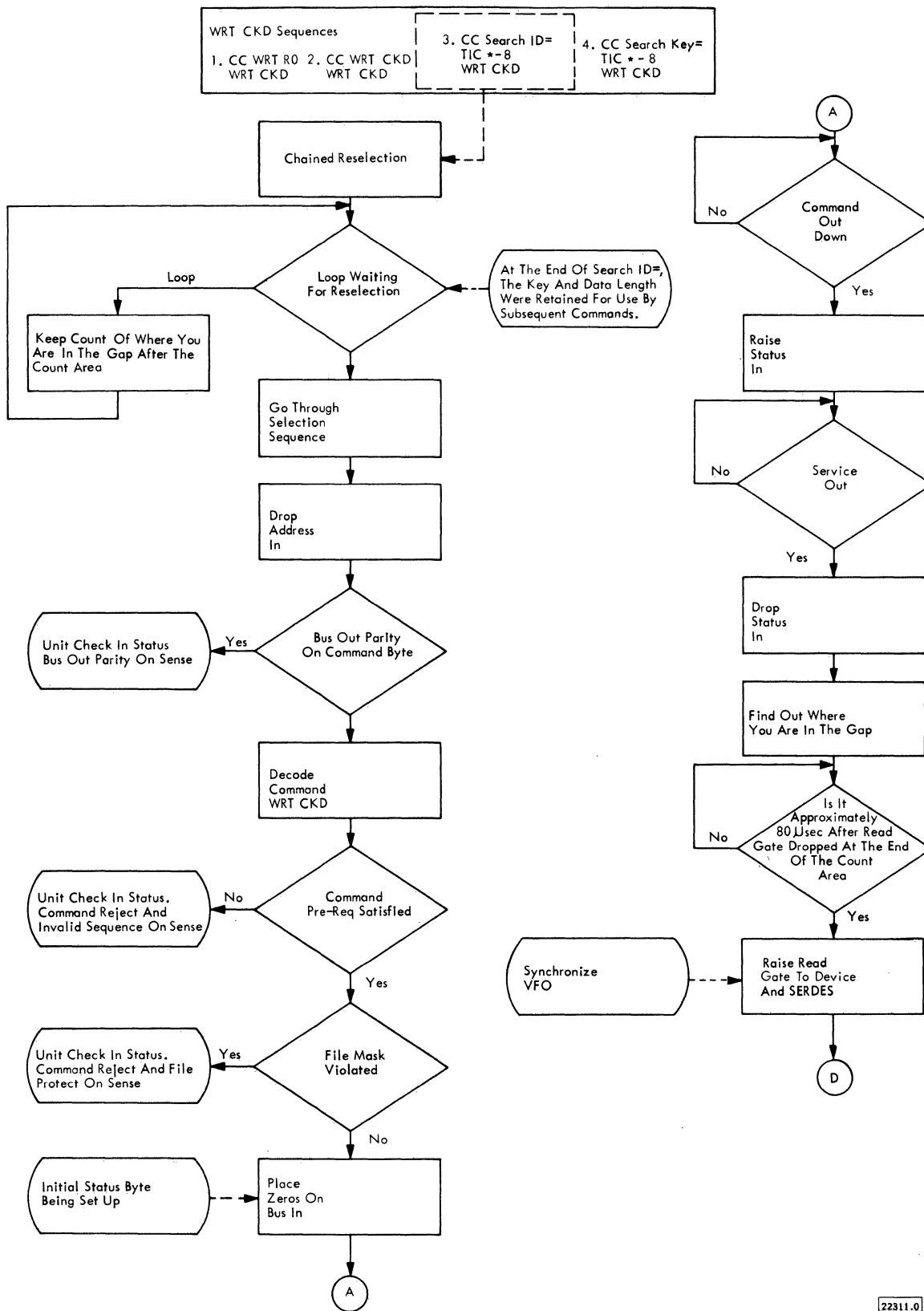
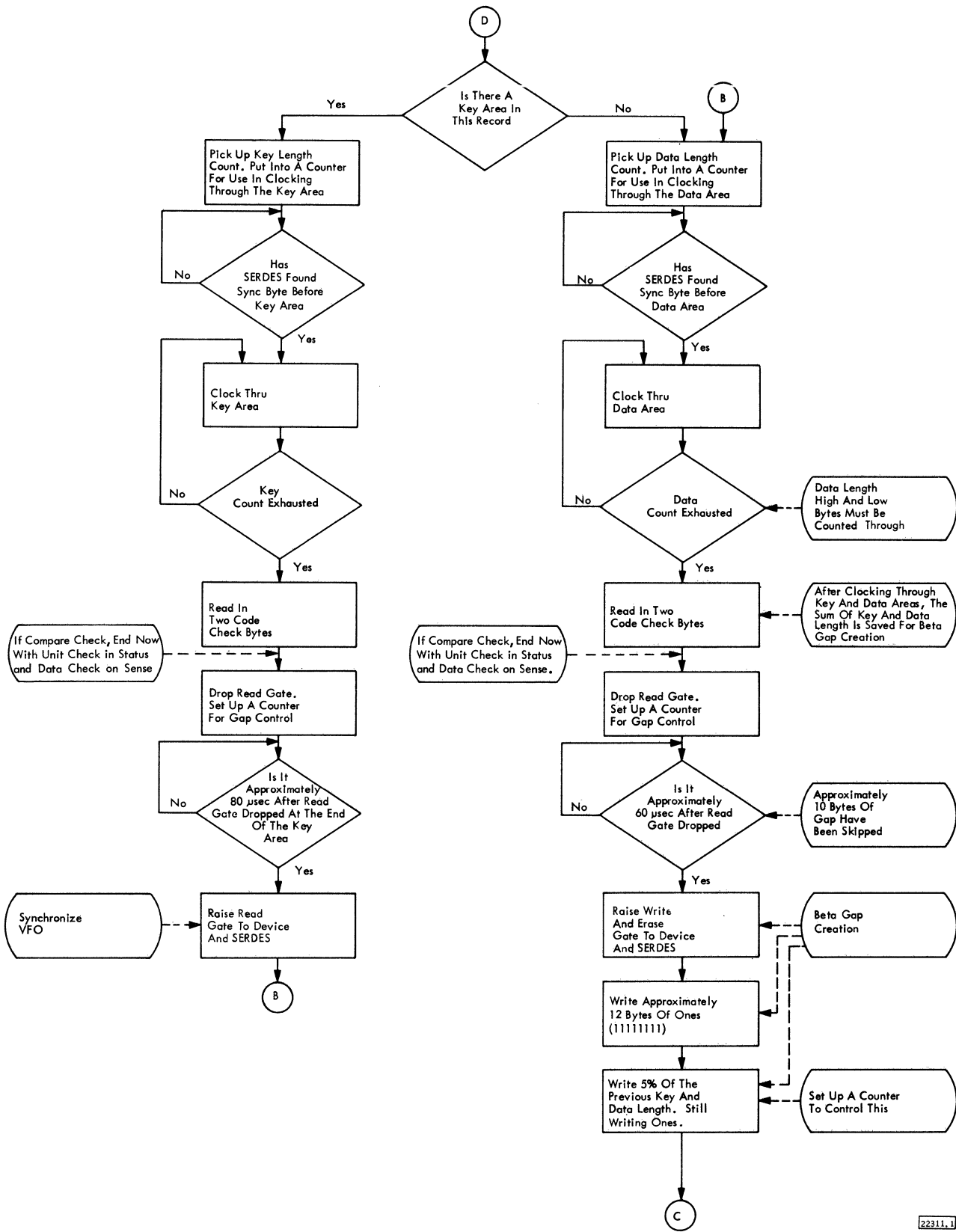


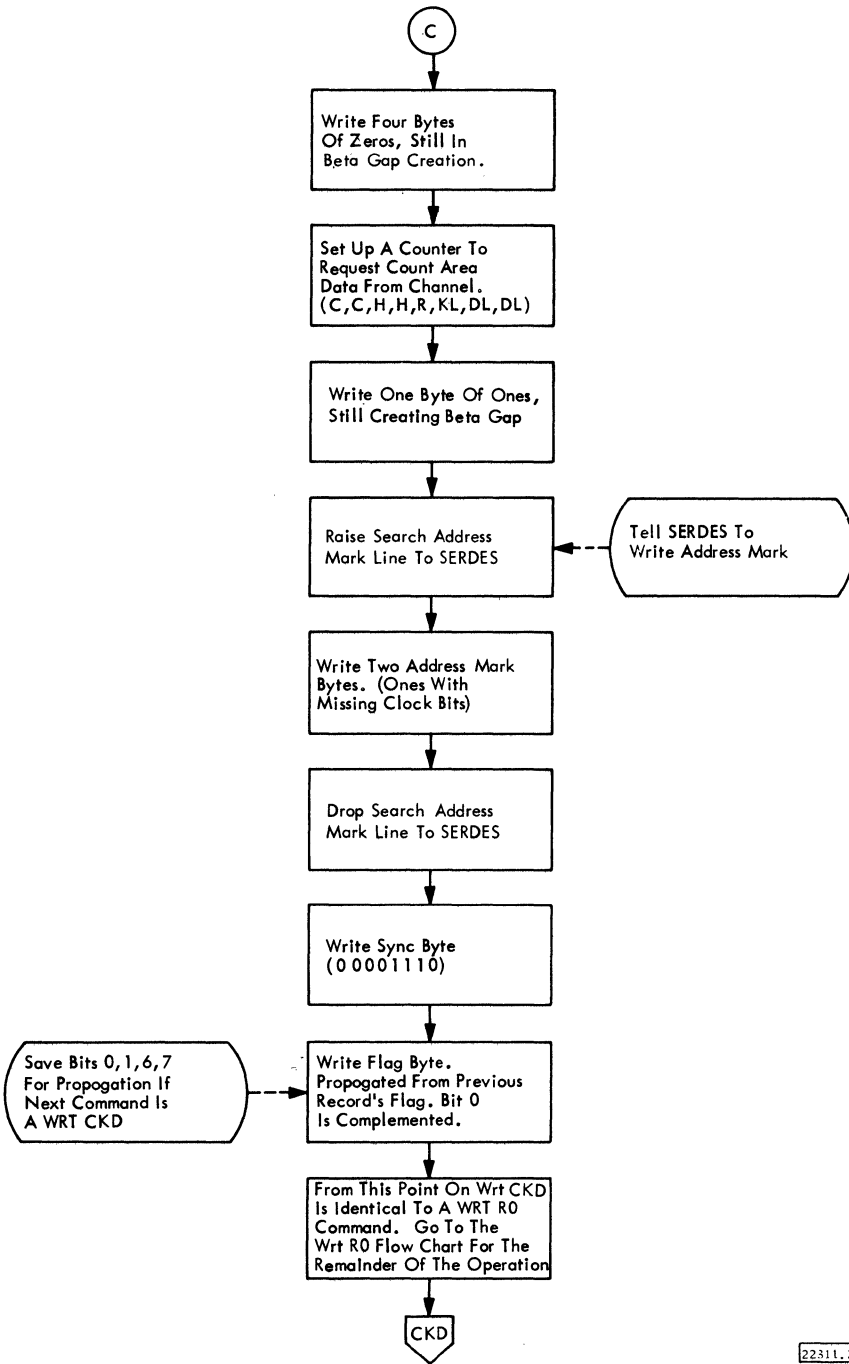
Figure 3-12a. Write Count - Key - Data - 2311



22311.1

Figure 3-12b. Write Count - Key - Data - 2311





22311.2

Figure 3-12c. Write Count - Key - Data - 2311

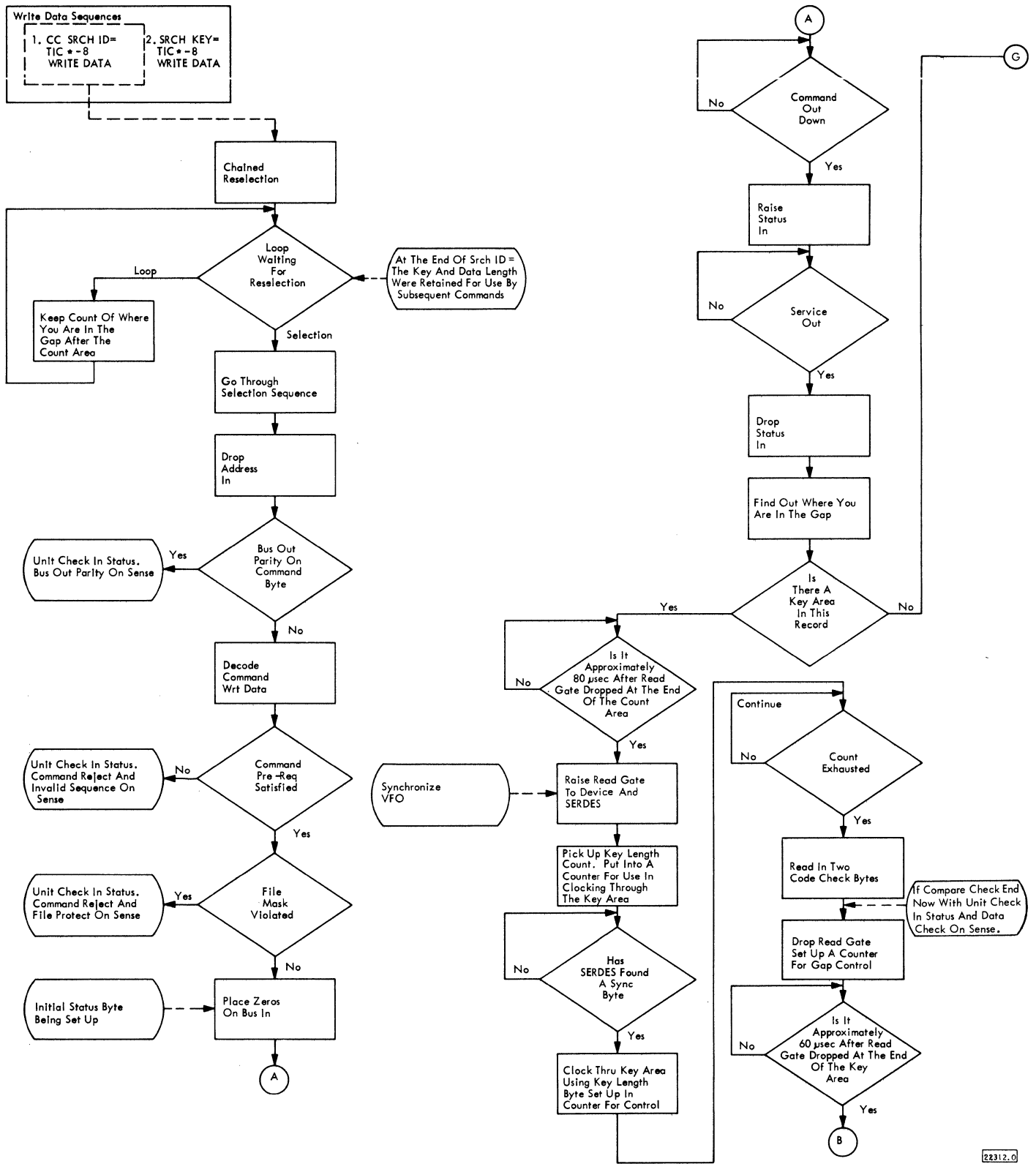
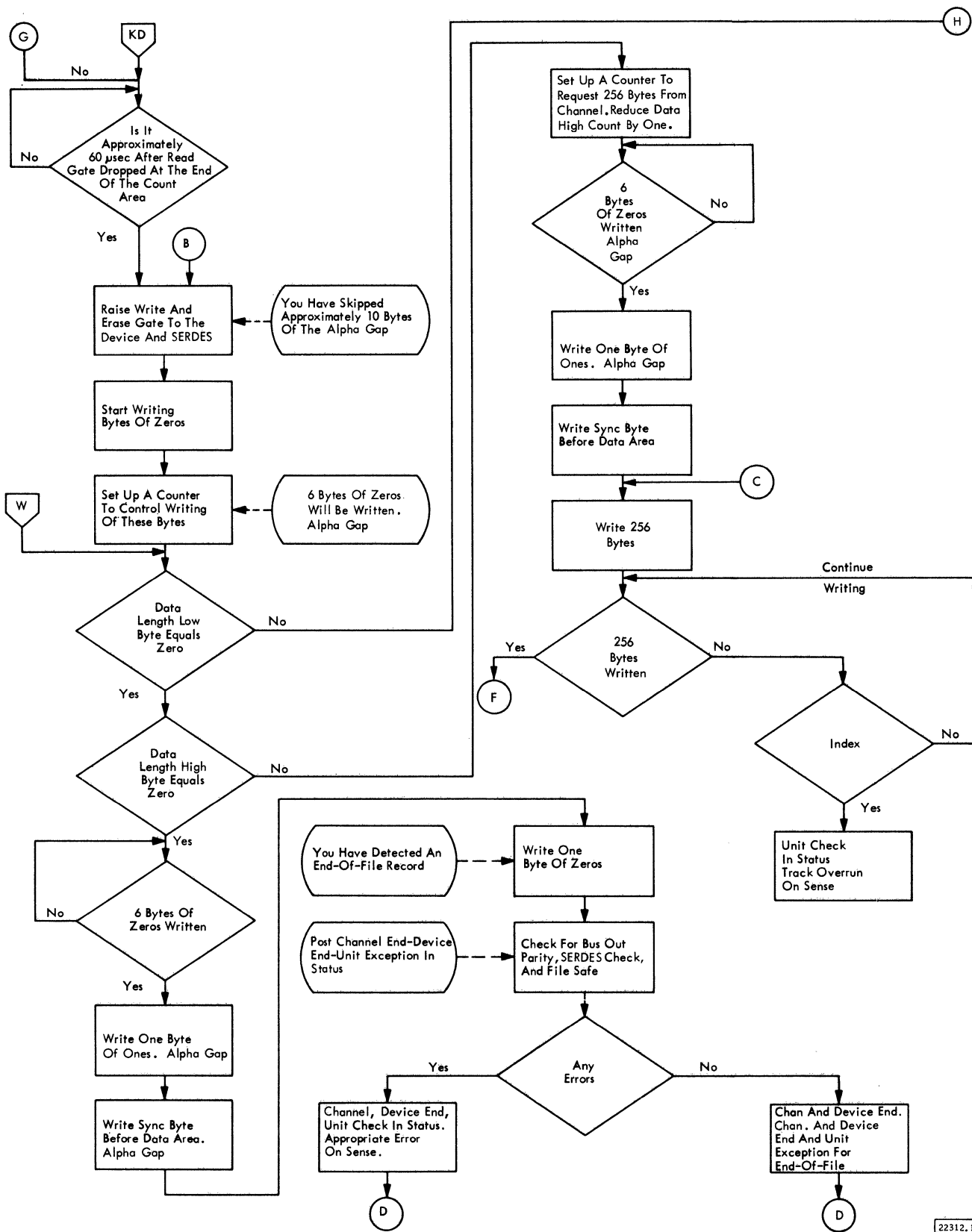


Figure 3-13a. Write Data - 2311

22312.0



22312.1

Figure 3-13b. Write Data - 2311

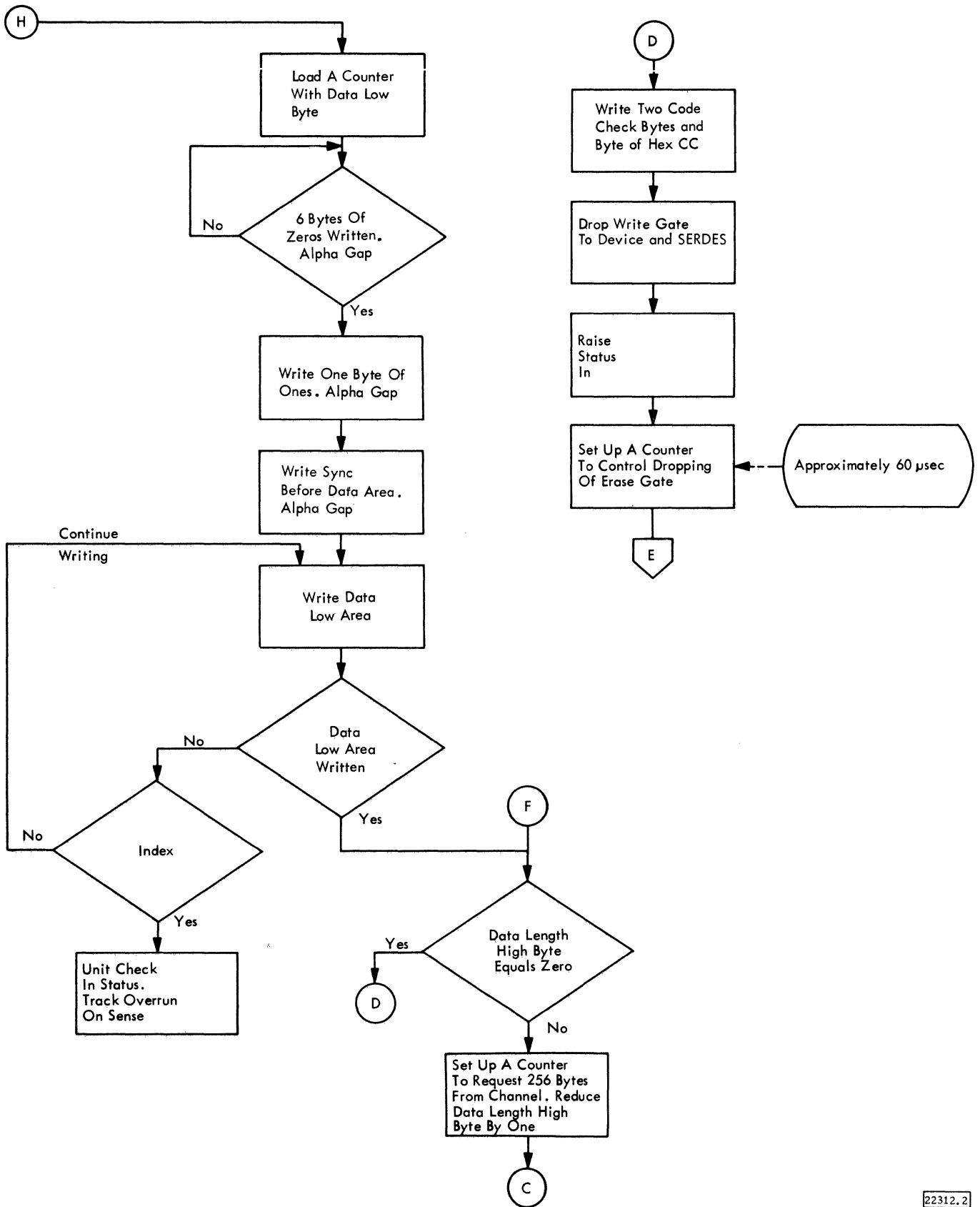


Figure 3-13c. Write Data - 2311

22312.2

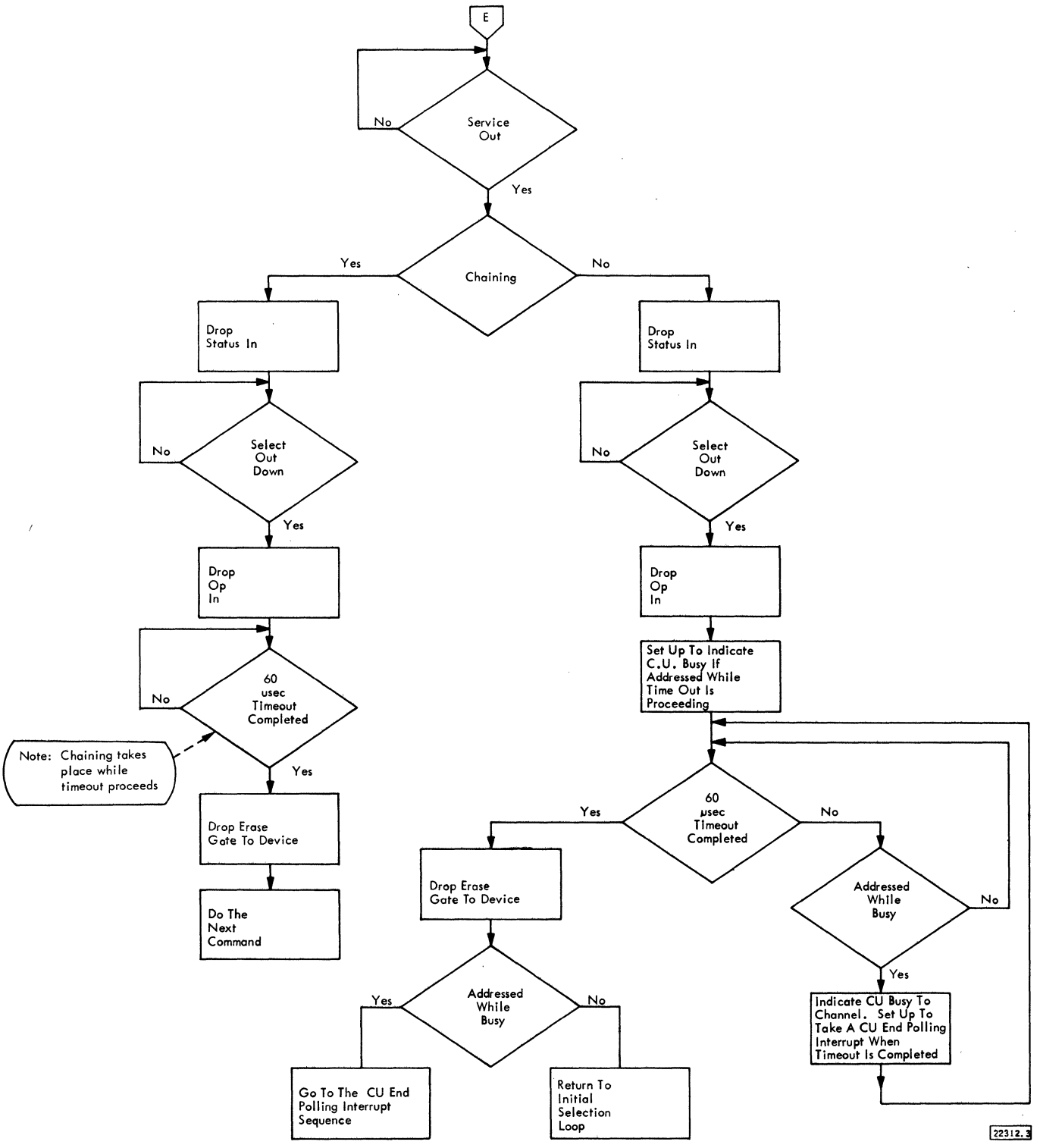


Figure 3-13d, Write Data - 2311

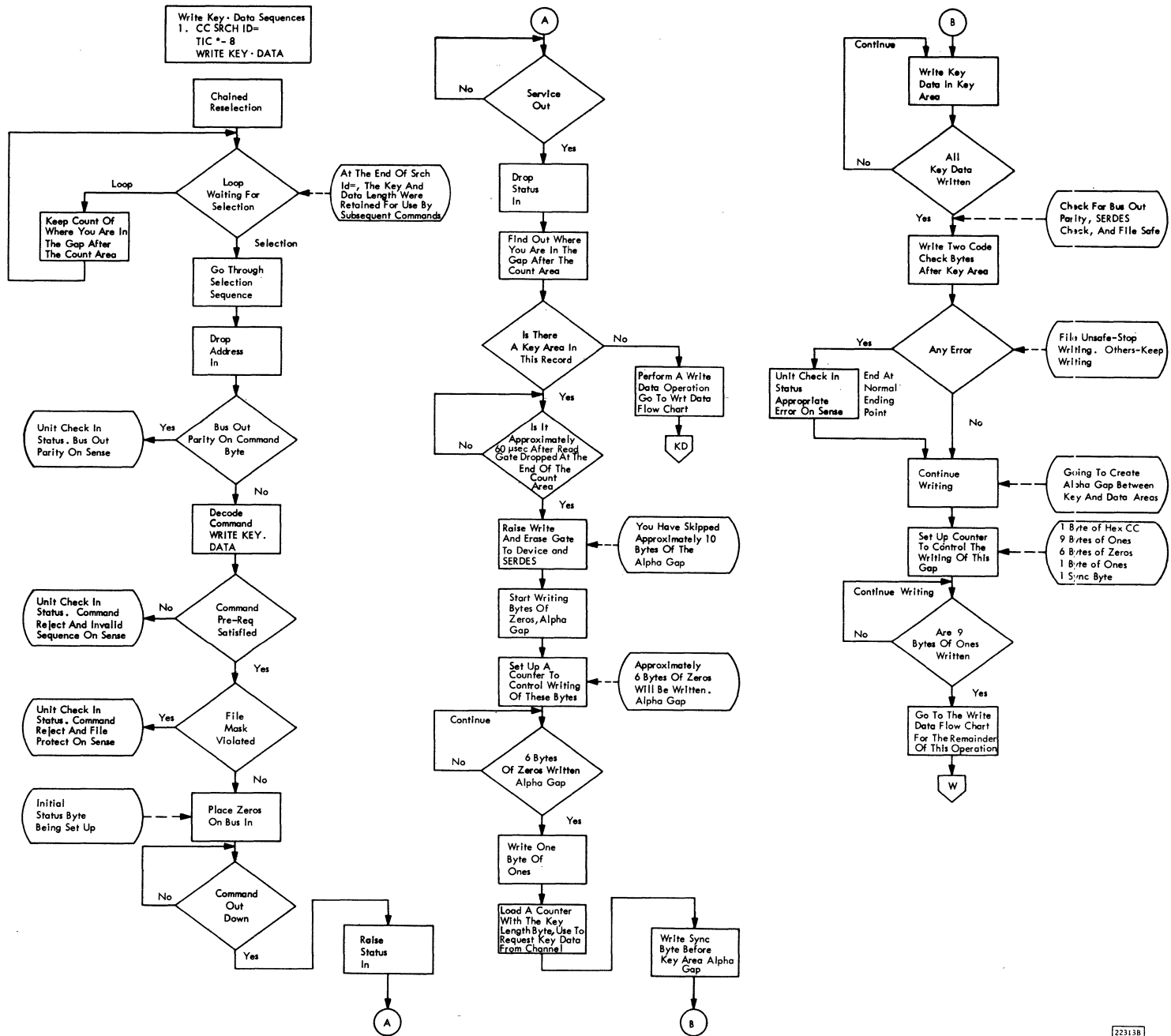
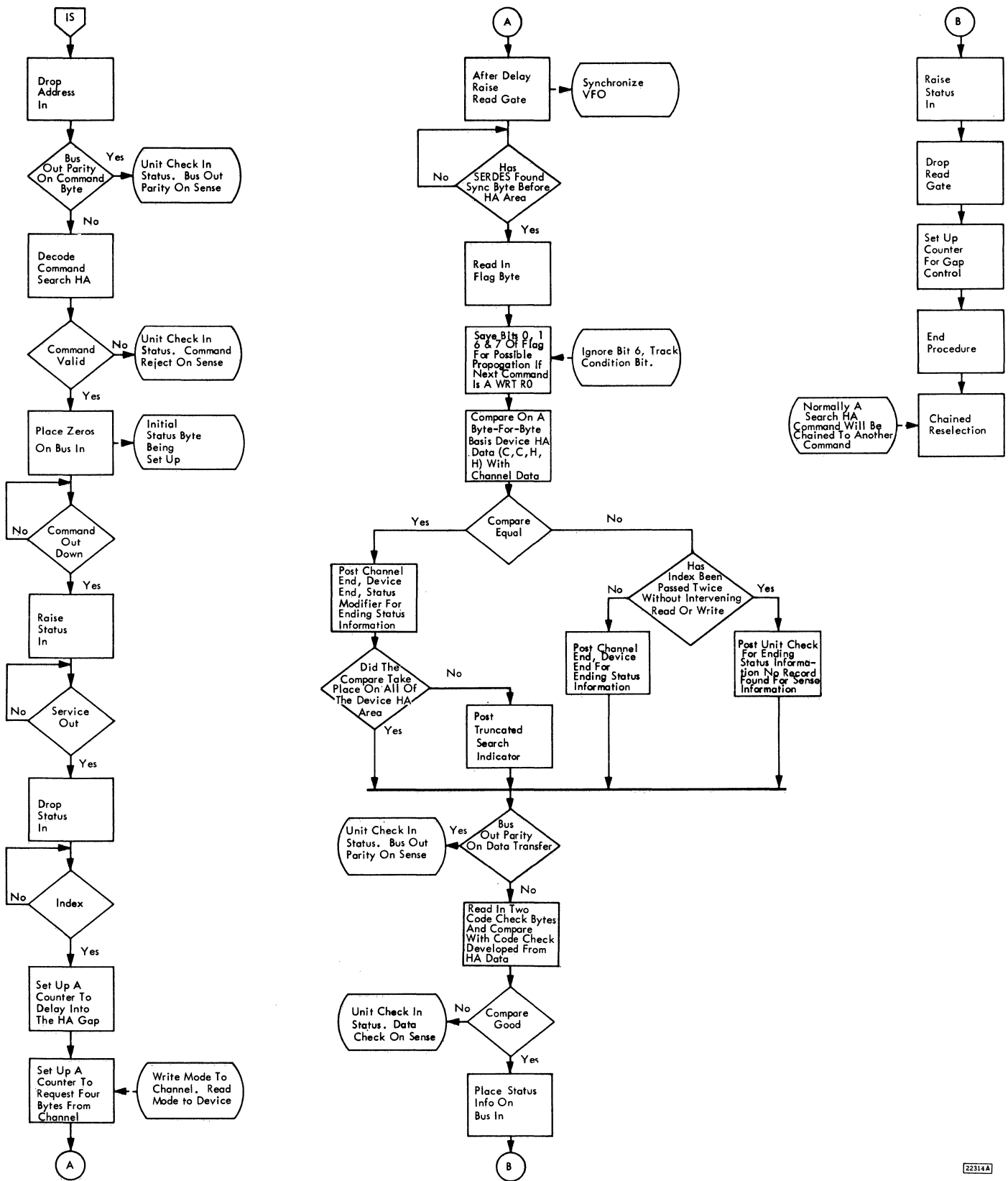
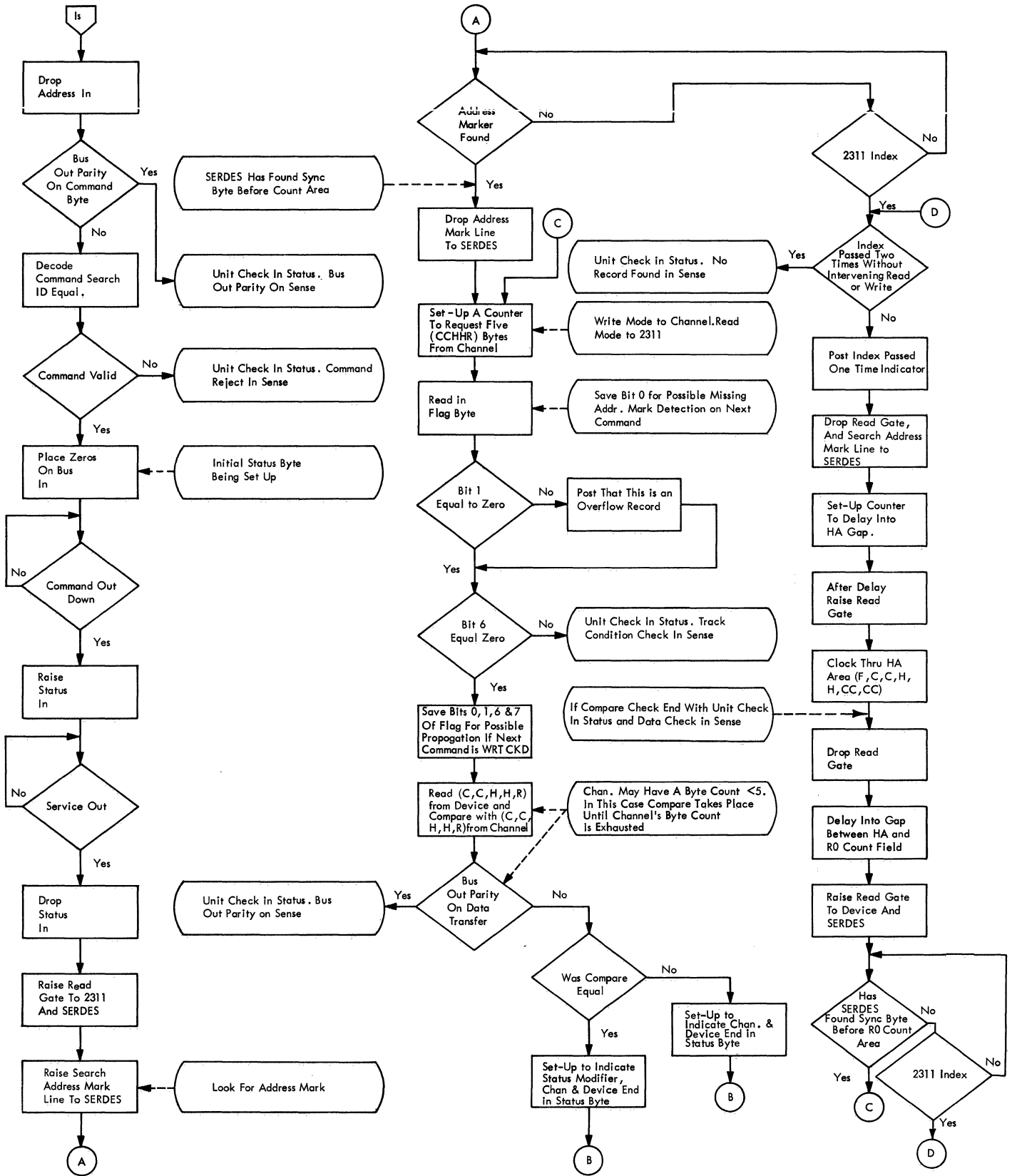


Figure 3-14. Write Key - Data - 2311



22314A

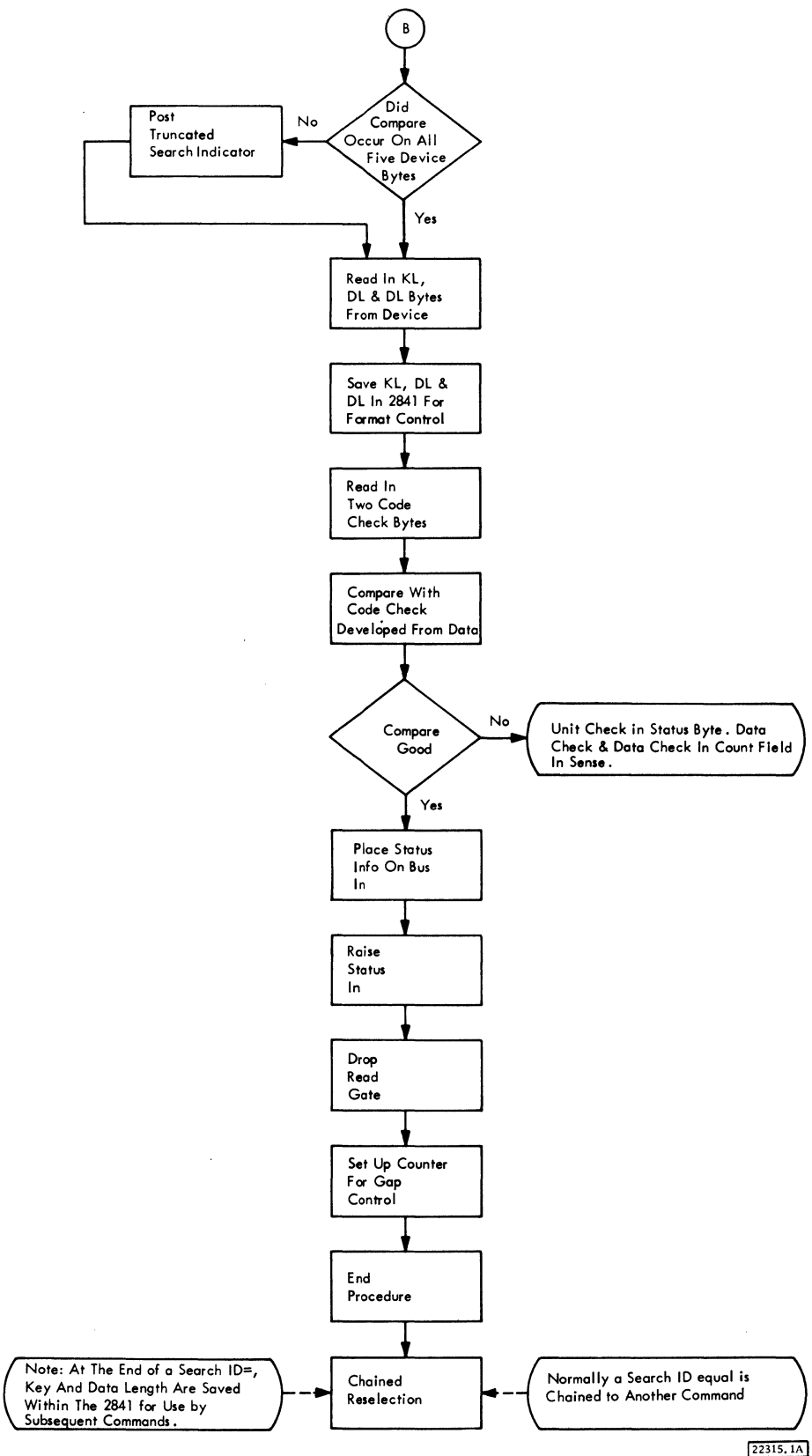
Figure 3-15. Search Home Address - 2311



22315.08

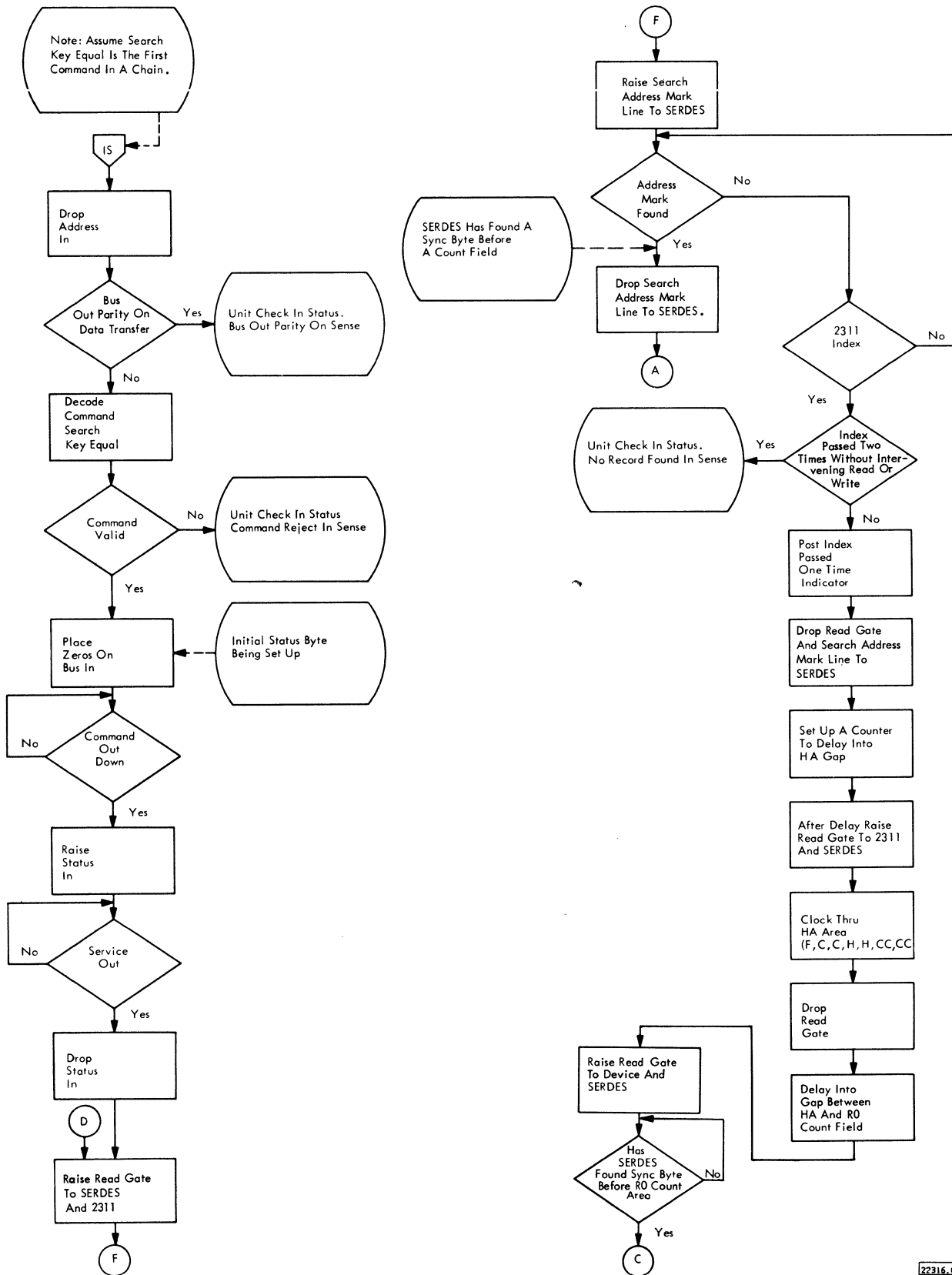
Figure 3-16a. Search ID Equal - 2311





22315.1A

Figure 3-16b. Search ID Equal - 2311



22316.0

Figure 3-17a. Search Key Equal - 2311

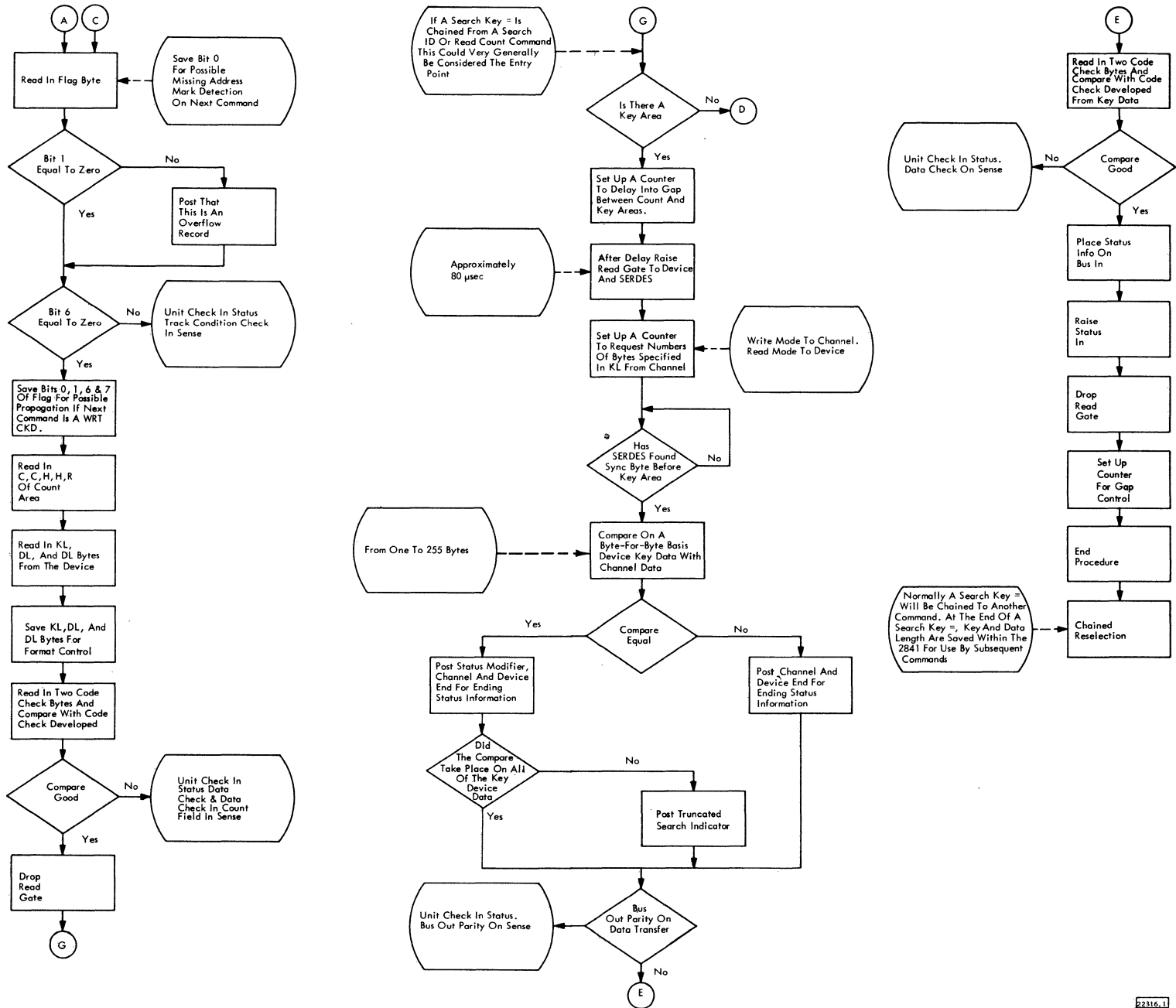
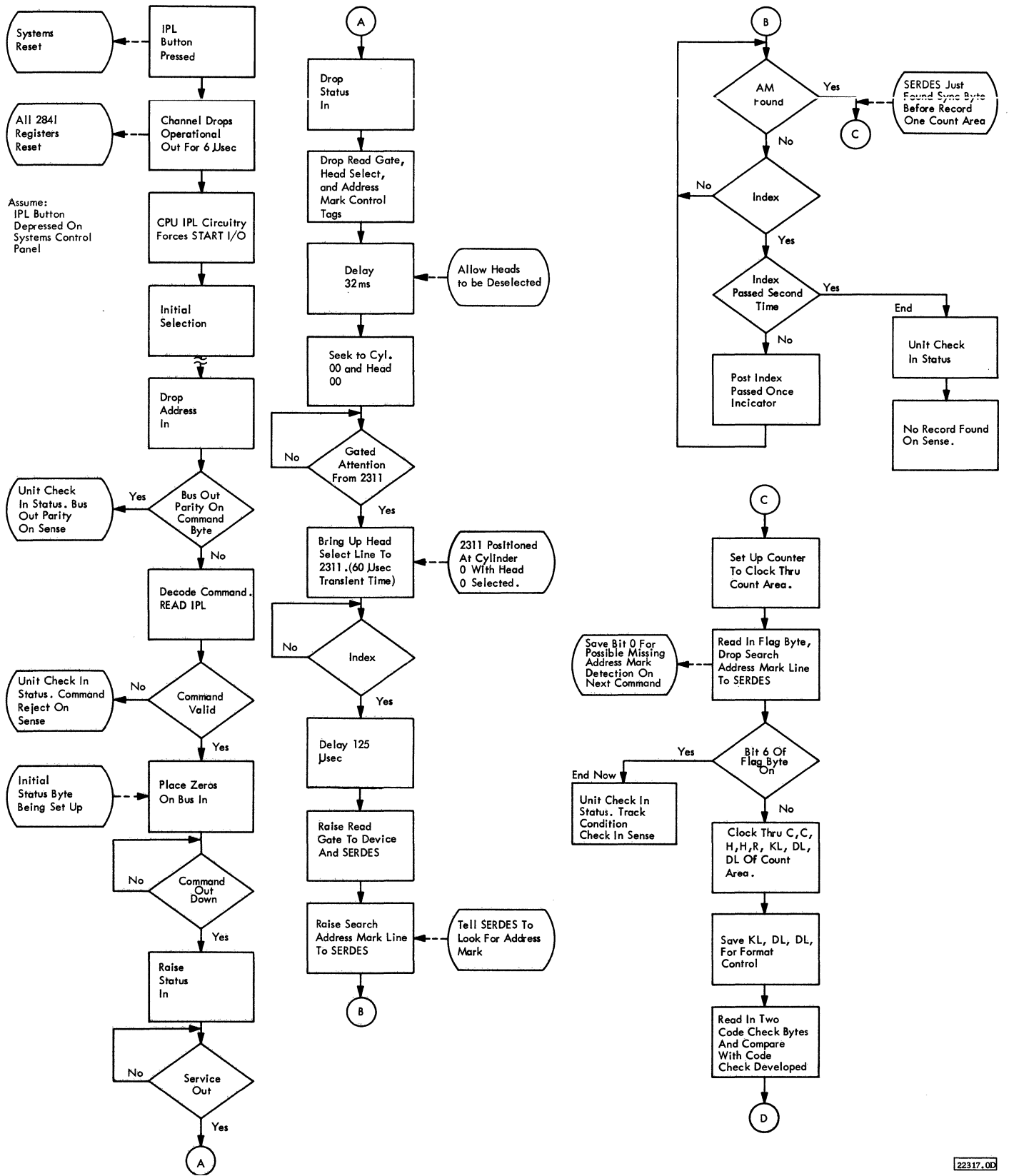
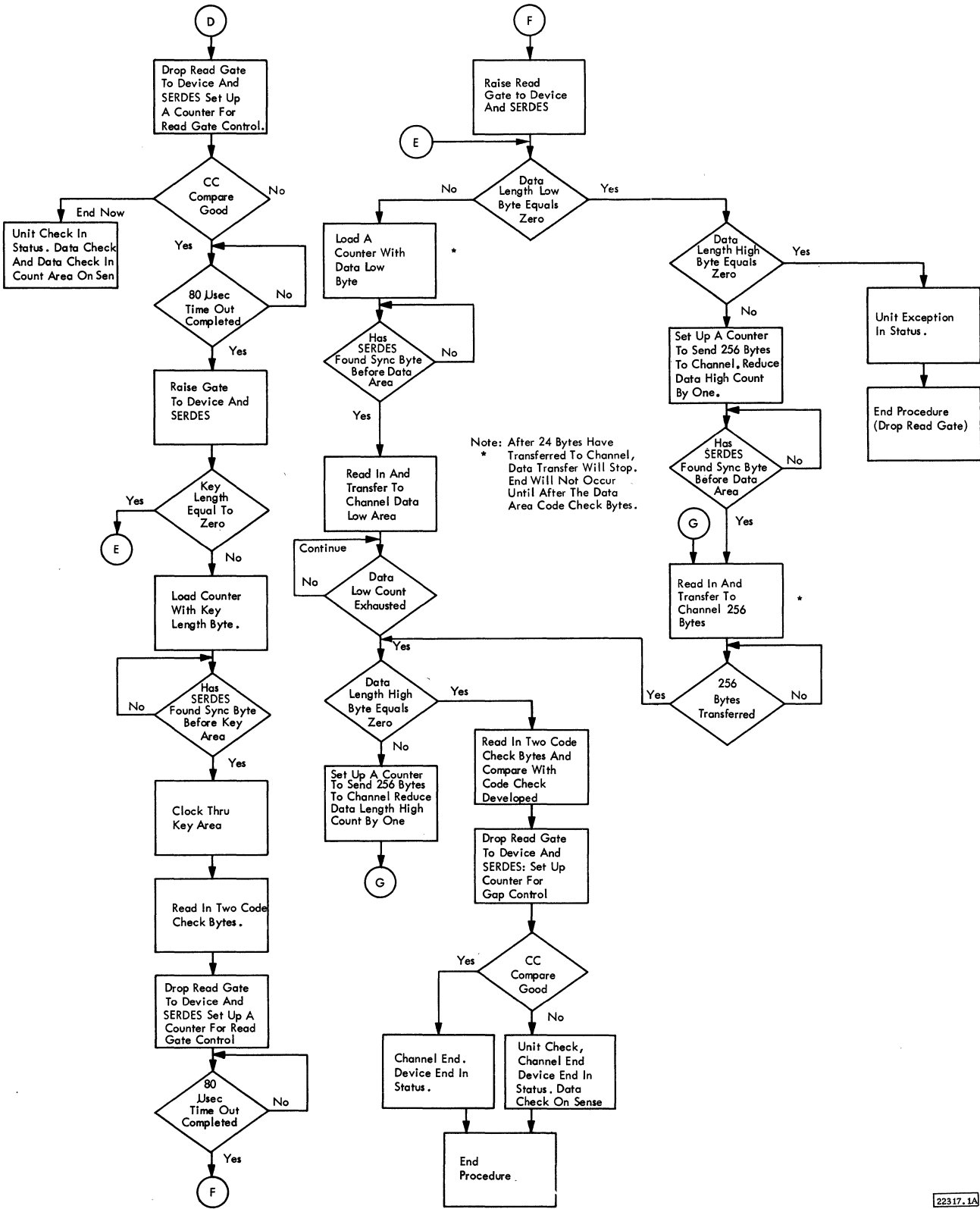


Figure 3-17b. Search Key Equal - 2311



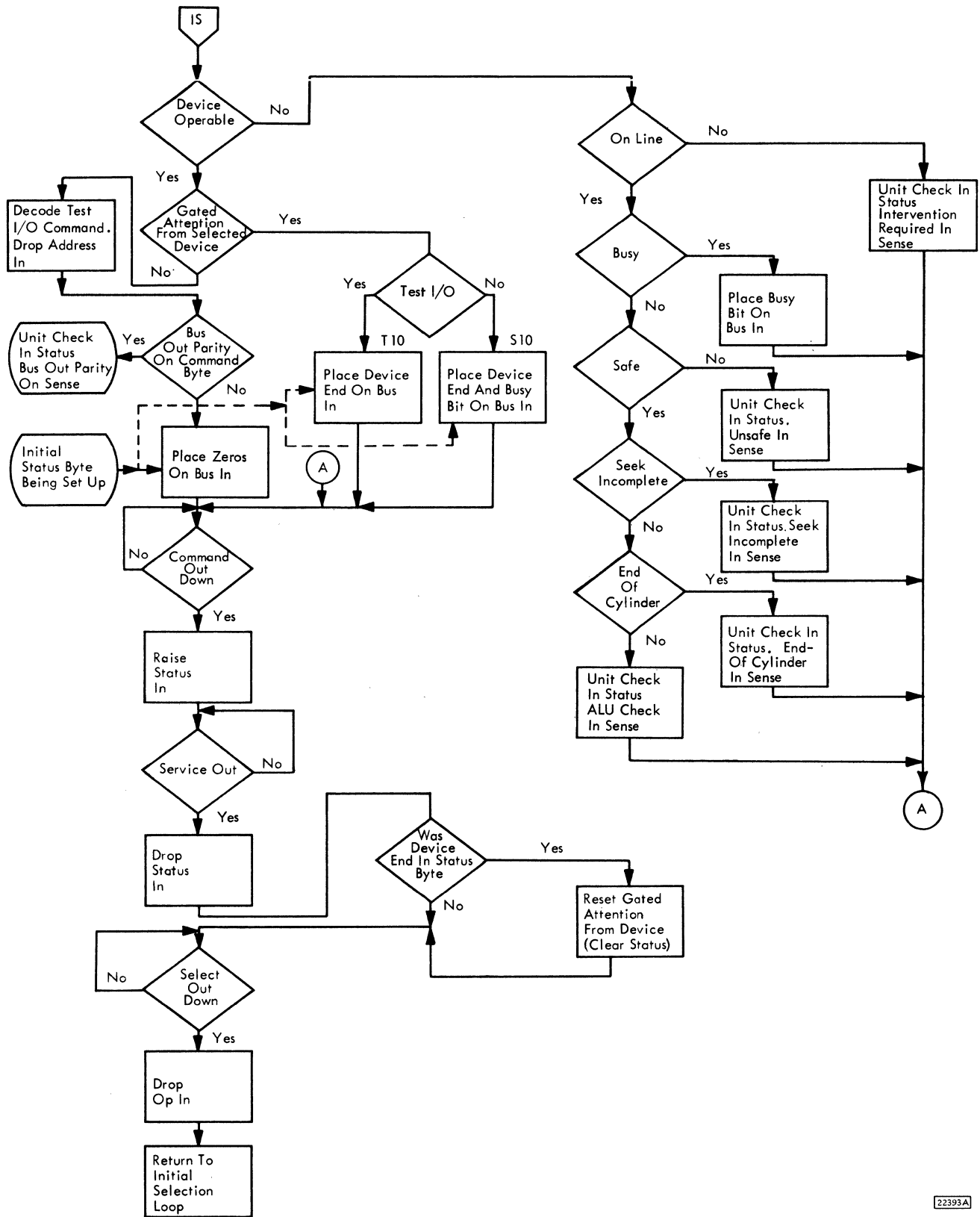
22317.00

Figure 3-18a. Initial Program Load - 2311



22317\_1A

Figure 3-18b. Initial Program Load - 2311



22393A

Figure 3-19. Test I/O, or Start I/O with Device Inoperable or Outstanding Status

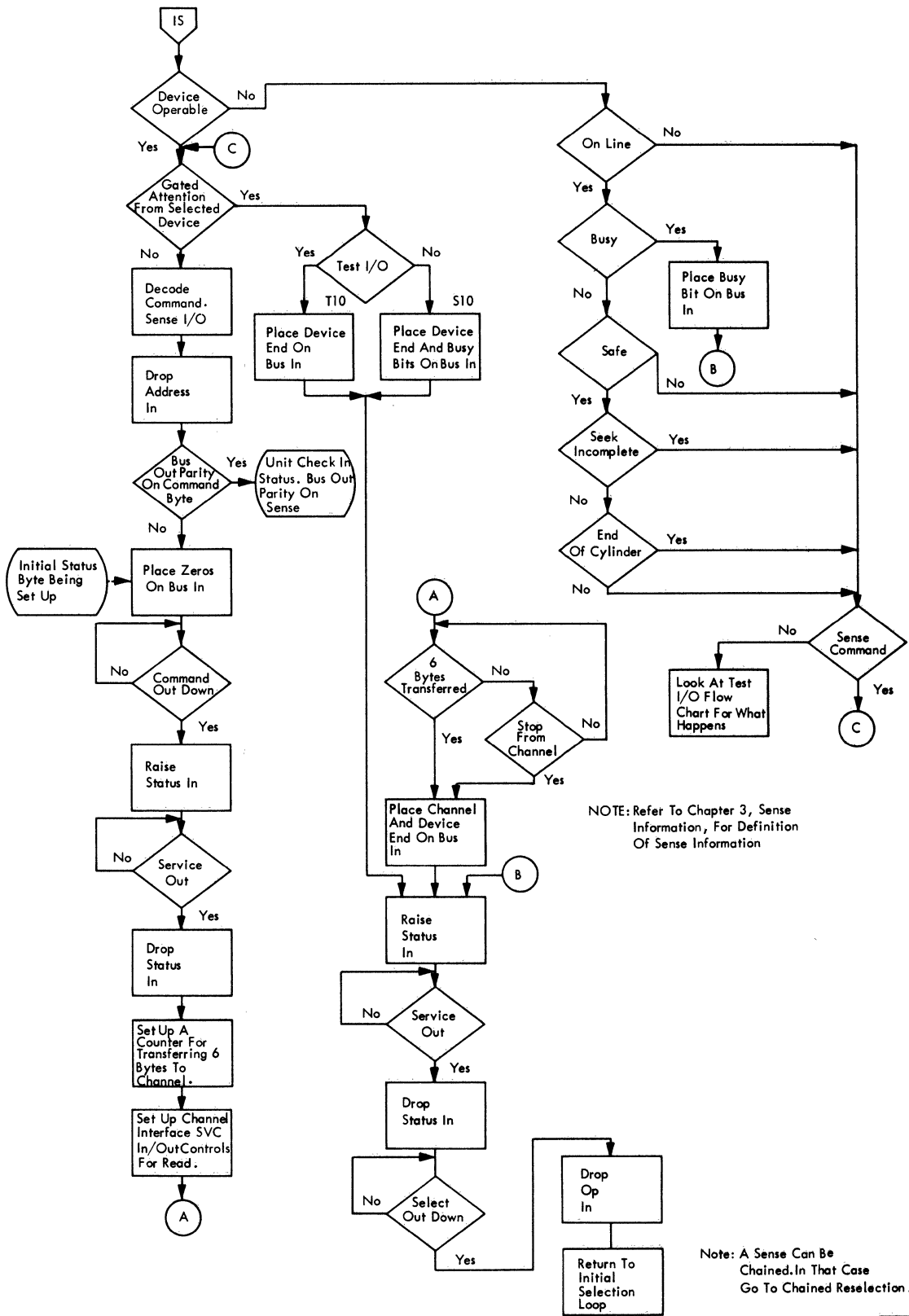
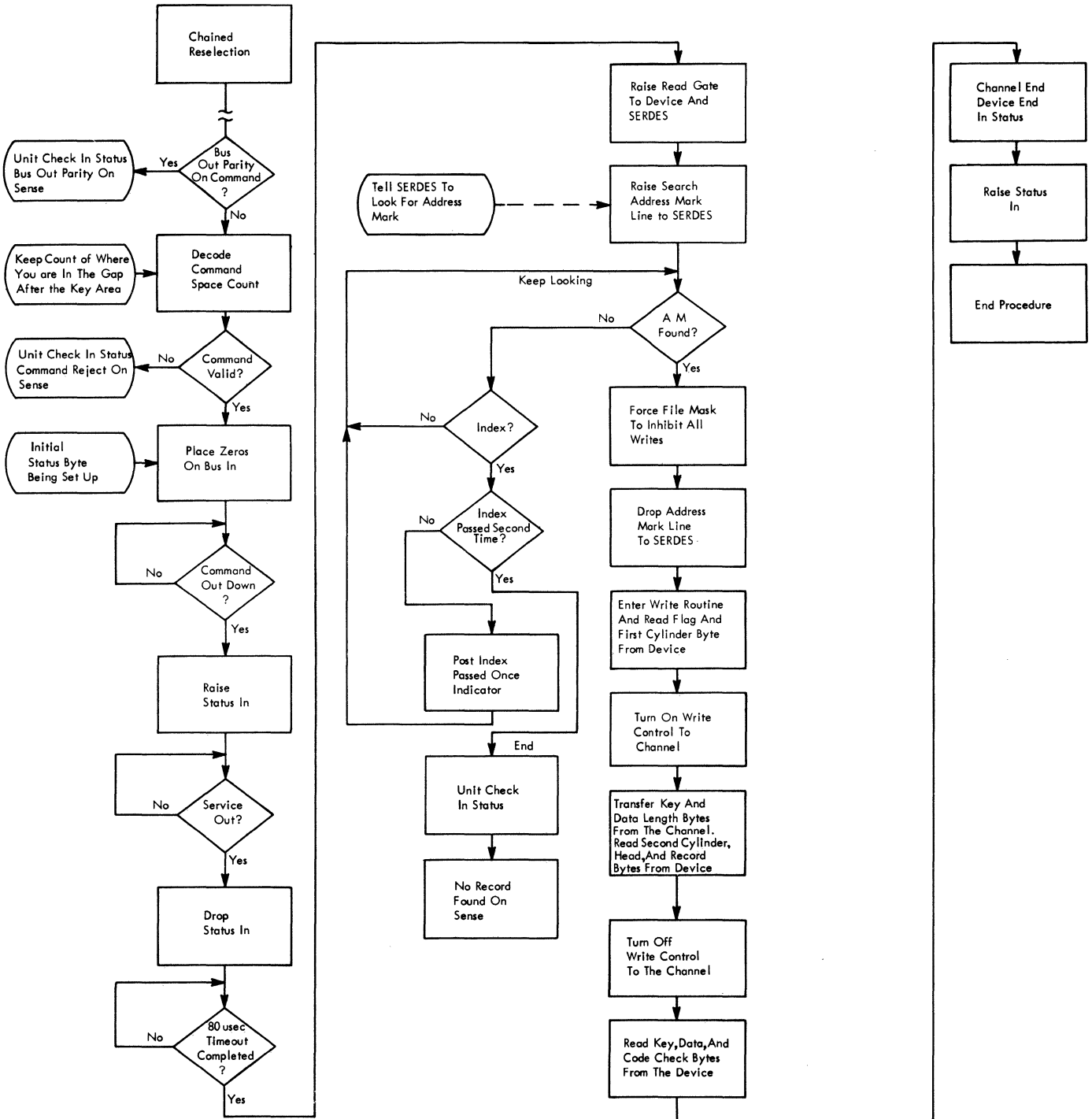


Figure 3-20. Sense I/O

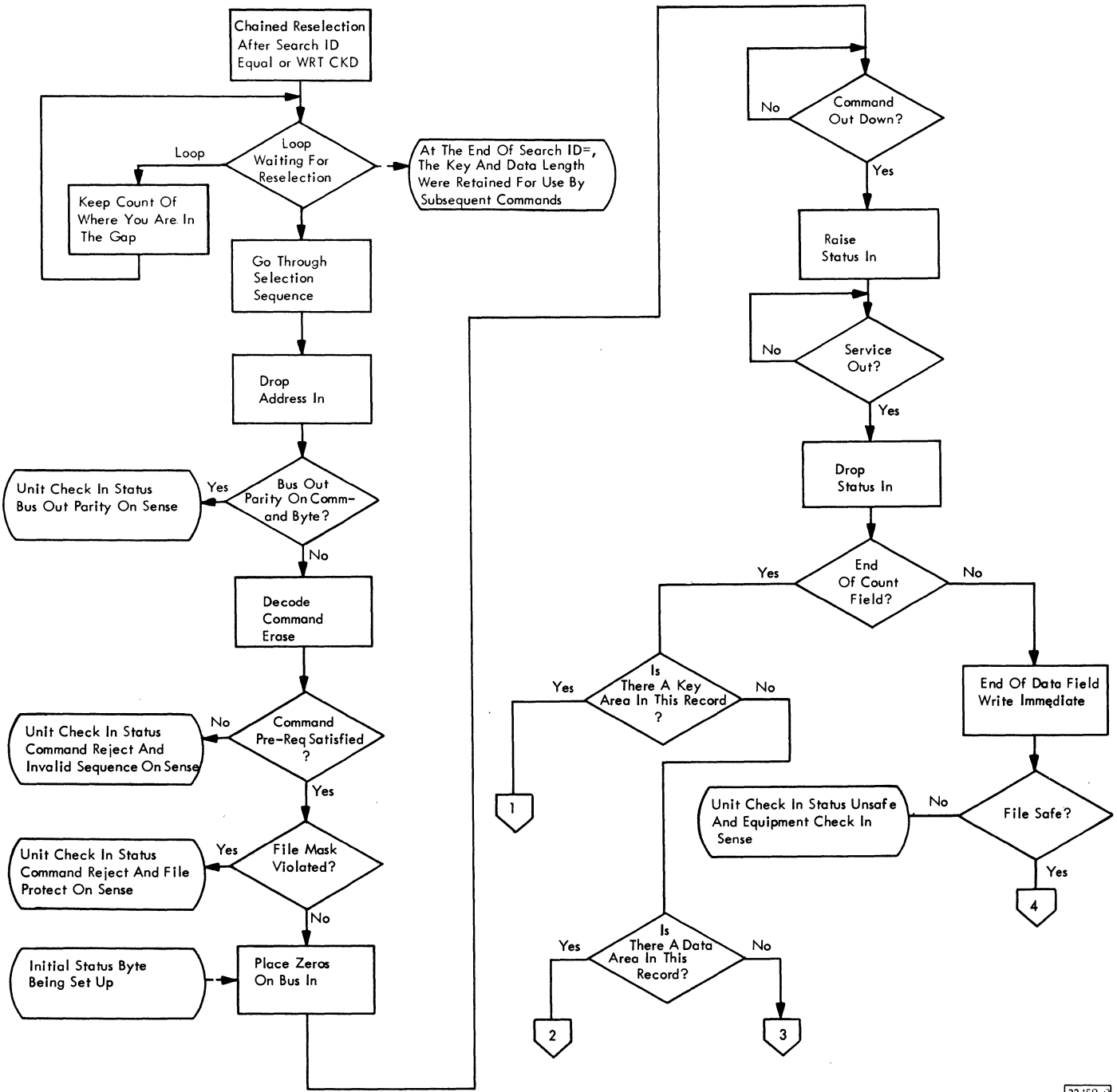
Assume: CC SRCH KEY =  
 TIC \* - 8  
 Space Count  
 At the end of Srch Key =,  
 the key and data length were  
 retained for use by subsequent  
 commands



22449

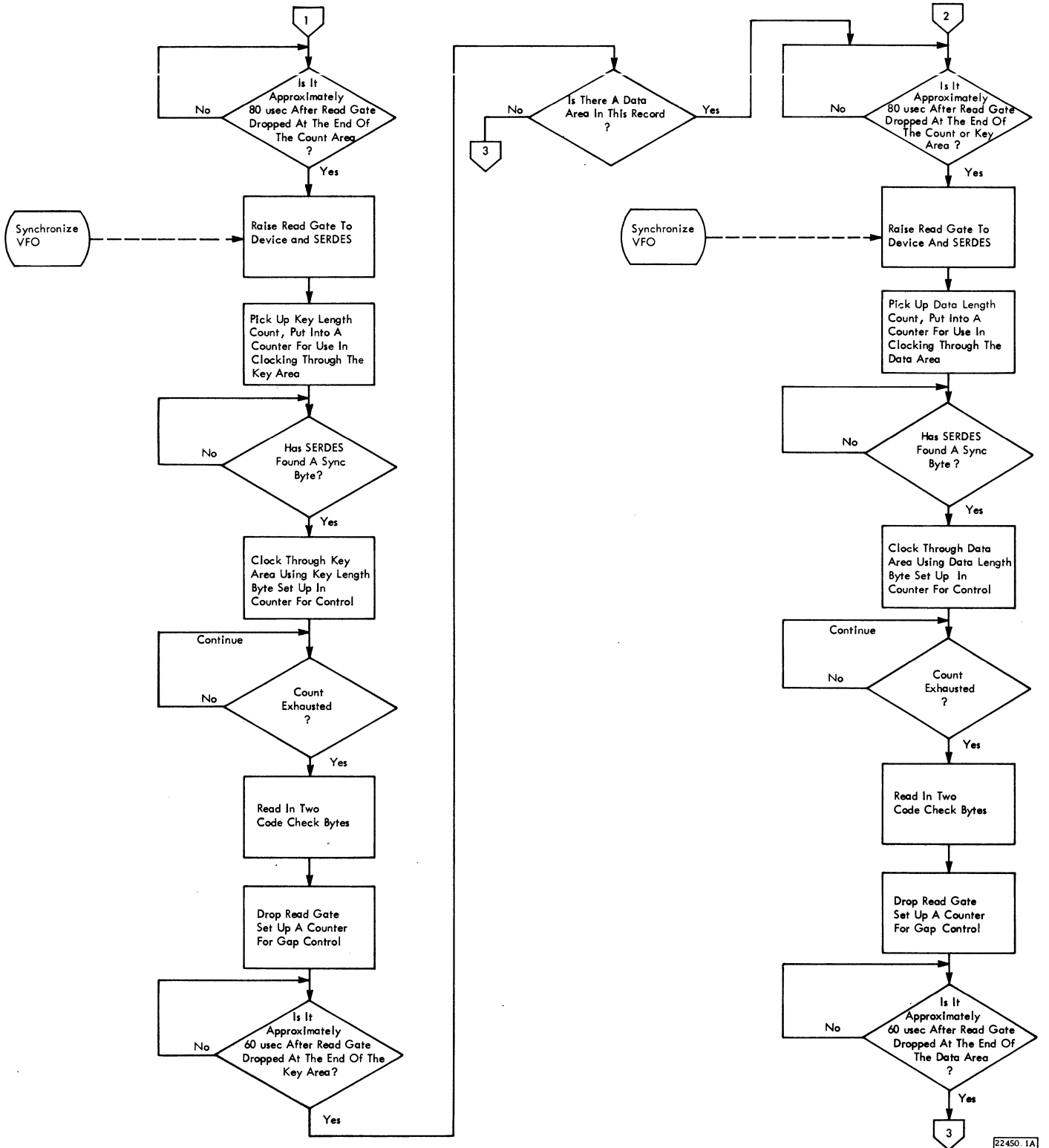
Figure 3-21. Space Count Command - 2311





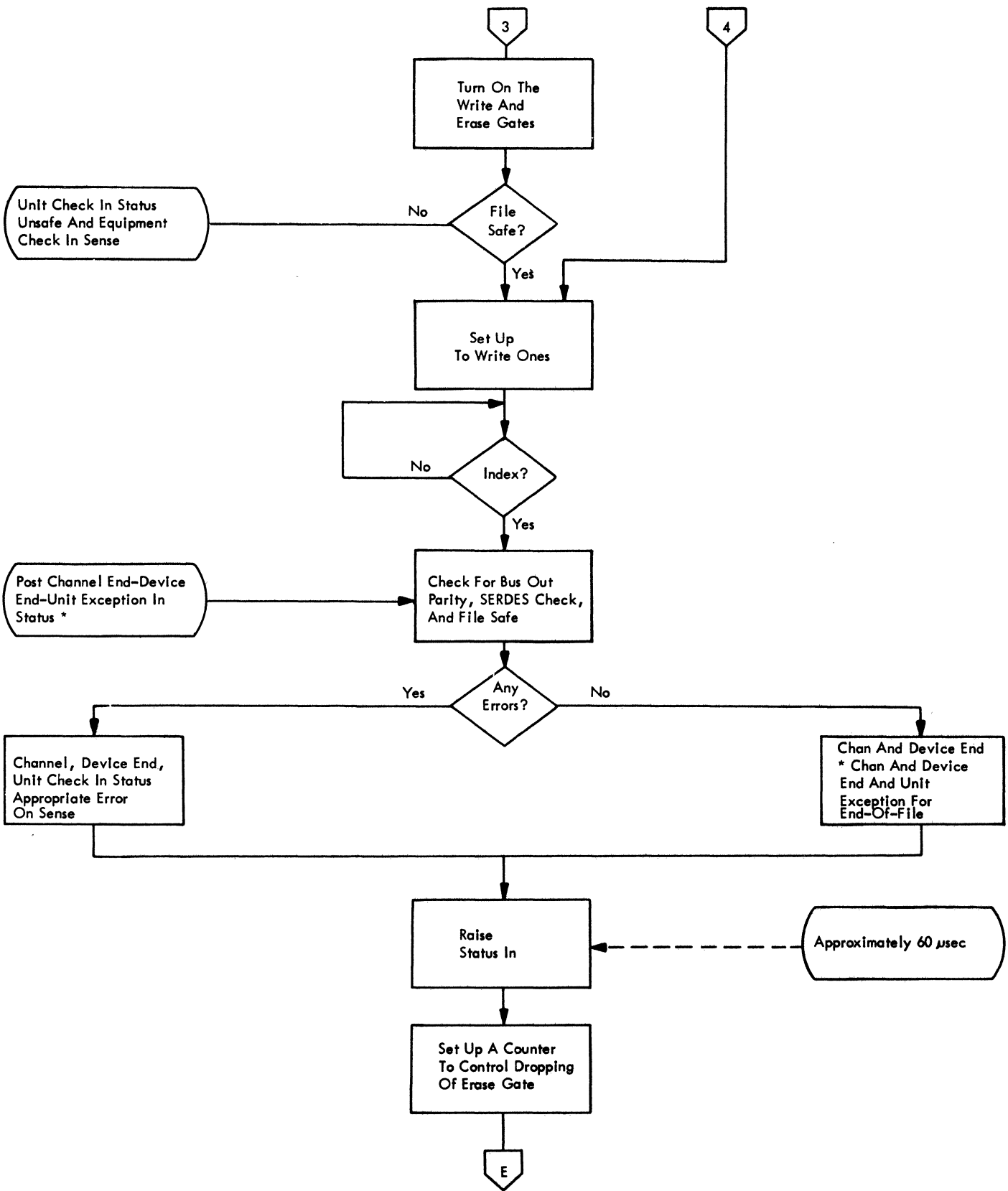
22-450.0

Figure 3-22a, Erase Command - 2311



22450. 1A

Figure 3-22b. Erase Command - 2311



22450.2

Figure 3-22c. Erase Command - 2311

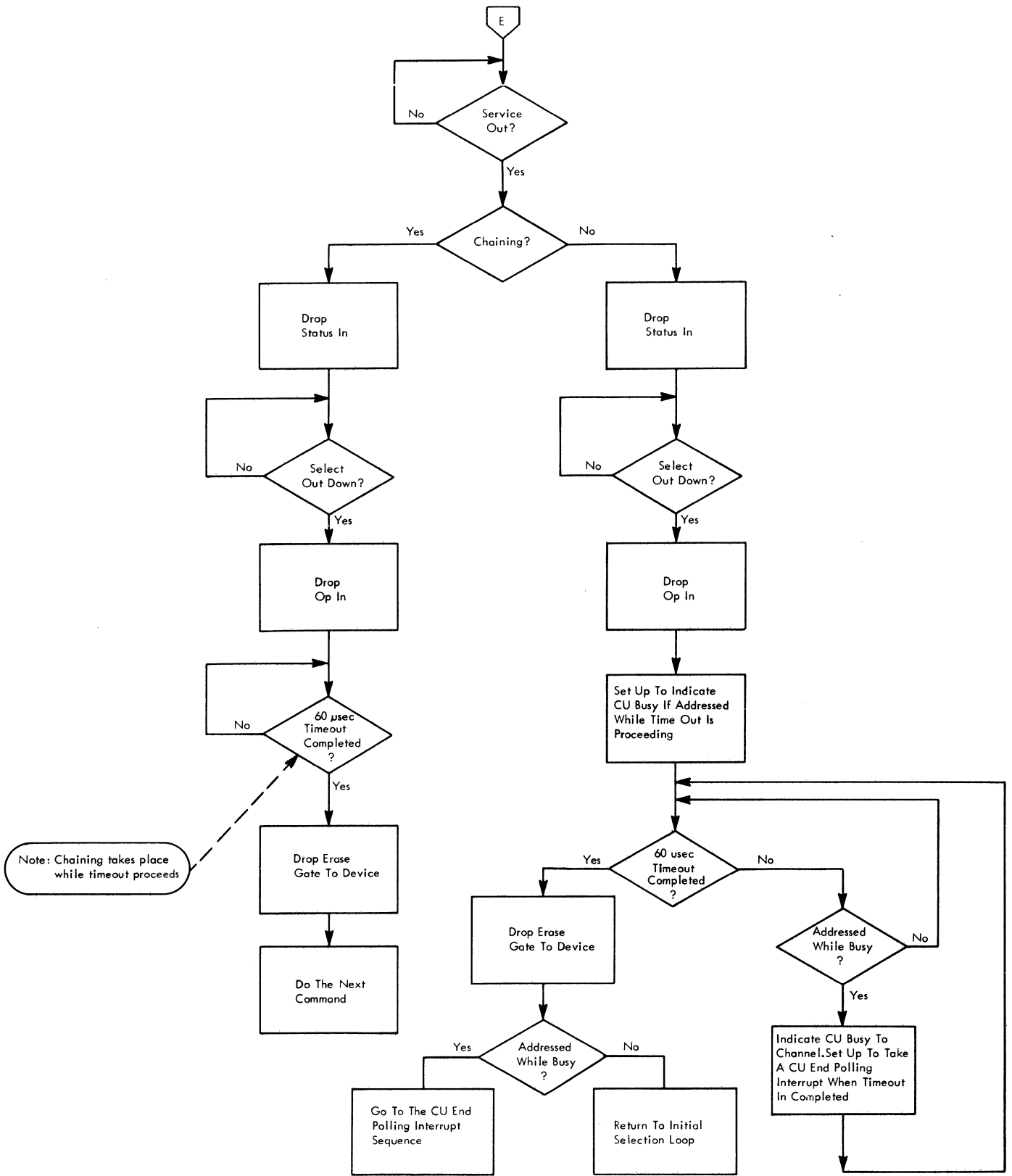


Figure 3-22d, Erase Command -2311

22450.3

### 3.5 CONDENSED MICROPROGRAM LOGIC

The purpose of this section is to give the overall organization of the microprogram (Figure 3-23). A functional description of each section of the program is included.

Register usage and bit coding is given on CLD pages QA008 and QA009. Status register and OP register bit usages are given on the CLD pages on entry to a section of the microprogram.

The microprogram is printed on the CLD's in full feature form. To follow the CLD's use the blocks that are in the machine depending on the features installed. (Refer to microblock symbology, line 7 for replaceable-word-code assignments.)

Refer to the TROS bit assignment chart (Figure 2-39), Figures 2-3 and 2-4, and the CLD's to the follow the flow.

#### 3.5.1 General

The operational microprogram is divided logically into five general sections and several sub-sections within each section (Figure 3-23). These sections are:

1. Select the 2841
  - a. Initial selection
    - 1) Channel initiated (start or test I-O)
    - 2) Polling interrupt (2841 initiated)
  - b. Chained reselection (command word chaining)
2. Command decode
3. Initial status presentation
  - a. Write immediate
  - b. General
4. Command execution
  - a. Load counts
  - b. Control commands
  - c. Read and clocking commands
  - d. Write commands
  - e. Search/scan commands
  - f. Gap spacing routine
  - g. Burst byte and exit decisions
  - h. Decode sense information
5. End procedure
  - a. Disconnect from channel
  - b. Deselect file

#### 3.5.2 Initial Selection

After a power on reset or at the end of a chain of commands, the microprogram enters the initial selection routine. The program loops, and is waiting for SELTO to rise. Two ways for SELTO to rise are:

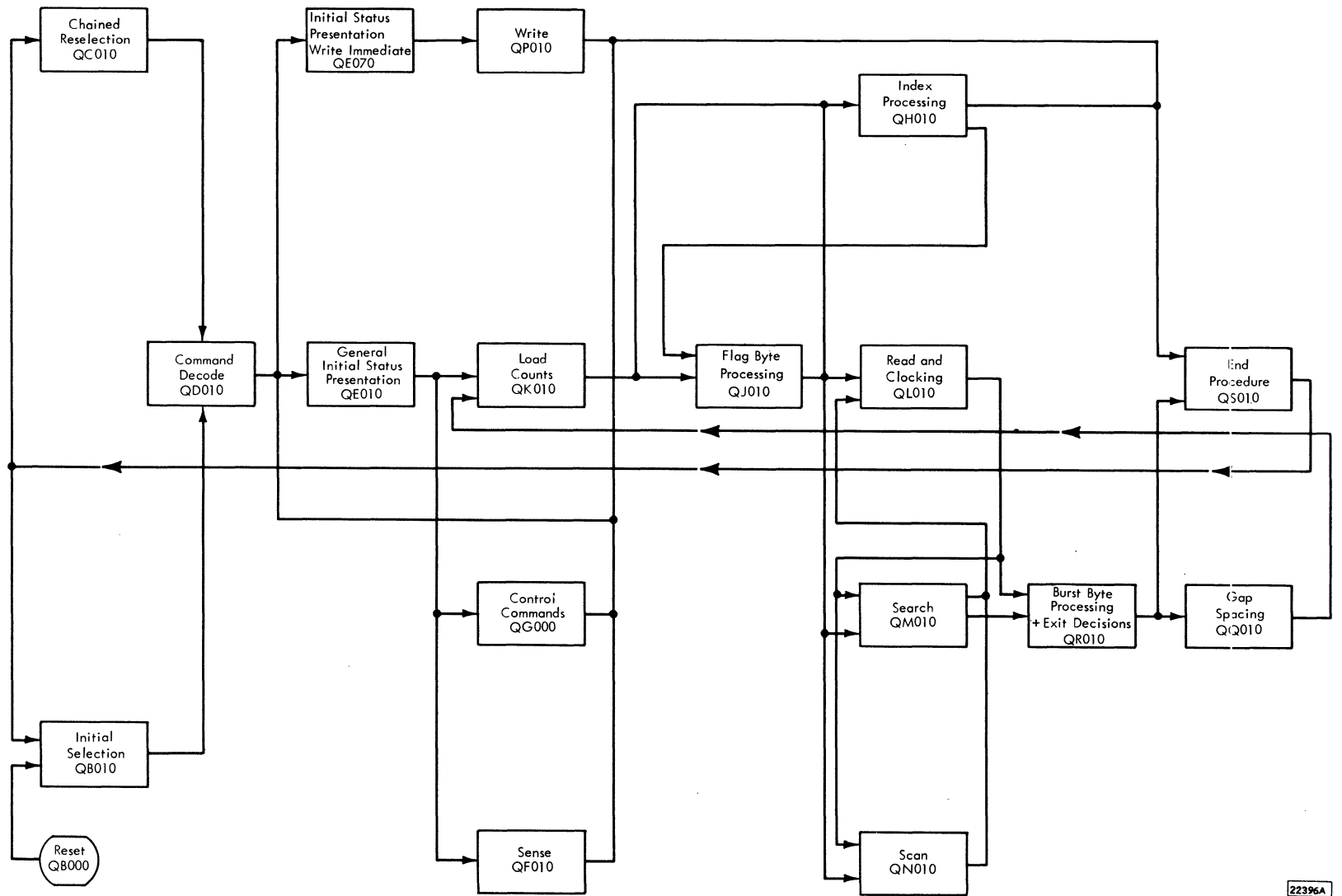
1. A start or test I/O is given and the control unit part of the address out byte matches the pre-wired 2841 CU Address.
2. The 2841 raising request in (polling interrupt) allows SELTO to rise when channel transmits select out.

SELTO up causes the 2841 to branch out of the loop to microblocks which test for type of selection. SELTO can be raised by one of the following:

- a. SELTO comes up via polling interrupt and is most likely a result of interrupt channel A from unchained SEEK commands.
- b. SELTO comes up via polling interrupt with ST (2) on, indicating some status information stacked in the 2841.
- c. If SELTO comes up via polling interrupt with ST (2) on, this indicates that the 2841 was addressed while finishing a write operation. This condition indicates that the CU was busy when addressed and is not now busy causing request-in to be set by the queued latch. The CU now transmits a CU end status byte.
- d. SELTO was raised from channel by a start or test I/O command.
- e. In this case outstanding status is also held in the 2841.

The following items are accomplished in the initial selection routine:

1. Operational-in raised.
2. Poll-enabled and queued latches reset.
3. The file mask information is reset.
4. The device part of the address-out byte is converted from 3-bit channel coding to one of eight bit module select type coding.
5. Address-in is raised.
6. The module select number is used in determining the type of device selected. This is accomplished by two CE punched ROS words. It is necessary for the 2841 to know the device type since there are slight differences in the microprogramming for each type.
7. The device type interface is selected. For 2311 this is accomplished with an 1 → FT statement. This selects the 2311 file tag interface register, thereby routing the output of UR to the 2311's. 2 → FT or 4 → FT selects the feature device file tag register, and blocks the 2311 file tag register. In this way, the output of UR is routed to the feature devices.
8. The interface is checked for unselected status. If there is any, the microprogram posts unselected status, waits for command-out, goes to the end procedure, transmits unit-check to the



22396A

Figure 3-23. Condensed Microprogram Logic

channel, and expands the error into 3 sense bytes, when a sense command is received.

9. Select a file by placing module select number in UR.
10. Wait for command-out.
11. Check operable. If inoperable, expand into either off line, busy, unsafe, seek-incomplete, or end-of-cylinder indication.
12. Check gated-attention. If gated-attention from a selected device is up on a test I/O operation, device-end in the initial status byte is set. Device-end and busy are set in the initial status byte on a start I/O operation. For both commands, device-end is cleared if channel does not stack the status byte.
13. Raise control and head-select tags.
14. The microprogram now exits to command decode.

### 3.5.3 Command Decode

Command Decode has entries from initial and chained reselection. In this section, the command is first decoded into either control, read, search, write, or test/sense I/O. The commands are then further decoded into IPL, HA, count, key, data (or combinations of these), control, sense or test I/O. Testing of the command by the file mask is done in this section. If the command violates the mask, the program exits to end procedure. In this section, the original command byte is destroyed and a new one formed. (Refer to QA009 for coding of the orientation data which identifies where the last command ended.)

All of these commands exit to the initial status presentation routine in order to present initial status to the channel. As the microprogram must have a method of entering the section of the microprogram selected by the command decode after presenting status, the operation register is set with a constant to allow branching to the selected section.

In addition, one of the registers is set with a code to indicate to the microprogram the types of fields, if any, to space over before starting the execution of the command.

#### Examples:

1. An unorientated read data command with the MTM bit off. BY equals: 00010110. This indicates a read data operation, with a skip of two fields before execution.
2. A write data command chained from a search key equal. BY equals: 10011000. The last

command ended after a key area. The microprogram next begins in a data area.

### 3.5.4 Initial Status Presentation

#### 3.5.4.1 General

This section is used to present initial status to the channel. In addition, the timing relationship to the track is maintained if the microprogram is oriented to the track. Also, index is checked in case read or write gate is still up. Read gate, if down, is turned on by the initial status routine. If the command does not need read gate up, it is reset in the command section.

#### 3.5.4.2 Write Immediate

This area is used to present initial status to channel for all commands which begin writing immediately. The timing relationship to the track is maintained.

At the proper time, write and erase gates are raised. Based on the previous setting of ST register bits, the microprogram either begins writing bytes of zeros (alpha gap), or continues writing bytes of ones (After a formatting write, not HA).

If there are no errors, exit is to the load counts section. OP now contains the type of operation and the track orientation necessary to accomplish the operation.

### 3.5.5 Load Counts

The load count routine is used on read and search/scan operations. It checks the type of command (CKD, KD, D), the present orientation to the track and sets up to read or clock the next field. The routine must maintain the totals of key length and data length for use in the gap spacing routine.

Load count also checks for end-of-file, data length of zero condition, missing key area, and key length zero. The load count routine sets up the controls to handle these conditions in the read or search/scan routines.

### 3.5.6 Write Operations

The write routine is entered from either the general section or the write immediate section of initial status. The write routine writes gaps (including address markds), handles service in/service out responses to receive data from the channel, and ST4 responses to supply bytes to SERDES.

This routine has its own load count section. It must keep track of orientation to the track for formatting the track and writing the beta gap. The alpha gap is written in the gap spacing routine. The routine loops within itself until the last area is written. It then exists to the end procedure.

### 3.5.7 Control Operations

The control command section is a group of routines which handle the control commands. The device type and the type of operation to be done are determined by the microprogram. Seek limits are set up depending on device type. The service in/service out responses are handled in order to transfer the address data to the 2841. The address data limits are checked. The address data is decoded. The address data and the proper tags are sent to the devices. The tags vary depending on the device type.

This section also handles the set-file-mask command. The mask data is received from the channel and stored for use on seek and write commands. Checking commands with the file mask is done in the command decode section.

The space-count and erase commands are handled in the write section even though space-count is classed as a control command.

### 3.5.8 Sense Operations

The sense I/O routine is entered from the initial status presentation routine after the status byte has been accepted by the channel.

A test is performed to see if the sense information is stored. If the information is not stored, the routine transfers bytes of zeros to the channel with the exception of the file status byte. If the information is stored, up to six bytes of information are transferred to the channel depending on the count in the CCW. The routine controls the service-in/service-out responses for the transfer and keeps track of how many bytes have been transferred. Exit is made to end procedure.

### 3.5.9 Flag Byte Processing

The flag byte processing routine is entered on all address-mark-search, read or search HA and read, write or search R0 operations. This routine checks for missing address marks, overflow records, and track condition bits. On search HA commands, the routine also stores the flag byte to be used in writing flag bytes on other records on the same track.

Exit is to the read/clocking or search/scan routine if the track condition is good. If the track condition is defective, exit is to end procedure.

### 3.5.10 Index Processing

The index processing routine may be entered from initial selection on read, write, search HA or R0 operations.

This routine checks for missing address marks, no-record-found indications and timing conditions when index is needed to control the operation.

On write-home-address operations, the index processing routine requests the flag byte from the channel and sets up to control the size of the HA gap.

On multi-track operation, this routine handles head advancing and checks for an end-of-cylinder condition.

### 3.5.11 Read/Clocking

The read/clocking routine is entered from flag byte processing, search/scan or gap spacing.

The read routine must service the ST4 responses from SERDES, transfer the byte through ALU to insert the parity bit if needed, generate burst bytes and handle the service-in/service-out responses to transfer the information to the channel. The routine also handles field count decrementing to determine when the field operated on has been completed.

The routine is used for clocking over areas that are not needed for the command being done, i. e., key area on a read data CCW. This is done by not setting up the service-in/service-out response. Therefore, no data is transferred to the channel. Burst byte generation is done but errors do not cause an exit to end-procedure while clocking.

Orientation to the track is updated in the read/clocking routine so that the proper decisions may be made in the burst byte and exit decisions section.

### 3.5.12 Search Operations

The search routine handles the service-in/service-out responses in write mode in order to transfer data from the channel. The search routine also handles the ST4 responses from SERDES in order to transfer data from the device. The routine transfers data through the ALU for parity generation. Burst bytes are also generated. The data from the channel and the data from the device are compared on a byte-for-byte basis for high, low or equal as determined by the command. The routine sets controls which later cause setting of the status modifier if the conditions are satisfied.



Exits are made to burst byte processing or clocking routines as called for by the type of command.

### 3.5.13 Scan Operations

The scan routine replaces the search routine if the scan feature is installed.

Search operations work in the same manner as before.

Scan operations are the same as search operations with these exceptions:

1. The scan routine must be able to suspend comparing when a mask byte (Hex FF) is received from the channel.
2. Because scan operates on the data area as well as on count and key areas, the scan routine must decrement a two-byte count.

Exit is made to burst byte processing or clocking routines.

### 3.5.14 Burst Byte and Exit Decisions

Entry to the burst byte and exit decisions section is from read/clocking or search/scan routines.

This routine reads the two code check bytes and exclusive OR's the two check bytes with the generated burst bytes, and checks both bytes for zero. If the result is not zero, set burst error condition for use in the sense bytes.

Track orientation is updated in this routine and an exit decision is made to return to read/clocking or search/scan by way of the gap spacing routine or exit to end procedure.

### 3.5.15 Gap Spacing Operations

Entries to the gap spacing routine are from the burst byte and exit decision routine, or from the gap writing routine. The gap spacing routine contains a timer which is set up to control the resetting of read gate and the timing out and turning on of read gate. Read gate is turned on in order to read the sync byte in the gap to locate the next record. Exit from the read gap spacing routine is to the index processing routine on overflow records or to the initial status presentation routine. Entry to the initial status routine is made after the presentation of status is complete in order to make decisions on entering the next area.

The gap writing routine contains a timer to control the number of bytes written in the gap. The routine also controls the byte configuration for the gaps. The number of bytes written varies depending upon the type of device being used. This routine writes up to, but not including, the sync byte which

is taken care of in the write routine. Exit from the gap writing routine is back to the write routine.

### 3.5.16 End Procedure

Entry to the end procedure routine is made from command-decode, initial-status-presentation, write, index processing, burst byte or exit decisions routines. Entry is also made from any place where an error may have occurred or an end of operation detected. End procedure determines if a chained or unchained end of operation exists and presents the ending status of the operation.

To present the ending status, the status-in/service-out response within the end procedure routine is controlled. This routine also sets up a timer on chained operations to determine if the next command is received without an over-run condition. The end procedure routine also regenerates the address of the selected device for use in the chained and initial selection routines.

Exits from the end procedure timed section for chaining operations are to the chained reselection section. Exit from the end procedure untimed routine is to the initial selection loop to wait for the next operation.

### 3.5.17 Chained Reselection

Entry to chained reselection is from end procedure in operations that are indicated as being chained from the previous operation. Because the next operation must come within a given amount of time in order to prevent running into the next area of the track, a timer is maintained to control the turning on and off of read gate, write gate and erase gate.

Checks are made within this routine for index, in case index may enter into the sequence of the operation. If an index is detected, the program exits to the index processing routine. A check is also made to see if the selected device is safe or unsafe. If the device is found to be unsafe, the routine exits back to end procedure in order to indicate to the channel that the selected device can no longer be used.

Before exiting from the chained reselection routine, an indicator is set up to indicate to command decode, whether the device is oriented for a write or a not-write condition. Exit from the chained reselection routine is to command decode in order to wait for the command and decode it before going on with the next operation.

### 3.5.18 Command Orientation Summary

Refer to Figure 3-24 for the valid orientation at the beginning and end of each command.

Command	Command Prerequisite	Valid Orientation State at Beginning of Command	Orientation State at Completion of Command
Read CKD	None	AM	Data
Read KD	None	Count	Data
Read D	None	AM	Data
Write CKD (Also Write Special CKD)	Search Equal Count or Key	Count	Data
Write KD	Write CKD	Key	Data
Write D	Write RO	Data	Data
Search ID	Search Equal Count	Count	Data
Search Key	Search Equal Count or Key	Key	Data
Search Key-Data	None	AM or IP	Count
Search Home Address	None	AM	Key
Read RO	None	Count	Data
Write RO	SFM	AM	Data
Read HA	Search Equal Home Address	Home Address	Home Address
Write HA	Write HA	IP	Home Address
Read IPL	None	IP	Home Address
Read Count	SFM	AM	Data
Control Space	None	AM	Count
Record	Search (any)	AM	Reset Orientation
Control Erase	Read (any)	AM	Reset Orientation
Control NOP	Search Equal Count or Key	Count	Reset Orientation
	Write CKD	Key	Data
	Write RO	Data	Data
	None	Any	Reset Orientation

22023

Figure 3-24. Command Orientation Summary



4.1 GENERAL POWER SUPPLY DESCRIPTION

The 2841 contains the necessary power supplies for the operation of 2841 circuitry and certain voltages for the attached devices. The 2841 power supplies furnish the following voltages for internal use:

+6 vdc, +3 vdc, -3 vdc, +12 vdc, -36 vdc

In addition, the 2841 supplies the following voltages to the attached 2311's in the subsystem:

+6 vdc, +3 vdc, -3 vdc, -36 vdc

Power input to the 2841 is 208/230 vac 3 phase 30 amperes for 60 cycle machines. Power input for 50 cycle machines in 195, 220/380, or 235/408 vac 3 phase. Taps are provided on the input transformers of the power supplies to match the voltage supplied by the customer.

Each power supply is equipped with a voltage regulator card and a circuit breaker for over-current protection. The output voltage of each of the supplies can be adjusted by means of a potentiometer on the supply. For more information on power supplies refer to IBM Field Engineering Manual of Instruction Solid Logic Technology Power Supplies, Form 223-2799.

All power supplies are brought up together except the +12 vdc supply which must wait until +6 vdc comes up.

The 2841 provides a controlled ground to the attached 2311's and 2303's to control power on and off sequencing of the devices. When 2303 Drum Storage units are installed, the sequencing controls first power up the 2303 units and then power up the 2311's.

The 2841 provides 208/230 vac, 3 phase power to the attached 2311's and 2303's via CB-2 and CB-3. AC power to 2303's comes directly from CB-3. AC power to the 2311's is controlled by K2 and CB-2.

The 2303's power up and down under control of the 2841 power sequence controls. The 2841 power down sequence is held up until the 2303's have powered down.

**CAUTION:** 208 vac is available to the 2303 even when the 2841 power is down. The 208 vac is used in the 2303 to keep the drum housing blower going at all times.

All DC power for the 2303 is supplied by the 2303.

Due to the AC power requirements of the 2303, the number of 2311's also on the same 2841 must be reduced. With one 2303, from zero to three 2311's can be attached. With two 2303's, no 2311's can be attached.

There are RPQ's (request for price quotation) available to attach additional 2311's.

Power on/off control of the 2841 is controlled by the CE/normal (remote) switch. With the CE/normal switch in the CE position, power must be brought up and down by means of the ON/OFF switch on the 2841 CE panel. With the CE/normal switch in the NORMAL position, power on and off is under control of the using system and the CE panel controls are inoperative. Emergency Power Off can drop power regardless of the position of the CE/normal switch. (Figures 4-1, 4-2, 4-3, 4-4.)

4.1.1 Power Supply Components

4.1.1.1 Circuit Breakers

CB - 2	20A - AC power to 2311's
CB - 3	30A - All power to K2, CB 2, and convenience outlet and 15 vac, 40 vac, 24 vac transformers.

4.1.1.2 Circuit Protectors

CP - 1	3A - +6 vdc power supply no. 2
CP - 2	3A - -3 vdc, -36 vdc,
CP - 3	3A - +3 vdc, +6 vdc no. 1
CP - 4	1A - 24 vac, +12v (1.5A, 50 ~)
CP - 5 (60~ only)	5A - Convenience outlets -115v

4.1.1.3 Contactors

K - 1	- convenience outlet contactor
K - 2	- 2311 and power supplies contactor
K - 3	- Emergency power off contactor (There will be no 24 vac control power if K3 is not up)

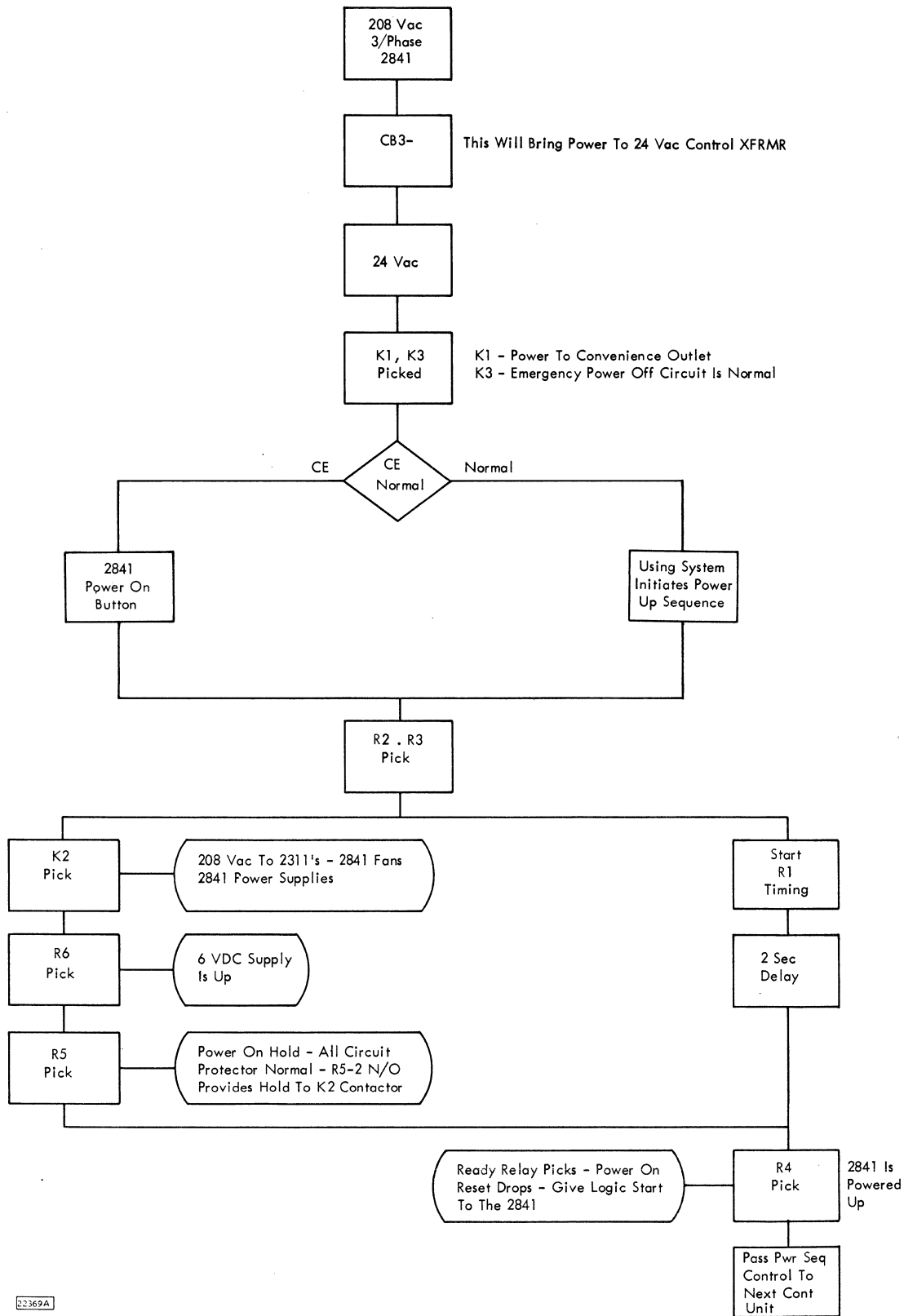


Figure 4-1. Power On Sequence

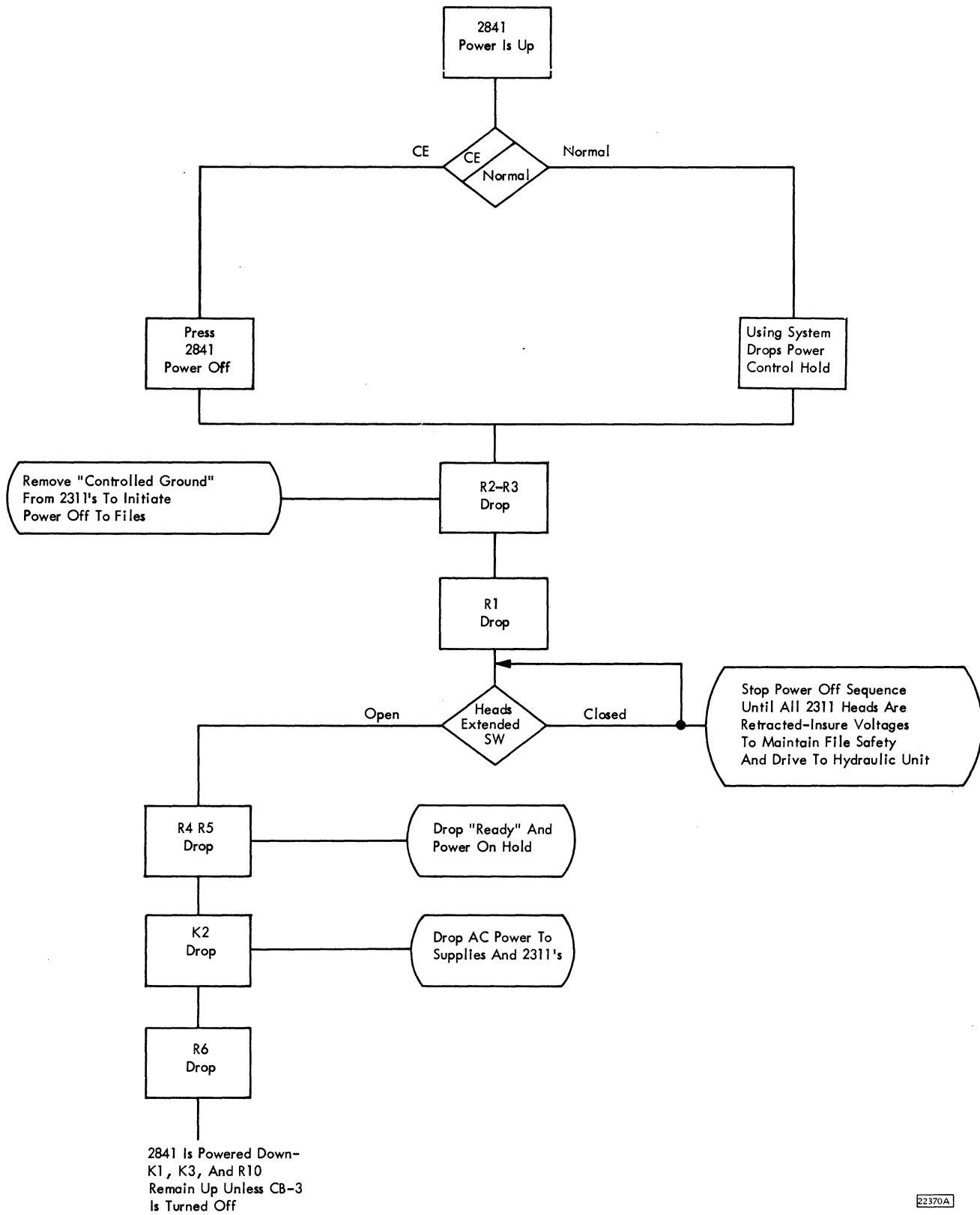


Figure 4-2. Power Off Sequence

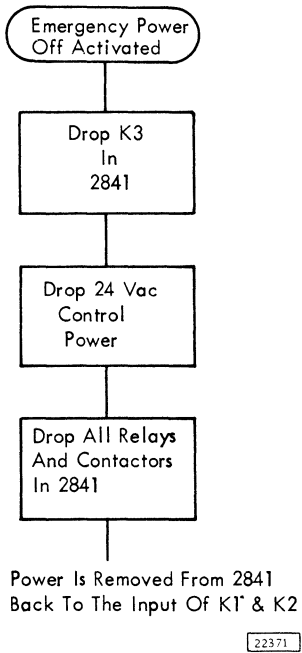


Figure 4-3. Power Off Sequence - Emergency Power Off

#### 4.1.2 Thermal Considerations

There are four thermal cutout switches. One is mounted in the TROS gate A. One is mounted above board B1 and one is mounted above board C2. The fourth thermal is mounted above the power supplies. Opening of any of the thermal switches drops R6 which drops R4 and R5 causing a normal power down sequence.

#### 4.1.3 Marginal Checking

No facilities for marginal checking are provided in the 2841 other than actually varying the voltages at the power supplies.

#### 4.1.4 Power Distribution

The power supply outputs are fed to bus bars on the front side of the 2841. From these bus bars, the voltages are distributed to various points in the machine.

The A gate receives its power via a laminated T bus which ends in terminal strips on the bottom of the A gate. The A gate receives the following voltages:

- 36 vdc
- +12 vdc
- +3 vdc
- 3 vdc
- +6 vdc
- ground bus

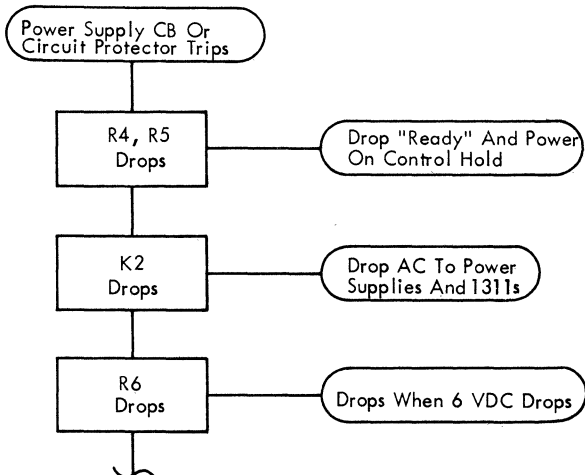
The TROS gate receives the following voltages via a laminated T bus on boards A1 and A2 on the TROS array:

- +3 vdc
- 3 vdc
- +6 vdc
- ground bus

Cooling fans for the A gate, TROS array and the power supply stack receive their ac power from terminal strip TS-1 located within the ac sequencing box on the left side of the 2841.

#### 4.1.5 Power Interlocks

Relay 1 is a 2 second time delay relay which begins timing when power sequencing is started on the 2841 (CE or NORMAL (REMOTE)). Two seconds after the sequencing has begun, the power on hold control is transferred to relay 5, if relay 5 has not picked at this time, power will sequence down. The 2 second time delay also allows 2 seconds for power on surge current to settle down before allowing the next control unit to begin its power up sequence.



At This Point The 2841 Will Not Automatically Sequence Up When The Circuit Breaker Is Restored - Place The CE/Normal Switch In CE (This Activates The Power On/Off Controls On The 2841 CE Panel)- Press The Power Off To Restore The 2841 Power Sequencing Controls- Press Power On (On 2841) To Bring Power Back Up Again.

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Figure 4-4. Power Off Sequence - Power Supply Overload or Circuit Protection Trip

5.1 2302 MODELS 3 AND 4, 2321 AND 2303 ATTACHMENT

- Provides circuitry to attach 2302 Models 3 and 4, 2303, and 2321 devices.
- Provides signals to control device operation.
- Provides signals to the basic 2841 from the devices.
- Circuitry for all three devices is on one large SLT board A3.

Board A3 provides the circuitry to attach the 2302, Models 3 and 4, 2303, and 2321 devices to the basic 2841-2311 (Figures 5-1 to 5-11).

Signals provided by the microprogram are developed and sent to the devices to control the operations. Signals from the devices are gated so that they may be used by the microprogram.

Selection of the feature interface is done by the microprogram checking the unit address with constants set in the microprogram by the CE to assign the device type to a unit address.

The microprogram selects the 2311 interface with the statement 1 → FT; the feature interface is selected with a 2 → FT or 4 → FT statement. A description of the interface lines for these feature devices is included in the applicable device FETO.

The attachment consists of the same basic units as the 2311 attachment; FT and FC registers, module selection, attention and file status gating.

The FT and FC bit decodes vary from the 2311 decodes and vary with each of the devices. The microprogram varies the set up of the control lines and timings for the type selected.

Figure 5-12 shows the differences in capacity and timing for the devices controlled by the 2841. Figures 5-13 and 5-14 show the differences in line names and controls for the devices controlled by the 2841.

The addressing scheme for the seek address varies with the different devices as shown in the following chart:

Type	Cell Number		Cylinder Number		Head Number	
	Byte 0	Byte 1	Byte 2	Byte 3	Byte 4	Byte 5
2311	0	0	0	0-202	0	0-9
2302 Mod. 3 Mod. 4	0	0	0	0-249	0	0-45
2303	0	0	0	0-79	0	0-9
2321	0	0-9	0-19 Subcell	0-9 Strip	0-4 Bar	0-19 Head No.
Example of a 2311 binary address (bit configuration)	Cell Number 0 00000000 00000000		Cylinder Number 163 00000000 10100011		Head Number 5 00000000 00000101	



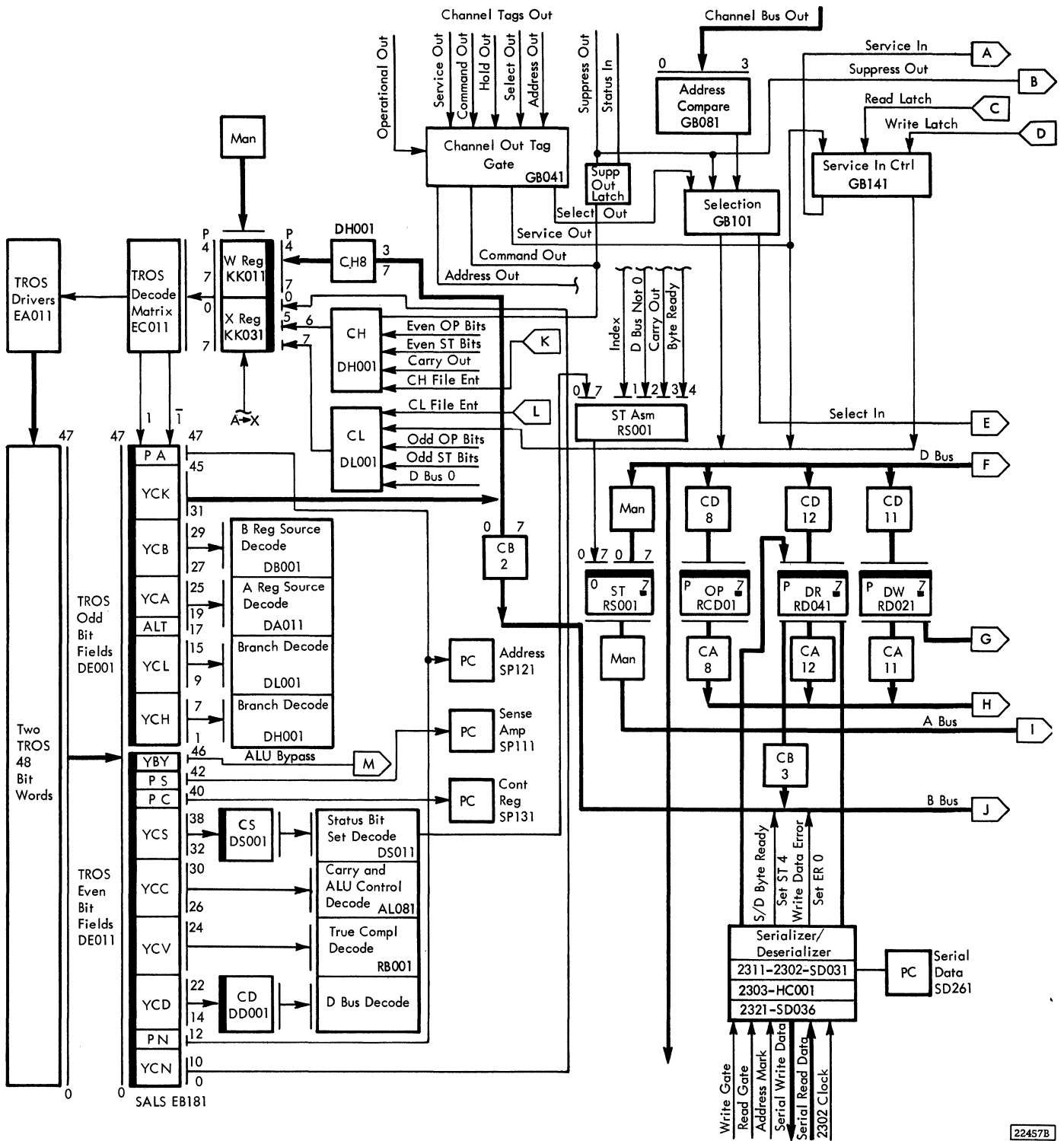


Figure 5-1a. Data Flow - Basic 2841 and Channel Attachment

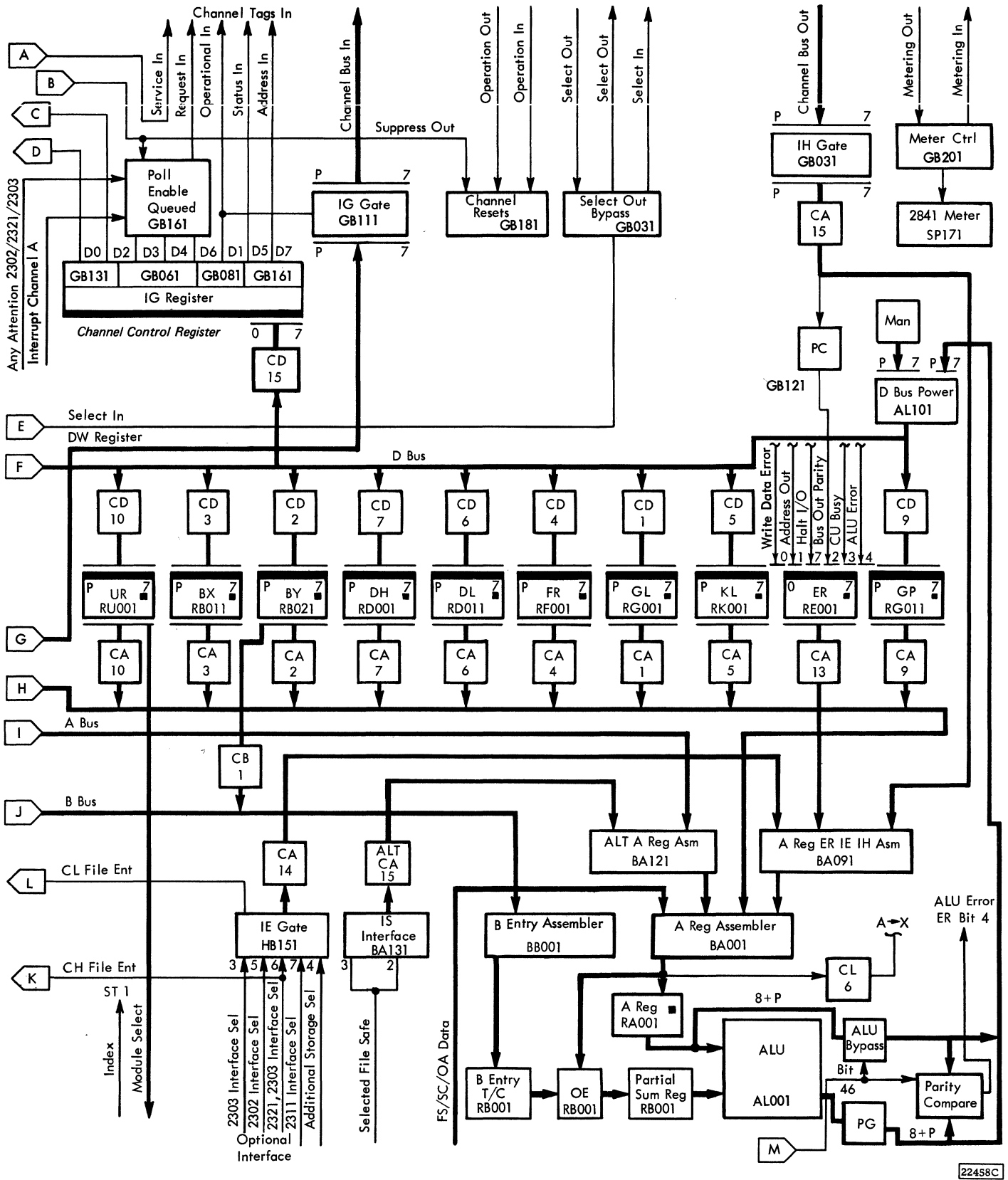
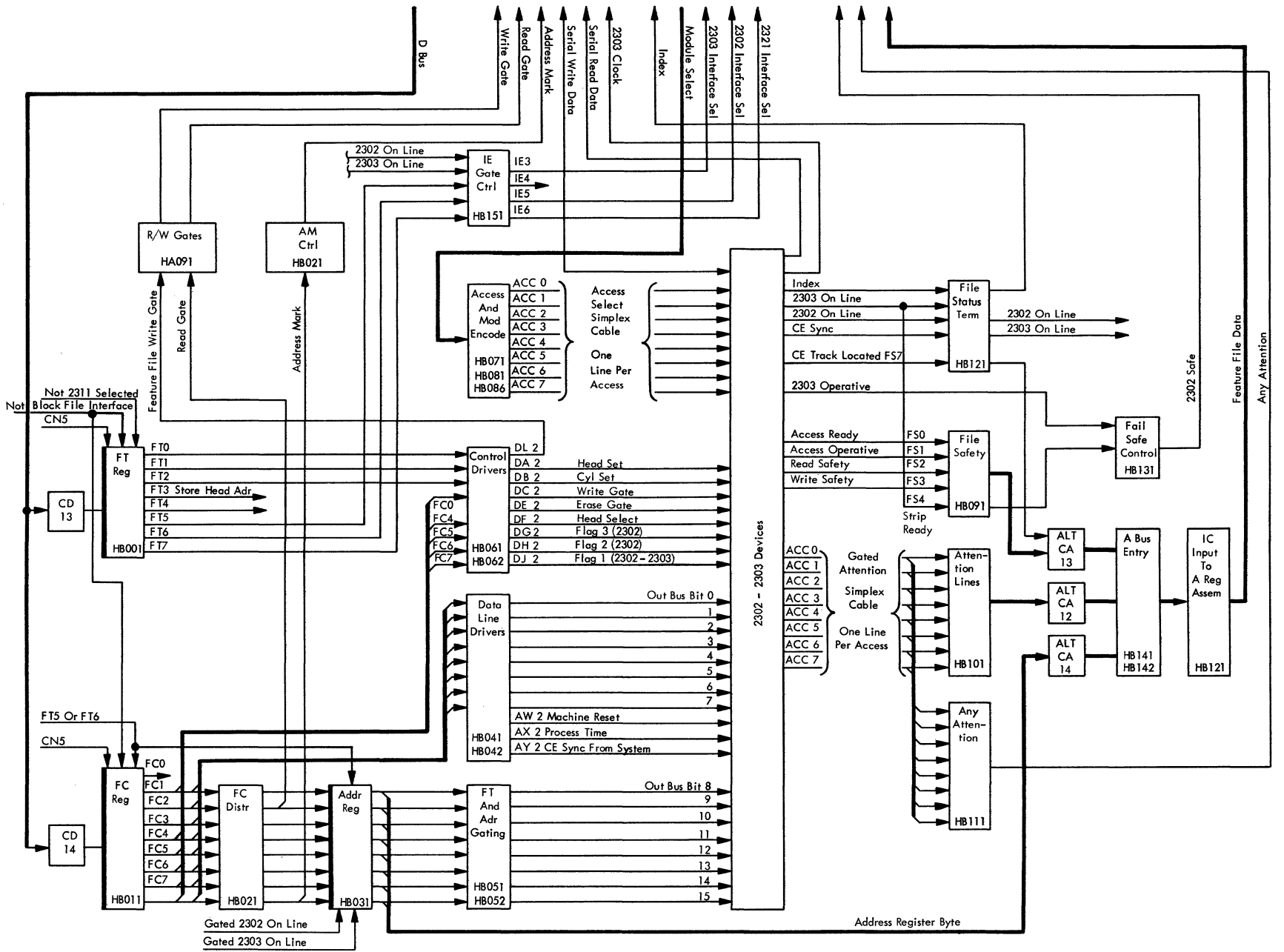


Figure 5-1b. Data Flow - Basic 2841 and Channel Attachment

Figure 5-2. Data Flow - 2302 - 2303 Attachment



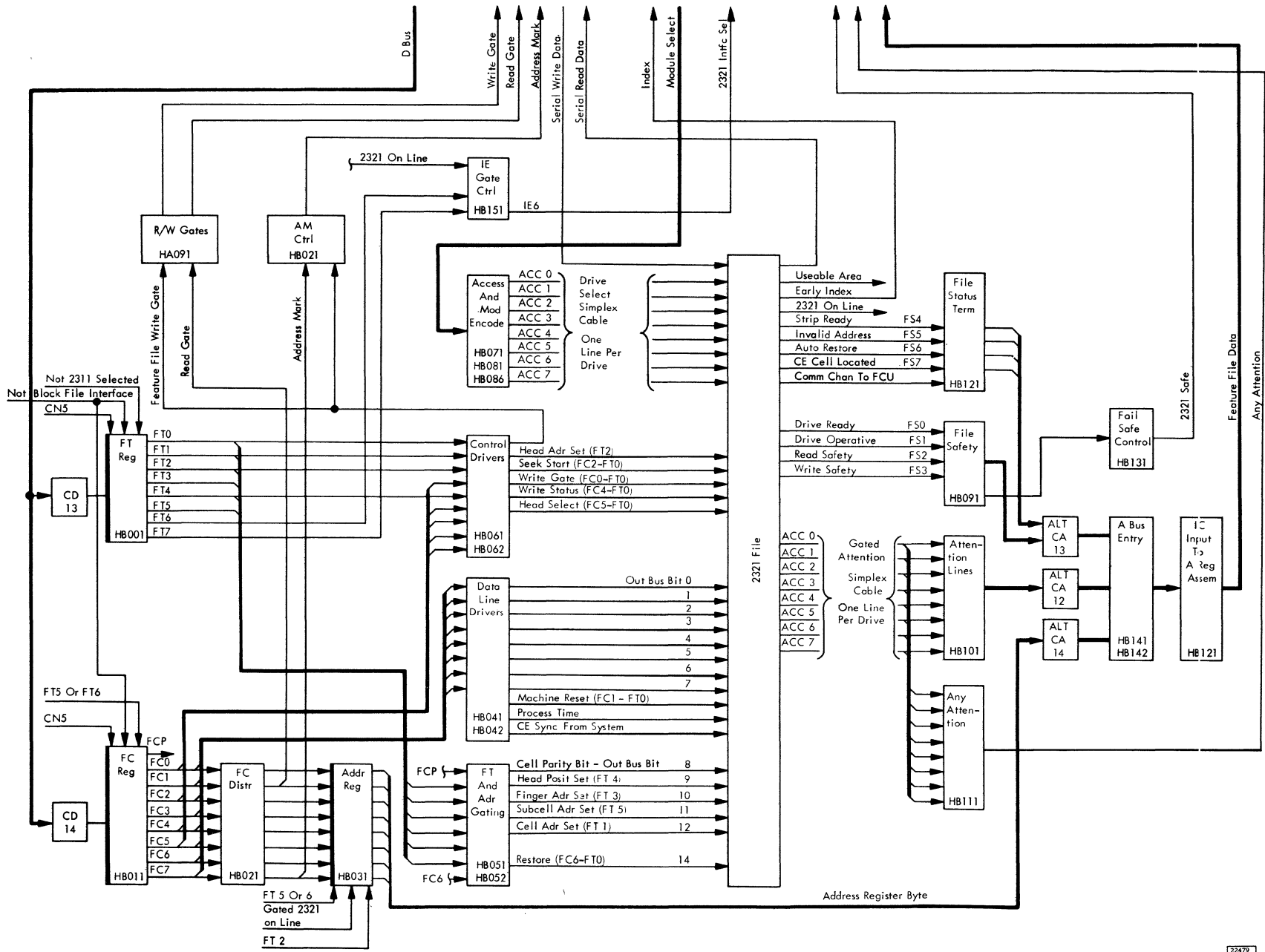
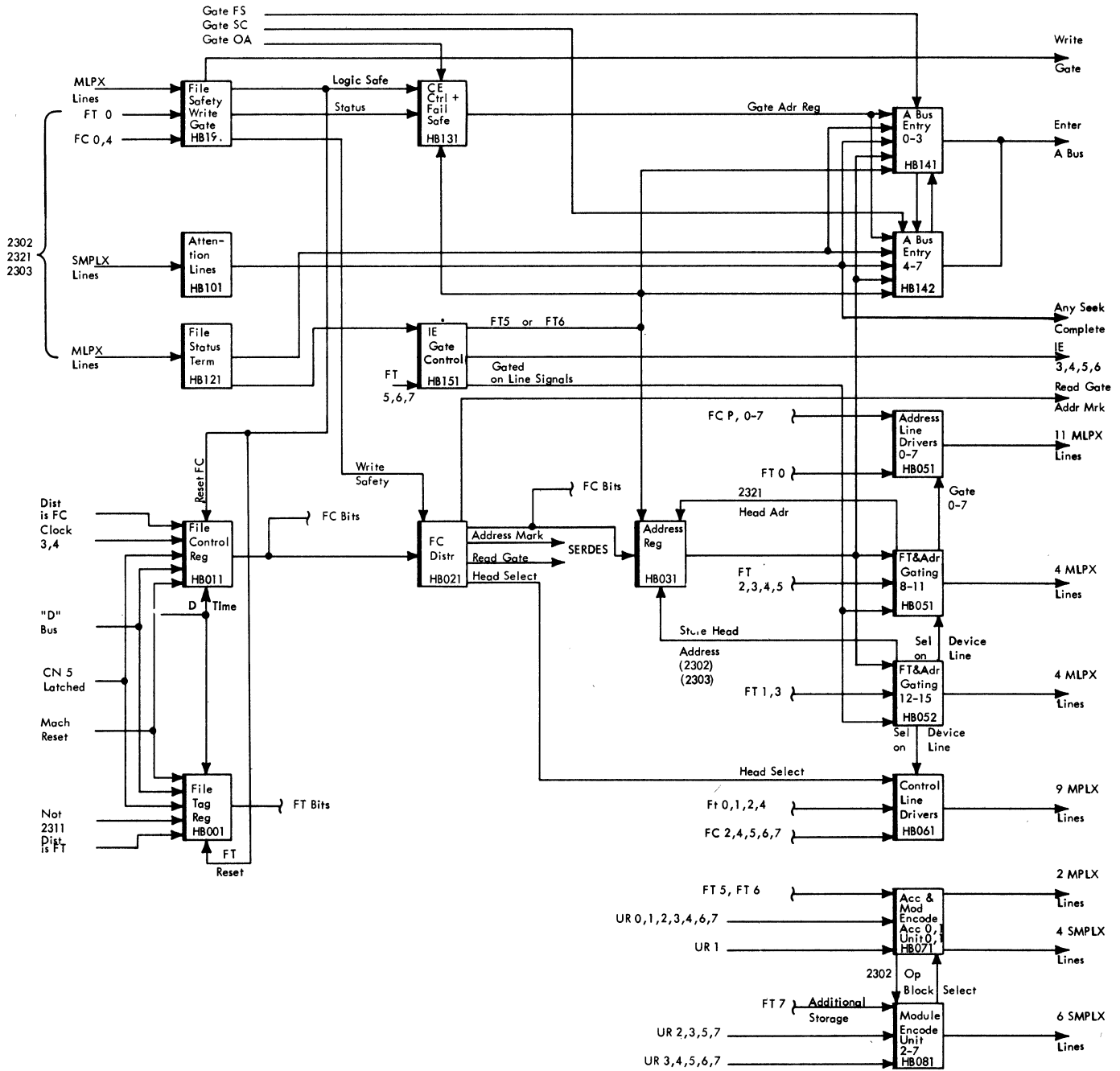


Figure 5-3. Data Flow - 2321 Attachment



22480

Figure 5-4. Feature Device Interface

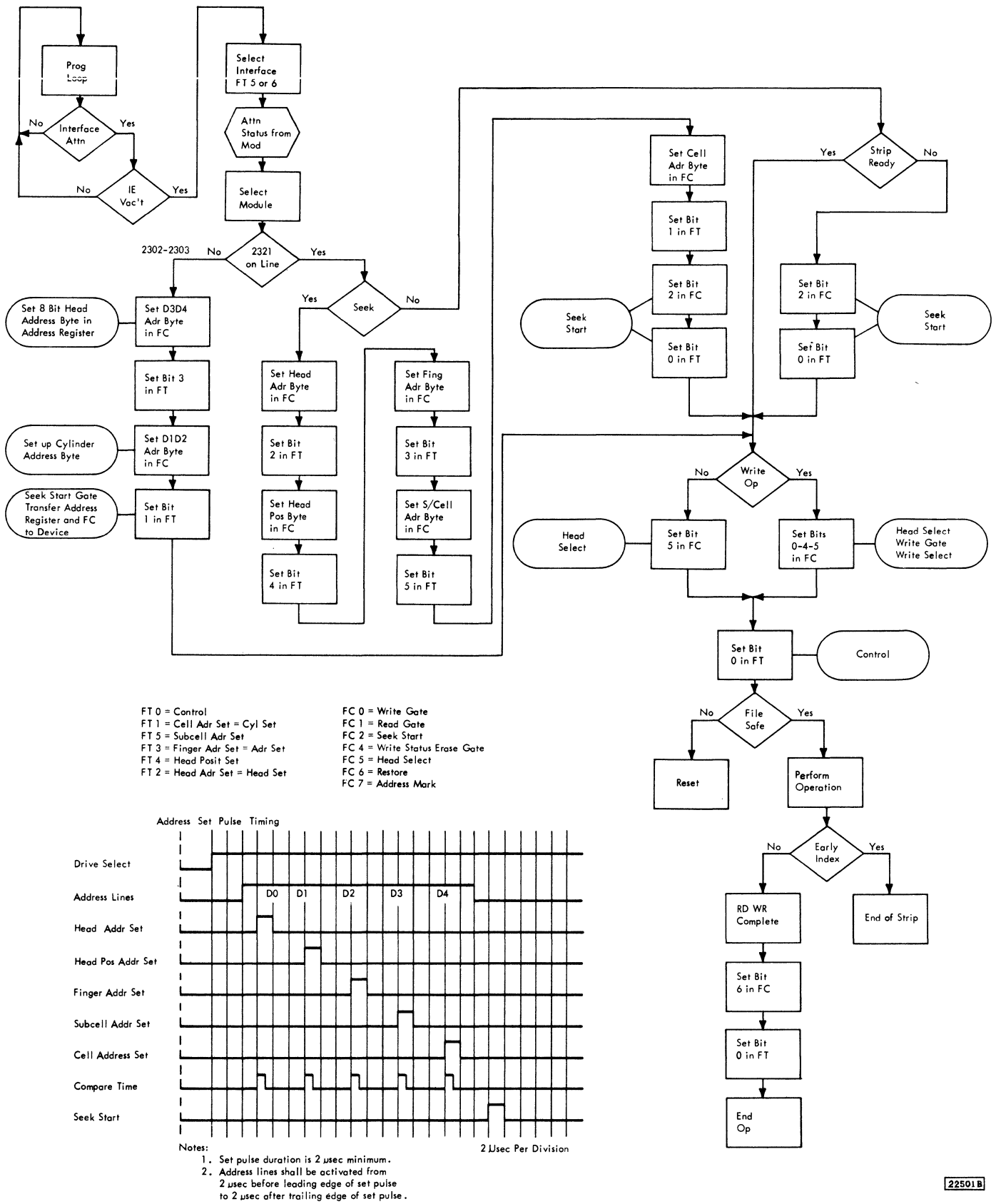


Figure 5-5. Serial Address Sequence

22501 B

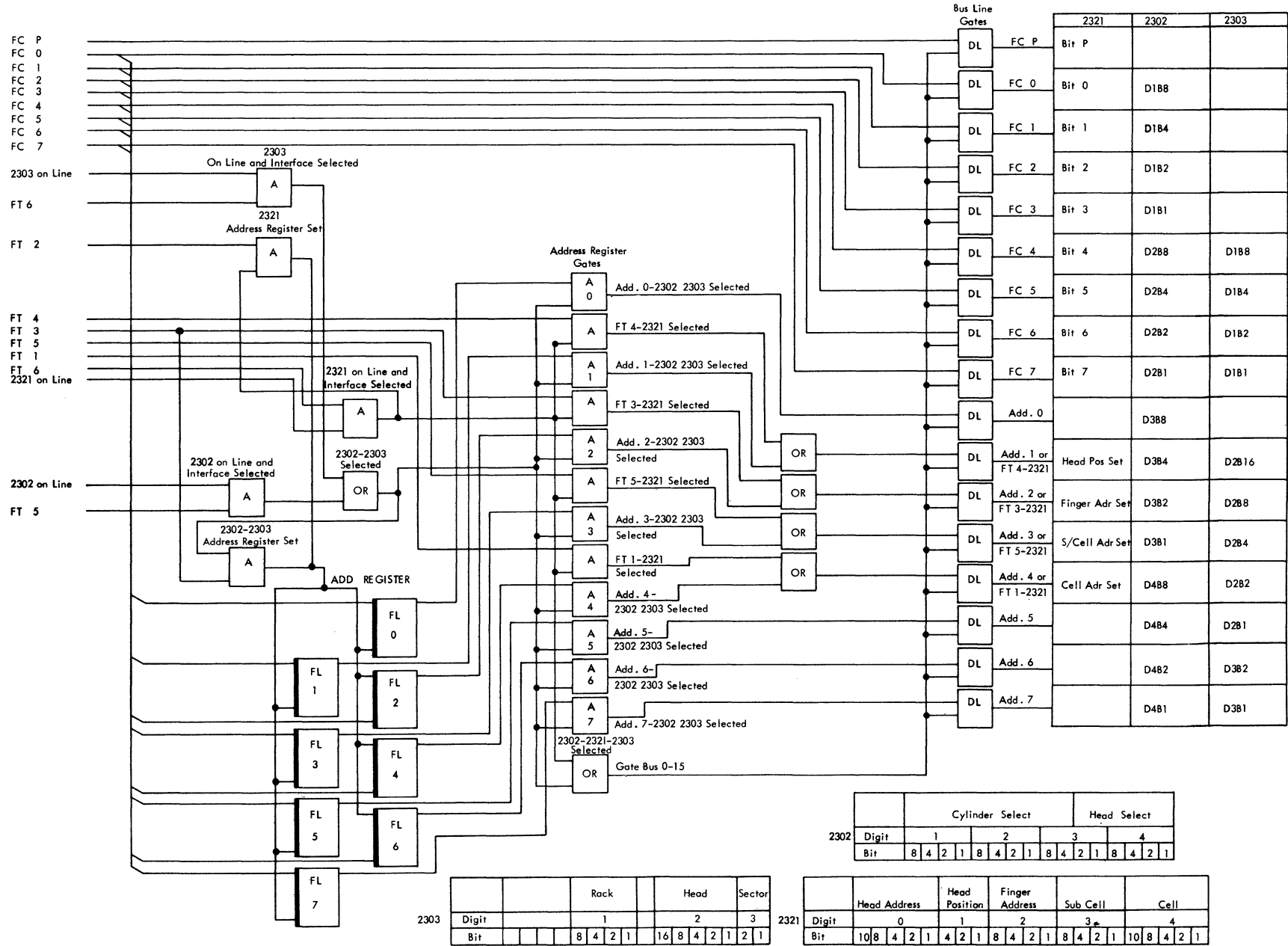
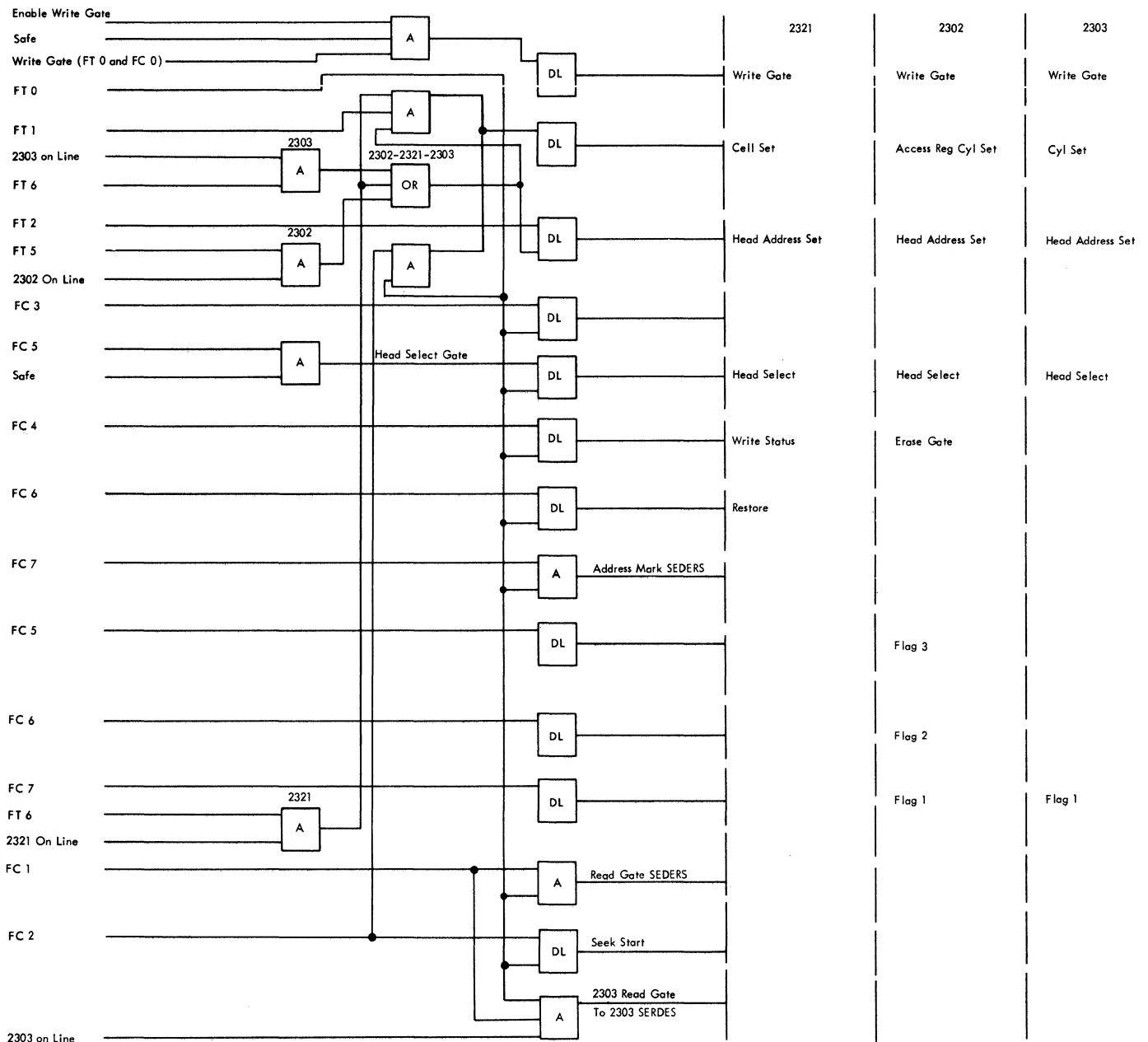


Figure 5-6. Address Register



23901-5

Figure 5-7. Device Control Gate

### 5.1.1.1 Device Attachment Limits

#### 5.1.1.1.1 Attachment Limits of Basic 2841

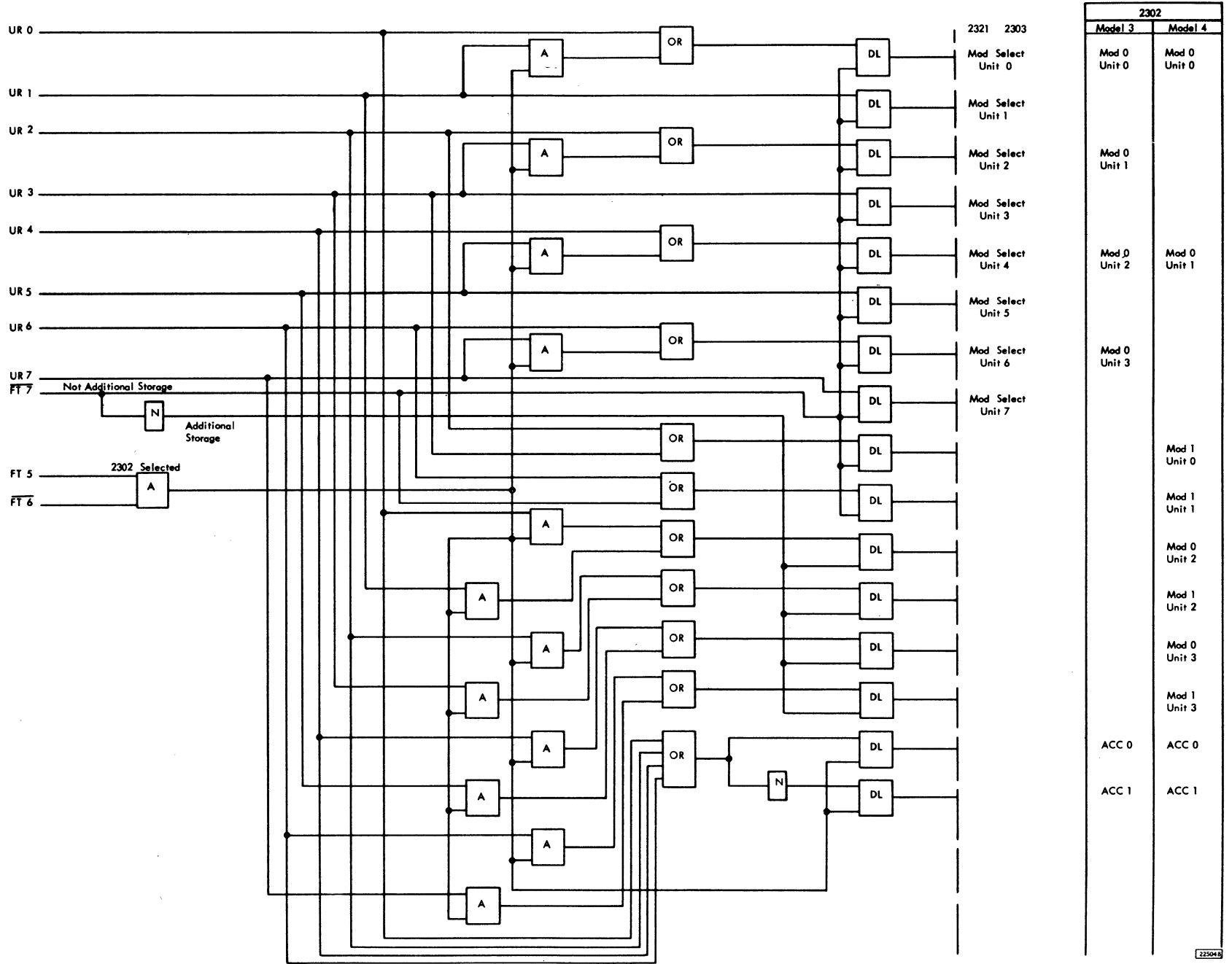
A maximum of eight 2311's may be attached.

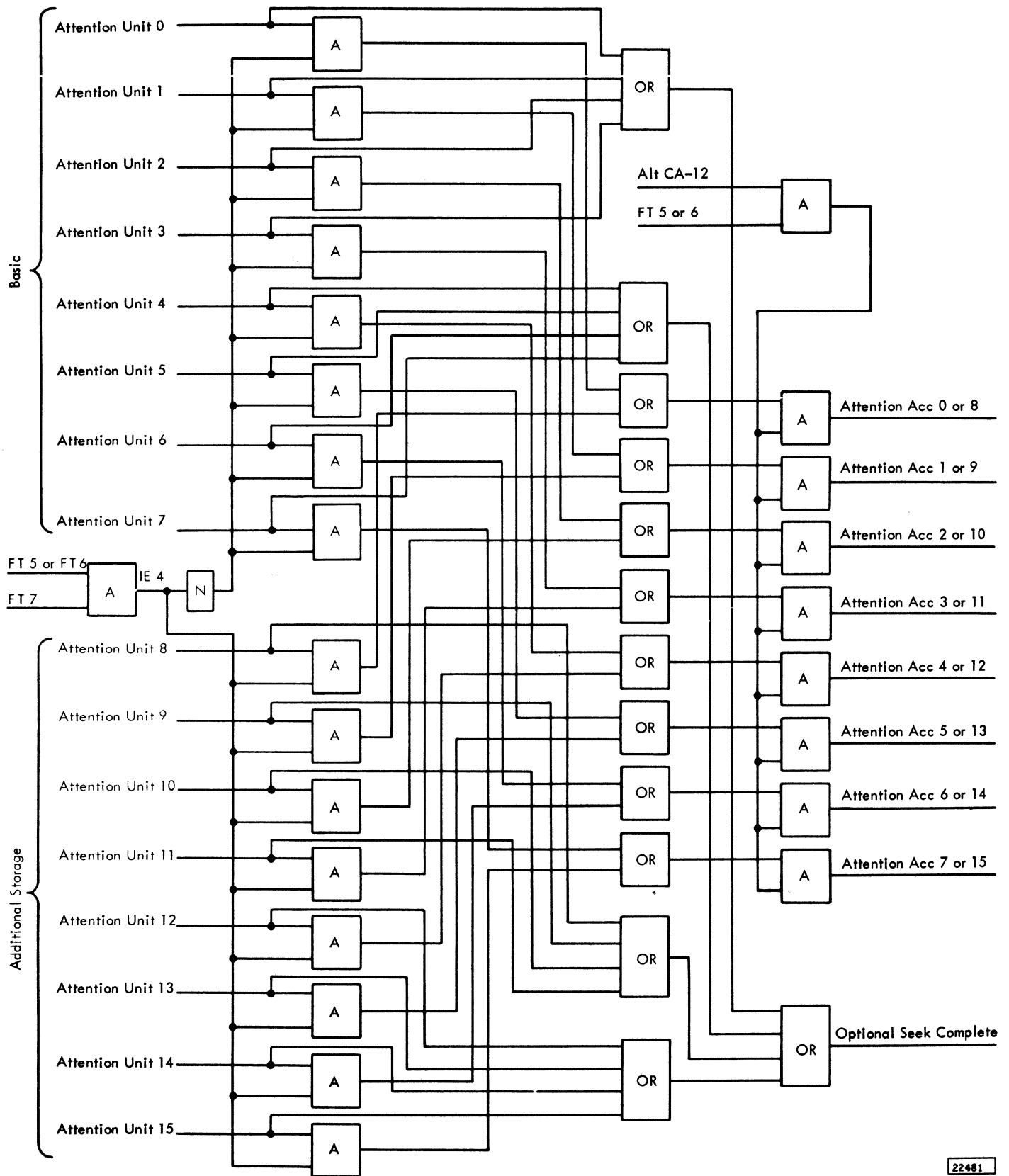
#### 5.1.1.2 Feature Device Attachment:

This feature permits the installation of 2302, 2303 or 2321 direct access storage devices. Any combination of devices that does not exceed eight accesses can be installed. For this count, the number of accesses per physical device is:



Figure 5-8. Module Select Gate

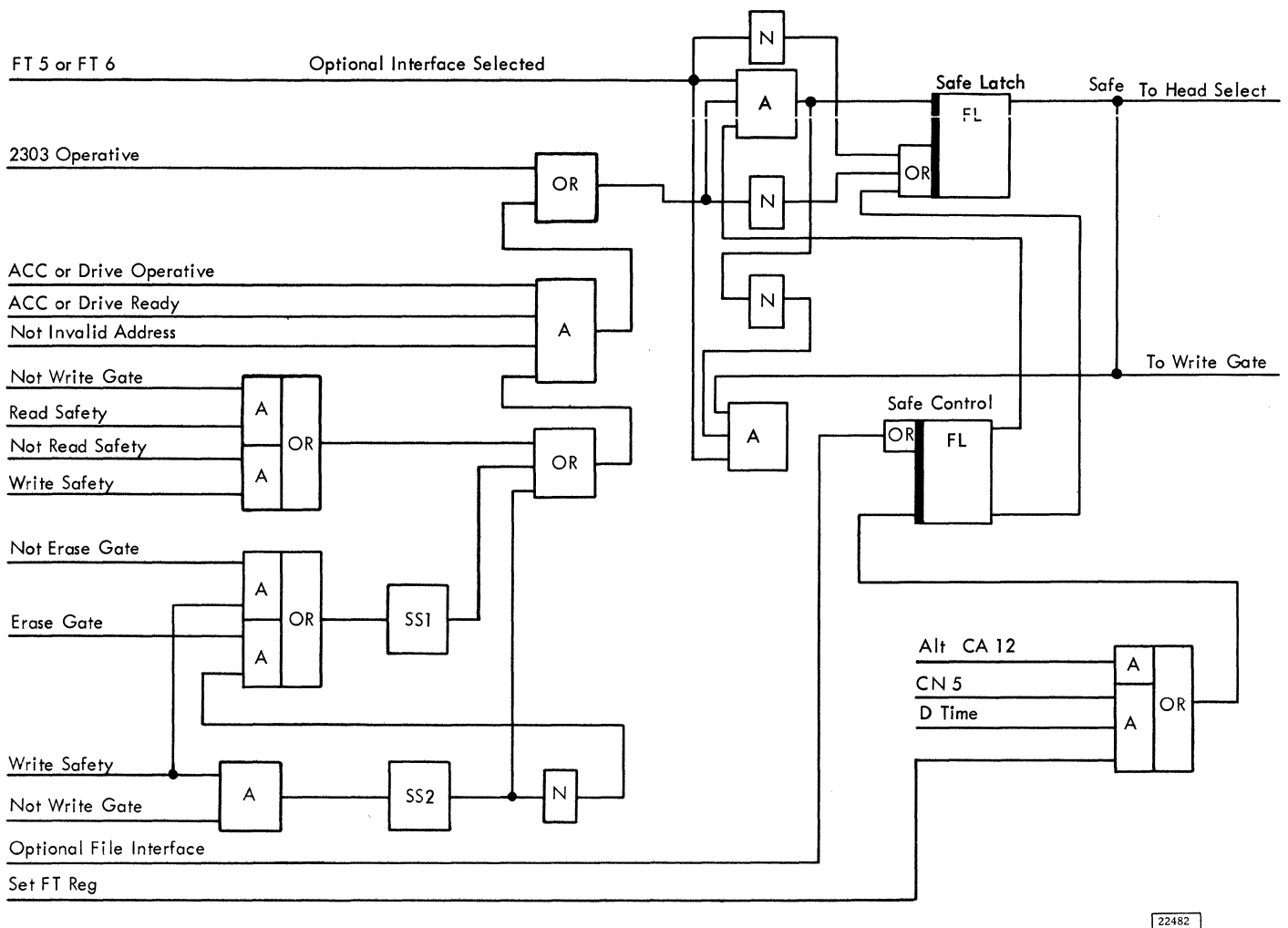




22481

Figure 5-9. Seek Complete Gate





22482

Figure 5-11. Fail Safe

The 2302 has the same bit rate and format as the 2311 and uses the same read and write circuits in SERDES. The HA gap is larger than the HA gap for the 2311 (Figure 5-15).

### 5.1.3 2321 Operation

- Provide selection, address transfer and head selection of 2321.

When the channel command calls for a 2321 operation, the microprogram determines that a feature device is called for and gives a 2 → FT statement to

select the feature attachment. FT bit 6 and 2321 on line determines that the 2321 is selected. (Figures 5-1, 5-3, 5-4, and 5-5.)

The 2321 operation is different than the operation of the 2311 and the 2302. The address transfer sequence and timing for the 2321 are shown in Figure 5-5.

The slower byte rate of the 2321 requires the use of a 875 kc-write-oscillator. The selection of a 2321 operation gates the 875 kc oscillator and de-gates the basic 2.5 mc oscillator.

The slower byte rate also requires a different VFO circuit. The operation of this VFO is the same as the basic VFO but at a slower timing rate. The

Function	2311	2321	2302	2303
Pack or Module Capacity	7.25 million 8 bit bytes	400 million 8 bit bytes	112.79 million 8 bit bytes Per Module	3.91 million 8 bit bytes
Tracks Per Module or Access	2,030	200,000	11,500	800
Tracks Per Head	203	5	250	1
Number of Heads	10	20	46	800
Track Capacity	3,660	2,031	5,046	4,892
Maximum Record	3,625	2,000	4,984	4,892
Rotation Period	25 ms	50 ms	33.83 ms	17.5 ms
Byte Rate	156.2 kc	51.1 kc	156.3 kc	303.8 kc
Access Time				
Maximum	135 ms	600 ms	180 ms	17.5 ms
Average	85 ms	---	162 ms	8.6 ms
Minimum	25 ms	95 ms	50 ms	0.0 ms

22035A

Figure 5-12. Differences in Specifications 2311, 2302, 2303, and 2321

block-bit-ring-advance single shot is timed for 4600 ns instead of 1600 ns (Figures 5-16 through 5-19).

The track format is changed for the 2321 by the addition of an address mark ahead of the HA field.

On the 2321 if a defect is found on the strip in the HA or Record 0 areas they may be moved approximately 800 bytes from index. This is done by

making the flag byte bits 1 and 6 one's and by doing a write-HA-CCW.

A restore command is added with the 2321. This command causes the 2321 to take the strip from the read station and return it to the cell (Figure 5-20).

The 2321 attachment circuits, flow charts of operations, and timing charts are shown in the 2841 Stage 2 FEMDM (pages 1221, 1613, 1712, 1737 and included on other diagrams).

Function	2311 Selected by FT 7 IE 7	2321 Selected by FT 6 IE 6	2302 Selected by FT 5 IE 5	2303 Selected by FT 6 IE 6 & 3
Seek Address	200 tracks in one binary coded byte, Head address sent later	Cell, subcell, strip, head position and head number, 200,000 tracks and 20 heads	Cylinder and head number, 250 tracks and 40 heads (46 heads if flag tracks used).	80 cylinders and 10 heads.
Address data transfer to interface	1 byte parallel	5 bytes serial.	2 bytes serial.	2 Bytes serial
Address data transfer to device.	1 byte parallel FT 1=set cylinder	5 BCD digits serial. FT 1 set cell. FT 2 set head number. FT 3 set finger. FT 4 set head position. FT 5 set sub cell.	4 BCD digits parallel. FT 1 set cylinder. FT 2 set head number. FT 4 set flag. FT 3 sets head address to OA register.	3 Digits parallel FT 1 set Seek Complete FT 3 sets head address to OA Register
Seek start	Separate command (FT 0 and FC 2)	Separate command (FT 0 and FC 2)	Seek operation starts when cylinder address transferred to device.	No motion required but selection starts with head address set FT 2 Seek Complete Signal turned on by FT 1.
Head address.	10 heads in portion of binary coded byte.	20 heads in 5 bits.	40 heads in 2 BCD digits, and 6 flag heads for a total of 46 tracks.	10 heads in one byte.
Head address transfer to device.	Separate transfer parallel (requiring separate reset operation). Set by FT 2.	Separate transfer parallel (reset not required). Set by FT 2.	May be separate or sent at seek address transfer time (reset not required). Set by FT 2.	Same as 2302 Set by FT 2.
Head advance (multiple track).	Incrementing head register steps ahead one when FT 4 and FT 0=1	Static register in device. Head address stored in interface register. Read out to A bus, incremented in ALU and read back to interface register. Set to device with FT 2	Static register may be incremented (or decremented) by setting new head address. Operation same as 2321	Same as 2302
Select head.	Must be latched into FC 5 but kept on throughout entire read/write operation.	Same as 2311. Set by (FT 0 and FC 5) if write safety (from device) is down.	Same as 2321. Set by (FT 0 and FC 5).	Same as 2321 Set by (FT 0 & FC 5).
Read gate.	Must be held up throughout entire read operation. Set by FT 0 and FC 1.	Not required by 2321. Developed in interface for serializer/deserializer. FT 0 and FC 1.	Same as 2321 erase gate control required. FT=0, FC 0 and FC 4.	Same as 2321
Write gate.	Must be held up throughout entire data transfer to 2311. 2311 requires erase gate control when write gate used. FT 0, FC 0 and FC 4.	Same as 2311 except erase gate not required, instead write status line to 2311 must be controlled when write gate is used. FT 0, FC 0 and FC 4.		Write gate must be held up throughout data transfer. Neither erase gate or write status required. FT 0 & FC 0.

22036.1

Figure 5-13a. Differences in Operations 2311, 2302, 2303, and 2321 (Sheet 1 of 4)

Function	2311	2321	2302	2303
Erase gate.	Must be held up through-out data transfer. Must be held 9 bytes after write gate falls. FT 0, FC 4 and FC 0).	Erase gate not used, however equivalent signal is write status. Write status must rise 5 $\mu$ s prior to write gate. FT 0, FC 4 and FC 0.	Same as 2311 except erase gate must be held up a minimum of 40 $\mu$ s (more than 7 bytes). FT 0, FC 4 and FC 0).	Erase gate not required (FT 0 & FC 0 provides write gate).
Return to 00	Used for initial program load. To position access to cylinder 000. FT 0 and FC 6.	Return to 00 not used, an equivalent signal restore used to replace strip in cell. FT 0 and FC 6.	No such function available in 2302-3 and 4. Can be achieved by seek operation to invalid address followed by seek to any address.	No such function.
Set difference	Used to indicate direct seek data. FT 3.	No such function. All seeks are direct seek.	Same as 2321.	Same as 2321.
Head reset.	Used to set head address to 00.	Equivalent function is set head address. FT 2.	Same as 2321.	Same as 2321.
Set control	Used to indicate that bits on data line represent control data. FT 0.	Used to gate data bus signals to proper cable connections on 2321 channel. FT 0.	Same as 2321.	Same as 2321.
Attention.	Signal from 2311 to 2841 that seek operation has been completed. gated to ALU by ALT CA 12. SC=Mod #.	Same as 2311. Signal is turned off by FT 0 and FC 1 on next module select operation to 2321 concerned. SC= Mod # gated by ALT CA= 12.	Same as 2311.	No motion required. However, Attention signal is response to set Seek Complete Operation at present, reset by mod select.
Old address.	Lines to 2841 which represent present cylinder position. gated to ALU by ALT CA 14	Used to read old head number from head address register in interface. Gated by ALT CA= 14.	Same as 2321.	Same as 2321.

22036.2

Figure 5-13b. Differences in Operations 2311, 2302, 2303, and 2321 (Sheet 2 of 4)

Function	2311	2321	2302	2303
STATUS SIGNALS	As explained individually below. Gated by ALT CA 13.	Same as 2311. gated by ALT CA=13.	Same as 2321.	Same as 2321.
Ready	Indicates selected device is safe and ready to perform. FS 0 and ALT CA 13.	Exact signal not available. Equivalent is drive ready indicating that a strip has been picked and is ready or that the interlocks are satisfied and a seek operation may be started. FS 0 and ALT CA 13.	Exact signal not available. Equivalent is access ready indicating that access has arrived and seek operation may start FS 0 and ALT CA 13.	Signal not avail. Equivalent is 2303 On Line indicated by IS 2 & ALTCA 13 or by IE 3 & 6.
On line	When up indicates selected 2311 is operable but not necessarily ready. Gated by ALT CA 13 and FS 1	When up indicates that the module number addressed was a 2321. Separate on line signals provided for 2321 and 2302 and are sent to IE as bits 3, 5 and 6. If interface is selected and no module select operation has been done or the module selected does not exist, all three bits (3, 5 and 6) are on. When a module is selected only the bit for that type is left on. This permits the program to test for wrong type or missing device (misplugged cable) or selection failure. If 2321 is selected IE=Bit 6.	See 2321 except if 2302 selected IE=Bit 5.	See 2321 except if 2303 selected IE-Bits 3 & 6.
Unsafe	Signal from 2311 that indicates selected 2311 is unsafe and will not perform any operation. Gated by ALT CA 13 and FS 2	Signal is generated in interface and indicates that drive ready, or drive operative, or read/write safety failure has occurred. When unsafe condition occurs, drop write gate deselect head and drop write status, for maximum protection to data; however, the not safe condition is latched on for testing purposes until FT register is set. 2321 unsafe is indicated by IS 2=0. Gated by ALT CA 15. File safe indicated by IS 2=1  Note: FC is not reset by unsafe if CE switch is in local and 2321 is on CE track.	See 2321. Except signals tested (monitored) in interface are access ready, access operative, read safety, and write safety.	Exact Signal not Available-- only signal returned by 2303 is 2303 On Line. This signal is interpreted as file safe. 2303 unsafe indicated by IS 2=0

22036.3

Figure 5-13c. Differences in Operations 2311, 2302, 2303, and 2321 (Sheet 3 of 4)



Function	2311	2321	2302	2303
Seek incomplete	Indicates that seek complete did not occur within 600 ms after seek command was given. FS 7 gated by ALT CA 13.	Signal not available. Equivalent signals are drive inoperative (indication of motion control malfunction) or invalid address in file register or a physical misposition of the drive). Drive inoperative FS 1=0. Invalid address FS 5=0. Gated by ALT CA 13.	Signal not available. Equivalent signals are access inoperative (indication of motion circuit failure) or CE cylinder located (access located on non-data surface). Access inoperative FS 1=0, CE cylinder located FS 7=1. Gated by ALT CA 13.	No such signal exists. Equivalent condition is failure to get seek complete signal from 2303. Seek complete Failure indication SC=Not Mod # Addressed. Gated by ALT CA 12.
End of cylinder	Indicates selected 2311 has head address of 10 or 11 (invalid). FS 5 gated by ALT CA 13.	Signal does not exist. Information available from count field on data track or in OA register in interface.	Same as 2321.	Same as 2321.
Any file attention	This is an OR of the attention signals. IS 7 gated by ALT CA 15.	Same as 2311. IS 6 gated by ALT CA 15.	Same as 2311 except IS 6 gated by ALT CA 15.	Same as 2311 except IS 6 Gated by ALT CA 15

22036.4

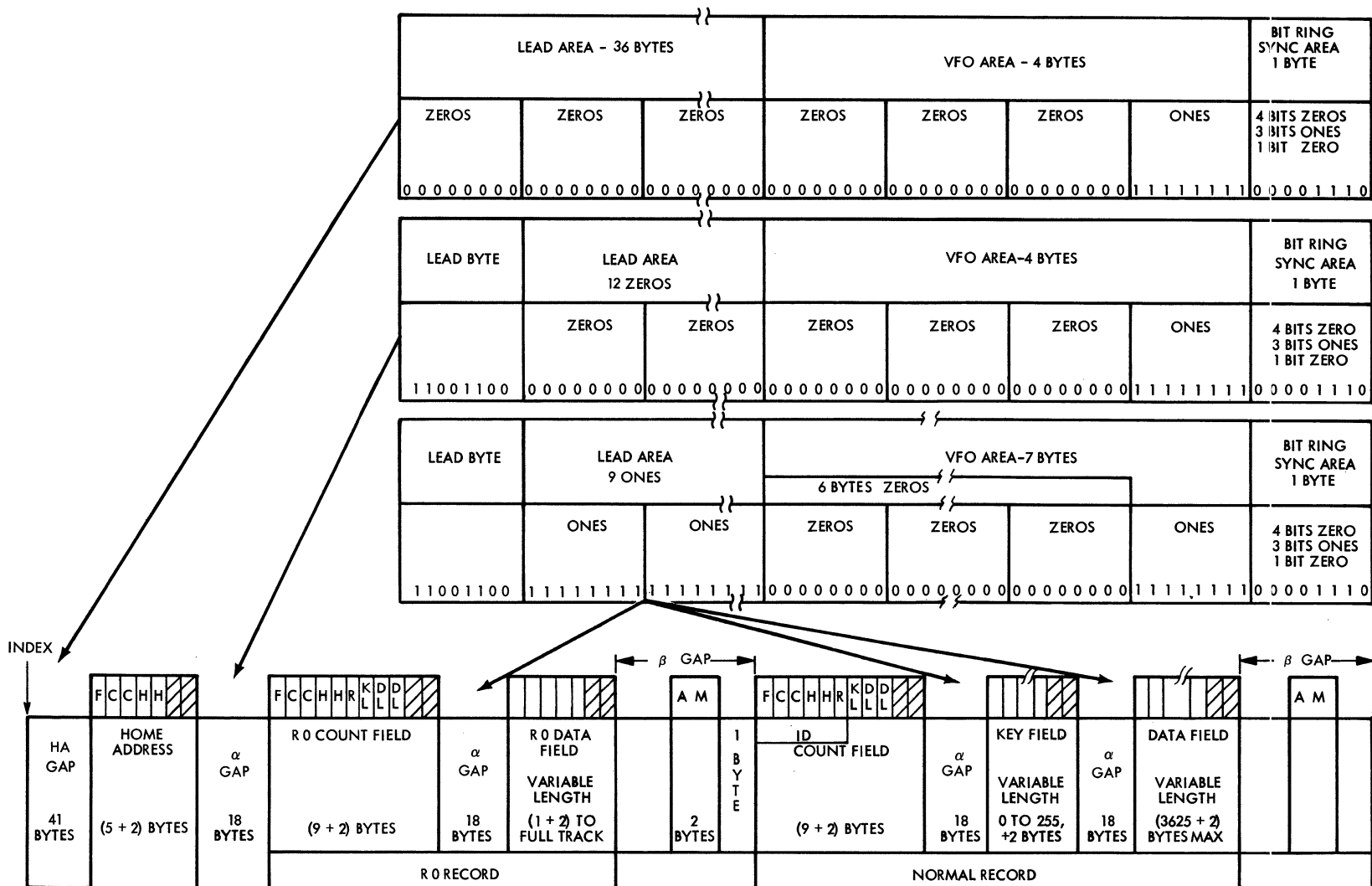
Figure 5-13d. Differences in Operations 2311, 2302, 2303, and 2321 (Sheet 4 of 4)

Function	2311	2321	2302	2303
Strip ready (2321)	Exact signal does not exist. Equivalent signal is on line. FS 4 gated by ALT CA 13.	Indicates that the clutch has been picked and has passed early index. FS 4=1 gated by ALT CA 13.	Exact signal does not exist. Equivalent signal is on line. FS 4 gated by ALT CA 13.	Exact signal does not exist. Equivalent signal is On Line FS 4. Gated by ALT CA 12.
Drive operative (2321)	Exact signal does not exist. Equivalent signal is ready. FS 0 gated by ALT CA 13	Indicates that drive is functionally capable and a proper drive was selected and not in CE mode. FS 1=1 gated by ALT CA 13.	Exact signal does not exist. Equivalent signal is access operative. FS 1=1 gated by ALT CA 13.	Exact signal does not exist. Equivalent signals are: 1) 2303 On Line IE 3 & 6. 2) File Safe IS 2. 3) Attention SC=Mod #. 4) Any Seek complete. IS 6=1.
Auto restore (2321)	Signal does not exist.	Indicates that strip is being (or has been) returned to cell because drive has not been addressed for 800 ms. FS 6=1 gated by ALT CA 13.	Exact condition does not exist. Equivalent condition is rezero, indicated by CE cylinder located. FS 7=1.	Signal does not exist.
Invalid address (2321)	Equivalent conditions are: 1) End of cylinder FS=5. 2) Seek incomplete, FS 7 gated by ALT CA=13.	Indicates that address in register is invalid or that drive is physically mispositioned. FS 6 gated by ALT CA=13.	Exact signal does not exist. Equivalent signal is CE cylinder located. FS 6 gated by ALT CA=13.	Condition does not exist.
CE cell located (2321) CE cylinder located (2302)	Signal not available.	Indicates CE cell located at access station.	Indicates that access located at non data surface.	Signal does not exist.

22037

Figure 5-14. Functions not in the 2311

Figure 5-15. HA or Alpha Gap Bit Configuration - 2302



22024A



Figure 5-17. HA or Alpha Gap Timing Diagram - 2321

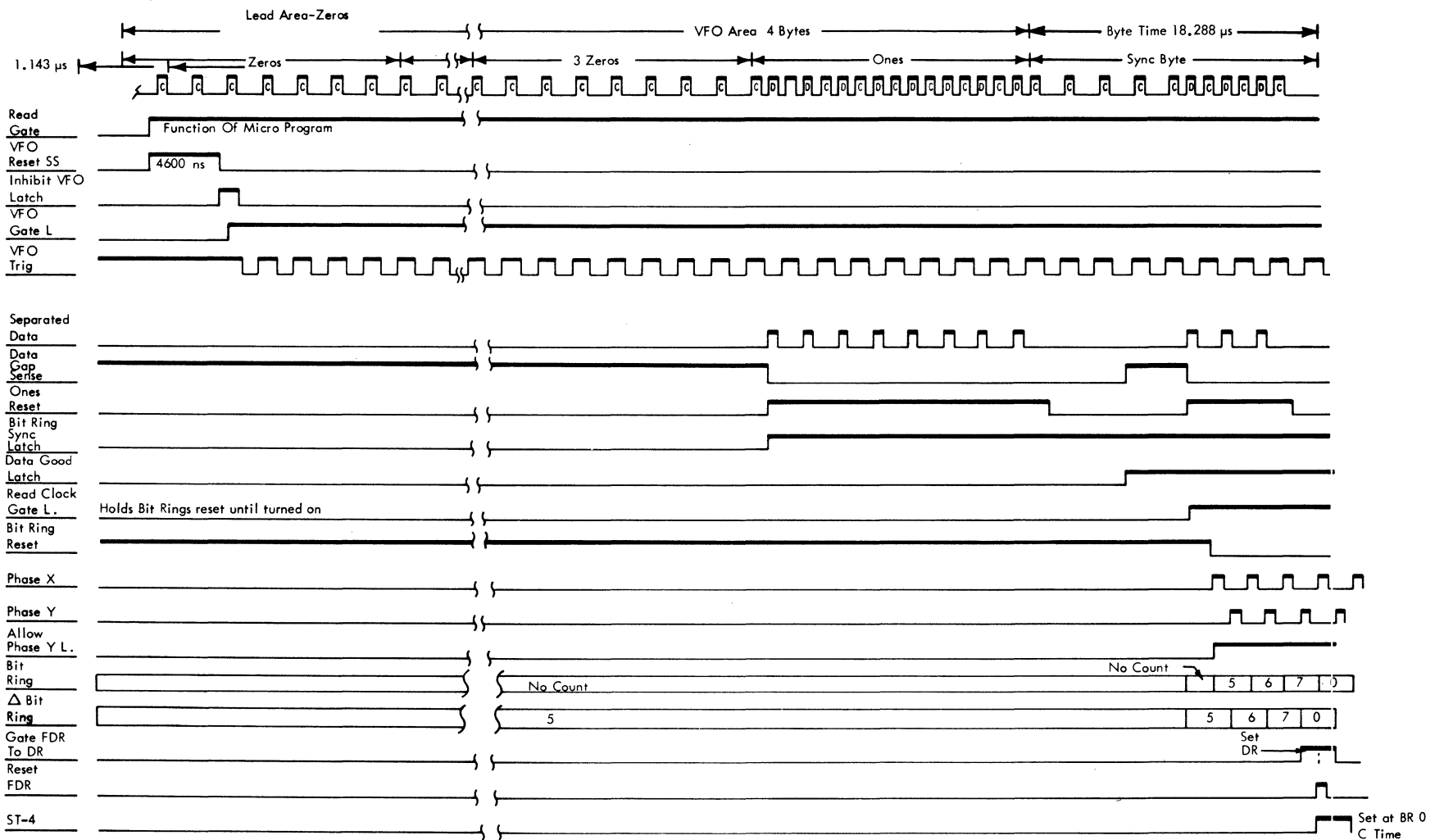
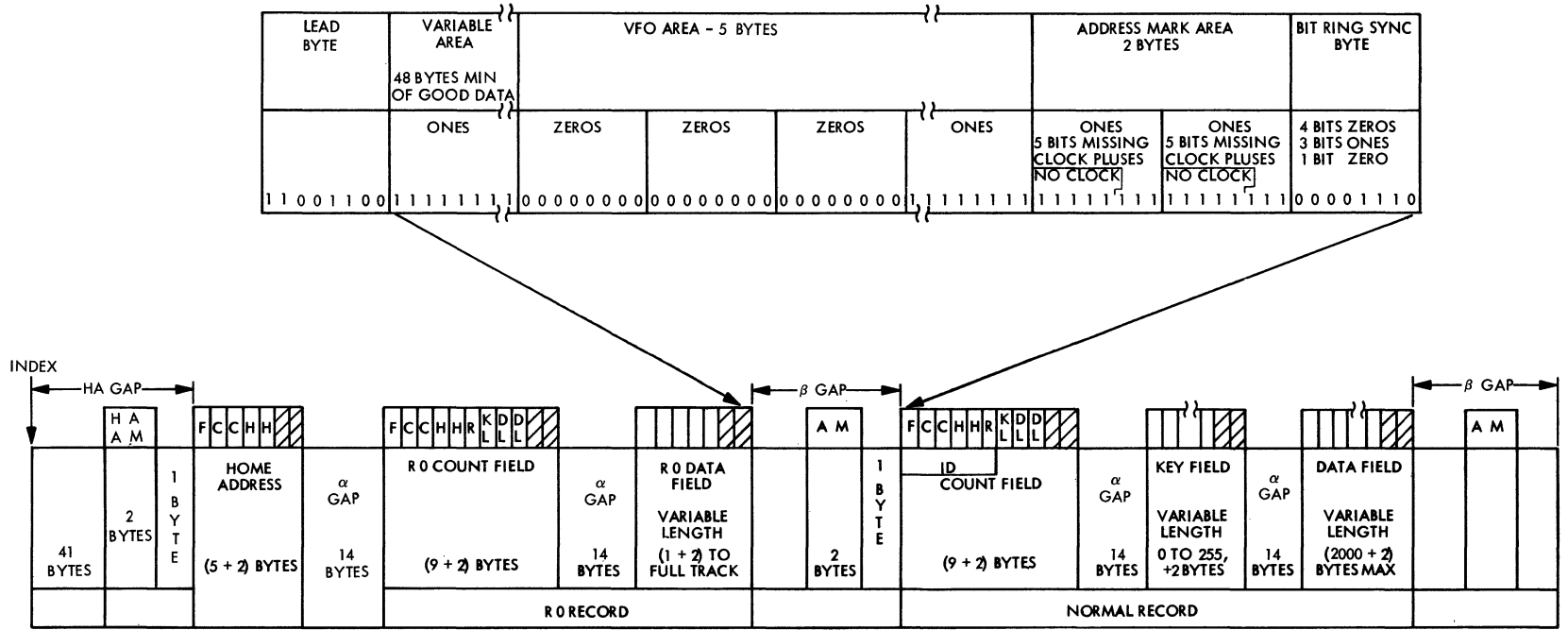
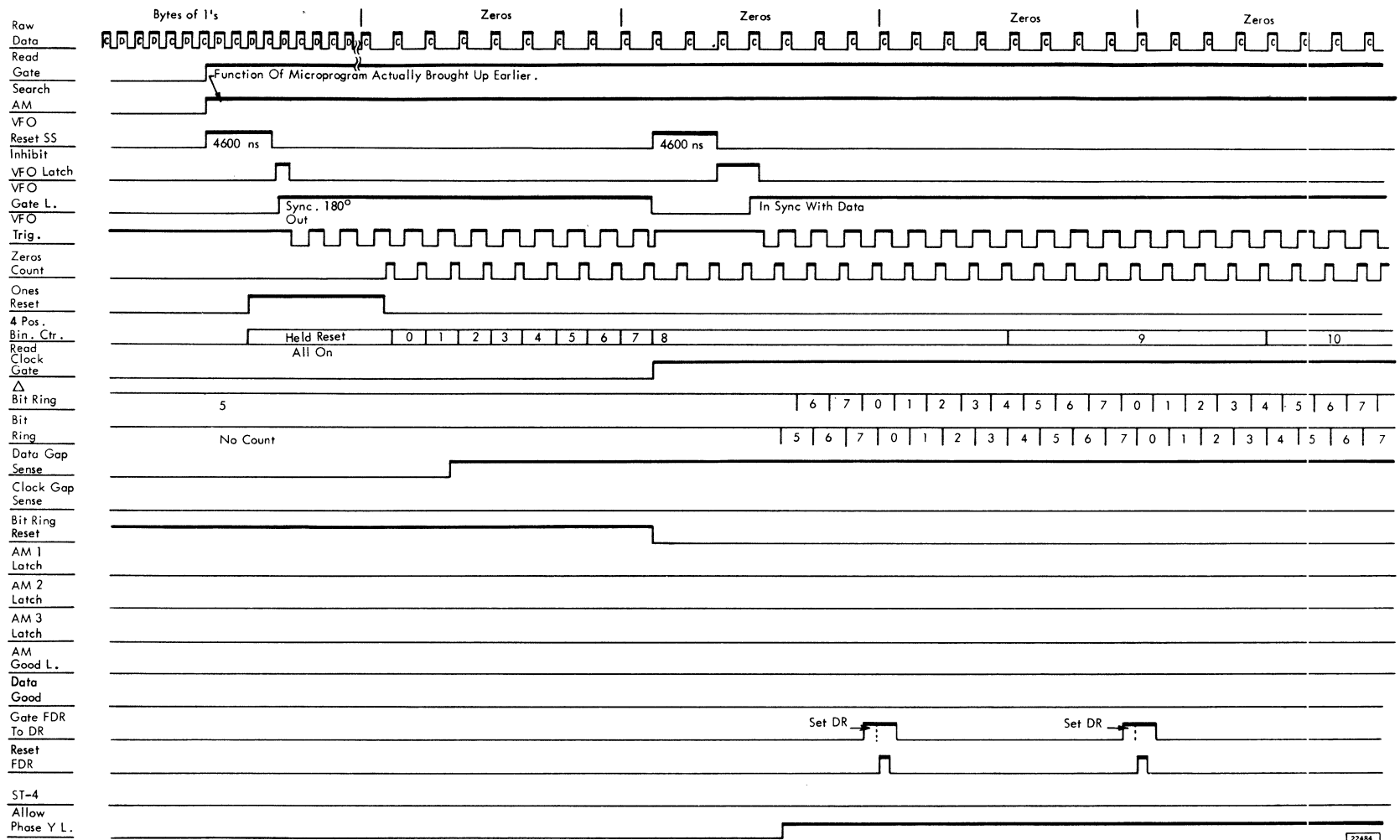


Figure 5-18. Beta Gap Bit Configuration - 2321





22484

Figure 5-19a. Beta Gap Timing Diagram - 2321 (Sheet 1 of 2)

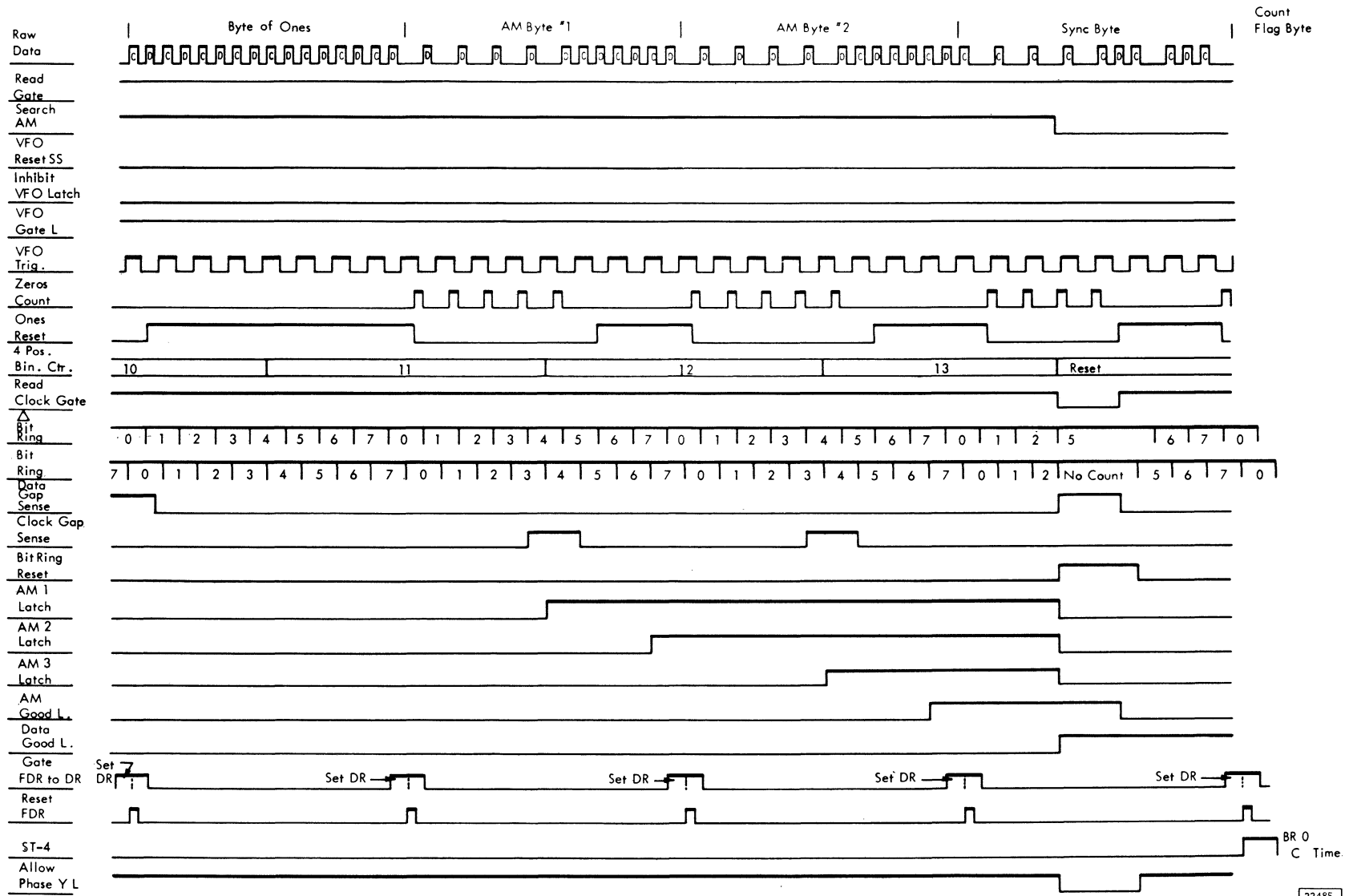


Figure 5-19b. Beta Gap Timing Diagram - 2321 (Sheet 2 of 2)

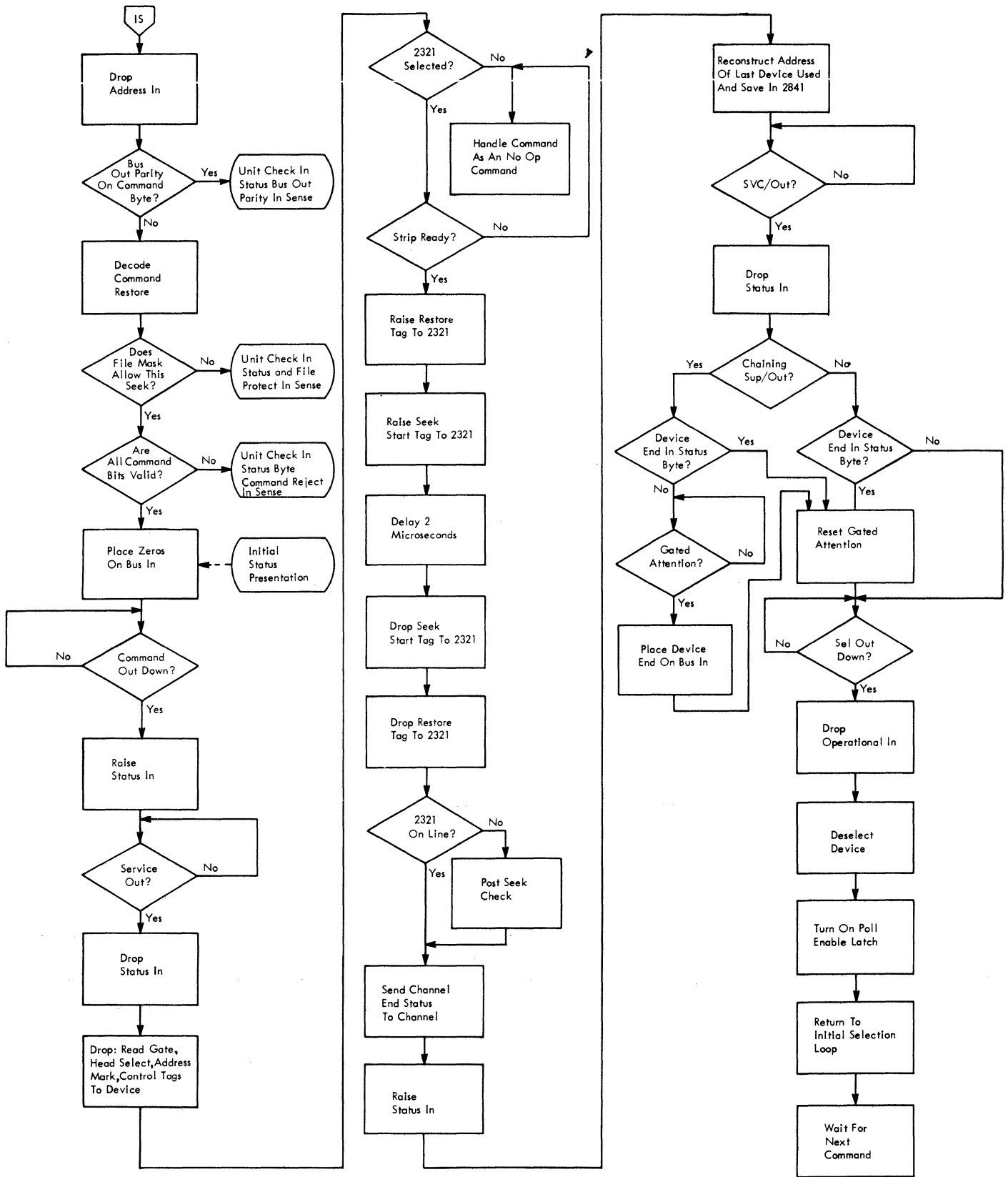


Figure 5-20. Restore Command - 2321



### 5.1.4 2303 Operation

- Provide selection, address transfer and head selection of the 2303.

When the channel command calls for a 2303 operation, the microprogram determines that a feature device is called for and gives a 2 → FT statement to select the feature attachment. FT bit 6 and 2303 on line determines that the 2303 is selected (Figures 5-1, 5-2, 5-4, and 5-5).

The 2303 drum storage has a capacity of 3.91 million bytes, contained in 800 tracks of 4,892 bytes of data. The byte rate is 3.29 μs per byte which is much higher than the 2311 byte rate.

Because of the higher byte rate and the differences in gap size and bit configuration, (Figures 5-21 and 5-22) many parts of the basic microprogram cannot be used for 2303 operations.

Figure 5-23 shows the areas of the program that are branched into for 2303 operations. These routines operate in much the same manner as the basic routines, but they handle only 2303 operations, so they can operate at a high byte rate.

The 2303 microprogram tapes are located in modules 0, 1, and 2 of the C gate of TROS. The hex addresses of these modules are: 8XX, 9XX, and AXX. TROS address bit 11 causes the modules on gate C to be addressed.

System programming for the 2303 is much the same as for the 2311. A list of differences follows:

1. **Multiple track operation:** Allows for multiple track operation on all 800 tracks. A full seek or cylinder seek command must precede a multiple track command in a chain of commands.
2. **Defective track flagging:** There is no need for defective track flagging as the 2303 has extra

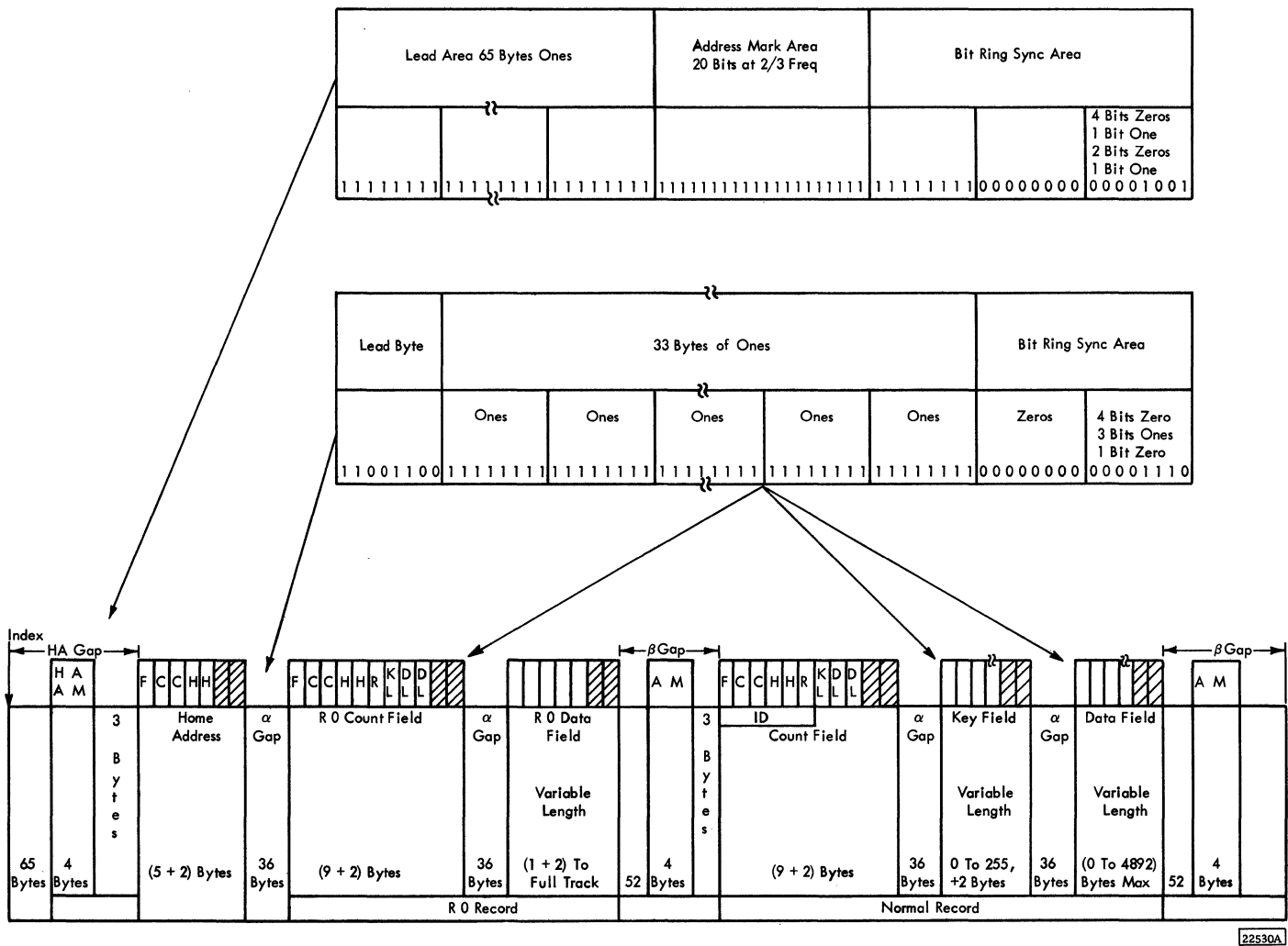
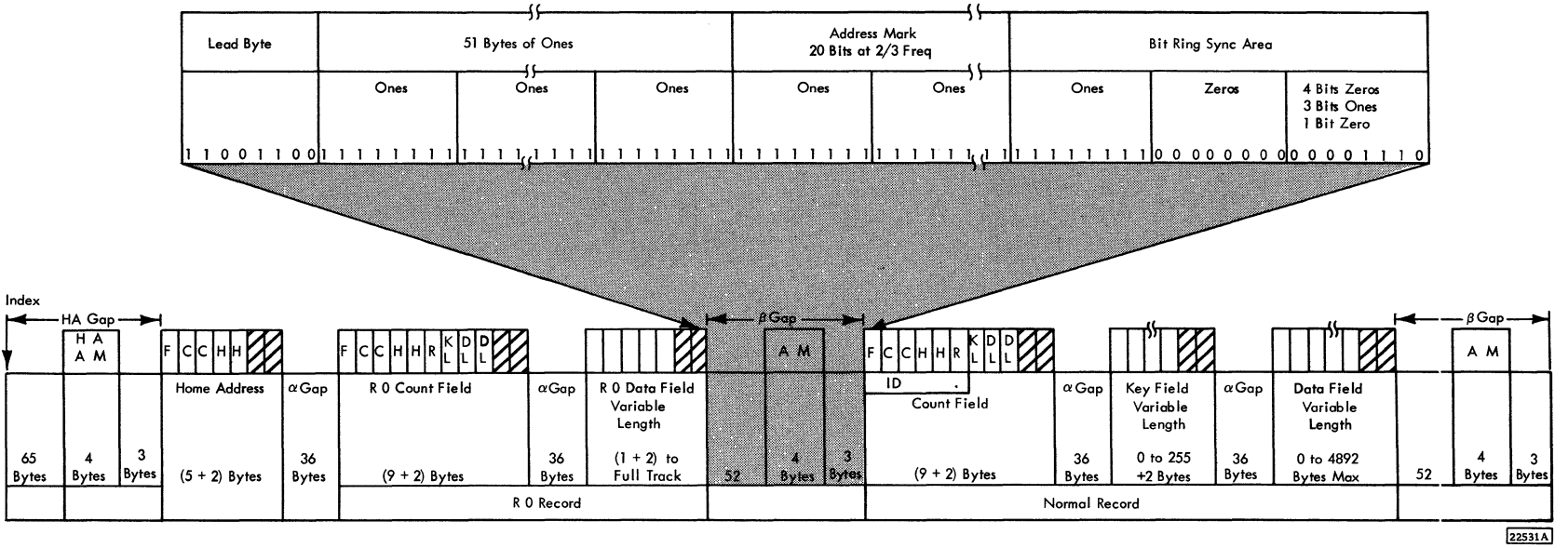


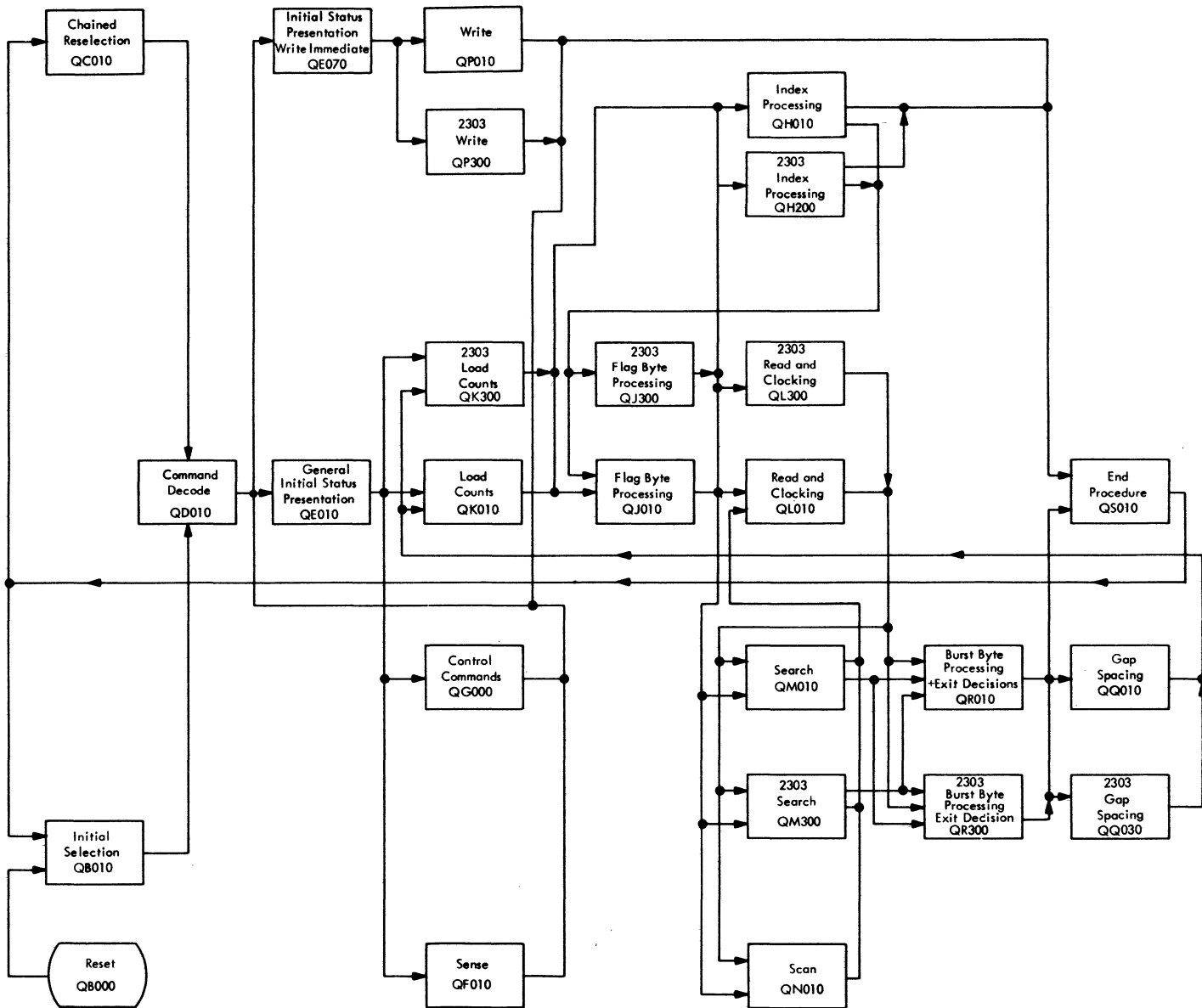
Figure 5-21. HA or Alpha Gap Bit Configuration - 2303

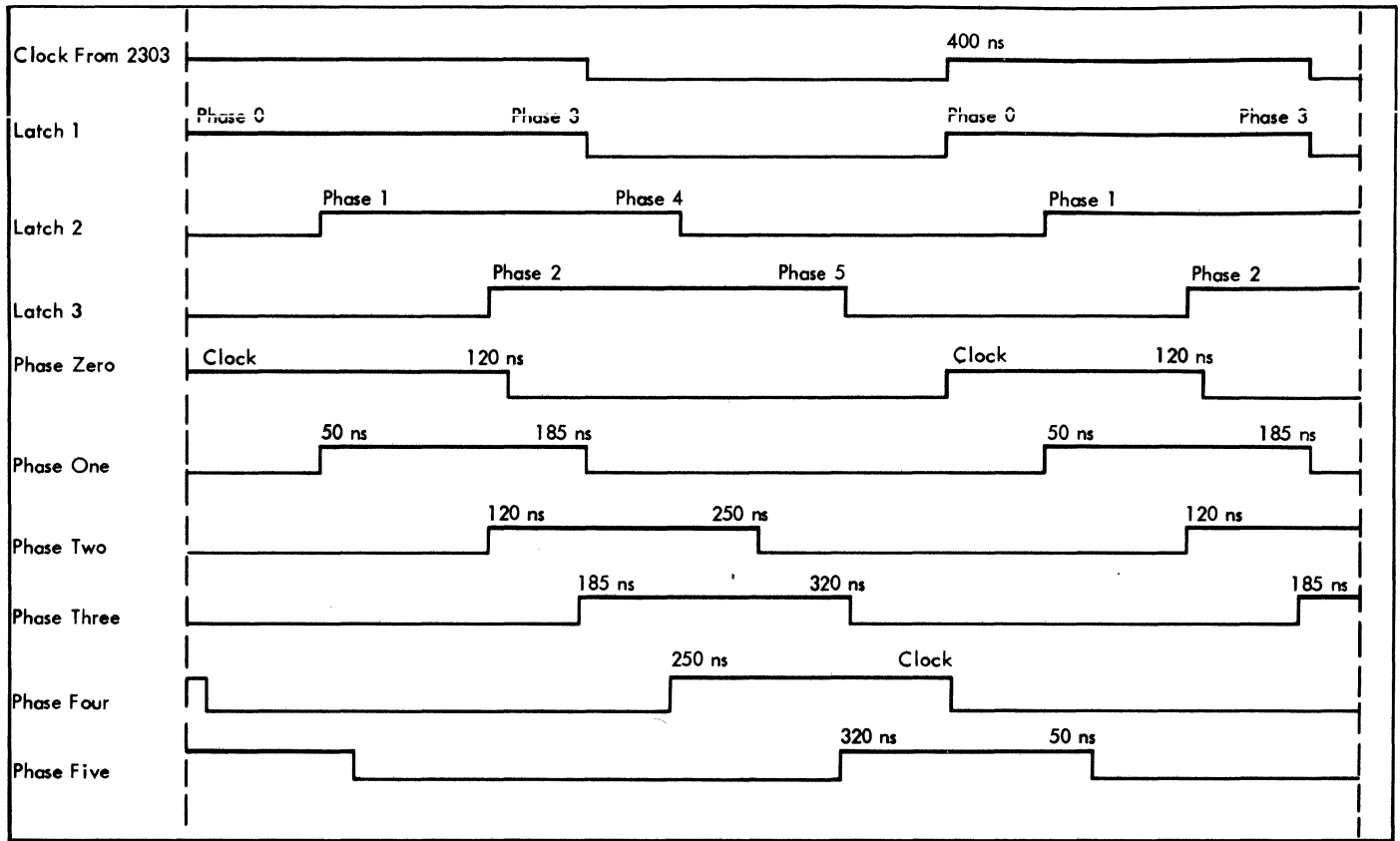
Figure 5-22. Beta Gap Bit Configuration - 2303



22531A

Figure 5-23. Condensed Micro Program Logic - 2303





22533

Figure 5-24. 2303 Clock Phase Timing

heads to rewire to replace defective track surfaces.

3. File scan feature: The file scan command is rejected if the 2303 is selected.
4. Restore command: This command is treated as a no operation if the 2303 is selected.
5. Recalibrate command: This command is treated as a no operation command if the 2303 is selected.

### 2303 Serializer/Deserializer

When the 2303 is selected for a read or write operation, the basic serializer/deserializer (S/D) is blocked by the 2303-selected line. The 2303-selected line controls:

1. Selected-read-data (blocked).
2. Bit-ring-reset (held active).

The 2303 on-line signal blocks the writing of clock pulses.

The 2303 S/D is needed because the 2303 uses a clock track, because the 2303 records only data pulses on the data tracks, and because of the high data rate of the 2303 must use circuit cards faster than the normal S/D.

Serializer/Deserializer Write Operation: These are the objectives of a 2303 write-home-address operation:

1. Select the 2303 interface.
2. Select the 2303.
3. Select the 2303 head.
4. Set up to write 65 bytes of ones in the gap.
5. Wait for the index pulse.
6. Bring up the write-gate line to activate the serializer/deserializer (SD).
7. Write 65 bytes of ones.
8. Bring up address-mark line to activate the 2/3-frequency oscillator.
9. Write 20 bits at 2/3 frequency (address mark).
10. Drop address-mark line.

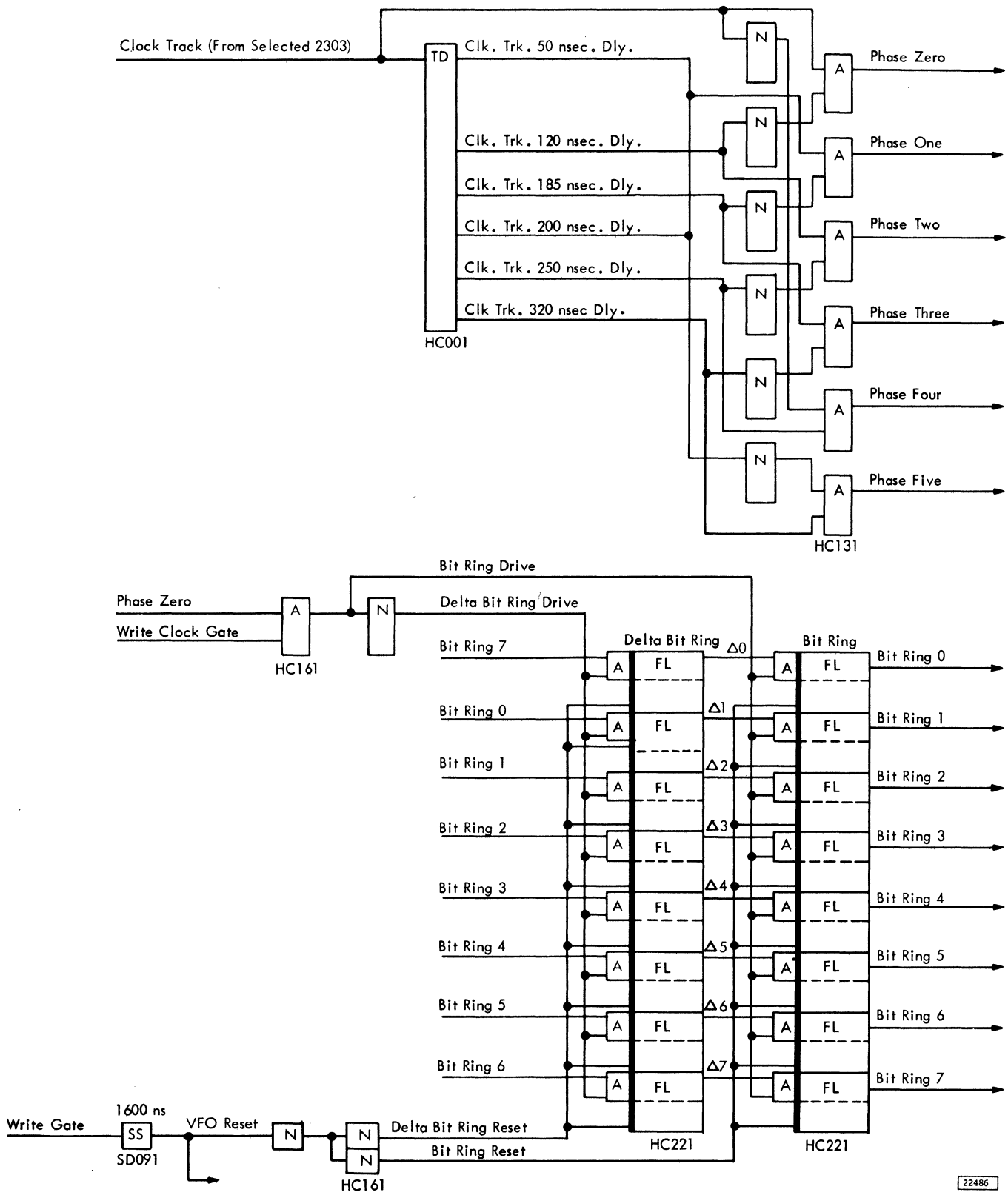
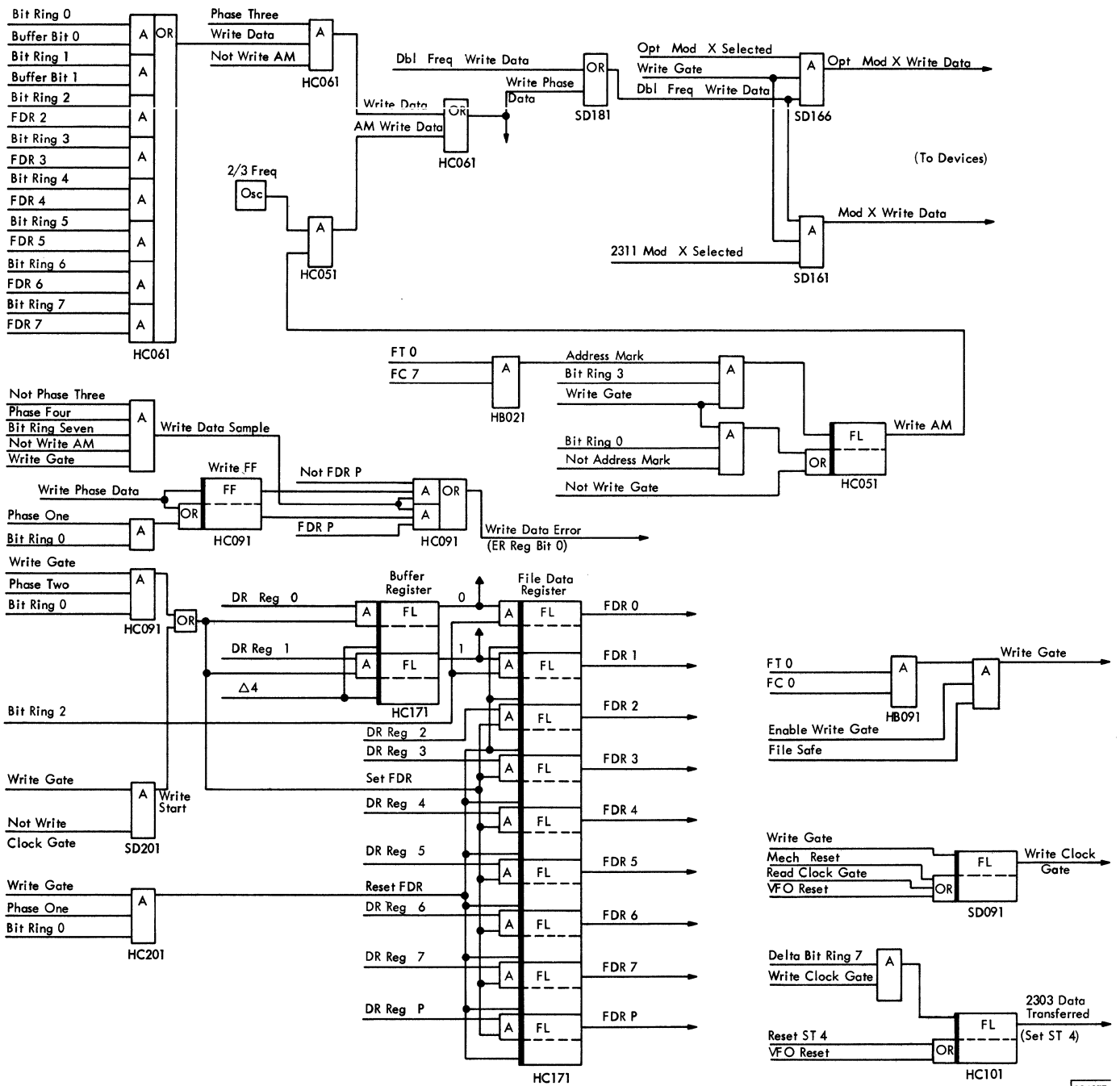


Figure 5-25a. 2303 S/D - Write Data Flow



22487B

Figure 5-25b. 2303 S/D - Write Data Flow

11. Write one byte of normal frequency ones.
12. Write one byte of zeros.
13. Write one sync byte (hex 14).
14. Transfer to S/D and write data (home address).

Before a write operation can take place, the 2303 must be selected and the proper head selected with a seek command. When the 2303 is selected, clock-track pulses from the 2303 are sent to the 2841 (Figure 5-25). The clock-track pulses are fed to a time delay circuit and ANDed together to develop phase zero through phase five pulses that are used for timing the write operation (Figure 5-26).

Assuming a write-home-address operation, the microprogram brings up write-gate after index and sets the DR register to hex FF to write the index gap of 65 bytes of hex FF (Figures 5-25 and 5-26).

Write-gate coming up starts the 1600 ns single shot timing to give VFO-reset which resets the delta-bit-ring (1 on, all others off) and the bit-ring (all off) and holds the write-clock-gate FL off to allow the clock-track pulses to recover from the noise pulses found at index. Write-gate and not-write-clock-gate gives the write-start pulse to transfer the DR register contents (hex FF) to the file-data register (FDR) and the two position buffer register.

When the VFO-reset single shot has timed out, the write-clock-gate FL turns on and at the next phase zero time starts the delta-bit-ring and bit-ring running.

At bit-ring 2 time, the buffer register bits are transferred into the 0 and 1 positions of the FDR. Because the FDR contains all one bits at bit-ring 2, phase-three time, the write-data line to the selected 2303 is brought up for the first time and is brought up at each phase three thereafter.

Each write-phase-data pulse changes the state of the write FF. At bit-ring seven time of each byte, the output of the write FF is checked with the output of the FDR parity bit to see that the proper number of data bits were written. If a write-data-error is detected, the ER register bit one is turned on.

At delta-bit-ring 7 time, the 2303-data-transferred FL is turned on to signal the microprogram, by turning on ST register bit 4, that the 2303 S/D is ready for a new byte.

At bit-ring 0, phase-one time the write FF and the FDR FL's are reset. At bit-ring 0, phase-two time the new byte is transferred from DR to FDR.

This sequence is repeated for 65 bytes of hex FF.

The microprogram then brings up the address-mark line which turns on the write-address-mark FL. The write-address-mark FL gates the 2/3-frequency oscillator, blocks the write-data line, and brings up the address-mark-write-data line to send

2/3-frequency-data pulses to the selected 2303. While the 2/3 frequency pulses are going to the 2303 the bit-rings, the FDR, and the 2303-transferred FL are operating at normal clock track frequency. The microprogram drops the address mark line after four byte times have passed and places a byte of hex 00 in DR.

Because of timing, one more byte of hex FF is written then the byte of hex 00. The microprogram sets up the sync byte (hex 14) in DR and starts to transfer the home address data (F, C, C, H, H) from the channel.

Serializer/Deserializer Read Operation: These are the objectives of a 2303 read-home-address operation.

1. Select the 2303 interface.
2. Select the 2303.
3. Select the 2303 head.
4. Wait for the index pulse.
5. Bring up the read-gate and address-mark lines to activate the serializer/deserializer (SD).
6. Search for the address mark.
7. Read the byte of zeros.
8. Synchronize bit-rings to the data from the 2303.
9. Read the sync byte serial data and set the data in the file-data register.
10. Transfer the sync byte in parallel to the DR register.
11. Repeat items 9 and 10 for each byte of home address data.

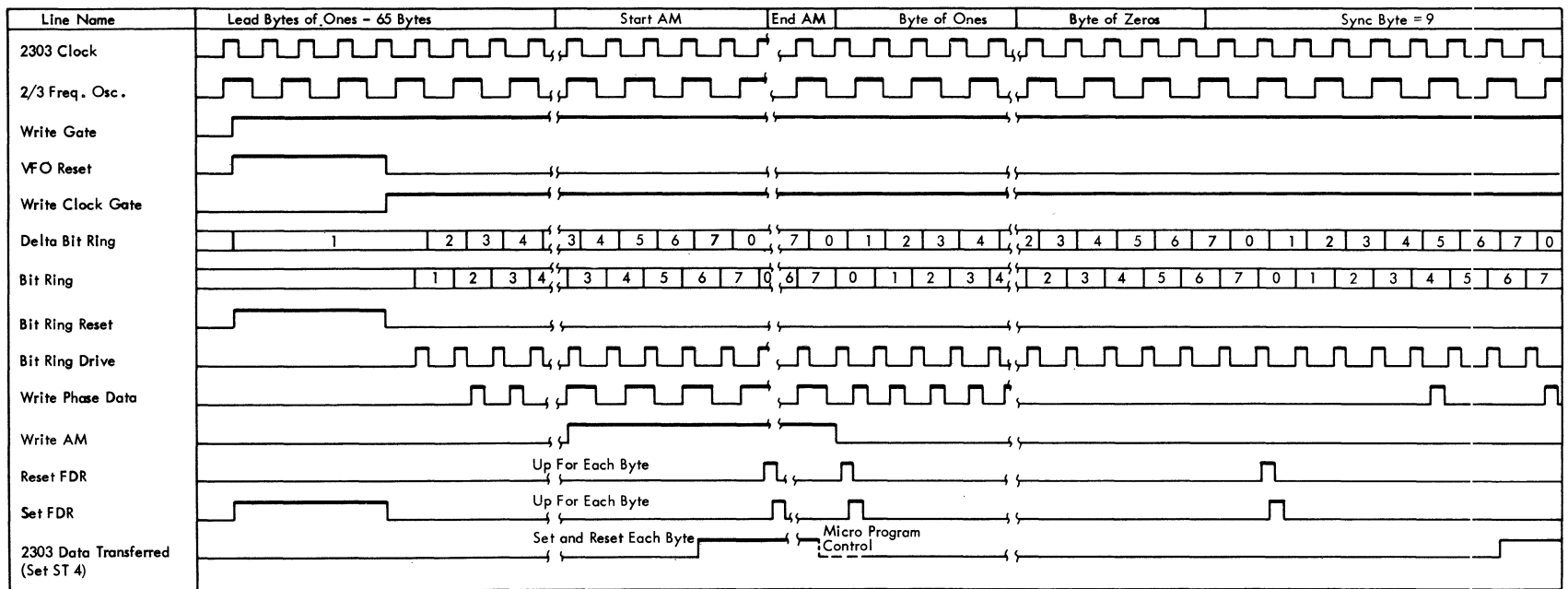
Before a read operation can take place, the 2303 must be selected and the proper head selected with a seek command. When the 2303 is selected, clock-track pulses are fed to a time delay circuit and ANDed together to develop phase-zero through phase-five pulses that are used for timing the read operation (Figure 5-24).

Assuming a read-home-address operation, the microprogram brings up the read-gate and the address-mark lines after a time out period after index has passed (Figures 5-27 and 5-29).

The read-gate line coming up brings up the VFO reset line to turn off all the bit-ring FL's and turn off all the delta-bit-ring FL's but the delta-bit-ring one FL which is turned on. The read-gate line coming up starts the select-phase latch, hold-phase FL sequence but because the address-mark line comes up the select-phase and hold-phase FL's are turned off. The address-mark line turns on the search-address mark FL.

When the bit-ring reset line drops, the delta-bit-ring and bit-ring start running.

With the search-address-mark FL on the address-mark-detection FL's (500-720, leading-



22535

Figure 5-26. 2303 S/D - Write Timing



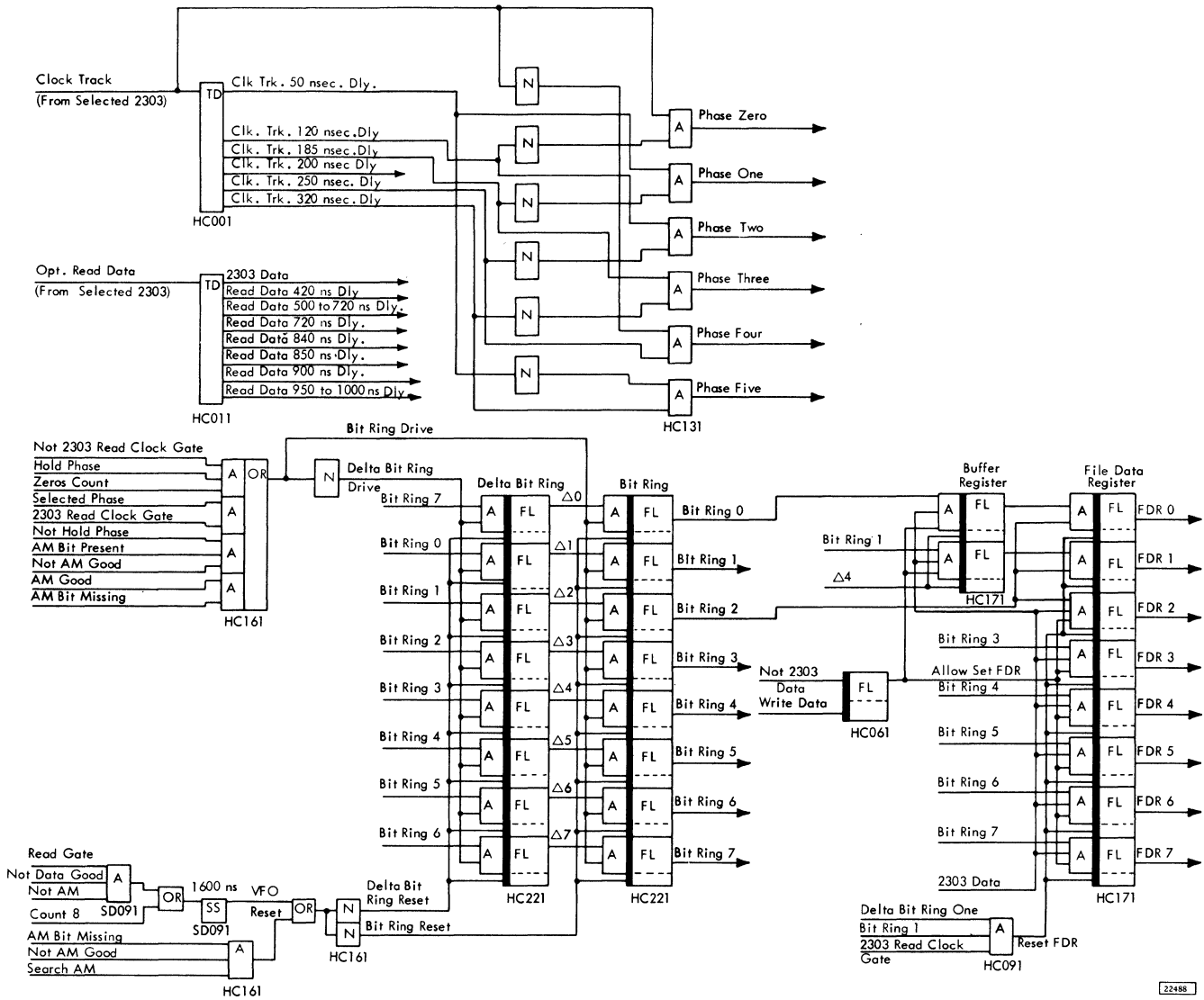
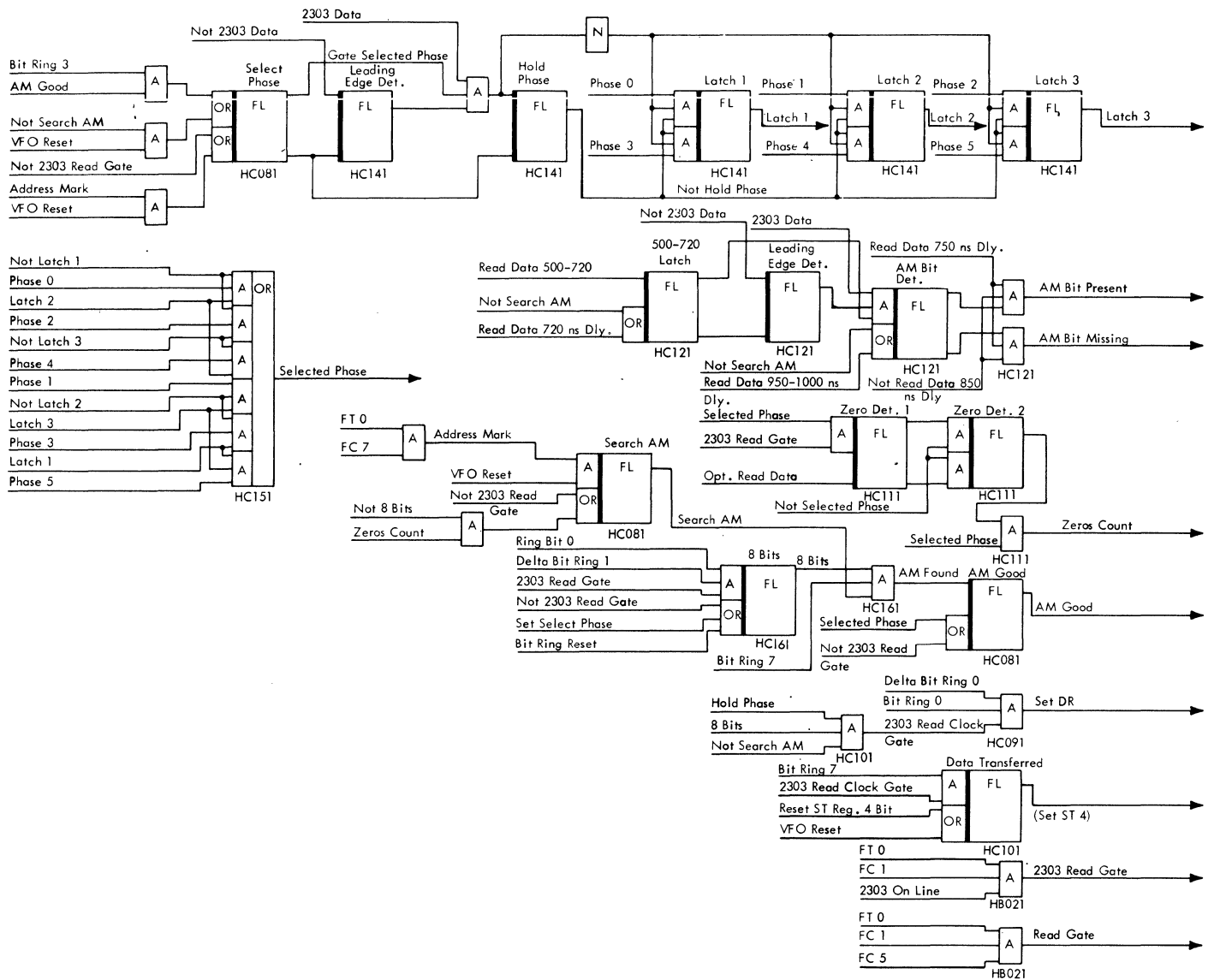
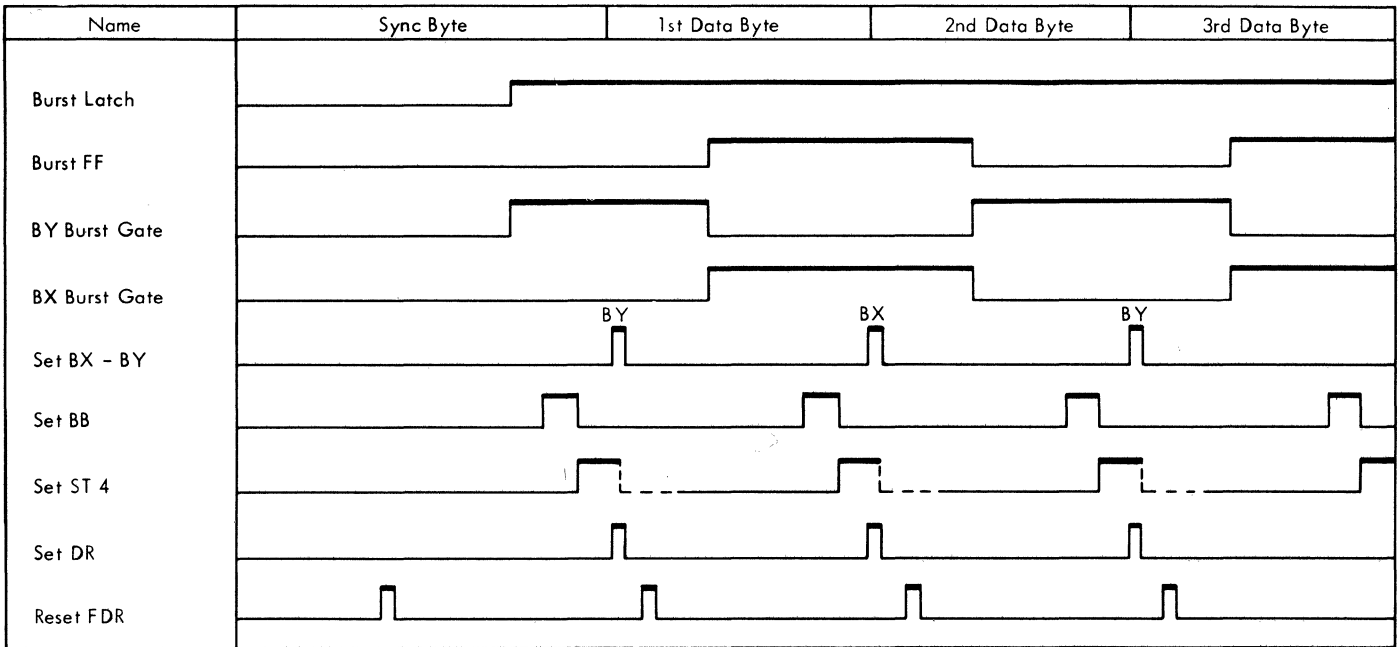
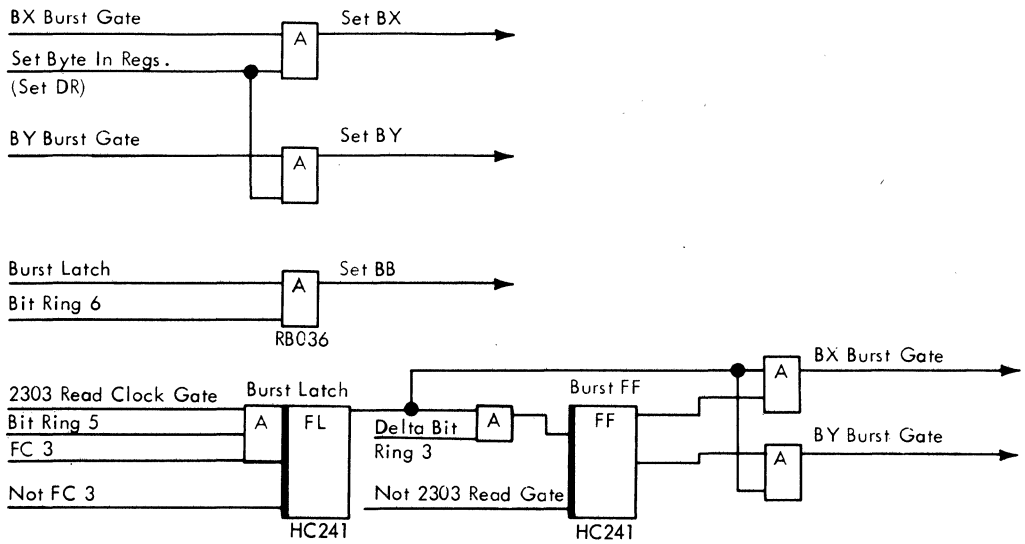


Figure 5-27a. 2303 S/D - Read Data Flow



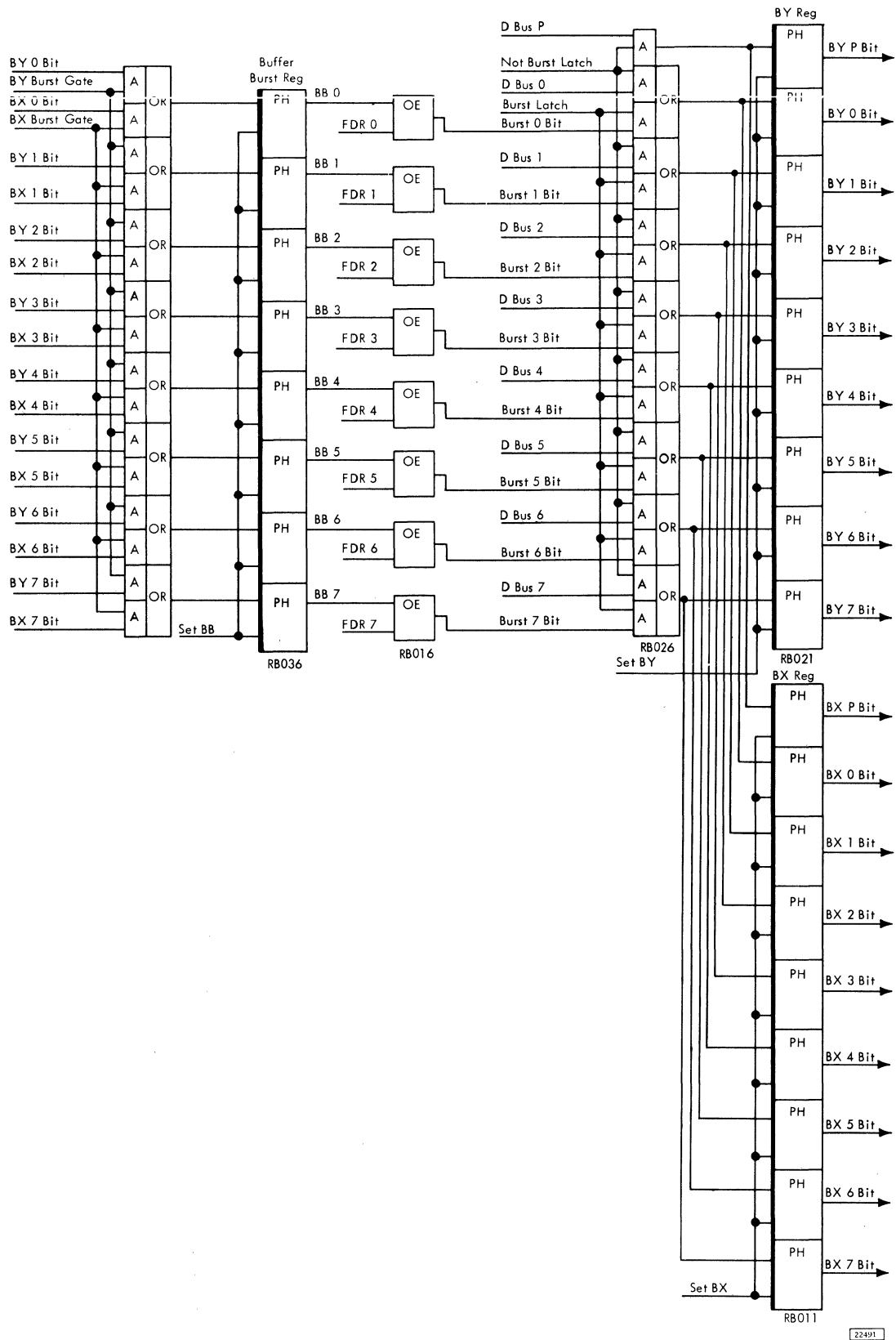
22489

Figure 5-27b. 2303 S/D - Read Data Flow



22490

Figuré 5-28a. 2303 Burst Circuit



22491

Figure 5-28b. 2303 Burst Circuit

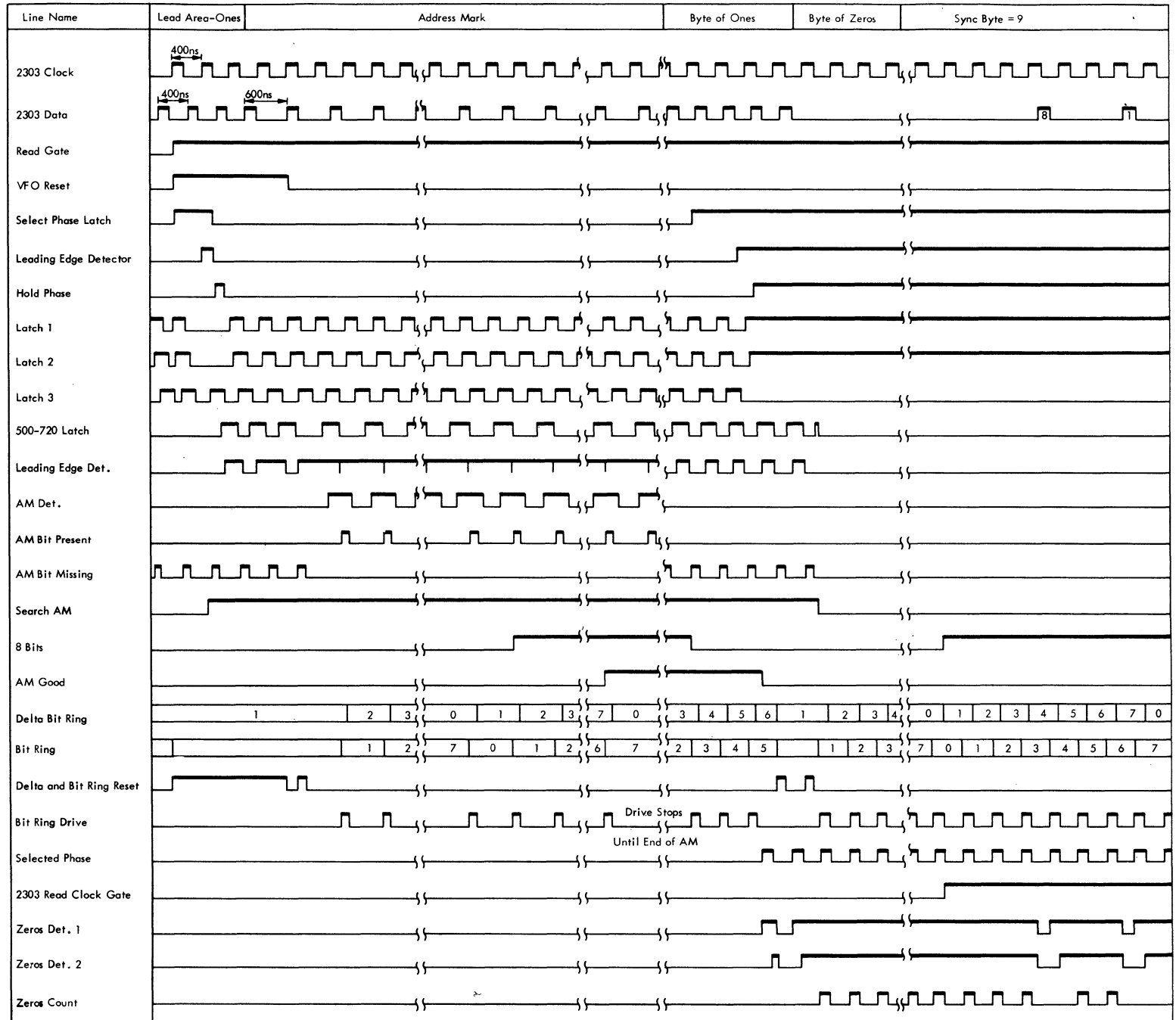


Figure 5-29. 2303 S/D - Read Timing

edge-det. and AM det.) start their sequence. The timing of the 500-720 FL and the leading-edge-det. FL with the normal data input rate prevents AM Det. FL from turning on until the address mark data is reached.

The bit-rings are driven by the address-mark-bit-present line to keep the rings in step with the data.

The 8 bits FL is turned on when eight address-mark bits have been read. The AM-good FL is turned on at the next bit-ring-7 time.

The select-phase FL is turned on at the next bit-ring-3 time. The leading-edge-detector FL is turned on with the fall of the next data pulse allowing the hold-phase FL to turn on with the following data pulse. The hold-phase FL blocks the advance of the latch sequence with some combination of latches on. The latches on and the phase time from the clock-track delay circuit gives selected-phase to lock the S/D circuits to the data from the 2303.

The selected-phase line turns off the AM-good FL and the bit-rings are reset to delta-bit-ring 1, and bit-ring all off.

At the end of the byte of ones following the address mark bytes, the zeros-count line comes up to drive the bit-rings while the byte of zeros is read.

The 8 bits FL is turned on at delta-bit-ring 1 time of the sync byte to turn off the search-address-mark FL and bring up the 2303-read-gate line.

The 2303-read-gate line allows the selected-phase line to drive the bit-rings in step with the data.

The data pulses from the 2303 turn on the file-data register (FDR) FL's or the buffer register FL's. The contents of FDR are transferred to the DR register at bit-ring-0 time of each data byte. Because of the timing conditions, 2303-data pulses for bit-ring-0 and 1 times are set into the buffer register. The FDR FL's are turned off at bit-ring-1 time. The buffer FL contents are transferred to the FDR zero and one FL's at bit-ring-2 time.

In the 2303 attachment, the development of the burst bytes is done by the circuits and not by the microprogram (Figure 5-28). The microprogram enables the circuit by giving a 16 → FC statement and setting constants in the BX and BY registers before the sync byte is reached. The burst-latch FL is turned on at bit-ring-5 time of the sync byte. Because the burst FF was held off until the 2303-read-gate line came up, the BY-burst-gate line is up to set the sync byte data into the BY register. The constants set into the BX (HA-AM=246) and BY (255) registers plus the sync byte data from FDR (HA-AM

=9) leave the BX and BY registers with all ones after the sync word. The contents of the BY register are transferred to the BB register and exclusive ORed with the contents of the FDR resulting in the BY register being equal to 255.

The burst FF is turned on at delta-bit-ring-3 time of the 1st data byte and the BX-burst-gate line comes up. The contents (255) of the BX register are transferred to the BB register and exclusive ORed with the contents of the FDR (1st data byte) and set into the BX register.

This bursting sequence is continued to the end of the field and the microprogram checks the BX and BY registers for zero.

## 5.2 ADDITIONAL STORAGE FEATURE

- This feature allows attachment of additional units of 2302 Models 3 and 4 to a basic 2841.
- A maximum of sixteen accesses in any combination of 2311, 2321, 2302-3, 2302-4 and 2303's is provided.
- All accesses above the basic eight must be 2302-3's or 2302-4's.
- Maximum of eight units.

The 2302-3 has two access mechanisms in each physical unit. Two consecutive access addresses must be assigned to each unit beginning with an even address (0-1, 2-3, 14-15).

The 2302-4 has four access mechanisms in each physical unit. Four consecutive access addresses must be assigned to each unit beginning with an address divisible by four (0, 1, 2, 3-12, 13, 14, 15).

It is presumed that there will be no more than one 2302-3 on a 2841. This is because one 2302-4 has the same functions as two 2302-3's for substantially less rental.

The hardware capability is:

1. Standard. A total of two physical 2302-3 or 2302-4 units attached to a 2841 in any of the following combinations:

2302-3	2302-4	Total Accesses
2	0	4
1	1	6
0	2	8

2. Standard plus Additional Storage Feature. A total of four physical 2302-3 or 2302-4 units attached to a 2841 in any of the following combinations:

2302-3	2302-4	Total Accesses
4	0	8
3	1	10
2	2	14
1	3	14
0	4	16

Two additional I/O connectors are added to the feature file connectors. They are addressed with a module select of 8 and 12 respectively.

As shown in Figure 5-8, the FT register bit 7, with the optional interface selected, gates the section of the additional accesses.

### 5.3 FILE SCAN FEATURE

- The file scan feature allows search operations on the data field.

The file scan function provides an automatic rapid search for a specific identifier or condition (Figures 5-30 and 5-31). The search applies to both the key and data fields. A control mask consisting of bytes of information on which a comparison is or is not to be made is placed in core storage. The bytes on which a comparison is not to be made are identified by a special configuration of bits (all one's). A scan command must be given for each key and data field to be scanned.

This feature provides three new commands, each of which may be used in multitrack mode.

Search Key - Data Equal (0010 1101)  
 Search Key - Data High (0100 1101)  
 Search Key - Data High or Equal (0110 1101)

If a logical comparison on equal is encountered, channel end, device end, and status modifier signals are generated. If a logical comparison is unequal, only channel end and device end signals are generated.

The length of the search is dependent upon the setting of the M/T bit of the search command and the sequence of commands given by the channel. If the M/T bit is a 1, the search continues until the specified condition is met or until the end-of-cylinder is encountered. Should the M/T bit be a 0, the search continues until the condition is satisfied or until two index points are sensed at which time unit check (no

record found), channel end, and device end signals are generated.

A KL of zero compares data only to the core mask.

If the CCW count is greater than (KL+DL), the search operation is completed when (KL+DL) equals zero. The 2841 terminates the command with status of channel end and device end. The status modifier bit is generated if the logical comparison was satisfied.

If a bus out parity error, overrun, or data check is detected during a search-key and data equal operation, unit check, channel end, and device end status is generated at the completion of the command.

If the 2303 is attached the file scan feature does not apply to the 2303 but may be used on the other devices.

### 5.4 TWO-CHANNEL SWITCH FEATURE

- The two-channel-switch feature provides the circuitry required to attach the 2841 Storage Control unit to a second channel. Switching from one channel to the other is done electronically under program control.

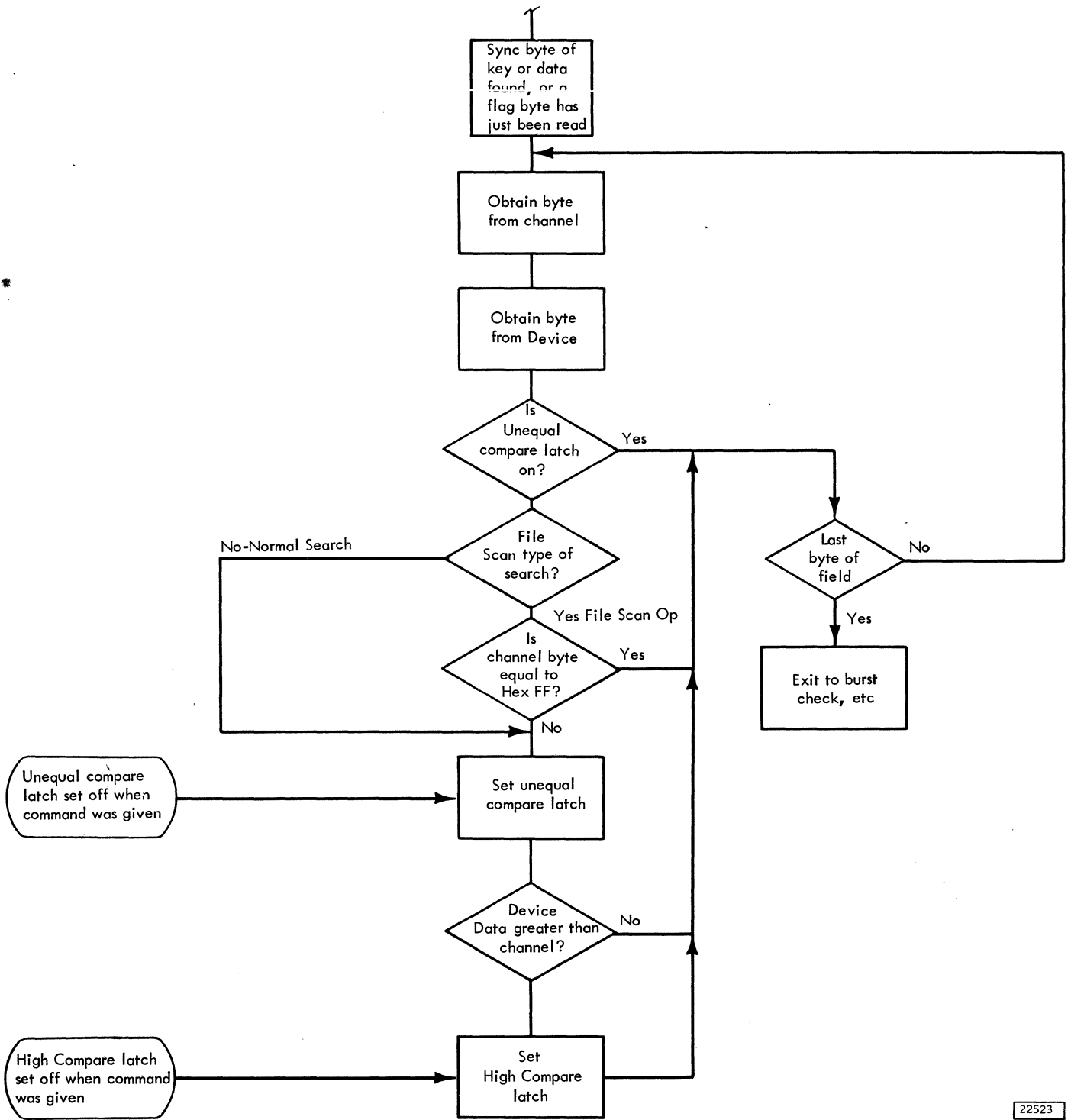
The two-channel-switch feature allows the 2841 Storage Control unit to be switched to either one of two channels or to a neutral position. (Figure 5-32).

The channel selection switch has three positions: channel A, channel B and neutral. When the switch is in the neutral position, the 2841 is selected by the first channel to complete the selection sequence. In the event both channels attempt to select the 2841 simultaneously, the tie is resolved by the switch logic.

Once the 2841 has been selected by a channel, it remains selected to that channel until ending status is presented. At that time the channel selection switch returns to neutral unless:

1. The channel indicates command chaining,
2. The last status byte was part of a channel-initiated signal sequence and was stacked by the channel,
3. The last status byte contained the unit-check bit (Contingent Connection), or
4. No command other than test I/O or no-op has been initiated since condition (3) occurred.

While a channel connection is being maintained as a result of condition (3) or (4) above, the 2841 will not respond to polling by the channel except to present stacked status, or control-unit-end. Once



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Figure 5-30. Expansion of Search/Scan Data Compare Loop





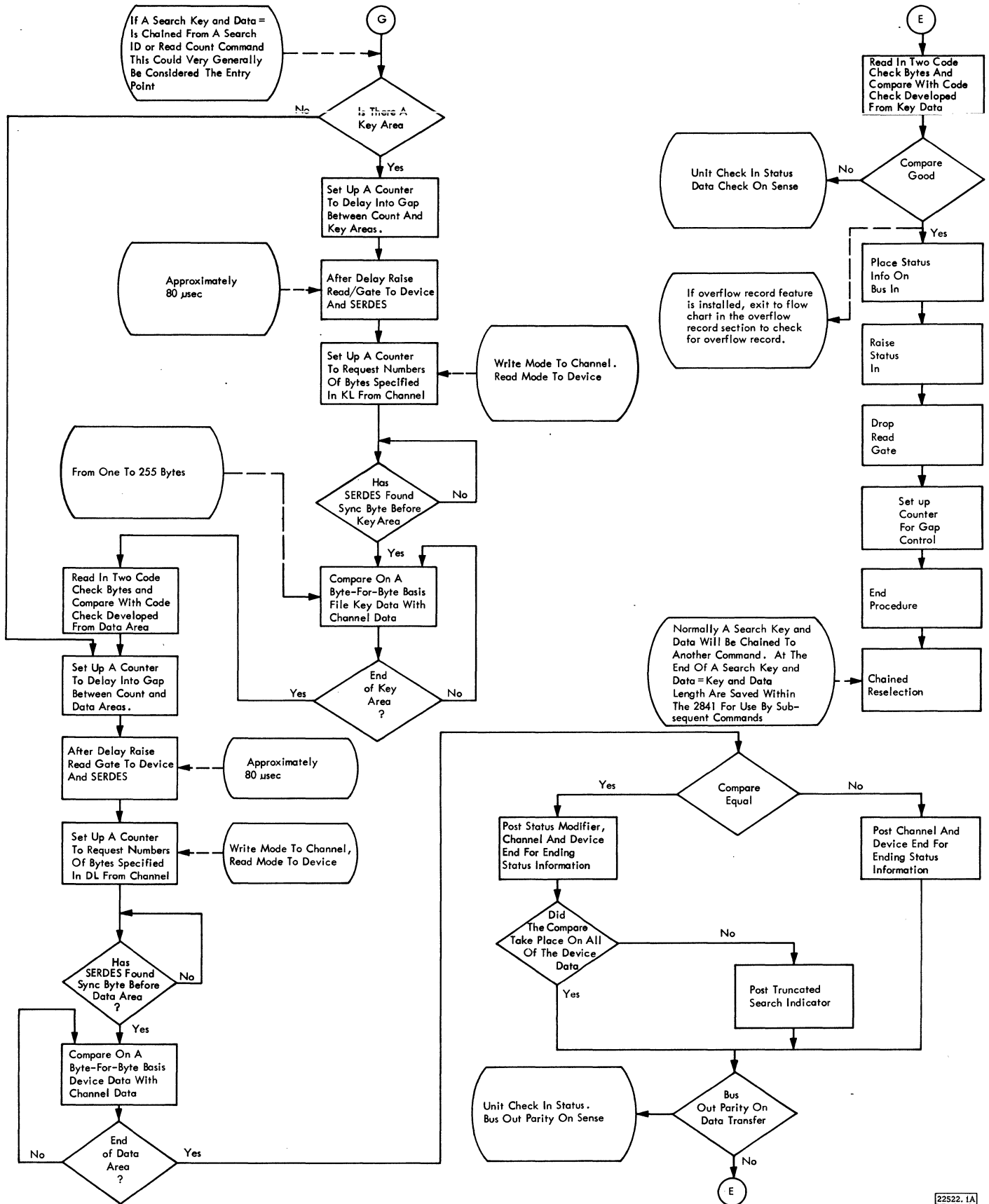


Figure 5-31b. Search/Scan Key and Data Equal

22522. 1A

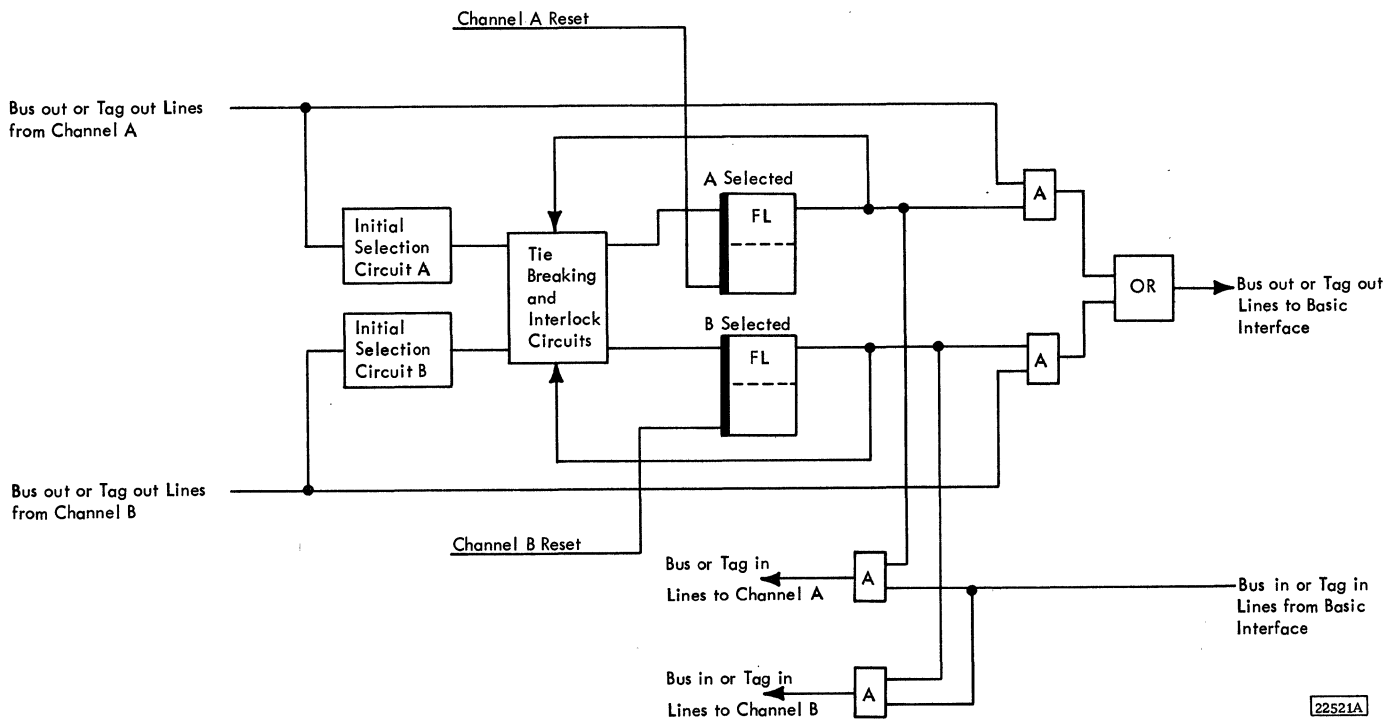


Figure 5-32. Two Channel Switch Data Flow

this connection is terminated, the sense information is reset by any signal sequence other than test I/O, sense I/O, or no-op over either interface.

If channel A (B) attempts to select the 2841 while the 2841 is selected to channel B (A), the 2841 responds to channel A (B) with the short control-unit-busy sequence. (Under no circumstances does the 2841 post control-unit-busy and control-unit-end in the same status byte.) This short control-unit-busy sequence may occur on any channel-initiated selection sequence (IPL, test I/O, and all initial commands of a CCW chain).

Whenever the short control-unit-busy sequence occurs, the 2841 attempts (by means of the request-in line) to present to channel A (B) a status byte containing control-unit-end after the channel selection switch returns to the neutral position. The address byte associated with this status condition is the base address of the 2841 on that channel. This pending control unit condition, in itself, does not cause the 2841 to appear busy to channel B (A) as long as the channel selection switch is not actually connected to channel A (B).

Both request-in lines may be up at one time if the channel selection switch is in the neutral position. The request-in line on one channel is degated whenever the channel selection switch is connected to the other channel.

The 2841 responds with unit check (command-reject) to all commands in the sense group other than sense I/O, device reserve or device release regardless of whether or not the two-channel-switch feature is installed.

#### 5.4.1 Device Reserve Command (1011 0100)

The device reserve command includes all of the functions of the sense I/O Command, and in addition, causes the addressed device to become reserved to the channel issuing the command. Once a device becomes reserved to a channel, it remains reserved until that channel causes the 2841 to execute a device release command addressed to that device or to perform a system reset.

A device reserve command is executed regardless of any abnormal device status conditions such as off line, unsafe, etc.

A device reserve command which is preceded in the same command chain by a set-file-mask command is rejected with unit-check (command-reject and invalid-sequence).

The device reserve command is rejected with unit-check (command-reject) by a 2841 which does not have the two-channel-switch feature installed.

#### 5.4.2 Device Release Command (1001 0100)

The device release command includes all of the functions of the sense I/O command, and in addition, causes the reservation of the addressed device to be terminated.

A device release command is executed regardless of any abnormal device status conditions such as off line, unsafe, etc.

A device release command which is preceded in the same command chain by a set-file-mask command is rejected with unit-check (command-reject and invalid-sequence).

The device release command is rejected with unit-check (command-reject) by a 2841 which does not have the two-channel-switch feature installed.

#### 5.4.3 Device Status

##### 5.4.3.1 General Condition

Whenever a device is busy for any reason, including reservation to channel A (B), any command from channel B (A) addressed to that device is rejected with busy status. This, in turn, causes the 2841 to attempt (by means of the request-in line) to present to channel B (A) a status byte containing device-end after the busy condition is terminated. The address byte associated with this status byte is the same as that associated with the busy-status byte.

No request-in is presented on channel A (B), as long as the requesting device is reserved on channel B (A).

Device-end status resulting from any channel command which causes mechanical motion of an access is presented to the channel that issued the command.

Device-end status resulting from a not-ready to ready transition is presented to both channels. Each channel must accept this device-end before it can use the device.

If, as a result of control unit initiated switching, a channel stacks a status byte containing device-end or control-unit-end alone, the channel selection switch returns to neutral and the control unit is not control-unit-busy to other device addresses from either channel, but attempts to present the stacked status again under control of suppress-out.

##### 5.4.3.2 Contingent Connection

A contingent connection state exists in the control unit after a unit check is generated, and lasts until an initial status byte of zero is given to some command other than test I/O. In this state, the control unit operates in the following manner:

1. Does not raise request-in or respond to polling caused by status pending in a device. (However,

status pending in the control unit does cause request-in.)

2. Stays connected to the channel on which the unit check occurred.
3. Maintains a logical connection to the device unless another device attached to the control unit is addressed while no status is pending in the control unit for this channel. This logical connection makes the device unavailable (busy) to other channels.

#### 5.4.4 Miscellaneous

##### 5.4.4.1 Addressing

The base address (four high-order bits) of the 2841 on one channel is independent of the base address of the 2841 on the other channel. However, the four low-order address bits for any attached device must be the same on both channels. Bit position 4 of all device addresses must be zero.

##### 5.4.4.2 System Reset

A system reset can be initiated by either channel at any time. A system reset causes all reservations and status conditions stored in the 2841 and related to the resetting channel to be reset. Reservations, operations, and status conditions related to the other channel are not affected. Both channels may initiate system resets at the same time. If a channel initiates a system reset when the channel selection switch is not selected to the other channel, the 2841 performs a machine reset. A selective reset has no effect on device reservations or status.

##### 5.4.4.3 Interface Timing

Occasionally, an interface signal sequence requires more than 32  $\mu$  sec. This cannot occur on any CCW following the first CCW in a chain. All signal sequences require less than 64  $\mu$  sec. This is an exception to the interface definition.

##### 5.4.4.4 Use Meter

A single usage meter records process time in the 2841; however, a separate meter-enable switch is provided for each channel interface. These switches allow each interface to be disabled independently and provide a partitioning capability. While in the disabled state, an interface always propagates select-out and cannot raise any inbound tag line.

An optional feature is available to remove the meter-enable switches from the 2841 and place them on a remote configuration unit (such as the IBM 2167) for time sharing systems.

In order to disable a channel interface, the following conditions must exist:

1. The enable switch for that channel must be in the DISABLE position,
2. The channel selection switch in the 2841 must not be selected to that channel, and
3. The clock-out line from that channel must be down.

In order to allow a channel interface to return to the enabled state, the following conditions must exist:

1. The enable switch for that channel must be in the ENABLE position, and
2. The clock-out line from that channel must be down.

**Programming Note:** If a CPU is allowed to enter the stopped or wait state when the 2841 contains outstanding status, the status may be made unavailable if the meter enable switch has previously been set to DISABLE.

The clock-out line to the attached devices is up if either interface is enabled and has clock-out up.

#### 5.4.4.5 Power Control

A power control interface is provided for each channel. If either channel indicates power on, the 2841 turns on. The 2841 will turn off only if both channels indicate power off. The normal CE power control is available as described in Chapter 4.

The emergency power off (EPO) line from either channel A or B drops the 2841 EPO relay. The dropping of the EPO lines is controlled by channel power control circuit.

#### 5.4.5 Two-Channel Switch Circuit Description

The two-channel switch feature provides the circuits for: the two sets of channel interface connectors (A and B), two select out jumper cards, two address decode jumper cards, selection circuits for each channel, gated 'in' and 'out' lines to and from both channels, and eight SW registers. The two-channel circuits are shown on FEMDM pages 1450-1 through 1450-4. The selection circuits shown on FEMDM 1450-1 are activated as follows:

1. 'Address out' from channel A is activated and passes through the address jumper card and address compare circuits to activate the 'addr compare A' line.
2. 'Addr compare A' and '(not)select out A' lines AND to turn on the 'steering latch A' (1450-1).
3. 'Select out' from channel A is activated and passes through the selection relay (1450-4) to turn on the 'select out' latch, activating the 'select out A' line.

4. 'Select out A' and 'steering latch A' lines (1450-1) are ANDed to activate the 'switched to A' line. The 'switched to A' line gates the 'bus out' lines from channel A and blocks the 'switched to B' line, preventing a selection by channel B until channel A deactivates the 'hold out' line.

The balance of the operation is the same as a single channel interface using the circuits gated by the 'switched to A' line.

There are eight SW registers added to the 2841 with the two-channel switch feature (1450-4). The SW registers are used by the microprogram to keep track of the status of each device for each channel. The specific UR register 'module select bit' that is on determines the SW register to be used for an operation.

Each SW register is functionally divided into two parts. Bit positions 0-3 are related to channel A, and bit positions 4-7 to channel B.

0	1	2	3	4	5	6	7
Res. to A	DE* Pack Change	DE* SC + Busy	DE* Seek In Prog. + Busy	Res. to B	DE* Pack Change	DE* SC + Busy	DE* Seek In Prog. + Busy
Channel A				Channel B			
SW Register for the Selected Module							

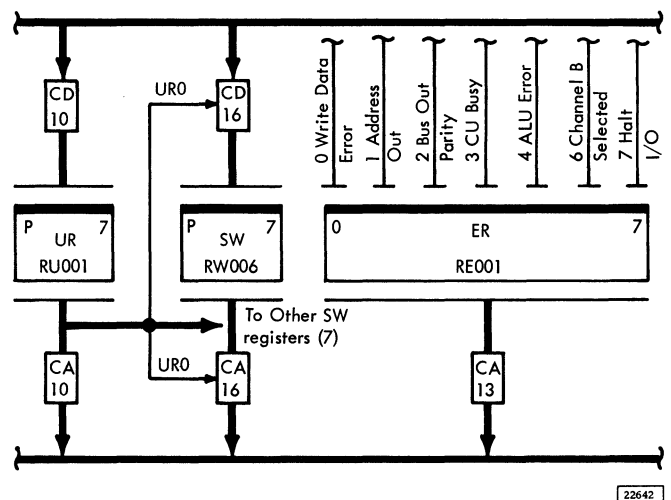
The SW bit position assignments are as follows:

Position	Name	Meaning
0	Reserve Unit "x" A	Bit 0 is turned on by the microprogram when channel A issues a reserve command and the module is not reserved to channel B. This bit is turned off when channel A issues a release command.
1	Device end* pack change "x" A	This bit is turned on by the microprogram when the 'gated attention' line (from the selected module) is detected, and no previous seek command has been issued. This condition means the 'attention' was caused by:

<u>Position</u>	<u>Name</u>	<u>Meaning</u>
1 (Cont)		a power-on seek, a pack change, or the meter switch (on the module) has been transferred from DISABLED to ENABLED. This bit is turned off when the 'device end' has been presented to and accepted by channel A.
2	Device end* seek complete + busy "x" A	This bit is turned on by the microprogram when the 'gated attention' line from the selected module (following a previously issued seek command) is detected If the module is reserved to channel B and channel A attempts to select the module, bit 2 is turned on. This 'device end' condition is presented to channel A after channel B has released the module to allow channel A to determine that the module is available.
3	Seek in progress + busy "x" A	This bit is turned on by the microprogram when the 'seek start' condition is sent to the module (seek command issued by channel A). This bit indicates a seek is in progress and is used (with bits 1 and 2) by the microprogram to determine if a 'gated attention' from the selected module is the result of a seek command or a pack change. The bit is turned off when the 'gated attention' from the module is acknowledged by turning on bit 2.

<u>Position</u>	<u>Name</u>	<u>Meaning</u>
4	Reserve Unit "x" B	These bit positions have the same functions as bit positions 0-3 respectively, but are related to channel B.
5	Device end* pack change "x" B	
6	Device end* seek complete + busy "x" B	
7	Seek in progress + busy "x" B	

The SW registers have entries from the D bus and exits to the A bus.



The SW register circuits are shown on FEMDM 1450-4.

The SW register output lines 'reserve unit B', 'device end\* S.C. + busy A', 'device end\* pack change A', 'seek in progress + busy A', and 'seek in progress + busy B' lines are used in developing 'attention unit "x" Ch A' lines to poll the channel (1450-4).

#### 5.4.6 Command Examples

The following is an example of how the two-channel switch feature operates. Assume the following:

1. A 2841 with eight 2311's attached, and the two-channel switch feature installed, is being shared by two CPU's (Figure 5-33).
2. Interface A is attached to the MPX channel on System/360 Model 30.
3. Interface B is attached to a selector channel on a System/360 Model 40.
4. The 2841 is looping, waiting for selection, and all hardware has been reset.
5. The System/360 Model 40 (channel B) contacts the 2841 first.

The sequence of events is:

Channel B issues a 'reserve' command to the 2311 module 2; then channel A issues 'reserve' and seek commands to the 2311 module 5.

##### 5.4.6.1 Reserve Command Execution (Channel B)

The System/360 Model 40 (channel B) issues a 'reserve' command to the 2311 module 2. The 'switched to B' line turns on the ER6 bit during initial selection. ER6 indicates that channel B is working with the 2841 and allows the microprogram the capability of detecting which channel is acting with the 2841. Only channel B can turn on the ER6 bit.

The microprogram in the 2841 executes the 'reserve' command and turns on bit position 4 of SW register 2. Bit position 4 being on indicates to the microprogram that the 2311 module 2 is now exclusively reserved to channel B. This ends the 'reserve' command execution.

If, at this time, the System/360 Model 30 (channel A) tries to select the 2311 module 2, then the microprogram examines SW register 2, and finds bit position 4 on. Bit 4 on indicates that the 2311 module 2 is exclusively reserved to channel B. The microprogram then sends a device busy condition back to the System/360 Model 30 (channel A) during initial selection status presentation. The busy status indicates that this device cannot perform any work for channel A. The microprogram turns on bit position 2 (device end\* seek complete + busy 2 A) in SW register 2. The posted 'device end' condition does not affect any operations while the 2311 module 2 is reserved to channel B. When channel B no longer requires the 2311 module 2, it issues a 'release'

command to cancel the previous reservation. The microprogram then finds that bit position 2 in SW register 2 is on. Bit 2 on indicates that channel A attempted to use the 2311 module 2 while it was reserved to channel B. Because channel B has released module 2, the microprogram sends a 'device end' condition to channel A, indicating the 2311 module 2 is now available.

##### 5.4.6.2 Seek Command Execution (Channel A)

The System/360 Model 30 (channel A) contacts the 2841 to issue a 'reserve' command to 2311 module 5. The microprogram checks to see if the 2311 module 5 is reserved to channel B. Since it is not, bit position 0 in SW register 5 is turned on indicating the reservation of this device exclusively to channel A.

The System/360 Model 30 issues a seek cylinder command to the 2311 module 5. The microprogram checks the ER register 6 bit to see which channel is working with the 2841. In this example ER6 is off because only channel B can turn ER6 on.

The microprogram initiates the transfer of the six seek bytes from the CPU to the 2841. The microprogram establishes contact with the 2311 module 5 and transfers the necessary seek information to set up CAR, HAR, and the difference counter. 'Seek start' condition is sent to the 2311 module 5 to initiate movement of the access mechanism.

The seek is now under way and the microprogram turns on bit position 3 (seek in progress + busy 5 B) in SW register 5.

Ending status is now presented to channel A with the 'channel end' bit on in the status byte. The 'device end' bit is not turned on, because the seek has not been completed.

Upon completion of the seek operation by the 2311 module 5, the 'gated attention' latch is turned on indicating the seek has been completed. The 'gated attention' and 'poll enable' lines AND to cause 'request in' to be raised to channel A for presentation of 'device end' status (1450-4). During the selection sequence with channel A, the microprogram detects the outstanding attention on the 2311 module 5 and enters into a routine to determine if the attention is a result of a 'power-on seek', 'pack change', or a previously issued 'seek' command, and the microprogram now turns on bit position 2 (device end\* seek complete + busy 5 A) in SW register 5. Bit position 3 (seek in progress) is reset in SW register 5, because the seek has been completed and the type of 'gated attention' at the 2311 module 5 has been identified.

2841 TWO CHANNEL SWITCH

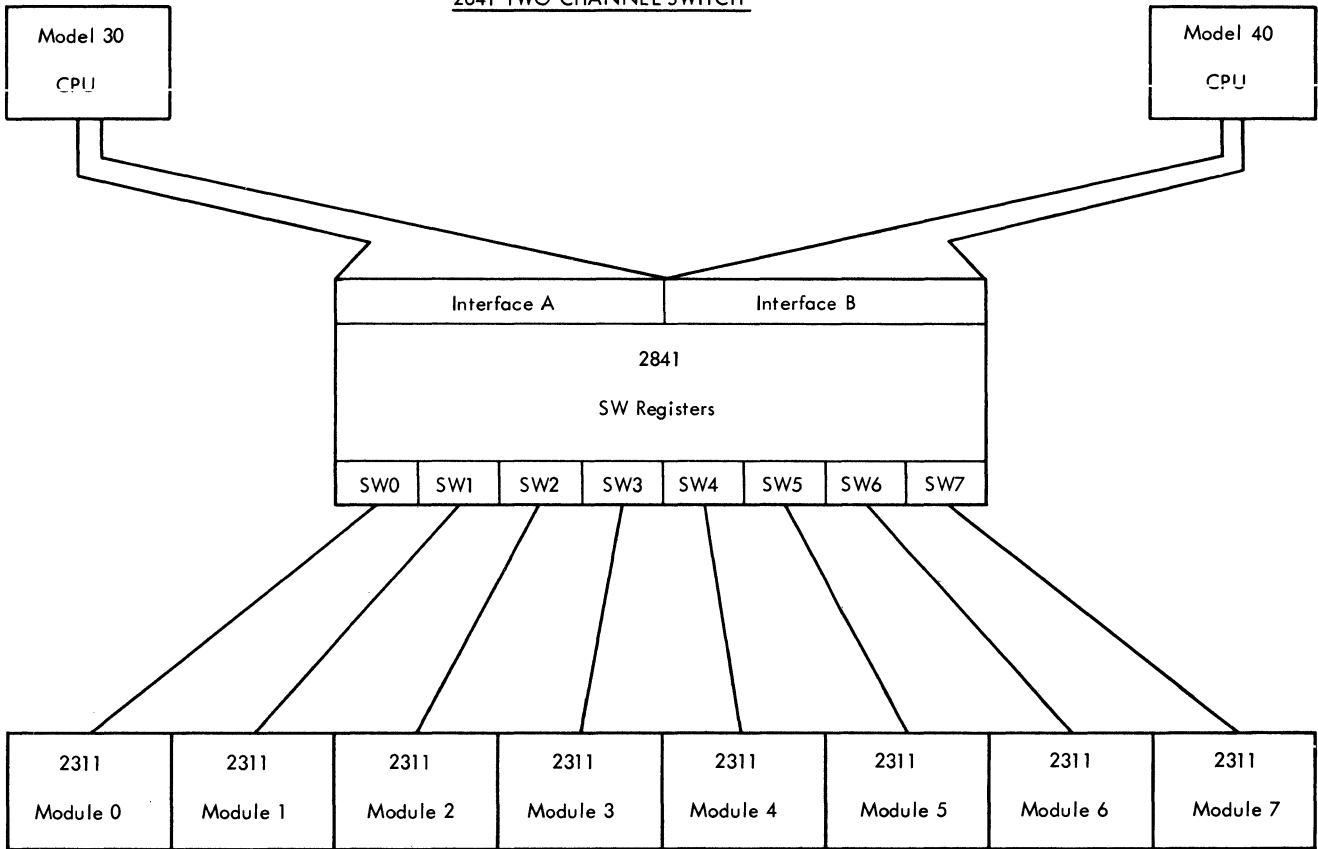


Figure 5-33. Two Channel Switch Configuration

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The 'gated attention' condition is reset in the 2311 module 5 because a record of that attention exists in SW register 5, bit position 2. The 'device end' condition is now presented to channel A. If the channel should respond to the presentation of device ending status with 'command out', the 2841 has a record of the 'device end' in SW bit position 2.

#### 5.4.6.3 Microprogram Flow Chart

The two-channel switch feature requires changes to the microprogram. To illustrate the changes, a flow chart of a 'reserve' or 'release' command is given in Figure 5-34. Only the direct path is shown. The flow chart assumes that channel B is selecting the 2841 and all modules are ready. There is no outstanding status stored, and all SW registers are at zero.

### 5.5 RECORD OVERFLOW FEATURE

- The record overflow feature allows a logical record to be more than one track in length.

The record overflow feature allows a logical record to overflow from one track to another. Record overflow is useful in achieving a greater data packing efficiency and in formatting records which exceed the capacity of a track. The limiting factor in the size of a record which can be overflowed is the cylinder boundary.

#### 5.5.1 Formatting Overflow Records

The portion of an overflow record which is written on one track is called a record segment. Each record segment is processed as a normal record during format write operations (Figure 5-35). The write special CKD CCW (0000 0001) is the command used for formatting all segments of an overflow record except for the last segment. The last segment is written by the normal write CKD CCW.

The write special CKD CCW causes a 1-bit to be written in bit position one of the flag byte of the record segment being written. Otherwise, the write special CKD CCW functions just like the normal write CKD CCW. Note that a write special CKD CCW is not a valid prerequisite for a normal write CKD CCW and results in the record flagged as a segment of an overflow record being the last record on a track.

When formatting overflow records, all segments other than the first must be recorded in the first record position following the R0 record on a track.

All segments, other than the first segment, are normally recorded without a key field, since only the key field of the first segment has significance.

All segments of an overflow record, other than the first and the last segments, are the only records on the track following the R0 record.

An overflow record may be formatted with a sequence of CCW's similar to the following. This sequence assumes that a set file mask instruction was performed prior to the initiation of the scan sequence.

- |                      |  |
|----------------------|--|
| 1. Seek              | Position access mechanism and select head. |
| 2. Search ID         | Determine beginning location.              |
| 3. Write Special CKD | Write first segment.                       |
| 4. Seek Head         | Select next head.                          |
| 5. Search HA or R0   | Locate next record.                        |
| 6. Write CKD         | Write last segment.                        |

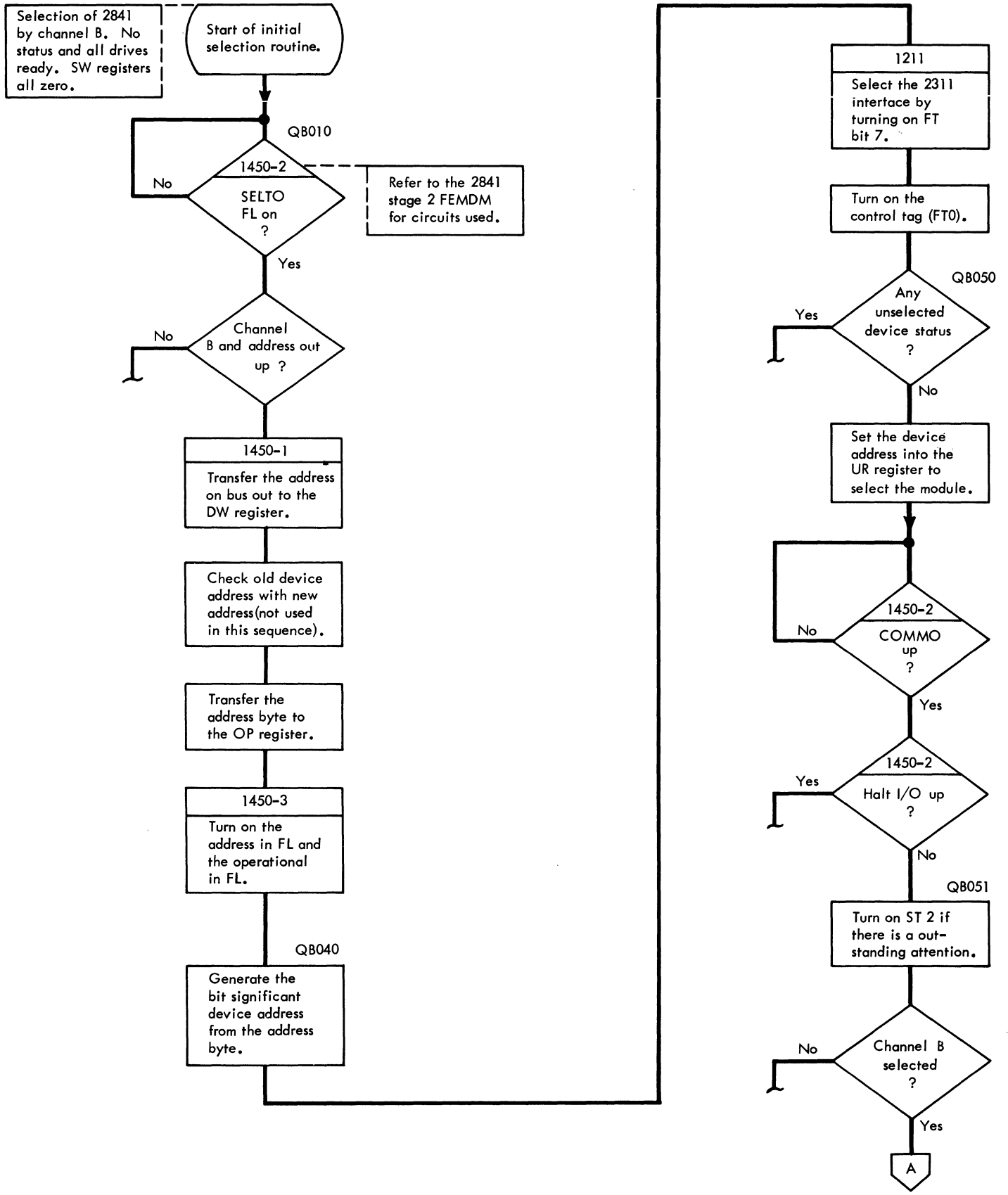
Items 3, 4, and 5 are repeated as often as needed.

#### 5.5.2 Processing Overflow Records

The read-data, read-key and data, read-count-key and data, write-data, write-key and data CCW's operate on an overflow record as though it were a normal record (Figure 5-35).

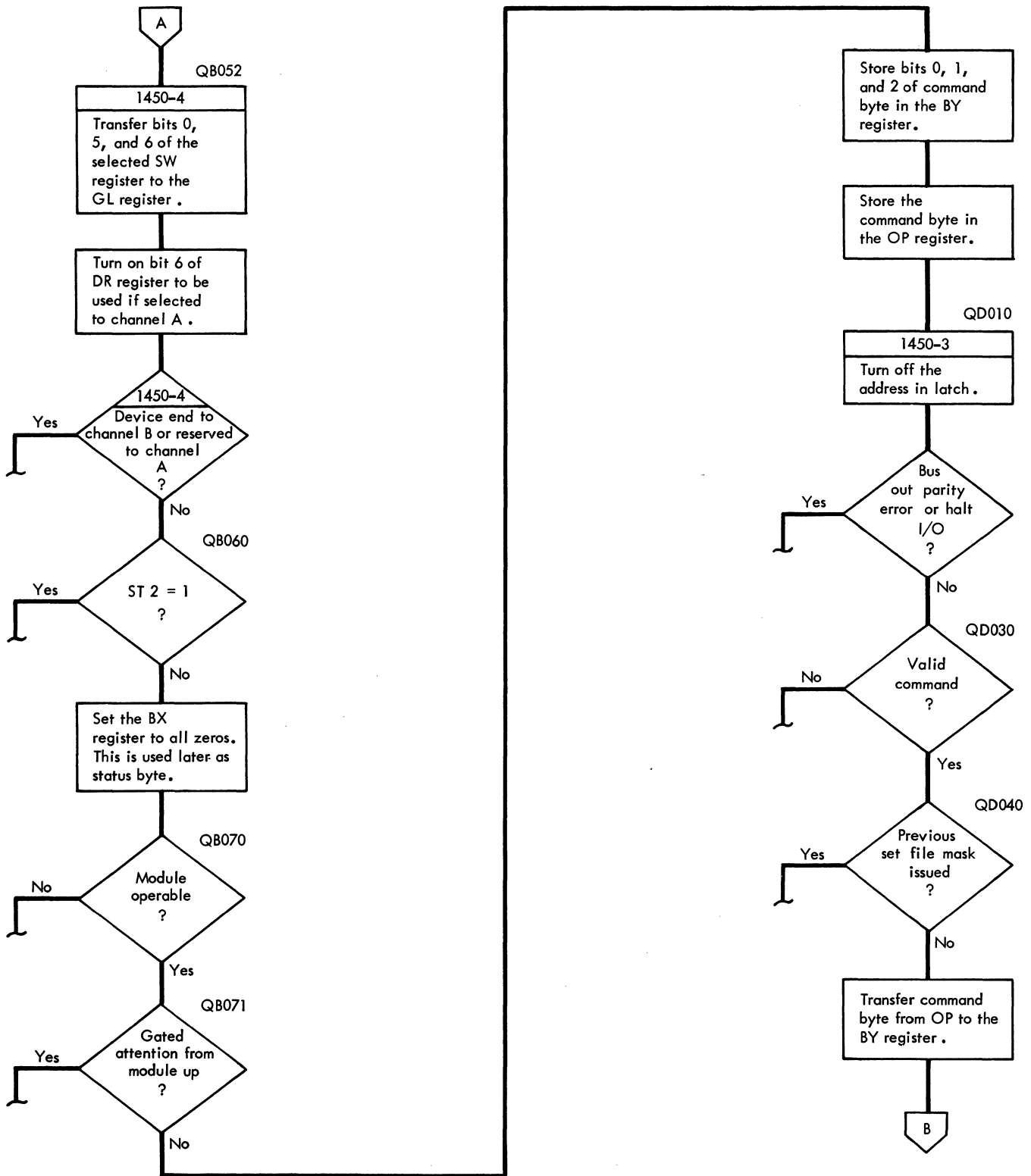
The 2841 detects that bit position on in the flag byte is a one bit. After completing the read or write operation in the first segment, the 2841 causes a search for the index point. At index point, the next sequential head is selected and a comparison of head number in the home address is done. If the comparison is equal, the 2841 searches for the first address mark on the track. Then, under control of the data count in the count field, it processes the data field of this record segment. This operation continues until the 2841 detects a record segment which contains a zero bit in bit position one of the flag byte. At the end of this record segment, the operation is terminated.

Only the data fields of all record segments except the first segment are processed when reading or writing, i. e., read-CKD reads CKD of the first segment and data only of all other segments. A CCW chain which starts operation on a record segment other than the first segment is processed as though it started on the first segment. This type of operation may make it desirable to repeat the key field in all record segments if the chain of CCW's is dependent on a satisfied search key equal.



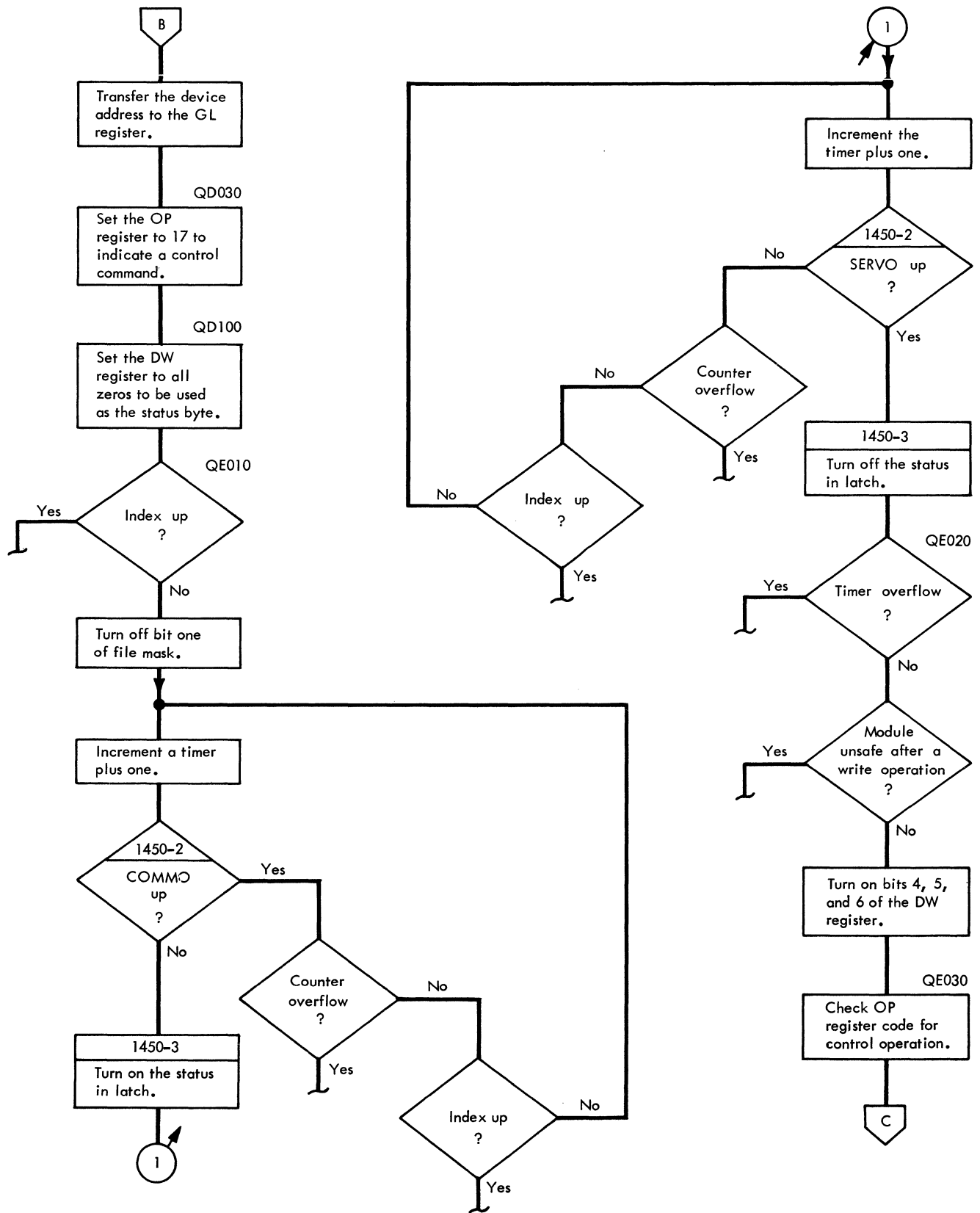
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Figure 5-34a. Two Channel Switch Flow Chart (Reserve or Release)



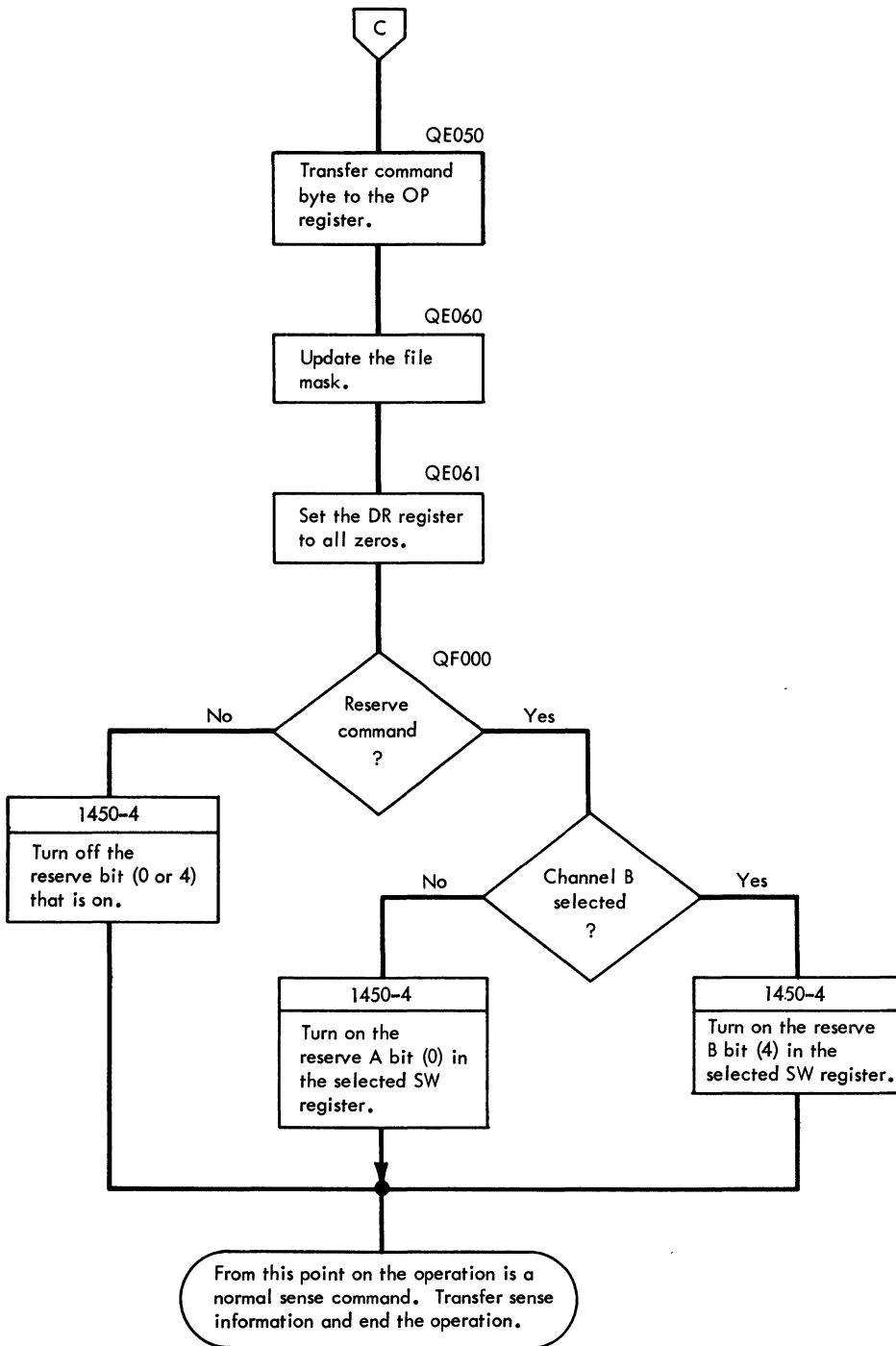
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Figure 5-34b. Two Channel Switch Flow Chart (Reserve or Release)



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Figure 5-34c. Two Channel Switch Flow Chart (Reserve or Release)



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Figure 5-34d. Two Channel Switch Flow Chart (Reserve or Release)

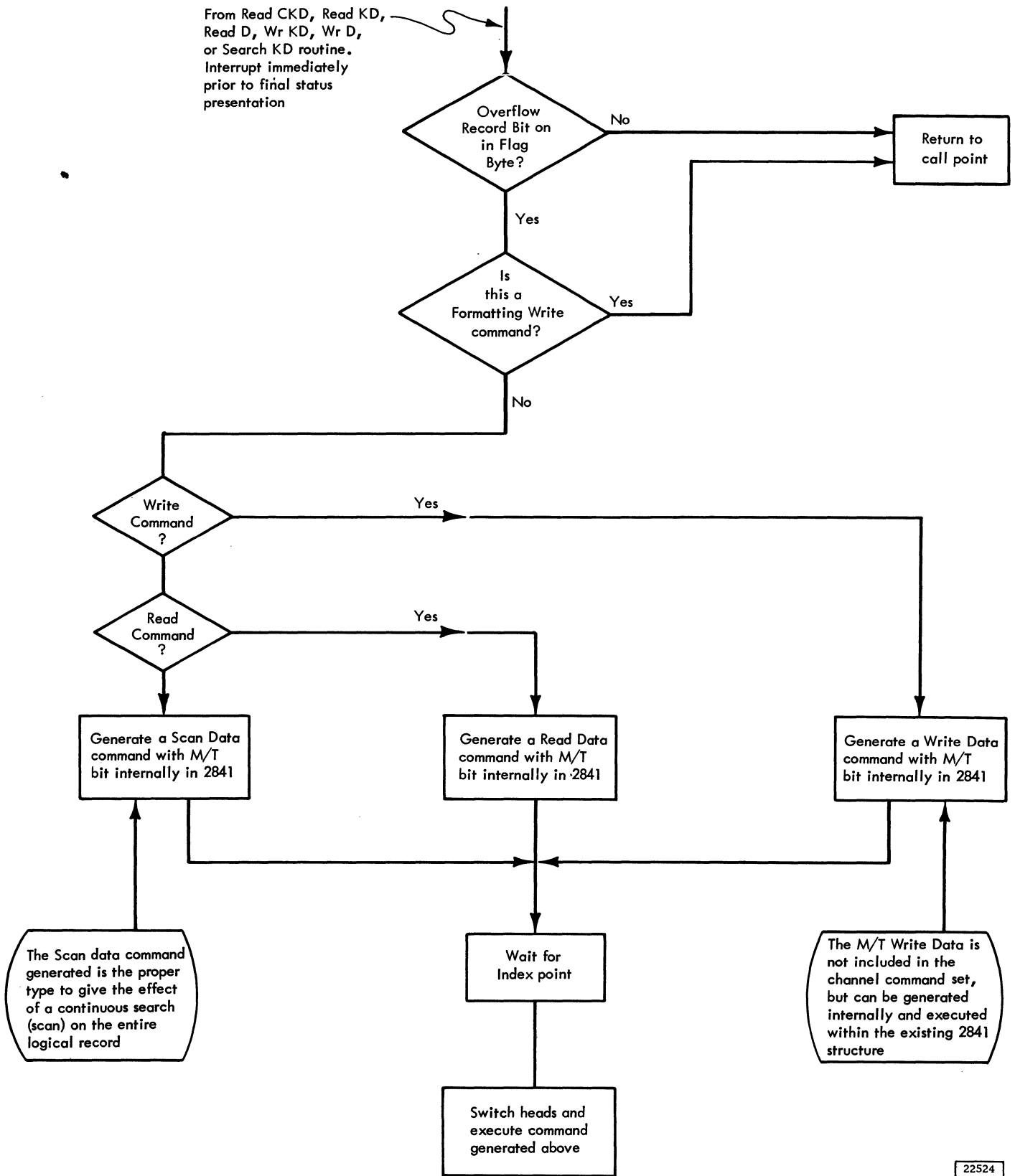


Figure 5-35. Execution of Commands with Overflow Record Feature

Search-ID, search-key and read-count CCW's operate on each record segment as though each segment were a normal record.

### 5.5.3 Unusual Conditions

In addition to the checks provided in normal processing of any record, certain conditions can occur which are unique to overflow records. The commands stop immediately on detecting the following conditions:

Overflow To a Bad Track: Overflow incomplete and track condition sense bits occur when overflowing to a track which has been flagged as being bad and two additional sense bytes, Bytes 4 and 5, are presented to the channel.

1. Byte 4 – This byte is all zeroes. It is a dummy byte inserted for control unit compatibility of byte 5 with other control units.
2. Byte 5 – This byte is zero at all times except when overflow incomplete occurs (Byte 1, Bit 7). When overflow incomplete occurs, this byte has one of the following configurations.
  - 00000110 – A read command was in progress when the overflow incomplete interrupt occurred.
  - 00000101 – A non-formatting write command was in progress.
  - 00100101 – A search key-data equal command was in progress, and the compare was equal to this point.
  - 01000101 – A search key-data high command was in progress, and the compare was equal to this point.
  - 01100101 – A search key-data high or equal command was in progress, and the compare was equal to this point.
  - 01010101 – Any search key-data was in progress and the compare was low, or a search equal key-data was in progress and the compare is unequal to this point. (i.e., it has already been determined that no status modifier bit would be set in the entire logical record.)
  - 01110101 – A search high or high-equal key data command was in progress, and the compare was high to this point, i.e., it has already been determined that a status modifier bit would be set in the logical record.

Byte 5 is used by programming systems to resume the scan loop after seeking to a new track.

Overflow From an Alternate Track: Overflow-incomplete and track-condition-check sense bits are

set if an attempt is made to overflow from a track flagged as an alternate.

Overflow to a File Protected Boundary: Attempting to overflow in violation of a file mask sets overflow-incomplete, file-protected, and command-reject.

Overflow to a Track with Incorrect Head Number: Overflow-incomplete and command-reject sense bits are set if the head number compare is unequal during an overflow. This condition occurs if the last seek address issued to the 2841 is not the address of the track with the overflow record and an overflow record is being read or written.

## 5.6 CHANNEL ISOLATION FEATURE

The channel isolation feature allows the 2841 to be powered up or down while the system is operating.

The feature is installed in all new machines, and may be installed on field machines, at no cost, on an as required basis.

The feature is identified by the version 007 indication on the ALD pages and by the different placement of the channel connectors.

To power down the 2841:

### Caution

Operating the interface degate switch out of the proper sequence can cause CPU problems.

1. The meter switch(es) is transferred to DISABLE.
2. When all outstanding status has been presented to and accepted by the channel(s), the meters disabled indicator light comes on.
3. The interface degate switch is transferred.
4. The mode switch is changed to CE mode, and the power off switch is transferred.

The circuits for the feature are shown on FEMDM 1450-1 through 1450-4.

On 1450-4 a relay is added in parallel to the selection relay. A point of this relay is grounded when the relay is not energized. The relays drop when the +6V supply power is dropped or the interface degate switch is transferred. The ground on the n/c point deactivates the 'power off gate' line. This blocks the 'in tag' lines, and the 'bus in' lines to prevent unwanted signals from being sent to the channel as the 2841 powers down.

On 1450-2 the 'select out latch' is added to hold the 'select out A(B)' line up until the channel drops the 'hold out' line.

The meters disabled indicator is shown on 1450-3. The 'meter enabled' latch cannot be turned off until the outstanding status has been accepted.

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875 kc (kHz) Write Oscillator 5-13



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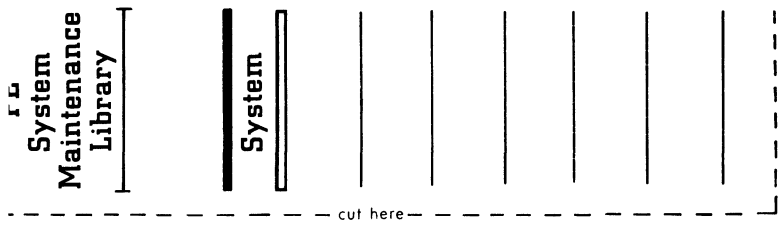
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