

IBM

**Field Engineering
Maintenance - Diagram**

Y27-0018-0

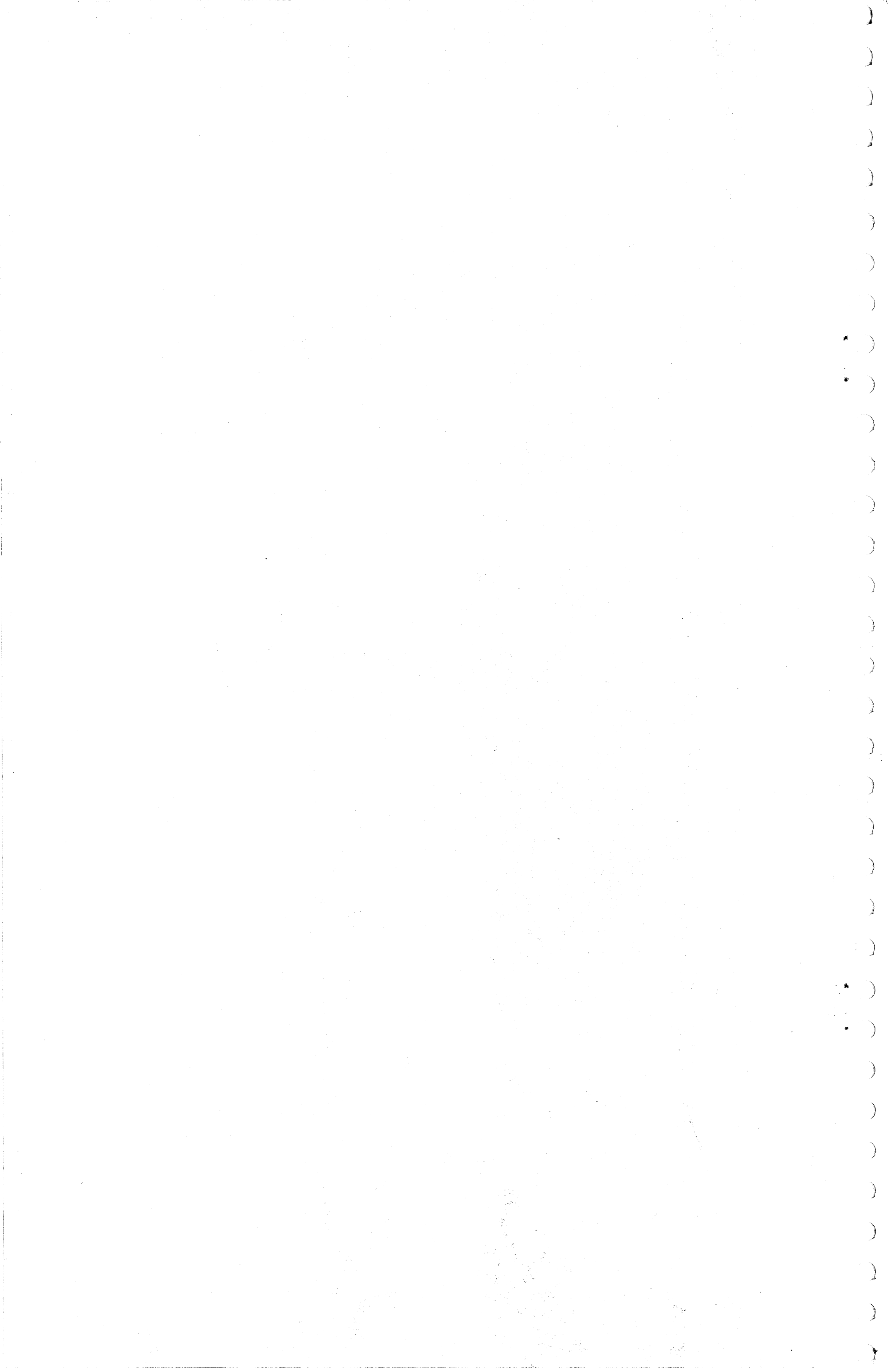
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1971 / 1980

Buffered Terminal



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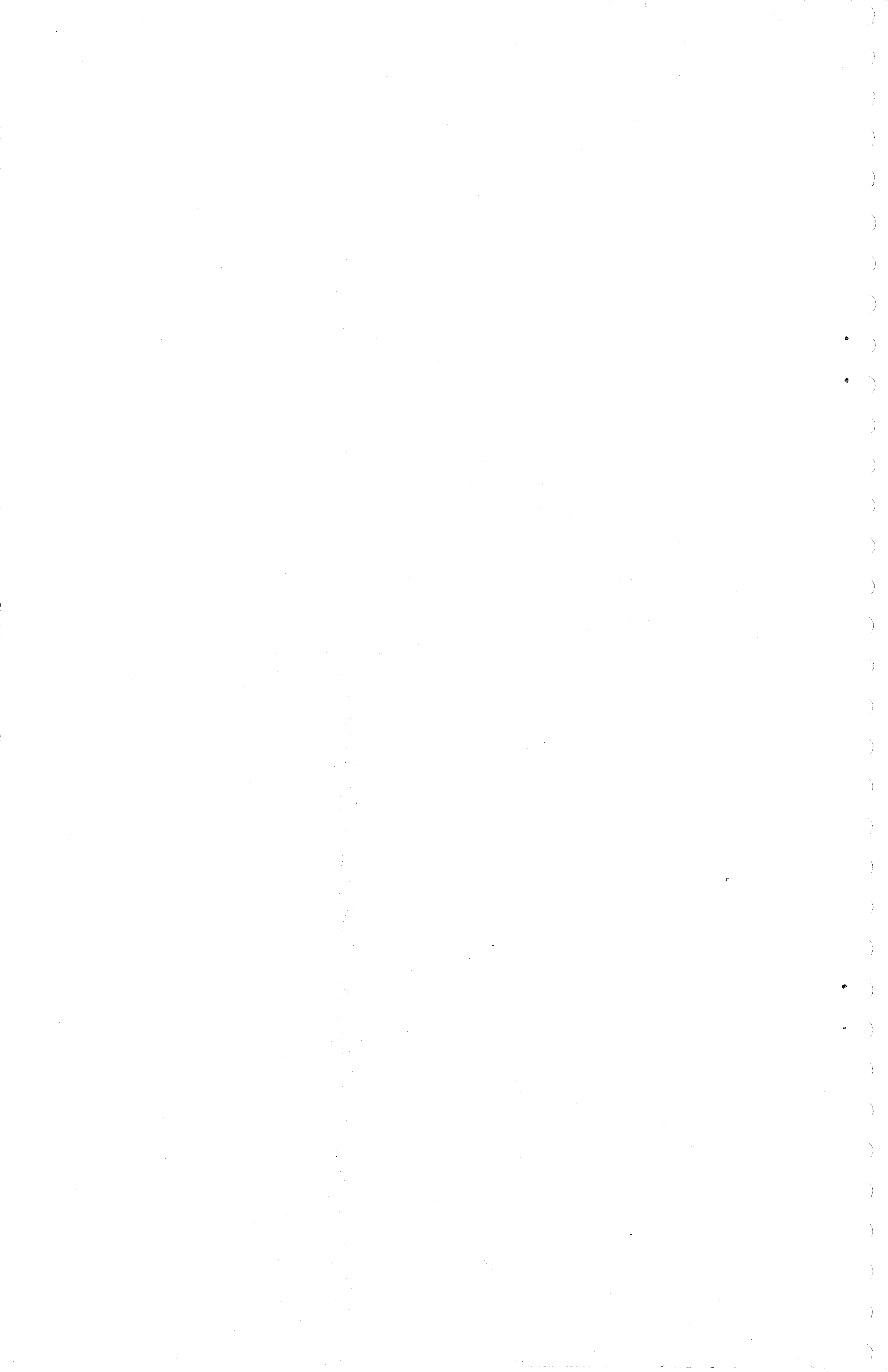
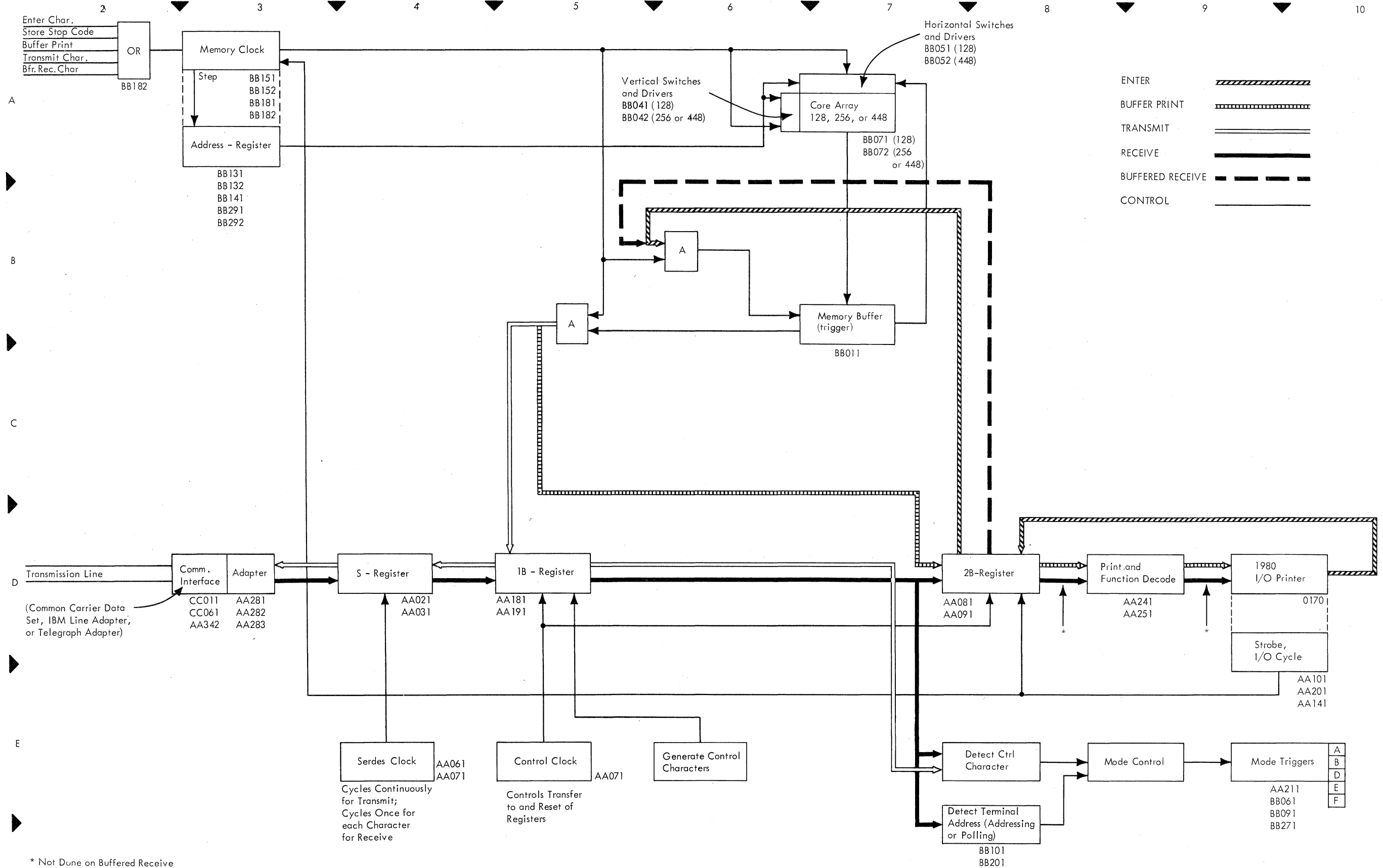
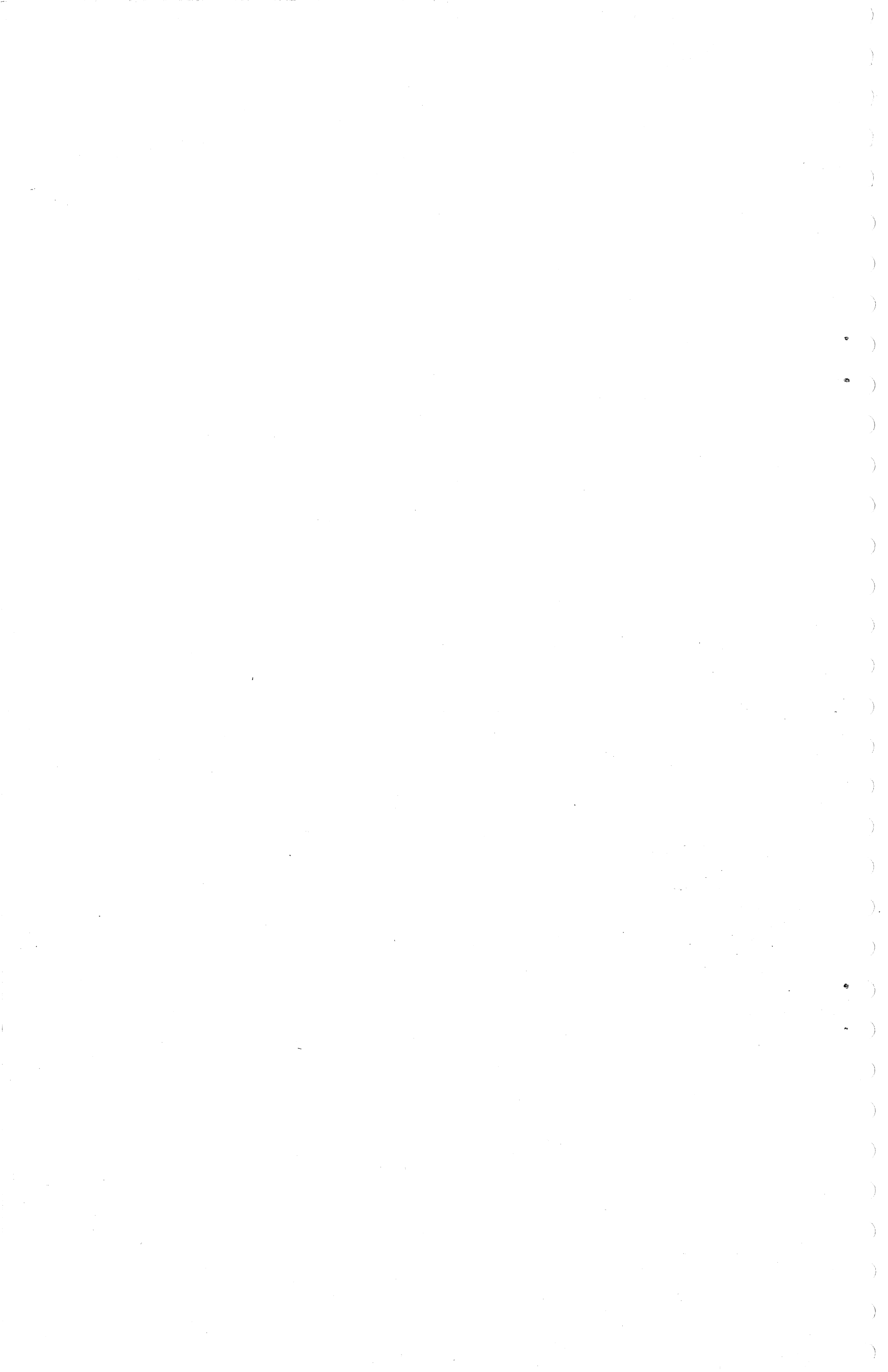


Figure UDC-1. 1971/1980 Buffered Terminal



* Not Done on Buffered Receive



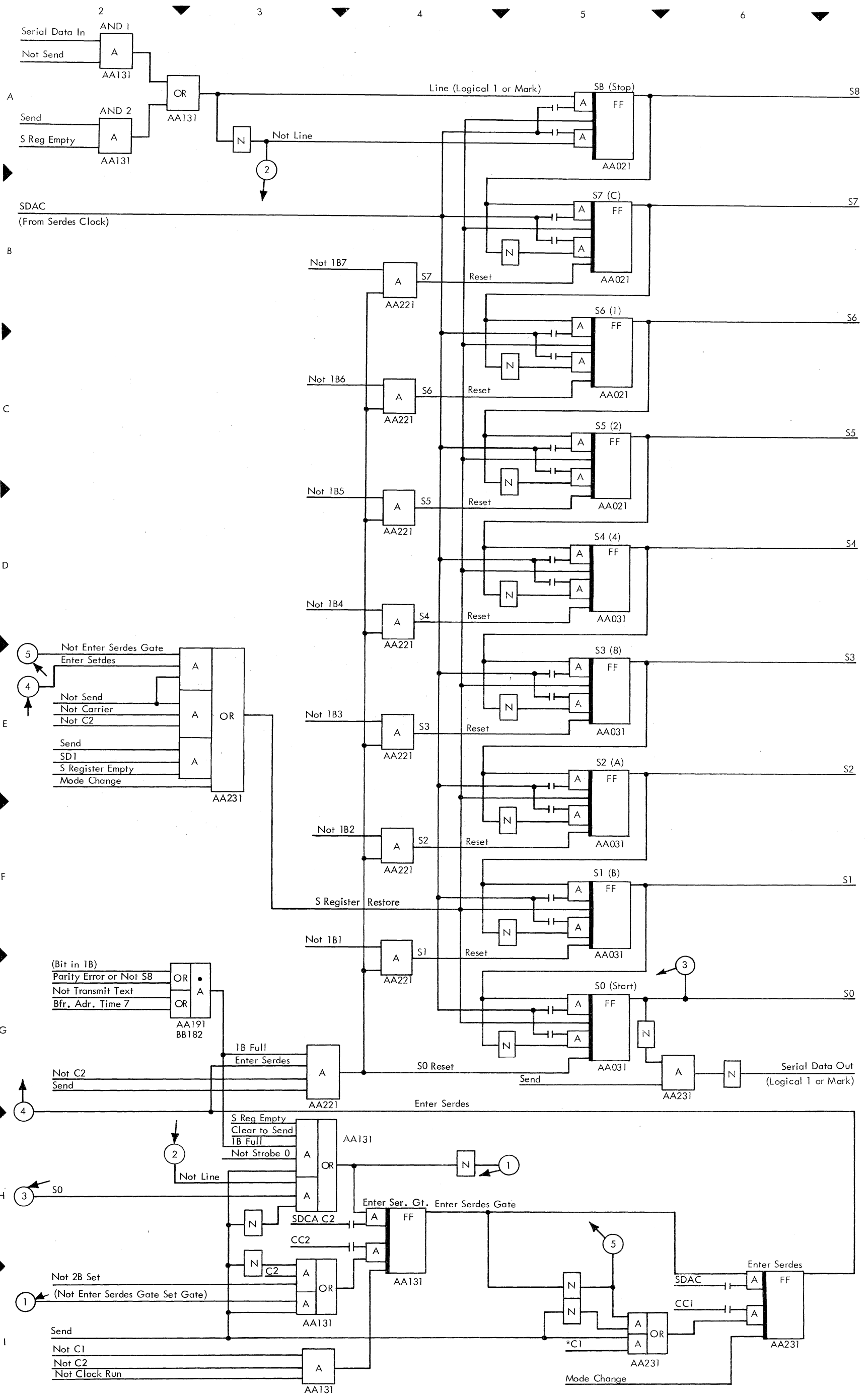


Figure FU-1. S-Register

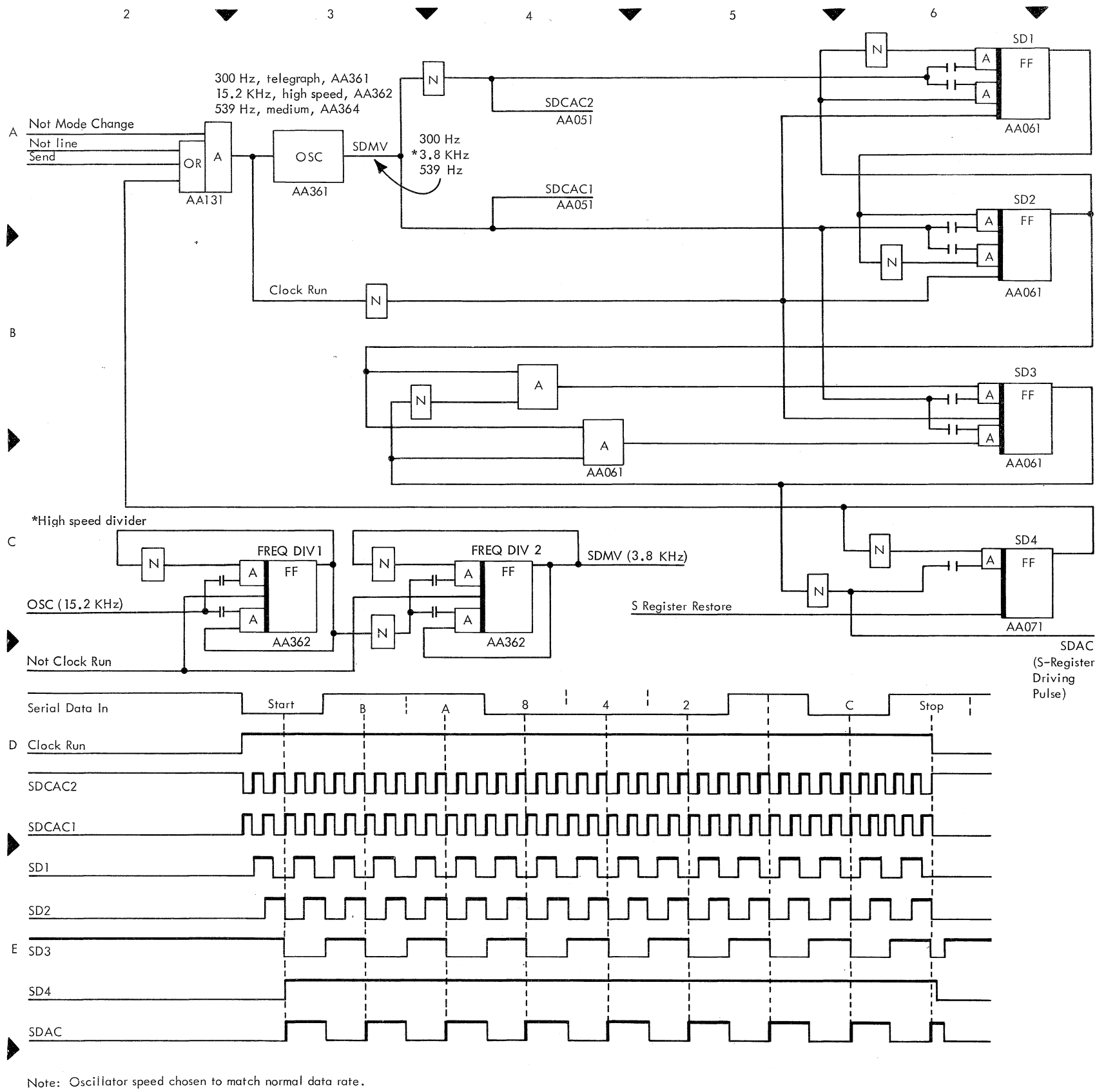
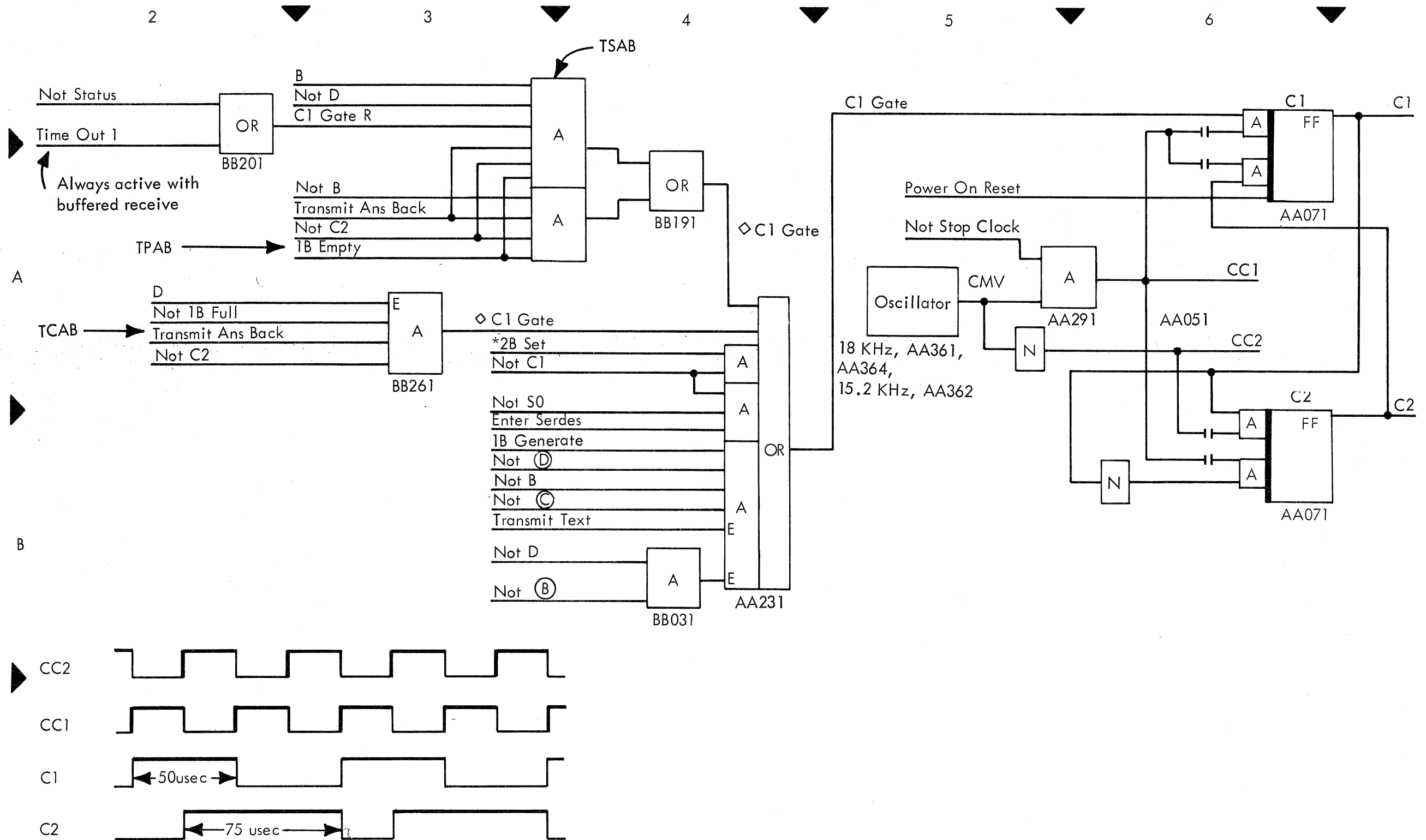


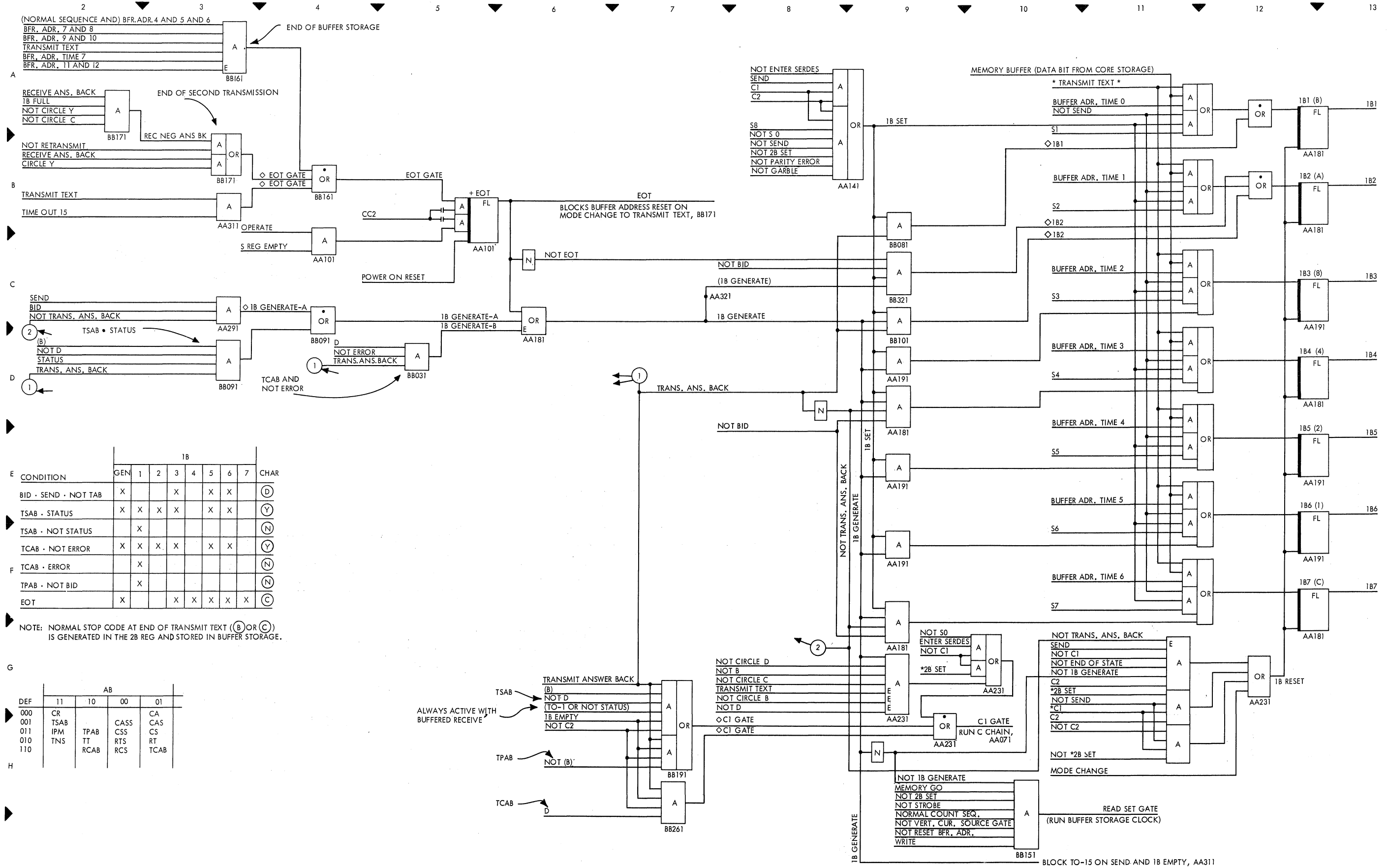
Figure FU-2. Serdes Clock

Figure FU-3. Control Clock



Note: Timing is slightly slower with 15.2 KHz oscillator. CC pulse duration is approx. 32.5 microseconds.

Figure FU-4. 1B-Register



(NORMAL SEQUENCE AND) BFR. ADR. 4 AND 5 AND 6
 BFR. ADR. 7 AND 8
 BFR. ADR. 9 AND 10
 TRANSMIT TEXT
 BFR. ADR. TIME 7
 BFR. ADR. 11 AND 12

RECEIVE ANS. BACK
 1B FULL
 NOT CIRCLE Y
 NOT CIRCLE C

NOT RETRANSMIT
 RECEIVE ANS. BACK
 CIRCLE Y

TRANSMIT TEXT
 TIME OUT 15

SEND
 BID
 NOT TRANS. ANS. BACK

NOT D
 STATUS
 TRANS. ANS. BACK

CONDITION	1B							CHAR	
	GEN	1	2	3	4	5	6		7
BID · SEND · NOT TAB	X			X	X	X			(D)
TSAB · STATUS	X	X	X	X		X	X		(Y)
TSAB · NOT STATUS		X							(N)
TCAB · NOT ERROR	X	X	X	X		X	X		(Y)
TCAB · ERROR		X							(N)
TPAB · NOT BID		X							(N)
EOT	X			X	X	X	X	X	(C)

NOTE: NORMAL STOP CODE AT END OF TRANSMIT TEXT (B) OR (C) IS GENERATED IN THE 2B REG AND STORED IN BUFFER STORAGE.

DEF	AB			
	11	10	00	01
000	CR		CASS	CA
001	TSAB		CSS	CAS
011	IPM	TPAB	RTS	CS
010	TNS	TT	RTS	RT
110		RCAB	RCS	TCAB

H

BLOCK TO-15 ON SEND AND 1B EMPTY, AA311

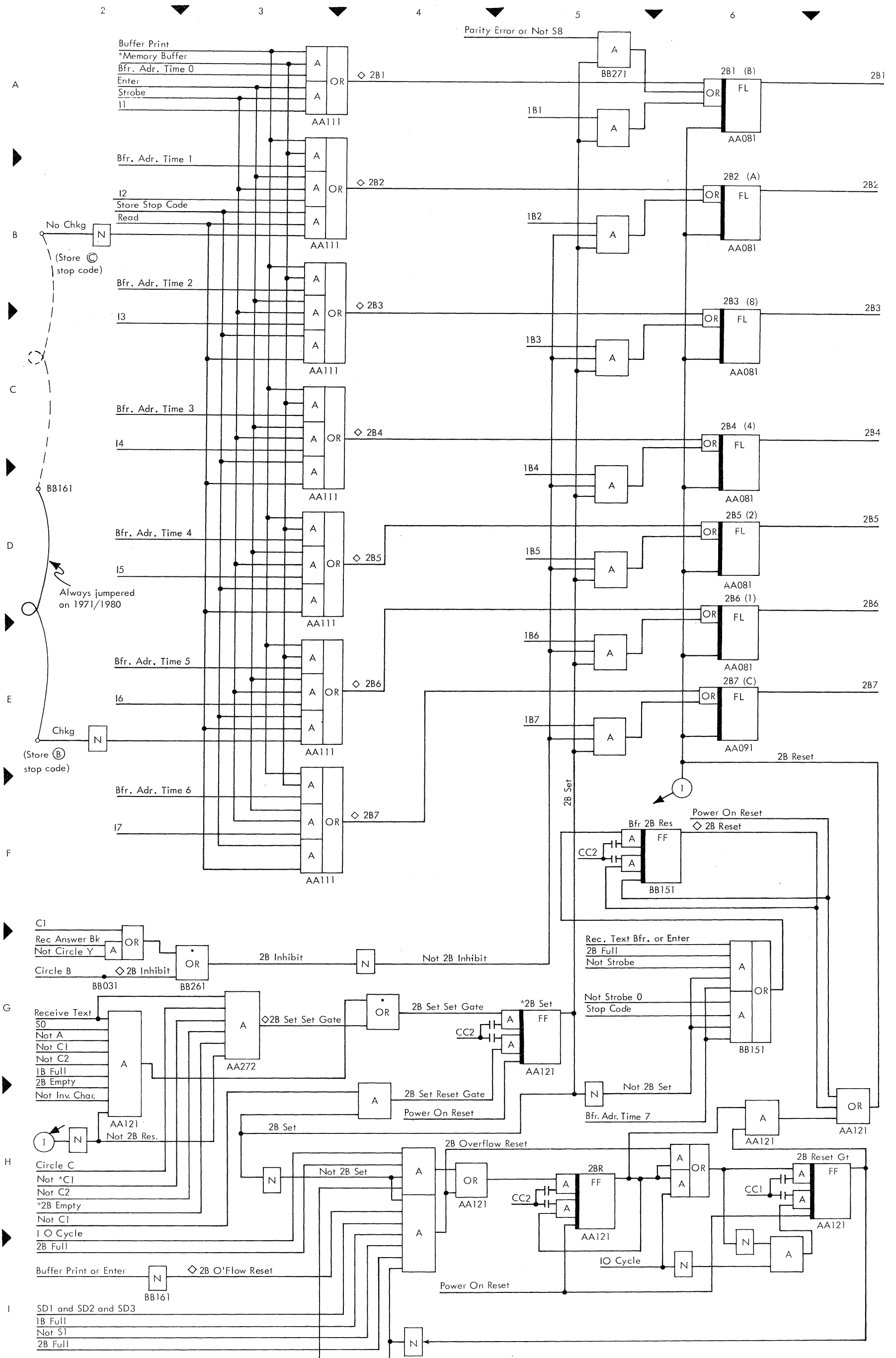


Figure FU-5. 2B-Register

Figure FU-6. Print and Function Decode

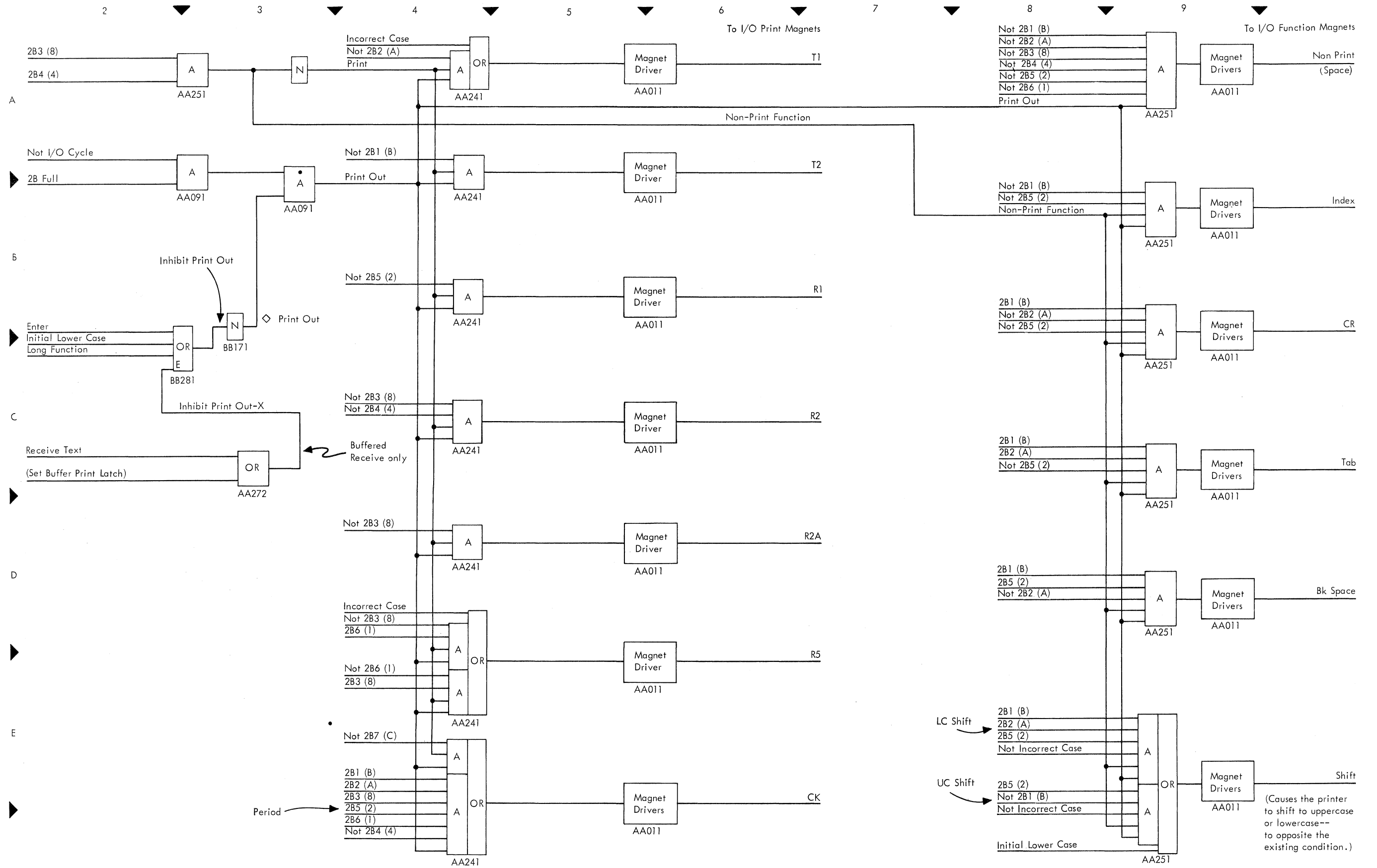
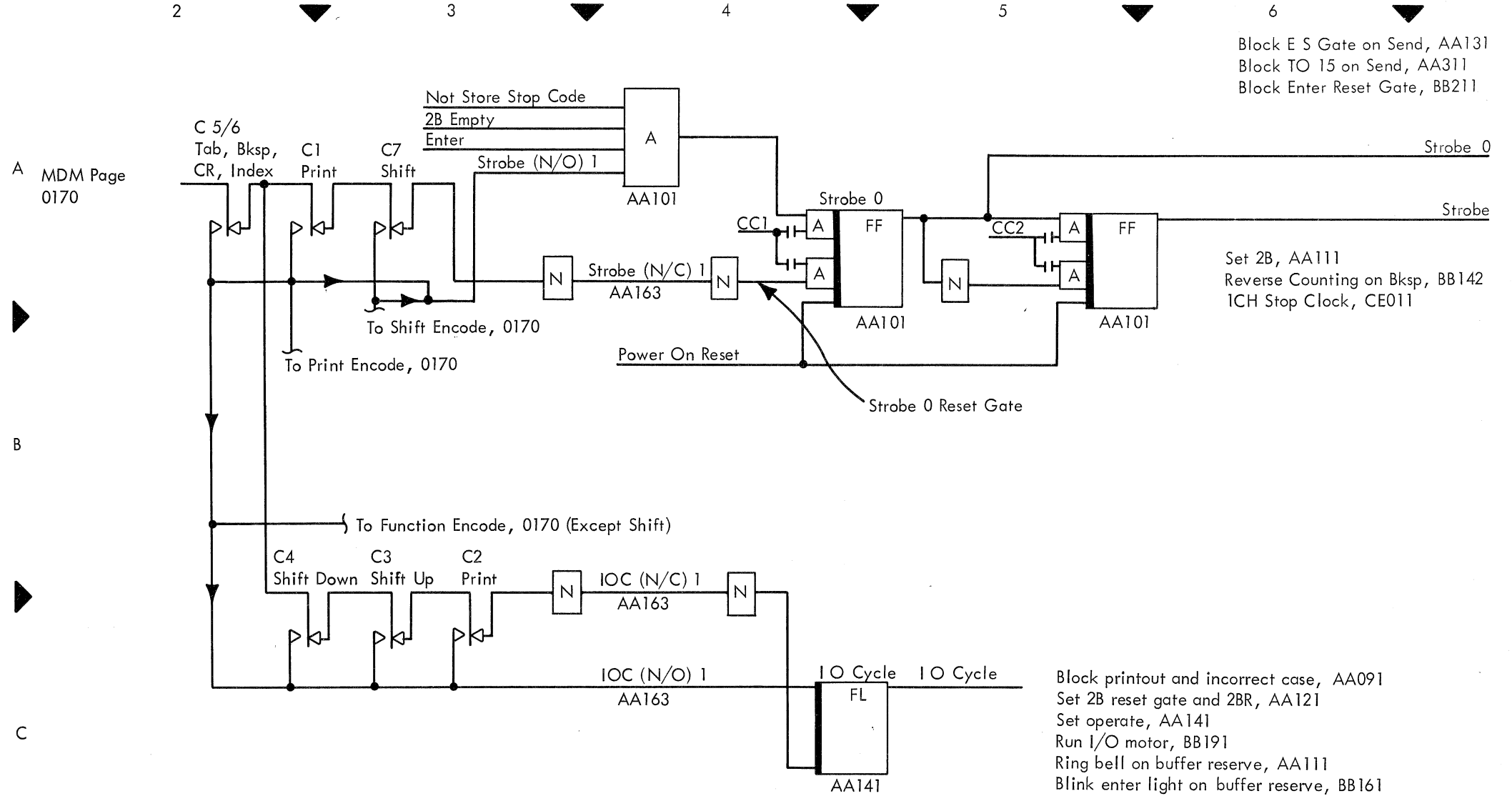
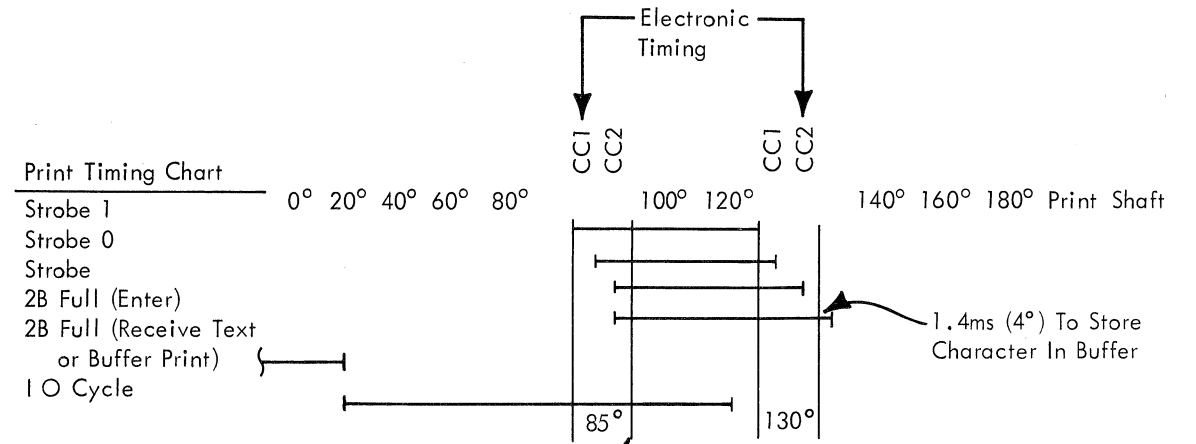


Figure FU-7. Strobe and I/O Cycle



Operation	Strobe 1	IOC 1
Print	85°-130°	20°-120°
Shift	100°-145°	35°-145°
Tab, Bksp	70°-115°	70°-115°
CR, Index	165°-300°	165°-300°

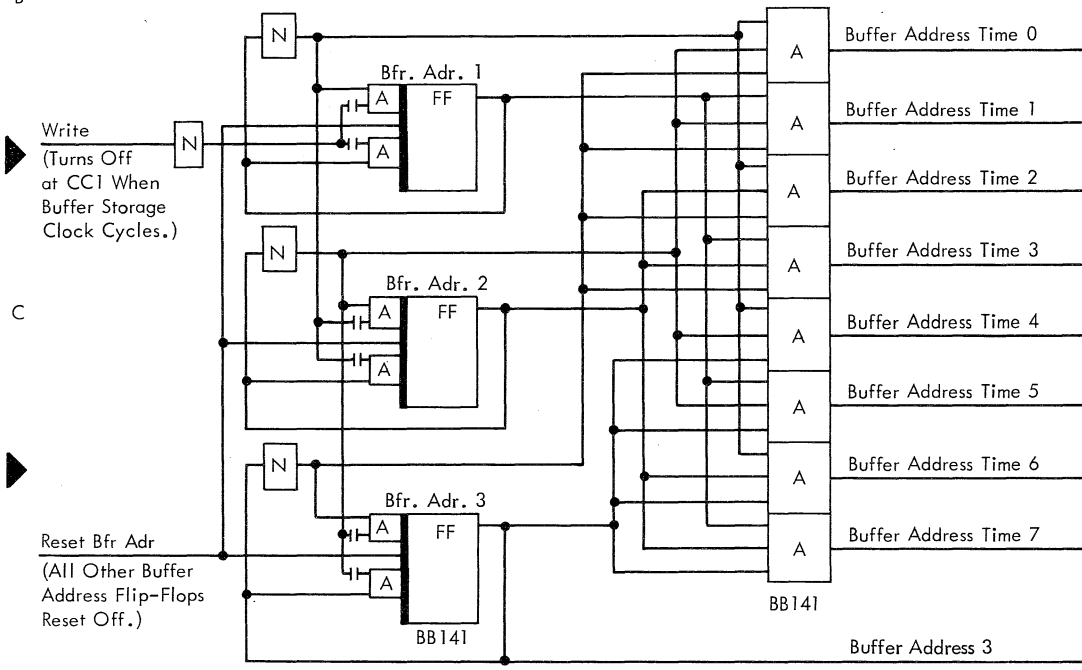


I/O Cycle causes 2B reset at this time. However, 2B is forced full by strobe and enter (FU-5.)

A

B

C

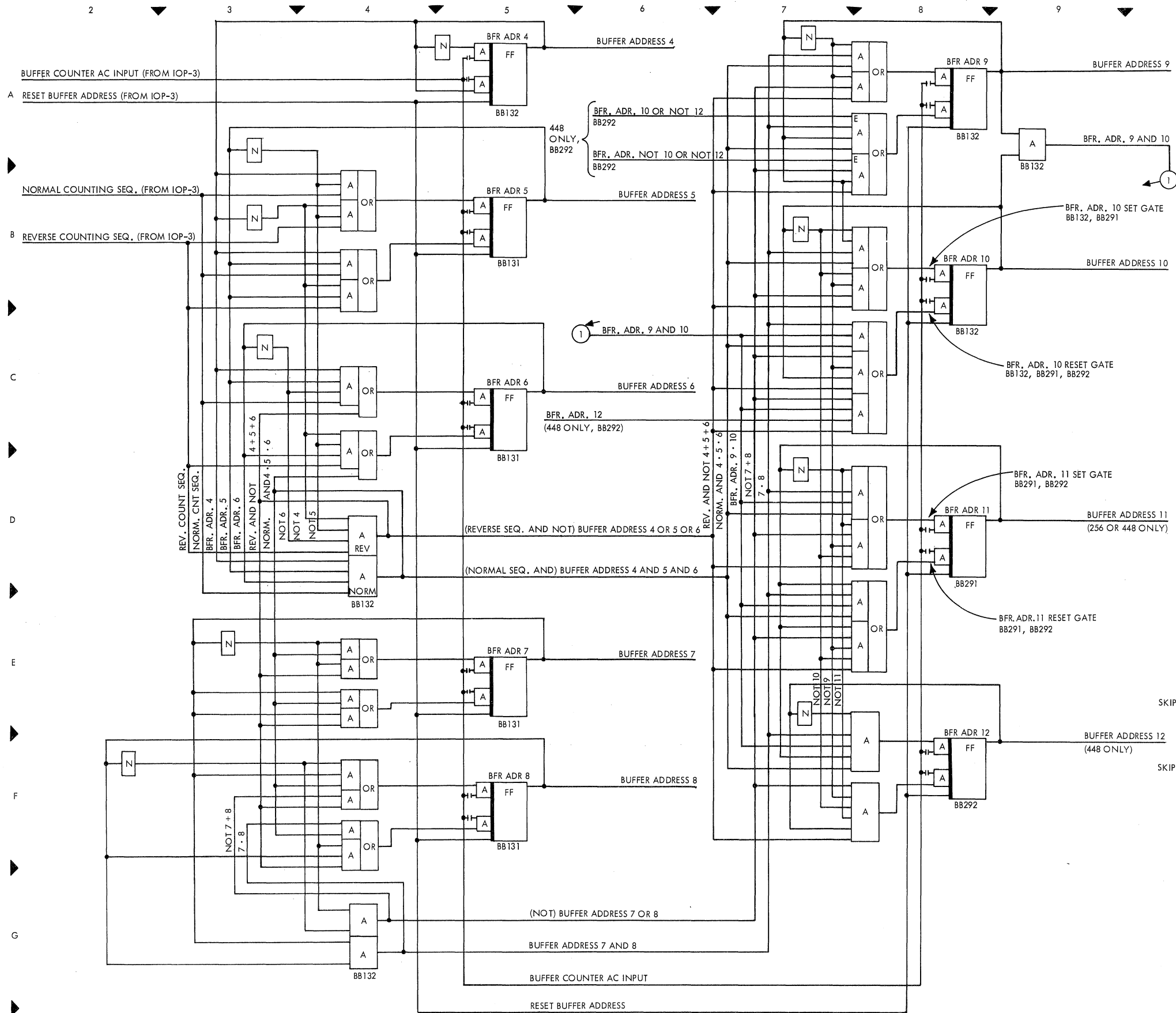


Character Cycle

Not - Write Pulse	BA3	BA2	BA1	Bfr. Adr. Time	1B or 2B Register
Reset	X	X	X	7	-
1				0	1
2			X	1	2
3		X		2	3
4		X	X	3	4
5	X			4	5
6	X		X	5	6
7	X	X		6	7
8	X	X	X	7	-

Figure FU-8. Bit Counter and Buffer Address Time Decode

Figure FU-9. Buffer Address Register



ADDRESS ADVANCE EXAMPLES, NORMAL AND REVERSE

DECIMAL COUNT	BUFFER ADDRESS											
	12	11	10	9	8	7	6	5	4	3	2	1
1	-	-	-	-	-	-	-	-	-	-	-	-
2	-	-	-	-	-	-	-	-	-	-	-	-
3	-	-	-	-	-	-	-	-	-	-	-	-
4	-	-	-	-	-	-	-	-	-	-	-	-
5	-	-	-	-	-	-	-	-	-	-	-	-
6-7	-	-	-	-	-	-	-	-	-	-	-	-
8	-	-	-	-	-	-	-	-	-	-	-	-
9	-	-	-	-	-	-	-	-	-	-	-	-
10-15	-	-	-	-	-	-	-	-	-	-	-	-
16	-	-	-	-	-	-	-	-	-	-	-	-
17	-	-	-	-	-	-	-	-	-	-	-	-
18-31	-	-	-	-	-	-	-	-	-	-	-	-
32	-	-	-	-	-	-	-	-	-	-	-	-
33	-	-	-	-	-	-	-	-	-	-	-	-
34-63	-	-	-	-	-	-	-	-	-	-	-	-
64	-	-	-	-	-	-	-	-	-	-	-	-
65	-	-	-	-	-	-	-	-	-	-	-	-
66-127	-	-	-	-	-	-	-	-	-	-	-	-
128	-	-	-	-	-	-	-	-	-	-	-	-
129	-	-	-	-	-	-	-	-	-	-	-	-
130-255	-	-	-	-	-	-	-	-	-	-	-	-
256	-	-	-	-	-	-	-	-	-	-	-	-
257	-	-	-	-	-	-	-	-	-	-	-	-
258-319	-	-	-	-	-	-	-	-	-	-	-	-
320	-	-	-	-	-	-	-	-	-	-	-	-
353	-	-	-	-	-	-	-	-	-	-	-	-
354-383	-	-	-	-	-	-	-	-	-	-	-	-
384	-	-	-	-	-	-	-	-	-	-	-	-
385	-	-	-	-	-	-	-	-	-	-	-	-
386-447	-	-	-	-	-	-	-	-	-	-	-	-
448	-	-	-	-	-	-	-	-	-	-	-	-
481	-	-	-	-	-	-	-	-	-	-	-	-
482-511	-	-	-	-	-	-	-	-	-	-	-	-
512	-	-	-	-	-	-	-	-	-	-	-	-
-32	-	-	-	-	-	-	-	-	-	-	-	-
-32	-	-	-	-	-	-	-	-	-	-	-	-
448 MAXIMUM CAPACITY	-	-	-	-	-	-	-	-	-	-	-	-

Figure FU-10. Garble and Time Out 15

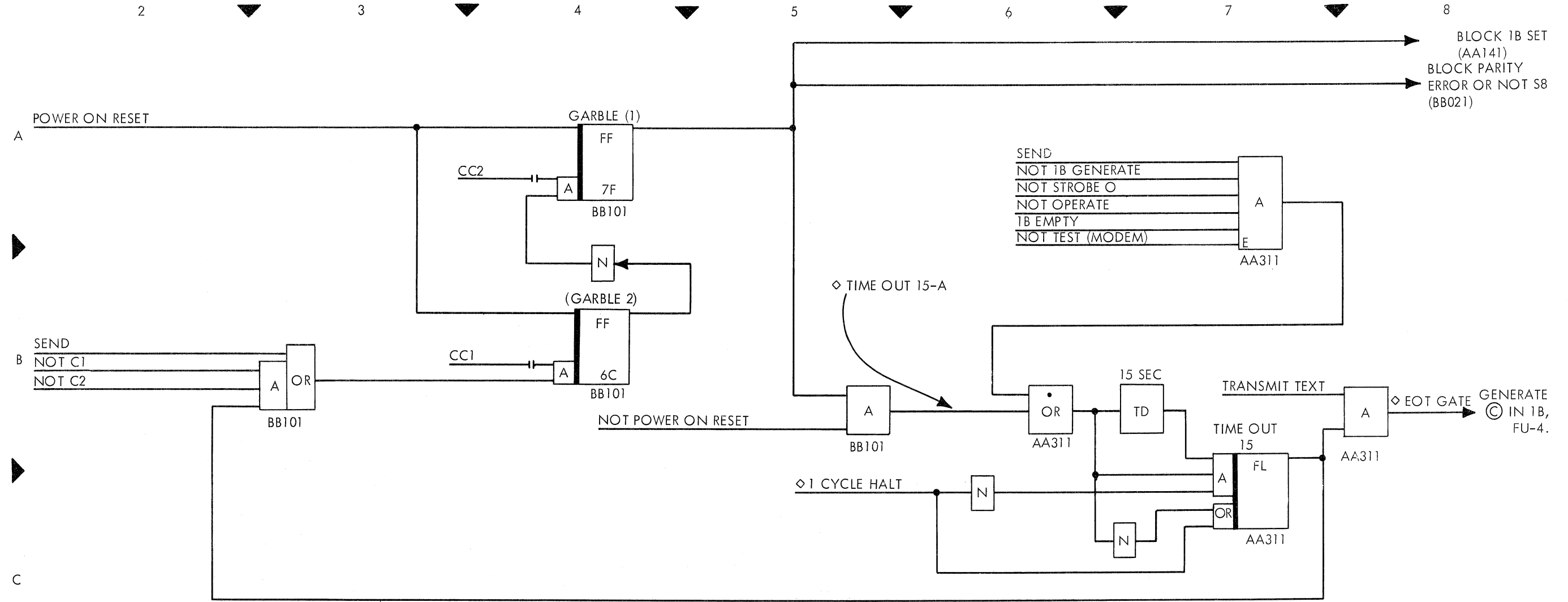
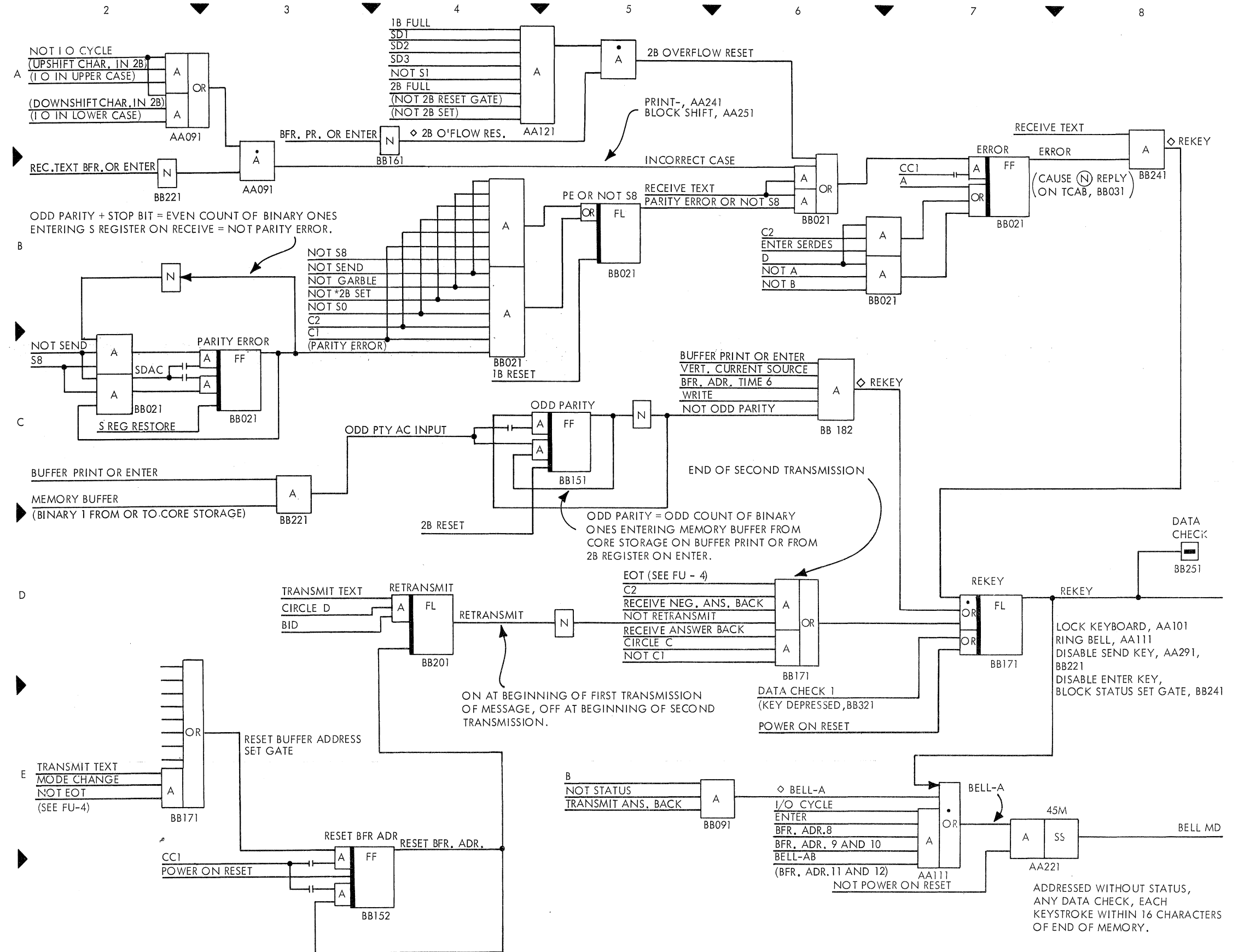


Figure FU-11. Data Check and Error



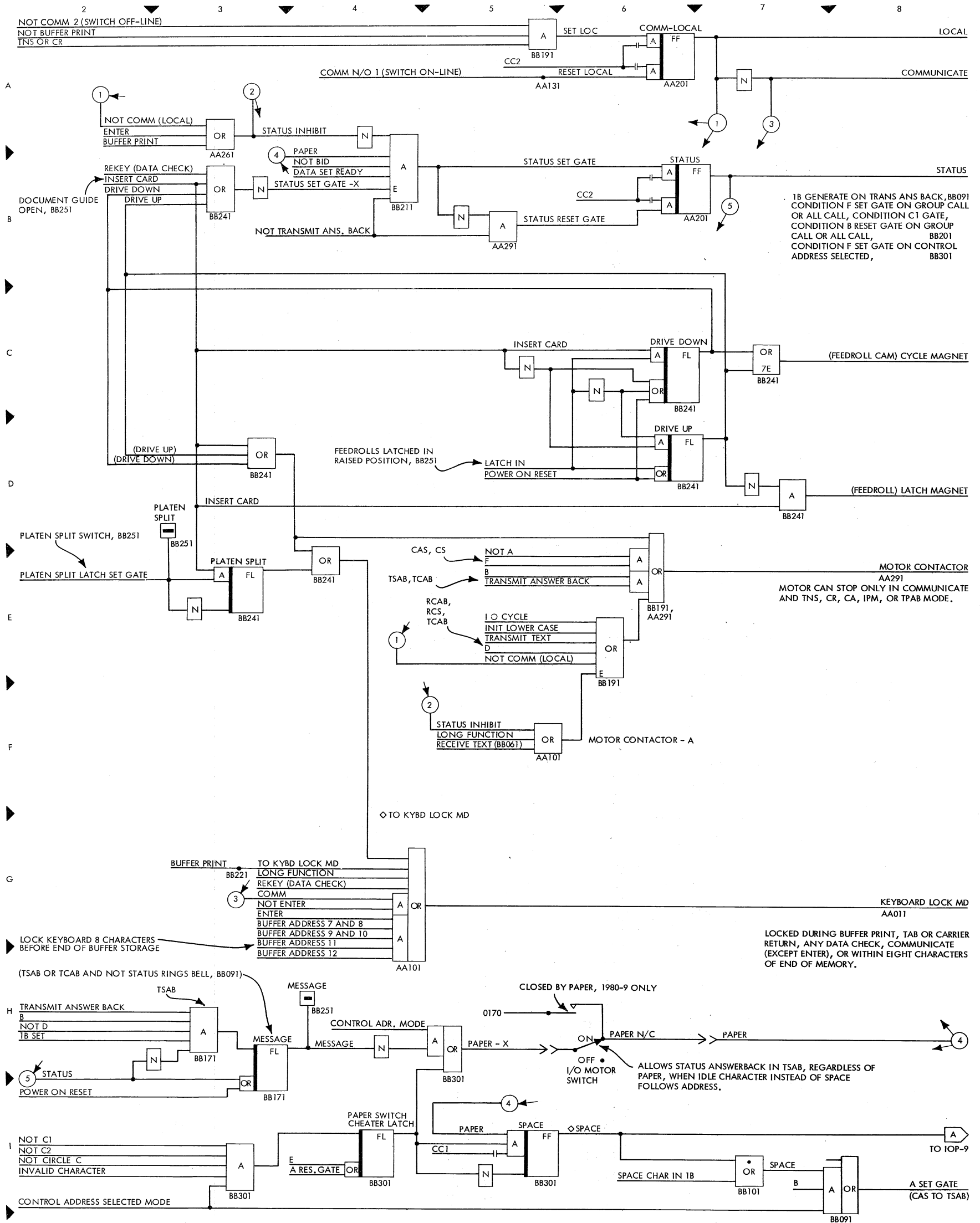
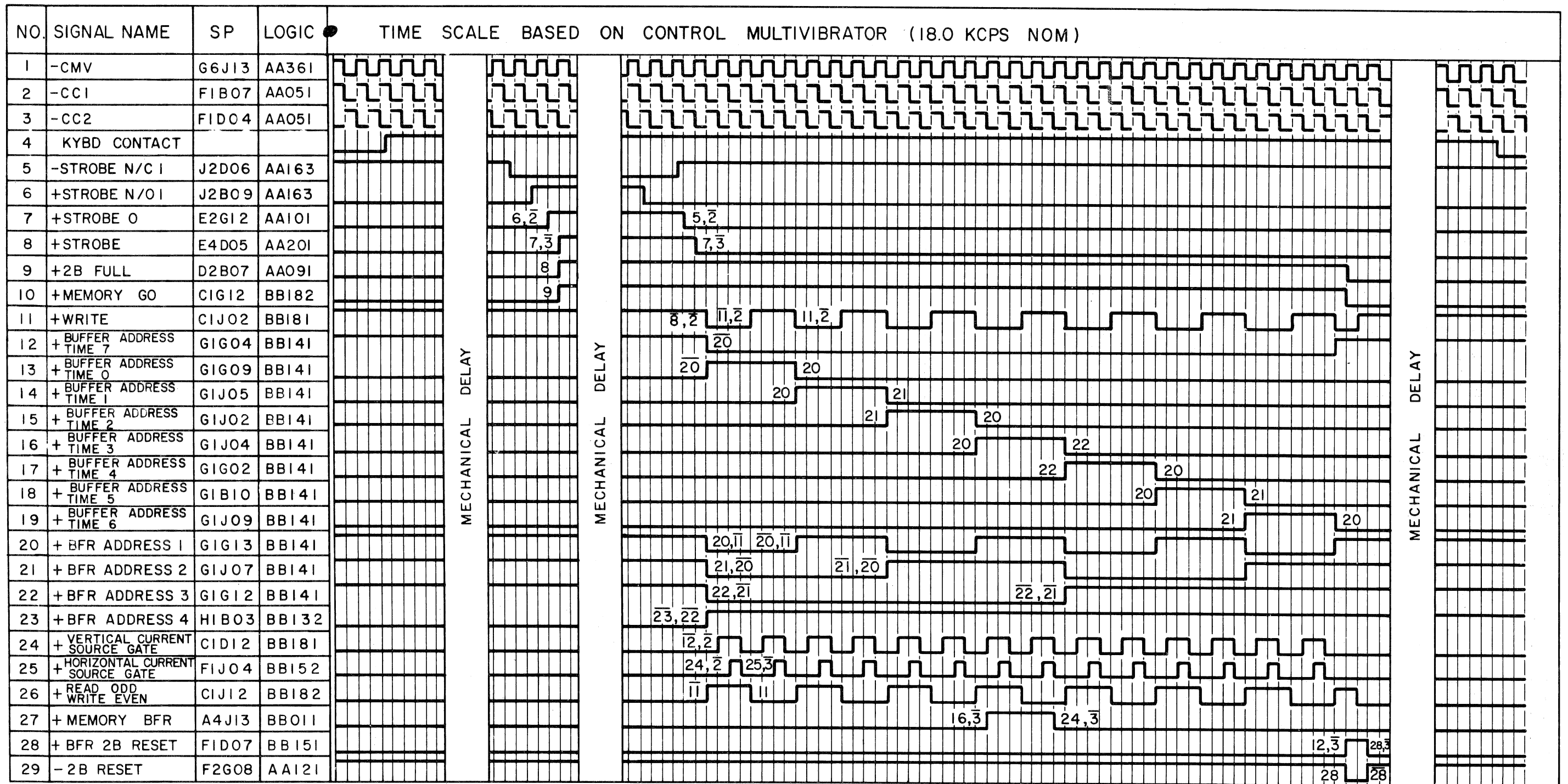


Figure FU-12. Local-Communicate, Status, and Document Insertion Circuits

Figure IOP-1. Enter (Sheet 3 of 3) Enter Numeral 4 from Keyboard to Memory



NOTE: IN THE ENTER MODE, TRANSFER A CHARACTER (NUMERAL 4) FROM KEYBOARD TO 2B, THEN FROM 2B TO MEMORY

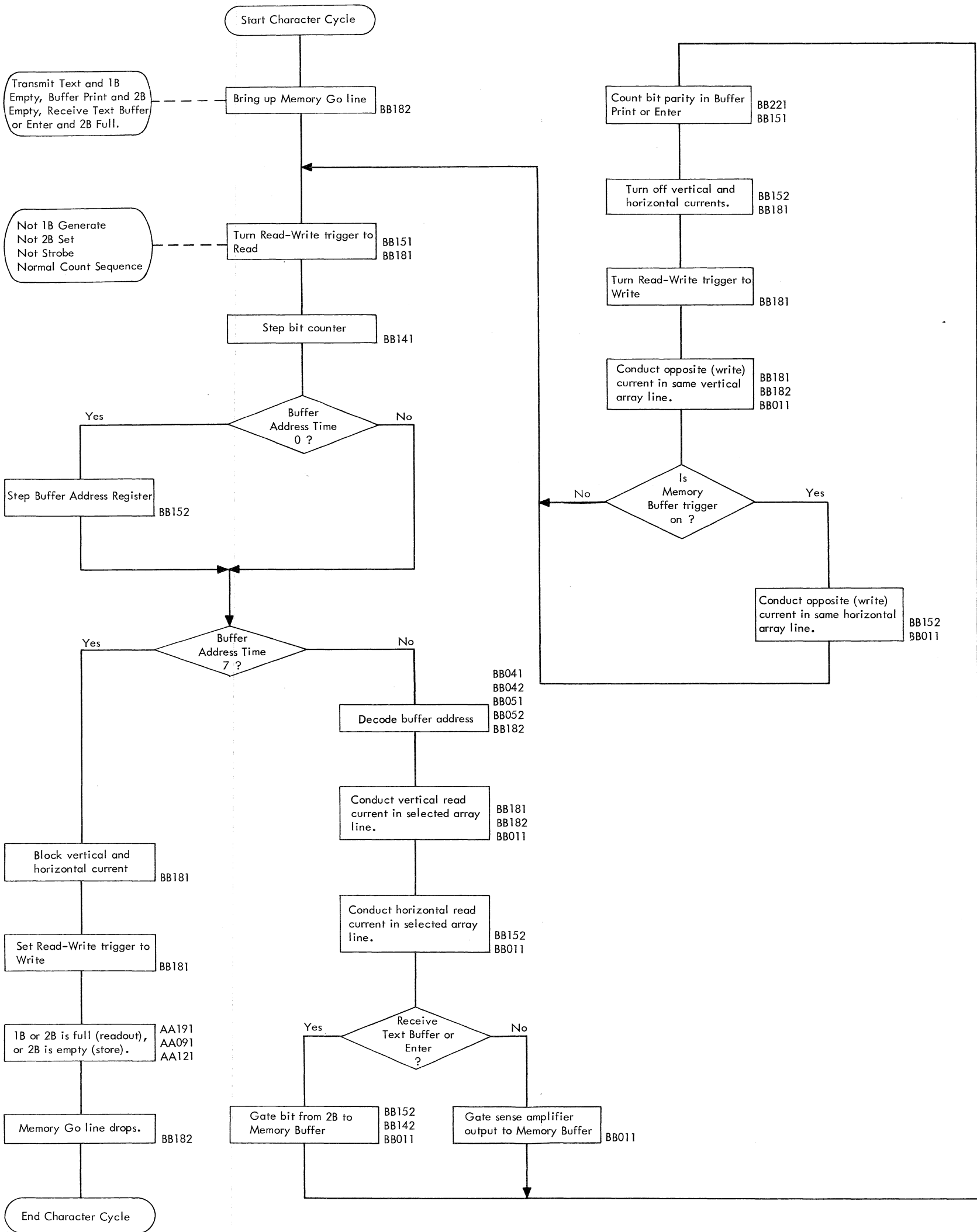
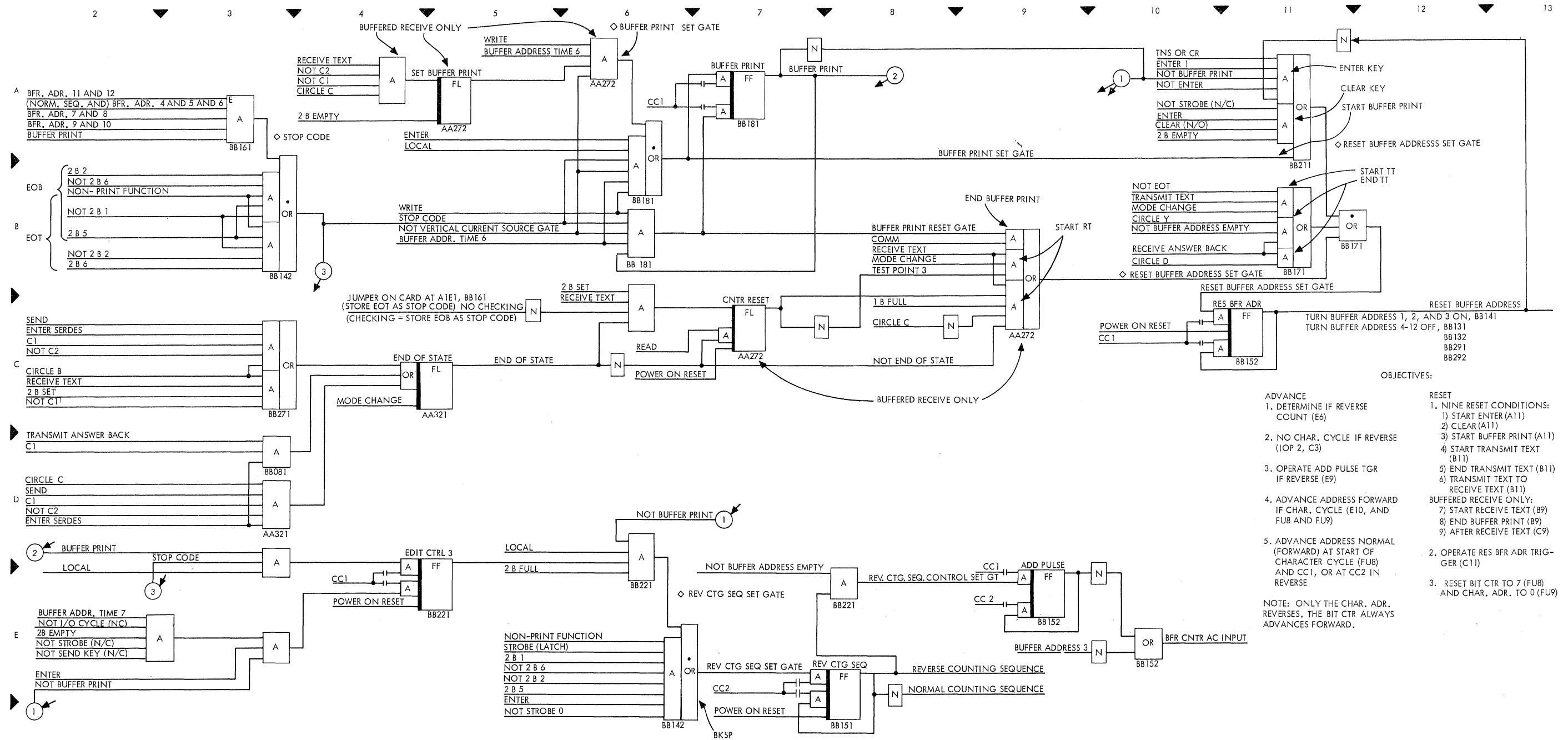


Figure IOP-2. Buffer Storage Operation (Sheet 1 of 2)

Figure IOP-3. Advance or Reset Buffer Storage Address (Normal or Reverse Sequence)



- OBJECTIVES:**
- | | |
|---|---|
| <p>ADVANCE</p> <ol style="list-style-type: none"> 1. DETERMINE IF REVERSE COUNT (E6) 2. NO CHAR. CYCLE IF REVERSE (IOP 2, C3) 3. OPERATE ADD PULSE TGR IF REVERSE (E9) 4. ADVANCE ADDRESS FORWARD IF CHAR. CYCLE (E10, AND FUB AND FU9) 5. ADVANCE ADDRESS NORMAL (FORWARD) AT START OF CHARACTER CYCLE (FU8) AND CC1, OR AT CC2 IN REVERSE | <p>RESET</p> <ol style="list-style-type: none"> 1. NINE RESET CONDITIONS: <ol style="list-style-type: none"> 1) START ENTER (A11) 2) CLEAR (A11) 3) START BUFFER PRINT (A11) 4) START TRANSMIT TEXT (B11) 5) END TRANSMIT TEXT (B11) 6) TRANSMIT TEXT TO RECEIVE TEXT (B11) 7) START RECEIVE TEXT (B9) 8) END BUFFER PRINT (B9) 9) AFTER RECEIVE TEXT (C9) 2. OPERATE RES BFR ADR TRIGGER (C11) 3. RESET BIT CTR TO 7 (FU8) AND CHAR. ADR. TO 0 (FU9) |
|---|---|
- NOTE: ONLY THE CHAR. ADR. REVERSES, THE BIT CTR ALWAYS ADVANCES FORWARD.**

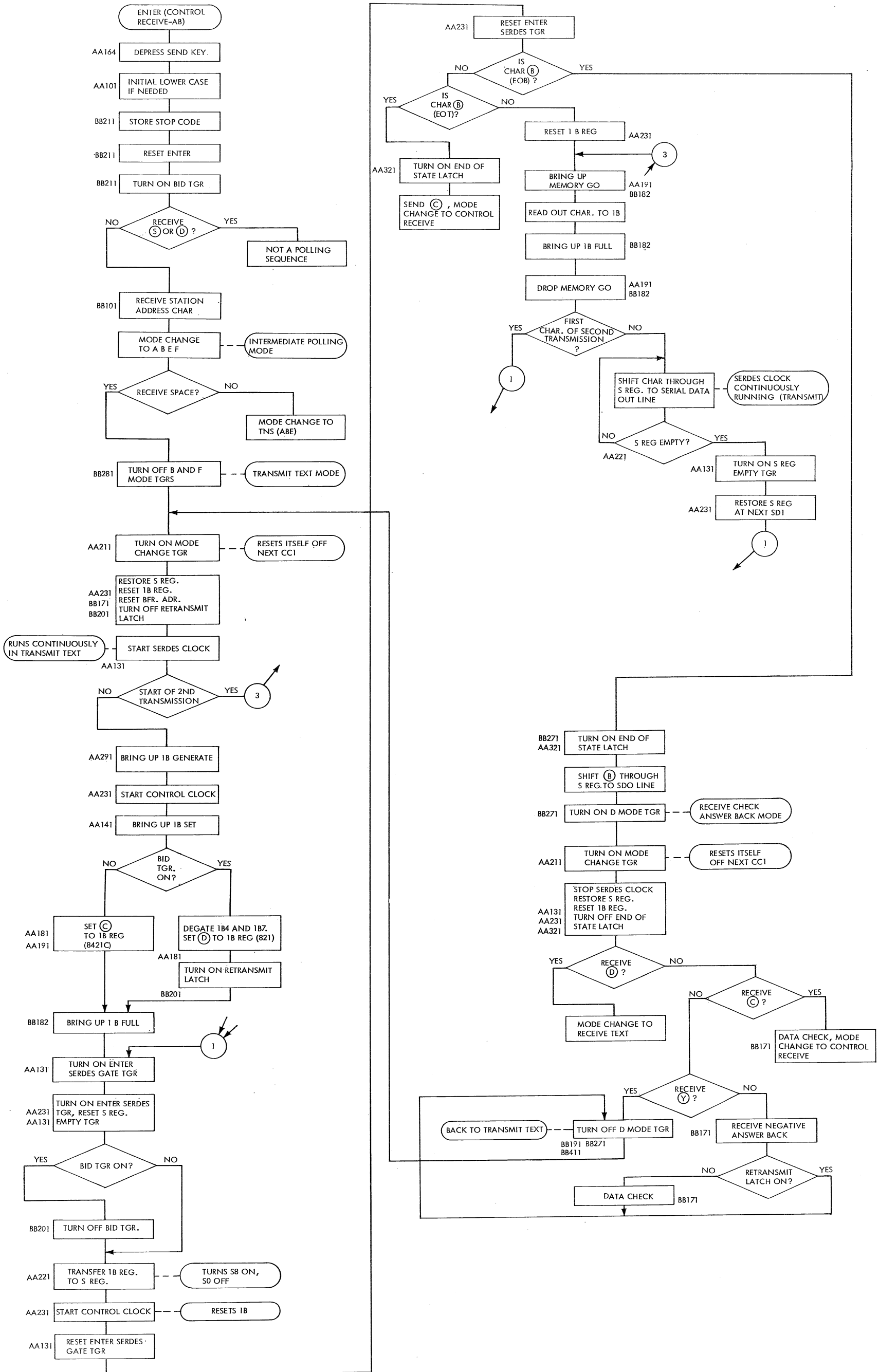
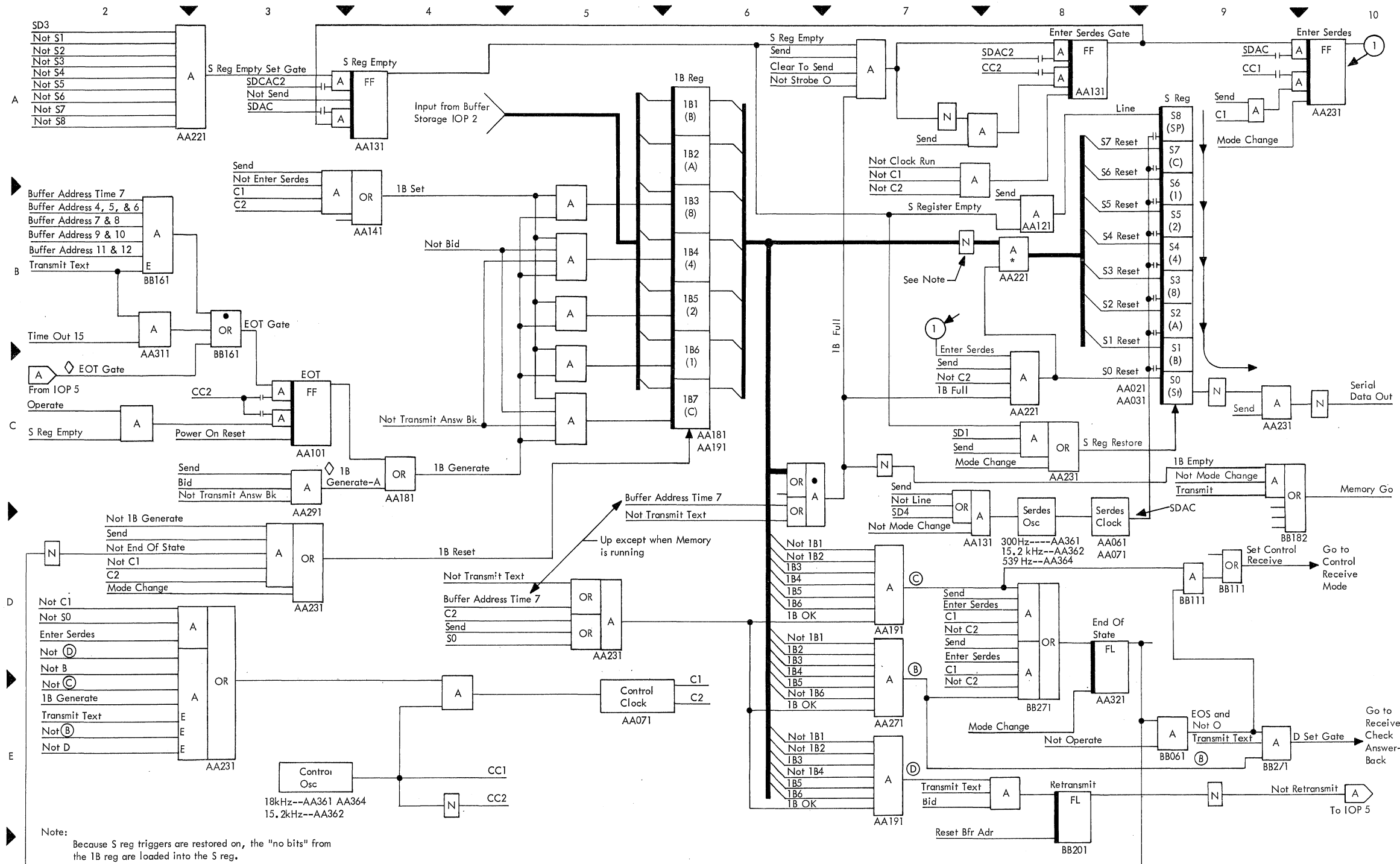


Figure IOP-4. Transmit (Sheet 1 of 3)

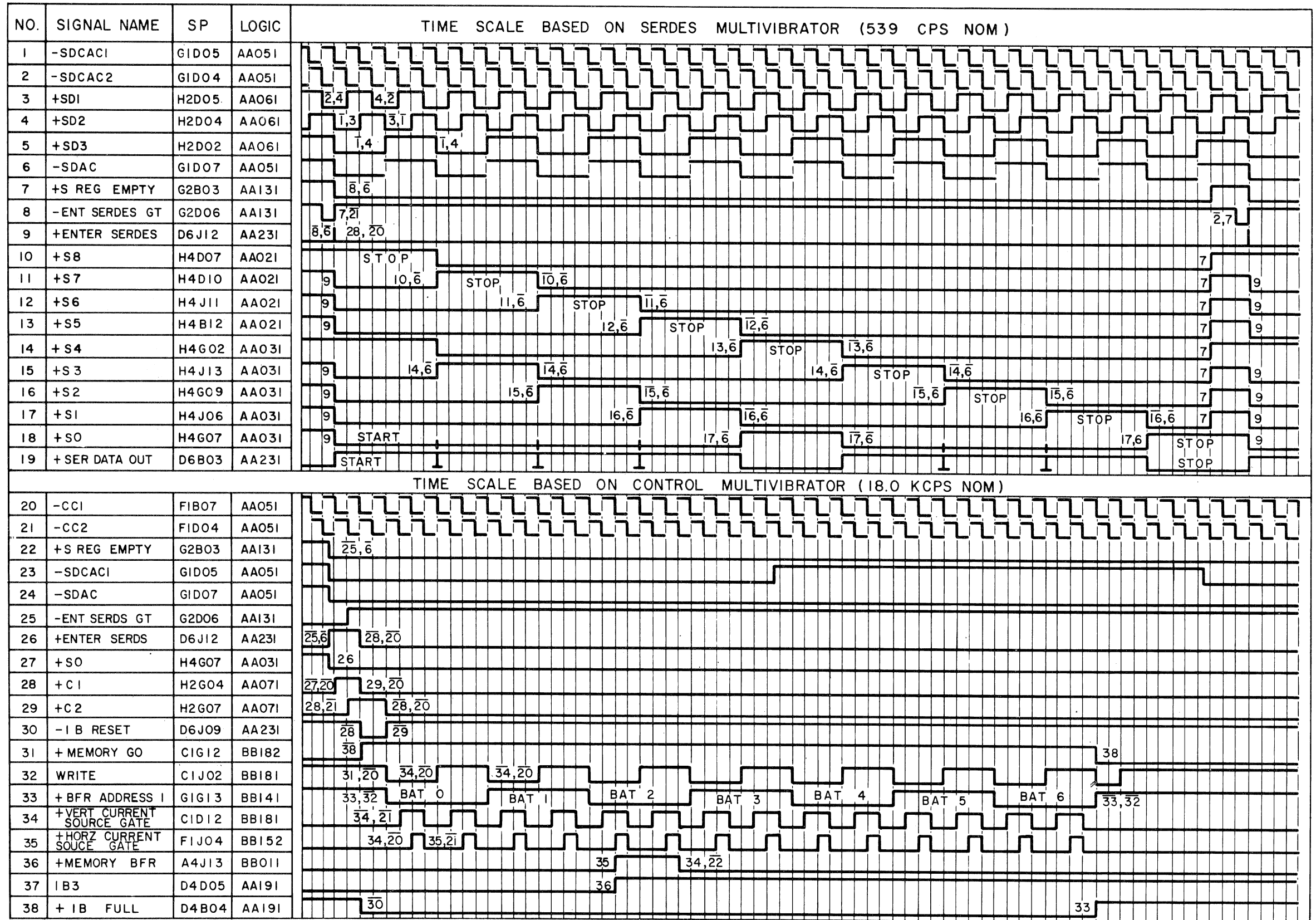
Figure IOP-4. Transmit (Sheet 2 of 3)



OBJECTIVES

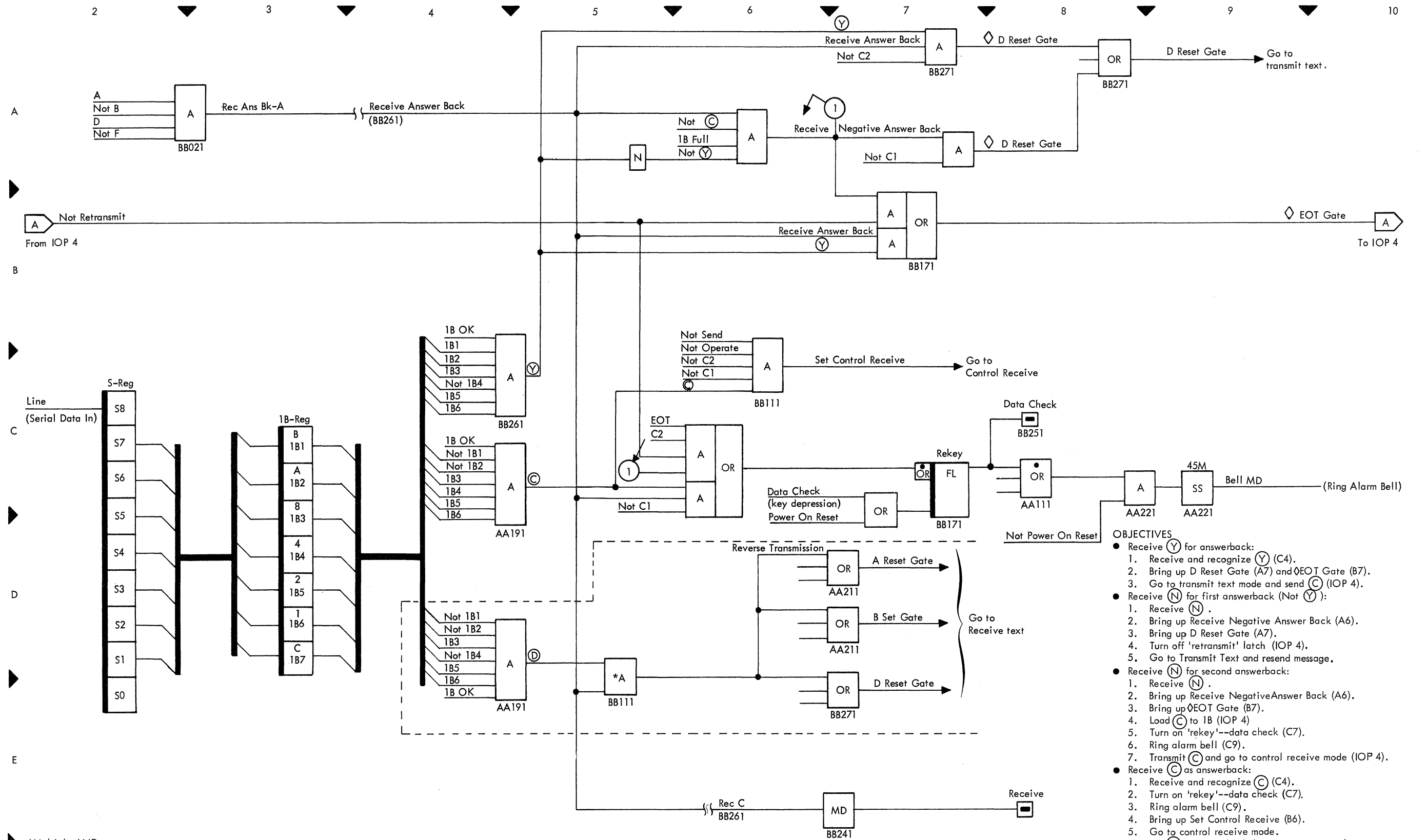
- Generate (D) (8, 2, 1, bits) after successful poll:
 1. Bring up 1B Generate (C4).
 2. Start control clock (E5).
 3. Bring up 1B Set (B4).
 4. Not Transmit Answer Back blocks set of '1B4' and '1B7' (C4).
 5. Turn on 'retransmit' (E8).
- Transfer character to S register:
 1. 'S register empty' turned on by Not Send (from previous mode) or when S register emptied following transmission of previous character (A4).
 2. Turn on 'enter serdes gate' and bring up S Register Restore (A8 and C8).
 3. Turn on 'enter serdes' (A 10).
 4. Bring up S0 Reset (B8).
- Transmit character:
 1. Serdes clock runs continuously during send operations (D8).
 2. Character is shifted to Serial Data Out line
- Reset 1B register:
 1. Start control clock (E5).
 2. Bring up 1B Reset (C3).
- Load 1B from buffer storage:
 1. Bring up Memory Go (C10).
 2. Scan character to 1B (IOP 2).
- Detect final character from memory (B):
 1. Recognize (D7).
 2. Turn on 'end of state' (D8).
 3. Prevent 1B Reset (D3).
 4. Go to receive check answer back (E9).
 5. Reset 1B during mode change (D3).
- Generate (C) if memory hangs up for 15 seconds, or end of memory is reached:
 1. Turn on 'EOT' (C3).
 2. Bring up 1B Generate (C4).
 3. Start control clock (E5).
 4. Bring up 1B Set (B4).
 5. Turn on '1B3', '1B4', '1B5', '1B6', and '1B7' latches (B5, C5)
 6. Go to control receive mode (D9).

Figure IOP-4. Transmit (Sheet 3 of 3) Transfer Character from Memory and Transmit



NOTE: TRANSFER CHARACTER (NUMERAL 4) FROM IB TO SERDES AND BEGIN TRANSMISSION, THEN READ FROM MEMORY (NUMERAL 8) AND STORE IN IB.

Figure IOP-5. Receive Check Answerback



*Multiple ANDs

- OBJECTIVES**
- Receive (Y) for answerback:
 1. Receive and recognize (Y) (C4).
 2. Bring up D Reset Gate (A7) and EOT Gate (B7).
 3. Go to transmit text mode and send (C) (IOP 4).
 - Receive (N) for first answerback (Not (Y)):
 1. Receive (N).
 2. Bring up Receive Negative Answer Back (A6).
 3. Bring up D Reset Gate (A7).
 4. Turn off 'retransmit' latch (IOP 4).
 5. Go to Transmit Text and resend message.
 - Receive (N) for second answerback:
 1. Receive (N).
 2. Bring up Receive Negative Answer Back (A6).
 3. Bring up EOT Gate (B7).
 4. Load (C) to 1B (IOP 4).
 5. Turn on 'rekey'--data check (C7).
 6. Ring alarm bell (C9).
 7. Transmit (C) and go to control receive mode (IOP 4).
 - Receive (C) as answerback:
 1. Receive and recognize (C) (C4).
 2. Turn on 'rekey'--data check (C7).
 3. Ring alarm bell (C9).
 4. Bring up Set Control Receive (B6).
 5. Go to control receive mode.
 - Receive (D) as answerback (reverse transmission):
 1. Receive and recognize (D) (D4).
 2. Bring up A Reset Gate, B Set Gate, and D Reset Gate (D7).
 3. Go to receive text mode.

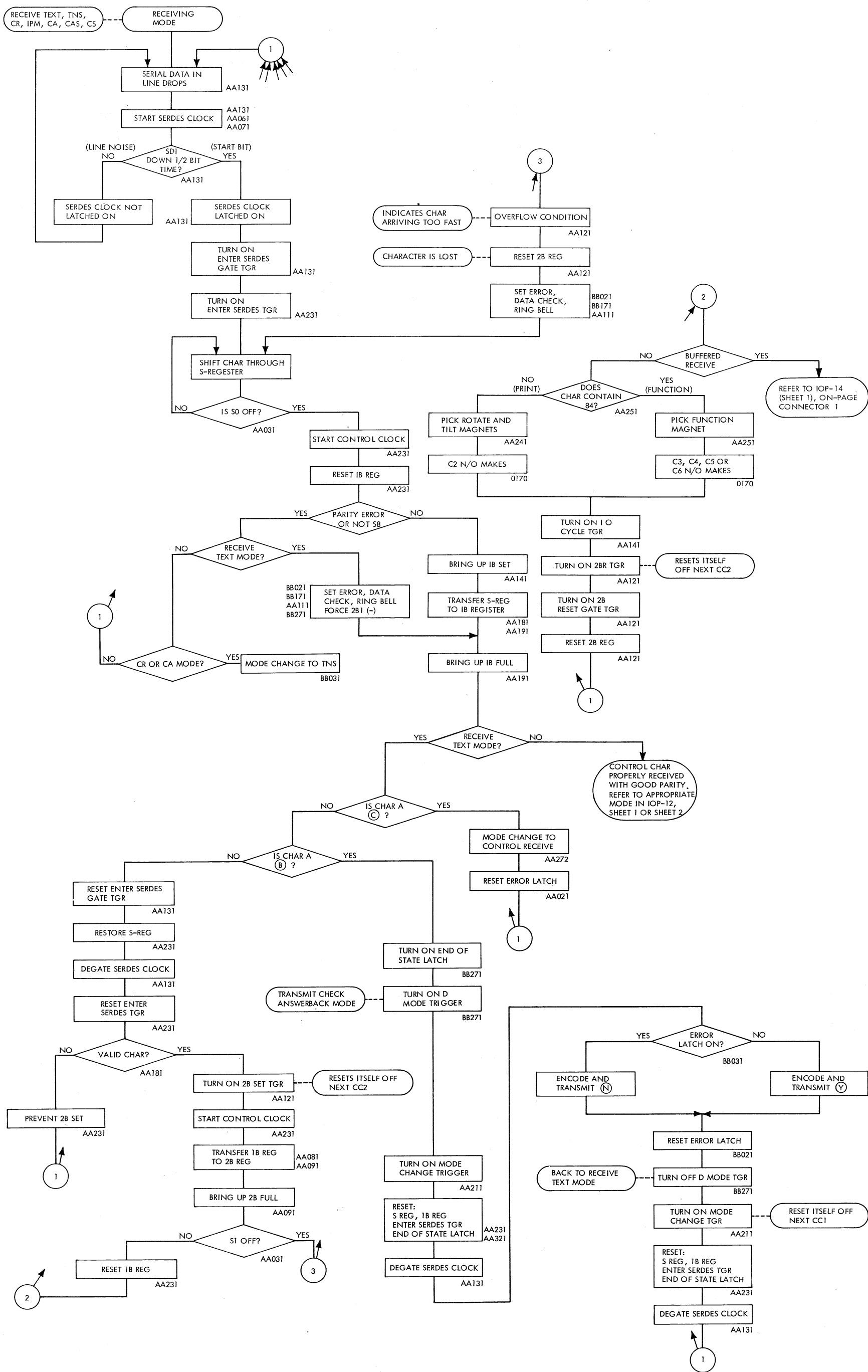
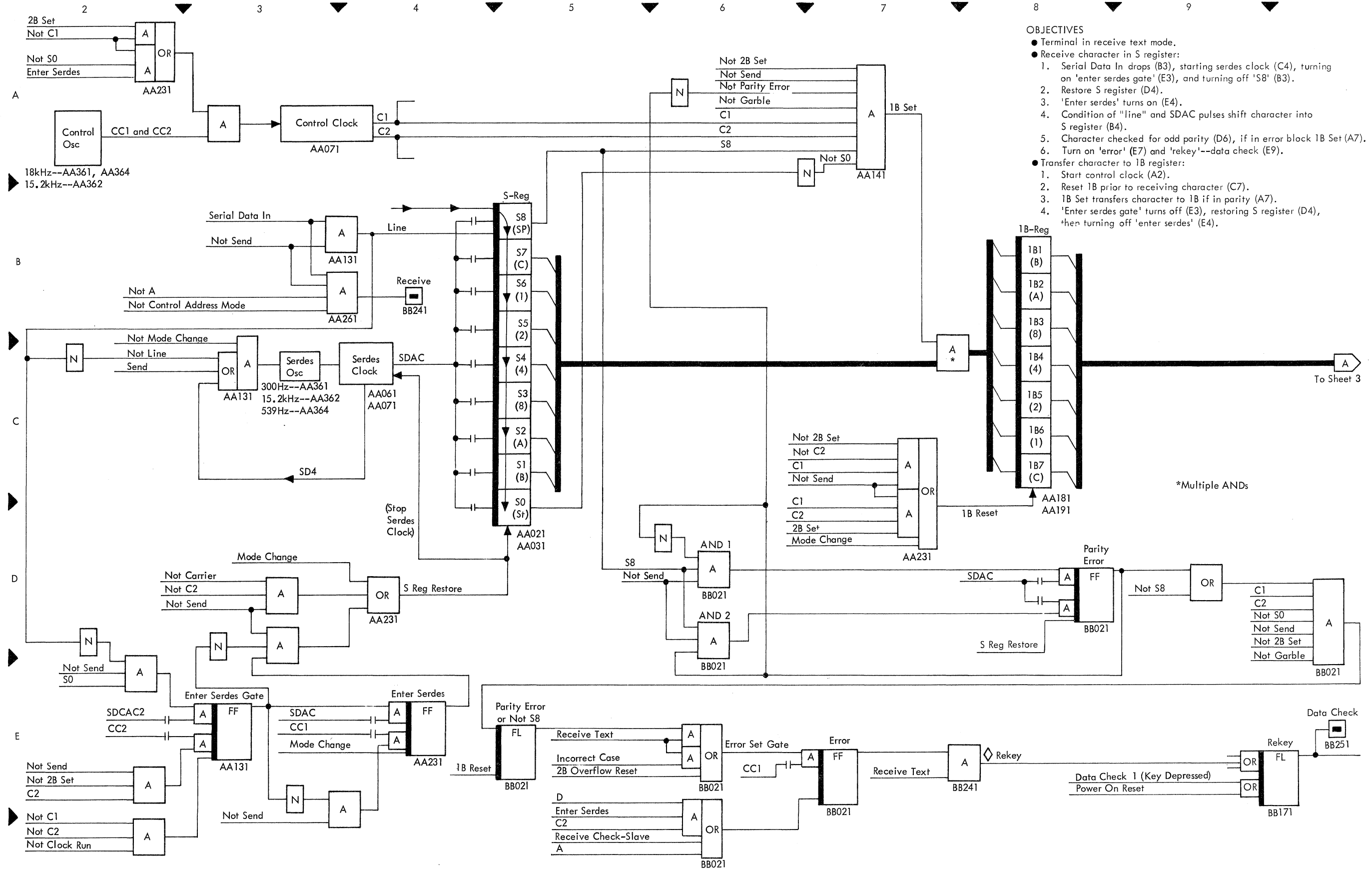


Figure IOP-6. Receive (Sheet 1 of 5)

Figure IOP-6. Receive (Sheet 2 of 5)

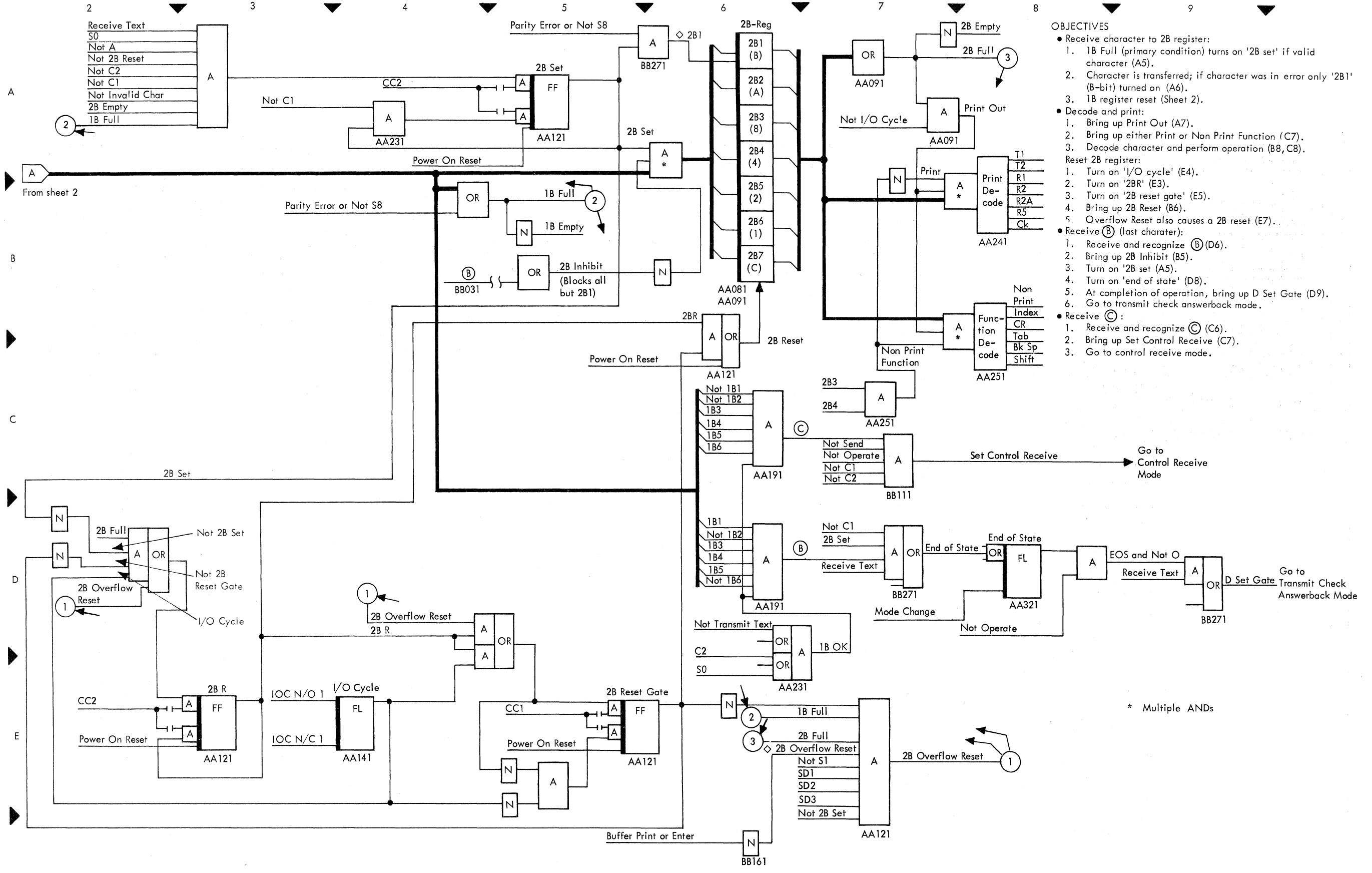


- OBJECTIVES**
- Terminal in receive text mode.
 - Receive character in S register:
 1. Serial Data In drops (B3), starting serdes clock (C4), turning on 'enter serdes gate' (E3), and turning off 'S8' (B3).
 2. Restore S register (D4).
 3. 'Enter serdes' turns on (E4).
 4. Condition of "line" and SDAC pulses shift character into S register (B4).
 5. Character checked for odd parity (D6), if in error block 1B Set (A7).
 6. Turn on 'error' (E7) and 'rekey'---data check (E9).
 - Transfer character to 1B register:
 1. Start control clock (A2).
 2. Reset 1B prior to receiving character (C7).
 3. 1B Set transfers character to 1B if in parity (A7).
 4. 'Enter serdes gate' turns off (E3), restoring S register (D4), then turning off 'enter serdes' (E4).

To Sheet 3

*Multiple ANDs

Figure IOP-6. Receive (Sheet 3 of 5)



- OBJECTIVES**
- Receive character to 2B register:
 - 1B Full (primary condition) turns on '2B set' if valid character (A5).
 - Character is transferred; if character was in error only '2B1' (B-bit) turned on (A6).
 - 1B register reset (Sheet 2).
 - Decode and print:
 - Bring up Print Out (A7).
 - Bring up either Print or Non Print Function (C7).
 - Decode character and perform operation (B8, C8).
 - Reset 2B register:
 - Turn on 'I/O cycle' (E4).
 - Turn on '2BR' (E3).
 - Turn on '2B reset gate' (E5).
 - Bring up 2B Reset (B6).
 - Overflow Reset also causes a 2B reset (E7).
 - Receive (B) (last character):
 - Receive and recognize (B) (D6).
 - Bring up 2B Inhibit (B5).
 - Turn on '2B set' (A5).
 - Turn on 'end of state' (D8).
 - At completion of operation, bring up D Set Gate (D9).
 - Go to transmit check answerback mode.
 - Receive (C):
 - Receive and recognize (C) (C6).
 - Bring up Set Control Receive (C7).
 - Go to control receive mode.

* Multiple ANDs

Figure IOP-6. Receive (Sheet 4 of 5) Deserialize Character and Transfer to 1B Register

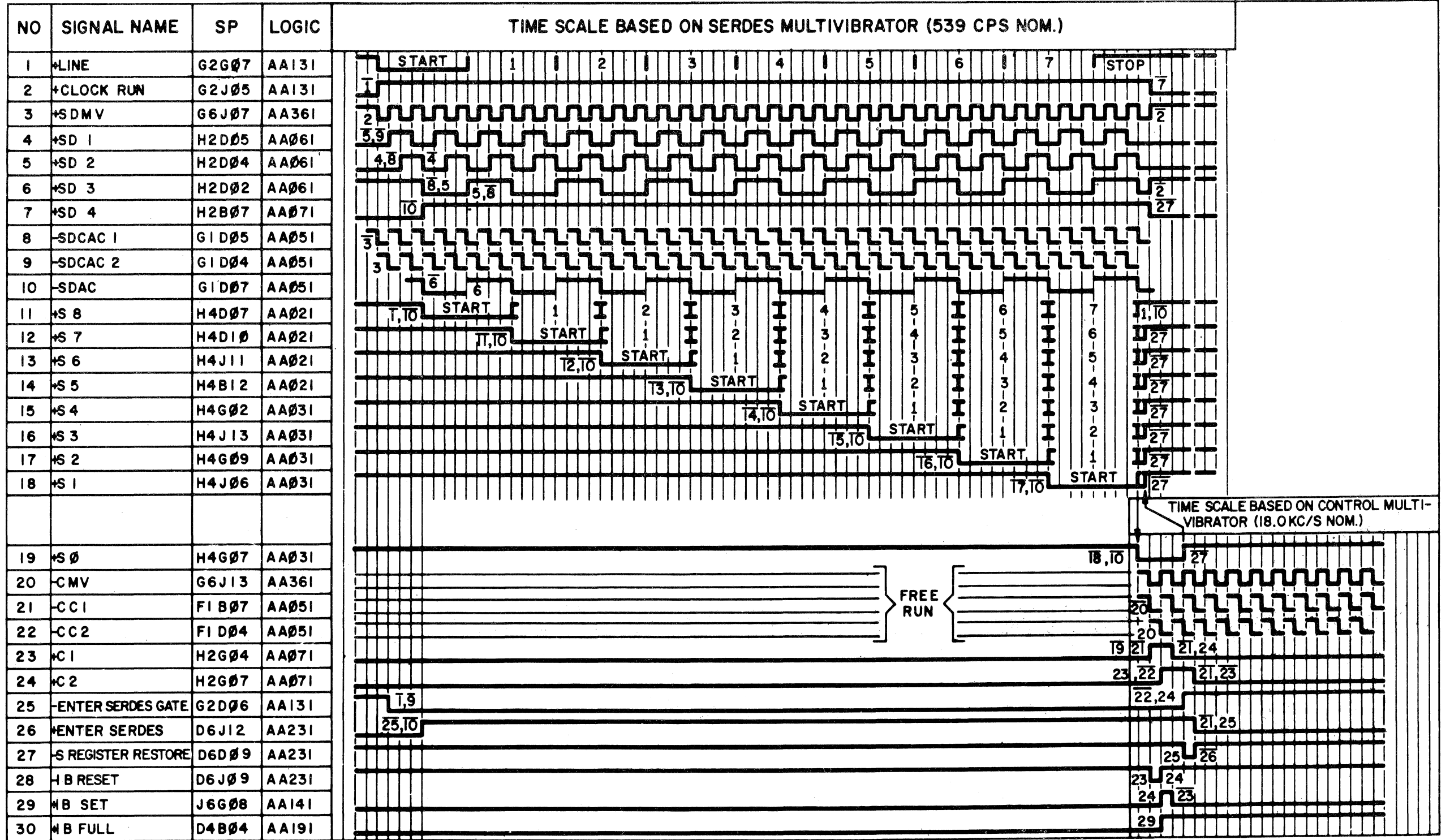
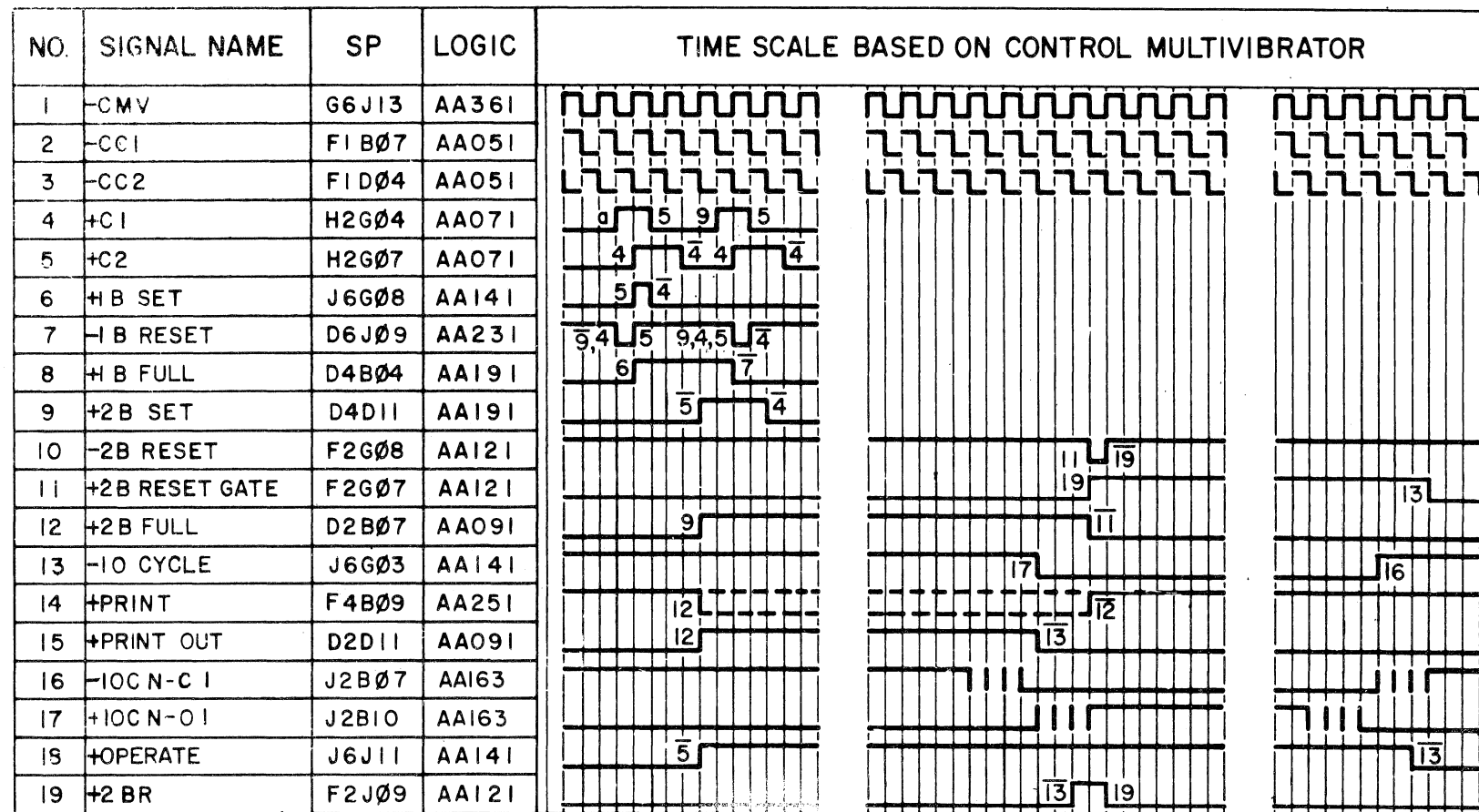


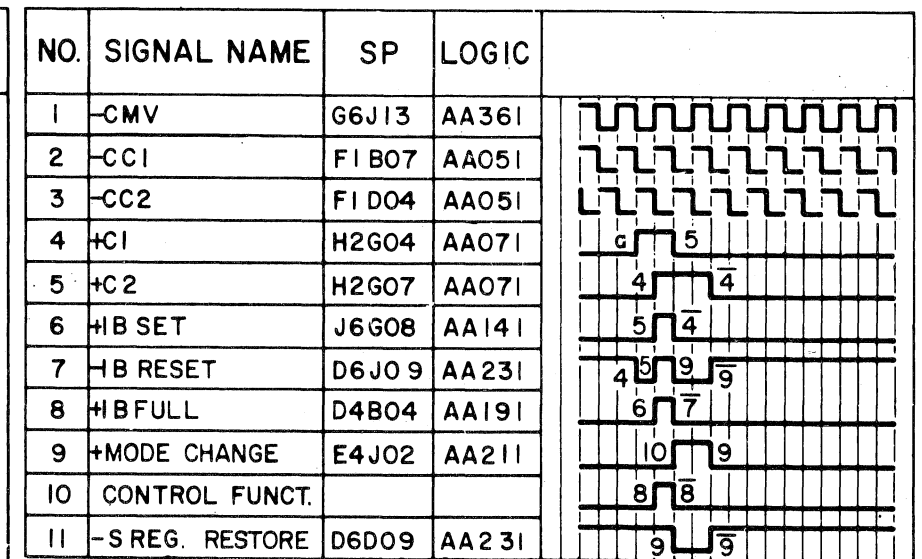
Figure IOP-6. Receive (Sheet 5 of 5)

NOTE: TRANSFER A CHARACTER FROM 1B TO 2B AND PRINT IN THE RECEIVE MODE

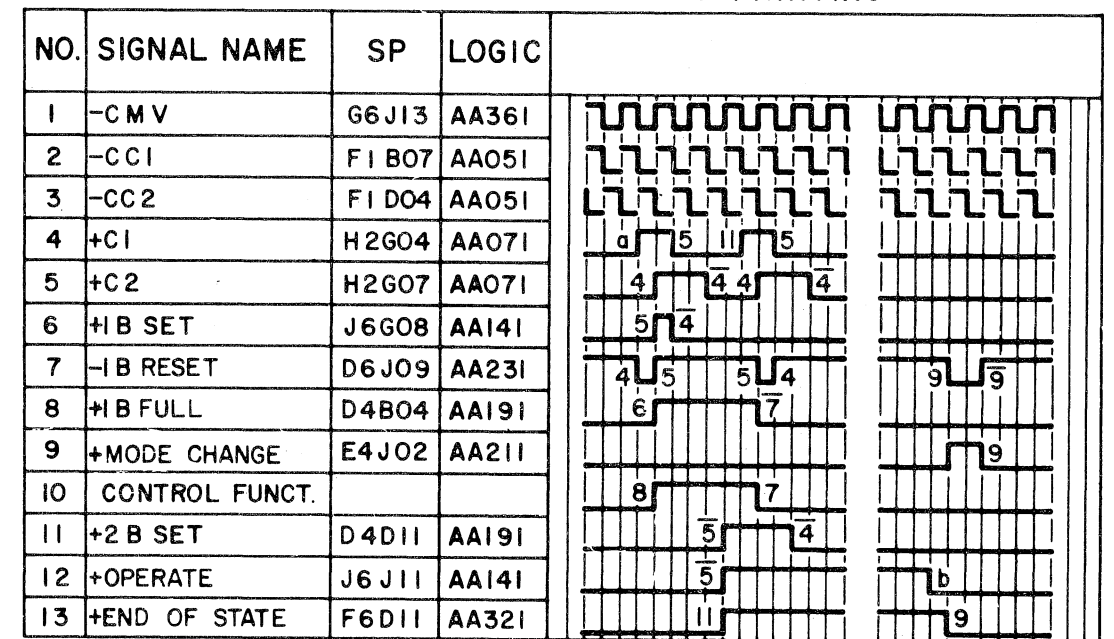


a. THE FINAL GATE CONDITION FOR CI IS - S Ø

NOTE: CHANGE MODES ON RECEIPT OF A CONTROL CHARACTER WITHOUT PRINTING

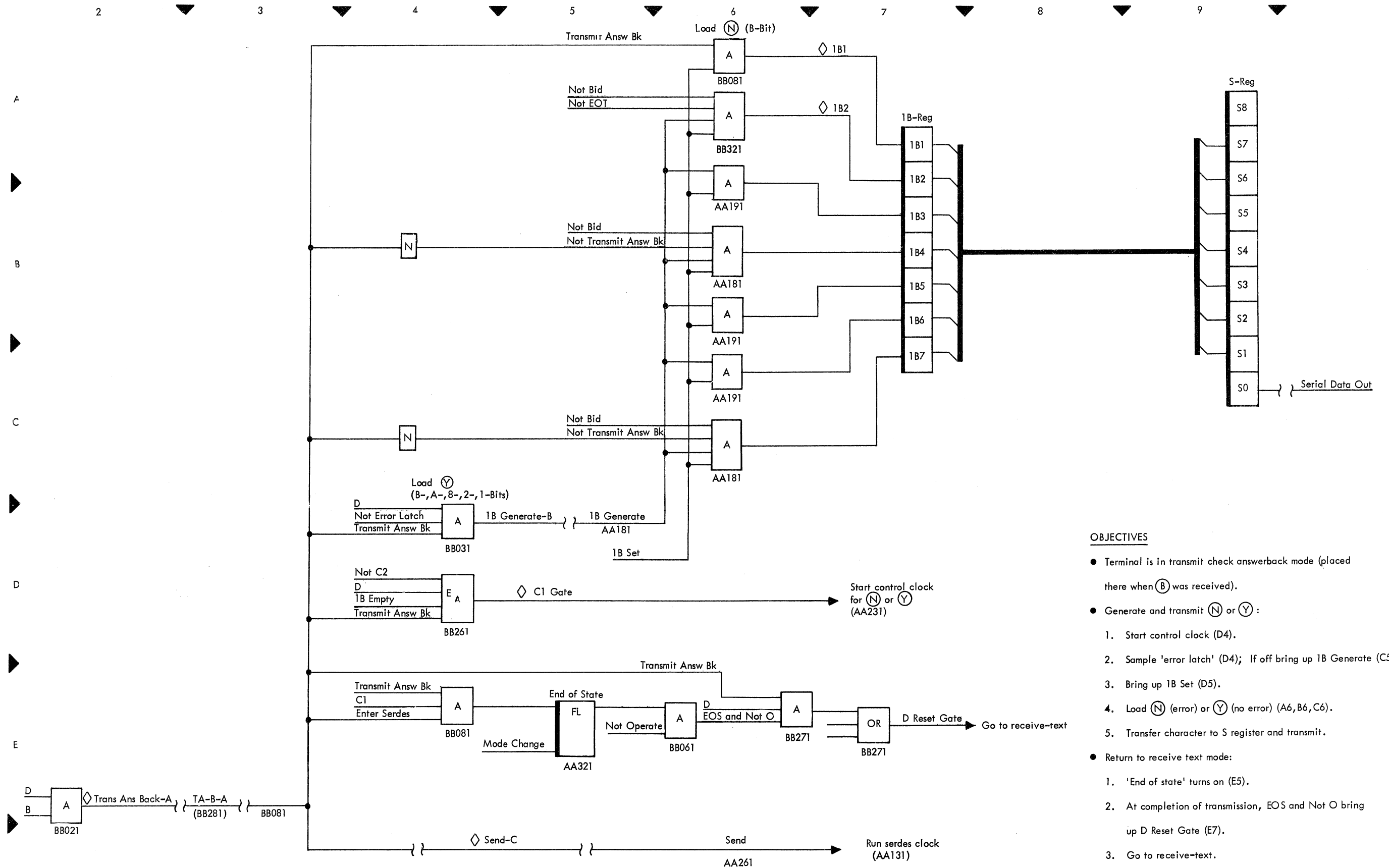


NOTE: CHANGE MODES ON RECEIPT OF A CONTROL CHARACTER AFTER PRINTING



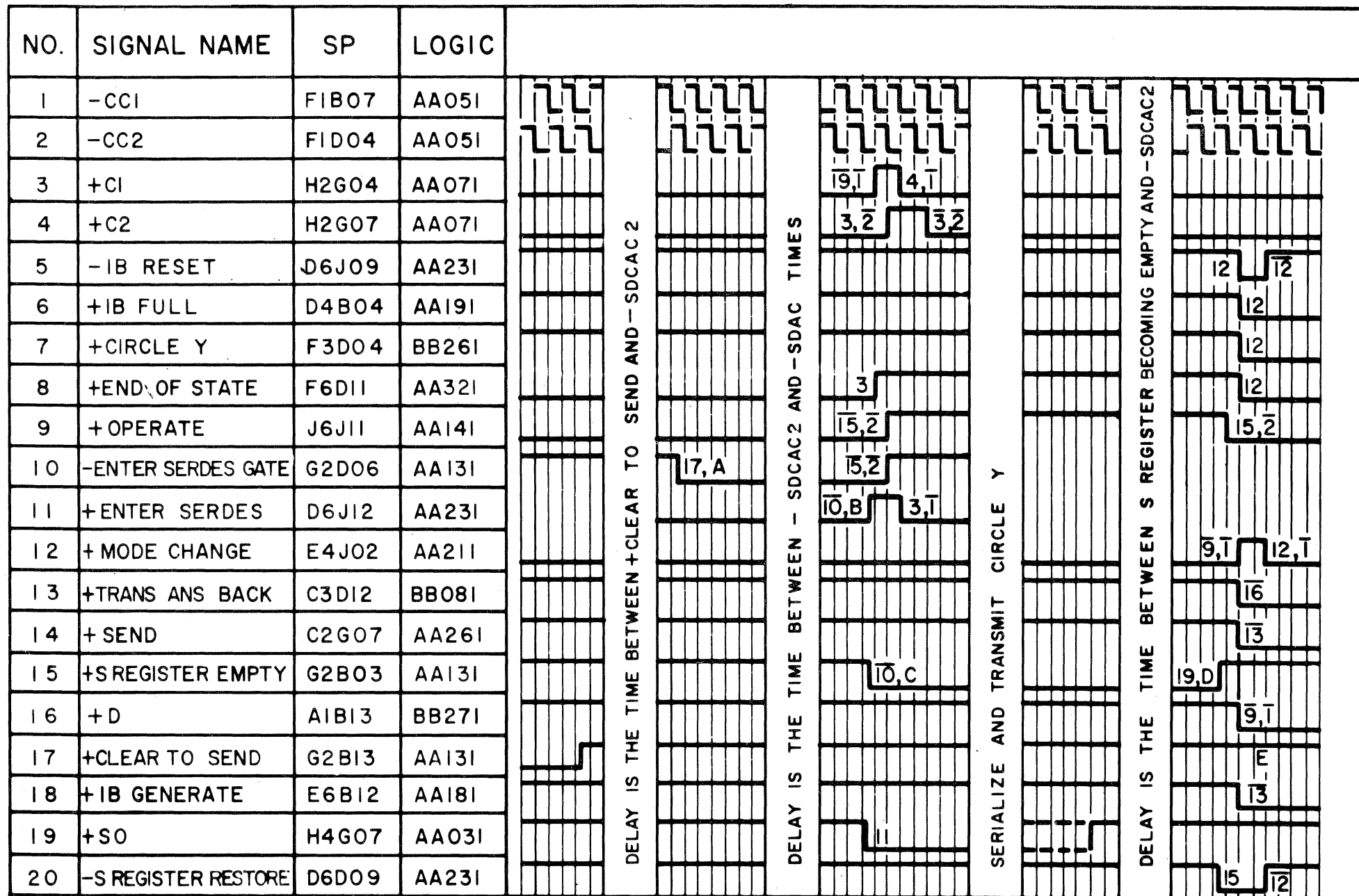
b. 10 CYCLE GOING TO ZERO IS THE FINAL GATING CONDITION ALLOWING OPERATE TO BE RESET BY CC2

Figure IOP-7. Transmit Check Answerback (Sheet 1 of 2)



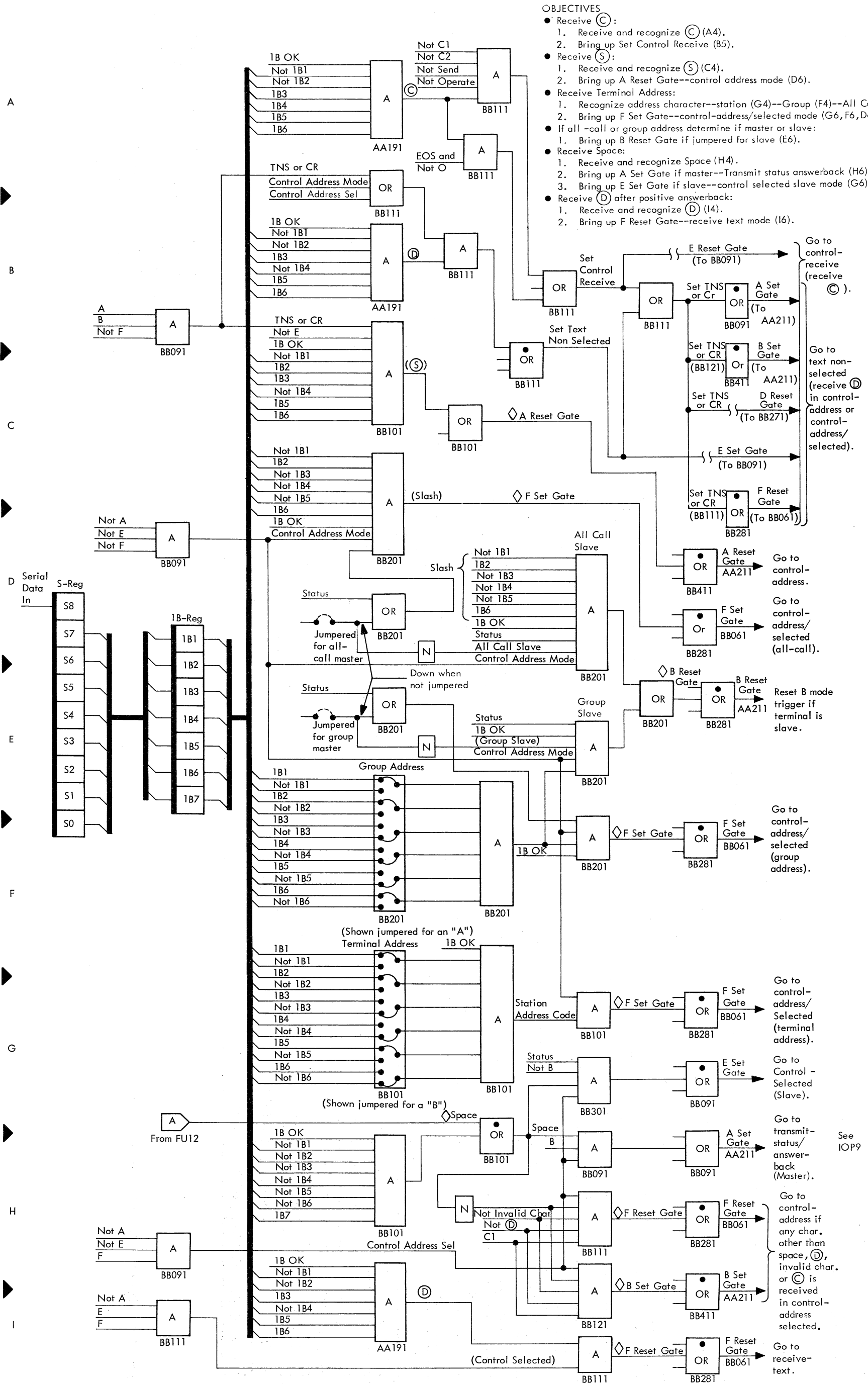
OBJECTIVES

- Terminal is in transmit check answerback mode (placed there when (B) was received).
- Generate and transmit (N) or (Y) :
 1. Start control clock (D4).
 2. Sample 'error latch' (D4); If off bring up 1B Generate (C5).
 3. Bring up 1B Set (D5).
 4. Load (N) (error) or (Y) (no error) (A6, B6, C6).
 5. Transfer character to S register and transmit.
- Return to receive text mode:
 1. 'End of state' turns on (E5).
 2. At completion of transmission, EOS and Not O bring up D Reset Gate (E7).
 3. Go to receive-text.



TRANSMIT A (Y) IN TRANSMIT CHECK ANSWER BACK, AND CHANGE MODES TO RECEIVE TEXT.

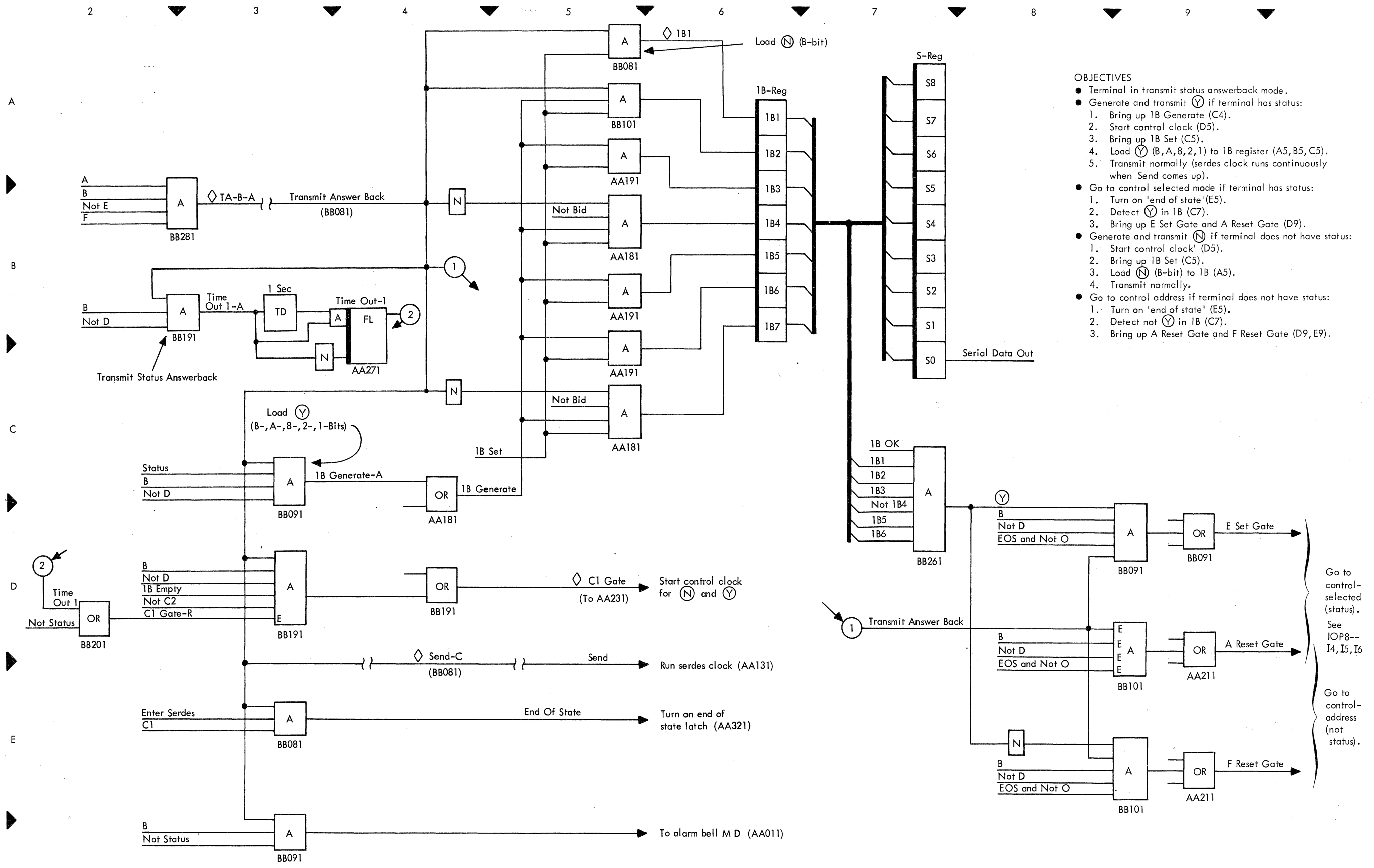
- A. -ENTER SERDES GATE IS SET BY -SDAC 2.
- B. +ENTER SERDES IS SET BY -SDAC.
- C. +S REGISTER EMPTY IS SET BY -SDAC.
- D. +S REGISTER EMPTY IS SET BY -SDCAC2
- E. -SEND WILL CAUSE CLEAR TO SEND TO FALL BUT IT WILL BE DELAYED.



- OBJECTIVES
- Receive (C):
 1. Receive and recognize (C) (A4).
 2. Bring up Set Control Receive (B5).
 - Receive (S):
 1. Receive and recognize (S) (C4).
 2. Bring up A Reset Gate--control address mode (D6).
 - Receive Terminal Address:
 1. Recognize address character--station (G4)--Group (F4)--All Call (C4).
 2. Bring up F Set Gate--control-address/selected mode (G6, F6, D6).
 - If all -call or group address determine if master or slave:
 1. Bring up B Reset Gate if jumpered for slave (E6).
 - Receive Space:
 1. Receive and recognize Space (H4).
 2. Bring up A Set Gate if master--Transmit status answerback (H6).
 3. Bring up E Set Gate if slave--control selected slave mode (G6).
 - Receive (D) after positive answerback:
 1. Receive and recognize (D) (I4).
 2. Bring up F Reset Gate--receive text mode (I6).

Figure IOP-8. Receive Addressing Character Sequence (Master or Slave)

Figure IOP-9. Addressing, Transmit Status Answerback

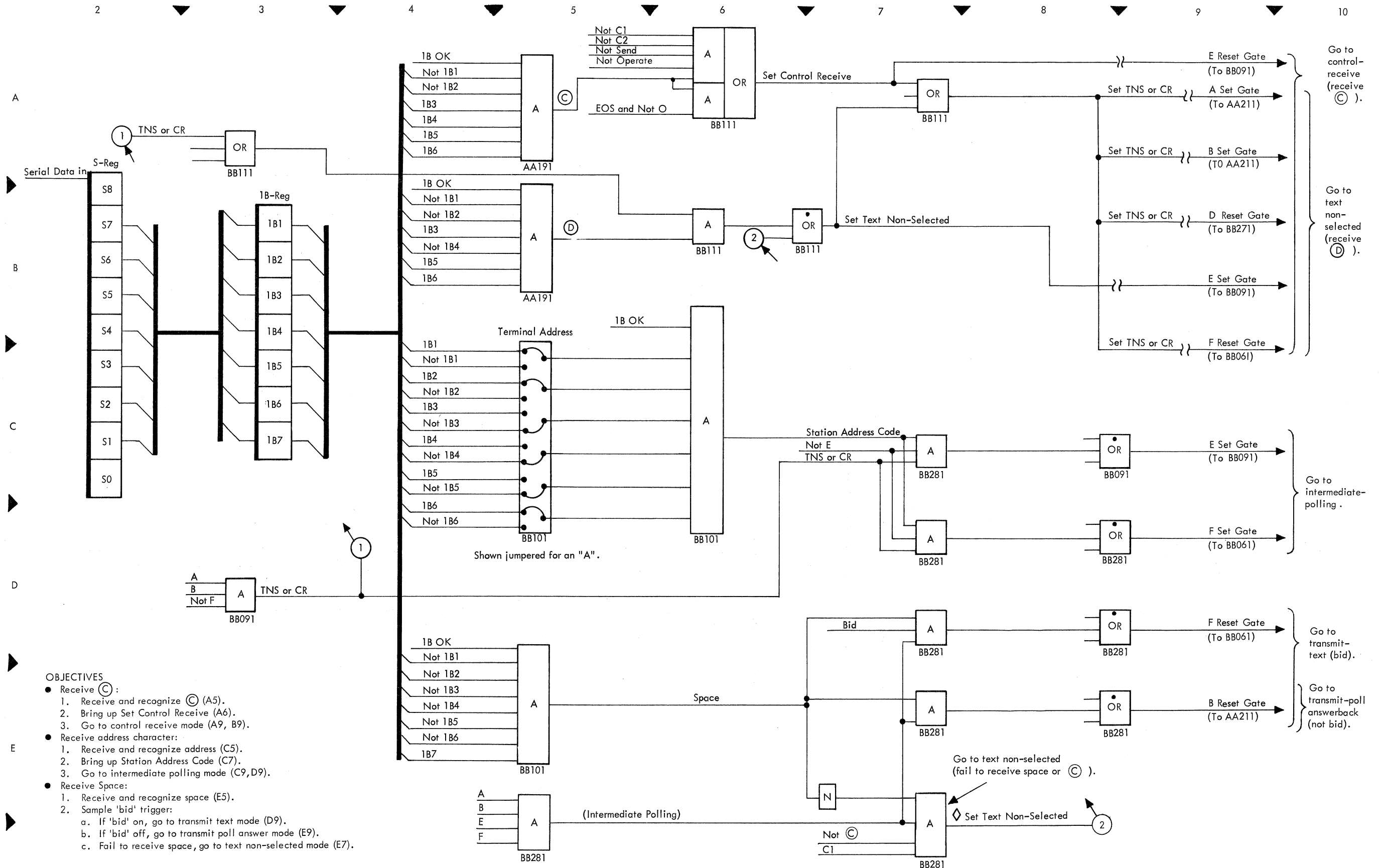


- OBJECTIVES**
- Terminal in transmit status answerback mode.
 - Generate and transmit \odot if terminal has status:
 - Bring up 1B Generate (C4).
 - Start control clock (D5).
 - Bring up 1B Set (C5).
 - Load \odot (B, A, 8, 2, 1) to 1B register (A5, B5, C5).
 - Transmit normally (serdes clock runs continuously when Send comes up).
 - Go to control selected mode if terminal has status:
 - Turn on 'end of state' (E5).
 - Detect \odot in 1B (C7).
 - Bring up E Set Gate and A Reset Gate (D9).
 - Generate and transmit \odot if terminal does not have status:
 - Start control clock' (D5).
 - Bring up 1B Set (C5).
 - Load \odot (B-bit) to 1B (A5).
 - Transmit normally.
 - Go to control address if terminal does not have status:
 - Turn on 'end of state' (E5).
 - Detect not \odot in 1B (C7).
 - Bring up A Reset Gate and F Reset Gate (D9, E9).

Go to control-selected (status). See IOP8--I4, I5, I6

Go to control-address (not status).

Figure IOP-10. Receive Polling Character Sequence



- OBJECTIVES**
- Receive (C):
 1. Receive and recognize (C) (A5).
 2. Bring up Set Control Receive (A6).
 3. Go to control receive mode (A9, B9).
 - Receive address character:
 1. Receive and recognize address (C5).
 2. Bring up Station Address Code (C7).
 3. Go to intermediate polling mode (C9, D9).
 - Receive Space:
 1. Receive and recognize space (E5).
 2. Sample 'bid' trigger:
 - a. If 'bid' on, go to transmit text mode (D9).
 - b. If 'bid' off, go to transmit poll answerback (E9).
 - c. Fail to receive space, go to text non-selected mode (E7).

Go to control-receive (receive (C)).

Go to text non-selected (receive (D)).

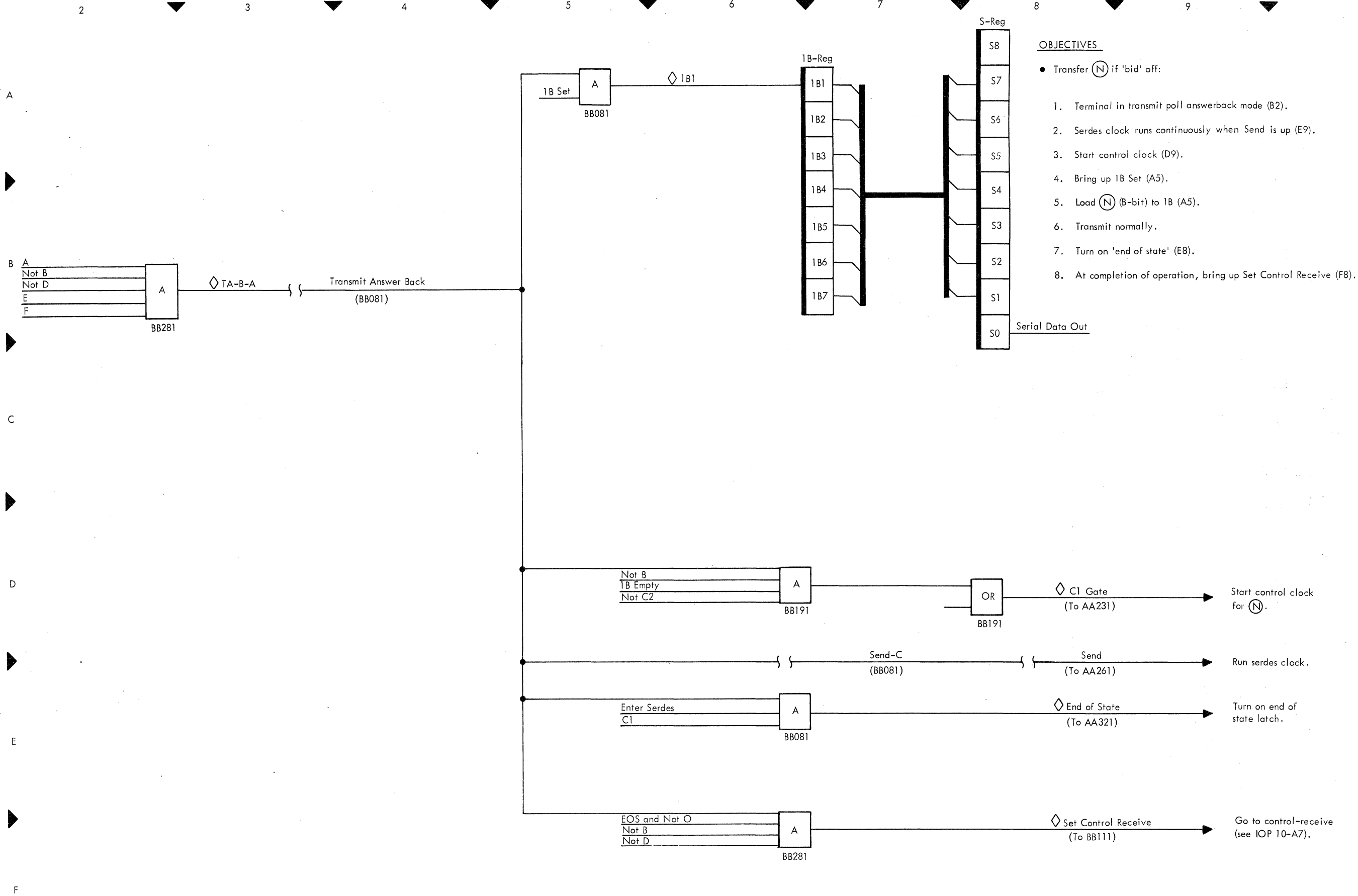
Go to intermediate-polling.

Go to transmit-text (bid).

Go to transmit-poll answerback (not bid).

Go to text non-selected (fail to receive space or (C)).

Figure IOP-11. Polling, Transmit Poll Answerback



ADDRESSING SEQUENCE: CENTRAL SENDS - * (C) (S) ADDR SPACE (C) OR (D) TEXT (B) (C)
 TERMINAL SENDS - (N) OR (Y) (Y) OR (N)

POLLING SEQUENCE: CENTRAL SENDS - * (C) ADDR SPACE *1 (Y) OR *2 (N) (Y) *3 OR (C) *4 OR (D) TEXT (B) (C)
 TERMINAL SENDS - (N) OR (D) TEXT (B) (C) TEXT (B) (C) (Y) OR (N)

NOTES: * (C) CLEARS THE LINE AND RETURNS ALL TERMINALS TO TNS OR CR.
 * 1 NORMAL ENDING
 * 2 TERMINAL RETRANSMITS SUCCESSFULLY
 * 3 CENTRAL DOES NOT ACKNOWLEDGE MESSAGE YES OR NO. TERMINAL SIGNALS DATA CHECK.
 * CENTRAL SENDS TEXT TO TERMINAL AFTER RECEIVING FROM TERMINAL

ALL ALD PAGE REFERENCES ARE TO MODE CHANGE LOGIC.

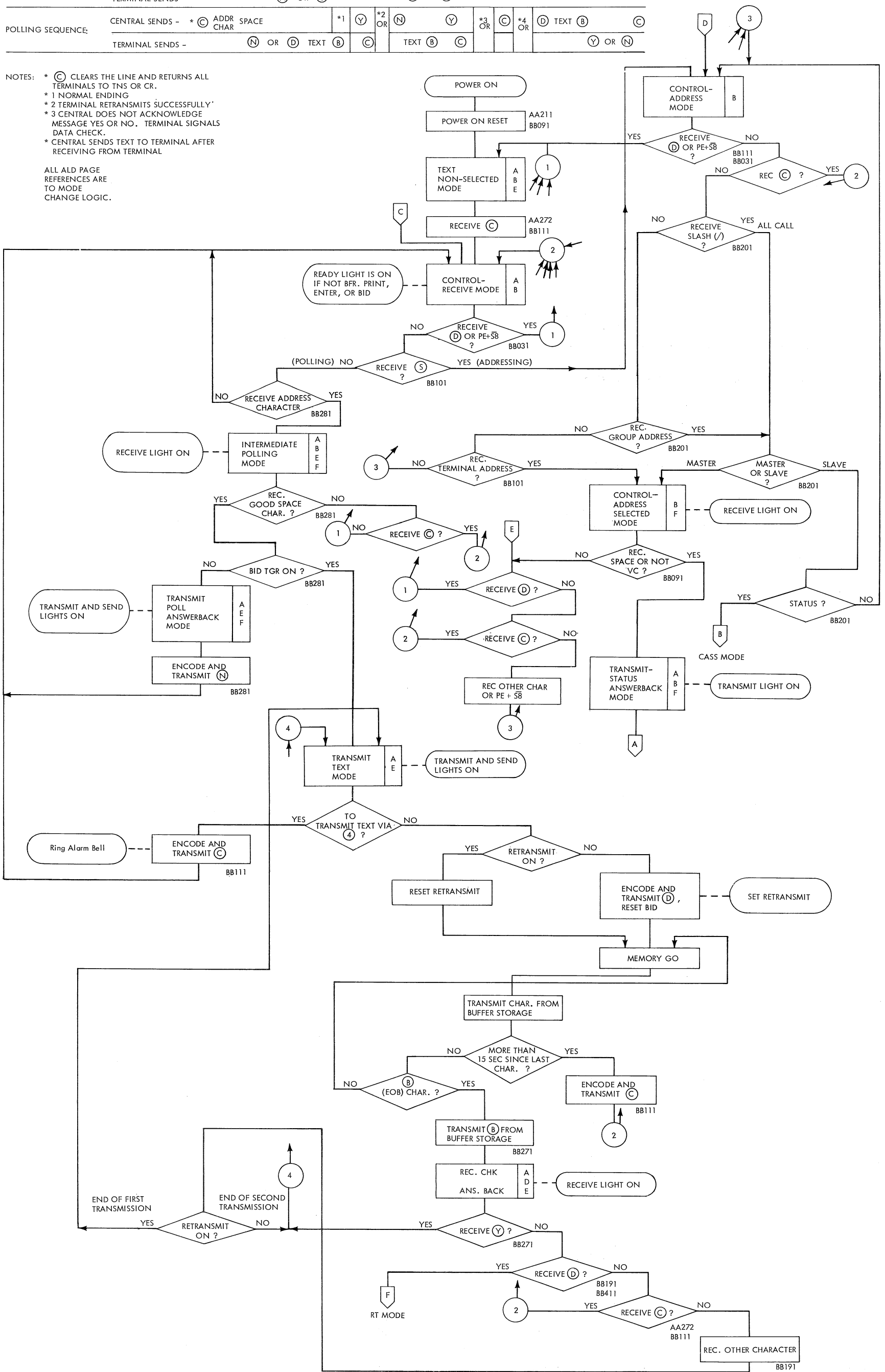


Figure IOP-12. Mode Control (Sheet 1 of 4)

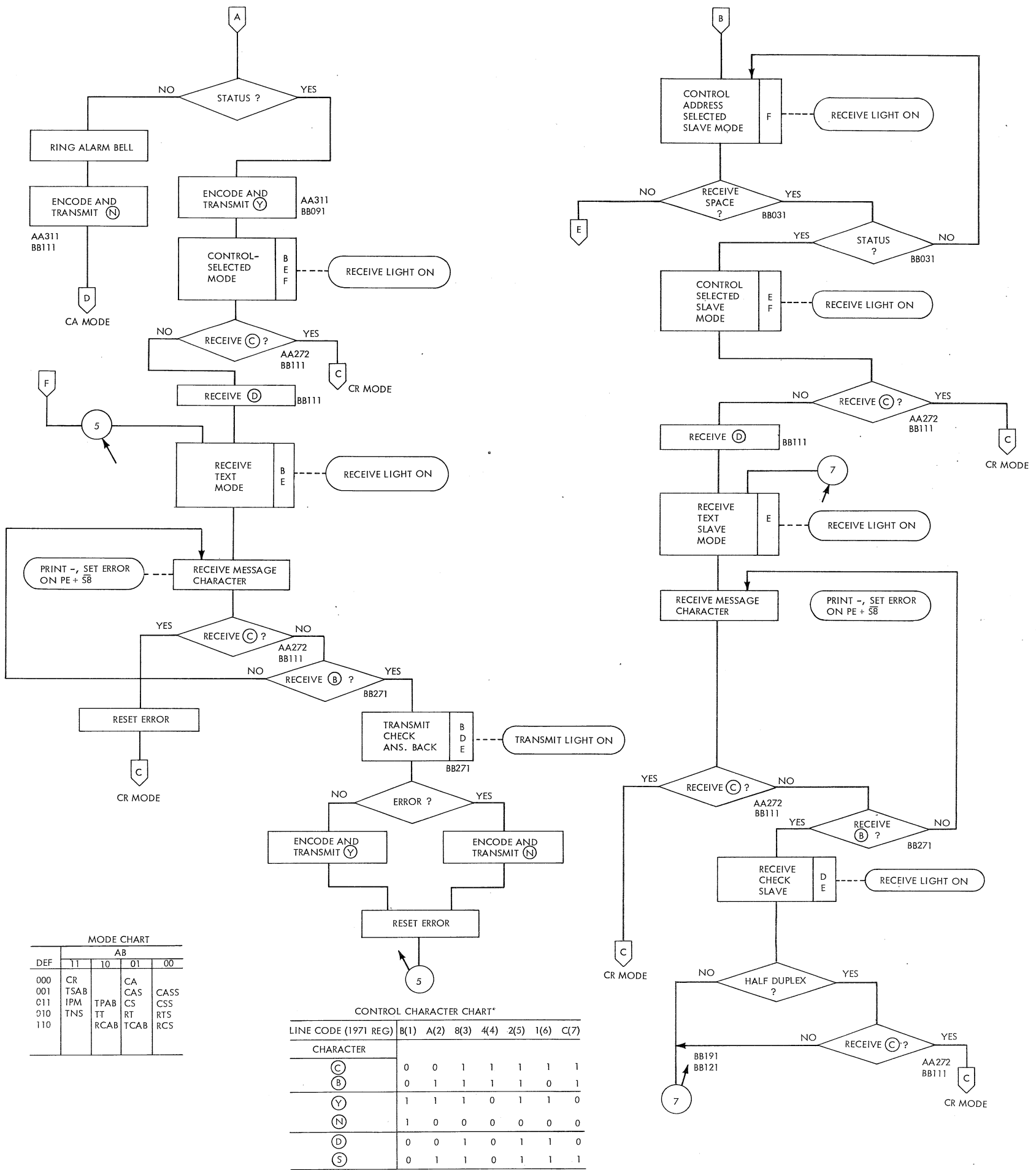


Figure IOP-12. Mode Control (Sheet 2 of 4)

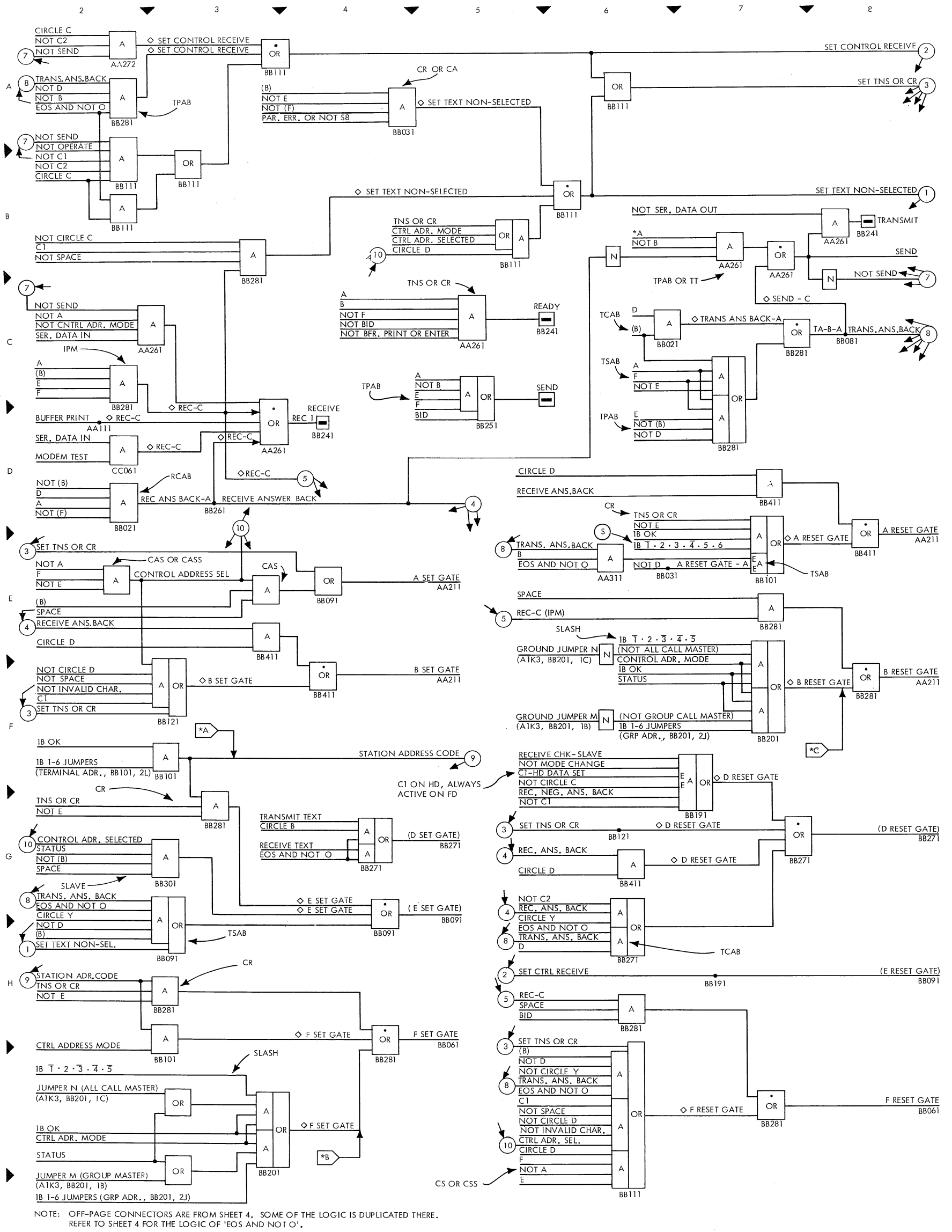
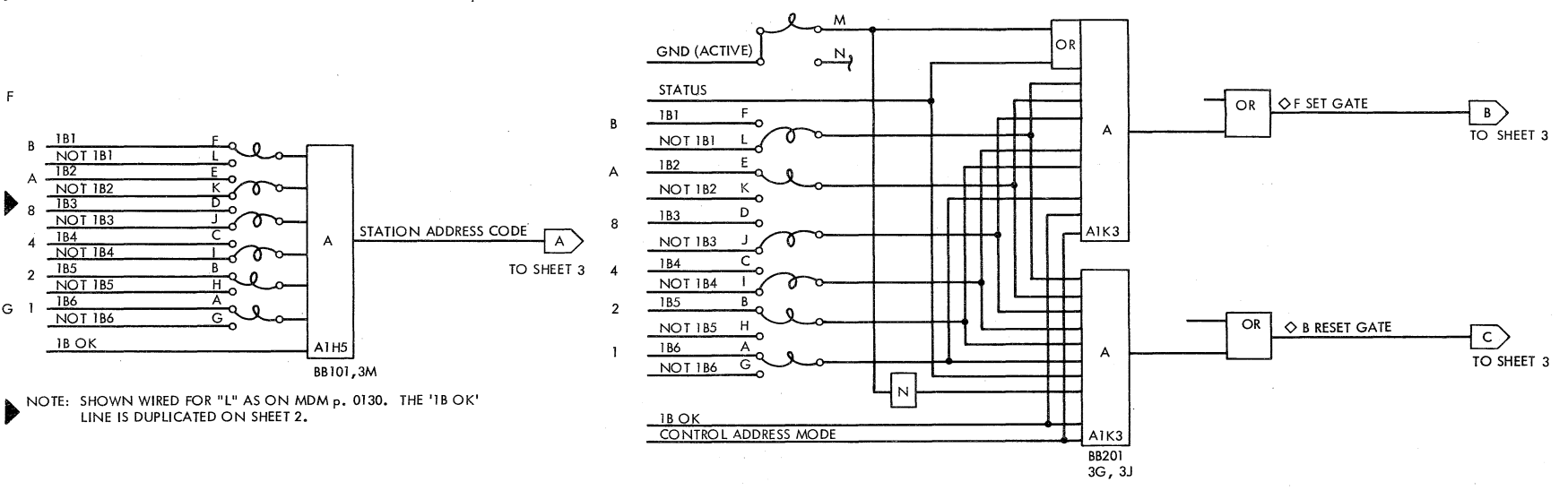
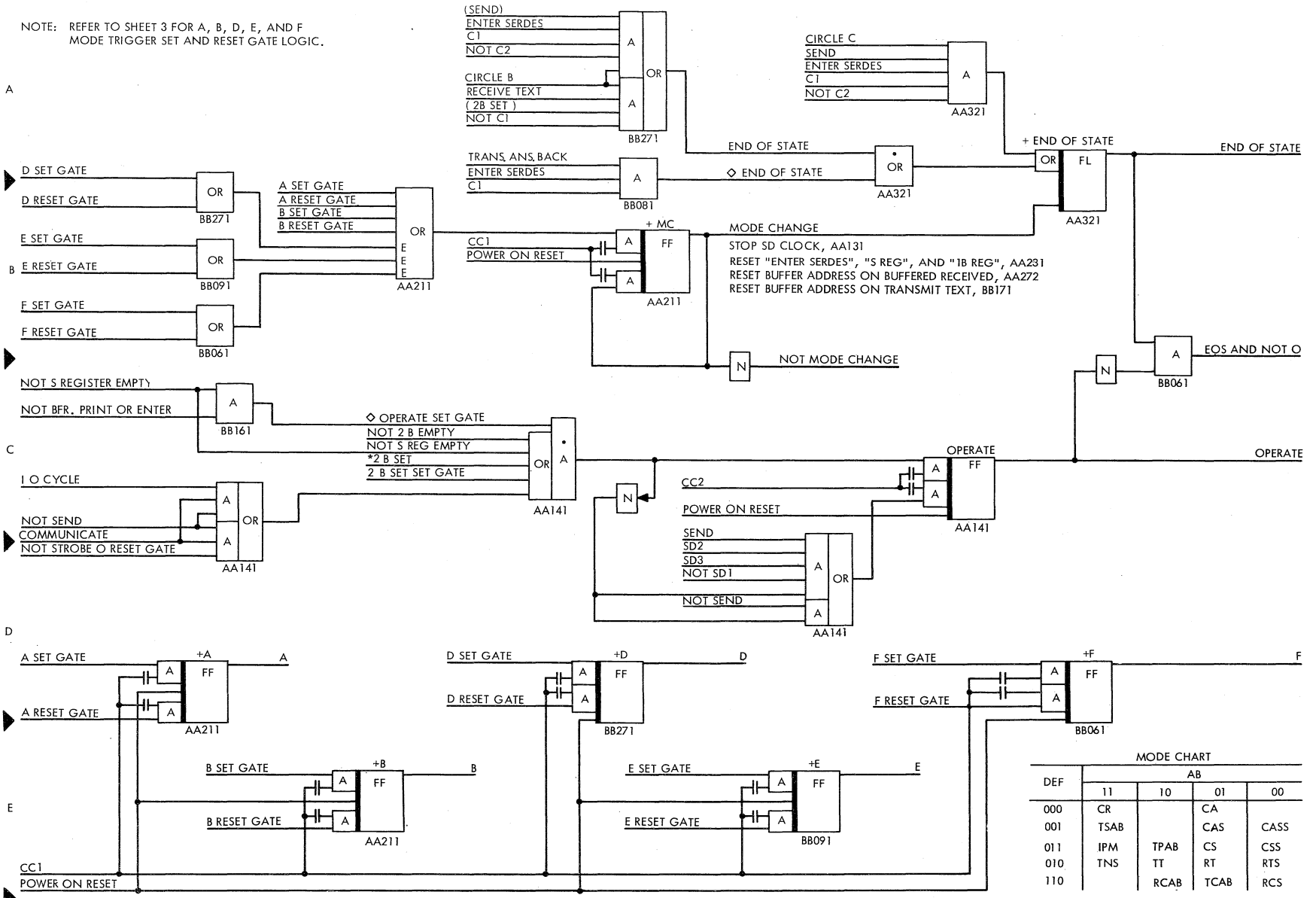


Figure IOP-12. Mode Control (Sheet 3 of 4)

NOTE: REFER TO SHEET 3 FOR A, B, D, E, AND F MODE TRIGGER SET AND RESET GATE LOGIC.



- H OBJECTIVES:**
1. SET END OF STATE (IF NEEDED) (SHEET 4, A7)
 2. TURN OFF OPERATE TGR AT END OF OPERATION (SHEET 4, C6)
 3. BRING UP MODE TRIGGER SET OR RESET GATE (S) (SHEET 3)
 4. TURN ON MODE CHANGE TGR (SHEET 4, B5) AND CHANGE MODE TRIGGERS (SHEET 4)
 5. RESET END OF STATE (SHEET 4, B7), TURN OFF MODE CHANGE TGR (SHEET 4, B5)

NOTE: SHOWN WIRED FOR "T" AND GROUP MASTER AS ON MDM p. 0130. SOME OF THE LOGIC IS DUPLICATED ON SHEET 3.

- J POSSIBLE MODE CHANGES IN ORDER OF POSSIBLE OCCURENCE STARTING FROM TNS:**
(MODE ABBREVIATIONS -- TNS - TEXT NON-SELECTED)
- CR - CONTROL RECEIVE
 - IPM - INTERMEDIATE POLLING MODE
 - TPAB - TRANSMIT POLL ANSWER BACK
 - TT - TRANSMIT TEXT
 - RCAB - RECEIVE CHECK ANSWERBACK
 - CA - CONTROL ADDRESS
 - CAS - CONTROL ADDRESS SELECTED
 - CASS - CONTROL ADDRESS SELECTED SLAVE
 - TSAB - TRANSMIT STATUS ANSWERBACK
 - CS - CONTROL SELECTED
 - CSS - CONTROL SELECTED SLAVE
 - RT - RECEIVE TEXT
 - RTS - RECEIVE TEXT SLAVE
 - TCAB - TRANSMIT CHECK ANSWERBACK
 - RCS - RECEIVE CHECK SLAVE

NOTE: ALL REFERENCES TO COORDINATES ARE ON SHEET 3, EXCEPT AS NOTED. EACH MODE IS FOLLOWED BY THE MODE TRIGGER CONFIGURATION IN PARENTHESES.

	FROM	TO	CAUSE	EOS?	COORDINATES
READY	TNS (ABE)	CR (AB)	RECEIVE (C) (EOT)		A2
	CR (AB)	IPM (ABEF)	RECEIVE ADDRESS CHAR.		F3, G3, H3
	CR (AB)	TNS (ABE)	RECEIVE (D) (START TEXT)		B5
	CR (AB)	TNS (ABE)	RECEIVE PAR. ERROR OR S8		A4
TRANSMIT SETUP	IPM (ABEF)	TPAB (AEF)	RECEIVE SPACE WITH BID OFF	YES	E7
	TPAB (AEF)	CR (AB)	SEND (N) (NEGATIVE)		A2
TRANSMIT	IPM (ABEF)	TT (AE)	RECEIVE SPACE WITH BID ON	YES	E7, H6
	TT (AE)	CR (AB)	15 SEC T-O, SEND (C) (EOT)	YES	(4, A7), (3, B2)
	TT (AE)	RCAB (ADE)	SEND B (END TEXT)		G4
	RCAB (ADE)	CR (AB)	RECEIVE (C) (EOT)		A2
	RCAB (ADE)	RT (BE)	RECEIVE (D) (START TEXT)		G6, D7, E3
	RCAB (ADE)	TT (AE)	RECEIVE (Y) (AFFIRMATIVE)		G6
	RCAB (ADE)	TT (AE)	REC. NEG. ANSBK. (NOT (Y), (D), (C))		F7
	TT (AE)	CR (AB)	SEND (C) (EOT)	YES	(4, A7), (3, B2)

	FROM	TO	CAUSE	EOS?	COORDINATES
RECEIVE SETUP	CR (AB)	CA (B)	RECEIVE (S)		D7
	CA (B)	CR (AB)	RECEIVE (C)		A2
	CA (B)	TNS (ABE)	RECEIVE (D)		B5
	CA (B)	TNS (ABE)	REC. PAR. ERROR OR NOT S8		A4
	CA (B)	CAS (BF)	RECEIVE ADDRESS CHAR.		H2
	CA (B)	CASS (F)	RECEIVE ADDRESS CHAR.		H2, E7, F7
	CAS (BF)	CA (B)	RECEIVE PE OR NOT S8, OR REC. VC THAT IS NOT (C), (D), OR SPACE		16, F2
	CASS (F)	CA (B)	RECEIVE (C)		A2
	CAS (BF)	CR (AB)	RECEIVE (C)		A2
	CASS (F)	CR (AB)	RECEIVE (D)		B5
RECEIVE-MASTER	CAS (BF)	TSAB (ABF)	RECEIVE SPACE OR NOT VC	YES	E3
	TSAB (ABF)	CA (B)	NOT STATUS, SEND (N)	YES	E7, 16
	TSAB (ABF)	CS (BEF)	STATUS, SEND (V)		E3, G2
	CS (BEF)	CR (AB)	RECEIVE (C)		A2
	RT (BE)	RT (BE)	RECEIVE (D) (BEGIN TEXT)		16
RECEIVE-SLAVE	RT (BE)	TCAB (BDE)	RECEIVE (B) (END TEXT)	YES	G4
	TCAB (BDE)	RT (BE)	SEND (Y) OR (N)	YES	H6
RECEIVE-MASTER	RT (BE)	CR (AB)	RECEIVE (C)		A2
	CASS (F)	CSS (EF)	RECEIVE SPACE OR NOT VC WITH STATUS		G2
	CSS (EF)	CR (AB)	RECEIVE (C)		A2
	CSS (EF)	RTS (E)	RECEIVE (D) (BEGIN TEXT)	YES	16
	RTS (E)	RCS (DE)	RECEIVE (B) (END TEXT)		G4
	RCS (DE)	RTS (E)	FULL DUPLEX - AUTOMATIC		F6
RECEIVE-SLAVE	RCS (DE)	RTS (E)	HALF DUPLEX - RECEIVE NOT (C)		F6
	RCS (DE)	CR (AB)	HALF DUPLEX - RECEIVE (C)		A2
	RTS (E)	CR (AB)	RECEIVE (C)		A2

Figure IOP-12. Mode Control (Sheet 4 of 4)

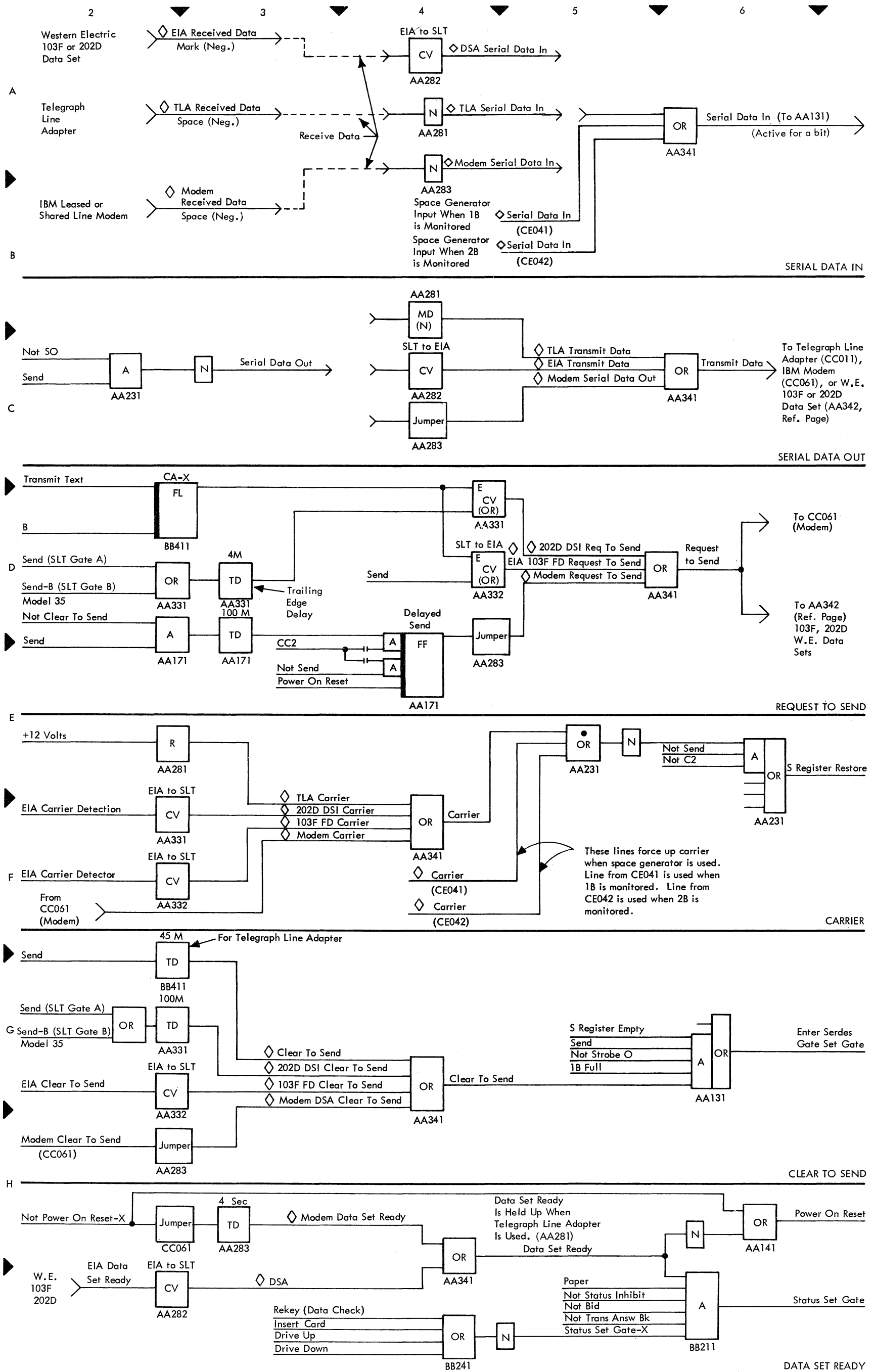


Figure IOP-13. Terminal to Line Adapter Interface (Sheet 1 of 2)

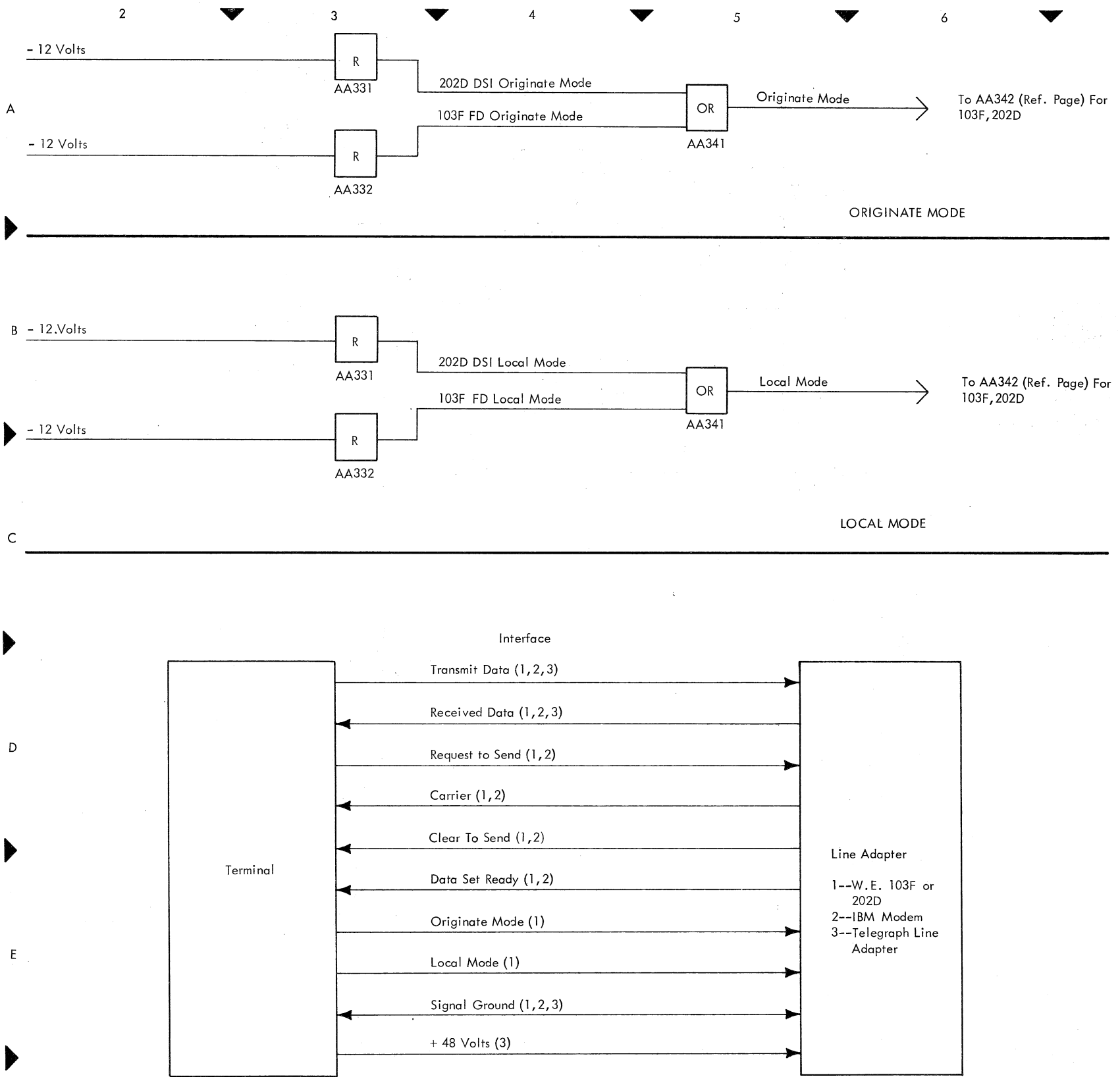
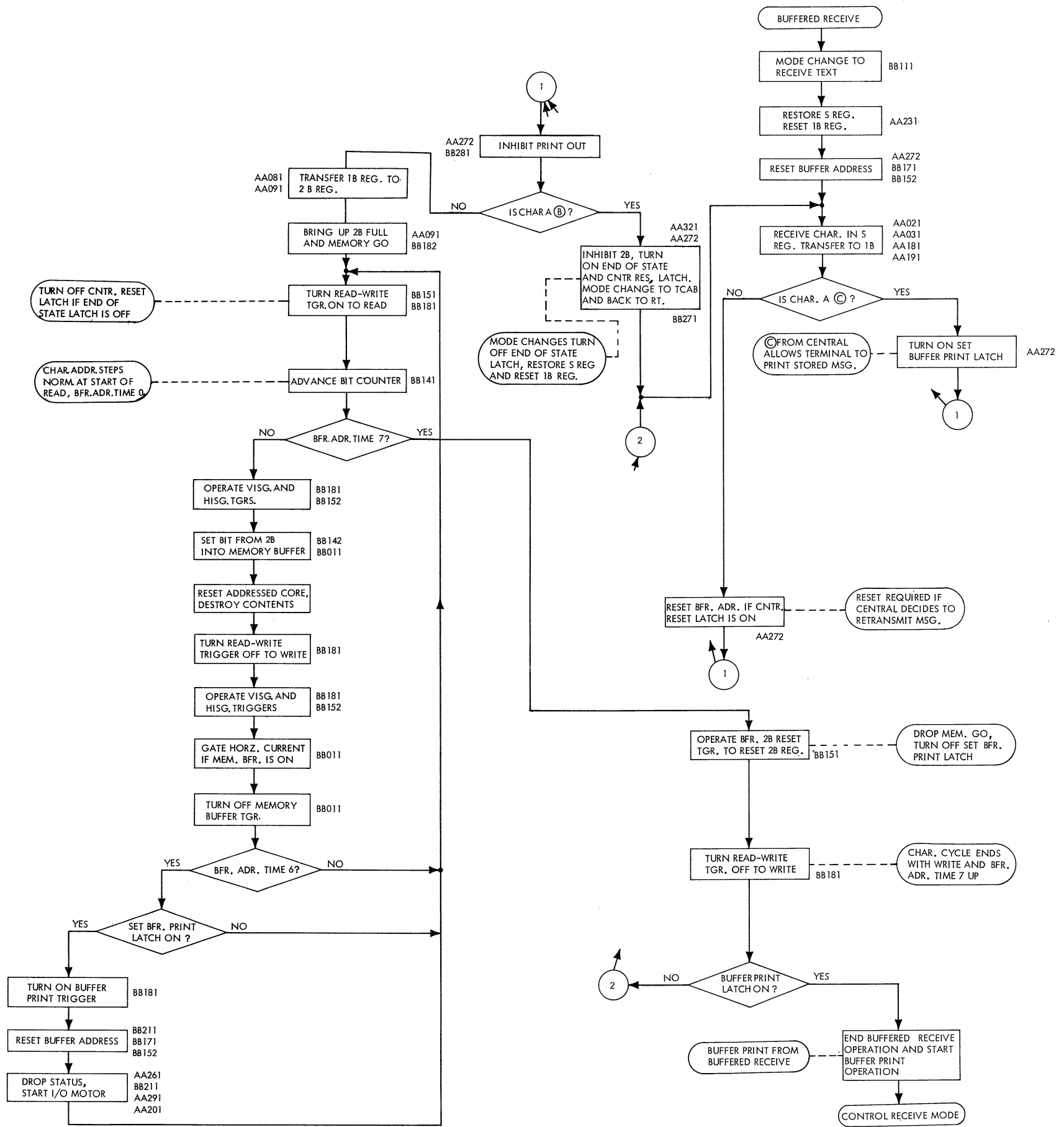


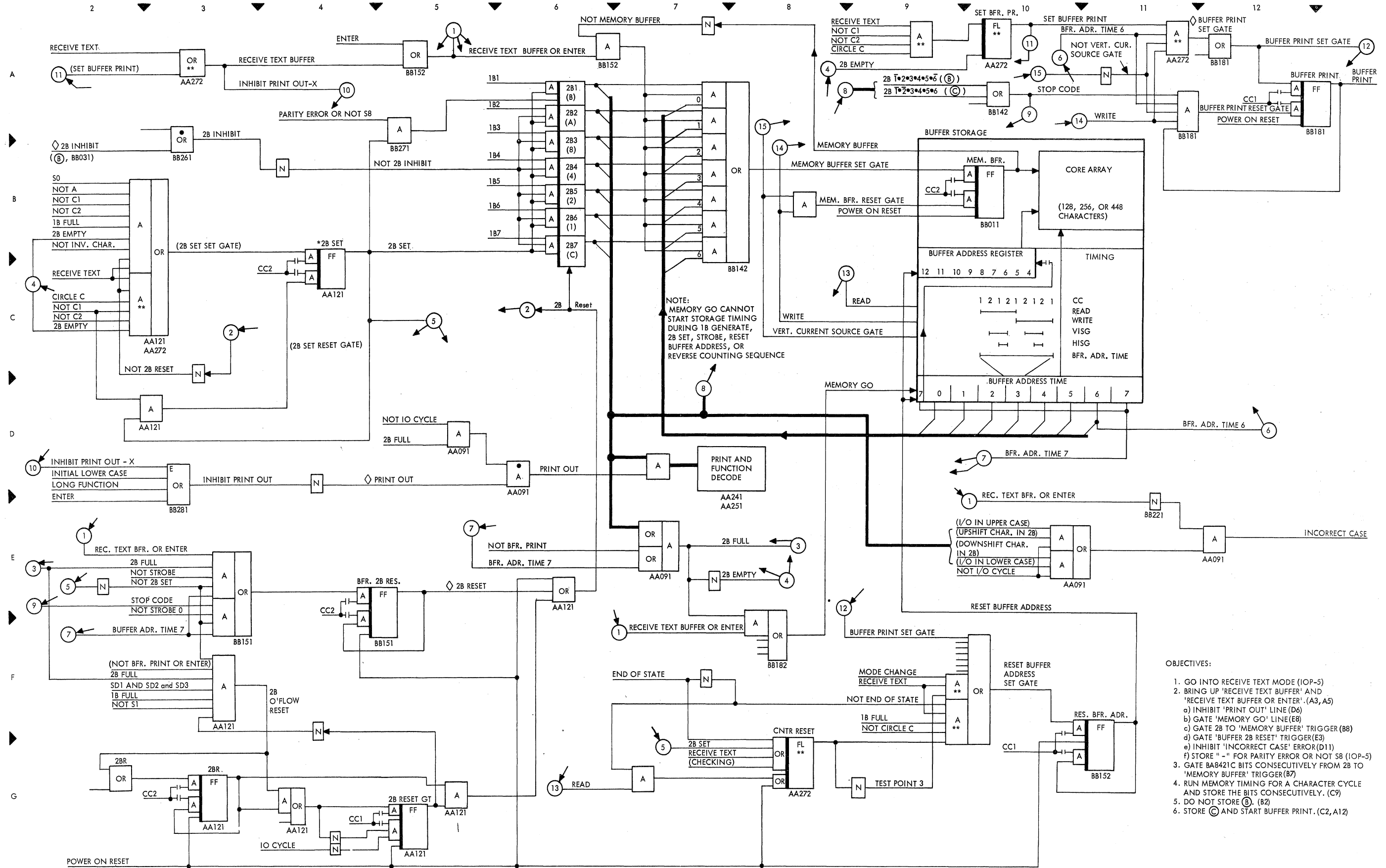
Figure IOP-13. Terminal to Line Adapter Interface (Sheet 2 of 2)



NOTE:
REFER TO IOP-6 FOR MORE
DETAILED INFORMATION
ON RECEIVE CIRCUITS.

Figure IOP-14. Buffered Receive (Sheet 1 of 2)

Figure IOP-14. Buffered Receive (Sheet 2 of 2)



** PRESENT ONLY WITH BUFFERED RECEIVE.

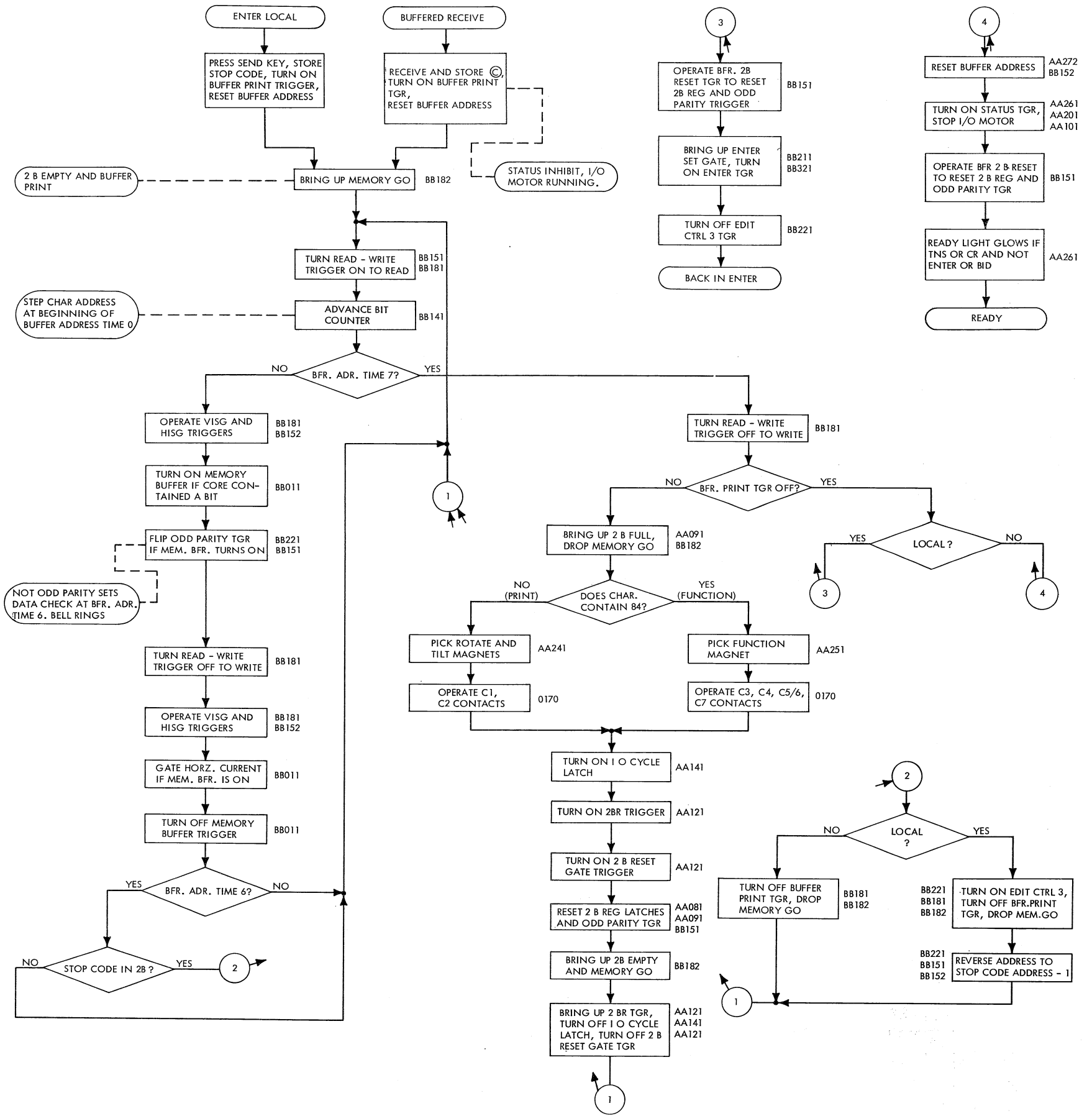
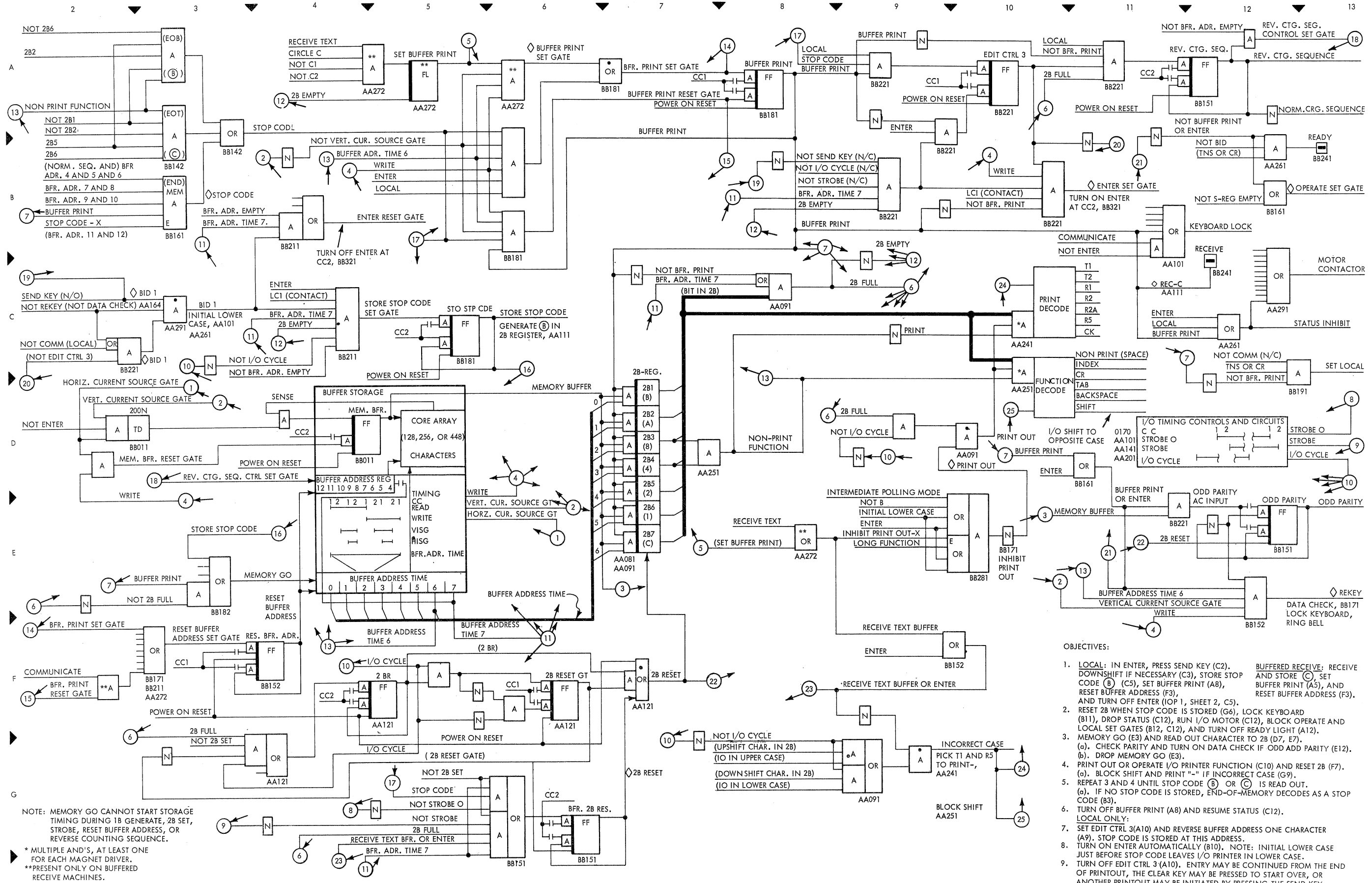


Figure IOP-15. Buffer Print (Sheet 1 of 2)

Figure IOP-15. Buffer Print (Sheet 2 of 2)

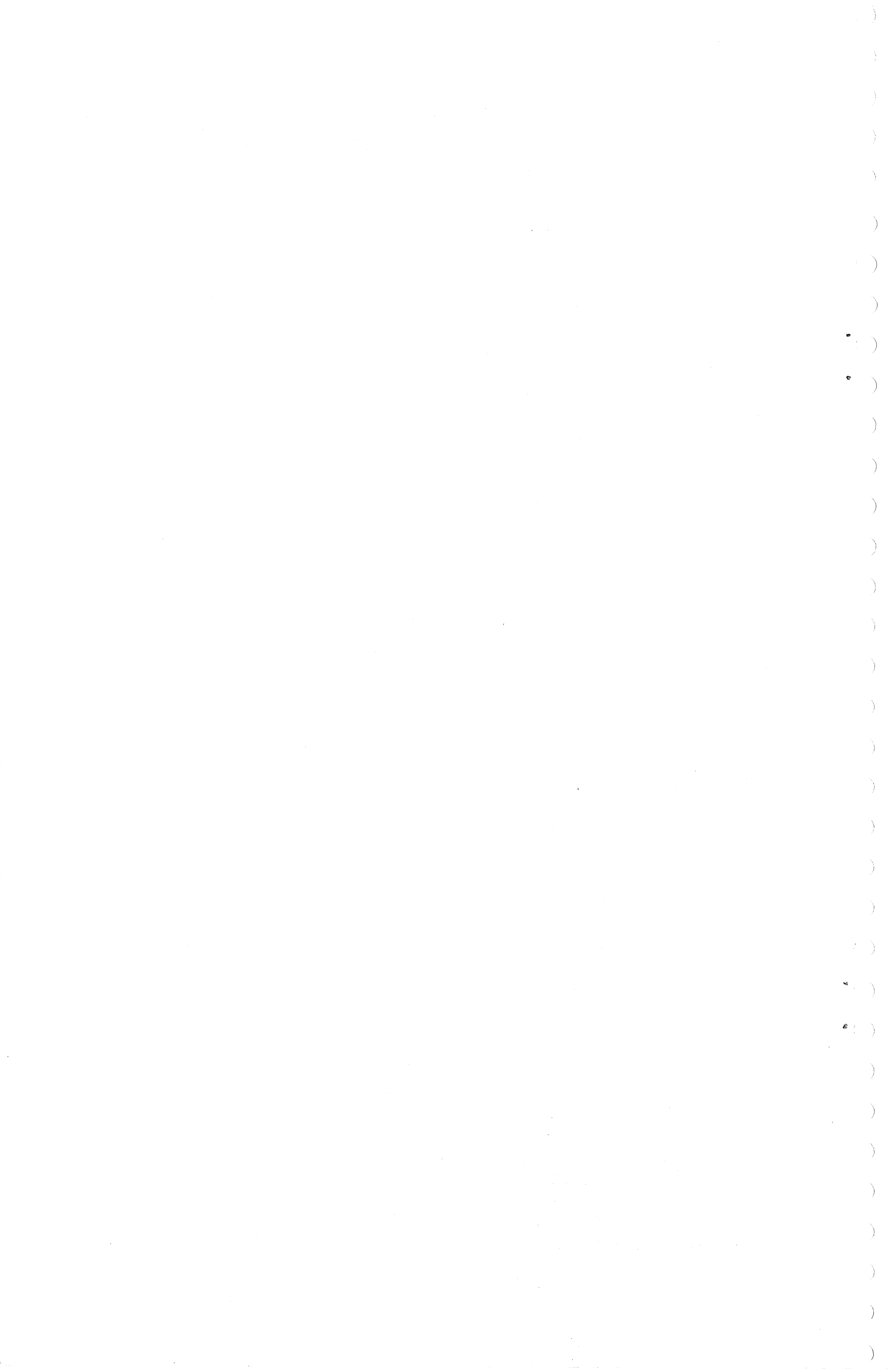


NOTE: MEMORY GO CANNOT START STORAGE TIMING DURING 1B GENERATE, 2B SET, STROBE, RESET BUFFER ADDRESS, OR REVERSE COUNTING SEQUENCE.

* MULTIPLE AND'S, AT LEAST ONE FOR EACH MAGNET DRIVER.

**PRESENT ONLY ON BUFFERED RECEIVE MACHINES.

- OBJECTIVES:
1. LOCAL: IN ENTER, PRESS SEND KEY (C2). DOWNSHIFT IF NECESSARY (C3), STORE STOP CODE (B) (C5), SET BUFFER PRINT (A8), RESET BUFFER ADDRESS (F3), AND TURN OFF ENTER (IOP 1, SHEET 2, C5).
 2. RESET 2B WHEN STOP CODE IS STORED (G6), LOCK KEYBOARD (B11), DROP STATUS (C12), RUN I/O MOTOR (C12), BLOCK OPERATE AND LOCAL SET GATES (B12, C12), AND TURN OFF READY LIGHT (A12).
 3. MEMORY GO (E3) AND READ OUT CHARACTER TO 2B (D7, E7). (a). CHECK PARITY AND TURN ON DATA CHECK IF ODD ADD PARITY (E12). (b). DROP MEMORY GO (E3).
 4. PRINT OUT OR OPERATE I/O PRINTER FUNCTION (C10) AND RESET 2B (F7). (a). BLOCK SHIFT AND PRINT "-" IF INCORRECT CASE (G9).
 5. REPEAT 3 AND 4 UNTIL STOP CODE (B) OR (C) IS READ OUT. (a). IF NO STOP CODE IS STORED, END-OF-MEMORY DECODES AS A STOP CODE (B3).
 6. TURN OFF BUFFER PRINT (A8) AND RESUME STATUS (C12).
- LOCAL ONLY:
7. SET EDIT CTRL 3 (A10) AND REVERSE BUFFER ADDRESS ONE CHARACTER (A9). STOP CODE IS STORED AT THIS ADDRESS.
 8. TURN ON ENTER AUTOMATICALLY (B10). NOTE: INITIAL LOWER CASE JUST BEFORE STOP CODE LEAVES I/O PRINTER IN LOWER CASE.
 9. TURN OFF EDIT CTRL 3 (A10). ENTRY MAY BE CONTINUED FROM THE END OF PRINTOUT, THE CLEAR KEY MAY BE PRESSED TO START OVER, OR ANOTHER PRINTOUT MAY BE INITIATED BY PRESSING THE SEND KEY.



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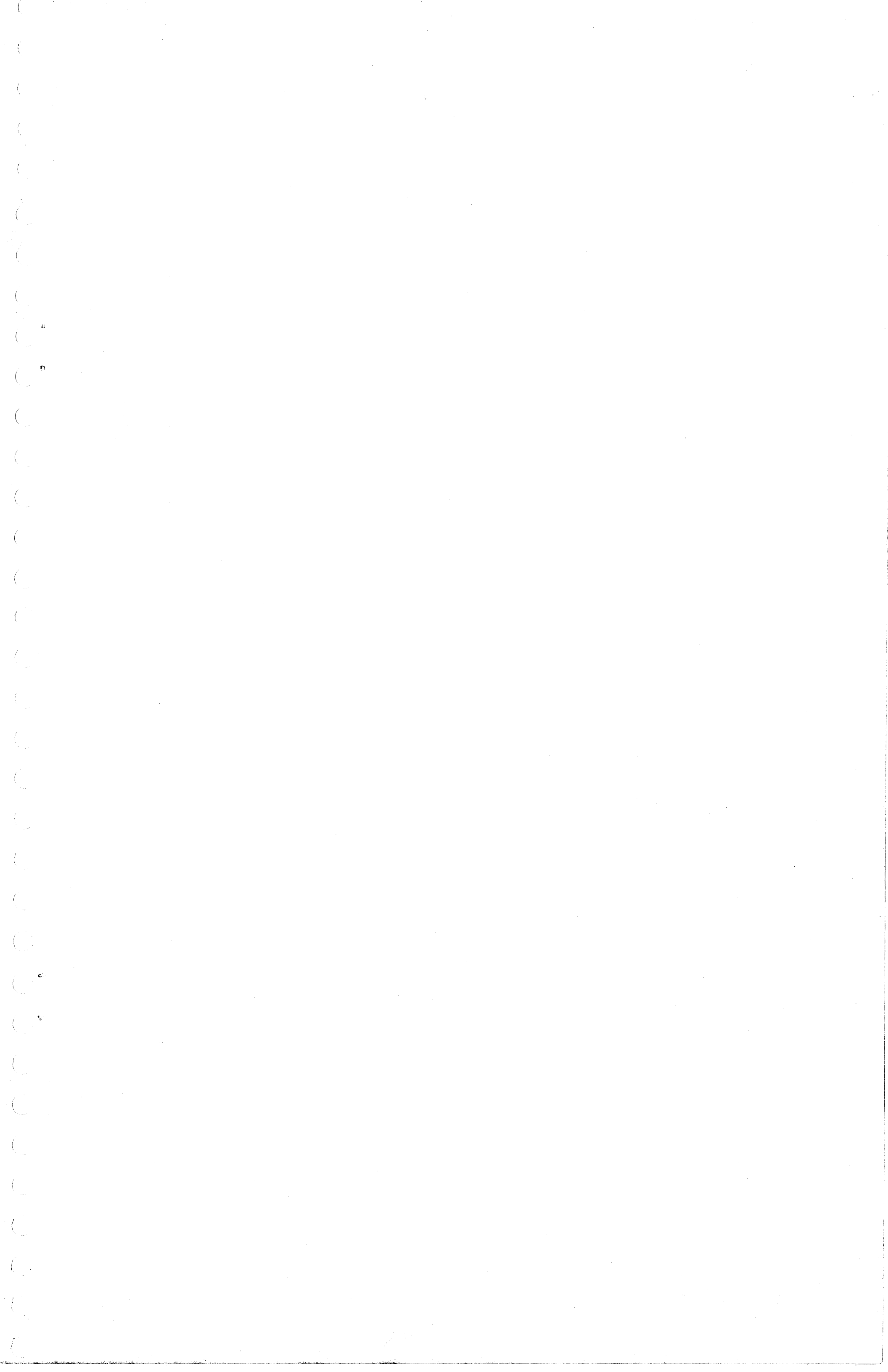
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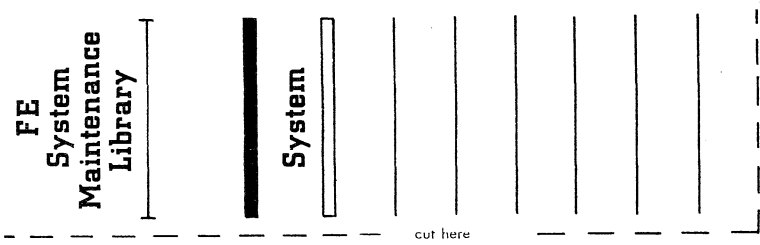
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