HP 13255

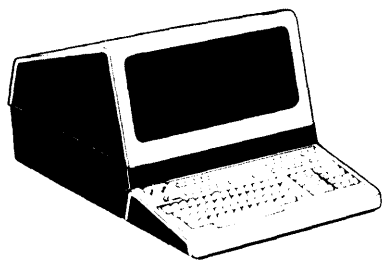
MEMORY CONTROLLER MODULE

Manual Part No. 13255-~~91249~~ 91252

PRINTED

JUN-23-81

DATA TERMINAL
TECHNICAL INFORMATION



HEWLETT hp PACKARD

Printed in U.S.A.

1.0 INTRODUCTION.

The processor (8085A-2) module functions as the main controlling unit for the 2747F terminal. It also contains the hardware to interface the processor to the external keyboard. The processor fetches instructions from memory and performs I/O operations on other modules attached to the terminal data bus (backplane assembly). The 8085A-2 module has the capability of down loading code in a RAM based 2647F.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Processor (8085A-2) Module is contained in tables 1.0 through 6.7

Table 1.0 Physical Parameters

PART NUMBER	NOMENCLATURE	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60249	PROCESSOR (8085A-2)	12.5 x 4.0 x 0.5	0.5

NUMBER OF BACKPLANE SLOTS REQUIRED: 1

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NOTE: This document is part of the 2647F DATA TERMINAL product series Technical Information Package (HP 13255).

1.0 INTRODUCTION.

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Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 4.774 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(+/- 5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 0.5 A	@	@	@ mA
	NOT APPLICABLE	NOT APPLICABLE	NOT APPLICABLE

115 volts AC	220 volts AC
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Clock Frequency: 4.915 MHz

Table 4.0 Jumper Definition

PCA Designation	Function
W1	RAM/ROM Based Terminal (see section 3.8)

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYSCLK	4.915 MHz System Clock
-4		Not Used
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19	$\overline{\text{ADDR14}}$	Negative True, Address Bit 14
-20	$\overline{\text{ADDR15}}$	Negative True, Address Bit 15
-21	$\overline{\text{IO}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (cont)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C		Not Used
-D	PON	Positive True, System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not Used
-S	$\overline{\text{WAIT}}$	Negative True, Assert Wait State
-T		Not Used
-U		Not Used
-V	ADDR16	Positive True, Address Bit 16
-W	ADDR17	Positive True, Address Bit 17
-X	ADDR18	Positive True, Address Bit 18
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Valid)
-Z		Not Used

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2 and 3), the timing diagram (figure 4), and the parts list (02640-60252).

The Memory Controller Module provides program and variable space for the terminal. It consists of memory drivers and series termination resistors, data port, memory array, address multiplexer, refresh address generator, refresh timer, refresh cycle generator, bus interface and board select circuitry, and a memory cycle generator.

3.1 SERIES TERMINATION RESISTORS

The series termination resistors minimize undershoot by terminating the bus lines with the line impedance. This approximates to 20 ohms since it consists of an 80 ohm line with distributed, lumped, and capacitive loads. Current limit protection is provided free which limits the driver output to 75 mA if two or more array inputs are shorted together.

3.2 DATA PORT

3.2.1 The data port consists of a 74LS244 data in driver (U46) and a 74LS373 data out transparent latch. This port is enabled whenever $\overline{\text{BOARD SELECT}}$ (U53-6) and $\overline{\text{REQ}}$ (P1-Y) are both low, causing U56-3 to go low. The direction of data flow is arbitrated by $\overline{\text{WRITE}}$ (P1-P) in the following manner: if $\overline{\text{WRITE}}$ is high, then U56-8 will be active, resulting in data transmission from the Memory Controller to the data bus. If $\overline{\text{WRITE}}$ is low, then U56-6 will be active, and the data flow will be from the bus to the memory array. Data is latched in the output latch by the trailing edge of $\overline{\text{CAS}}$, the column address strobe.

3.2.2 The transparent data latch (U27) allows data to propagate through the latch prior to being latched. This means the RAM access time is optimized and if a higher speed RAM is used, the memory will appear to be correspondingly higher in speed. The data is latched so that completion of the memory cycle does not depend on the completion of the processor memory handshake.

3.3 MEMORY ARRAY

3.3.1 The memory array consists of up to thirty-two 64K RAMS. The RAMs are socketed to allow field upgrade and repair.

3.3.2 The power distribution is via a low impedance 4-layer PC board structure. The ceramic capacitors which supply the transient current are organized such that some redundancy exists. This allows reliable operation with one open circuit component.

3.3.3 The memory array is organized as four modules of equal size (if all are loaded). The entire array is activated by the start of a memory cycle, which is when U71-9 goes low. At that time, a row address strobe is sent to all four banks. The column address strobe passes through a four to one decoder which determines which module is selected for read or write.

3.4 ADDRESS MULTIPLEXER

3.4.1 The address multiplexer consists of two 74LS258 quad inverting 2 to 1 line tri-state multiplexers (U75,76) and a 74LS244 octal tri-state buffer (U55).

3.4.2 The 74LS258 multiplexers select the row or column address from the terminal bus address lines for memory cycles. Which address is selected

is determined by R/$\overline{C}$ (delay line R12-2). These multiplexers are put in the hi-Z state during refresh cycles and during power on (when refresh is occuring continuously).

3.4.3 The function of the 74LS244 buffer is to either transfer or block the refresh address counter outputs from the internal address bus. This buffer is enabled whenever refresh cycles are occuring (i.e. refresh cycle or power on).

3.4.4 Whether the multiplexer is in the refresh or memory state is controlled by a 74LS74 D-flip flop (U24). This flip flop can be set to the refresh state in one of two ways: the power on signal is fed to the preset input to initialize the system and to allow for continuous refresh during power on. The flip flop can also be clocked to the refresh state by the signal RFSH (U14-8) which indicates the start of a refresh cycle. The multiplexor is reset to the memory state by the signal $\overline{\text{RFSH}}$ $\overline{\text{STALL}}$ (U13-5) at the clear input. This occurs halfway through the $\overline{\text{RAS}}$ precharge time of the previous refresh cycle to allow the memory addresses sufficient setup time before the next memory cycle.

3.5 REFRESH ADDRESS GENERATOR

The refresh address generator consists of a 74LS393 dual four bit counter (U45). This counter is allowed to come up in an indeterminant state and is then continuously clocked through the 128 possible refresh addresses. The eigth bit also counts although it is not necessary as a refresh address line. The counter is clocked by the signal COUNT (U26-6). COUNT is the inverted refresh row address strobe, and therefore the refresh address generator is clocked each refresh cycle by the trailing edge of the row address strobe.

3.6 REFRESH TIMER

3.6.1 Each row of the dynamic memories must be completely refreshed every 2 msec. Since each memory is organized into 128 rows, there must be 128 refresh cycles every 2 msec to avoid loss of information. This means that a refresh cycle must occur every 15.63 usec. The system clock is 4.915 MHz. If this clock is divided by 64 and the resulting edge used to trigger a refresh cycle, a refresh will occur every 13.02 usec.

3.6.2 The refresh timer consists of a 74LS393 dual four bit counter (U22) set up as a divide by 64. The output of this counter is synchronized with the falling edge of the system clock to avoid collisions between memory and refresh cycles (the memory cycle is synchronized to the rising edge of the system clock by the processor board). This synchronization is accomplished by use of a 74S74 flip flop (U71). The synchronized out~ put (U71-6) feeds the preset input of another 74S74 flip flop (U52) which acts as a refresh pending latch. The output of this flip flop

(U52-5) is ANDed with the signal $\overline{\text{MEM BUSY}}$ (U52-8) which indicates if a memory cycle is previously in progress. The positive true output of this gate (U14-8) is the signal RFSH, which indicates an active refresh cycle in progress.

3.7 REFRESH CYCLE GENERATOR

The refresh cycle generator generates a row address strobe which is fed to the memory chips along with the refresh address; the combination of

these signals performs a $\overline{\text{RAS}}$ only refresh cycle for the memory array.

3.7.1 The cycle is triggered by the signal RFSH, inverted and presented to the clock input of a 74LS112 J-K flip flop (U26). This flip flop is tied to a permanent set state. Setting this flip flop causes the K input of the other half of U26 to go high resulting in the toggle state at the inputs of this flip flop (U26-2,3). The next rising edge of the

clock causes signal $\overline{\text{RFSH RAS}}$ to go low; it will remain so for one en~ tire clock cycle (204 nsec). Two 74LS74 D flip flops (U13,23) extend the refresh cycle by one more complete clock cycle to allow sufficient RAS precharge and address setup time as discussed above. U23-5 feeds back to the refresh timer to end the cycle and allow a new timing cycle to begin.

3.7.2 During power on, the signal $\overline{\text{RESET}}$ forces U26 to the toggle state perma~

nently, resulting in continuous refreshing until $\overline{\text{RESET}}$ returns to the high state.

3.8 BUS INTERFACE AND BOARD SELECT CIRCUITRY

3.8.1 The bus interface circuitry consists of several buffer drivers, a wait state generator and an IO port designed to be used by OEM's for software protection. The bus signals SYSCLK, $\overline{REQ}$, and PON are buffered by 74LS244 drivers to reduce loading. In addition, SYSCLK and $\overline{REQ}$ are also inverted to be used in that state by the timing circuitry.

3.8.2 The Memory Controller Module requires one additional wait state be added to the normal bus cycle in order to provide sufficient time to accomplish memory reads and writes. To add this extra state, a wait state latch is used. This latch is a 74LS112 J-K flip flop (U44). This flip flop is set by (U71-9), which signals the start of a memory cycle and is cleared by CAS, the column address strobe. This timing results in the addition of one extra wait state. $\overline{WAIT}$ is driven on to the bus by a 74S03 open collector NAND gate (U42-3).

3.8.3 The Memory Controller Module incorporates a feature which will allow any interested party to protect his applications software on the 2647F by providing space for a four byte code which can be burned into a 32x8 PROM by the user; this code can be used to encrypt the applications software by any number of algorithms. U41 is a socket for a 32x8 field programmable PROM (Harris 7603 or equivalent). The four byte code can be accessed by reading IO ports 8A00, 8A02, 8A04, and 8A06 (hex). The codes will appear to the processor to be the inverted state of what is encoded in the PROM.

3.8.4 The board select circuitry combines the state of two of the three most significant bus address lines, ADDR16 and ADDR18, as follows:

Table 6.0

ADDR18	ADDR17	ADDR16	FUNCTION
0	0	0	Code Page 0
0	0	1	Unused
0	1	0	Code Page 1
0	1	1	Unused
1	0	0	RAM Space for Variables
1	0	1	Unused
1	1	0	RAM for BASIC Workspace
1	1	1	Display/IO Space

As can be seen from the above table, a RAM-based terminal would have to respond to all four cases where ADDR16=0; a ROM-based terminal needs to respond to the two cases where ADDR18 and ADDR16=10. When jumper W1 is absent, the output of the AND gate (U14-6) passes the inverted value of ADDR18. This gets combined with the value of ADDR16 to generate $\overline{\text{MEMGO}}$ (U42-6). It is also combined with IO to generate $\overline{\text{BOARD SELECT}}$ (U53-6) which is used to enable the data port and to enable the row and column address strobes to the memory array.

3.8.5 When W1 is present, U14-5 is tied to ground, therefore the output of the AND gate (U14-6) is permanently low. In this case, $\overline{\text{MEMGO}}$ and $\overline{\text{BOARD SELECT}}$ depend only on the value of ADDR16.

3.9 MEMORY CYCLE GENERATOR

3.9.1 The memory cycle generator is a synchronous sequntial state machine composed of several flip flops and gates. The purpose of this state machine is to generate the row and column address strobes for memory cycle operations with the appropriate timing.

3.9.2 A memory cycle begins when $\overline{\text{MEMGO}}$ goes low. This is synchronized with the leading edge of $\overline{\text{REQ}}$ by a 74S74 flip flop (U71). This also accomplishes the rising edge clock synchronization mentioned above in section 3.6.2, as $\overline{\text{REQ}}$ is synchronized with the clock by the processor. The output of this flip flop (U71-9) represents a memory cycle pending. This signal is ANDed with RFSH to prevent a memory cycle from starting while a refresh cycle is in progress. The output of this gate(U15-6) indicates an active memory cycle. The leading (negative) edge of this cycle active signal sets $\overline{\text{MEM BUSY}}$ to the true state, thus preventing the start of any refresh cycle; it also clocks a 74LS112 flip flop which starts $\overline{\text{MEMRAS}}$, the row address strobe (U12-12). Two flip flops (U13 and U25) then maintain $\overline{\text{MEMRAS}}$ in the low state for 2 clock cycles (408 nsec). The output of the second flip flop (U25-9) is the column address strobe, CAS. It lasts for one clock cycle (204 nsec) and follows the leading edge of MEMRAS by 204 nsec subject to logic delays.

3.9.3 As with the refresh cycle generator, two 74LS74 D flip flops (U21) are used to extend the memory cycle to allow for $\overline{\text{RAS}}$ precharge time. The output of the second of these (U21-5) resets $\overline{\text{MEM BUSY}}$ to the false state, thus ending the memory cycle.

3.9.4 $\overline{\text{MEMRAS}}$ is fed to a delay line (HP part # 1810-0384, 50 nsec delay, taps at 10 nsec intervals) where it is delayed 40 nsec to become R/$\overline{\text{C}}$, the signal which determines which half of the address is fed through the address multiplexers (see section 3.4.2).

3.9.5 $\overline{\text{MEMRAS}}$ is ANDed with $\overline{\text{BOARD SELECT}}$ the ORed with $\overline{\text{RFSH RAS}}$ to form the row address strobe signal to the memory array (U14-11). $\overline{\text{CAS}}$ is used to latch data out; in addition, $\overline{\text{CAS}}$ is used to determine which module of memory is being addressed. This is accomplished with a 74LS138, 3 to 8 line decoder. This decoder uses ADDR18 and ADDR17 at the address pins (U17-2,1) to determine which of the four memory modules is being accessed. When the decoder is enabled by $\overline{\text{BOARD SELECT}}$, a $\overline{\text{CAS}}$ at the other enable input (U17-5) produces a similar pulse at one of four outputs; this pulse is used as the column address strobe for the accessed module.

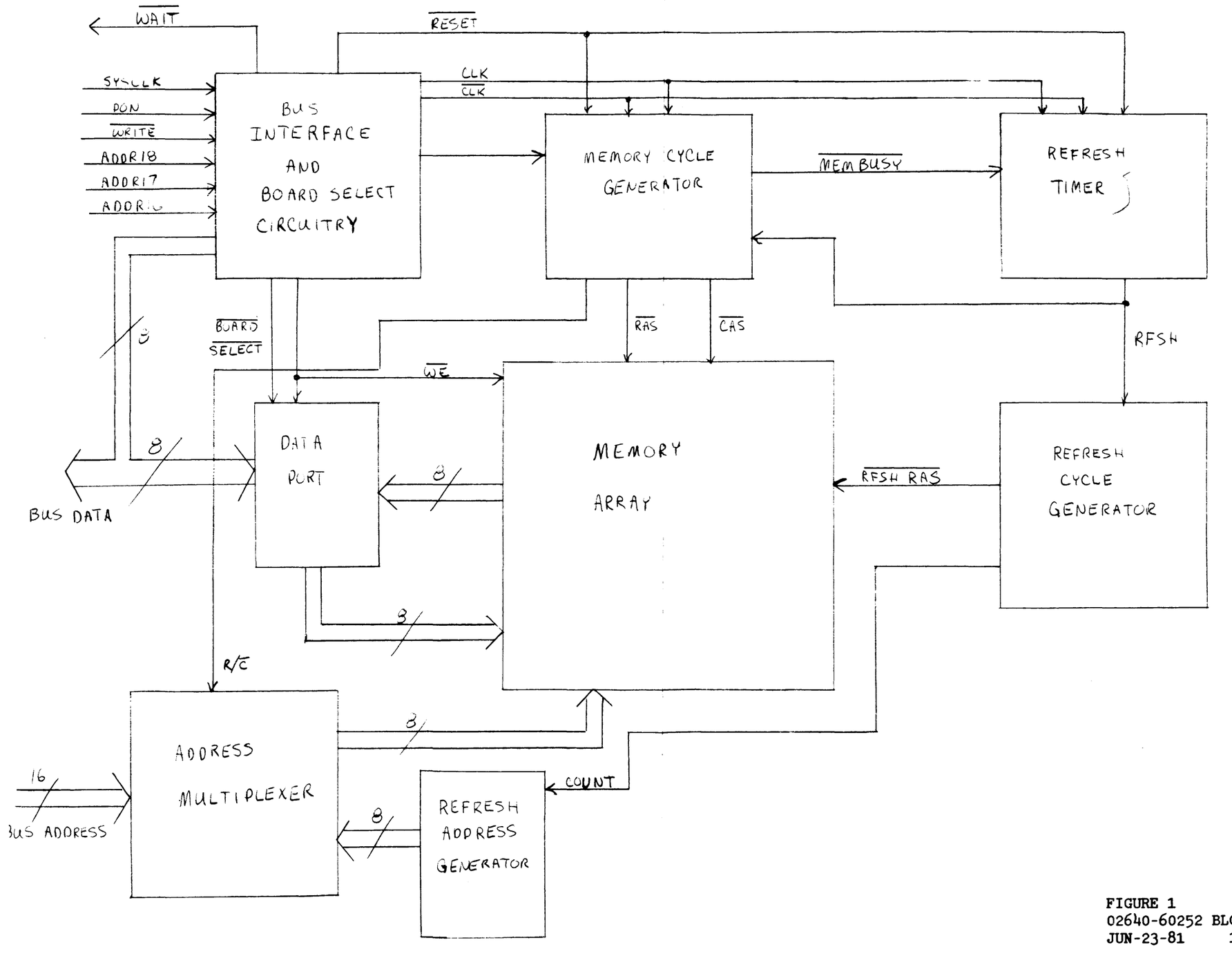
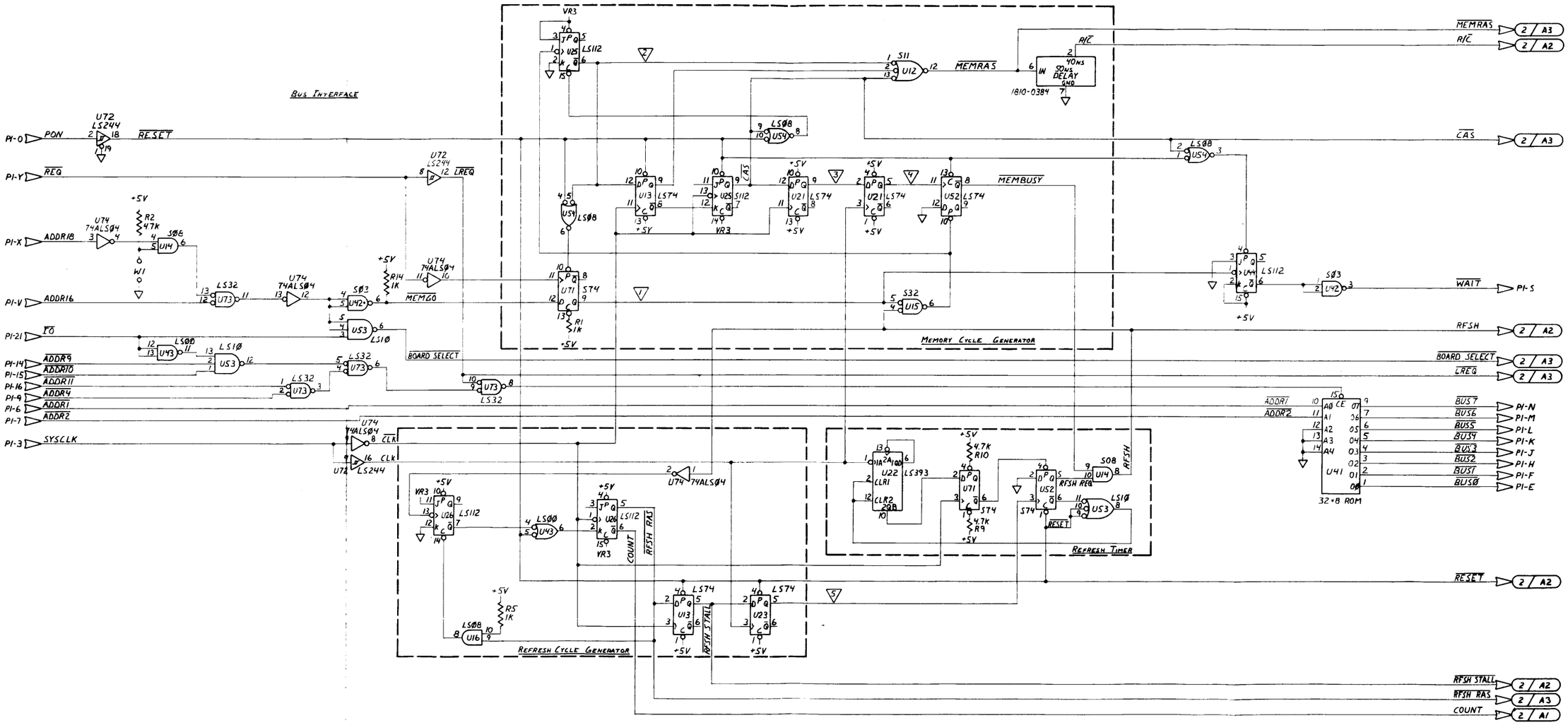


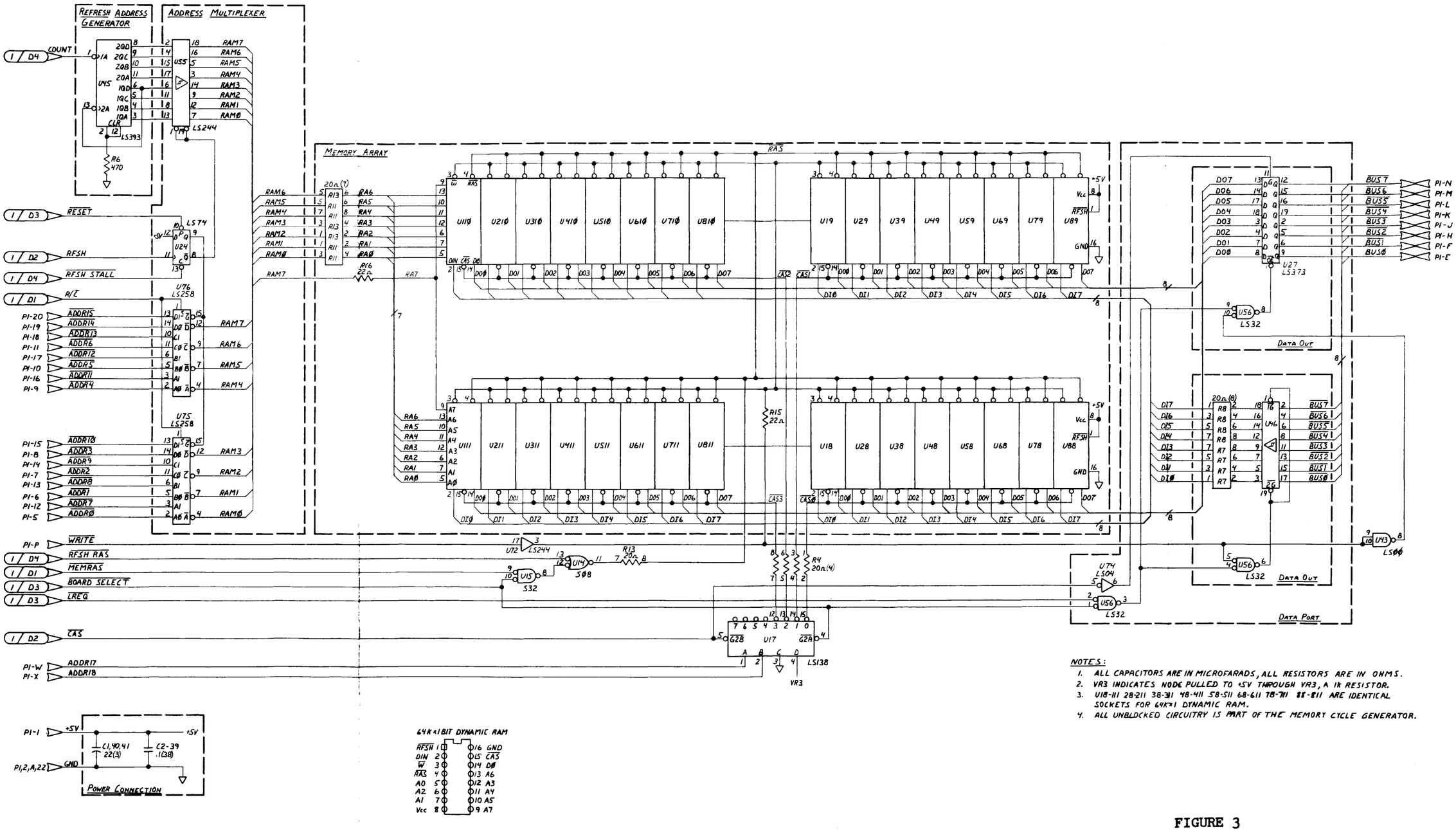
FIGURE 1
02640-60252 BLOCK DIAGRAM
JUN-23-81 13255-91252



NOTES:

1. ALL RESISTORS ARE IN OHMS.
2. VR3 INDICATES NODE PULLED TO +5V THROUGH VR3, A 1K RESISTOR.
3. ▽ REFERS TO A NODE ON THE TIMING DIAGRAM.

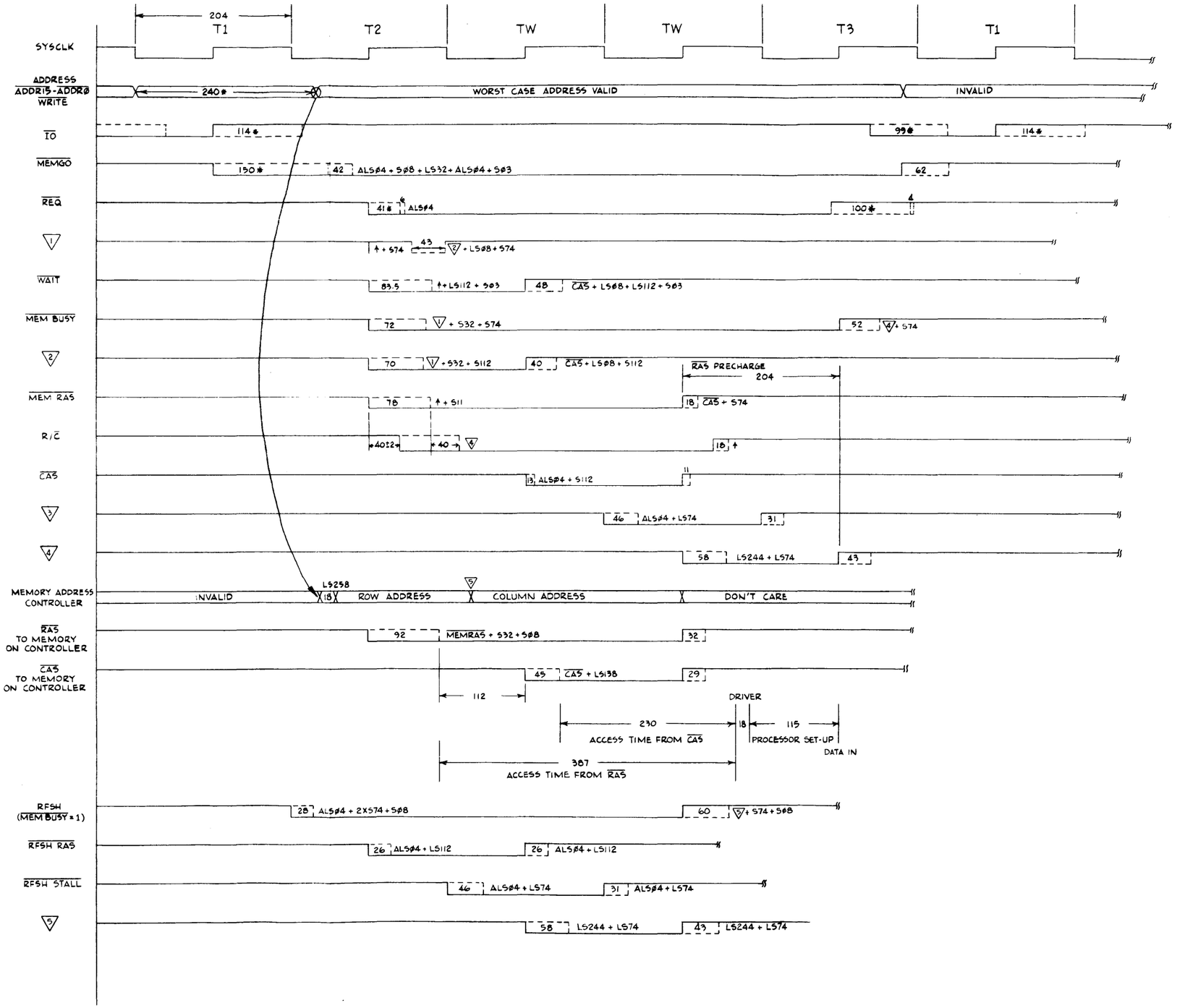
FIGURE 2
MEMORY CONTROLLER SCHEMATIC (PAGE 1)
JUN-23-81 13255-91252



NOTES:

1. ALL CAPACITORS ARE IN MICROFARADS, ALL RESISTORS ARE IN OHMS.
2. VR3 INDICATES NODE PULLED TO +5V THROUGH VR3, A 1K RESISTOR.
3. U18-11 28-21 38-31 48-41 58-51 68-61 78-71 88-81 ARE IDENTICAL SOCKETS FOR 64K×1 DYNAMIC RAM.
4. ALL UNBLOCKED CIRCUITRY IS PART OF THE MEMORY CYCLE GENERATOR.

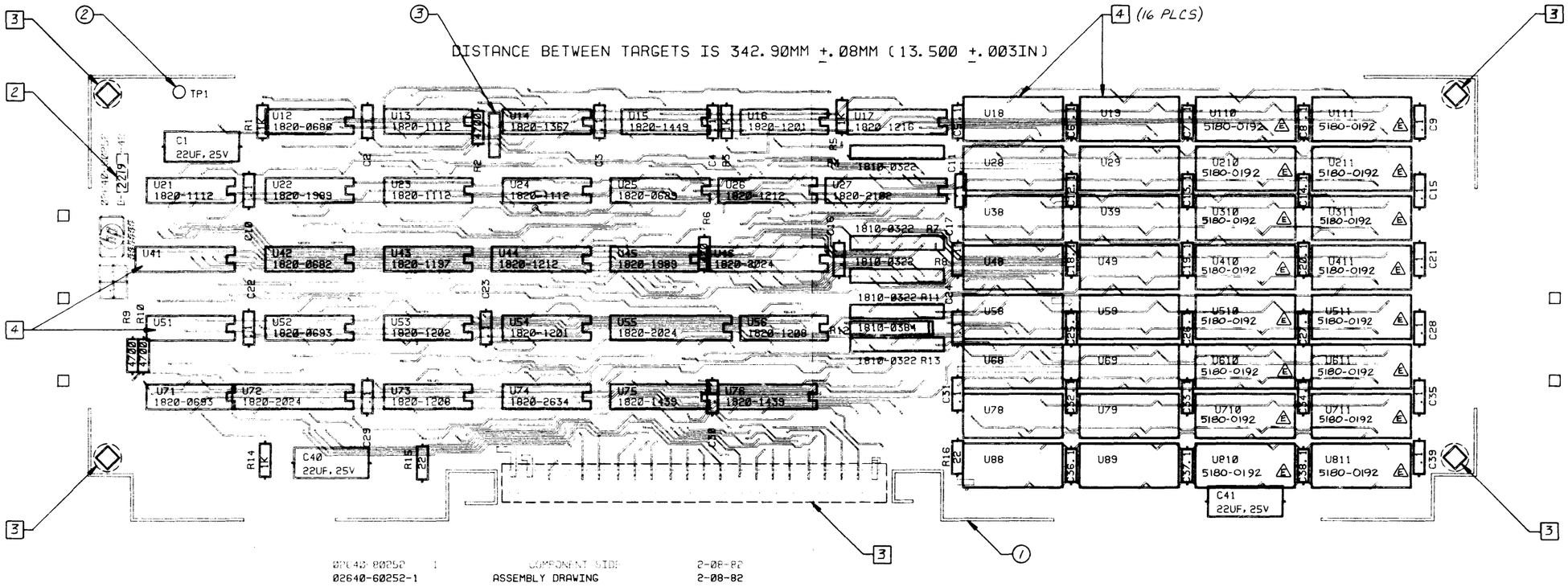
FIGURE 3
MEMORY CONTROLLER SCHEMATIC (PAGE 2)
JUN-23-81 13255-91252



NOTES:

1. ALL TIMES IN NANOSECONDS.
2. * INDICATES PROCESSOR DELAY. ALL OTHER DELAYS ARE DUE TO ON-BOARD LOGIC.
3. OUTPUT DATA LATCHED OFF BOARD.
4. R/C IS MEMRAS THROUGH A DELAY LINE:
   IF MEMRAS IS SLOW, R/C WILL BE SLOW
   AND VISE VERSA.
5. COLUMN ADDRESS AVAILABLE:
   24ns AFTER RAS EARLIEST.
   42ns AFTER RAS LATEST ON CONTROLLER BOARD.
   78ns AFTER RAS LATEST ON ARRAY BOARD.

FIGURE 4
MEMORY CONTROLLER TIMING
JUN-23-81 13255-91252



NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS
   ALL CAPACITANCE IN MICROFARADS
2. MARK DATE CODE (OPER 33)
3. MASK AS INDICATED PRIOR TO WAVE SOLDER.
4. ITEMS U41, U51, U18, U19, U28, U29, U38, U39, U48, U49, U58, U59, U68, U69, U78, U79, U88, AND U89 ARE NOT TO BE INSTALLED OR MASKED.

(E)

REFERENCE DWGS:

SCHEMATIC: D-02640-60252 - 51 & 52

FIGURE 5
MEMORY CONTROLLER COMPONENT LOCATION DIAGRAM
JUN-23-81 **13255-91252**

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02640-60252	4	1	RAM CONTROLLER, PCA	28480	02640-60252
C1	0180-2879	7	3	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C2	0160-4557	0	38	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C3	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C4	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C5	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C6	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C7	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C8	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C9	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C10	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C11	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C12	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C13	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C14	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C15	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C16	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C17	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C18	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C19	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C20	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C21	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C22	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C23	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C24	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C25	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C26	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C27	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C28	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C29	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C30	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C31	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C32	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C33	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C34	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C35	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C36	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C37	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C38	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C39	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C40	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C41	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
R1	0683-1025	9	4	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R2	0683-4725	2	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R3	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R4	1810-0322	9	5	NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R5	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R6	0683-4715	0	1	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R7	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R8	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R9	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R10	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R11	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R12	1810-0384	3	1	DELAY LINE TOTAL DELAY: 50 NS (TAPS AT	01961	20666
R13	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R14	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R15	0683-2205	9	2	RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R16	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
TP1	0360-0535	0	1	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U12	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U13	1820-1112	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U14	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U15	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U16	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U17	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U21	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U22	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U23	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U24	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U25	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U26	1820-1212	9	2	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
U27	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U42	1820-0682	5	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S03N
U43	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U44	1820-1212	9		IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
U45	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U46	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U52	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U53	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U54	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U55	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U56	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U71	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U72	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U73	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U74	1820-2634	1	1	IC INV TTL ALS HEX	01295	SN74ALS04N
U75	1820-1439	2	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
U76	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
				MISCELLANEOUS PARTS		
	1251-0697	5	2	EYELIT JUMPER	28480	1251-0697
	5180-0192	8	16	RAM- 64K	28480	5180-0192

MANUFACTURERS CODE LIST

AS OF 08/05/82

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
01961	PULSE ENGINEERING INC	SAN DIEGO	CA	92111
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH	NC	27604
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34344	MOTOROLA INC	FRANKLIN PARK	IL	60131
34371	HARRIS SEMICON DIV HARRIS-INTERTYPE	MELBOURNE	FL	32901
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
50088	MOSTEK CORP	CARROLLTON	TX	75006
55576	SYNERTEK	SANTA CLARA	CA	95051
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
91637	DALE ELECTRONICS INC	COLUMBUS	NE	68601