HP 13255

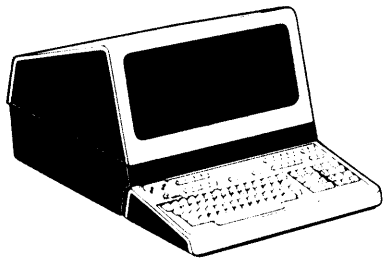
DISPLAY CONTROLLER MODULE

Manual Part No. 13255-91112

REVISED

SEP-10-77

DATA TERMINAL
TECHNICAL INFORMATION



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1.0 INTRODUCTION.

1.1 GENERAL DESCRIPTION.

The Display Controller Module is a high speed, special purpose I/O device. Its function is to provide drive signals to the CRT monitor, initiate data transfers from the terminal memory, and convert ASCII characters into a video signal.

The full screen capability of the display is 24 rows of 80 characters each. The minimum system can display 64 characters with one display feature--inverse video fields. An additional 64-character ROM may be added to the basic system for 128-character operation.

The Display Memory Access PCA (DMA) is that portion of the Display Controller Module which reads characters from the memory, buffers them in 80-character shift registers, and sends them to the Display Timing and Display Control PCA's. The operation of the DMA is controlled by the Display Timing and Display Control PCA's which initiate the transfer of rows of characters. It should be noted that there are two possible Display Control PCAs. Unless otherwise noted, reference to the Display Control PCA will apply to both assemblies.

1.2 PACKAGING.

The Display Controller Module consists of three PCA's, the Display Control, Display Timing, and the Display Memory Access PCA's. The DMA is adjacent to the Display Timing and Display Control PCA's and all three boards are connected together with the Top Plane Connector Assembly. The connection to the CRT monitor is made with the Sweep Cable Assembly from the CRT monitor to the Display Timing PCA.

1.3 CHARACTER FONT.

The basic character cell is a 9-dot by 15-scan line rectangle. Within this cell is the 7 x 9 character surrounded by one dot on either side for horizontal spacing, four scan lines below for lower case character descenders, and one scan line above and below for row-to-row spacing. The appearance of the characters is enhanced by means of a half-shift capability which generates smoother angles and curves by utilizing extra bits in the character ROMs. Each character scan line segment is stored in ROM as an 8-bit word. Seven of the bits (BIT1-BIT7) correspond to the dot positions D1-D7 within the character cell. The eighth bit (BIT0) controls whether the dots will occur during the normal dot times or will be delayed by one-half dot time, corresponding to a shift to the right by half a dot position on the screen. This increases the effective character resolution to 13 x 9; seven unshifted dot positions and six interstitial positions.

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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1.4 DISPLAY TIMING AND CONTROL-DMA INTERFACE.

The two communication paths between the DMA and the Display Timing and Control PCA's consist of the control signals between the PCA's and the returned data to be displayed.

In practice, a pair of odd/even character shift registers store one row each of characters and their enhancement fields. While a row is being scanned and displayed from one odd/even character shift register, the next row is being loaded into the other odd/even character shift register by the DMA. The odd/even character shift registers are toggled at the end of each row of characters.

1.5 DISPLAY CONTROLLER-PROCESSOR INTERFACE.

The Display Controller Module is the recipient of the cursor X and Y position on the screen. When the cursor is to be positioned to a new location, the processor outputs either a new cursor X or Y position. These positions are strobed into registers and are used to generate the visible cursor. No data or control paths exist from the display back to the processor.

In addition, the Display Controller Module receives two commands, one which turns the DMA on or off, and the other which turns the display on and off.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Display Controller Module is contained in tables 1.0 through 6.2.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60112	Display Control PCA	12.9 x 4.0 x 0.5	0.44
02640-60152	Display Control PCA	12.9 x 4.0 x 0.5	0.44
02640-60009	Display Memory Access PCA	12.5 x 4.0 x 0.5	0.38
02640-60088	Display Timing PCA	12.5 x 4.0 x 0.6	0.31
02640-60012	Top Plane Connector Assembly	N/A	N/A

Number of Backplane Slots Required: 3

Table 2.0 Reliability and Enviromental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 2.527 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 1600 mA	@ 68 mA	@ 27 mA	@ mA
(MODULE TOTAL)	(02640-60152 only) NOT APPLICABLE	(DMA PCA ONLY)	NOT APPLICABLE
115 volts ac		220 volts ac	
@ A		@ A	
NOT APPLICABLE		NOT APPLICABLE	
Clock Frequency: 21.060 MHz (DISPLAY TIMING AND CONTROL PCA'S) 4.915 MHz (DMA PCA)			

Table 4.0 Jumper Definitions

PCA Designation	Function	
	In	Out
Display Control PCA		
	128-character base set:	64-character base set:
W1	Assumes the 128-character option is installed. All 128 characters of the base set are displayed.	Upper case characters (ASCII 40-137B) are displayed. Control characters are displayed as blanks and ASCII 140-177B are upshifted to 100-137B.

Table 5.0 Connector Information - Display Control PCA

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3		Not Used
-4		
-5		
-6		
-7		
-8		
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11		Not Used
-12		
-13		
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17		Not used
-18		
-19		
-20		
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information - Display Control PCA (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not used
-C		
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L		Not Used
-M		
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R		Not used
-S		
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not used
-W		
-X		
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not used

Table 5.1 Connector Information - Display Timing PCA

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
P1, Pin 3 through Pin 21		Not Used
-22	GND	Ground Common Return (Power and Signal)
P1, Pin A	GND	Ground Common Return (Power and Supply)
-B		Not Used
-C		
-D		
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N		Not Used
-P		
-R		
-S		
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W		
-X		
-Y		
-Z		

Table 5.2 Connector Information - DMA PCA

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
-2	GND	Ground Common Return (Power and Signal)
-3	SYS CLK	4.915 MHz System Clock
-4	-12V	-12 Volt Power Supply
-5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
-6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
-7	$\overline{\text{ADDR2}}$	Negative True, Address Bit 2
-8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
-9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12	$\overline{\text{ADDR7}}$	Negative True, Address Bit 7
-13	$\overline{\text{ADDR8}}$	Negative True, Address Bit 8
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17	$\overline{\text{ADDR12}}$	Negative True, Address Bit 12
-18	$\overline{\text{ADDR13}}$	Negative True, Address Bit 13
-19		Not Used
-20		
-21		
-22	GND	Ground Common Return (Power and Signal)

Table 5.2 Connector Information - DMA PCA (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not used
-C		
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P		Not Used
-R		
-S	$\overline{\text{WAIT}}$	Negative True, Wait Control Line
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V		Not Used
-W	$\overline{\text{BUSY}}$	Negative True, Bus Currently Busy (Not Available)
-X		Not Used
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z		Not used

Table 5.3 Connector Information - Display Control PCA

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1	GND	Ground
-2	LC0	Scan Line Counter Bit 0
-3	LC2	Scan Line Counter Bit 2
-4	BIT0	ASCII Bit 0
-5	BIT2	ASCII Bit 2
-6	BIT4	ASCII Bit 4
-7	BIT6	ASCII Bit 6
-8	$\overline{BSS1}$	Negative True, Buffered Set Select Bit 1
-9	LCSEL	Lower Case Character ROM Select
-10	UCSEL	Upper Case Character ROM Select
-11	$\overline{DBIT1}$	Negative True, Dot 1 Output
-12	$\overline{DBIT3}$	Negative True, Dot 3 Output
-13	$\overline{DBIT5}$	Negative True, Dot 5 Output
-14	$\overline{DBIT7}$	Negative True, Dot 7 Output
-15	GND	Ground

Table 5.3 Connector Information - Display Control PCA (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P2, Pin A	GND	Ground
-B	LC1	Scan Line Counter Bit 1
-C	LC3	Scan Line Counter Bit 3
-D	BIT1	ASCII Bit 1
-E	BIT3	ASCII Bit 3
-F	BIT5	ASCII Bit 5
-H	$\overline{BSS0}$	Negative True, Buffered Set Select Bit 0
-J	$\overline{SET0}$	Negative True, Base Set Select
-K	$\overline{E1}$	Negative True, Base Set Enable
-L	$\overline{DBIT0}$	Negative True, Dot 0 Output
-M	$\overline{DBIT2}$	Negative True, Dot 2 Output
-N	$\overline{DBIT4}$	Negative True, Dot 4 Output
-P	$\overline{DBIT6}$	Negative True, Dot 6 Output
-R		Not Used
-S	GND	Ground

Table 5.4 Connector Information - Display Control PCA

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	$\overline{D0}$	Negative True, Character Dot Position 0
-2	$\overline{D6}$	Negative True, Character Dot Position 6
-3	$\overline{103}$	Negative True, Column Count 103
-4		Not Used
-5	$\overline{D1}$	Negative True, Character Dot Position 1
-6	CLEN	Cursor Line Enable
-7	VDR	Vertical Drive
-8	EVEN	Even Row
-9		Not Used
-10	GVS	Vertical Sync
-11	CYEN	Cursor Y Position True
-12		Not Used
-13		
-14		
-15		
-16	$\overline{BSS0}$	Negative True, Buffered Set Select Bit 0
-17	$\overline{BSS1}$	Negative True, Buffered Set Select Bit 1
-18		Not Used
-19	$\overline{BLNK}$	Negative True, Blanking
-20		Not Used
-21		
-22		

Table 5.4 Connector Information - Display Control (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	DSPY CLK	21.060 MHz Display Clock
-B	GND	Ground
-C	$\overline{D2}$	Negative True, Character Dot Position 2
-D	$\overline{D8}$	Negative True, Character Dot Position 8
-E	$\overline{14}$	Negative True, Scan Line Counter Reset
-F	L11	Scan Line Count 11
-H	VRTCLK	Scan Line Counter Clock
-J	VBLNK	Vertical Blanking
-K		Not Used
-L		
-M	INTSET	Display Controller Interrupt
-N	$\overline{CXS}$	Negative True, Cursor X Position Strobe
-P	$\overline{BIT0}$	Negative True, ASCII Bit 0
-R	$\overline{BIT1}$	Negative True, ASCII Bit 1
-S	$\overline{BIT2}$	Negative True, ASCII Bit 2
-T	$\overline{BIT3}$	Negative True, ASCII Bit 3
-U	$\overline{BIT4}$	Negative True, ASCII Bit 4
-V	$\overline{BIT5}$	Negative True, ASCII Bit 5
-W	$\overline{BIT6}$	Negative True, ASCII Bit 6
-X	$\overline{CYS}$	Negative True, Cursor Y Position Strobe
-Y	GND	Ground
-Z	$\overline{BITS}$	Negative True, Serial Bit Stream

Table 5.5 Connector Information Display Timing PCA

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1	$\overline{D0}$	Negative True, Character Dot Position 0
- 2	$\overline{D6}$	Negative True, Character Dot Position 6
- 3	$\overline{103}$	Negative True, Column Count 103
- 4	BUFCLK	Enhancement Buffer Clock
- 5	$\overline{D1}$	Negative True, Character Dot Position 1
- 6	CLEN	Cursor Line Enable
- 7	VDR	Vertical Drive
- 8		Not Used
- 9		
-10	GVS	Vertical Sync
-11	CYEN	Cursor Y Position True
-12	$\overline{BBL}$	Negative True, Buffered Blink
-13	$\overline{IV}$	Negative True, Inverse Video
-14	$\overline{BUL}$	Negative True, Buffered Underline
-15	$\overline{BUF\ HLF\ BRT}$	Negative True, Buffered Half-Bright
-16		Not Used
-17		
-18	$\overline{81}$	Negative True, Column Count 81
-19	$\overline{BLNK}$	Negative True, Blanking
-20	$\overline{XBITS2}$	Negative True, External Bit Stream 2
-21		Not Used
-22	$\overline{XBITS1}$	Negative True, External Bit Stream 1

Table 5.5 Connector Information - Display Timing PCA (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A	DSPY CLK	21.060 MHz Display Clock
-B	GND	Ground
-C	$\overline{D2}$	Negative True, Character Dot Position 2
-D	$\overline{D8}$	Negative True, Character Dot Position 8
-E		Not Used
-F	L11	Scan Line Count 11
-H	VRTCLK	Scan Line Counter Clock
-J	VBLNK	Vertical Blanking
-K	OCIRC	Line Buffer Circulation
-L	OCIRCEN	Line Buffer Circulation Enable
-M		Not Used
-N	$\overline{CXS}$	Negative True, Cursor X Position Strobe
-P		Not Used
-R		
-S		
-T		
-U		
-V		
-W		
-X	$\overline{CYS}$	Negative True, Cursor Y Position Strobe
-Y	GND	Ground
-Z	$\overline{BITS}$	Negative True, Serial Bit Stream

Table 5.6 Connector Information - DMA PCA

Connector and Pin No.	Signal Name	Signal Description
P3, Pin 1		
-2		
-3		Not Used
-4		
-5	$\overline{D1}$	Negative True, Character Dot Position 1
-6		
-7		Not Used
-8	EVEN	Even Row
-9	LBLOAD	Bus Buffer Load
-10	GVS	Vertical Sync
-11		
-12		Not Used
-13	$\overline{IV}$	Negative True, Inverse Video
-14		
-15		
-16		
-17		Not Used
-18		
-19		
-20		
-21	LOAD	Line Buffer Load
-22		Not Used

Table 5.6 Connector Information - DMA PCA (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P3, Pin A		Not Used
-B	GND	Ground
-C		Not Used
-D		
-E		
-F		
-H		
-J		
-K	OCIRC	Line Buffer Circulation
-L	OCIRCEN	Line Buffer Circulation Enable
-M	INTSET	Display Controller Interrupt
-N		Not Used
-P	$\overline{\text{BIT0}}$	Negative True, ASCII Bit 0
-R	$\overline{\text{BIT1}}$	Negative True, ASCII Bit 1
-S	$\overline{\text{BIT2}}$	Negative True, ASCII Bit 2
-T	$\overline{\text{BIT3}}$	Negative True, ASCII Bit 3
-U	$\overline{\text{BIT4}}$	Negative True, ASCII Bit 4
-V	$\overline{\text{BIT5}}$	Negative True, ASCII Bit 5
-W	$\overline{\text{BIT6}}$	Negative True, ASCII Bit 6
-X	$\overline{\text{CYS}}$	Negative True, Cursor Y Position Strobe
-Y	GND	Ground
-Z		Not Used

Table 5.7 Connector Information - Display Timing PCA

Connector and Pin No.	Signal Name	Signal Description
P4, Pin 1	VIDEO	Video
-2	BUF HLF BRT	Negative True, Buffered Half-Bright
-3	GND	Ground
-4	VDR	Vertical Drive
-5	HDR	Horizontal Drive
-6	GND	Ground

Table 6.0 Module Bus Pin Assignment - Display Control PCA

Function Performed: Output Cursor Y Position and Set Display On/Off

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0111)

Function Specifier: ADDR5 = 1

Data Bus Bit Interpretation:

B7 Display Off

B6 Not Used

B5 Not Used

B4 Cursor Y Position $\overline{BIT4}$

B3 Cursor Y Position $\overline{BIT3}$

B2 Cursor Y Position $\overline{BIT2}$

B1 Cursor Y Position $\overline{BIT1}$

B0 Cursor Y Position $\overline{BIT0}$

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
1	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.1 Module Bus Pin Assignments - Display Timing PCA

Function Performed: Output Cursor X Position

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0111)

Function Specifier: ADDR5 = 0

Data Bus Bit Interpretation:

B7 Not Used

B6 Cursor X Position $\overline{BIT6}$

B5 Cursor X Position $\overline{BIT5}$

B4 Cursor X Position $\overline{BIT4}$

B3 Cursor X Position $\overline{BIT3}$

B2 Cursor X Position $\overline{BIT2}$

B1 Cursor X Position $\overline{BIT1}$

B0 Cursor X Position $\overline{BIT0}$

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
1	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.2 Module Bus Pin Assignments - DMA PCA

Function Performed: DMA PCA On/Off

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0111)

Function Specifier: When asserted via $\overline{CYS}$ through the P3 connector, B6 turns off the DMA PCA

Data Bus Bit Interpretation:

B7 Not Used

B6 DMA Off

B5 Not Used

B4 Not Used

B3 Not Used

B2 Not Used

B1 Not Used

B0 Not Used

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
1	ADDR 10
1	ADDR 9
X	ADDR 8
X	ADDR 7
X	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

3.0 FUNCTIONAL DESCRIPTION - Display Timing and Display Control PCAs. Refer to the Display Timing and Display Control PCAs block diagram (figure 1), schematic diagrams (figures 2 and 17), timing diagrams (figures 4 through 7), component location diagrams (figures 8 and 18), and parts lists (02640-60012, 02640-60088, 02640-60112, and 02640-60152) located in the appendix.

The function of the Display Timing and Display Control PCAs is to generate the drive signals for the CRT monitor, to initiate data transfers from the display memory via the Display Memory Access PCA (DMA PCA), and to convert the ASCII characters into a serial video dot stream. The Display Timing and Display Control PCAs constitute the display controller and will be referred to as such in the functional description. The DMA PCA functional description is detailed in section 4.0.

3.1 DISPLAY CONTROLLER CLOCK - Display Timing PCA. The display controller clock is a 21.060 MHz crystal oscillator which provides a source of all display related timing. The display controller clock is a TTL square wave which results in a 60 Hz frame rate. In export systems, for use in 50 Hz power line environments, the crystal is changed to 17.550 MHz. When grounded, the TEST pin disables the oscillator for test purposes.

3.2 DOT GENERATOR - Display Control PCAs. The dot generator is a module 9 ring counter. Each output of the dot generator is a negative true signal of 47 nanoseconds duration. Each state of the ring counter corresponds to a dot position within each row of the character cell. The ring counter is clocked at the display clock rate and runs whenever power is applied to the Display Controller Module.

3.3 MODULO 104 COLUMN COUNTER - Display Timing PCA. The column counter is clocked by the positive edge of $\overline{D0}$. It is a binary counter which resets when it reaches count 103. The reset signal, $\overline{103}$, is used by other circuits. Counts 1 through 80 of the counter correspond to the 80 visible columns on the screen and count 0 and counts 81 through 103 correspond to the horizontal retrace time.

3.4 SCAN LINE COUNTER - Display Control PCAs. The scan line counter (U27) is a modulo 15 binary counter which counts the 15 scan lines (from 0 to 14) required for each row of characters. It is clocked by VRTCLK which is generated by the horizontal logic block on the Display Timing PCA.

The Scan Line Counter Reset signal ($\overline{14}$) is used by other circuits within the display controller.

3.5 MODULO 25 ROW COUNTER - Display Control PCAs. The row counter is a binary counter clocked by $\overline{14}$. It counts from 0 to 23 which correspond to visible rows 0 through 23 respectively. Count 24 constitutes the vertical retrace time. On Display Control PCA 02640-60112, U42 counts the 4 least significant bits and U24, Pin 10 is the MSB of the counter. During the 24th row, the counter reset signal at U23, Pin 6 is inverted by U22, Pin 10 and is used as VBLNK to blank the display during vertical retrace.

On Display Control PCA 02640-60152, U42 counts the 4 least significant bits and U33, Pin 10 is the MSB of the counter. During the 24th row, the counter reset signal at U31, Pin 6 is inverted by U21, Pin 4 and is used as VBLNK to blank the display during vertical retrace.

3.6 HORIZONTAL LOGIC - Display Timing PCA.

3.6.1 The horizontal logic along with the video logic on the Display Control PCA, generates those signals which are needed to control both the DMA PCA and the CRT monitor.

3.6.2 The Horizontal Drive signal (HDR) is a square wave which drives the horizontal deflection circuitry of the sweep. It is set high by $\overline{24}$ (the twenty-fourth column count) acting on U44, Pin 13. HDR goes low when $\overline{81}$ (the eighty-first column count) sets U44 at Pin 10. The high-to-low transition initiates horizontal retrace.

3.6.2.1 Negative Horizontal Blanking ($\overline{\text{HBLNK}}$) at U44, Pin 6 occurs at the end of the visible portion of scan line. $\overline{\text{HBLNK}}$ goes low as a resultof $\overline{\text{D1}}$ at U29, Pin 8 and flip-flop U44 is set on the falling edge of $\overline{\text{D1}}$ during column 81. The $\overline{\text{HBLNK}}$ signal goes high at the startof a scan line, thus unblanking the screen by means of the trailing edge of $\overline{\text{D8}}$ during column 0.

3.6.2.2 The Line Buffer Circulation signal (0CIRC) occurs once per visible column. It clocks the data in the odd/even character shift register, circulating its character sychronously with the column counts on the raster. 0CIRC is generated by a simple R-S flip-flop comprised of U37, Pin 6 and U37, Pin 8. 0CIRC runs continuously and is gated by 0CIRCEN on the DMA PCA. 0CIRCEN gates exactly 80 0CIRC pulses to the odd/even character shift register currently available to the display controller. Each 0CIRC pulse rotates the ASCII character codes in the odd/even character shift register one position. Signal $\overline{D2}$, during column 103 toggles $\overline{0CIRCEN}$ at U45, Pin 7 causing it to go low. 0CIRCEN goes low at the end of the visible portion of the scan line by the action of U47, Pin 8 via the trailing edge of 0CIRC during column 78. Considering that one character time is required to access the ASCII from the odd/even character shift register, 0CIRC at columns 103 and 78 results in characters in columns 0 and 79 respectively.

3.6.2.3 Display enhancements must be buffered for one character column while the character's dots are accessed from the character ROMs. This buffering is clocked by BUFCLK, a strobe signal which occurs at dot position 8 time during the visible portion of the horizontal sweep.

3.6.2.4 The scan line counter is clocked by the leading edge of VRTCLK, a signal which is set by $\overline{81}$ and reset by the leading edge of $\overline{D1}$ during column 103. Since the leading edge of VRTCLK occurs during horizontal blanking, the display is not disturbed by the changing statesof the scan line counter, and subsequently, the modulo 25 row counter.

3.7 VIDEO LOGIC - Display Control PCA (02640-60112)
Refer to Section 3.23 for functional description of 02640-60152 PCA.

3.7.1 The video logic, along with the horizontal logic on the Display Timing PCA generates those signals which are needed to control both the DMA and the CRT monitor.

3.7.2 The Vertical Drive signal (VDR) is generated by U33, Pin 7. VDR is normally high, going low for 14 scan lines within which time the CRT monitor must accomplish vertical retrace. VDR goes low at the end of row 23 (the last visible row on the screen) by the action of U43, Pin 6 on the clock (Pin 13) of U33. U43, Pin 6 is high during rows 22 and 23 only. U23, Pin 11 goes low and resets VDR high at the start of the 15th scan line of row 24. This insures that the integrator in the

vertical section of the CRT monitor has one scan line's time to begin it's ramp before unblanking the screen at the end of row 24. Vertical blanking occurs during the horizontal blanking interval. It occurs at the bottom of the screen after the last scan line of row 23 and resets after the 15th scan line of row 24. VBLNK is the inverse of the row counter reset signal at U22, Pin 10.

3.7.2.1 Two odd/even character shift registers are used; one accumulates a line of ASCII and the other displays the previously accumulated line. Line toggling occurs on the DMA PCA under control of EVEN, a signal which is true when the line being displayed is even in row count. U23, Pin 8 inverts the LSB of the row count to generate EVEN. Thus, when row 8 is being displayed, the DMA PCA is loading row 9 and EVEN is true.

3.7.2.2 After EVEN toggles the odd/even character shift registers, INTSET initiates the next burst of data transfers on the DMA PCA. INTSET is a short pulse occurring shortly after EVEN changes states. It occurs during scan line 0, column 103 of all rows, 0 through 23.

3.7.2.3 Once per frame, a Vertical Sync pulse (GVS) is sent to the DMA PCA to insure synchronization between the display top of screen and the DMA's memory pointer. GVS is generated at U43, Pin 8 by gating one INTSET pulse during row 23.

3.8 CHARACTER SELECT LOGIC - Display Control PCA (02640-60112)
Refer to Section 3.24 for functional description of 02640-60152 PCA.

3.8.1 The character select logic maps the lower case ASCII codes onto the upper case ASCII codes when only the base 64-character ROM is installed. When the 128-character option is added, it allows all 128 characters to be mapped into the two ROMs.

3.8.2 When W1 is not installed, the upper case character ROM (U310) is enabled for ASCII codes 40B to 137B. When lower case codes (140-177B) are received they are mapped to ASCII 100B-137B. When control codes (00-37B) are received, they are routed to the nonexistent lower case ROM and appear as blanks. When the 128-character option is installed, W1 is also inserted allowing ASCII codes 00-37B and 140-177B to be routed to the lower case ROM, and thus displaying all 128 characters.

The Chip Enable signal $\overline{E1}$ is asserted whenever the base character set is selected by U23, Pin 3. Whenever an alternate character set is selected, $\overline{E1}$ is false and the base set is not selected.

3.9 CHARACTER ROMS - Display Control PCA (02640-60112). Refer to Section 3.25 for functional description of 02640-60152 PCA. Bipolar ROMs are used for the storage of the dot images of the character set. Each ROM is 1K words in length by 8-bits wide. The minimum system has only the upper case ROM (U310) installed. When the 128-character option is added, the lower case ROM (U28) must also be installed.

3.10 DOT SHIFT GENERATOR - Display Control PCA (02640-60112). Refer to

i.e., $\overline{\text{DBIT0}}$ is false, then seven clock pulses are sent. When $\overline{\text{DBIT0}}$ is true, six clock pulses are transmitted after an initial delay of one-half clock period, thus resulting in a shift to the right of one-half dot. The clock pulse occurring during dot position 8 time is always inserted in the SHFT line by U37, Pin 6. Its function is to parallel load the data from the character ROMs into the parallel-to-serial converter when the load line at U510, Pin 15 is held low by $\overline{\text{D8}}$.

3.11 PARALLEL-TO-SERIAL CONVERTER - Display Control PCA (02640-60112). Refer to Section 3.27 for functional description of 02640-60152 PCA. During dot position 8 time, the parallel-to-serial converter is parallel loaded with the dot information for the next character by one clock pulse on the SHFT signal.

Depending on the state of $\overline{\text{DBIT0}}$, either 7 clock pulses occurring during dot time 1 through 7, or 6 clock pulses occurring during dot times 1 1/2 through 6 1/2 will be sent to U510 to serially shift the information out at Pin 13 as $\overline{\text{BITS}}$.

3.12 INVERSE VIDEO FLIP-FLOP - Display Timing PCA. The Inverse Video flip-flop buffers the inverse video enhancement for one character time while the character to which it will be applied has its dots fetched from the character ROMs. It is clocked at dot position 0 time by BUFCLK from U28, Pin 8.

3.13 VIDEO GENERATOR LOGIC - Display Timing PCA.

3.13.1 The video generator logic combines the internal and external serial bit streams, blinking signals, cursor information, and display enhancement information to generate video and half-bright signals.

3.13.2 Three serial bit streams, $\overline{\text{BITS}}$, $\overline{\text{XBITS1}}$, and $\overline{\text{XBITS2}}$ are merged at U18, Pin 6 to form a composite serial stream. This is merged with the cursor at U19, Pin 5 and blinking at U29, Pin 4. Finally, it is stretched by video stretcher Q2 and inverted if necessary at U310, Pin 6. The bit stream is blanked at U28, Pin 6 and becomes the VIDEO signal. Half-bright fields are stretched by Q4 and are applied to the CRT monitor by U38, Pin 6.

3.14 MODULO 12 COUNTER - Display Timing PCA. The modulo 12 counter divides the frame rate by 12, beginning the BLINK signal generation. The counter is a synchronous, 12-state counter clocked by the GVS signal. Its output is at 4 times the blink rate of 1.25 Hz for the 60 Hz frame rate.

3.15 BLINK GENERATOR - Display Timing PCA.

3.15.1 The blink generator produces the necessary signals for the blink function, cursor blink rate, and cursor blink inhibit.

3.15.2 The basic blink rate is achieved by dividing the output of the modulo 12 counter by 4. U43, Pin 9 outputs the BLINK signal to the video generator logic. The basic cursor blink rate is set at twice the blink enhancement rate or at half the output rate of the modulo 12 counter. U43, Pin 5 drives U29 along with the blink inhibit one-shot (U42) to produce the final Cursor Blink signal at U29, Pin 3. Whenever the cursor is updated, the one-shot fires, thus inhibiting blinking until it times out. This results in cessation of cursor blinking while it is moving and prevents "cursor galloping". Whenever one-shot U42 fires, flip-flop U36 is enabled and divides the VDR signal by 2 and thus chops the $\overline{\text{CURSOR REFRESH}}$ line at U36, Pin 6. This prevents the perception of overlapping cursors when it is moved on the screen.

3.16 BUS DECODER NETWORK - Display Control PCA. The bus decoder network decodes the module address and produces $\overline{\text{CXS}}$ and $\overline{\text{CYS}}$ in order to strobe the cursor X and Y positions respectively into latches when $\overline{\text{REQ}}$ is pulsed.

3.17 CURSOR X HOLDING REGISTER - Display Timing PCA. The cursor X holding register is a 7-bit latch which holds the cursor X position. The cursor X register is divided into two portions. The four LSB are held in U59 while the three MSB are in U510. The $\overline{\text{CXS}}$ signal strobes the new cursor X position into the latches.

3.18 CURSOR Y HOLDING REGISTER - Display Control PCA. The cursor Y holding register is a 6-bit latch which holds the cursor Y position and the display on/off control line. The 5 LSB of the holding register hold the 5-bit cursor Y position while the MSB holds the display on/off control line, $\overline{\text{BLNK}}$. The $\overline{\text{CYS}}$ signal strobes the new cursor Y position into the latch.

3.19 CURSOR X COMPARATOR - Display Timing PCA. The cursor X comparator is divided into two parts and compares the cursor X position against the column being scanned. The six LSB of the cursor position are compared against the six LSB of the column counter by U410. The MSB of both the cursor X position and the column counter are compared by U310, Pin 11.

3.20 CURSOR Y COMPARATOR - Display Control PCA. The cursor Y comparator compares the cursor Y position against the row being scanned. It is a 5-bit comparator whose output is true when the instantaneous row count is equal to the cursor Y position held in the latch (U51).

3.21 CURSOR LINE ENABLE LOGIC - Display Control PCA. The cursor line enable logic generates the Cursor Line Enable signal (CLEN) which is true whenever the scan line counter is at either scan lines 11 or 12. This signal is used to gate the cursor so that it appears only during those scan lines.

3.22 CURSOR GENERATOR - Display Timing PCA.

3.22.1 The cursor generator combines CLEN with the outputs of both the cursor X and cursor Y comparators. When all three are true, it outputs a cursor signal during the next column count.

3.22.2 The outputs of the cursor X and Y comparators are merged at U58, Pin 8. When all three signals are true, flip-flop U45 is allowed to output a signal during the next column appearing on the screen. This signal is in turn gated by CLEN and $\overline{\text{CURSOR REFRESH}}$ to form the final cursor signal at U18, Pin 8.

3.23 Video Logic - Display Control PCA (02640-60152)

3.23.1 The video logic, along with the horizontal logic on the Display Timing PCA generates those signals which are needed to control both the DMA and the CRT monitor.

3.23.2 The Vertical Drive signal (VDR) is generated by U21, Pin 6. VDR is normally high, going low for 14 scan lines within which time the CRT monitor must accomplish vertical retrace. VDR goes low at the end of row 23 (the last visible row on the screen) by the action of U46, Pin 6 which is clocked into U23, Pin 3, at the end of scan line 14. U47, Pin 6 is high during rows 22 and 23 only. U31, Pin 8 goes low and resets VDR high at the start of the 15th scan line of row 24. This insures that the integrator in the vertical section of the CRT monitor has one scan line's time to begin it's ramp before unblanking the screen at the end of row 24. Vertical blanking occurs during the horizontal blanking interval. It occurs at the bottom of the screen after the last scan line of row 24. VBLNK is the inverse of the row counter reset signal at U21, Pin 4.

3.23.2.1 Two odd/even character shift registers are used; one accumulates a line of ASCII and the other displays the previously accumulated line. Line toggling occurs on the DMA PCA under control of EVEN, a signal which is true when the line being displayed is even in row count. U31, Pin 3 inverts the LSB of the row count to generate EVEN. Thus, when row 8 is being displayed, the DMA PCA is loading row 9 and EVEN is true.

3.23.2.2 After EVEN toggles the odd/even character shift registers, INTSET initiates the next burst of data transfers on the DMA PCA. INTSET is a short pulse occurring shortly after EVEN changes states. It occurs during scan line 0, column 103 of all rows, 0 through 23.

3.23.2.3 Once per frame, a Vertical Sync pulse (GVS) is sent to the DMA PCA to insure synchronization between the display top of screen and the DMA's memory pointer. GVS is generated at U47, Pin 12 by gating one INTSET pulse during row 23.

3.24 CHARACTER SELECT LOGIC - Display Control PCA (02640-60152)

3.24.1 The character select logic maps the lower case ASCII codes onto the upper case ASCII codes when only the base 64-character ROM is installed. When the 128-character option is added, it allows all 128 characters to be mapped into the two ROMs.

3.24.2 When W1 is not installed, the upper case character ROM (U59) is enabled for ASCII codes 40B to 137B. When lower case codes (140-177B) are received they are mapped to ASCII 100B-137B. When control codes (00-37B) are received, they are routed to the nonexistent lower case ROM and appear as blanks. When the 128-character option is installed, W1 is also inserted allowing ASCII codes 00-37B and 140-177B to be routed to the lower case ROM, and thus displaying all 128 characters.

The Chip Enable signal $\overline{E1}$ is asserted whenever the base character set is selected by U46, Pin 3, and the ASCII character to the ROM is valid. While the next character is being shifted from the line buffer during D0-D4, $\overline{E1}$ is held false by the wired AND at U31, Pin 12. Disabling the ROMs avoids tri-state conflict of the character ROM outputs as LCSEL and UCSEL change. Whenever an alternate character set is selected, $\overline{E1}$ is false and the base set is not selected.

3.25 CHARACTER ROMS - Display Control PCA (02640-60152). SOS/MOS ROMs are used for the storage of the dot images of the character set. Each ROM is 1K words in length by 8-bits wide. The minimum system has only the uper case ROM (U59) installed. When the 128-character option is added, the lower case ROM (U58) must also be installed.

3.26 DOT SHIFT GENERATOR - Display Control PCA (02640-60152). The dot shift generator gates either 6 or 7 clock pulses to the clock input line (Pin 7) of the parallel-to-serial converter (U57) in the form of the SHFT signal. When the scan line segment of a character is not to be half-shifted, i.e., DBITO is false, then seven clock pulses are sent. When DBITO is true six clock pulses are transmitted after an initial delay of one-half clock period, thus resulting in a shift to the right of one-half dot. The clock pulse occurring during dot position 8 time is always inserted in the SHFT line by U27, Pin 3. Its function is to parallel load the data from the character ROMS into the parallel-to-serial converter when the load line at U57, Pin 15 is held low by D8.

3.27 PARALLEL-TO-SERIAL CONVERTER- Display Control PCA (02640-60152). During dot position 8 time, the parallel-to-serial converter is parallel loaded with the dot information for the next character by one clock pulse on the SHFT signal. Depending on the state of $\overline{DBITO}$, either 7 clock pulses occurring during dot time 1 through 7, or 6 clock pulses occurring during dot times 1 1/2 through 6 1/2 will be sent to U57 to serially shift the information out at Pin 13 as $\overline{BITS}$.

4.0 FUNCTIONAL DESCRIPTION - DMA PCA. Refer to the DMA PCA block diagram (figure 10),schematic diagram (figure 11),timing diagrams (figures 12 through 14), DMA data encoding (figure 15), component location diagram (figure 16), and parts list (02640-60009) located in the appendix.

The function of the Display Memory Access PCA (DMA) is to read charac-

ters from the display memory and to load them into odd/even character shift registers. Two shift registers are used concurrently; while one is being loaded by the DMA the other is circulated 15 times by the display controller. At the end of a row, shift registers are toggled and the start of data transfer is again initiated by the display controller.

In the process of obtaining characters from the memory, the DMA edits the characters it receives and performs the following functions:

Link	An additional byte is fetched from memory and becomes the next location address from which data is to be read.
End Of Line	The remainder of the line is written with blanks.
End Of Page	The remainder of the page is written with blanks.
Flags	No operation.
Display Enhancements	The DMA uses $\overline{\text{BUS1}}$ as the inverse video bit and passes it to the display controller.
Character	The 7-bit code represents 1 of 128 characters in the character generator.

Figure 15 tabulates the coding of the control, link, and flag information in the data bytes.

4.1 80-CHARACTER COUNTER - DMA PCA.

4.1.1 The counter (U19 and U110) is used to keep track of the number of displayable characters fetched from memory. When 80 characters have been loaded into the odd/even character shift register, it turns off the bus control logic.

4.1.2 The modulo 80 counter is reset to "0" by the INTSET signal at the start of a new row by the display controller. This causes U38, Pin 11 to go high, thereby allowing the bus control logic to begin sequencing. As displayable characters are loaded into the appropriate shift registers (determined by EVEN) the counter is incremented by the LOAD signal. When the terminal count of 80 is reached U38, Pin 11 goes low and shuts off the bus control logic.

4.2 UPPER AND LOWER BYTE ADDRESS COUNTER - DMA PCA.

4.2.1 The upper and lower byte address counter is a 14-bit down counter. Its output appears on the terminal address bus and it points to the current byte of memory being accessed. The counter counts down under control of the bus control logic. When a link byte is fetched, it is loaded into the upper byte counter (U36 and U37) while the next byte in memory is loaded into the lower byte counter (U34 and U35). These, together, constitute the 14-bit address of the first character of the next block of memory.

4.2.1.1 The receipt of a GVS pulse from the display controller clears out the counter, which due to the negative true address bus, forces the next fetch from address 37777B, which is the pointer to the first displayable character on the screen.

4.2.1.2 Receipt of an end of line (EOL) or end of page (EOP) byte inhibits further counting until a new row or page is initiated respectively. The counter output is 3-state under command of the bus control logic.

4.3 HOLDING REGISTER - DMA PCA.

4.3.1 The holding register is an 8-bit latch which stores the most recently read byte from memory.

4.3.2 The holding register receives its input from the terminal data bus under command of the data control logic (U48, Pin 8). When an EOL or EOP is detected, a pseudo read operation is performed. The data bus is then read as "0" and, with the output of U26, Pin 11 being low, an ASCII "blank" character is loaded into the holding register.

4.3.2.1 The output of the holding register is decoded into either control or displayable characters. If the outputs are control signals then the selected flip-flops are set in the data control logic. Otherwise, the character is loaded from the holding register into the appropriate shift register.

4.3.2.2 When a link is detected in the holding, register another fetch is initiated. The contents of the holding register and the data bus outputs are then simultaneously loaded into the upper and lower byte registers respectively. The holding register is cleared at power on (PWR ON).

4.4 DISPLAY FUNCTION ENCODER AND DECODER - DMA PCA.

4.4.1 Encoded ASCII, control, link, EOP, EOL, and flag data in the holding register are decoded by the display function encoder and decoder logic.

4.4.2 The data in the holding register represents ASCII characters, display control information, links, EOP, EOL, or flags as shown in figure 15. The output of the display function encoder (U33) is a binary encoder of the highest order input. This is subsequently decoded by U28 (a 3-to-8 line decoder) into five signals: $\overline{\text{CONTROL}}$ (U28, Pin 15), $\overline{\text{CHARACTER}}$ (U28, Pin 7), $\overline{\text{EOP}}$ (U28, Pin 9), $\overline{\text{EOL}}$ (U28, Pin 10), and $\overline{\text{LINKI}}$ (U38, Pin 3). For any byte in the holding register, one of the five outputs will be true depending on the type of information in the register.

4.5 DATA CONTROL LOGIC - DMA PCA.

4.5.1 The data control logic receives bus timing related signals from the bus control logic, and, as a function of the display function decoder, it controls the upper and lower byte address counters, the holding register, the Inverse Video flip-flop, and the odd/even character shift register.

4.5.2 The Byte Register Clock signal (U48, Pin 8) enters the data bus contents into the holding register at the leading edge of the Wait state (011). If the byte is an ASCII character (U28, Pin 7 low) then U29, Pin 6 is enabled. At the Release state (001) of the bus control logic U29, Pin 4 goes high and on its trailing edge loads the character into the odd/even character shift register enabled by EVEN. LOAD also increments the 80-character counter provided it has not yet reached 80. If it does reach 80, then U36, Pin 11 inhibits the bus control logic at its Idle state (000).

4.5.2.1 Any display ennancements (inverse video half-bright, underline, and blinking) stored in the ennancement flip-flops are loaded in parallel with the ASCII characters into the shift registers. Only the Inverse Video flip-flop is resident on the DMA (U27, Pin 5). The other three are on the Display Enhancement PCA (see Display Expansion Module, section 13255-91024 of this manual).

4.5.2.2 If the byte in the holding register is a display control byte, then U26, Pin 1 is low, thus forcing U26, Pin 3 low and LBLOAD at U29, Pin 10 clocks the data into the display enhancement flip-flops. The DMA's Inverse Video flip-flop is set by LBLOAD if $\overline{BUS1}$ is true. LBLOAD does not increment the 80-character counter and another byte is fetched from memory.

4.5.2.3 If the byte in the holding register is an EOL, EOP, or Link, then at the end of the Release state (001) CLK LOGIC sets respective flip-flops U210, Pin 6; U210, Pin 8; and U310, Pin 5. The setting of U210, Pin 6 (EOL) or U210, Pin 8 (EOP) forces U29, Pin 13, and thus disables the upper and lower byte address counter. U29, Pin 13 simulates a control command at U26, Pin 2 and prevents $\overline{REQ}$ from being asserted at U47, Pin 11. This in turn causes the bus data to always be high for all subsequent reads. By virtue of U26, Pin 11, the null is converted to an ASCII blank (040B) which is loaded into the odd/even character shift register. This is continued until either the end of the line or page is reached. The simulated control command at U26, Pin 2 also loads "0" into the display enhancement flip-flops, thus clearing them. The EOL flip-flop (U210, Pin 6) is cleared at the end of the line by $\overline{80}$, the terminal count signal. The EOP flip-flop (U210, Pin 8) is cleared by GVS.

4.5.2.4 If a link is received, then U310, Pin 5 goes low and inhibits the clocking of the holding register by disabling BYTE REG CLK at U48, Pin 8. This prevents the loss of the most significant byte of the link address from the holding register. $\overline{LINK}$ at U310, Pin 5 also enables the parallel loading of the address counters (U34 through U37) at Pin 9. The leading edge of the BUS INPUT CLK (U410, Pin 5) signal at the start of the bus Release state (001) loads the most significant byte of the link from the holding register and the least significant byte from the data bus after the next read from memory.

4.6 BUS CONTROL LOGIC - DMA PCA.

4.6.1 The bus control logic is a 6-state sequential machine which periodically grabs control of the terminal bus and transfers 80 displayable characters into the odd/even character shift registers. (Refer to the Backplane Module, section 13255-91001, for detailed discussion of bus protocol.)

4.6.2 The six states of the bus control logic are held by U410, Pin 8, U410 Pin 6; and U310, Pin 8, which form a Johnson counter. In the idle state (000) all three flip-flop outputs are low. Upon receipt of an INTSET signal from the display controller, the terminal count signal ($\overline{80}$) goes high at U38, Pin 11 enabling U39, Pin 12 if the DMA PCA is also on (U27, Pin 9 high). This clocks the bus control logic to the Bus Bid state, (100). Terminal bus signal PRIOR OUT is pulled low by U48, Pin 11 and if PRIOR IN is high, then U39, Pin 8 goes high and the bus is obtained (state 110). $\overline{\text{BUSY}}$ is pulled low by U47, Pin 8 and the upper and lower byte address counter is put out onto the address bus by U38, Pin 8 enabling the 3-state address drivers.

4.6.2.1 The Request state (111) is the same as (110) with the addition of $\overline{\text{REQ}}$ going low by means of U47, Pin 11, given that neither EOL or EOP is set. The bus control logic then waits until $\overline{\text{WAIT}}$ goes high. When this occurs U49, Pin 8 resets U410, Pin 8 on the next clock pulse, and the bus control logic goes to the official Wait state (011) where PRIOR OUT is released.

4.6.2.2 The bus control logic finally goes to the Release state (001) which releases $\overline{\text{BUSY}}$ and the address bus. Then it returns to the Idle state (000). If the character counter has not reached the terminal count and the DMA is still on (U29, Pin 9 is still set), then the DMA grabs the bus again.

4.7 ODD/EVEN CHARACTER SHIFT REGISTERS - DMA PCA.

4.7.1 The odd/even character shift register is comprised of a pair of ping-ponged shift registers, each 80 characters in length by 8 bits in width. Each shift register stores a row of ASCII characters and the inverse video enhancement for each character.

4.7.2 The selection of the shift register to be loaded by the DMA PCA is controlled by the EVEN signal. The other shift register (the one not being loaded, but rather being rotated) is controlled by the display controller.

4.7.2.1 U32 and U52 comprise the most and least significant four bits of the even shift register. Similarly, U21 and U41 form the odd shift register. The EVEN signal and its complement, when true, control which shift register is to be recirculated by the display controller. Conversely, the other shift register is loaded by the DMA.

4.7.2.2 Circulation is accomplished by OCIRC and OCIRCEN which rotate the contents of the displayed shift register through all 80 characters, 15 times, once per scan line of a row. The loaded shift register has data clocked in via the DMA's LOAD signal. The output of the displayed shift register goes to the selector latch.

4.8 SHIFT REGISTER CONTROL - DMA PCA. The shift register control block is a combinatorial logic circuit which routes the circulation signals and LOAD to the appropriate shift register under control of EVEN. OCIRCEN gates 80 OCIRC pulses at U26, Pin 6. These are applied to data selector (U22) and appear at U12, Pin 10 or U12, Pin 12 if EVEN is low or high, respectively. Conversely, the LOAD signal appears at the other output.

4.9 SELECTOR LATCH - DMA PCA. The selector is a latching data selector controlled by the EVEN signal, which outputs either the even or the odd row shift register to the display bus. The output of the displayed shift register is selected by U31 and U51 and is latched by clock pulse $\overline{D1}$ (U12, Pin 2). The stable output of the latch is then applied to the display bus top plane connector, P3.

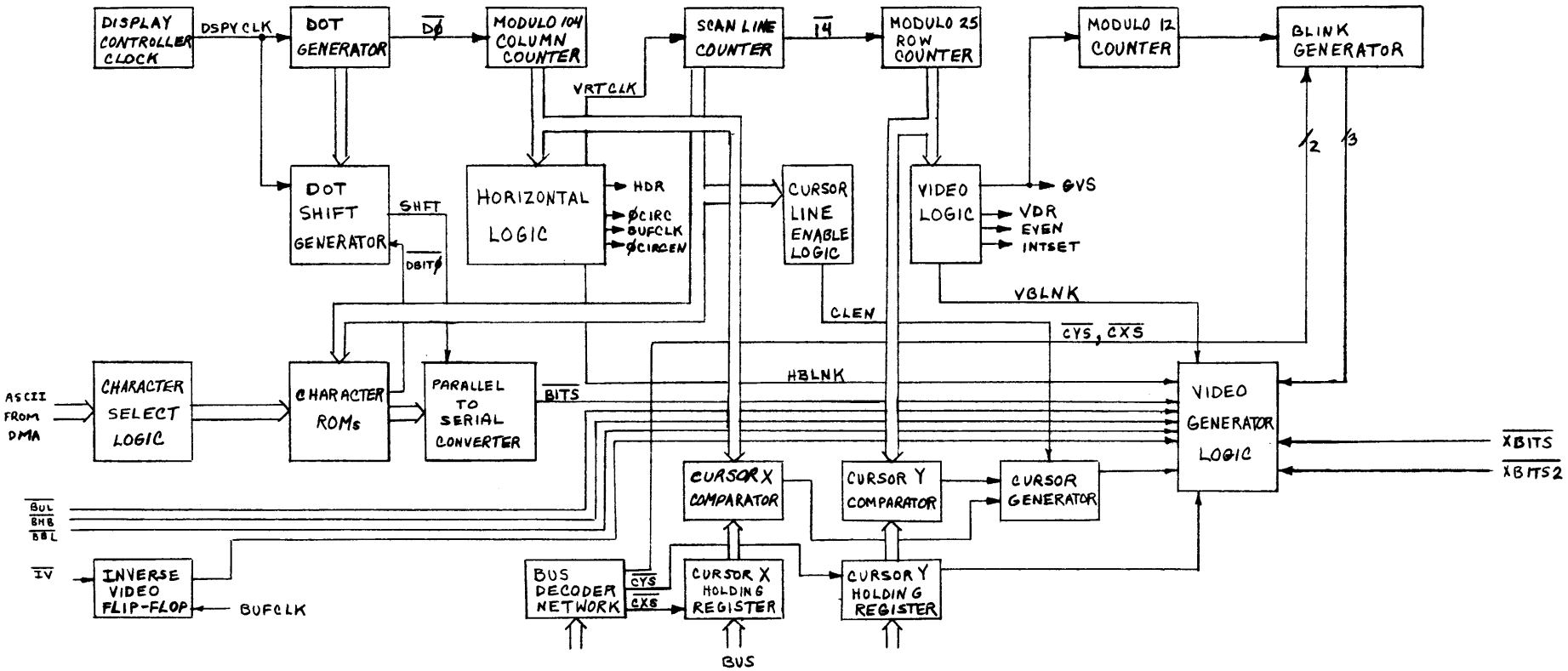
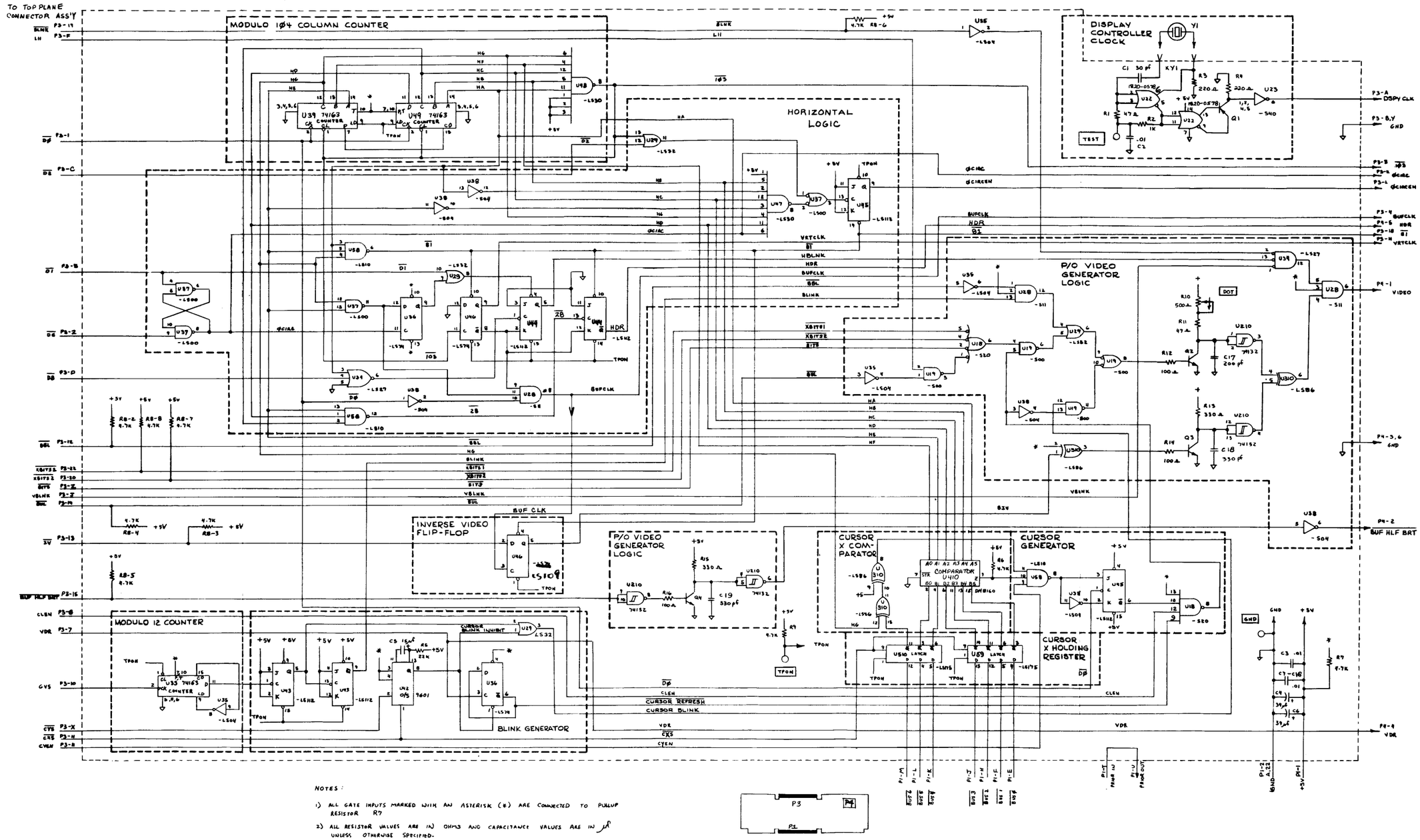


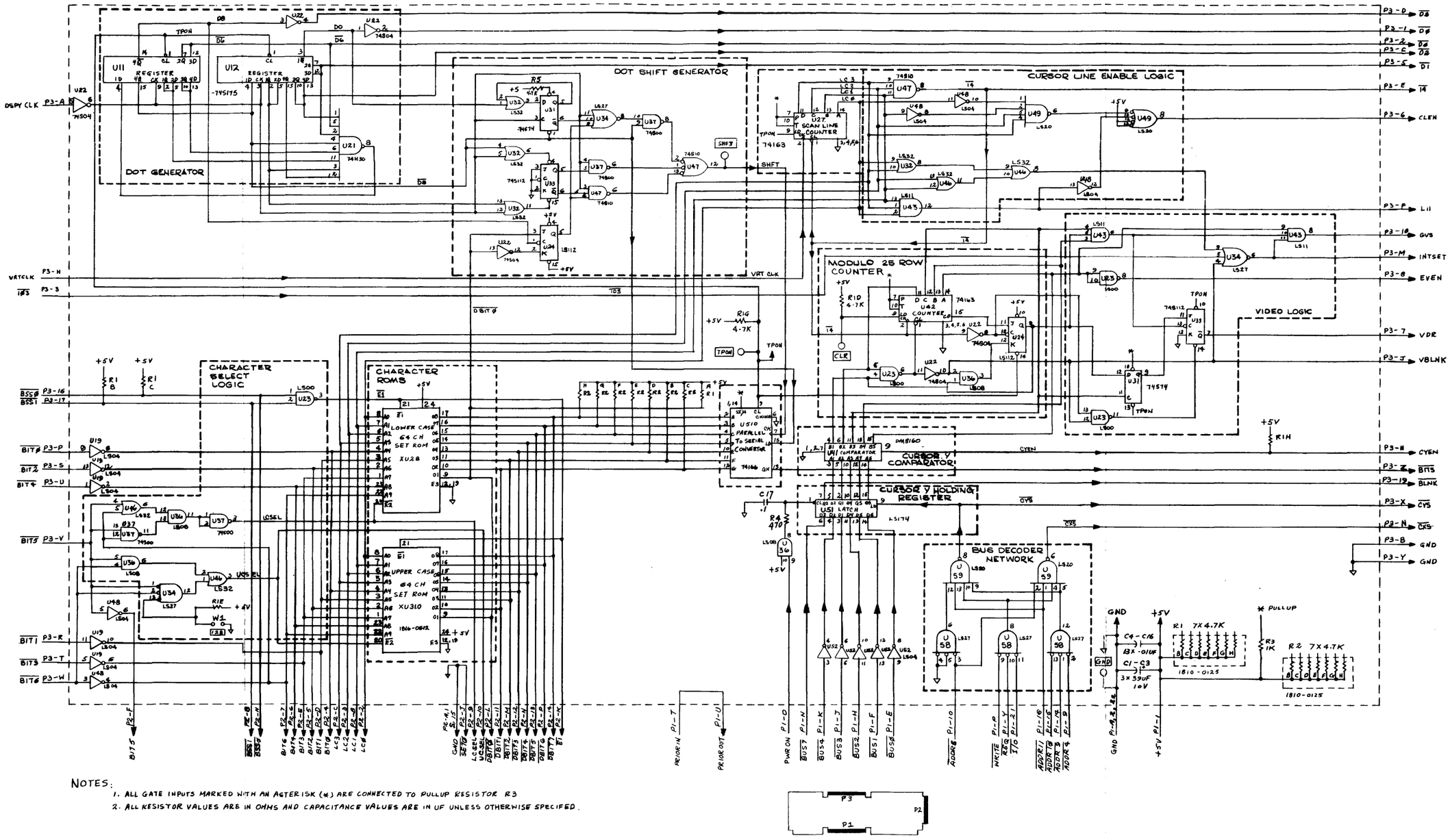
Figure 1
Display Timing & Display Control PCA's Block Diagram
SEP-10-77 13255-91112



NOTES:

1) ALL GATE INPUTS MARKED WITH AN ASTERISK (*) ARE CONNECTED TO PULLUP RESISTOR R7
2) ALL RESISTOR VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN μF UNLESS OTHERWISE SPECIFIED.

Figure 2
Display Timing PCA Schematic Diagram
SEP-10-77 13255-91112



NOTES:

1. ALL GATE INPUTS MARKED WITH AN ASTERISK (*) ARE CONNECTED TO PULLUP RESISTOR R3
2. ALL RESISTOR VALUES ARE IN OHMS AND CAPACITANCE VALUES ARE IN UF UNLESS OTHERWISE SPECIFIED.

Figure 3
Display Control PCA Schematic Diagram
SEP-10-77 13255-91112

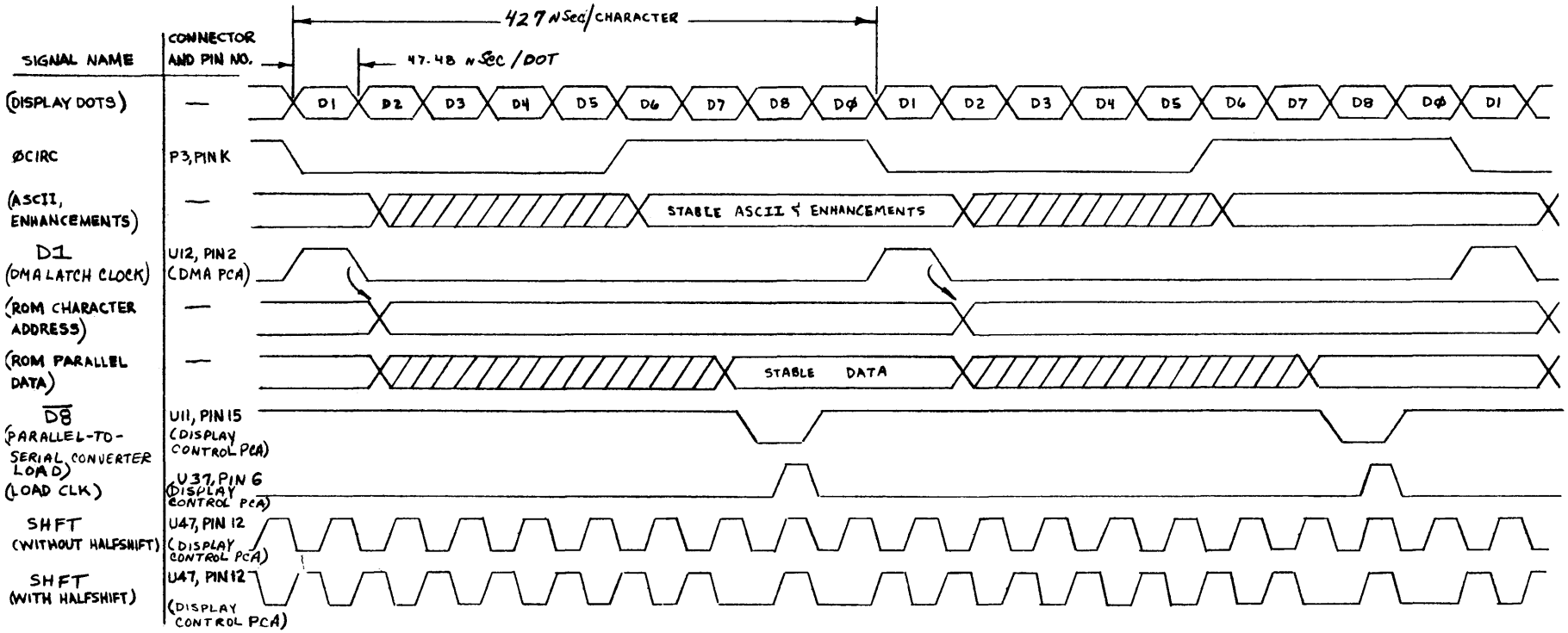


Figure 4
Character and Dot Shifting Timing Diagram
SEP-10-77 13255-91112

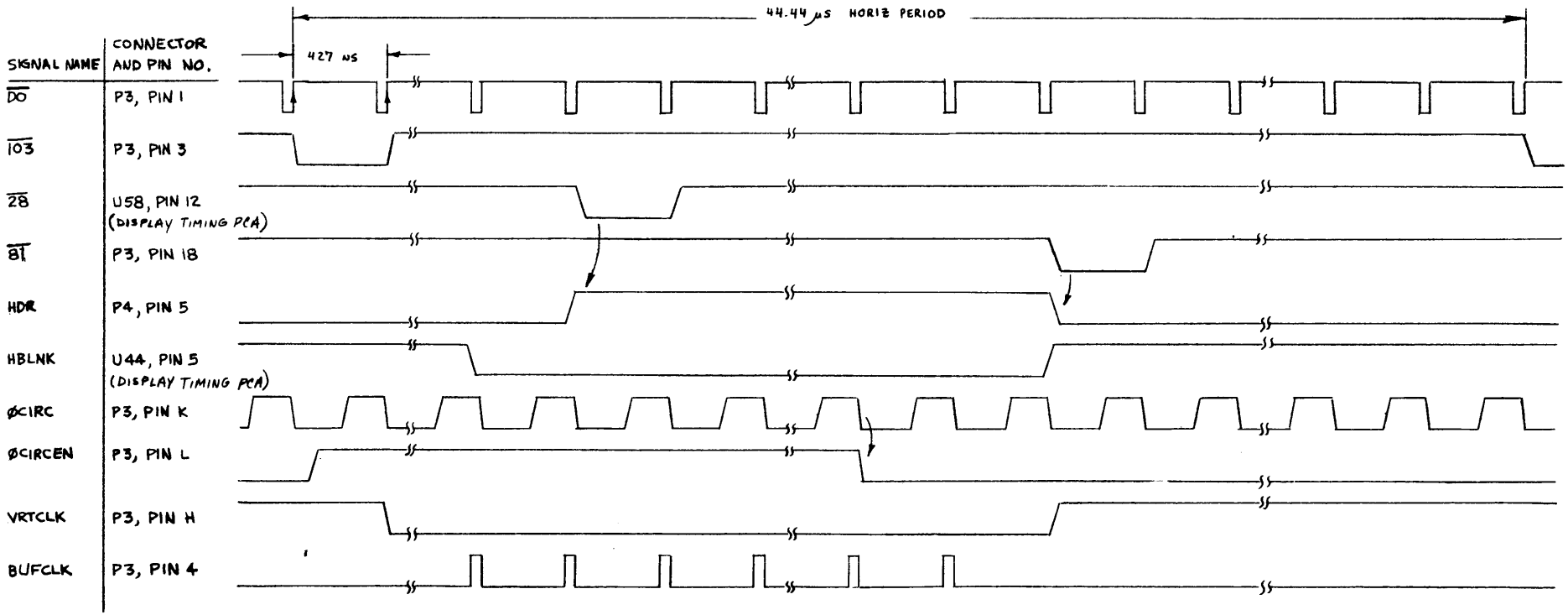


Figure 5
Horizontal Timing Diagram
SEP-10-77 13255-91112

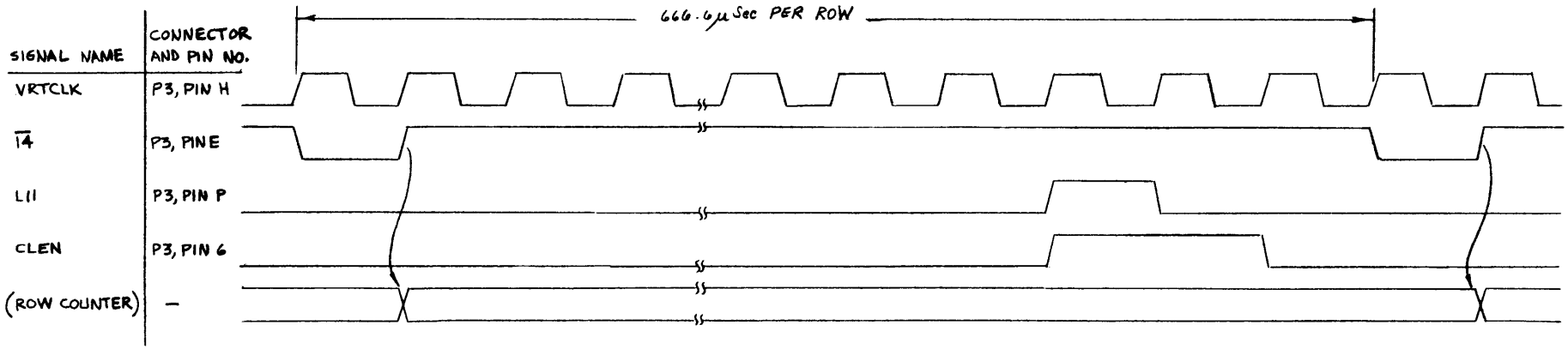


Figure 6
Scan Line Timing Diagram
SEP-10-77 13255-91112

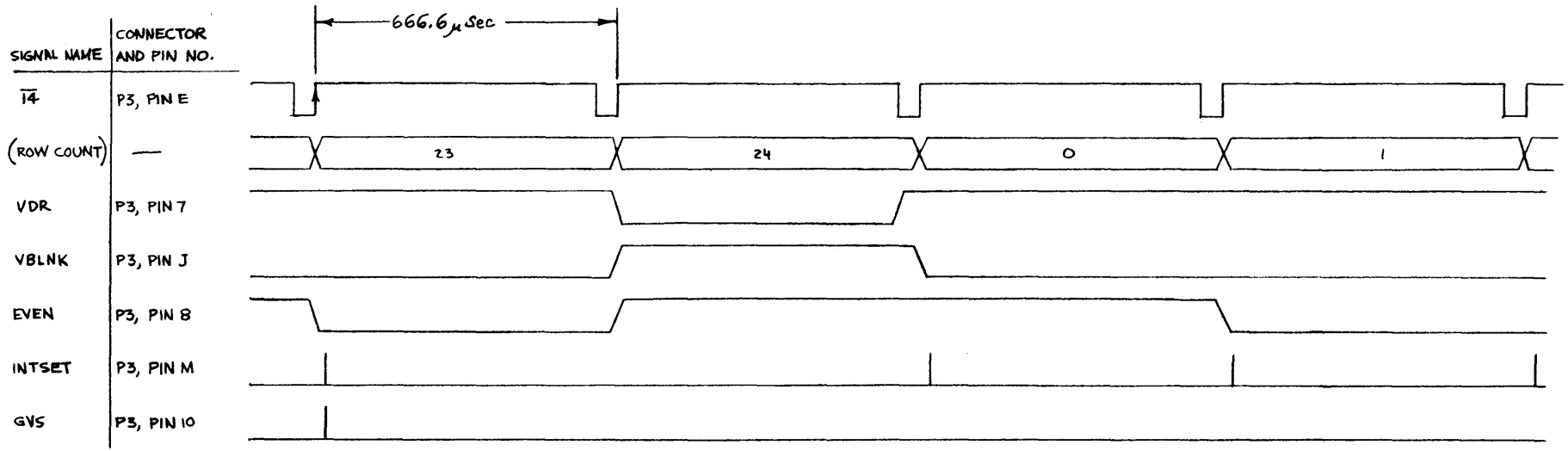


Figure 7
Row Timing Diagram
SEP-10-77
13255-91112

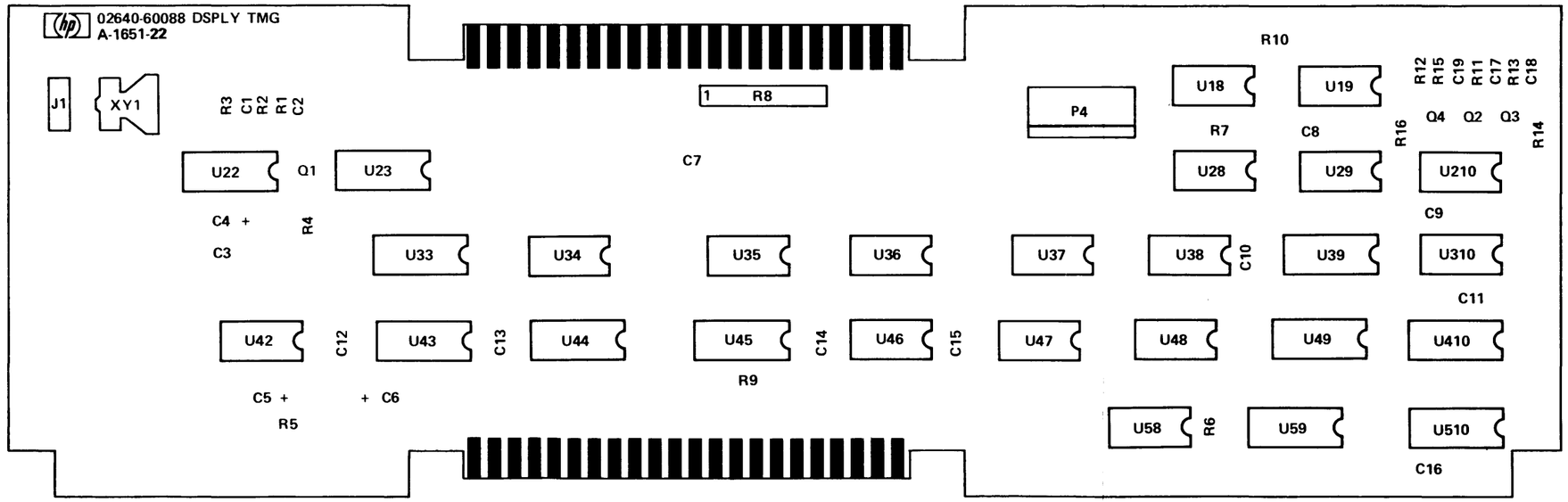


Figure 8
Display Timing PCA Component Location Diagram
SEP-10-77 13255-91112

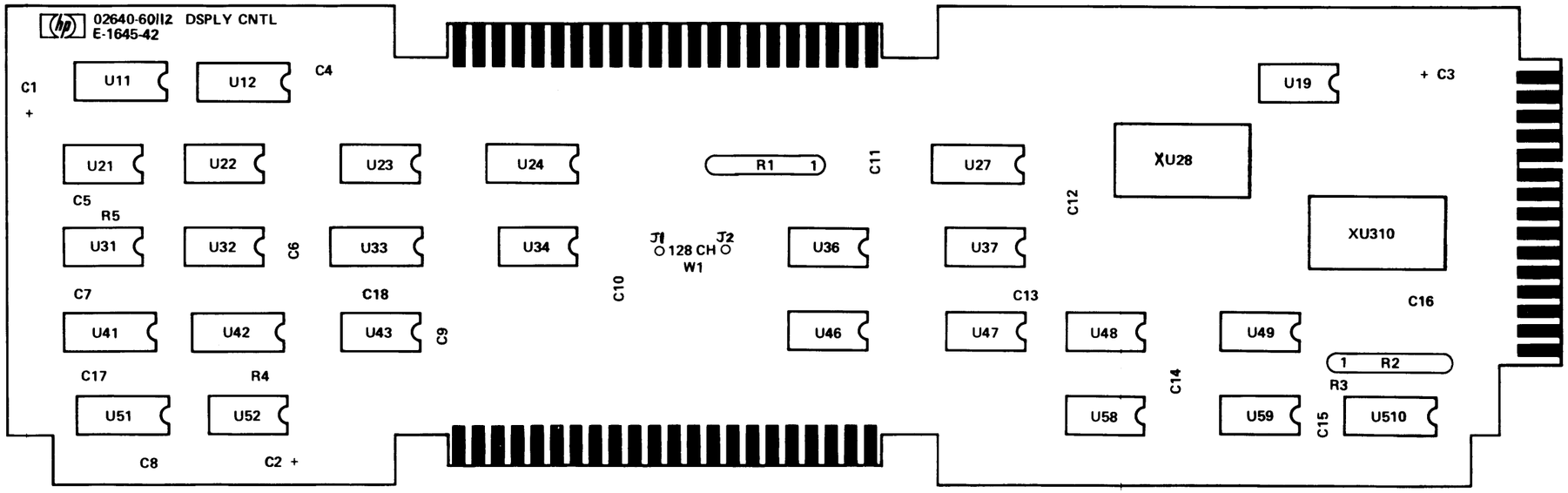


Figure 9
Display Control PCA Component Location Diagram
SEP-10-77 13255-91112

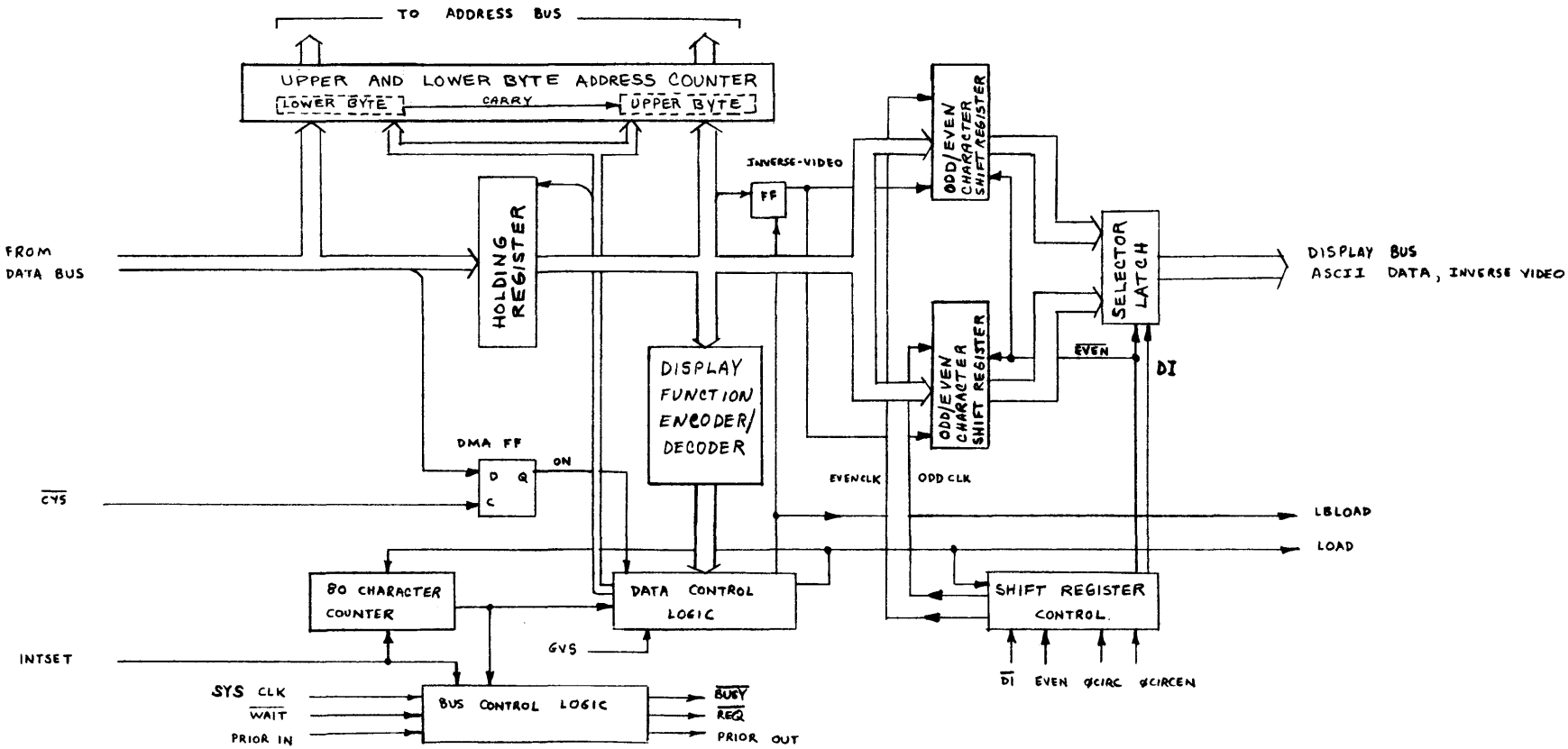


Figure 10
Display Memory Access (DMA) PCA Block Diagram
SEP-10-77 13255-91112

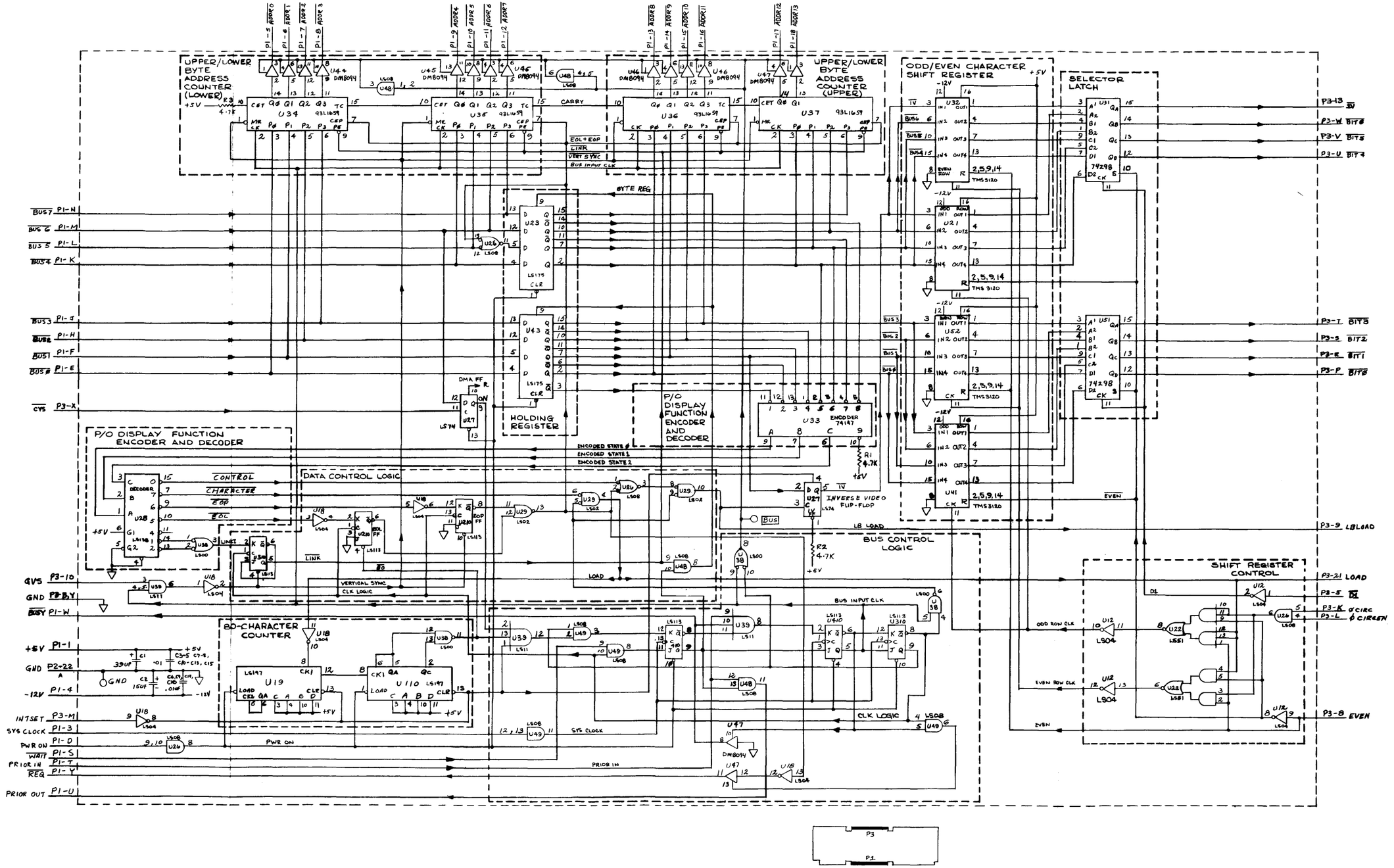


Figure 11
Display Memory Access (DMA) PCA Schematic Diagram
SEP-10-77 13255-91112

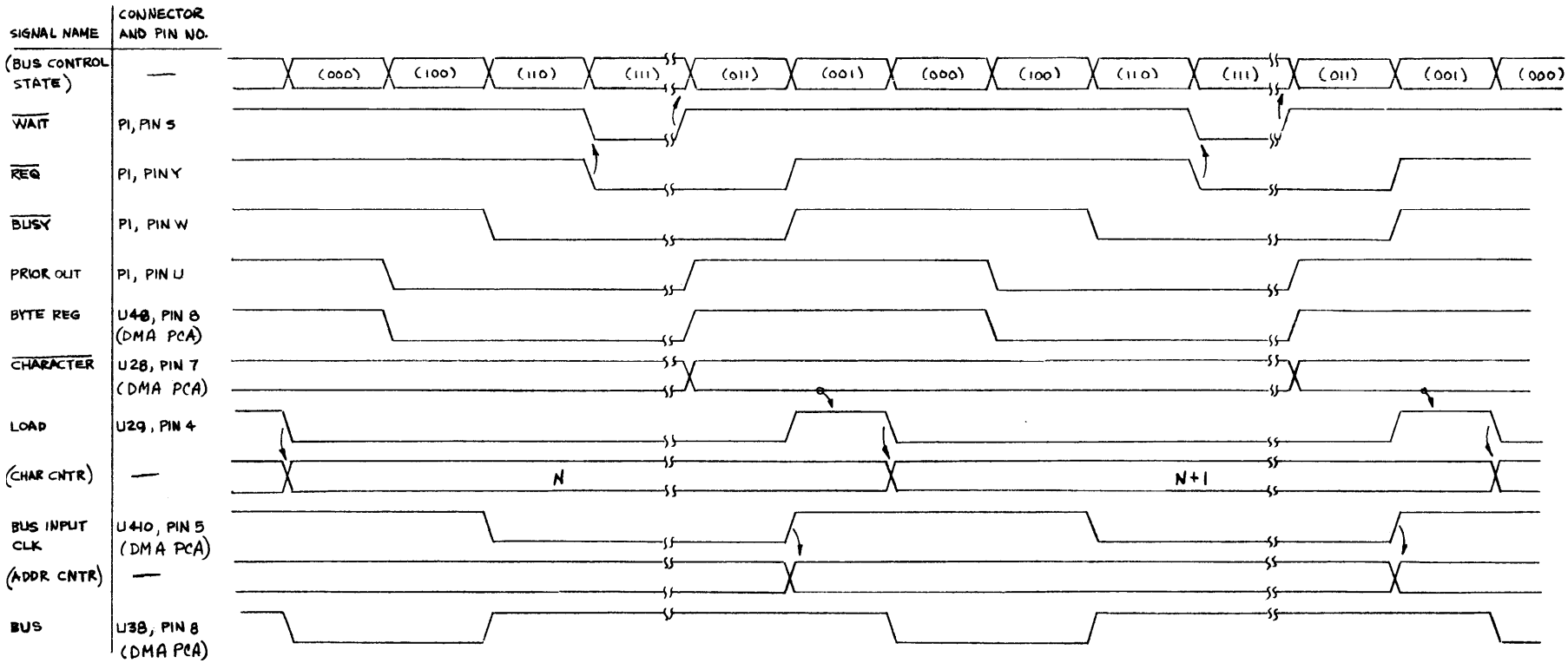


Figure 12
Character-To-Character DMA Transfer Timing Diagram
SEP-10-77 13255-91112

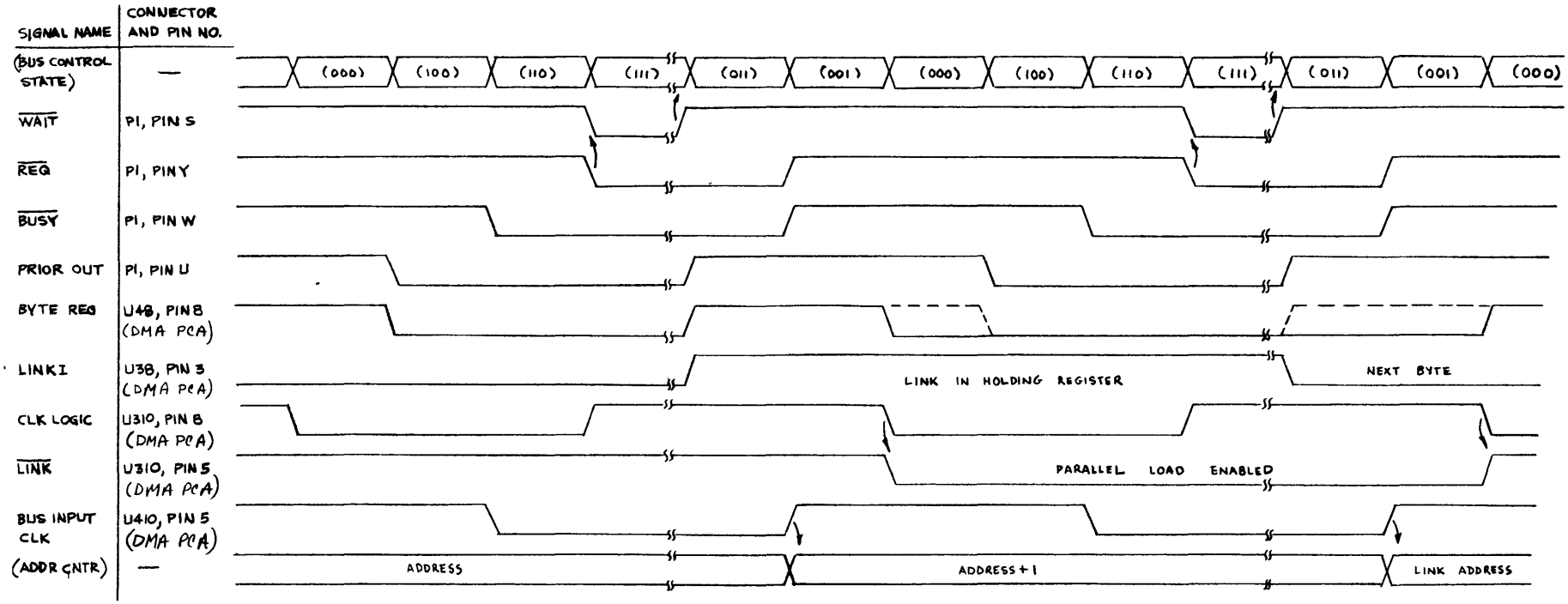


Figure 13
Link-Byte Fetch Timing Diagram
SEP-10-77 13255-91112

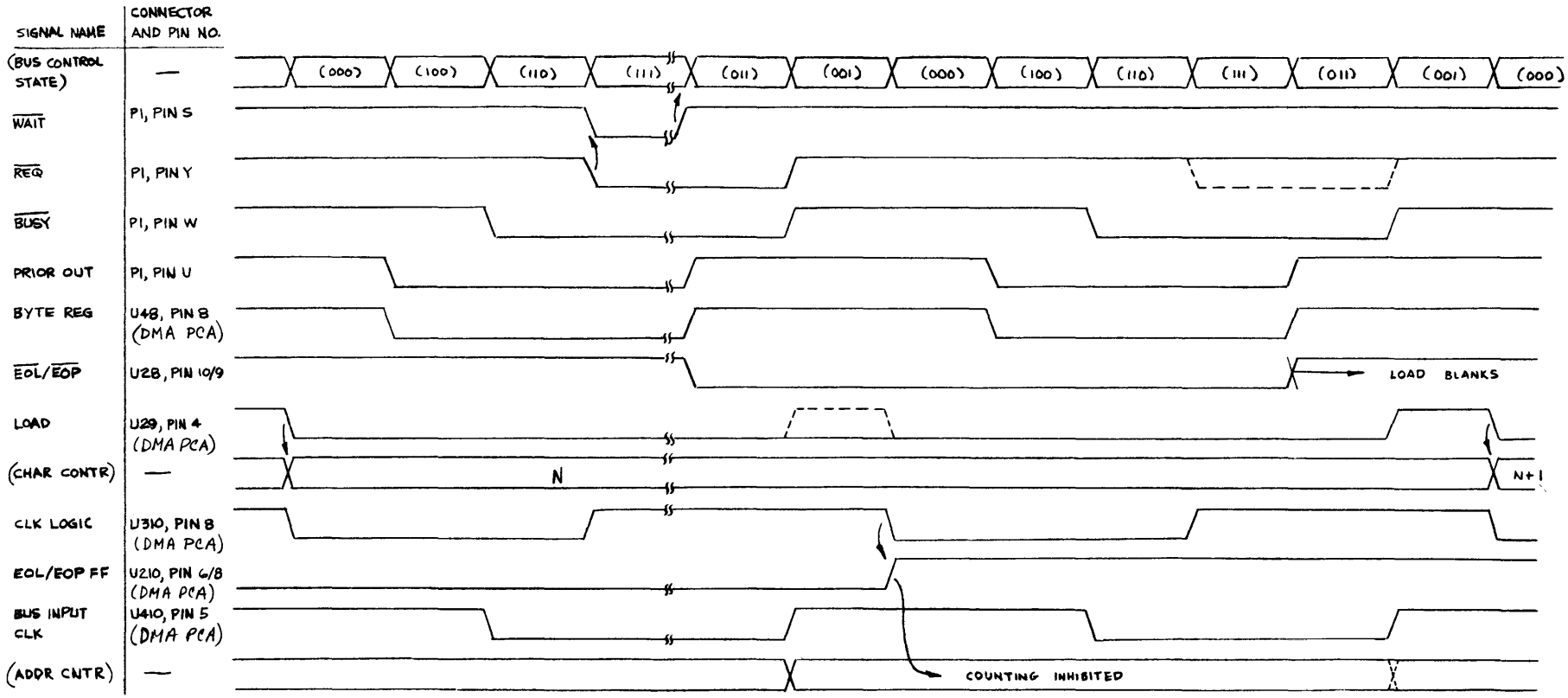


Figure 14
EOL or EOP Data Transfer Timing Diagram
SEP-10-77 13255-91112

BIT	7	6	5	4	3	2	1	Ø	
	0	X	X	X	X	X	X	X	CHARACTERS
	1	0	X	X	X	X	X	X	CONTROL
	1	1	1	X	X	X	X	X	LINK
	1	1	0	1	X	X	X	X	LINK
	1	1	0	0	0	X	X	X	FLAGS
	1	1	0	0	1	1	0	0	END OF LINE
	1	1	0	0	1	1	1	0	END OF PAGE

CHARACTERS : 128 ASCII CHARACTERS

CONTROL : CHARACTER SET SELECT, HALF-BRIGHT, UNDERLINE, INVERSE VIDEO, BLINK

BIT	5	4	3	2	1	Ø
	SET SELECT 1	SET SELECT Ø	HALF-BRIGHT	UNDERLINE	INVERSE VIDEO	BLINK

LINK : MOST SIGNIFICANT BYTE OF LOCATION OF NEXT BLOCK OF CHARACTERS

FLAGS : USED BY FIRMWARE. NO HARDWARE OPERATION.

END OF LINE: BLANK TO END OF LINE.

END OF PAGE: BLANK TO END OF PAGE.

Figure 15
DMA Data Encoding Diagram
SEP-10-77 13255-91112

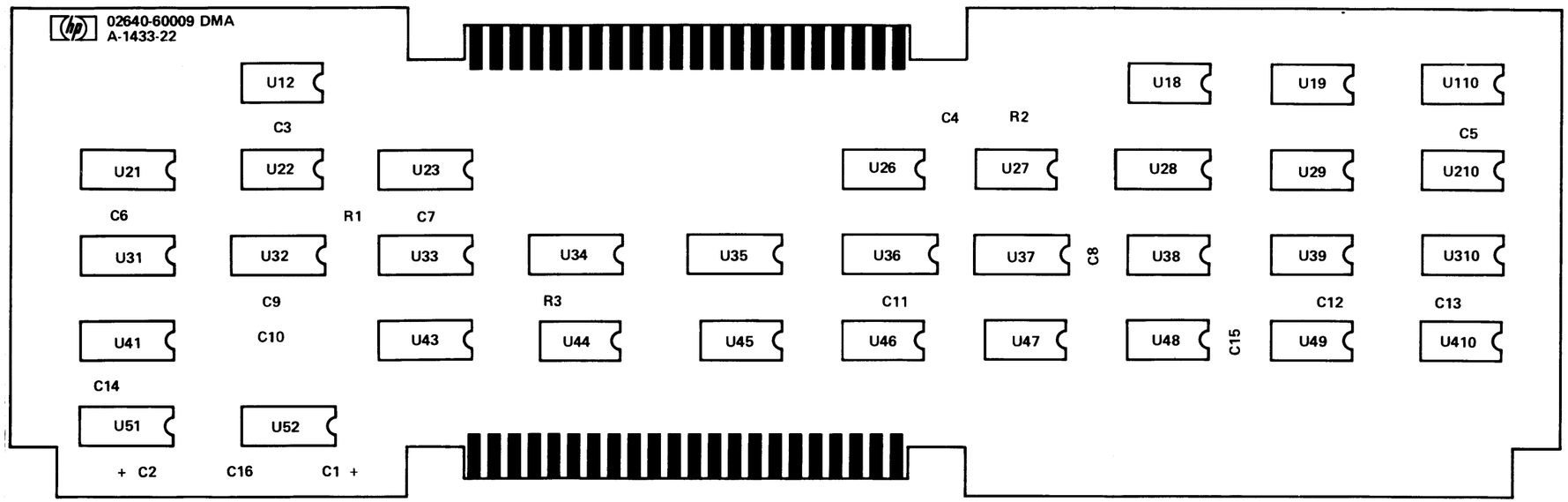


Figure 16
Display Memory Access (DMA) PCA
Component Location Diagram
SEP-10-77 13255-91112

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60088	1	DISPLAY TIMING ASSEMBLY DATE CODE: A-1651-22 REVISION DATE: 07-15-77	28480	02640-60088
C1	0160-2199	1	CAPACITOR-FXD 30PF +-5% 300WVDC MICA	28480	0160-2199
C2	0160-2055	12	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C3	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C4	0180-0393	2	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C5	0180-1746	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C6	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C17	0140-0198	1	CAPACITOR-FXD 200PF +-5% 300WVDC MICA	72136	DM15F201J0300WV1CR
C18	0160-2208	2	CAPACITOR-FXD 330PF +-5% 300WVDC MICA	28480	0160-2208
C19	0160-2208		CAPACITOR-FXD 330PF +-5% 300WVDC MICA	28480	0160-2208
E1	0360-0124	3	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
J1	1251-1123	1	CONNECTOR-SGL CONT SKT .08-IN-BSC-SZ RND	74970	105-0752-001
P4	1251-3766	1	CONNECTOR 6-PIN M POST TYPE	27264	09-88-2061
Q1	1853-0015	1	TRANSISTOR PNP SI PD=200MW FT=500MHZ	28480	1853-0015
Q2	1854-0019	3	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q3	1854-0019		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q4	1854-0019		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
R1	0683-4705	2	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R2	0683-1025	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R3	0683-2215	2	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R4	0683-2215		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R5	0683-2235	1	RESISTOR 22K 5% .25W FC TC=-400/+800	01121	CB2235
R6	0683-4725	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R7	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R8	1810-0125	1	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R9	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R10	2100-3351	1	RESISTOR-TRMR 500 10% C SIDE-ADJ 1-TRN	73138	72-142-0
R11	0683-4705		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R12	0683-1015	3	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R13	0683-3315	2	RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
R14	0683-1015		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R15	0683-3315		RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
R16	0683-1015		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
U18	1820-0688	1	IC-DIGITAL SN74S20N TTL S DUAL 4 NAND	01295	SN74S20N
U19	1820-0681	1	IC-DIGITAL SN74S00N TTL S QUAD 2 NAND	01295	SN74S00N
U22	1820-0578	1	IC-DIGITAL MC1024P ECL DUAL 2 OR-NOR	04713	MC1024P
U23	1820-0690	1	IC-DIGITAL SN74S40N TTL S DUAL 4 NAND	01295	SN74S40N
U26	1820-0686	1	IC-DIGITAL SN74S11N TTL S TPL 3 AND	01295	SN74S11N
U29	1820-1208	1	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U33	1820-0713	3	IC-DIGITAL SN74163N TTL BIN SYNCHRO	01295	SN74163N
U34	1820-1206	1	IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
U35	1820-1199	1	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U36	1820-1112	2	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U37	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U38	1820-0683	1	IC-DIGITAL SN74S04N TTL S HEX 1	01295	SN74S04N
U39	1820-0713		IC-DIGITAL SN74163N TTL BIN SYNCHRO	01295	SN74163N
U42	1820-0207	1	IC-DIGITAL 9601PC TTL MONOSTBL	07263	9601PC
U43	1820-1212	3	IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
U44	1820-1212		IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
U45	1820-1212		IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN74LS112N
U46	1820-1112		IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U47	1820-1207	2	IC-DIGITAL SN74LS30N TTL LS 8 NAND	01295	SN74LS30N
U48	1820-1207		IC-DIGITAL SN74LS30N TTL LS 8 NAND	01295	SN74LS30N
U49	1820-0713		IC-DIGITAL SN74163N TTL BIN SYNCHRO	01295	SN74163N
U58	1820-1202	1	IC-DIGITAL SN74LS10N TTL LS TPL 3 NAND	01295	SN74LS10N
U59	1820-1195	2	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U210	1820-1056	1	IC-DIGITAL SN74132N TTL QUAD 2 NAND	01295	SN74132N
U310	1820-1211	1	IC-DIGITAL SN74LS86N TTL LS QUAD 2	01295	SN74LS86N

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
			DISPLAY TIMING ASSEMBLY CONT'D.		
U410	1820-1131	1	IC-DIGITAL DM8160N TTL	27014	DM8160N
U510	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
XY1	1200-0546	1	SOCKET-XTAL 2-CONT HC-25/U DIP-SLDR	28480	1200-0546
			MISCELLANEOUS		
	8151-0013		WIRE 22AWG 1X22	28480	8151-0014

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60112	1	DISPLAY CONTROL ASSEMBLY DATE CODE: E-1645-42 REVISION DATE: 07-15-77	28480	02640-60112
C1	0180-0393	3	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C3	0180-0393		CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C4	0160-2055	13	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C5	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C17	0150-0121	1	CAPACITOR-FXD .1UF +80-20% 50WVDC CER	28480	0150-0121
E1	0360-0124	4	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E3	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E4	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
R1	1810-0125	2	NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R2	1810-0125		NETWORK-RES 8-PIN-SIP .125-PIN-SPCG	11236	750
R3	0683-1025	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R4	0683-4715	1	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R5	0683-4725	1	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
U11	1820-1191	2	IC-DIGITAL SN74S175N TTL S QUAD	01295	SN74S175N
U12	1820-1191		IC-DIGITAL SN74S175N TTL S QUAD	01295	SN74S175N
U19	1820-1199	3	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U21	1820-0375	1	IC-DIGITAL SN74H30N TTL H 8 NAND	01295	SN74H30N
U22	1820-0683	1	IC-DIGITAL SN74S04N TTL S HEX 1	01295	SN74S04N
U23	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U24	1820-1282	1	IC-DIGITAL SN74LS112N TTL LS DUAL	01295	SN53656
U27	1820-0713	2	IC-DIGITAL SN74163N TTL BIN SYNCHRO	01295	SN24744
U31	1820-0693	1	IC-DIGITAL SN74S74N TTL S DUAL	01295	SN74S74N
U32	1820-1208	2	IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U33	1820-0629	1	IC-DIGITAL SN74S112N TTL S DUAL J-K	01295	SN74S112N
U34	1820-1206	2	IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
U35	1820-1201	1	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U37	1820-0681	1	IC-DIGITAL SN74S00N TTL S QUAD 2 NAND	01295	SN74S00N
U41	1820-1131	1	IC-DIGITAL DM8160N TTL	27014	DM8160N
U42	1820-0713		IC-DIGITAL SN74163N TTL BIN SYNCHRO	01295	SN24744
U43	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U46	1820-1208		IC-DIGITAL SN74LS32N TTL LS QUAD 2 OR	01295	SN74LS32N
U47	1820-0685	1	IC-DIGITAL SN74S10N TTL S TPL 3 NAND	01295	SN74S10N
U48	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U49	1820-1204	2	IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
U51	1820-1196	1	IC-DIGITAL SN74LS174N TTL LS HEX	01295	SN74LS174N
U52	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U58	1820-1206		IC-DIGITAL SN74LS27N TTL LS TPL 3 NOR	01295	SN74LS27N
U59	1820-1204		IC-DIGITAL SN74LS20N TTL LS DUAL 4 NAND	01295	SN74LS20N
U510	1820-1107	1	IC-DIGITAL SN74166N TTL R-S PRL-IN	01295	SN74166N
XU28	1200-0541	2	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU510	1200-0541		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
J1	1251-0697	2	SOCKET-PC SINGLE		
J2	1251-0697		SOCKET-PC SINGLE		
	1258-0124	1	JMPR PLUG .3" C-C		

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60009	1	DMA ASSEMBLY DATE CODE: A-1433-22 REVISION DATE: 07-15-77	28480	02640-60009
C1	0180-0393	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C2	0180-1746	1	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
C3	0160-2055	14	CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C4	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C5	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C6	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C7	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C8	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C9	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C10	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C11	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C12	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C13	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C14	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C15	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
C16	0160-2055		CAPACITOR-FXD .01UF +80-20% 100WVDC CER	28480	0160-2055
E1	0360-0124	2	TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
E2	0360-0124		TERMINAL-STUD SGL-PIN PRESS-MTG	28480	0360-0124
R1	0683-4725	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R2	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R3	0683-4725		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
U12	1820-1199	2	IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U18	1820-1199		IC-DIGITAL SN74LS04N TTL LS HEX 1	01295	SN74LS04N
U19	1820-1193	2	IC-DIGITAL SN74LS197N TTL LS BIN	01295	SN74LS197N
U21	1820-1346	4	IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U22	1820-1210	1	IC-DIGITAL SN74LS51N TTL LS DUAL 2	01295	SN74LS51N
U23	1820-1195	2	IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U26	1820-1201	3	IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U27	1820-1112	1	IC-DIGITAL SN74LS74N TTL LS DUAL	01295	SN74LS74N
U28	1820-1216	1	IC-DIGITAL SN74LS138N TTL LS 3	01295	SN74LS138N
U29	1820-1144	1	IC-DIGITAL SN74LS02N TTL LS QUAD 2 NOR	01295	SN74LS02N
U31	1820-1100	2	IC-DIGITAL SN74298N TTL QUAD 2	01295	SN74298N
U32	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U33	1820-1082	1	IC-DIGITAL SN74147N TTL 10	01295	SN74147N
U34	1820-0778	4	IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U35	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U36	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U37	1820-0778		IC-DIGITAL 93L16DC TTL L BIN SYNCHRO	07263	93L16DC
U38	1820-1197	1	IC-DIGITAL SN74LS00N TTL LS QUAD 2 NAND	01295	SN74LS00N
U39	1820-1203	1	IC-DIGITAL SN74LS11N TTL LS TPL 3 AND	01295	SN74LS11N
U41	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U43	1820-1195		IC-DIGITAL SN74LS175N TTL LS QUAD	01295	SN74LS175N
U44	1820-0846	4	IC-DIGITAL DM8094N TTL QUAD 1 NON-INV	27014	DM8094N
U45	1820-0846		IC-DIGITAL DM8094N TTL QUAD 1 NON-INV	27014	DM8094N
U46	1820-0846		IC-DIGITAL DM8094N TTL QUAD 1 NON-INV	27014	DM8094N
U47	1820-0846		IC-DIGITAL DM8094N TTL QUAD 1 NON-INV	27014	DM8094N
U48	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U49	1820-1201		IC-DIGITAL SN74LS08N TTL LS QUAD 2 AND	01295	SN74LS08N
U51	1820-1100		IC-DIGITAL SN74298N TTL QUAD 2	01295	SN74298N
U52	1820-1346		IC-DIGITAL TMS3120NC PMOS QUAD	01295	TMS3120NC
U110	1820-1193		IC-DIGITAL SN74LS197N TTL LS BIN	01295	SN74LS197N
U210	1820-1213	3	IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U310	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N
U410	1820-1213		IC-DIGITAL SN74LS113N TTL LS DUAL	01295	SN74LS113N

Reference Designation	HP Part Number	Qty	Description	Mfr Code	Mfr Part Number
	02640-60012	1	CONNECTOR ASSEMBLY (3) REVISION DATE: 12-01-76	28480	02640-60012
	0403-0347	3	BUMPER FOOT, 0.25" W	13862	9668
	1251-1387	3	CONNECTOR-PC EDGE 22-CONT/ROW 2-ROWS	71785	252-22-30-340