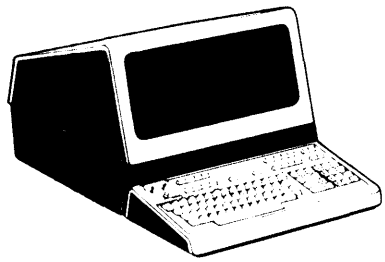
ENHANCED ASYNCHRONOUS DATACOM MODULE

Manual Part No. 13255-91239

REVISED

OCT-15-79

DATA TERMINAL
TECHNICAL INFORMATION



HEWLETT hp PACKARD

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1.0 INTRODUCTION.

The Enhanced Asynchronous Datacom PCA along with an interface cable assmebly comprise the Enhanced Asynchronous Datacom Module and provide a communication link between the terminal and an external computer.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Enhanced Asynchronous Datacom Module is contained in tables 1.0 through 6.4.

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.100 Inches	Weight (Pounds)
02640-60239	Enhanced Asynchronous Datacom PCA	12.9 x 4.0 x 0.5	0.38

Number of Backplane Slots Required: 1

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NOTE: This document is part of the 264XX DATA TERMINAL product series Technical Information Package (HP 13255).

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Table 2.0 Reliability and Environmental Information

Environmental: (X) HP Class B ( ) Other:
Restrictions: Type tested at product level
Failure Rate: 0.870 (percent per 1000 hours)

Table 3.0 Power Supply and Clock Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+5 Volt Supply	+12 Volt Supply	-12 Volt Supply	-42 Volt Supply
@ 100 mA	@ 40 mA	@ 80 mA	@ mA NOT APPLICABLE

115 volts ac	220 volts ac
@ A NOT APPLICABLE	@ A NOT APPLICABLE

Clock Frequency: 4.915 MHz +/-0.1%

Table 4.0 Switch Definitions

PCA	Function
$\overline{THE}$	Transmit Handshake Enable Open - Enable Transmit Handshake Circuit Closed - Disable Transmit Handshake Circuit SWITCHES $\overline{200}$, $\overline{600}$, $\overline{EBE}$ WORK ONLY WHEN KEYBOARD BAUD RATE SELECTION DIAL IS TURNED TO EXT.
$\overline{EBE}$	External Baud Rate Enable Open - Enable External Baud Rate Clock Closed - Disable External Baud Rate Clock and enable either 200 or 600 Baud
$\overline{200}$	200 Baud Rate Enable Open - Enable 200 Baud Closed - Disable 200 Baud
$\overline{600}$	600 Baud Rate Enable Open - Enable 600 Baud Closed - Disable 600 Baud ****NOTE**** Only 1 of switches $\overline{EBE}$, $\overline{200}$, $\overline{600}$ may be left open at any time

Table 5.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P1, Pin 1	+5V	+5 Volt Power Supply
- 2	GND	Ground Common Return (Power and Signal)
- 3	SYS CLK	4.915 MHz System Clock
- 4	-12V	-12 Volt Power Supply
- 5	$\overline{\text{ADDR0}}$	Negative True, Address Bit 0
- 6	$\overline{\text{ADDR1}}$	Negative True, Address Bit 1
- 7		Not Used
- 8	$\overline{\text{ADDR3}}$	Negative True, Address Bit 3
- 9	$\overline{\text{ADDR4}}$	Negative True, Address Bit 4
-10	$\overline{\text{ADDR5}}$	Negative True, Address Bit 5
-11	$\overline{\text{ADDR6}}$	Negative True, Address Bit 6
-12		Not used
-13		
-14	$\overline{\text{ADDR9}}$	Negative True, Address Bit 9
-15	$\overline{\text{ADDR10}}$	Negative True, Address Bit 10
-16	$\overline{\text{ADDR11}}$	Negative True, Address Bit 11
-17		Not used
-18		
-19		
-20		
-21	$\overline{\text{I/O}}$	Negative True, Input Output/Memory
-22	GND	Ground Common Return (Power and Signal)

Table 5.0 Connector Information (Cont'd.)

Connector and Pin No.	Signal Name	Signal Description
P1, Pin A	GND	Ground Common Return (Power and Signal)
-B		Not Used
-C	+12V	+12 Volt Power Supply
-D	PWR ON	System Power On
-E	$\overline{\text{BUS0}}$	Negative True, Data Bus Bit 0
-F	$\overline{\text{BUS1}}$	Negative True, Data Bus Bit 1
-H	$\overline{\text{BUS2}}$	Negative True, Data Bus Bit 2
-J	$\overline{\text{BUS3}}$	Negative True, Data Bus Bit 3
-K	$\overline{\text{BUS4}}$	Negative True, Data Bus Bit 4
-L	$\overline{\text{BUS5}}$	Negative True, Data Bus Bit 5
-M	$\overline{\text{BUS6}}$	Negative True, Data Bus Bit 6
-N	$\overline{\text{BUS7}}$	Negative True, Data Bus Bit 7
-P	$\overline{\text{WRITE}}$	Negative True, Write/Read Type Cycle
-R -S		} Not Used
-T	PRIOR IN	Bus Controller Priority In
-U	PRIOR OUT	Bus Controller Priority Out
-V -W -X		} Not Used
-Y	$\overline{\text{REQ}}$	Negative True, Request (Bus Data Currently Valid)
-Z	$\overline{\text{ATN}}$	Negative True, Datacom Interrupt Request

Table 5.1 Connector Information

Connector and Pin No.	Signal Name	Signal Description
P2, Pin 1		Not Used
Pin 2		Not Used
Pin 3	-12V	-12 Volt Power Supply
Pin 4 through Pin 12		Not Used
Pin 5		Not Used
Pin 6		Not Used
Pin 7	+12V	+12V Power Supply
Pin 8 through Pin 12		Not Used
Pin 13	+5V	+5V Power Supply
Pin 14		Not Used
Pin 15	TEST	Special Test Point- Presets Baud Rate Counters

Table 5.1 Connector Information (Cont'd)

Connector and Pin No.	Signal Name	Signal Description *NOTE: Signals with an asterisk below are TTL levels and should not be connected to RS232C drivers.
P2, Pin A	GND	Terminal Logic Ground
-B	BA	Serial Data Out
-C	BB	Serial Data In
-D	CA	Request to Send
-E	CB	Clear to Send
-F	CC	Data Set Ready
-H	AB	Signal Ground
-J	CF	Receiver Carrier
-K	X8 CLK*	External x8 Baud Rate Clock Out
-L	X16 OUT*	External x16 Baud Rate Clock Out
-M	SA	Secondary Channel Transmit
-N	SB	Secondary Channel Receive
-P	CD	Data Terminal Ready
-R	CH	Rate Select
-S	X16 IN*	External x16 Baud Rate Clock In

Table 6.0 Module Bus Pin Assignments

Function Performed: Output Control Register Bits

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0001)

Function Specifier: ADDR 5 = 0
ADDR 6 = 1

Data Bus Bit Interpretation:

B7 0=CH High
1=CH Low

B6 0 = No Break
1 = Break (SA is high, BA is low)

B5 0 = Parity Enable
1 = Parity Disable

B4 0 = Odd Parity
1 = Even Parity

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
0	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Transmit/Receive Baud Rate

	EXT	110*	150	300	1200	2400	4800	9600
B3	0	1	0	1	0	1	0	1
B2	0	0	1	1	0	0	1	1
B1	0	0	0	0	1	1	1	1

*Selects two stop bits.

B0 0 = CA is on
1 = CA is off

Table 6.1 Module Bus Pin Assignments

Function Performed: Input Received Data Character

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0001)

Function Specifier: ADDR 5 = 0
ADDR 6 = 0

Data Bus Bit Interpretation:

B7 Receive Data Bit 7
(Equals 0 if parity is selected, otherwise is equal to most signficant data bit)

B6 Receive Data Bit 6

B5 Receive Data Bit 5

B4 Receive Data Bit 4

B3 Receive Data Bit 3

B2 Receive Data Bit 2

B1 Receive Data Bit 1

B0 Receive Data Bit 0

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
0	ADDR 9
X	ADDR 8
X	ADDR 7
0	ADDR 6
0	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.2 Module Bus Pin Assignments

Function Performed: Output data character for transmission

Poll Bit: Not Applicable

Module Address: (ADDR 11,10,9,4) = (0001)

Function Specifier: ADDR 5 = 1
ADDR 6 = 1

Data Bus Bit Interpretation:

B7 Transmit Data Bit 7 } If Parity is Enabled Bit 7 is replaced by proper parity.

B6 Transmit Data Bit 6

B5 Transmit Data Bit 5

B4 Transmit Data Bit 4

B3 Transmit Data Bit 3

B2 Transmit Data Bit 2

B1 Transmit Data Bit 1

Value	Bus Signal
X	ADDR 15
X	ADDR 14
X	ADDR 13
X	ADDR 12
0	ADDR 11
0	ADDR 10
0	ADDR 9
X	ADDR 8
X	ADDR 7
1	ADDR 6
1	ADDR 5
1	ADDR 4
X	ADDR 3
X	ADDR 2
X	ADDR 1
X	ADDR 0
B7	BUS 7
B6	BUS 6
B5	BUS 5
B4	BUS 4
B3	BUS 3
B2	BUS 2
B1	BUS 1
B0	BUS 0

1=Logical 1=Bus Low
0=Logical 0=Bus High
X=Don't Care

Table 6.3 Module Bus Pin Assignments

Function Performed: Input Datacom Status	Value	Bus Signal
	X	ADDR 15
Poll Bit: Not Applicable	X	ADDR 14
	X	ADDR 13
Module Address: (ADDR 11,10,9,4) = (0001)	X	ADDR 12
	0	ADDR 11
	0	ADDR 10
	0	ADDR 9
Function Specifier: ADDR 5 = 1	X	ADDR 8
ADDR 6 = 0	X	ADDR 7
	0	ADDR 6
	1	ADDR 5
	1	ADDR 4
	X	ADDR 3
Data Bus Bit Interpretation:	X	ADDR 2
	X	ADDR 1
B7 Timer Interrupt } ALTERNATE STATUS (A0=1)	X	ADDR 0
} ---- --- ----- --		
} Data Set Ready (CC)	B7	BUS 7
	B6	BUS 6
_____ __	B5	BUS 5
B6 Secondary Channel Receive (SB)	B4	BUS 4
	B3	BUS 3
	B2	BUS 2
_____ __	B1	BUS 1
B5 Clear to Send (CB)	B0	BUS 0
	1=Logical 1=Bus Low	
	0=Logical 0=Bus High	
_____ __	X=Don't Care	
B4 Carrier (CF)		
B3 0 = No Parity Error }		
1 = Parity Error }		
} Overrun and parity errors are set/reset		
} after each character is received.		
B2 0 = No Overrun }		
1 = Overrun Error }		
B1 0 = Transmit Holding Register Full } ALTERNATE STATUS (A0=1)		
1 = Transmit Holding Register Empty} 0= Transmission in progress		
} 1= Transmission Complete		
B0 0 = No Data Received} Data received is made "0" by inputting a		
1 = Data Received } received data character (see table 5.1).		

Table 6.4 Module Bus Pin

Function	Value	Signal
Function Performed: Input instruction to Set/Reset Data Terminal Ready (CD) and Enable/Disable Timer	X	ADDR 15
	X	ADDR 14
Poll Bit: Not Applicable	X	ADDR 13
	X	ADDR 12
Module Address: (ADDR 11,10,9,4) = (0001)	A11	ADDR 11
	A10	ADDR 10
	A9	ADDR 9
	X	ADDR 8
Function Specifier: ADDR 5 = 0	X	ADDR 7
ADDR 6 = 0	1	ADDR 6
	1	ADDR 5
	A4	ADDR 4
	A3	ADDR 3
A3 = 0, CD On	A2	ADDR 2
A3 = 1, CD Off	X	ADDR 1
	X	ADDR 0
	B7	BUS 7
	B6	BUS 6
A0 = 1 Enable Timer	B5	BUS 5
A0 = 0 Disable Timer	B4	BUS 4
	B3	BUS 3
A1 = 1 Not Used	B2	BUS 2
A1 = 0 Clear Timer Interrupt	B1	BUS 1
	B0	BUS 0
	1=Logical	1=Bus Low
	0=Logical	0=Bus High

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), and parts list (02640-60239) located in the appendix.

The Enhanced Asynchronous Datacom Module is the primary interface between the terminal and external data processing equipment. It provides characterter parallel data, status, and control information to the terminal microprocessor by way of firmware control. Individual characters are sent and received bit-serial and character-serial using an EIA RS232C electrical interface. The PCA can be connected to external data processing equipment directly or by modem depending on the on the interface cable assembly used. The module functional groups consist of the universal asynchronous receiver/transmitter (UART), bus decoder logic, control logic, baud rate generator, RS232C drivers, Hardware Timer Logic, Transmit Handshake and Fifo buffer.

3.1 UART.

3.1.1 The UART is Western Digital's TR1602B and is the key element of the module. It accepts a parallel character from the terminal data bus, appends the necessary asynchronous character formatting and parity bits, and transmits the information serially at a rate determined by an input clock. The UART has a master reset input for power on initialization, control inputs and status outputs for firmware control of the interface, and clock inputs for determining the serial data bit rate. The UART receives serial data, deletes the start and stop framing bits, optionally checks incoming parity, and outputs a parallel character.

3.1.2 The UART (U25), provides all control logic and data storage necessary to implement an asynchronous parallel-to-serial (transmit) and serial-to-parallel (receive) converter. It has control inputs to determine character size and formatting, including an optional parity bit (generated on output and checked on input). The UART has status outputs for determining when the UART can accept another parallel character for transmission or for indicating that a character has been received and is ready for input. The UART has transmit and receive clock inputs which are clocked at 16 times the desired baud rate.

3.1.2.1 There are five control inputs (Pins 35, 39, 36, 37, and 38) for the UART which define character format and parity. The character size is always eight bits with the optional even or odd parity being placed in the most significant bit of the character when selected. If 110 baud is the bit rate used, an extra stop bit is added to the asynchronous character formatting. When transmitted, each character will consist of a start bit, eight data bits (optional parity) least significant bit first, and one or two (110 baud) stop bits.

3.1.2.2 Characters to be transmitted are loaded into the UART by $\overline{\text{DATA STROBE}}$. This output command from the bus decoder circuit strobes data into the UART using input THRL (Transmit Holding Register Load) at Pin 23. This causes the THRE (Transmit Holding Register Empty) at Pin 22 output to go low and remain false until the character in the buffer is transferred into the UART's serial output shifter. The character in the buffer is transferred to the shifter when the shifter is empty or has completed the previous character and the THRE output goes true again. Data bits and format bits (start, stop, and parity) are shifted out of the UART at TRO (Transmitter Register Output) at Pin 25 according to the inputs from the control logic. Each individual bit takes 16 transmit clocks to be shifted out.

3.1.2.3 The UART uses the RRC (Receiver Clock) signal at Pin 17 to sample the RI input (Receive Serial In) at Pin 20 for an asynchronous start bit. When it detects a valid start bit, the UART begins shifting data (16 clocks per bit) into the receive serial shifter. When the character is completed, the UART removes the asynchronous format bits (start and stop) transfers the character in parallel to UART outputs Pins 5 through 12 and sets DR (Data Received) at Pin 19 high. When one character is received, the UART updates two status bits, PE (Parity Error) at Pin 13 and OE (Overrun Error) at Pin 15. PE is set high only when odd or even parity is selected by the control logic and the input character had the incorrect parity. OE is set high when the UART has already received a character, DR (Pin 19) is high and a new character is loaded into it. When Data Input (U36, Pin 4) is decoded, the UART data outputs are gated onto the terminal bus and DRR (Data Received Reset) at Pin 18 is pulse, setting DR (Pin 19) low. The UART is then ready for another character.

3.2 BUS DECODER LOGIC.

3.2.1 The bus decoder logic provides the interface for the module and includes module address decoding and input and output enable signals. Module address and data bus control signals determine when the PCA will input (Processor Read) data or control and when it will output (Processor Write) data or status.

3.2.2 The address of the Enhanced Asynchronous Datacom PCA is determined by two logic gates, (U57, Pin 8 and U36, Pin 10). These connect to the terminal address lines ($\overline{\text{ADDR11}}$, $\overline{\text{ADDR10}}$, $\overline{\text{ADDR9}}$ and $\overline{\text{ADDR4}}$). The module is further addressed by inputs from the terminal bus to a 1-of-8 decoder (U46), which samples $\overline{\text{WRITE}}$, $\overline{\text{ADDR6}}$, and $\overline{\text{ADDR5}}$ with $\overline{\text{REQ}}$ and $\overline{\text{I/O}}$ enabling the decoder.

3.2.2.1 The normal bus addressing sequence is for all of the module address information to be placed on the terminal data bus and allowed to become stable. Then $\overline{\text{REQ}}$ which is the final enabling signal (execute or strobe command) is set true (low). This creates one of the following output strobes from the 1-of-8 decoder (U42): $\overline{\text{DATA STROBE}}$ (U46, Pin 15), $\overline{\text{CONTROL LOAD}}$ (U46, Pin 14), STATUS INPUT (U36, Pin 6), DATA INPUT (U36, Pin 4), Timer Function (U36,Pin 12) and Firmware Control Read (U47, Pin 5).

3.2.2.2 Data output from the UART and interface status are available to the terminal data bus through buffers (U13, U14, U15, and U16). The three input commands (STATUS INPUT, DATA INPUT, and FIRMWARE READ) enable status or data to be gated onto the terminal data bus. During a data input, DR at U25, Pin 19 is set while the data is gated to the terminal bus.

3.2.2.3 The occurance of a FIRMWARE READ gates a (C0) hex on to the data bus. This differentiates this Datacom board from the General Purpose (02640-60143) Datacom board.

3.3 CONTROL LOGIC.

3.3.1 The control logic circuit is loaded from the terminal data bus by a microprocessor output command. There are seven bit positions which control interface signals, define UART controls, and select the data in/out bit rate (baud rate).

3.3.2 The control register is program loaded into hex register U43. The inputs to the control register are $\overline{BUS0}$ through $\overline{BUS7}$. The control

The control information is loaded into the register by $\overline{CONTROL\ LOAD}$ (U46, Pin 14). (Refer to table 5.0 for definition of conrol register bits.)

3.3.2.1 The three baud rate select bits (CB3, CB2, and CB1) go to the multiplexer and determine which part of the divider chain or if the X16 IN clock is to be used as the bit rate clock. The baud rate select code for 110 baud is detected by two gates (U48, Pin 13 and U38, Pin 11) indicating two stop bits to the UART control and enabling the preset function of the divider chain to obtain 110 baud.

3.3.2.2 The Break flip-flop controls DATA OUT by making it high without regard to data being transmitted from the UART. $\overline{BREAK}$ is used by the terminal for remote interrupt to data processing equipment. If the Break flip-flop is not set, data is treated normally by the RS232C driver.

3.4 BAUD RATE GENERATOR.

3.4.1 The baud rate generator defines bit timing during transmit and receive operations. It consists of a 12-bit counter chain and a multiplexer which selects one of eight possible baud rates. The counter chain divides the terminal data bus System Clock (SYS CLK) down into useable baud rate frequencies.

3.4.2 Three counters (U32, U22, and U12) and an eight-input multiplexer (U42) comprise the baud rate generator. Seven of the baud rates are generated from the terminal System Clock and the eighth is an external input. As outputs, the PCA generates external signals equal to the baud rate times sixteen and times eight (TTL level signals).

3.4.2.1 The three counters generate six baud rates directly by dividing System Clock by factors of two. The other baud rate (110 baud) is not directly derived by dividing by two. The select code for 110 baud is detected (U48, Pin 13 and U38, Pin 11) and a preset function is enabled when the counter chain overflows (U32, Pin 15). A constant is parallel-loaded into the last two counters (U32 and U22), which perform a divide by 175 instead of 256. This gives the transmit and receive clocks (X16) necessary for that baud rate (the frequency is exactly 1755 +/-1 Hz).

Baud Rate Summary

Baud Rate Select Bits Control Register 3	2	1	Baud Rate	Frequency (Hz)	System Clock (Divide by)
1	1	1	9600	153,600	32
1	1	0	4800	76,800	64
1	0	1	2400	38,400	128
1	0	0	1200	19,200	256
0	1	1	300	4,800	1024
0	1	0	150	2,400	2048
0	0	1	110	1,755	2800
0	0	0	External Clock In (max 10000)	(max 160 kHz)	-

3.4.2.2 The three baud rate select bits from the control logic go to a multiplexer (U42) in the baud rate generator. Seven of the baud rates are generated by the counter chain, the eighth is the $\overline{\text{X16 IN}}$ clock (P2-S) which can be no greater than 160 kHz (10,000 baud) and TTL specification levels. One output of the multiplexer goes to the UART clocks and the other to a buffer which provides a TTL level X16 baud rate clock (X16 OUT) at P2, Pin L. Flip-flop (U23, Pin 6) divides the baud rate clock to provide an external TTL level X8 Clock (X8 CLK) at P2, Pin K.

3.4.2.3 In addition to the above baud raes, 200 and 600 Baud may be selected. By disabling the external baud rate generater (close switch $\overline{\text{EBE}}$), setting baud rate to EXT, and enabling either 200 or 600 Baud (by opening appropiate switch), the user can select either 200 or 600 Baud.

3.5 RS232C DRIVERS.

3.5.1 The interface between the Enhanced Asynchronous Datacom Module and external devices conforms to the EIA RS232C standard, which specifies electrical and logical operation, interface limitation, and defines the signal functions. The RS232C interface allows the PCA and thus the terminal to be connected locally to data processing equipment or to modems for remote operation using the telephone network. The RS232C drivers provide serial data out and three control outputs.

3.5.2 The interface signals are available at the PCA rear connector (P2) for connection to a cable assembly. The RS232C voltage outputs are signals converted from TTL levels (+5 volts and ground) by integrated circuit drivers (U39 and U49).

The $\overline{\text{REQUEST TO SEND}}$ output comes directly from the control logic at U22, Pin 7 and is used in modem applications to begin a transmit operation. The DATA TERMINAL READY output is always high (except in auto dial timer mode)the terminal power is on. Secondary Channel Transmit (SA) is used on Bell 202 or equivalent data sets and is high unless the

Break flip-flop (U43, Pin 7) is low or $\overline{\text{REQUEST TO SEND}}$ is low. Capacitors C6 are used for slew rate control.

3.6 RS232C RECEIVERS. The RS232C receivers also meet the EIA standard and provide DATA IN and three control inputs. The RS232C inputs are converted to TTL levels by integrated circuit receivers (U19,U29). Capacitors C7, C8, C9, and C10 on the input receivers are used for noise suppression. DATA IN (BB), is converted to TTL levels by the receiver and goes directly to the UART. Four inputs (CF, CB, CC, SB) are provided for modem status monitoring by the terminal processor.

3.7 TIMER ROUTINES - Several Critical timing functions must be performed to implement the auto dial feature. By programming (in firmware) the Baud Rate Generator to 110 Baud, and using the X8 clock, we have a timer of 1.12 ms duration. By counting these timer interrupts, critical times of longer duration be achieved with a high accuracy. Specific timer firmware controls are shown in Table 6.4.

3.8 TRANSMIT HANDSHAKE

3.8.1 The transmit handshake circuit provides the capability of handshaking transmitted data with an RS232C control line. When the transmit

handshake circuit is enabled ($\overline{\text{THE}}$ Switch open), the terminal responds to the CB control line temporarily stopping data transmission. Transmisssion is halted by turning off the Transmit Ready Status bit.

3.8.2 This circuit is a 2-state, syschronous machine that is clocked at 16 times the transmit baud rate. CB must be stable at the middle of the last sixteenth of the last stop bit of a character with at least 150 nanoseconds of setup time. The Off state of CB signals a "busy" condition. If a "busy" signal appears at CB, then the transmission will be held off temporarily.

3.9 FIFO BUFFER

3.9.1 In order to give the main processor enough time to receive and process incoming characters from the datacom interface card, an extra layer of buffering (U14 and U15) is added to the existing one character buffer available within the UART. Serial data flow therefore is from the RS232C signal interface to the UART, the resulting parallel data is routed to the buffer and then finally is gated onto the backplane when the proper signal (from the processor) is received.

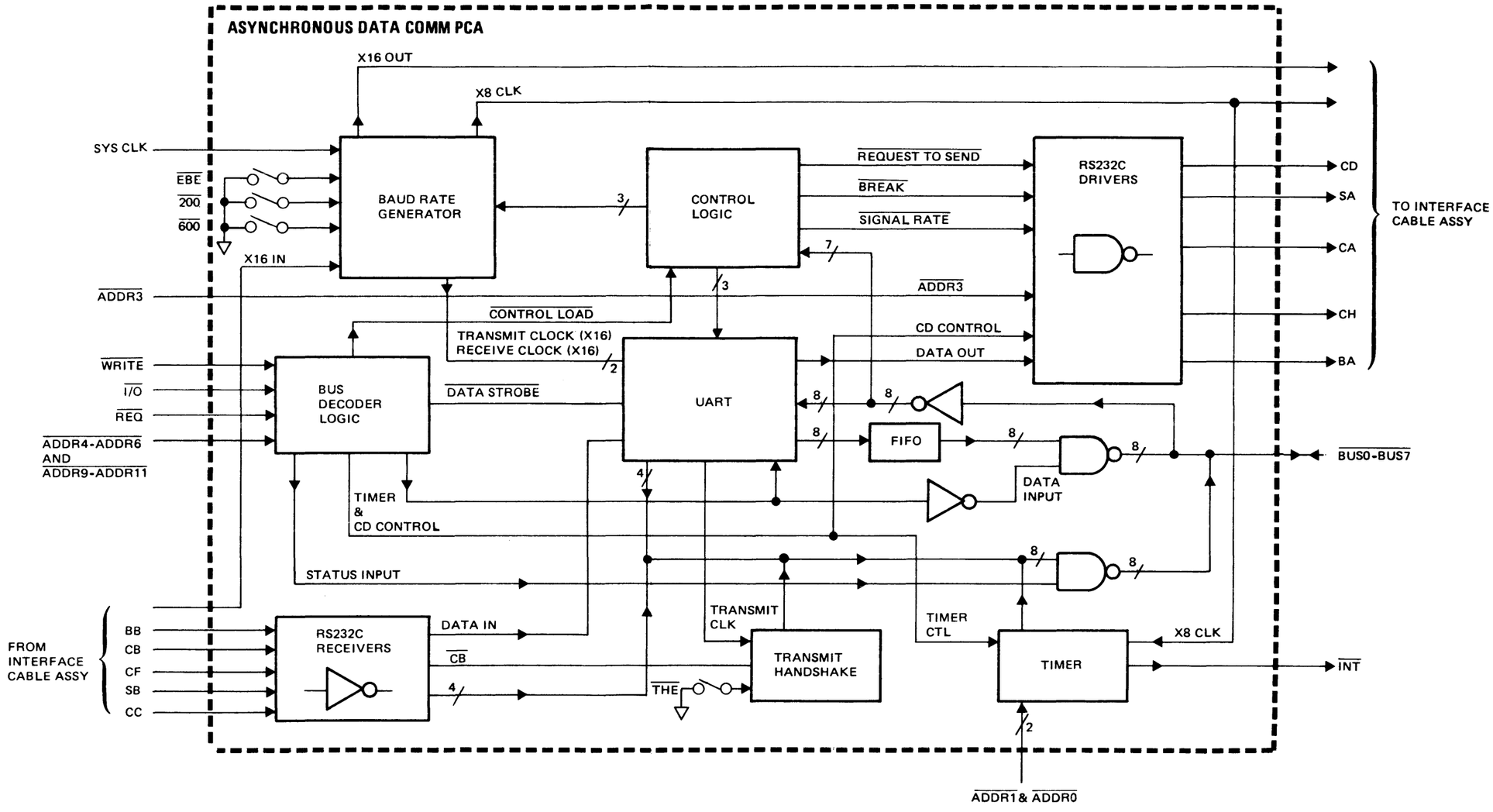

Figure 1
Enhanced Asynchronous Datacom Block Diagram
OCT-15-79 13255-91239

BAUD RATE GENERATOR

P2-E TEST

P2-S X16 IN

P2-K X8 CLK

P2-L X16 CLK

P2-D CH

P2-M SCA

P2-B PA

P2-R CH

P2-P CD

P2-C BB

P2-J CF

P2-E A3

P2-N SB

P2-F M

SYS CLK P1-3

PWRON P1-D

BUS7 P1-N
BUS6 P1-M
BUS5 P1-L
BUS4 P1-K
BUS3 P1-J
BUS2 P1-H
BUS1 P1-F
BUS0 P1-E

ADIT P1-16
AD10 P1-15
AD9 P1-14
AD4 P1-9
REQ P1-Y
IO P1-21
WRITE P1-P
AD6 P1-11
AD5 P1-10

AD3 P1-8
AD1 P1-6
AD0 P1-5
ATN P1-7

Figure 2
Enhanced Asynchronous Datacom PCA Schematic Diagram
OCT-15-79
13255-91239

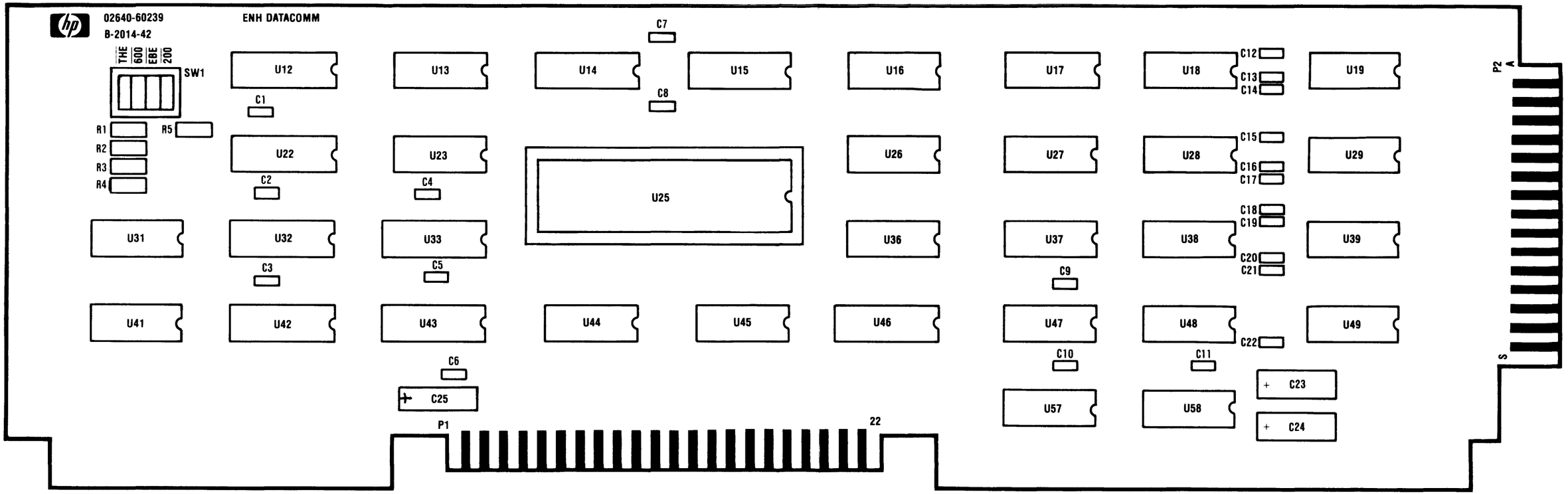

Figure 3
Enhanced Asynchronous Datacom PCA Component Location Diagram
OCT-15-79 13255-91239

Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	02640-60239	7	1	ENHANCED ASYNCH DATACOMM-PCA DATA CODE:B-2014-42	28480	02640-60239
C1	0160-4554	7	11	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C2	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C4	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C5	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C6	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C8	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C9	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C10	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C11	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C12	0160-4574	1	10	CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C13	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C14	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C15	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C16	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C17	0160-4801	7	1	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C18	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C19	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C20	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C21	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C22	0160-4574	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4574
C23	0180-2879	7	3	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C24	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C25	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
F1	2110-0423	8	3	FUSE-1.5A AXIAL LEAD	28480	2110-0423
F2	2110-0423	8		FUSE-1.5A AXIAL LEAD	28480	2110-0423
F3	2110-0423	8		FUSE-1.5A AXIAL LEAD	28480	2110-0423
J1	1251-1126	7	1	CONNECTOR-SGL CONT SKT .08-IN-BSC-SZ RND	28480	1251-1126
R1	0683-4725	2	4	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R2	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R3	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R4	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R5	0683-1025	9	1	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
SW1	3101-2063	8	1	SWITCH-TOGGLE 4-1A NS	28480	3101-2063
U12	1820-0778	0	3	IC CNTR TTL L BIN SYNCHRO POS-EDGE-TRIG	07263	93L16PC
U13	1820-1209	4	5	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U14	1820-1196	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U15	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U16	1820-1209	4		IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U17	1820-1209	4		IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U18	1820-1209	4		IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U19	1820-0990	8	2	IC RCVR DTL NAND LINE QUAD	04713	MC1489AL
U22	1820-0778	0		IC CNTR TTL L BIN SYNCHRO POS-EDGE-TRIG	07263	93L16PC
U23	1820-1112	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U25	1820-1219	6	1	IC UART PMOS	52840	TR1602A
U26	1820-1209	4		IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U27	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U28	1820-1197	9	3	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U29	1820-0990	8		IC RCVR DTL NAND LINE QUAD	04713	MC1489AL
U31	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U32	1820-0778	0		IC CNTR TTL L BIN SYNCHRO POS-EDGE-TRIG	07263	93L16PC
U33	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112AN
U36	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U37	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U38	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U39	1820-0509	5	2	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U41	1820-1202	7	2	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U42	1820-1217	4	1	IC MUXR/DATA-SEL TTL LS 8-TO-1-LINE	01295	SN74LS151N
U43	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U44	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U45	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U46	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
U47	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U48	1820-1074	1	1	IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
U49	1820-0509	5		IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U57	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
U58	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XU25	1200-0552	4	1	SOCKET-IC 40-CONT DIP-SLDR	28480	1200-0552
	0360-0124	3	1	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85062
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
52840	WESTERN DIGITAL CORP	NEWPORT BEACH	CA	92626
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
91637	DALE ELECTRONICS INC	COLUMBUS	NE	68601