# HP 13255 <br> CARTRIDGE TAPE MODULE <br> Manual Part No. 13255-91032 <br> PRINTED <br> AUG-01-76 <br> DATA TERMINAL TECHNICAL INFORMATION 




#### Abstract

1.0 INTRODUCTION.

The Cartridge Tape Module consists of a Cartridge Tape Unit (CTU) Interface PCA, a Readiwrite PCA, a CTU Top Plane Assembly, two CTU Transport Assemblies, and one or more mini tape cartridges. Each tape cartridqe contains 150 feet of single-track $0.150-i n c h$ tape with a maximum formatted storage capacity of 110 K eight-bit data bytes. The dual cartridge tape units provide full read and write capabilities for phase-encoded data. Data, command, status information, and address interfacing between this subsection and other terminal modules is provided by the Backplane Assembly and CTU Interface PCA. The Read/Write PCA controls recording, reading, and tape motion of the two ctu Transport Assemblies. Interfacing between the two PCA's is provided by the CTU Top Plane Assembly and interfacing between the Read/write PCA and the two CTU Transport Assemblies is provided by a Motor Cable Assembly and two CTU ribbon cable assemblies.


### 2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Cartridge Tape Module is contained in tables 1.0 through 5.3.

Table 1.0 Physical Parameters


1 Number of Backplane Slots Required: 2


HP 13255

## CARTRIDGE TAPE MODULE

Manual Part No. 13255-91032
PRINTED
AUG-01-76

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NOTE: This document is part of the $264 \times X$ DATA TERMINAL product series Technical Information Package (HP 13255).

### 1.0 INTRODUCTION.

The Cartridge Tape Module consists of a Cartridge Tape Unit (CTU) Interface PCA, a Read/write PCA, a CTU Top Plane Assembly, two CTU Transport Assemblies, and one or more mini tape cartridges. Each tape cartridqe contains 150 feet of single-track $0.150-i n c h$ tape with a maximum formatted storage capacity of 110 K eight-bit data bytes. The dual cartridge tape units provide full read and write capabilities for phase-encoded data. Data, command, status information, and address interfacing between this subsection and other terminal modules is provided by the Backplane Assembly and CTU Interface PCA. The Read/Write PCA controls recording, reading, and tape motion of the two cTu Transport Assemblies. Interfacing between the two PCA's is provided by the CTU Top Plane Assembly and interfacing between the Read/write PCA and the two CTU Transport Assemblies is provided by a motor cable assembly and two CTU ribbon cable assemblies.
2.0 OPERATING PARAMETERS.

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Table 1.0 Physical Parameters


Table 2.0 Reliability and Environmental Information


Iaple 3.0 Total Module power Supply and Clock Requirements - Measured While Accelerating to 60 ips (At $+/-5 \%$ Unless otherwise Specified)


Table 4.0 Connector Information for CTU Interface PCA



Table 4.0 Connector Information for CTU Interface PCA (Cont ${ }^{\circ}$. )


Table 4.1 Connector Information for CTU Interface PCA


Table 4.2 Connector Intormation for Read/inite PCA


Table 4.3 Connector Information for Read/Write PCA



-2 i GND 1 Ground common Return (Power and sianal)

Ground Common Return (Power and Sianal)
Not Used

- 12 Volt Power Supply
is
Pin -51 I\} 1
through 1 is

Pin-22 1
|-P1, Pin A $\mid$
tnrough 1 I)
Not Used
$\mathrm{Pin}-\mathrm{B}$
$-\mathrm{C}$
Pin - D
through Pin -5 i
$-T \quad$ PRIOR IN 1

- 11 P 1 PRIUR OUT 1

Not UsedI

Table 4.4 Connector Information for Read/write PCA (Cont ${ }^{\circ} d_{\text {. }}$ )


Table 4.5 Connector Information for Cartridge Electronics PCA


Table 5.0 Module Bus Pin Assignments


Table 5.1 Module Bus Pin Assignments


Table 5.2 Module Bus Pin Assignments


BL - RIP indicates the presence of head current while recording a gap. The state of this signal is not defined during read operations or while data is being recorded.

0 = No write current (tape protected)
1 = Write current present while in gap
BI - CIR indicates that a cartridge is inserted in the right CTU Transport Assembly and is cleared when the cartridge is removed.
$0=$ No cartridge in riaht CTU Transport Assembly
1 = Cartridge inserted in right CTU Transport Assembly
$B 0=C I L$ indicates that a cartridge is inserted in the left ctu Transport Assembly and is cleared when the cartridge is removed.
$0=$ No cartridge in left CTU Transport Assembly
1 = Cartridge inserted in left CTU Transport Assembly

Table 5.3 Module Bus Pin Assignments


| 3 | FUNCTIONAL DESCRIPTION - CTU InTERFACE PCA. Refer to the block diaqram (figure 1), schematic diagram (figure 2), component location diagram (figure 3), and parts lists (02640-60021 and 02640-60033) located in the appendix. <br> The terminal processor communicates with the Cartridge Tape Module via the terminal bus (Backplane Assembly). The CTU Interface PCA is responsible for converting processor commands into siqnals to control tape motion, unit selection, read or write operation, and the state of the efect button lights. The CTU Interface PCA provides status information allowing the processor to determine the present state of the selected CTU Transport Assembly. Finally, the CTU Interface PCA encodes data bytes into serial patterns of bit transitions to be recorded on the tape and vice versa (i.e.. decodes bit transitions on the tape into data bytes). |
| :---: | :---: |

3.0.1 BUS FUNCTION DECODER AND TIMING LOGIC - CTU INTERFACE PCA.
3.0.1.1 The bus tunction decoder and timing logic generates signals based upon inputs from the terminal bus which control the flow of commands, status, and data bytes to and from the terminal bus.
3.0.1.2 The bus function decoder (U16) generates one of four command signals by decoding $\overline{W R I T E}$ and $\overline{A D D R} \overline{5}$. The commands are enabled by $\overline{I / O}$ (for an
 In addition, data clock, RD+WRT, RD/wRT SELECT, READ EN, and STATUS EN are generated.
3.0.2 COMMAND LOGIC - CTU INTERFACE PCA.
3.0.2.1 The purpose of the command logic is to acquire command information from the terminal bus when the signals are valia. The command information completely specifies the operation as well as the selection of the ctu Transport assemblies. In addition, the command logic stops tape motion thus oreventing tape runoff when a hole is detected by the hole detect logic.
3.0.2.2 The command signals from the terminal bus are latched into 015 , U21 (Pins 5 and 0 ), and 024 by the CMND CLK signal from the bus function decoder and timing logic.

Two versions of the Run command are contained in the command register (U15). SPUN (Servo kun) is generated at U24, Pin 8 to enable the tape motion decoder (U16). SRUN is cleared if the hole edae detector (U23, Pin 12) detects a transition into a nole. IRUN (Interface Run) is generated at U24, Pin 6 to enable the slow forward tape motion decoder at

U36, Pin 8 which generates ISF (used only by the encoder/decoder logic). This prevents a discontinuity in encoded or decoded data when movina across a hole. Both SRUN and IRUN are cleared after a system reset.

The $\overline{S R U N}, \overline{F O R W A R D}$, and $\overline{F A S T}$ signals are translated in this block into the signals $\overline{\operatorname{SREV}}$ (slow reverse), $\overline{\operatorname{SFD}}$ (slow forward), FREV (fast reverse), and $F F D$ (fast forward) which are used by the servo electronics on the Read/write PCA.

The CLRINT sianal is generated for the interrupt logic by u27, Pin 8 when the processor performs a status request, enabling the STATUS EN signal. The CLRINT signal is present for one cycle of SYS CLK after STATUS EN goes low.
3.0.3 DATA PATH CONTROL - CTU INTERFACE PCA.
3.0.3.1 The data path control circuitry transfers data to and from the terminal bus. It also converts serial bits from the tape into bytes and converts bytes trom the terminal bus into serial bits.
3.0.3.2 The data $1 / 0$ buffer (U13 and $U 33$ ) is an 8-bit register with a 2-port input multiplexer. It provides one byte of buffering between the terminal bus and the serial data register.
3.0.3.3 In Record mode, the data is loaded into the data $1 / 0$ buffer from the terminal bus, enabled by RD/WRT SELECT being low. (Note that the data buffer is loaded with complement data since it is loaded from the ground true terminal bus.) The data byte is loaded into the serial data register after the previous byte nas been encoded. The serial
data register is then shifted right (via REC DATA) into the encoder at mid cell point (data transition position) and the encoder is complemented at end cell point (phase position).
3.0.3.4 In Read mode, the serial biphase data is read into the transition detector (U28. Pin 14) of the encoder/decoder logic and shifted into
the serial data register at the appropriate time corresponding to the zone for data transitions). When the last data bit has been detected at the decoder (there are 7 bits in the serial data register), the data I/O buffer is parallel loaded from the serial data register (shifted right one Dit). The data $1 / 0$ buffer is subsequently output to the terminal bus via drivers U11 and U32, which are enabled by the READ EN signal.
3.0.4 ENCODER/DECODER LOGIC - CTU INTERFACE PCA.
3.0.4.1 This logic provides the timing and control functions for encoding or decoding a data byte. The operation of the encoder/decoder logic is based upon the following theoretical analysis. The code that is recorded on the cartridge tape is Serial Biphase Mark Code (see below). Therefore, the code shown below would be seen at the encoder output (U17, Pin 10) when in Record mode or at the transition detector (U28, Pin 15) in Read mode. The code rules state that there is always a data transition at mid cell, a l-bit is a transition towards gap level while a 0 -bit is a transition away from gap level, and a phase transition occurs at a cell houndary if adjacent data transitions are the same.

*Indicates cell boundaries (125 microseconds)
3.0.4.2 Timing and control for the encode and decode operations is provided by a cell decode counter (J212) and a variable modulus (divide by N) counter (J213, U214, U312, and U313) which are both synchronous with the bus System Clock. The variable modulus counter generates a carry output at time intervals equal to one biphase cell period divided by eight which increments the cell decode counter. By initializing both counters at the beginning of a biphase cell, timing points (for encoding phase and data transitions in Read mode) and timing zones (for decoding phase and data transitions in kead mode) can be decoded from the cell decode counter and variable modulus counter carry output.

The variable modulus counter consists of two counters. one is an $8-b i t$ counter (U213 and U214) which counts from a base state to the overflow state (which generates a carry output); the second is an 8-bit up-down counter which contains the value of the base state. The up-down counter is loaded with the two's complement of the desired modulus. In Record mode, the up-down counter is reset (U311, Pin 11 and U313, pin 11) to the two's complement of 115 octal ( 77 decimal) giving a carry output at


In Read mode, the up-down counter is initialized to the same value. Then, based on the actual frequency of the phase/data transitions, the up-down counter is incremented or decremented. (Note that incrementing the up-down counter decrements the modulus of the counter.)

The cell decode counter is decoded as follows when in kecord mode.


When in Read mode, the cell decode counter appears as follows.


| 0.4 .3 | The encoder operation can be best explained by considering the recording of a gap and a 2-byte preamble. The preamble consists of a zero byte and a byte with the value 200 octal. |
| :---: | :---: |
|  | First, the command RUN.FORWARD.RECORD.GAP is output to the command register from the processor. This sets the encoder to record flux in the gap direction. Additionally, the command sets the modulus of the variable modulus counter to 77 and enables the preset signals of the variable modulus, bit, and cell decode counters. while the gap is |
|  | time. Since $D Z X$ is set when in record mode, this results in the serial data register being loaded serially with all $1^{\prime}$ s. Because the data register contains the complement data, the register is effectively loaded with the first preamble byte (all zeroes). |
|  | After the proper gap interval has been recorded, the GAP command is turned off and the last preamble byte is loaded into the data $1 / 0$ |
|  | buffer. When $\overline{R E C} G A P$ is set, the preset signals on the variable modulus, bit, and cell decode counters are removed and the encoder is no longer forced to record in the gap direction. |
|  | Each bit is recorded (encoded) as follows: |
|  | 1) The variable modulus counter counts up and generates a carry output (CIN) every 77 system clocks. The carry output increments the cell decode counter. |
|  | 2) Tne cell decode counter is decoded at mid cell setting the |
|  | encoder to DATA (the value of the rightmost bit of the serial data register), and the serial data reaister is shifted right |
|  | 3) At end cell, the bit counter increments, the encoder is complemented, and the cell decode ana variable modulus counters are initialized. |

The process is repeated for each of the eight data bits. After all eight bits have been encoded, the bit counter, cell decode counter, and the variable modulus counter are initialized. The serial data register is loaded from the data I/O buffer and BYTE RDY is set. If byTE RDY signal is already set, then data is not loaded from the data I/O buffer and the same byte is recorded, shifted right one bit.


When the preamble begins to be read, the gap detect circuitry indicates data present. This causes the preset to be removed from the modulus of the variable modulus counter which allows the modulus to be adjusted accordingly. The decoder then proceeds as follows-

The variable modulus counter counts up and generats CiN every $N$ system clocks ( $N$ is initially 77). CIN increments the cell decode
counter. When a transition is sensed by the $\overline{D Z X}$ transition detector, it is decoded using the cell decode counter and results in one of three possiole actions:

1) Transition occurs in the illegal zone- the cell decode and variable modulus counters are initialized. The process continues waiting for the next transition.
2) Transition occurs in the phase zone- the modulus of the variable modulus counter is incremented or decremented (see 3.0.4.2) and the cell decode and variable modulus counters are initialized. The process continues waiting for the next transition.
3) Transition occurs in the data zone- the modulus of the variable modulus counter is incremented or decremented (see 3.0.4.2) and the cell decode and variable modulus counters are initialized. If the data is decoded as a zero ("0"), the process continues waiting for the next transition. Otherwise, a one ("1") indicates the end of the preamble and causes READ SYNC and BYTE RDY to be set.
when READ SYNC is set, the decoder will automatically switch modes to read in data bytes. The initial BYTE RDY indicates that the end of the preamble has been found. BYTF RDY must be cleared by either a RD dATA or WR DATA. However, the data byte read will be meaningless.

While reading in data, transitions detected are handled in the same manner as when reading the preamble except for transitions occuring in the data zone. In this case, RD DATA is shifted right into the serial data register and bit counter is incremented. when the last bit is decoded, the data $1 / 0$ buffer is parallel loaded from the serial data register (shifted right one bit), BYTE RDY is set, and the process is repeated for the next byte. The data in the $1 / 0$ buffer must be read (which clear ByTE RDY) before the next byte is decoded in order to avoid losina data.
3.0.5 HOLE DETECI LOGIC - CTU INTERFACE PCA.
3.0.5.1 This circuitry detects the presence of a hole in the tape of either ciu Transport assembly (depending on which transport is selected) and generates the DHOL, DHOL DET, and USO signals.
3.0.5.2 The Read/Write PCA provides the signals $\overline{H O L O}$ and $\overline{H O L I}$ that indicate the presence of a nole on Unit 0 or Unit 1 , resnectively when the signal is low. When Unit 1 is selected and a hole is detected, U22, Pin 11 will be high. When Unit 0 is selected, USO at U35, Pin 4 is high, a hole is detected, and U22, Pin 8 is high. Pins 8 and 11 of $U 22$ are wire ored into U 28 , Pin 6 where they are synchronized to sys CLK and provide the DHOL signal at U28, Pin 7. DHOL at U29, Pin 4 is exclusive-ORed with DHOL delayed by one cycle of SYS CLK at U29, Pin 5 and generates the DHOL DET siqnal which provides a pulse when a nole is initially detected and another pulse when it is no longer detected. It should be noted that DHOL and DHOL DET are ANDed in the command logic to orovide a single pulse when a nole is initially detected.
3.0.6 TACH lugic - CtU interface pCa.
3.0.6.1 The tach logic divides the TACH signal from the Read/Write PCA by a factor of two and uses the resulting signal to generate the signals TACH/2 and DTACH/2.
3.0.6.2 The TACH signal is used as the clock input for U26, which is configured as a filip-flop, and results in one transition of the signal at U26, Pin 6 for every two transitions of the $T A C H$ signal. $u 28$ synchronizes the signal from U26, Pin 6 with the SYS CLK and generates the TACH/2
signal for the status drivers. The $T A C H / 2$ signal is delayed one cycle of SYS CLK by U28, Pin 5 and is then exclusive-ORed to produce DTACH/2 at U29, Pin 8. DTACH/2 produces a pulse at each transition of TACH/2 with a width equal to one cycle of SYS CLK.
3.0.7 STATUS DRIVERS - CTU INTERFACE PCA.
3.0.7.1 The status drivers present status information for the module to the terminal bus.
3.0.7.2 The CINO, CIN1, RIP, and INTERRUPT signals are gated onto the terminal bus by U31 which is enabled by STATUS EN. The signals are inverted on the bus to provide ground true logic levels. The TACH, HOLE, GAP, and BYTE RDY signals are gated onto the terminal bus by $U 12$ which is enabled by STATUS EN.
3.0.8 INTERRUPT LOGIC - CTU INTERFACE PCA.
3.0.8.1 The interrupt logic provides an interrupt when a transition occurs in
the tach/2 signal, when a nole is present, or when a byte of data must
be received or sent from the processor.
3.0.8.2 The DTACH/2 signal sets flip-flop U25, causing Pin 9 to be low when a transition occurs in TACH/2. The CLRINT signal from the command logic resets $U 25$, causing Pin 9 to go high. The DHOL signal sets flip-flop U25, causing Pin 7 to be low, and indicates the presence of a hole in the tape. The CLRINT signal resets U25, causing Pin 7 to go high.
when U25, Pin 9 is low or U25, Pin 7 is low or BYTE RDY is low, or some combination of these events occurs, then INTERRUPT will be hiqh. This
causes $\overline{A r N 2}$ to be low thereby indicating an interrupt condition to the
processor. If U 25 , Pin 7 is high and $\overline{\mathrm{BYTE}} \overline{\mathrm{RDY}}$ is nigh, then no interrupt condition exists and INTERRUPT will be low.
3.1 FUNCTIUNAL DESCRIPTIUN - READ/WRITE PCA. Refer to the block diagram (fiqure 4), schematic diagram (figure 5), component location diagram (figure 6), and parts list (02640-60032) located in the appendix.

The Read/write PCA contains circuitry to record flux transitions onto cartridges in either CTU Transport, to convert flux transitions recorded on the cartridges into $T$ th signal levels, and to detect the
presence of gap (absence of flux transitions) on the tape. In addition, this PCA contains the servo electronics for controlling tape motion and speed for either CTU lransport. Analysis of the PCA indicates that much of the circuitry is common for servo control and read/ write operations. The routing of signals is accomplished for each drive by the read select switch, the unit function decoder, the amplifier select logic, and the tachometer feedback select and conditioning circuits. (Refer to the block diagram in figure 4.)
3.1.1 UNIT FUNCTION DECODFR - READ/WRITE PCA.
3.1.1.1 The unit function decoder (U3) is a $1-0 f-10$ decoder which determines whether the Read/write PCA is in Read or Write mode. It also determines the ctu Transport from which flux transitions are received, or to which flux transitions are sent.
3.1.1.2 When $\overline{R E}$ and line $\overline{U S O}$ are $10 w, \bar{Q} \overline{0}$ and $\overline{Q 1}$ are active outputs and Head 1 is driven by $\overline{D A T A}$ as shown in the truth table below. when $\overline{R E}$ is low, and USO is high, $\overline{Q 2}$ and $\overline{Q 3}$ are active outputs and Head 0 is drven by $\overline{D A T A}$ as shown below.

```
1-Df - 10 Decoder (U3)
    Truth Table
```

| 1 | INPUTS |  |  | 1 |  |  |  | OUTPUTS |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 1 | -- |  | - | 1 |  |  |  |  | -- |  |  |  |
| 1 | RE | USO | DATA | 1 | Q0 | 01 | Q2 | Q3 | 04 | Q5 | Q6 | Q7 |
|  |  |  |  |  |  |  |  |  |  |  |  |  |
| 1 |  |  | ----- | 1 |  |  |  |  |  |  |  |  |
| 1 | 1 L | L | LI | 1 | 1 L | HI | H | H | H | H | H | H |
| 1 | 1 L | L | H H | 1 | 1H | LI | H | H | H | H | H | H |
| 1 |  |  | ------ | 1 |  |  |  | -- |  |  |  |  |
| 1 | 1 L | H | LI | 1 | H | H | 1 L | HI | H | H | H | H |
| 1 | 1 L | H | HI | 1 | H | H | IH | LI | H | H | H | H |
|  |  |  | ---*- | 1 |  |  |  |  |  | -- |  |  |
| 1 | 1H | L | L L | 1 | H | H | H | H | IL | HI | H | H |
| 1 | IH | L | HI | 1 | H | H | H | H | IH | LI | H | H |
| 1 |  |  |  | 1 |  |  |  |  |  |  |  |  |
| 1 | IH | H | LI | 1 | H | H | H | H | H | H | 1L | HI |
| 1 | 1 H | H | HI | 1 | H | H | H | H | H | H | 1 H | L I |
| 1 |  |  | ----0- | 1 |  |  |  |  |  |  |  |  |

### 3.1.2 WRITE CURRENT CIRCUIT - READ/WRITE PCA.

3.1.2.1 The write current circuit provides the current source for either head as selected by the unit function decoder. In addition, the RIP signal is generated allowing the firmware to determine whether a cartridge is protected.
3.1.2.2 when $\overline{R E}$ is low (write) U17, Pin 4 is high and Q15 turns on. This, in turn, drives Q16, the current source, on. When $\overline{R E}$ is high (read), U17. Pin 4 is low and Q15 is cut off which in turn cuts off Q16. The emitter current of $Q 16$ is primarily determined by the +12 volts supply, R42, CR13, and is nominally 9.85 mA . when the current source (016) is off, the RIP driver (Q17) is turned on through R42, CR11, CR10, R44.
3.1.2.3 when the current source is on and supplying current to the head, the emitter of Q16 is at approximately +4.6 volts and CR11 isolates the base of Q17 from this voltaqe. The collector of $Q 16$ is at a low voltage when any one of U3's outputs (Pins 1, 2, 3, or 4) is low, then CR12 removes the drive to the base of 017 cutting it off. If the current source is on, and not supplying current to the head (i.e., the file protect switch is open, or the head leads are broken), the collector of Q16 is then connected to a high resistance path (CR12, R44, R49) and Q16 saturates causing most of its emitter current to flow out its base into $Q 15$ and CR13 to ground. Then the collector voltage of $Q 16$ which is now about the same as the emitter voltage, drives 917 on through CR12 and R44. The two paths driving 017 assure that RIP is true only when nead current is actually drawn.

3.1.3 READ SELECT SWITCH - READ/WRITE PCA.
3.1.3.1 The read select switch (U16) is a FEr switch used to connect the head on the selected cTu Transport Assembly with the preamp in the read amplifier circuit when the Read/write PCA is in the Read mode.

# 3.1.3.2 Refer to the truth table in section 3.1.1.2 for a summary of the following. When $\overline{R E}$ is nigh (read) and USO is low (DATA is a don't care), Q4 and Q5 are tied togetner and go low. This arives Ui7, Pin 12 high turning switches 1 and 2 on and Head 1 is connected to the preamp. <br> when $\overline{R E}$ and Us0 are high ( $\overline{D A T A}$ is a don't care), 06 and 07 are tied together and go low. This drives ul7, Pin 6 high turning switches 3 and 4 on and Head 0 is connected to the preamp. 

3.1.4 READ AMPLIFIER CIRCUIT - READ/WRITE PCA.


#### Abstract

3.1.4.1 The read amplifier circuit amplifies the input signal from either head, differentiates the signal so that the peaks of the flux transitions become zero crossing, and then detects these zero crossings to produce a TTL signal with transitions at each zero crossings (flux transitions peak).


3.1.4.2 The preamp (U5) is a differential input/differential output op-amp. Its gain is determined by k 39 and R40 plus the MUS switch on resistance in one leg, and by R38 and R41 plus the MOS switch on resistance in the other leg. The differential gain is 40 dB . R38 and C36 on one side, and R39 and C39 on the other side, roll off the response starting at 30 kHz . C40 resonates the head at approximately 50 kHz , effectively compensating for some loss in the head output.
3.1.4.3 Differentiator (U4) is also a differential input/differential output op-amp. Its differentiating characteristics are determined by C21, R46, C16, and R34 in one leg, and by R47, C22, C19, and R35 in the other leg. Its gain at the two frequencies of interest ( 4 kHz and 8 KHz ) is $\mathbf{- 2} \mathrm{dB}$ and +4 dB , respectively. C21 with R46, and C22 with R47 stop its gain rise at +20 cB at 80 kHz ; and R34 with C16, R34 with C16, R34 with C16, and R35 with C19 start its roll off at 160 kHz . The preamp outputs are connected to this differentiator which translates each amplitude peak of the preamp outputs to zero crossings.
3.1.4.4 The differentiator outputs are ac coupled at Pins 8 and 9 to comparator U1. The two inputs to $u 1$ are lifted off ground and reference to +5 V through R101F and R101G. This is necessary because this particular comparator must not have its inputs allowed to go below -0.3 vdc. This comparator detects the zero crossings of the differentiator outputs and changes state each time, effectively squaring the differentiator output waveform. A small amount of nysteresis is used to assure that
the comparator output is at the correct polarity, i.e., low in the steady state (no data) and also to give it a snap action when a state change occurs. The positive feedback is derived from the output of U13. Pin 4. Since the comparator inputs are referenced to +5 volts, a level shifting is required and is accomplished by CR4, R33 and R32. In the high state, the output of U13, Pin 4 must be kept at a Tt level and CR4, R33 and R32 are also responsible for that. This voltage is +4.4 volts nominally. The +4.4 volts plus the CR4 Zener voltage make the voltaqe level at the junction of R33, R48, and CR4 equal to +10.6 volts. In the low state, the voltage at this junction is the CR4 voltage plus the low output voltage of U13, Pin 4 (or approximately +6.6 volts). Therefore at this junction, a rectangular wave exists between +6.6 volts and +10.6 volts. The hysteresis voltage is then derived from this through the R48, R101G divider. Nominally, Pin 8 of U 1 is 32 millivolts positive with respect to pin 9.

### 3.1.5 GAP DETECT CIRCUIT - READ/WRITE PCA.

3.1.5.1 The gap detect circuit provides the GAP signal, which indicates the absence of flux transitions (if GAP is high) or the presence of flux transitions (if GAP is low). Whenever flux transitions beqin or terminate, the GAP signal reflects this change after a delay of eight bit times.
3.1.5.2 A single output (U5. Pin 4) is also ac coupled to Ul at pin 10 , used here as a threshold detector. The two inputs of this comparator are referenced to +6 volts through R36 and R37. The threshold level is set by R103E and R37 and is nominally +0.057 volts, which is 15 per cent of the specified 1600 FRPI nead output times the gain of the preamp. Pin 11 of U 1 is +0.057 volts positive with respect to pin 10 . The output of U 1 . Pin 13 will change state every time the input to pin 10 reaches this level, up or down. As a result, the output is not perfectly symmetrical, but has a duty cycle of approximately $45 / 55$ at 1600 FRPI .
3.1.5.3 The output of U1, Pin 13 drives the integrator driver (018). R57, R58, and C45 together with U13, Pin 6 form the gap detector. U13, Pin 6 (a Schmitt-Trigger) triggers on at +1.7 volts and off at +0.9 volts. The time constants of the integrator are proportioned so that eight bit times at 1600 FRPI (or 1 millisecond) is required to reach the on level. This delay assures that the gap detect circuitry will not be triggered by random noise. once $u 13$, Pin 6 is on (output low) and data is received, GAP will be false. When data stops, C45 will begin to discharge through R58 and Q18; when its level reaches +0. 9 volts, U13, pin 6 will trigger off indicating beginning of gap. Nominally, this
time is also 1 millisecond. Therefore, GAP is true 1 millisecond after data stops until 1 millisecond into the next block. The output of U13, pin 4 is connected to pin 10 of U12 and the output of U13, Pin 6 is
connected to OR gate U12, Pin 9. This serves to quiet the DZX output during gap time.
3.1.6 TACHOMETER FEFDBACK SELECT AND CONDITIONING CIRCUITS - READ/WRITE PCA.
3.1.6.1 The tachometer feedback select and conditioning circuits condition the inputs from the tachometers by filtering and by comparison and then select the signal from the tachometer associated with the ctu Transport that is selected.
3.1.6.2 The tachometer on the capstan drive motor is a variable reluctance type which produces a sine wave output of approximately 300 millivolts peak-to-peak at 10 inches per second tape speed. This signal is fed into the Read/Write PCA. The signal nas a 0.027 microfarad (C2 and C4) filter capacitor shunting it to roll off the output of the tachometer above the frequencies of interest ( 4 kHz ). A tach signal then drives a comparator (U1. Pin 6 or U1, Pin 4) with positive nysteresis (33 millivolts). NAND gates Ull select the signal TACH FREQ from the selected CTU Transport. This signal drives a delay circuit producing the DELAYED PACH signal.
3.1.7 AMPLIFIER SELECT LOGIC - READ/WRITE PCA.
3.1.7.1 The amplifier select logic determines which motor is to be driven based upon which CTU Transport is selected.
3.1.7.2 If the RUNG signal is $10 w$, then $1 S E L$ and $0 S E L$ are $h i g h$, inhibiting the motor drive circuitry. If RUNG is high, both gates of Uil in this block are enabled. If Unit 0 is selected (USO high) and a cartridge is inserted in Unit 0 (CINO high), then OSEL will be low, selecting the CTU drive circuits associated with CTU Transport Unit 0 . on the other hand, if Unit 1 is selected (USO low) and a cartridge is inserted in Unit 1 (CINi high), then $1 S E L$ will be low, selecting the CTU drive circuits associated with CTU Transport Unit 1.

### 3.1.8 COMMAND RAMP AND FEEDBACK CIRCUITS - READ/WRITE PCA.


#### Abstract

3.1.8.1 The command ramp circuits translate command signals to move the tape fast forward, slow forward, fast reverse, and slow reverse into ramped voltages used by the CTU drive circuits. The feedoack circuit provides a voltage directly proportional to the speed of the motor. The feedback Voltage (FDBK VULTAGE) and the Ramp Command Voltage (RAMP VOLTAGE) are summed to provide an error signal for the power amplifiers in the CTU drive circuits.


3.1.8.2 $\overline{F F D}, \overline{S F D}, \overline{F R E V}$ and $\overline{S R E V}$ run command lines drive open-collector TTL inverters which have 10 kilonm pullup resistors to a 10 -volt Zener reference. unly one input should be pulled low at any one time. These commands cause the servo to drive at $+60,+10,-60$ and -10 ips. Fast and slow command voltage values are determined by the relative values of R12 through R15. Reverse commands are inverted hefore being applied to the ramp circuit by op-amp $u 6$ (all op-amos are dual internally compensated op-amp packages). The two op-amps (U8) make up the ramp circuit which together are analogous to a single inverting op-amp with a slow linear slew rate. The first half of the ramp circuit is a nigh gain (196K divided by $1 \mathrm{kilonm}=196$ ) voltage driver which supplies bias current to a bidrectional voltage reference composed of CR5 and CR6. This reference voltage (approximately $+/-6.9$ volts) is supplied to the second op-amp operated as a Miller integrator and has a slew rate of 6.9 volts divided by R23, all divided by C27 (31 volts per second). R22 feeds back the output of the integrator which sets the dc gain of the ramp circuitry. The output for slow commands is $+/-1.2$ volts and for high speed commands is $+/-7.2$ volts.

Q3, Q4, U13, and opmamp U6 form a bidirectional threshold detector that indicates the polarity of the command voltage as well as the 1 ips (either forward or reverse) threshold of the ramp command voltage, generating the signals +FDBK FN and -FDBK EN.
3.1.8.3 The TACH FREQ and DELAYED TACH signals go into an exclusive-OR gate made up of 412 and two gates of Ul5. The output of the exclusive-or gate is a pulse for every input transition, thus doubling the frequency of the tach signal. This double frequency signal drives a precision one-shot whose output ( 93 microsec ond period) is fed to one of two TTL open-collector buffers (U10), depending on the desired feedback polarity. The feedback polarity is determined by the polarity of the command voltage. The $+F D B K E N$ and $-F D B K E N$ signals gate the one-shot output to the appropriate rTh buffer. One TTL buffer output is in= verted by the first half of $U 7$, operated also as a 3 kHz low pass
filter. The filter integrates the pulses of the one-snot to help reduce the ripple on the feedback signal. Both tach feedback polarities are ted to the main 2 -pole minimum phase Chebychev filter (2 poles at 200 Hz ). This output is the servo Feedback voltage (FDBK voltage). The Feedback Voltage waveform looks like the ramp command waveform with extra ripple riding on it. This is risidual digital tach ripple that is not filtered out by the 2-pole filter, but instead is filtered out by the mechanical pole of the motor drive.
3.1.9 CTU DRIVE CIRCUITS - READ/WRITE PCA.
3.1.9.1 The CTU drive circuits use the error voltage generated at the summing junction as an input to the power amplifier determined by the selected CTU rransport driving the motor for that transport.
3.1.9.2 A 2-drive tape system nas two dc servo motors which must be selectively driven. The selection of the motor to be driven is done at the low signal level using junction field effect transistors. Each power amp has two Fers associated with it. The first FET (Q6 or Q10) switches a power amp to the power amp summing junction. The r55 speed adjust potentiometer and R25 convert the Ramp Voltages (RAMP VOLTAGE) to command currents into the power amp summing junction. In addition, FDBK VOLTAGE is changed to a feedback current by R24 into the power amp summing junction. The second FET ( 05 or 09 ) clamps the unused power amp off so that leakage currents cannot cause the non-selected motor to turn. The power amps are op-amps (U9) with high gain bipolar emitter followers (Q7 and Q8 or Q11 and Q12). The buffer power transistors are mounted on an aluminum heat sink.

The outputs of the power amplifiers are fed to the drive motors. The return side of the motors come through a current sensing resistor (R31). The motor current produces a voltage across this resistor which drives current limit detector transistors 013 and Q14. They clamp the power amp through diode bridge CR8. C32 and C33 stabilize the current limit feedback loop. The current sense voltage also is used for compensation of the velocity feedback loop by locally characterizing the response of the power amp through R29, R28, C34 and C35 back to the power amp summing junction. This compensation gives the servo velocity loop a 55 -hertz bandwidth (with typically 45 degrees phase margin and 12 dB gain margin).
3.1.10 CARTRIDGE DETECT CIRCUIT - READ/WRITE PCA.

### 3.1.10.1 The cartridge detect circuit delays the $\bar{C} I$ signal from the Ctu Transport allowing time for the CTU Transport to mechanically stabilize after a cartridge is inserted.

| 3.1.10.2 | When a cartridge is inserted in Unit 1 , the $\bar{C} \bar{I}$ line is pulled low caus $=$ ing U17, Pin 8 to go high. This allows C3 to charge through R2 and R3. After approximately $1 / 2$ second, $Q 2$ turns on and pulls U13, Pin 1 low causing CIN1 to go high and indicating the presence of a cartridge. U13 is a Schmitt gate used to provide hysteresis so that the slow fall time of the collector $Q 2$ will not cause oscillations at the output of U13. <br> When the cartridge is ejected from Unit 1 , all actions of the signals are inverted with the exception of capacitor c 3 which discharges only through R2 (C3 discharges 464 times faster than it charges when a cartridge is inserted). The analysis for unit o cartridge insertion and ejection are similar, except that U17, Pin 10, R1, R50, C1, Q1, and U13. Pin 10 are involved in affecting the state of CiNo. |
| :---: | :---: |
| 3.2 | FUNCTIUNAL DESCRIPTION - CARTRIDGE ELECTRONICS PCA. Refer to the block diagram (figure 7), schematic diagram (figure 8), component location diagram (figure 9), and parts lists (02640-60034 and 02640-60066) located in the appendix. <br> The cartridge Electronics PCA is a small PCA (part of the head bridge assembly of the CTU Transport) mounted to the tape mechanism s head mount. This assembly includes a 14-conductor ribbon cable which plugs into the Read/write PCA. The ribbon cable provides all the electrical connections required by the mechanism, except motor current. |
| 3.2 .1 | CI SWITCH - CARTRIDGE ELECTRONICS PCA. |
| 3.2.1.1 | The Cartridge Inserted (CI) switch (S2) is activated by the presence of a cartridge in the mechanism. The information concerning the presence or absence of a cartridge is transferred to the firmware, which takes the appropriate action. |

3.2.1.2 When a cartridge is inserted, contact is made between two pads on the Cartridge Electronics PCA. This action connects the $\overline{C I}$ line to ground. when a cartridge is not inserted, the $\overline{C I}$ line is pulled to +5 volts by a resistor on the Read/write PCA. No "debouncing" circuitry is required since a delay is provided by circuitry on the Read/write PCA.
3.2.2 FP SWITCH - CARTRIDGE ELECTRONICS PCA.
3.2.2.1 The File Protect (FP) switch (S1) is activated when the RECORD tab on
the cartridge is in the record position. Ihis allows the user to
innibit accidental recording of data.
3.2.2.2 with the RECORD tab in the recora position, contact is made between two pads on the Cartridge flectronics PCA. This contact allows current to flow through the center tap of the head which causes recording on the tape. If contact is not made then data may not be recorded on the tape, irrespective of whether or not the Read/write circuitry is in the write mode.
3.2.3 LAMP DRTVER - CARTRTDGE ELECTRONICS PCA.
3.2.3.1 The lamp driver accepts the ground true Lamp ( $\bar{L}$ ) signal and drives the lamp used as an indicator for the user. The state of the lamp is controlled by the firmware.

3.2.4 HOLE DETECT - CARTRIDGE ELECTRONICS PCA.
3.2.4.1 The hole detect circuitry consists of a pulse generator and diode driver and a detection circuit. The hole detect circuit detects the
holes in the tape and provides a ground true signal (HOLE) that is used in the determination of BOT, load point (LP), early warning (EW), and EOT. Holes are detected with an infrared emitting diode and a phototransistor. Most of the time the irradiance emitted by the diode is blocked by the opaqueness of the tape. When a hole moves in the path, the irradiance travels to the photo-transistor and activates it. The infrared emitting diode in the nole detect circuit is not on continuously, but is pulsed at approximately 13 kHz . By pulsing the diode, more output can be obtained with less average current and power dissipation.

The pulsed diode output is detected, shaped and fed into the monostable multivibrator (one-shot). The one-shot is retriggerable and its time out is slightly longer than the time period of 13 kHz . Therefore, the output of the one-shot will remain true as long as it receives an input of at least a nominal 13 kHz . By measuring the time that the oneshot's output remains true, it can be decided whether the detection circuit has seen a scratch, a normal hole, or the tape has run completely off the end. This technique eliminates ambient light problems.
3.2.4.2 The pulse generator consists of U2, R6, R7 and C2. The resistors and capacitor control the frequency and symmetry of the output. The frequency is $13.125+/-1.5 \mathrm{KHz}$. The output of U 2 , Pin 3 has the following waveform.

3.2.4.3 C1, CR1, R1, R2, and $1 / 2$ of 01 make up the diode driver. During the time that the output of U1 is high (off) C1 charges through R2. When the output of Ul goes low, C1 is discharged through R1 and CR1. R1 limits the current through CR1 and R2 isolates this low impedence path from the +5 volts. The peak current through infrared emitting diode (CR1) is approximately 200 mA , and should provide a beam power output (minimum, peak) of 2.5 mililwatts.
3.2.4.4 The detection circuit consists of Q1, Q2, Q3, CR2, U3, R4, R5, R8, R9, R10, and C4. Irradiance striking its base reqion causes current to flow through Q1. Most of this current flows through $Q 3$ and into the base of Q2. Q2 saturates, providing a negative transition which initiates the time out of the one-shot multivibrator, U3. R5 and CR2 provide a de level to the base of $Q 3$ that wlll allow the collector of Q3 to overcome the $V(B E)$ of $Q 2$. R5 also keeps the capacitance of CR2 and 43 cnarged allowing faster circuit response. CR2 and Q3 provide a low impedence load to the photo-transistor Q1, which has a high C(be) thus also increasing response time. R4 sets the threshold of the detector circuit. 01 must provide enougn current to raise the voltage drop across $R 4$ above the $V(B E)$ of $Q 2$ before $Q 2$ will turn on. $R 9$ is the collector load for $Q 2$ and provides current for the inputs of $U 3$ in their high state. R10 provides a high state for the other inputs of U3. R8 and C4 are the timing components for the monostable multivibrator U3. The time out is $110+/-20$ microseconds. R11 provides approximately 5 to 10 ner cent positive feedback giving the detection circuit a Schmitt-trigger characteristic. This provides a more detinite detection of the hole edges.

3.3.1 BASE ASSEMBLY - CTU TRANSPORT ASSEMBLY.
3.3.1.1 The base assembly provides the support structure for the drive.
3.3.1.2 The base assembly is mounted to the terminal using two $5 / 16$ inch well nuts and two number $6-32$ screws. The wall thickness at the mounting surface should be $>/=12$ gauge for metal or other material. The well nuts with associated screws provide convenient captive fasteners. More importantly, they attenuate mechanical vibrations in the 1 kHz region and above. Without this attenuation, sharp impacts to the terminal could cause read or write errors. A third mounting surface, faced with a rubber pad, is used for location and stabilization of the drive.

In the normal mounting attitude the cartridge is held at 15 degrees to the horizontal. Other mounting positions may be possible but care should be taken to avoid having the head surface facing upwards to collect dirt. Also the eject spring may have to be changed for other mounting attitudes. Provision has been made in the tooling die for the base for an alternate 0 degrees mounting attitude; nowever, this has not yet been implemented in an optional product. mounting dimensions and an outline of the mechanism are shown in figure 11. An outline of the cartridge is shown in figure 12.

To prevent loss of intimate tape-head contact due to insufficient wrap and to minimize head and tape wear due to excessive wrap, the base
assembly has reqistration surfaces which control the fore and aft position of the cartridge. These surfaces are accurate to within $+/-0.001$ inch with respect to locating pin holes on the base. These holes in turn determine the position of the head bridge assembly. Side-to-side location of the cartridge, a less critical registration, is accomplished by maintaining minimum clearance between the cartridge and the drive.


Four rollers provide the locating force. Two rollers press against the corner of the notch in the cartridge base at about 45 degrees resulting in an upward force component. The other two rollers press straight up holding the cartridge against the locating olanes in the base. A force of about 4 pounds is required to insert the cartridge. The retention force is over 3 pounds.

Pressing the button releases the latch taking the pressure off the four rollers and allowing the cartridge to pop out to a detent position for easy removal. The cartridge is ejected part way by the motor assembly swinging forward. At this point the ejector rises out of the base and continues the cartridge motion out to the detent position. In this manner, the ejection force does not oppose the latching force when the cartridge is fully inserted. The mechanism resets itself during the ejection and is then ready to accept a cartridge again. The detent action is effected by a pawl which is spring loaded against the cartridge by the same spring that returns the release bution.

### 3.3.2 HEAD BRTDGE ASSEMBLY - CTU TRANSPORT ASSEMBLY.

3.3.2.1 The head bridge assembly provides the critical reference surfaces for nead-to-tape positioning and provides mounting for the cartridge Electronics PCA.
3.3.2.2 The head bridge assembly has three pads which contact three small areas on the reference surface of the cartridge. This defines a reference plane both for the cartridge and the drive. The magnetic head is adjusted for hoth tilt and azimuth with respect to this plane as part of the manufacturing process. The nead itself has a ball socket which engages a spherical "bump" molded into the plastic head bridge. Since the socket is centered on the magnetic gap in the nead, the tilt and
azimuth adjustments are independent of one another. The vertical head position is controlled by maintaining close tolerances on the head and head bridae, and thus no height adjustment is required. The spherical bump is also within $+/-0.001$ inch with respect to the locating pins molded into the head bridge. Inis accurately controls the fore and aft position of the head to maintain the oroper tape-nead wrap andle. Once set, the head adjusting screws are sealed in position and no further head adjustment is required either at initial assembly or during field replacement. Thus any head bridge assembly works interchangeably with any base assembly.
3.3.2.3 The head bridge assembly also includes the Cartridge Electronics PCA (detailed in section 3.2) which performs various functions. Circuitry for sensing the position holes in the tape is included on this board. The infrared LED light source for this function is retained and precisely positioned by a molded-in clamp taking advantage of the strength and dimensional stability of the plastic material used in the head bridge to grip the LED without additional parts or machining. Cartridge insertion and the position of the RECORD tab on the cartridge are sensed by the position of two switches. Fixed contact nads for these switches are on the circuit board while the moveable contacts with their plunger actuators are enclosed within the head bridge giving inexpensive, reliable, enclosed switches.
3.3.2.4 The indicator lamp (previously mentioned) is also located on this PCA and is enclosed by a snield molded of titanium-dioxide filled plastic for maximum reflectivity. This part serves the dual functions of blocking stray light from the lamp while concentrating the light entering the light pipe portion of the release button. Since all interconnections are made on the board, no wiring harness is necessary on the mechanism.
3.3.3 MOTOR/TACHOMETER ASSEMBLY - CTU TRANSPORT ASSEMBLY.
3.3.3.1 The third subassembly of the CTU Transport is the motor/tachometer assembly which consists of a motor with drive capstan, a motor mount and a tachometer to provide velocity feedback to the servo.
3.3.3.2 The motor/tachometer assembly is single axis gimballed about its center of gravity to eliminate acceleration effects on the force developed between the motor capstan and the belt capstan in the cartridge. This force is provided by two extension springs which also serve to retain the assembly in the gimbal and to aid in ejecting the cartridge. The force between capstans is $15+/-1.5$ ounces. The gimbal consists simply of two hemispherical ball and socket joints between the motor/tachometer assembly and the base assembly. The assemblies are held together
by two extension springs which also provide the correct capstan force. The right hand ball and socket set prevents translation while the left set has an elongated socket to prevent rotation about two axes without causing binding due to tolerance accumulations.

As well as retaining the motor/tachometer assembly in its gimbal, the two extension springs load the motor capstan against its mating belt capstan within the cartridge. This spring loading takes up an accumulation of dimensional tolerances within both the cartridge and the drive while holding the force between the capstans within specified limits. The motor capstan is a polyurethane elastomer covered aluminum part 0.338 inches in diameter. The elastomer used has the best combination of high coefficient of friction, resistance to compression set and resistance to wear of a selection of potential materials which were tested. The capstan is set-screwed to the motor shaft and its height can be set without special tools or fixtures. A variable reluctance tachometer is mounted to the motor/tachometer assembly. This consists of a 48-tooth disc staked to the motor capstan, a pickup coil and permanent magnetic flux gate assembly screwed to the motor mount. The disc-to-pickup distance is set at 0.012 inches $+/-0.002$ inches. Motor capstans with disc attached can be field replaced without need for further adjustment.
3.4 FUNCTIONAL DESCRIPTION - TAPE CARTRIDGE. Refer to the tape cartridge diagram (figure 13), hole status format (figure 14), and valid recording area (figure 15) located in the appendix.

The tape cartridge shown in figure 13 provides 120,000 bytes of storage in 256 -byte record, single-track $0.130+/-0.005$ inches, 800 BPI ( 1600 FRPI) $+/-60$ BPI standard format. At 10 ips, this gives a typical burst rate of 1000 bytes per second and 748 bytes per second average throughput. The cartridge consists of a metal base plate and plastic cover.

The tape contains 140 feet (minimum) of $0.150-i n c h 8138$ computer tape suitable for recording purposes. The tab labeled RECORD is used to enable recording on the cartridge. A cartridge door is used to protect the tape during transport and storage. When the cartridge is inserted into the CTU Transport Assembly, the door is opened automatically. The mirror is used with the nole sense scheme. An infrared emitter located in the CTU Transport Assembly base shines through the dase plate onto the mirror. Lignt is then reflected through the front of the cartridge to a photo-sensor in the CTU Transport Head Bridge Assembly. The light is intercepted by the tape normally indicating no nole. If a hole is present the light will be detected by the photo-sensor. The motor capstan drives the belt capstan which then moves the cartridge tape via the belt. The belt consists of an elastomeric belt which drives the tape by transmitting the belt capstan force to both tape reels. The tape cleaner consists of a scraper which is displaced approximately 1.125 inches in front of the head.

| 3.4.1 HOLE STATUS F and the durat Cartridge Ele | HOLE STATUS fORMAT. The positioning of holes in the cartridge tape and the duration of the signal from the hole detect circuitry on the Cartridge Electronics PCA is shown in figure 14. |
| :---: | :---: |
| 3.4.2 INTERCHANGE S region of val as follows in | INTERCHANGE STANDARDS. The code, format of the encoded data, and the region of valid recording area on the 3 M 9585 mini cartridge should be as follows in order to facilitate product interchange. |
| valid $\underset{\text { AREA }}{\text { RECORDING }}$ | DRECORDING The portion of the tape where data may be recorded AREA |
|  | FILES There may be 1 to 344 files per cartridge. |
|  | BYTES $\quad \begin{aligned} & \text { Recording is bit serial, eight bits to a byte, LSB to } \\ & \text { MSB. }\end{aligned}$ |
|  | RECORDS <br> Records are variable in length and may contain from 12 to 267 bytes. There may be 444 to 517 records of of maximum length per cartridge. |
| RECORDURGANIZATION:Preamble |  |
|  | Header (2) bytes to define binary length of record (most <br> significant byte first).  significant byte first). |
|  | Body 1 to 256 data bytes. |
|  | Checksum $\quad 1$ byte binary addition modulo 256. |
|  |  |
| INTEK-RECORD GAPS: |  |
|  | Polarity <br> The IRG shall magnetize so that the beginning of the tape is a north seeking pole. NOTE: There are 0.01712 $+/-0.0003^{\prime \prime}$ of tape travel for each detected edge. |
|  | Le marks <br> Files shall be separated by a unique length gap and record as follows: 1.61" min., 1.81" max. gap followed by a $1.61^{\prime \prime}$ min., $1.81^{\prime \prime}$ max. gap. <br> NOTE: The file mark record header is unique insofar as the most significant byte is always a "1". |
| END Of Valid data mark | ALID Data mark a file mark followed by a gap of 11 +/-0.5" |

3.4.3 MECHANICAL SPECIFICATIONS.

The mechanical characteristics of the cartridge are summarized in the following table:



Figure 1




Figure 4
Read/write PCA Block Diagram



## CARTRIDGE ELECTRONICS PCA




Figure 8



Figure 10



Figure 12


Figure 13
Tape Cartridge Diagram


- BOT = BEGINNING OF TAPE ( 2 CONSECUTVE HOLES) (3PARR BOT HOLES
- LP = LOAD POINT ( 1 HOLE)
- EW = EARLK WARNING (1 HOLE)
- EOT = END OF TAPE ( 1 HOLE) ( 3 EOT HOLES)

USING THE HOLE STATUS FROM THE CTU TRANSPORT ASSEMELY, THE HOLE TIMING ISAS FOLOWS:

| SPEED | $T_{1}$ |  | $T_{2}$ |  | $T_{3}$ |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | MIN | MAX | MIN | MAX | MIN | MAX |
| 9-11 IPS | 2.53 ms | 8.57 ms | 11.23 ms | 25.2 ms | 2.12 sec | 2.7 sec |
| 56-64 IPS | 0.577 ms | 1.49 ms | 1.92 ms | 3.9 ms | 353 ms | 450 ms |

HOLE STATUS FORMAT

Figure 14

a) 0.55 INCHES BEHIND LP MIN.

* EVD = END OF VALID DATA GAP
b) 5.50 INCHES BEHIND EWMAX.

NOTE; THE READ/WRITE HEAD IS DISPLACED FROM THE HOLE DETECTOR BY APPROXIMATELY 1.5 INCHES \&FROM THE TAPE CLEANER BY APPROXIMATELY 1.125 INCHES

Replaceable Parts


Replaceable Parts


Replaceable Parts


Replaceable Parts


Replaceable Parts


Replaceable Parts

| Reference <br> Designation | HP Part <br> Number | Oty |  | Description | Mfr <br> Code | Mfr Part Number |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- |
|  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |

Replaceable Parts


Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 02 640－60032 | 1 | READ／WRIIE ASSEMBLY DATE CODE：E－1535－22 REVISICN DATE：08－06－76 | 28480 | 02640－60032 |
| $\checkmark 1$ | 0180－0106 | 2 | CAPACITOR－FXO 6OUF＋－202 6VUC TA | 56289 | $1500606 \times 0006 \mathrm{B2}$ |
| ${ }_{6}$ | $0160-0166$ $0180-0106$ | 2 |  | 56289 56289 | $292 P 68392$ $1500606 \times 000682$ |
| 63 | $0180-0106$ $0160-0166$ |  | CAPACIITRR－FXD 60UF－202 6 VOC TA CAPACITOR－FXD $0068 \mathrm{HF}+-10 \pm 200 \mathrm{hVDC} \mathrm{POLYE}$ | 56289 56289 | $1500606 \times 000682$ $292 P 68392$ |
| 65 | 0180－0309 | 5 | CAPACITOR－FXD 4．7UF＋－20\％LOVOC TA | 56289 | $1500475 \times 001042$ |
| 60 | 0140－0161 | 1 | CAPACITOR－FXD 3932PF＋－12 300WVDC MICA | 72136 | OM2 OF 3932 RF 0300 WVICR |
| C\％ $C 8$ | $0180-1746$ $0180-1746$ | 2 |  | 56289 56289 | $1500156 \times 902082$ $1500156 \times 902082$ |
| cod | 0180－1746 |  | CAPACITOR－FXD 15UF－10\％20VDC TA | 56289 28480 | 1500156 01502082 |
| 411 | $0150-0121$ $0180-0309$ | 7 | CAPACITOR－FXD－1UF $+80-208$ 50WVDC CER CAPACITOR－FXD $4.7 U F+-20 \%$ LOVOC IA | 28480 56289 | 0150－0121 $150045 \times 001022$ |
| 414 | 0180－0309 |  | CAPACITOR－FXD 4．7UF＋－20\％1OVOC TA | 56289 | $1500475 \times 001042$ |
| Cb | $0180-0309$ |  | CAPACITOR－FXO 4．7UF＋－20\％LOVDC TA | 56289 | $1500475 \times 001042$ |
| 610 | $0160-2260$ | 2 | CAPACITOR－FXD 13PF＋－5\％500WVUC CER | 28480 | 0160－2260 |
| 6.17 | 0140－0190 | 4 | CAPACITOR－FXD 39PF＋－5\％300WVDC MICA | 72136 | DM15E390」03 00WV1CR |
| 610 | 0140－0190 |  | CAPACIIUR－FXD 39PF＋－5\％300wVDC HICA | 72136 | DH15E390J0300WV1CR |
| 618 | 01t0－2260 |  | CAPACITOR－FXO 13PF＋－5\％500wVOC CER | 28480 | 0160－2260 |
| C20 | $0160-0159$ | 3 | CAPACITOR－FXD 6800PF＋－10\％200WVDC POLYE | 56289 | 292P68292 |
| $4<1$ | 0140－0200 | 2 | CAPACITOR－FXO 390PF t－5\％300WVCC MICA | 72136 | OH15F391J0300MVICR |
| L2L | 0140－0200 |  | CAPACITOR－FXD 390PF \％－5\％300WVDC MICA | 72136 | DM15F391J0300WVICR |
| C24 | 0160－0153 | 4 | CAPACITOR－FXO 1000PF＋－108 200nVDC POLYE | 56289 | 292P10292 |
| C23 | $0160-0167$ | 1 | CAPACITOR－FXC ．082UF＋－10\％200hVOC POLYE | 56289 | 292P82392 |
| $4<0$ | $0160-0159$ |  | CAPACITOR－FXO 6800PF＋－10\％ 200 VVOC POLYE | 56289 | $292 P 68292$ |
| C2I | 0160－3238 | 1 | CAPACITOR－FXD－15UF t－5\％200WVOC POLYE | 56289 | 292P15452 |
| Lid | 0150－0121 |  | CAPAC ITOR－FXD ． $1 \mathrm{LUF}+80-203$ 50WVOC CER | 28480 | 0150－0121 |
| Lく9 | 0150－0121 |  | CAPACITOR－FXD ．1UF＋80－203 50WVDC CER | 28480 | 0150－0121 |
| L 50 | 0150－0121 |  | CAPACITOR－FXD－1UF＋80－20\％SOWVOC CER | 28480 | 0150－0121 |
| C31 | 0150－6121 |  | CAPACIIOR－FXD－1UF＋80－208 50nVOC CER | 28480 | 0150－0121 |
| L3 | $0160-0153$ |  | CAPACITOR－FXD TOOOPF＋－10\％20UnVDC POLYE | 56289 | 292P10292 |
| L33 | $0160-0153$ |  | CAPACITOR－FXD 1000PF＋－10\％200WVDC POLYE | 56289 <br> 28480 | 292P10292 |
| 634 | $0160-0970$ | 1 | CAPACITOR－FXD－ 47 UF ＋－102 8OWVOC POLYE | 28480 | 0160－0970 |
| 435 | $01 \in U 0163$ | 1 |  | 56289 28480 | 292P33392 |
| 630 637 | $0160-2263$ $0140-0190$ | 2 | CAPACIITR－FXD 18PF＋5\％500WVOC CER CAPACITOR－FXD 39PF＋－5\＄300WVOC MICA | 28480 72136 | 0160－2263 ${ }^{\text {DM15E390J03 00WV1CR }}$ |
| 630 | 0140－0190 |  | CAPACITOR－FXD 39PF＋－5\％300WVDC MICA | 72136 | DH15E390J03DOHVICR |
| 63y | 0160－2263 |  | CAPACITOR－FXD 18PF＋－5\％500WVOC CER | 28480 | 0160－22 63 |
| 640 | $0160-0153$ |  | CAPACITOR－FXO 1000PF＋－10\％200WVOC POLYE | 56289 | 292P10292 |
| 441 | $0150-0121$ $0180-0291$ |  | CAPACITOR－FXD－1UF $+80-20 \% 50 \mathrm{wVOC}$ CER CAPACITOR－FXD LUF -10835 VOC TA | 28480 56289 | 0150－0121 $1500105 \times 903542$ |
| C44 | $0180-0291$ $0180-0291$ | 3 | CAPACIITRR－FXD LUFt－10\％35VOC TA CAPACITOR－FXD LUF－108 35 VOC TA | 56289 56289 | $1500105 \times 9035 A 2$ $1500105 \times 9035 A 2$ |
| 644 | 0150－0121 |  | CAPACITOR－FXD ．LUF＋80－20\％50WVDC CER | 28480 | 0150－0121 |
| $4{ }^{4} 5$ | 0160－0291 |  | CAPACITOR－FXD 1UF＋10\％35VOC TA | 56289 | $1500105 \times 903542$ |
| 446 | 0180－0309 |  | CAPACITOR－FXD 4．7UF＋－202 10VOC TA | 56289 | 1500475 0001042 |
| 647 443 | $0160-2055$ $0160-2055$ | 3 | CAPACITOR－FXD－ $01 \mathrm{UF}+80-20 \mathrm{E}$ 100WVOC CER | 28480 28480 | 0160－2055 |
| 443 | 0160－2055 |  | CAPACITOR－FXD－01UF＋80－20\％ 100 WVOC CER CAPACITOR－FXD $6800 \mathrm{PF}+$－10z 200 WVOC POLYE | 28480 | 0160－2055 |
| L49 | 0160－0159 |  | CAPACITOR－FXD 6800PF＋ 103200 WVDC POLYE | 56289 | 292P68292 |
| bo | 0160－2055 |  | CAPACITOR－FXD ．OLUF $+80-202$ 100WVDC CER | 28480 | 0160－2055 |
| CK2 | 19C2－0049 | 5 | DIODE－ZNR 6．19V 5\％00－7 PO＝．4W TC＝＋．022\％ | 28480 | 1902－0049 |
| CKS | 19C2－0049 |  |  | 28480 | 1902－0049 |
| Cr4 | 1962－0049 |  | DIGDE－2NR 6．19V 5\％DO－7 PD $=4 \mathrm{4W}$ TC $=+.022 \pm$ | 28480 | 1902－0049 |
| （k） | 1912－0049 |  | DIODE－2NR 6．19V 58 DO－7 PO＝－4W TC＝t．022\％ | 28480 | 1902－0049 |
| cko | 19C2－0049 |  | DLODE－2NR 6．19V 5\％DO－7 PO＝4W TC $=+$ ． 0222 | 28480 | 1902－0049 |
| LKJ | 19C1－0304 | 1 | DIODE－FW BRDG 200 V 1A | 04713 | SDA $10185-4$ |
| Cky | 19C2－0025 | 1 | DIODE－2NR LOV 5z DO－7 PD＝ $4 \mathrm{4W}$ TC＝$=+06 \%$ | 28480 | 1902－0025 |
| GKLU | 1961－0040 | 1 | DIODE－SWITCHING 30V 50MA 2NS DC－35 DIODE－2NR 7．5V 58 DO－7 PD 0.4 W TC $=+.05 \%$ | 28480 28480 | 1901－0040 |
| CK11 | $19 \mathrm{C2}-0064$ $15 \mathrm{Cl}-0460$ | 1 |  | 28480 28480 | 1902－0064 |
| CR13 | 1902－3059 | 1 | DIODE－2NR 3．83V 57 DO－7 PD＝．4W TC＝－．051\％ | 15818 | CD 35586 |
| E 1 | 03＜0－0124 | 3 | IERMINAL－STUD SGL－PIN PRESS－MTG | 28480 | 0360－0124 |
| $t 2$ | $0360-0124$ $0360-0124$ |  | TERMINAL－STUD SGL－PIN PRESS－MTG TERMINAL－STUD SGL－PIN PRESS－MTG | 28480 28480 | 0360－0124 |
| ts | 0360－6124 |  | IERMINAL－STUD SGL－PIN PRESS－MTG | 28480 | 0360－0124 |
| 14 | 120000474 | 2 | SOCKET－IC 14－CONT DIP－SLDE | 28480 | 1200－0474 |
| 」り | $12 \mathrm{CO-0} 474$ |  | SOCKET－IC 14－CONT DIP－SLUR | 28480 | 1200－0474 |
| Jo | 1251－3873 | 1 | CONNECTOR 4－PIN M POST TYPE | 27264 | 09－88－2041 |
| 41 | $1854-0215$ $1854-0215$ | 7 | TRANSISTOR NPN SI PD＝350MW FT $=300 \mathrm{MHZ}$ <br> TRANSISTGR NPN SI PD＝350Mw FT $=300 \mathrm{MHZ}$ | 04713 04713 | $\begin{aligned} & \text { SPS } 3611 \\ & \text { SPS } 3611 \end{aligned}$ |
| 4 | 1854－0215 |  | TRANS ISTOR NPN SI PD $=350 \mathrm{MW} \quad F T=300 \mathrm{MHL}$ | 04713 | SPS 3611 |
| 4 | 1853－0036 | 3 | TRANSISTOR PNP SI PD＝310NW FT $=250 \mathrm{MHZ}$ | 28480 | 1853－0036 |
| － | 1855－0052 | 4 | TRANSISTOR MCSFET P－CHAN D－MUDE IO－92 SI | 07263 | 2N4360 |

Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | REAP／WRITE ASSEMBLY Cont ${ }^{\text {do }}$ O． |  |  |
| ${ }^{46}$ |  | 2 |  |  | ¢ |
| ${ }_{9}^{8}$ |  |  |  | 04713 07263 0.263 |  |
|  |  |  |  |  |  |
| （ 0112 |  |  |  | 0477 04713 0.713 0.15 |  |
| S 814 |  |  |  |  | Sps 3 Sil |
|  | 13 |  | TRANSISTOR NEN SI PDe350nm rie 300 nhz |  |  |
| ${ }^{818}$ | － 18.3 － 0036 |  |  | 28480 | ${ }_{\text {che }}^{\text {SPS3－0036 }}$ |
| ${ }^{817}$ | － 18.4002025 |  |  | － $\begin{aligned} & 04713 \\ & 04713\end{aligned}$ | SPS SPS 3611 |
| $R 2$ $R_{2}$ 2. |  | ： |  | 24546 <br> 24546 | C4－1／8－70－6812－F |
| ${ }_{8}{ }_{8}{ }^{2}$ | ${ }^{0}$ |  |  | － | C4t18－10－6812－F |
| R ${ }_{\text {R4 }}$ | － $07757-04622$ |  |  | 24546 24546 |  |
| ${ }_{k}{ }^{6}$ | －9757－0420 | $4_{4}^{4}$ |  | 24546 24546 |  |
|  |  |  |  | － 245454 |  |
| ${ }_{\text {kid }}^{\text {R9 }}$ |  |  |  | 24546 <br> 24546 |  |
| R21 R | $0777-0461$ $0.58-3260$ | 2 |  | ${ }_{\text {24，}}^{24546}$ | C64－1／8－T0－6812－F |
|  | － $075750-0461$ |  |  | ${ }^{244546}$ | ${ }_{\text {Com }}$ |
| 员14． |  |  |  | 21637 24546 |  |
| ${ }_{\text {R } 214}$ | －0767－0459 | 6 |  | 24546 | C64－1／8－10－5622－F |
| R18 | ${ }^{075750.059}$ |  |  | 24546 <br> 24546 <br> 2 |  |
| R20 |  | 1 | RESIS | 24546 24546 |  |
| R21 | －0757－0459 |  |  | 24546 | C4－1／0－To－5622－F |
|  | － |  | Ressisfor | － |  |
|  | －0775－0447 | 1 |  | 24546 24546 |  |
|  | －0757－0462 |  |  | 224546 | C4－1／8－T0－7502－F |
| ${ }_{\text {k }}$ | ${ }_{0} 0658$－3453 | 2 |  | ${ }_{\text {24546 }}^{24546}$ |  |
| ¢ | － $\begin{array}{r}\text { O659－3158 } \\ 0757-0346\end{array}$ | 2 |  | 24546 <br> 24546 |  |
| R331 | －081－1552 | 4 |  | 25042 |  |
| ， | － | 2 |  | － | C4－1／8－501621－F |
| R，35 | －0757－062 |  |  | 24546 <br> 24546 |  |
| R336 | 0757 97－043 075770002 | $\stackrel{4}{4}$ |  | 224546 |  |
|  |  | 2 |  |  |  |
| 盛420 |  | 3 |  | 24546 <br> 2454 | ${ }_{6}$ |
|  | － 0 0577－0420 |  |  | 244464 24546 |  |
| ${ }_{\substack{\text { R } \\ R+4}}$ | O6S8－3158 $0757-0346$ |  |  | 24546 24546 2 |  |
| Ret | － |  | Resis | 244546 24546 |  |
| R．ts | 0663－8245 | 1 |  |  |  |
| ${ }_{\substack{\text { k } \\ \text { k5 } \\ \text { St }}}$ | － 0658 O－3438 |  |  |  |  |
| ¢ | $\begin{aligned} & 0658-3453 \\ & 0757-0438 \end{aligned}$ |  |  | 24546 24546 2454 |  |
| R，55 | ${ }^{21} 21003207$ | 1 |  |  | 72－145－0 |
| cis | 年0757－040 |  |  | 24546 <br> 24546 | come |
| R． |  | 1 |  |  |  |
| RR88 | 0757－0420 |  |  | 22454 |  |
|  |  |  |  | － |  |
|  |  |  | Resisior | 24546 $2+546$ 254 | coile |
| ${ }_{6} 65$ | 0757－0420 |  | RESISTIOR 750 18 ．1254 F T $C=0+100$ | 24546 | C4－1／8－50－751－F |
| ${ }_{\substack{\text { K102 } \\ \mathrm{R} 102}}$ | $1810-0125$ $1810-0125$ | 2 |  |  |  |
| ${ }^{6103}$ | ${ }^{181000251}$ | 2 | NELWRK－RES | 28430 | ${ }^{180}$ |
| ${ }_{\substack{\text { R104 } \\ \text { R．40 }}}^{\text {R20 }}$ | （ $\begin{array}{r}18180-0151 \\ 1880-0037\end{array}$ | 2 |  | 28480 11236 1123 |  |

Replaceable Parts

| Reference Designation | HP Part Number | Qty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
| K107 | 1810-0037 |  | READ/WRITE ASSEMBLY CONT'D. <br> NETMORK-RES 16-PIN-OIP .1-PIN-SPCG | 11236 | 760 SERIES/ 16 PIN |
| $u_{1}$ | 1826-0138 |  | IC LM 339 CEMPARATOR | 27014 |  |
| 42 43 43 | 1820-1260 | 1 | IC-DIGITAL SNT4221N TTL DUAL | 01295 | SN74221N |
| 43 | 1820-0491 | 1 | IC-DIGIJAL SN74145N TTL 4 BCD-TO-DEC | 01295 | SN74145N |
| 04 4 4 | $1826-0200$ $1826-0200$ | 2 | IC MC IC MC 1420 1420 OPP AMP | 04713 04713 | MC14206 MC14206 |
| Uo | 1826-0139 | 4 | IC MC 1458 OP AMP | 04713 | MC1458P1 |
| 47 | 1826-0139 |  | IC MC 1458 OP AMP | 04713 | MC1458P1 |
| Us | 1826-0139 |  | IC MC 1458 OP AMP | 04713 | MC1458P 1 |
| 49 | $18<6-0139$ $1820-0577$ |  | IC MC 1458 CP AMP | 04713 | MC1458P 1 |
| U10 | 1820-0577 | 2 | IC-DIGITAL SN7416N ITL HEX 1 | 01295 | SN7416N |
| 411 412 | $1820-0514$ $1820-1208$ | 1 | IC-DIGITAL SN7426N TIL QUAD 2 NAND IC-DIGITAL SN74LS32N TIL LS QUAD 2 OR | 01295 | SN7426N SN74LS32N |
| U13 | $1820-1416$ | 1 | IC-DIGITAL SN74LSI4N TIL LS HEX 1 INV | 01295 | SN74LS1 ${ }^{\text {SN }}$ |
| U14 | 1820-1202 | 1 | IC-DIGITAL SN74LSION TTL LS TPL 3 NAND | 01295 | SNTHLSLIEN |
| 015 | 1820-1425 | 1 | IC-DIGITAL SM74LSI32N TIL LS QUAD 2 Nand | 01295 | SN74LS1 32N |
| $\begin{aligned} & U_{10} \\ & v_{117} \end{aligned}$ | $1820-0981$ 18200577 102001201 | 1 | IC-DIGITAL CO4016AY CMOS DUAD BILATL | 02735 01295 01295 | CD4016AY SNT 4160 STH |
|  |  |  | miscellaneous |  |  |
|  | $\begin{aligned} & 0340-0585 \\ & 12 C 0-0081 \\ & 2190-0004 \\ & 22 C 0-0143 \\ & 2260-0002 \end{aligned}$ | 1 4 4 4 4 | insulator mica <br> INSULATOR-BSHG-FLG NYLON <br> WASHER-LK INTL T NO.-4 . 115 -IN-ID <br> SCREN-MACH 4-40 .375-IN-LG PAN-HD-POZI <br> NUT-HEX-DBL-CHAM 4-4D-THD .062-THK | 28480 28480 06791 28480 28480 | $\begin{aligned} & 0340-0585 \\ & 1200-0087 \\ & 418-8 C \text { EVERLOCK MASHER } \\ & 2200-0143 \\ & 2260-0005 \end{aligned}$ |
|  | $\begin{aligned} & 6040-0<39 \\ & 02640-20001 \end{aligned}$ | 1 | greasesillicane ccmpound HEAT SINK | $\begin{aligned} & 05820 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 120-56 \mathrm{n} \\ & 02640-20001 \end{aligned}$ |

Replaceable Parts


Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 02640-60034 | 1 | CTU ELECTRONICS ASSEMBLY DATE CODE: B-1632-22 REVISION DATE: 08-04-76 | 28480 | 02640-60034 |
| 4 | $0180-1701$ | 1 | CAPAC ITOR-FXO 6. BUF+-209 GVOC TA | 56289 | $1500685 \times 0006$ A2 |
| 62 | 0160-0153 | 1 | CAPACITOR-FXO 1000PF +-10\% 200WVOC POLYE | 56289 | $292 P 10292$ $1500396 \times 901082$ |
| し4 | $0160-0194$ | 1 | CAPACITOR-FXO . 015 UF +-10\% 200wVOC POLYE | 56289 | 292P15392 |
| Luc | 19C1-0040 | 1 | DIOOE-SWSTCHING 30V 50MA 2NS DC-35 | 28480 | 1901-0040 |
| DSA | $\begin{aligned} & 2140-0450 \\ & 4040-1017 \end{aligned}$ | 1 | LAMP-IAC AND 7362 5VDC 115 MA T-1-3/4-BULB SHIELD, LIGHT | $\begin{aligned} & 71744 \\ & 28480 \end{aligned}$ | $\mathrm{CM7}_{4040-1017}^{\text {CMS }}$ |
| J1 | 12¢1-3192 | 1 | CONNECTOR 3-PIN M POSI TYPE | 27264 | 09-60-1031(2403-03A) |
| - | $1854-0071$ $1853-0020$ | 1 | IRANSISTCK NPN SI PD=300MH FT $=200 \mathrm{MHZ}$ TRANSISTOR PAP SI PD=300MH FT=150MHZ | $\begin{aligned} & 28480 \\ & 28480 \end{aligned}$ | $\begin{aligned} & 1854-0071 \\ & 1853-0020 \end{aligned}$ |
| K1 $k$ $k$ | 0683-0475 | 1 |  | 01121 | C84765 C85605 |
| kS | 06E3-1015 |  | RESISTOR 10058.25 W FC TC $=-400 /+500$ | 01121 | C81015 |
| $\kappa_{4}$ | 0083-1525 | 1 | RESISTOR 1.5K 5\% .25W FC TC $=-400 /+700$ | 01121 | C81525 |
| kS | 0683-1035 | 3 | RESISTOR 1OK 5\% . 25W FC TC=-400/+700 | 01121 | CB 1035 |
| No | $0658-3159$ $0757-0459$ | $\frac{1}{1}$ |  | 24546 24546 | C4-1/8- ${ }^{\text {c }} 0-2612-F$ $C 4-1 / 8-50-5622-F$ |
| $\ldots$ | $06588-3158$ | 1 | RESISTOR 23.7K 1\% .125W F TC $=0+-100$ | 24546 | C4-1/8-50-2372-F |
| $\ldots$ | 0683-1035 |  | RESISTOR 10K 58.25 HFC IC $=-400 /+700$ | 01121 | C81035 |
| kiv | 0683-1035 |  | RESISTOR 10K 58.25 W FC $\mathrm{TC}=-400 /+700$ | 01121 | C81035 |
| K11 K 12 | $0683-6835$ $0663-1505$ | 1 |  | 01121 | $\begin{aligned} & \text { C86835 } \\ & \text { CB1505 } \end{aligned}$ |
| 41 42 | $1820-0535$ $1826-0373$ | 1 | IC-DIGITAL SN75451BP TTL DUAL 2 AND IC LINEAR | 01295 | SN754518P |
| us | $\begin{aligned} & 18<000207 \\ & 1251-4099 \end{aligned}$ | 1 | IC-DIGITAL 9601PC TIL MONOSTBL CONN - SC CONN - SC | 07263 | 9601PC |

Replaceable Parts


Replaceable Parts

| Reference Designation | HP Part Number | Oty | Description | Mfr Code | Mfr Part Number |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | 02640-60055 <br> 0050-1831 <br> U4C3-033 <br> 0470-0443 <br> $0624-0296$ <br> 1251-2510 <br> 1251-2599 <br> $1460-1412$ <br> 3140-0544 <br> $02640-60057$ $02640-60076$ <br> 02640-60074 |  | MOTOR/TACHOMETER ASSEMBLY <br> REVISION DATE: 03-13-76 <br> CASTING <br> BUMPER FOCT, RUBEER $0.312^{*}$, <br> AUHESIVE BCNDING: W224-1 <br> $\begin{array}{llll}\text { SCREW-MACH M2 } & \times 0.40 \text { 6-MM-LG } 90 \text { DEG } \\ \text { SCREW-TPG } 2-56 & .375-\text { IN-LG }\end{array}$ <br> CONNECTOR 2-RIN M UTILITY <br> CONTACT-CGNN MALE CRP .093-IN-CONT-SL CABLE TIE .062-.625-DIA 091-WD NYL WASHER-SRR BLVL. NO.-2.093-IN-ID <br> MOTOR-OC PERM MAG GV 5000-RPM <br> ASSY: TACH CCIL <br> ASSY, MAGNET |  | 02640-60055 <br> 0050-1831 <br> 459 <br> 0515-0029 <br> 0624-0300 <br> 03-09-2022 <br> 02-09-2116 TYB-23M-8 <br> $1460-1412$ <br> B0187-007 <br> 3140-0544 02640-60057 <br> 02640-60074 |

Replaceable Parts


Replaceable Parts


Replaceable Parts


