HP 13220

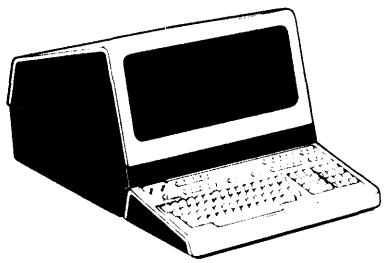
Processor Module

Manual Part No. 13220-91097

REVISED

APR-03-81

DATA TERMINAL
TECHNICAL INFORMATION



HEWLETT hp PACKARD

Printed in U.S.A.

Table of Contents

HP 13220

Processor Module

Manual Part No. 13220-91097

REVISED

APR-03-81

NOTICE

The information contained in this document is subject to change without notice.

HEWLETT-PACKARD MAKES NO WARRANTY OF ANY KIND WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Hewlett-Packard shall not be liable for errors contained herein or for incidental or consequential damages in connection with the furnishing, performance, or use of this material.

NOTE: This document is part of the 262XX DATA TERMINAL product series Technical Information Package (HP 13220).

Table of Contents

1.0 INTRODUCTION

This document describes the operation of the 02620-60097 processor module. This module is used in the HP 2624A and the HP 2624B data terminals. Section 2 lists operating parameters and connector information. A functional description is given in section 3, and section 4 contains a glossary of the signal names used in the module. A parts list, timing diagram, schematic diagrams, and components location diagram follow section 4.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Processor Module is contained in tables 1.0 through 4.0

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.1 Inches	Weight (Pounds)
02620-60097	Processor PCA	14.3 x 10.9 x 0.5	1.4

Table 2.0 Reliability and Environmental Information

Environmental:	HP Class B
Restrictions:	Type tested at product level
Failure Rate:	6.00085 (percent per 1000 hours)

Table 3.0 Power Supply Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+16 Volt Supply	+12 Volt Supply	+5 Volt Supply	-12 Volt Supply
@ 0 mA	@ 500 mA	@ 3 A	@ 70 mA
NOT APPLICABLE			

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Table 4.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
J1		** PRINTER **
Pin -1	$\overline{PSEL}$	Negative True, Printer Select
-2	$\overline{PWR\ FAIL}$	Negative True, Power Failing
-3	$\overline{PWR}$	Negative True, Printer Write
-4	PCNTL1	Printer Control 1
-5	$\overline{FLAG}$	Negative True, Acknowledge Flag
-6	$\overline{DATA\ 0}$	LSB - Negative True, Data
-7	$\overline{DATA\ 1}$	"
-8	$\overline{DATA\ 2}$	"
-9	$\overline{DATA\ 3}$	"
-10	$\overline{DATA\ 4}$	"
-11	$\overline{DATA\ 5}$	"
-12	$\overline{DATA\ 6}$	"
-13	$\overline{DATA\ 7}$	MSB - Negative True, Data
-14	GND	Printer ID
-15	$\overline{PRD}$	Negative True, Printer Read
-16	$\overline{INT}$	Negative True, Printer Interrupt
-17	PCNTL0	Printer Control 0
-18	+5V	Vcc Power
-19	+5V	"
-20	+5V	"
-21	+5V	"
-22	GND	Power Return
-23	GND	"
-24	GND	"
-25	GND	"
-26	GND	"

Table 4.0 Connector Information (Cont'd)

Connector and Pin No.	Signal Name	Signal Description
J2		** POWER SUPPLY **
Pin -1	+5V	+5V Power
-2		N/C
-3	+5V	+5V Power
-4	+12V	+12V Power
-5	GND	Return for Power
-6	GND	Return for Power
-7	PWR FAIL	Negative True, Power Failing
-8	-12V	-12V Power
-9	BATTERY	Positive Battery Terminal
-10	BATRET	Negative Battery Terminal
J3		** SWEEP **
Pin -1	HLFBRT	Negative true, Half Bright Video
-2		N/C
-3	RETURN	Return for half bright
-4	FULLBRT	Negative true, Full Bright Video
-5	RETURN	Return for Video
-6	RETURN	Return for Drive signals
-7	VERDR	Negative True, Vertical Drive
-8	HORDR	Horizontal Drive
J4		** KEYBOARD **
Pin -1	KEYA0	Key Data (LSB)
-2	KEYA1	Key Data
-3	KEYA2	Key Data
-4	KEYA3	Key Data
-5	KEYA4	Key Data
-6		N/C
-7	KEYA5	Key Data
-8	KEYA6	Key Data (MSB)
-9	KEYACT	Key Active (Status of key selected)
-10	GND	Power Return
-11	BELL	Bell Line
-12	+5v	+5v Power
-13 to -16		N/C

Table 4.0 Connector Information (Cont'd)

Connector and pin No.	Signal Name	Signal Description
J5		** DATA COMM **
Pin -1		N/C
-2	SD (BA)	Send Data
-3	RD (BB)	Receive Data
-4	RS (CA)	Request to Send
-5	CS (CB)	Clear to Send
-6	DM (CC)	Data Mode
-7	SG	Signal Ground
-8	RR (CF)	Receiver Ready
-9		N/C
-10		N/C
-11		N/C
-12	OCR2 (SCF)	
-13		N/C
-14		N/C
-15		N/C
-16		N/C
-17		N/C
-18		N/C
-19	OCD2 (SCA)	
-20	TR (CD)	Terminal Ready
-21		N/C
-22	OCR1 (CE)	Optional Control Receiver 1
-23	OCD1 (CH)	Optional Control Driver 1
-24		N/C
-25		N/C

Table 4.0 Connector Information (Cont'd)

Connector and pin No.	Signal Name	Signal Description
J6		** DATA COMM **
Pin -1	OCD4	Optional Control Driver 4
-2		N/C
-3		N/C
-4		N/C
-5		N/C
-6		N/C
-7	TT (DA)	Terminal Timing
-8		N/C
-9	OCR1	Optional Control Receiver 1
-10	+12V	
-11	-12V	
-12	SD (BA)	Send Data
-13	RS (CA)	Request to Send
-14	TR (CD)	Terminal Ready
-15	OCD2	Optional Control Driver 2
-16 to -22		N/C
-23	GND	Signal Ground
-24		N/C
-25		N/C
-26	OCD3	Optional Control Driver 3
-27 to -34		N/C
-35	+5V	
-36	+5V	
-37	GND	Logic Ground
-38	GND	Logic Ground
-39	GND	Logic Ground
-40	OCD1	Optional Control Driver 1
-41	ST (DB)	Send Timing
-42	RD (BB)	Receive Data
-43	RT (DD)	Receive Timing
-44	CS (CB)	Clear to Send
-45	DM (CC)	Data Mode
-46	RR (CF)	Receiver Ready
-47	OCR2	Optional Control Receiver 2
-48	SG (AB)	Signal Ground
-49	TTL X8 CLK	TTL Level Times 8 Clock
-50	TTL X16 CLK	TTL Level Times 16 Clock

3.0 PROCESSOR MODULE FUNCTIONAL DESCRIPTION

The 02620-60097 (02620-60053) Processor Module is logically divided into four sections: the microprocessor controller, the datacomm subsystem, the keyboard/printer subsystem, and the display subsystem. Each subsystem will be described in detail in the following sections of this document. Throughout this document, refer to the block diagram, the schematic, the timing diagram, the component location diagram, and the parts list.

3.1 Microprocessor Controller

3.1.1 The main processor for the terminal is the Z80A-CPU (U714). It processes data that is obtained from and sent to the other subsystems. A memory map is shown below.

Address Range	Bank 1	Bank 2
0000-1FFF	ROM0 (U912)	ROMA (U911)
2000-3FFF	ROM1 (U914)	ROMB (U916)
4000-5FFF	ROM2 (U913)	ROMC (U917)
6000-7FFF	ROM3 (U915)	
6000-60FF		CMOS RAM (U713)
	Independent of Bank	
8000-BFFF	RAM (U41-48)	
C000-FFFF	RAM (U51-58)	

There are two banks of memory in the lower 32K of the address range. Selection of banks is made through the selftest register, U515. (See I/O address map below). The main microprocessor code for the terminal is stored in five 8K byte ROMs (ROM0-3 in bank 1 and ROMA in bank 2). However, to provide for expansion, there is space for two more ROMs in bank 2 (ROMB-C). The ROMs are addressed by lines BA12-BA0. Address lines BA13, BA14 and signal BANK2 are the inputs to a 3 to 8 decoder (U813) that selects which ROM will be enabled. The 10K pull-up resistor on ROM data line D4 is used in checking for the presence of the ROMs.

3.1.2 The 256 by 4 CMOS RAM is used to store the terminal and datacomm port configurations. Battery power for the CMOS RAM is provided when power fails or when the terminal is powered down. A 4.2V mercury or 3.2V lithium battery supplies the back-up power. The terminal's +5V supply and the battery are diode isolated to ensure battery usage only when the terminal power is off. The emitter follower circuit is used to control the chip enable line of the CMOS RAM. The $\overline{PDWN}$ line is held below 0.2V until $\overline{PFAIL}$ becomes false. U215 is driven by $\overline{PFAIL}$; this resets the CPU and other logic on power-up. $\overline{PDWN}$ is not used to drive the inverter because input circuits of TTL gates may pull $\overline{PDWN}$ above 0.2V, which violates the CMOS RAM chip enable specifications for data retention.

3.1.3 Eight 16K by 1 dynamic RAMs comprise display memory and program work-space. Another 16k bytes of RAM are available as an option. Either the processor or display subsystem may access display RAM. Control of the address bus for display RAM is determined by MUXB and $\overline{MUXB}$. On scan lines 0, 4, and 8, the display subsystem has control of the address bus (See section on the display subsystem). Shift registers U91 and U81 and the associated logic create the RAS and CAS signals used by the RAM. MUXA (multiplex address) controls the RAM address multiplexers. $\overline{VBUSY}$ and $\overline{ZBUSY}$ ensure that the address multiplexers do not switch between video and processor access during a RAM access cycle. This is done by controlling the clear and preset inputs of MUXB's latch (U94). The direction of data through U59, a tristate octal bus transceiver, is controlled by Z2RAM (Z80A-CPU to RAM). U59 is tristated when the display subsystem is accessing RAM.

WE, write enable, is a combination of CAS, Z2RAM, and ZBUSY.

3.1.3.1 The $\overline{RAS}$, MUXA, and $\overline{CAS}$ signals needed to address RAM are generated at one dot time separation by U81. The input to U81 consists of the logical OR (U72) of LBC, for video display memory accesses (DMA), and ZBUSY, for Z80A-CPU accesses. LBC, which runs at a character rate, initiates and terminates successive video accesses, except for the first character of a line. Since $\overline{RAS}$, MUXA, and $\overline{CAS}$ follow the falling edge of LBC, an additional falling edge is needed for the first character of a line. U91 (clocked on the negative edge of LCG) generates this first edge by delaying LRC by 3 character times. LRC end terminates $\overline{RAS}$ and $\overline{CAS}$ for the last character of a line. These edges are combined with LBC to obtain the input to U81 (See figure 5).

Figure 6 shows how $\overline{RAS}$, MUXA, and $\overline{CAS}$ are generated by U81. $\overline{RAS}$ is taken from Qc, MUXA is taken from Qd, and $\overline{CAS}$ is taken from Q of U64. Both U81 and U64 are clocked by DRC. Thus $\overline{RAS}$, MUXA, and $\overline{CAS}$ are time delayed images of LBC. $\overline{RAS}$ is delayed by 3 dot times, MUXA by 4 dot times, and $\overline{CAS}$ by 5 dot times. DMALATCH (output Qa of U81) is inverted through U17 to clock video data in U49 during DMA. DMALATCH is LBC delayed by one dot time. Thus the falling edge of LBC clocks U49.

Z80A-CPU accesses are initiated through $\overline{ZBUSY}$, which is a combination of $\overline{MREQ}$, BA15, and MUX. ($\overline{ZUBUSY}$ indicates the Z80A-CPU has access to RAM). Figure 7 shows how U81 generates $\overline{RAS}$, MUXA, and $\overline{CAS}$. Note that $\overline{CAS}$ is raised before $\overline{RAS}$ by U81 pulling the preset of U64.

3.1.4 The Z80A-CPU processor operates with a 3.6816 MHz clock (PHI) resulting in a 271.6 ns cycle time. The clock frequency is derived from DFREQ, a 25.7715 MHz signal from the display subsystem. DFREQ is divided by 7 using a 4 bit binary counter (U513). The resulting waveform is shaped by R31 and C84 to obtain a 50% duty cycle. In order to ensure a logic level of Vcc-0.6 volts and a sufficiently fast rise time, the active pull-up provided by Q5 is used.

The $\overline{BUSREQ}$, $\overline{BUSACK}$, and $\overline{HALT}$ signals are not used, so $\overline{BUSACK}$ and $\overline{HALT}$ are not connected and $\overline{BUSREQ}$ is pulled high through R47.

3.1.4.1 Wait states for the Z80A-CPU are generated by U213, U214, and U317 on M1 cycles (opcode fetches) and CMOS accesses because the ROM and CMOS RAM access times are slower than the normal Z80A-CPU cycles. The WAIT signal also synchronizes the operation of the Z80A-CPU with that of the CRT controller DMA by suspending the Z80A-CPU during DMAs. (See section 3.4.3.3)

3.1.4.2 Because the Z80A-CPU has limited drive capabilities, the address and data busses are buffered using tristate gates (U711 and U712). Data lines from the ROMs are buffered by U715. Address bits A8 through A15 are buffered and latched in U712. This is necessary because glitches in RAM can occur if the bank is switched while $\overline{RAS}$ is active. This could happen when the Z80A-CPU is executing instructions from RAM because $\overline{MEMR}$ and the address are removed at the same time in M1 cycles (opcode fetches). Since $\overline{RAS}$ is active for several dot times after $\overline{MEMR}$ is raised (U81 is clocked by DRC), short $\overline{RAS}$ signals could be applied to one bank of RAM if a switch to that bank were made before $\overline{RAS}$ was raised. To prevent this problem, $\overline{ADDRLATCH}$ (the OR of U81 Qd and MUXB) is active (low) whenever the Z80A-CPU address bus has RAM access, or while $\overline{RAS}$ is active (low).

3.1.5 There are eight I/O devices that the Z80A-CPU communicates with. The Z80A-CPU I/O addressing scheme decodes the three most significant I/O address bits, A7-A5. Each I/O device consists of registers that are decoded by address bits A4-A0. I/O addresses are allocated as follows:

I/O ADDRESS (HEX)	DEVICE
00	Selftest Register (U515)
20	Keyboard/Printer 8041A data bus buffer (U514)
21	Keyboard/Printer 8041A status register (U514)
40	Video 8041A data bus buffer (U710)
41	Video 8041A status register (U710)
60	Interrupt Vector Register (U615)
80	Z80A-SIO/2 Port A data (U716)
81	Z80A-SIO/2 Port B data (U716)
82	Z80A-SIO/2 Port A command (U716)
83	Z80A-SIO/2 Port B command (U716)
A0	Datacomm OCDs (U217, U518, U618, U718)
C0	Datacomm OCRs (U717, U817)
E0	Dual Baud Rate Generator (U516)

The interrupt vector register and the selftest register are described below. The other I/O devices are described in their respective sections.

3.1.5.1 There are three devices capable of interrupting the Z80A-CPU: the video 8041A, the keyboard/printer 8041A, and the Z80A-SIO/2. The interrupt vector register (U615) allows the Z80A-CPU to determine which device is interrupting at any given time. The interrupt lines ($\overline{VRDY}$, $\overline{KRDY}$, and $\overline{SINT}$) for the three devices are ORed together (by U315 U415) to form $\overline{INT}$, which is connected to the Z80A's $\overline{INT}$ input. The interrupt vector register is polled in the interrupt routine to see which device has interrupted.

The I/O selector, U216, is disabled when M1 is high and $\overline{IORQ}$ is low. This condition occurs during an interrupt/acknowledge cycle of the Z80A-CPU. Because this system uses polling to determine which device has interrupted, the selector is disabled during this cycle.

3.1.5.2 The selftest register, U515, is a write only latch that drives the selftests LEDs. The terminal selftest is run each time the terminal is powered on, and it can be run by executing one of the "service keys" functions. The meaning of the LEDs is shown in table 1. The latch also has outputs that: control which bank of firmware ROMs is being addressed (BANK2), reset the video 8041A on hard reset ($\overline{VRESET}$), and control the frame rate of the CRT Controller (50/60 Hz).

Table 1

LED DISPLAYED ERRORS

Error description	Error code LED4-------LED0
0) Selftest passed	0 0 0 0 0
1) Z80A-CPU Processor failure	0 0 0 0 1
2) RAM functional error	0 0 0 1 0
3) RAM traveling 1's and 0's test failed	0 0 0 1 1
4) Video 8041A selftest failed	0 0 1 0 0
5) RAM marching 1's and 0's test failed	0 0 1 0 1
6) Keyboard/Printer 8041A selftest failed	0 0 1 1 0
7) No character ROM(s)	0 0 1 1 1
8) Bad firmware ROM 0 (See Note 1)	0 1 0 0 0
9) CRC error - firmware ROM 0	0 1 0 0 1
10) Bad firmware ROM 1	0 1 0 1 0
11) CRC error - firmware ROM 1	0 1 0 1 1
12) Bad firmware ROM 2	0 1 1 0 0
13) CRC error - firmware ROM 2	0 1 1 0 1
14) Bad firmware ROM 3	0 1 1 1 0
15) CRC error - firmware ROM 3	0 1 1 1 1
16) Bad firmware ROM A	1 0 0 0 0
17) CRC error - firmware ROM A	1 0 0 0 1
18) Bad firmware ROM B	1 0 0 1 0
19) CRC error - firmware ROM B	1 0 0 1 1
20) Bad firmware ROM C	1 0 1 0 0
21) CRC error - firmware ROM C	1 0 1 0 1
22) Integral printer error	1 0 1 1 0
23) CRC error - CMOS RAM	1 0 1 1 1
24) RAM error - nondestructive test	1 1 0 0 0
25) CRC error - character ROM 0	1 1 0 0 1
26) CRC error - character ROM 1	1 1 0 1 0
27) Port 1 error	1 1 0 1 1
28) Port 2 error	1 1 1 0 0
29) Undefined	1 1 1 0 1
30) Undefined	1 1 1 1 0
31) Selftest not run	1 1 1 1 1

NOTE 1: Bad firmware can be: bad ID, wrong configuration address, or no ROM)

NOTE 2: The error codes are binary, 1=LED on, 0=LED off. The LEDs are placed on the processor board with the most significant bit being LED4, and the least significant bit being LED0. LED0 is nearest to the rear edge of the board, where the datacomm and keyboard ports are located.

3.2 DATACOMM SUBSYSTEM

3.2.1 The datacomm interface consists of a Z80A-SIO/2 (a two channel asynchronous/synchronous communications chip), an I/O write only latch (U517) for Optional Control Drivers (OCDs), and buffers (U811) for Optional Control Receivers (OCRs). The Z80A-SIO/2 performs serial-to-parallel and parallel-to-serial data conversion for receiving and transmitting, performs parity checking/generating, and detects framing errors. Channel A is used for port 1 (J-6) and channel B is used for port 2 (J-5). The Z80A-SIO/2 contains a three byte receive buffer and a one byte transmit buffer. Clock selection for port 1 is effected by U815 and follows the truth table below. Port 2 uses only an asynchronous x16 clock.

Port 1 Clock Select

S1	S0	TxCa	RxCa	Usage
0	0	ST	RT	SYNC
0	1	x16	x16	ASYNC
1	0	ST	ST	CLOCK input
1	1	Hblnk	Hblnk	TEST

The $\overline{INT}$ line from the Z80A-SIO/2 is latched by an RS flip-flop to ensure that the Z80A-CPU acknowledges and services datacomm interrupts that may occur. This is necessary because execution of a RETI (return from interrupt) instruction by the Z80A-CPU will cause the Z80A-SIO/2 to deassert its INT line. If a video interrupt is being serviced when the Z80A-SIO/2 asserts its interrupt, the RETI from the video interrupt would cause the Z80A-SIO/2 to remove its interrupt.

Motorola MC1488 and MC1489 (or equivalent) transmitters and receivers are used on the RS-232-C signal lines and on the OCRs and OCDs in order to meet EIA RS-232-C, CCITT V.28, and CCITT V.24 recommendations.

3.2.2 Baud rates are generated from a Dual Baud Rate Generator (a Motorola K1135B), which is a hybrid circuit containing its own crystal oscillator (base frequency= 5.0688 MHz). Each channel is programmed independently; both channels may operate at any of the internally preprogrammed speeds. The upper nibble of the data byte selects the baud rate for channel B, and channel A's speed is determined by the lower nibble. The supported baud rates are EXT., 110, 134.5, 150, 300, 600, 1200, 1800, 2000, 2400, 3600, 4800, and 9600. The base frequency is buffered to obtain X1 and X2, which are clock signals for the video and keyboard/printer 8041As. One counter of U616 (a dual 4 bit binary counter) is clocked by the base frequency of the baud rate generator to obtain the Terminal Timing and TTLX8 clock signals, which are output on port 1. The other counter of U616 is used by the keyboard/printer subsystem. (See section 3.3.2)

3.3 KEYBOARD/INTEGRAL PRINTER SUBSYSTEM

3.3.1 The Keyboard/Printer Interface is controlled by an 8041A slave microprocessor (U514). The 8041A scans the keyboard, passes keycodes to the Z80A, and rings the bell. The keyboard is scanned every 38 ms. The 8041A also is responsible for reading the character ROMs, formatting and passing dot information to the Thermal Print Mechanism (TPM), and controlling the TPM. U414 (an octal tristate transceiver) buffers lines KEYA0-KEYA7. This bus is used for key scanning signals, printer status and data transactions between the TPM and the 8041A.

The Keyboard/Printer 8041A interrupts the Z80A-CPU whenever the status of a key changes, during key repeat, or at the completion of a TPM operation.

3.3.2 Dot data for the TPM is obtained from the character ROM in the following manner. ASCII data for a character (including PSC0, character set select bit 0) is output on port 1 of the 8041A (PSC1, character set select bit 1, is output on port 2, line P25, and latched in U317). When clocked by a signal on line P24, the ASCII data is latched in U412, and the scan line counter (1/2 of U616) is cleared. The character ROM is now being addressed for the first scan line of dot data for the current ASCII character. Valid dot data is returned on PFONT, and latched in U512 when clocked by LRC. LRC is used for the clock because the read can only occur during horizontal blank time. This is the only time the display subsystem is not using the character ROMs. The Z80A-CPU processes the dot data for the characters and sends the required information to the TPM. As the current scan line is read, the scan line counter is incremented and U512's outputs are disabled by line P23 (the act of disabling U512's outputs clocks the scan line counter because CNTRCLK is the inverse of P23's state). The next scan line is thus addressed on the character ROM and read when LRC clocks the latch (U512).

3.4 DISPLAY SUBSYSTEM

3.4.1 All of display allocated RAM is segmented into 128 (or 256) byte blocks on 128 (or 256) byte boundaries; the low 7 bits are zero for the first address in the block. One or two of these blocks contain all of the information necessary for one character row. This includes ASCII codes, hardware enhancement information, and software enhancement information. If two blocks are needed to describe a character row, they must be contiguous and start on a 256 byte boundary. There are five types of bytes that occur in a character row block, an ASCII character (1 byte), two software enhancement bytes (the two bytes always occur in an ordered pair), and two hardware enhancement bytes. The table below shows the definitions of each byte's bit positions.

DISPLAY MEMORY BYTE TYPES

0	ASCII CHARACTER

Software Bytes

1	0	NDT	field end	field start	total fill	MDT	REQ'D

1	0	0/blank fill	justi-fied	FIELD EDIT TYPES (See below)

Hardware Bytes

1	1	0	SEC	HB	UL	IV	BL

1	1	1	SPARE	NHS	CHAR SET	EOL

Field Edit Types

0 = Unrestricted
1 = Alphabetic
2 = Upper case alphabetic
3 = Alphanumeric
4 = Integer
5 = U.S. Signed Decimal
6 = Implied decimal
7 = Constant
8 = Integer/fill
9 = Signed decimal/fill
A = Implied decimal/fill
B = Numeric
C = Currently unused
D = Currently unused
E = Currently unused
F = Currently unused

Enhancement Type Abbreviations

BL = blinking
EOL = end of line
CHAR SET = character set
HB = halfbright
IV = inverse video
MDT = modified data tag
NDT = non-display terminator
NHS = no half-shift
REQ'D = required
SEC = security (no display)
UL = underline

The first 8 bytes of each block contain flags, pointers, and a crunched block address (described in section 3.4.3.2). The firmware maintains a linked list of the row start addresses of the character row blocks. It is this sequencing of character row blocks that makes up the terminal display.

3.4.2 The heart of the Display Subsystem is the CRT Controller (CRTC), a National DP8367N. The CRTC generates all timing and control necessary for terminal display. This includes the horizontal and vertical blank signals, the scan line counters, the dot clock and all clocks needed by the line buffers and dot shift registers.

3.4.3 An 8041A provides the intelligent interface between the Z80A-CPU and the CRTC. The 8041A does the following: provides the CRTC with row pointer information, controls the cursor position hardware, determines the blink rate for both the cursor and the blinking enhancement, and blanks the screen upon request. The duty cycle for the blink rate of the cursor is 50% (a period of 400 ms), while the blinking enhancement has a 83% duty cycle (a period of 800 ms).

3.4.3.1 The Video 8041A interrupts the Z80A-CPU every frame near the beginning of Vertical Blank. The Z80A-CPU is permitted at this time to give the 8041A information affecting the next video frame. This information may be a new cursor position, 26 row start pointers for the next frame, a command to turn video off, a command to turn video on, a start selftest command, or a no change in frame command. If the Z80A-CPU is servicing another interrupt when a video interrupt occurs, the video 8041A will time out, remove its interrupt, an assume no change in frame.

3.4.3.2 The row start pointers consist of a single byte that is a crunched block address. This is possible because the lower 7 bits of the address are "0's" (all blocks begin on 128 byte boundaries) and the most significant bit is a "1" (all RAM is located in the upper 32K of the address range). Thus, a single byte contains the necessary information for the block address.

3.4.3.3 While a character row is being displayed, the CRT Controller is addressing display memory for information for the next character row to be displayed. This display memory access (DMA) also performs RAM refresh. The CRT Controller performs its display memory addressing during lines 0, 4, and 8 of the fifteen scan lines of a character row. To obtain all of the data for the longest possible line, 240 bytes of RAM must be addressed. U77 decodes the scan line counter outputs, from which $\overline{LC048}$ is generated. When $\overline{LC048}$ is active, U94 turns on MUXB, which gives the CRTC access to memory.

Since the CRTC reads 80 sequentially addressed bytes at a time, and it must read 240 bytes per character row, 3 pointers are passed to the CRTC per row. The 8041A is given a single pointer per character row by the Z80A-CPU (See section 3.4.3.1). This address pointer plus 8 is latched in U79 and U89. (The value 8 is added because the first 8 bytes of a block do not contain character data). As the scan line counter rolls to 0, but during horizontal blank, this value is loaded into the CRTC (the load signal is generated by U84 and U85), and 80 bytes of RAM are addressed by the CRTC. The 8041A is interrupted during the CRTC load sequence by $\overline{LC048}$. This informs the 8041A that the next pointer will be needed. To obtain the next pointer the 8041A adds 80 to the original address pointer and latches the new value in U79 and U89. The new value is loaded into the CRTC on scan line 4, 80 bytes of RAM are addressed, and the 8041A is interrupted again. This time the 8041A adds 160 to the original address pointer and latches this in U79 and U89. On scan line 8, the CRTC is loaded with this value and 80 bytes of RAM are addressed. This sequence is repeated for each character row. The 3 lowest bits of the row start pointer are 0 (tied to ground) because the initial value was incremented by 80 or 160; the three least significant bits are not needed to represent these numbers.

The 8041A must be synchronized with the CRTC so the correct pointers for the current row are passed to the CRTC. This is accomplished by monitoring $\overline{LC048}$ and the VSYNC output of the CRTC. The microcode for the 8041A knows how many interrupts per frame $\overline{LC048}$ generates. When VSYNC becomes active, the interrupts are counted and when the appropriate number for the frame rate (50 or 60 Hz) have occurred, the next interrupt will be for the first scan line of the first row of the next frame. The CRTC and the 8041A are then synchronized with each other and the addressing sequence described above is performed.

3.4.3.4 If the Z80A-CPU attempts to access RAM during scan lines 0, 4, or 8, it is put into wait states by VWAIT (video wait). This means the Z80A-CPU is locked out of system/display RAM about twenty percent of the time. However, VWAIT is the logical AND of the following conditions: RAM is being accessed (state of BA15), the CRTC is accessing RAM (state of MUXB), and the Z80A-CPU is attempting to access RAM (state of $\overline{MEMR}$). Thus, the Z80A-CPU is not prevented from making ROM or I/O operations during video access to RAM.

3.4.4 The character row information is contained in a byte-serial format, and is read sequentially by the CRT Controller. The sequentially addressed bytes are latched in U49, which is clocked by DMALATCH. The bytes are then decoded one at a time by U15, U17, U18, U25, and U27. Bytes decoded as software enhancements are discarded, hardware enhancement bytes (video enhancements) are latched in U39 and held for subsequent ASCII codes, and character set select bits are latched in U28. Bytes decoded as ASCII codes cause two 80 byte shift registers to be clocked, one clocking in the ASCII code itself (U29), the other shift register (U38) clocking in parallel the last hardware enhancement byte latched. It is in this way that a single enhancement byte stored in a character row block propagates to the end of the block.

3.4.4.1 Once 240 bytes of RAM have been addressed and decoded, shift registers U29 & U38 contain either 80 new bytes or fewer than 80 new bytes for the next row. The shift registers must be justified if they do not contain 80 new bytes. For instance, if 10 ASCII bytes have been clocked into U29, these bytes must be the first 10 bytes to be clocked out (into the line buffers) if they are to be displayed as the first 10 characters of the next row on the CRT. Justification of the data in U28 & U39 is accomplished as follows:

The REC (recirculate) signal from the CRTC is input on bit A1 of U38; the state of this bit at the output is used to determine when U29 & U38 are justified (Full). At the start of a new row, U38 contains all "0's" for bit A1 because REC was low during scan line 15 of the previous row (See section 3.4.4.2). A "1" is clocked into bit A1 on the first clock of the next row, so this "1" is coincident with the first byte (ASCII and its enhancement, as U29 & U38 are clocked together) of the next row. When the "1" appears at the output of U38, the shift register is full and the clock signal (LBCDEL) is disabled by JUSTIFIED. If there are fewer than 80 new bytes, U38 is filled with enhancement bytes that have only the SEC (security) bit set. The EOL (end of line) enhancement bit (an "E1" Hex enhancement byte is always present at the end of a logical row) sets the flip-flop comprised of U25 (gates on pins 1 & 13) which sets the SEC bit (via U211 pin 6) and clears all other enhancements (U39 is cleared). Thus, characters after an "E1" are clocked into U29 to justify the row, but are not displayed because the SEC bit is set. Justification must take place before scan line 15, so scan line 13 was chosen.

3.4.4.2 The line buffers (U210 & U37) recirculate data on the first 14 scan lines (REC is high) and load the data for the new character row on the last scan line (REC is low). The 80 bytes in U29 & U38 are transferred to U210 & U37 on the fifteenth scan line of the row currently being displayed. The line buffers then contain all of the ASCII codes and enhancements for the next row. The ASCII codes are output and latched in U310, which is clocked by LCG, for character ROM addressing. The character set select bits and scan lines are latched in U311 (See section 3.4.5). Hardware enhancements are latched in U35 and then U34. The one character time delay introduced by U34 is necessary because the dots from the character ROMs are latched one character time after they were addressed; the delay synchronizes the dots with the appropriate enhancement. The data in the line buffers is recirculated so the dots for each scan line may be addressed.

3.4.5 The character ROMs (U410 and U411) are addressed by the ASCII codes from U310, and by the character set select bits and scan line counter outputs from U311. See the memory map below. Each character's scan line segment is stored in ROM as an 8-bit word. A "0" stored in the ROM indicates a dot is present. Usually, seven of the bits are used for character dots, while the eighth is used for specifying half-shifting of the character dots. For character sets requiring the full width of a character cell (9 dots), all eight bits are used for character dots, the first dot being duplicated to yield nine dots. This does put a constraint on the way full width character sets are defined, but the 2645A compatible line drawing set and large character set do not suffer from this drawback.

Character ROM Address Map

BIT	CONTENTS
0-3	scan lines
4-10	ASCII character
11, S1	character set select

The data from the character ROMs is serialized by two four bit parallel access shift registers, U510 and U511. For characters using 7 dot positions, the data is clocked on the rising edge of DRC in U313. If half-shifting of dots is used, the data is clocked on the falling edge of DRC in U314. To obtain 9 dot characters, the Qd output of U511 is used for the first dot, while the rest of the dots are taken from $\overline{Qd}$ and clocked through U212. Decoding of 9 dot, 7 dot, or 6 dot half-shifted data is done by U312. The selector inputs are NINEDOT, LOAD, and HALFSHIFT. The waveform of the dotstream from U312's output is shaped by the circuit of Q1. The effect of this circuit is to stretch the trailing edge of the dots to make a better looking character on the CRT. The data is then synchronized with the hardware enhancements from the U34, and sent to the sweep PCA for display.

The character ROM data is also addressed by the keyboard/printer 8041A for the TPM. The dot data is sent in parallel to U512 for use by the TPM. (See section 3.3.2)

3.4.6 The terminal display contains 26 rows of 80 columns. The last two character rows are used for soft keys and error messages. Each character occupies a nine dot by fifteen scan line cell. The entire screen, then, contains 390 scan lines, and 720 dot columns. The dot frequency of 25.7715 MHz (38.8 ns) is controlled by Y1, making a character rate of 2.863 MHz (349 ns). The horizontal scan frequency is 24.9 KHz (40.16 us), because horizontal blanking takes 35 character times (12.24 us) in addition to the 80 character times that are displayed. To refresh the CRT at 50 or 60 Hz, extra scan lines are added for 50 Hz refresh instead of changing the horizontal sweep frequency. Thus, there are 415 scan lines for 60 Hz, and 498 scan lines for 50 Hz. The AC vertical centering used by the sweep PCA effects a final constraint in the raster control circuitry. To implement these functions, each frame has the following states:

SSL - Starting Scan Lines
Six scan lines are used after vertical retrace to stabilize the display.

ACTIVE VIDEO - Video Display
The character field consists of 390 scan lines, 26 character rows of 15 scan lines per row.

ESL - Extra Scan Lines
38 extra scan lines are added for 50 Hz CRT refresh before vertical retrace for 50 Hz. None are added for 60 Hz refresh.

VR - Vertical Retrace
The vertical retrace period is 19 scan lines for 60 Hz and 64 scan lines for 50 Hz.

Figure 1 shows a diagram of the states in each frame.

4.0 GLOSSARY OF SIGNAL NAMES

NOTE: All names listed below are defined for the positive sense of the signal (active high). If a bar appears above the label on the schematic, the signal is active low.

0K	chip enable for ROM0
0K2	chip enable for ROMA
8K	chip enable for ROM1
8K2	chip enable for ROMB
16K	chip enable for ROM2
16K2	chip enable for ROMC
24K	chip enable for ROM3
A15-A0	unbuffered address lines from the Z80A-CPU
ADDRLATCH	controls latching of the upper 8 address bits (see section 3.1.4.2)
BA15-BA0	buffered address lines from the Z80A-CPU
BATRET	backup battery return line
BATTERY	backup battery Vcc
BELL	unbuffered bell signal from the keyboard/printer 8041A
BLINKING CURSOR	complete blinking cursor signal
BLRATE	rate of blinking enhancement
CAS	dynamic memory column address strobe
CAS1,2	CAS1 is for U41-U48, CAS2 is for U51-U58
CNTRCLK	clock signal for one counter of U616, controlled by the keyboard/printer 8041A
CNTRCLR	clear signal for one counter of U616, controlled by the keyboard/printer 8041A

CONFIG	CMOS RAM chip enable
CURBLINK	cursor blinking signal
CURSOR	cursor signal, active during part of scan line 13
D7-D0	unbuffered data lines from the Z80A-CPU
DFREQ	buffered 25.7715 MHz signal from the CRTC, from which PHI is obtained (inverse of DRC)
DMALATCH	clock signal for line buffer U49 (see section 3.4.4.1)
DOT8	character ROM data bit 8, used to select half-shifting of dots within a character cell
DOTS	serial video data line
DRC	buffered dot rate clock (25.7715 MHz), from the CRTC
FULLBRIGHT	full-bright video data
GND	signal and power ground
HALFBRIGHT	half-bright video data
HALFSHIFT	half-shift dot data
HBLANK	horizontal blanking signal
HORDR	horizontal drive signal
IEO	Z80A-SIO/2 interrupt enable output
INT	Z80A-CPU interrupt request input
IORQ	Z80A-CPU input/output request line
JUSTIFIED	indicates when line buffers U38 and U29 are full (justified)
KBELL	buffered bell signal that drives the speaker in the keyboard housing
KEYA6-A0	key address
KEYACT	status of selected key
KRDY	keyboard/printer 8041A maskable interrupt output

LBC	line buffer clock, active at the character rate frequency and inactive during horizontal blank
LBCDEL	delayed line buffer clock, lags LBC by about 4 dot times
LC048	indicates scan lines 0, 4, and 8
LC13	indicates scan line 13
LCG	latch character generator address, active at the character rate frequency, used to clock the latches (U310 & U311) for character ROM addressing
LFREQ	line frequency, selects a frame rate of 50 or 60 Hz
LOAD	clocks NINEDOT and HALFSHIFT latches and selects the type of dot data displayed (see section 3.4.5)
LRC	line rate clock, active at the scan line frequency
LVSR	load video (dot) shift register, active at the character rate frequency, during video time
M1	Z80A-CPU machine cycle one, indicates an OP code fetch cycle
MA14-0	multiplexed address lines, video or processor access is determined by the state of the 4 selectors U610, U611, U68, and U69
MEMR	Z80A-CPU memory request, active on all memory accesses except during refresh time
MRD	memory read, both MEMR and RD are active
MREQ	Z80A-CPU memory request, this indicates that there is a valid address on the bus for memory operations
MUXA	multiplex address, controls the RAM address multiplexers
MUXB	enables the video address bus multiplexers on scan lines 0, 4, and 8
NHS	no half-shift
NINEDOT	display all nine dots of a character cell

NMI	Z80A-CPU non maskable interrupt request input
PASCII6-0	character ROM ASCII character address
PCNTL1-0	TPM control lines
PCS1-0	character ROM character set select bits
PDATA7-0/KEYA7-A0	TPM data bus
PDWN	CMOS memory chip enable
PFAIL	power fail signal from the power supply
PFONT7-0	dot data for one scan line of one character, from the character ROM
PHI	clock signal for the Z80A-CPU, 3.6816 MHz
PHIV	buffered PHI
PRD	TPM, printer read
PSCAN3-0	character ROM scan line address
PSEL	TPM, printer select
PWR	TPM, printer write
RAS	dynamic memory row address strobe
RD	Z80A-CPU read signal
REC	line buffer recirculate enable
RESET	main reset signal line
RFSH	Z80A-CPU memory refresh line Note: not used for refresh control, but for other timing
ROMD7-D0	ROM data lines
SBAUD	baud rate generator address strobe
SCAN3-0	unbuffered TPM scan line address, from U616
SELBL	select blinking enhancement
SELIV	select inverse video enhancement

SELND	select non display (security)
SELUL	select underline enhancement
SEXT	selftest register clock
SINT	latched Z80A-SIO/2 interrupt request (output)
SIVREG	interrupt vector register chip enable
SKEYBRD	keyboard/printer 8041A chip select
SOCD	datacomm optional control driver latch clock
SOCR	datacomm optional control receiver register chip enable
SSIO	Z80A-SIO/2 chip enable
SUBD7-D0	keyboard/printer 8041A port 1
SVID	video 8041A chip select
VBLANK	vertical blanking signal
VBUSY	video RAM multiplexer busy, prevents the Z80A-CPU from switching the address multiplexers
VERDR	vertical drive signal
VOFF	video off
VRDY	video ready, video 8041A maskable interrupt ouput
VRESET	video reset
VWAIT	video wait, suspends Z80A-CPU RAM access during video RAM access
WAIT	Z80A-CPU wait input
WE	dynamic memory write enable
WR	Z80A-CPU write signal
X1	clock for both 8041As, 5.0688 MHz
X2	clock for both 8041As, 5.0688 MHz
ZBUSY	Z80A-CPU RAM multiplexer busy, prevents video from switching address multiplexers
Z2RAM	Z80A-CPU to RAM, controls the direction of data flow through U59, the RAM data transceiver

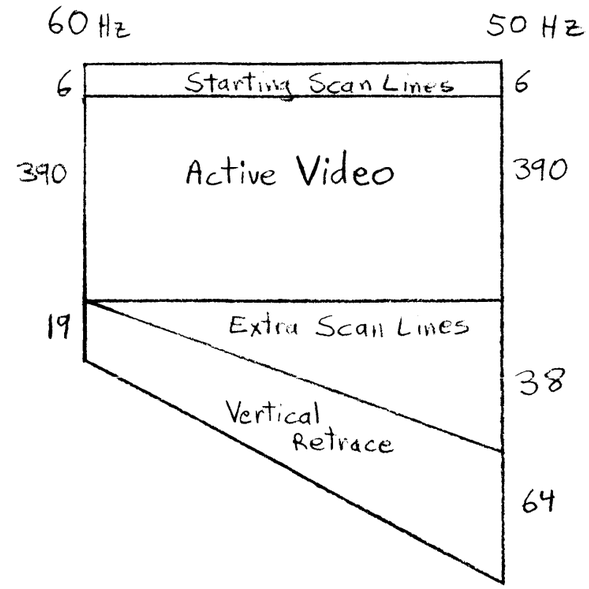
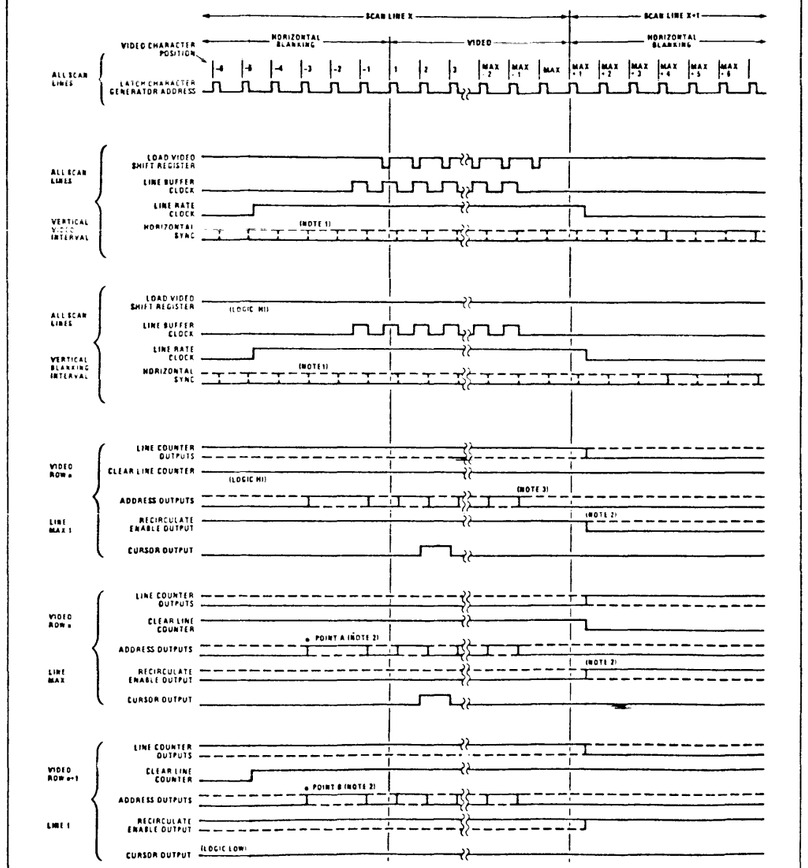


Figure 1
Frame State Diagram
APR-03-81 13220-91097

Timing Diagrams



Note 1: The horizontal sync output start and stop point positions are a function of device type or custom option.

Note 2: The position of the recirculate enable output logic "0" level is dependent on the state of the address mode input. When address mode = "0", recirculate enable occurs on the max. line of a character row (solid line) and the address counter outputs roll over to the new row address at point A. When address mode = "1", recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 3: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR).

Character/Line Rate Functional Diagram

Figure 2
CRTC CHAR/LINE RATE Timing Diagram
APR-03-81 13220-91097

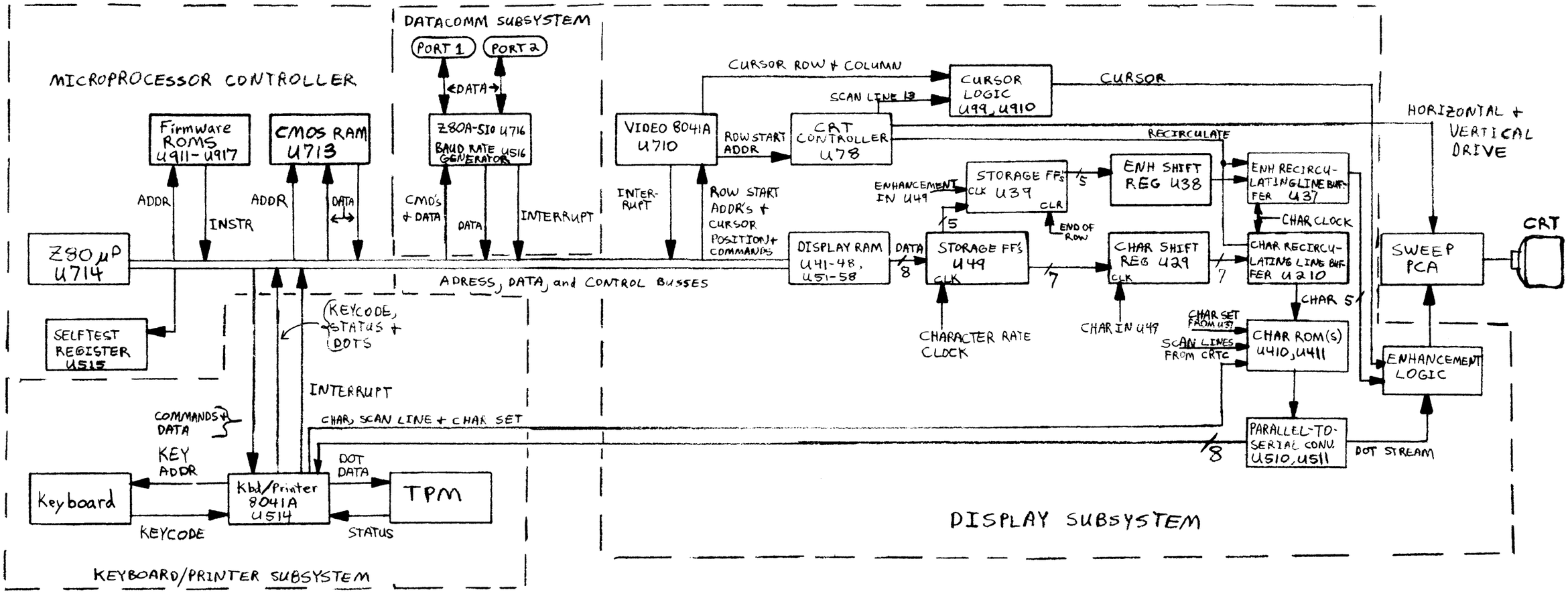


Figure 3
Processor Module Block Diagram
APR-03-81 13220-91097

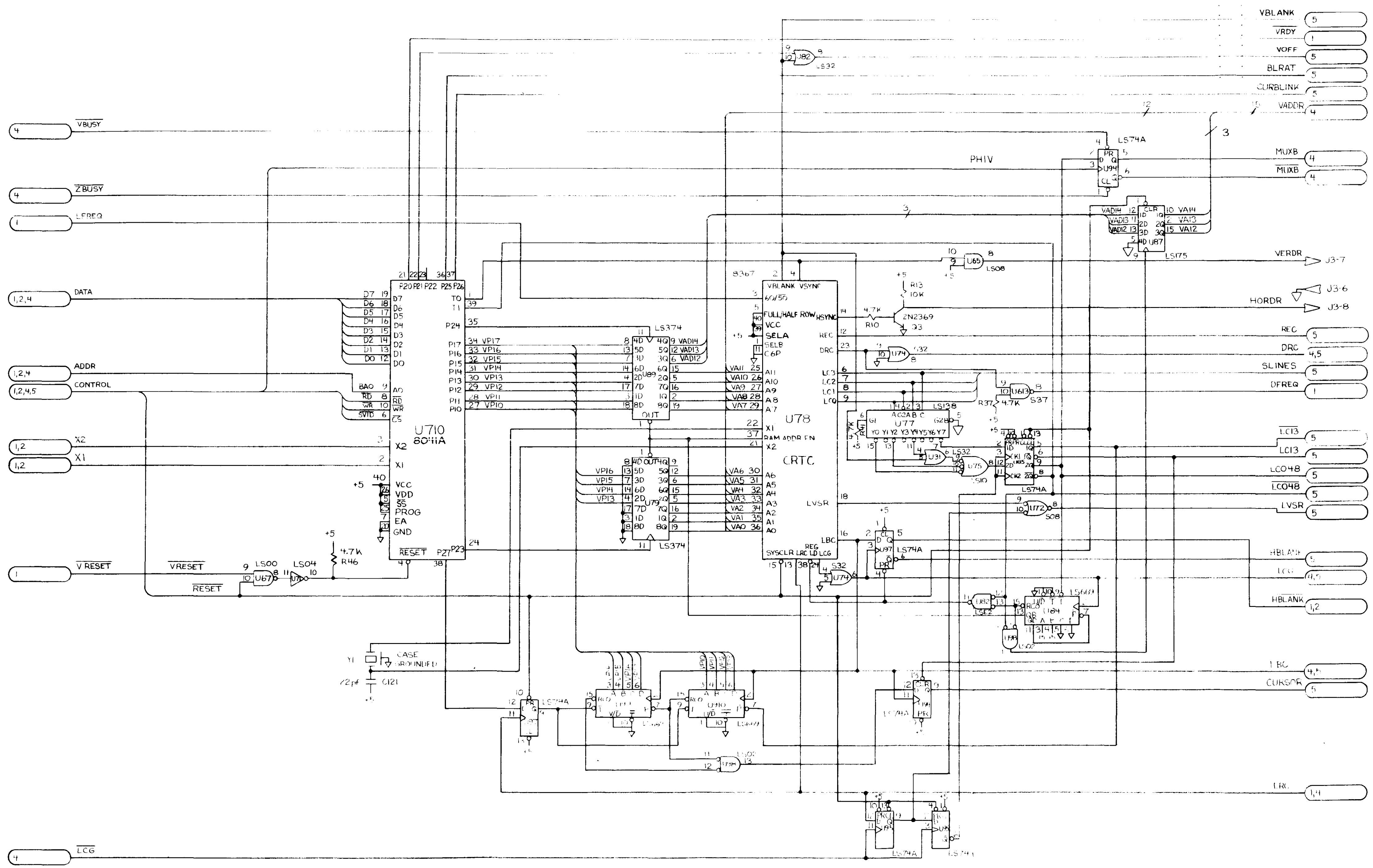
IO ADDRESSES	
BITS	FUNCTION
000	LED'S
001	KEYBRD IPTR
010	VIDEO BOW
011	INT. VECTOR
100	SIO
101	OCD
110	OCR
111	BAUD RATE

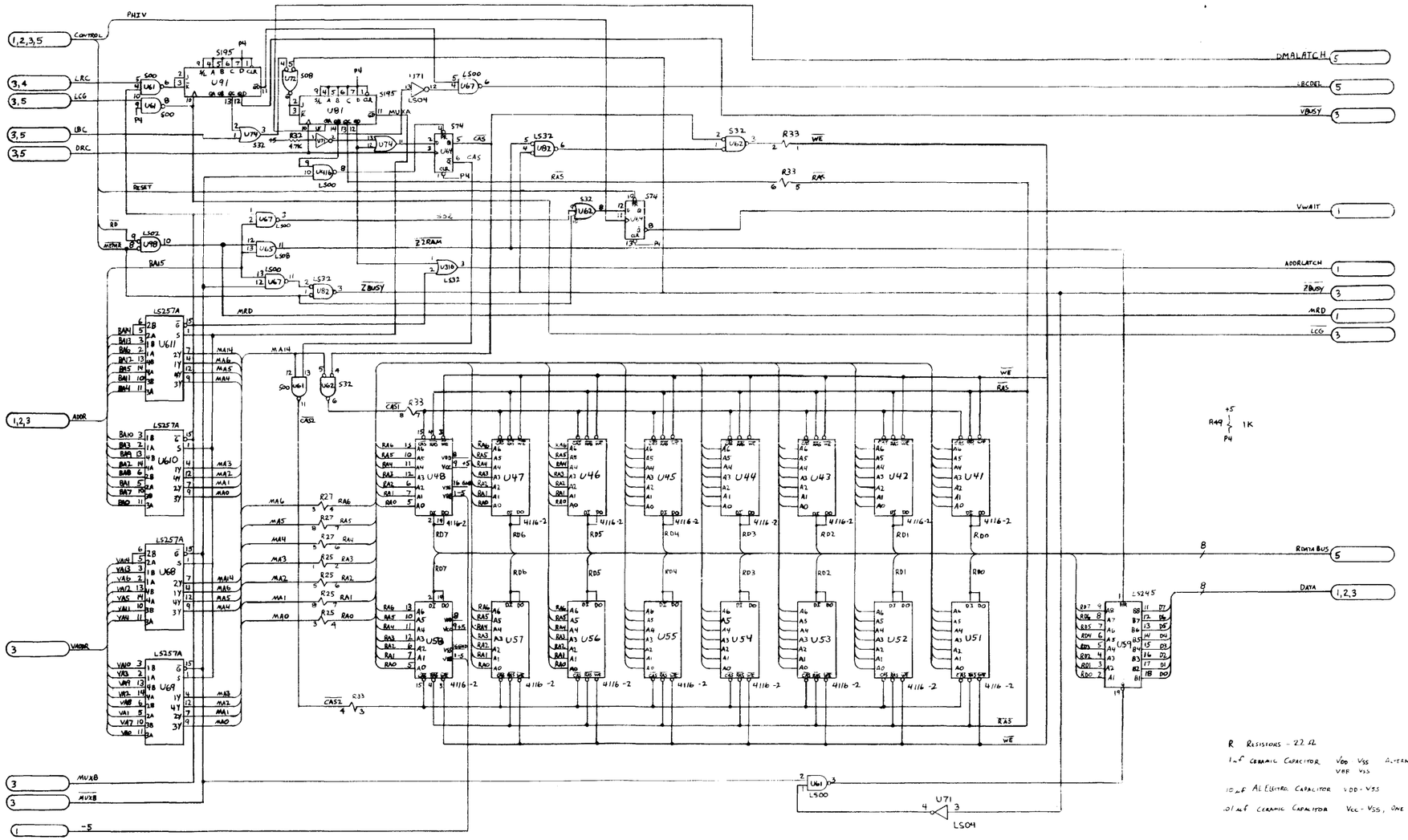
† ROM WIRE JUMPERS:
BA12 IS JUMPERED PER THE FOLLOWING
(ALL ARE PIN # 21):
U911: WG TO BA12 OR W5 TO +5V
U912: W3 TO BA12 OR W7 TO +5V
U916: W10 TO BA12 OR W9 TO +5V
U917: W11 TO BA12 OR W12 TO +5V

* C1-5, 12-21, 26-35, 38-44, 46, 58-61, 67, 69, 72, 74, 76, 79-82, 85, 86, 89-98, 104-110, 112, 116-120, 122-129

† C50-57, 66, 68, 70, 71, 73, 75, 77, 78

Figure 4
Schematic Diagram
APR-03-81 13220-91097


VBUSY
ZBUSY
LFREQ
DATA
ADDR
CONTROL
X2
X1
V RESET
VRESET
RESET
LCG
U710
8041A
U78
CRTC
LS374
LS74A
LS175
LS00
LS04
LS32
LS08
S32
S37
S08
R46
4.7K
R13
10K
R10
R37
2N2369
Q3
C121
CASE GROUNDED
PHIV
VBLANK
VRDY
VOFF
BLRAT
CURBLINK
VADDR
MUXB
VERDR
J3-7
J3-6
HORDR
J3-8
REC
DRC
SLINES
DFREQ
LC13
LC048
LVSR
HBLANK
LBC
CURSOR
LRC



NOTE: WIRE JUMPERS

a) U41-U48 AND U51-U58 PIN 8
W1 JUMPERS TO +12 V
W2 JUMPERS TO +5 V

b) U41-U48 AND U51-U58 PIN 1
W3 JUMPERS TO -5 V
W4 JUMPERS TO +5 V

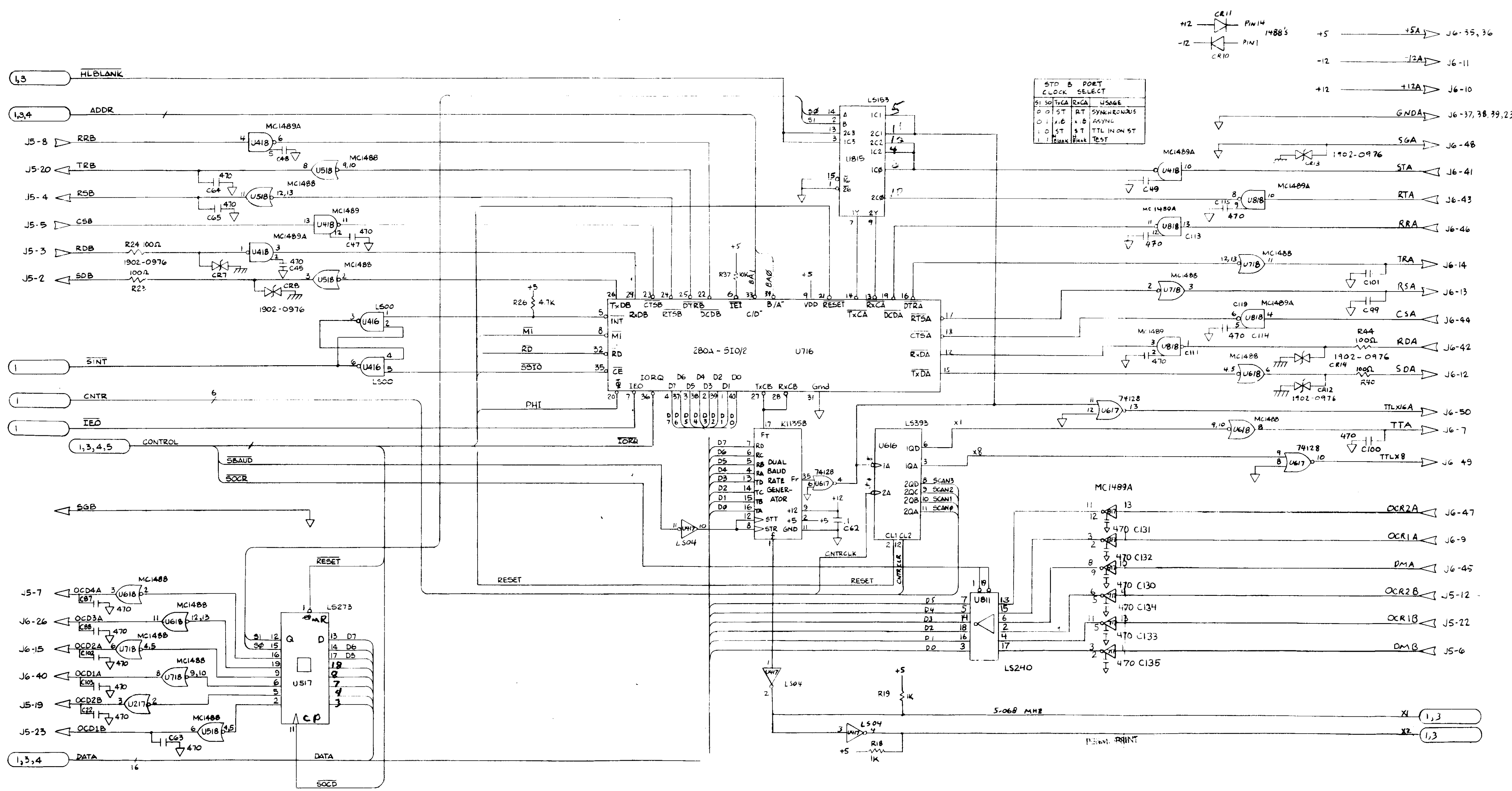
R RESISTORS - 22 Ω — TOTAL 11

1 uF CERAMIC CAPACITOR VDD VSS ALTERNATING VBB VSS — TOTAL = 16

10 uF ALECTRO CAPACITOR VDD - VSS — TOTAL = 1

.01 uF CERAMIC CAPACITOR VCC - VSS, ONE EACH ROW — TOTAL = 2

		PRODUCT
J6 -	DATACOM (A)	STD - 50 PIN
J5 -	PRINTER (B), ext	STD - 25 PIN
J4 -	KEYBOARD	16 PIN RIBBON
J3 -	SWEEP	MOLEX - 7 PIN
J1 -	PRINTER	26 PIN RIBBON
J7 -	POWER SUPPLY	MOLEX - 9 PIN (10 PIN?)



VDEF
HBLANK
CURSOR
RDATA BUS
CURBLINK
BLRATE
LC04B
LC04B
LC13
LBCDEL
REC
VBLANK
DMALATCH
LBC
SLINES
LC6
LC12
CPUPRT
DRC
LWSR
CONTROL
RESET
PSCII6
PSCII5
PSCII4
PSCII3
PSCII2
PSCII1
PSCII0
PCS1
PCS0
PSCAN3
PSCAN2
PSCAN1
PSCAN0
LC11
BLINKING CURSOR
SELBL
SELUL
SLAND
HALFBRIGHT
FULLBRIGHT
J3-1
J3-3
J3-4
J3-5
JUSTIFIED
DAT8
WHS
PSCII15
PSCII16
DW STRETCH
PFONT
R12 1KΩ
R11 1KΩ
P2
P1
4.7K R36
2332 4K×8 ROM
2332 4K×8 ROM

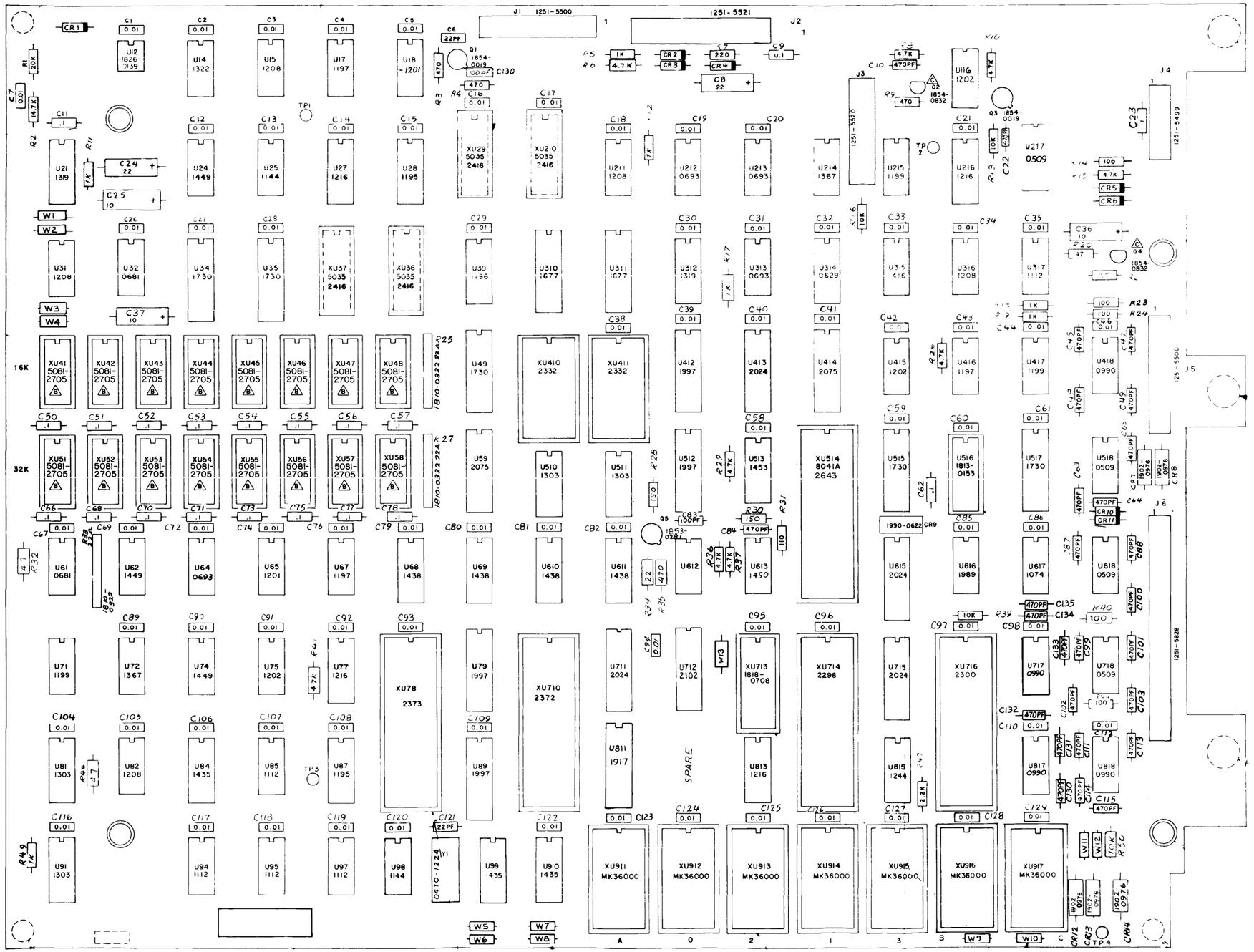


Figure 11
Component Location Diagram
APR-03-81 13220-91097

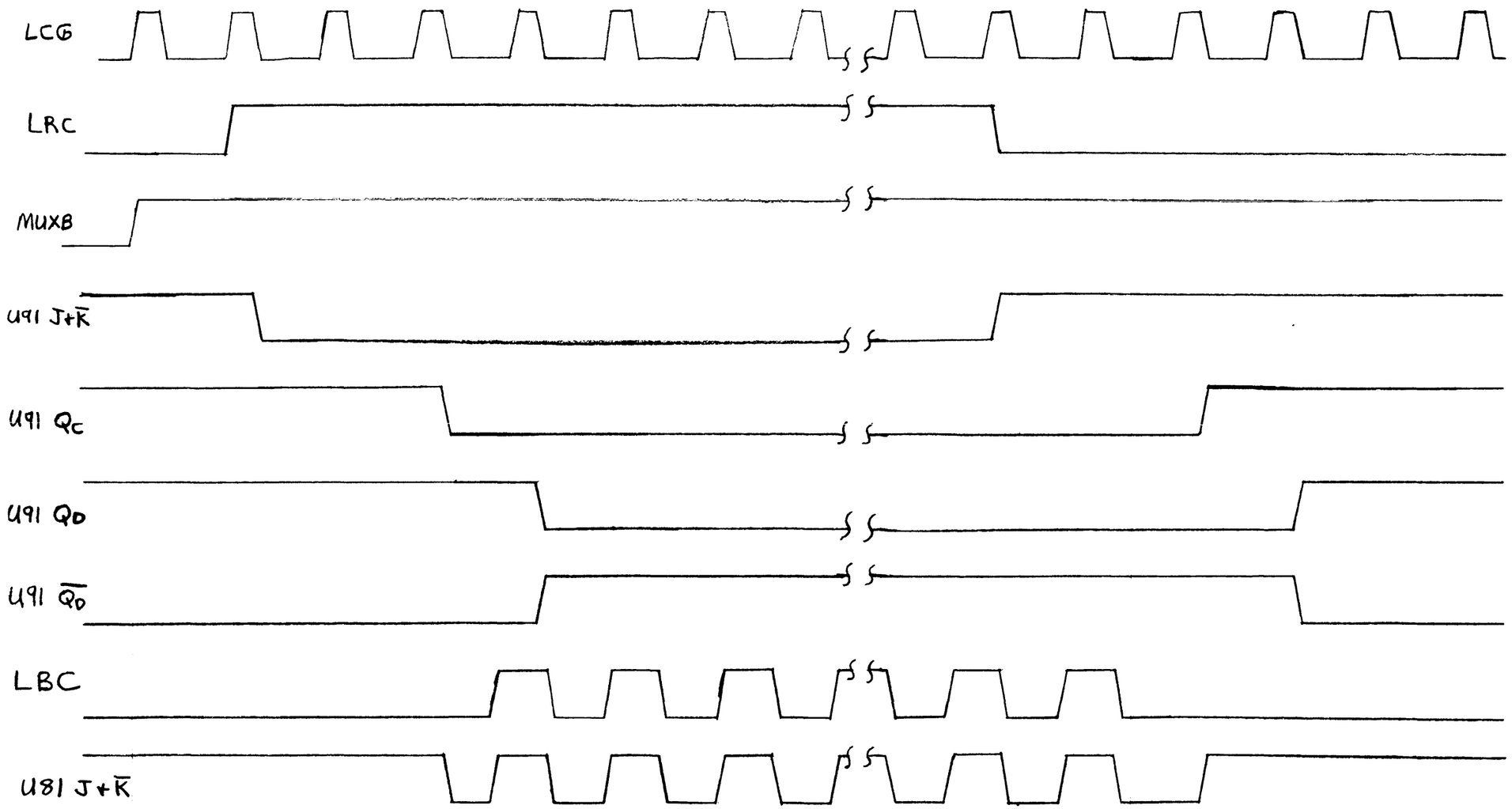


Figure 5
Video RAM access, U91 timing
APR-03-81 13220-91097

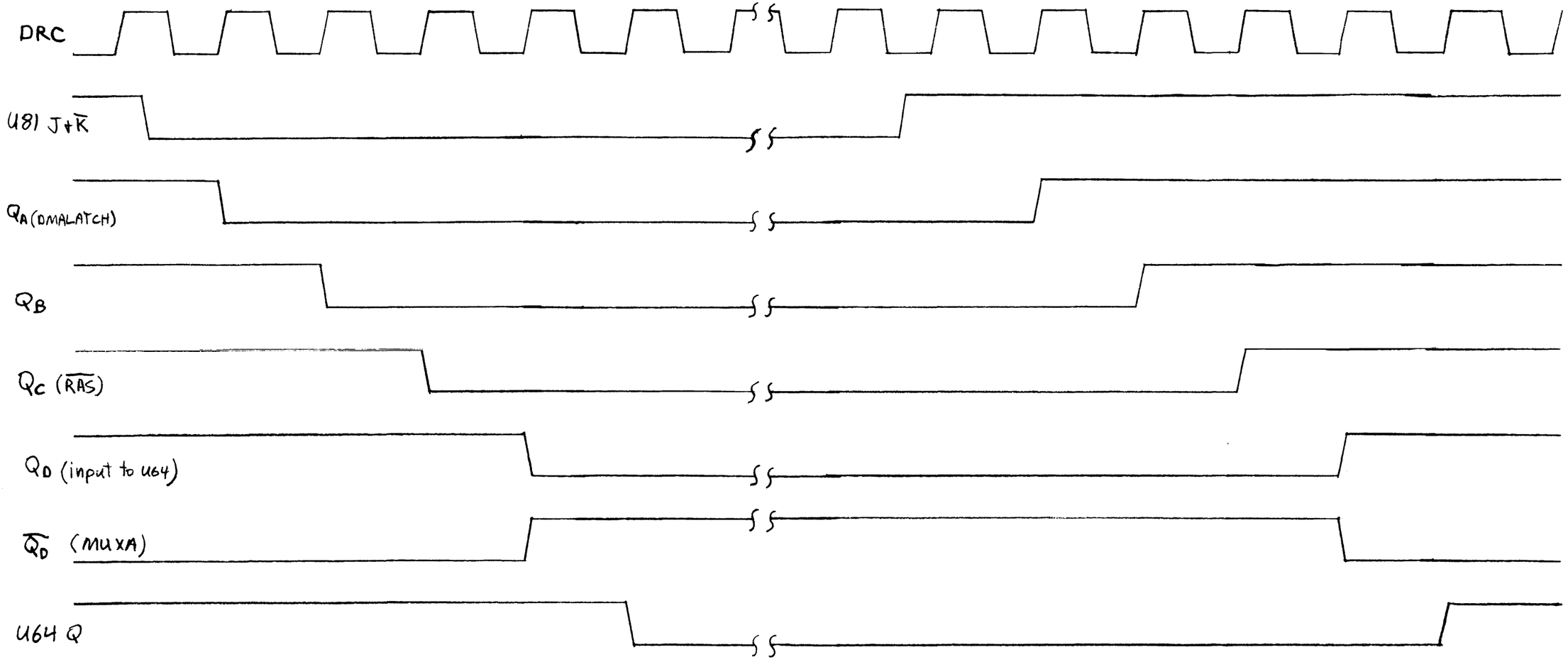


Figure 6
Video RAS, MUXA, and CAS generation
APR-03-81 13220-91097

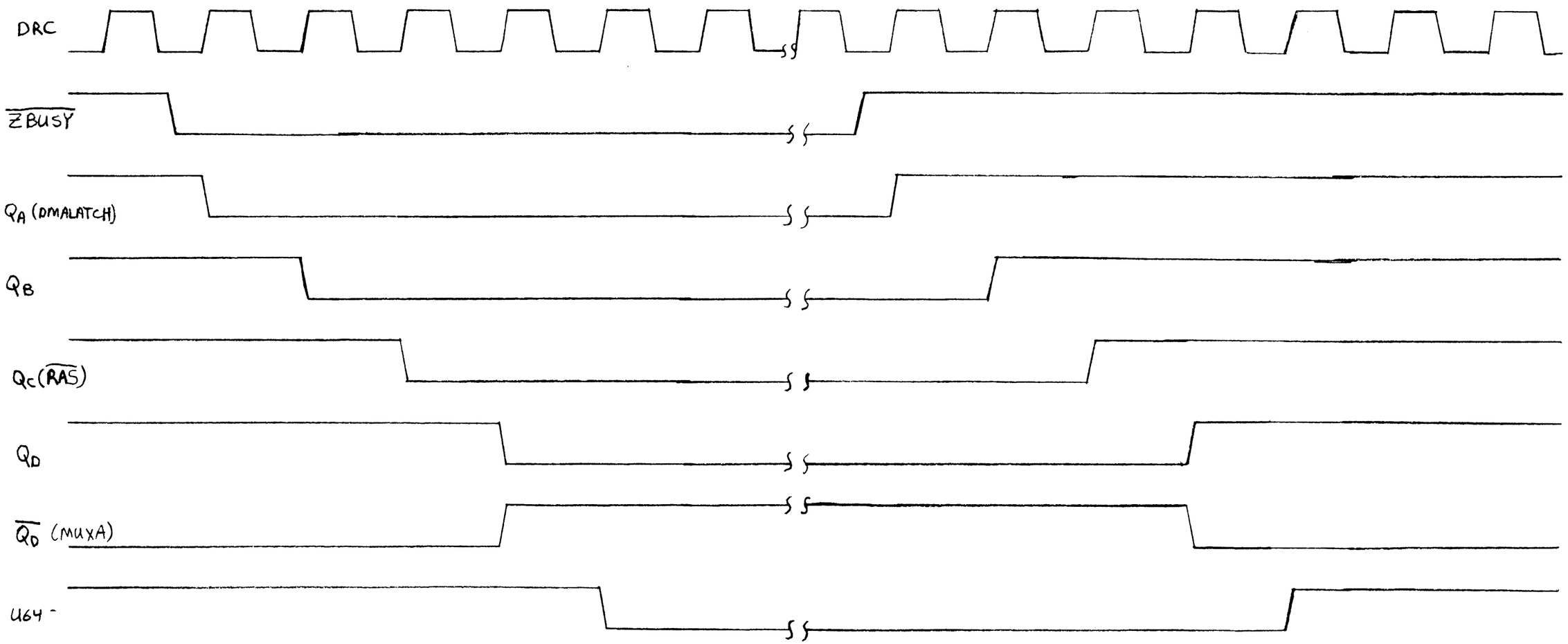
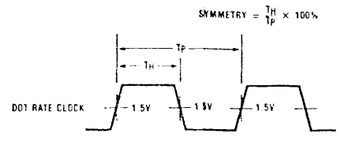
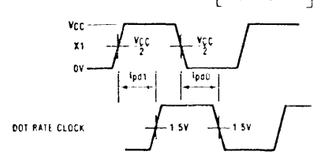


Figure 7
Z80A-CPU RAM accesses, U81
APR-03-81 13220-91097

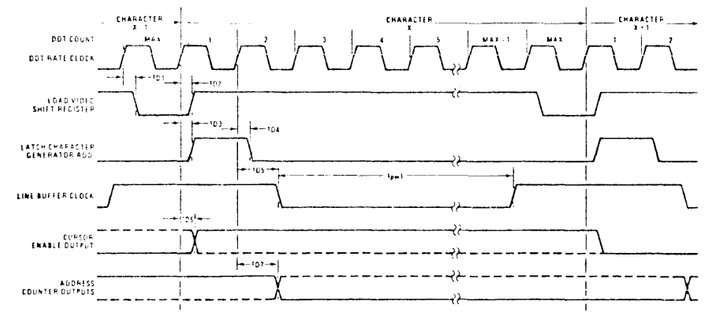
Switching Waveforms



Dot Rate Clock Output Waveform Symmetry with Crystal Control

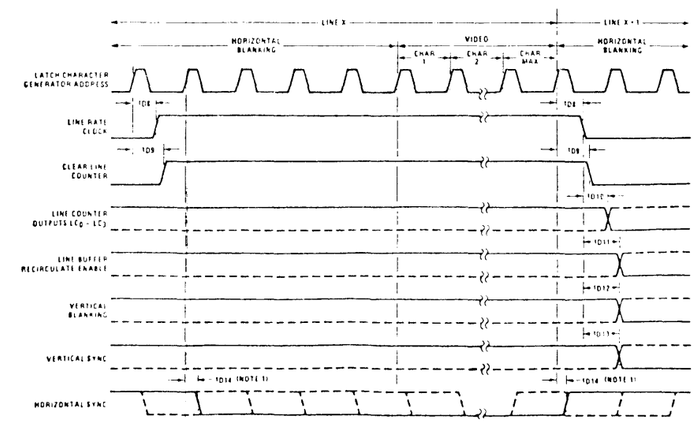


X1 Input to Dot Rate Clock Output Propagation Delay



Note 1: All measurement points are 1.5V

Dot/Character Rate Timing

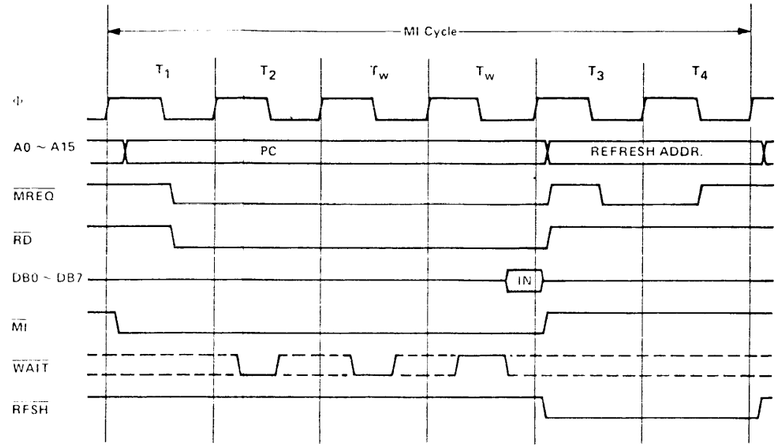


Note 1: Actual polarity and position of the horizontal sync start and stop points is a function of the particular device format

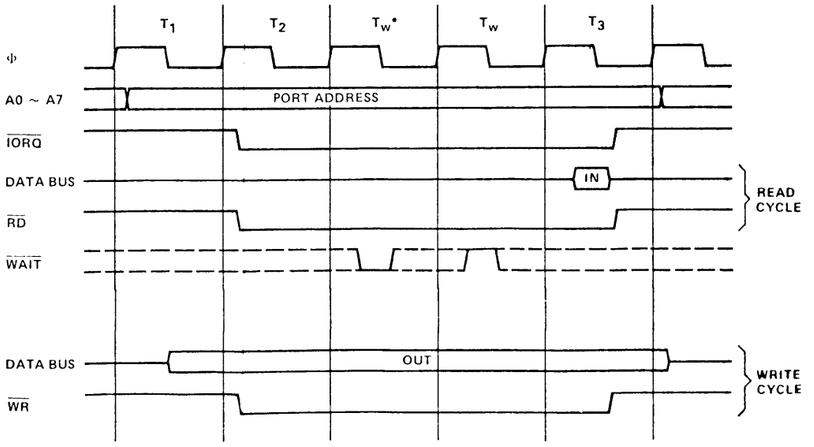
Note 2: All measurement points are 1.5V.

Character/Line Rate Timing

Figure 8
Dot/Char and Char/Line Timing
APR-03-81 13220-91097

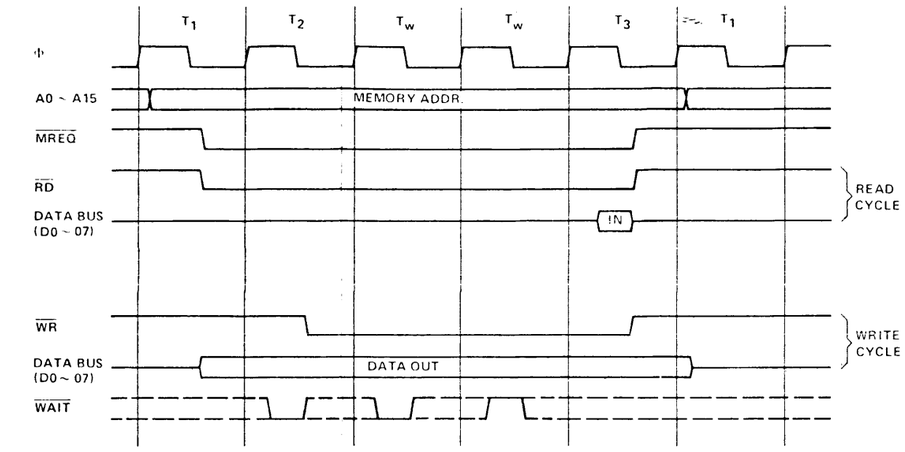


INSTRUCTION OP CODE FETCH WITH WAIT STATES

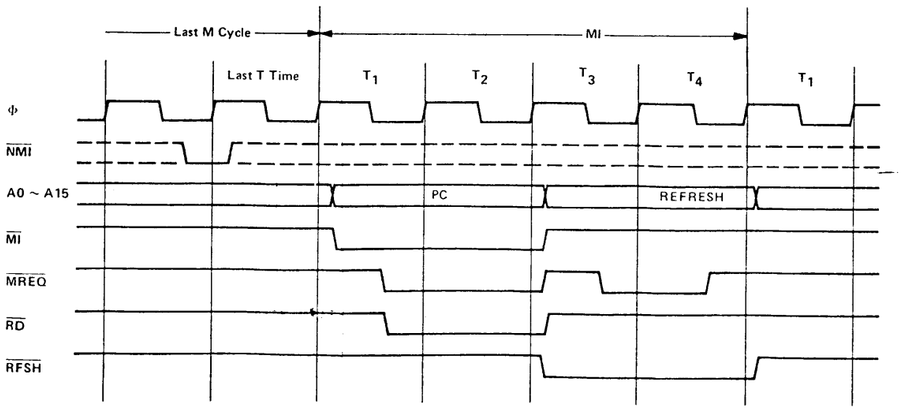


INPUT OR OUTPUT CYCLES WITH WAIT STATES

Figure 9
Z80A-CPU M1 and I/O cycles
APR-03-81 13220-91097



MEMORY READ OR WRITE CYCLES WITH WAIT STATES



NON MASKABLE INTERRUPT REQUEST OPERATION

Figure 10
Z80A-CPU Memory and NMI cycles
APR-03-81 13220-91097

Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	02620-60097	1		PROCESSOR - 2624A	28480	02620-60097
C1	0160-4554	7	82	CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C2	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C3	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C4	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C5	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C6	0160-4787	8	2	CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30	28480	0160-4787
C7	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C8	0180-2879	7	2	CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C9	0160-4557	0	20	CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C10	0160-4808	4	27	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C11	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C12	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C13	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C14	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C15	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C16	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C17	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C18	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C19	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C20	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C21	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C22	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C23	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C24	0180-2879	7		CAPACITOR-FXD 22UF+50-10% 25VDC AL	28480	0180-2879
C25	0180-2881	1	3	CAPACITOR-FXD 10UF+50-10% 50VDC AL	28480	0180-2881
C26	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C27	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C28	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C29	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C30	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C31	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C32	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C33	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C34	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C35	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C36	0180-2881	1		CAPACITOR-FXD 10UF+50-10% 50VDC AL	28480	0180-2881
C37	0180-2881	1		CAPACITOR-FXD 10UF+50-10% 50VDC AL	28480	0180-2881
C38	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C39	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C40	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C41	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C42	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C43	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C44	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C45	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C46	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C47	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C48	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C49	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C50	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C51	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C52	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C53	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C54	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C55	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C56	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C57	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C58	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C59	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C60	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C61	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C62	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C63	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C64	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C65	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C66	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C67	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C68	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C69	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C70	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
C71	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C72	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C73	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C74	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C75	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C76	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C77	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C78	0160-4557	0		CAPACITOR-FXD .1UF +-20% 50VDC CER	16299	CAC04X7R104M050A
C79	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C80	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C81	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C82	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C83	0160-4801	7	2	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C84	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C85	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C86	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C87	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C88	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C89	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C90	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C91	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C92	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C93	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C94	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C95	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C96	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C97	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C98	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C99	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C100	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C101	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C102	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C103	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C104	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C105	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C106	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C107	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C108	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C109	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C110	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C111	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C112	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C113	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C114	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C115	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C116	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C117	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C118	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C119	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C120	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C121	0160-4787	8		CAPACITOR-FXD 22PF +-5% 100VDC CER 0+-30	28480	0160-4787
C122	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C123	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C124	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C125	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C126	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C127	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C128	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C129	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C130	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C131	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C132	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C133	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C134	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C135	0160-4808	4		CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C136	0160-4801	7		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C137	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
C138	0160-4554	7		CAPACITOR-FXD .01UF +-20% 50VDC CER	28480	0160-4554
CR1	1901-0050	3	8	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR2	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR3	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR4	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR5	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR7	1902-0976	4	5	DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR8	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR9	1990-0622	2	1	LED-LAMP ARRAY LUM-INT=200UCD	28480	1990-0622
CR10	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
CR11	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR12	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR13	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
CR14	1902-0976	4		DIODE-ZNR 14.5V PD=5W TC=+.088% IR=5UA	11961	1.5SE18C
J1	1251-5500	9	2	CONNECTOR 26-PIN M POST TYPE	28480	1251-5500
J2	1251-5521	4	1	CONNECTOR 9-PIN M POST TYPE	28480	1251-5521
J3	1251-5520	3	1	CONNECTOR 7-PIN M POST TYPE	28480	1251-5520
J4	1251-5499	5	1	CONNECTOR 16-PIN M POST TYPE	28480	1251-5499
J5	1251-5500	9		CONNECTOR 26-PIN M POST TYPE	28480	1251-5500
J6	1251-5828	4	1	CONNECTOR 50-PIN M POST TYPE	28480	1251-5828
Q1	1854-0019	3	2	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q2	1854-0467	5	2	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q3	1854-0019	3		TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0019
Q4	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q5	1853-0281	9	1	TRANSISTOR PNP 2N2907A SI TO-18 PD=400MW	04713	2N2907A
R1	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
R2	0698-3156	2	1	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
R3	0683-4715	0	4	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R4	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R5	0683-1025	9	7	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R6	0683-4725	2	11	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R7	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R8	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R9	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R10	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R11	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R12	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R13	0683-1035	1	4	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R14	0683-1015	7	6	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R15	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R16	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R17	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R18	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R19	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R20	0683-4705	8	2	RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R21	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R23	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R24	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R25	1810-0322	9	3	NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R26	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R27	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R28	0757-0284	7	2	RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
R29	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R30	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
R31	0757-0402	1	1	RESISTOR 110 1% .125W F TC=0+-100	24546	C4-1/8-T0-111-F
R32	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R33	1810-0322	9		NETWORK-RES 8-SIP20.0 OHM X 4	01121	408B200J
R34	0683-2205	9	1	RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
R35	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
R36	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R37	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R39	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R40	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R41	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R44	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R46	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R47	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
R49	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R50	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R51	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
U1	5081-2705	3	8	IC-RAM 16K	28480	5081-2705
U25	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U29	1820-2416	7	4	IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U32	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U34	1820-1730	6	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U35	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U37	1820-2416	7		IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U38	1820-2416	7		IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U49	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U59	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U61	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U64	1820-0693	8	4	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U78	1820-2373	5	1	IC-NAT 8367 CRT C	28480	1820-2373
U79	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U85	1820-1112	8	5	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U89	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U94	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U95	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U97	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U98	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U121	1826-0139	9	1	IC OP AMP GP DUAL 8-DIP-P PKG	3L585	CA1458G
U210	1820-2416	7		IC SHF-RGTR NMOS SERIAL-IN SERIAL-OUT	27014	MM5035P
U212	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U213	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U217	1820-0509	5	4	IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U310	1820-1677	0	2	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U311	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U313	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U314	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U317	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U412	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U413	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U414	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U418	1820-0990	8	4	IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U512	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U513	1820-1453	0	1	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U515	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U516	1813-0153	0	1	IC OSC HYBRID DUAL	34344	K1135B
U517	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U518	1820-0509	5		IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U613	1820-1450	7	1	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U615	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U616	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U617	1820-1074	1	1	IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
U618	1820-0509	5		IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U710	1820-2372	4	1	IC-VIDEO 8041A	28480	1820-2372
U711	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U712	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U713	1818-0708	1	1	IC CMOS 1024 (1K) STAT RAM 650-NS 3-S	S0545	UPD5101LC
U714	1820-2298	3	1	IC-Z80A CPU	28480	1820-2298
U715	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U716	1820-2300	8	1	IC-Z80A SIO/2	28480	1820-2300
U717	1820-0990	8		IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U718	1820-0509	5		IC DRVR DTL LINE DRVR QUAD	04713	MC1488L
U811	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U817	1820-0990	8		IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
U818	1820-0990	8		IC RCVR DTL NAND LINE QUAD	01295	SN75189AJ
W1	8159-0005	0	6	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W3	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W6	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W8	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W10	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
W13	8159-0005	0		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	8159-0005
XU29	1200-0639	8	4	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU37	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU38	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU41	1200-0607	0	16	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU42	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU43	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU44	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU45	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU46	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU47	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU48	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU51	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU52	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU53	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU54	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU55	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU56	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU57	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU58	1200-0607	0		SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0607
XU78	1200-0654	7	5	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU210	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
XU410	1200-0541	1	9	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU411	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU514	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU516	1200-0539	7	1	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XU710	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU713	1200-0612	7	1	SOCKET-IC 22-CONT DIP DIP-SLDR	28480	1200-0612
XU714	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU716	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU911	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU912	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU913	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU914	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU915	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU916	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU917	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
Y1	0410-1224	3	1	CRYSTAL- 25.7715 MHZ	28480	0410-1224
	0360-0124	3	4	CONNECTOR-SGL CONT PIN .04-IN-BSC-SZ RND	28480	0360-0124
	1200-0546	6	1	SOCKET-XTAL 2-CONT HC-25/U DIP-SLDR	28480	1200-0546
	1390-0104	3	4	FASTENER-SNAP-IN GROM PANEL THKNS	28480	1390-0104
	1390-0281	7	4	FASTENER-SNAP-IN PLGR PANEL THKNS	28480	1390-0281

MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
80545	NIPPON ELECTRIC CO	TOKYO	JP	
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
03508	GE CO SEMICONDUCTOR PROD DEPT	AUBURN	NY	13201
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
11961	SEMICON INC	BURLINGTON	MA	01803
16299	CORNING GLASS WKS COMPONENT DIV	RALEIGH	NC	27604
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
3L585	RCA CORP SOLID STATE DIV	SOMERVILLE	NJ	
34344	MOTOROLA INC	FRANKLIN PARK	IL	60131