HP 13220

Processor Module

Manual Part No. 13220-91003

REVISED

JAN-22-79

HEWLETT PACKARD

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NOTE: This document is part of the 26XX DATA TERMINAL product series Technical Information Package (HP 13220).

1.0 INTRODUCTION.

The PROCESSOR PCA performs all of the terminal logic functions. These can be divided into 3 major sections; Microprocessor Controller, Terminal Timing, and Video Control. The Microprocessor section is a complete microprocessor system within itself. It contains program ROM, scratch-pad RAM, a Keyboard interface, a Datacomm interface, and an optional Printer interface. This is where the terminal identity is formed by creative micro-programming. The Terminal Timing section generates all the necessary timing signals, and terminal states. The Video Control section fetches characters from the display memory, and displays them on the screen. Each of these three sections will be described in greater detail in section 3.0.

2.0 OPERATING PARAMETERS.

A summary of operating parameters for the Processor Module is contained in tables 1.0 through 4.0

Table 1.0 Physical Parameters

Part Number	Nomenclature	Size (L x W x D) +/-0.1 Inches	Weight (Pounds)
02620-60003	Processor PCA	12.3 x 10.9 x 0.5	1.4

Table 2.0 Reliability and Environmental Information

Environmental:	HP Class B
Restrictions:	Type tested at product level
Failure Rate:	3.71 (percent per 1000 hours)

Table 3.0 Power Supply Requirements - Measured
(At +/-5% Unless Otherwise Specified)

+16 Volt Supply	+12 Volt Supply	+5 Volt Supply	-12 Volt Supply
@ 0 mA	@ 200 mA	@ 1.5 A	@ 50 mA
NOT APPLICABLE			

115 volts ac	220 volts ac
@ A	@ A
NOT APPLICABLE	NOT APPLICABLE

Table 4.0 Connector Information

Connector and Pin No.	Signal Name	Signal Description
J1		** PRINTER **
Pin -1	CMD	Negative True, Printer Strobe
-2	PWR ON/FAIL	Negative True,Power On/Failing
-3	GND	Signal Ground
-5	FLAG	Negative True, Acknowledge Flag
-6	DATA 0	LSB - Negative True, Data
-7	DATA 1	-
-8	DATA 2	-
-9	DATA 3	-
-10	DATA 4	-
-11	DATA 5	-
-12	DATA 6	-
-13	DATA 7	MSB - Negitave True, Data
-18	+5V	Vcc Power
-19	+5V	.
-20	+5V	.
-21	+5V	.
-22	GND	Power Return
-23	GND	.
-24	GND	.
-25	GND	.
-26	GND	.

Table 4.0 Connector Information (Cont'd)

Connector and Pin No.	Signal Name	Signal Description
J2		** POWER SUPPLY **
Pin -1	+5V	+5V Power
-2		N/C
-3	+5V	+5V Power
-4	+12V	+12V Power
-5	GND	Return for Power
-6	GND	Return for Power

-7	PWR ON/FAIL	Negative True, Power On/Failing
-8	-12V	-12V Power
-9	BATTERY	Positive Battery Terminal
-10	BATRET	Negative Battery Terminal
J3		** SWEEP **

Pin -1	HLFBRT	Negative true, Half Bright Video
-2		N/C
-3	RETURN	Return for half bright twisted pair

-4	FULLBRT	Negative true, Full Bright Video
-5	RETURN	Return for Video twisted pair
-6	RETURN	Return for Drive signals

-7	VERDR	Negative True, Vertical Drive
-8	HORDR	Horizontal Drive
J4		** KEYBOARD **
Pin -1	KEYA0	Key Data (LSB)
-2	KEYA1	Key Data
-3	KEYA2	Key Data
-4	KEYA3	Key Data
-5	KEYA4	Key Data
-6		N/C
-7	KEYA5	Key Data
-8	KEYA6	Key Data (MSB)

-9	KEYACT	Key Active (Status of key selected)
-10	GND	Power Return
-11	BELL	Bell Line
-12	+5v	+5v Power

Table 4.0 Connector Information (Cont'd)

Connector and pin No.	Signal Name	Signal Description
J5		** DATA COMM **
Pin -1	EXCLK	Times 16 External TTL clock in
-2	+5V	+5V Pod Power
-3	+5V	+5V Pod Power
-4	GND	Power Return
-5	GND	Power Return
-6	GND	Power Return
-7	CH	Rate Select (23)
-8		N/C
-9	BB	Received Data (3)
-10		N/C
-11	CB	Clear To Send (5)
-12	CC	Data Set Ready (6)
-13	CF	Data Carrier Detect (8)
-14	SCF	Secondary Data Carrier Detect (12)
-15	AB	Signal Ground (7)
-16	8XCLKO	Times 8 TTL Level Clock Out
-17	16XCLKO	Times 16 TTL Level Clock Out
-18	CE	Ring Indicator (22)
-19	+12V	+12V Pod Power
-20	-12V	-12V Pod Power
-21	BA	Transmitted Data (2)
-22	CA	Request To Send (4)
-23	CD	Ready (20)
-24	SCA	Secondary Request To Send (19)
-25		N/C
-26		N/C
-27		N/C
-28		N/C
-29		N/C
-30		N/C
-31		N/C
-32	GND	Return
-33	AA	Shield Ground (1)
-34		N/C

Notes: (n) denotes the RS-232 pin number

3.0 FUNCTIONAL DESCRIPTION. Refer to the block diagram (figure 1), schematic diagrams (figures 2-4), timing diagrams (figures 5-9), component location diagram (figure 10), and parts list (02620-60003) located in the appendix.

INTRODUCTION. The Processor module is logically divided into 3 sections; the Microprocessor Controller, Terminal Timing, and the Video Control Circuitry. These three circuits will be dicussed in sections 3.1, 3.2, and 3.3 respectively.

3.1 MICROPROCESSOR CONTROLLER.

Refer to the schematic diagram (figure 2) and timing diagram (figure 5) located in the appendix. The microprocessor controller consists of the Z80 Microprocessor, devices that connect directly to the processor bus, and their associated support devices.

3.1.1 Z80 PROCESSOR.

The Z80 is the main terminal processor. It opperates with a 1.8432MHz clock, resulting in 5.43ns cycle time. The address space is decoded in 8K byte increments by (U77), and is allocated as follows:

ADDRESS RANGE	DEVICE
0000-1FFF	First Program Rom (U79)
2000-3FFF	Second Program Rom (U701)
4000-7FFF	available
8000-9FFF	CMOS scratch pad memory (256 bytes)
A000-DFFF	Display Memory (4k bytes used)
E000-FFFF	available

The Z80's I/O addresses are impartially decoded by the most significant 5 I/O address bits (A7-A3), with A2-A0 allowing for 8 registers within each I/O device. The I/O addresses are allocated as follows:

I/O ADDRESS	DEVICE
98 & 99	Datacomm Interface
58 & 59	Keyboard Interface
38 & 3A	Printer Interface
10-17/08-0F	available

The $\overline{WAIT}$ line is used to synchronize the Z80 with the hardware display memory accesses (DMAs). If the Z80 attempts a display memory oopperation while tne Video Control is fetching characters for display refresh, WAIT becomes active, which automatically hangs the current Z80 instruction until tne DMA is done. This makes the display memory lockouts transparent to the Z80 software, but may insert up to a 30us delay in each display memory access.

3.1.2 PROGRAM ROMS.

The two Program ROM sockets will accept either 2, 4, or 8k-byte parts. Address lines A0-A11 are supplied directly to the ROMs, while ROM address A12 (pin 21) may be conected to either address A12 or +5 volts. This option allows 27XX EPPOMs to be used if w2 & w4 are installed. All other ROMs should have w1 & W3 installed.

The ROM addressed at location 0000 (ROM0K) may be disabled by a external source by connecting +5V to U201.4. This feature allows in-nouse testing to use a special diagnostic ROM.

3.1.3 BATTERY BACKED-UP CMOS RAM.

The CMOS RAMs (U69 & U601) provide the Z80 with 256 bytes of fast RAM (tnere are no DMA lockouts). These RAMs are battery backed-up to retain the terminal configuration while the terminal is unpowered.

Tne 2621 uses a 4.2V mercury or 3.8V lithium battery for back-up power. The terminals +5V and the battery are diode isolated to insure battery usage only when the terminal is unpowered. The battery return (BATRET) is grounded thru a 1K ohm resistor to enable tne measurement of the battery current. The battery specifications are as follows:

Battery limits, power on or off	Min	Max
Voltage (measured at U59.14)	2.0V	5.5V
Current (voltage across R4)	-0.02V	0.0V

3.1.4 KEYBOARD INTERFACE.

The keyboard interface is controlled by a 8041 slave microprocessor, which in addition to scanning the keyboard, rings the bell and operates as a general purpose Z80 I/O port. The keyboard processor scans the entire keyboard every 24ms, and only reports ASCII or control key changes to the Z80. The external latch (U404), and the lower 5 bits of PORT2, are directly accessable by the Z80 with 3 keyboard commands (see Keyboard chip interface specifications). The 8 bit latch is writable only, while the 5 bits of PORT2 are bi-directional. These 13 I/O lines are used as hardware straps (BAUD rate select, 50/60 Hz select, simple datacomm enabled, display blanking), and to handle the datacomm lines not handled directly by the datacomm chip. A final input, T1, is used to detect a vertical retrace. This allows the Z80 to obtain retrace or 200ms timer interrupts for software timing applications.

PORT1 of the 8041 is used for keyboard control. The lower 7 bits are the inverted key address. These lines are buffered by U505 and U504.12 to provide additional drive. The state of the addressed key is returned as $\overline{\text{KEYACT}}$, and is buffered by U703.8. The remaining bit in PORT2, P17, is used to drive the bell, and is clocked under software control. U203.12 and Q4 are used to buffer this signal to directly drive an 8-ohm speaker. The 6.8uF capacitor de-squares the output waveform, resulting in a purer sounding bell tone.

The 8041 is clocked by DPC2 (5.727MHz), resulting in a machine cycle time of 2.62us. The inverters in U503, and pull-up resistors R33 and R34 provide the Intel recommended TTL drive circuitry.

3.1.5 DATACOMM INTERFACE.

The terminal Data Communications are centered around the M6850 ACIA (Asyncronous Communications Interface Adaptor). This chip performs the serial to parallel data conversion for RS-232 data transmission, as well as detecting parity, framing, and overrun errors. In addition, the signals RTS, CTS, and DCD are handled by the 6850. The remaining datacomm signals necessary for RS-232C transmissions are controlled by the 8041's I/O ports.

Buffers U602, U603, U702 & U703 provide the necessary level conversions for RS-232C data tranmissions. The 470pF capacitors used on each driver and receiver are used for slew rate control, and allow the datacomm lines to be driven up to 19.2K BAUD.

3.1.6 BAUD RATE GENERATION.

The 11 supported BAUD rates are derived directly from the 25.7715MHz system clock. Counters U24 & U31 divide this signal by 14 to generate a 1.8432MHZ clock. This frequecy is used as the Z80 clock, and divided down for the BAUD rate generation. The BAUD rate generation circuitry is best described by the overall function. From the 4 rate selects (RATE3, RATE2, RATE1, & RATE0), and the 1.8432MHz clock, 16 frequencies are generated. With a given rate selected, the counters U402, U403, and half of U49 form a free running divider chain. The demultiplexer, U401, selects one of these frequencies to be used as the BAUD rate base (BCLK), which is 16 times the bit rate. BCLK is used to clock the ACIA, and is again divided by U49.9 to provide a times-8 clock. Both the 8x and 16x clocks are buffered by U68, and provided on the Datacomm connector for external use. The following table describes the function of the BAUD rate counters:

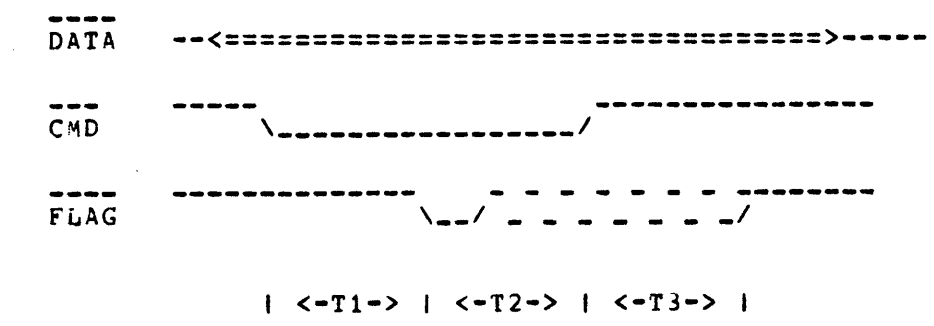
RATE VALUE	BAUD RATE	BCLK (Hz)	BCLK (uS)	U403 DIVISOR	U402 DIVISOR	BAUDRATE % ERROR
0	110	1743	574.	12	11	-.97
1	200	3196	313.	12	12	-.13
2		6973	143.	12	11	
3		12783	78.2	12	12	
4		14381	69.5	16	16	
5	1800	28763	34.8	16	16	-.13
6	3600	57526	17.4	16	16	-.13
7	EXT	0	0	16	16	
8	150	2397	417.	6	16	-.13
9	300	4794	209.	6	16	-.13
A	600	9588	104.	6	16	-.13
B	1200	19175	52.2	6	16	-.13
C	2400	38350	26.1	6	16	-.13
D	4800	76701	13.0	6	16	-.13
E	9600	153402	6.52	6	16	-.13
F	EXT	0	0	6	16	

Notes:

1) RATE_VALUE = RATE3*8 + RATE2*4 + RATE1*2 + RATE0*1
2) The divisors are the amount that the counters divide by.
3) The % error does not include the crystal error.
4) An external input is used instead of 19.2K BAUD

3.1.7 PRINTER INTERFACE.

The printer interface is controlled by the I/O ports of an 8041 processor. PORT2 is used for the printer data, and buffered by 74LS38's for extended drive. PORT1 is used for printer control, along with providing the Z80 with free use of the unused I/O pins (P10-P14, & T0). This 8041 (U75) uses the LC network of C45, C46 & L1 for the basic clock. This should result in a clock rate of 4 to 6 MHz. The SYNC output (U75.11) should be in the range of 2.5 to 3.75uS.
The printer interface may be characterized by the following timing diagram:



Printer Acknowledge: 0 < T1 < 15 Sec

Terminal Acknowledge: 0 < T2 < 20 Us

Printer Done: 0 < T3 < 1 Sec

* Note: The combined time of T2+T3 need only be greater than 1 Us.

3.2 TERMINAL TIMING.

FUNCTIONAL DISCRIPTION. Refer to block diagram (figure 1), schematic diagram (figure 3), and timing diagrams (figures 6-9) located in the appendix.

3.2.1 SYSTEM CLOCK.

All terminal clocks are derived from the 25.7715MHz system clock. A clock disable is provided to allow an external source to disable the system clock, and insert a slower clock rate.

The Hybrid crystal oscillator, U40, generates a 25.7715 MHz TTL level clock. In normal operation, $\overline{\text{OSCDSBL}}$ and EXTCLK will have no external connections, and are pulled high. In this fashion, U22.6 and U22.3 will simple act as buffers. To use a slower clock rate for testing, $\overline{\text{OSCDSBL}}$ must be pulled low, and then the external clock supplied to U22.2 (EXTCLK).

3.2.2 DOT POSITION COUNTER.

The dot position counter defines the width of a character, and generates timing signals needed on a character basis for the video display hardware. DMARAS is used to generate dynamic memory timing signals (RAS & CAS) for each byte fetched by the hardware. DPC8 and DPLD are used for character control timing. DPC8 is used to edge clock character data, and DPLD is used as a synchronous load enable, also for character data.

U32 counts from 6 thru 14, for a basic divide-by-9 function. DPLD-(U23.6) detects the count of 14, and is used to syncronously reset the dot position counter, and to load dot data into the video shift register. DPC8 (U50.8 & U32.11) provide a character data clock, and is used throughout the board to clock character data.

3.2.3 CHARACTER POSITION COUNTER.

The character position counter divides a CRT raster into 115 character positions. The first 80 characters are displayed on the screen, while the remaining 35 character times are used for horizonal retrace. The signal HBLANK defines these two times. HDRIVE is the horizontal sync pulse required by the sweep PCA. This same signal is used to syncronize the switching power supply to the horizontal sweep rate.

The position counter is made up of U33, U34, and the gating of U22.8 and U23.8. The counters are preset to 80 (hex) by CP114 (U23.8), and go through 115 sequential counts before being syncronously preset to a 80 again. HDRIVE is generated by U24, and is active during CP65-CP72. A transistor (Q1) is used to provide an open collector drive signal for the power supply. CPWAIT is started on CP84 and is active for 24 character times. It starts 4 character times after the last display memory fetch (CP80), and quits 6 character times (CP107) before the first display memory fetch (CP114). This insures that Processor and Video Controller display memory access are mutually exclusive. CPWAIT, along with DMAROW, define whether the Z80 or the Video Controller has access to display memory. When DMAROW is false, the Z80 has unrestricted access to display memory. If DMAROW is true, the Z80 will insert wait states in its display memory operations until CPWAIT is false. CPWAIT is also used to clock the Character Height & Row counters during horizonal retrace.

3.2.4 CHARACTER HEIGHT AND ROW COUNTERS.

The character height counter is a pseudo divide-by-15, to account for the 15 raster lines per character cell. The character row counter provides the 26 character rows, and the extra scan lines for vertical retrace. Figure 5 shows the relation of these signals during the frame. To allow the hardware to refresh the CRT at 50 or 60Hz, extra scan lines are added for 50Hz refresh instead of changing the horizonal sweep frequency. This results in 415 scan lines for 60Hz, and 498 scan lines for 50Hz. A final constrant in the raster control circuitry is imposed by the AC vertical centering employed by the sweep PCA. To perform these functions, the following 4 states are generated per frame:

a) SSL - Starting Scan Lines
   Six Scan lines are used after vertical retrace to stablize the display. This is caused by VLOAD- loading a -6 (9H) into the CHARACTER HEIGHT COUNTER, and a -1 (7FH) into the CHARACTER ROW COUNTER at the end of Vertical Retrace.

b) VIDEO - Video display
   The Character field is formed by 26 character rows of 15 scan lines each, resulting in 390 scan lines.

c) ELS - Extra Scan Lines
   For 50Hz CRT refresh, 38 extra scans are added before vertical retrace. None are added for 60Hz refresh.

d) VR - Verticle Retrace
Vertical retrace period; 19 scans for 60Hz, or 64 scans for 50Hz opperation.

3.2.5 DMA ROW DECODE.

The Z80 processor is able to complete a display memory access only when the Video Controller relinquishes its control. CPWAIT (~8uS), which always occurs during horizonal retrace is one such period. The other period is during an entire character row (~40uS), when the scan is not refreshing the CRT display or performing a dynamic memory refresh. This is decoded by the signal DMAROW. ("DMA" represents Display Memory Access by the video generation hardware). Those rows in which DMA takes place are the following (for 4K memory parts):

a) During SSL, all rows are used for DMA. This enables the Hardware to fetch the Top_Of_Screen pointer.

b) During the first 25 video display rows (CR0-CR24), 13 raster scans (CH2-CH14) are used for character refresh. The other two are decoded as CHBLANK- (CH1 & CH15), which blanks the screen, and allows the processor to have unrestricted access to display memory. If CR- is active, which will blank the display, the video display hardware will only use CH12 for Dynamic Ram refresh, and allows the processor unrestricted access to the other 14 rows.

c) During CR25, which is the Soft Key row, all 15 raster scans are used for character generation. This is required to generate the inverse video.

d) During ESL and Vertical Retrace (CRG25), only CH12 is used to refresh the dynamic memories. The remaining 14 rows are given up for unrestricted processor access.

If it is desired to use 16K memory chips instead of the current 4K devices, part "a" above will change to the DMA requiring CH15 for all character rows. This will cause a significant reduction in processor access to display memory, and is not a supported feature.

3.3 VIDEO CONTROLLER.

FUNCTIONAL DISCRIPTION. Refer to the block diagram (figure 1), and schematic diagram (figure 4).

The Video Contoller circuitry fetchs the ASCII characters from display memory, and alonq with the basic terminal timinq signals, converts them into a serial video dot stream.

3.3.1 DISPLAY MEMORY STRUCTURE.

The Display Memory is divided into 3 sections, Window Pointers, Row Pointers, and Character data.

3.3.2 WINDOW POINTERS - The Top_Of_Screen pointer is located at A080. The value at this location points to the first Row Pointer. This Row Pointer, as well as the next 23 Row Pointers are used to sequentially refresh the CRT. The Soft_Key_Label pointer is located at A081. This is a Row Pointer pointing to the data to be displayed during the 26th character row (CR25).

3.3.3 ROW POINTERS - The first 64 bytes of display memory (A000-A03F) are Row Pointers, and are used to index the character rows. These 8 bit values form the most Significant 8 bits of the display address of the first character of a display character row. The remaining 4 address bits are zeroed. This allows the Row Pointer to point to any one of the 256 links in display memory, a link being 16 consecutive bytes.

3.3.4 CHARACTER DATA - The remaining portion of display memory is used to store Z80 variables or characters. Each character row is required to start at the link beginning, and each row uses 80 consecutive memory locations.

3.3.5 CHARACTER POINTER.

The Character Pointer is a 12-bit register containing the address of the next character to be displayed. During CP114, which is the last character time before the 80 displayed characers are fetched, the Character Pointer is loaded with the Row Pointer addressed by the Index Pointer. Since display memory is only 8 bits wide, the least significant 4 bits are always zeroed. This results in the character pointer being able to point to any one of the 256 links in display memory. This is the address of the first character to be displayed. The next 80 bytes are then fetched from display memory, with the Character Pointer being incremented after each read.

3.3.6 ROW INDEX.

The Row Index is a 6 bit register which contains the address of the row pointer currently being used to index the displayed character row. During SSL (before the frame starts), the Row Index is initialized with the Top_Of_Screen Pointer, which is read from location A080. The Top_Of_Screen Pointer points to the first Row pointer to be used. This register is incremented after each character row is finished, resulting in 24 consecutive row pointers to be used to refresh the CRT display. With only this 6-bit address, location A000 automatically follows A03F, resulting in automatically hardware wrap-around. For the Soft Key labels (26th row), the Row Index is set to address location A081, which is then used as the row pointer for that row.

3.3.7 DISPLAY MEMORY ADDRESS MULTIPLEXER.

The Display Memory is addressed from three sources; the Z80, the Character Pointer, and the Row Index. These three addresses, as well as the row/column address multiplexing, are controlled by the Display Memory Address Multiplexer (U51-U56). During a non-DMA raster scan, or during part of horizontal retrace (CPWAIT), the Z80 address is selected. Only during a DMA row are the two pointers enabled. The character pointer is active during HBLANK (CP0-CP79), and the Row Index is active during CP114. The Row/Column multiplexing is controlled by the Display Memory Timing, and is the same for all three sources.

3.3.8 DISPLAY MEMORY TIMING.

The display memory timing generates the appropiate timing signals for the dynamic RAM's. A memory cycle begins with either the DMA or the Z80 requesting a Display memory cycle. A DMA cycle is requested by DMA, with DMARAS used as the timing signal. DMA will always fetch 81 consecutive bytes provided CR is not activated. When the Z80 cycle addresses the display memory, VDA goes high. When MEMGO is also high, which is when the Video Controller allows Z80 memory access, the memory cycle Flop is clocked on the rising edge of PHI. This generates MEMCYCLE, and begins the RAS/CAS shift register. Once the Z80 has begun a cycle, it will be finished, even if the CPWAIT becomes active. This is why CPWAIT begins 6 character times (2.1uS) before a DMA fetch occurs. ascyncronous request, RAMCYCLE will go high. This signal is clocked through the delay shift register U30, yeilding a 38.8 ns delay for each output tap. This timing generates RAS, Row/Column address select, and CAS signals. The RAS and CAS signals, along with the Write signal are buffered by U50, a 74S37. All control and address lines are damped with 82-ohm resistors.

3.3.9 DISPLAY MEMORY.

The Display Memory consists of 4K bytes of memory, using standard 320ns cycle time, 16 pin dynamic memories.

3.3.10 VBB POWER SUPPLY.

The Vbb power supply generates the necessary -5 volt bias for the dynamic RAMs from the -12 volt supply.

The resistor-divider R45/R46 generates a -5 volt reference from the -12 volt supply. The resistor-divider was chosen to allow an external tester to vary the RAM supply voltages by simple varying the main power supply voltages. U70 is a M1458 operational Amplifier, used to buffer Vbb, with CR5 insuring that the Vbb supply never exceeds Vdd.

3.3.11 VIDEO BLANKING.

The video blanking circuitry generates screen blanking from the terminal timing and control signals. The screen is blanked during the following times:

a) During VBLANK. This is during all character rows except the 26 displayed rows, CR0-CR25

b) During CR24. This is the demarcation line between the 24 row display, and the Soft_Key labels.

c) During HBLANK+2. Since the characters are delayed by two character times (Display memory fetch, and the character ROM look-up time), this signal is run through to character delay latches (U37), before becoming part of the blanking. This blanking represents the horizontal retrace.

d) During ZBLANK. This signal is Z80 controlled, and allows the entire display to be blanked under program control.

e) During CHBLANK. This is CH1 and CH15 of the first 24 character rows. These are always blank for a standard character set (which is all that the 2621 is designed to support), so these scans are externally blanked to give the Z80 more access to the Dynamic memories.

f) During CR time. When a carriage return is detected in display memory, CR indicates this signal on a character boundary. This will blank the carriage return, as well as the rest of the row. Optionally, CR may be generated by ZBLANK, depending on the input to U204.3 (In either case, CR will give the Z80 more access time to display memory).

$\overline{\text{BLANK}}$ is the logical "OR" of the above signals, and used to disable the video drive signals, $\overline{\text{FULLBRT}}$ and $\overline{\text{HLFBRT}}$.

3.3.12 VIDEO CHARACTER GENERATION.

CHARACTER FONT - The basic character cell is a 9-dot by 15-scan line rectangle. Within this cell is the 7 x 9 character, surrounded by one dot on either side for horizontal spacing, four scan lines below for lower case character desenders, and one scan line above and below for row-to-row spacing. The appearance of the characters is enhanced by means of a half-shift capability, which generates smoother angles and curves by using extra bits in the character ROM. Each character scan line segment is stored in ROM as an 8-bit word. Seven of the bits (D1-D7) are used for the character dots, and the eighth (D0) is used to specify Half-shifting of the dot data. If a character scan is half-shifted, the data is delayed by half a clock cycle, or shifted to the right on the screen. This increases the effective character resolution to 13-dots x 13-scans; seven unshifted dot positions, and six interstitial positions.

3.3.13 CHARACTER LATCH - Since the character time of 349ns is faster than the combined display memory access time and character ROM access time, this latch is used to hold the display memory data while addressing the Character ROM.

3.3.14 CHARACTER ROM - This ROM uses the ASCII Character data, and the character scan height to generate the dot images. Bit 01 is used to specify half-shifting of the particular character height.

3.3.15 SERIAL-TO-PARALLEL-CONVERSION - During dot position 8, the video bits are loaded into the parallel-to-serial converting shift registers, U302 & U303. To perform the halfshifting of the video dots, both the normal and half-shifted dots are present at all times. The normal data is at U303.11. This data is then clocked on the opposite clock edge in U204.9, resulting in the half shifted data. The Half-shift select from the character ROM is saved in U37, and used to select the appropriate video bits by the multiplexer function of U102.

3.3.16 VIDEO STREAM - The eighth bit of display memory is used as a display enhancement. During character row 25 (soft key label row), it is used to select inverse-half-bright video. For the other rows, it is used as an underline (or cursor), and turns on all dots during character height 12. The final video dots are stretched by Q2 to form a more pleasing character.

4.0 GLOSSARY OF SIGNAL NAMES

60Hz	Selects a 50Hz or 60Hz frame refresh
An	Z80 address lines (A0-A15, A15 is the MSA)
BATTERY	& BATTERRET - Battery connections
BCLK	BAUD rate clock (16 times the bit rate)
BELL	Speaker drive signal
BLANK	Video blanking signal
CAS	Dynamic memory Column Address Strobe
CHn	Character Height raster count (1-15)
CH1	Top raster scan of a character row
CH12	Cursor position in a character row, and used for display memory refresh
CH15	Bottom raster line of a character row Optionally used to refresh 16k memory chips
CHBLANK	Blanks CH1 & CH15 of the first 25 character rows DMA is inhibited during this time to increase the Z80 display memory access time
CHCn	Character Height Counter binary output
CP114	Last character raster position Used to reset the Character Position Counter, and to set up the Character Pointer before each scan
CPCn	Character Position Counter binary output
CPWAIT	Character Position wait positions This signal defines the character positions needed to refresh the display, and provides a hold-off so Z80 and DMA memory cycles are mutually exclusive
CR	This processor controlled signal blanks the screen at the next character, and inhibits the DMA during all raster scans except CH12, which is used for Dynamic Memory refresh
CR24	Blanking signal for character row 24
CR25	Character Row 25 The Soft key row
CRCn	Character Row Counter binary output
CRB	Carriage Return Blanking This signal detects a carriage return in display memory, to allow the rest of the line to be blanked, if enabled
CRG25	Character Row Greater Than 25 Active during all scans after the 26 valid video character rows
CS	Dynamic memory chip select for 4k parts, or the seventh address line for 16k parts
CURPOS	Cursor position This will display the cursor or underline during CH12

DDRAM	Disable Dynamic Rams Test point to disable the dynamic RAM outputs for testing
DISPMEM	Display memory access Active whenever the DMA must read characters from display memory to refresn the RAMs or display characters
DMA	Display Memory Access requested by the Video Controller
DMARAS	Master dynamic memory timing signal Gated with an enable signal to begin all DMA RAM timing
DMAROW	A row required by the DMA for screen or memory refresh
DPCn	Dot Position Counter binary output
DPC2	Used as the 8041 clock
DPC8	Edge to clock characters about the hardware
DPLD	Last dot time in a character, used for synchronized character loading
Dn	Z80 data bus (D0-D7, D7 is the MSB)
EXTCLK	External system clock input Used for testing only
FULLBRT	Full bright video data
HALFSHFT	Specifies half shifted dot data for this character
HLFBRT	Half bright video data, used for inverse characters only
HB+1	Horizontal blanking signal delayed by 1 character time
HBLANK	Horizontal blanking signal Due to the memory access time and the character ROM access time, this signal must be delayed by 2 character times before real blanking can occur
HDRIVE	Horizontal drive signal for sweep board Also used to sync the power supply with the horizontal scan rate
INT	Z80 interrupt maskable line
IO	Signifies a Z80 I/O request opperation
IOREQ	Z80 I/O request or INTERRUPT ACK cycle
KEYACT	Key Active, status of selected key
KEYn	Key address (KEY0-KEY7, KEY7 is MSA)
Ln	Character ROM ASCII data
M1	Z80 instruction fetch cycle
MEMGO	Time when Z80 has access to the display memory
MMn	Damped memory address line
MUXA	Selects the Top_Of_Screen pointer
MUXB	Selects Character pointer
MUXC	Dynamic memory Row/Column address select
Mn	Multiplexed dynamic memory address
NMI	Non maskable interrupt line
NONROW	Used to fetch the 26th line Causes the Top_Of_Screen pointer to be read from display memory address SA081
PWRONFAIL	Power on reset signal, and power fail indicator

PHI	Z80 clock
OSCDSBL	Disables internal 257715 MHz oscillator, and enables the external clock
RAS	Dynamic memory row address strobe
RATEn	BAUD rate select binary value
RD	Z80 read request
RESET	Hardware reset
RFSH	Indicates a Z80 memory refresh cycle
RFSH16K	Used to refresh the upper or lower half of 16k memory chips
RP128	Enables the upper 8k of display memory if 16k parts are used
RPCLR	Row pointer clear
RPEN	Row pointer enable
RPLD	Row pointer load
RST	Flip-Flop reset Allows an external tester to get all flops in a know state
RSTLCH	Reset latch, insures that the carriage return detect circuitry is reset at the start of each line, and disables the cursor during horizonal retrace
SIMPLEDC	Simple Datacomm Disables the CTS & DCD inputs on the M6850 Required for simple 3-wire Datacomm
SYSCLK	System clock, 257715 MHz, or the external clock applied to EXTCLK
VBLANK	Vertical Blanking, Blanks the display on a line by line basis
VDA	Valid Display Address Active when the Z80 is addressing the display memory
VDRIVE	Vertical Drive to the sweep PCA
VLOAD	Vertical load Presets the vertical timing counters
WAIT	Z80 wait input Used to hold off the Z80 during display memory access if the DMA is active
WD	Z80 write data request
WE	Write enable to dynamic RAMs
ZBLANK	Z80 Blanking, bit set by the Z80 to blank the display, and get more display memory processing time

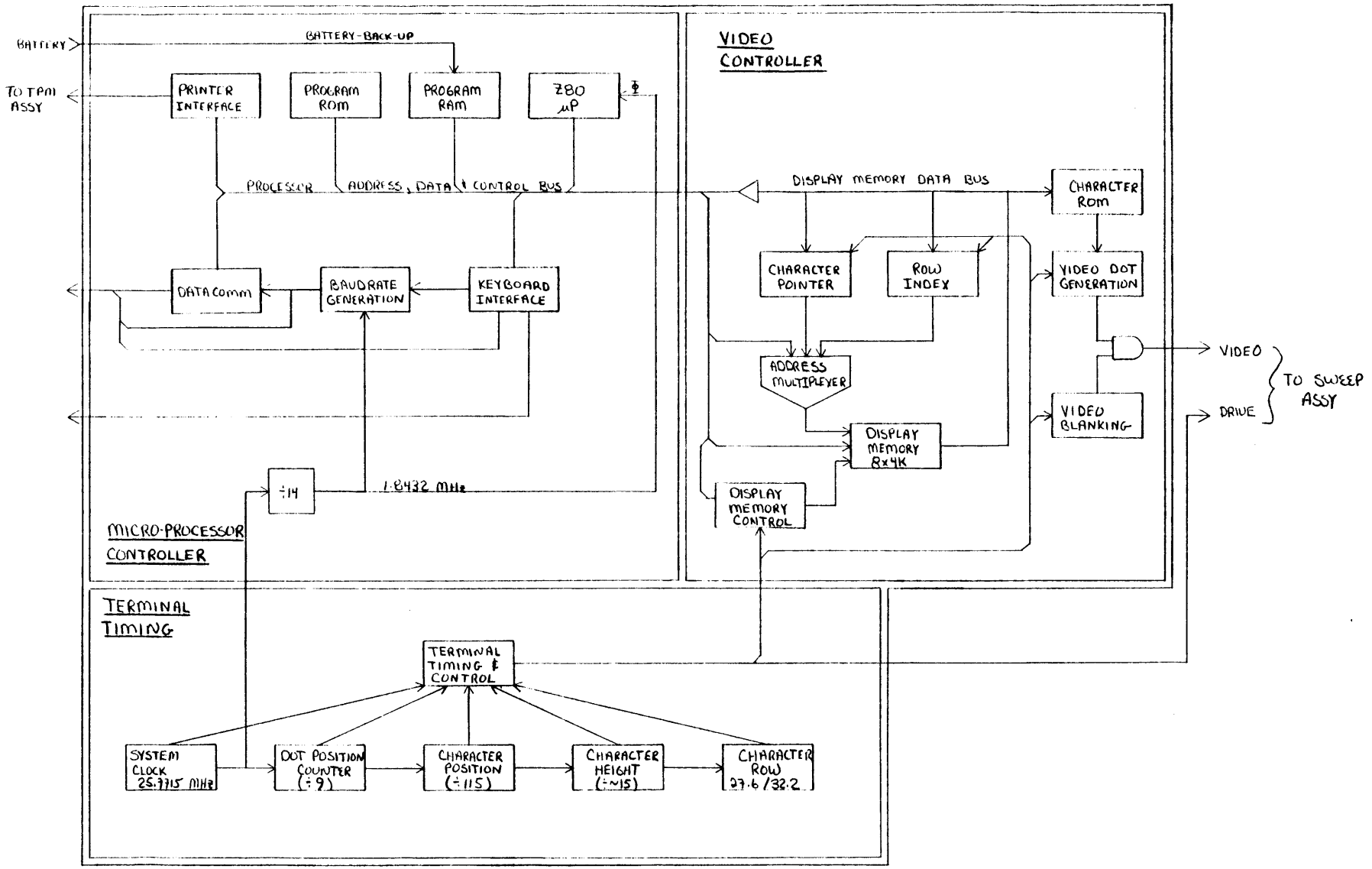


Figure 1
Processor Module Block Diagram
JAN-22-79 13220-91003

MICROPROCESSOR CONTROLLER

POWER SUPPLY

PROCESSOR, RAM, ROM

PRINTER INTERFACE

BAUD RATE GENERATION

DATA COMM

SPARES

NOTES:
1) No R20, R21, R35
2) Conn J7 for test only
3) SIGNALS: RD, WD, Φ and GRG25 ON WRONG SIDE OF SCHEMATIC
4) U504 = 74LS05 ; U505 = 74LS04

Figure 2
Processor PCA Schematic
Microprocessor Controller
JAN-22-79 13220-91003

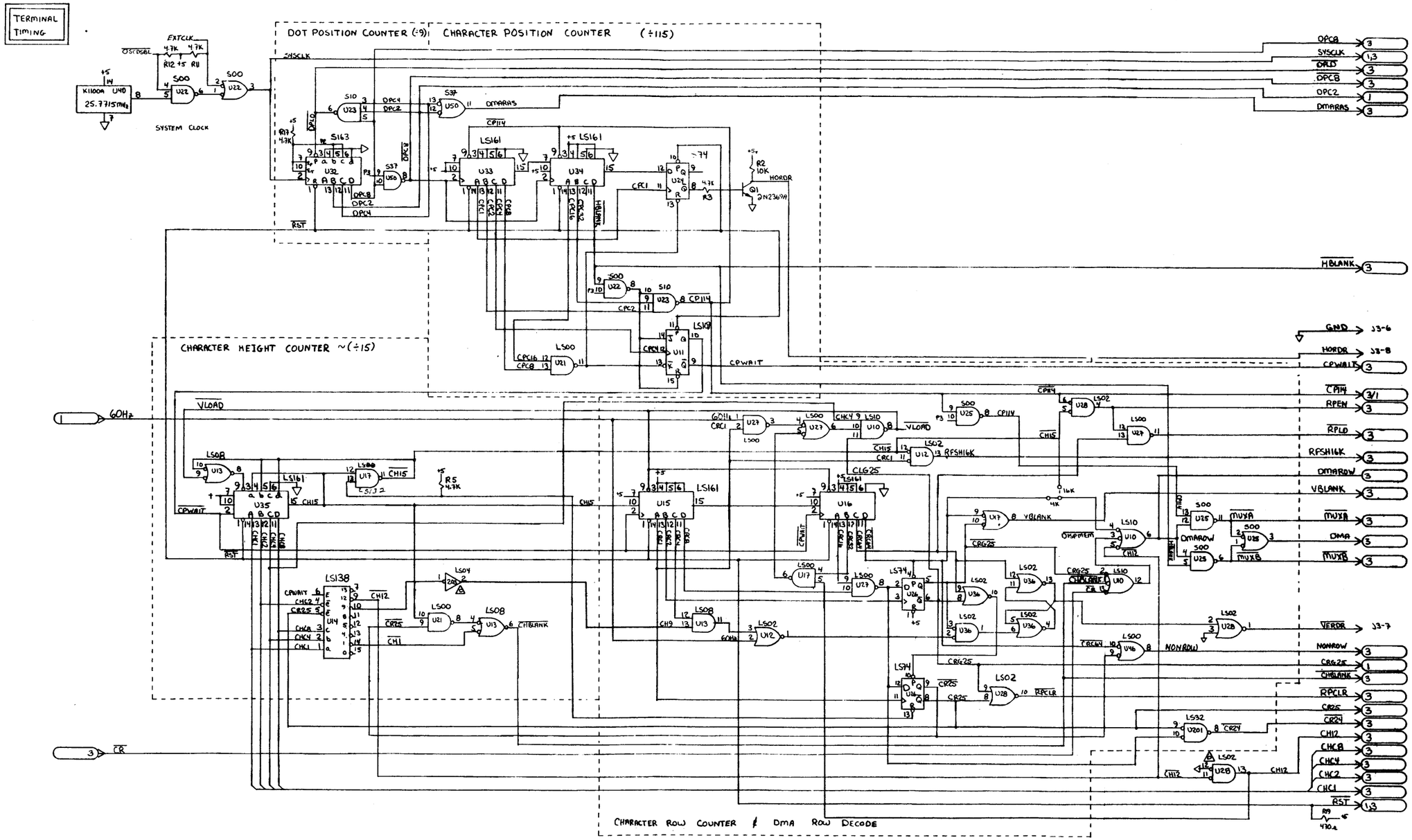


Figure 3
Processor PCA Schematic
Terminal Timing
JAN-22-79 13220-91003

VIDEO CONTROLLER

CHARACTER LATCH

VIDEO CHARACTER GENERATION

CHARACTER POINTER

ROW INDEX

DISPLAY MEMORY ADDRESS MULTIPLEXER

DISPLAY MEMORY TIMING

VIDEO BLANKING

DOT STRETCH

NORMAL DOTS

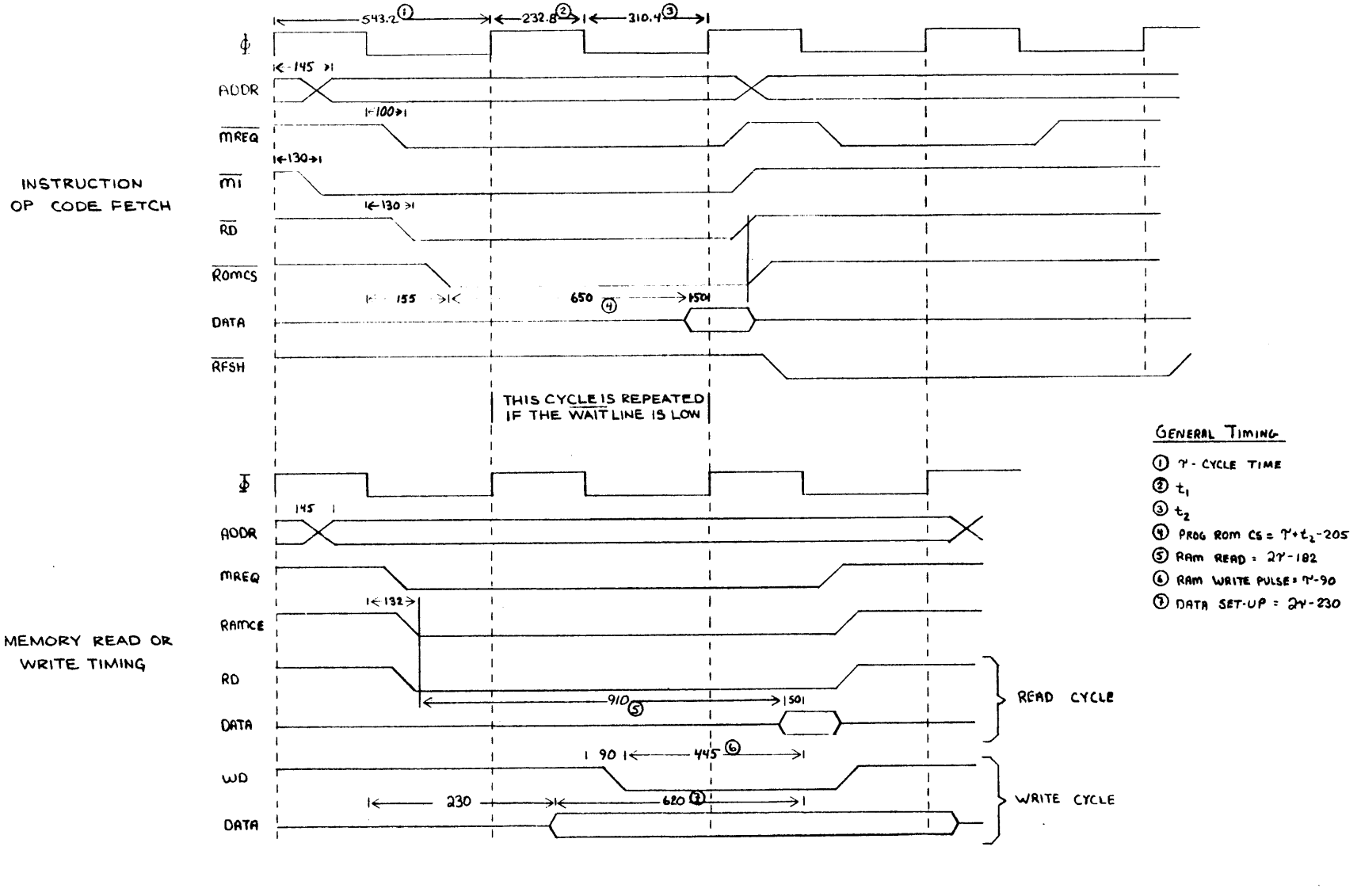
HALF-SHIFTED DOTS

DISPLAY MEMORY

NOT LOADED

Figure 4
Processor PCA Schematic
Video Controller
JAN-22-79 13220-91003

Z80 TIMING



NOTE: ALL TIMES IN NANOSECONDS

Figure 5
Z80 Timing
JAN-22-79 13220-91003

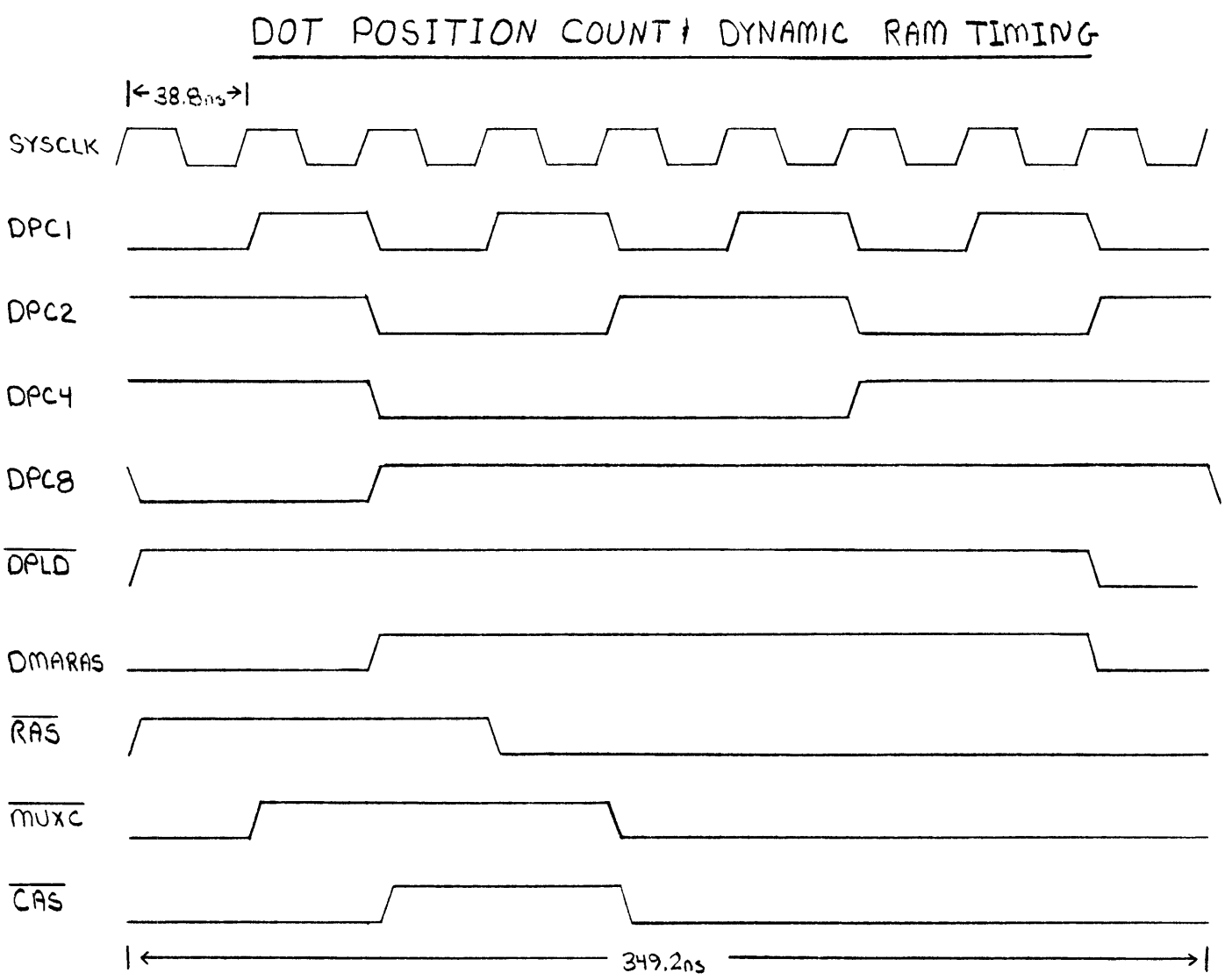


Figure 6
Dot Position Count & Dynamic Ram Timing
JAN-22-79 13220-91003

CHARACTER POSITION COUNT TIMING

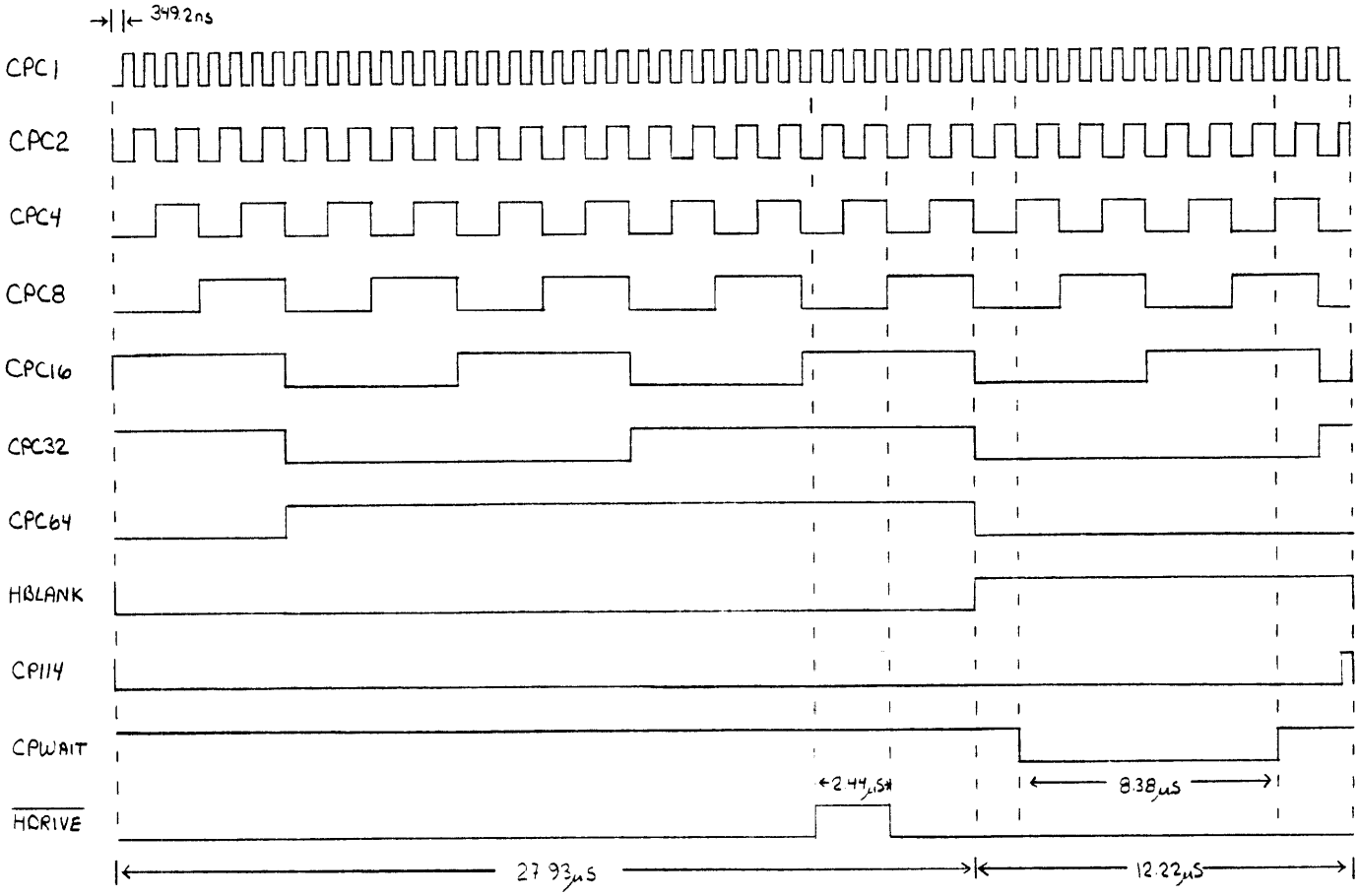


Figure 7
Character Position Count Timing
JAN-22-79 13220-91003

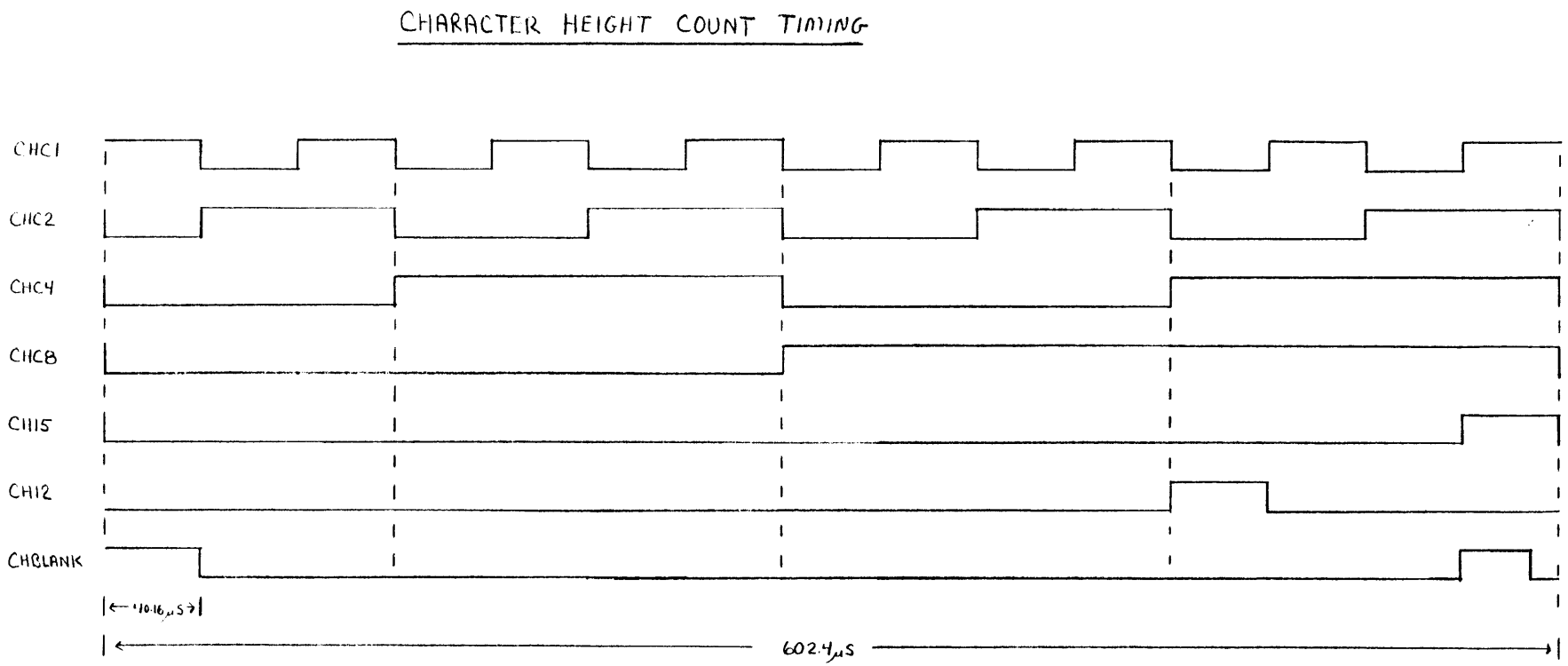


Figure 8
Character Height Count Timing
JAN-22-79 13220-91003

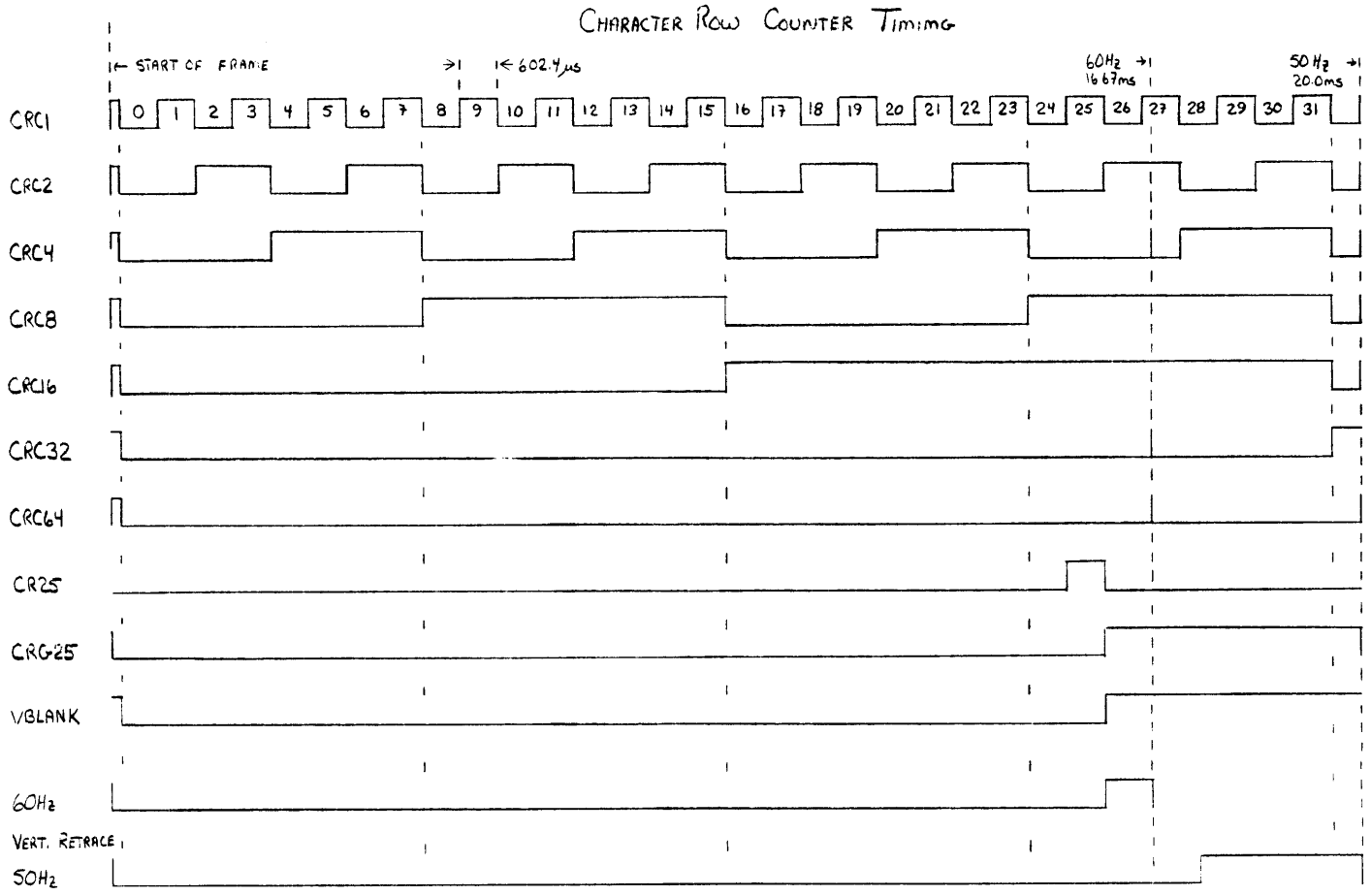


Figure 9
Character Row Counter Timing
JAN-22-79 13220-91003

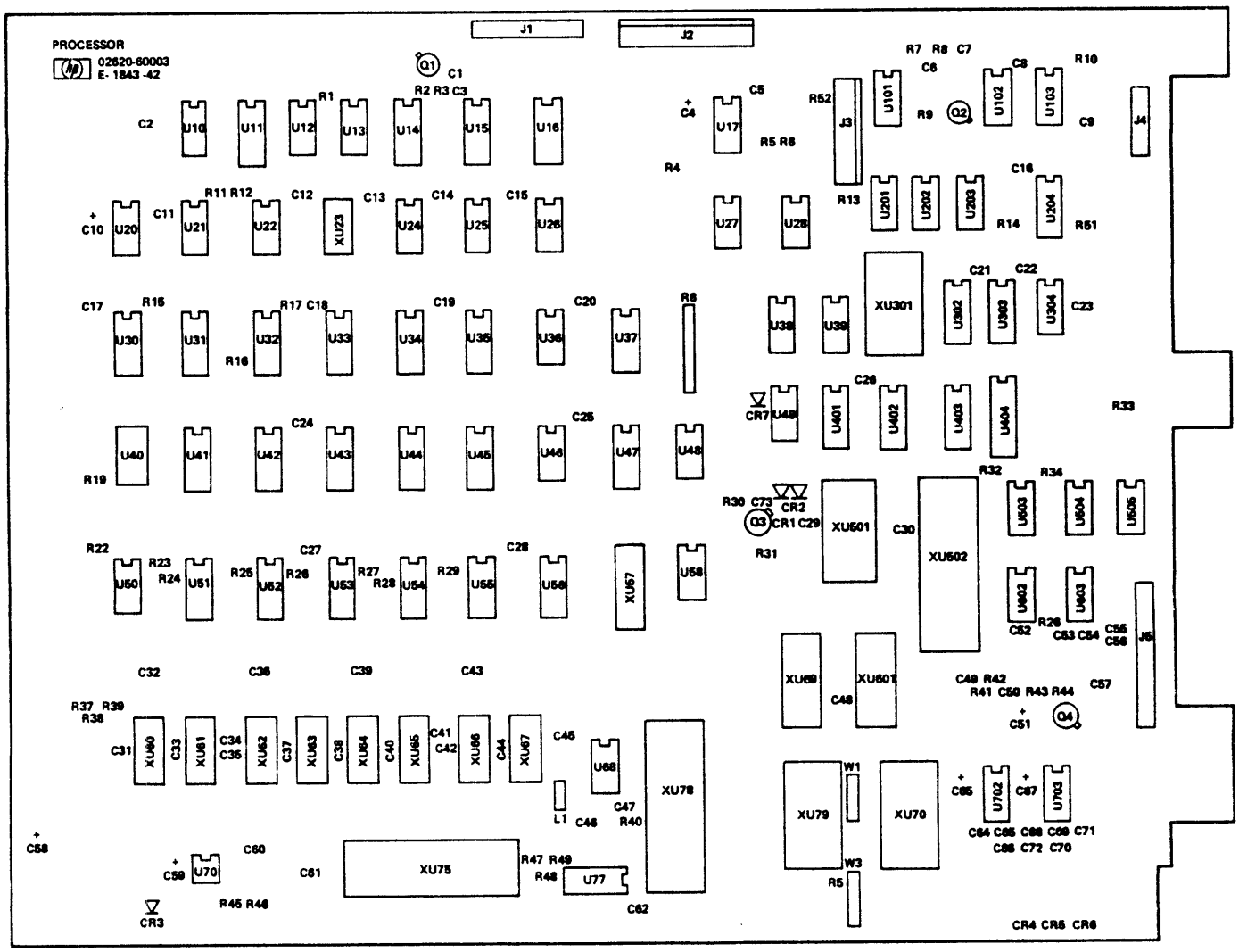


Figure 10
Processor PCA Component Location Diagram
JAN-22-79 13220-91003

DATE CODE: E-1843-42

CAP 27PF 5% 300V	0160-2306	4
C6,45,46,72		
CAP 470PF 10%	0160-3335	12
C52-56,64-66,68,69		
C71,73		
CAP.01UF 20%	0160-4554	30
C2,3,5,7,8,11-22,30,		
C47,48,57,60-62,70,		
C24-28		
CAP .1UF	0160-4557	19
C1,9,29,31-44,49,50		
CAP 6.8UF 20%	0180-1701	1
C51		
CAP 15UF 10% 20V	0180-1746	7
C4,10,23,58,59,63,67		
STUD SOLDER TERM	0360-0124	4
TP1-4		
RES 1K 5% .25	0683-1025	15
R4,13,14,15,32,33,34		
R36,41,42,44,47,48,49,10		
RES 10K 5% .25	0683-1035	2
R2,40		
RES 150 5% .25	0683-1515	1
R16		
RES 47 5% .25	0683-4705	1
R43		
RES 470 5% .25	0683-4715	3
R7,19,31		
RES 4700 5% .25	0683-4725	11
R1,3,5,6, 11,12,17,		
R22,30,50,51		
RES 82 5% .25W	0683-8205	11
R8,23-29,37-39		
RES 100 5% .5	0686-1015	1
R52		
RES 19.6K 1%.125	0698-3157	1
R45		

RES 14K 1% .125W	0698-4479	1	R46
XTAL OSC 25.77M	0960-0528	1	U40
SOCKET 24 PIN	1200-0541	4	XU79,301,501,701
SKT 16 DIP SLDR	1200-0607	8	XU60-67
SKT-IC 22-CONT	1200-0612	2	XU69,601
SKT-IC 14-CONT	1200-0638	1	XU23
SKT-IC 20-CONT	1200-0639	1	XU57
SKT-IC 40-CONT	1200-0654	3	XU75,78,502
CONN-POST 16P	1251-5499	1	J4
CONN-POST 26P	1251-5500	1	J1
CONN POST 7M CKT	1251-5520	1	J3
CONN POST 9M CKT	1251-5521	1	J2
CONN 34 PIN M	1251-5546	1	J5
FSTNR-SNP-IN	1390-0104	4	
FSTNR SNP IN	1390-0281	4	
NETWORK-RES SIP	1810-0279	1	R18
RAM 1K P5101L	1818-0708	2	U69,601
IC MC1488L	1820-0509	2	U602,702
IC SN74S112N	1820-0629	1	U204

IC	SN74S00N	1820-0681	4
U20,22,25,102			
IC	SN74S10N	1820-0685	2
U23,103			
IC	SN74S74N	1820-0693	1
U24			
IC	MC1489AL	1820-0990	2
U603,703			
IC	SN74128N	1820-1074	1
U68			
IC	SN74LS74N	1820-1112	1
U26			
IC	SN74LS02N	1820-1144	4
U12,28,36,304			
IC	SN74LS174N	1820-1196	2
U37,47			
IC	SN74LS00N	1820-1197	4
U21,27,46,202			
IC	SN74LS04N	1820-1199	3
U203,503,505			
IC	SN74LS05N	1820-1200	1
U504			
IC	SN74LS08N	1820-1201	1
U13			
IC	SN74LS10N	1820-1202	1
U10			
IC	SN74LS20N	1820-1204	1
U39			
IC	SN74LS27N	1820-1206	1
U38			
IC	SN74LS32N	1820-1208	1
U201			
IC	SN74LS38N	1820-1209	2
U48,58			
IC	SN74LS138N	1820-1216	2
U14,77			
IC	SN74LS151N	1820-1217	7

	PART NO CONT	1820-1217	
U51-56,401			
	IC 74LS109	1820-1282	1
U11			
	IC SN74S195N	1820-1303	3
U30,302,303			
	IC SN74S132N	1820-1307	1
U101			
	IC SN74LS132N	1820-1425	1
U17			
	IC SN74LS161N	1820-1430	13
U15,16,31,33-35,41-45 U402,403			
	IC SN74LS293 N	1820-1443	1
U49			
	IC SN74S37N	1820-1450	1
U50			
	IC SN74S163N	1820-1453	1
U32			
	IC M6850	1820-1690	1
U501			
	IC SN74LS273N	1820-1730	1
U404			
	IC SN74LS244N	1820-2024	1
U57			
	IC Z 80 CPU PS	1820-2188	1
U78			
	IC MC1458 OP AMP	1826-0139	1
U70			
	XSTR 2N2369 TO18	1854-0019	2
Q1,2			
	XSTR 2N4401 TO92	1854-0467	2
Q3,4			
	DIODE-SILICON	1901-0050	4
CR1-3,7			
	DIO TR SUP 18V	1902-0976	3
CR4-6			

	RES VAR 1K 10%	2100-3352	1
R9			
	WIRE JUMPERS	8159-0005	2
W1,3			
	COIL	9100-2272	1
L1			
	4K RAM	5090-0108	8
U60-67			
	ETCHED BOARD	02620-80003	1