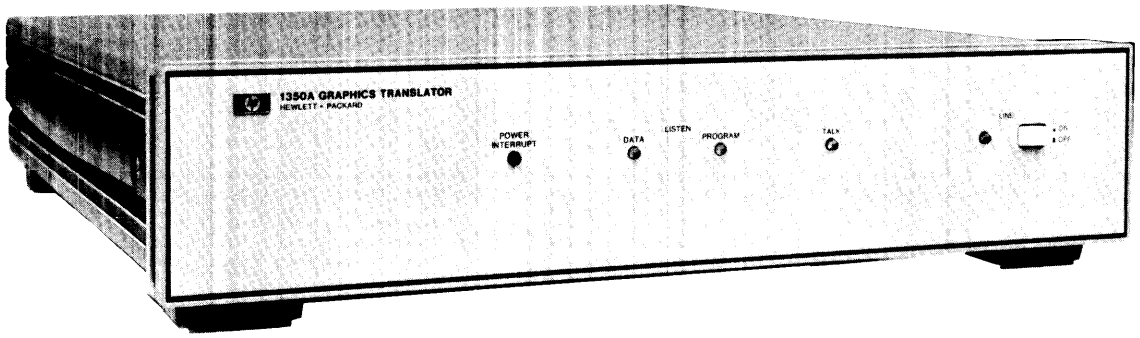
OPERATING AND SERVICE MANUAL

1350A
GRAPHICS TRANSLATOR



HEWLETT hp PACKARD

HP 1350A

OPERATING AND SERVICE MANUAL

MODEL 1350A
GRAPHICS TRANSLATOR

(Including Options 900, 901, 902, 904, 905, 906, 908, and 909)

SERIAL NUMBERS

This manual applies directly to instruments with serial numbers prefixed **1920A.**

With changes described in Section VII, this manual also applies to instruments with serial numbers prefixed **1906A, 1750A.**

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Manual Part Number 01350-90904
Microfiche Part Number 01350-90804

PRINTED: JULY 1979

SAFETY

This product has been designed and tested according to International Safety Requirements. To ensure safe operation and to keep the product safe, the information, cautions, and warnings in this manual, must be heeded. Refer to Section I and the Safety Summary for general safety considerations applicable to this product.

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard product is warranted against defects in material and workmanship for a period of one year from date of shipment. During the warranty period, Hewlett-Packard Company will, at its option, either repair or replace products which prove to be defective.

For warranty service or repair, this product must be returned to a service facility designated by HP. However, warranty service for products installed by HP and certain other products designated by HP will be performed at Buyer's facility at no charge within the HP service travel area. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses.

For products returned to HP for warranty service, Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

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The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

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THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

S C W & A 9/78

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

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SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This Operating and Service Manual contains information required to install, operate, test, adjust, and service the HP Model 1350A Graphics Translator.

1-3. Listed on the title page of this manual is a Microfiche part number. This number can be used to order 4- by 6-inch microfilm transparencies of the manual. Each microfiche contains up to 96 photo-duplicates of the manual pages. The microfiche package also includes the latest MANUAL Changes supplement.

1-4. SPECIFICATIONS.

1-5. Instrument specifications are listed in table 1-1. These specifications are the performance standards or limits against which the instrument is tested. Table 1-2 lists supplemental characteristics. Supplemental characteristics are not specifications but are typical characteristics included as additional information for the user.

1-6. SAFETY CONSIDERATIONS.

WARNING

To prevent personal injury, observe all safety precautions and warnings stated on the instrument and in this manual.

1-7. This product is a Safety Class 1 instrument (provided with a protective earth terminal). Review the instrument and manual for safety markings and instructions before operation. Specific warnings, cautions, and instructions are placed wherever applicable throughout this manual. Refer to the Safety Summary in the front of this manual and to Sections II and III for further safety precautions. These precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standard of design, manufacture, and intended use of this instrument. Hewlett-Packard assumes no liability for the customer's failure to comply with these requirements.

1-8. INSTRUMENTS COVERED BY MANUAL.

1-9. Attached to the instrument is a serial number tag. The serial number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the serial prefix, and the last five digits are the suffix. The prefix is the same for all identical instruments. The suffix, however, is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the serial number prefix(es) listed under SERIAL NUMBERS on the title page.

1-10. An instrument manufactured after the printing of this manual may have a serial number prefix that is not listed on the title page. This unlisted serial number prefix indicates that the instrument is different from those described in this manual. The manual for this newer instrument is accompanied by a Manual Changes supplement. This supplement contains "change information" that explains how to adapt the manual to the newer instrument.

1-11. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and part number, both of which appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard.

1-12. For information concerning a serial number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard office.

1-13. DESCRIPTION.

1-14. The Hewlett-Packard Model 1350A converts digital information to X, Y, and Z analog signals for driving high-resolution, directed-beam, nonstorage CRT displays. The 1350A accepts digital data from the Hewlett-Packard Interface Bus (HP-IB; IEEE Std. 488-1978) or RS-232C interface bus (optional) and stores the information in a 2048-word random-access memory (RAM). RAM is continually accessed to generate vectors and characters that refresh one or more displays.

1-15. Each of the 2048 words in RAM can be either a vector end-point (X and Y coordinates) or an ASCII character. A character read-only memory (ROM) generates the vectors necessary for each ASCII character. Therefore each character uses only one word of RAM. Each X-Y coordinate pair uses one word of RAM.

1-16. The RAM can be divided into as many as 32 files. All vectors and characters in a file may then be manipulated as one unit via file management commands. Each

file can be individually rewritten, erased, blanked, or flashed on and off the display for highlighting information of special interest. Erasing a waveform that intersects other waveforms (vectors) will not leave blank spaces at intersections. File management allows graphs to be quickly updated and compared, mechanical drawings to be "built up" or "stripteased," or three-dimensional "rotating" drawings to be created, for just a few examples.

1-17. The 1350A is also capable of driving an HP Model 1338A Tri-color display so that information can be displayed in three colors. The colors provide enhanced differentiation of information. This is especially desirable in applications such as radar, where quick judgements must be made from several types of information.

1-18. If a hard-copy plot is desired, the program that drives the 1350A can be quickly translated in order to drive a plotter.

1-19. OPTIONS.

1-20. Standard options are modifications installed on HP instruments at the factory and are available on request. The following options are available for the 1350A.

OPTION 001: RS-232C interface with selectable baud rates, replaces HP-IB interface. A field-installable kit (HP Part No. 52102A) is available that allows a standard 1350A to be modified for Option 001 capability.

OPTION 908: rackmount flange assembly without front handles (see outline drawing in table 1-2). A field-installable kit (HP Part No. 5061-0074) is available.

OPTION 909: rackmount flange assembly with front handles. A field-installable kit (HP Part No. 5061-0075) is available.

1-21. ACCESSORIES SUPPLIED.

1-22. The following accessories are supplied with the 1350A:

One 2.3 m (7.5 ft) AC Power Cord, HP Part No. 8120-1521 (90 °C IEC to NEMA 5-151P, 3-conductor for use in Canada, Mexico, Japan, and U.S.).
One Operating and Programming Guide.
One 0.8 AT (slow-blow) fuse, HP Part No. 2110-0020 (for 220-240 Vac operation).

1-23. ACCESSORIES AVAILABLE.

1-24. The following items are available for use with the 1350A:

Model 10184A Soft Copy Graphics Library. Allows HP Model 9825A graphics programs to drive 1350A (for soft copy) and HP plotters (for hard copy). This allows the same 9825A instructions to produce either soft or hard copy without using programmer time for translations.

Model 52125A. A one meter cable with four color-coded wires. Simplifies 1350A connection to display(s).

1-25. RECOMMENDED TEST EQUIPMENT.

1-26. Equipment required to test and maintain the 1350A is listed in table 1-3. Other equipment may be substituted if it meets or exceeds the critical specifications listed in the table.

Table 1-1. Specifications

INPUT INTERFACE: HP-IB listener only that conforms to IEEE 488-1978.
X and Y ANALOG OUTPUTS: +0.2 Vdc to +1.2 Vdc into 50 ohms. Positive up and to the right.
Z ANALOG OUTPUT: 0 to 1 Vdc unblanked, −1 Vdc blanked, into 50 ohms.
REFRESH RATE: dependent on total length of vectors displayed. Contact your HP Field Engineer for exact refresh rate for a given application.
ADDRESSABLE RESOLUTION: 1022 x 1023 points.

MEMORY

2048 vectors or characters.

32 Addressable Files: files can be erased or blanked. Files may be of any length, the total of which does not exceed memory size.
Addressable Write Pointer: allows new data to be written from that address forward.

CHARACTER GENERATOR

8 x 12 Resolution stroke characters. Modified full ASCII set (compatible with HP 9825A keyboard). Character strokes are stored in plug-in ROMs.
4 Programmable Sizes: 1X, 2X, 4X, 8X. 80 characters per line and 51 lines (not to exceed memory size) at 1X character size.
2 Programmable Orientations: 0° and 90° CCW.

Table 1-2. Supplemental Characteristics

AUXILIARY CONNECTOR: rear panel, allows 1350A to output color information to an HP 1338A Tri-color Display.

INPUT CONNECTOR: rear panel, conforms to IEEE 488-1978.

OUTPUT CONNECTORS: three rear panel BNCs for X,Y, and Z axes with shields grounded. Four rear panel BNC auxiliary outputs for TTL blanking of displays (high = blank).

FRONT PANEL

Indicator Lights: power interrupt, listen data, listen program, power on.

On/Off Switch

OPERATING ENVIRONMENT

Temperature: (operating) 0°C to +55°C (+32°F to +130°F); (non-operating) -40°C to +70°C (-40°F to +158°F).

Humidity: to 95% relative humidity at +40°C(+104°F).

Altitude: (operating) to 4600 m (15 000ft); (non-operating) to 7600 m (25 000 ft).

Shock: 30 g level with 11 ms duration and 1/2 sine wave shape.

Vibration: vibrated in three planes for 15 min. each with 0.25 mm (0.010 in.) excursion, 10 to 55 Hz.

POWER: selectable 100, 120, 220, or 240 Vac, +5%, -10%, 48 Hz to 440 Hz, max power 100 VA (approx 80 W). Average power dissipation at 60 Hz and 120 V without any options is approx 74 W.

SIZE: see outline drawing.

WEIGHT: net, 4.5 kg (10 lb); shipping, 11.8 kg (26 lb).

NOTES

1. DIMENSIONS ARE FOR GENERAL INFORMATION ONLY. IF DIMENSIONS ARE REQUIRED FOR BUILDING SPECIAL ENCLOSURES, CONTACT YOUR H.P. FIELD ENGINEER.

2. DIMENSIONS ARE IN MILLIMETRES AND (INCHES).

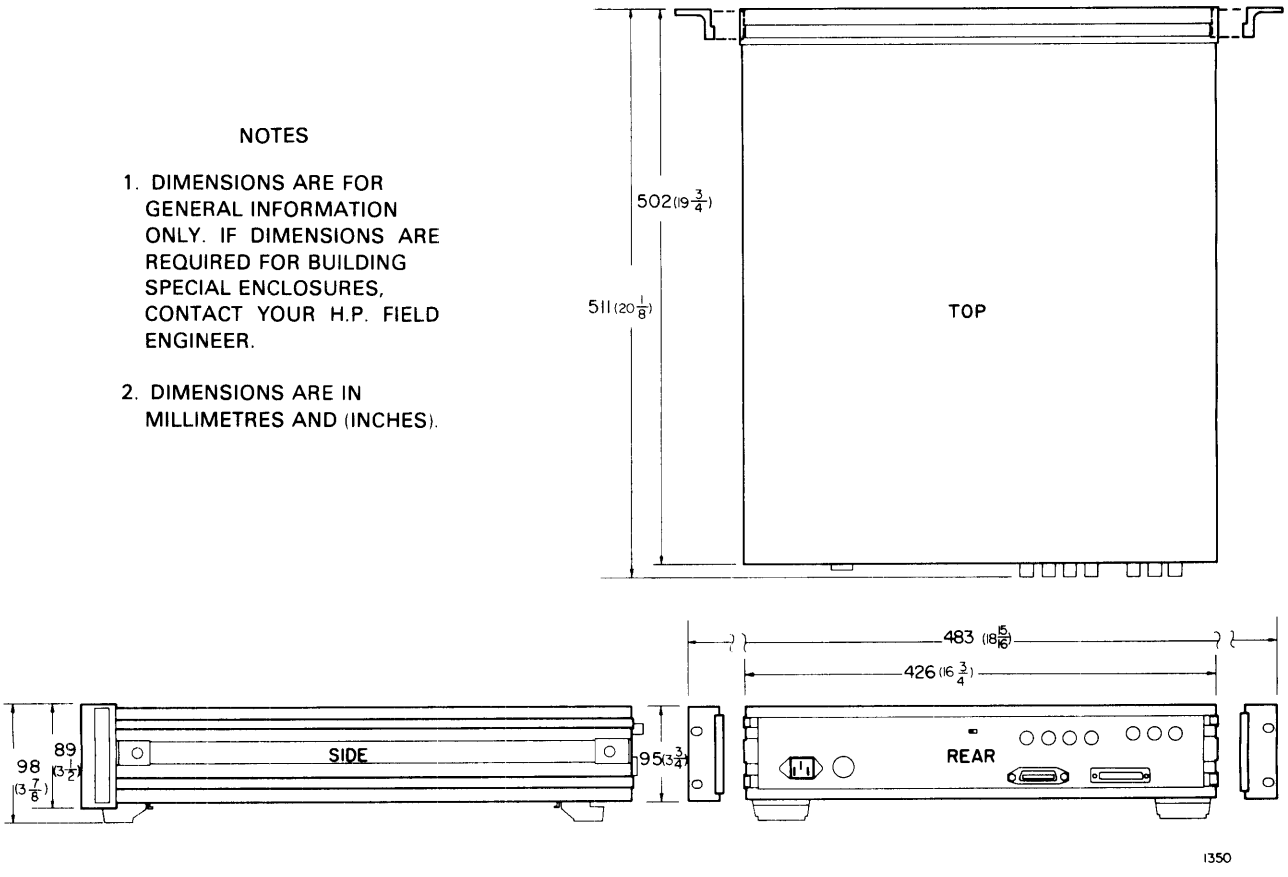


Table 1-3. Recommemded Test Equipment

Instrument	Critical Specifications	Recommended Model	Use*
Digital Voltmeter	+ or - 100 Vdc range, 0.3% accuracy	HP 3476A	A,T
Dual Channel Oscilloscope	50 MHz BW min	HP 1740A	T
X-Y Display	Directed-beam, 2MHz X,Y BW min; <25 ns Z rise time; full-scale deflection 1 V.	HP 1311A	P,A,T
HP-IB controller	IEEE 488-1978 Controller Capability (C1)	HP 9825A Opt.002 (23K byte R/W memory). Equipped with: 98034A HP-IB interface; 98210A String-Adv. Program ROM; 98213A Gen. I/O-Extended I/O ROM	P,A,T
Current Tracer		HP 547A	T
* P=Performance Test; A=Adjustment; T=Troubleshooting			

1-27. HP-IB INTERFACE CAPABILITY.

1-28. The interface capability of the 1350A (see table 1-4) is defined in accordance with IEEE Standard 488-1978, "Standard Digital Interface for Programmable Instrumentation."

Table 1-4. Model 1350A HP-IB Capabilities

Code	Interface Function
SH0	No Source Handshake
AH1	Acceptor Handshake
T0	No Talker
L2	Basic Listener
SR0	No Service Request
RL0	No Remote/Local
PP0	No Parallel Poll
DC0	No Device Clear
DT0	No Device Trigger
C0	No controller
E1	Open-collector Bus Drivers

1-29. HP-IB RESPONSE TIMES.

1-30. The 1350A receives each byte from HP-IB within approximately 1 microsecond. Certain commands cause the 1350A to generate internal delays that must be satisfied before the next byte can be received correctly. These commands and their approximate time requirements are listed in table 1-5.

Table 1-5. Command Time Requirements

Command	Time
EM (see Section III)	Twice the 1350A refresh time
EN	"
EX	"
BM	"
UM	"
FF	"
EF	"
BF	"
UF	"
(Note: If EM is done first, then the time for each of the others goes to approximately 6.67 ms.)	
";" following PA	3 microseconds
TX characters	3 microseconds/character

Table 1-6. Auxiliary Connector

Pin No.	Signal	Function
1-3	none	No connection.
4	TTL1	Same as DISPLAY 1 TTL blanking connector.
5	TTL2	Same as DISPLAY 2 TTL blanking connector.
6	Remote	Places auxiliary device under remote (1350A) control when low. Also holds off operation of pins 9 and 13 during power on reset.
7	C1	Color code LSB.
8	C2	Color code MSB.
9	Color Valid	Positive edge clock signals data on C1 and C2 is valid. Occurs approximately 250 ns after code is placed on C1 and C2.
10	Vector Busy	Low while 1350A is drawing a vector to prevent a color change.
11	+5 V	Output through a 10 ohm resistor.
12	+5 V	Output through a 10k ohm resistor.
13	Color Busy	A low from auxiliary device prevents 1350A from outputting vectors.
14-16	GND	Ground.
17	TTL3	Same as DISPLAY 3 TTL blanking connector.
18	TTL4	Same as DISPLAY 4 TTL blanking connector.
19-25	GND	Ground.

1-31. AUXILIARY CONNECTOR.

1-32. The rear-panel AUXILIARY connector allows the 1350A to output color information (select colors for data) when used with an HP 1338A Tri-color display. The interface signals from and to this connector are all TTL levels. Table 1-6 lists AUXILIARY connector pins, signals, and functions.

1-33. The "TRI-COLOR" paragraphs in Section III describe 1350A operation for color graphics. Table 1-7 lists 1350A color code outputs and their corresponding 1338A colors.

Table 1-7. 1350A File Name, Code Output, and 1338A Colors

File Name	C2 (MSB) pin 8	C1 (LSB) pin 7	1338A Color
0-15	high	high	Green
16-31	high	low	Yellow
32-47	low	high	Red
48-63	low	low	Yellow

1-34. HP 9825A MEMORY CONSIDERATIONS.

1-35. The 9825A Opt.002 has approximately 23K bytes of read/write memory available. This capacity can be increased to approximately 31K bytes by ordering Opt.003. The String-Adv. Programming and Extended I/O ROMs must be deleted. General I/O ROM must be included. For further information, contact your nearest Hewlett-Packard office.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section provides installation instructions for the Model 1350A Graphics Translator. This section also includes information about initial inspection and damage claims, preparation for use, and storage and shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until the contents of the shipment have been checked for completeness and the instrument has been checked mechanically and electrically. The contents of the shipment should be as listed in the "Accessories Supplied" paragraph in Section I. Procedures for checking electrical performance are given in Section IV. If the contents are incomplete, if there is mechanical damage or defect, or if the instrument does not pass the Performance Tests, notify the nearest Hewlett-Packard Sales/Service office. If the shipping container is damaged, or the cushioning material shows signs of stress, notify the carrier as well as the Hewlett-Packard office. Keep the shipping material for carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP Option without waiting for claim settlement.

2-5. PREPARATION FOR USE.

WARNING

Read the Safety Summary in the front of this manual and the "Safety Considerations" paragraph in Section I before installing or operating this instrument.

2-6. POWER REQUIREMENTS.

2-7. The 1350A requires a power source of 100, 120, 220, or 240 Vac +5%, -10%, single phase, 48 Hz to 440 Hz that can deliver approximately 100 VA (maximum). Average power dissipation at 60 Hz and 120 Vac without any options is approximately 74 W.

2-8. AC LINE VOLTAGE SELECTION.

CAUTION

Instrument damage may result if both line voltage selection switches are not set for the proper input voltage.

2-9. The instrument is normally set at the factory for 120 Vac operation. To operate the instrument from any other power source, proceed as follows:

a. Disconnect power cord from 1350A.

b. Using a blade-type screwdriver, position rear-panel LINE VOLTAGE SELECT switches for desired ac input. (Figure 2-1 shows switches set for 120 Vac operation.)

c. For 220 Vac or 240 Vac operation, replace rear-panel fuse (F1) with the 0.8 AT (slow blow) fuse, HP Part No. 2110-0020, supplied with the instrument.

d. Reconnect power cord.

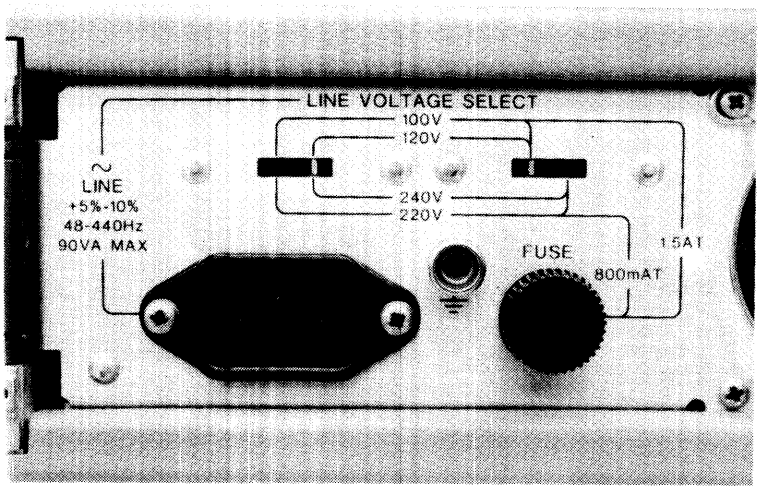


Figure 2-1. Line Voltage Selection Switches

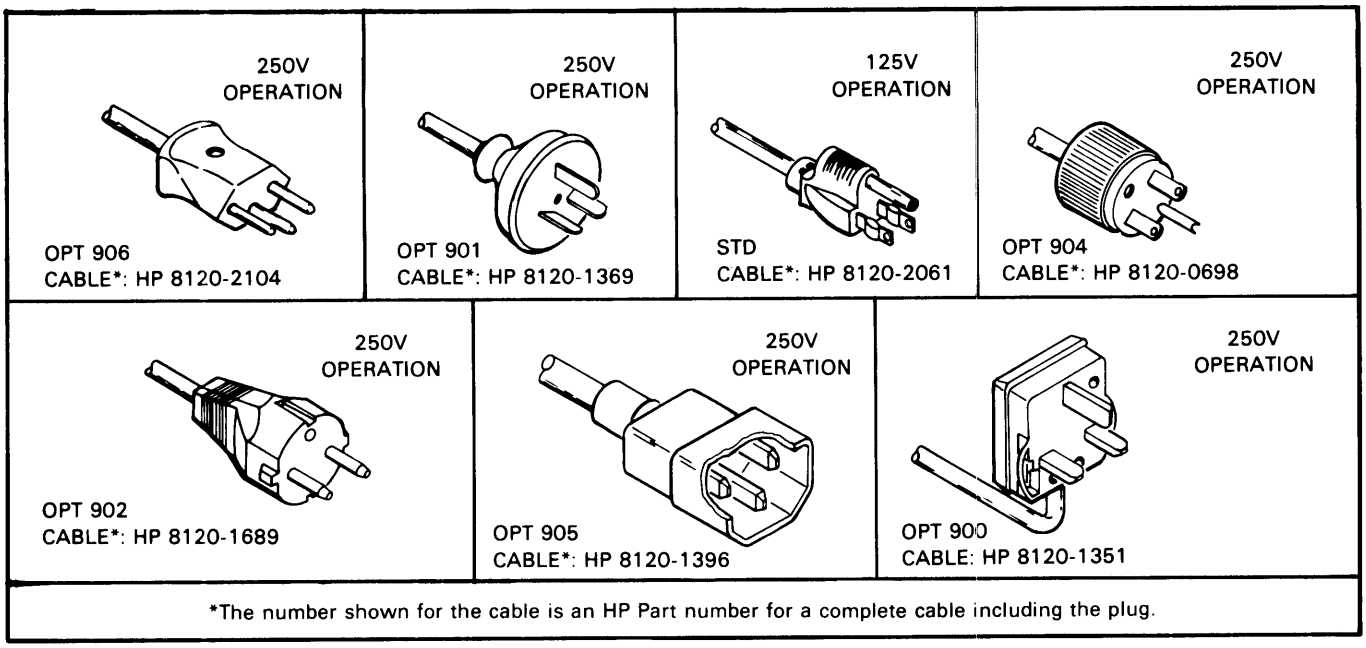


Figure 2-2. Power Cables Available

2-10. AC POWER CABLE.

2-11. This instrument is equipped with a three-wire power cable. When connected to an appropriate ac power receptacle this cable grounds the instrument cabinet. The type of power cable plug shipped with each instrument depends on the country of destination. Figure 2-2 shows the part numbers (and associated option numbers) for the power cables and plug configurations available.

2-12. OPERATING ENVIRONMENT.

2-13. TEMPERATURE. The instrument may be operated in temperatures from 0°C to +55°C (+32°F to +130°F).

2-14. HUMIDITY. The instrument may be operated in environments with humidity up to 95%. However, the instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-15. ALTITUDE. The instrument may be operated at altitudes up to 4600 m (15 000 ft).

2-16. STORAGE AND SHIPMENT.

2-17. ENVIRONMENT.

2-18. The instrument may be stored or shipped in environments within the following limits:

Temperature: -40°C to +70°C (-40°F to +158°F)
Humidity: Up to 95%
Altitude: Up to 7600 m (26 000 ft)

The instrument should also be protected from temperature extremes which cause condensation within the instrument.

2-19. PACKAGING.

2-20. Original Packaging. Containers and materials identical to those used in factory packaging are available through Hewlett-Packard offices. If the instrument is being returned to Hewlett-Packard for servicing, attach a tag indicating the type of service required, return address, model number, and full serial number. Also mark the container FRAGILE to ensure careful handling. In any correspondence, refer to the instrument by model number and full serial number.

2-21. Other Packaging. The following general instructions should be used for re-packing with commercially available materials:

a. Wrap instrument in heavy paper or plastic. (If shipping to Hewlett-Packard office or service center, attach tag indicating type of service required, return address, model number, and full serial number.)

b. Use strong shipping container. A double-wall carton made of 350-pound test material is adequate.

c. Use a layer of shock-absorbing material 70 to 100 mm (3-to 4-inch) thick around all sides of the instrument to provide firm cushioning and prevent movement inside container. Protect control panel with cardboard.

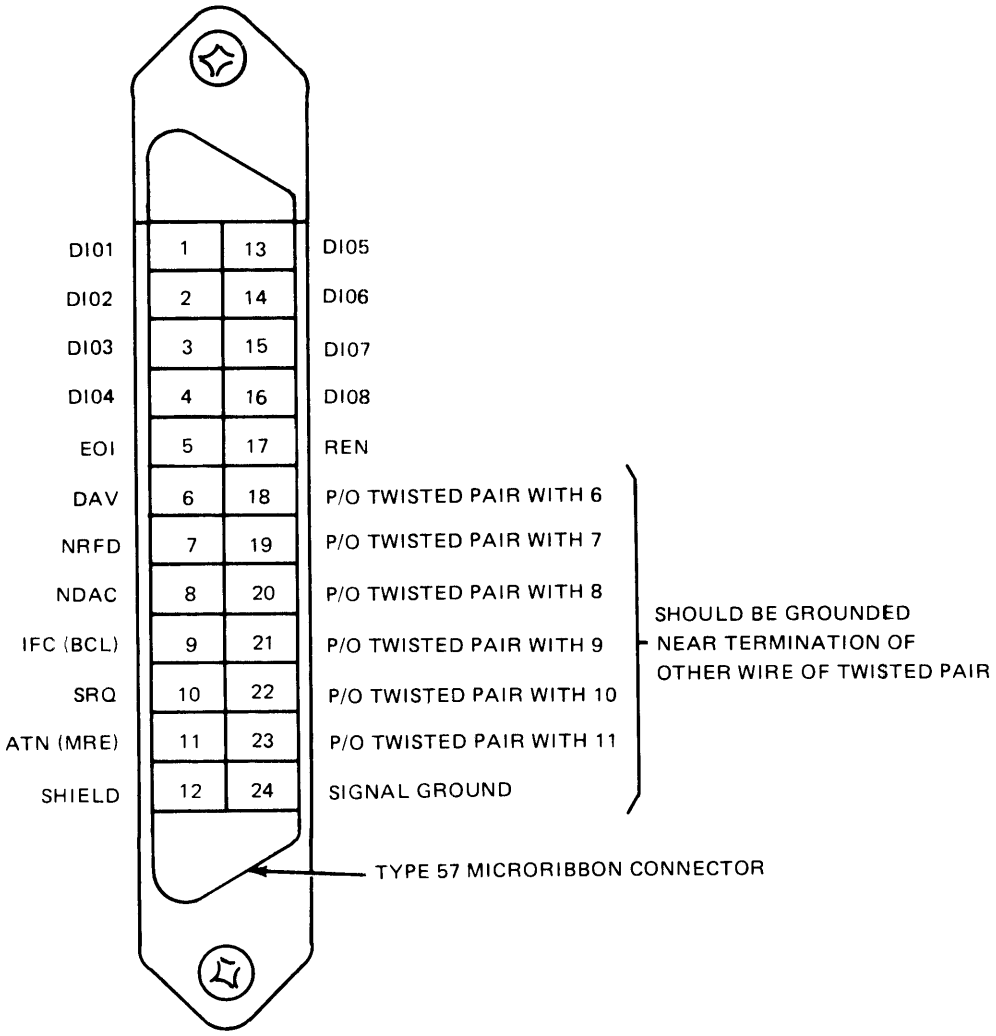
d. Seal shipping container securely.

e. Mark shipping container FRAGILE to ensure careful handling.

f. In any correspondence, refer to instrument by model number and full serial number.

2-22. HP-IB SYSTEM INTERFACE CONNECTIONS.

2-23. The 1350A is connected to the HP-IB by connecting an HP-IB interface cable to the 1350A rear-panel HP-IB connector (figure 2-3). As many as 14 instruments can be connected to the same interface bus. The maximum cable length that can be used must not exceed: (a) two meters (6.5 ft) times the number of instruments connected to the bus; or (b) 20 meters, whichever is less.



Mating Cables: HP 10631A, 0.9 meters (3 ft.); HP 10631B, 1.8 meters (6 ft.); HP 10631C, 3.7 meters (12 ft.).

Bus Mnemonics:

DI01-DI08	Data Input/Output
EOI	End or Identify
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Data Not Accepted
IFC	Interface Clear
SRQ	Service Request
ATN	Attention
REN	Remote Enable

Figure 2-3. Hewlett-Packard Interface Bus Connector

2-24. HP-IB ADDRESS SELECTION.

2-25. The listen address for the 1350A is selected by Address Switch A3S1 located on Input/Output Assembly A3. The five switches labeled 1 thru 5 are used to select the unique listen address for the 1350A. The 1350A may be left at its factory setting (10010 = 18 in base 10), or it may be set to any alternate setting available. Refer to figure 2-4 and table 2-1 for address codes and their corresponding switch settings. Switch section "1" (nearest rear panel) is the least significant bit (LSB).

2-26. Make sure to remove power cord from 1350A before changing address switch.

NOTE

The 5-bit decimal code, consisting of bits A1 thru A5, is used by contollers (which use this code convention) as a system device number for addressing instruments.

2-27. DISPLAY CONNECTIONS.

2-28. The 1350A can drive several displays in a parallel configuration. If different information is to be presented on each display, the 1350A TTL outputs must be connected to TTL inputs (positive blanking) on the displays. Figure 2-5 shows connections in a single display application. Figure 2-6 shows connections when four displays are used.

2-29. The number of displays that can be driven without degradation of the display image is dependent on the type and length of the interconnecting cables. In multiple display applications the display farthest from the 1350A (cable length) must be in 50 ohm input configuration, and all others must be in high impedance input configuration. In single display applications the display must be in 50 ohm input configuration. For further information regarding multiple display applications, contact your nearest Hewlett-Packard Sales/Service office.

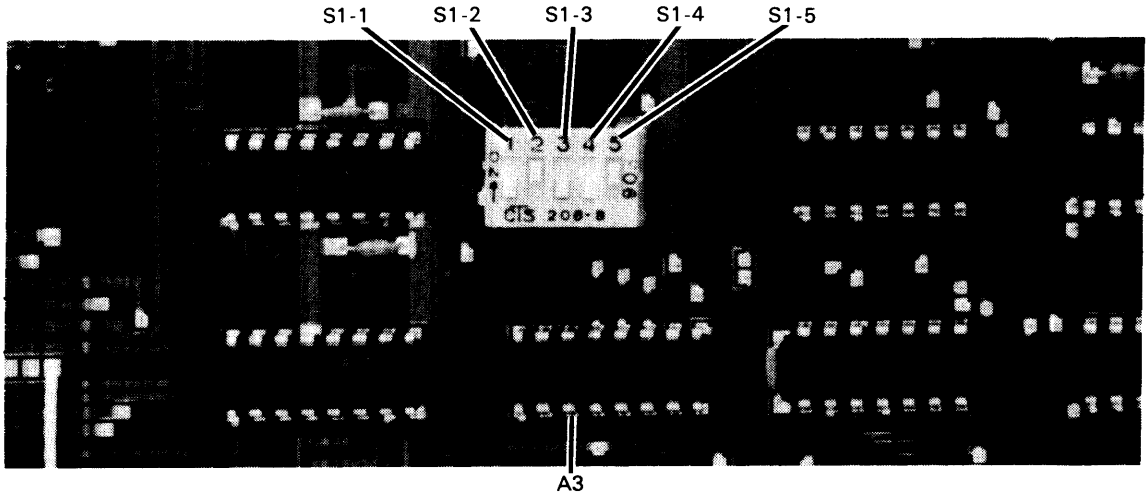


Figure 2-4. Address Switch A3S1

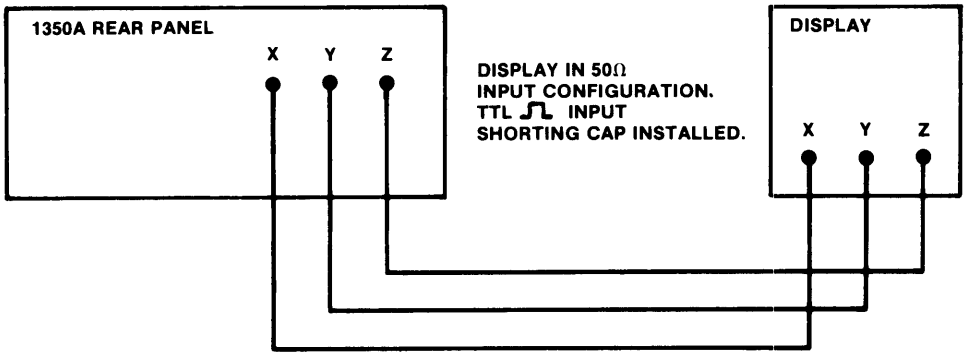


Figure 2-5. 1350A Connected to a Single Display

Table 2-1. HP-IB Address Codes

ASCII CHARACTER		BINARY CODE							OCTAL CODE		5 BIT DECIMAL
Listen Address	Talk Address	*b_7	b_6	A5 b_5	A4 b_4	A3 b_3	A2 b_2	A1 b_1	Listen	Talk	Value**
SP	@			0	0	0	0	0	040	100	0
!	A			0	0	0	0	1	041	101	1
"	B			0	0	0	1	0	042	102	2
#	C			0	0	0	1	1	043	103	3
$	D			0	0	1	0	0	044	104	4
%	E			0	0	1	0	1	045	105	5
&	F			0	0	1	1	0	046	106	6
'	G			0	0	1	1	1	047	107	7
(	H			0	1	0	0	0	050	110	8
)	I			0	1	0	0	1	051	111	9
*	J			0	1	0	1	0	052	112	10
+	K			0	1	0	1	1	053	113	11
,	L			0	1	1	0	0	054	114	12
-	M			0	1	1	0	1	055	115	13
.	N			0	1	1	1	0	056	116	14
/	O			0	1	1	1	1	057	117	15
0	P			1	0	0	0	0	060	120	16
1	Q			1	0	0	0	1	061	121	17
2 ***	**R *****			**1**	**0**	**0**	**1**	**0 *****	**062**	**122**	**18 *****
3	S			1	0	0	1	1	063	123	19
4	T			1	0	1	0	0	064	124	20
5	U			1	0	1	0	1	065	125	21
6	V			1	0	1	1	0	066	126	22
7	W			1	0	1	1	1	067	127	23
8	X			1	1	0	0	0	070	130	24
9	Y			1	1	0	0	1	071	131	25
:	Z			1	1	0	1	0	072	132	26
;	[			1	1	0	1	1	073	133	27
<	/			1	1	1	0	0	074	134	28
=	]			1	1	1	0	1	075	135	29
>	^			1	1	1	1	0	076	136	30

* Only the first five bits of the binary code are listed. These bits (set by A3S1) are the same for both the TALK and LISTEN address. The sixth and seventh bits (b_6 and b_7 become bus DIO6 and DIO7 lines from controller) determine whether the instrument is being addressed to TALK or LISTEN.

Function	Bit 7	6
Talk	1	0
Listen	0	1

** Derived from the binary value of the first five address bits.

*** 1350A factory set address.

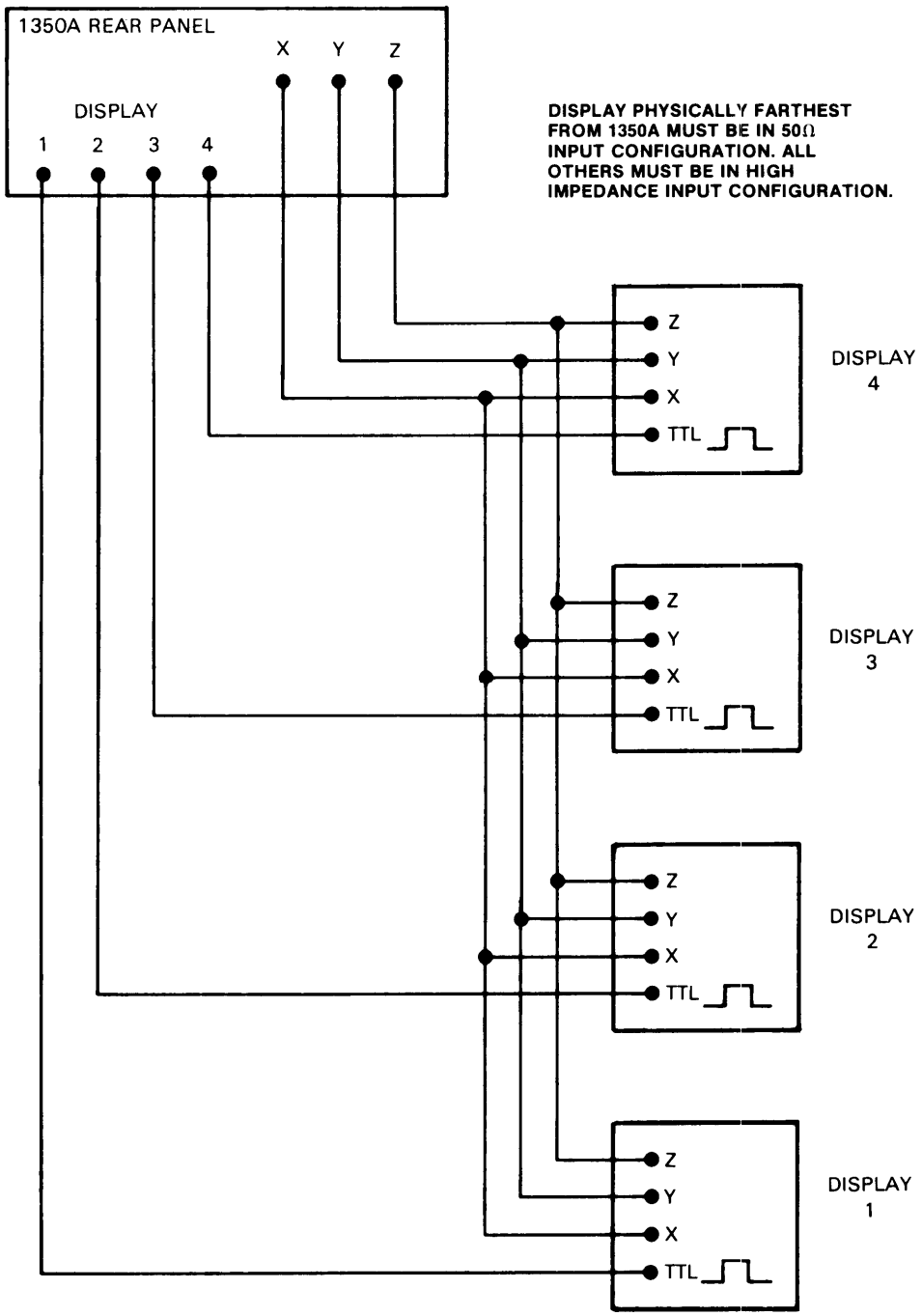


Figure 2-6. 1350A Connected to Four Displays (Using TTL Blanking)

SECTION III

OPERATION

3-1. INTRODUCTION.

3-2. This section provides basic programming information and explains 1350A controls, connectors, and indicators.

3-3. For detailed operating information when the 1350A is used with an HP Model 9825A Controlling Calculator, see 1350A Operating and Programming manual.

3-4. PANEL FEATURES.

3-5. The 1350A front and rear panels are shown and described in figure 3-1.

3-6. OPERATING CHARACTERISTICS.

3-7. The 1350A translates digital information to analog signals. The digital information is received from HP-IB (or RS-232C). The analog signals "draw" vectors (and characters) on the CRT(s) of directed-beam X-Y display(s).

NOTE

In single display applications, the X-Y display must be in 50 ohm input configuration. If not, the CRT will have compressed video on the right-hand side. In multiple display applications, the display that is physically farthest from the 1350A must be in 50 ohm configuration. All other displays must be in high impedance input configuration.

3-8. 1350A REFRESH RATE.

3-9. The time required for the 1350A to completely cycle through its memory determines how often the 1350A will refresh the CRT.

3-10. This memory cycle time is called 1350A refresh time. The recriprocal of refresh time is the 1350A refresh rate. 1350A refresh time is the total drawing time of all vectors and characters to be presented on a CRT.

3-11. Maximum 1350A refresh rate is 300 Hz. Therefore, minimum 1350A refresh time is 3.33 ms (1/300 Hz). Refresh time becomes important when calculating the time required for the 1350A to process certain commands (so that the next command can be properly received). See table 3-7 for refresh-delayed commands.

3-12. Typical drawing times for characters and vectors are listed in table 3-1. To determine 1350A refresh time, total the drawing times for all characters and vectors to be presented. If the total is less than 3.33 ms, then use 3.33 ms for refresh time and 300 Hz for refresh rate.

Table 3-1. Typical Drawing Times for Vectors and Characters

Average character	15 μs (microseconds)
Vectors:	
1/2 or greater screen diameter	48 μs
1/4 to 1/2 screen diameter	24 μs
1/8 to 1/4 screen diameter	12 μs
1/16 to 1/8 screen diameter	6 μs
1/32 to 1/16 screen diameter	3 μs
1/64 to 1/32 screen diameter	1.5 μs

Example:

A CRT presentation contains: 50 characters, a graticule of 20 vertical and 20 horizontal lines; 30 tick marks on graticule lines; and 200 data points joined by short vectors.

Refresh time calculation:

50 characters x 15 μs (microseconds) = 750 μs
40 graticlue vectors x 48 μs = 1,920 μs
(30 + 200) short vectors x 1.5 μs = 345 μs

Total = 3,015 μs

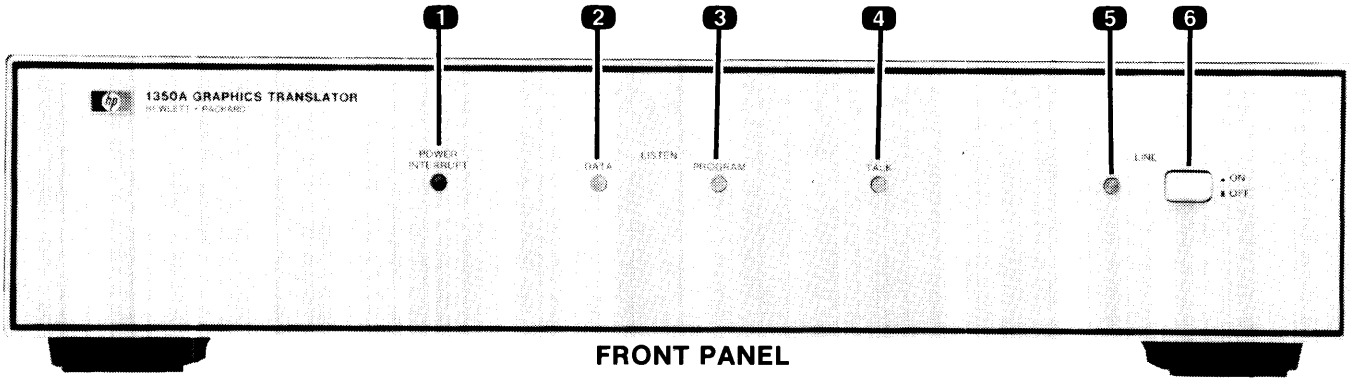
3,015 μs = 3.015 ms

Since 3.015 ms is less than minimum 1350A refresh time of 3.33 ms, use 3.33 ms for refresh time and 300 Hz for refresh rate.

3-13. If the 1350A is in LINE SYNC, first calculate refresh time as shown above. Then use the next larger value of the recriprocal of two times the line frequency. For example, if refresh time is calculated as 7.37 ms and line frequency is 60 Hz, then use 1/120 = 8.33 ms for refresh time. The general formula is n*(1/2t) where n is the appropriate integer and t is the line frequency.

3-14. 1350A MEMORY MANAGEMENT.

3-15. The 1350A memory management scheme uses Files for selective displaying and updating of information. For example, the axes and labeling on a graph may be placed in one file. Each line on the graph may then be placed in its own file (up to 32 files possible). This allows



FRONT PANEL

1 POWER INTERRUPT. Indicates voltage changes in A.C. line power that could cause HP-IB information or information stored in 1350A memory to be altered.

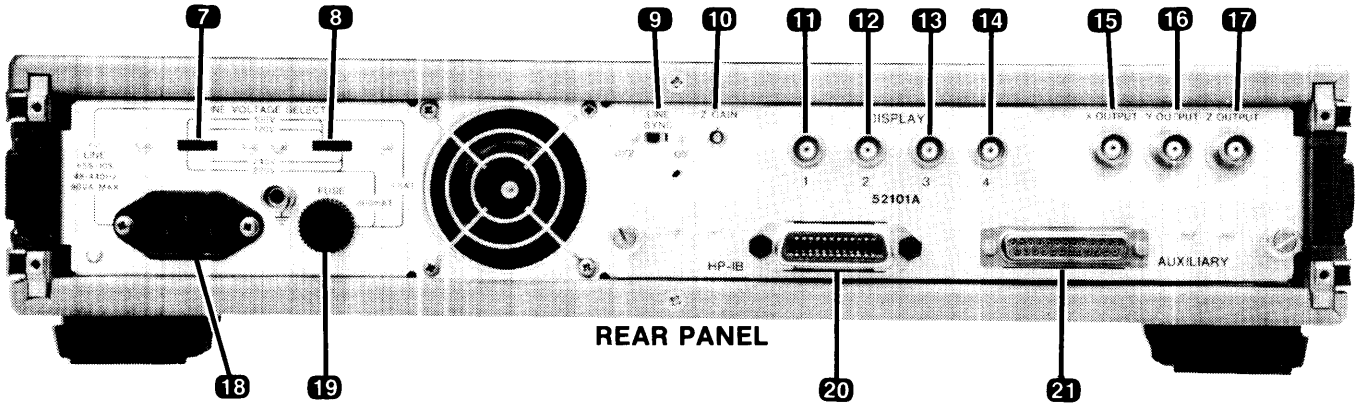
2 LISTEN DATA. Indicates that the 1350A has been addressed to listen and is receiving parameter (or text) bytes following a two-letter "PROGRAM" command.

3 LISTEN PROGRAM. Indicates that the 1350A has been addressed to listen and is receiving a two-letter "PROGRAM" command.

4 TALK. Indicates that the 1350A has received and responded to its talk address. This state should never occur, as the 1350A is not configured to transmit data on HP-IB.

5 LINE. Indicates if A.C. line power is on or off.

6 ON/OFF. Turns A.C. line power on or off.



REAR PANEL

7 & 8 LINE VOLTAGE SELECT. Selects desired AC line voltage.

9 LINE SYNC. Synchronizes 1350A to A.C. power line.

10 Z GAIN. Adjusts output amplitude of Z axis signal.

11 12 13 14 DISPLAY. Provides TTL blanking to four separate displays.

15 X OUTPUT. X axis analog output signal for display input.

16 Y OUTPUT. Y axis analog output signal for display input.

17 Z OUTPUT. Z axis analog output signal for display input.

18 A.C. INPUT POWER.

19 FUSE. A.C. line protection.

20 HP-IB. Connector for Hewlett-Packard Interface Bus Cable (from controller).

21 AUXILIARY. Connector that has TTL blanking outputs (same as 11-14) as well as information to control the Hewlett-Packard 1338A Tri-Color Display.

Figure 3-1. 1350A Controls, Connectors, and Indicators

rapid updating in order to show new results, or selective blanking and unblanking of the files for comparison.

3-16. The 1350A memory also allows information to be displayed selectively on up to four X-Y displays. Sixteen possible combinations allow different displays to be either blanked or unblanked as desired.

NOTE

The 1350A is capable of drawing 2048 vectors (or 2048 characters, or a total of 2048 vectors and characters). Only vector ("PA") and text ("TX") commands will cause these 2048 locations in 1350A memory to be occupied. Each vector (or character) occupies one location.

3-17. PROGRAMMING.

3-18. Device-dependent commands (ASCII characters) for the 1350A are listed in table 3-2. These commands provide vector, character, file management, memory control, multiple display management, and color control information to the 1350A.

3-19. The 1350A can respond to its device-dependent commands only when addressed to listen.

3-20. The 1350A device-dependent command set is called Graphics Translator Machine Language (GTML).

3-21. FORMATTING RULES.

3-22. All commands are two letters (ASCII). They may be either upper or lower case.

NOTE

ASCII characters are shown within quote marks (") except for Carriage Return (CR), Line Feed (LF), End of Text (ETX), and DC4.

3-23. All commands must be terminated (delimited) by a colon (":"), or a Carriage Return (CR), or a Line Feed (LF) character.

3-24. Following a Text ("TX") command, the 1350A must receive an ASCII ETX (3 in base 10 = End of Text) character in order to exit text mode. A ":" (or CR or LF) is then required to terminate the "TX" command. Special text characters are listed in table 3-3.

3-25. If numeric parameters follow a command:

a. The first value (from one to four digits long) must be followed by a comma (",").

b. In the case of a Plot Absolute ("PA") command, the X value (one to four digits) must be followed by a comma (",") and the Y value (one to four digits) must be followed by a semicolon (";").

c. Several vectors may be drawn by one PA command before termination by a ":" (or CR or LF).

Example:

"pa500,800;200,300;1000,1023;:"

d. Following the two-letter command, a data field exists until delimited by a comma (","). The data field is of variable length. In this field, only the last four characters will be latched into the 1350A. If less than four characters are placed in the data field, the 1350A automatically inserts leading zeroes internally. If more than four characters are placed in the data field (leading spaces for example), the 1350A will ignore all except the last four characters. Any characters in these last four positions (preceeding the comma) will be treated as digits by the 1350A.

Example:

"nfXXXXXXXXXX...XXXXDDDD,:"
Where X= don't care; D = ASCII digit.

NOTE

Data fields (parameters following a two letter command) must contain integer values only in the last four positions preceeding the comma. If computed values (for example SIN X) are liable to produce noninteger results, then format statements should be used to truncate the decimal point and all values to the right of the decimal point.

3-26. A Character Size ("CS") command should precede a "TX" command. This preconditions the size and rotation of text. The 1350A follows the last Character Size command received when in text mode.

3-27. The 1350A follows the last Pen Enable ("PE") command received (CRT beam on or off). "PE" can be overridden by Blank Memory ("BM") or Blank File ("BF") commands.

3-28. FILES.

3-29. Data (vectors and/or characters) may be assigned to a file. 1350A memory may be sectioned into as many as 32 files (0-31). Each file can contain from one to 2048 vectors (or characters, or a combination of both). Total contents of all files must not exceed 1350A memory size of 2048 words (vectors + characters).

3-30. Each file may be blanked, unblanked, erased, or written over with new data.

3-31. A file, even though named, does not exist until something has been placed in it.

3-32. A Stop Name (SN) command should follow the last entry into a file.

3-33. A file cannot be addressed via Find File (FF), Erase File (EF), Blank File (BF), or Unblank File (BF) commands until it has been named and has contents.

Table 3-2. 1350A GTML Commands

Two letter mnemonic	Parameter	Description
		VECTOR GROUP
peD,	D = 0 pen up (beam off) D = 1 pen down (beam on)	Pen Enable. Defines CRT blank/unblank.
paX,Y;	X = 0 to 1022 Y = 0 to 1023	Plot Absolute (X,Y)
csD,	D = 0 X1 0° D = 1 X2 0° D = 2 X4 0° D = 3 X8 0° D = 4 X1 90° CCW D = 5 X2 90° CCW D = 6 X4 90° CCW D = 7 X8 90° CCW	Character Size. Defines size and rotation for text.
tx	desired text (See table 3-3.)	Text. ETX required to exit (ETX=3 base 10).
		MEMORY GROUP
em	none	Erase Memory. Erases vector and pen values. Moves write pointer to address 0.
bm	none	Blank Memory. Blanks entire 1350A memory. Prevents any output of information.
um	none	Unblank Memory. Allows information to be displayed in accordance with other commands.
flD,	D = 0 to 2047	Find Location. Moves the write pointer so that the next word is written into the location specified by FL parameter.
		FILE GROUP
nfD,	D = 0 to 31 (non-color operation)	Name File. Name following data as file number D.
sn	none	Stop Naming. Ends data entry into file.

Table 3-2. 1350A GTML Commands (Cont'd)

Two letter mnemonic	Parameter	Description
bfD,	D = 0 to 31	Blank File. Blanks all data in file D.
ufD,	D = 0 to 31	Unblank File. Unblanks data in file D in accordance with PE commands.
ffD,	D = 0 to 31	Find File. Moves write pointer to first memory location in file D.
efD,	D = 0 to 31	Erase File. Erases all data in file D.
en	none	Erase Names. Erases all file names. All data in memory is assigned to file 0. Data in memory is not changed.
		MULTIPLE DISPLAY GROUP
wxD,	D = 0 to 15	Write Auxiliary. Parameter blanks/unblanks up to four displays in 16 possible combinations. All data entered after WX will be displayed according to WX parameter until a SX.
sx	none	Stop Auxiliary. Stops assigning data to a WX TTL output combination.
ex	none	Erase Auxiliary. Sets all WX parameters to 0. All TTL outputs are unblanked.

3-34. REQUIRED INITIALIZATION SEQUENCE.

3-35. Whenever the 1350A is powered on, or whenever a new program is to be sent to the 1350A, an initialization sequence is required. This sequence provides the proper starting point by "clearing out" the 1350A.

3-36. The initialization sequence is: (1) IFC; (2) ETX; (3) DC4; (4) CR; (5) LF; (6) "EM::"; (7) "EN::"; (8) "EX::"; (9) "SN::"; (10) "SX::"; (11) "UM::".

3-37. The initialization sequence is shown below using an HP Model 9825A controller as an example.

```
0: cli 7
1: wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
```

The cli 7 command pulls HP-IB IFC (Interface Clear) line low momentarily. The 1350A requires this in order to insure that it will handshake properly on HP-IB.

The wtb 718 addresses 9825A to talk and 1350A to listen; it then sends the following information to the 1350A:

3	=	EXT (End of Text). This insures that 1350A is not in text mode.
20	=	ASCII DC4 character to turn off POWER INTERRUPT LED.
13	=	Carriage Return.
10	=	Line Feed.
EM		Erases vector and pen enable data following random power up of memory cells.
:		Terminates command.
EN		Erases all file names following random power up of memory cells.
EX		Erases all TTL blanking information.
SN		Insures that no files are named until desired.
SX		Insures that no TTL blanking is done until desired.
UM		Insures that 1350A memory is unblanked.

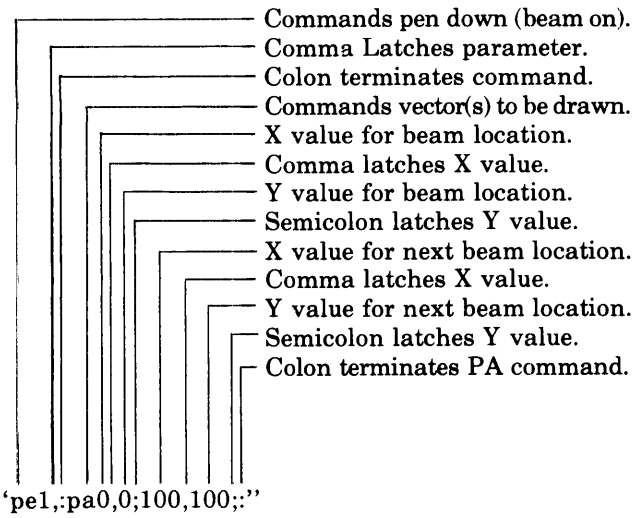
Table 3-3. Text Mode Special Characters

Decimal Value	Definition
3	ETX (End of Text). Used to exit text mode.
8	Backspace. Depends on character size.
9	Inverse Line Feed. Depends on character size.
10	Line Feed. Depends on character size.
11	Vertical Tick Mark. (')
12	Horizontal Tick Mark. (-)
13	Carriage Return. Moves beam to left edge of display.
14	X Marker Symbol.
15	Rectangle Symbol.
19	Pointer Symbol. (<--)
30	Diamond Symbol.

Note: For a complete list of the 1350A modified ASCII character set, see 1350A Operating and Programming manual.

3-38. EXAMPLE COMMAND STRINGS.

The following command string will cause the 1350A to draw a vector from the lower left corner of the CRT to approximately 1/8 screen diameter in a diagonal direction.



The following command string places the vectors for a triangle in file 16.

"nf16,:pe1,:pa1000,1000;1000,0;0,0;:sn:"

The following command string causes a diagonal vector to be displayed on displays 1 and 2. Displays 3 and 4 are blanked.

"wx12,:pe1,:pa0,0;1000,1000;:sx:"

The following command string: (a) blanks CRT; (b) positions beam; (c) unblanks CRT; (d) preconditions text size and rotation. Text message (Hello!) is displayed going up the CRT. The 3 is ETX; 13 is Carriage Return; 10 is Line Feed.

"PE0,:PA500,500;:PE1,:CS5,:txHello !",3,13,10

3-39. TTL BLANKING.

3-40. All vectors and characters (data) entered between a WX and an SX will be displayed on multiple displays according to the WX parameter. Table 3-4 lists the blank/unblank combinations for all WX parameters.

3-41. A Stop Auxiliary ("SX") command should follow the last entry placed under a Write Auxiliary ('WX') command.

Table 3-4. WX TTL Blank/ Unblank Combinations

WX Parameter	Display 4	3	2	1
0	U	U	U	U
1	U	U	U	B
2	U	U	B	U
3	U	U	B	B
4	U	B	U	U
5	U	B	U	B
6	U	B	B	U
7	U	B	B	B
8	B	U	U	U
9	B	U	U	B
10	B	U	B	U
11	B	U	B	B
12	B	B	U	U
13	B	B	U	B
14	B	B	B	U
15	B	B	B	B

U = Unblank. B = Blank.

3-42. HARDWARE BLINKING.

3-43. TTL Outputs 1, 2, and 3 can each be set to blink at a 4 Hz rate when unblanked by WX parameters 8 thru 15. Figure 3-2 shows the location of the Blinking Switch on the Input/Output Board. Table 3-5 lists possible blinking combinations for displays that are unblanked by WX 8-15. Blinking is not possible with WX 0-7.

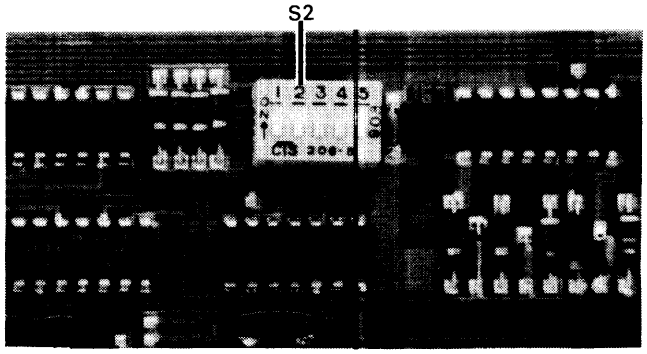


Figure 3-2. Blinking Switch S2 Location on Input/Ouput Board

Table 3-5. TTL Blink Combinations for WX 8-15

WX Parameter	Display 4	3	2	1
8	B	U*	U*	U*
9	B	U*	U*	B
10	B	U*	B	U*
11	B	U*	B	B
12	B	B	U*	U*
13	B	B	U*	B
14	B	B	B	U*
15	B	B	B	B

B = Blank. U* = Unblank and Blink if switch set.

3-44. POINT BLANKING.

3-45. The Point Blanking switch (figure 3-3) allows the X-Y display to be blanked during the time interval between vectors. This is useful when a slow X-Y display is used.

3-46. The switch is set to unblank position at the factory. When an HP Model 1338A Tri-color display is used the switch should be set to blank (rear) position.

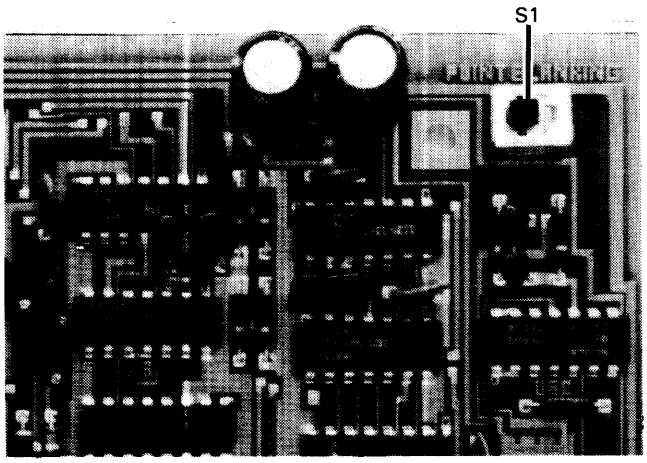


Figure 3-3. Point Blanking Switch Location on Control Board

3-47. LINE SYNC.

3-48. For systems having severe ground loop problems (or environments with strong magnetic fields) the 1350A may be synchronized to the ac line frequency. This is done with rear-panel LINE SYNC switch. Switch position nearest fan is OFF.

3-49. Line sync should be used only when absolutely necessary. When line sync is used the display refresh rate may be reduced to the point where flicker becomes objectionable.

3-50. TRI-COLOR.

3-51. 1350A file name determines the color of data displayed by a 1338A Tri-color Display. Table 3-6 lists the colors of data placed in 1350A files.

3-52. Only 32 files (0 thru 31) are used in the 1350A. However, file names 0 thru 47 are necessary to select all three colors on the 1338A. Files 32 thru 47 "wrap around" into files 0 thru 15. For example, data entered into file 35 is displayed in red, but due to "wrap around" the data is automatically stored in file 3 by the 1350A. This can cause a problem if file 3 is supposed to contain its own data (35 - 32 = 3).

3-53. Because of "wrap around", we recommend that files 0 thru 7 be used for GREEN, files 16 thru 31 for YELLOW, and files 40 thru 47 for RED.

Table 3-6. File Name Colors

File Name	Color
0 - 15	GREEN
16 - 31	YELLOW
32 - 47	RED
48 - 63*	YELLOW
*Files 48 - 63 not used due to "wrap around."	

3-54. PHOSPHOR PROTECT ON LARGE SCREEN DISPLAYS.

3-55. When the 1350A is used with a large screen display (such as an HP 1311A), the display may need to have its Phosphor Protect Switch "off" in order to produce desired intensity. Refer to display manual for switch location and function.

3-56. 1350A COMMAND RESPONSE TIMES.

3-57. The 1350A receives each byte from HP-IB within approximately 1 microsecond. Certain commands cause the 1350A to generate internal delays that must be satisfied before the next byte can be received correctly. These commands and their approximate time requirements are listed in table 3-7.

Table 3-7. Command Time Requirements

Instruction	Time
EM	Twice the 1350A refresh time
EN	"
EX	"
BM	"
UM	"
FF	"
EF	"
BF	"
UF	"
(Note: If EM is done first, then time for others ~6.67 ms each.)	
";" following PA	3 μs
each character following TX	3 μs

Examples:

A "pe1,:" will require approximately 5 μs. If followed by CR LF (Carriage Return; Line Feed), then about 7 microseconds.

A "pa50,50;100,100;:" will require about 21 μs (3 μs for each semicolon after pa; 1 us for each other character).

'A "txHello There!" will require about 38 μs (12 characters at 3 μs/character +2 μs for tx).

3-58. POTPOURRI.

3-59. DUMMY FILES.

3-60. The following example "dummy" program (using an HP 9825A calculator) will create four files in 1350A memory. File 0 will have 548 words allocated. Files 1, 2, and 3 will each have 500 words allocated. This "sectioning off" in 1350A memory provides a simple and efficient method for entering and updating file information without the confusion of nebulous file boundaries.

3-61. The required 1350A Initialization Sequence should precede the "dummy" program. Next, the Find Location (FL) and Find File (FF) commands may be used to enter data into files.

Example "dummy" program on an HP 9825A:

```
0: fmt 1,f4.0,","
1: wrt 718,"FL0000,:"
2: for F=1 to 3
3: wrt 718.1,"NF",F
4: for N=1 to 500
5: wrt 718,"pe0,:pa0,0;:"
6: next N
7: wrt 718,"SN:"
8: next F
9: end
```

3-62. Line 0 sets 9825A format so that any calculated variables are integers of up to four digits with no digits to the right of the decimal point. Line 1 moves 1350A memory write pointer to location zero. Lines 2 and 3 set up file names 1, 2, and 3. Lines 4 and 5 enter 500 "blank" locations into each file. Line 7 makes sure that each file is delimited before the next one is named.

NOTE

File 0 contains locations 0 thru 547.
File 1 contains locations 548 thru 1047.
File 2 contains locations 1048 thru 1547.
File 3 contains locations 1548 thru 2047.

3-63. EXAMPLE PROGRAMS.

3-64. The following example programs show how different controllers can be used to produce the same results in the 1350A. All of the following programs cause the 1350A to draw a triangle (from file 1) and place the text "1350A" (from file 16) on a CRT. Figure 3-4 shows the CRT display that results from any of the example programs.

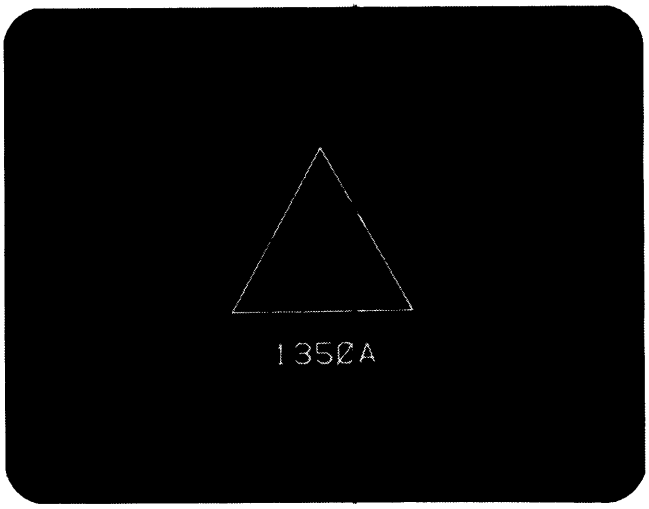


Figure 3-4. Display for Example Programs

9825A Example:

```
0: "clear the HP-IB":cli 7
1: "clear the 1350A":
2: wtb 718,3,20,"::em::en::ex::sn::sx::um::"
3: "draw a triangle in file 1":
4: wrt 718,"nf1,:pe0,:pa300,300;:pe1,:pa500,700;700,300;:"
5: wrt 718,"pa300,300;:sn::"
6: "write text into file 16":
7: wrt 718,"nf16,:pe0,:pa390,175;:pe1,:"
8: wtb 718,"cs2,:tx1350A",3,":sn:"
9: end
```

9835A and 9845A Example:

```
10 REM SET UP OUTPUT TO THE 1350A VIA HP-IB
20 PRINTER IS 7,18
30 REM CLEAR THE 1350A
40 PRINT CHR$(3),CHR$(20),"::EM::EN::EX::SN::SX::UM::"
50 REM DRAW A TRIANGLE IN FILE 1
60 PRINT "NF1,:PE0,:PA300,300;:PE1,:PA500,700;700,300;:"
70 PRINT "PA300,300;:SN::"
80 REM WRITE TEXT INTO FILE 16
90 PRINT "NF16,:PE0,:PA390,175;:PE1,:"
100 PRINT "CS2,:TX1350A",CHR$(3),":SN::"
110 PRINTER IS 16
120 STOP
130 END
```

HP system 1000 FORTRAN Example:

```
0001    FTN4,L
0002    C - - -       EXAMPLE FORTRAN PROGRAM FOR 1350A ON SYSTEM 1000
0003                  PROGRAM EXPLF
0004    C . . . . .   SET THE HPIB LU TO 11
0005                  LHPIB=11
0006    C . . . . .   SET THE 1350A LU TO 19
0007                  IPLT=19
0008    C . . . . .   CLEAR THE HPIB AND THE 1350A
0009                  CALL HPIB(IPLT,LHPIB)
0010    C . . . . .   DRAW A TRIANGLE IN FILE 1
0011                  WRITE(IPLT,1)
0012          1       FORMAT("NF1,:PE0,:PA300,300;:PE1,:PA500,700;700,300;300,300;:SN:")
0013    C . . . . .     WRITE TEXT INTO FILE 16
0014    C . . . . .       SET UP THE ETX CODE (UPPER HALF OF 16 BIT WORD)
0015                  IETX=3*256
0016                  WRITE(IPLT,2) IETX
0017          2       FORMAT("NF16,:PE0,:PA390,175;:PE1,:CS2,:TX1350A",A1,":SN:")
0018                  STOP
0019                  END
0020    C
0021    C - - - - - - - - - - - HPIB - - - - - - - - - - - - - - -
0022    C
0023    C  CLEARS THE HPIB AND THE 1350A, WHERE
0024    C         IPLT IS LU OF THE 1350A
0025    C         LHPIB IS LU OF THE HPIB I/O CARD, DRIVER 0
0026    C
0027                  SUBROUTINE HPIB (IPLT,LHPIB)
0028    C . . . . .   DO AN INTERFACE CLEAR TO THE CARD ITSELF
0029                  CALL EXEC(3,LHPIB)
0030    C . . . . .   SEND AN ASCII "ETX" + "DC4" AND CLEAR THE 1350A
0031    C . . . . .     ETX TAKES THE 1350A OUT OF TEXT MODE
0032    C . . . . .     DC4 CLEARS 1350A POWER INTERRUPT
0033                  I=01400B+24B
0034                  WRITE(IPLT,1) I
0035          1       FORMAT(A2,"EM:EN:EX:SN:SX:UM:")
0036                  RETURN
0037                  END
```

FTN4 COMPLIER: HP92060-16092 REV. 1901 (781201)

This program was written for a system equipped with RTE II-IV, Driver 37, and a 59310B I/O card. HP-IB is cleared (IFC line set low) by a CALL EXEC(3,LUHPIB) program statement. When a delay is necessary, use CALL EXEC(12,0,1,0,-n) where n = 100 times the desired number of milliseconds. For example, for a delay of 70 ms, use n = -7.

NOTE

3* 256 = 768 = 01400 in base 8. 20 in base 10 = 24 in base 8. The program statement I=01400B+24B sets ETX into the upper 8 bits and DC4 into the lower 8 bits of the computer word.

HP system 1000 BASIC Example:

```
10   REM        CLEAR THE HPIB AND 1350A INTERFACE
20   CALL    CLEAR(11,2)
30   REM       CLEAR THE 1350A
40   PRINT     #18;"EXD4:EM:EN:EX:SN:SX:UM:"
50   REM       DRAW THE TRIANGLE IN FILE 1
60   PRINT     #18;"NF1,:PE0,:PA300,300;:PE1,:PA500,700;700,300;300,300;:SN:"
70   REM       WRITE TEXT INTO FILE 16
80   PRINT     #18;"NF16,:PE0,:PA390,175;:PE1,:"
90   PRINT     #18;"CS2,:TX1350AEX:SN:"
100   STOP
110   END
```

The control characters (ETX = 3, DC4 = 20) are obtained by pressing the Control key (CNTL) and proper key at the same time.

3 = ETX = CNTL/C = C/C = E_X
20 = DC4 = CNTL/T = C/T = D_4

NOTE

To clear the HP-IB (IFC line set low), the HP-IB system command that can be loaded using RTETG is needed. RTETG is discussed in the HP BASIC/1000D manual, change 3, 4th Edition.

3-65. QUICK REFERENCE TO COMMANDS.

3-66. Table 3-8 lists 1350A commands in alphabetical order with a brief description of parameter ranges. For a more complete description, see the "Programming" paragraph and complete list of commands presented earlier in this section. For convenience when programming the 1350A, table 3-8 may be photo-copied for handy reference.

3-67. REDUCING CRT FLICKER.

3-68. In some applications the 1350A can be made to refresh the CRT more often in order to reduce flicker.

3-69. Presort and group data for minimum beam movement when producing the desired display. This reduces time spent "traveling back and forth" between displayed data and optimizes the display.

Table 3-8. Quick Reference to 1350A Commands

Command	Parameter(s)	Name
bfD,	D = 0 to 31	Blank File
bm	none	Blank Memory
csD,	D = 0 to 7	Character Size
efD,	D = 0 to 31	Erase File
em	none	Erase Memory
en	none	Erase Names
ex	none	Erase Auxiliary
ffD,	D = 0 to 31	Find Files
flD,	D = 0 to 2047	Find Location
nfD,	D = 0 to 31	Name File
paX,Y;	X = 0 to 1022 Y = 0 to 1023	Plot Absolute
peD,	D = 0 or 1	Pen Enable
sn	none	Stop Naming
sx	none	Stop Auxiliary
tx	ASCII characters	Text
ufD,	D = 0 to 31	Unblank File
um	none	Unblank Memory
wxD,	D = 0 to 31	Write Auxiliary

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. The procedures in this section provide an abbreviated test that provides approximately 90% assurance of proper 1350A operation.

4-3. EQUIPMENT REQUIRED.

4-4. The verification programs are written for an HP Model 9825A Calculating Controller equipped with Options: 98210A (String-Advanced Programming ROM); 98214A (9862A Plotter-General I/O-Extended I/O ROM); and 98034A (HP-IB Interface) with the 98034A set to "7". The comments that accompany the programs should allow them to be translated for use with other HP-IB Controllers (IEEE Std. 488-1978 "C1" capability). The X-Y display must satisfy the critical specifications listed in table 1-3.

NOTE

The performance test programs may be put on tape. This will save time and prevent errors whenever the tests are repeated.

4-5. PERFORMANCE TEST PROCEDURES.

4-6. PERFORMANCE VERIFICATION.

4-7. The following program assumes that the 1350A is set to its factory-set address of "18".

DESCRIPTION:

A sequence of program steps is sent to the 1350A via HP-IB. At appropriate points the program stops and the 1350A front panel or the display CRT is checked. These program steps exercise most 1350A functions.

EQUIPMENT:

HP-IB Controller	HP9825A
X-X Display	HP1311A

PROCEDURE:

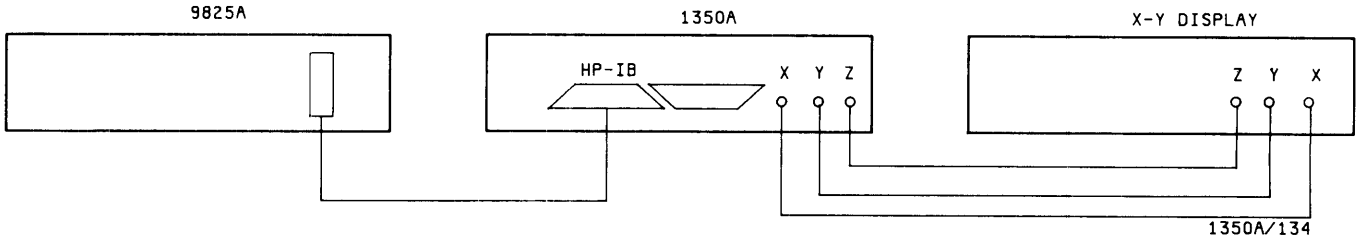


Figure 4-1. Performance Verification Test Setup

a. Connect 1350A X, Y, and Z outputs to display X, Y, and Z inputs.

b. Make sure that display is in 50 ohm input configuration. Also, make sure that display TTL blanking input has shorting cap installed on positive-going input.

c. Connect HP-IB cable from 9825A to rear of 1350A and secure. Equipment should now be as shown in figure 4-1.

d. Cycle the LINE power switches for the 9825A, the 1350A, and the X-Y display being used. Verify that random vectors are displayed by the display CRT.

PERFORMANCE TESTS

e. Enter the following program on the 9825A.

```
0: cli 7;wrt 718;beep;stp
1: wtb 718,"PA";beep;stp
2: wtb 718,3,20,13,10;beep;stp
3: wrt 718,"EM";beep;stp
4: wrt 718,"EM::EN::EX::SN::SX::UM::"
5: wrt 718,"PE1,:PA1022,1023;";beep;stp
6: wrt 718,"EM::EN::EX::SN::SX::UM::"
7: wtb 718,"PE0,:PA400,300;:PE1,:CS0,:TXB",3,13,10
8: wtb 718,"CS7,:TX S",3,13,10;beep;stp
9: wrt 718,"EM::EN::EX::SN::SX::UM::"
10: wrt 718,"NF0,:PE1,:PA800,300;:SN"
11: wrt 718,"NF31,:PA100,800;:SN";beep;stp
12: wrt 718,"BF0,";wait 1000;wrt 718,"BF31,";beep;stp
13: wrt 718,"EN::UF0,";beep;stp
14: wrt 718,"BM";wait 1000;wrt 718,"UM";beep
15: dsp "That's all FOLKS!!";wait 500;gto 14
16: end
```

f. Press 9825A RUN key. 9825A should make a "beep" sound. Verify that 1350A front-panel "LISTEN PROGRAM" LED is on.

Line 0: cli 7; sets HP-IB IFC line low to insure that the 1350A will handshake properly.
wrt 718; addresses 9825A to "talk" and 1350A to "listen".
beep; causes 9825A to make "beep" sound.
stp causes program to stop.

g. Press 9825A CONTINUE key. 9825A should beep. Verify that 1350A "LISTEN DATA" LED is on, "PROGRAM" LED is off.

line 1: wtb 718,"PA"; addresses 1350A to "listen" and sends two "program" instruction bytes without a terminating ":" (colon) or CR (Carriage Return) or LF (Line Feed). This fools the 1350A into staying in "listen for data".

h. Press 9825A CONTINUE key. Verify that 1350A POWER INTERRUPT LED has been turned off. ("PROGRAM" LED will be on.)

line 2: 3 (base 10) = ASCII ETX (End of Text) value in decimal.
This insures that the 1350A is not in Text mode.
20 = ASCII DC4 character to turn off POWER INTERRUPT.
13 = ASCII CR (Carriage Return) character.
10 = ASCII LF (Line Feed) character.

i. Press 9825A CONTINUE key. Verify that CRT is now blank.

line 3: "EM" erases Pen Enable and vector values from 1350A memory following random power-up.

j. Press 9825A CONTINUE key. Verify that CRT displays a diagonal vector from lower left corner to upper right corner.

line 4: initializes 1350A.
line 5: turns beam on and causes 1350A to draw the vector.

k. Press 9825A CONTINUE key. Verify that the vector is no longer displayed. Verify that the CRT displays a small "B" (not rotated) and a large "S" (rotated 90 degrees).

line 6: initializes 1350A (removes vector).
line 7: blanks beam while it is positioned; sets character size and rotation; unblanks beam; instructs 1350A to output a "B". (Note: 3 = ETX, 13 = CR, 10 = LF).
line 8: changes character size and rotation; instructs 1350A to output a " S" (space-S).

PERFORMANCE TESTS

l. Press 9825A CONTINUE key. Verify that the CRT displays two vectors that are roughly a ">" shape.

line 9: initializes 1350A (removes text).
line 10: places the bottom vector in File "0".
line 11: places the top vector in File "31".

m. Press 9825A CONTINUE key. Verify that the bottom vector is blanked first, and the top vector is blanked about one second afterward.

line 12: blanks contents of File "0" (bottom vector); waits about one second and then blanks the contents of File "31" (top vector).

n. Press 9825A CONTINUE key. Verify that both vectors are now displayed (">" pattern).

line 13: erases all file names so that all vectors are defaulted to File "0". Unblanks File "0" to display all vectors in 1350A memory.

o. Press 9825A CONTINUE key. Verify that ">" flashes on the CRT. The 9825A should display "That's all FOLKS!!" and beep periodically.

line 14: blanks 1350A memory to inhibit CRT; waits about one second; unblanks 1350A memory to enable CRT.
line 15: really not necessary. To get out of the loop, press 9825A STOP key. The "gto 14" causes CRT vector presentation to flash.

4-8. AUXILIARY (COLOR) VERIFICATION.

DESCRIPTION:

The following program is provided to quickly check 1350A color interface outputs when used with an HP 1338A Tri-color display. It should be used as an addition to the Performance Verification procedure shown above.

EQUIPMENT:

HP-IB Controller HP9825A
Tri-color Display HP1311A

PROCEDURE:

a. Connect Auxiliary cable from 1338A to rear of 1350A.
b. Connect HP-IB cable from 9825A to 1350A.
c. Connect 1350A X, Y, and Z to 1338A.
d. Make sure that 1338A X, Y, and Z inputs are in 50 ohm configuration.
e. Press 9825A [ERASE] [a] [EXECUTE] keys, if necessary, to clear 9825A memory. Enter the following program in the 9825A.

```
0: cli 7
1: wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
2: wrt 718,"NF1,:PE1,:PA1000,1000;:SN::"
3: wrt 718,"NF16,:PE1,:PA1000,0;:SN::"
4: wrt 718,"NF40,:PE1,:PA0,1000;:SN::"
5: end
```

f. Press 9825A RUN key. Verify that 1338A displays: (1) a green vector from lower left corner to upper right corner; (2) a yellow vector from upper right to lower right corners; and (3) a red vector from lower right corner to upper left corner.

line 0: sets IFC low.
line 1: initializes 1350A
line 2: uses File "1" to create the green vector.
line 3: uses File "16" to create the yellow vector.
line 4: uses File "40" to create the red vector.

SECTION V

ADJUSTMENTS

5-1. INTRODUCTION.

5-2. This section contains a complete adjustment procedure for the 1350A. The adjustment programs used in this section may be put on tape. This will save time and prevent errors whenever the adjustments are repeated.

WARNING

Read the Safety Summary at the front of this manual before performing adjustment procedures.

5-3. EQUIPMENT REQUIRED.

5-4. Test equipment is listed in the Recommended Test Equipment Table in Section I of this manual.

5-5. ADJUSTMENTS.

5-6. The power supply adjustment may be done separately following repairs or in sequence during periodic calibration. All other adjustments should be done in the sequence given.

ADJUSTMENTS

5-7. +5 VOLT POWER SUPPLY ADJUSTMENT.

REFERENCE:
Service Sheet 6B.

DESCRIPTION:
The +5 Vdc Power Supply is adjusted for an output of +4.95 Vdc.

EQUIPMENT:
DMM (Digital Multimeter) HP3476A

PROCEDURE:
a. Disconnect 1350A power cord.
b. Remove 1350A top and bottom covers (captive screw at rear of cover secures the cover).
c. Connect the (+) input of DVM to +5 V test point on Display Board. Connect (–) input of DVM to GND (figure 5-1).
d. Reconnect power cord and place LINE switch in "on" position.
e. Adjust A5R15 (figure 5-2) until DVM indicates +4.95 V (limits +4.93 to +4.97 V).

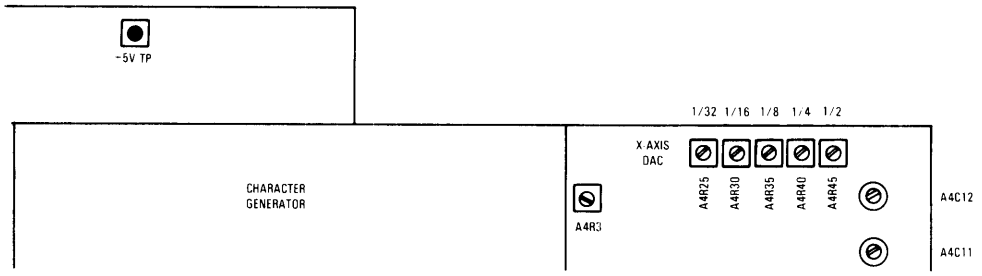


Figure 5-1. +5 V Test Point Location on Display Board

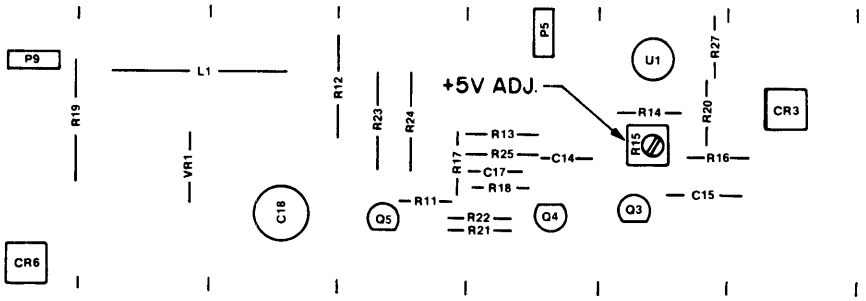


Figure 5-2. +5 V Adjustment Location on Power Supply

ADJUSTMENTS

5-8. Z-AXIS OUTPUT ADJUSTMENT.

REFERENCE:

Service Sheet 3E.

DESCRIPTION:

The 1350A rear-panel Z-AXIS output is adjusted for proper levels to insure uniform intensity for vectors of different lengths. The rear-panel Z-AXIS adjustment is then set for compatibility with the X-Y display being used.

EQUIPMENT:

HP-IB Controller	HP9825A
X-Y Display	HP1311A
Oscilloscope	HP1740A

PROCEDURE:

a. Connect 1350A X, Y, and Z outputs to display X, Y, and Z inputs.

b. Make sure that display in in 50 ohm input configuration. Also, make sure that display TTL blanking input has shorting cap installed.

c. Connect and secure HP-IB cable from 9825A to rear of 1350A. Equipment should appear as in figure 5-3.

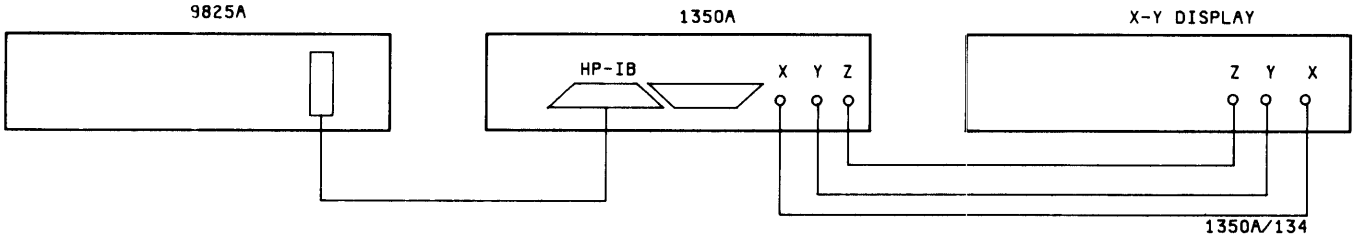


Figure 5-3. Equipment Setup

d. Cycle the LINE power switches on the 1350A, the 9825A, and the X-Y display. The CRT should display random vectors.

e. Connect oscilloscope probe to Z-axis output on Control Board (figure 5-4).

ADJUSTMENTS

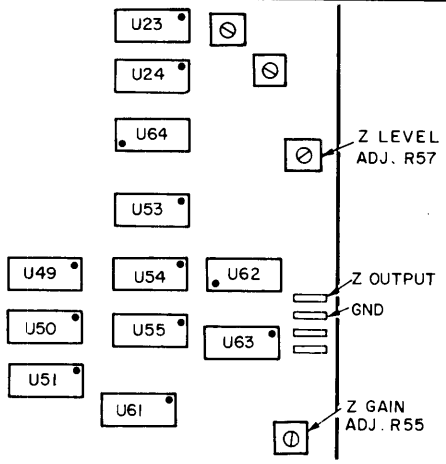


Figure 5-4. Z-axis Output and Adjustment Locations on Control Board

f. Enter the following program on the 9825A.

```
0: cli 7
1: wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
2: wrt 718,"PA31,31;:"
3: wrt 718,"PE1,:PA31,31;:"
4: wrt 718,"PA62,62;:"
5: end
```

g. Set 1350A rear-panel Z-AXIS control fully clockwise (CW).

h. Press 9825A RUN key.

i. Set Z LEVEL ADJ. A1R57 (see figure 5-4) so that the portion of the waveform marked "A" in figure 5-5 is at +40 mV.

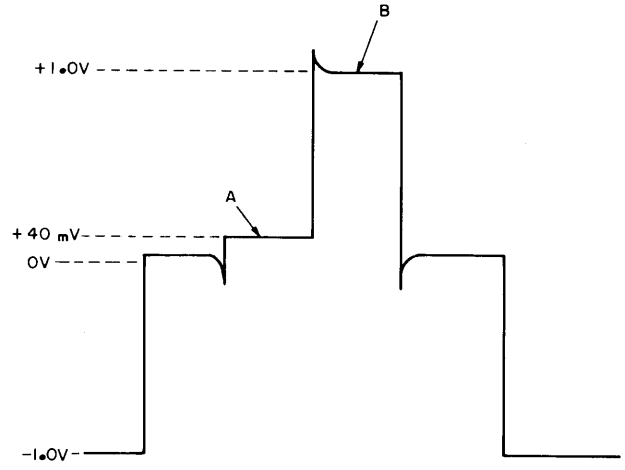


Figure 5-5. Z-axis Adjustment Waveform

j. Set Z GAIN LIMIT ADJ. A1R55 (see figure 5-4) so that the portion of the waveform marked "B" in figure 5-5 is at +1.0 V.

k. Cycle 1350A LINE power switch. The CRT should display random vectors.

l. Set X-Y Display INTENSITY control to minimum (full CCW).

m. Adjust 1350A rear-panel Z-AXIS control until random vectors are just extinguished.

n. Set X-Y Display INTENSITY control to normal viewing level.

ADJUSTMENTS

5-9. X-AXIS DAC ADJUSTMENTS.

REFERENCE:

Service Sheet 4E.

DESCRIPTION:

X-axis Digital-to-Analog Converter (DAC) circuits are adjusted to produce an even pattern on the CRT. This pattern is developed by a 9825A program. The 9825A loads 1350A memory. 1350A memory then drives the X-axis DAC.

EQUIPMENT:

HP-IB Controller HP9825A
X-Y Display HP1311A

PROCEDURE:

a. Connect equipment as shown in figure 5-3.

b. Enter the following program on the 9825A.

```
0: fmt f4.0,",",f4.0,";"
1: cli 7
2: wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
3: for T=0 to 1022 by 2
4: wrt 718,"PA",T,250;wrt 718,"PE1,:PA",T,450;wrt 718,"PE0,"
5: next T
6: dsp "X DAC Calibration";beep
7: end
```

c. Press 9825A RUN key. CRT should display a horizontal band of vectors.

d. Adjust X-axis digital-to-analog converter (DAC) to minimize gaps or overlapping for each adjustment (figure 5-6). The adjustments (figure 5-7) interact and should be done in the following sequence.

1) A4R25 ..... 1/32 screen
2) A4R30 ..... 1/16 screen
3) A4R35 ..... 1/8 screen
4) A4R40 ..... 1/4 screen
5) A4R45 ..... 1/2 screen

Readjust as necessary.

ADJUSTMENTS

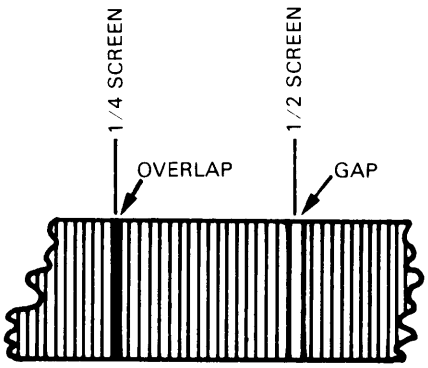


Figure 5-6. DAC Adjustment Indication on CRT

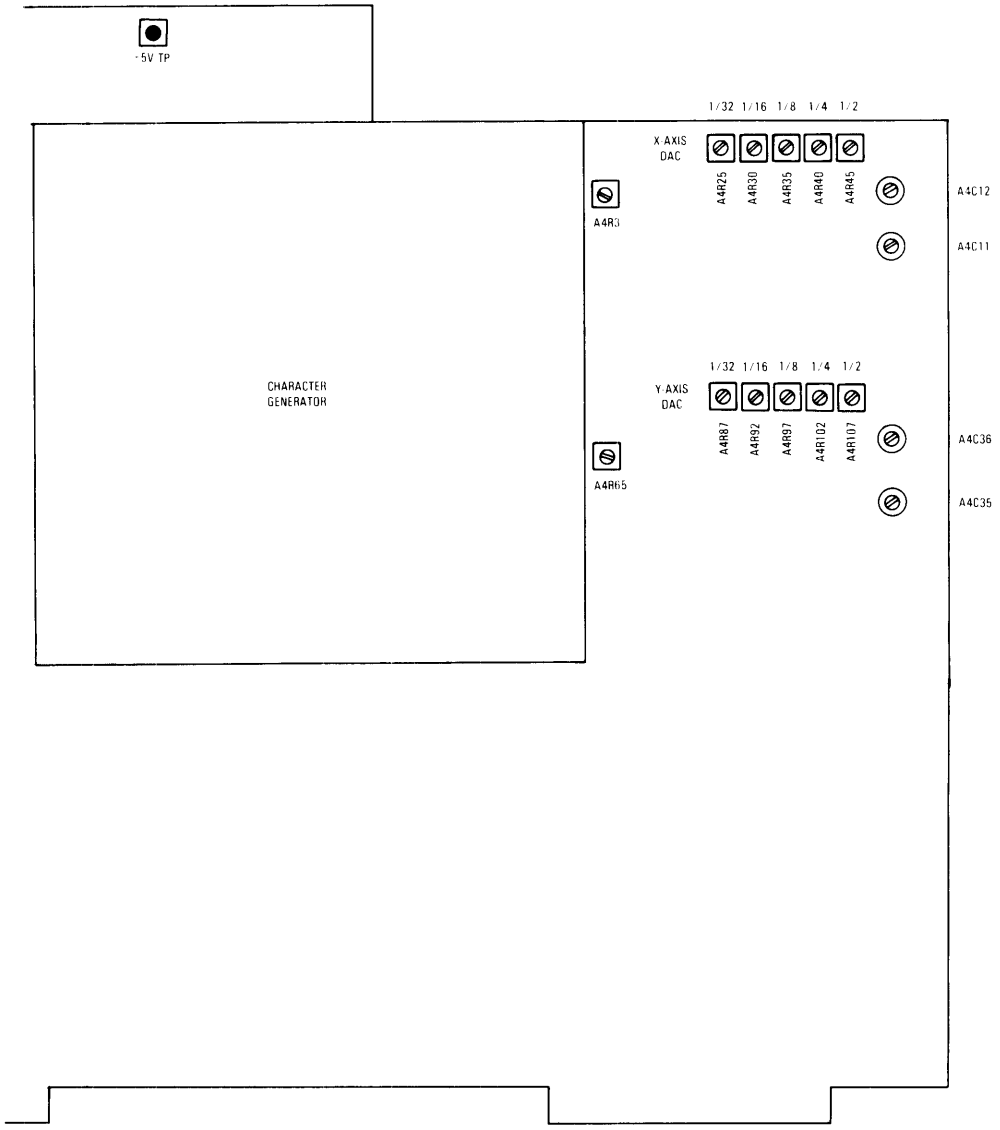


Figure 5-7. DAC Adjustment Locations on Display Board

ADJUSTMENTS

5-10. Y-AXIS DAC ADJUSTMENTS.

REFERENCE:
Service Sheet 4E.

DESCRIPTION:
Y-axis Digital-to-Analog Converter (DAC) circuits are adjusted to produce an even pattern on the CRT. This pattern is developed by a 9825A program. The 9825A loads 1350A memory. 1350A memory then drives the Y-axis DAC.

EQUIPMENT:
HP-IB Controller HP9825A
X-Y Display HP1311A

PROCEDURE:
a. Connect equipment as shown in figure 5-3.

b. Enter the following program on the 9825A.

```
0: fmt f4.0,",",f4.0,";"
1: cli 7
2: wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
3: for T=0 to 1022 by 2
4: wrt 718,"PA",250,T;wrt 718,"PE1,:PA",450,T;wrt 718,"PE0,"
5: next T
6: dsp "Y DAC Calibration";beep
7: end
```

c. Press 9825A RUN key. CRT should display a vertical band of vectors.

d. Adjust Y-axis digital-to-analog converter (DAC) to mimimize gaps or overlapping for each adjustment (figure 5-6). The adjustments (figure 5-7) interact and should be done in the following sequence.

1) A4R87 ..... 1/32 screen
2) A4R92 ..... 1/16 screen
3) A4R97 ..... 1/8 screen
4) A4R102 ..... 1/4 screen
5) A4R107 ..... 1/2 screen

Readjust as necessary.

5-11. DAC TIMING ADJUSTMENTS.

REFERENCE:
Service Sheet 4E.

DESCRIPTION:
The timing of the X and Y DACs is adjusted to minimize vector distortion. A 9825A program develops the vector pattern and loads 1350A memory. 1350A memory then drives the DACs.

EQUIPMENT:
HP-IB Controller HP9825A
X-Y Display HP1311A

PROCEDURE:

a. Connect equipment as shown in figure 5-3.

b. Enter the following program on the 9825A. (Note: The entry 2↑ means "2 raised to the".)

```
0: fmt f4.0,",",f4.0,";"
1: cli 7
2: wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
3: for V=7 to 9
4: wrt 718,"PE0,:PA",2↑V-8,520;wrt 718,"PE1,"
5: wrt 718,"PA",2↑V+8,570;wrt 718,"PA",2↑V-8,620;wrt 718,"PE0,"
6: wrt 718, "PA",520,2↑V-8;wrt 718,"PE1,:PA",570,2↑V+8
7: wrt 718,"PA",620,2↑V-8;wrt 718,"PE0,"
8: next V
9: dsp "Check DAC Timing Adjustments";beep
10: end
```

c. The CRT will display six pointed vectors as shown in figure 5-8.

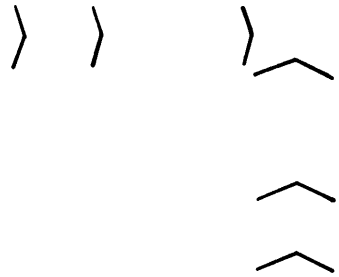


Figure 5-8. DAC Timing Adjustment CRT display

d. Adjust the vectors for minimum distortion as shown in figure 5-8. Figure 5-9 shows undesired vector shapes. The adjustments (figure 5-7) interact and should be done in the following sequence.

1) A4C11 ..... X axis
2) A4C12 ..... X axis
3) A4R3 ..... X axis
4) A4C35 ..... Y axis
5) A4C36 ..... Y axis
6) A4R65 ..... Y axis

Readjust as necessary.

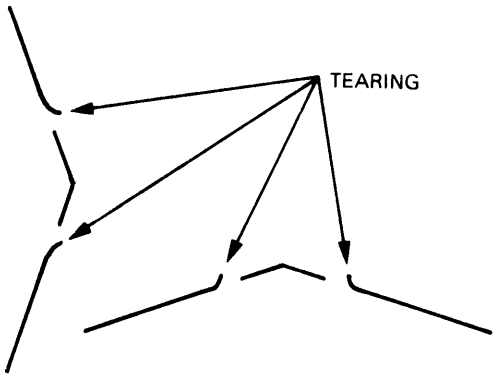


Figure 5-9. Undesired vector shape for DAC timing

ADJUSTMENTS

5-12. POINT BLANKING ADJUSTMENTS.

REFERENCE:
Service Sheet 3E.

DESCRIPTION:
Point blanking is adjusted to provide the proper Z-axis blanking interval between vectors.

EQUIPMENT:
HP-IB Controller HP9825A
X-Y Display HP1311A

PROCEDURE:
a. Connect equipment as shown in figure 5-3.

b. Enter the following program on the 9825A.

```
0: cli 7
1: wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
2: wrt 718,"PE0,:PA0,500;"
3: wtb 718,"PE1,:CS1,:TX**********",3,13,10
4: dsp "Blanking Adj.";beep
5: end
```

c. Press 9825A RUN key. CRT should display a horizontal line of asterisks (*).

d. Adjust A1R37 and A1R39 (figure 5-10) so that the asterisks have proper shape and uniform intensity.

e. Change position of point blanking switch (figure 5-10). Shape and intensity of the asterisks should not change. Readjust if necessary until no change. Return switch to forward position.

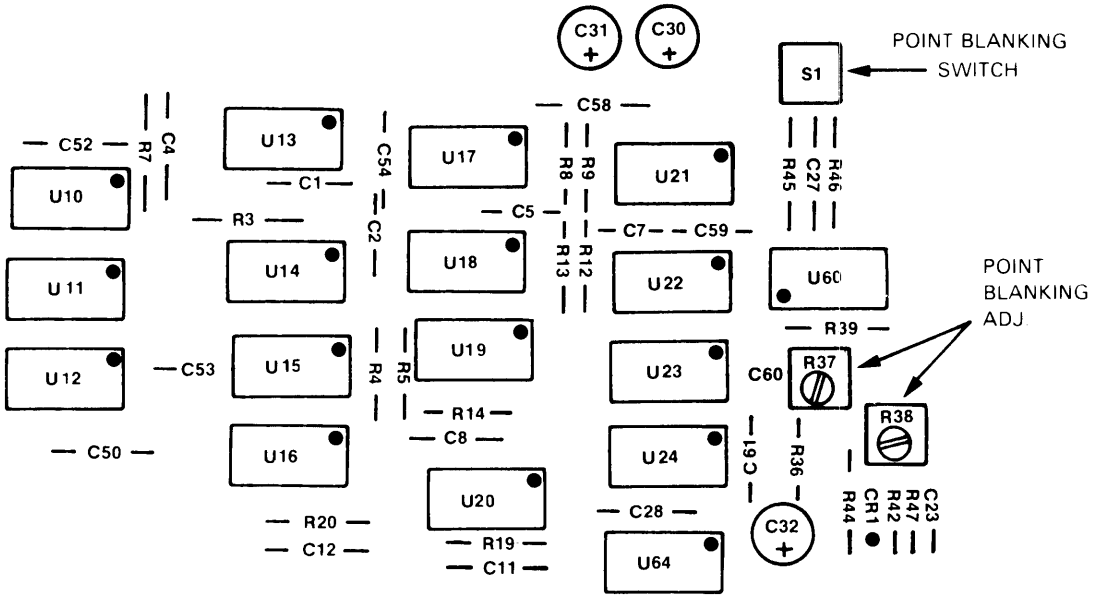


Figure 5-10. Point Blanking Switch and Adjustment Locations on Control Board

ADJUSTMENTS

5-13. TTL BLANKING ADJUSTMENT.

REFERENCE:
Service Sheet 2D.

DESCRIPTION:
TTL output timing is adjusted to prevent Blank/Blink changes while the 1350A is drawing a vector.

EQUIPMENT:
HP-IB Controller HP9825A
X-Y Display HP1311A

PROCEDURE:

a. Connect equipment as shown in figure 5-3.

b. Remove shorting cap from X-Y display TTL blanking positive-going input.

c. Connect 1350A TTL1 output to X-Y display TTL blanking positive-going input.

d. Enter the following program on the 9825A.

```
0: cli 7
1: wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::UM::"
2: wrt 718,"PE0,:PA100,400;"
3: wrt 718,"PE1,:PA900,400;"
4: wrt 718,"WX1,:PA100,600;900,600;900,600;:SX"
5: dsp "Check TTL Blanking Timing Adj.";beep
6: end
```

e. Set Blink Switch A3S2 section 1 (figure 5-11) to "on" position.

f. Press 9825A RUN key. CRT should display a horizontal line.

g. Adjust Blanking Delay A3R43 (figure 5-12) on Input/Output Board until a spot directly above the right end of the horizontal line is extinguished.

NOTE

This adjustment is performed at normal viewing intensity.

ADJUSTMENTS

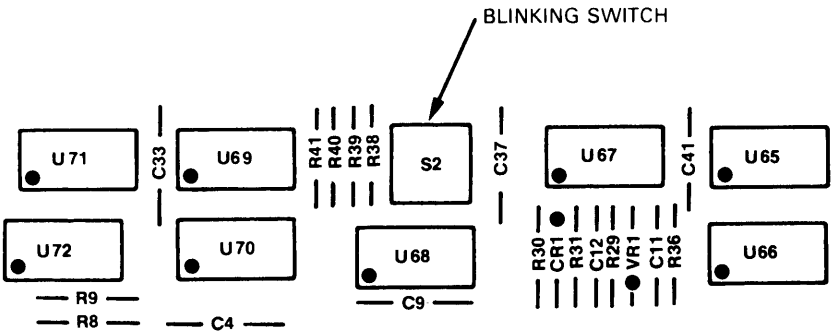


Figure 5-11. Blinking Switch Location on Input/Output Board

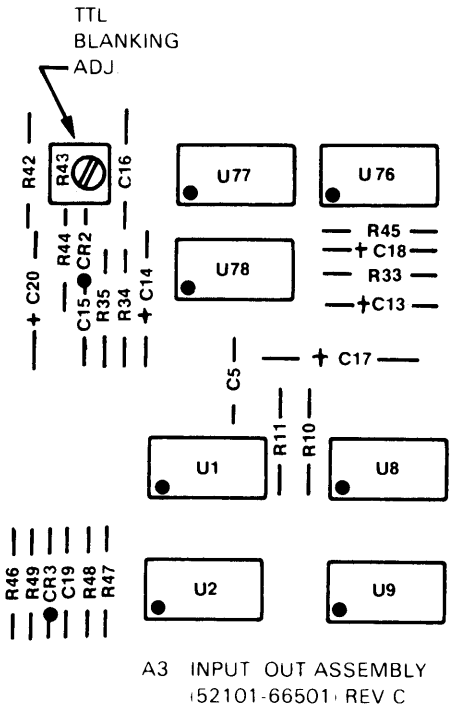


Figure 5-12. Blanking Delay Adjustment Location on Input/Output Board

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts. Table 6-1 lists abbreviations used in the parts list. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturer's code numbers. Figure 6-1 shows the illustrated parts breakdown.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics, and throughout the manual. In some cases, two forms of the abbreviations are used: one in all capital letters and one partial or no capitals. This occurs because the abbreviations in the parts list are always in capitals. However, in other parts of the manual other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS LIST.

6-6. Table 6-2 is the list of replaceable parts and is organized as follows:

a. Electrical assemblies in alphanumerical order by reference designation.

b. Chassis-mounted parts in alphanumerical order by reference designation.

c. Electrical assemblies and their components in alphanumerical order by reference designation.

The information given for each part consists of the following:

a. Reference designation.

b. Hewlett-Packard part number.

c. Part number Check Digit (CD).

d. Total quantity (Qty) in instrument (or on assembly).

e. Description of part.

f. Typical manufacturer of part in an identifying five-digit code.

g. Manufacturer's number for the part.

The total quantity for each part is given only once - at the first appearance of the part number in the list.

6-7. ORDERING INFORMATION.

6-8. To order a part listed in the material lists, quote the Hewlett-Packard part number, indicate the quantity desired, and address the order to the nearest Hewlett-Packard Sales/Service Office.

6-9. To order a part that is not listed in the material lists, include the instrument model number, instrument serial number, a description of the part (including its function), and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-10. DIRECT MAIL ORDER SYSTEM.

6-11. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using this system are:

a. Direct ordering and shipment from the HP Parts Center in Mountain View, California.

b. No maximum or minimum on any mail order (there is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing).

c. Prepaid transportation (there is a small handling charge for each order).

d. No invoices.

To provide these advantages, a check or money order must accompany each order.

6-12. Mail order forms and specific ordering information is available through your local HP office. Addresses and phone numbers are located at the back of this manual.

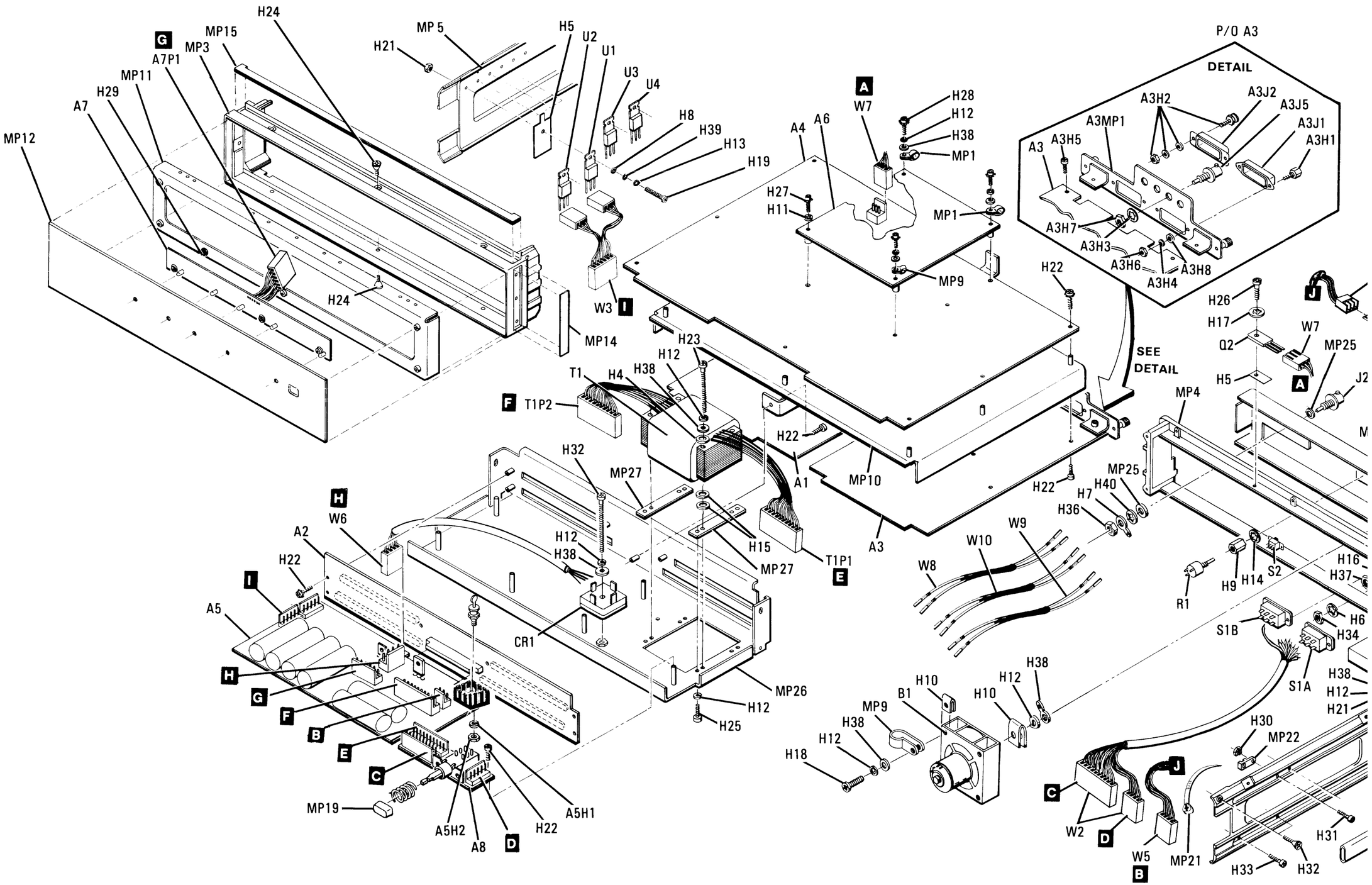
Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without


H24
MP15
MP3
A7P1
MP11
H29
A7
MP12
MP 5
H21
H5
U2
U1
U3
U4
H8
H39
H13
H19
H24
W3
I
MP14
A
W7
H28
H12
H38
MP1
A4
A6
H27
H11
MP1
MP9
H22
P/O A3
DETAIL
A3H2
A3J2
A3J5
A3MP1
A3J1
A3H1
A3
A3H5
A3H7
A3H3
A3H6
A3H8
A3H4
SEE DETAIL
H26
H17
J
W7
Q2
MP25
H5
A
J2
MP4
M
T1
H4
H38
H12
H23
F
T1P2
H22
A1
MP10
A3
H22
H22
MP25
H40
H7
H36
H32
MP27
H
W6
A2
H12
H38
H15
MP27
T1P1
E
W10
W9
W8
R1
H9
H14
S2
H16
H37
H22
I
A5
CR1
S1B
H6
H34
S1A
H38
H12
H21
H
G
F
B
E
C
MP26
H12
H25
H10
B1
H10
H12
H38
MP9
H38
H12
H18
H30
MP22
C
W2
D
J
W5
B
MP21
H31
H33
H32
MP19
A5H2
A8
D
H22
A5H1

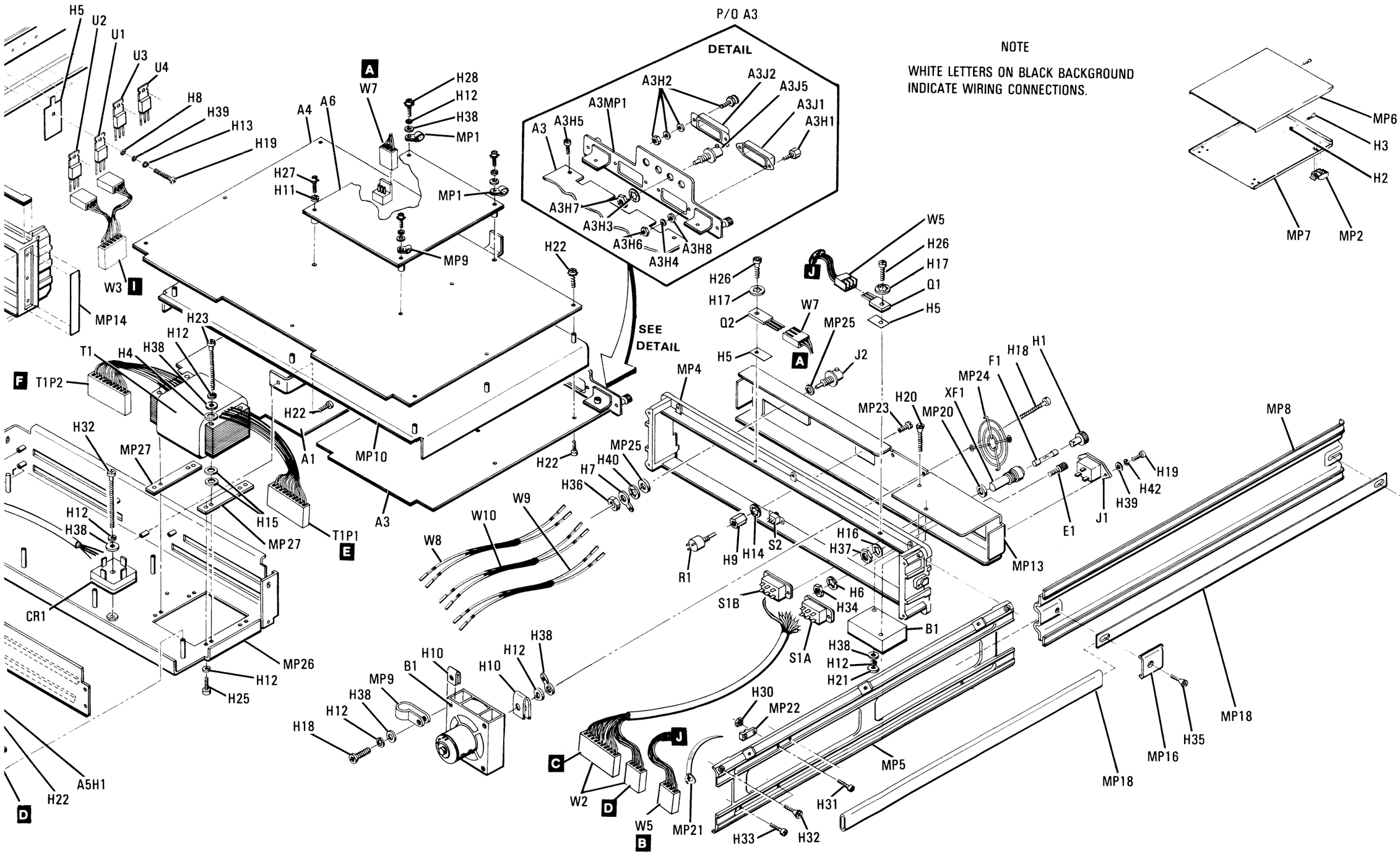


Figure 6-1.
Chassis Parts and Board Assy Identification

Table 6-2. Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01350-66514	0		CONTROL BOARD ASSEMBLY	28480	01350-66514
A2	01350-66505	9		INTERCONNECTION BOARD ASSEMBLY	28480	01350-66505
A3	52101-66504	4		I/O BOARD ASSEMBLY	28480	52101-66504
A4	01350-66511	7		DISPLAY BOARD ASSEMBLY	28480	01350-66511
A5	01350-66515	1		POWER SUPPLY BOARD ASSEMBLY	28480	01350-66515
A6	01350-66512	8		CHARACTER BOARD ASSEMBLY	28480	01350-66512
A7	01350-66506	0		LED BOARD ASSEMBLY	28480	01350-66506
A8	01350-66507	1		LINE SWITCH ASSEMBLY	28480	01350-66507
B1	3160-0303	9	1	FAN-TBAX 47-CFM 6-16VDC	28480	3160-0303
CR1	1906-0093	4	1	DIODE-FW BRDG 100V 35A	04713	MDA3501
E1	1510-0038	8	1	BINDING POST ASSY SGL THD-STUD	28480	1510-0038
F1	2110-0020	1	1	FUSE .8A 250V SLO-BLO 1.25X.25 UL (FOR 220-240V OPERATION)	75915	313.800
F1	2110-0059	6	1	FUSE 1.5A 250V SLO-BLO 1.25X.25 UL (FOR 110-120V OPERATION)	71400	MDX 1-1/2
H1	2110-0465	8	1	FUSEHOLDER CAP EXTR PST; BAYONET; 20A	28480	2110-0465
H2	0510-0043	4	2	RETAINER-RING E-R EXT .141-IN-DIA STL	28480	0510-0043
H3	0570-1171	7	2	SCREW-SPCL 6-32 .406-IN-LG UNCT 100	28480	0570-1171
H4	0340-0114	9	8	INSULATOR-FLG-BSHG NYLON	28480	0340-0114
H5	0340-0614	4	6	INSULATOR-XSTR ALUMINUM HD-ANDZ	28480	0340-0614
H6	0360-0040	2	1	TERMINAL-SLDR LUG LK-MTG FOR-#1/4-SCR	28480	0360-0040
H7	0360-1632	0	3	TERMINAL-SLDR LUG LK-MTG FOR-#3/8-SCR	28480	0360-1632
H8	3050-0791	6	4	INSULATOR-XSTR NYLON	28480	3050-0791
H9	0590-0043	2	1	NUT-HEX-DBL-CHAM 1/4-32-THD .375-IN-THK	00000	ORDER BY DESCRIPTION
H10	0590-0127	3	5	NUT-SHMET-U-TP 4-40-THD .25-WD STL	28480	0590-0127
H11	2190-0007	2	1	WASHER-LK INTL T NO. 6 .141-IN-ID	28480	2190-0007
H12	2190-0018	5	8	WASHER-LK HLCL NO. 6 .141-IN-ID	28480	2190-0018
H13	2190-0019	6	8	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0019
H14	2190-0027	6	2	WASHER-LK INTL T 1/4 IN .256-IN-ID	28480	2190-0027
H15	3050-0055	5	8	WASHER-FL MTLC NO. 8 .188-IN-ID	28480	3050-0055
H16	2190-0102	8	1	WASHER-LK INTL T 15/32 IN .472-IN-ID	28480	2190-0102
H17	2190-0909	3	2	WASHER-LK INTL T NO. 6 .146-IN-ID	28480	2190-0909
H18	2200-0123	6	4	SCREW-MACH 4-40 1.25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H19	2200-0143	0	3	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H20	2200-0171	4	2	SCREW-MACH 4-40 .75-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
H21	2260-0001	5	11	NUT-HEX-DBL-CHAM 4-40-THD .094-IN-THK	28480	2260-0001
H22	2360-0115	4	35	SCREW-MACH 6-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H23	2360-0139	2	4	SCREW-MACH 6-32 2-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H24	2360-0190	5	6	SCREW-MACH 6-32 .188-IN-LG 100 DEG	00000	ORDER BY DESCRIPTION
H25	2360-0197	2	5	SCREW-MACH 6-32 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H26	2360-0201	9	1	SCREW-MACH 6-32 .5-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H27	2360-0207	5	1	SCREW-MACH 6-32 .875-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H28	2360-0209	7	3	SCREW-MACH 6-32 1-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H29	2420-0001	5	8	NUT-HEX-W/LKWR 6-32-THD .109-IN-THK	00000	ORDER BY DESCRIPTION
H30	2500-0003	7	3	NUT-HEX-DBL-CHAM 6-32-THD .047-IN-THK	00000	ORDER BY DESCRIPTION
H31	2510-0101	7	3	SCREW-MACH 8-32 .312-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
H32	2510-0192	6	8	SCREW-MACH 8-32 .25-IN-LG 100 DEG	28480	2510-0192
H33	2510-0193	7	14	SCREW-MACH 8-32 .375-IN-LG PAN-HD-POZI	28480	2510-0193
H34	2580-0003	5	3	NUT-HEX-W/LKWR 8-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H35	2680-0172	1	4	SCREW-MACH 10-32 .375-IN-LG 100 DEG	28480	2680-0172
H36	2950-0001	8	3	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
H37	2950-0054	1	3	NUT-HEX-DBL-CHAM 1/2-28-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
H38	3050-0066	8	12	WASHER-FL MTLC NO. 6 .147-IN-ID	28480	3050-0066
H39	3050-0235	3	11	WASHER-FL MTLC NO. 4 .117-IN-ID	28480	3050-0235
H40	3050-0580	1	1	WASHER-FL MTLC 10-MM-ID 16-MM-OD BRS	28480	3050-0580
H41	0362-0227	1	4	CONNECTOR-SGL CONT SKT 1.14-MM-BSC-SZ	28480	0362-0227
J1	1251-4470	0	1	CONNECTOR-AC PWR CEE-22 MALE REC-FLG	28480	1251-4470
J2	1250-0118	3	3	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
J3	1250-0118	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
J4	1250-0118	3		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0118
MP1	1400-0024	9	2	CLAMP-CABLE .25-DIA .5-WD NYL	28480	1400-0024
MP2	5040-7201	8	4	FOOT(STANDARD)	28480	5040-7201
MP3	5020-8801	4	1	FRAME, FRONT, FULL	28480	5020-8801
MP4	5020-8802	5	1	FRAME, REAR	28480	5020-8802
MP5	5020-8887	6	2	SIDE STRUT 18"	28480	5020-8887
MP6	5060-9835	0	1	TOP COVER	28480	5060-9835
MP7	5060-9847	4	1	BOTTOM COVER	28480	5060-9847
MP8	5060-9876	9	2	SIDE COVER - WITH HANDLE	28480	5060-9876
MP9	1400-0053	4	2	CLAMP-CABLE .172-DIA .375-WD NYL	28480	1400-0053
MP10	01350-00103	5	1	DECK, MAIN	28480	01350-00103

See introduction to this section for ordering information
*Indicates factory selected value

PART NUMBER 9320-3991

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
MP11	01350-00201	4	1	PANEL, FRONT	28480	01350-00201
MP12	01350-00202	5	1	PANEL, DRESS	28480	01350-00202
MP13	01350-00204	7	1	PANEL, REAR	28480	01350-00204
MP14	5001-0438	7	2	TRIM, SIDE	28480	5001-0438
MP15	5040-7202	9	1	TRIM, TOP	28480	5040-7202
MP16	5040-7219	8	4	STRAP, HANDLE, CAP-FRONT	28480	5040-7219
MP17	5040-7220	1	4	STRAP, HANDLE, CAP-REAR	28480	5040-7220
MP18	5060-9804	3	2	HANDLE STRAP	28480	5060-9804
MP19	5041-0235	6	1	KEY CAP, BLANK	28480	5041-0235
MP20	1400-0090	9	1	FUSEHOLDER COMPONENT - NEOPRENE WASHER	28480	1400-0090
MP21	1400-0265	0	3	CABLE TIE 1.75-DIA .19-WD NYL	28480	1400-0265
MP22	1400-0786	0	3	MOUNT-CA TIE .19-DIA .375-WD NYL	59730	TC112
MP23	1490-0968	9	1	BUSHING-PNL .14-ID .3-LG 1/4-32-THD	28480	1490-0968
MP24	3160-0305	1	1	FINGER GUARD	28480	3160-0305
MP25	5040-0702	0	6	INSULATOR:CONNECTOR	28480	5040-0702
MP26	01350-00105	7	1	DECK, POWER	28480	01350-00105
MP27	01350-04702	8	2	SPACER, TRANSFORMER	28480	01350-04702
Q1	1854-0433	5	1	TRANSISTOR NPN SI PD=90W FT=2MHZ	28480	1854-0433
Q2	1854-0558	5	1	TRANSISTOR NPN SI DARL PD=70W FT=1MHZ	28480	1854-0558
R1	2100-2083	9	1	RESISTOR-VAR CONTROL CCP 20K 20% LIN	28480	2100-2083
S1A	3101-2042	3	2	SWITCH-SL DPDT STD 2A 250VAC SLDR-LUG	28480	3101-2042
S1B	3101-2042	3		SWITCH-SL DPDT STD 2A 250VAC SLDR-LUG (LINE SELECT SWITCH)	28480	3101-2042
S2	3101-1787	1	1	SWITCH-SL DPDT SUBMIN .5A 125VAC/DC (LINE SYNCH SWITCH)	28480	3101-1787
T1	9100-4013	6	1	TRANSFORMER-POWER 100/120/220/240V	28480	9100-4013
T1P1	1251-3537	8	3	CONNECTOR 10-PIN F POST TYPE	28480	1251-3537
P1P2	1251-3537	8		CONNECTOR 10-PIN F POST TYPE	28480	1251-3537
T1P1E1	1251-3073	7	26	CONTACT-CONN U/W-POST-TYPE FEM CRP	28480	1251-3073
U1	1826-0106	0	1	IC 7815 V RGLTR TO-220	04713	MC7815CP
U2	1826-0147	9	1	IC 7812 V RGLTR TO-220	04713	MC7812CP
U3	1826-0214	1	1	IC V RGLTR TO-220	04713	MC7915CT
U4	1826-0294	7	1	IC V RGLTR TO-220	04713	MC7905CT
W1	8120-2061	6	1	CABLE ASSY 18AWG 3-CNDCT BLK-JKT	28480	8120-2061
W2	01350-61601	6	1	CABLE, POWER	28480	01350-61601
W2P1	1251-0512	3	1	CONNECTOR 5-PIN F POST TYPE	28480	1251-0512
W2P2	1251-3537	8	3	CONNECTOR 10-PIN F POST TYPE	28480	1251-3537
W2P2E1	1251-3073	7		CONTACT-CONN U/W-POST-TYPE FEM CRP	28480	1251-3073
W3	01350-61605	0	2	CABLE, TRANS CONN	28480	01350-61605
W4	01350-61605	0		CABLE, TRANS CONN	28480	01350-61605
W5	01350-61612	9	1	CABLE ASSEMBLY	28480	01350-61612
W6	01350-61613	0	1	CABLE ASSEMBLY	28480	01350-61613
W7	01350-61606	1	1	CABLE, TRANS CONN	28480	01350-61606
W8	01350-61610	7	1	CABLE ASSEMBLY, OUTPUT (Z)	28480	01350-61610
W9	01350-61608	3	1	CABLE ASSEMBLY, OUTPUT (X)	28480	01350-61608
W10	01350-61609	4	1	CABLE ASSEMBLY, OUTPUT (Y)	28480	01350-61609
XF1	2110-0470	5	1	FUSEHOLDER BODY EXTR PST; BAYONET; TND	75915	345003-010
				MISCELLANEOUS PARTS		
	6040-0239	9		LUBRICANT-GREASE SIL	05820	120

See introduction to this section for ordering information
*Indicates factory selected value

PART NUMBER 9320-3991

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	01350-66514	0	1	CONTROL BOARD ASSEMBLY	28480	01350-66514
A1C1	0160-2331	4	2	CAPACITOR-FXD 8200PF +-1% 100VDC MICA	28480	0160-2331
A1C2	0160-2204	0	5	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A1C3	0160-2218	6	1	CAPACITOR-FXD 1000PF +-5% 300VDC MICA	28480	0160-2218
A1C4	0160-2331	4		CAPACITOR-FXD 8200PF +-1% 100VDC MICA	28480	0160-2331
A1C5	0160-2199	2	3	CAPACITOR-FXD 30PF +-5% 300VDC MICA	28480	0160-2199
A1C6	0160-2201	7	8	CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A1C7	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A1C8	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A1C9	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A1C10	0160-3768	3	1	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-3768
A1C11	0160-2215	3	1	CAPACITOR-FXD 750PF +-5% 300VDC MICA	28480	0160-2215
A1C12	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A1C13	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A1C14	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A1C15	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A1C16	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A1C17	0160-2012	8	1	CAPACITOR-FXD 330PF +-5% 500VDC MICA	28480	0160-2012
A1C18	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A1C19	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A1C20	0160-2055	9	33	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C21	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A1C22	0140-0149	6	1	CAPACITOR-FXD 470PF +-5% 300VDC MICA	72136	DM15F471J0300WV1CR
A1C23	0160-2199	2		CAPACITOR-FXD 30PF +-5% 300VDC MICA	28480	0160-2199
A1C24	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C26	0140-0202	2	2	CAPACITOR-FXD 15PF +-5% 500VDC MICA	72136	DM15C150J0500WV1CR
A1C27	0160-2199	2		CAPACITOR-FXD 30PF +-5% 300VDC MICA	28480	0160-2199
A1C28	0140-0202	2		CAPACITOR-FXD 15PF +-5% 500VDC MICA	72136	DM15C150J0500WV1CR
A1C29	0180-1714	7	1	CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X9006B2
A1C30 - 33	0180-0423	3	4	CAPACITOR-FXD 100UF+50-10% 25VDC AL	28480	0180-0423
A1C34	0160-2242	6	1	CAPACITOR-FXD 2.4PF +-.25PF 500VDC CER	28480	0160-2242
A1C35	0140-0178	1	1	CAPACITOR-FXD 560PF +-2% 300VDC MICA	72136	DM15F561G0300WV1CR
A1C36 - 65	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1CR1	1901-0179	7	1	DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A1L1	9100-3139	5	1	COIL 75UH 15% .5DX.875LG-NOM	28480	9100-3139
A1Q1	1854-0404	0	1	TRANSISTOR NPN SI TO-18 PD=360MW	28480	1854-0404
A1R1	0683-2725	8	15	RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R2	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R3	0698-3158	4	1	RESISTOR 23.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2372-F
A1R4	0683-4715	0	5	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R5	0683-3915	0	1	RESISTOR 390 5% .25W FC TC=-400/+600	01121	CB3915
A1R6	0684-2711	4	2	RESISTOR 270 10% .25W FC TC=-400/+600	01121	CB2711
A1R7	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A1R8	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R9	0683-2225	3	11	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R10	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R11	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R12	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R13	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R14	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R15	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R16	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R17	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R18	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R19	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R20	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R21	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R22	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R23	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R24	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R25	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R26	0757-0401	0	2	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R27	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R28	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R29	0684-2711	4		RESISTOR 270 10% .25W FC TC=-400/+600	01121	CB2711
A1R30	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R31	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R32	0757-0280	3	5	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R33	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R35	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A1R36	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R37	2100-3253	7	2	RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	28480	2100-3253
A1R38	2100-3253	7		RESISTOR-TRMR 50K 10% C TOP-ADJ 1-TRN	28480	2100-3253
A1R39	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R40	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A1R41	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R42	0757-0278	9	1	RESISTOR 1.78K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1781-F
A1R43	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A1R44	0757-0408	7	1	RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-T0-243R-F
A1R45	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R46	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R47	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R48	0757-0438	3	1	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A1R49	0757-1000	7	1	RESISTOR 51.1 1% .5W F TC=0+-100	28480	0757-1000
A1R50	0698-5418	3	1	RESISTOR 50 .1% .125W F TC=0+-50	28480	0698-5418
A1R51	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R52	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R53	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A1R54	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A1R55	2100-0558	9	1	RESISTOR-TRMR 20K 10% C TOP-ADJ 1-TRN	28480	2100-0558
A1R56	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A1R57	2100-3210	6	1	RESISTOR-TRMR 10K 10% C TOP-ADJ 1-TRN	28480	2100-3210
A1S1	3101-1341	3	1	SWITCH-SL SPDT SUBMIN .5A 125VAC/DC	28480	3101-1341
A1U1	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
A1U2	1820-0686	9	2	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A1U3	1820-1077	4	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A1U4	1820-0693	8	7	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U5	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U6	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U7	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A1U8	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U9	1820-1449	4	2	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A1U10	1820-1112	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A1U11	1820-0688	1	1	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
A1U12	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U13	1820-1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1U14	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U15	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U16	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U17	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
A1U18	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U19	1820-1212	9	1	IC FF TTL LS J-K NEG-EDGE-TRIG	01295	SN74LS112N
A1U20	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A1U21	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
A1U22	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
A1U23	1820-1453	0	1	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
A1U24	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U25	1820-1196	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U26	1820-0511	9	3	IC GATE TTL AND QUAD 2-INP	01295	SN7408N
A1U27	1820-0511	9		IC GATE TTL AND QUAD 2-INP	01295	SN7408N
A1U28	1820-0511	9		IC GATE TTL AND QUAD 2-INP	01295	SN7408N
A1U29	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A1U30	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A1U31	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U32	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U33	1820-1470	1	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A1U34	1820-1206	1	2	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
A1U35	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A1U36	1820-1207	2	1	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A1U37	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U38	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A1U39	1820-1202	7	3	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U40	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U41	1820-1144	6	3	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U42	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A1U43	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A1U44	1820-1206	1		IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
A1U45	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
A1U46	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A1U47	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U48	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U49	1820-1440	5	1	IC LCH TTL LS QUAD	01295	SN74LS279N
A1U50	1820-1202	7		IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U51	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A1U53	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U54	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U55	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A1U60	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A1U61	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A1U62	1826-0188	8	1	IC CONV 8-B-D/A 16-DIP-C	04713	MC1408L-8
A1U63	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A1U64	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A1U65	1826-0081	0	1	IC OP AMP WB TO-99	27014	LM318H
				A1 MISCELLANEOUS PARTS		
	0360-1653	5	11	CONNECTOR-SGL CONT PIN .045-IN-BSC-8Z SQ	28480	0360-1653
	0360-1788	7	4	CONNECTOR-SGL CONT PIN .045-IN-BSC-8Z SQ	28480	0360-1788
	1205-0235	0	1	HEAT SINK SGL TO-18-CS	28480	1205-0235
A2	01350-66505	9	1	INTERCONNECTION BOARD ASSEMBLY	28480	01350-66505
A2XA1P1	1251-5088	8	2	CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-5088
A2XA3P1	1251-5088	8		CONNECTOR-PC EDGE 50-CONT/ROW 2-ROWS	28480	1251-5088
A2XA4P1	1251-5087	7	2	CONNECTOR-PC EDGE 40-CONT/ROW 2-ROWS	28480	1251-5087
A2XA4P2	1251-5087	7		CONNECTOR-PC EDGE 40-CONT/ROW 2-ROWS	28480	1251-5087
A2XA5P1	1251-1886	6	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	28480	1251-1886
A3	52101-66504	4	1	I/O BOARD ASSEMBLY	28480	52101-66504
A3C1	0160-3443	1	27	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C2	0160-2201	7	7	CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C3	0140-0220	4	1	CAPACITOR-FXD 200PF +-1% 300VDC MICA	72136	DM15F201F0300WV1CR
A3C4	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C5	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C6	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C7	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C8	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C9	0160-2201	7		CAPACITOR-FXD 51PF +-5% 300VDC MICA	28480	0160-2201
A3C10	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C11	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C12	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C13	0180-0161	6	3	CAPACITOR-FXD 3.3UF+-10% 35VDC TA	28480	0180-0161
A3C14	0180-0161	6		CAPACITOR-FXD 3.3UF+-10% 35VDC TA	28480	0180-0161
A3C15	0160-3768.	3	1	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-3768
A3C16	0160-2197	0	1	CAPACITOR-FXD 10PF +-5% 300VDC MICA	28480	0160-2197
A3C17	0180-0161	6		CAPACITOR-FXD 3.3UF+-10% 35VDC TA	28480	0180-0161
A3C18	0180-0228	6	2	CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X901582
A3C19	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C20	0180-0228	6		CAPACITOR-FXD 22UF+-10% 15VDC TA	56289	150D226X901582
A3C21	0180-1714	7	2	CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X900682
A3C22	0180-1714	7		CAPACITOR-FXD 330UF+-10% 6VDC TA	56289	150D337X900682
A3C23-A3C44	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A3C45	0160-0153	4	1	CAPAITOR-FXD 1000PF +-10% 200VDC POLYE	28480	0160-0153
A3C46	0160-2204	0	1	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A3CR1	1901-0040	1	3	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR2	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3CR3	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A3H1	0380-0643	3	2	STANDOFF-HEX .255-IN-LG 6-32THD	00000	ORDER BY DESCRIPTION
A3H2	1251-0218	6	2	LOCK-SUBMIN D CONN	28480	1251-0218
A3H3	2190-0016	3	4	WASHER-LK INTL T 3/8 IN .377-IN-ID	28480	2190-0016
A3H4	2190-0108	4	2	WASHER-LK HLCL NO. 4 .115-IN-ID	28480	2190-0108
A3H5	2360-0113	2	4	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A3H6	2420-0002	6	2	NUT-HEX-DBL-CHAM 6-32-THD .109-IN-THK	28480	2420-0002
A3H7	2950-0001	8	4	NUT-HEX-DBL-CHAM 3/8-32-THD .094-IN-THK	00000	ORDER BY DESCRIPTION
A3J1	1251-3283	1	1	CONNECTOR 24-PIN F MICRORIBBON	28480	1251-3283
A3J2	1251-0064	0	1	CONNECTOR 25-PIN F D SERIES	28480	1251-0064
A3J3	1250-0083	1	4	CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A3J4	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A3J5	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A3J6	1250-0083	1		CONNECTOR-RF BNC FEM SGL-HOLE-FR 50-OHM	28480	1250-0083
A3L1	9100-3139	5	1	COIL 75UH 15% .5DX.875LG-NOM	28480	9100-3139
A3MP1	52101-00302	2	1	DOOR, PC BOARD	28480	52101-00302
A3Q1	1854-0071	7	3	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A3Q2	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A3Q3	1854-0071	7		TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3R1	0683-6815	5	1	RESISTOR 680 5% .25W FC TC=-400/+600	01121	CB6815
A3R2	0683-4715	0	5	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A3R3	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A3R4	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A3R5	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A3R6	0683-2225	8	10	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R7	0683-2725	3	8	RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A3R8	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A3R9	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R10	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A3R11	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R12	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A3R13	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R14	0684-4731	2	3	RESISTOR 47K 10% .25W FC TC=-400/+800	01121	CB4731
A3R15	0684-1811	3	3	RESISTOR 180 10% .25W FC TC=-400/+600	01121	CB1811
A3R16	0684-4731	2		RESISTOR 47K 10% .25W FC TC=-400/+800	01121	CB4731
A3R17	0684-1811	3		RESISTOR 180 10% .25W FC TC=-400/+600	01121	CB1811
A3R18	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A3R19	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R20	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A3R21	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R22	0684-1001	3	10	RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R23	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R24	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R25	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R26	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R27	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R28	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R29	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A3R30	0684-1021	7	3	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A3R31	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A3R32	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R33	0683-1045	3	4	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A3R34	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A3R35	0684-1011	5	2	RESISTOR 100 10% .25W FC TC=-400/+500	01121	CB1011
A3R36	0684-4731	2		RESISTOR 47K 10% .25W FC TC=-400/+800	01121	CB4731
A3R37	0684-1811	3		RESISTOR 180 10% .25W FC TC=-400/+600	01121	CB1811
A3R38	0684-4721	0	4	RESISTOR 4.7K 10% .25W FC TC=-400/+700	01121	CB4721
A3R39	0684-4721	0		RESISTOR 4.7K 10% .25W FC TC=-400/+700	01121	CB4721
A3R40	0684-4721	0		RESISTOR 4.7K 10% .25W FC TC=-400/+700	01121	CB4721
A3R41	0684-4721	0		RESISTOR 4.7K 10% .25W FC TC=-400/+700	01121	CB4721
A3R42	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A3R43	2100-3214	0	1	RESISTOR-TRMR 100K 10% C TOP-ADJ 1-TRN	28480	2100-3214
A3R44	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A3R45	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A3R46	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R47	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R48	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R49	0684-1031	9	1	RESISTOR 10K 10% .25W FC TC=-400/+700	01121	CB1031
A3R50	0684-1001	3		RESISTOR 10 10% .25W FC TC=-400/+500	01121	CB1001
A3R51	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=-400/+700	01121	CB2725
A3R52	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A3R53	0684-1011	5		RESISTOR 100 10% .25W FC TC=400/+500	01121	CB1011
A3R54	0683-2725	8		RESISTOR 2.7K 5% .25W FC TC=400/+700	01121	CB2725
A3R55	0683-2225	3		RESISTOR 2.2K 5% .25W FC TC=400/+700	01121	CB2225
A3S1	3101-2159	3	2	SWITCH-SL 5-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-2159
A3S2	3101-2159	3		SWITCH-SL 5-1A DIP-SLIDE-ASSY .1A 50VDC	28480	3101-2159
A3U1	1820-1112	8	11	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U2	1820-1689	4	4	IC UART TTL QUAD	04713	MC3446P
A3U3	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A3U4	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A3U5	1820-1689	4		IC UART TTL QUAD	04713	MC3446P
A3U6	1820-1199	1	3	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U7	1816-1120	9	1	IC TTL 8 1K ROM 50-NS 0-C	18324	N82S126F PROGRAMMED
A3U8	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U9	1820-1201	6	5	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U10	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U12	1820-0706	4	1	IC COMPTR TTL MAGTD 5-BIT	07263	9324PC
A3U13	1820-1207	2	2	IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A3U14	1820-1216	3	1	IC DCDR TTL LS 3-TO-8-LINE 3-INP	01295	SN74LS138N
A3U15	1820-1203	8	3	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A3U16	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U17	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U18	1820-1144	6	3	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A3U19	1820-1202	7	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS10N
A3U20	1820-1281	2	1	IC DCDR TTL LS 2-TO-4-LINE DUAL 2-INP	01295	SN74LS139N
A3U21	1820-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A3U22	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U23	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U24	1820-1208	3	3	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U25	1820-1196	8	7	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A3U26	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U27	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U28	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A3U29	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U30	1820-1203	8		IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A3U31	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
A3U32	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A3U33	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U34	1820-1244	7	1	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS153N
A3U35	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U36	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A3U37	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A3U38	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A3U39	1820-1300	6	4	IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
A3U40	1820-1300	6		IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
A3U41	1820-1300	6		IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
A3U42	1820-1300	6		IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS195AN
A3U43	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U44	1820-1441	6	10	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U45	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U46	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U47	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U48	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U49	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U50	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U51	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U52	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U53	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U54	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A3U55	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A3U56	1820-1444	9	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
A3U57	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
A3U58	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
A3U59	1820-1438	1	3	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
A3U60	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
A3U61	1820-1438	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
A3U62	1820-1444	9		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
A3U63	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A3U64	1820-1207	2		IC GATE TTL LS NAND 8-INP	01295	SN74LS30N
A3U65	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U66	1820-1307	3	1	IC SCHMITT-TRIG TTL S NAND QUAD 2-INP	01295	SN74S132N
A3U67	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A3U68	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U69	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A3U70	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A3U71	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A3U72	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A3U73	1820-1416	5	1	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
A3U74	1820-1074	1	2	IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A3U75	1820-1074	1		IC DRVR TTL NOR QUAD 2-INP	01295	SN74128N
A3U76	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A3U77	1820-1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U78	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A3U79	1820-1203	8		IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
A3U80	1810-0076	0	2	NETWORK-RES 9-SIP1.8K OHM X 8	28480	1810-0076
A3U81	1810-0076	0		NETWORK-RES 9-SIP1.8K OHM X 8	28480	1810-0076
A3VR1	1902-3149	9	1	DIODE-ZNR 9.09V 5% DO-7 PD=.4W TC=+.057%	28480	1902-3149
A4	01350-66511	7	2	DISPLAY BOARD ASSEMBLY	28480	01350-66511
A4C1	0180-1746	5	2	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A4C2	0160-2055	9	58	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4C11	0121-0046	2	4	CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A4C12	0121-0046	2		CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A4C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C14	0180-0423	3	5	CAPACITOR-FXD 100UF+50-10% 25VDC AL	28480	0180-0423
A4C15	0160-3443	1	19	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C16	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C17	0140-0194	1	2	CAPACITOR-FXD 110PF +-5% 300VDC MICA	72136	DM15F111J0300WV1CR
A4C18	0140-0145	2	2	CAPACITOR-FXD 22PF +-5% 500VDC MICA	72136	DM15C220J0500WV1CR
A4C19	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C20	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C21	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C22	0160-2209	5	2	CAPACITOR-FXD 360PF +-5% 300VDC MICA	28480	0160-2209
A4C23	0140-0220	4	2	CAPACITOR-FXD 200PF +-1% 300VDC MICA	72136	DM15F201F0300WV1CR
A4C24	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C25	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020B2
A4C26	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C27	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C28	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C29	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C30	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C31	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C32	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C33	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C34	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C35	0121-0046	2		CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A4C36	0121-0046	2		CAPACITOR-V TRMR-CER 9-35PF 200V PC-MTG	52763	304322 9/35PF N650
A4C37	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C38	0180-0423	3		CAPACITOR-FXD 100UF+50-10% 25VDC AL	28480	0180-0423
A4C39	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C40	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C41	0140-0194	1		CAPACITOR-FXD 110PF +-5% 300VDC MICA	72136	DM15F111J0300WV1CR
A4C42	0140-0145	2		CAPACITOR-FXD 22PF +-5% 500VDC MICA	72136	DM15C220J0500WV1CR
A4C43	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C44	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C45	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C46	0160-2209	5		CAPACITOR-FXD 360PF +-5% 300VDC MICA	28480	0160-2209
A4C47	0140-0220	4		CAPACITOR-FXD 200PF +-1% 300VDC MICA	72136	DM15F201F0300WV1CR
A4C48	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C49	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C50	0180-0423	3		CAPACITOR-FXD 100UF+50-10% 25VDC AL	28480	0180-0423
A4C51	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C52	0180-0423	3		CAPACITOR-FXD 100UF+50-10% 25VDC AL	28480	0180-0423
A4C53	0160-0938	3	1	CAPACITOR-FXD 1000PF +-5% 100VDC MICA	28480	0160-0938
A4C54	0140-0197	4	4	CAPACITOR-FXD 180PF +-5% 300VDC MICA	72136	DM15F181J0300WV1CR
A4C55	0140-0197	4		CAPACITOR-FXD 180PF +-5% 300VDC MICA	72136	DM15F181J0300WV1CR
A4C56	0140-0197	4		CAPACITOR-FXD 180PF +-5% 300VDC MICA	72136	DM15F181J0300WV1CR
A4C57	0140-0197	4		CAPACITOR-FXD 180PF +-5% 300VDC MICA	72136	DM15F181J0300WV1CR
A4C58	0180-0424	4	1	CAPACITOR-FXD 470UF+100-10% 25VDC AL	28480	0180-0424
A4C59	0180-2500	1	1	CAPACITOR-FXD 1500UF+50-10% 16VDC AL	37942	TT152U016G1C3P
A4C60						
A4C90	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C91	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C92	0140-0202	2	4	CAPACITOR-FXD 15PF +-5% 500VDC MICA	72136	DM15C150J0500WV1CR
A4C93	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C94	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C95	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C96	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C97	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A4C98	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C99	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C100	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C101	0140-0202	2		CAPACITOR-FXD 15PF +-5% 500VDC MICA	72136	DM15C150J0500WV1CR
A4C102	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C103	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C104	0160-2150	5	2	CAPACITOR-FXD 33PF +-5% 300VDC MICA	28480	0160-2150
A4C105	0160-2150	5		CAPACITOR-FXD 33PF +-5% 300VDC MICA	28480	0160-2150
A4C106	0140-0192	9	1	CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A4C107	0160-3070	0	1	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-3070
A4C108	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A4C109	0140-0199	6	2	CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A4C110	0180-0423	3		CAPACITOR-FXD 100UF+50-10% 25VDC AL	28480	0180-0423
A4C111	0140-0199	6		CAPACITOR-FXD 240PF +-5% 300VDC MICA	72136	DM15F241J0300WV1CR
A4C112	0140-0202	2		CAPACITOR-FXD 15PF +-5% 500VDC MICA	72136	DM15C150J0500WV1CR
A4C113	0140-0202	2		CAPACITOR-FXD 15PF +-5% 500VDC MICA	72136	DM15C150J0500WV1CR

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4CR1	1901-0179	7	20	DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR2	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR3	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR4	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR5	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR6	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR7	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR8	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR9	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR10	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR11	1901-0047	8	2	DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A4CR12	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR13	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR14	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR15	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR16	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR17	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR18	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR19	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR20	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR21	1901-0179	7		DIODE-SWITCHING 15V 50MA 750PS DO-7	28480	1901-0179
A4CR22	1901-0047	8		DIODE-SWITCHING 20V 75MA 10NS	28480	1901-0047
A4CR23	1901-0040	1	5	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR24	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR25	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR26	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4CR27	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A4E1	0360-1653	5	6	CONNECTOR-SGL CONT PIN .045-IN-BSC-8Z SQ	28480	0360-1653
A4E2	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-8Z SQ	28480	0360-1653
A4E3	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-8Z SQ	28480	0360-1653
A4E4	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-8Z SQ	28480	0360-1653
A4E5	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-8Z SQ	28480	0360-1653
A4E6	0360-1653	5		CONNECTOR-SGL CONT PIN .045-IN-BSC-8Z SQ	28480	0360-1653
A4J3	1251-4335	6	4	CONNECTOR 8-PIN M POST TYPE	28480	1251-4335
A4J4	1251-4335	6		CONNECTOR 8-PIN M POST TYPE	28480	1251-4335
A4J5	1251-3192	1	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-3192
A4L1	9100-3139	5	3	COIL 75UH 15% .5DX.875LG-NOM	28480	9100-3139
A4L2	9100-3139	5		COIL 75UH 15% .5DX.875LG-NOM	28480	9100-3139
A4L3	9100-3139	5		COIL 75UH 15% .5DX.875LG-NOM	28480	9100-3139
A4L4	9170-0029	3	2	CORE-SHIELDING BEAD	28480	9170-0029
A4L5	9170-0029	3		CORE-SHIELDING BEAD	28480	9170-0029
A4MP1	1205-0213	4	2	HEAT SINK SEL TO-5/TO-39-CS	28480	1205-0213
A4Q1-A4Q40	1853-0036	2	40	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
A4R1	0699-0001	2	4	RESISTOR 2.7 10% .5W CC TC=0+412	01121	EB27Q1
A4R2	0757-0284	7	2	RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R3	2100-3212	8	2	RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	28480	2100-3212
A4R4	0757-0408	7	2	RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-T0-243R-F
A4R5	0698-6612	1	10	RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R6	0757-0401	0	39	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R7	0698-6996	4	22	RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R8	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R9	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R10	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R11	0698-6989	5	16	RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R12	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R13	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R14	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R15	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R16	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R17	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R18	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R19	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R20	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R21	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R22	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R23	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R24	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R25	2100-0568	1	10	RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R26	0698-0083	8	10	RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R27	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R28	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R29	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R30	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R31	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R32	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R33	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R34	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R35	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R36	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R37	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R38	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R39	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R40	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R41	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R42	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R43	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R44	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R45	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R46	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R47	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R48	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R49	0757-0421	4	2	RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A4R50	0757-0435	0	2	RESISTOR 3.92K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3921-F
A4R51	0757-0280	3	4	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R52	0757-0429	2	4	RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A4R53	0757-0274	5	2	RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A4R54	0757-0416	7	6	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R55	0757-0178	8	2	RESISTOR 100 1% .25W F TC=0+-100	24546	C5-1/4-T0-101-F
A4R56	0698-3440	7	2	RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A4R57	0757-0460	1	2	RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A4R58	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R59	0757-0445	2	2	RESISTOR 13K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1302-F
A4R60	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R61	0757-0413	4	2	RESISTOR 392 1% .125W F TC=0+-100	24546	C4-1/8-T0-392R-F
A4R62	0698-5418	3	2	RESISTOR 50 .1% .125W F TC=0+-50	28480	0698-5418
A4R63	0699-0001	2		RESISTOR 2.7 10% .5W CC TC=0+412	01121	EB2701
A4R64	0757-0284	7		RESISTOR 150 1% .125W F TC=0+-100	24546	C4-1/8-T0-151-F
A4R65	2100-3212	8		RESISTOR-TRMR 200 10% C TOP-ADJ 1-TRN	28480	2100-3212
A4R66	0757-0408	7		RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-T0-243R-F
A4R67	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R68	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R69	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R70	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R71	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R72	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R73	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R74	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R75	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R76	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R77	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R78	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R79	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R80	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R81	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R82	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R83	0698-6612	1		RESISTOR 2K .1% .125W F TC=0+-50	28480	0698-6612
A4R84	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R85	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R86	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R87	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R88	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R89	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R90	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R91	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R92	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R93	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R94	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R95	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R96	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R97	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R98	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R99	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R100	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989
A4R101	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R102	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R103	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R104	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R105	0698-6989	5		RESISTOR 400 .1% .125W F TC=0+-50	28480	0698-6989

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4R106	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R107	2100-0568	1		RESISTOR-TRMR 100 10% C TOP-ADJ 1-TRN	28480	2100-0568
A4R108	0698-0083	8		RESISTOR 1.96K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1961-F
A4R109	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R110	0698-6996	4		RESISTOR 200 .1% .125W F TC=0+-50	28480	0698-6996
A4R111	0757-0421	4		RESISTOR 825 1% .125W F TC=0+-100	24546	C4-1/8-T0-825R-F
A4R112	0757-0435	0		RESISTOR 3.92K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3921-F
A4R113	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R114	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A4R115	0757-0274	5		RESISTOR 1.21K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1213-F
A4R116	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R117	0757-0178	8		RESISTOR 100 1% .25W F TC=0+-100	24546	C5-1/4-T0-101-F
A4R118	0698-3440	7		RESISTOR 196 1% .125W F TC=0+-100	24546	C4-1/8-T0-196R-F
A4R119	0757-0460	1		RESISTOR 61.9K 1% .125W F TC=0+-100	24546	C4-1/8-T0-6192-F
A4R120	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R121	0757-0445	2		RESISTOR 13K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1302-F
A4R122	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A4R123	0757-0413	4		RESISTOR 392 1% .125W F TC=0+-100	24546	C4-1/8-T0-392R-F
A4R124	0698-5418	3		RESISTOR 50 .1% .125W F TC=0+-50	28480	0698-5418
A4R125	0699-0001	2		RESISTOR 2.7 10% .5W CC TC=0+412	01121	EB27G1
A4R126	0699-0001	2		RESISTOR 2.7 10% .5W CC TC=0+412	01121	EB27G1
A4R127	0757-0389	3	2	RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-33R2-F
A4R128	0698-3432	7	2	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
A4R129	0757-0389	3		RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-33R2-F
A4R130	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
A4R131	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R132	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R133	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R134	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R135	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R136	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R137	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R138	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R139	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R140	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R141	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R142	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R143	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R144	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R145	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R146	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R147	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R148	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R149	0686-3915	6	1	RESISTOR 390 5% .5W CC TC=0+529	01121	EB3915
A4R150	0757-0442	9	11	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R151	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R152	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A4R153	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A4R154	0757-0429	2		RESISTOR 1.82K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1821-F
A4R155	0757-0346	2	1	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
A4R156	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R157	0757-0453	2	1	RESISTOR 30.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3012-F
A4R158	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R159	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R160	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R161	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R162	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R163	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R164	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R165	0757-0401	0		RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A4R166	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R167	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
A4R168	0698-0084	9	2	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A4R169	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
A4R170	0698-3132	4	1	RESISTOR 261 1% .125W F TC=0+-100	24546	C4-1/8-T0-2610-F
A4R171	0811-1666	7	1	RESISTOR 1 5% 2W PW TC=0+-800	75042	BWH2-1R0-J
A4TP1- A4TP10	0360-0535	0	10	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A4U1- A4U16	1818-0156	3	16	IC NMOS 4K RAM DYN 470-NS 3-S	28480	1818-0156
A4U17	1820-1470	1	3	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A4U18	1820-1447	2	3	IC TTL LS 16-BIT RAM 45-NS 3-S	01295	SN74LS670N
A4U19	1820-1453	0	3	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN748163N
A4U20	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A4U21	1820-1447	2		IC TTL LS 16-BIT RAM 45-NS 3-S	01295	SN74LS670N
A4U22	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN748163N
A4U23	1820-1470	1		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS157N
A4U24	1820-1447	2		IC TTL LS 16-BIT RAM 45-NS 3-S	01295	SN74LS670N

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4U25	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN748163N
A4U26	1820-1810	3	1	IC DRVR TTL CLOCK DRVR	04713	MC3460P
A4U27	1820-1196	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A4U28	1820-0706	4	1	IC COMPTR TTL MAGTD 5-BIT	07263	9324PC
A4U29	1820-1641	8	2	IC DRVR TTL LS BUS DRVR HEX 1-INP	01295	SN74LS365AN
A4U30	1820-1641	8		IC DRVR TTL LS BUS DRVR HEX 1-INP	01295	SN74LS365AN
A4U31	1820-1280	1	6	IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U32	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U33	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U34	1820-1411	0	7	IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U35	1820-1211	8	5	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U36	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U37	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U38	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U39	1820-1444	9	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS298N
A4U40	1820-1210	7	2	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A4U41	1820-1210	7		IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A4U42	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74802N
A4U43	1820-1275	4	2	IC GATE TTL S NOR DUAL 5-INP	01295	SN748260N
A4U44	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U45	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U46	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U47	1820-0683	6	3	IC INV TTL S HEX 1-INP	01295	SN74804N
A4U48	1820-1411	0		IC LCH TTL LS D-TYPE 4-BIT	01295	SN74LS75N
A4U49	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U50	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U51	1820-1280	1		IC ARITH-LGC-UN TTL LS 4-BIT	01295	SN74LS181N
A4U52	1820-1943	3	6	IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN748169J
A4U53	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN748169J
A4U54	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN748169J
A4U55	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN748169J
A4U56	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN748169J
A4U57	1820-1943	3		IC CNTR TTL S BIN UP/DOWN SYNCHRO 4-BIT	01295	SN748169J
A4U58	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U59	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U60	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
A4U61	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN748260N
A4U62	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74804N
A4U63	1820-1032	1	5	IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U64	1820-1905	7	1	IC GATE TTL LS NOR DUAL 5-INP	07263	74LS260PC
A4U65	1820-1032	1		IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U66	1820-1032	1		IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U67	1820-1032	1		IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U68	1820-1032	1		IC SHF-RGTR TTL R-S PRL-IN PRL-OUT 8-BIT	01295	SN74198N
A4U69	1820-0744	0	6	IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U70	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U71	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U72	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U73	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U74	1820-0744	0		IC CNTR TTL BIN SYNCHRO POS-EDGE-TRIG	01295	SN7497N
A4U75	1820-1441	6	1	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
A4U76	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A4U77	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74802N
A4U78	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74800N
A4U79	1820-0693	8	4	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74874N
A4U80	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74800N
A4U81	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74874N
A4U82	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74874N
A4U83	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74804N
A4U84	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74811N
A4U85	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74874N
A4U86	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74832N
A4U87	1820-0704	2	1	IC MV TTL MONOSTBL RETRIG	01295	SN74122N
A4U88	1820-1199	1	1	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
A4U89	1826-0357	3	2	IC OP AMP WB TO-99	27014	LF357H
A4U90	1826-0167	3	2	IC OP AMP PRGMBL TO-99	21921	CA3094AT
A4U91	1826-0357	3		IC OP AMP WB TO-99	27014	LF357H
A4U92	1826-0167	3		IC OP AMP PRGMBL TO-99	21921	CA3094AT
A4VR1	1902-0041	4	4	DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=-.009%	28480	1902-0041
A4VR2	1902-0041	4		DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=-.009%	28480	1902-0041
A4VR3	1902-0025	4	2	DIODE-ZNR 10V 5% DO-7 PD=.4W TC=+.06%	28480	1902-0025
A4VR4	1902-0041	4		DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=-.009%	28480	1902-0041
A4VR5	1902-0041	4		DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=-.009%	28480	1902-0041
A4VR6	1902-0025	4		DIODE-ZNR 10V 5% DO-7 PD=.4W TC=+.06%	28480	1902-0025

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A4Y1	0410-0424	3	1	CRYSTAL-QUARTZ 24.61000 MHZ	28480	0410-0424
A5	01350-66515	1	1	POWER SUPPLY BOARD ASSEMBLY	28480	01350-66515
A5C1	0160-3452	2	9	CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C2	0160-3452	2		CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C3	0160-3452	2		CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C4	0160-3452	2		CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C5	0160-3452	2		CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C6	0160-3452	2		CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C7	0180-2395	2	6	CAPACITOR-FXD 3000UF+75-10% 40VDC AL	28480	0180-2395
A5C8	0180-2395	2		CAPACITOR-FXD 3000UF+75-10% 40VDC AL	28480	0180-2395
A5C9	0180-2395	2		CAPACITOR-FXD 3000UF+75-10% 40VDC AL	28480	0180-2395
A5C10	0180-2395	2		CAPACITOR-FXD 3000UF+75-10% 40VDC AL	28480	0180-2395
A5C11	0180-2395	2		CAPACITOR-FXD 3000UF+75-10% 40VDC AL	28480	0180-2395
A5C12	0180-2395	2		CAPACITOR-FXD 3000UF+75-10% 40VDC AL	28480	0180-2395
A5C13	0160-3443	1	3	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C14	0160-0939	4	1	CAPACITOR-FXD 430PF +-5% 300VDC MICA	28480	0160-0939
A5C15	0160-0160	3	1	CAPACITOR-FXD 8200PF +-10% 200VDC POLYE	28480	0160-0160
A5C16	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C17	0160-3452	2		CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C18	0180-2750	3	1	CAPACITOR-FXD 3300UF+100-10% 6.3VDC AL	56289	672D338M6R3JE2C
A5C19	0160-3452	2		CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C20	0160-3452	2		CAPACITOR-FXD .02UF +-20% 100VDC CER	28480	0160-3452
A5C21	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A5C22	0160-3508	9	4	CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C23	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C24	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C25	0160-3508	9		CAPACITOR-FXD 1UF +80-20% 50VDC CER	28480	0160-3508
A5C26	0160-3451	1	1	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-3451
A5CR1	1906-0006	9	4	DIODE-FW BRDG 400V 1A	28480	1906-0006
A5CR2	1906-0006	9		DIODE-FW BRDG 400V 1A	28480	1906-0006
A5CR3	1906-0006	9		DIODE-FW BRDG 400V 1A	28480	1906-0006
A5CR4	1906-0006	9		DIODE-FW BRDG 400V 1A	28480	1906-0006
A5CR5	1901-0513	3	1	DIODE-DUAL 100V	28480	1901-0513
A5CR6	1901-0708	8	1	DIODE-PWR RECT 1N5828 40V 15A DO-4	28480	1901-0708
A5CR7	1901-0028	5	2	DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A5CR8	1901-0028	5		DIODE-PWR RECT 400V 750MA DO-29	28480	1901-0028
A5F1	2110-0056	3	1	FUSE 6A 250V FAST-BLO 1.25X.25 UL IEC	75915	312006
A5H1	2190-0034	5	1	WASHER-LK HLCL NO. 10 .194-IN-ID	28480	2190-0034
A5H2	2740-0002	4	1	NUT-HEX-DBL-CHAM 10-32-THD .125-IN-THK	00000	ORDER BY DESCRIPTION
A5J1	1251-3475	3	1	CONNECTOR 10-PIN M POST TYPE	28480	1251-3475
A5J2	1251-3976	9	2	CONNECTOR 6-PIN M POST TYPE	28480	1251-3976
A5J3	1251-3976	9		CONNECTOR 6-PIN M POST TYPE	28480	1251-3976
A5J4	1251-3195	4	1	CONNECTOR 4-PIN M POST TYPE	28480	1251-3195
A5J5	1251-3192	1	1	CONNECTOR 3-PIN M POST TYPE	28480	1251-3192
A5J6	1251-3276	2	1	CONNECTOR 6-PIN M POST TYPE	28480	1251-3276
A5L1	9140-0242	9	1	COIL 100UH 10% .937DX1.625LG-NOM	28480	9140-0242
A5MP1	1205-0213	4	2	HEAT SINK SGL TO-5/TO-39-CS	28480	1205-0213
A5MP2	1205-0226	9	1	HEAT SINK SGL TO-5/TO-39-CS	28480	1205-0226
A5MP3	1205-0310	2	1	HEAT SINK SGL TO-3-CS	28480	1205-0310
A5MP4	1400-0265	0	3	CABLE TIE 1.75-DIA .19-WD NYL	28480	1400-0265
A5MP5	2110-0269	0	2	FUSEHOLDER-CLIP TYPE,25D-FUSE	28480	2110-0269
A5MP6	0362-0174	7	1	TERMINAL-SLDR LUG LK-MTG FOR-#6-8CR	86928	A373-152-1
A5Q1	1884-0256	3	2	THYRISTOR-TRIAC TO-5	28480	1884-0256
A5Q2	1854-0071	7	1	TRANSISTOR NPN SI PD=300MW FT=200MHZ	28480	1854-0071
A5Q3	1853-0084	0	1	TRANSISTOR PNP 2N4918 SI PD=30W FT=3MHZ	04713	2N4918
A5Q4	1854-0472	2	1	TRANSISTOR NPN SI DARL PD=500MW	04713	MPS-A14
A5Q5	1884-0082	3	1	THYRISTOR-SCR 2N4441 VRRM=50	04713	2N4441
A5Q6	1884-0256	3		THYRISTOR-TRIAC TO-5	28480	1884-0256
A5R1	0683-1045	3	4	RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R2	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R3	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R4	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
A5R5	0687-1821	1	1	RESISTOR 1.8K 10% .5W CC TC=0+647	01121	EB1821
A5R6	0683-1015	7	5	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A5R7	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A5R8	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A5R9	0757-0446	3	1	RESISTOR 15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1502-F
A5R10	0683-1025	9	3	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025

See introduction to this section for ordering information
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Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A5R11	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A5R12	0811-1200	5	3	RESISTOR .1 10% 2W PW TC=0+-800	75042	BWH2-2-1/10-K
A5R13	0684-3941	4	1	RESISTOR 390K 10% .25W FC TC=-800/+900	01121	CB3941
A5R14	0757-0317	7	1	RESISTOR 1.33K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1331-F
A5R15	2100-0554	5	1	RESISTOR-TRMR 500 10% C TOP-ADJ 1-TRN	28480	2100-0554
A5R16	0757-0435	0	1	RESISTOR 3.92K 1% .125W F TC=0+-100	24546	C4-1/8-T0-3921-F
A5R17	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A5R18	0683-2205	9	2	RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
A5R19	0757-1090	5	1	RESISTOR 261 1% .5W F TC=0+-100	28480	0757-1090
A5R20	0683-2205	9		RESISTOR 22 5% .25W FC TC=-400/+500	01121	CB2205
A5R21	0683-1205	7	1	RESISTOR 12 5% .25W FC TC=-400/+500	01121	CB1205
A5R22	0683-0275	9	1	RESISTOR 2.7 5% .25W FC TC=-400/+500	01121	CB27G5
A5R23	0811-1200	5		RESISTOR .1 10% 2W PW TC=0+-800	75042	BWH2-2-1/10-K
A5R24	0811-1200	5		RESISTOR .1 10% 2W PW TC=0+-800	75042	BWH2-2-1/10-K
A5R25	0683-2225	3	1	RESISTOR 2.2K 5% .25W FC TC=-400/+700	01121	CB2225
A5R26	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A5R27	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A5R28	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
A5R29	0811-1668	9	2	RESISTOR 1.5 5% 2W PW TC=0+-400	75042	BWH2-1R5-J
A5R30	0811-1668	9		RESISTOR 1.5 5% 2W PW TC=0+-400	75042	BWH2-1R5-J
A5TP1	0360-0535	0	9	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
A5U1	1820-0196	6	1	IC 723 V RGLTR TO-100	04713	MC1723CG
A5VR1	1902-0041	4	2	DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=-.009%	28480	1902-0041
A5VR2	1902-3193	3	1	DIODE-ZNR 13.3V 5% DO-7 PD=.4W TC=+.059%	28480	1902-3193
A5VR3	1902-0041	4		DIODE-ZNR 5.11V 5% DO-7 PD=.4W TC=-.009%	28480	1902-0041
A6	01350-66512	8	1	CHARACTER BOARD ASSEMBLY	28480	01350-66512
A6C1	0180-0106	9	2	CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A6C2	0160-2055	9	17	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C3	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C4	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C5	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C6	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C7	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C8	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C9	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C10	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C11	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C12	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C13	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C14	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C15	0180-0106	9		CAPACITOR-FXD 60UF+-20% 6VDC TA	56289	150D606X0006B2
A6C16	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C17	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C18	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6C19	0160-2204	0	2	CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A6C20	0160-2204	0		CAPACITOR-FXD 100PF +-5% 300VDC MICA	28480	0160-2204
A6C21	0140-0202	2	1	CAPACITOR-FXD 15PF +-5% 500VDC MICA	72136	DM15C150J0500WV1CR
A6C22	0140-0198	5	2	CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A6C23	0160-2202	8	1	CAPACITOR-FXD 75PF +-5% 300VDC MICA	28480	0160-2202
A6C24	0140-0198	5		CAPACITOR-FXD 200PF +-5% 300VDC MICA	72136	DM15F201J0300WV1CR
A6C25	0160-2055	9		CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A6P1	1251-5012	8	4	CONNECTOR 8-PIN F POST TYPE	28480	1251-5012
A6P2	1251-5012	8		CONNECTOR 8-PIN F POST TYPE	28480	1251-5012
A6R1	0757-0416	7	1	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
A6R2	0683-1015	7	1	RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
A6R3	0683-1035	1	10	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R4	0757-0281	4	1	RESISTOR 2.74K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2741-F
A6R5	0757-0200	7	1	RESISTOR 5.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5621-F
A6R6	0757-0438	3	2	RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R7	0757-0438	3		RESISTOR 5.11K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5111-F
A6R8	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R9	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R10	0683-4715	0	8	RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-2. Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
A6R11	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A6R12	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A6R13	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A6R14	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A6R15	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A6R16	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A6R17	0683-4715	0		RESISTOR 470 5% .25W FC TC=-400/+600	01121	CB4715
A6R18	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R19	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R20	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R21	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R22	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R23	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6R24	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
A6U1	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U2	1820-1423	4	2	IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A6U3	1820-1197	9	4	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U4	1820-1423	4		IC MV TTL LS MONOSTBL RETRIG DUAL	01295	SN74LS123N
A6U5	1820-1905	7	1	IC GATE TTL LS NOR DUAL 5-INP	07263	74LS260PC
A6U6	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U7	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U8	1820-1077	4	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
A6U9	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74N
A6U10	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U11	1816-1104	9	1	IC TTL S 1K ROM 50-NS 0-C	28480	1816-1104
A6U12	1820-1238	9	4	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A6U13	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A6U14	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A6U15	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
A6U16	1820-1196	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
A6U17	1816-1118	5	1	IC TTL S 256K ROM 50-NS 0-C	28480	1816-1118
A6U18	1816-1119	6	1	IC TTL S 256K ROM 50-NS 0-C	28480	1816-1119
A6U19	1820-1193	5	3	IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS197N
A6U20	1820-1193	5		IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS197N
A6U21	1820-1193	5		IC CNTR TTL LS BIN ASYNCHRO	01295	SN74LS197N
A6U22	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
A6U23	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A6U24	1816-1105	0	1	IC TTL S 1K ROM 50-NS 0-C	28480	1816-1105
A6U26	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
A6XU11	1200-0622	9	3	SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0622
A6XU17	1200-0473	8		SOCKET-IC 16-CONT DIP-SLDR	28480	1200-0473
A6XU18	1200-0473	8	2	SOCKET-IC 16-CONT DIP—SLDR	28480	1200-0473
A6XU24	1200-0622	9		SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0622
A6XU25	1200-0622	9		SOCKET-IC 24-CONT DIP-SLDR	28480	1200-0622
A7	01350-66506	0	1	LED BOARD ASSEMBLY	28480	01350-66506
A7DS1	1990-0521	0	1	LED-VISIBLE LUM-INT=2.2MCD IF=50MA-MAX (GRN)	28480	5082-4955
A7DS2	1990-0524	3	3	LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX (YEL)	28480	5082-4550
A7DS3	1990-0524	3		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4550
A7DS4	1990-0524	3		LED-VISIBLE LUM-INT=1MCD IF=20MA-MAX	28480	5082-4550
A7DS5	1990-0586	7	1	LED-VISIBLE LUM-INT=800UCD IF=50MA-MAX (RED)	28480	5082-4855
A7P1	1251-3275	1	1	CONNECTOR 6-PIN F POST TYPE	28480	1251-3275
A7P1E1	1251-3073	7	6	CONTACT-CONN U/W-POST-TYPE FEM CRP	28480	1251-3073
A8	01350-66507	1	1	LINE SWITCH ASSEMBLY	28480	01350-66507
A8H1	0520-0128	7	1	SCREW-MACH 2-56 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A8H2	0610-0001	6	1	NUT-HEX-DBL-CHAM 2-56-THD .062-IN-THK	00000	ORDER BY DESCRIPTION
A8H3	2190-0045	8	1	WASHER-LK HLCL NO. 2 .088-IN-ID	28480	2190-0045
A8J1	1251-0513	4	1	CONNECTOR 5-PIN M POST TYPE	28480	1251-0513
A8J2	1251-3475	3	2	CONNECTOR 10-PIN M POST TYPE	28480	1251-3475
A8J3	1251-3475	3		CONNECTOR 10-PIN M POST TYPE	28480	1251-3475
A8S1	3101-0555	9	1	SWITCH-PB DPDT ALTNG 4A 250VAC	28480	3101-0555

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
00000	ANY SATISFACTORY SUPPLIER	MILWAUKEE	WI	53204
01121	ALLEN-BRADLEY CO	DALLAS	TX	75222
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	WHIPPANY	NJ	07981
03888	KDI PYROFILM CORP	PHOENIX	AZ	85062
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	WAKEFIELD	MA	01880
05820	WAKEFIELD ENGINEERING INC	MOUNTAIN VIEW	CA	94042
07263	FAIRCHILD SEMICONDUCTOR DIV	SUNNYVALE	CA	94086
18324	SIGNETICS CORP	SOMERVILLE	NJ	08876
21921	RCA CORP SOLID STATE DIV	BRADFORD	PA	16701
24546	CORNING GLASS WORKS (BRADFORD)	SANTA CLARA	CA	95051
27014	NATIONAL SEMICONDUCTOR CORP	PALO ALTO	CA	94304
28480	HEWLETT-PACKARD CO CORPORATE HQ	INDIANAPOLIS	IN	46206
37942	MALLORY P R AND CO INC	CAZENOVIA	NY	13035
52763	STETTNER-TRUSH INC	NORTH ADAMS	MA	01247
56289	SPRAGUE ELECTRIC CO	ELIZABETH	NJ	07207
59730	THOMAS & BETTS CO THE	ST LOUIS	MO	63107
71400	BUSSMAN MFG DIV OF MCGRAW-EDISON CO	WILLIMANTIC	CT	06226
72136	ELECTRO MOTIVE CORP SUB IEC	PHILADELPHIA	PA	19108
75042	TRW INC PHILADELPHIA DIV	DES PLAINES	IL	60016
75915	LITTELFUSE INC	GLENDALE	CA	91201
86928	SEASTROM MFG CO			

See introduction to this section for ordering information

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section contains information for adapting this manual to instruments for which the content does not apply directly.

7-3. MANUAL CHANGES.

7-4. To adapt this manual to your instrument, refer to table 7-1 and make all of the manual changes listed opposite your instrument serial number. Perform these changes in the sequence listed.

7-5. If your instrument serial number is not listed on the title page of this manual or in table 7-1 below, it may be documented in a yellow MANUAL CHANGES supplement. For additional information about serial number coverage refer to INSTRUMENTS COVERED BY MANUAL in Section I.

Table 7-1. Manual Changes

Serial Prefix Number	Make Manual Changes
1906A	1
1750A	1,2

7-6. MANUAL CHANGE INSTRUCTIONS.

CHANGE 1 (S/P 1906A)

Paragraph 5-8. Z-AXIS OUTPUT ADJUSTMENT,
Replace paragraph 5-8 with the following procedure:

5-8. Z-AXIS OUTPUT ADJUSTMENT.

REFERENCE:
Service Sheet 3E.

DESCRIPTION:
The 1350A rear-panel Z-AXIS control is adjusted for compatibility with the X-Y display being used.

EQUIPMENT:
X-Y Display ..... HP 1311A

PROCEDURE:

a. Connect 1350A X, Y, and Z outputs to display X, Y and Z inputs.

b. Make sure that display is in 50-ohm input configuration. Also, make sure that display TTL blanking input has shorting cap installed.

c. Cycle the LINE power switches on the 1350A and the X-Y display. The CRT should display random vectors.

d. Set X-Y display control to minimum intensity (full CCW).

e. Adjust 1350A rear-panel Z-AXIS control until random vectors are just extinguished. Set X-Y display intensity to normal viewing level.

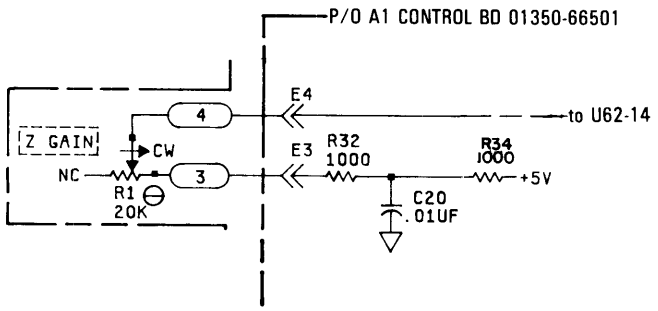
Table 6-2. Replaceable Parts,
Change: Al HP and Mfr Part Nos. to 01350-66501 (2 places).
Add: A1R34, HP Part No. 0757-0278, CD 9, RESISTOR 1.78K 1% .125W F TC=+-100, Mfr Code 24546, Mfr Part No. C4-1/8-T0-1781F.
Delete: A1R55, A1R56, A1R57.
Change: A3 HP and Mfr Part Nos to 52101-66503, and CD to 3 (2 places).
Delete: A3C45, A3C46, A3R54, A3R55.

Figure 8-11. Input/Output Board A3 Componet Locator,
Replace figure 8-11 with figure 7-1.

Figures 8-12, 8-15, 8-16, 8-17. Schematics 2A through 2D,
Replace schematics 2A through 2D with figures 7-2 through 7-5 respectively.

Figure 8-21. Control Board A1 Component Locator,
Add: R34 adjacent to C20 at loction J2.
Delete: R55, R56, R57.

Figure 8-28. Schematic 3E,
Delete: A1R55, A1R56, A1R57.
Add: A1R34 as shown below:

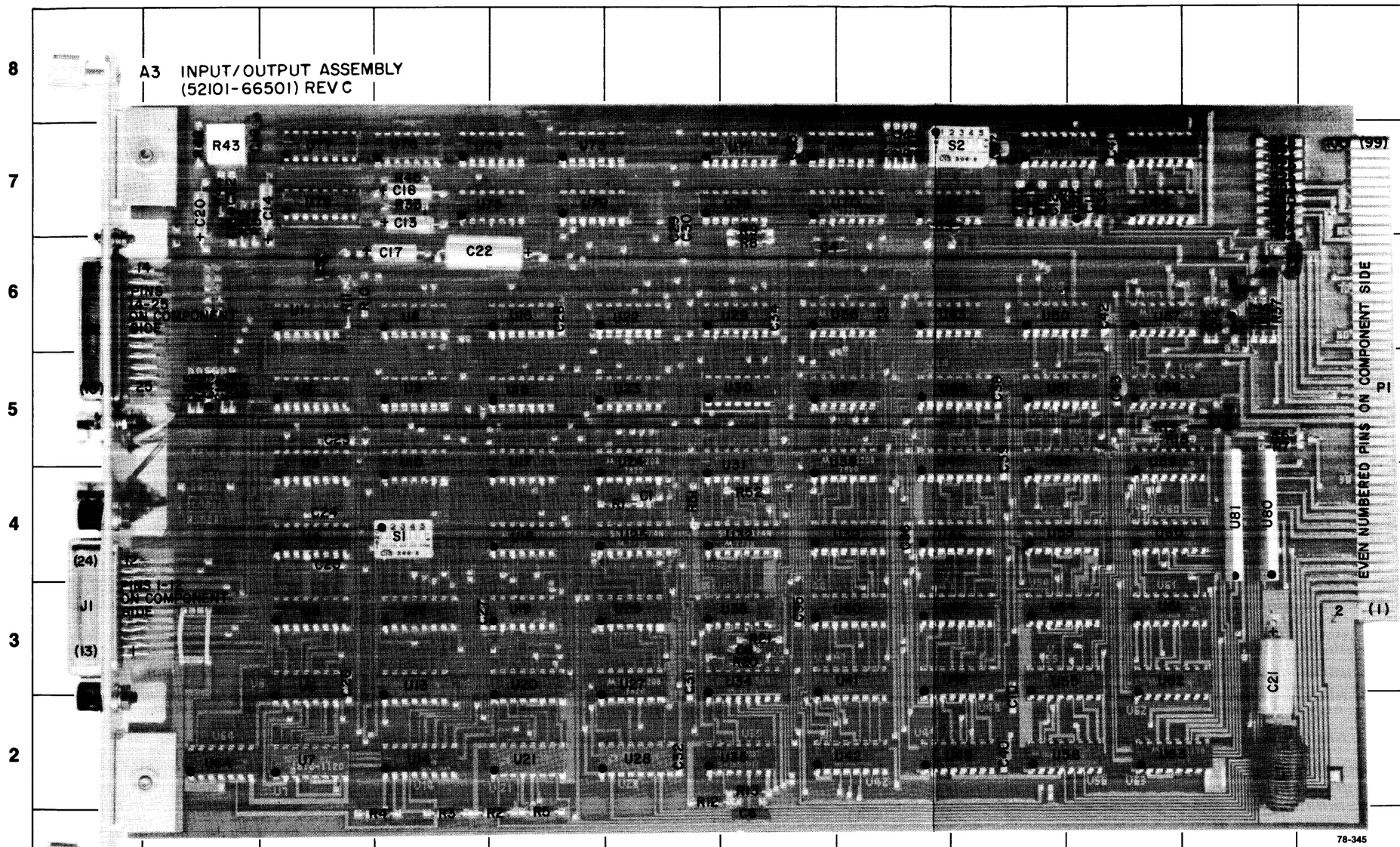


CHANGE 2 (S/P 1750A)

Table 6-2. Replaceable Parts,
- Change: A5 HP and Mfr Part Nos. to 01350-66503, and CD to 7 (2 places).
- Change: MP26 HP and Mfr Part Nos. to 01350-00104, and CD to 6.
- Delete: A5C19 through A5C25.
- Delete: A5CR7, A5CR8.
- Delete: A5J4.
- Add: A5J7, HP Part No. 1251-0513, CD 4, Qty 1, CONNECTOR 5-PIN M POST TYPE, Mfr Code 28480, Mfr Part No. 1251-0513.
- Add: A5J8 and A5J9, HP Part No. 1251-3475, CD 3, Qty 2, CONNECTOR 10-PIN M POST TYPE, Mfr Code 28480, Mfr Part No. 1251-3475.
- Delete: MP1.
- Change: Q1 HP Part No. 1884-0074, CD 3, Qty 1, THYRISTOR - SCR 2N5060 T0=92 VRRM=30, Mfr Code 04713, Mfr Part No. 2N5060.
- Delete: A5Q6.
- Change: A5R12, HP Part No. 0811-1666, CD 7, RESISTOR-1 5% 2W PW TC=0+800, Mfr Code 75042, Mfr Part No. BWH2-1R2-J.
- Delete: A5R28, A5R29, A5R30.
- Add: A5S1, HP Part No. 3101-0555, CD 9, Qty 1, SWITCH-PB DPDT ALTNG 4A 250VAC, Mfr Code 28480, Mfr Part No. 3101-0555.
- Delete: A5VR3.
- Delete: A8 (2 places) and all A8 entries.

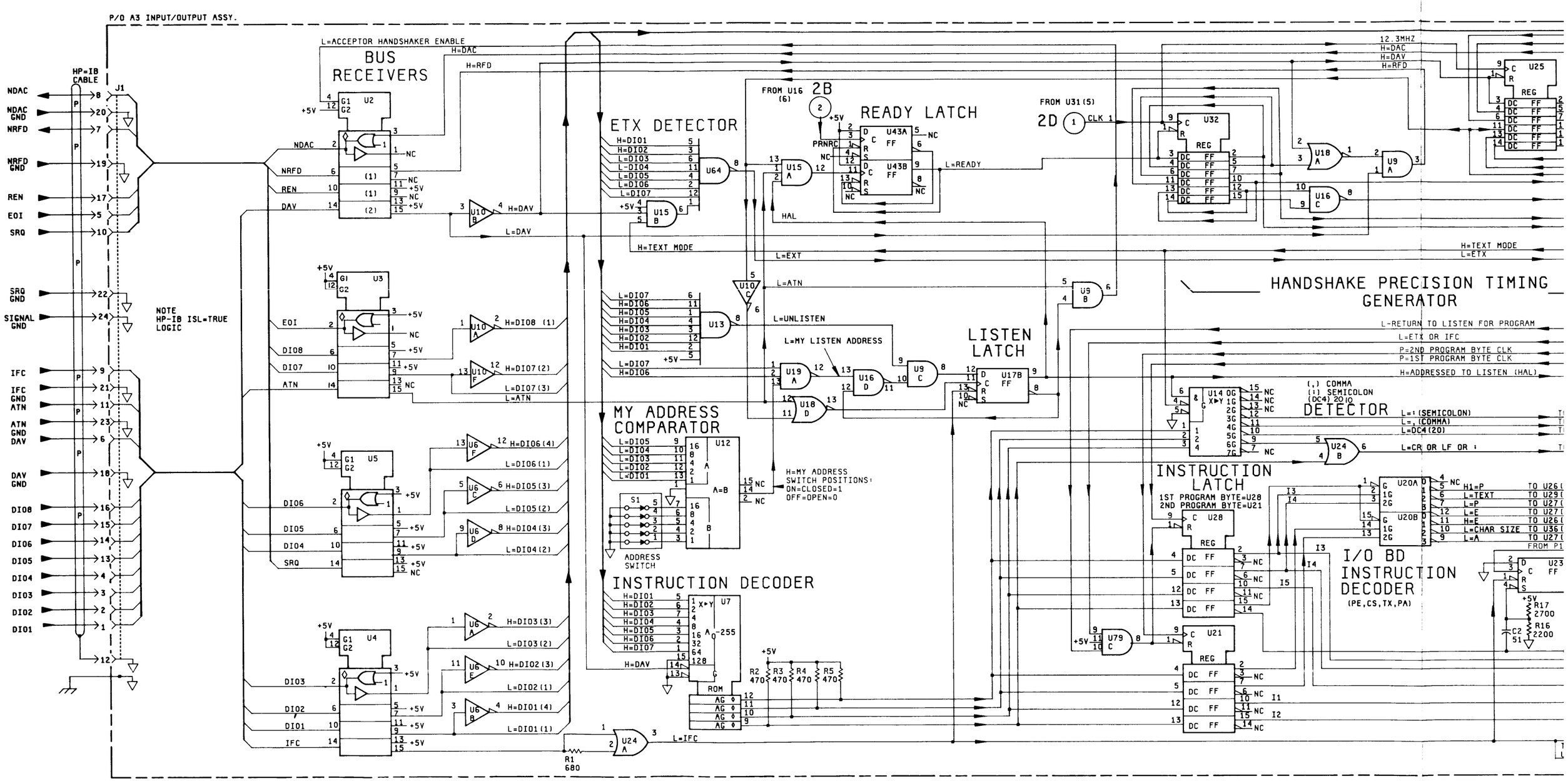
Figure 8-44. Power Supply Board A5 Component Locator,
- Replace figure 8-44 with figure 7-6.

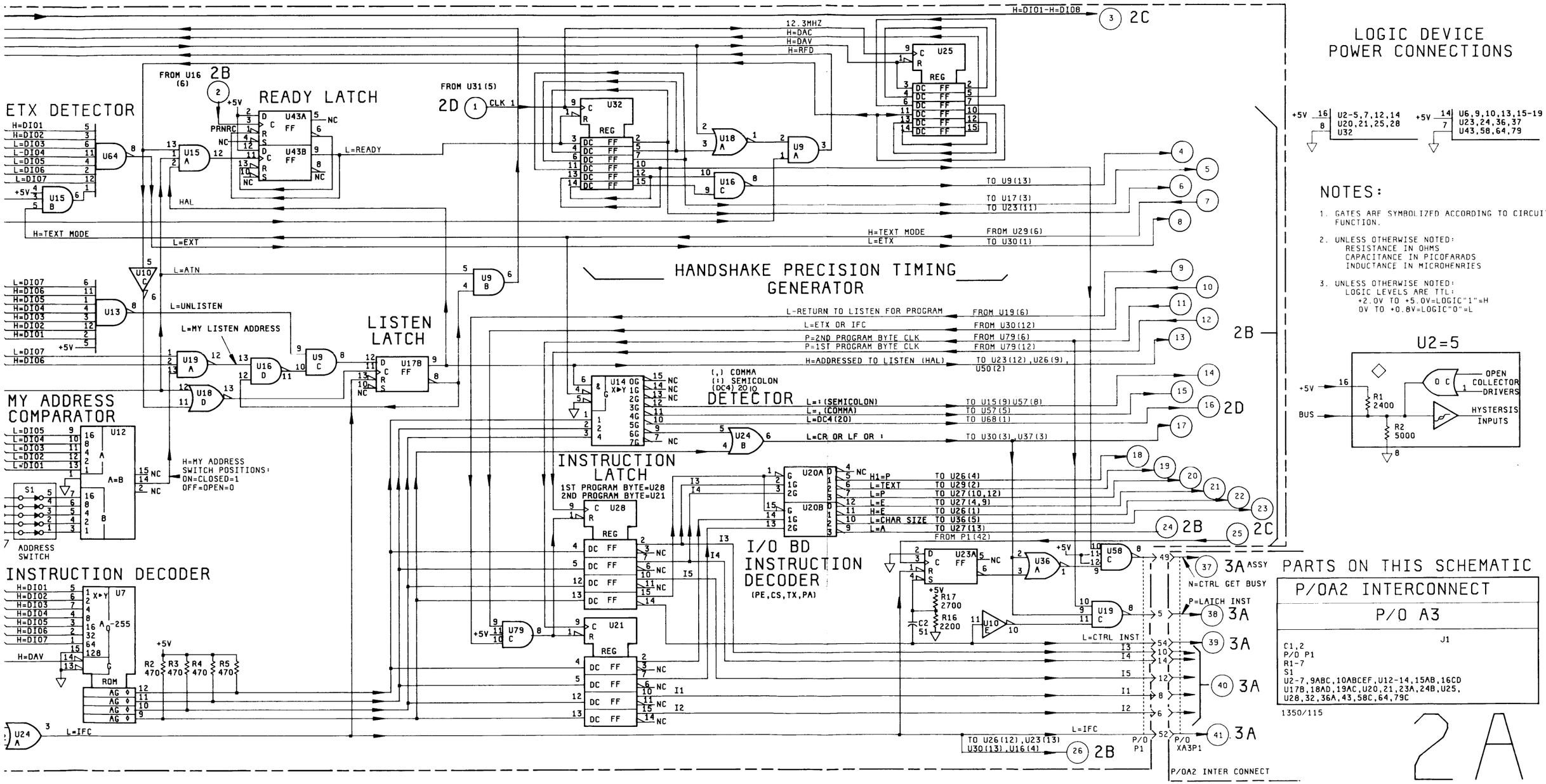
Figure 8-45 and 8-46. Schematics 6A and 6B,
- Replace schematics 6A and 6B with figures 7-7 and 7-8 respectively.



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	F-4	R10	C-6	U21	E-2
C2	K-6	R11	C-6	U22	F-6
C3	H-6	R12	F-2	U23	F-5
C4	G-6	R13	G-2	U24	F-5
C5	C-6	R14	K-6	U25	F-4
C6	G-1	R15	K-6	U26	F-3
C7	K-5	R16	K-6	U27	F-3
C8	G-3	R17	K-6	U28	F-2
C9	H-7	R18	J-5	U29	G-6
C10	I-2	R19	J-5	U30	G-5
C11	J-7	R20	G-3	U31	G-4
C12	I-7	R21	G-3	U32	G-4
C13	D-7	R22	K-7	U33	G-3
C14	C-7	R23	K-7	U34	G-3
C15	B-7	R24	K-7	U35	G-2
C16	B-7	R25	K-7	U36	H-6
C17	D-6	R26	K-7	U37	H-5
C18	D-7	R27	K-7	U38	H-5
C19	B-5	R28	K-7	U39	H-4
C20	B-7	R29	I-7	U40	H-3
C21	K-3	R30	I-7	U41	H-3
C22	D-6	R31	I-7	U42	H-2
C23	C-5	R32	K-6	U43	H-6
C24	C-4	R33	D-7	U44	I-5
C25	C-4	R34	B-7	U45	I-5
C26	C-3	R35	B-7	U46	I-4
C27	D-3	R36	J-7	U47	I-3
C28	E-6	R37	K-6	U48	I-3
C29	F-7	R38	H-7	U49	I-2
C30	F-7	R39	H-7	U50	I-6
C31	F-3	R40	H-7	U51	I-5
C32	F-2	R41	H-7	U52	I-5
C33	G-7	R42	B-7	U53	I-4
C34	G-6	R43	B-7	U54	I-3
C35	G-3	R44	B-7	U55	I-3
C36	H-4	R45	D-7	U56	I-2
C36	H-4	R46	B-5	U57	J-6
C37	I-7	R47	B-5	U58	J-5
C38	I-5	R48	B-5	U59	J-5
C39	I-5	R49	B-5	U60	J-4
C40	I-2	R50	K-7	U61	J-3
C41	J-7	R51	F-4	U62	J-3
C42	J-6	R52	G-4	U63	J-2
C43	J-5	S1	D-4	U64	B-2
C44	K-5	S2	I-7	U65	J-7
CR1	I-7	U1	C-6	U66	J-7
CR2	B-7	U2	C-5	U67	I-7
CR3	B-5	U3	C-5	U68	H-7
J1	A-3	U4	C-4	U69	H-7
J2	A-6	U5	C-3	U70	H-7
L1	K-2	U6	C-3	U71	G-7
P1	L-5	U7	C-2	U72	G-7
Q1	K-6	U8	D-6	U73	E-7
Q2	K-6	U9	D-5	U74	E-7
Q3	K-6	U10	D-5	U75	E-7
R1	F-4	U12	D-3	U76	D-7
R2	E-1	U13	D-3	U77	C-7
R3	D-1	U14	D-2	U78	C-7
R4	D-1	U15	E-6	U79	E-7
R5	E-1	U16	E-5	U80	K-4
R6	K-5	U17	E-5	U81	K-4
R7	K-5	U18	E-4	VR1	J-7
R8	G-6	U19	E-3		
R9	G-7	U20	E-3		

Figure 7-1.
Replacement for Input/Output Board A3 Component Locator (S/P 1906A)


P/O A3 INPUT/OUTPUT ASSY.
HP-IB CABLE
J1
NDAC
NDAC GND
NRFD
NRFD GND
REN
EOI
SRQ
SRQ GND
SIGNAL GND
IFC
IFC GND
ATN
ATN GND
DAV
DAV GND
DIO8
DIO7
DIO6
DIO5
DIO4
DIO3
DIO2
DIO1
NOTE HP-IB ISL=TRUE LOGIC
L=ACCEPTOR HANDSHAKER ENABLE
BUS RECEIVERS
H=DAC
H=RFD
H=DAV
L=DAV
ETX DETECTOR
H=TEXT MODE
L=EXT
L=ATN
L=UNLISTEN
L=MY LISTEN ADDRESS
READY LATCH
FROM U16 (6)
2B
FROM U31 (5)
2D
CLK
L=READY
HAL
12.3MHZ
H=DAC
H=DAV
H=RFD
HANDSHAKE PRECISION TIMING GENERATOR
L-RETURN TO LISTEN FOR PROGRAM
L=ETX OR IFC
P=2ND PROGRAM BYTE CLK
P=1ST PROGRAM BYTE CLK
H=ADDRESSED TO LISTEN (HAL)
LISTEN LATCH
MY ADDRESS COMPARATOR
H=MY ADDRESS SWITCH POSITIONS: ON=CLOSED=1 OFF=OPEN=0
ADDRESS SWITCH
INSTRUCTION DECODER
ROM
R1 680
L=IFC
(,) COMMA
(:) SEMICOLON
(DC4) 20 10
DETECTOR
L=: (SEMICOLON)
L=, (COMMA)
L=DC4 (20)
L=CR OR LF OR :
INSTRUCTION LATCH
1ST PROGRAM BYTE=U28
2ND PROGRAM BYTE=U21
I/O BD INSTRUCTION DECODER
(PE,CS,TX,PA)
H1=P
L=TEXT
L=P
L=E
H=E
L=CHAR SIZE
L=A
FROM P1
R17 2700
R16 2200
C2 51



LOGIC DEVICE POWER CONNECTIONS

+5V	16	U2-5,7,12,14 U20,21,25,28 U32
	8	
+5V	14	U6,9,10,13,15-19 U23,24,36,37 U43,58,64,79
	7	

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

U2=5

PARTS ON THIS SCHEMATIC

P/OA2 INTERCONNECT

P/O A3

J1

C1,2
P/O P1
R1-7
S1
U2-7,9ABC,10ABCEF,U12-14,15AB,16CD
U17B,18AD,19AC,U20,21,23A,24B,U25,
U28,32,36A,43,58C,64,79C

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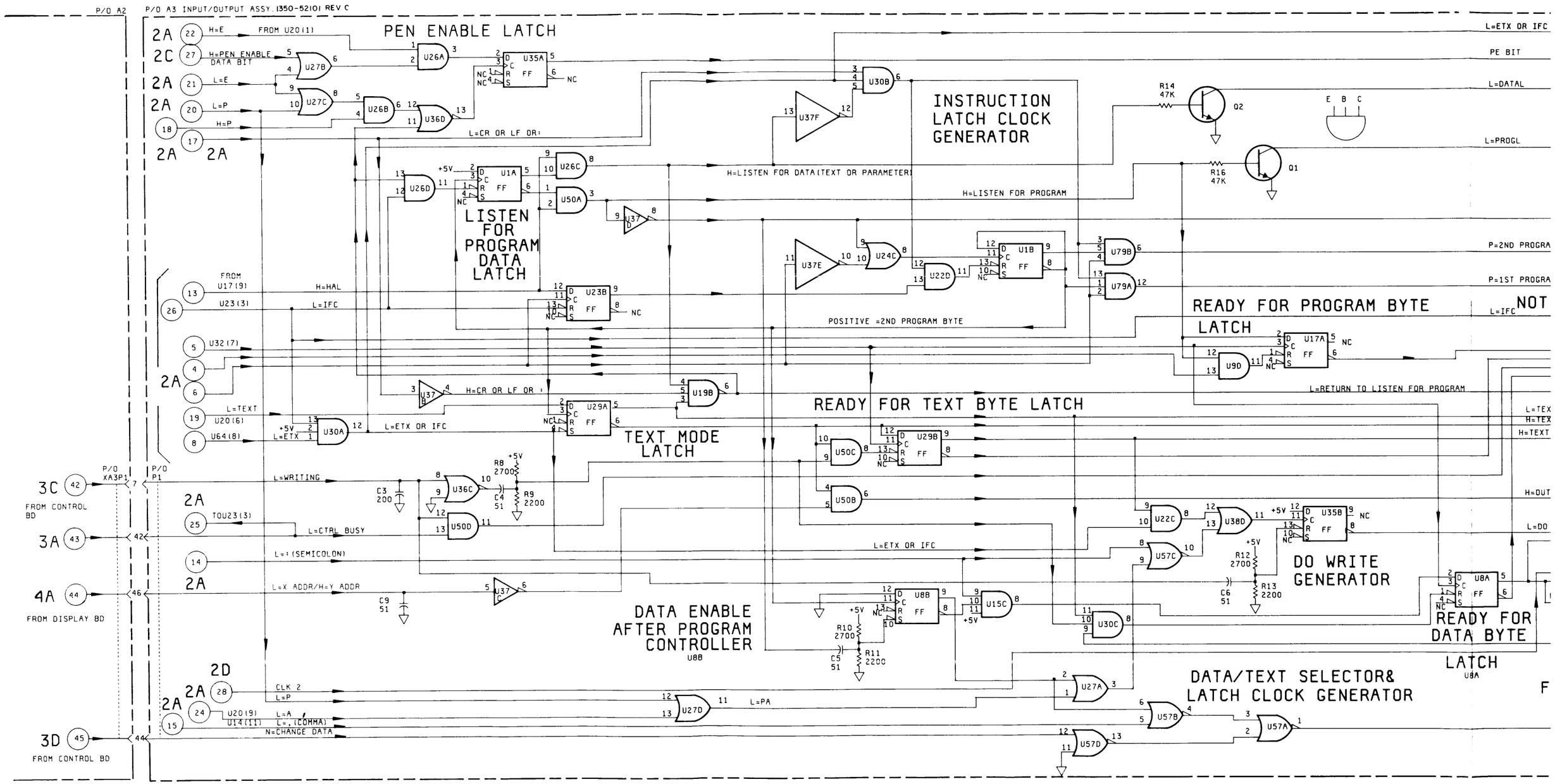
Figure 7-2. Replacement for Schematic 2A (S/P 1906A)


P/O A2
P/O A3 INPUT/OUTPUT ASSY. 1350-52101 REV C
PEN ENABLE LATCH
INSTRUCTION LATCH CLOCK GENERATOR
LISTEN FOR PROGRAM DATA LATCH
READY FOR PROGRAM BYTE LATCH
READY FOR TEXT BYTE LATCH
TEXT MODE LATCH
DO WRITE GENERATOR
DATA ENABLE AFTER PROGRAM CONTROLLER
U8B
READY FOR DATA BYTE LATCH
U8A
DATA/TEXT SELECTOR& LATCH CLOCK GENERATOR
FROM CONTROL BD
FROM DISPLAY BD
FROM CONTROL BD
H=E
FROM U20(1)
H=PEN ENABLE DATA BIT
L=E
L=P
H=P
L=CR OR LF OR:
H=LISTEN FOR DATA(TEXT OR PARAMETER)
H=LISTEN FOR PROGRAM
POSITIVE =2ND PROGRAM BYTE
L=ETX OR IFC
PE BIT
L=DATAL
L=PROGL
P=2ND PROGRA
P=1ST PROGRA
L=IFC
L=RETURN TO LISTEN FOR PROGRAM
H=HAL
L=IFC
H=CR OR LF OR :
L=ETX OR IFC
L=TEXT
L=ETX
L=WRITING
L=CTRL BUSY
L=: (SEMICOLON)
L=X ADDR/H=Y ADDR
CLK 2
L=P
L=A
L=, (COMMA)
N=CHANGE DATA
L=PA
L=DO
H=OUT
R14 47K
R16 47K
Q1
Q2
E B C
R8 2700
R9 2200
C3 200
C4 51
C9 51
R10 2700
R11 2200
C5 51
R12 2700
R13 2200
C6 51

INSTRUCTION LATCH CLOCK GENERATOR

H=LISTEN FOR DATA(TEXT OR PARAMETER)

H=LISTEN FOR PROGRAM

POSITIVE =2ND PROGRAM BYTE

READY FOR PROGRAM BYTE LATCH

READY FOR TEXT BYTE LATCH

TEXT MODE LATCH

DATA ENABLE AFTER PROGRAM CONTROLLER U8B

DO WRITE GENERATOR

READY FOR DATA BYTE LATCH U8A

NOT READY CONTOLLER

DATA/TEXT SELECTOR& LATCH CLOCK GENERATOR

FOUR STATE COUNTER U33

L=ETX OR IFC (L=CLEAR INSTRUCTION LATCH) TO 10 2A

PE BIT (H=PE1/L=PE0) P/O P1 33

L=DATAL R15 180 53

L=PROGL R17 180 51

P/O A2 P/O XA3P1 46 TO CONTROL BD 3B

47 6B

TO FRONT PANEL LEADS 48 6B

+5V 14 7 ALL IC SUPPLY CONFIGURATIONS

TO U22(5) 29 2C

P=2ND PROGRAM BYTE CLK TO U21(9) U19(10) 11 2A

P=1ST PROGRAM BYTE CLK TO U28(9) 12 2A

L=IFC

P=RNCR 2 2A 2C

9 2C

L=RETURN TO LISTEN FOR PROGRAM 9 2A

L=TEXT MODE 30 2C

H=TEXT MODE 7 2A

H=TEXT:L=BINARY DATA 31 2C

H=OUTPUT X AS 1023 (TEXT FLAG) 32 2C

L=DO WRITE 33 2D

34 2C

35 2C

48 49 3C TO CONTROL BD

L=PA

NEG=LATCH OUTPUT DATA 36 2C

TO U37(1),62(11) U56(11),22(4)

LOGIC DEVICE POWER CONNECTIONS

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A3

C3-9
Q1-2
R8-21
U1,8,9D,15C,16B,17A,19B,22CD
U23B,24C,26,27,29,30ABC,33,35
U36CD,37B-F,38D,50,57,58A,79AB

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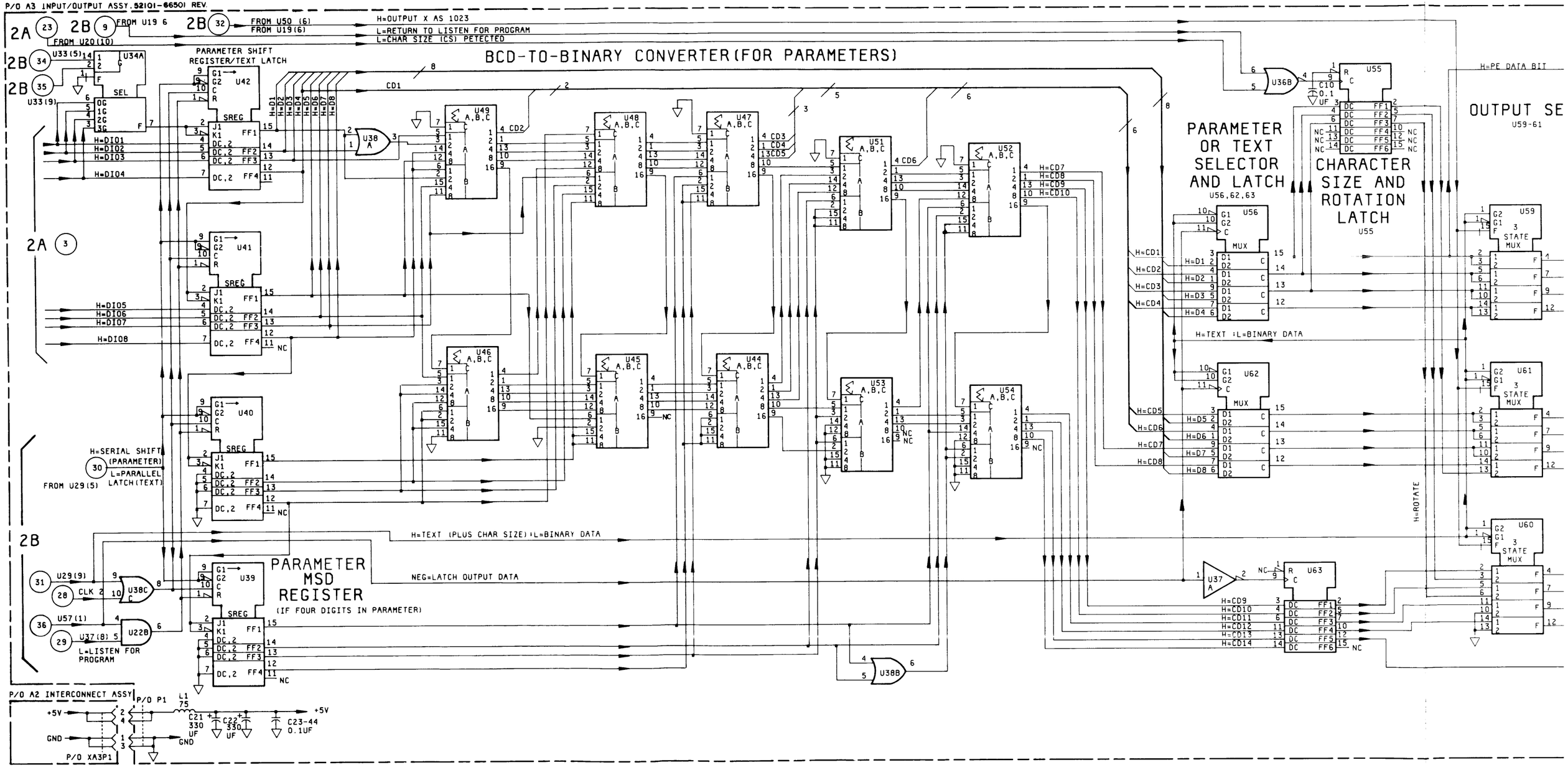
2B

Figure 7-3.
Replacement for Schematic 2B (S/P 1906A)


P/O A3 INPUT/OUTPUT ASSY 52101-66501 REV
BCD-TO-BINARY CONVERTER (FOR PARAMETERS)
PARAMETER SHIFT REGISTER/TEXT LATCH
PARAMETER MSD REGISTER
(IF FOUR DIGITS IN PARAMETER)
PARAMETER OR TEXT SELECTOR AND LATCH
U56,62,63
CHARACTER SIZE AND ROTATION LATCH
U55
OUTPUT SE
U59-61
FROM U19 6
FROM U50 (6)
FROM U19(6)
FROM U20(10)
H=OUTPUT X AS 1023
L=RETURN TO LISTEN FOR PROGRAM
L=CHAR SIZE (CS) DETECTED
H=PE DATA BIT
H=SERIAL SHIFT (PARAMETER) L=PARALLEL LATCH (TEXT)
FROM U29(5)
H=TEXT (PLUS CHAR SIZE) ;L=BINARY DATA
NEG=LATCH OUTPUT DATA
H=TEXT ;L=BINARY DATA
H=ROTATE
L=LISTEN FOR PROGRAM
P/O A2 INTERCONNECT ASSY
P/O XA3P1
P/O P1
+5V
GND
L1 75
C21 330 UF
C22 330 UF
C23-44 0.1UF
C10 0.1 UF

RY CONVERTER(FOR PARAMETERS)

P/O A2 INTERCONNECT ASSY

TO U27(5)

H=PE DATA BIT → 27 2B

OUTPUT SELECTOR
U59-61

PARAMETER OR TEXT SELECTOR AND LATCH
U56,62,63

CHARACTER SIZE AND ROTATION LATCH
U55

U36B

C10 0.1 UF

U48 A,B,C

U47 A,B,C

U51 A,B,C

U52 A,B,C

U45 A,B,C

U44 A,B,C

U53 A,B,C

U54 A,B,C

4 CD3
1 CD4
13 CD5
4 CD6
4 H=CD7
1 H=CD8
13 H=CD9
10 H=CD10

U56 MUX
U62 MUX

H=CD1
H=CD2
H=CD3
H=CD4
H=CD5
H=CD6
H=CD7
H=CD8
H=D1
H=D2
H=D3
H=D4
H=D5
H=D6
H=D7
H=D8

H=TEXT ;L=BINARY DATA

U59 3 STATE MUX
U61 3 STATE MUX
U60 3 STATE MUX

U80 180 +5V
U81 180 +5V

ID1
ID2
ID3
ID4
ID5
ID6
ID7
ID8
ID9
ID10
ID11
ID12
ID13

P/O P1
P/O XA3P1

50 3B
TO CONTROL BD
HIGH TRUE

H=ROTATE

U37 A

U63

H=CD9
H=CD10
H=CD11
H=CD12
H=CD13
H=CD14

U38B

NC
NC

P1 PINS NOT CONNECTED:
11,13,15,16,26,28,30,32,
34-41,43,47,55,56,59-70,74,
76-79,81-84,87-100

H=VECT 0 → 73 76 3C

LOGIC DEVICE POWER CONNECTIONS

+5V 14 7 U22,36-38

+5V 16 8 U34,39-42,44-49 U51-56,59-63

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC "1"=H
   0V TO +0.8V=LOGIC "0"=L

PARTS ON THIS SCHEMATIC

P/O A3

C10,21-44
L1
P/O P1
U22B,34,36B,37A,38A,B,C
U39-42,44-49,51-56,59-63
U80,81

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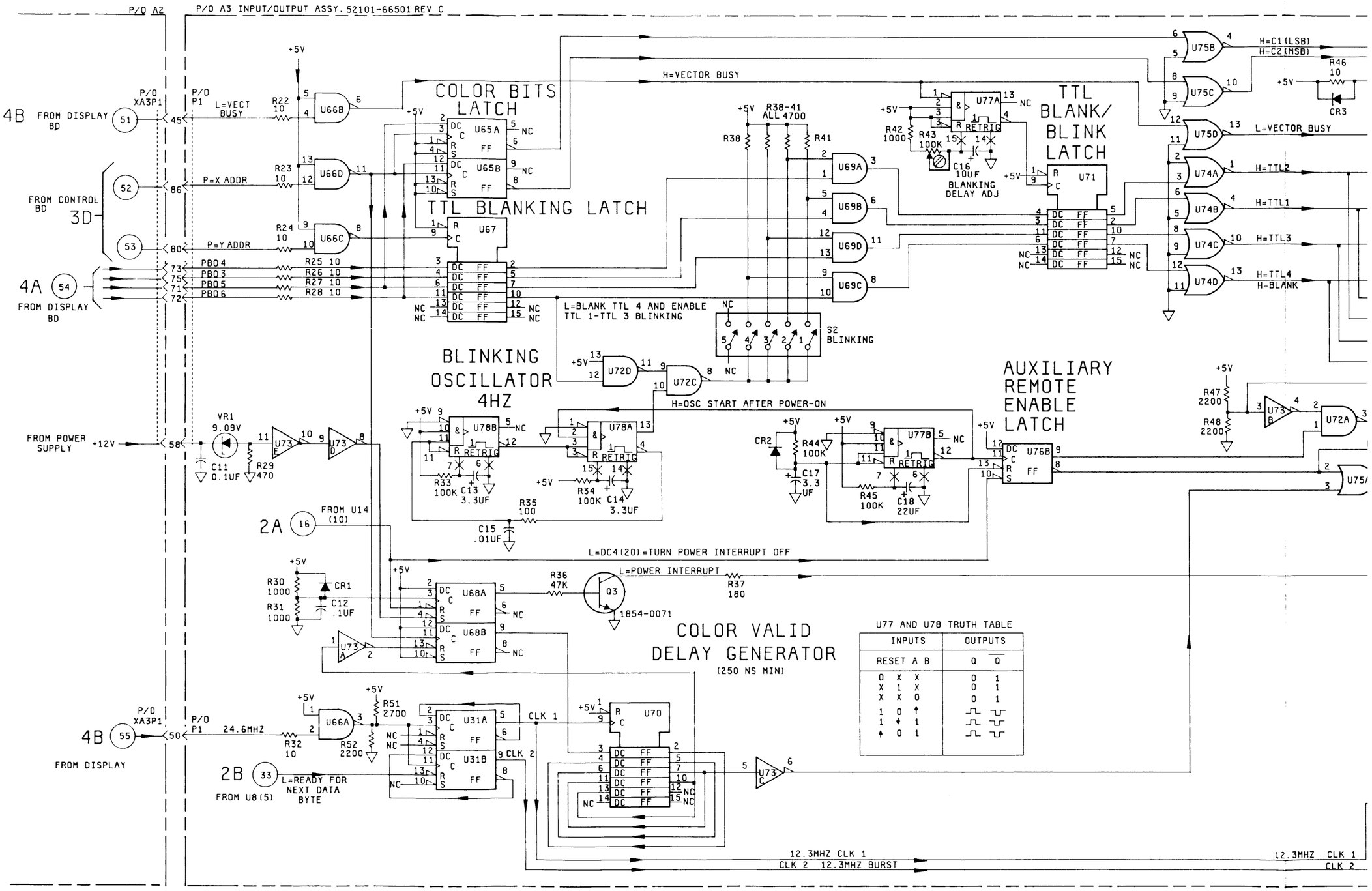
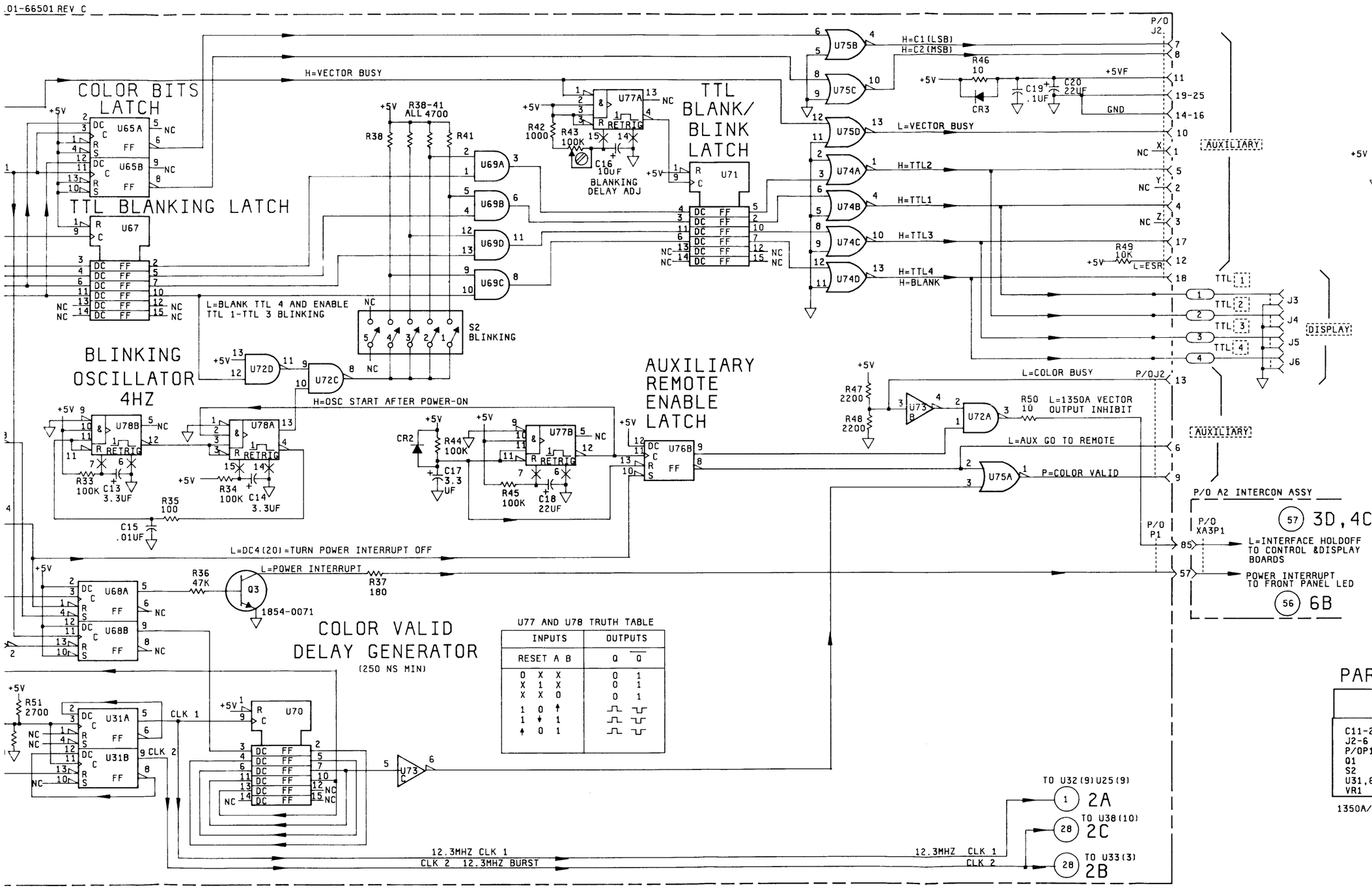
2C

Figure 7-4. Replacement for Schematic 2C (S/P 1906A)

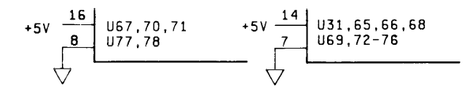

P/O A2
P/O A3 INPUT/OUTPUT ASSY. 52101-66501 REV C
4B FROM DISPLAY BD
P/O XA3P1
P/O P1
L=VECT BUSY
FROM CONTROL BD 3D
P=X ADDR
P=Y ADDR
4A FROM DISPLAY BD
PB0 4
PB0 3
PB0 5
PB0 6
R22 10
R23 10
R24 10
R25 10
R26 10
R27 10
R28 10
U66B
U66D
U66C
+5V
COLOR BITS LATCH
U65A
U65B
TTL BLANKING LATCH
U67
H=VECTOR BUSY
R38-41 ALL 4700
R38
R41
U69A
U69B
U69D
U69C
L=BLANK TTL 4 AND ENABLE TTL 1-TTL 3 BLINKING
S2 BLINKING
U77A
R42 1000
R43 100K
C16 10UF
BLANKING DELAY ADJ
TTL BLANK/ BLINK LATCH
U71
U75B
U75C
U75D
U74A
U74B
U74C
U74D
H=C1(LSB)
H=C2(MSB)
R46 10
CR3
L=VECTOR BUSY
H=TTL2
H=TTL1
H=TTL3
H=TTL4
H=BLANK
FROM POWER SUPPLY +12V
VR1 9.09V
C11 0.1UF
R29 470
U73F
U73D
BLINKING OSCILLATOR 4HZ
U78B
U78A
R33 100K
C13 3.3UF
R34 100K
C14 3.3UF
R35 100
C15 .01UF
2A
FROM U14 (10)
H=OSC START AFTER POWER-ON
CR2
R44 100K
C17 3.3 UF
R45 100K
C18 22UF
U77B
U72D
U72C
AUXILIARY REMOTE ENABLE LATCH
R47 2200
R48 2200
U73B
U72A
U75A
L=DC4(20)=TURN POWER INTERRUPT OFF
L=POWER INTERRUPT
R36 47K
Q3
1854-0071
R37 180
R30 1000
R31 1000
CR1
C12 .1UF
U68A
U68B
U73A
COLOR VALID DELAY GENERATOR
(250 NS MIN)
U77 AND U78 TRUTH TABLE
INPUTS
RESET A B
OUTPUTS
Q Q
4B FROM DISPLAY
P/O XA3P1
P/O P1
24.6MHZ
R32 10
U66A
R51 2700
R52 2200
U31A
U31B
CLK 1
CLK 2
2B FROM U8(5)
L=READY FOR NEXT DATA BYTE
U70
U73C
12.3MHZ CLK 1
CLK 2 12.3MHZ BURST



U77 AND U78 TRUTH TABLE

INPUTS	OUTPUTS
RESET A B	Q $\overline{Q}$
0 X X	0 1
X 1 X	0 1
X X 0	0 1
1 0 ↑	⊓ ⊔
1 ↓ 1	⊓ ⊔
↑ 0 1	⊓ ⊔

LOGIC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. J1-6 AND HARDWARE IS PART OF A3 I/O ASSY(52101-66501)

BINARY COLOR CODE

FILE NAME	COLOR	C1(LSB) PIN 7	C2(MSB) PIN 8
16-31	YELLOW	0	1
32-47	RED	1	0
48-63*	YELLOW	0	0
0-15	GRN	1	1

*FILES 48-63 NOT USED DUE TO "WRAP AROUND". SEE 1350A OPERATING AND PROGRAMMING MANUAL.

PARTS ON THIS SCHEMATIC

P/O A3	
C11-20	CR1-3
J2-6	
P/OP1	
Q1	
S2	
U31,65-78	
VR1	

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2D

Figure 7-5.
Replacement for Schematic 2D (S/P 1906A)

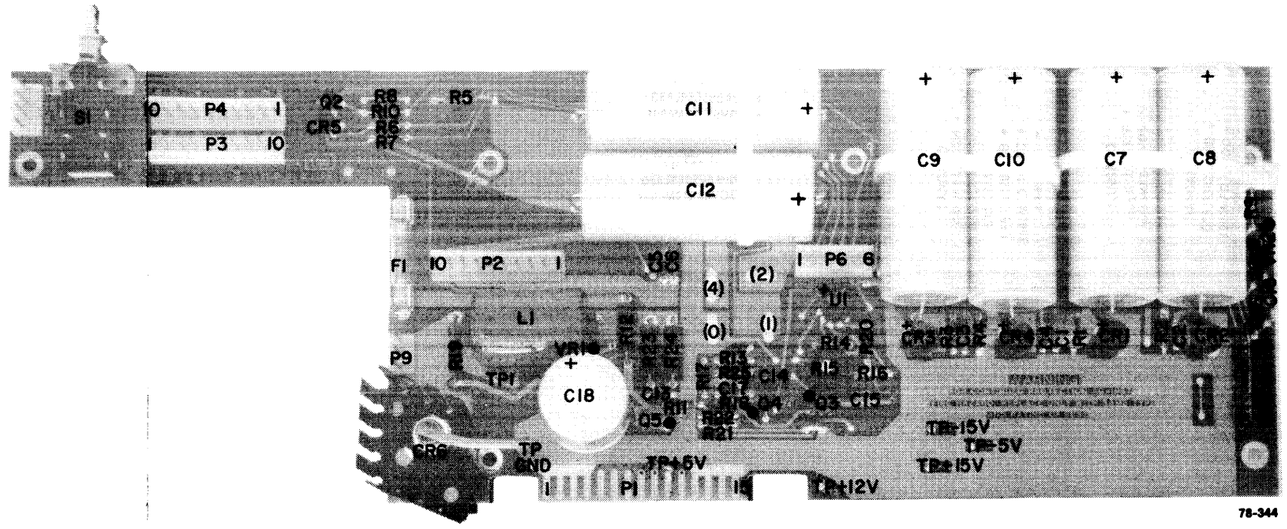
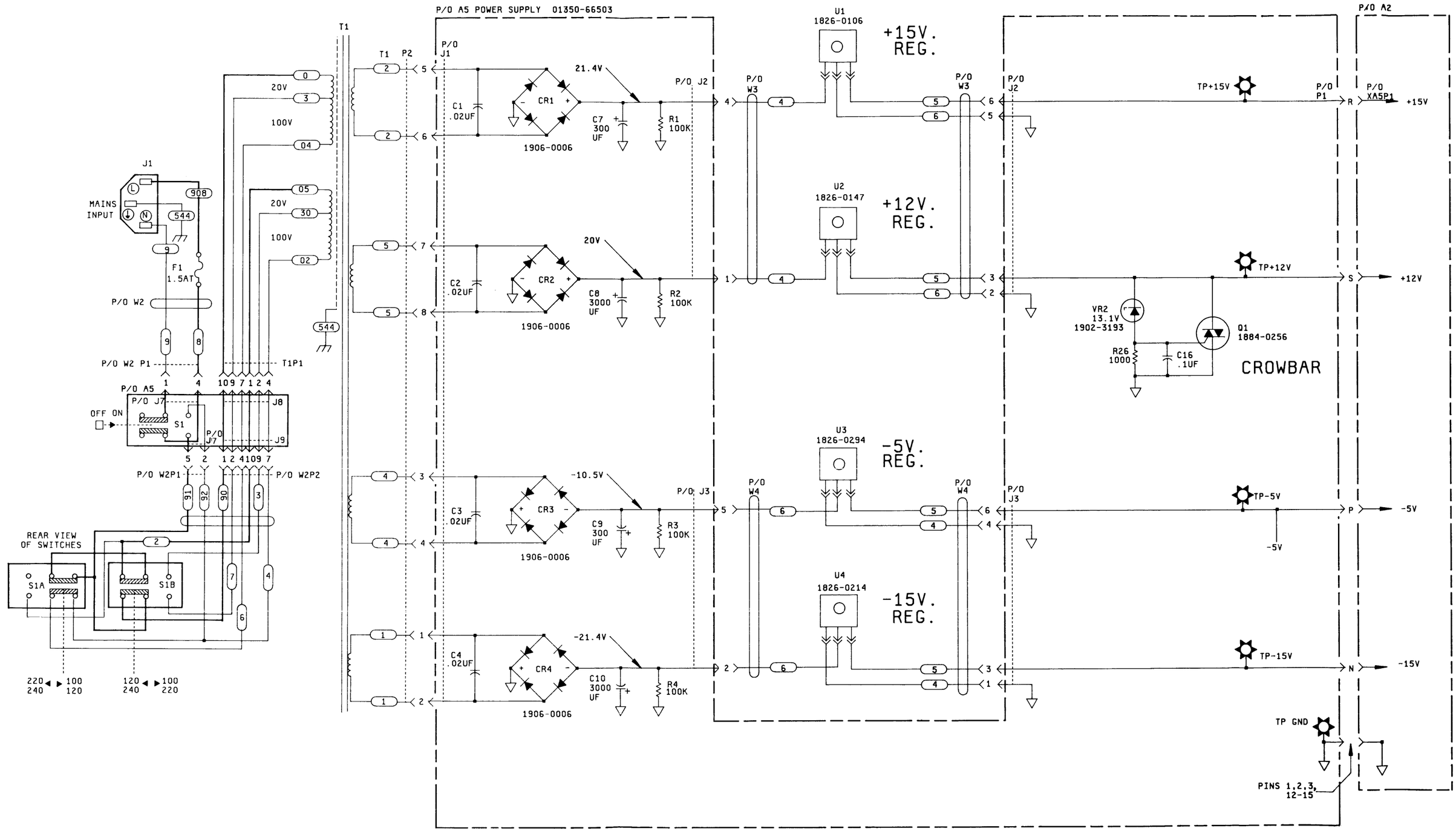
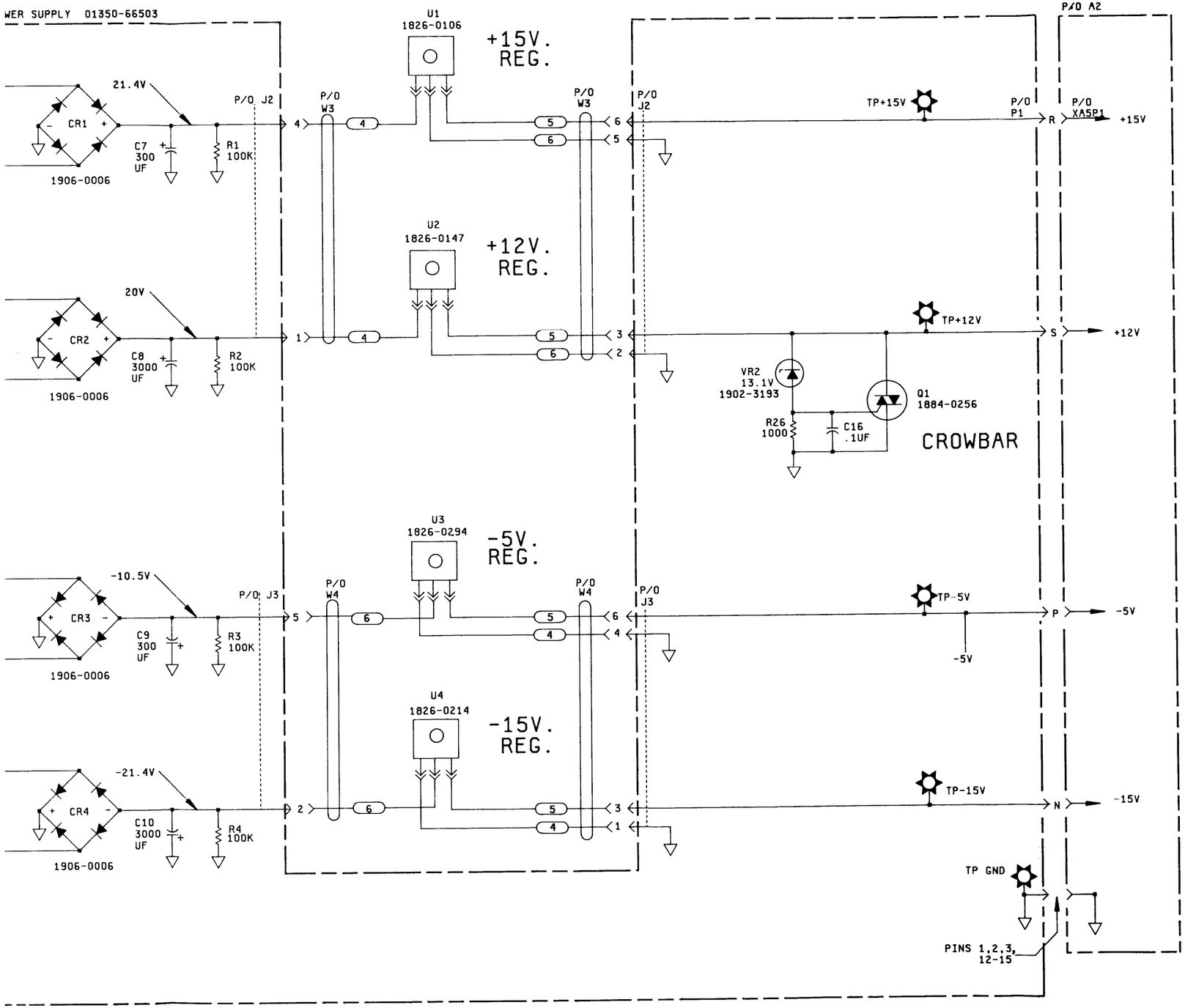


Figure 7-6. Replacement for Power Supply Board A5 Component Locator (S/P 1750A)


P/O A5 POWER SUPPLY 01350-66503
P/O A2
T1
J1
MAINS INPUT
L
N
908
544
9
F1
1.5AT
P/O W2
P/O W2 P1
T1P1
P/O A5
P/O J7
J8
J9
OFF ON
S1
P/O W2P1
P/O W2P2
REAR VIEW OF SWITCHES
S1A
S1B
220 240
100 120
120 240
100 220
0
3
04
05
30
02
20V
100V
T1 P2
P/O J1
C1 .02UF
CR1
1906-0006
21.4V
C7 300 UF
R1 100K
P/O J2
C2 .02UF
CR2
20V
C8 3000 UF
R2 100K
C3 .02UF
CR3
-10.5V
C9 300 UF
R3 100K
P/O J3
C4 .02UF
CR4
-21.4V
C10 3000 UF
R4 100K
P/O W3
P/O W4
U1
1826-0106
+15V. REG.
U2
1826-0147
+12V. REG.
U3
1826-0294
-5V. REG.
U4
1826-0214
-15V. REG.
TP+15V
TP+12V
TP-5V
TP-15V
TP GND
+15V
+12V
-5V
-15V
VR2
13.1V
1902-3193
Q1
1884-0256
R26
1000
C16
.1UF
CROWBAR
PINS 1,2,3, 12-15



NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
2. 120HZ RIPPLE ON +15V SUPPLIES
   MUST NOT EXCEED 0.050V P-P

PARTS ON THIS SCHEMATIC

A4	A5	A2	CHASIS
C110 J1 R168-171	C1-4,7-10, 16 CR1-4 P/O J1,2,3, 7-9 Q1 R1-4,26, VR 2	P/O XA5P1	B1 F1 J1 Q2 S1A,B P/O T1 U1-4 W2-4,7

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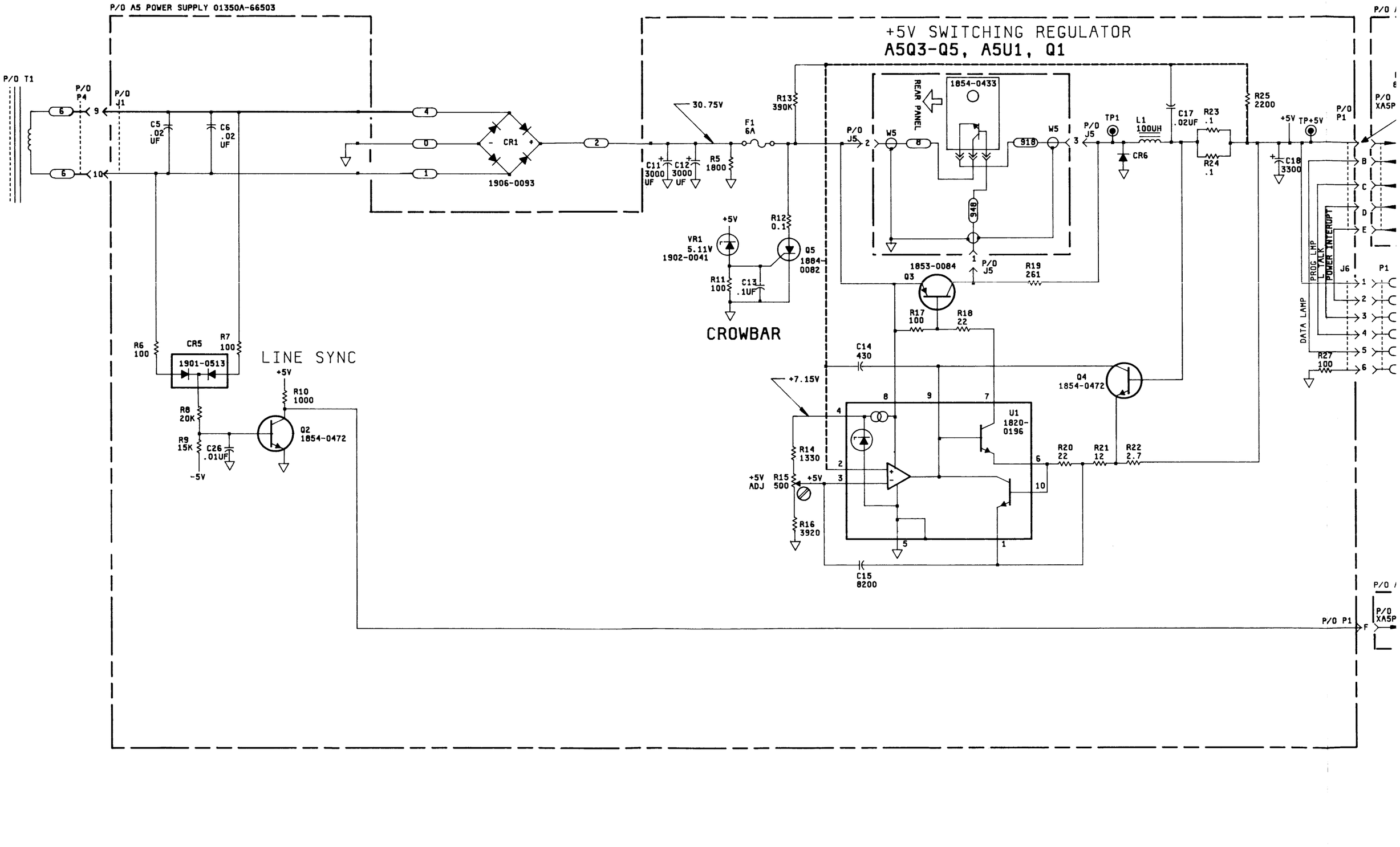
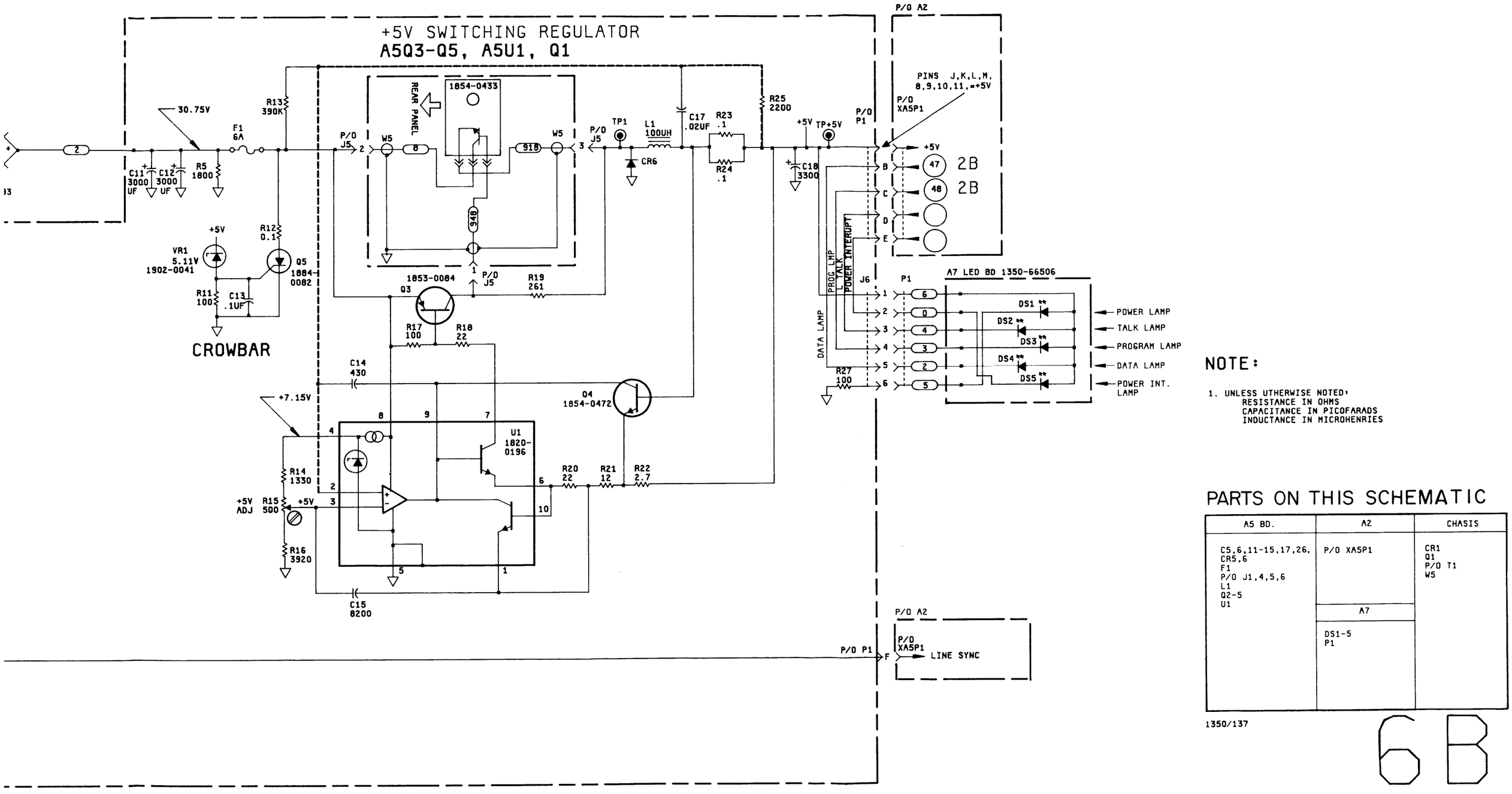
6A

Figure 7-7.
Replacement for Schematic 6A (S/P 1750A)


P/O A5 POWER SUPPLY 01350A-66503
+5V SWITCHING REGULATOR
A5Q3-Q5, A5U1, Q1
P/O T1
P/O P4
P/O J1
C5 .02 UF
C6 .02 UF
CR1
1906-0093
30.75V
F1 6A
R13 390K
C11 3000 UF
C12 3000 UF
R5 1800
REAR PANEL
1854-0433
P/O J5
W5
918
948
P/O TP1
L1 100UH
C17 .02UF
R23 .1
R24 .1
R25 2200
+5V
TP+5V
C18 3300
P/O P1
P/O XA5P
+5V
VR1 5.11V 1902-0041
R12 0.1
Q5 1884-0082
R11 100
C13 .1UF
CROWBAR
1853-0084
Q3
P/O J5
R19 261
R17 100
R18 22
C14 430
+7.15V
Q4 1854-0472
U1 1820-0196
R14 1330
+5V ADJ
R15 500
+5V
R16 3920
C15 8200
R20 22
R21 12
R22 2.7
R6 100
CR5
1901-0513
R7 100
LINE SYNC
+5V
R10 1000
R8 20K
R9 15K
C26 .01UF
-5V
Q2 1854-0472
J6
P1
PROG LMP
TALK
POWER INTERRUPT
DATA LAMP
R27 100
P/O P1
P/O XA5P



NOTE:

1. UNLESS UTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES

PARTS ON THIS SCHEMATIC

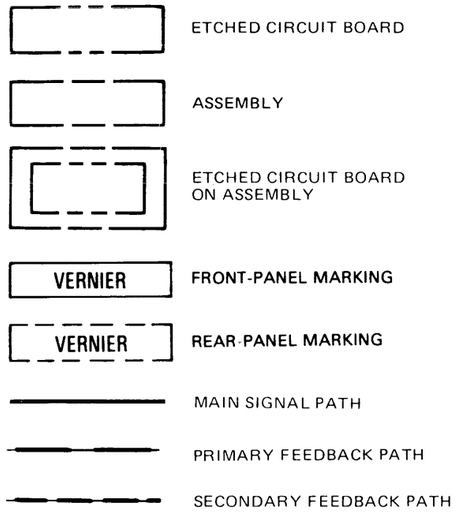
A5 BD.	A2	CHASIS
C5,6,11-15,17,26, CR5,6 F1 P/O J1,4,5,6 L1 Q2-5 U1	P/O XA5P1	CR1 Q1 P/O T1 W5
	A7	
	DS1-5 P1	

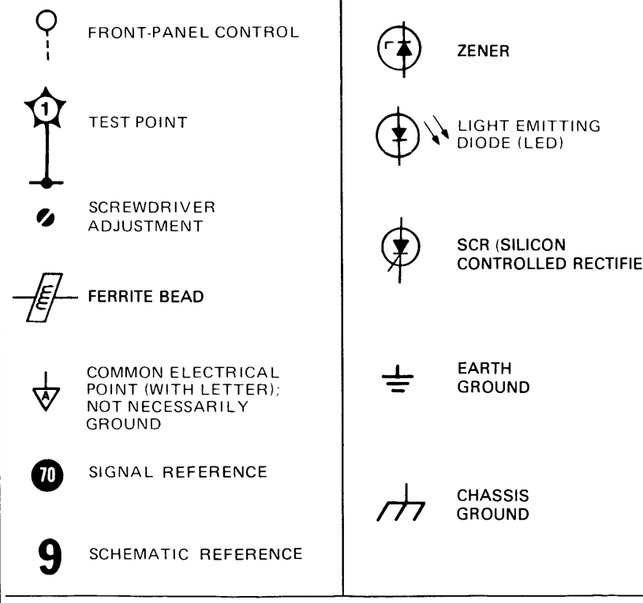
1350/137

6B

Figure 7-8.
Replacement for Schematic 6B (S/P 1750A)

REFER TO ANSI Y 32.2 AND Y32.14 FOR SCHEMATIC SYMBOLS NOT LISTED IN THIS TABLE.





CW	CLOCKWISE END OF VARIABLE RESISTOR	VF (A)	V - VOLTAGE
NC	NO CONNECTION		F - FILTERED
P/O	PART OF		(A) - FILTER SOURCE

Figure 8-1. Schematic Diagram Symbols

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section provides instructions for troubleshooting and repairing the Model 1350A Graphics Translator.

8-3. Detailed theory of operation and troubleshooting information are located opposite the schematics on foldout Service Sheets.

8-4. The Service Sheets are organized so that all schematics for each printed circuit (PC) board are grouped together. A component locator is provided for each group of schematics.

8-5. THEORY OF OPERATION.

8-6. A brief "get acquainted" description of 1350A operation is provided with the Simplified Block Diagram (figure 8-5). An overview of each PC board precedes the detailed theory for each group of schematics. The detailed theory is located opposite each schematic in a group. Figure 8-1 explains symbols that appear on the schematics.

8-7. LOGIC CONVENTIONS. Positive logic convention is used in this manual, unless otherwise noted on the schematics. Positive logic convention defines a logic "1" as the more positive voltage (high) and a logic "0" as the more negative voltage (low).

8-8. MNEMONICS. Signals in the 1350A have been assigned mnemonics that describe the active state and function of the signal line. A prefix letter (H,L,P, or N) indicates the active state of the signal. The remainder of the signal name indicates function of the signal. An H prefix indicates the function is active in the high state; an L prefix indicates the function is active in the low state. For edge-controlled devices, the prefix P indicates the function is active on the positive-going transition; prefix N indicates the function is active on the negative-going transition.

8-9. LOGIC SYMBOLOGY. This manual uses logic symbols as per American National Standards Institute standard Y32.14-1973. The purpose of these symbols is to graphically represent device functions so that operation can be understood without having to "look up" how a device works. Figures 8-2 and 8-3 show examples of ANSI Y32.14 symbols.

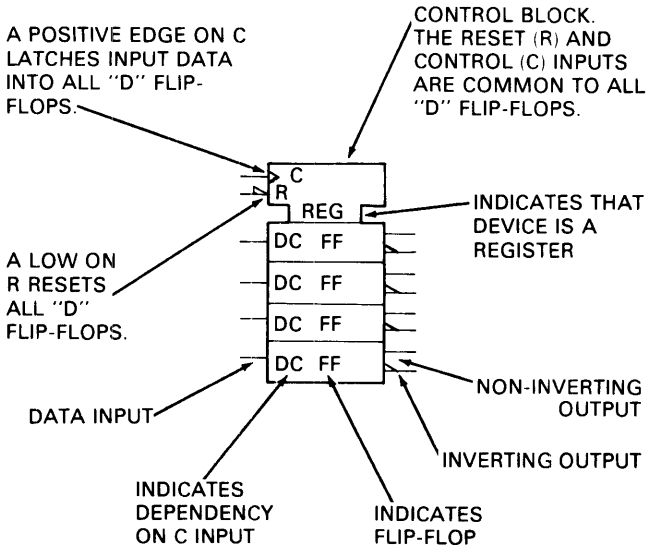


Figure 8-2. Symbol for a Quad D Flip-Flop

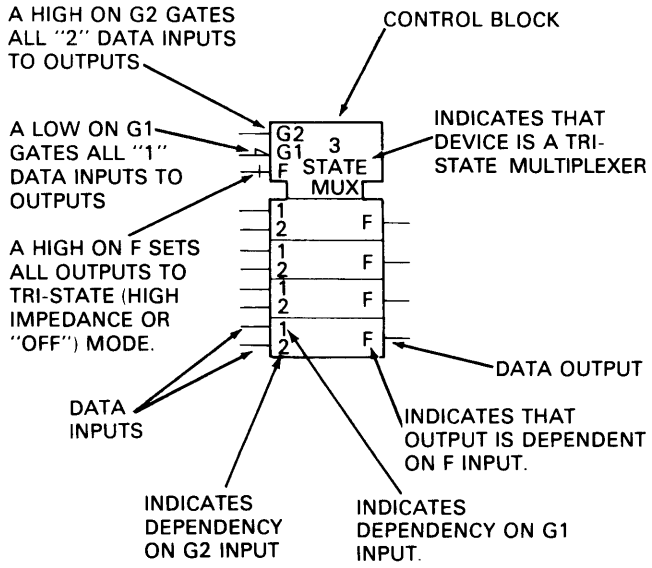


Figure 8-3. Symbol for a Quad Data Selector/Multiplexer

8-10. TROUBLESHOOTING.

WARNING

Maintenance and troubleshooting procedures described herein are performed with power applied to the instrument and protective covers removed. Service should be performed only by qualified personnel who are aware of hazards involved (such as fire or electrical shock). Read the Safety Summary at the front of this manual before troubleshooting the instrument.

8-11. TROUBLESHOOTING PROCEDURE. Before troubleshooting in detail, try to perform the adjustment procedures in Section V of this manual. Some apparent malfunctions may be corrected by these adjustments. Failure to obtain a correct adjustment may reveal the source of trouble.

8-12. If trouble is suspected, visually inspect the instrument. Look for loose or burned components that might suggest a source of trouble.

8-13. Verify that all circuit board connections are making good contact and are not shorting to an adjacent circuit. Sometimes a problem can be solved by cleaning printed circuit edge connectors with a pencil eraser and a clean cloth.

8-14. Check instrument power-supply voltages and external power source.

8-15. The most important prequisites for successful troubleshooting are: (a) an understanding of 1350A programming; and (b) a knowledge of 1350A circuit operation. An improper response to a programming command will often isolate the problem to a specific area.

8-16. TROUBLE DIAGNOSIS. A troubleshooting flow chart (figure 8-4) uses common symptoms to isolate the fault to a printed circuit board within the 1350A. Troubleshooting procedures for individual boards are located with the service sheet for that board.

8-17. Since the 1350A is used in systems along with an X-Y display and a computer, any suspected fault should first be isolated to a specific instrument in the system. Suspected 1350A malfunctions may actually be malfunctions in the X-Y display or in the computer.

8-18. PREVENTIVE MAINTENANCE.

8-19. Cleaning. Painted surfaces can be cleaned with a commercial , spray-type window cleaner or with a mild soap and water solution.

CAUTION

Avoid the use of chemical cleaning agents that might damage the plastics used in this instrument. Recommended cleaning agents are isopropyl alcohol, kelite (1 part kelite, 20 parts water), or a solution of 1% mild detergent and 99% water.

8-20. Corroded spots are best removed with soap and water. Stubborn residues can be removed with a fine abrasive. Protect such areas from further corrosion with an application of silicone resin such as GE DRIFILM 88.

8-21. QUICK REFERENCE TO SERVICE SHEETS.

8-22. Table 8-1 provides a quick reference to figures contained in the Service Sheets.

Table 8-1. Service Sheet Quick Reference

Fig. No.	Title
8-4	Troubleshooting Flow Chart (for board isolation)
8-5	Schematic 1A. Simplified Block Diagram
8-6	Schematic 1B. 1350A Wiring and Interconnect Diagram
8-7	Schematic 1C. Interface Board A2 Schematic
8-8	Input/Output Board A3 Block Diagram
8-9	1350A Memory Organization
8-10	HP-IB Handshake Sequence for Data Transfer
8-11	Input/Output Board A3 Component Locator
8-12	Schematic 2A
8-13	Plot Absolute DO WRITE, WRITING, CHANGE DATA Sequence
8-14	Text Mode DO WRITE, WRITING, CHANGE DATA Sequence
8-15	Schematic 2B
8-16	Schematic 2C
8-17	Schematic 2D
8-18	Control Board A1 Block Diagram
8-19	Control Instruction Handshake Timing
8-20	Typical Frame and File Detector Response to BF
8-21	Control Board A1 Component Locator
8-22	Schematic 3A
8-23	Schematic 3B
8-24	Pointer Control Signal Timing
8-25	Schematic 3C
8-26	Memory Timing Signals
8-27	Schematic 3D
8-28	Schematic 3E
8-29	Display Board A4 Troubleshooting Flow Chart
8-30	Simplified Block Diagram for Schematic 4A
8-31	Component Locator for Schematic 4A
8-32	Schematic 4A
8-33	Simplified Block Diagram for Schematics 4B-4E
8-34	Rate Multiplier Timing Diagram

Table 8-1. Service Sheet Quick Reference (Cont'd)

Fig. No.	Title
8-35	Vector Generation Timing Diagram
8-36	Component Locator for Schematic 4B, part of Schematic 4C, and Schematic 4D
8-37	Schematic 4B
8-38	Schematic 4C
8-39	Schematic 4D
8-40	Component Locator for Schematic 4E and part of Schematic 4C
8-41	Schematic 4E
8-42	Character Generator Board A6 Component Locator
8-43	Schematic 5
8-44	Power Supply Board A5 Component Locator
8-45	Schematic 6A
8-46	Schematic 6B
8-47	1350A Adjustment Locations

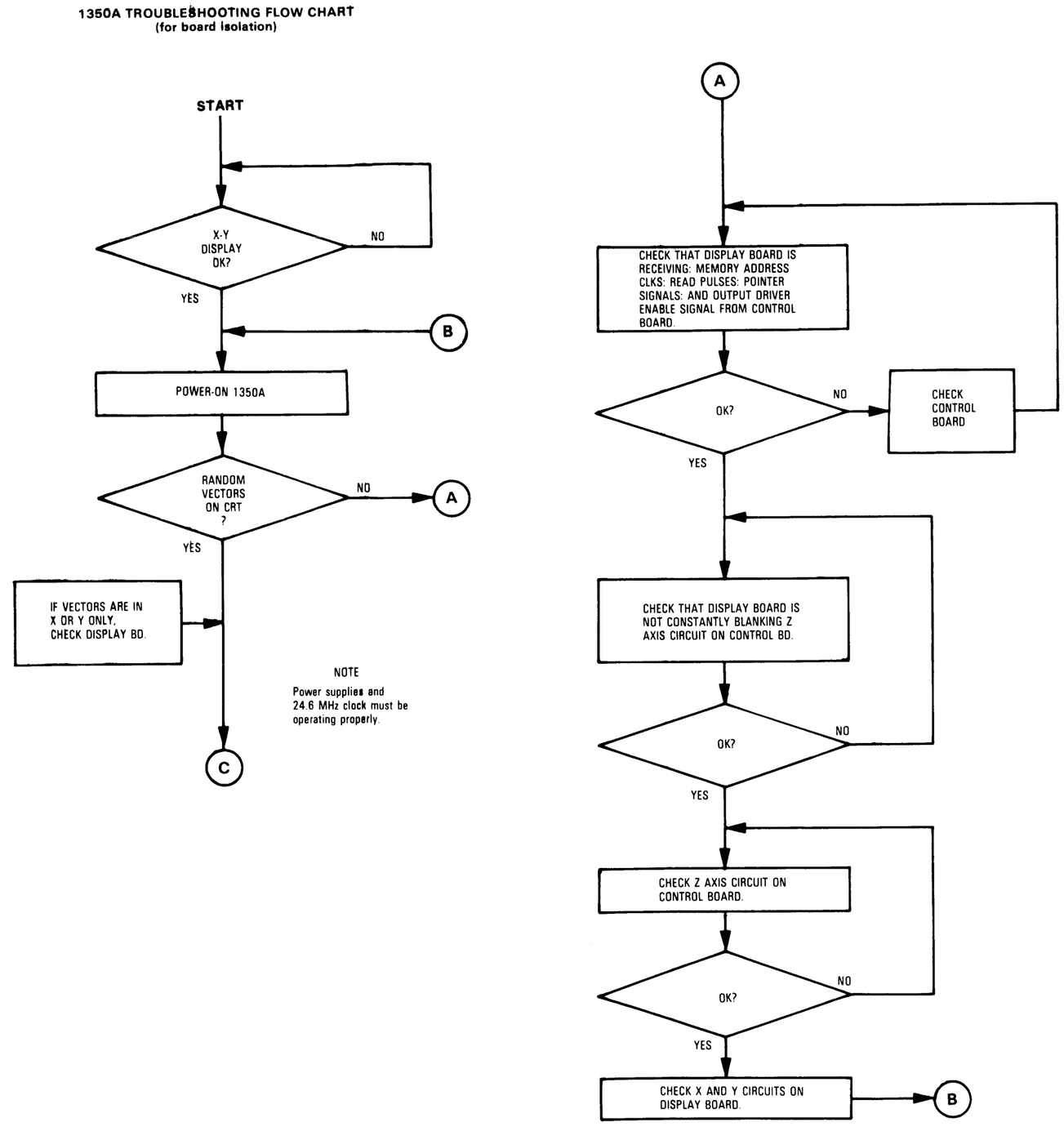


Figure 8-4.
Troubleshooting Flow Chart (for board isolation) (Sheet 1 of 2)

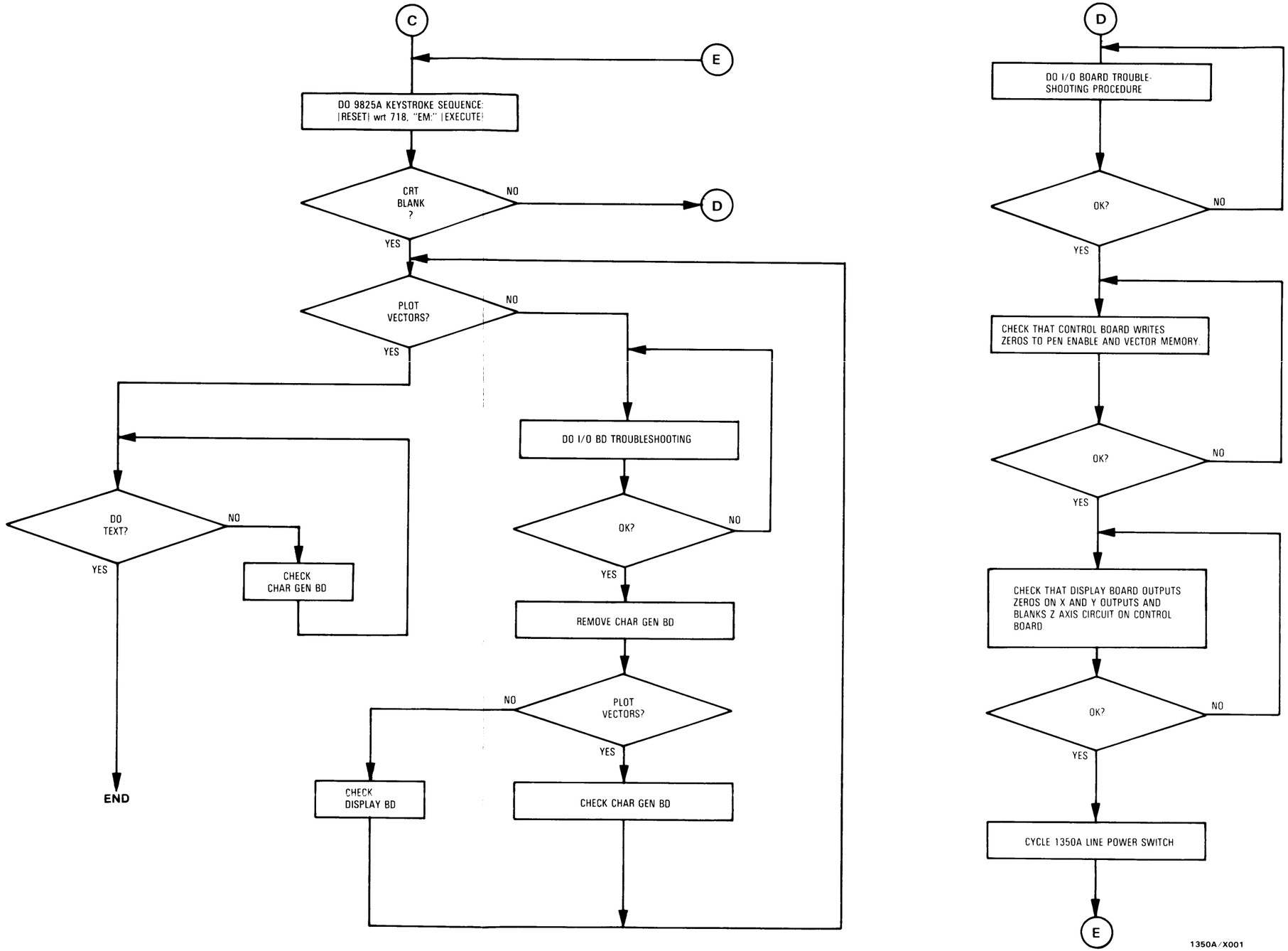


Figure 8-4. Troubleshooting Flow Chart (for board isolation (Sheet 2 of 2)

8-23. SIMPLIFIED BLOCK DIAGRAM DESCRIPTION (SERVICE SHEET 1).

Memory is the heart of the 1350A. Digital information from memory produces the X, Y, and Z analog signals that "draw" vectors on a CRT. This Display Memory, along with Vector Generator circuits, is located on the Display Board (schematics 4A-4E).

Information is read from (or written to) memory via the Control Board (schematics 3A-3E). The Control and Display boards "talk" to each other. The Control Board clocks the memory address counter and determines the type of memory cycle. On a memory-read cycle, the Display Board tells the Control Board to "wait" until the vector (as determined by memory data output from the read operation) has been completed. Upon vector completion, the Display Board signals "done" and the Control Board increments the address counter for the next memory cycle.

At power-on, random vectors appear on the CRT. Memory cells power up in an indeterminate manner (high or low at each location). The "conversation" between the Control and Display boards causes the entire memory to be scrolled through. As each location in memory is read, it outputs its "nonsense" data, contributing to the "garbage" on the CRT.

The Input/Output (I/O) Board receives commands from outside the 1350A. The I/O Board then tells the Control Board to write this meaningful data into memory.

Before vector (or character) data is sent to the I/O Board, the I/O Board should first receive commands that cause the Control Board to erase all random power-on data from memory.

When the I/O Board receives a command for the 1350A to draw a character, a flag is placed in memory. When this flag is output by the memory, the Character Generator (schematic 5) takes over command of the Vector Generator. All vectors necessary to produce the character are generated by a Read Only Memory (ROM) on the Character Generator Board. This conserves space in the main memory.

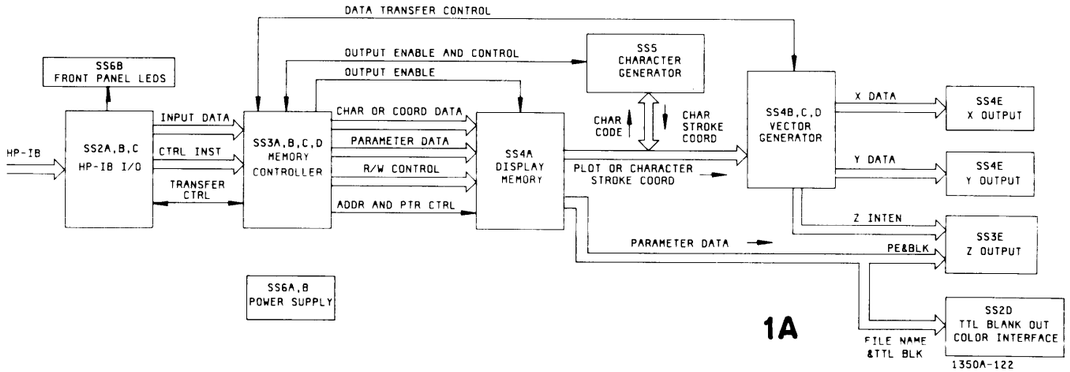
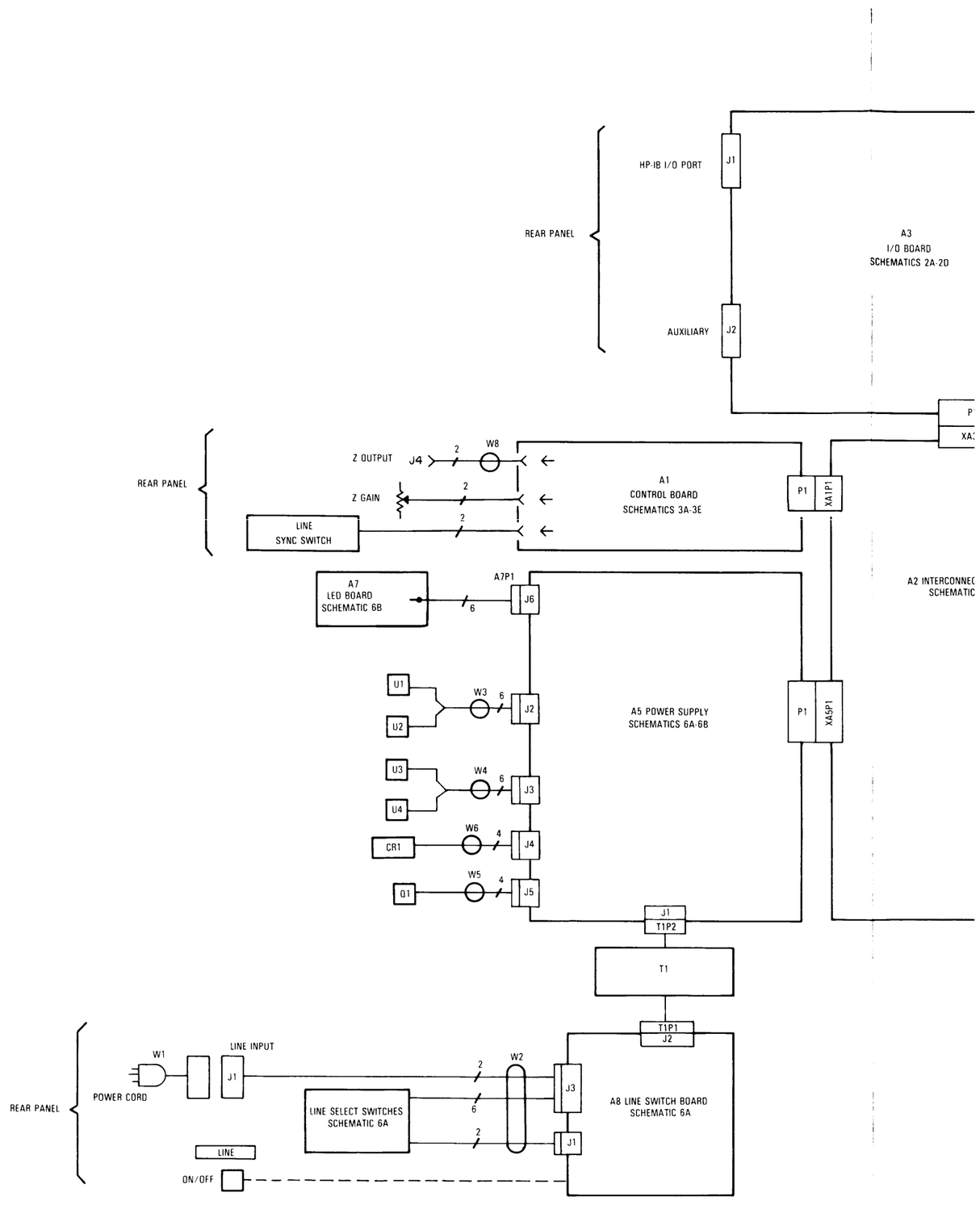


Figure 8-5. 1350A Simplified Block Diagram



"conversation"
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as each location
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RT.

commands from
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memory. When
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conserves space

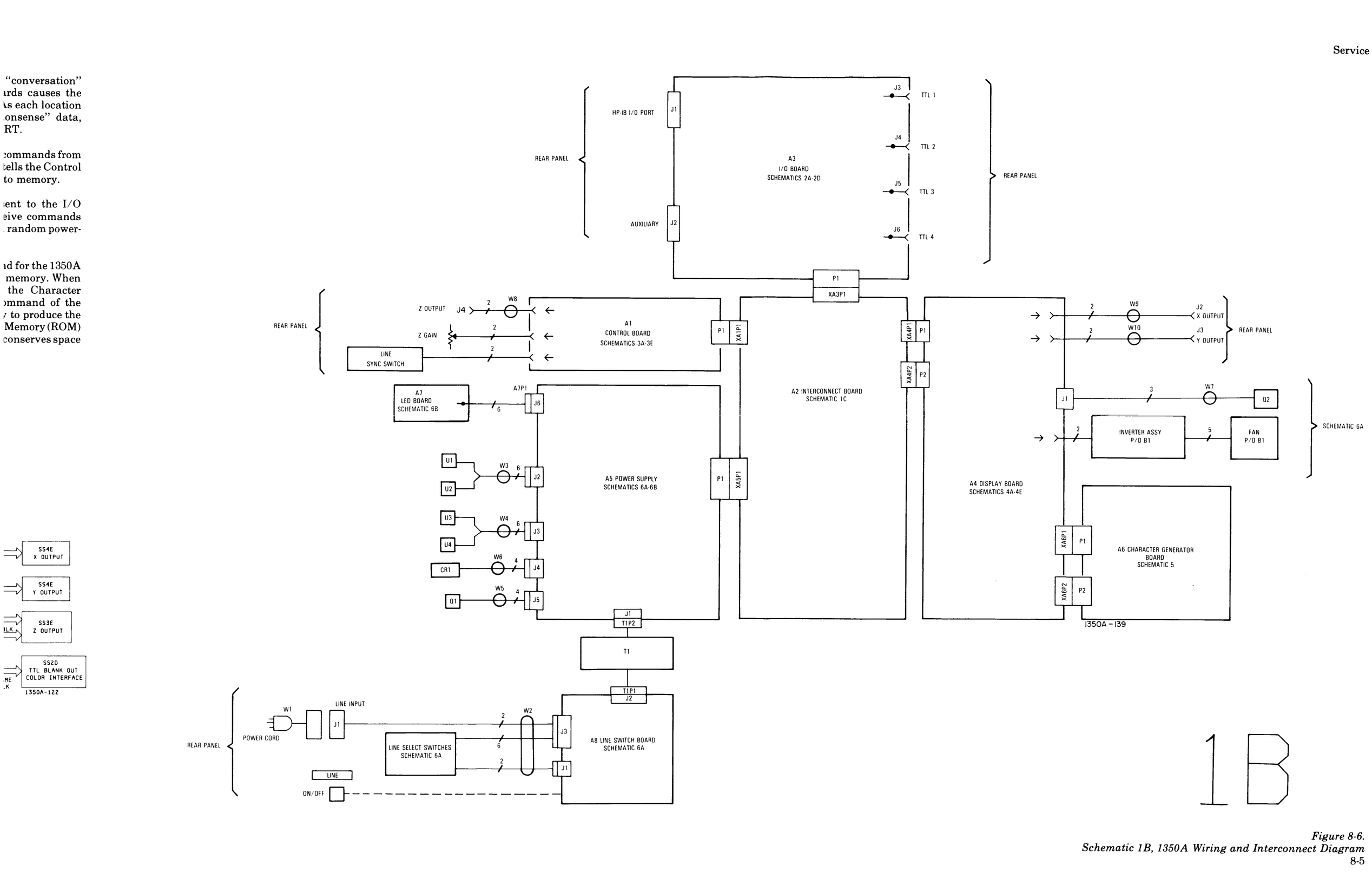


Figure 8-6.
Schematic 1B, 1350A Wiring and Interconnect Diagram

PIN CONNECTION TABLE XA1P1 (CONTROL BOARD)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	+15V	*	*
2	−15V	*	*
3	N=LOAD ADDR CTR	XA1P1-3	XA4P1-61
4	−5V	*	*
5	N=STORE POINTER ADDR	XA1P1-5	XA4P1-67
6	N=MEMORY CLK	XA1P1-6	XA4P1-57
7	P=FIND FILE	XA1P1-7	XA4P1-53
8	L=MEM CHIP ENABLE	XA1P1-8	XA4P1-55
9	L=CHAR	XA6P1-5	XA1P1-9; XA3P1-100
10	+5 V	*	*
11	24.6 MHz	XA4P2-71	XA1P1-11; XA3P1-50
12	+5 V	*	*
13	L=DO WRITE	XA3P1-48	XA1P1-13
14	L=WRITING	XA1P1-14	XA3P1-7
15	L=VECTOR BUSY	XA4P2-63	XA1P1-15; XA3P1-45
16	GND	*	*
17	D-13	XA1P1-17	XA4P1-49
18	NOT USED		XA3P1-47; XA1P1-18
19	P=CHAR LATCH X	XA4P2-23	XA1P1-19
20	L=INTERFACE HOLDOFF	XA3P1-85	XA1P1-20; XA4P2-33
21	P=CHAR LATCH Y	XA4P2-25	XA4P2-21
22	P=LATCH X	XA1P1-24	XA4P2-15
23	L=LOAD ADDR	XA1P1-23	XA4P1-73
24	P=LATCH Y	XA1P1-22	XA4P2-17
25	L=CHAR HOLDOFF	XA4P2-19	XA1P1-25
26	P=X ADDR	XA1P1-26	XA3P1-86; XA4P2-35
27	POINTER SEL 2	XA1P1-27	XA4P1-63
28	NC		
29	POINTER SEL 1	XA1P1-29	XA4P1-65
30	P=Y ADDR	XA1P1-30	XA3P1-80; XA4P2-21
31	N=CHANGE DATA	XA1P1-31	XA3P1-44
32	NOT USED		XA1P1-32; XA3P1-56
33	L=MEMORY OUTPUT ENABLE	XA1P1-33	XA4P1-40
34	L=VECTOR INHIBIT	XA1P1-34	XA4P2-43
35	L=CHAR OUTPUT ENABLE	XA1P1-35	XA4P2-27
36	L=CONTROL BUSY	XA1P1-36	XA3P1-42
37	NOT USED		XA1P1-37; XA3P1-82; XA4P1-75
38	I2	XA3P1-6	XA1P1-38
39	H=FILE FOUND	XA4P1-51	XA1P1-39
40	I1	XA3P1-8	XA1P1-40
41	N=CONTROL GET BUSY	XA3P1-49	XA1P1-41
42	L=BLANK VECTOR	XA1P1-42	XA4P2-41
43	L=RESET	XA3P1-52	XA1P1-43
44	I4	XA3P1-14	XA1P1-44
45	A0	XA4P1-6	XA1P1-45; XA3P1-46; XA3P1-93
46	I3	XA3P1-10	XA1P1-46
47	PE BIT	XA3P1-33	XA1P1-47
48	N=LATCH INST	XA3P1-5	XA1P1-48
49	D12	XA1P1-49	XA4P1-47
50	I5	XA3P1-12	XA1P1-50
51	D11	XA1P1-51	XA4P1-45
52	ID12	XA3P1-20	XA1P1-52
53	D8	XA1P1-53	XA4P1-39
54	ID11	XA3P1-18	XA1P1-54
55	D9	XA1P1-55	XA4P1-41
56	ID10	XA3P1-27	XA1P1-56
57	D10	XA1P1-57	XA4P1-43
58	ID9	XA3P1-25	XA1P1-58
59	D7	XA1P1-59	XA4P1-37
60	ID8	XA3P1-21	XA1P1-60
61	D6	XA1P1-61	XA4P1-35
62	ID7	XA3P1-23	XA1P1-62
63	D5	XA1P1-63	XA4P1-33
64	ID6	XA3P1-19	XA1P1-64

PIN CONNECTION TABLE XA1P1 (CONTROL BOARD) (Cont'd)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
65	D4	XA1P1-65	XA4P1-31
66	ID5	XA3P1-17	XA1P1-66
67	D3	XA1P1-67	XA4P1-29
68	ID4	XA3P1-31	XA1P1-68
69	D2	XA1P1-69	XA4P1-27
70	ID3	XA3P1-24	XA1P1-70
71	D1	XA1P1-71	XA4P1-25
72	ID2	XA3P1-22	XA1P1-72
73	NOT USED		XA1P1-73; XA3P1-59
74	ID1	XA3P1-29	XA1P1-74
75	N=CLR ADDR	XA1P1-75	XA4P1-59
76	ID13	XA3P1-9	XA1P1-76
77	LINE SYNC	XA5P1-F	XA1P1-77
78	NOT USED		XA1P1-78; XA3P1-16
79	PARA BIT 2	XA1P1-79	XA4P1-15
80	PARA BIT 1	XA1P1-80	XA4P1-13
81	PARA BIT 4	XA1P1-81	XA4P1-19
82	PARA BIT 3	XA1P1-82	XA4P1-17
83	PARA BIT 6	XA1P1-83	XA4P1-23
84	PARA BIT 5	XA1P1-84	XA4P1-21
85	L=CTRL INST	XA3P1-54	XA1P1-85
86	L=WRITE DATA	XA1P1-86	XA4P1-26
87	L=WRITE PB0	XA1P1-87	XA4P1-24
88	L=WRITE PB5	XA1P1-88	XA4P1-22
89	L=WRITE PB4	XA1P1-89	XA4P1-20
90	L=WRITE PB3	XA1P1-90	XA4P1-18
91	L=WRITE PB2	XA1P1-91	XA4P1-16
92	L=WRITE PB1	XA1P1-92	XA4P1-14
93	PBO-1	XA4P1-28	XA1P1-93; XA3P1-77
94	PBO-2	XA4P1-30	XA1P1-94; XA3P1-79
95	Z0	XA4P2-5	XA1P1-95
96	L=BLANK CHAR	XA4P2-29	XA1P1-96
97	Z2	XA4P2-9	XA1P1-97
98	Z1	XA4P2-7	XA1P1-98
99	Z4	XA4P2-13	XA1P1-99
100	Z3	XA4P2-11	XA1P1-100

*See Pin Connection Table XA5P1 (Power Supply) for Origins and Connections on Supply Voltage and GND.

PIN CONNECTION TABLE XA3P1 (I/O BOARD)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	GND	*	*
2	+5 V	*	*
3	GND	*	*
4	+5 V	*	*
5	N=LATCH INST	XA3P1-5	XA3P1-48
6	I2	XA3P1-6	XA3P1-38
7	L=WRITING	XA3P1-14	XA3P1-7
8	I1	XA3P1-8	XA1P1-40
9	ID13	XA3P1-9	XA1P1-76
10	I3	XA3P1-10	XA1P1-46
11	NC		
12	I5	XA3P1-12	XA1P1-50
13	NC		
14	I4	XABP1-14	XA1P1-44
15	NC		
16	NOT USED		XA1P1-78; XA3P1-16
17	ID5	XA3P1-17	XA1P1-66
18	ID11	XA3P1-18	XA1P1-54
19	ID6	XA3P1-19	XA1P1-64
20	ID12	XA3P1-20	XA1P1-52
21	ID8	XA3P1-21	XA1P1-60
22	ID2	XA3P1-22	XA1P1-72
23	ID7	XA3P1-23	XA1P1-62
24	ID3	XA3P1-24	XA1P1-70
25	ID9	XA3P1-25	XA1P1-58

PIN CONNECTION TABLE XA3P1 (I/O BOARD) (Cont'd)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
26	NC		
27	ID10	XA3P1-27	XA1P1-56
28	NC		
29	ID1	XA3P1-29	XA1P1-74
30	NC		
31	ID4	XA3P1-31	XA1P1-68
32	NC		
33	PE BIT	XA3P1-33	XA1P1-47
34	NC		
41			
42	L=CONTROL BUSY	XA1P1-36	XA3P1-42
43	NC		
44	N=CHANGE DATA	XA1P1-31	XA3P1-44
45	L=VECT BUSY	XA4P2-69	XA1P1-15 XA1P1-45
46	A0	XA4P1-6	XA1P1-45; XA3P1-46; XA3P1-93
47	NOT USED		XA3P1-47; XA1P1-18
48	L=DO WRITE	XA3P1-48	XA1P1-13
49	N=CONTROL GET BUSY	XA3P1-49	XA1P1-41
50	24.6 MHz	XA4P2-71	XA3P1-50; XA1P1-11
51	L=PROGL	XA3P1-51	XA5P1-C
52	L=RESET	XA3P1-52	XA1P1-43
53	L=DATAL	XA3P1-53	XA5P1-B
54	L=CTRL INST	XA3P1-54	XA1P1-85
55	NOT USED		XA5P1-D; XA3P1-55
56	NOT USED		XA1P1-32; XA3P1-56
57	L=POWER INTERRUPT	XA3P1-57	XA5P1
58	+12 V	*	*
59	NOT USED		XA1P1-73; XA3P1-59
60	+15 V	*	*
61	NOT USED		XA3P1-61; XA4P1-58
70			XA3P1-62; XA4P1-60 XA3P1-63; XA4P1-54 XA3P1-64; XA4P1-56 XA3P1-65; XA4P1-50 XA3P1-66; XA4P1-48 XA3P1-67; XA4P1-42 XA3P1-68; XA4P1-46 XA3P1-69; XA4P1-52 XA3P1-70; XA4P1-44
71	PBO5	XA4P1-36	XA3P1-71
72	PBO6	XA4P1-38	XA3P1-72
73	PBO4	XA4P1-34	XA3P1-73
74	−5 V	*	*
75	PBO3	XA4P1-32	XA3P1-75
76	−15 V	*	*
77	PBO1	XA4P1-28	XA1P1-93; XA3P1-77
78	NC		
79	PBO2	XA4P1-30	XA1P1-94; XA3P1-79
80	P=YADDR	XA1P1-30	XA3P1-80; XA4P2-21

PIN CONNECTION TABLE XA3P1 (I/O BOARD) (Cont'd)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
81	NOT USED		XA3P1-81; XA4P2-20 XA3P1-82; XA4P1-75; XA1P1-37 XA3P1-83 XA3P1-84
84			
85	L=INTERFACE HOLDOFF	XA3P1-85	XA1P1-20; XA4P2-33
86	P=XADDR	XA1P1-26	XA3P1-86; XA4P2-35
87	NOT USED		XA3P1-87; XA4P1-12 XA3P1-88; XA4P1-11 XA3P1-89; XA4P1-10 XA3P1-90; XA4P1-9 XA3P1-91; XA4P1-8 XA3P1-92; XA4P1-7
92			
93	A0	XA4P1-6	XA1P1-45; XA3P1-46; XA3P1-93
94	NOT USED		XA3P1-94; XA4P1-5 XA3P1-95; XA4P1-4 XA3P1-96; XA4P1-3 XA3P1-97; XA4P1-1
97			
98	NC		
99	NOT USED		XA3P1-99; XA4P1-2
100	NOT USED		XA3P1-100; XA1P1-9; XA6P1-5

*See Pin Connection Table XA5P1 (Power Supply) for Origins and Connections on Supply Voltage and GND.

PIN CONNECTION TABLE XA4P1 (DISPLAY BOARD)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	NOT USED		XA3P1-97; XA4P1-1 XA3P1-99; XA4P1-2 XA3P1-96; XA4P1-3 XA3P1-95; XA4P1-4 XA3P1-94; XA4P1-5
5			
6	A0	XA4P1-6	XA1P1-45; XA3P1-93
7	NOT USED		XA3P1-92; XA4P1-7 XA3P1-91; XA4P1-8 XA3P1-90; XA4P1-9 XA3P1-89; XA4P1-10 XA3P1-88; XA4P1-11
11			

PIN CONNECTIO

PIN	SIG
12	NOT USED
13	PARA BIT 1
14	L=WRITE DATA
15	PARA BIT 2
16	L=WRITE DATA
17	PARA BIT 3
18	L=WRITE DATA
19	PARA BIT 4
20	L=WRITE DATA
21	PARA BIT 5
22	L=WRITE DATA
23	PARA BIT 6
24	L=WRITE DATA
25	D1
26	L=WRITE DATA
27	D2
28	PB01
29	D3
30	PB02
31	D4
32	PB03
33	D5
34	PB04
35	D6
36	PB05
37	D7
38	PB06
39	D8
40	L=MEMORY OU
41	D9
42	NOT USED
43	D10
44	NOT USED
45	D11
46	NOT USED
47	D12
48	NOT USED
49	D13
50	NOT USED
51	H=FILE FOUNI
52	NOT USED
53	P=FIND FILE
54	NOT USED
55	L=MEMORY C
56	NOT USED
57	N=MEMORY C
58	NOT USED
59	N=CLR ADDR
60	NOT USED
61	N=LOAD ADD
62	NC
63	POINTER SEL
64	−5 V
65	POINTER SEL
66	+12 V
67	N=STORE PO
68	+12 V
69	NC
70	+5 V

Cont'd)	
NNECTS TO	
A4P1-31	
A1P1-66	
A4P1-29	
A1P1-68	
A4P1-27	
A1P1-70	
A4P1-25	
A1P1-72	
A1P1-73;	
XA3P1-59	
A1P1-74	
A4P1-59	
A1P1-76	
A1P1-77	
A1P1-78;	
XA3P1-16	
A4P1-15	
A4P1-13	
A4P1-19	
A4P1-17	
A4P1-23	
A4P1-21	
A1P1-85	
A4P1-26	
A4P1-24	
A4P1-22	
A4P1-20	
A4P1-18	
A4P1-16	
A4P1-14	
A1P1-93;	
XA3P1-77	
A1P1-94;	
XA3P1-79	
A1P1-95	
A1P1-96	
A1P1-97	
A1P1-98	
A1P1-99	
A1P1-100	
Connections	
NNECTS TO	
•	
•	
•	
•	
A3P1-48	
A3P1-38	
A3P1-7	
A1P1-40	
A1P1-76	
A1P1-46	
A1P1-50	
A1P1-44	
A1P1-78;	
XA3P1-16	
A1P1-66	
A1P1-54	
A1P1-64	
A1P1-52	
A1P1-60	
A1P1-72	
A1P1-62	
A1P1-70	
A1P1-58	

PIN CONNECTION TABLE XA3P1 (I/O BOARD) (Cont'd)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
26	NC		
27	ID10	XA3P1-27	XA1P1-56
28	NC		
29	ID1	XA3P1-29	XA1P1-74
30	NC		
31	ID4	XA3P1-31	XA1P1-68
32	NC		
33	PE BIT	XA3P1-33	XA1P1-47
34	NC		
↓			
41			
42	L=CONTROL BUSY	XA1P1-36	XA3P1-42
43	NC		
44	N=CHANGE DATA	XA1P1-31	XA3P1-44
45	L=VECT BUSY	XA4P2-69	XA1P1-15 XA1P1-45
46	A0	XA4P1-6	XA1P1-45; XA3P1-46; XA3P1-93
47	NOT USED		XA3P1-47; XA1P1-18
48	L=DO WRITE	XA3P1-48	XA1P1-13
49	N=CONTROL GET BUSY	XA3P1-49	XA1P1-41
50	24.6 MHz	XA4P2-71	XA3P1-50; XA1P1-11
51	L=PROGL	XA3P1-51	XA5P1-C
52	L=RESET	XA3P1-52	XA1P1-43
53	L=DATAL	XA3P1-53	XA5P1-B
54	L=CTRL INST	XA3P1-54	XA1P1-85
55	NOT USED		XA5P1-D; XA3P1-55
56	NOT USED		XA1P1-32; XA3P1-56
57	L=POWER INTERRUPT	XA3P1-57	XA5P1 •
58	+12 V	•	
59	NOT USED		XA1P1-73; XA3P1-59
60	+15 V	•	•
61	NOT USED		XA3P1-61; XA4P1-58
↓			XA3P1-62; XA4P1-60
			XA3P1-63; XA4P1-54
			XA3P1-64; XA4P1-56
			XA3P1-65; XA4P1-50
			XA3P1-66; XA4P1-48
			XA3P1-67; XA4P1-42
			XA3P1-68; XA4P1-46
			XA3P1-69; XA4P1-52
70			XA3P1-70; XA4P1-44
71	PBO5	XA4P1-36	XA3P1-71
72	PBO6	XA4P1-38	XA3P1-72
73	PBO4	XA4P1-34	XA3P1-73
74	–5 V	•	•
75	PBO3	XA4P1-32	XA3P1-75
76	–15 V	•	•
77	PBO1	XA4P1-28	XA1P1-93; XA3P1-77
78	NC		
79	PBO2	XA4P1-30	XA1P1-94; XA3P1-79
80	P=YADDR	XA1P1-30	XA3P1-80; XA4P2-21

PIN CONNECTION TABLE XA3P1 (I/O BOARD) (Cont'd)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
81	NOT USED		XA3P1-81; XA4P2-20
↓			XA3P1-82; XA4P1-75; XA1P1-37
			XA3P1-83
84			XA3P1-84
85	L=INTERFACE HOLDOFF	XA3P1-85	XA1P1-20; XA4P2-33
86	P=XADDR	XA1P1-26	XA3P1-86; XA4P2-35
87	NOT USED		XA3P1-87; XA4P1-12
↓			XA3P1-88; XA4P1-11
			XA3P1-89; XA4P1-10
			XA3P1-90; XA4P1-9
			XA3P1-91; XA4P1-8
92			XA3P1-92; XA4P1-7
93	A0	XA4P1-6	XA1P1-45; XA3P1-46; XA3P1-93
94	NOT USED		XA3P1-94; XA4P1-5
↓			XA3P1-95; XA4P1-4
			XA3P1-96; XA4P1-3
97			XA3P1-97; XA4P1-1
98	NC		
99	NOT USED		XA3P1-99; XA4P1-2
100	NOT USED		XA3P1-100; XA1P1-9; XA6P1-5

*See Pin Connection Table XA5P1 (Power Supply) for Origins and Connections on Supply Voltage and GND.

PIN CONNECTION TABLE XA4P1 (DISPLAY BOARD)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	NOT USED		XA3P1-97; XA4P1-1
↓			XA3P1-99; XA4P1-2
			XA3P1-96; XA4P1-3
			XA3P1-95; XA4P1-4
5			XA3P1-94; XA4P1-5
6	A0	XA4P1-6	XA1P1-45; XA3P1-93
7	NOT USED		XA3P1-92; XA4P1-7
↓			XA3P1-91; XA4P1-8
			XA3P1-90; XA4P1-9
			XA3P1-89; XA4P1-10
11			XA3P1-88; XA4P1-11

PIN CONNECTION TABLE XA4P1 (DISPLAY BOARD) (Cont'd)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
12	NOT USED		XA3P1-87; XA4P1-12
13	PARA BIT 1	XA1P1-80	XA4P1-13
14	L=WRITE DATA PB1	XA1P1-92	XA4P1-14
15	PARA BIT 2	XA1P1-79	XA4P1-15
16	L=WRITE DATA PB2	XA1P1-91	XA4P1-16
17	PARA BIT 3	XA1P1-82	XA4P1-17
18	L=WRITE DATA PB3	XA1P1-90	XA4P1-18
19	PARA BIT 4	XA1P1-81	XA4P1-19
20	L=WRITE DATA PB4	XA1P1-89	XA4P1-20
21	PARA BIT 5	XA1P1-84	XA4P1-21
22	L=WRITE DATA PB5	XA1P1-88	XA4P1-22
23	PARA BIT 6	XA1P1-83	XA4P1-23
24	L=WRITE DATA PB0	XA1P1-87	XA4P1-24
25	D1	XA1P1-71	XA4P1-25
26	L=WRITE DATA	XA1P1-86	XA4P1-26
27	D2	XA1P1-69	XA4P1-27
28	PB01	XA4P1-28	XA1P1-93; XA3P1-77
29	D3	XA1P1-67	XA4P1-29
30	PB02	XA4P1-30	XA1P1-94; XA3P1-79
31	D4	XA1P1-65	XA4P1-31
32	PB03	XA4P1-32	XA4P1-32
33	D5	XA1P1-63	XA4P1-33
34	PB04	XA4P1-34	XA4P1-34
35	D6	XA1P1-61	XA4P1-35
36	PB05	XA4P1-36	XA4P1-36
37	D7	XA1P1-59	XA4P1-37
38	PB06	XA4P1-38	XA4P1-38
39	D8	XA1P1-53	XA4P1-39
40	L=MEMORY OUTPUT ENABLE	XA1P1-33	XA4P1-40
41	D9	XA1P1-55	XA4P1-41
42	NOT USED		XA3P1-67; XA4P1-42
43	D10	XA1P1-57	XA4P1-43
44	NOT USED		XA3P1-70; XA4P1-44
45	D11	XA1P1-51	XA4P1-45
46	NOT USED		XA3P1-68; XA4P1-46
47	D12	XA1P1-49	XA4P1-47
48	NOT USED		XA3P1-66; XA4P1-48
49	D13	XA1P1-17	XA4P1-49
50	NOT USED		XA3P1-65; XA4P1-50
51	H=FILE FOUND	XA4P1-51	XA1P1-39
52	NOT USED		XA3P1-69; XA4P1-52
53	P=FIND FILE	XA1P1-7	XA4P1-53
54	NOT USED		XA3P1-63; XA4P1-54
55	L=MEMORY CHIP ENABLE	XA1P1-8	XA4P1-55
56	NOT USED		XA3P1-64; XA4P1-56
57	N=MEMORY CLK	XA1P1-6	XA4P1-57
58	NOT USED		XA3P1-61; XA3P1-58
59	N=CLR ADDR	XA1P1-75	XA4P1-59
60	NOT USED		XA3P1-62; XA4P1-60
61	N=LOAD ADDR CTR	XA1P1-3	XA4P1-61
62	NC		
63	POINTER SEL 2	XA1P1-27 •	XA4P1-63 •
64	–5 V		
65	POINTER SEL 1	XA1P1-29 •	XA4P1-65 •
66	+12 V		
67	N=STORE POINTER ADDR	XA1P1-5 •	XA4P1-67 •
68	+12 V		
69	NC		
70	+5 V	•	•

PIN CONNECTION TABLE XA4P1 (DISPLAY BOARD) (Cont'd)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
71	NOT USED		XA3P1-84; XA4P1-71
72	+5 V	•	•
73	L=LOAD ADDRESS	XA1P1-23	XA4P1-73
74	GND	•	•
75	NOT USED		XA1P1-37; XA3P1-82; XA4P1-75
76	GND	•	•
77	GND	•	•
78	GND	•	•
79	+5 V	•	•
80	+5 V	•	•

*See Pin Connection Table XA5P1 (Power Supply) for Origins and Connections on Supply Voltage and GND.

PIN CONNECTION TABLE XA4P2 (DISPLAY BOARD)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	+5 V	•	•
2	+5 V	•	•
3	GND	•	•
4	GND	•	•
5	Z0	XA4P2-5	XA1P1-95
6	GND	•	•
7	Z1	XA4P2-7	XA1P1-98
8	GND	•	•
9	Z2	XA4P2-9	XA1P1-97
10	+5 V	•	•
11	Z3	XA4P2-11	XA1P1-100
12	NC		
13	Z4	XA4P2-13	XA1P1-99
14	+12 V	•	•
15	P=LATCH Y	XA1P1-24	XA4P2-15
16	+12 V	•	•
17	P=LATCH X	XA1P1-22	XA4P2-17
18	NC		
19	L=CHAR HOLDOFF	XA4P2-19	XA1P1-25
20	NOT USED		XA3P1-81; XA4P2-20
21	P=Y ADDR	XA1P1-30	XA3P1-80; XA4P2-21
22	NOT USED		XA3P1-83; XA4P2-22
23	P=CHAR LATCH X	XA4P2-23	XA1P1-19
24	NC		
25	P=CHAR LATCH Y	XA4P2-25	XA1P1-21
26	NC		
27	L=CHAR OUTPUT ENABLE	XA1P1-35	XA4P2-27
28	NC		
29	L=BLANK CHAR	XA4P2-29	XA1P1-96
30	–15 V	•	•
31	L=CHAR	XA6P1-5	XA1P1-9; XA3P1-100
32	+15 V	•	•
33	L=INTERFACE HOLDOFF	XA3P1-85	XA1P1-20; XA4P2-33
34	NC		
35	P=X ADDR	XA1P1-26	XA3P1-86; XA4P2-35
36	NC		
↓			
40			

Figure 8-7. Schematic 1C, Interface Board A2 Schematic (Sheet 1 of 2)

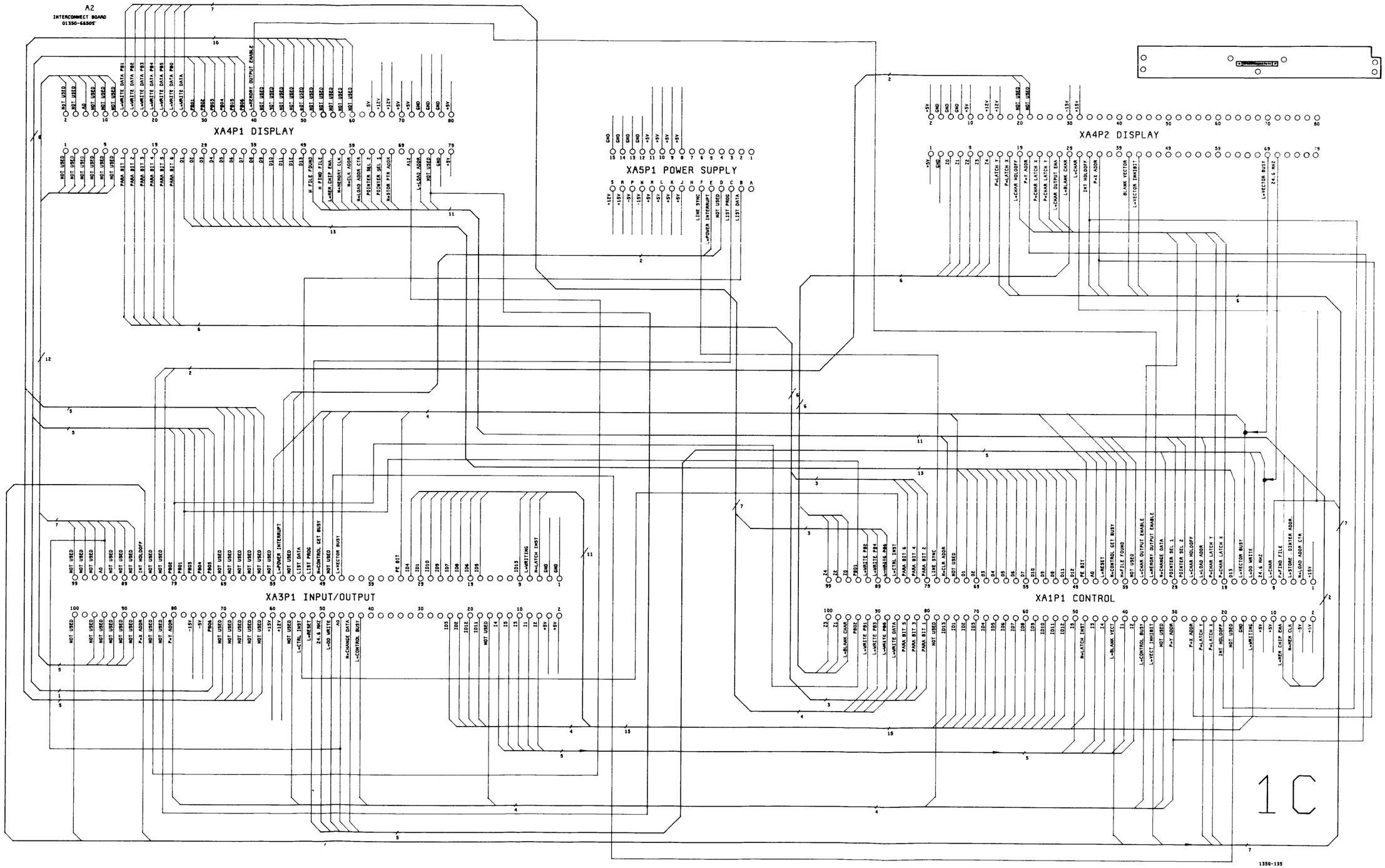


Figure 8-7.
Schematic 1C, Interface Board A2 Schematic (Sheet 2 of 2)

8-24. HP-IB INPUT/OUTPUT ASSEMBLY A3 (SERVICE SHEET 2).

8-25. INPUT/OUTPUT (I/O) BOARD TROUBLESHOOTING (Using an HP9825A Calculator).

1. "LISTEN PROGRAM" check. This check shows that the I/O Board will recognize its HP-IB listen address and automatically go to "listen for program" mode.

a. Cycle 1350A LINE power switch.
b. Make 9825A entry:

[RESET] wrt 718 [EXECUTE]

c. Verify that PROGRAM LED is on: DATA LED is off. U17B pin 9 on Schematic 2A = high. U1A pin 6 (Schematic 2B) = high. If this does not work, check Ready Latch U43, Handshake circuits, Bus Receivers, and Listen Latch U17B.

NOTE

[RESET] key (or a cli 7 command) causes HP-IB IFC line to be set low momentarily.

2. Unlisten check. This check shows that the I/O Board will recognize an HP-IB Unlisten command. Unlisten is an ASCII ? sent while ATN = low. (ASCII "?" = 63 in base 10.)

a. Make 9825A entry:

cmd 7,"?" [EXECUTE]

b. Verify that PROGRAM and DATA LEDs are both off. U13 Schematic 2A detects Unlisten.

3. "LISTEN DATA" check. This shows that the I/O Board will automatically go to "listen for data" after it has received two "program" bytes from HP-IB.

a. Make 9825A entry:

[RESET] wtb718,"PA" [EXECUTE]

b. Verify that DATA LED is on: PROGRAM LED is off. U17B pin 9 (Schematic 2A) = high. U1A pin 5 (Schematic 2B) = high.

NOTE

A 9825A "wtb" statement does not generate a CR LF (Carriage Return;Line Feed) when quotes are closed.

4. Return to "listen for program" check. This shows that the I/O Board will return to "listen for program" from "listen for data" when a command-terminating ":" (colon) is received from HP-IB.

a. Make 9825A entry:

wrt 718,":" [EXECUTE]

b. Verify that DATA LED is now off: PROGRAM LED is now on. U19B (Schematic 2B) causes "return to listen for program" when a ":" (or CR or LF) is received from HP-IB.

5. Clear POWER INTERRUPT LED check. This shows that the I/O Board will recognize an ASCII DC4 character (20 in base 10) in order to clear its POWER INTERRUPT LED.

a. Make 9825A entry:

wtb 718,20,13,10 [EXECUTE]

b. Verify that POWER INTERRUPT LED is now off. PROGRAM LED will be on. U68A pin 5 (Schematic 2D) = low.

NOTE

13 = CR (Carriage Return); 10 = LF (Line Feed).

6. Pen Enable (PE) check. This shows that the I/O Board will recognize its PE command and parameter.

a. Make 9825A entry:

wrt 718,"PE0," [EXECUTE]

b. Verify that U35 pin 5 (Schematic 2B) is low.

c. Make 9825A entry:

wrt 718,"PE1," [EXECUTE]

d. Verify that U35 pin 5 is high.

7. Character Size (CS) check. This shows that the I/O Board will recognize its CS command and parameter.

a. Make 9825A entry:

wrt 718,"CS0," [EXECUTE]

b. Verify that U55 pins 2, 5, and 7 (Schematic 2C) are all low.

c. Make 9825A entry:

wrt 718,"CS7," [EXECUTE]

d. Verify that U55 pins 2, 5, and 7 are all high. (Note: This also partly checks the BCD-to-Binary Converter circuits.)

PIN CONNECTION TABLE XA4P2 (DISPLAY BOARD) (Cont'd)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
41	L=BLANK VECTOR	XA1P1-42	XA4P2-41
42	NC		
43	L=VECTOR INHIBIT	XA1P1-34	XA4P2-43
44	NC		
↓			
68			
69	L=VECTOR BUSY	XA4P2-63	XA1P1-15; XA3P1-45
70	NC		
71	24.6 MHz	XA4P2-71	XA1P1-11; XA3P1-50
72	NC		
↓			
80			

*See Pin Connection Table XA5P1 (Power Supply) for Origins and Connections on Supply Voltage and GND.

PIN CONNECTION TABLE XA5P1 (POWER SUPPLY BOARD)

PIN	SIGNAL	ORIGIN PIN	CONNECTS TO
1	GND	XA5P1-1 thru 4, 12 thru 15	XA1P1-16; XA3P1-1, 3; XA4P1-74 thru 76,78; XA4P2-3, 4, 6
2	GND	Same as Pin 1	Same as Pin 1
3	GND	Same as Pin 1	Same as Pin 1
4	GND	Same as Pin 1	Same as Pin 1
5	NC		
6	NC		
7	NC		
8	+5 V	XA1P1-J,K,L,M, 8 thru 11	XA1P1-10,12; XA3P1-2, 4; XA4P1-70,72,79,80; XA4P2-1, 2, 10
9	+5 V	Same as Pin 8	Same as Pin 8
10	+5 V	Same as Pin 8	Same as Pin 8
11	+5 V	Same as Pin 8	Same as Pin 8
12	GND	Same as Pin 1	Same as PiN 1
13	GND	Same as Pin 1	Same as Pin 1
14	GND	Same as Pin 1	Same as Pin 1
15	GND	Same as PIn 1	Same as Pin 1
A	NC		
B	L=DATAL	XA3P1-53	XA5P1-B
C	L=PROGL	XA3P1-51	XA5P1-C
D	NOT USED		XA5P1-D; XA3P1-55
E	L=POWER INTERRUPT	XA3P1-57	XA5P1-E
F	LINE SYNC	XA5P1-F	XA1P1-77
H	NC		
J	+5 V	Same as Pin 8	Same as Pin 8
K	+5 V	Same as Pin 8	Same as Pin 8
L	+5 V	Same as Pin 8	Same as Pin 8
M	+5 V	Same as Pin 8	Same as Pin 8
N	−15 V	XA5P1-N	XA1P1-2; XA3P1-76; XA4P2-30
P	−5 V	XA5P1-P	XA1P1-4; XA3P1-74; XA1P1-4
R	+15 V	XA5P1-R	XA1P1-1; XA3P1-60; XA4P2-32
S	+12 V	XA5P1-S	XA3P1-58; XA4P1-66; XA4P2-14, 16

8. BCD-to-Binary Converter check. This shows that the I/O Board will convert ASCII digits from BCD to binary.

a. Make 9825A entry:

wtb 718,"FL0000," [EXECUTE]

b. Verify that pins 4, 7, 9, and 12 of U59, U60, and U61 are all low. (ID1-12 on Schematic 2C = low)

c. Make 9825A entry:

wtb 718,"FL2047," [EXECUTE]

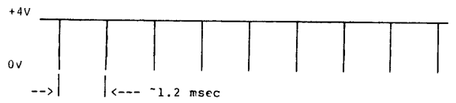
d. Verify that ID1 - ID11 = high; ID12 =low (U59, U60, U61).

9. Plot Absolute DO WRITE check. This shows that the I/O Board will generate the DO WRITE signal from its PA command.

a. Make 9825A entry:

[RESET] wrt 718,"PA;";jmp 0 [EXECUTE]

b. Verify low-going pulses at U35B pin 8 (Schematic 2B) as shown below.



c. Press 9825A [STOP] key. Ignore "error G8" if displayed.

10. Text DO WRITE check. This shows that the I/O Board will generate the DO WRITE signal from its TX command.

a. Make 9825A entry:

[RESET] wrt 718,"TX";jmp 0 [EXECUTE]

b. Verify low-going pulses at U35B pin 8 as shown in step 9b.

c. Press 9825A [STOP] key. Ignore "error G8" if displayed.

11. CHANGE DATA check. This shows that the I/O Board will respond properly to a CHANGE DATA signal from the Control Board.

a. Make 9825A entry:

[RESET] wtb 718,"PA0," [EXECUTE]

b. Verify that ID1 - ID12 = low (U59, U60, U61 on Schematic 2C).

c. Make 9825A entry:

wtb 718,"PA0,1023;" [EXECUTE]

d. Verify that ID1 - ID10 = high; ID11 and ID12 = low.

12. CONTROL INSTRUCTION, LATCH INSTR, and CONTROL GET BUSY check. This shows that the I/O Board outputs the proper signals when a Control Board instruction is received from HP-IB.

a. Make 9825A entry:

[RESET] wrt 718,"EM";jmp 0 [EXECUTE]

b. Set oscilloscope to 2 msec/div sweep speed. On Schematic 2A, verify low-going pulses (narrow) on U19C pin 8 and U58C pin 8. Check for high-going pulses on U28 pin 14.

c. Press 9825A [STOP] key. Ignore "error G8" if displayed.

13. TTL Blanking check. (Note: This check requires the Control and Display Boards to be working properly.) Checks that I/O Board will output TTL blanking in accordance with Write Auxiliary (WX) commands.

a. Make 9825A entry:

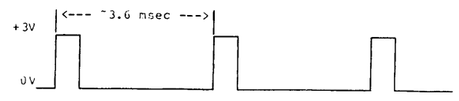
[RESET] wtb 718,3,20,13,10,
"EM::EN::EX::SN::SX::UM::" [EXECUTE]

b. Verify that rear-panel TTL1 - TTL4 outputs are all low.

c. Make 9825A entry:

wrt 718,"WX15,:PE1,:PA500,500;:SX" [EXECUTE]

d. Verify high-going pulses on TTL1 — TTL4 outputs as shown below.



14. TTL Blinking check. (TTL Blanking must be working properly.) Checks 4 Hz hardware blinking of TTL outputs.

a. Make 9825A entries:

[RESET] wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::
UM::" [EXECUTE]

wrt 718,"WX8,:PE1,:PA500,500;:SX" [EXECUTE]

b. Connect X-Y display TTL blank input to 1350A TTL1 output. Set Blinking Switch S2 section 1 to "on." Verify that CRT blinks.

c. Connect X-Y display TTL blank input to 1350A TTL2 output. Set Blinking Switch S2 section 2 to "on." Verify that CRT blinks.

d. Repeat above procedure for 1350A TTL3 output using section 3 of Blinking Switch S2.

15. Color Code Output check. (Note: This check requires the Control and Display Boards to be working properly.) Checks that I/O Board outputs correct color code according to file name of data.

a. Make 9825A entries:

[RESET] wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::
UM::" [EXECUTE]

wrt 718,"NF1,:PE1,:PA1000,1000;:SN" [EXECUTE]

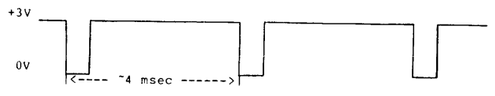
b. Verify that C1 (U75 pin 4) and C2 (U75 pin 10) on Schematic 2D are both high. This is the code for "green."

c. Make 9825A entries:

[RESET] wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::
UM::" [EXECUTE]

wrt 718,"NF16,:PE1,:PA1000,0;:SN" [EXECUTE]

d. Verify that C2 = high and C1 has waveform as shown below. This is the code for "yellow."



e. Make 9825A entries:

[RESET] wtb 718,3,20,13,10,"EM::EN::EX::SN::SX::
UM::" [EXECUTE]

wrt 718,"NF40,:PE1,:PA0,1000;:SN" [EXECUTE]

f. Verify that C1 = high and C2 has waveform as shown above. This is the code for "red."

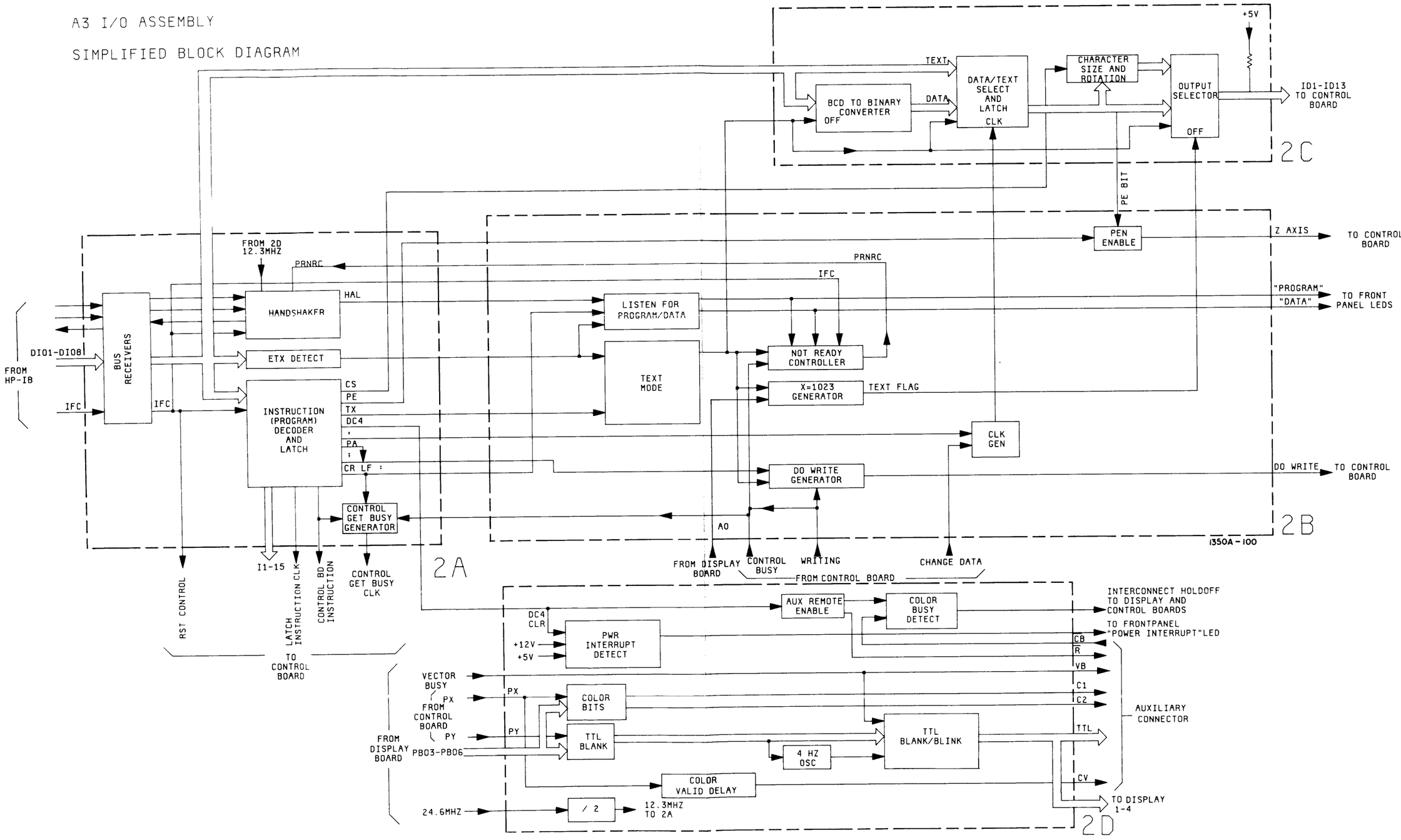


Figure 8-8. Input/Output Board A3 Block Diagram

8-26. GENERAL INFORMATION.

Input/Output Assembly A3 contains the input connector for information from HP-IB and output connectors for Display TTL blanking and Auxiliary control of a Tri-color display.

The Simplified Block Diagram (figure 8-8) for A3 shows major functional stages and their corresponding schematic locations (2A-2D). Detailed signal and stage descriptions are covered by the explanations of each of the four schematics.

Schematic 2A contains HP-IB interface circuits. Schematic 2B contains control and timing circuits. Schematic 2C contains BCD to Binary converter and data output circuits. Schematic 2D contains Auxiliary interface and Power Interrupt detection circuits.

8-27. OPERATING OVERVIEW.

After the 1350A has been addressed to listen by an HP-IB controller, it listens in one of two modes:

1) Program
2) Data.

In "listen for program" mode the 1350A receives two bytes from HP-IB that define the 1350A instruction. These two-letter instructions are the Graphics Translator Machine Language (GTML) mnemonics.

After two "program" bytes are received, the 1350A automatically goes to "listen for data" mode. The 1350A now receives parameter (or text) bytes until a ":" (colon), a CR (Carriage Return), or a LF (Line Feed) byte is received. The ":" (or CR or LF) causes the 1350A to return to "listen for program" mode.

NOTE

If text is being received, an ETX (End of Text) character must precede the ":" (or CR or LF).

"Program" Input Instruction Types.

All two-byte "program" instructions are one of two types: (1) an Input/Output Board instruction; or (2) a Control Board instruction.

The four Input/Output (I/O) Board instructions are:

1) Plot Absolute (PA)
2) Character Size (CS)
3) Text (TX)
4) Pen Enable (PE).

All other 1350A "program" instructions are Control Board instructions.

"Data" Types.
In "listen for data" mode, all bytes received are either parameter bytes or text bytes.

Parameter bytes are converted to binary values on the Input/Output Board. Text bytes are not converted.

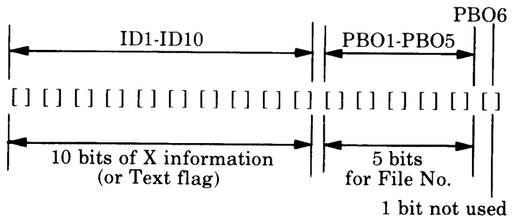
Data (parameter or text) is sent to the Control Board from the I/O Board via the ID1-ID13 lines.

ID1-ID13 Information Definition.
The ID13 line is reserved for future 1350A memory expansion and is not used at this time.

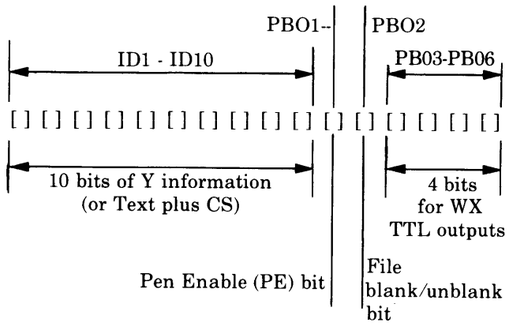
Information contained on ID1-ID12 is defined by: (a) type of instruction (I/O Board or Control Board); and (b) state of 1350A memory address line A0.

Three cases will be used to show ID1-ID12 information content for different instruction types. Each case is divided into two parts to show ID line definitions for A0 both low and high. The three cases are: (1) I/O Board instruction; (2) Control Board instruction other than Find Location (FL); and (3) Find Location Control Board instruction.

Figure 8-9 shows 1350A memory organization. Table 8-2 shows ID1-ID12 definitions for the three cases. These two things are necessary to understand the 1350A memory management scheme.



a) Memory byte definition when A0 = low.



b) Memory byte definition when A0 = high.

Figure 8-9. 1350A Memory Organization

The 1350A memory capacity is 2048 words of 32 bits. Each 32-bit word contains two 16-bit bytes. Byte content is defined by the state of memory address line A0.

CASE 1.

If an Input/Output Board instruction is detected, then ID1-ID10 are defined as follows.

a) When A0 = low:

1. If ID1-ID10 = 1023 (all high), then 1350A is in Text mode.

2. If ID1-ID10 < 1023, then 1350A is in Plot mode and ID1-ID10 is the binary X value.

b) When A0 = high:

1. If Text mode, then ID1-ID7 = ASCII character, ID8 and ID9 = character size (1,2,4,8), ID10 = rotate bit (low = 0; high = 90 degrees).

NOTE

A Character Size (CS) command must precede a Text (TX) command.

2. If Plot mode, then ID1-ID10 = binary Y value.

CASE 2.

If a Control Board instruction other than Find Location (FL) is detected, then ID1-ID6 become PBO1-PBO6 and are defined as follows.

a) When A0 = low:

PBO1-PBO5 = file name (binary).

PBO6 = don't care.

PBO1-PBO5 are for Erase File (EF), Name File (NF), Find File (FF), Blank File (BF), or Unblank File (UF) parameter.

b) When A0 = high:

PBO1 = Z-axis (Pen Enable command and parameter detected on I/O Board and sent separately to Control Board as Z-axis bit to become PBO1).

PBO2 = file blanking bit (used with BF and UF).

PBO3-PBO6 = TTL blanking bits (used with WX).

CASE 3.

If the Control Board instruction Find Location (FL) is detected, then ID1-ID12 = binary value (0-2047) used when A0 = low as the next write pointer to address 1350A memory.

Table 8-2. ID1-ID12 Definitions

A0 State	CASE 1. I/O Instruction (DO WRITE)	CASES 2&3. Control Board Instruction (Get Busy)
low	ID1-ID10 = 1023 is Text flag	Case 2. Not FL ID1-ID6 become PBO1-6 PBO1-PBO5 = file no. PBO6 = don't care
	ID1-ID10 < 1023 is binary X value (Plot mode)	Case 3. FL instruction ID1-ID12 = binary X value used as next write pointer
high	If Text mode: ID1-ID7 = ASCII ID8&ID9 = character size ID10 = character rotation bit	Case 2. PBO1 = Z-axis bit PBO2 = file blanking bit PB03-PB06 = TTL blanking bits
	If Plot mode: ID1-ID10 = binary Y value	

8-28. SCHEMATIC 2A PRINCIPLES OF OPERATION.

HP-IB Input/Output Assembly A3 configures the 1350A to be an addressable listen-only device on the Hewlett-Packard Interface Bus (HP-IB).

Schematic 2A contains: (a) HP-IB interface and handshake circuits; (b) Instruction decoder and latch; and (c) Control Get Busy circuits.

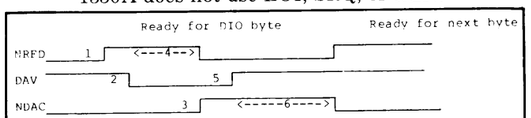
The 1350A receives all information from HP-IB via 8-bit bytes on the DIO lines. Bytes are transferred one at a time via a 3-wire handshake (NRFD,DAV,NDAC). If the handshake sequence is not completed, then no more bytes will be transferred and bus communication stops (bus is "hung").

Bus Mnemonics: (HP-IB is low = true logic; low = "1" and high = "0")

DIO1-DIO8 ..... Data Input/Output
NRFD ..... Not Ready For Data
DAV ..... Data Valid
NDAC ..... Data Not Accepted
IFC ..... Interface Clear
ATN ..... Attention
EOI ..... End Or Identify
SRQ ..... Service Request
REN ..... Remote Enable

NOTE

1350A does not use EOI, SRQ, or REN.



1. NRFD goes high (wired-And; all listeners are ready for a data byte).
2. DAV goes low (talker says data byte on DIO lines is valid).
3. NDAC goes high (wired-And; all listeners have accepted the byte).

NOTE

Steps 1, 2, and 3 complete the transfer sequence. The handshake lines must now return to initial conditions before another byte can be transferred.

4. Listener can return NRFD low when DAV goes low. NRFD must return low before or at the same time as NDAC goes high.
5. Talker can return DAV high after NDAC goes high.
6. Listener can return NDAC low when DAV goes high. NDAC must return low before or at the same time as NRFD goes high.

Figure 8-10. HP-IB Handshake Sequence for Data Transfer

Operation of circuits on schematic 2A is covered by three cases:

1. IFC (Interface Clear).
2. HP-IB in Command Mode (ATN = low).
3. HP-IB in Data Mode (ATN = high).

8-29. IFC (Interface Clear).

After the 1350A is powered on (or whenever a new program is to be sent to the 1350A) the Controller should first set IFC low momentarily.

IFC = low clears Listen Latch U17B and Control Get Busy Enable Latch U23A. It also ensures that the 1350A will be in "listen for program" and prevents Text mode (schematic 2B, U1A and U29A) after 1350A is first addressed to listen.

Also, IFC = low causes Ready Latch U43A to be clocked via U16B on schematic 2B. This enables U18A so that the 1350A can signal Ready For Data (NRFD = high) when its Acceptor Handshake is enabled.

8-30. COMMAND MODE (ATN = low).

When ATN goes low, 1350A Acceptor Handshake is enabled (U9B output is low). This allows the 1350A to participate in handshakes.

While ATN is low the 1350A can recognize: (1) its listen address; or (2) a Universal Unlisten command. If addressed to listen, Listen Latch U17B will cause Acceptor Handshake to remain enabled after ATN goes high. If not addressed or if an Unlisten command (ASCII "?") is received (U13 output = low), then U17B causes Acceptor Handshake to be disabled (U19B pin 6 = high) when ATN goes high.

8-31. DATA MODE (ATN = high).

If addressed to listen, the 1350A will receive its device-dependent commands (GTML mnemonics) and required parameters.

First the 1350A goes to "listen for program" mode. Two bytes are received, decoded by Instruction Decoder U7, and latched into Instruction Latch U28 and U21.

After two "program" bytes the 1350A automatically goes to "listen for data" mode (schematic 2B). Parameter (or text) bytes are then received until a ":" (colon) or a CR (Carriage Return) or a LF (Line Feed) byte is received. When this happens, the 1350A returns to "listen for program."

CR or LF or ":" bytes are detected by U14 and U24B. Since U14 is disabled in Text mode, the 1350A must receive an ETX (End of Text) byte before it will be able to exit Text mode and return to "listen for program." ETX is detected by U64.

Handshake Precision Timing Generator.

After each byte is received from HP-IB, whether instruction "program" or data, Ready Latch U43 must be clocked by PRNRC (Positive, Release Not Ready Condition). This allows the 1350A to signal Ready For Data and receive the next DIO byte.

When DAV goes low, U18A causes NRFD to return low because U10B output goes high. Approximately 250 ns after DAV goes low U25 causes U43B to be clocked so that U32 is released to count. U32 produces clock signals for circuits on schematic 2B that control latching of DIO parameter (or text) byte on schematic 2C. U18A will continue to hold NRFD low after U32 has been clocked twice.

Approximately 500 ns after DAV goes low NDAC is set high by U25. NDAC returns low as soon as DAV is returned high by the talker (U25 reset by U10B).

Ready Latch U43 must now be clocked by PRNRC in order for the next handshake to proceed.

Control Board Instructions.

"Program" instructions are either I/O Board or Control Board instructions. When a Control Board two-byte instruction is detected, CTRL INST goes low. The negative edge of this level change is passed by C2 so that U23A sees a momentary low pulse on its set input. When set, U23A enables U36A.

When a ":" (or CR or LF) delimiter is detected, U19C produces a positive edge that latches the instruction (I1-I5) on the Control Board.

The ":" (or CR or LF) also allows U36A to enable U58C. Approximately 570 ns after the instruction latch clock (U19C), a negative edge clock is produced by U58C that tells the Control Board to act on the command (Control Get Busy).

After sensing a Control Get Busy clock, the Control Board signals its "busy" status by setting CTRL BUSY low. When the Control Board has finished processing the command it returns CTRL BUSY high. This positive edge clocks U23A inverting output high. U36A and U58C are now disabled until the next Control Board instruction is detected.

The positive edge of CTRL BUSY also causes a PRNRC clock to be produced (schematic 2B) so that the 1350A can signal Ready For Data.

If the Control Board never returns CTRL BUSY high, then PRNRC will not be produced and the 1350A will hang the bus. For example, this can occur when a file is addressed via FF, EF,BF, or UF that was not previously named (NF #).

I/O Board Instructions.

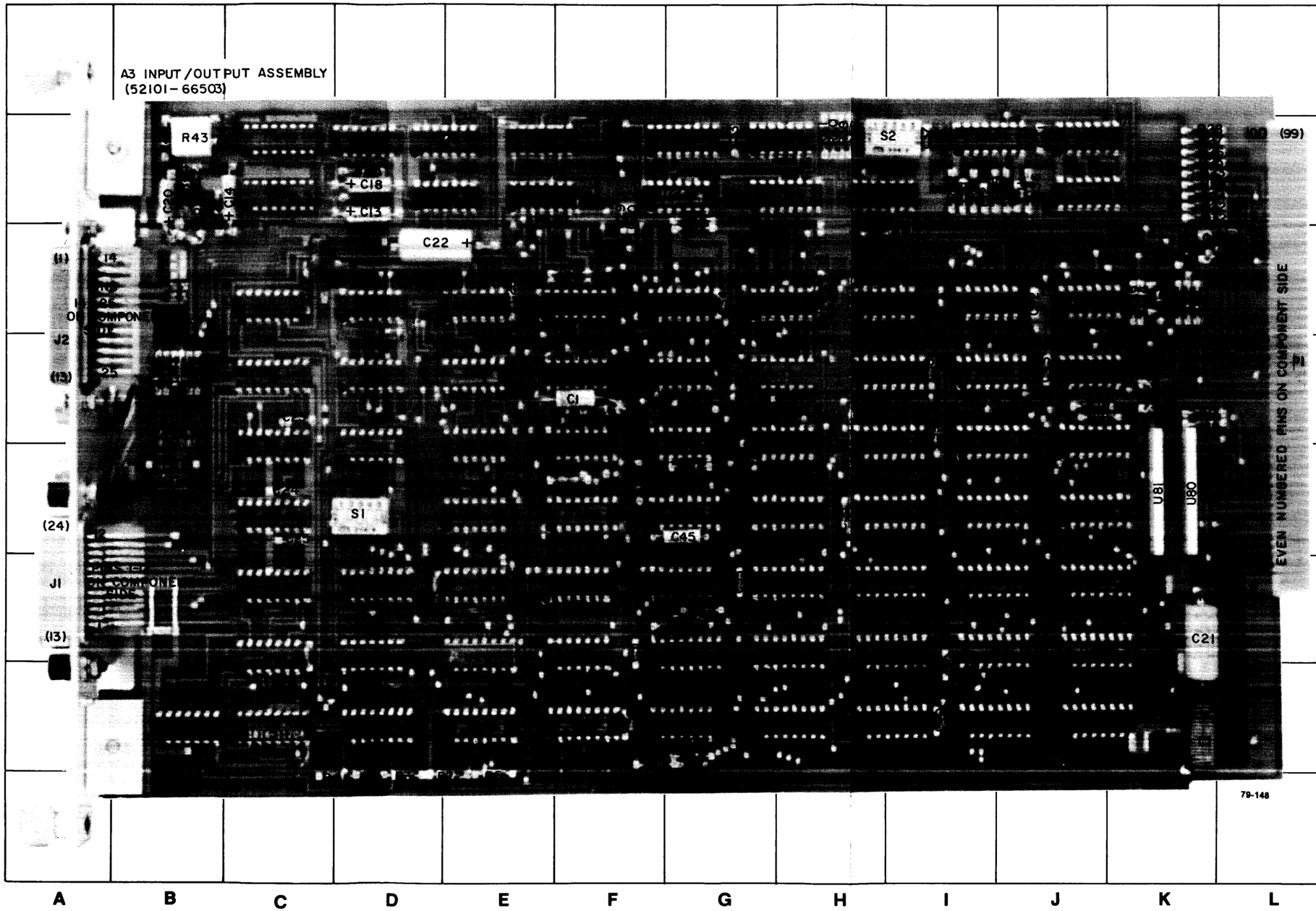
When an Input/Output Board "program" instruction is detected CTRL INST goes high. Latch Instruction clock (LTCH INST) and Control Get Busy clock are not produced.

I/O Instruction Decoder U20 is enabled. U20 outputs control signals to I/O Board circuits on schematics 2B and 2C. I/O Board "program" instructions are: (1) Pen Enable (PE); (2) Character Size (CS); (3) Text (TX); and (4) Plot Absolute (PA).

Table 8-3. A3 U7 ROM (1816-1120) Character Decoding

DI0 Address Lines							Decimal	Char.	U7 Output Pins			
									MSB			LSB
7	6	5	4	3	2	1	Value	ASCII	9	10	11	12
0	0	0	0	0	1	1	3	ETX	0	0	0	1
0	0	0	1	0	1	0	10	LF	0	1	1	0
0	0	0	1	1	0	1	13	CR	0	1	1	0
0	0	1	0	1	0	0	20	DC4	0	1	0	1
0	1	0	1	1	0	0	44	,	0	1	0	0
0	1	1	1	0	1	0	58	:	0	1	1	0
0	1	1	1	0	1	1	59	;	0	0	1	1
1	0	0	0	0	0	1	65	A	0	1	1	1
1	0	0	0	0	1	0	66	B	1	1	0	0
1	0	0	0	0	1	1	67	C	0	0	0	0
1	0	0	0	1	0	1	69	E	1	0	0	0
1	0	0	0	1	1	0	70	F	1	1	1	0
1	0	0	1	1	0	0	76	L	1	0	0	0
1	0	0	1	1	0	1	77	M	0	1	0	0
1	0	0	1	1	1	0	78	N	1	0	0	1
1	0	1	0	0	0	0	80	P	0	0	1	1
1	0	1	0	0	1	1	83	S	1	0	1	0
1	0	1	0	1	0	0	84	T	0	0	1	0
1	0	1	0	1	0	1	85	U	1	0	1	1
1	0	1	0	1	1	1	87	W	1	1	0	1
1	0	1	1	0	0	0	88	X	0	0	0	0
1	1	0	0	0	0	1	97	a	0	1	1	1
1	1	0	0	0	1	0	98	b	1	1	0	0
1	1	0	0	0	1	1	99	c	0	0	0	0
1	1	0	0	1	0	1	101	e	1	0	0	0
1	1	0	0	1	1	0	102	f	1	1	1	0
1	1	0	1	1	0	0	108	l	1	0	0	0
1	1	0	1	1	0	1	109	m	0	1	0	0
1	1	0	1	1	1	0	110	n	1	0	0	1
1	1	1	0	0	0	0	112	p	0	0	1	1
1	1	1	0	0	1	1	115	s	1	0	1	0
1	1	1	0	1	0	0	116	t	0	0	1	0
1	1	1	0	1	0	1	117	u	1	0	1	1
1	1	1	0	1	1	1	119	w	1	1	0	1
1	1	1	1	0	0	0	120	x	0	0	0	0

Note: 0 = low; 1 = high.



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	F-5	R10	C-6	U20	E-3
C2	K-6	R11	C-6	U21	E-2
C3	H-6	R12	F-2	U22	F-6
C4	G-6	R13	G-2	U23	F-5
C5	C-6	R14	K-6	U24	F-5
C6	G-1	R15	K-6	U25	F-4
C7	K-5	R16	K-6	U26	F-3
C8	G-3	R17	K-6	U27	F-3
C9	H-7	R18	J-5	U28	F-2
C10	I-2	R19	J-5	U29	G-6
C11	J-7	R20	G-3	U30	G-5
C12	I-7	R21	G-3	U31	G-4
C13	D-7	R22	K-7	U32	G-4
C14	C-7	R23	K-7	U33	G-3
C15	B-7	R24	K-7	U34	G-3
C16	B-7	R25	K-7	U35	G-2
C17	D-6	R26	K-7	U36	H-6
C18	D-7	R27	K-7	U37	H-5
C19	B-5	R28	K-7	U38	H-5
C20	B-7	R29	I-7	U39	H-4
C21	K-3	R30	I-7	U40	H-3
C22	D-6	R31	I-7	U41	H-3
C23	C-5	R32	K-6	U42	H-2
C24	C-4	R33	D-7	U43	H-6
C25	C-4	R34	B-7	U44	I-5
C26	C-3	R35	B-7	U45	I-5
C27	D-3	R36	J-7	U46	I-4
C28	E-6	R37	K-6	U47	I-3
C29	F-7	R38	H-7	U48	I-3
C30	F-7	R39	H-7	U49	I-2
C31	F-3	R40	H-7	U50	I-6
C32	F-2	R41	H-7	U51	I-5
C33	G-7	R42	B-7	U52	I-5
C34	G-6	R43	B-7	U53	I-4
C35	G-3	R44	B-7	U54	I-3
C36	H-4	R45	D-7	U55	I-3
C36	H-4	R46	B-5	U56	I-2
C37	I-7	R47	B-5	U57	J-6
C38	I-5	R48	B-5	U58	J-5
C39	I-5	R49	B-5	U59	J-5
C40	I-2	R50	K-7	U60	J-4
C41	J-7	R51	F-4	U61	J-3
C42	J-6	R52	G-4	U62	J-3
C43	J-5	R53	F-5	U63	J-2
C44	K-5	R54	F-6	U64	B-2
C45	G-4	R55	F-6	U65	J-7
C46	G-5	S1	D-4	U66	J-7
CR1	I-7	S2	I-7	U67	I-7
CR2	B-7	U1	C-6	U68	H-7
CR3	B-5	U2	C-5	U69	H-7
J1	A-3	U3	C-5	U70	H-7
J2	A-6	U4	C-4	U71	G-7
L1	K-2	U5	C-3	U72	G-7
P1	L-5	U6	C-3	U73	E-7
Q1	K-6	U7	C-2	U74	E-7
Q2	K-6	U8	D-6	U75	E-7
Q3	K-6	U9	D-5	U76	D-7
R1	F-4	U10	D-5	U77	C-7
R2	E-1	U12	D-3	U78	C-7
R3	D-1	U13	D-3	U79	E-7
R4	D-1	U14	D-2	U80	K-4
R5	E-1	U15	E-6	U81	K-4
R6	K-5	U16	E-5	VR1	J-7
R7	K-5	U17	E-5		
R8	G-6	U18	E-4		
R9	G-7	U19	E-3		

Figure 8-11. Input/Output Board A3 Component Locator

Mnemonics on I/O Board A3

A0 — Memory Address Bit 0 — Serves important functions on both the Display and Control Boards. It is used on the Display Board to determine when x or y information is being read or written. It determines the configuration of RAM for storage. On the Control Board it is a multiplex select line to determine whether File Name bits or Blanking bits are sent to memory. During x-time (A0 = low) File Names are selected and during y-time (A0 = high) Blanking information is selected. When selecting which type of data, A0 also determines the read/write status of the memories by means of the Memory Read/ Write Controller.

I1-I5 — Control instruction bus - used for internal instrument control utilizing information decoded from the HP-IB bus.

ID1-ID12 — Input Data bus - after data from the HP-IB bus is buffered and latched, it is decoded for parameters (BLANK, UNBLANK, PEN ENABLE, etc.), multiplexed, gated and becomes the data bus D1-D12. ID13 is not used.

L = CONTROL BUSY — Inhibits further control instruction exectuion when low. Low only when instructions are being carried out.

L =CONTROL INST — Goes low when control instructions have been received and decoded and stays low until instructions have been completed and the Control Instruction Handshaker has reset CONTROL BUSY to a logic high.

L = DATAL — Low level turns front panel LED on. Low when data is being received.

L = DO WRITE — A low level allows information to be written into memory - low only when data is being transferred to memory.

L = INTERFACE HOLDOFF — Inhibits further vector generation until the 1338A display can assimilate the data it has. Low inhibits, high continues.

L = POWER INTERRUPT — Low level indicates a line voltage fluctuation or power interrupt has occurred. Stays low until power is reset or instrument receives a DC4(20) ASCII command via HP-IB.

L = PROGL — Low level turns front panel LED on. Low when program — Control Board or I/O Board instructions — are being received.

L = RESET — Momentarily low when instrument is powered on or a new program is to be initiated. Resets U17B and U23A.

L = VECTOR BUSY — Indicates that data is being translated into analog form in the D/A Converter. When high, the Vector Generator is processing available values and has not sent them to the D/A.

N = CHANGE DATA — This negative transition signals the I/O board that the first byte of data (x-coordinates) has been written and it is ready for the second byte (y-coordinates).

N = CONTROL GET BUSY — Negative transition clocks U42A via U411 (schematic 3A) to initiate the "Control Busy" sequence.

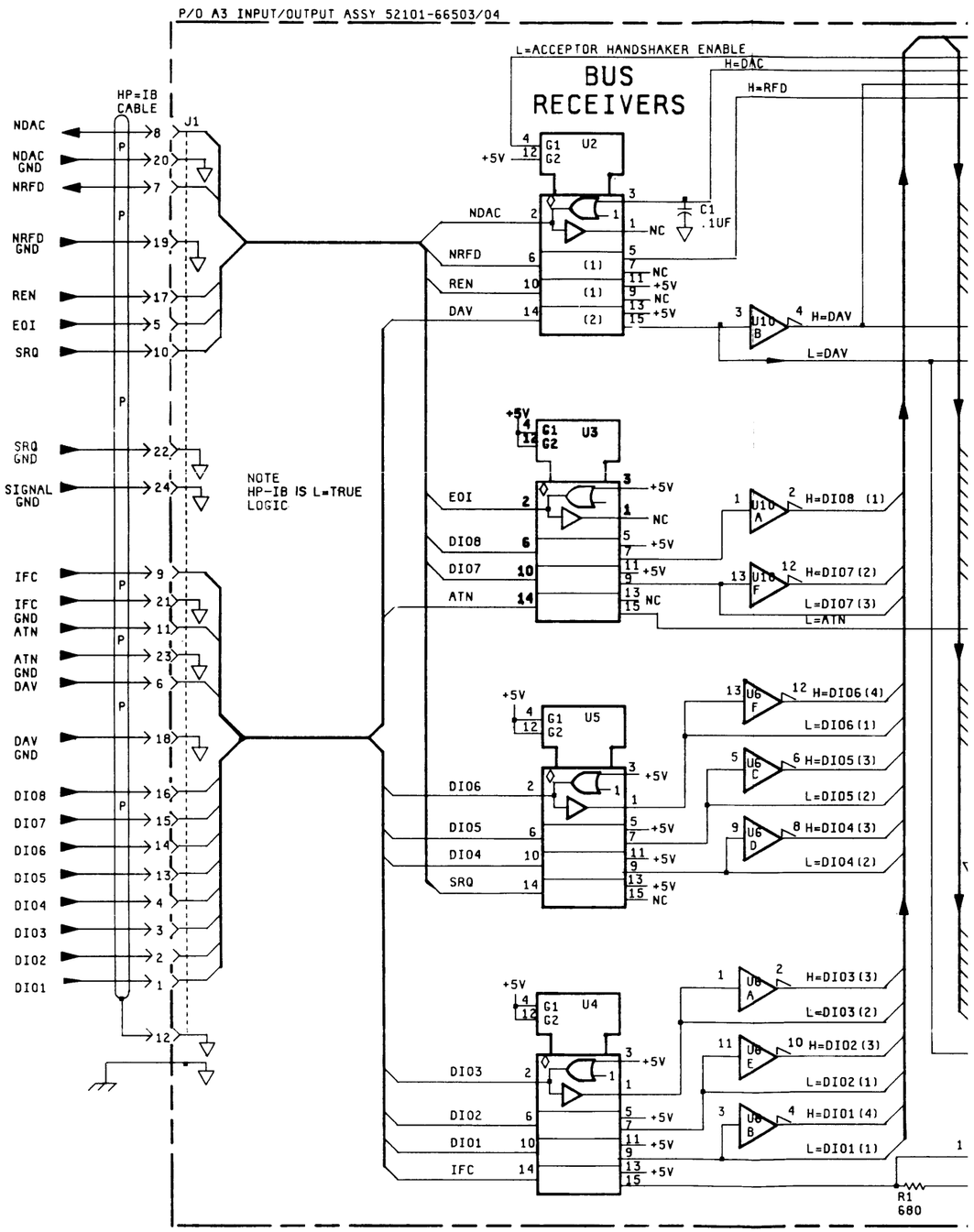
N = LATCH INST — Negative transition causes control instructions to be latched into the Instruction Latch, U25. It also allows L = CONTROL INST to be clocked to the output of U42B, disabling the CONTROL INSTRUCTION HANDSHAKER (all on Schematic 3A). This ensures that no new control instructions are latched in until the current instructions have been executed.

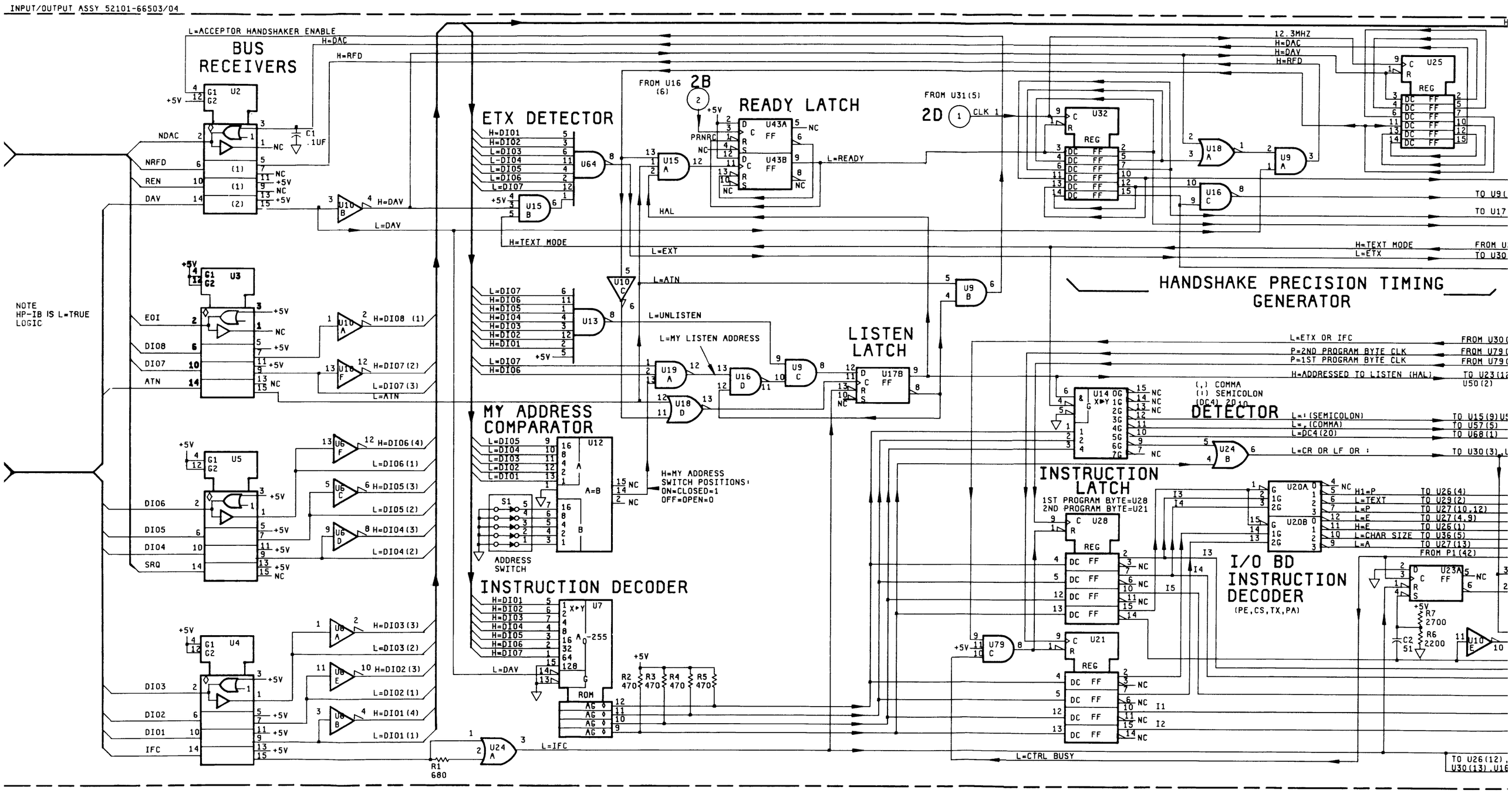
P = X ADDR — Used to latch File Name Bits PBO5 and 6 into Color Bits Latch U65A. Also used to generate Color Valid Signal for 1338A Tri-color Display.

P = Y ADDR — Inverted and used as clock for TTL Blanking Latch U67. This latches information from File Name Bits PBO3-6 to determine which of 4 TTL outputs will be high (blanked).

PBO1-PBO5 — Name Bits — See Section 8 - 1350 Memory Organization, for more complete explanation.

PE BIT — Pen Enable Bit — tells the 1350A to blank or unblank when drawing a character or vector. 1 = unblanked (pen down), 0 = blanked (pen up). It is sent as a parameter in the y byte.




INPUT/OUTPUT ASSY 52101-66503/04
BUS RECEIVERS
ETX DETECTOR
READY LATCH
LISTEN LATCH
MY ADDRESS COMPARATOR
INSTRUCTION DECODER
HANDSHAKE PRECISION TIMING GENERATOR
DETECTOR
INSTRUCTION LATCH
I/O BD INSTRUCTION DECODER
(PE,CS,TX,PA)
NOTE
HP-IB IS L=TRUE LOGIC
L=ACCEPTOR HANDSHAKER ENABLE
H=DAC
H=RFD
H=DAV
L=DAV
H=TEXT MODE
L=EXT
L=ATN
L=UNLISTEN
L=MY LISTEN ADDRESS
L=READY
L=IFC
L=CTRL BUSY
L=ETX OR IFC
P=2ND PROGRAM BYTE CLK
P=1ST PROGRAM BYTE CLK
H=ADDRESSED TO LISTEN (HAL)
L=CR OR LF OR :
H=MY ADDRESS SWITCH POSITIONS: ON=CLOSED=1 OFF=OPEN=0
ADDRESS SWITCH
1ST PROGRAM BYTE=U28
2ND PROGRAM BYTE=U21
12.3MHZ
FROM U16 (6)
FROM U31(5)
FROM P1(42)
ROM
R1 680
R2 470
R3 470
R4 470
R5 470
R6 2200
R7 2700
C1 .1UF
C2 51

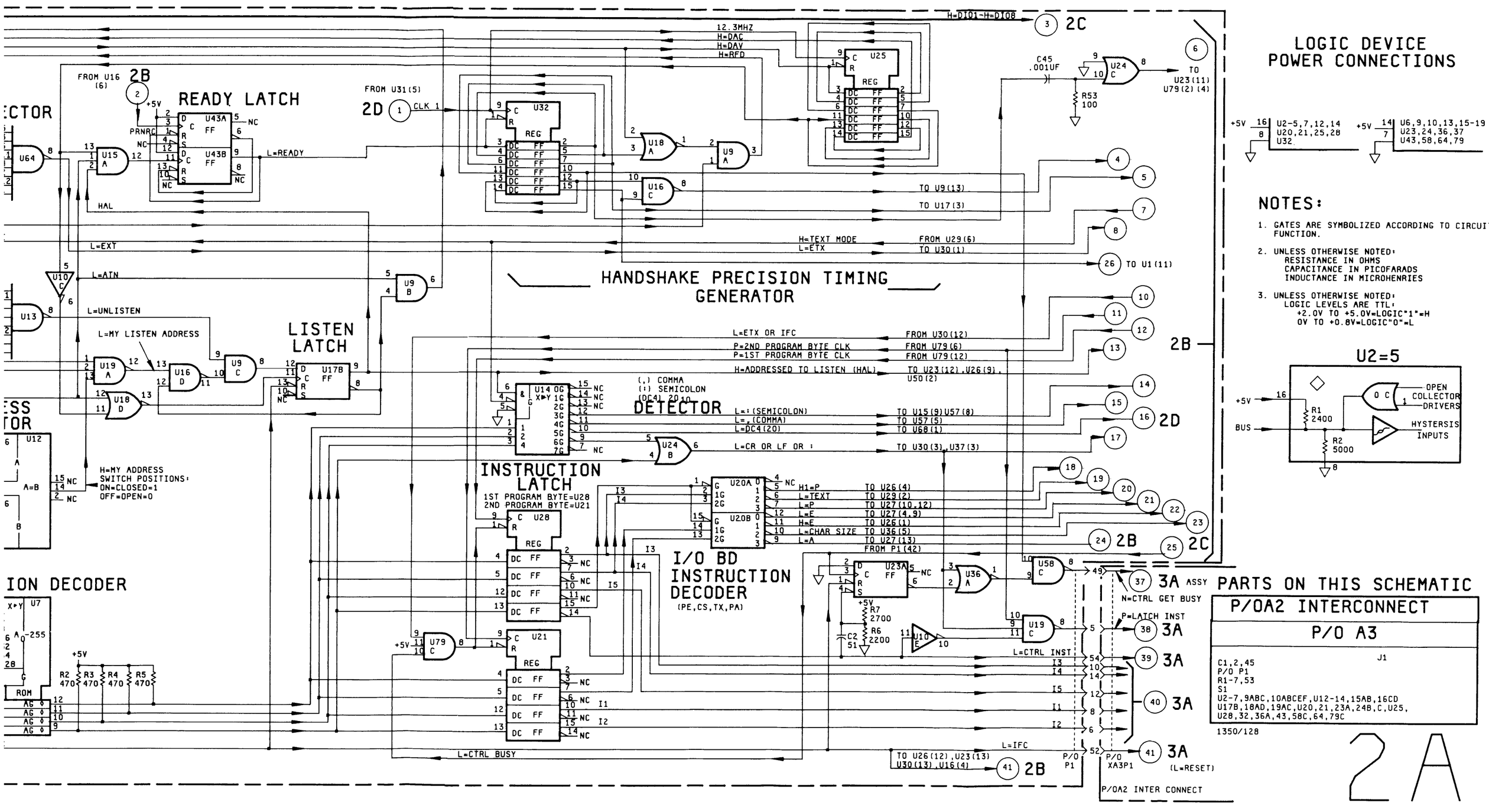


Figure 8-12.
Schematic 2A
8-15

8-32. SCHEMATIC 2B PRINCIPLES OF OPERATION.

Schematic 2B is made up of circuits that: (a) determine whether the 1350A is in "listen for program" or "listen for data"; (b) indicate when the 1350A can signal that it is ready for the next DIO byte from HP-IB; (c) produce the DO WRITE signal; and (d) provide Pen Enable (Z-axis) status to the Control Board.

8-33. LISTEN FOR PROGRAM/DATA CIRCUITS.

Listen For Program.

After the 1350A has received an IFC = low signal and then been addressed to listen by an HP-IB Controller, U50A output goes high. This turns Q1 on. LPROGL (Low, Program Listen) goes low to turn on front-panel "listen for program" LED.

U1B and U79A/B are enabled. Ready For Program Byte Latch U17A controls the handshaking of "program" bytes from HP-IB by producing PRNRC (via U58A and U16B) to release the Not Ready condition on schematic 2A. U79A and U79B produce clock edges that latch the two instruction (program) bytes on schematic 2A.

When Listen For Program/Data Latch U1A first causes U50A to allow "listen for program", the negative-going edge from U37D output is passed by C5. This sets Data Enable After Program Controller U8B, preventing the Ready For Data Byte sequence from ocurring until after the 1350A has gone to "listen for data".

Listen For Data.

When the second "program" byte is received, U1B inverting output (in the Instruction Latch Clock Generator) produces a positive edge. This clocks U1A, U29A, and U8B.

Listen For Program/Data Latch U1A now causes U26C output to be high. This turns Q2 on and Q1 off. LDATAL (Low, Data Listen) goes low to turn on front-panel "LISTEN for DATA" LED. LPROGL goes high to turn off front-panel "LISTEN for PROGRAM" LED. U37F disables the Instruction Latch Clock Generator while in "listen for data".

Text Mode Latch U29A reports whether or not a Text (TX) instruction was received.

Data Enable after Program Controller U8B now permits the Ready for Data Byte sequence if not in Text mode. This sequence allows the 1350A to capture parameter bytes from HP-IB until the 1350A receives a ":" (or CR or LF). Ready For Data Byte Latch U8A Q output gets clocked high when a parameter byte is received from HP-IB. This turns on 12.3 MHz CLK2 for four pulses (schematic 2D). Four State Counter U33A/B causes DIO1-DIO4 to be converted from parallel to serial and stored (schematic 2C). After the fourth state, U33B causes U8A to be reset (via U30C) and the 1350A can signal that it is ready for the next data byte from HP-IB.

The parameter binary value is latched for output to the Control Board by a "," (comma) from HP-IB. This negative clock edge is produced by Data/Text Selector and Latch Clock Generator U57A.

If Text Mode Latch U29A indicates that a Text (TX) instruction has been received, then text byte handshaking from HP-IB is controlled by Ready For Text Byte Latch U29B.

8-34. DO WRITE CIRCUITS.

Low-going DO WRITE pulses are produced as a result of Plot Absolute (PA) or Text (TX) "program" instructions. DO WRITE tells the Control Board to write X and Y (or text) values to 1350A memory. The Control Board responds with a low-going WRITING signal and a negative-going CHANGE DATA clock.

When A0 (1350A memory address line zero) is low, the Control Board writes X value to 1350A memory following DO WRITE. If Text mode, U50B causes X value to be output as 1023 (ID1-ID10 are high, schematic 2C). This is the Text flag to 1350A character Generator.

Generation of DO WRITE will be covered by two cases: (1) Plot Absolute; and (2) Text.

CASE 1.

Detection of a Plot Absolute by U27D allows U57C to produce a low-going DO WRITE signal when a ";" (semicolon) is received from HP-IB. Prior to the ";" the 1350A should receive X and Y values separated by a "," (comma).

Data byte acquisition from HP-IB is controlled by the Ready For Data Byte sequence for each parameter byte.

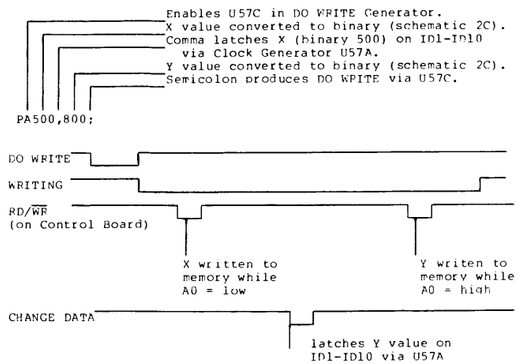


Figure 8-13. Plot Absolute DO WRITE, WRITING, CHANGE DATA Sequence

CASE 2.

Detection of a Text command allows Ready For Text Byte Latch U29B and U22C in the DO WRITE Generator to produce a low-going DO WRITE pulse for each text byte received.

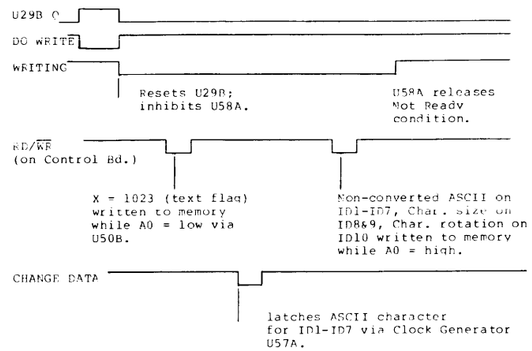


Figure 8-14. Text Mode DO WRITE, WRITING, CHANGE DATA Sequence

8-35. RETURN TO LISTEN FOR PROGRAM.

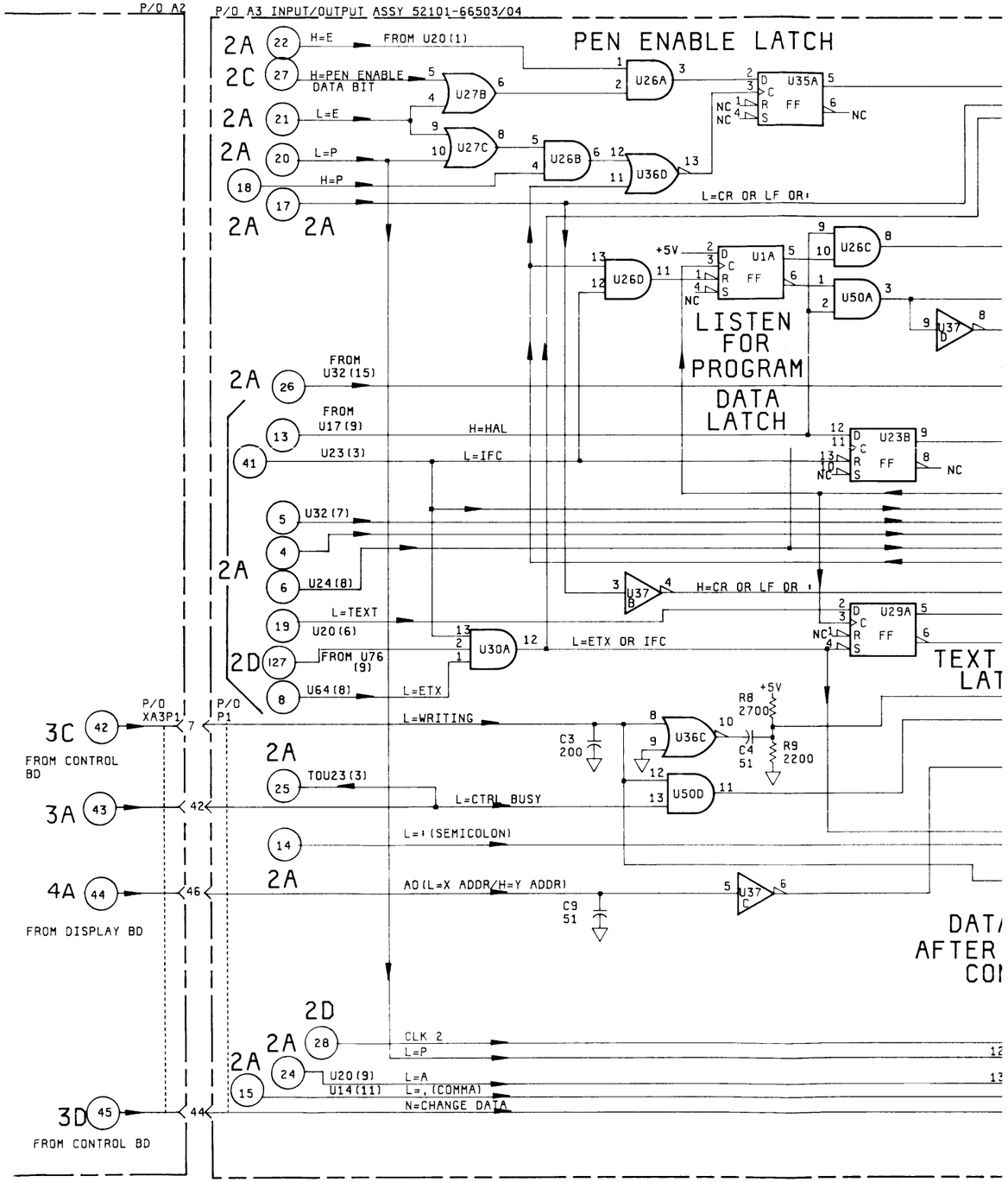
If 1350A is in Text mode, an ETX (End of Text) is required in order to exit Text mode.

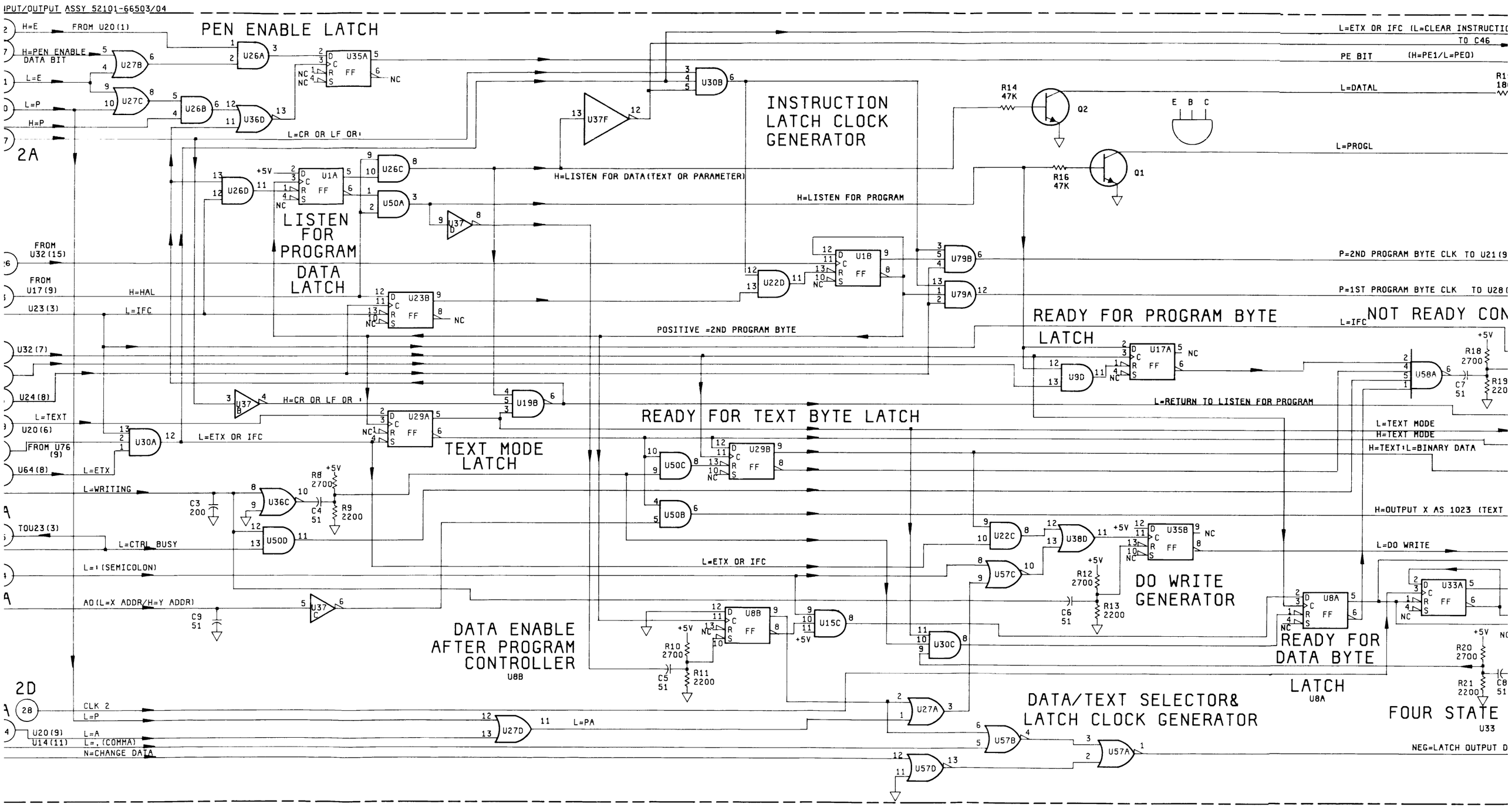
To terminate any instruction (including a previously exited Text instruction) the 1350A requires a ":" (or CR or LF) character from HP-IB. This causes U19B output to go low. Listen For Program/Data Latch U1A is reset to "program." Instruction (program) Latch U28 and U21 on schematic 2A is reset.

8-36. PEN ENABLE (Z-AXIS) CIRCUIT.

Pen Enable (PE) "program" instruction is decoded by U20 on schematic 2A. PE parameter is converted to binary on schematic 2C. PE parameter is latched on schematic 2C by a "," (comma) from HP-IB via Clock Generator U57A. This becomes the Pen Enable Data Bit which is applied to U27B. This Data Bit is clocked into Pen Enable Latch U35A when U19B output goes low to signal "return to listen for program."

Pen Enable Latch U35A output defines Z-axis status for all 1350A vectors and characters. High = beam on; low = beam off. Z-axis status is sent via the Control Board to the Display Board. From the Display Board, Z-axis status is sent back to the Control Board as PBO1 when A0 = high. This enables/disables 1350A Z-axis output (unless overridden by file blank/unblank bit PBO2).


P/O A2
P/O A3 INPUT/OUTPUT ASSY 52101-66503/04
PEN ENABLE LATCH
2A 22 H=E
FROM U20(1)
2C 27 H=PEN ENABLE DATA BIT
2A 21 L=E
2A 20 L=P
18 H=P
17
2A 2A
U26A
U27B
U27C
U26B
U36D
U35A
NC
L=CR OR LF OR
+5V
U1A
U26D
U26C
U50A
U37
LISTEN FOR PROGRAM DATA LATCH
2A 26 FROM U32(15)
13 FROM U17(9)
41 U23(3)
H=HAL
L=IFC
U23B
5 U32(7)
4
2A 6 U24(8)
U37
H=CR OR LF OR
19 L=TEXT
U20(6)
U29A
TEXT LAT
2D 127 FROM U76 (9)
8 U64(8)
U30A
L=ETX OR IFC
L=ETX
P/O XA3P1
P/O P1
3C 42
FROM CONTROL BD
L=WRITING
R8 2700
R9 2200
C3 200
C4 51
U36C
2A 25 TOU23(3)
3A 43
L=CTRL BUSY
U50D
14 L=: (SEMICOLON)
4A 44
FROM DISPLAY BD
A0(L=X ADDR/H=Y ADDR)
C9 51
DATA AFTER CO
2D
2A 28 CLK 2
L=P
2A 24 U20(9)
15 U14(11)
L=A
L=, (COMMA)
N=CHANGE DATA
3D 45
FROM CONTROL BD



PEN ENABLE LATCH
INSTRUCTION LATCH CLOCK GENERATOR
LISTEN FOR PROGRAM DATA LATCH
READY FOR PROGRAM BYTE LATCH
NOT READY CON
READY FOR TEXT BYTE LATCH
TEXT MODE LATCH
DO WRITE GENERATOR
DATA ENABLE AFTER PROGRAM CONTROLLER
U8B
READY FOR DATA BYTE LATCH
U8A
DATA/TEXT SELECTOR& LATCH CLOCK GENERATOR
FOUR STATE
U33
H=E
FROM U20(1)
H=PEN ENABLE DATA BIT
L=E
L=P
H=P
2A
L=CR OR LF OR
H=LISTEN FOR DATA(TEXT OR PARAMETER)
H=LISTEN FOR PROGRAM
L=ETX OR IFC (L=CLEAR INSTRUCTI
TO C46
PE BIT
(H=PE1/L=PE0)
L=DATAL
L=PROGL
R14 47K
R16 47K
Q2
Q1
E B C
FROM U32(15)
FROM U17(9)
U23(3)
H=HAL
L=IFC
POSITIVE =2ND PROGRAM BYTE
P=2ND PROGRAM BYTE CLK TO U21(9
P=1ST PROGRAM BYTE CLK TO U28(
L=IFC
U32(7)
U24(8)
L=TEXT
U20(6)
FROM U76 (9)
U64(8)
L=ETX
L=WRITING
TOU23(3)
L=CTRL BUSY
L=: (SEMICOLON)
AO(L=X ADDR/H=Y ADDR)
H=CR OR LF OR
L=ETX OR IFC
L=RETURN TO LISTEN FOR PROGRAM
L=TEXT MODE
H=TEXT MODE
H=TEXT:L=BINARY DATA
H=OUTPUT X AS 1023 (TEXT
L=DO WRITE
L=ETX OR IFC
R8 2700
R9 2200
C3 200
C4 51
C9 51
R10 2700
R11 2200
C5 51
R12 2700
R13 2200
C6 51
R18 2700
R19 220
C7 51
R20 2700
R21 2200
C8 51
2D
CLK 2
L=P
L=A
L=, (COMMA)
N=CHANGE DATA
U20(9)
U14(11)
L=PA
NEG=LATCH OUTPUT D

INSTRUCTION LATCH CLOCK GENERATOR

READY FOR TEXT BYTE LATCH

READY FOR PROGRAM BYTE LATCH

NOT READY CONTOLLER

DO WRITE GENERATOR

READY FOR DATA BYTE LATCH

U8A

DATA/TEXT SELECTOR& LATCH CLOCK GENERATOR

FOUR STATE COUNTER

U33

LOGIC DEVICE POWER CONNECTIONS

ALL IC SUPPLY CONFIGURATIONS

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A3

C3-9
Q1-2
R8-21
U1,8,9D,15C,16B,17A,19B,22CD
U23B,26,27,29,30ABC,33,35
U36CD,37B,C,D,F,38D,50,57,58A,79AB

1350/125

2B

Figure 8-15. Schematic 2B

8-37. SCHEMATIC 2C PRINCIPLES OF OPERATION.

Schematic 2C contains: (1) Parameter Shift Register/ Text Latch; (2) BCD-to-Binary Converter (for parameters); (3) Parameter or Text Selector and Latch; (4) Character Size and Rotation Latch; and (5) Output Selector circuits.

Operation of circuits on schematic 2C will be covered for two cases: (1) 1350A receiving parameter(s); and (2) 1350A receiving text.

8-38. CASE 1. 1350A RECEIVING PRAMETER(S).

In "listen for data" mode, the four LSBs (DIO1-DIO4) of each parameter byte are converted from Binary Coded Decimal (BCD) to binary. This is because the four LSBs of the ASCII code for digits is in BCD.

This conversion process continues for each digit in the parameter until a "," (comma) is received from HP-IB. The "," delimits (bounds) the parameter value by latching the binary result of the conversion for output to the Control Board. If a Plot Absolute (PA) comand was received, then the "," latches the binary value of the X parameter and a CHANGE DATA signal (schematic 2B) from the Control Board latches the binary value of the Y parameter (in response to a ";" from HP-IB).

NOTE

Several vectors may be entered following each PA command. For example, "PA100,300; 200,500; 300,800;400,1000;:". This draws four vectors.

BCD TO BINARY CONVERSION.

The Parameter Shift Register/Text Latch (U39-U42) is placed in its shift register mode if Text Mode Latch U29A (schematic 2B) does not receive a text command. Data selector U34 converts DIO1-DIO4 from parallel to serial. Each serial DIO value is shifted through U42, U41, U40, and U39 by CLK2.

CLK2 is turned on by Ready For Data Byte Latch U8A (schematic 2B). Four CLK2 pulses are produced for each digit in the parameter. Each digit in the parameter gets shifted down through the cascaded shift register by subsequent CLK2 bursts. For example, if a parameter contains three digits, the first digit will be in U40, the second in U41, and the third in U42.

Parameter Shift Register (U39-U42) outputs are automatically converted to binary by the full-adder network of the BCD-to-Binary Converter (U44-U49, U51-U54).

Binary parameter value (CD1-CD14) is selected at Parameter or Text Selector and Latch (U56, U62, U63) when Ready For Text Byte Latch U29B (schematic 2B) signals that the 1350A is NOT in Text mode.

Latch Converted Parameter For Output.

The binary value of the parameter is latched for output at the Parameter or Text Selector and Latch (U56, U62, U63). The latching clock signal comes from Clock Generator U57A on schematic 2B.

This clock is produced when a "," (comma) is received from HP-IB or when the Control Board produces a CHANGE DATA signal (schematic 2B).

For a Plot Absolute, the comma latches the X binary value and the CHANGE DATA latches the Y binary value.

Character Size And Rotation.

When a Character Size (CS) command is detected by U20 on schematic 2A, the input to U36B pin 5 goes low. This enables U36B. Next, the CS parameter is converted to binary and latched into U56 by a "," (comma) from HP-IB. When the 1350A receives a ":" (or CR or LF) the CS command is delimited (completed). U36B clocks the CS parameter into Character Size and Rotation Latch U55 via U19B (schematic 2B) to preserve this preconditioning for any subsequent Text (TX) commands.

8-39. CASE 2. 1350A RECEIVING TEXT.

In Text mode, ASCII DIO bytes (received from HP-IB while 1350A is in "listen for data" mode) are not converted to binary. Each unconverted ASCII byte is latched and presented to the Control Board (along with the character size and rotation bits) immediately following the text flag.

The text flag is generated by setting ID1-ID10 lines all high (= 1023) when memory address line A0 is low. Following the text flag, ID1-ID10 are defined as follows when A0 goes high:

ID1-ID7 = ASCII character
ID8 & ID9 = character size (1,2,4,8)
ID10 = rotation bit (low = 0; high = 90 degrees).

Latch Unconverted Text Byte For Output.

Parameter Shift Register/Text Latch (U39-U42) is placed in its parallel latch mode when Text Mode Latch U29A on schematic 2B receives a Text command.

The 8 DIO bits are latched into U41 and U42 by Ready For Text Byte Latch U29B on schematic 2B.

Unconverted ASCII (D1-D8) is selected at Parameter or Text Selector and Latch (U56, U62) by Ready For Text Byte Latch U29B on schematic 2B. This is the same signal that clocks U41 and U42.

After being selected, the unconverted ASCII byte is latched into the Parameter or Text Selector and Latch (U56, U62, U63) by a CHANGE DATA signal (schematic 2B). The CHANGE DATA signal causes a negative edge to be produced by Clock Generator U57A on schematic 2B.

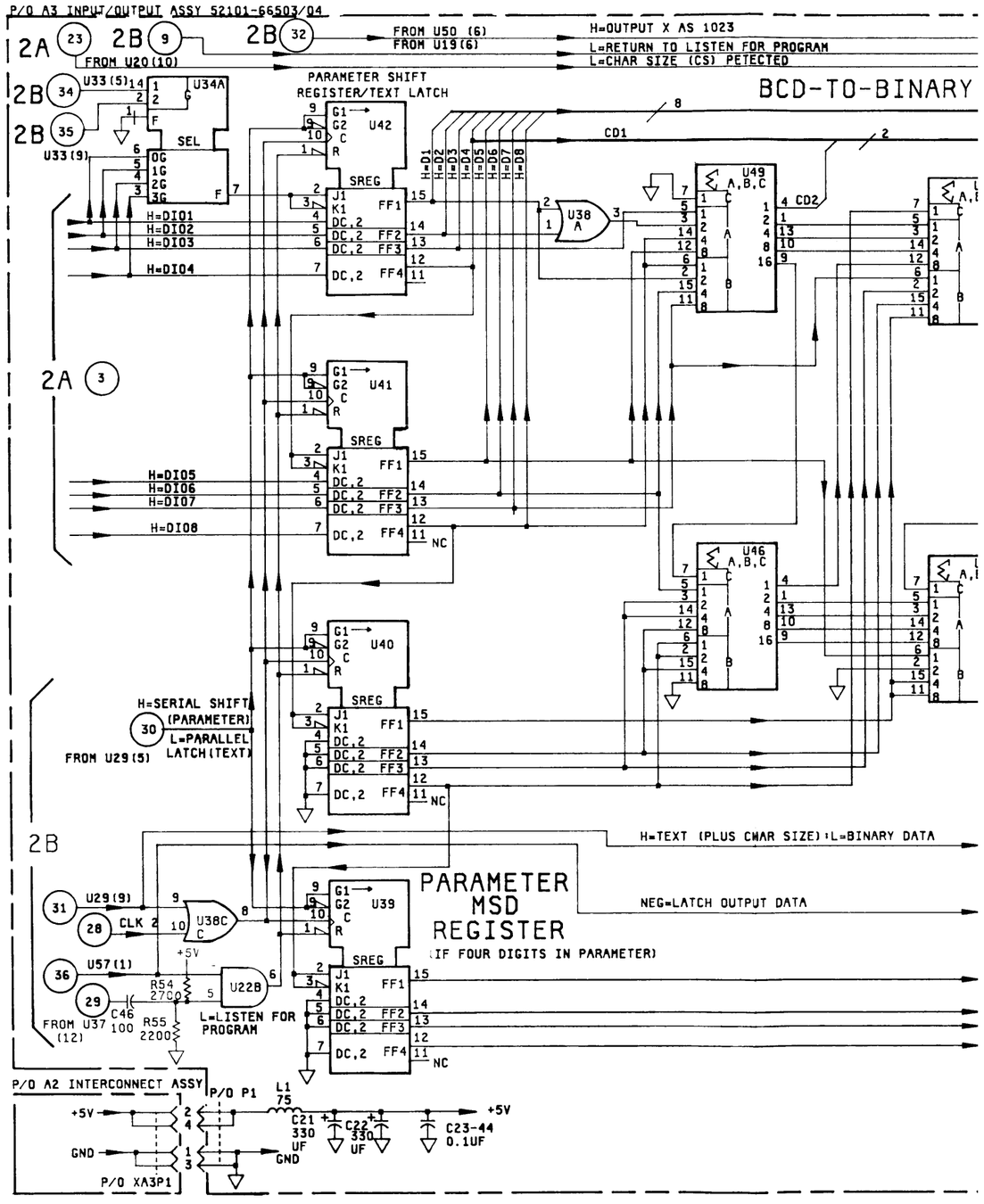
OUTPUT SELECTOR OPERATION IN TEXT MODE.

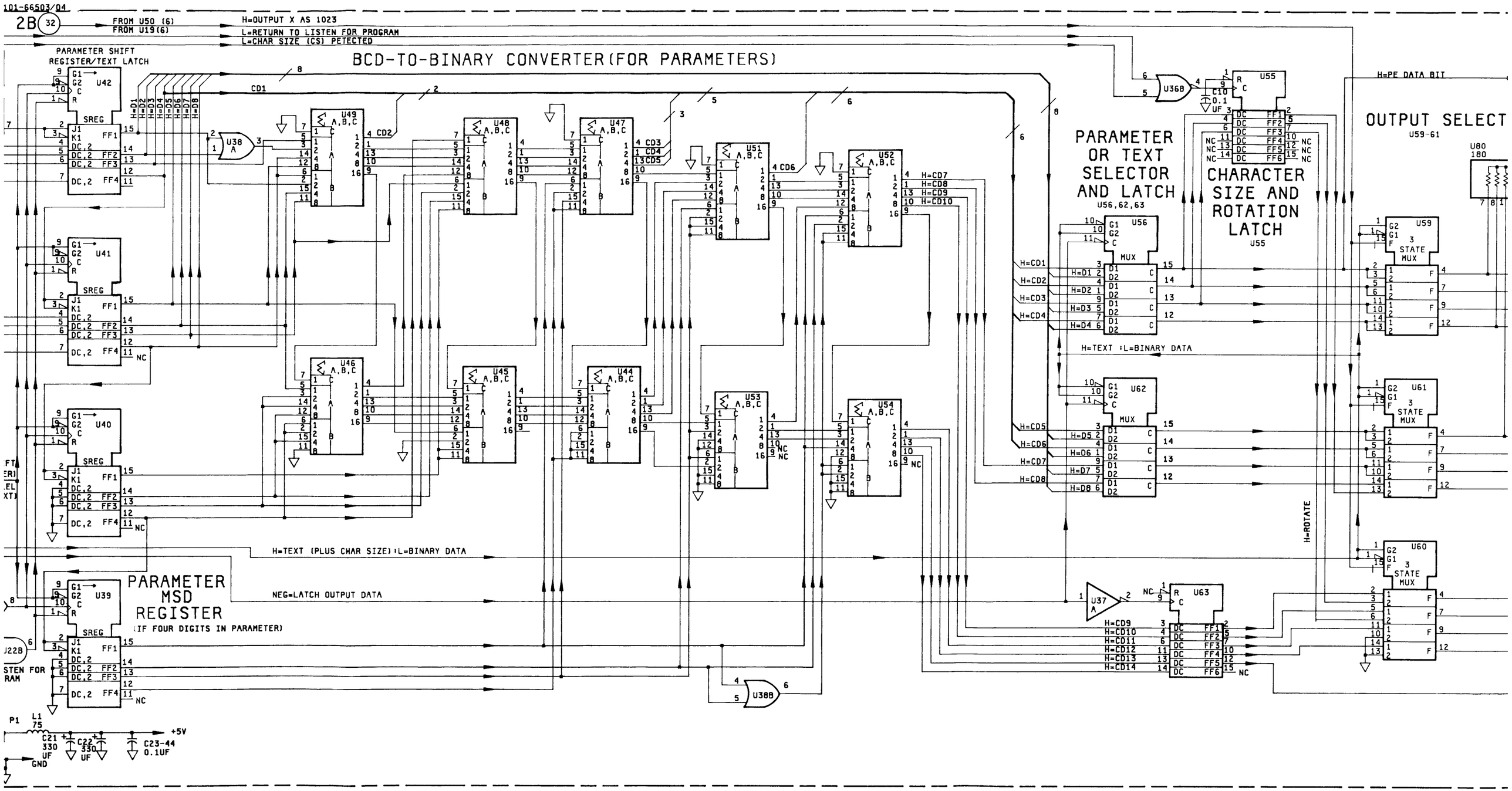
In Text mode, Ready For Text Byte Latch U29B on schematic 2B causes a DO WRITE signal to be sent to the Control Board. After the DO WRITE, the Control Board writes an X value from ID1-ID10 to 1350A memory when A0 is low.

U50B on schematic 2B causes Output Selector U59-U61 to turn off when A0 is low in Text mode. The Output Selector is turned off by setting its "F" (tri-state) inputs high. Since ID1-ID10 are pulled high via U80 and U81, the X value = 1023. This is the text flag.

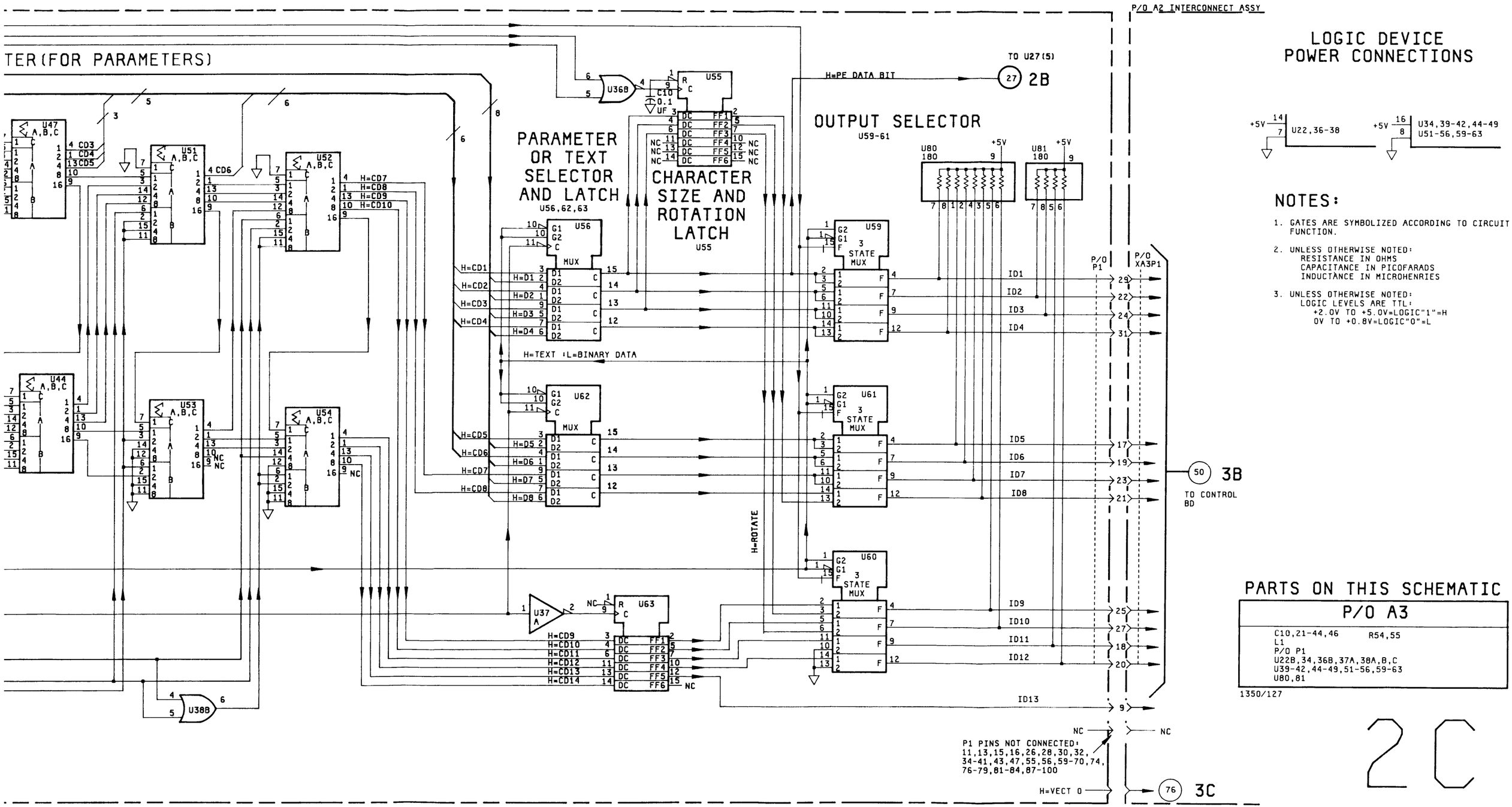
Following a CHANGE DATA signal from the Control Board, a Y value is written to memory when A0 goes high. In this case, the Y value is defined as ASCII plus character size and rotation since the X value was the text flag.

U50B turns the Output Selector back on when A0 goes high. The ASCII character bits from U56 and U62, along with character size and rotation bits from U55, are selected for output on ID1-ID10 by Ready For Text Byte Latch U29B on schematic 2B.


P/O A3 INPUT/OUTPUT ASSY 52101-66503/04
FROM U50 (6)
FROM U19 (6)
FROM U20 (10)
H=OUTPUT X AS 1023
L=RETURN TO LISTEN FOR PROGRAM
L=CHAR SIZE (CS) PETECTED
BCD-TO-BINARY
PARAMETER SHIFT REGISTER/TEXT LATCH
U42
U41
U40
U39
U34A
U33 (5)
U33 (9)
SEL
SREG
H=DI01
H=DI02
H=DI03
H=DI04
H=DI05
H=DI06
H=DI07
H=DI08
CD1
CD2
U38 A
U49 A,B,C
U46 A,B,C
H=SERIAL SHIFT (PARAMETER)
L=PARALLEL LATCH (TEXT)
FROM U29 (5)
H=TEXT (PLUS CHAR SIZE) : L=BINARY DATA
NEG=LATCH OUTPUT DATA
PARAMETER MSD REGISTER
(IF FOUR DIGITS IN PARAMETER)
U29 (9)
CLK
U38C
U57 (1)
U22B
R54 2700
C46 100
R55 2200
FROM U37 (12)
L=LISTEN FOR PROGRAM
P/O A2 INTERCONNECT ASSY
P/O P1
L1 75
C21 330 UF
C22 330 UF
C23-44 0.1UF
+5V
GND
P/O XA3P1



101-66503/04
2B 32
FROM U50 (6)
FROM U19(6)
H=OUTPUT X AS 1023
L=RETURN TO LISTEN FOR PROGRAM
L=CHAR SIZE (CS) PETECTED
PARAMETER SHIFT REGISTER/TEXT LATCH
BCD-TO-BINARY CONVERTER(FOR PARAMETERS)
PARAMETER OR TEXT SELECTOR AND LATCH
U56,62,63
CHARACTER SIZE AND ROTATION LATCH
U55
OUTPUT SELECT
U59-61
H=PE DATA BIT
H=TEXT ;L=BINARY DATA
H=TEXT (PLUS CHAR SIZE);L=BINARY DATA
NEG=LATCH OUTPUT DATA
PARAMETER MSD REGISTER
(IF FOUR DIGITS IN PARAMETER)
H=ROTATE
STATE MUX
+5V
GND



LOGIC DEVICE POWER CONNECTIONS

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A3

C10,21-44,46 R54,55
L1
P/O P1
U22B,34,36B,37A,38A,B,C
U39-42,44-49,51-56,59-63
U80,81

1350/127

2C

Figure 8-16.
Schematic 2C

8-40. SCHEMATIC 2D PRINCIPLES OF OPERATION.

Schematic 2D contains: (1) CLK1 and CLK2 generators; (2) Power Interrupt detector; (3) TTL Blanking and TTL Blinking circuits; and (4) interface circuits for driving an HP 1338A Tri-color Display (AUXILIARY).

8-41. CLK1 AND CLK2 GENERATORS.

CLK1 runs all the time. U31A divides the 24.6 MHz clock from the Display Board down to 12.3 MHz. The 12.3 MHz CLK1 signal provides the reference for Color Valid Delay Generator U70 and for the Handshake Precision Timing Generator on schematic 2A. CLK1 has to be running for the 1350A to receive bytes from HP-IB.

CLK2 runs in four pulse bursts at a rate of 12.3 MHz. U31B produces a CLK2 burst for each parameter byte received from HP-IB via Ready For Data Byte Latch U8A on schematic 2B. CLK2 clocks both the Four State Counter U33 (schematic 2B) and the Parameter Shift Register/Text Latch (schematic 2C) when the 1350A is receiving a parameter byte.

8-42. POWER INTERRUPT DETECTOR.

If a power interruption occurs, the front-panel POWER INTERRUPT LED will be turned on. This indicates a possible deviation from proper 1350A operation. Memory may have been altered or HP-IB instructions may have been misinterpreted.

U68A and Q3 detect interruptions in the +5 V and +12 V power supplies that can occur as a result of line voltage variations. After power-on, U68A Q output is high, turning Q3 on. Q3 collector voltage goes low (Vce approaches 0) to turn on the POWER INTERRUPT LED.

As part of its Initialization program the 1350A should receive an ASCII DC4 character (DC4 = 20) from HP-IB. The DC4 character resets U68A via U14 on schematic 2A. With U68A Q output low, Q3 turns off and the POWER INTERRUPT LED is extinguished.

8-43. TTL BLANKING.

Up to four displays can be driven by the 1350A. These displays can be blanked or unblanked by 16 different combinations of 1350A TTL blanking outputs (DISPLAY 1-4).

The parameter for a Write Auxiliary (WX) instruction determines the TTL blank/unblank combination. The binary value of the WX parameter is inverted on the Display Board and applied to TTL Blanking Latch U67 as PBO3-PBO6 when A0 = high. This blanking information is latched into U67 by the PY signal from the Control Board.

Blanking information from U67 is gated with possible blinking signals and latched into TTL Blanking/Blinking Latch U71. U71 is clocked by U77A. U77A introduces an adjustable delay after the Display Board returns VECTOR BUSY signal high. This delay prevents changes in TTL blanking/blinking outputs while the 1350A is drawing a vector.

U71 outputs are inverted by U74 and applied to AUXILIARY and DISPLAY TTL1-TTL4 rear-panel outputs.

Example:

For a "WX0,:" instruction, the binary value for the parameter is 0000. This is inverted so that PBO3-PBO6 value is 1111. U71 output of 1111 is inverted by U74 so that TTL1-4 output is 0000 (base 2). If four displays are connected, then they will all be unblanked.

8-44. TTL BLINKING.

For WX parameters 8 to 15, Display 4 will always be blanked and Displays 1-3 may be blinked according to settings of Blinking Switch S2. Displays 1-3 are only able to be blinked when unblanked by WX 8-15 combination.

Selected displays (1-3) are blinked at approximately a 4 Hz rate by Blinking Oscillator U78B/U78A. The Blinking Oscillator is started shortly after power-on by a positive edge from U77B. The high level following this positive edge keeps U78A enabled.

U72C output goes low at the 4 Hz rate when enabled by U72D. This 4 Hz signal is gated with selected blanking information to blink displays 1-3 by setting the appropriate TTL outputs high.

8-45. AUXILIARY.

The AUXILIARY connector provides as interface whereby the 1350A can control the color output by an HP 1338A Tri-color Display.

The 1350A must first place the 1338A under Remote control via Auxiliary Remote Enable Latch U76.

Color bits C1 and C2 will now determine the color output of the 1338A. Color codes output by C1 and C2 binary combinations are determined by 1350A file names.

C1 and C2 are latched into Color Bits Latch U65 as File Name bits PBO5 and PBO6. The latching is done by the PX signal from the Control Board.

PX is then delayed approximately 250 ns by Color Valid Delay Generator U70. After this delay U75A produces a positive edge that tells the 1338A that the color code on C1 and C2 is valid.

The 1338A is prevented from changing colors while the 1350A is drawing a vector. After the 1350A has completed a vector, the Display Board returns VECTOR BUSY high. This causes U75D output to go high, releasing the 1338A to change color if necessary.

The 1338A outputs a COLOR BUSY signal when its color change circuits are active. COLOR BUSY prevents the 1350A from outputting a new vector (U72A output = low) until the 1338A is ready.

Table 8-4. Binary Color Code

File Name	Color	C1 = LSB (Pin 7)	C2 = MSB (Pin 8)
0-15	Green	1	1
16-31	Yellow	0	1
32-47	Red	1	0
48-63*	Yellow	0	0

* Files 48-63 not used due to "wrap-around."

P/O A2 | P/O A3 INPUT/OUTPUT ASSY (52101-66503)

4B FROM DISPLAY BD — P/O XA3P1 — P/O P1 — 51 — 45 — L=VECT BUSY — R22 10 — U66B

FROM CONTROL BD 3D — 52 — 86 — P=X — R23 10 — U66D

53 — 80 — P=Y — R24 10 — U66C

4A FROM DISPLAY BD — 54 — 73 PB04 R25 10; 75 PB03 R26 10; 71 PB05 R27 10; 72 PB06 R28 10

COLOR BITS LATCH

U65 A FF; U65 B FF

TTL BLANKING LATCH

U67

H=VECTOR BUSY

L=BLANK TTL 4 AND ENABLE TTL 1-TTL 3 BLINKING

R38-41 ALL 4700 — R38, R41 — U69A, U69B, U69C, U69D

S2 BLINKING

U77A R RETRIG — R42 1000 — R43 100K — C16 10 — BLANKING DELAY ADJ

TTL BLANK/ BLINK LATCH

U71; U75B, U75C, U75D, U74A, U74B, U74C, U74D

H=C1 (LSB); H=C2 (MSB); R46 10; CR3; C19 .1UF

L=VECTOR BUSY; H=TTL2; H=TTL1; H=TTL3; H=TTL4; H=BLANK

BLINKING OSCILLATOR 4HZ

U78B R RETRIG — R33 100K — C13 3.3UF

U78A R RETRIG — R34 100K — C14 3.3UF

R35 100 — C15 .01UF

U72D — U72C

H=OSC START AFTER POWER-ON

AUXILIARY REMOTE ENABLE LATCH

CR2; R44 100K; C17 3.3 UF

U77B R RETRIG — R45 100K — C18 22UF

U76B

R47 2200; R48 2200; U73 B; U72A; R50 10

L=AUX G

U75A

TO U30 (2)

FROM POWER SUPPLY +12V — 50 — VR1 9.09V — C11 0.1UF — R29 470 — U73 E — U73 D

2A — 16 — FROM U14 (10)

L=DC4 (20) =TURN POWER INTERRUPT OFF

R30 1000; R31 1000; CR1; C12 .1UF

U73 A

U68 A FF; U68 B FF

R36 47K — Q3 — 1854-0071 — L=POWER INTERRUPT — R37 180

COLOR VALID DELAY GENERATOR

(250 NS MIN)

U77 AND U78 TRUTH TABLE

INPUTS			OUTPUTS	
RESET	A	B	Q	$\overline{Q}$
0	X	X	0	1
X	1	X	0	1
X	X	0	0	1
1	0	↑	⊓	⊓
1	↓	1	⊓	⊓
↑	0	1	⊓	⊓

4B FROM DISPLAY BD — P/O XA3P1 — P/O P1 — 55 — 50 — 24.6MHZ — R32 10 — U66A — R51 2700 — R52 2200

2B — 33 — FROM U8 (5) — L=READY FOR NEXT DATA BYTE

U31 A FF; U31 B FF — CLK 1 — CLK 2

U70 — U73C

12.3MHZ CLK 1
CLK 2 12.3MHZ BURST

12.3MHZ CLK 1
CLK 2

TO

01-66503)

COLOR BITS LATCH

TTL BLANKING LATCH

TTL BLANK/ BLINK LATCH

BLINKING OSCILLATOR 4HZ

AUXILIARY REMOTE ENABLE LATCH

COLOR VALID DELAY GENERATOR (250 NS MIN)

H=VECTOR BUSY

L=BLANK TTL 4 AND ENABLE TTL 1-TTL 3 BLINKING

S2 BLINKING

BLANKING DELAY ADJ

H=OSC START AFTER POWER-ON

L=DC4(20)=TURN POWER INTERRUPT OFF

L=POWER INTERRUPT

H=C1(LSB)
H=C2(MSB)

L=VECTOR BUSY

H=TTL2

H=TTL1

H=TTL3

H=TTL4
H=BLANK

L=ESR

L=COLOR BUSY

L=1350A VECTOR OUTPUT INHIBIT

L=AUX GO TO REMOTE

P=COLOR VALID

TO U30(2) 2B

P/O J2

AUXILIARY

DISPLAY

TTL 1 J3
TTL 2 J4
TTL 3 J5
TTL 4 J6

P/O A2 INTERCON ASSY

P/O XA3P1 (57)

L=INTERCONNECT HOLDOFF TO CONTROL &DISPLAY BOARDS

POWER INTERRUPT TO FRONT PANEL LED (56) 3,4

P/O P1

TO U32(9)U25(9) (1) 2A

TO U38(10) (28) 2C

TO U33(3) (28) 2B

12.3MHZ CLK 1
CLK 2 12.3MHZ BURST

12.3MHZ CLK 1
CLK 2

U77 AND U78 TRUTH TABLE

INPUTS			OUTPUTS	
RESET	A	B	Q	$\overline{Q}$
0	X	X	0	1
X	1	X	0	1
X	X	0	0	1
1	0	↑	⊓	⊔
1	↓	1	⊓	⊔
↑	0	1	⊓	⊔

LOGIC DEVICE POWER CONNECTIONS

+5V 16 8 U67,70,71 U77,78

+5V 14 7 U31,65,66,68 U69,72-76

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. J1-6 AND HARDWARE IS PART OF A3 I/O ASSY(52101-66501)

BINARY COLOR CODE

FILE NAME	COLOR	C1(LSB) PIN 7	C2(MSB) PIN 8
16-31	YELLOW	0	1
32-47	RED	1	0
48-63*	YELLOW	0	0
0-15	GRN	1	1

*FILES 48-63 NOT USED DUE TO "WRAP AROUND". SEE 1350A OPERATING AND PROGRAMMING MANUAL.

PARTS ON THIS SCHEMATIC

P/O A3

C11-20
J2-6
P/OP1
Q1
S2
U31,65-78
VR1
CR1-3

1350A/126

2D

Figure 8-17. Schematic 2D

8-46. CONTROL BOARD A1 (SERVICE SHEET 3).

8-47. CONTROL BOARD TROUBLESHOOTING.

1. The following procedures provide techniques for checking the function of the program dependent stages on the Control Board. These include all stages except the MEMORY TIMING GENERATOR. It is essentially free running and is best checked by confirming the pulse timing illustrated in the theory accompanying Service Sheet 3D.

2. In the following procedures, the "EM" instruction is used as the primary example for stages that decode many control instructions. By substituting other instructions in the 9825A program statement, other stage conditions may be verified.

NOTE

Viewability of waveforms on the Control Board is enhanced for many stages if the 1350A is put in LINE SYNC mode (rear panel switch) and the oscilloscope is line triggered.

3. Control Instruction Latch and Handshake Check. This verifies the Control Board can receive the Control Instruction "EM" from the I/0 Board. Refer to Service Sheet 3A.

a. Make 9825A entry:

[RESET] wrt718,"EM";jmp0[EXECUTE]

b. Verify low going pulses from U42-8, L=CONTROL BUSY (~16 MSEC wide).

If not present, check U36-3 for low going pulses on N = NONE ERASE OR FIND.

c. Verify low going pulses from U29-11, L = MEMORY and U30-15, L = ERASE.

d. Press 9825A [STOP] key.

4. Frame and File Detect Check. This procedure verifies the EF instruction causes the Frame and File Detect circuit to output the control signals FRAME and FOUND. Refer to Service Sheet 3A.

a. Make 9825A entry:

[RESET] wrt 718,"EN::" [EXECUTE]
wrt 718,"EF0,::";jmp0[EXECUTE]

b. Verify high going pulses on U39-8, U40-12 and low going pulses on U48-3 and U40-6.

c. Press 9825A [STOP] key.

5. Data Gate Check. This procedure verifies an EM instruction zeros the DATA BUS to the Display Memory. Refer to Service Sheet 3B.

a. Make 9825A entry.

[RESET] wrt 718,"EM";jmp0[EXECUTE]

b. Verify low going pulses on U35-11, L = DATA ZERO and on outputs of U28, U27, U26, U17A, and U31C.

c. Press 9825A [STOP] key.

6. Memory Read/Write Controller Check. This procedure verifies that an EM instruction pulls the WRITE DATA and WRITE PBI-6 signals low. Refer to Service Sheet 3B.

a. Make 9825A entry:

[RESET] wrt 718,"EM";jmp0[EXECUTE]

b. Verify U35-6, H = ERASE FILE OR FRAME, goes high (~10MSEC pulse) and that at the outputs of U47 and U51B,C,D there are 1 μsec low going pulses.

c. Press 9825A [STOP] key.

7. Display Parameter Latch and Multiplexer Check. This procedure verifies that file name and TTL blanking data can be latched and multiplexed on the PARA BIT 1-6 lines to the Display Memory. Refer to Service Sheet 3B.

a. Make 9825A entry:

[RESET] wrt 718,"NF31,::"[EXECUTE]

b. Verify the outputs of U32 are all hgih and that the outputs of U33 and U36 are high when A0 is low.

c. Make 9825A entry:

wrt 718,"EN::"[EXECUTE]

d. Verify the outputs of U32 and U33, 36 (when A0 is low) are now all low.

e. In a similar manner to steps a through d, verify the Auxillary Blanking Latch using the instructions WX15 and EX.

8. Memory Mode Controller Check. This procedure verifies the three modes: Read, Write, and Refresh can be entered by the 1350A. Refer to Service Sheet 3C.

a. Make 9825A entry:

[RESET] wrt 718,"PA;";jmp0[EXECUTE]

b. Verify narrow pulses (~2 MSEC period) on U16-6. U16-6 should have many pulses between each write pulse. Also check for negative edges at U18-6.

c. Press 9825A [STOP] key.

d. Verify U16-3 is low and U16-6 has low going pulses ~1.5 μsec wide.

e. Using a piece of wire, jumper between pins 13 and 25 of the auxilary connector (rear panel). Check that the 1350A is in Refresh mode, U16-3 low and U16-6 high.

f. Remove jumper.

9. Vector Generator Controller Check. This procedure verifies the Control Board can generate the signals needed to enable vector data to be output from the Display Memory and the Character Generator.

a. Make 9825A entry:

[RESET] wtb 718,"PE1,::CS3,::TXRRR",3,15,10

b. Verify the complimentary waveforms at U20-8 and U16-11. The three low pulses on U16-11 correspond to the transfer of the coordinates for each "R" from the Character Generator to the Vector Generator.

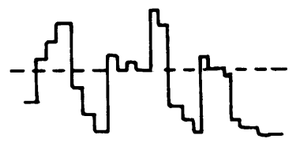
c. Verify the pulses from U3-4 and U3-7. While U20-8 is low, there should be two positive edges produced. While U16D is low, there should be nine positive edges.

10. Z-Axis Output Check. The following steps verify the Z-axis output stages are functional. Refer to Service Sheet 3E.

a. The 1350A should be in the uninitialized (power-on) state. Normally, many random vectors and characters are displayed.

b. Look at the Z-axis output with a scope. Set vertical sensitivity to .5 V/DIV and sweep speed to .2 MSEC/DIV. The waveform may not produce a stable trigger but can be interpreted as follows:

Table 8-5. Z-Axis Output Diagnostics

Waveform Characteristic		Indication - Probable Fault
Complex waveform with excursions above and below 0 VDC Example: Z-output	+1VDC 0VDC -1VDC 	1. Normal Z-axis output.
Waveform entirely below 0VDC, no display image when display is set to normal intensity. Example: Z-output	+1VDC 0VDC -1VDC	1. Z output continuously blanked; Check inputs to Blanking Controller and the BLANK BEAM signal (U60-9). 2. No output from Level Controller Check voltage across R41.
Waveform entirely above 0VDC, no vectors blanked on display. Example: Z-output	+1VDC 0VDC -1VDC	1. Z-axis Blanking Controller not producing BLANK BEAM. Check blanking inputs.

Make 9825A entry:

RESET] wrt 718,"PA;";jmp0[EXECUTE]

Verify narrow pulses (~2 MSEC period) on U16-6. should have many pulses between each write Also check for negative edges at U18-6.

Press 9825A [STOP] key.

Verify U16-3 is low and U16-6 has low going ~1.5 μsec wide.

Using a piece of wire, jumper between pins 13 of the auxilary connector (rear panel). Check that 50A is in Refresh mode, U16-3 low and U16-6 high.

Remove jumper.

Vector Generator Controller Check. This ure verifies the Control Board can generate the s needed to enable vector data to be output from splay Memory and the Character Generator.

a. Make 9825A entry:

[RESET] wtb 718,"PE1,::CS3,::TXRRR",3,15,10

b. Verify the complimentary waveforms at U20-8 and U16-11. The three low pulses on U16-11 correspond to the transfer of the coordinates for each "R" from the Character Generator to the Vector Generator.

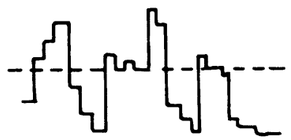
c. Verify the pulses from U3-4 and U3-7. While U20-8 is low, there should be two positive edges produced. While U16D is low, there should be nine positive edges.

10. Z-Axis Output Check. The following steps verify the Z-axis output stages are functional. Refer to Service Sheet 3E.

a. The 1350A should be in the uninitialized (power-on) state. Normally, many random vectors and characters are displayed.

b. Look at the Z-axis output with a scope. Set vertical sensitivity to .5 V/DIV and sweep speed to .2 MSEC/DIV. The waveform may not produce a stable trigger but can be interpreted as follows:

Table 8-5. Z-Axis Output Diagnostics

Waveform Characteristic		Indication - Probable Fault
nplex waveform with ursions above and ow 0 VDC ample: Z-output	+1VDC 0VDC -1VDC 	1. Normal Z-axis output.
veform entirely below DC, no display image en display is set to mal intensity. mple: Z-output	+1VDC 0VDC -1VDC	1. Z output continuously blanked; Check inputs to Blanking Controller and the BLANK BEAM signal (U60-9). 2. No output from Level Controller Check voltage across R41.
veform entirely above DC, no vectors blanked display. mple: Z-output	+1VDC 0VDC -1VDC	1. Z-axis Blanking Controller not producing BLANK BEAM. Check blanking inputs.

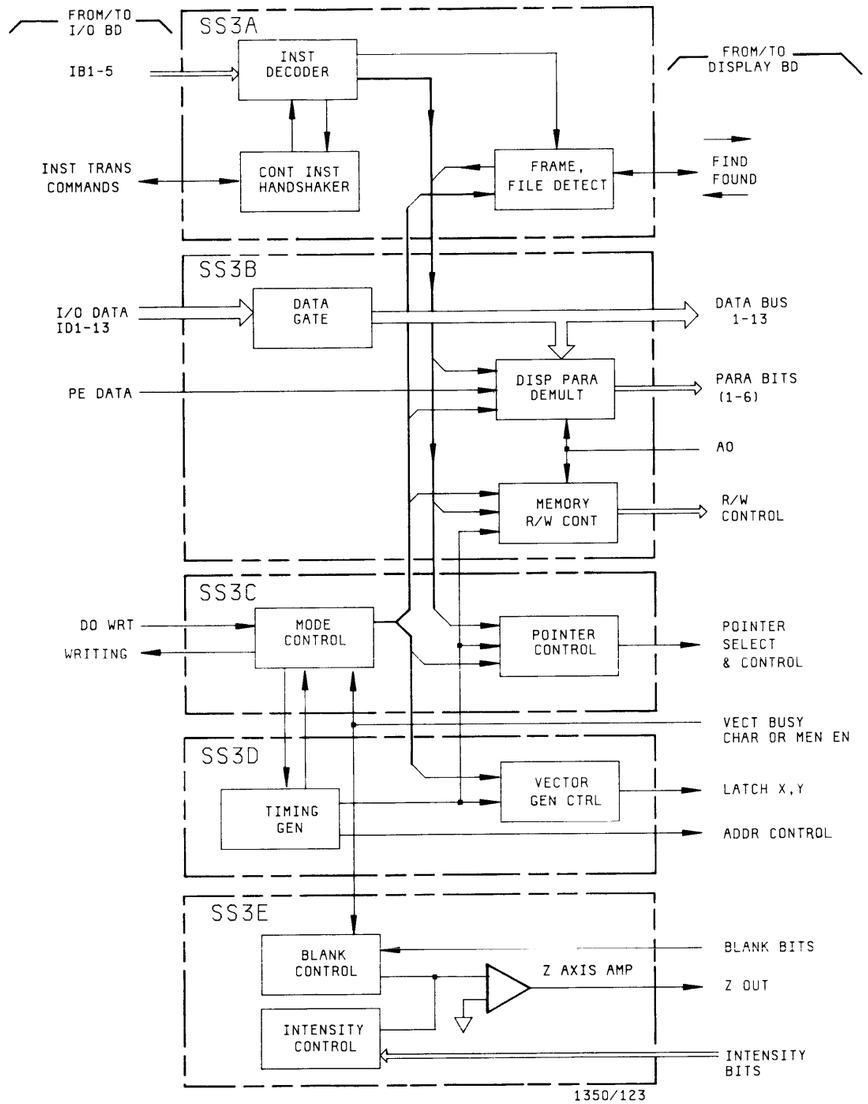


Figure 8-18. Control Board A1 Block Diagram

8-48. GENERAL INFORMATION.

The Control Board Assembly, A1, generates the timing and control signals needed to transfer data into and out of the 1350A Display Memory. The Z-axis output circuitry is also on A1. The simplified block diagram for A1, figure 8-18, shows the major functional stages and their schematic locations. An overview of the Control Board is given in the following paragraphs; circuit details are given adjacent to each schematic.

8-49. OPERATING OVERVIEW.

The Control Board is the memory manager for the 1350A. It clocks data from the Display Memory to the Vector Generator, and, under software control, it inserts, deletes, or modifies data in memory. The following paragraphs provide background information about the memory interface requirements and program inputs to the Control Board.

Memory Organization And Addressing.

The Display Memory is comprised of sixteen 4096 by 1 bit RAMs: ten are used for coordinate or text data and six are used for display parameter data (file names and blanking information). For every X-Y coordinate pair and every text flag/character code pair stored in memory, two successive address locations are used in each of the sixteen RAMs. The first location is the X data byte and is always at an even address. (In other words, the X data byte is always at a location for which the least significant address bit, A0, is low.) The second location is the Y data byte and is always at an odd (A0 high) memory address. Together, the X and Y data bytes form a 32 bit data word, the basic unit of display information. Table 8-6 lists the location of coordinate and text word data in memory.

The Control Board selects one of three possible Display Memory operating modes: DO VECTOR, DO WRITE, or REFRESH.

DO VECTOR is the highest priority mode. In this mode, one word is read, one byte at a time, into the Vector Generator and is translated into the analog waveforms for display. Also, under program control, certain display parameter bits may be modified as they are read.

If the I/O Board receives a PA or TX instruction, it requests the Control Board to perform a DO WRITE operation. In this mode, the Vector Generator is disabled, the Z-axis output is blanked, and the X and Y data bytes of the coordinate or text word are written into memory.

REFRESH is an internal default mode operation. It is used occasionally when the 1350A is in LINE SYNC or when it is plotting large characters. REFRESH insures the RAM refresh rate requirements are satisfied.

In each mode, memory operations are performed on a word by word basis. For every word, a three step memory cycle occurs. First, the X data byte location is addressed. Second, the Y data byte location is addressed. Third, the next X data byte address is generated and stored. After the third step, the Control Board reselects the memory mode and initiates a new mode cycle. The value stored as the next X data byte address is then recalled and becomes the X data byte address in the new cycle. In this way, the 1350A scrolls sequentially through all 2048 word locations; after the last memory address, the process begins again with location 0. Each complete pass through all 2048 word locations is called a frame.

For each mode there is a special memory register in which the next X data byte address is stored. These registers are the Read, Write, and Refresh Pointers. The pointer system allows the Control Board to change from one mode to another, addressing different areas of memory, but still remember the proper location for the next operation in each mode. Furthermore, there are several ways in which the Write Pointer may be loaded with a specific address to enable the programmer to access particular word locations. The pointers are discussed in more detail in the following paragraphs and in the theory accompanying Service Sheet 3C.

Control Instructions.

Of the twenty instructions the 1350A recognizes, four are decoded by the I/O Board and the remaining fourteen, the Control Instructions, are decoded by the Control Board. Table 8-7 summarizes these instructions and their basic characteristics. The I/O Instructions PE and CS latch data bits (on the I/O Board) to be written into memory with PA and/or TX instructions. PA and

Table 8-6. Coordinate and Text Word Data in Memory

Word Addr		Memory Addr	Coord/Text Data (10 Bits)	Disp Para (6 Bits)
1	COORD WORD	0 1	X Data Byte: X Coordinate Y Data Byte: Y Coordinate	File Name Blanking Bits
2	TEXT WORD	2 3	X Data Byte: Text Flag Y Data Byte: ASCII+CS	File Name Blanking Bits

TX enter data into memory by initiating a DO WRITE cycle. Control Instructions are used to perform three basic functions: to latch file name or auxilary blanking data for future DO WRITE operations, to preset a particular address in the Write Pointer, and to modify data already in memory. All Control Instructions are executed during DO VECTOR operations.

The 1350A I/O Board reads Control Instructions from the controller and transfers them in a five bit code to the Control Board. The board to board instruction transfer is a handshake operation which is inhibited while an instruction is being executed.

Table 8-7. Summary of Control Instruction Characteristics

Instruction	Parameter	Circuit Action	Mode
file name/aux			
NF Name File	5 bit (0-31)	latch name, enable wrt	DO WRITE
SN Stop Names	--	disable wrt name	--
WX Write auX	4 bit (0-15)	latch data, enable wrt	DO WRITE
SX Stop auX	--	disable wrt aux	--
blanking bit			
BF Blank File	5 bit (0-31)	for all words in file: wrt blanking bit = 0; if enabled, wrt aux bits	DO VECTOR
UF Unblank File	5 bit (0-31)	for all words in file: wrt blanking bit = 1; if enabled, wrt aux bits	DO VECTOR
BM Blank Memory	--	for all words in memory: wrt blanking bit = 0; if enabled, wrt aux bits	DO VECTOR
UM Unblank Memory	--	for all words in memory: wrt blanking bit = 1; if enabled, wrt aux bits	DO VECTOR
pointer			
FF Find File	5 bit (0-31)	load Write Pointer with first address of file	--
FL Find Location	11 bit (0-2047)	load Write Pointer with specified address	--
erase			
EF Erase File	5 bit (0-31)	for all words if file: wrt COORD/TEXT bits = 0; load addr 0 into Wrt Ptr	DO VECTOR
EN Erase Names	--	for all words in memory: wrt file name = 0	DO VECTOR
EM Erase Memory	--	load addr 0 into Wrt Ptr for all words in memory: wrt COORD/TEXT bits = 0; load addr 0 into Wrt Ptr; wrt Pen Enable bits=0	DO VECTOR
EX Erase auX	--	for all words in memory: wrt aux bits = 0 load addr 0 into Wrt Ptr	DO VECTOR

Some Control Instructions require bits of parameter data to accompany them. These data are transferred from the I/O Board on the ID1-13 data bus and latched on the Control Board or stored in the Display Memory depending on the instruction.

The Control Instructions divide into four basic groups: file name/auxilary bit control, blanking bit control, pointer control, and erase control instructions. Each group has a different pattern of execution.

File name/auxilary Control. The WX, NF, SX, and SN commands are all immediately executed; they simply latch data and/or toggle write enable flip-flops.

Blanking Bit Control. To execute BF, UF, BM, nd UM the memory must first be cycled to word address 0 in the DO VECTOR mode. Then during the next frame the blanking bit modification takes place. BF and UF rewrite the blanking bits in the display parameter portion of the Y Data Byte of all words in the specified file. BM and UM rewrite the blanking bits of all words in memory. Execution is complete when the last word of the frame has been addressed. If write aux is enabled (i.e., if WX is sent and then SX is not sent), the auxilary blanking data will be written into all words modified by the blanking instruction.

Pointer Control. FF and FL are executed after an addres is loaded into the Write Pointer. FF requires cycling to address 0, and then on until the first word in the specified file is found. Execution is completed during the next DO VECTOR cycle when the address of this word is loaded into the Write Pointer. FL loads the address specified in program into the Write Pointer during the next DO VECTOR cycle.

Erase Control. EF, EN, EM, and EX all require a complete frame, starting with address 0, and then complete their execution during the first word of the next frame. These instructions each erase a portion of the word data from memory and then enter address 0 into the Write Pointer.

8-50. SCHEMATIC 3A PRINCIPLES OF OPERATION (CONTROL SIGNAL GENERATOR).

8-51. INTRODUCTION.

Schematic 3A covers three stages on the Control Board:

Instruction Latch and Decoder
Control Instruction Handshaker
Frame and File Detector

The Instruction Latch and Decoder latches Control Instructions from the I/O Board and decodes them into board level control signals. The Control Instruction Handshaker controls the transfer of Control Instructions from the I/O Board to the Control Board. The Frame and File Detector interfaces with circuits in the Display Memory (on A4) to generate the signals which gate frame or file dependent instruction execution. These stages generate 14 signals which comprise the Control Instruction Bus.

8-52. CONTROL INSTRUCTION LATCH AND DECODER.

After the I/O Board receives a Control Instruction, it transfers it to the Control Board with the positive edge of LATCH INSTRUCTION CLK. This latches the five bit code from I1-5 into U25. When the Control Instruction Handshaker generates CONTROL BUSY low, U29B and U30 are enables to decode the instruction. For each instruction there are two bits, one from each decoder, that are active (low). Table 8-8 lists the Control Instructions, their code on I1-5, and the corresponding decoded outputs.

Note that the outputs from U29B designate which data bits are involved in the Control Instruction operation and the outputs from U30 designate what kind of operation is to take place. The two bits of each instruction can act singly and/or together, depending on the instruction, to select the required control functions in subsequent stages.

Table 8-8. Control Instructions, I1-5 Codes, and Decoded Control Instruction Bus Signals

Program Instruction		Code On I1-5 I1	I2	I3	I4	I5	Decoder U29B	Outputs U30
NF	Name File	1	1	1	0	0	FILE	NAME
SN	Stop Names	0	1	0	1	0	NAMES	STOP
WX	Write auX	0	0	1	0	1	AUX	WRITE
SX	Stop auX	0	0	0	1	0	AUX	STOP
BF	Blank File	1	1	0	1	1	FILE	BLANK
UF	Unblank File	1	1	1	1	0	FILE	UNBLANK
BM	Blank Memory	1	0	0	0	1	MEMORY	BLANK
UM	Unblank Memory	1	0	1	1	0	MEMORY	UNBLANK
FF	Find File	1	1	0	1	1	FILE	FIND
FL	Find Location	0	1	0	1	1	NAMES	FIND
EF	Erase File	1	1	0	0	0	FILE	ERASE
EN	Erase Names	0	1	0	0	0	NAMES	ERASE
EM	Erase Memory	1	0	0	0	0	MEMORY	ERASE
EX	Erase auX	0	0	0	0	0	AUX	ERASE

8-53. CONTROL INSTRUCTION HANDSHAKER.

Control Instructions are transferred from the I/O Board to the Control Board via a handshake operation. The four signals used in the handshake are: CONTROL INSTRUCTION, LATCH INSTRUCTION, CONTROL GET BUSY, and CONTROL BUSY. Figure 8-19 illustrates the sequence in which they occur.

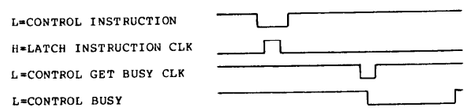


Figure 8-19. Control Instruction Handshake Timing

The handshake circuit remains in the "busy" state until U36 detects a low pulse at any of its inputs. Any low input will reset U42A and return CONTROL BUSY high. The I/O Board is then enabled to issue a new Control Instruction. There are four different sequences which lead to the resetting of U42A:

U36-1, 2, and 6 sense completion of the immediate execute instructions NF, SN, WX, and SX. Note: both SN and SX are detected when U30 decodes (L=) STOP.

U36-12 detects execution of BF, UF, BM, and UM on the positive transition of FRAME (at U45-9). This transition signals the end of the frame during which the blanking bit modification occurs.

U36-3 detects execution of FF, FL, EF, EN, EM, and EX when DONE ERASE OR FIND is pulled low by the Memory Pointer Controller (Service Sheet 3C). This negative transition is the trailing edge of the pulse that loads the Write Pointer, the last step in execution of these instructions.

U36-11 detects RESET from the I/O Board. RESET low clears out any Control Instruction being executed. Thus, it will pull the 1350A "out of the weeds" if it is trying to execute an invalid program statement that is read as a Control Instruction.

8-54. FRAME AND FILE DETECTOR.

The Frame and File Detector is enabled by any Control Instruction that generates BLANK, UNBLANK, FIND, or ERASE low. Any of these signals generates FIND FILE high. This enables U40A to be toggled and latches a new file name into the File Name Comparator on A4 (although the comparator output is only used for the file dependent commands FF, EF, BF, and UF).

When the Display Memory is addressing the Y Data Byte of the last word in memory (word address 2047), it outputs LAST ADDRESS high. U39A clocks U40A on the falling edge of LAST ADDRESS and FRAME goes low. When execution of the instruction is complete, U40A is reset.

The toggling of U40A also enables U40B to sense the File Name Comparator output, FILE FOUND, as each next X data byte is addressed. If the next word to be addressed in DO VECTOR mode is in the program specified file, then U48A outputs FOUND low.

Figure 8-20 illustrates typical Frame and File Detector waveforms.

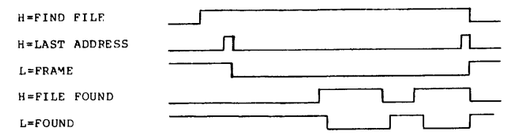
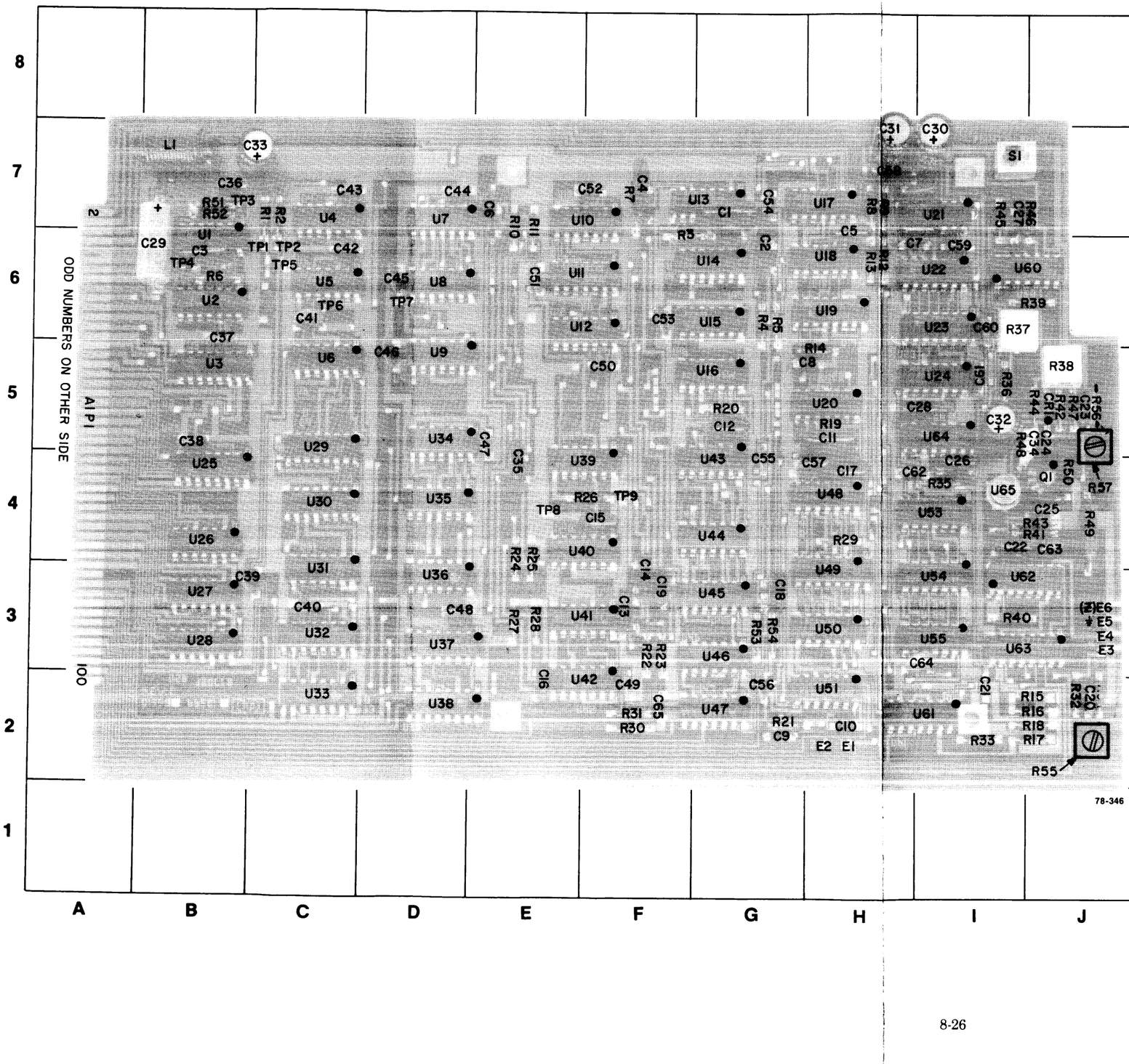


Figure 8-20. Typical Frame and File Detector Response to BF



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	G-7	C41	C-6	R7	F-7	R48	I-5	U21	I-7
C2	G-6	C42	C-6	R8	H-7	R49	J-4	U22	I-6
C3	B-6	C43	C-7	R9	H-7	R50	J-4	U23	I-6
C4	F-7	C44	D-7	R10	E-7	R51	B-7	U24	I-5
C5	H-7	C45	D-6	R11	E-7	R52	B-7	U25	B-4
C6	E-7	C46	D-5	R12	H-6	R53	G-3	U26	B-4
C7	I-6	C47	E-5	R13	H-6	R54	G-3	U27	B-3
C8	H-5	C48	D-3	R14	H-5	R55	J-2	U28	B-3
C9	G-2	C49	F-2	R15	J-2	R56	J-5	U29	C-5
C10	H-2	C50	F-5	R16	J-2	R57	J-5	U30	C-4
C11	H-5	C51	E-6	R17	J-2	S1	I-7	U31	C-4
C12	G-5	C52	F-7	R18	J-2	TP1	C-6	U32	C-3
C13	F-3	C53	F-6	R19	H-5	TP2	C-6	U33	C-2
C14	F-3	C54	G-7	R20	G-5	TP3	B-7	U34	D-5
C15	F-4	C55	G-4	R21	G-2	TP4	B-6	U35	D-4
C16	E-2	C56	G-2	R22	F-3	TP5	C-6	U36	D-3
C17	H-4	C57	H-4	R23	F-3	TP6	C-6	U37	D-3
C18	G-3	C58	H-7	R24	E-4	TP7	D-6	U38	D-2
C19	F-3	C59	I-6	R25	E-4	TP8	E-4	U39	F-4
C20	J-2	C60	I-6	R26	F-4	TP9	F-4	U40	F-4
C21	I-2	C61	I-5	R27	E-3	U1	B-6	U41	F-3
C22	I-4	C62	I-4	R28	E-3	U2	B-6	U42	F-2
C23	J-5	C63	J-4	R29	H-4	U3	B-5	U43	G-4
C24	J-5	C64	I-3	R30	F-2	U4	C-7	U44	G-4
C25	J-4	C65	F-2	R31	F-2	U5	C-6	U45	G-3
C26	I-4	CR1	J-5	R32	J-2	U6	C-5	U46	G-3
C27	I-7	E1	H-2	R33	I-2	U7	D-7	U47	G-2
C28	I-5	E2	H-2	R35	I-4	U8	D-6	U48	H-4
C29	B-6	E3	J-3	R36	I-5	U9	D-5	U49	H-4
C30	I-7	E4	J-3	R37	I-6	U10	F-7	U50	H-3
C31	H-7	E5	J-3	R38	J-5	U11	F-6	U51	H-2
C32	I-5	E6	J-3	R39	J-6	U12	F-6	U53	I-4
C33	B-7	L1	B-7	R40	I-3	U13	G-7	U54	I-3
C34	J-5	Q1	J-4	R41	J-4	U14	G-6	U55	I-3
C35	E-4	R1	C-7	R42	J-5	U15	G-6	U60	J-6
C36	B-7	R2	C-7	R43	J-4	U16	G-5	U61	I-2
C37	B-6	R3	F-6	R44	J-5	U17	H-7	U62	J-3
C38	B-5	R4	G-6	R45	I-7	U18	H-6	U63	J-3
C39	B-3	R5	G-6	R46	J-7	U19	H-6	U64	I-5
C40	C-3	R6	B-6	R47	J-5	U20	H-5	U65	I-4

Figure 8-21. Control Board A1 Component Locator

Mnemonics on Control Board A1

A0 — Memory Address Bit 0 — Serves important functions on both the Display and Control Boards. It is used on the Display Board to determine when x or y information is being read or written. It determines the configuration of RAM for storage. On the Control Board it is a multiplex select line to determine whether File Name bits or Blanking bits are sent to memory. During x-time (A0 = low) File Names are selected and during y-time (A0 = high) Blanking information is selected. When selecting which type of data, A0 also determines the read/write status of the memories by means of the Memory Read/ Write Controller.

D1-D13 — Data Bits 1-12 transfer data lines between the Control Board and Pointer Address Multiplexer. D13 is not used.

H = FILE FOUND — File name information from the data lines is compared with those stored in the Parameter Memories. When a match occurs, H = FILE FOUND goes high.

I1-I5 — Control instruction bus - used for internal instrument control utilizing information decoded from the HP-IB bus.

ID1-ID12 — Input Data bus - after data from the HP-IB bus is buffered and latched, it is decoded for parameters (BLANK, UNBLANK, PEN ENABLE, etc.), multiplexed, gated and becomes the data bus D1-D12. ID13 is not used.

L = BLANK CHAR — Blanks the beam between characters. Drives the Z-axis Blanking Controller.

L = BLANK VECTOR — Blanks the vector beam between non-connected points.

L = CHAR — Selects P = CHAR LATCH X and P = CHAR LATCH Y through Vector Generator Controller U3 (Schematic 3D) and causes these signals to transfer each stroke to the Vector Generator. Low only when the data is text, as controlled by the Character Generator.

L = CHAR HOLDOFF — Swings low after a character is detected to allow time for the text code to be decoded. Prevents any output from the Character Generator.

L = CHAR OUTPUT ENABLE — After L = CHAR has occurred there is a delay provided by the C12 - U16D combination (schematic 3D). This allows time for text data to be latched to the Character Generator and decoded (L = CHAR HOLDOFF helps in this latter function). The low level of L = CHAR OUTPUT ENABLE enables the character output selectors U12, 13, 14 and 26 (schematic 5) and causes the character data to be sent to the Vector Generator.

L = CONTROL BUSY — Inhibits further control instruction exectuion when low. Low only when instructions are being carried out.

L = CONTROL INST — Goes low when control instructions have been received and decoded and stays low until instructions have been completed and the Control Instruction Handshaker has reset CONTROL BUSY to a logic high.

L = DO WRITE — A low level allows information to be written into memory - low only when data is being transferred to memory.

L = INTERFACE HOLDOFF — Inhibits further vector generation until the 1338A display can assimilate the data it has. Low inhibits, high continues.

L = LOAD ADDR — Active low loads pointer address into memory.

L = MEM CHIP ENABLE — Enables U26 Memory Chip Enable Drive (Schematic 4A) which allows Parameter Memory and Vector Memory RAMs to load data.

L = MEM OUTPUT ENABLE — Enables memory output drivers U29 and U30 (schematic 4A). This is the all encompassing write line which enables both Parameter and Vector Memories.

L = RESET — Momentarily low when instrument is powered on or a new program is to be initiated. Resets 17B and U23A.

L = VECTOR BUSY — Indicates that data is being translated into analog form in the D/A Converter. When high, the Vector Generator is processing available values and has not sent them to the D/A.

L = VECTOR INHIBIT — Holds the Vector Generator in a reset condition in which it cannot process or output data.

L = WRITE DATA — Write enable for the Vector Memory RAMs. Enables only the Vector Memories.

L = WRITE PB1-PB6 — Write Display Parameter Bits — Write enables lines for only the Parameter Memories — can be used to write to individual memories depending on requirements.

L = WRITING — Generated from the DO WRITE command, this signal along with L = WRITE ENABLE, is used to create the L = WRITE DATA signal and to enable the WRITE PB1-PB6 lines.

LINE SYNC — This signal, generated on the Power Supply board, is used to signal the start of the next frame. Sync rate is 120 Hz.

N = CHANGE DATA — This negative transition signals the I/O board that the first byte of data (x-coordinates) has been written and it is ready for the second byte (y-coordinates).

N = CLR ADDR — Negative transition clears all memory address counters.

N = CONTROL GET BUSY — Negative transition clocks U42A via U411 (schematic 3A) to initiate the "Control Busy" sequence.

N = LATCH INST — Negative transition causes control instructions to be latched into the Instruction Latch, U25. It also allows L = CONTROL INST to be clocked to the output of U42B, disabling the CONTROL INSTRUCTION HANDSHAKER (all on Schematic 3A). This ensures that no new control instructions are latched in until the current instructions have been executed.

N = LOAD ADDR CTR — Causes the address value from the pointer register to be transferred to the Memory Address Counter.

N = MEMORY CLK — Clock for the Memory Address Counters.

N = STORE POINTER ADDR — Stores the next x address.

P = CHAR LATCH X — Latches each Char Stroke to the Vector Generator (x).

P = CHAR LATCH Y — Latches each Char Stroke to the Vector Generator (y).

P = FIND FILE — Frame and File Detector (schematic 3A) is enabled by any of the control instructions that state BLANK, ERASE, UNBLANK, or FIND. This causes a new file name to be latched into the File Name Comparator.

P = LATCH X — Clocks the x data into the Vector Generator.

P = LATCH Y — Clocks the y data into the Vector Generator.

P = X ADDR — Used to latch File Name Bits PBO5 and 6 into Color Bits Latch U65A. Also used to generate Color Valid Signal for 1338A Tri-color Display.

P = Y ADDR — Inverted and used as clock for TTL Blanking Latch U67. This latches information from File Name Bits PBO3-6 to determine which of 4 TTL outputs will be high (blanked).

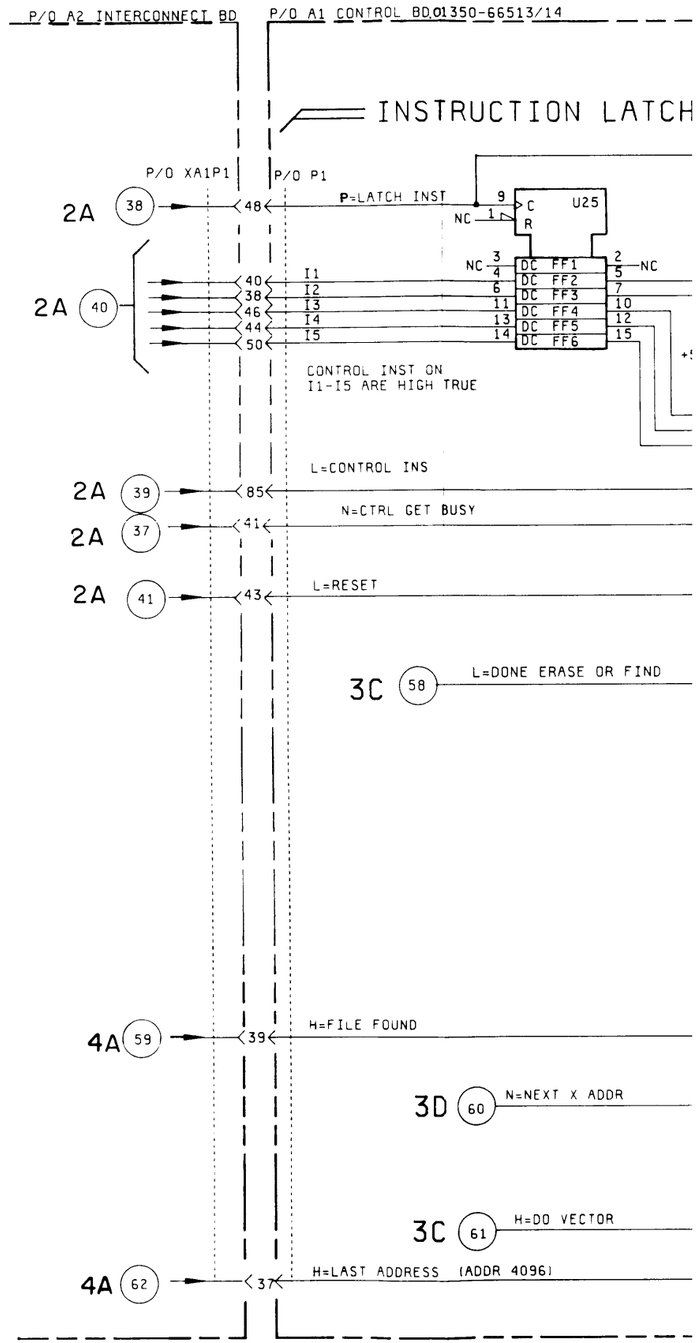
PARA BITS 1-6 — Parameter Bits - carries parameter information to the Parameter Memories. A0 determines the contents. When A0 = low (x-time) the Para Bits carry File Name data. When A0 = high (y-time) they carry "Pen Enable," "File Blanking," and "Auxiliary Bits."

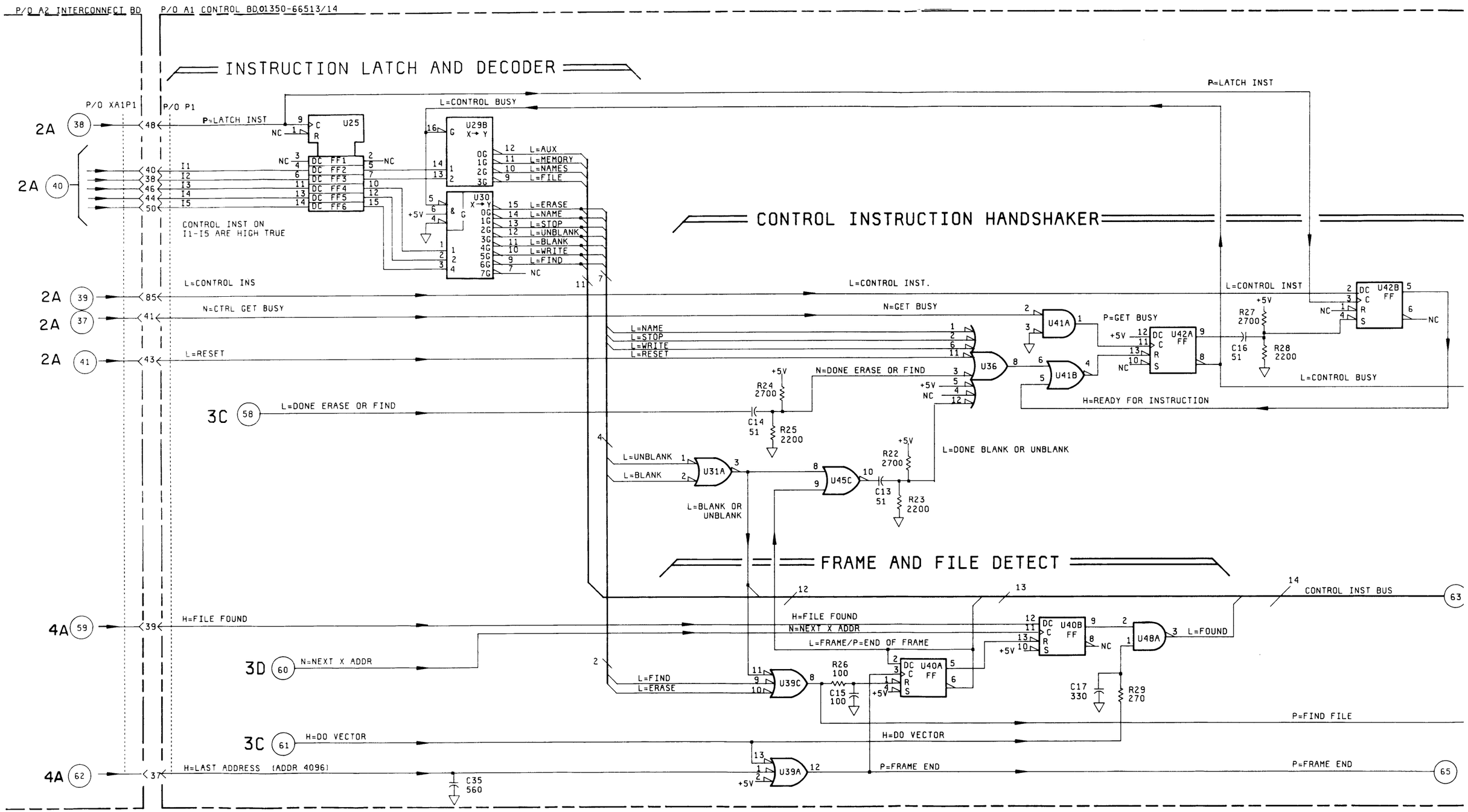
PBO1-PBO5 — Name Bits — See Section 8 - 1350 Memory Organization, for more complete explanation.

PE BIT — Pen Enable Bit — tells the 1350A to blank or unblank when drawing a character or vector. 1 = unblanked (pen down), 0 = blanked (pen up). It is sent as a parameter in the y byte.

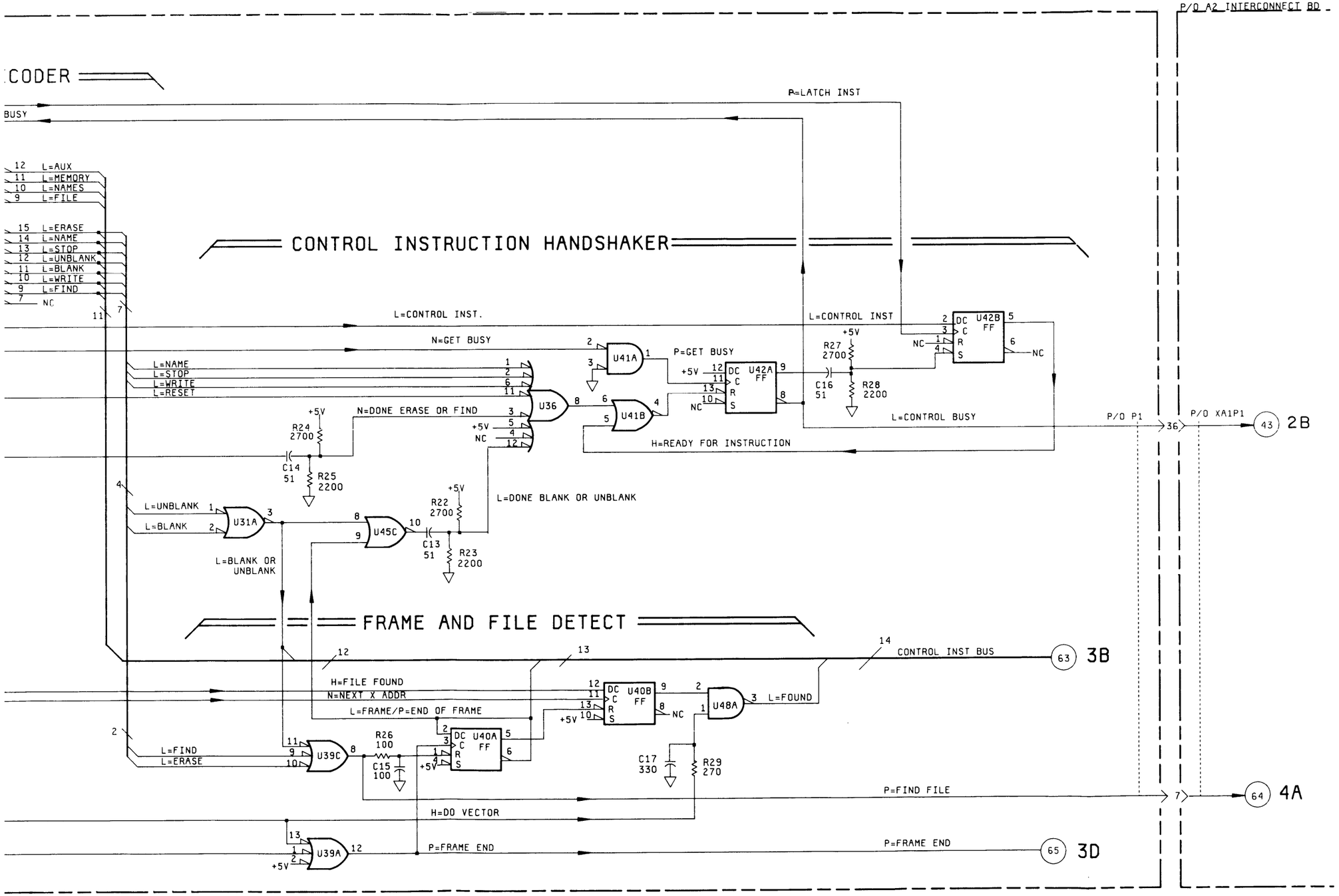
POINTER SEL 1&2 — Generated from DO VECTOR, WRITING and STORE WRITE POINTER. These are the address lines to the four bit pointer register stack in Display Memory (U18, U21, and U24 on schematic 4A).

Z0-Z4 — Blanking Level Bits - carries information on the intensity of the vectors to the z-axis Level Controller.





P/O A2 INTERCONNECT BD
P/O A1 CONTROL BD,01350-66513/14
INSTRUCTION LATCH AND DECODER
CONTROL INSTRUCTION HANDSHAKER
FRAME AND FILE DETECT
P/O XA1P1
P/O P1
P=LATCH INST
L=CONTROL BUSY
L=AUX
L=MEMORY
L=NAMES
L=FILE
L=ERASE
L=NAME
L=STOP
L=UNBLANK
L=BLANK
L=WRITE
L=FIND
CONTROL INST ON
I1-I5 ARE HIGH TRUE
L=CONTROL INS
N=CTRL GET BUSY
L=RESET
L=DONE ERASE OR FIND
L=CONTROL INST.
N=GET BUSY
P=GET BUSY
N=DONE ERASE OR FIND
H=READY FOR INSTRUCTION
L=DONE BLANK OR UNBLANK
L=BLANK OR UNBLANK
H=FILE FOUND
N=NEXT X ADDR
L=FRAME/P=END OF FRAME
L=FOUND
CONTROL INST BUS
P=FIND FILE
H=DO VECTOR
H=LAST ADDRESS (ADDR 4096)
P=FRAME END



LOGIC DEVICE POWER CONNECTIONS:

+5V — 14 — U31,36,39-42, U45,48 — 7

+5V — 16 — U25,29,30 — 8

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE INDICATED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

PART OF A1 CONTROL BD

C13-17,35 P/OP1	R22-29 U25,29B,30,31A	U36,39A,39C,40 U41A,41B,42,45C U48A

1350/106

3A

Figure 8-22. Schematic 3A

8-55. SCHEMATIC 3B PRINCIPLES OF OPERATION (DATA INPUT CONTROL).

8-56. INTRODUCTION.

Schematic 3B covers three functional stages on the Control Board:

Data Gate
Display Parameter Latch and Multiplexer
Memory Read/Write Controller

The Data Gate buffers data lines ID1-13 and switches them all low during ERASE operations. The Display Parameter Latch stores X and Y byte parameter data to be written into memory. The Display Parameter Multiplexer alternately outputs the X and Y byte parameter data on PB1-6 as each X and Y address is generated. The Memory Read/Write Controller enables the appropriate RAMs in the Display Memory to accept data during DO WRITE or Control Instruction executions.

8-57. DATA GATE.

The Data Gate consists of U17A, U26, U27, and U28. It is always enabled except during an EF or EM execution. These two instructions are detected by U31B, U35C and U35D. EF or EM operations pull DATA ZERO low and cause the Data Gate to output all zeros. The erasure is then accomplished by writing these zeros over the coordinate or text data in the specified file or in the entire memory. The Table 8-9 summarizes the data on the INPUT DATA lines, ID1-13, and DATA lines, D1-13, during execution of Control Instructions.

8-58. DISPLAY PARAMETER LATCH AND MULTIPLEXER.

The Display Parameter Latch consists of U31C, U49A, U48C, U32, U48D, and U37. Under program control, these chips store parameter data to be written into memory except the PEN ENABLE (PE) bit, which is stored on the I/O Board.

The PE bit data is gated by U31C with DATA ZERO. DATA ZERO is low during all ERASE operations; for each word addressed in EM or EF executions, the PE bit is also erased (written=0).

The BLANKING bit is latched by U49A. If UNBLANK or ERASE NAMES is decoded, UNBLANK FILE (U49-4) toggles high. A BLANK (FILE or MEMORY) instruction resets U49A and pulls UNBLANK FILE low.

File names are latched by U32 from D1-5 when NAME is decoded. EN gated by FRAME clears U32.

Auxillary blanking bits are latched by U37 from D1-4 when WRITE is decoded. AUX gated by FRAME clears the data from U37.

The selectors, U33 and U38, are driven by the A0 line of the MEMORY ADDRESS BUS (from the Display Memory). For A0 low (all even addresses), FILE NAME BIT 1-6 are passed through to the Display Memory on PARAMETER BIT 1-6. For A0 high; PE, UNBLANK FILE, and AUX BLANKING BIT 1-4 are passed onto PARAMETER BIT 1-6. Table 8-10 lists the data on each of the PARAMETER BIT lines during X and Y addressing periods.

Table 8-9. Data on DATA Lines During Control Instructions

Control Instruction		Data Line	Content
NF	Name File	D1-5	5 bit file name (0-31)
SN	Stop Names	----	
WX	Write auX	D1-4	4 bit aux blanking code (0-15)
SX	Stop auX	----	
BF	Blank File	D1-5	5 bit file name (0-31)
UF	Unblank File	D1-5	5 bit file name (0-31)
BM	Blank Memory	----	
UM	Unblank Memory	----	
FF	Find File	D1-5 5	bit file name (0-31)
FL	Find Location	D1-11	11 bit word address (0-2047)
EF	Erase File	D1-5	5 bit file name (0-31)
EN	Erase Names	----	
EM	Erase Memory	----	
EX	Erase auX	----	

Table 8-10. Data on PARAMETER BIT 1-6 During X and Y Data Byte Addresses

Parameter Bit	A0 Low (X Byte Address)	A0 High (Y Byte Address)
1	FILE NAME BIT 1	PEN ENABLE BIT
2	FILE NAME BIT 2	FILE BLANKING BIT
3	FILE NAME BIT 3	AUX BLANKING BIT 1
4	FILE NAME BIT 4	AUX BLANKING BIT 2
5	FILE NAME BIT 5	AUX BLANKING BIT 3
6	- NOT USED -	AUX BLANKING BIT 4

8-59. MEMORY READ/WRITE CONTROLLER.

For every modification of memory content performed in the 1350A, the Memory Read/Write Controller (R/W Controller) must enable the required RAMs to accept the data. To perform this selection, the R/W Controller needs the following data: the mode of memory operation, whether the location addressed is to be modified, and the functions to be executed.

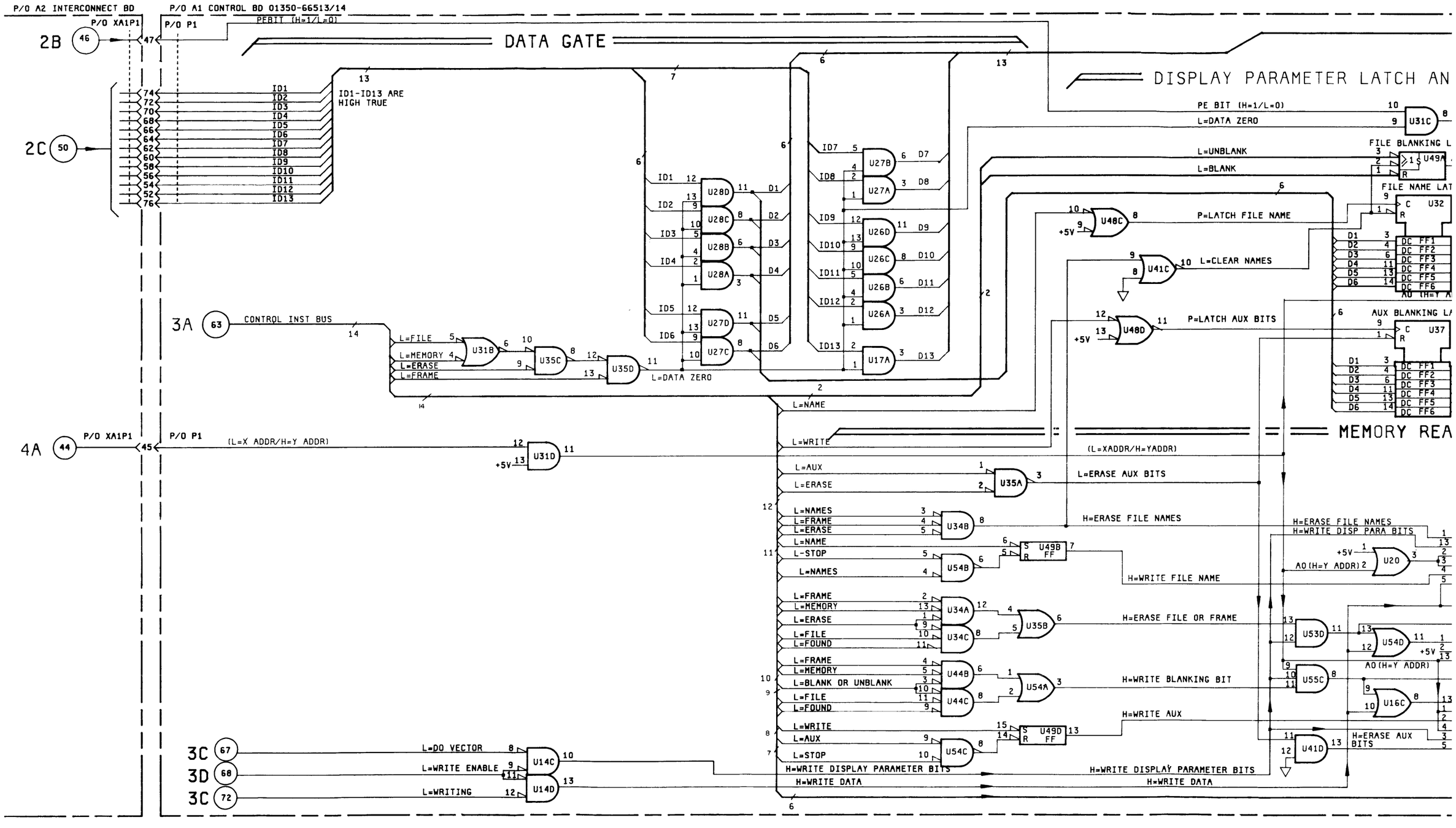
The mode information, either DO VECTOR or WRITING low, comes through U14C and U14D. The gating signal, WRITE ENABLE, is low only while the X and Y data bytes are addressed (not when the next X data byte is addressed). The resulting signals, WRITE DATA and WRITE DISPLAY PARAMETER BITS, enable the write functions in each respective mode. For instance, WRITE DATA high enables WRITE AUX BITS (U16C, U46A), WRITE PE BIT (U54D,U55A), WRITE FILE NAME (U50B), and directly drives U47A to produce WRITE DATA low.

The qualification of whether an address is to be modified is made by the A0 line and the control signals, FRAME and FOUND.

A0 distinguishes between X and Y Data Bytes. When A0 is low, write operations involving the X Data Byte (file dependent operations) are enabled. When A0 is high, Y data byte write operations (blanking or auxillary) are enabled.

FRAME and FOUND (from the Frame and File Detector on Service Sheet 3A) gate MEMORY and FILE operations respectively. FRAME gates EN, EM, EX, BM, and UM (U35A, U34B, U34A, U44B) to begin the execution of these instructions with address 0. FOUND, which is also gated by FRAME, gates EF, BF, and UF (U34C, U44C). FOUND indicates the word addressed is in the program specified file.

When a Control Instruction is decoded, the resultant control signals define which RAMs data is written into. For example, U34B goes high after EN is decoded, when the next frame (FRAME low) begins. Then ERASE FILE NAMES high goes through U50 when enabled by A0 low and WRITE DISPLAY PARAMETER BITS high. WRITE OR ERASE FILE NAME high, then pulls WRITE PB1-6 low and writes the data from the PARAMETER BIT 1-6 into the current address location.


P/O A2 INTERCONNECT BD
P/O A1 CONTROL BD 01350-66513/14
P/O XA1P1
P/O P1
PEBIT (H=1/L=0)
DATA GATE
2B
46
47
2C
50
ID1
ID2
ID3
ID4
ID5
ID6
ID7
ID8
ID9
ID10
ID11
ID12
ID13
ID1-ID13 ARE HIGH TRUE
3A
63
CONTROL INST BUS
L=FILE
L=MEMORY
L=ERASE
L=FRAME
U31B
U35C
U35D
L=DATA ZERO
U28D
U28C
U28B
U28A
U27D
U27C
U27B
U27A
U26D
U26C
U26B
U26A
U17A
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
L=NAME
L=WRITE
4A
44
45
(L=X ADDR/H=Y ADDR)
U31D
+5V
3C
67
3D
68
3C
72
L=DO VECTOR
L=WRITE ENABLE
L=WRITING
U14C
U14D
L=AUX
L=ERASE
U35A
L=ERASE AUX BITS
L=NAMES
L=FRAME
L=ERASE
L=NAME
L-STOP
U34B
U54B
U49B FF
H=ERASE FILE NAMES
H=WRITE FILE NAME
L=FRAME
L=MEMORY
L=ERASE
L=FILE
L=FOUND
U34A
U34C
U35B
H=ERASE FILE OR FRAME
L=FRAME
L=MEMORY
L=BLANK OR UNBLANK
L=FILE
L=FOUND
U44B
U44C
U54A
H=WRITE BLANKING BIT
L=WRITE
L=AUX
L=STOP
U54C
U49D FF
H=WRITE AUX
H=WRITE DISPLAY PARAMETER BITS
H=WRITE DATA
DISPLAY PARAMETER LATCH AN
PE BIT (H=1/L=0)
L=DATA ZERO
U31C
FILE BLANKING L
L=UNBLANK
L=BLANK
U49A
FILE NAME LAT
U32
P=LATCH FILE NAME
U48C
L=CLEAR NAMES
U41C
AUX BLANKING LA
U37
P=LATCH AUX BITS
U48D
MEMORY REA
(L=XADDR/H=YADDR)
H=ERASE FILE NAMES
H=WRITE DISP PARA BITS
U20
A0 (H=Y ADDR)
U53D
U54D
U55C
U16C
U41D
H=ERASE AUX BITS

DISPLAY PARAMETER LATCH AND MULTIPLEXER

MEMORY READ / WRITE CONTROLLER

P/O A2 INTERCONNECT BD

DATA BUS

D1-D13 ARE HIGH TRUE

P/O P1

P/O XA1P1

PE BIT (H=1/L=0)

L=DATA ZERO

U31C

H=ENABLE PEN

FILE BLANKING LATCH

U49A

L=UNBLANK

L=BLANK

H=UNBLANK FILE

FILE NAME LATCH

U32

U48C

P=LATCH FILE NAME

U41C

L=CLEAR NAMES

U48D

P=LATCH AUX BITS

AUX BLANKING LATCH

U37

BIT 1

BIT 2

BIT 3

BIT 4

BIT 5

BIT 6

NC

A0 (H=Y ADDR/L=X ADDR)

U33

U38

MUX

PARA BIT 1

PARA BIT 2

PARA BIT 3

PARA BIT 4

PARA BIT 5

PARA BIT 6

70 4A

71 4A

L=NAME

L=WRITE

L=AUX

L=ERASE

(L=XADDR/H=YADDR)

U35A

L=ERASE AUX BITS

L=NAMES

L=FRAME

L=NAME

L-STOP

U34B

U54B

U49B FF

H=ERASE FILE NAMES

H=WRITE FILE NAME

L=MEMORY

L=FILE

L=FOUND

U34A

U34C

U35B

H=ERASE FILE OR FRAME

L=BLANK OR UNBLANK

U44B

U44C

U54A

H=WRITE BLANKING BIT

U54C

U49D FF

H=WRITE AUX

H=WRITE DISPLAY PARAMETER BITS

H=WRITE DATA

H=ERASE FILE NAMES

H=WRITE DISP PARA BITS

U20

A0 (H=Y ADDR)

U50A

U50B

U50C

H=WRITE OR ERASE FILE NAME

H=WRITE DATA

H=ERASE DATA

U53D

U54D

U55A

H=WRITE PEN ENABLE BIT

U55C

A0 (H=Y ADDR)

H=WRITE FILE BLANKING BIT

U16C

U46A

U46B

U46C

H=WRITE AUX BITS

U41D

H=ERASE AUX BITS

CONTROL INSTRUCTION BUS

73 3C

U47A

U51D

U51C

U51B

U47D

U47C

U47B

1 L=WRITE DATA

13 L=WRITE PB1

10 L= WRITE PB2

4 L=WRITE PB3

13 L=WRITE PB4

10 L=WRITE PB5

4 L=WRITE PB6

101 4A

72 4A

LOGIC DEVICE POWER CONNECTIONS

+5V 16 / 8 — U32,33,37, U38,49

+5V 14 / 7 — U16,17,20,26-28 U31,34,35,41,44, U46,47,48,50,51, U53-55

NOTE:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARDS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

PART OF A1 CONTROL BD		
P/O P1 U14C,14D,16C, U17A,20A,26-28 U31B,31C,31D,	U32,33,34,35, U37,38,41C,41D, U44B,44C,46,47, U48C,48D,49A,	U49B,49D,50, U51B,51C,51D, U53D,54,55A,55C

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3B

Figure 8-23.
Schematic 3B

8-60. SCHEMATIC 3C PRINCIPLES OF OPERATION (MODE AND POINTER CONTROL).

8-61. INTRODUCTION.

Schematic 3C covers two stages on the Control Board:

Memory Mode Controller
Memory Pointer Controller

The Memory Mode Controller selects the mode of memory operation, DO VECTOR, DO WRITE, or REFRESH. It also initiates each addressing cycle on a word by word basis. The Memory Pointer Controller generates the signals used to access the pointer registers and to modify their content.

8-62. MEMORY MODE CONTROLLER.

The three modes of operation, in order of priority, are: DO VECTOR, DO WRITE, and REFRESH. During each one word memory cycle, one of the three Flip-Flops, U5B, U8B, or U8A, will be toggled into the active state. This inhibits U11B, the MODE SELECT gate. Each cycle is selected until END OF MEMORY CYCLE low produces the negative-going RESET. U11B is then enabled to pass the clock signal; U5B, U8B, and U8A then select the next mode.

Each DO VECTOR mode cycle transfers a Coordinate or Text word into the input latch of the Vector Generator. If the data is a Text word, the Character Generator holds off further DO VECTOR cycles while it outputs the character stroke data. The individual strokes are transferred to the Vector Generator like a series of DO VECTOR mode Coordinate word transfers. For details about data transfer, see Service Sheet 3D, Vector Generator Controller, and Service Sheet 5, Character Generator.

While new data is being transferred into the Vector Generator, the data latched with the last DO VECTOR or character stroke transfer is being translated into analog display waveforms. VECTOR BUSY low indicates data is being translated. When VECTOR BUSY goes high, the Vector Generator begins to process the newly latched values. This transition also enables the Memory Mode Contoller to start a new DO VECTOR cycle - to transfer another set of data into the Vector Generator input latches. If a character is being drawn, VECTOR BUSY high enables the transfer of the next stroke coordinates.

Preconditions for entering DO VECTOR mode are established by U2B. This gate inhibits DO VECTOR mode if it receives VECTOR INHIBIT low, CHAR low, or for ~280 ns after the last DO VECTOR operation. VECTOR INHIBIT is generated by the Vector Generator Controller (on Service Sheet 3D). When low, this signal locks out further DO VECTOR cycles during LINE SYNC HOLDOFF, INTERCONNECT HOLDOFF, or CHAR HOLDOFF conditions.

CHAR is produced by the Character Generator; it signals that the word just read from the Display Memory is a text word. CHAR low locks out DO VECTOR cycles while the Character Generator outputs the individual strokes of the character.

The time delay of ~280 ns established by R6 and C3 to allow a DO WRITE cycle to be executed between DO VECTOR cycles.

When enabled by U2B, U5A produces DO VECTOR NEXT high with the first clock after VECTOR BUSY goes high. This inhibits DO WRITE and REFRESH modes via U7A and U7B. On the next clock, U5B toggles and DO VECTOR mode is selected. DO VECTOR low inhibits the Mode Selector through U11B until END OF MEMORY CYCLE low.

DO WRITE mode is entered after the I/O Board latches a complete word to be written into memory. When the data is ready for transfer, the I/O Board pulls DO WRITE low. On the next clock, U4B toggles WRITE NEXT low. Then, while U5A is inhibited (typically because of the ~280 ns time delay between DO VECTOR cycles), U8B is clocked. This toggles WRITING high and begins the execution of the write operation.

U11A and U10B are used to holdoff a DO WRITE cycle after a character has been drawn. At the end of drawing a character, CHAR goes high. U10-8 toggles low; U4B is held "set". The next DO VECTOR cycle resets U10B and allows DO WRITE cycles again to be executed.

A REFRESH mode cycle is executed if DO VECTOR mode is inhibited for more than ~75 μs. This insures the minimum refresh rate requirement of the Display Memory RAMs is satisfied. U13 generates the time window during which a DO VECTOR cycle must occur. U21B holds the timer reset during the execution of each DO VECTOR or REFRESH cycle.

8-63. MEMORY POINTER CONTROLLER.

For each one word memory cycle, control signals must be generated to select the appropriate pointer, to transfer its data to the Memory Address Counter, and then, at the end of the cycle, to store a new address value back into the pointer.

U16A and U16B generate the pointer select code based upon the signals: DO VECTOR, WRITING, and STORE WRITE POINTER. The outputs of these gates, POINTER SELECT 1 and 2, are the address lines to the four byte pointer register stack in the Display Memory. Table 8-11 lists the address code of each pointer register.

Table 8-11. Pointer Register Addresses

Pointer	Pointer Select 1	Pointer Select 2
Read	0	0
Write	1	1
Refresh	0	1

As each memory cycle is begun, U7C sets U18C and U18D enabling U24 to count two clocks, then generate LOAD POINTER high and LOAD ADDR CNTR low. LOAD POINTER triggers the Memory Timing Generator (on Service Sheet 3D) which provides the clock and enable signals to the Display Memory. LOAD ADDR CNTR transfers the address value from the selected pointer register to the Memory Address Counter.

At the end of each memory cycle, a new address is stored in the respective pointer. The Memory Timing Generator outputs END OF CYCLE low which U17C translates to STORE POINTER ADDR low. This signal loads the next X address from the Memory Address Counter into the pointer register selected by U16A and B.

The Write Pointer is also loaded with an address during execution of ERASE or FIND instructions. This operation occurs during a DO VECTOR cycle after the X Data Byte address is transferred from the Read Pointer into the Memory Address Counter. The new address to be written into the Write Pointer is established on the input lines to the pointer register stack while the X Data Byte is addressed. It is then clocked in by STORE POINTER ADDR low. Figure 8-24 illustrates pointer control signal timing.

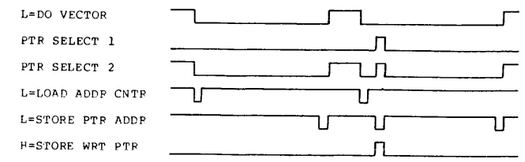
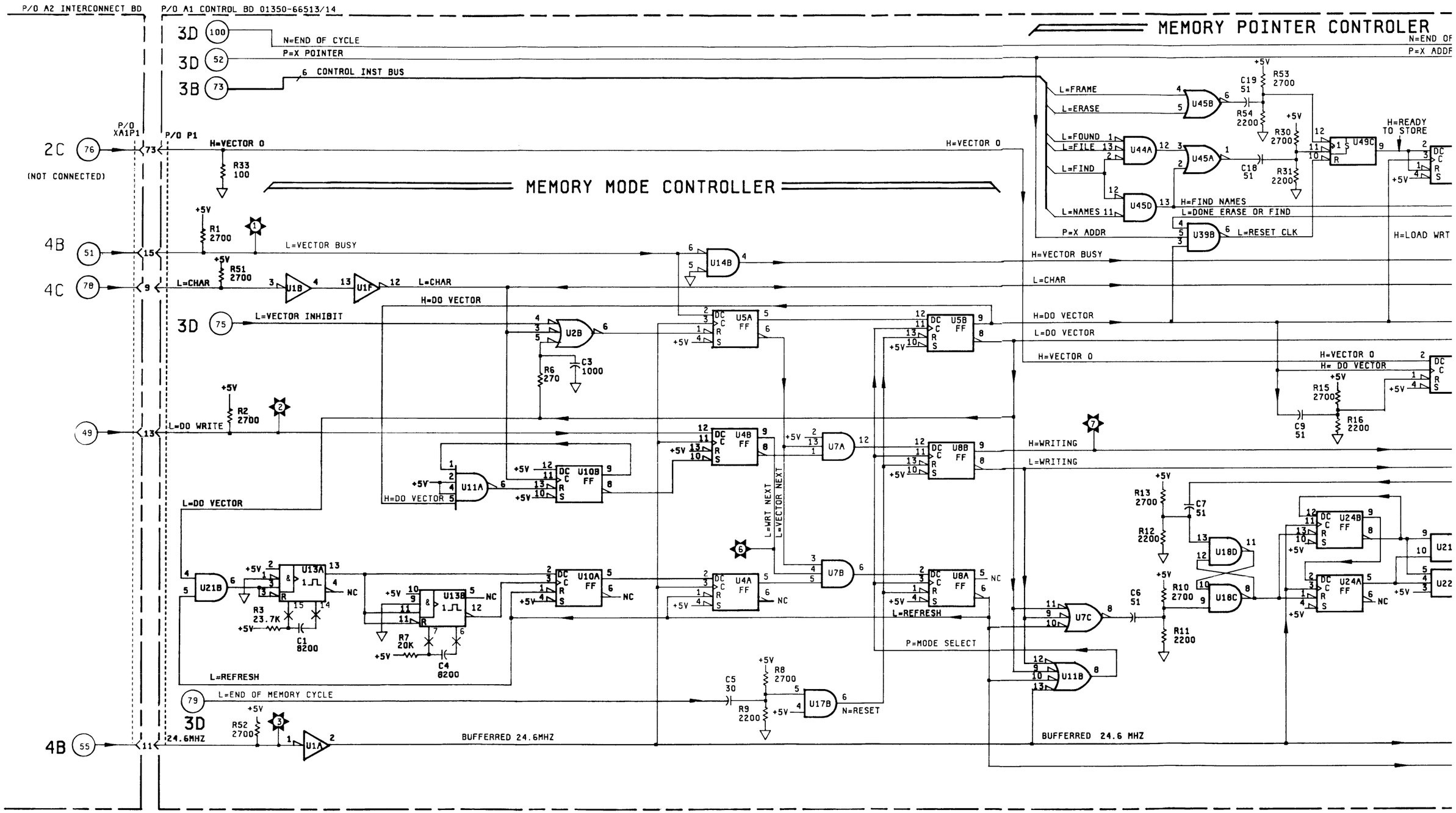


Figure 8-24. Pointer Control Signal Timing

For example, ERASE instructions load address 0 into the Write Pointer. Erasures are always completed at the last address in memory, when FRAME goes high. U45B detects this edge and sets U49C. READY TO STORE is clocked into U60A at the start of the next DO VECTOR cycle. This produces LOAD WRT POINTER high which enables U17D. At the pointer register inputs is the X Data Byte address of the first word of the new frame, address 0. The X ADDR goes high and U17D outputs STORE WRT POINTER high. This edge drives U16A and B to the select code for the Write Pointer and causes U17C to output STORE POINTER ADDR low. U49C and U60A are then reset and POINTER SELECT 1 and 2 return to the code for the Read Pointer. The resetting of U60A produces DONE ERASE OR FIND which signals to the Control Instruction Handshaker that the ERASE instruction execution is complete.

The FIND instructions, FF and FL, modify the Write Pointer data in a similar fashion. FF sets U49C when the File Detector outputs FOUND low. This signals that the next word to be addressed in DO VECTOR mode is in the program specified file. So when the X Data Byte of the next word is addressed, this value is loaded into the Write Pointer. FL sets U49C directly. When LOAD WRT POINTER goes high, U20B outputs LOAD ADDR low. This causes the pointer register inputs to read data from the D1-13 lines. The program specified address is on D1-13 and is loaded into the Write Pointer when STORE POINTER ADDR goes low.


P/O A2 INTERCONNECT BD
P/O A1 CONTROL BD 01350-66513/14
MEMORY POINTER CONTROLER
MEMORY MODE CONTROLLER
3D 100
N=END OF CYCLE
3D 52
P=X POINTER
3B 73
6 CONTROL INST BUS
P/O XA1P1
P/O P1
2C 76
(NOT CONNECTED)
H=VECTOR 0
R33 100
4B 51
L=VECTOR BUSY
R1 2700
4C 78
L=CHAR
R51 2700
U1B
U1F
3D 75
L=VECTOR INHIBIT
U2B
C3 1000
R6 270
U14B
U5A FF
U5B FF
U45B
U44A
U45A
U45D
U49C
U39B
C19 51
R53 2700
R54 2200
R30 2700
C18 51
R31 2200
L=FRAME
L=ERASE
L=FOUND
L=FILE
L=FIND
L=NAMES
P=X ADDR
H=FIND NAMES
L=DONE ERASE OR FIND
L=RESET CLK
H=READY TO STORE
H=LOAD WRT
H=VECTOR BUSY
L=CHAR
H=DO VECTOR
L=DO VECTOR
H=VECTOR 0
H= DO VECTOR
R15 2700
R16 2200
C9 51
49 13
L=DO WRITE
R2 2700
U11A
U10B FF
U4B FF
U7A
U8B FF
H=WRITING
L=WRITING
L=WRT NEXT
L=VECTOR NEXT
U21B
U13A
U13B
R3 23.7K
C1 8200
R7 20K
C4 8200
U10A FF
U4A FF
U7B
U8A FF
L=REFRESH
P=MODE SELECT
U7C
U11B
R13 2700
C7 51
R12 2200
U18D
U18C
R10 2700
C6 51
R11 2200
U24B FF
U24A FF
U21
U22
C5 30
R8 2700
R9 2200
U17B
N=RESET
79
L=END OF MEMORY CYCLE
3D 24.6MHZ
R52 2700
U1A
4B 55
BUFFERRED 24.6MHZ
BUFFERRED 24.6 MHZ
+5V
NC

MEMORY POINTER CONTROLER

P/O A2 INTERCONNECT BD

LOGIC DEVICE POWER CONNECTIONS

+5V 16/8 U13,49 +5V 14/7 U1,2,4,5,7-11,14 16-18,20-22,24,39, 44,45,60,61

NOTES:

1: GATES ARE SYMBOLIZED ACCORDING TO FUNCTION

2: UNLESS OTHERWISE NOTED:
RESISTANCE IN OHMS
CAPACTANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

3: UNLESS OTHERWISE NOTED:
LOGIC LEVELS ARE TTL
+2.0V TO +5.0V=LOGIC "1"=H
0V TO +0.8V=LOGIC "0"=L

POINTER REGISTER ADDR		
MODE	POINTER SELECT 1	POINTER SELECT 2
READ	0	0
WRITE	1	1
REFRESH	0	1

PARTS ON THIS SCHEMATIC

PART OF A1 CONTROL BD

C1,3-7,9,18,19	P/O P1 R1-3,6-13,15, R16,30,31,51-54 TP1,2,3,6,7	U1A,1B,1E,2B, U4,5,7,8,9B, U10,11,13,14, U16A,16B,17B, U17C,17D,18B, U18C,18D,20B, U21,22B,24,39B, U44A,45A,45B, U45D,49C,60A, U61A

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3C

Figure 8-25.
Schematic 3C
8-31

8-64. SCHEMATIC 3D PRINCIPLES OF OPERATION (MEMORY TIMING AND OUTPUT CONTROL).

8-65. INTRODUCTION.

Schematic 3D covers two stages on the Control Board:

Memory Timing Generator
Vector Generator Controller

The Memory Timing Generator produces the clocks and enable signals which govern the memory addressing and data transfer. The Vector Generator Controller selects the source of data and control signals into the Vector Generator.

8-66. MEMORY TIMING GENERATOR.

The Memory Timing Generator is triggered by the trailing edge of LOAD POINTER. As each memory cycle is initiated, the pointer transfers the pointer address to the Memory Address Counter and sets U15A. CLOCK INHIBIT toggles low and the clock gate, U6A, is enabled to pass the 24.6 MHz reference clocks.

The basic timing pulses are produced from this reference clock by U23 and U22A. U23-11 outputs a positive edge at the count of eight clocks. At the count of eleven, U22A outputs NEXT ADDR low. This enables U23 to parallel load zeros on the next (twelfth) clock.

When U23 loads zeros, U22-12 returns high. This transition enables U23 to start counting again and clocks U19. Each clocking of U19 defines a new addressing period. A complete memory cycle has three distinct periods: X Data Byte address, Y Data Byte address, and next X Data Byte address.

The circuit of U12A, U6B, U12B, and U15 detects the eighth clock in the third (next X) period. U12B outputs END OF CYCLE low which enables U23 to reset on the next reference clock. It also stores the current (next X) address in the pointer stack. (See Memory Pointer Controller, Schematic 3C.)

The ninth clock in the next X Data Byte period completes the cycle. It switches END OF CYCLE high and resets U23. U15A toggles, producing END OF MEM CYCLE low and CLOCK INHIBIT high. END OF MEM CYCLE low inhibits U23 from counting. It also resets U15B for the next memory cycle and resets the Mode Controller (Schematic 3C). CLOCK INHIBIT high blocks the reference clock until the next memory cycle is begun.

The Memory Address Counters are incremented by MEM CLK. This pulse is generated by U21A at the start of each of the three addressing periods.

The X,Y, and NEXT X ADDR signals are used to latch data from the Display Memory into the Character Generator and Vector Generator. These signals occur after the corresponding address is established in the Display Memory and the RAM output data is valid. U29A decodes the outputs from U19 during DO VECTOR cycles. It then selects the appropriate gates, U6C, U6D and U9D, or U9C to enable.

U18A, U1D, and U12C produce the enable signal to the RAM chips and provide the clock pulse to the address clock gates. The output of U18A goes low at the beginning of each addressing period and stays low until the ninth reference clock. U12C produces a low pulse during the period of the eighth reference clock.

U20D produces a negative edge when U19-5 is toggled high. CHANGE DATA low signals the I/O Board that the Y address period is beginning and to put the Y data on D1-13. Figure 8-26 illustrates typical memory timing waveforms.

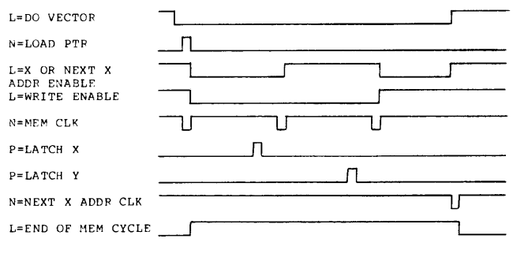


Figure 8-26. Memory Timing Signals

8-67. VECTOR GENERATOR CONTROLLER.

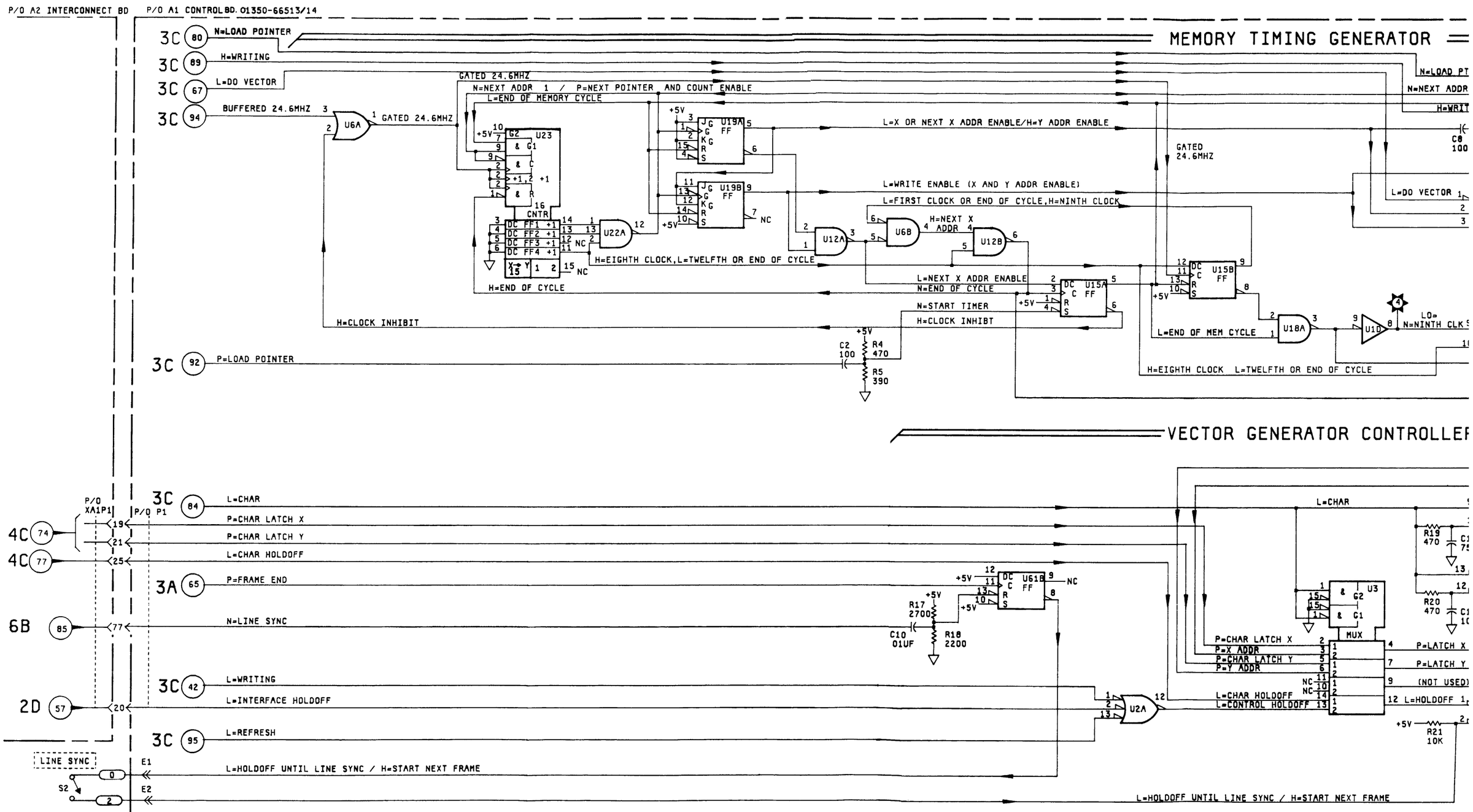
When the 1350A is in DO VECTOR mode, X and Y Data Bytes are transferred into the Vector Generator and the Character Generator from the Display Memory. If the addressed word contains the text flag (X data = 1023) the Character Generator outputs the series of vectors (strokes) defined by the character code in the Y Data Byte. The Vector Generator processes coordinate and text data in the same way; the basic operational difference between the two is the source of the data and data transfer control signals.

When a word is read from the Display Memory by the Vector and Character Generators, CHAR is high. U20C and U16D are in their normal state, MEMORY OUTPUT ENABLE low and CHAR OUTPUT ENABLE high. If the word is text, the Character Generator pulls CHAR low. U20C and U16D then disable the Display Memory output and enable the Character Generator to output the character stroke data to the Vector Generator.

The LATCH X and Y signals clock the data to be drawn into the Vector Generator. When CHAR is high, these signals are actually X ADDR and Y ADDR CLKs. They signify the X and Y Data Bytes are addressed and that valid data is on V1-10 bus. If the data is text, the Character Generator pulls CHAR low and outputs CHAR LATCH X and Y to transfer each stroke to the Vector Generator.

VECTOR INHIBIT low holds the Vector Generator in a reset condition in which it cannot process or output data. While CHAR is high, U2A determines whether a holdoff condition exists. It senses when the Mode Controller has selected DO WRITE or REFRESH mode, or if the I/O Board has received a holdoff request from a display. Any of these conditions generate CONTROL HOLDOFF low. When a character is first detected, the Character Generator outputs CHAR HOLDOFF low. It stays low until the text code is decoded and the Character Generator is ready to output the stroke data.

U53A OR's the HOLDOFF signal with the output of the line sync circuit. In LINE SYNC mode the 1350A begins each new frame in phase with the second harmonic of line frequency. The positive edge of FRAME END toggles U61B, and generates HOLDOFF UNTIL LINE SYNC. If S2 is closed, U53A then outputs VECTOR INHIBIT until U61B is reset.


P/O A2 INTERCONNECT BD
P/O A1 CONTROL BD. 01350-66513/14
MEMORY TIMING GENERATOR
VECTOR GENERATOR CONTROLLER
3C 80 N=LOAD POINTER
3C 89 H=WRITING
3C 67 L=DO VECTOR
3C 94 BUFFERED 24.6MHZ
3C 92 P=LOAD POINTER
U6A
GATED 24.6MHZ
N=NEXT ADDR 1 / P=NEXT POINTER AND COUNT ENABLE
L=END OF MEMORY CYCLE
U23
CNTR
U19A
U19B
L=X OR NEXT X ADDR ENABLE/H=Y ADDR ENABLE
L=WRITE ENABLE (X AND Y ADDR ENABLE)
L=FIRST CLOCK OR END OF CYCLE,H=NINTH CLOCK
U22A
H=EIGHTH CLOCK,L=TWELFTH OR END OF CYCLE
U12A
U6B
U12B
H=NEXT X ADDR
L=NEXT X ADDR ENABLE
N=END OF CYCLE
H=END OF CYCLE
N=START TIMER
H=CLOCK INHIBT
H=CLOCK INHIBIT
U15A
U15B
GATED 24.6MHZ
L=END OF MEM CYCLE
U18A
U1D
H=EIGHTH CLOCK L=TWELFTH OR END OF CYCLE
C2 100
R4 470
R5 390
N=LOAD PI
N=NEXT ADDR
H=WRIT
C8 100
L=DO VECTOR
LO= N=NINTH CLK
P/O XA1P1
P/O P1
4C 74
4C 77
3A 65
6B 85
2D 57
3C 84 L=CHAR
P=CHAR LATCH X
P=CHAR LATCH Y
L=CHAR HOLDOFF
P=FRAME END
N=LINE SYNC
3C 42 L=WRITING
L=INTERFACE HOLDOFF
3C 95 L=REFRESH
LINE SYNC
S2
E1
E2
L=HOLDOFF UNTIL LINE SYNC / H=START NEXT FRAME
U61B
R17 2700
C10 01UF
R18 2200
U2A
MUX
P=CHAR LATCH X
P=X ADDR
P=CHAR LATCH Y
P=Y ADDR
L=CHAR HOLDOFF
L=CONTROL HOLDOFF
P=LATCH X
P=LATCH Y
(NOT USED)
12 L=HOLDOFF 1
R19 470
R20 470
R21 10K
L=HOLDOFF UNTIL LINE SYNC / H=START NEXT FRAME

MEMORY TIMING GENERATOR

P/O P1

P/O XA1P1

P/O A2 INTERCONNECT BD

N=LOAD PTR

N=NEXT ADDR

H=WRITING

U21A

U20D

C8 100

R14 470

N=MEMORY CLK

L=END OF MEM CYCLE

N=CHANGE DATA

L=X OR NEXT X ADDR ENABLE/H=Y ADDR ENABLE

GATED 24.6MHZ

L=WRITE ENABLE

L=WRITE ENABLE (X AND Y ADDR ENABLE)

L=FIRST CLOCK OR END OF CYCLE,H=NINTH CLOCK

L=DO VECTOR

U29A X→Y

U6C

U6D

P=X ADDR

P=Y ADDR

U12A

U6B

H=NEXT X ADDR

U12B

END OF CYCLE

L=NEXT X ADDR ENABLE

N=END OF CYCLE

U15A DC C FF R S

U15B DC C FF R S

+5V

N=START TIMER

H=CLOCK INHIBT

C2 100

R4 470

R5 390

U18A

U10

LO= N=NINTH CLK

U12C

N=POINTER

U9D

U9C

N=Y ADDR

N=NEXT X ADDR

L=MEMORY CHIP ENABLE

L=END OF MEM CYCLE

H=EIGHTH CLOCK L=TWELFTH OR END OF CYCLE

N=END OF CYCLE

93 4A

79 3C

45 2B

68 3B

52 3C

52 2D,4C

53 2D,4C

69 3E

60 3A

60 2C (NOT USED)

66 4A

100 3C

VECTOR GENERATOR CONTROLLER

L=CHAR

U20C

U16D

R19 470

C11 750

R20 470

C12 100

L=MEMORY OUTPUT ENABLE

L=CHAR OUTPUT ENABLE

90 4A

96 4C

U61B DC C FF R S

R17 2700

C10 01UF

R18 2200

NC

U3 MUX

P=CHAR LATCH X

P=X ADDR

P=CHAR LATCH Y

P=Y ADDR

L=CHAR HOLDOFF

L=CONTROL HOLDOFF

P=LATCH X

P=LATCH Y

(NOT USED)

L=HOLDOFF

U2A

U53A

R21 10K

L=VECTOR INHIBIT

P=LATCH X

P=LATCH Y

(NOT USED)

97 4D

NC

75 4B

75 3C

L=HOLDOFF UNTIL LINE SYNC / H=START NEXT FRAME

LOGIC DEVICE POWER CONNECTIONS

+5V pin 14 / pin 7: U1,2,6,9,12,15, U16,18,20,22, U53,61

+5V pin 16 / pin 8: U3,19,23,29

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARDS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

PARTS ON CHASSIS

S2 [LINE SYNC]

P/O A1 CONTROL BD

C2,8,10,11,12, E1,2 P/O P1 R4,5,14, 17-21 TP4	U1D,2A,3,6,9C,9D,12A,12B,12C, U15,16D,18A,19,20C,20D,22A, U23,29A,53A,61B

1350/113

3D

Figure 8-27.
Schematic 3D

8-68. SCHEMATIC 3E PRINCIPLES OF OPERATION (Z-AXIS OUTPUT).

8-69. INTRODUCTION.

Schematic 3E covers three stages on the Control Board:

Z-axis Blanking Controller
Z-axis Level Controller
Z-axis Amplifier

The Z-axis Blanking Controller reads the blanking data of each coordinate or text word as its transferred to the Vector Generator. From this data, it generates the blanking input to the Z-axis amplifier. The Z-axis Level Controller latches the five bit intensity code computed by the Vector Generator and converts it into an analog waveform. The Z-axis amplifier sums the blanking and intensity signals and drives the 50-ohm Z-axis output.

8-70. Z-AXIS BLANKING CONTROLLER.

The blanking inputs are combined in U51A, U43A, and U53B. U43A latches the PE and UNBLANK FILE data on the positive (trailing) edge of Y ADDR. This word level data is then OR'ed with BLANK CHAR so the individual strokes of a character may be blanked.

As each vector or character stroke is drawn, VECTOR BUSY goes high and clocks the blanking data into U43B. VECTOR BUSY high also triggers U64B which provides a delayed clock to U60B. The delay compensates for the delay time required in the Vector Generator. With the trailing edge from U64B, U60B loads and outputs the blanking signal.

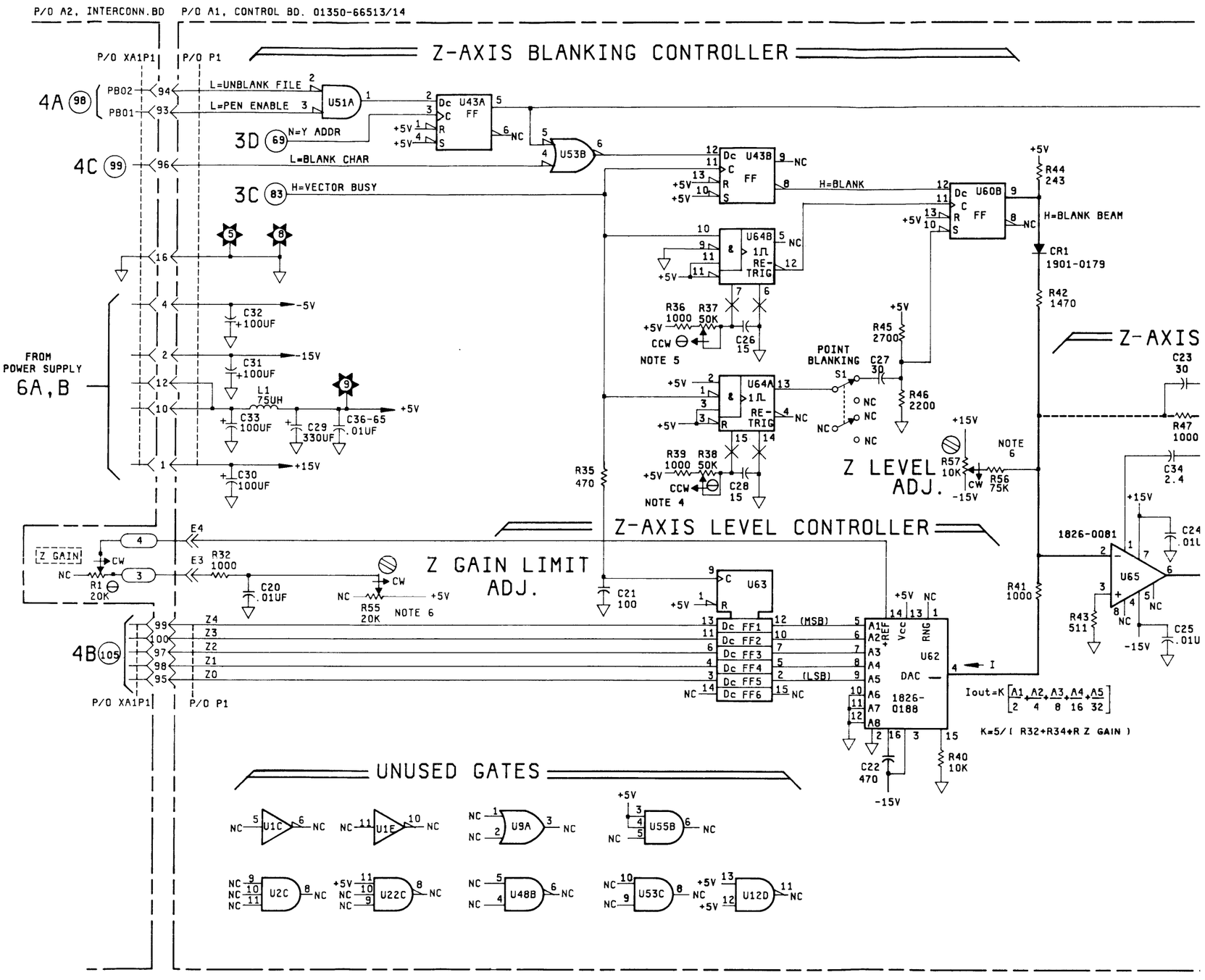
For some types of display information, a clearer picture is drawn if the Point Blanking circuit, U64A, is enabled. U64A generates a blanking pulse after each vector or character stroke is drawn. C28 and R38 set the delay from the end of the stroke (VECTOR BUSY low) until the blanking pulse is generated. This allows the user to optimize the output for the display being driven.

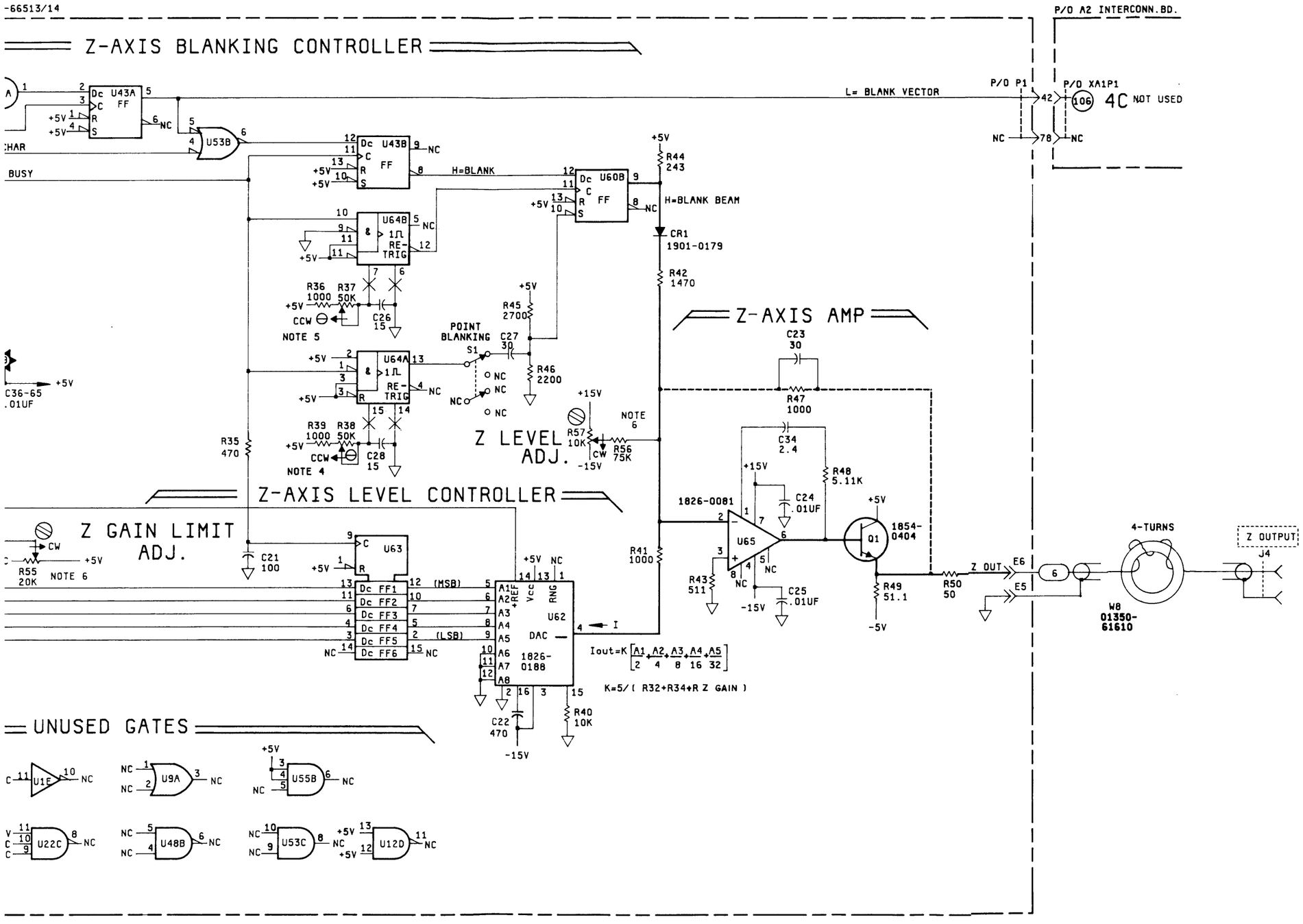
8-71. Z-AXIS LEVEL CONTROLLER.

The Vector Generator computes how bright each vector should be drawn. This data is put on the Z0-4 lines; VECTOR BUSY is pulled high, and the vector is drawn. U63 latches the intensity bits on the transition of VECTOR BUSY high and U62 converts them into a proportional current. Note the +REF input on U62. The current into it scales the output current. R55 is adjusted such that when the rear panel Z-GAIN pot is fully clockwise and Z0-4 are all high, the Z-axis output is +1 volt.

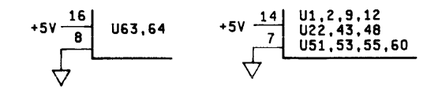
8-72. Z-AXIS AMPLIFIER.

U65 sums the output currents from the Blanking and Level Controllers, and converts them to a voltage. Q1 provides the buffering needed to drive the 50-ohm output. R56 and 57 provide an offset adjustment which is used to set the minimum unblanked Z output at ~40 mV when Z0-4 are all low.


P/O A2, INTERCONN.BD
P/O A1, CONTROL BD. 01350-66513/14
Z-AXIS BLANKING CONTROLLER
P/O XA1P1
P/O P1
4A (98)
PB02
PB01
L=UNBLANK FILE
L=PEN ENABLE
U51A
3D (69)
N=Y ADDR
U43A FF
4C (99)
L=BLANK CHAR
U53B
3C (83)
H=VECTOR BUSY
U43B FF
H=BLANK
U60B FF
H=BLANK BEAM
R44 243
CR1 1901-0179
R42 1470
U64B 1µ RE-TRIG
U64A 1µ RE-TRIG
NOTE 5
NOTE 4
R36 1000
R37 50K
C26 15
R39 1000
R38 50K
C28 15
POINT BLANKING
S1
C27 30
R45 2700
R46 2200
R57 10K
CW
R56 75K
NOTE 6
Z LEVEL ADJ.
FROM POWER SUPPLY 6A,B
C32 +100UF
C31 +100UF
L1 75UH
C33 100UF
C29 330UF
C36-65 .01UF
C30 100UF
-5V
-15V
+5V
+15V
R35 470
Z-AXIS LEVEL CONTROLLER
Z GAIN
R1 20K
R32 1000
C20 .01UF
Z GAIN LIMIT ADJ.
R55 20K
NOTE 6
C21 100
U63
4B (105)
Z4
Z3
Z2
Z1
Z0
Dc FF1
Dc FF2
Dc FF3
Dc FF4
Dc FF5
Dc FF6
(MSB)
(LSB)
U62
DAC
1826-0188
Iout=K [A1 A2 A3 A4 A5 / 2 4 8 16 32]
K=5/(R32+R34+R Z GAIN)
C22 470
R40 10K
R41 1000
R43 511
C25 .01U
1826-0081
U65
C23 30
R47 1000
C34 2.4
C24 .01U
UNUSED GATES
U1C
U1E
U9A
U55B
U2C
U22C
U48B
U53C
U12D



LOGIC DEVICE POWER CONNECTIONS:



NOTE:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE INDICATED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE INDICATED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V ="1"=H
   0V TO +0.8V ="0"=L
4. R38 IS USED TO COMPENSATE FOR THE RESPONSE TIME OF THE DISPLAY BEING DRIVEN WHEN POINT BLANKING IS ENABLED. ADJUST PER INSTRUCTIONS IN SECTION V.
5. R37 COMPENSATES THE DELAY OF X AND Y OUTPUT DATA THROUGH THE VECTOR GENERATOR. ADJUST PER INSTRUCTIONS IN SECTION V.
6. R55 & R57 ADJUST THE SPAN AND OFFSET OF THE Z OUTPUT SIGNAL. ADJUST PER INSTRUCTIONS IN SECTION V.

PARTS ON THIS SCHEMATIC

PARTS ON CHASSIS		
A2XA1 J3 Z OUT	R1 W8 Z GAIN	
PART OF A1 CONTROL BD		
C20-34 C36-65 CR1 E3-6 L1 P/OP1	Q1 R32,35-50,55-57 S1:POINT BLANKING TP5:GND TP8:GND TP9:+5V	U1E,1F,2C,9D U12D,22C,43,48D U51D,53C,53D U55C,60B,62-65

1350A-101

3E

Figure 8-28. Schematic 3E

8-73. DISPLAY BOARD ASSEMBLY A4. (SERVICE SHEET 4).

8-74. DISPLAY BOARD TROUBLESHOOTING.

A troubleshooting flow chart for the Display Board assembly is shown in figure 8-29.

8-75. GENERAL INFORMATION.

Display Board Assembly A4 contains the Memory for all data, control, and parameter functions; the control circuits for processing Vector information in the plot absolute (PA) mode; and two Digital to Analog Converter (DAC) circuits as output to the X-Y Display.

The Simplified Block Diagrams for A4 show major functional stages and their corresponding schematic locations (4A-4E). Detailed signal and stage descriptions are covered by the explanations of each of the five schematics. Figure 8-30 is the Simplified Block Diagram for Schematic 4A. Figure 8-33 is the Simplified Block Diagram for Schematics 4B-4E.

8-76. OPERATING OVERVIEW.

The Display Board contains three functional areas:

Memory and assocaited circuits, Arithmetic circuits for vector generation, and two Digital To Analog Converters.

All Memory Data and Control signals are received from the Control Board. Data is written to, and read from the Display Memory under control of the Memory Read/Write line and Chip Enable signal. PARAMETER BITS 1-6 are written to, and read from the Display Memory under the control of six individual Read/Write lines and the Chip Enable signal.

Memory is normally addressed sequentialy from memory address 0 to 2048 by the Memory Address Counter. Should an interruption in the sequential addressing occur, the next address in the sequence is stored as a pointer in the Pointer Address Memory. The pointers allow the system to remember the next location to be addressed in each mode of operation. A pointer is stored to remember the next memory location to be read from, written to, or refreshed.

After data has been programmed and stored in Display Memory, the memory data is then read for use of the Vector and Character generators.

The first data byte from memory is always read when Address line 0 (A0) is low. If all vector data (V1-V10) in the first byte is low (=1023) this indicates the word is text and the following byte (A0=H) is sent to the character generator. If the data in the first byte (A0=L) is not all low (<1023), this byte is the X Vector Coordinate and the following byte (A0=H) is the Y Vector Coordinate. The X and Y Coordinates are then sent to the Vector Generator portion of the Display Board.

Display Memory data (V1-V10) is latched into the X and Y Vector Generator logic circuits by the LATCH X and LATCH Y signals from the Control Board.

After the X and Y Coordinates are stored in the X and Y Coordinate Storage registers a vector is generated from the end of the previous vector to the new X,Y coordinate.

Vector Generation is accomplished by first determining how far in each plane (X and Y) the pen (beam) must move. This is done by subtracting the starting position from the input coordinate. This subtraction results in the absolute length of the vector in each plane and determines the direction of the vector. As an example, if the position is less than the coordinate (position 0; coordinate 200) the vector must be drawn in the positive direction (left to right in the X plane; bottom to top in the Y plane), however, if the position is larger than the coordinate (position 200; coordinate 0) the vector must be drawn in the negative direction. The direction of the vector determines if the Position Counter will count up (positive direction vector) or down, and the absolute length of the vector determines how many counts the Position Counter must make.

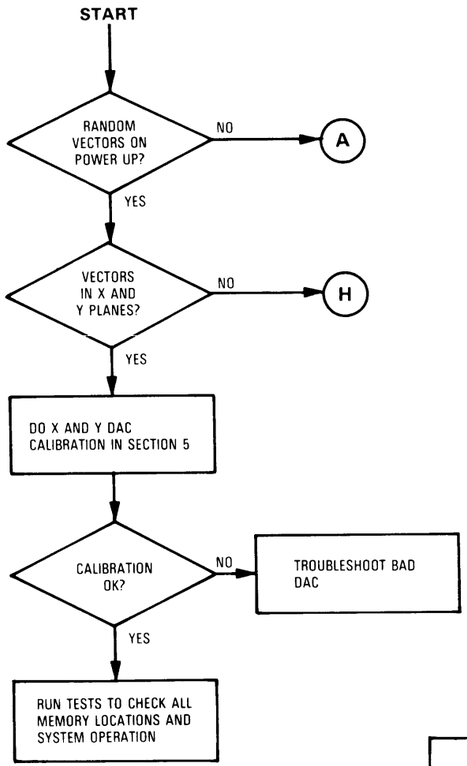
The position-to-coordinate difference will be complemeted if it is a negative value. The complement causes the absolute length input to the X and Y Length Detectors to be the same regardless of sign.

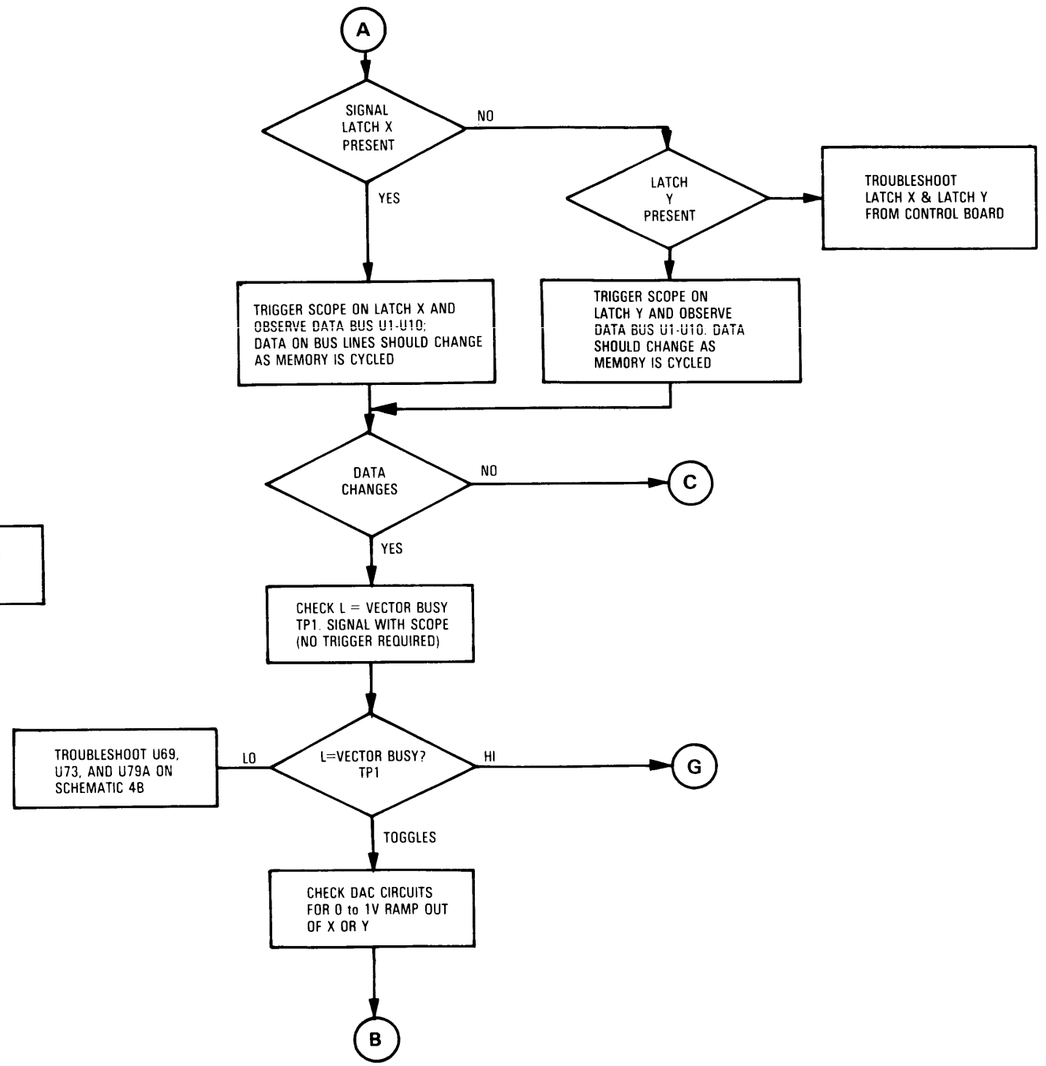
The X and Y Length Detectors are loaded with the absolute length value of the vector and do a shift right operation until the length of the longest vector is determined. This shift operation will determine the time required to draw this vector.

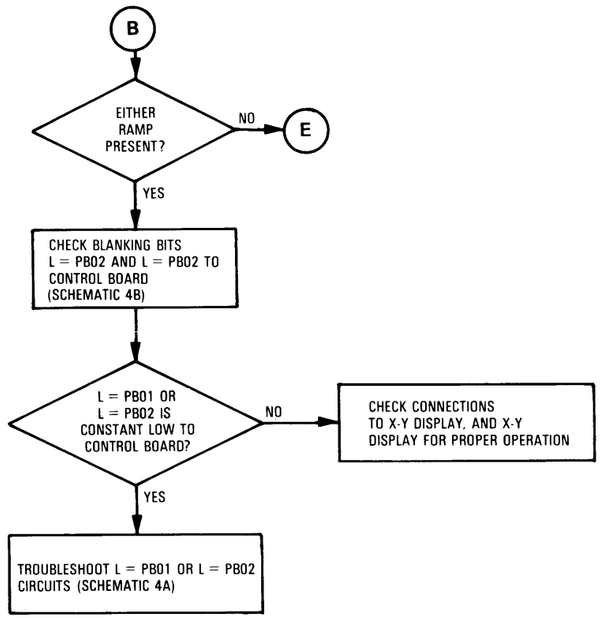
After the shift right operation is complete, the Vector Busy Flip-Flop is set and 24.6 MHz clocks are gated to the X and Y Length-Rate Clock and End of Vector Clock circuits. The X and Y Length-Rate Clock circuits provide clocks to their respective Position Counters, causing the counters to increment or decrement to the input coordinate position. The End of Vector Clock circuit counts input clocks and will reset the Vector Busy Flip-Flop after a predetermined time.

As the Position Counters are incremented or decremented, the inputs to the Digital to Analog Converters are changed. The DACs convert the Position Counter outputs to a ramp potential of 0 V to 1 V for input to the X-Y Display unit.

Intensity Modulation data is extracted from the X and Y Length Detectors and provided to the Control Board as Z0-4.


START
RANDOM VECTORS ON POWER UP?
NO
A
YES
VECTORS IN X AND Y PLANES?
NO
H
YES
DO X AND Y DAC CALIBRATION IN SECTION 5
CALIBRATION OK?
NO
TROUBLESHOOT BAD DAC
YES
RUN TESTS TO CHECK ALL MEMORY LOCATIONS AND SYSTEM OPERATION


A
SIGNAL LATCH X PRESENT
NO
LATCH Y PRESENT
TROUBLESHOOT LATCH X & LATCH Y FROM CONTROL BOARD
YES
TRIGGER SCOPE ON LATCH X AND OBSERVE DATA BUS U1-U10; DATA ON BUS LINES SHOULD CHANGE AS MEMORY IS CYCLED
TRIGGER SCOPE ON LATCH Y AND OBSERVE DATA BUS U1-U10. DATA SHOULD CHANGE AS MEMORY IS CYCLED
DATA CHANGES
NO
C
YES
CHECK L = VECTOR BUSY TP1. SIGNAL WITH SCOPE (NO TRIGGER REQUIRED)
TROUBLESHOOT U69, U73, AND U79A ON SCHEMATIC 4B
LO
L=VECTOR BUSY? TP1
HI
G
TOGGLES
CHECK DAC CIRCUITS FOR 0 to 1V RAMP OUT OF X OR Y
B


B
EITHER RAMP PRESENT?
NO
E
YES
CHECK BLANKING BITS L = PB02 AND L = PB02 TO CONTROL BOARD (SCHEMATIC 4B)
L = PB01 OR L = PB02 IS CONSTANT LOW TO CONTROL BOARD?
NO
CHECK CONNECTIONS TO X-Y DISPLAY, AND X-Y DISPLAY FOR PROPER OPERATION
YES
TROUBLESHOOT L = PB01 OR L = PB02 CIRCUITS (SCHEMATIC 4A)

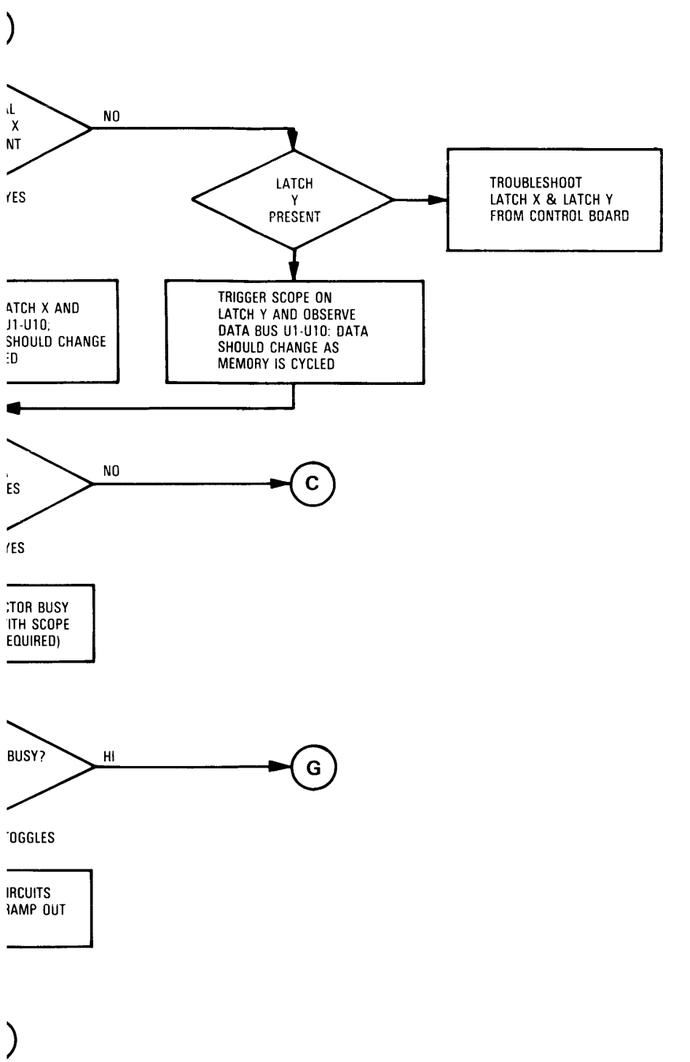
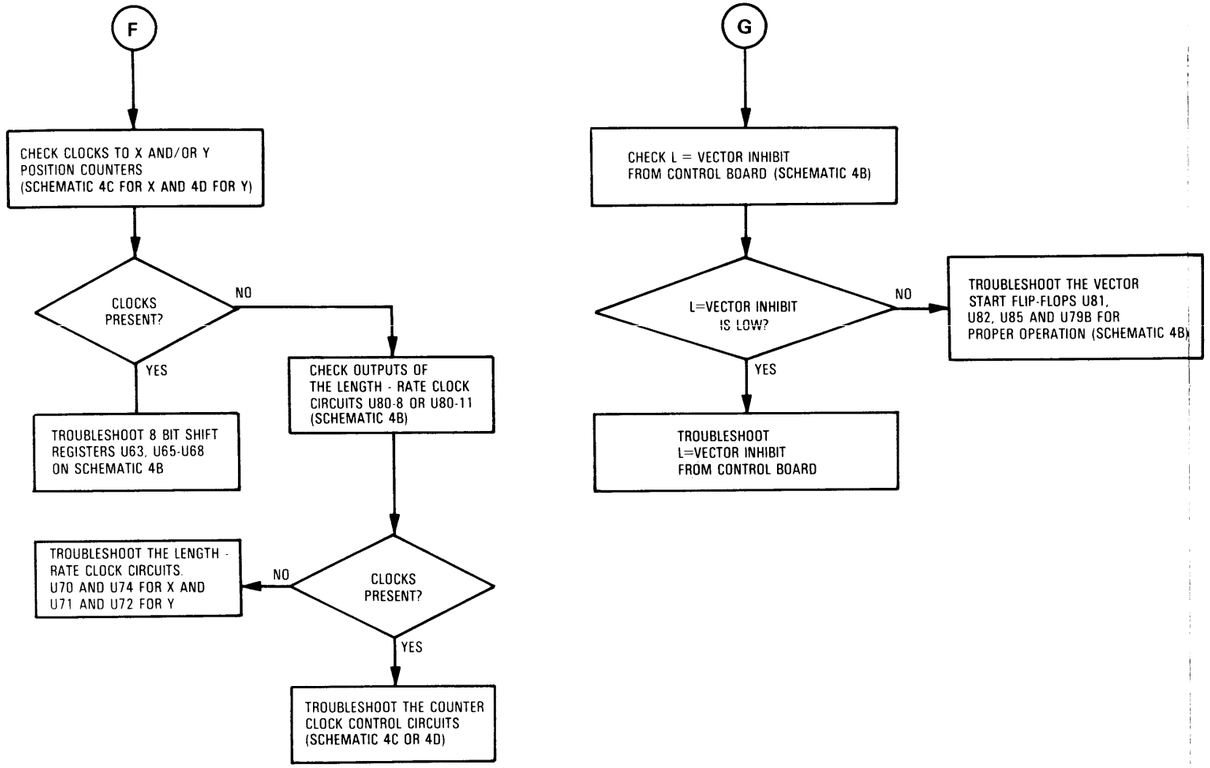


Figure 8-29.
Display Board A4 Troubleshooting Flow Chart (Sheet 1 of 2)


F
CHECK CLOCKS TO X AND/OR Y POSITION COUNTERS (SCHEMATIC 4C FOR X AND 4D FOR Y)
CLOCKS PRESENT?
NO
YES
TROUBLESHOOT 8 BIT SHIFT REGISTERS U63, U65-U68 ON SCHEMATIC 4B
CHECK OUTPUTS OF THE LENGTH - RATE CLOCK CIRCUITS U80-8 OR U80-11 (SCHEMATIC 4B)
CLOCKS PRESENT?
NO
YES
TROUBLESHOOT THE LENGTH - RATE CLOCK CIRCUITS. U70 AND U74 FOR X AND U71 AND U72 FOR Y
TROUBLESHOOT THE COUNTER CLOCK CONTROL CIRCUITS (SCHEMATIC 4C OR 4D)
G
CHECK L = VECTOR INHIBIT FROM CONTROL BOARD (SCHEMATIC 4B)
L=VECTOR INHIBIT IS LOW?
NO
YES
TROUBLESHOOT THE VECTOR START FLIP-FLOPS U81, U82, U85 AND U79B FOR PROPER OPERATION (SCHEMATIC 4B)
TROUBLESHOOT L=VECTOR INHIBIT FROM CONTROL BOARD
TROUBLESHOOT LATCH X FROM CONTROL BOARD

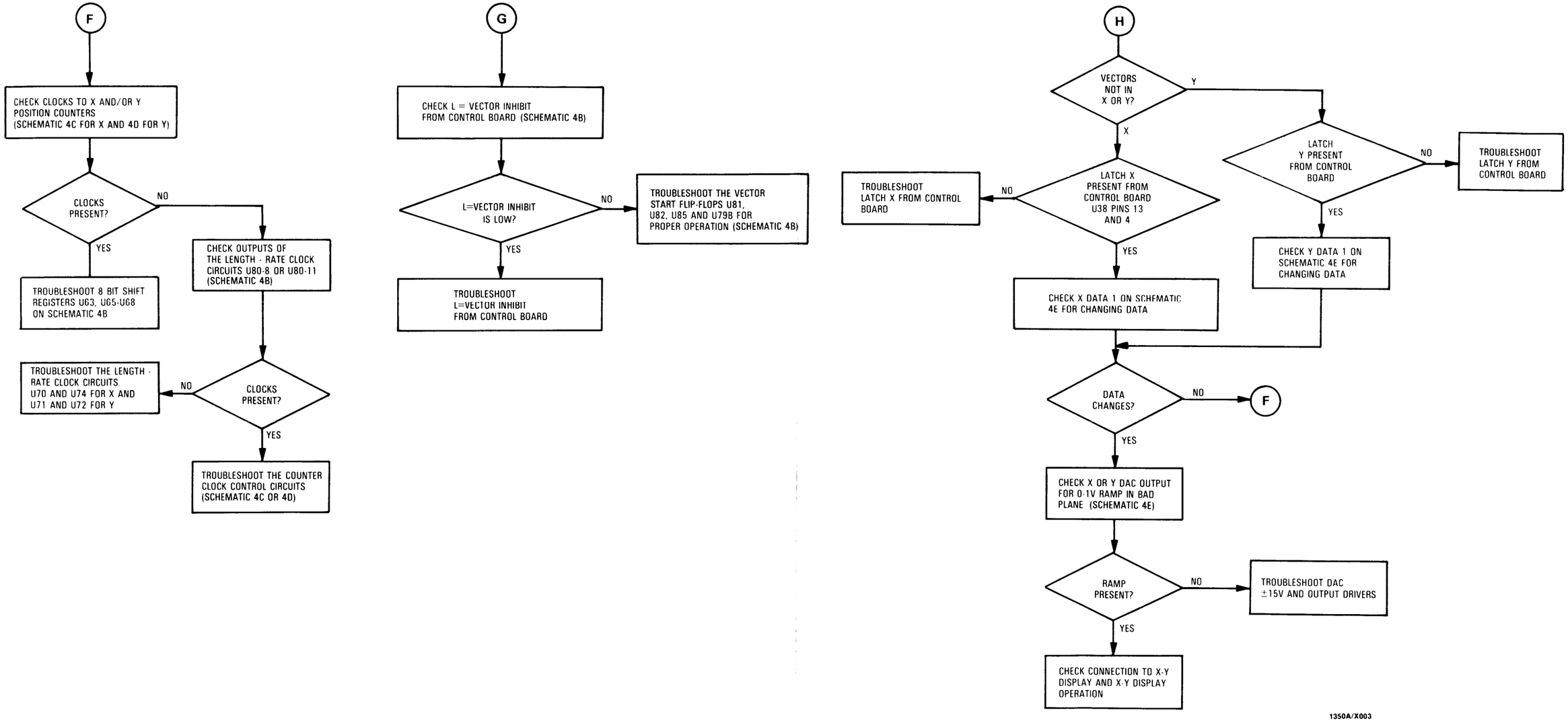


Figure 8-29. Display Board A4 Troubleshooting Flow Chart (Sheet 2 of 2)

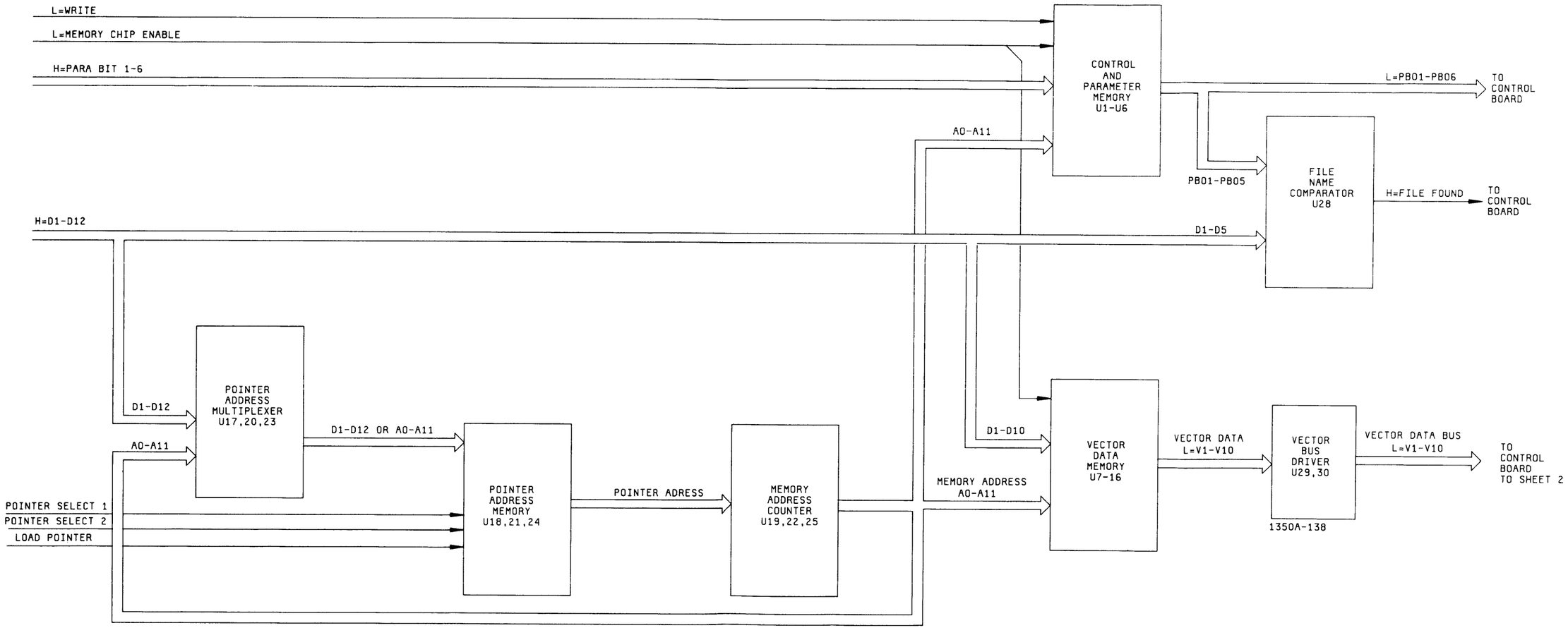


Figure 8-30.
Simplified Block Diagram for Schematic 4A

8-77. SCHEMATIC 4A PRINCIPLES OF OPERATION.

Schematic 4A contains:

1. Display Memory
2. Memory Chip Enable
3. Memory Address Counter
4. Pointer Address Memory
5. Pointer Address Multiplexer
6. File Name Comparator
7. Vector Bus Driver

8-78. OPERATING OVERVIEW.

The Display Memory is comprised of sixteen random access memory (RAM) ICs (U1-U16). Each RAM is a 4096 by 1 bit device. Of these RAMs, U7-U16 are used for vector coordinate data or text data and U1-U6 are used for display parameter data (file names and blanking information). For every X-Y Coordinate pair and every Text Flag/Character Code pair stored in memory, two successive address locations are used in each of the 16 RAMs. The first location is the X Data Byte and is always at an even address. The second location is the Y Data Byte and is always at an odd address. Together, the X and Y Data Bytes form a 32 bit data word, the basic unit of display information. Table 8-12 lists typical locations of coordinate and text word data in memory.

The Control Board selects one of three possible Display Memory operating modes: DO VECTOR, DO WRITE, or REFRESH.

DO VECTOR is the highest priority mode. In this mode, one word is read, one byte at a time, into the vector generator and is translated into the analog waveforms for display. Also, under program control, certain display parameter bits may be modified as they are read.

If the I/O Board receives a PA or TX instruction, it requests the Control Board to perform a DO WRITE operation. In this mode, the vector generator is disabled, the Z-axis output is blanked, and the X and Y data bytes of the coordinate or text word are written into memory.

REFRESH is a default mode which is strictly an internal operation. It is used occasionally when the 1350A is in LINE SYNC or when it is plotting large characters to insure that the RAM refresh requirements are satisfied.

In each mode, memory operations are performed on a word by word basis. For every word, a three step memory cycle occurs. First, the X Data Byte location is addressed. Second, the Y Data Byte location is addressed. Third, the next X Data Byte address is generated and stored. After the third step, the Control Board reselects the memory mode and a new cycle is initiated. The value stored as the next X Data Byte address is then recalled and becomes the X Data Byte address for the new cycle. In this way, the 1350A scrolls sequentially through all 2048 word locations; after the last memory address, the process begins again with location 0. Each complete pass through all 2048 word locations is called a frame.

For each mode there is a special memory register (U18,21,24) in which the next X Data Byte address is stored. These registers are the Pointer Address Memory and contain the Read, Write, and Refresh pointers. The pointer system allows the Control Board to change from one mode to another, addressing different areas of memory, but still remember the proper location for the next operation in each mode. There are several ways in which the write pointer may be loaded with a specific address to enable the programmer to access a particular word location. Operation of the pointers is discussed in more detail in the following paragraphs.

8-79. DETAILED OPERATION.

The three major modes of operation, DO VECTOR, DO WRITE, REFRESH, and the File Name Comparator are discussed in detail as follows:

DO VECTOR

When the Control Board selects the DO VECTOR mode, the Control Board will input the signals required by the Display Board to read an X Data Byte from memory, increment the Memory Address Counter one count, read a Y Data Byte from memory, increment the address counter a second time, and write the new X Data Byte address into the Pointer Address Memory as a read pointer.

The sequence of signals for this operation is as follows:

1. Input lines POINTER SELECT 1 and POINTER SELECT 2 are pulled low to address the Read Pointer locations of the Pointer Address Memory (U18,21,24), making the read address available to the Memory Address Counter.

2. L=LOAD ADDR CNTR and a positive transistion on the L=MEM CLK will load the read pointer into the Memory Address Counter.

3. L=MEMORY CHIP ENABLE is set high to bring all memory chips (U1-U16) out of the low power standby state.

4. L=WRITE DATA and L=PARAMETER BITS 1-6 are all set high to place Display Memory in the read mode.

5. L=MEMORY OUTPUT ENABLE will go low to enable the Vector Bus Driver (U29, 30) outputs V1-V10. At this point the X Data Byte is available on the V1-V10 output bus. A LATCH X signal is now produced by the Control Board to store the X Data Byte in the X Coordinate Storage register on schematic 4C.

6. L=MEMORY CHIP ENABLE will go low.

7. L=MEM CLK will increment the Memory Address Counter (U19, 22, 25).

8. L=MEMORY CHIP ENABLE is returned high. The Y Data Byte is now available on the V1-V10 lines. A LATCH Y signal is now produced by the Control Board to store the Y Data Byte in the Y Coordinate Storage register on schematic 4D.

9. L=MEM CLK will again increment the Memory Address Counter (U19, 22, 25).

10. L=LOAD ADDR is brought high to gate the Memory Address Counter output through the Pointer Address Multiplexer.

11. L=STORE POINTER ADDR will go low, which writes the new X Data Byte address into the same location of the Pointer Address Memory (U18, 21, 24) that was read to begin this sequence.

DO WRITE

When a DO WRITE command is sent from the I/O Board to the Control Board, the Control Board will provide the signals required to read the Write Pointer, write an X Data Byte into memory, increment the Memory Address Counter one count, write a Y Data Byte into memory, increment the Memory Address Counter a second time, and write the new X Data Byte address into the Pointer Address Memory as a Write Pointer.

The sequence of signals for the DO WRITE operation is as follows:

1. Input lines POINTER SELECT 1 and POINTER SELECT 2 will both go high to select the write pointer location of the Pointer Address Memory (U18, 21, 24), making the write address available to the Memory Address Counter.

2. L=LOAD ADDR CNTR and a positive transistion on the L=MEM CLK will load the write pointer into the Memory Address Counter (U19, 22, 26).

3. L=MEMORY CHIP ENABLE is set to high to bring all memory chips (U1-U16) out of the low power standby state.

4. L=WRITE DATA to U7 through U16 and L=WRITE PARAMETER BITS 1-6 to U1 through U6 will all be low to put Display Memory in the write mode.

5. Data on input lines D1-D10 and PARAMETER BIT 1-6 are written to the addressed Display Memory locations as the X Data Byte.

6. L=MEMORY CHIP ENABLE will go low.

7. L=MEM CLK will increment the Memory Address Counter one count.

8. L=MEMORY CHIP ENABLE will be returned high.

9. Data on data lines D1-D10 and PARAMETER BIT 1-6 are written to the addressed Display Memory locations as the Y Data Byte.

10. L=MEMORY CHIP ENABLE will go high.

11. L=MEM CLK will again increment the Memory Address Counter one count.

12. L=LOAD ADDR is brought high to gate the Memory Address Counter output through the Pointer Address Multiplexer.

13. L=STORE POINTER ADDR will go low, which writes the new X Data Byte address into the same location of the Pointer Address Memory that was read in the first step of this sequence.

Table 8-12. Coordinate and Text Words in Memory

Word Addr		Memory Addr	Coord/Text Data	Parameter
1	COORD WORD	0 1	X Data Byte: X Coordinate Y Data Byte: Y Coordinate	File Name Blanking Bits
2	TEXT WORD	2 3	X Data Byte: Text Flag Y Data Byte: ASCII+CS	File Name Blanking Bits

REFRESH

All Display Memory must be refreshed every 2 milliseconds so that data is not lost. Refresh is accomplished by cycling through the 64 addresses of the lower-order address inputs, A0 through A5, or by addressing every row of memory, A6 through A11, within any 2 millisecond period. Normally, all Display Memory will be addressed within 2 ms while operating in the DO VECTOR mode. However, when operating in Line Sync or drawing a series of large characters the refresh requirements may not be satifised. In this case the Control Board will initiate a Refresh Cycle. In the Refresh Cycle the Control Board will input the signals required to read the Refresh Pointer, increment the Memory Address Counter, and write the new Refresh Pointer into Pointer Address Memory.

The sequence of signals for the Refresh Cycle is as follows:

1. Input line POINTER SELECT 1 is pulled low and POINTER SELECT 2 is set high to address the refresh location of Pointer Address Memory (U18, 21, 24).

2. L=LOAD ADDRESS and a positive transistion of the L=MEM CLK will load the refresh pointer into the Memory.

3. L=MEMORY CHIP ENABLE is set high to bring all memory chips (U1-U16) out of the low power standby state.

4. L=MEMORY CHIP ENABLE is dropped low.

5. L=MEM CLK will increment the Memory Address Counter (U19, 22, 28) one count.

6. Steps 3 through 5 are repeated to address one X Data Byte location and one Y Data Byte location.

7. L=LOAD ADDRESS is brought high to gate the Memory Address Counter (U19, 22, 25) outputs through the Pointer Address Multiplexer (U17, 20, 23).

8. L=STORE POINTER ADDR will go low, which writes the new pointer address into Pointer Address Memory (U18, 21, 24). This cycle is repeated as necessary to insure all Display Memory locations are refreshed within a 2 ms period.

FILE NAME COMPARATOR

The File Name Comparator is a special function circuit on schematic 4A and is used when a FIND FILE signal is sent from the Control Board to the Display Board. The I/O instructions Find File, Blank File, Unblank File, Erase File, Blank Memory, Unblank Memory, and Find Location all cause the Control Board to produce the FIND FILE signal.

The file to be found must have been previously named and data stored in the file location for the file to exist. Should a Find File be attempted for a file that does not exist, the system will lock-up in a memory search operation.

The FIND FILE command causes the memory to be searched until a comparison is made between a name in memory and a Control Board input. The file to be found is "named" on data input lines D1 through D5. The sequence of signals for the find file operation is as follows:

1. A positive transistion on the FIND FILE signal input P1 pin 53 latches the "name" into the storage register U27.

2. L=MEMORY CHIP ENABLE is brought high to bring all memory chips (U1-U16) out of the low power standby state.

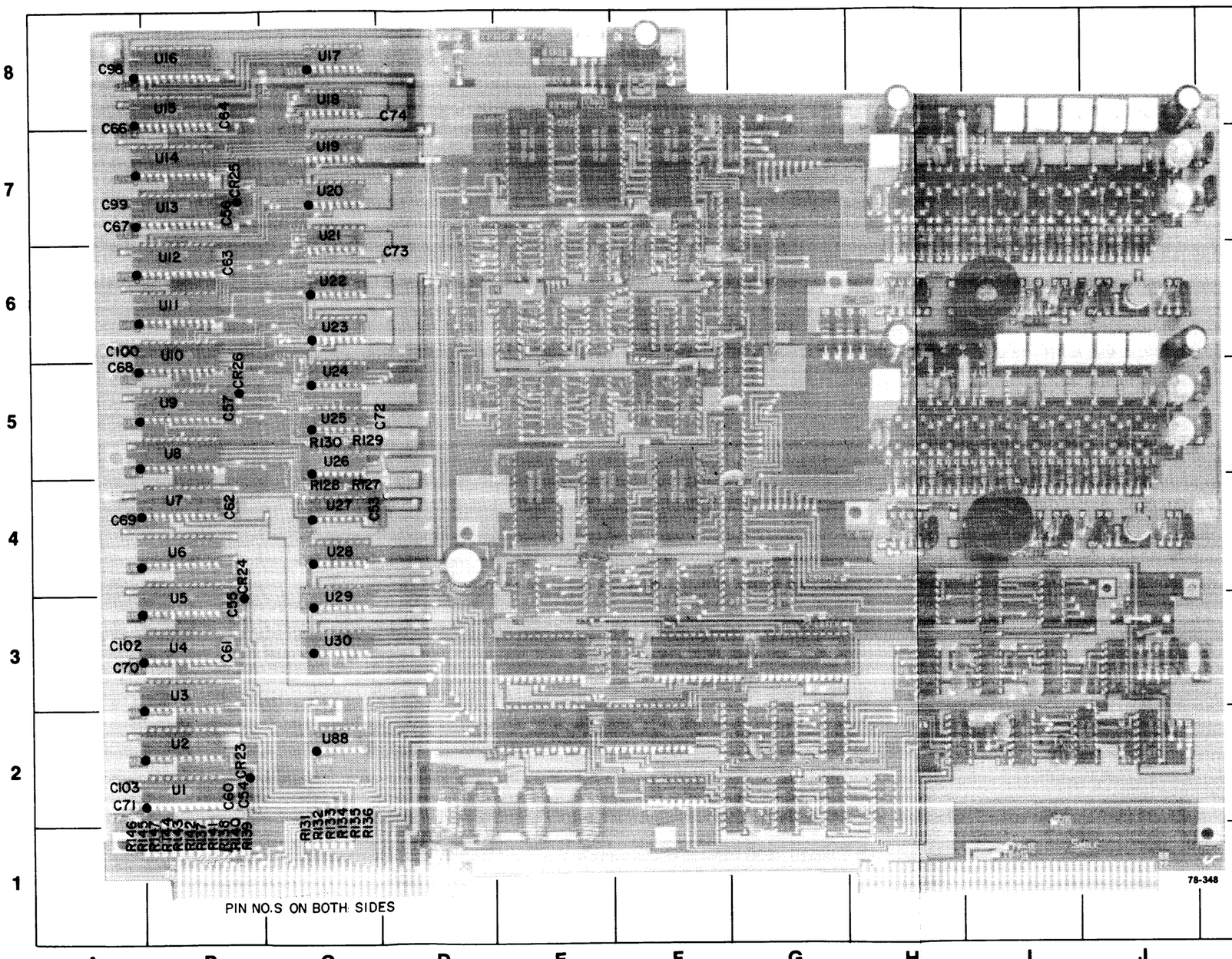
3. L=WRT PB1-5 are brought high to place U1-U5 in the read mode.

4. The data lines L=BO1 through L=BO5 are now compared in U28 with the stored D1-D5 "name".

5. If the values ("names") are identical a H=FILE FOUND is sent from U28 to the Control Board.

6. If the values did not compare the Memory Address Counter (U19, 22, 25) is incremented and a comparison is made at the next memory location.

7. When the file has been found the Control Board will write the memory address of the file into the Pointer Address Memory (U18, 21, 24) as a Write Pointer.



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C54	B-2	R139	B-1
C55	B-4	R140	B-1
C57	B-5	R141	B-1
C60	B-2	R142	B-1
C61	B-3	R143	B-1
C62	B-4	R144	B-1
C63	B-6	R145	A-1
C64	B-8	R146	A-1
C65	B-7	R147	B-1
C66	A-8	U1	B-2
C67	A-7	U2	B-2
C68	A-5	U3	B-3
C69	A-4	U4	B-3
C70	A-3	U5	B-4
C71	A-2	U6	B-4
C72	C-5	U7	B-4
C73	D-6	U8	B-5
C74	D-8	U9	B-5
C91	D-5	U10	B-6
C92	D-4	U11	B-6
C98	A-8	U12	B-6
C99	A-7	U13	B-7
C100	A-6	U14	B-7
C102	A-3	U15	B-8
C103	A-2	U16	B-8
CR23	B-2	U17	C-8
CR24	B-4	U18	C-8
CR25	B-7	U19	C-7
CR26	B-5	U20	C-7
R127	C-4	U21	C-7
R129	C-5	U22	C-6
R130	C-5	U23	C-6
R131	C-1	U24	C-5
R132	C-1	U25	C-5
R133	C-1	U26	C-5
R134	C-1	U27	C-4
R135	C-1	U28	C-4
R136	C-1	U29	C-3
R137	B-1	U30	C-3
R138	B-1	U88	C-2

Figure 8-31. Component Locator for Schematic 4A

Mnemonics on Display Board A4

A0 — Memory Address Bit 0 — Serves important functions on both the Display and Control Boards. It is used on the Display Board to determine when x or y information is being read or written. It determines the configuration of RAM for storage. On the Control Board it is a multiplex select line to determine whether File Name bits or Blanking bits are sent to memory. During x-time (A0 = low) File Names are selected and during y-time (A0 = high) Blanking information is selected. When selecting which type of data, A0 also determines the read/write status of the memories by means of the Memory Read/ Write Controller.

D1-D13 — Data Bits 1-12 transfer data lines between the Control Board and Pointer Address Multiplexer. D13 is not used.

H = FILE FOUND — File name information from the data lines is compared with those stored in the Parameter Memories. When a match occurs, H = FILE FOUND goes high.

L = BLANK CHAR — Blanks the beam between characters. Drives the Z-axis Blanking Controller.

L = BLANK VECTOR — Blanks the vector beam between non-connected points.

L = CHAR — Selects P = CHAR LATCH X and P = CHAR LATCH Y through Vector Generator Controller U3 (Schematic 3D) and causes these signals to transfer each stroke to the Vector Generator. Low only when the data is text, as controlled by the Character Generator.

L = CHAR HOLDOFF — Swings low after a character is detected to allow time for the text code to be decoded. Prevents any output from the Character Generator.

L = CHAR OUTPUT ENABLE — After L = CHAR has occurred there is a delay provided by the C12 - U16D combination (schematic 3D). This allows time for text data to be latched to the Character Generator and decoded (L = CHAR HOLDOFF helps in this latter function). The low level of L = CHAR OUTPUT ENABLE enables the character output selectors U12, 13, 14 and 26 (schematic 5) and causes the character data to be sent to the Vector Generator.

L = INTERFACE HOLDOFF — Inhibits further vector generation until the 1338A display can assimilate the data it has. Low inhibits, high continues.

L = LOAD ADDR — Active low loads pointer address into memory.

L = MEM CHIP ENABLE — Enables U26 Memory Chip Enable Drive (Schematic 4A) which allows Parameter Memory and Vector Memory RAMs to load data.

L = MEM OUTPUT ENABLE — Enables memory output drivers U29 and U30 (schematic 4A). This is the all encompassing write line which enables both Parameter and Vector Memories.

L = VECTOR BUSY — Indicates that data is being translated into analog form in the D/A Converter. When high, the Vector Generator is processing available values and has not sent them to the D/A.

L = VECTOR INHIBIT — Holds the Vector Generator in a reset condition in which it cannot process or output data.

L = WRITE DATA — Write enable for the Vector Memory RAMs. Enables only the Vector Memories.

L = WRITE PB1-PB6 — Write Display Parameter Bits — Write enables lines for only the Parameter Memories — can be used to write to individual memories depending on requirements.

N = CLR ADDR — Negative transition clears all memory address counters.

N = LOAD ADDR CTR — Causes the address value from the pointer register to be transferred to the Memory Address Counter.

N = MEMORY CLK — Clock for the Memory Address Counters.

N = STORE POINTER ADDR — Stores the next x address.

P = CHAR LATCH X — Latches each Char Stroke to the Vector Generator (x).

P = CHAR LATCH Y — Latches each Char Stroke to the Vector Generator (y).

P = FIND FILE — Frame and File Detector (schematic 3A) is enabled by any of the control instructions that state BLANK, ERASE, UNBLANK, or FIND. This causes a new file name to be latched into the File Name Comparator.

P = LATCH X — Clocks the x data into the Vector Generator.

P = LATCH Y — Clocks the y data into the Vector Generator.

P = X ADDR — Used to latch File Name Bits PBO5 and 6 into Color Bits Latch U65A. Also used to generate Color Valid Signal for 1338A Tri-color Display.

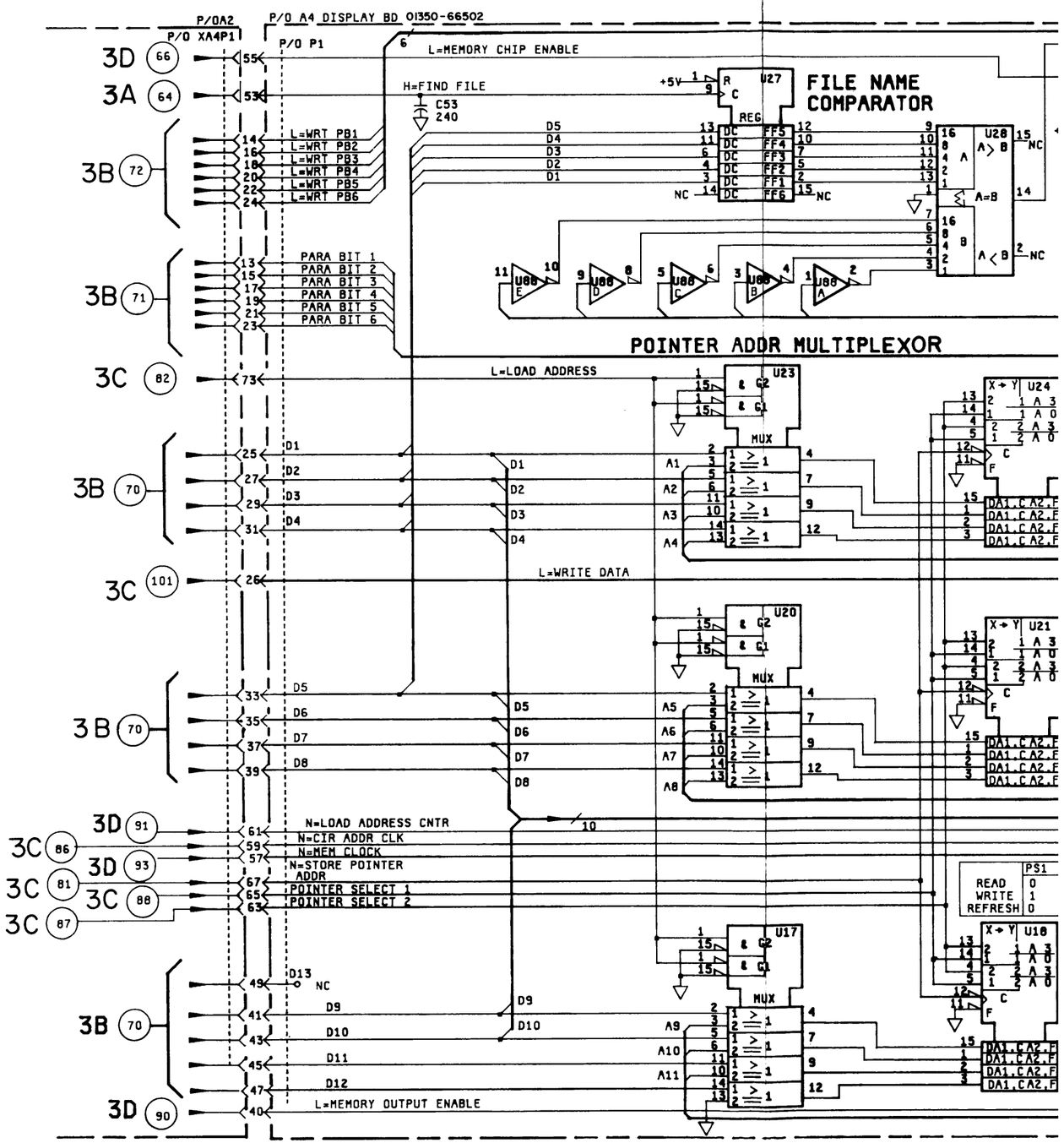
P = Y ADDR — Inverted and used as clock for TTL Blanking Latch U67. This latches information from File Name Bits PBO3-6 to determine which of 4 TTL outputs will be high (blanked).

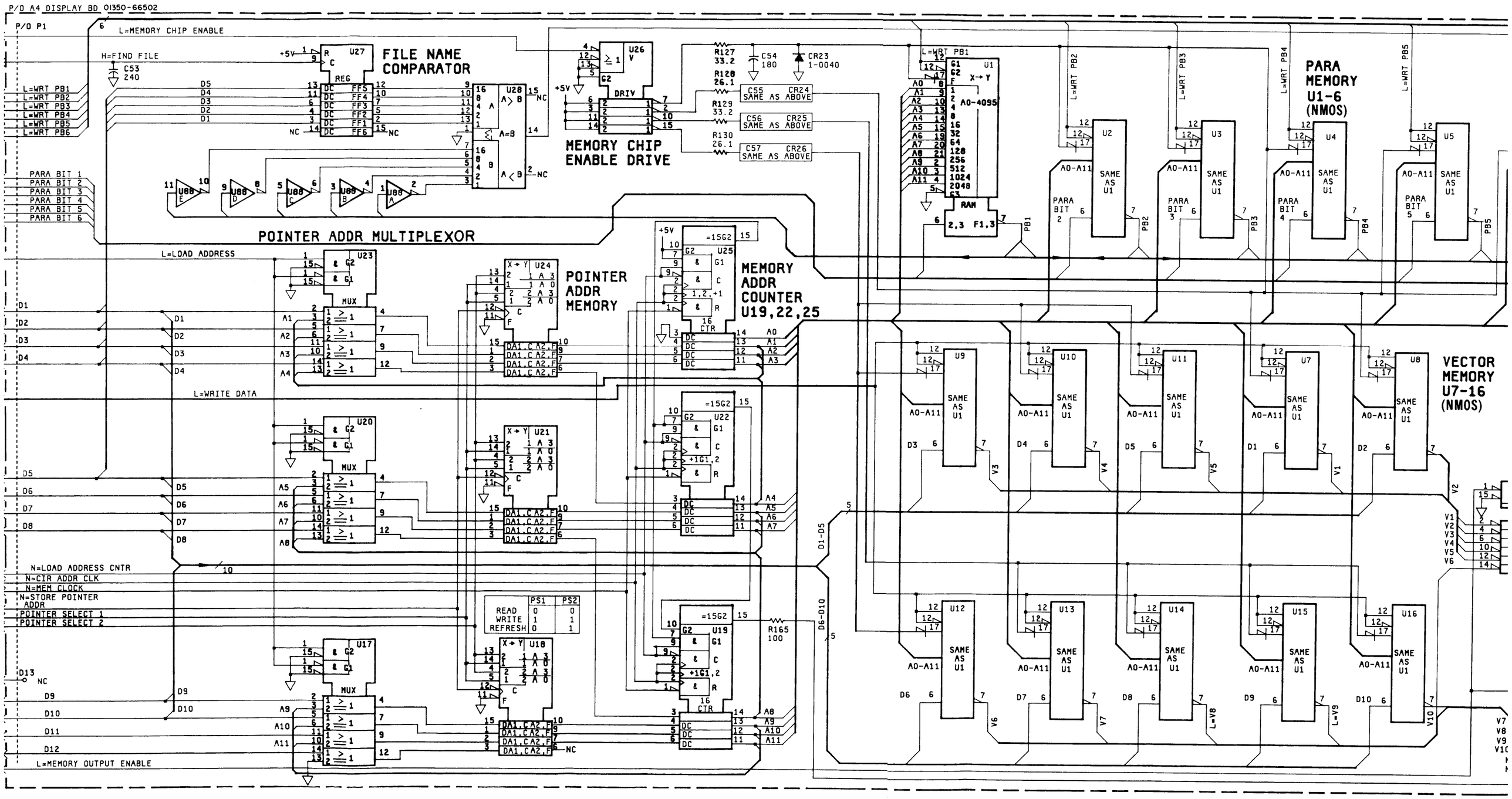
PARA BITS 1-6 — Parameter Bits - carries parameter information to the Parameter Memories. A0 determines the contents. When A0 = low (x-time) the Para Bits carry File Name data. When A0 = high (y-time) they carry "Pen Enable," "File Blanking," and "Auxiliary Bits."

PBO1-PBO5 — Name Bits — See Section 8 - 1350 Memory Organization, for more complete explanation.

POINTER SEL 1&2 — Generated from DO VECTOR, WRITING and STORE WRITE POINTER. These are the address lines to the four bit pointer register stack in Display Memory (U18, U21, and U24 on schematic 4A).

Z0-Z4 — Blanking Level Bits - carries information on the intensity of the vectors to the z-axis Level Controller.




P/O A4 DISPLAY BD 01350-66502
P/O P1
L=MEMORY CHIP ENABLE
H=FIND FILE
C53 240
FILE NAME COMPARATOR
MEMORY CHIP ENABLE DRIVE
R127 33.2
R128 26.1
R129 33.2
R130 26.1
C54 180
CR23 1-0040
C55 CR24 SAME AS ABOVE
C56 CR25 SAME AS ABOVE
C57 CR26 SAME AS ABOVE
PARA MEMORY U1-6 (NMOS)
POINTER ADDR MULTIPLEXOR
L=LOAD ADDRESS
POINTER ADDR MEMORY
MEMORY ADDR COUNTER U19,22,25
L=WRITE DATA
VECTOR MEMORY U7-16 (NMOS)
N=LOAD ADDRESS CNTR
N=CIR ADDR CLK
N=MEM CLOCK
N=STORE POINTER ADDR
POINTER SELECT 1
POINTER SELECT 2
READ WRITE REFRESH
PS1 PS2
R165 100
L=MEMORY OUTPUT ENABLE
SAME AS U1
PARA BIT 1
PARA BIT 2
PARA BIT 3
PARA BIT 4
PARA BIT 5
PARA BIT 6
L=WRT PB1
L=WRT PB2
L=WRT PB3
L=WRT PB4
L=WRT PB5
L=WRT PB6

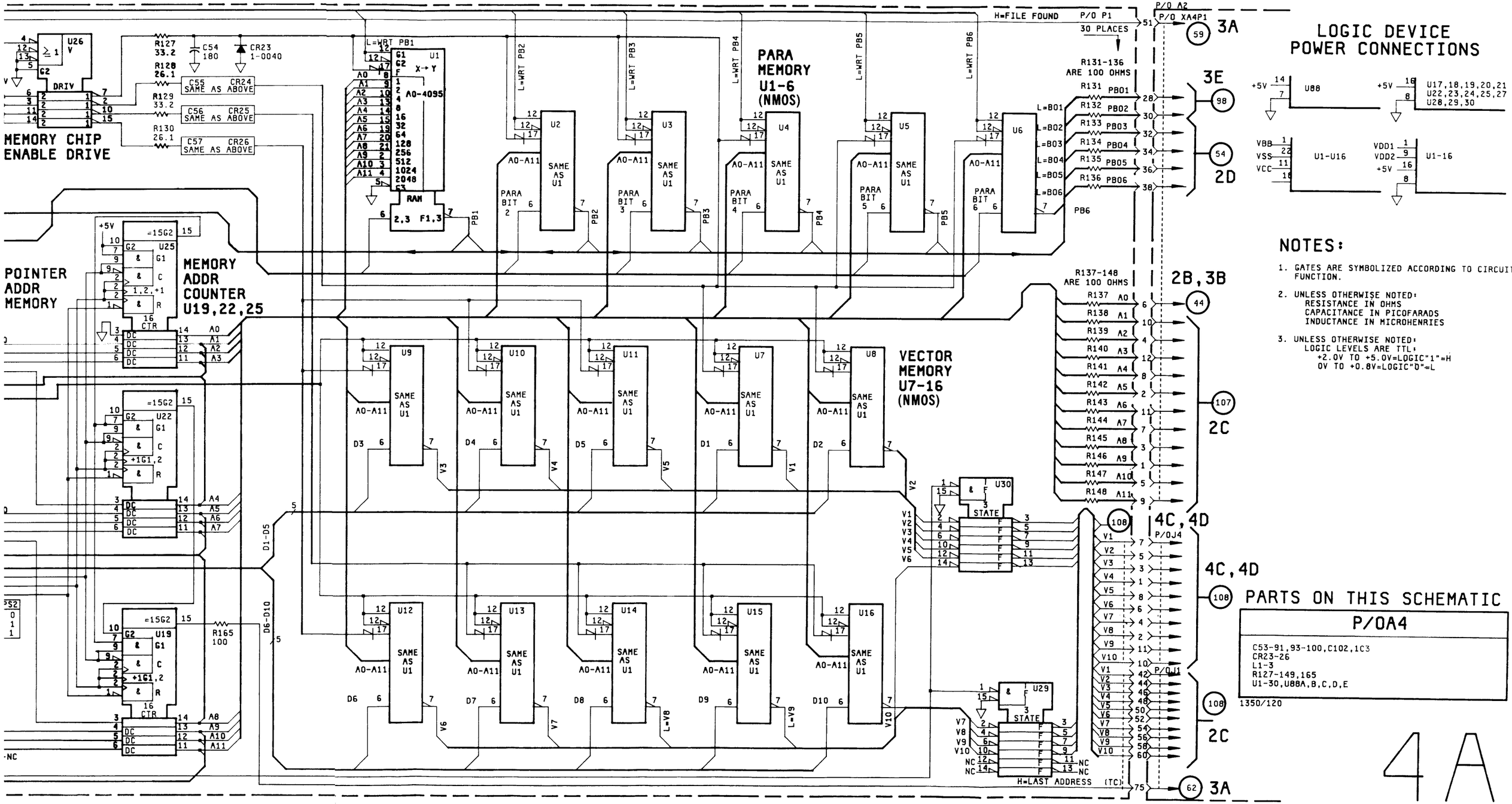


Figure 8-32. Schematic 4A

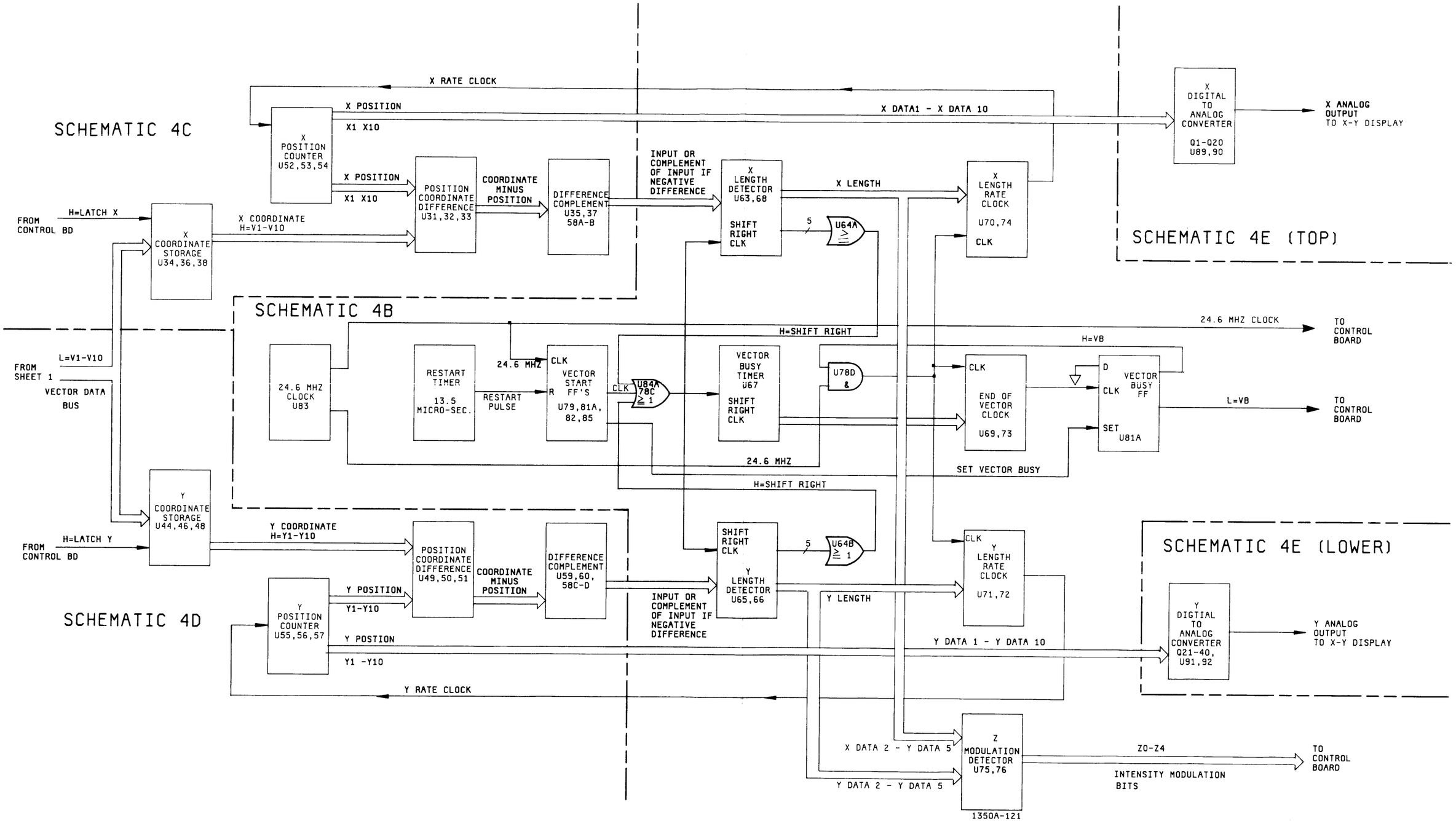


Figure 8-33. Simplified Block Diagram for Schematics 4B-4E

8-80. SCHEMATIC 4B PRINCIPLES OF OPERATION.

Schematic 4B contains:

1. X and Y Vector Length Detectors.
2. X and Y Length-Rate Clock circuits.
3. End of Vector Clock circuit.
4. 24.6 MHz Clock.
5. Restart Timer.
6. Z Intensity Modulation Detector.
7. Start Vector Flip-Flops.
8. Vector Busy Flip-Flops.

Operation of the circuits on schematic 4B will be covered as follows:

Case 1 - Special Hardware
Case 2 - Vector Generation

8-81. CASE 1. SPECIAL HARDWARE.

8-BIT SHIFT REGISTERS (U63 and U65-U68).

The 8-Bit Shift Registers are used as the X Vector Length Detector (U63, U68), Y Vector Length Detector (U65, U66), and the End of Vector Clock circuit (U67). These devices provide a parallel load, a shift right, and a shift left function. During normal operation only the parallel load and shift right function are used; the other functions are included in this discussion as an aid to troubleshooting. The functions are under control of pins 1 and 23 as follows:

1. Pins 1 and 23 are both high, the device is in a parallel load function. The data on input pins 3, 5,7,9,15,17,19, and 21 is available on the eight output pins after a positive transistion on the clock input pin 11.

2. Pin 1 is high and pin 23 is low, the device is in a shift right function and data is shifted right (top to bottom on schematic 4B) one data cell with each positive transition of the clock input pin 11 (the shift right serial input is pin 2).

3. Pin 1 is low and Pin 23 is high, the device is in the shift left function and data is shifted left (bottom to top on schematic 4B) one data cell with each positive transistion of the clock on pin 11 (the shift left serial input is pin 22).

4. Pins 1 and 23 are both low, the device will inhibit the clocking action of pin 11.

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIERS (U69-U74)

The Synchronous 6-Bit Binary Rate Multipliers are used in the X Length-Rate Clock (U70, U74), Y Length-Rate Clock (U71, U72), and the End of Vector Clock circuit (U69, U73). These devices operate as follows: Parallel input data is applied to pins 3,2,15,14,1, and 4 which effectively divide the clock input on pin 9 by 2,4,8, 16,32 and 64 respectively. The clock input (pin 9) is gated with the parallel data inputs in such a manner that the output (pin 5) serial pulse train is proportional to the parallel input data. A timing diagram (figure 8-34) shows the relationship of the output pulses (pin 5) to the input clock (pin 11). Waveforms 1 through 6 show the outputs on pin 5 for each of the conditions where one, and only one, of the parallel inputs are active (high). When more than one of the parallel inputs are active their outputs (waveforms 1 through 6) are "ORed" together. As an example, with input pins 1 and 4 active a pulse is output on the 16th, 32nd, and 48th clock pulses as shown by waveform 7. Many combinations of active inputs are possible and the output will be different for each combination. During the period of the 64th clock cycle the "enable output" pin 7 will be low. After the 64th clock cycle the device is in a reset or start condition.

8-82. CASE 2. VECTOR GENERATION.

Refer to figure 8-35 and Schematic 4B throughout this discussion.

The 24.6 MHz Clock is a constantly running clock circuit and is the basis for all timing of the circuits of schematic 4B.

After the Vector Data has been read from memory and processed by the circuits of schematics 4C and 4D, an absolute length value for the X and Y Vectors is available as the parallel inputs to the X (U63,U68) and Y (U65,U66) Vector Length Detectors. The Vector Start Flip-Flops will begin their start sequence on the positive transistion of the first 24.6 MHz clock, which will set U82 pin 9 high. U82 pin 9 going high will clock U79B to the set state. With U79 pin 9 high the "D" input to U85B is enabled. U85B will set with the second positive transistion of U82 pin 9 (third 24.6 MHz clock) if L=VECTOR INHIBIT from the Control Board is high. U85B when set will place a low on the reset input of U82A, which will then fire the Restart Timer. When U85B is set it also enables the parallel load function of all Shift Registers (U63 and U65-U68). Data will be parallel loaded into the Shift Registers on the third positive transistion of U82 pin 9. The fourth positive transistion of U82 pin 9 will reset U85B and clock U85A into the set condition.

The data now contained in the X Vector Length Detector is the absolute distance the pen (beam) must move in the X plane and the Y Vector Length Detector contains the absolute distance the pen must move in the Y Plane. If either of these distances is 1/32 screen length or greater, one or more right shifts will take place. A Vector length of 1/32 screen or greater but less than 1/16 screen will load a high on output pin 14 of U63 or U65. A Vector length of 1/16 or greater but less than 1/8 screen will produce a high on output pin 10. A length of 1/8 screen or greater but less than 1/4 screen will produce a high on pin 8. A length of 1/4 screen or greater but less than 1/2 screen will produce a high on pin 6. A length of 1/2 screen or greater will produce a high on pin 4.

If a high is present on any input to U64A or U64B all Shift Registers are in the Shift Right function. A Shift Right will occur with each positive transistion of U82 pin 9 as long as any high is input to U64A or U64B. With each Shift Right operation the data is moved down in the Shift Register one data cell and a low is loaded into the top data cell. When all "ones" have been shifted out of the first five data cells, U81B is set with the next positive transition of U82 pin 9. The low on U81 pin 8 will force set the Vector Busy Flip-Flop removing the force set from U79A, and enable U78D. 24.6 MHz clocks are now available to the End of Vector Clock and Length-Rate Clock circuits.

The X and Y Length-Rate Clock circuits now output a pulse train (see timing diagram 1) to schematics 4C and 4D to increment/decrement the position counters. The End of Vector Clock circuit will clock the Vector Busy FF reset after the predetermined maximum vector length time has been reached. If no shift right operations occurred (<1/32 screen length vectors) U69 will count 32 of the 24.6 MHz clocks and output a low on pin 5. If one or more shift operations occurred, U69 will count 64 of the 24.6 MHz clocks and output a low on pin 7 allowing the next 24.6 MHz clock to toggle U79A. One 24.6 MHz clock is routed (U86A) to U73, then U79A is toggled back to its original state. If one shift had occurred the Vector Busy Flip-Flop will be reset after 64 clocks (U73 pin 5 going low). If more than one shift had occurred, the sequence repeats until the maximum count of 1024 clocks. After 1024 clocks the Vector Busy Flip-Flop must be reset.

When the Vector Busy Flip-Flop goes set, Z Intensity Modulation data is available to the Control Board.

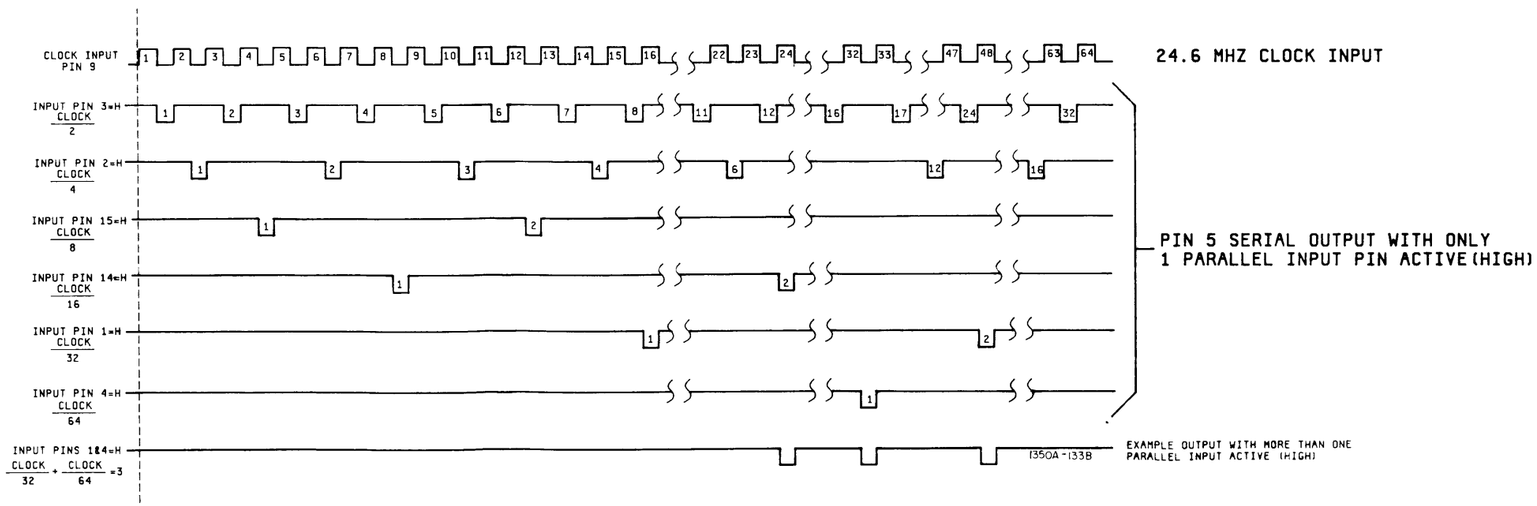


Figure 8-34. Rate Multiplier Timing Diagram

RATE MULTI-

ltipliers are used
), Y Length-Rate
tor Clock circuit
follows: Parallel
4,1, and 4 which
1 9 by 2,4,8, 16,32
n 9) is gated with
er that the output
al to the parallel
8-34) shows the
to the input clock
he outputs on pin
and only one, of
When more than
re their outputs
together. As an
a pulse is output
ses as shown by
ictive inputs are
ferent for each
64th clock cycle
ter the 64th clock
ondition.

N.

throughout this

ning clock circuit
uits of schematic

After the Vector Data has been read from memory and processed by the circuits of schematics 4C and 4D, an absolute length value for the X and Y Vectors is available as the parallel inputs to the X (U63,U68) and Y (U65,U66) Vector Length Detectors. The Vector Start Flip-Flops will begin their start sequence on the positive transistion of the first 24.6 MHz clock, which will set U82 pin 9 high. U82 pin 9 going high will clock U79B to the set state. With U79 pin 9 high the "D" input to U85B is enabled. U85B will set with the second positive transistion of U82 pin 9 (third 24.6 MHz clock) if L=VECTOR INHIBIT from the Control Board is high. U85B when set will place a low on the reset input of U82A, which will then fire the Restart Timer. When U85B is set it also enables the parallel load function of all Shift Registers (U63 and U65-U68). Data will be parallel loaded into the Shift Registers on the third positive transistion of U82 pin 9. The fourth positive transistion of U82 pin 9 will reset U85B and clock U85A into the set condition.

The data now contained in the X Vector Length Detector is the absolute distance the pen (beam) must move in the X plane and the Y Vector Length Detector contains the absolute distance the pen must move in the Y Plane. If either of these distances is 1/32 screen length or greater, one or more right shifts will take place. A Vector length of 1/32 screen or greater but less than 1/16 screen will load a high on output pin 14 of U63 or U65. A Vector length of 1/16 or greater but less than 1/8 screen will produce a high on output pin 10. A length of 1/8 screen or greater but less than 1/4 screen will produce a high on pin 8. A length of 1/4 screen or greater but less than 1/2 screen will produce a high on pin 6. A length of 1/2 screen or greater will produce a high on pin 4.

If a high is present on any input to U64A or U64B all Shift Registers are in the Shift Right function. A Shift Right will occur with each positive transistion of U82 pin 9 as long as any high is input to U64A or U64B. With each Shift Right operation the data is moved down in the Shift Register one data cell and a low is loaded into the top data cell. When all "ones" have been shifted out of the first five data cells, U81B is set with the next positive transition of U82 pin 9. The low on U81 pin 8 will force set the Vector Busy Flip-Flop removing the force set from U79A, and enable U78D. 24.6 MHz clocks are now available to the End of Vector Clock and Length-Rate Clock circuits.

The X and Y Length-Rate Clock circuits now output a pulse train (see timing diagram 1) to schematics 4C and 4D to increment/decrement the position counters. The End of Vector Clock circuit will clock the Vector Busy FF reset after the predetermined maximum vector length time has been reached. If no shift right operations occurred (<1/32 screen length vectors) U69 will count 32 of the 24.6 MHz clocks and output a low on pin 5. If one or more shift operations occurred, U69 will count 64 of the 24.6 MHz clocks and output a low on pin 7 allowing the next 24.6 MHz clock to toggle U79A. One 24.6 MHz clock is routed (U86A) to U73, then U79A is toggled back to its original state. If one shift had occurred the Vector Busy Flip-Flop will be reset after 64 clocks (U73 pin 5 going low). If more than one shift had occurred, the sequence repeats until the maximum count of 1024 clocks. After 1024 clocks the Vector Busy Flip-Flop must be reset.

When the Vector Busy Flip-Flop goes set, Z Intensity Modulation data is available to the Control Board.

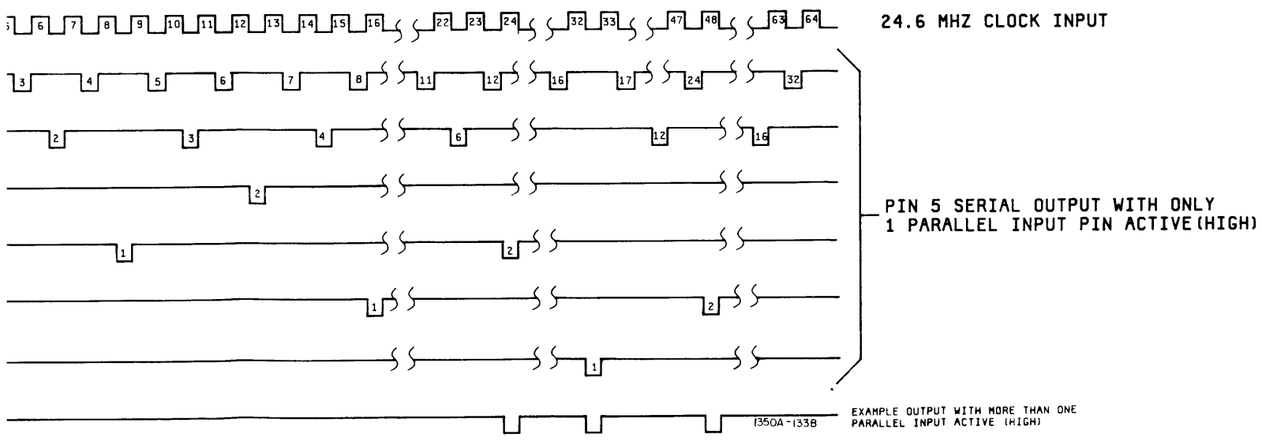


Figure 8-34. Rate Multiplier Timing Diagram

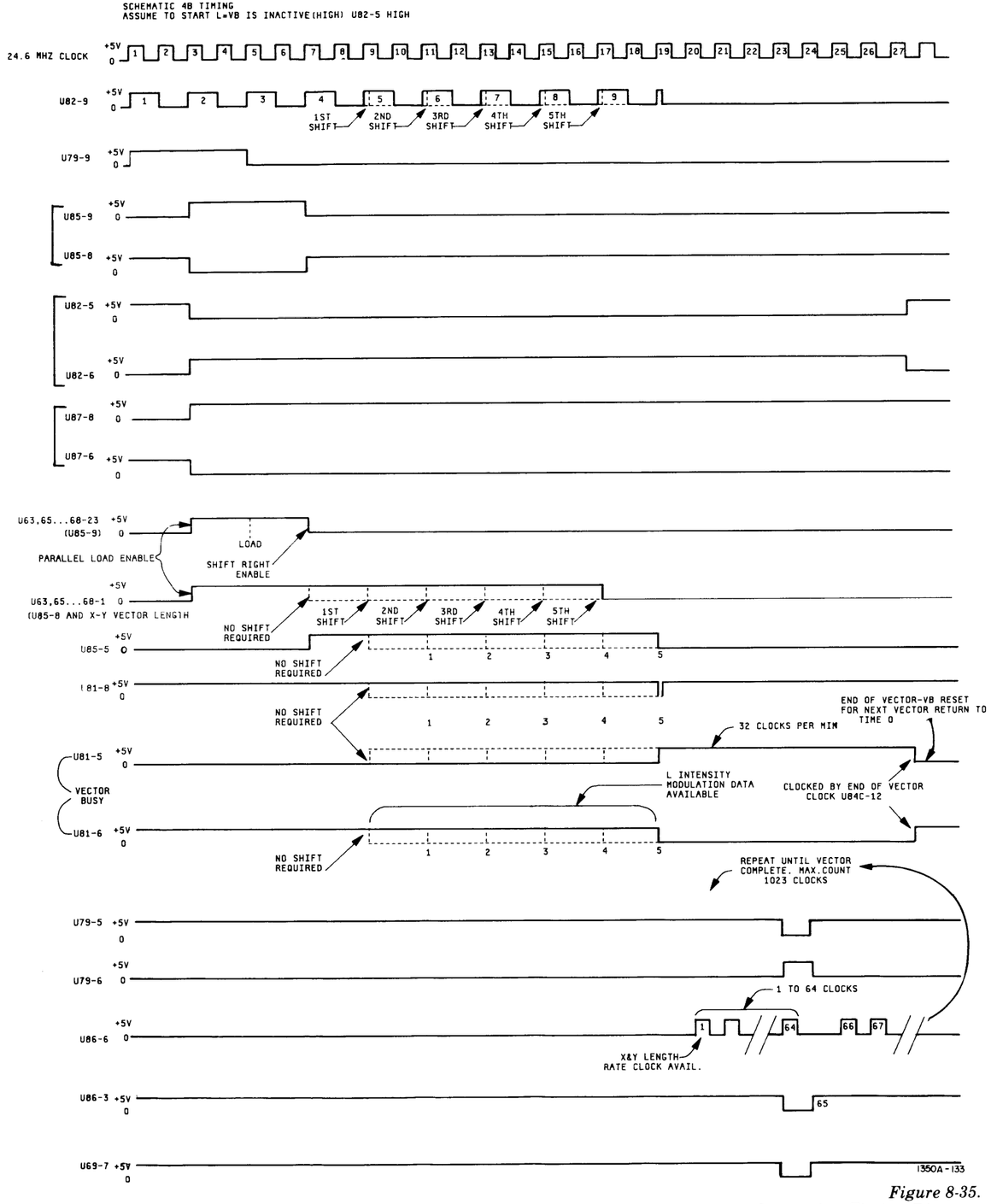
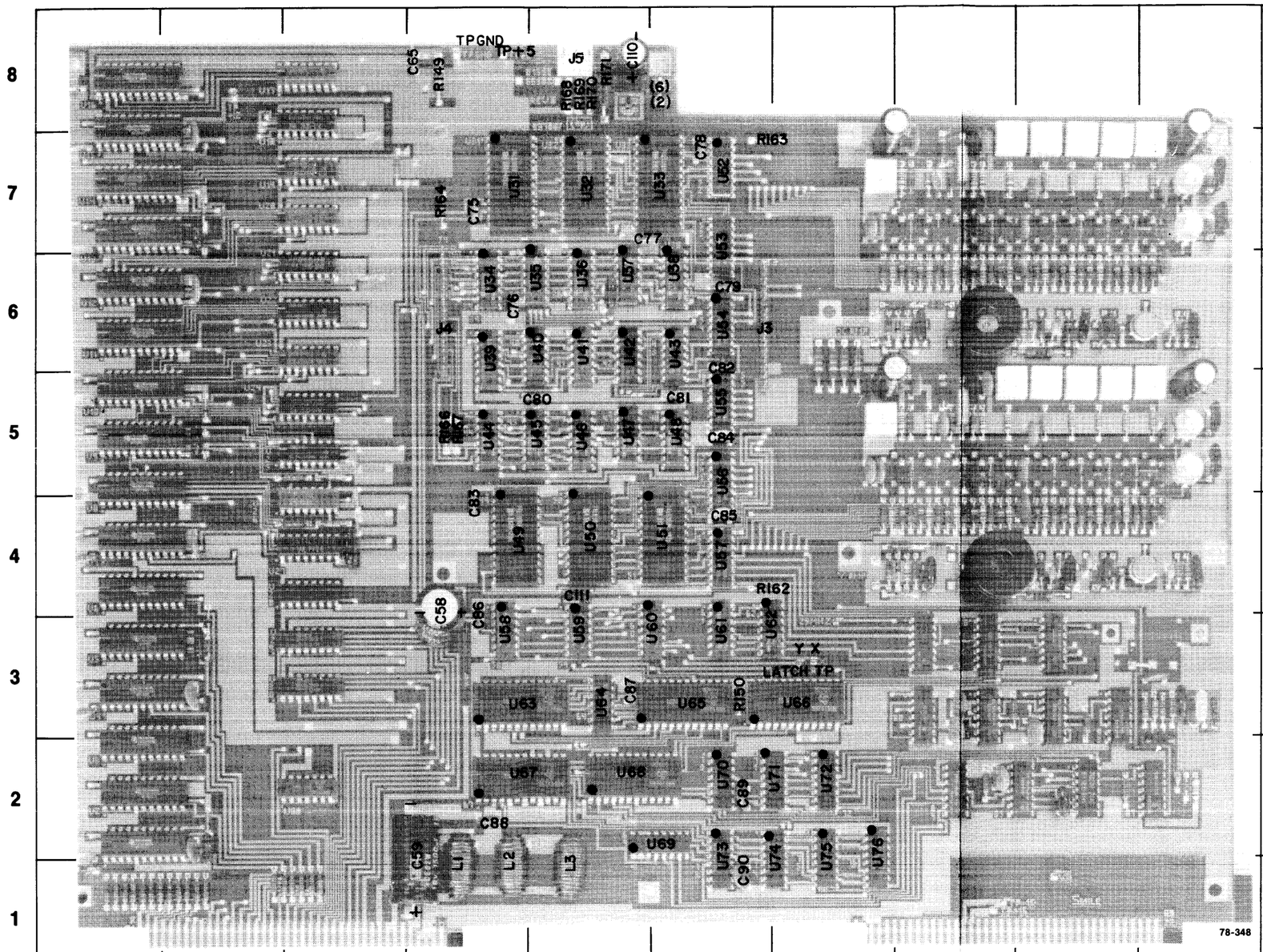
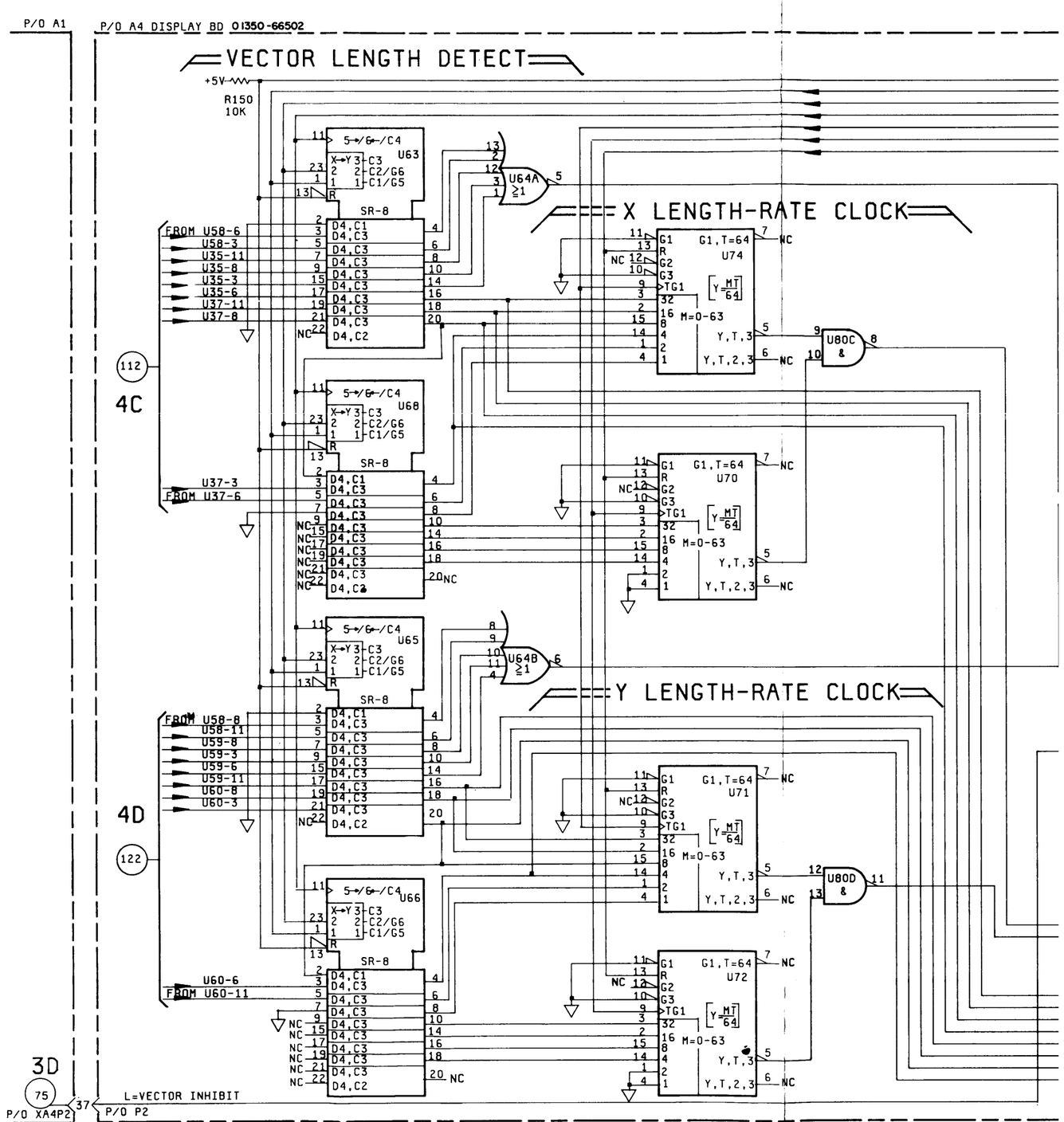


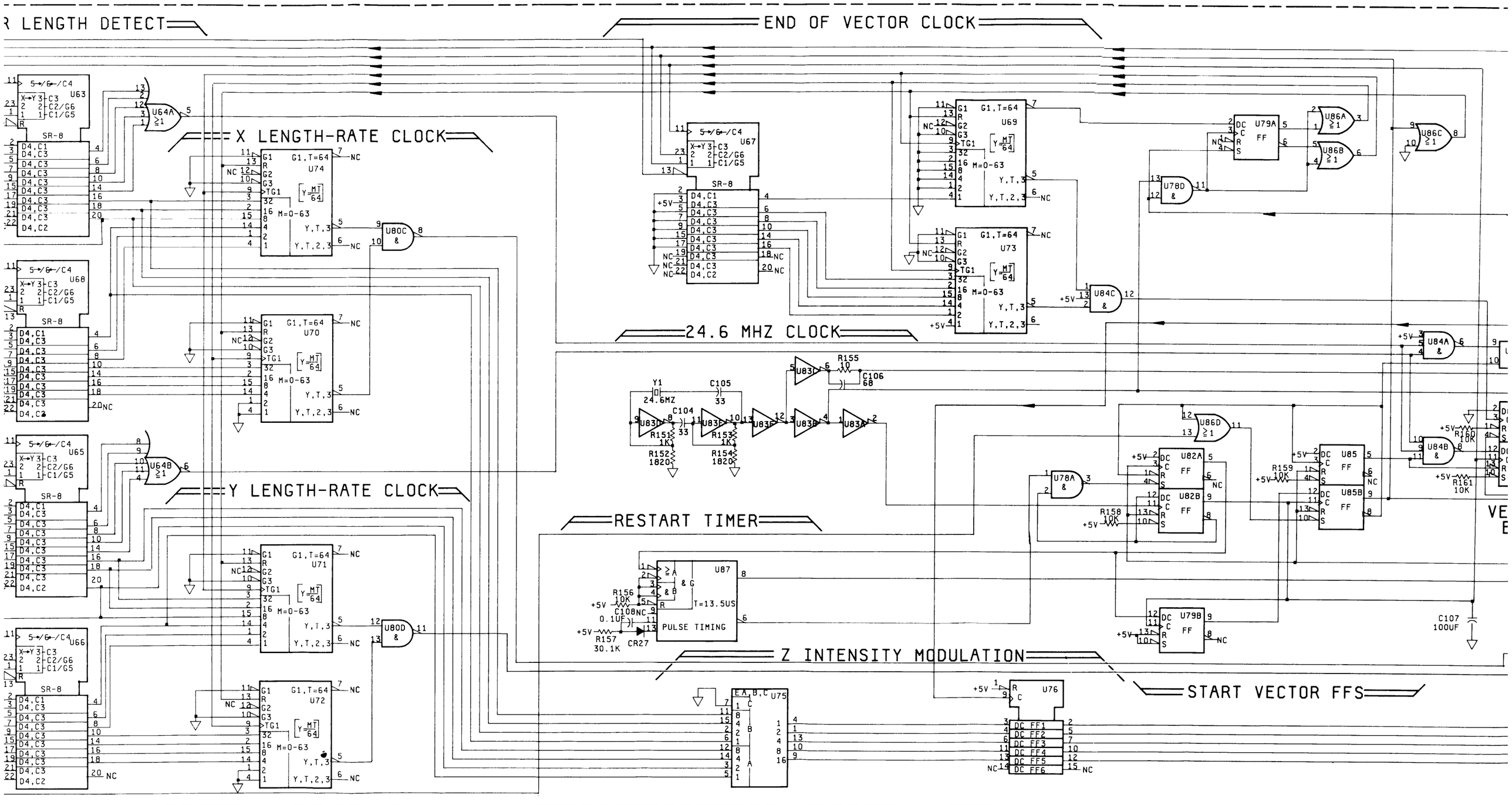
Figure 8-35. Vector Generation Timing Diagram



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C58	D-4	U35	E-6
C59	D-2	U36	E-6
C65	D-8	U37	E-6
C73	D-7	U38	F-6
C76	D-6	U39	D-6
C77	E-7	U40	E-6
C78	F-7	U41	E-6
C79	F-6	U42	E-6
C80	E-5	U43	F-6
C81	F-5	U44	D-5
C82	F-6	U45	E-5
C83	D-4	U46	E-5
C84	F-5	U47	E-5
C85	F-4	U48	F-5
C86	D-3	U49	D-4
C87	E-3	U50	E-4
C88	D-2	U51	F-4
C89	F-2	U52	F-7
C90	F-1	U53	F-6
C110	E-8	U54	F-6
C111	E-4	U55	F-5
J3	F-6	U56	F-5
J4	D-6	U57	F-4
L1	D-1	U58	D-3
L2	D-1	U59	E-3
L3	E-1	U60	F-3
R149	D-8	U61	F-3
R150	F-3	U62	F-3
R162	F-4	U63	D-3
R163	F-7	U64	E-3
R164	D-7	U65	F-3
R166	D-5	U66	G-3
R167	D-5	U67	D-2
R168	E-8	U68	E-2
R169	E-8	U69	E-2
R170	E-8	U70	F-2
R171	E-8	U71	G-2
TP5	D-8	U72	G-2
U31	D-7	U73	F-2
U32	E-7	U74	G-2
U33	F-7	U75	G-2
U34	D-6	U76	G-2

Figure 8-36. Component Locator for Schematic 4B, part of Schematic 4C, and Schematic 4D


P/O A1
P/O A4 DISPLAY BD 01350-66502
VECTOR LENGTH DETECT
+5V
R150
10K
U63
U64A
≥1
X LENGTH-RATE CLOCK
FROM U58-6
U58-3
U35-11
U35-8
U35-3
U35-6
U37-11
U37-8
112
4C
U68
U37-3
FROM U37-6
U74
U70
U80C
&
U64B
≥1
Y LENGTH-RATE CLOCK
FROM U58-8
U58-11
U59-8
U59-3
U59-6
U59-11
U60-8
U60-3
4D
122
U65
U66
U60-6
FROM U60-11
U71
U72
U80D
&
3D
75
P/O XA4P2
37
L=VECTOR INHIBIT
P/O P2



R LENGTH DETECT
END OF VECTOR CLOCK
X LENGTH-RATE CLOCK
24.6 MHZ CLOCK
Y LENGTH-RATE CLOCK
RESTART TIMER
Z INTENSITY MODULATION
START VECTOR FFS
PULSE TIMING

END OF VECTOR CLOCK

24.6 MHZ CLOCK

RESTART TIMER

Z INTENSITY MODULATION

START VECTOR FFS

P/O A2

LOGIC DEVICE POWER CONNECTIONS

VCC 14 / 7 — U78-87

VCC 16 / 8 — U69-76

VCC 24 / 12 — U63-68

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

24.6MHZ P/O P2 71 — P/O XA4P2 55 — 2D,3C TO I/O & CONTROL BD.

24.6MHZ XA6P1 4 — P/O P1 55 — 5 TO CHAR.GEN.BOARD

L=VB TO U77-8 — 51 — 4D

U77-11 — 51 — 4C

PO P2 69 — XA4P2 51 — 2D,3C TO I/O & CONTROL BD.

POXA6P1 8 — P/O P1 51 — 5 TO CHAR.GEN.BOARD

TO U45-4 — 124 — 4D

H= RESTART POXA6P1 3 — P/O P1 125 — 5

X RATE CLOCK TO U80-2 — 119 — 4C

Y RATE CLOCK TO U80-4 — 123 — 4D

Z INTENSITY BIT 0
Z INTENSITY BIT 1
Z INTENSITY BIT 2
Z INTENSITY BIT 3
Z INTENSITY BIT 4
P/O P2 — XA4P2 — 105 — 3E TO CONTROL BOARD

PARTS ON THIS SCHEMATIC

P/O A4

C104,105,106,107,108
CR27
R150-161,
U63-76,78A,D,C,79,80C,D,81,82,83A-F,84B,C,A,
U85,86A,B,C,D,87
Y1

1350/105

4B

Figure 8-37. Schematic 4B

8-83. SCHEMATIC 4C PRINCIPLES OF OPERATION.

Schematic 4C contains:

1. X Coordinate Storage.
2. X Position Counter.
3. X Position-Coordinate Difference circuit.
4. X Position Clock Control.

Operation of the circuits on Schematic 4C will be covered for two cases: (1) Vector Generation; and (2) Character Generation.

8-84. CASE 1. VECTOR GENERATION.

When an X Coordinate value is available from memory on the V1-V10 data bus a H=LATCH X pulse will be input from the Control Board and latch that value into U34, U36, and U38, the X Coordinate Storage register.

After the coordinate is latched, a one's complement subtraction takes place in the X Position-Coordinate Difference circuit (U31, U32, U33). The subtraction is an A minus B operation. That is, the actual pen (beam) position (B) is subtracted from the input coordinate (A). The result of the subtraction is the absolute distance the pen must move in the X plane. If the pen is to move toward the right of the screen the result of the subtraction will be a positive number and U31 pins 11 and 16 will remain low. If the pen is to move toward the left of the screen the result of the subtraction will be a negative number and U31 pins 11 and 16 will be high.

With U31 pins 11 and 16 low the Exclusive OR gates (U35, U37, U58A and U58B) have no effect on the data and their outputs are identical to their inputs. The low on U31 pin 11 via U41 pin 6 on schematic 4D will place the X Position Counter in an up-count mode. When U31 pins 11 and 16 are high the Exclusive ORs will complement the data and the X Position Counter is in the down-count mode.

The output data of the Exclusive ORs (U35, U37, U58A, and U58B) is further processed on schematic 4B which will return a RATE CLOCK (U80-2) to increment or decrement the X Position Counter. Only the correct number of clocks will be input to the X Position Counter to move the pen the absolute distance required. The contents of the X Position Counter is sent (H=XDATA1 through H=XDATA10) to the X Digital To Analog Converter, schematic 4E.

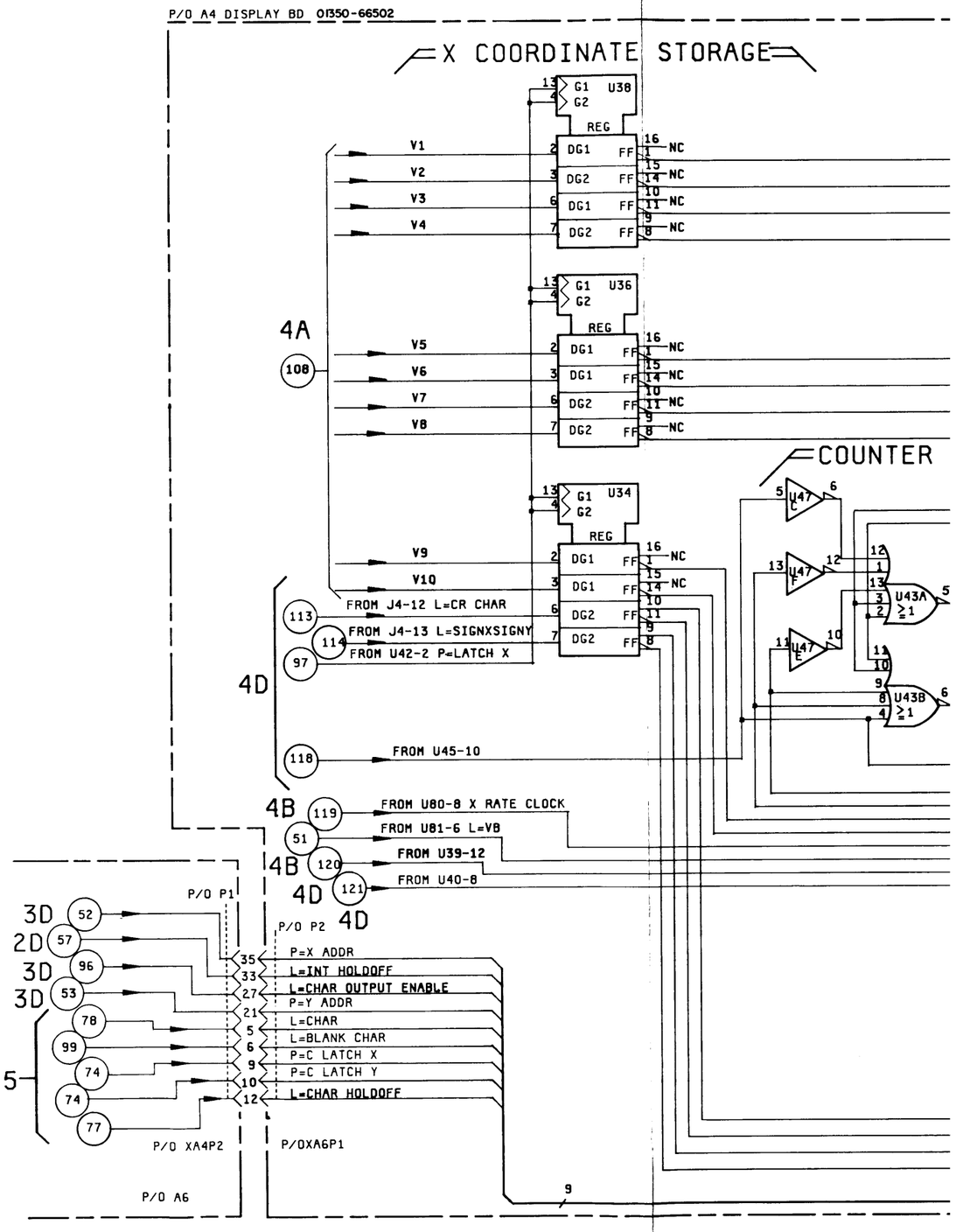
The X Position Counter will not be incremented/decremented if the RATE CLOCK is blocked in the Counter Control circuit by one of the following: (1) loss of L=VB from schematic 4B; (2) maximum display length (count of 1023) is reached when in up-count; (3) minimum display length (count of 0) is reached when in down-count.

8-85. CASE 2. CHARACTER GENERATION.

When in text mode the X Position Counter is controlled by the Character Generator Board. Two inputs (U41 pin 3 and U41 pin 4, from the Character Generator Board via schematic 4D) control the up/down count input to the X Position Counter. The input to U41 pin 3 also changes the X Position-Coordinate Difference circuit from an "Output=A-B" operation to "Output=A".

In the text mode the data latched into the X Coordinate Storage is from the Character Generator (Display Memory contains a "text flag"). The data on bus lines V1 through V10 is latched in the X Coordinate Storage by the signal H=LATCH X when character data is available on the bus lines.

The Exclusive OR output data is sent to schematic 4B without a subtract or complement taking place. RATE CLOCKs will be returned from schematic 4B to increment or decrement the X Position Counter as required for each character. The output of the X Position Counter is converted to an analog signal by the Digital to Analog Converter (schematic 4E).


P/O A4 DISPLAY BD 01350-66502
X COORDINATE STORAGE
G1 U38
G2
REG
V1
V2
V3
V4
DG1 FF
DG2 FF
NC
G1 U36
V5
V6
V7
V8
4A
108
G1 U34
V9
V10
COUNTER
U47 C
U47 F
U47 E
U43A ≥1
U43B ≥1
FROM J4-12 L=CR CHAR
FROM J4-13 L=SIGNXSIGNY
FROM U42-2 P=LATCH X
113
114
97
4D
118
FROM U45-10
4B
119
FROM U80-8 X RATE CLOCK
51
FROM U81-6 L=VB
120
FROM U39-12
121
FROM U40-8
P/O P1
P/O P2
3D
2D
52
57
96
53
78
99
74
77
5
P=X ADDR
L=INT HOLDOFF
L=CHAR OUTPUT ENABLE
P=Y ADDR
L=CHAR
L=BLANK CHAR
P=C LATCH X
P=C LATCH Y
L=CHAR HOLDOFF
35
33
27
21
5
6
9
10
12
P/O XA4P2
P/OXA6P1
P/O A6
9

P/O A4 DISPLAY BD 01350-66502

X COORDINATE STORAGE

U38 G1 G2 REG — DG1 FF, DG2 FF — V1, V2, V3, V4 — NC

U36 G1 G2 REG — DG1 FF, DG2 FF — V5, V6, V7, V8 — NC

U34 G1 G2 REG — DG1 FF, DG2 FF — V9, V10 — NC

FROM J4-12 L=CR CHAR (113)
FROM J4-13 L=SIGNXSIGNY (114)
FROM U42-2 P=LATCH X (97)
FROM U45-10 (118)
FROM U80-8 X RATE CLOCK (4B 119)
FROM U81-6 L=VB (51)
FROM U39-12 (4B 120)
FROM U40-8 (4B 4D 121)

4A (108)

COUNTER CLOCK CONTROL

U47 C, U47 F, U47 E
U43A ≥1, U43B ≥1
U77A ≥1, U77D ≥1
U80A &

X POSITION COUNTER

U52, U53, U54: X→Y, 15+4 0+3, 1,2,4+1 1,2,3-1, & C, & G1, G2, G3, G4, CNTR, CD

R163 10K +5V

H=XDATA1 H=XDATA2 H=XDATA3 H=XDATA4 H=XDATA5 H=XDATA6 H=XDATA7 H=XDATA8 H=XDATA9 H=XDATA10

X DATA 1-10 (109 4E)

POSITION-COORDINATE DIFFERENCE

U33, U32, U31: X→Y, G31 G00, +5V

ALU: F(A,B,C), A, B, C, 0000, F(A,B)=15, F(A,B)>15

U37B 6 TO U68-5
U37A 3 TO U68-3
U37C 8 TO U63-21
U37D 11 TO U63-19
U35B 6 TO U63-17
U35A 3 TO U63-15
U35C 8 TO U63-9
U35D 11 TO U63-7
U58A 3 TO U63-5
U58B 6 TO U63-3

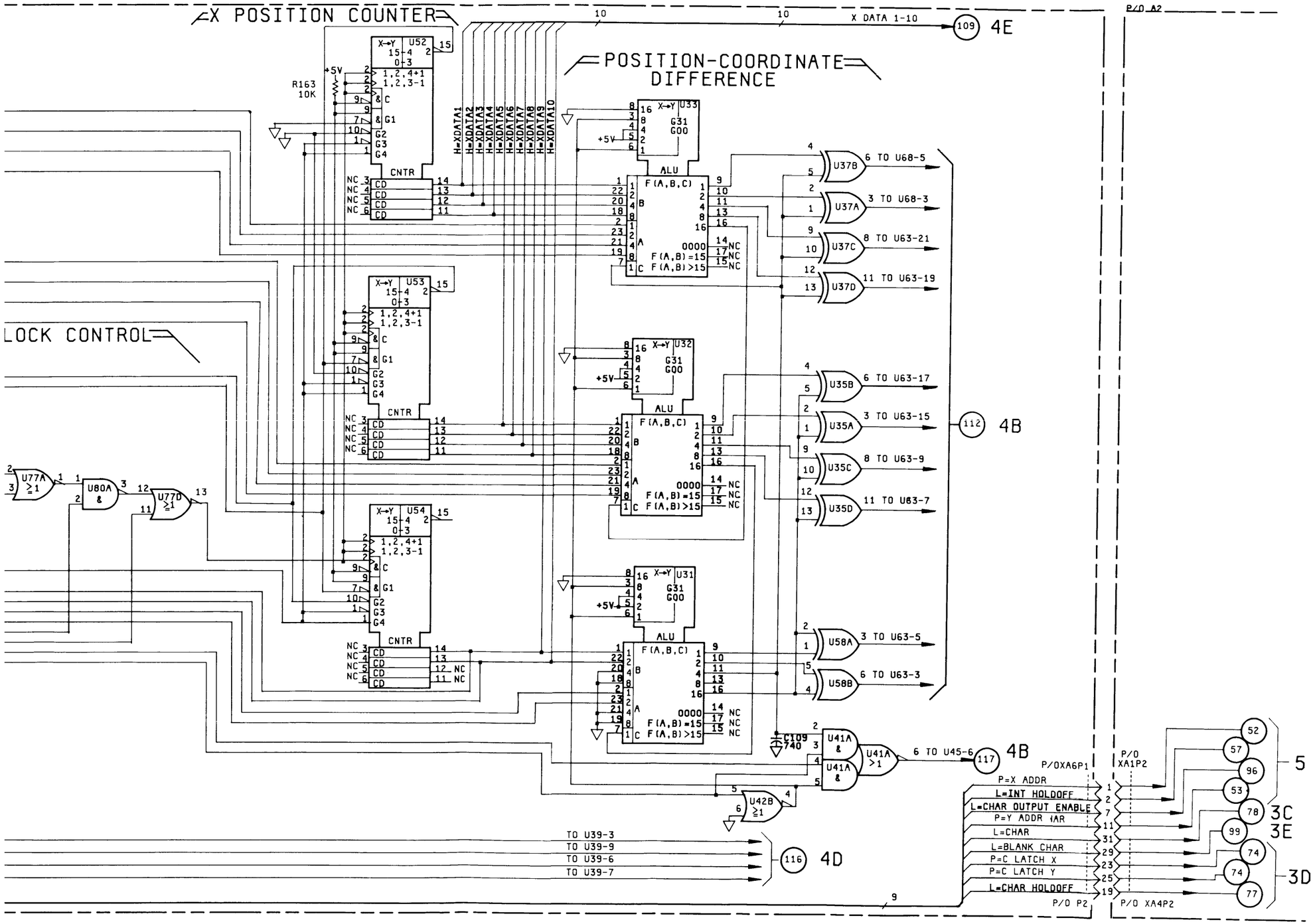
C109 740
U41A &, U41A ≥1 — 6 TO U45-6 (117 4B)
U42B ≥1

TO U39-3
TO U39-9
TO U39-6
TO U39-7
(116 4D)

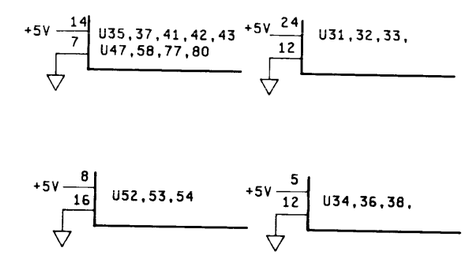
P/O P1
P/O P2
P/O XA4P2
P/OXA6P1
P/O A6

P=X ADDR
L=INT HOLDOFF
L=CHAR OUTPUT ENABLE
P=Y ADDR
L=CHAR
L=BLANK CHAR
P=C LATCH X
P=C LATCH Y
L=CHAR HOLDOFF

(112 4B)
P/OXA
P=X ADDR
L=INT HOLDOF
L=CHAR OUTPUT EN
P=Y ADDR (AR
L=CHAR
L=BLANK CHAR
P=C LATCH X
P=C LATCH Y
L=CHAR HOLDOF
P/O



LOGIC DEVICE POWER CONNECTIONS



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. UNUSED PINS
   ON J1 49,62,69,70,71
   ON J2 2,10 THRU 28 ALL EVEN
   34 THRU 80 ALL EVEN,37,39,41
   45 THUR 67,73 THUR 79 ALL ODD

PARTS ON THIS SCHEMATIC

P/O A4
C109 R163 U31-38,41A,42B,43A,B,47C,E,F52,53, U54,77A,D,80A

1350/108

4C

Figure 8-38. Schematic 4C

8-86. SCHEMATIC 4D PRINCIPLES OF OPERATION.

Schematic 4D contains:

1. Y Coordinate Storage.
2. Y Position Counter.
3. Y Position-Coordinate Difference circuit.
4. Y Position Clock Control.

Operation of the circuits on Schematic 4D will be covered for two cases: (1) Vector Generation; and (2) Character Generation.

8-87. CASE 1. VECTOR GENERATION.

When a Y Coordinate value is available from memory on the V1-V10 data bus a H=LATCH Y pulse will be input from the Control Board and latch that value into U44, U46, and U48, the Y Coordinate Storage register.

After the coordinate is latched a ones complement subtraction takes place in the Y Position-Coordinate Difference circuit (U49, U50, U51). The subtraction is an A minus B operation, that is, the actual pen (beam) position (B) is subtracted from the input coordinate (A). The result of the subtraction is the absolute distance the pen must move in the Y plane. If the pen is to move toward the right of the screen the result of the subtraction will be a positive number and U49 pins 11 and 16 will remain low. If the pen is to move toward the left of the screen the result of the subtraction will be a negative number and U49 pins 11 and 16 will be high.

When U49 pins 11 and 16 are low the Exclusive OR gates (U59, U60, U58C and U58D) have no effect on the data and their outputs are identical to their inputs. The low on U49 pin 11 via U41-8 and U45-9 will place the Y Position Counter in an up-count mode. When U49 pins 11 and 16 are high the Exclusive ORs will complement the data and the Y Position Counter is in the down-count mode.

The output data of the Exclusive ORs (U59, U60, U58C, and U58D) is further processed on schematic 4B which will return a RATE CLOCK (U80-4) to increment or decrement the Y Position Counter. Only the correct number of clocks will be input to the Y Position Counter to move the pen the absolute distance required. The contents of the Y Position Counter is sent (H=YDATA1 through H=YDATA10) to the Y Digital To Analog Converter, schematic 4E.

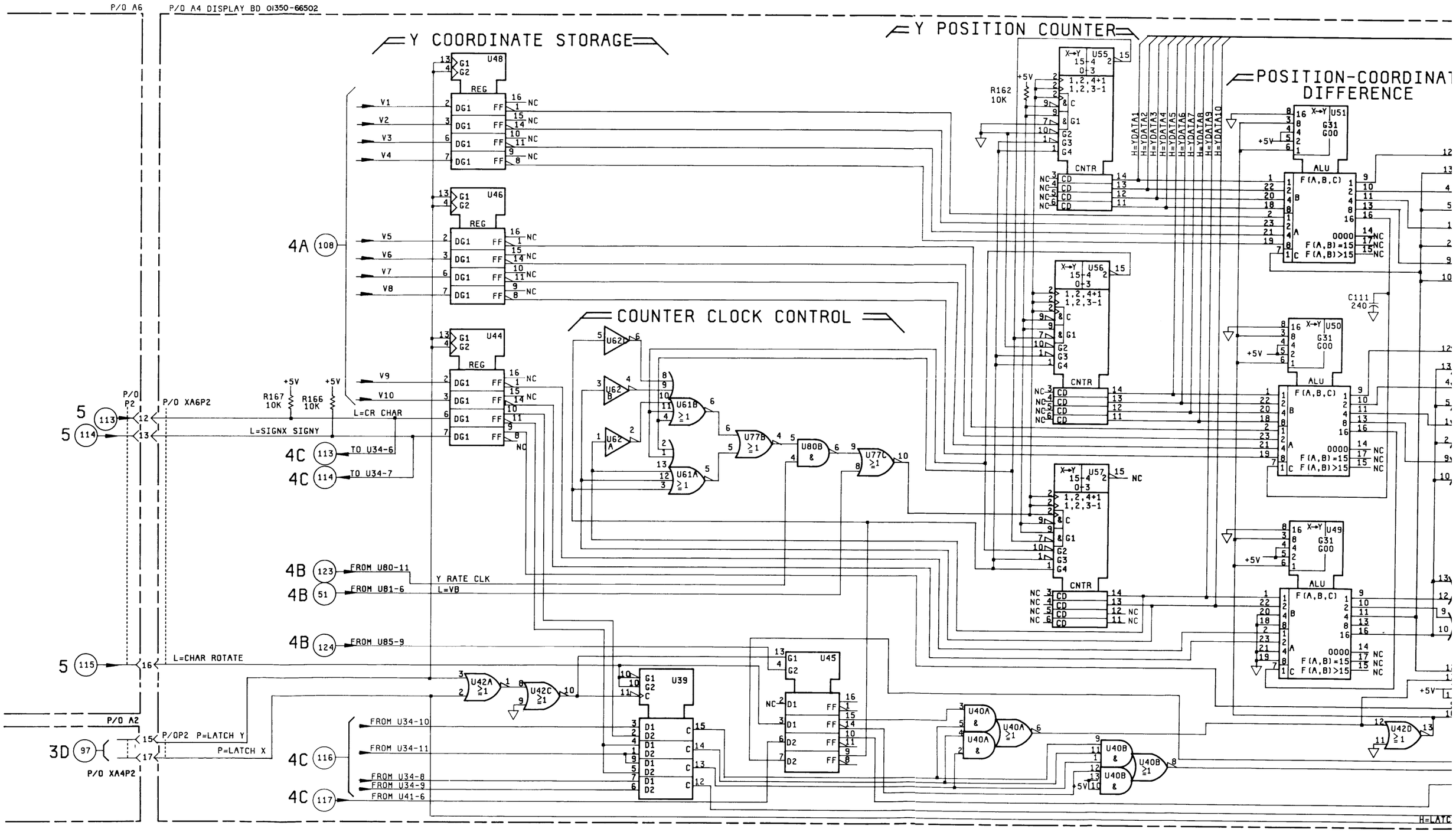
The Y Position Counter will not be incremented/decremented if the RATE CLOCK is blocked in the Counter Control circuit by one of the following: (1) loss of L=VB from schematic 4B; (2) maximum display length (count of 1023) is reached when in up-count; (3) minimum display length (count of 0) is reached when in down-count.

8-88. CASE 2. CHARACTER GENERATION.

When in text mode the Y Position Counter is controlled by the Character Generator Board. Two inputs U41 pin 9 and U41 pin 13 from the Character Generator Board control the up/down count input to the Y Position Counter. The input to U41 pin 10 also changes the Y Position-Coordinate Difference circuit from an "Output=A-B" operation to "Output=A".

In the text mode the data latched into the Y Coordinate Storage is from the Character Generator. The data on bus lines V1 through V10 is latched in the Y Coordinate Storage by the signal LATCH Y when character data is available on the bus lines.

The Exclusive OR output data is sent to schematic 4B without a subtract or complement taking place. RATE CLOCKs will be returned from schematic 4B to increment or decrement the Y Position Counter as required for each character. The output of the Y Position Counter is converted to an analog signal by the Digital to Analog Converter (schematic 4E).



P/O A6
P/O A4 DISPLAY BD 01350-66502
Y COORDINATE STORAGE
Y POSITION COUNTER
POSITION-COORDINAT
DIFFERENCE
COUNTER CLOCK CONTROL
U48
U46
U44
U55
U56
U57
U51
U50
U49
U39
U45
U62
U61B
U61A
U77B
U77C
U80B
U42A
U42C
U40A
U40B
U42D
REG
CNTR
ALU
F(A,B,C)
F(A,B)=15
F(A,B)>15
V1
V2
V3
V4
V5
V6
V7
V8
V9
V10
R162 10K
R167 10K
R166 10K
C111 240
4A 108
4B 123
4B 51
4B 124
4C 113
4C 114
4C 116
4C 117
5 113
5 114
5 115
3D 97
P/O P2
P/O XA6P2
P/O A2
P/O XA4P2
P/OP2 P=LATCH Y
P=LATCH X
L=CR CHAR
L=SIGNX SIGNY
TO U34-6
TO U34-7
FROM U80-11
FROM U81-6
FROM U85-9
Y RATE CLK
L=VB
L=CHAR ROTATE
FROM U34-10
FROM U34-11
FROM U34-8
FROM U34-9
FROM U41-6
H=YDATA1
H=YDATA2
H=YDATA3
H=YDATA4
H=YDATA5
H=YDATA6
H=YDATA7
H=YDATA8
H=YDATA9
H=YDATA10
H=LATC

NATE STORAGE

Y POSITION COUNTER

YDATA1-YDATA10 (110) 4E

POSITION-COORDINATE DIFFERENCE

COUNTER CLOCK CONTROL

(122) 4B

(4C)

TO U41-3 (121)
TO U47-5 (118)
TO U41-4 (120)
H=LATCH X TO U38-13 (97)

LOGIC DEVICE POWER CONNECTIONS

+5V — 14 — 7 — U40,41,42,58 U59,60,61,62 U77,80

+5V — 16 — 8 — U39,55,56,57

+5V — 5 — 12 — U44,45,46,48

+5V — 24 — 12 — U49,50,51

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

P/O A4

C111
R162,164,166,167
U39,40A,B,41B,42A,C,D,44-46,48-51
U55-57,58C,D,59A,B,C,D,U60A,B,C,D,
U61A,B,62A,B,C,77B,C,80B

1350/114

4D

Figure 8-39. Schematic 4D

8-89. SCHEMATIC 4E PRINCIPLES OF OPERATION.

Schematic 4E contains:

1. X Digital to Analog Converter (X DAC).
2. Y Digital to Analog Converter (Y DAC).

8-90. OPERATION.

Operation of the circuits on Schematic 4E will be covered using the first two input stages of the XDAC as operational examples. The XDAC and YDAC actually contain 10 input stages each, however, all 20 are identical in operation, therefore, a discussion of two is sufficient.

Each input stage contains a current source, a switching transistor, and a portion of a resistive ladder network. In the example, Q1 and Q3 are the current source transistors, Q2 and Q4 are the switching transistors, and R7, R8, R11, R12 are part of the resistive ladder network.

With all DAC inputs low from the position counter, Q1 and Q3 will be conducting. The current path for Q1 is from a low XDATA1 input through CR1 and Q1 to +15V. With low inputs, Q2 and Q4 are not conducting.

When the input XDATA1 goes high, Q2 is biased to turn on. A current is now flowing in the resistive ladder network causing a change at the input of the active filter (U89). When the position counter is incremented one count, XDATA1 will go low and XDATA2 will be high causing Q4 to conduct and Q2 to cutoff. The current source Q3 supplies the same amount of current to the resistive ladder network as Q1 did, however, because it is one stage closer to the active filter (U89) it has an effect on the input of U89 which is twice the change Q1 made.

When the position counter is again incremented XDATA1 and XDATA2 will both be high. The switching transistors, Q2 and Q4, will both be conducting, causing a change at the input of the active filter (U89) which is three times the effect of Q1 only.

Each input stage to the right on schematic 4E has twice the effect on the active filter (U89) of the previous stage. This is because the resistor network is a binary ladder.

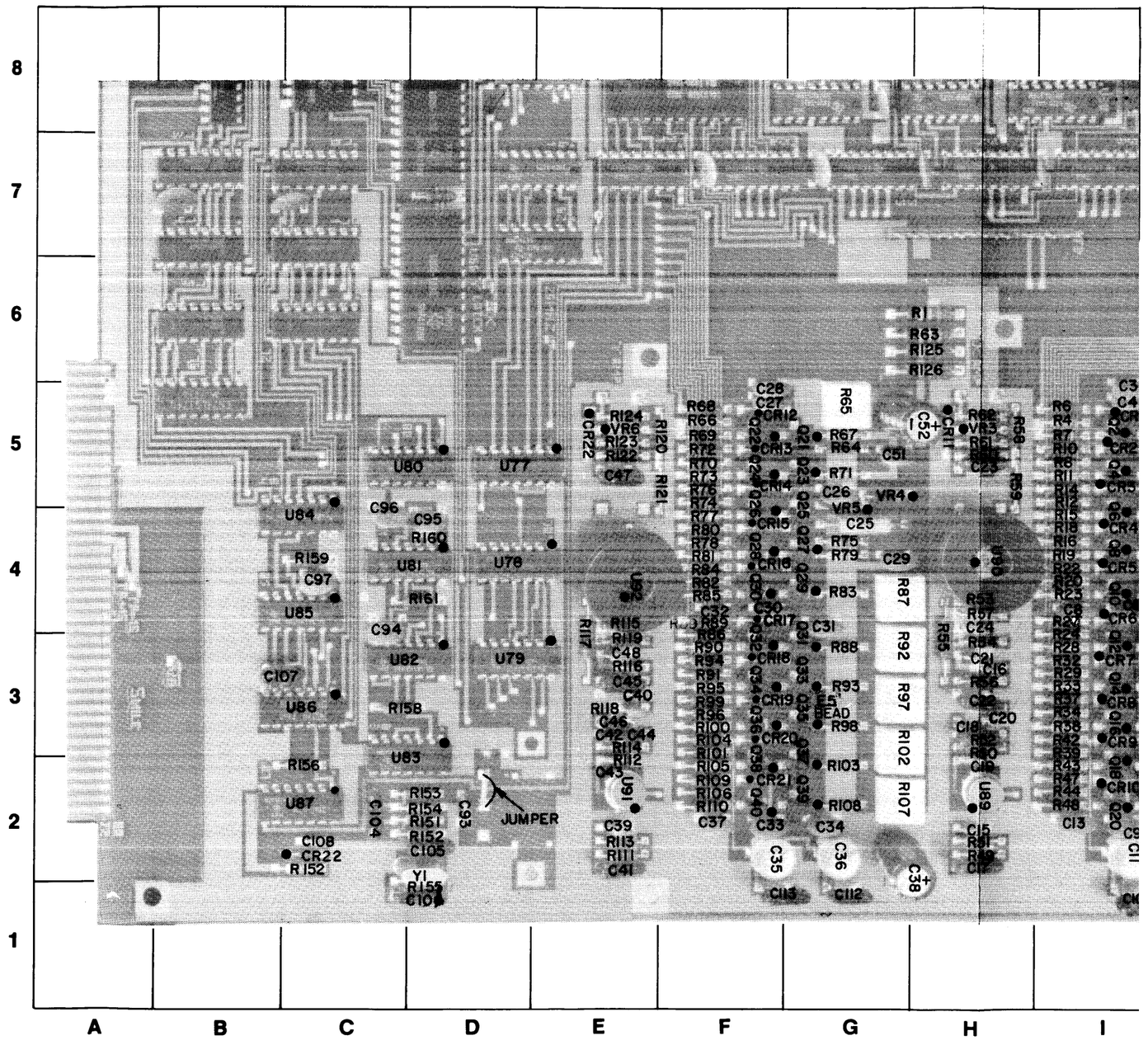
The X and Y position data bits are connected to the current sources such that bit 10 causes 1/2 screen deflection, bit 9 causes 1/4 screen deflection, etc.

The operational amplifiers U89 and U91 are operating as active filter devices. The operational amplifiers U90 and U92 are operated as output driver stages.

The X and Y outputs are a positive 0 volt to 1 volt ramp potential for the display inputs.

8-91. ADJUSTMENTS.

A4R25, A4R30, A4R35, A4R40, and A4R45 are used to minimize gaps or overlapping of the X DAC. A4R87, A4R92, A4R97, A4R102, and A4R107 are used to minimize gaps or overlapping of the Y DAC. A4C11, A4C12, A4R3, A4C35, A4C36, and A4R65 are used to adjust the vectors for minimum distortion. See Section V of this manual for adjustment procedures.



cutoff. The current
ınt of current to the
ıowever, because it is
(U89) it has an effect
the change Q1 made.

again incremented
high. The switching
conducting, causing
filter (U89) which is

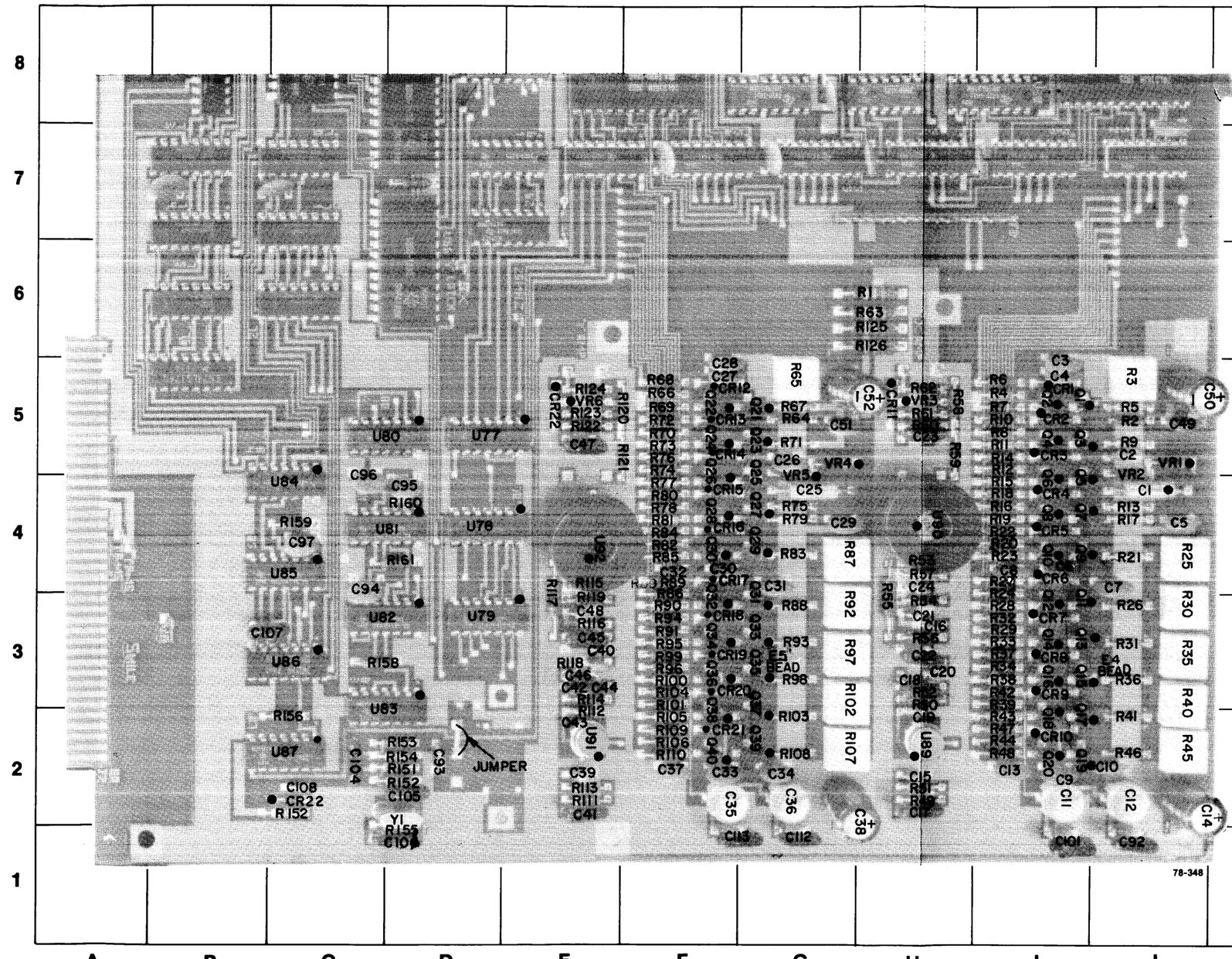
ıematic 4E has twice
of the previous stage.
k is a binary ladder.

ıre connected to the
causes 1/2 screen
deflection, etc.

ıd U91 are operating
ional amplifiers U90
iver stages.

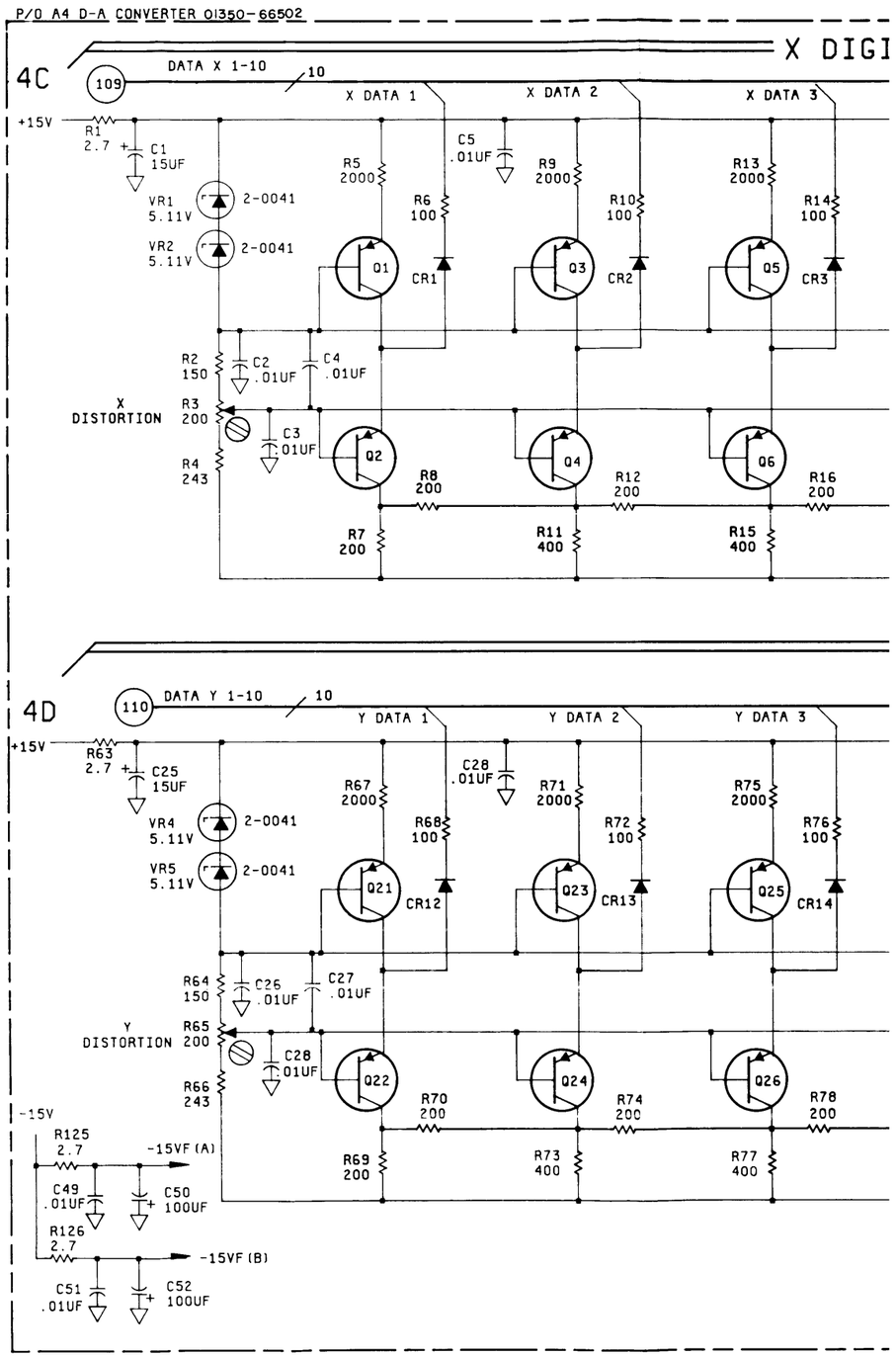
0 volt to 1 volt ramp

d A4R45 are used to
the X DAC. A4R87,
4R107 are used to
the Y DAC. A4C11,
l A4R65 are used to
ortion. See Section V
cedures.



REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	J-4	C101	I-1	Q26	F-4	R44	I-2	R102	G-3
C2	J-5	C104	C-2	Q27	G-4	R45	J-2	R103	G-2
C3	I-5	C105	D-2	Q28	F-4	R46	J-2	R104	F-3
C4	I-5	C106	D-1	Q29	G-4	R47	I-2	R105	F-3
C5	J-4	C107	C-3	Q30	F-4	R48	I-2	R106	F-2
C6	I-4	C108	C-2	Q31	G-4	R49	H-2	R107	G-2
C7	J-4	C112	G-1	Q32	F-4	R50	H-2	R108	G-2
C8	I-4	C113	F-1	Q33	G-3	R51	H-2	R109	F-2
C9	I-2	CR1	I-5	Q34	F-3	R52	H-3	R110	F-2
C10	J-2	CR2	I-5	Q35	G-3	R53	H-4	R111	E-2
C11	I-2	CR3	I-5	Q36	F-3	R54	H-3	R112	E-2
C12	J-2	CR4	I-4	Q37	G-3	R55	H-3	R113	E-2
C13	I-2	CR5	I-4	Q38	F-2	R56	H-3	R114	E-3
C14	J-2	CR6	I-4	Q39	G-2	R57	H-4	R115	E-4
C15	H-2	CR7	I-3	Q40	F-2	R58	H-5	R116	E-3
C16	H-3	CR8	I-3	R1	G-6	R59	H-5	R117	E-4
C17	H-2	CR9	I-3	R2	J-5	R60	H-5	R118	E-3
C18	H-3	CR10	I-2	R3	J-5	R61	H-5	R119	E-3
C19	H-2	CR11	H-5	R4	I-5	R62	H-5	R120	E-5
C20	H-3	CR12	F-5	R5	J-5	R63	G-6	R121	E-5
C21	H-3	CR13	F-5	R6	I-5	R64	G-5	R122	E-5
C22	H-3	CR14	F-5	R7	I-5	R65	G-5	R123	E-5
C23	H-5	CR15	F-4	R8	I-5	R66	F-5	R124	E-5
C24	H-3	CR16	F-4	R9	J-5	R67	G-5	R125	G-6
C25	G-4	CR17	F-4	R10	I-5	R68	F-5	R126	G-6
C26	G-5	CR18	F-3	R11	I-5	R69	F-5	R151	D-2
C27	F-6	CR19	F-3	R12	I-5	R70	F-5	R152	D-2
C28	F-6	CR20	F-3	R13	J-4	R71	G-5	R153	D-2
C29	G-4	CR21	F-2	R14	I-5	R72	F-5	R154	D-2
C30	F-4	CR22	E-4	R15	I-4	R73	F-5	R155	D-1
C31	G-4	CR27	C-2	R16	I-4	R74	F-5	R156	C-2
C32	F-4	E1	J-3	R17	J-4	R75	G-4	R157	C-2
C33	F-2	E2	G-3	R18	I-4	R76	F-5	R158	C-3
C34	G-2	Q1	I-5	R19	I-4	R77	F-4	R159	C-4
C35	F-2	Q2	I-5	R20	I-4	R78	F-4	R160	D-4
C36	G-2	Q3	I-5	R21	J-4	R79	G-4	R161	D-4
C37	F-2	Q4	I-5	R22	I-4	R80	F-4	U77	D-5
C38	H-2	Q5	I-4	R23	I-4	R81	F-4	U78	D-4
C39	E-2	Q6	I-4	R24	I-3	R82	F-4	U79	D-3
C40	E-3	Q7	I-4	R25	J-4	R83	G-4	U80	D-5
C41	E-2	Q8	I-4	R26	J-3	R84	F-4	U81	D-4
C42	E-3	Q9	I-4	R27	I-4	R85	F-4	U82	C-2
C43	E-2	Q10	I-4	R28	I-3	R86	F-5	U83	C-2
C44	E-3	Q11	I-3	R29	I-3	R87	G-4	U84	C-4
C45	E-3	Q12	I-3	R30	J-3	R88	G-3	U85	C-4
C46	E-3	Q13	I-3	R31	J-3	R89	F-4	U86	C-3
C47	E-5	Q14	I-3	R32	I-3	R90	F-4	U87	C-2
C48	E-3	Q15	I-3	R33	I-3	R91	F-3	U89	H-2
C49	J-5	Q16	I-3	R34	I-3	R92	G-3	U90	H-4
C50	J-5	Q17	I-2	R35	J-3	R93	G-3	U91	E-2
C51	G-5	Q18	I-2	R36	J-3	R94	F-3	U92	E-4
C52	H-5	Q19	I-2	R37	I-3	R95	F-3	VR1	J-5
C92	J-1	Q20	I-2	R38	I-3	R96	F-3	VR2	J-4
C93	D-2	Q21	G-5	R39	I-2	R97	G-3	VR3	H-5
C94	C-4	Q22	F-5	R40	J-3	R98	G-3	VR4	G-5
C95	D-4	Q23	G-5	R41	J-2	R99	F-3	VR5	G-5
C96	C-4	Q24	F-5	R42	I-3	R100	F-3	VR6	E-5
C97	C-4	Q25	G-4	R43	I-2	R101	F-3	Y1	D-2

Figure 8-40. Component Locator for Schematic 4E and Part of Schematic 4C


P/O A4 D-A CONVERTER 01350-66502
4C
DATA X 1-10
10
109
X DATA 1
X DATA 2
X DATA 3
+15V
R1
2.7
C1
15UF
VR1
5.11V
2-0041
VR2
5.11V
2-0041
R5
2000
C5
.01UF
R9
2000
R13
2000
R6
100
R10
100
R14
100
Q1
Q3
Q5
CR1
CR2
CR3
R2
150
C2
.01UF
C4
.01UF
X
DISTORTION
R3
200
C3
01UF
R4
243
Q2
Q4
Q6
R8
200
R12
200
R16
200
R7
200
R11
400
R15
400
4D
110
DATA Y 1-10
10
Y DATA 1
Y DATA 2
Y DATA 3
+15V
R63
2.7
C25
15UF
VR4
5.11V
2-0041
VR5
5.11V
2-0041
R67
2000
C28
.01UF
R71
2000
R75
2000
R68
100
R72
100
R76
100
Q21
Q23
Q25
CR12
CR13
CR14
R64
150
C26
.01UF
C27
.01UF
Y
DISTORTION
R65
200
C28
01UF
R66
243
Q22
Q24
Q26
R70
200
R74
200
R78
200
R69
200
R73
400
R77
400
-15V
R125
2.7
-15VF (A)
C49
.01UF
C50
100UF
R126
2.7
-15VF (B)
C51
.01UF
C52
100UF

4 D-A CONVERTER 01350-66502

X DIGITAL TO ANALOG CONVERTER

DATA X 1-10 (109) — 10

X DATA 1 | X DATA 2 | X DATA 3 | X DATA 4 | X DATA 5 | X DATA 6 | X DATA 7 | X DATA 8 | X DATA 9 | X DATA 10

R1 2.7 — C1 15UF

VR1 5.11V 2-0041

VR2 5.11V 2-0041

R5 2000 | R9 2000 | R13 2000 | R17 2000 | R21 2000

R6 100 | R10 100 | R14 100 | R18 100 | R22 100

C5 .01UF

1/32 SCREEN R25 100 — R26 1960 — R27 100

1/16 SCREEN R30 100 — R31 1960 — R32 100

1/8 SCREEN R35 100 — R36 1960 — R37 100

1/4 SCREEN R40 100 — R41 1960 — R42 100

1/2 SCREEN R45 100 — R46 1960 — R47 100

X DISTORTION

C11 9-35 — C101 15 — C12 9-35 — C92 15 — C14 100 UF

CR1 | CR2 | CR3 | CR4 | CR5 | CR6 | CR7 | CR8 | CR9 | CR10

E1 BEAD

Q1 | Q3 | Q5 | Q7 | Q9 | Q11 | Q13 | Q15 | Q17 | Q19

R2 150 — C2 .01UF — C4 .01UF

X DISTORTION — R3 200 — C3 01UF — R4 243

C6 .01UF — C7 .01UF — C8 .01UF

C9 .01UF — C10 .01UF — C13 .01UF

Q2 | Q4 | Q6 | Q8 | Q10 | Q12 | Q14 | Q16 | Q18 | Q20

R8 200 | R12 200 | R16 200 | R20 200 | R24 200 | R29 200 | R34 200 | R39 200 | R44 200

R7 200 | R11 400 | R15 400 | R19 400 | R23 400 | R28 400 | R33 400 | R38 400 | R43 400 | R48 200

R49 825 — R50 3920 — C18 22 — C19 0.1 UF — R51 1000 — R53 1210

C17 110 — R52 1820 — C20 0.1UF — R59 13K

U89

-15V (A) VR3 2-0025 10V — R58 511 — -15VF

FILTE 1826-(

Y DIGITAL TO ANALOG CONVERTER

DATA Y 1-10 (110) — 10

Y DATA 1 | Y DATA 2 | Y DATA 3 | Y DATA 4 | Y DATA 5 | Y DATA 6 | Y DATA 7 | Y DATA 8 | Y DATA 9 | Y DATA 10

R63 2.7 — C25 15UF

VR4 5.11V 2-0041

VR5 5.11V 2-0041

R67 2000 | R71 2000 | R75 2000 | R79 2000 | R83 2000

R68 100 | R72 100 | R76 100 | R80 100 | R84 100

C28 .01UF

1/32 SCREEN R87 100 — R88 1960 — R89 100

1/16 SCREEN R92 100 — R93 1960 — R94 100

1/8 SCREEN R97 100 — R98 1960 — R99 100

1/4 SCREEN R102 100 — R103 1960 — R104 100

1/2 SCREEN R107 100 — R108 1960 — R109 100

Y DISTORTION

C35 9-35 — C113 15 — C36 9-35 — C112 15 — C38 100 UF

CR12 | CR13 | CR14 | CR15 | CR16 | CR17 | CR18 | CR19 | CR20 | CR21

E2 BEAD

Q21 | Q23 | Q25 | Q27 | Q29 | Q31 | Q33 | Q35 | Q37 | Q39

R64 150 — C26 .01UF — C27 .01UF

Y DISTORTION — R65 200 — C28 01UF — R66 243

C29 .01UF — C30 .01UF — C31 .01UF

C33 .01UF — C34 .01UF — C37 .01UF

Q22 | Q24 | Q26 | Q28 | Q30 | Q32 | Q34 | Q36 | Q38 | Q40

R70 200 | R74 200 | R78 200 | R82 200 | R86 200 | R91 200 | R96 200 | R101 200 | R106 200

R69 200 | R73 400 | R77 400 | R81 400 | R85 400 | R90 400 | R95 400 | R100 400 | R105 400 | R110 200

R111 825 — R112 3920 — C42 22 — C43 0.1 UF — R113 1000 — R115 1210

C41 110 — R114 1820 — C44 0.1UF — R121 13K

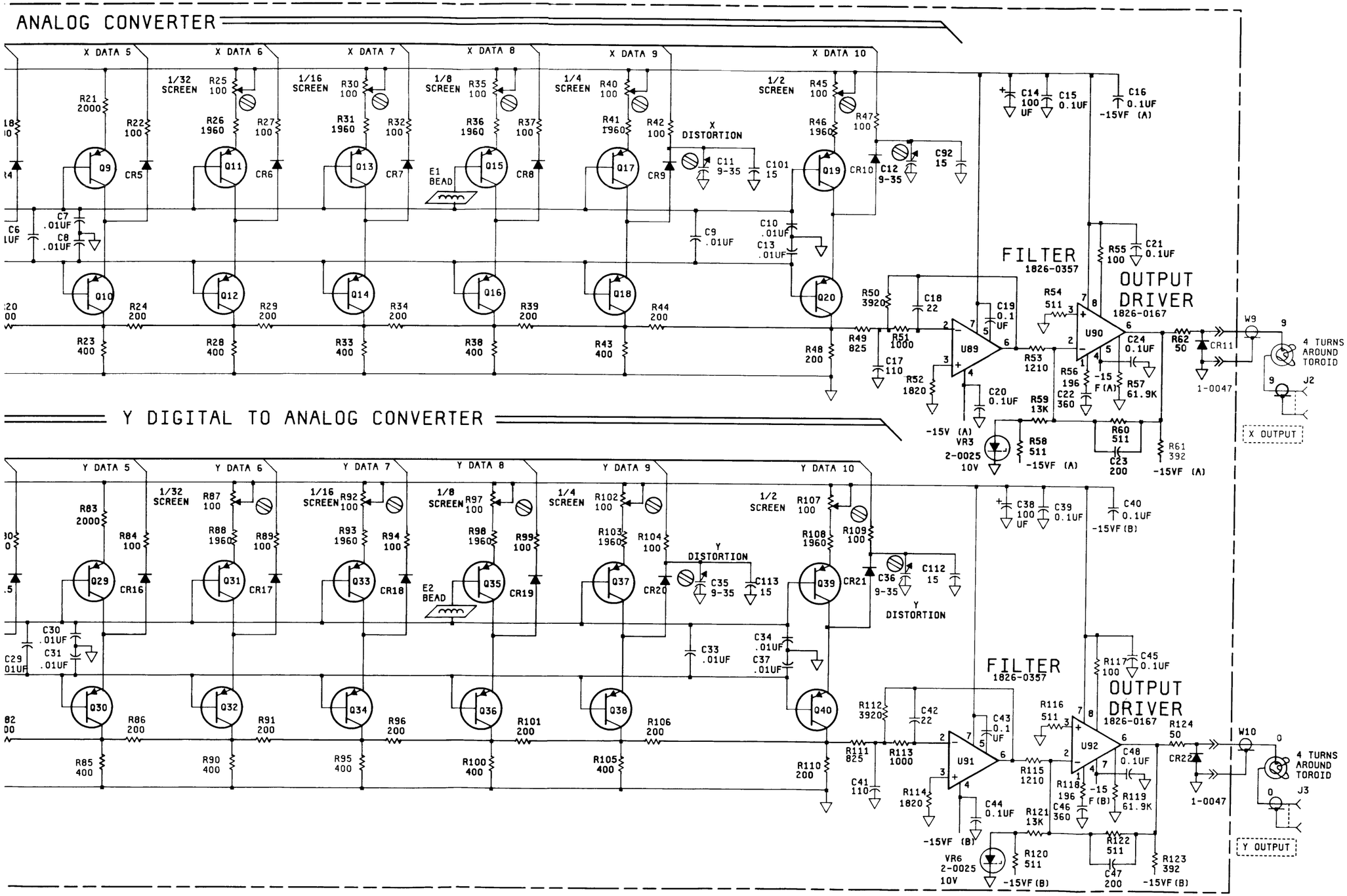
U91

-15VF (B) VR6 2-0025 10V — R120 511 — -15VF (B)

FILTER 1826-0357

-15VF (A) — C50 100UF

-15VF (B) — C52 100UF



NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L
4. Q1-40=1853-0036
   CR1-10=1901-0179
   CR12-21=1901-0179

PARTS ON THIS SCHEMATIC

P/O A4	CHASSIS
C1-52,92,101,112,113 CR1-22 E1,2 Q1-40 R1-126 U89-92 VR1-6	W9,W10

1350-119

4E

Figure 8-41.
Schematic 4E

8-92. CHARACTER GENERATOR A6 (SERVICE SHEET 5).

8-93. SCHEMATIC 5 PRINCIPLES OF OPERATION.

Schematic 5 contains the entire Character Generator. The circuits on the upper half of the schematic provide control and timing. The circuits on the lower half process an ASCII code on lines V1-V10 into a series of vector data. This data is sent back out the V1-V10 lines to the Vector Generator (on the Display Board), where it is added to the current beam location in order to produce a character.

The lower half of the schematic will be discussed first. Whenever an ASCII character is output from the current memory location, the X coordinate will be all zeroes on V1-V10. The all zero state is detected by U5 and U6B (Character Request Detector). This plus the X address clock resets U7A, starting the character generation mode. The next data present on V1-V10 is a 7-bit ASCII character code plus 2 bits for character size and one bit for character rotation. When a Y address clock is received, ASCII Latches U15 and U16 latch the character information and apply it to the Character ROM Address Decoders. These decoders are themselves ROMs which generate a unique 8-bit number that is applied to the Address Counters for parallel loading.

The Address Counters are stepped one count each time VECTOR BUSY goes high, meaning that the last vector has been processed by the Vector Generators. The ten outputs of the counters are applied to the Character ROMs as addresses. The Character ROMs are programmed to provide vector numbers characteristic of the strokes needed to produce the ASCII character.

The four data selectors U12-U14, and U26 (at the right side of the schematic) change the significance of the Character ROM outputs on V1-V10. The incoming size information on V8 and V9 control the data selectors by shifting the top four lines of the Character ROMs from V1-V4 through V4-V7. This in effect shifts the significance or weighting of the character stroke data to the Vector Generator, resulting in larger-sized characters.

U10A, U10D, and U22 select the ROM containing the desired character. ROM 1 (U24) contains the first 64 characters from the modified 1350A ASCII set. ROM 2 (U11) contains the rest of the characters. Refer to the Operating and Programming manual for the modified ASCII character set used in the 1350A.

The circuits along the upper part of the schematic provide control and timing for character generation. U1B is set when a Y address clock occurs.

U2A provides a 200 to 300 nanosecond pulse to the Address Counters for parallel loading of the unique number generated by the Character ROM Address Decoders.

U7A FF is clocked to its reset state whenever an X address clock is received and the current data on V1-V10 is all zeroes. All zeroes in the X coordinate means the Y coordinate following will contain an ASCII code for a character. U7B is clocked to its reset state following U7A's recognition of a character request and a Y address clock, meaning the data on V1-V10 is now a valid ASCII code.

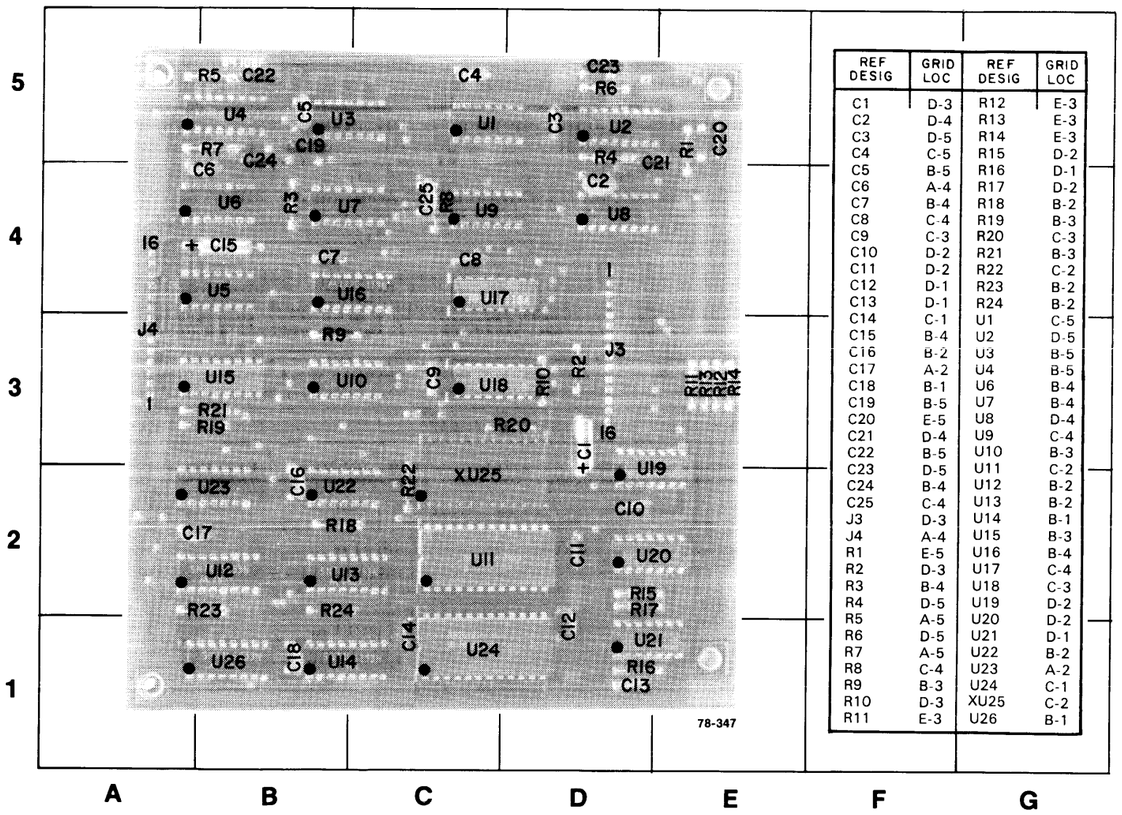
U4A and U4B generate timing pulses to the Vector Generator through multiplexer U9. Unless a character rotation is received to reverse the order, U4A will enable the data coming from the Character ROMs to go to the X Vector Generator. U4B generates a similar pulse following the trailing edge of the U4A pulse to enable the Y Vector Generator. With these two bytes of data the Vector Generator computes the length and direction of the character stroke.

U2B generates a short delay after VECTOR BUSY goes high before the Address Counters are advanced one count.

After the last stroke of a character, while the beam is going to the starting position of the next character, the Character ROM outputs an End of Character signal. U1A FF sets after U4B times out, enabling U10C. When U2B times out ~90 nanoseconds after VECTOR BUSY returns high, U10C sets U7A and U7B. The Character Generator circuit is now ready to receive another character upon a character request detection.

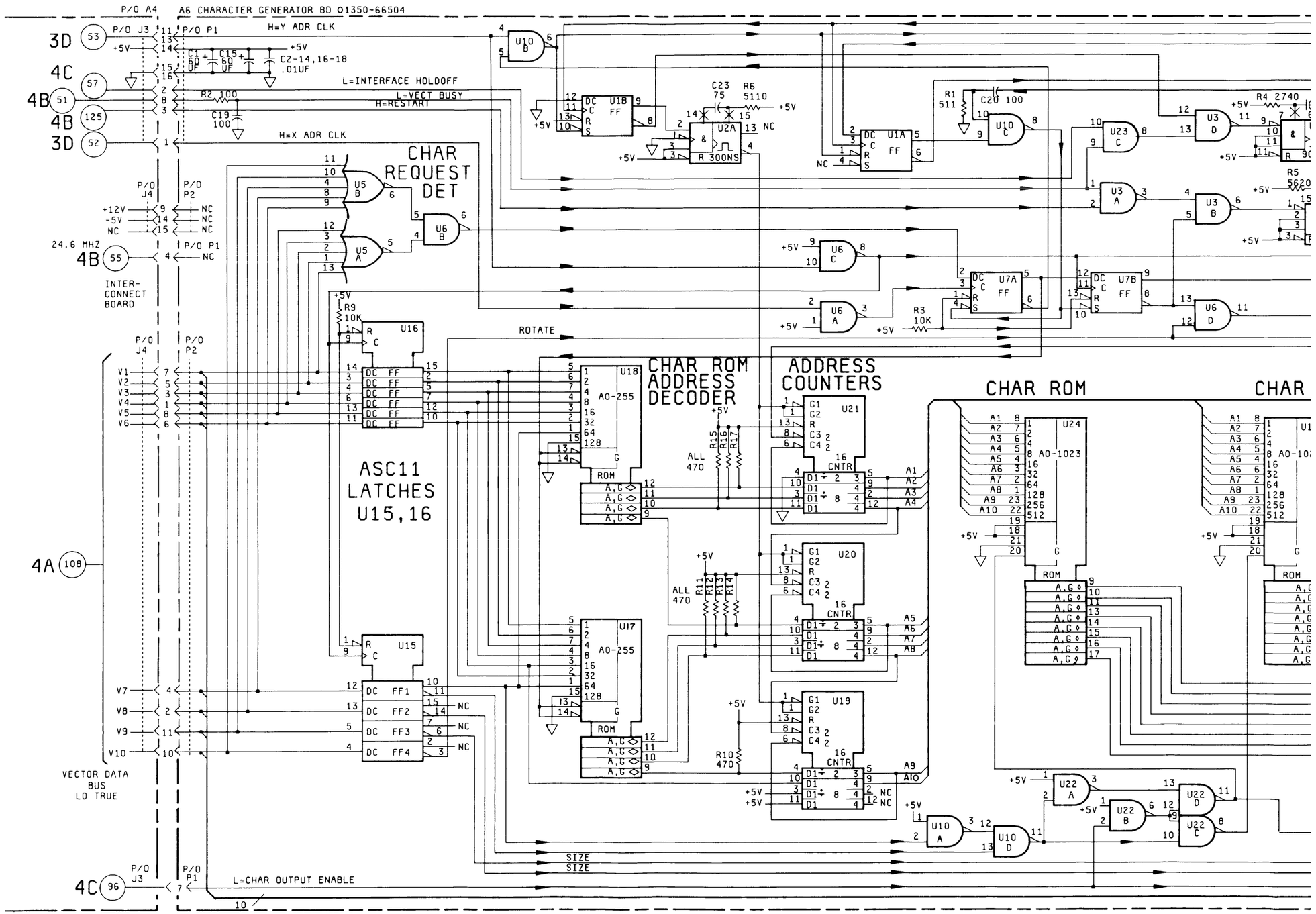
NOTE

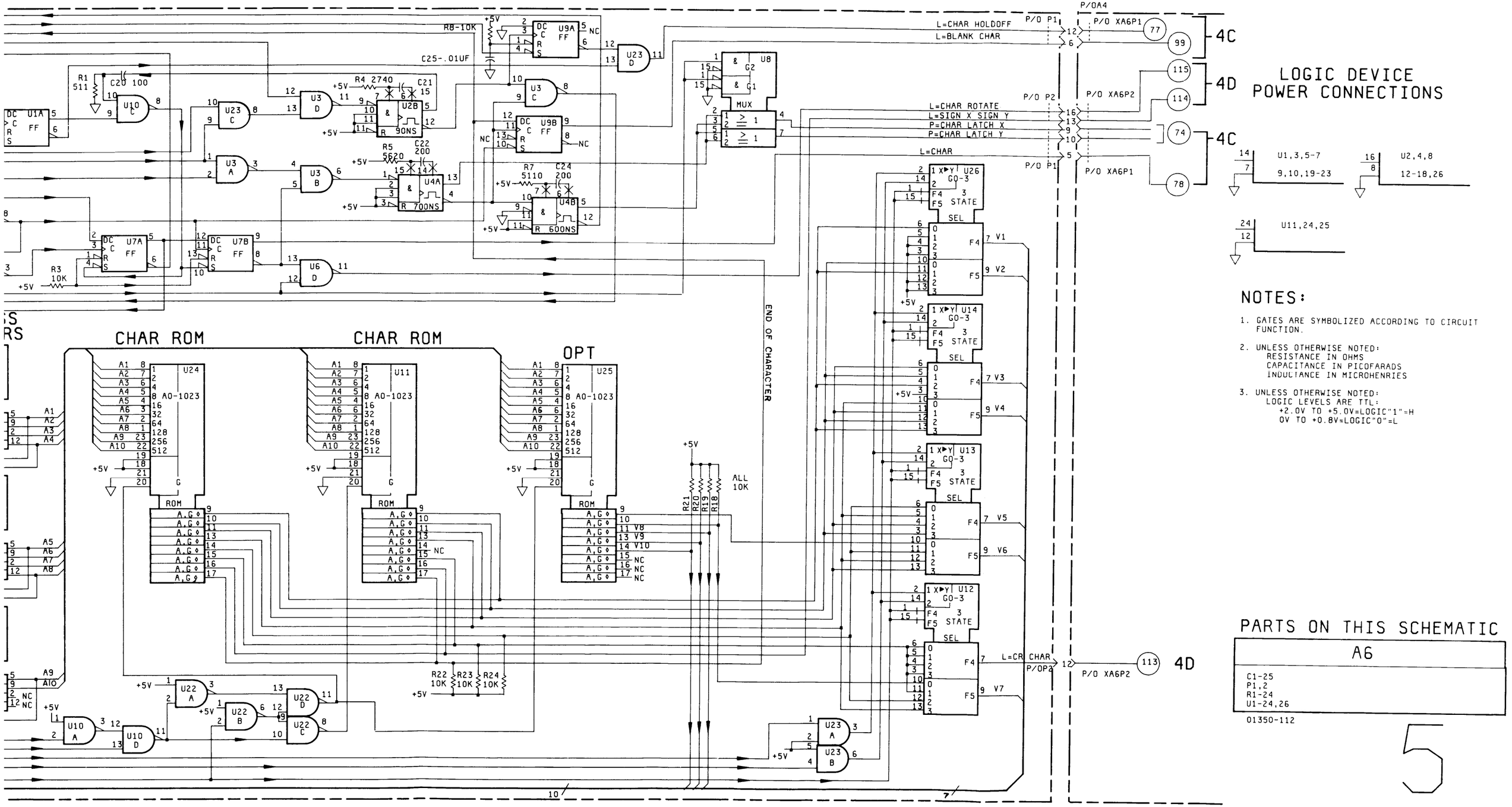
The Character Generator Board (A6) can be completely removed and the 1350A will still be able to produce vectors. This allows isolation when troubleshooting, as the Character Generator can "hang-up" the 1350A, preventing any output.



REF DESIG	GRID LOC	REF DESIG	GRID LOC
C1	D-3	R12	E-3
C2	D-4	R13	E-3
C3	D-5	R14	E-3
C4	C-5	R15	D-2
C5	B-5	R16	D-1
C6	A-4	R17	D-2
C7	B-4	R18	B-2
C8	C-4	R19	B-3
C9	C-3	R20	C-3
C10	D-2	R21	B-3
C11	D-2	R22	C-2
C12	D-1	R23	B-2
C13	D-1	R24	B-2
C14	C-1	U1	C-5
C15	B-4	U2	D-5
C16	B-2	U3	B-5
C17	A-2	U4	B-5
C18	B-1	U6	B-4
C19	B-5	U7	B-4
C20	E-5	U8	D-4
C21	D-4	U9	C-4
C22	B-5	U10	B-3
C23	D-5	U11	C-2
C24	B-4	U12	B-2
C25	C-4	U13	B-2
J3	D-3	U14	B-1
J4	A-4	U15	B-3
R1	E-5	U16	B-4
R2	D-3	U17	C-4
R3	B-4	U18	C-3
R4	D-5	U19	D-2
R5	A-5	U20	D-2
R6	D-5	U21	D-1
R7	A-5	U22	B-2
R8	C-4	U23	A-2
R9	B-3	U24	C-1
R10	D-3	XU25	C-2
R11	E-3	U26	B-1

Figure 8-42. Character Generator Board A6 Component Locator Schematic 5


P/O A4
A6 CHARACTER GENERATOR BD 01350-66504
H=Y ADR CLK
L=INTERFACE HOLDOFF
L=VECT BUSY
H=RESTART
H=X ADR CLK
CHAR REQUEST DET
24.6 MHZ
INTER-CONNECT BOARD
ROTATE
CHAR ROM ADDRESS DECODER
ADDRESS COUNTERS
CHAR ROM
ASC11 LATCHES U15,16
VECTOR DATA BUS LO TRUE
L=CHAR OUTPUT ENABLE
SIZE
SIZE



LOGIC DEVICE POWER CONNECTIONS

14 / 7	U1,3,5-7 9,10,19-23
16 / 8	U2,4,8 12-18,26
24 / 12	U11,24,25

NOTES:

1. GATES ARE SYMBOLIZED ACCORDING TO CIRCUIT FUNCTION.
2. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
3. UNLESS OTHERWISE NOTED:
   LOGIC LEVELS ARE TTL:
   +2.0V TO +5.0V=LOGIC"1"=H
   0V TO +0.8V=LOGIC"0"=L

PARTS ON THIS SCHEMATIC

A6

C1-25
P1,2
R1-24
U1-24,26

01350-112

5

Figure 8-43.
Schematic 5

8-94. POWER SUPPLY A5 (SERVICE SHEET 6).

8-95. SCHEMATIC 6A PRINCIPLES OF OPERATION.

Schematic 6A contains the power input wiring, +15 V, +12 V, -5 V, -15 V regulators, protective overvoltage crowbars, and fan control circuits.

8-96. THREE-TERMINAL REGULATOR SUPPLIES.

The +12 V regulator will be described and is typical of all four regulators.

A DC voltage of ~+20 volts is obtained from the Bridge Rectifier (CR2)/Filter (C8) circuit and applied to U2. U2 is a 3-terminal, fixed-voltage regulator. The output of the regulator IC is a voltage of +12 volts accurate to within 5%. These regulators have internal current limit and thermal protection.

On the output of the regulator is an Overvoltage Crowbar circuit. The crowbar shorts the output of the regulator should the voltage go above approximately 13.5 volts. The Overvoltage Crowbar is a protection circuit only. When the crowbar "fires" the Line fuse should open.

The +15 V and -15 V supplies are protected against reverse voltage conditions by diodes across their outputs.

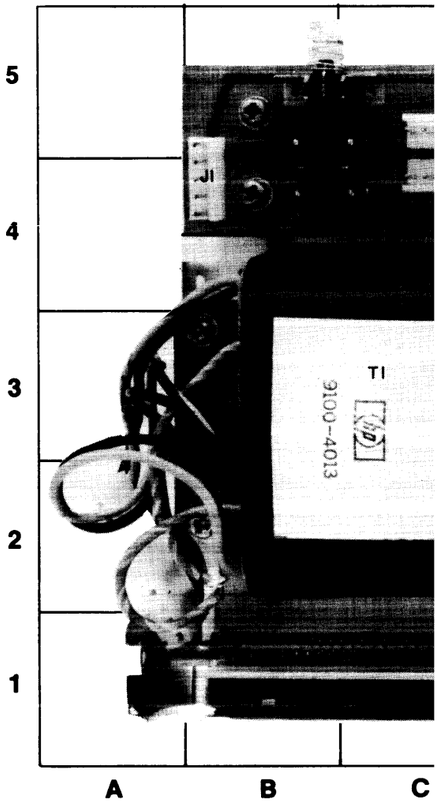
8-97. FAN CIRCUIT.

The fan circuit consists of a filter (located at the rear of the Display Board A4) and an Inverter/Fan assembly. Transistor Q2 limits the maximum current drawn by the fan assembly.

8-98. TROUBLESHOOTING.

Troubleshooting any of the supplies is best done by disconnecting the loads via removing Printed Circuit boards from the 1350A. This will isolate the problem to one of the boards or to the power supply. The Overvoltage Crowbar circuits can be isolated by lifting R30 or R29.

If trouble is experienced with the fan, check the voltage and connections on the red (2) and blue (6) wires.



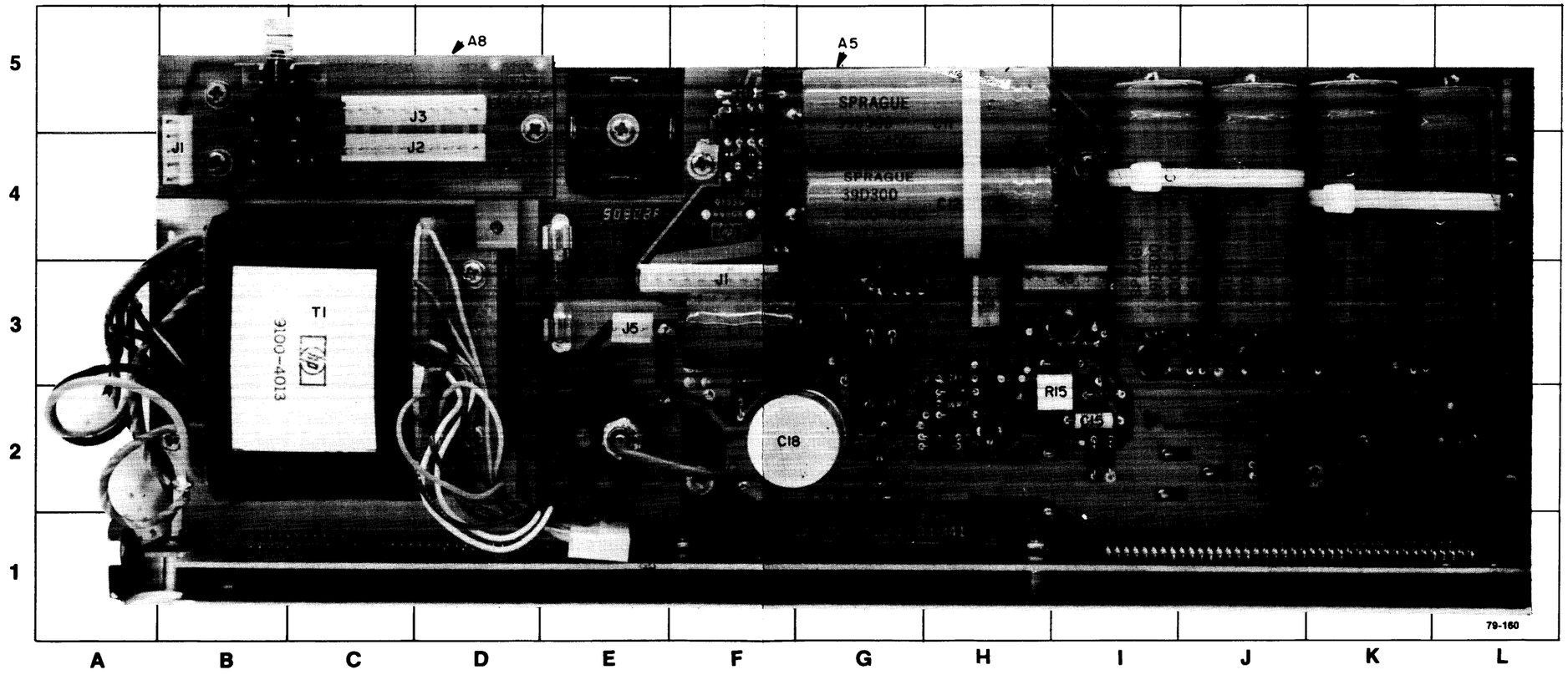


Figure 8-44. Power Supply Board A5 Component Locator

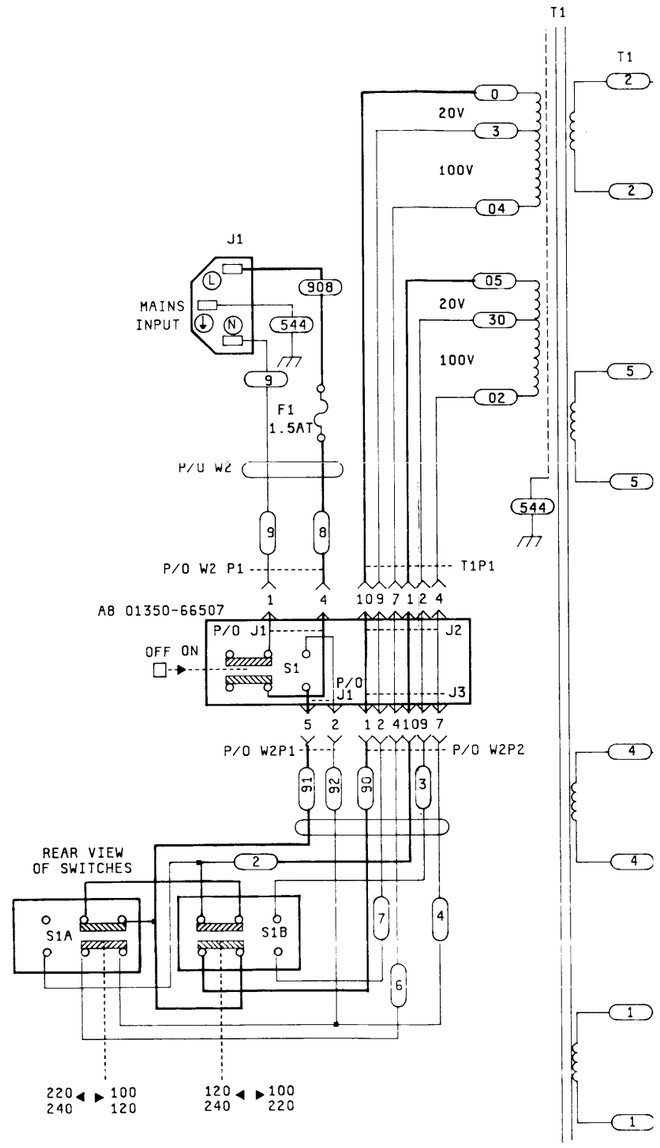
Mnemonics on Power Supply Board A5

L = DATAL — Low level turns front panel LED on. Low when data is being received.

L = POWER INTERRUPT — Low level indicates a line voltage fluctuation or power interrupt has occurred. Stays low until power is reset or instrument receives a DC4(20) ASCII command via HP-IB.

L = PROGL — Low level turns front panel LED on. Low when program — Control Board or I/O Board instructions — are being received.

LINE SYNC — This signal, generated on the Power Supply board, is used to signal the start of the next frame. Sync rate is 120 Hz.



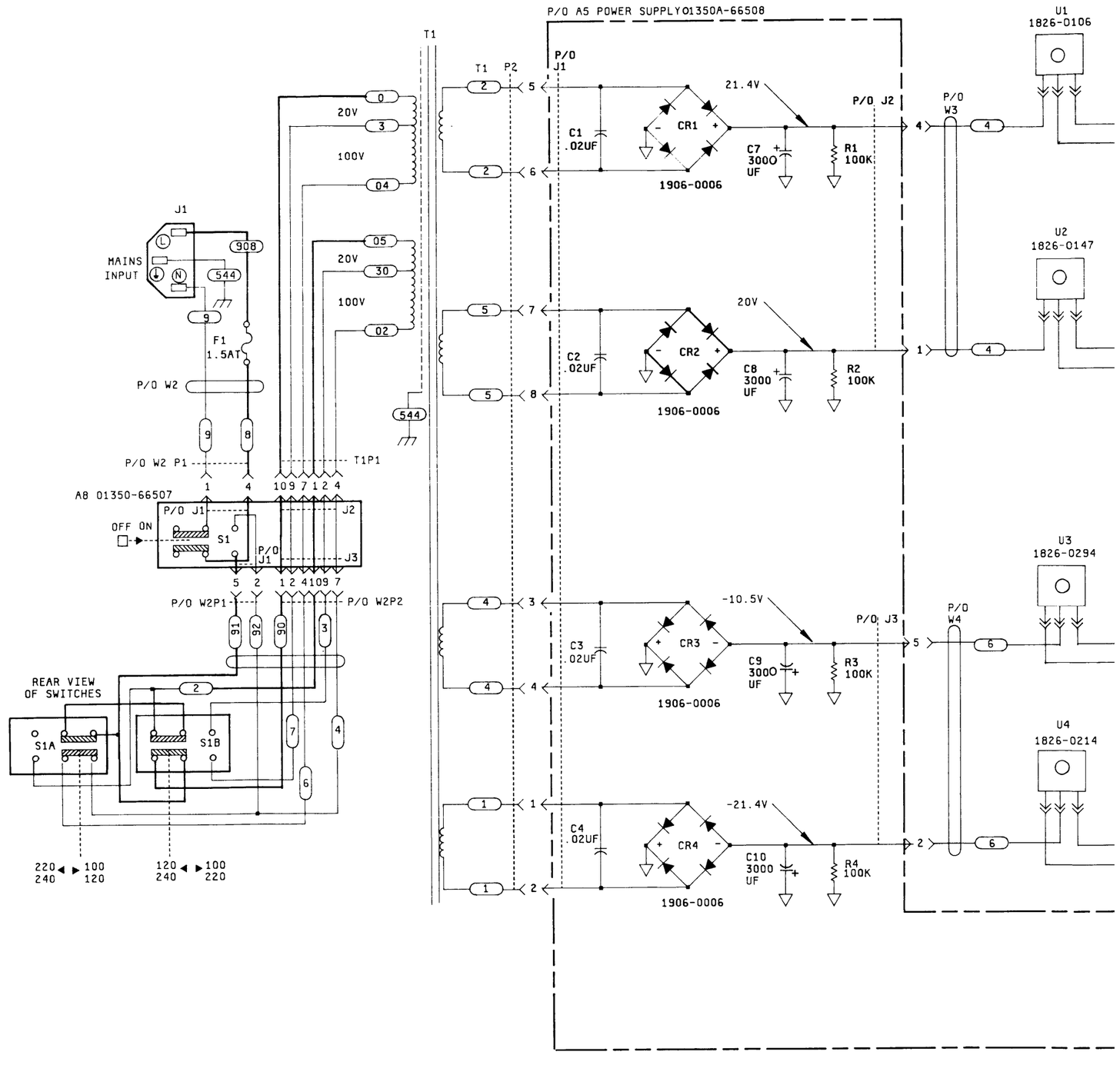
Board A5

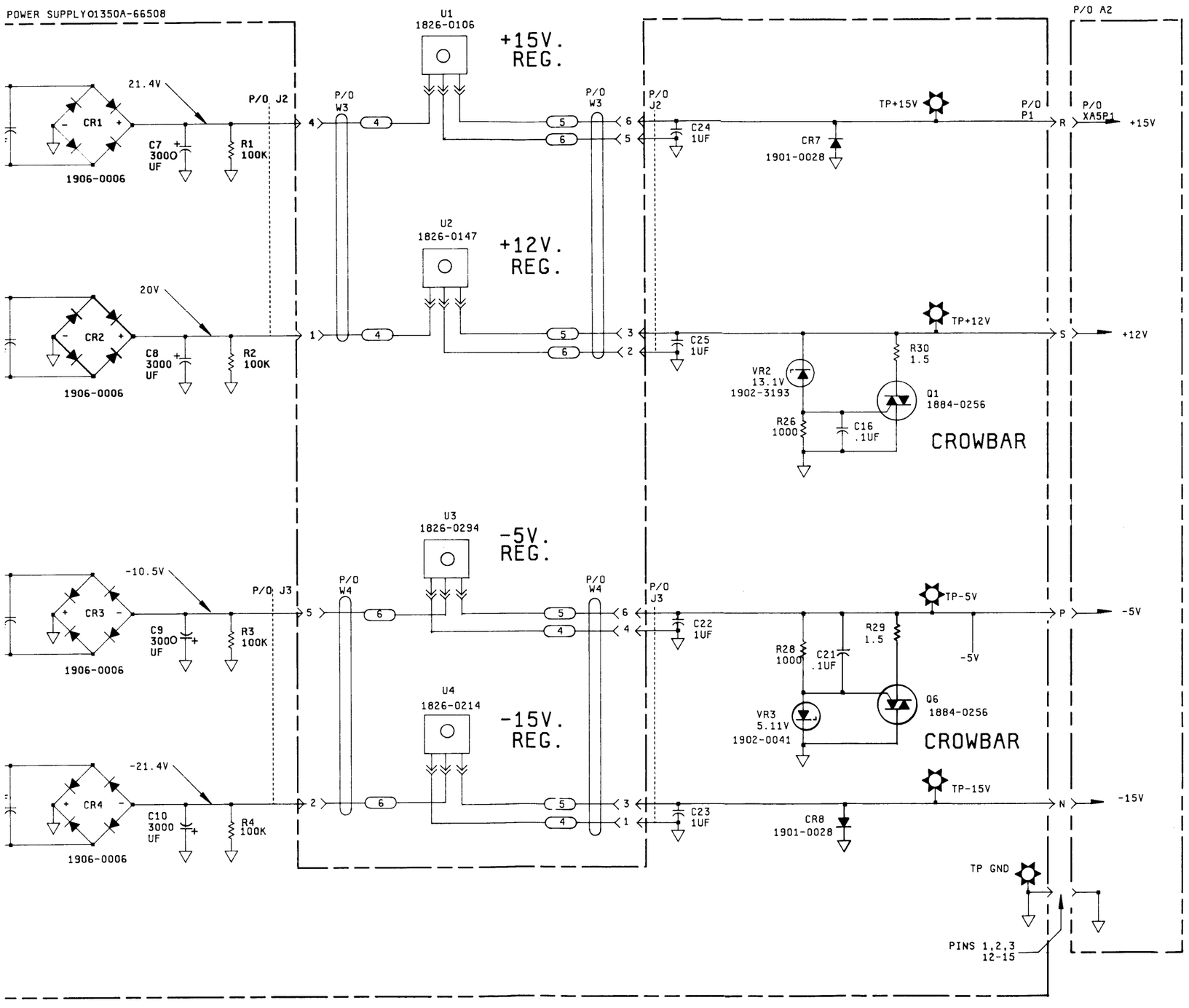
ıen data is being received.

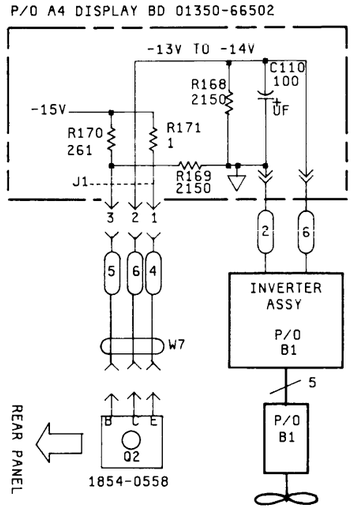
fluctuation or power inter-
or instrument receives a

program — Control Board

›oard, is used to signal the







NOTES:

1. UNLESS OTHERWISE NOTED:
   RESISTANCE IN OHMS
   CAPACITANCE IN PICOFARADS
   INDUCTANCE IN MICROHENRIES
2. 120HZ RIPPLE ON +15V SUPPLIES MUST NOT EXCEED 0.050V P-P

PARTS ON THIS SCHEMATIC

A4	A5	A8	CHASIS
C110 J5 R168-171	C1-4,7-10, 16,21-25 CR1-4,7,8 P/O J1,2,3 Q1,6 R1-4,26, 28-30 VR 2,3	J1-3 S1	B1 F1 J1 P1-4 Q2 S1A,B P/O T1 U1-4 W2-4,7

1350/110

6A

Figure 8-45.
Schematic 6A

8-99. SCHEMATIC 6B PRINCIPLES OF OPERATION.

Schematic 6B contains the Switching Regulator +5 V supply, Line Sync Generator, and front panel LEDs.

8-100. +5 VOLT POWER SUPPLY.

The +5 volt power supply is a switching regulator type and is used to power all the integrated circuits except for the Random Access Memories (RAMs).

The ICs in the instrument are protected by an Overvoltage Crowbar circuit consisting of A5Q5 and A5VR1. A5VR1 is connected to the output of the regulator circuit. If an overvoltage condition occurs then VR1 conducts, turning on A5Q5 to open the Line fuse. The approximate firing voltage for the crowbar is +5.75 volts.

Q1 (located on the rear deck above the fan) is used as a switch. The duty cycle (on/on+off time) is controlled by A5U1. The duty cycle changes, depending on the load, to keep the charge across A5C18 equal to 5 volts. When Q1 is on, the charge rate of A5C18 is controlled by A5L1 producing a ramp. When an upper limit is reached Q1 is turned off, A5CR6 conducts, and the energy stored on A5L1 dumps into A5C18. When the voltage across A5C18 decays to a lower limit Q1 is again turned on and the process repeats.

A5U1 senses the charge across A5C18 and compares it to an internally generated reference of +7.15 volts divided down to +5 volts by A5R14-16. Oscillation (Q1 on-off cycle) is sustained by feedback from A5C17 and A5C15.

A5Q3 functions as a driver for Q1. A5Q4 limits the maximum charge current into A5C18, protecting Q1.

8-101. LINE SYNC GENERATOR.

The Line Sync Generator is an overdriven amplifier which generates a 2-times-line-frequency square wave to sync the display to the line. A switch on the rear panel enables the LINE SYNC feature (see Schematic 3D). A5CR5 is a full-wave rectifier that provides the 2-times-line-frequency switching action.

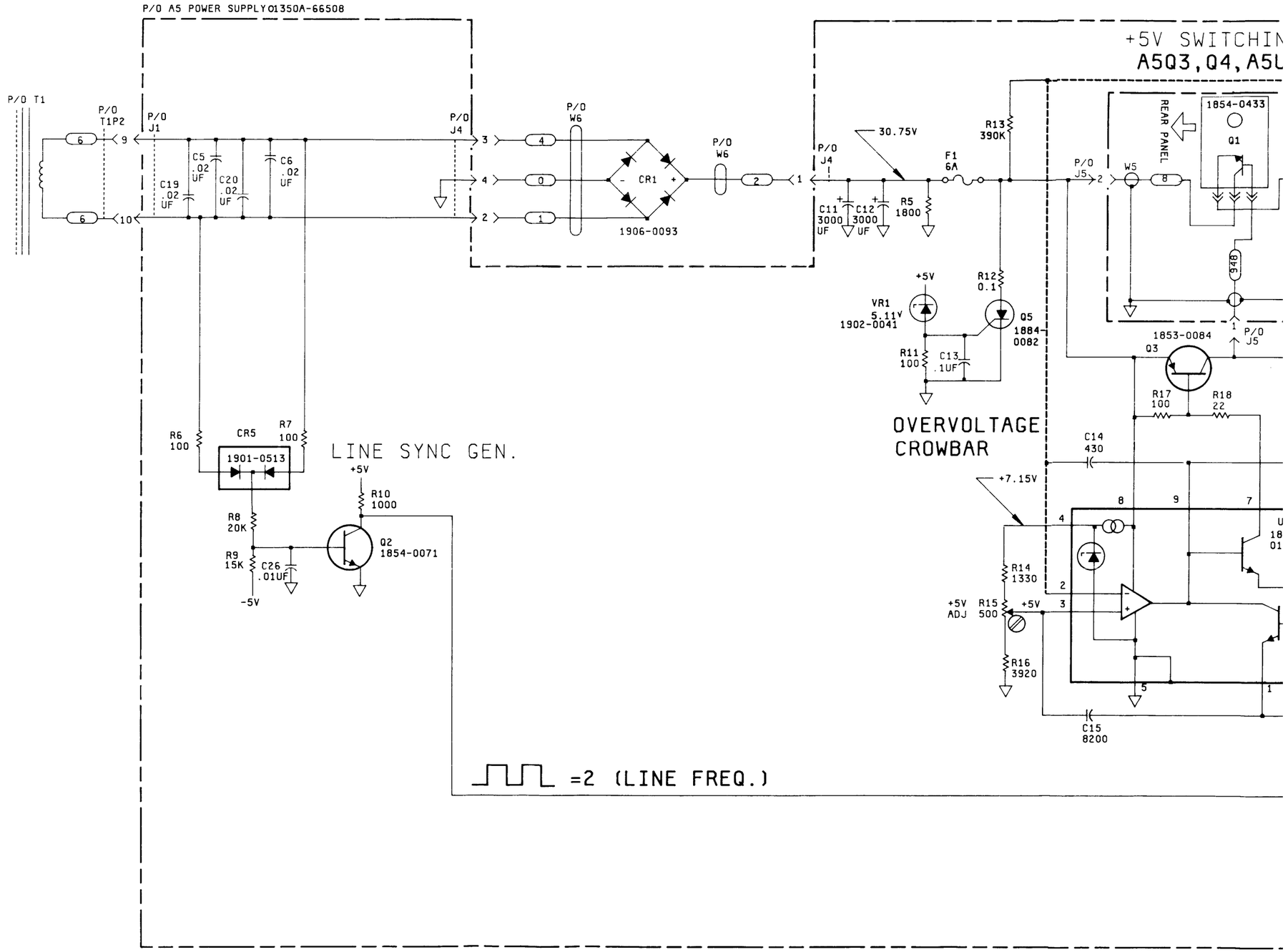
8-102. TROUBLESHOOTING.

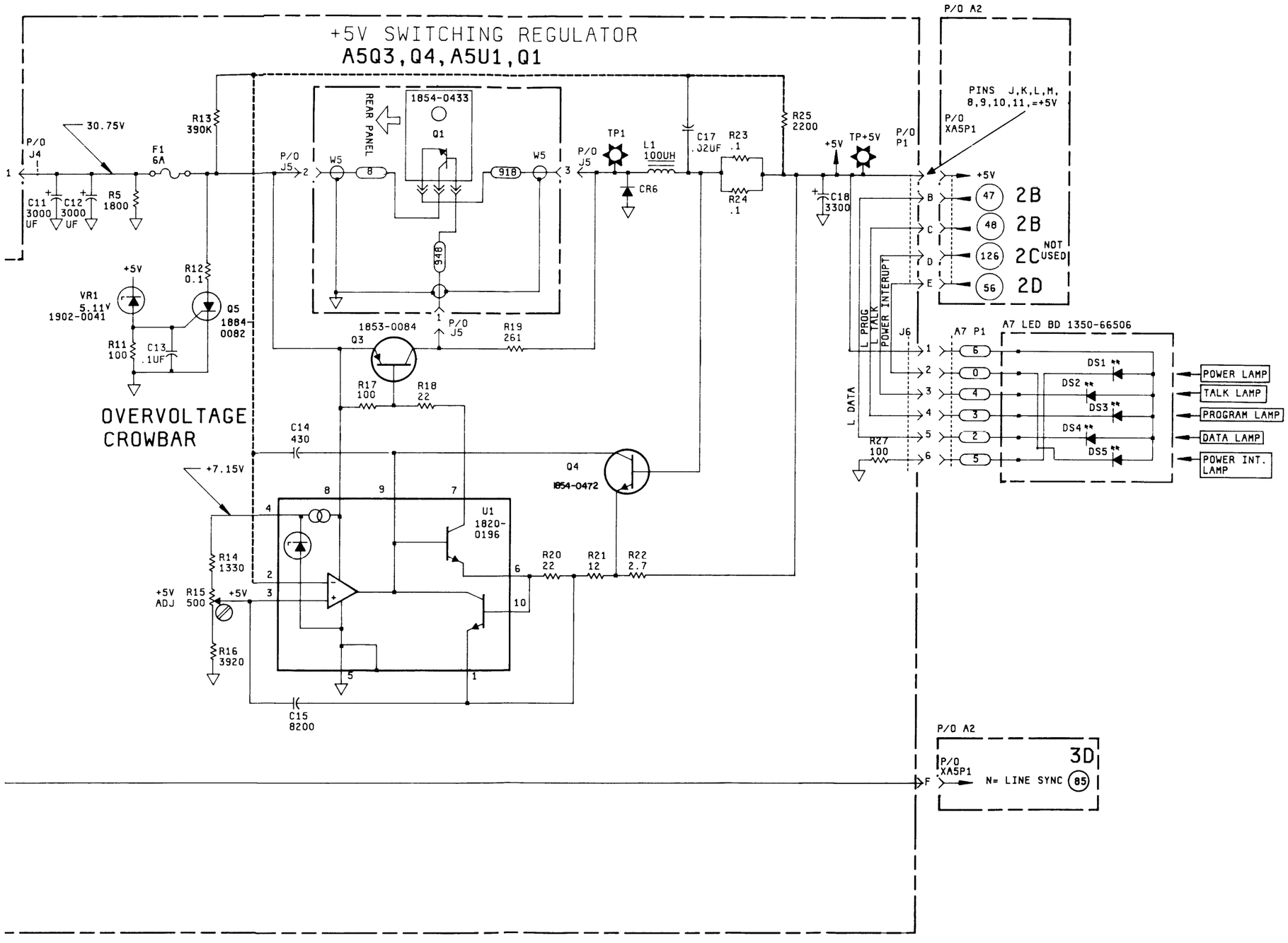
Check for the proper voltage at the fuse. If the +5 V Switching Regulator will not oscillate check Q1, A5Q3, A5Q4, and A5U1. U1 is best checked by simply replacing it. The following list gives the expected voltages and waveforms around A5U.

pin 1 ..... +5 V
pin 2 ..... +5 V
pin 3 ..... +5 V
pin 4 ..... +7.15 V
pin 5 ..... Ground (connected to chassis)
pin 6 ..... +5 V with +0.5 V pulse ~20 kHz
pin 7 ..... +30 V with -1.5 V pulse ~20 kHz
pin 8 ..... +30 V
pin 9 ..... +5 V with +0.5 V pulse ~20 kHz
pin 10 ..... +5 V with +0.5 V pulse ~20 kHz

Test Point 1 above A5CR6 should have a 30 V 20% duty cycle pulse. This is approximate and varies with the load.

The TALK lamp is not used and will not light.


P/O A5 POWER SUPPLY01350A-66508
P/O T1
P/O T1P2
P/O J1
P/O J4
P/O W6
C5 .02 UF
C20 .02 UF
C6 .02 UF
C19 .02 UF
CR1
1906-0093
30.75V
F1 6A
R13 390K
C11 3000 UF
C12 3000 UF
R5 1800
+5V SWITCHIN
A5Q3,Q4,A5L
REAR PANEL
1854-0433
Q1
P/O J5
W5
+5V
VR1 5.11V 1902-0041
R12 0.1
Q5 1884 0082
R11 100
C13 .1UF
1853-0084
Q3
R17 100
R18 22
OVERVOLTAGE CROWBAR
C14 430
+7.15V
R14 1330
+5V ADJ
R15 500
R16 3920
C15 8200
R6 100
CR5
1901-0513
R7 100
LINE SYNC GEN.
R10 1000
R8 20K
R9 15K
C26 .01UF
-5V
Q2 1854-0071
=2 (LINE FREQ.)



NOTE:

UNLESS OTHERWISE NOTED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

2. 120HZ RIPPLE ON +5V SUPPLY MUST NOT EXCEED 0.10V P-P.MAX. 20KHZ RIPPLE IS 0.050V P-P.

PARTS ON THIS SCHEMATIC

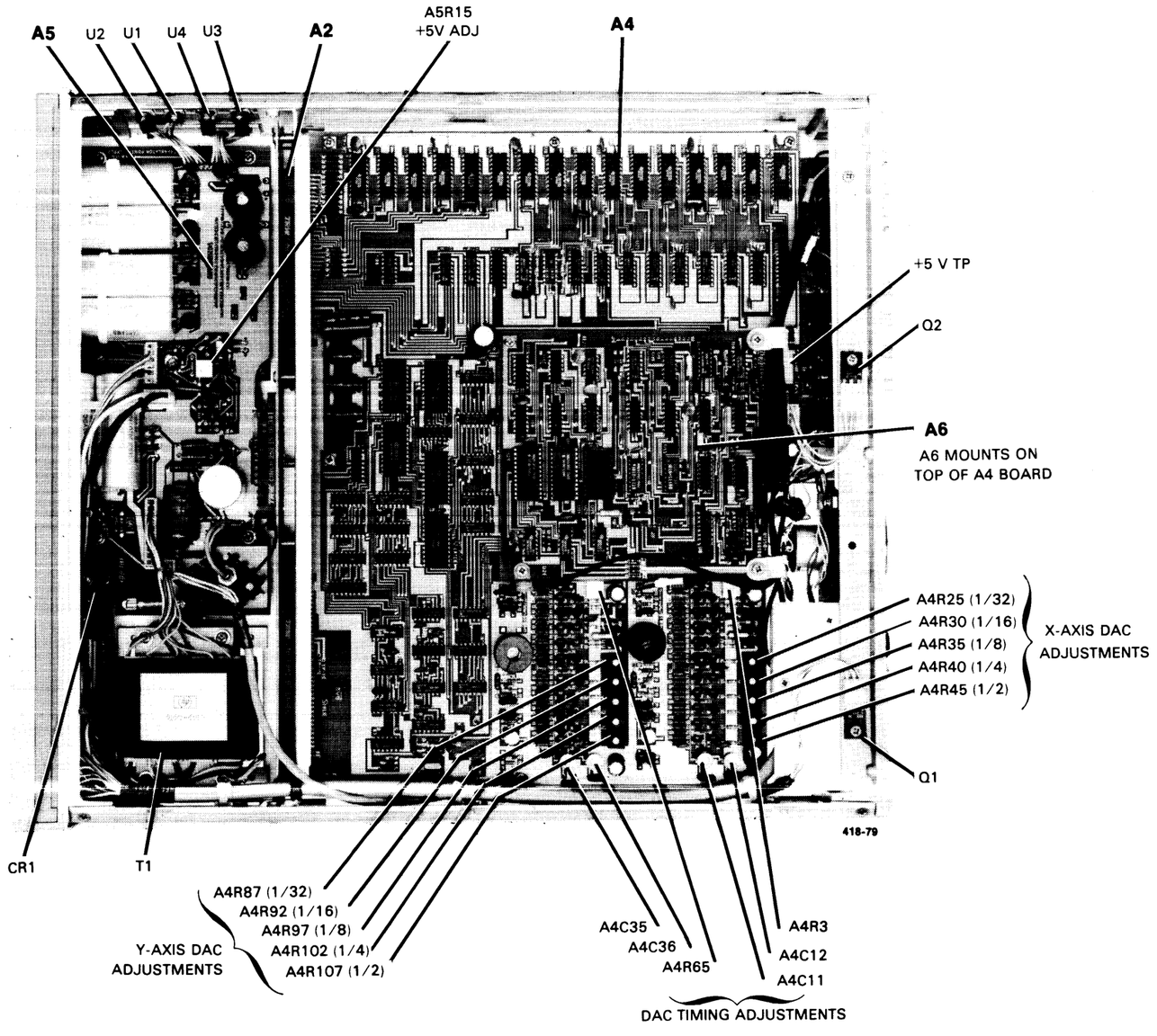
A5 BD.	A2	CHASIS
C5,6,11-15,17-20, 26 CR5,6 F1 J P/O 1,4,5,6 L1 Q2-5 U1	P/O XA5P1 A7 DS1-5 P1	CR1 P/O P4 Q1 P/O T1 W3,5

1350/111

6B

Figure 8-46.
Schematic 6B

TOP VIEW



BOTTOM VIEW

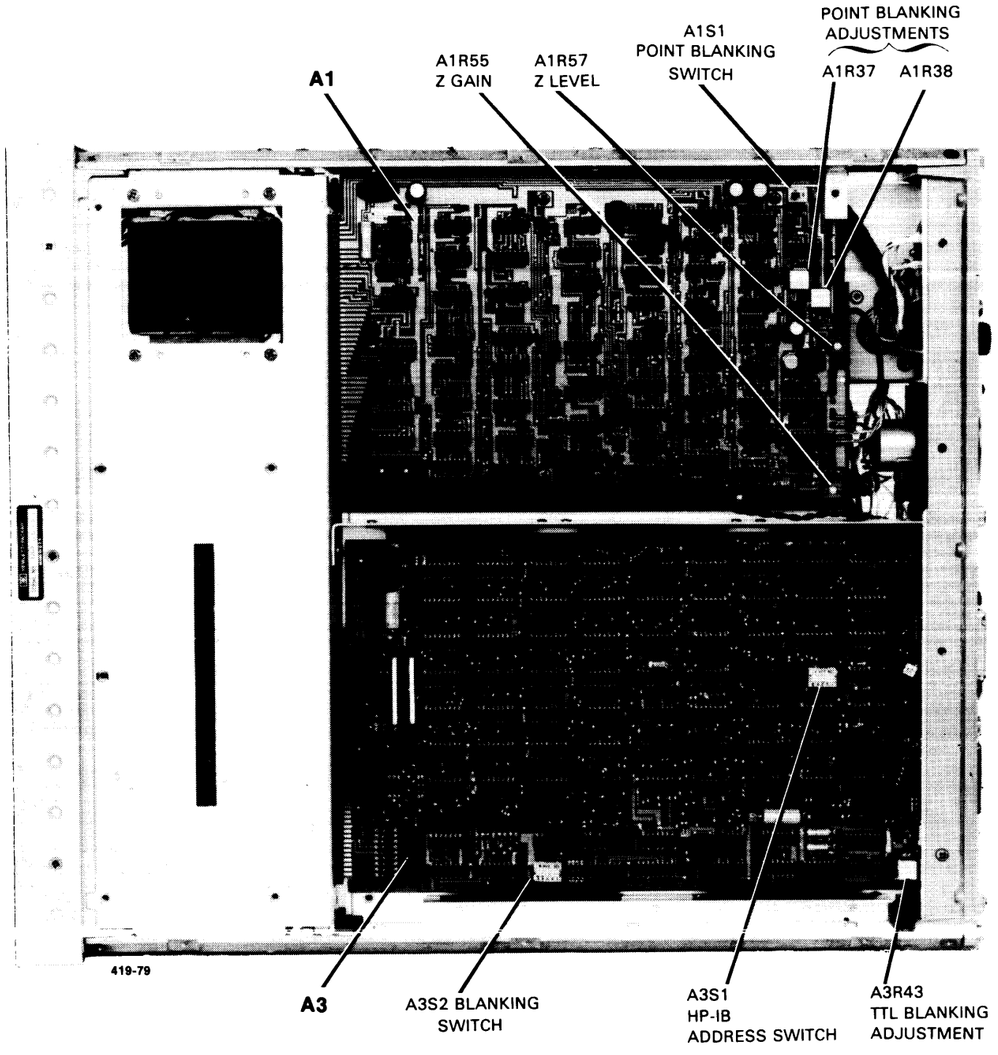


Figure 8-47.
1350A Adjustment Locations