7902A & C/9895K
Flexible Disc Drive
Service Documentation

Hewlett-Packard Greeley Division
3404 E. Harmony Road, Fort Collins Colorado 80525

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7902A/9895K/7902C

Introduction

This service manual contains service information for the 7902A, 9895K and the 7902C flexible disc drives and the controller boards used on the HP 250, 300, 1000, and 3000 series 30 and 33 systems. The following brief history describes the changes that have taken place on the disc drives and controller boards and the reasons for the changes.

The first production model 7902A flexible disc drives were installed in the HP 250, 300 and 3000 systems. The 7902A drives (P/N 07902-68811) designed for use in the HP 250 and the 7902A drives (P/N 07902-60038/07902-60023) for use in the 300/3000 were non-interchangeable. For this reason a common drive (P/N 07902-67914) was developed as a replacement. Refer to service notes HP 250-01 and 7902A-01 for instructions if one of the old drives is discovered in the field. In the past, the drive mechanisms for the 7902A had been manufactured by Shugart and utilized a tri-compliant head design. As of September, 1980, this drive was replaced with one using a bi-compliant head design used on the 7902C.

The drive used on the 9895K is built by CDC and utilizes a tri-compliant head design. These drives are not interchangeable between systems because of differences in drive boards used on the various systems. The drive boards used on the HP 300/3000 systems are designed and built by HP and utilize control signals which are non-industry standard. The drive boards used on the HP 250 systems are designed and built by both Shugart and CDC and utilize industry standard control signals.

The controller board (P/N 45000-66510) used on the old HP 250 systems, and the controller board (P/N 07902-60024) used on the old HP 300/1000/3000 systems, were also non-interchangeable and they both utilized in MC^2 micro CPU. A new controller board (P/N 07902-66520) was designed as a replacement for the 45000-66510 board. If one should fail in the field, refer to service note 07902A-5A for instructions. The controller board used on the old HP 300/1000/3000 systems (P/N 07902-60024) is interchangeable with the new controller board (P/N 07902-66501) designed for use with the 7902C. The new HP 3000 systems no longer use the 7902 disc drives. The 9895A flexible disc drives will be used in place of the 7902.

Repair Philosophy

The 7902A/C/9895K Flexible Disc Drives are comprised of two serviceable areas: the disc drive assembly (mechanical drive assembly with drive electronics assembly) and the controller assembly. These assemblies are serviced on the exchange program with the exception of some parts on the mechanical assembly. The field replaceable parts and field adjustments are outlined in the maintenance section.

Although detailed information is provided in this service manual, it is not recommended that component level repair be performed in the field.

Repair of the 9895K/7902C is restricted to board/drive exchange.

Manual Structure

Introduction

This section describes the structure of this manual and the 7902A, 9895K and the 7902C flexible disc drives. This section may prove useful when troubleshooting the 7902 flexible disc drives due to the many changes which have taken place on disc drives and controller boards. Its intent is to help direct you through the manual to the section that you desire.

DRIVES

	Systems			Refer to:
45000-67914	Old HP-250, 300,3000 1000			Chap 2 Page 2-19
09895-67914		New HP-250		Chap 2 Page 2-50
07902-67902			New HP-300/ 1000	Chap 2 Page 2-56

CONTROLLERS

	Systems			Refer to:
45000-66510	7902A Old HP-250	9895K	7902C	Chap 3 Page 3-24
45000-60024	Old HP-300/ 1000/ 3000			Chap 3 Page 3-45
07902-66510		New HP-250		Chap 3 Page 3-68
07902-66520	Old HP-250 (Repair Only)			Chap 3 Page 3-88
07902-66501			New HP-300/ 1000	Chap 3 Page 3-107

Chapter 1
General Description

Introduction

This section contains a general description of the HP 7902/9895K Disc Drive, and specifications.

General Description

The HP 7902/9895K Flexible Disc Drive is a random-access data storage system employing a flexible medium. The HP 7902/9895K consists of a controller printed-circuit assembly (PCA), a disc drive assembly, and a drive PCA. All necessary operating voltages must be provided by the host system. The controller PCA accepts and interprets commands over the Hewlett-Packard Interface Bus (HP-IB), controls the interface to the disc drive assembly, stores and retrieves data from the disc drive assembly, and returns disc drive and disc operation status information. The drive PCA is mounted in the disc drive assembly and contains read and write circuits, interlocks, and head positioning and head load circuits. The remainder of the drive electronics circuitry is located on the separately-mounted controller PCA.

The flexible medium used in the HP 7902/9895K is a flexible disc. The flexible disc is 20 centimeters (7.9 inches) in diameter and has a 3.8-centimeter (1.5 inch) hole for alignment on the spindle of the disc drive. The disc is enclosed in a protective polyvinylchloride (PVC) jacket with a slot for head access to the recording surface. Both sides of the flexible disc are used for data storage.

The recording head in the disc drive assembly is positioned by a mechanism that includes a stepper motor, capstan, and taut metal band. The mechanism operates in an open loop configuration — there is no positive feedback to determine the actual position of the head. The recording head has two read/write heads, one for each side of the flexible disc. When the heads are loaded, both contact the media. The heads remain loaded for approximately one second after no further commands are received.

The controller PCA contains a micro CPU chip (MC^2 or Z80), a processor-to-HP-IB interface (PHI) chip, read-only memory (ROM), random access memory (RAM), and the associated logic circuits necessary to provide an interface between up to four disc drive assemblies and the HP-IB interface channel. The MC^2 or Z80 handles data and commands directly at the byte level, eliminating the need for direct-memory access (DMA) hardware.

The controller PCA also contains an extensive self-test capability, including options for reading from an already formatted flexible disc and reading and writing on a previously unformatted disc. All self-test functions except reading from a previously formatted disc may be initiated via HP-IB command or by manual switching. The preformatted read self-

test is switch initiated. The controller PCA performs a subset of self-test each time power is applied to the HP 7902/9895K. This subset does not include reading or writing on the flexible disc. Self-test results are available as a four-bit binary word displayed on an LED array mounted on the controller PCA or two bytes of status information which can be read by the host system.

The HP 7902/9895K will read and write the HP standard flexible disc format used on the HP 9885 Flexible Disc Drive on either single-sided or double-sided flexible discs. The HP 7902/9895K will also read and write the IBM 128 byte/sector standard data interchange format (IBM 3740) on single-sided flexible discs only. When a new (previously formatted) flexible disc is loaded into the disc drive, the controller PCA will determine which format is being used and whether the disc is single or double-sided. Format and disc type are both reported as status information. When a disc is reformatted, the controller PCA performs defective track sparing and track reformatting.

Data transfers can be buffered on a sector-to-sector basis. This allows devices connected to the HP 7902/9895K to access data at any rate up to the maximum burst rate. Unbuffered data transfers may also be done, but this requires that the devices accept data at the rate that the HP 7902/9895K sends it.

A modular replacement philosophy has been implemented in the HP 7902/9895K to minimize on-site repair time. Troubleshooting the HP 7902/9895K is simplified by its self-test diagnostics. In addition, more extensive diagnostic testing using automatic test equipment connected to the controller PCA is possible. These diagnostics are not described in this manual since they are a function of the host system.

Specifications

Recording Specifications

HP Double Density Format

Encoding: Modified modified frequency modulated (M^2 FM)

Rotatinal Speed: CDC— 360 RPM, ±2.0 (±7.2 RPM)

Shugart— 360 RPM, ±3.5 (±12.6 RPM)

Bit Density @ 360 RPM:

Track No.	Head 0 Single/Double-Sided	Head 1 Double-Sided Only
0	3651 BPI*	3736 BPI
38	4702	4845
76	6536	6816

* BPI — Bits Per Inch

Track Density: 48 tracks per inch

Tracks per Surface: 77

Surfaces Per Disc: 2

IBM Single Density Format

Encoding:	Modified frequency modulated (MFM)
Rotational Speed:	360 RPM, ±1 (±3.6 RPM)
Bit Density @ 360 RPM: CDC	3268 BPI, track 76, head 0
Shugart	3200 BPI, track 76, head 0
Track Density:	48 tracks per inch (approx. 19 tracks per cm)
Tracks Per Surface:	77
Surfaces Per Disc:	2

Capacity

HP Double Density Format

Bytes/Sector:	256
Sectors/Track:	30
Tracks:	154 on two surfaces
Bytes/Disc (Formatted):	1.18 megabytes (154 tracks)

IBM Single Density Format

Bytes/Sector:	128
Sectors/Track:	26
Tracks:	77 (head 0 only)
Bytes/Disc (Formatted):	256 kilobytes

Access Time	CDC	Shugart
Track-to-Track Seek:	3ms/track, plus 20ms settling	3ms/track, plus 15ms settling
Maximum Track-to-Track Seek (76 Tracks):	248ms	246ms
Average Track-to-Track Seek:	96ms	91ms
Maximum Rotational Latency:	167ms	167ms
Average Rotational Latency:	83ms	88ms
Maximum Data Access Time (Seek Plus Latency):	415ms	413ms
Average Data Access Time:	179ms	174ms
Head Load Time:	40ms	174ms

Data Transfer Rate	CDC	Shugart
Read Burst Transfer Rate:	190 kilobytes/second	135 kilobytes/second
Write Burst Transfer Rate:	190 kilobytes/second	110 kilobytes/second
HP Format Average Transfer Rate:	25.6 kilobytes/second[1]	23 kilobytes/second
IBM Format Average Transfer Rate:	11.1 kilobytes/second[2]	10 kilobytes/second

Environmental Specifications

Operating Limits

Temperature:	10°C to 40°C (50°F to 104°F)
Relative Humidity:	20 to 80 non-condensing with maximum wet bulb temperature not to exceed 25.5°C (77.9°F)
Altitude:	0 to 4572 M (0 to 15,000 feet)

Non-Operating Limits (Storage and Transit)

Temperature:	−40°C to 60°C (−40°F to 140°F)
Altitude:	−304.8 to 15240M (−1,000 to 50,000 feet)

Alignment Limits

Radial Alignment:	±0.0001 inch (.025 mm) of track center at track 38 for both head 0 and head 1

1 Interleave parameter dependent -- best case every other sector.

2 Interleave parameter dependent -- best case every other sector. If sectors are not staggered, then only one sector per revolution can be transferred in buffered mode -- 768 bytes/second.

Power Requirements

Controller Boards

+5V:	2.5A typical, 2.7A maximum (Note 4)
+12V:	0.25A typical, 0.30A maximum (Note 5)
−12V:	0.08A typical, 0.1A maximum (Note 5)

Drive Board (Shugart)

+5V:	0.6A typical, 0.7A maximum (Note 4)
+12V:	0.8A typical, 1.0A maximum (Note 5)
−12V:	0.8A typical, 1.0A maximum (Note 5)

Drive Board (CDC)

+5V ±5%

1A maximum

+24V ±10%

1.2A maximum

Disc Drive Assembly

86 to 127 Vac at 0.3A typical, 0.44A maximum
50/60 Hz ± 3.5% HP format
50/60 Hz ± 1% IBM format

Note 4: Voltage tolerance for +5V is +5%, −3%.
Note 5: Voltage tolerance for +12V and −12V is ±5%

Safety Considerations

General

This product and related documentation must be reviewed for familiarization with safety markings and instructions before operation.

Safety Symbols

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. it calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

Safety Earth Ground

This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

Before Applying Power

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction), make sure the common terminal is connected to the earth terminal of the main power source.

Servicing

Any servicing, adjustment, maintenance or repair of this product must be performed only by service-trained personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.
Capacitors inside this product may still be charged even when disconnected from its power source.
To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

Drive Select and System Select Switch (HP Drive Board 07902/67914)

The drives connected to a controller board are differentiated by their drive number. The drive number is set between 0 and 2 by the drive select switch.

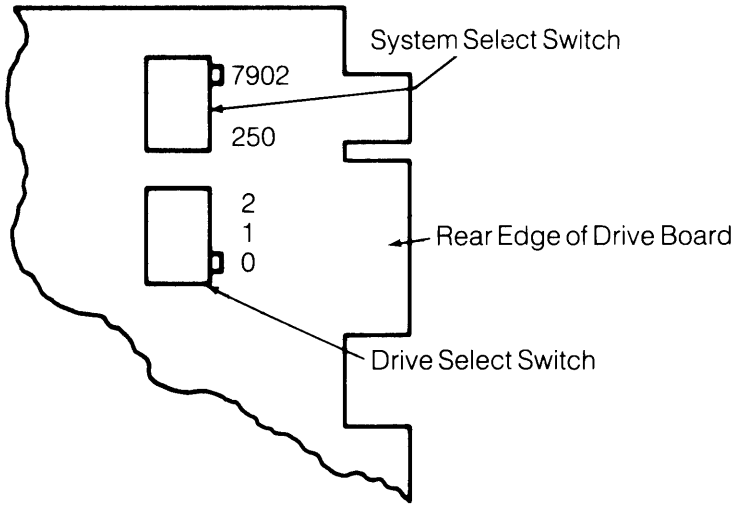


Figure 1-1. Drive and System Select Switches

The system select switch is used to tailor the drive to the system it is to be installed in. When the drive is installed in an HP-250 system, the slide switch must be positioned to "250". When the drive is installed in systems other than the HP-250 the switch must be set to "7902".

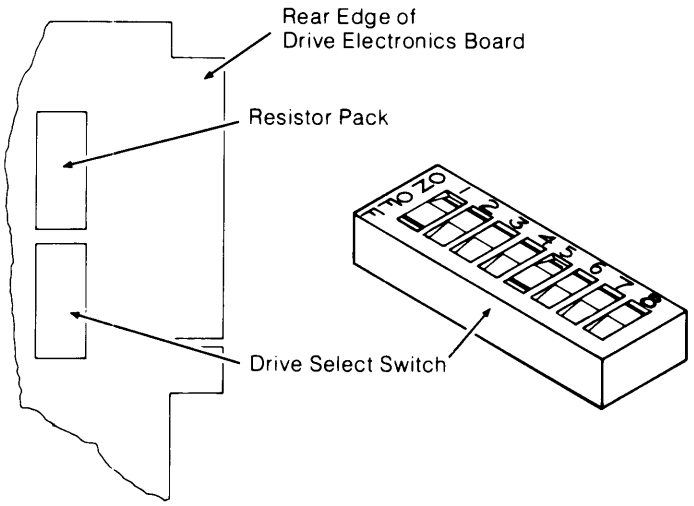
NOTE

When replacing a drive assembly in an HP-250 system, be sure to remove the jumper from J2 on the failed assembly and install it on the replacement assembly.

Drive or Unit Number (CDC Drive Boards)

The drives connected to a controller board are differentiated by their drive number. The drive number must be between 0 and 2. The factory sets drives to 0 and 1.

Set the switch segments according to the following diagram.



Select Code	Segments 1	2	3	4	5	6	7	8
3	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF
2	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF
1	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
0	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON

Figure 1-2. Setting the Drive Number

Flexible Disc Media

The storage medium used in the 7902/9895K is a flexible disc. The flexible disc is 200mm (7.9 inches) in diameter and has a 38mm (1.5 inch) hole for alignment on the disc drive spindle. The disc is enclosed in a protective plastic jacket with a slot for head access to the recording surface. Both sides of the flexible disc are used for data storage.

By using flexible discs identified as "double-sided", up to 1.2 megabytes of data can be stored on each disc. Double-sided, double-density discs (HP part number 92195A, package of ten) are available from HP's computer supplies catalog. Phone orders may be placed by calling the toll free order number 800-538-8787. The disc memory can also handle single-sided flexible discs, allowing slightly over ¼ megabytes of storage using single density recording ½ megabytes using double-density recording. Since some storage is used in

subsystem overhead, the exact amount available for user storage depends upon the controller subsystem. Refer to the appropriate mainframe programming or reference manual for details.

Each flexible disc must be initialized before it can be used for data storage. The initialization procedure marks each disc track, checks for defective tracks, and may establish file directories. Refer to the mainframe programming or reference manual for the correct procedure.

CAUTION

USE ONLY HP MEDIA P/N 92195A. THE USE OF NON-HP MEDIA CAN RESULT IN PREMATURE DISC FAILURE OR DAMAGE TO THE 7902/9895K.

USING NON-HP MEDIA FOR ONE TIME ONLY APPLICATIONS SUCH AS DATA INTERCHANGE WILL NOT DAMAGE THE DRIVE OR DESTROY THE MEDIA, BUT IF REPEATED USAGE IS ANTICIPATED, THE DATA SHOULD BE TRANSFERRED TO HP MEDIA P/N 92195A.

For your convenience, HP offers a package of 10 discs for the 7902/9895K (HP part number 92195A).

Operating Cleanliness

To prevent potential damage or data loss, it's extremely important to maintain the cleanliness of the disc and air within the disc drive. The disc drive should not be operated in an environment in which dust, smoke, moisture, oil or chemical vapor, or other foreign matter are present. Also, be sure to strictly follow the disc handling guidelines.

The critical elements involved in the read/write process are shown below. The read/write heads must maintain contact with the disc during read and write operations. Also shown are various types of contaminants and their size relationships. A contaminant particle hard enough and of the right size may scratch either the oxide coating or the head surface. Even if not hard enough to scratch, it may be large enough to lift the head from the surface, causing data errors.

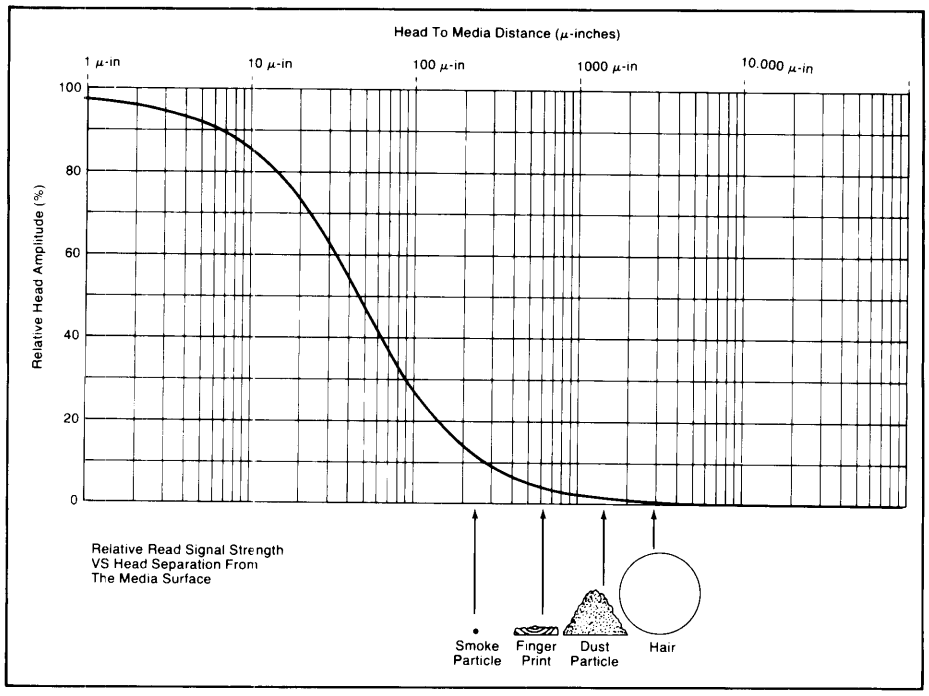


Figure 1-3. Head/Media Critical Requirements

Handling Discs

The flexible disc is basically maintenance free, but it is delicate and MUST BE HANDLED CAREFULLY. Remember, the disc contains your valuable data and programs and should be treated accordingly. A good rule of thumb is to treat your disc as you would a valuable record album. Here are some specific Do's and Don'ts to avoid loss of data or damage to your discs.

EVEN A LITTLE CARELESSNESS IN DISC HANDLING CAN DRAMATICALY REDUCE THE LIFE OF THE DISC.

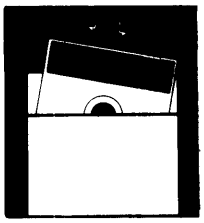
DO

Backup Discs Frequently

There is always a chance of losing data when mass storage devices are accessed. There are many causes in any computer system — a programming bug, operator error, power failure, or hardware failure. In the case of flexible discs, another mode is possible — media failure from contamination or wearout. YOUR ONLY PROTECTION AGAINST DATA LOSS IS FREQUENT BACKUP OF YOUR FILES.

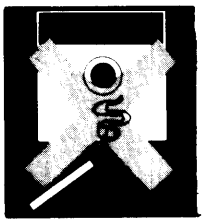
DO

Return Disc to Storage Envelope When Not In Use



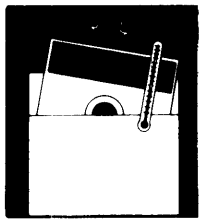
This is the single most important thing to remember about handling your disc because it prolongs disc life by protecting it from dust and scratches. Between uses discs should be stored upright in a dust free container. The box the discs are shipped in, or a similar container, is a good choice.

Operate Your System In a Clean Environment



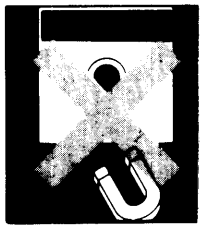
Airborne contaminates and particles accidently dropped onto the disc will cause your disc to wear out prematurely and may cause unreliable data storage and retrieval operations. Some of the most common contaminates are DUST, SMOKE, ASHES, ERASER CRUMBS, and BREADCRUMBS. Chemical vapors may also cause premature wearout.

Maintain Proper Temperature and Humidity



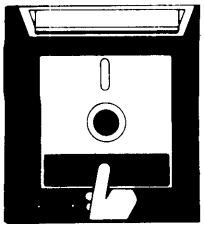
The proper operating range is 10 C (50 F) to 40 C (104 F) and 20% to 80% relative humidity. While temperature is usually easy to control, it may be necessary to make special provisions to keep the humidity in the proper range. Although the disc will continue to operate outside the normal humidity range, it will wear out more quickly and will have a higher error rate.

Avoid Magnetic Fields



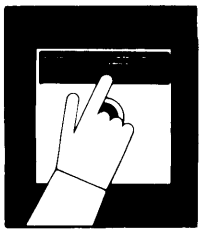
Since the data is stored as a pattern of magnetic fields on the disc, it can be erased by an external magnetic field. Avoid placing a disc near power transformers, magnets or large disc memories. Additionaly, while HP goes to great lengths to confine the magnetic fields produced by it's CRT deflection shields (so well that some our discs drives are mounted in the same cabinet as the display) CRT's with magnetic deflection systems have been known to wipe out discs, and it is a good idea to avoid placing discs on top of CRT's.

Remove Disc From Drive When Not In Use



Remove the disc completely from the drive when access is not needed for an extended period of time. The disc continues to rotate as long as it is in a drive which is turned on, even if it is not accessed. This rotation will eventually wear the disc out.

Use a Felt Tip Pen tp Label Your Disc



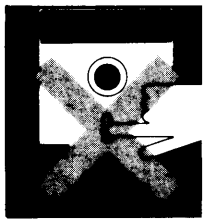
Use a soft felt tip pen to label your disc, and be careful to write only in the label area. Avoid the exposed media while labeling the disc. If possible, write on the large labels provided BEFORE applying them to the disc.

Replace Discs Frequently

Although discs are designed to provide several million revolutions of useful life, they will eventually wear out. The life of a disc is VERY dependent on how carefully it is handled and how much it is used. A disc used sparingly (less then 20 minutes a day) should last over a year. A disc that is used heavily (more than 2 hours a day) should not be expected to last more than 3 months. To be safe, you should copy your data to a new disc and discard the old disc every 3 months for a heavily used disc or at least once a year, even for lightly used discs. If you ever see visible signs of abrasion on the disc, do an immediate backup and discard the worn disc.

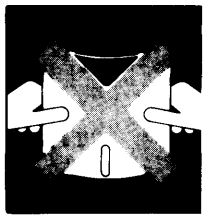
DON'T

Do Not Touch the Surface of the Disc



The thickness of a fingerprint is enough to lift the head off the disc and cause errors. The oils in a fingerprint will also collect dust which can cause a disc to wear out sooner than it normally would.

Do Not Bend or Fold the Disc



The disc is flexible but will not operate if it is creased. Using ball point pens, rubber bands, paper clips, etc. can crease the disc.

Do Not Try to Clean a Disc

The inside surface of the disc jacket is covered with a special material that cleans the disc as it rotates. Any other method of cleaning may cause solvent damage to the media or scratch the disc, causing loss of data. If a disc becomes dirty or scratched, immediately transfer the data to a new disc and dispose of the old disc.

CAUTION

IF YOU EVER DESTROY MEDIA (IF IT LOOKS ANYTHING LIKE THE PHOTO BELOW) IN YOUR 7902/9895K STOP USING THE DRIVE UNTIL IT CAN BE SERVICED. THIS IS EXCEPTIONALY IMPORTANT, AS CONTINUED USE OF THE DRIVE WILL DESTROY MORE MEDIA. IMMEDIATELY CALL YOUR NEAREST HP SALES AND SERVICE OFFICE (SEE THE LIST IN THE BACK OF THIS MANUAL FOR THE NEAREST OFFICE.)

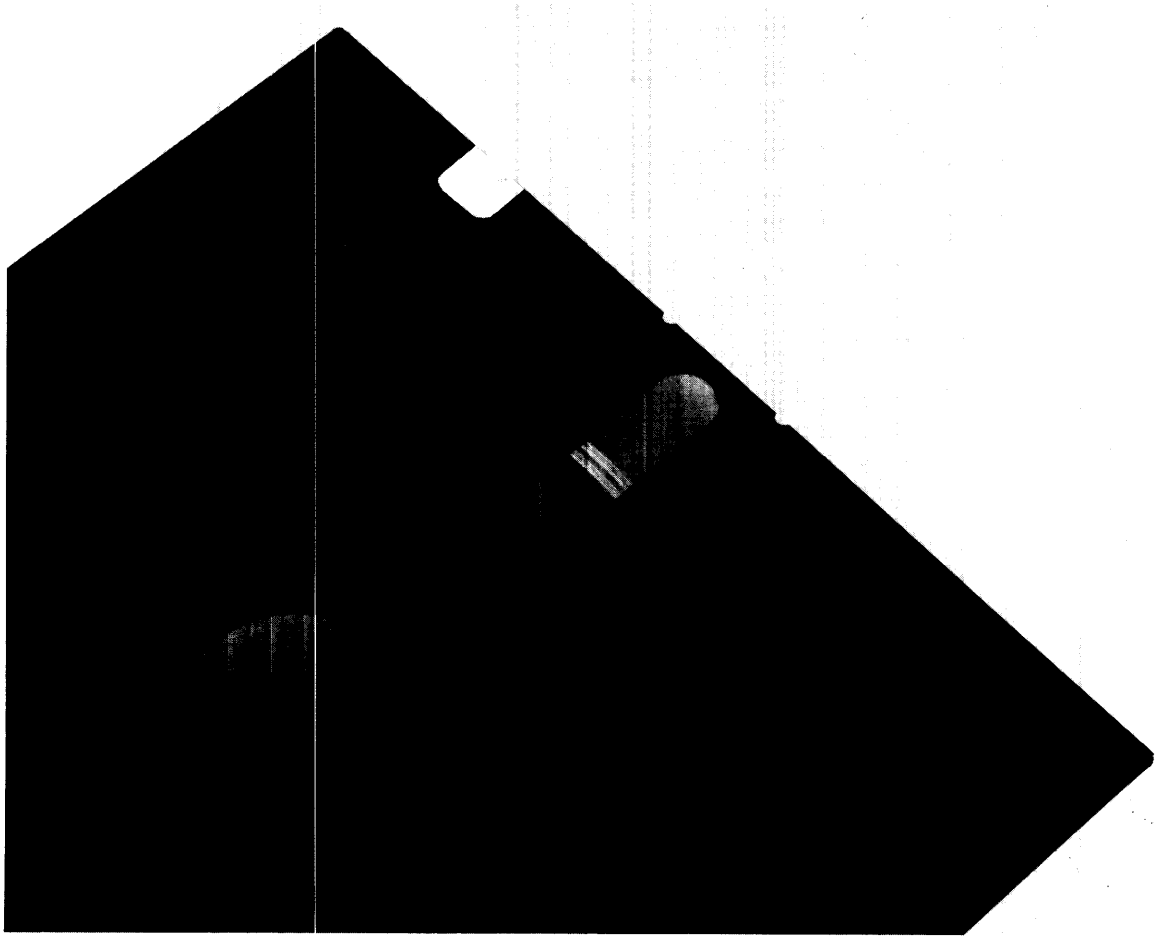


Figure 1-4. Damaged Media

Chapter 2
Flexible Disc Drives

Introduction

This section provides information on operation, theory of operation, interfacing and maintenance of the 7902A, 9895K and 7902C flexible disc drives.

Operation

Refer to Figure 2-1 for proper loading of the flexible disc medium into the disc drive. To load a disc properly, perform the following steps:

NOTE

Disk loading or unloading must be done while the drive power is applied and the drive spindle is rotating.

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1. Open the door on the front of the drive by depressing the release button.
2. Insert the disc into the drive, with the lable toward the operator.
3. Press the door handle down until it locks into place.

There are no operator controls on the 7902A/7902C/9895K disc drives.

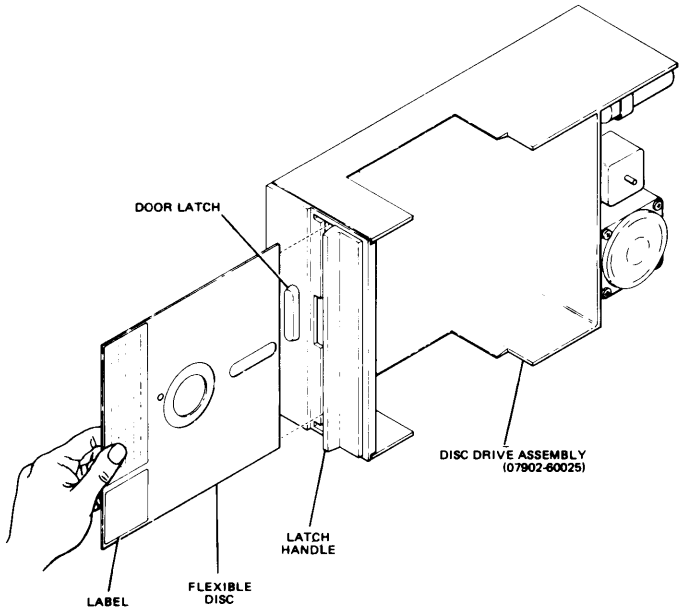
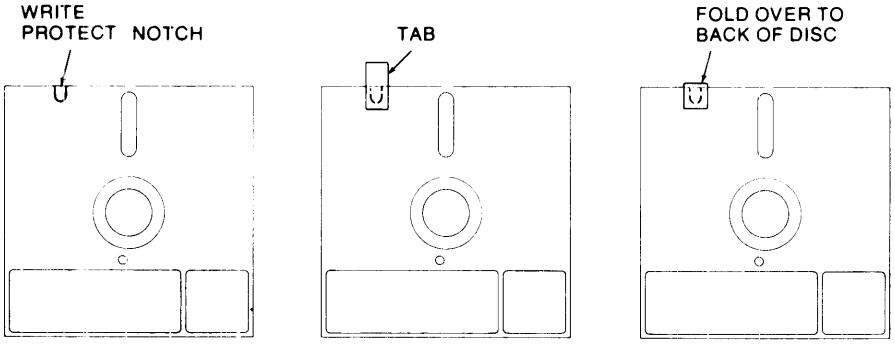


Figure 2-1. Flexible Disc Loading Details

Write Protection

Data and programs stored on a flexible disc can be protected from being written over. The disc is "write-protected" by uncovering a notch in the sealed protective jacket. When the notch is covered, as shown below, writing is allowed. HP discs are supplied with the notch covered, enabling you to write on the disc. Any opaque tape, can also be used. **Remember, fingerprints can be disastrous to your data, so be careful not to touch the surface of the disc.**



General Description

The disc drive assembly consists of a drive mechanism, read/write heads, a head positioning mechanism, and control interlocks. Drive Board A2 includes read and write circuits, control circuits for head positioning and loading, and read, write, and erase enabling.

Drive Mechanism

The drive mechanism is composed of a drive motor, spindle hub, and drive belt. The drive motor rotates the spindle at 360 rpm through the drive belt. Constant rotational speed is achieved for 60 Hz or 50 Hz primary power by changing the drive motor pulley and belt. A registration hub, centered on the spindle hub, positions the flexible disc. A hub clamp that moves in conjunction with the cartridge guide fixes the flexible disc to the registration hub.

Read/Write Heads

The read/write heads are single-element ceramic devices with straddle head erase elements to provide erase areas between tracks. The heads, one for each side of the disc, are mounted on a carriage assembly that is positioned by a stepper motor. The flexible disc is inserted through a disc access door on the front of the disc drive and is held in place perpendicular to the read/write heads by a plate located on the drive frame. During a read/write operation, the heads are in direct contact with the disc.

Head Positioning Mechanism

A mechanism that includes a stepper motor, capstan, and taut metal band positions the read/write carriage assembly on the flexible disc. The stepper motor, driven by signals from drive board A2, rotates in 3.6-degree increments moving the heads one track per increment. The HP-IB channel supplies controller board A1 with head positioning commands which in turn supplies positioning data to A2.

Drive Electronics

The drive electronics circuitry is contained on drive board A2 which is attached to the bottom of the disc drive frame. A2 is connected between the controller board A1 and the various electromechanical components of the disc drive thereby providing the necessary interface for disc drive operation. A2 recognizes when the disc drive is selected and initiates the proper head positioning and loading actions. For write operations, A2 turns on write and erase current generators and provides the correct write current transitions. During read operations, data obtained from the flexible disc is amplified and conditioned, and sent to controller board A1. A2 also contains interlock circuits that prevent drive operations when the disc access door is not closed and latched, the heads are not loaded, or the flexible disc is write protected. In adition, A2 makes available status information.

Functional Description

The following paragraphs provide a functional description of the circuits on drive board A2 and the operation of the associated disc drive electromechanical components. Refer to Figure 2-2 for a detailed functional block diagram of A2.

The circuits on A2 are divided into four principle systems: a control system, a head positioning system, a read/write system, and a power supply filtering system. The control system provides the interface between controller board A1 and the disc drive, the head actuating system moves and loads the read/write heads in response to signals from A1, the read/write system reads information from or writes information onto the surface of the flexible disc, and the power supply filtering system filters and distributes the dc voltages from the host system.

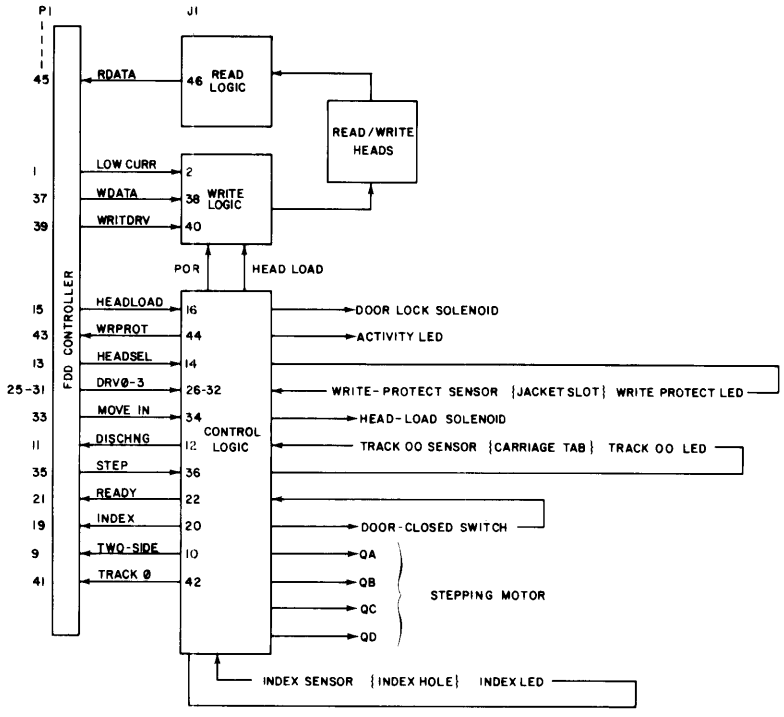


Figure 2-2. Drive Functional Block Diagram

Input/Output Signals

There are 14 signals input to drive board A2 from controller board A1, five signals output from A2 to A1, and two input/output (bidirectional) signals between A2 and A1. These signals, together with identifying mnemonics, are described in the table 2-1.

Logic Signal Notation

In the disc drive logic circuits, a signal is applied to its destination at all times in one of two states: active or inactive. A signal is active when the voltage level (high or low) is such as to make the action occur for which the signal was intended. This action is usually identified by the signal mnemonic. To indicate the active voltage level of the signals, the mnemonics for all active high signals have an "H" suffix and the mnemonics for all active low signals have an "L" suffix. Table 2-2 uses an active high signal (REDYH) and an active low signal (TRKOL) to summarize the details of the signal notation system.

Table 2-1. Drive Board A2 Input/Output Signals

Mnemonic	Signal	Function
	Output to Controller PCA	
INDXL	Index	Active when index hole in flexible disc passes index photodetector. Signal is active once per revolution of disc (6 times/second).
REDYH	Ready	Active when disc drive is in a ready state, i.e., a disc is in drive and spinning, drive is select, heads are loaded, and head 1 is not selected with single-sided disc.
SPINL	Spinning	Becomes active after a Reset Spinning (RSPNH) if the disc drive is nominally up to speed. Also alerts controller PCA to removal and insertion of a new flexible disc.
TRK0L	Track Zero	Active when read/write heads are positioned at track zero (outermost track used on disc).
WPRTL	Write Protect	Active when flexible disc in disc drive is write protected (allows reading only).
	Input from Controller Board	
DLCKL	Door Lock	When active and held by control latch, locks disc access door (without regard to heads being loaded).
DSLVL	Drive Select Valid	When active, validates Drive Select signals DSLOH, DSL 1H, and DSL2H.
DSLOH, DSL1H, DSL2H	Drive Select	Binary-coded decimal signals used to identify disc drive with which controller desires to communicate.
HDACTL	Head Load	When active and held by the control latch, signal enables stepper, loads heads, and locks door.

Table 2-1. Drive Board A2 Input/Output Signals (Continued)

Mnemonic	Signal	Function
	Input from Controller PCA (Continued)	
HED1H	Head One	When active and held by the control latch, it selects head 1. When inactive, head 0 is selected.
LDCTL	Load Control	When active, with drive selected and not in a write mode, clocks the control latch which latches input signals HDACTL, PHIBH, DLCKL, and HED1H on the drive PCA.
PHIBH PHIAH	Phase B Phase A	When held by control latch, generates signals which drive stepper motor in head actuator assembly.
PONH	Power On	When active, enables the control gates that activate the write circuits. Write is allowed if drive is selected and ready, write mode is selected, and disc drive does not contain a write-protected flexible disc.
PORH	Power On Reset	When active, resets control latch index counter and spinning flip-flop. This reset action disables stepper, unloads heads, unlocks door, selects head 0, and makes SPINL inactive.
RSPNH	Reset Spinning	When active, clocks output of the Index Counter into the spinning (SPINH) flip-flop.
WRIT	Write	When active, places disc drive in write mode.
	Output To/Input from Controller PCA	
DATAH DATAL	Data	Bidirectional differential lines carrying read and write information to and from the controller PCA.

Table 2-2. Logic Signal Notation

Signal Mnemonic	Volage Level	State	Message Transmitted
REDYH	high	active	Drive ready
REDYH	low	inactive	Drive not ready
TRKOL	low	active	Read/write heads at track 0
TRKOL	high	inactive	Read/write heads not at track 0

Control System

The control system responds to inputs from controller board A1 and places the disc drive in a write mode or a read mode. In addition, the system provides A1 with drive status information. To ensure that the drive mechanism is in the correct condition for reading and writing, the control system also monitors the state of four photodetector sensors and a door-closed switch in the drive mechanism. The actions of the various circuits comprising the control system are discussed in the following paragraphs.

Drive Select

To permit the controller board A1 to communicate with one disc drive at a time, each disc drive is assigned an identity number between 0 and 7. A1 uses this number to select the disc drive with which it desires to communicate. Drive board A2 employs a comparator to decode the identity number. The comparator compares the state of binary-coded decimal Drive Select inputs DSL0H, DSL1H, and DSL2H from A1 with BCD inputs from the front panel Drive Select switch. If the coding of the two sets of inputs coincide, and Drive Select Valid signal DSLVL is active, the drive select circuit outputs Drive Select signal DSLH. If a Drive Select switch is not connected to A2, the circuit defaults to 0.

Door Closed Detector

The disc drive assembly contains a door-closed switch which is activated by the disc guide assembly. The switch has two output lines: Door Open and Door Closed, both of which are active low. The Door Closed line is active when the disc access the door closed detector on drive board A2 to output an active high Door Closed signal. When the disc access door is open, the active Door Open signal resets the detector, causing the output to become inactive.

Write Protect Detector

The write protect detector is a phototransistor assembly mounted on the disc guide assembly. The purpose of the detector is to sense if the write protect slot in the cover of a flexible disc inserted into the drive is open or covered by a tab. The output of the photodetector is coupled to an interface circuit on drive board A2. The output of the interface is active when the write protect slot is open. The output signal from the interface inhibits the write operation by gating off the write interlock which in turn prevents operation of the write current and erase current sources. The output of the write protect photodetector can be observed at a test point labeled WPRTH.

Track Zero Detector

The track detector is a phototransistor assembly mounted on the main casting of the disc drive. The purpose of the detector is to sense when the read/write carriage assembly reaches track 00. The phototransistor output is active for tracks −01, 00, and 01, and inactive for tracks 02 and above. The phototransistor output is connected to an interface circuit on drive board A2. The interface output is AND'ed with the head actuator stepper motor phase A and B drive lines to develop a unique track 0 signal. The signal, identified as TRK0L, is coupled via a line driver to controller PCA-A1. The output of the interface circuit, before it is AND'ed with phases A and B, can be observed at a test point labeled TK0H.

Single/Double-Sided Disc Index Detector

The index detector assembly consists of two phototransistors mounted on the disc guide

assembly. The purpose of the index detector is to sense the presence of the index hole in the flexible disc. One phototransistor senses the index hole of a single-sided disc and the other phototransistor senses the index hole of a double-sided disc. The two outputs from the phototransistors are coupled to an interface circuit on drive board A2. The two interface outputs are OR'ed together to give one output which can be observed at a test point labeled INDEXH. When either a single-sided or double-sided disc is rotating in the disc drive, signal INDEXH is a pulse which occurs once per revolution of the disc. Signal INDEXH is a (connected to an index counter, and b) coupled via an inverting line driver to controller board A1 as signal INDXL. The separate outputs from the interface, before they are OR'ed, can be observed at test points labeled INDEX0L (one-sided disc index pulse) and INDEX1L (double-sided disc index pulse).

Single-Sided Disc Detector
The purpose of the single-sided disc detector is to inform controller board A1 when a single-sided disc is inserted into the disc drive. The detector monitors the state of single-sided disc index signal INDEX0L from the index detector. When INDEX0L is active, the single-sided disc detector output SSDH is active. The detector is reset at power-on and when the disc access door is opened.

Index Counter
The index counter provides Disc Spinning signal SPINH which is active when certain disc drive operating conditions are valid. These conditions are: disc loaded, disc access door closed and latched, and the occurrence of two successive index pulses (an indication that the disc is rotating). The index counter also returns disc drive status information to controller board A1.

The index counter consists of three D-type flip-flops connected in cascade. The clear input to all three flip-flops is derived from the output of the door closed detector and an inverted Power On Reset (PORH) input. As long as the disc access door is open, the clear line is held low and no circuit action can occur. The Q output of the third flip-flop, connected via an inverting line driver to A1, is status signal SPINL. Signal SPINL is inactive at this time since the clear input to the flip-flop holds its Q output low.

As soon as a disc is loaded into the disc drive and the disc access door is closed and latched, the clear line goes high and allows the first two flip-flop to start counting. When a second index pulse occurs, the second flip-flop a) lights an LED labeled B (disc ready) on drive board A2 and the DISC READY LED on the optional front panel indicator display, and b) pulls the D-input of the third flip-flop high. When PCA-A1 checks the status of the disc drive, it pulses the Reset Spinning (RSPNH) line. This action clocks the third flip-flop, causing its Q output to go high. Status signal SPINH is now active. Signal SPINH is also used internally in the A2 circuitry that determines if the disc drive is ready.

Drive Ready
Several signals in the drive PCA-A2 circuitry are gated together to produce status signal Drive Ready (REDYH). The following conditions must be true for REDYH to become active:

- SPINH active, i.e., a flexible disc has been inserted into the disc drive, the disc access door is closed and latched, and the disc is spinning.
- Drive selected with signal DSLH active.

- Heads loaded.
- Head 1 not selected if a single-sided flexible disc is in the disc drive.

Read Enable
The read mode of operation is enabled when Drive Ready signal REDYH is active and the Write (WRITL) input is inactive. These conditions enable a) the output of the read circuit, and b) the driver section of the data transceiver.

Write Enable
The write mode of operation is enabled when Drive Ready signal REDYH is active, the Write (WRITL) input is active, and the Write Protect (WPRTH) line is inactive. These conditions enable the write interlock circuit.

Write Interlock
The write interlock supplies drive to the current switches in the write current and erase current sources when the write enable signal is active. However, operation of the write interlock is inhibited if the Power On (PONH) line is inactive. Both PONH and write enable must be active in order to enable the write interlock. Signal PONH, generated in the host system power supply, is inactive when the ac line voltage input to the supply falls below its low limit specification.

Front Panel Display Drivers
The front panel display drivers provide drive for three LED's on an optional front panel indicator display that can be connected to A2 via connector A2J6. The LED's are labeled DRIVE SELECTED, DISC READY, and WRITE PROTECTED. The DRIVE SELECTED LED is driven by signal HDACTH from the control latch; the DISC READY LED is driven by the Q output of the second flip-flop in the index counter; and the WRITE PROTECTED LED is driven by a signal from the write protect interface. Two LED's on A2 are also activated by the front panel display drivers. These LED's are labeled A (drive selected) and B (disc ready).

Head Actuating System

The function of the head actuating system is load the read/write heads on any one of the 77 tracks on the flexible disc, select either of the two read/write heads for a read/write operation, and lock the disc access door to prevent removal of the flexible disc while the heads are loaded. The system circuits on drive board A2 include a control latch, a head unload delay circuit, a head load driver, a stepper driver, and a door lock driver. Associated electromechanical components on the disc drive assembly include a head load solenoid, a head actuator assembly with stepper motor, and a door lock solenoid.

Control Latch
The control latch retains inverted Head Actuate (HDACTL), Stepper Phase (PHIAH, PHIBH), Door Lock (DLCKL) and Head Select (HED1H) information received from controller A1. The latch is clocked by the Load Control (LDCTL) signal from A1, AND'ed and Drive Select (DSLH) and an inverted Write (WRITL). These signals prevent a) the latch from clocking in new information when the drive is not select or if it is in a write mode, and b) accidental stepping to other tracks when the disc drive is writing on a particular track.

The control latch is reset by the Power On Reset (PORH) input from A1. When reset, the latch is in a state whereby the heads are unloaded, the stepper motor is disabled, the disc access door is unlocked, and head 0 is selected.

Head Unload Delay
The head unload delay circuit delays unloading of the heads for approximately 1.5 seconds after the Head Actuator (HDACTL) signal becomes inactive. This allows the disc drive to respond without any settling delay to another head load command occuring less than 1.5 seconds after the previous one ended. The HDACTL signal from the conrol latch is input to a 1.5-second delay circuit, the output of which is OR'ed with HDACTL. When HDACTL is active, it loads the heads via the OR gate output. When HDACTL becomes inactive, the output of the delay circuit remains active for a further 1.5 seconds, continuing to load the heads for this period. The output of the OR gate also enables the stepper motor driver circuit.

Head Load Driver
The head load driver provides drive to the head load solenoid which, when activated, allows the heads to contact the surface of the flexible disc. The head load driver is energized when the HDACTH signal from the head load delay circuit is active and the output of the second flip-flop in the index counter is active. This gating ensures that the heads cannot be loaded without having a flexible disc in the disc drive. The input to the head load driver can be monitored at a test point labeled HDLDL.

Stepper Driver
The stepper driver provides drive for the 4-phase 3.6-degree per step permanent magnet stepper motor driving the head actuator assembly. The rotary motion of the stepper motor is transformed into linear motion by an actuator mechanism that employs a capstan and taut metal band. Each 3.6-degree step of the motor increments the head position one track.

The 4-phase coils of the stepper motor are connected to form two pairs of 2-phase coils in parallel. Current is driven into the pairs in either direction according to the stepping sequences desired. To switch the direction of current through the coils, the stepper drivers must be able to source current or sink current. Each driver pair is enabled such that one is the inverse of the other. Controller board A1 supplies two phase inputs to drive board A2. These are labeled Phase A (PHIAH) and Phase B (PHIBH). The control latch outputs non-inverted and inverted phase signals QA, QA, QB, and QB to the stepper driver. The stepping sequence for the actuator stepper motor is shown in Figure 2-3. The stepper motor driver is enabled by the output of the head unload delay circuit previously described.

Door Lock Driver
The door lock driver, when energized, energizes a door lock solenoid that holds the disc access door locked by disengaging the latch of the door opening button. The solenoid is energized by either a Door Lock (DLCKL) signal or a Head Load (HDLDL) signal. An LED on A2 labeled D (door lock) monitors the input signal to the door lock driver.

Head Switch
The head switch circuit selects read/write head 0 or head 1 by grounding the center tap of the selected head. This grounding action forward biases diodes in the input circuit of the

read preamplifier allowing it to pick up the output of the selected head. When in the write mode the grounding forward biases diodes in the write current source and the erase current source, allowing the sources to supply current to the selected head. The two outputs from the head switch circuit can be monitored at test points H0CTL (head 0) and H1CTL (head 1).

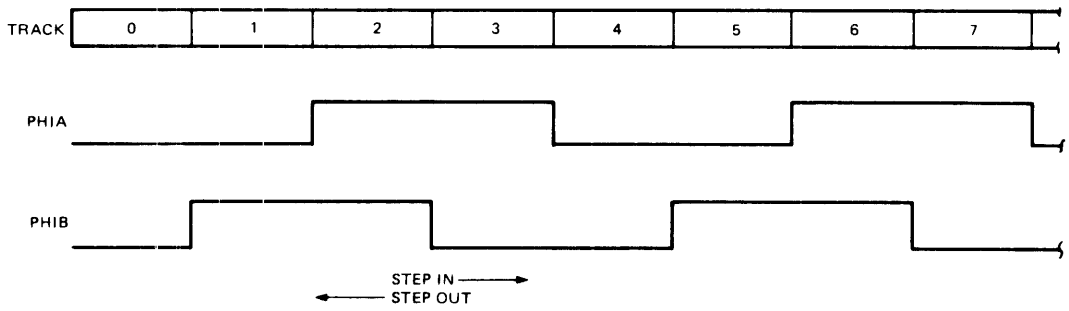


Figure 2-3. Stepper Motor Switching Sequence

Read/Write System

The function of the read/write system is to provide the means to read information from or write information onto the surface of the flexible disc. Included in the following paragraphs are functional descriptions of the read/write heads, the read mode of operation, and the write mode of operation.

Read/Write Heads

Each read/write head is a gapped ferrite core housed in a ceramic shoe (or slider). The head rides in direct contact with the surface of the disc. Two read/write windings are wound around the core. The windings are connected to a common point and phase such that the common point acts as a center tap. The windings are used for both reading and writing by detecting or providing a magnetic flux change at the gap in the ferrit core. An erase coil, wound on a yoke spanning the track being written by the read/write head, provides a constant megnetic field perpendicular to the read/write head. The erase coil is energized during the write operation and results in the outer edges of the track being trim erased. The erase head ensures that the track being recorded does not exceed the 0.012-inch track width. It also allows for minor deviations in read/write head current so that as one track is recorded it will not "splash over" to adjacent tracks.

Each data bit/clockpulse written is directed to alernate read/write coils, thus causing a change in the direction of current flow through the read/write head. The alternate switching will cause a change in the flux field of the core for each bit. The current through either of the read/write coils will cause the previously recorded information on the disc to be erased as new information is recorded.

On a read operation, as the flux field direction changes on the disc surface as it passes under the core gap, current will be induced into the windings of the read/write head. This current will result in voltage output of differing polarity. When the next bit passes under the gap, another flux reversal in the recordng surface takes place. This flux change reverses the induced head current, causing a polarity reversal of the voltage output pulses.

Read Mode Operation

As the surface of the flexible disc moves under the data head, the magnetically stored flux field intersect the gap in the ferrite core of the head. The motion of the flux reversals passing the head gap causes a current to be induced into the read/write windings wound around the core. The resulting voltage are converted to pulses and coupled to controller board A1 where they are analyzed to define the data recorded on the surface of the disc. Each flux field reversal, caused by a write current polarity change, generates a readback voltage pulse.

Read Circuit

The read circuitry on drive board A2 is enabled in the read mode. A differential signal from the selected read/write head is coupled via a cable to the input of a read preamplifier stage. The input of the read circuit is isolated from the write current source by isolating diodes. The output of the preamplifier is coupled through a balanced lowpass filter to a differentiator stage. The preamplifier signals at the output of the filter can be observed at test points labeled PREAMP + and PREAMP −. The differentiator stage transforms the read waveforms such that the data points are represented by zero crossing rather than the peaks produced at the head. The output of the differentiator can be viewed at test points labeled DIFF + DIFF −.

The output of the differentiator stage is connected to the input of a zero-crossing detector. The detector is a TTL bipolar one shot that produces pulses for positive or negative-going zero crossings. The output of the zero-crossing detector is connected to a droop detector. This circuit detects false zero crossing caused by droop in the differential output. The droop detector allows only valid output pulses from the zero crossing one-shot to pass through. The output of the detector can be viewed at a test point labeled READ DATA. An LED labeled C (read), also connected to the output of the droop detector, is dimly lit when the disc drive is in the read mode and there is data on the flexible disc.

The output of the droop detector is connected to the driver section of a data transceiver for transmission via differential lines to controller board A1.

Write Mode Operation

Information is written on the disc by passing a current through the windings of the read/write head. The current generates a flux field across the gap in the ferrite core, causing the iron oxide particles coated on the recording surface of the disc to be magnetized. The writing process orients the poles of each magnetized particle to permanently store the direction of the flux field as the oxide passes under the head. The direction of the flux is a function of the polarity of the write current. A data bit/clock pulse is written by reversing the write current through the head windings. This change in write current polarity switches the direction of the flux field across the gap. Erasing old data is accomplished by writing over any data which may have been previously written on the disc.

Write Current

The write circuit consists of a complementary write current source and an erase current source, both of which are enabled when the write mode is selected.

Data bits/clock pulses are input to drive PCA-A2 from controller PCA-A1. (Encoding is performed by circuits on A1.) The information is applied via the receiver section of the data transceiver to the clock input of a toggle flip-flop in the write current source. The flip-flop produces two complementary signals (Q and Q) that activate the write current source. The source consists of two transistor current amplifiers, one for each winding on the selected read/write head. The complementary outputs of the flip-flop alternately turn on each source. The switching action selects the head winding through which current will pass. A transistor switch in the write current source, controlled by the write interlock, supplies +12 Vdc to the source when conditions for the write mode of operation are valid.

A light-emitting diode labeled E (write), connected to the Q output of the toggle flip-flop, is dimly illuminated when the write mode is selected and the flip-flop is being toggled by signals from the receiver section of the data transceiver.

The erase current source consists of a single transistor that supplies dc current to the erase winding on the selected read/write head. Operation of the erase current source is controlled by the write interlock.

Power Supply Filtering

Drive board A2 is powered by dc voltages supplied by the host system via connector A2J5. The input voltages are +12 Vdc, +5 Vdc, and −12 Vdc. A −5 Vdc three-terminal negative regulator located on drive PCA-A2 and powered by the −12 Vdc input supplies a −5 Vdc regulated potential. The four voltages are filtered and then distributed throughout drive board A2. The disc drive spindle motor is powered by ac voltage obtained by cable directly from the host system.

Disc Structure

The flexible disc is a circle of plastic 200 mm (7.9 inches) in diameter, enclosed in a sealed black plastic jacket. Bonded onto the surface of the disc is a ferromagnetic iron oxide with characteristics similar to magnetic tape. Data is stored in the form of binary digits represented by magnetized spots on the disc. Information is stored and retrieved by read/write heads that come in contact with the disc's upper and lower surfaces.

Data is stored in concentric tracks on each side of the disc. Each disc has 77 circular tracks, numbered 0 thru 76. Each track is subdivided into either 30 sectors using HP format or 26 sectors using IBM format. Each sector contains either 256 bytes of data using HP format or 128 bytes using IBM format. The data contained in one sector is the smallest amount of information that can be written at a time. The disc is soft sectored, that is, there is no hardware indication of where each sector starts. Instead, the beginning of each sector is indicated by information recorded on the disc.

Drive Theory of Operation

Introduction

This section provides a general description of the drive module and will only cover those areas common to all versions.

General Description

The basic function of the drive is to indicate to the controller when it is ready to operate, and respond to the commands of the controller to:

- Receive and generate control signals,
- Position the read/write heads to selected tracks,
- Read or write data on the disc when selected.

Signals received and transmitted by the drive are shown in Table 2-3. Some signals received by the drive are gated with drive select so that no stepping, reading or writing can be performed on an unselected drive. Also, some signals generated within the drive are gated with drive select so that they can't be transmitted from an unselected drive.

Table 2-3. Control, Status and Data Lines Between the Controller and Drive Electronics

Signal	Mnemonic	Function
		Control Signals
Drive Select	DRV0-3	Identifies disc drive with which controller desires to communicate.
Head Load	HEADLOAD	Loads the heads and locks the door on the unit identified by Drive Select.
Head Select	HEADSEL	Selects head 1 when active, head 0 otherwise.
Low Current	LOWCURR	Reduces write current on inner tracks to decrease bit shift.
Move In	MOVEIN	Causes heads to move toward center of disc when active during a Step command. Heads move away from center when active during a Step command.
Step	STEP	Causes heads to move in direction specified by MOVEIN.
Write Enable	WRITDRV	Places disc drive in write mode when active.
		Status Signals
Disc Change	DISCHNG	Asserted when the elected drive is either not ready (due to no disc) or has a new disc inserted.
Disc Two-Sided	TWO-SIDE	Asserted when disc is found to be two-sided.
Index	INDEX	Asserted when index hole in disc passes photodetector.
Ready	READY	Asserted when a disc in the selected drive has rotated for at last two revolutions.

Track Zero	TRACK0	Asserted when heads are positioned at track zero.
Write Protect	WRPROT	Asserted when disc in selected drive is write protected.
		Data Lines
Read Data	RDATA	Carries read data to the controller from the drive.
Write Data	WDATA	Carries write data to the drive from the controller.

During the write operation, the selected drive must have head-load, head select, write enable and write data signals. During the read operation, the selected drive will perform a head load. The write enable line remaining high implies a read operation. Under these conditions the drive will transfer read data to the controller. Controller step and direction commands are received initiating a track-seek operation on a selected drive. The selected drive transmits a track 00 signal to the controller whenever the read/write heads are at track 00.

Positioning the carriage-mounted read/write heads is accomplished by a band-driven stepper motor. Each step command from the user system increments the stepper motor which, in turn, moves the band. The band increments the read/write heads one track for each step command.

A read or write operation begins by placing the read/write heads in contact with the disc with a Head-Load command at the desired track. To write on the disc, write enable is sent by the controller to condition the write logic. The write current then in the head reverses polarity synchronous with the high-to-low transitions of the write-data pulses from the controller. The current reversals cause magnetic flux reversals on the desired disc track. Erasure of previously recorded data is simultaneously accomplished during the writing operation in addition to a delayed tunnel erase which ensures disc interchangeability.

To read from the disc, magnetized bits in the format of the pre-recorded data are sensed by the read/write heads. This signal is amplified, digitized and transmitted to the controller.

Functional Characteristics and Communication Protocol

Introduction

This section describes the recording formats used in HP disc memory.

Recording Formats

The HP disc drive supports both the HP Standard Disc Format (hereafter referred to as the HP Format) and the IBM (IBM 3740) Standard Data Interchange Format (hereafter referred to as the IBM Format). Format similarities and differences are described in the following paragraphs.

Format Similarities

The following features are common to both the IBM Format and the HP Format.

Media. A double-sided disc is used as the recording medium. The disc is composed of recording material and is enclosed in a square plastic jacket. An index hole in the disc is used to provide a rotational position reference. The disc drive will also accept a single-sided disc. Single-sided discs must be used for the IBM Format mode of operation.

Tracks. There are 77 physical tracks on each side of the disc, with a spacing of 0.0208 inch between track centers (48 tracks per inch). The outermost track is Track 0 and the innermost track is Track 76.

Recording. Information is stored on the disc as a series of magnetic flux reversals. Since a single head is used to read from and write on each side of the disc, a self-clocking code must be used to store the information.

The portion of the disc or the duration of the time used to store a single bit is referred to as a bit cell. The first part of the bit cell is called the clock window and the remainder of the bit cell is called the data window. A flux reversal in the clock window is called a clock transition and a flux reversal in the data window is called a data transition. A bit cell that contains a data transition stores a 1 and a bit cell with no data transition stores a 0.

Track Format. Each track is divided into sectors, as shown in Figure 2-3. The data contained in one sector is the smallest amount of information that can be written at a time. The disc is soft-sectored, that is, there is no hardware indication of where each sector starts. Instead, the beginning of each sector is indicated by information recorded on the disc.

In order to allow soft-sectoring, each sector is divided into two fields. First, there is an ID field which contains information to identify the sector. Next, there is a data field which contains the actual data. The ID field is written only when the disc is formatted, never during actual operation. Thus, an ID field serves as a fixed marker for the beginning of each sector. The entire data field is re-written each time a write operation occurs to the sector.

The makeup of the ID and data fields is similar. Both fields start with a series of sync-up bytes. These bytes end with a long string of identical bits. During a read, the bit string allows the controller's decoder circuitry time to synchronize itself with the data on the disc. Next comes an address mark byte, which indicates that the beginning of an ID or data field has been found. The data stored in this byte indicates which type of field it is part of. In order that no other byte can be mistaken for an address mark, the address mark byte contains an abnormal pattern of clock transitions. The first bit of an address mark is opposite type from the last bit of a sync-up field. This feature simplifies detection of address marks.

Following the address marks is a series of information bytes. In an ID field, these bytes indicate the logical track, head and sector address. In a data field, these bytes are the data being stored in the sector.

At the end of each field are two Cyclic Redundancy Check (CRC) bytes. These bytes allow the detection of most errors that occur in the storage and recovery of information from the disc.

There are gaps between each field on the track. The gaps allow for variations in disc rotational speed. The sectors are logically numbered consecutively. However, the sectors may occur in any physical order around the track. This allows the sectors to be staggered to optimize system performance.

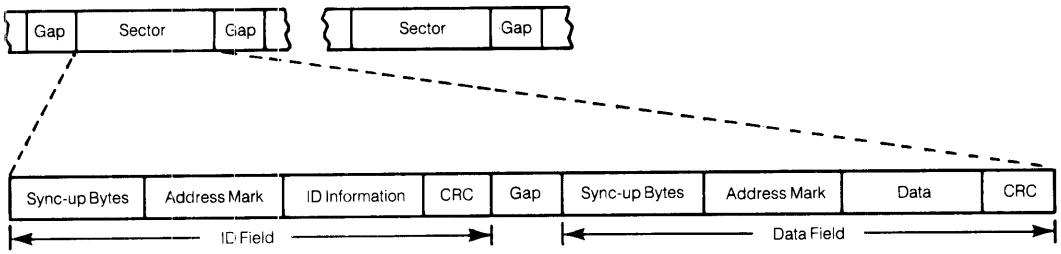


Figure 2-4. Track Format

Track Numbering. Each track has a physical address as previously described. There is also a logical track address associated with each good track. The logical track address is written in the ID field of each sector on the track. If a disc has no bad tracks, the logical address of a track is the same as the physical address.

A disc with N bad tracks can be made to look like a 77 — N track disc with no bad tracks. To do this, the logical track address stored in the ID field of each sector of every bad track is set to !FF. Tracks of this type are known as invisible tracks. All visible tracks are then sequentially assigned logic track numbers. Logical Track 0 is the outermost good track, not necessarily physical Track 0.

Format Differences

Table 2-4 summarizes the principal differences between the IBM Format and the HP Format. Details of these differences are provided in the following paragraphs.

Coding. The IBM Format uses a single-density encoding scheme known as frequency modulation (FM). The rules for FM coding are as follows:

- A 0 bit cell has no data transition.
- A 1 bit cell has a data transition.
- Every bit cell has a clock transition.

The minimum, distance between transitions is one-half bit cell, that is, the distance from a clock transition to a data transition.

Table 2-4. Format Differences

Feature	HP Format	IBM Format
Usable Physical Tracks	0 — 76	0 — 76
Sectors Per Track	30	26
Sector Numbering	0 — 29	1 — 26
Bytes Per Sector	256	128
Data Order	LS Byte First LS Bit First	MS Byte First MS Bit First
Coding	MMFM	FM
Precompensation Required	Yes	No
Sync-UP Bytes	Four Bytes of !00 And Four Bytes of !FF	Six Bytes of !00
Address Marks	Extra Clock Transitions	Missing Clock Transitions
CRC Includes Address Mark	No	Yes

The HP Format uses a double-density encoding scheme known as Modified Modified Frequency Modulation (MMFM). The rules for MMFM coding are as follows:

- A 0 bit cell has no data transition.
- A 1 bit cell has a data transition.
- A 0 bit cell has a clock transition if there is no transition in the preceding bit cell.
- A 1 bit cell never has a clock transition.

For the same recording density (flux transitions per inch), there are twice as many data transitions in MMFM coding as in FM coding.

Precompensation. Transitions which are written close together tend to appear shifted apart when they are read back. This effect is known as bit shift. Due to its large bit cell, the IBM Format is not affected by bit shift. However, because of the smaller bit cell used in the HP Format, bit shift is noticeable. To compensate for bit shift, certain MMFM transitions are written closer together. This action is called precompensation. The actual precompensation used on a transition is dependent upon the pattern being recorded.

Address Marks. There are four types of HP address marks. All are unique in that they include a bit cell with an extra clock transition. The HP address mark byte is not included in CRC generation. Address mark is abbreviated AM.

Name	Data Pattern	Clock Pattern	Where Found
ID AM	!70	!0E	ID Field
Defective Track AM	!F0	!0E	ID Field
Data AM	!50	!0E	Data Field
ECC Data AM	!D0	!0E	Data Field

At the command set level, a clear d bit indicates an ID AM in the ID field, and a set D bit indicates a defective track AM in the ID field.

There are four types of IBM Format address marks. All are unique in that they include bit cells which contain no clock transition. The IBM address mark byte is included in CRC generation.

Name	Data Pattern	Clock Pattern	Where Found
Index AM	!FC	!D7	At Index Hole
ID AM	!FE	!C7	ID Field
Data AM	!FB	!C7	Data Field
Deleted Data AM	!F8	!C7	Data Field

At the command set level, a clear D bit indicates a data AM in data field and a set D bit indicates a deleted data AM in the data field.

Presently, all data fields contain a data AM. If error correcting code (ECC) bytes added to the data field in the future, an ECC data AM will be used, allowing interchange between ECC and non-ECC systems.

Track Format. Detailed track formats for the HP format and IBM Format are shown in Figures 2-5 and 2-6, respectively.

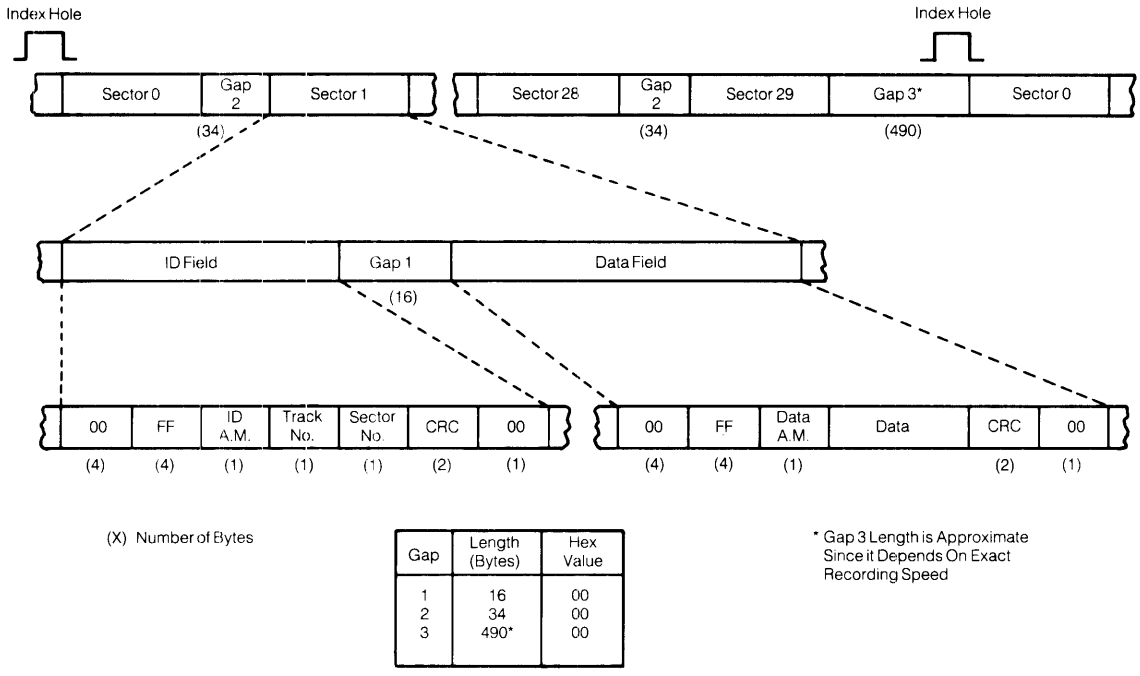
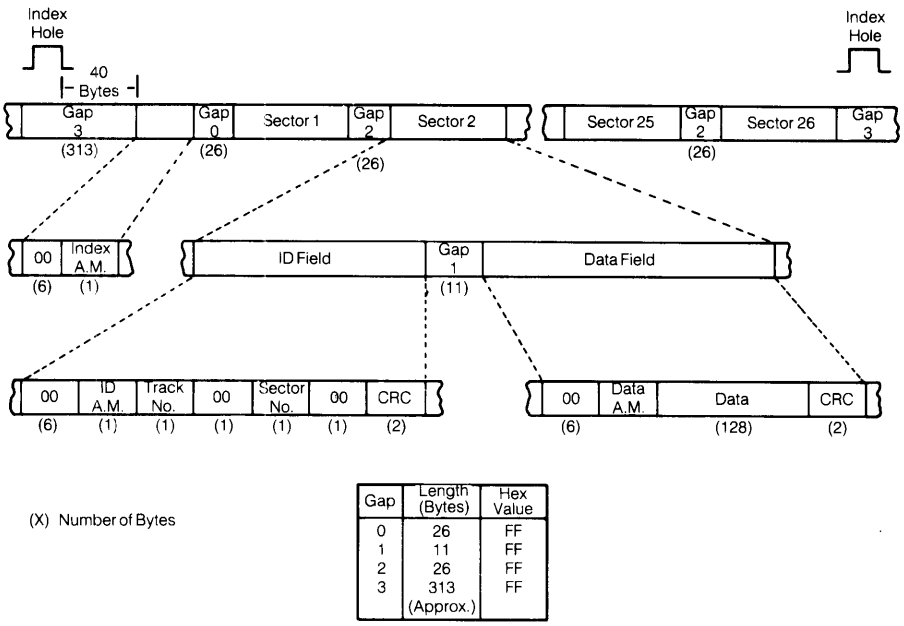


Figure 2-5. Hewlett-Packard Standard Sector Recording Format



Gap	Length (Bytes)	Hex Value
0	26	FF
1	11	FF
2	26	FF
3	313 (Approx.)	FF

Figure 2-6. IBM Standard Sector Recording Format

Interface Information
7902A Flexible Disc Drive (P/N 45000-67914)

Introduction

This section provides information required to interface the HP 7902A Disc Drive with a host system. Included are power requirements, cabling data, switch settings, environmental limitations, and design details for a front panel display.

Power Requirements

Drive Board-A2

+5V 0.6A typical, 0.7A max, voltage tolerance: +5%, −3%
+12V 0.8A typical, 1.0A max, voltage tolerance: ±5%
−12V 0.8A typical, 1.0A max, voltage tolerance: ±5%

Disc Drive Assembly

86 — 127 Vac at 0.3A typical, 0.44A max
50/60 Hz ±3.5% HP Format
50/60 Hz ±1% IBM Format

Power Sequencing

Power On signal PON should stay low until well after all dc supply voltages have stabilized (greater than 100 milliseconds). Signal PON should go low immediately if ac power is not within specifications, or if dc power is about to fail.

System Reset (SYSRST) is a logic level, active low, signal which performs the same function as PON for the controller. It forces the system to First Status state.

AC power must be within specification for at least two seconds before reading and/or writing. This is to allow the spindle rotational speed to stabilize.

Cooling Requirements

The operating limits of the disc drive assembly and medium are specified as 10°C to 40°C, 20 to 80 percent relative humidity (RH) with maximum wet-bulb temperature of 25.5°C. these limits allow for a rise in the disc drive of 10°C. The actual operating limits are set by the medium. IBM sets the limits at 10°C to 52.6°C, 8 to 80 percent RH, maximum wet-bulb temperature of 29.4°C.

Shieldng Requirements

No shielding is required under normal operating conditions. If the disc drive assembly is subjected to medium -- to high-intensity electromagnetic fields such as those from the yoke of a cathode-ray tube, an aluminum or steel shield should be placed between the source of the field and the disc drive. The head load solenoid has a small dc external field that may cause CRT deflection. A shield wrapped around the disc drive assembly will eliminate this source of interference.

Hardware Interface

The following information describes the drive board connector pin outs and signal lines. This information is the same for drive boards designed and manufactured by HP.

Figure 2-7 shows the location of the connectors on the HP drive circuit boards A2. Connection to the controller is through the 50 pin connector A2J7. DC power is supplied via A2J4. Table 2-5 lists the pin assignments for connectors A2J7, A2J8, A2J4 and A2J3. Connections for a drive display panel are provided by connector A2J2. A2J8 is used for daisy chainging drives.

AC power for the disc drive assembly is connected directly to a 3-pin connector, located on the drive, between the actuator and the spindle motor capacitor. See Figure 2-8. Pin assignments for the connector are as follows:

Pin	Signal
1	ac line
2	frame ground
3	ac neutral

Mating parts for the connector are:

Body, part no. 1251-3913 (Amp 1-480700-0)

Pin, part no. 1251-3915 (Amp 350547-1)

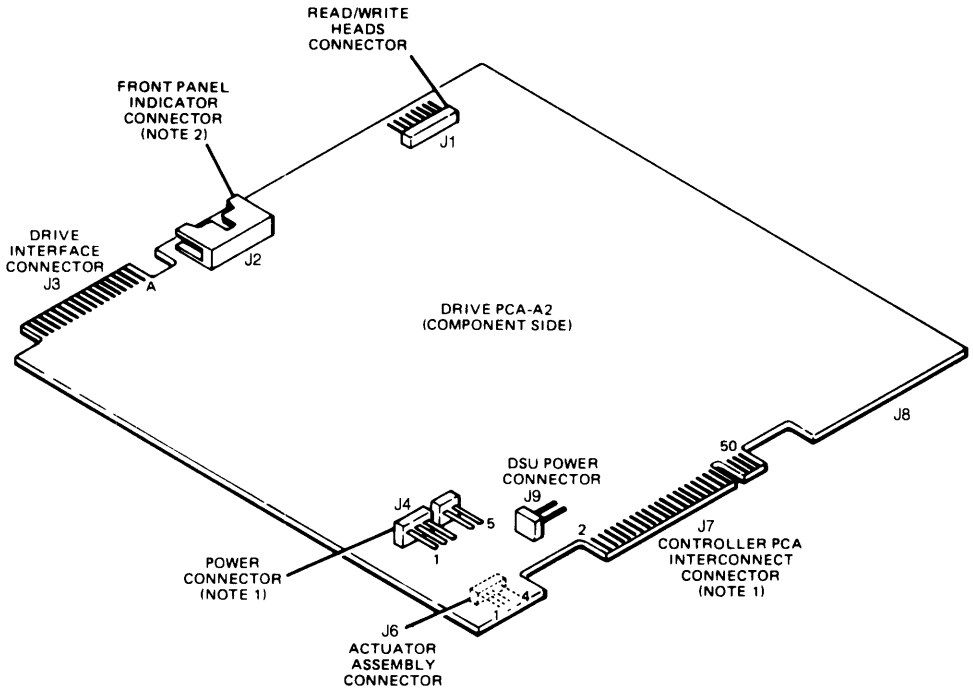


Figure 2-7. HP Drive Board A2 Connectors

Table 2-5. 7902A Drive Board A2 Connector Pin Assignments

A2J7/A2J8 (See Notes 1 and 3)

Pin	Signal	Pin	Signal
1	GND	2	DSL0H
3	GND	4	DSL1H
5	GND	6	DSL2H
7	GND	8	DSLVL
9	GND	10	LDCTL
11	GND	12	STENL
13	GND	14	DRSPNH
15	GND	16	WRITL
17	GND	18	PHIBH
19	GND	20	PHIAH
21	GND	22	DLCKL
23	GND	24	HED1H
25	GND	26	PORH
27	GND	28	INDXL
29	GND	30	SPINL
31	GND	32	TRK0L
33	GND	34	WPRTL
35	GND	36	REDYH
37	GND	38	DATAH
39	GND	40	DATAL

41	KEY	44	KEY
45	GND	46	NC
47	GND	48	PONH
49	GND	50	−5V TP

A2J4 (See Note 2)

Pin	Signal
1	GND
2	GND
3	+12V
4	KEY
5	−12V
6	+5V

A2J3

Pin	Signal
1	Enabled
2	Disc Spinning
3	Ready
4	Write Protected
5	Sel 2
6	In Use
7	Sel 0
8	Sel 1
9	GND
10	+5V

Notes:

1. Odd-numbered pins are on circuit side of the board, even-numbered pins are on component side.
2. A2J4 mating connector: part no. 1251-3275 (Molex 09-50-7061)
   A2J4 connector contacts: part no. 1251-0670 (Molex 08-50-0105)
   A2J4 connector key: part no. 1251-0627 (Molex 15-04-0219)
3. Refer to table for definitions of the signal mnemonics.

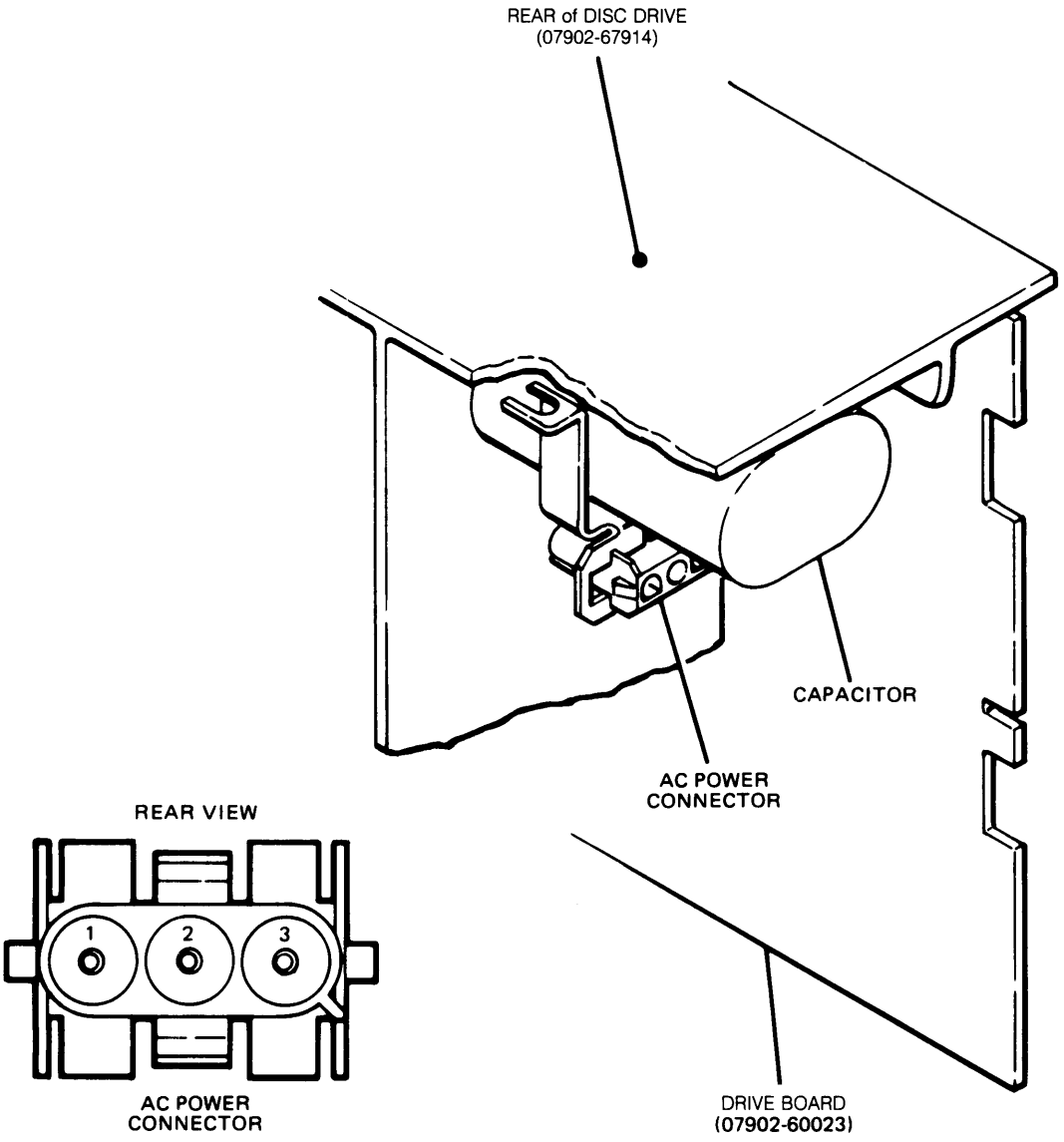
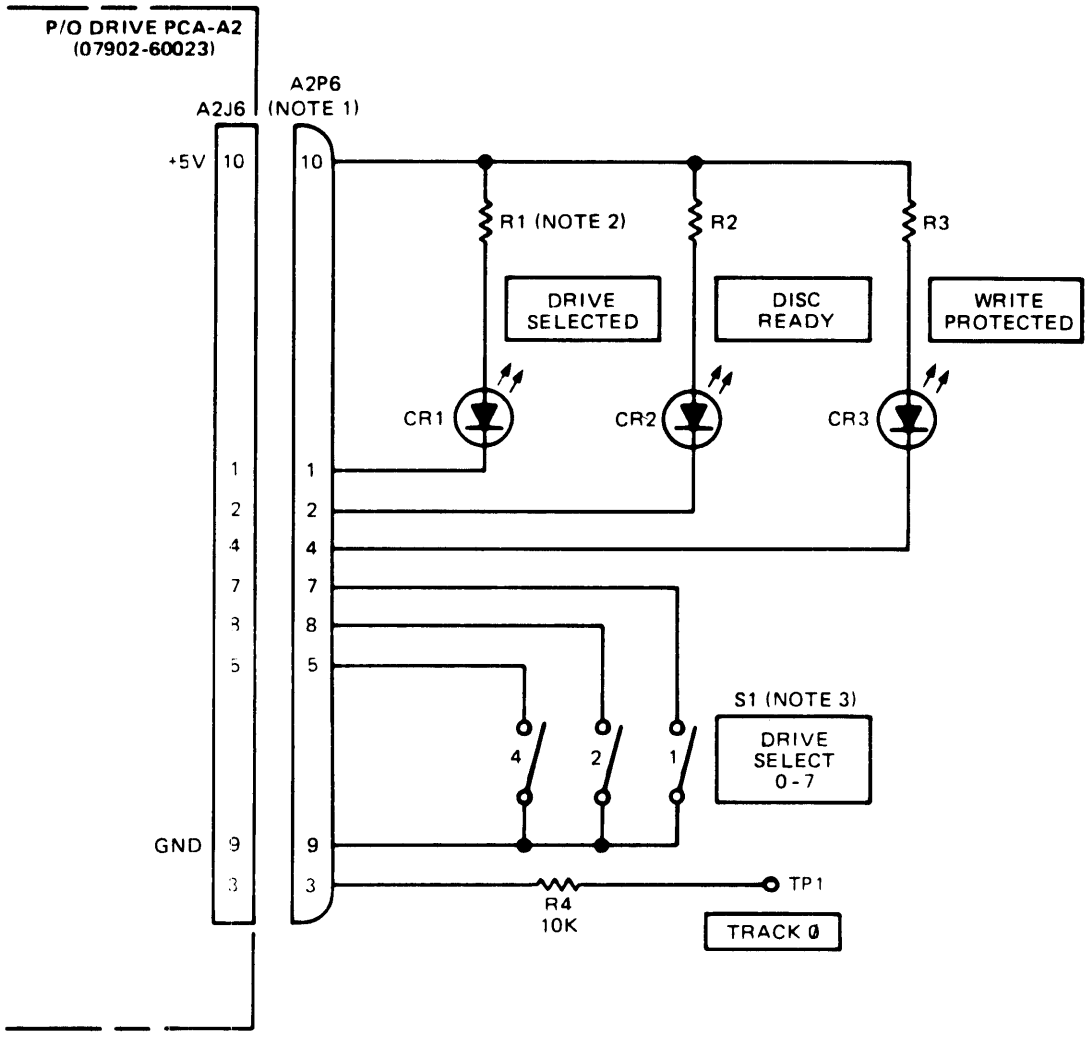


Figure 2-8. AC Power Connectors

Front Panel Indicator Display

Connector A2J2 on drive board (see Figure 2-7) is available for displaying disc drive status and for disc drive number selection. A typical design for a front panel indicator display employing the data available at A2J2 is shown in Figure 2-9. If no DRIVE SELECT switch is connected to A2J2, drive select will default to number 0. The LED status indicators shown in the design are driven by low-power Schottky buffers (active low). The LED current should be limited to 20 milliamperes or less.



NOTES: 1. A2P6 IS A 10-PIN RIBBON CONNECTOR, HP PART NO. 1251-4006 (3M, PART NO. 3473-0000).

2. LED'S CR1 THROUGH CR3 ARE DRIVEN BY LOW-POWER SCHOTTKY BUFFERS (ACTIVE LOW). LIMIT LED CURRENT TO 20 mA OR LESS.

3. S1 IS A BINARY ENCODED 1 OF 8 SWITCH, LOW TRUE. A TYPICAL PC MOUNT THUMBWHEEL SWITCH IS HP PART NO. 3100-3395 (EECO, PART NO. 1A-21-50-61G).

Figure 2-9. Typical Front Panel Indicator Display

Maintenance

Introduction

This section contains a listing of the standard and special tools and test equipment required to service the 07902-67914 disc drive, the preventive maintenance schedule, and all required preventive maintenance inspection and cleaning procedures.

WARNING

- TO AVOID PERSONNEL INJURY AND/OR DAMAGE TO EQUIPMENT, OBSERVE ALL WARNINGS AND CAUTIONS STATED IN THIS PUBLICATION AND AS DETAILED BELOW.
- USE EXTREME CAUTION WHEN WORKING ON THE DISC DRIVE WITH POWER APPLIED. HAZARDOUS VOLTAGES ARE PRESENT INSIDE THE DISC DRIVE WHENEVER IT IS CONNECTED TO AN ACTIVE AC POWER SOURCE.
- DO NOT ATTEMPT TO REMOVE OR CHANGE PRINTED CIRCUIT ASSEMBLIES (PAC'S) OR INTERCONNECTING CABLES WITHOUT FIRST REMOVING POWER FROM THE DISC DRIVE.

CAUTION

- NEVER ATTEMPT TO SWING OPEN THE CARTRIDGE GUIDE ASSEMBLY WITHOUT FIRST UNLOADING THE HEADS FROM THE HEAD LOAD BAIL.
- NEVER ALLOW THE HEADS TO TOUCH EACH OTHER. WHENEVER THE HEADS ARE UNLOADED FROM THE HEAD LOAD BAIL, PLACE A PIECE OF CLEAN LENS TISSUE BETWEEN THE HEADS TO PREVENT THEM FROM TOUCHING.
- ENSURE THAT THE HEAD LOAD ACTUATOR UP STOP ADJUSTMENT IS PROPERLY SET. THIS ENSURES THAT THE FLEXIBLE DISC WILL CLEAR THE HEADS WHEN IT IS LOADED INTO THE DISC DRIVE.
- ENSURE THAT THE DOOR LOCK ASSEMBLY IS FUNCTIONING PROPERLY. THIS ENSURES THAT THE FLEXIBLE DISC CANNOT BE REMOVED FROM THE DISC DRIVE WHILE THE HEADS ARE LOADED.
- THE READ/WRITE HEADS ARE FACTORY ALIGNED WITH A FOUR-TRACK OFFSET BETWEEN THE HEADS. LOOSENING THE HEAD-MOUNTING SCREW WILL DESTROY THIS OFFSET AND NECESSITATE THE RETURN OF THE DISC DRIVE FOR REALIGNMENT.
- DO NOT LUBRICATE THE DISC DRIVE — OIL WILL CAUSE DUST AND DIRT TO ACCUMULATE.
- DO NOT TOUCH THE HEADS OR ATTEMPT TO CLEAN THEM.

Service Tools and Test Equipment

The following paragraphs list those standard and special tools and test equipment required to service the disc drive.

Standard Tools

Table 2-6 lists the standard tools required to service the disc drive. Equivalent tools may be used, when necessary.

Table 2-6. List of Standard Service Tools

Tool	HP Part No.
Extractor, Pin (or paper clip)	—
Nutdriver, ¼-inch socket	8720-0002
Nutdriver, 11/32-inch socket	8720-0004
Pliers, Diagonal Cutting	8710-0006
Pliers, Long Nose	8710-0016
Screwdriver, slot drive, 4 x ¼-inch	8720-0001
Screwdriver, slot drive, 3 x 3/16-inch	8730-0019
Screwdriver, Pozidriv, 4-inch	8710-0900
Screwdriver, Pozidriv, 3-inch	8710-0899
Soldering Iron	8690-0011
Soldering Iron Tip	8690-0021
Wrench Set, Hex Key	8720-0019

Standard Test Equipment

An oscilloscope (HP 1707B Oscilloscope or equivalent) is the only piece of standard test equipment required to service the disc drive. The oscilloscope is used primarily to check the alignment of various components in the disc drive and for troubleshooting.

NOTE

All oscilloscope sensitivity settings specified in the procedures given in this section assume the use of 10:1 oscilloscope probes. If 1:1 probes are ued, the sensitivity settings should be scaled accordingly.

Special Tools

Table 2-7 lists the special tools required to service the disc drive. Substitutions must not be made.

Table 2-7. List of Special Service Tools

Tool	HP Part No.
Alignment Flexible Disc	9164-0111
Cartridge Guide Adjustment Tool	1150-1310
Bail Adjustment Tool	1535-3875
Disc Service Unit	12748-60008

Special Test Equipment

Disc Service Unit. the Disc Service Unit (DSU), part no. 12748-60008 is the only item of special test equipment required to service the disc drive. It is used for on-site preventive maintenance, alignment, adjustment, and troubleshooting of the disc drive.

The DSU provides the means to simulate drive board. A1 signals to the disc drive and process disc drive responses. Simulated signals are produced either manually or automatically to operate the disc drive. Modes of operation include seek to track, alternate seek, single step, and writes. A numerical keypad and 3-digit numerical display permits selection of test parameters including drive number, alternate seek minimum and maximum track addresses, seek to track address, and track-to-track seek time. Self-test circuitry contained in the DSU is activated at power turn-on and provides a visual indication of the DSU serviceability.

DSU Installation. To install the DSU, proceed as follows:

1. Remove power from the disc drive.
2. Disconnect the cable from connector J7 on drive board A2.
3. Connect the ribbon cable connector on the DSU cable to J7 on drive board A2.
4. Connect the 3-pin connector on the DSU cable to J9 of the drive board A2. Ensure that the connector is correctly oriented. The slots in the connector should be facing upward, away from the component side of the drive board A2.

CAUTION

ENSURE THAT THE DISC DRIVE DOES NOT CONTAIN A FLEXIBLE DISC AT POWER TURN-ON. FAILURE TO OBSERVE THIS PRECAUTION MAY RESULT IN ACCIDENTAL ERASURE OF DATA FROM A NONWRITE-PROTECTED DISC.

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5. Restore power to the disc drive.

DSU Operating Instructions

Figure 2-10 identifies the DSU front panel controls and indicators and Table 2-8 defines the functions of these components. An abbreviated instruction set for the DSU is given in Table 2-9 and additional operating instructions are provided in the following paragraphs.

Power Turn-on. At DSU power turn-on, the DSU performs a self-test. If the self-test passes, all DSU LED's, with the exception of those controlled by the disc drive (INDEX, RD/WR DATA, DRIVE READY, TRACK 0, and WRITE PROTECTED), are lit for 5 seconds. The disc drive is now recalibrated and initialized and the DSU is reset. Reset conditions for DSU include SELECT HD 1, LOCK DOOR, and HEAD LOAD pushbuttons is a non-asserting state; no WRITE condition selected, STOP LED lit; DRIVE NUMBER — 7; MAX TRACK — 76; MIN TRACK — 0; STEP RATE — 3; and keypad display — 0.

NOTE

Self-test may not occur at power turn-on if application of dc voltage is slow. In this event press the SYSTEM RESET pushbutton to initiate self-test.

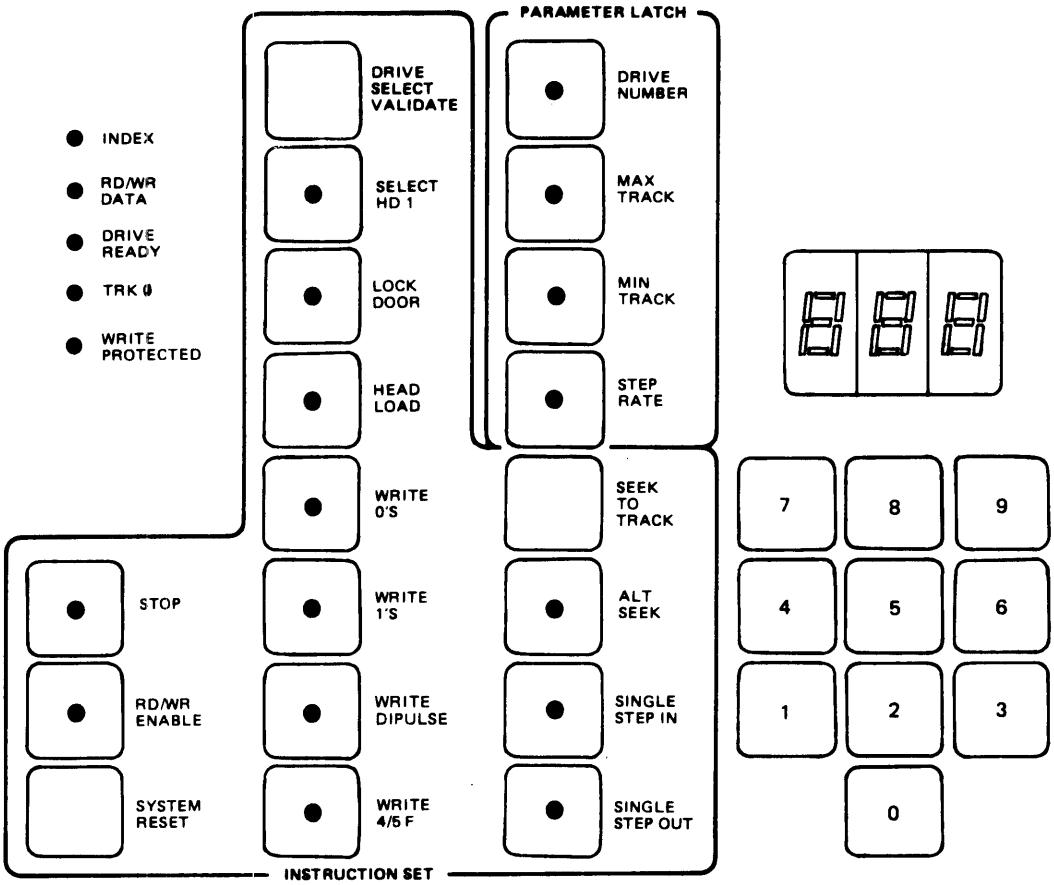


Figure 2-10. Disc Service Unit Front Panel Controls and Indicators

Table 2-8. Disc Service Unit Controls and Indicators

DECIMAL KEYPAD	Programs value for drive number, maximum and minimum tracks (alternate seek), step rate, and seek to track parameters. Each time a key is pressed, that number is entered into least significant digit of 3-digit decimal display and other numbers shift up. The programmed number is entered when appropriate parameter pushbutton is pressed. At power turn-on and reset, 3-digit readout is reset to 0.
	Parameter Latch Pushbuttons
DRIVE NUMBER	Enters keypad number selected for drive number. Pushbutton indicator flashes if number is greater than 7. Selection of a new number automatically recalibrates drive.
MAX TRACK	Enters keyboard number selected for alternate seek maximum track number. Pushbutton indicator flashes if number is less than current alternate seek minimum track number. At power turn-on and reset, number is automatically set to 76.
MIN TRACK	Enters keypad number selected for alternate seek minimum track number. Pushbutton indicator flashes if number is more than current alternate seek maximum track number. At power turn-on and reset, number is automatically set to 0.
STEP RATE	Enters keypad number in milliseconds selected for track-to-track seek time. Pushbutton indicator flashes if number is less than 3. At power turn-on and at reset, number is automatically set to 3.
	Instruction Set Pushbuttons
SEEK to TRACK	Disc drive seeks to track number selected by keypad. If number selected is greater than 76, disc drive seeks to track 76. At power turn-on and reset, track 0 is automatically selected (Keypad is reset to 0.)
ALT SEEK	Disc drive seeks between keypad selected minimum and maximum track numbers. Pushbutton indicator is lit during seek operation. At power turn-on and reset, alternate seek is automatically set to occur between tracks 0 and 76.
SINGLE STEP IN	Head assembly steps inward one track. Pushbutton indicator flashes if heads are at outermost track (0).
STOP	Stops DSU continuous operations (alternate seek, continuous write) and error signals. Pushbutton indicator lights when DSU is waiting for a command.
RD/WR ENABLE	Resets disc drive status signal (Spinning). Pushbutton must be pressed at power turn-on or when a disc is removed during a test before DSU operation can continue. Pushbutton indicator lights when Spinning signal is in asserted state.

SYSTEM RESET	Reset entire system and disc drive. DSU self-test is initiated and disc drive is recalibrated and initialized.
WRITE 0's	Writes 0's (250 kHz) on disc. Pushbutton indicator lights when write 0's is selected.
WRITE 1's	Writes 1's (500 kHz) on disc. DSU pushbutton indicator lights when Write 1's is selected.
WRITE DIPULSE	Writes dipulses on disc. Pushbutton indicator lights when write dipulses is selected.
WRITE 4/5 F	Writes at 200 kHz on disc. Pushbutton indicator lights when write 4/5 F is selected.

NOTE

If a WRITE pushbutton is pressed and released in less than 1.5 seconds, write lasts for one revolution of the disc; longer than 1.5 seconds produces a continuous write.

DRIVE SELECT VALIDATE	Validates drive number. Pushbutton indicator is lit when drive number is validated.
SELECT HD1	Selects head. When pushbutton indicator is lit, head 1 is selected; when indicator is off, head 0 is selected. At DSU power turn-on and reset, head 0 is selected.
HEAD LOAD	Loads the heads. Heads are loaded when pushbutton indicator is lit. At DSU power turn-on and reset, heads are unloaded. Pushbutton must be pressed before a seek to track, alternate seek, or single step in/out operation can be initiated, assuming drive is selected.
	LED's
INDEX	Lights each time index hole in disc passes disc drive index sensor. LED operation is gated by disc drive selected (SELECT DRIVE number entered and DRIVE SELECT VALIDATE pressed).
RD/WR DATA	Lights when DSU is writing or reading from a disc.
DRIVE READY	Lights when disc drive is ready to be exercised. It also lights when disc drive is not selected.
TRK 0	Lights when heads are at outermost track. LED operation is gated by disc drive selected.
WRITE PROTECTED	Lights when a write protected disc is in disc drive. Write operations are inhibited. LED operation is gated by disc drive selected.
	Test Points
INDEX	Output of disc drive index sensor. Signal is active high.
RD/WR DATA	Disc drive data signal.

HEAD LOAD	Disc drive head load signal. Signal is low when heads are loaded.
+5V	+5 Vdc supplied to DSU.
GND	+5 Vdc ground.

Drive Select. To select a drive, enter the desired drive number on the keypad display and then press the following pushbuttons: DRIVE NUMBER, DRIVE SELECT VALIDATE, RD/WR ENABLE, and HEAD LOAD.

Exercising Drive. The heads must loaded before a seek to track, alternate seek, single step in/out, or write operation can be performed. The heads are loaded when the HEAD LOAD pushbutton indicator is lit.

Alternate Seek. AT DSU power turn-on, the DSU is automatically set to perform alternate seeks between tracks 0 and 76 when the ALT SEEK pushbutton is pressed. To change the track limits requires the use of the MAX TRACK and MIN TRACK pushbuttons as described in Table 2-8. Alternate seek is halted with the STOP pushbutton.

Table 2-9. Disc Service Unit Instruction Set

DSU INSTRUCTION SET

Connect DSU to disc drive and apply power. Insert flexible disc, close door, select drive number, press DRIVE NUMBER, DRIVE SELECT VALIDATE, RD/WR ENABLE, and HEAD LOAD.

I. OPERATING MODES

MODE	DESCRIPTION
System Reset	First a DSU self-test is performed. If self-test passes, DSU is reset and disc drive is recalibrated and initialized. DSU reset includes HEAD LOAD, LOCK DOOR and SELECT HD 1 inactive; MIN TRACK = 7; and Keypad = 0.
	Ifself-test fails, 3-digit readout indicates "Bad", and Keypad is disabled.
Seek to Track	Carriage steps to selected track address and stops.
Single Step In/Out	Operator may single step carriage inward one track or outward one track.
Alternate Seek	Carriage steps from one selected extreme track address to other selected extreme track address.
Write	0's or 1's (250 kHz or 500 kHz) can be written on a scratch flexible disc to check write circuits. Dipulse and 4/5 F (200 kHz) writing is also possible.

II. OPERATING FEATURES

FEATURES	DESCRIPTION
Decimal Keypad	Programs values for drive number, seek to track, min. and max. tracks (alternate seek) and step rate parameters. At DSU power turn-on and system reset, readout is reset to 0.
Drive Select	Selects drive number (0 — 7).
INDEX LED	Lights each time index hole in disc passes disc drive index sensor.
INDEX TP	Monitors output of disc drive index sensor. Signal is active high.
RD/WR DATA LED	Lights when DSU is writing on or reading from a disc.
RD/WR DATA TP	Monitors disc drive read/write signal.
TRK 0 LED	Lights when heads are at outermost track.
WRITE PROTECTED LED	Lights when a write protected disc is in disc drive.
DRIVE READY LED	Lights when disc drive is ready to be exercised.
HEAD LOAD TP	Active low when heads are loaded.

PROCEDURE

a. Press SYSTEM RESET. Note: System reset also occurs at DSU power-on.

a. Select desired track-to-track step rate on Keypad and press STEP RATE.
b. Select desired track number on Keypad.
c. Press SEEK TO TRACK.

a. Press SINGLE STEP OUT or SINGLE STEP IN, as desired.

a. Select desired minimum track number on Keypad and press MIN TRACK.
b. Select desired maximum track number on Keypad and press MAX TRACK.
c. Select desired track-to-track step rate on Keypad and press STEP RATE.
d. Press ALT SEEK.
e. Press STOP to stop alternate seek.

a. Seek to desired track.
b. Select desired head with SELECT HD 1 bushbutton.
c. Press desired WRITE pushbutton. Note: If a WRITE pushbutton is pressed and released in less than 1.5 seconds produces a continuous write.
d. Press STOP to stop continuous write.

PROCEDURE

a. Set desired number on 3-digit display.
b. Press appropriate PARAMETER pushbutton to enter number into DSU.

a. Select desired drive number on Keypad.
b. Press DRIVE NUMBER.
c. Press DRIVE SELECT VALIDATE.

None

None

None

None

None

None

None

None

Preventive Maintenance Schedule

The disc drive is designed for a minimum of preventive maintenance. A schedule for periodic inspection of the disc drive is provided in Table 2-10. It is recommended that the procedures listed in the schedule be performed at 12-month intervals. Also, the head radial alignment check must be performed when the disc drive is integrated into the host system and at installation of the host system. The general operation of the disc drive should be verified before regular scheduled maintenance is performed and again after it has been completed. Run the appropriate diagnostic tests in accordance with the instructions provided in the host system diagnostic manual.

Table 2-10. Preventive Maintenance Schedule

ITEM	ROUTINE
Actuator Assembly	Remove all oil, dust, and dirt. Do not clean unless absolutely necessary.
Belt	Check for frayed or weakened areas. Replace if necessary.
Base	Remove all dust and dirt. Check for loose screws, connectors, and switches.
Read/Write Heads	Check for proper azimuth and radial alignment. **CAUTION** Do not touch or attempt to clean the heads.

Head Azimuth and Alignment Checks

The following paragraphs contain instructions for testing head azimuth and radial alignment. Since the heads are not field replaceable, failure to meet any one or more of the specifications listed for these tests will necessitate replacement of the disc drive assembly.

Head Azimuth Test

An aximuth test on the heads of the 7902A is now available with the use of the new alignment disc, 9164-0111. This test checks the offset of each head from the perpendicular to the tangent of the track. It should be performed any time read errors occur or when there is incompatibility between discs and drives.

To perform this test requires alignment disc P/N 9164-0111. There is a unique pattern on track 76 to measure the amount of angular offset of the head gap to the track. An offset deviation of + or − 18 minutes allowable. The following procedures check that the drive is within these limits.

a. Set the oscilloscope controls as follows:

   Sweep: .5 msec/div
   Sensitivity: .1 volts/div
   Input: DC
   Display: A + B, B inverted
   Trigger: Normal, external, +

b. connect the A-channel probe to TP Diff + B-Channel probe to TP Diff − and the EXT TRIG probe to TP INDEX.

c. Insert the Alignment Disc into the drive to be aligned, and close the drive door.

d. With the DSU, select the drive to be aligned, seek to track 76, and select head 0 and do a continuous read.

NOTE

The disc drive unit under test must be in its normal operating position, i.e., horizontal or vertical. Failure to properly position the drive will result in errors in the azimuth measurement.

---

e. Follow the flowchart below. Reject the disc drive or continue to step f as directed by the flowchart.

f. Repeat steps d and e for HEAD 1.

Head Radial Alignment Check

The head radial alignment is factory set and adjustment is not normally required. To check head radial alignment, proceed as follows:

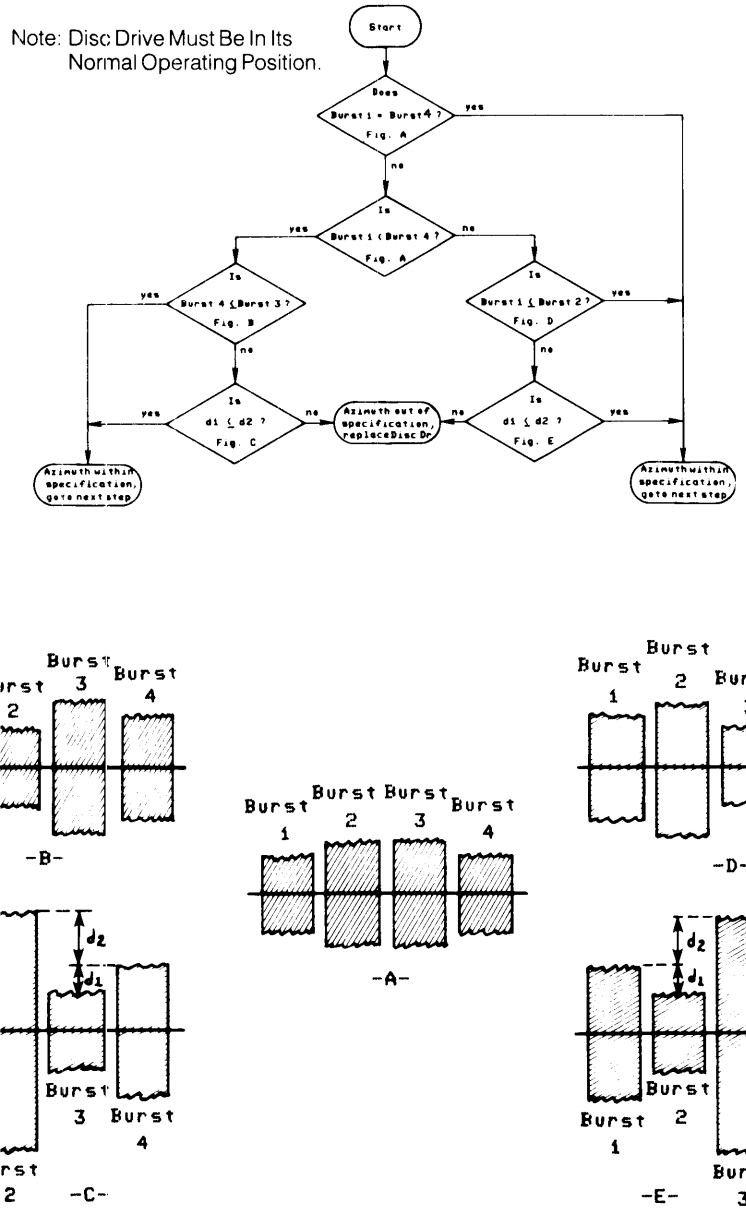


Figure 2-11. Azimuth Test Waveforms

NOTE

Due to variations in disc size with temperature and humidity, approximately 20 minutes should be allowed for the Alignment Disc to stablize at the ambient room conditions. For best results, the disc should be removed from the PSP as soon as you arrive at the test site. This lets the disc acclimate as fast as possible. The longer you can wait, the more accurate the test results.

---

a. Insert alignment disc, part no. 9164-0111 into the disc drive.

b. Step to track 38, select head 0 and do a continuous read.

c. Using 10:1 probes, connect an oscilloscope to the following test points on drive PCA-A2:

   Channel A — PREAMP +
   Channel B — PREAMP −

   Use drive PCA-A2 INDEX H test point for oscilloscope sync and GND 3 point for signal ground.

d. Set the oscilloscope controls as follows:

   Sweep — 20 msec/div
   Sensitivity — 0.01 volt/div
   Input — DC
   Trigger — EXT, DC, +, NORM
   Display — A + B, INV B

e. Make an estimate of the relative humidity in the room where the drive is operating, i.e. is it low (8% to 39%), medium (40% to 59%), or high (60% to 80%).

f. Compare the waveform with that shown in Figure 2-12. Head Radial Alignment Waveforms. Use the following limits when checking the waveforms.

   LOW HUMIDITY (8% to 39%): The left lobe amplitude must be between 65% and 105% of the right lobe amplitude.

   MEDIMUM HUMIDITY (40% to 59%): The smaller lobe amplitude, either left or right, must be at least 80% of the larger lobe amplitude.

   HIGH HUMIDITY (60% to 80%): The right lobe amplitude must be between 65% and 105% of the left lobe amplitude.

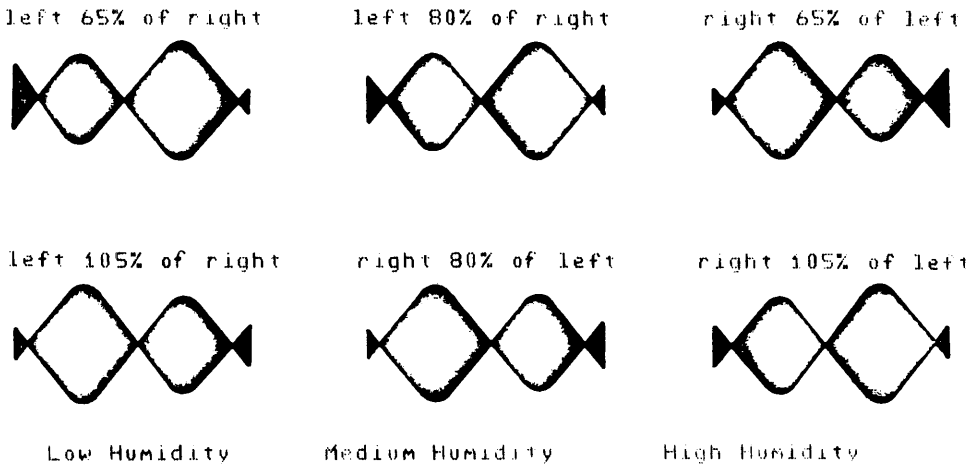


Figure 2-12. Head Radial Alignment Waveforms

g. Loosen the two mounting screws securing the motor plate to the support bracket.

h. Move the plate by rotating the eccentric adjustment nut.

i. When the lobes are within specification, tighten the motor screws.

j. Check the adjustment by stepping off track 38 and returning to it. Check in both directions.

k. Select head 1 and check that the amplitude of the two lobes is within specs. If the lobes are out of specification, repeat steps g through j. It will now be necessary to select head 0 and recheck the lobes. Continue the adjustment untilthe lobe amplitudes for both head 0 and head 1 are within specification.

l. If the specified waveforms cannot be obtained, replace the disc drive.

m. Following satisfactory adjustment of the head radial alignment, perform the track 0 detector adjustment procedure.

Removal and Replacement

Introduction

This section provides detailed removal and replacement procedues for those disc drive assemblies that are field replaceable. The order of presentation is based on which assemblies are most often removed or replaced before another assembly can be removed.

A procedure is presented early in this section for removing power from the disc drive since power must be removed before any of the assemblies can be removed.

Adjustments and/or checks must be performed following the replacement or movement of certain items in the disc drive. These items, and the required adjustments and checks, are detailed in Table 2-11.

WARNING

THE INFORMATION GIVEN IN THIS SECTION IS FOR SERVICE-TRAINED PERSONNEL ONLY. TO AVOID POTENTIALLY SERIOUS ELECTRICAL SHOCK, DO NOT PROCEED FURTHER IN THIS SECTION UNLESS QUALIFIED TO DO SO.

Table 2-11. Adjustments/Checks Required Following Component Replacement

Component	Adjustment/Check
Write Protect Detector	Write protect detector adjustment procedure.
Head Load Actuator	Head load actuator adjustment procedure. Head load actuator timing check.
Sector/Indes Phototransistor	Sector/Index phototransistor adjustment procedure.
Sector/Index LED	Sector/Index phototransistor adjustment procedure.
Track 0 Detector	Track 0 detector adjustment procedure.

Power Removal and Restoration

Most of the removal and replacement procedues given in this section require that the disc drive power be removed before they are performed. To remove power from the disc drive, proceed s follows:

a. Set the power switch on the host system of OFF.
b. Disconnect J5 and the ac power connector from the disc drive.

Power is restored to the disc drive by reversing this procedure.

Connector P2 Pin Extraction

Certain of the removal and replacement procedures require that pins (and attached wires) be extracted from connector P3. To remove a pin from connector P2, proceed as follows:

a. At the front of connector P3, insert the end of a pin extractor tool (or the end of a paper clip) between the desired pin and the wall of the connector.
b. Push down on the pin extractor to release the locking spring on the pin.
c. Remove the pin by pulling on attached wire from the rear of the connector.

To replace a pin in connector P3, push the pin into the appropriate opening at the rear of the connector until it locks in place.

NOTE

Repeated extractions of a pin will flatten the locking spring and prevent the pin from locking into the connector. When this occurs, carefully bend the spring forward until its locking action is restored.

Drive Board

The drive board is removed from the disc drive as follows:

a. Remove power from the drive.
b. Disconnect the cables from the following connectors on the drive board.
   J7, J1, J2,J6

NOTE

The drive boards are matched to the drive mechanics at the factory. For this reason, when a drive board is removed it must be reinstalled on the same drive.

---

c. Remove four screws securing the drive board to the disc drive frame.
d. Disconnect the cable from connector J3 on the drive board and remove the board from the disc drive.

The drive board is installed by reversing this procedure. Ensure that all of the connectors removed in steps b and d are firmly connected to the drive board.

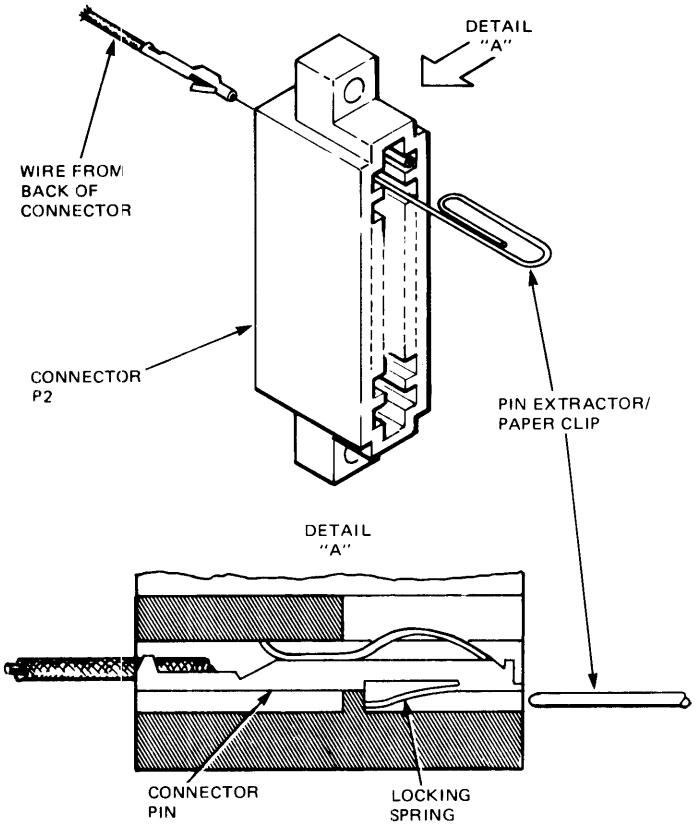


Figure 2-13. Connector P2 Pin Extraction

Head Cover Shield

The head cover shield is removed from the disc drive as follows:

a. Remove power from the disc drive.
b. Loosen the two screws securing the head cover shield to the guide opening assembly.
c. Move the head cover shield towards the head assembly until the shield is free of the two retaining screws.
d. Remove the head cover assembly from the disc drive.

The head cover shield is installed by reversing this procedure.

Cartridge Guide

Cartridge Guide Access

The cartridge guide assembly swings open to provide access to certain components mounted on the cartridge guide and the frame of the drive. To swing open the cartridge guide, proceed as follows:

a. Remove power from the disc drive.

b. Remove the head cover shield.

c. Position the read/write heads to approximately track 0 by turning the stepper actuator shaft fully counterclockwise.

d. Unlatch the cartridge guide assembly by pressing the push bar on the front of the drive.

CAUTION

THE HEADS SHOULD NEVER TOUCH EACH OTHER. ALWAYS INSERT A PIECE OF CLEAN LENS TISSUE BETWEEN THE HEADS WHEN THE HEAD LOAD BAIL IS DISENGAGED FROM THE HEAD LOAD ARM.

---

e. Refer to Figure 2-13. Carefully hold the moveable arm of head 1 with one finger while pushing the load bail up and back until the tab on the movable arm clears the head load bail. Be sure that the bail clears the head load arm before releasing the bail.

f. Insert a clean piece of lens tissue between the lower and upper heads to prevent them from touching and then gently release (lower) the moveable arm of head 1.

g. Loosen the two screws securing the door latch plate to the cartridge guide assembly.

h. Refer to Figure 2-13. Release the safety catch on the guide opening assembly by pressing the catch towards the rear of the drive. When the catch is released, swing the cartridge guide assembly up and away from the frame of the disc drive, as illustrated in Figure 2-13.

The cartridge guide assembly is restored to its normal operating position by reversing this procedure. Following restoration to normal operation, perform the cartridge guide assembly adjustment procedure.

Cartridge Guide Adjustment

To check the adjustment of the cartridge guide assembly, proceed as follows:

a. Insert end no. 2 of cartridge guide adjustment tool, part no. 1150-1310, through the cartridge guide tool hole and screw it completely into the disc drive frame. Hand tighten the tool.

b. Move the door handle into the latched position and hold it tightly against the latch.

c. Tighten the two screws securing the cartridge guide to the latch plate.

d. Remove the tool and check to determine if the flange on the clamp hub clears the cartridge guide when the spindle is rotating. If the clamp hub rubs on the cartridge guide, repeat steps a through c.

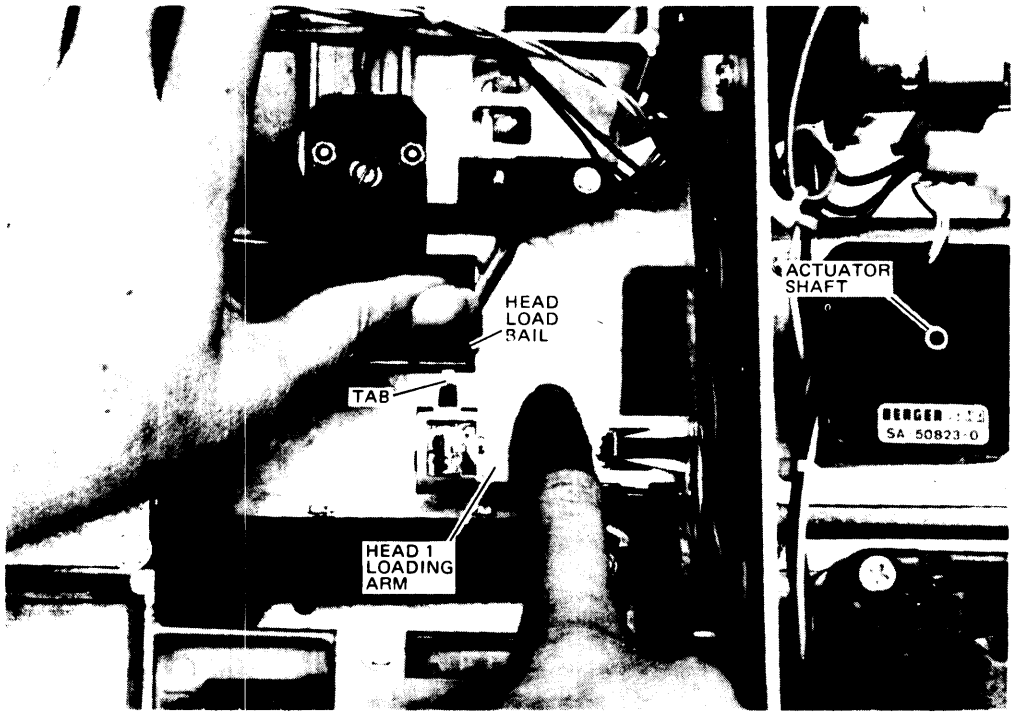
e. Adjust the cartridge guide stop so that it is within 0.005 inch of the disc drive frame.

f. Insert a flexible disc into the drive, close and open the door, and check for proper operation.

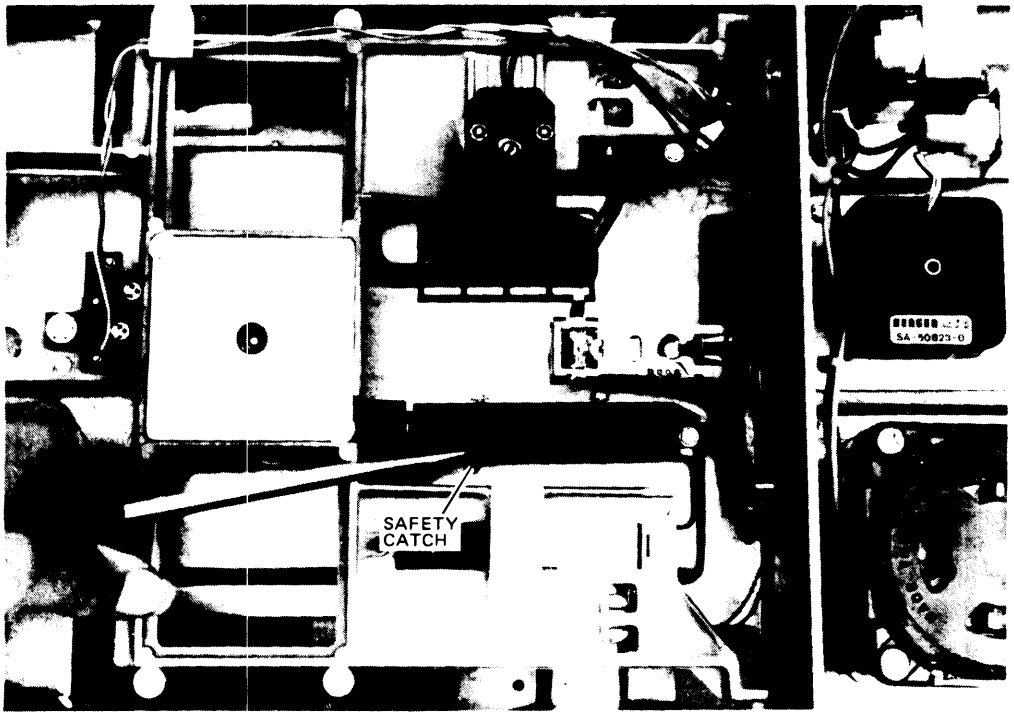
g. Following the completion of this adjustment procedure, perform the following procedures:

   1. Sector/Index Phototransistor Adjustment Procedure

2. Write Protect Detector Adjustment Procedure.
3. Head Load Actuator Adjustment Procedure.



A. HEAD UNLOADING



B. SAFETY CATCH RELEASE

Figure 2-14. Cartridge Guide Access Details

Sector/Index LED

The sector/index LED assembly is removed from the disc drive as follows:

a. Remove power from the disc drive.
b. Note the color coding of the two wires attached to the sector/index LED assembly and then unsolder the wires.
c. Remove the screw securing the sector/index LED assembly to the cartridge guide assembly and remove the LED assembly.

The sector/index LED assembly is replaced by reversing this procedure. Following installation, perform the sector/index phototransistor adjustment procedure.

Write Protect Detector

Write Protect Detector Removal

The write protect detector assembly is removed from the disc drive as follows:

a. Remove power from the disc drive.
b. Remove the drive board.
c. Extract the following pins from connector P2:

Pin	Wire
4	red
D	black
11	white
M	gray

d. Remove the screw securing cable clamp to the disc drive frame.
e. Remove the screw securing the write protect detector assembly bracket to the disc drive frame and remove the detector assembly.

The write protect detector assembly is installed by reversing this procedure. Following installation, perform the write protect detector adjustment procedure.

Write Protect Detector Adjustment

To check the adjustment of the write protect detector assembly, proceed as follows:

a. Restore power to the disc drive.
b. Insert a flexible disc having an open write protect notch (or hole) into the disc drive.
c. Using a 10:1 probe, connect an oscilloscope to the WPRTH test point on the drive board. Use drive board GND 1 test point for signal ground.

NOTE

All oscilloscope sensitivity settings given in this section assume the use of 10:1 oscilloscope probes. If 1:1 probes are used, the sensitivity settings should be scaled accordingly.

---

d. Set the oscilloscope controls as follows:

   Sweep — 2 msec/div
   Sensitivity — 0.1 volt/div
   Input — DC
   Trigger — INT, DC
   Display — A

e. Slightly loosen the screw securing the write protect detector assembly bracket to the disc drive.

f. Adjust the position of the write protect detector assembly until the waveform observed on the oscilloscope is at maximum amplitude. Tighten the screw loosened in step e.

g. Check that the position of the write protect detector does not restrict insertion of a flexible disc into the disc drive. If necessary repeat steps e and f above.

Head Load Actuator

Head Load Actuator Removal

The head load actuator assembly is removed from the disc drive as follows:

a. Remove power from the disc drive.

b. Remove the head cover shield.

c. Extract the following pins from connector P2.

Pin	Wire
17	black
U	black

d. Swing open the cartridge guide assembly.

e. Remove the screw securing the head load actuator to the cartridge guide assembly.

The head load actuator is installed by reversing this procedure. Hold the actuator in the position shown in Figure 2-14 when tightening its mounting screw. Do not install the head load shield at this time. Following installation of the actuator, perform the head load actuator adjustment procedure and the timing check.

Head Load Actuator Adjustment

To check the adjustment of the head load actuator assembly, proceed as follows:

a. Restore power to the disc drive.

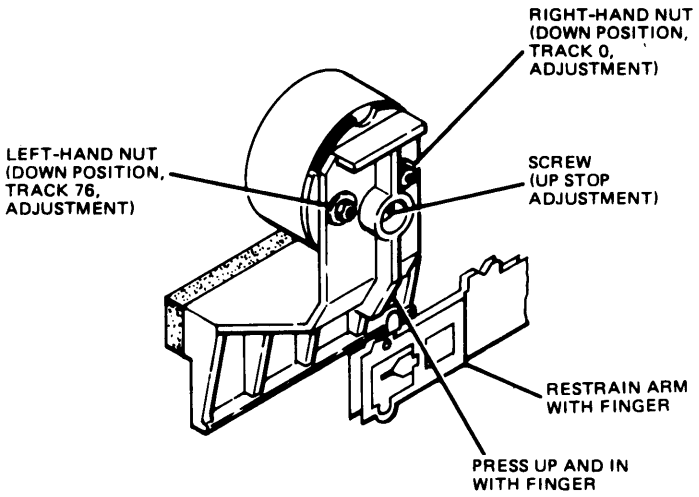
b. Position the heads to approximately track 0.

c. Insert a flexible disc into the disc drive and energize the head load actuator coil by selecting the drive.

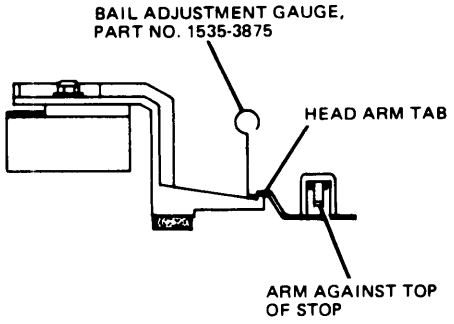
d. The down position of the head load actuator bail is adjusted with two self-locking nuts that secure the bail to the actuator.

e. With the read/write heads at track 0, adjust the right-hand nut until the tip of bail

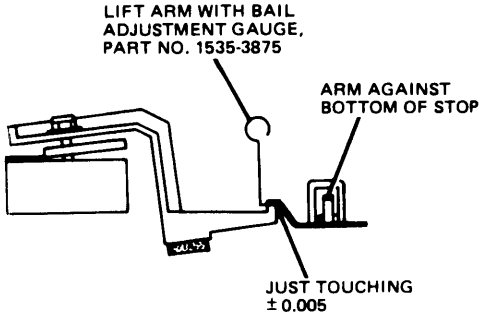
adjustment gauge, part no. 1535-3875, just fits between the bail and the tab on the head 1 moveable arm.



A. ADJUSTMENT CONTROLS AND UNLOADING DETAILS



B. DOWN POSITION ADJUSTMENT



C. UP POSITION ADJUSTMENT

Figure 2-15. Head Load Actuator Unloading and Adjustment Details

f. Position the heads at track 76 and repeat step e, this time adjusting the left-hand nut.

g. Return to track 0 and recheck the clearance. If necessary, readjust the setting of the right-hand nut.

h. Continue to check the clearance at track 0 and track 76 until both are correct.

i. Deselect the drive and open the cartridge guide assembly by pressing the push bar on the front panel of the drive.

j. With the loop of the bail adjustment tool hooked over the tip of the load arm tab, carefully pull the arm out to its maximum travel (do not flex the arm).

k. Adjust the up stop adjustment screw until the bail just contacts the tab of the head load arm. It may be necessary to first adjust the screw too far in and back if off, as required.

l. Following the adjustment, ensure that there is clearance between the disc and the outside head when a flexible disc is inserted into the drive.

Head Load Actuator Timing Check

To check the timing of the head actuator, proceed as follows:

a. Restore power to the disc drive.

b. Insert a flexible disc into the disc drive. Select head 0 and step to track 0. Write a series of 0's on the disc.

c. Using 10:1 probes, connect an oscilloscope to the following test points on the drive board:

   Channel A — PREAMP +
   Channel B — −

   Use test point HDLDL on the drive board for oscilloscope sync and test point GND 3 for signal ground.

d. Set the oscilloscope controls as follows:

   Sweep — 10 msec/div
   Sensitivity — 0.01 volt/div
   Input — DC
   Trigger — EXT, −, DC, NORM, SINGLE
   Display — A + B, B INV

e. Observe the read signal on the oscilloscope. The signal should reach 50% of full amplitude in 35 milliseconds or less. See Figure 2-15. If this is not the case, proceed with the remainder of this procedure.

f. Repeat the head load actuator adjustment procedure.

CAUTION

DO NOT ADJUST THE HEAD LOAD ACTUATOR UP STOP ADJUSTMENT SCREW MORE THAN ¼-TURN CLOCKWISE.

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g. Repeat step e. If the timing is still not correct, adjust the head load actuator up stop adjustment screw clockwise until the timing is correct.

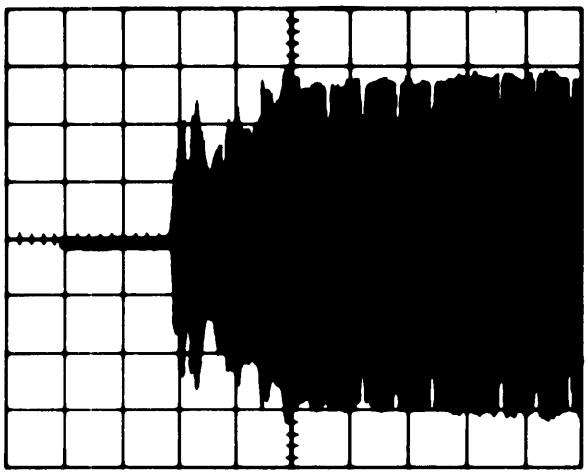


Figure 2-16. Head load Actuator Timing Check Waveform

Sector/Index Phototransistor

Sector/Index Phototransistor Removal

The sector/index phototransistor assembly is removed from the disc drive as follows:

a. Remove power from the disc drive.
b. Disconnect connector P2 from the drive board.
c. Detach the following wires from the door closed switch.

Switch	Wire
Common	orange
N/C	gray
N/O	red

d. Extract the following wires from connector P2:

Pin	Wire
12	black
N	green
P	brown
6	orange
F	gray
H	red

e. Remove the screw securing cable clamp to the frame of the drive.
f. Remove the sector/index phototransistor assembly from the disc drive.

The sector/index phototransistor assembly is installed by reversing this procedure. Following installation, perform the sector/index phototransistor adjustment.

Sector/Index Phototransistor Adjustment

To check the adjustment of the sector/index phototransistor assembly, proceed as follows:

a. Restore power to the disc drive.

b. Insert double-sided alignment disc, part no. 9164-0111, into the disc drive and close the door.

c. Using 10:1 probes, connect an oscilloscope to test point INDEX H on the drive board.

d. Set the oscilloscope controls as follows:

   Sweet — 2 msec/div
   Sensitivity — 0.2 volt/div
   Input — DC
   Trigger — INT, +, DC, NORM
   Display — A

e. Check that two pulses are present as shown in the Figure 2-16. The amplitude of the pulses should be approximately 4.0 volts. If the two pulses are not correct, proceed to step f and attempt to obtain the correct signal. If it is correct, the procedure is complete.

f. Loosen the screw securing the sector/index phototransistor assembly until the assembly can just be moved.

g. Adjust the position of the sector/index phototransistor assembly until the oscilloscope waveform agrees with step e.

h. Tighten the sector/index transistor assembly retaining screw and check that the waveform is still acceptable.

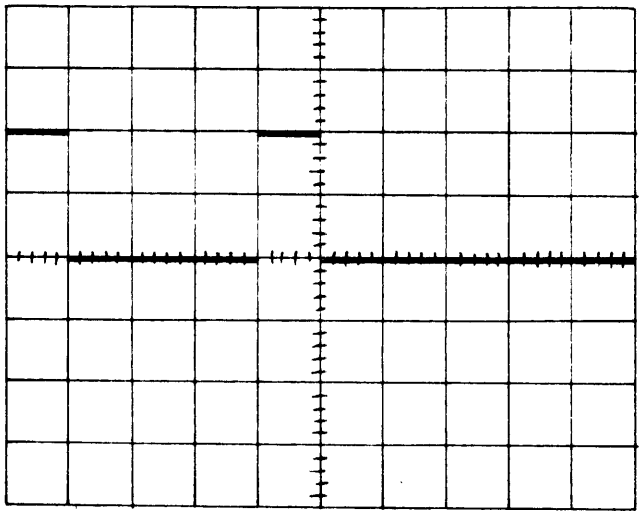


Figure 2-17. Index Pulse Waveform

Track 0 Detector

Track 0 Detector Removal

The track 0 detector is removed from the disc drive as follows:

a. Remove power from the disc drive.
b. Manually rotate the stepper actuator shaft fully clockwise to track 77.
c. Remove the screw securing the track 0 detector bracket to the frame of the disc drive and remove the track 0 detector assembly.
d. Remove the drive PCA from the disc drive.
e. Extract the following pins from connector P2:

Pin	Wire
3	brown
C	black
O	orange
L	red

f. Remove the screw securing the cable clamp to the disc drive.
g. Remove the track 0 detector from the disc drive.

The track 0 detector is installed by reversing this procedure. Following installation, perform the track 0 detector adjustment procedure.

Track 0/76 Stop Adjustment

This adjustment is not field adjustable.

Track 0 Detector Adjustment

To check that the track 0 detector is correctly adjusted, proceed as follows:

a. Before performing this procedure, check the head radial alignment and adjust if necessary.
b. Insert the alignment disc into the disc drive.
c. Loosen the screw securing the track 0 detector and move the detector back as far as possible toward the actuator assembly. Tighten the securing screw.
d. Recalibrate the disc drive by pressing the RESET pushbutton on the DSU.
e. Using 10:1 probes, connect an oscilloscope to the following points on the drive board:

   Channel A — PREAMP +
   Channel B — PREAMP −

f. Use test point INDEX H on the drive board for oscilloscope sync and test point GND 3 for signal ground.
g. Set the oscilloscope controls as follows:

   Sweep — 20 msec/div
   Sensitivity — 0.01 volt/div
   Input — DC
   Trigger — EXT, −, DC, NORM
   Display — A + B, B INV

h. Using the DSU, step the carriage assembly in until the data burst recorded on track 0 is visible.

i. Loosen the screw securing the track 0 detector and move the detector forward until the TRACK 0 LED on the DSU lights. Tighten the securing screw.

j. Using a 10:1 probe, connect the oscilloscope to drive PCA test point TK0H. use drive PCA GND 1 test point for signal ground. Set oscilloscope for a vertical deflection of 0.1 volt/div, continuous sweep.

k. Check that voltage level at TK0H test point is high (+5 volts).

l. If the voltage is not high, loosen the screw securing the track 0 detector. Move the detector forward towards the spindle until the TK0H test point goes high.

m. Step the carriage to track 02. Check that the TK0H test point goes low. If this is not the case, move the track 0 detector back towards the actuator assembly.

n. Recheck the adjustment by stepping the heads between tracks 01 and 02. Check that TK0H test point is low at track 02 and high at track 01. A perfect adjustment presents a squarewave on the oscilloscope.

Front Plate

The front plate assembly is removed from the disc drive as follows:

a. Remove power from the disc drive.

b. Insert the cartridge guide adjustment tool through the cartridge guide tool hole in the cartridge guide assembly and screw it into the disc drive frame. Hand tighten the tool.

c. Remove the following pins from the connector P2:

Pin	Wire
2	black
B	brown
9	blue
K	purple

d. Remove the screw securing cable clamp and remove the clamp.

e. Remove the two Allen-head screws securing the handle to the front plate and remove the handle.

f. Remove the two screws securing the lock plate assembly to the front plate.

The front plate is installed by reversing this procedure. Following replacement, perform the sector/index phototransistor adjustment procedure.

Lock Plate Assembly

The lock plate assembly is removed from the disc drive as follows:

a. Perform the front plate removal procedure.

b. Remove the lock plate assembly from the disc drive.

The lock plate assembly is replaced by reversing this procedure. Following installation, adjustment of the door lock solenoid (10) should not be necessary. If adjustment is required, the gap between the armature tab and the latch should be 0.15 ± 0.010 inch. The adjustment can by made by loosening the two screws on the armature.

Line Frequency Conversion Procedure

The following procedure is given to convert the 7902A drive from 60 Hz operation to 50 Hz operation or vice versa.

The parts required to perform the conversion are as follows:

For 60 Hz operation

1 — Drive pulley HP part no. 1500-0499
1 — Drive belt HP part no. 1535-3651

For 50 Hz operation

1 — Drive pulley HP part no. 1535-3650
1 — Drive belt HP part no. 1535-3649

Follow these steps to perform the conversion:

1. Remove the drive board from the drive assembly.
2. Remove and retain the old drive belt and pulley. The pulley is held in place with a small setscrew.
3. Install the new drive pulley by sliding it onto the drive motor shaft until it touches the motor fan. Tighten the setscrew and install the new drive belt.
4. Reinstall the drive board.

Replaceable Parts

Introduction

This section provides the HP 7902A flexible disc drive parts list. The total quantity of a part is shown only the first time it is used on a particular assembly.

The number shown in the "CD" column is the part number's check digit. Include the check digit number wth the part number when ordering a part from HP.

Table 2-12. HP 7902A Replaceable Parts

HP Part No.	CD	Description	Units Per Assembly
		Disc Drive Assembly	1
1535-3652	0	Door Closed Switch	1
1535-3847	5	Lock Plate Assembly	1
1535-3872	6	Sector/Index Phototransistor Assembly	1
1535-3651	9	Drive Belt 60 Hz	1
1500-0499	4	Drive Pulley 60 Hz	1
1535-3649	5	Drive Belt 60 Hz	1

1535-3650	8	Drive Pulley 50 Hz	1
1535-3870	0	Head Load Actuator	1
1535-3871	5	Sector/Index LED Assembly	1
1150-1309	4	Write Protect Detector Assembly	1
1535-3873	7	Track 0 Detector Assembly	1
9164-0096	1	Flexible Disc, Double-Sided, Unformatted	

9895K Flexible Disc Drive (HP Part No. 09895-67914)

Introduction

This section provides interface and maintenance information for the 9895K flexible disc drive.

Power Requirements

Table 2-13: HP 9895K Disc Drive Power Requirements

Drive Board (A2)
+5V 0.6A typical, 0.7A max, voltage tolerance: ±5%,
+24VDC 1.4A Nominal, voltage tolerance ±10%.

Disc Drive Assembly
86 — 127 Vac at 0.3A typical, 0.44A max
50/60 Hz ±3.5% HP Format
50/60 Hz ±1% IBM Format

Cooling Requirements

The operating limits of the disc drive assembly and medium are specified as 10°C to 40°C, 20 to 80 percent relative humidity (RH) with maxium wet-bulb temperature of 25.5°C. These limits allow for a rise in the disc drive of 10°C. The actual operating limits are set by the medium. IBM sets the limits at 10°C to 52.6°C, 8 to 80 percent RH, maximum wet-bulb temperature of 29.4°C.

Shielding Requirements

No shielding is required under normal operating conditions. If the disc drive assembly is subjected to medium to high-intensity electromagnetic fields such as those from the yoke of a cathode-ray tube, an aluminum or steel shield should be placed between the source of the field and the disc drive. The head load solenoid has a small dc external field that may cause CRT deflection. A steel shield wrapped around the disc drive assembly will eliminate this source of interference.

Interface Information

Figure 2-17 shows the location of the connectors on the CDC industry standard drive board A2. Connection to the controller is through the 50 pin connector A2J1. DC power is supplied via connector A2J4. Refer to Table 2-14 for the connector pin assignments.

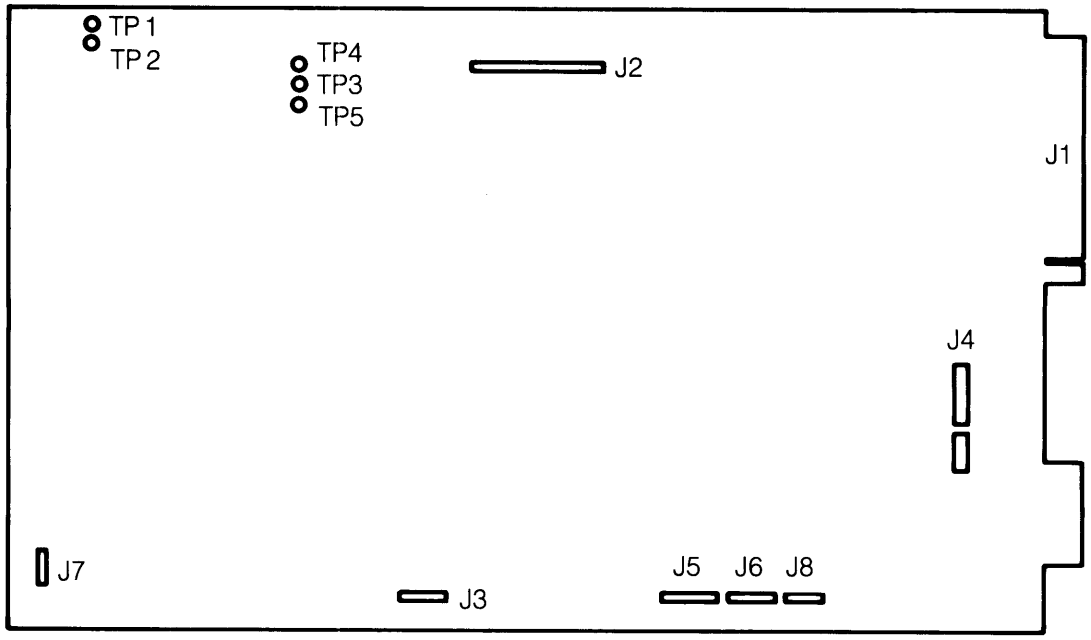


Figure 2-18. CDC Industry Standard Drive Board

Table 2-14. Connector Pin Assignments

J4

Pin	Description
1	Not Used
2	+5VDC
3	GND
4	+24VDC
5	Key
6	+24VDC Return
7	Not Used

A2J1

2	Low Current
4	Opt.
6	Opt.
8	Opt.
10	Two Sided
12	Disc Change
14	Head Select (Opt.)
16	In Use
18	Head Load
20	Index
22	Drive Ready
24	Sector

26	Drive Select 1
28	Drive Select 2
30	Drive Select 3
32	Drive Select 4
34	Direction
36	Step
38	Write Data
40	Write Enable
42	Track 00
44	Write Protect
46	Read Data
48	Sep Data
50	Sep Clock

Alignment and Adjustments

Introduction

This section provides information for the alignment and adjustments which may be performed on the 9895K flexible disc drive. This drive assembly is identical to the one used in the 9895A. Additional adjustments may be performed by inserting the 9895K drive assembly into a 9895A and following the procedures as outlined in the 9895A service manual.

DC Voltage and SignalCheck of Drive Module

1. Input dc power should be +5 Vdc ±5% at pin 5 of dc connector (pin 6 is +5V return), and +24V ±10% at pin 1 (pin 2 is +24V return).
2. Various detector functions can be checked by observing the dc level at the board connector. Table 2-15 contains a list of these functions and the point to check for the signal.

Table 2-15. Detector Functions

Function	Connector, Pin 2 Wire Color
Write Protect	J5-12 Red
Track 0	J6-3 Red
Index (Single-Sided)	J6-5 Black
Index (Double-Sided)	J6-6 Purple
Door Closed	J5-2 Yellow

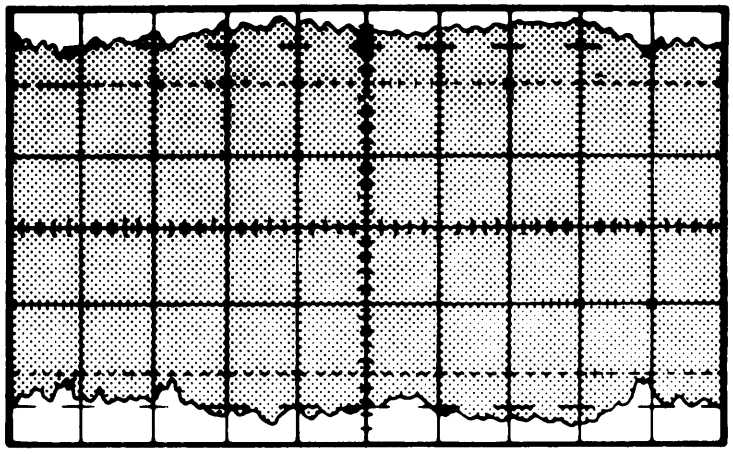
3. Certain functions used in the adjustment procedures have built-in test points. These functions are listed in Table 2-16.

Table 2-16. Adjustment Test Points

Function	Test Point
Differentiated Analog	1
Read Data (Differential)	2
Analog Read Data	3
Differential	4
Ground	15

SCOPE
SETTINGS:

200mv/cm
20ms/cm



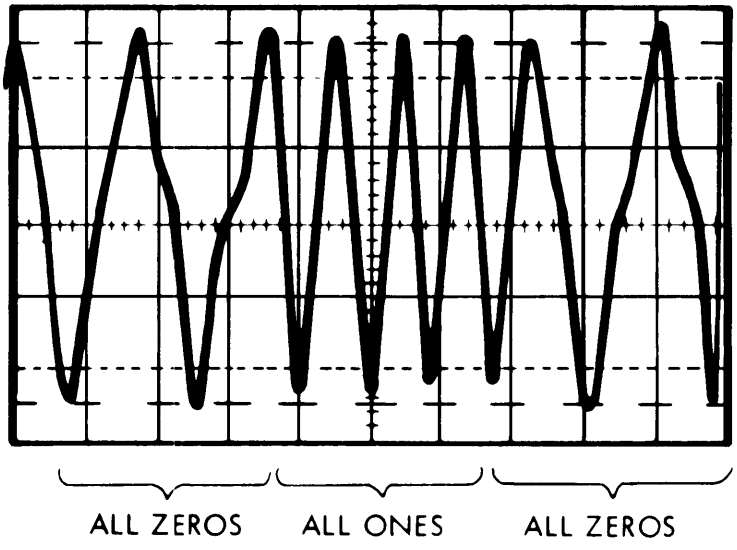
TP3 AND TP4

APPROX. AMPLITUDE RANGE,
INNER TO OUTER TRACKS:
100mv - 1100mv ALL ONES
300mv - 1200mv ALL ZEROS

Figure 2-19. Differential Read Signal for Entire Track

SCOPE
SETTING:

200mv/cm
10us/cm



TP3 AND TP4

Figure 2-20. Differential Read Signal for Portion of Outer Track

Corrective Maintenance Procedures

There are no corrective maintenance procedures for the power module or the controller, except replacement. There are a number of corrective adjustments for the drive module. This section contains these adjustments. They are as follows:

Disc Ejector Adjustment
Disc Load-Pad Adjustment
Head-Unload Clearance Adjustment

Disc Ejector

Insert a disc fully and note a clicking noise as the ejector engages a pin on the door.

While observing the ejector latch and latch block close the door. Note that closing the door moved the ejector further to the rear, allowing the latch to rotate counterclockwise until the tip drops over the step in the latch block.

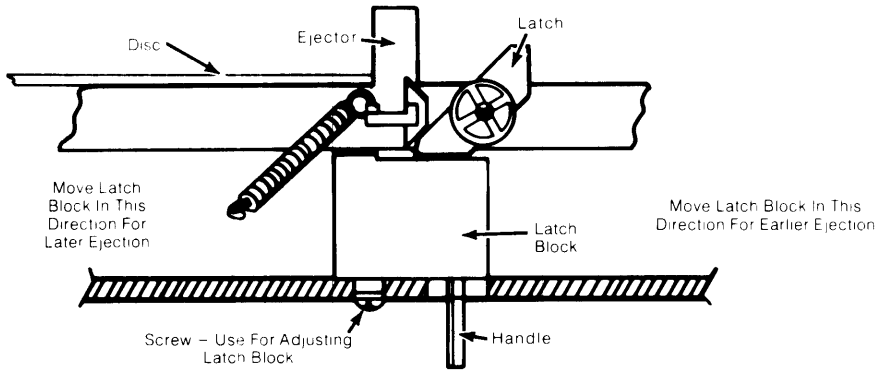


Figure 2-21. Ejector, Latch and Latch Block

With the door closed, adjust the latch block (Figure 2-20) so the tip of the latch directly below the rear edge of the ejector.

Check by opening the door slowly and observing the door position when the disc is ejected. To avoid damage, it is to be ejected when the door is ¼ inch maximum from the fully opened position. If further adjustment is required, move the latch block as indicated by the arrows and instruction in Figure 2-20.

Cycle the door several times and observe the the disc ejection is within the ¼ inch maximum described above.

Disc-Load-Pad Adjustment

1. Install a disc.
2. Close the door and load the heads by seeking to a track.
3. Loosen solenoid mounting screws.
4. Move solenoid down on bracket to obtain a clearance of 0.010 to 0.015 inch between

the load plate and the lift extension of the upper-head arm at the location of mimimum clearance. Move the carriage through its full travel manually to determine the location of minimum clearance.

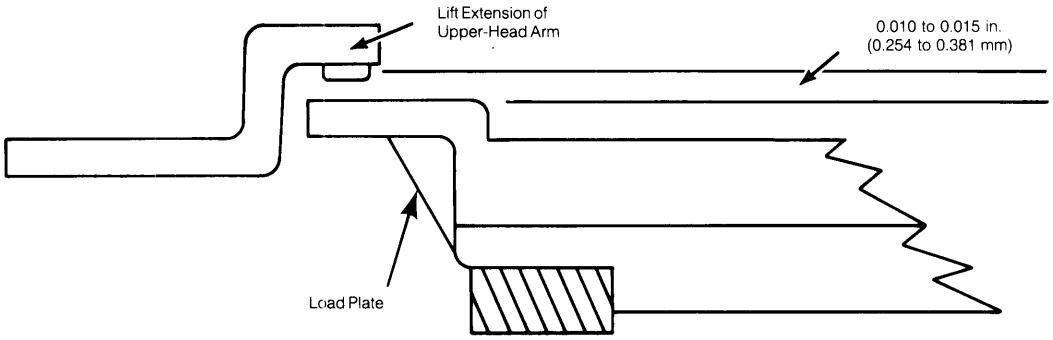


Figure 2-22. Load-Pad Adjustment

Head-Unload Clearance

Adjust setscrew on door for 0.100 inch to 0.125 inch clearance (Figure 2-22) between flyer pads with head-load solenoid de-energized and door closed.

CAUTION
MEASURE THIS DISTANCE BY EYE ONLY. DO NOT USE A GAUGE.

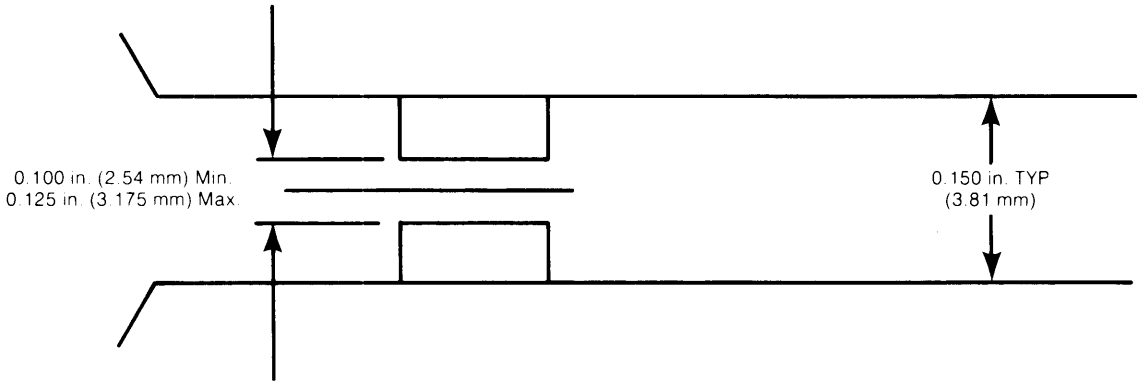


Figure 2-23. Head Unload Clearance

Line Frequency Conversion Procedure

This procedure is to be used to convert the unit from 60 Hz operation to 50 Hz operation, or vice versa. This is accomplished by reversing the dual-diameter reversible pulley on the spindle-motor shaft using the following steps:

1. Remove ac power.

2. Remove printed circuit board assembly.
3. Remove the belt from the spindle-motor pulley (accessible from the underside of unit).
4. Loosen setscrew and remove pulley.
5. Reverse pulley and replace on motor shaft.
6. Position pulley allowing clearance of 0.039 inch, ±0.010 inch between shoulder of motor mounting screws and pulley (Figure 2-23).
7. Tighten down setscrew.
8. Replace belt and printed circuit board.

CAUTION
IT IS IMPORTANT THAT THE NEW OPERATING FREQUENCY BE MARKED ON THE UNIT'S RATING NAMEPLATE. .

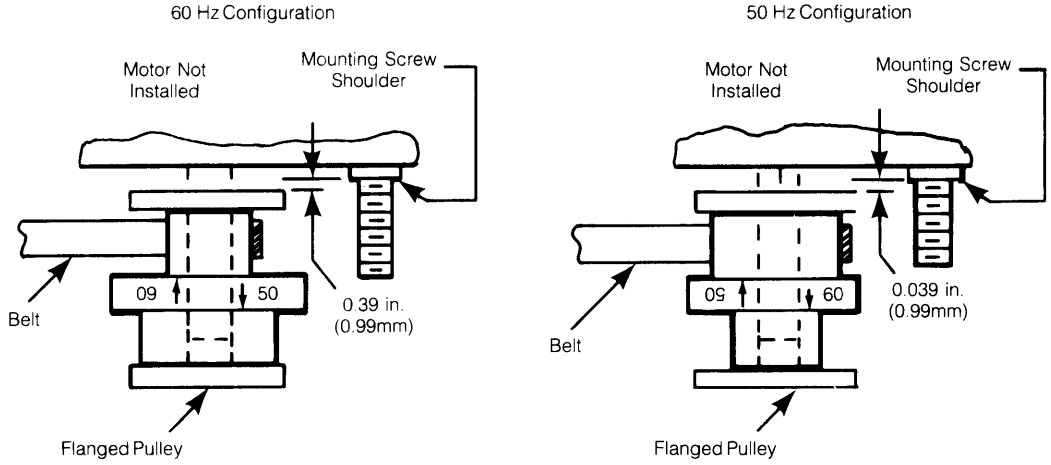


Figure 2-24. Drive Pulley Reversal

7902C Flexible Disc Drive (Part No. 07902-67902)

Introduction

This section contains interface and maintenance information for the 7902C flexible disc drive.

Power Requirements

Table 2-17. HP 7902C Disc Drive Power Requirements

Drive Board (A2)
+5V 0.6A typical, 0.7A max, voltage tolerance: +5%, −3%
+12V 0.8A typical, 1.0A max, voltage tolerance: ±5%
−12V 0.8A typical, 1.0A max, voltage tolerance: ±5%

Disc Drive Assembly
86 — 127 Vac at 0.3A typical, 0.44A max
50/60 Hz ±3.5% HP Format
50/60 Hz ±1% IBM Format

Cooling Requirements

The operating limits of the disc drive assembly and medium are specified as 10°C to 40°C, 20 to 80 percent relative humidity (RH) with maximum wet-bulb temperature of 25.5°C. These limits allow for a rise in the disc drive of 10°C. The actual operating limits are set by the medium. IBM sets the limits at 10°C to 52.6°C, 8 to 80 percent RH, maximum wet-bulb temperature of 29.4°C.

Shielding Requirements

No shielding is required under normal operating conditions. If the disc drive assembly is subjected to medium to high-intensity electromagnetic fields such as those from the yoke of a cathode-ray tube, an aluminum or steel shield should be placed between the source of the field and the disc drive. The head load solenoid has a small dc external field that may cause CRT deflection. A steel shield wrapped around the disc drive assembly will eliminate this source of interference.

Interface Information

Figure 2-24 shows the location of the connectors on drive board A2. Connection to the controller is through a 50-pin connector A2J7. DC power is connected via A2J4. Table 2-5 lists the pin assignments for connectors A2J3, J4 and J7. Power for the DSU is supplied by connector A2J9. Connections for a disc drive display panel are provided by connector A2J2.

AC power for the disc drive assembly is connected directly to a 3-pin connector, located on the drive, between the actuator and the spindle motor capacitor. See Figure 2-25. Pin assignments for the connector are as follows:

Pin	Signal
1	ac line
2	frame ground
3	ac neutral

Mating parts for the connector are:

Body, part no. 1251-3913 (Amp 1-480700-0)
Pin, part no. 1251-3915 (Amp 350547-1)

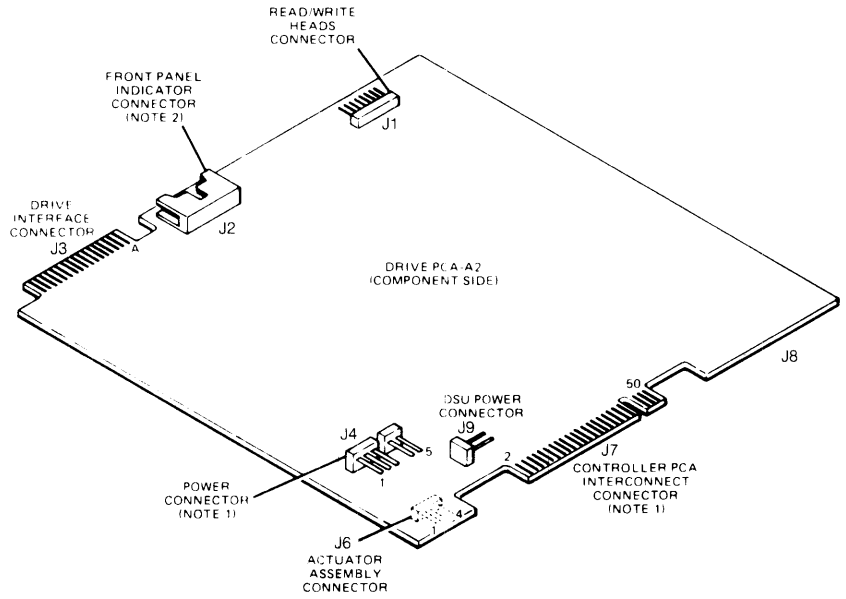


Figure 2-25. HP Drive Board A2 Connectors

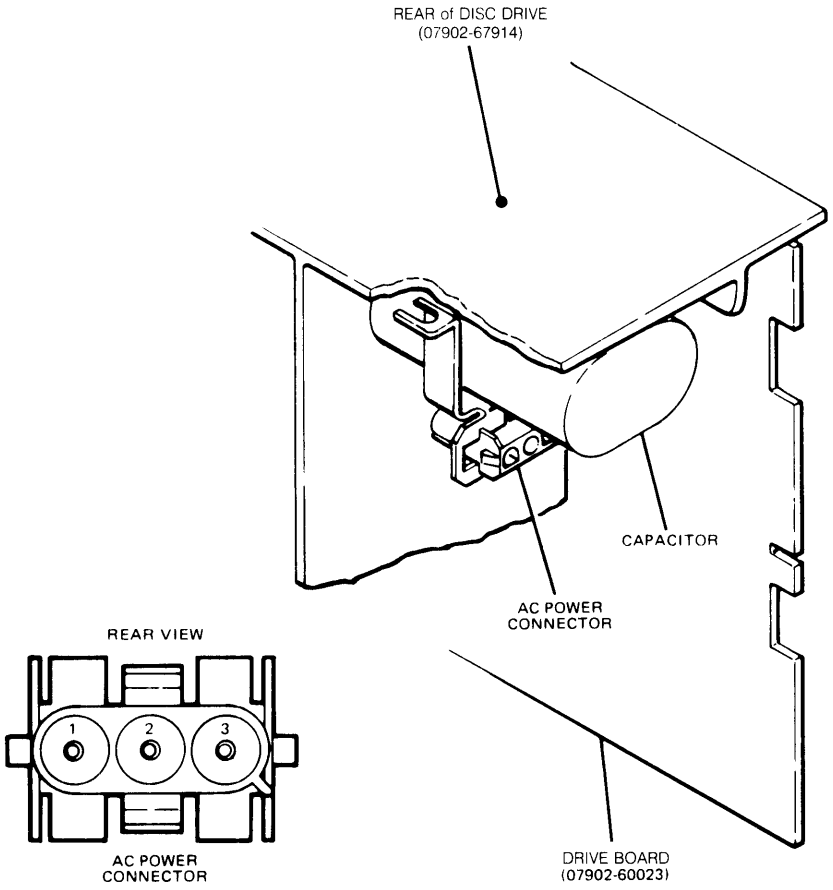


Figure 2-26. AC Power Connector

7902C Alignment and Adjustments

The 7902C disc drive assembly is an exchange assembly that is non-repairable. With the exception of the drive belt and pulley for line frequency conversion, component part replacement on this assembly can not be done.

Line Frequency Conversion Procedure

The following procedure is given to convert the 7902C drive from 60 Hz operation to 50 Hz operation or vice versa.

The parts required to perform the conversion are as follows:

For 60 Hz operation

1 — Drive pulley HP part no. 1500-0499
1 — Drive belt HP part no. 1535-3651

For 50 Hz operation

1 — Drive pulley HP part no. 1535-3650
1 — Drive belt HP part no. 1535-3649

Follow these steps to perform the conversion:

1. Remove the drive board from the drive assembly.
2. Remove and retain the old drive belt and pulley. The pulley is held in place with a small setscrew.
3. Install the new drive pulley by sliding it onto the drive motor shaft until it touches the motor fan. Tighten the setscrew and install the new drive belt.
4. Reinstall the drive board.

Chapter 3
Controller Boards

Introduction

This section contains the controller boards Theory of Operation, System Self-tests, in Use LED Patterns, Operation, Block Diagrams, Interface Information, Schematic Diagrams and Replaceable Parts Lists.

The first part of this section describes the theory of operation for the 07902-60024 and 45000-66510 controller boards, followed by the theory of operation for the 07902-66510, 07902-66520 and the 07902-66501 controller boards.

Controller Board Theory of Operation (P/N 07902-60024/45000-66510)

Controller board A1 provides an interface between the Hewlett-Packard Interface Bus (HP-IB) channel and up to four disc drives. Commands are accepted from the HP-IB channel and interpreted to provide the proper operating sequences for the selected disc drive. This includes providing control and timing signals, sending data to the disc drive, receiving data from the disc drive, and handling all input/output communication with the drive channel. A1 interprets HP-IB channel commands for seeks, data transfers, and error reporting; provides the control signals to the drive board A2; and receives the resulting status information.

If an error occurs, or when a flexible disc is removed or inserted into a disc drive, PCA-A1 requests attention from the HP-IB. A1 also generates and decodes error detection bits which are recorded with the data. In addition to these normal operations, self-tests are performed on A1 and any connected disc drives.

Figure 3-1 shows the basic organization of A1. A processor system occupies the top half of the figure and the bottom half is occupied by a disc drive interface. The processor system includes an HP-IB interface (PHI) chip, a micro-CPU (MC^2) chip, and associated read-only and random-access memories. The disc drive interface circuitry includes a data serializer/deserializer (SERDES), a cyclic redundancy check (CRC) generator checker, a data decoder, a data encoder, and control and status registers.

HP-IB Interface

The PHI chip provides a high-speed interface to the HP-IB via PHI/HP-IB converters for the host system and the MC^2. The PHI appears to the MC^2 as a bank of eight addressable registers. All interaction with the HP-IB is performed by reading or writing these registers. In addition, the PHI chip provides buffering for inbound and outbound data through two

8-byte FIFO's which can be accessed by the host processor. The lines provided by the PHI chip for interfacing to MC² include:

- A 10-bit wide data bus.
- Three register select lines for selecting among the eight registers.
- A data direction line for specifying either reading or writing of the selected register.
- Two handshake lines to coordinate data transfer.
- An interrupt line to alert the host processor of selected events.

Four quad instrumentation bus transceivers are used with the PHI chip for interfacing with the HP-IB. Two transceivers are assigned for 8-bit data transfer between the HP-IB and the PHI chip and two are used for HP-IB commands and handshakes.

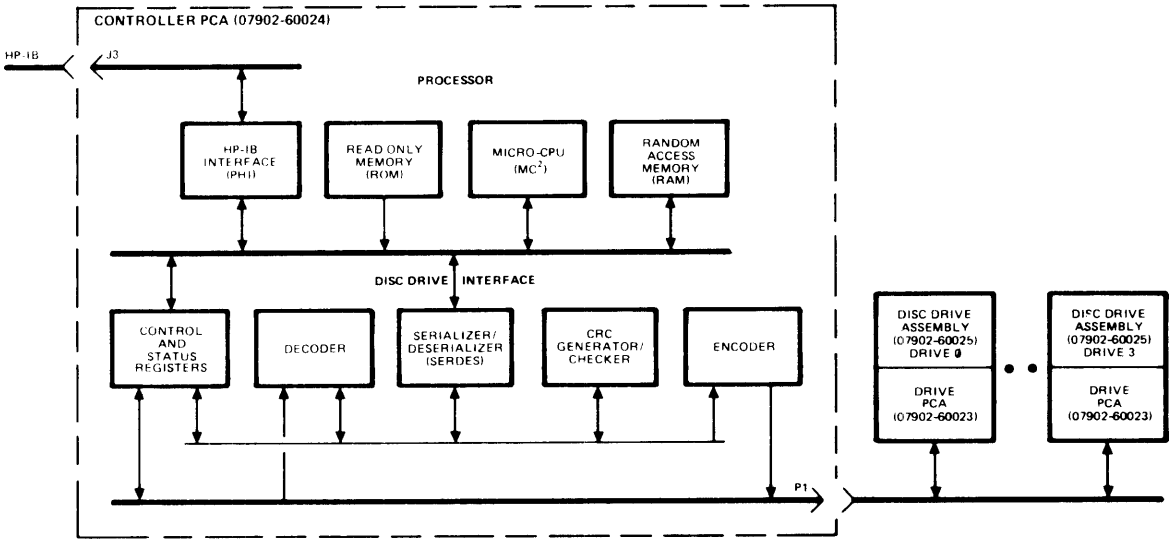


Figure 3-1. Controller A1 (07902-60024 and 45000-66510) Block Diagram

Processor

The MC² chip is a 16-bit parallel, high performance, low power processor that is designed for controller applications. The instruction cycle is typically 0.95 to 2 microseconds to execute any of the fixed width, 16-bit instructions which can process one, four, eight or 16-bit fields. Operations for logical decision making include direct bit testing of internal and external registers, indexed branches, priority encoder for most significant bit finder, external event synchronization, and a program status register that records salient characteristics of the last produced result.

When the MC² has control, data may be moved from the RAM to the HP-IB, from the HP-IB to the RAM, or from the TTL bus to the MC². When idle, direct data transfer between the TTL bus and the RAM or the HP-IB is possible. Since the MC² contains several internal

registers, all other registers on the controller board are considered to be external registers. Therefore, when operating on external registers, the program provides appropriate commands to selected registers, using the external control lines.

Two 24-pin 256 x 8 random access memory (RAM) chips are used in A1. Part of the RAM is called the buffer, part is called the stack, and part is used as a scratch pad. The buffer holds the preamble, data, and postamable either before they are sent to the disc drive or after receiving them from the disc drive. The stack is used when the MC^2 calls up subroutines and the scratch pad is for temporary storage of variables used by the program.

Eight 24-pin, 1024 x 8 read only memory (ROM) chips are used for main program storage, including the self-test program.

Decoder

When a disc drive is reading from a disc, controller A1 receives a pulse from every flux transition which is detected on the disc. The decoder synchronizes itself with this pulse train and separates it into clock and data pulses according to the rules of the recording format in use. These pulses are used to generate serial data and serial clock signals which are fed to the SERDES. The decoder consists of a phase-locked loop, a data separator, and some sequencing logic.

Encoder

When a write is taking place, the disc drive requires a pulse whenever a transition should be written on the disc. The encoder takes serial data and clock information from the SERDES (or CRC) and converts it to the pulse stream needed by the disc drive. The encoder employs the encoding rules of the format being used. This includes the addition of precompensation when the HP double density format is selected.

For diagnostic purposes, the encoder can be connected directly to the decoder. This allows testing much of the controller hardware without writing on or reading back a flexible disc.

Serializer/Deserializer

The serializer/deserializer (SERDES) is basically a shift register which converts serial data to parallel data or vice versa. There are two shift registers — one for data and one for clock information. When reading from a disc, serial data and serial clock are shifted into the SERDES. This produces parallel data and parallel clock that the MC^2 can read. When writing to a disc, the MC^2 writes parallel data and clock into the SERDES which then shifts it out to generate serial data and serial clock which are sent to the encoder and CRC circuitry. The SERDES appears to the MC^2 as two registers in the external register bank dedicated to the selected disc drive.

CRC

In order to allow detection of errors, cyclic redundancy check (CRC) information is recorded along with data on the flexible disc. When writing a field on the disc, the CRC circuitry uses the serial data coming from the SERDES to generate a 16-bit check word. At the end of the field, the check word is sent to the encoder to be written on the disc. When reading from the disc, serial data rom the SERDES is fed back into the CRC circuitry. A field of information and its associated check word will leave the CRC circuitry in a known state.

Thus, it is possible to determine if an error has occurred by looking at the state of the CRC circuitry after read has been completed.

Control and Status Registers

Six registers in the disc external register bank allow the MC^2 to manipulate and test various signals from the controller and the disc drives. This includes MC^2 control of which disc drive is selected, the operation of the head actuator stepping motor, head selection, the self-test LED's and the operation of read/write circuitry in the controller. The MC^2 can test the status of the selective drive. the self-test and device address switches, and the status of the read/write circuitry in the controller. In addition to the registers, there is also logic that controls the handshaking with the processor system.

Firmware

In order to read or write the disc, the MC^2, under firmware control, must sequence the operation of the other parts of the controller. The following sequence is typical of how the data transfers occur.

The firmware constantly monitors the PHI chip, waiting for bytes to arrive from the HP-IB. Incoming bytes are checked to see if they form a command. If a valid read command is received, the data buffer in the RAM is filled with data from the disc. The data is then sent through the PHI chip to the HP-IB. If a write command is received, the buffer is filled with data from the HP-IB. This data is then written to the disc.

In order to transfer data between the data buffer and the disc, the proper sector of the disc must be found. To do this, the read circuitry is enabled to search for the next field on the disc. If a data field is encountered, it is ignored and a new search for the next field is started.

When an ID field is encountered, the track and sector numbers it contains are checked. If the cylinder number is incorrect, the controller attempts to seek to the proper cylinder, and then starts the process again. If the cylinder number is correct, and the sector numbers are correct, the desired sector has been found. Now, if data is to be written on the disc, the entire data field of the sector is rewritten using data from the data buffer.

Controller Board Theory of Operation (P/N 07902-66510/07902-66520 and 07902-66501)

The controller module provides an interface between a Hewlett-Packard Interface Bus (HP-IB) channel and up to four disc drives. Commands are accepted from the HP-IB channel and interpreted to provide the proper operating sequences for the selected disc drive. This includes:

- Providing control and timing signals,
- Sending data to the disc drive,
- Receiving data from the disc drive,
- Handling all input/output communication with the channel.

The controller provides control signals to the drive and receives the resulting status information.

If an error occurs, or when a disc is removed or inserted into a disc drive, the controller requests attention from the HP-IB. It also generates and decodes error detection bits which are recorded with the data. In addition to these normal operations, self-tests are performed on the controller and the disc drives.

Controller Interface to HP-IB (PHI Chip)

The PHI chip provides a high-speed interface to the HP-IB via PHI/HP-IB converters for the host system and the Z80. The PHI appears to the Z80 as a bank of eight addressable registers. All interaction with the HP-IB is performed by reading from or writing to these registers. In addition, the PHI chip provides buffering for in-bound and out-bound data through two 8-byte, first-in, first-out buffers (FIFO's) which can be accessed by the host processor. The lines provided by the PHI chip for interfacing to the Z80 include:

- An 8-bit-wide data bus,
- Three register select lines for selecting the eitht registers,
- A data direction line for specifying either reading or writing of the selected register,
- Two handshake lines to coordinate data transfer,
- An interrupt line to alert the host processor to selected events.

Four, quad instrumentation bus transceivers are used with the PHI chip for interfacing with the HP-IB. Two transceivers are assigned for 8-bit data transfer between the HP-IB and the PHI chip, and two are used for HP-IB commands and handshakes.

Processor and Memory

The processor on the controller is a Z80A microprocessor. It is a single chip, 4 MHz, 8-bit microprocessor. The Z80A executes the programs stored in four, 2048 x 8-bit Programmable Read Only Memory (PROM) chips or one, 8192 x 8-bit Read Only Memory (ROM) chip to perform the controller functions. Also available are two, 1024 x 4-bit Random Access Memory (RAM) chips for stack operations, scratchpad memory, and buffering the data sent to and from the disc drive.

The Z80A microprocessor is constantly monitoring the PHI chip for in-bound commands from the HP-IB. If it receives a command, the Z80A will execute the necessary programs from ROM to implement the command. On completion, the Z80A goes back to monitoring the PHI chip for a command.

The Z80A communicates with the PHI chip and several registers on the controller via its I/O ports. The PHI chip's registers are assigned I/O ports 10_{16} through 17_{16}, and the controller registers are assigned I/O ports 60_{16} through 67_{16}.

The controller registers contain:

- Status information rom the disc drives,
- Control signals sent to the disc drives,
- Status of switches and error indicators on the controller,
- Control signals to enable read, write, and error detection electronics on the controller, the serializer/deserializer (SERDES) registers, and the self-test LED display.

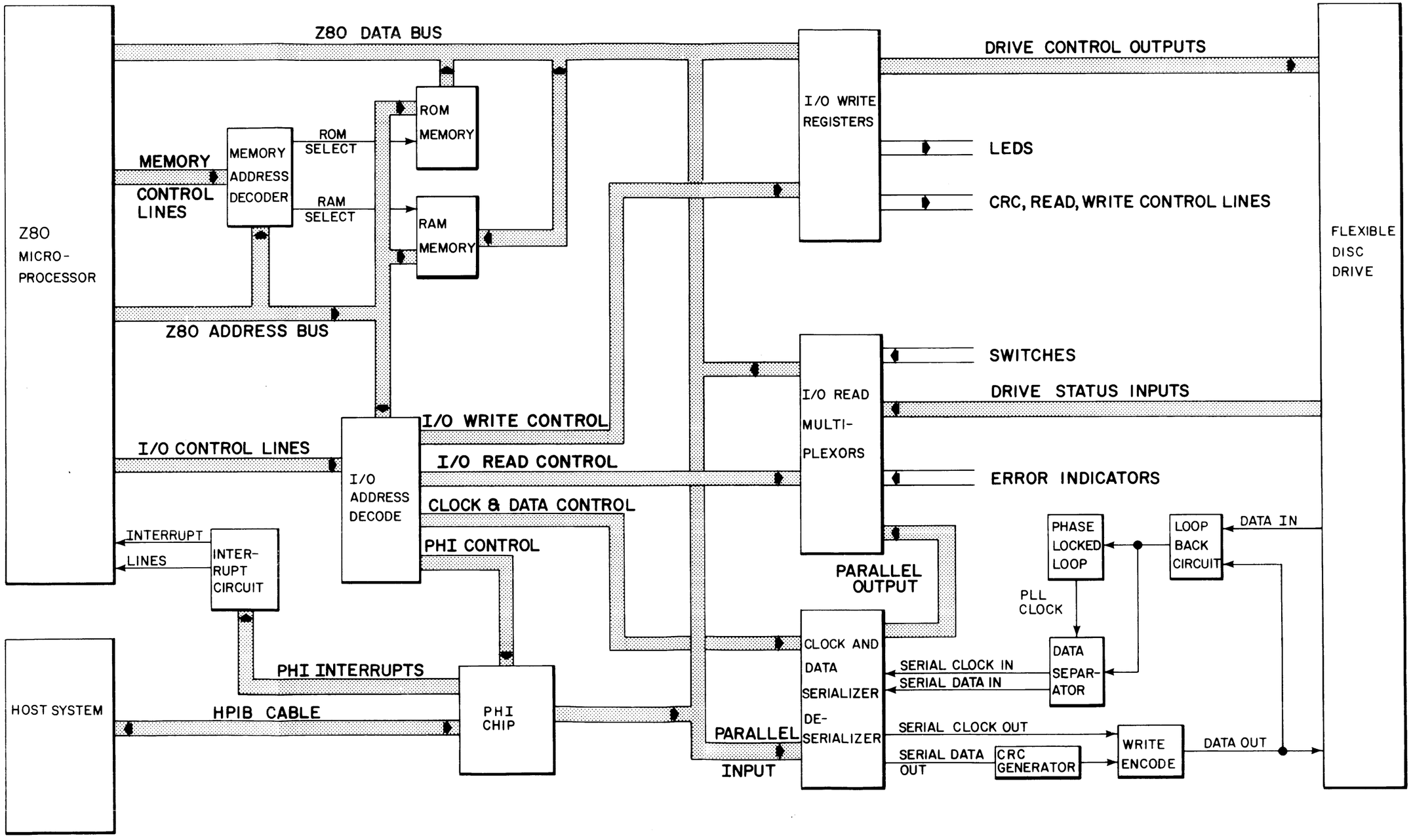


Figure 3-2. Controller A1 (07902-66510/66520/66501) Block Diagram

Read Operation

When the Z80A receives a command from the HP-IB to read a sector from the disc, it selects the specified drive, enables the drive to read, and enables the read electronics on the controller. The disc drive begins sending a pulse stream which represents the flux transitions on the disc. The phase locked loop synchronizes to the clock bits recorded with the data to generate a bit clock. The pulse stream is then clocked into the data separator circuit which separates the pulses into clock bits and data bits according to the recording format of the disc. The serial clock and data bits are then shifted into the SERDES shift registers and presented to the Z80A as two 8-bit parallel bytes. The Z80A then reads the I/O ports corresponding to the SERDES registers and stores the data in a RAM buffer. When a entire sector has been read and is stored in RAM buffer, the Z80A transfers the buffer to the host system via the HP-IB.

Write Operation

When the Z80A receives a write command from the HP-IB, it fills the RAM buffer with a sector of data from the HP-IB. It then enables the write electronics and writes eight bits of parallel data and eight bits of parallel clock to the SERDES. The SERDES changes the parallel clock and data bytes to serial bit streams which are input to the write encoder. The write encoder combines the clock and data bits into a single pulse stream according to the recording format of the disc. This pulse stream, which represents the flux transitions to be stored on the disc, is then sent to the disc drive.

Error Detection

Several types of errors are detected by electronics on the controller. These are CRC error, overrun error and margin error.

The Cyclic Redundancy Check (CRC) is two, 8-bit data bytes that are written on the disc with every sector. As the serial data is sent to the write encoder, it also goes to a CRC chip which computes the CRC for the data stream. After the last data byte is written on the disc, the two CRC bytes are written. When a sector is read back, the separated serial data, including the two CRC bytes, are again input to the CRC chip. The CRC bytes are computed such that when the data field and its CRC are input to the CRC chip, the chip can detect an error in the bit stream. After reading the data field, the Z80A checks a bit in the controller status register to see if a CRC error occurred. If so, the error is reported to the host system via HP-IB.

An overrun error occurs if the Z80A is not sending or receiving data fast enough to keep up with the bits coming off the disc. This is detected by a logic circuit on the controller. At the conclusion of the read or write operation, the Z80A checks a bit in the controller status register to see if an overrun occurred, and notifies the host system accordingly.

A margin error occus when a clock or data bit occurs too close to the edge of the clock or data window of the bit stream. This does not indicate that the data was read incorrectly, but only that the controller may not be able to read the sector in the future if the bits shift any further within the window. This error is checked by the Z80A following a read operation and reported to the host system only if the host system requests a verify or read operation.

Seek Operation

Before reading or writing a sector of data, the controller must position the read/write head of the disc drive over the desired sector. To do this, the controller sends signals to the disc drive to step the head to the desired track. The controller then begins to read the disc. Track and sector information is stored as a preamble to each sector, and the disc is formatted in a manner to allow the controller to detect the beginning of a preamble. On finding a preamble, the Z80A first checks that the track number is correct. If not, it will continue to step the head until the correct track is found. The sector number is then compared. If correct, the Z80A waits for the mark to indicate the beginning of the data field and then begin reading or writing the data field. If incorrect, it passes over this sector and looks for the next until it finds the desired sector. If it can't find the sector after two revolutions of the disc, an error condition is indicated to the host system.

In-Use LED Pattern List

When the controller is operating under the control of a mainframe, the LED display will indicate what function the controller is performing. The following list of LED patterns and controller functions is included as an aid in troubleshooting.

LED Pattern	The Controller is:
00010	waiting for a command and monitoring drive status.
00100	sending data to host system.
00110	receiving data from host system.
01000	determining status and format from requested unit.
01010	loading heads on a drive.
01100	waiting for a secondary HP-IB command.
01110	formatting a track.
1000	waiting for a command; last operation completed without error. DSJ = 0.
10010	waiting for a command;lst operation completed with error. DSJ = 1.
10100	waiting for a command; power-on holdoff is active. DSJ = 2.
10110	waiting for a command; parity error was enabled and detected on last command. DSJ =3.
11000	executing VERIFY command.
11010	moving the heads one track.
11100	writing a sector.
11110	reading a sector.

Note that if the right-hand LED is lit, the controller is not operating under the control of the mainframe. Refer to Table 3-1 for a list of error codes.

7902A System Self-tests

Introduction

This section decribes the system self-tests and provides a summary of the LED display patterns that indicate particular self-test failures. These self-tests are valid on controller boards 45000-66510 and 07902-60024.

WARNING

THE HP 7902A/C AND 9895K DISC DRIVES DO NOT CONTAIN OPERATOR SERVICEABLE PARTS. TO PREVENT ELECTRICAL SHOCK, REFER ALL TROUBLESHOOTING ACTIVITIES TO SERVICE-TRAINED PERSONNEL.

Self-Test Overview

Self-test is a firmware procedure which is implemented by the controller board to check it's functional operation. The self-tests can be initiated in the following three ways:

- Power On Sequence: At power on, the controller board executes a power on sequence that includes a self-test.
- Remote, Programmatically: The INITIATE SELF-TEST command can be executed over the HP-IB channel. Once initiated, the self-test will proceed until successfully completed or until a hard or soft error is detected.

NOTE

A hard error will prevent the controller from going on line; a soft error will allow the controller to go on line at the end of the self-test.

- Local, Manually: The user may execute the self-test by depressing the self-test switch located on the front of the controller board. See Figures 3-3 and 3-4 for the location of the switch and associated controls and indicators.

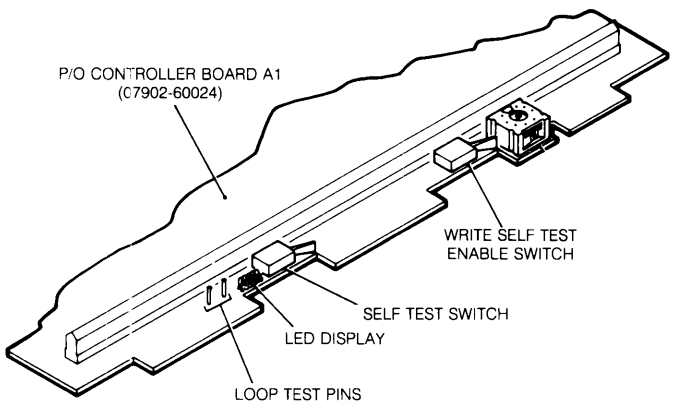


Figure 3-3. Controller Board A1 (07902-60024) Self-Test Controls and Indicators

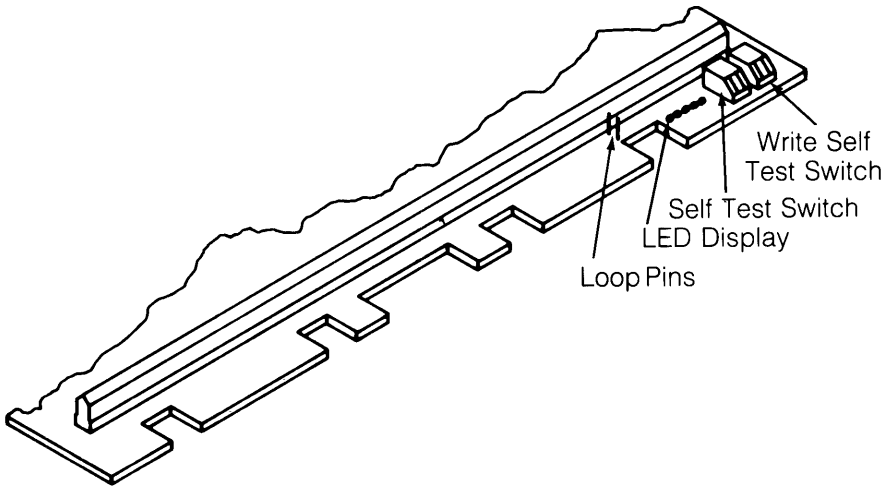


Figure 3-4. Controller Board A1 (45000-66510) Self-test Controls and Indicators

Manual Initiation of Self-Test

After power has been applied to the controller the self-test procedure can be initiated and controlled through the self-test switch, loop pin, and write test switch.

The self-test switch is mounted on the left or top side of the controller board next to the LED pack. To initiate the self-test, momentarily depress the switch. This should cause the LED pattern test to begin. After the self-test is initiated, the self-test switch function changes. The new function is dependent upon the state of the loop pins and write test switch.

The loop pins are the two test pins mounted to the immediate left of the LED pack. They are used to control the execution of self-test to loop on the failing test or on the entire test if there is no failure. Its function is dependent on the state of the self-test switch. The loop pins are termed "on" when the two pins are connected together and "off" when they are not.

The write test switch is mounted on the controller board next to the HP-IB device address switch. Tis switch is used to command the self-test to append the write and read tests after the normal self-test has been completed.

CAUTION

ALL DATA ON THE TEST CYLINDER WILL BE LOST WHEN THIS TEST IS PERFORMED. REMEMBER TO USE A BLANK DISC FOR THIS TEST.

Once the write test has begun the switch may be released.

Test Selection

There are three tests selectable in the manually invoked self-test, they are:

a. Default self-test,

b. Self-test with write/read test appended,
c. Self-test with read only test appended.

Default Self-Test

The default self-test is selected by momentarily depressing the self-test switch. Once self-test has started the self-test switch must be released. At this point one pass of the self-test procedure is executed then the controller will go on line. If an error is found self-test will pause for 20 seconds and display the number of the failing test in the LED's, then go on line. If no error is found self-test will pause for 10 seconds displaying the end-of-self-test number (00001) in the LED's then go on line. Connecting the loop pins will cause self-test to, if no error is found, continously repeat self-test, or if an error is found, to re-attempt the failing test until it passes.

Self-Test Switch	Loop Pins	No Error	Error
off	off	One pass of the default test, then go online.	Pause 20 displaying error number, then online.
off	on	Repeat self-test until loop pin removed. No pause after pass complete.	Pause, then repeat failing test until it passes.
on	off	— Defines read only self-test —	
on	on	— Defines read only self-test —	

Write/Read Self-Test

The self-test with the write/read test appended is selected by holding the write test enable switch in while depressing the self-test switch. Caution: this test will destroy data and format the test cylinder. If the self-test switch is released, one pass of the write test procedure is executed. If the self-test switch is held in, self-test will repeat, stepping in one cylinder each pass, until an error is found and then pause until the self-test switch is released. Once the self-test switch is released the controller will go online. Connecting the loop pins (''on'') will cause self-test, if no error is found, to repeat the self-test with the write and read test appended after stepping in one cylinder. If an error is found self-test will display the test number and, if the self-test switch is depressed, stop until the self-test switch is released, else, loop on the failing test until it passes.

Write/Read Self-Test

Self-Test Switch	Loop Pin	No Error	Error
off	off	One pass of write/ read self-test, pause 10 seconds, then go online.	Pause 20 seconds with error number in LED's, then go online.

off	on	After one pass, step in one cylinder and repeat write/ read test. No pause after pass.	Pause, then repeat failing test until it display error number.

Read Only Test

The self-test with the read only test appended is selected by depressing and holding the self-test switch in. Note: This test will read the test cylinder (either single or double sided disc) checking for all errors associated with the read operation. Holding the self-test switch in cause self-test to loop, stepping the head in one cylinder each pass, reading a cylinder. If no error is found, self-test will continue to loop, if an error is found, self-test will stop and wait for the self-test switch to be released. If the loop pins are connected and no error is found, self-test will loop faster, if an error is found, self will repeat the failing test until it passes.

Self-Test Switch	**Loop Pins**	**No Error**	**Error**
off	off		— Default self-test —
off	on	— Default self-test —	
on	off	Repeat complete read only self-test. Pause after pass complete.	Stop until self-test switch is released, display error number.
on	on	Repeat complete read only self-test. No pause after pass complete	Repeat failing test until it passes.

Self-Test Error Explanations

This section describes how to interpret the results of the self-test procedure from either the Return Self-Test Results command or from the LED's mounted on the 7902 controller board. Self-test is broken into steps called tests and subtest. Each test and subtest has an associated number returned and displayed when an error is encountered during the execution of that step. Both the test and subtest numbers can be read with the Return Self-Test Results command, while only the test number is displayed in the LED's on the controller board.

NOTE

ET #12309 will allow the operator to display the complete 16 bits of self-test resuls from the controller board.

The two bytes read in the Return Self-Test Results command have the following format:

EHUUFSSS SSSTTTTA

The 5 LED's mounted on the 7902 controller board are interpreted during self-test as the following:

ABCD*	Label on controller board stiffener
ooooo	LED polypack
TTTTA	Test number

Where:

E	ERROR INDICATOR. On if an error was encountered, else off.
H	HEAD NUMBER. Indicates which head the read or write test failed on.
UU	UNIT NUMBER. Indicates which unit or drive the controller and selected at the time of the failure.
F	FORMAT of OPERATION. Indicates if the controller was in the IBM (0) or HP (1) mode when the test failed.
SSS SSS	SUBTEST NUMBER. Indicates which subtest of the current test failed.
TTTT	TEST NUMBER. Indicates which test failed.
A	"*" LED. This LED is on (lit) only when the controller is performing self-test. When off, the controller is on line and ready to accept HP-IB commands.

If there is no error detected, the two bytes returned in "Return Self Test Results" are zero, and a "00001" is displayed on the controller board LED's.

If an error is encountered, the error number is displayed on the LED's and is made available for the "Return Self Test Results" command. The following is an explanation of the possible failing tests. If viewed from the LED's only the current test can be determined and the reasons for the failure could be any one of the subtests.

Table 3-1. Error Codes

Test Number	Subtest Number	Error Explanation	Corrective Action
0000		**End of self-test**. Self-test passed with no errors.	Replace controller board
0001		ROM Checksum Test 1	"
	000 000	ROM Checksum Test 1	"
	000 001	ROM Checksum Test 1	"
	000 010	ROM Checksum Test 1	"
	000 011	ROM Checksum Test 1	"
0010		ROM Checksum Test 2	Replace controller board
	000 000	ROM Checksum Test 2	"
	000 001	ROM Checksum Test 2	"
	000 010	ROM Checksum Test 2	"
	000 011	ROM Checksum Test 2	"
0011		ROM Checksum Test 3	Replace controller board
	000 000	ROM Checksum Test 3	"

	000 001	ROM Checksum Test 3	"
	000 010	ROM Checksum Test 3	"
	000 011	ROM Checksum Test 3	"
0100		ROM Checksum Test 4	Replace controller board
	000 000	ROM Checksum Test 4	"
	000 001	ROM Checksum Test 4	"
	000 010	ROM Checksum Test 4	"
	000 011	ROM Checksum Test 4	"
0101		RAM Test 1	Replace controller board
0110		RAM Test 2	Replace controller board
0111		PHI Chip Test	Replace controller board
1000		Overrun/Timeout logic test	Replace controller board
	000 000	Timeout indicated but not expected.	"
	000 001	Timeout expected but not indicated.	"
	000 010	Overrun indicated but not expected.	"
	000 011	Overrun expected but not indicated.	"
1001		DLoop/Mark detect or margin error.	Replace controller board
	000 000	**DLoop IBM Mode**. Data received was not what was expected.	"
	000 001	**DLoop IBM Mode**. Clockpattern received was not what was expected.	"
	000 010	**DLoop HP Mode**. Data pattern received was not what was expected.	"
	000 011	**DLoop HP Mode**. Clockpattern received was not what was expected.	"
	000 100	**Address Mark Detect**. Address mark indicated but not expected.	"
	000 101	Address Mark Detect. Address mark expected but not indicated.	"
	000 110	**Margin Error**. Margin error indicated but not expected.	"
	000 111	**Margin Error**. Margin error expected but not indicated.	"
1010		CRC logic error	Replace controller board
	000 000	CRC error expected but not indicated.	"
	000 001	**CRC DLoop**. CRC value not the expected value.	"
	000 010	CRC error indicated but not expected.	"
1011		Drive Board Test	Replace drive assembly
	000 000	**Illegal Drive Status**. Spinning is indicated but not ready.	"
	000 0001	**Head Delay**. The failure of this subtest indicates a problem with the head and phase load delay logic. The condition being that there was no delay, or that the delay was less then .5 seconds.	"

	000 010	**Head Delay**. The failure of this subtest indicates a problem with the head and phase load delay logic. The condition being that the delay was longer than 2.25 seconds.	"
	000 011	**Seek**. The failure of this subtest indicates a problem in the seek logic. The condition being that after 100 steps toward track 0 there was no track 0 indicator found.	"
	000 100	**Track 0 Indicator**. The failure of this test indicates a problem with the track 0 indicator logic. The condition being that the track 0 indicator was on at a phase other then phase 0 when the actuator was being stepped out.	"
	000 101	**Seek**. The failure of this subtest indicates a problem with the seek logic. The condition being that the track 0 indicator was on when not expected as the actuator was being stepped in.	"
	000 110	**Seek**. The failure of this subtest indicates a problem with the seek logic. The condition being that the track 0 indicator was not on when expected.	" "
	000 111	**No Drives**. The failure of this test indicates that no drives were found connected to the controller. This may or may not be an error.	
1100		**Drive Test**. Note: This test will only be performed if there is a disc present in the drive.	Replace drive assembly
	000 000	**No Index Mark**. The failure of this test indicates that the drive, through status, indicated that a diskette was present and spinning, but, no index mark was found	"
	000 001	**Speed**. This subtest indicates that the diskette was spinning faster then specified limits.	"
	000 010	**Speed**. This subtest indicates that the diskette was spinning slower then specified limits.	"
	000 011	**Speed (IBM)**. This subtest indicates that the diskette was spinning faster than specification allows in IBM format.	"
	000 100	**Speed (IBM)**. This subtest indicates that the diskette was spinning slower than specification allows in IBM format.	"
1101		**Write Test**. The failure of this test indicates a problem with recording data formatting the disc in the indicated drive.	"
	000 000	**Not Ready**. The failure of this subtest indicates that the selected drive is not ready. A drive with a single sided diskette could cause this error.	"
	000 001	**No Diskette**. This test would fail if the selected drive indicated that there was no diskette inserted in the drive or that the door is not closed.	"
	000 010	**Write Protected**. The failure of this test indicates that the status from the selected drive shows the diskette as write protected.	"

1110		**Read Test**. The failure in this test indicates a problem in reading data from the disc. This may result in a failure to write or read correctly or bad media.	Replace drive assembly
	000 000	**Not Ready**. The failure of this subtest indicates that the selected drive is not ready. i.e., maybe the diskette has been removed.	"
	000 001	**Bad ID Field**. The failure of this subtest indicates that current ID field contained misinformation.	
	000 010	**No ID Fields Found**. The failure of this subset indicates that no ID fields were found after 2 revolutions of the diskette.	"
	000 011	**Wrong ID Field**. The failure of this subtest indicates that during the current read, some ID fields were found but the target ID field was not.	"
	000 100	**No Data Mark**. The failure of this subtest indicates that during the current read, the target ID field was found but the corresponding data mark was not found.	"
	000 101	**CRC Error**. The failure of this subtest indicates that the current data fild contained a CRC error.	"
	000 110	**Overrun**. The failure of this subtest indicates that an overrun error occured in the current read attempt.	
	000 111	**Data Miscompare**. The failure of this test indicates that the status indicates a "good" read but the read data does not compare with the expected value.	"
	001 000	**Seek Not Ready**. This failure indicates that the drive is not ready during the logical seek opera tion. This subtest is only executed if the read only test is selected.	Replace controller board
	001 001	**Unknown Format**. This test is only executed during the read only self test. Its failure indicates that the controller is unable to determine the format of the diskette in the indicated drive.	"
	001 010	**Seek Failure**. The failure of this subtest indicates that the logical seek algorithim could not find the target track.	"
1111		**SLP Failure**. The failure of this test indicates a problem with the MCC, PHI or RAM logic.	Replace controller board
	000 000	**Initialization**. This is the first test executed by the controller. It is not a rest in the true sense but only an attempt to change the LEDs to signal the operator that the self-test procedure has begun.	"
	000 001	**Processor Fault**. The failure of this test indicates that the MCC or ROM memory self-test are not working correctly.	"
	000 010	SLP Fault. The failure of this subtest indicates that either the MCC, ROM or RAM are not working correctly.	"

7902C and 9895K System Self-Tests

This section contains information pertaining to the diagnosis of problems using the 09895-66506 Status Display Board. These tests are valid on controller boards P/N 07902-66510, 07902-66520 and 07902-66501.

General Description of Diagnosis Method

The Controller contains 2 kbytes of code dedicated to a self-exercise of the drive system to verify its correct operation. The self-exercise is designed to halt at any failure. Fortunately, status of the self-test can be monitored at 15 bits of data. Ten bits indicate which test and subtest are being performed, and the other five contain miscellaneous information such as format being used. When a halt occurs, the ten bits may be read as an error code, and the problem narrowed down to a smaller area. The next few sections detail how to initiate the self-exercise, how to use the Status Display Board to obtain the error code and how to translate the error code into a specific problem area.

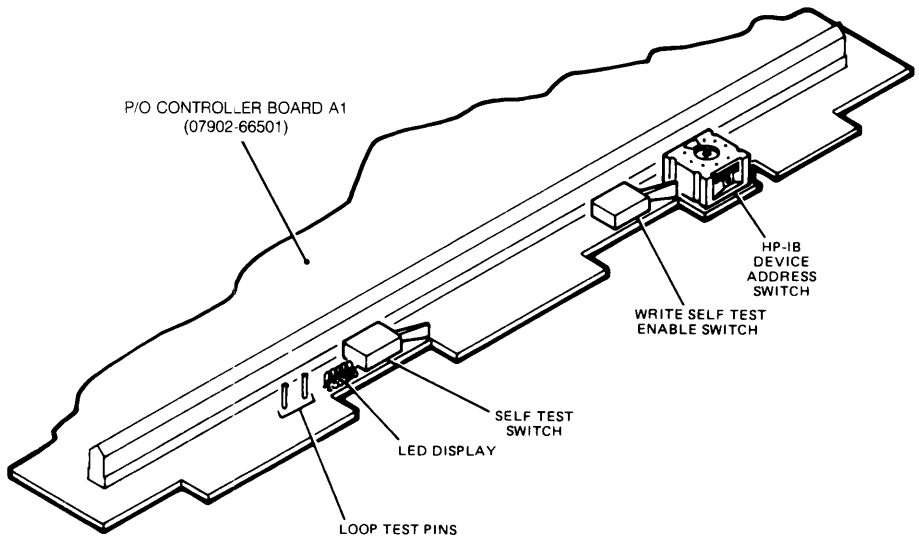


Figure 3-5. Controller Board A1 (07902-66501) Self-Test Controls and Indicators

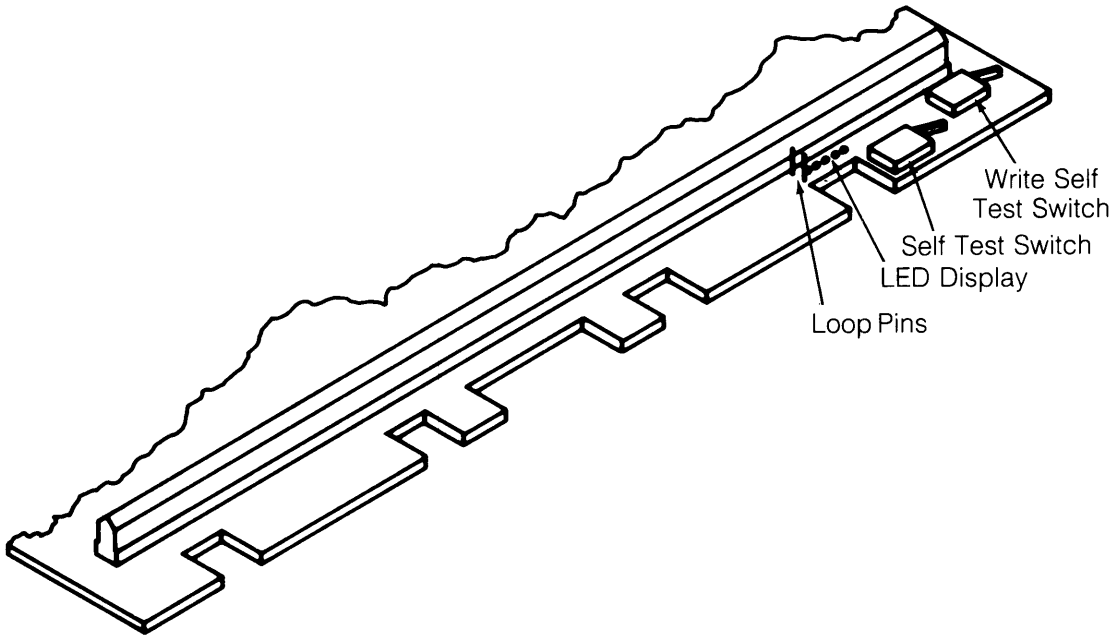


Figure 3-6. Controller Board A1 (07902-66510/66520)
Self Test Controls and Indicators

Self-Test Initiation

The basic self-test may be initiated in any of three ways:

1. By turning the power on,
2. From the host system by means of the disc memory command set,
3. By pressing the self-test switch.

Turning the disc drive on automatically initiates the start-up sequence which includes self-test. Note that the basic self-test doesn't contain any read or write functions; therefore, a disc need not be installed in any drive.

Using the command set from the controller is by far the best way to initiate self-test, since the command set can also be used to display the results on any chosen medium.

In order to allow the disc drive to self-test without being connected to other devices, self-test input/output hardware was added to the front of the controller board. The self-test switch is pressed to start the self-test routine. The read/write self-test switch is used to enable the read/write functions detailed in the next section. The loop pins are used to enable the repeat function detailed in the next section. The right-most LED indicates that the controller is busy doing self-test. The four left-most LED's display the number of the test being run. If the routine halts on any test, the LED display may be read as an error code (see Table 3-4).

Test Selection

There are three classes of tests selectable in the manually-invoked self-test. There are:

1. Default self-test,
2. Read-only self-test,
3. Write/read self-test.

Default Self-Test

The default self-test is selected by momentarily depressing the self-test switch.

Loop Pins	Self-Test Switch	Function
Open	Released	Perform standard self-test only and then go on-line. If soft error occus, pause 20 seconds before going on-line.
Closed	Released	Perform standard self-test repetitively. If soft error occurs, pause 20 seconds before repeating.

Read-Only Self-Test

The read-only self-test is selected by pressing and holding the self-test switch.

Loop Pins	Self-Test Switch	Function
Open	Held	Perform read-only test on incrementing tracks with .5 second delay between increments. If error occurs, wait for release of self-test switch before going on-line.
Closed	Held	Perform ready-only test on incrementing tracks with no wait between increments. If error occurs, pause .2 second before repeating failed test.

Write/Read Self-Test

Write/read self-test is selected by holding the write enable switch in while pressing the self-test switch. If the write enable switch is held in during execution of the test, the read after write is performed with reduced margins.

Loop Pins	Self-Test Switch	Function
Open	Released	Perform write/read test on track 0 and then go on-line. If error occurs, pause 20 seconds before going on-line.
Open	Held	Perform write/read test on incrementing tracks with .5 second dely between increments. If error occurs, wait for release of self-test switch before going on-line.
Closed	Released	Perform write/read test on incrementing tracks with no wait between increments. If error occurs, pause 20 seconds before continuing test.
Closed	Held	Perform write/read test on incrementing tracks with no wait between increments. If error occurs, pause .2 second before repeating failed test.

Using the Status Display Board for Failure Analysis

Although the four digits displayed on the LEDs can narrow the problem down to a small area, there is much more information available. It can be read by the controller using the disc memory command set. It is also available at connector J2. The module is designed to fit on this connector and present this information as an LED display. To use the module, follow this procedure:

1. With the power turned off, remove all interconnecting cables.
2. Locate connector J2. Slide the module onto this connector, component side up.
3. Hook the +5V clip onto the +5V pin. If the +5V pin is missing, +5V is available at the top of the LED display.
4. Turn power on. The start-up sequence includes the basic self-test.
5. After the self-test has finished running (that is, the LED pattern has stopped changing), press and release the self-test switch.
6. The basic self-test should now occur. When it has finished running, put an initialized scratch disc in each drive and close the doors.
7. Pressing and releasing the read/write enable switch and hold it in until after pressing the self-test switch. The basic self-test with read/write should now occur.
8. To make self-test repeat, short loop pins together.

Self-test information can be read directly from the LED's, using the methods presented in the next section.

Obtaining Test Results from LED Display

The two pieces of information which we are interested in are the four-bit test number and the five-bit subtest number. The test number appears as four red LED's labeled TEST. The MSB is nearest the controller board. The subtest number appears as five green LED's labeled SUB-TEST. These two numbers are listed in Table 3-5, along with the meaning of the code. Note that only nine of ten error code bits are used. The tenth digit is always zero, as can be seen by using the controller and command set, which present all ten bits.

Table 3-2. LED Display

ERR	Turns on when error is detected.
HEAD	Off for head 0, on for head 1.
UNIT	Unit number of drive being tested (in binary).
HPFMT	Off for IBM format, on for HP format.
TEST	indicates number of test being performed.
SUBTEST	Indicates number of subtest being performed.
DONE	Indicates board is functioning. Test has completed if only this LED is on.
UNIT 0 ERR	Counts number of errors found in drive unit 0.
UNIT 1 ERR	Counts number of errors found in drive unit 1.

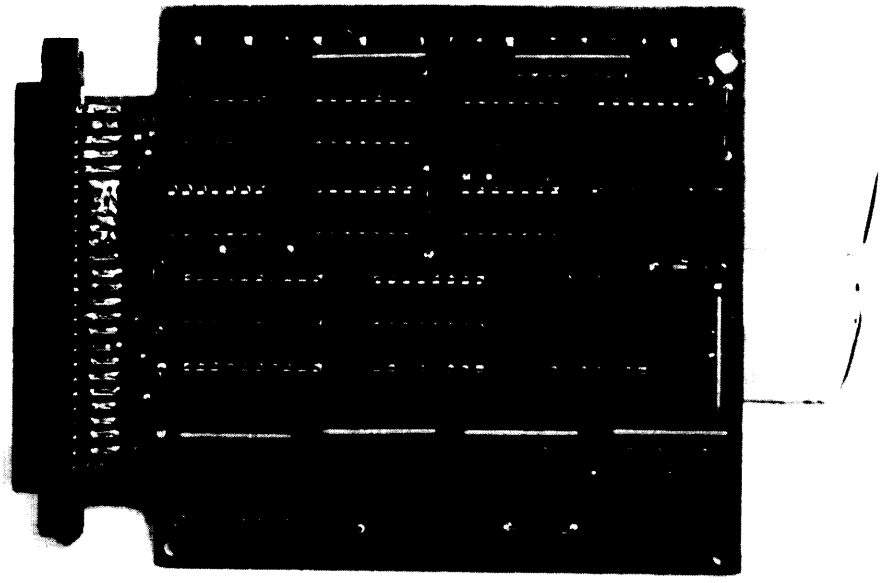


Figure 3-7. 09895-66506 Status Display Board

Error Rate Testing with the Status Display Board

The Status Display Board can be used for error rate testing of up to two drives at a time. It counts the number of passes of the selected self-test, and counts errors separately for each drive. This is the procedure:

1. Attach a jumper between the loop pins.
2. Put a disc with no defective tracks in each drive, and close the door.
3. Turn the power on.
4. Press the write enable switch and hold it in while pressing the self-test switch. Hold the self-test switch in with an insulated clip. The write/read test will now run continuously.
5. The HP bit error rate standard is no more than one error in 10^9 bits. 7862 passes are the equivalent of 10^9 bits. A drive would pass if it has no more than five errors in 39,308 passes. A problem arises in that the pass counter only counts to 9999 and then re-sets. This problem may be circumvented in one of two ways. Put the system into operation and allow it to run for an hour or two. If errors have accumulated, the drive is defective. To prove that a drive is good, determine the length of time the system takes to make a countable number of passes, say 3,000 or 10,000 and then calculate how long 39,308 would take. Allow the system to run for that length of time, and stop when the counter reads 9308. If no more than five errors have accumulated on a drive, it is a good drive.
6. Note that the self-test routine cannot determine whether a track is good or bad, but attempts to write on every track. If errors appear to occur at the same point on the disc, there is probably a defective track at that point.

Table 3-3. Error Codes

Test Number	Subtest Number	Error Explanation	Corrective Action
0001	00000	ROM checksum Test: This test sums the contents of the ROM and compares it to the checksum value stored in the ROM.	Replace controller board
0100	00000	RAM Addressing Test: This test writes patterns to the RAM memory which will verify that the RAM is being addressed correctly.	Replace controller board
		RAM Pattern Tests: These tests write to the RAM and then rea back and compare	
0110	00000	Indicates a failure in the upper four bits.	Replace controller board
0111	00000	PHI Test: This test exercises the internal opera tions of the PHI chip.	Replace controller board
		Time-Out Bit Test: These subtests measure the pulse of the time-out one-shot and test for re-triggerability.	
1000	00000	Time-out is high when it should be low.	Replace controller board
	00001	Time out is low when it should be high.	Replace controller board
		Overrun Bit Test: These subtests verify functioning of the overrun circuit — ability to reset the overrun bit and ability of circuit to detect an overrun condition.	
	00010	Overrun is high when it should be low.	Replace controller board
	00011	Overrun is low when it should be high.	Replace controller board
1001		IBM Data Loop Test: These subtests exercise the data loop in IBM format mode. A pattern is written to the clock and data registers; it loops through the serializer, write encoder, data separator and deserializer, and is read back from the clock and data registers.	Replace controller board
	00000	Error in clock byte read.	Replace controller board
	00001	Error in data byte read.	Replace controller board
	00010	HP Data Loop Test: Exactly the same as the	Replace controller board
	00011	IBM Data Loop Test except that it runs in HP format mode.	Replace controller board
		Address Mark Test: These subtest check the address mark detect circuit.	
	00100	Address mark detect is on when it should be off.	Replace controller board
	00101	Address mark detect is off when it should be on.	Replace controller board
		Margin Error Test: These subtests check the margin error detect circuit.	
	00110	Margin error is on when it should be off.	Replace controller board
	00111	Margin error is off when it should be on.	Replace controller board

1010		CRC Test: This test exercise the cyclic redundancy check generator. it tests ability to detect a CRC error and to generate the correct CRC for a specific data pattern.	Replace controller board
	00000	CRC ERR is off when it should be on.	Replace controller board
	000011	Wrong CRC bytes were generated.	Replace controller board
	00010	CRC ERR is on when it should be off.	Replace controller board
1011		Re-calibrate/Seek Test: This test attemps to select each drive, re-calibrate the drive, step in to track 76 and step out to track 0.	Replace drive assembly
	00100	Track 0 indicator came on while stepping in to track 76.	Replace drive assembly
	00101	Track 0 indicator came on while steppong out to track 0.	Replace drive assembly
	00110	Track 0 indicator did not come on when it should have.	Replace drive assembly
	00111	No drives were found attached to the controller. or a drive failed to re-calibrate.	Replace drive assembly
1100		Rotational Timing Test: This test measures the time for revolution of the disc and compares it to the specification.	Replace drive assembly
	00000	No index mark was found.	Replace drive assembly
	00001	Disc is spinning too fast.	Replace drive assembly
	00010	Disc is spinning too slow.	Replace drive assembly
1101		Write Test: This test formats a track in both HP and IBM formats and reads back what was written.	Replace drive assembly
	00000	Drive went not ready during format.	Replace drive assembly
	00001	No disc in the drive.	Replace drive assembly
	00010	Disc is write-protected.	Replace drive assembly
1110		Read Test: This test reads a track on the disc. It may be part of the write/read test or it may be a ready-only test, depending on switch settings.	Replace drive assembly
		Subtest common to both write/read and read-only tests.	
	00000	Drive went not ready.	
	00001	Head, track or format information written in the ID field is incorrect.	
	00010	No ID fields were found.	Replace controller board
	00011	Current sector was not found	Replace controller board
	00100	Data mark for the desired sector was not found.	Replace controller board
	00101	CRC error occured.	Replace controller board
	00110	Overrun error occured.	Replace drive assembly
		Subsets in write/read test only.	
	00111	Data read back not the same as what was written.	Replace controller board

	01000	Margin error occured.	Replace controller board
	10000	Drive went not ready while seeking to the desired track.	Replace drive assembly
	10001	Unknown format.	Replace controller board
	10010	Seek to desired track failed.	
	10011	No disc in the drive.	Replace drive assembly
1111		Processor Test: This test exercise the op erations of the processor.	Replace controller board
	00001	Problem with the internal functions of the processor — branching, register arithmetic and logic functions.	Replace controller board
	00010	Problem with functions with access the RAM- read and write of RAM, stack operations and indexed and indirect addressing of RAM.	Replace controller board

Controller Board Assembly (P/N 45000-66510)

Introduction

This section provides operation interface information, schematic diagrams and replaceable parts list for controller board P/N 45000-66510.

Interface Information

Refer to Figure 3-8 for the connector locations. Table 3-8 describes the connector pin assignments.

Table 3-4. 45000-66510 Connector Pin Assignments

J3			
PIN	**SIGNAL**	**PIN**	**SIGNAL**
1	GND	A	CWRITE
2	CFETCH	B	CPON
3	CINT	C	CIAK
4	N.C.	D	CGNI
5	CIOG0	E	CIO END
6	CMG0	F	CMEND
7	GND	H	CIDLE
8	CA14	J	CA15
9	CA12	K	CA13
10	CA10	L	CA11
11	CA8	M	CA9
12	CA6	N	CA7
13	CA4	P	CA5
14	CA2	R	CA3
15	CA0	S	CA1
16	GND	T	GND
17	CDI	U	CD1
18	CD3	V	CD2

19	CD5	W	CD4
20	CD7	X	CD6
21	CD9	Y	CD8
22	CD11	Z	CD10
23	CD13	AA	CD12
24	CD15	BB	CD14
25	CLK 250	CC	GND

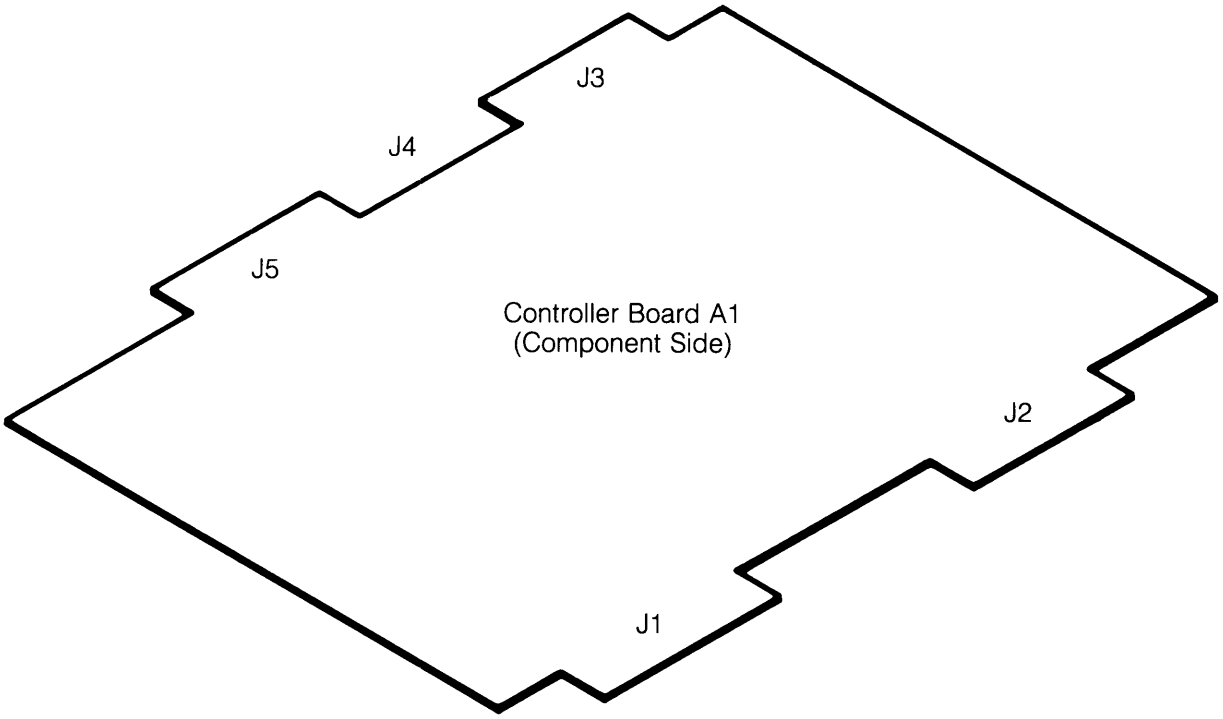


Figure 3-8. Controller Board A1 (45000-66510) Connectors

J5

PIN	SIGNAL	PIN	SIGNAL
1	LWPRT	A	PON
2	HREDY	B	LTRK0
3	LSPIN	C	N.C.
4	LINDX	D	HR SPIN
5	LDRLK	E	N.C.
6	STPHA	F	LSTEN
7	LWRTON	H	N.C.
8	STPHB	J	LDSLV
9	HHEDI	K	N.C.
10	LLDCT	L	HDSL2
11	HDSL1	M	N.C.
12	HOSL0	N	N.C.
13	N.C.	P	N.C.

14	N.C.	R	N.C.
15	HDATA	S	LDATA
16	N.C.	T	N.C.
17	N.C.	U	N.C.
18	N.C.	V	N.C.
19	N.C.	W	N.C.
20	N.C.	X	N.C.
21	N.C.	Y	N.C.
22	N.C.	Z	N.C.
23	N.C.	AA	N.C.
24	N.C.	BB	N.C.
25	PONR	CC	N.C.

HP-IB Connector

J4

PIN	SIGNAL	PIN	SIGNAL
2	SPARE	20	DI08
4	ATN	22	DI07
6	SRQ	24	DI06
8	NDAC	26	DI05
10	NRFD	28	DI04
12	IFC	30	DI03
14	REN	32	DI02
16	DAV	34	DIO1
18	EOI		

1 to 33 Odd = GND

Schematic Diagrams

Introduction

This section contains the circuit diagrams for controller board P/N 45000-66510.

NOTE: *VALUES SELECTED IN TEST

CLAMP
8MHZ
LCKUP
HIDEN
HIDEN
RDATA
DREAD
DWRITE
WRTCLK
PLLIN
W1
W2
W3
RAMP
PLL CLK
RECLAMP
RECLAMP
TRANS
XMGN
SERIAL CLOCK IN
SCLKIN
SERIAL DATA IN
SDATIN
BITCLK
BITCLK

U57 U77 U78 U79 U80 U81 U82 U2 U13 U41 U60 U61 U62 U69 U70 U71 U72 U73 U58 U59
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8 Q9 Q10 Q11 Q12 Q13 Q14 Q15
CR1 CR2 CR3 CR4 CR5 CR6 CR7 CR8 CR9 CR10 CR11 CR12 CR13 CR14 CR15
L1 2000μH
RP4-7 RP4-8 RP2-6 RP4-6

Figure 3-9. Controller Board A1 (45000-66510) Schematic Diagrams (Sheet 1)

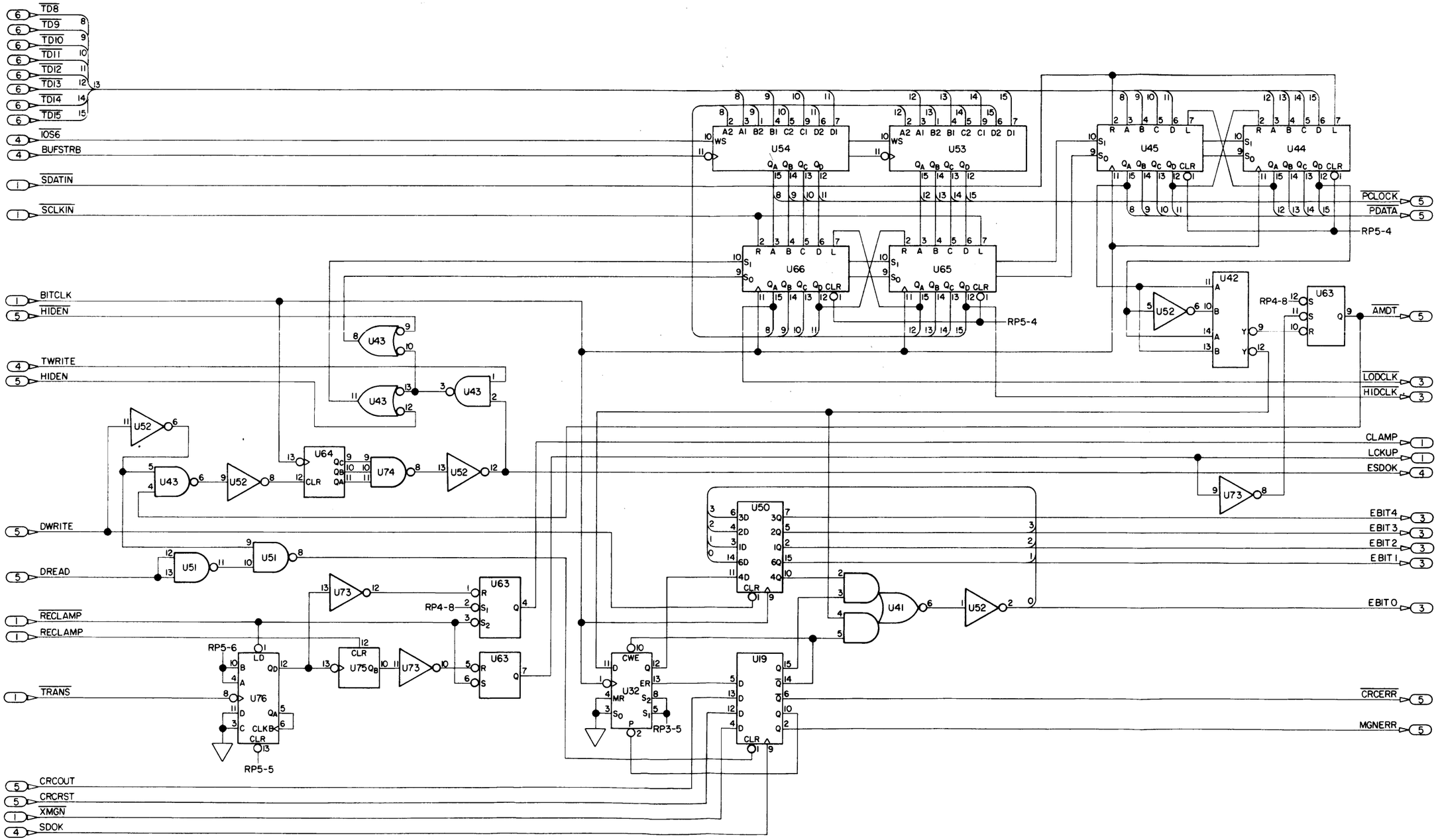


Figure 3-9. Controller Board A1 (45000-66510) Schematic Diagrams (Sheet 2)

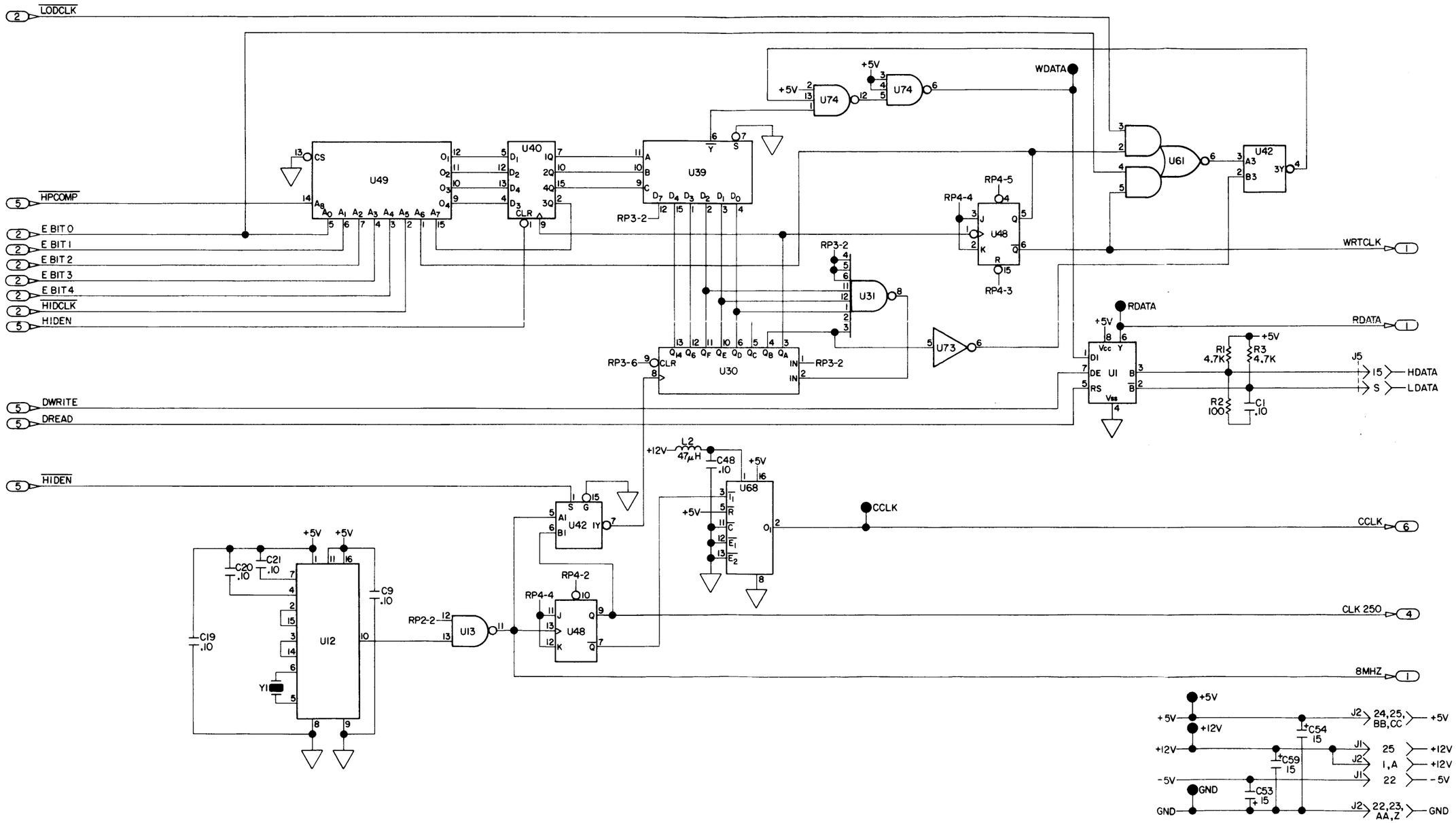


Figure 3-9. Controller Board A1 (45000-66510) Schematic Diagrams (Sheet 3)

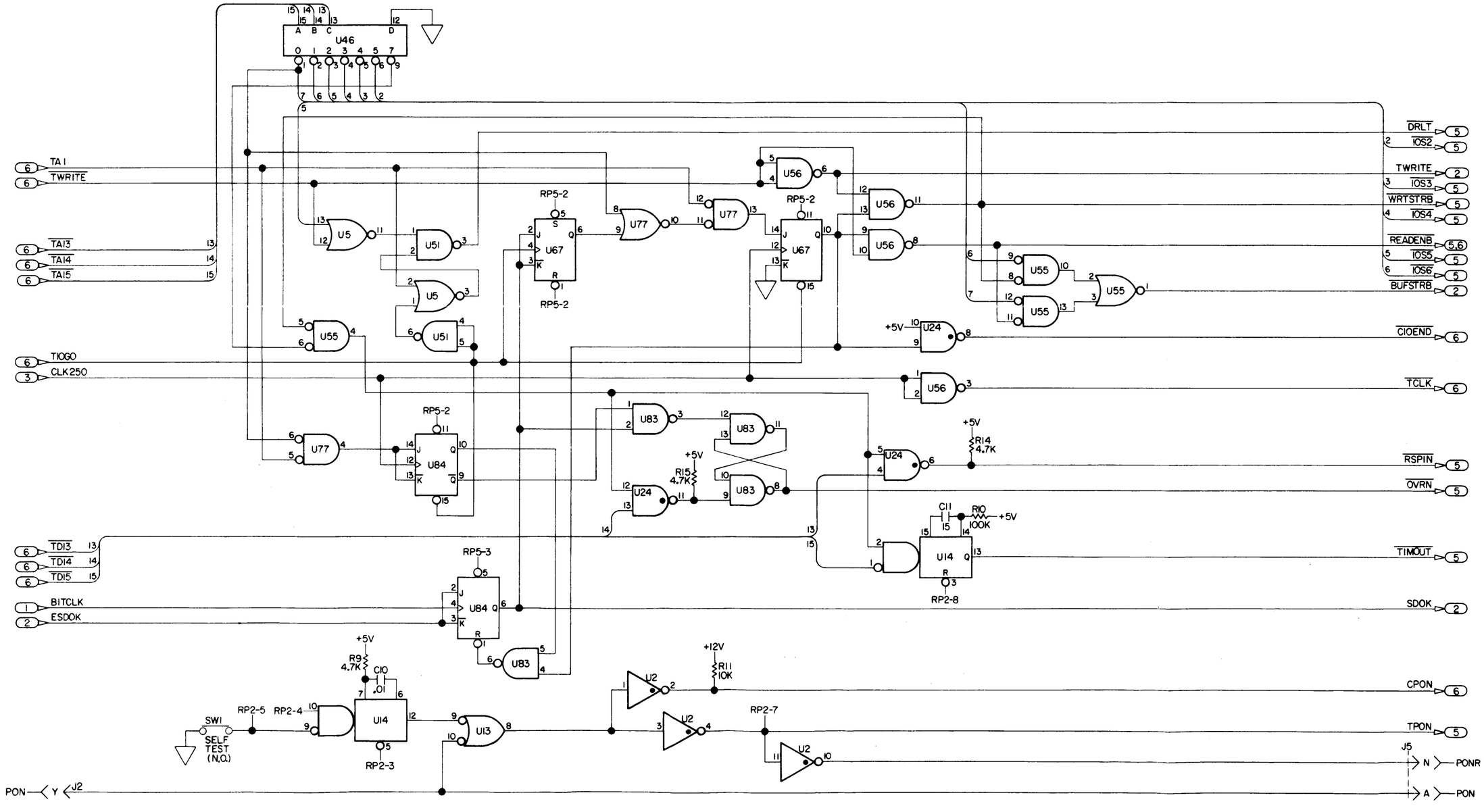


Figure 3-9. Controller Board A1 (45000-66510) Schematic Diagrams (Sheet 4)

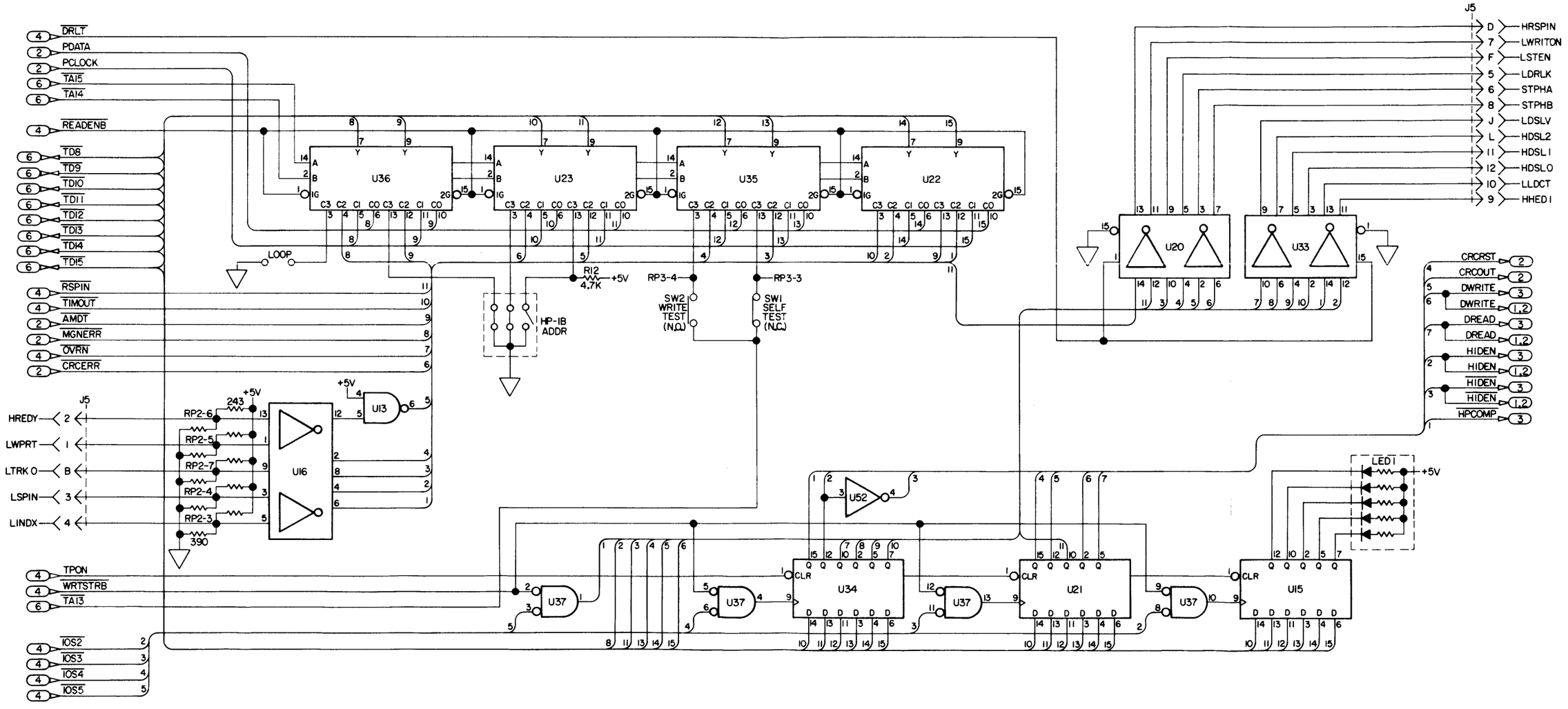


Figure 3-9. Controller Board A1 (45000-66510) Schematic Diagrams (Sheet 5)

Figure 3-9. Controller Board A1 (45000-66510) Schematic Diagrams (Sheet 6)

Replaceable Parts

Introduction

The controller board P/N 45000-66510 parts list is provided in this section. The total quantity of a part is shown only the first time it is used on this assembly.

The number shown in the "CD" column is the part check digit. Include the check digit number with the part number when ordering a part from HP.

Reference designators are listed in alphanumeric order in lieu of item numbers for printed circuit assembly parts.

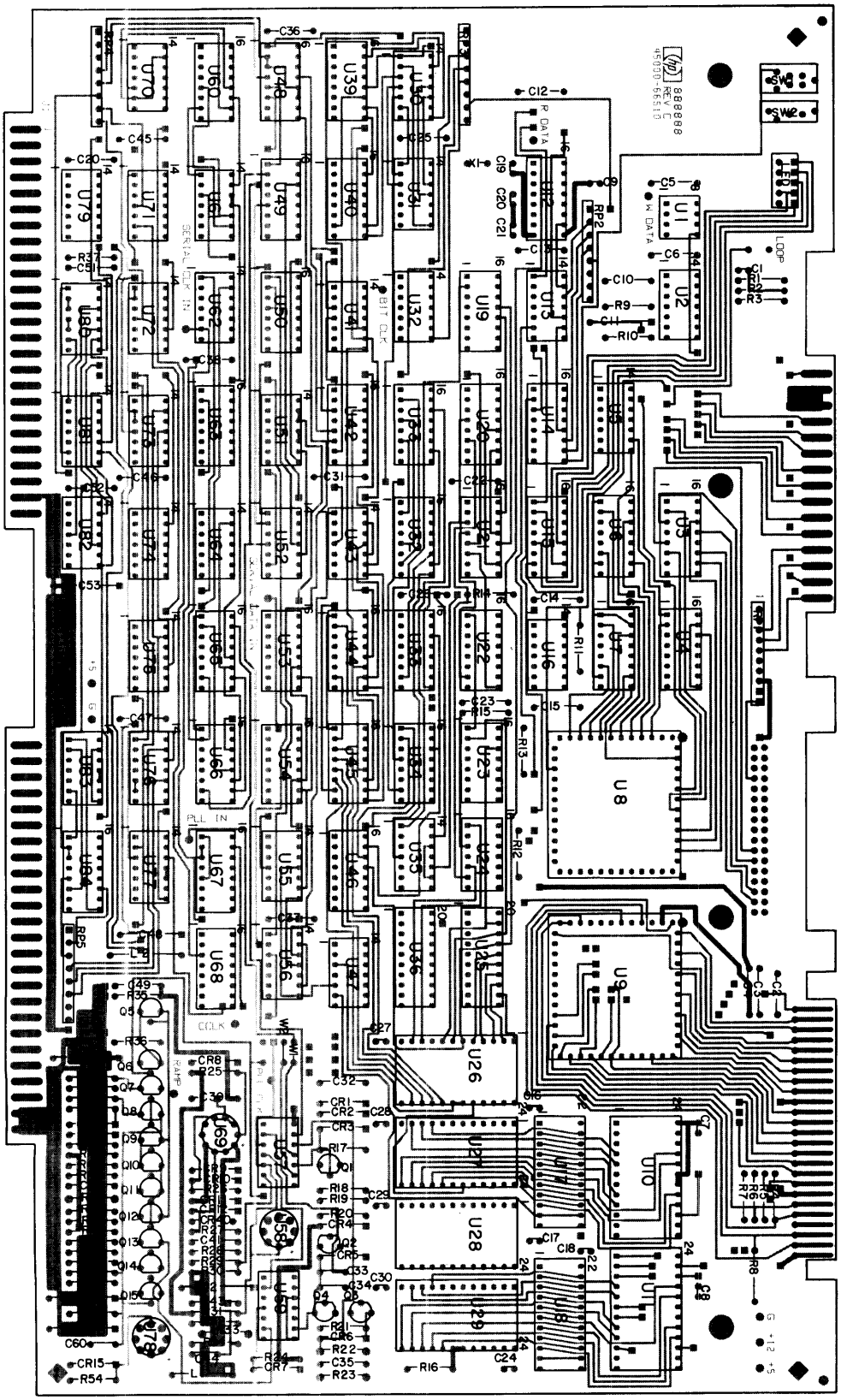


Figure 3-10. Controller Board A1 (45000-66510) Component Locator

Controller Board 45000-66510

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
C1	5	0160-0576	5	C-F:.1UF;50V
C2	2	0160-0127	2	C-F:1UF;25V
C3	9	0160-3847	32	C-F:.01UF;100V
C4	9	0160-3847		C-F:.01UF;100V
C5	9	0160-3847		C-F:.01UF;100V
C6	9	0160-3847		C-F:.01UF;100V
C7	7	0160-3879	10	C-F:.01UF;100V
C8	7	0160-3879		C-F:.01UF;100V
C9	5	0160-0576		C-F:.1UF;50V
C10	9	0160-3847		C-F:.01UF;100V
C11	5	0180-1746	5	C-F:15UF;20V
C12	9	0160-3847		C-F:.01UF;100V
C13	9	0160-3847		C-F:.01UF;100V
C14	9	0160-3847		C-F:.01UF;100V
C15	9	0160-3847		C-F:.01UF;100V
C16	7	0160-3879		C-F:.01UF;100V
C17	7	0160-3879		C-F:.01UF;100V
C18	7	0160-3879		C-F:.01UF;100V
C19	5	0160-0576		C-F:.1UF;50V
C20	5	0160-0576		C-F:.1UF;50V
C21	5	0160-0576		C-F:.1UF;50V
C22	9	0160-3847		C-F:.01UF;100V
C23	9	0160-3847		C-F:.01UF;100V
C24	7	0160-3879		C-F:.01UF;100V
C25	9	0160-3847		C-F:.01UF;100V
C26	9	0160-3847		C-F:.01UF;100V
C27	7	0160-3879		C-F:.01UF;100V
C28	7	0160-3879		C-F:.01UF;100V
C29	7	0160-3879		C-F:.01UF;100V
C30	7	0160-3879		C-F:.01UF;100V
C31	9	0160-3847		C-F:.01UF;100V
C32	9	0160-3847		C-F:.01UF;100V
C33	3	0160-2009	1	C-F:820PF;300V
C34	8	0160-0363	1	C-F:620PF;300V
C35	9	0160-3847		C-F:.01UF;100V
C36	9	0160-3847		C-F:.01UF;100V
C37	9	0160-3847		C-F:.01UF;100V
C38	9	0160-3847		C-F:.01UF;100V
C39	9	0160-3847		C-F:.01UF;100V
C40	2	0160-0127		C-F:1UF;25V
C41	9	0160-3847		C-F:.01UF;100V
C42	5	0180-1746		C-F:15UF;20V
C43	9	0160-3847		C-F:.01UF;100V
C44	4	0160-2307	1	C-F:47PF;300V
C45	9	0160-3847		C-F:.01UF;100V
C46	9	0160-3847		C-F:.01UF;100V
C47	9	0160-3847		C-F:.01UF;100V
C48	2	0180-1743	1	C-F:.1UF;35V
C49	9	0160-3847		C-F:.01UF;100V
C50	9	0160-3847		C-F:.01UF;100V
C51	9	0160-3847		C-F:.01UF;100V
C52	9	0160-3847		C-F:.01UF;100V
C53	5	0180-1746		C-F:15UF;20V
C54	5	0180-1746		C-F:15UF;20V
C55	9	0160-3847		C-F:.01UF;100V
C56	9	0160-3847		C-F:.01UF;100V
C57	9	0160-3847		C-F:.01UF;100V

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
C58	3	0160-0194	1	C-F:15000PF;200V
C59	5	0180-1746		C-F:15UF;20V
C60	7	0160-0362	1	C-F:510PF;300V
CR1	1	1901-0040	12	DIODE:SWITCHING
CR2	1	1901-0040		DIODE:SWITCHING
CR3	1	1901-0040		DIODE:SWITCHING
CR4	1	1901-0040		DIODE:SWITCHING
CR5	1	1901-0040		DIODE:SWITCHING
CR6	1	1901-0040		DIODE:SWITCHING
CR7	1	1901-0040		DIODE:SWITCHING
CR8	1	1901-0040		DIODE:SWITCHING
CR9	1	1901-0040		DIODE:SWITCHING
CR10	1	1901-0040		DIODE:SWITCHING
CR11	3	1902-3002	2	DIODE:ZENER;2.3V
CR12	3	1902-3002		DIODE:ZENER;2.3V
CR13	1	1901-0040		DIODE:SWITCHING
CR14	1	1901-0040		DIODE:SWITCHING
CR15	1	1902-3092	1	DIODE:ZENER;4.99V
CR16	5	1902-9622	1	DIODE:LED
J4	2	1251-5066	1	CONNECTOR:MALE;34 PIN
L1	7	9100-0541	1	COIL:250UH
L2	4	9100-1629	1	COIL:47UH
Q1	2	1854-0092	3	TRANSISTOR:2N3563
Q2	5	1853-0089	12	TRANSISTOR:2N4917
Q3	5	1853-0089		TRANSISTOR:2N4917
Q4	5	1853-0089		TRANSISTOR:2N4917
Q5	2	1854-0092		TRANSISTOR:2N3563
Q6	5	1853-0089		TRANSISTOR:2N4917
Q7	5	1853-0089		TRANSISTOR:2N4917
Q8	5	1853-0089		TRANSISTOR:2N4917
Q9	5	1853-0089		TRANSISTOR:2N4917
Q10	2	1854-0092		TRANSISTOR:2N3563
Q11	5	1853-0089		TRANSISTOR:2N4917
Q12	5	1853-0089		TRANSISTOR:2N4917
Q13	5	1853-0089		TRANSISTOR:2N4917
Q14	5	1853-0089		TRANSISTOR:2N4917
Q15	5	1853-0089		TRANSISTOR:2N4917
R1	2	0683-4725	7	R-F:4.7K OHM;5;.25W
R2	7	0683-1015	5	R-F:100 OHM;5;.25W
R3	2	0683-4725		R-F:4.7K OHM;5;.25W
R4	1	0683-1035	9	R-F:10K OHM;5;.25W
R5	1	0683-1035		R-F:10K OHM;5;.25W
R6	1	0683-1035		R-F:10K OHM;5;.25W
R7	1	0683-1035		R-F:10K OHM;5;.25W
R8	1	0683-1035		R-F:10K OHM;5;.25W
R9	2	0683-4725		R-F:4.7K OHM;5;.25W
R10	6	0757-0465	1	R-F:100K OHM;1;.125W
R11	1	0683-1035		R-F:10K OHM;5;.25W
R12	2	0683-4725		R-F:4.7K OHM;5;.25W
R13	8	0698-3136	1	R-F:17.8K OHM;1;.125W
R14	2	0683-4725	1	R-F:4.7K OHM;5;.25W
R15	2	0683-4725	4	R-F:4.7K OHM;5;.25W
R16	2	0683-4725	1	R-F:4.7K OHM;5;.25W
R17	4	0683-1525		R-F:1.5K OHM;5;.25W
R18	9	0683-1025		R-F:1K OHM;5;.25W
R19	8	0683-2725		R-F:2.7K OHM;5;.25W
R20	1	0683-1035		R-F:10K OHM;5;.25W
R21	1	0757-0428	1	R-F:1.62K OHM;1;.125W
R22	7	RESISTOR	1	TEST SELECT

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
R23	7	RESISTOR	1	TEST SELECT
R24	9	0683-1025		R-F:1K OHM;5;.25W
R25	9	0683-1025		R-F:1K OHM;5;.25W
R26	9	0683-1025		R-F:1K OHM;5;.25W
R27	5	0698-4123	2	R-F:499 OHM;1;.125W
R29	7	0757-0424	1	R-F:1.1K OHM;1;.125W
R30	3	0757-0420	20	R-F:750 OHM;1;.125W
R31	6	0683-5115	1	R-F:510 OHM;5;.25W
R32	7	0698-0082	1	R-F:464 OHM;1;.125W
R33	7	RESISTOR	1	TEST SELECT
R34	1	0683-5615	1	R-F:560 OHM;5;.25W
R35	7	0757-0416	1	R-F:511 OHM;1;.125W
R36	2	0698-3445	1	R-F:348 OHM;1;.125W
R37	4	0698-3447	1	R-F:422 OHM;1;.125W
R38	7	0683-1015		R-F:100 OHM;5;.25W
R39	7	0683-1015		R-F:100 OHM;5;.25W
R40	1	0683-1035		R-F:10K OHM;5;.25W
R41	1	0683-1035		R-F:10K OHM;5;.25W
R42	6	0683-2715	1	R-F:270 OHM;5;.25W
R43	7	0683-1015		R-F:100 OHM;5;.25W
R44	7	0683-1015		R-F:100 OHM;5;.25W
R45	7	RESISTOR	1	TEST SELECT
R46	9	0698-3202	1	R-F:1.74K OHM;1;.125W
R47	4	0757-0273	1	R-F:3.01K OHM;1;.125W
R48	9	0757-0442	1	R-F:10K OHM;1;.125W
R49	3	0757-0438	1	R-F:5.11K OHM;1;.125W
R50	3	0757-0420		R-F:750 OHM;1;.125W
R51	3	0757-0470	1	R-F:162K OHM;1;.125W
R52	8	0698-0083	1	R-F:1.96K OHM;1;.125W
R53	5	0698-3456	1	R-F:287K OHM;1;.125W
R54	7	0683-3615	1	R-F:360 OHM;5;.25W
RP1	7	1810-0362	1	R-F:NETWORK
RP2	0	1810-0125	4	R-F:NETWORK
RP3	0	1810-0125		R-F:NETWORK
RP4	0	1810-0125		R-F:NETWORK
RP5	0	1810-0125		R-F:NETWORK
SW1	1	3101-2256	1	SWITCH:PUSH BUTTON
SW2	4	3101-2259	1	SWITCH:SLIDE
U1	5	1820-2159	1	IC:75117
U2	7	1820-0577	2	IC:7416
U3	3	1820-2058	4	IC:TRANSCEIVER
U4	3	1820-2058		IC:TRANSCEIVER
U5	8	1820-0239		IC:MC3002
U6	3	1820-2058		IC:TRANSCEIVER
U7	3	1820-2058		IC:TRANSCEIVER
U8	1	1820-2147	1	IC:1AA6-6004
U9	0	1820-1966	1	IC:1AA1-6003
U10	8	1818-0333	2	IC:1AA3-6001
U11	8	1818-0333		IC:1AA3-6001
U12	3	1820-1977	1	IC:MC12061P3
U13	9	1820-1197	5	IC:74LS00
U14	4	1820-1423		IC:74LS123
U15	8	1820-1196	4	IC:74LS174
U16	6	1820-1053	1	IC:7414
U17	1	1820-2048	2	IC:RCA/CTX CMOS=TTL
U18	1	1820-2048		IC:RCA/CTX CMOS=TTL
U19	7	1820-1195	2	IC:74LS175
U20	0	1820-1255	2	IC:DM8098
U21	8	1820-1196		IC:74LS174

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
U22	9	1820-1238	4	IC:74LS253
U23	9	1820-1238		IC:74LS253
U24	0	1820-1198	1	IC:74LS03
U25	6	1820-1954	2	IC:1AB7-6001
U30	6	1820-1433	1	IC:74LS164
U31	2	1820-1207	1	IC:74LS30
U32	3	1820-2016	1	IC:CRC GEN
U33	0	1820-1255		IC:DM8098
U34	8	1820-1196		IC:74LS174
U35	9	1820-1238		IC:74LS253
U36	9	1820-1238		IC:74LS253
U37	6	1820-1144	3	IC:74LS02
U38	6	1820-1954		IC:1AB7-6001
U39	4	1820-1217	1	IC:74LS151
U40	7	1820-1195		IC:74LS175
U41	7	1820-1210	2	IC:74LS51
U42	9	1820-1428	1	IC:74LS158
U43	9	1820-1197		IC:74LS00
U44	5	1820-1276	4	IC:74LS194
U45	5	1820-1276		IC:74LS194
U46	7	1820-1418	1	IC:74LS42
U47	9	1820-1197		IC:74LS00
U48	9	1820-1212	1	IC:74LS112
U49	1	1816-0710	1	IC:MEMORY
U50	8	1820-1196		IC:74LS174
U51	9	1820-1197		IC:74LS00
U52	1	1820-1199	3	IC:74LS04
U53	9	1820-1444	2	IC:74LS298
U54	9	1820-1444		IC:74LS298
U55	6	1820-1144		IC:74LS02
U56	8	1820-1287	2	IC:74LS37
U57	7	1820-0577		IC:7416
U58	4	1820-0475	1	IC:LINEAR
U59	4	1821-0001	1	IC:CA3046
U60	8	1820-1419	1	IC:74LS85
U61	7	1820-1210		IC:74LS51
U63	5	1820-1440	1	IC:74LS279
U64	7	1820-1989	2	IC:74LS393
U65	5	1820-1276		IC:74LS194
U66	5	1820-1276		IC:74LS194
U67	3	1820-1282	2	IC:74LS109
U68	8	1820-1758	1	IC:DIGITAL
U69	6	1820-0427	1	IC:MC1496
U70	3	1820-1464	1	IC:74393
U71	8	1820-1112	2	IC:74LS74
U72	8	1820-1112		IC:74LS74
U73	1	1820-1199		IC:74LS04
U74	7	1820-1202	1	IC:74LS10
U75	7	1820-1989		IC:74LS393
U76	5	1820-1193	1	IC:74LS197
U77	6	1820-1144		IC:74LS02
U78	8	1826-0021	1	IC:OP AMP
U79	0	1810-0315	1	IC:DELAY LINE
U80	1	1820-1199		IC:74LS04
U81	8	1820-1211	1	IC:74LS86
U82	8	1820-1287		IC:74LS37
U83	9	1820-1197		IC:74LS00
U84	3	1820-1282		IC:74LS109
Y1	0	0410-1031	1	CRYSTAL

Controller Board Assembly (P/N 07902-60024)

Introduction

This section provides interface information, schematic diagrams and replaceable parts list for controller board P/N 07902-60024.

Interface Information

Refer to Figure 3-11 for the connector locations. Table 3-10 describes the connector pin assignments.

Addressing

The address of each individual drive is composed of two parts, the bus address and the drive or unit number. Each of these parts is set on a different switch in a different location using a different set of rules. Since it is essential that this address be set correctly, these will be covered in detail.

Bus Address

The various devices on an HP-IB channel are differentiated by the bus address portion of the address. The drive must use a bus address between 0 and 7. The bus address select switch is located on the front of the controller board (see Figure 3-10). Note that although as many as four drives may be controlled by one controller board, they all have the same bus address. If several controller boards are connected to an HP-IB, each must have a different bus address. If you change the bus address, change the number on the front panel, also.

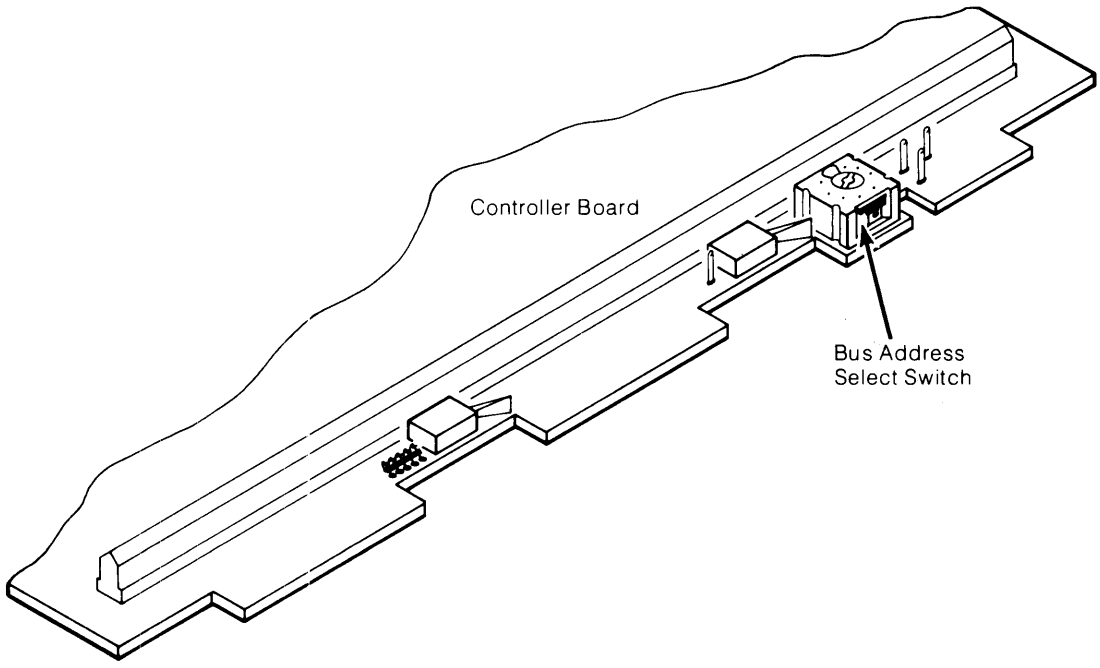


Figure 3-11. Bus Address Selector Switch

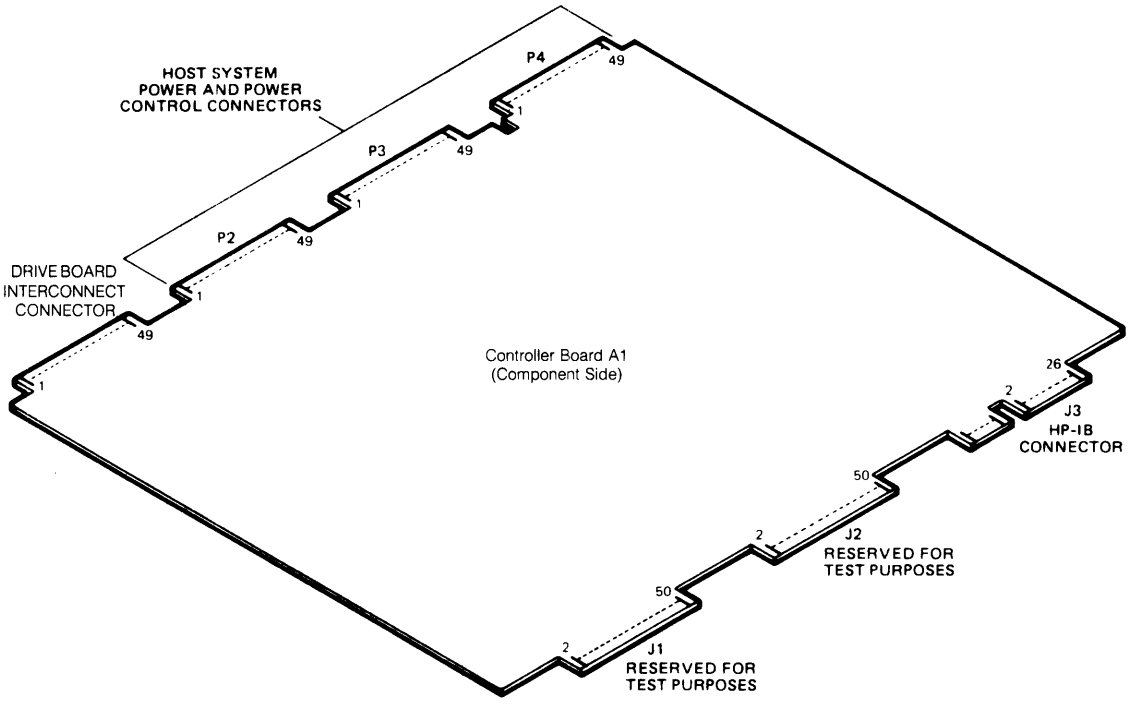


Figure 3-12. Controller Board A1 (07902-60024) Connectors

Table 3-5. 07902-60024 Connector Pin Assignments

A1P1 (See Notes 1)

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	DSLOH
3	GND	4	DSL1H
5	GND	6	DSL2H
7	GND	8	DSLVL
9	GND	10	LDCTL
11	GND	12	STENL
13	GND	14	RSPNH
15	GND	16	WRITL
17	GND	18	PHIBH
19	GND	20	PHIAH
21	GND	22	DLCKL
23	GND	24	HED1H
25	GND	26	PORH
27	GND	28	INDXL
29	GND	30	SPINL
31	GND	32	TRK0L
33	GND	34	WPRTL
35	GND	36	REDYH
37	GND	38	DATAH
39	GND	40	DATAL
41	GND	42	NC
43	KEY	44	KEY

45	GND	46	NC
47	GND	48	PONH
49	GND	50	−5V TP

A1J3 (See Note 2)

PIN	SIGNAL	PIN	SIGNAL
1	NC	2	NC
3	GND	4	GND (Shield)
5	GND	6	ATN
7	GND	8	SRQ
9	GND	10	IFC
11	GND	12	NDAC
13	GND	14	NRFD
15	GND	16	DAV
17	REN	18	EOI
19	DIO8	20	DIO4
21	DI07	22	DIO3
23	DIO6	24	DIO2
25	DIO5	26	DIO1

A1P2 (See Note 1)

PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	+5V
3	+5V	4	+5V
7	−12V	8	−12V
13	+12V	14	+12V
17	NC	18	GND
27	NC	28	GND
35	GND	36	PON
45	GND	46	GND

A1P4 (See Note 1)

PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	+5V
3	+5V	4	+5V
7	−12V	8	−12V
13	+12V	14	+12V
17	NC	18	GND
27	NC	28	GND
33	SYSRST	34	NC
35	GND	36	PON
45	GND	46	GND

Notes:

1. Even-numbered pins are on circuit side of Board, odd-numbered pins are component side.
2. Odd-numbered pins are on circuit side of the Board, even-numbered pins are on component side.

Schematic Diagrams

Introduction

This section contains the circuit diagrams for the controller board P/N 07902-60024.

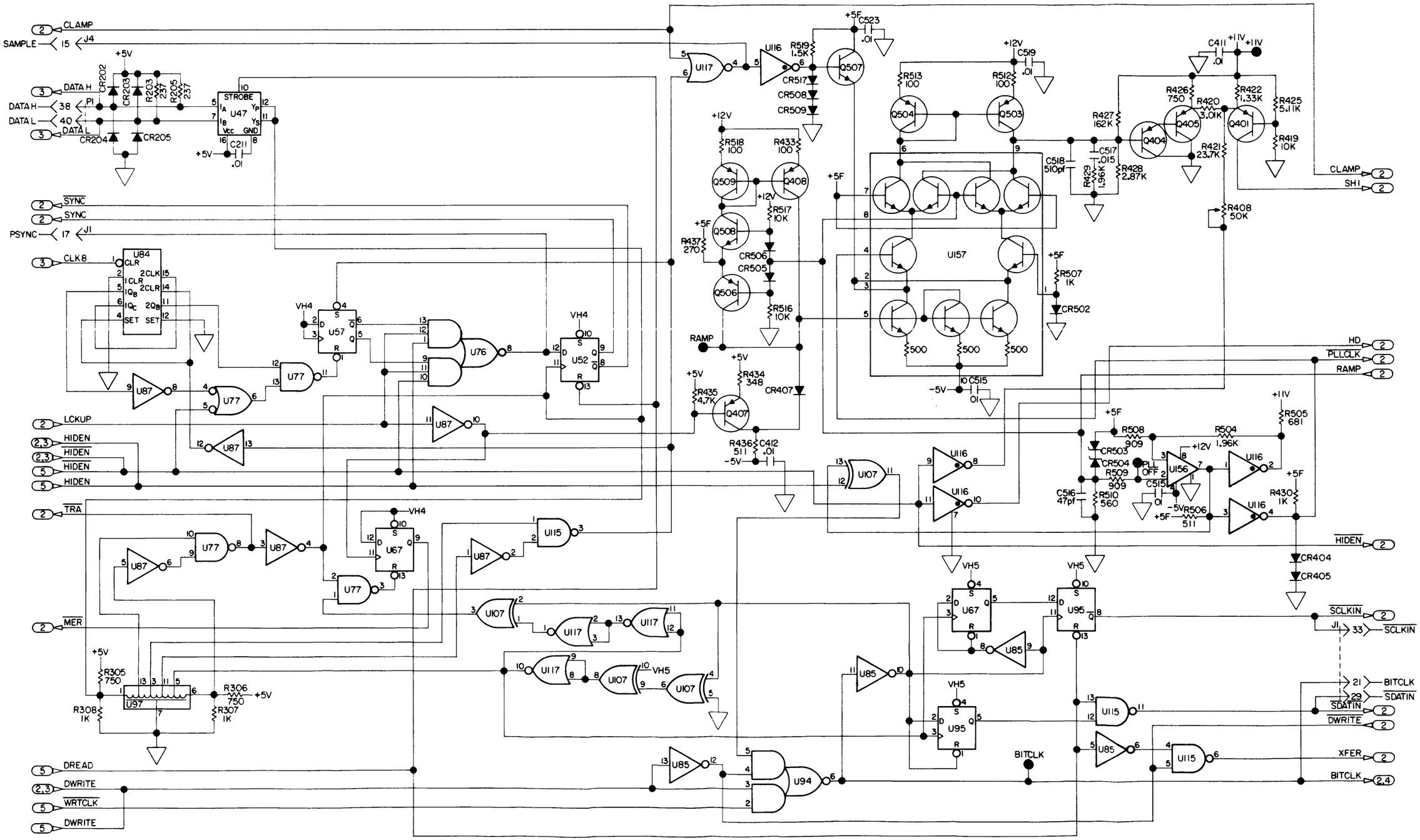


Figure 3-13. Controller Board A1 (07902-60024) Schematic Diagrams (Sheet 1)

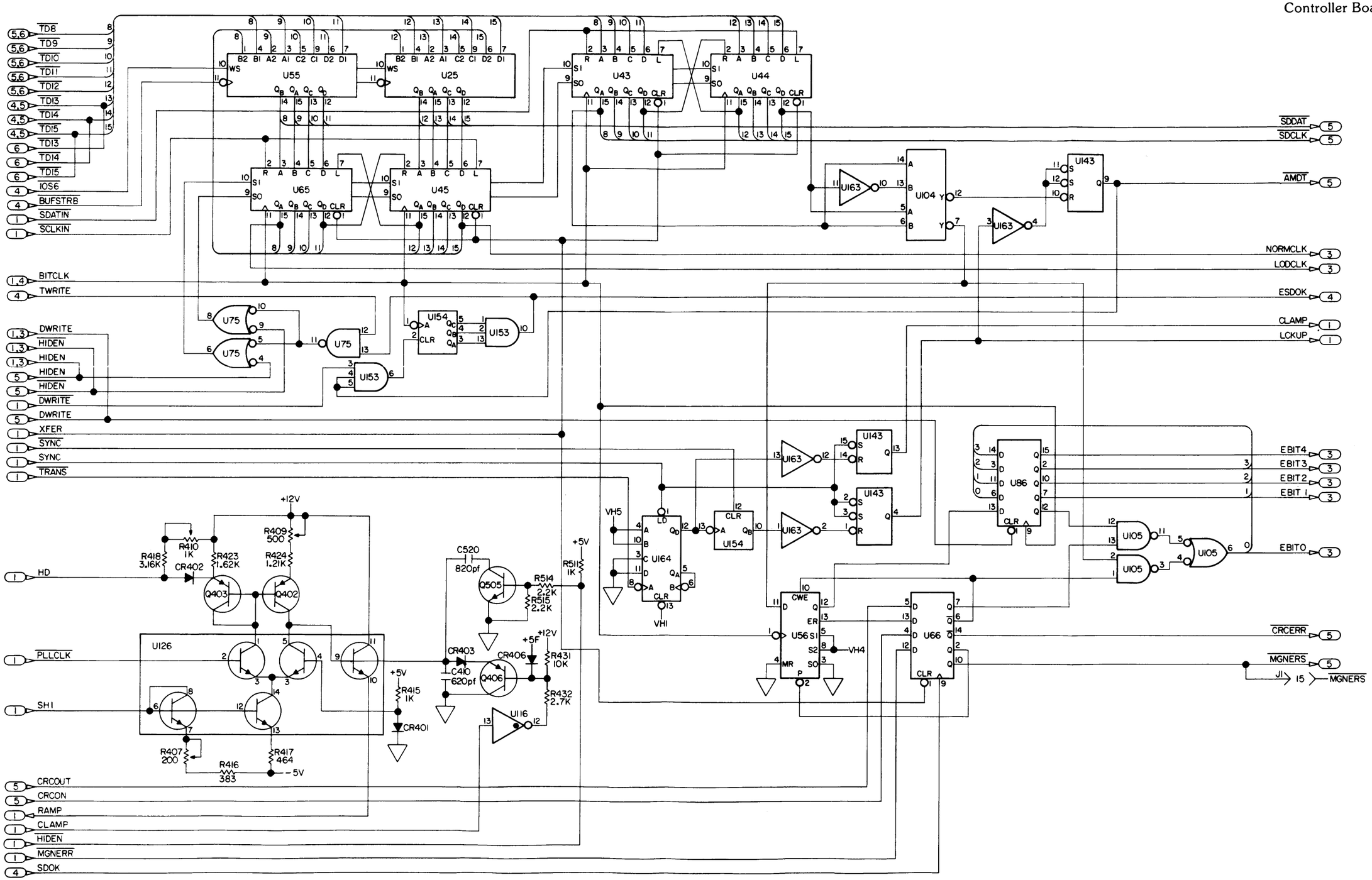


Figure 3-13. Controller Board A1 (07902-60024) Schematic Diagrams (Sheet 2)

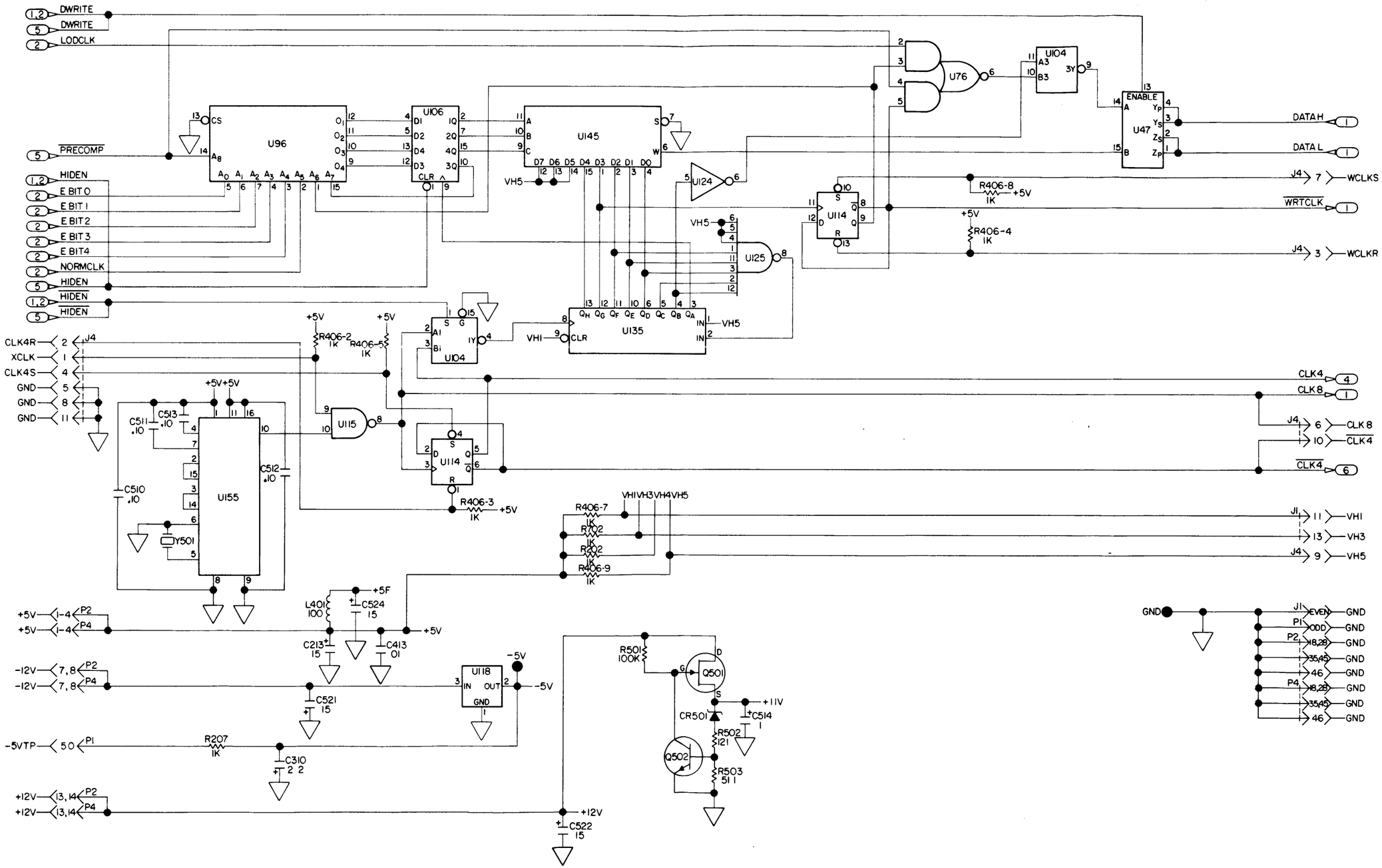


Figure 3-13. Controller Board A1 (07902-60024) Schematic Diagrams (Sheet 3)

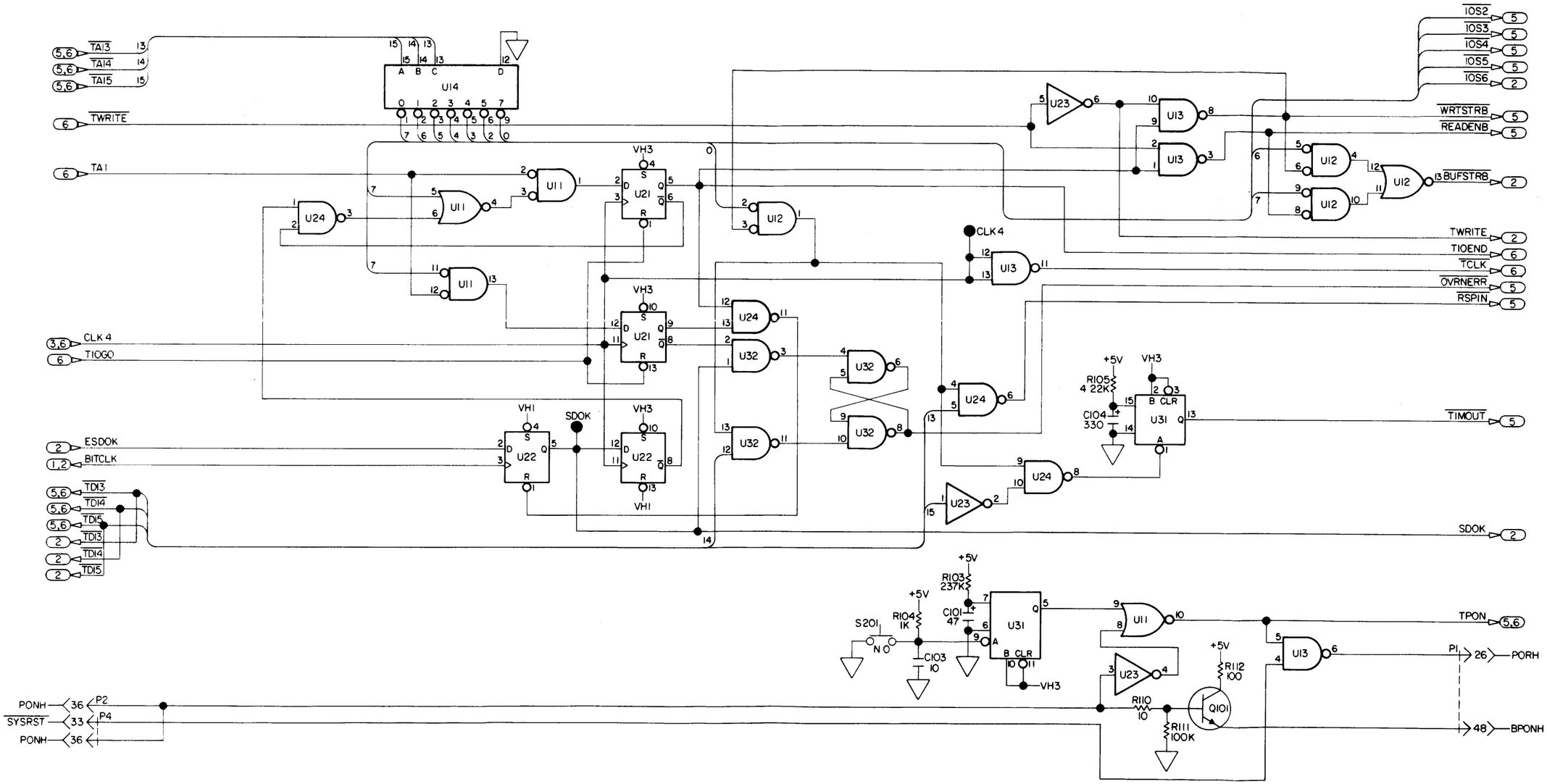


Figure 3-13. Controller Board A1 (07902-60024) Schematic Diagrams (Sheet 4)

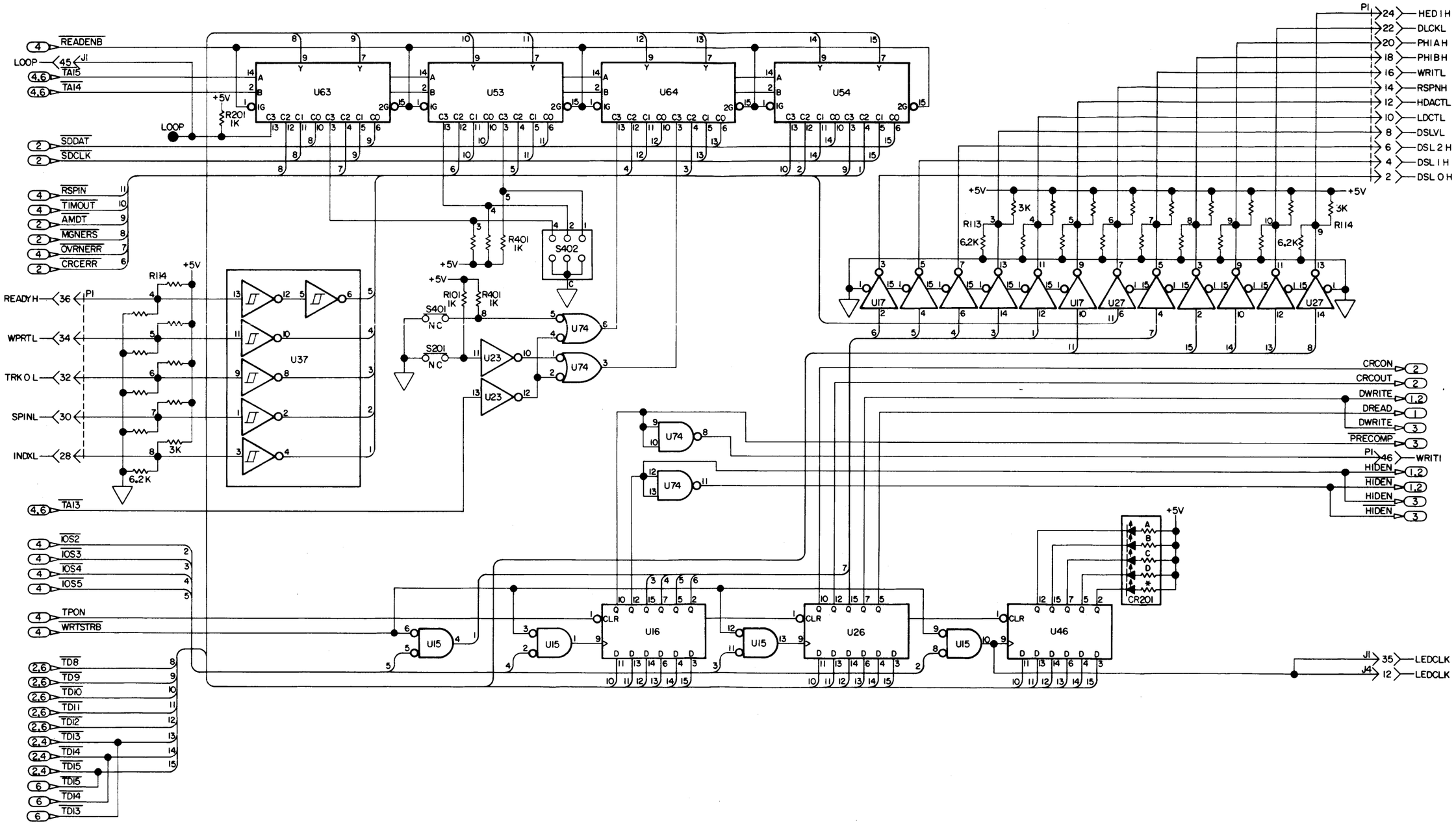


Figure 3-13. Controller Board A1 (07902-60024) Schematic Diagrams (Sheet 5)

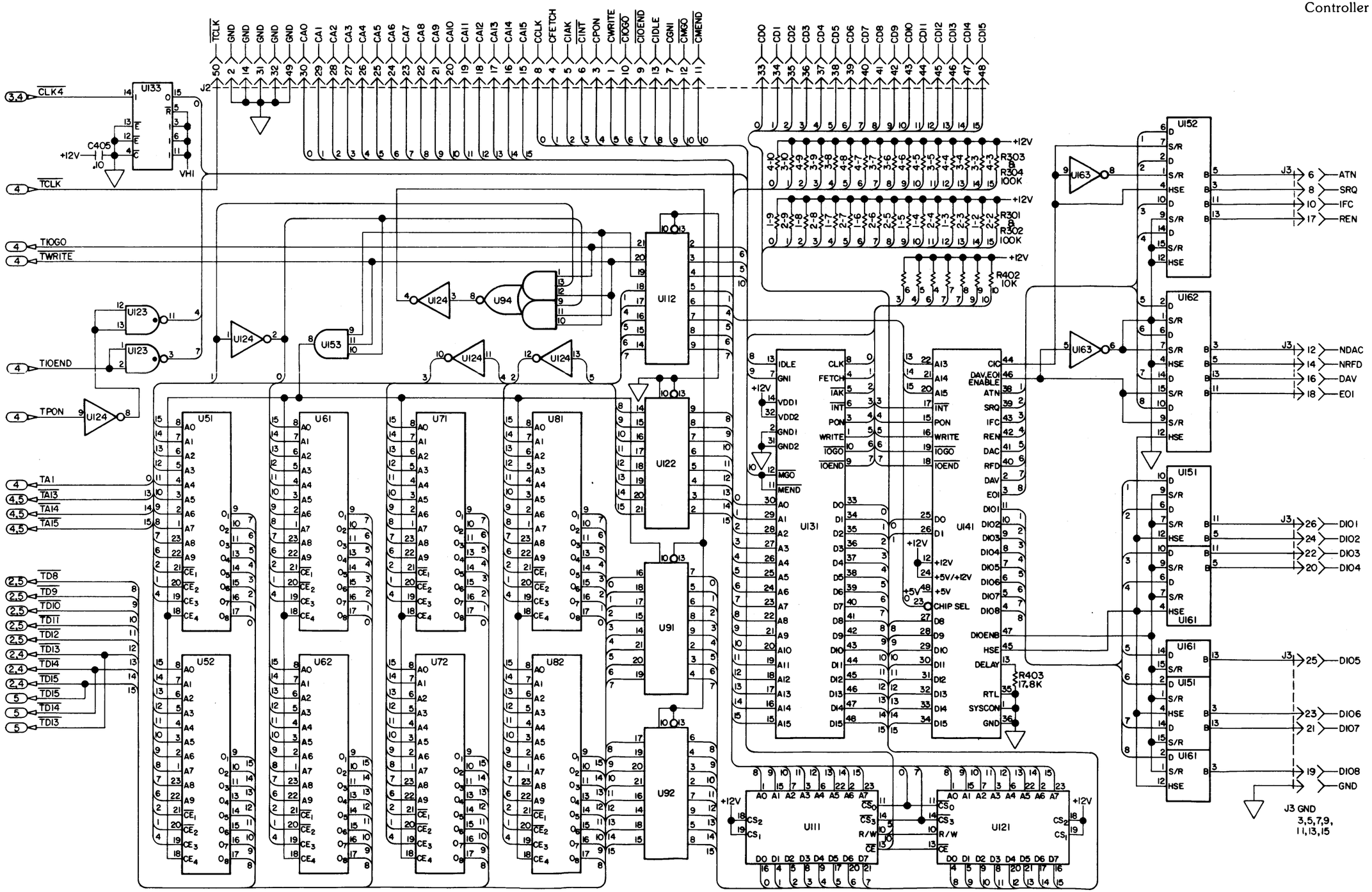


Figure 3-13. Controller Board A1 (07902-60024) Schematic Diagrams (Sheet 6)

Replaceable Parts

Introduction

The controller board P/N 07902-60024 parts list is provided in this section. The total quantity of a part is shown only the first time it is used on this assembly.

The number shown in the "CD" column is the parts check digit. Include the check digit number with the part number when ordering a part from HP.

Reference designators are listed in a alphanumeric order in lieu of item numbers for printed circuit assembly parts.

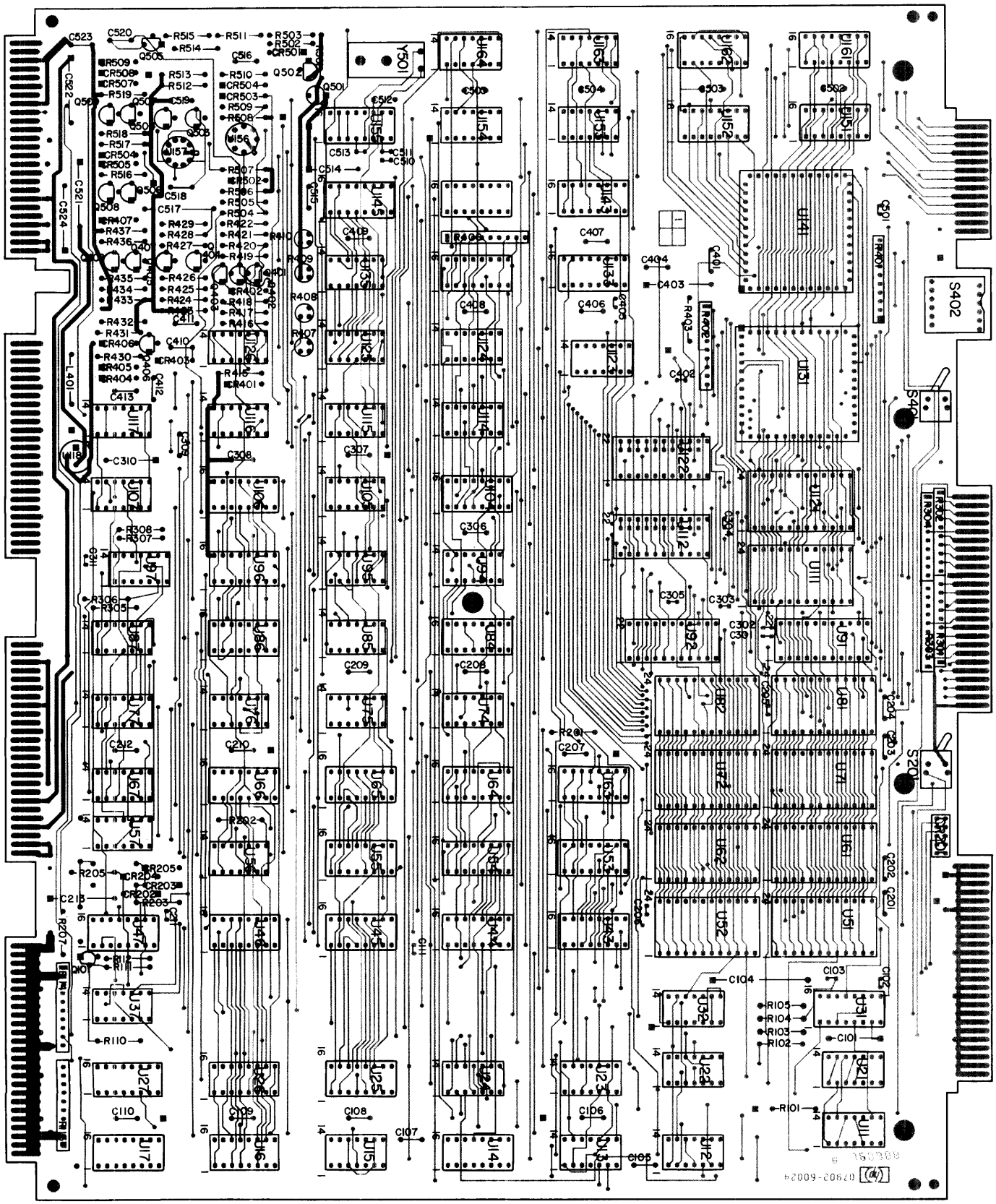


Figure 3-14. Controller Board A1 (07902-60024) Component Locator

Controller Board 07902-60024

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
C101	5	0180-0376	1	C-F:.47 UF;35V
C102	5	0160-0576	8	C-F:.1 UF;50V
C103	5	0160-0576		C-F:.1 UF;50V
C104	9	0160-2055	36	C-F:.01 UF;100V
C105	9	0160-2055		C-F:.01 UF;100V
C106	9	0160-2055		C-F:.01 UF;100V
C107	9	0160-2055		C-F:.01 UF;100V
C108	9	0160-2055		C-F:.01 UF;100V
C109	9	0160-2055		C-F:.01 UF;100V
C110	7	0180-1714	1	C-F:330 UF;6V
C111	5	0160-0576		C-F:.1 UF;50V
C201	9	0160-2055		C-F:.01 UF;100V
C202	9	0160-2055		C-F:.01 UF;100V
C203	9	0160-2055		C-F:.01 UF;100V
C204	9	0160-2055		C-F:.01 UF;100V
C205	5	0160-0576		C-F:.1 UF;50V
C206	5	0160-0576		C-F:.1 UF;50V
C207	9	0160-2055		C-F:.01 UF;100V
C208	9	0160-2055		C-F:.01 UF;100V
C209	9	0160-2055		C-F:.01 UF;100V
C210	9	0160-2055		C-F:.01 UF;100V
C211	5	0160-0576		C-F:.1 UF;50V
C212	9	0160-2055		C-F:.01 UF;100V
C213	5	0180-1746	5	C-F:15 UF;20V
C301	5	0160-0576		C-F:.1 UF;50V
C302	5	0160-0576		C-F:.1 UF;50V
C303	5	0160-0576		C-F:.1 UF;50V
C304	5	0160-0576		C-F:.1 UF;50V
C305	5	0160-0576		C-F:.1 UF;50V
C306	9	0160-2055		C-F:.01 UF;100V
C307	9	0160-2055		C-F:.01 UF;100V
C308	9	0160-2055		C-F:.01 UF;100V
C309	9	0160-2055		C-F:.01 UF;100V
C310	8	0180-0197	1	C-F:2.2 UF;20V
C311	5	0160-0576		C-F:.1 UF;50V
C401	9	0160-2055		C-F:.01 UF;100V
C402	5	0160-0576		C-F:.1 UF;50V
C403	5	0180-1746		C-F:15 UF;20V
C404	9	0160-2055		C-F:.01 UF;100V
C405	5	0160-0576		C-F:.1 UF;50V
C406	9	0160-2055		C-F:.01 UF;100V
C407	9	0160-2055		C-F:.01 UF;100V
C408	9	0160-2055		C-F:.01 UF;100V
C409	9	0160-2055		C-F:.01 UF;100V
C410	8	0160-0363	1	C-F:620 PF;300V
C411	9	0160-2055		C-F:.01 UF;100V
C412	9	0160-2055		C-F:.01 UF;100V
C413	9	0160-2055		C-F:.01 UF;100V
C501	5	0160-0576		C-F:.1 UF;50V
C502	9	0160-2055		C-F:.01 UF;100V
C503	9	0160-2055		C-F:.01 UF;100V
C504	9	0160-2055		C-F:.01 UF;100V
C505	9	0160-2055		C-F:.01 UF;100V
C510	5	0160-0576		C-F:.1 UF;50V
C511	5	0160-0576		C-F:.1 UF;50V
C512	9	0160-2055		C-F:.01 UF;100V
C513	5	0160-0576		C-F:.1 UF;50V

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
C514	3	0180-0291	1	C-F:1 UF;35V
C515	9	0160-2055		C-F:.01 UF;100V
C516	4	0160-2307	1	C-F:47 PF;300V
C517	3	0160-0194	1	C-F:15000 PF;200V
C518	1	0160-3534	1	C-F:510 PF;100V
C519	9	0160-2055		C-F:.01 UF;100V
C520	3	0160-2009	1	C-F:820 PF;300V
C521	5	0180-1746		C-F:15 UF;20V
C522	5	0180-1746		C-F:15 UF;20V
C523	9	0160-2055		C-F:.01 UF;100V
C524	5	0180-1746		C-F:15 UF;20V
CR201	2	1990-0622		DIODE;LED
CR202	1	1901-0040		DIODE:SWITCHING
CR203	1	1901-0040		DIODE:SWITCHING
CR204	1	1901-0040		DIODE:SWITCHING
CR205	1	1901-0040		DIODE:SWITCHING
CR401	1	1901-0040		DIODE:SWITCHING
CR402	1	1901-0040		DIODE:SWITCHING
CR403	1	1901-0040		DIODE:SWITCHING
CR404	1	1901-0040		DIODE:SWITCHING
CR405	1	1901-0040		DIODE:SWITCHING
CR406	1	1901-0040		DIODE:SWITCHING
CR407	1	1901-0040		DIODE:SWITCHING
CR501	2	1902-3150		DIODE;ZENER;9.09V
CR502	1	1901-0040		DIODE:SWITCHING
CR503	3	1902-3002		DIODE:ZENER;2.3V
CR504	3	1902-3002		DIODE:ZENER;2.3V
CR505	1	1901-0040		DIODE:SWITCHING
CR506	1	1901-0040		DIODE:SWITCHING
CR507	1	1901-0040		DIODE:SWITCHING
CR508	1	1901-0040		DIODE:SWITCHING
CR509	1	1901-0040		DIODE:SWITCHING
L401	1	9140-0210	1	COIL:100UH;5
Q101	1	1854-0215		TRANSISTOR:2N3904
Q401	5	1853-0089		TRANSISTOR:2N4917
Q402	5	1853-0089		TRANSISTOR:2N4917
Q403	5	1853-0089		TRANSISTOR:2N4917
Q404	5	1853-0089		TRANSISTOR:2N4917
Q405	5	1853-0089		TRANSISTOR:2N4917
Q406	5	1853-0089		TRANSISTOR:2N4917
Q407	5	1853-0089		TRANSISTOR:2N4917
Q408	5	1853-0089		TRANSISTOR:2N4917
Q501	2	1855-0420		TRANSISTOR:2N4391
Q502	1	1854-0215		TRANSISTOR:2N3904
Q503	5	1853-0089		TRANSISTOR:2N4917
Q504	5	1853-0089		TRANSISTOR:2N4917
Q505	1	1854-0215		TRANSISTOR:2N3904
Q506	5	1853-0089		TRANSISTOR:2N4917
Q507	2	1854-0092		TRANSISTOR:2N3563
Q508	2	1854-0092		TRANSISTOR:2N3563
Q509	5	1853-0089		TRANSISTOR:2N4917
R101	9	0683-1025	12	R-F:1K OHM;5;.25W
R102	9	0683-1025		R-F:1K OHM;5;.25W
R103	5	0698-3266	1	R-F:237K OHM;1;.125W
R104	9	0683-1025		R-F:1K OHM;5;.25W
R105	0	0698-3154	1	R-F:4.22K OHM;1;.125W
R110	5	0683-1005	1	R-F:10 OHM;5;.25W
R111	3	0683-1045	2	R-F:100K OHM;5;.25W
R112	7	0683-1015	5	R-F:100 OHM;5;.25W

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
R113	3	1810-0136	2	R-F:NETWORK
R114	3	1810-0136		R-F:NETWORK
R201	9	0683-1025		R-F:1K OHM;5;.25W
R202	9	0683-1025		R-F:1K OHM;5;.25W
R203	9	0698-3442	2	R-F:237 OHM;1;.125W
R205	9	0698-3442		R-F:237 OHM;1;.125W
R207	9	0683-1025		R-F:1K OHM;5;.25W
R301	9	1810-0281	4	R-F:NETWORK
R302	9	1810-0281		R-F:NETWORK
R303	9	1810-0281		R-F:NETWORK
R304	9	1810-0281		R-F:NETWORK
R305	3	0757-0420	3	R-F:750 OHM;1;.125W
R306	3	0757-0420		R-F:750 OHM;1;.125W
R307	9	0683-1025		R-F:1K OHM;5;.25W
R308	9	0683-1025		R-F:1K OHM;5;.25W
R401	1	1810-0275	2	R-F:NETWORK
R402	8	1810-0280	1	R-F:NETWORK
R403	8	0698-3136	1	R-F:17.8K OHM;1;.125W
R406	1	1810-0275		R-F:NETWORK
R407	3	2100-2061	1	R-F:THERMISTOR;200 OHM;10
R408	7	2100-2031	1	R-F:THERMISTOR;50K OHM;10
R409	9	2100-1788	1	R-F:THERMISTOR;500 OHM;10
R410	9	2100-1986	1	R-F:THERMISTOR;1K OHM;10
R415	9	0683-1025		R-F:1K OHM;5;.25W
R417	7	0698-0082	1	R-F:464 OHM;1;.125W
R418	0	0757-0279	1	R-F:3.16K OHM;1;.125W
R419	1	0683-1035	4	R-F:10K OHM;5;.25W
R420	4	0757-0273	1	R-F:3.01K OHM;1;.125W
R421	4	0698-3158	1	R-F:23.7K OHM;1;.125W
R422	7	0757-0317	1	R-F:1.33K OHM;1;.125W
R423	1	0757-0428	1	R-F:1.62K OHM;1;.125W
R424	5	0757-0274	1	R-F:1.21K OHM;1;.125W
R425	3	0757-0438	1	R-F:5.11K OHM;1;.125W
R426	3	0757-0420		R-F:750 OHM;1;.125W
R427	3	0757-0470	1	R-F:162K OHM;1;.125W
R428	5	0698-3456	1	R-F:287K OHM;1;.125W
R429	8	0698-0083	2	R-F:1.96K OHM;1;.125W
R430	9	0683-1025		R-F:1K OHM;5;.25W
R431	1	0683-1035		R-F:10K OHM;5;.25W
R432	8	0683-2725	1	R-F:2.7K OHM;5;.25W
R434	2	0698-3445	1	R-F:348 OHM;1;.125W
R435	2	0683-4725	1	R-F:4.7K OHM;5;.25W
R436	7	0757-0416		R-F:511 OHM;1;.125W
R437	6	0683-2715	1	R-F:270 OHM;5;.25W
R501	3	0683-1045		R-F:100K OHM;5;.25W
R502	2	0757-0403	1	R-F:121 OHM;1;.125W
R503	0	0757-0394	1	R-F:51.1 OHM;1;.125W
R504	8	0698-0083		R-F:1.96K OHM;1;.125W
R505	0	0757-0419	1	R-F:681 OHM;1;.125W
R506	7	0757-0416	2	R-F:511 OHM;1;.125W
R507	9	0683-1025		R-F:1K OHM;5;.25W
R508	5	0757-0422	2	R-F:909 OHM;1;.125W
R509	5	0757-0422		R-F:909 OHM;1;.125W
R510	1	0683-5615	1	R-F:560 OHM;5;.25W
R511	9	0683-1025		R-F:1K OHM;5;.25W
R514	3	0683-2225	2	R-F:2.2K OHM;5;.25W
R515	3	0683-2225		R-F:2.2K OHM;5;.25W
R516	1	0683-1035		R-F:10K OHM;5;.25W
R517	1	0683-1035		R-F:10K OHM;5;.25W

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
R519	4	0683-1525	1	R-F:1.5K OHM;5;.25W
S201	6	3101-1675	2	SWITCH:TOGGLE;DPST
S401	6	3101-1675		SWITCH:TOGGLE;DPST
S402	9	3100-3395	1	SWITCH:THUMBWHEEL;8 POS
U11	6	1820-1144		IC:74LS02
U12	6	1820-1144	4	IC:74LS02
U13	8	1820-1287	2	IC:74LS37
U14	7	1820-1418	1	IC:74LS42
U15	6	1820-1144		IC:74LS02
U16	8	1820-1196	4	IC:74LS174
U17	6	1820-1368	2	IC:74366
U21	8	1820-1112	6	IC:74LS74
U22	8	1820-1112		IC:74LS74
U23	1	1820-1199	5	IC:74LS04
U24	9	1820-1197	6	IC:74LS00
U25	9	1820-1444	2	IC:74LS298
U26	8	1820-1196		IC:74LS174
U27	6	1820-1368		IC:74366
U31	4	1820-1423	1	IC:74LS123
U32	9	1820-1197		IC:74LS00
U37	5	1820-1416	1	IC:74LS14
U43	5	1820-1276	4	IC:74LS194
U44	5	1820-1276		IC:74LS194
U45	5	1820-1276		IC:74LS194
U46	8	1820-1196		IC:74LS174
U47	8	1820-2128	1	IC:75116
U51	5	1816-1407	1	IC:MEMORY
U52	6	1816-1408	1	IC:MEMORY
U53	9	1820-1238	4	IC:74LS253
U54	9	1820-1238		IC:74LS253
U55	9	1820-1444		IC:74LS298
U56	3	1820-2016	1	IC:CRC GEN
U57	8	1820-1112		IC:74LS74
U61	7	1816-1409	1	IC:MEMORY
U62	0	1816-1410	1	IC:MEMORY
U63	9	1820-1238		IC:74LS253
U64	9	1820-1238		IC:74LS253
U65	5	1820-1276		IC:74LS194
U66	7	1820-1195	2	IC:74LS175
U67	8	1820-1112		IC:74LS74
U71	1	1816-1411	1	IC:MEMORY
U72	2	1816-1412	1	IC:MEMORY
U74	8	1820-1287		IC:74LS37
U75	9	1820-1197		IC:74LS00
U76	7	1820-1210	2	IC:74LS51
U77	9	1820-1197		IC:74LS00
U81	3	1816-1413	1	IC:MEMORY
U82	4	1816-1414	1	IC:MEMORY
U84	7	1820-2078	1	IC:74LS490
U85	1	1820-1199		IC:74LS04
U86	8	1820-1196		IC:74LS174
U87	1	1820-1199		IC:74LS04
U91	1	1820-2048	4	IC:RCA/CTX CMOS=TTL
U92	1	1820-2048		IC:RCA/CTX CMOS=TTL
U94	7	1820-1210		IC:74LS51
U95	8	1820-1112		IC:74LS74
U97	0	1810-0315	1	R-F:NETWORK
U104	9	1820-1428	1	IC:74LS158
U105	9	1820-1197		IC:74LS00

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
U106	7	1820-1195		IC:74LS175
U107	8	1820-1211	1	IC:74LS86
U111	8	1818-0333	2	IC:1AD3-6001
U112	1	1820-2048		IC:RCA/CTX CMOS=TTL
U114	8	1820-1112		IC:74LS74
U115	9	1820-1197		IC:74LS00
U116	7	1820-0577	1	IC:7416
U117	6	1820-1144		IC:74LS02
U118	9	1826-0220	1	IC:LM3208-05
U121	8	1818-0333		IC:1AD3-6001
U122	1	1820-2048		IC:RCA/CTX CMOS=TTL
U123	6	1820-1417	1	IC:74LS26
U124	1	1820-1199		IC:74LS04
U125	2	1820-1207	1	IC:74LS30
U126	4	1821-0001	1	IC:CA3046
U131	0	1820-1966	1	IC:1AA1-6003
U133	8	1820-1758	1	IC:DIGITAL
U135	6	1820-1433	1	IC:74LS164
U141	1	1820-2147	1	IC:1AA6-6004
U143	5	1820-1440	1	IC:74LS279
U145	4	1820-1217	1	IC:74LS151
U151	3	1820-2058	4	IC:TRANSCEIVER
U152	3	1820-2058		IC:TRANSCEIVER
U153	8	1820-1203	1	IC:74LS11
U154	7	1820-1989	1	IC:74LS393
U155	9	1820-2012	1	IC:CRYSTAL OSC
U156	4	1820-0475	1	IC:LINEAR
U157	6	1820-0427	1	IC:MC1496
U161	3	1820-2058		IC:TRANSCEIVER
U162	3	1820-2058		IC:TRANSCEIVER
U163	1	1820-1199		IC:74LS04
U164	5	1820-1193	1	IC:74LS197
Y501	0	0410-1031	1	CRYSTAL

Controller Board Assembly (P/N 07902-66510)

Introduction

This section provides interface information, schematic diagrams and replaceable parts list for controller board P/N 07902-66510.

Interface Information

Refer to Figure 3-13 for the connector and locations. Table 3-12 describes the connector pin assignments.

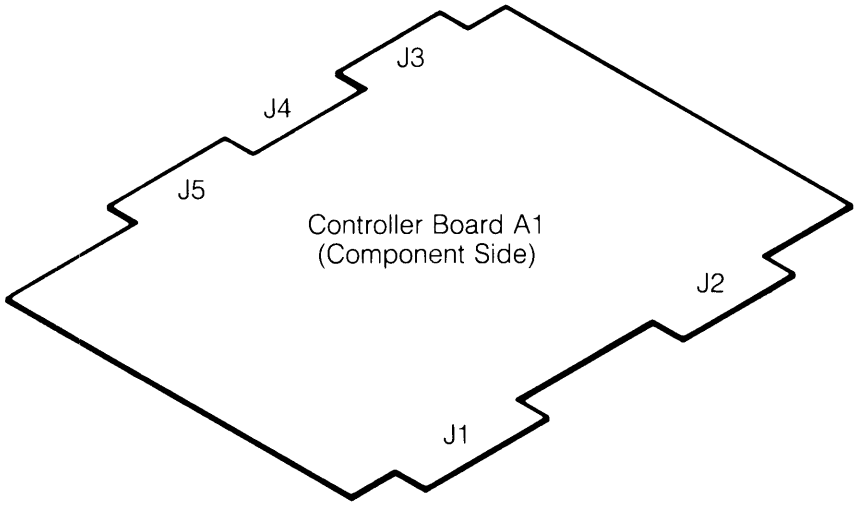


Figure 3-15. Controller Board A1 (07902-66510) Connectors

Table 3-6. 07902-66510 Connector Pin Assignments

HP-IB Connector

J4

PIN	SIGNAL	PIN	SIGNAL
2	SPARE	20	DIO8
4	ATN	22	DIO7
6	SRQ	24	DIO6
8	NDAC	26	DIO5
10	NRFD	28	DIO4
12	IFC	30	DIO3
14	REN	32	DIO2
16	DAV	34	DIO1
18	EOI		

1 to 33 Odd = GND

J5

PIN	SIGNAL	PIN	SIGNAL
2	LOW CURR	28	DRV1
4	N.C.	30	DRV2
6	N.C.	32	DRV3

8	N.C.	34	MOVE IN
10	TWO-SIDE	36	STEP
12	DISK CHANG	38	WDATA
14	HEAD SEL	40	WRIT DRV
16	HEAD LOAD	42	TRACK 0
18	N.C.	44	WRTPRT
20	INDEX	46	RDATA
22	READY	48	N.C.
24	N.C.	50	N.C.
26	DRV0		

1 to 49 Odd = GND

J3

PIN	SIGNAL	PIN	SIGNAL
A	RD	1	GND
B	RESET	2	M1
C	INT	3	NMI
D	RFSH	4	WR
E	WAIT	5	IORQ
F	GND	6	MREQ
H	HALT	7	GND
J	A0	8	A1
K	A2	9	A3
L	A4	10	A5
M	A6	11	A7
N	A8	12	A9
P	A10	13	A11
R	A12	14	A13
S	A14	15	A15
S	A14	15	A15
T	GND	16	GND
U	GND	18	GND
V	GND	18	GND
W	GND	19	GND
X	GND	20	GND
Y	D7	21	D6
Z	D5	22	D4
AA	D3	23	D2
BB	D1	24	D0
CC	GND	25	HMHZ

J1

PIN	SIGNAL	PIN	SIGNAL
B	GND	2	GND
C	GND	3	GND
BB	−5V	24	−5V
CC	+12V	25	−12V

J2

PIN	SIGNAL	PIN	SIGNAL
A	−12V	1	−12V
Y	POP	21	H.C.
Z	GND	22	GND
AA	GND	23	GND

BB	−5V	24	−5V
CC	−5V	25	−5V

All other pins on J1
and J2 are N.C.

Schematic Diagrams

Introduction

This section contains the circuit diagrams for controller board P/N 07902-66510.

NOTE:
* VALUES SELECTED IN TEST.

Figure 3-16. Controller Board A1 (07902-66510) Schematic Diagrams (Sheet 1)

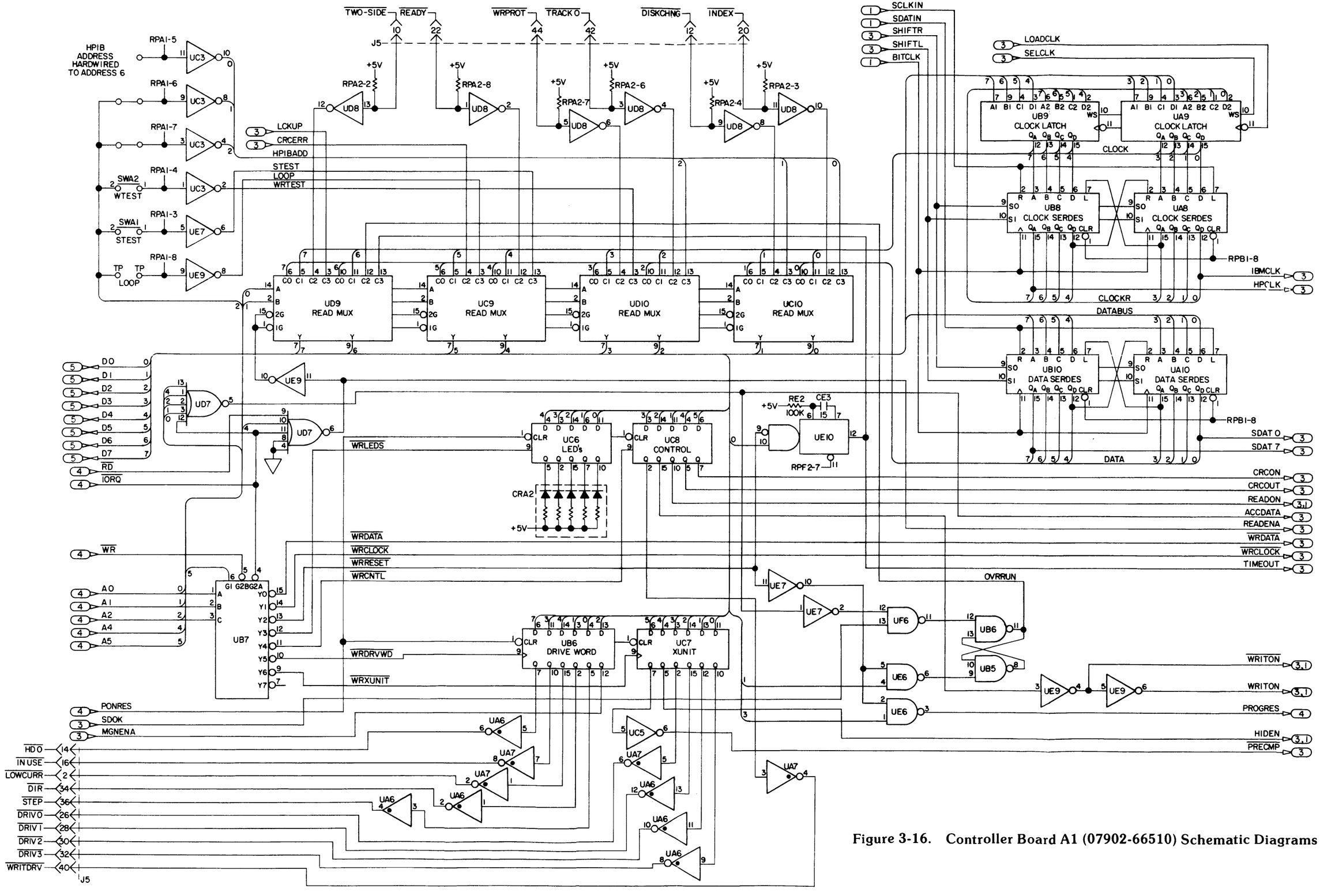


Figure 3-16. Controller Board A1 (07902-66510) Schematic Diagrams (Sheet 2)

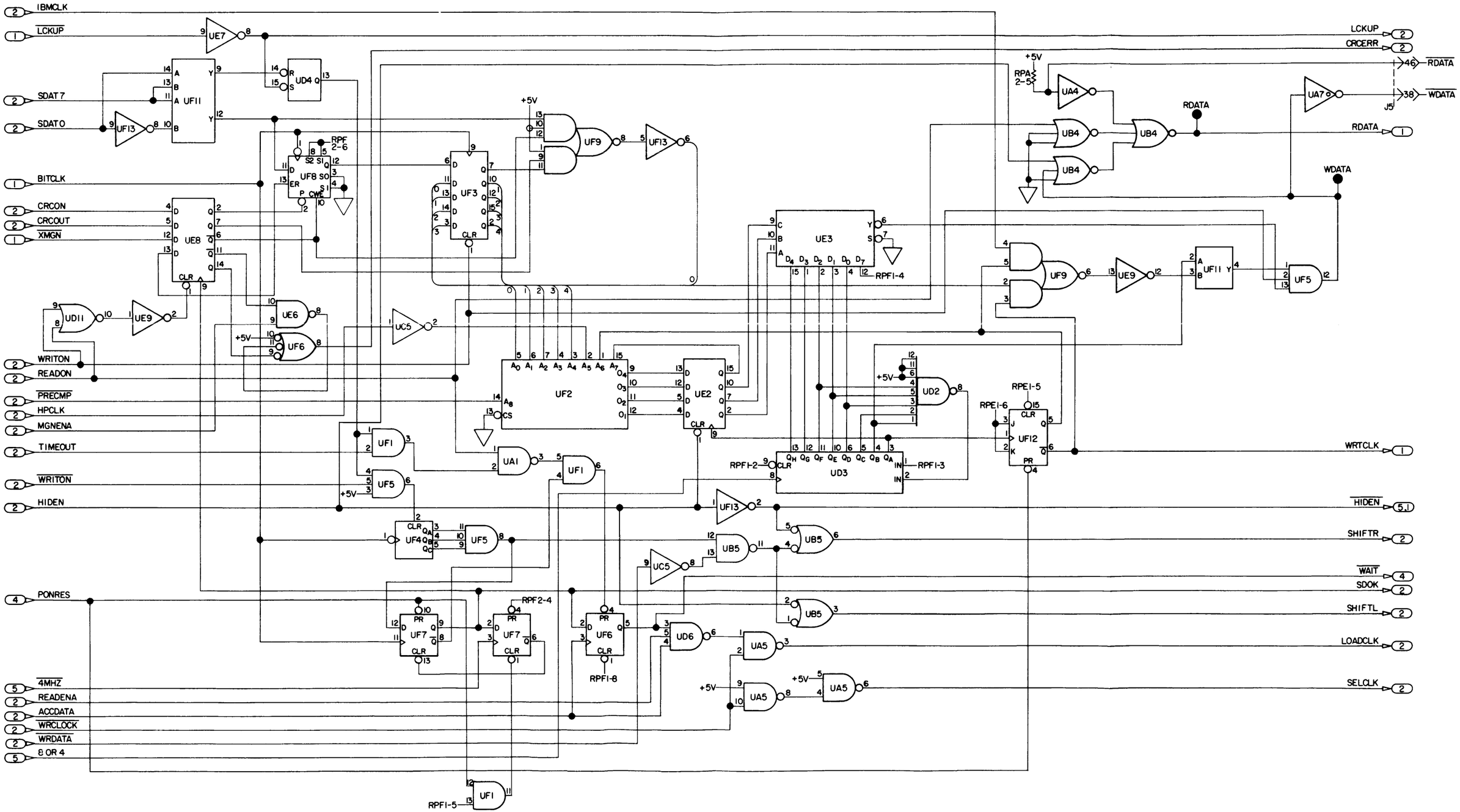


Figure 3-16. Controller Board A1 (07902-66510) Schematic Diagrams (Sheet 3)

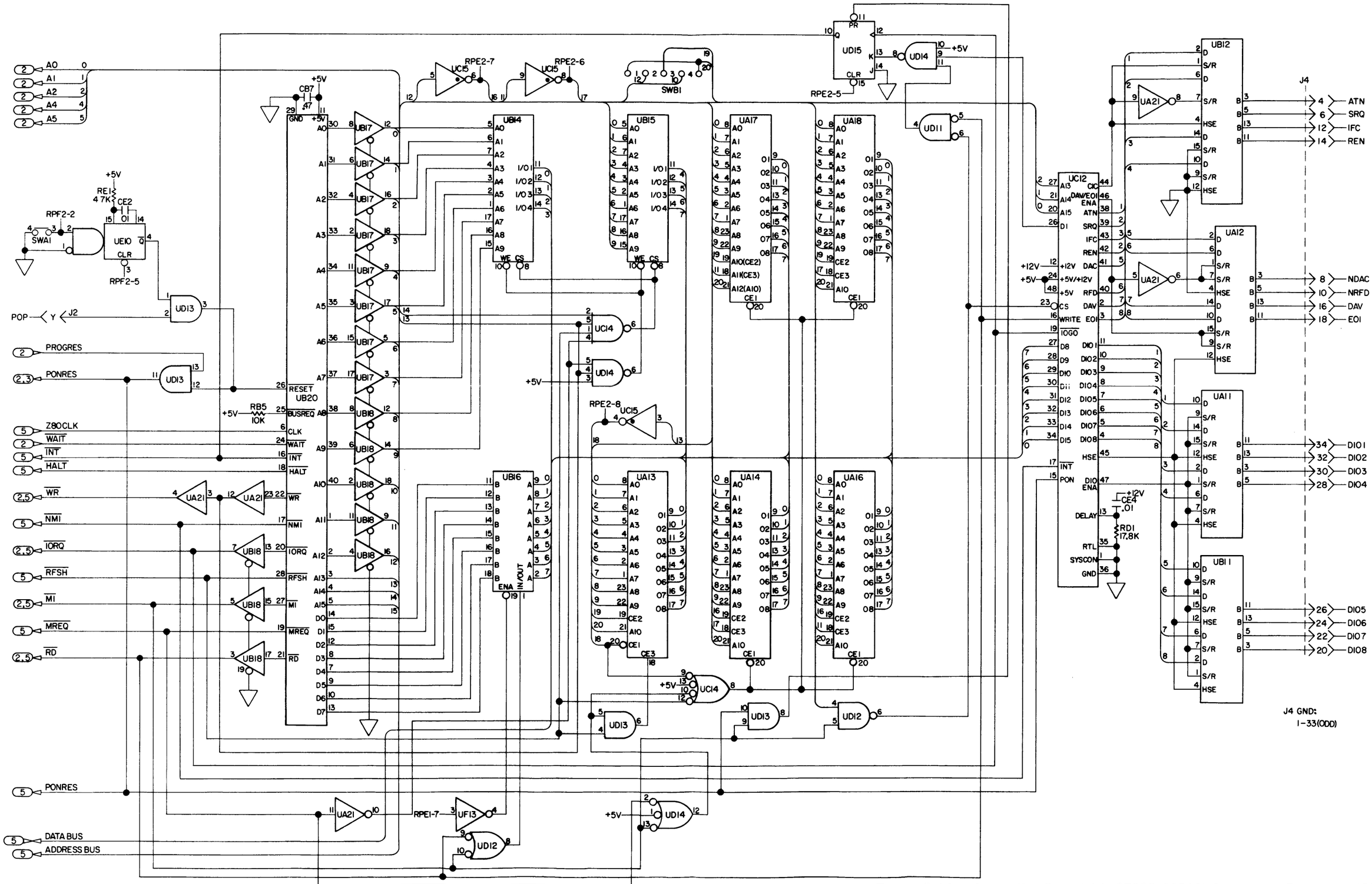


Figure 3-16. Controller Board A1 (07902-66510) Schematic Diagrams (Sheet 4)

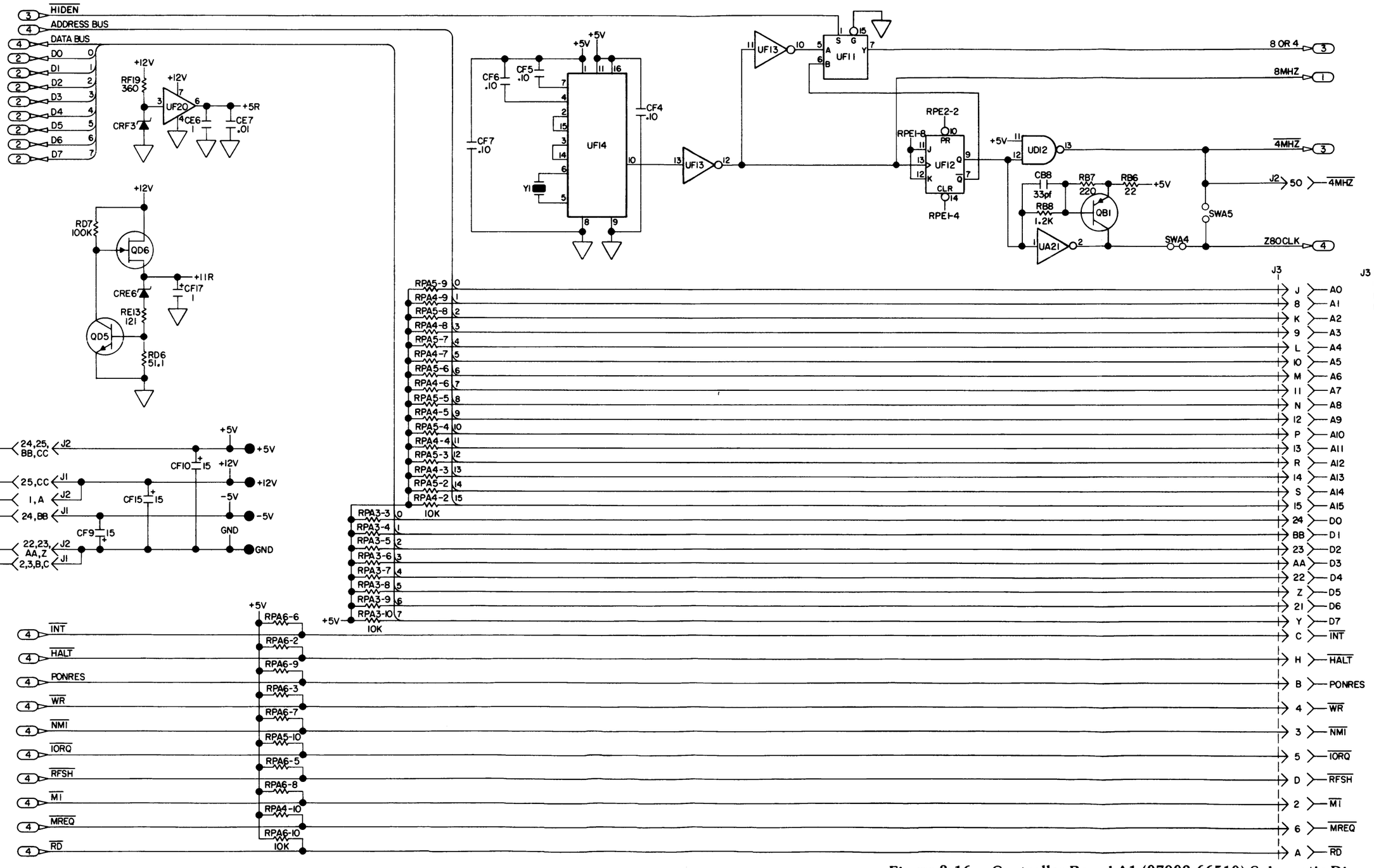


Figure 3-16. Controller Board A1 (07902-66510) Schematic Diagrams (Sheet 5)

Replaceable Parts

Introduction

The controller board P/N 07902-66510 parts list is provided in this section. The total quantity of a part is shown only the first time it is used on this assemblly.

The number shown in the "CD" column is the parts check digit. Include the check digit number with the part number when ordering a part from HP.

Reference designators are listed in alphanumeric order in lieu of item numbers for printed circuit assembly parts.

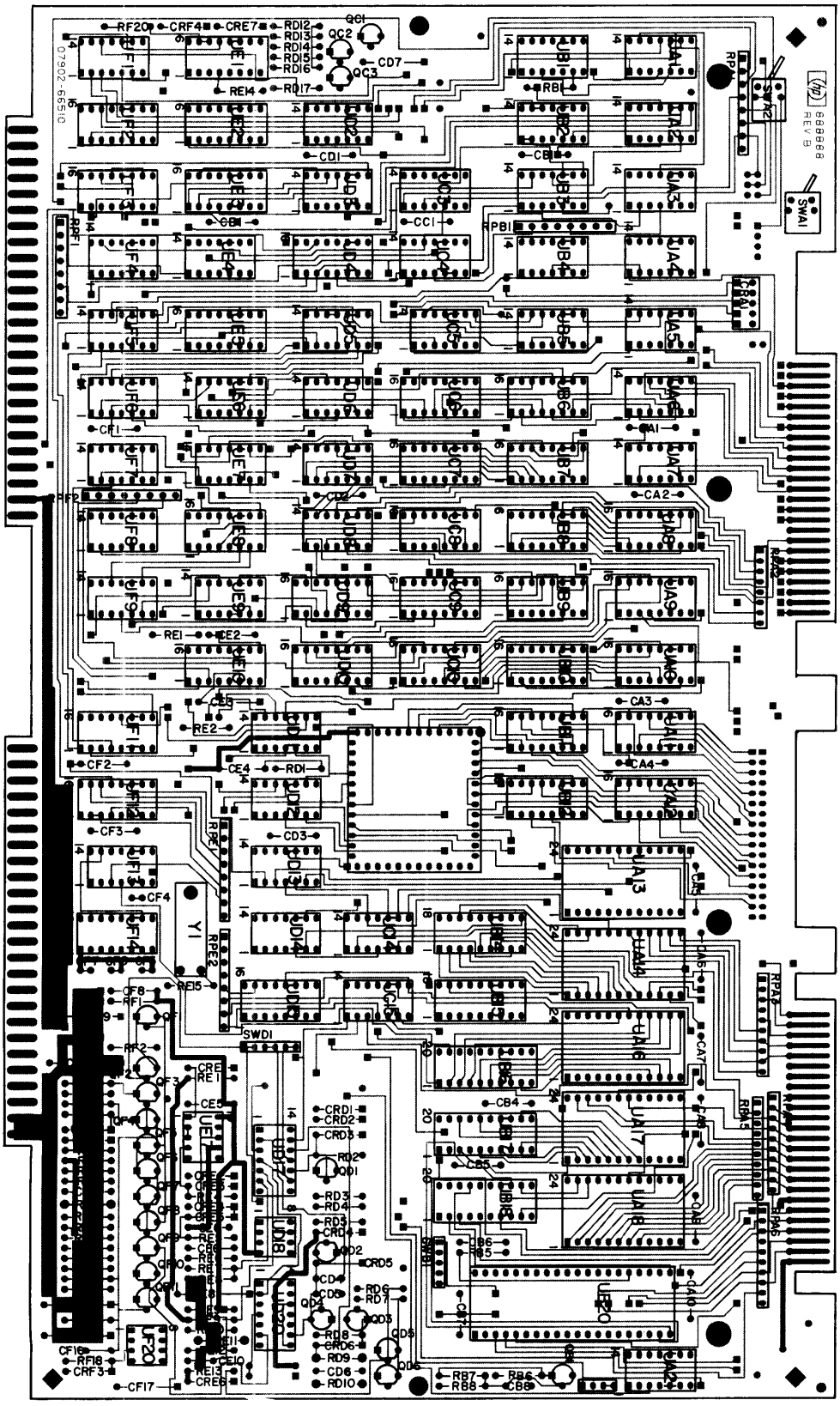


Figure 3-17. Controller Board A1 (07902-66510) Component Locator

Controller Board 07902-66510

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
CA1	9	0160-3847	32	C-F;.01UF;100V
CA2	9	0160-3847		C-F;.01UF;100V
CA3	9	0160-3847		C-F;.01UF;100V
CA4	9	0160-3847		C-F;.01UF;100V
CA5	9	0160-3847		C-F;.01UF;100V
CA6	9	0160-3847		C-F;.01UF;100V
CA7	9	0160-3847		C-F;.01UF;100V
CA8	9	0160-3847		C-F;.01UF;100V
CA9	9	0160-3847		C-F;.01UF;100V
CA10	9	0160-3847		C-F;.01UF;100V
CB1	9	0160-3847		C-F;.01UF;100V
CB4	9	0160-3847		C-F;.01UF;100V
CB5	9	0160-3847		C-F;.01UF;100V
CB6	9	0160-3847		C-F;.01UF;100V
CB7	9	0160-0174	1	C-F;.47UF;25V
CB8	5	0160-2150	1	C-F;33PF;300V
CC1	9	0160-3847		C-F;.01UF;100V
CD1	9	0160-3847		C-F;.01UF;100V
CD2	9	0160-3847		C-F;.01UF;100V
CD3	9	0160-3847		C-F;.01UF;100V
CD4	3	0160-2009	4	C-F;820PF;300V
CD5	8	0160-0363	1	C-F;620PF;300V
CD6	9	0160-3847		C-F;.01UF;100V
CD7	5	0180-1746	6	C-F;15UF;20V
CE1	9	0160-3847		C-F;.01UF;100V
CE2	9	0160-3847		C-F;.01UF;100V
CE3	5	0180-1746		C-F;15UF;20V
CE4	9	0160-3847		C-F;.01UF;100V
CE5	9	0160-3847		C-F;.01UF;100V
CE6	2	0160-0127	1	C-F;1UF;25V
CE7	9	0160-3847		C-F;.01UF;100V
CE8	5	0180-1746		C-F;15UF;20V
CE9	9	0160-3847		C-F;.01UF;100V
CE10	4	0160-2307	1	C-F;47PF;300V
CF1	9	0160-3847		C-F;.01UF;100V
CF2	9	0160-3847		C-F;.01UF;100V
CF3	9	0160-3847		C-F;.01UF;100V
CF4	5	0160-0576	4	C-F;.1UF;50V
CF5	5	0160-0576		C-F;.1UF;50V
CF6	5	0160-0576		C-F;.1UF;50V
CF7	5	0160-0576		C-F;.1UF;50V
CF8	9	0160-3847		C-F;.01UF;100V
CF9	5	0180-1746		C-F;15UF;20V
CF10	5	0180-1746		C-F;15UF;20V
CF11	9	0160-3847		C-F;.01UF;100V
CF12	9	0160-3847		C-F;.01UF;100V
CF13	9	0160-3847		C-F;.01UF;100V
CF14	3	0160-0194	1	C-F;1500PF;200V
CF15	5	0180-1746		C-F;15UF;20V
CF16	7	0160-0362	1	C-F;510PF;300V
CF17	3	0180-0291	1	C-F;1UF;35V
CRA1	2	1990-0622	1	DIODE;LED
CRD1	1	1901-0040	12	DIODE;SWITCHING
CRD2	1	1901-0040		DIODE;SWITCHING
CRD3	1	1901-0040		DIODE;SWITCHING
CRD4	1	1901-0040		DIODE;SWITCHING
CRD5	1	1901-0040		DIODE;SWITCHING

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
CRD6	1	1901-0040		DIODE;SWITCHING
CRD7	1	1901-0040		DIODE;SWITCHING
CRE1	1	1901-0040		DIODE;SWITCHING
CRE2	1	1901-0040		DIODE;SWITCHING
CRE3	1	1901-0040		DIODE;SWITCHING
CRE4	3	1902-3002	2	DIODE;ZENER;2.3V
CRE5	3	1902-3002		DIODE;ZENER;2.3V
CRE6	2	1902-3150	1	DIODE;ZENER;9.09V
CRE7	2	1901-0025	2	DIODE;SWITCHING
CRF1	1	1901-0040		DIODE;SWITCHING
CRF2	1	1901-0040		DIODE;SWITCHING
CRF3	1	1902-3092	1	DIODE;ZENER;4.99V
CRF4	2	1901-0025		DIODE;SWITCHING
QB1	2	1853-0036	1	TRANSISTOR;2N3906
QC1	9	1854-0354	3	TRANSISTOR;SS2077
QC2	9	1854-0354		TRANSISTOR;SS2077
QC3	9	1854-0354		TRANSISTOR;SS2077
QD1	2	1854-0092	3	TRANSISTOR;2N3563
QD2	5	1853-0089	12	TRANSISTOR;2N4917
QD3	5	1853-0089		TRANSISTOR;2N4917
QD4	5	1853-0089		TRANSISTOR;2N4917
QD5	1	1854-0215	1	TRANSISTOR;2N3904
QD6	2	1855-0420	1	TRANSISTOR;?N4391
QF1	2	1854-0092		TRANSISTOR;2N3563
QF2	5	1853-0089		TRANSISTOR;2N4917
QF3	5	1853-0089		TRANSISTOR;2N4917
QF4	5	1853-0089		TRANSISTOR;2N4917
QF5	5	1853-0089		TRANSISTOR;2N4917
QF6	2	1854-0092		TRANSISTOR;2N3563
QF7	5	1853-0089		TRANSISTOR;2N4917
QF8	5	1853-0089		TRANSISTOR;2N4917
QF9	5	1853-0089		TRANSISTOR;2N4917
QF10	5	1853-0089		TRANSISTOR;2N4917
QF11	5	1853-0089		TRANSISTOR;2N4917
RB1	4	0698-3447	1	R-F;422 OHM;1;.125W
RB5	1	0683-1035	5	R-F;10K OHM;5;.25W
RB6	9	0683-2205	1	R-F;2.2K OHM;5;.25W
RB7	1	0683-2215	1	R-F;220 OHM;5;.25W
RB8	1	0683-1225	1	R-F;1.2K OHM;5;.25W
RD1	8	0698-3136	1	R-F;17.8K OHM;1;.125W
RD2	4	0683-1525	2	R-F;1500 OHM;5;.25W
RD3	9	0683-1025	7	R-F;1K OHM;5;.25W
RD4	8	0683-2725	1	R-F;2700 OHM;5;.25W
RD5	1	0683-1035		R-F;10K OHM;5;.25W
RD6	0	0757-0394	1	R-F;51.1 OHM;1;.125W
RD7	3	0683-1045	1	R-F;100K OHM;5;.25W
RD8	1	0757-0428	1	R-F;1.62K OHM;1;.125W
RD9	7	RESISTOR	1	TEST SELECT
RD10	7	RESISTOR	1	TEST SELECT
RD11	9	0683-1025		R-F;1K OHM;5;.25W
RD12	1	0683-1035		R-F;10K OHM;5;.25W
RD13	0	0757-0279	1	R-F;3.16K OHM;1;.125W
RD14	9	0683-1025		R-F;1K OHM;5;.25W
RD15	9	0683-1025		R-F;1K OHM;5;.25W
RD16	9	0757-0400	1	R-F;90.9 OHM;1;.125W
RD17	9	0683-1025		R-F;1K OHM;5;.25W
RE1	2	0683-4725	1	R-F;4.7K OHM;5;.25W
RE2	6	0757-0465	1	R-F;100K OHM;1;.125W
RE3	9	0683-1025		R-F;1K OHM;5;.25W

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
RE4	9	0683-1025		R-F;1K OHM;5;.25W
RE5	5	0757-0422	2	R-F;909 OHM;1;.125W
RE7	8	0698-0083	2	R-F;1.96K OHM;1;.125W
RE8	0	0757-0419	1	R-F;681 OHM;1;.125W
RE9	6	0683-5115	1	R-F;510 OHM;5;.25W
RE10	7	0698-0082	1	R-F;464 OHM;1;.125W
RE11	7	RESISTOR	1	TEST SELECT
RE12	1	0683-5615	1	R-F;560 OHM;5;.25W
RE13	2	0757-0403	1	R-F;121 OHM;1;.125W
RE14	2	0683-1515	2	R-F;150 OHM;5;.25W
RF1	1	0683-2025	1	R-F;2K OHM;5;.25W
RF2	4	0683-1525		R-F;1500 OHM;5;.25W
RF3	7	0683-1015	4	R-F;100 OHM;5;.25W
RF4	7	0683-1015		R-F;100 OHM;5;.25W
RF5	1	0683-1035		R-F;10K OHM;5;.25W
RF6	1	0683-1035		R-F;10K OHM;5;.25W
RF7	6	0683-2715	1	R-F;270 OHM;5;.25W
RF8	7	0683-1015		R-F;100 OHM;5;.25W
RF9	7	0683-1015		R-F;100 OHM;5;.25W
RF10	7	RESISTOR	1	TEST SELECT
RF11	7	0757-0317	1	R-F;1.33K OHM;1;.125W
RF12	4	0757-0273	1	R-F;3.01K OHM;1;.125W
RF13	9	0757-0442	38	R-F;10K OHM;1;.125W
RF14	3	0757-0438		R-F;5.11K OHM;1;.125W
RF15	3	0757-0420	1	R-F;750 OHM;1;.125W
RF16	3	0757-0470	1	R-F;162K OHM;1;.125W
RF17	8	0698-0083		R-F;1.96K OHM;1;.125W
RF18	5	0698-3456	1	R-F;287K OHM;1;.125W
RF19	7	0683-3615	1	R-F;360 OHM;5;.25W
RF20	2	0683-1515		R-F;150 OHM;5;.25W
RPA1	0	1810-0125	5	R-F;NETWORK
RPA2	0	1810-0381	1	R-F;NETWORK
RPA3	8	1810-0280	4	R-F;NETWORK
RPA4	8	1810-0280		R-F;NETWORK
RPA5	8	1810-0280		R-F;NETWORK
RPA6	8	1810-0280		R-F;NETWORK
RPB1	0	1810-0125		R-F;NETWORK
RPE1	0	1810-0125		R-F;NETWORK
RPE2	6	1810-0030	1	R-F;NETWORK
RPF1	0	1810-0125		R-F;NETWORK
RPF2	0	1810-0125		R-F;NETWORK
SWA1	6	3101-1675	2	SWITCH:TGL
SWA2	6	3101-1675		SWITCH:TGL
SWB1	8	1251-5103	1	CONNECTOR;5 PIN;MALE
UA1	8	1820-1287	2	IC:74LS37
UA1	8	1820-1287	2	IC:74LS37
UA2	8	1820-1211	1	IC:74LS86
UA3	8	1820-1112	5	IC:74LS74
UA4	6	1820-1053	2	IC:7414
UA5	9	1820-1197	3	IC:74LS00
UA6	7	1820-0577	1	IC:SN7416
UA7	7	1820-0577		IC:SN7416
UA8	5	1820-1276	4	IC:74LS194
UA9	9	1820-1444	2	IC:74LS298
UA10	5	1820-1276		IC:74LS194
UA11	3	1820-2058	4	IC:TRANSCEIVER
UA12	3	1820-2058		IC:TRANSCEIVER
UA14	9	1816-1237	4	IC:PROM (SEE NOTE 1)
UA16	9	1816-1237		IC:PROM (SEE NOTE 1)

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
UA17	9	1816-1237		IC:PROM (SEE NOTE 1)
UA18	9	1816-1237		IC:PROM (SEE NOTE 1)
UA21	6	1820-0683	1	IC:74S04
UB1	0	1810-0315	1	IC:DELAY LINE
UB2	8	1820-1112		IC:74LS74
UB3	8	1820-1112		IC:74LS74
UB4	1	1820-1206	1	IC:74LS27
UB5	9	1820-1197		IC:74LS00
UB6	8	1820-1196	5	IC:74LS174
UB7	3	1820-1216	1	IC:74LS138
UB8	5	1820-1276		IC:74LS194
UB9	9	1820-1444		IC:74LS298
UB10	5	1820-1276		IC:74LS194
UB11	3	1820-2058		IC:TRANSCEIVER
UB12	3	1820-2058		IC:TRANSCEIVER
UB14	1	1818-0443	2	IC:MEMORY
UB15	1	1818-0443		IC:MEMORY
UB16	4	1820-2075	1	IC:74LS245
UB17	3	1820-2024	2	IC:74LS244
UB18	3	1820-2024		IC:74LS244
UB20	3	1820-2298	1	IC:Z80A:CPU
UC3	1	1820-1199	5	IC:74LS04
UC4	5	1820-1193	1	IC:74LS197
UC5	1	1820-1199		IC:74LS04
UC6	8	1820-1196		IC:74LS174
UC7	8	1820-1196		IC:74LS174
UC8	8	1820-1196		IC:74LS174
UC9	9	1820-1238	4	IC:74LS253
UC10	9	1820-1238		IC:74LS253
UC12	1	1820-2147	1	IC:1AA6-6004
UC14	9	1820-1204	1	IC:74LS20
UC15	7	1820-0577		IC:SN7416
UD2	2	1820-1207	1	IC:74LS30
UD3	6	1820-1433	1	IC:74LS164
UD4	5	1820-1440	1	IC:74LS279
UD5	7	1820-1210	2	IC:74LS51
UD6	7	1820-1202	2	IC:74LS10
UD7	4	1820-1275	1	IC:74LS260
UD8	6	1820-1053		IC:7414
UD9	9	1820-1238		IC:74LS253
UD10	9	1820-1238		IC:74LS253
UD11	6	1820-1144	1	IC:74LS02
UD12	8	1820-1287		IC:74LS37
UD13	6	1820-1201	1	IC:74LS08
UD14	7	1820-1202		IC:74LS10
UD15	3	1820-1282	1	IC:74LS109
UD17	7	1820-0577		IC:SN7416
UD18	4	1820-0475	1	IC:LINEAR
UD20	4	1821-0001	1	IC:CA3046
UE1	9	1820-1212	2	IC:74LS112
UE2	7	1820-1195	2	IC:74LS175
UE3	4	1820-1217	1	IC:74LS151
UE4	9	1820-2096	2	IC:74LS393
UE5	8	1820-1419	1	IC:74LS85
UE6	9	1820-1197		IC:74LS00
UE7	1	1820-1199		IC:74LS04
UE8	7	1820-1195		IC:74LS175
UE9	1	1820-1199		IC:74LS04
UE10	4	1820-1423	1	IC:74LS123

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
UE17	6	1820-0427	1	IC:MC1496
UF1	6	1820-1201		IC:74LS08
UF2	1	1816-0710	1	IC:PROM (SEE NOTE 1)
UF3	8	1820-1196		IC:74LS174
UF4	9	1820-2096		IC:74LS393
UF5	8	1820-1203	1	IC:74LS11
UF6	8	1820-1112		IC:74LS74
UF7	8	1820-1112		IC:74LS74
UF8	3	1820-2016	1	IC:CRC GEN
UF9	7	1820-1210		IC:74LS51
UF11	1	1820-1470	1	IC:74LS157
UF12	9	1820-1212		IC:74LS112
UF13	1	1820-1199		IC:74LS04
UF14	3	1820-1977	1	IC:MC12061
UF20	8	1826-0021	1	IC:OP AMP
Y1	0	0410-1031	1	CRYSTAL

Controller Board Assembly (P/N 07902-66520)

Introduction

This section provides interface information, schematic diagrams and replaceable parts list for controller board P/N 07902-66520.

Interface Information

Refer to Figure 3-15 for the connector locations. Table 3-14 describes the connector pin assignments.

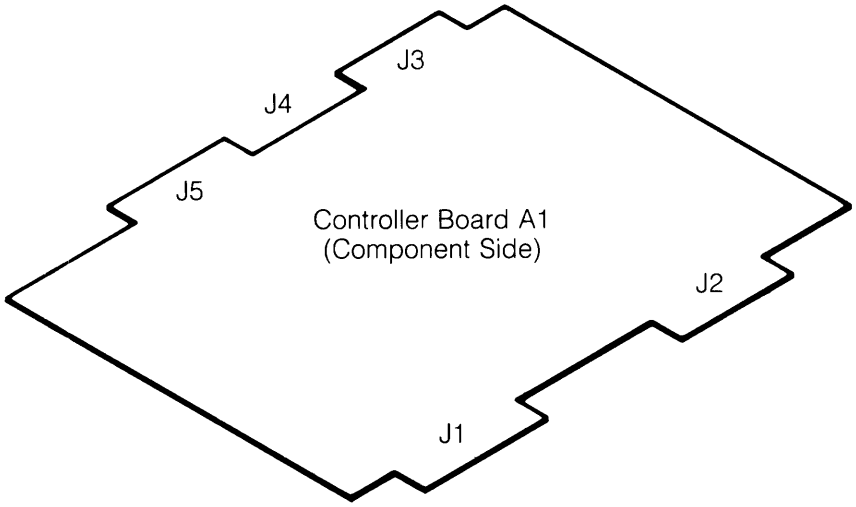


Figure 3-18. Controller Board A1 (07902-66520) Connectors

Table 3-7. 07902-66520 Connector Pin Assignments

HP-IB Connector

J4

PIN	SIGNAL	PIN	SIGNAL
2	SPARE	20	DIO8
4	ATN	22	DIO7
6	SRQ	24	DIO6
8	NDAC	26	DIO5
10	NRFD	28	DIO4
12	IFC	30	DIO3
14	REN	32	DIO2
16	DAV	34	DIO1
18	EOI		

J3

PIN	SIGNAL	PIN	SIGNAL
A	RD	1	GND
B	RESET	2	MI
C	INT	3	NMI
D	RFSH	4	WR
E	WAIT	5	IORQ

F	GND	6	MREQ
H	HALT	7	GND
J	A0	8	A1
K	A2	9	A3
L	A4	10	A5
M	A6	11	A7
N	A8	12	A9
P	A10	13	A11
R	A12	14	A13
S	A14	15	A15
T	GND	16	GND
U	GND	17	GND
V	GND	18	GND
W	GND	19	GND
X	GND	20	GND
Y	D7	21	D6
Z	D5	22	D4
AA	D3	23	D2
BB	D1	24	D0
CC	GND	25	HMHZ

J5

PIN	SIGNAL	PIN	SIGNAL
A	PON	1	WPRT
B	TRACK0	2	READY
C	GND	3	SPIN
D	RSPIN	4	INDEX
E	GND	5	DLCK
F	HDACT	6	PHIA
H	GND	7	WRIT
J	DSLV	8	PHIB
K	GND	9	HED1
L	DSL2	10	LDCT
M	GND	11	DSL1
N	PONR	12	DSL0
P	GND	13	GND
S	GND	14	GND
T	LDATA	15	HDATA

J1

PIN	SIGNAL	PIN	SIGNAL
B	GND	2	GND
C	GND	3	GND
BB	−5V	24	−5V
CC	+12V	25	+12V

J2

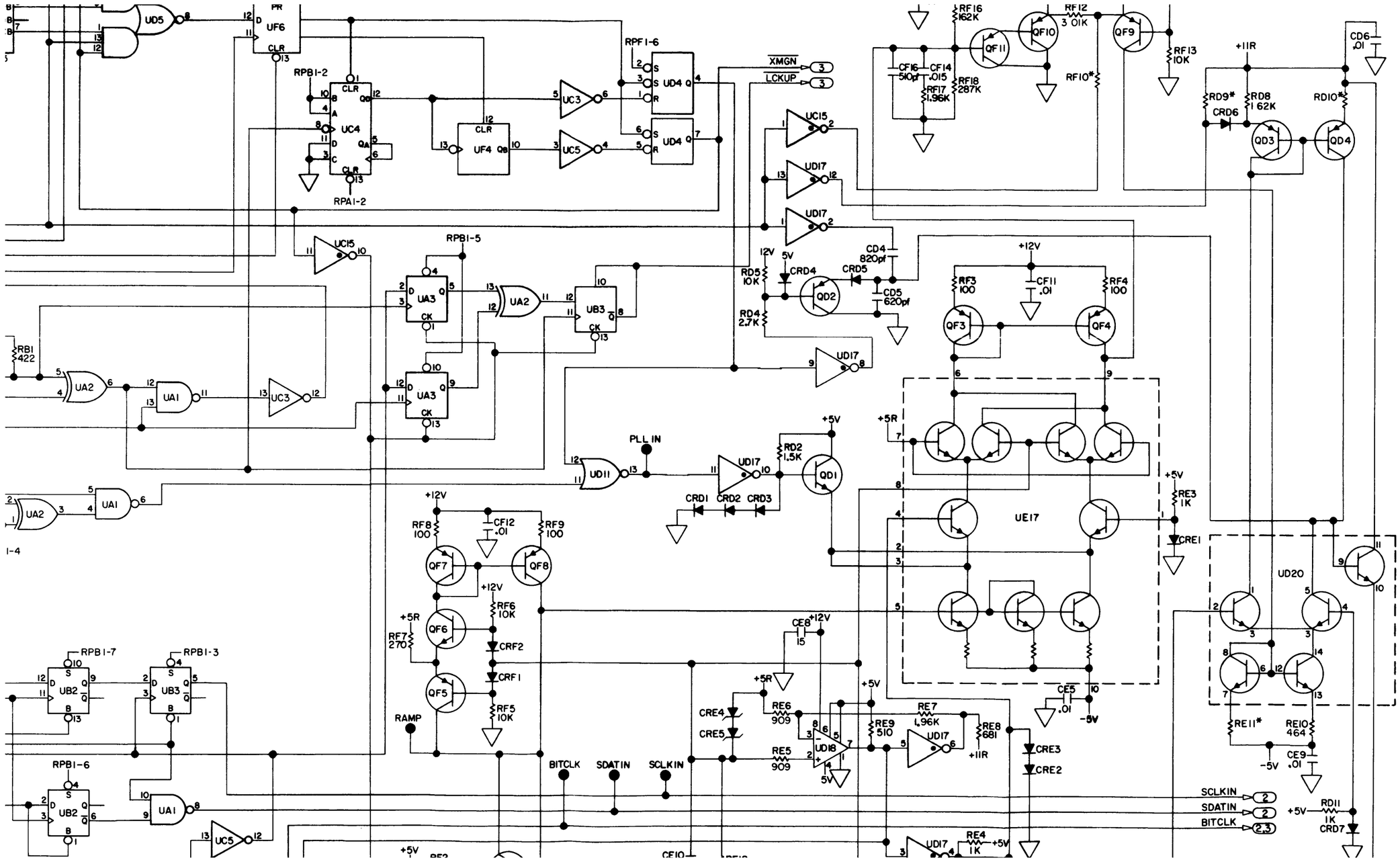
PIN	SIGNAL	PIN	SIGNAL
A	+12V	1	+12V
Y	POP	21	N.C.
Z	GND	22	GND
AA	GND	23	GND
BB	+5V	24	+5V
CC	+5V	25	+5V

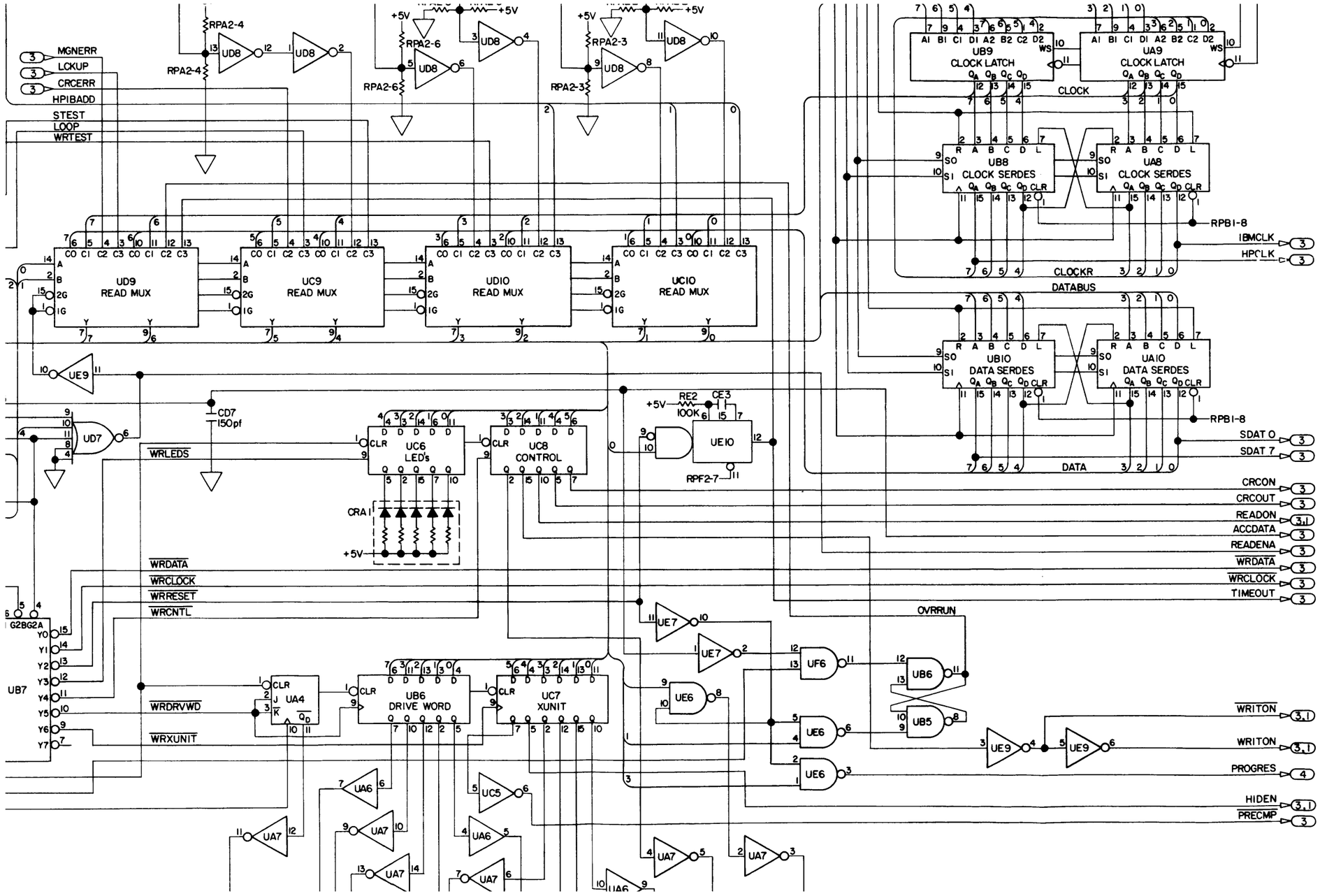
All other pins on J1
and J2 are N.C.

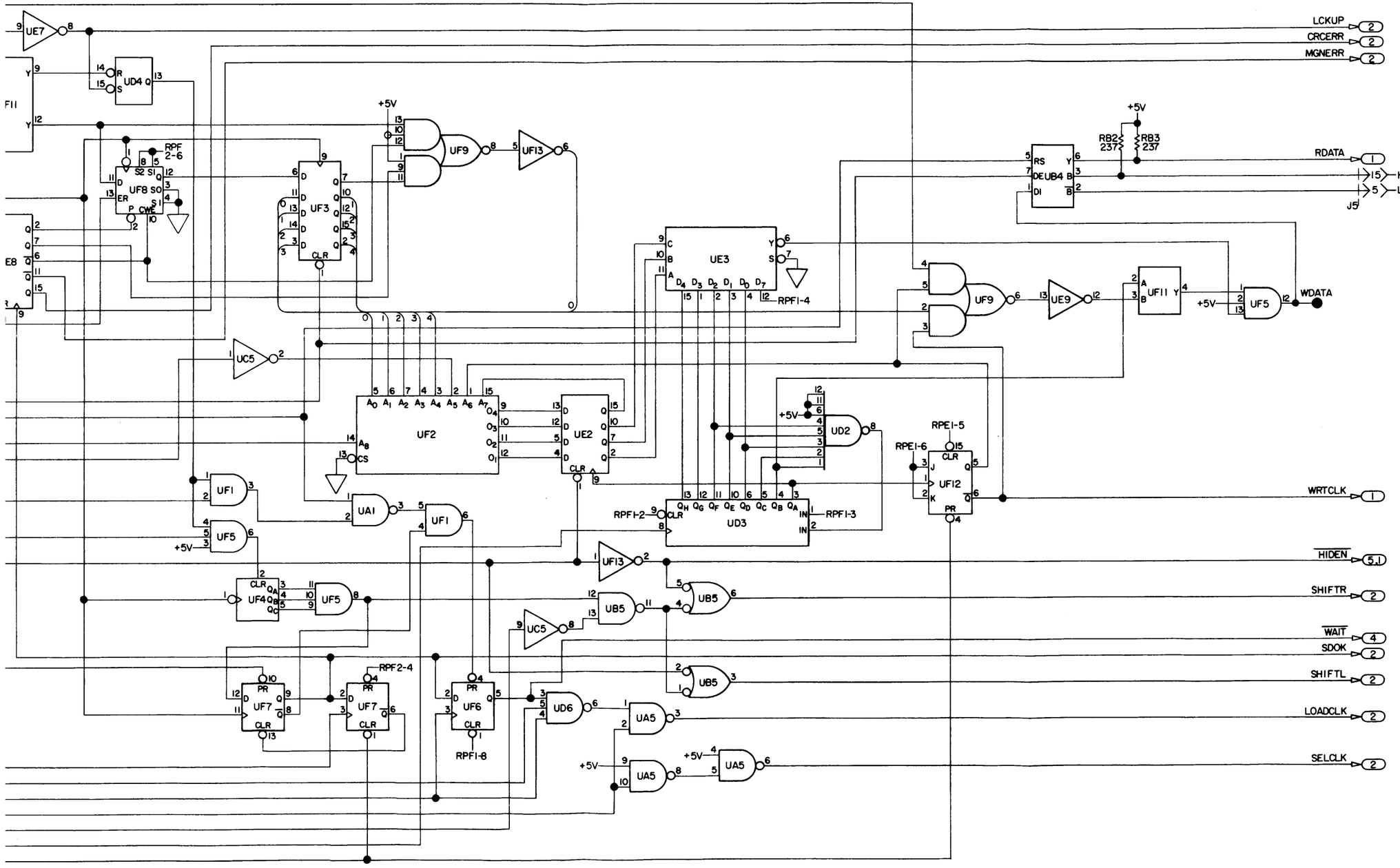
Schematic Diagrams

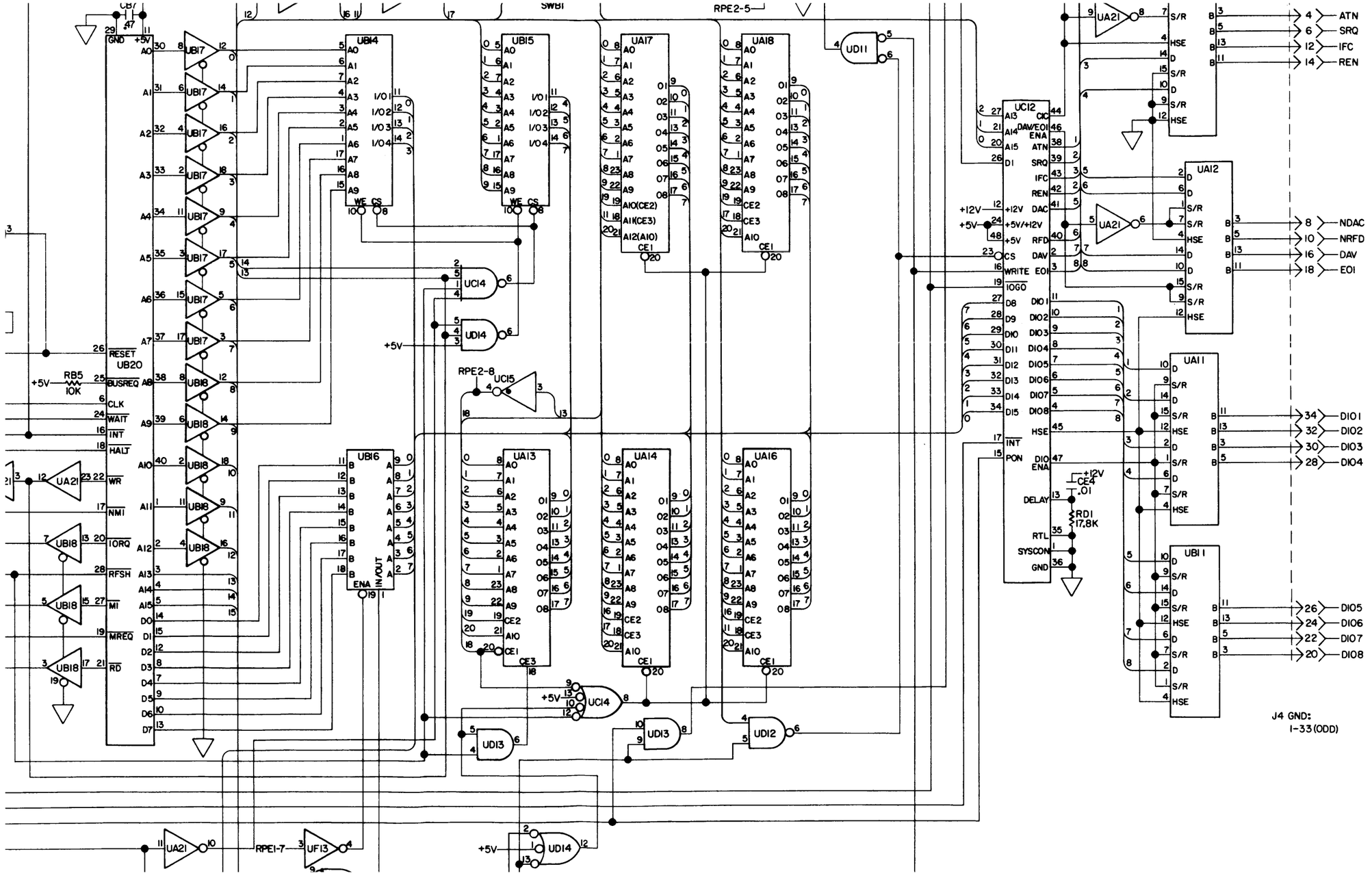
Introduction

This section contains the circuit diagrams for controller board P/N 07902-66520.


UD5
UF6
PR
CLR
RPB1-2
RPA1-2
UC4
UF4 QB
UC3
UC5
RPF1-6
UD4 Q
XMGN
LCKUP
UC15
UDI7
RF16 162K
RF12 3 01K
QF10
QF11
QF9
CF16 510pf
CF14 .015
RF17 1.96K
RF18 287K
RF10*
RF13 10K
+11R
RD9*
RD8 1 62K
RD10*
CRD6
QD3
QD4
CD6 .01
RPB1-5
UA3
UA2
UB3
CD4 820pf
CD5 620pf
CRD4
CRD5
QD2
12V
5V
RD5 10K
RD4 2.7K
+12V
RF3 100
CF11 .01
RF4 100
QF3
QF4
RBI 422
UA1
UE17
RE3 1K
CRE1
UD20
RF8 100
CF12 .01
RF9 100
QF7
QF8
RF6 10K
CRF2
CRF1
QF6
QF5
RF7 270
RF5 10K
RAMP
CE8
RPB1-7
RPB1-3
UB2
RPB1-6
BITCLK
SDATIN
SCLKIN
RE6 909
RE5 909
CRE4
CRE5
RE7 4.96K
RE9 510
RE8 681
UD18
CE5 .01
-5V
CRE3
CRE2
RE11*
RE10 464
CE9 .01
RD11 1K
CRD7
PLL IN
UD11
RD2 1.5K
QD1
CRD1
CRD2
CRD3
+5R
+5V
RE4 1K
CE10
1-4


MGNERR
LCKUP
CRCERR
HPIBADD
STEST
LOOP
WRTEST
RPA2-4
RPA2-6
RPA2-3
+5V
UD8
UD9 READ MUX
UC9 READ MUX
UDIO READ MUX
UCIO READ MUX
UE9
UD7
CD7 150pf
WRLEDS
UC6 LED's
UC8 CONTROL
CRA1
RE2 100K
CE3
UE10
RPF2-7
UB9 CLOCK LATCH
UA9 CLOCK LATCH
CLOCK
UB8 CLOCK SERDES
UA8 CLOCK SERDES
RPB1-8
IBMCLK
HPCLK
CLOCKR
DATABUS
UBIO DATA SERDES
UAIO DATA SERDES
SDAT 0
SDAT 7
DATA
CRCON
CRCOUT
READON
ACCDATA
READENA
WRDATA
WRCLOCK
TIMEOUT
OVRRUN
UB7
G2BG2A
Y0
Y1
Y2
Y3
Y4
Y5
Y6
Y7
WRDRVWD
WRXUNIT
UA4
UB6 DRIVE WORD
UC7 XUNIT
UE7
UE6
UF6
UB6
UB5
UE9
WRITON
PROGRES
HIDEN
PRECMP
UA6
UA7
UC5


LCKUP
CRCERR
MGNERR
RDATA
HDATA
LDATA
J5
WDATA
WRTCLK
HIDEN
SHIFTR
WAIT
SDOK
SHIFTL
LOADCLK
SELCLK
+5V
RB2 237
RB3 237
UE7
UD4
UF8
UF3
UF9
UF13
UE3
RPF1-4
UE9
UF11
UF5
UB4
UC5
UF2
UE2
UF1
UA1
UF4
UB5
UF7
UF6
UD6
UA5
UD2
UD3
RPE1-5
RPE1-6
UF12
RPF1-2
RPF1-3
RPF2-4
RPF1-8


SWB1
RPE2-5
RPE2-8
RPE1-7
+5V
+12V
GND
RB5
10K
RESET
BUSREQ
CLK
WAIT
INT
HALT
NMI
MI
MREQ
RFSH
WR
RD
IORQ
UB20
UBI7
UBI8
UBI4
UBI5
UBI6
UBI1
UA11
UA12
UA13
UA14
UA16
UA17
UA18
UA21
UC12
UC14
UC15
UD11
UD12
UD13
UD14
UF13
CE4
.01
RD1
17.8K
DELAY
RTL
SYSCON
DAV/EOI ENA
DAC
RFD
DAV
EOI
WRITE
IOGO
DIO ENA
ATN
SRQ
IFC
REN
NDAC
NRFD
DAV
EOI
DIO1
DIO2
DIO3
DIO4
DIO5
DIO6
DIO7
DIO8
J4 GND:
1-33(ODD)

+12V
UF20
+5R
CE6
CE7 .01
+11R
CF17
+5V
+12V
-5V
GND
15
CF6 .10
CF5 .10
CF7 .10
CF4 .10
UF14
Y1
UF13
UF11
8MHZ
RPE2-2
RPE1-8
RPE1-4
UF12
PR
CLR
+5V
UD12
4MHZ
CB8 33pf
RB7 220
RB6 22
RB8 1.2K
Q81
SWB2
SWB1
UA21
J2 50 4MHZ
Z80CLK
RPA6-9 0
RPA5-9 1
RPA6-8 2
RPA5-8 3
RPA6-7 4
RPA5-7 5
RPA6-6 6
RPA5-6 7
RPA6-5 8
RPA5-5 9
RPA6-4 10
RPA5-4 11
RPA6-3 12
RPA5-3 13
RPA6-2 14
RPA5-2 15
10K
RPA4-3 0
RPA4-4 1
RPA4-5 2
RPA4-6 3
RPA4-7 4
RPA4-8 5
RPA4-9 6
RPA4-10 7
10K
RPA7-6
RPA7-2
RPA7-9
RPA7-3
RPA7-7
RPA6-10
RPA7-5
RPA7-8
RPA5-10
RPA7-10
J3
J3 GND: 1,7,16,17,18, 19,20,F,T,U, V,W,X,CC
J A0
8 A1
K A2
9 A3
L A4
10 A5
M A6
11 A7
N A8
12 A9
P A10
13 A11
R A12
14 A13
S A14
15 A15
24 D0
BB D1
23 D2
AA D3
22 D4
Z D5
21 D6
Y D7
C INT
H HALT
B PONRES
4 WR
3 NMI
5 IORQ
D RFSH
2 MI
6 MREQ
A RD

Replaceable Parts

Introduction

The controller board P/N 07902-66520 parts list is provided in this section. The total quantity of a part is shown only the first time it is used on this assembly.

The number shown in the "CD" column is the parts check digit. Include the check digit number with the part number when ordering a part from HP.

Reference designators are listed in alphanumeric order in lieu of item numbers for printed circuit assembly parts.

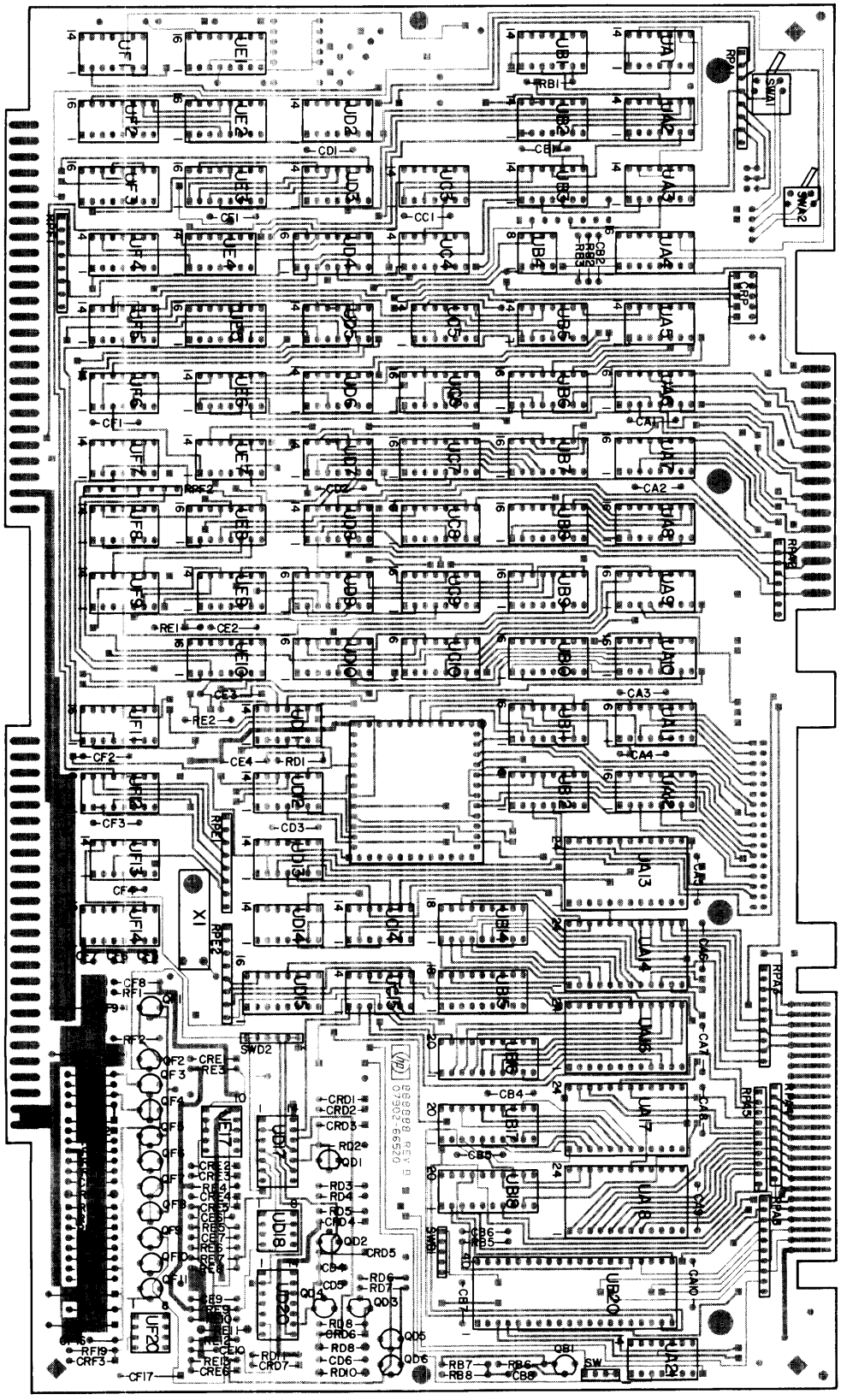


Figure 3-20. Controller Board A1 (07902-66520) Component Locator

Controller Board 07902-66520

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
CA1	9	0160-3847	33	C-F;.01UF;100V
CA2	9	0160-3847		C-F;.01UF;100V
CA3	9	0160-3847		C-F;.01UF;100V
CA4	9	0160-3847		C-F;.01UF;100V
CA5	9	0160-3847		C-F;.01UF;100V
CA6	9	0160-3847		C-F;.01UF;100V
CA7	9	0160-3847		C-F;.01UF;100V
CA8	9	0160-3847		C-F;.01UF;100V
CA9	9	0160-3847		C-F;.01UF;100V
CA10	9	0160-3847		C-F;.01UF;100V
CB1	9	0160-3847		C-F;.01UF;100V
CB2	9	0160-3847		C-F;.01UF;100V
CB4	9	0160-3847		C-F;.01UF;100V
CB5	9	0160-3847		C-F;.01UF;100V
CB6	9	0160-3847		C-F;.01UF;100V
CB7	9	0160-0174	1	C-F;.47UF;25V
CB8	5	0160-2150	1	C-F;33PF;300V
CC1	9	0160-3847		C-F;.01UF;100V
CD1	9	0160-3847		C-F;.01UF;100V
CD2	9	0160-3847		C-F;.01UF;100V
CD3	9	0160-3847		C-F;.01UF;100V
CD4	3	0160-2009	1	C-F;820PF;300V
CD5	8	0160-0363	1	C-F;620PF;300V
CD6	9	0160-3847		C-F;.01UF;100V
CD7	2	0160-4814	1	C-F;150PF;100V
CE1	9	0160-3847		C-F;.01UF;100V
CE2	9	0160-3847		C-F;.01UF;100V
CE3	5	0180-1746	5	C-F;15UF;20V
CE4	9	0160-3847		C-F;.01UF;100V
CE5	9	0160-3847		C-F;.01UF;100V
CE6	2	0160-0127	1	C-F;1UF;25V
CE7	9	0160-3847		C-F;.01UF;100V
CE8	5	0180-1746		C-F;15UF;20V
CE9	9	0160-3847		C-F;.01UF;100V
CE10	4	0160-2307	1	C-F;47PF;300V
CF1	9	0160-3847		C-F;.01UF;100V
CF2	9	0160-3847		C-F;.01UF;100V
CF3	9	0160-3847		C-F;.01UF;100V
CF4	5	0160-0576	4	C-F;.1UF;50V
CF5	5	0160-0576		C-F;.1UF;50V
CF6	5	0160-0576		C-F;.1UF;50V
CF7	5	0160-0576		C-F;.1UF;50V
CF8	9	0160-3847		C-F;.01UF;100V
CF9	5	0180-1746		C-F;15UF;20V
CF10	5	0180-1746		C-F;15UF;20V
CF11	9	0160-3847		C-F;.01UF;100V
CF12	9	0160-3847		C-F;.01UF;100V
CF13	9	0160-3847		C-F;.01UF;100V
CF14	3	0160-0194	1	C-F;1500PF;200V
CF15	5	0180-1746		C-F;15UF;20V
CF16	7	0160-0362	1	C-F;510PF;300V
CF17	3	0180-0291	1	C-F;1UF;35V
CRA1	2	1990-0622	1	DIODE;LED
CRD1	1	1901-0040	12	DIODE;SWITCHING
CRD2	1	1901-0040		DIODE;SWITCHING
CRD3	1	1901-0040		DIODE;SWITCHING
CRD4	1	1901-0040		DIODE;SWITCHING

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
CRD5	1	1901-0040		DIODE:SWITCHING
CRD6	1	1901-0040		DIODE:SWITCHING
CRD7	1	1901-0040		DIODE:SWITCHING
CRE1	1	1901-0040		DIODE:SWITCHING
CRE2	1	1901-0040		DIODE:SWITCHING
CRE3	1	1901-0040		DIODE:SWITCHING
CRE4	3	1902-3002	2	DIODE;ZENER:2.3V
CRE5	3	1902-3002		DIODE;ZENER:2.3V
CRE6	2	1902-3150	1	DIODE;ZENER:9.09V
CRF1	1	1901-0040		DIODE:SWITCHING
CRF2	1	1901-0040		DIODE:SWITCHING
CRF3	1	1902-3092	1	DIODE;ZENER:4.99V
QB1	2	1853-0036	1	TRANSISTOR:2N3906
QD1	2	1854-0092	3	TRANSISTOR:2N3563
QD2	5	1853-0089	12	TRANSISTOR:2N4917
QD3	5	1853-0089		TRANSISTOR:2N4917
QD4	5	1853-0089		TRANSISTOR:2N4917
QD5	1	1854-0215	1	TRANSISTOR:2N3904
QD6	2	1855-0420	1	TRANSISTOR:2N4391
QF1	2	1854-0092		TRANSISTOR:2N3563
QF2	5	1853-0089		TRANSISTOR:2N4917
QF3	5	1853-0089		TRANSISTOR:2N4917
QF4	5	1853-0089		TRANSISTOR:2N4917
QF5	5	1853-0089		TRANSISTOR:2N4917
QF6	2	1854-0092		TRANSISTOR:2N3563
QF7	5	1853-0089		TRANSISTOR:2N4917
QF8	5	1853-0089		TRANSISTOR:2N4917
QF9	5	1853-0089		TRANSISTOR:2N4917
QF10	5	1853-0089		TRANSISTOR:2N4917
QF11	5	1853-0089		TRANSISTOR:2N4917
RB1	4	0698-3447	1	R-F:422 OHM:1;.125W
RB2	9	0698-3442	2	R-F:237 OHM:1;.125W
RB3	9	0698-3442		R-F:237 OHM:1;.125W
RB5	1	0683-1035	4	R-F:10K OHM:5;.25W
RB6	9	0683-2205	1	R-F:2.2K OHM:5;.25W
RB7	1	0683-2215	1	R-F:220 OHM:5;.25W
RB8	1	0683-1225	1	R-F:1.2K OHM:5;.25W
RD1	8	0698-3136	1	R-F:17.8K OHM:1;.125W
RD2	4	0683-1525	1	R-F:1500 OHM:5;.25W
RD3	9	0683-1025		R-F:1K OHM:5;.25W
RD4	8	0683-2725	1	R-F:2700 OHM:5;.25W
RD5	1	0683-1035		R-F:10K OHM:5;.25W
RD6	0	0757-0394	1	R-F:51.1 OHM:1;.125W
RD7	3	0683-1045	1	R-F:100K OHM:5;.25W
RD8	1	0757-0428	1	R-F:1.62K OHM:1;.125W
RD9	7	RESISTOR	1	TEST SELECT
RD10	7	RESISTOR	1	TEST SELECT
RD11	9	0683-1025		R-F:1K OHM:5;.25W
RE1	2	0683-4725	1	R-F:4.7K OHM:5;.25W
RE2	6	0757-0465	1	R-F:100K OHM:1;.125W
RE3	9	0683-1025		R-F:1K OHM:5;.25W
RE4	9	0683-1025	4	R-F:1K OHM:5;.25W
RE5	5	0757-0422	2	R-F:909 OHM:1;.125W
RE6	5	0757-0422		R-F:909 OHM:1;.125W
RE7	8	0698-0083	2	R-F:1.96K OHM:1;.125W
RE8	0	0757-0419	1	R-F:681 OHM:1;.125W
RE9	6	0683-5115	1	R-F:510 OHM:5;.25W
RE10	7	0698-0082	2	R-F:464 OHM:1;.125W
RE11	7	RESISTOR	1	TEST SELECT

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
RE12	1	0683-5615	1	R-F:560 OHM:5:.25W
RE13	2	0757-0403	1	R-F:121 OHM:1:.125W
RF1	7	0757-0416	1	R-F:511 OHMS:1:.125W
RF2	2	0698-3445	1	R-F:348 OHMS:1:.125W
RF3	7	0683-1015	4	R-F:100 OHM:5:.25W
RF4	7	0683-1015	1	R-F:100 OHM:5:.25W
RF5	1	0683-1035		R-F:10K OHM:5:.25W
RF6	1	0683-1035		R-F:10K OHM:5:.25W
RF7	6	0683-2715		R-F:270 OHM:5:.25W
RF8	7	0683-1015		R-F:100 OHM:5:.25W
RF9	7	0683-1015		R-F:100 OHM:5:.25W
RF10	7	RESISTOR	1	TEST SELECT
RF11	7	0757-0317	1	R-F:1.33K OHM:1:.125W
RF12	4	0757-0273	1	R-F:3.01K OHM:1:.125W
RF13	9	0757-0442	1	R-F:10K OHM:1:.125W
RF14	3	0757-0438	1	R-F:5.11K OHM:1:.125W
RF15	3	0757-0420	1	R-F:750 OHM:1:.125W
RF16	3	0757-0470	1	R-F:162K OHM:1:.125W
RF18	5	0698-3456	1	R-F:287K OHM:1:.125W
RF19	7	0683-3615	1	R-F:360 OHM:5:.25W
RPA1	0	1810-0125	5	R-F:NETWORK
RPA2	0	1810-0381	1	R-F:NETWORK
RPA3	8	1810-0280	4	R-F:NETWORK
RPA4	8	1810-0280		R-F:NETWORK
RPA5	8	1810-0280		R-F:NETWORK
RPA6	8	1810-0280		R-F:NETWORK
RPB1	0	1810-0125		R-F:NETWORK
RPE1	0	1810-0125		R-F:NETWORK
RPE2	6	1810-0030	1	R-F:NETWORK
RPF1	0	1810-0125		R-F:NETWORK
RPF2	0	1810-0125		R-F:NETWORK
SWA1	6	3101-1675	1	SWITCH:TGL
SWA2	6	3101-1675		SWITCH:TGL
UA1	8	1820-1287	1	IC:74LS37
UA2	8	1820-1211	1	IC:74LS86
UA3	8	1820-1112		IC:74LS74
UA4	6	1820-1300	1	IC:74LS195
UA5	9	1820-1197	2	IC:74LS00
UA6	2	1820-2007	1	IC:74366
UA7	6	1820-1368	1	IC:74365
UA8	5	1820-1276	4	IC:74LS194
UA9	9	1820-1444	2	IC:74LS298
UA10	5	1820-1276		IC:74LS194
UA11	3	1820-2058	4	IC:TRANSCEIVER
UA12	3	1820-2058		IC:TRANSCEIVER
UA14	9	1816-1237	4	IC:PROM (SEE NOTE 1)
UA16	9	1816-1237		IC:PROM (SEE NOTE 1)
UA17	9	1816-1237		IC:PROM (SEE NOTE 1)
UA18	9	1816-1237		IC:PROM (SEE NOTE 1)
UA21	6	1820-0683	1	IC:74S04
UB1	0	1810-0315	1	IC:DELAY LINE
UB2	8	1820-1112	5	IC:74LS74
UB3	8	1820-1112		IC:74LS74
UB4	5	1820-2159	1	IC:75117
UB6	8	1820-1196		IC:74LS174
UB7	3	1820-1216	1	IC:74LS138
UB8	5	1820-1276		IC:74LS194
UB9	9	1820-1444		IC:74LS298
UB10	5	1820-1276		IC:74LS194

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
UB11	3	1820-2058		IC:TRANSCEIVER
UB12	3	1820-2058		IC:TRANSCEIVER
UB14	1	1818-0443	2	IC:MEMORY
UB15	1	1818-0443		IC:MEMORY
UB16	4	1820-2075	1	IC:74LS245
UB17	3	1820-2024	2	IC:74LS244
UB20	3	1820-2298	1	IC:Z80A:CPU
UC3	1	1820-1199	5	IC:74LS04
UC4	5	1820-1193	1	IC:74LS197
UC5	1	1820-1199		IC:74LS04
UC6	8	1820-1196	5	IC:74LS174
UC7	8	1820-1196		IC:74LS174
UC8	8	1820-1196		IC:74LS174
UC9	9	1820-1238	4	IC:74LS253
UC10	9	1820-1238		IC:74LS253
UC12	1	1820-2147	1	IC:1AA6-6004
UC14	9	1820-1204	1	IC:74LS20
UD2	2	1820-1207	1	IC:74LS30
UD3	6	1820-1433	1	IC:74LS164
UD4	5	1820-1440	1	IC:74LS279
UD5	7	1820-1210	2	IC:74LS51
UD6	7	1820-1202	2	IC:74LS10
UD7	4	1820-1275	1	IC:74LS260
UD8	6	1820-1053	1	IC:7414
UD9	9	1820-1238		IC:74LS253
UD10	9	1820-1238		IC:74LS253
UD11	6	1820-1144	1	IC:74LS02
UD12	8	1820-1287		IC:74LS37
UD13	6	1820-1201	2	IC:74LS08
UD15	3	1820-1282	1	IC:74LS109
UD17	7	1820-0577	2	IC:SN7416
UD18	4	1820-0475	1	IC:LINEAR
UD20	4	1821-0001	1	IC:CA3046
UE2	7	1820-1195	8	IC:74LS175
UE3	4	1820-1217	1	IC:74LS151
UE4	9	1820-2096	2	IC:74LS393
UE5	8	1820-1419	1	IC:74LS85
UE6	9	1820-1197		IC:74LS00
UE7	1	1820-1199		IC:74LS04
UE8	7	1820-1195		IC:74LS175
UE9	1	1820-1199		IC:74LS04
UE10	4	1820-1423	1	IC:74LS123
UE17	6	1820-0427	1	IC:MC1496
UF1	6	1820-1201		IC:74LS08
UF2	1	1816-0710	1	IC:PROM (SEE NOTE 1)
UF3	8	1820-1196		IC:74LS174
UF4	9	1820-2096		IC:74LS393
UF5	8	1820-1203	1	IC:74LS11
UF6	8	1820-1112		IC:74LS74
UF7	8	1820-1112		IC:74LS74
UF8	3	1820-2016	1	IC:CRC GEN
UF9	7	1820-1210		IC:74LS51
UF11	1	1820-1470	1	IC:74LS157
UF12	9	1820-1212	1	IC:74LS112
UF13	1	1820-1199		IC:74LS04
UF14	3	1820-1977	1	IC:MC12061
UF20	8	1826-0021	1	IC:OP AMP
Y1	0	0410-1031	1	CRYSTAL

Controller Board Assembly (P/N 07902-66501)

Introduction

This section provides interface information, schematic diagrams and replaceable parts list for controller board P/N 07902-66501.

Addressing

The address of each individual drive is composed of two parts, the bus address and the drive or unit number. Each of these parts is set on a different switch in a different location, using a different set of rules. Since it is essential that this address be set correctly, these will be covered in detail.

Bus Address

The various devices on an HP-IB channel are differentiated by the bus address portion of the address. The drive must use a bus address between 0 and 7. The bus address select switch is located on the front of the controller board (see Figure 3-17). Removing the front cover provides access to the switch. Note that although as many as four drives may be controlled by one controller board, they all have the same bus address. If several controller boards are connected to an HP-IB, each must have a different bus address. If you change the bus address, change the number on the front panel, also.

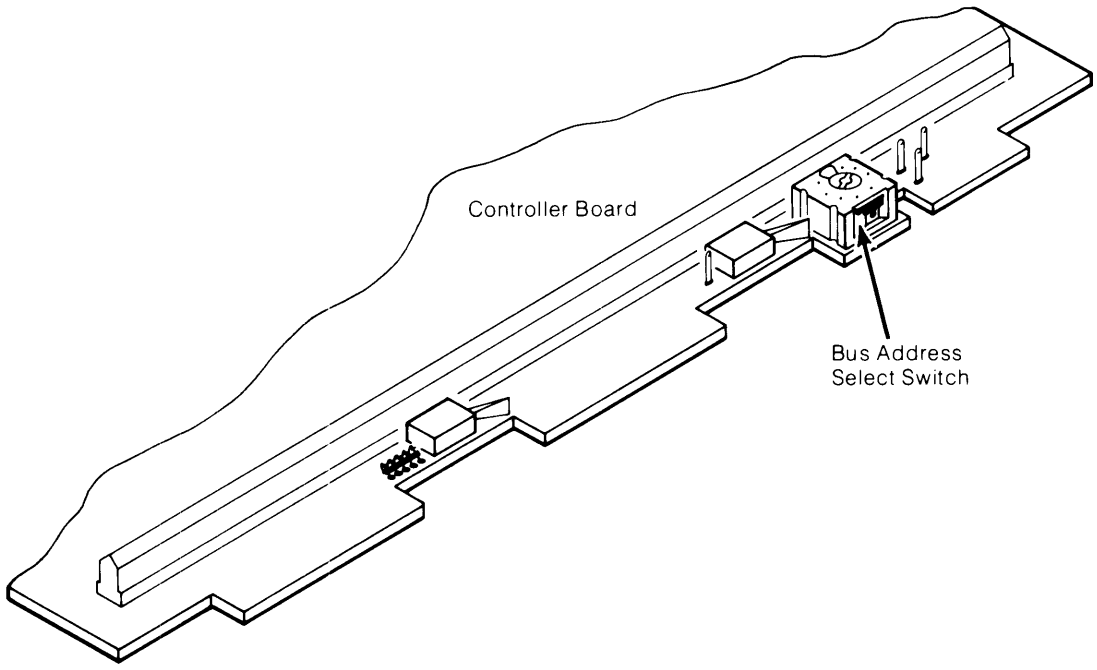


Figure 3-21. Bus Address Selector Switch

Interface Information

Refer to Figure 3-18 for the connector locations. Table 3-16 describes the connector pin assignments.

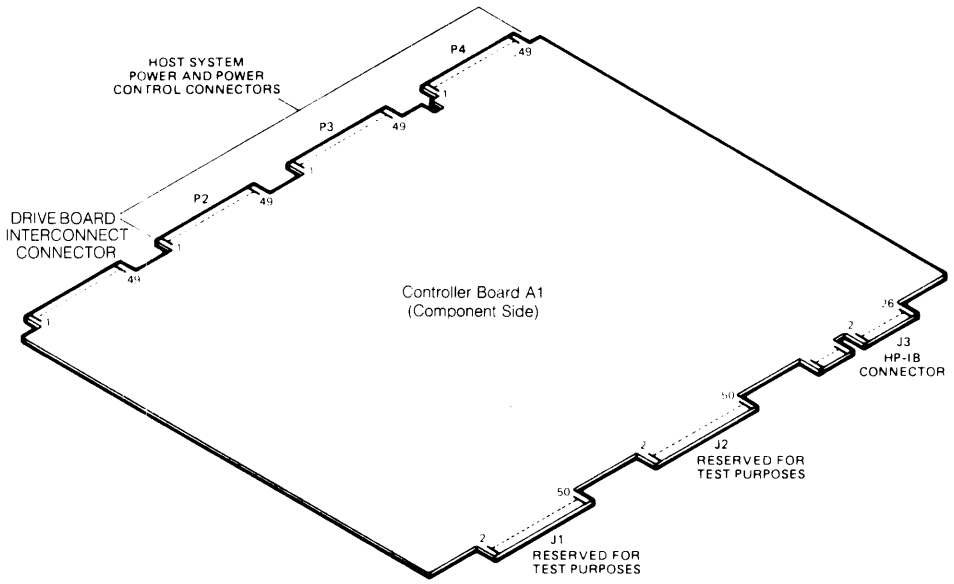


Figure 3-22. Controller Board A1 (07902-66501) Connectors

Table 3-8. 07902-66501 Connector Pin Assignments

A1P1 (See Notes 1)

PIN	SIGNAL	PIN	SIGNAL
1	GND	2	DSL0H
3	GND	4	DSL1H
5	GND	6	DSL2H
7	GND	8	DSLVL
9	GND	10	LDCTL
11	GND	12	STENL
13	GND	14	RSPNH
15	GND	16	WRITL
17	GND	18	PHIBH
19	GND	20	PHIAH
21	GND	22	DLCKL
23	GND	24	HED1H
25	GND	26	PORH
27	GND	28	INDXL
29	GND	30	SPINL
31	GND	32	TRK0L
33	GND	34	WPRTL
35	GND	36	REDYH
37	GND	38	DATAH
39	GND	40	DATAL
41	GND	42	NC
43	KEY	44	KEY
45	GND	48	PONH
49	GND	50	–5V TP

A1J3 (See Note 2)

PIN	SIGNAL	PIN	SIGNAL
1	NC	2	NC
3	GND	4	GND (Shield)
5	GND	6	ATN
7	GND	8	SRQ
9	GND	10	IFC
11	GND	12	NDAC
13	GND	14	NRFD
15	GND	16	DAV
17	REN	18	EOI
19	DIO8	20	DIO4
21	DIO7	22	DIO3
23	DIO6	24	DIO2
25	DIO5	26	DIO1

A1P2 (See Note 1)

PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	+5V
3	+5V	4	+5V
7	−12V	8	−12V
13	+12V	14	+12V
17	NC	18	GND
27	NC	28	GND
35	GND	36	PON
45	GND	46	GND

A1P4 (See Note 1)

PIN	SIGNAL	PIN	SIGNAL
1	+5V	2	+5V
3	+5V	4	+5V
7	−12V	8	−12V
13	+12V	14	+12V
17	NC	18	GND
27	NC	28	GND
33	SYSRST	34	NC
35	GND	36	PON
45	GND	46	GND

Notes:

1. Even-numbered pins are on circuit side of Board, odd-numbered pins are on component side.
2. Odd-numbered pins are on circuit side of board, even-numbered pins are component side.

Schematic Diagrams

Introduction

This section contains the circuit diagrams for the controller board P/N 07902-66501.

NOTE:
* VALUES SELECTED IN TEST.

Figure 3-23. Controller Board A1 (07902-66501) Schematic Diagrams (Sheet 1)

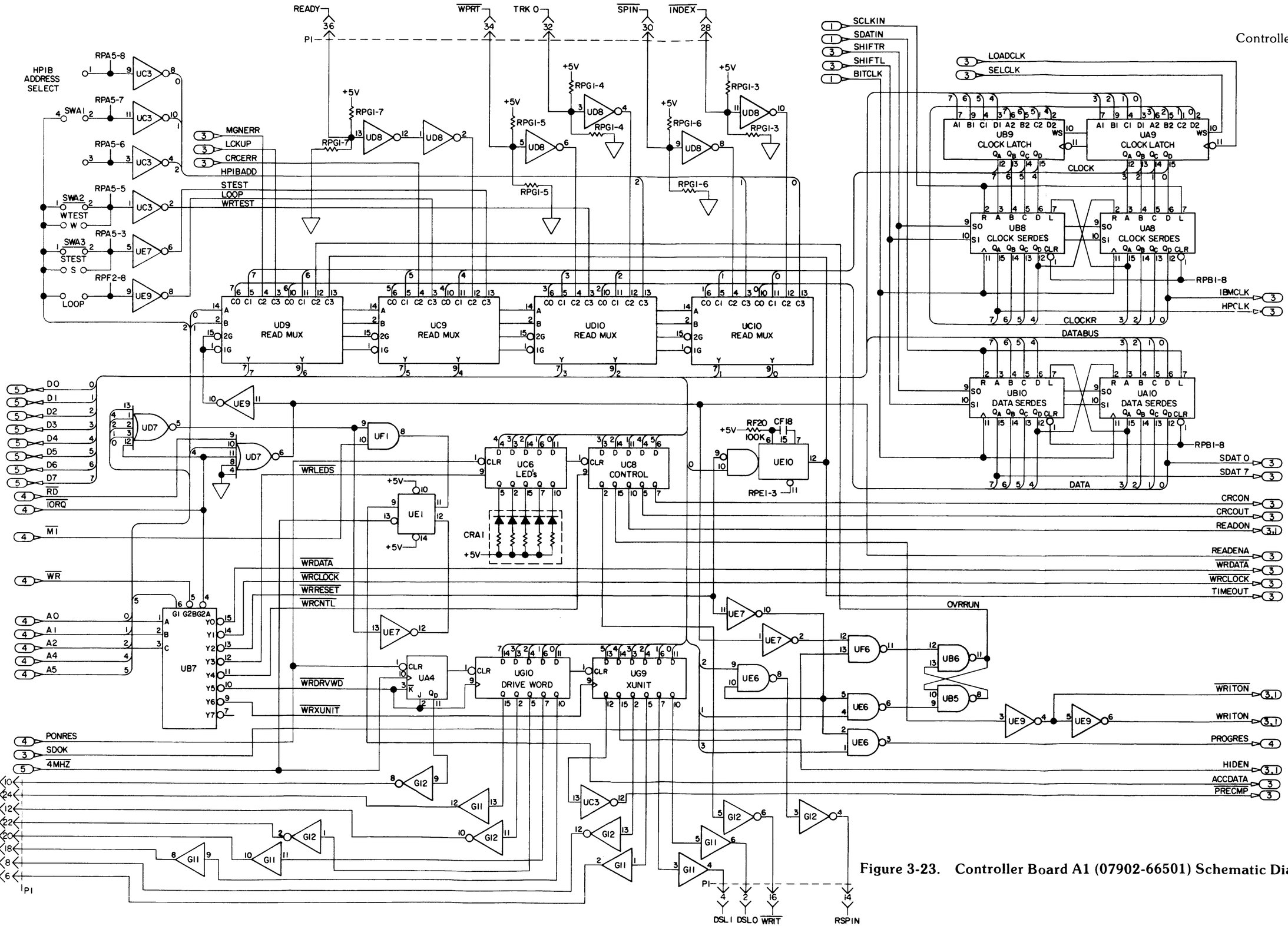


Figure 3-23. Controller Board A1 (07902-66501) Schematic Diagrams (Sheet 2)

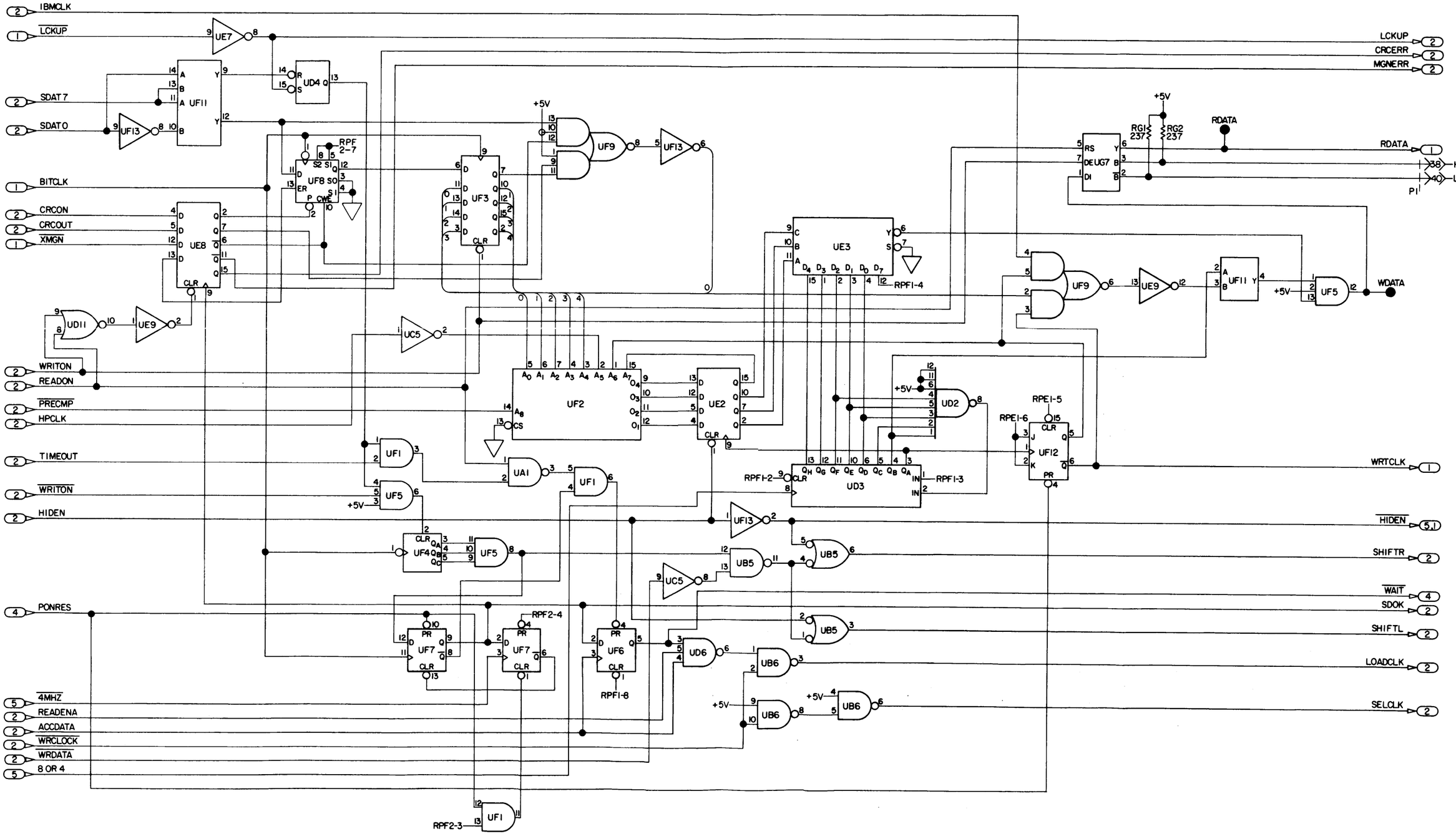


Figure 3-23. Controller Board A1 (07902-66501) Schematic Diagrams (Sheet 3)

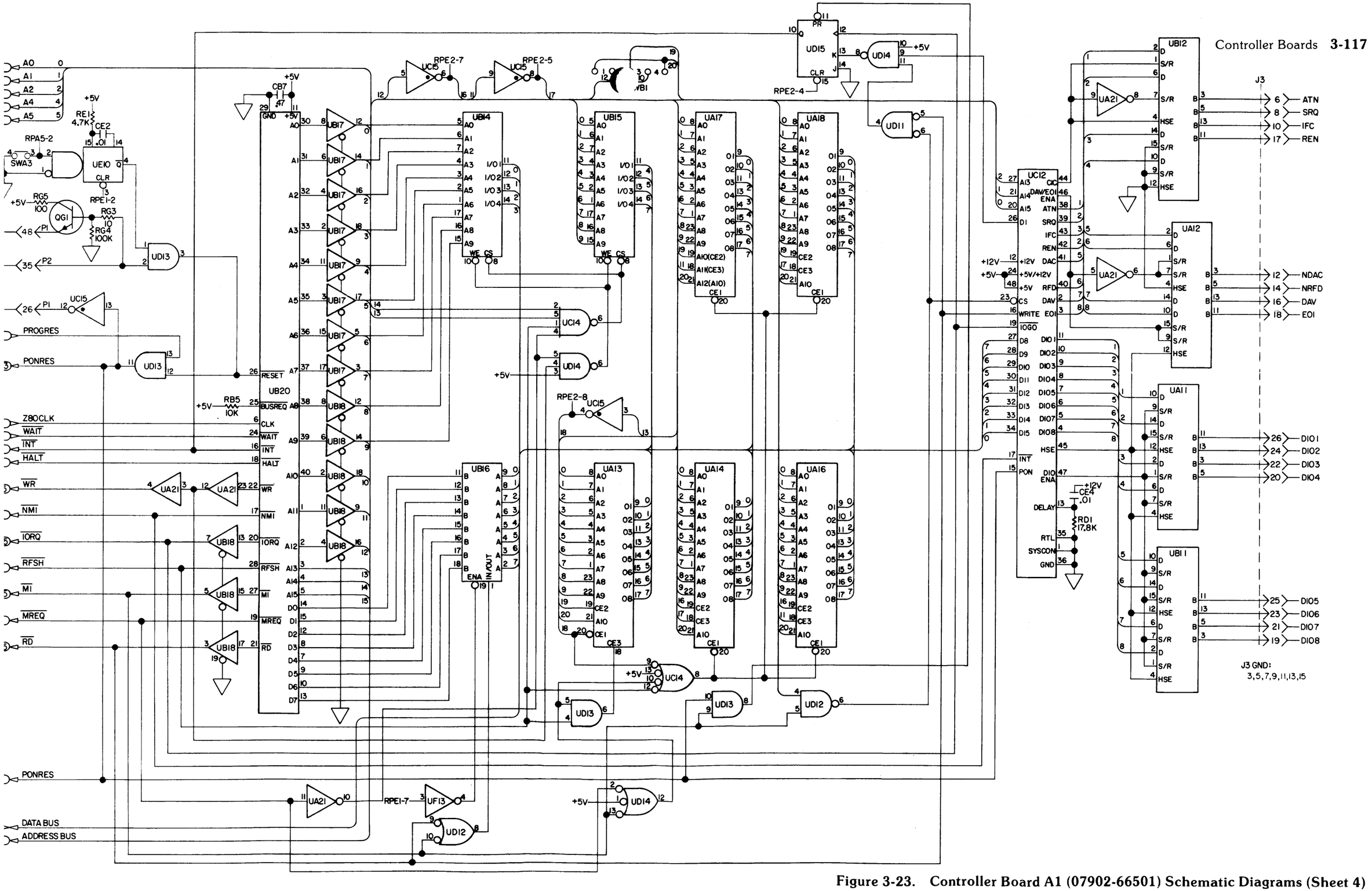


Figure 3-23. Controller Board A1 (07902-66501) Schematic Diagrams (Sheet 4)

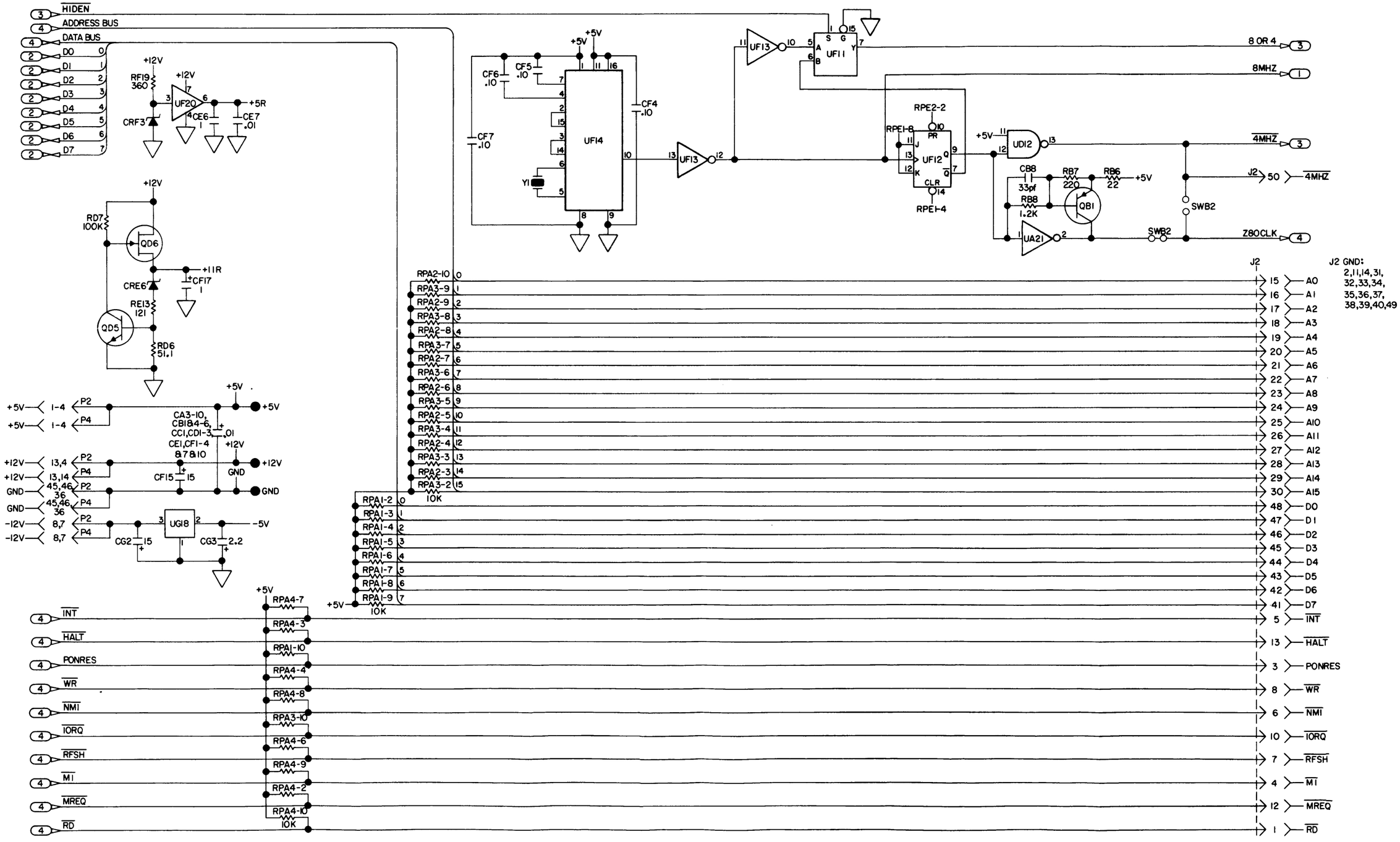


Figure 3-23. Controller Board A1 (07902-66501) Schematic Diagrams (Sheet 5)

Replaceable Parts

Introduction

The controller board P/N 07902-66501 parts list is provided in this section. The total quantity of a part is shown only the first time it is used on this assembly.

The number shown in the "CD" column is the parts check digit. Include the check digit number with the part number when ordering a part from HP.

Reference designators are listed in alphanumeric order in lieu of item numbers for printed circuit assembly parts.

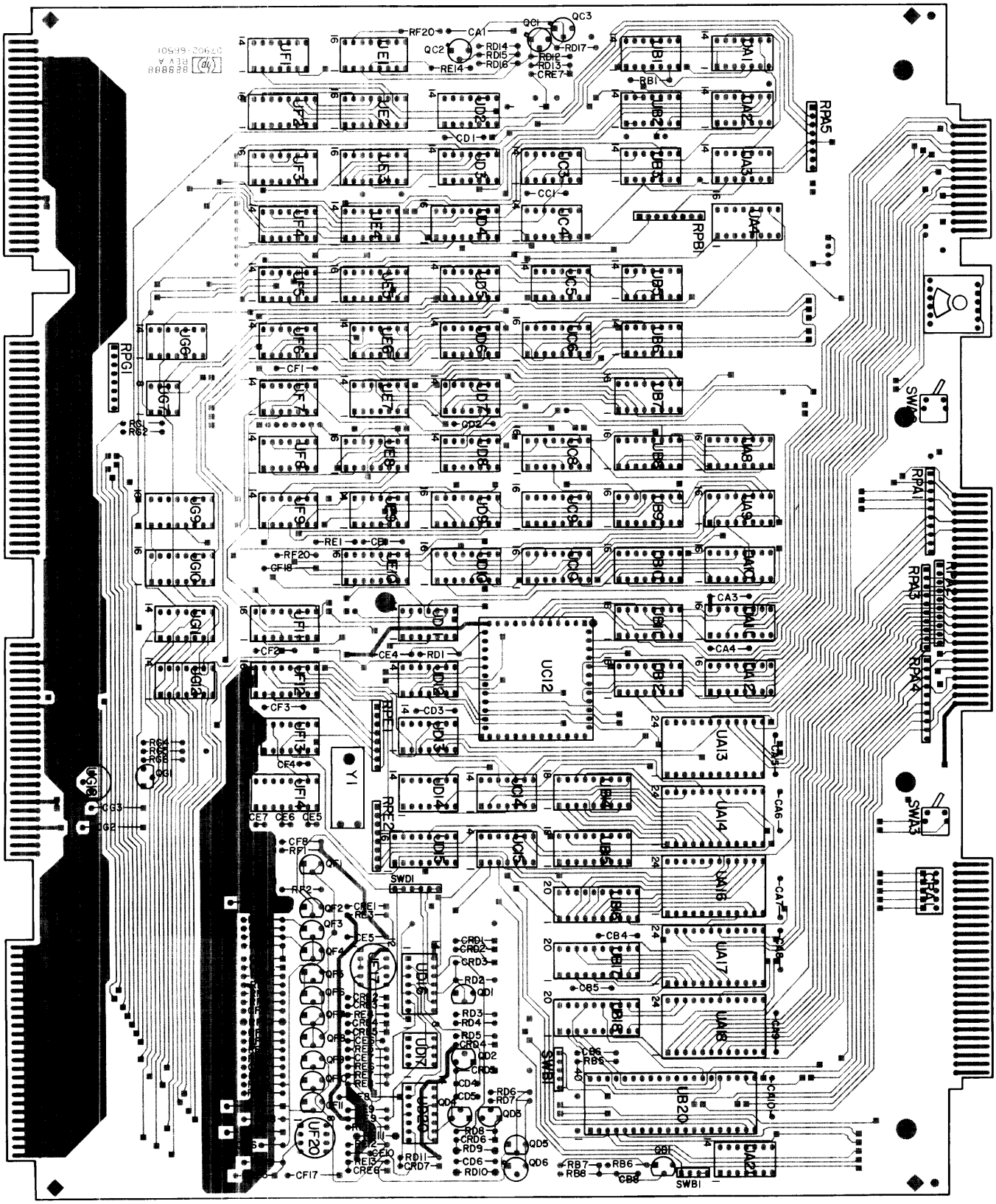


Figure 3-24. Controller Board A1 (07902-66501) Component Locator

Controller Board 07902-66501

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
CA3	9	0160-3847	29	C-F;.01UF;100V
CA4	9	0160-3847		C-F;.01UF;100V
CA5	9	0160-3847		C-F;.01UF;100V
CA6	9	0160-3847		C-F;.01UF;100V
CA7	9	0160-3847		C-F;.01UF;100V
CA8	9	0160-3847		C-F;.01UF;100V
CA9	9	0160-3847		C-F;.01UF;100V
CA10	9	0160-3847		C-F;.01UF;100V
CB1	9	0160-3847		C-F;.01UF;100V
CB4	9	0160-3847		C-F;.01UF;100V
CB5	9	0160-3847		C-F;.01UF;100V
CB6	9	0160-3847		C-F;.01UF;100V
CB7	9	0160-0174	1	C-F;.47UF;25V
CB8	5	0160-2150	1	C-F;33PF;300V
CD1	9	0160-3847	5	C-F;.01UF;100V
CD2	9	0160-3847		C-F;.01UF;100V
CD3	9	0160-3847		C-F;.01UF;100V
CD4	3	0160-2009	1	C-F;820PF;300V
CD5	8	0160-0363	1	C-F;620PF;300V
CD6	9	0160-3847		C-F;.01UF;100V
CD7	5	0180-1746		C-F;15UF;20V
CE1	9	0160-3847		C-F;.01UF;100V
CE2	9	0160-3847		C-F;.01UF;100V
CE4	9	0160-3847		C-F;.01UF;100V
CE5	9	0160-3847		C-F;.01UF;100V
CE6	2	0160-0127	1	C-F;1UF;25V
CE7	9	0160-3847		C-F;.01UF;100V
CE8	5	0180-1746		C-F;15UF;20V
CE9	9	0160-3847		C-F;.01UF;100V
CE10	4	0160-2307	1	C-F;47PF;300V
CF1	9	0160-3847		C-F;.01UF;100V
CF2	9	0160-3847		C-F;.01UF;100V
CF3	9	0160-3847		C-F;.01UF;100V
CF4	5	0160-0576	4	C-F;.1UF;50V
CF5	5	0160-0576		C-F;.1UF;50V
CF6	5	0160-0576		C-F;.1UF;50V
CF7	5	0160-0576		C-F;.1UF;50V
CF8	9	0160-3847		C-F;.01UF;100V
CF10	5	0180-1746		C-F;15UF;20V
CF11	9	0160-3847		C-F;.01UF;100V
CF12	9	0160-3847		C-F;.01UF;100V
CF13	9	0160-3847		C-F;.01UF;100V
CF14	3	0160-0194	1	C-F;1500PF;200V
CF15	5	0180-1746		C-F;15UF;20V
CF16	7	0160-0362	1	C-F;510PF;300V
CF17	3	0180-0291	1	C-F;1UF;35V
CG2	5	0180-1746		C-F;15UF;20V
CG3	8	0180-0197	1	C-F;2.2UF;20V
CRA1	2	1990-0622	1	DIODE;LED
CRD1	1	1901-0040	14	DIODE;SWITCHING
CRD2	1	1901-0040		DIODE;SWITCHING
CRD3	1	1901-0040		DIODE;SWITCHING
CRD4	1	1901-0040		DIODE;SWITCHING
CRD5	1	1901-0040		DIODE;SWITCHING
CRD6	1	1901-0040		DIODE;SWITCHING
CRD7	1	1901-0040		DIODE;SWITCHING
CRE1	1	1901-0040		DIODE;SWITCHING

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
CRE2	1	1901-0040		DIODE;SWITCHING
CRE3	1	1901-0040		DIODE;SWITCHING
CRE4	3	1902-3002	2	DIODE;ZENER;2.3V
CRE5	3	1902-3002		DIODE;ZENER;2.3V
CRE6	2	1902-3150	1	DIODE;ZENER;9.09V
CRE7	2	1901-0025		DIODE;SWITCHING
CRF1	1	1901-0040		DIODE;SWITCHING
CRF2	1	1901-0040		DIODE;SWITCHING
CRF3	1	1902-3092	1	DIODE;ZENER;4.99V
CRF4	2	1901-0025		DIODE;SWITCHING
QB1	2	1853-0036	1	TRANSISTOR;2N3906
QC1	9	1854-0354	3	TRANSISTOR;SS2077
QC2	9	1854-0354		TRANSISTOR;SS2077
QC3	9	1854-0354		TRANSISTOR;SS2077
QD1	2	1854-0092	3	TRANSISTOR;2N3563
QD2	5	1853-0089	12	TRANSISTOR;2N4917
QD3	5	1853-0089		TRANSISTOR;2N4917
QD4	5	1853-0089		TRANSISTOR;2N4917
QD5	1	1854-0215	2	TRANSISTOR;2N3904
QD6	2	1855-0420	1	TRANSISTOR;2N4391
QF1	2	1854-0092		TRANSISTOR;2N3563
QF2	5	1853-0089		TRANSISTOR;2N4917
QF3	5	1853-0089		TRANSISTOR;2N4917
QF4	5	1853-0089		TRANSISTOR;2N4917
QF5	5	1853-0089		TRANSISTOR;2N4917
QF6	2	1854-0092		TRANSISTOR;2N3563
QF7	5	1853-0089		TRANSISTOR;2N4917
QF8	5	1853-0089		TRANSISTOR;2N4917
QF9	5	1853-0089		TRANSISTOR;2N4917
QF10	5	1853-0089		TRANSISTOR;2N4917
QF11	5	1853-0089	12	TRANSISTOR;2N4917
QG1	1	1854-0215		TRANSISTOR;2N3904
RB5	1	0683-1035	6	R-F;10K OHM;5;.25W
RB6	9	0683-2205	1	R-F;2.2K OHM;5;.25W
RB7	1	0683-2215	1	R-F;220 OHM;5;.25W
RB8	1	0683-1225	1	R-F;1.2K OHM;5;.25W
RD1	8	0698-3136	1	R-F;17.8K OHM;.125W
RD2	4	0683-1525	1	R-F;1500 OHM;5;.25W
RD3	9	0683-1025	7	R-F;1K OHM;5;.25W
RD4	8	0683-2725	1	R-F;2700 OHM;5;.25W
RD5	1	0683-1035		R-F;10K OHM;5;.25W
RD6	0	0757-0394	1	R-F;51.1 OHM;1;.125W
RD7	3	0683-1045	1	R-F;100K OHM;5;.25W
RD8	1	0757-0428	1	R-F;1.62K OHM;1;.125W
RD9	7	RESISTOR	1	TEST SELECT
RD10	7	RESISTOR	1	TEST SELECT
RD11	9	0683-1025		R-F;1K OHM;5;.25W
RD12	1	0683-1035		R-F;10K OHM;5;.25W
RD13	0	0757-0279	1	R-F;3.16K OHM;1;.125W
RD14	9	0683-1025		R-F;1K OHM;5;.25W
RD15	9	0683-1025		R-F;1K OHM;5;.25W
RD16	9	0757-0400	1	R-F;90.9 OHM;1;.125W
RD17	9	0683-1025		R-F;1K OHM;5;.25W
RE1	2	0683-4725	1	R-F;4.7K OHM;5;.25W
RE2	6	0757-0465	1	R-F;100K OHM;1;.125W
RE3	9	0683-1025		R-F;1K OHM;5;.25W
RE4	9	0683-1025		R-F;1K OHM;5;.25W
RE5	5	0757-0422	2	R-F;909 OHM;1;.125W
RE6	5	0757-0422		R-F;909 OHM;1;.125W

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
RE7	8	0698-0083	2	R-F;1.96K OHM;1;.125W
RE8	0	0757-0419	1	R-F;681 OHM;1;.125W
RE9	6	0683-5115	4	R-F;510 OHM;5;.25W
RE10	7	0698-0082	1	R-F;464 OHM;1;.125W
RE11	7	RESISTOR	1	TEST SELECT
RE12	1	0683-5615	1	R-F;560 OHM;5;.25W
RE13	2	0757-0403	1	R-F;121 OHM;1;.125W
RE14	2	0683-1515		R-F;150 OHM;5;.25W
RF1	1	0683-2025	1	R-F;2K OHM;5;.25W
RF2	4	0683-1525	1	R-F;1500 OHM;5;.25W
RF3	7	0683-1015	5	R-F;100 OHM;5;.25W
RF4	7	0683-1015		R-F;100 OHM;5;.25W
RF5	1	0683-1035		R-F;10K OHM;5;.25W
RF6	1	0683-1035		R-F;10K OHM;5;.25W
RF7	6	0683-2715	1	R-F;270 OHM;5;.25W
RF8	7	0683-1015		R-F;100 OHM;5;.25W
RF9	7	0683-1015		R-F;100 OHM;5;.25W
RF10	7	RESISTOR	1	TEST SELECT
RF11	7	0757-0317	1	R-F;1.33K OHM;1;.125W
RF12	4	0757-0273	1	R-F;3.01K OHM;1;.125W
RF13	9	0757-0442	1	R-F;10K OHM;1;.125W
RF14	3	0757-0438	1	R-F;5.11K OHM;1;.125W
RF15	3	0757-0420	1	R-F;750 OHM;1;.125W
RF16	3	0757-0470	1	R-F;162K OHM;1;.125W
RF17	8	0698-0083		R-F;1.96K OHM;1;.125W
RF18	5	0698-3456	1	R-F;287K OHM;1;.125W
RF19	7	0683-3615	1	R-F;360 OHM;5;.25W
RF20	2	0683-1515		R-F;150 OHM;5;.25W
RF21	7	0757-0416		R-F;511 OHM;1;.125W
RG1	9	0698-3442	2	R-F;237 OHM;1;.125W
RG2	9	0698-3442		R-F;237 OHM;1;.125W
RG3	5	0683-1005	1	R-F;10 OHM;5;.25W
RG4	1	0683-1035		R-F;10K OHM;5;.25W
RG5	7	0683-1015		R-F;100 OHM;5;.25W
RPA1	0	1810-0125	4	R-F;NETWORK
RPA2	0	1810-0381		R-F;NETWORK
RPA3	8	1810-0280		R-F;NETWORK
RPA4	8	1810-0280		R-F;NETWORK
RPA5	8	1810-0280	5	R-F;NETWORK
RPB1	0	1810-0125		R-F;NETWORK
RPE1	0	1810-0125		R-F;NETWORK
RPE2	6	1810-0030	1	R-F;NETWORK
RPF1	0	1810-0125		R-F;NETWORK
RPF2	0	1810-0125		R-F;NETWORK
RPG1	7	1810-0362	1	R-F;NETWORK
SWA1	9	3100-3395		SWITCH;THWHL;8 POS
SWA2	6	3101-1675	2	SWITCH;TGL
SWA3	6	3101-1675		SWITCH;TGL
UA1	8	1820-1287	2	IC;74LS37
UA2	8	1820-1211	1	IC;74LS86
UA3	8	1820-1112	5	IC;74LS74
UA4	6	1820-1053	1	IC;7414
UA8	5	1820-1276	4	IC;74LS194
UA9	9	1820-1444	2	IC;74LS298
UA10	5	1820-1276		IC;74LS194
UA11	3	1820-2058	4	IC;TRANSCEIVER
UA12	3	1820-2058		IC;TRANSCEIVER
UA17	8	1818-1349		IC;ROM
UA21	6	1820-0683	1	IC;74S04

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
UB1	0	1810-0315	1	IC:DELAY LINE
UB2	8	1820-1112		IC:74LS74
UB3	8	1820-1112		IC:74LS74
UB5	9	1820-1197	3	IC:74LS00
UB6	8	1820-1196		IC:74LS174
UB7	3	1820-1216	1	IC:74LS138
UB8	5	1820-1276		IC:74LS194
UB9	9	1820-1444		IC:74LS298
UB11	3	1820-2058		IC:TRANSCEIVER
UB12	3	1820-2058		IC:TRANSCEIVER
UB14	1	1818-0443	2	IC:MEMORY
UB15	1	1818-0443		IC:MEMORY
UB16	4	1820-2075	1	IC:74LS245
UB17	3	1820-2024	2	IC:74LS244
UB18	3	1820-2024		IC:74LS244
UB20	3	1820-2298	1	IC:Z80A:CPU
UC3	1	1820-1199	5	IC:74LS04
UC4	5	1820-1193	1	IC:74LS197
UC5	1	1820-1199		IC:74LS04
UC6	8	1820-1196		IC:74LS174
UC7	8	1820-1196		IC:74LS174
UC8	8	1820-1196		IC:74LS174
UC9	9	1820-1238	4	IC:74LS253
UC10	9	1820-1238		IC:74LS253
UC12	1	1820-2147	1	IC:1AA6-6004
UC14	9	1820-1204	1	IC:74LS20
UC15	7	1820-0577	2	IC:SN7416
UD2	2	1820-1207	1	IC:74LS30
UD3	6	1820-1433	1	IC:74LS164
UD4	5	1820-1440	1	IC:74LS279
UD5	7	1820-1210	2	IC:74LS51
UD6	7	1820-1202	1	IC:74LS10
UD7	4	1820-1275	1	IC:74LS260
UD8	6	1820-1053	1	IC:7414
UD9	9	1820-1238		IC:74LS253
UD10	9	1820-1238		IC:74LS253
UD11	6	1820-1144	1	IC:74LS02
UD12	8	1820-1287		IC:74LS37
UD13	6	1820-1201	2	IC:74LS08
UD14	7	1820-1202		IC:74LS10
UD15	3	1820-1282	1	IC:74LS109
UD17	7	1820-0577		IC:SN7416
UD18	4	1820-0475	1	IC:LINEAR
UD20	4	1821-0001	1	IC:CA3046
UE1	9	1820-1212	1	IC:74LS112
UE2	7	1820-1195	2	IC:74LS175
UE3	4	1820-1217	1	IC:74LS151
UE4	9	1820-2096	2	IC:74LS393
UE5	8	1820-1419	1	IC:74LS85
UE6	9	1820-1197		IC:74LS00
UE7	1	1820-1199		IC:74LS04
UE8	7	1820-1195		IC:74LS175
UE9	1	1820-1199		IC:74LS04
UE10	4	1820-1423	1	IC:74LS123
UE17	6	1820-0427	1	IC:MC1496
UF1	6	1820-1201		IC:74LS08
UF2	6	1816-1474		IC:PROM
UF3	8	1820-1196		IC:74LS174
UF4	9	1820-2096		IC:74LS393

REFERENCE DESIGNATOR	CHECK DIGIT	HP PART NUMBER	TOTAL QUANT.	DESCRIPTION
UF5	8	1820-1203	1	IC:74LS11
UF6	8	1820-1112		IC:74LS74
UF7	8	1820-1112		IC:74LS74
UF8	3	1820-2016	1	IC:CRC GEN
UF9	7	1820-1210		IC:74LS51
UF11	1	1820-1470	1	IC:74LS157
UF12	9	1820-1212		IC:74LS112
UF13	1	1820-1199		IC:74LS04
UF14	3	1820-1977	1	IC:MC12061
UF20	8	1826-0021	1	IC:OP AMP
UG7	5	1820-2159	1	IC:75117
UG9	8	1820-1196	5	IC:74LS174
UG10	8	1820-1196		IC:74LS174
UG11	6	1820-1368	1	IC:74365
UG12	2	1820-2007	1	IC:74366
UG18	7	1820-0220	1	IC:LM320H
Y1	0	0410-1031	1	CRYSTAL

Appendix A

HP 7902/9895K Disc Memory Command Set

Introduction

The following description of the HP 7902/9895K Flexible Disc Memory command set is HP-IB rather than CPU oriented. It is given in terms of operations (mainly bytes sent) over the HP-IB. Since this level is common to any interface to the 7902/9895K, it is machine independent.

A basic knowledge of the HP-IB operation including primary commands, secondary commands, and parallel poll operation is assumed. An HP publication "Condensed Description of the Hewlett-Packard Interface Bus", Part No. 59401-90030, is available for background information. HP-IB is an implementation of IEEE Standard #488-1978.

Bus Controller	As used in the manual, is the current HP-IB controller in charge of the HP-IB.
Controller	The 7902/9895K disc controller hardware or firmware.
Unit	One of up to four drives connected to the controller.
Flexible Disc, Disc or Diskette	The coated mylar media used to record data on by the 7902/9895K.
HP Format	The double-density, single- or double-sided, HP standard recording format.
IBM Format	The single-sided IBM standard recording format.
Physical Track Number	The track number relative to the outer-most track on the disc.
Logical Track Number	The track number recorded on the disc at a physical track. Logical track numbers may or may not be the same as the physical track number.
Head	One of the two sets of read, write and erase elements used to record data in the unit.
Track	The area defined by a cylinder and head address.
Cylinder	The recording area accessible by the two heads without moving the head actuator.
Sector	The smallest block of data that can be read or written from the disc.
Host System	The system which contains the bus controller.

Command Compatibility

The 7902/9895K belongs to a set of command compatible HP-IB interface discs. All of these discs meet the "HP-300 Compatible HP-IB" standards. In addition, the same sequence of HP-IB operations can be used to transfer data to and from any of these discs.

There are some subtle differences between HP-300 Compatible HP-IB and IEEE Standard #488-1978.

1. An identify code sequence by the host to determine what class of devices and which device is connected, is not supported by IEEE #488-1978.
2. Disc read and write operations cannot be suspended and then resumed; i.e., an Untalk or Unlisten command terminates command operation. This is not consistent with IEEE #488-1978.

Since the capacity and organization of a flexible disc is different from other HP-IB compatible discs, the allowable range of certain parameters is also different from the other discs.

Certain commands used in formatting a disc or for diagnostic purposes are unique to the 7902/9895K. Similarly, certain commands supported by other discs are not supported by the 7902/9895K. An unrecognized command causes an error to be set, but has no detrimental effect on controller operation.

Command Sequences

Much of the 7902/9895K command set shown in this section is made up from two basic types of HP-IB sequences.

To send information (commands or data) to the 7902/9895K, the bus controller addresses it to listen, and then sends a secondary command byte followed by a series of information bytes. The last information byte sent must be tagged with an EOI. Finally, the bus controller sends an Unlisten command, and the sequence is complete.

To receive information (status or data) from the 7902/9895K, the bus controller addresses it to talk, and then sends a secondary command byte. At this point the device sends back a series of information bytes. In some cases the last information byte will be tagged with an EOI. In cases where the last information byte is not tagged with an EOI, an additional byte tagged with an EOI is made available. The extra byte may be used to detect that a byte was dropped on the HP-IB, or it can be used to determine the end of a transfer without maintaining a byte count. Finally, the bus controller issues an Untalk and the sequence is complete.

Sequences other than the ones shown may, in some cases, work; but there is no guarantee that they will be compatible with other HP-IB discs or with future HP disc memories.

The controller only operates on a single command at any given time; i.e., overlapped operations on multiple drives are not possible.

Parallel Poll Response

Parallel poll is used as an additional means of communication between the 7902/9895K and the bus controller. If the 7902/9895K is ready to accept the next part of a command sequence, it will respond to the parallel poll conducted by the bus controller.

After accepting most secondary command bytes, the 7902/9895K disables the parallel poll response. This indicates that the device is busy processing the current part of the command sequence. The actual disabling of parallel poll response may occur up to 100 microseconds after the secondary is accepted by the 7902/9895K. Thus, if the 7902/9895K has parallel poll enabled, and the bus controller is fast enough to send a command sequence and then conduct a parallel poll before the 7902/9895K has disabled the poll, the bus controller would see the wrong parallel poll response. To solve this problem, an intentional delay can be introduced, or a DSJ command (this disables parallel poll) can be issued before other commands.

The exception to the parallel poll response interlock concerns the Clear commands. The DSJ command, unlike the Clear commands, may not be a valid or recognized command in all states of the controller. Thus, the controller may reject or not even see the DSJ command and not disable the parallel poll response. If the bus controller had expected the DSJ to lower the parallel poll in the case where the controller can not accept the DSJ, the bus controller would see the wrong parallel poll after the Clear command.

Cylinder and Track Numbering

Starting from the outer cylinder, cylinders are numbered sequentially from 0 to 76. These numbers are also the physical track addresses. A track is the intersection of a cylinder and a head. There is also a logical track address associated with each good track. If a disc has no bad tracks, the logical address of a track is the same as the physical address.

A disc with bad tracks can be made to look like a slightly smaller disc with no bad tracks. To do this, the bad tracks are specially marked to indicate that they have no logical address. A track marked in this way is referred to as an invisible track. The remaining good tracks are sequentially assigned logical track numbers. Logical track 0 is the outer-most good track (it may or may not be physical track 0).

During normal operations, the user need be concerned only with logical addresses. The 7902/9895K controller will take care of finding the proper physical address.

Target Addressing

Each unit has a target address associated with it. This is the logical address of the next sector which will be accessed by a Data Transfer command or return for an address request. This sector is referred to as the target sector. It is uniquely determined by a target cylinder address, a target head address and a target sector address.

Following a power up or a Clear command, the target address will be set to cylinder 0, head 0 and sector 0 for HP format and 1 for IBM format.

A Seek command sets the target address to the cylinder, head and sector indicated in the command sequence.

During a data transfer, the target address is automatically updated so the successive logical sectors can be read without issuing a seek to each sector. This includes updates which cross track or cylinder bounds. The 7902/9895K is always in cylinder mode; that is, the head address will be incremented before the cylinder address.

If a data transfer terminates abnormally, the target address is left pointing at the sector which caused the termination.

The D Bit

Each sector has a flag called the D bit. It is used to indicate that a track is defective (which is different than invisible). The D bit can be set or cleared using the Initialize command. A set D bit affects the Read, Write and Format commands and is indicated in the returned status.

The Format command is used to convert all tracks flagged with the D bit into invisible tracks.

HP and IBM Formats

The 7902/9895K can work with discs which use either the HP single- or double-sided formats or the single-sided IBM format. After a disc is inserted in a unit, the first status request for that unit will cause the controller to determine which format is present. This information is available as part of the returned status.

Many details of operation vary slightly for the two formats. These include the allowable range of target address, the updating of target addresses and the effect of the D bit. These differences will be noted in the appropriate command descriptions.

Loading of the Recording Heads

Control of the position of the heads is done by the controller. Any command received correctly that needs to read or write the disc will load the heads for its operation. In addition, the controller will keep the heads loaded for approximately 2 seconds after the command completes the operation in anticipation of a subsequent command. In multiple drive configurations, the time the heads remain loaded on inactive drives can increase from 2 seconds to approximately 10 seconds, as a function of the operation in progress on some active drive, the interleave of the disc in the active drive and the frequency of the command from the host system. If the host system should malfunction, and leave the controller in a state expecting to receive or send data, the controller will abort the operation in approximately 60 seconds and proceed to its idle loop where the heads could be unloaded. The host system has the ability to lock the access door on any/all of the drives to prevent unwarranted access to the discs; in this case, the doors will not be unlocked if the above error condition should occur.

Holdoffs

The 7902/9895K will not execute most operations when it enters either of the two states described below. It is very important to know these states and the commands that will remove the holdoffs.

1. DSJ = 2 or Power On State

   This state is entered after:

   a. The 7902/9895K is powered up.
   b. After the execution of the Initiate Self-Test command.

   As long as DSJ = 2, a value unique to this state, the commands listed below will not be executed. There are, however, three commands which may be executed either to change the DSJ or override its holdoff. These commands are:

   a. The DSJ command,
   b. The Clear commands,
   c. The Cold Load Read command.

   For both DSJ and Clear, the DSJ value becomes 0, the cold load read will override the holdoff and set the DSJ according to the outcome of the read.

   The only way for the bus controller to realize that the device was in the Power On state is by sending the DSJ command (which clears the state).

   The purpose of this holdoff state is to withhold all operations that may occur during normal usage until the bus controller can become aware that the power has been interrupted.

   The following is a list of the commands not executed while in the DSJ = 2 state:

   a. All Read commands
   b. All Write commands
   c. Verify
   d. Initialize
   e. Format
   f. Seek
   g. End
   h. Request status
   i. Request disc address commands

   The 7902/9895K will, however, respond to a Talk command from the above group by sending one byte (of value 1) tagged with an EOI. Also, all data bytes sent to the 7902/9895K as part of the commands listed above will be accepted but ignored. These actions will cause the 7902/9895K not to hang (timeout) the HP-IB until the bus controller is aware of the holdoff.

2. First Status State

   This state is entered for a particular drive after:

   a. A disc is inserted in the drive during normal operation,
   b. The 7902/9895K is powered up with a disc in the drive,
   c. The 7902/9895K is issued an Initiate Self-Test command, with a disc in the drive.

   When this state is entered, a flag in the status 2 word for the drive(s) affected is set. All operations requiring access to the newly inserted disc are disabled until the status of the drive is requested or the Cold Load Read command is issued.

   The holdoff ensures that the HP-IB controller is aware that the disc is a newly inserted one before it is actually accessed. In addition, the first request of status for that drive will cause the device to find out the format of the newly-inserted disc, thereby enabling proper use of the disc.

   Commands not executed while first status is set are:

   a. Read commands
   b. Write commands
   c. Verify
   d. Initialize
   e. Format
   f. Seek

   It should be noted that after a power-on has occurred or after the execution of the Initiate Self-Test command, the DSJ is set to 2 and the first status bit is set for any drive containing a disc. Thus, both holdoffs, DSJ and first status, will be in effect.

   Therefore, to enable access to a disc, two command sequences may be used. They are:

   a. A DSJ or Clear followed by a Status command,
   b. A Cold Load Read command.

Command Execution Checks

In addition to the above holdoffs, the controller will verify other conditions before a particular operation is permitted to execute.

1. Correct number of command bytes.

   Obviously, the correct command syntax must be received, or else an I/O program error is defined by the controller.

2. DSJ = 1 and status 1 <> I/O program error
   DSJ = 1 and status 1 <> illegal opcode

   The above condition exists when the most recent command terminated with an error. The following commands are disabled when this condition exists until the host system requests status and hence is aware of the status of that last operation:

a. Read commands,
b. Write commands,
c. Door lock/unlock.

3. Disc format.

   Most commands that operate on the disc will verify that the format is either HP or IBM. If an unknown disc is in the requested drive, these operations will abort with a status 2 error. The commands are:

   a. Seek,
   b. Read commands,
   c. Write commands,
   d. Initialize command.

4. Obviously, the disc must not be write protected when any command that needs to write information on the disc is given. The commands that make this check are:

   a. Write commands,
   b. Initialize command,
   c. Format command.

Commands

The details of the 7902/9895K HP-IB command set are given in this section. The following conventions are used:

+ +) / + +	Byte sent between the bus controller and the 7902/9895K.
P P D P P E	Parallel poll disabled. Parallel poll enabled.
ADDR	The 7902/9895K's current HP-IB device address.
P	HP-IB parity bit.
ATN	HP-IB bus control signal; this signal indicates that a command is present on the bus.
EOI	End or identify; this signal specifies that the present data byte is the last of the sequence or, if ATN is concurrently asserted, then a parallel poll is being conducted by the bus controller.
UUUU or UNIT	Unit number (0 <= UUUU <= 3).
Stat 1	Status one word: Most significant byte is S1; Least significant byte is unit number.
Stat 2	Status two word.

The bit numbering notation for words is as follows:

15 14 13 12	**11 10 9 8**	**7 6 5 4**	**3 2 1 0**
X X X X	X X X X	X X X X	X X X X

All command sequences are verified for validity when received. This involves testing the secondary command, the command number and the number of data bytes in the command sequence for correctness. An I/O program error is defined whenever there is a problem with a command sequence.

Command Table

	Primary	Secondary	Key[1]	Opcode	Key[2]	# Bytes
Identify	U	ADDRS		—		—
DSJ	T	!10	P	—		1
Read Self-Test	T	!1F	—	—		2
Read Loopback	T	!1E		—		1 to 256
Request Status	L	!08	H	!03	C	2
Request Status	L	!0A	J	!03	C	2
Req (Logical) Address	L	!0A	J	!14	T	2
Req (Logical) Address	L	!08	H	!14	T	2
Req (Physical) Address	L	!0C	L	!14	T	2
Send Status or Address	T	!08	H	—		4
Universal Clear	U	—		—		—
Selected Device Clear	L	—		—		—
HP-300 Clear	L	!10	P	—		1
Initiate Self-Test	L	!1F	—	—		2
Write Loopback	L	!1E		—		1 to 256
Download Controller	L	!0F	O	—		1 to 256
Door Lock	L	!0C	L	!19	Y	2
Door Unlock	L	!0C	L	!1A	Z	2
HP-IB CRC	T/L	!11	Q	—		—
Seek	L	!08	H	!02	B	6
End	L	!08	H	!15	U	2
Buffered Read	L	!0A	J	!05	E	2
Unbuffered Read	L	!08	H	!05	E	2
Verify	L	!08	H	!07	G	4
Buffered Read Verify	L	!0B	K	!05	E	2
Unbuffered Read Verify	L	!0C	L	!05	E	2
Cold Load Read	L	!08	H	!00	@	2
ID Triggered Read	L	!0B	K	!06	F	2
Send Data	T	!00	@	—		—
Buffered Write	L	!09	I	!08	H	2
Unbuffered Write	L	!08	H	!08	H	2
Initialize	L	!08	H	!0B	K	2
Format	L	!0C	L	!18	X	4
Receive Data	L	!00	@	—		—

[1] To generate the command Secondary, hold the Control key down while pressing the listed key.

[2] To generate the command Opcode, hold the Control key down while pressing the listed key.

Command Table

! – Hexadecimal Number
T – Talk Primary
L – Listen Primary
U – Universal Primary

Sense Commands

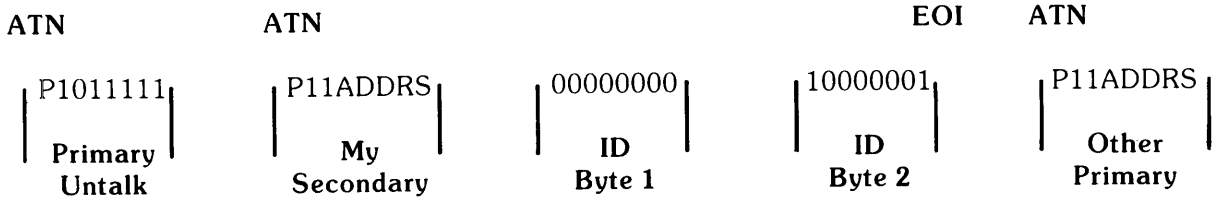
Identify

Type: Sense.

Purpose: The 7902/9895K will return a code unique to the disc subsystem to allow for auto-configuration of systems.

Description: Upon the reception of the untalk primary followed by the secondary corresponding to the 7902/9895K's current HP-IB address, the 7902/9895K's PHI will respond by sending the ID bytes of 0 and 81 hex, the second byte being tagged with an EOI. These two bytes will continue to be sent until another command is transmitted on the bus.

HP-IB Sequence:



DSJ

Type: Sense.

Purpose: The 7902/9895K returns a byte indicating if the last operation completed normally or abnormally, or if the power to the 7902/9895K has just been restored, or if a parity error has been detected on the HP-IB. The DSJ command also provides a way to disable the 7902/9895K's parallel poll response.

Description: After accepting the DSJ secondary, the 7902/9895K disables its parallel poll response (usually within 100 microseconds) and returns a byte (the DSJ byte) reflecting the status of the controller.

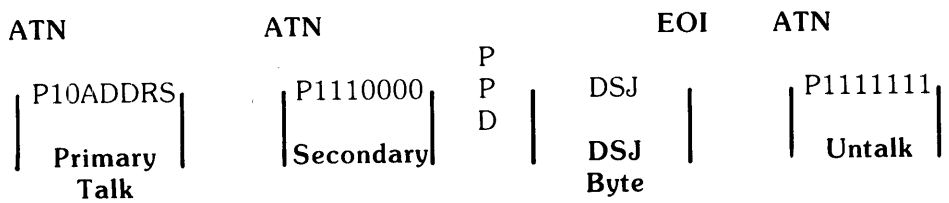
DSJ = 0 – The 7902/9895K completed its last operation normally.

DSJ = 1 – The 7902/9895K aborted its last operation abnormally. Status will indicate the current error.

DSJ = 2 – The 7902/9895K has just completed a power up sequence and is in the DSJ = 2 holdoff state.

DSJ = 3 – A parity error has occurred on the HP-IB. Repeat the request to receive the pre-parity error DSJ.

HP-IB Sequence:



Status (Upon Command Completion):

No errors.

S1 – Unchanged
Stat 2 – Unchanged
DSJ – For DSJ = 0 or DSJ = 1 unchanged
– For DSJ = 2 then 0
– For DSJ = 3 then previous DSJ

Parallel Poll:

Parallel poll is disabled after the reception of the secondary and is not re-enabled after the completion of the command.

Read Self-Test Results

Type:

Sense.

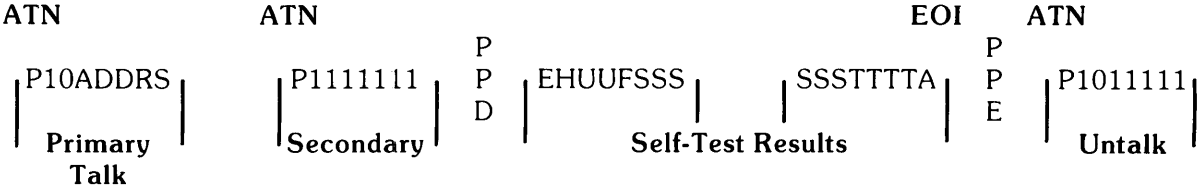
Purpose:

The 7902/9895K returns the results of the last self-test it has performed. This is useful after the Initiate Self-Test command or after the 7902/9895K has been powered on (it performs a self-test at power on).

Description:

After receiving the self-test secondary, the 7902/9895K makes two bytes of the self-test results available. The second byte will be tagged with an EOI.

HP-IB Sequence:



Where:

E – Error bit. If on, then an error has occurred.

H – Head number. Indicates which head the read or write test failed on.

UU – Unit number. Indicates which unit was selected when the error occurred.

F – Format of operation. Indicates if the controller was in IBM (0) or HP (1) operation at the time of failure.

SSSSSS – Subtest number. Number of the failing subtest.

TTTT – Test number. Number of the failing test.

A – "*" LED. Indicates state of the "*" LED.

Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – Unchanged

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

Read Loopback Record

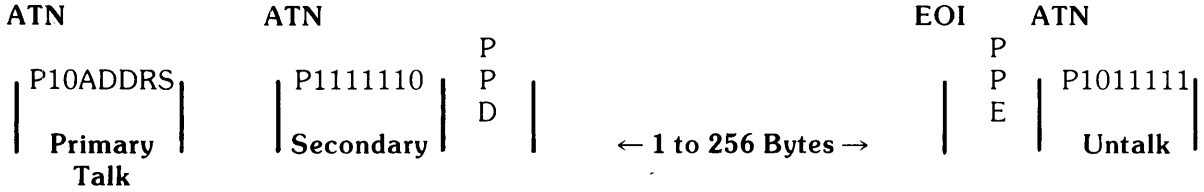
Type: Sense.

Purpose: The 7902/9895K sends up to 256 bytes (see Write Loopback Record) from its internal data buffer over the HP-IB. This is used by diagnostics to test the HP-IB data path.

Description: Upon accepting the loopback secondary, the 7902/9895K sends the bytes stored in its internal buffer. The most significant byte of the first word is transferred first. The 256th byte will be tagged with an EOI and the transfer terminated. If fewer than 256 bytes are requested, the device will realize that the transfer is complete when:

1. The 7902/9895K has been untalked,
2. It accepts another byte from the HP-IB.

HP-IB Sequence:



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – Unchanged

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

Request Status

Type: Sense.

Purpose: The device returns four bytes of status information. These status bytes indicate how the last attempted operation completed, which unit was involved and the current status of the unit specified.

Description:

After receiving the Request Status command, parallel poll response is disabled. If the unit's first status bit is set, the 7902/9895K attempts to determine the type and format of the current disc (this may take up to 10 seconds). After the status operation has completed, the parallel poll response is re-enabled.

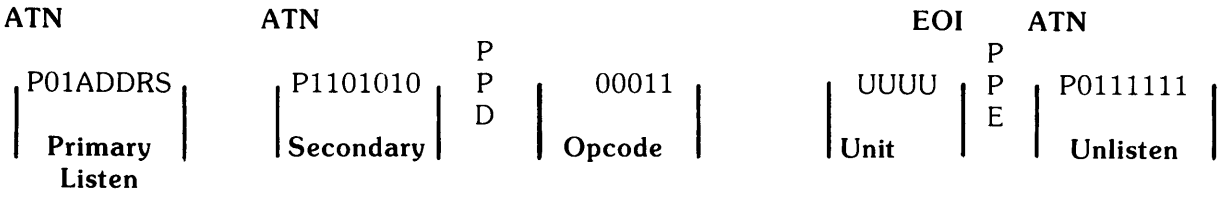
NOTE

There is also an unbuffered status request which uses a different secondary whose operation is identical.

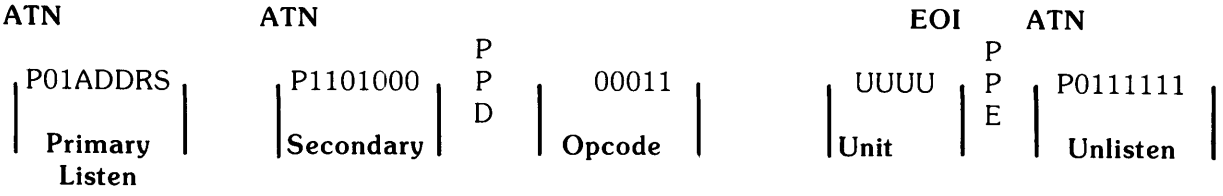
After the send status secondary, the 7902/9895K sends four bytes of status information. The first two bytes (known as Stat 1) includes information about the last operation which the device performed. The Stat 1 unit field indicates which drive was involved in the operation. The D bit is set if a D bit was encountered during the operation.

HP-IB Sequence:

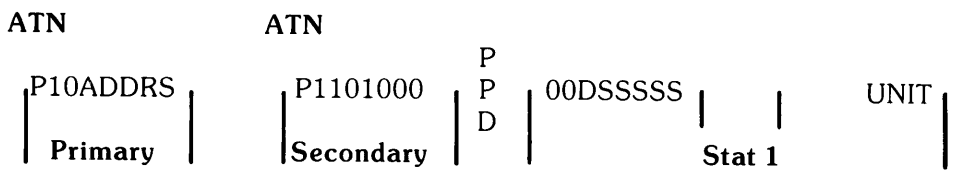
Request Status (Buffered)

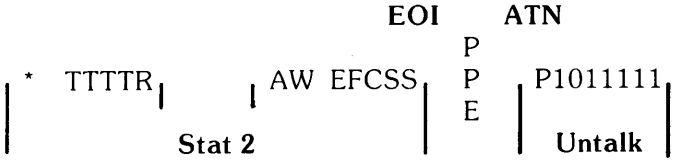


Request Status (Unbuffered)



Receive Status





Where:

	Bit Number	Description
	Stat 1	(From previous operation)
D	13	D Bit
SSSSS	12-8	S1 (see following table)
UNIT	3-0	Unit Number
	Stat 2	**(From current operation)**
*	15	Set if one or more starred bits are set.
TTTT	12-9	Disc Type
R	8	Reserved
A	7	Drive Attention
W	6	Disc is Write Protected
E	4	*Drive Fault
F	3	First Status Bit
C	2	*Seek Check
SS	1, 0	*Drive Ready Status

S1 Binary (Decimal)	**Meaning**
00000 (0)	Normal completion. The operations completed without error, or the controller has just been cleared or powered up.
00001 (1)	Illegal opcode. The last command contained an opcode which is not recognized by the 7902/9895K.
00111 (7)	Cylinder compare error. The target cylinder has one or more sectors in which the track number does not correspond with the track number of the remainder of the sectors. The controller will automatically re-try the read/write operation once if this is encountered.
01000 (8)	Uncorrectable data error. The disc read or verify operation was terminated because a CRC error was detected in the data field. The data is still transmitted for the bad sector.
01001 (9)	Sector compare error. The target sector cannot be found in the current track. Up to two passes of the track are made before this status is set. In this case, a CRC error exists in the preamble of the requested sector, or the subsequent data field cannot be found.
01010 (10)	I/O program error. This error is defined when: 1. An illegal secondary is received. 2. An improper number of data bytes are received. This status can only be set if the previous S1 was zero.

S1 Binary (Decimal)	Meaning
10001 (17)	Defective track or sector. During an HP write, read, read verify or verify, a set D bit was encountered.
10010 (18)	Re-tryable hardware error. An internal hardware timing error occurred during a data transfer or seek. The operation should be re-tried.
10011 (19)	Stat 2 error. Some condition in Stat 2 prevented the drive-related operation from completing normally. These conditions include: 1. Specified unit is between 0 and 3, but that drive is not connected to the controller. 2. There is no disc in the drive. 3. A hardware problem is detected in the drive. 4. The disc is unformatted or has an unknown format. 5. The disc is write protected (error only during a disc write operation). 6. The selected drive's first status bit is set. 7. IBM format requested on a double-sided disc. 8. ID triggered read attempted on an IBM disc.
10111 (23)	Unit unavailable. A command included a request for a unit number greater than 3.
11111 (31)	Drive attention. The indicated drive is requesting attention because: 1. A seek completed normally. 2. A Seek command failed due to: a. Drive fault, b. Out of bounds target cylinder or sector, c. The controller cannot find the target address. 3. Following an End command, a change in drive status was detected, including: a. Inserting a disc, b. Removing a disc.

Stat 2	Bit #	Meaning
*	15	Stat 2 error. This bit is set if one or more of the following bits are set in stat 2: 1. Drive fault, 2. Seek check, 3. Any drive not ready error. (See code 10011 in S1 table for list of possible causes.)
TTTT	12-9	Disc type. These four bits indicate the type and format of the disc currently present in the selected drive as follows: 0000 – Empty drive 0001 – Blank or unknown format, single-sided 0010 – HP format, single-sided 0101 – Blank or unknown format, double-sided 0110 – HP format, double-sided 1000 – IBM format, single-sided
A	7	Attention. This bit is set when a seek completes (successfully or unsuccessfully), or following an End command when stat 2 changes. It is cleared after the status is read.
W	6	Write protected. The disc in the selected drive has the write protect notch present.
E	4	Drive fault. This bit is set after the following occurs: 1. Drive goes not ready after End command, 2. Drive goes not ready during data transfer, 3. Hardware failure. Drive fault is cleared after the status is read.
F	3	First status bit. This bit is set when a disc is present in the selected drive after: 1. Power on, 2. The door is closed, 3. Self-test completion. First status is cleared after the status is read.
C	2	Seek check. This bit is set when a seek fails for one or more of the following reasons: 1. An out-of-bounds target sector was specified, 2. An attempt was made to access a non-existent physical track, 3. The seek algorithm could not find the target logical track. The seek check bit is cleared after the status is read.
SS	1, 0	Drive (not) ready. These two bits indicate the state of the selected drive as follows:

Stat 2	Bit #	Meaning
		00 – Drive ready 01 – Undefined 10 – No drive connected to controller (this condition is established at power on and will not change if a new drive is added while the controller is operating normally) 11 – No disc in drive
Status:		No errors. S1 – 0 Stat 2 – Bits A, E, F and C are cleared DSJ – 0
Parallel Poll:		If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command. An extra byte (the value of 1) tagged with an EOI will be sent if the controller requests more than the specified number of bytes.

Request (Logical) Disc Address

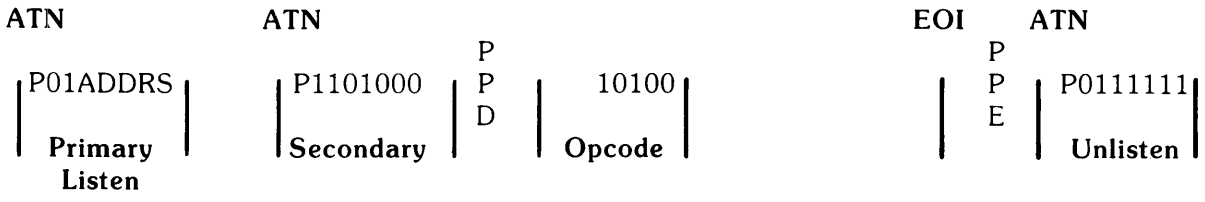
Type: Sense.

Purpose: The 7902/9895K returns bytes indicating the current target address. This command is used to determine the address of the offending sector after a data error has occurred.

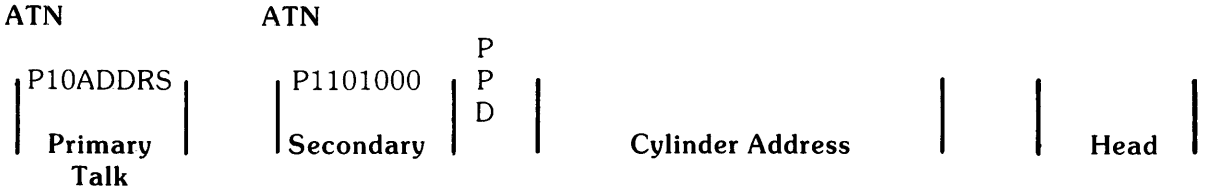
Description: Following reception of the appropriate command sequence, the 7902/9895K returns four bytes indicating the current target sector. This includes two bytes of target cylinder address, one byte of target head address and one byte of target sector address.

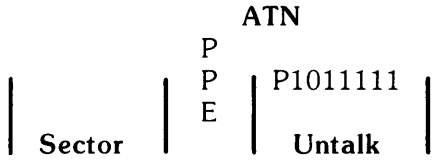
HP-IB Sequence:

Request (Logical) Disc Address



Send Address Command





Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

An extra byte (the value of 1) tagged with an EOI will be sent if the controller requests more than the specified number of bytes. However, this request is not necessary for normal operations.

Request (Physical) Disc Address

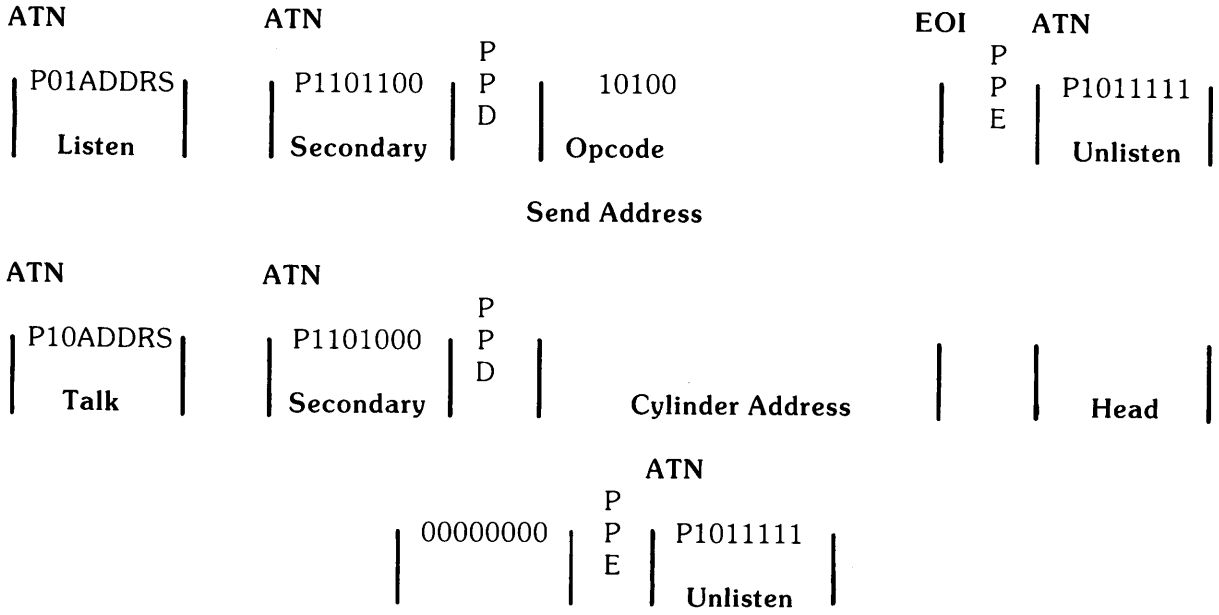
Type: Sense.

Purpose: The 7902/9895K returns bytes indicating the physical cylinder on which the head actuator is positioned. This is useful for calculating the number of invisible tracks between the outer-most track and the current track. This is done by subtracting the physical cylinder address from the target cylinder address.

Description: After receiving the request (physical), the 7902/9895K returns two bytes containing the physical cylinder address, one byte containing the head address and one byte of zeros.

HP-IB Sequence:

Request (Physical) Disc Address



Status: See Request (Logical) Address.

Parallel Poll: See Request (Logical) Address.

Control Commands

Universal or Selected Device Clear

Type: Control.

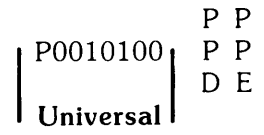
Purpose: A clear places the 7902/9895K in a known state. Thus, it is useful when initializing a system on power up or after a host system crash. The clear also allows a power up DSJ of 2 to be cleared by sending a single byte. Since a clear updates the device's HP-IB address, it is useful if the system is being re-configured.

Description: Upon reception of either a universal or selected device Clear command, the 7902/9895K stops handshaking with the HP-IB, parallel poll response is disabled and the following are performed:

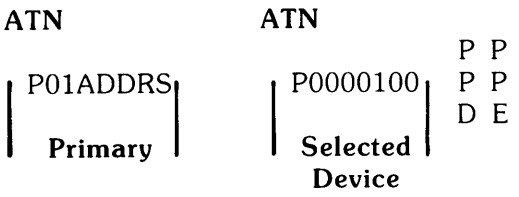
1. The PHI is reset,
2. HP-IB is updated from the device address on the controller board,
3. Stat 1 is cleared,
4. Stat 2 is updated appropriately,
5. DSJ set to 0,
6. All drives are re-calibrated to physical track 0,
7. The target address is set to cylinder 0, head 0, sector 0/1 for HP/IBM format,
8. Disable HP-IB parity checking.

HP-IB Sequence:

Universal Device Clear



Selected Device Clear



Status: No errors.

S1 – 0
Stat 2 – All bits cleared, then bits E and SS are set, if appropriate.
DSJ – 0

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Clear

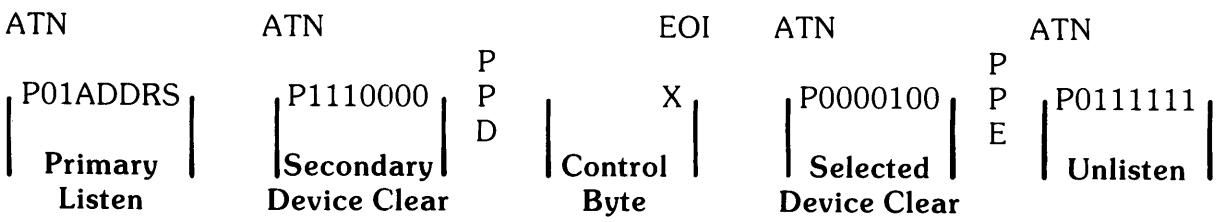
Type: Control.

Purpose: This command gives the user the capability to place the 7902/9895K controller in a known state and to programatically enable or disable the HP-IB parity check logic.

Description: After reception of the HP-300 clear secondary, the data byte and the device clear, the controller sets or clears the HP-IB parity enable in the PHI.

HP-IB Sequence:

HP-300 Device Clear



Where: X – HP-IB parity check bit:
0 – Disable parity check,
1 – Enable parity check.

Status: No errors.

S1 – 0
Stat 2 – All bits cleared, then E and SS set, if appropriate.
DSJ – 0

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Initiate Self-Test

Type: Control.

Purpose: This command gives the user the capability to remotely initiate the 7902/9895K self-test. The self-test results may then be read back using the Read Self-Test Results command. Self-test takes approximately 7 seconds to complete.

Description:

Two bytes are sent following the self-test secondary and contain the following information:

The first byte contains the cylinder to be tested and is only pertinent if the W bit is set in the second byte of the command. The W bit is interpreted as follows:

0 – No write/read test performed,
1 – The write/read test is performed on the designated cylinder.

If the write/read test is selected, a double-sided disc is required and all data on both sides of the selected cylinder will be lost.

After the execution of the self-test, the controller will be in the same state as a power on condition would leave it.

NOTE

The self-test write test will re-format the selected test cylinder. This re-formatting will destroy data on the selected cylinder and change the sector interleave and offset so that it may no longer be optimal for the host system. After the write test is performed, the disc should be re-formatted by the Format command.

HP-IB Sequence:

Initiate Self-Test

ATN	ATN			EOI	ATN
P01ADDRS	P1111111	P P D	Cylinder	W	P P E	P0111111
Primary Listen	**Secondary**			**Control**		**Unlisten**

Status:

No errors.

S1 – 0
Stat 2 – Cleared, the bits E, F, C and * set, if appropriate.
DSJ – 2

Illegal cylinder number.

S1 – Drive attention
Stat 2 – Bit C and * are set.
DSJ – 1

Parallel Poll:

The parallel poll response is re-enabled after the operation is completed, normally or abnormally. If additional commands are sent before the controller is ready and while self-test is in progress, they will be lost.

Write Loopback Record

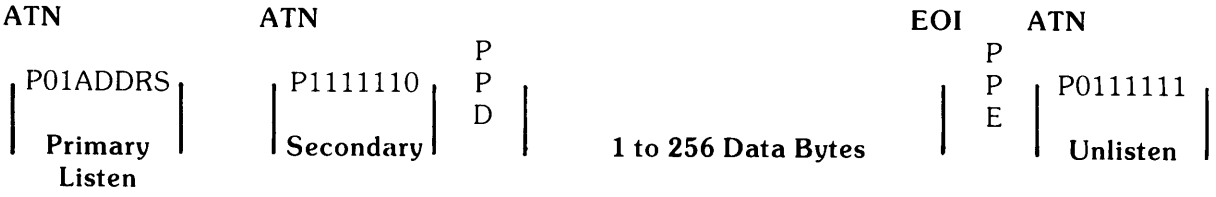
Type: Control.

Purpose: The 7902/9895K stores up to 256 bytes in its internal buffer. A diagnostic could use the command, along with the read loopback record, to test the operation of the HP-IB link.

Description: After receiving the write loopback record secondary, the controller will store up to 256 bytes in the internal buffers. If less than 256 bytes are sent, the last byte must be tagged with an EOI.

HP-IB Sequence:

Write Loopback Record



Status: No errors.

S1 – Unchanged
Stat 2 – Unchanged
DSJ – Unchanged

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

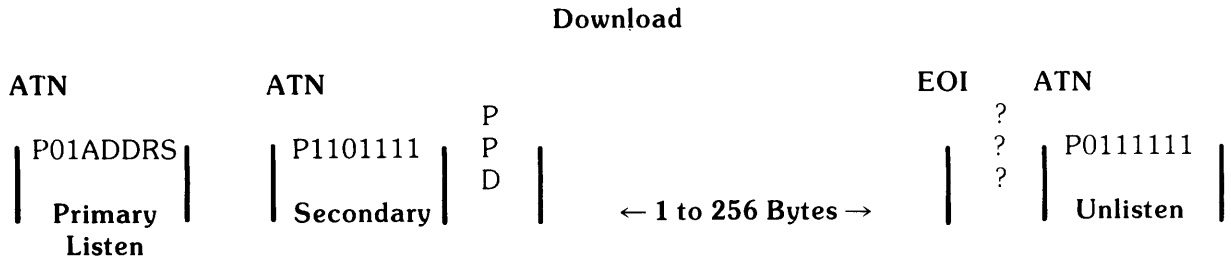
Download

Type: Control.

Purpose: This command allows the downloading and execution of MCC or Z80 code into the controller's internal RAM memory. It is intended for diagnostic purposes only, and as such should be used with care.

Description: After receiving the download secondary, up to 256 bytes are stored in the controller's RAM memory. Following the reception of the last byte, the code will be executed starting at the first byte if the controller processor is an MCC, or starting at the third byte if the controller processor is a Z80.

HP-IB Sequence:



NOTE

Updating of status and the operation of parallel poll is dependent upon downloaded code.

Seek

Type: Control.

Purpose: The Seek command updates a unit's target address and moves the head actuator to the new target cylinder. A seek usually precedes a data transfer operation or a series of consecutive data transfers.

It is important to note that the 7902/9895K controller is totally dedicated to the selected drive during any drive-related operation (e.g., the Seek command). This disallows any overlapped seek operation between multiple drives.

Description: The device receives 6 bytes, including the seek opcode, the unit number, and the target cylinder, head and sector address. Checks are made to assure that the specified drive is available, that the entire command has been received and that the new target address lies within the following bounds:

	HP		IBM
	Single	Double	Single
Cylinder address:	0 <= C <= 76	0 <= C <= 76	0 <= C <= 76
Head address:	H = 0	0 <= H <= 1	H = 0
Sector address:	0 <= S <= 29	0 <= S <= 29	1 <= S <= 26

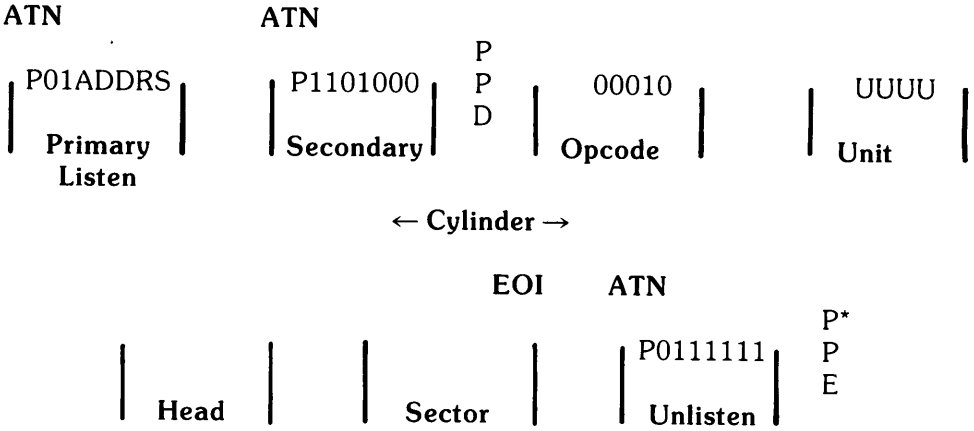
If any of these tests fail, the status is updated and the Seek command is aborted with a "Seek Check" indication.

The following algorithm is used to locate a logical target track during the seek operation:

1. Determine if present logical track is the same as that requested. If they are, then seek is complete. Otherwise, proceed with step 2.
2. Read current cylinder location from disc.

3. If current address is not the location expected, then do physical seek to cylinder 0.
4. Estimate the direction and number of steps to the target cylinder.
5. Step actuator to target and read current head position.
6. If not at target cylinder address, repeat steps 3 and 4 until target found or re-try exhausted.

HP-IB Sequence:



* On seek completion.

Status:

Successful seek.

S1 – Drive attention
Stat 2 – Bit A set (drive attention)
DSJ – 0

Unsuccessful seek.

1. Illegal seek parameter, target track not found, off end of disc.

S1 – Drive attention
Stat 2 – Bits A and C set (seek check)
DSJ – 1

2. Drive not ready during seek, track 0 indicator not found when expected.

S1 – Drive attention
Stat 2 – Bits A and E set (drive fault)
DSJ – 1

No disc, disc not ready, first status bit holdoff, disc not formatted, unknown format.

S1 – Status 2 error
Stat 2 – Unchanged
DSJ – 1

Parallel Poll:

The parallel poll response is re-enabled after the operation is completed, normally or abnormally. Normal completion occurs when the target cylinder is reached.

End

Type: Control.

Purpose: The End command serves a dual purpose as follows:

1. It causes the 7902/9895K to cease responding to a parallel poll and puts the controller and drives in a "Stand By" state, and,
2. In case of a status change in any of the drives, the 7902/9895K immediately re-activates its parallel poll response which can serve as a pseudo-interrupt facility to the bus controller.

Description: The End command should be issued after a series of commands to a single unit have been completed. The following is performed by the 7902/9895K upon reception of an End command:

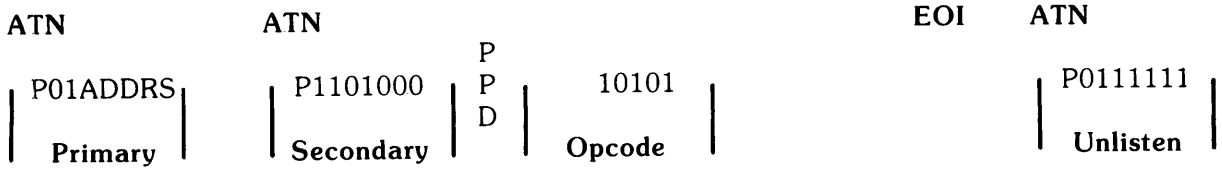
1. S1 – 0
   Stat 2 – Unchanged
   DSJ – 0
2. Disable parallel poll response.
3. Wait for change in drive status.

The 7902/9895K will continue to check the status of all drives and will, at the same time, remain ready to execute any new HP-IB command. However, if no new command has been issued to the 7902/9895K, and the state of a drive changes since the last time status was requested, the following is performed by the device:

1. Disc removed
   S1 – Drive attention
   Stat 2 – Bit A
   DSJ – 1
2. Disc inserted
   S1 – Drive attention
   Stat 2 – Bits A and F set (first status)
   DSJ – 1
3. Parallel poll is enabled on the HP-IB.

HP-IB Sequence:

End Command



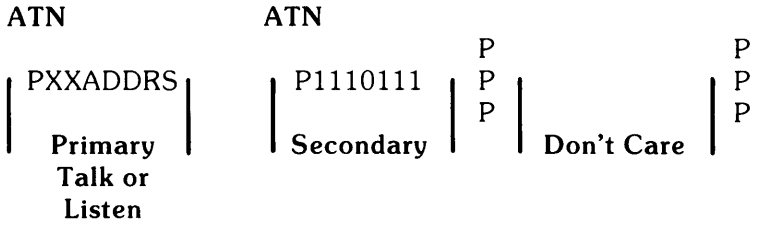
HP-IB CRC Secondary

Type: Control.

Purpose: The HP-IB CRC secondary is part of the 7902/9895K command set to be compatible with future HP-IB devices which use the CRC data tests of the future HP-IB control chips. The 7902/9895K will ignore this command; that is, not set I/O program error when it is received.

Description: The 7902/9895K can be addressed to talk or listen. If addressed to listen, any number of data bytes may be sent; if addressed to talk, an EOI will be sent over the HP-IB.

HP-IB Sequence:



Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Door Lock

Type: Control.

Purpose: This command will lock the disc access door on the selected drive.

NOTE

Normal operation of the 7902/9895K will lock the access door whenever a drive is selected for an operation.

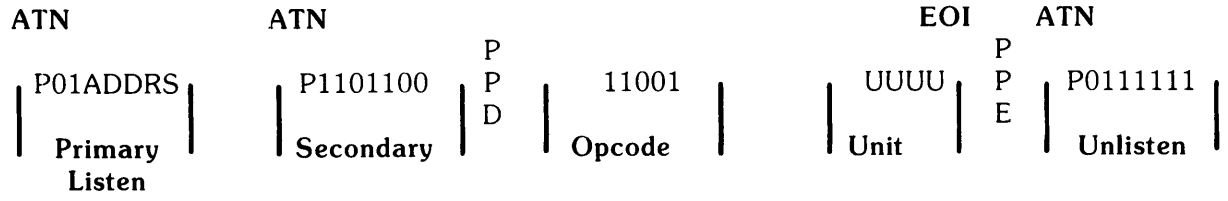
When the door is locked, the heads are also loaded. The heads loaded position represents the maximum wear condition for the disc.

Description: After sending the secondary, the opcode and the unit number, the 7902/9895K will issue a command to the selected drive to lock the door. The door will remain locked and the heads loaded until one of the following conditions occur:

1. A Door Unlock command,
2. A Clear command,
3. An Initiate Self-Test command.

HP-IB Sequence:

Door Lock Request



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Door Unlock

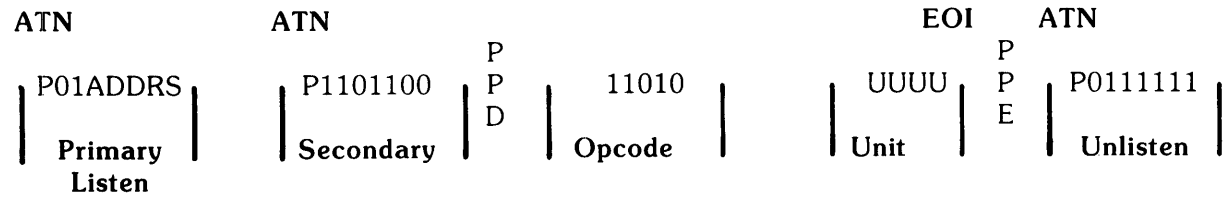
Type: Control.

Purpose: This command is used to unlock the disc access door. It is useful after the Door Lock command is given (see Door Lock).

Description: After the reception of the secondary, opcode and unit number, the 7902/9895K will issue a command to the selected drive to unlock the access door. This command has no effect if the door was not previously locked.

HP-IB Sequence:

Door Unlock



Status: (See Door Lock)

Disc Read Commands

Buffered Read

Type: Disc read.

Purpose: Data is transferred through an internal buffer in 7902/9895K before being sent to the HP-IB. This allows HP-IB data transfers to be asynchronous with the disc, and to vary from an arbitrarily low rate to about 190K bytes per second. The maximum number of bytes to be transferred in a buffered read is 256 (1 sector); the read request must be repeated for each additional sector transferred.

Description: Following reception of the Read command, parallel poll response is disabled and the status of the specified unit is checked. If the unit can be accessed, then the current cylinder number is read and compared with the target cylinder address. If they differ, a seek to the target cylinder is performed. This may occur if the actuator has slipped or if an auto-increment to the next cylinder is required.

If an HP format disc is being used, then the target sector's 256 bytes are read into the controller's buffer. If the read completes successfully, then the target address is incremented by one sector. If the sector is not found, a CRC error is indicated, or a D bit is encountered, the target address is not incremented.

If an IBM disc is present, then the target sector's 128 bytes are read into the controller's buffer. If the read completes successfully, then the target address is incremented by one. If the target sector is not found, a CRC error is indicated, or the D bit is encountered, then the target address is not incremented.

After the data has been buffered into the controller, the parallel poll response is re-enabled, indicating that the device has data ready to transmit. The bus controller should request the data by issuing the "Send Data" secondary. Upon receiving the secondary, the 7902/9895K again disables parallel poll.

If the read was terminated before data was loaded into the buffer (i.e., any error except CRC or D bit on), the device will respond by sending an EOI tagged byte and enabling parallel poll response.

If there was no error, the sector's worth of data is made available. The bus controller can take any number of bytes up to a sector's length. If more than one sector is requested, the 7902/9895K will send a byte tagged with an EOI. The number of bytes taken has no effect on the updating of the target address.

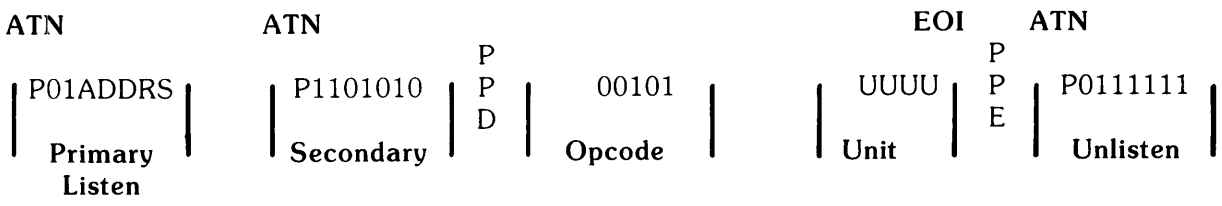
If the D bit or CRC error occurs, the corresponding data may be invalid.

Parallel poll response will be enabled after sending the last byte, sending another secondary to the 7902/9895K or by untalking the 7902/9895K.

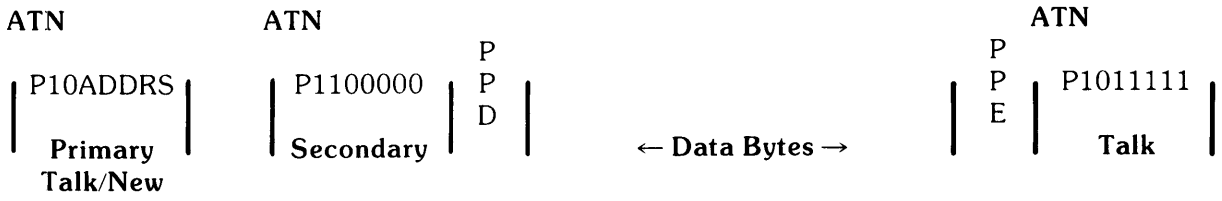
If more than one sector is to be transferred, then any number of buffered reads can be used in succession. If an error is encountered, all following reads will be held off due to a bad DSJ, so there is no chance of an error in the middle of a long read going unreported. However, error detection will be hastened if a DSJ is used after each read.

HP-IB Sequence:

Buffered Read Request



Send Data Request



status:

No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful read.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution:

1. Unit 0 <= U <= 3
2. DSJ <> 2
3. Disc present and ready
4. Not first status
5. Stat 1 = Normal completion,
   I/O program error, or,
   Illegal opcode error.
6. Disc format is HP or IBM.

Parallel Poll:

The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

An extra byte (the value of 1) tagged with an EOI will be sent if the controller requests more than the specified number of bytes. However, this request is not necessary for normal operations.

Unbuffered Read

Type:

Disc read.

Purpose:

The unbuffered read allows more than one sector to be transferred from the disc to the bus controller using a single command.

Description:

Following reception of the Read command, parallel poll response is disabled and the status of the selected unit is checked. If the unit can be accessed (requirements for execution), the internal buffer is filled with a sector of data from the disc, just as in the buffered read. Now the 7902/9895K waits for the Send Data command, then begins sending data to the bus controller. When all the bytes from the sector have been sent, the 7902/9895K then reads the next sector into the internal buffer and sends it to the bus controller. This process continues until a termination condition is reached:

If the unit becomes unavailable, or a sector cannot be found when the buffer is empty, or if a CRC error or D bit is encountered, the sector in the buffer is sent followed by an EOI.

If at any time during the operation the device notices that it has been untalked or that the bus controller has sent a byte, the process is stopped.

Following any of the above terminations, status is updated and parallel poll response is re-enabled. If there was an error in reading the data from the disc, the target address is left pointing to the sector in which the error occurred. Otherwise, the target address points to the sector following the last sector read from the disc. Occurrence of the error will cause a dummy byte tagged with EOI to be transmitted to the host system, thereby terminating the read process.

As has been seen, the unbuffered read actually uses the internal buffer to store the data. However, the protocol used is unbuffered in that the parallel poll response is not used to indicate when data is available. Thus, there is a pause in data flow to the HP-IB each time the buffer is re-filled from the disc. This pause occurs at the beginning of the read and after every sector has been transferred. Depending on when the read is started and the sector interleaving, this pause may be up to 160 milliseconds long.

HP-IB Sequence:

Unbuffered Read Request

ATN	ATN			EOI	ATN
P01ADDRS	P1101000	PPD	00101	UUUU PPE	P0111111
Primary Listen	**Secondary**		**Opcode**	**Unit**	**Unlisten**

Send Data Request

ATN	ATN			EOI	ATN
P10ADDRS	P1100000	PPD	← Data Bytes →	PPE	P1011111
Primary Talk	**Secondary**				**Untalk**

Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful read.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirement for Execution: See Buffered Read.

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

Verify

Type: Disc read.

Purpose: The Verify command is a read with reduced margins which does not transfer data to the HP-IB. This is useful for performing a surface analysis of the disc or checking the integrity of the data on the disc.

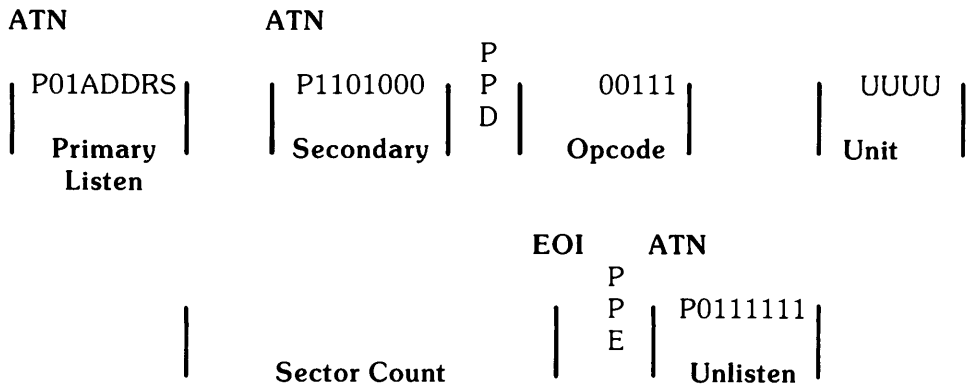
Description: As with other read commands, parallel poll is disabled, the availability of the unit is checked, and the target sector is sought. Starting with the target sector, consecutive sectors are read using reduced margins until any of the following occurs:

1. Unable to begin verify operation,
2. Sector count given in the command expires,
3. A seek or read error occurs,
4. A sector marked defective is detected,
5. The end of the disc is reached.

Parallel poll response is re-enabled upon completion of the verify. If an error was detected, the target address points to the sector in which the error occurred. Otherwise, the target address points to the sector following the last sector read.

HP-IB Sequence:

Verify Request



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Verify error.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution:

1. 0 <= Unit <= 3
2. DSJ <> 2
3. Disc present and ready
4. Not first status bit
5. Sector count >= 0
6. Disc of known format.

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Buffered Read Verify

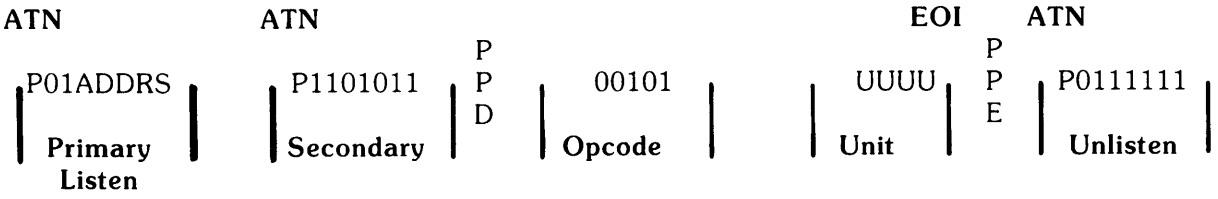
Type: Disc read.

Purpose: The buffered read verify is identical to the Buffered Read command except that the margins for good data are reduced. This command gives a high confidence that the data on the disc is recoverable.

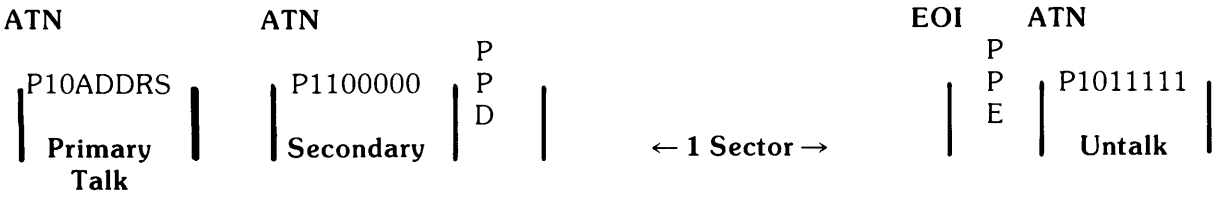
Description: See Buffered Read.

HP-IB Sequence:

Request Buffered Read Verify



Send Data



Status: See Buffered Read.

Requirements for Execution: See Buffered Read.

Unbuffered Read Verify

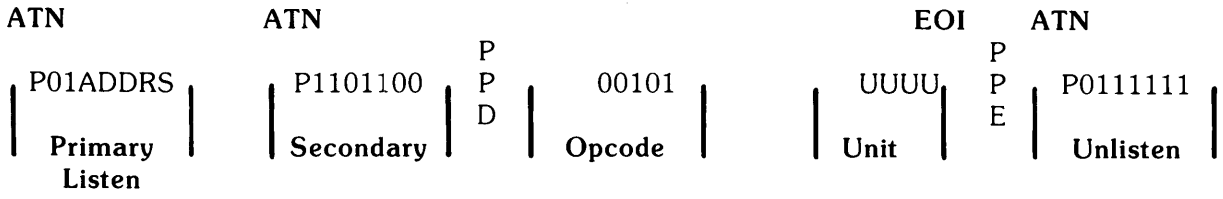
Type: Disc read.

Purpose: The unbuffered ready verify is identical to the Unbuffered Read command except that the margins for good data are reduced. This command gives a high confidence that the data on the disc is recoverable.

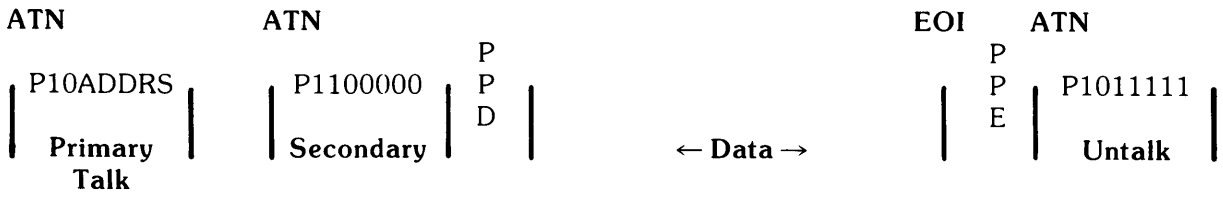
Description: See Unbuffered Read.

HP-IB Sequence:

Request Unbuffered Read Verify



Send Data



Status: See Unbuffered Read.

Requirements for Execution: See Unbuffered Read.

Cold Load Read

Type: Disc read.

Purpose: The cold load read is a command to read from unit 0, cylinder 0 at a specified head and sector address. This command consists of a seek to cylinder 0 followed by a read operation starting at the specified head and sector. Consecutive sectors are read until the bus controller stops the read.

Description: Following reception of the Read command, parallel poll is disabled, the DSJ cleared and the first status bit checked. If first status is set, the format of the disc is determined and the first status bit cleared. If the unit can be accessed, the 7902/9895K performs a seek to cylinder 0, reads the specified sector into the internal buffer, then asserts parallel poll waiting for the send data secondary. After the send data secondary is received, parallel poll is disabled and the buffered sector is sent to the bus controller. When the sector has been sent, the controller fills the buffer with the next sector from the disc and then sends it to the bus controller. This process is repeated until one of the terminating conditions occurs:

1. If the unit becomes unavailable or a sector cannot be found when the buffer is empty, a byte tagged with EOI is sent.
2. If a CRC error or D bit is encountered, the sector is sent followed by a byte tagged with an EOI.

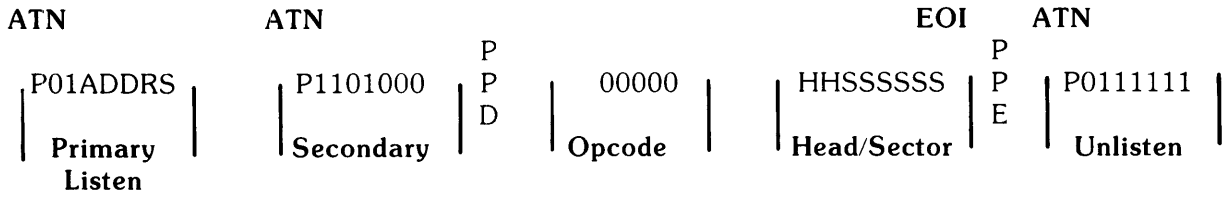
3. If at any time during the operation the device notices that it has been untalked or that the bus controller has sent a byte, the transfer will be stopped.

Following any of the above terminations, status is updated and parallel poll response is re-enabled. If there was an error in reading data from the disc, the target address is left pointing to the sector in which the error occurred. Otherwise, the target sector points to the sector following the last sector read from the disc.

The cold load read uses unbuffered HP-IB protocol, although all sector transfers take place through the buffer. Thus, there is a pause in data flow to the HP-IB each time the buffer is re-filled from the disc. This pause occurs at the beginning of the read and after every sector is transferred. Depending on when the read is started and the staggering of the sectors (see the Format command), this inter-sector pause may be up to 160 milliseconds long.

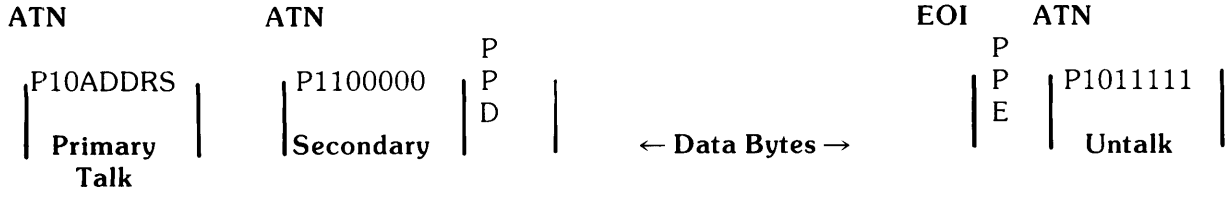
HP-IB Sequence:

Cold Load Read Request



Where: HH – Head address
SSSSSS – Sector address

Send Data



Status:

No errors.

S1 – 0
Stat 2 – Type field updated.
DSJ – 0

Unsuccessful read.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 0

Requirements for Execution:

1. Unit available,
2. Disc ready,
3. Disc of known format,
4. Valid head and sector number.

Parallel Poll: If less than the specified number of bytes is accepted by the HP-IB controller, the parallel poll response will be re-enabled by the Untalk command.

ID Triggered Read

Type: Disc read.

Purpose: ID triggered read is used to read a sector of which the ID field cannot be found or read correctly. As an example, if the status from a read indicates that the target address sector is not found, the ID triggered read would be used to locate and trigger off of the previous sector's ID field to read the target sector. The host processor must be aware of the sector interleaving to request the correct sector to trigger from (see Format).

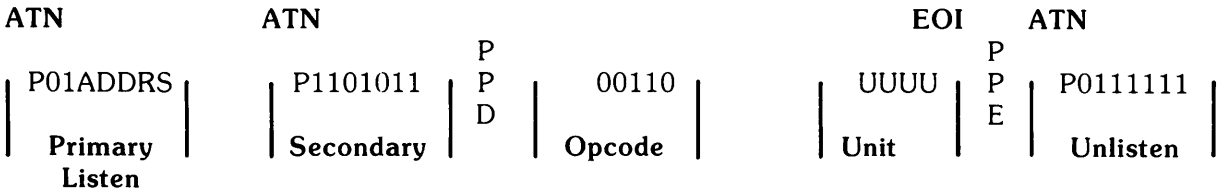
NOTE

ID triggered read is only supported for HP format and uses buffered protocol.

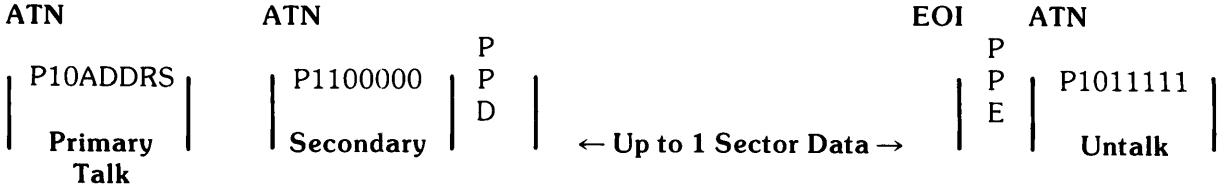
Description:

HP-IB Sequence:

Request ID Triggered Read



Send Data



Status: See Buffered Read.

Requirements for Execution: Disc must be in HP format. See Buffered Read.

Disc Write Commands

Buffered Write

Type: Disc write.

Purpose: The disc controller takes data transmitted on the HP-IB and stores it in an internal buffer before writing it on the disc. This buffering allows the host system to transmit asynchronously from an arbitrarily slow rate to about 190K bytes per second. The maximum HP-IB data rate is faster than the data rate to the disc, thus less time is used to transfer one sector over the HP-IB than it takes to write that sector. During the remaining time the HP-IB is free to be used by other devices on the bus.

Description: Following reception of the Write command, parallel poll response is disabled, status of the specified unit is checked and the parallel poll response is re-enabled.

At this time the bus controller should send the receive data secondary followed by up to one sector of data bytes. After seeing the receive data secondary, the 7902/9895K will disable parallel poll response and begin placing data bytes in its buffer. The 7902/9895K will stop accepting bytes after:

1. It receives a byte tagged with an EOI,
2. It has accepted one sector.

NOTE

If less than one sector is sent, the sector will be filled with data in the buffer from previous operations.

After the buffer has been accepted by the controller, the current address is checked with the target address. If they differ, a seek to the target cylinder is performed. This may occur if the actuator has slipped or if an auto-increment to the next cylinder is required.

If an HP format disc is being used, the 7902/9895K attempts to write the 256 bytes in the buffer to the target sector. If the write completes successfully, the target address is incremented by one sector. If the target sector cannot be found or a D bit is encountered, the sector is not written and the target track is not incremented.

If an IBM format disc is being used, only 128 bytes from the buffer are written to the disc. If the write completes successfully, the target address is incremented by one sector. If the target sector is not found, the sector is not written and the target address not updated.

NOTE

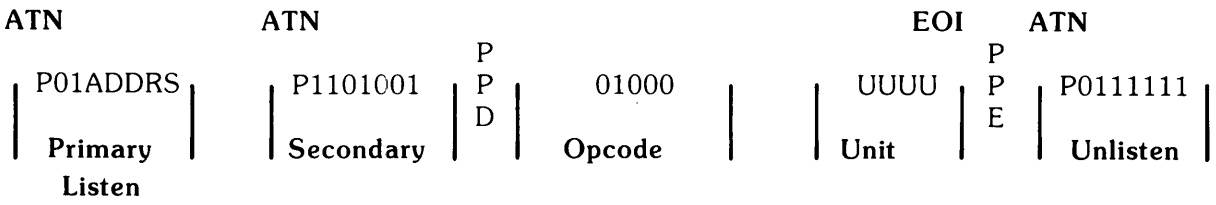
In IBM format, writing to a sector which has the D bit on clears the D bit.

Parallel poll is re-enabled after the write completes or aborts.

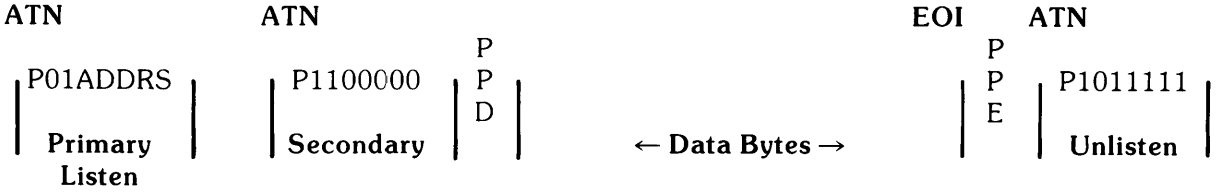
If more than one sector is to be written, any number of write commands can be used in succession. The 7902/9895K will update the target address automatically. A write will fail if it follows another write which failed, so there is no chance of an error in the middle of a long transfer going unreported. However, error detection will be quickened if a DSJ is used after each write sequence is completed.

HP-IB Sequence:

Buffered Write Request



Receive Data



Status:

No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful write.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution:

1. 2 data bytes in command
2. 0 <= Unit <= 3
3. DSJ <> 2
4. Disc present and ready
5. First status bit not set
6. Stat 1 = Normal completion,
   I/O program error or illegal opcode error
7. Disc not write protected

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Unbuffered Write

Type: Disc write.

Purpose: The unbuffered write allows more than one sector to be transferred from the bus controller to the disc using a single HP-IB command sequence. Due to the inability to share the HP-IB during the transfer, the unbuffered write is not the preferred mode when HP-IB performance is desired.

Description: Following reception of the Write command, parallel poll response is disabled and status of the specified unit is checked. The 7902/9895K now waits for the receive data secondary and then fills its internal buffer with one sector from the bus controller. When the buffer is full, the 7902/9895K searches for the target sector and writes the buffer to it. When the buffer has been emptied, the 7902/9895K accepts another sector from the HP-IB and in turn writes it to the next sector of the disc. This process continues until a byte tagged with an EOI is received or an error occurs. The buffer containing the byte tagged with the EOI is written to the disc before the write completes.

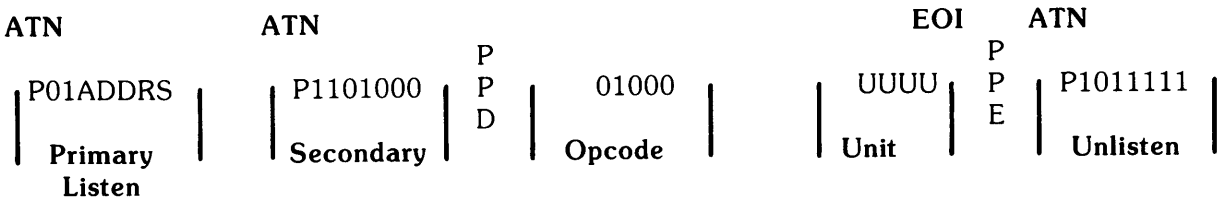
If an error occurs (i.e., drive goes not ready, an HP format D bit is encountered, the sector can't be found, etc.), writing to the disc will stop, but the 7902/9895K will continue accepting bytes until an EOI tagged byte is received.

If an error occurs, the target address will point to the sector in which it occurred. Otherwise, the target address will point to the sector following the last sector written. When writing has been completed, parallel poll response will be re-enabled.

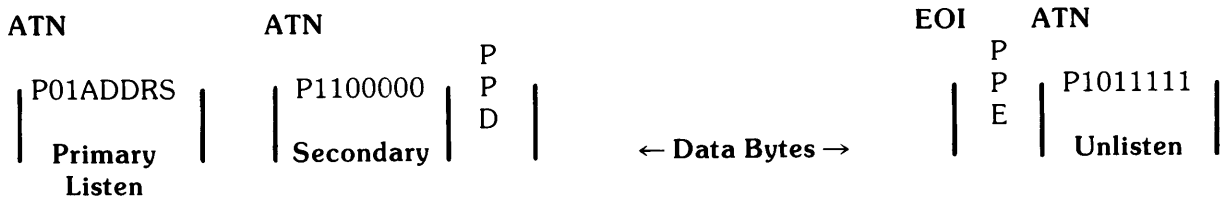
As in the unbuffered read, unbuffered write actually uses the internal buffer of the controller. However, the protocol used is unbuffered in that parallel poll is not used to indicate when data may be sent to the 7902/9895K. Like unbuffered read, there is a pause in the data flow to the 7902/9895K each time the buffer is written to the disc. The pause occurs after each sector is transferred. Depending on when the write starts and the staggering of the sectors (see the Format command), this pause may be up to 160 milliseconds long.

HP-IB Sequence:

Unbuffered Write Request



Receive Data



Status:

No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful write.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution: See Buffered Write Command.

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Initialize

Type: Disc write.

Purpose: The Initialize command is used to set or re-set D bits. It is similar to the buffered write with the following exception:

1. For HP format discs, all D bits on the target track will be set or re-set before the target sector is written.
2. For IBM format discs, the D bits of the target sector are set or re-set as the sector is written.

The Initialize command is especially useful when used with the Format command to make invisible tracks.

Description: Following reception of the Initialize command, parallel poll is disabled and the status of the selected unit is checked.

If an HP format disc is present, the entire target track is re-formatted, with the D bit in all sectors set or re-set according to the D bit specified in the opcode byte of the command. This re-formatting has several results:

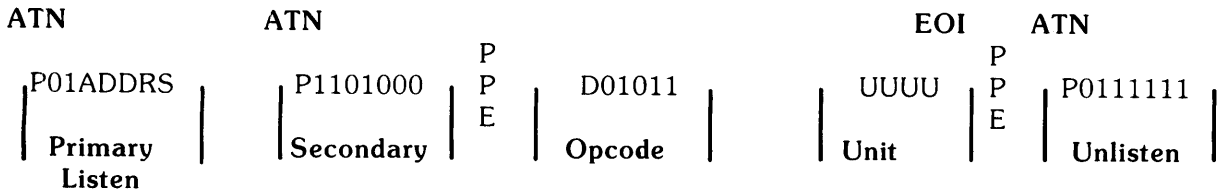
1. All data on the target track is lost,
2. The sector interleave of the track is changed to 2 (every other sector),
3. The spiral offset of the target track may no longer be optimal.

If an IBM format disc is present, the D bit is set or re-set according to the D bit specified in the opcode data byte as each sector is written. The initialization of an IBM sector does not affect the format or data of the remaining sectors of the target track, as does an HP format.

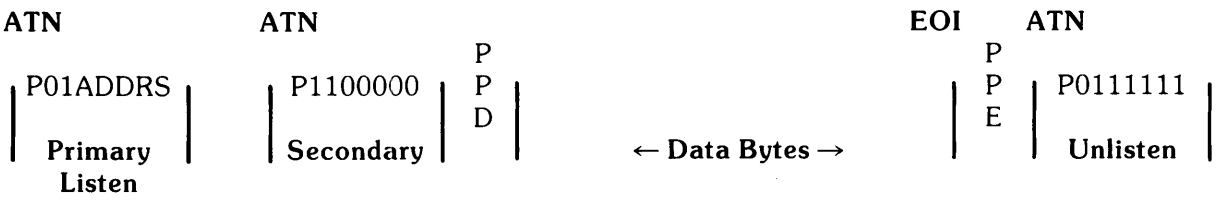
After the initialize request is sent, the command accepts and writes data in a manner identical to the Buffered Write command.

HP-IB Sequence:

Initialize Request



Receive Data



Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful.

S1 – Error
Stat 2 – Bits A, E and C set, if appropriate.
DSJ – 1

Requirements for Execution: See Buffered Write requirement.

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.

Format

Type: Disc write.

Purpose: The Format command is a part of the sequence of commands which changes a disc which is unformatted or has the wrong format into a disc with a usable format. The 7902/9895K supports three types of formats: HP double density, single- or double-sided and single-sided standard IBM format disc. The formatting operation also can make tracks marked with the D bit into invisible tracks.

The format sequence was designed to allow the disc controller to do as much of the work of formatting as possible, but still allow the host system to set its own criteria for:

1. Format type,
2. Bad track detection,
3. Sector interleave,
4. Spiral offset,
5. Format data byte.

Description: After receiving the Format command, parallel poll is disabled and the status of the specified unit is checked. If the unit can be used, the disc is formatted according to the type, old format override, interleave and selected data byte.

If the disc is of a different format than the Format command requests or the override old format bit is set, the entire disc will be formatted without invisible tracks.

If the disc is the same type as that requested by the Format command and the override old format bit is not set, 7902/9895K will attempt to read from each track before it is formatted and make that track invisible if:

1. The track is already invisible,
2. A sector with a D bit set is found,
3. The track has no readable sectors.

NOTE

The 7902/9895K looks at the D bit of a random sector to decide whether or not to make that track invisible. HP format requires that the D bit of all the sectors be set so there is no problem. But, IBM format allows a mixture of set and cleared D bits on one track. Therefore, before formatting an IBM disc, all D bits on a good track should be cleared and all D bits on a bad track set.

If the type parameter is set to 2, the disc will be given HP format. Double-sided discs will automatically be formatted on both sides, and single-sided disc only on head 0. If the type parameter is set to 8, the disc will be formatted IBM. Double-sided discs are not supported in IBM format. Single-sided discs will be formatted on head 0 only (IBM standard). Other values of type will cause an I/O program error.

The interleave parameter determines the order in which the sectors occur on a track. Data transfers which use the internal buffer on the 7902/9895K, or host systems that accept data slower than the disc rate, operate more efficiently if the ordering of the sectors is non-sequential. Non-sequential sectors ordering allows for sectors to be arranged on the disc by logical use instead of by physical location.

In general, the interleave parameter indicates the number of disc revolutions required to send or receive one track's worth of data. For example, an interleave value of 5 would indicate that the sectors would be arranged on the disc in a manner that would require five revolutions to read one track.

NOTE

An interleave parameter value of 2 (two revolutions per track) generates the sector sequence with the minimum time required to transfer one track.

HP format also uses the interleave parameter to determine the inter-track spiral offset. This offset minimizes the effect of track-to-track seeks by physically arranging sector 29 of one track and sector 0 of the next to make the track seek time approximately the same as the rotational latency.

HP-IB Sequence:

Format Request

ATN	ATN					
P01ADDRS	P1101100	P P D	11000		UUUU	FTTTTTTT
Primary Listen	**Secondary**		**Opcode**		**Unit**	**Type**

			EOI	ATN
			P P E	P0111111
Interleave		**Data Byte**		**Unlisten**

Where: ADDRS – 7902/9895K HP-IB address
F – Override old format bit
TTTTTTT – Wanted format type
2 – HP
8 – IBM
Interleave – 1 to 29 for HP
– 1 to 25 for IBM

Status: No errors.

S1 – 0
Stat 2 – Unchanged
DSJ – 0

Unsuccessful.

S1 – Error
Stat 2 – Bits A, F and C set, if appropriate.
DSJ – 1

Parallel Poll: The parallel poll response is re-enabled after the operation is completed, normally or abnormally.