HEWLETT PACKARD

INSTALLATION AND SERVICE MANUAL

MODEL 13037A
DISC CONTROLLER

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GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION

This installation and service manual covers general information, installation, an instruction set, theory of operation, preventive maintenance, adjustments, troubleshooting, replacement procedures, and a list of replaceable parts for the HP 13037A Disc Controller (figure 1-1). This section covers a general description, identification, supporting documentation, and other basic information.

The various sections in this manual provide information as follows:

a. SECTION II, INSTALLATION. Provides information relative to unpacking and inspection, power requirements, mounting, and checkout.

b. SECTION III, CONTROLLER INSTRUCTION SET. Provides a listing and description of the command words which operate the controller and, in turn, are converted to commands for the disc drive.

c. SECTION IV, THEORY OF OPERATION. Provides an overall functional description and block diagram to the "board" level.

d. SECTION V, SERVICE. Provides preventive maintenance information, safety precautions, suggested reference material, and flowcharts for troubleshooting analysis.

e. SECTION VI, REPLACEABLE PARTS. Provides ordering information for all replaceable parts and assemblies on a "board-level" exchange basis.

1-2. GENERAL DESCRIPTION

The HP 13037A Disc Controller is a microprocessor-controlled device capable of connecting up to eight HP 7905A Disc Drives to a computer interface. The controller is capable of supporting one or two interface ports, which in turn, can be connected to one or two different computers.

The function of the controller is to take high-level command words and translate them into commands which are intelligible to the disc drive. In so doing, the controller takes steps to ensure data integrity. Errors are detected

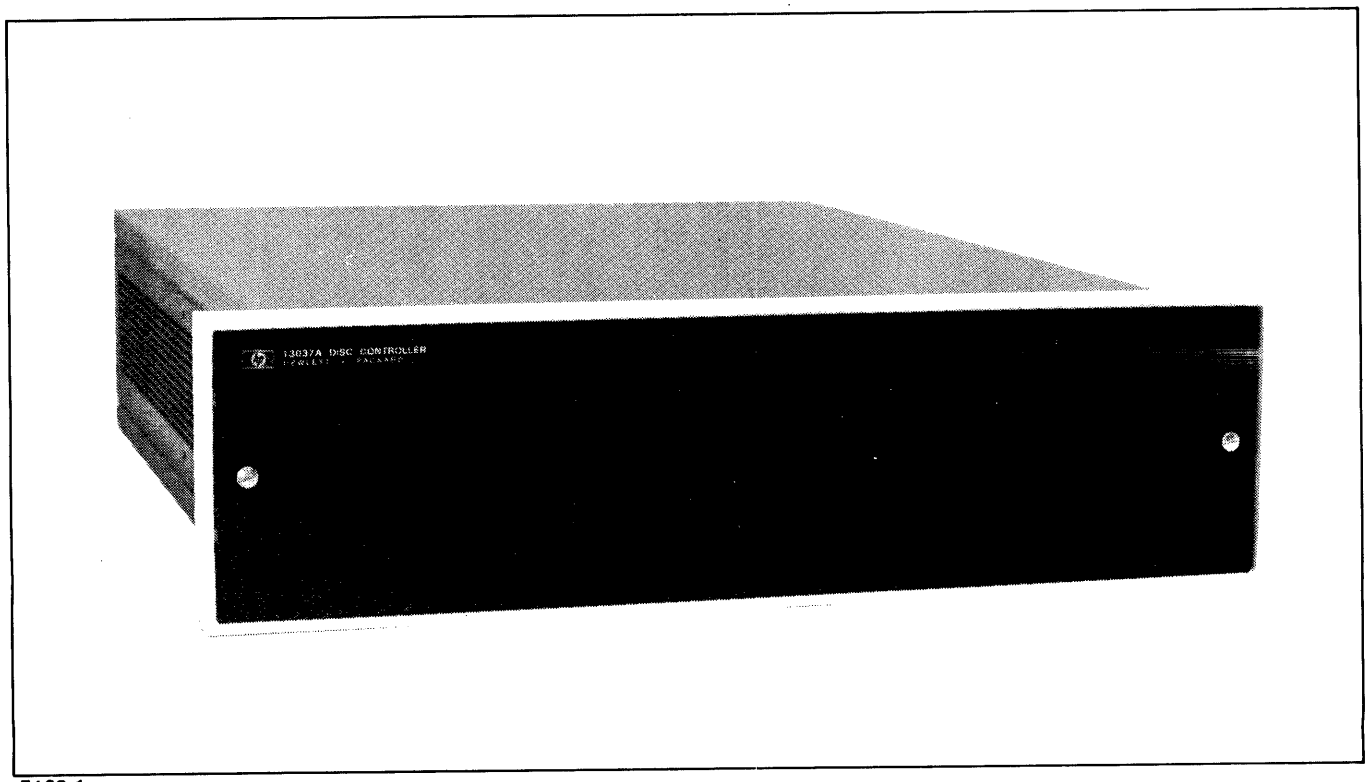

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Figure 1-1. HP 13037A Disc Controller

and certain types can be corrected. Software must be invoked for correcting an error. If the error is uncorrectable, the computer interface is notified. Along with the translation of commands, the controller transfers data bidirectionally between a disc drive and computer interface.

1-3. CONTROLLER ASSEMBLIES

Three printed-circuit assemblies (PCA's) and a chassis make up the controller; each PCA is an input/output (I/O) assembly that is plugged into the controller chassis. The PCA's are as follows: microprocessor (part no. 13037-60001), device controller (part no. 13037-60002), and error correct (part no. 13037-60004). Additionally, a power regulator PCA (part no. 13037-60018) is mounted in the controller chassis and supplies all necessary power to the above mentioned PCA's.

1-4. SERVICE DOCUMENTATION AVAILABLE

The following additional service documentation may be ordered from a Hewlett-Packard Sales and Service office. Sales and Service offices are listed at the back of this manual.

a. *HP 7905A Disc Drive Installation and Service Manual,* part no. 07905-90007.

b. *HP 12962A Disc Subsystem Installation and Service Manual*, part no. 12962-90003.

c. *HP 7905A Disc Drive Operator's Manual*, part no. 07905-90009.

d. *HP 30129A Disc Subsystem Installation and Service Manual*, part no. 30129-90003.

e. *HP 12962A Cartridge Disc Subsystem Diagnostic Reference Manual*, part no. 12962-90001.

f. *Stand-Alone HP 30129A Cartridge Disc Diagnostic*, part no. 30129-90006.

INSTALLATION

SECTION II

2-1. INTRODUCTION

This section provides installation instructions for the controller. Included in these instructions are site preparation data, unpacking and inspection, installation procedures, claims procedures, and recommended packing and shipping methods.

2-2. SITE PREPARATION

Site preparation information for the controller includes environmental limitations, power requirements, and mounting considerations.

2-3. ENVIRONMENTAL LIMITATIONS

Environmental limitations for operating and non-operating conditions of the controller are specified in table 2-1. The environmental limitations imposed by other peripheral devices must be considered when these devices are located adjacent to the controller.

Table 2-1. Controller Environmental Limitations

AMBIENT TEMPERATURE	
Operating:	0° to 55°C (32° to 131°F)
Non-operating:	−40° to 75°C (−40° to 167°F)
ALTITUDE	
Operating:	4,573 meters (15,000 feet)
Non-operating:	7,622 meters (25,000 feet)
RELATIVE HUMIDITY	
0 to 95% at 25° to 40°C (77° to 104°F) without condensation.	

2-4. POWER REQUIREMENTS

The controller is shipped with the flexibility to operate from single-phase power mains of 100/120 volts at 2 amperes or 220/240 volts at 1 ampere. (See figure 2-3.) The line voltage may vary −10 to +5 percent of the nominal value. The line frequency may vary from 47 to 66 Hz. Maximum power consumption of the HP 13037A is 220 watts.

Various safety codes require that instrument chassis, panels, and housings be grounded to protect operating and service personnel. A grounded three-conductor female power outlet must be made available to satisfy this requirement.

2-5. COOLING REQUIREMENTS

There are no external cooling requirements for the controller. Internal fans provide adequate ventilation when operated within the environmental limitations specified in table 2-1.

2-6. MOUNTING CONSIDERATIONS

The controller is housed in a 133-millimeter (5-1/4-inch) by 425-millimeter (16-3/4-inch) by 584-millimeter (23-inch) chassis. A rack mount kit (part no. 13037-60012) is provided to permit mounting the chassis in a standard 483-millimeter (19-inch) equipment rack. The weight of the controller is 15.9 kilograms (35 pounds) (with PCA's).

2-7. UNPACKING AND INSPECTION

When the controller shipment arrives, check to ensure receipt of the container as specified by the carrier's papers. Inspect the shipping container immediately upon receipt for evidence of mishandling during transit. If the container is damaged in any way, or if it is water-stained, request the carrier's agent be present when the container is opened.

Open the shipping container and locate the envelope marked "CUSTOMER RECORDS." One of the items in this envelope is a list of equipment supplied. Compare this list against the purchase order to verify that the shipment is correct. Unpack the shipping container and inspect each item for external damage. Look for damage such as broken controls and connectors, dented corners, bent panels, scratches, and loose components. Check also the rigid foam-plastic cushioning (if used) for signs of deformation which could be indicative of rough handling during transit.

If the visual examination reveals any damage to the controller, follow the damage-claim procedure described in paragraph 2-19. Retain the shipping container and packing material for examination in the settlement of claims or for future reuse.

2-8. INSTALLATION PROCEDURE

The following paragraphs describe installations with the controller enclosed in a chassis. If the controller chassis is not used and the PCA's are installed separately, refer to the appropriate document listed in section I of this manual.

2-9. MANUAL UPDATING

Before installing the controller, perform any updating that may be required for the HP 13037A Disc Controller documentation. (A list of directly related hardware and software documentation is provided in section I of this manual.) Updating instructions (if any) are provided with the appropriate document.

2-10. TOOLS AND TEST EQUIPMENT REQUIRED

2-11. TOOLS. No installation tools other than ordinary hand tools are required.

2-12. TEST EQUIPMENT. Test equipment required to verify adequacy of the ac mains voltage and proper adjustments of the controller power supply are listed in table 2-2.

Note: Even though the 30 MHz oscillator has an adjustable trim capacitor, no adjustment is required or should be made to the trimmer.

2-13. AC POWER INSTALLATION AND VERIFICATION

2-14. AC POWER MAINS OUTLET AND EXTERNAL GROUND. The female power outlet to be used to supply ac power to the controller must be checked by a qualified electrician to ensure that it furnishes the proper voltage for which the controller is configured. The outlet and its associated wiring and fuses (or circuit breakers) must be capable of carrying the current specified in paragraph 2-4.

Figures 2-1 and 2-2 illustrate and provide the necessary details on the various ac power cord configurations available. Make sure that the local electrical code permits use of the type of power cord furnished with the controller.

Have a qualified electrician check the power outlet with an ac voltmeter to ensure that the required single-phase voltage is present. For proper operation of the controller, the mains voltage must be in the range specified in paragraph 2-4. Bear in mind that the electrical load imposed by the controller may reduce the line voltage below the non-load value.

If the line voltage is in the correct range, have the electrician check the power outlet to ensure that it is wired correctly with respect to ac high potential, ac neutral, and equipment ground. If the outlet is wired improperly, corrections must be made by a qualified electrician.

For safety reasons, it is mandatory that a connection be made between the controller "chassis ground" and cabinet "ground". Also required is a connection between cabinet "ground" and "earth". Refer to the appropriate site preparation manual for electrical connection requirements. For installation in a mobile environment (e.g., a ship, an aircraft or a train), the chassis ground wire in the controller ac power cord must be connected to the hull or metal frame of the vehicle.

A line module, located on the rear panel below the power switch, allows operation on four different input line voltages. Voltage selection is made by a plug-in "circuit card". Figure 2-3 shows how the voltage selection is made.

Table 2-2. Installation Test Equipment

INSTRUMENT	CRITICAL SPECIFICATIONS	RECOMMENDED HP MODEL
Digital Voltmeter	At least four-digit readout. Minimum input impedance 10 megohms; full-scale ranges of 0.999 and 99.99 volts dc.	HP 3439A Digital Voltmeter with HP 3441A Range Selector.
AC Voltmeter	Expanded-scale or digital-readout type capable of measuring ac power mains to ±1.0%. Voltage range must be from 88 to 132 volts ac or 176 to 264 volts ac.	HP 3445 AC/DC Range Unit. Also performs functions of HP 3441A Range Selector listed above. Requires an HP 3449A Digital Voltmeter.

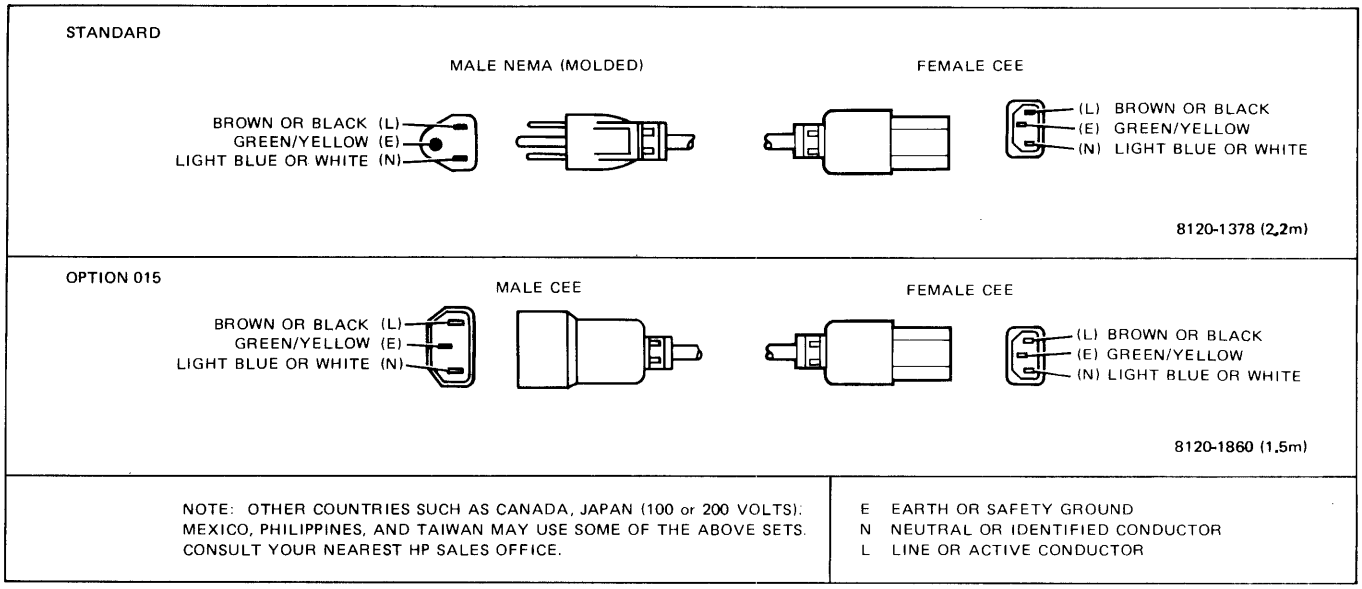

Figure 2-1. AC Power Cord Sets (USA)

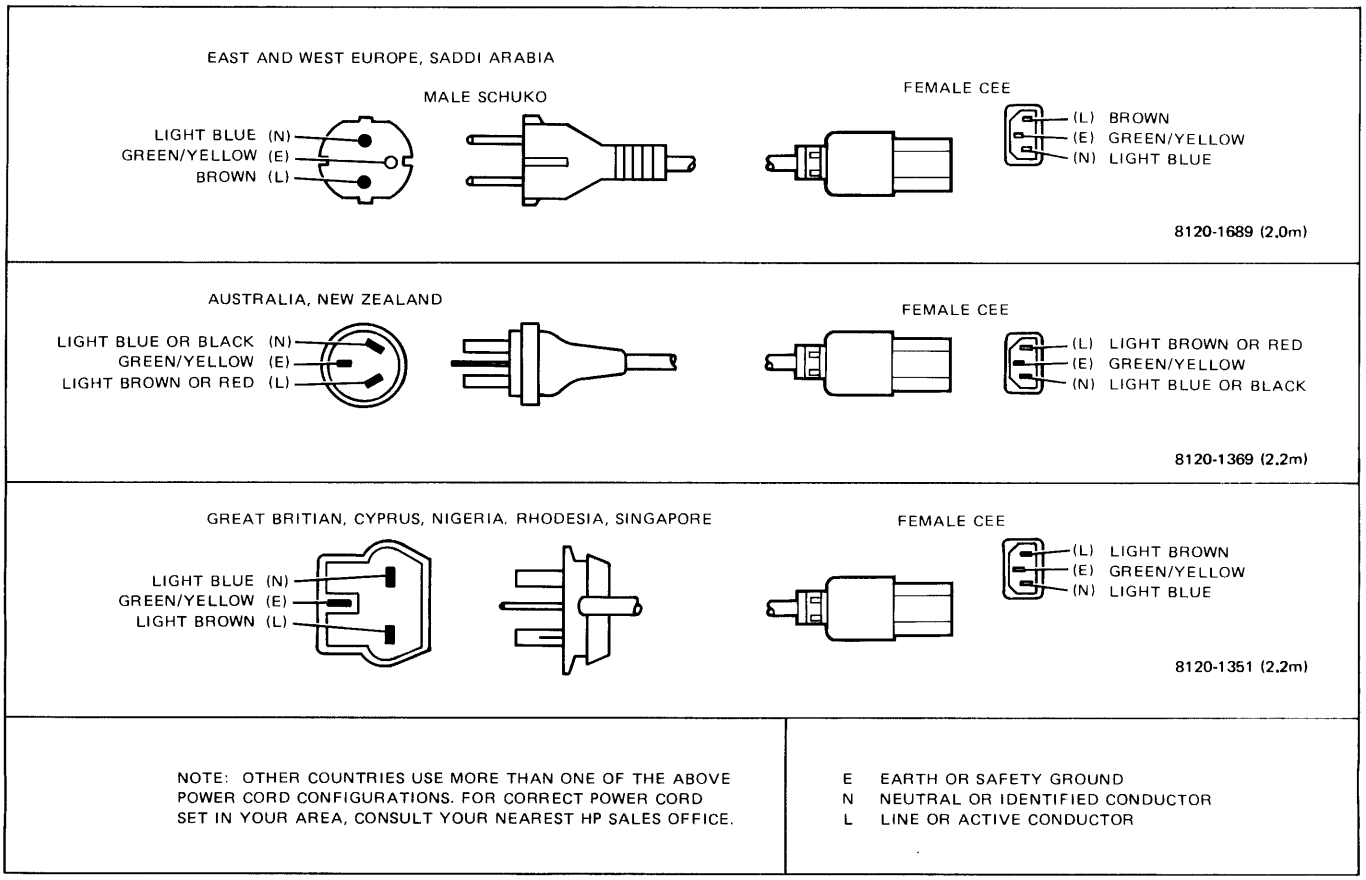

Figure 2-2. AC Power Cord Sets (Non-USA)

2-15. FUSE RATING CHECK. The controller is equipped with one primary power fuse (F1) and one secondary fuse (F2).

WARNING

Observe the warning label affixed to the rear panel when replacing the primary power fuse.

The primary power fuse is located on the rear panel in the line module. See figure 2-3 for proper insertion and removal of the fuse. Check that the rating of the primary power fuse conforms to the rating specified in table 2-3.

The secondary fuse is located on the power supply PCA. This fuse protects the +5 Vdc power supply. The required rating is 20A, 250V.

Table 2-3. Primary Power Fuse Rating

SOURCE VOLTAGE	REQUIRED RATING
100 Vac	4A, 250V
120 Vac	4A, 250V
220 Vac	2A, 250V
240 Vac	2A, 250V

2-16. MOUNTING INSTRUCTIONS

For most installations, the controller will be rack mounted in an equipment cabinet. The rack mounting kit, part no. 13037-60012, is provided for mounting the controller in an equipment cabinet. Mount the rails to the inside of the equipment cabinet according to the instructions furnished with the kit. Then install the controller in the equipment cabinet. Secure the controller to the equipment cabinet with four no. 10-32 rack mounting screws. Two screws are used on each side of the mounting flange.

2-17. POWER SUPPLY CHECK

Check the power supply voltages. Table 2-4 lists the power supply voltage ranges. The +5 Vdc is the only portion of the power supply that can be adjusted. Figure 2-4 shows the adjustment and test points.

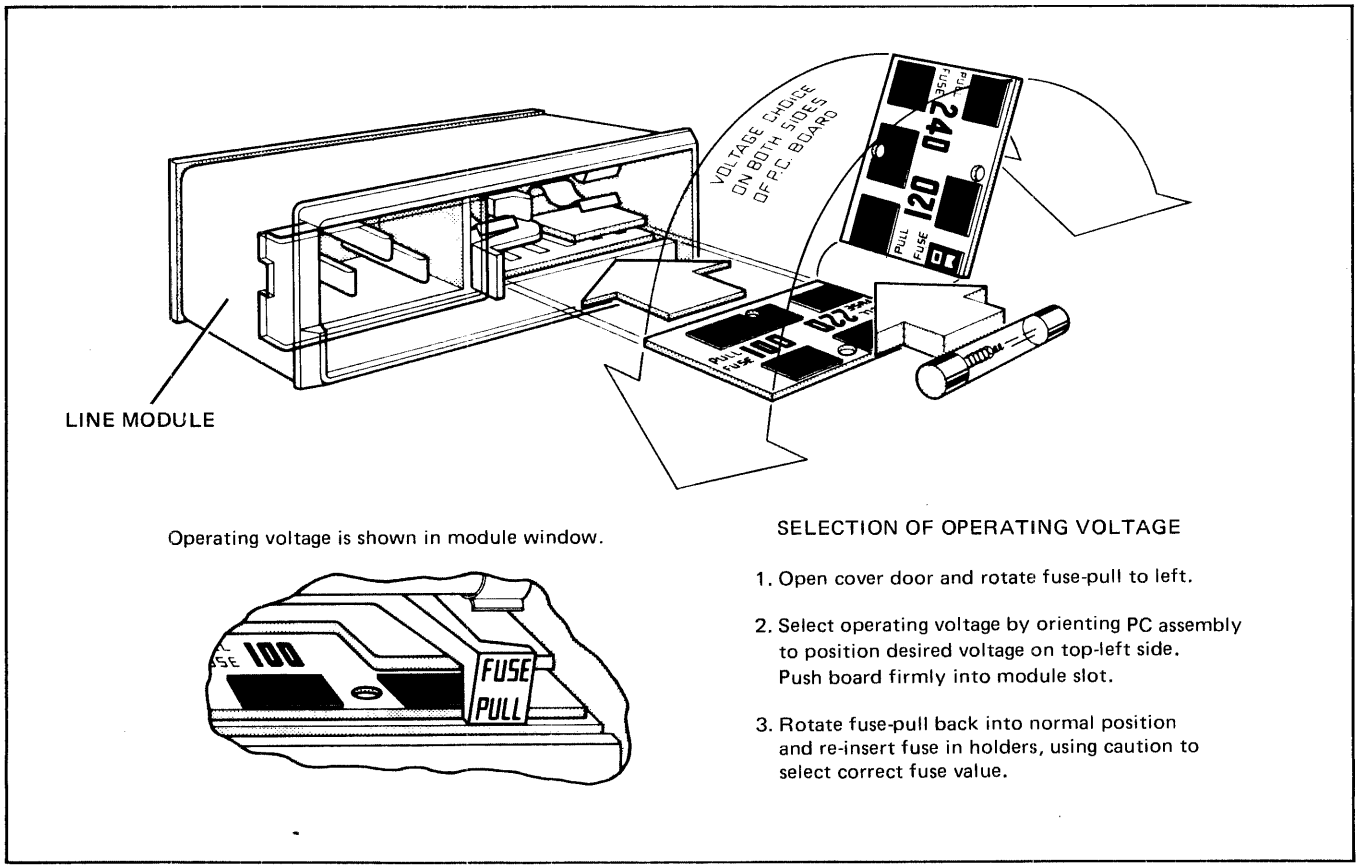

Figure 2-3. Line Module Voltage Selection

Plug the controller power cord into the power outlet and proceed as follows:

a. Remove the top cover.

WARNING

Hazardous voltages are exposed when the top cover is removed.

b. On rear panel, set POWER switch to ON.

c. Connect positive lead of digital voltmeter to +5V test point and connect common lead to common test point.

d. Check +5V; if not within range adjust +5V potentiometer (see figure 2-4) to obtain voltmeter indication listed in table 2-4.

e. Set POWER switch to OFF.

Table 2-4. Power Supply Voltage

SUPPLY	TEST POINT	RANGE
+5.1	+5V	+5.1 to +5.36
Common	↓	

f. Disconnect voltmeter and replace top cover on controller.

2-18. CONTROLLER PCA CONFIGURATION

Both the device controller and microprocessor PCA's must be installed adjacent to the error correction PCA. Figure 2-5 shows a recommended PCA configuration.

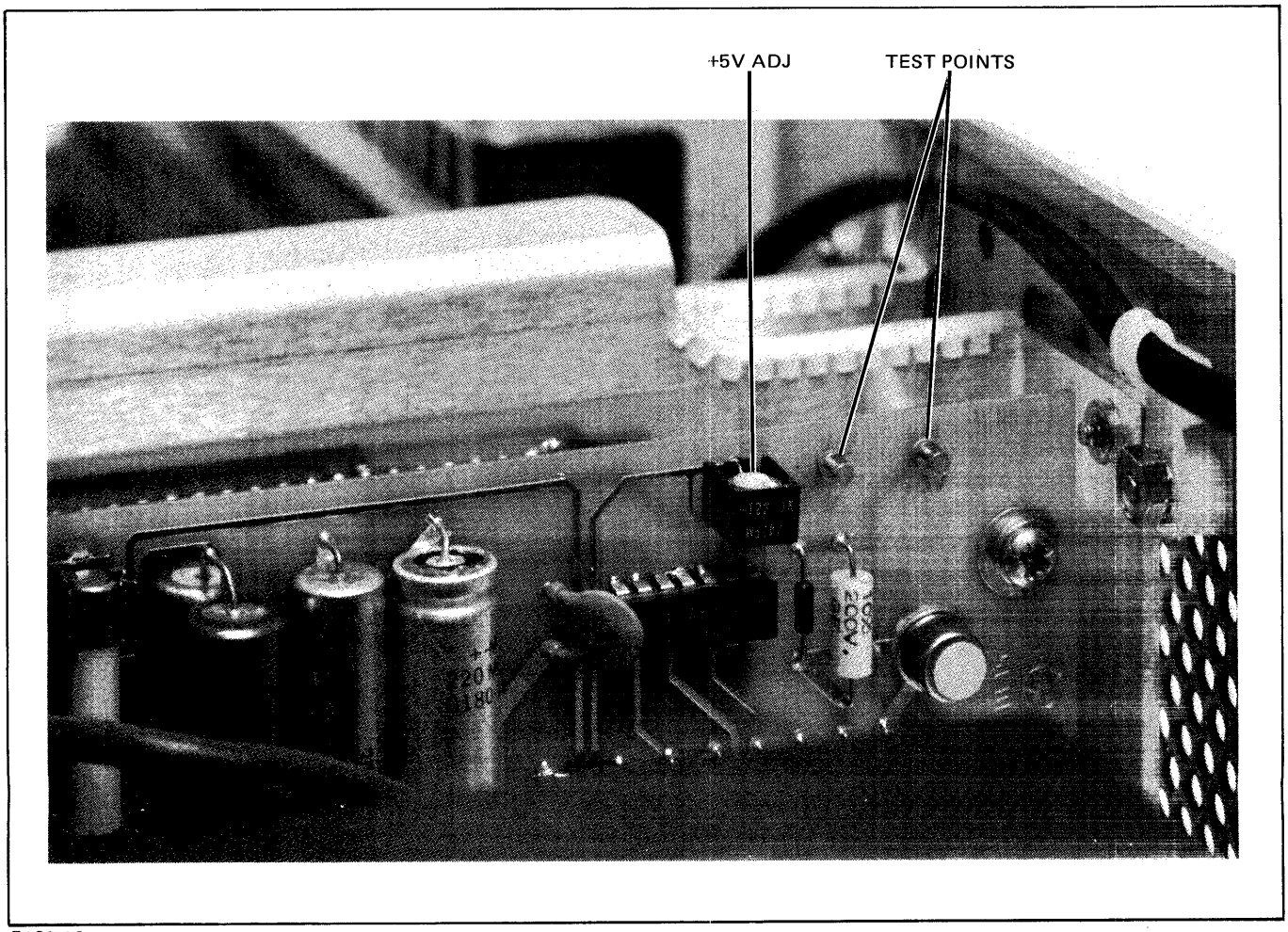

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Figure 2-4. Power Supply Adjustment and Test Points

2-19. CLAIMS PROCEDURE

If the shipment is incomplete or if the equipment is damaged or fails to meet specifications, notify the nearest Hewlett-Packard Sales and Service Office. If damage occurred in transit, notify the carrier, as well. Hewlett-Packard will arrange for replacement or repair without waiting for settlement of claims against the carrier. In the event of damage in transit, retain the shipping container(s) and packaging material for inspection.

2-20. REPACKAGING FOR SHIPMENT

The following paragraphs provide instructions for repackaging the controller for shipment. Included are instructions for shipping the controller using the original packaging or new packaging.

2-21. SHIPMENT USING ORIGINAL PACKAGING

The same containers and materials used in factory packaging can be used for reshipment of the controller. Alternatively, the correct containers and packing materials may be obtained from Hewlett-Packard Sales and Service Offices. Use the following instructions as a guide when packaging the controller with the original factory packaging materials:

a. If the controller is being sent to the factory for servicing, attach a tag specifying the return address, type of service or repair required, model number, and full serial number.

b. Seal the shipping container securely and mark it "FRAGILE" to ensure careful handling.

c. In any subsequent correspondence with the factory, refer to the controller by model number and full serial number.

2-22. SHIPMENT USING NEW PACKAGING

The following instructions should be used as a guide when packaging the controller with commercially available materials:

a. Wrap the controller in heavy paper or sheet plastic. If the controller is being sent to the factory for servicing, attach a tag specifying the return address, type of servicing or repair required, model number, and full serial number.

b. Use a strong shipping container. A double-wall carton constructed of 158.9-kilogram (350-pound) test material is adequate.

c. Use sufficient shock-absorbing material on all sides of the controller to provide a firm cushion and to prevent movement inside the container. Use particular care to protect the controller corners and chassis.

d. Seal the shipping container securely and mark it "FRAGILE" to ensure careful handling.

e. In any subsequent correspondence with the factory, refer to the controller by model number and full serial number.

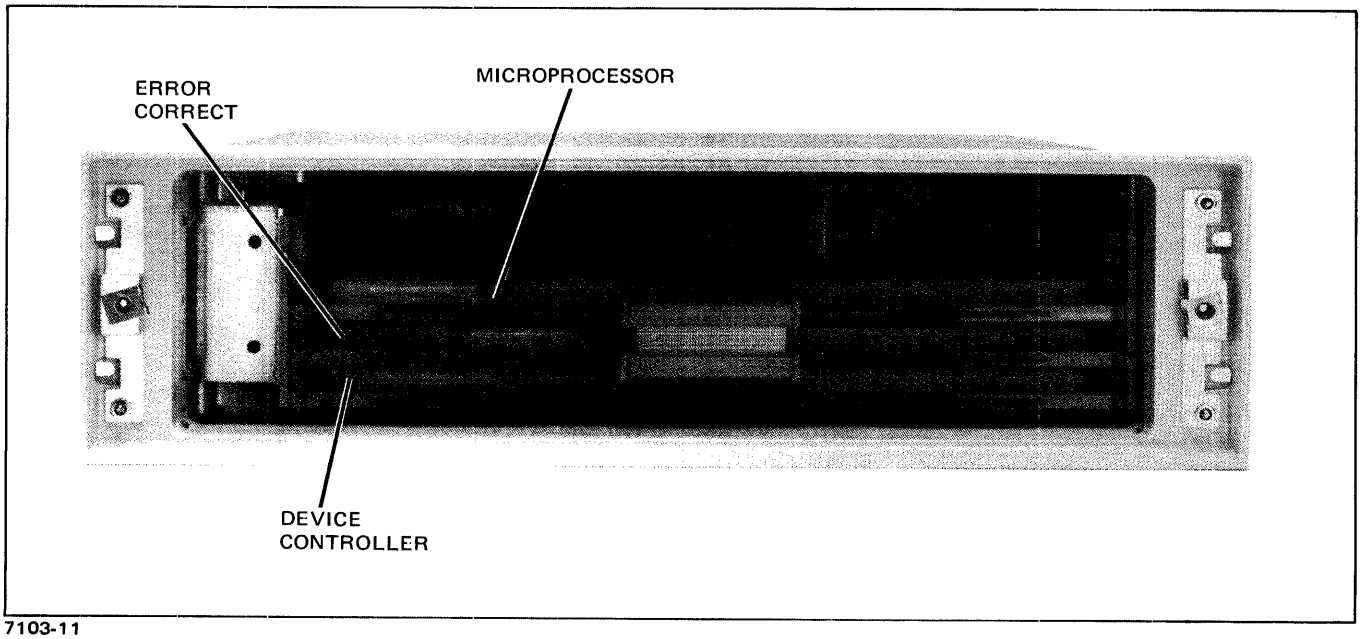

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Figure 2-5. Controller PCA Configuration

Section III

CONTROLLER INSTRUCTION SET

3-1. DISC DRIVE UNIT CHARACTERISTICS

To give the reader a better understanding of the relationship between the controller and disc drive, some of the disc drive characteristics and the controller instruction set are discussed in this section.

The HP 7905 Disc Drive contains two discs; one removable and the other fixed. (See figure 3-1.) It accesses the data on three surfaces with three read/write heads. Head positioning information and sector clock generation is derived from the fourth (servo) surface through the servo head on the fixed disc. There are 411 cylinders available for information storage. The cylinder address range is from zero to 410. Each cylinder consists of three tracks, one on each disc surface. Each track is divided into 48 sectors. Sectors are addressed by specifying a head and sector address within a cylinder. Head addresses range from zero to two and sector numbers range from zero to 47.

3-2. TRACK RECORDING FORMAT

The track recording format is shown in figure 3-2. Each track is divided into 48 equal sectors which are derived by counting transitions from the servo track. All are data sectors. Each sector has a sector number and sector address. The location of sector 0 is defined by an index mark. On the fixed disc, the index mark is a unique pattern on each servo track which indicates the location of sector 0 on the single recording surface. On the removable disc, the index mark is a small notch in the center hub which is detected as a magnetic discontinuity by a special transducer. Since the index mark of the removable disc is randomly aligned with that of the fixed disc, two sets of sector counting electronics are provided in the disc drive. Each of the counters is incremented once each sector and set to zero each time its index marker is sensed. When a data transfer command sequence is initiated, the controller transmits a cylinder, head, and sector address and then waits for the disc drive to respond by asserting a Sector Compare signal. The transfer is then initiated. When the controller issues a SEEK address to the drive, that address includes a sector number. After issuance, the controller disconnects from the disc drive and the computer which issued the command, and services other computers while waiting for the seek to complete. The disc drive does not notify the controller that the seek is complete until the heads have reached the proper cylinder and the addressed sector is some fixed number of sectors away from

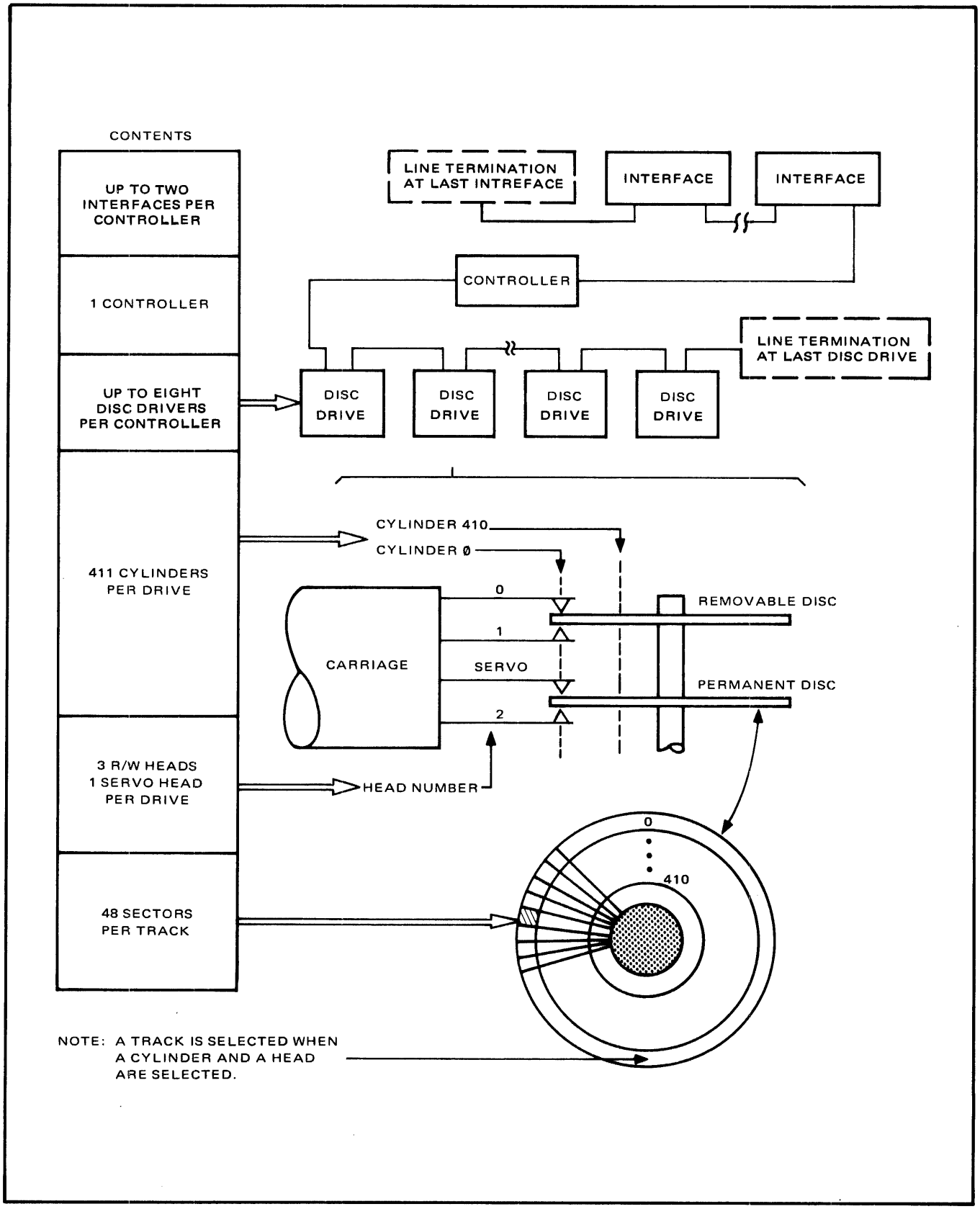


Figure 3-1. Addressing Structure of HP 7905A Disc Drive

rotating under the read/write heads (rotational position sensing -- RPS). This operation ensures that the controller and computer are free for as much time as possible, and are not tied up during disc latency. The controller can then notify the computer that the seek has completed and, when the computer issues the data transfer command, a minimum amount of time is lost waiting for the disc drive.

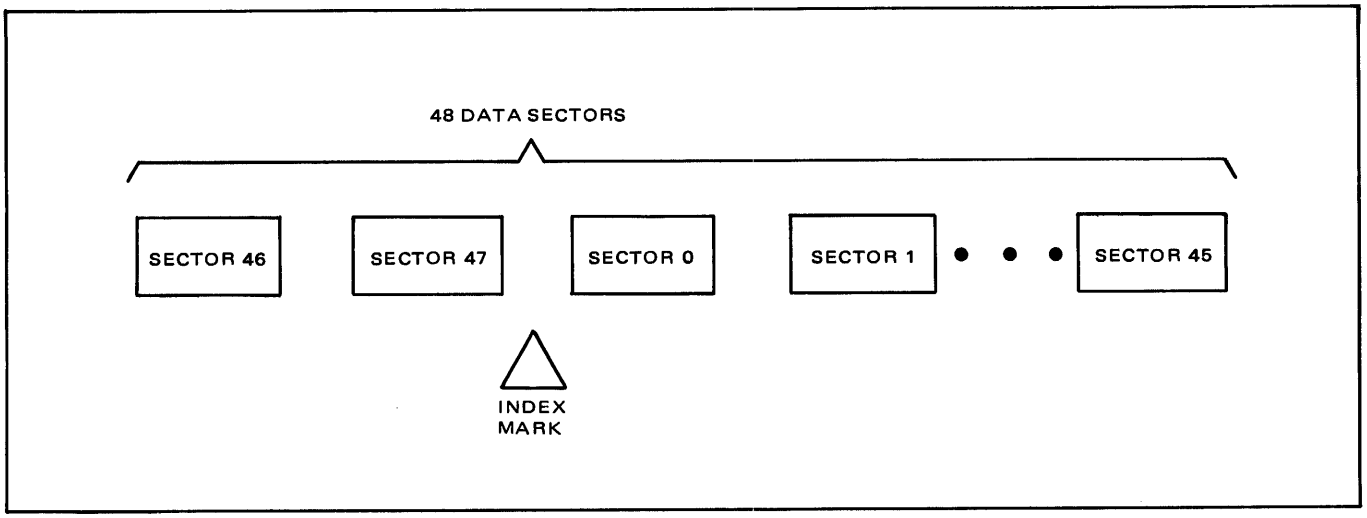
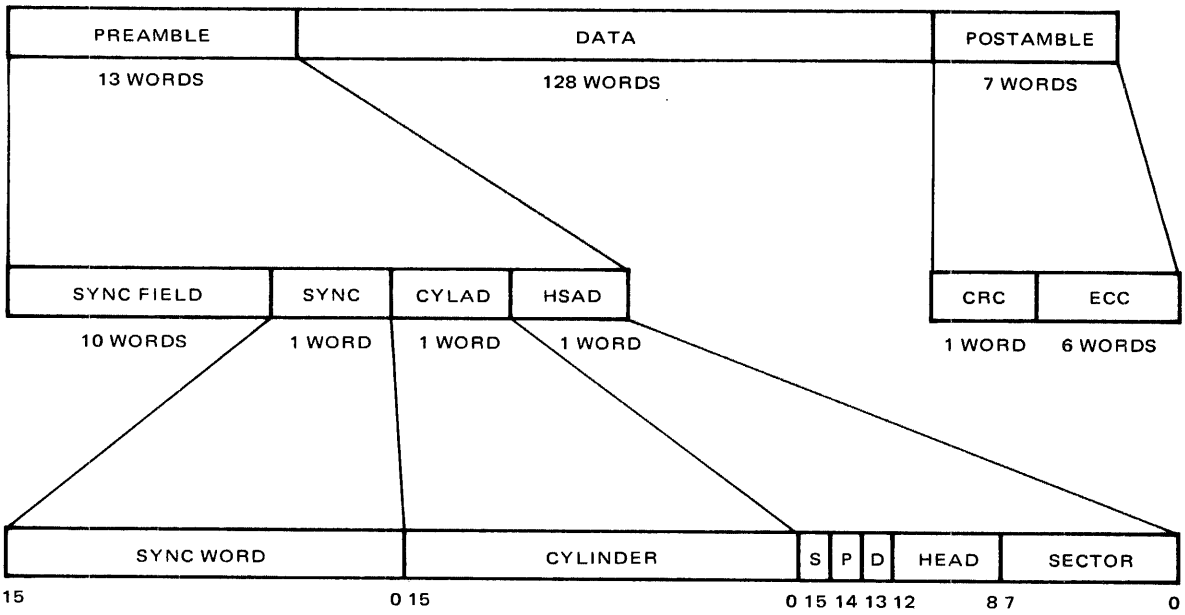


Figure 3-2. Track Recording Format

3-3. SECTOR RECORDING FORMAT

The smallest addressable data storage area in the disc drive is a sector. Accessing a sector is accomplished by specifying the address of the cylinder, head, and sector. (See figure 3-3.)



PREAMBLE – 13 WORDS FOR SYNCHRONIZATION AND ADDRESSING

DATA – 128 WORDS OF DATA

POSTAMBLE – DATA CHECKING AND ERROR CORRECTION INFORMATION

SYNC FIELD – 10 WORDS (160 BITS) OF Ø'S

SYNC – SYNC WORD – 100376_8 IF ECC FIELD IS VALID
100377_8 OTHERWISE

CYLAD – CYLINDER – CYLINDER ADDRESS

HSAD – HEAD ADDRESS (LOGICAL)
SECTOR ADDRESS (LOGICAL)
S – IF "1", SPARE TRACK IN ACTIVE USE
P – IF "1", PROTECTED TRACK
D – IF "1", DEFECTIVE TRACK

CRC – CYCLIC REDUNDANCY CHECK – 1 WORD OF CHECK INFORMATION

ECC – ERROR CORRECTION CODE – 6 WORDS OF CHECK AND CORRECTION INFORMATION

Figure 3-3. Sector Recording Format

Each sector contains a sector address field, a data field, and data checking and error correction fields. The sector address field

contains the cylinder, head, and sector addresses of the sector, as well as indicators for spare, defective, and protected tracks. The data field stores 128 words of data. Each data word is defined as 16-bits. Only the data field is transferred to and from the computer in most data operations. The preamble and postamble are normally generated and checked in the controller. All fields except the sync are error checked by the controller.

3-4. COMMAND WORDS

To initiate an operation, the controller accepts a 16-bit command word from the CPU-Interface, decodes, and executes the operation specified. The command may pertain to the controller only, a selected disc drive only, or both. Some commands require additional information from the interface for proper execution. Each command is discussed separately in the following paragraphs. The command word format relating to a specific command is shown at the beginning of each paragraph. Bits 8 through 12 of the command are used for the opcode, that is, the octal representation that identifies each command. The U referred to in the command format is the disc drive unit number. (The crosshatched bits indicated in some of the command words are not processed by the controller.) Table 3-1 is a listing of command codes and commands. The commands are listed functionally as control, sense, read, and write groups. They are also discussed in the following paragraphs in functional groups. The timeout function referred to in the discussion is approximately 1.8 seconds.

Each disc drive has a "hold" bit associated with it to prevent two different CPU-interfaces from accessing the same disc drive at the same time. Each command to the controller (which references a disc drive) includes a one-bit hold field which is retained by the controller. While a hold bit is set for a particular disc drive, no other CPU-interface may access it with a command that could modify the disc drive status. An attempt to access a held disc drive results in a "unit unavailable" error termination by the controller.

Table 3-1. Command Codes

CODE (OCTAL)	COMMAND AND GROUP			
	CONTROL	SENSE	READ	WRITE
ØØØ			Cold Load Read	
ØØ1	Recalibrate			
ØØ2	Seek			
ØØ3		Request Status		
ØØ4		Request Sector Address		
ØØ5			Read	
ØØ6			Read Full Sector	
ØØ7			Verify	
Ø1Ø				Write
Ø11				Write Full Sector
Ø12	Clear			
Ø13				Initialize
Ø14	Address Record			
Ø15		Request Syndrome		
Ø16			Read with Offset	
Ø17	Set File Mask			

Table 3-1. Command Codes (Continued)

CODE (OCTAL)	COMMAND AND GROUP			
	CONTROL	SENSE	READ	WRITE
Ø22			Read without Verify	
Ø23		Load TIO Register		
Ø24		Request Disc Address		
Ø25	End			
Ø26	Wakeup			

To give the reader a better understanding of the commands, a glossary of terms is listed for mnemonics used in the command descriptions. Since the terms listed are hardware implemented, they are discussed in section IV.

Controller-CPU Interface

CLEAR — Hard clear on controller logic
IBUS Ø-15 -- Data Bus
ENID -- Enable Interface Drivers
ENIR -- Enable Interface Receivers
IFNØ-3 -- Function Bus
IFCLK — Interface Clock (Validates Data Bus)
IFVLD -- Interface Function Valid

Flags from Interface

CMRDY — Command Ready
DTRDY -- Data Ready
EOD -- End of Data
INTOK — Interrupt O.K.
OVRUN -- Overrun
XFRNG — Transfer No Good

Function Bus Commands

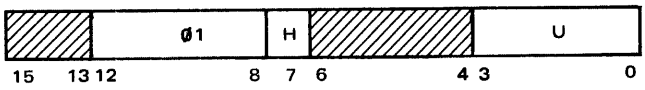
BUSY -- Set or Clear Interface Busy Bit
DSCIF -- Disconnect Interface
DVEND -- Device End

IFIN -- Data In, Controller to Interface
IFGTC -- Get Command from Interface
IFOUT -- Data Out, Interface to Controller
IFPRF -- Pre-fetch Command from Interface
RQSRV -- Request Service
SELIF -- Select Interface
SRTRY -- Set Retry Counter
STDFL -- Set Data Flag
STINT -- Set Interrupt
WRTIO -- Write Interface Status Register

3-5. CONTROL COMMANDS

Control commands start operations not involving a transfer of data sectors between the controller and computer. For most functions,the entire operation to be started is specified by the control command.

3-6. RECALIBRATE.

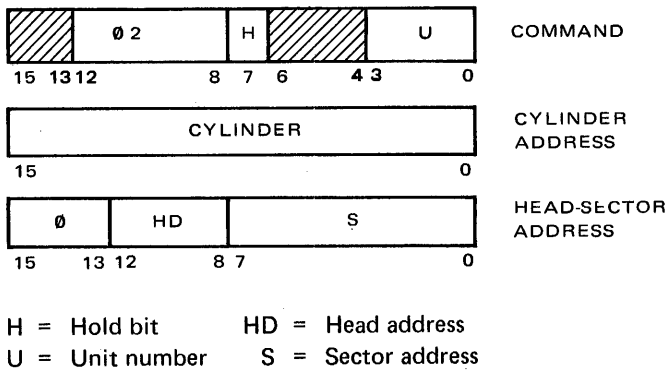


H = Hold bit
U = Unit number

To perform this command, only the command word is necessary. The word contains only the opcode, the hold bit, and unit number. If the addressed unit is available and ready, the controller issues a RECALIBRATE command and returns to the poll loop. (Refer to paragraph 4-5.) The disc drive positions its heads over cylinder Ø and clears its "current cylinder address" register. Disc drive attention bit is set when the drive completes the recalibrate function. If Interrupt O.K. (INTOK) is true, the controller transmits Set Interrupt (STINT) to the interface and clears the drive's attention request. The computer must wait for completion before issuing the next command.

If the unit is not available or not ready, the controller sends Set Interrupt (STINT) to the interface and waits for a command to be issued from the interface or a timeout to occur.

3-7. SEEK.

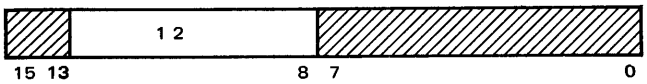


This command causes positioner motion and is initiated by issuing the command word followed by two additional words in the order shown. The first contains the cylinder address and the second contains the head and sector address. The controller requests each of these words by transmitting STDFL to the interface. The controller then transmits them to the disc drive and begins polling. When an attention interrupt is received from the drive and Interrupt O.K. (INTOK) is true, the controller interrupts the interface and clears the attention request. The head and sector address are retained in the controller for future data operations, but will be overwritten by a subsequent ADDRESS RECORD or SEEK command. Since the controller polls other interfaces before reporting a seek completion, the programmer should issue an ADDRESS RECORD command immediately preceding a disc drive operation if other interfaces are active in this disc subsystem.

If the unit is not ready, the controller sends Set Interrupt (STINT) to the interface after accepting the address words. The controller then waits for a new command to be issued from the interface or a timeout to occur.

If the unit is unavailable, the controller sends STINT to the interface after the command is received. The interface busy bit will be false. The address words should not be sent because the controller will not process them. After transmitting STINT, the controller waits for a new command or timeout to occur.

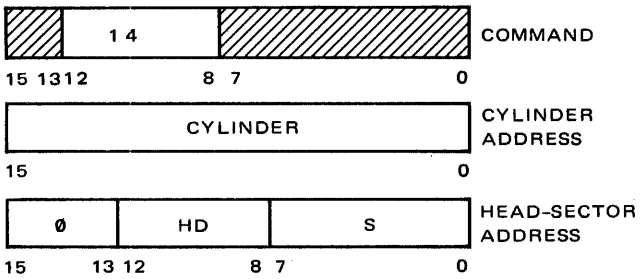
3-8. CLEAR.



Upon receipt, the controller will issue a CLEAR to all drives, clear status, clear any clock or head offset, turn off the timer, clear the interface busy bit, disconnect all disc drives, transmit Set Data Flag (STDFL) to the interface, and resume polling. A unit number is not required. CLEAR is executed because of an explicit command,

controller power on, or hard CLEAR from an interface.

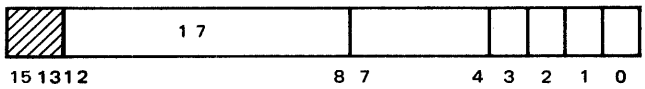
3-9. ADDRESS RECORD.



HD = Head address S = Sector address

This command is used to set a logical address in the controller without transmitting it to the disc drive. The issuance of the command word is followed by two words in the order shown. The first contains the cylinder address and the second contains the head and sector address. The controller requests each of these words by transmitting STDFL to the interface. Upon receipt, the controller transmits Request Service (RQSRV) to the interface and waits until either a command is received or a timeout occurs. Polling is suspended on completion of this command. If used in a multiple computer environment, an ADDRESS RECORD should follow each SEEK or RECALIBRATE command, or should precede a data transfer operation if the SEEK or RECALIBRATE is not used.

3-10. SET FILE MASK.



Bit Ø — Allows automatic seek as per bit 3.

Bit 1 — If set (cylinder mode), a logical cylinder consists of all available surfaces; end-of-cylinder occurs when last sector on last surface has been transferred. If not set (surface mode), end-of-logical-cylinder occurs when last sector of any surface has been transferred.

Bit 2 — Allows automatic seek to spare track.

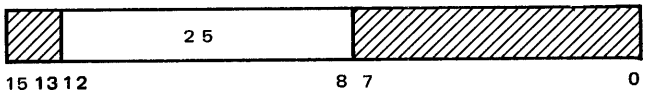
Bit 3 — If set, decremental seek at end of logical cylinder. If not set, incremental seek at end of logical cylinder. If bit Ø = Ø, this bit is ignored.

Bits 4-7 — Number of retries allowed.

The mask sets the mode of operation for the controller. The controller transfers bits Ø-3 into its "mask" register which is used to control the action taken while transferring data. The entire word is

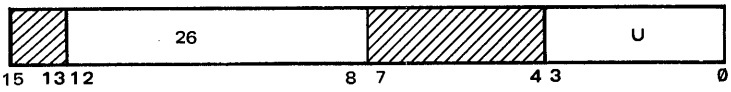
transmitted to the interface via a Set Retry Counter (SRTRY) order. For computers with a data channel separate from the CPU, the retry counter allows the channel program to retry a data transfer in case of an error. The programmer sets the counter with bits 7 thru 4 of this command. After the specified number of retries, the interface interrupts the CPU. After sending SRTRY,the controller transmits Set Data Flag (STDFL) to the interface. Polling is suspended on completion. The controller takes no further action until a command is received or a timeout occurs. At power up, the mask is set to no-automatic-seek, surface mode, and no sparing.

3-11. END.



This command is used to avoid a timeout if no other command is expected to be outputed from an interface and the controller is waiting for a command from that interface. When the controller accepts this command from an interface, no action is taken except to resume polling. This command should follow any string of commands when they have been completed.

3-12. WAKEUP.



U = Unit number

This command checks if the specified unit is available (hold bit clear). If not, the command is left pending on the interface and the controller resumes polling of other interfaces.

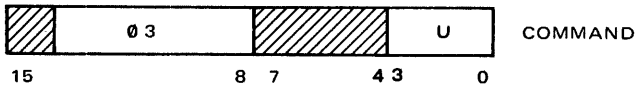
If the unit is available, the status register is set to indicate "unit available" and STDFL is transmitted to the interface. The controller then waits until a command is received or until timeout occurs.

This command should not be issued unless the controller has previously returned a "unit unavailable" status since only the hold bit is checked, not the interface to which the drive is assigned. If the Wakeup command is issued while the drive is being held by the same interface, the interface will lock up while waiting for itself.

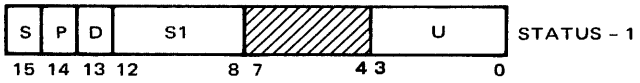
3-13. SENSE COMMANDS.

The sense commands determine the status of the disc drive and controller and identify the specific nature of any errors or unusual conditions that have occurred.

3-14. REQUEST STATUS.



U = Unit number



U — Unit number to which status on last operation applies; if S1 is 37 (drive attention), U is number of interrupting drive. If no unit number is appropriate, U will be zero.

S1 — Encoded termination status (octal).

The various encoded termination status values in the S1 field are explained below.

ØØ — NORMAL COMPLETION. This status is transmitted in one of two situations:

a. When command has been fully executed without error.

b. At completion of a REQUEST STATUS command whenever the command immediately follows another REQUEST STATUS command or when it is the first command issued after interface is connected to controller during a polling sequence.

Ø1 — ILLEGAL OPCODE. A command word has been received by the controller of which bits 12-8 contain a command code which is not one of controller's command set.

Ø2 — UNIT AVAILABLE. Controller transmits this status after interface has put out a WAKEUP command for a specific drive and after hold bit for that drive has been cleared.

Ø7 — CYLINDER COMPARE ERROR. During verification of address of sector previous to first sector to be read from or written to, the contents of cylinder address field of that sector do not match contents of controller's cylinder address register. This status is transmitted only after the sequence of events listed below. When this status is received, the system should issue a Recalibrate command and then retry data transfer sequence

a. Addresses do not compare as described above.

b. Controller generates a seek to address in its cylinder address register and head sector address register.

c. Controller again attempts to verify a sector.

d. Addresses still do not compare.

e. The S bit is not set at new track address.

1Ø — UNCORRECTABLE DATA ERROR. This status is generated by the error correction circuits and is transmitted in one of three cases:

a. Immediately following a data transfer (or VERIFY) command if error is uncorrectable.

b. In response to a REQUEST SYNDROME command whenever a Possibly Correctable Data Error has proved uncorrectable.

c. During verification of address of sector previous to first sector to be read from or written to, controller is unable to read (verify) any of 16 consecutive sectors without error.

11 – HEAD SECTOR COMPARE ERROR. Similar to Cylinder Compare Error, including controller's recovery attempt sequence described for that status, except that head and/or sector address field of disc sector does not compare with corresponding field in controller's head sector address register. The system need not issue a RECALIBRATE command when this status is received.

12 – I/O PROGRAM ERROR. Systems containing a programmable data channel separate from CPU may have their interface detect abnormal channel operations and notify controller. At that time, controller will interrupt CPU with this status. An example of such an error might be an inconsistent direction of data transfer (a Read command has been transmitted to controller, but channel has been programmed to write).

14 – END OF CYLINDER. A multiple-sector data transfer must continue beyond end-of-logical-cylinder, but file mask will not allow controller to automatically seek to next logical cylinder and continue.

16 – OVERRUN. Detected by interface (read) or controller (write) whenever instantaneous data rate of controller exceeds that of CPU-interface combination. The overrun is reported at end of sector in which it occurred. The contents of that sector, either on disc (write) or in I/O buffer (read) should be considered invalid.

Note: The controller always transfers complete sectors. If CPU or data channel wishes to transfer less than a complete sector, it must notify interface (or controller) when transfer is complete so that subsequent controller requests for data transfer do not cause an Overrun error.

17 – POSSIBLY CORRECTABLE DATA ERROR. This status is generated by the error correction circuits and is transmitted in one of two cases:

a. Immediately following a data transfer (or VERIFY) command if error is possibly correctable.

b. In response to a REQUEST SYNDROME command if error is in fact correctable. In this case, proceed as described in REQUEST SYNDROME command.

20 – ILLEGAL ACCESS TO SPARE TRACK. The same conditions and sequence of events described for a Cylinder Compare Error or Head Sector Compare Error have occurred, except that S bit is set at new track address. This error usually results from trying to directly access (via a SEEK command) a spare track in active use. The addresses will not compare because of the way in which spare tracks are set up and this status merely differentiates between this situation and other address errors.

21 – DEFECTIVE TRACK. During verification of track status of sector previous to first sector to be read from or written to, the D bit is found to be set but File Mask will not allow automatic seeking to a spare track.

22 – ACCESS NOT READY DURING DATA OPERATION. While in process of transferring data to or from disc, the track center detector in drive detected head motion. The transfer should be retried.

23 – STATUS-2 ERROR. The controller is unable to complete a command due to some condition in disc drive. The Status-2 word may be examined for reason. Examples of Status-2 Errors are:

a. An Initialize command, but Format switch is off or Protected switch is on.

b. A command is issued to a drive which is Not Ready (heads unloaded) or for which a Drive Fault has occurred.

26 – ATTEMPT TO WRITE ON PROTECTED TRACK. During verification of track status of sector previous to first sector to be written to using a Write command, the P bit is found to be set.

27 – UNIT UNAVAILABLE. This status is returned in two cases:

a. An interface has requested a drive whose hold bit has been set by another interface.

b. The U field of the command word is greater than 12 (octal).

Note: The interface busy bit is false whenever this status is returned. This status is not set for REQUEST SECTOR ADDRESS command whether drive is held by another interface or not. This is because the command only accesses the "current sector" counter in disc drive without changing any operating parameter of drive or controller.

37 – DRIVE ATTENTION. Controller generates an interrupt (issues STINT) to interface which last accessed drive which is requesting attention (or interface Ø if this is first attention after power-on or hand clear) whenever:

a. Drive is requesting attention.

b. Interface does not have a subsequent command pending in its command buffer excepting Wakeup, which is ignored here.

c. Interface flag INTOK (Interrupt O.K.) is set, thereby allowing attention interrupts.

Briefly, conditions causing a drive to request attention are:

a. Seek completion.

b. Drive becomes ready (heads load).

c. Drive becomes not ready (heads unload).

d. Seek check.

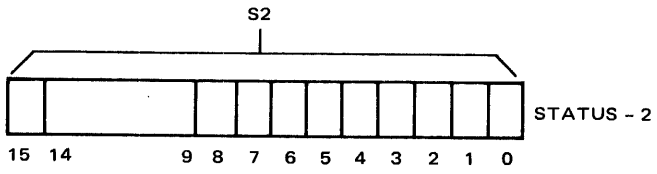
e. Drive Fault.

Refer to Disc Drive Operating Manual, part no. 07905-90009, for a more complete description of these conditions.

S – Spare track

P – Protected track

D – Defective track



S2 – Unit status

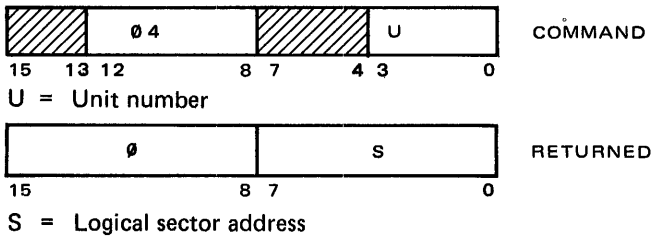
Bit

Ø* – Drive busy
1* – Drive not ready (heads not loaded)
2* – Seek check
3 – First status
4* – Fault
5 – Format
6 – Protected
7 – Attention
8 – Ø
9-14 – Address of last available surface (head)
15 – Status-2 error (true if any bit marked * is true)

After receipt of the command, the controller returns two status words to the interface. The first (Status-1) contains information relating to the last operation performed, and the second (Status-2) contains information pertaining to the disc drive addressed in the command word. Any hold bit is ignored, and the First Status bit in Status-2 is cleared by this command. The controller then clears STATUS-1 and waits for a command from the same interface or a timeout to occur.

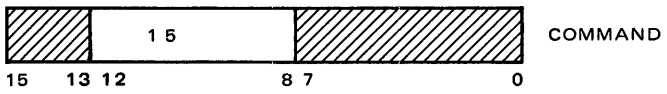
Note: The Status-1 word is also transmitted to the interface at the completion of all commands or at an error interrupt. The WRTIO function bus command is used.

3-15. REQUEST SECTOR ADDRESS.



After receipt of the command, the controller returns the logical address of the sector currently passing under the heads of the specified unit. The existing hold bit is not checked or altered. Polling is suspended on completion.

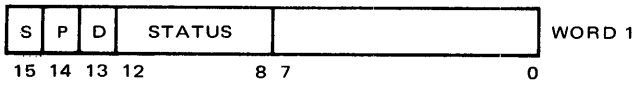
3-16. REQUEST SYNDROME.



This command is used when errors have been detected by the controller after transferring data from the disc drive to the computer. The command may be issued after a READ, COLD LOAD READ, READ WITH OFFSET, or READ WITHOUT VERIFY command which terminates with a Status-1 word indicating "Possibly Correctable". The software correction routine should not try to correct the preamble or postamble since these areas have not been transmitted to the data buffer in the computer. See figure 3-3 for the sector recording format and related nomenclature pertaining to this discussion.

This command should only be issued if the Status-1 field immediately following a data transfer (or VERIFY command) contains Possibly Correctable Error status. False results will be obtained if this command is issued at any other time (including after a previous REQUEST SYNDROME command).

Seven words are returned, with the following significance:

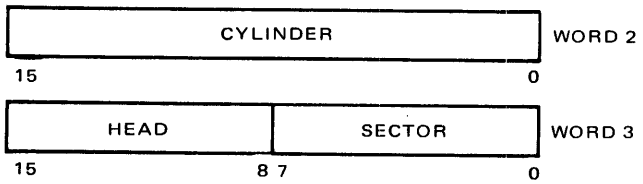


S — Spare track

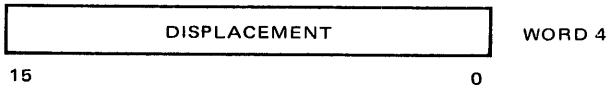
P — Protected track

D — Defective track

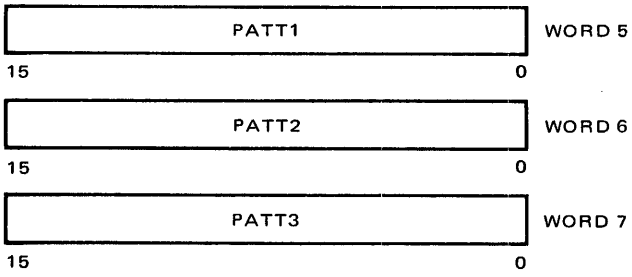
Status — May be "Correctable" or "Uncorrectable" (Ø17 or Ø1Ø octal) at this point. If uncorrectable, ignore displacement and pattern words. If correctable (Ø17), correction data is available in displacement and pattern words.



Cylinder, Head, Sector — The logical address of sector in which error occurred.



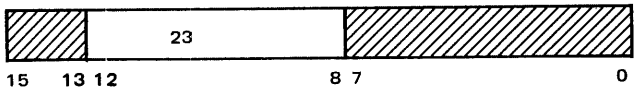
Displacement — Indicates beginning word within sector where first bit error occurred. The indication is given relative to first data word. The first data word is numbered zero. Thus, to obtain address of first word to be corrected, displacement is added to buffer base address of sector (first data word). If displacement number is negative or greater than 125, all or part of error occurred in preamble or postamble. The computer should not try to correct errors in these areas, since their contents were not transferred into computer's memory. If full sector was not transferred, computer must check to ensure that displacement is within buffer.



Three words, PATT1, PATT2, and PATT3, are generated by the controller for error correction. These words are "exclusive- or'ed" with the data word errors, beginning with the word indicated by the displacement number. The word patterns are "exclusive-or'ed" with any contiguous 32-bit frame within the data word portion of the sector. Performance of the "exclusive-or" function of the computer corrects the errors.

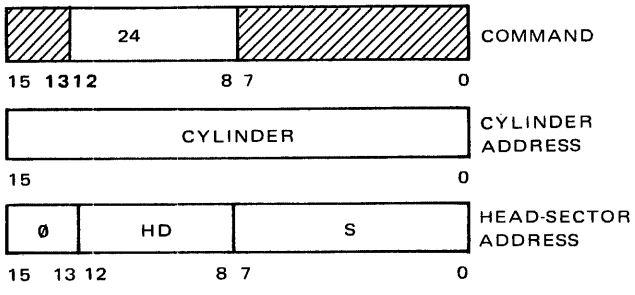
The command will complete in <28 milliseconds. When the process is complete, the controller addresses the next logical sector and waits for a command or until timeout occurs. If the transfer was not complete, the interface may issue a READ without an intervening SEEK or ADDRESS RECORD to continue the transfer. Polling is not resumed when REQUEST SYNDROME is completed.

3-17. LOAD TIO REGISTER.



The controller accepts a word of data which is written into the TIO (status) register on the interface by a Write Interface Status Register (WRTIO) order. The controller then transmits Request Service (RQSRV) to the interface and suspends polling. This command is intended as a diagnostic tool for those interfaces which have a TIO register.

3-18. REQUEST DISC ADDRESS.



HD = Head address
S = Sector address

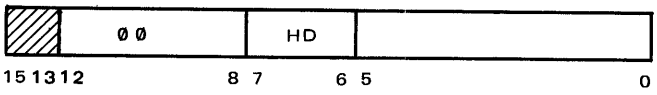
The controller returns two words in the order and format of the address words passed in a SEEK command. The command may be used following a multiple-sector I/O or VERIFY command which aborted with an error. This command allows the operating system to determine where the abort occurred. After completion, the controller then transmits Request Service (RQSRV) to the interface and waits for a command or

until timeout occurs.

3-19. READ COMMANDS.

Read commands transfer information from a disc drive to the computer. All operate in single-track mode. On all read commands, the controller examines correction and cyclic code words to check the validity of each record area.

3-20. COLD LOAD READ.



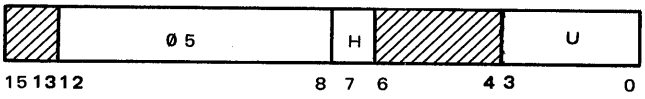
HD = Head address
S = Sector address

After issuing a SEEK to unit 0, cylinder 0 and the head and sector specified in the command word, and waiting for seek completion, the controller sets the FILE MASK to Sparing Enabled, Incremental Seek Not Allowed, and Surface Mode. The controller also transmits a 0 retry count to the interface and then begins reading, starting with the sector and head addressed in the command word.

The controller continues to transfer 128 words per sector until the interface sets End of Data (EOD) or the end-of-logical-cylinder is reached. The last sector does not have to be completely transferred. At the end of each sector, checks are made for overrun (detected by the interface) and data errors. If any errors are detected, the operation will be aborted regardless of End of Data (EOD). Sparing will occur if it is necessary.

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun or data error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

3-21. READ.



H = Hold bit
U = Unit number

The controller first checks that the specified unit is available. If not, the controller sends Set Interrupt (STINT) to the interface. The

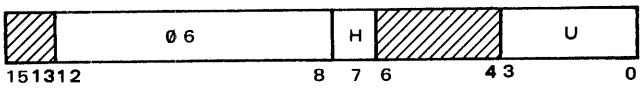
controller then waits for a new command or a timeout to occur. The following description assumes that the unit is available.

After sparing (if necessary and enabled) and waiting for seek completion, the controller begins reading from (1) the sector last addressed by a SEEK command; (2) the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the last one transferred, whichever occurred most recently.

The controller continues to transfer 128 words per sector until the interface sets End of Data (EOD). The last sector does not have to be completely transferred. At the end of each sector, checks are made for overrun (detected by the interface) and data errors. If any errors are detected, the operation will be aborted regardless of End of Data (EOD). Sparing will occur at the end of any track if necessary and enabled.

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun or data error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

3-22. READ FULL SECTOR.



H = Hold bit
U = Unit number

The controller first checks that the specified unit is available. If not, the controller sends Set Interrupt (STINT) to the interface. The controller then waits for a new command or a timeout to occur. The following description assumes that the unit is available.

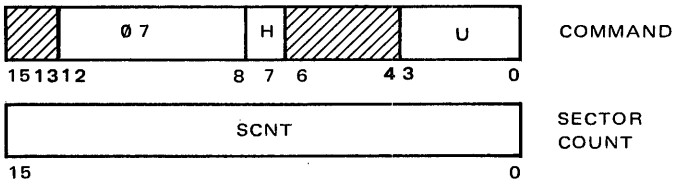
After waiting for seek completion (without sparing), the controller begins reading from (1) the cylinder, head and sector last addressed by a SEEK command, (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command or (2) the sector following the last sector transferred, whichever occurred most recently.

The controller then transfers 138 words per sector (sync word, cylinder address, head-sector address, 128 data words, CRC word, and 6 ECC words) to the computer until the interface sets End of Data (EOD). The last sector does not have to be completely transferred. At the end of each sector, a check is made for overrun (detected by the interface). If an error is detected, the operation will be aborted

regardless of End of Data (EOD).

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun or data error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

3-23. VERIFY.



H = Hold bit
U = Unit number
SCNT = Sector count

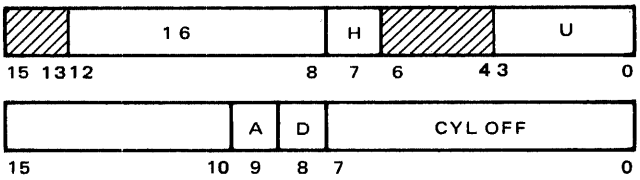
The command word and one word specifying sector count are passed to the controller. Starting with the currently addressed sector, the controller reads from the disc without passing data to the computer. At the end of each sector, a check is made for data errors. If any errors are detected, the operation will be aborted regardless of sector count word (SCNT). The controller continues to scan sectors until SCNT has decremented to zero. The SCNT designates how many sectors are to be verified. If SCNT is zero, the interpretation is 65,536 (decimal) words.

The controller first checks that the specified unit is available. If not, the controller sends Set Interrupt (STINT) to the interface. The controller then waits for a new command or a timeout to occur. The following description assumes that the unit is available.

After sparing (if necessary and enabled) and waiting for seek completion, the controller begins reading (without transmitting to the interface) from (1) the sector last addressed by a SEEK command; (2) the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the sector last transferred, whichever occurred most recently. Sparing will occur at the end of any track if necessary and enabled.

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On data error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

3-24. READ WITH OFFSET.



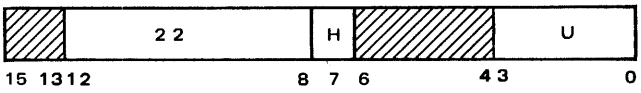
H = Hold bit
U = Unit number
CYL OFF = Cylinder offset parameter
A = Advance clock
D = Delay clock

This command performs like a normal read except that the heads are moved off of track center by an amount proportional to an offset parameter word requested from the computer before data transfer begins. After fetching the parameter, the controller transmits RQSRV and STDFL to the interface. Direct memory access (DMA) should not be activated for the data transfer portion of the command until one or both of these signals are received on the interface.

The controller transmits the cylinder offset to the selected disc drive, and may also advance or delay the separator clock 10 nanoseconds with respect to the data. A cylinder offset of zero is on the track center. Offset parameters in the range of +63 to -63 move the heads off of track center by 25 microinches per increment. (A negative parameter is in two's complement form.) All offsets are removed after normal command completion or error terminations.

This command is usually used only in error recovery situations when normal re-reads and REQUEST SYNDROME commands have failed. Since each offset operation requires a minimum of 1.5 milliseconds to complete, the target sector will have passed under the heads by the time the offset is complete, thus requiring an extra rotation of the disc. A similar amount of time is required at the end of the command to restore the heads to track center.

3-25. READ WITHOUT VERIFY.



H = Hold bit
U = Unit number

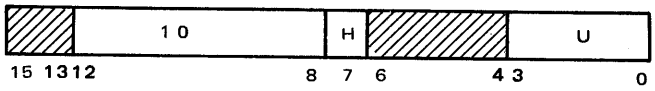
This command performs like a normal read, but does not verify the preceding sector. Therefore, no address checking or sparing operations occur unless a track boundary is crossed during the operation. This command is provided for "wraparound read" operation or error recovery.

3-26. WRITE COMMANDS.

Write commands transfer information from the system main storage to the controller for recording on a disc. While writing a record on a disc track, the controller appends the preamble and appropriate correction code words to each record area.

Note: The computer must supply all words except the 10-word sync field during a WRITE FULL SECTOR command.

3-27. WRITE.



H = Hold bit
U = Unit number

The controller accepts data from the computer and writes the addressed sector (preamble, data, and postamble) after verifying the previous sector. The command will not be executed if the surface is protected or the P-bit is set.

The controller first checks that the specified unit is available. If not, the controller sends Set Interrupt (STINT) to the interface. The controller then waits for a new command or a timeout to occur. The following description assumes that the unit is available.

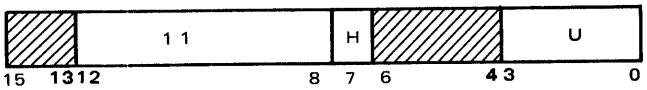
After sparing (if necessary and enabled) and waiting for seek completion, the controller begins writing on (1) the sector last addressed by a SEEK command; (2) the sector last addressed by an ADDRESS RECORD command; or (3) the sector following the last sector transferred, whichever occurred most recently.

On all data transfers out of the computer, the controller will request 128 words of data. If the computer transfers less, the controller will repeatedly write the last transmitted word into the remainder of the sector data field. If the controller fills the sector in this manner and then finds that the computer has more data available, it will flag an overrun error and terminate the operation. (Overrun is detected by the controller.) Normally, the controller continues to transfer 128 data words per sector until the interface sets End of Data (EOD). At the end of each sector, a check is made for overrun. If an error is detected, the operation will be aborted regardless of End of Data (EOD). Sparing will occur at the end of any track if necessary and enabled.

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

The operation will be aborted whenever a track is encountered which has been flagged protected or defective, or if the surface is protected by the disc drive PROTECT switches.

3-28. WRITE FULL SECTOR.



H = Hold bit
U = Unit number

This command is like a write except that the computer must pass the sync word, address words, and postamble to the controller in addition to the data field.

The controller first checks that the specified unit is available. If not, the controller sends Set Interrupt (STINT) to the interface. The controller then waits for a new command or a timeout to occur. The following description assumes that the unit is available.

After waiting for seek completion (without sparing), the controller begins reading from (1) the cylinder, head and sector last addressed by a SEEK command, (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command or (2) the sector following the last sector transferred, whichever occurred most recently.

The controller will request 138 words per sector (sync word, cylinder address, head-sector address, 128 data words, CRC word, and 6 ECC words). If the computer transfers less, the controller will repeatedly write the last transmitted word into the remainder of the sector data field. If the controller fills the sector in this manner and then finds that the computer has more data available, it will flag an overrun error and terminate the operation. (Overrun is detected by the controller.) Normally, the controller continues to transfer 138 words per sector until the interface sets End of Data (EOD). At the end of each sector, a check is made for overrun. If an error is detected, the operation will be aborted regardless of End of Data (EOD).

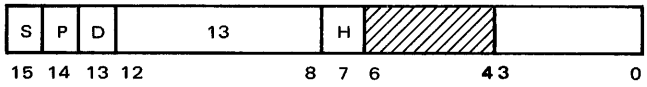
On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

The operation will be aborted if the FORMAT switch on the disc drive is set to off, or if the surface is protected by the disc drive PROTECT switches.

This command is intended only as a diagnostic tool. In any case, it is strongly recommended that any multiple sector transfers not cross a

track boundary since all address verification and track status checks are off.

3-29. INITIALIZE.



S = Flag track spare
P = Flag track protected
D = Flag track defective
H = Hold bit
U = Unit number

On receipt of the command word, the controller checks that the surface is not protected and that the FORMAT switch on the drive is set to on before executing the command. The controller then begins requesting data from the computer and writes 128 data words on the addressed sector without verifying the preceding sector. Data transfer continues until the interface sets End of Data (EOD).

The controller first checks that the specified unit is available. If not, the controller sends Set Interrupt (STINT) to the interface. The controller then waits for a new command or a timeout to occur. The following description assumes that the unit is available.

After waiting for seek completion (without sparing), the controller begins reading from (1) the cylinder, head and sector last addressed by a SEEK command, (2) the cylinder and head last addressed by a SEEK command and the sector last addressed by an ADDRESS RECORD command or (2) the sector following the last sector transferred, whichever occurred most recently.

On all data transfers out of the computer, the controller will request 128 words of data. If the computer transfers less, the controller will repeatedly write the last transmitted word into the remainder of the sector data field. If the controller fills the sector in this manner and then finds that the computer has more data available, it will flag an overrun error and terminate the operation. (Overrun is detected by the controller.) Normally, the controller continues to transfer 128 data words per sector until the interface sets End of Data (EOD). At the end of each sector, a check is made for overrun. If an error is detected, the operation will be aborted regardless of End of Data (EOD).

On normal completion, Set Data Flag (STDFL) and Request Service (RQSRV) are sent to the interface. On an overrun error, Device End (DVEND) and Request Service (RQSRV) are transmitted. Any other error causes the controller to transmit STINT to the interface. The controller then waits for a command from the same interface or a timeout to occur.

Bits 13, 14, and 15 of the command word are used to flag the track defective, protected, or spare. Subsequently, when a drive operation is attempted on a track so marked, the status of the track last accessed by that operation will appear in bits 13-15 of STATUS-1 word. It is the responsibility of the system to ensure that all sectors on a track have the same status.

If the D-bit is set, the track is considered defective and sparing will occur if required and enabled. The only drive operations allowed on a track so marked are READ FULL SECTOR, READ WITHOUT VERIFY, INITIALIZE, and WRITE FULL SECTOR. The latter two will not preserve track status unless specifically directed to do so.

If the P-bit is set, a write operation will not be allowed on that track. INITIALIZE or WRITE FULL SECTOR will be allowed, but will not preserve track status unless specifically directed to do so.

If the S-bit is set on a track, a spare track is in active use. Data operations including VERIFY but excepting INITIALIZE, WRITE FULL SECTOR, READ FULL SECTOR, and READ WITHOUT VERIFY will not be allowed on a track so marked unless access is made through its corresponding defective track. INITIALIZE and WRITE FULL SECTOR will not preserve track status unless directed to do so.

It is strongly recommended that any multiple sector transfers using the INITIALIZE command not cross a track boundary, since all address verification and status checks are off. In addition, a track boundary must not be crossed during a multiple sector transfer whenever tracks are being flagged spare or defective since the automatic track sparing algorithm may not work on these tracks.

Section IV

THEORY OF OPERATION

4-1. INTRODUCTION

This section discusses the functional operation of the controller first from an overall concept. Each block is then segmented and described separately. Included are the microprocessor, device controller, error correction, interfaces between the controller and CPU-disc drive, and power supply. For maintenance reasons, the microcode instruction format and associated descriptions are described in section V.

4-2. OVERVIEW OF DISC CONTROLLER

The controller can access from one to eight disc drives. (See figure 4-1.) Each disc drive contains one disc which is fixed and one disc which is removable from the front of the drive. Each disc surface contains five Megabytes storage. Data is transferred to and from the disc at 7.5 Megabits/second, or about 936 Kilobytes/ second. Either one or two CPU-interfaces are connected to the controller. The CPU-interface PCA transfers commands from the CPU to the controller. The interface could include data buffering, provisions for different programming methods of sending commands to the controller, logic level differences between the controller and a CPU, and handshake signals and sequences needed by an I/O section of a CPU.

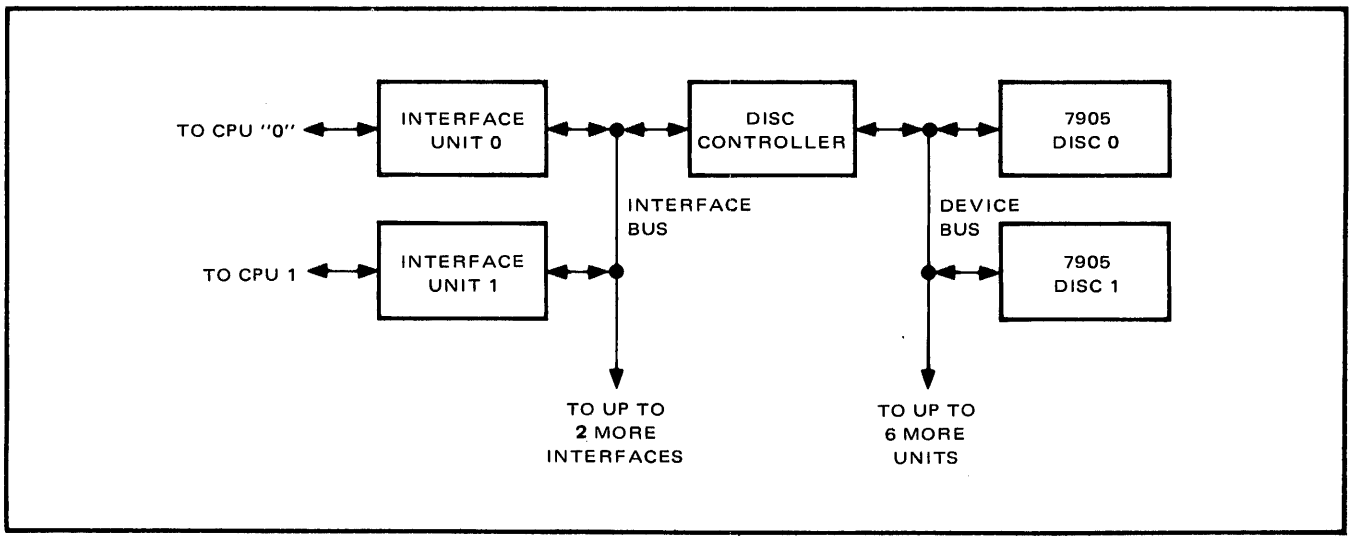


Figure 4-1. Disc Drive Subsystem Block Diagram

The controller is organized into four major hardware areas. (See figure 4-2.) They are microprocessor, device controller, error correction code, and interface circuitry (not indicated on the block

diagram). Operation of the controller is directly controlled by a microprogram stored in the microprocessor read-only-memory (ROM). The microprogram generates control signals for the controller during command execution. The control signals generated by the microprogram cause the device controller to send orders to disc drives, enabling data to be stored or retrieved. Disc drive status is monitored by the microprogram and sent to the interface upon command. Data integrity is constantly checked by the controller through the use of cyclic redundancy checking and error correction codes which are processed by the error correction circuitry. The interfaces are contained on the device controller PCA and consist of busses, buffers, drivers, and receivers for communication between the controller-disc drive and controller-CPU interface.

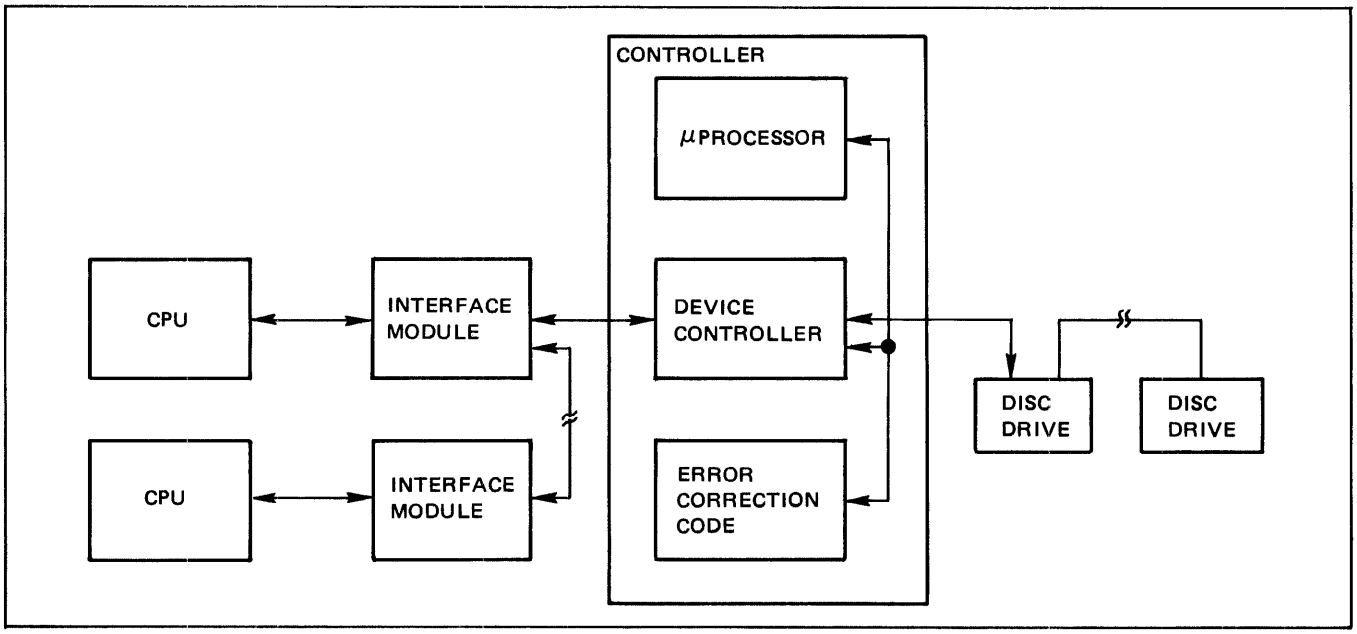


Figure 4-2. Controller Overall Functional Block Diagram

4-3. FUNCTIONAL DESCRIPTION

The execution of commands requiring data transfer requires the controller to perform numerous internal operations. When data supplied by the computer is to be written by the disc drive, the control of the write operation includes transferring disc drive addresses, transferring head-sector and cylinder addresses, checking

that the disc drive went to the correct address, ensuring proper sector format (which includes an address field and a data field), performing parallel-to-serial conversion of data words, generating check and error correction words, and continuously monitoring the write operation until completed. When data is to be transferred to the computer, the control of the read operation includes transferring head-sector and cylinder addresses, transferring disc drive addresses, checking that the disc drive went to the correct address, performing serial-to-parallel conversion of data words, checking for data errors, and continuously monitoring the read operation until completed.

4-4. GENERAL CONTROLLER DESCRIPTION

The microprocessor controls the overall controller operation by implementing instructions from the microprogram read from read-only-memory (ROM). As shown in figure 4-3, the microprocessor consists of the following functional blocks:

a. The internal clock logic and crystal (not shown) that controls the overall controller timing.

b. The 12-bit ROM address register (RAR) logic used to implement instructions read from ROM.

c. The ROM output register (ROR) logic which holds and distributes 24-bit microcode instruction words received from ROM.

d. Decoding logic (not shown) to decode instructions of the microprogram.

e. Flag logic (not shown) to control branching within the microprogram.

f. Eight 16-bit general purpose register logic (AØ-A3 and BØ-B3) under control of the microprogram instructions.

g. The arithmetic logic unit (ALU) which performs arithmetic and logic functions as directed by the microprogram to control operation of the controller.

h. Rotate-shift logic (shifter) which follows the ALU.

i. The microcode subroutine stack (three-level) which provides storage for return addresses so that the main microprogram can resume at the correct place after a subroutine is complete.

All data and command communication conducted between the microprocessor, error correction code, and device controller is routed via the MIO-bus. Input data is loaded into the selected registers. As directed by the microprogram, the data is processed via the A-and B-buses to the Arithmetic Logic unit, and back to the MIO-bus. The A-bus is driven by the Immediate Operand field of the microcode instruction and registers AØ thru A3. The B-bus is driven by BØ thru B3 registers. The MIO-bus is used for input/output and as the return path to the registers. The microprocessor microcode instruction set contains arithmetic and logical instructions and conditional branching microinstructions that control the ALU and rotate/shift logic. Seventeen external flag lines and six processor status indicators that permit selective branching on condition are also provided. The A-and B-registers are divided into upper and lower bytes. Therefore, the option of selecting the upper byte, lower byte, or a full 16-bit word is provided. Five destination/source bits are provided to select the source or destination desired when executing an input/output instruction.

MICRO PROCESSOR

ERROR CORRECTION CODE

17

CONDITION SELECT

I/O STROBES

3

COMMAND DECODING

CCB

BRANCH SELECT

24

5

8

IMMEDIATE OPERAND

A0 A1 A2 A3

B0 B1 B2 B3

16

A BUS

16

16

B BUS

ROR

ALU

12

6

ROM

PSR

3

3

T-REG

X ADDR DECODE

12

ROM ADDR REG

ADDR GATING

12

SHIFTER

TO CLOCKS AND OUTPUT ENABLES OF DEVICE CONTROLLER REGISTERS

SUBROUTINE STACK

12

12

EXTERNAL

16

A

OUT

B

A

OUT

B

READ DATA

DATA CLOCK

INHIBIT CLOCK ENABLE & SHIFT/LOAD

DEVICE CONTROLLER

MIO BUS

17 FLAGS

CPU DATA REG

DRIVERS

DRIVE CTRL REG

TO CPU INTERFACE

RAM ADDR REG

RAM

TO DISC DRIVE

SERDES

DATA FORMATTER/ SEPARATOR

DATA TO/FROM DISC DRIVE

CPU TAG REG

11 FLAGS

DRIVE TAG REG

DATA CLOCK TO ALL SERDES DATA HANDLING CIRCUITS

6

CRCC

MIOO BUS

SECTOR COMPARE

7103-7

6 FLAGS FROM INTERFACE

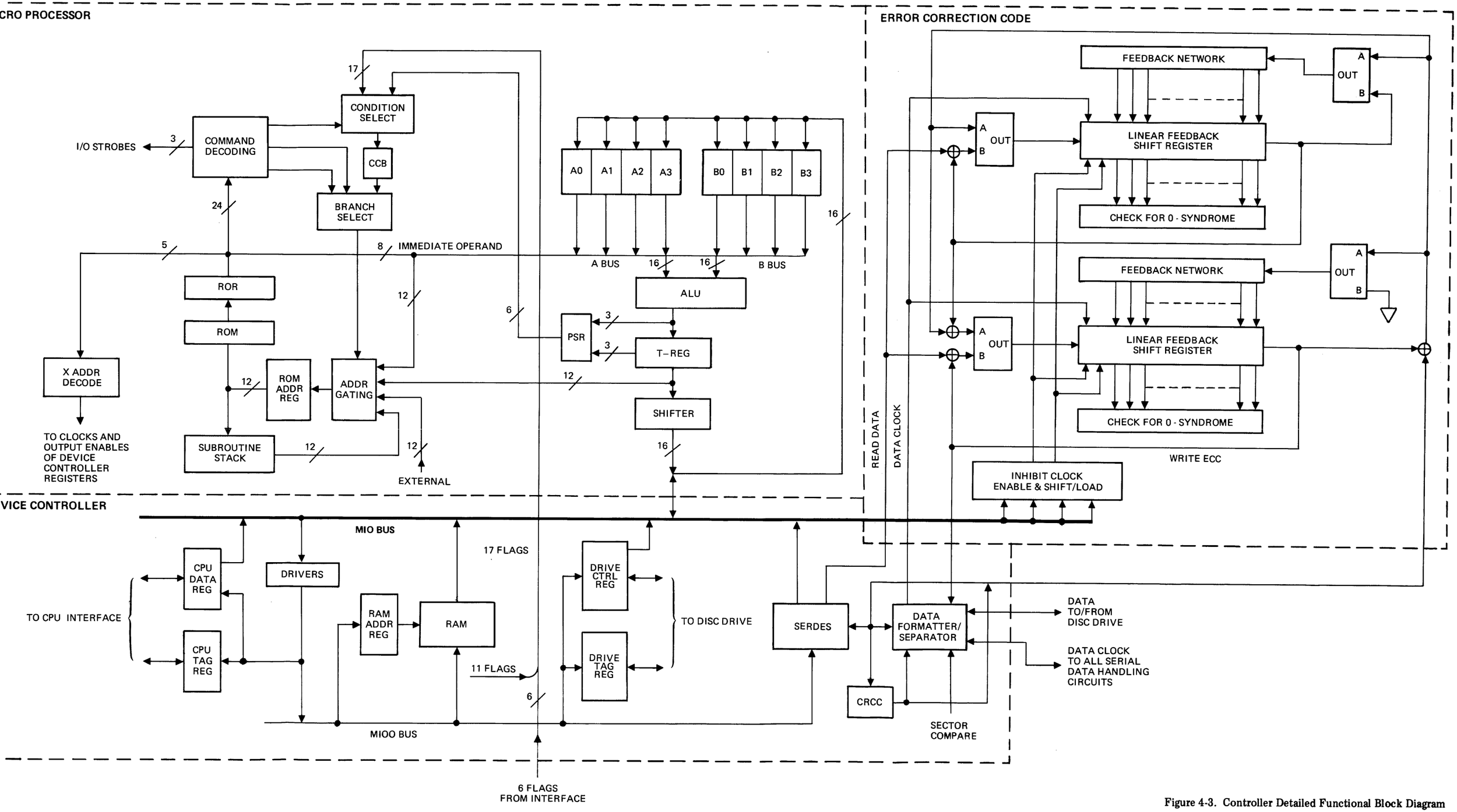


Figure 4-3. Controller Detailed Functional Block Diagram

The output of the rotate/shift logic is driven by three-state drivers on the MIO-bus. The drivers have three output conditions: high, low, or null. Data is valid to device controller or error correction only when an input or output strobe is present. Shift and pass instructions in the microprocessor can be used with upper or lower bytes, or full words. Rotate and swap instructions require full words only.

The ROM address register (RAR) addresses the ROM and the ROM output register (ROR) receives the ROM microcode instructions. The majority of ROR field readout in the microprocessor goes to the decode and control logic. The exception is the Immediate Operand field which is passed to the address gating and ALU.

The device controller is used as the input/output section of the controller. The microprogram controls the clocks and enables of the device controller for the proper transferring of data between a computer and disc drive. The format in which address and data fields are written on the disc is controlled by a data formatter. A sector compare pulse from the disc drive activates the formatter. By counting bits and 16-bit words and enabling data to be written at prescribed times, each sector is written in the format shown in figure 3-3.

Serial data from the output of the serial-deserializer (Serdes) is fed to cyclic redundancy check character (CRCC) and error correction code (ECC) generators. The bit pattern of the 16-bit CRCC word is a function of the sync word, address words, and data field bit patterns and the Boolean equation of the CRCC generator. The ECC words are generated as a function of the sync word, address words, data, and CRCC fields.

Serial data read from the disc drive is applied to a phase-lock loop in the data separator. Because variations in the rotational speed of disc drives causes the frequency of the clock information contained in the read data to vary, the phase-lock loop includes a voltage-controlled oscillator that provides the frequency flexibility required to compensate for these variations. The phase-lock loop produces a nominal output of 7.25 MHz, the precise frequency of the data when written. The combination of the phase-lock loop output and the read data input is used to generate a data clock which clocks the serial data bits at the frequency they are actually coming from the disc drive. Separated data is routed to Serdes, the CRCC generator, and the ECC circuitry. The CRCC and ECC generators process the read data and corresponding check words at the end of each data field and determine if a data error has occurred. If a possibly correctable data error is reported and, in response, a REQUEST SYNDROME command is received, the controller will attempt to provide information required to correct the error.

The random-access-memory (RAM) is a 64-bit (16x4) read/write memory device used as a scratch pad memory by the controller. Since the controller has the capability to be connected with four interfaces and

eight disc drives, RAM is used to store which disc drive an interface is connected to. A "hold" bit sent with a command from the interface is also stored. The RAM address register is used to address a particular memory location in RAM.

4-5. CONTROLLER POLLING

The controller treats each of two CPU ports (interfaces) as a peripheral device. Each is serially polled and asked for a command. If none is available, the controller checks the disc drives for interrupt (attention) requests, and if none is pending, polls the next port. When a port has a command request, the controller accepts the command and, if applicable, checks the unit number. The unit number is used to address a particular RAM location containing the number of the port last using the unit. If the requesting port number matches, the "hold/release" bit (passed in the command word) is placed in the memory with the port number. If set, the bit is used to block accesses to the unit by other ports during sequential operations (e.g.,seek-read). The controller checks the hold bit stored in RAM during the last operation on the unit. If it is set, access by a different requesting port is blocked and the operation is aborted. If it is not set, the number of the requesting port and the hold bit from the command word are stored in the RAM location corresponding to the disc drive and the operation proceeds.

If a disc drive interrupt request is noted during the poll sequence, the port number stored in the RAM location corresponding to the unit is retrieved. The poll is suspended and the port last using that disc drive is interrupted. The controller then awaits a command from that port.

Several commands leave information (status of some type, record address, etc.) in the controller. Because storage in both the port and the controller is limited, the controller suspends the poll to avoid destroying the information and remains connected to the port issuing the command. It is then up to the port to retrieve the information and ultimately issue a command that releases the controller, thus allowing it to resume its polling sequence. For most commands, the controller starts a timeout of 1.8 seconds. If the port does not respond with further commands during that time period, it is disconnected and polling resumes. The port is disconnected by an explicit END command, a timeout, or during execution of a SEEK or RECALIBRATE command. The port remains connected at all other times, including after a SEEK or RECALIBRATE command is completed. If a port is disconnected by a timeout, all hold bits set by that port are cleared.

Whenever the poll sequence is resumed, polling continues with the port that would have been connected next regardless of the fact that the controller may have processed an attention interrupt in between sequencing. Therefore, the sequence is never broken.

4-6. DETAILED DESCRIPTION

The following paragraphs give a detailed description of the microprocessor, device controller, error correction code, interfaces, and power supply.

4-7. MICROPROCESSOR

As shown in the microprocessor block of figure 4-3, the left half is instruction sequencing logic and the right half is the registers and arithmetic and logic modules.

All microinstructions are contained in the ROM. The command decoding block uses the current instruction to create control signals which operate the arithmetic-logic section. The ROM address register (RAR) contains the address in the ROM of the next instruction. This address is one greater than the previous address if a branch is not being executed. If a branch is being executed, the address gating network selects the proper branch address from one of four possible sources; the subroutine stack, an external address, the T-register, or the immediate field of a branch instruction.

The condition select block tests a flag and sets the condition code bit (CCB). The branch select logic looks at the CCB to decide if the branch is to succeed or fail. It also determines what type of branch is to occur.

The right part of figure 4-3 shows the four A- and four B-registers which may act as inputs for the ALU. Note that an 8-bit immediate operand may replace an A-register in some instructions. The ALU output is buffered in the T-register. Following this, the shifter rotates, shifts, or swaps bytes, putting the result on the MIO bus. This result is then directed to either an A- or B-register or to an external destination. The processor status register (PSR) latches six ALU and T-register conditions and makes them available to the conditional branch test circuitry.

4-8. ARITHMETIC LOGIC UNIT (ALU). The ALU performs all of the functions listed below. ROM bits 16 thru 20 and 14 in arithmetic and I/O microcode instructions specify which operation is to be performed. All operations may be performed on a 16-bit (full word) or 8-bit (byte) basis. ALU status is available after each arithmetic instruction and is held in the processor status register (PSR). Binary operations (marked *) must be performed on data in an A-register and a B-register. Two registers of the same type are not allowed. The result may go in any register. Note that subtraction is always A MINUS B.

The functions are:

PLUS*	INCLUSIVE OR*
MINUS*	EXCLUSIVE OR*
PASS	COMPLEMENT (one's complement)
INCREMENT (A-reg only)	LOGICAL AND*
DECREMENT (A-reg only)	

4-9. BUSES. The ALU is driven by the A- and B-buses, each of which connects to four 16-bit registers. The A-bus also connects to the 8-bit Immediate Operand field of the ROR. It should be noted that all binary immediate operations are with B-registers. All information on these buses is ground true. The MIO-bus is a three-state bus which connects the output of the ALU-shift unit to the registers. As shown in figure 4-3, this bus is also connected to the device controller and error correction functional blocks. Information on this bus is ground true.

4-10. A- AND B-REGISTERS. Eight 16-bit registers are implemented. Four registers (AØ-A3) drive the A-bus and four (BØ-B3) drive the B-bus. All are fed from the MIO bus. Microcode instructions may affect only the upper or the lower byte of these registers and, in some cases, may affect the entire 16 bits.

4-11. CONDITIONS. Seventeen external flags and six processor status indicators are available for use in conditional branches. They are positive true. The flags indicate conditions in the device controller or CPU-interface. Processor status is recorded during each arithmetic instruction in the PSR and is available until the next arithmetic instruction. These conditions are:

EQUAL-- available after a subtract instruction. Signifies that contents of selected A- and B-registers are equal.

UOVER-- signifies overflow (carry) out of ALU upper byte.

LOVER-- indicates carry out of lower byte of ALU.

TNZRO-- indicates that contents of T-register are not zero.

TMSB-- sign bit of T-register is true.

TLSB--least significant bit (LSB) of T-register is true.

FALSE--provided to prevent branching.

A set condition code (SCC) instruction should be executed before a branch to clock the selected condition into the condition code bit (CCB). The following branch will depend on the value set in the CCB by the last SCC instruction. If the CCB is false, the branch will not succeed and the microprogram continues at the next address. Any unsuccessful branch sets the CCB true to allow subsequent branching.

The following code is:

RS-- any SCC instruction can be coded to reverse the sense of any flag or PSR bit. For example, "CC = TNZRO,RS" would set the CCB true if the T-register contains zero.

4-12. SUBROUTINE STACK. The subroutine stack is a three-level last-in-first-out (LIFO) or push-down-stack. This register can store up to three microcode return addresses which allows three levels of subroutine nesting. Using this type of mechanization, the main microprogram can be diverted to a subroutine and return to the correct place after the subroutine is complete.

4-13. T-REGISTER. The T-register stores the results from the ALU. An indirect branch loads the contents of the T-register into the RAR.

4-14. SHIFTER. The shifter receives the ALU output through the T-register, does the necessary shifting, and outputs the result to the MIO bus. Allowable shifts are: shift left, shift right, rotate left, rotate right, swap bytes and pass (unchanged). All shifts are valid on full word (16-bit) operations. The only shifts valid for byte operations are shift left, shift right and pass.

4-15. CLOCKS. The controller runs on a crystal-controlled 30-MHz clock. The output of the clock is fed into a ring counter which generates six phases labeled T0 through T5. Each microcode instruction (except branches) is executed in 200 nanoseconds. A branch instruction inserts phases TX1 through TX3 after T5 and requires 300 nanoseconds.

4-16. ROM ADDRESS REGISTER AND ADDRESS GATING. The ROM address register (RAR) is a 12-bit counter register which addresses the ROM. Normally, the next instruction is the current address plus one, so RAR is incremented during each instruction. The RAR address gating provides for different types of branching in the microcode instructions. In a branch, one of four different address sources is loaded into the RAR. This address may come from the BRANCH ADDRESS field of the ROM, subroutine stack, T-register, or an external source (not shown) such as service device attached to the controller.

4-17. READ ONLY MEMORY (ROM). The microprocessor ROM consists of twenty-four 256x4 bit chips. These ROM's are organized as four banks (horizontal rows) of six ROM's per bank. This configuration gives an instruction word length of 24 bits and allows 1024 microcode instructions to be stored.

4-18. DEVICE CONTROLLER

The device controller contains circuitry which serializes and deserializes (Serdes) data as it is transmitted/received to/from the disc drive as a serial bit stream and to/from the CPU-interface as 16-bit words. The functional block also has a data formatter/separator which translates between non-return-to-zero (NRZ) coded data and time delay modulated data. The device controller has a

cyclic redundancy code check (CRCC) generator for checking the validity and integrity of data transmitted/received with the disc drive. A RAM is used as a look-up table (which can be changed) of interconnections between the eight disc drives and CPU-interfaces. The device controller also contains interfaces, registers, drivers, and receivers that support the tag and control busses for the disc drive. It also contains interfaces, registers, drivers and receivers that support the function and data busses for the CPU-interface.

Basically, all connections made external to the controller (i.e., the CPU-interface and disc drive) are made through the device controller. The device controller and microprocessor are linked by the bi-directional 16-bit MIO-bus, five external address lines, and several flags. All registers, drivers, and receivers are connected to the MIO-bus and are assigned one of 32 external addresses.

4-19. SERIAL-DESERIALIZER (SERDES). The Serdes converts parallel-to-serial and serial-to-parallel data between the CPU-interface and disc drive. A 16-bit word is received in parallel from the CPU-interface and is shifted out serially to the formatter-separator. From the formatter-separator, the data is transmitted serially to the disc drive. When reading from the disc drive, data is received serially by the formatter-separator. The serial data is clocked from the formatter-separator to Serdes. When 16 bits have accumulated in the serial-to-parallel input buffer of Serdes, the data word is transmitted in parallel to the CPU-interface.

4-20. DATA FORMATTER/SEPARATOR. The data formatter/separator is the final data output to/from the disc drive. The following discussion is divided into write and read operations. Figure 4-4 is an overall block diagram of the data formatter/separator.

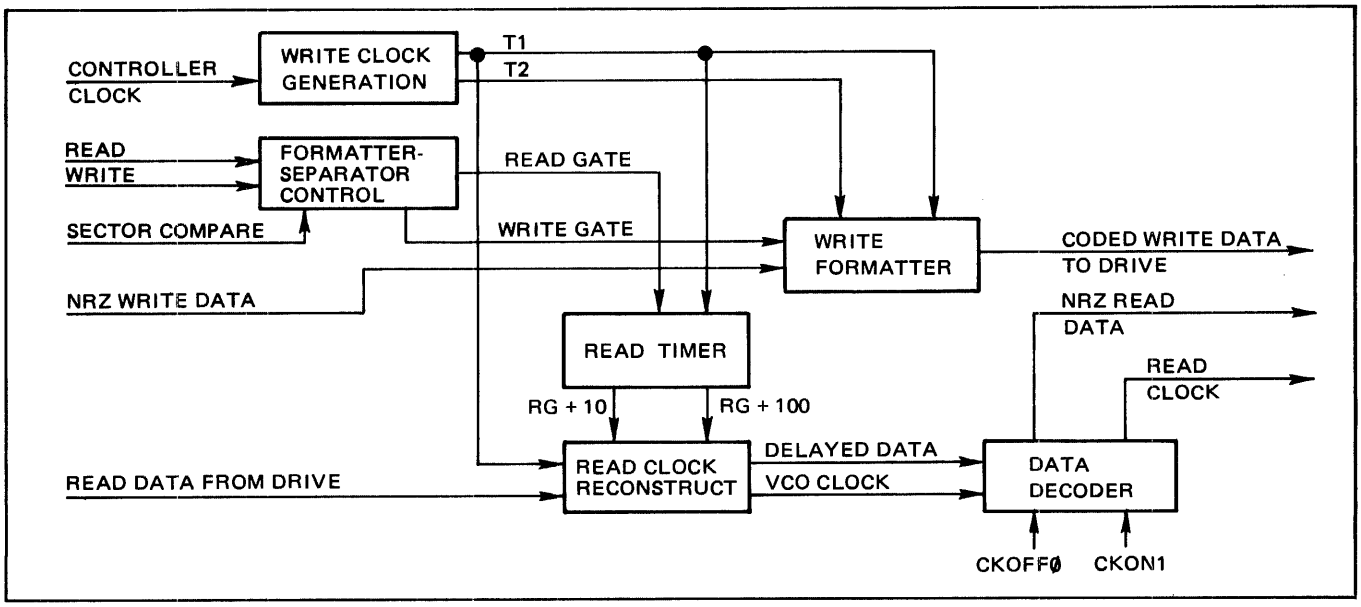


Figure 4-4. Data Formatter/Separator Block Diagram

The encoded write and read data is transmitted in a common shielded twisted pair transmission line between the controller and disc drive. Multiple disc drives are data cabled in a "star" configuration with each disc drive connected directly to a data port on the device controller. There are eight data ports on the device controller. These ports are non-dedicated. That is, any disc drive (logical unit) may be connected to any port. The line driver or receiver for each port is enabled by unit select being returned with a ground state from a selected disc drive on the shield of the interconnecting data cable.

4-21. Write Formatter. When enabled by a write command from an internal control word and a sector compare is received from a disc drive (formatter spearator control), the write clock generation clocks data to be written through a four-bit shift register. The data is clocked from Serdes at a 7.5-MHz rate derived from the 30 MHz clock on the microprocessor. As the data passes through the shift register, it is NRZ encoded and precorrected before being transmitted to the disc drive. Modified frequency modulation (MFM) coding is implemented using the following rules: (1) a transition is made in the middle of a "one" bit cell, and (2) a transition is made between two adjacent "zero" bit cells. The encoding is accomplished by sensing the pattern in the shift register and passing an appropriately phased write clock pulse where a transition should be made. The precorrection function decreases the effects of pulse crowding during a read operation. In summary, patterns in the shift register are detected to select an amount of time delay for each encoded write pulse. Pulses receiving no precorrection are nominally delayed and pulses to be advanced or retarded receive less or greater delay, respectively. Pulses preceded by a two-bit cell gap and followed by a one-bit cell gap are retarded. Pulses preceded by a one-bit cell gap and followed by a two-bit cell gap are advanced.

4-22. Read Separator. When a read command is received from the internal control word and a sector compare from a disc drive (formatter separator control), a timing sequence is initiated. The timing is done at a bit cell rate and referenced to the controller clock (write clock generation and read timer). For ten bit cells, the incoming data is ignored and the data separator phase-lock-loop (PLL) (read clock reconstruct) is locked to the controller clock which is the normal state for other than read operations. After the ten bit cell interval, the signal input of the PLL is switched to the incoming data and the PLL locks to the zero field of the sector. After one hundred bit cells have been counted, the PLL is assumed locked to the zero field and is enabled to track and retain lock on data. The PLL then outputs a data clock to the data decoder. After the hundred bit cell interval, the data decoder is enabled and will detect "ones" in the data stream. The first "one" to be detected is the first bit of the sync word. With detection, the sync bit, all following data, and clock are outputted to Serdes. The timing between the read data and read clock as inputted to the data decoder may be modified slightly in either direction by the microprogram, to read data which might not be retrievable by some other method.

4-23. CYCLIC REDUNDANCY CODE CHECK (CRCC). During a write operation, CRCC receives the serial data simultaneously with the data formatter and ECC. The CRCC has a 16-bit shift register which is operated in a load mode while data is being written on the disc drive. Its outputs and inputs are interconnected with three exclusive-OR gates in such a way that data is shifted with feedback on each data clock. At the end of the data field on each sector, the shift register contains the 16-bit CRC word. On completion of the data field, the CRCC shift registers are switched from load to shift mode and the next 16 data clocks cause the contents of the shift registers to be shifted out to the data formatter and ECC. This word is written on the disc directly after the data field.

When reading from the disc drive and as the data is being deserialized in Serdes, it is also being shifted into the CRCC shift register (load mode). The shifting is stopped within the shift register when the last bit of the CRC word is received. With the CRC word in this frozen state, circuitry within the CRCC acts as a 16-bit input OR gate which OR's together each bit of the CRC word. If any bit is not zero, there is an error in the sector and a CRC error flag is generated.

4-24. RANDOM ACCESS MEMORY (RAM). To implement the multiple CPU-interface communication ability of the controller, a 16-word by-4-bit (16x4) RAM is used in the device controller. This RAM correlates each disc drive (up to 8) with the last CPU to access it. The RAM also contains hold bits that indicate whether or not each disc drive may be accessed by a CPU-interface other than the last one to access it. This allows the overlapping seek feature to be implemented.

The following diagram is the layout of RAM which maps the disc drive unit number (same as the RAM word number except for numbers 11 through 15) into the number of the CPU-interface which last accessed that disc drive. Word 15 contains the number of the interface last polled to see if a command was pending. Word 14 contains the number of the interface currently connected to the controller. Word 13 is a sector counter used by the microprogram. Word 12 contains a disc drive type word, four encoded bits returned from the disc drive, which allow the controller to determine the number of heads and the number of sectors per track. Bit 3 of word 11, if true, indicates that the platter protect switch for the current surface is enabled, thereby prohibiting writing of any kind. Bit 2, if true, indicates that the format switch is enabled to override. Status bits correspond to CPU-interface numbers as shown in the diagram. All information is stored ground true.

BIT 3 2 1 Ø	WORD
X I I I	15
X I I I	14
C C C C	13
DRV TYP	12
P F X X	11
I I I B	1Ø
I I I B	9
	.
	.
	.
I I I B	1
I I I B	Ø

I--A 3-bit number (Ø through 7) representing CPU-interface to which associated disc drive (word number) was last connected. For words 15 and 14 only, I-field is as listed above in diagram. Words 15 and 14 are the same except when controller is responding to a disc drive attention request. There can be no disc drive numbers 11 through 15.

B--When set, indicates that CPU-interface has reserved disc drive for a series of operations. While B is set, no other CPU-interface may access that disc drive.

C--A sector counter used by microprogram.

P--When set, indicates that platter protect switch is enabled.

F--When set, indicates that format switch is enabled to override.

X--Not used.

4-25. RAM ADDRESS REGISTER. The RAM address register addresses a particular word in RAM for reading or writing in that cell.

4-26. DRIVERS. These circuits are drivers that receive from the MIO bus and drive a bus called "MIOO". The MIOO is a unidirectional 16-bit bus connected only to receiving devices.

4-27. CONTROLLER/CPU INTERFACE. The logical and physical interface provides the means for the computer I/O hardware to communicate with the controller. The CPU-interface must map from the computer I/O signals to those described in the following paragraphs. In general, the CPU-interface acts on orders from the CPU and from the controller. It is considered a slave to the controller in that the CPU I/O functions do not directly affect the controller, but are acted upon by the controller only after the controller interrogates the

CPU-interface. See figure 4-5 for a block diagram of the CPU-interface with the controller.

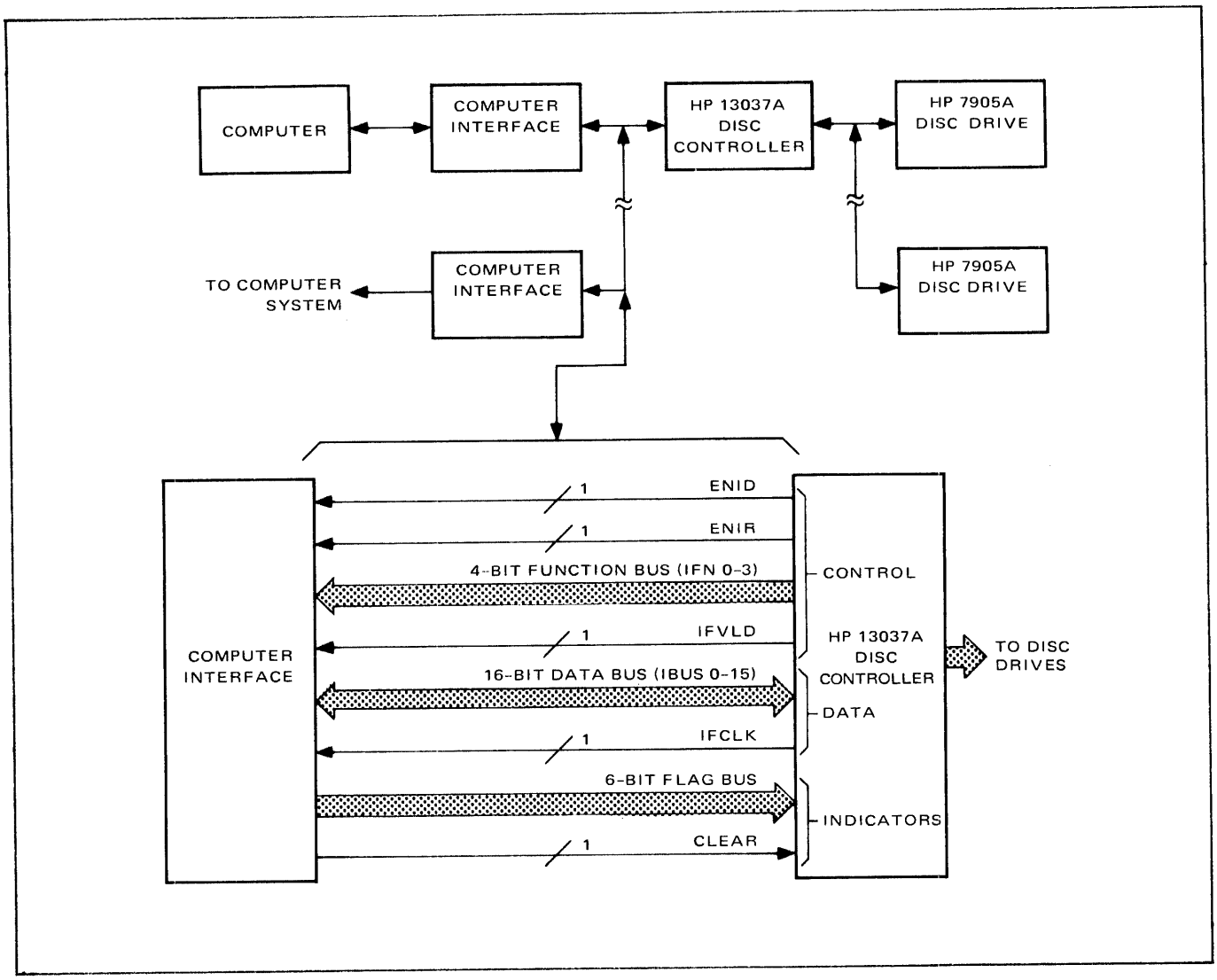


Figure 4-5. CPU-Interface to Controller Interface

The following signals describe the functions shown in figure 4-5.

Clear -- Hard clear on controller logic.

Data Bus (IBUS Ø-15) -- Bi-directional 16-bit bus used to transmit commands, data, status, and addresses between controller and CPU-interface.

ENID (Enable Interface Drivers) -- CPU-interface must be selected. Enables data bus drivers on CPU-interface.

ENIR (Enable Interface Receivers) -- Enables data bus receivers on CPU-interface.

Function Bus (IFN Ø-3) -- Four bit bus validated by IFVLD. Transmits CPU-interface functions from controller.

IFCLK (Interface Clock) -- Validates word transfers on data bus while IFIN, IFGTC, IFOUT, or WRTIO is true. Trailing edge must be used. (When IFOUT is true, the controller reads data at the leading edge.)

IFVLD (Interface Function Valid) -- Validates function on function bus. No function is valid if this line is not true.

Flags From Interface

Flags are gated out by a CPU-interface whose select bit is set.

CMRDY (Command Ready) -- True if a command is present in command register. Cleared by IFGTC.

DTRDY (Data Ready) -- True if data is present in data buffer. Cleared when data buffer is emptied.

EOD (End of Data) -- True if CPU-interface has completed a block transfer and data buffer is empty. Not set during data chaining until entire transfer is complete. Cleared when next command is fetched by controller. Note that controller may continue to fetch from data buffer after EOD is set while completing a sector transfer. Therefore, the next command may not be prefetched into data buffer.

OVRUN (Read Overrun) -- True if data buffer is full and controller tries to overwrite or data buffer is empty and CPU attempts to fetch. Setting is prohibited by EOD. Cleared when next command is fetched by controller.

Note: Write Overrun is detected by the controller whenever the data buffer is empty and controller attempts to fetch (unless EOD is also set).

XFRNG (Transfer No Good) -- False unless the CPU-interface detects an error condition (other than overrun) which prohibits transfer of data. Cleared by STINT.

INTOK (Interrupt OK) -- True if CPU-interface can be interrupted by a disc drive attention request. Other interrupt conditions do not examine this flag.

Function Bus Orders

Orders listed are validated by IFVLD. All edge validations are by trailing edge. The number immediately following the mnemonic is the octal code for that order. Table 4-1 contains a summary of the

function bus orders which includes the function bus octal code, mnemonic, mnemonic function description, and the data bus contents.

BUSY (16) -- Interface must be selected. ENIR is true. Clocks bit Ø of data bus into a bit on CPU-interface which, when bit Ø is high, signifies that controller has accepted a command and is executing it and that requested disc drive (if any) is available. (Bit Ø low=not busy.)

DSCIF (11)(Disconnect Interface) -- All CPU-interfaces respond. Used to clear CPU-interface select bit. When select bit is false, CPU-interface will not respond to select-required commands, or gate its flags or data bus out to the controller.

DVEND (Ø5)(Device End) -- CPU-interface must be selected. Transmitted by controller to terminate an operation it considers retryable (correctable or uncorrectable data error on read operations, overrun on any data operation).

IFIN (14)(Data In, Controller to CPU-Interface) -- CPU-interface must be selected. ENIR is true. Enables transfers into CPU from controller. While IFIN is true, trailing edge of IFCLK validates individual word transfers. This function is used for all transfers into the CPU.

IFGTC (15)(Get Command from CPU-Interface) -- CPU-interface must be selected. ENID is true. Used to gate contents of CPU-interface command register onto data bus. Clears CMRDY flag.

IFOUT (13)(Data Out, CPU-Interface to Controller) -- CPU-interface must be selected. ENID is true. Gates CPU-interface data buffer onto data bus. (Data is accepted by controller at leading edge of IFCLK.) Transfer validation is indicated by trailing edge of IFCLK. Used in all word fetches to controller except command fetch which uses IFGTC.

IFPRF (Ø2)(Pre-Fetch Command from Interface) -- CPU-interface must be selected. ENID is true. Gates contents of command register on CPU-interface onto data bus as in IFGTC, but does not clear CMRDY flag or otherwise alter CPU-interface.

RQSRV (Ø7)(Request Service) -- CPU-interface must be selected. Sets service request explicitly at end of any block transfer (in or out) involving more than command word (e.g., SEEK, READ, STATUS, etc.). While a block transfer is in progress CPU-interface may not fetch next command unless it goes to a buffer other than data buffer; RQSRV signals CPU-interface that controller has finished with its block transfer and it is all right to fetch next command.

SELIF (Ø3)(Select Interface) -- CPU-interface need not be selected. ENIR is true. A three-bit address is present on data bus (Ø:2). If it matches jumpered address on CPU-interface, CPU-interface uses IFVLD to set its select bit. When select bit is true

CPU-interface responds to select-required commands, responds to ENID, and gates its flags to controller.

SRTRY (Ø4)(Set Retry Counter) -- CPU-interface must be selected. ENIR is true. One byte of mode control data is present on data bus (Ø:7). Data bus (Ø:3) is interpreted by controller and should be ignored by CPU-interface. Data bus (4:7) is for use by CPU-interface (e.g., as a retry counter setting). The byte is an image of lower byte passed in a SET FILE MASK controller instruction.

STDFL (Ø1)(Set Data Flag) -- CPU-interface must be selected. Sets a bit on CPU-interface as follows:

To request direct transfer of a single word (SEEK, ADDRESS RECORD, STATUS, REQUEST SYNDROME, VERIFY, READ WITH OFFSET, REQUEST SECTOR, LOAD TIO REGISTER).

When a data operation is complete (COLD LOAD, READ, READ FULL SECTOR, VERIFY, WRITE, WRITE FULL SECTOR, INITIALIZE, READ WITH OFFSET, READ WITHOUT VERIFY).

To signal completion of a single-transaction command (SET FILE MASK, WAKEUP, CLEAR).

STINT (ØØ)(Set Interrupt) -- CPU-interface must be selected. Sets interrupt request bit on CPU-interface when controller discovers an error condition or when a disc drive is requesting attention.

WRTIO (12)(Write TIO) -- CPU-interface must be selected. ENIR is true. Data bus (Ø:15) contains controller status to be clocked into a CPU-test table status register.

Table 4-1. Function Bus Summary

FUNCTION BUS (3:0)	MNEMONIC	FUNCTION DESCRIPTION	DATA BUS CONTENTS
00	STINT	Interrupt Request	
01	STDFL	Information Request	
02	IFPRF	Pre-fetch Command	Command Word
03	SELIF	Select Interface	Interface Address
04	SRTRY	Set Retry Counter	Retry Count
05	DVEND	Device End (Set JMP MET)	
06		(Reserved)	
07	RQSRV	Request Service	
10		(Reserved)	
11	DSCIF	Disconnect Interface	
12	WRTIO	Write TIO	Status-1
13	IFOUT	Data Out (Write to Disc)	Data
14	IFIN	Data In (Read from Disc)	Data
15	IFGTC	Get Command	Command Word
16	BUSY	Set/Clear Controller Busy Bit	Busy Status
17		(Reserved)	

4-28. CONTROLLER/DISC DRIVE. As shown in figure 4-6, the controller/disc drive has the following groups of lines:

Tag Bus -- Four lines specifying what function is to be performed.

Control Bus -- Sixteen bi-directional lines containing additional command information (e.g., cylinder address, status).

Command Strobe -- Validates all tag bus functions.

Formatted Data -- A bi-directional line transmitting bit formatted data between the controller and disc drive.

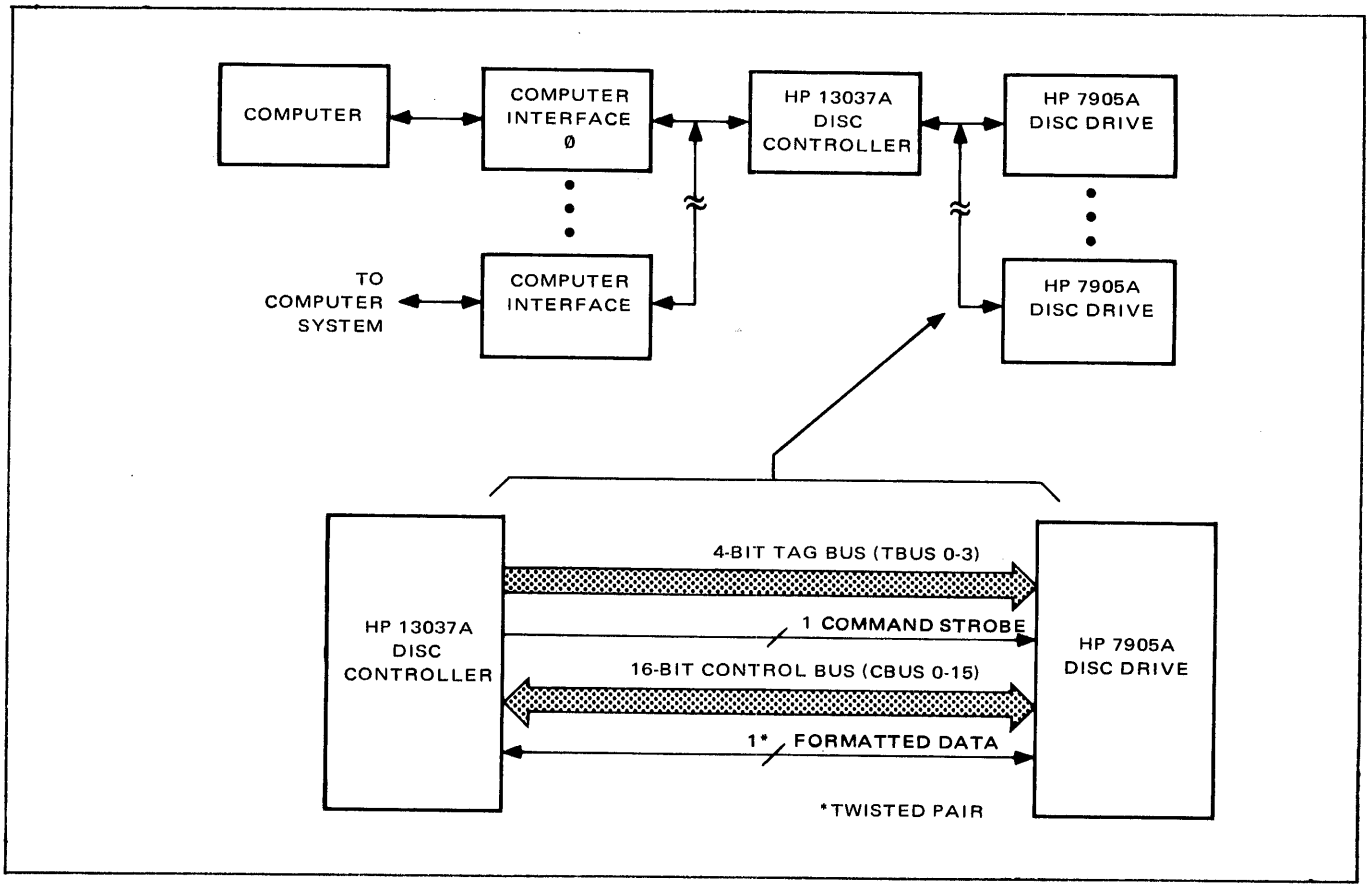


Figure 4-6. Controller/Disc Drive Interface Block Diagram

Tag Bus Functions

The tag bus is a four bit bus validated by command strobe, transmitting drive functions from the controller. All edge validations are by the leading edge of the strobe. Table 4-2 contains a summary of the tag bus functions which includes the octal code, operation, and relationship to control bus.

Read -- Select required. Disc drive gates status on control bus. When this function is valid, disc drive waits for leading edge of its internal sector compare signal, transmits sector compare in status word, and transmits bit-encoded data to selected head on formatted data lines.

Write -- Select required. Disc drive gates status on control bus. When this function is valid, disc drive waits for leading edge of its internal sector compare signal, transmits sector compare in status word, and accepts bit-encoded data from selected head on formatted data lines.

Request Status -- Select required. When this function is valid, disc drive gates contents of its status register on control bus.

Request Attention -- Select not required. When this function is valid, disc drive gates its attention bit on line of control bus corresponding to its unit number.

Disconnect -- Select not required. Disc drive responds to this function by clearing its select bit. When this bit is false, disc drive will not respond to select-required functions.

Clear -- Select not required. Disc drive clears its attention bit, non-destructive read/write faults, and any other appropriate bits (e.g., first status, sector address register).

Request Sector -- Select required. Disc drive transmits contents of its "current address" counter and head address register on control bus.

Note: There are two sector counters; one for each of the discs.

Seek -- Select required. Control bus contains cylinder address. On leading edge of command strobe, disc drive clocks control bus contents into its cylinder address register and initiates a seek to that address. Upon completion of seek, attention bit is set. If address is illegal, disc drive sets seek check and attention.

Address Record -- Select required. Control bus contains head-sector address. On leading edge of command strobe, disc drive clocks control bus contents into its head-sector address register. If address is illegal, it sets seek check.

Address Unit -- Select not required. Control bus contains 3-bit unit number. Disc drive responds by setting its select bit if control bus contents match disc drive address. If this bit is true, it responds to all select- required commands.

Recalibrate -- Select required. Disc drive positions its heads over cylinder Ø and clears its "current cylinder address" register.

Transmit Sector -- Select required. Control bus contains head-sector address. On leading edge of command strobe, disc drive clocks sector address only into its sector address register. Head address register is not modified.

Offset -- Select required. On leading edge of command strobe, disc drive clocks control bus contents into its position offset register.

Clear Status -- Select required. Control bus contains bits specifying what disc drive status to clear. Disc drive clears appropriate status bits in response to this function.

Table 4-2. Tag Bus Functions Summary

TAG BUS			
OCTAL CODE	OPERATION	CONTROL BUS (Refer to table 4-3)	
ØØ	READ*	STATUS	INFORMATION FROM THE DISC DRIVE
Ø1	WRITE*	STATUS	
Ø2	REQUEST STATUS*	STATUS	
Ø3	REQUEST ATTENTION	ATTENTION	
Ø4	DISCONNECT		
Ø5	CLEAR		
Ø6	REQUEST SECTOR*	HEAD-SECTOR ADDRESS	
Ø7			
1Ø	SEEK*	CYLINDER ADDRESS	INFORMATION FROM THE CONTROLLER
11	ADDRESS RECORD*	HEAD-SECTOR ADDRESS	
12	ADDRESS UNIT	UNIT ADDRESS	
13	RECALIBRATE*		
14	TRANSMIT SECTOR*	SECTOR ADDRESS	
15	OFFSET*	OFFSET	
16	CLEAR STATUS*	SELECT CLEAR	
17			

*Only selected units will respond.

Tag bus bit 3 determines whether controller or disc drive will place information on control bus.

Units respond to commands only after being selected except for Address Unit, Request Attention, Disconnect, and Clear.

Control Bus Functions

The control bus is a sixteen-bit bi-directional bus used to transmit control information and modifiers between the disc drive and the controller. Depending on the tag bus, the control bus contains one of the following functions. Table 4-3 contains a summary of the control bus functions which includes the bus lines and the relationship of the function to a specific line.

Attention -- A line-per-drive response. Each disc drive sets its attention bit when it loads, unloads, completes a seek, faults, or sets seek check. Attention bit is cleared by a clear or a clear command status command with bit Ø on. When attention is put on control bus, each disc drive unit drives only the bus line corresponding to its logical unit number.

Unit -- Valid unit numbers are Ø through 7.

Cylinder -- Valid cylinder numbers are Ø through 41Ø.

Head-Sector -- Valid head numbers are Ø through 2. Valid sector numbers are Ø through 47.

Offset -- Valid offset numbers are Ø through 63, positive or negative.

Clear Status — Bit Ø on specifies that attention bit should be cleared. Bit 1 on specifies that first status bit be cleared.

Status -- Contains current disc drive status:

Drive Busy -- True if heads are not positioned and settled over a valid track.

Drive Ready -- True if heads are over disc (loaded).

Seek Check -- Set if controller transmits an invalid cylinder, head, sector address, or if a seek is attempted while disc drive is still executing a previous seek command. Cleared when a valid operation is performed to correct error. Attention bit can then be reset by controller.

Note: The bounds checking is done by disc drive.

First Status -- Set when disc drive first loads heads on disc, i.e., by going from a "not ready" to a "ready" condition. Cleared by a clear status command with bit 1 set.

Drive Fault -- Set when disc drive detects either a read/write or servo fault; neither can be caused by controller under normal circumstances. Non-destructive read/write faults can be cleared by a clear command. Servo faults and destructive read/write faults unloads heads, and therefore requires operator intervention.

Format -- Transmits condition of format switch located at front of disc drive. This switch may be set to "FORMAT" position to allow track initialization.

Protected -- Transmits condition of platter protect switch located on front of disc drive corresponding to currently addressed head.

Attention -- Condition of attention bit. Cleared by a clear status command with bit Ø set.

Sector Compare -- True while a read or write command is true following coincidence of a leading edge of disc drive's internal signal comparing sector address register and "current sector address" counter. Cleared when command is removed or when disc drive determines that it is not safe to continue transfer because sector has almost passed.

Drive Type -- Four encoded bits which allows controller to determine number of heads and number of sectors per track.

Command Strobe Line -- Validates all functions on tag bus. No function is valid if this line is not true. If an edge is used it must be leading edge.

Formatted Data Lines -- A differential pair used to transmit serial bit formatted data to and from disc drive.

Table 4-3. Control Bus Functions Summary

BUS LINE	CLEAR STATUS	OFF-SET	CYL-INDER	HEAD-SECTOR	UNIT	STATUS	ATTEN-TION (Unit)
Ø	Atten-tion	1	1	Sector 1	1	Drive Busy	Ø
1	First Status	2	2	2	2	Drive Ready	1
2		4	4	4	4	Seek Check	2
3		8	8	8		First Status	3
4		16	16	16		Drive Fault	4
5		32	32	32		Format	5
6		64	64			Pro-tected	6
7		Sign	128			Atten-tion	7
8			256	Head 1		Sector Compare	
9			512	2		Drive Type 1	
10						Drive Type 2	
11						Drive Type 4	
12						Drive Type 8	
13							
14							
15							

4-29. ERROR CORRECTION CODE.

The error correction code (ECC) consists of three major functional parts corresponding to the three major functions that are performed on the disc drive subsystem. These functions performed are write, read and, if required, detect and correct errors. Figure 4-7 is a functional block diagram of the ECC which shows conceptually how the the shift registers are switched to perform the various operations.

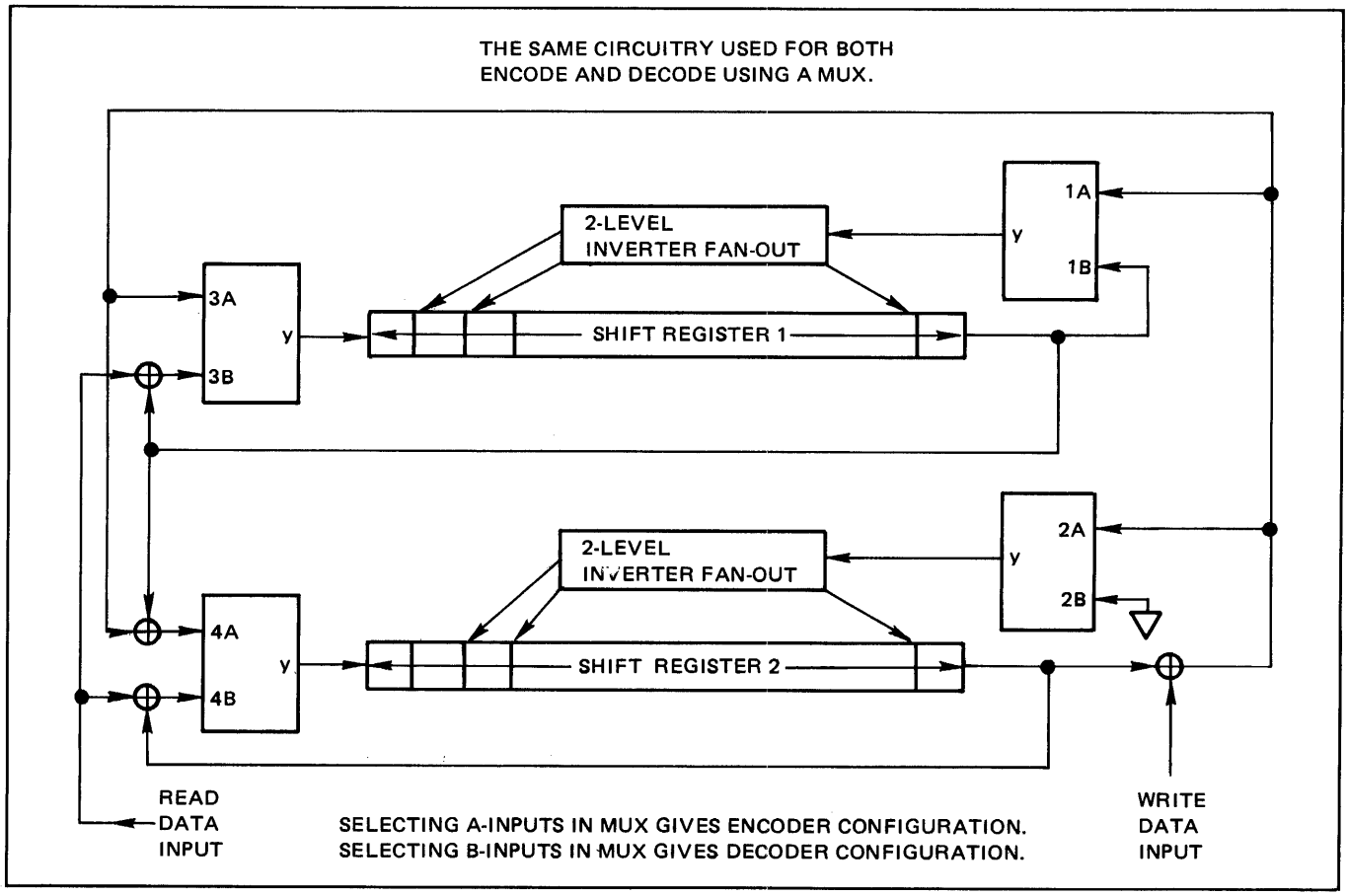


Figure 4-7. ECC Functional Block Diagram

4-30. ECC WRITE IMPLEMENTATION. For write operations, serial binary data is supplied to the ECC along with the data clock. The A-inputs of the multiplexers (MUX) are selected to provide the encoder configuration. (See figures 4-7 and 4-8.) At the end of the data, the check information is retrieved from ECC to be written in the last 6-word field of a sector on the disc. The data, when entered in the write mode, is pre-multiplied before being divided by the generator polynomial. The shift register is operated in a parallel load mode to

facilitate the division process. A control signal is provided to signify the entry of the last data bit. Also provided is control circuitry to enable the shift registers to shift out the computed check polynomial bit-stream to be appended to the data.

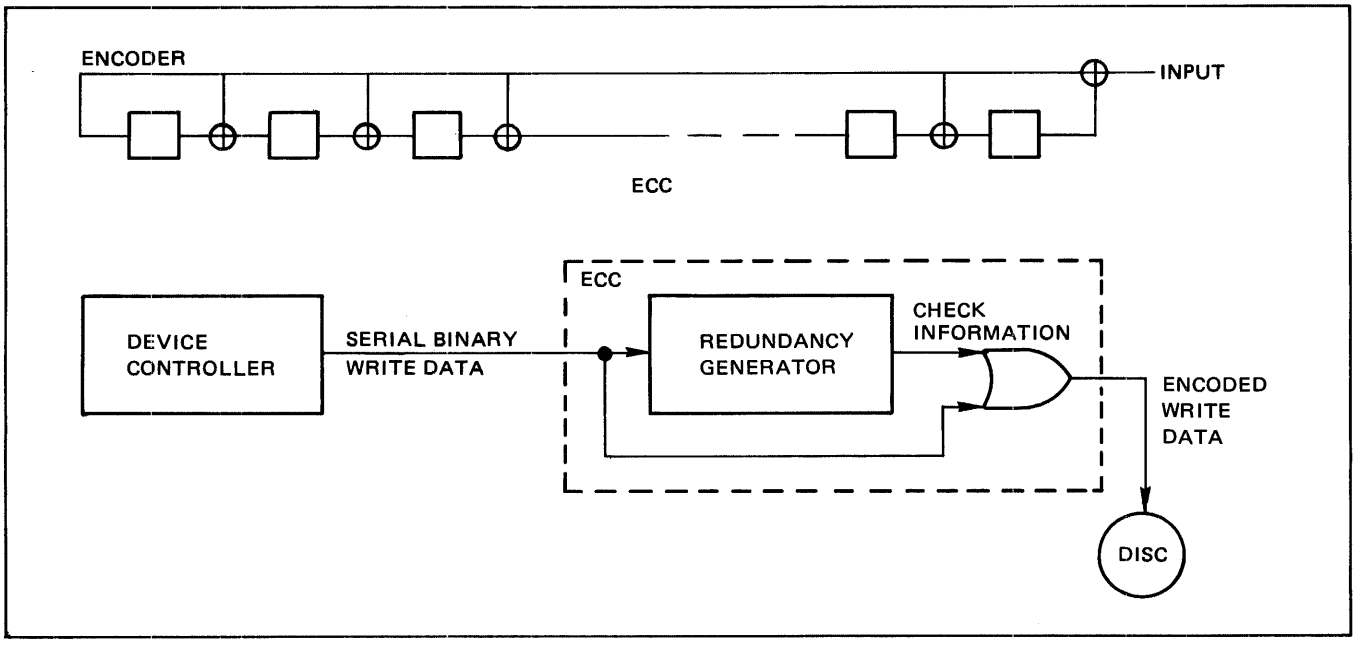


Figure 4-8. ECC Write Mechanization

4-31. ECC READ IMPLEMENTATION. During read operations, the B-inputs of the multiplexers (see figures 4-7 and 4-9) are selected to provide the decoder configuration. Serial data, along with the previously computed check bits, is supplied to both read inputs simultaneously. The input data is also accompanied by the data clock. The received polynomial is reduced by the generator polynomial and a control signal inhibits the shift registers from further computation when the last check bit has been input.

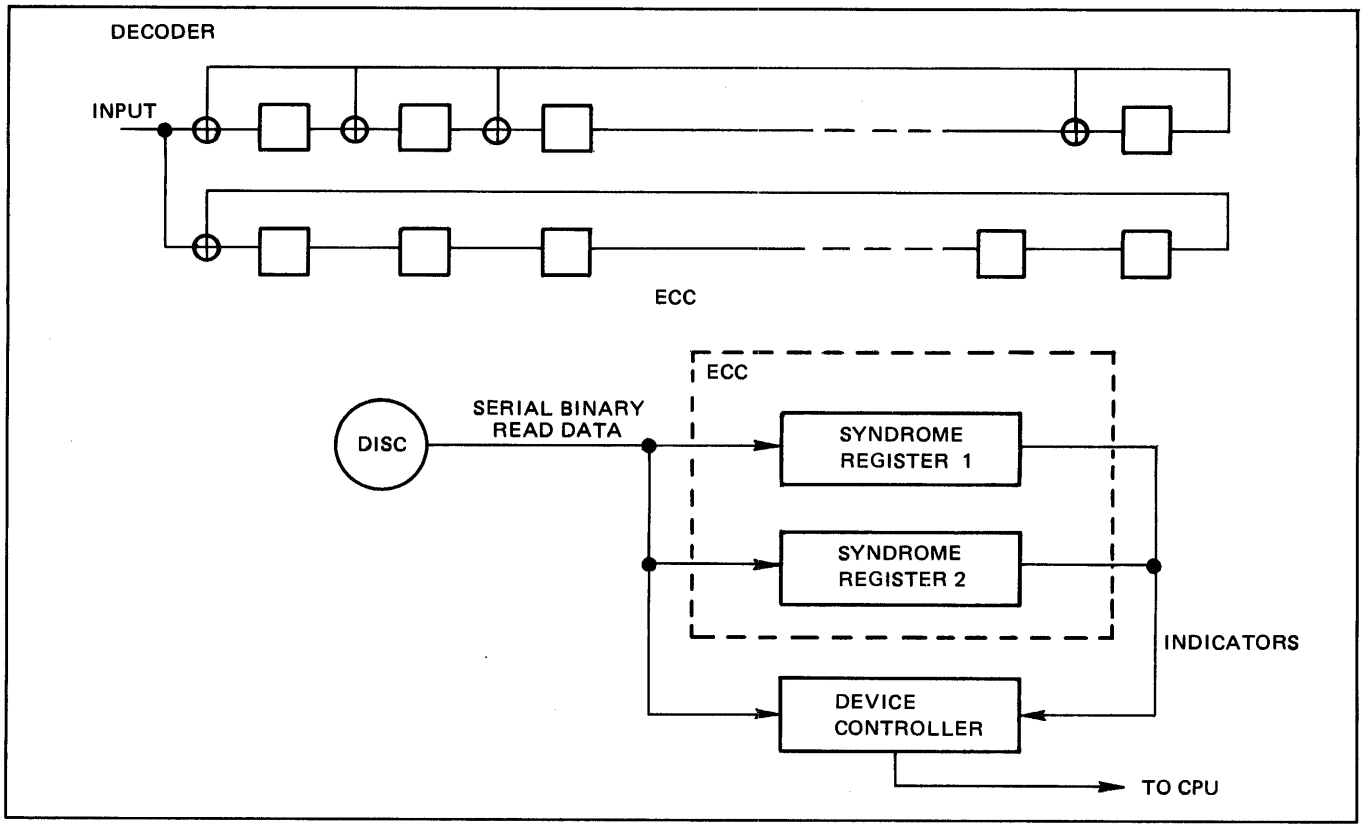


Figure 4-9. ECC Read Mechanization

4-32. ECC DETECTION AND CORRECTION. After the last check bit has been read in, the residues in the registers are checked for non-Ø value by the check-for-Ø-syndrome circuitry which consists of a network of OR gates. The device controller checks the two syndrome indicators and decides if an error has occurred. For detection of errors, the ECC defines the following types:

a. If both syndromes are Ø, there is no error.

b. If only one syndrome is Ø, an uncorrectable error has occurred.

c. If both syndromes are non-Ø, a possibly correctable error has occurred.

The device controller then interrupts the CPU-interface and reports the appropriate status that describes one of the above conditions and awaits the next command. If a possibly correctable error was reported to the CPU-interface and the device controller subsequently receives the REQUEST SYNDROME command from the computer, the algorithm (error correction) stored in ROM of the microprocessor is invoked. Execution of the algorithm is accomplished by ALU in the microprocessor. This algorithm terminates with either of two possible outcomes; the error is uncorrectable or, the error is correctable and the information required to correct the error has been successfully computed. If the error is correctable, the data pattern can be obtained by shifting the syndromes in their respective registers until they have the same representations. The error pattern required to correct the error is then sent to the computer. For further detail of the REQUEST SYNDROME command, refer to the description in section III.

4-33. POWER SUPPLY.

The controller power supply (see figure 4-10) consists of a printed circuit assembly (PCA) and various electronic components mounted in the rear portion of the controller chassis. The dc power is supplied to the controller PCA's through each board's power connector P1. The power supply provides +5V @ 15A, -5V @ 300mA, -15V (unregulated), and a power up signal to the controller logic. Overvoltage and overcurrent protection circuits and fuses in the transformer primary and secondary circuits protect the controller logic boards.

The input line voltage is reduced to the proper level by the power transformer and is coupled to the rectifier and filter. Series pass transistors act as variable resistances to keep the output voltage constant. The series pass transistors are driven by an error amplifier and comparator which compares the output voltage to a reference voltage. Current sense circuitry detects an overcurrent condition and shuts down the series pass transistors by grounding the output of the error amplifier. If an overvoltage condition is detected, the power supply is shut down. The -5 volt supply is rectified, filtered, and regulated independently from the +5 volt supply. The unregulated -15 volt supply is generated with a voltage doubler.

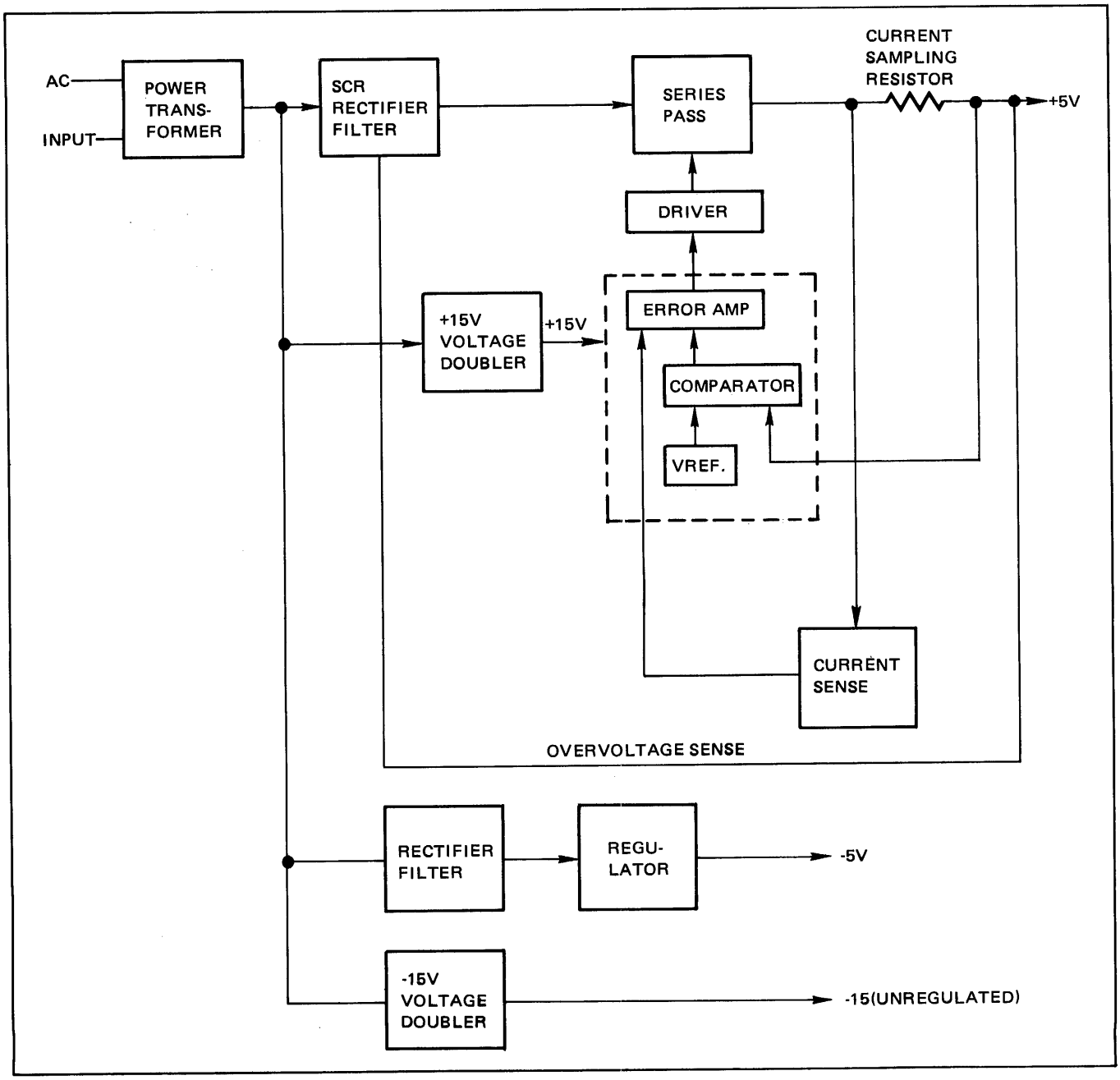


Figure 4-10. Power Supply Functional Block Diagram

The power supply will operate on nominal line voltages of 100V, 120V, 220V, and 240V. Line voltage selection is accomplished by orienting a small printed circuit card which plugs into the line module. (See figure 2-3.) The line module accepts the line cord, directs the line current through a fuse, and selects the proper power transformer primary wires. The power supply fan and the controller logic board fan connect to the power transformer primary wires in such a way that the fans always receive a nominal 120 VAC regardless of the line voltage. The power supply will operate on 50 Hz or 60 Hz with no adjustments. The filter capacitor and power transformer are bolted to the rear of the chassis behind the power regulator board. Except for the line module, all other power supply components are located on the power regulator circuit board.

Section V

SERVICE

5-1. INTRODUCTION

This section includes general servicing information, maintenance reference material, preventive maintenance, and troubleshooting. Within the maintenance reference section is a circuit diagram for power distribution, a description of the microprocessor instructions and microinstruction formats, and an operating procedure for the controller service unit (CSU).

5-2. GENERAL SERVICING INFORMATION

Ensure that controller printed-circuit assemblies (PCA's) remain firmly installed in their PCA module slots with the extractor handles locked in place. All cables should also be firmly attached to connectors.

Dangerous voltages are present in the controller. Use caution when working on controller components. It is essential that all cautions and warnings stated in cabinet or other maintenance documents be observed.

WARNING

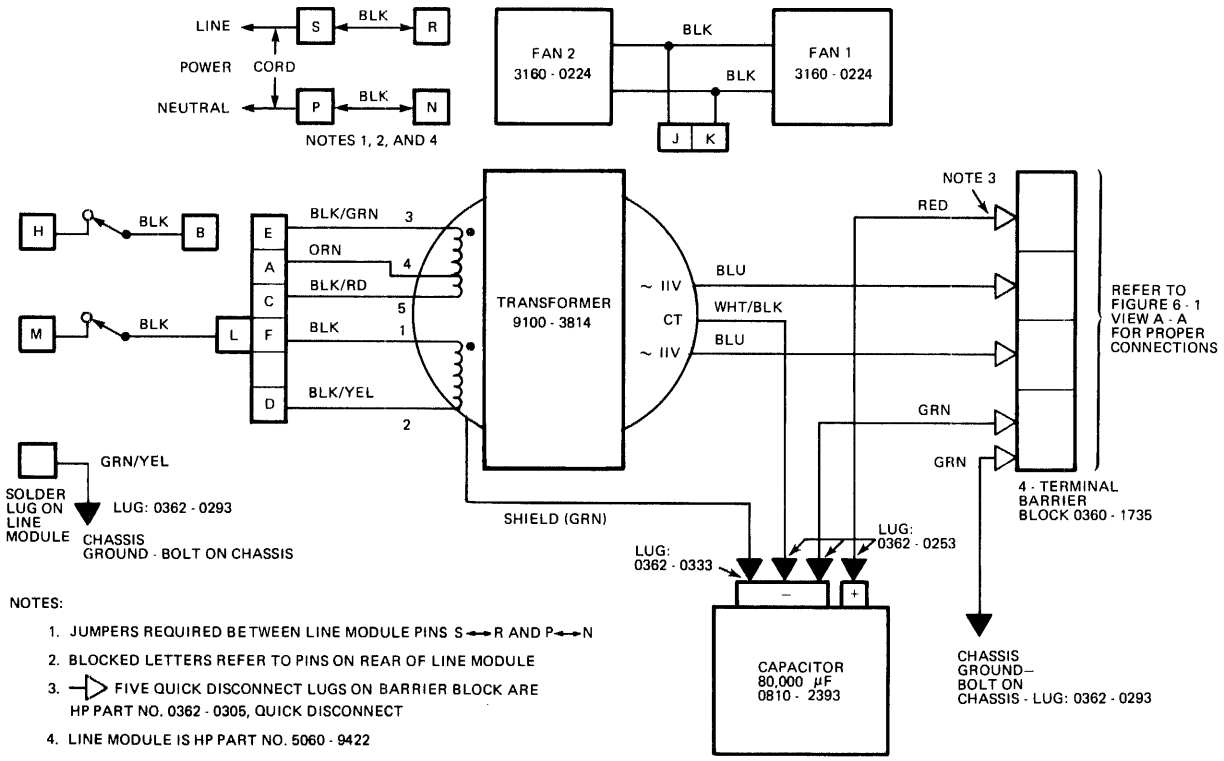
Hazardous voltages are exposed when the top cover is removed.

Before removing or installing controller PCA's, set the POWER switch to OFF to remove power from the PCA connectors. Also follow this procedure for PCA extender assemblies.

5-3. MAINTENANCE REFERENCE INFORMATION

5-4. POWER DISTRIBUTION

Power distribution for the controller is shown in figure 5-1. This diagram applies only when the three PCA's are enclosed in the controller chassis. If the controller chassis is not used and the PCA's are installed separately, refer to the appropriate document listed in section I of this manual.



7103-8

Figure 5-1. Controller Power Distribution

5-5. MICROPROCESSOR INSTRUCTIONS

The microprogram controls the hardware of the controller through the sequencing of the microinstructions. These microinstructions are divided into fields whereby each field controls a specific function in the hardware. Each microinstruction is 24 bits in length. The microcode is stored in the microprocessor ROM. There are five microinstruction word formats. Each format, and the fields contained therein, raises specific controls which operate upon the logic circuits. The formats are Output Immediate Operand (OTI), Arithmetic (ARITH), I/O Command (IOC), Branch, and Condition Code (CC). Bits 21 through 23 define the type of microinstruction to be executed. The general microinstruction format is shown in figure 5-2.

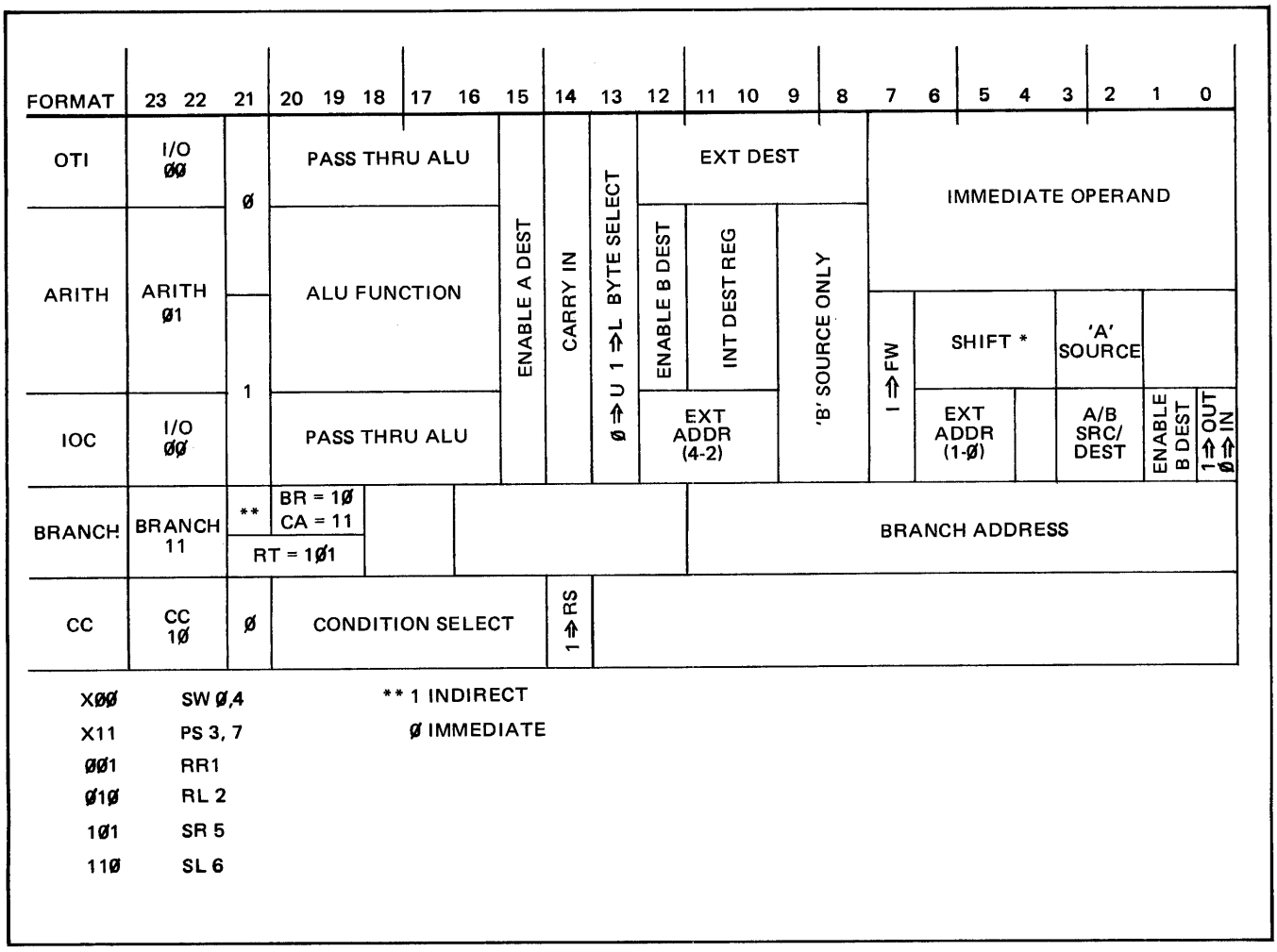


Figure 5-2. Microinstruction Format

5-6. OUTPUT IMMEDIATE OPERAND (OTI). The OTI format is shown in figure 5-3. OTI passes the immediate operand contained in bits Ø-7 through the ALU (bits 16-2Ø) and shifter to the MIO-bus. Information on the MIO-bus is ground true. The external destination contained in bits 8-12 is put on the external address bus and is positive true. External select is true for the entire instruction time. At time T5, the UB or LB strobe (depending on bit 13) is transmitted. The strobe occurs for one clock period and is positive true. No shift is performed.

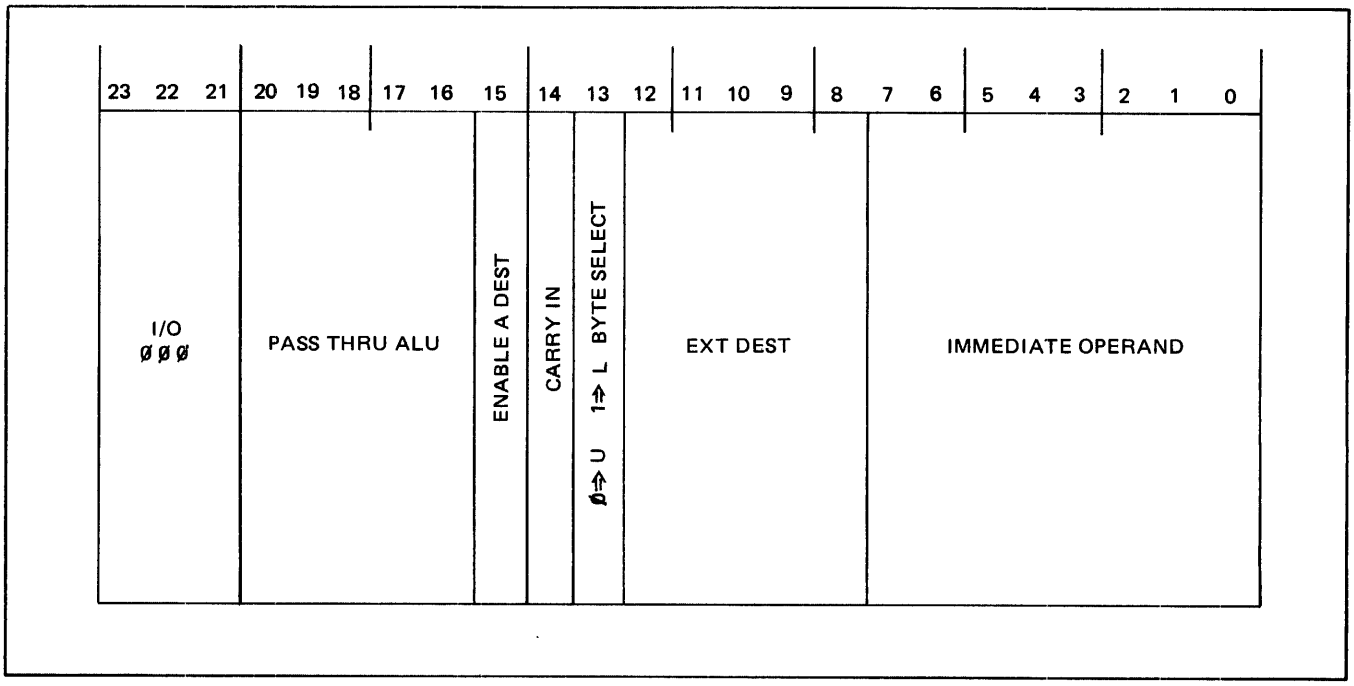


Figure 5-3. Output Immediate Operand Format

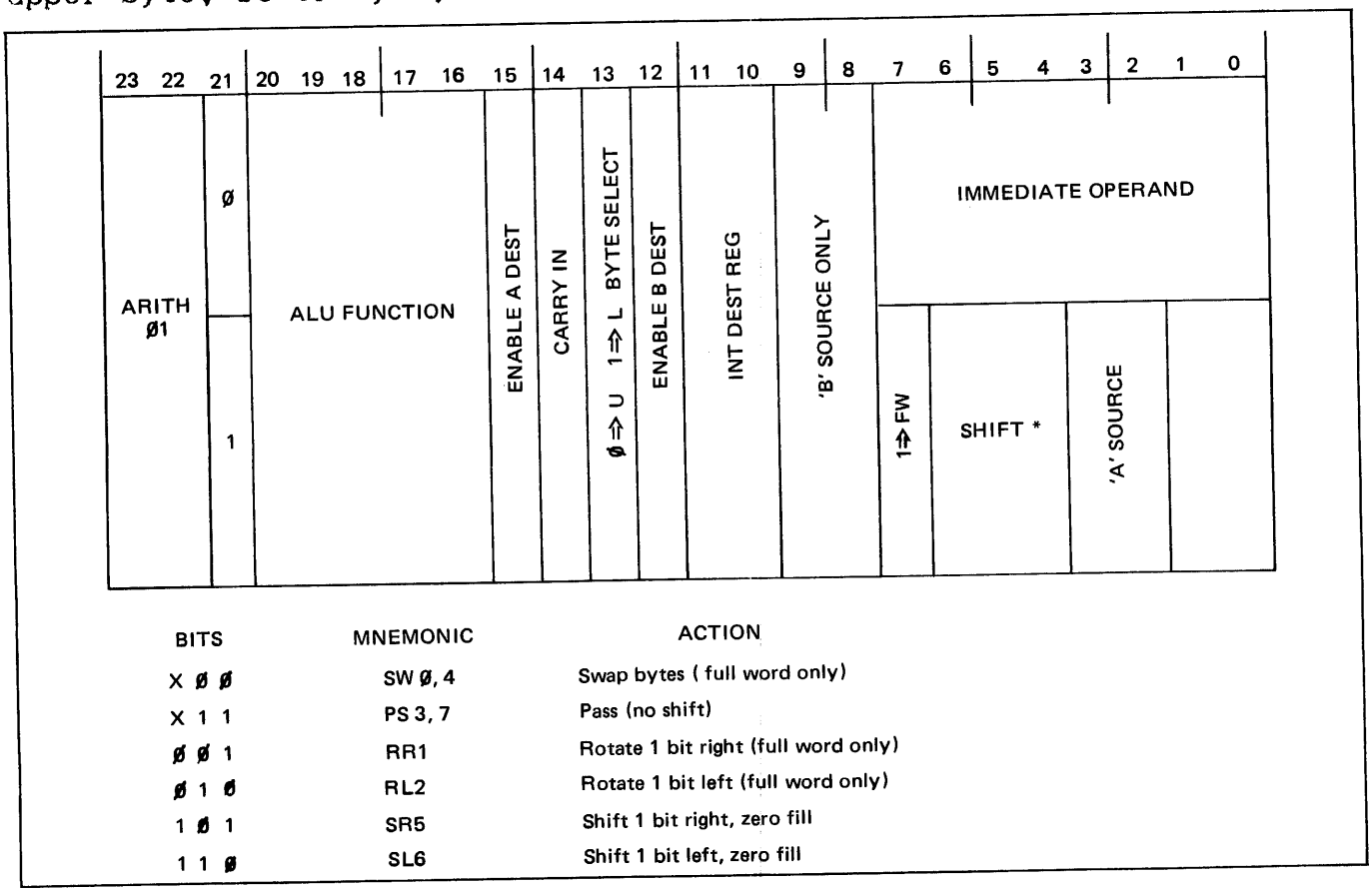
The fields shown in figure 5-3 are described in the following paragraphs.

U/L field — If Ø, immediate operand is put on upper byte of MIO-bus. If 1, immediate operand is put on lower byte.

EXT DEST field — A five-bit field containing address of external destination of immediate operand.

IMMEDIATE OPERAND field — An eight-bit field containing binary information to be output to address contained in EXT DEST field.

5-7. ARITHMETIC (ARITH). There are two different formats within the ARITH instruction. They are with and without the immediate operand. The ARITH format is shown in figure 5-4. With immediate operand, the ALU performs the operation specified by bits 14, and 16-20. It takes as inputs the immediate operand (bits 0-7) from the A-bus and a B-register specified by bits 8 and 9. Bits 10 and 11 specify the number of the register into which the result is written. Bits 15 and 12 specify whether an A-register, B-register, both, or neither are written into. U/L specifies which byte is affected. No shift is performed. Without immediate operand, the ALU performs the operation specified by bits 14 and 16-20. It takes as inputs an A-register specified by bits 2 and 3 and a B-register specified by bits 8 and 9. A shift specified by bits 4-6 is performed on the result. Bits 10 and 11 specify the number of the register into which the result is written. Bits 15 and 12 specify whether an A-register, B-register, both, or neither are written into. U/L and FW specify whether the upper byte, lower byte, or both are affected.



BITS	MNEMONIC	ACTION
X 0 0	SW 0, 4	Swap bytes (full word only)
X 1 1	PS 3, 7	Pass (no shift)
0 0 1	RR1	Rotate 1 bit right (full word only)
0 1 0	RL2	Rotate 1 bit left (full word only)
1 0 1	SR5	Shift 1 bit right, zero fill
1 1 0	SL6	Shift 1 bit left, zero fill

Figure 5-4. Arithmetic Format

The fields shown in figure 5-4 are described in the following paragraphs.

ENABLE A DEST and ENABLE B DEST fields

Either, if set to 1, causes result of operation to be written into a register on A- or B-bus. If both are set, an A- and

B-register are paired and result is written into both registers. If neither is set, result is left in T-register until T4 of next instruction. This allows computation of a final branch address or testing one or more bits in processor status indicator (PSR) without need to write information back into a register.

INT DEST REG field

Contains number of register into which result will be written. ENABLE A DEST and ENABLE B DEST determine which group (A or B) will be written into.

A SOURCE and B SOURCE fields

Specifies which register is put on each bus for an ALU operation.

IMMEDIATE OPERAND field

An eight-bit number used in an ALU operation with a B-register. Only one byte is affected.

U/L and FW fields

These bits determine which byte(s) is affected during an operation. If FW=1, both bytes of sources are used and both bytes of result are written in destination. If only U and L is specified, only that byte of operand(s) and destination are affected. Remaining byte in both source(s) and destination is left unaffected.

SHIFT field

A three-bit field specifying what shift operation is to be done on result from ALU before result is written into its destination. May not be used with an immediate operand.

5-8. I/O COMMAND (IOC). The IOC format is shown in figure 5-5. There are two different conditions for IOC. They are input and output with a selected register. During input to a register, IOC selects an external source and loads a selected register with the contents of that source. The external source address (bits 8-12) is put on the external address bus; external select is false. Input strobe is sent out positive true. At the trailing edge of T5, the data on the MIO-bus is written into the register(s) selected by bits 2, 3, 15, and 1 (an A-register, B-register, both, or neither). If FW=1, the entire 16 bits of the MIO-bus is stored. If only U or L is true, only the appropriate byte is stored. During output from a register, IOC outputs a selected register to a selected external destination. The source register is selected by bits 2 and 3. Note that bits 15 and 1 (Enable A Destination and Enable B Destination) are meaningless in this case. External select is true during the entire instruction time. At time T5, UB out, LB out or both (depending on U,L and FW) is transmitted.

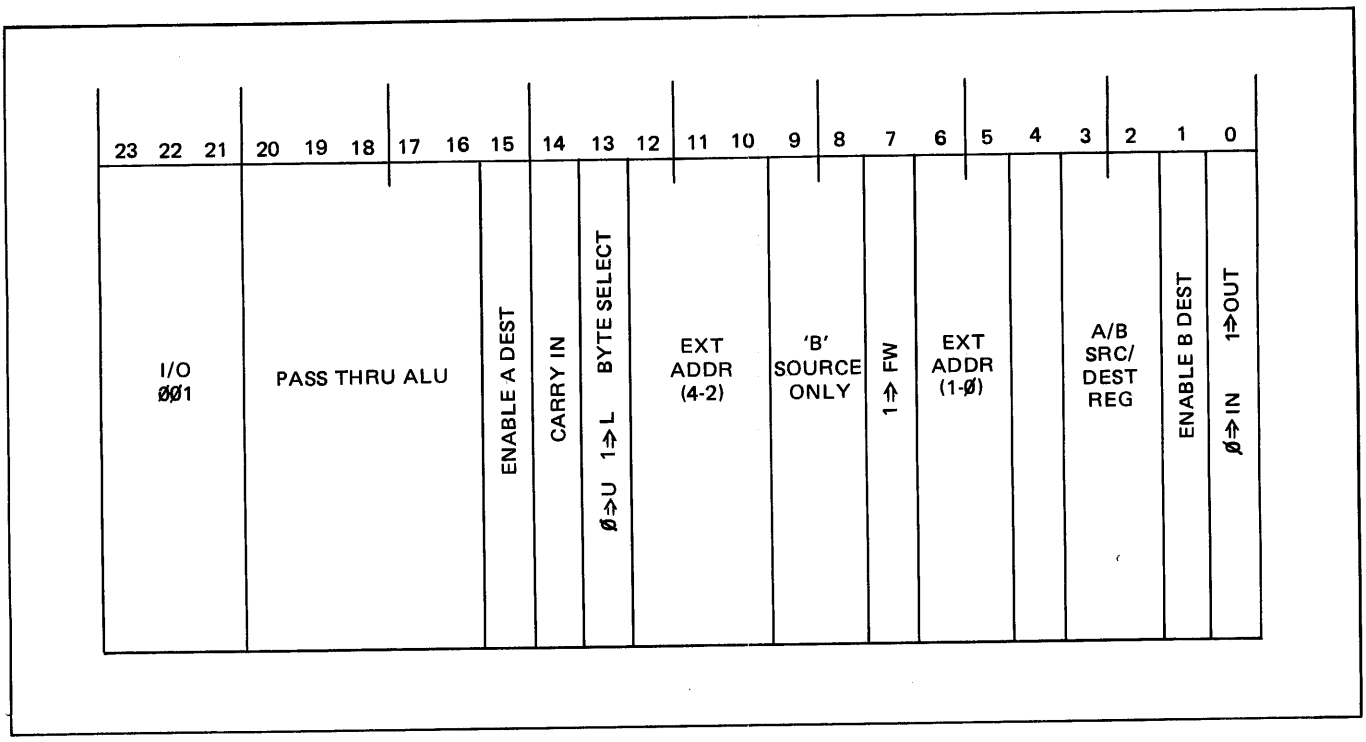


Figure 5-5. I/O Command Format

The fields shown in figure 5-5 are described in the following paragraphs.

ENABLE A DEST and ENABLE B DEST fields

Input only. Output is meaningless. Either, if set to 1, causes result of operation to be written into a register on A- or B-bus. If both are set, an A- and B-register are paired and result is written into both registers. If neither is set, result is left in T-register until T4 of next instruction. This allows computation of a final branch address or testing one or more bits in PSR without need to write information back into a register.

U/L and FW fields

These bits determine which byte(s) is affected during an operation. If FW=1, both bytes of sources are used and both bytes of result are written in destination. If only U and L is specified, only that byte of operand(s) and destination are affected. Remaining byte in both source(s) and destination is left unaffected.

EXT ADDR field

For input, a five-bit field containing address of an external source whose contents are to be stored in a processor register.

For output, five-bit field containing address of external destination of information stored in designated processor register.

A/B SRC/DEST REG field

On input, used in conjunction with ENABLE A DEST and ENABLE B DEST fields to specify register(s) into which information is to be written. On output, number address of register to be output. Used in conjunction with ALU FUNCTION field in determining specific register to be accessed.

I/O field

A one-bit field specifying whether a register is to be input or output.

5-9. BRANCH. The BRANCH format is shown in figure 5-6. There are three different instructions in the BRANCH format; branch, call, and return.

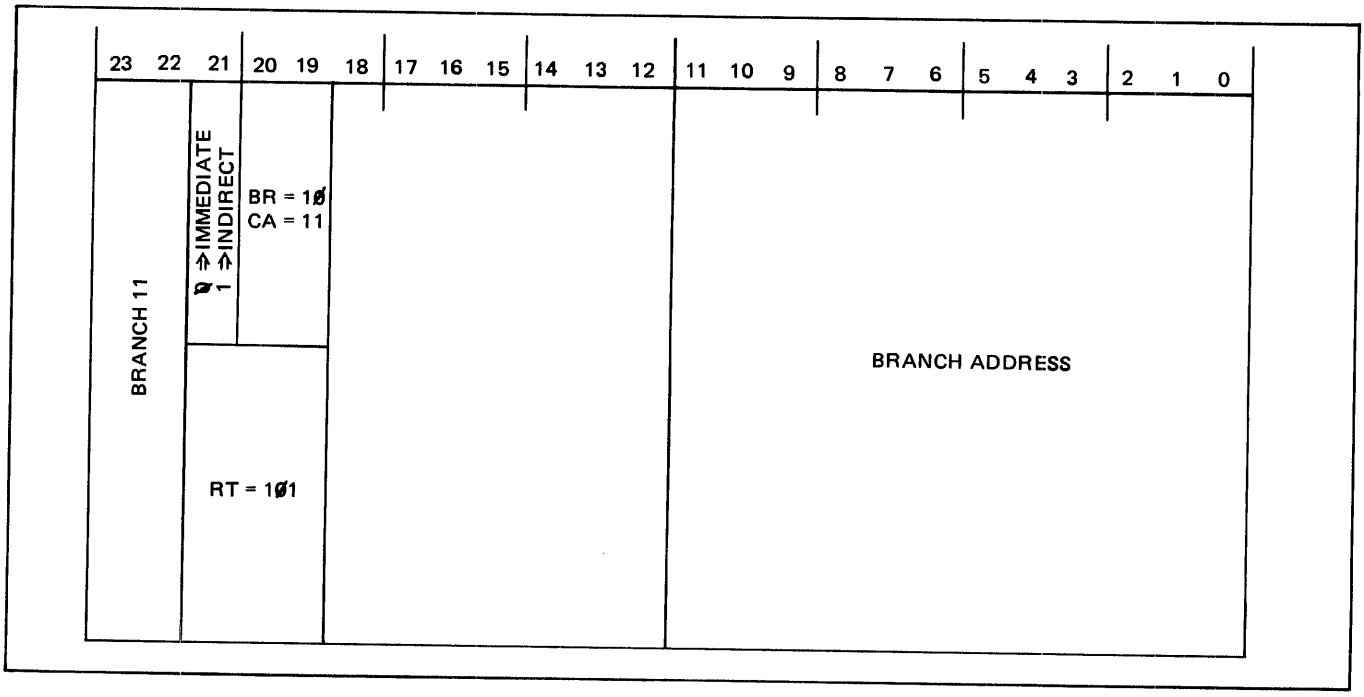


Figure 5-6. Branch Format

The fields shown in figure 5-6 are described in the following paragraphs.

BR field If CCB is false, branch is not taken, CCB is set true and instruction following the branch is executed. If CCB is

true and if branch is specified by bit 21 to be indirect, contents of T-register replaces contents of P-register, i.e., T-register contains address of next instruction. If bit 21 specifies a direct branch, address contained in bits Ø-11 is used as address of next instruction. CCB is always set true at end of instruction.

CA field — Operation is like a branch except that before branch is taken (only if CCB is true) contents of P-register are written into S-register. CCB is always set true at end of instruction.

RT field — If CCB is true, address in S-register top-of-stack (TOS) replaces address in P-register, and S-register is shifted. If more than three shifts are made, first-in address will always be used. If CCB is false, P-register is incremented. CCB is set true at end of instruction.

5-1Ø. CONDITION CODE. The CONDITION CODE format is shown in figure 5-7. The CONDITION CODE samples the condition specified (one of 17 external flags, PSR status, or unconditional) and sets its value into the condition code bit (CCB). RS may be used to reverse the sense of the condition. The next branch will be affected by the condition of this bit.

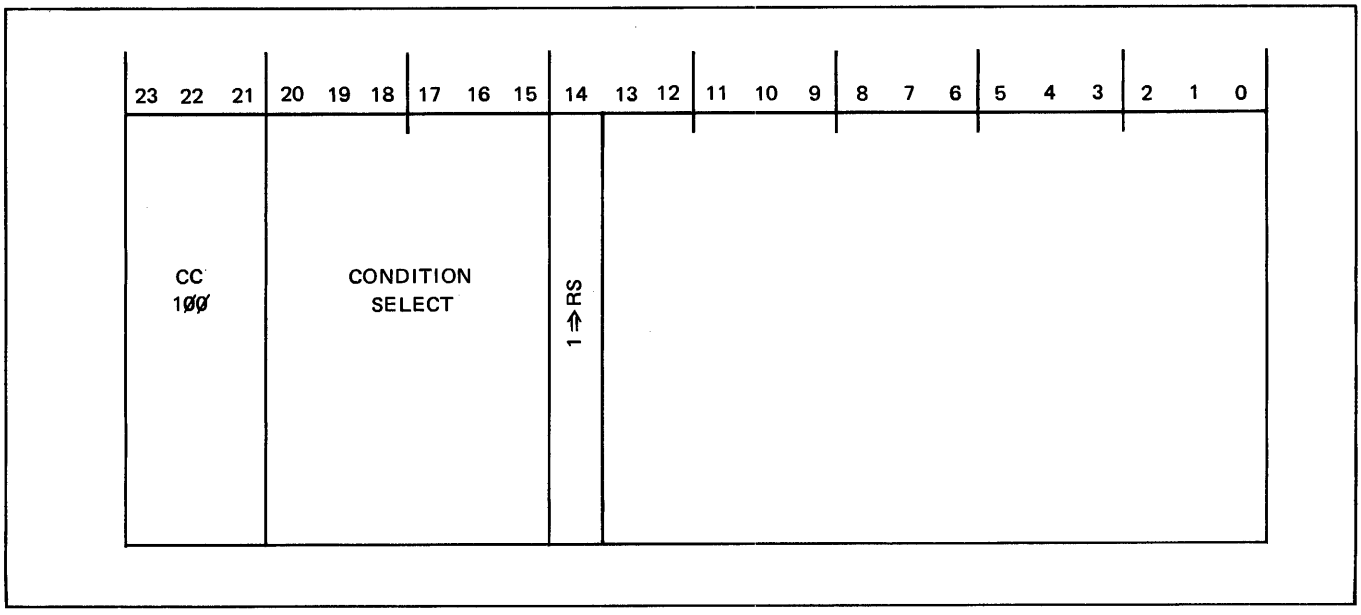


Figure 5-7. Condition Code Format

The field shown in figure 5-7 is described in the following paragraph.

CONDITION SELECT field

01 0000 thru 01 1111	External flags 00B-17B
10 0000	External flag 20B
10 0001	LOVER - Lower byte ALU carry
10 0010	EQUAL (A=B, available after SUB)
10 0011	UOVER (ALU overflow)
10 0100	TNZRO (contents of T are not 0)
10 0101	TMSB (Sign of contents of T)
10 0110	TLSB (LSB of contents of T)
10 0111	FALSE (Unconditional false)

5-11. CONTROLLER SERVICE UNIT (CSU)

The CSU for the HP 13037A Disc Controller consists of one PCA of the same physical size as the PCA's in the controller. The CSU is connected to a control/display unit by two cables. It has four modes of operation: on-line, microdiagnostic, ROM test, and single CPU instruction. Operating procedures and connections will be supplied at a later date.

5-12. ON-LINE MODE. The CSU monitors the operation of the controller in this mode. The controller may or may not be connected to a CPU or to a disc drive. The following functions are performed:

a. Display in octal the contents of the RAR.

b. Display in octal the contents of the MIO-bus, ground true or plus true.

c. Display in octal the 24-bit ROM word corresponding to the current RAR contents.

d. Display the current clock phase: one light-emitting-diode (LED) per clock phase, T0 through T5.

e. Allow the 30 MHz internal microprocessor clock to be replaced by:

   (1) A clock of arbitrary frequency from an external signal generator.

   (2) A signal derived from a push button on the CSU. This push button advances the clock one phase each time the button is pressed.

f. Load an external address from switches on the CSU into ROM address register of the controller microprocessor.

g. Clear the controller, setting the RAR to address zero.

h. Set a breakpoint address for the microprocessor. When the RAR reaches this breakpoint, it will halt if the BREAKPOINT ENABLE

switch is asserted. A "breakpoint trigger" terminal provides a pulse whenever RAR address equals the breakpoint address. This pulse may be used to trigger an oscilloscope.

5-13. MICRODIAGNOSTIC MODE. The CSU contains 1Ø24 words of programmable ROM (pROM) which consists of a micro-diagnostic program. This program must be run with both the CPU and disc drive disconnected from the controller and the error correction PCA removed from the controller. The diagnostic pROM program checks the microprocessor and device controller PCA's. If a hardware failure is detected, the diagnostic program halts. The error condition can then be determined by correlating the address displayed in the RAR LED's with a listing of the micro-diagnostic. If no hardware failures are detected, the diagnostic program cycles endlessly and the RAR LED's appear blurred.

5-14. ROM TEST MODE. When the TEST ROM button is pressed, each word of ROM is added together and the 24-bit result is displayed in the LED's. By comparing this ROM check word to the correct word for the ROM, a go-no-go indication for the entire ROM may be obtained.

5-15. SINGLE CPU INSTRUCTION MODE. This type of operation may be used when the controller is connected to a disc drive, but not to a CPU. The CSU operator may enter into the CSU, in binary, one CPU level instruction to the controller (e.g., SEEK, SET FILE MASK, VERIFY, ...etc.). Pressing CMRDY and DTRDY on the CSU then causes the controller to execute the instruction. If an instruction such as REQUEST STATUS or READ tries to cause data to be returned to a CPU, the last word that the controller tries to send is displayed in the CSU LED's. Proper disc drive and controller operation can thus be verified using this mode of operation.

5-16. PREVENTIVE MAINTENANCE

There are no extensive procedures required for maintaining the controller. Cleaning and inspection should be done annually. The 5-volt power supplies should be monitored at the same time to ensure that the output voltages are within the accepted tolerances.

5-17. TROUBLESHOOTING

The troubleshooting philosophy for the controller is to check the power input, power supplies for the PCA's, make a visual inspection of all cables and connectors, and change one of the four PCA's if the problem is not found in one of the previous areas. An appropriate diagnostic can be run if the controller is connected to an HP 2000 or 3000 Computer System. Refer to the applicable subsystem manual for operation and interpretation of the diagnostic. Figure 5-8 is a troubleshooting flowchart which presents a sequential procedure for checking power input and the PCA power supplies.

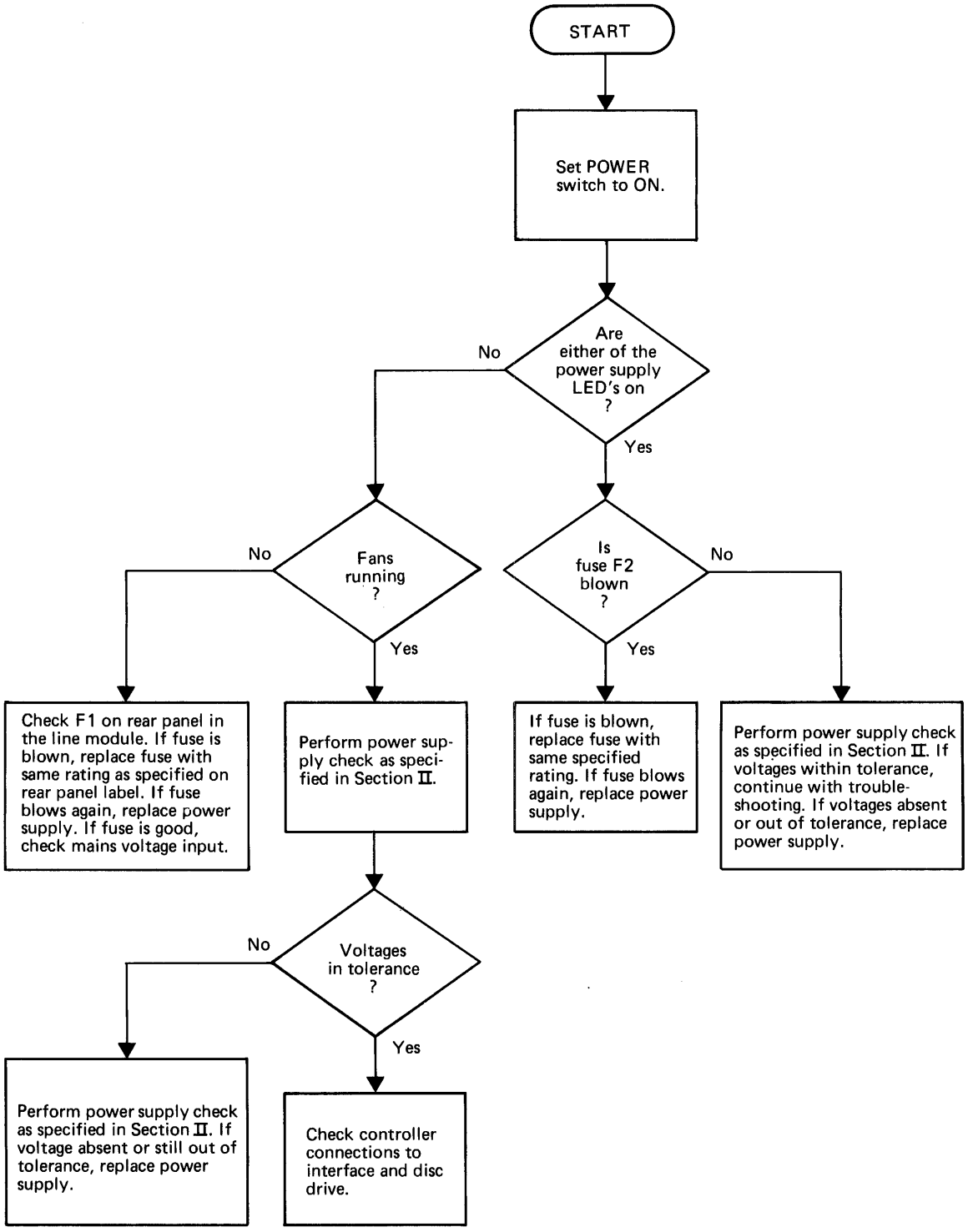


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Figure 5-8. Troubleshooting Flowchart

Section VI

REPLACEABLE PARTS

6-1. CONTROLLER REPLACEABLE PARTS

This section provides a listing of field-replaceable parts and an illustrated parts breakdown of the HP 13037A Disc Controller. Component parts of printed-circuit assemblies (PCA's) are not included since these parts are considered replaceable only at the factory or a depot.

Figures 6-1, 6-2, and 6-3 illustrate the field-replaceable parts of the HP 13037 Disc Controller. The replaceable parts are indexed in each figure and are referenced to the exploded view in a table located on the apron of the foldout drawing. Each table lists the index number, quantity required, description, and HP part number of its associated illustrated parts.

An individual PCA can be ordered by the following part number:

Microprocessor, part no. 13037-60001.

Device Controller, part no. 13037-60002.

Error Correction, part no. 13037-60004.

Power Regulator, part no. 13037-60018.

6-2. ORDERING INFORMATION

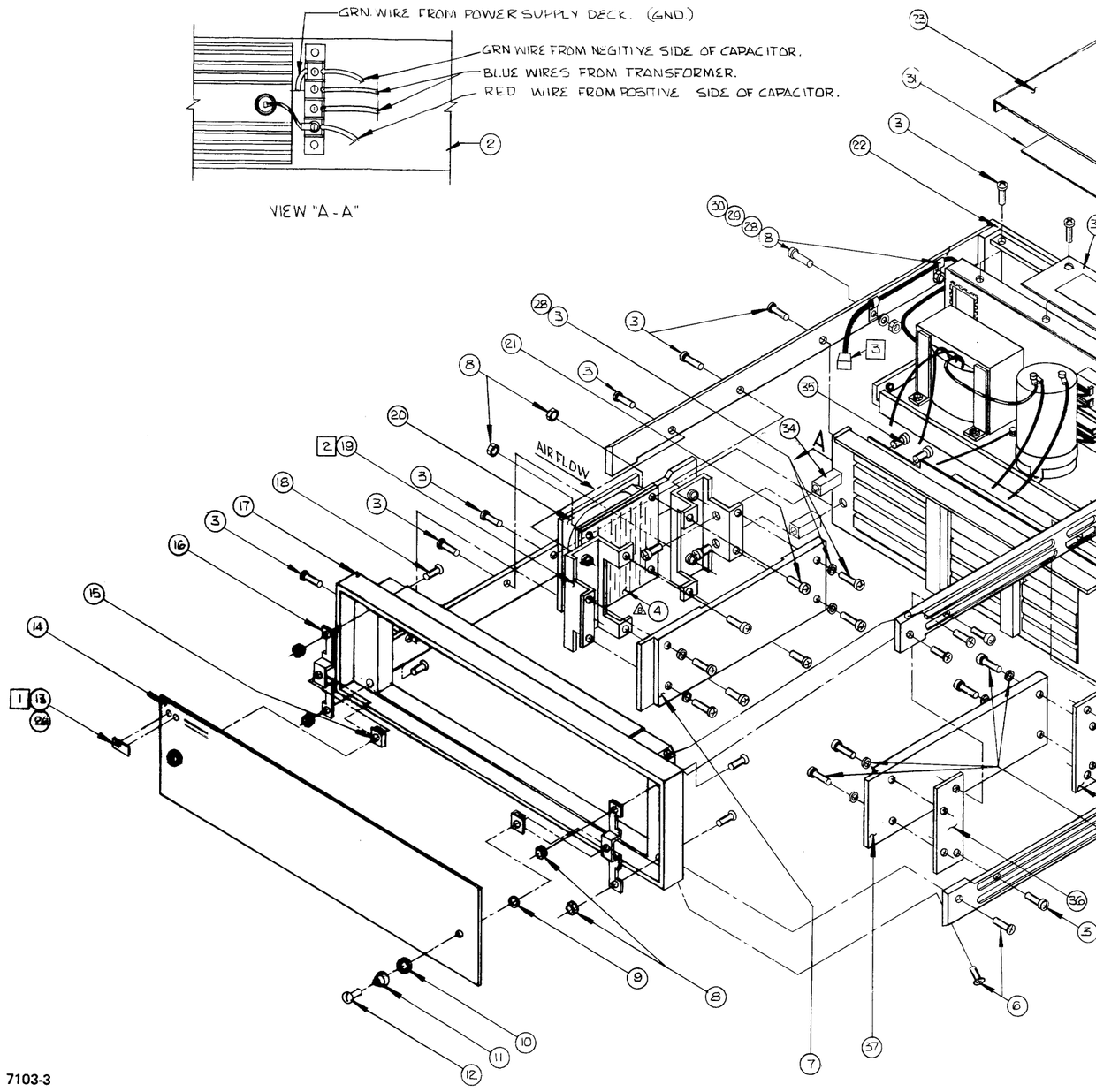
To order replaceable parts, address the order to the local Hewlett-Packard Sales and Service Office listed at the end of this manual. The following information should be included in the order for each replaceable part:

a. Complete model number (including options and accessories) and serial number.

b. Hewlett-Packard part number for each part.

c. Complete description for each part as provided in the replaceable parts lists.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.
37	1	GUIDE P.C. RIGHT	13037-20004
36	1	PLATE FRONT	13037-00008
35	4	SCREW 10-32 x .438	2680-0053
34	2	STAND OFF	0380-0495
33	1	LABEL WARNING	7120-3185
32	1	COVER AC LINE	13037-00009
31	1	INSULATOR	0340-0541
30	2	SCREW PH 6-32 x 1/2 LG.	2360-0201
29	2	CABLE CLAMP	1400-0440
28	20	WASHER FLAT #6	3050-0228
27	.80FT	GROMMENT-CHANNEL	0400-0082
26	A/R	ADHESIVE	0470-0010
25	4	CORNER-STRUT	5020-8838
24	2	COVER-SIDE	02105-00008
23	2	COVER-TOP FULL MOD.	5020-9830
22	1	FRAME-REAR 5.25 HIGH	5020-8804
21	4	SCREW PH 6-32 x .750	2360-0205
20	1	FAN TUBEAXIAL	3160-0224
19	2	BRACKET-P.C. GUIDE & FAN	13037-00001
18	4	SCREW FH 82° 6-32 x .500	2360-0202
17	1	FRAME FRONT 5.25 HIGH	5020-7337
16	2	BRACKET-FRONT PANEL	02105-00012
15	2	RECEPTACLE	1390-0091
14	1	PANEL-FRONT	13037-00004
13	1	LOGO HP	7120-1254
12	2	STUD	1390-0080
11	2	SPRING CONICAL	1390-0096
10	2	WASHER-CUP	1390-0071
9	2	RETAINER	1390-0257
8	10	NUT 6-32	2420-0001
7	1	GUIDE LEFT P.C. BD	13037-20002
6	16	SCREW FH 100° 8-32 x .250	2510-0098
5	1	PLATE-PC GUIDE REAR	13037-00002
4	1	GUARD; FAN	5000-8015
3	33	SCREW PH 6-32 x .375	2360-0117
2	1	ASSY REGULATOR/BACKPLANE	SEE FIGURE 6-2
1	1	ASSY DECK/REAR	SEE FIGURE 6-3



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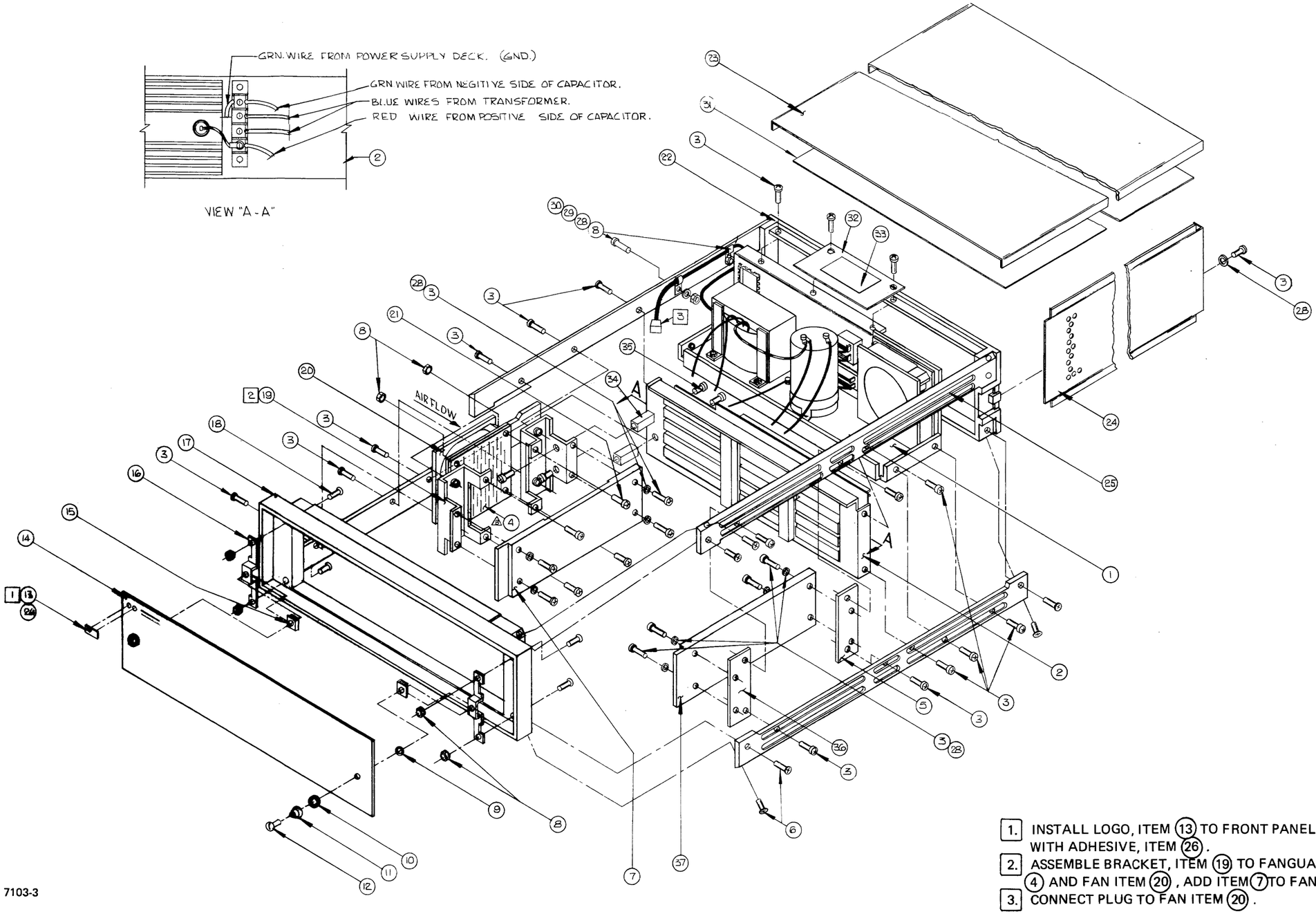


1. INSTALL LOGO, ITEM (13) TO FRONT PANEL, ITEM (14) WITH ADHESIVE, ITEM (26).
2. ASSEMBLE BRACKET, ITEM (19) TO FANGUARD ITEM (4) AND FAN ITEM (20), ADD ITEM (7) TO FAN ASSEMBLY.
3. CONNECT PLUG TO FAN ITEM (20).

Figure 6-1. Controller Main Frame Assembly

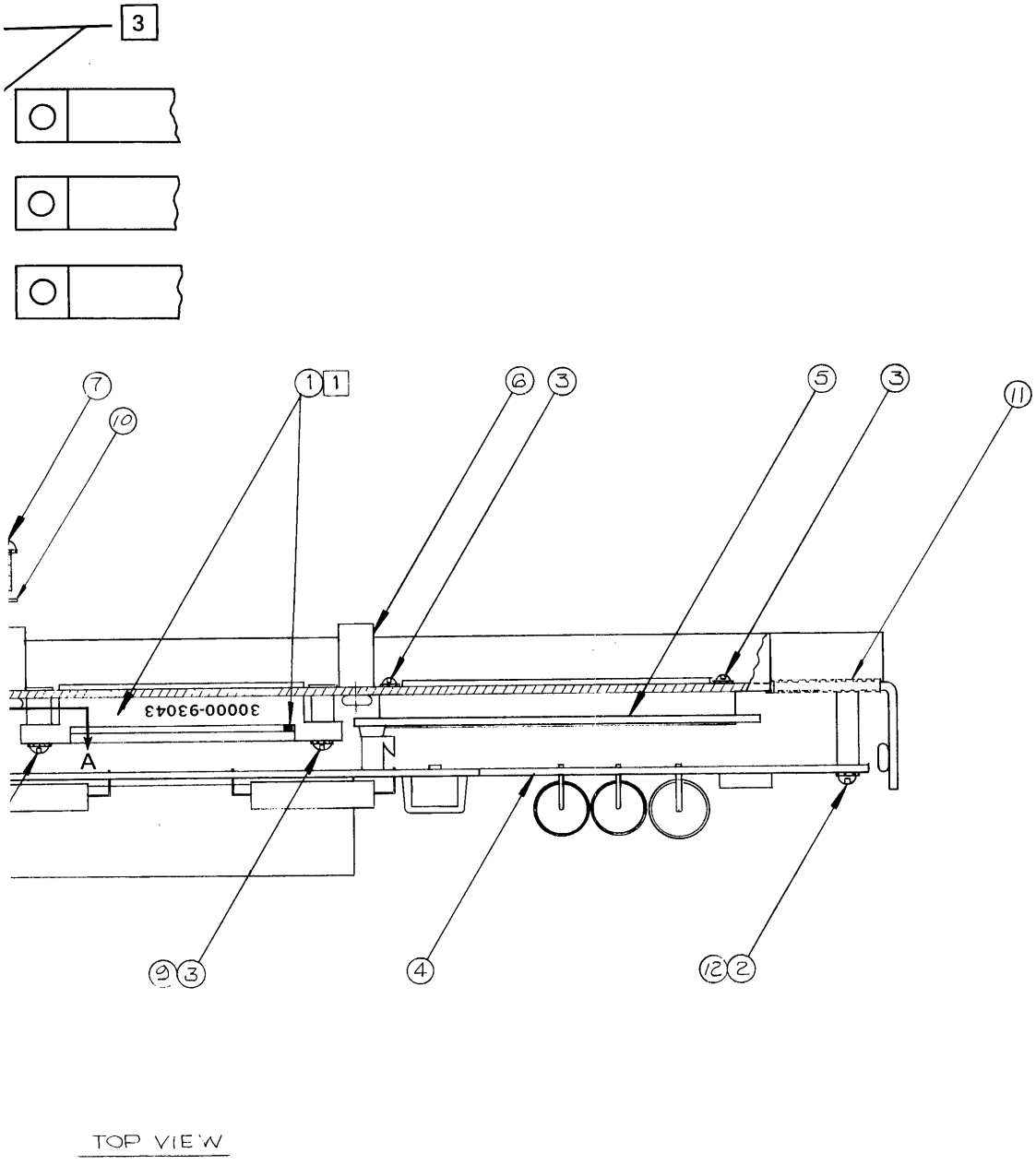
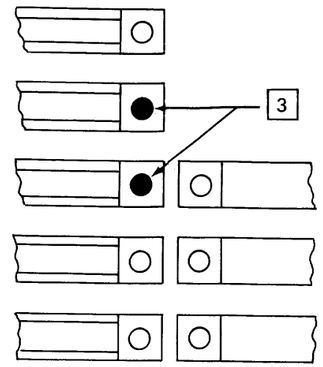
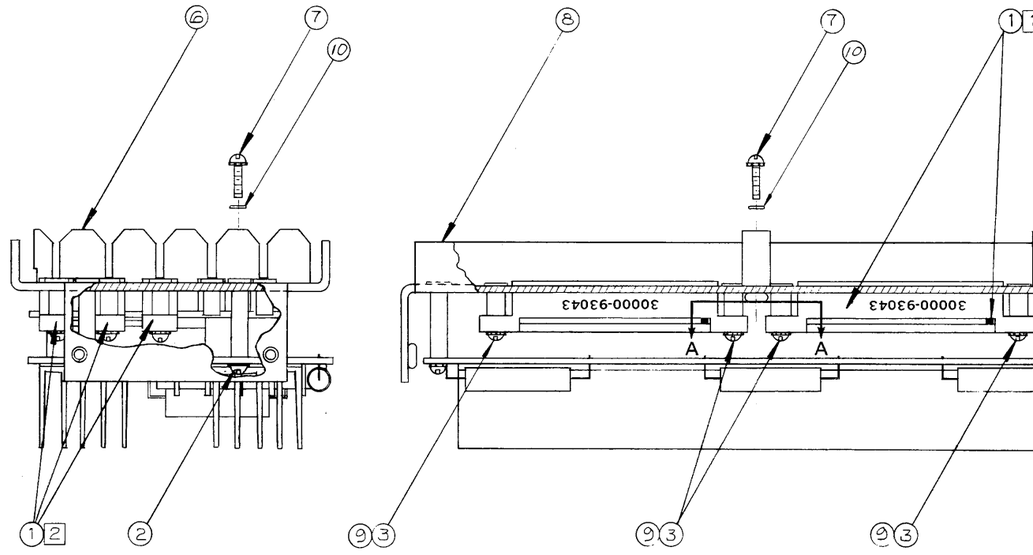


Figure 6-2. Regulator and Backplane Assembly

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.
12	4	SPLITLOCK #6	2190-0006
11	.15 FT	GROMMET CHANNEL	0400-0082
10	4	WASHER FLAT #6	3050-0228
9	20	WASHER FLAT #4	3050-0229
8	1	FRAME BACKPLANE	13037-00003
7	4	SCREW 6-32×.750	2360-0125
6	2	GUIDE P.C. BD. REAR	13037-20003
5	1	ASSY P.C. INTERCONN. BD.	13037-60020
4	1	ASSY P.C. REGULATOR BD.	13037-60018
3	30	SCREW 4-40×.375 W/L	2200-0107
2	4	SCREW 6-32×.250	2360-0195
1	2	CABLE RIBBON-3 CONN.	30000-93043

VIEW A-A



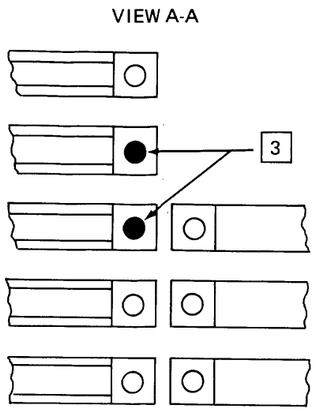


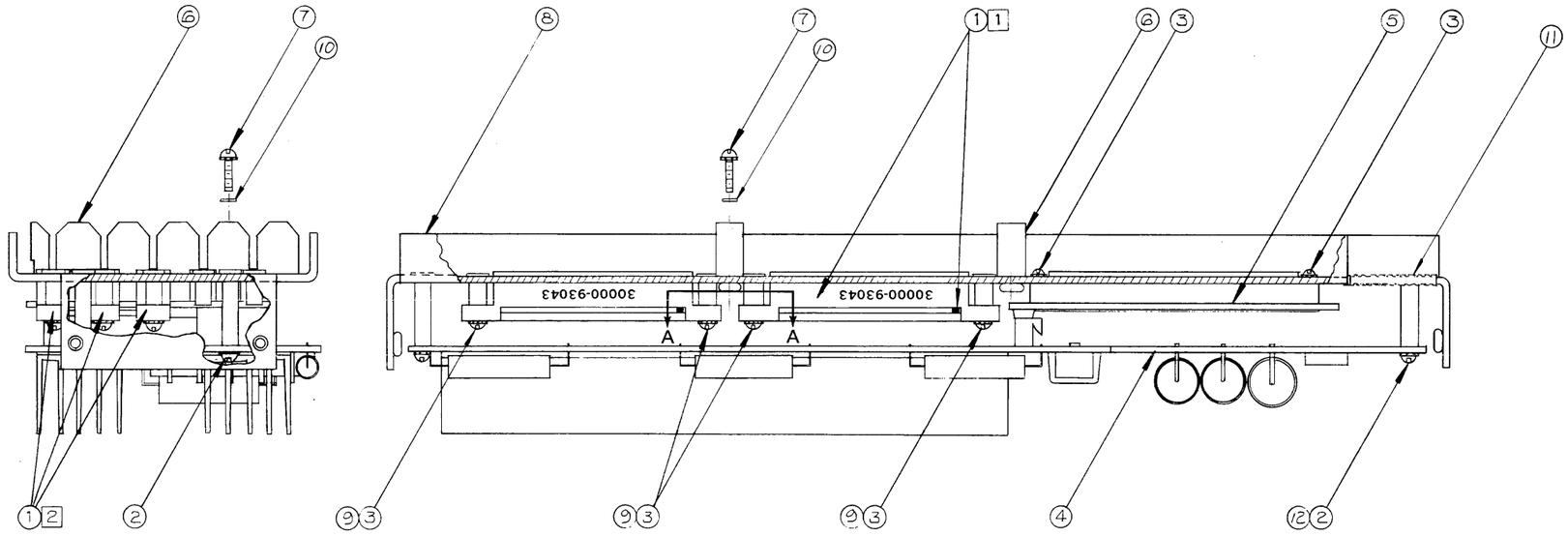
7103-4

TOP VIEW

1. RIBBON CONN. ITEM (1), TO BE INSTALLED WITH RED CABLE MARKING AS SHOWN.
2. MOUNT RIBBON CONN. ITEM (1), TO FIRST 3 POSITIONS OF FRAME BACKPLANE ITEM (8), AS SHOWN.
3. THESE TWO SCREWS MUST BE NYLON WHEN USING 13037-60020 DATE CODED B-1520-22. (NYLON SCREWS PREVENT SHORTING THE +5 VOLT SUPPLY TO GROUND)

CK #6	2190-0006
T CHANNEL	0400-0082
FLAT #6	3050-0228
FLAT #4	3050-0229
BACKPLANE	13037-00003
6-32 x .750	2360-0125
P.C. BD. REAR	13037-20003
. INTERCONN. BD.	13037-60020
. REGULATOR BD.	13037-60018
4-40 x .375 W/L	2200-0107
6-32 x .250	2360-0195
21BBON-3 CONN.	30000-93043
ATERIAL-DESCRIPTION	MAT'L-PART NO.



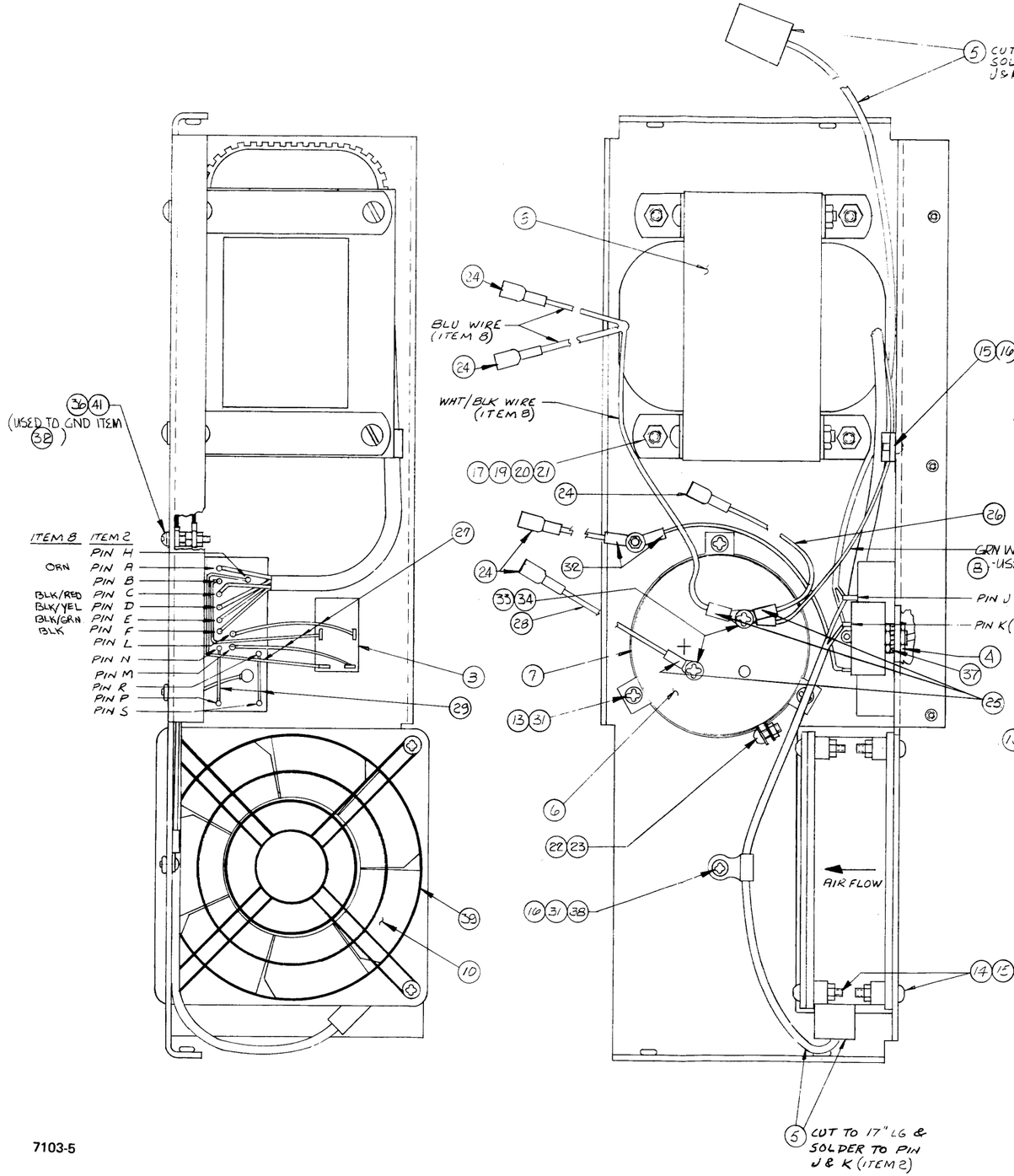


7103-4

1. RIBBON CONN. ITEM (1), TO BE INSTALLED WITH RED CABLE MARKING AS SHOWN.
2. MOUNT RIBBON CONN. ITEM (1), TO FIRST 3 POSITIONS OF FRAME BACKPLANE ITEM (8), AS SHOWN.
3. THESE TWO SCREWS MUST BE NYLON WHEN USING 13037-60020 DATE CODED B-1520-22. (NYLON SCREWS PREVENT SHORTING THE +5 VOLT SUPPLY TO GROUND)

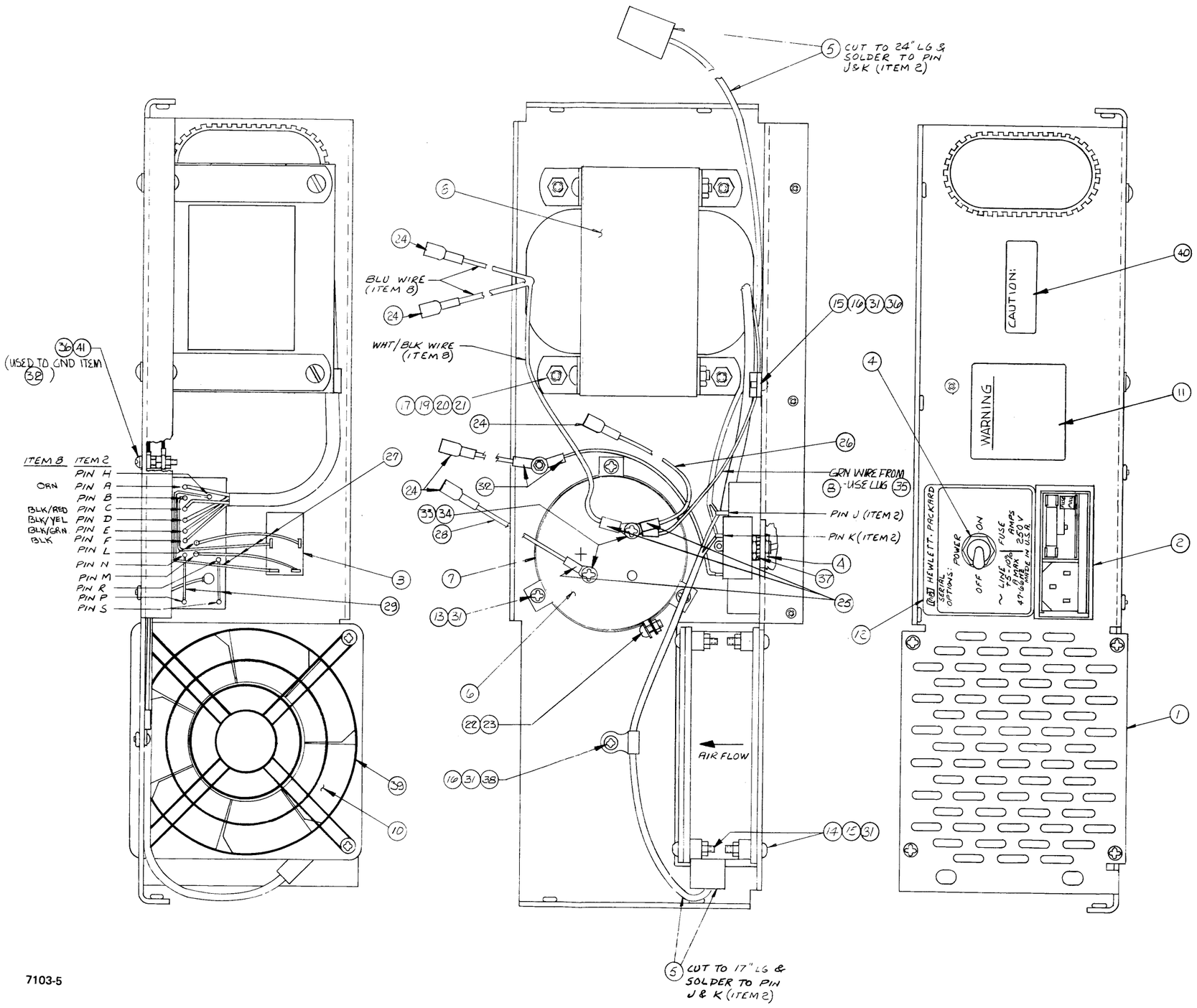
Figure 6-2. Regulator and Backplane Assembly

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.
41	3	NUT 6-32 HEX	2420-0002
40	1	LABEL "OPR. WARN"	7120-3528
39	1	GUARD FAN	3160-0099
38	1	SCREW PH 6-32x1/2 W/L	2360-0121
37	1	INT. LOCK WASH 1/2"	2190-0068
36	2	SCREW PH 6-32x1/2	2360-0201
35	1	#10 LUG-CRIMP - RED	0362-0333
34	2	#10 INT LOCK	2190-0011
33	2	SCREW PH #10-32 x 3/8	2680-0099
32	2	LUG-CRIMP YEL RING	0362-0330
31	8	#6 FLAT WASH.	3050-0228
30	1	WIRE - YEL/GRN 6" LG	8150-2624
29	2	WIRE-18GA, BLK, 2" LG	8150-2890
28	1	WIRE-14GA, RED, 7" LG	8150-2464
27	4	WIRE-18GA, BLK, 4" LG	8150-2890
26	1	WIRE-14GA, GRN, 7" LG	8150-2466
25	3	LUG-CRIMP	0362-0253
24	5	LUG-CRIMP QUICK DISC. YEL	0362-0305
23	1	NUT #8-32	2580-0003
22	1	SCREW-PAN HD #8-32 x 9/16	2510-0107
21	4	WASHER #10	3050-0019
20	4	NUT 10-32	2740-0002
19	4	SCREW-HEX HD #10-32 x 1/2" LG	0570-0124
18	1	WIRE 14GA, GRN 6" LG	8150-2466
17	4	SPLIT-LOCK	2190-0043
16	2	CLAMP - CABLE	1400-0440
15	5	NUT #6-32	2420-0001
14	4	SCREW-PAN HD #6-32 x 3/4" LG	2360-0205
13	4	SCREW PH. W/L #6-32 x 5/16 LG	2360-0115
12	1	LABEL INFORMATION	7120-4402
11	1	LABEL INFORMATION	7120-4369
10	1	FAN TUBEAXIAL	3160-0224
9	1	INSULATION 7.5" LG	0400-0082
8	1	TRANSFORMER	9100-3814
7	1	CLAMP 3" DIA.	0180-1958
6	1	CAPACITOR	0180-2393
5	2	CORD	8120-1478
4	2	NUT - 15/32 -32 HEX.	2950-0035
3	1	SWITCH	3101-0646
2	1	LINE MODULE	5060-9422
1	1	CHASSIS - POWER SUPPLY	13037-00006



7103-5

HEX	2420-0002
WARN'	7120-3528
N	3160-0099
-32x1/2 W/L	2360-0121
WASH 1/2"	2190-0068
6-32x1/2	2360-0201
CRIMP - RED	0360-0333
OCK	2190-0011
ID-32 x 3/8	2680-0099
YEL RING	0362-0330
ASH.	3050-0228
RN 6" LG	8150-2624
BLK, 2" LG	8150-2890
RED, 7" LG	8150-2464
BLK, 4" LG	8150-2890
GRN, 7" LG	8150-2466
	0362-0253
CK DKL. YEL	0362-0305
	2580-0003
D#8-32x9/16	2510-0107
	3050-0019
	2740-0002
#10-32x1/2" LG	0570-0124
RN 6" LG	8150-2466
	2190-0043
LE	1400-0440
	2420-0001
#6-32x3/4" LG	2360-0205
#6-32x5/16 LG	2360-0115
RMATION	7120-4402
RMATION	7120-4369
AL	3160-0224
7.5" LG	0400-0082
R	9100-3814
A.	0180-1958
	0180-2393
	3120-1478
HEX.	2950-0035
	3101-0646
E	5060-9402
ER SUPPLY	13037-00006
ESCRIPTION	MAT'L-PART NO.



7103-5

Figure 6-3. Rear Deck Assembly