HEWLETT PACKARD

HP 64783A/B Emulators for Motorola 68040, 68EC040, and 68LC040 Processors

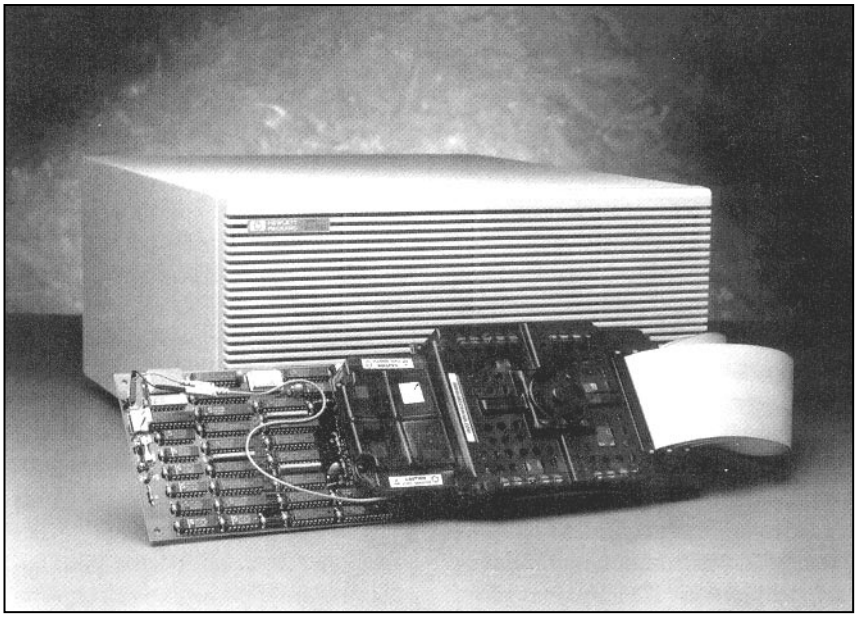
Technical Data

Design, debug, and integrate real-time embedded systems

Description

The HP 64783A/B active probe emulators support Motorola 68040 microprocessors from 16.7 to 40 MHz operation. These emulators offer the measurement capabilities that include interpreted displays of on-chip registers, nonintrusive display of emulation memory, deep trace analyzer, and hardware break events. In addition, hardware assisted software breakpoints allow setting of breakpoints in target ROM space to simplify the debugging of ROM. Foreground and background monitors are included to make it easier to accommodate various targets.

Designers using the Motorola 32-bit 68040 microprocessor are assured of a full line of support with modular emulation tools and software support on a range of design platforms. The emulator is an integrated part of a total solution for the design of your 68040 embedded system. HP has integrated code-development, debug, emulation, software performance analysis, and software test verification into a comprehensive package that will meet your embedded design requirements. You have the choice of selecting the entire development package or only the parts that you need at a specific time.



For PC hosted embedded development, a Real-Time C Debugger* user interface combines the ease of use of a full MS Windows user interface with HP 64700's transparent, real-time emulation. This combination provides an unmatched ability to debug embedded C programs at the source level, while your target runs at full speed.

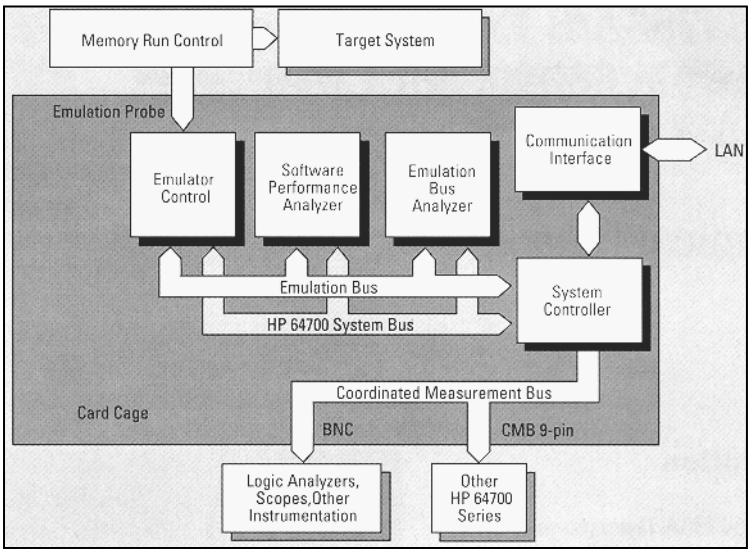
Workstation hosted embedded development is supported with an X/Motif based Embedded Debug Environment which is an integrated suite of tools that span the entire software development process. The environment provides easy-to-use measurement capabilities ranging from real-time, nonintrusive analysis to high-level, C and C++ source code debugging. In addition, the Embedded Debug Environment automatically integrates with the HP Softbench framework to provide a complete CASE environment for embedded software development

MOTOROLA DEVELOPER PROGRAM

HP is a Platinum member of the Motorola Developer Program.

Features

- 33 MHz (HP 64783A) or 40MHz (HP 64783B) active probe emulators
- Supports burst and synchronous mode in target memory and emulation memory
- Supports 68040 features like DMA cycles, cache copyback, and bus snooping
- Symbolic support (with PC and workstation interfaces)
- Supports D~EMMU functions
- Supports zero wait states out of target memory through 25 MHz. From 25 - 40 MHz, one wait state is required (Table 1 pg 6)
- Supports zero wait states out of HP 64172A/B emulation memory through 25 MHz and one wait state from 25 up to 40 MHz (Table 1 pg 6)
- Supports one wait state out of HP 64173A* emulation memory from 16.7 to 40 MHz (Table 1 pg 6)
- Supports 68360 companion mode
- Selective cache inhibit for arbitrary blocks of memory (256 byte resolution)
- Support for IEEE-695, HP-OMF, Motorola S-Records, and Extended Tek HEX file formats (symbols supported with IEEE-695 and HP-OMF)
- Unlimited software execution breakpoints
- Software ROM breakpoints
- Eight hardware execution breakpoints
- Eight real-time hardware break events
- Simulated I/0 (on workstations)
- Multiprocessor emulation
  - Synchronous start of up to 32 emulators
  - Cross triggering from another emulator, logic analyzer, or oscilloscope
- Integrated C language system available
- 36-inch probe cable terminating an active probe



HP 64700 Series development tools include an emulator, an emulation bus analyzer, and an optional software performance analyzer.

Emulation Bus Analyzer

- 80 channels available with trace buffer depths of 1K, SK, 64K, or 256K
- Postprocessed SW based dequeued trace with symbols and source lines
- Eight events, each consisting of address, status, and data comparators
- Events may be sequenced 8 levels deep; can be used for complex trigger qualification/selective store
- Timing and state counts
- Prestore capability

Emulation Memory

- 256 Kbyte, 512 Kbyte, 1 Mbyte, 1.25 Mbyte, 2 Mbyte, (4 Mbyte, 4.25 Mbyte, 5 Mbyte, and 8 Mbyte) memory configurations*
- Mapping resolution of 256 bytes

Card Cage

The cardcage is the basis for modular emulators and analyzers. It can be disassembled and reassembled easily for cost-saving reconfiguration to support 8-, 16-, and 32-bit processors.

The cardcage contains a combination RS-232-C/RS-422 serial port with a standard 25-pin serial connector. RS-422 can be programmed to operate at rates up to 460 KB.

Networking

In many embedded design environments, it is not possible for each team member to have a target system and an emulator. This makes it essential to have remote access from a networked host. The HP 64700 series emulators offer a LAN connection so that you are able to share a central emulator and target from either a PC or workstation. Not only does the LAN capability allow team members to share a common emulator and data base, but you also have rapid file transfers at rates of up to six megabytes per minute for increased productivity. The cardcage connects to all popular Ethernet/803.2 networks through a 10Base2 ThinLAN BNC connector or a 15-pin AUI attachment unit interface. TCP/IP protocols, LAN gateways, and ARPA/Berkeley standards are supported.

Emulation Bus Analysis

Emulation bus analysis provides real-time, nonintrusive operation along with extensive triggering, tracing and qualification features. Analysis features offer selective tracing, time-tagging, prestore, and a selection of trace depths of 1K, 8K, 64K, or 256K. These comprehensive resources combine to solve both simple and complex problems.

Real-time, nonintrusive analysis is achieved through dual-bus architecture. This allows traces to be set up and reviewed without breaking processor execution. Selective tracing of microprocessor code flow, without breaking execution, is a major strength of the HP 64700 Series emulators and analyzers.

Up to eight hardware breakpoint resources, each consisting of address, data, and status event comparators, can be combined in sequential trace specifications, using "find A, followed by B..." constructs up to eight levels deep. A range comparator can be applied to address or data events at any one of these levels. The analyzer will trigger on and store all subsequent execution or store only specified execution information.

Precise time tagging of events helps you identify discrepancies in code execution times. Each event is logged into the analyzer with an execution time. Bus cycle, instruction, and module duration times can be measured at full processor speeds.

Prestore assists you in pinpointing possible problem areas in your code. For example, prestore determines which of several different functions is accessing a variable and is responsible for corrupting it.

Real-time Emulation

The HP 64783A/B are active probe emulators that contain the microprocessor, emulation monitor, run-control circuits, and up to 8 Mbytes of emulation memory. Each emulator includes foreground and background monitors. The foreground monitor is used for interrupt-sensitive systems or for customizing the monitor to the target system. A foreground monitor can respond to target system interrupts while in a monitor idle loop. The background monitor uses a separate monitor memory space so that no target address space is used by the monitor.

Extensive breakpoint capabilities let you define where to stop the execution of code. Software breakpoints can be set up in the emulator, allowing execution to be halted at an instruction point.

Hardware breakpoints allow setting of breakpoints in ROM. Real-time hardware break events increase the flexibility and power of this feature, extending functionality to include stopping at processor address, data, status points, or a combination of all three.

Flexible Memory Configuration

Memory modules are used for emulation memory. Two slots are available on the active probe, allowing you to plug in the amount of memory you need up to eight megabytes. If you initially order less than the maximum amount, you can easily expand your system by adding the appropriate module(s). Modules for 256 Kbytes (HP 64172A), 1 Mbyte (HP 64172B), and 4 Mbytes (HP 64173A*) are available.

In addition to the memory modules, four kilobytes of dual-ported emulation RAM is available when the background monitor is used. This dual-ported memory allows you to display and modify critical program variables without halting the target system.

Robust Symbolic Support

Symbolic debugging is available when using the PC hosted real-time C debugger, debugger/emulator, and workstation hosted software tools. Symbolic debugging clarifies trace list interpretation by allowing you to see program symbols in the trace list. This facilitates quick identification of problems involving the interaction of software and hardware. You also can use symbols in emulation commands and expressions to simplify command entries and user interaction.

Software Performance Analysis

Real-time software performance analysis enables you to tune and verify the time-critical aspects of your design. These capabilities are provided at both the C source and assembly language levels. Through automated one-key set up, this system quickly identifies code bottlenecks and gathers statistics and timing information that aid in solving time-critical problems.

These easy-to-use, performance measurements are possible by using marker technology for accurate function and interval duration as well as activity measurements. Markers are used with the 68040 processor because of its deep prefetch capability. Markers are write statements that are placed at the start and end of each function. When using markers the software performance analyzer automatically defines both the address range of the function and the start and end addresses of the markers.

One advantage of markers is that you can turn on the microprocessor instruction cache and data cache (if write statements can write through the cache) and the software performance analyzer can make valid performance measurements. With the instruction cache enabled, your program runs in a manner that better reflects the performance of your final product. The markers may be compiled manually or automatically by using the marker preprocessor which is supported on HP and MRI compilers.

The software performance analyzer is an optional card that plugs into the card cage. It operates with HP 9000 Series 300/400/700 workstations and Sun SPARCstations.

Companion Mode

The HP 64783A/B emulators support the Motorola 68360 companion mode through the HP interface software for workstations and PCs. Motorola designed the 68360 processor to have a glueless interface with the 68040 where it controls the peripheral registers of the 68360. The extensive control and measurement capabilities of the HP 64783A/B emulators make them ideal for supporting 68360 peripheral registers.

Key features of 68040 emulation companion mode support include:

- Peripheral register contents displayed with English descriptions of bit field values.
- Graphical register modification system speeds development
- Automatic generation of host code for configuring 68360 SIM 60 unit makes easy system boot up
- Save-and-restore peripheral register settings to files make checkpointing and testing easy
- Supports one to 31 companion mode 68360 processors
- Built-in help system gets embedded system development started fast

Workstation Hosted Environment

The HP embedded debug environment is a group of integrated tools that assist you during software development. These tools include the real-time software performance analyzer, emulator/analyzer user interface, debugger/emulator, debugger/simulator, advanced cross language system, HP branch validator, and RTOS measurement tools.

The emulator/analyzer tool gives you the ability to perform trace analysis, set breakpoints, and establish emulator configuration parameters. In addition, the graphical interface tool is integrated with the embedded debug environment, which coordinates high-level software debugging with low-level microprocessor run control.

The HP debugger/emulator and debugger/simulator share a common user interface for ease of learning. Both interfaces support data types, stack backtrace, and stack resident local variables. The debugger/emulator also works with your code in real time and allows you to set breakpoints directly without having to switch to the emulator/analyzer.

The advanced cross language system includes HP's ANSI C compiler, assembler, and linker. These tools are integrated with the HP debug environment to provide a comprehensive array of features and functions that address embedded development needs. For example, the combination of the cross language system and debug environment allows you to display memory and symbolic trace information with overlaid C source. This allows you to view your target code from both a high-and low-level perspective to aid in debugging complex problems.

HP Branch Validator verifies software test effectiveness on complete hardware/software systems. This tool provides an easy-to-use environment for branch analysis which supports rapid iteration of the compile-test-analyze loop. Comprehensive reports, resulting from the branch validator sessions, provide detailed feedback on the execution of test suites.

The real-time operating system measurement tools allow you to transparently trace operating system task flow, service call activity, and measure system performance on running systems. Real-time operating systems supported with these tools include pSOS+, VRTX32, and user-developed operating systems.

The HP debug environment supports many popular language tools from MRI and Intermetrics, as well as the HP advanced cross-language system of compilers, assemblers, and linkers. The debug environment also operates within the optional HP SoftBench environment, which brings advanced CASE tools and techniques to the realm of embedded software design.

PC Hosted Environment

The Real-time C Debugger (HP B3629A*) is an MS-Window-based, graphical user interface for HP 64700 emulators. It provides a mouse-driven method of controlling emulator functions, making measurements of target system activity and controlling the state of a target system.

The Real-time C Debugger provides several windows and dialogs to access and modify C variables, memory, and I/O ports.

If you do not need a graphical user interface, there is another PC user interface (HP 64783S Opt 006) that provides real-time symbolic assembly-level debug capabilities. It runs on PC/AT-class computers as a DOS application and communicates with the emulator over RS-232-C or RS-422.

Terminal mode operation

A firmware-resident ASCII terminal interface is embedded in the emulator, supplying commands for all emulation and analysis features. Commands are ASCII strings; file transfers using industry-standard formats are accepted. Since a terminal can access these commands, host independence is realized.

Specifications

Processor Compatibility

Model 64783A/B:
Motorola 68040, 68EC040, 68LC040
Note: 68EC040 targets will try to run FPU instructions if they exist in user code

Electrical

Minimum clock speed:
HP 64783A, 16.67 MHz; HP 64783B, 20 MHz

Power: 1.8 A max from target system, all other power supplied by card cage.

Environmental

Temperature: operating, 0 to +40° C (+32° to +104°F; nonoperating, -40° to +70°C (-40° to +158° F)

Altitude: operating/nonoperating 4600 m (15,000 ft)

Regulatory compliance: when installed in HP 64700 card cage.

Electromagnetic interference:
CISPR 11:1990/EN 55011 (1991): group 1 class A
IEC 802-2:1991/EN 50082-1 (1992): 4 kV CD, 8 kV AD
IEC 801-3:1984/EN 50082-1 (1992): 3 V/m, 800% modulation, 26 MHz-1000 MHz
IEC 801-4:1988/EN 50082-1 (1992): 0.5 kV signal lines, 1 kV power lines

Safety: self-certified to UL 1244, IEC 348/HD 401 SI, CSA-C22.2 no. 231 Series-M89

Physical

Cable length: probe to card cage approximately 914 mm (36 in.)

Probe dimensions:

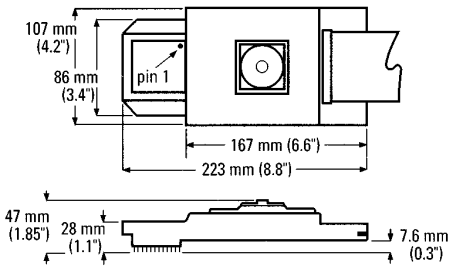


Table 1. Clock Speed/Wait States

Emulator Model No.	Clock Speed MHz	Memory Wait States Target	Memory Wait States Emulation	**Emulation Memory Model No.
64783A	16-25	0	0	64172A/B
64783A	25-33	1	1	64172A/B
64783A	16-25	0	1	64173A
64783A	25-33	1	1	64173A
64783B	20-25	0	0	64172A/B
64783B	25-40	1	1	64172A/B
64783B	20-25	0	1	64173A*
64783B	25-40	1	1	64173A

***When mixing HP 64172A/B and 64173A memory modules, emulation memory wait states for the HP 64173A module apply.*

Emulator DC Electrical Specifications (68040/EC040/LC040):
(V_{CC} = 5.0 Vdc±5%)

Characteristic	Symbol	Min	Max	Unit
Input High Voltage	V_{IH}	2.0	V_{CC}	V
Input Low Voltage	V_{IL}	GND	0.8	V
Undershoot		-	0.5	V
Input Leakage Current @ 0.5/2.4 V				
AVEC, BCLK, BG, CDIS, MDIS, IPLx, PCLK, RSTI, SCx	I_{IL}	-250	-	µA
TBI, TLNx, TCI, TCK, TEA	I_{IH}	-	25	µA
Hi-Z (Off-State) leakage Current @ 0.5/2.4 V	I_{TSI}			
An, CIOUT, Dn, LOCK, LOCKE, SIZx, TDO, TMx, TLNx, TTx, UPAx		-50	50	µA
BB, R/W, TIP, TS		-100	100	µA
TA		-200	200	µA
Output High Voltage	V_{OH}			
I_{OH}=-32 mA:				
An, Dn, SIZx, TTx, UPAx, LOCK, LOCKE, TLNx, CIOUT, TMx, PSTx, RSTO, BR, MI, BG, reset flying lead		2.0	-	V
I_{OH}=-3.2 mA:				
R/W, TS, TIP, BB, TA, IPEND		2.4	-	V
Output Low Voltage	V_{OL}			
I_{OL} = 64 mA:				
An, Dn, SIZx, TTx, UPAx, LOCK, LOCKE, TLNx, CIOUT, TMx, PSTx, RSTO, BR, MI, BG, reset flying lead		-	0.55	V
I_{OL} = 24 mA:				
R/W, TS, TIP, BB, TA, IPEND		-	0.5	V
Capacitance	C_{in}	-	25	pF
V_{in} = 0 V, f = 1 MHz				
Supply Current	I_{CC}			
f = 25 MHz		-	1.4	A
f = 33 MHz		-	1.8	A

Note: BCLK and PCLK have additional input current and capacitive loading because of terminations. The numbers given in the HP 64783A/B DC electrical specifications table do not include the terminations.The HP 64783A/B emulators run in large buffer mode.

Clock AC Timing Specifications:

Num.	Characteristic	25 MHz Min	25 MHz Max	33 MHz Min	33 MHz Max	40 MHz Min	40 MHz Max	Unit
	Frequency of Operation	16.67	25	16.67	33	20	40	MHz
1	PCLK Cycle Time	20	30	15	30	12.5	25	ns
2	PCLK Rise Time	-	1.7	-	1.7	-	1.5	ns
3	PCLK Fall Time	-	1.6	-	1.6	-	1.5	ns
4	PCLK Duty Cycle Measured at 1.5 V	47.50	52.50	46.67	53.33	46	54	%
4a[1]	PCLK Pulse Width High Measured at 1.5 V	9.50	10.50	7	8	5.75	6.75	ns
4b[1]	PCLK Pulse Width Low Measured at 1.5 V	9.50	10.50	7	8	5.75	6.75	ns
5	BLCK Cycle Time	40	60	30	60	25	50	ns
6,7	BCLK Rise and Fall Time	-	4	-	3	-	3	ns
8	BCLK Duty Cycle Measured at 1.5 V	40	60	40	60	40	60	%
8a[1]	BCLK Pulse Width High Measured at 1.5 V	16	24	12	18	10	15	ns
8b[1]	BCLK Pulse Width Low Measured at 1.5 V	16	24	12	18	10	15	ns
9	PCLK, BCLK Frequency Stability	-	1000	-	1000	-	1000	ppm
10	PCLK to BCLK Skew	-	n/a	-	n/a	-	n/a	ns

Note: Specification values at maximum frequency of operation

Output AC Timing Specifications:

Num.	Characteristic	25 MHz[1] Min	25 MHz[1] Max	33 MHz[1] Min	33 MHz[1] Max	40MHz[1] Min	40MHz[1] Max	Unit
11	BCLK to Address CIOUT, LOCK, LOCKE, R/W, SIZx, TLNx, . TMx,TTx, UPAx Valid	9	25	6.5	22.5	5.25	21	ns
12	BCLK to Output Invalid (Output Hold)	9	-	6.5	-	5.25	-	ns
13	BCLK to TS Valid	9	25	6.5	22.5	5.25	21	ns
14	BCLK to TIP Valid	9	25	6.5	22.5	5.25	22	ns
18	BCLK to Data Out Valid	9	27	6.5	24.5	5.25	23	ns
19	BCLK to Data Out Invalid (Output Hold)	9	-	6.5	-	5.25	-	ns
20	BCLK to Output Low Impedance	3	-	3	-	3	-	ns
21	BCLK to Data-Out High Impedance	9	32	6.5	27	5.25	24.5	ns
26[2]	BCLK to Multiplexed Address Valid	n/a	n/a	n/a	n/a	n/a	n/a	ns
27[2]	BCLK to Multiplexed Address Driven	n/a	-	n/a	-	n/a	-	ns
28[2]	BCLK to Multiplexed Address High Impedance	n/a	n/a	n/a	n/a	n/a	n/a	ns
29[2]	BCLK to Multiplexed Data Driven	n/a	-	n/a	-	n/a	-	ns
30[2]	BCLK to Multiplexed Data Valid	n/a	n/a	n/a	n/a	n/a	n/a	ns
38	BCLK to Address, CIOUT, LOCK, LOCKE, R/W, SIZx, TS,..... TLNx, TMx, TTx, UPAx High Impedance	9	31	6.5	26	5.25	23.5	ns
39	BCLK to BB, TA, TIP High Impedance	19	31	14	26	11.5	23.5	ns
40	BCLK to BR, BB Valid	9	25	6.5	22.5	5.25	21	ns
43	BCLK to MI Valid	9	25	6.5	22.5	5.25	21	ns
48	BCLK to TA Valid	9	25	6.5	22.5	5.25	21	ns
50	BCLK to IPEND, PSTx, RSTO Valid	9	25	6.5	22.5	5.25	21	ns

Notes:

1 Output timing is given for output drivers specified in the DC specs (Refer to the table of HP 64783 Electrical Specifications). Large/small buffer mode select has no effect.

2 Address multiplex mode is not supported.

Input AC Timing Specifications:

Num.	Characteristic	25 MHz Min	25 MHz Max	33 MHz Min	33 MHz Max	40 MHz Min	40 MHz Max	Unit
15	Data-In Valid to BCLK (Setup)	10	-	10	-	8	-	ns
16	BCLK to Data-In Invalid (Hold)	4	-	4	-	3	-	ns
17	BCLK to Data-In High Impedance (Read Followed by Write)	49	-	36.5	-	-	30.25	ns
22a	$\overline{TA}$ Valid to BCLK (Setup)	15	-	15	-	13	-	ns
22b	$\overline{TEA}$ Valid to BCLK (Setup)	15	-	15	-	14	-	ns
22c	$\overline{TCI}$ Valid to BCLK (Setup)	15	-	15	-	14	-	ns
22d	$\overline{TBI}$ Valid to BCLK (Setup)	15	-	15	-	14	-	ns
23	BCLK to $\overline{TA}$, $\overline{TEA}$, $\overline{TCI}$, $\overline{TBI}$ Invalid (Hold)	2	-	2	-	2	-	ns
24	$\overline{AVEC}$ Valid to BCLK (Setup)	10	-	10	-	10	-	ns
25	BCLK to $\overline{AVEC}$ Invalid (Hold)	2	-	2	-	2	-	ns
31[1]	DLE Width High	n/a	-	n/a	-	n/a	-	ns
32[1]	Data-In Valid to DLE (Setup)	n/a	-	n/a	-	n/a	-	ns
33[1]	DLE to Data-In Invalid (Hold)	n/a	-	n/a	-	n/a	-	ns
34[1]	BCLK to DLE Hold	n/a	-	n/a	-	n/a	-	ns
35[1]	DLE High to BCLK	n/a	-	n/a	-	n/a	-	ns
36[1]	Data-In Valid to BCLK (DLE Mode Setup)	n/a	-	n/a	-	n/a	-	ns
37[1]	BCLK to Data-In Invalid (DLE Mode Hold)	n/a	-	n/a	-	n/a	-	ns
41a	$\overline{BB}$ Valid to BCLK (Setup)	12	-	12	-	12	-	ns
41b	$\overline{BG}$ Valid to BCLK (Setup)	12	-	12	-	12	-	ns
41c	$\overline{CDIS}$, $\overline{MDIS}$ Valid to BCLK (Setup)	13	-	13	-	13	-	ns
41d	IPLx Valid to BCLK (Setup)	8	-	8	-	8	-	ns
42	BCLK to $\overline{BB}$, $\overline{BG}$, $\overline{CDIS}$, IPLx, $\overline{MDIS}$ Invalid (Hold)	2	-	2	-	2	-	ns
44a	Address Valid to BCLK (Setup)	12	-	12	-	12	-	ns
44b	SIZx Valid to BCLK (Setup)	13	-	13	-	13	-	ns
44c	TTx Valid to BCLK (Setup)	13	-	13	-	13	-	ns
44d	R/$\overline{W}$ Valid to BCLK (Setup)	10	-	10	-	10	-	ns
44e	SCx Valid to BCLK (Setup)	16	-	16	-	13	-	ns
45	BCLK to Address, SIZx, TTx, R/$\overline{W}$ SCx Invalid (Hold)	2	-	2	-	2	-	ns
46	$\overline{TS}$ Valid to BCLK (Setup)	14	-	14	-	12	-	ns
47	BCLK to $\overline{TS}$ Invalid (Hold)	2	-	2	-	2	-	ns
49	BCLK to $\overline{BB}$ High Impedance (MC68040 Assumes Bus Mastership)	-	9	-	9	-	9	ns
51	$\overline{RSTI}$ Valid to BCLK	9	-	9	-	9	-	ns
52	BCLK to $\overline{RSTI}$ Invalid	2	-	2	-	2	-	ns
53[2]	Mode Select Setup to $\overline{RSTI}$ Negated	n/a	-	n/a	-	n/a	-	ns
54[2]	$\overline{RSTI}$ Negated to Mode Selects Invalid	n/a	-	n/a	-	n/a	-	ns

Notes:
1 Data Latch mode is not supported.
2 Mode selects are not used.

Ordering Information

Terminal-Based Emulation System for 68040 Processors

Model	Description
64783A	16.7 to 33 MHz active probe emulator with space for up to 8 Mbytes of emulation memory for 68040 processors (includes demo board)
64783B	20 to 40 MHz active probe emulator with space for up to 8 Mbytes of emulation memory for 68040 processors (includes demo board)
64748C	Emulation control card
64704A	1K deep 80-channel emulation bus analyzer card
64700A/B	Card cage

Emulation System Options

Model	Description
64172A	256 Kbyte, SRAM memory module (20 ns)
64172B	1 Mbyte, SRAM memory module (20 ns)
64173A*	4 Mbyte, SRAM memory module (25 ns)
64701A	LAN card (for HP 64700A card cage)
64037A	RS-422 interface card for PC compatibles
64708A	Software performance analyzer card, (supported on HP 9000 Series workstations and SUN SPARCstations, HP B1487A software required)
64023A	CMB cable (4m long; includes three 9-pin connectors)
64794A	8K deep emulation bus analyzer card, 80-channel
64794C	64K deep emulation bus analyzer card, 80-channel
64794D	256K deep emulation bus analyzer card, 80-channel
E3429A	PGA to PGA flexible extender

** Contact your HP Field Engineer for the configuration information and availability of 4 Mbyte memory modules and graphical PC interface.*

Software Options for Workstations

For each software model number ordered, purchase one media option and at least one license option for each concurrent user:

Model	Description
Embedded Debug Environment	
B3090B	Graphical emulator/analyzer
B1467B	Debugger/simulator
B1477B	Debugger/emulator
B1487A	Software performance analyzer (requires HP 64708A analyzer card)
B1418A	Branch validator
B3080A	Real-time operating system measurement tool for pSOS+
B3081A	Real-time operating system measurement tool for VRTX32
B3082A	Custom real-time operating system measurement tool
Advanced Cross Language Tools	
B3640A	Assembler/linker
B3641A	ANSI C cross compiler
Media/License Options	
Opt AAH	HP 9000 Series 300/400 manuals/media (DDS DAT tape)
Opt AAX	HP 9000 Series 300/400 manuals/media (1/4 inch cartridge tape)
Opt UBX	HP 9000 Series 300/400 single user license
Opt AAY	HP 9000 Series 700 manuals/media (DDS DAT tape)
Opt UBY	HP 9000 Series 700 single user license
Opt AAV	Sun SPARCstation manuals/media (1/4 inch cartridge tape)
Opt UBK	Sun SPARCstation single user license

Software Options for PCs

For each software model number ordered, purchase one media option and at least one license option for each concurrent user:

Model	Description
B3629A*	Real-time C debugger interface
64783S	
Opt 006	Hosted user interface
Advanced Cross Language Tools	
B3640A	Assembler/linker
B3641A	ANSI C compiler
Media/License Options	
Opt AJ4	IBM 3 1/2" manuals/media
Opt AJ5	IBM 5 1/4" manuals/media
Opt UDY	IBM single user license

Software Support

HP provides software upgrades through the purchase of the software materials subscription (SMS) service. Contact your HP field engineer for more information.

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For more information, call your local HP sales office listed in your telephone directory or an HP regional office listed below for the location of your nearest sales office.

United States:
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(800) 447-3282

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Rockville, MD 20850
(301) 258-2000

Hewlett-Packard Company
5201 Tollview Drive
Rolling Meadows, IL 60008
(708) 255-9800

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Fullerton, CA 92631
(714) 999-6700

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(404) 980-7351

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Tokyo 168, Japan
(813) 3335 8192

Latin America:
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Latin American Region Headquarters
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(305) 267-4245/4220

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Blackburn, Victoria 3130
Australia (A.C.N. 004 394 763)
(03) 895-2895

Far East:
Hewlett-Packard Pacific Ltd.
22-30/F Peregrine Tower, Lippo Centre
89 Queensway, Central,
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(852) 848-7070

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