64000

HP64000 Logic Development System

Model 64310A Software Performance Analyzer

HEWLETT PACKARD

CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

CW&A 2/81

HEWLETT-PACKARD

SERVICE MANUAL

MODEL 64310A

SOFTWARE PERFORMANCE ANALYZER

REPAIR NUMBERS

This manual applies directly to models
with repair numbers prefixed 2245A.

Manual Part Number: 64310-90901
Microfiche Part Number: 64310-90801

Printed: March 1983

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

Dangerous voltages, capable of causing death, are present in this instrument. Use extreme caution when handling, testing, and adjusting.

QUICK REFERENCE GUIDE - 64310A SOFTWARE PERFORMANCE ANALYZER

OPERATION.

The software performance analyzer is used with Hewlett-Packard 64000 series emulator subsystems. It is installed in the emulator subsystem like a model 64300A or 64302A logic analyzer, but does not replace them. Rather, it provides additional capabilities for monitoring the emulation bus. Unlike the logic analyzers, which operate only as a part of the emulation mode software, the software performance analyzer has its own separate mode of operation.

ON-BOARD MICROPROCESSOR.

The 64310A has its own on-board microprocessor that communicates with the host development station via an asynchronous interface. The development station initializes the 64310A by sending a signal to the ansynchronous interface to reset the microprocessor. After receiving the signal, the microprocessor runs a reset routine that is resident in on-board ROM. When a failure prevents the host station from correctly communicating with the 64310A, most of the performance verification test results are not valid.

PERFORMANCE VERIFICATION.

When the software performance analyzer is selected under <option_test> PV, the following tests are displayed.

PERFORMANCE ANALYZER RESET. Checks the microcontroller composed of a 68B09 microprocessor, ROM, and RAM.

MAINFRAME/ANALYZER INTERFACE. Checks interface, and RAM addressing capablility.

DATA ACQUISITION. Checks trigger and run latch and measurement context circuitry.

TIME, EVENT, AND SEQUENCE COUNTER. Checks programmable time, event and sequence counters.

STATISTICS. Checks the statistics circuitry composed of the time, event, and sequence counters, flip-flops, and interrupt controller. The statistics test may require removal of the emulation bus cables. A prompt indicates when this is necessary.

INTER-MODULE BUS. Checks the IMB interface between the 64310A and another option board with IMB capabilities. This test requires an IMB cable be connected between the 64310A and the option board used as the IMB stimulus. When there is no other option board with IMB capabilities present, the inter-module bus test does not appear.

QUICK REFERENCE GUIDE - 64310A SOFTWARE PERFORMANCE ANALYZER

When the emulator connected to the 64310A is selected under <option_test> PV, the analyzer stimulus test is one of the tests displayed.

ANALYZER STIMULUS. Checks the 24 bit analyzer address bus, even though the emulator may have only a 16 bit address bus. For these emulators, the upper 8 bits may be tied high or low during testing. See Performance Analyzer Stimulus Test paragraphs in Section IV Performance Tests.

BE AWARE OF THE FOLLOWING.

Under normal operating conditions, comparator chips U27-32 and U42-47 run hot, about 45 degrees centigrade.

There is a test switch on the board. When incorrectly set, the analyzer will not operate or self-test properly. See Basic Microcontroller Failure paragraphs in Section IV Performance Tests.

When using a 16-bit-address emulator, the analyzer stimulus test may display 'Can count address = FFxxxxH'. This occurs because the analyzer emulation address bus is 24 bits wide and some emulators tie the unused upper 8 bits high during testing.

TABLE OF CONTENTS

TABLE OF CONTENTS (Cont'd)

TABLE OF CONTENTS (Cont'd)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Cont'd)

Figure Page

LIST OF TABLES

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This service manual explains how to install, test, and service the Hewlett-Packard Model 64310A Software Performance Analyzer. Detailed operating instructions are provided in a separate operating manual supplied with the instrument.

Service information contained in this manual allows the user to isolate functional problems to the board or component level. Board level troubleshooting is in support of the Hewlett-Packard Bluestripe board exchange program.

1-3. Described in this section are instruments covered, the general features of the software performance analyzer, power supply loads, and its use with Hewlett-Packard emulators. Also included are conventions used in the manual.

1-4. Shown on the title page is a microfiche part number. This number can be used to order 4 x 6 inch microfilm transparencies of the manual. Each microfiche contains up to 96 photoduplicates of the manual pages.

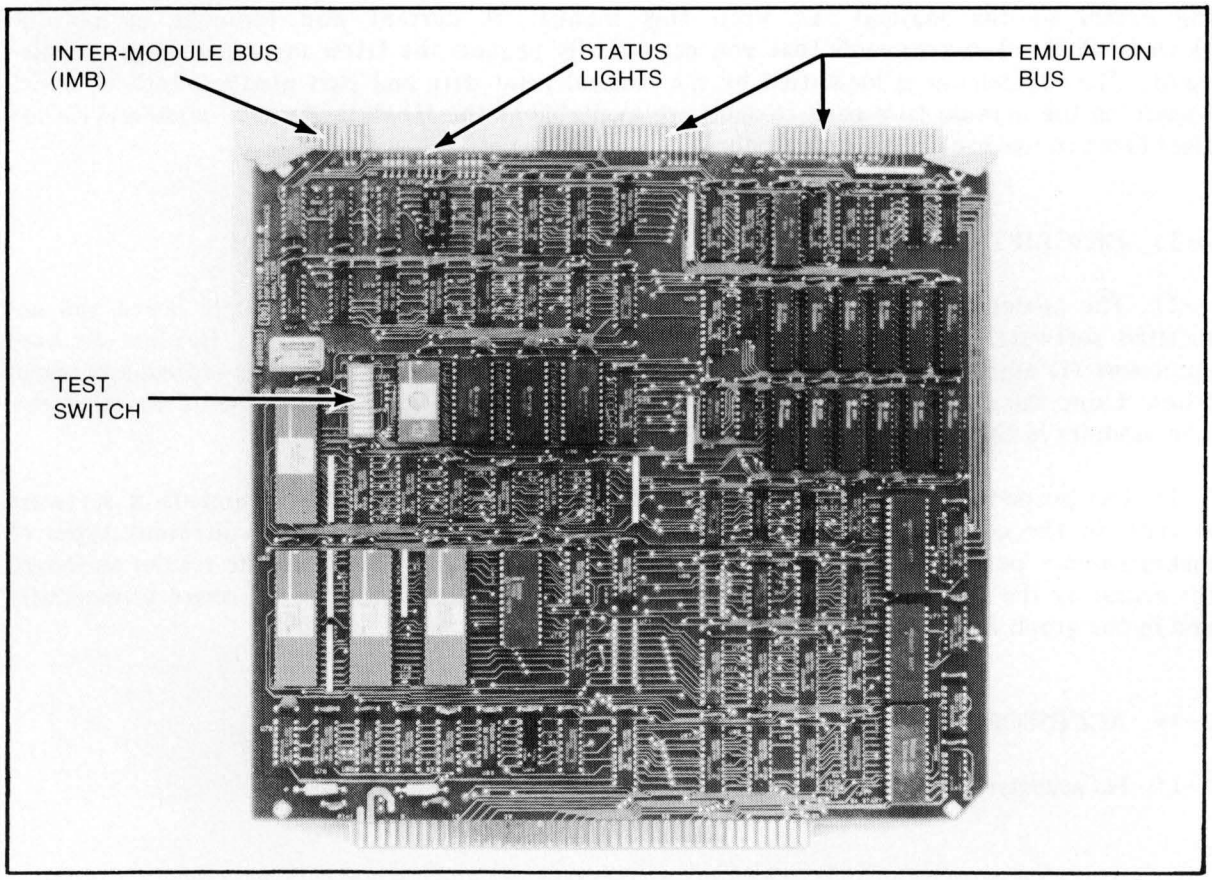


Figure 1-1. Model 64310A Software Performance Analyzer

1-5. RELATED SERVICE MANUALS.

1-6. Service manuals for the models listed below provide additional information that may be useful in servicing the analyzer.

a. Development station models 64100A and 64110A.

b. Internal analyzer models 64300A and 64302A.

1-7. INSTRUMENTS COVERED BY THIS MANUAL.

1-8. Attached to the Model 64310A Software Performance Analyzer is a repair number tag. The repair number is in the form 0000A 00000. It is in two parts; the first four digits and the letter are the prefix and the last five digits are the suffix. The prefix is the same for identical 64310A Software Performance Analyzers; but the suffix is different and uniquely identifies each analyzer manufactured. This manual applies to all 64310A Software Performance Analyzers with a repair prefix that is listed on the title page.

1-9. A model 64310A manufactured after the printing of this manual may have repair number not listed on the title page. The manual for the newer analyzer is accompanied by a yellow manual change supplement. The supplement explains how to adapt the manual to the analyzer.

1-10. In addition to change information, the supplement may contain information for correcting errors in the manual. To keep this manual as current and accurate as possible, Hewlett-Packard recommends that you periodically request the latest manual changes supplement. The supplement is identified by the manual print date and part number, both of which appear on the manual title page. Copies are available at the Hewlett-Packard sales/service offices listed in the back of this manual.

1-11. DESCRIPTION.

1-12. The model 64310A Software Performance Analyzer consists of a single board and associated software. It is a 64000 series internal analyzer that connects to Hewlett-Packard emulators via emulation bus cables. The analyzer monitors only the emulator address and status buses. Using the inter-module bus (IMB), the analyzer can trigger, or be triggered by other option modules in the card cage.

1-13. The purpose of the software performance analyzer is to make measurements of software activity in the connected emulator. Basically, the analyzer can make six different types of measurements, perform statistical analysis of the measurements, and store the results on-board for access by the development station. Results of the measurements are expressed numerically and in bar graph form on the development station display.

1-14. ACCESSORIES SUPPLIED.

1-15. No accessories are supplied with the analyzer.

1-16. ADDITIONAL EQUIPMENT REQUIRED.

1-17. The Model 64310A Software Performance Analyzer must be connected to a Hewlett-Packard emulator controller that is installed in a Hewlett-Packard 64000 series development station.

1-18. POWER REQUIREMENTS.

1-19. Power requirements of the software performance analyzer are shown in table 1-1.

Table 1-1. +5 Volt Power Supply Load

+5 volt supply; current = 5 amps maximum

1-20. LEVEL OF SERVICE.

1-21. This is a final component-level service manual. It contains performance verification (PV) and signature analysis (SA) test information for component level service of the software performance analyzer. Detailed schematics and parts lists are provided to assist in the servicing of the board.

1-22. CONVENTIONS.

1-23. The following conventions are used in the text and schematics.

a. Abbreviations, see table 6-1.

b. Mnemonics (signal names); see table 8-2.

The letters to the left of the slash (/) indicate the electrical status of the signal. The letters to the right of the slash show the signal function. For example, L/STB is low/strobe. Typical status indicators are:

L=low, or latched, H=high, B=buffered, E=ECL

Both TTL- and ECL-level signals are used. The ECL signal menemonics have an E in the electrical status. For example, EL/ANAL is the ECL version of the TTL signal L/ANAL. Mnemonics that do not have electrical status are assumed to be TTL with no predominant active level. For example, POL is a polarity signal.

c. Logic symbols, see table 8-3.

d. Softkeys are indicated by arrow brackets, while normal keys are shown in square brackets. For example, <stop> indicates the software labeled stop key, while [RETURN] indicates the keyboard labeled return key.

e. Component designators are assigned according to the upper left to lower right method.

f. Logic levels in volts:

	Input high threshold	Input low threshold	Output high threshold	Output low threshold
TTL	+2.0	+0.8	+2.4	+0.2
ECL	-1.1	-1.5	-1.1	-1.5

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information necessary to install the Model 64310A Software Performance Analyzer in a 64000 series development station. Also included is information concerning initial inspection, damage claims, environmental considerations, storage and shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents have been checked for completeness and the model 64310A has been checked mechanically and electrically. If the contents are incomplete, if there is mechanical damage or defect, or if the model 64310A does not pass performance verification, notify the nearest Hewlett-Packard sales/service office. If the shipping container or cushioning material is damaged, notify the carrier as well as the Hewlett-Packard office. Keep the shipping materials for carrier's inspection. The Hewlett-Packard office will arrange for repair or replacement at HP option without waiting for claim settlement.

2-5. SERVICE, CARD CAGE CONFIGURATIONS.

2-6. When performing service tests, it is best to initially use the actual card cage operating configuration. When a normal operating configuration is not established, one of the configurations shown in figure 2-1 can be used. Each configuration is designed to optimize cable lengths and positions within the card cage.

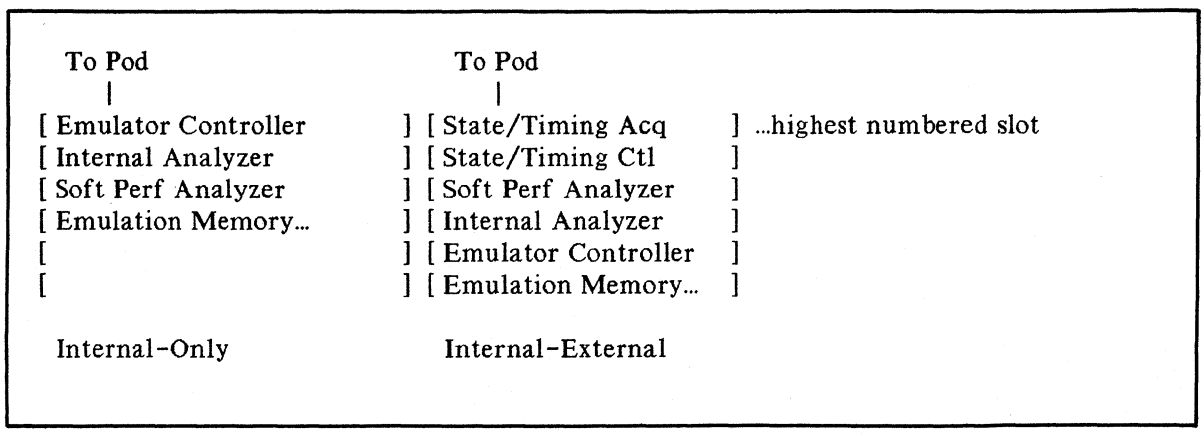


Figure 2-1. Typical Card Cage Configurations

2-7. When connections between the analyzer options and the target system are required, the external-internal configuration is preferable. For example, this configuration is used when the model 64600S Logic Timing Analyzer, or the 64620S Logic State Analyzer subsystems are present.

2-8. When no external connections are required between analyzer options and the target system, the internal-only configuration is better. For example, this configuration is used when the model 64300A or 64302A Logic Analyzers are the only analyzer options present.

2-9. In either case, complete testing of the software performance analyzer is not possible unless an emulator subsystem and an option card with IMB capabilities are connected to the software performance analyzer via emulation and IMB cables. When an emulator is not present, the analyzer stimulus test cannot be performed. This reduces the number of circuit nodes tested by approximately 22%. When no option board with IMB capablities is present, the software performance analyzer's Inter-Module Bus test is not executed.

CAUTION

The Model 64310A Software Performance Analyzer must be installed and removed with the development station power turned off.

2-10. INSTALLATION.

2-11. For detailed installation instructions, refer to the operating manuals for the option boards required in the card cage. For quick reference, the basic steps are presented below

2-12. To install the option boards necessary for complete testing of the software performance analyzer, perform the following steps.

a. Remove the card cage cover. Position the development station so there is clear access to the card cage.

b. Install the emulator control board and the emulator pod.

c. When the emulator requires emulation memory option boards, install the memory controller first, then the memory board(s).

d. Install an option board with inter-module bus capabilities.

e. Install the software performance analyzer.

f. Use two 50-pin cables to connect the edge connectors on the emulation bus.

g. Use a 20-pin cable to connect the edge connectors on the inter-module bus.

2-13. REMOVAL.

2-14. To remove the software performance analyzer, proceed as follows:

a. Remove the card cage cover. Position the development station so there is clear access to the card cage.

b. Locate the software performance analyzer. The extraction tabs on the analyzer are labeled PERFANL and 64310A.

c. Remove the two 50-pin emulation cables; and remove the 20-pin inter-module bus cable.

d. Unseat the analyzer by lifting up the outside edges of the extractor tabs.

e. The software performance analyzer can now be removed by sliding it out of the card cage slot.

2-15. OPERATING ENVIRONMENT.

2-16. The Model 64310A Software Performance Analyzer can be operated in environments within the limits shown below. It should be protected from temperature extremes which cause condensation within the instrument.

Temperature.....0 to +40 degrees Celsius.
Humidity.....5 to 80 % relative humidity.
Altitude.....4,600 m (15,000 ft).

2-17. STORAGE AND SHIPPING ENVIRONMENT.

2-18. The software performance analyzer can be stored and shipped in environments within the limits given below.

Temperature.....-40 to +40 degrees Celsius.
Humidity.....5 to 80 % relative humidity.
Altitude.....15,240 m (50,000 ft).

2-19. ORIGINAL PACKAGING.

2-20. Containers and packing materials identical to those used in factory packaging are available through Hewlett-Packard sales and service offices.

2-21. OTHER PACKAGING.

2-22. The following general instructions should be used for repackaging with commercially available materials.

a. Wrap the Model 64310A Software Performance Analyzer in heavy paper or plastic Use a strong shipping container. A double wall carton made of 350 pound test material is adequate.

b. Use a layer of shock absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the model 64310A to provide firm cushioning and prevent movement inside the container

c. Seal shipping container securely.

d. Mark shipping container FRAGILE to request careful handling.

e. In any correspondence, refer to instrument by model number and full repair number.

SECTION III

OPERATION

The operation of the Model 64310A Software Performance Analyzer is a function of the 64000 Logic Development System software and is beyond the scope of this service manual. Please refer to the software performance analyzer operator manual.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section describes the performance verification (PV), and signature analysis techniques, for testing and troubleshooting the software performance analyzer.

Troubleshooting of the analyzer may be carried out to the component level, as described in this section, or to the module level. Although not specifically described in this section, module level repair simply involves replacement of the analyzer board if any of the performance verification tests fail. Module level repair is supported by the Hewlett-Packard Bluestripe exchange program.

4-3. SYSTEM CONSIDERATIONS.

4-4. Failure isolation must be performed to eliminate other sections of the logic development system as the source of the failure. It is assumed in this manual that the development station PV has been successfully conducted and that other option cards have also been checked. It is also assumed that the target system being emulated has been disconnected from the emulator pod, thus eliminating it as a possible source of the failure.

4-5. PERFORMANCE VERIFICATION TESTS.

4-6. The performance verification for the software performance analyzer is a subsection of the system Option Test Performance Verification. The system level PV tests all option modules that are located in the development station card cage. In addition, the PV can be used as a stimulus for troubleshooting using signature analysis techniques.

4-7. REQUIRED EQUIPMENT.

a. Development station with most recent PV software.

b. To test the inter-module bus (IMB), another option card with IMB capabilities must be present and connected to the software performance analyzer via an IMB cable. Some products that have this capability are a Model 64302A Wide Logic Analyzer, 64601A Timing Control Board, 64621A State Control Board, or another software performance analyzer.

c. To test the comparator circuitry and emulation bus latches, an emulator must be connected to the software performance analyzer via emulation bus cables. The emulator performance verification software must be available to run the analyzer stimulus test.

d. To print PV results, a printer must be attached to the system.

e. For troubleshooting, a Hewlett-Packard Model 545A Logic Probe, and 5005A Signature Multimeter, or equivalent equipment, is required.

4-8. STARTING PERFORMANCE VERIFICATION.

4-9. To test the software performance analyzer proceed as follows.

a. With the operating system initialized and awaiting a command, figure 4-1, enter:

option_test [RETURN]

b. The PV now displays a directory of the installed option boards and their card slot numbers, figure 4-2. The first step in the PV is to locate the card slot of the Model 64310A Software Performance Analyzer and enter the slot number; for example, if it is in slot 8 of the card cage, enter:

8 [RETURN]

c. When the card cage contains no other option cards with Inter Module Bus (IMB) capabilites, the Total PV display appears, and IMB testing is automatically suppressed.

d. When one option card with IMB capabilities is present, the Total PV display appears and IMB testing is automatically activated. Make certain the IMB cable is connected, or the results of the test will be invalid.

e. When two or more option cards with IMB capabilities are present, the display prompts

Select IMB external stimulus for test.

f. Enter the card slot of the option card to provide the stimulus. The Total PV Display then appears. Once chosen, the stimulus source can not be changed without restarting the software performance analyzer PV. Make certain the IMB bus cable is connected to the external stimulus board, or the results of the test will be invalid.

4-10. PERFORMANCE VERIFICATION AND THE MICROCONTROLLER.

4-11. The 64310A performance verification tests operate in a different manner from most other 64000 option cards because the analyzer has an on-board microprocessor, ROM and RAM. The on-board 68B09 microprocessor and associated ROM and RAM circuitry is referred to as the microcontroller. The development station processor does not have direct control over the analyzer microcontroller and must communicate with it via a handshake protocol, passing test data only when both the analyzer microcontroller and the development station are ready.

4-12. There are three 2K byte RAMs in the microcontroller and one 2K ROM. ROM U35 contains all of the performance analyzer reset test code and the first three steps of the mainframe / analyzer interface test. Also in ROM U35 is code to transfer data between the analyzer and the development station. When the analyzer passes the tests contained in ROM U35, it loads PV code from the development station into RAM U38 to perform further tests.

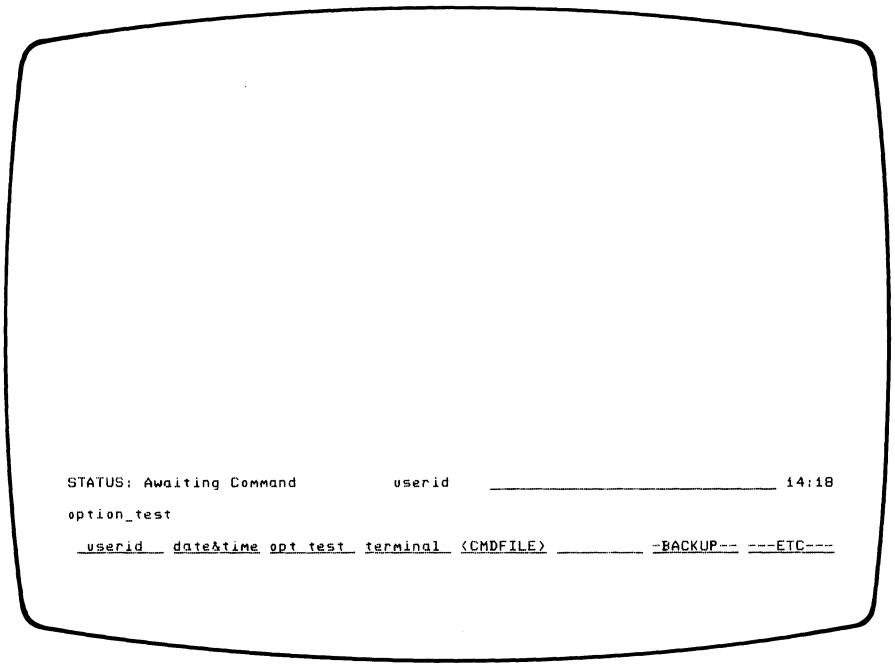


Figure 4-1. System Awaiting Command Display

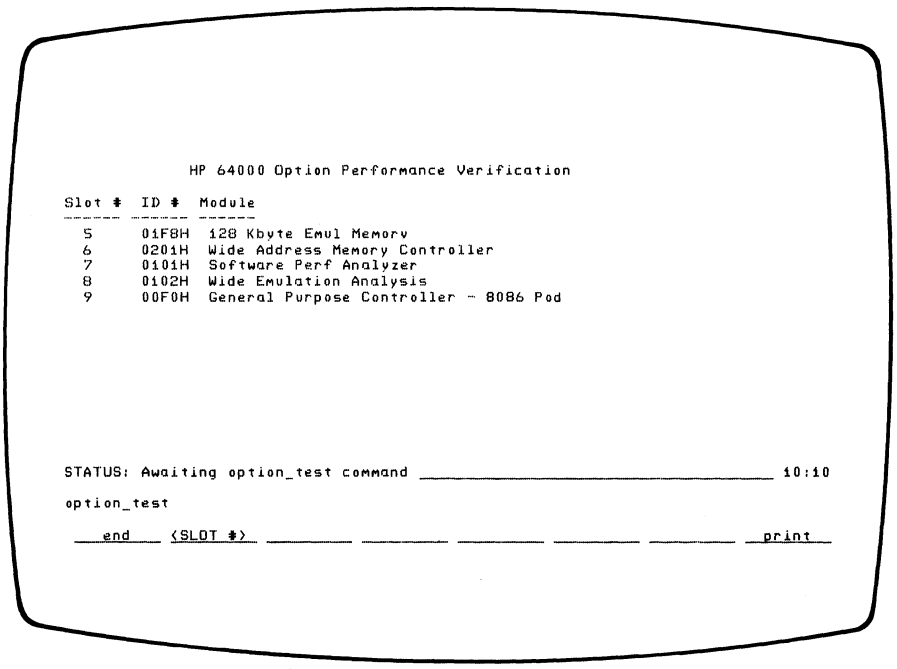


Figure 4-2. Card Cage Directory Display

4-13. When the analyzer microcontroller is not executing code correctly, the development station may never receive the results of the requested test; therefore, the station has a test time-out feature. When a time-out occurs, the screen displays

Test fails because of no response from 64310A Performance Analyzer !

4-14. The time-out error message may appear only on the data acquisition; time, event, and sequence counter; statistics, inter-module, and analyzer stimulus tests.

4-15. PERFORMANCE VERIFICATION COMMANDS.

4-16. Each PV display provides prompting for commands that can be executed. These commands are selected by 'softkeys' that are defined in table 4-1.

Table 4-1. Performance Verification Softkeys

<cycle>	Starts highlighted test and continues through other tests. When pressed during cycling, it stops the testing.
<disp_test>	Displays test details. (Use 'display_test' in command files.)
<end>	Terminates performance verification and returns to the card cage directory display. It resets all test and failure counters to zero.
<exit_test>	Stops the test and returns to next higher level display.
<next_test>	Moves highlight line to following test category.
<print>	Outputs display to attached printer.
<start>	Begins the test. When pressed during testing, it stops the test.

4-17. TOTAL PV TEST DISPLAY.

4-18. Purpose. All test categories available for the card cage configuration are shown in this display. When one or more test categories have been executed, the results are displayed. Use the display to choose the test categories to be performed or to review the overall results of the PV.

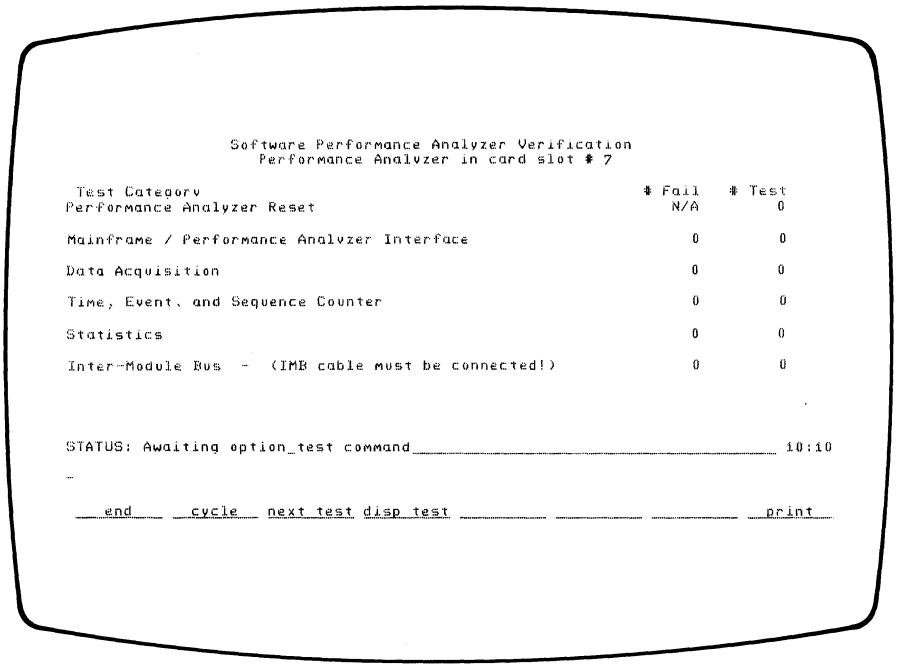


Figure 4-3. Total PV Test Display

4-19. Running the Total PV. To run all the tests shown on the display, press the <cycle> softkey. Each test category is executed and the results are displayed. A complete cycle requires approximately 15 seconds. To stop the iterations, press the <cycle> softkey again.

4-20. Reading the Total PV Results. When the tests are complete, examine the # Fail column. When all entries are zero, it indicates that 72% of the circuit nodes have been checked and no errors have been found. Another 22% of the nodes can be checked by running the emulator Analysis Stimulus Test described at the end of this section.

4-21. A non-zero value represents the number of errors detected in the test category. Determine the exact cause of the error by viewing the failed test category in detail. Do this by positioning the highlight line over the test category and pressing the <disp_test> softkey.

4-22. OVERALL TROUBLESHOOTING STEPS.

4-23. Begin at paragraph 4-8. Starting Performance Verification.

4-24. When the software performance analyzer is in the card cage, but does not appear in the card cage display, troubleshoot the board ID circuit. See schematic 1.

4-25. If the Total PV Display does not appear, the software performance analyzer PV software is not available, and must be loaded.

4-26. Go to paragraph 4-17. Total PV Test Display.

4-27. Cycle through the tests, and look at the mainframe / analyzer interface test, # Fail column. When there is an interface test failure, go to paragraph 4-70. Mainframe / Analyzer Interface Test Troubleshooting. Do not attempt to troubleshoot any other failures until the interface test executes successfully.

4-28. When the mainframe / analyzer interface test is executing successfully, begin troubleshooting of other failures in the same sequence as the tests appear in the Total PV Display. Go to the paragraphs shown below, as appropriate.

a. 4-106. Data Aquisition Test Troubleshooting

b. 4-120. Time, Event, and Sequence Counter Test Troubleshooting

c. 4-150. Statistics Test Troubleshooting

d. 4-168. Inter-Module Bus Test Troubleshooting

e. 4-187. Analyzer Stimulus Test Troubleshooting

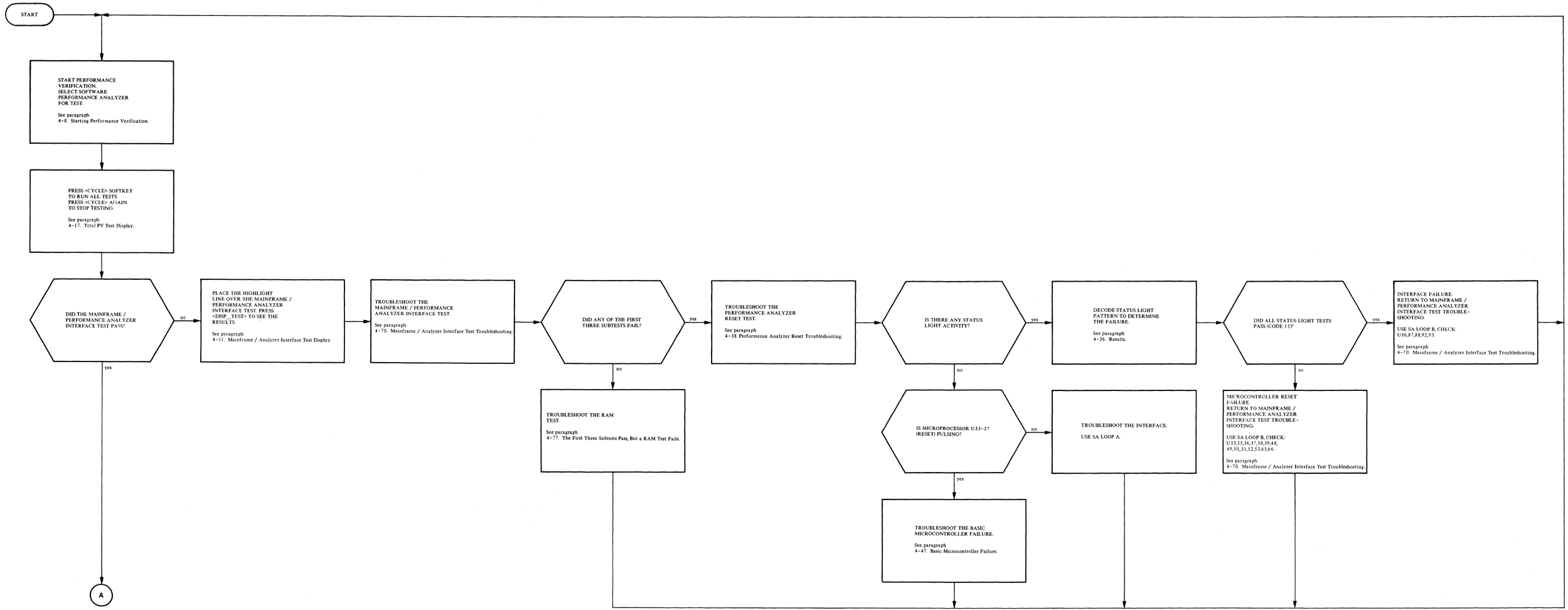


Figure 4-4.
Troubleshooting Flowchart

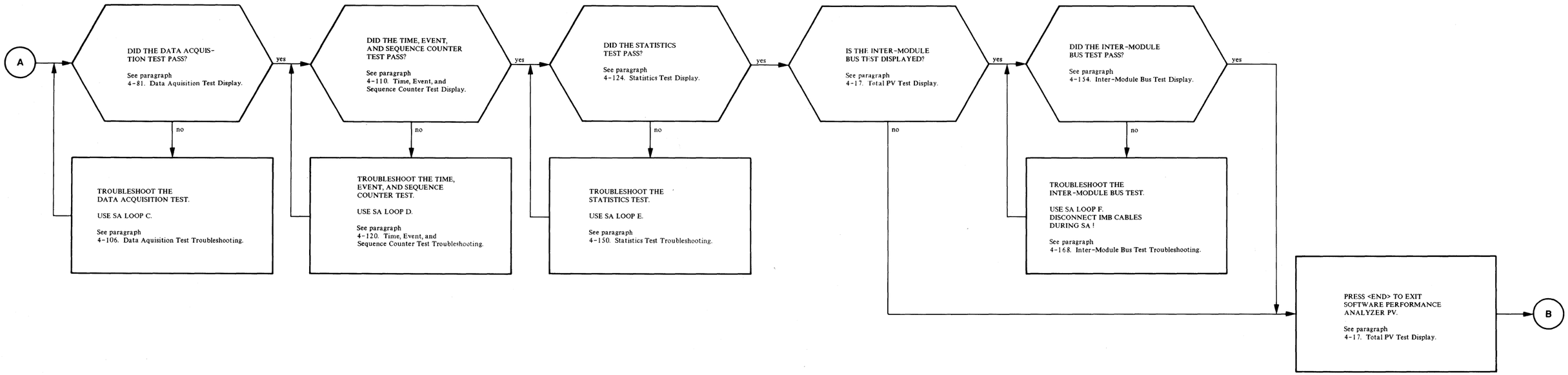


Figure 4-4. Troubleshooting Flowchart (Cont'd)

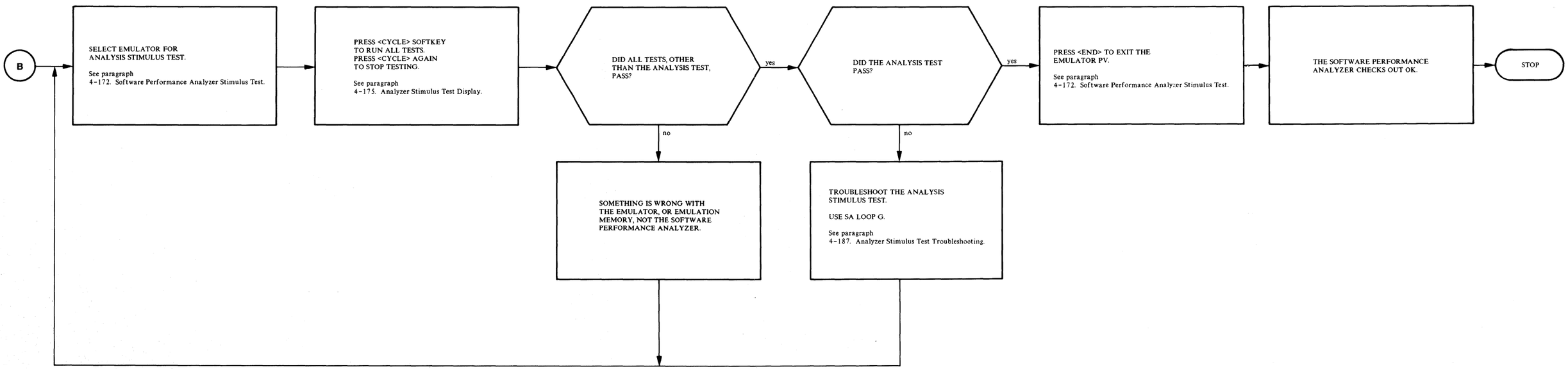


Figure 4-4.
Troubleshooting Flowchart (Cont'd)

4-29. PERFORMANCE ANALYZER RESET TEST DISPLAY.

4-30. Purpose. This test checks microprocessor U33 for its ability to run the reset program stored in ROM U35. RAM U38 is tested for address and data errors, while RAMs U36 and U37 are tested for data errors only.

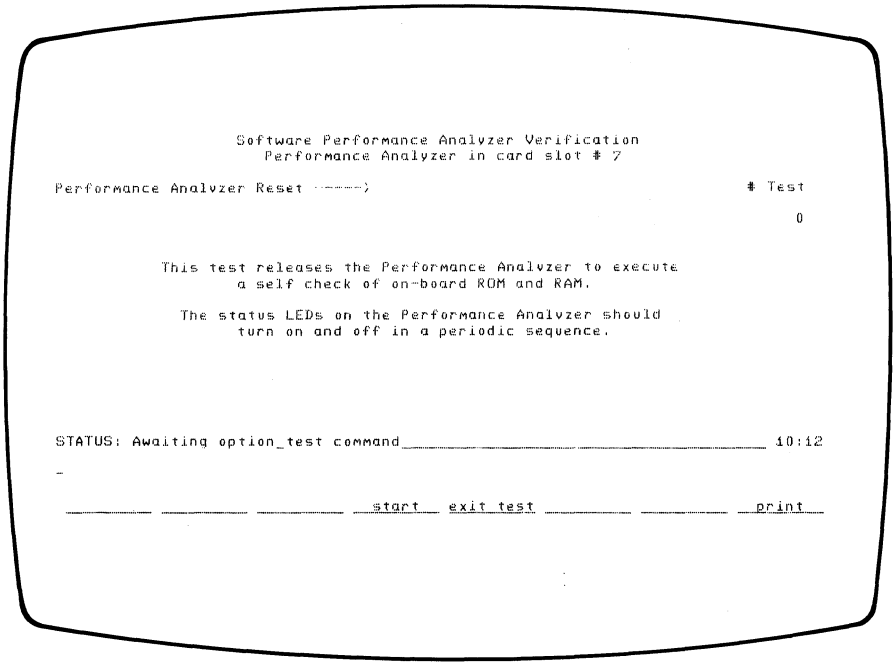


Figure 4-5. Performance Analyzer Reset Test Display

4-31. Running the Performance Analyzer Reset Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Performance Analyzer Reset' and then press the <disp_test> softkey. Next, press the <start> softkey to begin the test. The test continues to run until a softkey is pressed. The test takes less than five seconds per iteration.

4-32. Reading the Performance Analyzer Reset Test Results. The # Fail column always shows the letters 'N/A', meaning 'not available'. This is because approximately every five seconds the development station sends the analyzer a reset. The reset causes the microcontroller to execute the reset test stored in ROM U35, but no test results are transferred back to the development station.

4-33. Errors can be identified on the LED lights at the top edge of the analyzer board. Details on decoding these errors are given in the following paragraphs.

4-34. How. The test resets the analyzer to run code from ROM U35. This routine is run every time the analyzer is configured; thus, each PV test includes execution of this reset code at least once.

4-35. There are eight steps within the reset test. At the start of the test, the status lights at the top of the analyzer board are initialized. As each step begins, the lights are updated. When a test fails, microprocessor U33 executes an endless loop; thus, the lights are locked-up and indicate the test step that failed. There is no accumulation of errors and the development station cannot communicate with the analyzer at this point in the testing.

4-36. Results. The test results are interpreted by reading lights abcdefg at the top of the board. Between each iteration of the reset test there is a pause, and the light pattern is momentarily static. Note the exact pattern at this point; when it matches the last pattern shown below (code 11), all steps of the reset test are executing correctly. When there is a different pattern, decode the specific test that is failing. Light o should be illuminated in all steps, except the very first.

Light Pattern	7 Bit Code	Reset Test Steps
o abc defg		
o ooo oooo	00	Microprocessor U33 register test.
x xxx xxxx	7F	All lights on, then walking lights test, to provide visual verification of activity.
x ooo ooox	01	ROM U35 checksum test, to validate programs stored in the ROM.
x ooo ooxx	03	RAM U38 data test.
x ooo oxoo	04	RAM U37 data test.
x ooo oxox	05	RAM U36 data test.
x ooo oxxo	06	RAM U38 address test.
x oox ooox	11	All steps passed. Awaiting next test (pause).

x = illuminated, o = not illuminated.

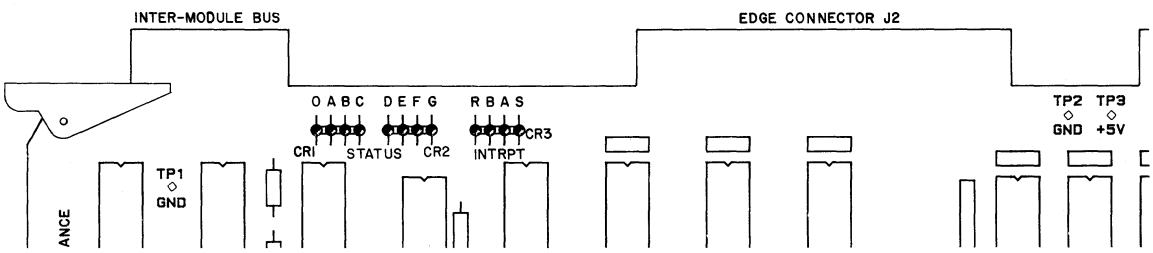


Figure 4-6. Status Light Decoding

4-37. When the reset test is successfully completed, the analyzer signals the development station that it is ready to transfer data. At this point the station can request the remaining PV tests be performed. As these tests are executed, the status lights continue to be updated. However, the lights cannot be decoded to identify an error, because the microcontroller does not lock up when an error is detected. The table below indicates the nature of the status light activity.

Light Pattern	7 Bit Code	Test in Progress
o abc defg		
		MAINFRAME / ANALYZER INTERFACE TEST
x oox oooo	10	Enable interrupts & stacking in RAM
x oox ooox	11	Opcode output to performance analyzer
x oox ooxo	12	Data input from performance analyzer
x oox ooxx	13	Data output to performance analyzer
x oox oxoo	14	RAM address line check (U36)
x oox oxox	15	RAM address line check (U37)
		DATA ACQUISITION TEST
x oxo oooo	20	Trigger and run latch control
x oxo ooox	21	Comparator bus
x oxo ooxo	22	Status qualifier RAM data
x oxo ooxx	23	Status qualifier RAM address
x oxx oooo	30	Context state register reset
x oxx ooxo	32	Context FPLA 1 checksum
x oxx ooxx	33	Context FPLA 2 checksum
x oxx oxoo	34	U57 check, using FPLA 1 sum
		TIME, EVENT, AND SEQUENCE COUNTER TEST
x xoo oooo	40	Time, event, and sequence counter reset
x xoo ooox	41	Time, counter walking 1,0 and decrement
x xoo ooxo	42	Event counter walking 1,0 and decrement
x xoo ooxx	43	Sequence counter walking 1,0 and decrement
		STATISTICS TEST
x xox oooo	50	Interrupt controller reset and response
x xox ooox	51	Time counter response
x xox ooxo	52	Event counter control
x xox ooxx	53	Time sequence counter
x xox oxoo	54	Event sequence counter
x xox oxox	55	Counter error response
		INTER-MODULE BUS TEST
x xxo oooo	60	EL/ME drive
x xxo ooox	61	EL/TE drive
x xxo ooxo	62	EH/TR drive
x xxo ooxx	63	EL/ME and EL/TE receive
x xxo oxoo	64	EL/ME, EL/TE, and EH/TR enable line test

Figure 4-7. Status Light Activity

4-38. PERFORMANCE ANALYZER RESET TROUBLESHOOTING.

4-39. Use these troubleshooting instructions to determine the nature of the failure found in the mainframe / analyzer interface test. The performance analyzer reset test must be running during this troubleshooting.

4-40. THERE IS STATUS LIGHT ACTIVITY.

4-41. When there is some status light activity, decode the light pattern using paragraph 4-36. Results. Determine which of the following status light test conditions exists.

All reset tests pass (code 11) or A reset test has failed.

Note the status light test condition, and if pertinent, note the failing test, and suspected component. Return to the mainframe / analyzer interface test troubleshooting for signature analysis LOOP B instructions.

4-42. THERE IS NO STATUS LIGHT ACTIVITY.

4-43. Verify that the reset test is running by watching the # Test indicator. Each time the # Test counter increments, the eight status lights should show some activity.

4-44. When there is no activity, use a logic probe or signature analyzer etc., and check microprocessor U33, pin 37 RESET. When it is not pulsing, there is an interface problem; use signature analysis Loop A instructions below. When it is pulsing, go to the paragraphs on basic microcontroller failure below.

4-45. SIGNATURE ANALYSIS - LOOP A.

4-46. Connect the signature analyzer as directed for SA Loop A, in Appendix A. The performance analyzer reset test provides the stimulus and must be running when signatures are taken. Reference schematics 1 and 2 in Section VIII. Check the components that process the reset signal, and check the basic microprocessor power and control.

Schematic 1, check: U89, U91. Schematic 2, check: U33.

4-47. BASIC MICROCONTROLLER FAILURE.

4-48. If RESET is pulsing, the software performance analyzer is receiving the reset signal from the development station. The microprocessor is not executing code correctly; thus, there is probably something wrong in the basic microcontroller. Possible problem areas are:

Microprocessor U33. ROM U35. Control or power supply line.

Address or data line shorted or open. Test switch SU34 set incorrectly.

Status light circuits

4-49. At this point, signature analysis is not possible; therefore, test switch SU34 is used. To test microprocessor U33, perform the steps shown below. When the switch is set to the test position, a one-byte opcode is jammed onto the data bus. This causes the microprocessor to continually fetch this opcode; therefore, the address lines should be pulsing. While in the test position, probe each pin on microprocessor U33 to verify a high, low, or pulsing condition.

a. Turn off the development station power.

b. Remove the software performance analyzer from the development station. If necessary, see removal instructions in Section II.

c. Install the software performance analyzer on a service extender board.

d. Locate test switch SU34, and set to the test position. After testing, DO NOT FORGET to reset the switch to the normal operating position.

Normal	Test
open	closed
open	closed
closed	open
closed	open
closed	open
closed	open
closed	open
closed	open
closed	open
closed	open

Figure 4-8. SU34 Test Switch Positions

e. Place the analyzer and extender back into the development station.

f. Turn on the power and start the software performance analyzer PV.

g. SELECT the performance analyzer reset test and start it running.

h. Using a logic probe, signature analyzer, etc., test each pin on microprocessor U33. See table 4-2 for expected pin status; and refer to schematic 2 in Section VIII.

1) Are pin 7 Vcc and pin 1 ground valid ?

2) Is pin 38 EXTAL pulsing ?

3) Is pin 37 RESET going from an active low to a high ?

4) Is pin 34 E pulsing ?

5) Is pin 32 READ/WRITE high, indicating a read operation ?

6) Is the microprocessor status correct;
pin 6 BA low, and pin 5 BS pulsing ?

7) Is the microprocessor data bus correct;
LHLHHHHH on pins 31 thru 24 ? L=low, H=high.

8) Are all the microprocessor address lines pulsing;
pins 8 thru 23 ?

9) Are all the buffered address lines pulsing;
U48 and U49 ?

i. When all of the pins checkout, the interface between the microprocessor and ROM U35 is suspect. In this case check the ROM output enable pin U35-20; it should be low. Check the ROM chip select pin U35-18; it should be pulsing. It is possible that ROM U35 is faulty.

j. DO NOT FORGET to return the test switch to the normal operating position when the test of microprocessor U33 is completed.

k. If all pins checkout, it may be necessary to use an ohmmeter and check the continuity of the microcontroller circuitry shown on schematic 2.

4-50. After troubleshooting the failure, return to the mainframe / analyzer interface test paragraphs and re-run the test to see that the problem is corrected.

Table 4-2. Reset Test, Microprocessor U33 Troubleshooting

Pin	Status	Pin	Status	Pin	Status	Pin	Status
1	low	11	pulsing	21	pulsing	31	high
2	high	12	pulsing	22	pulsing	32	high
3	low	13	pulsing	23	pulsing	33	high
4	pulsing	14	pulsing	24	low	34	pulsing
5	pulsing	15	pulsing	25	high	35	pulsing
6	low	16	pulsing	26	low	36	pulsing
7	high	17	pulsing	27	high	37	pulsing
8	pulsing	18	pulsing	28	high	38	pulsing
9	pulsing	19	pulsing	29	high	39	low
10	pulsing	20	pulsing	30	high	40	high

4-51. MAINFRAME / ANALYZER INTERFACE TEST DISPLAY.

4-52. **Purpose.** The first three tests shown on this display check the ability of analyzer to receive and send selected information to the development station. The last two tests check the analyzer microprocessor's ability to address RAMs U36 and U37.

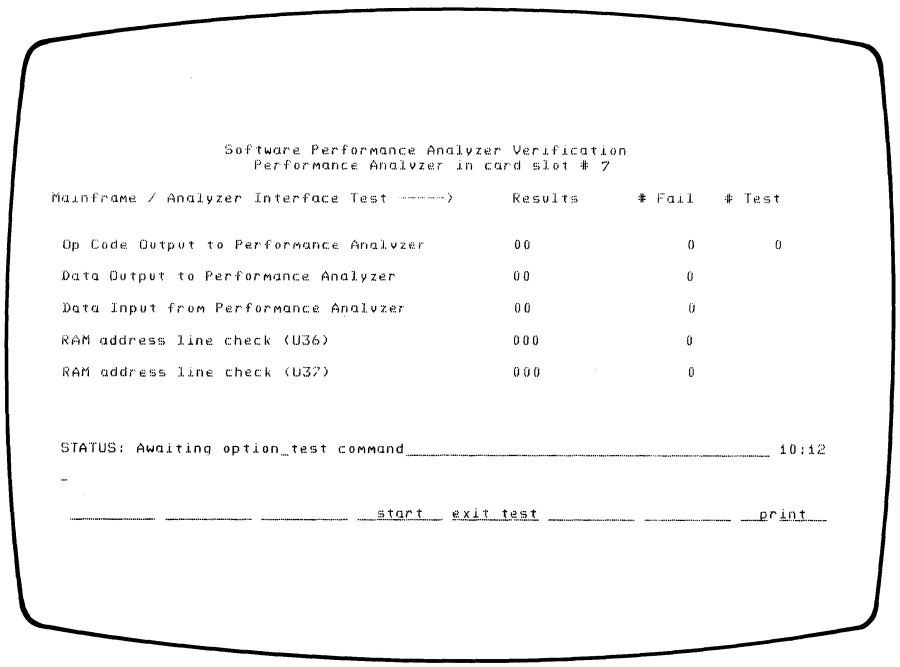


Figure 4-9. Mainframe / Analyzer Interface Test Display

4-53. **Running the Mainframe / Analyzer Interface Test.** To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Mainframe / Analyzer Interface' and then press the <disp_test> softkey. Next, press the <start> softkey to begin the test. The test continues to run until a softkey is pressed. Each iteration takes less than 8 seconds, if there are no failures. Failures may lengthen the execution time.

4-54. **Reading the Mainframe / Analyzer Interface Test Results.** The # Failures column shows the total number of errors detected during the test. Each error code in the result column represents a single failure encountered during the last iteration.

4-55. OPCODE OUTPUT TO PERFORMANCE ANALYZER.

4-56. How. After successful completion of the performance analyzer reset test, the analyzer signals the development station that it is ready to receive information. The station then sends the opcode sequence 0 through 20H. After each opcode is sent, the station briefly waits for the analyzer to signal that it is ready to receive the next opcode. When the station does not receive a signal from the analyzer in the allotted time, a failure is recorded.

4-57. Results. When a failure is detected, the result column shows the next opcode that would have been sent to the analyzer. Thus, if the analyzer never sends a ready signal, the results are 00H.

Op Code Output to Performance Analyzer.....xxH

4-58. DATA OUTPUT TO PERFORMANCE ANALYZER.

4-59. How. When the opcode output test is successfully completed, the development station sends the data sequence 0 through FFH. After each data word is sent, the station briefly waits for the analyzer to signal that it is ready to receive data. When the station does not receive a signal from the analyzer in the allotted time, a failure is recorded.

4-60. Results. When a failure is detected, the result column shows next data word that would have been sent to the analyzer.

Data Output to Performance Analyzer.....xxH

4-61. DATA INPUT FROM PERFORMANCE ANALYZER.

4-62. How. Upon successful completion of the data input test, the analyzer sends the development station the data sequence 0 through FFH. The station compares the data received with expected values; any discrepancies are recorded as failures.

4-63. Results. When an error is detected, the result column shows the exclusive OR product of data-sent with data-expected. If the two previous tests have not passed, the results of this test are probably invalid.

Data Input from Performance Analyzer.....xxH

4-64. RAM ADDRESS LINE CHECK (U36).

4-65. How. Each address bit is tested by writing zero to the lowest address in RAM U36. At this location all address lines are low. In sequence, each address line is brought high, and that location is loaded with FFH. The lowest address is read; it should contain zero. Any discrepancies from expected values is noted as an address bit error.

4-66. Results. The hexadecimal error word is decoded as follows.

RAM address line check (U36) xxxH =

Binary	Signal in Error	
0000 0000 0000	None	
---- ---- ---1	L/ADR0	U36-8
---- ---- --1-	L/ADR1	U36-7
---- ---- -1--	L/ADR2	U36-6
---- ---- 1---	L/ADR3	U36-5
---- ---1 ----	L/ADR4	U36-4
---- --1- ----	L/ADR5	U36-3
---- -1-- ----	L/ADR6	U36-2
---- 1--- ----	L/ADR7	U36-1
---1 ---- ----	L/ADR8	U36-23
--1- ---- ----	L/ADR9	U36-22
-1-- ---- ----	L/ADR10	U36-19
---- ---- ----	na	

4-67. RAM ADDRESS LINE CHECK (U37).

4-68. How. Each address bit is tested by writing zero to the lowest address in RAM U37. At this location all address lines are low. In sequence, each address line is brought high, and that location is loaded with FFH. The lowest address is read; it should contain zero. Any discrepancies from expected values is noted as an address bit error.

4-69. Results. The hexadecimal error word is decoded as follows.

RAM address line check (U37) xxxH =

Binary	Signal in Error	
0000 0000 0000	None	
---- ---- ---1	L/ADR0	U37-8
---- ---- --1-	L/ADR1	U37-7
---- ---- -1--	L/ADR2	U37-6
---- ---- 1---	L/ADR3	U37-5
---- ---1 ----	L/ADR4	U37-4
---- --1- ----	L/ADR5	U37-3
---- -1-- ----	L/ADR6	U37-2
---- 1--- ----	L/ADR7	U37-1
---1 ---- ----	L/ADR8	U37-23
--1- ---- ----	L/ADR9	U37-22
-1-- ---- ----	L/ADR10	U37-19
---- ---- ----	na	

4-70. MAINFRAME / ANALYZER INTERFACE TEST TROUBLESHOOTING.

4-71. ANY OF THE FIRST THREE SUBTESTS FAIL.

4-72. When one or more of the first three subtests fail, the microcontroller has a malfunction. Go to paragraph 4-38. Performance Analyzer Reset Troubleshooting and determine the nature of the problem. If directed, return here to the signature analysis LOOP B paragraphs.

4-73. SIGNATURE ANALYSIS - LOOP B.

4-74. Connect the signature analyzer as directed for SA Loop B, in Appendix B. The mainframe / analyzer interface test provides the stimulus and must be running when signatures are taken. Reference schematic 2 in Section VIII.

4-75. When one of the status light tests fails, the microcontroller is executing code, but part of the microcontroller circuit is failing. Check the basic microcontroller circuitry: the microprocessor, ROM, RAM, data bus transceiver, address bus buffers, I/O decoder, wait-state shift register, and miscellaneous gates and inverters.

Schematic 2, check: U33, U35, U36, U37, U38, U39,
U48, U49, U50, U51, U52, U53, U65, U66.

4-76. When all of the status light tests pass (code 11), the microcontroller is executing code correctly, but is unable to transfer data to the development station correctly. Check the address and data interface with the development station.

Schematic 1, check: U86, U87, U88, U92, U93.

4-77. THE FIRST THREE SUBTESTS PASS, BUT A RAM TEST FAILS.

4-78. When this happens, troubleshoot the failing RAM test. Test results can be decoded using the information in Results paragraphs for the interface test.

4-79. SIGNATURE ANALYSIS - LOOP B.

4-80. Connect the signature analyzer as directed for SA Loop B, in Appendix B. The mainframe / analyzer interface test provides the stimulus and must be running when signatures are taken. Reference schematic 2 in Section VIII. Check the failing RAM.

Schematic 2, check: U36, U37, U38.

4-81. DATA ACQUISITION TEST DISPLAY.

4-82. Purpose. The seven tests shown on this display check the trigger and run latch and measurement context circuitry.

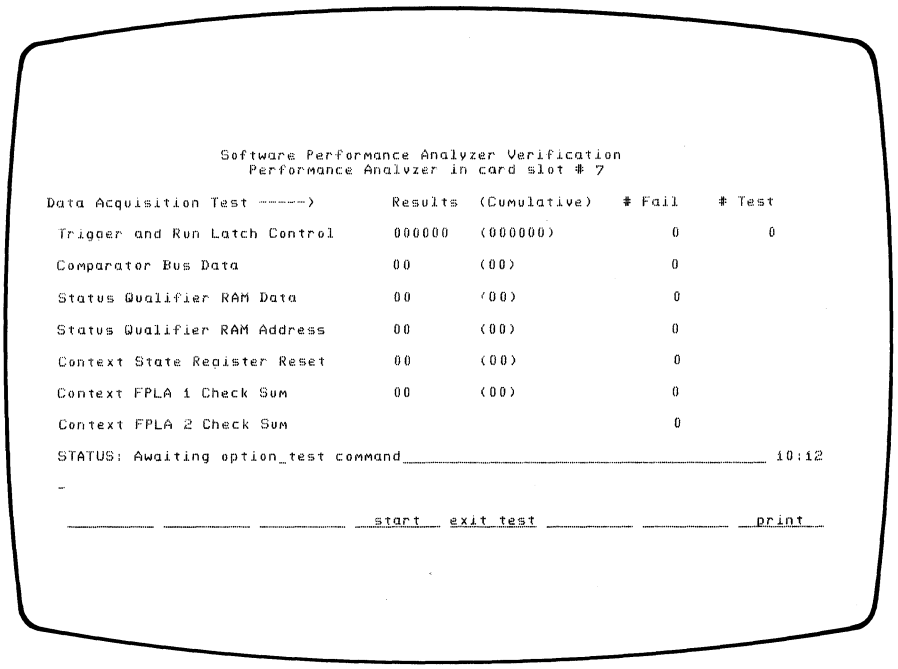


Figure 4-10. Data Acquisition Test Display

4-83. Running the Data Acquisition Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Data Acquisition Test' and then press the <disp_test> softkey. Next, press the <start> softkey to begin the test. The test continues to run until a softkey is pressed. Each iteration takes less than 2 seconds.

4-84. Reading the Data Acquisition Test Results. The # Failures column shows the total number of errors detected during the test. Each error code in the present column represents a single failure encountered during the last iteration. The cumulative error code represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-85. TRIGGER AND RUN LATCH CONTROL.

4-86. How. Six test steps are performed in the sequence described below. The reset command is H/HALT, U24-7.

1. Flip-flop U23 is reset; signal H/TRIGGER is read. It should be low.
2. Flip-flop U23 is set. Signal H/TRIGGER is read; it should be high.
3. Flip-flop U23 is reset again; H/TRIGGER should be low.
4. Signal H/RUN is read, it should be low.
5. Flip-flop U22 is clocked; H/RUN should be high.
6. Finally, flip-flop U22 is reset; H/RUN should be low.

4-87. Results. The error bits are decoded as follows.

Trigger and Run Latch Control...xxxxxx =

Bits	Test Step in Error
000000	None
-----1	1 H/TRIGGER U23-9
----1-	2 H/TRIGGER U23-9
---1--	3 H/TRIGGER U23-9
--1---	4 H/RUN U22-5
-1----	5 H/RUN U22-5
1-----	6 H/RUN U22-5

4-88. COMPARATOR BUS DATA.

4-89. How. Input latch U73 is enabled and drives output latch U75. Latch U73 is loaded in sequence with the decimal values 0 through 63. After each load, output latch U75 is read and compared with the loaded value.

4-90. Results. The hexadecimal error word is decoded as follows.

Comparator Bus Data.....xxH =

Binary	Signal in Error		
0000 0000	None		
---- ---1	BH/COMOUT1	U73-2	U75-2
---- --1-	BH/COMOUT2	U73-19	U75-17
---- -1--	BH/COMOUT3	U73-5	U75-4
---- 1---	BH/COMOUT4	U73-16	U75-15
---1 ----	BH/COMOUT5	U73-6	U75-6
--1- ----	BH/COMOUT6	U73-15	U75-13
---- ----	na		
---- ----	na		

4-91. STATUS QUALIFIER RAM DATA.

4-92. How. All 256 locations of emulator status RAM U11 are loaded in sequence with the data 0 through 3. After each load, the data is read back via output latch U75. The data read should match the loaded value. Note that only two of the four bits of RAM data are used.

4-93. Results. The error bits are decoded as follows.

Status Qualifier RAM Data.....xx =

Bits	Signal in Error	
00	None	
-1	H/QUAL 1	U11-12
1-	H/QUAL 2	U11-10

4-94. STATUS QUALIFIER RAM ADDRESS.

4-95. How. The first location in emulator status RAM U11 is 4000H to microprocessor U33; and, at this address, all the status qualifier RAM address lines are low. The location is loaded, via latch U10, with zero. In sequence, each address line is brought high and 0FH is loaded into the addressed location. After each load, location 4000H is read. It should still contain 0. If it does not, the last address bit brought high is displayed as a failure.

4-96. Results. The hexadecimal error word is decoded as follows.

Status Qualifier RAM address...xx =

Binary	Signal in Error		
0000 0000	None		
---- ---1	L/ADR0	U10-9	U11-4
---- --1-	L/ADR1	U10-6	U11-3
---- -1--	L/ADR2	U10-5	U11-2
---- 1---	L/ADR3	U10-2	U11-1
---1 ----	L/ADR4	U10-19	U11-21
--1- ----	L/ADR5	U10-16	U11-5
-1-- ----	L/ADR6	U10-15	U11-6
1--- ----	L/ADR7	U10-12	U11-7

4-97. CONTEXT STATE REGISTER RESET.

4-98. How. The context state flip-flops U56 and U68 are reset via decoder U69-12. The flip-flops are then read via buffer U74. All bits should be zero.

4-99. Results. The hexadecimal error word is decoded as follows.

Context State Register Reset...xxH =

Binary	Signal in Error		
0000 0000	None		
---- ---1	H/CONERR	U56-2	U74-2
---- --1-	L/CONEND	U56-15	U74-17
---- -1--	H/GATE B	U56-10	U74-4
---- 1---	H/GATE A	U56-7	U74-15
---1 ----	H/STATE 1	U68-2	U74-6
--1- ----	H/STATE 2	U68-15	U74-13
-1-- ----	H/STATE 3	U68-10	U74-8
1--- ----	H/STATE 4	U68-7	U74-11

4-100. CONTEXT FPLA 1 CHECKSUM.

4-101. How. Logic array U76, measurement context 1, is tested by doing a checksum. The outputs for each unique input condition to the array are added together. Input lines to the array come from mode latch U72, test latch U73, and emulator status RAM U11.

4-102. Results. The right hand bit indicates an error in performing the checksum when flip-flop U57, pin 1 is held low. The left hand bit indicates an error in performing the checksum when flip-flop U57 pin 1 is held high.

Context FPLA 1 Check Sum.....xx

4-103. CONTEXT FPLA 2 CHECKSUM.

4-104. How. Logic array U58, measurement context 2, is tested by doing a checksum. The outputs for each unique input condition to the array are added together. Input lines to the array come from mode latch U72, test latch U73, and emulator status RAM U11. Flip-flop U57 pin 1 is held low.

4-105. Results. The results of this test are not decoded. A failure indicates an incorrect checksum.

4-106. DATA ACQUISITION TEST TROUBLESHOOTING.

4-107. Do not attempt to troubleshoot the data acquisition test until the mainframe / analyzer interface test has been successfully completed. Instructions in the preceding Results paragraphs provide information on how to determine which component is suspect.

4-108. SIGNATURE ANALYSIS - LOOP C.

4-109. Connect the signature analyzer as directed for SA Loop C, in Appendix C. The data acquisition test provides the stimulus and must be running when signatures are taken. Reference schematics 2, 5 and 7 in Section VIII. Check the components in the measurement context circuits, and the trigger and run control circuits.

Schematic 2, check: U65.

Schematic 5, check: U58, U68, U69, U72, U73, U74, U75, U76, U77.

Schematic 7, check: U5, U6, U7.

4-110. TIME, EVENT, AND SEQUENCE COUNTER TEST DISPLAY.

4-111. Purpose. The test shown on this display checks the programmable event counter U60, time counter U61 and sequence counter U62. It also tests the bidirectional data bus transceiver U70 and the statistics I/O decoder U85. The microcontroller sends commands to the programmable counters and reads back counter responses via the microcontroller data bus.

Figure 4-11. Time, Event, and Sequence Counter Test Display

4-112. Running the Time, Event, and Sequence Counter Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Time, Event, and Sequence Counter' and then press the <disp_test> softkey. Next, press the <start> softkey to begin the test. The test continues to run until a softkey is pressed. Each iteration takes less than 3 seconds.

4-113. Reading the Time, Event, and Sequence Test Results. The # Failures column shows the the total number of errors detected during the test. Each error code in the display represents a single failure encountered during the last iteration.

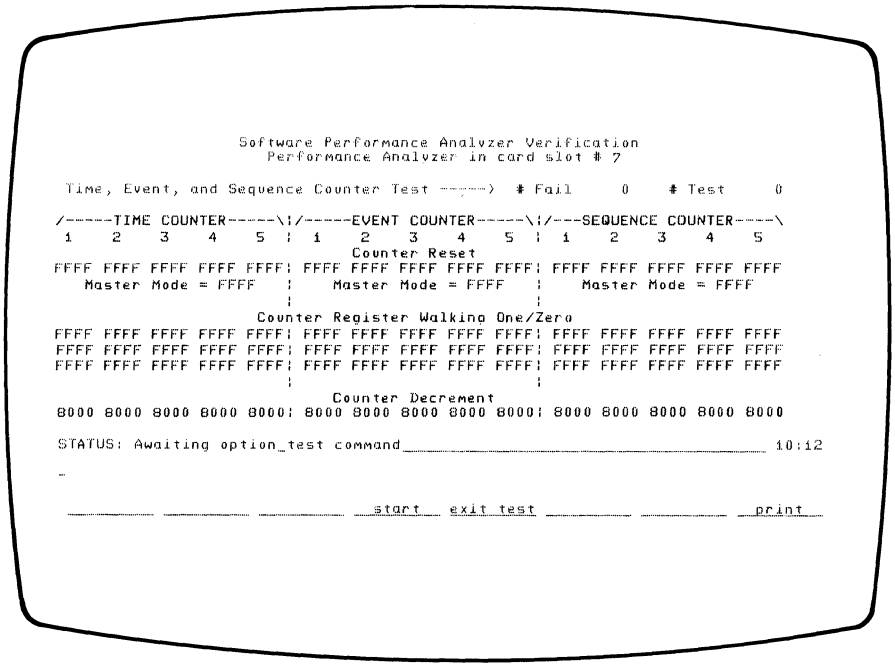


Figure 4-12 a. Sample Transceiver or Decoder Failure

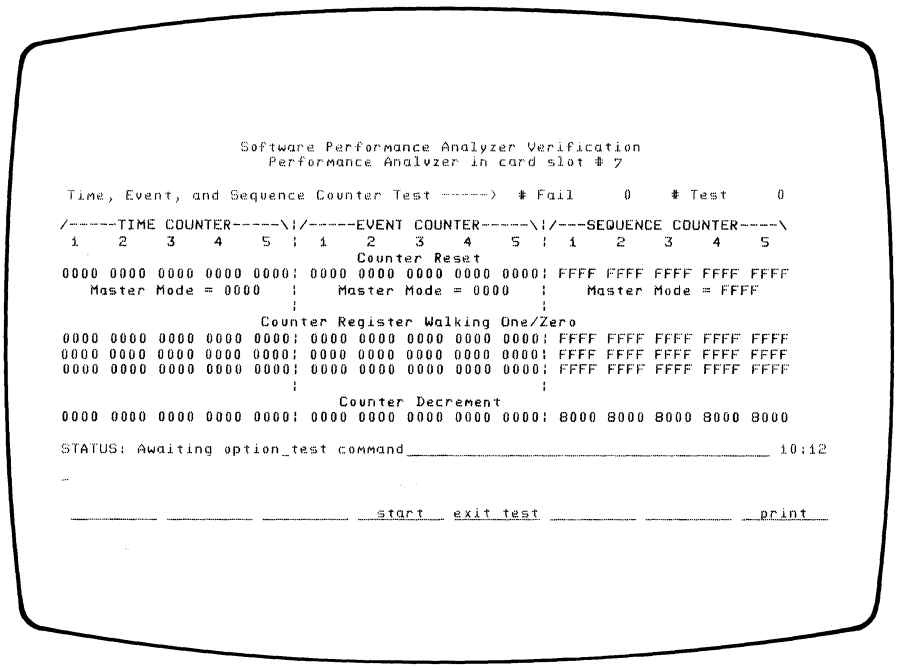


Figure 4-12 b. Sample Counter Failure

4-114. How. First, microprocessor U33 sends a reset command to programmable event counter U60, time counter U61, and sequence counter U62. The counters' internal hold and master mode registers are read and displayed; all bits should be zero after the reset.

4-115. Second, the counters' internal load and mode registers are loaded and read back with the sequence 1, 2, 4, 8, 16, 32, 64, and 128. Any discrepancy between the data written and read back is displayed as an error.

4-116. Third, all counters are loaded with 0FFFFH and configured to count down in binary. The counters are then issued 0FFFDH step commands. The internal hold registers are read and should contain 0002H. Any discrepancy is noted as an error in the display.

4-117. Results. Each character is a hexadecimal digit. Don't be intimidated by all the characters in the display; it is not necessary to decode each one. Look for general patterns. When all characters are zero, there are no test failures.

4-118. When there are non-zero characters in the display, a failure has been detected. Look at the distribution of the characters. When the non-zero characters appear under more than one counter heading, the bidirectional bus transceiver, or the statistics I/O decoder is failing the test. See figure 4-12a for an example.

4-119. When the non-zero characters appear under one counter heading, only the counter is failing the test. See figure 4-12b for an example.

4-120. TIME, EVENT, AND SEQUENCE COUNTER TEST TROUBLESHOOTING.

4-121. Do not attempt to troubleshoot the time, event, and sequence counter test until the mainframe / analyzer interface test and the data acquisition test have been successfully completed. Instructions in the preceding Results paragraphs provide information on how to determine which component is suspect.

4-122. SIGNATURE ANALYSIS - LOOP D.

4-123. Connect the signature analyzer as directed for SA Loop D, in Appendix D. The data acquisition test provides the stimulus and must be running when signatures are taken. Reference schematic 6 in Section VIII. Check the event counter, time counter, sequence counter, data bus transceiver, and statistics I/O decoder.

Schematic 6, check: U60, U61, U62, U70, U85.

4-124. STATISTICS TEST DISPLAY.

4-125. Purpose. The seven tests shown on this display check the statistics interrupt controller U63 and the programmable event counter U60, time counter U61, and sequence counter U62. Each counter has several SOURCE and GATE inputs, and several OUT outputs.

4-126. Under software control, the counters are initialized, and configured to count transitions on a SOURCE input and produce an active OUT after a specified count. The context state flip-flop U56 sends count enable signals to the counters. The active OUT results in an interrupt to interrupt controller U63, which, in turn, sends an IRQ interrupt to the microcontroller.

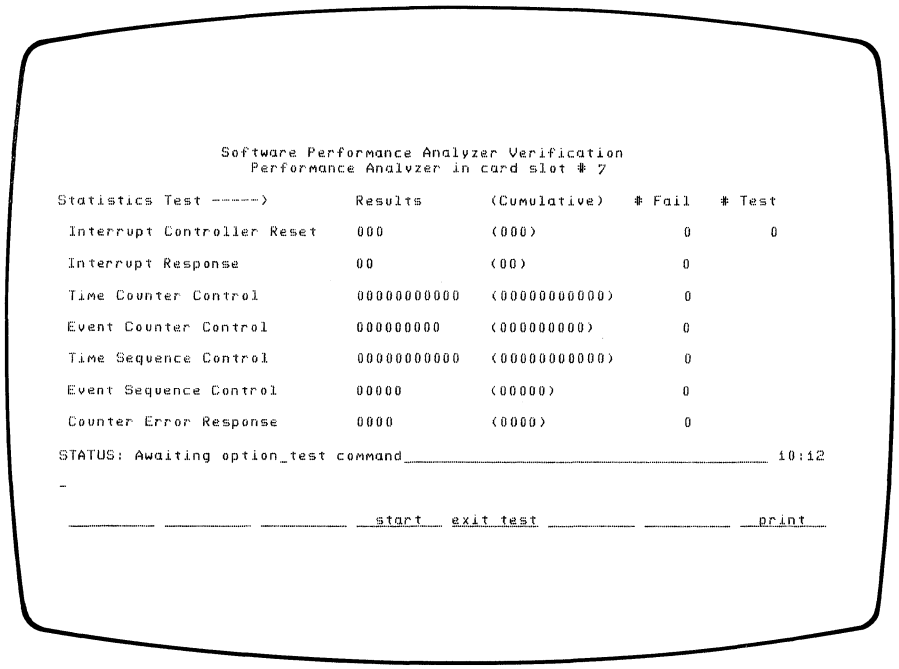


Figure 4-13. Statistics Test Display

4-127. Running the Statistics Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Statistics' and then press the <disp_test> softkey. Next, press the <start> softkey to begin the test. The test continues to run until a softkey is pressed. Each iteration takes less than 1 second.

4-128. Reading the Statistics Test Results. The # Failures column shows the total number of errors detected during the test. Each error code in the present column represents a single failure encountered during the last iteration. The cumulative error code represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-129. INTERRUPT CONTROLLER RESET.

4-130. How. Three test steps are performed in the sequence described below.

1. After interrupt controller U63 is initialized, the internal interrupt register is read; it should be zero.

2. Signal H/CONERR is brought high and the interrupt request register is read; H/DATA6 should be high.

3. On the same read of the interrupt request register, H/TOOFAST is checked; H/DATA7 should be low.

4-131. Results. The error bits are decoded as follows.

Interrrupt Controller Reset.....xxx =

Bits	Test Step in Error
000	None
--1	1
-1-	2
1--	3

4-132. INTERRUPT RESPONSE.

4-133. How. Two test steps are performed in the sequence described below.

1. Processor U33-3 IRQ interrupt is enabled and an IR6 interrupt is sent to controller U63. An IRQ interrupt service routine should be executed by processor U33.

2. All interrupts coming into interrupt controller U63 are masked out. Processor U33-3 IRQ interrupts are enabled and an IR6 interrupt is sent to the controller. An IRQ interrupt routine should not be executed.

4-134. Results. The error bits are decoded as follows.

Interrrupt Response.....xx =

Bits	Test Step in Error
00	None
-1	1
1-	2

4-135. TIME COUNTER CONTROL.

4-136. How. Eleven test steps are performed on time counter U61, in the sequence described below. In each test step, 25MHz is the counting source.

1. Count SOURCE 1 with no gating; H/RUN held high. Causes active OUT 3 and interrupt IR4.

2. Count SOURCE 1 with no gating; H/RUN held high. Causes active OUT 5 and interrupt IR5.

3. Count SOURCE 1 with no gating; H/RUN is held low. The result is an inactive OUT 5 and no interrrupt IR5.

4. Count SOURCE 1, with gating on GATE 3; GATE 3 is held low; H/RUN is held high. The result is an inactive OUT 3 and no interrupt IR4.

5. Count SOURCE 1, with gating on GATE 3; GATE 3 is held high; H/RUN is held high. The result is an active OUT_3 and interrupt IR4.

6. Count SOURCE 2, with no gating; H/RUN and H/GATE B are held high. Causes active OUT 5 and interrupt IR5.

7. Count SOURCE 2, with no gating; H/RUN is held high; H/GATE B is held low. The result is an inactive OUT 5 and no interrupt IR5.

8. Count SOURCE 3, with no gating; H/RUN and H/GATE B are held high. Causes an active OUT 5 and interrupt IR5.

9. Count SOURCE 4, with no gating; H/RUN and H/GATE A are held high. Produces an active OUT 5 and interrupt IR5.

10. Count SOURCE 4, with no gating; H/RUN is held high; H/GATE A is held low. Causes an inactive OUT_5 and no interrupt IR6.

11. Count SOURCE 5 with no gating; H/RUN and H/GATE A are held high. Produces an active OUT 5 and interrupt IR6.

4-137. Results. The error bits are decoded as follows.

Time Counter Control.....xxxxxxxxxxx =

Bits	Test Step in Error
00000000000	None
----------1	1
---------1-	2
--------1--	3
-------1---	4
------1----	5
-----1-----	6
----1------	7
---1-------	8
--1--------	9
-1---------	10
1----------	11

4-138. EVENT COUNTER CONTROL.

4-139. How. Nine test steps are performed on event counter U60, in the sequence described below. In each test step H/PHASE 5 is the counting source.

1. Count SOURCE 1, with no gating. Produces an active OUT 3 and an interrupt IR2.
2. Count SOURCE 1, with no gating. Produces an active OUT 5 and an interrupt IR3.
3. Count SOURCE 1, with high GATE_3. Produces an active OUT 3 and an interrupt IR2.
4. Count SOURCE 2, with no gating; H/GATE B is held high. Produces an active OUT 5 and an interrupt IR3.
5. Count SOURCE 2, with no gating; H/GATE B is held low. Produces inactive OUT 5 and no interrupt IR3.
6. Count SOURCE 3, with no gating; H/GATE B is held high. Produces an active OUT 5 and an interrupt IR3.
7. Count SOURCE 4, with no gating. Produces an active OUT 5 and an IR3. GATE_A should be high.
8. Count SOURCE 4 with no gating and low GATE_A. Produces inactive OUT 5 and no IR3.
9. Count SOURCE 5 with no gating; H/GATE A is held high. Produces an active OUT 5 and an interrupt IR3.

4-140. Results. The error bits are decoded as follows.

Event Counter Control.....xxxxxxxx =

Bits	Test Step in Error
000000000	None
--------1	1
-------1-	2
------1--	3
-----1---	4
----1----	5
---1-----	6
--1------	7
-1-------	8
1--------	9

4-141. TIME SEQUENCE CONTROL.

4-142. How. Eleven test steps are performed on sequence counter (SC) U62, in the order described below. All test steps are performed with time counter U61 counting SOURCE 1; and SC U62 using time-counter OUT 1 as the counting source. Signal H/RUN is held high in all test steps.

1. With no gating; yields an active SC OUT 1 and interrupt IR1.
2. With no gating, yields an active SC OUT 2 and interrupt IR0.
3. With no gating, yields an active SC OUT 3 and interrupt IR3.
4. With no gating, yields an active SC OUT 4 and interrupt IR4.
5. With no gating, yields an active SC OUT 5 and interrupt IR5.
6. Starting SC counting on negative edge of GATE 1. No edge is sent, producing an inactive OUT 1 and no interrupt IR1.
7. Starting SC counting on negative edge of GATE 1. An edge is sent, producing an active OUT 1 and interrupt IR1.
8. Starting SC counting on a high GATE 2. A low on GATE 2 produces an inactive OUT 2 and interrupt IR0.
9. Starting SC counting on a high GATE 2. A high on GATE 2 produces an active OUT 2 and interrupt IR0.
10. Starting SC counting on a high GATE 3. A low on GATE 3 produces an inactive OUT 3 and interrupt IR3.
11. Starting SC counting on a high GATE 3. A high on GATE 3 produces an active OUT 3 and interrupt IR3.

4-143. Results. The error bits are decoded as follows.

Time Sequence Control....xxxxxxxxxxx =

Bits	Test Step in Error
00000000000	None
----------1	1
---------1-	2
--------1--	3
-------1---	4
------1----	5
-----1-----	6
----1------	7
---1-------	8
--1--------	9
-1---------	10
1----------	11

4-144. EVENT SEQUENCE COUNTER.

4-145. How. Five test steps are performed on sequence counter (SC) U62, in the order described below. All test steps are performed with the event U60 counting SOURCE_1 and SC U62 counting event-counter OUT_1. Signal H/PHASE 5 is the counting source in all tests.

1. With no gating, yields an active SC OUT 2 and no interrupt IR1.

2. Starting SC counting on active high GATE 4. A low GATE 4 produces an inactive OUT 4 and no interrupt IR4.

3. Starting SC counting on active high GATE 4. A high GATE 4 produces an active OUT 4 and interrupt IR4.

4. Starting SC counting on active high GATE 5. A low GATE 5 produces an inactive OUT 5 and no interrupt IR5.

5. Starting SC counting on active high GATE 5. A high GATE 5 produces an active OUT 5 and interrupt IR5.

4-146. Results. The error bits are decoded as follows

Event Sequence Counter.....xxxxx =

Bits	Test Step in Error
00000	None
----1	1
---1-	2
--1--	3
-1---	4
1----	5

4-147. COUNTER ERROR RESPONSE.

4-148. How. Four test steps are performed in the order described below.

1. Signal H/OVERFLOW (U7-5) is brought low and the H/TRIGGER flag is reset. H/TRIGGER (U23-9) is read and should be low.

2. The H/TRIGGER flag is set via decoder U24-12. H/TRIGGER is read and should be high.

3. The H/TRIGGER flag is reset via decoder U24-10. The H/TRIGGER flag is then clocked via NOR gate U8-3. H/TRIGGER is read and should be high.

4. Signal H/OVERFLOW is brought low, the H/RUN flag is set, and the H/TRIGGER flag is reset. Then H/OVERFLOW is brought high, clocking the H/TRIGGER flag. H/TRIGGER is read and should be high.

4-149. Results. The error bits are decoded as follows.

Counter Error Response.....xxxx =

Bits	Test Step in Error
0000	None
---1	1
--1-	2
-1--	3
1---	4

4-150. STATISTICS TEST TROUBLESHOOTING.

4-151. Do not attempt to troubleshoot the statistics test until the mainframe / analyzer interface test, the data acquisition test; and time, event, and sequence counter test have been successfully completed. Instructions in the preceding Results paragraphs provide information on how to determine which component is suspect.

4-152. SIGNATURE ANALYSIS - LOOP E.

4-153. Connect the signature analyzer as directed for SA Loop E, in Appendix E. The data acquisition test provides the stimulus and must be running when signatures are taken. Reference schematics 6 and 7 in Section VIII. Check the components in the event, time, and sequence counter circuitry, and the toofast and trigger control logic.

Schematic 6, check: U60, U61, U62, U63, U64, U70, U78, U79, U80, U81, U82, U83, U84, U85.

Schematic 7, check: U5, U8, U19, U23.

4-154. INTER-MODULE BUS TEST DISPLAY.

4-155. Purpose. The test shown on this display checks the analyzer status latch U7, TTL-to-ECL converter U1, active terminator U2, and the ECL-to-TTL converter U3. When no card with IMB capabilites is present in the card cage, this test does not appear.

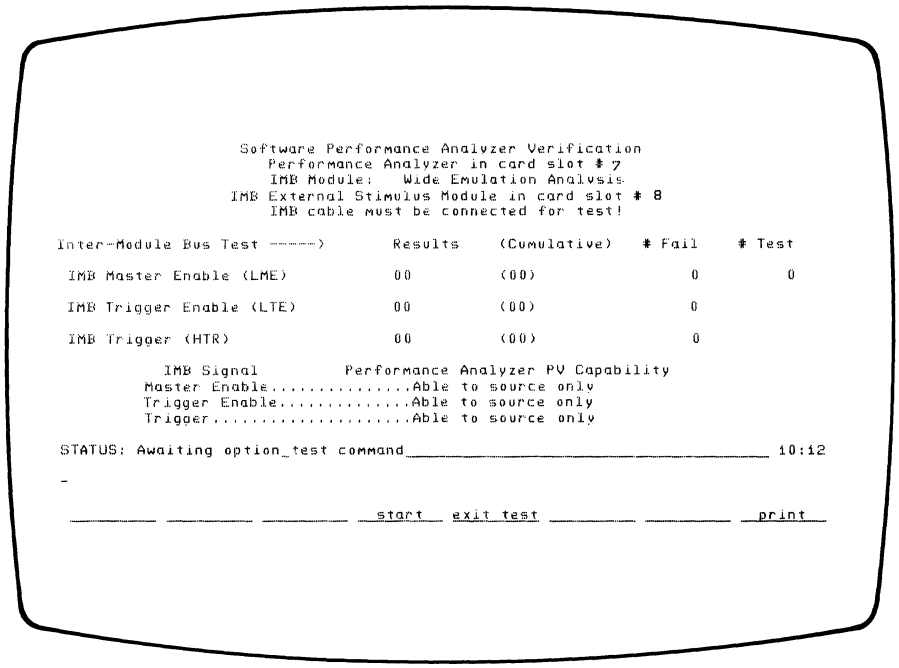


Figure 4-14. Inter-Module Bus Test Display

4-156. Running the Inter-Module Bus Test. To view this test display, begin with the Total PV Display (figure 4-3). Position the highlight line over 'Inter-Module Bus' and then press the <disp_test> softkey. Next, press the <start> softkey to begin the test. The test continues to run until a softkey is pressed. Each iteration takes less than 1 seconds.

4-157. Reading the Inter-Module Bus Test Results. The # Failures column shows the total number of errors detected during the test. Each error code in the present column represents a single failure encountered during the last iteration. The cumulative error code represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-158. Test results are invalid, unless the software performance analyzer inter-module bus is connected by an IMB cable to the option card selected for IMB stimulus.

4-159. IMB MASTER ENABLE.

4-160. How. Two test steps are performed in the sequence described below.

1. The analyzer is configured to drive EL/ME high and the external module reads EL/ME; it should be high. The analyzer is then configured to drive EL/ME low and the external module reads EL/ME (U1-3); it should be low.

2. The analyzer is put into the IMB default mode and the external module reads EL/ME; it should be high.

4-161. Results. The error bits are decoded as follows.

IMB Master Enable .....xx =

Bits	Test Step in Error
00	None
-1	1
1-	2

4-162. IMB TRIGGER ENABLE.

4-163. How. Two test steps are performed in the sequence described below.

1. The analyzer is configured to drive EL/TE high and the external module reads EL/TE; it should be high. The analyzer is then configured to drive EL/TE low and the external module reads EL/TE (U1-12); it should be low.

2. The analyzer is put into the IMB default mode and the external module reads EL/TE; it should be high.

4-164. Results. The error bits are decoded as follows.

IMB Trigger Enable .....xx =

Bits	Test Step in Error
00	None
-1	1
1-	2

4-165. IMB TRIGGER.

4-166. How. Two test steps are performed in the sequence described below.

1. The analyzer is configured to drive EH/TR high and the external module reads EH/TR; it should be high. The analyzer is then configured to drive EH/TR low and the external module reads EH/TR (U1-14); it should be low.

2. The analyzer is put into the IMB default mode and the external module reads EH/TR; it should be high.

4-167. Results. The error bits are decoded as follows.

IMB Trigger .....xx =

Bits	Test Step in Error
00	None
-1	1
1-	2

4-168. INTER-MODULE BUS TEST TROUBLESHOOTING.

4-169. Do not attempt to troubleshoot the inter-module bus test until the mainframe / analyzer interface test, the data acquisition test; the time, event, and sequence counter test; and the statistics test have been sucessfully completed. Instructions in the preceding Results paragraphs provide information on how to determine which component is suspect.

4-170. SIGNATURE ANALYSIS - LOOP F.

4-171. Connect the signature analyzer as directed for SA Loop F, in Appendix F. The data acquisition test provides the stimulus and must be running when signatures are taken. Reference schematic 7 in Section VIII. Check the flip- flops, gates, and TTL/ECL converters in the IMB and control circuits.

Schematic 7, check: U1, U3, U5, U7, U8, U17, U18, U20, U22, U23.

4-172. SOFTWARE PERFORMANCE ANALYZER STIMULUS TEST.

4-173. The software performance analyzer stimulus test is not part of the software performance analyzer PV and cannot be run or viewed while the analyzer PV is running. The analyzer stimulus test is part of emulation software and an emulator must be installed before the test can be executed. Perform all other emulator tests before executing the analyzer stimulus test, or the stimulus test results may be invalid.

NOTE

Do not proceed until all software performance analyzer PV tests have been successfully run. When any of the tests fail, results of the analyzer stimulus test may be invalid.

When running emulation PV, different emulators may display different names for this test, such as analysis test, analyzer stimulus, etc. Test procedures are the same regardless of name.

4-174. To execute the analyzer stimulus test proceed as follows.

a. Exit the software performance analyzer PV.

b. Make certain an emulator is installed. If necessary, refer to the emulator manual for installation instructions.

c. With the operating system initialized and awaiting a command, enter:

option_test [RETURN]

d. The PV now displays a directory of the installed option boards and their card slot numbers. Locate the card slot of the emulator and enter the slot number. For example, if the emulator controller is in slot 9 of the card cage, enter:

9 [RETURN]

e. When the software performance analyzer is the only analysis option in the card cage, the next display shows the emulation tests that can be performed. Position the highlight line over the analyzer stimulus test and press the <disp_test> softkey.

f. When the software performance analyzer is not the only analysis option in the card cage, the display prompts

Select analyzer for test

Enter the card slot of the software performance analyzer; the next display shows the emulator tests that can be performed. Position the highlight line over analyzer stimulus test, and press the <disp_test> softkey.

4-175. ANALYZER STIMULUS TEST DISPLAY.

4-176. Purpose. The tests shown on this display check the emulation bus address latches U12-14, and address range comparators U27-32 and U42-47. The comparator selection circuitry U40, 54, 55, 67 and comparator decoding circuitry U26 and U41 are checked. Also tested are the emulation status bus latch U49 and part of the arming circuit U7 and U20.

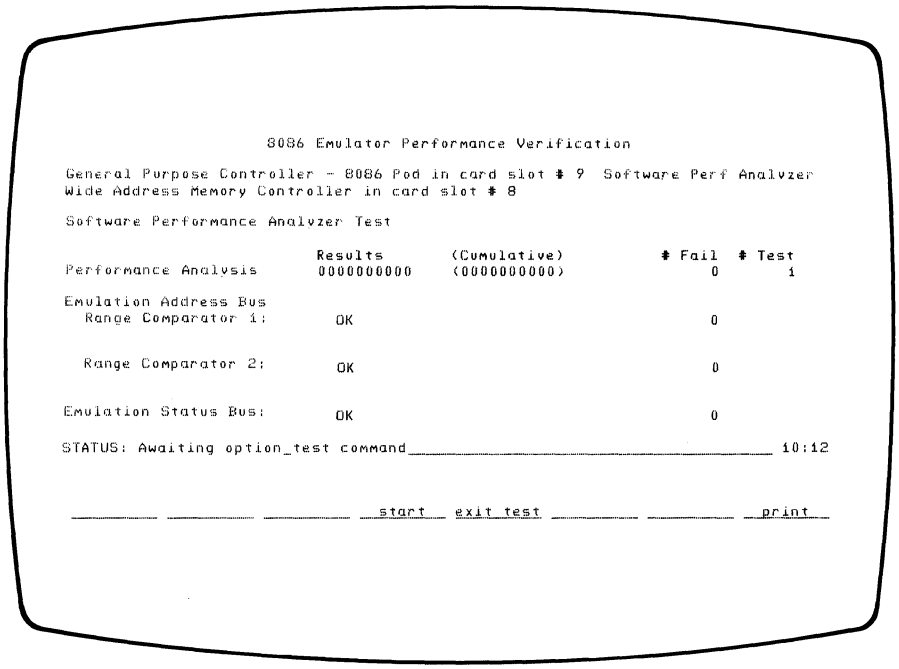


Figure 4-15. Analyzer Stimulus Test Display

4-177. Running the Analyzer Stimulus Test. Begin the emulator PV as directed on the previous page. To view this test display, position the highlight line over 'Analyzer Stimulus' and then press the <disp_test> softkey. Next, press the <start> softkey to begin the test. The test continues to run until a softkey is pressed. Each iteration takes approximately 5 seconds, depending upon the emulator used.

4-178. Reading the Analyzer Stimulus Test Results. The # Failures column shows the total number of errors detected during the test. Each error code in the present column represents a single failure encountered during the last iteration. The cumulative error code represents the sum of all errors detected during the test. Cumulative error codes that differ from error codes in the results column indicate multiple, or intermittent errors. When the error codes are the same, the errors are systematic.

4-179. How. The emulator calls a program that toggles all bits on the emulation bus. Two lists are passed to the analyzer software; one, a list of memory addresses used in the program, and two, a list of status codes generated during the program. Analyzer comparators 1 and 2 are configured to count the memory address occurrences and the emulator is released to loop continuously through the program. When both comparators successfully count occurrences of the expected addresses, the analyzer checks to see that all expected status codes are received. Components tested are shown below.

4-180. PERFORMANCE ANALYSIS.

4-181. Results. This display line is a summary of the emulator address bus test, the status bus test, and some individual tests. Each comparator is tested separately. When both fail, it is likely that the emulator is not operating correctly, or signal L/ANAL is not toggling correctly. The error bits are decoded as follows.

Performance Analysis xxxxxxxxxxx =

Bits	Error
00000000000	None
---------00	Comparator 1, address test summary OK.
---------01	no addresses counted.
---------10	some addresses counted, but not all.
---------11	only invalid addresses counted.
-------00--	Comparator 2, address test summary OK.
-------01--	no addresses counted.
-------10--	some addresses counted, but not all.
-------11--	only invalid addresses counted.
-----00----	Decoder test, comparators 1 and 2 OK.
------1----	U26 pin 1 or 10 or 13 held high.
-----1-----	U41 pin 1 or 4 or 10 held high.
---00------	Pull-up resistor test, OK.
----1------	one of U27 through U32 pin 1 held low.
---1-------	one of U42 through U47 pin 1 held low.
-00--------	Arming test, U7 and U20 OK.
--1--------	U20 pin 6 high, or U7 pin 12 low.
-1---------	U20 pin 8 high, or U7 pin 9 low.
0----------	Status qualifier test OK.
1----------	Status qualifier test failed.

4-182. EMULATION ADDRESS BUS.

4-183. Results. Correct operation is indicated by an OK message. Incorrect operation can produce two different error messages. Each comparator is tested separately; thus, when both fail, it is likely that the emulator is not operating correctly, or signal L/ANAL is not toggling correctly. The error messages are as follows.

a. Cannot count any address !

   Comparator circuitry is unable to count any of the expected addresses.

b. Cannot count address = 000032H !
   Can count address = 000004H

   In this example, the list of expected addresses is checked and 32H is the first address not found. Location 4H is the first address which was found.

4-184. EMULATION STATUS BUS.

4-185. How. When both comparators are successfully tested, the emulation status bus L/ES0-7 is tested. This is done by checking simultaneously for an expected address and its associated emulator processor status code. When both the address and status code cannot be identified, an error is recorded.

4-186. Results.

a. Status qualifier faulty !

   The expected address has been found but the status code associated with the address is not the expected code.

b. Not tested because of Emulation Address Bus Failure !

   The emulation address bus test has failed. No status bus test has been performed.

4-187. ANALYZER STIMULUS TEST TROUBLESHOOTING.

4-188. Do not attempt to troubleshoot the analyzer stimulus test until all the software performance analyzer PV tests have been successfully completed. Instructions in the preceding Results paragraphs provide information on how to determine which component is suspect.

4-189. When the message shown below appears, there is complete failure of both comparator circuits. Check the cabling first, then check for an active L/ANAL. See schematic 3. Check U21-13; it should be toggling. See schematic 7.

Cannot count any address !

4-190. SIGNATURE ANALYSIS - LOOP G. Connect the signature analyzer as directed for SA Loop G, in Appendix G. Reference schematics 3, 4 and 7 in Section VIII. Check the components in the comparator circuits.

Schematic 3, check: U27, U28, U29, U30, U31, U32.

4-191. The signatures are valid whether or not the emulation bus cables are connected. This is because the signature stimulus is provided by the microcontroller, and only control bit signatures are checked. Address lines are stimulated by the emulator, which runs asynchronously to the analyzer.

NOTE

In normal operation, comparators
U27 - U32, and U42 - U47 run hot.

SECTION V

ADJUSTMENTS

There are no adjustments on the Model 64310A Software Performance Analyzer.

SECTION VI

REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information for ordering parts for the Model 64310A Software Performance Analyzer. Table 6-1 lists abbreviations used in the parts list and throughout the manual. Table 6-2 lists all replaceable parts in reference designator order. Table 6-3 contains the names and addresses that correspond to the manufacturers' five digit code numbers.

6-3. ABBREVIATIONS.

6-4. Table 6-1 lists abbreviations used in the parts list, the schematics and throughout the manual. In some cases, two forms of the abbreviation are used: one, all in capital letters, and one partial or no capitals. This occurs because the abbreviations in the parts list are always capitals. However, in the schematics and other parts of the manual, other abbreviation forms are used with both lowercase and uppercase letters.

6-5. REPLACEABLE PARTS.

6-6. Table 6-2, the replaceable parts list, is organized as follows:

a. Chassis mounted parts in alphanumerical order by reference designator.

b. Electrical assemblies and their components in alphanumerical order by reference designator.

c. Miscellaneous parts.

6-7. The total quantity for each part is given only once, at the first appearance of the part number in the list. The information given for each part consists of the following.

a. The Hewlett-Packard part number and the check digit.

b. The total quantity (Qty) in the instrument.

c. The description of the part.

d. A five digit code that indicates the manufacturer.

e. The manufacturer's part number.

6-8. ORDERING INFORMATION.

6-9. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard office.

6-10. To order a part that is not listed in the replaceable parts table, include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard office.

6-11. DIRECT MAIL ORDER SYSTEM.

6-12. Within the USA, Hewlett-Packard can supply parts through a direct mail order system. Advantages of using the system are as follows:

a. Direct ordering and shipment from the HP parts center in Mountain View, California.

b. No maximum or minimum on any mail order. There is a minimum order amount for parts ordered through a local HP office when the orders require billing and invoicing.

c. Prepaid transportation. There is a small handling charge on each order.

d. No invoices - to provide these advantages, a check or money order must accompany each order.

6-13. Mail order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are located at the back of this manual.

6-14. EXCHANGE ASSEMBLIES

6-15. Exchange assemblies are available from the HP Corporate Parts center on a trade in basis. These exchange assemblies, are listed in Table 6-2.

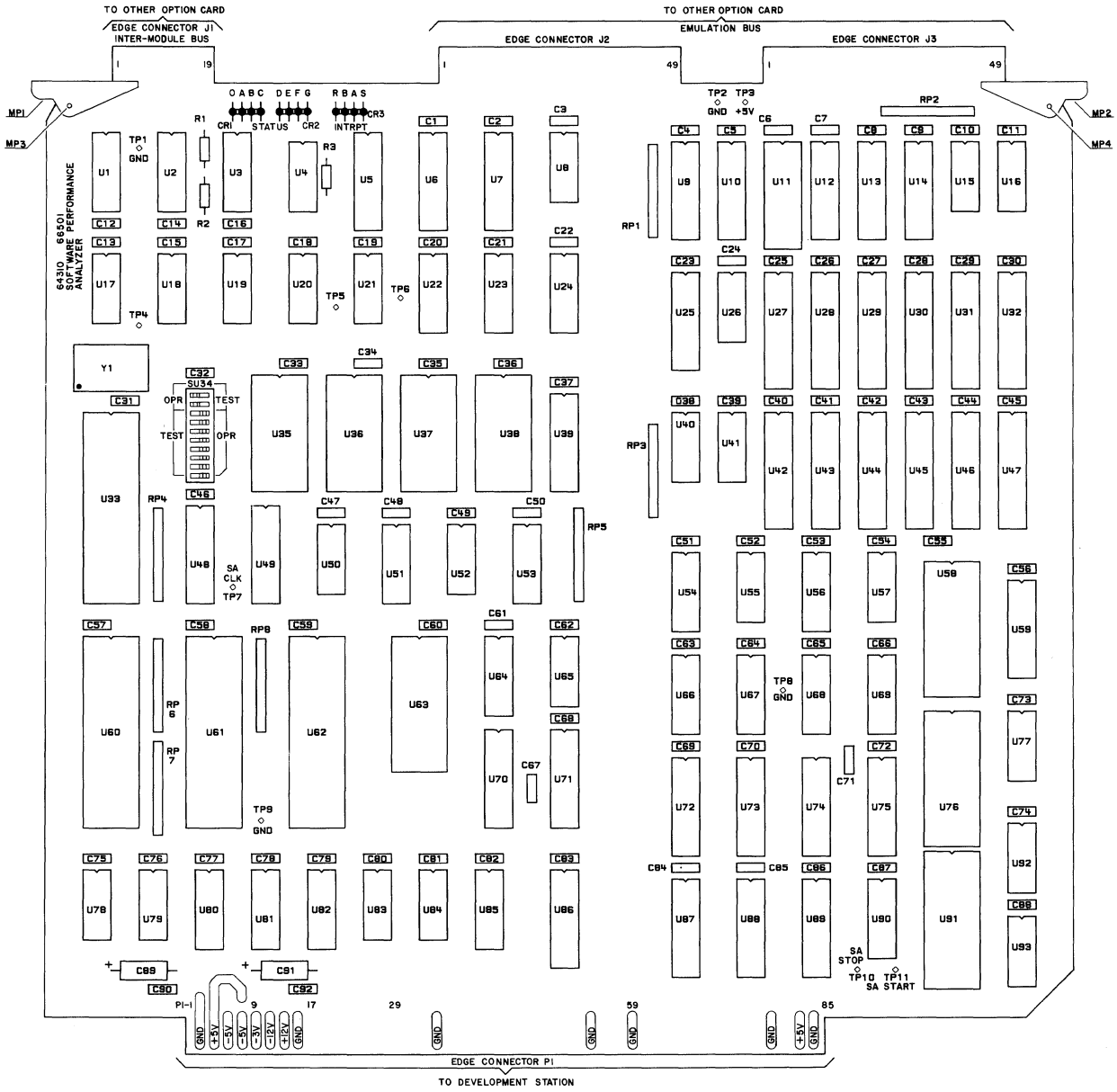


Figure 6-1. Component Locator

Table 6-1. Reference Designators and Abbreviations

REFERENCE DESIGNATORS

A	= assembly	**F**	= fuse	**MP**	= mechanical part	**U**	= integrated circuit
B	= motor	**FL**	= filter	**P**	= plug	**V**	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	**IC**	= integrated circuit	**Q**	= transistor		
C	= capacitor	**J**	= jack	**R**	= resistor	**VR**	= voltage regulator
CP	= coupler	**K**	= relay	**RT**	= thermistor	**W**	= cable
CR	= diode	**L**	= inductor	**S**	= switch	**X**	= socket
DL	= delay line	**LS**	= loud speaker	**T**	= transformer	**Y**	= crystal
DS	= device signaling (lamp)	**M**	= meter	**TB**	= terminal board	**Z**	= tuned cavity network
E	= misc electronic part	**MK**	= microphone	**TP**	= test point		

ABBREVIATIONS

A	= amperes	**H**	= henries	**N/O**	= normally open	**RMO**	= rack mount only
AFC	= automatic frequency control	**HDW**	= hardware	**NOM**	= nominal	**RMS**	= root-mean square
AMPL	= amplifier	**HEX**	= hexagonal	**NPO**	= negative positive zero (zero temperature coefficient)	**RWV**	= reverse working voltage
		HG	= mercury				
BFO	= beat frequency oscillator	**HR**	= hour(s)				
BE CU	= beryllium copper	**HZ**	= hertz	**NPN**	= negative-positive-negative	**S-B**	= slow-blow
BH	= binder head					**SCR**	= screw
BP	= bandpass			**NRFR**	= not recommended for field replacement	**SE**	= selenium
BRS	= brass	**IF**	= intermediate freq			**SECT**	= section(s)
BWO	= backward wave oscillator	**IMPG**	= impregnated	**NSR**	= not separately replaceable	**SEMICON**	= semiconductor
		INCD	= incandescent			**SI**	= silicon
CCW	= counter-clockwise	**INCL**	= include(s)			**SIL**	= silver
CER	= ceramic	**INS**	= insulation(ed)	**OBD**	= order by description	**SL**	= slide
CMO	= cabinet mount only	**INT**	= internal	**OH**	= oval head	**SPG**	= spring
COEF	= coeficient			**OX**	= oxide	**SPL**	= special
COM	= common	**K**	= kilo=1000			**SST**	= stainless steel
COMP	= composition					**SR**	= split ring
COMPL	= complete	**LH**	= left hand	**P**	= peak	**STL**	= steel
CONN	= connector	**LIN**	= linear taper	**PC**	= printed circuit		
CP	= cadmium plate	**LK WASH**	= lock washer	**PF**	= picofarads= 10^{-12} farads	**TA**	= tantalum
CRT	= cathode-ray tube	**LOG**	= logarithmic taper			**TD**	= time delay
CW	= clockwise	**LPF**	= low pass filter	**PH BRZ**	= phosphor bronze	**TGL**	= toggle
				PHL	= phillips	**THD**	= thread
DEPC	= deposited carbon	**M**	= milli=10^{-3}	**PIV**	= peak inverse voltage	**TI**	= titanium
DR	= drive	**MEG**	= meg=10^{6}	**PNP**	= positive-negative-positive	**TOL**	= tolerance
		MET FLM	= metal film			**TRIM**	= trimmer
ELECT	= electrolytic	**MET OX**	= metallic oxide	**P/O**	= part of	**TWT**	= traveling wave tube
ENCAP	= encapsulated	**MFR**	= manufacturer	**POLY**	= polystyrene		
EXT	= external	**MHZ**	= mega hertz	**PORC**	= porcelain	**U**	= micro=10^{-6}
		MINAT	= miniature	**POS**	= position(s)		
F	= farads	**MOM**	= momentary	**POT**	= potentiometer	**VAR**	= variable
FH	= flat head	**MOS**	= metal oxide substrate	**PP**	= peak-to-peak	**VDCW**	= dc working volts
FIL H	= fillister head	**MTG**	= mounting	**PT**	= point		
FXD	= fixed	**MY**	= "mylar"	**PWV**	= peak working voltage	**W/**	= with
						W	= watts
G	= giga (10^{9})	**N**	= nano (10^{-9})	**RECT**	= rectifier	**WIV**	= working inverse voltage
GE	= germanium	**N/C**	= normally closed	**RF**	= radio frequency		
GL	= glass	**NE**	= neon	**RH**	= round head or right hand	**WW**	= wirewound
GRD	= ground(ed)	**NI PL**	= nickel plate			**W/O**	= without

Table 6-2. Replaceable Parts List

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	64310A	7	1	SOFTWARE PERFORMANCE ANALYZER	28480	64310A
	64310-66501	9	1	BOARD ASSEMBLY-STATIC MODULE-NEW	28480	64310-66501
	64310-66501	9	1	BOARD ASSEMBLY-STATIC MODULE-EXCHANGE	28480	64310-69501
C1	0160-5298	8	88	CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C2	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C3	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C4	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C5	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C6	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C7	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C8	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C9	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C10	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C11	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C12	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C13	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C14	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C15	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C16	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C17	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C18	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C19	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C20	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C21	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C22	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C23	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C24	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C25	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C26	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C27	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C28	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C29	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C30	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C31	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C32	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C33	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C34	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C35	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C36	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C37	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C38	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C39	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C40	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C41	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C42	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C43	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C44	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C45	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C46	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C47	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C48	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C49	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C50	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C51	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C52	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C53	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C54	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C55	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C56	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C57	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C58	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C59	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C60	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C61	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C62	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C63	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C64	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C65	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C66	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C67	0160-5298	8		NOT LOADED	28480	0160-5298
C68	0160-5298	8		NOT LOADED	28480	0160-5298
C69	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C70	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C71	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C72	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C73	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C74	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C75	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
C76	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C77	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C78	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C79	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C80	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C81	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C82	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C83	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C84	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C85	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C86	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C87	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C88	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C89	0180-0229	7	2	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C90	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
C91	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C92	0160-5298	8		CAPACITOR FXD CER .01UF 100VDC	28480	0160-5298
CR1	1990-0652	8	3	LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
CR2	1990-0652	8		LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
CR3	1990-0652	8		LED-LAMP ARRAY LUM-INT=200UCD IF=5MA-MAX	28480	1990-0652
MP1	64310-85001	4	1	EXTRACTOR,'64310A'	28480	64310-85001
MP2	64310-85002	5	1	EXTRACTOR,'SW-PERF'	28480	64310-85002
MP3	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP4	1480-0116	8		PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
MP5	7124-0271	8	1	LABEL-ORANGE DOT	85480	QD25 TAPE B-810-OR
R1	0757-0280	3	3	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R3	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
RP1	1810-0280	8	8	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP2	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP3	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP4	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP5	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP6	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP7	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
RP8	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
SW34	3101-2102	6	1	DIP ROCKER SWITCH	28480	3101-2102
TP1	0360-0535	0	11	TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP2	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP3	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP4	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP5	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP6	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP7	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP8	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP9	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP10	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
TP11	0360-0535	0		TERMINAL TEST POINT PCB	00000	ORDER BY DESCRIPTION
U1	1820-1173	1	1	IC XLTR ECL TTL-TO-ECL QUAD 2-INP	04713	MC10124L
U1	1820-2359	7	1	IC MISC ECL 14-INP	07263	F10014PC
U3	1820-1052	5	1	IC XLTR ECL ECL-TO-TTL QUAD 2-INP	04713	MC10125L
U4	1813-0193	8	1	DEL LINE 200NS	07393	TTLDM-200
U5	1820-1917	1	4	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U6	1820-1997	7	12	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U7	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U8	1820-2684	1	3	IC GATE TTL F NAND QUAD 2-INP	07263	74F00PC
U9	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U10	1820-2102	8	1	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U11	1816-1308	5	1	IC-93L422 PC	07263	93L422PC
U12	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U13	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U14	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U15	1820-2686	3	2	IC GATE TTL F AND QUAD 2-INP	07263	74F08PC
U16	1820-2686	3		IC GATE TTL F AND QUAD 2-INP	07263	74F08PC
U17	1820-0682	5	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S03N
U18	1820-2689	6	1	IC GATE TTL F NAND DUAL 4-INP	07263	74F20PC
U19	1820-1203	8	1	IC GATE TTL LS AND TPL 3-INP	01295	SN74LS11N
U20	1820-2684	1		IC GATE TTL F NAND QUAD 2-INP	07263	74F00PC
U21	1820-2685	2	5	IC GATE TTL F NOR QUAD 2-INP	07263	74F02PC
U22	1820-0629	0	5	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U23	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U24	1820-1240	3	7	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U25	1820-1624	7	1	IC BFR TTL S OCTL 1-INP	01295	SN74S241N

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U26	1820-2685	2		IC GATE TTL F NOR QUAD 2-INP	07263	74F02PC
U27	1820-2899	0	12	IC-74AS885	28480	1820-2899
U28	1820-2899	0		IC-74AS885	28480	1820-2899
U29	1820-2899	0		IC-74AS885	28480	1820-2899
U30	1820-2899	0		IC-74AS885	28480	1820-2899
U31	1820-2899	0		IC-74AS885	28480	1820-2899
U32	1820-2899	0		IC-74AS885	28480	1820-2899
U33	1820-2770	6	1	IC-UP 68B09L	28480	1820-2770
U35	64310-80000	3	1	EFROM,BOOT	28480	64310-80000
U36	1818-1611	7	3	IC HM6116P-3	S4013	HM6116P-3
U37	1818-1611	7		IC HM6116P-3	S4013	HM6116P-3
U38	1818-1611	7		IC HM6116P-3	S4013	HM6116P-3
U39	1820-2206	3	2	IC MISC TTL LS	01295	SN74LS640N
U40	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U41	1820-2685	2		IC GATE TTL F NOR QUAD 2-INP	07263	74F02PC
U42	1820-2899	0		IC-74AS885	28480	1820-2899
U43	1820-2899	0		IC-74AS885	28480	1820-2899
U44	1820-2899	0		IC-74AS885	28480	1820-2899
U45	1820-2899	0		IC-74AS885	28480	1820-2899
U46	1820-2899	0		IC-74AS885	28480	1820-2899
U47	1820-2899	0		IC-74AS885	28480	1820-2899
U48	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U49	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U50	1820-1416	5	2	IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U51	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U52	1820-2685	2		IC GATE TTL F NOR QUAD 2-INP	07263	74F02PC
U53	1820-1276	5	1	IC SHF-RGTR TTL LS R-S PRL-IN PRL-OUT	01295	SN74LS194AN
U54	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U55	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U56	1820-2696	5	2	IC FF TTL F D-TYPE POS-EDGE-TRIG COM CLK	07263	74F175PC
U57	1820-1112	8	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U58	64310-80003	6	1	LOGIC ARRAY,MEASUREMENT CONTEXT2	28480	64310-80003
U59	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U60	1820-2604	5	3	IC NMOS 16-BIT	34335	AM9513CC
U61	1820-2604	5		IC NMOS 16-BIT	34335	AM9513CC
U62	1820-2604	5		IC NMOS 16-BIT	34335	AM9513CC
U63	1820-2601	2	1	IC-8259A	28480	1820-2601
U64	1820-2654	5	1	IC MUXR/DATA-SEL TTL F 2-TO-1-LINE QUAD	07263	74F157PC
U65	1820-1197	9	2	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U66	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U67	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U68	1820-2696	5		IC FF TTL F D-TYPE POS-EDGE-TRIG COM CLK	07263	74F175PC
U69	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U70	1820-2206	3		IC MISC TTL LS NOT LOADED	01295	SN74LS640N
U72	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U73	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U74	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U75	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U76	64310-80002	5	1	LOGIC ARRAY,MEASUREMENT CONTEXT1	28480	64310-80002
U77	1820-1416	5		IC SCHMITT-TRIG TTL LS INV HEX 1-INP	01295	SN74LS14N
U78	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U79	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U80	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U81	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U82	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U83	1820-2684	1		IC GATE TTL F NAND QUAD 2-INP	07263	74F00PC
U84	1820-2685	2		IC GATE TTL F NOR QUAD 2-INP	07263	74F02PC
U85	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U86	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U87	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U88	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U89	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U90	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U91	64310-80001	4	1	LOGIC ARRAY,MAINFRAME CONTROL	28480	64310-80001
U92	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U93	1820-0682	5		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S03N
XU33	1200-0654	7	4	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU35	1200-0541	1	4	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU36	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU37	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU38	1200-0541	1		SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
XU58	1200-0553	5	4	SOCKET-IC 28-CONT DIP-SLDR	28480	1200-0553
XU60	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU61	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU62	1200-0654	7		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
XU63	1200-0553	5		SOCKET-IC 28-CONT DIP-SLDR	28480	1200-0553

See introduction to this section for ordering information

Table 6-2. Replaceable Parts List (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
XU76	1200-0553	5		SOCKET-IC 28-CONT DIP-SLDR	28480	1200-0553
XU91	1200-0553	5		SOCKET-IC 28-CONT DIP-SLDR	28480	1200-0553
Y1	1813-0188	1	1	OSC-8.00 MHZ	28480	1813-0188

Table 6-3. List of Manufacturers' Codes

Mfr No.	Manufacturer Name	Address		Zip Code
S4013	HITACHI	TOKYO	JP	
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
07393	COLSON CORP THE	JONESBORO	AR	72401
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247
85480	BRADY W H CO	MILWAUKEE	WI	53209

SECTION VII

MANUAL CHANGES

This section normally contains backdating information for models with repair numbers prior to the one shown on the title page. Because this edition includes only the first repair number, there is no backdating material.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains reference information for servicing the Model 64310A Software Performance Analyzer. For convenience, the schematics, component locator, and other service information are provided on foldout service sheets.

8-3. The following functional blocks implement the operation of the analyzer.

Block	Schematic
Development Station Interface	1
Microcontroller	2
Address Recognition	3, 4
Context Recognition	5
Statistics	6
Control and Timing	7

8-4. GENERAL THEORY.

8-5. Software performance analyzer operation is directed by the microcontroller circuit. The microcontroller consists of a 68B09 microprocessor operated at 8 MHz, 6K bytes of RAM, and 2K bytes of ROM. Software is loaded into the RAM by the development station. The only routines in the ROM are the bootstrap loading, and initial performance verification test.

8-6. The 68B09 microprocessor drives a fourteen bit address bus via a set of buffers. Most of the address lines are used only within the microcontroller circuitry for RAM/ROM addressing. The lowest four address bits and the eight bit data bus also go to other parts of the board. These four address bits and the data bus connect all functional blocks of the board and allows direct I/O to hardware registers by way of decoders. The I/O is memory mapped.

8-7. Address recognition, context recognition, and statistics are done in real-time hardware to measure emulator instruction rates of up to 5 MHz. The address recognition circuit indicates if an address on the emulation bus falls within a specified range. It consists of two circuits that compare the twenty-four bit address with the upper and lower bound of a user specified range. Each comparator circuit produces the signals shown below, for a total of six comparator output bits.

Equal to upper bound. In range. Equal to lower bound.

8-8. The context recognition circuit latches eight emulation status bits. The status bits are checked with a recognition RAM and generate two qualifier bits. The qualifiers distinguish memory access types as shown below and have different bit assignments for different emulators.

Instruction fetch Memory read/write DMA cycle

8-9. The two qualifier bits, six comparator output bits, and measurement mode bits all go into the context recognition state machine which does all of the triggering for the operator specified address ranges, event and trace start and stop, sequences, etc. Programmable logic arrays provide the majority of the circuitry in the state machine.

8-10. Statistical analysis of emulation address states is performed by three AMD9513 programable counters, one for events, one for time, and one for sequence. The programable counters are gated on and off by the context recognition state machine and can collect statistics up to a maximum rate of 7 MHz. This means collection of statistics is as fast as memory cycles on the emulation bus. Time resolution is 160ns. The time reference comes from the development station 25 MHz back plane clock, and is synchronized and divided by four prior to feeding into the time counter.

8-11. The counters are continually building one bar on the occurrence histogram, and one bar on the time histogram. An entire histogram is built by having the 68B09 microprocessor dynamically reprogram the address recognition comparators and accumulate each bar in turn.

8-12. The IMB and control section interfaces the analysis clock L/ANAL and inter-module bus to the 64310A internal control signals. High speed strobe signals, H/PHASE 4 AND H/PHASE 5, cause the various acquisition registers to fire in the proper pipelined fashion. This pipelining allows a new measurement to come in while an old measurement is still being accumulated, thereby giving a 5 MHz acquistion rate, although an entire measurement cycle takes about 350 ns.

8-13. Performance verification circuitry is built-in to allow the 68B09 microprocessor to read/write the six comparator output bits, read the context recognition outputs, and read/write the programable counter registers. This allows the performance verification software to do extensive testing of the board.

8-14. DEVELOPMENT STATION INTERFACE, SCHEMATIC 1.

8-15. All communication between the development station and the analyzer is accomplished via a handshake method using the development station data bit 15. Whenever the development station wants to transfer data to or from the analyzer, it first checks bit 15. When bit L/D15 is clear, the development station reads or writes data from the analyzer interface latches U86, U87, and U88.

8-16. This process sets the H/BPCREQ interrupt to the microcontroller. The microcontroller then recognizes the interrupt and clears it. When the microcontroller is ready for the transfer, it writes its data to the output latch U88. The process of writing the data to the development station clears bit L/D15. When the microcontroller is reading data from the development station latch U87, a dummy write is done to the output latch to clear the handshake bit.

8-17. All of the arbitration for this communication is contained in logic array U91. Synchronization is handled by flip-flop U92 and prevents changing of the handshake bit while the development station is checking status. The development station interface handles any hard resets of the microcontroller via the L/RESET line. This line is always set true at power-up by L/POP and can be set/reset by the development station.

8-18. MICROCONTROLLER, SCHEMATIC 2.

8-19. The heart of the microcontroller is a 68B09 microprocessor with an 8 MHz clock, 6K bytes of RAM, and 2K bytes of ROM. The microcontroller drives a negative true address bus, a positive true data bus to memory, and a negative true data bus to I/O and control. Primary address decoding is handled by decoder U51 and primary data bus driving and inversion is handled by transceiver U39.

8-20. The main purpose of the microcontroller is to handle the hardware configuration for measurements and to accumulate measurement data. All data for a current measurment is maintained by the microcontroller. In this way, the analyzer is able to run and acquire measurement data independent of the development station. The microcontroller recognizes two interrupts, one from the development station for data transfers, and one from the statistics section for measurement end, start, or error. The microcontroller software recognizes the source of the interrupt and acts accordingly.

8-21. Four-bit shift register U53 is a wait-state generator. It is enabled whenever ROM or statistics is addressed by the microprocessor. The wait-state generator is disabled whenever L/RESET is true to allow proper startup of the 68B09 from powerup. Switch SU34 is used for service, and forces an LDA instruction onto the data bus. This causes a constant toggling of the address bits, thus providing a constant stimulus for SA.

8-22. ADDRESS RECOGNITION, SCHEMATICS 3 AND 4.

8-23. The analyzer has the ability to simultaneously recognize two different, twenty-four bit emulation addresses. This is accomplished in two address range comparator circuits. Each circuit consits of six TI AS885 eight-bit comparator chips, organized in two banks of three chips. One bank is programmed for the address range upper bound, and one for the lower bound. By processing the outputs of each bank with NOR gates U26 and U41, the comparator output bits shown below are obtained.

a. H/COMOUT1, 4; emulation address equals upper bound.

b. H/COMOUT2, 5; emulation address is in range.

c. H/COMOUT3, 6; emulation address equals lower bound.

8-24. The range comparators are programmed on a byte-by-byte basis by the microcontroller. Address decoding is handled by decoders U67 and U54. The upper seven bits and the least significant bit can be placed into a don't care condition when the microcontroller writes a pattern to latch U59. The outputs of this latch enable/disable AND gates U15 and U16. This places the inputs of the range comparator into a known state. The microcontroller knows the don't care pattern and handles the addresses accordingly.

8-25. CONTEXT RECOGNITION, SCHEMATIC 5.

8-26. The context recognition section performs all real-time measurement operations. It consists of a context state machine, mode latch, emulation status bits qualifier, and data buffers.

8-27. The heart of this section is the context recognition state machine which consists of logic arrays U76 and U58, state feedback register U68, and state output latch U56. The state machine's registers are cleared whenever the microcontroller programs mode latch U72. The microcontroller addresses the various elements of this section through decoder U69.

8-28. The state machine monitors the L/COMOUT1-6 bits, the two status qualifier bits and mode latch U72. The mode latch is programmed with the measurment request code and logic array select bit. In this way, different sets of equations are selected for the requested measurement. Each logic array holds forty-eight, sixteen-term equations.

8-29. Flip-flop U57 monitors L/COMOUT 4 from comparator 2 to 'memorize' an event occurrence. This is needed for disable conditions because the state machine clock is paused during reprogramming of range comparator 1 for certain types of measurements. This flip-flop is enabled, disabled, and cleared by the microcontroller.

8-30. The state machine outputs are connected to the statistics section, and based on emulation address and status, start, stop, retrigger, and interrupt statistics accumulation.

8-31. The status qualifier consists of RAM U11 which recognizes patterns on the status bus. Only two of the RAM outputs, H/QUAL1,2 are used by the state machine. The RAM is programmed by the microcontroller for the type of measurement requested. The RAM occupies a 256 byte block of write address space in the microcontroller memory.

8-32. Three buffers and one latch are provided in this section for performance verification. Buffer U25, and latch U73 are used to provide microcontroller stimulation of the six comparator output bits. Buffer U25 disables the address recognition section from the comparator output bits. Buffer U75 allows monitoring of the comparator output bits and the status RAM outputs by the microcontroller to check operation of the state machine and its feedback register.

8-33. STATISTICS, SCHEMATIC 6.

8-34. The statistics section handles the real-time data reduction. Depending on the measurement requested, time data, event data, or both are collected. Time data is recorded as counts of 160 ns on counter U61. Events are counted as occurrences of emulation addresses on counter U60. Counter U62 functions as a sequence counter. Each counter is an AMD9513 which contains five 16-bit counters. The counters are configured by the microcontroller to record the statistics as thirty-two bit words.

8-35. The microcontroller addresses the statistics section via decoder U85. The statistics section also has its own bus driver to reduce loading and to invert the data bus. The time reference is supplied by the 25MHz backplane source and is divided by four to produce the 160ns clock. Flip-flops U80, U81, U82 are used for the division, and also provide synchronization with the state machine. The timers are also gated on and off with the L/BKG signal from the emulator to assure they are not running when the emulator is in background.

8-36. The statistics section also contains an interrupt controller that is operated in a polled fashion. The active interrupt is determined by the requested measurement and programmed by the microcontroller. The interrupt acknowledge signal is generated by a software strobed line. Four of the inputs to the interrupt controller are multiplexed by two-to-one selector U64 to allow different measurements to select the interrupts they require.

8-37. Time boundary flip-flops U78 and U79 are connected to the outputs of the time and event counters. They are used when the analyzer is making duration measurements. One flip-flop is set when the lower time boundary is crossed. The outputs are clocked into sequence counter U62 on the rising edge of H/CONEND. By taking the difference between the counts, the period of time the counters were in the programmed range can be determined.

8-38. IMB AND CONTROL, SCHEMATIC 7.

8-39. The IMB and control section generates the pipeline timing and handles all IMB functions. The timing generator produces H/PHASE 4 and H/PHASE 5 signals from the rising edge of L/ANAL. Each phase is a positive going pulse of 80 to 90ns duration. Signal H/PHASE 4 has a 160ns period and clocks the context recognition state machine. Signal H/PHASE 5 has a 200ns period and clocks the event counter.

8-40. The timing generator is turned on and off by the microcontroller. The microcontroller is synchronized to the timing generator by run and go flip- flop U-22. When a run command is issued, U22-5 H/RUN is set high. Signal H/RUN is then gated with IMB signals by NOR gate U18. When all signals are true, then the input on go flip-flop U22-11 is high. On the next rising edge of L/ANAL, U22-9 H/GO goes high. This signal is then inverted by U21 and passed to the delay chip U4.

8-41. Delay chip U4 then generates H/PHASE 4 and H/PHASE 5. The 40% tap on U4, L/GOCLR, is sent back, to reset go flip-flop U22. This clears the flip- flop after a delay of 80ns.

8-42. The IMB functions are limited to the receiving and driving trigger enable, EL/TE. When the analyzer is receiving EL/TE, it is simply used to gate H/RUN on and off. When the analyzer is driving EL/TE, the state of EL/TE is determined by the microcontroller software.

8-43. Signals L/BRK, E/DTR, and EH/TR are never driven, even though there is hardware to do so. Signals H/OVTIME and H/OVCOUNT are always disabled.

NOTE

When an external module is windowing the analyzer, only the occurrence counters are disabled; the timers continue to run.

8-44. There is one latch, half of a buffer, and one gate used for performance verification in this section. Buffer U5 allows the microcontroller to monitor the status of flip-flops U23 and U22, trigger and run signals. Latch U6 is used to drive the analyzer status light array. This latch is directly written to by the microcontroller.

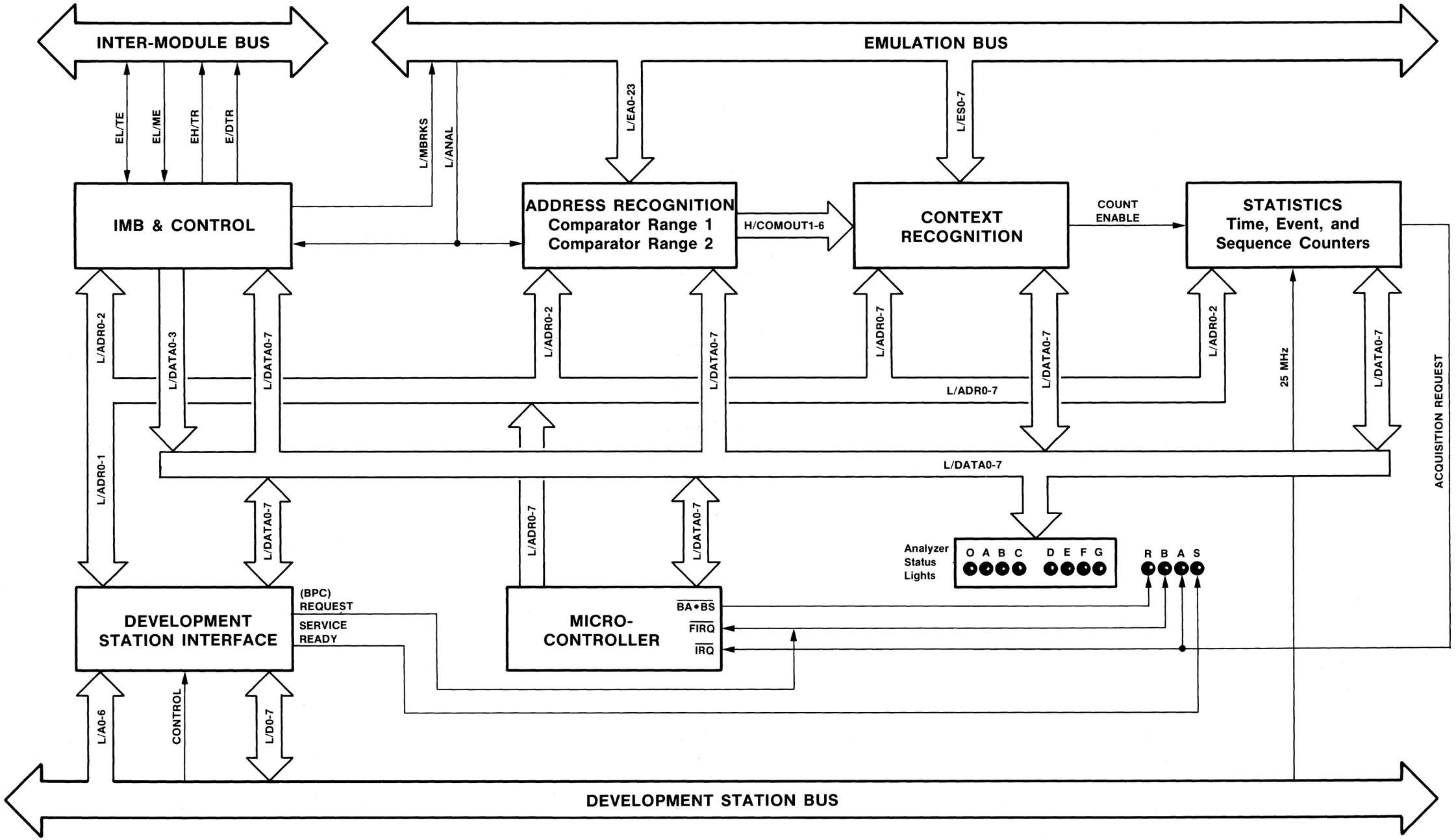


Figure 8-1.
Software Performance Analyzer Block Diagram

Table 8-1. Connector Signals

Connector P1		Connector J1	Connector J2	Connector J3
Schematic 1		Schematic 7	Schematic 5	Schematic 3
Pin		Pin	Pin	Pin
1 gnd	51 L/D14	1 E/GMC	1 L/BRK	1 L/EA0
2 gnd	52 L/D15	2 gnd	2 not used	2 gnd
3 +5v	53 gnd	3 not used	3 gnd	3 L/EA1
4 +5v	54 gnd	4 gnd	4 gnd	4 gnd
5 -5.2v	55 L/HSYN	5 not used	5 L/ED0	5 L/EA2
6 -5.2v	56 L/VSYN	6 gnd	6 L/ED1	6 gnd
7 -5.5v	57 L/VID	7 not used	7 L/ED2	7 L/EA3
8 -5.2v	58 L/IVIDT	8 gnd	8 L/ED3	8 gnd
9 -3.2v	59 gnd	9 E/DTR	9 L/ED4	9 L/EA4
10 -3.2v	60 gnd	10 gnd	10 L/ED5	10 gnd
11 -12v	61 L/BYTE	11 not used	11 L/ED6	11 L/EA5
12 -12v	62 L/UPB	12 gnd	12 L/ED7	12 gnd
13 +12v	63 L/STM	13 EL/ME	13 gnd	13 L/EA6
14 +12v	64 L/STB	14 gnd	14 gnd	14 gnd
15 +17v-ret	65 L/WRT	15 EL/TE	15 L/ED8	15 L/EA7
16 +17v	66 L/MSYN	16 gnd	16 L/ED9	16 gnd
17 +40v	67 L/ID	17 EL/SE	17 L/ED10	17 L/EA8
18 not used	68 L/MAP1	18 gnd	18 L/ED11	18 gnd
19 L/A0	69 L/MAP2	19 EH/TR	19 L/ED12	19 L/EA9
20 L/A1	70 L/MAP3	20 gnd	20 L/ED13	20 gnd
21 L/A2	71 L/IR1		21 L/ED14	21 L/EA10
22 L/A3	72 L/SEL	To Other	22 L/ED15	22 gnd
23 L/A4	73 BNC4	Option Cards	23 gnd	23 L/EA11
24 L/A5	74 L/OPC		24 gnd	24 gnd
25 L/A6	75 BNC3		25 L/EBYT	25 L/EA12
26 L/A7	76 L/POP		26 gnd	26 gnd
27 L/A8	77 BNC2		27 L/EBUP	27 L/EA13
28 L/A9	78 BNC1		28 gnd	28 gnd
29 L/A10	79 gnd		29 L/REFRE	29 L/EA14
30 L/A11	80 gnd		30 gnd	30 gnd
31 L/A12	81 25MHz		31 H/REFAK	31 L/EA15
32 L/A13	82 not used		32 gnd	32 gnd
33 L/A14	83 +5v		33 L/MBRKS	33 L/EA16
34 L/A15	84 +5v		34 gnd	34 L/EA20
35 gnd	85 gnd		35 L/BKG	35 L/EA17
36 gnd	86 gnd		36 gnd	36 L/EA21
37 L/D0			37 not used	37 L/EA18
38 L/D1	To		38 gnd	38 L/EA22
39 L/D2	Development		39 L/ANAL	39 L/EA19
40 L/D3	Station		40 gnd	40 L/EA23
41 L/D4			41 L/ES0	41 H/MAV
42 L/D5			42 L/ES1	42 gnd
43 L/D6			43 L/ES2	43 H/READY
44 L/D7			44 L/ES3	44 gnd
45 L/D8			45 L/ES4	45 L/EWRT
46 L/D9			46 L/ES5	46 gnd
47 L/D10			47 L/ES6	47 L/WDV
48 L/D11			48 L/ES7	48 gnd
49 L/D12			49 gnd	49 H/USER
50 L/D13			50 gnd	50 gnd
			To Other Option Cards	To Other Option Cards

Table 8-2. Mnemonics

Mnemonic	Description
25MHz	25MHz CLOCK. The time reference for the time-counter circuitry in the statistics section. It is the inverted version of L/25MHz. Schematics 1*, 6.
BH/COMOUT1-6	BUFFERED HIGH COMPARATOR OUTPUT BUS. The buffered version of H/COMOUT1-6. The buffered bus allows the comparators to be disconnected from the context recognition circuitry during PV testing. Schematic 5.
EH/DTR	ECL HIGH DRIVE TRIGGER. Not Used. Schematic 7.
EH/TR	ECL HIGH TRIGGER. Not used in normal operation. Driven in PV testing. Schematic 7.
EL/ME	ECL LOW MASTER ENABLE. Not used in normal operation. Driven in PV testing. Schematic 7.
EL/TE	ECL LOW TRIGGER ENABLE. Inter-module bus (IMB) signal that is both driven and received by the analyzer. When driven, it enables another module to look for its trigger. When received, the analyzer is enabled to look for its trigger. Schematic 7.
H/ACQREQ	HIGH ACQUISITION REQUEST. An signal generated by interrupt controller U63 that causes an interrupt of microprocessor U33. Schematics 2, 6*.
H/ARM	HIGH ARM. Input to the H/GO flip-flop that indicates the analyzer is ready to begin data acquisition. Schematic 7
H/BPCREQ	HIGH BPC REQUEST. Indicates the development station is requesting a data transfer with the analyzer. It is derived from development station control signals by logic array chip U91. Schematics 1*, 2.
H/BREAK	HIGH BREAK. Emulator control bit. Not used. Schematic 7.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
H/COMOUT1-3	HIGH COMPARATOR OUTPUT BUS 1-3. Address range 1 comparator output. Bit one idicates the emulator address is equal to the upper bound of the specified range. Bit two means the emulator address is within the range, and bit three indicates the address is equal to the lower bound. Schematics 3*, 5.
H/COMOUT4-6	HIGH COMPARATOR OUTPUT BUS 4-6. Address range 2 comparator output. Bit one idicates the emulator address is equal to the upper bound of the specified range. Bit two means the emulator address is within the range, and bit three indicates the address is equal to the lower bound. Schematics 4*, 5.
H/CONERR	HIGH CONTEXT ERROR. Indicates the context recognition circuitry has detected an error. Schematics 5*, 6.
H/DATA0-7	HIGH DATA BUS 0-7. Microcontroller data bus 0-7. When inverted, becomes L/DATA0-7. Schematics 2*, 6*.
H/GATEA	HIGH GATE A. Output from the context recognition circuit that is a counting source for event counter U60. Schematics 5*, 6.
H/GATEB	HIGH GATE B. Output from the context recognition circuit that is a counting source for event counter U60. Schematics 5*, 6.
H/GO	HIGH GO. Indicates the analyzer is in the measurement mode. Schematic 7.
H/ID	HIGH IDENTIFICATION. Output from logic array U91. Places board ID on the development station L/D0-7 data bus. Schematic 1.
H/INCLK	HIGH DATA-IN CLOCK. Output from logic array U91. Clocks data-in latch U87 when the development station is sending data to the analyzer. Schematic 1.
H/OUTCLK	HIGH DATA-OUT CLOCK. Output from the interface I/O decoder U90. Clocks data-out latch U88 when the analyzer is getting ready to send data to the development station. Schematic 1.
H/OVERFLOW	HIGH OVERFLOW. Control bit output from analyzer status latch U7 that clears the trigger flip-flop. Schematic 7.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
H/PHASE4	HIGH PHASE 4. Output of delay line U4 that clocks the context state flip-flop. Schematics 5, 7*.
H/PHASE5	HIGH PHASE 5. Output of delay line U4 that controls the source input of the even counter. Schematics 6, 7*.
H/PVTEST	HIGH PERFORMANCE VERIFICATION TEST. Output from mode latch U72 that enables various latches and buffer during performance verification testing. Schematic 5.
H/QUAL1-2	HIGH STATUS QUALIFIER BITS. Each bit indicates that the emulator status matches the specified condition. Bit one is for comparator range 1, and bit two is for comparator range 2. Schematic 5.
H/RUN	HIGH RUN. Indicates the analyzer is running. Schematics 6, 7*.
H/SERRDY	HIGH SERVICE READY. Indicates the analyzer is ready to transfer data with the development station. Schematic 1.
H/SERVICE	HIGH SERVICE. Indicates the development station is requesting a data transfer. Schematic 1.
H/STATE1-4	HIGH CONTEXT STATE BITS. Feedback bits in the context recognition circuit state machine. Schematic 5.
H/TOOFAST	HIGH TOO FAST. Indicates the emulator is running too fast for software analysis. Schematics 6, 7*.
H/TRIGGER	HIGH TRIGGER. Output of flip-flop U23 that controls the trigger signals on the inter-module bus (IMB). Schematic 7.
L/ACQ	LOW ACQUISITION. Output from the master I/O decoder U51 that enables the comparator and context recognition I/O decoders. Schematics 2*, 3, 4, 5.
L/ACQCLR	LOW ACQUISITION CLEAR. Output from the context I/O decoder U69 that clears the time and event counter flip-flops. Schematics 5*, 6.
L/ADR0-12	LOW ADDRESS BUS 0-12. Microcontroller address bus. Uses negative logic: high = 0, low = 1. Schematics 1, 2*, 3, 4, 5, 6.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
L/ANAL	LOW ANALYSIS. Signals the analyzer that the emulation bus contains a valid emulation state. It is driven by the emulator. Schematics 3, 5*, 7.
L/BPC	LOW BPC. Output from master I/O decoder U51 that enables the interface I/O decoder for data transfer with the development station. Schematics 1, 2*.
L/CONEND	LOW CONTEXT END. Output from the context recognition circuitry that gates operation of the time, event and sequence counters. Schematics 5*, 6.
L/CTL	LOW CONTROL. Output from the master I/O decoder U51 that enables the IMB and control decoder U24. Schematics 2*, 7.
L/DATA-IN	LOW DATA-IN. Enables the data-in latch U87 when the development station is sending data to the analyzer. Schematic 1.
L/DATA-OUT	LOW DATA-OUT. Enables the data-out latch U88 when the analyzer is sending data to the development station. Schematic 1.
L/DATA0-7	LOW DATA BUS 0-7. Microcontroller data bus. Uses negative logic: high = 0, low = 1. Schematics 1*, 2*, 3, 4, 5*, 6*, 7*.
L/EA0-23	LOW EMULATOR ADDRESS BUS 0-23. Emulator address bus that is monitored by the analyzer. Uses negative logic: high = 0, low = 1. Schematic 3.
L/EN1-6	LOW ENABLE COMPARATOR BITS 1-6. Enables the six comparators in address range 1. Schematic 3.
L/EN7-12	LOW ENABLE COMPARATOR BITS 7-12. Enables the six comparators in address range 2. Schematic 4.
L/ES0-7	LOW EMULATOR STATUS BUS 0-7. Emulator status bus that is monitored by the analyzer. Uses negative logic: high = 0, low = 1. Schematic 5.
L/GATEA	LOW GATE A. Output from the context recognition circcit that is a counting source for time counter U60. Schematics 5*, 6.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
L/GATEB	LOW GATE B. Output from the context recognition circuit that is a counting source for time counter U60. Schematics 5*, 6.
L/GOCLR	LOW GO CLEAR. Output from delay chip U4 that clears the go flip-flop. Schematic 7.
L/INTACK	LOW INTERRUPT ACKNOWLEDGE. Output from the IMB and control decoder U24 that indicates to the interrupt controller U63 that the microprocessor is ready to service the interrupt. Schematics 6, 7*
L/INTCLR	LOW INTERRUPT CLEAR. Output from the interface I/O decoder U90 that indicates the development station interrupt to transfer data is complete. Schematic 1.
L/MBRKS	LOW MEMORY BREAK STATUS. Emulation bus bit driven by the analyzer that controls emulation memory breaks. Schematic 5, 7*.
L/MODE1-6	LOW MODE BITS 1-6. Output from mode latch U72 that controls the context logic arrays. Schematic 5.
L/MODE4	LOW MODE BIT 4. Output from mode latch U72 that controls the sequence count flip-flops. Schematics 5*, 6.
L/MODECLK	LOW MODE CLOCK. Output from the context I/O decoder U69 that clocks the mode latch and clears the context state flip-flops. Schematic 5.
L/MSTCLK	LOW MASTER CLOCK. A clock signal derived from the microprocessor internal clock. It is used to enable the comparator I/O decoders. Schematics 2*, 3, 4.
L/OPR	LOW OPERATION. Output from the interface I/O decoder U90 that enables the operation latch when the development station is sending an operation instruction to the analyzer. Schematic 1.
L/OVCOUNT	LOW OVER COUNT. Not used. Schematics 6*, 7.
L/OVTIME	LOW OVER TIME. Not used. Schematics 6*, 7.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
L/PVTEST	LOW PERFORMANCE VERIFICATION TEST. An inverted version of H/PVTEST that enables various latches and buffers during performance verification testing. Schematic 5.
L/PVTEST1	LOW PERFORMANCE VERIFICATION TEST 1. Output from context I/O decoder U69 that enables buffer U5 to place control bits on the L/DATA bus. Schematics 5*, 7.
L/PVTEST2	LOW PERFORMANCE VERIFICATION TEST 2. Output from context I/O decoder U69 that enables buffer U75 to place comparator output, and status qualifier bits on the L/DATA bus. Schematic 5.
L/PVTEST3	LOW PERFORMANCE VERIFICATION TEST 3. Output from context I/O decoder U69 that enables buffer U74 to place context state bits on the L/DATA bus. Schematic 5.
L/RAM1-3	LOW RAM BITS 1-3. Output from master I/O decoder U51 that enables RAMs U38, U37, and U36. Schematic 2.
L/RESET	LOW RESET. Output from logic array U91 that resets the analyzer. Schematics 1*, 2, 7.
L/ROM	LOW ROM. Output from master I/O decoder U51 that enables ROM U35. Schematic 2.
L/RUN	LOW RUN. Not used. Schematic 6.
L/STATCLK	LOW STATUS BUFFER CLOCK. Output derived from the microprocessor internal timing and address lines that clocks status RAM buffer U10. Schematics 2*, 5.
L/STATIO1-8	LOW STATISTICS INPUT-OUTPUT BITS 1-8. Output bits from the statistics I/O decoder U85 that control the read and writer operations of the time, even, and sequence counter and the interrupt controller. Schematic 6.

Table 8-2. Mnemonics (Cont'd)

Mnemonic	Description
L/STATS	LOW STATISTICS. Output from the master I/O decoder U51 that enables the data bus transceiver U70, and statistics I/O decoder U85. Schematics 2*, 6.
L/STATWRT	LOW STATISTICS WRITE. Output derived from the microprocessor internal timing and address lines that enables read and write operations on status RAM U11. Schematics 2*, 5.
L/STEP	LOW STEP. Output from the IMB and control decoder U24 that controls the time event, and sequence counters, during 'step' mode operation. Schematics 6, 7*.
L/WRITE	LOW WRITE. Output derived from the microprocessor internal timing and read/write lines that enables most I/O sections. Schematics 1, 2*, 5, 6, 7.
L/WRTCLK	LOW WRITE CLOCK. Output derived from the microprocessor internal timing and read/write lines that clocks RAMs U36, U37, and U38. Schematic 2.
LL/DATA0-7	LATCHED, LOW DATA BUS 0-7. Latched version of the microcontroller L/DATA bus. It is used to set emulator address 'don't care' bits. Schematic 3.
LL/EA0-23	LATCHED, LOW EMULATOR ADDRESS BUS 0-23. Latched version of the emulator address bus; it is the input to the address comparators. Schematics 3*, 4.
LL/ES0-7	LATCHED, LOW EMULATOR STATUS BUS 0-7. Latched version of the emulator status bus; it is the input to the emulator status RAM U11. Schematic 5.

Table 8-3. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

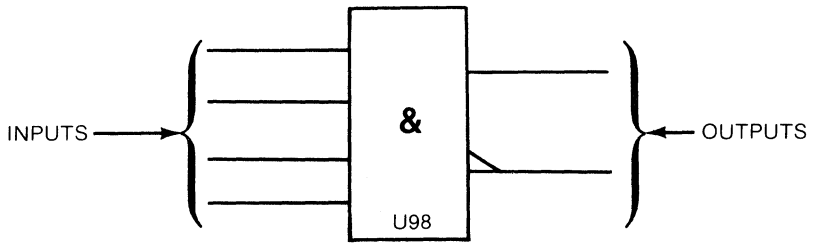
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

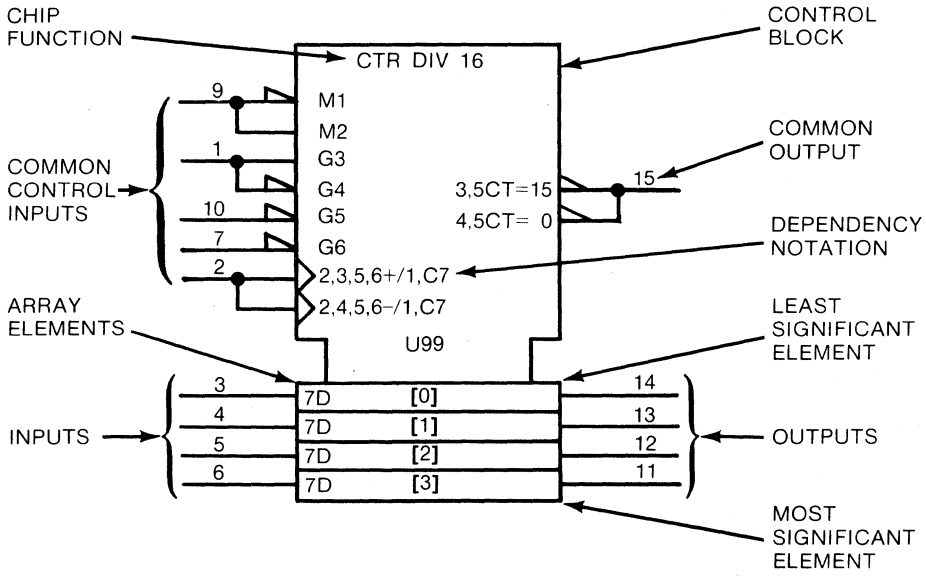
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in **[ ]**).

LS-08-09-82 - 1

Table 8-3. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D....C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.

b. Interconnection (Z) indicates connections inside the symbol.

c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.

d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.

e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).

f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.

g. Address (A) identifies the address inputs.

h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

LS-08-09-82 - 2

Table 8-3. Logic Symbols (Cont'd)

OTHER SYMBOLS

Analog Signal	Inversion	Shift Right (or down)
& AND	O Negation	/ Solidus (allows an input or output to have more than one function)
Bit Grouping	Nonlogic Input/Output	▽ Tri-State
Buffer	Open Circuit (external resistor)	, Causes notation and symbols to effect inputs/outputs in an AND relationship, and to occur in the order read from left to right.
! Compare	Open Circuit (external resistor)	( ) Used for factoring terms using algebraic techniques.
Dynamic	≥1 OR	[ ] Information not defined.
=1 Exclusive OR	Passive Pull Down (internal resistor)	Φ Logic symbol not defined due to complexity.
Hysteresis	Passive Pull Up (internal resistor)	
? Interrogation	Postponed	
Internal Connection	Shift Left (or up)	

LABELS

BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	–	Count Down

MATH FUNCTIONS

Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS

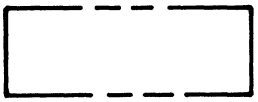
BCD	Binary Coded Decimal	DIR	Directional	RAM	Random Access Memory
BIN	Binary	DMUX	Demultiplexer	RCVR	Line Receiver
BUF	Buffer	FF	Flip-Flop	ROM	Read Only Memory
CTR	Counter	MUX	Multiplexer	SEG	Segment
DEC	Decimal	OCT	Octal	SRG	Shift Register

DELAY and MULTIVIBRATORS

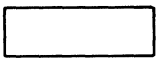
	Astable
100 ns	Delay
1	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable

LS-08-09-82 - 3

Table 8-4. Schematic Diagram Notes



ETCHED CIRCUIT BOARD



FRONT PANEL MARKING

REAR-PANEL MARKING

MANUAL CONTROL

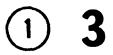
SCREWDRIVER ADJUSTMENT

ELECTRICAL TEST POINT
TP (WITH NUMBER)

NUMBERED WAVEFORM
NUMBER CORRESPONDS TO
ELECTRICAL TEST POINT NO.

LETTERED TEST POINT
NO MEASUREMENT AID
PROVIDED

COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.



NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION.
LARGE NUMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.

CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.

(925) WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE

[(925) IS WHT-RED-GRN]

0 - BLACK	5 - GREEN
1 - BROWN	6 - BLUE
2 - RED	7 - VIOLET
3 - ORANGE	8 - GRAY
4 - YELLOW	9 - WHITE

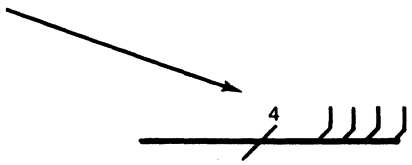
* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.

UNLESS OTHERWISE INDICATED:
RESISTANCE IN OHMS
CAPACITANCE IN PICOFARADS
INDUCTANCE IN MICROHENRIES

μP	=	MICROPROCESSOR
P/O	=	PART OF
NC	=	NO CONNECTION
CW	=	CLOCKWISE END OF VARIABLE RESISTOR

INDICATES SINGLE SIGNAL LINE

NUMBER OF LINES ON A BUS

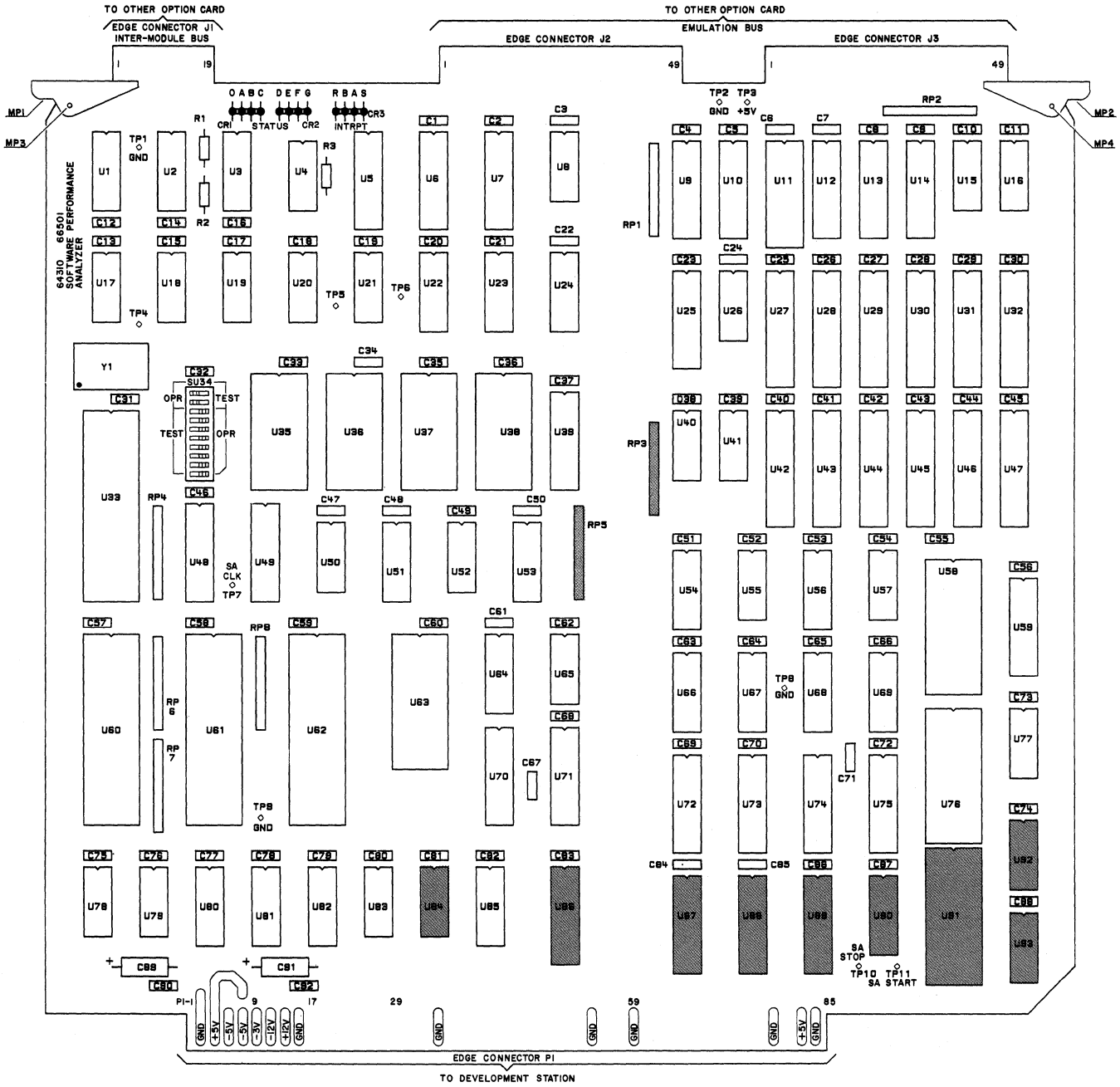


STD-20-09-81

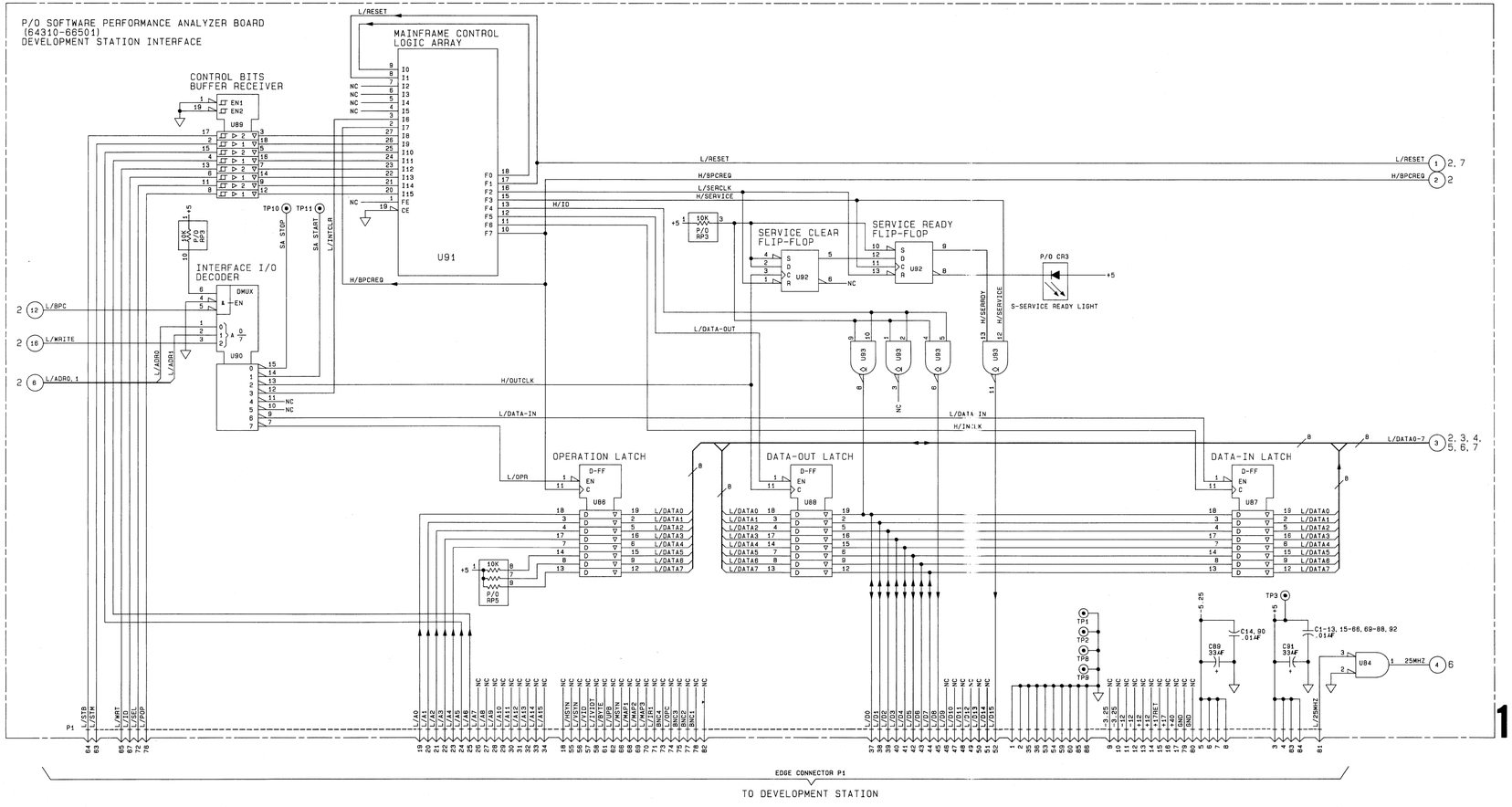
Table 8-5. IC to Schematic Cross-Reference

IC	Schematic
U1	7
U2	7
U3	7
U4	7
U5	7
U6	7
U7	7
U8	7
U9	5
U10	5
U11	5
U12	3
U13	3
U14	3
U15	3
U16	3
U17	7
U18	7
U19	7
U20	7
U21	7
U22	7
U23	7
U24	7
U25	5
U26	3
U27	3
U28	3
U29	3
U30	3
U31	3
U32	3
U33	2
SU34	2
U35	2
U36	2
U37	2
U38	2
U39	2
U40	4
U41	4, 5
U42	4
U43	4
U44	4
U45	4
U46	4
U47	4
U48	2
U49	2
U50	2, 5
U51	2
U52	2
U53	2
U54	4
U55	3
U56	5
U57	5
U58	5
U59	3
U60	6
U61	6
U62	6
U63	6
U64	6
U65	2
U66	2
U67	3
U68	5
U69	5
U70	6
U71	NA
U72	5
U73	5
U74	5
U75	5
U76	5
U77	2, 5
U78	6
U79	6
U80	6
U81	6
U82	6
U83	6
U84	1, 6
U85	6
U86	1
U87	1
U88	1
U89	1
U90	1
U91	1
U92	1
U93	1
Y1	2

NOTES



Component Locator



ICs ON SCHEMATIC 1

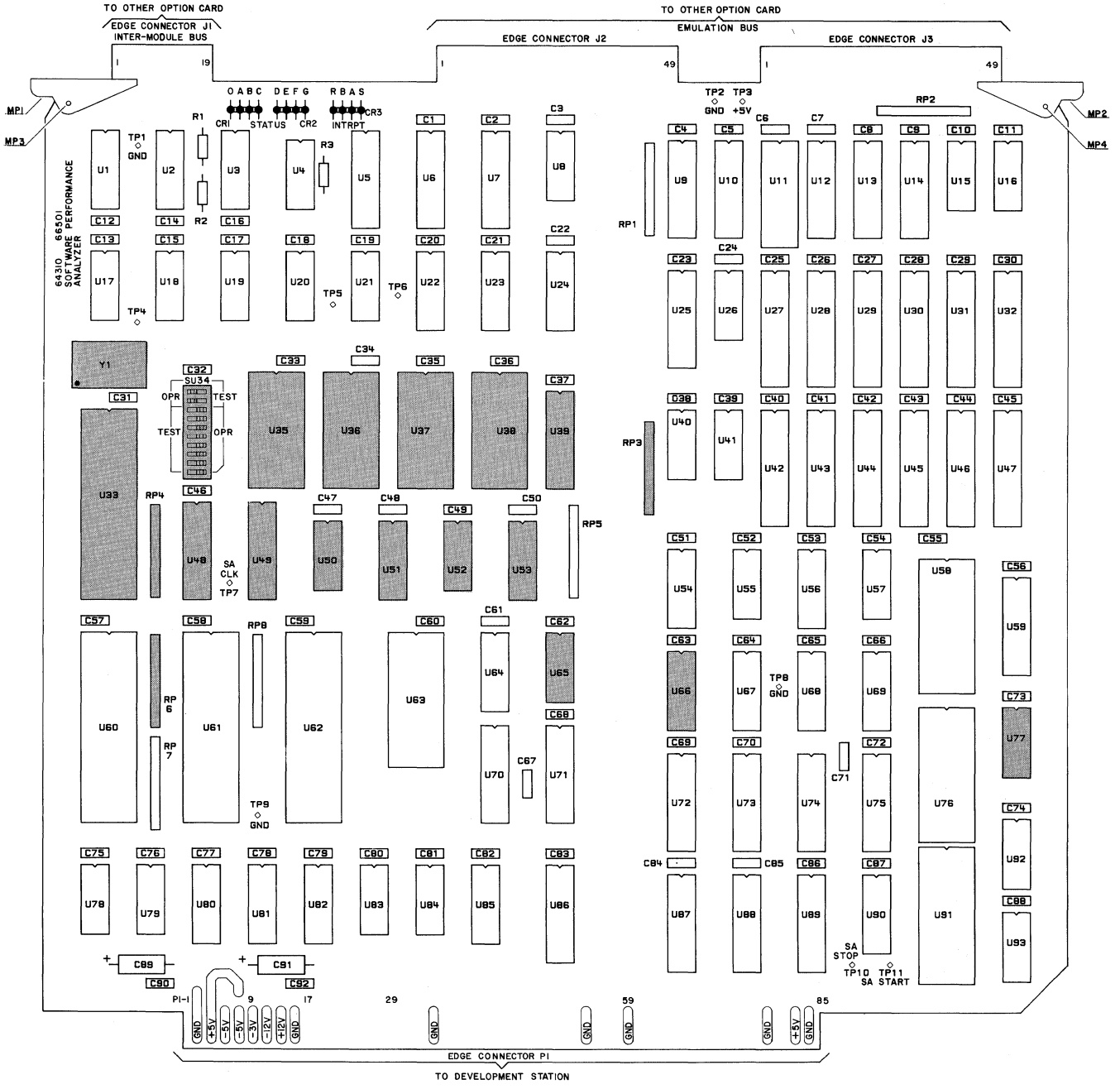
REF DES	HP PART NUMBER	MFG PART NUMBER	+5V PIN	GND PIN
U84	1820-2685	74F02PC	14	7
U86	1820-1997	SN74LS374N	20	10
U87	1820-1997	SN74LS374N	20	10
U88	1820-1997	SN74LS374N	20	10
U89	1820-1917	SN74LS240N	20	10
U90	1820-1240	SN74S138N	16	8
U91	64310-80001	64310-80001	28	14
U92	1820-1112	SN74LS74AN	14	7
U93	1820-0682	SN74S03N	14	7

PARTS ON SCHEMATIC 1

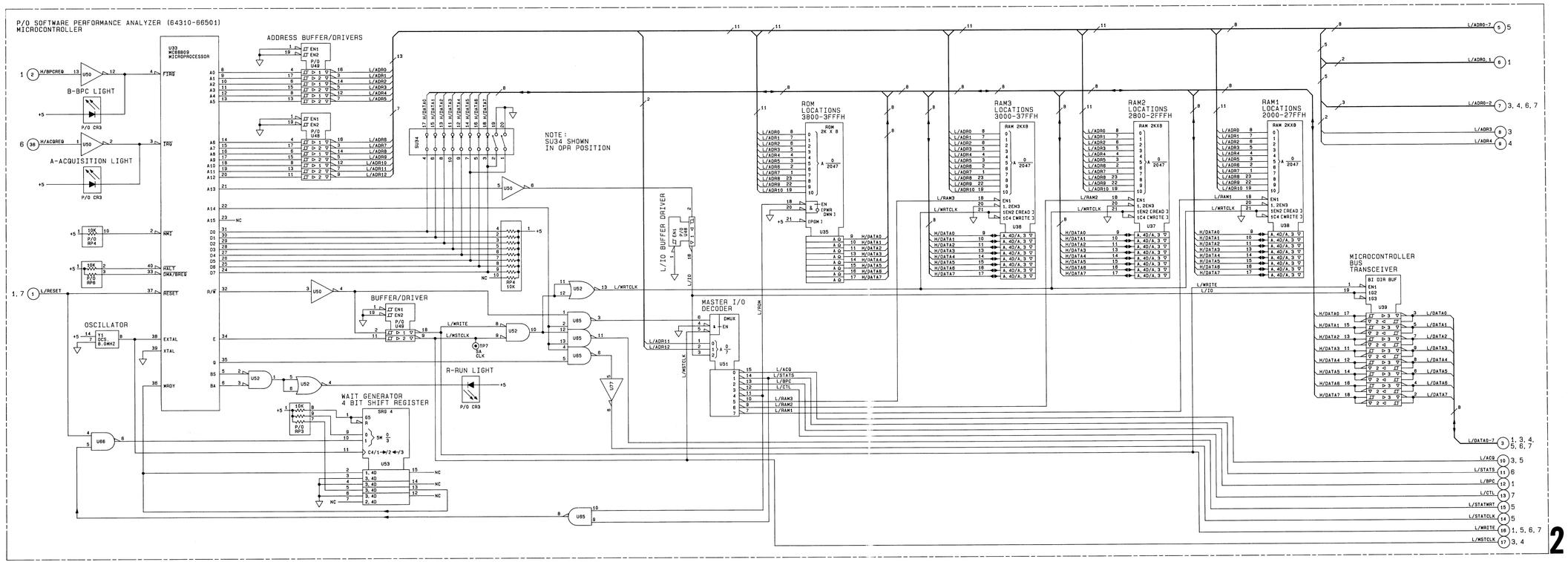
C1-66, C69-92. CR3. RP3, RP5.

TP1,2,3,4,8,9,10,11.

Figure 8-2. Schematic 1
Development Station Interface



Component Locator



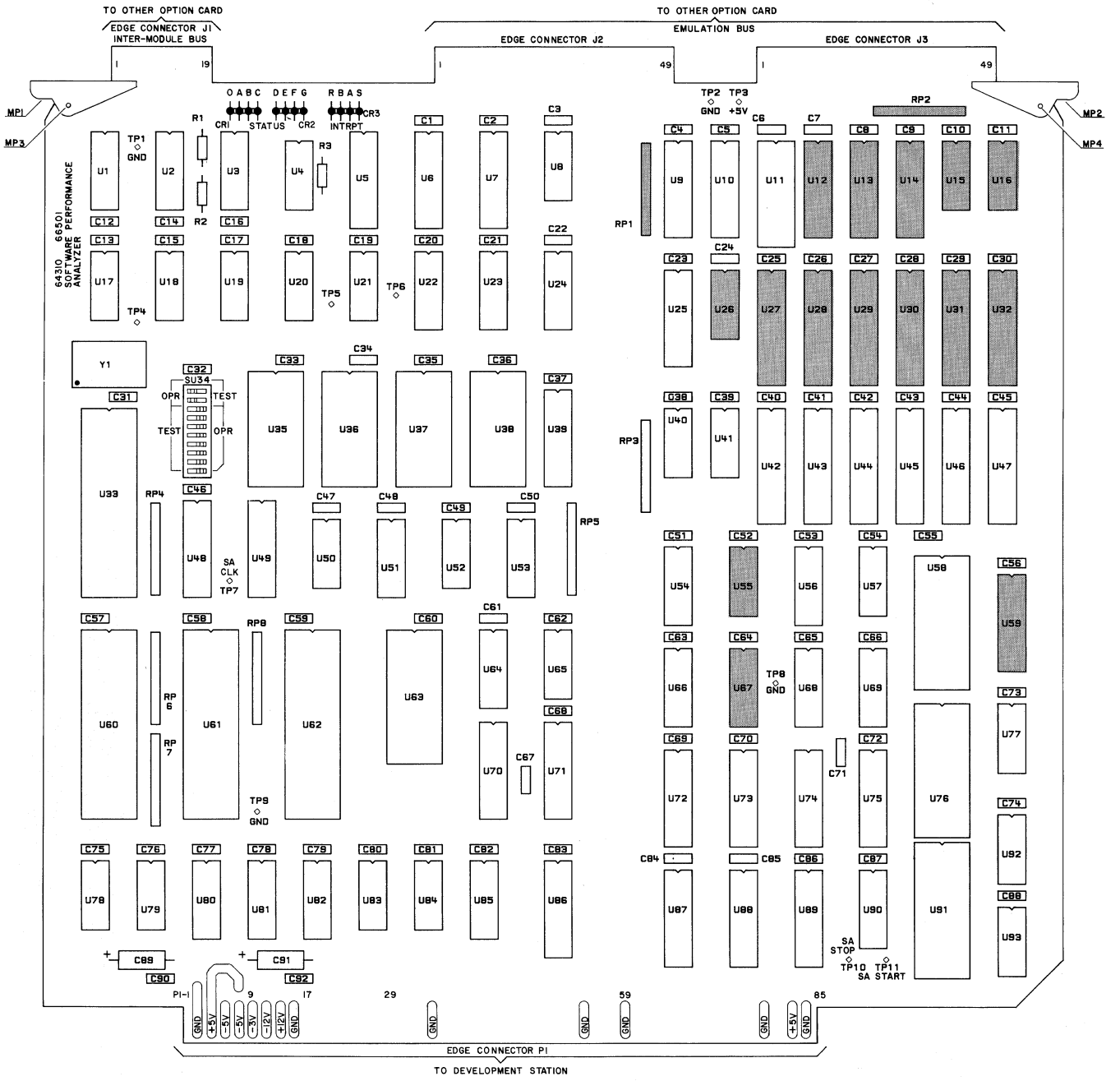
ICs ON SCHEMATIC 2

REF DES	HP PART NUMBER	MFG PART NUMBER	+5V PIN	GND PIN
U33	1820-2770	1820-2770	7	1
U35	64310-80000	64310-80000	24	12
U36	1818-1611	HM6116P-3	24	12
U37	1818-1611	HM6116P-3	24	12
U38	1818-1611	HM6116P-3	24	12
U39	1820-2206	SN74LS640N	24	12
U48	1820-1633	SN74S240N	20	10
U49	1820-1633	SN74S240N	20	10
U50	1820-1416	SN74LS14N	14	7
U51	1820-1240	SN74S138N	16	8
U52	1820-2685	74F02PC	14	7
U53	1820-1276	SN74LS194N	16	8
U65	1820-1197	SN74LS00N	14	7
U66	1820-1197	SN74LS00N	14	7
U77	1820-1416	SN74S14N	14	7
Y1	1813-0188	1813-0188	14	7

PARTS ON SCHEMATIC 2

CR3. RP3,4,6. SU34. TP7.

Figure 8-3. Schematic 2
Microcontroller
8-25



Component Locator

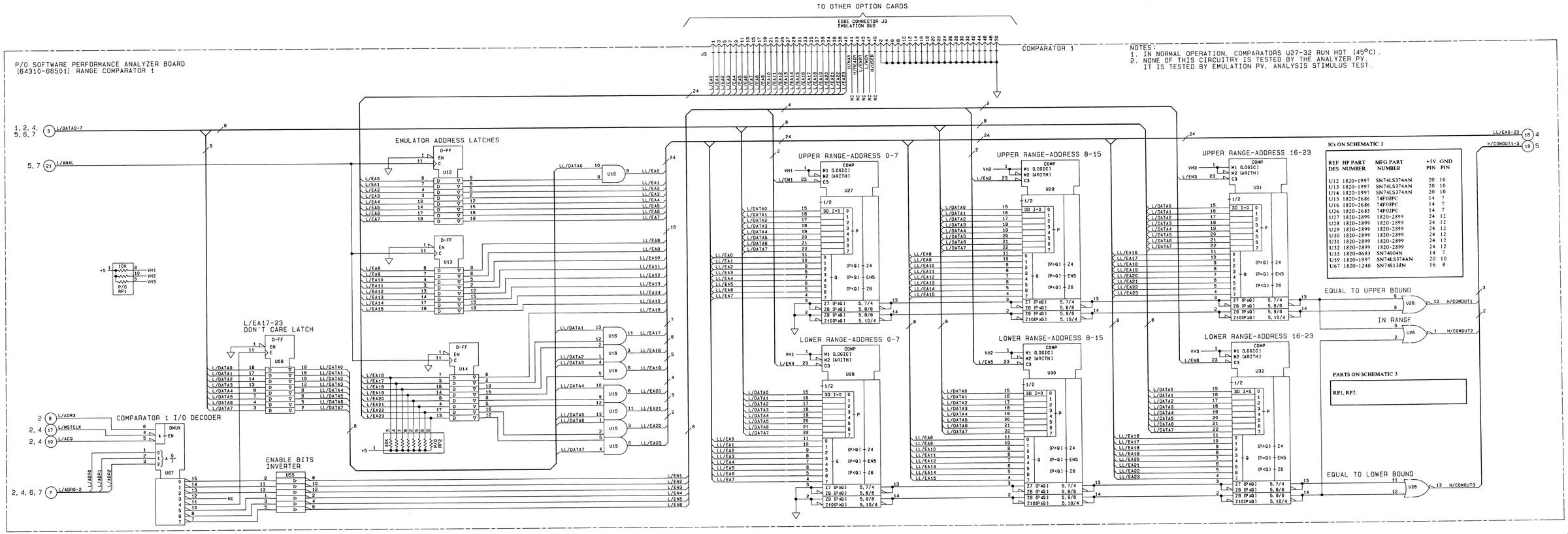
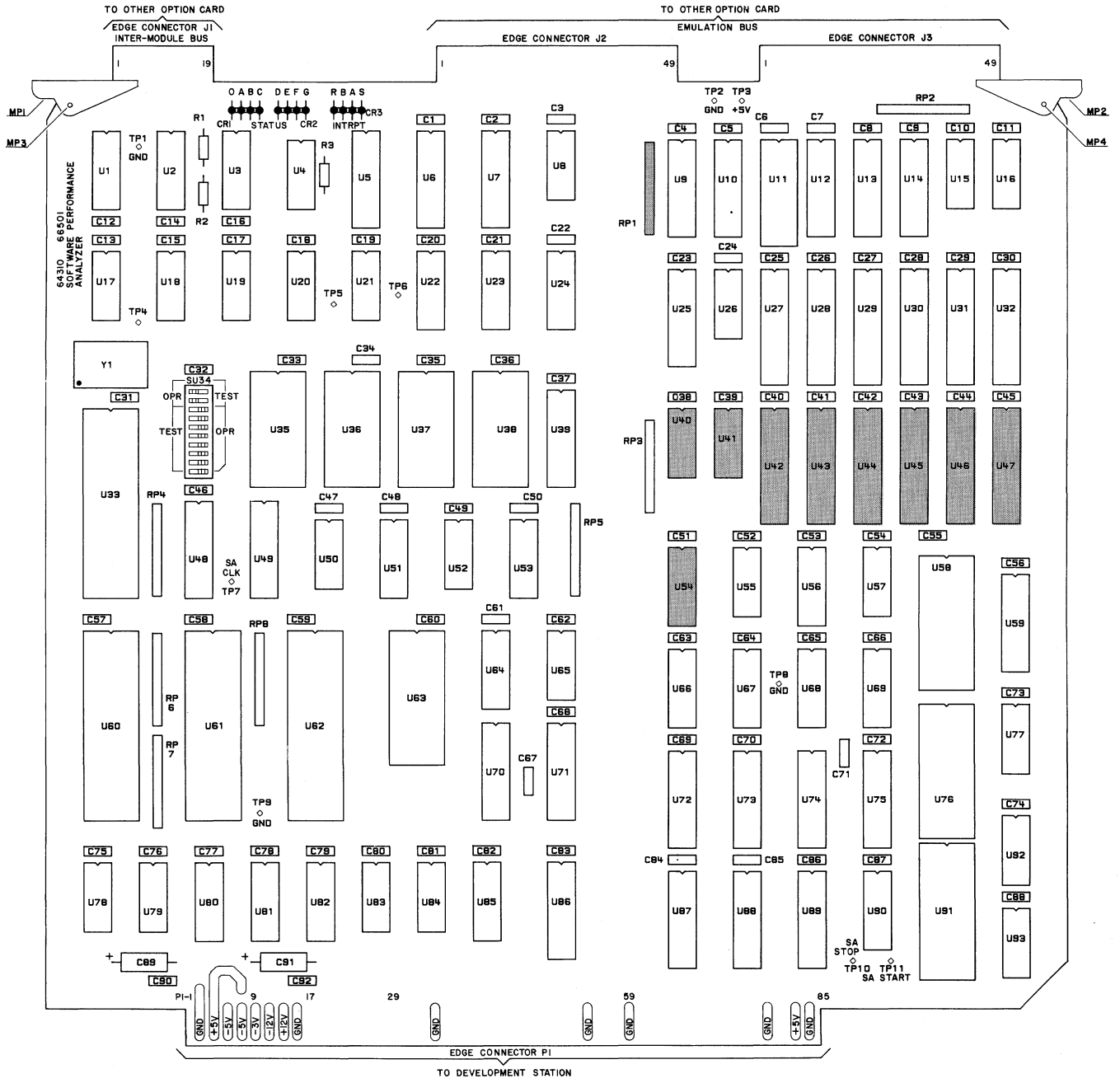
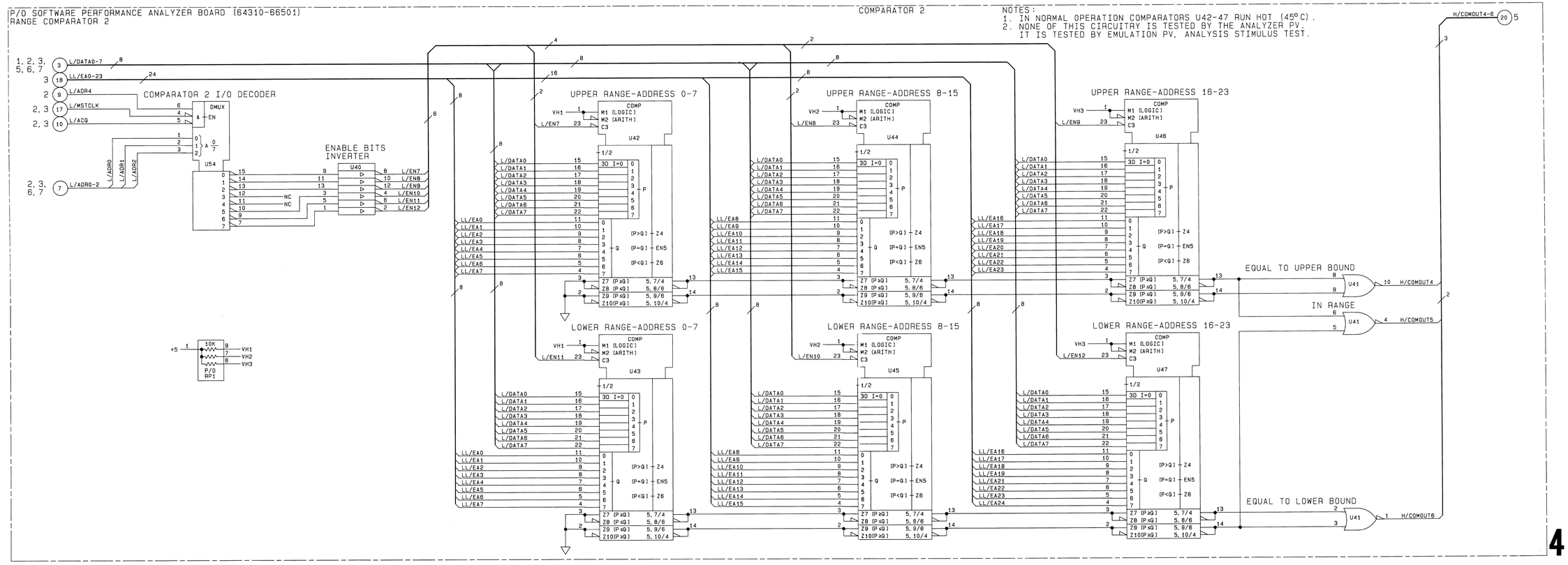


Figure 8-4. Schematic 3
Address Recognition, Comparator 1



Component Locator



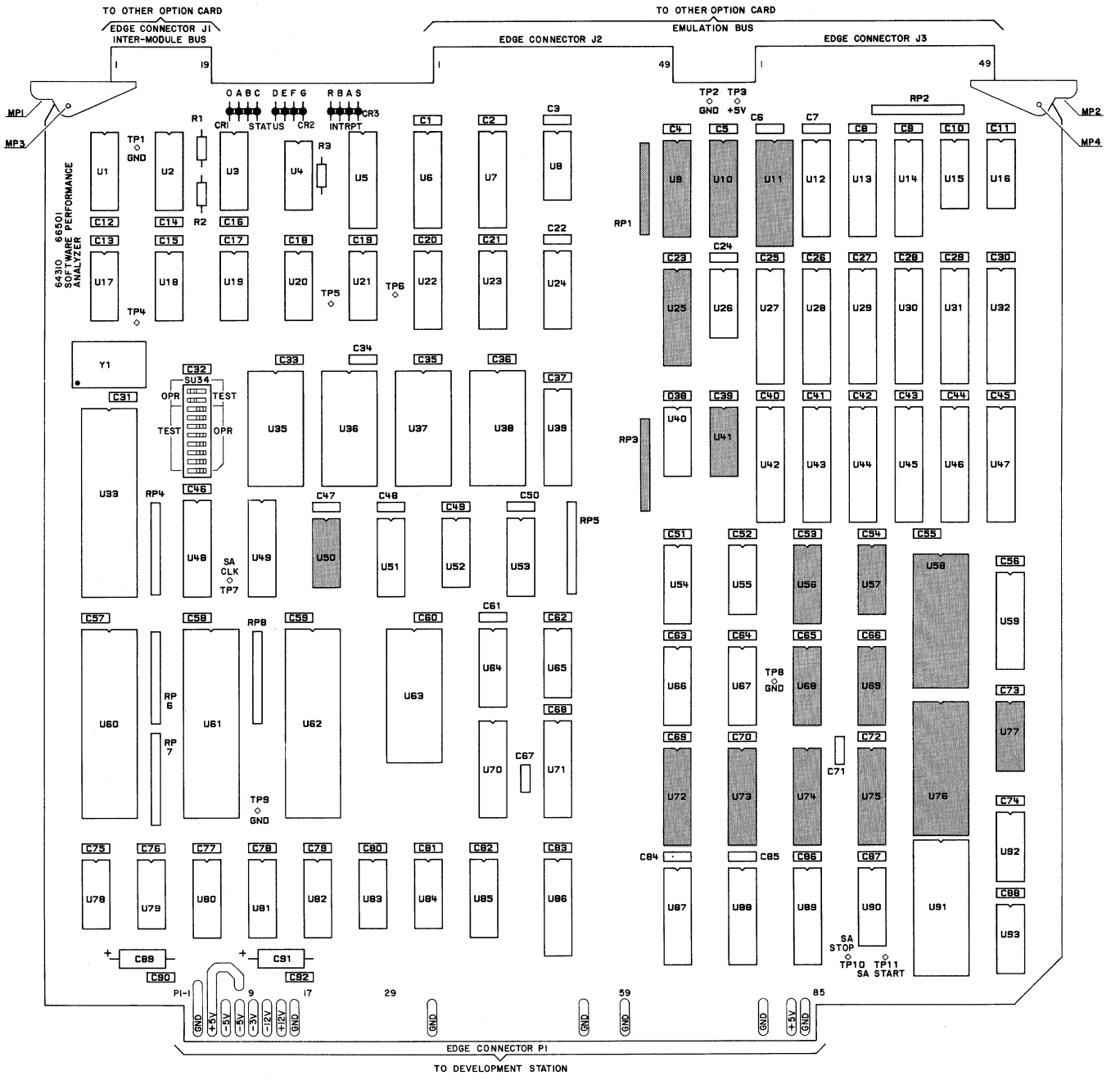
ICs ON SCHEMATIC 4

REF DES	HP PART NUMBER	MFG PART NUMBER	+5V PIN	GND PIN
U40	1820-0683	SN74S04N	14	7
U41	1820-2685	74F03PC	14	7
U42	1820-2899	1820-2899	24	12
U43	1820-2899	1820-2899	24	12
U44	1820-2899	1820-2899	24	12
U45	1820-2899	1820-2899	24	12
U46	1820-2899	1820-2899	24	12
U47	1820-2899	1820-2899	24	12
U54	1820-1240	SN74S138N	16	8

PARTS ON SCHEMATIC 4

RP1.

Figure 8-5. Service Sheet 4
Address Recognition, Comparator 2



Component Locator

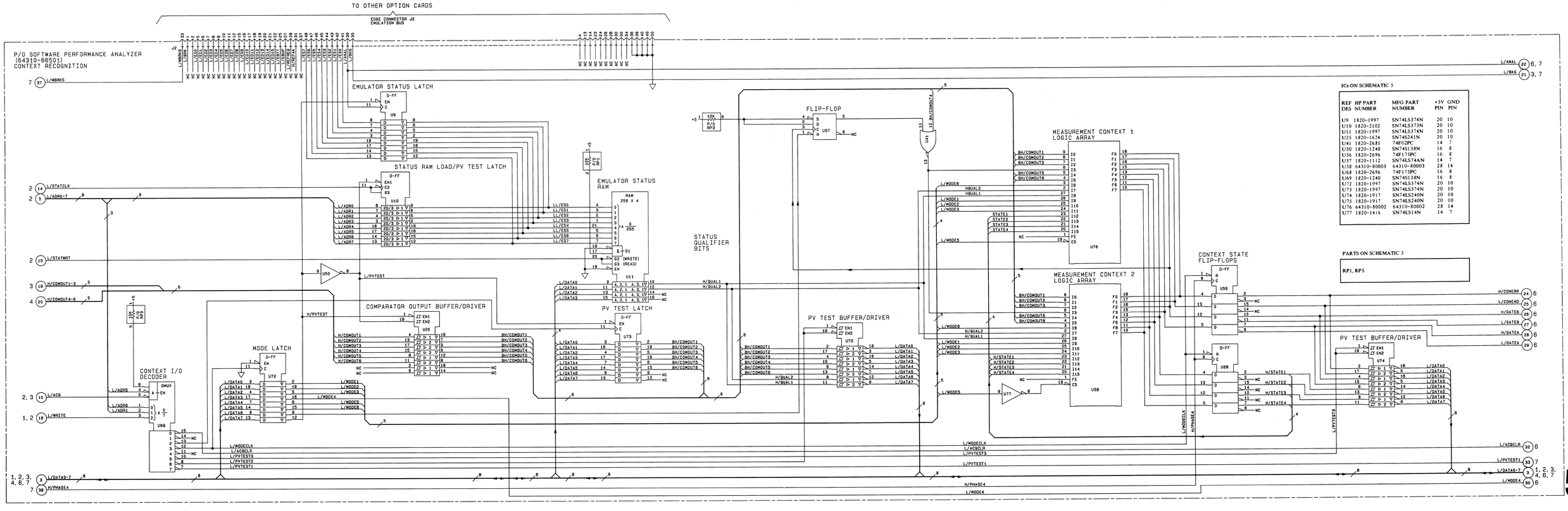
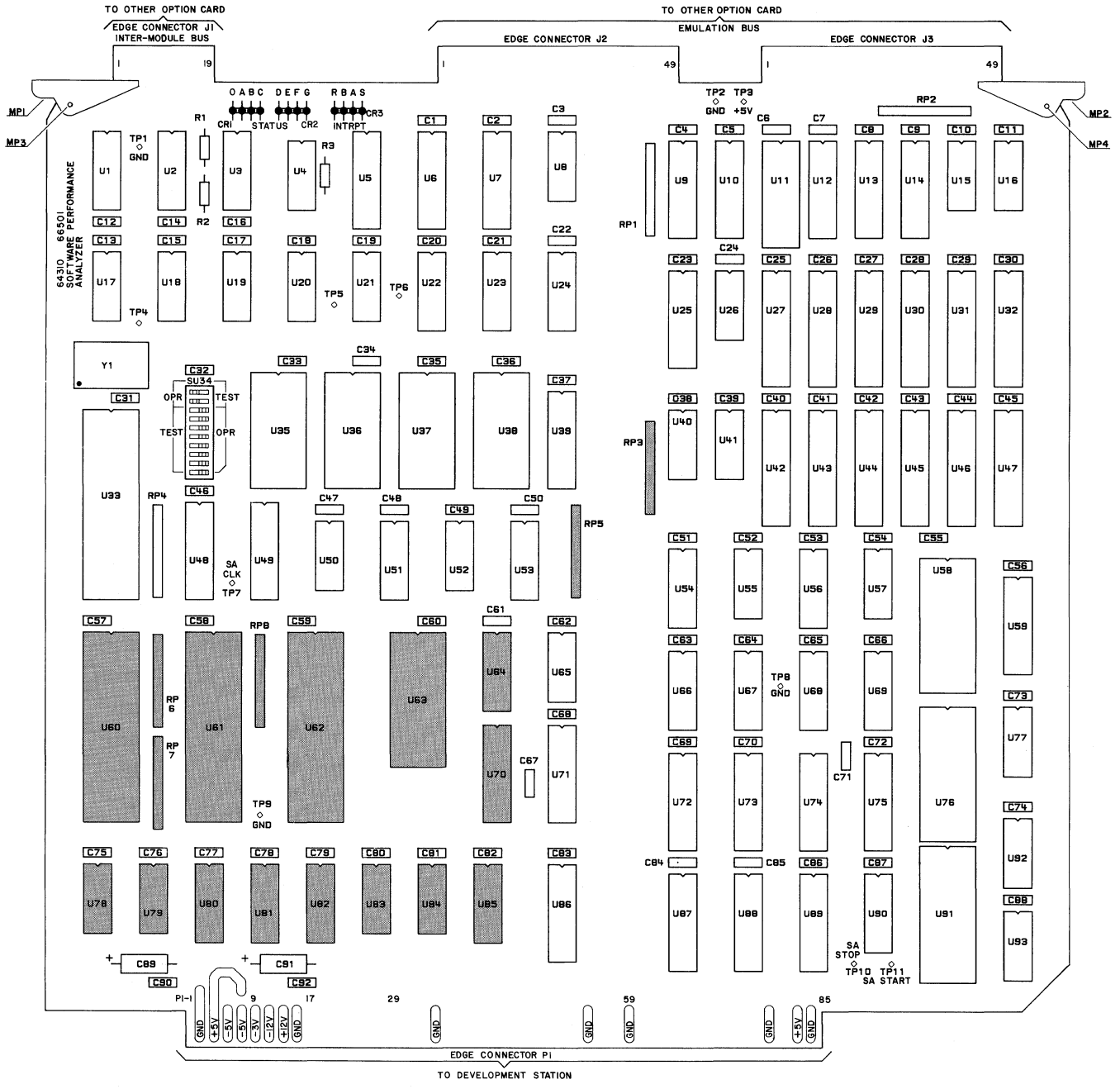
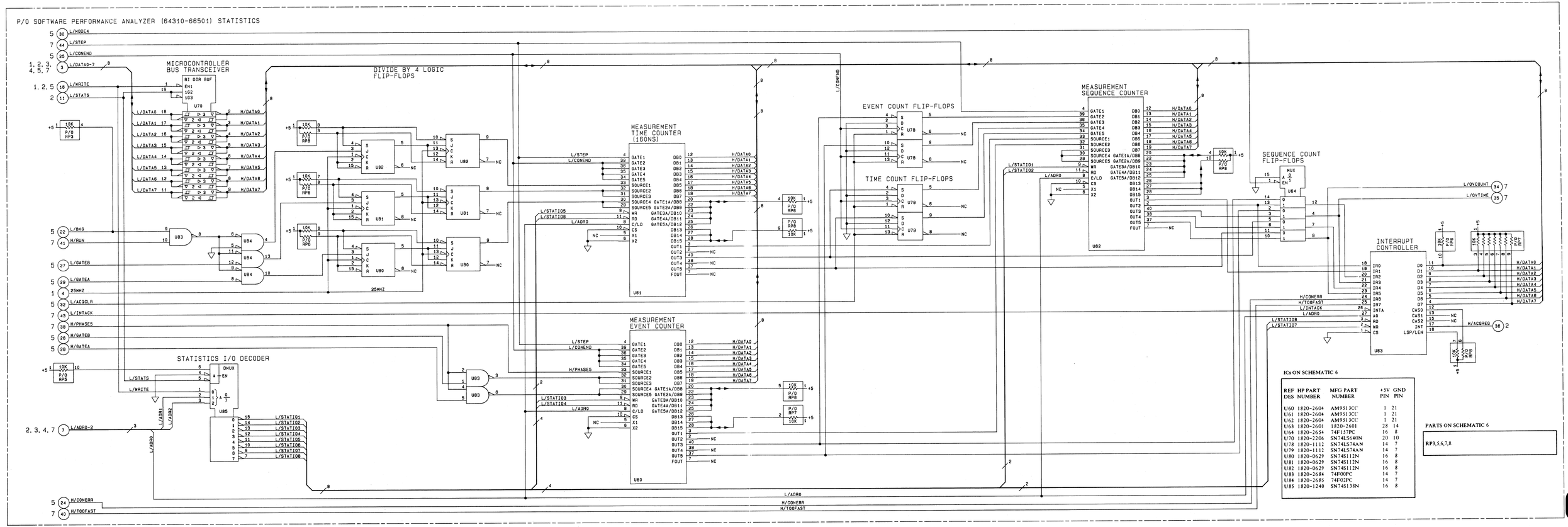


Figure 8-6. Schematic 5
Context Recognition



Component Locator



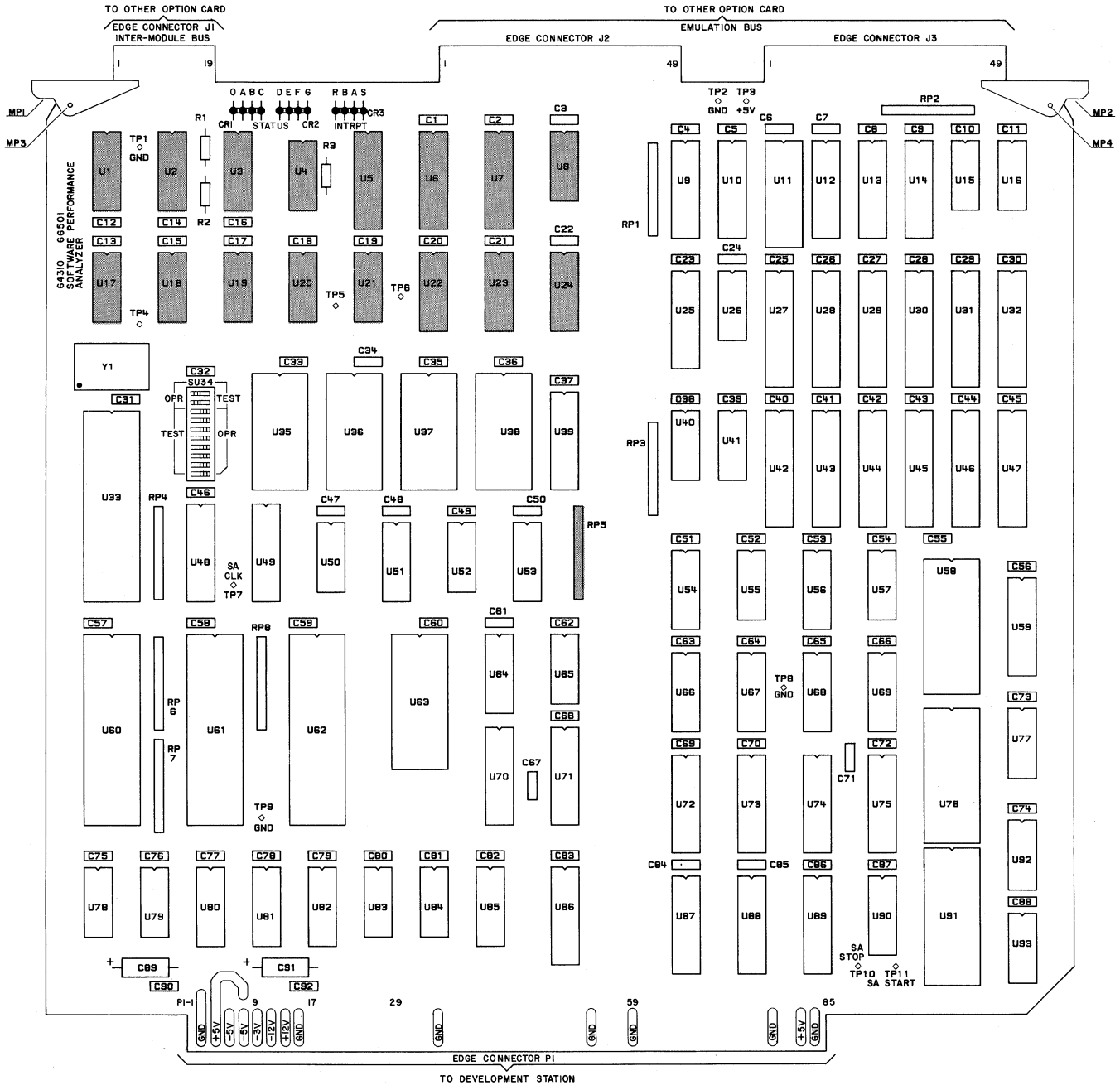
ICs ON SCHEMATIC 6

REF DES	HP PART NUMBER	MFG PART NUMBER	+5V PIN	GND PIN
U60	1820-2604	AM9513CC	1	21
U61	1820-2604	AM9513CC	1	21
U62	1820-2604	AM9513CC	1	21
U63	1820-2601	1820-2601	28	14
U64	1820-2654	74F157PC	16	8
U70	1820-2206	SN74LS640N	20	10
U78	1820-1112	SN74LS74AN	14	7
U79	1820-1112	SN74LS74AN	14	7
U80	1820-0629	SN74S112N	16	8
U81	1820-0629	SN74S112N	16	8
U82	1820-0629	SN74S112N	16	8
U83	1820-2684	74F00PC	14	7
U84	1820-2685	74F02PC	14	7
U85	1820-1240	SN74S138N	16	8

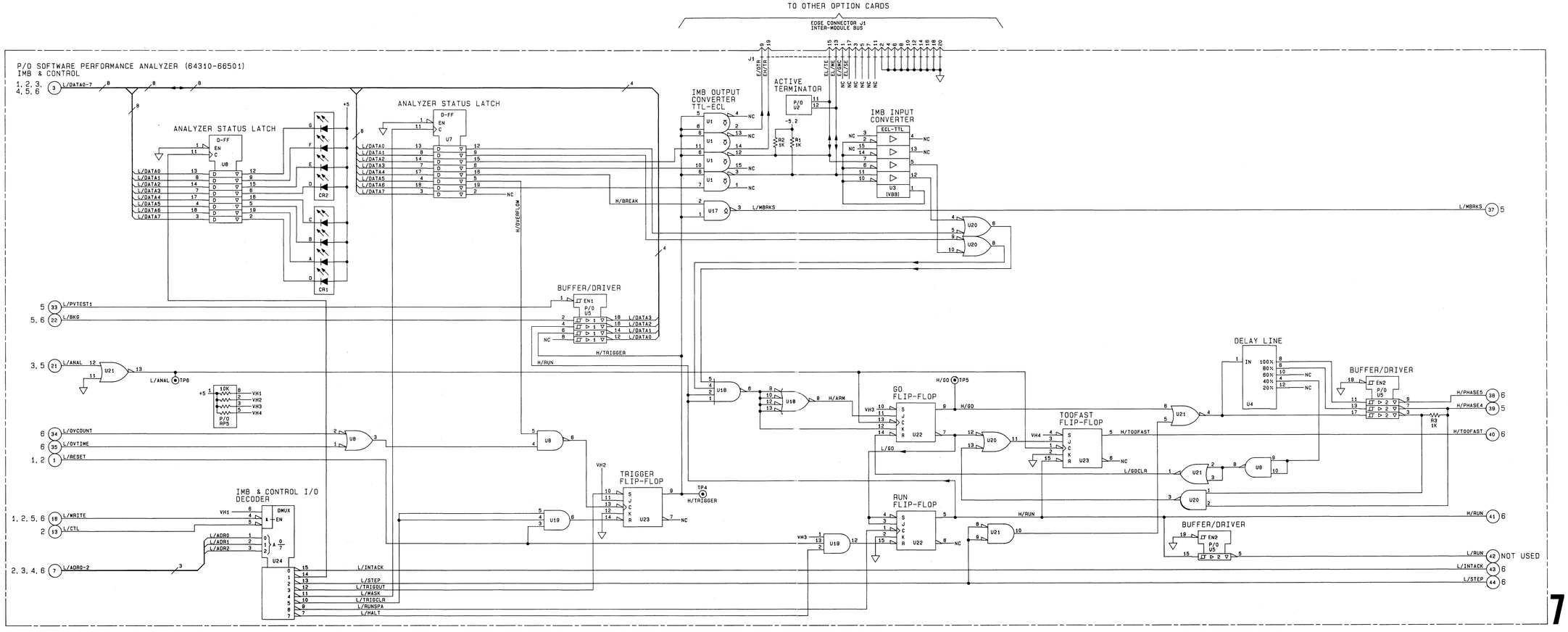
PARTS ON SCHEMATIC 6

RP3,5,6,7,8.

Figure 8-7. Schematic 6
Statistics



Component Locator



ICs ON SCHEMATIC 7

REF DES	HP PART NUMBER	MFG PART NUMBER	+5V PIN	GND PIN	-5V PIN
U1	1820-1173	MC10124L	9	16	8
U2	1820-2359	F10014PC	-	16	8
U3	1820-1052	MC10125L	9	16	8
U4	1813-0193	TTLDM-200	14	7	
U5	1820-1917	SN74LS240N	20	10	
U6	1820-1997	SN74LS374N	20	10	
U7	1820-1997	SN74LS374N	20	10	
U8	1820-2684	74F00PC	14	7	
U17	1820-0682	SN74S03N	14	7	
U18	1820-2689	74F20PC	14	7	
U19	1820-1203	SN74LS11N	14	7	
U20	1820-2684	74F00PC	14	7	
U21	1820-2685	74F02PC	14	7	
U22	1820-0629	SN74S112N	16	8	
U23	1820-0629	SN74S112N	16	8	
U24	1820-1240	SN74S138N	16	8	

PARTS ON SCHEMATIC 7

CR1,2. R1,2,3. RP5. TP4,5,6.

Figure 8-8. Schematic 7
Inter-Module Bus (IMB) and Control
8-35

SIGNATURE TABLE LOOP A

LOOP A signatures are valid while running the Performance Analyzer Reset Test.

Start = Positive edge of TP2 on the 64100A mainframe I/O board, or TP6 on the 64110A mainframe CPU/IO board.

Stop = Negative edge of TP2 on the 64100A mainframe I/O board, or TP6 on the 64110A mainframe CPU/IO board.

Clock = Negative edge of U89, pin 3 on the software performance analyzer.

Clock Qualifier = A high on U89, pin 9 on the software performance analyzer. Qualified signatures require a 5005A Signature Multimeter.

Ground = Use a ground lead from the probe to a ground point on the software performance analyzer.

high = a solid HIGH on the node under test.

low = a solid LOW on the node under test.

All logic is positive logic.

Vh = 0007

NODE	SIG
Microprocessor Schematic 2	
U 33- 1	low
U 33- 2	high
U 33- 4	0003
U 33- 7	high
U 33-37	0005

NODE	SIG
Control Bit Buffer/Receiver Schematic 2	
U 89- 1	low
U 89- 2	0007
U 89- 3	0007
U 89- 4	0004
U 89- 5	0002
U 89- 6	high
U 89- 7	0007
U 89- 8	high
U 89- 9	0007
U 89-10	low
U 89-11	0000
U 89-12	low
U 89-13	0000
U 89-14	low
U 89-15	0005
U 89-16	0003
U 89-17	0000
U 89-18	0007
U 89-19	low
U 89-20	high

NODE	SIG
Mainframe Control Logic Array Schematic 2	
U 91- 2	0004
U 91- 3	high
U 91- 8	0005
U 91- 9	0002
U 91-10	0004
U 91-11	0004
U 91-12	high
U 91-13	low
U 91-14	low
U 91-15	low
U 91-16	0001
U 91-17	0005
U 91-18	0002
U 91-19	low
U 91-20	low
U 91-21	0007
U 91-22	low
U 91-23	0007
U 91-24	0003
U 91-25	0002
U 91-26	0007
U 91-27	0007
U 91-28	high

SIGNATURE TABLE LOOP B.

LOOP B signatures are valid while running the Mainframe / Analyzer Interface Test.

Start = Positive edge of TP11 on the software performance analyzer.

Stop = Positive edge of TP10 on the software performance analyzer.

Clock = Positive edge of TP7 on the software performance analyzer.

Clock Qualifier = No qualified clocks are necessary.

Ground = Use a ground lead from the probe to a ground point on the software performance analyzer.

high = a solid HIGH on the node under test.

low = a solid LOW on the node under test.

All logic is positive logic.

Vh = CF44

NODE	SIG
Microprocessor	
Schematic 2	
U 33-1	low
U 33-2	high
U 33-3	high
U 33-4	CF44
U 33-5	0000
U 33-6	low
U 33-7	high
U 33-8	FAPF
U 33-9	H62A
U 33-10	F04P
U 33-11	F519
U 33-12	36PF
U 33-13	2353
U 33-14	A83F
U 33-15	6A03
U 33-16	A83F
U 33-17	A83F
U 33-18	A83F
U 33-19	6A02
U 33-20	6A03
U 33-21	6A03
U 33-22	A83F
U 33-23	A83F
U 33-32	6A03
U 33-33	high

NODE	SIG
U 33-34	CF44
U 33-35	0000
U 33-36	1478
U 33-37	CF44
U 33-38	0000
U 33-39	low
U 33-40	high
ROM	
Schematic 2	
U 35-12	low
U 35-18	H647
U 35-19	1478
U 35-20	low
U 35-21	high
U 35-24	high

NODE	SIG
RAMs	
Schematic 2	
U 36-12	low
U 36-18	CF44
U 36-19	1478
U 36-20	low
U 36-21	6A03
U 36-24	high
U 37-12	low
U 37-18	CF44
U 37-19	1478
U 37-20	low
U 37-21	6A03
U 37-24	high
U 38-12	low
U 38-18	CF44
U 38-19	1478
U 38-20	low
U 38-21	6A03
U 38-24	high

NODE	SIG
Data Bus	
Transceiver	
Schematic 2	
U 39-1	6A03
U 39-2	10PU
U 39-4	0146
U 39-6	CH32
U 39-8	03U4
U 39-19	6A03

NODE	SIG
Address Bus	
Buffers	
Schematic 2	
U 48-2	H647
U 48-3	H647
U 48-4	A83F
U 48-5	1478
U 48-6	A83F
U 48-7	H646
U 48-8	A83F
U 48-9	H647
U 48-11	6A03
U 48-12	1478
U 48-13	6A02
U 48-14	1478
U 48-15	A83F
U 48-16	1478
U 48-17	6A03
U 48-18	6A03
Misc Gates	
Schematic 2	
U 49-2	H647
U 49-3	6A6P
U 49-4	FAPF
U 49-5	795H
U 49-6	F04P
U 49-7	9U17
U 49-8	36PF
U 49-9	0000
U 49-11	CF44
U 49-12	8AA8
U 49-13	2353
U 49-14	7F0A
U 49-15	F519
U 49-16	76A8
U 49-17	H62A
U 49-18	6A03
Inverters	
Schematic 2	
U 50-1	low
U 50-2	high
U 50-3	6A03
U 50-4	H647
U 50-5	6A03
U 50-6	H647
U 50-12	CF44
U 50-13	0000

NODE	SIG
Master I/O	
Decoder	
Schematic 2	
U 51-1	H646
U 51-2	H647
U 51-3	6A03
U 51-4	low
U 51-5	0000
U 51-6	CF44
U 51-7	CF44
U 51-9	CF44
U 51-10	CF44
U 51-11	H647
U 51-12	6A02
U 51-13	CF45
U 51-14	high
U 51-15	high
Misc Gates	
Schematic 2	
U 52-1	CF44
U 52-2	0000
U 52-3	low
U 52-4	0000
U 52-5	CF44
U 52-6	CF44
U 52-8	6A03
U 52-9	0000
U 52-10	H647
U 52-11	H647
U 52-12	H647
U 52-13	6A03
Wait-State	
Shift Register	
Schematic 2	
U 53-9	high
U 53-10	H647
U 53-11	0000
U 53-13	1478

NODE	SIG
Misc Gates	
Schematic 2	
U 65-1	H647
U 65-2	A83F
U 65-3	CF44
U 65-8	6A03
U 65-9	high
U 65-10	H647
U 66-4	CF44
U 66-5	6A03
U 66-6	H647

NODE	SIG
Interface Address	
Latch	
Schematic 1	
U 86-1	pulsing
U 86-11	pulsing
Data-In Latch	
Schematic 1	
U 87-1	pulsing
U 87-11	pulsing
Data-Out Latch	
Schematic 1	
U 88-1	pulsing
U 88-11	pulsing
Ready Flip-flops	
Schematic 1	
U 92-1	pulsing
U 92-2	high
U 92-3	pulsing
U 92-4	high
U 92-5	pulsing
U 92-6	pulsing
U 92-8	pulsing
U 92-9	pulsing
U 92-10	high
U 92-11	pulsing
U 92-12	pulsing
U 92-13	pulsing
Board ID Gates.	
Schematic 1	
U 93-4	high
U 93-5	low
U 93-6	pulsing
U 93-8	pulsing
U 93-9	high
U 93-10	low
U 93-11	pulsing
U 93-12	pulsing
U 93-13	pulsing

SIGNATURE TABLE LOOP C.

LOOP C signatures are valid while running the Data Acquisition Test.

Start = Positive edge of TP11 on the software performance analyzer.

Stop = Positive edge of TP10 on the software performance analyzer.

Clock = Positive edge of TP7 on the software performance analyzer.

Clock Qualifier = No qualified clocks are necessary.

Ground = Use a ground lead from the probe to a ground point on the software performance analyzer.

high = a solid HIGH on the node under test.

low = a solid LOW on the node under test.

All logic is positive logic.

Vh = F186

NODE	SIG
Misc Buffers	
Schematic 7	
U 5-1	1650
U 5-2	high
U 5-3	CCF6
U 5-4	3721
U 5-5	U6A7
U 5-6	6H9C
U 5-7	CCF6
U 5-9	CCF6
U 5-11	7A40
U 5-13	7A40
U 5-15	3721
U 5-17	7A40
U 5-19	low
Analyzer Status	
Latch	
Schematic 7	
U 6-1	low
U 6-2	low
U 6-3	2A67
U 6-4	P1H0
U 6-5	low
U 6-6	high
U 6-9	PA98
U 6-11	02U6
U 6-12	85H5
U 6-15	1H4U
U 6-16	UCCU
U 6-17	3C2A
U 6-18	9A07
U 6-19	high
Analyzer Status	
Latch	
Schematic 7	
U 7-1	low
U 7-2	high
U 7-3	2A67
U 7-4	P1H0
U 7-5	low
U 7-6	high
U 7-9	high
U 7-11	H1AU
U 7-12	high
U 7-15	low
U 7-16	low
U 7-18	9A07
U 7-19	high
Status RAM	
Load Latch	
Schematic 5	
U 10-1	low
U 10-2	82A2
U 10-3	4HPH
U 10-4	5748
U 10-5	8AAU
U 10-6	P2U1
U 10-7	CAUH
U 10-8	F718
U 10-9	CH3U
U 10-11	0000
U 10-12	AUF1
U 10-13	CC67
U 10-14	H6CF
U 10-15	6C90
U 10-16	8H68
U 10-17	8P00
U 10-18	6258
U 10-19	F117
Status RAM	
Schematic 5	
U 11-8	low
U 11-10	FH61
U 11-12	9U6H
U 11-14	9780
U 11-16	0183
U 11-17	high
U 11-18	low
U 11-19	low
U 11-20	F497
U 11-22	high
Misc Gates	
Schematic 7	
U 20-1	CCF6
U 20-2	CCF6
U 20-3	7A40
U 20-4	AF1H
U 20-5	high
U 20-6	6H9C
U 20-8	6H9C
U 20-9	high
U 20-10	AF1H
U 20-11	CCF6
U 20-12	high
U 20-13	7A40

NODE	SIG
Misc Flip-flops	
Schematic 7	
U 22-1	FC83
U 22-2	low
U 22-3	high
U 22-4	high
U 22-5	3721
U 22-6	U6A7
U 22-7	high
U 22-9	low
U 22-10	high
U 22-11	AHC1
U 22-12	6F37
U 22-13	low
U 22-14	7A40
U 22-15	6C93
U 23-1	low
U 23-2	low
U 23-3	CCF6
U 23-4	high
U 23-5	low
U 23-6	high
U 23-7	AF1H
U 23-9	6H9C
U 23-10	1496
U 23-11	high
U 23-12	low
U 23-13	high
U 23-14	6P04
U 23-15	3721
IMB/Control	
I/O Decoder	
Schematic 7	
U 24-1	F718
U 24-2	CAUH
U 24-3	5748
U 24-4	4152
U 24-5	H540
U 24-6	high
U 24-7	6C93
U 24-9	FC83
U 24-10	6P04
U 24-11	H1AU
U 24-12	1496
U 24-13	7A40
U 24-14	02U6
U 24-15	high
Misc Gate	
Schematic 5	
U 41-11	1H46
U 41-12	993U
U 41-13	7076
Inverter	
Schematic 5	
U 50-8	low
U 50-9	high
Context State	
Flip-flops	
Schematic 5	
U 56-1	33A3
U 56-2	81P9
U 56-3	406U
U 56-4	7CC9
U 56-5	7UAU
U 56-6	H9FC
U 56-7	184H
U 56-9	CCF6
U 56-10	F17P
U 56-11	00U8
U 56-12	U0C0
U 56-13	HAUF
U 56-14	3U24
U 56-15	UPA2
Misc Flip-flop	
Schematic 5	
U 57-1	2P5F
U 57-2	high
U 57-3	U0C0
U 57-4	high
U 57-5	1H46
Context 2 Logic	
Array	
Schematic 5	
U 58-1	low
U 58-2	9U6H
U 58-10	P658
U 58-11	A65H
U 58-12	1945
U 58-13	76H8
U 58-14	low
U 58-15	7UAU
U 58-16	U0C0
U 58-17	HAUF
U 58-18	7CC9
U 58-19	C741
U 58-20	U525
U 58-21	U47U
U 58-22	UUFH
U 58-23	CHC4
U 58-27	FH61
U 58-28	high
Read/Write Gates	
Schematic 2	
U 65-1	80H4
U 65-2	HP21
U 65-3	F497
U 65-4	HP21
U 65-5	0000
U 65-6	F186
U 65-8	7HPC
U 65-9	high
U 65-10	CF6H
U 65-11	F497
U 65-12	80H4
U 65-13	HP21
Context State	
Flip-flops	
Schematic 5	
U 68-1	33A3
U 68-2	CHC4
U 68-3	7F32
U 68-4	76H8
U 68-5	P658
U 68-6	34A3
U 68-7	U525
U 68-9	CCF6
U 68-10	U47U
U 68-11	35U9
U 68-12	A65H
U 68-13	1945
U 68-14	3P4C
U 68-15	UUFH
Context I/O	
Decoder	
Schematic 5	
U 69-1	F718
U 69-2	CAUH
U 69-3	4152
U 69-4	8P00
U 69-5	H165
U 69-6	high
U 69-7	1650
U 69-9	P649
U 69-10	31C6
U 69-11	high
U 69-12	33A3
U 69-13	5U64
U 69-14	high
U 69-15	CH8C

NODE	SIG
Mode Latch	
Schematic 5	
U 72-2	1607
U 72-5	F65C
U 72-6	76F7
U 72-9	2P5F
U 72-12	high
U 72-15	5202
U 72-16	4070
U 72-19	F909
PV Test Latch	
Schematic 5	
U 73-2	4821
U 73-5	H2FH
U 73-6	7F37
U 73-15	CP6H
U 73-16	993U
U 73-19	2U11
PV Test Buffer	
Schematic 5	
U 74-2	81P9
U 74-4	F17P
U 74-6	CHC4
U 74-8	U47U
U 74-11	U525
U 74-13	UUFH
U 74-15	184H
U 74-17	UPA2

NODE	SIG
PV Test Buffer	
Schematic 5	
U 75-1	P649
U 75-2	4821
U 75-4	H2FH
U 75-6	7F37
U 75-8	9U6H
U 75-11	FH61
U 75-13	CP6H
U 75-15	993U
U 75-17	2U11
U 75-19	P649
Context 1 Logic Array	
Schematic 5	
U 76-1	low
U 76-10	P658
U 76-11	A65H
U 76-12	1945
U 76-13	76H8
U 76-14	low
U 76-15	7UAU
U 76-16	U0C0
U 76-17	HAUF
U 76-18	7CC9
U 76-19	76F7
U 76-20	U525
U 76-21	U47U
U 76-22	UUFH
U 76-23	CHC4
U 76-27	FH61
U 76-28	high
Inverters	
Schematic 5	
U 77-5	F186
U 77-6	0000
U 77-8	C741
U 77-9	76F7

SIGNATURE TABLE LOOP D.

LOOP D signatures are valid while running the Time, Event, and Sequence Counter Test.

Start = Positive edge of TP11 on the software performance analyzer.

Stop = Positive edge of TP10 on the software performance analyzer.

Clock = Positive edge of TP7 on the software performance analyzer.

Clock Qualifier = No qualified clocks are necessary.

Ground = Use a ground lead from the probe to a ground point on the software performance analyzer.

high = a solid HIGH on the node under test.

low = a solid LOW on the node under test.

All logic is positive logic.

Vh = 91H4

NODE	SIG
Event Counter Schematic 6	
U 60- 8	CH23
U 60- 9	25FU
U 60-10	low
U 60-11	91H4
Time Counter Schematic 6	
U 61- 8	CH23
U 61- 9	CH9U
U 61-10	low
U 61-11	07P6

NODE	SIG
Sequence Counter Schematic 6	
U 62- 8	CH23
U 62- 9	UPPC
U 62-10	low
U 62-11	91H4
Data Bus Transceiver Schematic 6	
U 70- 1	2P2P
U 70- 2	9P58
U 70- 3	3H4A
U 70- 4	0HP4
U 70- 5	3U54
U 70- 6	CP5U
U 70- 7	8U3C
U 70- 8	65H6
U 70- 9	U7FF
U 70-11	U4F7
U 70-12	5H5U
U 70-13	9FC4
U 70-14	AA65

NODE	SIG
Statistics I/O Decoder Schematic 6	
U 85- 1	2P2P
U 85- 2	90U6
U 85- 3	AFHF
U 85- 4	low
U 85- 5	U089
U 85- 6	high
U 85- 7	high
U 85- 9	high
U 85-10	07P6
U 85-11	CH9U
U 85-12	91H4
U 85-13	25FU
U 85-14	91H4
U 85-15	UPPC

SIGNATURE TABLE LOOP E.

LOOP E signatures are valid while running the Statistics Test.

Start = Positive edge of TP11 on the software performance analyzer.

Stop = Positive edge of TP10 on the software performance analyzer.

Clock = Positive edge of TP7 on the software performance analyzer.

Clock Qualifier = No qualified clocks are necessary.

Ground = Use a ground lead from the probe to a ground point on the software performance analyzer.

high = a solid HIGH on the node under test.

low = a solid LOW on the node under test.

All logic is positive logic.

Vh = AC79

NODE	SIG
Misc Gates	
Schematic 7	
U 5-4	0000
U 5-6	5958
U 8-1	P01C
U 8-5	0U3A
U 19-1	high
U 19-2	113P
U 19-3	high
U 19-4	P126
U 19-5	P126
U 19-6	P126
U 19-12	113P
U 19-13	high
Misc Flip-flops	
Schematic 7	
U 23-1	low
U 23-2	low
U 23-3	C014
U 23-4	high
U 23-5	low
U 23-6	high
U 23-7	U221
U 23-9	5958
U 23-10	9318
U 23-11	high
U 23-12	low
U 23-14	P126
U 23-15	0000
Event Counter	
Schematic 6	
U 60-2	low
U 60-3	0000
U 60-4	1C6H
U 60-29	1C6H
U 60-30	1C6H
U 60-31	1C6H
U 60-32	1C6H
U 60-33	C014
U 60-34	UP8H
U 60-35	UP8H
U 60-36	UP8H
U 60-37	0000
U 60-38	low
U 60-39	UP8H
Time Counter	
Schematic 6	
U 61-2	low
U 61-3	0000
U 61-4	1C6H
U 61-34	UP8H
U 61-35	UP8H
U 61-36	UP8H
U 61-37	0000
U 61-38	low
U 61-39	UP8H
Sequence Counter	
Schematic 6	
U 62-4	1C6H
U 62-32	0000
U 62-33	0000
U 62-34	AC79
U 62-35	AC79
U 62-36	AC79
U 62-37	0000
U 62-38	0000
U 62-39	AC79
Interrupt	
Controller	
Schematic 6	
U 63-1	low
U 63-2	H393
U 63-3	6FA0
U 63-4	719H
U 63-5	7F31
U 63-6	7H6H
U 63-7	F948
U 63-8	2P5A
U 63-9	U042
U 63-10	H67F
U 63-11	HH92
U 63-12	low
U 63-13	low
U 63-14	low
U 63-15	low
U 63-16	high
U 63-17	1489
U 63-20	804F
U 63-21	P01C
U 63-24	AU43
U 63-25	low
U 63-26	AC79
U 63-27	8427
U 63-28	high

NODE	SIG
Sequence Count	
Flip-flops	
Schematic 6	
U 64-1	5123
U 64-2	0000
U 64-3	0000
U 64-5	0000
U 64-6	0000
U 64-10	0000
U 64-11	0000
U 64-13	2PUA
U 64-14	0000
U 64-15	low
Data Bus	
Transceiver	
Schematic 6	
U 70-1	PC7H
U 70-2	HH92
U 70-3	H67F
U 70-4	U042
U 70-5	2P5A
U 70-6	F948
U 70-7	7H6H
U 70-8	7F31
U 70-9	719H
U 70-11	82AH
U 70-12	9H6H
U 70-13	4F87
U 70-14	U134
U 70-19	AC82
Event Count	
Flip-flop	
Schematic 6	
U 78-1	AC79
U 78-2	low
U 78-3	UP8H
U 78-4	0000
U 78-5	AC79
U 78-6	0000
U 78-8	0000
U 78-9	AC79
U 78-10	0000
U 78-11	UP8H
U 78-12	low
U 78-13	AC79
Time Count	
Flip-flop	
Schematic 6	
U 79-1	AC79
U 79-2	low
U 79-3	UP8H
U 79-4	0000
U 79-5	AC79
U 79-6	0000
U 79-8	0000
U 79-9	AC79
U 79-10	0000
U 79-11	UP8H
U 79-12	low
U 79-13	AC79
Divide-by-four	
Flip-flops	
Schematic 6	
U 80-2	high
U 80-3	0000
U 80-4	high
U 80-5	0000
U 80-6	AC79
U 80-7	AC79 or 0000
U 80-9	0000 or AC79
U 80-10	high
U 80-11	0000
U 80-12	0000
U 80-14	high
U 80-15	high
U 81-2	high
U 81-3	0000
U 81-4	high
U 81-5	0000
U 81-6	AC79
U 81-10	high
U 81-11	0000
U 81-12	0000
U 81-14	high
U 81-15	high
U 82-2	high
U 82-3	0000
U 82-4	high
U 82-5	0000
U 82-6	AC79
U 82-10	high
U 82-11	0000
U 82-12	0000
U 82-14	high
U 82-15	high
Misc Gates	
Schematic 6	
U 83-1	AU43
U 83-2	C014
U 83-3	1C6H
U 83-4	C014
U 83-5	AU43
U 83-6	1C6H
U 83-8	AC79
U 83-9	high
U 83-10	0000
U 83-11	high
U 83-12	low
U 83-13	low
U 84-2	low
U 84-4	0000
U 84-5	low
U 84-6	AC79
U 84-8	043A
U 84-9	AC79
U 84-10	0000
U 84-11	AC79
U 84-12	043A
U 84-13	0000
Statistics I/O	
Decoder	
Schematic 6	
U 85-1	PC7H
U 85-2	FH79
U 85-3	7A72
U 85-4	low
U 85-5	AC82
U 85-6	high
U 85-7	6FA0
U 85-9	H393
U 85-10	AC79
U 85-11	AC79
U 85-12	AC79
U 85-13	AC79
U 85-14	U5C8
U 85-15	4A70

SIGNATURE TABLE LOOP F.

LOOP F signatures are valid while running the Inter-Module Bus Test.

NOTE

The IMB CABLE MUST BE REMOVED during signature analysis.
This causes the test display to indicate a failure.

Start = Positive edge of TP11 on the software performance analyzer.

Stop = Positive edge of TP10 on the software performance analyzer.

Clock = Positive edge of TP7 on the software performance analyzer.

Clock Qualifier = No qualified clocks are necessary.

Ground = Use a ground lead from the probe to a ground point on the software performance analyzer.

ECL signatures require a 5005A Signature Multimeter:

To change from TTL to ECL --->
press the data threshold button three times.

To change from ECL to TTL --->
press the data threshold button five times.

high = a solid HIGH on the node under test.

low = a solid LOW on the node under test.

All logic is positive logic.

Vh = 86H2

NODE	SIG
TTL-to-ECL Converter	
Schematic 7	
U 1-2	86H2 ECL
U 1-3	5386 ECL
U 1-5	2A3U
U 1-6	2A3U
U 1-7	7P01
U 1-10	7HU8
U 1-11	54PU
U 1-12	53C9 ECL
U 1-14	86H2 ECL

NODE	SIG
ECL-to-TTL Converter	
Schematic 7	
U 3-5	53C9
U 3-7	53C9 ECL
U 3-11	5386 ECL
U 3-12	5386
Misc Buffer	
Schematic 7	
U 5-4	low
U 5-6	2A3U

NODE	SIG
Analyzer Status	
Latch	
Schematic 7	
U 7-1	low
U 7-6	7HU8
U 7-9	C7C4
U 7-11	7297
U 7-12	C7C4
U 7-15	54PU
U 7-19	7P01

NODE	SIG
Misc Gate	
Schematic 7	
U 8-1	low
U 8-2	low
U 8-3	high
U 8-4	high
U 8-5	low
U 8-6	high
U 17-1	2A3U
U 17-2	low
U 18-1	low
U 18-2	low
U 18-4	P40H
U 18-5	P432
U 18-6	high
U 20-4	5386
U 20-5	C7C4
U 20-6	P432
U 20-8	P40H
U 20-9	C7C4
U 20-10	53C9
Run Flip-flop	
Schematic 7	
U 22-1	high
U 22-2	low
U 22-3	high
U 22-4	high
U 22-5	low
Trigger Flip-flop	
Schematic 7	
U 23-7	AFPH
U 23-9	2A3U
U 23-10	3156
U 23-11	high
U 23-12	low

SIGNATURE TABLE LOOP G.

LOOP G signatures are valid while running an emulator analyzer stimulus test.

NOTE

This test is not part of the software performance analyzer PV. It must be run from emulation PV. These signatures are valid whether or not the emulation bus cables are connected.

Start = Positive edge of TP11 on the software performance analyzer.

Stop = Positive edge of TP10 on the software performance analyzer.

Clock = Positive edge of TP7 on the software performance analyzer.

Clock Qualifier = No qualified clocks are necessary.

Ground = Use a ground lead from the probe to a ground point on the software performance analyzer.

high = a solid HIGH on the node under test.

low = a solid LOW on the node under test.

All logic is positive logic.

Vh = 614P

NODE	SIG	NODE	SIG	NODE	SIG	NODE	SIG
Misc Gates Schematic 7		Address Range 1 Comparators Schematic 3		Address Range 2 Comparators Schematic 4		Comparator 2 I/O Decoder Schematic 4	
U 18- 1	9174						
U 18- 2	9174	U 27- 1	high	U 42- 1	high	U 54- 4	0000
U 18- 4	614P	U 27-23	CCFH	U 42-23	65HP	U 54- 5	9728
U 18- 5	614P					U 54- 6	40P6
U 18- 6	U03A	U 28- 1	high	U 43- 1	high	U 54- 7	4401
		U 28-23	2F59	U 43-23	2962	U 54- 9	482F
U 20- 4	614P					U 54-10	54A3
U 20- 5	0000	U 29- 1	high	U 44- 1	high	U 54-11	high
U 20- 6	614P	U 29-23	7149	U 44-23	A38A	U 54-12	high
U 20- 8	614P					U 54-13	F509
U 20- 9	0000	U 30- 1	high	U 45- 1	high	U 54-14	F2F4
U 20-10	614P	U 30-23	CHA8	U 45-23	35PH	U 54-15	0490
		U 31- 1	high	U 46- 1	high		
		U 31-23	88P9	U 46-23	A447		
		U 32- 1	high	U 47- 1	high		
		U 32-23	A9P9	U 47-23	254U		

Don't Care Latch
Schematic 3

U 59- 2 FF09
or 7783
U 59-11 667P
U 59-19 559P

Comparator 1
I/O Decoder
Schematic 3

U 67- 4 0000
U 67- 5 9728
U 67- 6 6588
U 67- 7 F8A7
U 67- 9 HFP6
U 67-10 4H17
U 67-11 667P
U 67-12 high
U 67-13 P9A7
U 67-14 1007
U 67-15 HA83

Mode Latch
Schematic 5

U 72-12 2PP1

64310-90901, MARCH 1983

PRINTED IN U.S.A.