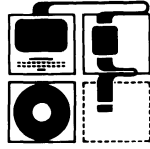


64000 LOGIC DEVELOPMENT SYSTEM



**MODEL 64212A/213A
6800/6802 EMULATOR PODS**



CERTIFICATION

Hewlett-Packard Company certifies that this product met its published specifications at the time of shipment from the factory. Hewlett-Packard further certifies that its calibration measurements are traceable to the United States National Bureau of Standards, to the extent allowed by the Bureau's calibration facility, and to the calibration facilities of other International Standards Organization members.

WARRANTY

This Hewlett-Packard system product is warranted against defects in materials and workmanship for a period of 90 days from date of installation. During the warranty period, HP will, at its options, either repair or replace products which prove to be defective.

Warranty service of this product will be performed at Buyer's facility at no charge within HP service travel areas. Outside HP service travel areas, warranty service will be performed at Buyer's facility only upon HP's prior agreement and Buyer shall pay HP's round trip travel expenses. In all other cases, products must be returned to a service facility designated by HP.

For products returned to HP for warranty service. Buyer shall prepay shipping charges to HP and HP shall pay shipping charges to return the product to Buyer. However, Buyer shall pay all shipping charges, duties, and taxes for products returned to HP from another country.

HP warrants that its software and firmware designated by HP for use with an instrument will execute its programming instructions when properly installed on that instrument. HP does not warrant that the operation of the instrument, or software, or firmware will be uninterrupted or error free.

LIMITATION OF WARRANTY

The foregoing warranty shall not apply to defects resulting from improper or inadequate maintenance by Buyer, Buyer-supplied software or interfacing, unauthorized modification or misuse, operation outside of the environmental specifications for the product, or improper site preparation or maintenance.

NO OTHER WARRANTY IS EXPRESSED OR IMPLIED. HP SPECIFICALLY DISCLAIMS THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.

EXCLUSIVE REMEDIES

THE REMEDIES PROVIDED HEREIN ARE BUYER'S SOLE AND EXCLUSIVE REMEDIES. HP SHALL NOT BE LIABLE FOR ANY DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES, WHETHER BASED ON CONTRACT, TORT, OR ANY OTHER LEGAL THEORY.

ASSISTANCE

Product maintenance agreements and other customer assistance agreements are available for Hewlett-Packard products.

For any assistance, contact your nearest Hewlett-Packard Sales and Service Office. Addresses are provided at the back of this manual.

PDF NOTE: This change notice is included here instead of being incorporated because the changes listed do not correspond correctly with the schematics herein. Either the notice is wrong, or it applies to a different manual version.

MANUAL IDENTIFICATION
Model Number: 64212A/213A
Date Printed: November, 1981
Part Number: 64213-90901

This supplement contains important information for correcting manual errors and for adapting the manual to instruments containing improvements made after the printing of the manual.

To use this supplement:

Make all ERRATA corrections.

Make all appropriate serial number related changes indicated in the tables below.

Serial Prefix or Number	Make Manual Changes	Serial Prefix or Number	Make Manual Changes
1952A	ALL		

▲ NEW ITEM

▲ **CHANGE 1**

Make the following changes to Model 64212A only.

Section VIII,

Page 8-29, Figure 8-6. User and Pod Bus Interface,

Add: R17 (332 ohms) between J2-15 and C2

Add: Connections to U23-4, U23-11, U23-9, U23-8, U23-12, U23-18, U17A all pins.

Replace: U17B with U19B

Connect: U23-4 to N TSC (U8-11)

Delete: U2

Connect: U12A-13 to U17A-2

U12A-1,2 to O PEN (U23-9)

U12A-12 to U16A-2 and to U19B-12,13

U12A-18 to U19B-9,10 and to U19A-1

U19B-8 to U11-19, U7-1,19, and U10-1,19

U17A-1 to LL HBA (U3-7)

U17A-3 to J2-13

NOTE

Manual change supplements are revised as often as necessary to keep manuals as current and accurate as possible. Hewlett-Packard recommends that you periodically request the latest edition of this supplement. When requesting copies, quote the manual identification information from your supplement, or the model number and print date from the title page of the manual.



▲CHANGE 1 (Cont'd)

Change: HP Part No. 64212-66501 in upper left corner to 64212-66502.
Page 8-31, Figure 8-7. Emulation Processor and Timing,
Delete: U16B-5 to U20A-3
Connect: U16B-5 to U20B-5
Delete: Connections between J3-3, U27-5, U12B-3.
Connect: U12B-3 to U11-18
Delete: U2
Delete: U17C
Move: U19B to Sheet 1
Delete: connection U3-39 to U2-1 and U16-6
Connect: U3-39 to ground
Change: HP Part No. 64212-66501 in upper left corner to 64212-66502.



PRELIMINARY SERVICE MANUAL

**MODEL 64212A
6800 EMULATOR POD**

AND

**MODEL 64213A
6802 EMULATOR POD**

REPAIR NUMBERS

This manual applies directly to Model 64212A Emulator Pods with repair numbers prefixed **1952A**, and to Model 64213A Emulator Pods with repair numbers prefixed **2029A**. For additional information about repair numbers see Section I, paragraph 1-3.

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Manual Part Number 64213-90901
Microfiche Part Number 64213-90801

PRINTED: NOVEMBER 1981

SAFETY SUMMARY

The following general safety precautions must be observed during all phases of operation, service, and repair of this instrument. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of the instrument. Hewlett-Packard Company assumes no liability for the customer's failure to comply with these requirements.

GROUND THE INSTRUMENT.

To minimize shock hazard, the instrument chassis and cabinet must be connected to an electrical ground. The instrument is equipped with a three-conductor ac power cable. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet. The power jack and mating plug of the power cable meet International Electrotechnical Commission (IEC) safety standards.

DO NOT OPERATE IN AN EXPLOSIVE ATMOSPHERE.

Do not operate the instrument in the presence of flammable gases or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.

KEEP AWAY FROM LIVE CIRCUITS.

Operating personnel must not remove instrument covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

DO NOT SERVICE OR ADJUST ALONE.

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

DO NOT SUBSTITUTE PARTS OR MODIFY INSTRUMENT.

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification of the instrument. Return the instrument to a Hewlett-Packard Sales and Service Office for service and repair to ensure that safety features are maintained.

DANGEROUS PROCEDURE WARNINGS.

Warnings, such as the example below, precede potentially dangerous procedures throughout this manual. Instructions contained in the warnings must be followed.

WARNING

**Dangerous voltages, capable of causing death, are present in this instrument.
Use extreme caution when handling, testing, and adjusting.**

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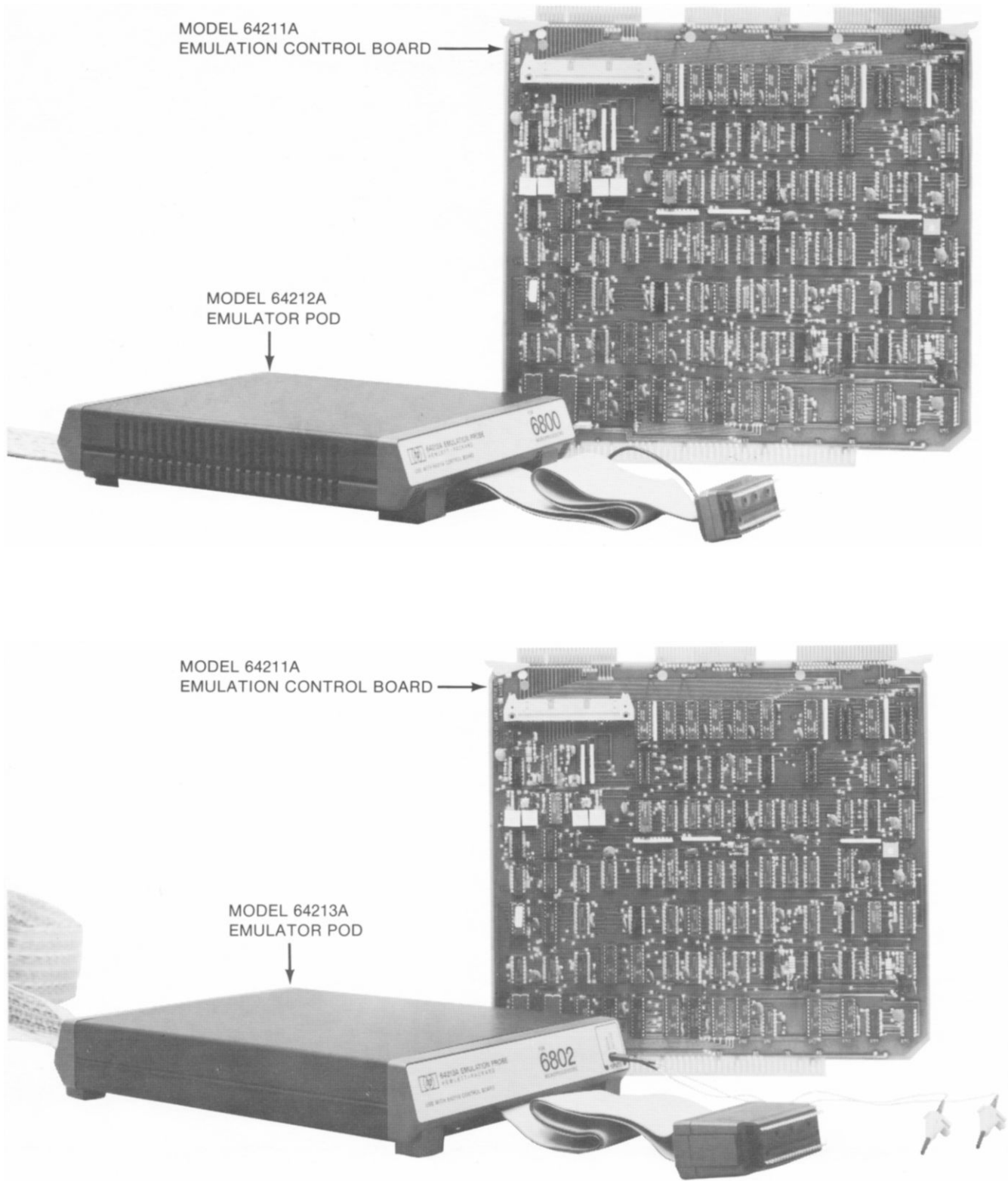


Figure 1-1. 6800 Emulator/6802 Emulator

SECTION I

GENERAL INFORMATION

1-1. INTRODUCTION.

1-2. This manual contains preliminary information concerning the installation, maintenance, and troubleshooting for the Model 64212A 6800 Emulator and the Model 64213A 6802/6808 Emulator used in the 64000 Logic Development System. Troubleshooting theory contained in this manual allows the user to identify failures to the board level. The Performance Verification (PV) and the block diagram descriptions include the Model 64211A Emulator Control Board.

1-3. This manual is organized with eight sections: Section I provides a brief physical and functional description. Section II contains installation and removal procedures. Section III covers operation. Section IV describes performance verification tests used to isolate failures to the card level. Section V describes adjustments. Section VI lists replaceable parts. Section VII provides backdating information needed to make this manual applicable to older units. Section VIII contains service data, including a block diagram and a discussion of the theory of operation at the block diagram level.

1-4. INSTRUMENTS COVERED BY THIS MANUAL.

1-6. Attached to the instrument or printed on the printed circuit card is the repair number. The repair number is in the form: 0000A00000. It is in two parts; the first four digits and the letter are the repair prefix and the last five are the suffix. The prefix is the same for all identical instruments. The suffix is assigned sequentially and is different for each instrument. The contents of this manual apply to instruments with the repair number prefix(es) listed under REPAIR NUMBERS on the title page.

1-7. An instrument manufactured after the printing of this manual may have a repair prefix that is not listed on the title page. This unlisted repair number prefix indicates that the instrument is different from those described in this manual. Updating the manual for this newer instrument is accomplished by a Manual Changes supplement. The supplement contains "change information" that explains how to adapt this manual for the newer instrument.

1-8. In addition to change information, the supplement contains information for correcting errors in this manual. To keep this manual as current as possible, Hewlett-Packard recommends that you periodically request the latest Manual Changes supplement. The supplement for this manual is identified with the manual print date and the part number, which both appear on the manual title page. Complimentary copies of the supplement are available from Hewlett-Packard Sales/Service Office.

1-9. For information concerning a repair number prefix that is not listed on the title page or in the Manual Changes supplement, contact your nearest Hewlett-Packard Sales/Service Office.

1-10. DESCRIPTION.

1-11. The 6800 Emulator consists of a Model 64211A Emulator Control Board and the Model 64212A 6800 Emulator Pod. The 6802 Emulator consists of a Model 64211A Emulator Control Board and the Model 64213A 6802 Emulator Pod. The Model 64211A Emulator Control Board is installed within the 64000 mainframe. The 6800 Emulator Pod consists of a user plug, which replaces the users microprocessor in the target system, the pod assembly, and the interconnecting cables. The 6802 Emulator Pod consists of a user plug which contains an oscillator circuit, the pod assembly, and the interconnecting cables.

1-12. Each emulator pod houses the emulation microprocessor, and the buffers, timing, and control circuits which provide the interface to the users target system and to the Emulator Control Board. The control board provides the interface to the optional memory and analysis functions and to the 64000 Development Station. The 64000 Development Station controls emulation functions through the interface with the Emulator Control Board.

1-13. ACCESSORIES SUPPLIED.

1-14. No accessories are supplied with the emulation pods. Supplied with the Emulator Control Board are two Part Number 64151-61602 bus cables which are required to connect the Emulator Control Board to the Emulation Memory Controller. The installation of these cables is discussed in Section II and in the Emulator Control Board Manual.

1-15. ADDITIONAL EQUIPMENT REQUIRED.

1-16. The Emulator Probes require a Model 64211A Emulator Control Board installed in a Model 64100A Development Station in order to complete a minimum configuration for in-circuit emulation.

1-17. POWER SUPPLY REQUIREMENTS.

1-18. The power requirements of each Emulator, including the Model 64211A Emulator Control Board, are listed in table 1-1.

Table 1-1. Power Supply Requirements

	64212A	64213A
+5 V	5.38 A	5.79 A
-5 V	Not used	
+12 V	Approx. 2 mA	

No other voltages are used.

1-19. ELECTRICAL CHARACTERISTICS.

1-20. MAXIMUM CLOCK SPEED. The maximum clock speeds of the 6800/6802 emulators are given below.

With all memory mapped in the target system and no wait states:

6800 = 2 MHz maximum clock frequency.
6800 = 235 ns minimum Peripheral Read Access Time.

6802 = 2 MHz maximum clock frequency.
(Clock Frequency = 1/4 oscillator frequency)
6802 = 245 ns minimum Peripheral Read Access Time.

With any references mapped to emulation memory:

6800 = minimum operating clock period (TCYC) which is the greater of;

$$T_{cyc} = 520 \text{ ns}$$

or

$$T_{cyc} = 4t_{\Phi r} + PW_{\Phi 1H} + PW_{\Phi 2H}$$

where: $4t_{\Phi r}$ = pulse rise time;
 $PW_{\Phi 1H}$ = 180 ns minimum;
 $PW_{\Phi 2H}$ = 295 ns minimum.

6802 = 1.4 MHz maximum clock frequency, without wait states.
2 MHz maximum clock frequency, with emulation wait states. (Wait states are added only for references to emulation memory.)

1-21. EMULATOR POD TO TARGET SYSTEM INTERFACE. The following load characteristics are imposed on the target system by the emulator.

- a. For all address, data and control lines the input and output characteristics are equivalent to low-power Schottky TTL levels and impedances plus approximately 20 pF.
- b. The 6800 Clock inputs are as specified in 6800 specifications plus approximately 20 pF.
- c. A circuit is provided within the 6802 user plug, which will act as the oscillator for circuits which use the on-board oscillator of the 6802, or as a buffer for circuits using an external oscillator. This circuit meets Motorola 6802/08 specifications plus 20 pF.

SECTION II

INSTALLATION

2-1. INTRODUCTION.

2-2. This section contains information for installing and removing the 6800/6802 Emulators. Included are initial inspection procedures and instructions for repacking emulators for shipment.

2-3. INITIAL INSPECTION.

2-4. Inspect the shipping container for damage. If the shipping container or cushioning material is damaged, it should be kept until contents of the shipment have been checked mechanically and electrically. Procedures for checking electrical performance are given in Section IV. If the contents are not complete, if there is mechanical damage or defect, or if the instrument does not pass the performance tests, notify the carrier as well as the Hewlett-Packard Sales/Service Office. Keep the shipping materials for carriers inspection. The Hewlett-Packard Sales/Service Office will arrange for repair or replacement at Hewlett-Packard's option without waiting for claim settlement.

2-5. INSTALLATION.

2-6. Figure 2-1 shows a top view of the 64100A mainframe card cage. The recommended slot for the Emulator Control Board is the rearmost position. This maximizes the free cable length to the emulator pod.

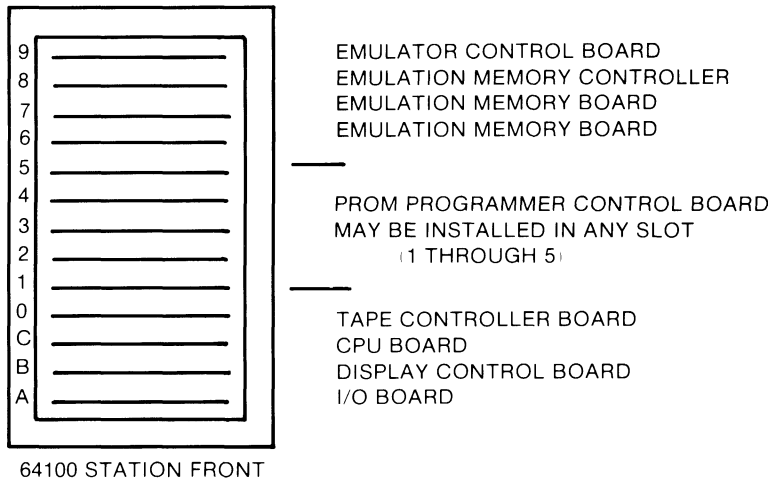
**WARNING**

To prevent personal injury, refer to the safety requirements listed in the 64000 mainframe service manual before installing this option.

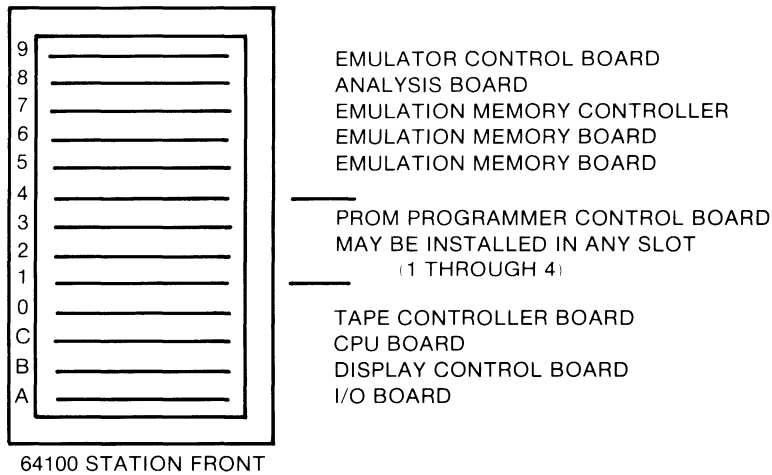
**CAUTION**

Emulators must be installed and removed with the 64000 power turned off to prevent damage to the system.

A. EMULATION AND MEMORY



B. EMULATION/ANALYSIS AND MEMORY



October 1981

Figure 2-1. Recommended Card Cage Configuration

2-7. To install the Emulator proceed as follows:

- a. Turn 64100A power OFF.
- b. Loosen the two hold down screws and remove the card cage access cover.
- c. Connect the selected emulator pod to the Emulator Control Board prior to the installation of the board in the card cage. This is done to simplify the connection of the multiconductor pod bus cables to the board. Two multicolored ribbon cables are used to connect the pod to the Emulator Control Board. One cable terminates in a female card-edge connector, the other terminates in a female socket-type connector. Pin 1 is indicated by a triangle molded into the body of each connector. The mating connectors for the cable connectors are located at the top left corner of the board as viewed from the component side. Pin 1 of the card-edge connector (J1) is indicated by a "1" etched into the board. Pin 1 of the connector block located directly below J1 (J4) is indicated by a triangle molded into the connector block. The connector block and the mating female connector on the cable have matching colored dots on their surfaces. The connector block is a latching type connector. Before installing the cable connector into the connector block insure that the latching tips are open (spread toward the outside edges of the board). Connect the card-edge connector first, then connect the socket-type connector to the connector block. Push the socket-type connector into the connector block until the latching tips snap over the top of the connector.
- d. Grasp the board by the extractor levers located at the top of the card. Be very careful not to dislodge the cables. Hold the card with the component side toward the front of the development station and the card-edge connector labeled P1 toward the bottom of the card cage. Insert the card into the selected card slot guide rails, make sure P1 and the motherboard connector are aligned, and push the card down until seated firmly in the connector.
- e. The bus cables supplied with the Emulator Control Board are used to connect to the optional Emulation Memory Controller. The bus cables are keyed so that they will seat on the edge connectors in only one position.
- f. Stack the emulator pod cables flat through one of the cable slots at the back of the development station.

CAUTION

The following precautions should be taken while using Hewlett-Packard Emulator Pods. Damage to the emulator circuitry may result if these precautions are not observed.

POWER DOWN TARGET SYSTEM.

Turn off power to the user target system and the emulation development station before inserting the user plug to avoid circuit damage resulting from voltage transients or mis-insertion of the user plug.

VERIFY USER PLUG ORIENTATION.

Make certain that Pin 1 of the target system microprocessor socket and Pin 1 of the user plug are properly aligned before inserting the user plug in the socket. Failure to do so may result in damage to the emulator circuitry.

PROTECT AGAINST STATIC DISCHARGE.

The emulator pod contains devices which are susceptible to damage by static discharge. Therefore, operators should take precautionary measures before handling the user plug to avoid emulator damage.

NOTE

When the user plug is installed in the target system it is important to understand the output driving and input loading characteristics which the emulator system presents to the target system. These are presented in Section I of this manual.

2-8. REMOVAL.

2-9. Emulators are removed using the following procedure:

- a. Turn the 64100 mainframe power OFF.
- b. Remove the bus cables from the card.
- c. Remove the Emulator Control Board from the card cage.

2-10. OPERATING ENVIRONMENT.

2-11. Emulators may be operated in environments within the following limits:

Temperature	0° to +40°C
Humidity	5% to 80% relative humidity
Altitude	4600 m (15 000 ft)

They should be protected from temperature extremes which cause condensation within the units.

2-12. STORAGE AND SHIPMENT ENVIRONMENT.

2-13. These units may be stored or shipped within the following limits:

Temperature	-40°C to +75°C
Humidity	5% to 80% relative humidity
Altitude	15 240 m (50 000 ft)

2-14. PACKAGING.

2-15. ORIGINAL PACKAGING. Containers identical to those used in factory packaging are available through Hewlett-Packard Sales/Service Offices.

2-16. OTHER PACKAGING. The following general instructions should be used for repacking with commercially available materials:

- a. Wrap the unit in heavy paper or plastic.
- b. Use a strong shipping container. A double-wall shipping container of 350 pound test material is adequate.
- c. Use a layer of shock absorbing material 70 to 100 mm (3 to 4 inch) thick around all sides of the unit to provide firm cushioning and to prevent movement inside the container.
- d. Seal shipping container securely.
- e. Mark shipping container FRAGILE to ensure careful handling.
- f. In any correspondence, refer to the unit by model number and full repair number.

SECTION III
OPERATION

3-1. INTRODUCTION.

3-2. The functions of the 6800/6802 Emulators are transparent to, and require no interaction with the operator. Refer to the Emulator/Analyzer Operator's manual for an explanation of emulation and the use of the emulator subsystem.

SECTION IV

PERFORMANCE TESTS

4-1. INTRODUCTION.

4-2. This section describes the Performance Verification (PV) tests for the 6800/6802 Emulators. The scope of the PV is to resolve problems to the board level only. This board level analysis is in support of the Blue Stripe Program.

4-3. For convenience, the figures which illustrate the PV displays are grouped together at the end of this section.

4-4. PERFORMANCE VERIFICATION.

4-5. The 6800/6802 Emulator PV is a subset of the Option Test PV. Option Test PV provides tests to exercise option modules which may be configured within the mainframe. The tests are identical for both the 6800 and the 6802 with the exception of a memory test for the 6802 internal memory. Each test description includes an explanation of the test and suspected causes for failures.

4-6. To run the emulator PV, use the following procedure:

- a. With the operating system initialized and awaiting a command, as shown in figure 4-1, type in the lower case command;

```
option_test      RETURN
```

(An **opt_test** softkey is provided with more recent software releases.)

- b. The CRT will now display a bus map listing the installed option modules with their corresponding card slot numbers as shown in figure 4-2. Enter the slot number indicated for the 6800_02 emulator. For example, if the 6802 Emulator Control Board is in slot 9, enter:

```
9          RETURN
```

- c. A menu will now appear which lists the tests available to exercise the emulator (figure 4-3). The test displayed in a reverse video field is the test which will be executed if the **start** softkey is pressed. To select a test other than the one which is currently highlighted, press the **next test** softkey. To stop a test or to exit the PV, press the **end** softkey. The **cycle** softkey is used to cycle through the tests executing each test once per pass. When the **cycle** softkey is used, the display maintains a count of the number of times each test is executed (# Test) and the number of failures detected (# Fail).
- d. Press the **cycle** softkey. The reverse video field steps through the tests indicating each test is executing properly. To terminate the tests press the **end** softkey. This returns the display to the Option Test PV Menu shown in figure 4-3.
- e. When a failure is observed, refer to the following sections for information about the operation of the tests and troubleshooting procedures.

4-7. PROCESSOR CONTROL TEST.

4-8. The Processor Control Test consists of four subtests used to check basic emulator functions. The four tests are: Reset, Release, Background, and Run. A description of each test is provided below. Figure 4-4 shows the PV Selection Menu with the Processor Control Tests selected and the Processor Control Test summary display.

4-9. **RESET.** In the Reset Test, the mainframe processor initializes the emulator by directing the LDEFIB line to go low. The emulator status registers are then compared to the expected status. Any status which does not agree with the expected status causes an error to be reported. Failures detected by the Reset Test indicate a failure of the Emulator Control Board or the emulation processor in the Emulator Pod. The following tests are not valid when failures are detected in the Reset Test.

4-10. BACKGROUND. In the Background Test, the mainframe processor writes several data patterns to all locations of the background memory on the Emulator Control Board. The data is then read back out and checked for errors. Failures in this test indicate a problem on the Emulation Control Card. The following tests may not be valid if the Background Test fails.

4-11. RELEASE. In the Release Test, the mainframe processor loads a program file into background memory and directs the emulation processor to execute this program. The program modifies a specific memory location in background memory. The mainframe processor allows enough time for the emulation processor to execute the program and then checks to see that the memory location has been modified. A failure detected by this test indicates an problem in the Emulator Control Board or the Emulator Pod.

4-12. RUN. In the Run Test, the mainframe processor checks for a trap condition. A background memory location is interrogated and then the emulator status registers are read and compared with the expected status. Any status bit which does not compare will be reported as a failure. Failures indicate a problem with either the Emulation Control Card or the Emulator Pod.

4-13. EMULATION BUS TEST.

4-14. The Emulation Bus Test verifies the operation of the emulation bus, address and data lines. The emulation bus is used to connect the Emulator Control Card to the optional Emulation Memory Control Card and Logic Analyzer. This test requires the Static Memory Control Card PV, Processor Control Test, be successfully completed. The 6800/6802 Processor Control Test must also be successfully completed prior to running the Emulation Bus Test. The Emulation Bus Test consists of two subtests; the Data Test and the Address Test. The Internal RAM Test status line provides notification whenever the internal RAM of a 6802 is involved in these tests. The PV selection menu with the Emulation Bus Test selected and the Emulation Bus Test summary display are shown in figure 4-5.

4-15. DATA TEST. The mainframe processor maps two blocks of emulation memory, one at each end of the 64K address range, for this test. In the first part of the test the memory is loaded through the Static Memory Control Card and reads back through the Emulation Control Card. In the second part of this test the inverse pattern is written to emulation memory through the Emulator Control Board and read back through the Static Memory Controller. A failure detected by the Emulation Bus Test indicates a problem on the Emulator Control Board, the Emulator Pod or the Static Memory Control Card.

4-16. ADDRESS TEST. The Address Test operates similarly to the data test except a pattern of addresses are used and the data lines are assumed to be good. Any failure detected by the Address Test is reported as an address error and indicates the same possible sources for errors.

4-17. INTERNAL RAM TEST. When a 6802 Emulator Pod user plug is installed in a target system, and the RAM Enable (RE) line is high, the Emulation Bus Tests will exercise the address and data lines to the on-board RAM in the pod during the tests. This results in the "Internal RAM Enabled" display. For a 6800 pod, or when the RE line is low, "Internal RAM Disabled" is displayed.

4-18. FOREGROUND TEST.

4-19. The Foreground Test checks the ability to emulate in the foreground memory. The Foreground Test is comprised of six subtests: the Release Test, the Run Test, the Processor Break Test, the Illegal Memory Reference Test, the Write to ROM Test, and the Illegal Opcode Test. A description of each test is provided below. The PV selection menu with the Foreground Test selected and the Foreground Test summary display are provided in figure 4-6.

4-20. RELEASE TEST. The Release Test loads a program into background memory and releases the emulation processor to execute the program. The program modifies a memory location. After a suitable time the mainframe processor examines the memory location which was to be modified. If the memory location contains the proper information the test passes, if not the test fails. A failure noted in this test indicates a problem in either the Emulator Pod or the Emulator Control Board.

4-21. RUN TEST. For the Run Test, the mainframe processor maps two blocks of emulation memory. From 0-1K is mapped as emulation RAM, and from 2-3K is mapped as emulation ROM. All remaining memory is mapped as illegal memory. A self-modifying program is loaded into the emulation RAM area and executed. The mainframe processor monitors the emulation status. If the status does not compare with the expected status, or if the program does not modify properly, the test fails. An error in this test indicates a problem on either the Emulator Control Board or the Emulation Memory Controller.

4-22. PROCESSOR BREAK. The mainframe processor compares the status registers of the Emulator Control Board during each test of the foreground tests. The received status is checked against expected values for break status, or last opcode address. The test fails for any miscompare. A failure in the processor break test indicates a problem in the emulator pod or the Emulation Control Card.

4-23. ILLEGAL MEMORY REFERENCE. In the Illegal Memory Reference Test, the mainframe processor causes the emulator to execute a foreground program which references an illegal memory location. The mainframe processor then verifies that a memory break and proper background operation occurred and verifies the last opcode register and emulation status. Any incorrect status or address causes the test to fail and indicates a problem in the Emulator Control Board or the emulator pod.

4-24. WRITE TO ROM. The mainframe processor causes the emulator to run a foreground program which attempts to write to memory space designated as ROM. The mainframe processor then checks that a break operation occurs correctly as with the Illegal Memory Reference Test previously described. Any failure indicates a problem in the Emulator Control Board or the emulator pod.

4-25. ILLEGAL OPCODE. The mainframe processor causes the emulator to execute a program which contains several illegal opcodes and verifies that a break operation occurs correctly. A failure in this test indicates a problem on the Emulator Control Board or the emulator pod.

4-26. ANALYSIS STIMULUS.

4-27. The Analysis Stimulus Test consists of four subtests: the Analysis Status Test, the Emulation Interrupt Test, the Address Test and the Data Test. The purpose of this test is to verify the operation of the optional Logic Analyzer. These tests require that the performance verification tests for the Logic Analyzer described in the Logic Analyzer Model 64300A manual, be successfully completed. All PV tests described above must also be completed. The Analysis Stimulus Test checks the interface with the optional Logic Analyzer and can only be executed when one is present. The PV Selection menu with the Analysis Stimulus Test selected and the Analysis Stimulus summary display are shown in figure 4-7. Figure 4-8 illustrates the single line modification to the PV Selection menus of the optional Logic Analyzer (Analysis) and Emulation Memory Controller (Static Memory) PV Tests. The added line in the Analysis PV is "Select slot #9 for Emulator stimulus tests". The added line to the Memory PV is "Select slot #9 for Emulation Bus and Foreground tests".

4-28. ANALYSIS STATUS. The Analysis Status Test verifies the ability to recognize a trigger event and to store data. When an error is detected a problem is indicated in the bus cable, the Logic Analyzer, or the Emulator Control Board.

4-29. EMULATION INTERRUPT. The Emulation Interrupt Test verifies the ability of the Logic Analyzer to stop the emulator, and the ability of the mainframe processor to recognize that the emulator has been stopped. Any failures detected indicate a problem with the Emulator Control Board, the bus cables or the Logic Analyzer.

4-30. ADDRESS TEST. The Address Test is similar to the Data Test except a failure is assumed to be in the addressing logic. Any error indicates a problem in the Logic Analyzer or the bus cables.

4-31. DATA TEST. In the Data Test, the mainframe processor causes the emulator to provide predetermined data to the Logic Analyzer. The data captured by the Logic Analyzer is then checked against the expected results. A failure indicates a problem in the Logic Analyzer or the bus cables.

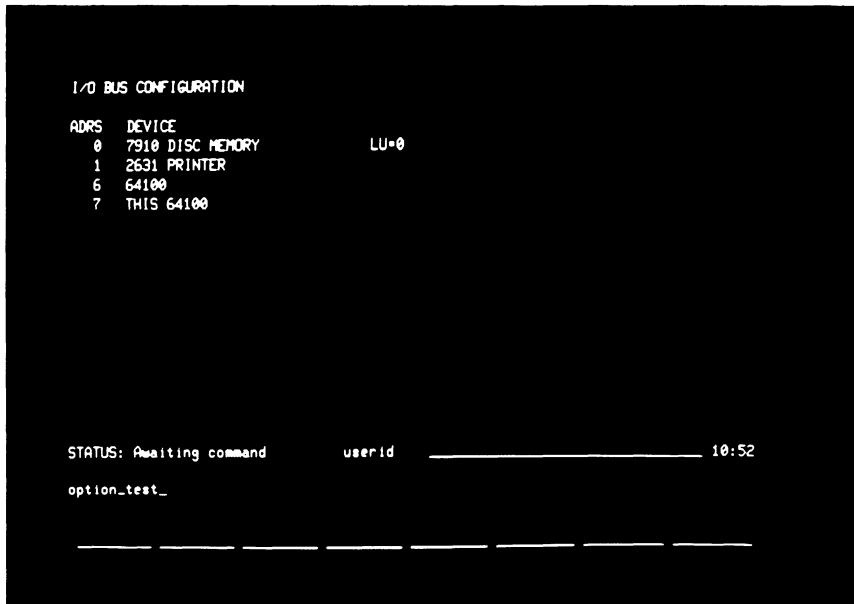


Figure 4-1. Awaiting Command Display

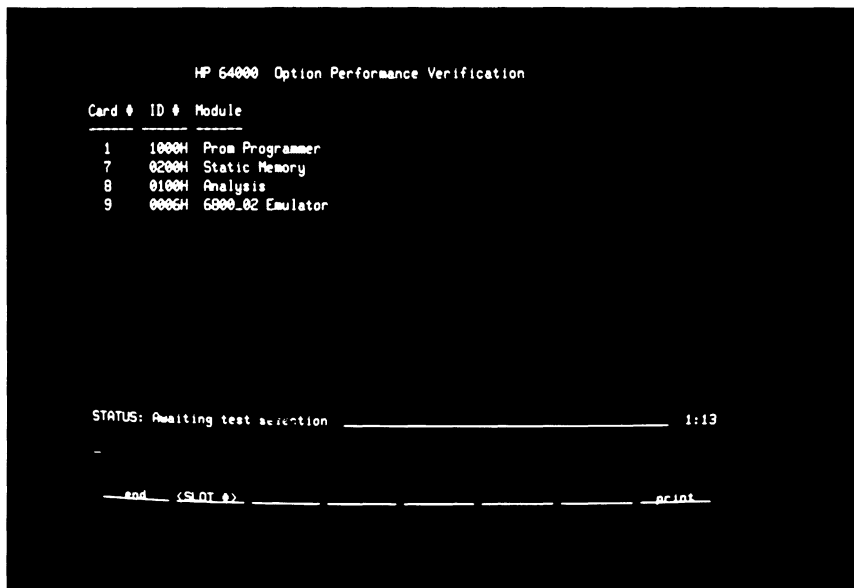


Figure 4-2. Option Map

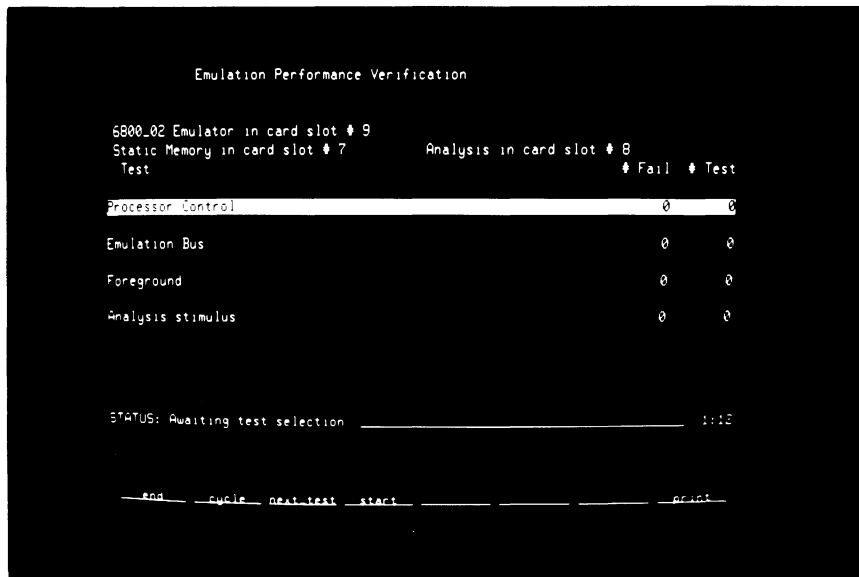


Figure 4-3. Emulator PV Menu

```
Emulation Performance Verification

6800_02 Emulator in card slot # 9
Static Memory in card slot # 7      Analysis in card slot # 8
Test                                # Fail # Test

Processor Control                    0      0
Emulation Bus                       0      0
Foreground                           0      0
Analysis stimulus                    0      0

STATUS: Awaiting test selection _____ 1:12
-
  end  cycle  next test  start  _____  print
```

Processor Control Test Selected

```
Emulation Performance Verification
Processor Control Test

6800_02 Emulator in card slot # 9
Static Memory in card slot # 7      Analysis in card slot # 8
Test                                # Fail # Test

Reset                               Status=0000  0      64
Background                          Error=00      0
Release                              0
Run                                  Status=0000  0

STATUS: Test in progress _____ 1:14
-
  end  _____  print
```

Test Summary

Figure 4-4. Process Control Test Displays

```

Emulation Performance Verification

6800_02 Emulator in card slot # 9
Static Memory in card slot # 7      Analysis in card slot # 8
Test                                # Fail # Test

Processor Control                    0    93
Emulation Bus                        0    0
Foreground                           0    0
Analysis stimulus                     0    0

STATUS: Awaiting test selection _____ 1:16
-
end      cycle      DEAT TEST      START      PRINT
    
```

Emulation Bus Test Selected

```

Emulation Performance Verification
Emulation Bus Test

6800_02 Emulator in card slot # 9
Static Memory in card slot # 7      Analysis in card slot # 8
Test                                # Fail # Test

Data                                  Read=0000    0    50
                                      Write=0000    0
Address                                Error=0000    0

Internal ram disabled

STATUS: Test in progress _____ 1:16
-
end      PRINT
    
```

Test Summary

Figure 4-5. Emulation Bus Test Displays

```
Emulation Performance Verification

6800_02 Emulator in card slot # 9
Static Memory in card slot # 7      Analysis in card slot # 8
Test                                # Fail # Test
Processor Control                    0     93
Emulation Bus                        0     67
Foreground                            0     0
Analysis stimulus                     0     0

STATUS: Awaiting test selection _____ 1:17

-
-
- end - cycle - next test - start - print -
```

Foreground Test Selected

```
Emulation Performance Verification
Foreground Test

6800_02 Emulator in card slot # 9
Static Memory in card slot # 7      Analysis in card slot # 8
Test                                # Fail # Test
Release                               0     206
Run                                   Status=0000 11
Processor Break                       Status=0000 11
Illegal Memory Reference              0
Write to Rom                          0
Illegal Opcode                        Status=FFFF 45

STATUS: Test in progress _____ 1:18

-
-
- end - print -
```

Test Summary

Figure 4-6. Foreground Test Displays

```

Emulation Performance Verification

6800_02 Emulator in card slot # 9
Static Memory in card slot # 7      Analysis in card slot # 8
Test                                # Fail # Test
Processor Control                    0      99
Emulation Bus                        0      97
Foreground                           66     250
Analysis stimulus                     0      0

STATUS: Awaiting test selection _____ 1:20
-
end _____ print
    
```

Analysis Stimulus Test Selected

```

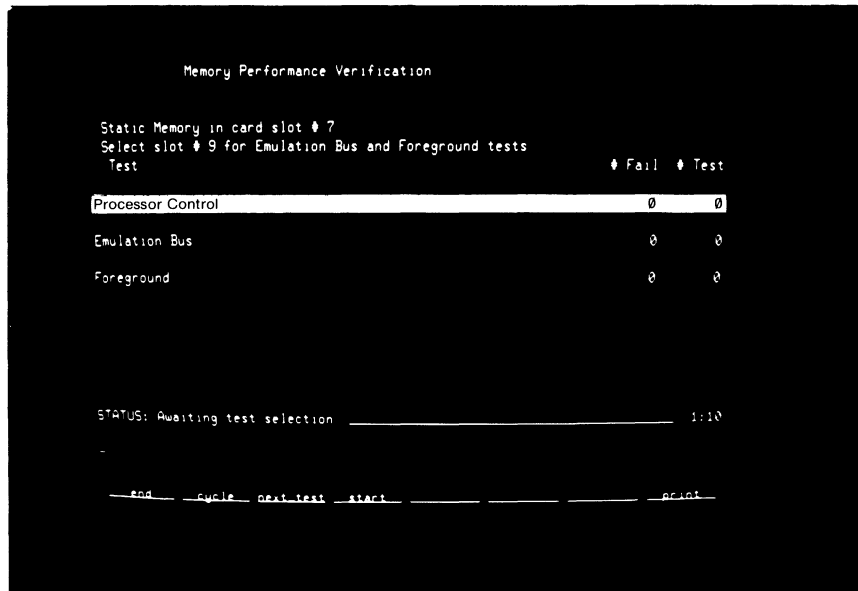
Emulation Performance Verification
Emulator Stimulus Test

6800_02 Emulator in card slot # 9
Static Memory in card slot # 7      Analysis in card slot # 8
Test                                # Fail # Test
Analysis Status      Trace Point      0      124
                    Measurement Complete 0
Emulation Interrupt  Trace Point      Status=0000 0
                    Measurement Complete Status=0000 0
Address              Error=0000      0
Data                 Error=0000      0

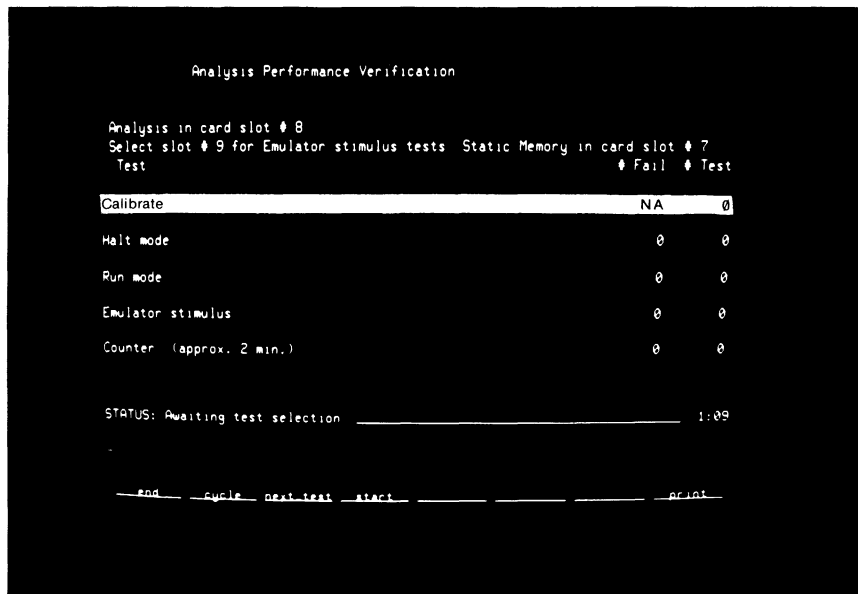
STATUS: Test in progress _____ 1:22
-
end _____ print
    
```

Test Summary

Figure 4-7. Analysis Stimulus Test Displays



Memory PV Display Changes



Analysis PV Display Changes

Figure 4-8. Changes to Memory and Analysis PV Display

SECTION V
ADJUSTMENTS

There are no adjustments to be made on these emulators.

SECTION VI
REPLACEABLE PARTS

6-1. INTRODUCTION.

6-2. This section contains information needed to order replacement parts. Table 6-1 lists the Blue Stripe Program replaceable assemblies. Table 6-2 lists reference designators and abbreviations used throughout the manual. Table 6-3 lists the replaceable parts for the 6800 Emulator Pod. Table 6-4 lists the replaceable parts for the 6802 Emulator Pod. The replaceable parts are listed in assembly/reference designator order. Table 6-5 contains the manufacturers' names and addresses corresponding to the five digit code numbers given in the parts lists.

6-3. BLUE STRIPE PROGRAM.

6-4. The Blue Stripe Program offers factory repaired and tested replacement boards, on an exchange basis only. Exchange assemblies carry a part number different from brand new assemblies and are available at a reduced cost. Exchange assemblies are available through the Hewlett-Packard Corporate Parts Center. Table 6-1 lists both the exchange and the new assembly Part Numbers for each printed circuit assembly.

Table 6-1. Blue Stripe Exchange Assembly Part Numbers

Model Number	Exchange	New
64211A	64211-69501	64211-66501
64212A	64212-69501	64212-66501
64213A	64213-69501	64213-66501

6-5. ABBREVIATIONS.

6-6. Table 6-2 lists the reference designators and abbreviations used in the parts list, the schematics and throughout the manual. Abbreviations are always presented in upper case in the parts list. Abbreviations using both upper and lower case letters are used in the schematics and other parts of the manual. This results in two forms of the abbreviation. Table 6-2 lists only the upper case form of the abbreviation.

6-7. REPLACEABLE PARTS LIST.

6-8. Table 6-3 is the list of replaceable parts for the Model 64212A 6800 Emulator Pod. Table 6-4 is the list of replaceable parts for the Model 64213A 6802 Emulator Pod. The parts lists are organized as follows:

- a. Chassis-mounted parts in alphanumeric order by reference designation.
- b. Electrical assemblies and their components in alphanumeric order by reference designation.
- c. Miscellaneous.

The information given for each part consists of the following:

- a. The Hewlett-Packard part number and the check digit.
- b. The total quantity in the instrument.
- c. The description of the part.
- d. A five digit code indicating the manufacturer.

- e. The manufacturers' part number.

The total quantity is given only at the first appearance of the part in the parts list.

6-9. MANUFACTURERS' CODES.

6-10. Table 6-5 gives the manufacturers' codes organized in the order they appear in the parts list. The five digit manufacturers' code is followed by the name address and zip code of the manufacturer.

6-11. ORDERING INFORMATION.

6-12. To order a part listed in the replaceable parts table, quote the Hewlett-Packard part number and check digit, indicate the quantity required, and address the order to the nearest Hewlett-Packard Sales/Service Office.

6-13. To order a part that is not listed in the replaceable parts table include the instrument model number, instrument repair number, the description and function of the part, and the number of parts required. Address the order to the nearest Hewlett-Packard Sales/Service Office.

6-14. DIRECT MAIL ORDER SYSTEM.

6-15. Within the USA Hewlett-Packard can supply parts through the direct mail order system. The advantages of using the system are as follows:

- a. Direct ordering and shipment from the Hewlett-Packard parts center in Mountain View, California.
- b. No minimum amount on any mail order (there is a minimum order amount for parts ordered through a local HP office when the order requires billing and invoicing).
- c. Prepaid transportation (there is a small handling charge for each order).
- d. No-invoices. To receive these advantages, a check or money order must accompany each order.

6-16. Mail-order forms and specific ordering information are available through your local HP office. Addresses and phone numbers are provided at the back of this manual.

Table 6-2. Reference Designators and Abbreviations

REFERENCE DESIGNATORS							
A	= assembly	F	= fuse	MP	= mechanical part	U	= integrated circuit
B	= motor	FL	= filter	P	= plug	V	= vacuum, tube, neon bulb, photocell, etc
BT	= battery	IC	= integrated circuit	Q	= transistor	VR	= voltage regulator
C	= capacitor	J	= jack	R	= resistor	W	= cable
CP	= coupler	K	= relay	RT	= thermistor	X	= socket
CR	= diode	L	= inductor	S	= switch	Y	= crystal
DL	= delay line	LS	= loud speaker	T	= transformer	Z	= tuned cavity network
DS	= device signaling (lamp)	M	= meter	TB	= terminal board		
E	= misc electronic part	MK	= microphone	TP	= test point		
ABBREVIATIONS							
A	= amperes	H	= henries	N/O	= normally open	RMO	= rack mount only
AFC	= automatic frequency control	HDW	= hardware	NOM	= nominal	RMS	= root-mean square
AMPL	= amplifier	HEX	= hexagonal	NPO	= negative positive zero (zero temperature coefficient)	RWV	= reverse working voltage
BFO	= beat frequency oscillator	HG	= mercury	NPN	= negative-positive-negative	S-B	= slow-blow
BE CU	= beryllium copper	HR	= hour(s)	NRFR	= not recommended for field replacement	SCR	= screw
BH	= binder head	HZ	= hertz	NSR	= not separately replaceable	SE	= selenium
BP	= bandpass	IF	= intermediate freq	OB	= order by description	SECT	= section(s)
BRS	= brass	IMPG	= impregnated	OH	= oval head	SEMICON	= semiconductor
BWO	= backward wave oscillator	INCD	= incandescent	OX	= oxide	SI	= silicon
CCW	= counter-clockwise	INCL	= include(s)	P	= peak	SIL	= silver
CER	= ceramic	INS	= insulation(ed)	PC	= printed circuit	SL	= slide
CMO	= cabinet mount only	INT	= internal	PF	= picofarads= 10 ⁻¹² farads	SPG	= spring
COEF	= coefficient	K	= kilo=1000	PH BRZ	= phosphor bronze	SPL	= special
COM	= common	LH	= left hand	PHL	= phillips	SST	= stainless steel
COMP	= composition	LIN	= linear taper	PIV	= peak inverse voltage	SR	= split ring
COMPL	= complete	LK WASH	= lock washer	PNP	= positive-negative-positive	STL	= steel
CONN	= connector	LOG	= logarithmic taper	P/O	= part of	TA	= tantalum
CP	= cadmium plate	LPF	= low pass filter	POLY	= polystyrene	TD	= time delay
CRT	= cathode-ray tube	M	= milli=10 ⁻³	PORC	= porcelain	TGL	= toggle
CW	= clockwise	MEG	= meg=10 ⁶	POS	= position(s)	THD	= thread
DEPC	= deposited carbon	MET FLM	= metal film	POT	= potentiometer	TI	= titanium
DR	= drive	MET OX	= metallic oxide	PP	= peak-to-peak	TOL	= tolerance
ELECT	= electrolytic	MFR	= manufacturer	PT	= point	TRIM	= trimmer
ENCAP	= encapsulated	MHZ	= mega hertz	PWV	= peak working voltage	TWT	= traveling wave tube
EXT	= external	MINAT	= miniature	RECT	= rectifier	U	= micro=10 ⁻⁶
F	= farads	MOM	= momentary	RF	= radio frequency	VAR	= variable
FH	= flat head	MOS	= metal oxide substrate	RH	= round head or right hand	VDCW	= dc working volts
FIL H	= fillister head	MTG	= mounting			W/	= with
FXD	= fixed	MY	= "mylar"			W	= watts
G	= giga (10 ⁹)	N	= nano (10 ⁻⁹)			WIV	= working inverse voltage
GE	= germanium	N/C	= normally closed			WW	= wirewound
GL	= glass	NE	= neon			W/O	= without
GRD	= ground(ed)	NI PL	= nickel plate				

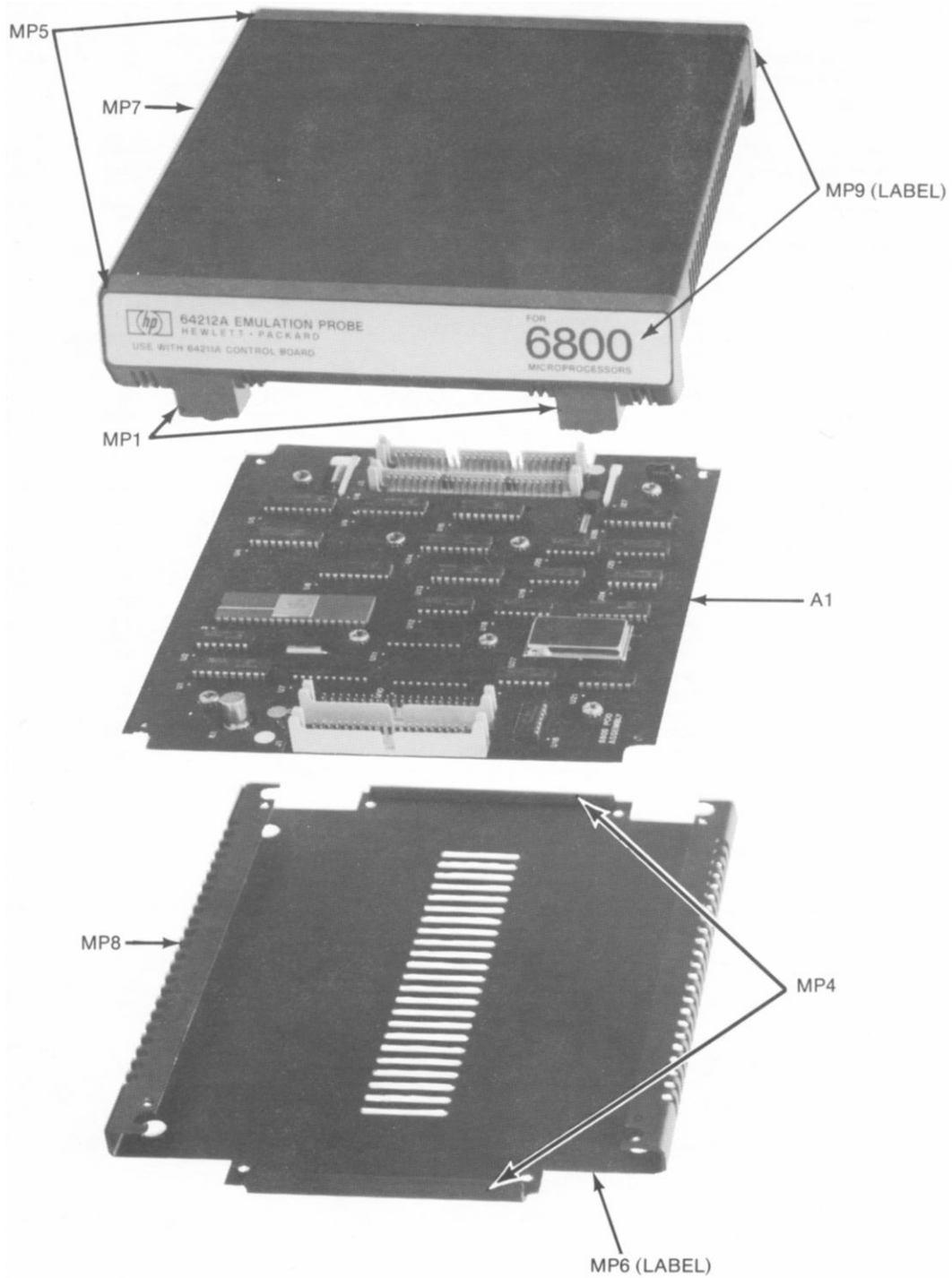


Figure 6-1. 6800 Illustrated Parts Breakdown (Sheet 1 of 2)

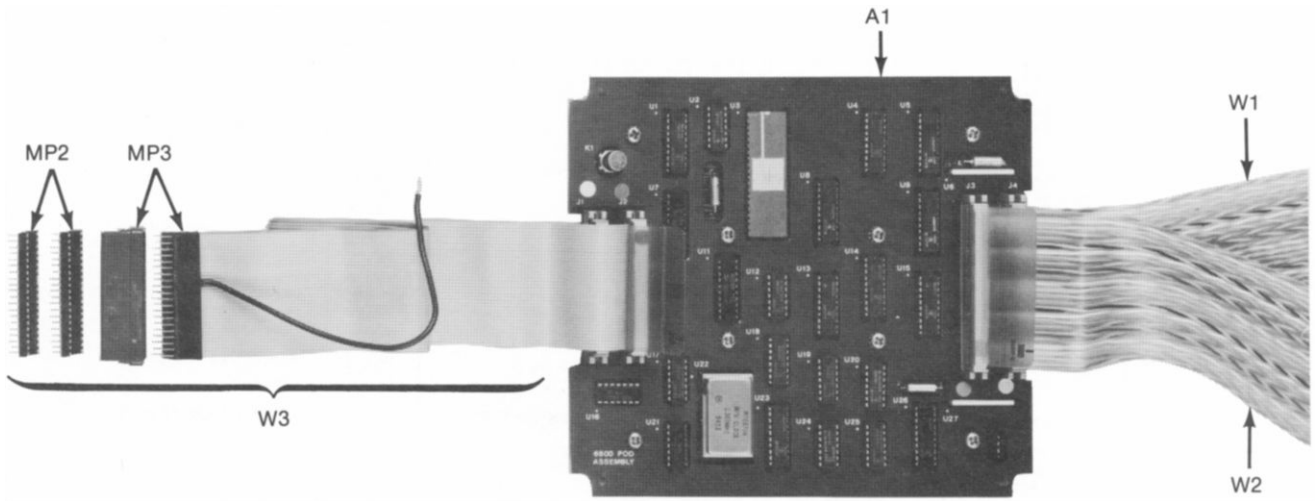


Figure 6-1. 6800 Illustrated Parts Breakdown (Sheet 2 of 2)

Table 6-3. 6800 Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	64212-62101	8	1	BOARD-POD 6800	28480	64212-62101
A1C1	0160-5428	6	21	CAPACITOR-FXD	28480	0160-5428
A1C2	0180-1746	5	4	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020R2
A1C3	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C4	0160-3443	1	5	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C5	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C6	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C7	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C8	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C9	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020R2
A1C10	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C11	0160-3619	3	1	CAPACITOR-FXD 680PF +-10% 100VDC CER	28480	0160-3619
A1C12	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C13	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C14	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C15	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C16	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C17	0160-3677	3		CAPACITOR-FXD 1000PF +-20% 250VDC CER	28480	0160-3677
A1C18	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C19	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C20	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C21	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C22	0160-3443	1		CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C23	0180-1746	5		CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	150D156X9020R2
A1C24	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C25	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C26	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C27	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C28	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C29	0160-5428	6		CAPACITOR-FXD	28480	0160-5428
A1C30	0140-0192	9		CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A1CR1	1901-0040	1	2	DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR2	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1CR3	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1CR4	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1CR5	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1CR6	1901-0040	1		DIODE-SWITCHING 30V 50MA 2NS DO-35	28480	1901-0040
A1CR7	1901-0535	9		DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1HW1	2360-0113	2	8	SCREW-MACH 6-32 .25-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
A1J1	1251-4563	2	2	CONNECTOR 40-PIN M POST TYPE	28480	1251-4563
A1J2	1251-4563	2		CONNECTOR 40-PIN M POST TYPE	28480	1251-4563
A1J3	1251-4427	7	2	CONNECTOR 50-PIN M POST TYPE	28480	1251-4427
A1J4	1251-4427	7		CONNECTOR 50-PIN M POST TYPE	28480	1251-4427
A1K1	0490-0670	9	1	RELAY 2C 5VDC-COIL 1A 28VDC	28480	0490-0670
A1L1	9100-1631	8	2	INDUCTOR RF-CH-MLD 56UH 5% .166DX.385LG	28480	9100-1631
A1MP1	64212-04102	7	1	PLATE-COLD 6800	28480	64212-04102
A1MP2	7120-8723	3		LABEL-WHITE DOT	28480	7120-8723
A1MP3	7124-0266	1		LABEL-BLUE DOT	85480	QD25 TAPE B-810-BL
A1MP4	7124-0269	4		LABEL-RED DOT	85480	QD25 TAPE B-810-RD
A1MP5	7124-0270	7		LABEL-YELLOW DOT	85480	QD25 TAPE B-810-YL
A1R1	0698-3430	5	3	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A1R2	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A1R3	0684-5611	9	2	RESISTOR 560 10% .25W FC TC=-400/+600	01121	CB5611
A1R4	0684-1021	7	5	RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R5	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R6	0757-0394	0	3	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R7	0684-5611	9		RESISTOR 560 10% .25W FC TC=-400/+600	01121	CB5611
A1R8	0757-0394	0		RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R9	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R10	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R11	0757-0447	4	2	RESISTOR 16.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1622-F
A1R12	0698-3156	2	2	RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A1R13	0684-1021	7		RESISTOR 1K 10% .25W FC TC=-400/+600	01121	CB1021
A1R14	0757-0389	3	1	RESISTOR 33.2 1% .125W F TC=0+-100	24546	C4-1/8-T0-33R2-F
A1R15	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
A1R16	0757-0408	7		RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-T0-243R-F
A1U1	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
A1U2	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U3	1820-2358	6	1	IC-68800	28480	1820-2358
A1U4	1820-1676	9	8	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U5	1820-1624	7	7	IC BFR TTL S OCTL 1-INP	01295	SN74S241N

Table 6-3. 6800 Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1U6	1810-0430	0	4	NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
A1U7	1820-2024	3	3	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U8	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U9	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U10	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U11	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
A1U12	1820-0686	9	2	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A1U13	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U14	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U15	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U16	1820-1201	6		IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U17	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
A1U18	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A1U19	1820-0688	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
A1U20	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
A1U21	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U22	1820-1637	2	1	IC MICPROC-ACCESS NMOS	04713	MC6870A
A1U23	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A1U24	1820-1210	7		IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A1U25	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
A1U26	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A1U27	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
A1XU1	1200-0637	6	13	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU2	1200-0474	9	9	SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU3	1200-0624	1	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0624
A1XU4	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU5	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU7	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU8	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU9	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU10	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU11	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU12	1200-0474	9		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU13	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU14	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU15	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU16	1200-0474	9		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU17	1200-0474	9		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU18	1200-0473	8	1	SOCKET-IC 16-CONT DIP DIP-SLDR	28480	1200-0473
A1XU19	1200-0474	9		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU20	1200-0474	9		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU21	1200-0474	9		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU22	1200-0622	9	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0622
A1XU23	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
A1XU24	1200-0474	9		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU25	1200-0474	9		SOCKET-IC 14-CONT DIP-SLDR	28480	1200-0474
A1XU26	1200-0637	6		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0637
HW1	2200-0107	6	16	SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
MP1	0403-0179	0	4	BUMPER-PLASTIC	28480	0403-0179
MP2	1200-0682	1	2	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0682
MP3	4040-1573	4	1	HOOD-PIN GUARD	28480	4040-1573
MP4	4320-0095	7	2	CHANNEL-RUBBER	28480	4320-0095
MP5	5041-1575	9	2	PROBE-ENDCAP	28480	5041-1575
MP6	5957-2260	2	1	LABEL-MADE IN USA	28480	5957-2260
MP7	64202-04101	4	1	COVER-TOP	28480	64202-04101
MP8	64202-04102	5	1	COVER-BOTTOM	28480	64202-04102
MP9	7120-8525	3	2	LABEL-IDENT	28480	7120-8525
W1	64202-61601	9	1	CABLE-EMULATOR INPUT	28480	64202-61601
W2	64202-61602	0	1	CABLE-EMULATOR INPUT	28480	64202-61602
W3	64212-61601	1	1	CABLE ASSEMBLY-6800	28480	64212-61601

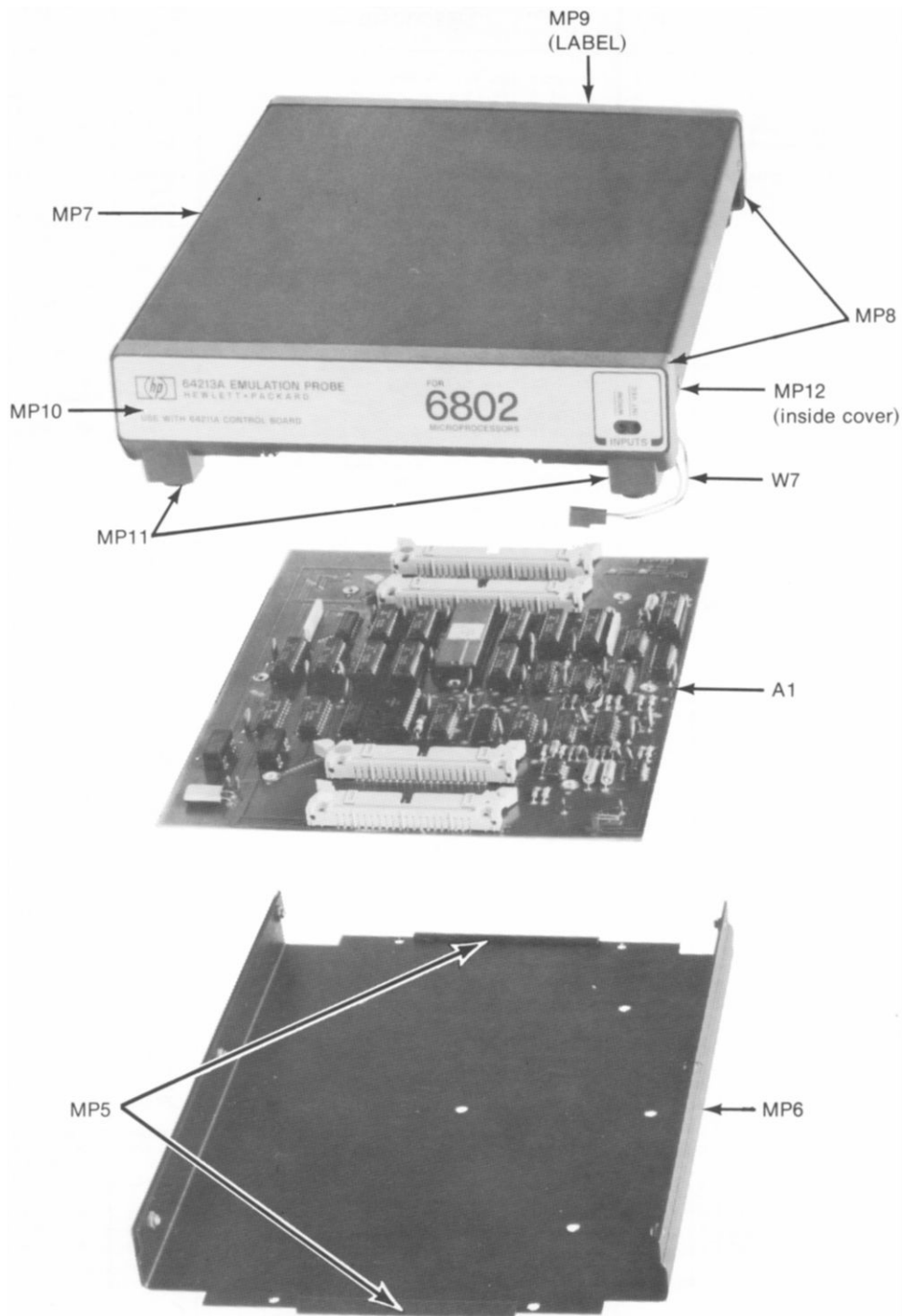
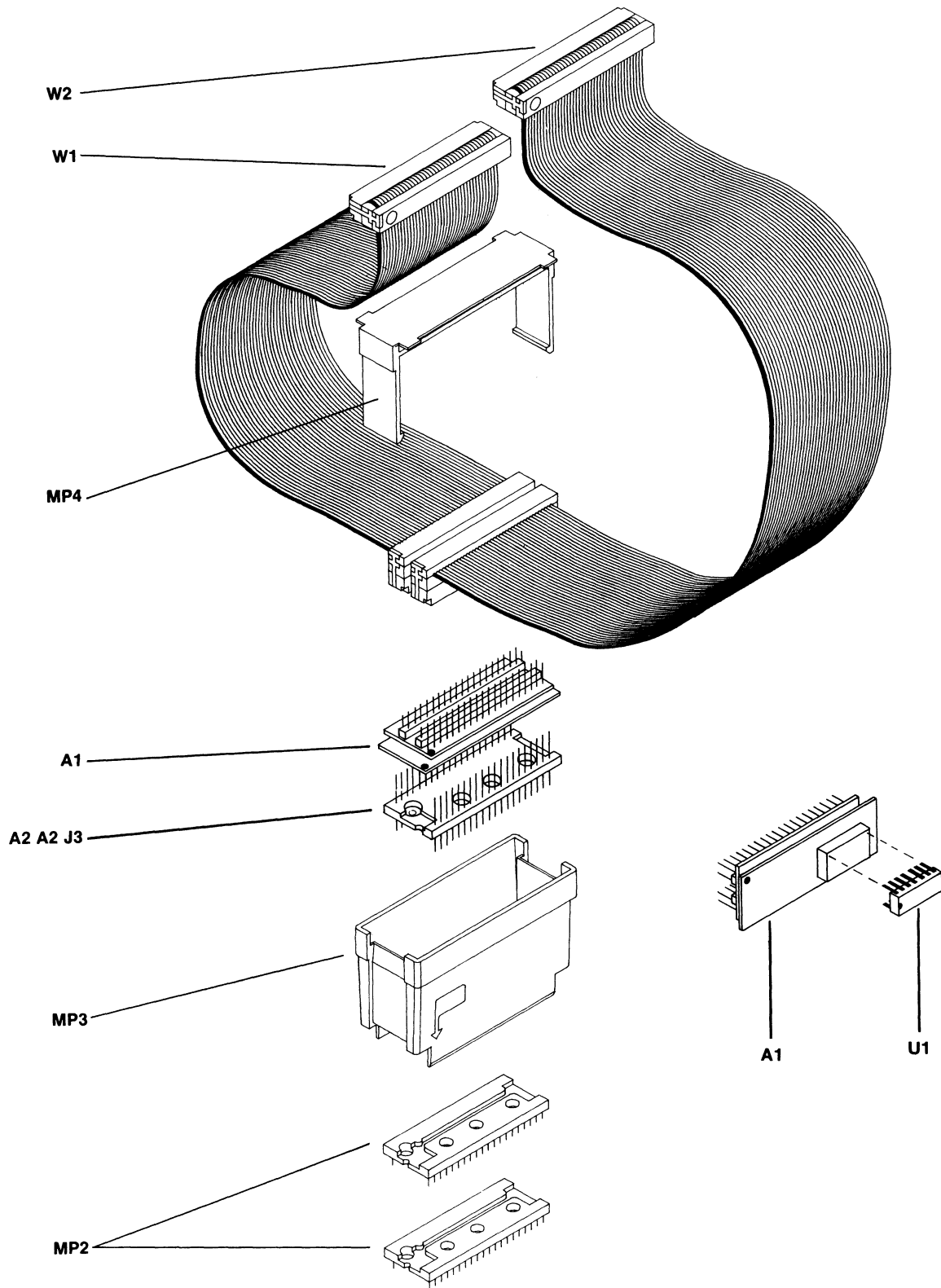


Figure 6-2. 6802 Illustrated Parts Breakdown (Sheet 1 of 2)



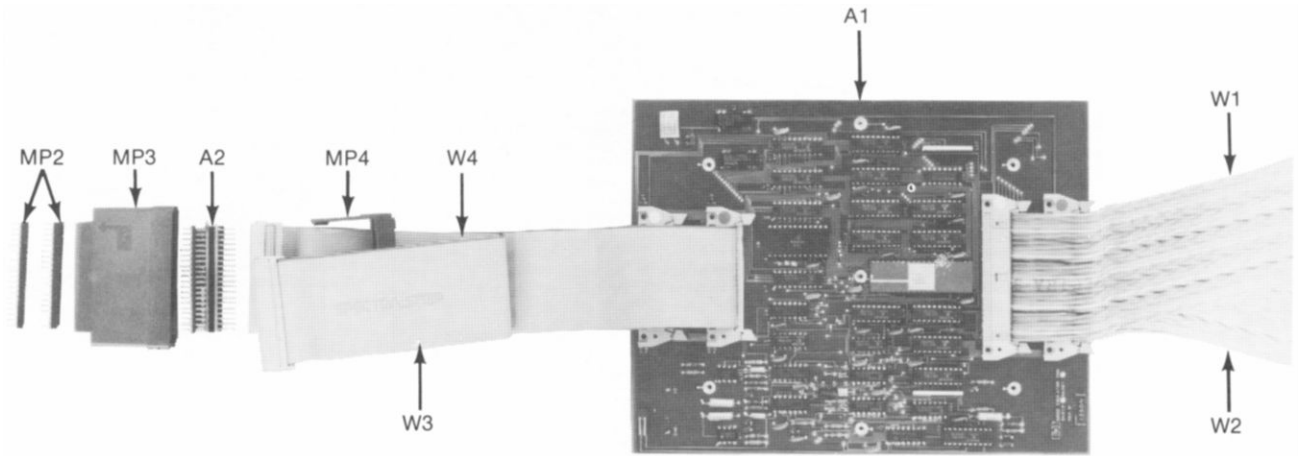


Figure 6-2. 6802 Illustrated Parts Breakdown (Sheet 2 of 2)

Table 6-4. 6802 Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	64213-66501	1	2	POD ASSEMBLY-EMULATOR 6802	28480	64213-66501
A1C1	0160-3569	2	2	CAPACITOR-FXD 27PF +-5% 100VDC CER 0+-30	28480	0160-3569
A1C2	0160-3569	2	2	CAPACITOR-FXD 27PF +-5% 100VDC CER 0+-30	28480	0160-3569
A1C3	0180-0374	3	2	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	1500106X9020R2
A1C4	0180-0374	3	2	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	1500106X9020R2
A1C5	0160-3470	4	4	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A1C6	0160-3470	4	4	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A1C7	0180-0309	4	2	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	1500475X0010A2
A1C8	0160-3470	4	4	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A1C9	0180-0309	4	4	CAPACITOR-FXD 4.7UF+-20% 10VDC TA	56289	1500475X0010A2
A1C10	0160-2055	9	27	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C11	0160-3677	3	2	CAPACITOR-FXD 1000PF +-20% 250VDC CER	28480	0160-3677
A1C12	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C13	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C14	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C15	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C16	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C17	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C18	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C19	0140-0192	9	2	CAPACITOR-FXD 68PF +-5% 300VDC MICA	72136	DM15E680J0300WV1CR
A1C20	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C20	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C21	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C22	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C23	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C24	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C25	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C26	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C27	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C28	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C29	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C30	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C31	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C32	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C33	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C34	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C35	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C36	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C37	0160-2055	9	9	CAPACITOR-FXD .01UF +80-20% 100VDC CER	28480	0160-2055
A1C38	0180-1746	5	5	CAPACITOR-FXD 15UF+-10% 20VDC TA	56289	1500156X9020R2
A1C39	0160-3470	4	4	CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A1C40	0160-3443	1	1	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1C41	0160-3443	1	1	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A1CR1	1901-0535	9	7	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1CR2	1901-0535	9	7	DIODE-SM SIG SCHOTTKY	28480	1901-0535
A1J1	1251-5652	2	2	CONNECTOR 40-PIN M POST TYPE	28480	1251-5652
A1J2	1251-5652	2	2	CONNECTOR 40-PIN M POST TYPE	28480	1251-5652
A1J3	1251-5653	3	2	CONNECTOR 50-PIN M POST TYPE	28480	1251-5653
A1J4	1251-5653	3	3	CONNECTOR 50-PIN M POST TYPE	28480	1251-5653
A1J5	1251-4836	2	1	CONNECTOR 2-PIN M METRIC POST TYPE	28480	1251-4836
A1K1	0490-0617	4	2	RELAY-REED 1C 250MA 28VDC 5VDC-COIL	28480	0490-0617
A1K2	0490-0617	4	2	RELAY-REED 1C 250MA 28VDC 5VDC-COIL	28480	0490-0617
A1L1	9170-0016	8	1	CORE-SHIELDING BEAD	28480	9170-0016
A1L2	9100-1631	8	2	INDUCTOR RF-CH-MLD 56UH 5% .166DX.385LG	28480	9100-1631
A1MP1	1251-5595	2	8	POLARIZING KEY-POST CONN	28480	1251-5595
A1R1	0757-0417	8	2	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A1R2	0757-0411	2	3	RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-T0-332R-F
A1R3	0757-0280	3	7	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R4	0757-0411	2	2	RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-T0-332R-F
A1R5	0757-0452	1	1	RESISTOR 27.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2742-F
A1R6	0757-0449	6	1	RESISTOR 20K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2002-F
A1R7	0757-0458	7	1	RESISTOR 51.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5112-F
A1R8	0757-0462	3	1	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
A1R9	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
A1R10	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
A1R11	0757-0280	3	3	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R12	0757-0280	3	3	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R13	0757-0411	2	2	RESISTOR 332 1% .125W F TC=0+-100	24546	C4-1/8-T0-332R-F
A1R14	0757-0417	8	2	RESISTOR 562 1% .125W F TC=0+-100	24546	C4-1/8-T0-562R-F
A1R15	0757-0408	7	2	RESISTOR 243 1% .125W F TC=0+-100	24546	C4-1/8-T0-243R-F

Table 6-4. 6802 Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1R16	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R17	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R18	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R19	0757-0280	3		RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
A1R20	0757-0447	4		RESISTOR 16.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1622-F
A1R21	0698-3156	2		RESISTOR 14.7K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1472-F
A1TP1	0360-2050	8	2	TERMINAL-TEST POINT	28480	0360-2050
A1TP2	0360-2050	8		TERMINAL-TEST POINT	28480	0360-2050
A1U1	1826-0851	2	1	IC-MOS VOLTAGE CONVERTER	28480	1826-0851
A1U2	1820-0217	2	1	IC OP AMP GP 8-DIP-P PKG	28480	1820-0217
A1U3	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
A1U4	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
A1U5	1820-1201	6	2	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
A1U6	1820-1208	3	2	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
A1U7	1820-1918	2	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
A1U8	1818-1751	6	1		28480	1818-1751
A1U9	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
A1U10	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A1U11	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
A1U12	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
A1U13	1820-0688	1	2	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
A1U14	1820-0685	8	2	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
A1U15	1820-1210	7	2	IC GATE TTL LS AND-OR-INV DUAL 2-INP	01295	SN74LS51N
A1U16	1820-1633	8	5	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A1U17	1820-2752	4	1		28480	1820-2752
A1U18	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U19	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U20	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A1U21	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U22	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
A1U23	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
A1U24	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
A1U25	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U26	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U27	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
A1U28	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U29	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
A1U30	1820-1130	0	1	IC GATE TTL S NAND 13-INP	01295	SN74S133N
A1U31	1810-0430	0		NETWORK-RES 10-SIP MULTI-VALUE	28480	1810-0430
A1X08	1200-0541	1	1	SOCKET-IC 24-CONT DIP DIP-SLDR	28480	1200-0541
A1XU16	1200-0639	8	11	SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU17	1200-0654	7	1	SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0654
A1XU18	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU19	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU20	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU21	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU22	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU25	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU26	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU27	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU28	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1XU29	1200-0639	8		SOCKET-IC 20-CONT DIP DIP-SLDR	28480	1200-0639
A1Y1	0410-1298	1	1	CRYSTAL-4 MHZ	28480	0410-1298
	7120-8723	3		LABEL-WHITE DOT	28480	7120-8723
	7124-0266	1		LABEL-BLUE DOT	85480	QD25 TAPE B-810-BL
	7124-0269	4		LABEL-RED DOT	85480	QD25 TAPE B-810-RD
	7124-0270	7		LABEL-YELLOW DOT	85480	QD25 TAPE B-810-YL
A1	64213-66501	1		POD ASSEMBLY-EM 6802	28480	64213-66501
A2	64213-62102	0	1	BOARD ASSEMBLY-ACTIVE CRT	28480	64213-62102
A2A1	64213-66502	2	1	BOARD ASSEMBLY-GROUNDING	28480	64213-66502
A2A1J1	1251-5943	4	2	CONN-POST TYPE	28480	1251-5943
A2A1J2	1251-5943	4		CONN-POST TYPE	28480	1251-5943
A2A2	64213-66504	4	1	BOARD ASSEMBLY-ACTIVE CKT	28480	64213-66504
A2A2C1	0160-3647	7	2	CAPACITOR-FXD 22PF +/-5% 100VDC CER 0+/-30	28480	0160-3647
A2A2C2	0160-3647	7		CAPACITOR-FXD 22PF +/-5% 100VDC CER 0+/-30	28480	0160-3647
A2A2C3	0160-3470	2	2	CAPACITOR-FXD .01UF +80-20% 50VDC CEK	28480	0160-3470
A2A2C4	0160-3470	2		CAPACITOR-FXD .01UF +80-20% 50VDC CER	28480	0160-3470
A2A2C5	0650-3443	1	1	CAPACITOR-FXD .1UF +80-20% 50VDC CER	28480	0160-3443
A2A2J1	1251-7948	3	2	CONNECTOR-20PIN ROW	28480	1251-7948
A2A2J2	1251-7948	3		CONNECTOR-20PIN ROW	28480	1251-7948
A2A2J3	1251-7948	3		CONNECTOR-20PIN ROW	28480	1251-7948
A2A2P1-1	1251-7851	7	1	CONNECTOR-40 PIN HEADER	28480	1251-7851
A2A2P1-40 THROUGH	1200-0475	0	40	CONNECTOR-SGR CONTSKT .017-IN-BSC-SZ	28480	1200-0475

Table 6-4. 6802 Replaceable Parts (Cont'd)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A2A2R1	0698-3113	1	1	RESISTOR 100 5% .125W CC TC=-270/+540	01121	BB1015
A2A2R2	0698-5426	3	1	RESISTOR 10K 10% .125W CC TC=-350/+857	01121	BB1031
A2A2R3	0675-1021	8	1	RESISTOR 1K 10% .125W CC TC=-270/+540	01121	BB1021
A2A2R4	0698-5422	9	2	RESISTOR 5.6K 10% .125W CC TC=-350/+857	01121	BB5621
A2A2R5	0698-5422	9	1	RESISTOR 5.6K 10% .125W CC TC=-350/+857	01121	BB5621
A2A2R6	0698-7926	2	1	RESISTOR 470 10% .125W CC TC=-330/+800	01121	BB4711
A2A2U1	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
HW1	2200-0107	6		SCREW-MACH 4-40 .375-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
HW2	2200-0510	5	7	SCREW-MACH 4-40 .75-IN-LG 82 DEG	00000	ORDER BY DESCRIPTION
HW3	2200-0512	7	6	SCREW-MACH 4-40 .312-IN-LG R2 DEG	00000	ORDER BY DESCRIPTION
MP1	10230-62101	7	2	GRABBER ASSEMBLY	28480	10230-62101
MP2	1200-0682	1		SOCKET-IC 40-CONT DIP DIP-SLDR	28480	1200-0682
MP3	4040-1566	5	1	PIN-BASE PLUG	28480	4040-1566
MP4	4040-1574	5	1	CLIP-TOP	28480	4040-1574
MP5	4320-0095	7		CHANNEL-RUBBER	28480	4320-0095
MP6	64213-04102	8	1	COVER-BOTTOM 9.5 IN.	28480	64213-04102
MP7	64213-64101	3	1	COVER ASSEMBLY (TOP)	28480	64213-64101
MP8	64232-60201	9	2	ENDCAP ASSY	28480	64232-60201
MP9	7121-1780	0	1	LABEL-"Hewlett-Packard"	28480	7121-1780
MP10	7121-2105	5	1	LABEL-"6802"	28480	7121-2105
MP11	0403-0179	0	4	BUMPER PLASTIC	28480	0403-0179
MP12	4040-1907	8	11	HEAT SINK RUBBER	28480	4040-1907
W1	8120-3724	5	1	USER CABLE 1	28480	8120-3725
W2	8120-3722	3	1	USER CABLE 2	28480	8120-3723
W3	64232-61603	7	1	CABLE ASSEMBLY - 1	28480	64232-61603
W4	64232-61604	8	1	CABLE ASSEMBLY - 2	28480	64232-61604
W5	5061-1217	8	1	PROBE-LEAD ASSEMBLY	28480	5061-1217
W6	5061-1218	9	1	PROBE-LEAD ASSEMBLY	28480	5061-1218
W7	64242-61602	8	1	CABLE JUMPER 2 CNDTR	28480	64242-61602

Table 6-5. Manufacturers' Codes

Mfr No.	Manufacturer Name	Address	Zip Code
00000	ANY SATISFACTORY SUPPLIER		
01121	ALLEN-BRADLEY CO	MILWAUKEE WI	53204
01295	TEXAS INSTR INC SEMICOND CHPNT DIV	DALLAS TX	75222
03888	KDI PYROFILM CORP	WHIPPANY NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX AZ	85062
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD PA	16701
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO CA	94304
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS MA	01247
72136	ELECTRO MOTIVE CORP SUB IEC	WILLIMANTIC CT	06226
85480	BRADY W H CO	MILWAUKEE WI	53209

SECTION VII

MANUAL CHANGES

7-1. INTRODUCTION.

7-2. This section would normally contain information needed to change this manual for models with repair numbers prior to those shown on the title page. No backdating material is contained within this edition because the first repair numbers for these models are included.

SECTION VIII

SERVICE

8-1. INTRODUCTION.

8-2. This section contains reference information for servicing the Model 64212A and Model 64213A Emulators. Theory of operation and block diagrams presented in this section include the Emulator Control Card. The component locators and schematics for the emulators are provided on foldout sheets for ease of use. The component locator and schematics for the Emulator Control Board are given in the Emulator Control Board manual. Table 8-1 lists the mnemonics used on the 6800 schematics. Table 8-2 lists mnemonics used on the 6802 schematics. Table 8-3 and table 8-4 explain the symbology used in the schematics.

8-3. SAFETY.

8-4. Read the safety summaries at the front of this manual and in the Mainframe service manual and the Service Overview manual prior to servicing this unit.

8-5. EMULATION SUBSYSTEM BLOCK DIAGRAMS.

8-6. Figure 8-1 provides the block diagram of a 6800 emulation subsystem. Figure 8-2 provides a block diagram of a 6802 emulation subsystem. Each emulation subsystem provides capabilities for hardware and software debugging, software development and real-time program execution. The emulation subsystem emulates a given microprocessor or family of microprocessors in a users target system.

8-7. DESCRIPTION.

8-8. EMULATOR POD. The emulator pod in each subsystem contains the microprocessor to be emulated. When not installed in the users target system, the pod may be used for software development. When the user plug is installed in the target systems microprocessor socket, target system operation can be evaluated. The 6800 Emulator Pod and the 6802 Emulator Pod block diagrams are very similar. The 6802 microprocessor contains an oscillator circuit which is emulated by adding an oscillator circuit to the user plug on the 6802 pod. In addition the 6802 pod contains a RAM to emulate the on-board memory of the 6802 microprocessor.

8-9. EMULATOR CONTROL BOARD. The Emulator Control Board provides the interface and control logic required between the pod, the optional memory and analysis cards, and the development system. The development system (Mainframe) controls the operation and monitors the status of the emulation subsystem through the mainframe bus interface to the control board.

8-10. INTERNAL ANALYSIS MODULE. The internal analysis module (Logic Analyzer) monitors the emulation bus for a specific state or combination of states to occur. When the required state(s) are detected, the Logic Analyzer stores the following states of the emulation bus. Software routines in the mainframe provide disassembly routines to convert the stored analysis data to equivalent instruction mnemonics for display on the development station CRT. Additional analysis modules may be added as shown.

8-11. EMULATION MEMORY CONTROLLER. The Emulation Memory Controller provides mapping and access control between the emulator and the optional Emulation Memory Boards. The mapping function is used to designate blocks of memory to function as ROM, RAM, user memory, or undefined memory. This allows software modifiable definitions for determining system requirements. The control function provides for in-circuit analysis, and breakpointing of the program being developed. This allows system operation to be observed and analyzed at near real-time operating speeds.

8-12. EMULATION MEMORY BOARDS. The Emulation Memory Boards contain banks of low-power RAM. These boards can be configured from 8k bytes on a single board, up to a maximum of 64k bytes on two boards.

8-13. EMULATOR POD BLOCK DIAGRAM.

8-14. Figure 8-3 is a combined block diagram of the emulator pods. Some circuits are contained on only the 6802 emulator pod and are noted as such.

8-15. DESCRIPTION.

8-16. EMULATION PROCESSOR. The Emulation Processor contained on the emulator pod board provides the nucleus for the emulation subsystem. The emulation processor may execute instructions stored in the target system memory or emulation memory, under control of the Emulator Control Board. The emulation processor is a high-speed model of the processor to be emulated.

8-17. EMULATION INTERNAL RAM. The emulation internal RAM for the 6802 emulator replaces the storage of the 6802 internal RAM. To allow maximum control of this feature, an external RAM is provided in the pod and the 6808 processor (which contains no internal RAM) is used. This is not a consideration for the 6800. Note that this block of the block diagram is noted as 6802 only.

8-18. EXTERNAL OSCILLATOR. The external oscillator circuit is used to emulate the on-board oscillator of the 6802. It is located in the user plug and will use a crystal from the target system to derive its operating frequency. If the target system uses a clock/driver, the external oscillator circuitry acts as a buffer. This active circuit in the user plug is another feature of the 6802 only.

8-19. PROCESSOR TIMING GENERATOR/SELECTOR. The processor timing generator/selector can be used as the source of processor timing when it is not desired to use the timing of the target system. In the 6800 emulator, a 1 MHz crystal oscillator is provided. In the 6802, a 4 MHz crystal is provided to set the operating frequency of the on-board oscillator. Selection of the internal clock or the target system timing is determined by the status of the INT/EXT line.

8-20. MICROPROCESSOR TIMING AND CONTROL. The microprocessor timing and control circuits provide control and coordination of the emulation processor for the development system host processor. The current mode of operation is selected through this interface and modifications to processor timing are implemented by these circuits. Components contained on the pod set time delays on the control card to ensure synchronization is maintained.

8-21. USER BUFFERS. To avoid loading the emulation processor control, data, and address lines and to provide for the control of emulator operation, buffers are provided between the emulation processor and the target system, and between the development system and the emulation processor. The User Interface buffers provide isolation and control of the control signals to and from the target system. The User Address buffers buffer the emulation processor address lines to the target system. Bidirectional buffering of the data lines to the target system is provided by the User Data buffers.

8-22. POD BUS BUFFERS. The Microprocessor Status and Control buffers provide isolation of the status and control lines from the microprocessor. The Emulator Control Board uses this information to monitor system activity, to check system operation, and to develop and maintain synchronization between the emulator pod and the mainframe processor. The Pod Data buffers provide the isolation and control of the interface between the control card and the emulation processor data lines. The Pod Address buffers isolate the emulation processor address lines from the control card.

8-23. BUFFER CONTROLS. The buffer controls provide control and coordination for the transfer of information between the control card and the emulator pod and between the target system and the pod. The buffer controls are developed from control and timing signals and selectively enable the needed buffers to support emulator operations.

8-24. EMULATOR CONTROL CARD BLOCK DIAGRAM.

8-25. The Emulator Control Card Block Diagram (figure 8-4) is provided here to assist in the understanding of the operation of the emulation subsystem. The component locator and schematics for this board are supplied in the Emulator Control Board Service Manual.

8-26. DESCRIPTION.

8-27. TIMING GENERATOR. The timing generator provides the timing for the emulator subsystem by coordinating the timing between the emulator and the development station host processor. All timing required to maintain synchronization is developed by the timing generator from the status and control lines from the pod bus. The timing generator controls timing to the emulation processor to ensure synchronization with the emulation bus for analysis and emulation memory references.

8-28. BACKGROUND MEMORY AND ACCESS CONTROL. The background memory and access control circuits consist of the Background Controller, the Jam Counter, the Background Memory and the Background Memory Access Controller. The development system controls the operation of the emulation processor by loading short programs into the background memory. The background memory controller directs the emulation processor to execute from background memory, or from user or emulation memory as directed by the mainframe processor. The background memory access controller ensures the host processor at least a 150 nsec access time slot immediately following each emulation processor memory cycle. During this time slot the mainframe processor may read data from, or write data to the background memory. When the mainframe processor wants to direct the emulation processor to change from one operation to another, the background controller directs the jam counter to force the address bus to contain a specific address of the background memory. A short program stored in this area of the background memory stores the important information from the emulation processor and provides control of the emulator to the mainframe processor.

8-29. Background Controller. The background controller is a four-state machine which controls the state of the emulation subsystem. Four states can be generated during the host processor access time; (1) Foreground, (2) Background-Jamming, (3) Background, and (4) Background-Exiting. In the Foreground state the emulation processor is executing from the user or emulation memory. In the Background-Jamming state the background controller disables the addresses generated by the emulation processor and impresses the addresses generated by the jam counter onto the address bus. The emulator will then enter and remain in the background state until the mainframe processor directs the emulation processor to fetch from a specified address in background memory. This causes the background controller to enter the background-exiting state. The location specified contains a jump to an address in the foreground memory. The emulation processor is again executing from user or emulation memory in the foreground state.

8-30. Jam Counter. The jam counter provides a series of addresses to the emulation processor address bus. These addresses contain the background-jamming data used to direct the emulation processor to store program and operational status in predetermined location and pass control to the mainframe processor.

8-31. Background Memory. The background memory consists of 256 RAM locations which are accessible by either the emulation processor or the mainframe processor. This dual accessibility allows the mainframe processor to load routines in the background memory which direct the emulation processor to provide status and address information for analysis.

8-32. Background Memory Access Controller. The background memory access controller uses control, timing, and status information derived from the timing generator and the pod bus interface to develop a 150 nsec time interval following every emulation processor memory reference. This time slot allows the mainframe processor to read data from, or write data to the background memory while the emulation processor is running.

8-33. CONTROL REGISTER. The control register is an eight bit register used as an addressable port. By setting and clearing the bits in this register, emulator functions can be enabled or disabled by the mainframe processor. Included in this register are bits for selecting the internal or external clock, resetting the emulation processor (DEFIB), suspending emulation processor operation by tri-stating it (LHOSTBRK), enabling the illegal opcode detector, and allowing asynchronous breaks under development system control.

8-34. ILLEGAL OPCODE DETECTOR. The illegal opcode detector is a ROM programmed to recognize all undefined opcodes. At the end of a fetch cycle the outputs of the ROM are latched into storage registers. A break condition results when an illegal opcode is detected causing the emulator to enter the background state. A bit in the control register controls the operation of the illegal opcode detector by controlling one of the ROM enables.

8-35. MISCELLANEOUS STATUS BUFFER. Eight bits of miscellaneous status are accessible through an addressable buffer. These eight bits contain the status information from the slow clock detector, the illegal opcode detector, and the background interrupt register, and control signals from the background memory and access controller.

8-36. LAST ADDRESS REGISTERS. Two last address registers are provided. One stores the last address before break and is clocked at the beginning of the memory cycle. The second stores the last opcode before break and is clocked at the end of each fetch cycle. When a break is caused by an illegal opcode both registers contain the same address. When the break is caused by a memory violation the two register contain different addresses. The address causing the the violation is in the last address register and the instruction causing the memory reference will be in the last opcode register.

8-37. MICROPROCESSOR PIN STATUS REGISTER. This 8-bit addressable register is used to store the status of selected emulation processor control pins. Data is latched into this register for each emulation clock cycle but is inhibited during background operations or while being read by the mainframe processor. This register is used to store the status of the tri-state control line (TSC), the HALT line, the interrupt request line (IRQ), the Non-Maskable Interrupt line (NMI), the internal RAM memory cycle control (LINHIB), the bus address valid pin (BA), and the RESET pin.

8-38. DATA BUFFER AND MULTIPLEXER. The data buffer and multiplexer is a bidirectional 8-bit to 16-bit multiplexer used to pack data from the emulator pod emulation data bus (ED0-7) into the emulation memory. The directional control signals cause the buffers to drive the internal emulation data bus (LED0-15) when the emulator is in the background state, if an access is made from user memory, or if a write operation is performed. At all other times the buffers drive the pod emulation data bus.

8-39. EMULATION BUS BUFFER. The emulation bus buffer is an 8-bit, bidirectional data buffer used for the 2nd emulation data bus (E2D0-7). This is a control bus used by the emulator for background memory and control functions. When not in the background mode the buffer is always driving the 2nd emulation bus unless the mainframe processor makes a reference, at which time the buffers will be tri-stated.

8-40. POD ADDRESS BUFFER. The pod address buffer is a tri-statable unidirectional buffer used to isolate the pod address bus (A0-15) from the control card buffered address bus (BA0-15). The emulation processor address is present on the buffered address bus at all times except during a JAM cycle or a mainframe processor access cycle. At these times the outputs of the pod address buffer are tri-stated.

8-41. HOST INTERFACE BUFFERS. Buffers are provided for the mainframe processor interface data and address lines. The host address buffer provides unidirectional buffering to the buffered address bus (BA0-15) during the mainframe access cycle time. At all other times the buffers are tri-stated. The host data buffer provides an eight bit bidirectional buffer from the mainframe data bus to the 2nd emulation data bus. The host data buffer is enabled during the host access cycle to read data from or write data to the background memory. At all other times the buffer is tri-stated.

8-42. READY MAPPER. The ready mapper is a RAM used to allow the use of low speed memory with high speed processors. This circuit is not used with the 6800/6802.

8-43. MNEMONICS.

8-44. Table 8-1 provides a list of the mnemonics used in the 6800 pod schematics. The table is organized with the target system interface first followed by the pod bus interface, followed by the inter-schematic mnemonics. Table 8-2 provides the same information but for the 6802 pod. The tables also list the source pin, the pages of the schematic on which the mnemonic appears, and a brief description of the signal including the active level.

8-45. LOGIC SYMBOLS.

8-46. Table 8-3 introduces the techniques used in the development of the logic symbols used in the schematics. Table 8-4 explains other symbols used on the schematics.

Table 8-1. 6800 Mnemonics

Mnemonic	Definition	Used On Sheets	Source
TARGET SYSTEM INTERFACE MNEMONICS			
ERESET	Emulator Reset. A level sensitive, low active input from the target system used to reset the emulation processor. When the time constraints listed in the 6800 specifications are observed this input can also function as a power up reset. Also an inter-schematic mnemonic.	1,2	Sheet 1 J1-2
UA0-15	User Address 0-15. Buffered address bus from the emulation processor to the target system.	1	Sheet 1 U7,U10
UBA	User Bus Available. Output signal to the target system, goes high when the user address bus is available to the target system. Normally low indicating the emulation processor is driving the bus.	1	Sheet 1 U21-3
UD0-7	User Data 0-7. Bidirectional buffered data bus between the emulation processor and the target system.	1	Sheet 1 U1
UDBE	User Data Bus Enable. Target system tri-state control for the emulation processor data bus lines. Enables outputs when held high. Also used as an inter-schematic mnemonic.	1,2	Sheet 2 U25-11
UHALT	User Halt. Input from target system which goes low to halt all activity in the emulation processor. Held high for normal operation. Also an inter-schematic mnemonic.	1,2	Sheet 1 J2-3
UIRQ	User Interrupt Request. Input from target system which goes low to request an interrupt of the emulation processor. This request is honored only after the current instruction cycle is completed, and only if the interrupt mask bit is cleared. Also an inter-schematic mnemonic.	1,2	Sheet 1 J2-7
UNMI	User Non-Maskable Interrupt. This is an edge sensitive input from the target system which goes low to request an interrupt of the emulation processor. This request will be honored immediately following the current instruction cycle. Also an inter-schematic mnemonic.	1,2	Sheet 1 J2-11

Table 8-1. 6800 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
U ϕ 1, U ϕ 2	User Clock Phase 1, Phase 2. Input lines from the target system for a two phase clock to set the processor operating speed. Also an inter-schematic mnemonic.	1,2	Sheet 1 J2-5 J1-8
UR/W	User Read/Low Write. Output to target system which defines the emulation processor operational state. When high the emulation processor is in a read state, when low the emulation processor is in a write state.	1	Sheet 1 U11-3
USER +5	User +5. This input from the V _{CC} pin of the target system microprocessor socket signals the emulator pod that the user plug is connected to a target system which is operating. Used to enable in-circuit emulation functions.	1	Sheet 1 J2-15
UTSC	User Three State Control. Input from the target system, goes high to stop the emulation processor for short periods of time. Low for normal operation. Also an inter-schematic mnemonic.	1,2	Sheet 1 J1-4
UVMA	User Valid Memory Address. Output to target system which goes high to indicate a valid address is present on the bus.	1	Sheet 1 U16-3
POD BUS INTERFACE MNEMONICS			
A0-15	Emulator Address 0-15. Buffered emulation processor address bus.	1	Sheet 1 U13,U15
BA	Bus Available. Buffered HBA from emulation processor. Goes high to indicate the address bus is available as during a processor halt or a wait state.	2	Sheet 2 U8-7
DELAY1	Delay 1. To allow for different delays for different processors used with the control board, the passive components for the single shot used to set the delay for strobing data onto the analysis bus are located in the Emulator Pod. Delay 1 sets a 227 nsec delay for one clock phase.	2	Sheet 2 J3-38
DELAY2	Delay 2. Sets a 206 nsec a delay for another clock phase.	2	Sheet 2 J3-42

Table 8-1. 6800 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
ED0-7	Emulation Data 0-7. Eight bit wide bidirectional emulation data bus from U5 and U8.	1	Sheet 1 U5,U8
EFG	Emulator Foreground. Goes high whenever a reference is made to memory addresses mapped as foreground memory. Also an inter-schematic mnemonic.	1,2	Sheet 2 J3-1
EINT/EXT	Emulator Internal/External Clock. Clock select signal sent to the pod from the mainframe processor through the control register to operate K1. When high the internal oscillator in the pod is enabled, when low the target system clock is used. Also an inter-schematic mnemonic.	1,2	Sheet 2 J3-11
ELBKG	Emulator Low Background. Goes low when the background controller enters the background state.	2	Sheet 2 J3-49
ELREFREQ	Emulator Low Refresh Request. Not used with current memory and analysis boards. When used, would provide for stopping the emulator processor for an emulation memory refresh cycle. Held high.	2	Sheet 2 J3-43
ELUSER	Emulator Low User. Buffer control signal to emulator. Goes low when address on emulator address bus is mapped to user memory space.	1	Sheet 1 J4-49
E Φ 1	Phase 1. Buffered Phase 1 of the emulation processor clock.	2	Sheet 2 J3-29
E Φ 2	Phase 2. Buffered Phase 2 of the emulation processor clock.	2	Sheet 2 J3-31
EPFG	Emulator Pre-Foreground. Goes high to indicate the background controller is going to change from background to foreground mode.	2	Sheet 2 J3-3
ETSC	Emulator Three-State Control. A microprocessor pin status bit from the emulator pod.	2	Sheet 2 U8-9

Table 8-1. 6800 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
ID0, ID1	Identification Bits 0,1. Used to to detect what emulator pod is being used. For both the 6800 and the 6802 ID0 is held high and ID1 is grounded.	2	Sheet 2 J3-47 J3-45
LEHALT	Low Emulation Halt. Goes low to request an emulator processor halt.	2	Sheet 2 J3-9
LDEFIB	Low Defibrillation. Goes low when the mainframe processor resets the emulation processor in the pod.	2	Sheet 2 J3-7
LHALT	Low Halt. A microprocessor pin status register bit. From pod emulator processor HALT pin.	2	Sheet 2 U8-16
LIACK	Low Interrupt Acknowledge. Not used. Not connected in 6800/6802 pods.	2	Sheet 2 J3-41
LIC	Last Instruction Cycle. Not used. Grounded in 6800/6802 pods.	2	Sheet 2 J3-37
LINHIB	Low Inhibit. Not used for 6800. Held high in the 6800 pod.	2	Sheet 2 J3-23
LIRQ	Low Interrupt Request. A processor status bit from the 6800 pod to the microprocessor pin status register to indicate a pending interrupt.	2	Sheet 2 U26-5
LNMI	Low Non-Maskable Interrupt. This is a microprocessor status bit which goes low to indicate the emulation processor is handling a nonmaskable interrupt.	2	Sheet 2 U26-3
LRESET	Low Reset. Buffered emulation reset line. Goes low whenever a reset is is applied to the emulation processor.	2	Sheet 2 U8-12
R/W	Read/Low Write. The emulation processor sets this line high for read operations and low for write operations.	2	Sheet 2 U14-2

Table 8-1. 6800 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
SYNC	Synchronize. Unused input from pod. Grounded in 6800 and 6802.	2	Sheet 2 J3-35
VMA	Valid Memory Address. Modified HVMA from the emulator processor. Goes high to indicate a valid memory address is present on the address bus (A0-15).	2	Sheet 2 U14-5
INTER-SCHEMATIC MNEMONICS			
B Φ 1, B Φ 2	Buffered Clock Phase 1, Phase 2. The two phase processor clock signal from the emulation processor. Phase 1 is buffered, Phase 2 is buffered and delayed.	1,2	Sheet 1 U26-7 U8-18
DBE	Data Bus Enable. Level sensitive input to enable the emulation processor data bus. The bus drivers in the emulation processor are enabled when this input high and tri-stated when this input is low.	1,2	Sheet 2 U25-11
D0-7	Data 0-7. Eight bit bidirectional emulation processor data bus.	1,2	Sheet 2 U3
EFG	Emulator Foreground. Goes high whenever a reference is made to memory addresses mapped as foreground memory. Also a Pod Bus Interface mnemonic.	1,2	Sheet 2 J3-1
EN	Enable. This line goes high when a foreground reference is made during in-circuit emulation. Enables the target system interface buffers for data, address and control.	1,2	Sheet 2 U20-3
ERESET	Emulator Reset. A level sensitive, low active input from the target system used to reset the emulation processor. When the time constraints listed in the 6800 specifications are observed this input can also function as a power up reset. Also a Target System Interface mnemonic.	1,2	Sheet 1 J1-2
HBA	High Bus Available. Output from the emulation processor. Low during normal operation, goes high during a HALT or WAIT state to signal the address bus is available for use by an external device.	1,2	Sheet 2 U3-7

Table 8-1. 6800 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
HVMA	High Valid Memory Address. An output from the emulation processor which goes high to indicate the address currently on the address bus is valid.	1,2	Sheet 2 U3-5
HALT	Halt. A low level is asserted here to halt the emulation processor. High for normal operation.	1,2	Sheet 2 U12-8
ICE	In-Circuit Emulation. Goes high when the user plug is installed in the microprocessor socket of the target system and power is present on the V _{CC} pin of the socket. Signals the pod that in-circuit emulation is now possible.	1,2	Sheet 1 U11-14
PA0-15	Processor Address 0-15. The 16 bit address bus from the emulation processor.	1,2	Sheet 2 U3
PEN	Prime Enable. Enables the UVMA signal and used as part of the selection of the data bus buffer to the target system.	1,2	Sheet 2 U25-6
Φ1, Φ2	Clock Phase 1, Phase 2. Output of clock selector relay to the emulation processor which sets the processor operating speed.	1,2	Sheet 2 K1-2 K1-7
PR/W	Processor Read/Low Write. Output from the emulation processor used to signal which operation is to be performed. When high the processor is in the Read state, when low the processor is in the Write state.	1,2	Sheet 2 U3-34
RESET	Reset. Goes low to reset the emulation processor, reinitializes the processor when it is running. Careful attention to timing constraints allow this line to be used as a power up reset.	1,2	Sheet 2 U20-8
TSC	Three State Control. Low for normal operation, goes high to insert short delays in the operation of the emulation processor.	1,2	Sheet 2 U21-6
UDBE	User Data Bus Enable. Target system tri-state control for the emulation processor data bus lines. Enables outputs when held high. Also used as a Target System Interface mnemonic.	1,2	Sheet 1 J1-10

Table 8-1. 6800 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
U Φ 1, U Φ 2	User Clock Phase 1, Phase 2. Input lines from the target system for a two phase clock to set the processor operating speed. Also a Target System Interface mnemonic.	1,2	Sheet 1 J2-5 J1-8
UTSC	User Three State Control. Input from the target system, goes high to stop the emulation processor for short periods of time. Low for normal operation. Also a target System Interface mnemonic.	1,2	Sheet 1 J1-4

Table 8-2. 6802 Mnemonics

Mnemonic	Definition	Used On Sheets	Source
TARGET SYSTEM INTERFACE MNEMONICS			
BEXTAL	Buffered External Crystal. This input from the oscillator/buffer circuit in user plug is the active input pin for the emulation processor when the external source is selected. Also an inter-schematic mnemonic.	1,2	Sheet 1 J1-4
BXTAL	Buffered Xtal. When external source is selected, this is the common side of the oscillator output from the oscillator/buffer circuit in the user plug. Also an inter-schematic mnemonic.	1,2	Sheet 1 J1-6
ERESET	Emulator Reset. A level sensitive, low active input from the target system used to reset the emulation processor. Also an inter-schematic mnemonic.	1,2	Sheet 1 J4-2
INT VECT	Interrupt Vector. Special line to assist in using the input/output expander options available in the 6800 series family.	2	Sheet 2 J5-1
UA0-15	User Address 0-15. Buffered address bus from the emulation processor to the target system.	1	Sheet 1 U10, U11
UBA	User Bus Available. Output signal to the target system, goes high when the user address bus is available to the target system. Normally low indicating the emulation processor is driving the bus.	1	Sheet 1 U7-12
UD0-7	User Data 0-7. Bidirectional buffered data bus between the emulation processor and the target system.	1	Sheet 1 U9
UE	User Enable. A buffered output to the target system of the emulation processor clock. Clock frequency is equal to the oscillator frequency divided by 4.	1	Sheet 1 U7-16
UHALT	User Halt. Input from target system which goes low to halt all activity in the emulation processor. Held high for normal operation. Also an inter-schematic mnemonic.	1,2	Sheet 1 J2-3

Table 8-2. 6802 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
UIRQ	User Interrupt Request. Input from target system which goes low to request an interrupt of the emulation processor. This request is honored only after the current instruction cycle is completed, and only if the interrupt mask bit is cleared. Also an inter-schematic mnemonic.	1,2	Sheet 1 J2-7
UMR	User Memory Ready. Held high for normal operation. Used to allow operation with slow memories. When taken low, emulation processor timing is modified. Also an inter-schematic mnemonic.	1,2	Sheet 1 J2-5
UNMI	User Non-Maskable Interrupt. This is an edge sensitive input from the target system which goes low to request an interrupt of the emulation processor. This request will be honored immediately following the current instruction cycle. Also an inter-schematic mnemonic.	1,2	Sheet 1 J2-11
URE	User RAM Enable. Input to the pod from the target system. When high the internal RAM emulation memory is enabled. When low the internal RAM emulation memory is disabled. Also a inter-schematic mnemonic.	1,2	Sheet 1 J1-10
UR/W	User Read/Low Write. Output to target system which defines the emulation processor operational state. When high the emulation processor is in a Read state, when low the Emulation processor is in a Write state.	1	Sheet 1 U6-3
USER +5	User +5. This input from the V _{CC} pin of the target system microprocessor socket signals the emulator pod that the user plug is connected to a target system which is operating. Used to enable in-circuit emulation functions.	1	Sheet 1 J2-15
UVMA	User Valid Memory Address. Output to target system which goes high to indicate a valid address is currently on the bus.	1	Sheet 1 U5-6
WROM	Write to ROM. A special line used used to overlay data to an area of user memory mapped as ROM.	2	Sheet 2 J5-2

Table 8-2. 6802 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
POD BUS INTERFACE MNEMONICS			
A0-15	Emulator Address 0-15. Buffered emulation processor address bus from U15, U13.	1	Sheet 1 U19, U21
BA	Bus Available. From the emulation processor. Goes high to indicate the address bus is available as during a processor halt or a wait state.	2	Sheet 2 U26-15
DELAY1	Delay 1. To allow for different delays for different processors used with the control board, the passive components for the single shot used to set the delay for strobing data onto the analysis bus are located in the Emulator Pod. Delay 1 sets a 227 nsec delay for one clock phase.	2	Sheet 2 J4-38
DELAY2	Delay 2. Sets a 206 nsec a delay for another clock phase.	2	Sheet 2 J4-42
ED0-7	Emulation Data 0-7. Eight bit wide bidirectional emulation data bus from U5 and U8.	1	Sheet 1 U28, U29
EFG	Emulator Foreground. Goes high whenever a reference is made to memory addresses mapped as foreground memory. Also an inter-schematic mnemonic.	1,2	Sheet 2 J4-1
EINT/EXT	Emulator Internal/External Clock. Clock select signal sent to the pod from the mainframe processor through the control register to operate K1 and K2. When high the internal oscillator in the pod is enabled, when low the target system clock is used.	2	Sheet 2 J4-11
ELBKG	Emulator Low Background. Goes low when the background controller enters the background state.	2	Sheet 2 J4-49
EReady	Emulation Ready. Used by the control card to insert wait states in the emulation processor. Goes low to initiate a MR delay in the emulation processor.	2	Sheet 2 J4-5

Table 8-2. 6802 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
ELREFREQ	Emulator Low Refresh Request. Not used with current memory and analysis boards. When used, would provide for stopping the emulator processor for an emulation memory refresh cycle. Held high.	2	Sheet 2 J4-43
ELUSER	Emulator Low User. Buffer control signal to emulator. Goes low when address on emulator address bus is mapped to user memory space.	1	Sheet 1 J3-49
E ϕ 1	Phase 1. Buffered, inverted clock from the emulation processor.	2	Sheet 2 U16-9
E ϕ 2	Phase 2. Buffered non-inverted emulator processor clock.	2	Sheet 2 U26-12
EPFG	Emulator Pre-Foreground. Goes high to indicate the background controller is going to change from background to foreground mode.	2	Sheet 2 J4-3
ETSC	Emulator Three-State Control. Not used in 6802. Grounded in the emulator pod.	2	Sheet 2 J4-15
ID0, ID1	Identification Bits 0,1. Used to detect what emulator pod is being used. For both the 6800 and the 6802 ID0 is held high and ID1 is grounded.	2	Sheet 2 J4-45 J3-45
LEHALT	Low Emulation Halt. Goes low to request an emulator processor halt.	2	Sheet 2 J4-9
LDEFIB	Low Defibrillation. Goes low when the mainframe processor resets the emulation processor in the pod.	2	Sheet 2 J4-7
LHALT	Low Halt. A microprocessor pin status register bit. Buffered emulator processor HALT pin.	2	Sheet 2 U26-9
LIACK	Low Interrupt Acknowledge. Not used. Not connected in 6800/6802 pods.	2	Sheet 2 J4-41

Table 8-2. 6802 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
LIC	Last Instruction Cycle. Not used. Grounded in 6800/6802 pods.	2	Sheet 2 J4-37
LINHIB	Low Inhibit. A low on this line inhibits emulation memory cycles independently of the memory mapper. Used by the 6802 to overlay 6802 internal RAM and to optionally allow user writes to ROM without generating a memory break. Held high in the 6800 pod.	2	Sheet 2 U26-18
LRESET	Low Reset. Buffered emulation reset line. Goes low whenever a reset is applied to the emulation processor.	2	Sheet 2 U26-14
EMR	Emulator Memory Ready. Output to control card micro-processor pin status register. Provides a buffered MR status monitor line.	2	Sheet 2 U25-18
R/W	Read/Low Write. The emulation processor holds this line high for read operations and low for write operations.	2	Sheet 2 U27-19
SYNC	Synchronize. Unused input from pod. Grounded in 6800 and 6802.	2	Sheet 2 J4-37
VMA	Valid Memory Address. Modified HVMA from the emulator processor. Goes high to indicate a valid memory address is present on the address bus (A0-15).	2	Sheet 2 U14-16
INTER-SCHEMATIC MNEMONICS			
BE	Buffered Emulator Clock. Buffered E clock signal from the emulation processor.	1,2	Sheet 1 U26-7
BEXTAL	Buffered External Crystal. This input from the oscillator/buffer circuit in user plug is the active input pin for the emulation processor when the external source is selected. Also an Target System Interface mnemonic.	1,2	Sheet 1 J1-4

Table 8-2. 6802 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
BR/W	Buffered Read/Low Write. Buffered PR/W from the emulation processor. High when the emulation processor is in the read state, low when the emulation processor is in the write state.	1,2	Sheet 1 U26-3
BXTAL	Buffered Xtal. When external source is selected, this is the common side of the oscillator output from the oscillator/buffer circuit in the user plug. Also a Target System Interface mnemonic.	1,2	Sheet 1 J1-6
DE	Delayed Emulator Clock. Delayed emulation processor E clock.	1,2	Sheet 1 U16-18
D0-7	Data 0-7. Bidirectional 8-bit data bus from the emulation processor.	1,2	Sheet 2 U17
E	External Processor Clock. The output of the internal clock of the emulation processor. Clock frequency equals oscillator frequency divided by four.	1,2	Sheet 2 U17-37
EFG	Emulator Foreground. Goes high whenever a reference is made to memory addresses mapped as foreground memory. Also an Pod Bus Interface mnemonic.	1,2	Sheet 2 J4-1
EN	Enable. This line goes high when a foreground reference is made during in-circuit emulation. Enables the target system interface buffers for data, address and control.	1,2	Sheet 2 U22-18
ERESET	Emulator Reset. A level sensitive, low active input from the target system used to reset the emulation processor. Also a Target System Interface mnemonic.	1,2	Sheet 1 J1-2
HBA	High Bus Available. Output of the emulation processor, low for normal operation, goes high to indicate the address bus is available for use by an external device. Occurs during a halt or a wait state.	1,2	Sheet 2 U17-7

Table 8-2. 6802 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
HVMA	High Valid Memory Address. Output of the emulation processor. Goes high to indicate the presence of a valid memory address on the bus.	1,2	Sheet 2 U17-5
LINTRAM	Low Internal RAM. Goes low to indicate a reference is being made to the internal RAM. Blocks the target system data bus for internal references.	1,2	Sheet 2 U30-9
ICE	In-Circuit Emulation. Developed from the V_{CC} of the micro-processor socket in the target system. Goes high to indicate to the pod that the user plug is inserted into a powered up target system.	1,2	Sheet 1 U5-11
PA0-15	Processor Address 0-15. The 16-bit address bus from the emulation processor.	1,2	Sheet 2 U17
PEN	Prime Enable. Enables the UVMA signal and used as part of the selection of the data bus buffer to the target system.	1,2	Sheet 2 U4-11
PR/W	Processor Read/Low Write. Output from the emulation processor used to signal which operation is to be performed. When high the processor is in the Read state, when low the processor is in the Write state.	1,2	Sheet 1 U17-34
UHALT	User Halt. Input from target system which goes low to halt all activity in the emulation processor. Held high for normal operation. Also a Target System Interface mnemonic.	1,2	Sheet 1 J2-3
UIRQ	User Interrupt Request. Input from target system which goes low to request an interrupt of the emulation processor. This request is honored only after the current instruction cycle is completed, and only if the interrupt mask bit is cleared. Also a Target System Interface mnemonic.	1,2	Sheet 1 J2-7
UMR	User Memory Ready. Held high for normal operation. Used to allow operation with slow memories. When taken low, emulation processor timing is modified. Also a Target System Interface mnemonic.	1,2	Sheet 1 J2-5

Table 8-2. 6802 Mnemonics (Cont'd)

Mnemonic	Definition	Used On Sheets	Source
UNMI	User Non-Maskable Interrupt. This is an edge sensitive input from the target system which goes low to request an interrupt of the emulation processor. This request will be honored immediately following the current instruction cycle. Also a Target System Interface mnemonic.	1,2	Sheet 1 J2-11
URE	User RAM Enable. Input to the pod from the target system. When high the internal RAM emulation memory is enabled. When low the internal RAM emulation memory is disabled. Also a Target System Interface mnemonic.	1,2	Sheet 1 J1-10

Table 8-3. Logic Symbols

GENERAL

All signals flow from left to right, relative to the symbol's orientation with inputs on the left side of the symbol, and outputs on the right side of the symbol (the symbol may be reversed if the dependency notation is a single term.)

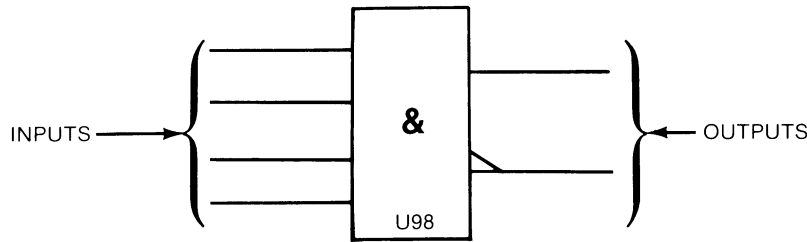
All dependency notation is read from left to right (relative to the symbol's orientation).

An external state is the state of an input or output outside the logic symbol.

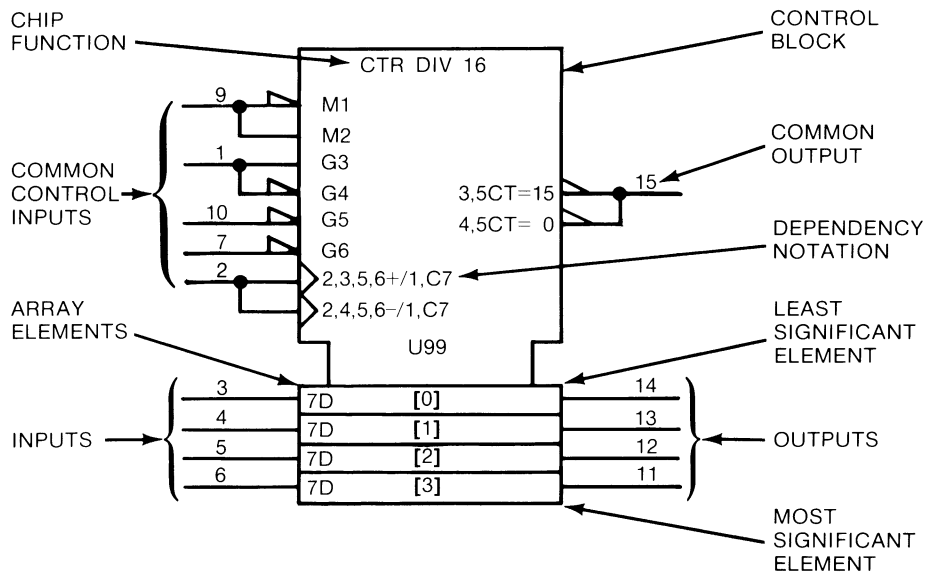
An internal state is the state of an input or output inside the logic symbol. All internal states are True = High.

SYMBOL CONSTRUCTION

Some symbols consist of an outline or combination of outlines together with one or more qualifying symbols, and the representation of input and output lines.



Some have a common Control Block with an array of elements:



CONTROL BLOCK - All inputs and dependency notation affect the array elements directly. Common outputs are located in the control block. (Control blocks may be above or below the array elements.)

ARRAY ELEMENTS -All array elements are controlled by the control block as a function of the dependency notation. Any array element is independent of all other array elements. Unless indicated, the least significant element is always closest to the control block. The array elements are arranged by binary weight. The weights are indicated by powers of 2 (shown in []).

Table 8-3. Logic Symbols (Cont'd)

INPUTS - Inputs are located on the left side of the symbol and are affected by their dependency notation.

Common control inputs are located in the control block and control the inputs/outputs to the array elements according to the dependency notation.

Inputs to the array elements are located with the corresponding array element with the least significant element closest to the control block.

OUTPUTS - Outputs are located on the right side of the symbol and are effected by their dependency notation.

Common control outputs are located in the control block.

Outputs of array elements are located in the corresponding array element with the least significant bit closest to the control block.

CHIP FUNCTION - The labels for chip functions are defined, i.e., CTR - counter, MUX - multiplexer.

DEPENDENCY NOTATION

Dependency notation is always read from left to right relative to the symbol's orientation.

Dependency notation indicates the relationship between inputs, outputs, or inputs and outputs. Signals having a common relationship will have a common number, i.e., C7 and 7D...C7 controls D. Dependency notation 2,3,5,6+/1,C7 is read as when 2 and 3 and 5 and 6 are true, the input will cause the counter to increment by one count....or (/) the input (C7) will control the loading of the input value (7D) into the D flip-flops.

The following types of dependencies are defined:

- a. AND (G), OR (V), and Negate (N) denote Boolean relationship between inputs and outputs in any combination.
- b. Interconnection (Z) indicates connections inside the symbol.
- c. Control (C) identifies a timing input or a clock input of a sequential element and indicates which inputs are controlled by it.
- d. Set (S) and Reset (R) specify the internal logic states (outputs) of an RS bistable element when the R or S input stands at its internal 1 state.
- e. Enable (EN) identifies an enable input and indicates which inputs and outputs are controlled by it (which outputs can be in their high impedance state).
- f. Mode (M) identifies an input that selects the mode of operation of an element and indicates the inputs and outputs depending on that mode.
- g. Address (A) identifies the address inputs.
- h. Transmission (X) identifies bi-directional inputs and outputs that are connected together when the transmission input is true.

DEPENDENCY NOTATION SYMBOLS

A	Address (selects inputs/outputs) (indicates binary range)	N	Negate (compliments state)
C	Control (permits action)	R	Reset Input
EN	Enable (permits action)	S	Set Input
G	AND (permits action)	V	OR (permits action)
M	Mode (selects action)	Z	Interconnection
		X	Transmission

Table 8-3. Logic Symbols (Cont'd)

OTHER SYMBOLS		
	Analog Signal	
	AND	
	Bit Grouping	
	Buffer	
	Compare	
	Dynamic	≥ 1 OR
$=1$	Exclusive OR	
	Hysteresis	
	Interrogation	
	Internal Connection	


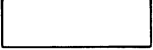










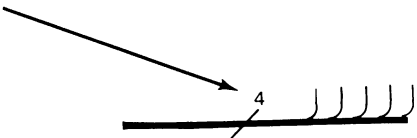
LABELS					
BG	Borrow Generate	CO	Carry Output	J	J Input
BI	Borrow Input	CP	Carry Propagate	K	K Input
BO	Borrow Output	CT	Content	P	Operand
BP	Borrow Propagate	D	Data Input	T	Transition
CG	Carry Generate	E	Extension (input or output)	+	Count Up
CI	Carry Input	F	Function	-	Count Down

MATH FUNCTIONS			
Σ	Adder	>	Greater Than
ALU	Arithmetic Logic Unit	<	Less Than
COMP	Comparator	CPG	Look Ahead Carry Generator
DIV	Divide By	π	Multiplier
=	Equal To	P-Q	Subtractor

CHIP FUNCTIONS			
BCD	Binary Coded Decimal	DIR	Directional
BIN	Binary	DMUX	Demultiplexer
BUF	Buffer	FF	Flip-Flop
CTR	Counter	MUX	Multiplexer
DEC	Decimal	OCT	Octal
		RAM	Random Access Memory
		RCVR	Line Receiver
		ROM	Read Only Memory
		SEG	Segment
		SRG	Shift Register

DELAY and MULTIVIBRATORS	
	Astable
	Delay
	Nonretriggerable Monostable
NV	Nonvolatile
	Retriggerable Monostable

Table 8-4. Schematic Symbols

	ETCHED CIRCUIT BOARD	(925)	WIRE COLORS ARE GIVEN BY NUMBERS IN PARENTHESES USING THE RESISTOR COLOR CODE
	FRONT PANEL MARKING		[(925) IS WHT-RED-GRN]
	REAR PANEL MARKING		0 - BLACK 5 - GREEN 1 - BROWN 6 - BLUE 2 - RED 7 - VIOLET 3 - ORANGE 8 - GRAY 4 - YELLOW 9 - WHITE
	MANUAL CONTROL		* OPTIMUM VALUE SELECTED AT FACTORY, TYPICAL VALUE SHOWN; PART MAY HAVE BEEN OMITTED.
	SCREWDRIVER ADJUSTMENT		
	ELECTRICAL TEST POINT TP (WITH NUMBER)		UNLESS OTHERWISE INDICATED: RESISTANCE IN OHMS CAPACITANCE IN PICO FARADS INDUCTANCE IN MICROHENRIES
	NUMBERED WAVEFORM NUMBER CORRESPONDS TO ELECTRICAL TEST POINT NO.	μP = MICROPROCESSOR	
	LETTERED TEST POINT NO MEASUREMENT AID PROVIDED	P/O = PART OF	
	COMMON CONNECTIONS. ALL LIKE-DESIGNATED POINTS ARE CONNECTED.	NC = NO CONNECTION	
	NUMBER ON WHITE BACKGROUND = OFF-PAGE CONNECTION. LARGE UMBER ADJACENT = SERVICE SHEET NUMBER FOR OFF-PAGE CONNECTION.	CW = CLOCKWISE END OF VARIABLE RESISTOR	
	CIRCLED LETTER = OFF-PAGE CONNECTION BETWEEN PAGES OF SAME SERVICE SHEET.		
	INDICATES SINGLE SIGNAL LINE		
	NUMBER OF LINES ON A BUS		

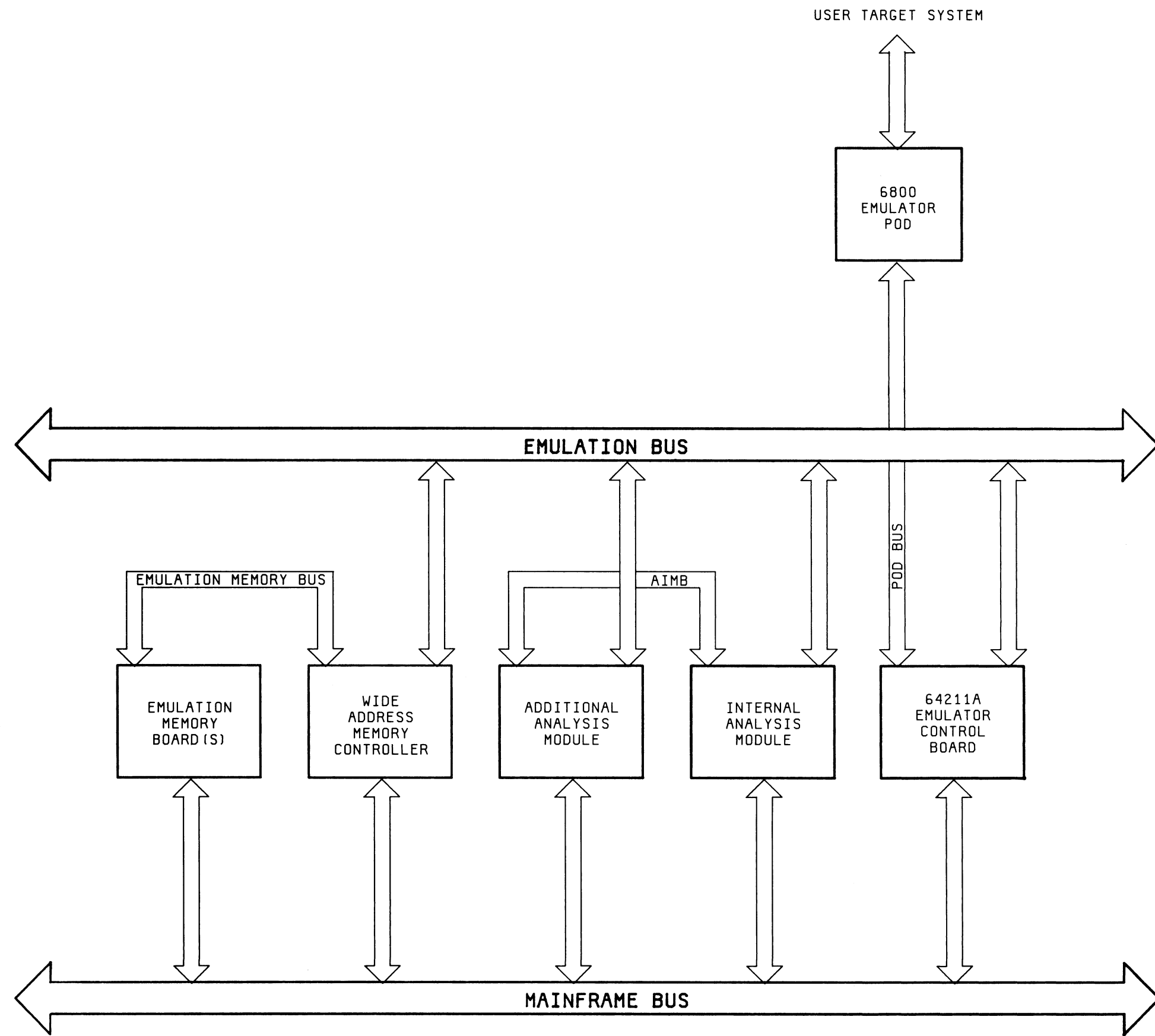


Figure 8-1. 6800 Emulation Subsystem Block Diagram

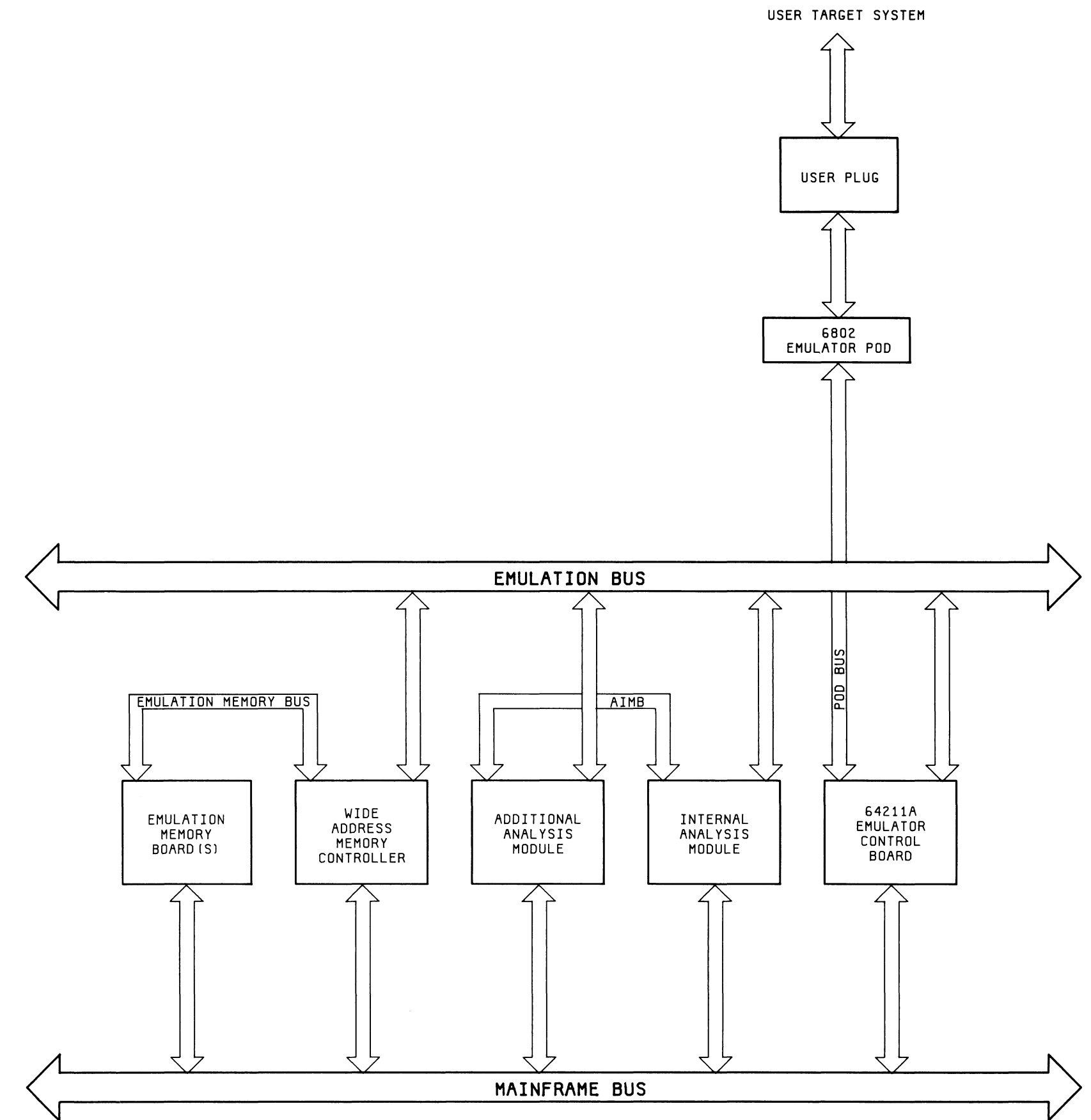


Figure 8-2. 6802 Emulation Subsystem Block Diagram
8-25

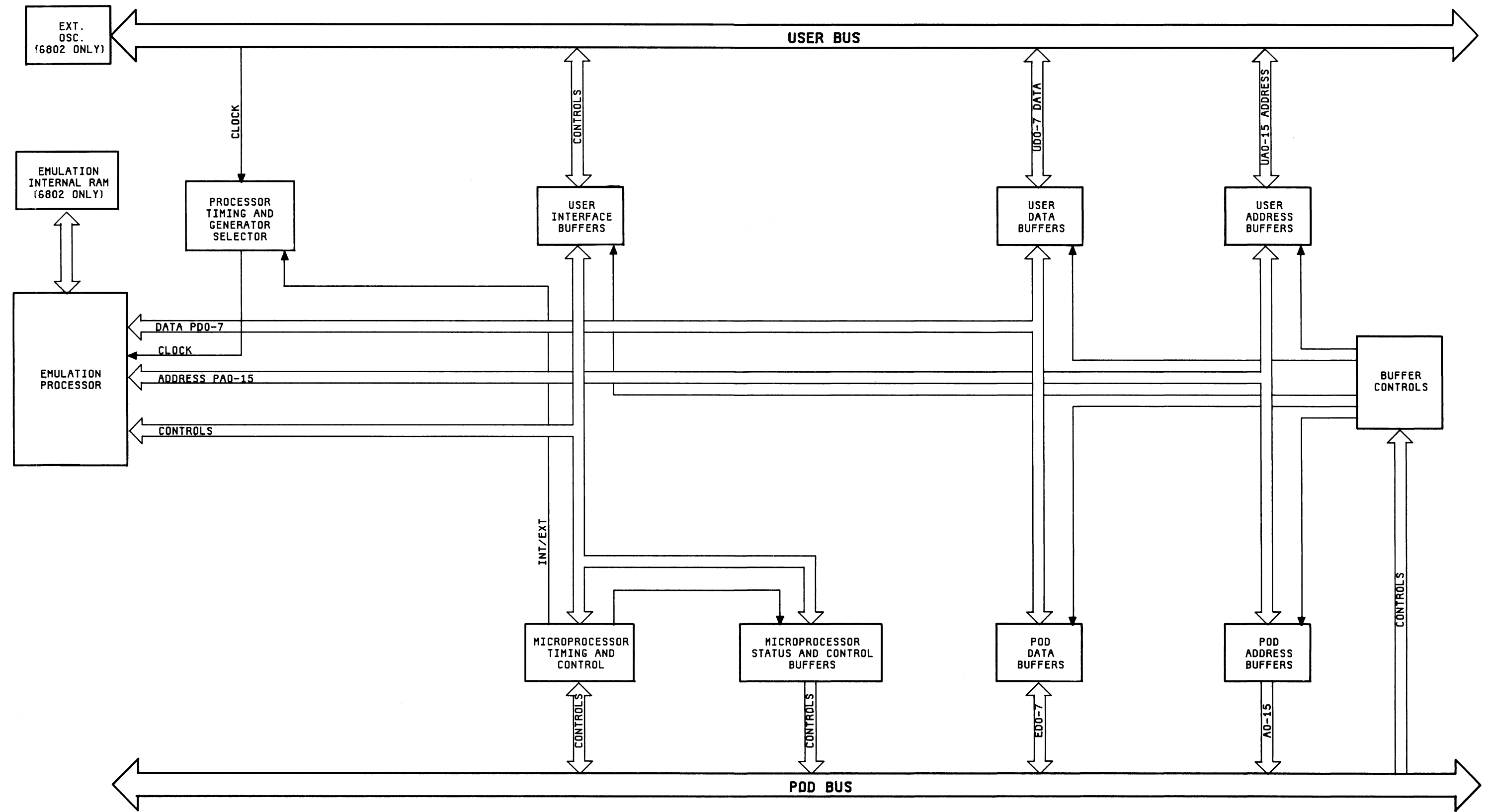


Figure 8-3. 6800/6802 Emulator Pod Block Diagram

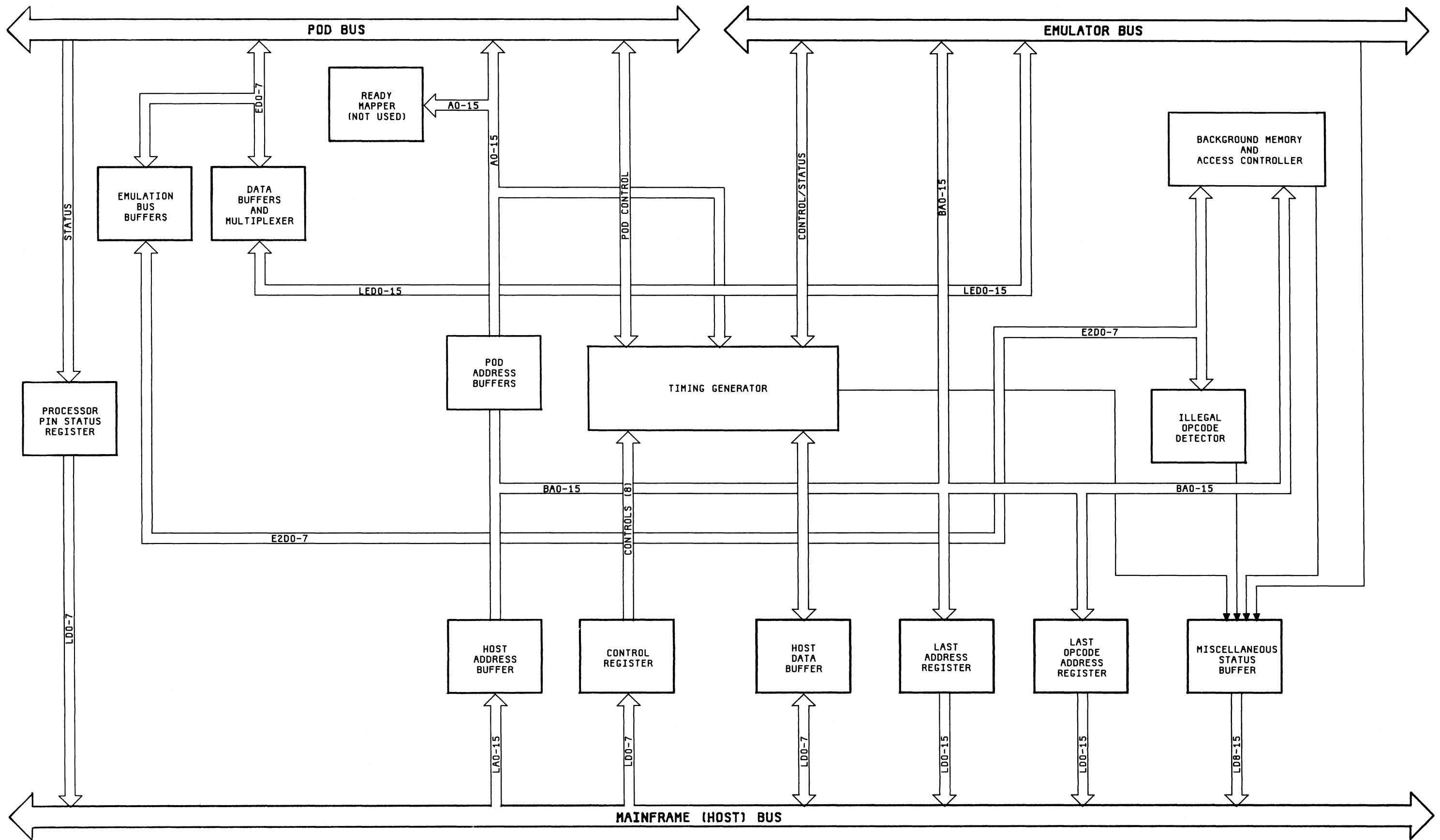


Figure 8-4.
64211A Emulator Control Card Block Diagram
8-27

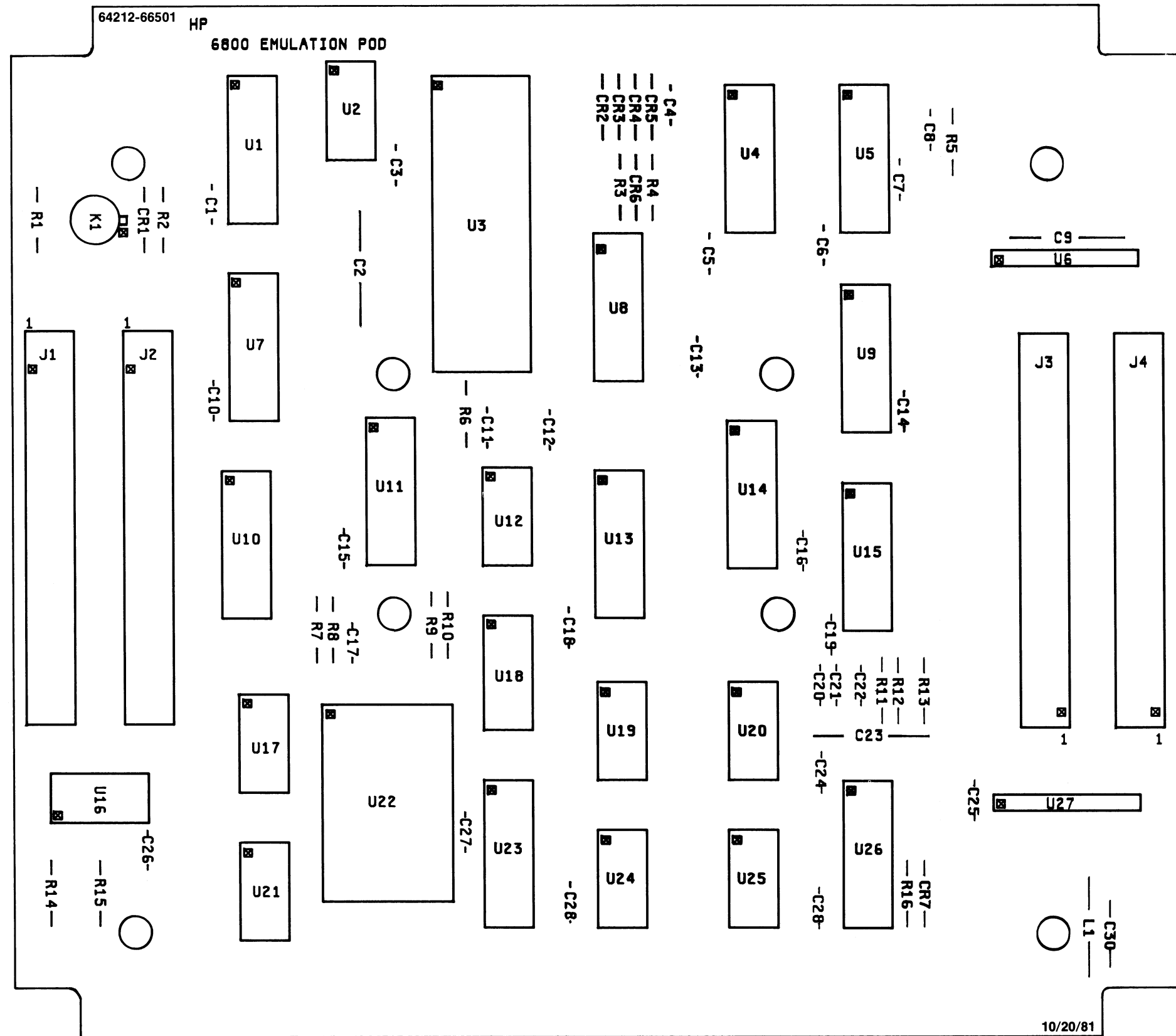
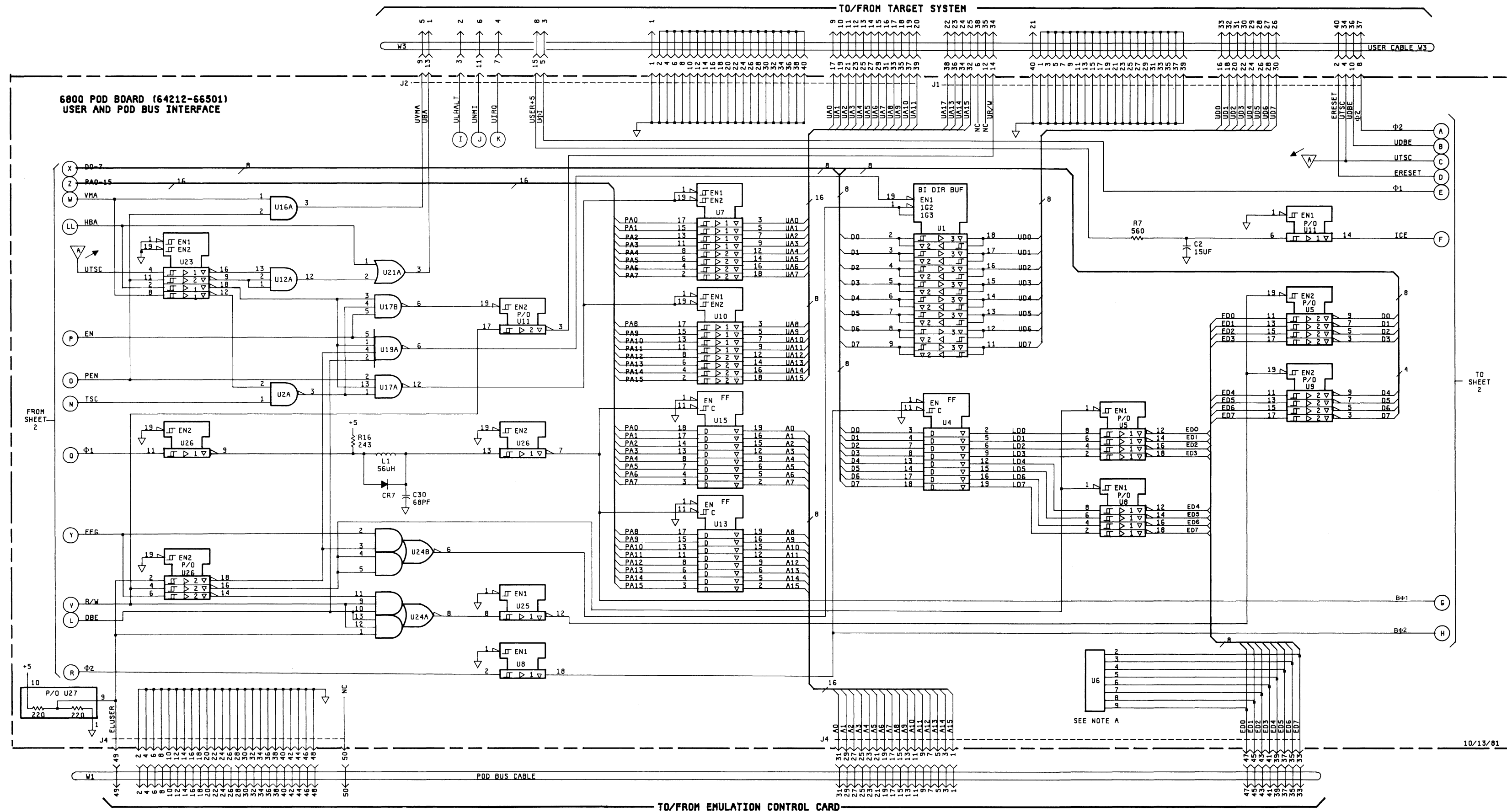


Figure 8-5. 64212A 6800 Emulator Pod, Component Locator

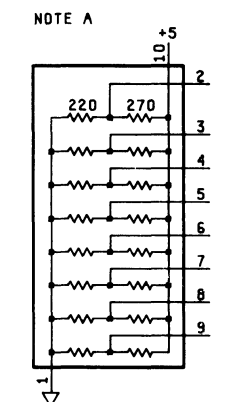


ICS ON THIS SCHEMATIC POWER PINS

REF. DES.	HP PART NO.	MFR. PART NO.	+5	GND
U1	1820-2075	74LS245	20	10
U2	1820-0681	74S00	14	7
U4, U13, U15	1820-1576	74S373	20	10
U5, U8, U9	1820-1624	74S241	20	10
U7, U10, U11	1820-2024	74LS244	20	10
U12	1820-0686	74S11	14	7
U16	1820-1201	74LS08	14	7
U17	1820-0685	74S10	14	7
U19	1820-0688	74S20	14	7
U21	1820-1208	74LS32	14	7
U23, U26	1820-1633	74S240	20	10
U25	1820-1449	74S32	14	7

PARTS ON THIS SCHEMATIC

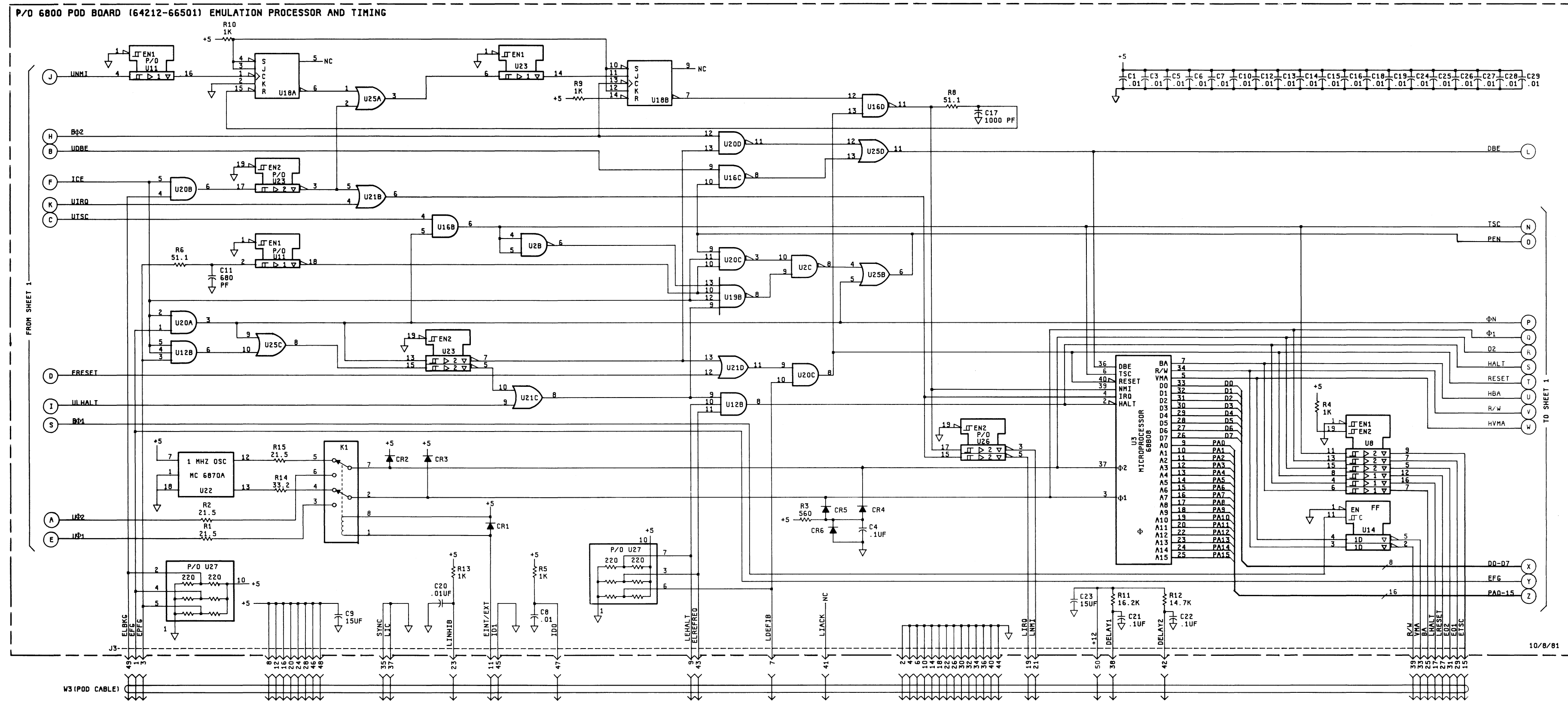
C2, C80
 L1
 R7, R16
 U1, U2, U4, U5, U6, U7, U8, U9, U10, U11
 U12, U13, U15, U16, U17, U19, U21, U23
 U25, U26, U27



10/13/81

1

Figure 8-6.
 6800 Emulator Pod, Service Sheet 1
 8-29/(8-30 blank)



ICS ON THIS SCHEMATIC

REF.	DES.	HP PART NO.	MFR. PART NO.	+5	GND
U2		1820-0681	74S00	14	7
U3		1820-1624	74S241	20	10
U8		1820-2024	74LS244	20	10
U11,12		1820-0686	74S11	14	7
U14		1820-1576	74S373	20	10
U16		1820-2358	MC68800	8	1,21
U18		1820-0629	74S112	16	8
U19		1820-0688	74S20	14	7
U20		1820-1367	74S08	14	7
U21		1820-1208	74LS32	14	7
U22		1820-1637	MC6870A	7	1,18
U23, U26		1820-1633	74S240	20	10
U25		1820-1449	74S32	14	7

PARTS ON THIS SCHEMATIC

C1, C3-C29
 K1
 R1-R6, R8-R15
 U2, U3, U8, U11, U12, U14, U16, U18
 U19, U20, U21, U22, U23, U25, U26, U27

10/8/81

2

Figure 8-7.
 6800 Emulator Pod, Service Sheet 2
 8-31

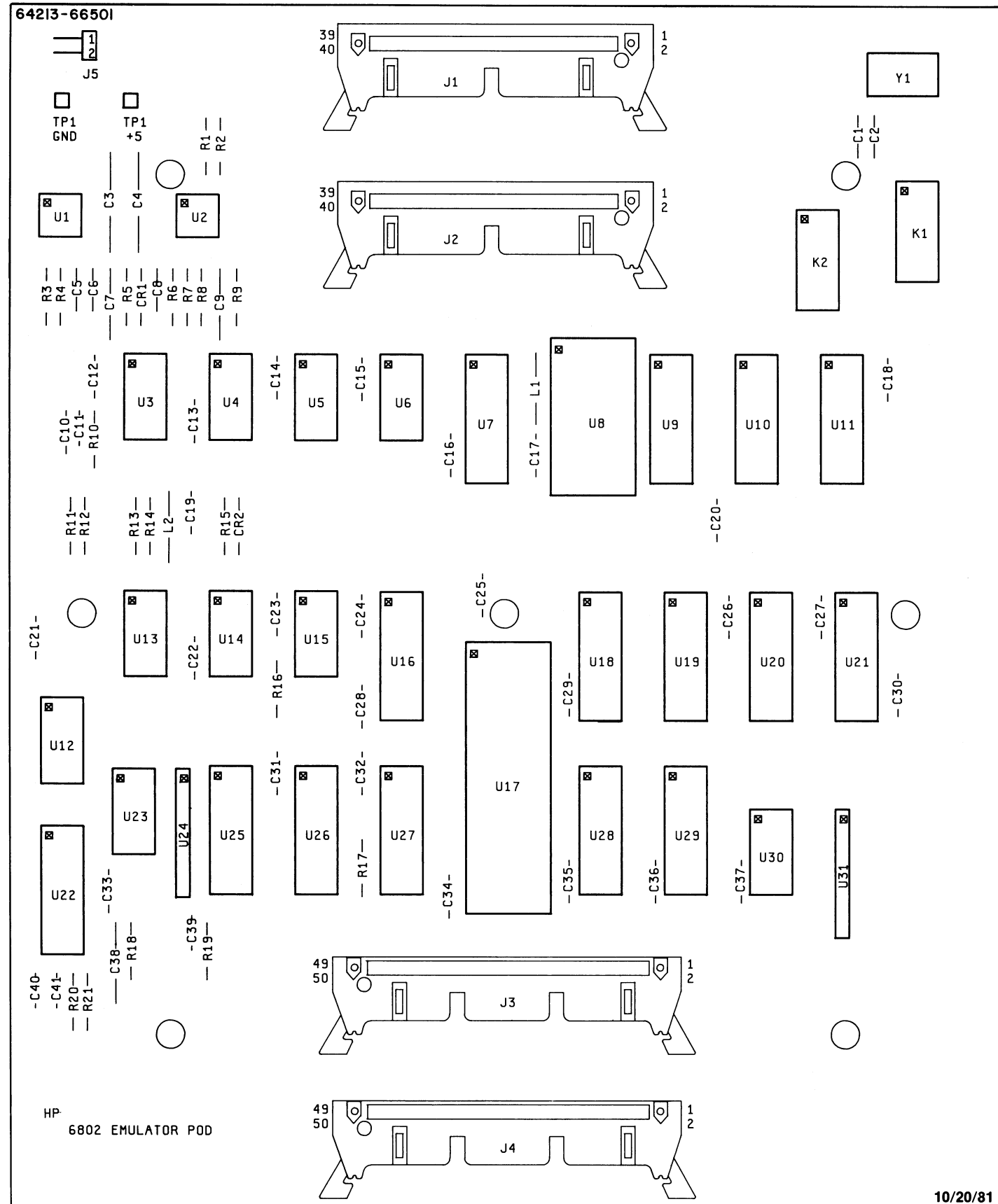


Figure 8-8. 64213A 6802 Emulator Pod, Component Locator

LOCATED UNDER FOLD



Figure 8-8. 64213A 6802 Emulator Pod, Component Locator

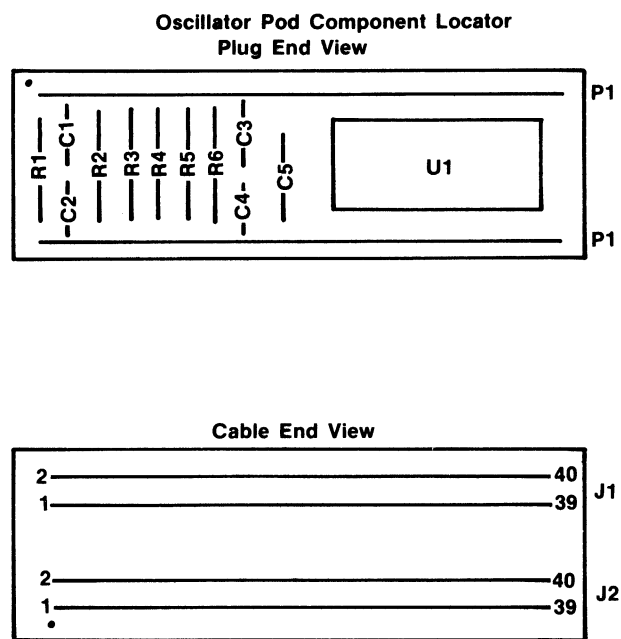
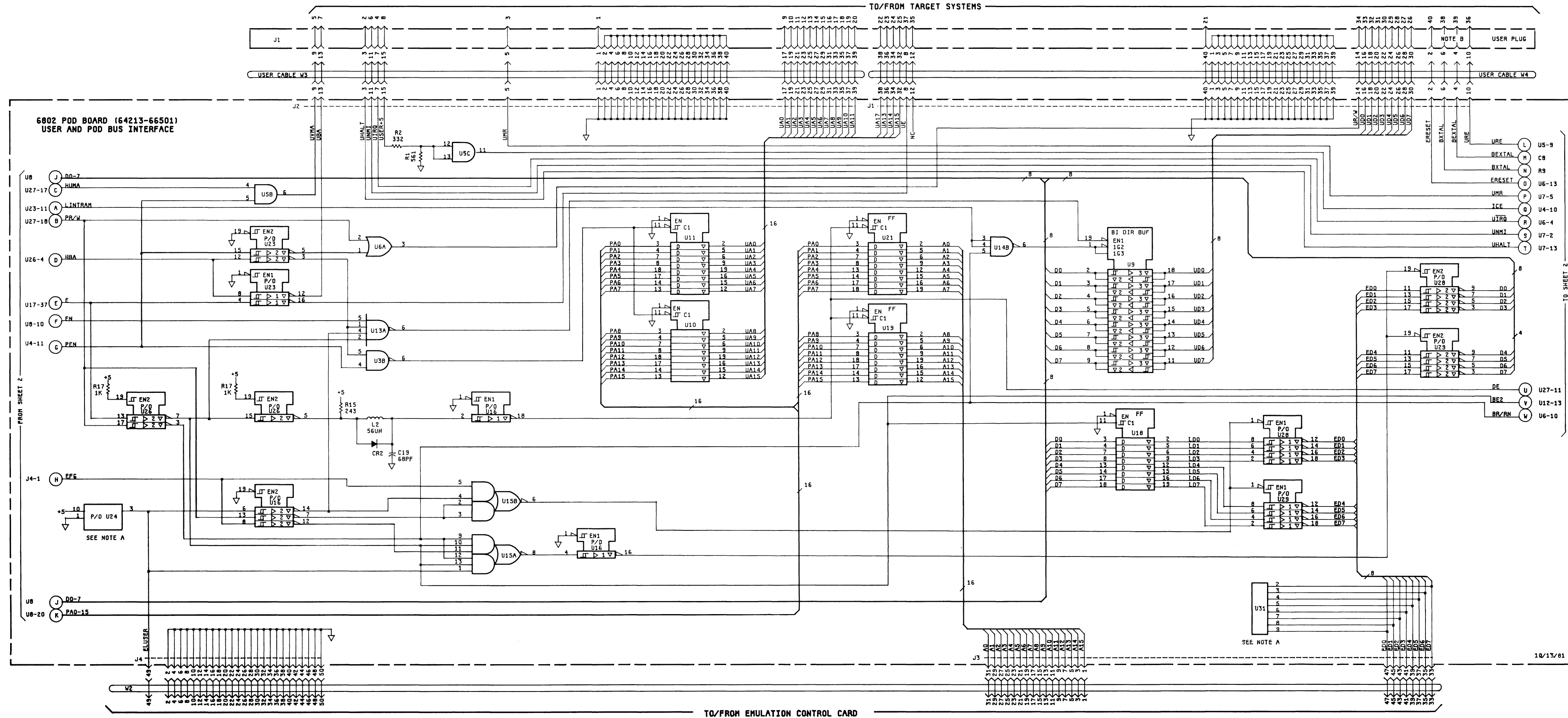


Figure 2

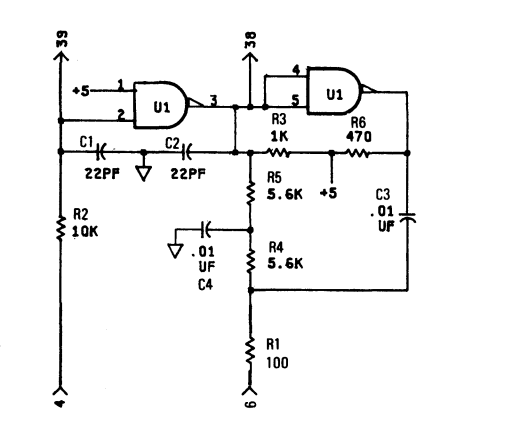
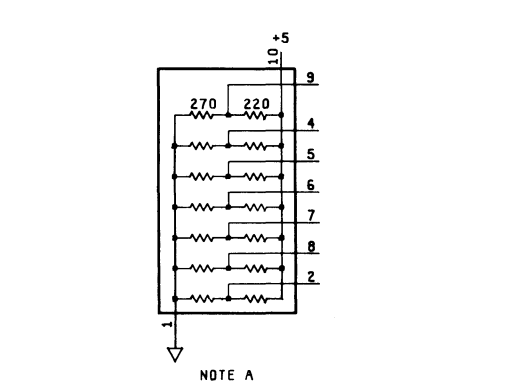


ICS ON THIS SCHEMATIC POWER PINS

REF. DES.	HP PART NO.	MFR. PART NO.	+5	GND
U3	1820-1367	74508	14	7
U5	1820-1201	74LS08	14	7
U6	1820-1208	74LS32	14	7
U7	1820-1918	74LS241	20	10
U9	1820-2075	74LS245	20	10
U10,11	1820-2102	74LS573	20	10
U13	1820-0688	74520	14	7
U14	1820-0685	74510	14	7
U15	1820-1210	74LS551	14	7
U16,22	1820-1676	745240	20	10
U18-19,21	1820-1676	745373	20	10
U26,28,9	1820-1624	745241	20	10

PARTS ON THIS SCHEMATIC

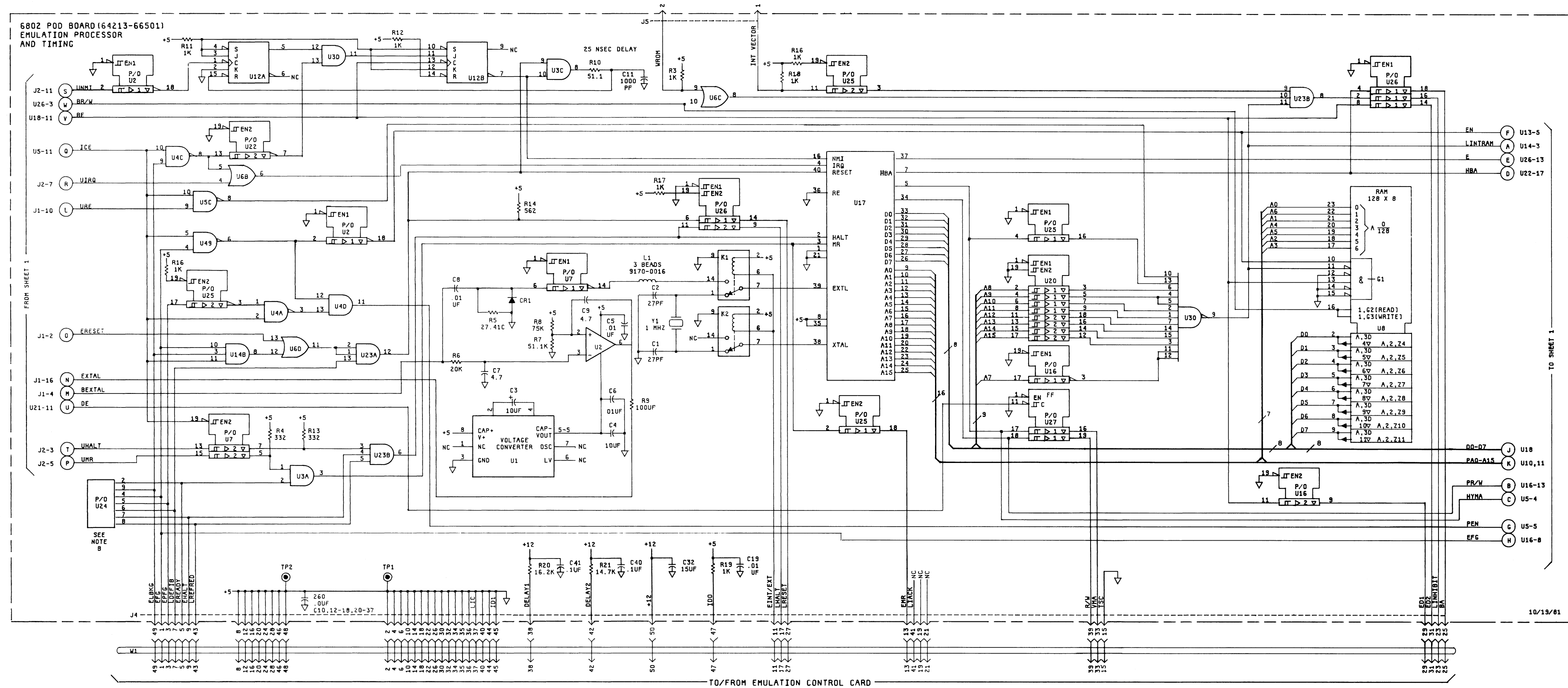
- C19
- CR2
- J1-3
- L2
- R1, 2, 15, 17
- U3, 5-7, 9-11, 13-16, 18, 19, 21, 22, 24, 26, 28, 29, 31



U1 IS 74LS08 EXT. OSC. CIRCUIT IS INTERNAL TO USER PLUG AND IS NOT REPAIRABLE

1

Figure 8-9. 6802 Emulator Pod, Service Sheet 1 8-33/(8-34 blank)



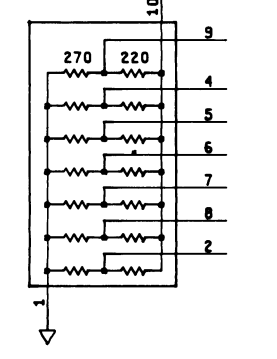
ICS ON THIS SCHEMATIC

REF DES	HP PART NO	MFG PART NO	+S	RET	-S
U1	1826-0851	ICL7660	8	3	5
U2	1820-0217	741 OP AMP	7	-	4
U3	1820-1367	74S08	14	7	-
U4	1820-0681	74S00	14	7	-
U5	1820-1201	74LS08	14	7	-
U6	1820-1208	74LS32	14	7	-
U7	1820-1918	74LS241	20	10	-
U8	1818-1751	68810	24	1	-
U12	1820-0629	74S112	16	8	-
U14	1820-0685	74S10	14	7	-
U16,20	1820-1633	74S240	20	10	-
U22					
U17	1820-2752	68808	8,35	1,21	-
U23	1820-0686	74S11	14	7	-
U25,26	1820-1624	74S241	20	10	-
U27	1820-1676	74S373	20	10	-
U30	1820-1130	74S133	16	8	-

PARTS ON THIS SCHEMATIC

- C1-18,20-41
- CR1
- J4,5
- K1,2
- L1
- U1-8,12,14,16,17,23-27,30
- R3-14,16,18-21
- TP1,2
- Y1

NOTE A



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Figure 8-10.
6802 Emulator Pod, Service Sheet 2
8-35

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Arranged alphabetically by country

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E Electronic Instruments & Measurement Systems
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 ** Support only for specific product line

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4



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