HEWLETT PACKARD

Engineering Diagrams Set

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First Edition ..... Jan 1979

PRINTING HISTORY

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The date on the title page and back cover of the manual changes only when a new edition is published. When an edition is reprinted, all the prior updates to the edition are incorporated. No information is incorporated into a reprinting unless it appears as a prior update. The edition does not change.

First Edition ..... Jan 1979

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TABLES

GENERAL INFORMATION

SECTION I

1-1. INTRODUCTION

The Engineering Diagrams set provides component location and schematic diagrams for the HP 3000 series 33 computer system. Also included is a breaf explanation of some logic symbology used to document the system, signal, and power distribution information.

1-2. SCOPE

This manual is intended for use by the Customer Engineers who are familiar with the system theory and maintenance procedures.

1-3. SECTIONS

0 Section II, Logic Symbology. Section II describes the logic symbology used in the system. It also provides integrated circuit diagrams and describes their operation.

0 Section III, Diagrams. Section III contains schematic, part location, and part number information for printed circuit assemblies (PCA's) used in the system.

0 Section IV, Wiring Information. Section IV contains information on connections between PCA's and functional areas.

0 Section V, Hardware Assemblies. Section V provides information to orient the reader to the system hardware and assembly procedures.

LOGIC SYMBOLOGY

SECTION II

2-1. INTRODUCTION

2-2. This section covers basic logic information and symbology as used in this and related manuals. Following the description of symbology is a table of integrated circuits containing diagram symbols for most circuits and descriptions of operation for complex logic functions.

2-3. LOGIC STATES.

2-4. The logic signals are always in one of two possible states, a "1" or a "0." These two states are also referred to as high (H) or low (L). The high and low states reflect the relative voltage levels of the signals; the high state is always relatively more positive than the low state. Note that both states may have actual voltage values that are positive, or both may be absolutely negative; the significance is in the *relative* levels of the two states. In the text of the manuals, logic states are normally described as "high" or "low."

2-5. The "not" bar associated with signal names is used to indicate whether the "active" state of the signal is high or low. For example, if the presence of data on a signal line is represented by a low signal, the signal name for the line might be "not" Data 1; if a signal clears the output register when the signal is low, the signal might be described as "not" Clear Output Register ($\overline{\text{COR}}$). The "not" bar must be considered an integral part of the signal name; this means that there are high states for "not" signals and low states for "not" signals, just as there are high and low states for signals without the "not" bar.

2-6. INVERSION.

2-7. Logic inversion is indicated by an inversion dot at the input or output of a logic symbol. When this dot appears at the input of a logic symbol, the input will be effective when the input signal is low. When the dot appears at the output of a logic symbol the output will be of the opposite state to what would be delivered if the dot were not present.

2-8. LOGIC SYMBOLOGY.

2-9. Three basic symbol shapes distinguish the major classes of logic circuits depicted in this manual. These are gates, regenerative switching elements, and amplifiers. Each symbol and a brief explanation of its operation is given in the following paragraphs.

2-10. In addition to the basic symbols, a general multipurpose symbol is used wherever a standardized logic symbol does not exist. A brief explanation of this multipurpose symbol is included.

2-11. GATES.

2-12. A gate is a circuit that produces a binary output when certain input conditions are met. The gate symbol has input lines connecting to one side of the symbol, and output lines connecting to the other side, as shown in figure 2-1. Since the inputs and outputs are easily identifiable, the symbol can be shown left-facing, right-facing, or facing up or down.

2-13. There are four basic types of gates: "and," "or," "nand," and "nor," each named for the logic function that it performs. Each of these gates is described in the following paragraphs. In addition, a brief explanation of an "expander" gate is given following the descriptions of the basic logic gates.

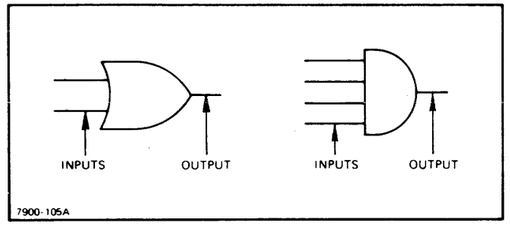
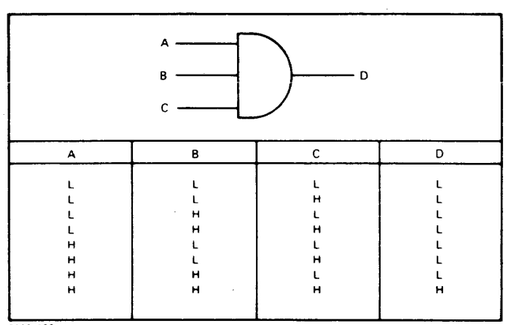


Figure 2-1. Gate Symbols

2-14. "AND" GATE.

2-15. The "and" gate shown in figure 2-2 performs a logical "and" function. It will produce a high output only when all of the input lines are high. Input A *and* input B *and* input C must be high for a high output to be generated.

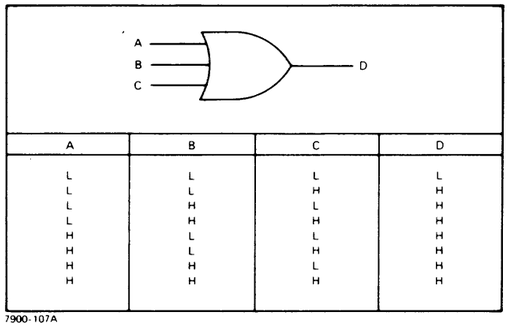


A	B	C	D
L	L	L	L
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	H

Figure 2-2. Three-Input "And" Gate Logic Symbol and Truth Table

2-16. "OR" GATE.

2-17. The "or" gate performs a logical "or" function. It produces a high output when one *or* more inputs are high. The truth table in figure 2-3 shows the various states of a three-input "or" gate.

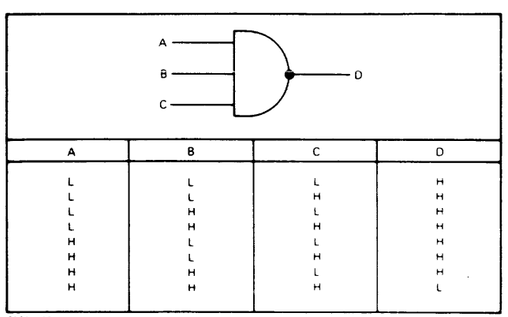


A	B	C	D
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	H

Figure 2-3. Three-Input "Or" Gate Logic Symbol and Truth Table

2-18. "NAND" GATE.

2-19. The "nand" gate is similar to the "and" gate described previously, except that its output is inverted. The gate generates a low output when all inputs are high. The various states of a three-input "nand" gate are shown in the truth table in figure 2-4.

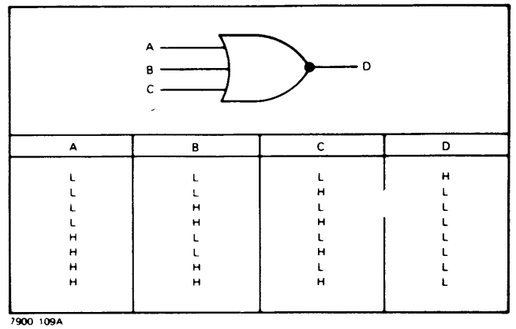


A	B	C	D
L	L	L	H
L	L	H	H
L	H	L	H
L	H	H	H
H	L	L	H
H	L	H	H
H	H	L	H
H	H	H	L

Figure 2-4. Three-Input "Nand" Gate Logic Symbol and Truth Table

2-20. "NOR" GATE.

2-21. The "nor" gate is identical to the "or" gate described previously, except that its output is inverted. The gate generates a low output when one or more inputs are high. The various states of a three-input "nor" gate are shown in the truth table in figure 2-5.

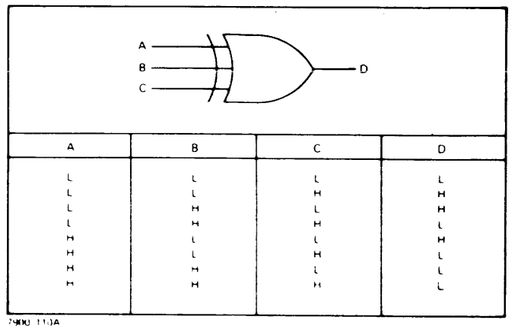


A	B	C	D
L	L	L	H
L	L	H	L
L	H	L	L
L	H	H	L
H	L	L	L
H	L	H	L
H	H	L	L
H	H	H	L

Figure 2-5. Three-Input "Nor" Gate Logic Symbol and Truth Table

2-22. "EXCLUSIVE OR" GATE.

2-23. The "exclusive or" gate is a variation of the basic "or" gate. It has two or more input signals. The output is high when only one input is high. The truth table in figure 2-6 shows the functioning of a three-input exclusive "or" gate.



A	B	C	D
L	L	L	L
L	L	H	H
L	H	L	H
L	H	H	L
H	L	L	H
H	L	H	L
H	H	L	L
H	H	H	L

Figure 2-6. Three-Input "Exclusive Or" Gate Logic Symbol and Truth Table

2-24. EXPANDER GATE

2-25. Some logic gates have additional input lines which may be used to increase or "expand" the number of input signals. These expanding input lines use different signal levels than the normal gate input. The expander gate provides these special signal levels. The expander gate may provide one or two output lines to drive the expanded gate.

2-26. An expanded input will normally be indicated by the letter "E". Figure 2-7 shows both single and double line expanded inputs. When more than one expander gate is used the expanded inputs are connected together.

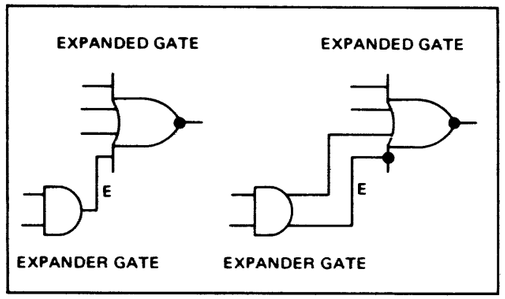


Figure 2-7. Expander Gate Logic Symbol

2-27. STROBE LINES.

2-28. Strobe lines may be used to enable the output lines of tri-state logic elements. The strobe inputs are shown connected at right angles to the normal signal flow. Examples of a strobe controlled gate and amplifier are shown in figure 2-8.

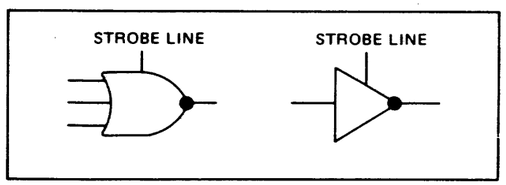


Figure 2-8. Strobe Controlled Gate and Amplifier Symbols

2-29. ENCODING GATE.

2-30. The encoding gate (figure 2-9) has one input and multiple outputs. When the input is high, all outputs (B, C, and D) are high. When the input is low, the outputs are all low.

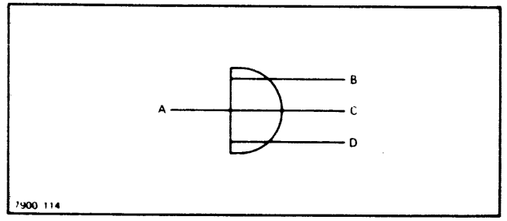


Figure 2-9. Three-Input Encoding Gate, Logic Symbol

2-31. A typical circuit for an encoding gate is shown in figure 2-10. With A high, all diodes conduct and all outputs are clamped high. With A low, each diode is practically an open circuit, and points B, C, and D assume the voltage level of the circuit to which each is connected.

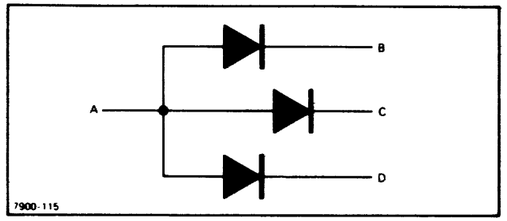


Figure 2-10. Typical Encoding Gate Circuit

2-32. MULTIVIBRATORS.

2-33. The multivibrators described here are of four main types: flip-flops, Schmitt trigger circuits, one-shot multivibrators, and free-running multivibrators. All furnish a binary output. However, unlike gate circuits, the duration of a multivibrator output signal is not dependent on the duration of an input signal.

2-34. The basic logic symbol for a multivibrator is a rectangle as shown in figure 2-11. Letters in the symbol indicate the type of multivibrator. The rectangle is divided horizontally, with the upper portion representing the "set side" and the lower portion representing the "clear side." The multivibrator is considered set when the output from the set side is high. It is considered cleared when the output from the clear side is high. To avoid confusion, the symbol is always oriented as shown in figure 2-11 inputs on the left, outputs on the right.

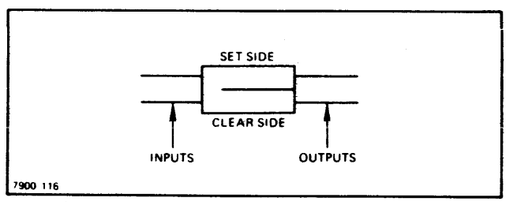


Figure 2-11. Basic Logic Symbol Multivibrator

2-35. FLIP-FLOP.

2-36. The symbol for a flip-flop is shown in figure A-12. The letters "FF" preceded by the name of the flip-flop distinguish this symbol from other types of multivibrators. Additional identification, described later, identifies the particular type of flip-flop.

2-37. A flip-flop is a bistable switching device; an external signal is required to set the flip-flop and another to clear it. The flip-flop remains in its current state until switched to the opposite state by the appropriate external signal. Various forms of flip-flops exist, of which seven are described here: the R-S (reset-set), clocked R-S, J-K, clocked J-K, toggle, latch, and delay flip-flops.

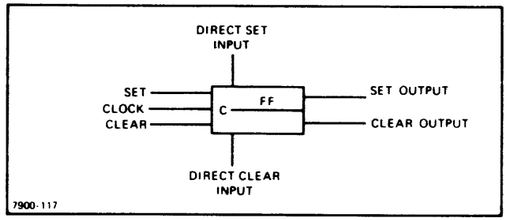
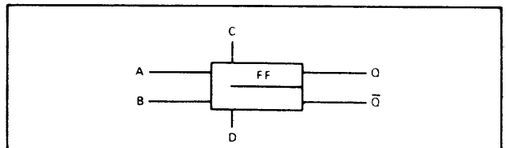


Figure 2-12. General Flip-Flop Logic Symbol

2-38. R-S FLIP-FLOP. The symbol for the R-S flip-flop as shown in figure 2-13 can be recognized by the fact that there is no information in the symbol identifying it as one of the other six types. The R-S flip-flop has a minimum of two input terminals (A and B in figure 2-13) and one or two output terminals Q and $\overline{Q}$. One or two additional input terminals, C and D, may be used.

2-39. The R-S flip-flop is set by a high input at A (assuming no inverting dot at this point). It can also be set by a high input at C, if this input terminal is present. The flip-flop is cleared by a high input at B or D. Figure 2-13 includes a truth table, showing the flip-flop outputs resulting from various input conditions.



INPUT		OUTPUT	
A	B	Q	$\overline{Q}$
L	L	No Change	
H	L	H	L
L	H	L	H
H	H	Indeterminate	

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Figure 2-13. R-S Flip-Flop, Logic Symbol, and Truth Table

2-40. After being set or cleared, the R-S flip-flop remains in that condition after termination of the set or clear pulse. If the flip-flop is either set or clear and it receives an input to place it in the existing state no change takes place in the state of the flip-flop.

2-41. Simultaneously high set and clear input signals normally are not permitted, and circuit design usually prevents occurrence of this condition at a time when the flip-flop outputs are used. If simultaneous set and clear inputs are received, both outputs of the flip-flop are high for the duration of the simultaneous inputs. The eventual state of the flip-flop is determined by the input that remains high longest.

2-42. CLOCKED R-S FLIP-FLOP. The clocked R-S flip-flop is similar to the R-S flip-flop, but it has a clock pulse input as shown in figure 2-14. The logic symbol can be recognized by the letter "C" at this input terminal. At the positive-going transition of the clock pulse, the flip-flop becomes set if input A is high, or it becomes clear if input B is high (assuming no inverting dot at the clock pulse input terminal). If inputs A and B are both low during the clock pulse, the flip-flop does not change state. It is not permissible that A and B both be high when the positive-going clock pulse transition takes place.

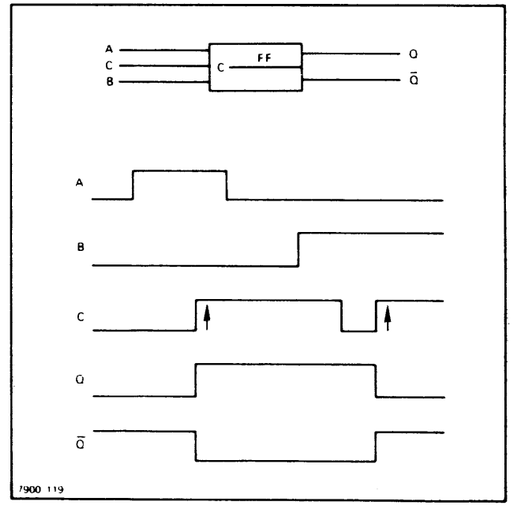


Figure 2-14. Clocked R-S Flip-Flop, Logic Symbol, and Switching Waveforms

2-43. When the clocked R-S flip-flop has an inverting dot at the clock pulse input (figure 2-15), the negative-going transition of the clock pulse is the transition that is effective in setting or clearing the flip-flop.

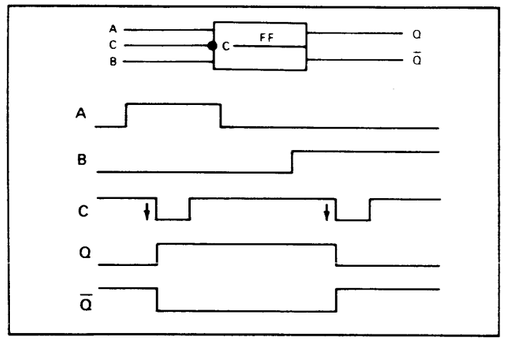


Figure 2-15. R-S Flip-Flop with Inverted Clock Input, Logic Symbol, and Switching Waveforms

2-44. In some cases the clocked R-S flip-flop has a set and clear input at the top and bottom of the logic symbol (inputs D and E, figure 2-16). These inputs are independent of the clock pulse, and are referred to as the direct set and direct clear inputs. They function as a result of a high or low level, rather than a positive- or negative-going transition. An inverting dot at the direct set or clear input indicates that a low level is required to set or clear the flip-flop. No dot indicates that a high level is required. The direct set and clear inputs are also used on other types of flip-flops.

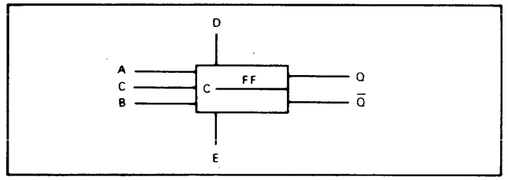


Figure 2-16. Logic Symbol for Clocked R-S Flip-Flop with Direct Set and Direct Clear Inputs

2-45. TOGGLE FLIP-FLOP. The symbol for the toggle flip-flop as shown in figure 2-17 can be recognized by the letter "T" in the symbol. This flip-flop has a single input. If there is no inverting dot at this input, each time the input signal becomes high, outputs Q and $\overline{Q}$ change state. Since two inputs are required to produce one complete cycle of the output, the toggle flip-flop functions as a divide-by-two element, and is commonly used in groups in counting circuits, with the output of one flip-flop driving the next. Figure 2-17 shows the switching waveforms for one flip-flop.

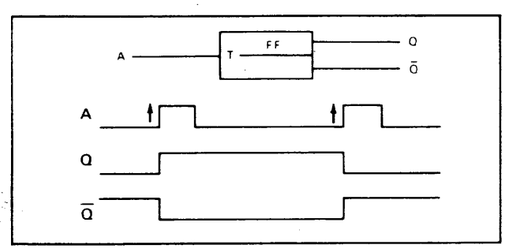


Figure 2-17. Toggle Flip-Flop Logic Symbol and Switching Waveforms

2-46. If a toggle flip-flop symbol has an inverting dot at the input connection, the flip-flop changes state at the negative-going transition of the input. The symbol and waveforms for this type of flip-flop are shown in figure 2-18.

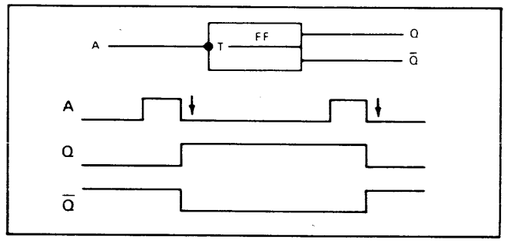


Figure 2-18. Toggle Flip-Flop with Inverted Input, Logic Symbol, and Switching Waveforms

2-47. J-K FLIP-FLOP. In the J-K flip-flop, simultaneous high inputs for both set and clear will reverse the existing state of the flip-flop. This requires some method of storing two conditions, the previous output state and the new output state, until the clock pulse time. The set and clear inputs are labeled J and K respectively. In order to provide the necessary output storage the flip-flops are combined in a dual-rank configuration, together with the necessary gates to form a single logic element. For simplicity the internal dual-rank arrangement of the flip-flop is not usually shown. (See figure 2-19.)

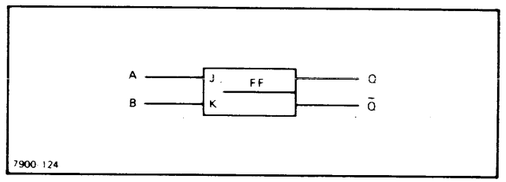


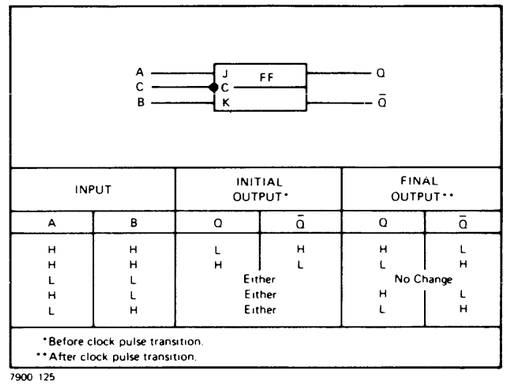
Figure 2-19. J-K Flip-Flop Logic Symbol

2-48. CLOCKED J-K FLIP-FLOP. The clocked J-K flip-flop as shown in figure 2-20 is similar to the clocked R-S flip-flop. However, simultaneous set and clear inputs to the J-K flip-flop are permissible. Under these conditions, the J-K flip-flop changes its state at the occurrence of each positive-going clock pulse transition. With an inverting dot at the clock pulse input, the flip-flop changes state at the negative-going clock pulse transition. If both J and K inputs are high, the flip-flop will toggle when a clock pulse is received.

2-49. The J-K flip-flop can also be operated with one high input and one low input. It then functions in the same manner as the clocked R-S flip-flop.

2-50. Figure 2-20 includes a truth table showing operation of the J-K flip-flop. Note that with both inputs high at the time of clock pulse transition, the final state of the flip-flop (after clock pulse transition) depends on the state before the transition. With only one input high, the initial state of the flip-flop is immaterial.

2-51. In some cases the J-K flip-flop consists of two separate flip-flops, with the output of one applied to the input of the other. Usually, a single flip-flop logic symbol is used to illustrate this circuit. The clock-pulse inverting dot, or the lack of it, indicates the clock pulse transition that affects the output flip-flop of the pair.



INPUT		INITIAL OUTPUT*		FINAL OUTPUT**	
A	B	Q	$\overline{Q}$	Q	$\overline{Q}$
H	H	L	H	H	L
H	H	H	L	L	H
L	H	Either		No Change	
H	L	Either		H	L
L	L	Either		L	H

*Before clock pulse transition.
**After clock pulse transition.

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Figure 2-20. Clocked J-K Flip-Flop Logic Symbol and Truth Table

2-52. LATCH FLIP-FLOP. The latch flip-flop shown in figure 2-21 can be recognized by the letter "L" in the symbol. The flip-flop has a clock input and a data input. Although the logic symbol shows one input-signal connection to the flip-flop, this seperates inside the integrated circuit package to form two inputs to the pack. After separation, one input is inverted (indicated by the inverting dot) before application to the flip-flop.

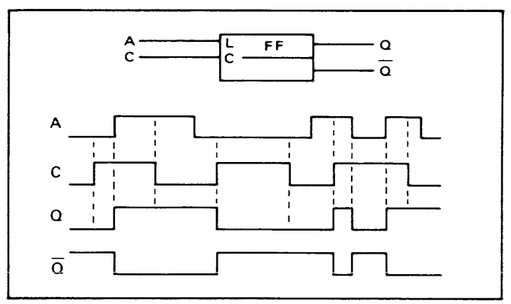


Figure 2-21. Latch Flip-Flop Logic Symbol and Switching Waveforms

2-53. The set-side input is responsive to high signal levels at A in figure 2-22, and the clear input is responsive to low signal levels at A. If there is no inverting dot at the clock input, this response takes place when the clock pulse is high. While the clock pulse remains high, the outputs follow any changes in the logic level at A as these changes take place. When the clock pulse becomes low, the flip-flop retains its current state, and no longer responds to changes of the input signal.

2-54. If the clock input connection of a latch flip-flop has an inverting dot, the flip-flop responds to the input signal while the clock pulse is low.

2-55. DELAY FLIP-FLOP. The delay flip-flop shown in figure 2-22 is identified by a letter "D" inside the flip-flop symbol. This type of flip-flop is similar to the latching flip-flop, except that it responds to the input signal only at the transition of the clock pulse. The delay flip-flop thus does not follow changes in the input signal as these changes take place.

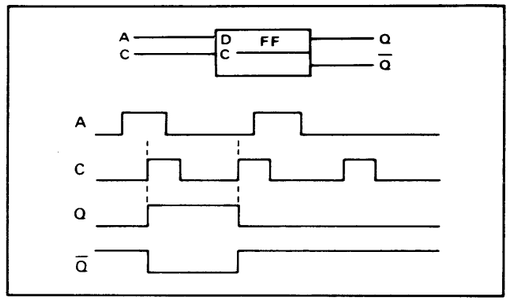


Figure 2-22. Delay Flip-Flop Logic Symbol and Switching Waveforms

2-56. GATE FLIP-FLOP. The gate flip-flop is made up of two logic gates, connected as shown in figure 2-23. The number of inputs to each gate can vary from that shown. The flip-flop can also be made up of two "nor" gates. The circuit may have a set output, a clear output, or both.

2-57. The gate flip-flop functions like an R-S flip-flop, but it has the advantage that it can "or" inputs without the addition of a separate "or" gate. Another reason for use of the gate flip-flop is that if two spare gates are available in integrated circuits on a circuit card, they can be employed as an R-S flip-flop without the need to add another integrated circuit to the card.

2-58. If the flip-flop is made up of two "nand" gates, as in figure 2-23, it is set by a low input at either A or B. Similarly, it is cleared by a low input at C or D. When the flip-flop is in the quiescent state (not undergoing transition), the inputs at A, B, C, and D are all high.

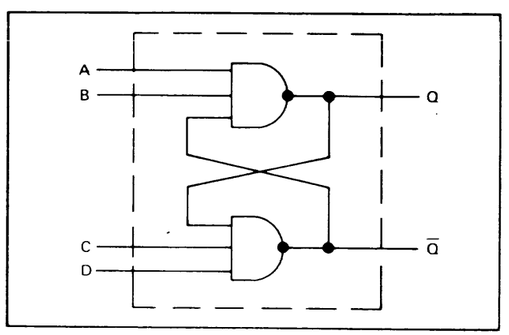


Figure 2-23. "Nand" Gate Flip-Flop, Logic Symbol

2-59. A "nor" gate flip-flop is shown in figure A-24. In this type of flip-flop all inputs are low when the device is in the quiescent state. A high input at A sets the flip-flop, and a high input at B clears it. The outputs cross in the illustration in order to align the set and clear inputs with the set and clears outputs, respectively.

2-60. In most circuits using the "nand" or "nor" gate flip-flop, input signals are such that the flip-flop does not receive high set and clear input signals simultaneously. If circuit design does permit this to occur, both the set- and the clear-side outputs are high for the duration of the condition. The eventual state of the flip-flop is determined by the input that remains longest in the activating condition.

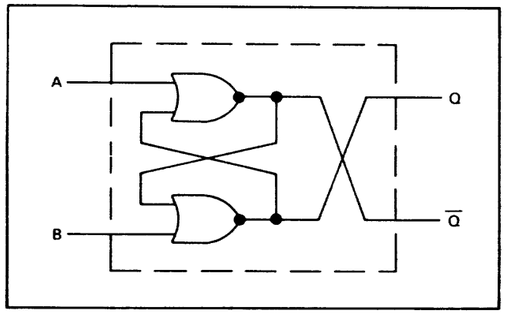


Figure 2-24. "Nor" Gate Flip-Flop Logic Symbol

2-61. SCHMITT TRIGGER.

2-62. The Schmitt trigger circuit shown in figure 2-25 can be identified by the letters "ST" appearing in the logic-diagram symbol. Like the various types of flip-flops this circuit is a two-state device which does not perform a Boolean function. It serves for level sensing or signal squaring. It may have a set-side output, a clear-side output, or both.

2-63. When the input voltage at A is below a certain level, the Schmitt trigger is in the clear state. When the input voltage rises above the reference level, the trigger assumes the set state. Circuit constants establish the reference level.

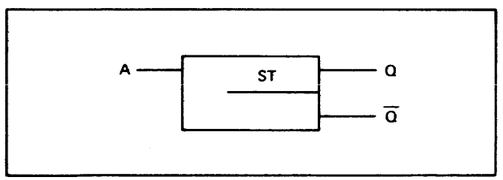


Figure 2-25. Schmitt Trigger Circuit Logic Symbol

2-64. Switching between states takes place rapidly, and the Schmitt trigger is therefore useful for squaring signals that have poor rise and fall times. It can produce a square-wave from a sine wave. Other uses of the Schmitt trigger are voltage level restoration, and detection of the rise of the input signal above a given level.

2-65. ONE-SHOT

2-66. The one-shot multivibrator (figure 2-26) is a monostable switching element, used to produce a pulse of predetermined duration. The device is triggered into its unstable state by an external signal. It returns to the stable state after a time interval determined by circuit constants.

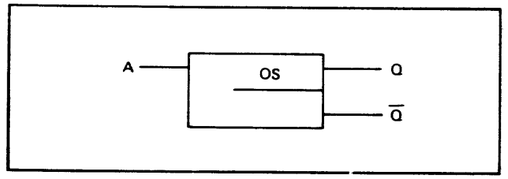


Figure 2-26. One-Shot Multivibrator Logic Symbol

2-67. If there is no inverting dot at the input, triggering is accomplished when input A undergoes a positive-going transition. If there is an inverting dot, a negative-going transition is required. The one-shot multivibrator may have a set-side output, a clear-side output, or both.

2-68. The symbol for the one-shot multivibrator is always drawn with the orientation shown in figure 2-26, with the input at the left and the output or outputs at the right.

2-69. FREE-RUNNING MULTIVIBRATOR.

2-70. The free-running multivibrator shown in figure 2-27 can be distinguished by the letters "MV" appearing in the symbol. This device produces trains of complementary pulses at Q and $\overline{Q}$. Pulse width is determined by circuit constants.

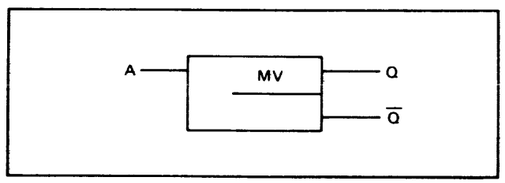


Figure 2-27. Free-Running Multivibrator Logic Symbol

2-71. In some instances a control signal is applied to the free-running multivibrator. If there is no inverting dot at the signal input to the symbol, the multivibrator runs when the control signal is high, and stops when the signal is low. When it is stopped, the multivibrator is in the clear condition. If there is an inverting dot at the control signal input, a low input is required to bring the multivibrator into operation. This type of multivibrator is in the set condition when it is not running.

2-72. Figure 2-28 shows typical waveforms for a controlled free-running multivibrator that runs when the control signal is high. The high and low portions of the output waveforms need not be of equal duration.

2-73. The symbol for the free-running multivibrator is always drawn with the orientation shown in figure 2-28, with the input (if any) at the left, and the output or outputs at the right.

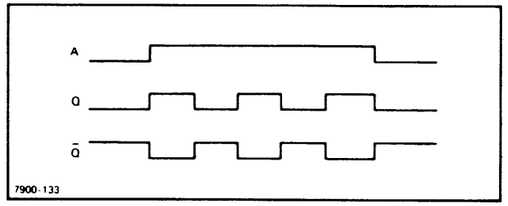


Figure 2-28. Input and Output Waveforms of Controlled Free-Running Multivibrator

2-74. AMPLIFIER.

2-75. The symbol for an amplifier is shown in figure 2-29. A differential amplifier is illustrated in figure 2-30. Like gates, these symbols may be oriented in any of four positions.

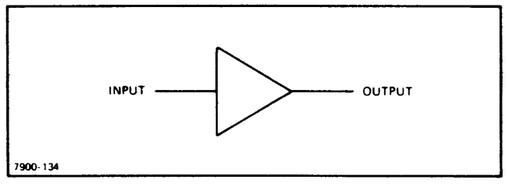


Figure 2-29. Amplifier Logic Symbol

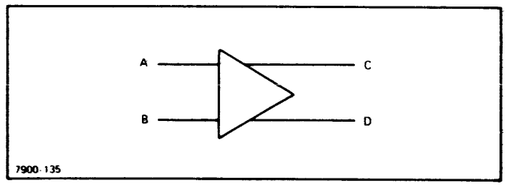


Figure 2-30. Differential Amplifier Logic Symbol

2-76. In most instances, the amplifier symbol has a non-binary input. A circuit which restores the voltage level of a binary input, or which furnishes a low-impedance output from a binary input, is indicated by a one-input "and" gate symbol. An inverting dot at the output of an amplifier symbol indicates that the amplifier inverts the input signal.

2-77. MULTIPURPOSE LOGIC SYMBOL.

2-78. The multipurpose logic symbol is used to indicate a logic function that has not received a standardized logic symbol. The multipurpose symbol is also used to depict multiple logic elements that act together to perform a single overall logic function such as decoding, data storage, or counting. The symbol shown in figure 2-31 may be of varying proportions (mostly commonly 2:1 or 1:2), but rectangular in shape. The symbol includes a descriptive name indicating the overall logic function performed. All active inputs should be labeled to indicate the effect on the overall function. Other descriptive information may be included as needed.

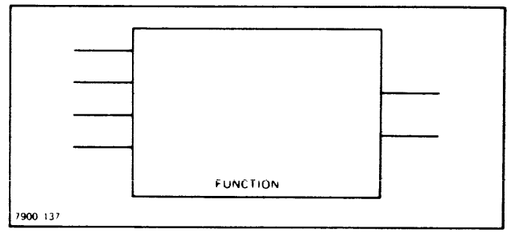


Figure 2-31. Multipurpose Logic Symbol

2-79. Examples of nonstandard symbols are given in figure 2-32. Figure 2-32a shows a binary-to-octal decoder. Figure 2-32b shows a four-bit up/down counter.

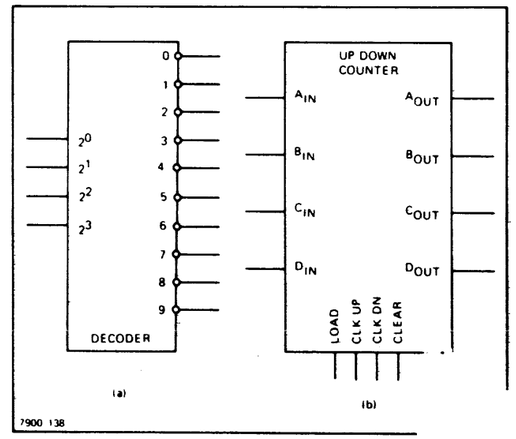
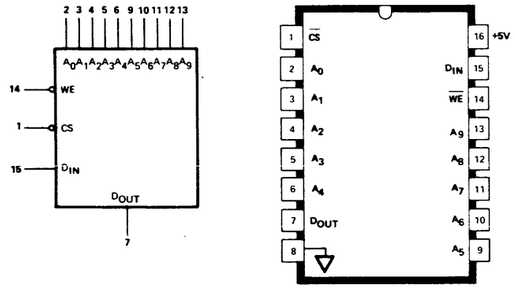
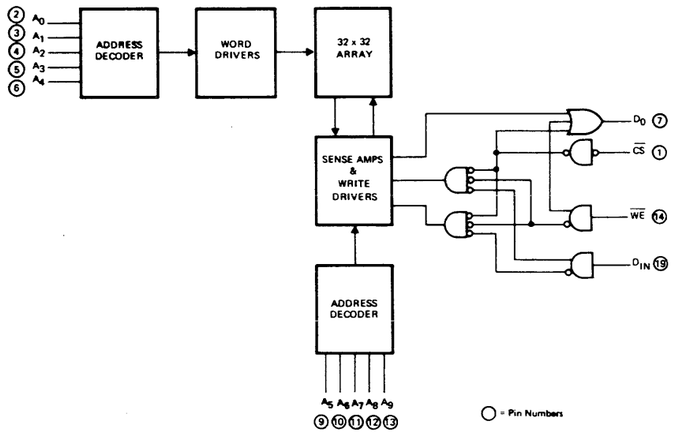


Figure 2-32. Nonstandard Logic Symbols

1816-0914
1024 BIT RAM

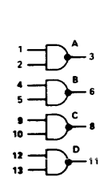


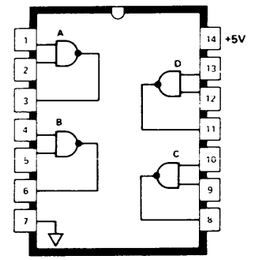
LOGIC DIAGRAM



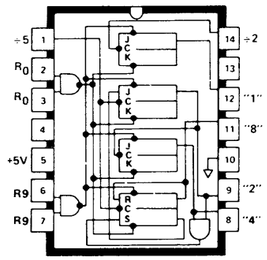
The 1024-bit RAM is organized in 1024 words by 1-bit. Full address decoding is included in the chip. Read and write operations are controlled by the state of the active low Write Enable $\overline{WE}$. With $\overline{WE}$ held low and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held high and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

1820-0054
QUAD 2-INPUT NAND GATE

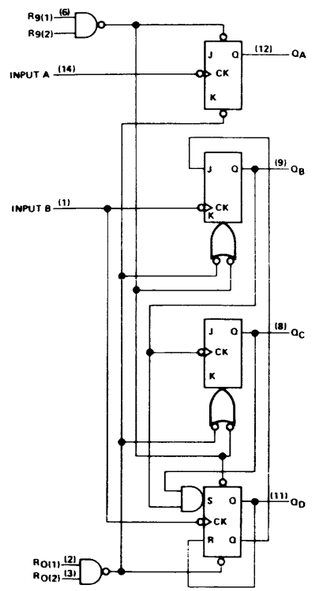


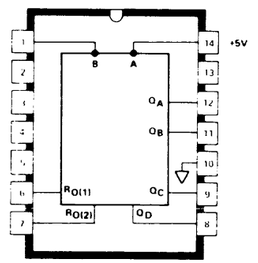


1820-0055
DECADE COUNTER



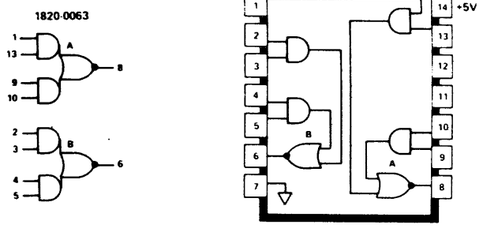
1820-0056
DIVIDE BY 12 COUNTER



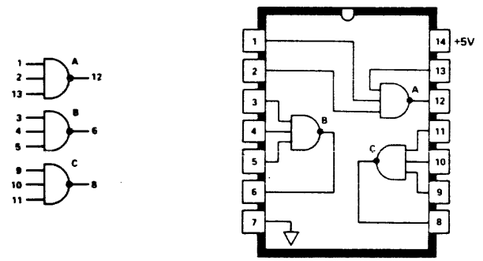


COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	L	H	L
9	H	L	H	H
10	H	H	L	L
11	H	H	L	H

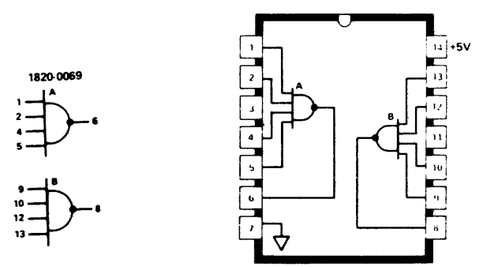
1820-0063
DUAL 2-WIDE 2-INPUT AND-NOR GATE



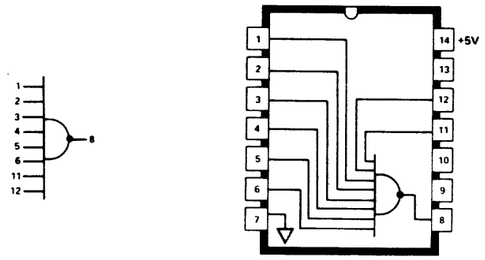
1820-0068
TRIPLE 3-INPUT NAND GATE



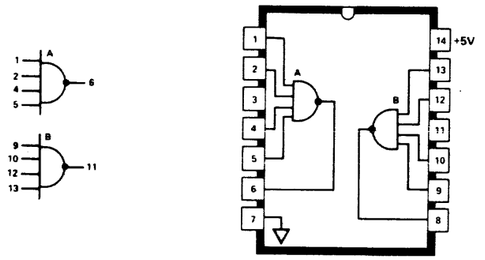
1820-0069
DUAL 4-INPUT NAND GATE



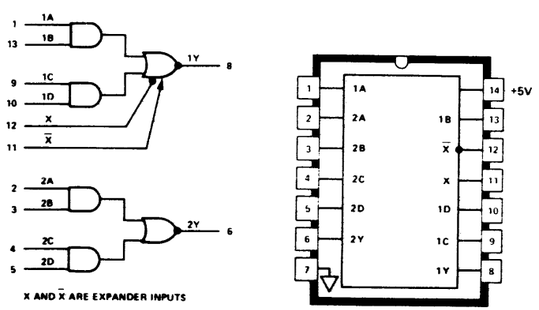
1820-0070
8-INPUT NAND GATE



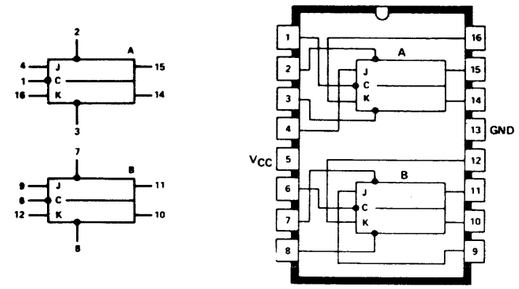
1820-0071
DUAL 4-INPUT NAND GATE



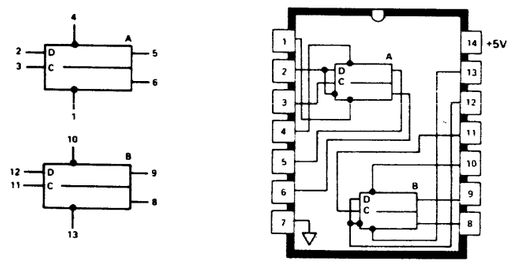
1820-0072
DUAL 2-WIDE 2-INPUT AND-NOR GATE



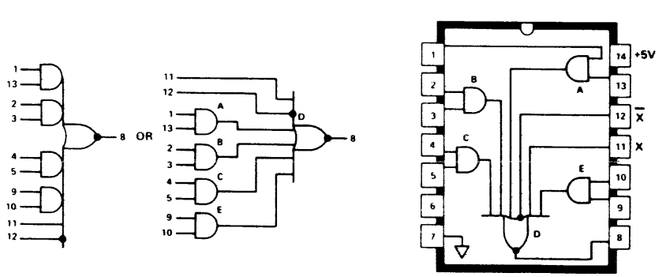
1820-0076
DUAL JK FLIP-FLOP



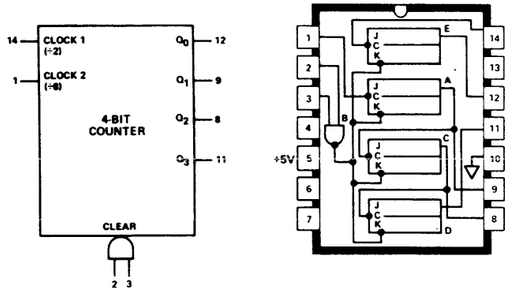
1820-0077
DUAL D FLIP-FLOP



1820-0084
4-WIDE AND-NOR GATE

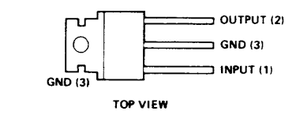


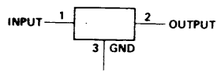
1820-0099
4-BIT BINARY COUNTER



High input signals on the clock 1 line cause the output at Q_0 to toggle. High input signals on the CLOCK 2 line cause outputs Q_1 - Q_3 to count. If the Q_0 output is used as the CLOCK 2 input, then the circuit will act as a simple 4-bit (÷ 16) counter. Simultaneous high signals at pins 2 and 3 will clear the counter.

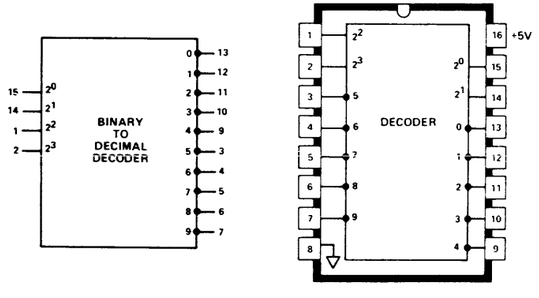
1820-0106
VOLTAGE REGULATOR





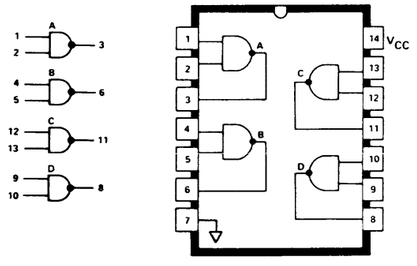
This integrated circuit is a 15 + 0.6 Vdc three terminal positive voltage regulator with current limiting. If internal power dissipation becomes to high thermal shutdown circuit takes over thus preventing the IC from overheating.

1820-0111
BINARY-TO DECIMAL DECODER

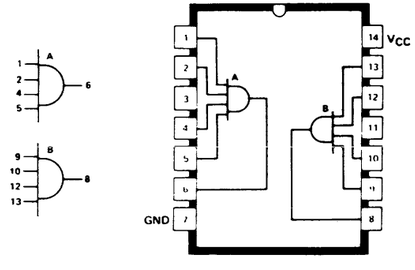


Data on the input lines is interpreted as a binary number. The output line representing the decimal equivalent of the binary input will go low and remain low until the input data is changed. Input data for decimal numbers greater than 9 result in all outputs being high.

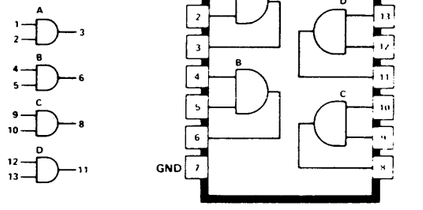
1820-0127
QUAD 2-INPUT NAND GATE



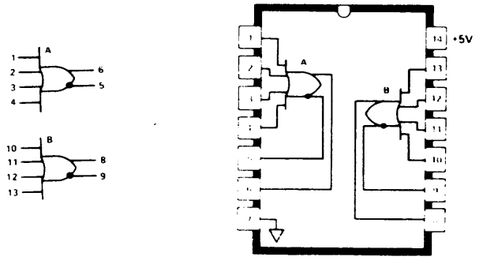
1820-0140
DUAL 4-INPUT AND GATE



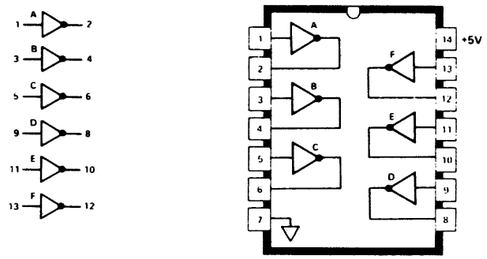
1820-0141
QUAD 2-INPUT AND GATE



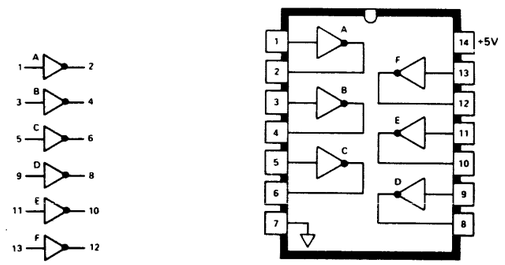
1820-0142
DUAL 4-INPUT OR-NOR GATE



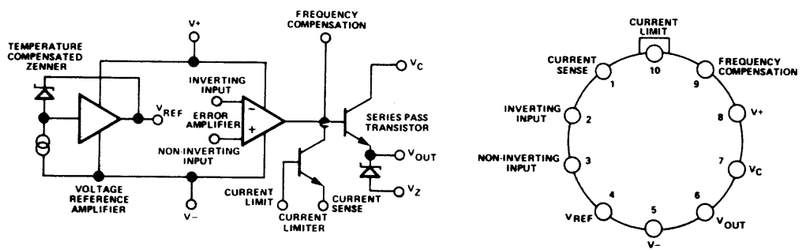
1820-0174
HEX INVERTER



1820-0175
HEX INVERTER

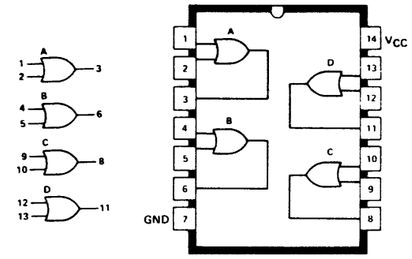


1820-0196
PRECISION VOLTAGE REGULATOR

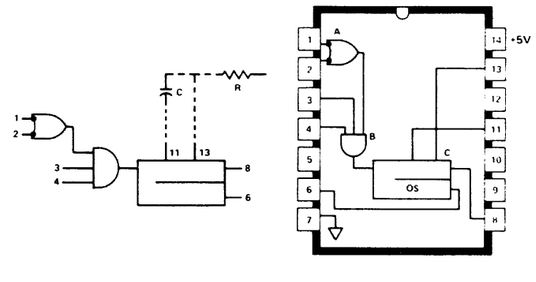


This integrated circuit provides a regulated output voltage and a low-current reference voltage. Provisions are included for voltage shut-down in the event of excessive current in an external circuit. The integrated circuit can be used with external components in a variety of configurations.

1820-0205
QUAD 2-INPUT CR GATE

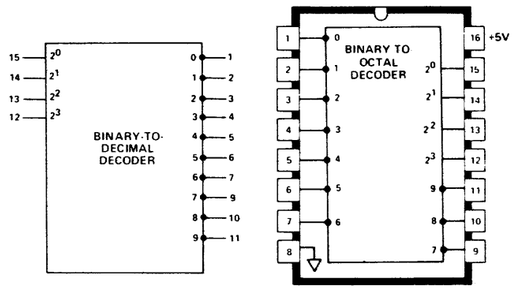


1820-0207
ONE-SHOT



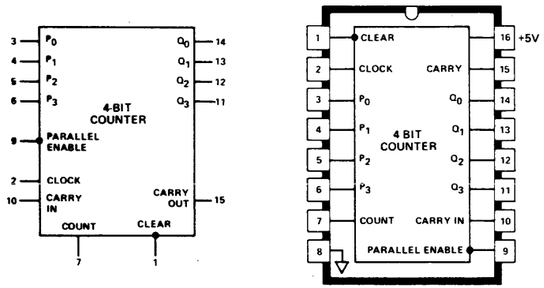
The one-shot is triggred bythe input signal. This produces a pulse with duration determined by the external RC elements.

1820-0214
BCD-TO-DECIMAL DECODER



The binary code on the input lines (2^0-2^3) is decoded and the appropriate output line (0-9) will go low. Codes greater than 9 result in all output lines remaining high.

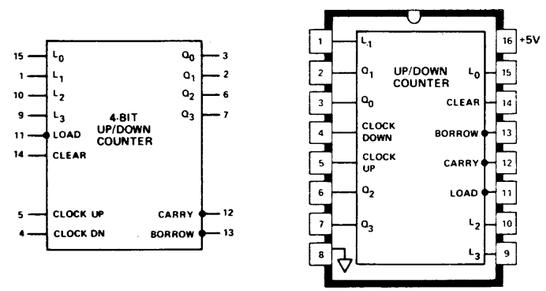
1820-0231
4-BIT COUNTER



The counter is set from the parallel input lines. When the clock input line goes high and a negative input is applied to the PARALLEL ENABLE line, the counter is loaded. When the clock goes high and both the COUNT and CARRY IN lines go high, the counter will be incremented. The new count will be present on the output lines following the low-to-high transition of the clock.

The CARRY OUT line will be high if the CARRY IN line is high and the counter lines are all high.

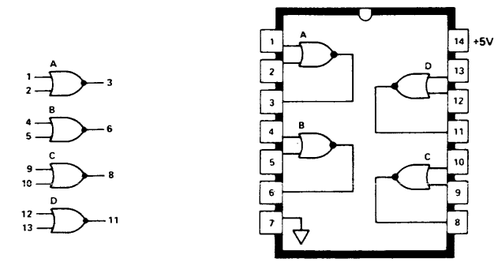
1820-0233
4-BIT UP/DOWN COUNTER



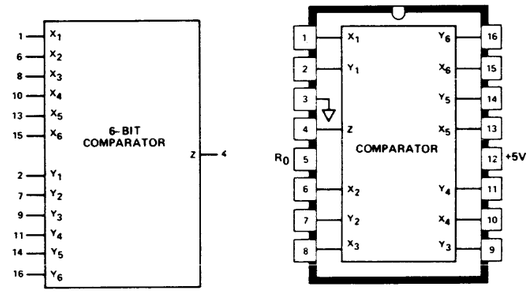
A negative pulse at the LOAD input will set the counter with the data on the input lines. A positive pulse on the CLEAR line will clear the counter. The counter is decremented for each positive-going pulse on the CLOCK DOWN line and incremented for each positive-going pulse on the CLOCK UP line.

A negative pulse occurs on the CARRY line when the outputs of the counter are all high and a negative pulse on the CLOCK UP line occurs. A negative pulse on the BORROW line occurs when the counter outputs are all low and a negative pulse on the CLOCK DOWN line occurs. When a BORROW pulse is generated the counter is set to all "ones".

1820-0239
QUAD 2-INPUT NOR GATE



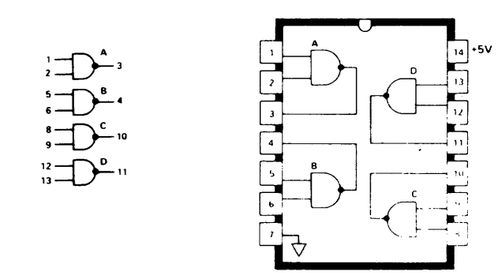
1820-0250
6-BIT COMPARATOR



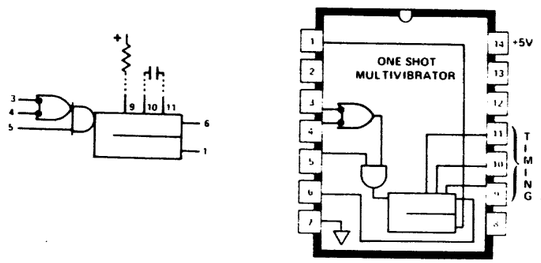
A- Z output is generated when each X input is equal to the respective Y input.

$$Z = (\overline{X_1 \otimes Y_1}) \cdot (\overline{X_2 \otimes Y_2}) \cdot (\overline{X_3 \otimes Y_3}) \cdot (\overline{X_4 \otimes Y_4}) \cdot (\overline{X_5 \otimes Y_5}) \cdot (\overline{X_6 \otimes Y_6})$$

1820-0256
QUAD 2-INPUT NAND GATE

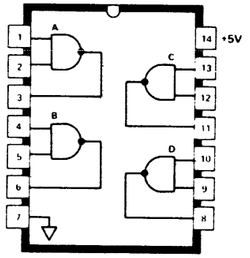


1820-0261
ONE-SHOT MULTIVIBRATOR

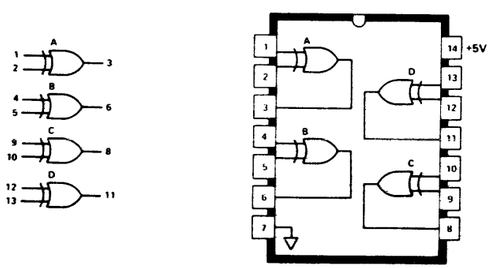


When input conditions are present an output pulse is generated. The pulse width may be determined by external timing circuits.

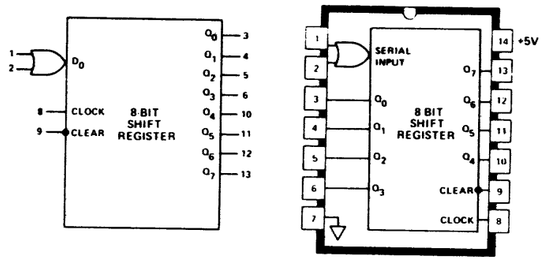
1820-0269
QUAD 2-INPUT POSITIVE NAND GATE



1820-0282
QUAD 2-INPUT EXCLUSIVE OR GATE

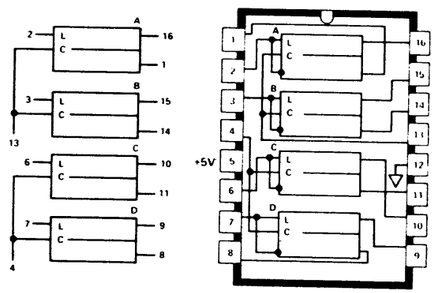


1820-0294
8-BIT SHIFT REGISTER

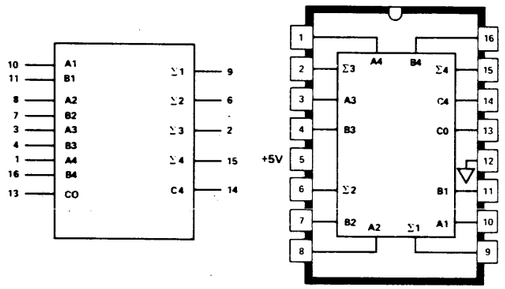


A positive clock pulse shifts the register contents one bit position and loads serial data into position Q_0. A low CLEAR signal clears the register.

1820-0301
4-BIT LATCH



1820-0305
4-BIT BINARY FULL ADDER



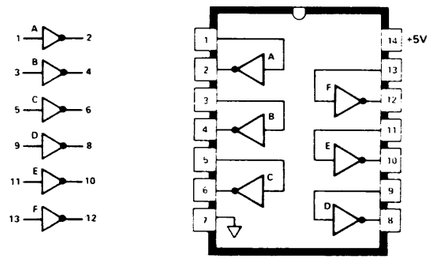
The full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C4) is obtained from the fourth bit.

INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	H	L	L	L	H	H	L
L	L	H	H	L	H	L	H	L	H
H	L	H	H	H	H	L	L	L	H
L	H	H	H	L	H	H	H	L	H
H	H	H	H	H	H	H	L	H	H
L	L	L	L	H	L	L	H	H	L
H	L	L	L	L	H	L	L	H	L
L	H	L	H	L	H	H	H	H	L
H	H	L	H	H	L	H	L	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	L	H
L	H	H	H	L	H	H	H	L	H
H	H	H	H	H	H	H	L	H	H

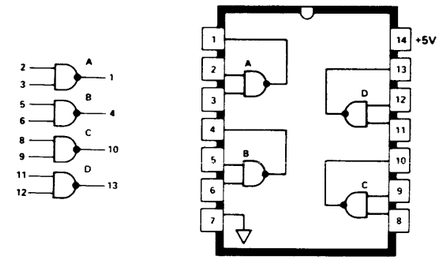
H = high level
L = low level

NOTE: Input conditions at A3, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

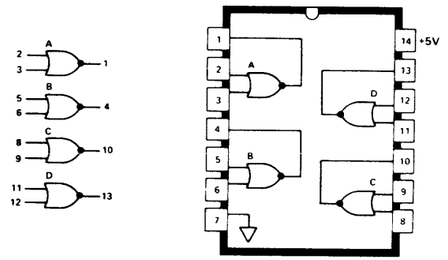
1820-0307
HEX INVERTER



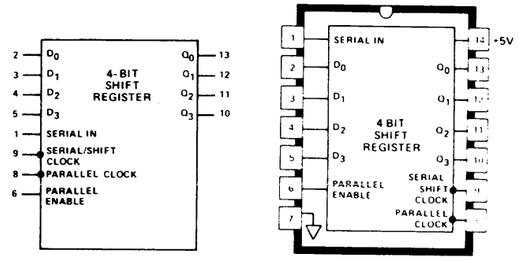
1820-0327
QUAD 2-INPUT NAND GATE



1820-0328
QUAD 2-INPUT NOR GATE

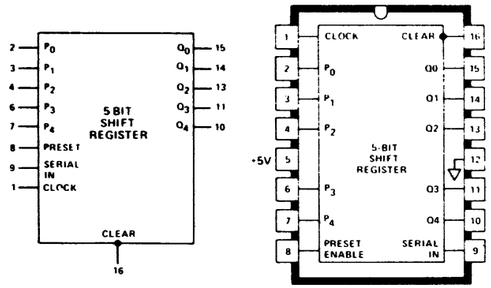


1820-0367
4-BIT SHIFT REGISTER



When the PARALLEL ENABLE line is high and a clock pulse occurs on the PARALLEL CLOCK line, data on parallel input lines (D_0 - D_3) will be stored in the register. Data is transferred to the output lines when the clock signal goes low. A clock pulse on the SERIAL SHIFT CLOCK line and a low on the PARALLEL ENABLE line will cause the contents of the register to be shifted one bit position. Data on the SERIAL IN line will be stored in the Bit 0 position. Data is transferred to the output lines when the clock goes low.

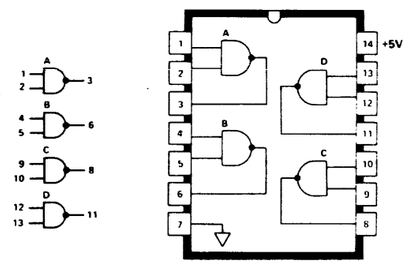
1820-0368
5-BIT SHIFT REGISTER



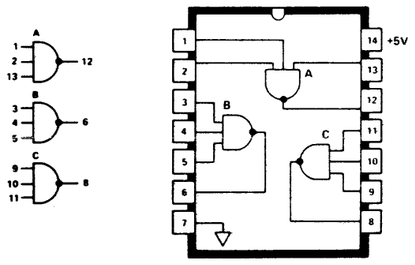
A high input signal on the PRESET line causes the register bits to be set if the corresponding P input line is high.

A clock signal loads the data present on the SERIAL IN line into the first register position and shifts the contents of the register.

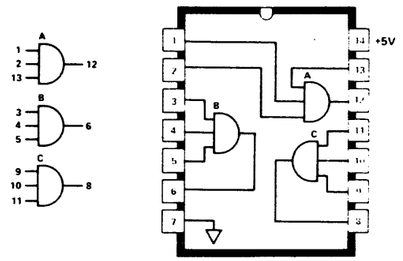
1820-0370
QUAD 2-INPUT NAND GATE



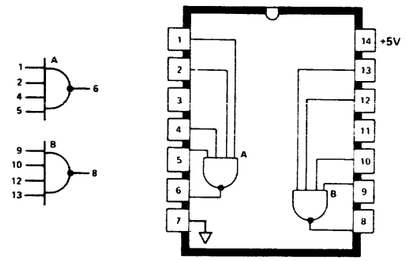
1820-0371
TRIPLE 3-INPUT NAND GATE



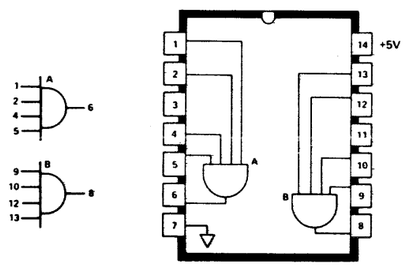
1820-0372
TRIPLE 3-INPUT AND GATE



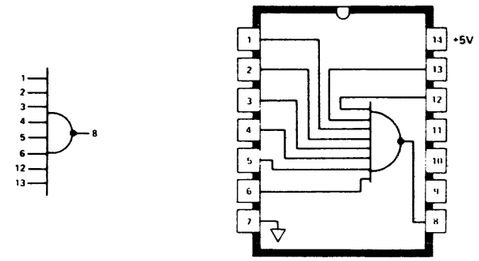
1820-0373
DUAL 4-INPUT NAND GATE



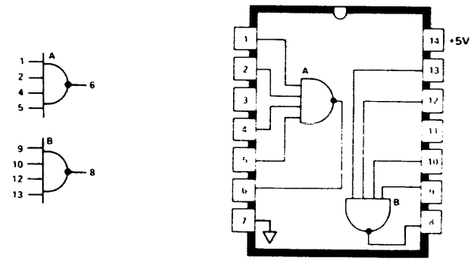
1820-0374
DUAL 4-INPUT AND GATE



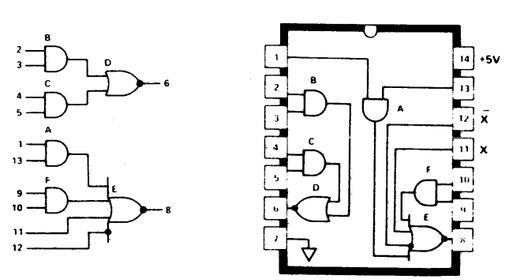
1820-0375
8-INPUT NAND GATE



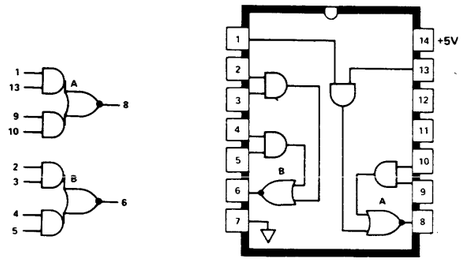
1820-0376
DUAL 4-BIT NAND GATE



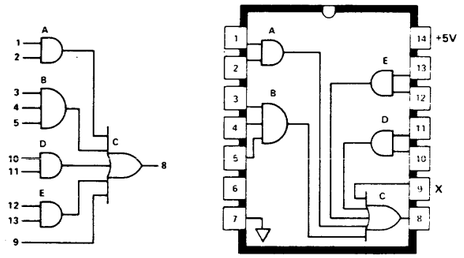
1820-0377
DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATE



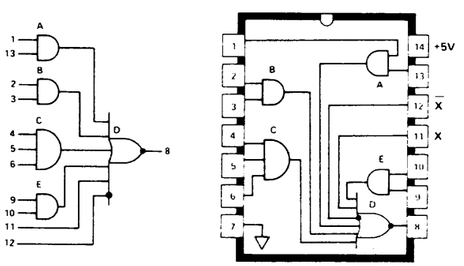
1820-0378
DUAL 2-WIDE 2-INPUT AND-NOR GATE



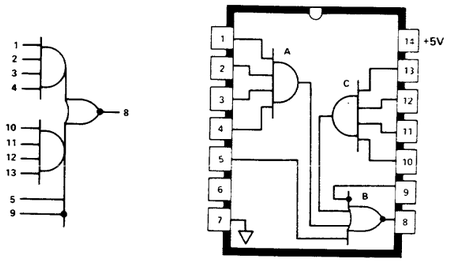
1820-0379
4-WIDE AND-OR GATE



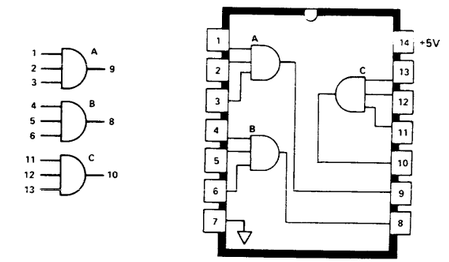
1820-0380
EXPANDABLE 4-WIDE AND-NOR GATE



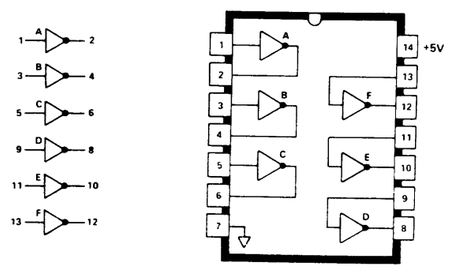
1820-0382
2-WIDE 4-INPUT AND-NOR GATE



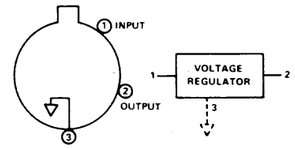
1820-0384
TRIPLE 3-INPUT AND GATE



1820-0424
HEX INVERTER

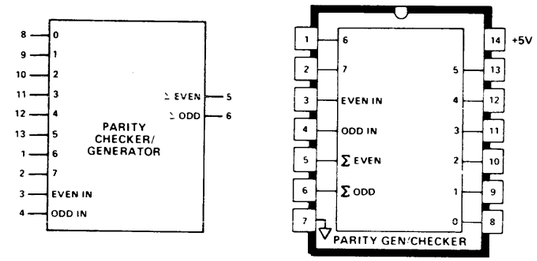


1820-0429
VOLTAGE REGULATOR



The regulator is a self-contained 5V regulator. Current limiting is included to limit the peak output current to a safe value. Thermal shutdown is also included to prevent overheating. Refer to the applicable equipment manual for specific use of the device.

1820-0435
9-BIT ODD/EVEN PARITY GENERATOR/CHECKER



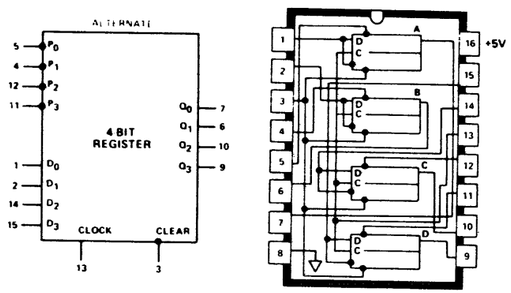
This circuit features odd/even outputs and control inputs to facilitate operation in either odd or even-parity applications. Depending on whether even or odd parity is being generated or checked, the even or odd inputs can be utilized as the parity or 9th-bit input.

FUNCTION TABLE

INPUTS			OUTPUTS	
Σ OF INPUTS AT 0 THRU 7	EVEN IN	ODD IN	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

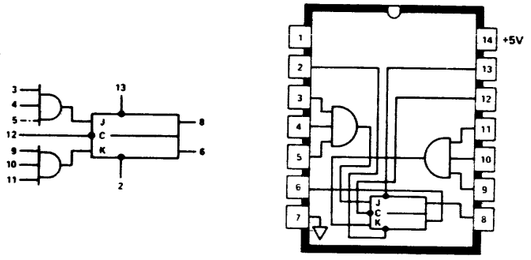
H = High Level, L = Low Level, X = Irrelevant

1820-0437
QUAD D FLIP-FLOP

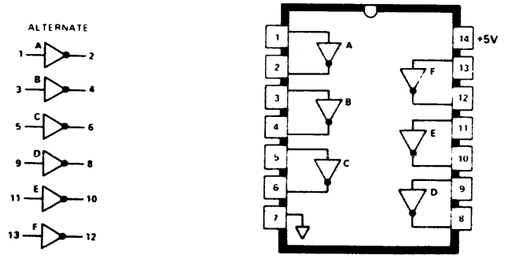


A low signal on any of the preset inputs (P_0-P_3) will cause the corresponding register bit to be set. A high on the clock line will cause the data on the D_0-D_3 lines to be stored. Data is stored on the positive going edge of the clock. A low on the CLEAR line clears the register.

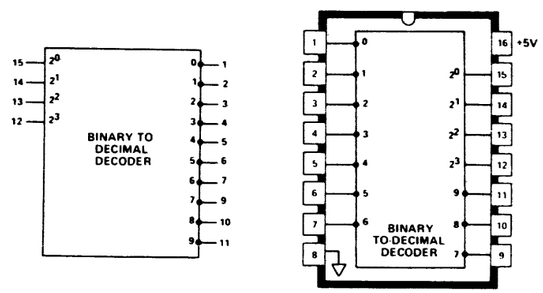
1820-0469
JK FLIP-FLOP WITH AND INPUTS



1820-0471
HEX INVERTER

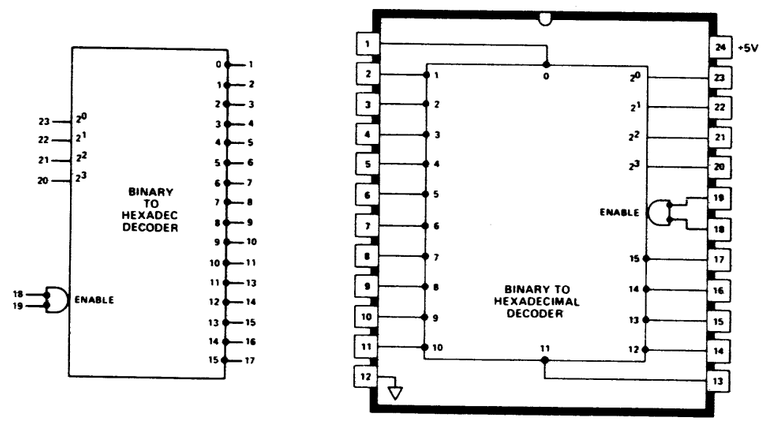


1820-0491
BINARY-TO-DECIMAL DECODER



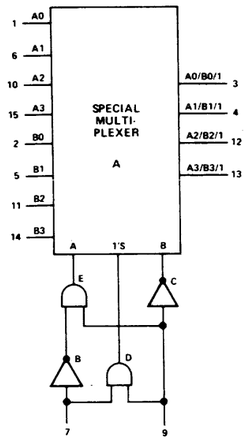
The binary input lines 2^0 through 2^3 appear directly as a decimal equivalent on the output lines 0 through 9 the selected output will be low. For binary inputs equivalent to decimal numbers greater than 9, all output lines will be high.

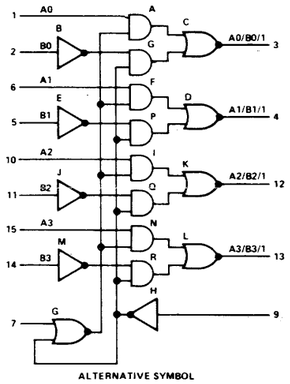
1820-0495
BINARY TO HEXADECIMAL DECODER

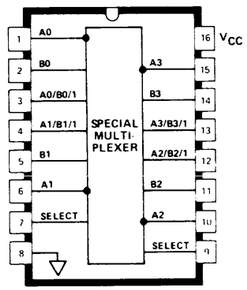


When both ENABLE inputs are low the binary coded input lines (2^0-2^3) are decoded and the equivalent output line (0-15) goes low.

1820-0506
2-INPUT 4-BIT MULTIPLEXER







This integrated circuit performs any of the following functions:

a. Passes (A0:A3) in 1's complement form.

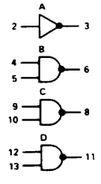
b. Passes (B0:B3) unchanged.

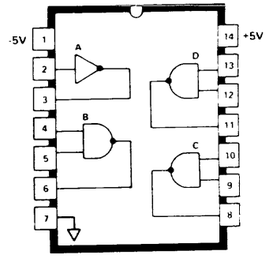
c. When like-numbered A and B inputs are connected, and with pin 7 low, the inputs are passed unchanged when pin 9 is low, or in 1's complement form when pin 9 is high.

d. Provides 1's at the outputs.

SELECT LINES		OUTPUTS			
PIN 7	PIN 9	PIN 3	PIN 4	PIN 12	PIN 13
L	H	A0	A1	A2	A3
X	L	B0	B1	B2	B3
H	H	1	1	1	1

1820-0509
TRIPLE 2-INPUT NAND-INVERT GATE

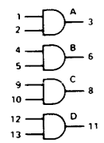


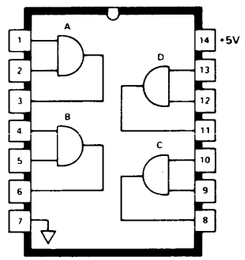


FUNCTION TABLE

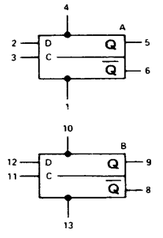
INPUTS			OUTPUTS	
Σ OF INPUTS AT 0 THRU 7	EVEN IN	ODD IN	Σ EVEN	Σ ODD
EVEN	H	L	H	L
ODD	H	L	L	H
EVEN	L	H	L	H
ODD	L	H	H	L
X	H	H	L	L
X	L	L	H	H

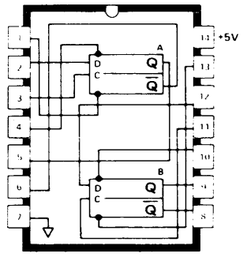
1820-0511
QUAD 2-INPUT AND GATE



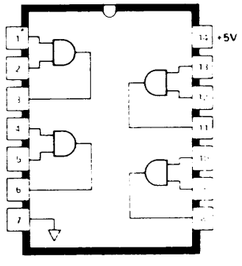


1820-0512
DUAL D FLIP-FLOP

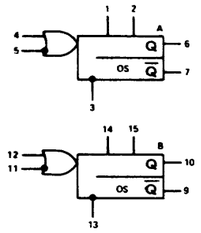


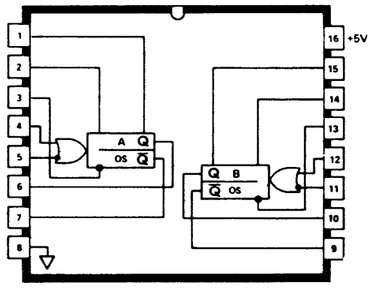


1820-0513
QUADRUPLE 2-INPUT POSITVE-AND GATES



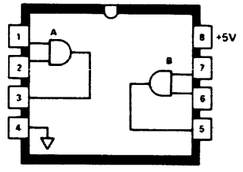
1820-0515
DUAL ONE-SHOT



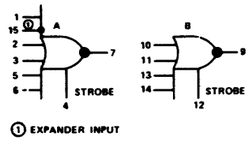


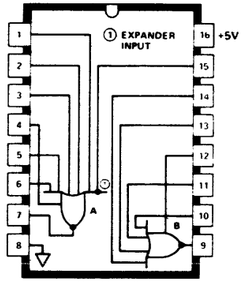
When either input condition is met the one shot will generate an output pulse. The pulse width is determined by an external RC network. The circuit may be initialized by a low clear input.

1820-0535
DUAL 2-INPUT AND GATE



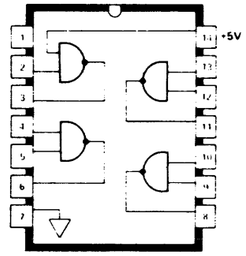
1820-0538
EXPANDABLE DUAL 4-INPUT POSITIVE NOR GATE



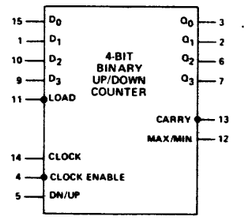


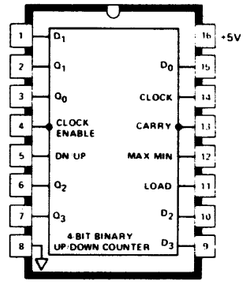
If any of the input lines are high or conditions for the expander input is present when the strobe input goes high, the output will go low.

1820-0539
QUAD 2-INPUT POSITIVE NAND GATE



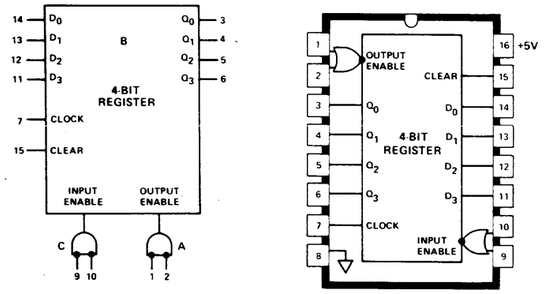
1820-0545
4-BIT BINARY UP/DOWN COUNTER





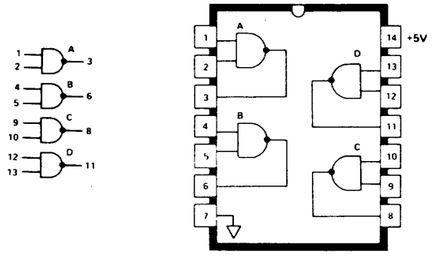
The counter is clocked by a low to high transition of the CLOCK line. The clock is effective only if the CLOCK ENABLE line is low. The CLOCK ENABLE line may only be changed while the CLOCK line is high. The direction of count is determined by the DN/UP line. If the DN/UP line is low the count is up. If the line is high the count is down. The counter may be preset with a low signal on the LOAD line. This will cause the data present on the input lines (D_0-D_3) to be stored. A low output signal is generated on the CARRY line if either a carry or borrow condition occurs. The MAX/MIN line outputs a high signal when the above conditions occur, but for a full clock cycle. This signal is used in "look-ahead carry" applications.

1820-0574
4-BIT REGISTER

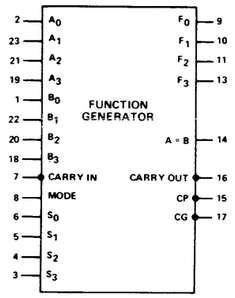


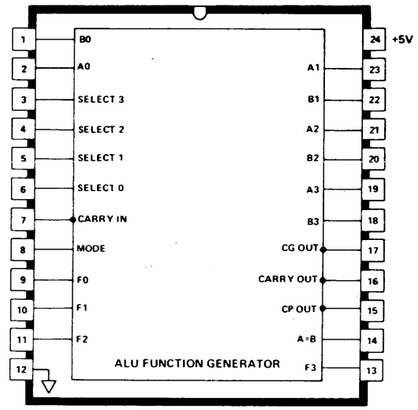
When INPUT ENABLE is true (both signal lines false) a true clock signal will cause data on the input lines to be stored. A true signal on the CLEAR line will clear the register. When OUTPUT ENABLE is true (both signal lines false) the contents of the register are gated to output lines Q_0 through Q_3.

1820-0605
QUAD 2-INPUT NAND GATE



1820-0606
ARITHMETIC LOGIC UNIT/FUNCTION GENERATOR





The MODE line determines whether an arithmetic or logic operation will be performed (A "1" for logic function and a "0" for arithmetic function). The S lines select the function to be performed according to the table given above. If the function code LHHL is used and the A inputs are the same as the B inputs the A=B output line will be true.

The CP (Carry Propagate) and CG (Carry Generate) lines are used for fast addition operations using a "look ahead" carry function. The CP line will go false when the following conditions are met: $CP = F_0 \cdot F_1 \cdot F_2 \cdot F_3$.

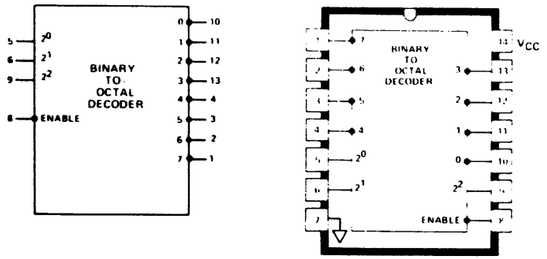
If the CARRY IN line is false and the CP condition is met, then the CARRY OUT line will also go false.

The CG line will go false if the pack addition results in a true CARRY OUT independent of the CARRY IN. The CG signal is defined as follows:

$$CG = A_3 \cdot B_3 + (A_2 \cdot B_2)(A_3 + B_3) + (A_1 \cdot B_1)(A_2 + B_2)(A_3 + B_3) + (A_0 \cdot B_0)(A_1 + B_1)(A_2 + B_2)(A_3 + B_3)$$

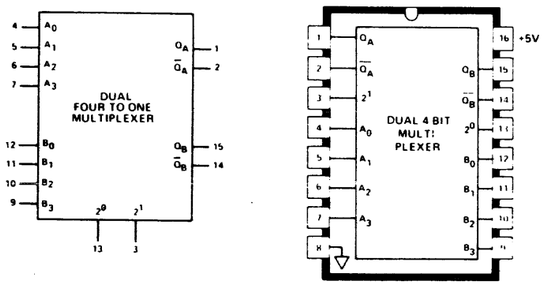
FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOGIC FUNCTIONS	ARITHMETIC OPERATIONS
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A+B}$	F = A+B
L	L	H	L	$F = \overline{A}B$	F = A+B
L	L	H	H	F = Logical 0	F = minus 1 (2's complement)
L	H	L	L	$F = \overline{AB}$	F = A plus $\overline{AB}$
L	H	L	H	$F = \overline{B}$	F = [A+B] plus $\overline{AB}$
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ minus 1
H	L	L	L	$F = \overline{A}+B$	F = A plus AB
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B
H	L	H	L	F = B	F = [A+$\overline{B}$] plus AB
H	L	H	H	F = AB	F = AB minus 1
H	H	L	L	F = Logical 1	F = A plus A 1
H	H	L	H	$F = A+\overline{B}$	F = [A+B] plus A
H	H	H	L	F = A+B	F = [A+$\overline{B}$] plus A
H	H	H	H	F = A	F = A minus 1

1820-0608
BINARY-TO-OCTAL DECODER



Binary data is decoded to octal when the ENABLE input is low. For a given input only one output line will be low.

1820-0610
DUAL 4-INPUT MULTIPLEXER



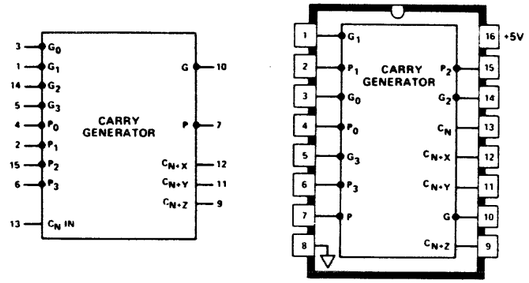
A two bit code selects one out of four bits to be propagated through the multiplexer. The dual output allows both states of the output bit to be used. A truth table of input codes and the resulting bit transfer is given.

TRUTH TABLE

SELECT LINES		INPUTS				OUTPUTS	
2^1	2^0	A_0	A_1	A_2	A_3	Q_A	$\overline{Q}_A$
0	0	0	X	X	X	0	1
0	0	1	X	X	X	1	0
0	1	X	0	X	X	0	1
0	1	X	1	X	X	1	0
1	0	X	X	0	X	0	1
1	0	X	X	1	X	1	0
1	1	X	X	X	0	0	1
1	1	X	X	X	1	1	0

X = irrelevant

1820-0611
LOOK AHEAD CARRY GENERATOR



This circuit is used together with 1820-0606 to provide fast addition. The Carry Generator uses CP (Carry Propagate) and CG (Carry Generate) signals from the adder circuits (P_0-P_3 and G_0-G_3) as well as the Carry In signal to the first adder circuit to provide carry in signals to succeeding adder circuits (C_{N+X}, C_{N+Y}, and C_{N+Z}). This is done without waiting for the "ripple carry" to propagate from adder to adder.

The G and P signals provide inputs to additional look ahead circuits if they are used. The output signals are defined as follows:

$$C_{N+X} = G_0 + P_0\, C_N$$

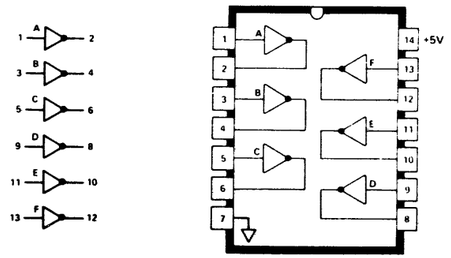
$$C_{N+Y} = G_1 + P_1\, G_0 + P_1\, P_0\, C_N$$

$$C_{N+Z} = G_2 + P_2\, G_1 + P_2\, P_1\, G_0 + P_2\, P_1\, P_0\, C_N$$

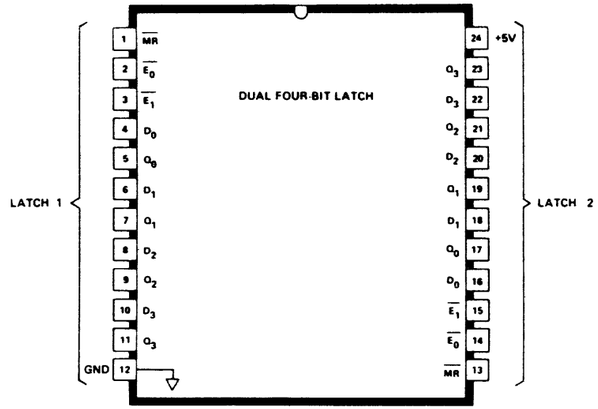
$$G = \overline{G_3 + P_3\, G_2 + P_3\, P_2\, G_1 + P_3\, P_2\, P_1\, G_0}$$

$$P = \overline{P_3\, P_2\, P_1\, P_0}$$

1820-0613
HEX INVERTER



1820-0614
DUAL FOUR-BIT LATCH



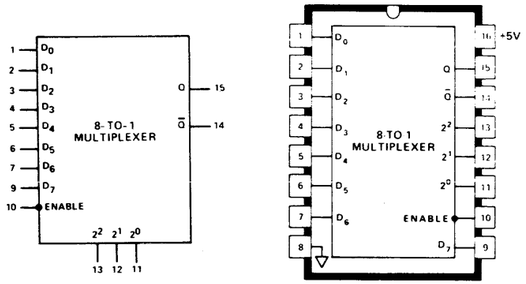
LATCH OPERATION — Data can be entered into the latch when both of the enable inputs are LOW. As long as this logic condition exists, output of the latch will follow the input. If either of the enable inputs goes HIGH, the data present in the latch at that time is held in the latch and is no longer affected by data input.

The master reset overrides all other input conditions and forces the outputs of all the latches LOW when a LOW signal is applied to the master reset input.

X = Irrelevant
L = LOW Logic Level
H = HIGH Logic Level
Q_n-1 = Previous Output State
Q_n = Present Output State

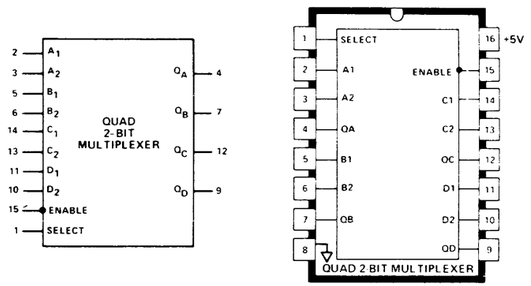
$\overline{MR}$	$\overline{E}_0$	$\overline{E}_1$	D	Q_0	OPERATION
H	L	L	L	L	Data Entry
H	L	L	H	H	Data Entry
H	L	H	X	Q_{n-1}	Hold
H	H	L	X	Q_{n-1}	Hold
H	H	H	X	Q_{n-1}	Hold
L	X	X	X	L	Reset

1820-0615
8-INPUT MULTIPLEXER



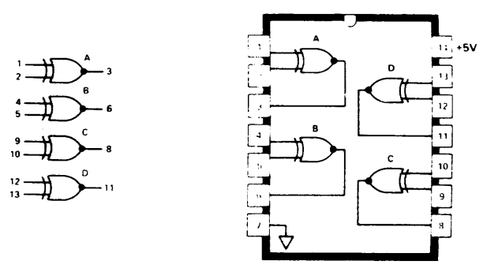
Data on one of the 8 input lines is transferred to the output line when the ENABLE line goes false. The specific input line to be transferred is determined by the three select lines.

1820-0616
QUAD 2-BIT MULTIPLEXER

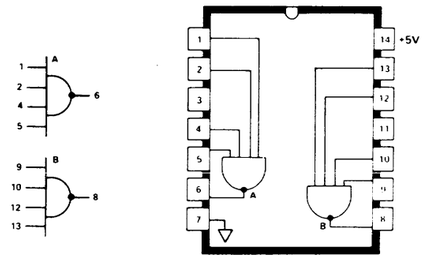


The circuit is used to select one of two four bit data words. The ENABLE must be low to allow the selection. The SELECT line is used to determine which data word will be transmitted. A "0" on the select line will transmit data word 1. A "1" on the select line will transmit data word 2.

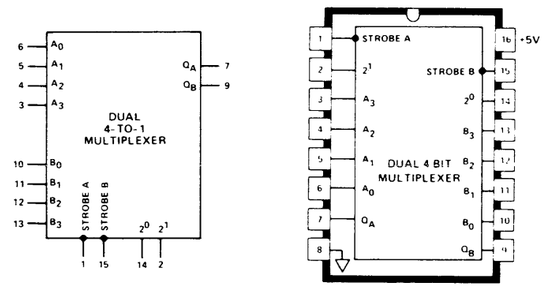
1820-0617
QUAD 2-INPUT EXCLUSIVE NOR GATE



1820-0619
DUAL 4-INPUT NAND GATE



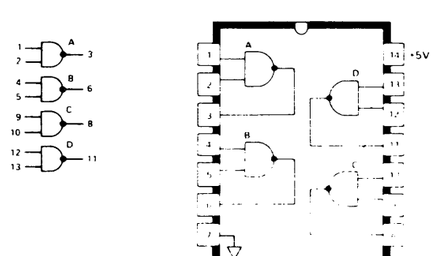
1820-0620
DUAL 4-BIT MULTIPLEXER



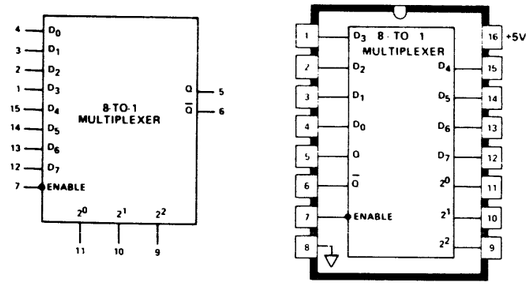
Each part of the multiplexer allows one of four bits to be placed at the output terminal. The data bits are placed on the input lines prior to the multiplexing operation. The code for the desired bit is then placed on the select lines (refer to the table above). The strobe line is used to gate the data bit onto the appropriate output line (A inputs to the Q_A terminal etc.).

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
2^1	2^0	A0	A1	A2	A3	A	QA
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

1820-0621
QUAD 2-INPUT EXCLUSIVE NOR GATE

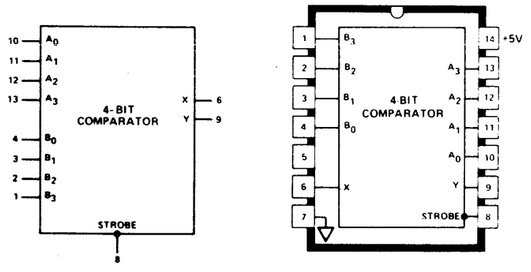


1820-0622
8-INPUT MULTIPLEXER



When the ENABLE line is false, the binary select lines 2^0 through 2^2 are used to select one of the eight inputs, lines D_0 through D_7, and apply it to the output lines Q and $\overline{Q}$.

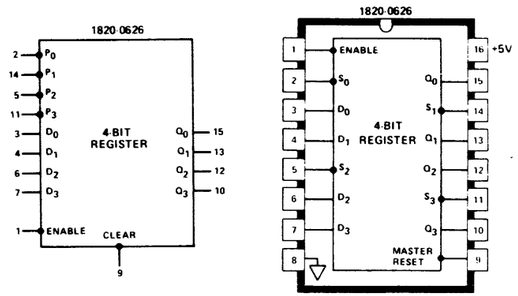
1820-0623
8-BIT COMPARATOR



When the STROBE line goes low the A bits are compared with the B bit. The result of the comparison is present on the output lines for the duration of the strobe. The output is decoded according to the truth table shown.

RELATION	X	Y
A > B	1	0
A < B	0	1
A = B	1	1

1820-0626
4-BIT REGISTER

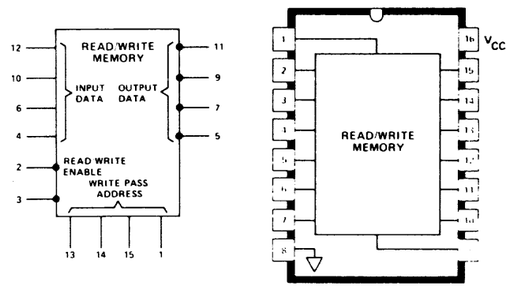


A low input on the ENABLE line allows data on the input lines to set the register. There are two modes of operation, one using the D input lines (most common) and the other using the P input lines.

If the D inputs are used the P inputs are held false. When the ENABLE line is low the register output lines will "follow" the D inputs. When the ENABLE line goes high the register will retain the last set of data inputs.

If the S inputs are used the D inputs are held true. When the ENABLE line is low, a false input on the S line will set the register bit. The register is then cleared by a low signal on the CLEAR line. The CLEAR line serves as a "master" register clear for both the D and S modes of operation.

1820-0628
READ/WRITE MEMORY



This 64-bit read/write memory, consisting of 64 flip-flops, provides 15 words of four bits each. The data outputs can be wire-"anded" to other integrated circuits of the same type to provide a memory of up to 4704 words. With output buffering, additional memory capacity is possible. Access time is typically 33 nanoseconds.

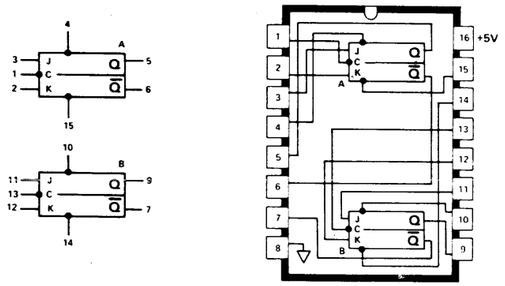
WRITE OPERATION. Information at the data inputs is written into the memory by addressing the desired location and maintaining pins 2 and 3 low. During this operation, the 1's complement of the input data is available at the output.

READ OPERATION (NON-DESTRUCTIVE). The 1's complement of the information written is obtained by addressing the desired location while holding pin 2 low.

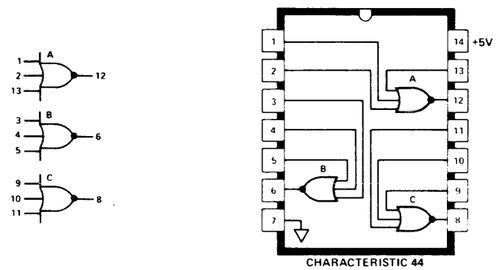
PASS-THROUGH OPERATION. With pin 3 low and pin 2 high, the 1's complement of the information at the data inputs is passed to the data outputs. No change is made to memory contents.

OPERATION	PIN 2	PIN 3	DATA OUTPUTS
Write	L	L	Complement of data inputs.
Read	L	H	Complement of addressed word.
Pass through	H	L	Complement of data inputs.
None	H	H	All high.

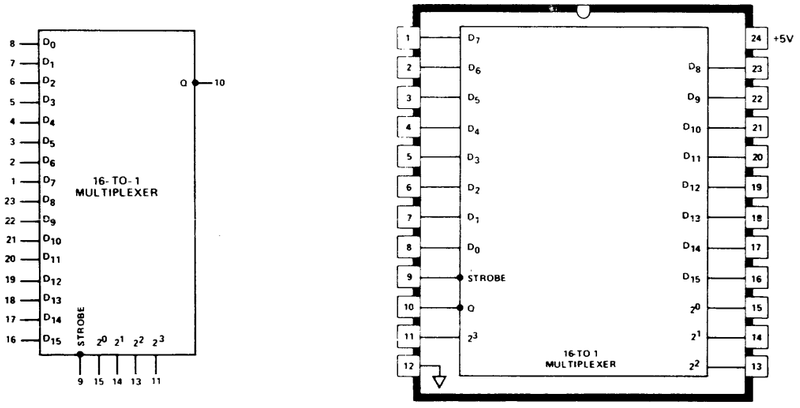
1820-0629
DUAL J-K FLIP FLOP



1820-0637
TRIPLE 3-INPUT NOR GATE

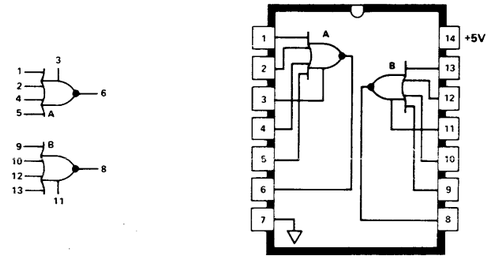


1820-0640
16-TO-1 MULTIPLEXER



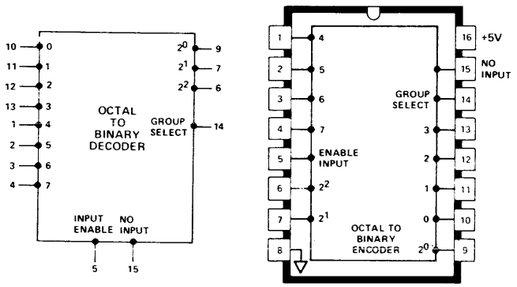
One of the 16 input data lines is selected by the select lines 2^0 - 2^3 . A low signal on the STROBE line causes the selected data line to be inverted and made available on the Q output.

1820-0655
DUAL 4-INPUT GATED NOR GATE



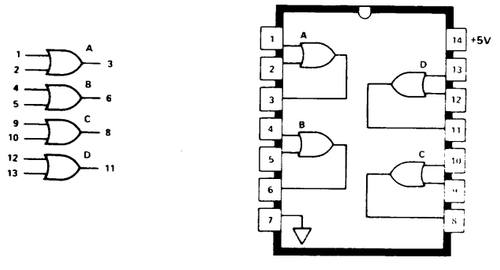
When the gate enable (strobe) is high and any gate input is high the gate output will go low.

1820-0657
OCTAL TO BINARY ENCODER

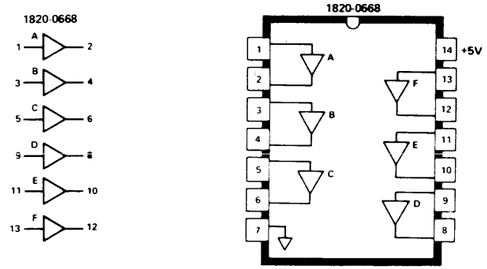


When the ENABLE INPUT line is low and one or more of the input lines 0-7 are low then the output lines making up the binary equivalent of the highest input lines will go low. When this occurs the GROUP SELECT output signals also goes low. If the INPUT ENABLE line is low and none of the input lines are selected (go low) then the NO INPUT line goes low. This allows the next stage of a decoder to be enabled.

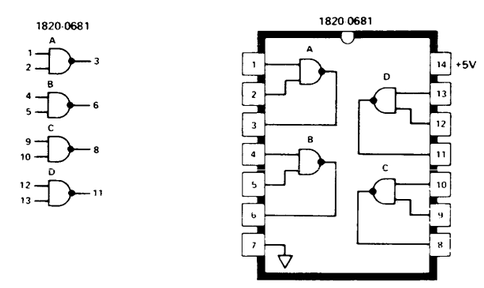
1820-0661
QUAD 2-INPUT OR GATE



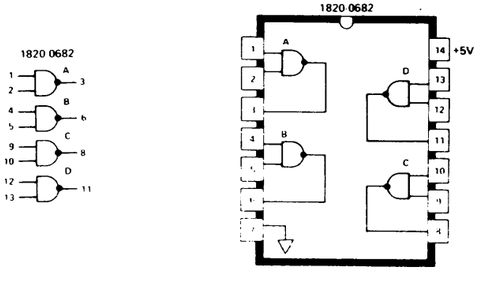
1820-0668
HEX DRIVER



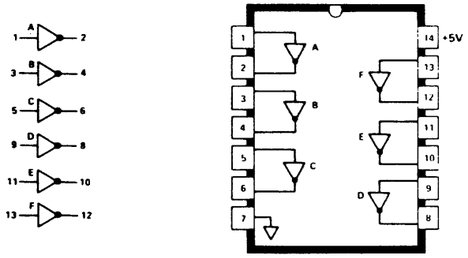
1820-0681
QUAD 2-INPUT NAND GATE



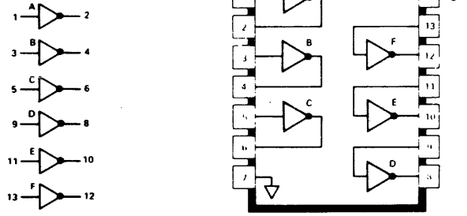
1820-0682
QUAD 2-INPUT NAND GATE



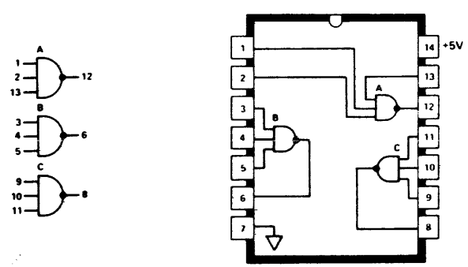
1820-0683
HEX INVERTER



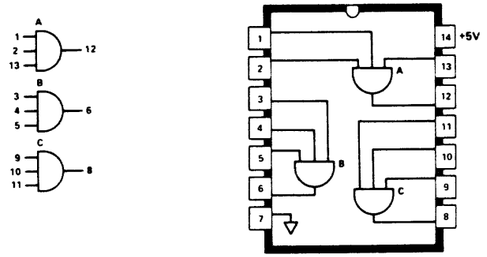
1820-0684
HEX INVERTER



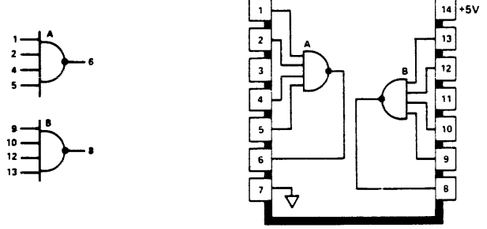
1820-0685
TRIPLE 3-INPUT NAND GATE



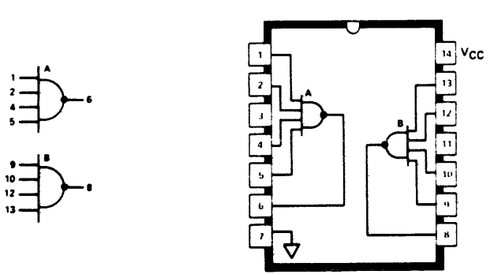
1820-0686
TRIPLE 3-INPUT AND GATE



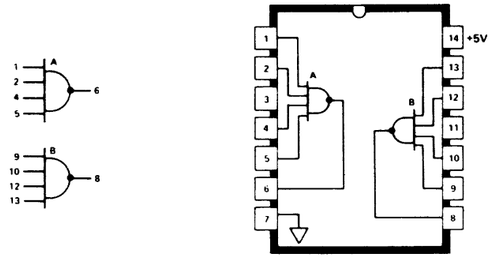
1820-0688
DUAL 4-INPUT NAND GATE



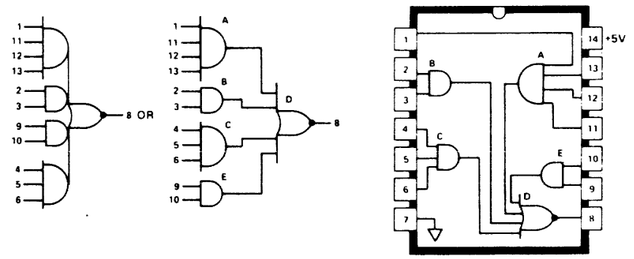
1820-0689
DUAL 4-INPUT NAND GATE



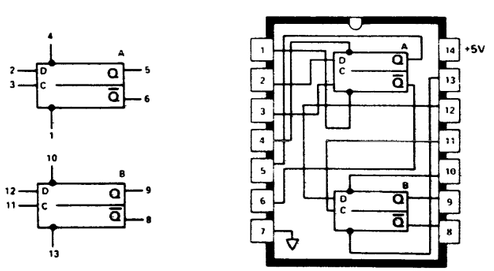
1820-0690
DUAL 4-INPUT NAND GATE



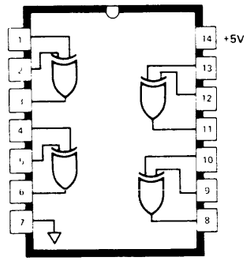
1820-0691
4-2-3-2 INPUT AND-NOR GATE



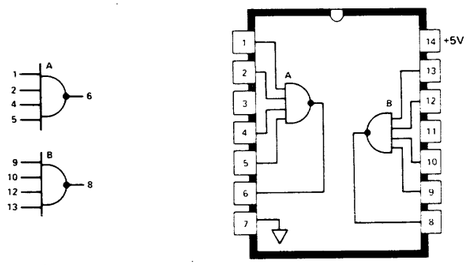
1820-0693
DUAL D FLIP-FLOP



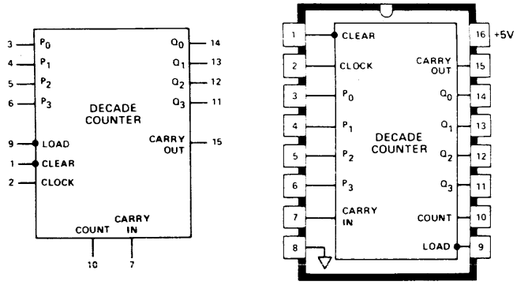
1820-0694
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE



1820-0697
DUAL 4-INPUT NAND GATE



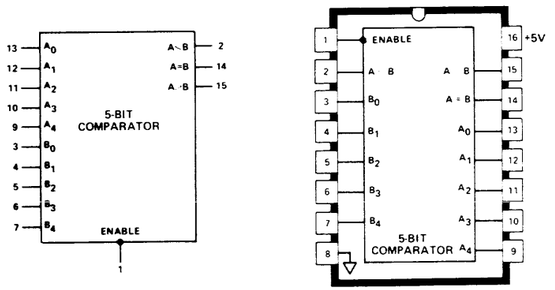
1820-0705
DECADE COUNTER



When the CLOCK input goes high and the LOAD line is low, data on the parallel input lines (P_0-P_3) is stored in the counter. When the CLOCK input goes high and both the COUNT and CARRY IN lines are high, the counter will be incremented. The new count will be present on the output lines (Q_0-Q_3) following the high-to-low transition of the clock.

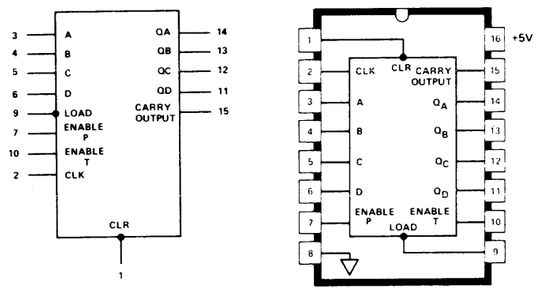
The CARRY OUT line will be high if the output lines Q_0-Q_3 equal nine (1001) and the CARRY IN line is high. The counter will be set to 0000 when the CLOCK line goes low.

1820-0706
5-BIT COMPARATOR



When the ENABLE line is low, input lines A_0 through A_4 are compared with B_0 through B_4. The appropriate output A > B, A = B, or A < B becomes true. The output remains unchanged until the ENABLE signal is removed or the input line signals changed.

1820-0713
4-BIT BINARY COUNTER

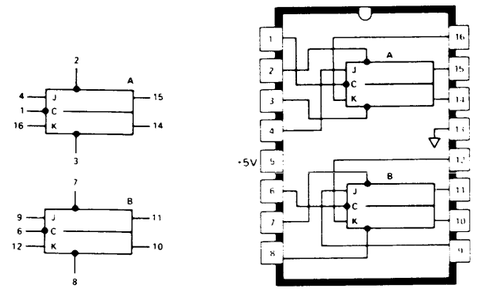


Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable inputs and internal gating. Clock inputs trigger the four flip-flops on the rising (positive-going) edge of the clock input.

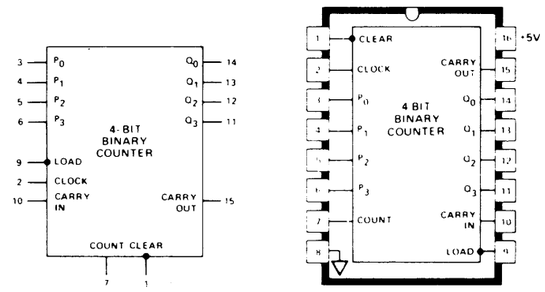
The counter is fully programmable. The outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function is synchronous and a low level at the clear input sets all four flip-flop outputs low after the next clock pulse, regardless of the levels of the enable inputs.

Both count-enable inputs (P and T) must be high to count, and the T input is fed forward to enable the carry output. The carry output, being enabled, will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output.

1820-0715
DUAL JK FLIP-FLOP



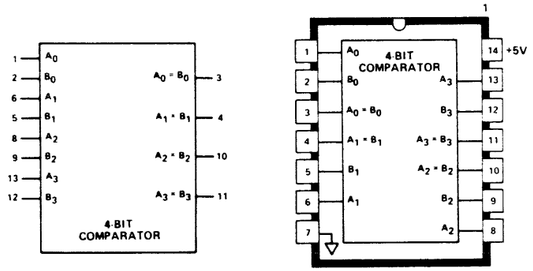
1820-0716
4-BIT BINARY COUNTER



When the CLOCK input goes high and the LOAD line is low, data on the parallel input lines (P_0-P_3) is stored in the counter. When the CLOCK input goes high and both the COUNT and CARRY IN lines are high, the counter will be incremented. The new count will be present on the output lines (Q_0-Q_3) following the high-to-low transition of the clock.

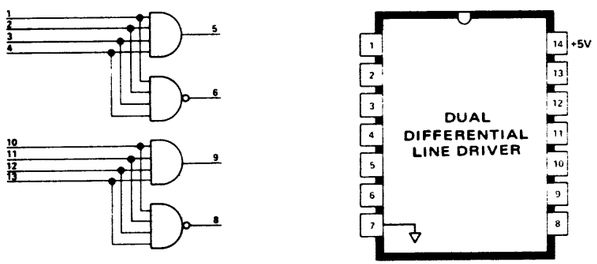
The CARRY OUT line will be high if the output lines Q_0-Q_3 are all high and the CARRY IN line is high.

1820-0719
4-BIT COMPARATOR



Four sets of two bits each are compared. If a set contains equal bits, the respective $A_i = B_i$ output line becomes true. The output line remains true until the input bit pattern is changed.

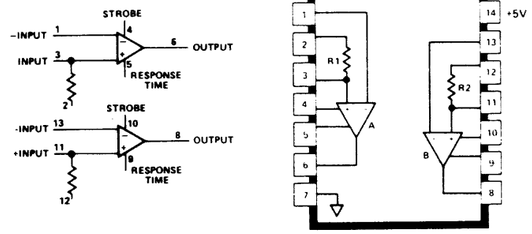
1820-0720
DUAL DIFFERENTIAL LINE DRIVER



The dual differential line driver also performs the dual four-input NAND or dual four-input AND function.

The differential outputs are balanced to drive long lengths of coax with characteristic impedances of 50 to 500 ohms.

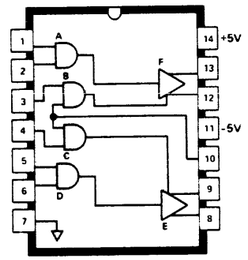
1820-0721
DUAL DIFFERENTIAL LINE RECEIVER



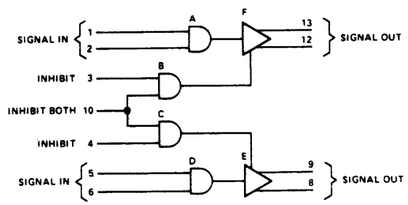
The dual differential line receiver receives inputs from twisted pair lines. The differential input rejects large common mode signals while responding to small differential signals.

Response time can be controlled with an external capacitor to reject input noise spikes. The output state is a logic 1 for both inputs open.

1820-0722
DUAL LINE DRIVER



This integrated circuit consists of two line drivers, each driving a line (such as twisted pair) and maintaining a nominal line current of 6 ma when the two wires in the line are at opposite logic levels. Output voltage levels are < 0.8 volts (low) and > 2.0 volts (high). When the line is isolated from ground the voltage across the line is at least 2.8 volts for the high-low or low-high state, and common-mode voltage (line to ground) can range from −3 volts to +10 volts. A low input to pin 3 or 4 allows either channel to be inhibited. A low input to pin 10 inhibits both channels.

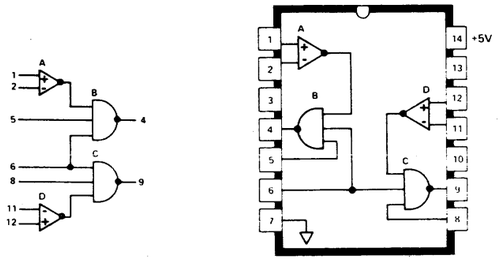


SIGNAL INPUTS		INHIBIT INPUTS		SIGNAL OUTPUTS	
PIN 1	PIN 2	PIN 3	PIN 10	PIN 13	PIN 12
X	X	L	X	H	H
X	X	X	L	H	H
L	Z	H	H	L	H
X	L	H	H	L	H
H	H	H	H	H	L

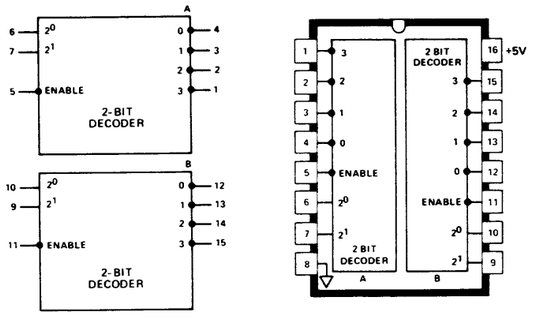
SIGNAL INPUTS		INHIBIT INPUTS		SIGNAL OUTPUTS	
PIN 5	PIN 6	PIN 4	PIN 10	PIN 9	PIN 8
X	X	L	X	H	H
X	X	X	L	H	H
L	X	H	H	L	H
X	L	H	H	H	L
H	H	H	H	L	H

X = irrelevant

1820-0723
DUAL LINE RECEIVER

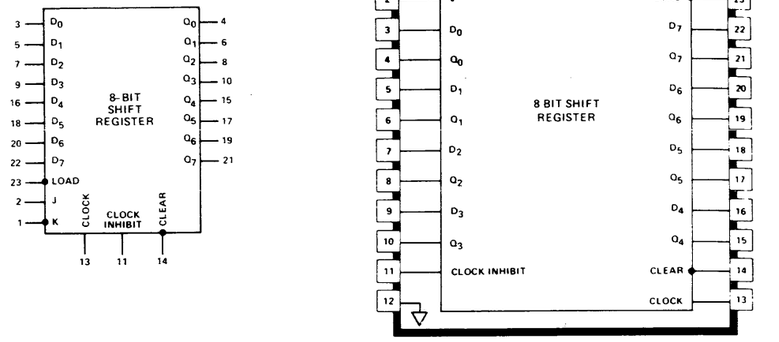


1820-0724
DUAL 2-BIT DECODER



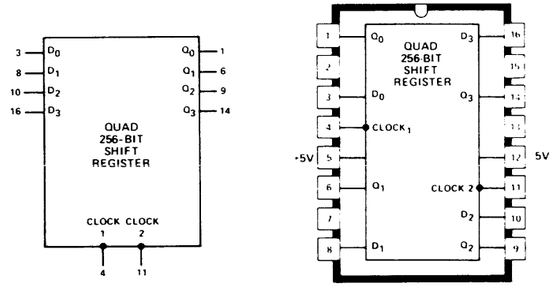
When the ENABLE line is low the input lines 2^0-2^1 select one of four output lines 0-4. The select line goes low.

1820-0726
8-BIT SHIFT REGISTER



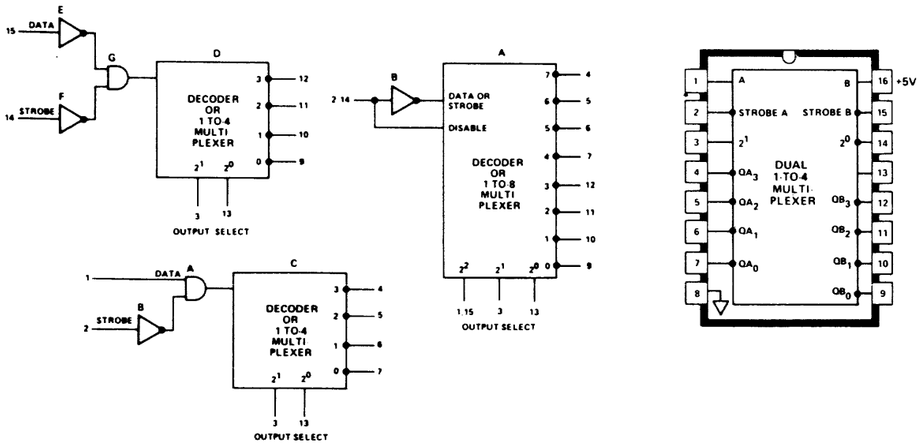
When the LOAD line is low data on the parallel input lines D_0-D_7 is loaded into the register. A low on the CLEAR line clears the register. The contents of the register are shifted one bit position (from D_0 to D_1 etc.) when the CLOCK INHIBIT line is low and a positive clock transition occurs. At this time the J and K inputs will be used to determine the next state of the D_0 bit position.

1820-0733
QUAD 256-BIT SHIFT REGISTER



Data on input lines D_0-D_3 is loaded into the register by a high to low transition of either the CLOCK1 or CLOCK2 line. The same clock signal shifts the contents of the register one position and presents the next output bits on the Q_0-Q_3 lines. The register is circular containing 256 4-bit words.

1820-0738
DUAL 2-TO-4 LINE DECODER/DEMULTIPLEXER



INPUT PINS				OUTPUT PINS			
3	13	2	1	7	6	5	4
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUT PINS				OUTPUT PINS			
3	13	14	15	9	10	11	12
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

USED AS DUAL 1 TO 4 MULTIPLEXER OR DUAL 2 BIT DECODER

INPUT PINS				OUTPUT PINS							
1,15	3	13	2,14	9	10	11	12	7	6	5	4
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

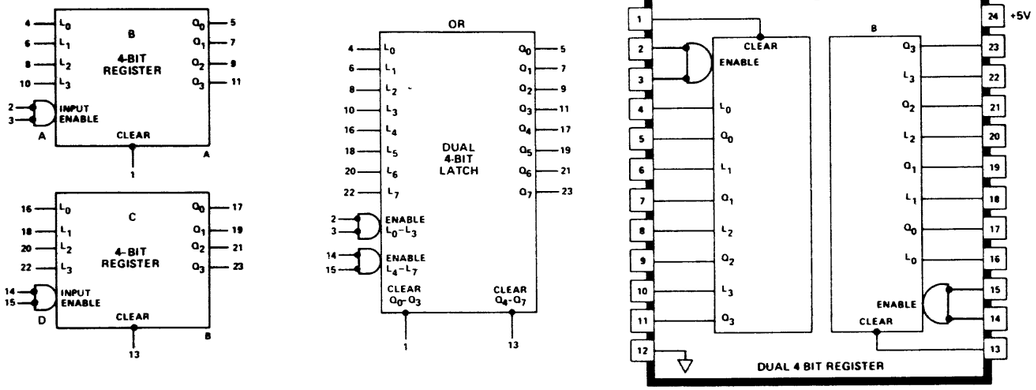
USED AS 1 TO 8 MULTIPLEXER OR 3 BIT DECODER

This integrated circuit can be used as a dual 1-to-4 multiplexer or dual 2-bit decoder. When used as a multiplexer, data supplied to pin 1 is inverted; data supplied to pin 15 is not inverted. The data and strobe inputs to pins 1 and 2 can be interchanged with a reversal of signal sense. The inputs to pins 15 and 14 also can be interchanged, with no change in signal sense. In decoder use, the output of gate A or gate G must be in the high state to enable the decoder.

By connecting pin 1 to pin 15, and pin 2 to 14, the integrated circuit may be used as a 1-to-8 multiplexer or 3-bit decoder.

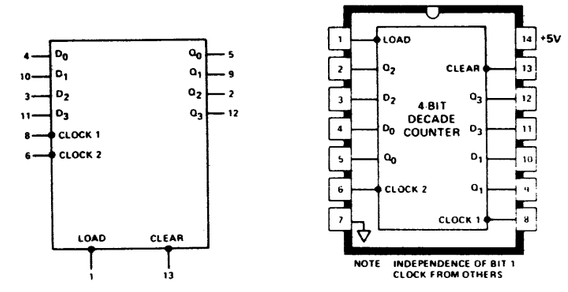
With the exception of the diagram showing physical position of pins, the diagrams above are simplified to show functional operation. An X in the tables indicates that the level is irrelevant.

1820-0742
DUAL 4-BIT LATCH



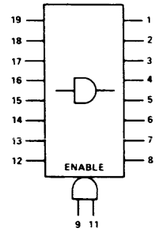
High inputs on both enable lines will cause the input data (L_0-L_3) to be stored in the register. The data is stored on the leading edge of the ENABLE signal. A low signal on the CLEAR line clears the register.

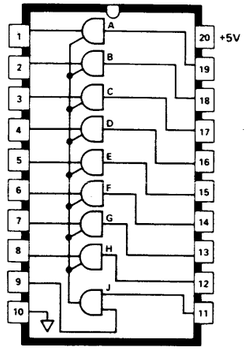
1820-0751
DECADE COUNTER



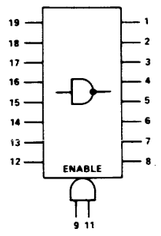
A low signal on the CLOCK1 line toggles the first bit of the counter. A low signal on the CLOCK2 line causes the remainder of the counter to be incremented (counting to 5). If the Q_0 output is used to provide the CLOCK2 input, the counter will act as a decade counter.

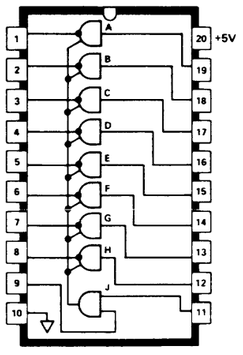
1820-0755
8-BIT DRIVER



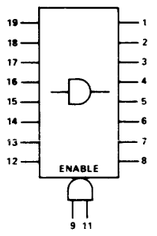


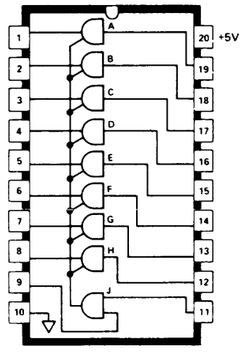
1820-0756
8-BIT DRIVER





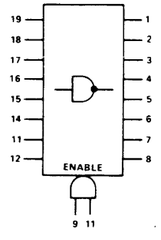
1820-0759
8-BIT RECEIVER

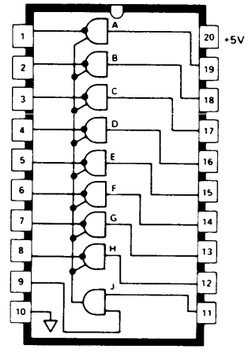




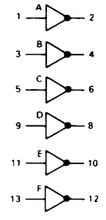
High signals on both enable lines gate the input data. The output data is inverted for 1820-0756 and 1820-0760.

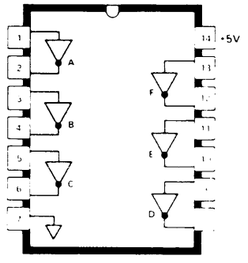
1820-0760
8-BIT RECEIVER



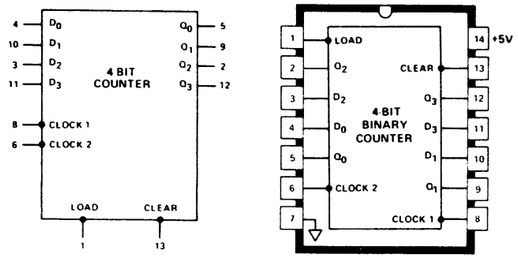


1820-0761
HEX INVERTER



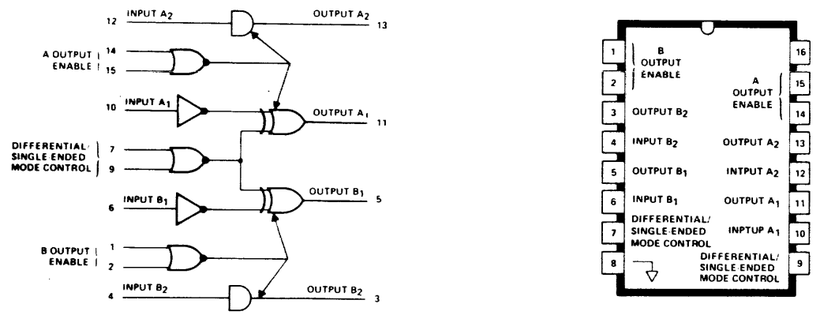


1820-0765
4-BIT COUNTER



A low signal on the LOAD line presets the counter with the data on the input lines D_0 through D_3. A low signal on the CLEAR line clears the counter. A low signal on the CLOCK1 line toggles the first bit of the counter. A low signal on the CLOCK2 line causes the remainder of the register to be incremented by one (counting to 7). If the Q_0 output is used to provide the CLOCK2 signal, the counter will act as a 4-bit binary counter.

1820-0780
QUAD TRI-LEVEL LINE DRIVER

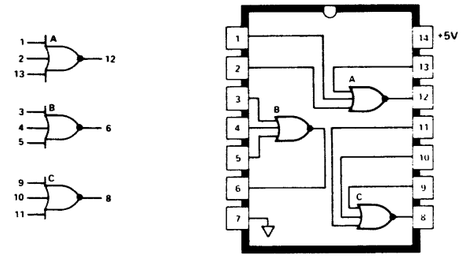


The quad tri-level line driver can be used as either a quad single-ended line driver or as a dual differential line driver.

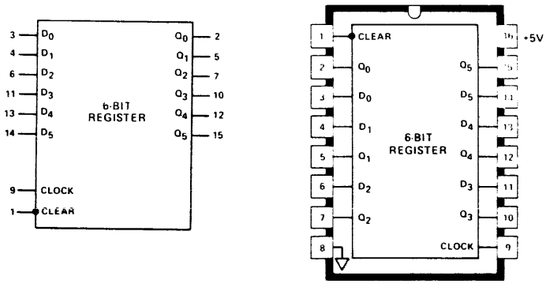
To operate as a quad single-ended line driver, a logic 0 is applied to the Output Enable pins to keep the outputs in the normal low impedance mode, and a logic 0 is applied to both Differential/Single-Ended Mode Control inputs. All four channels will then operate independently and no signal inversion will occur between inputs and outputs.

To operate as a dual differential line driver, logic 0 is applied to the Output Enable pins, and at least one logic 1 is applied to the Differential/Single-Ended Mode Control inputs. The inputs to the A channel are connected together and the inputs to the B channel are connected together. In this mode, signals applied to the resulting inputs will pass non-inverted on the A_2 and B_2 outputs, and inverted on the A_1 and B_1 outputs.

1820-0782
TRIPLE 3-INPUT NOR GATE

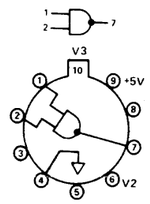


1820-0788
6-BIT REGISTER



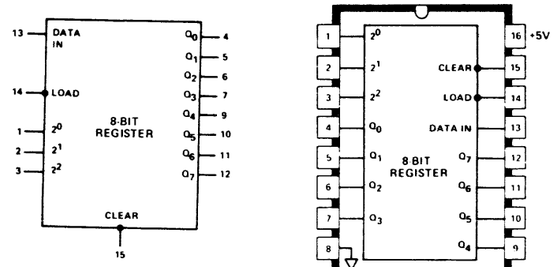
Data on the input lines is entered into the register by a positive going transition of the CLOCK line. The register is cleared by a low input on the CLEAR line.

1820-0832
TTL-TO-MOS TRANSLATOR/CLOCK DRIVER



Voltage references V2 and V3 determine the output signal level.

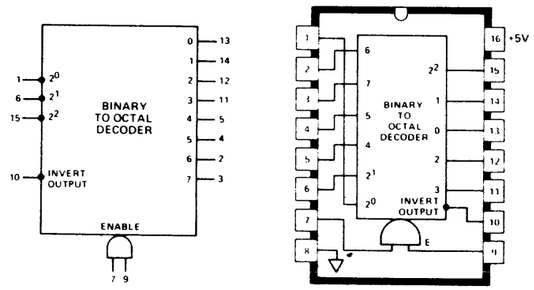
1820-0833
8-BIT REGISTER



When the LOAD line is low the information on the DATA IN line will be stored in the register position selected by the address lines (2^0-2^2). A low CLEAR signal together with a high LOAD signal will cause the register to be cleared.

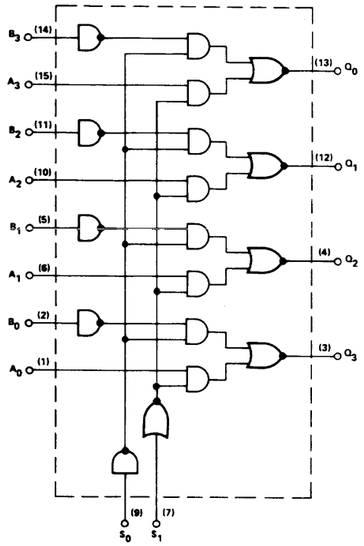
If both LOAD and CLEAR lines are low the register will act as a multiplexer, routing information on the DATA IN line to the output selected by the address lines.

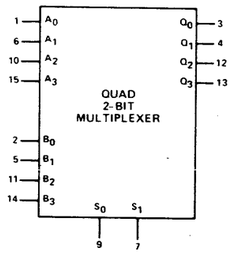
1820-0834
BINARY TO OCTAL DECODER

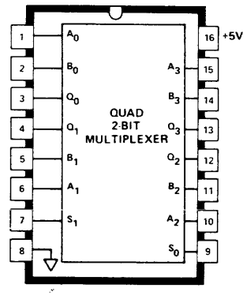


When both enable inputs are high the binary code inputs (2^0-2^2) are decoded. The equivalent octal output (0-7) will go high or low if the INVERT input is high or low respectively.

1820-0835
2-INPUT 4-BIT MULTIPLEXER



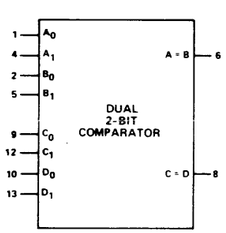




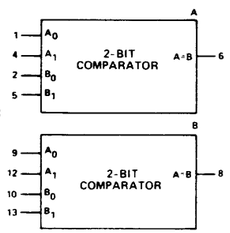
Input data (A_0-A_3 or B_0-B_3) is routed to the output lines (Q_0-Q_3) according to the table given below.

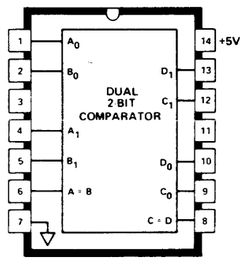
SELECT LINES		OUTPUT
S_0	S_1	Q_N (1,2,3,4)
0	0	B_N
0	1	B_N
1	0	$\overline{A}_N$
1	1	1

1820-0836
DUAL 2-BIT COMPARATOR



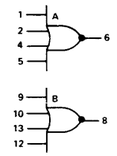
OR

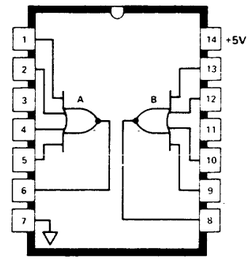




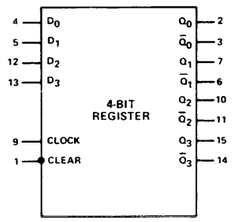
If the input bits A_0 and A_1 compare with the input bits B_0 and B_1 then the output line A=B will go high. Similarly for C and D bits.

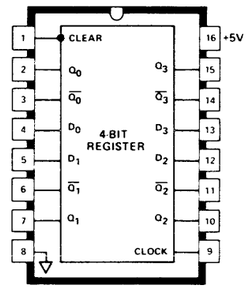
1820-0837
DUAL 4-INPUT NOR GATE





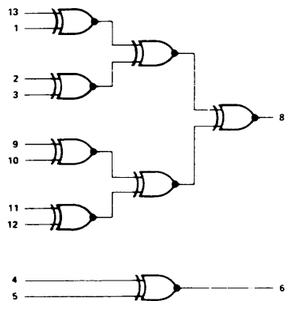
1820-0839
4-BIT REGISTER

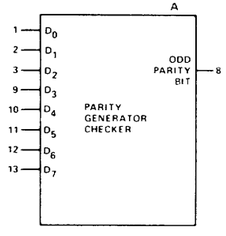


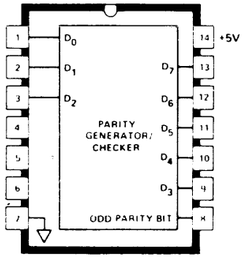


Data on the input lines (D_0-D_3) is stored at the low-to-high transition of the CLOCK line. A low signal on the CLEAR line will clear the register.

1820-0842
PARITY GENERATOR/CHECKER

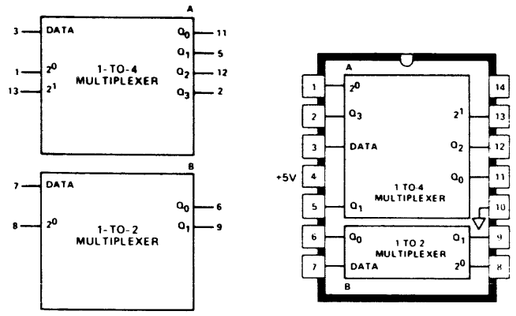






Pin 8 will be high as long as the high state is present on an even number of D inputs.

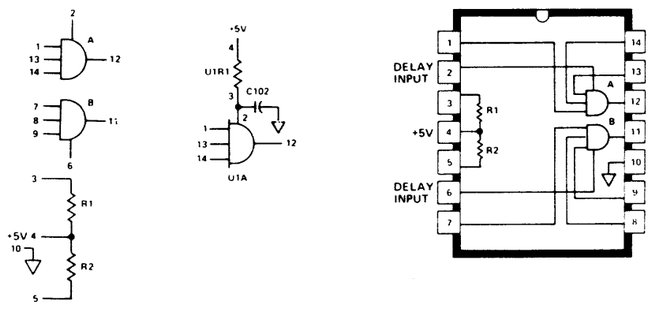
1820-0843
DUAL DATA DISTRIBUTOR



Element A multiplexes data on the DATA line to one of four output lines Q_0-Q_3. The output line is selected by the select lines 2^0 and 2^1.

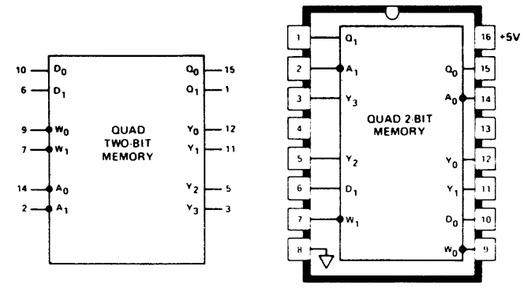
Element B multiplexes the data on the input line to one of the two output lines Q_0-Q_1. The output line is selected by the 2^0 select line.

1820-0844
DUAL 3-INPUT PULSE SHIFT/DELAY AND GATE



The outputs of the gates are delayed by an amount determined by an external RC network.

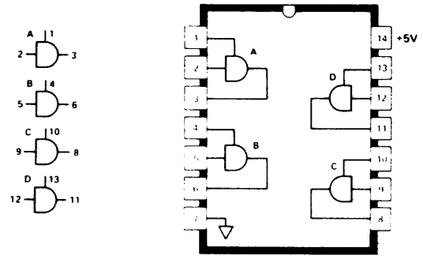
1820-0845
QUAD 2-BIT MEMORY



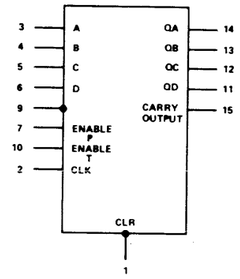
The memory is loaded by selecting the desired address with the W_0 and W_1 lines. Data present on the input lines D_0 and D_1 is then stored in the addressed word.

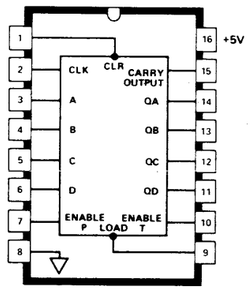
A word is read from memory by addressing the word with the A_0 and A_1 lines. The word content is then output to the Q_0 and Q_1 lines.

1820-0846
QUAD BUFFER



1820-0899
DECADE COUNTER



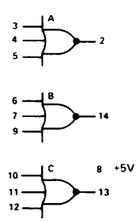


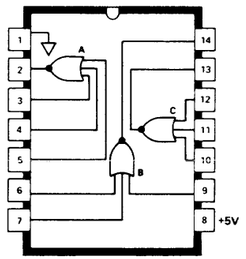
Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when instructed by the count-enable inputs and internal gating. Clock inputs trigger the four flip-flops on the rising (positive-going) edge of the clock input.

The counter is fully programmable. The outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the enable inputs.

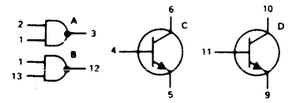
Both count-enable inputs (P and T) must be high to count, and the T input is fed forward to enable the carry output. The carry output, being enabled, will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output.

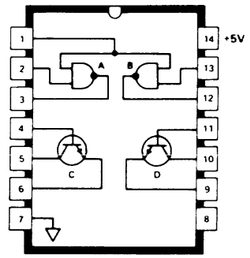
1820-0900
TRIPLE 3-INPUT NOR GATE



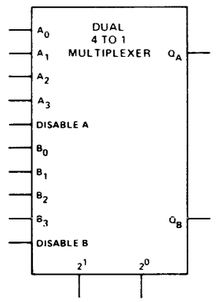


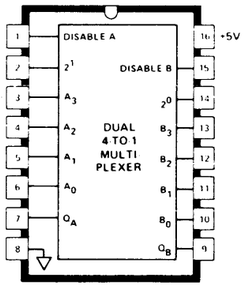
1820-0902
DUAL 2-INPUT DRIVER





1820-0906
DUAL 4-INPUT MULTIPLEXER



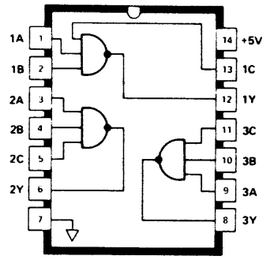


The multiplexer allows one of four bits to be placed at the output terminal. The data bits are placed on the input lines prior to the multiplexing operation. The code for the desired bit is then placed on the select lines (refer to the table above). The strobe line is used to gate the data bit onto the appropriate output line (A inputs to the Q_A terminal etc.).

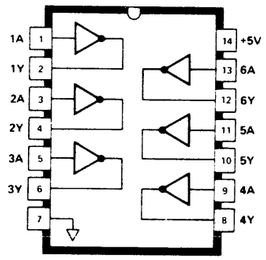
SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
2^1	2^0	A0	A1	A2	A3	A	QA
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Select inputs S_0 and S_1 are common to both sections.
X = irrelevant

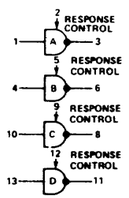
1820-0907
TRIPLE 3-INPUT POSITIVE-NAND GATE

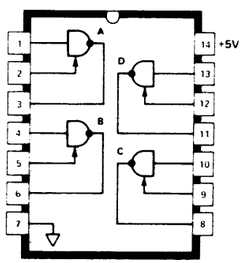


1820-0921
HEX INVERTER



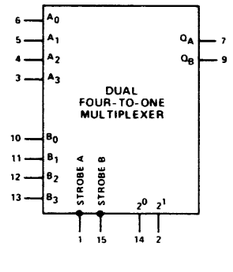
1820-0990
QUAD NAND LINE RECEIVER

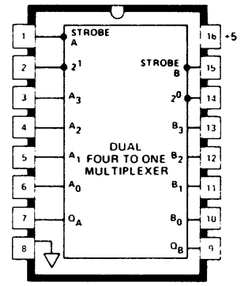




Each receiver section has an external response control input that permits the connection of an external resistor to control the threshold voltage level.

1820-0998
DUAL 4-TO-1 MULTIPLEXER



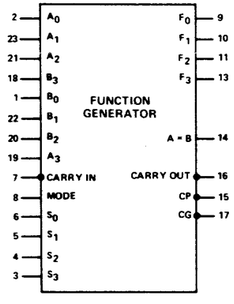


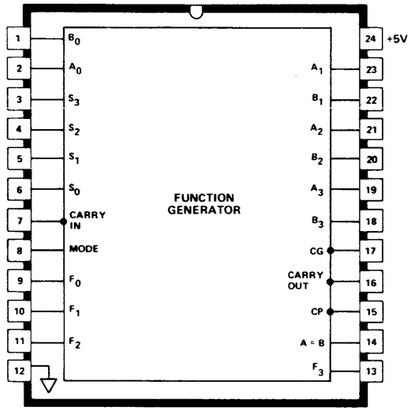
Each part of the 1820-0998 multiplexer allows one of four bits to be placed at the output terminal. The data bits are placed on the input lines prior to the multiplexing operation. The code for the desired bit is then placed on the select lines (refer to the table above). The strobe line is used to gate the data bit onto the appropriate output line (A inputs to the Q_A terminal etc.).

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
2^1	2^0	A0	A1	A2	A3	A	QA
X	X	X	X	X	X	1	0
0	0	0	X	X	X	0	0
0	0	1	X	X	X	0	1
0	1	X	0	X	X	0	0
0	1	X	1	X	X	0	1
1	0	X	X	0	X	0	0
1	0	X	X	1	X	0	1
1	1	X	X	X	0	0	0
1	1	X	X	X	1	0	1

Select inputs S_0 and S_1 are common to both sections.
X = irrelevant

1820-0999
FUNCTION GENERATOR





The MODE line determines whether an arithmetic or logic operation will be performed (A "1" for logic function and a "0" for arithmetic function). The S lines select the function to be performed according to the table given above. If the function code LHHL is used and the A inputs are the same as the B inputs the A = B output line will be true.

The CP (Carry Propagate) and CG (Carry Generate) lines are used for the fast addition operations using a "look ahead" carry function. The CP line will go false when the following conditions are met:

$$CP = F_0 \cdot F_1 \cdot F_2 \cdot F_3$$

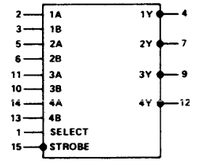
If the CARRY IN line is false and the CP condition is met, then the CARRY OUT line will also go false.

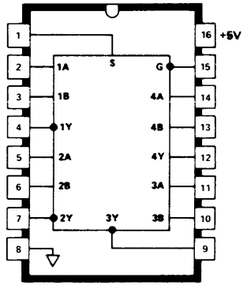
The CG line will go false if the pack addition results in a true CARRY OUT independant of the CARRY IN. The CG signal is defined as follows:

$$CG = A_3 \cdot B_3 + (A_2 \cdot B_2)(A_3 + B_3) + (A_1 \cdot B_1)(A_2 + B_2)(A_3 + B_3) + (A_0 \cdot B_0)(A_1 + B_1)(A_2 + B_2)(A_3 + B_3)$$

FUNCTION SELECT				OUTPUT FUNCTION	
S3	S2	S1	S0	LOGIC FUNCTIONS	ARITHMETIC OPERATIONS
L	L	L	L	$F = \overline{A}$	F = A
L	L	L	H	$F = \overline{A+B}$	F = A+B
L	L	H	L	$F = \overline{A}B$	F = A+B
L	L	H	H	F = Logical 0	F = minus 1 (2's complement)
L	H	L	L	$F = \overline{AB}$	F = A plus $\overline{AB}$
L	H	L	H	$F = \overline{B}$	F = [A+B] plus $\overline{AB}$
L	H	H	L	$F = A \oplus B$	F = A minus B minus 1
L	H	H	H	$F = A\overline{B}$	F = $A\overline{B}$ minus 1
H	L	L	L	$F = \overline{A}+B$	F = A plus AB
H	L	L	H	$F = \overline{A \oplus B}$	F = A plus B
H	L	H	L	F = B	F = [A+$\overline{B}$] plus AB
H	L	H	H	F = AB	F = AB minus 1
H	H	L	L	F = Logical 1	F = A plus A 1
H	H	L	H	F = A+$\overline{B}$	F = [A+B] plus A
H	H	H	L	F = A+B	F = [A+$\overline{B}$] plus A
H	H	H	H	F = A	F = A minus 1

1820-1015
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS



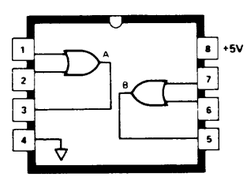


positive logic:
Low level at S selects A inputs
High level at S selects B inputs

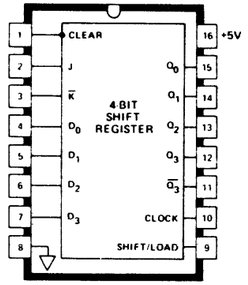
INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

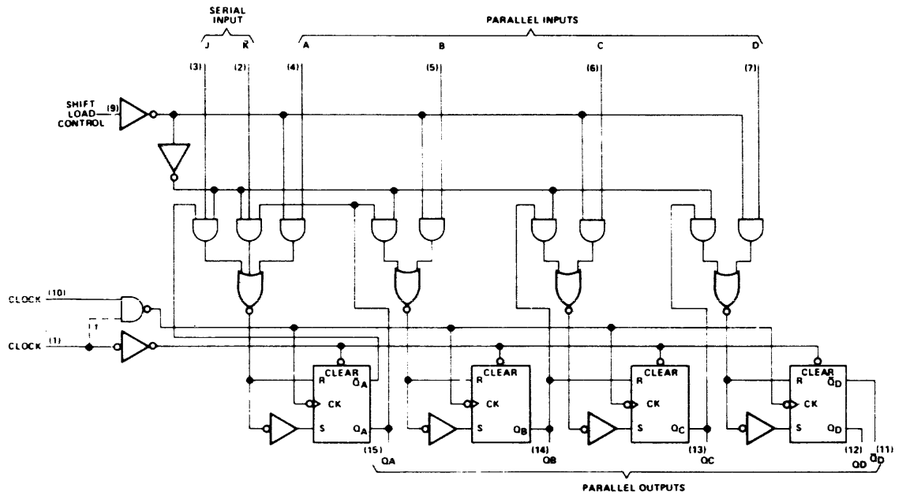
H = high level, L = low level, X = irrelevant

1820-1016
DUAL 2-INPUT OR GATE



1820-1027
4-BIT SHIFT REGISTER





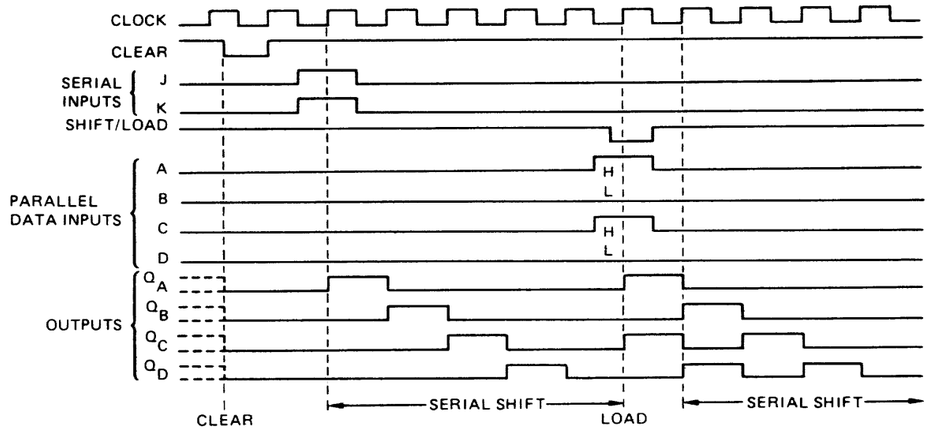
The 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel Load
Serial shift

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. Serial data flow is inhibited during loading.

Shifting is accomplished when the shift/load control input is high. Serial data is entered at the J-K inputs. These inputs permit the first stage to perform as a J-K, D-, or T-type flip-flop as shown in the function table.

1820-1027
4 BIT SHIFT REGISTER (CONTINUED)

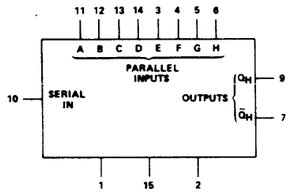


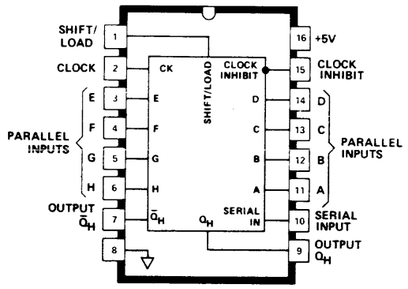
FUNCTION TABLE

INPUTS									OUTPUTS				
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q_A	Q_B	Q_C	Q_D	Q_D
			J	K	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	d
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	H	↑	H	L	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

H = High level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at A, B, C, or D, respectively
Q_{A0}, Q_{B0}, Q_{C0}, Q_{D0} = the level of Q_A, Q_B, Q_C or Q_D, respectively, before the indicated steady-state input conditions were established
Q_{An}, Q_{Bn}, Q_{Cn} = the level of Q_A, Q_B, or Q_C, respectively, before the most-recent transition of the clock

1820-1042
PARALLEL-LOAD 8-BIT SHIFT REGISTER WITH COMPLEMENTARY OUTPUT





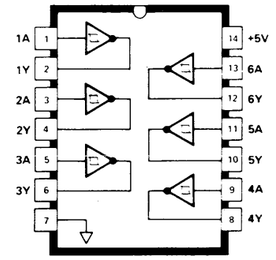
The 8-bit serial shift registers which shift the data in the direction of Q_A toward Q_H when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift-load input. The register has gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. Data at the parallel inputs are loaded directly into the register on a high-to-low transition of the shift-load input independently of the levels of the clock, clock inhibit, or serial inputs.

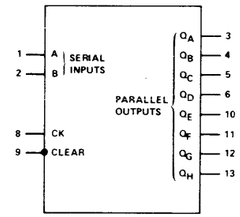
INPUTS					INTERNAL OUTPUTS		OUTPUT
SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	Q_A	$\overline{Q}_B$	Q_H
L	X	X	X	a...h	a	b	h
H	L	L	X	X	Q_{AO}	Q_{BO}	Q_{HO}
H	L	↑	H	X	H	Q_{AN}	Q_{Gn}
H	L	↑	L	X	L	Q_{AN}	Q_{Gn}
H	H	↑	X	X	Q_{AO}	Q_{BO}	Q_{HO}

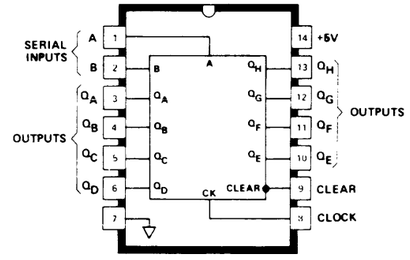
H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A thru H, respectively.
Q_{A0},Q_{B0},Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An},Q_{Gn} = the level of Q_A or Q_G, respectively, before the most-recent ↑ transition of the clock.

1820-1053
HEX SCHMITT-TRIGGER INVERTERS (PULSE SHAPING)



1820-1064
8-BIT PARALLEL-OUT SERIAL SHIFT REGISTER



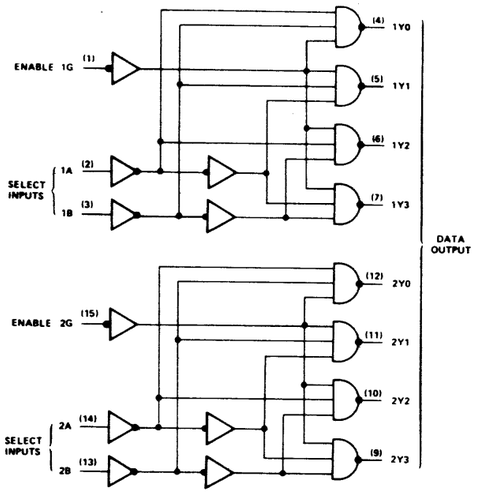


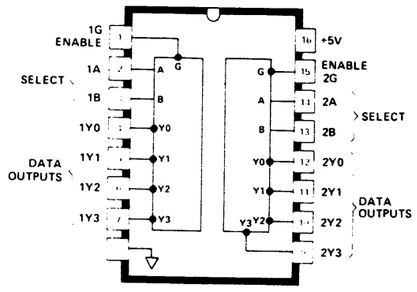
The 8-bit shift register has gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data. A low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
Q_{AO}, Q_{BO},Q_{HO} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

1820-1072
DECODER/MULTIPLEXER



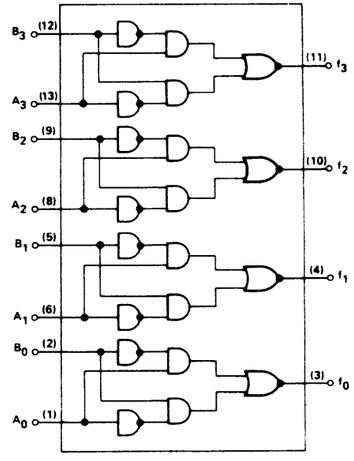


The decoder/demultiplexer consists of two individual two-line to four-line decoders in a single package.

INPUTS			OUTPUTS			
ENABLE	SELECT					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

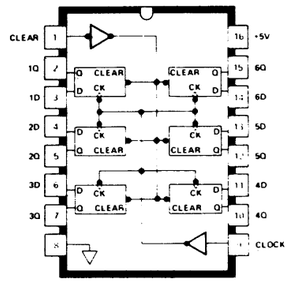
H = high level, L = low level, X = irrelevant

1820-1073
4-BIT QUAD EXCLUSIVE-NOR



+5V = (14), GND = (7), ( ) = Denotes Pin Numbers

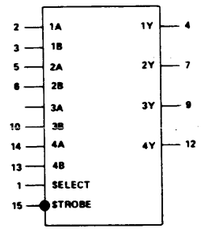
1820-1076
HEX D-TYPE FLIP-FLOPS WITH CLEAR

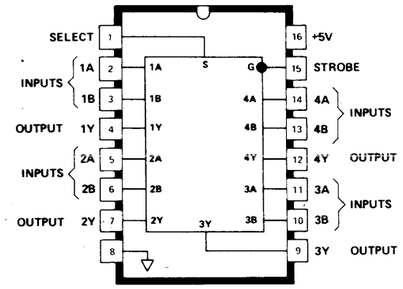


FUNCTION TABLE
(EACH FLIP FLOP)

INPUTS			OUTPUTS
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

1820-1077
QUADRUPLE 2-LINE-TO-1-LINE DATA SELECTORS/MULTIPLEXERS



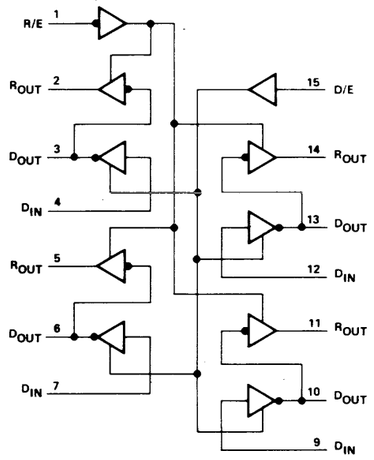


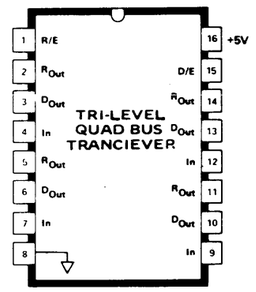
INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	H
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = High Level, L = Low Level, X = Irrelevant

positive logic:
Low level at S selects A inputs
High level at S selects B inputs

1820-1081
TRI-LEVEL QUAD BUS TRANSCEIVER



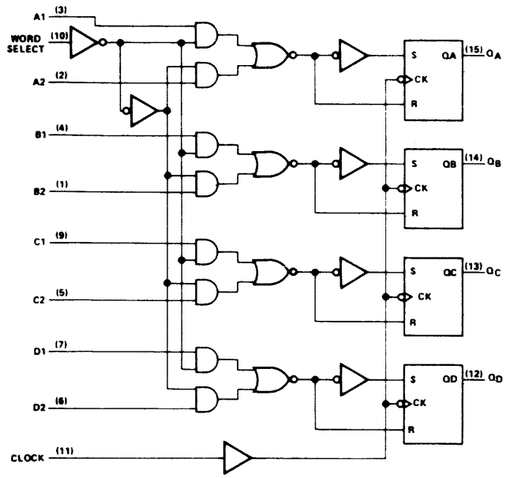


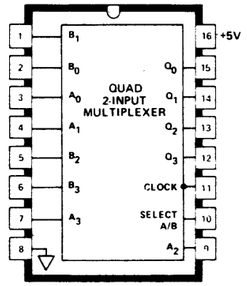
The Tri-Level Quad Bus Receiver consists of four pairs of tri-level logic elements configured as Quad Bus Drivers/ Receivers along with separate buffered receiver enable and driver enable lines.

A logic "1" on the Data Enable (D/E) inut allows input data to be transferred to the outputs of the Drivers while a logic "0" will force the outputs to a high impedance state.

The Receiver gates are enabled by a logic "0" on the Receiver Enable (R/E) pin. A logic "1" forces the Receiver outputs to a high impedance state and disables the inputs.

1820-1100
QUAD 2-INPUT MULTIPLEXER





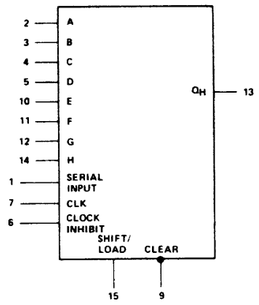
When the word-select input is low, word 1 (A1, B1, C1, D1) is applied to the flip-flops. A high input to word select will cause the selection of word 2 (A2, B2, C2, D2). The selected word is clocked to the output terminals on the negative-going edge of the clock pulse.

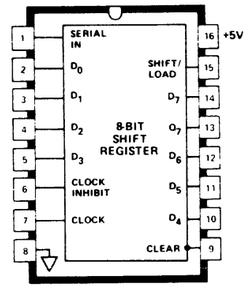
FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q_A	Q_B	Q_C	Q_D
L	↓	a1	b1	c1	d1
H	↓	a2	b2	c2	d2
X	H	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

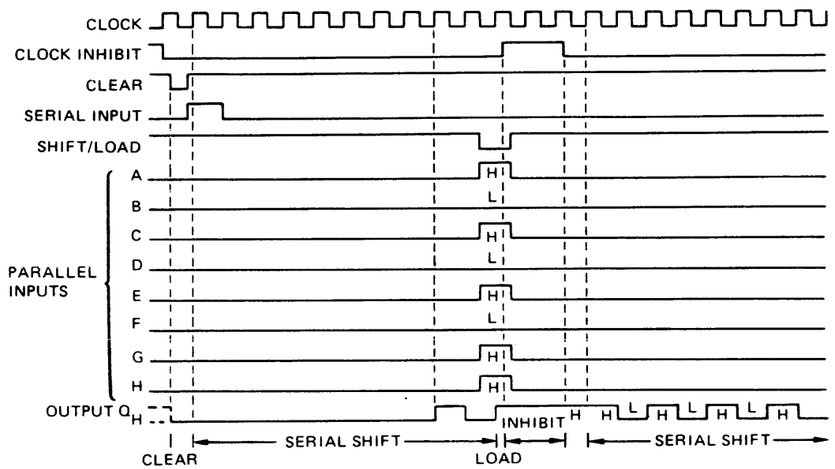
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↓ = transition from high to low level
a1, a2, etc. = the level of steady-state input at A1, A2, etc.
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered on the most-recent ↓ transition of the clock input.

1820-1107
8-BIT SHIFT REGISTER





The parallel or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the register for serial shifting with each clock pulse. When low, the parallel data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high level edge of the clock pulse. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. A direct clear input overrides all other inputs, including the clock, and sets the register to zero.

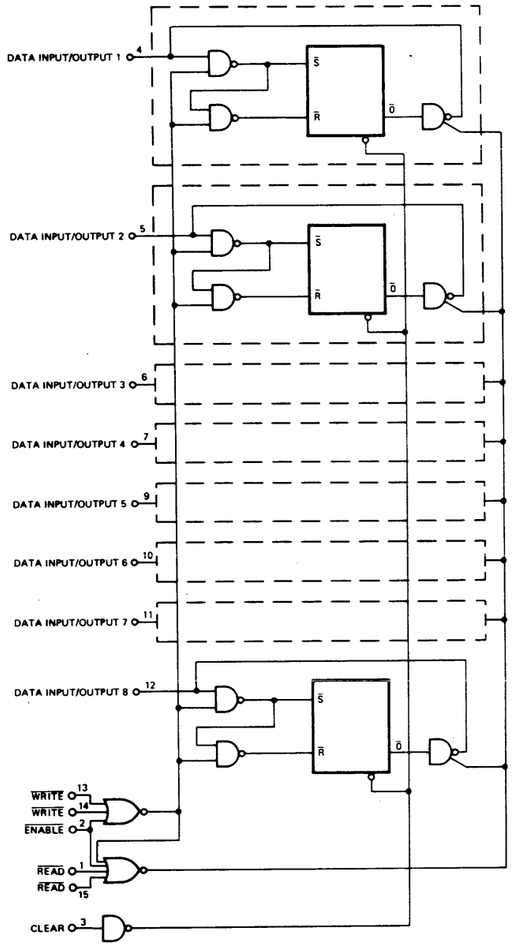


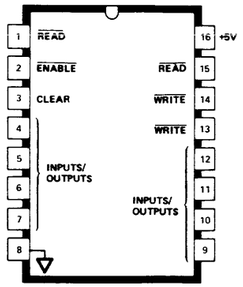
FUNCTION TABLE

INPUTS						INTERNAL OUTPUTS		OUTPUT
CLEAR	SHIFT/ LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A . . . H	Q_A	Q_B	Q_H
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	L	L	↑	X	a . . . h	a	b	h
H	H	L	↑	H	X	H	Q_{An}	Q_{Gn}
H	H	L	↑	L	X	L	Q_{An}	Q_{Gn}
H	X	H	↑	X	X	Q_{A0}	Q_{B0}	Q_{H0}

H = high level (steady-state)
L = low level (steady-state)
X = Irrelevant (any input, including transitions)
↑ = transition from low to high level
a . . . h = the level of steady-state input at inputs A through H, respectively.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_3, respectively, before the most-recent ↑ transition of the clock.

1820-1113
TRI-LEVEL 8-BIT LATCH



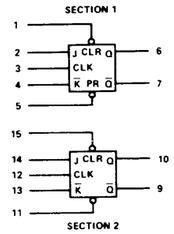


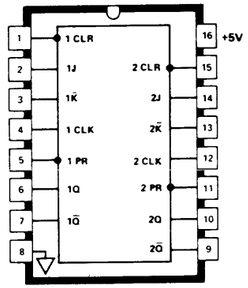
TRUTH TABLE

CLEAR	ENABLE	READ	WRITE	I/O STATE
1	0	0	x	Output = 0
x	x	1	1	Hi-Z
0	0	x	0	Write
0	0	0	1	Read

Inputs and outputs are accessed on the same leads of the tri-level 8-bit latch. When in the high impedance state, the outputs and inputs are disabled and no information can be entered. When the outputs are active, the gating associated with each latch prevents information from being entered. Outputs are disabled while information is entered.

1820-1116
DUAL J-K POSITIVE EDGE TRIGGERED FLIP-FLOP

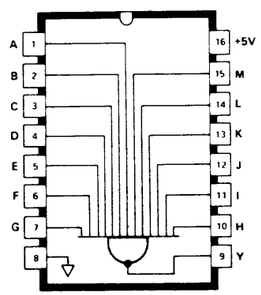




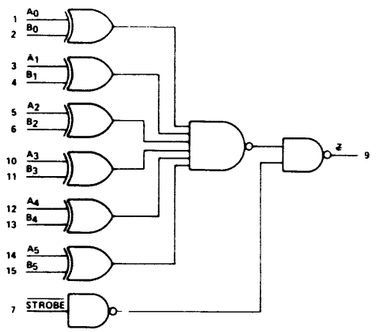
FUNCTION TABLE

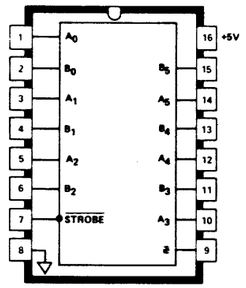
INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	Q_0
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	Q_0

1820-1130
13-INPUT POSITIVE-NAND GATE



1820-1131
6-BIT COMPARATOR

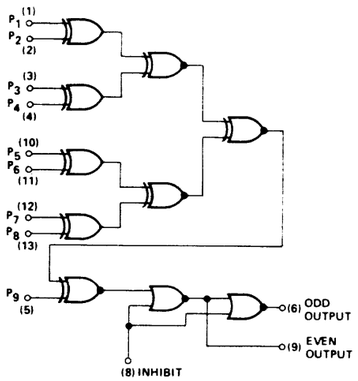


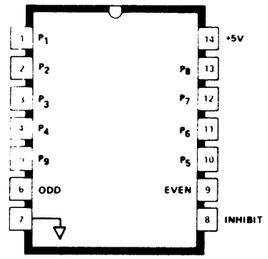


The comparator determines equality or non-equality between two 6-bit words. A strobe over-ride, when a logic 1, will force the output to a logical 1.

CONDITION	$\overline{\text{STROBE}}$ S	Z
A = B, A ≠ B	1	1
A = B	0	0
A ≠ B	0	0

1820-1140
9-BIT PARITY GENERATOR AND CHECKER





LOGIC EQUATIONS:

ODD OUTPUT = $P_1 * P_2 * P_3 * P_4 * P_5 * P_6 * P_7 * P_8 * P_9$

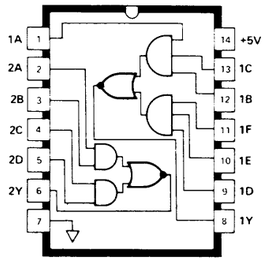
EVEN OUTPUT = $\overline{P_1 * P_2 * P_3 * P_4 * P_5 * P_6 * P_7 * P_8 * P_9}$

The 9-Input Parity Generator/Parity Checker is used to detect errors in data transmission or in data retrieval. Two outputs (EVEN and ODD) are provided for versatility. An INHIBIT input is provided to disable both outputs. (A logic 1 on the INHIBIT input forces both outputs to a logic 0.)

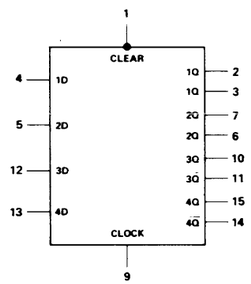
When used as a Parity Generator, the generator supplies a parity bit which is transmitted together with the data word.

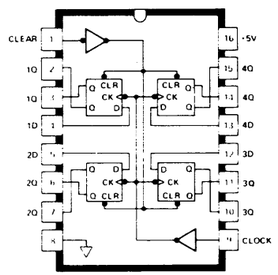
At the receiving end, the device acts as a Parity Checker and indicates that data has been received correctly or that an error has been detected.

1820-1158
2 WIDE 2-INPUT AND 3-INPUT AND-OR-INVERT GATES



1820-1191
QUADRUPLE D-TYPE FLIP-FLOPS WITH CLEAR

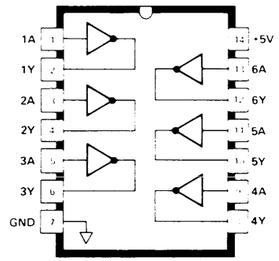




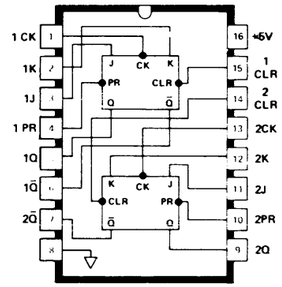
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\overline{Q}$↑
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q_0}$

H = high logic level (steady state)
L = low logic level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = The level of Q before the indicated steady-state input conditions were established

1820-1199
HEX INVERTER



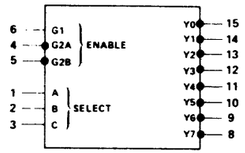
1820-1212
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

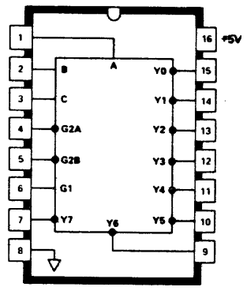


INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	$\overline{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\overline{Q}_0$

H = high level (steady state), L = low level (steady state),
X = irrelevant, ↓ = transition from high to low level
Q_0 = the level of Q before the indicated input conditions were established.
TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

1820-1216
DECODER/DEMULTIPLEXER

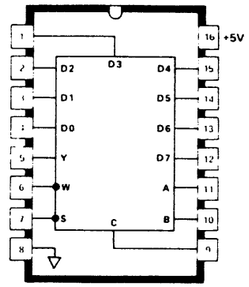


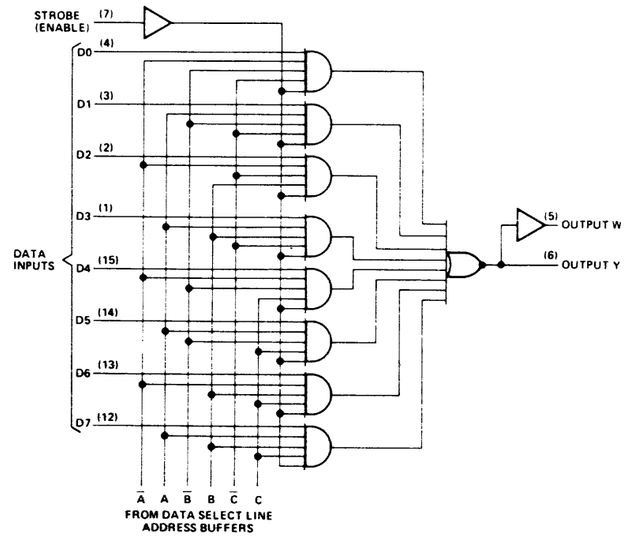


INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

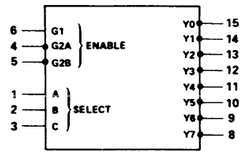
1820-1217
8-INPUT MULTIPLEXER WITH COMPLEMENTARY OUTPUTS

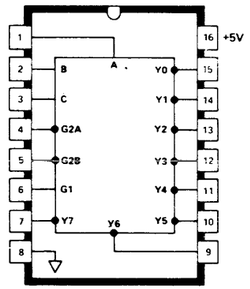




INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

1820-1240
DECODER/DEMULTIPLEXER

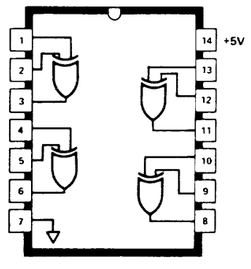




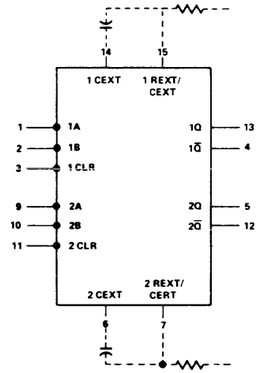
INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

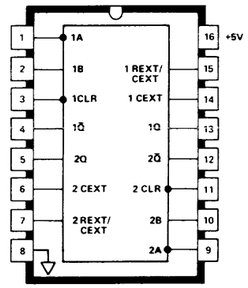
*G2 = G2A + G2B
H = high level, L = low level, X = irrelevant

1820-1250
QUAD 2-INPUT EXCLUSIVE OR GATE



1820-1260
DUAL MULTIVIBRATOR





Each multivibrator features a negative transition triggered input and a positive transition triggered input. Either input can be used as an inhibit input.

Output pulse width is determined by external component values. Approx. pulse width = 0.7 X RC.

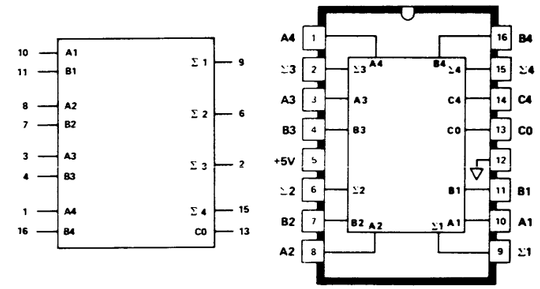
FUNCTION TABLE
(EACH MONOSTABLE)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎

Also see description and switching characteristics

H = high level (steady state)
L = low level (steady state)
↑ = transition from low to high level
↓ = transition from high to low level
⎍ = one high level pulse
⎎ = one low level pulse
X = irrelevant

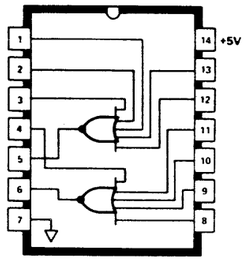
1820-1261
4-BIT BINARY FULL ADDER



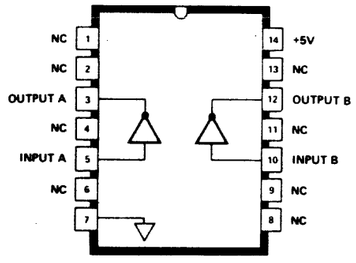
INPUT				OUTPUT					
				WHEN C0 = L			WHEN C0 = H		
				WHEN C2 = L			WHEN C2 = H		
A1 / A3	B1 / B3	A2 / A4	B2 / B4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4	Σ1 / Σ3	Σ2 / Σ4	C2 / C4
L	L	L	L	L	L	L	H	L	L
H	L	L	L	H	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L
H	H	L	L	L	H	L	H	H	L
L	L	H	L	L	H	L	H	H	L
H	L	H	L	H	H	L	L	L	H
L	H	H	L	H	H	L	L	L	H
H	H	H	L	L	L	H	H	L	H
L	L	L	H	L	H	L	H	H	L
H	L	L	H	H	H	L	L	L	H
L	H	L	H	H	H	L	L	L	H
H	H	L	H	L	L	H	H	L	H
L	L	H	H	L	L	H	H	L	H
H	L	H	H	H	L	H	L	H	H
L	H	H	H	H	L	H	L	H	H
H	H	H	H	L	H	H	H	H	H

H = high level, L = low level
NOTE: Input conditions at A1, B1, A2, B2, and C0 are used to determine outputs Σ1 and Σ2 and the value of the internal carry C2. The values at C2, A3, B3, A4, and B4 are then used to determine outputs Σ3, Σ4, and C4.

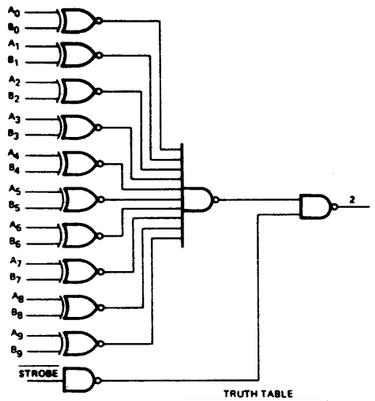
1820-1275
DUAL 5-INPUT POSITIVE-NOR GATES



1820-1288
DUAL CLOCK DRIVER



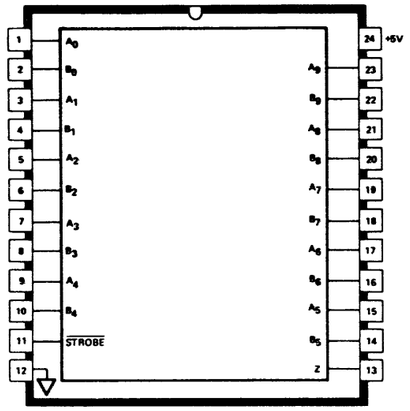
1820-1293
10-BIT COMPARATOR



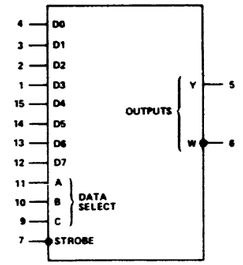
TRUTH TABLE

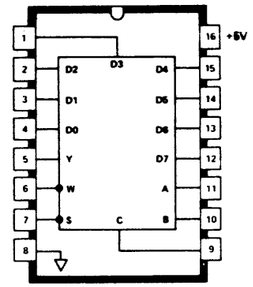
CONDITION	STROBE S	Z
A = B, A ≠ B	1	1
A = B	0	1
A ≠ B	0	0

A = A_0 thru A_9
B = B_0 thru B_9



1820-1302
DATA SELECTORS/MULTIPLEXERS WITH 3-STATE OUTPUTS



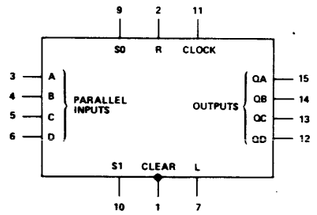


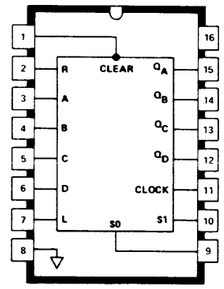
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	Z	Z
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

The data selector/multiplexer contains full binary decoding to select one-of-eight data sources and feature a strobe-controlled three-state output. The strobe must be at a low logic level to enable these devices. The three-state outputs permit a number of outputs to be connected to a common bus. When the strobe input is high, both outputs are in a high-impedance state in which both the upper and lower transistors of each totem-pole output are off, and the output neither drives nor loads the bus significantly. When the strobe is low, the outputs are activated and operate as standard TTL totem-pole outputs.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable time is shorter than the average output enable time.

1820-1304
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER





The register has four distinct modes of operation.

Parallel (broadside) load
Shift right (in the direction Q_A toward Q_D)
Shift left (in the direction Q_D toward Q_A)
Inhibit clock (do nothing)

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

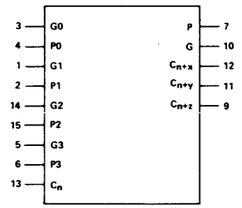
INPUTS										OUTPUTS			
	MODE			SERIAL		PARALLEL							
CLEAR	S1	S0	CLOCK	LEFT	RIGHT	A	B	C	D	Q_A	Q_B	Q_C	Q_D
L	X	X	X	X	X	X	X	X	X	L	L	L	L
H	X	X	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}
H	H	H	↑	X	X	a	b	c	d	a	b	c	d
H	L	H	↑	X	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}
H	L	H	↑	X	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}
H	H	L	↑	H	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	H
H	H	L	↑	L	X	X	X	X	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	L
H	L	L	X	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}

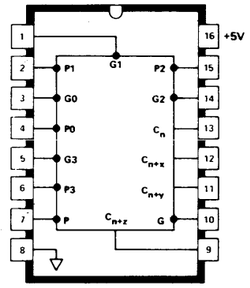
H = high level (steady state)
L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level
a, b, c, d = the level of steady-state input at inputs A, B, C, or D, respectively.

Q_{AO}, Q_{BO},Q_{CO}, Q_{DO} = the level of Q_A, Q_B, Q_C, or Q_D, respectively, before the indicated steady-state input conditions were established.

Q_{An}, Q_{Bn}, Q_{Cn}, Q_{Dn} = the level of Q_A, Q_B, Q_C, Q_D, respectively, before the most recent ↑ transition of the clock.

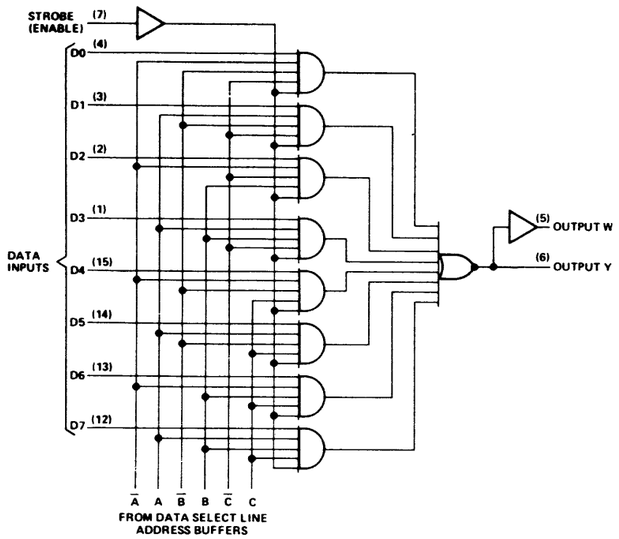
1820-1305
LOOK-AHEAD CARRY GENERATOR

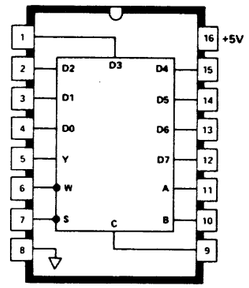




DESIGNATION	PIN NOS.	FUNCTION
G0,G1,G2,G3	3,1,14,5	ACTIVE LOW CARRY GENERATE INPUTS
P0,P1,P2,P3	4,2,15,6	ACTIVE LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y} C_{n+z}	12,11,9	CARRY OUTPUTS
G	10	ACTIVE LOW CARRY GENERATE OUTPUT
P	7	ACTIVE LOW CARRY PROPAGATE OUTPUT
+5V	16	SUPPLY VOLTAGE
GND	8	GROUND

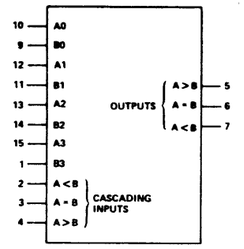
1820-1319
8-INPUT MULTIPLEXER WITH COMPLEMENTARY OUTPUTS

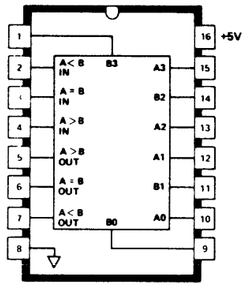




INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

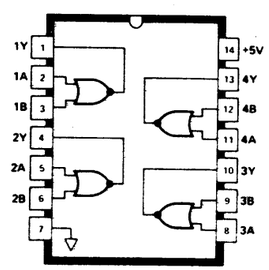
1820-1321
4-BIT MAGNITUDE COMPARATOR





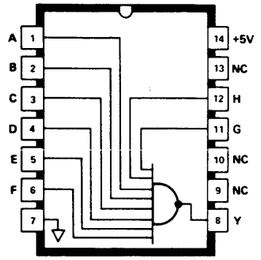
COMPARING UNITS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	X	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	L	L

1820-1322
QUADRUPLE 2-INPUT POSITIVE-NOR GATES

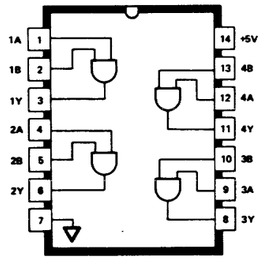


positive logic
$\overline{Y = A + B}$

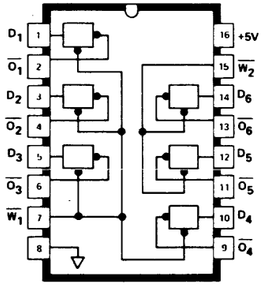
1820-1323
8-INPUT POSITIVE-NAND GATE



1820-1367
QUAD 2-INPUT AND GATE

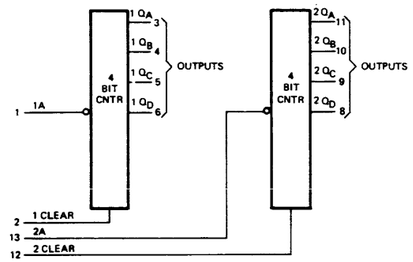


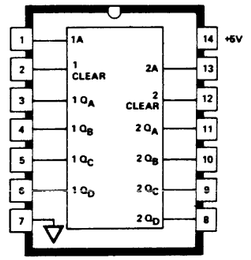
1820-1395
6-BIT LATCH



This integrated circuit contains six high speed latches organized as an independent 4 bit and 2 bit latches. The latches act as high speed inverters when the "write" input is "low".

1820-1464
DUAL 4-BIT BINARY COUNTER

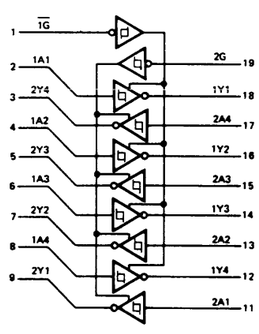


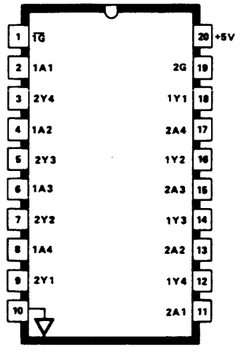


COUNT SEQUENCE (EACH COUNTER)

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

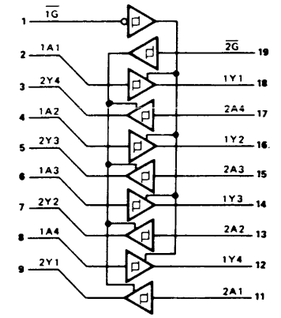
1820-1624
TRI-LEVEL
OCTAL LINE DRIVERS/
LINE RECEIVERS

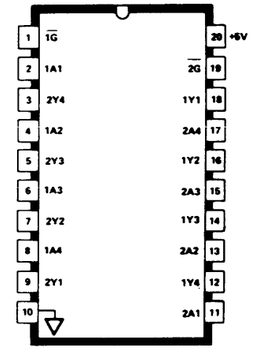




logic: 1Y = 1A when $\overline{1G}$ is low
2Y = 2A when $\overline{2G}$ is high
When $\overline{1G}$ is high 1Y outputs are at a high impedance
When 2G is low 2Y outputs are at a high impedance

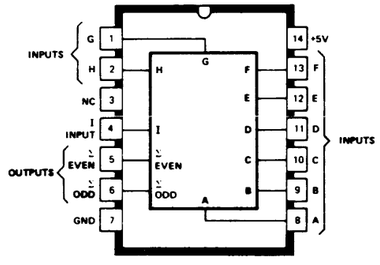
1820-1633
TRI-LEVEL
OCTAL LINE DRIVERS/
LINE RECEIVERS





logic: 1Y = 1A when $\overline{1G}$ is low
2Y = 2A when $\overline{2G}$ is low
When $\overline{1G}$ is high 1Y outputs are at a high impedance
When $\overline{2G}$ is high 2Y outputs are at a high impedance

1820-1638
9-BIT ODD/EVEN PARITY
GENERATOR/CHECKER



TRUTH TABLE

NUMBER OF INPUTS A THRU I THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

H = high level, L = low level

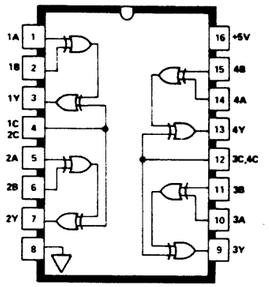
1820-1639
QUAD EXCLUSIVE OR/NOR GATE

TRUTH TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
L	L	H	H
L	H	H	L
H	L	H	L
H	H	H	H

H = high level, L = low level

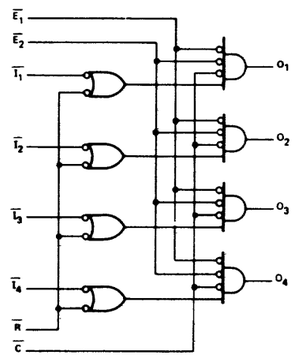
positive logic. $Y = (A \oplus B) \oplus C = A\bar{B}\bar{C} + \bar{A}B\bar{C} + \bar{A}\bar{B}C + ABC$

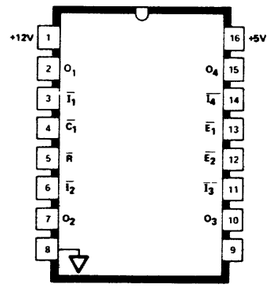


When C input is low, operates as a Exclusive OR gate. When C input is high, operates as a Exclusive NOR gate.

1820-1758
QUAD TTL TO MOS DRIVER

LOGIC DIAGRAM

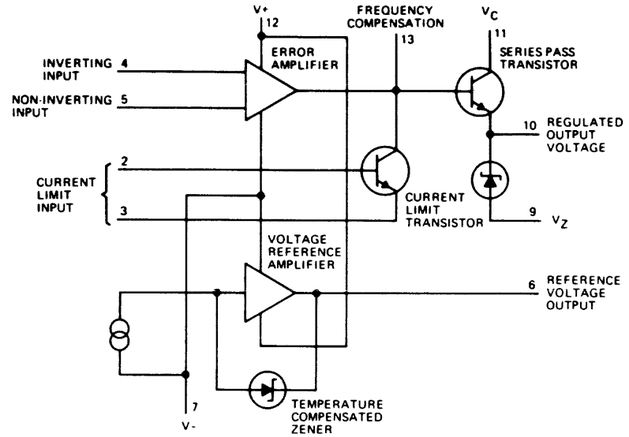


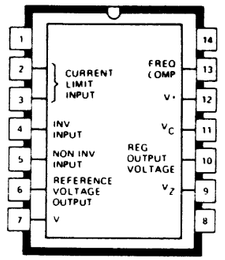


PIN NAMES

$\bar{I}_1 \cdot \bar{I}_4$ SELECT INPUTS	$O_1 \cdot O_4$ DRIVER OUTPUTS
$\bar{E}_1 \cdot \bar{E}_4$ ENABLE INPUTS	V_{CC} +5V POWER SUPPLY
$\bar{R}$ REFRESH SELECT INPUTS	V_{DD} +12V POWER SUPPLY
$\bar{C}$ CLOCK CONTROL INPUT	

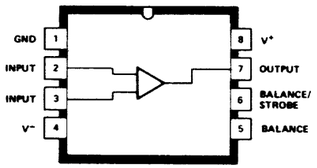
1826-0049
VOLTAGE REGULATOR



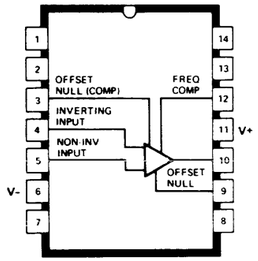


This integrated circuit provides a regulated voltage and a low-current reference voltage. Provisions are included for voltage shut-down in the event of excessive current in an external circuit. The integrated circuit can be used with external components in a variety of configurations. For specific information, refer to the applicable technical manual.

1826-0065
VOLTAGE COMPARATOR

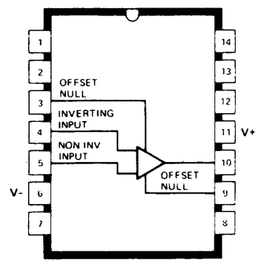


1826-0069
OPERATIONAL AMPLIFIER



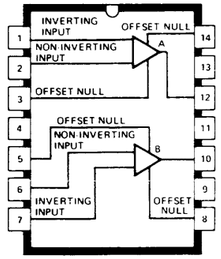
This integrated circuit is an operational amplifier. External components permit its use in a variety of functions, such as a long interval integrator, timer, sample-and-hold circuit square wave generator, or pulse-width modulator. For specific information, refer to the applicable technical manual.

1826-0070
OPERATIONAL AMPLIFIER



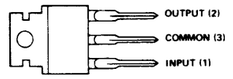
This integrated circuit is an operational amplifier. External components permit its use in a variety of functions. For specific information, refer to the applicable technical manual.

1826-0100
DUAL OPERATIONAL AMPLIFIER



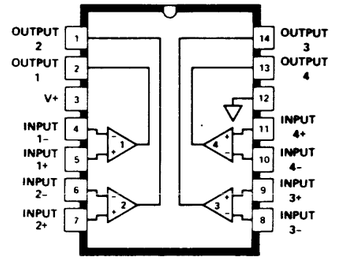
This integrated circuit consists of two separate operational amplifiers. External components permit their use in a variety of separate and combined functions. For specific information, refer to the applicable technical manual.

1826-0106
VOLTAGE REGULATOR



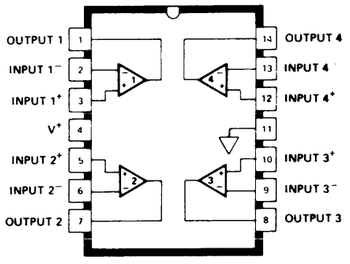
The voltage regulator provides a positive 15 volt output with current limiting, thermal shutdown, and safe area compensation internally incorporated in the device. Refer to the applicable equipment manual for specific use of the device.

1826-0138
QUAD VOLTAGE COMPARATOR



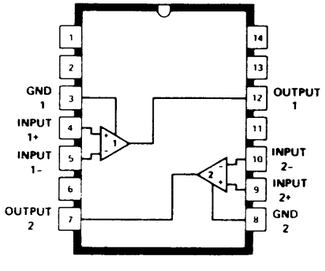
Refer to the applicable equipment manual for specific use of the device.

1826-0161
QUAD OPERATIONAL AMPLIFIER

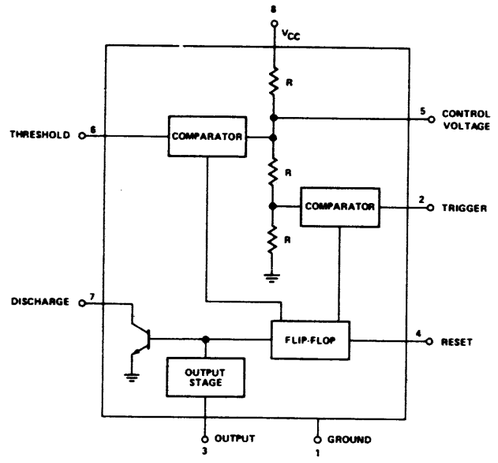


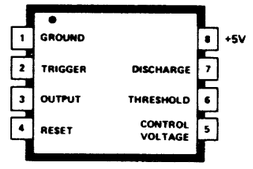
This Integrated circuit consists of four independent, high gain, internally frequency compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Input common mode voltage range includes ground. Differential input voltage range is equal to the power supply voltage, 3 to 30 volts.

1826-0175
DUAL VOLTAGE COMPARATOR



1826-0180
TIMER





The timer is a highly stable controller capable of producing accurate time delays or oscillation by the selected values of external components.

DIAGRAMS

SECTION III

3-1. INTRODUCTION

This section contains Engineering Diagrams for the printed circuit assemblies (PCA's) used in the HP 3000 series 33 system.

Each Diagram set contains a schematic diagram and part location diagram for each assembly. The Diagram sets are arranged numerically by the major assembly part number, as indicated in table 3-1.

3-2. PART LOCATION DIAGRAMS

Each diagram set contains a part location diagram. The part location diagram is provided as an aid in physically locating integrated circuits on the PCA.

3-3. SCHEMATIC DIAGRAMS

The Schematic diagram contents are exact duplicated of the engineering masters with no alterations to the information contained on each diagram.

TABLE 3-1. DIAGRAM INDEX

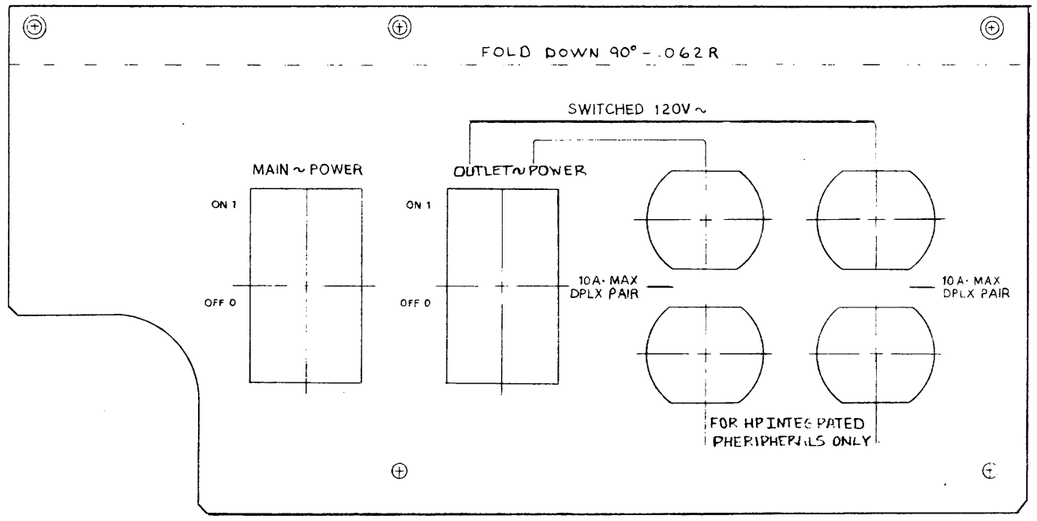
TABLE 3-1. DIAGRAM INDEX (Continued)

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22		25	29	30	32	33	38	43
45	46	61	63	67										

SEPIA

C-30016-00001-2

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		12/1/77
B	REVISE DESIGNER INFO. IN TITLE		6-22-78



ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE COVER P.C.M. TYPE

HEWLETT PACKARD

NEXT ASSEMBLY 30016-60051

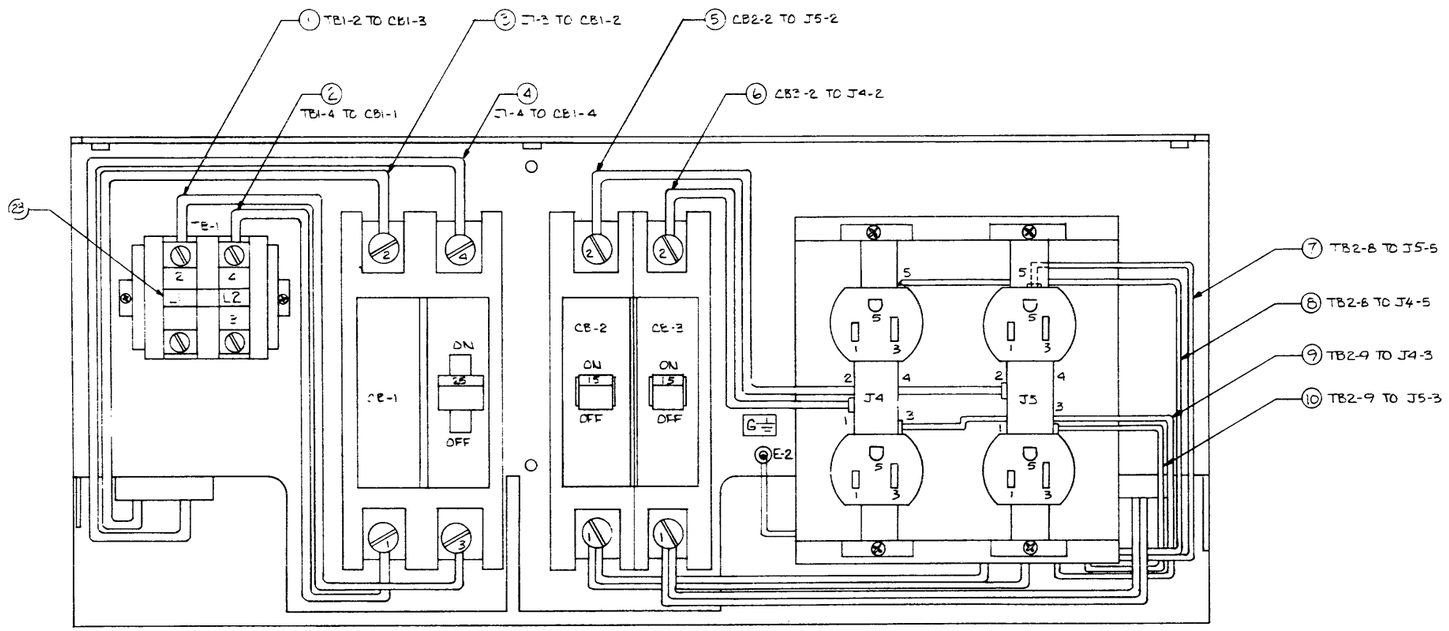
PART NUMBER 30016-00001

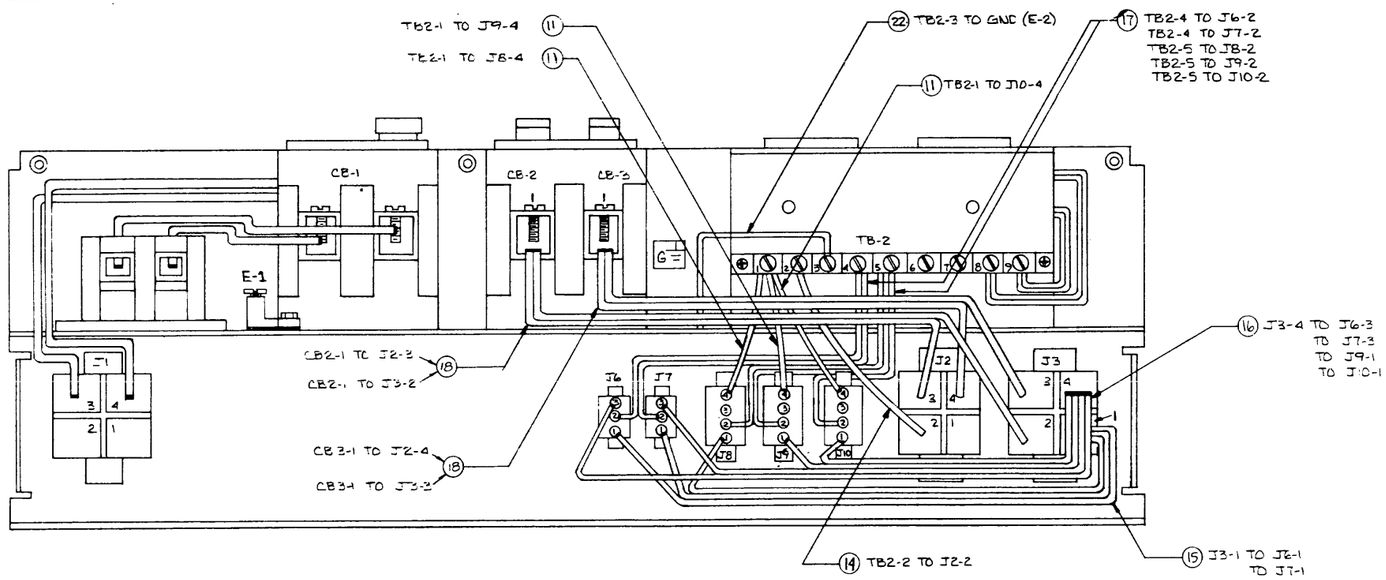
FINISH 1\|2\| SCALE NONE

C-30016-00001-2

SHEET 1 OF 1

STOCK NO 8290-0003 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT





ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L SPEC NO	MAT'L SPEC
23	1	LABEL L1-L2			
22	1	WIRE ASSY	30016-60021		
21		DELETED			
20		DELETED			
19		DELETED			
18	4	WIRE ASSY	30016-60007		
17	1	CA-GROUND	30016-60004		
16	1	CA-LINE 2	30016-60023		
15	1	CA-LINE 1	30016-60022		
14	1	WIRE ASSY	30016-60013		
13		DELETED			
12		DELETED			
11	3	WIRE ASSY	30016-60016		
10	1	WIRE ASSY	30016-60017		
9	1	WIRE ASSY	30016-60018		
8	1	WIRE ASSY	30016-60019		
7	1	WIRE ASSY	30016-60020		
6	1	WIRE ASSY	30016-60011		
5	1	WIRE ASSY	30016-60014		
4	1	WIRE ASSY	30016-60015		
3	1	WIRE ASSY	30016-60005		
2	1	WIRE NO. 2		A-2	
1	1	WIRE NO. 1		A-2	

TITLE	WIRING - POWER TYPE I - 240 VAC
NEXT ASSEMBLY	5001GA
FINISH	SCALE
PART NUMBER	30016-60001
	D-30016-60001-1
	SHEET 1 OF 1

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 16	
16 17 18 21 22 23 25 29 30 32 33 38 43	
45 46 61 63 64	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	25/Q4	9/1/82

J4 & J5 PHYSICAL LAYOUT

AC INPUT:
1 PHASE
W/ GROUND
50/60 HZ

TB 1

#10 RED

#10 BLACK

25A/250V CIRCUIT BREAKER

CKB 1

J1

TERM 1

E1

SYSTEM GROUND

TERM 2

E3

GROUND BRAID

TERM 3

LOCATED ON PCM

NOT PART OF POWER CONTROL MODULE

P1

SEE CONNECTION MATRIX AT LOWER LEFT

ISOLATION TRANSFORMER 9100-4062

120 V. #10 RED

0 #10 WHITE

120 V. #10 BLACK

P2

J2

P3

#10 BLK EA

#10 BLACK EA

LINE

CKB 4 20A.

LOCATED ON MAINFRAME CHASSIS

L1 #10 BLK

CKB 2 15A.

L2 #10 BLK

CKB 3 15A.

J4 (120 V. AT 10A)

GROUND #14 GREEN/YEL

NEMA DUPLEX OUTLETS

J5 (120 V. AT 10A.)

#14 WHITE EA

#10 WHITE

J3

#16 RED EA.

#16 WHT/YEL EA.

TB 3

GROUNDING BLOCK

J6 (240 V.) FOR PSU 1

J7 (240 V.) FOR PSU 2

J8 (120 V.) FOR PLENUMS 1&2

J9 (120 V.) FOR 7902H MOTOR

J10 (120 V.) FOR 7902H FAN

#10 GRN/YEL

TERM 4 E2

LOCATED ON PCM

1251-4780

GO TO POWER SUPPLY UNIT 1

GO TO POWER SUPPLY UNIT 2

#16

NO C

THIS CKB/SWITCH IS LOCATED IN FRONT TO THE RIGHT OF THE OPERATOR'S KNEE.

NOT PART OF AC DISTRIBUTION

CONNECTION MATRIX
PRIMARY VOLTAGE STRAPPING FOR ISOLATION TRANSFORMER
(NUMBERS IN TABLE REPRESENT TAPS ON THE ISOLATION TRANSFORMER)

VOLTAGE	A	B	C	D
200 V.	1	2	5	6
210 V.	1	3	5	6
220 V.	1	3	5	7
230 V.	1	4	5	7
240 V.	1	4	5	8

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

PWR CONTROL MOD
TYPE 1
SCHEMATIC DWG

HEWLETT PACKARD

NEXT ASSEMBLY 30016A

PART NUMBER 30016-60001

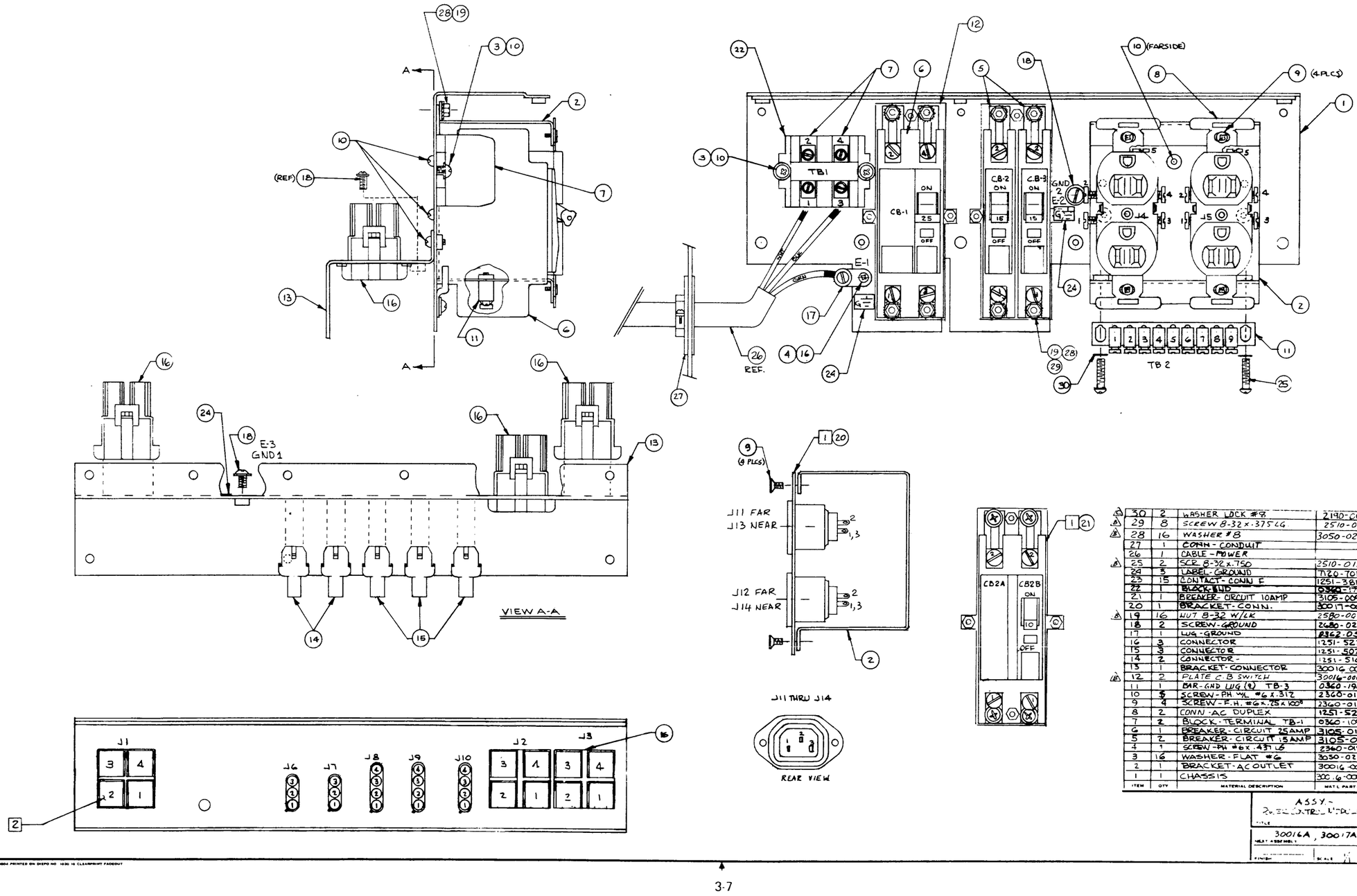
FINISH SCALE NONE

D - 30016 - 60001 - 51

SHEET 1 OF 1

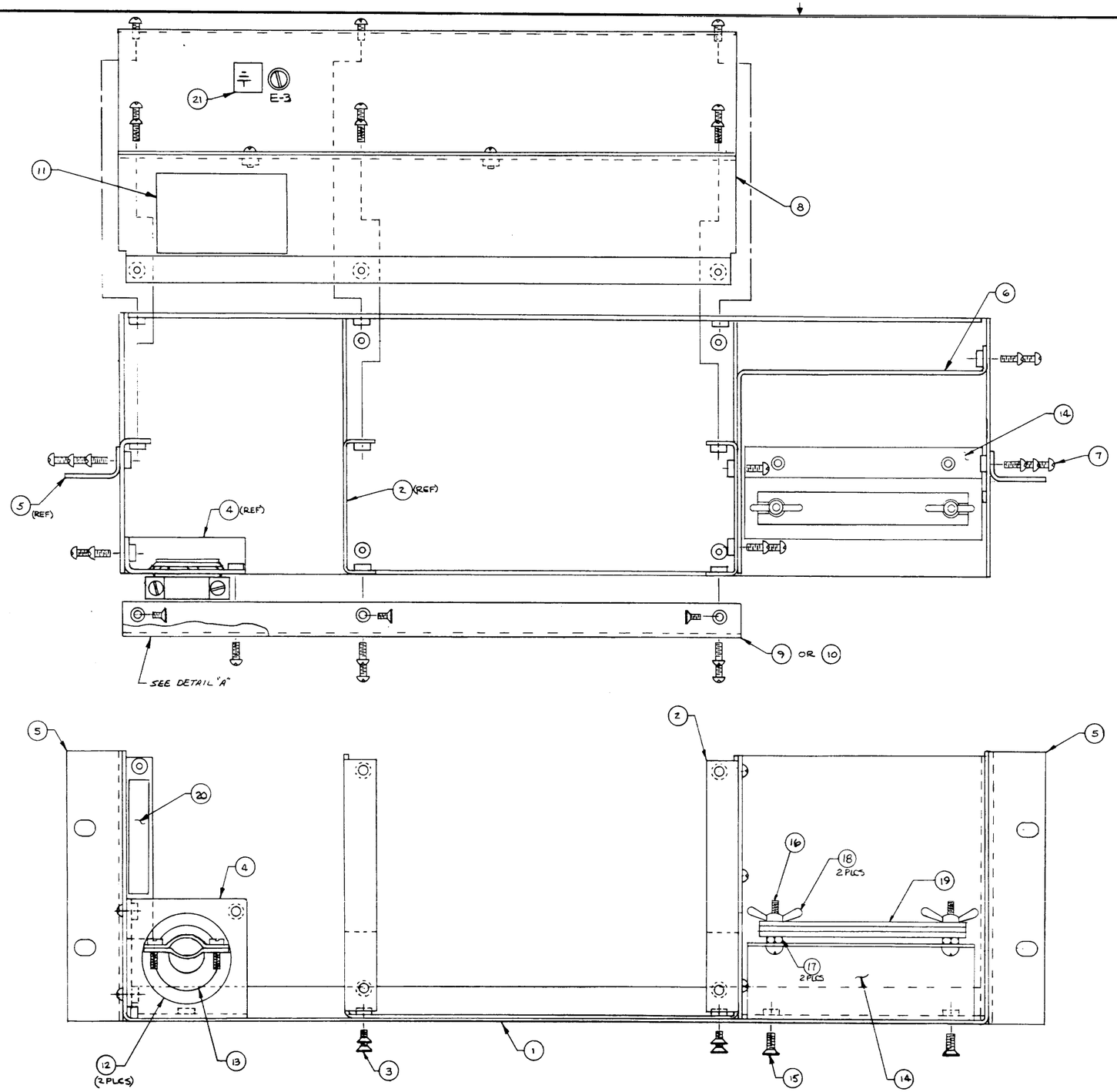
ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 15	
16 17 19 21 22 23 25 29 30 32 33 38 43	
46 46 61 63 67	

1-30016-90001-1			
STR	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	7/6/78
B	PRCR 'G' ITEM 12 WAS 2200-0165, ITEM 19 WAS 1251-5236, ITEM 25 WAS 2360-0125, ADD ITEMS 28, 29.	[illegible]	9-26-78
C	DEL. NOTE. ADD ITEM 30 PER DOC. CHG	[illegible]	10-9-78



	ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
	30	2	WASHER LOCK #8	2190-0073		
A	29	8	SCREW 8-32 x .375 LG	2510-0121		
A	28	16	WASHER #8	3050-0226		
	27	1	CONN - CONDUIT		D- x	
	26	1	CABLE - POWER		B-30016-60001-3	
A	25	2	SCR 8-32 x .750	2510-0111		
	24	3	LABEL - GROUND	7120-7016		
	23	15	CONTACT - CONN F	1251-3816		
	22	1	BLOCK, LID	0360-1795		
	21	1	BREAKER - CIRCUIT 10AMP	3105-0092		
	20	1	BRACKET - CONN.	30017-00001		
A	19	16	NUT 8-32 W/LK	2580-0003		
	18	2	SCREW - GROUND	2680-0226		
	17	1	LUG - GROUND	0362-0511		
	16	3	CONNECTOR	1251-5228		
	15	3	CONNECTOR	1251-5070		
	14	2	CONNECTOR -	1251-5106		
	13	1	BRACKET - CONNECTOR	30016-00008		
A	12	2	PLATE C B SWITCH	30016-00010		
	11	1	BAR - GND LUG (8) TB-3	0360-1900		
	10	5	SCREW - PH MS #6 X .312	2360-0115		
	9	4	SCREW - F.H. #6 x .25 x 100°	2360-0192		
	8	2	CONN - AC DUPLEX	1251-5235		
	7	2	BLOCK - TERMINAL TB-1	0360-1094		
	6	1	BREAKER - CIRCUIT 25AMP	3105-0100		
	5	2	BREAKER - CIRCUIT 15AMP	3105-0101		
	4	9	SCREW - PH #6 x .437 LG	2360-0199		
	3	16	WASHER - FLAT #6	3050-0227		
	2	1	BRACKET - AC OUTLET	30016-00006		
	1	1	CHASSIS	30016-00003		

TITLE	ASSY - POWER CONTROL MODULE
NEXT ASSY NO.	30016A, 30017A
FINISH	
SCALE	
	HEWLETT PACKARD
	30016-60001
PART NUMBER	30017-60001
	D-30016-90001-1
	SHEET 1 OF 1



ENGINEERING RESPONSIBILITY	SIZE
0 1 2 3 4	6 9 11 12 14 16
16 17 19	21 22 23 25 28 30 32 33 36 43
46 48 61 63	65

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	3/1/78
B	ADD 0590-0665 DELETE 3056-0019 PER [illegible]	[illegible]	7-10-78

D-30016-90001-2

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
21	1	LABEL-GROUND	7120-7016		
20	1	LABEL-WARNING	7120-7038		
19	3	CLAMP-CABLE	30070-00010		
18	2	NUT WING #10-32	0590-0665		
17	2	NUT-HEX 9/L #10	2940-0053		
16	2	SCREW-PH 10-32X2.00	2680-0073		
15	2	SCREW-F.H .088 8-32X.375	2510-0121		
14	1	CLAMP-BRT	30070-00069		
13	1	CONN CBL 3/4 3T	0100-0300		
12	2	WASHER, REDUCING	3050-0927		
11	2	LABEL-WARNING	7120-7039		
10	1	COVER-PCM	30017-00001		
9	1	COVER-P.C.M	30016-00001		
8	1	ASSY-CHASSIS & CONN			D-1
7	29	SCREW-PH W/L #6 X .312	2360-0115		
6	1	BRACKET-DRESS	30016-00007		
5	2	BRACKET-RACK	30016-00009		
4	1	BRACKET-A.C. INPUT	30016-00008		
3	7	SCREW-F.H #6 x .312	2360-0196		
2	1	SHIELD	30016-00006		
1	1	COVER-BOTTOM	30016-00002		

TITLE: ASSY-POWER CONTROL MODULE

NEXT ASSEMBLY: 30016A, 30017A

FINISH: —

SCALE: 1/1

HEWLETT PACKARD

PART NUMBER 30016-60001

PART NUMBER 30017-60001

D-30016-90001-2

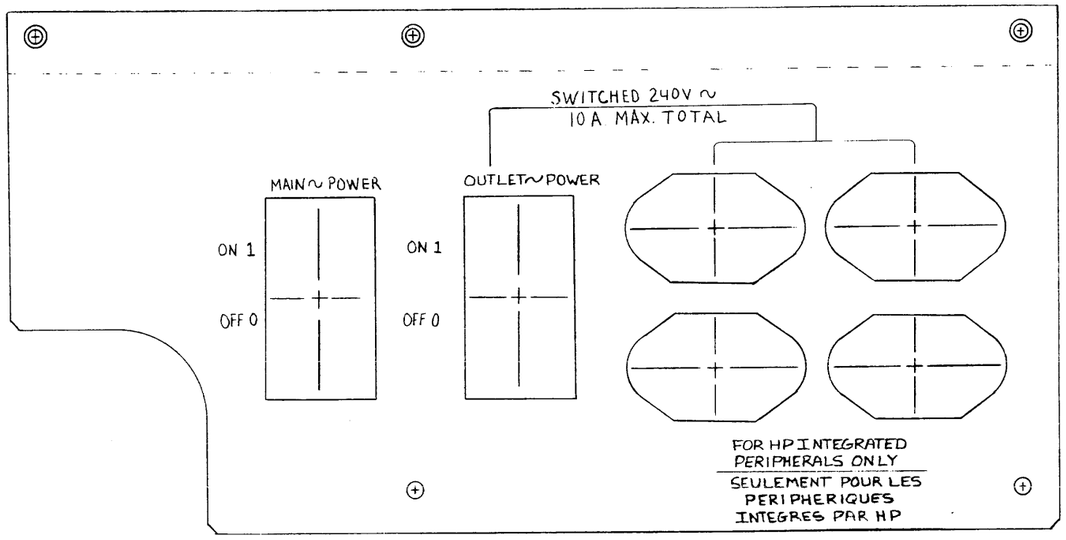
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY ▨ SEPIA ▨

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22		25	29	30	32	33	38	43
45	46	61	63	67										

C-30017-00001-2

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	1/31/78
B	CHANGED SLKSCREEN INFO PRCR'C"	[illegible]	4-22-78



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG NO.	MAT'L-SPEC.

TITLE: COVER-PCM TYPE 1

HEWLETT-PACKARD

NEXT ASSEMBLY: 30017-60001

PART NUMBER: 30017-00001

FINISH: 1. 2 | SCALE: NONE

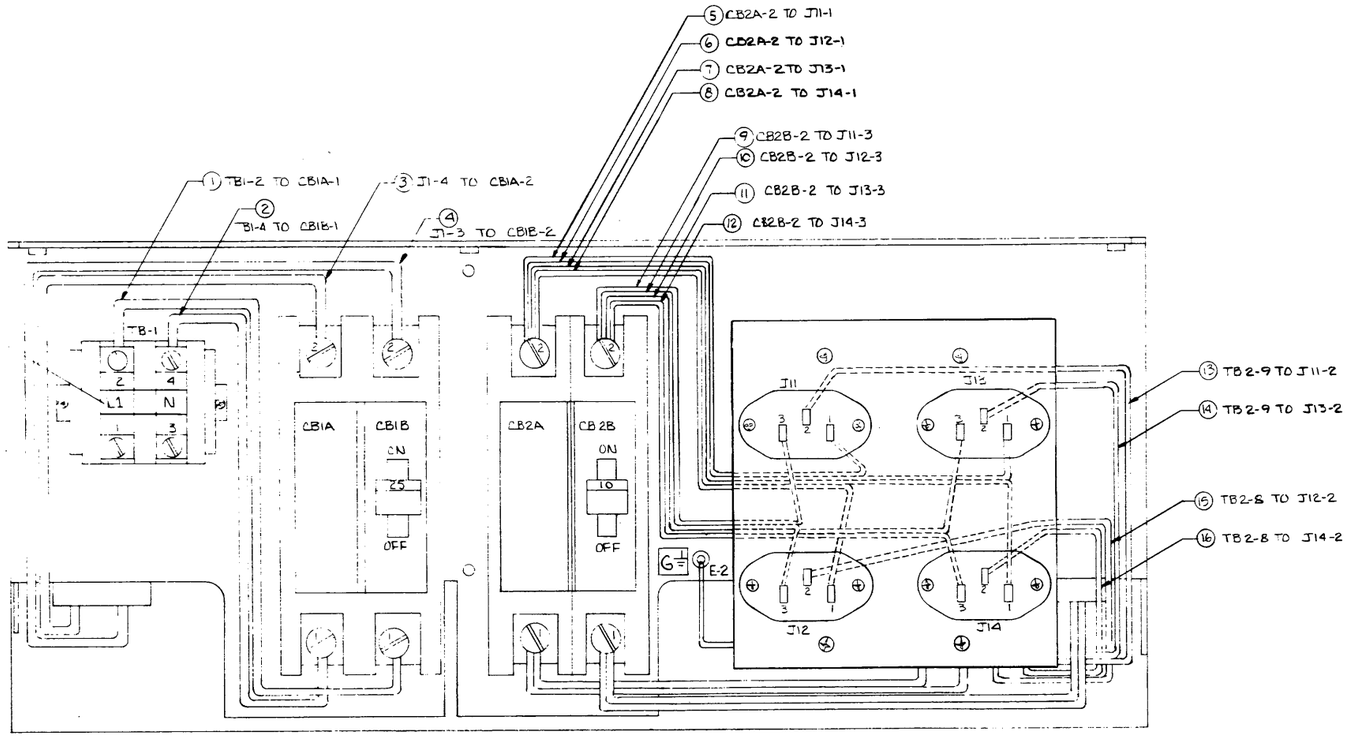
C-30017-00001-2

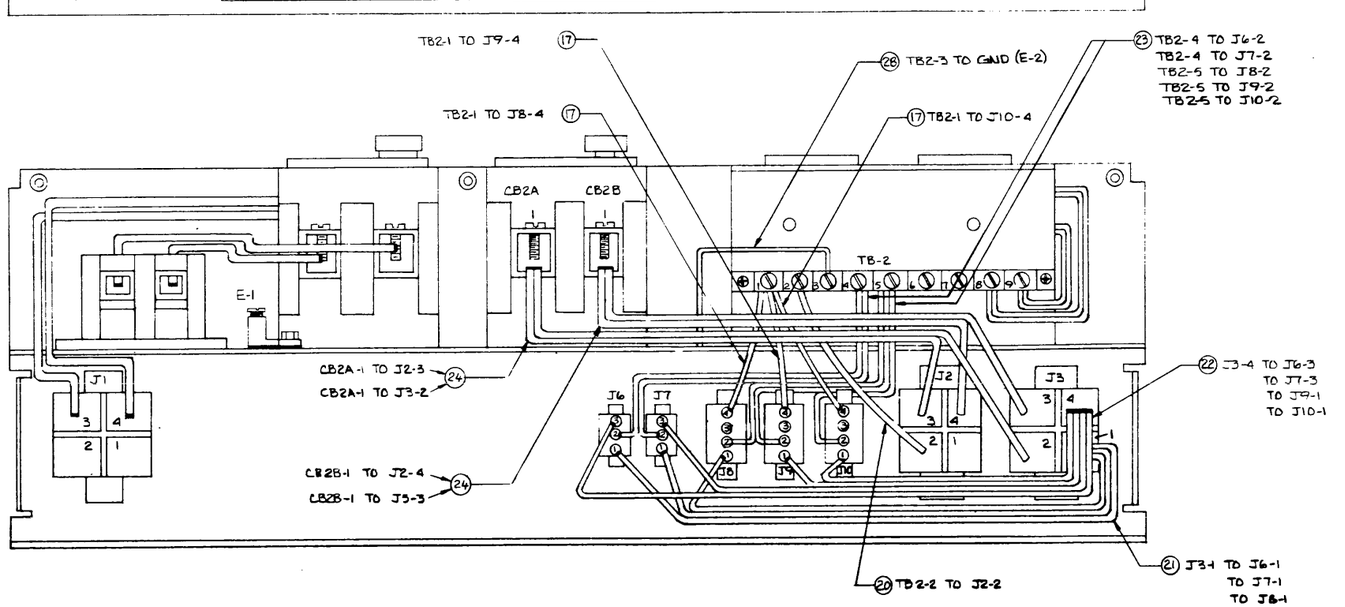
SHEET 1 OF 1

STOCK NO. 9280-0003 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 15	
16 17 18 21 22 23 25 29 30 32 33 38 43	
45 46 61 63 [47]	

STM	REVISIONS	APPROVED	DATE
A	AS ISSUED	02/08	7/6/78
B	REVISED PER ECR 9269 WIRE ASSY'S 30016-60008/9/10/11/12		7-14-78
C	DEL NOTE, ADD ITEM 18 PER DOC CHG.	VFI	12-5-78





ITEM	QTY	MATERIAL-DESCRIPTION	MFG PART NO	MFG CODE NO	MFG SPEC
24		DELETED			
28	1	WIRE ASSY	30016-60021	C 30016-90002-1	
27		DELETED			
26		DELETED			
25		DELETED			
24	4	WIRE ASSY	30016-60007	C 30016-90002-1	
23	1	CA-GROUND	30016-60004		
22	1	CA-LINE 2	30016-60003		
21	1	CA-LINE 1	30016-60002		
20	1	WIRE ASSY	30016-60013	C-30016-90002-1	
19		DELETED			
18	1	LABEL LI N	7120-7336		
17	3	WIRE ASSY	30016-60016	C 30016-90002-1	
16		WIRE NO 14		A-2	
15		WIRE NO 13		A-2	
14		WIRE NO 12		A-2	
13		WIRE NO 11		A-2	
12		WIRE NO 10		A-2	
11		WIRE NO 9		A-2	
10		WIRE NO 8		A-2	
9		WIRE NO 7		A-2	
8		WIRE NO 6		A-2	
7		WIRE NO 5		A-2	
6		WIRE NO 4		A-2	
5		WIRE NO 3		A-2	
4	1	WIRE ASSY	30016-60012	C-30016-90002-1	
3	1	WIRE ASSY	30016-60005	C-30016-90002-1	
2		WIRE NO 2		A-2	
1		WIRE NO 1		A-2	

TITLE: WIRING - PCM TYPE I - 50Hz	NEWLETT PACKARD
NEXT ASSEMBLY: 30017A	PART NUMBER: 30017-60001
FINISH: — SCALE: —	30017-60001

NOT PART OF POWER CONTROL MODULE

AC INPUT: 1-PHASE, W/ GROUND 50/60 HZ

TB 1 — 25A/250V. CIRCUIT BREAKER — J1

#10 RED — #10 RED

#10 BLACK — #10 BLACK — CKB 1

TERM 1 (E1) — SYSTEM GROUND

TERM 2 (E3) — GROUND BRAID — TERM 3

LOCATED ON FCM

P1 — #10 RED — #10 BLACK — "SEE CONNECTION MATRIX AT LOWER LEFT"

ISOLATION TRANSFORMER 9100-1062

A, B, C, D, P6, S6, S1, S2

9 — 120V. #10 RED — P2

10 — 0 — #10 WHITE

11

12 — 120V. #10 BLACK

LOCATED ON MAINFRAME CHASSIS

CONNECTION MATRIX
PRIMARY VOLTAGE STRAPPING FOR ISOLATION TRANSFORMER
(NUMBERS IN TABLE REPRESENT TAPS ON THE ISOLATION TRANSFORMER)

VOLTAGE	A	B	C	D
200 V.	1	2	5	6
210 V	1	3	5	6
220 V	1	3	5	7
230 V.	1	4	5	7
240 V.	1	4	5	8

J2 — L1, N, L2 — #10 WHITE

#10 BLACK (L1) — CKB 6 10A. — #16 RED EA

#10 BLACK (L2) — CKB 7 10A — #16 BLK/WHT EACH

#10 BLACK

J11, 240V. CEE RECEPTACLE

J12, 240V CEE RECEPTACLE

J13, 240V. CEE RECEPTACLE

J14, 240V. CEE RECEPTACLE

240V ∿ 10A. MAX

#16 GRN/YEL EACH

TB 3 — GROUNDING BLOCK 1

#14 WHITE EA.

J6, 240V. FOR PSU 1 — GROUND #14

J7, 240V FOR PSU 2 — GROUND #14 GREEN/YEL

#16 RED EA.

#10 GRN/YEL

TERM 4 (E2) — LOCATED ON PCM

J3 — P3 — #10 BLK EA.

#16 WHT/VIO EA.

J8, 120V. FOR PLENUMS 1 & 2 — GROUND #14 GREEN/YEL

J9, 120V. FOR 7902H MOTOR — GROUND #14 GREEN/YEL

J10, 120V. FOR 7902H FAN — GROUND #14 GREEN/YEL

#10 BLACK EA. — CKB 4 20A.

1251-4780 — TO PSU 1 — #16 — N.O. — C

TO PSU 2 — #16 — N.O. — C — 1251-4780

NOT PART OF THE AC DISTRIBUTION

THIS CKB/SWITCH IS LOCATED IN FRONT, TO THE RIGHT OF THE OPERATOR'S KNEE.

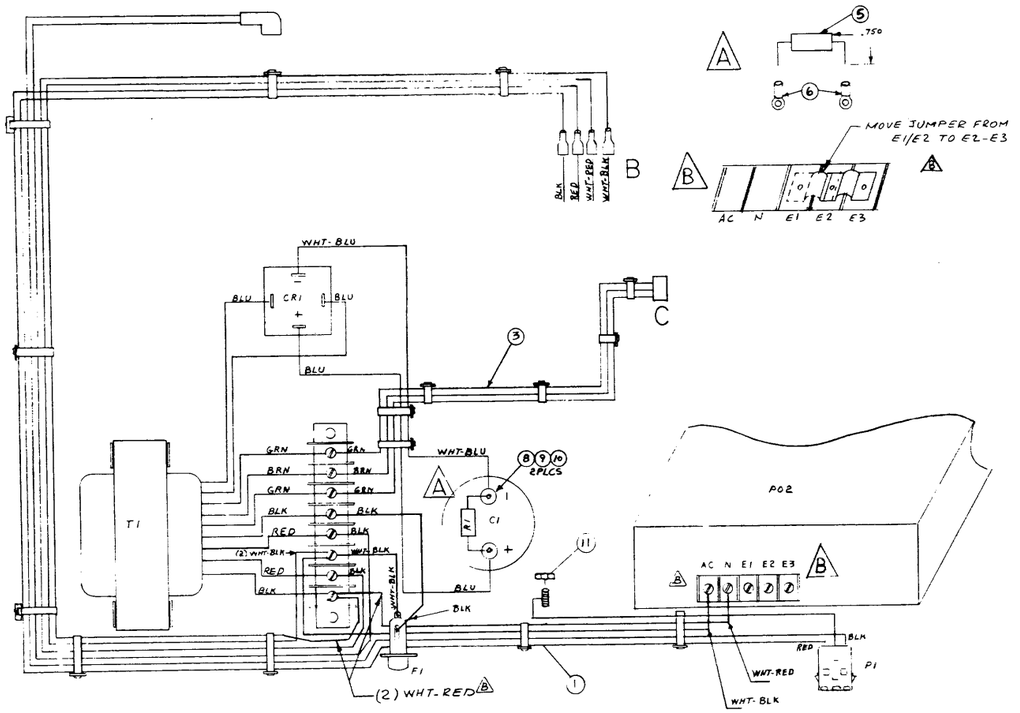
ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

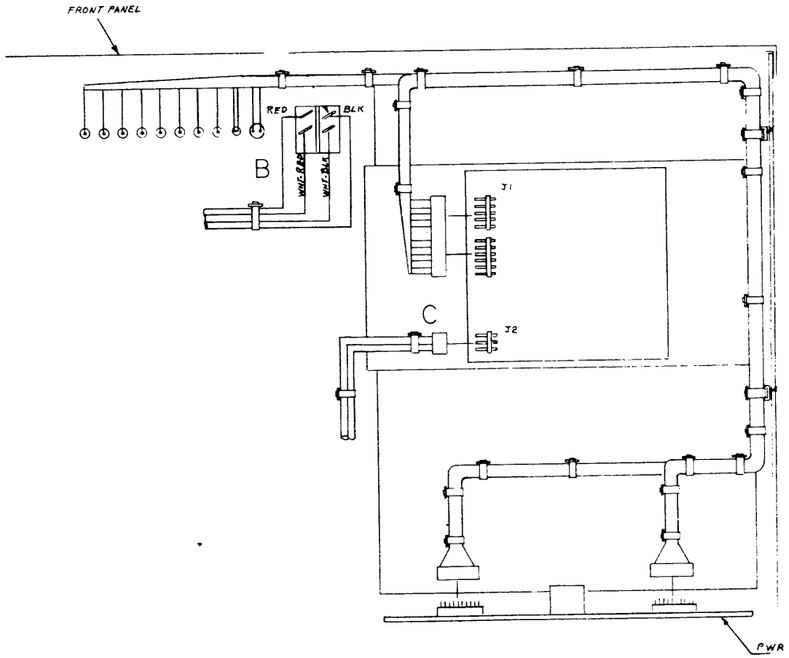
TITLE	PWR CONTROL MOD. TYPE 2 SCHEMATIC DWG	HEWLETT PACKARD	
NEXT ASSEMBLY	30017A	PART NUMBER	30017-60001
FINISH	SCALE NONE		D-30017-60001-51

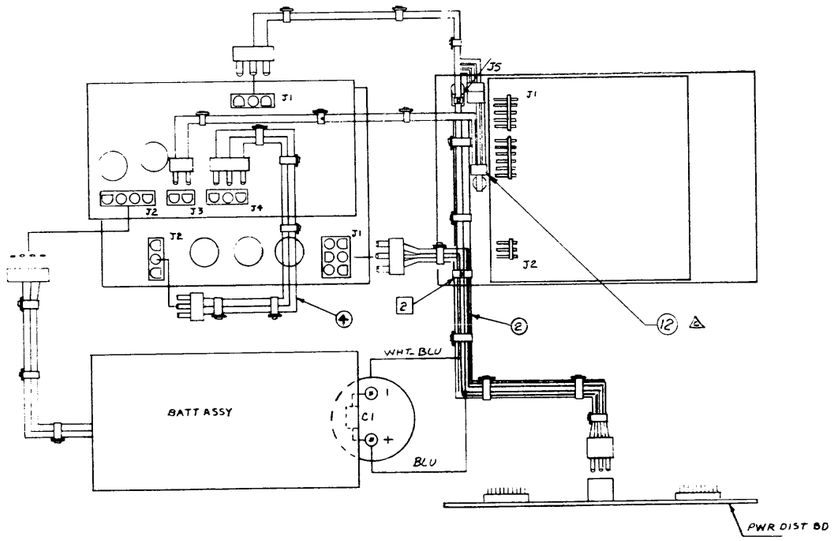
SHEET 1 OF 1

AC POWER 240V~
S1 3101-2251
F1 2100-0014 250V/5A
TB1
T1 9100-4066
CR1 1906-0093
R1 0764-0016 4.7K
C1 0160-2757 6900uf
BATT ASSY 31000-60001
MEM PRE-REG 31000-60067
MEM-REG 31000-60028
RELAY ASSY 30070-60071
63312F
V1 V2 V3
E5
E4 (RMT)
BIAS(15V)
UV
TC BACKPLANE P6 BROWN
P8 ORANGE
P9 BLUE
TO BREAKER P4
POWER DISTR BOARD 30070-60016
POWER CONTROL 31000-60056
FAN
TB1 0360-1870
TEST POINTS
+5 +5M +12 +12M -12 -12M BATT PON

POWER SUPPLY
HEWLETT PACKARD
30070-60007
D







ITEM	QTY	MATERIAL DESCRIPTION	MFG PART NO.	MFG SPEC
12	1	RELAY ASSY	REF 30070-60007	
11	1	NUT 6-32 W/LK	2420-0001	
10	2	WASHER FLT #6	3050-0226	
9	2	WASHER LK #10	2190-0034	
8	2	SCREW 10-32 X .438	2680-0101	
7	6	CABLE TIE	1400-0249	
6	2	LUG CRP22-18PT 10	0362-0319	
5	1	RES 4.7K 5% 2W	0764-0018	
4	1	CABLE PREREG OUT	31000-60024	
3	1	CABLE PWR SUP RECT	30070-60059	
2	1	CABLE PWR SUP -EC	30070-60058	
1	1	CABLE PWR SUP PRI	30070-60052	

ENGINEERING RESPONSIBILITY																		
0	1	2	3	4		6		8	9		11	12	14	15				
16	17		19		21	22	23	26	29	30	32	33	38	43				
45	46	61	63	62														

REVISIONS			
SYM		APPROVED	DATE
A	AS ISSUED	BK	7/3/78
B	REVISED PER ECN # "SEE SHEET"		9-7-78
C	ADD ITEM 12 PER ECN 47 427		6-7-79

D-30070-60007-2

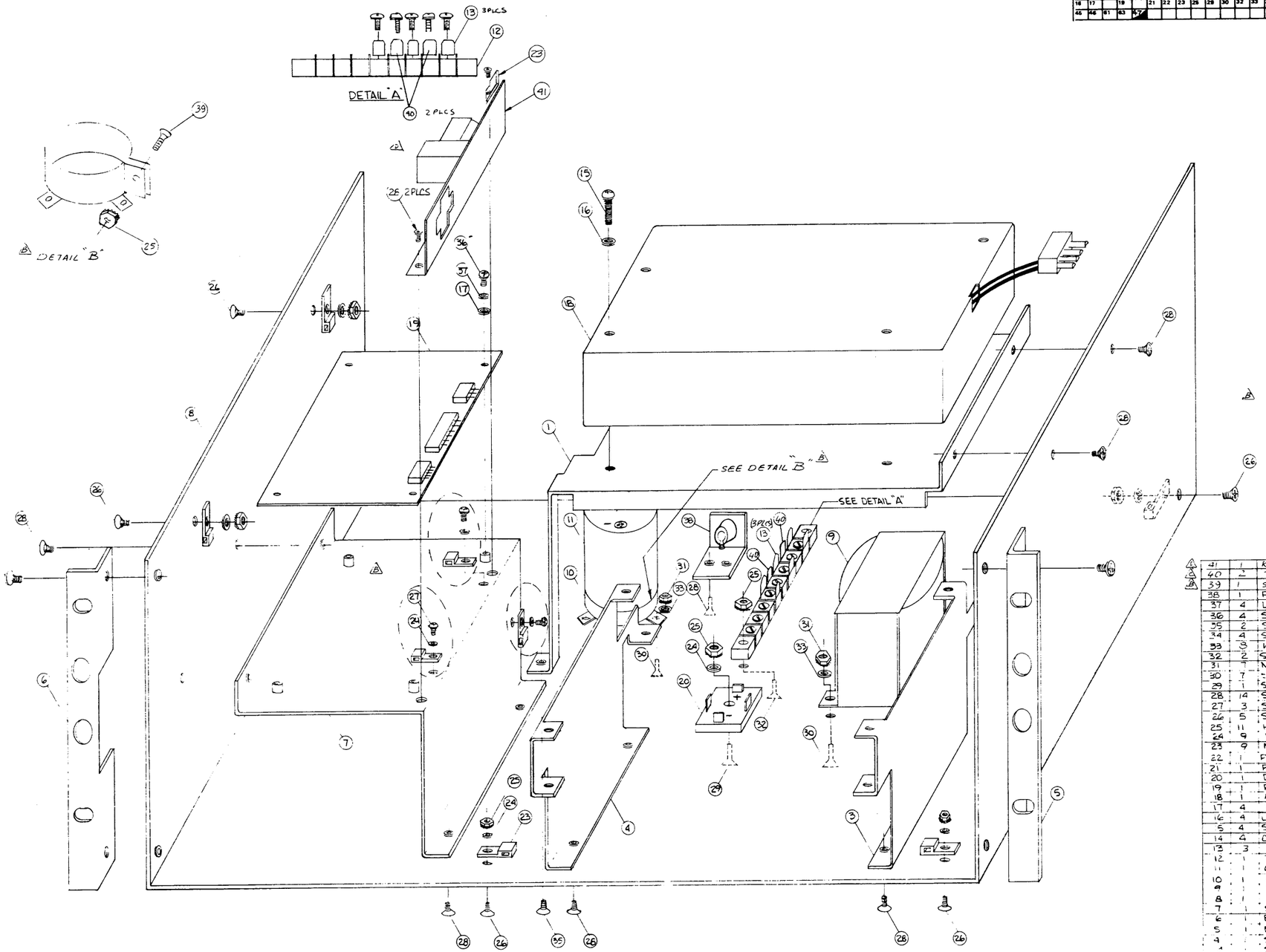
WIRING - FINAL
POWER SUPPLY

HEWLETT PACKARD

30070-60007

D 30070-60007 2

SHEET 1 OF 1



ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO.	MATL MFG NO.	MATL SPEC
41	1	RELAY ASSY	30070-6003		
40	2	TERM TAB	0360-1263		
39	1	SCR PH. 8-32 x .500 LG	2510-0049		
38	1	FUSE ASSY			B-6
37	4	LOCK WSHR 4-40	2190-0003		
36	4	SCR PH 4-40 x .312	2200-0141		
35	2	SCR FH 8-32 x .312	2510-0120		
34	4	SCR PH 8-32 x .380 W/LOCK	2510-0045		
33	5	WSHR 8-32	3050-0001		
32	2	SCR FH 6-32 x .750	2360-0211		
31	4	NUT HEX W/LOCK 8-32	2580-0003		
30	7	SCR FH 8-32 x .500	2510-0113		
29	1	SCR FH 6-32 x .875	2360-0212		
28	14	SCR FH 6-32 x .312	2360-0182		
27	3	SCR PH 6-32 x .312	2360-0115		
26	5	SCR FH 6-32 x .275	2360-0183		
25	11	HEX NUT 6-32 W/LOCK	2420-0001		
24	9	WSHR #6	3050-0227		
23	9	MT. CABLE TIE	1400-0786		
22	1	PCA-MEM REG	31000-60028		
21	1	PCA-MEM PRE-REG	31000-60067		
20	1	DIO-FWR 100V 35A	1906-0093		
19	1	PWR CONTROL BD	31000-60056		
18	1	ASSY-BATT PACK	31000-60001		
17	4	WSHR #4	3050-0105		
16	4	LK WSHR #8 HEL	2190-0073		
15	4	SCR RH 8-32 x .400	2520-0114		
14	4	CONNECTOR FEM 22-18 AWG	0262-0389		
13	3	TERM TAB .250	0360-1264		
12	1	TERM BLOCK	0360-1870		
11	1	CAP. 6900UF 75V	0180-2754		
10	1	CLAMP-CAPACITOR	0180-1969		
9	1	XFMR-PWR	9100-4066		
8	1	DECK	30070-60025		
7	1	SUP PC BD	30070-60031		
6	1	BKT. MTG. P.S LEFT	30070-60027		
5	1	BKT. MTG. P.S. RIGHT	30070-60026		
4	1	SUP PC. LEFT	30070-60030		
3	1	SUP. P.C. RIGHT	30070-60029		
2	6	[illegible]	[illegible]		
1	1	SUPPORT-BATTERY	30070-60034		

ENGINEERING RESPONSIBILITY																								
0	1	2	13	4		6		8	9		11	12	14	15										
16	17		19		21	22	23	25	28	30	32	33	38	43										
45	46	61	63	67																				

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	7/1/78
B	ADD DETAIL B, ITEM 39, ITEM 21 WAS 3180-6032, ITEM 22 WAS 32	[illegible]	7/17/78
C	DEC 78, ADD ITEM 40	[illegible]	3/14/79
D	ADD ITEM 41, 28 WAS 12, 23 WAS 8, PER ECO [illegible]	[illegible]	6/14/79

B-30070-60007-3

DECK ASSY — POWER SUPPLY

HEWLETT PACKARD

30070-60003

D

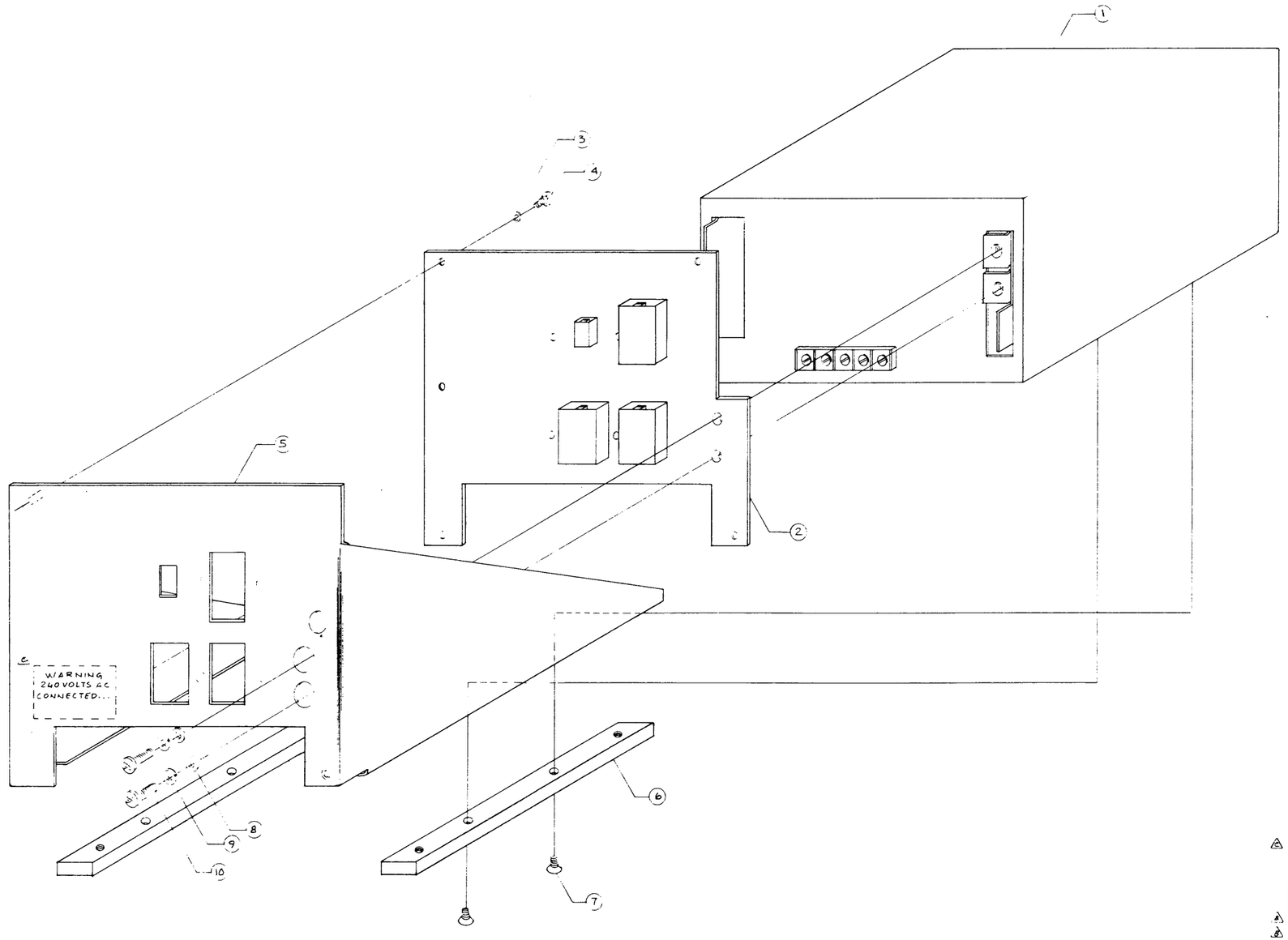
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY — BEPA

0	11	2	3	14		16		18	9		11	12	14	16
16	17		19		21	22	23	25	28	30	32	33	38	43
46	46	61	63	41										

30070 - 60007-4

STM	REVISIONS	APPROVED	DATE
A	AS ISSUED	05	7/27/76
B	"ASSY. QTY. WAS #10. PER DEC"		3-7-78
C	PRCR#Q. ADD ITEM 11.	WDJ	3-28-78



ITEM	QTY	MATERIAL DESCRIPTION	MFG. PART NO	MFG. FINISH NO	MFG. SPEC
11	1	LABEL WARNING	7120-1827		
10	2	SCR PH #6-32 x .750	2680-0167		
9	2	LKWSHR #10 HEL	2190-0024		
8	2	WSHR #10 SS	3050-0022		
7	4	SCR FH #6-32 x .500	2680-0118		
6	2	BRKT-MTG	30070-00032		
5	1	SUPPORT- P.D.B.	30070-00033		
4	11	SCR #6-32 x .375 W/LOCK	2360-0117		
3	11	WSHR #6 SS	3050-0228		
2	1	PCA-PWR DIST BD	30070-60016		
1	1	POWER SUPPLY	6231ZF-002		

ASSY- PS TO PWR DIST PCA

NEXT ASSEMBLY 30070-60065

HEWLETT PACKARD

PART NUMBER 30070-60007

D SIZE CODE IDENT -4

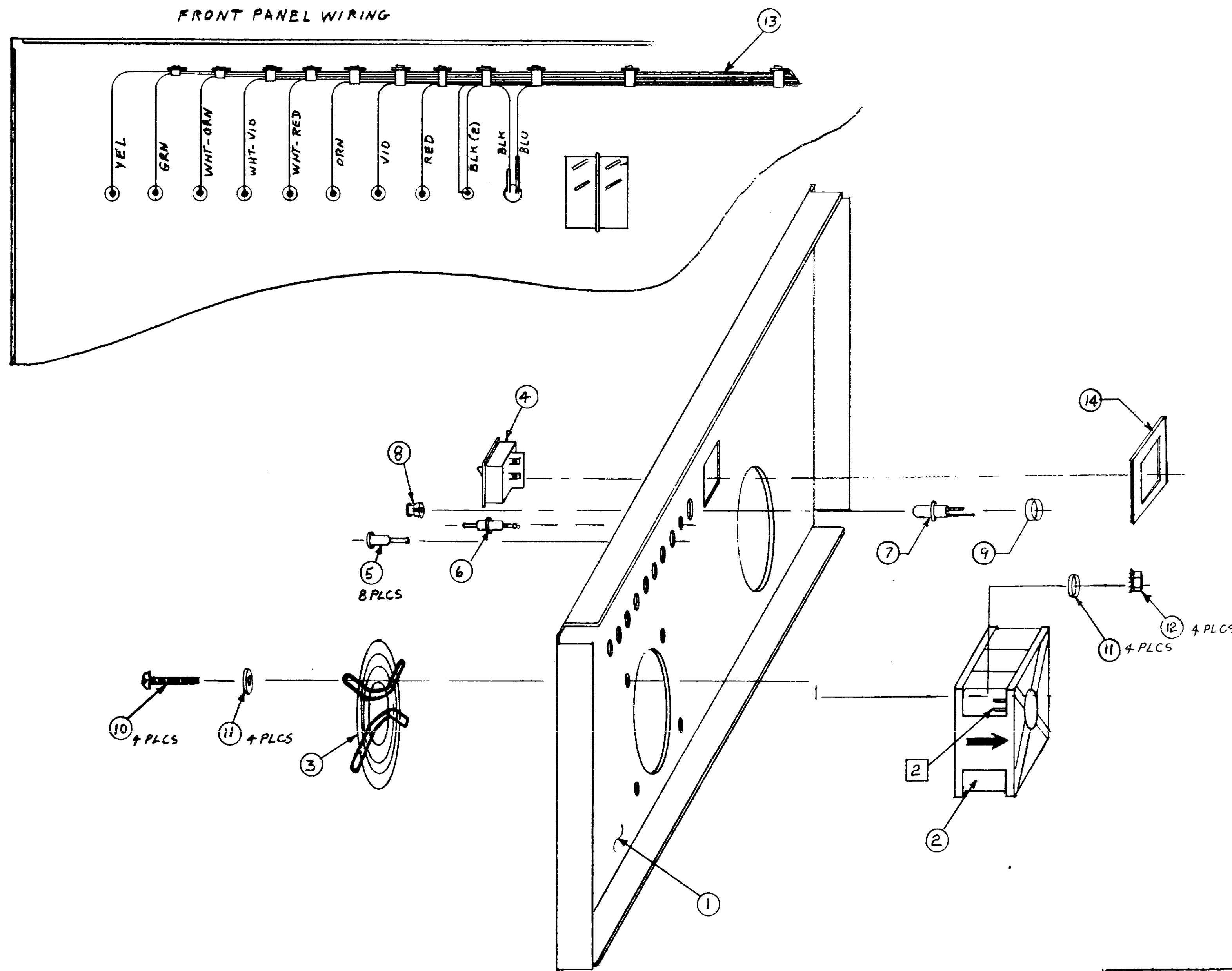
SHEET 1 OF 1

STOCK NO. 5180-0004 PRINTED ON DIEPO NO. 1035 IB CLEARPRINT FADEOUT

C-30070-60007-5

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		1/13/78
B	ADD ITEM 14. CHG WIRE LOCATIONS PRCR		3/9/78
C	ITEM 2 WAS 3160-0294 PC047-1562		10/24/78

FRONT PANEL WIRING



14	1	SHIM	30070-00120		
13	1	CABLE TEST POINT	30070-60023		
12	4	NUT-HEX-W/LKWR 6-32	2420-0001		
11	8	WASHER FLT.	3050-0227		
10	4	SCREW 6-32 X .725	2360-0125		
9	1	RING-RETAINING	1400-0540		
8	1	CLP/HLDR-CMPNT	1400-0547		
7	1	DIODE LIGHT EMIT	1990-0325		
6	1	TERMINAL FEED THRU	0340-0095		
5	8	CONN. TEST POINT	1251-0367		
4	1	SWITCH-ROCKER	3101-2281		
3	1	FAN GRILLE	3160-0092		
2	1	FAN	3160-0327		
1	1	PANEL FRONT	30070-00026		
ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE: ASSY & WIRING FRONT PANEL

HEWLETT PACKARD

NEXT ASSEMBLY: 30070-60065

PART NUMBER: C-30070-60007-5

FINISH: — SCALE: —

SHEET 1 OF 1

STOCK NO 9280-0003 PRINTED ON DIEPO NO 1030-10 CLEARPRINT FADEOUT

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	[illegible]
B	ADD P7-3 IEL PCL 4-14-7	[illegible]	6-16-78

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	83	41										

FROM			TO						
P11			P6	P8	P9	P11	P10	RESISTORS	P12
	1	GND			8				
	2	+5			5				
	3	-12		11					
	4	+12	12						
	5	PFW	6						
	6	PCN	9					R4 10K	10 (PON)
	7	UV							
	8	E5							
	9	+BIAS							
	10	E4						R3 10K	9 (BATT)
P7	⚠ 3								
	4	B1					1		
	7	B2					2		
	10	5M		5					
	11	-12M			11				2 (-12M)
	12	+12M			12				3 (+12M)
	13	5M		6					4 (5M)
	14	GNDM		8				R1 1K	
	15	GNDM		9					
								R2 330	8 (LED)
P13									
	1	5S	5						7 (5S)
	2								
	3	5RS	8						1 (5RS)
	4								
	5	E4					10		
	6	+BIAS					9		
	7	UV					7		
P14									
	1	+12S		12					6 (+12S)
	2,3,4	+12V	10	10	10				
	5,6,7,8	±12R	7	7	7				
	9	±12RS			9				
	10,11,12	-12V	4	4	4				
	14	-12S	11						5 (-12S)
	15	E5					8	R1 1K	
+5V			1,2,3	1,2,3	1,2,3				
+5R			13,14,15	13,14,15	13,14,15				

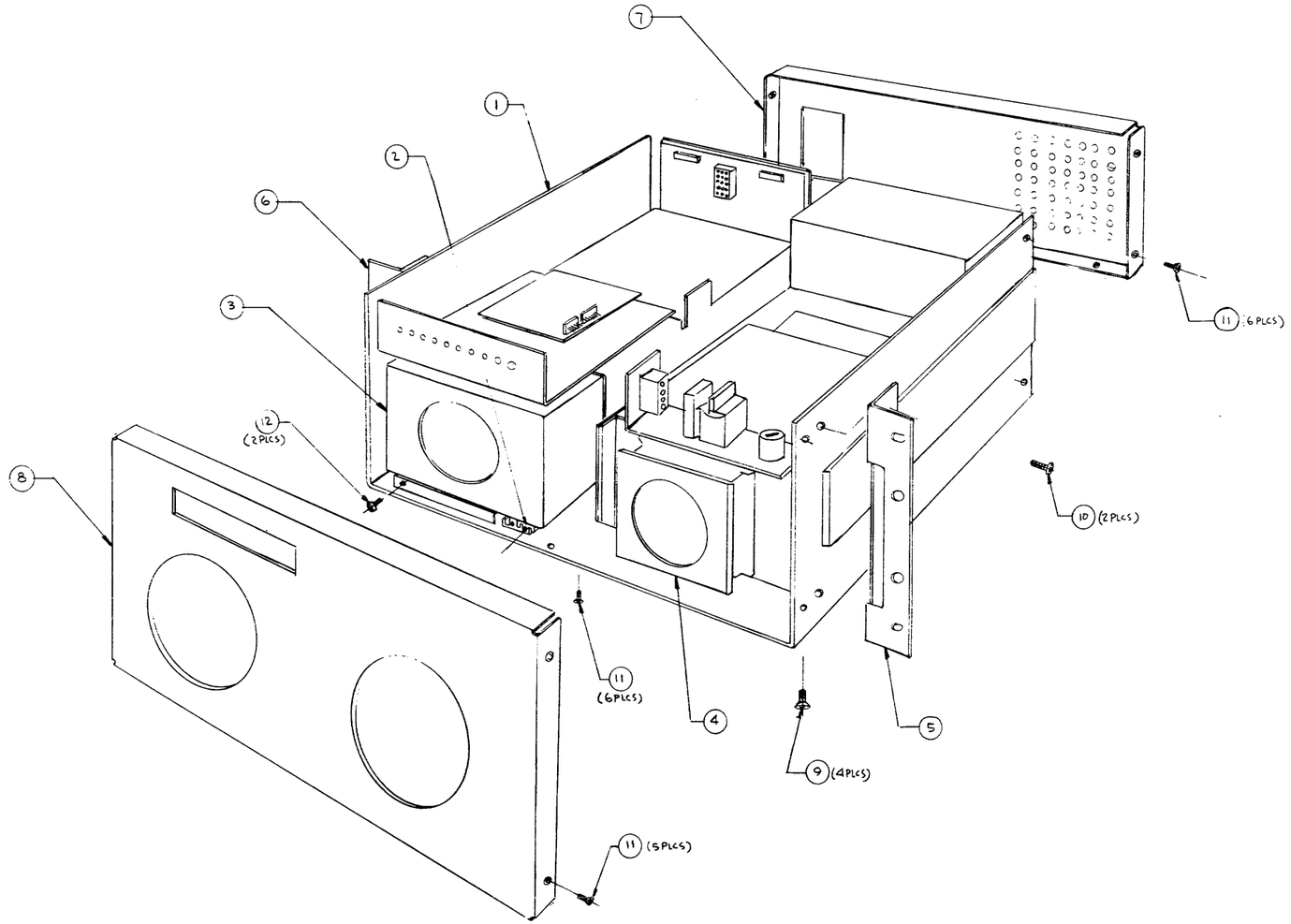
NOTES
1. R1 IS 1810-0037, R2-4 ARE 1/4W, 5% ALL RESISTORS IN OHMS

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO.	MAT'L CAGE NO.	MAT'L SPEC.

ENGINEERING RESPONSIBILITY	SEPIA

REVISIONS			
SYM		APPROVED	DATE
A	AS ISSUED		5 NOV

D - 30070 - 60078-1



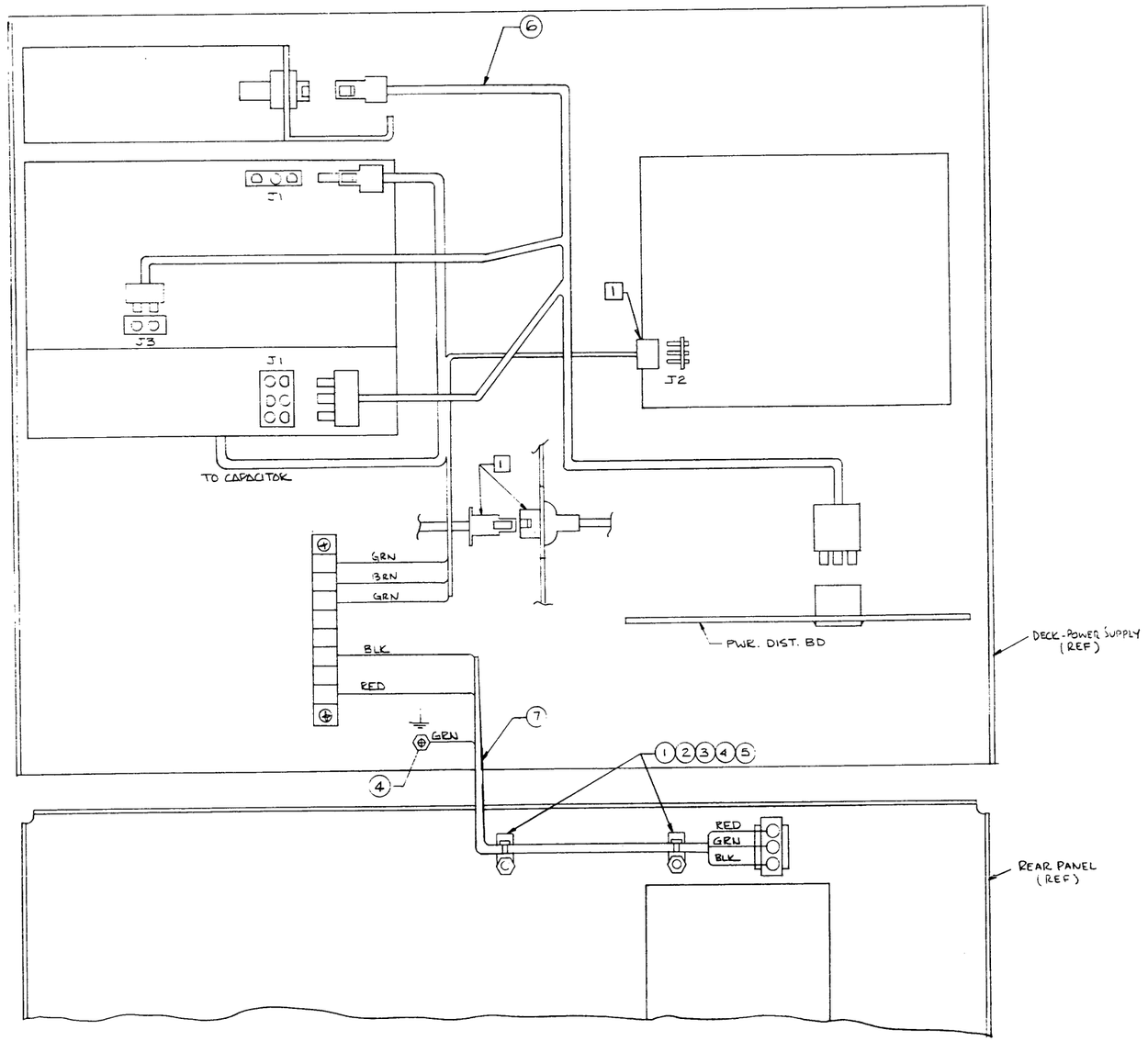
ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
15					
14					
13					
12	2	SCREW - RB 6-32 x 3/8 PH	2360-0155		
11	17	SCREW - RB 6-32 x 3/8 FH 82°	2360-0183		
10	4	SCREW - RB 6-32 x 3/8 PH	2510-0065		
9	4	SCREW - RB 6-32 x 3/8 FH 82°	2686-0178		
8	1	PANEL - FRONT	30070-00127		
7	1	PANEL - REAR	30070-00128		
6	1	MTG RAIL - LH	30070-00131		
5	1	MTG RAIL - RH	30070-00130		
4	1	ASSY - BATT BACKUP MODULE	30070-00080		
3	1	ASSY - PDE MODULE	30070-00079		
2	2	CORD - PDC	8120-1351		
1	1	CHASSIS - SHEET METAL	30070-00129		

TITLE	ASSY. POWER SUPPLY
NEXT ASSEMBLY	30070 A
FINISH —	SCALE NONE
	HEWLETT PACKARD
PART NUMBER	30070-60078
	D - 30070 - 60078-1

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY / SEPIA															
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
56	46	61	63	67											

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	5/30/78



NOTES:

[1] INTERBAY POWER CONNECT CABLES SHOWN AS REF. ONLY.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
7	1	POWER CABLE - REAR PANEL	30070-60082		
6	1	INTER-MODULAR CABLE	30070-60081		
5	2	SCR #6-32 x 3/8 PH W/LK	2360-0117		
4	3	NUT #6-32 W/LK	2420-0001		
3	2	WSHR #6 FLAT	3050-0227		
2	2	CABLE TIE	1400-0249		
1	2	MTG - CABLE TIE	0400-0186		

TITLE: ASSY- POWER SUPPLY WIRING

NEXT ASSEMBLY: 30070A

FINISH: —

DO NOT SCALE

HEWLETT PACKARD

PART NUMBER: 30070-60078

D-30070-60078-2

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 16	
18 17 19 21 22 23 25 29 30 32 33 38 43	
48 46 61 63 81	

D - 30070 - 60079 - 1			
SYM	REVISIONS	APPROVED	DATE
A	AS RELEASED		3-76

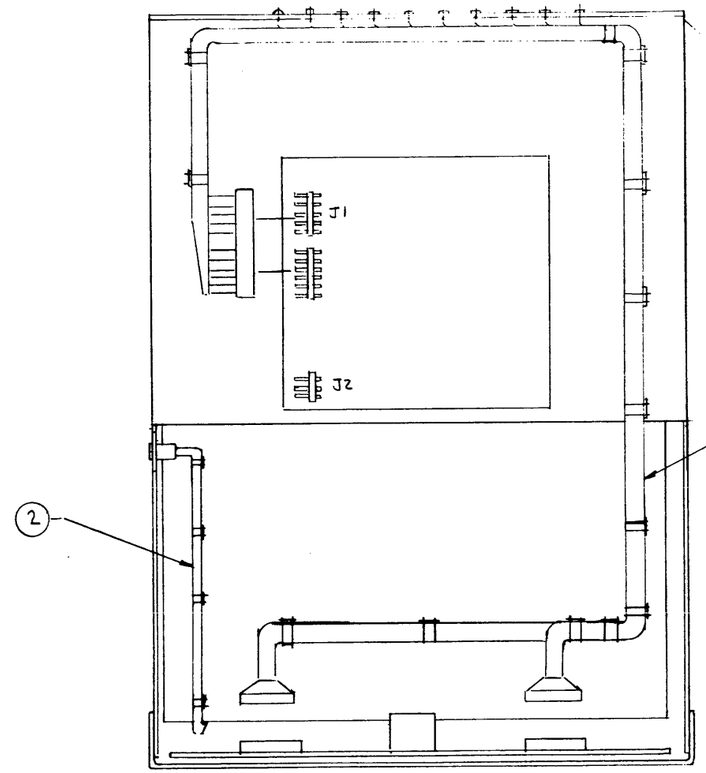
ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
21	4	WSHR-FLAT #6	3050-0227		
20	4	MTG - CABLE TIE	1400-0756		
19	2	WASHER - LOCK #10	2190-0034		
18	2	WASHER - FLAT #10	3050-0226		
17	23	SCREW - #6-32 x .312 PH W/LOCK WASH	2360-0115		
16	10	SCREW - #6-32 x .375 FH (82°)	2360-0183		
15	4	SCREW - #10-32 x .50 FH (100°)	2680-0104		
14	2	SCREW - #10-32 x .75 PH	2680-0107		
13	8	CONNECTOR - TEST POINT	1251-0367		
12	1	TERMINAL - FEED THRU	0340-0095		
11	1	RETAINING RING	0400-0540		
10	1	CLIP/HOLDER	1400-0547		
9	1	DIODE - LIGHT EMITTING	1990-0315		
8	1	PCB - POWER CONT	31000-60056		
7	1	BRACKET - TEST POINT	30070-00134		
6	1	BRACKET - DIST BOARD	30070-00133		
5	1	PCB - POWER DIST	30070-60016		
4	1	POWER SUPPLY	63312F-P02		
3	1	BRACKET - CLAMP	30070-00135		
2	2	GUIDE	30135-40001		
1	1	DECK - P02	30070-00132		

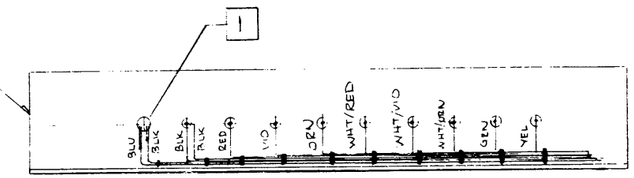
TITLE: ASSY - P02 MODULE	HEWLETT PACKARD
NEXT ASSEMBLY: 30070-00010	PART NUMBER: 30070-60079
FINISH: —	SCALE: 1:2.5
	D - 30070 - 60079 - 1
	SHEET 1 OF 1

ENGINEERING RESPONSIBILITY															SEPIA
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63		A										

SYM	REVISIONS	APPROVED	DATE
A	A	MK	

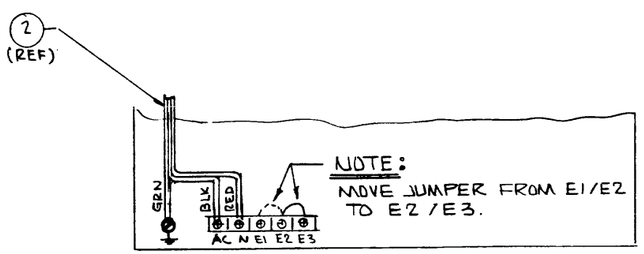
C - 30070 - 60079 -2





TEST POINT WIRING

1 HOOKUP BLU LEAD TO LONG PIN OF LED.



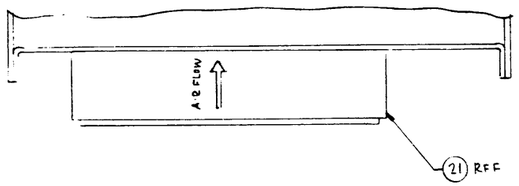
REAR VIEW P02

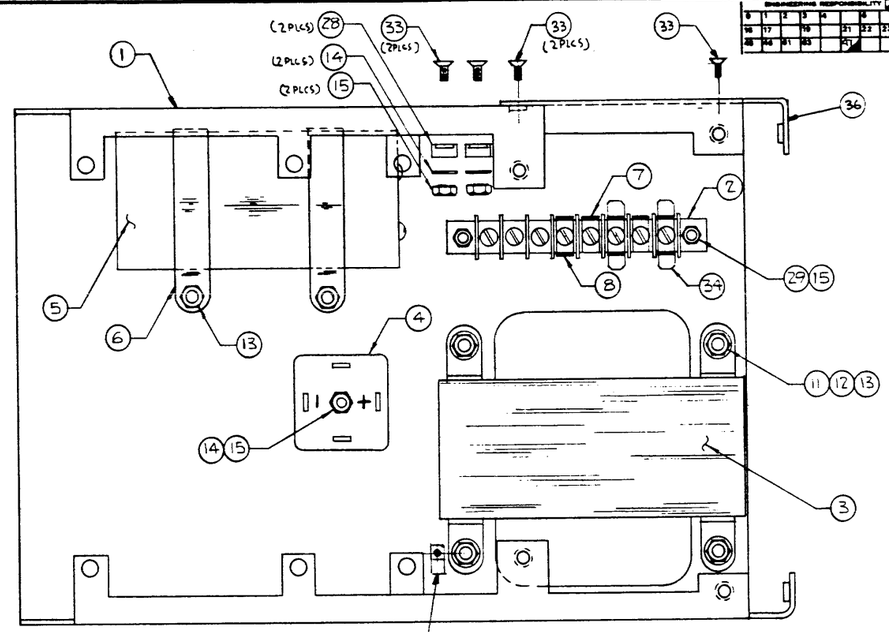
ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
2	1	CABLE - P02 POWER	30070-60083		
1	1	CABLE - TEST POINT	30070-60084		

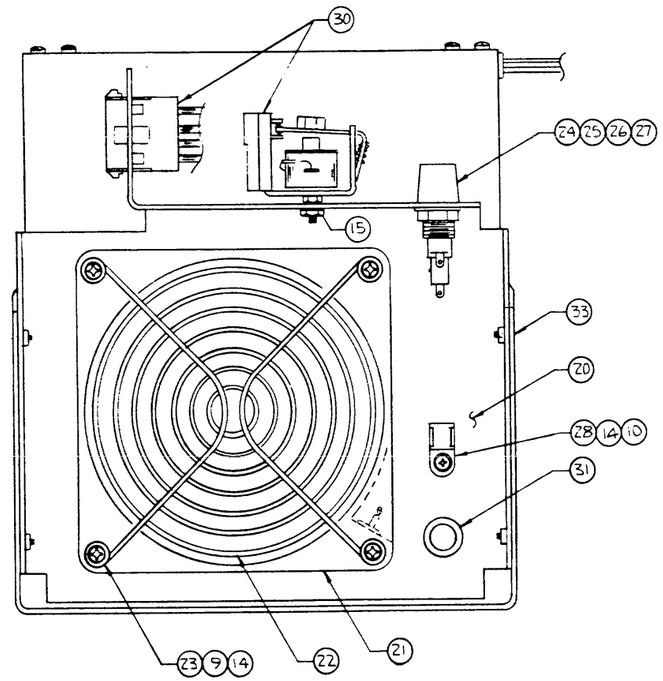
TITLE	WIRING - P02 MODULE
NEXT ASSEMBLY	30070-60079-1
FINISH	NONE
SCALE	NONE
PART NUMBER	30070-60079
	C - 30070 - 60079 -2
	SHEET 1 OF 1

HEWLETT PACKARD

STOCK NO 9280-0003 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT







ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
36	1	BRACKET- DECK	30070-00144		
35	4	LOCK WASHER - #8	2190-0073		
34	2	STRAIGHT TAB (BARRIER)	0360-0324		
33	10	SCREW 6-32X.312 FH	2360-0182		
32	1	CABLE - PRE REG	30070-60004		
31	1	GROMMET .375 I.D	0400-0056		
30	1	CABLE/RELAY ASS'Y	30070-60089		
29	2	SCREW 6-32X.625 FH	2360-0210		
28	4	MOUNT-CABLE TIE	1400-0786		
27	1	FUSE 5A NB	2110-0010		
26	1	FUSE HEX NUT	2110-0580		
25	1	FUSE CAP	2110-0565		
24	1	FUSE HOLDER	2110-0564		
23	4	SCREW 6-32X.875	2360-0318		
22	1	GRILLE	3160-0090		
21	1	FAN	3160-0327		
20	1	BRKT- FAN MTG	30070-00137		
9	4	SCREW 8-32X4.00	2520-0014		
8	1	BATTERY PACK	3000-6002		
7	1	PC BD-MEM PRE REG	31000-60067		
6	1	PC BD-MEM REG	31000-60028		
5	7	HEX NUT 6-32 W/LK	2420-0001		
4	9	FLAT WASHER #6	3050-0227		
3	6	HEX NUT 8-32 W/LK	2580-0003		
2	8	FLAT WASHER #8	3050-0061		
1	4	SCREW 8-32X.50 FH	2520-0123		
10	1	SCREW 6-32X.312 W/LK	2360-0115		
9	4	SPLIT WASHER #6	2190-0006		
8	3	DOUBLE TAB (BARRIER)	0360-0264		
7	2	SINGLE TAB (BARRIER)	0360-0263		
6	2	CLAMP 2.0 IN	1400-0273		
5	1	CAPACITOR	0180-0757		
4	1	BRIDGE - FW	1906-0093		
3	1	XFRMR - PWR	9100-4066		
2	1	BARRIER BLOCK	0360-1970		
1	1	DECK-CHASSIS	30070-00136		

ASSEMBLY-BATTERY BACK UP (MECHANICAL)

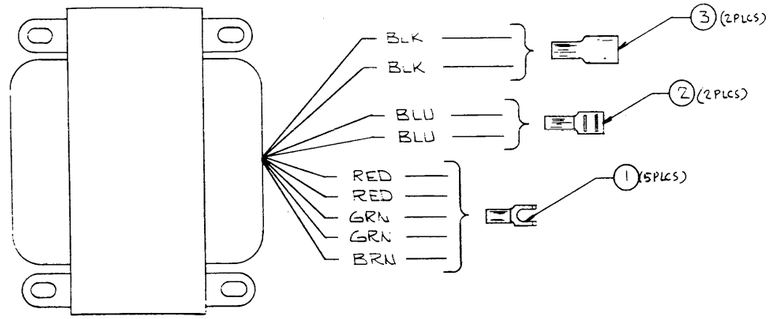
HEWLETT PACKARD

NEXT ASSEMBLY: 30070-60078

PART NUMBER: D-30070-60080-1

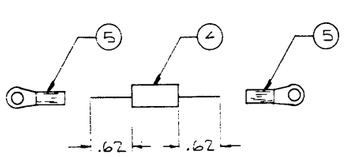
FINISH: —— SCALE: 1/1

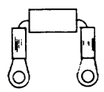
SHEET 1 OF 1



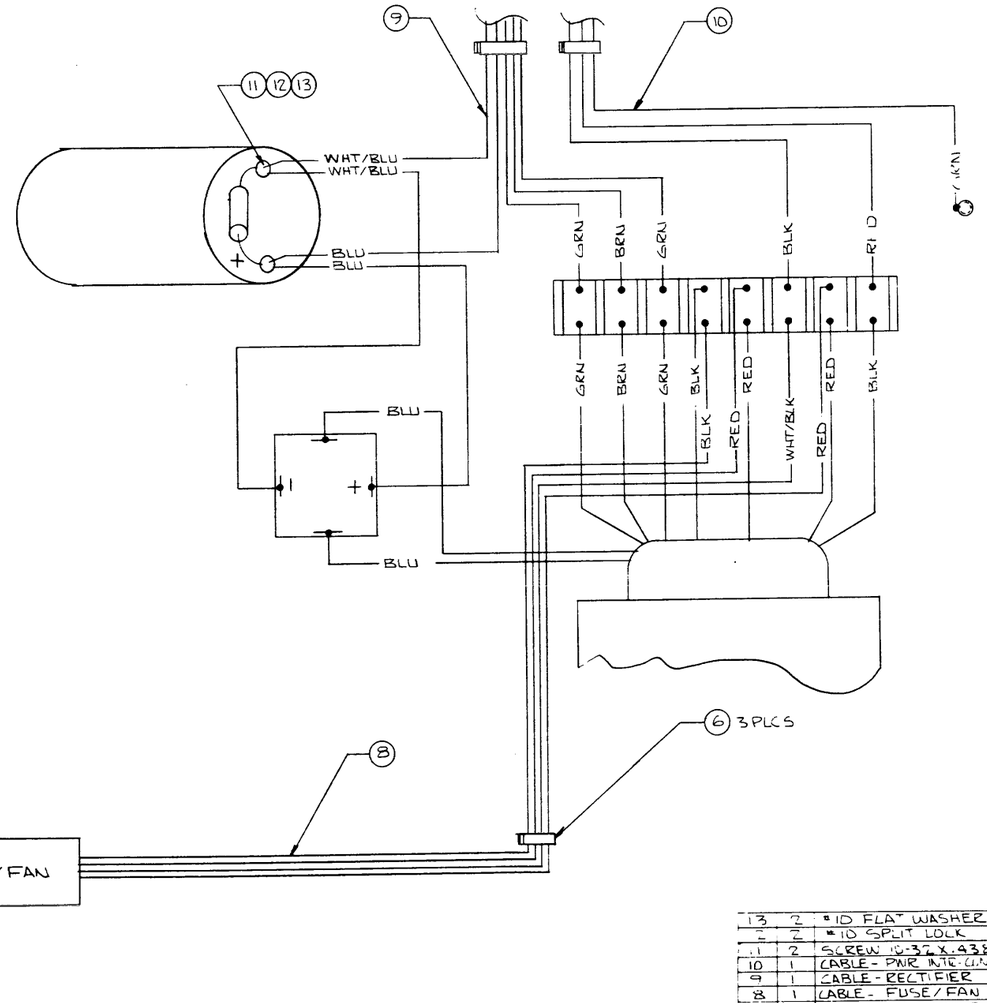
TRANSFORMER PREPARATION

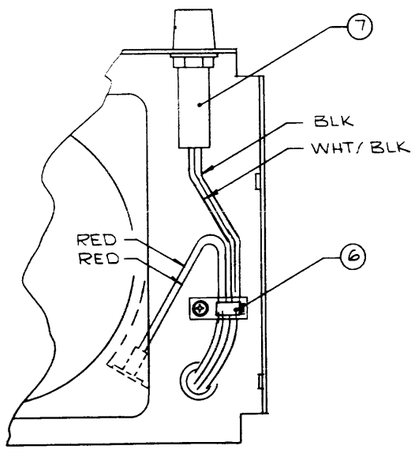
LEAD (COLOR) IS TYPE OF CRIMP TERMINATION





RESISTOR PREPARATION





FUSE - FAN CONNECTIONS

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
13	2	#10 FLAT WASHER	3050-0066		
12	2	#10 SPLIT LOCK	2190-0034		
11	2	SCREW 10-32 X .438	2680-0101		
10	1	CABLE - PWR INTF (AC)	30070-60085		
9	1	CABLE - RECTIFIER	30070-60086		
8	1	CABLE - FUSE/FAN	30076-60087		
7	A/R	SHRINK TUBING BLK	8890-0301		
6	4	TIE WRAP SM	1400-0248		
5	2	LUG 22-18AWG RED	0362-0319		
4	1	RES 4.7K 5% 2W	3704-0015		
3	2	LUG 16-14AWG BLU	0362-0254		
2	2	LUG 16-14 AWG BLU	0362-0353		
1	5	LUG 22-18AWG RES	0362-0317		

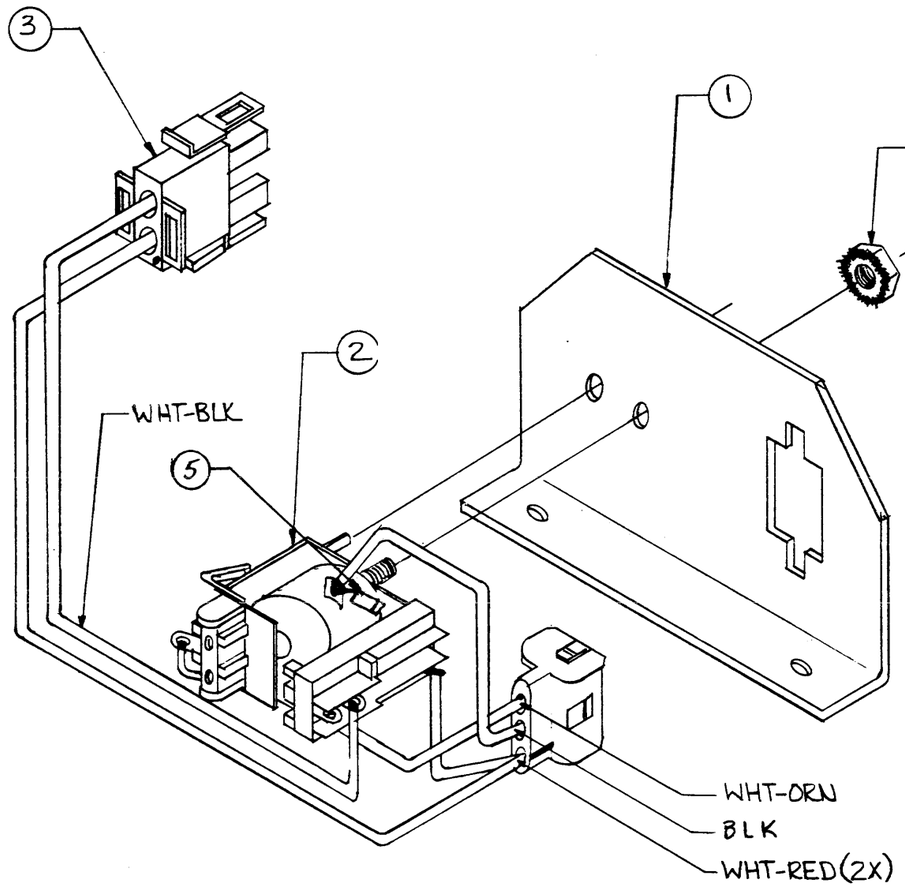
TITLE: ASSEMBLY - BATTERY CHARGER (WIRING)
NEXT ASSEMBLY: 30070-60080
FINISH: — SCALE: —
HEWLETT PACKARD
PART NUMBER: 30070-60080
D-30070-60080-2
SHEET 1 OF 1

B-30070-60071-1

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	47											

SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	JO	5-24-78 M
B	REVISED PER PCO 47-1463	[illegible]	8-9-78 M



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
5	1	DIODE	1901-0033		
4	1	NUT W/LK #6-32	2420-0001		
3	1	CABLE ASSY.	30070-60072		
2	1	RELAY	0490-1188		
1	1	MTG BRACKET- RELAY	30070-00125		

TITLE: POWER SUPPLY RELAY ASSY

HEWLETT hp PACKARD

NEXT ASSEMBLY: 30070-60007

PART NUMBER: 30070-60071

FINISH: ——

SCALE: ——

B-30070-60071-1

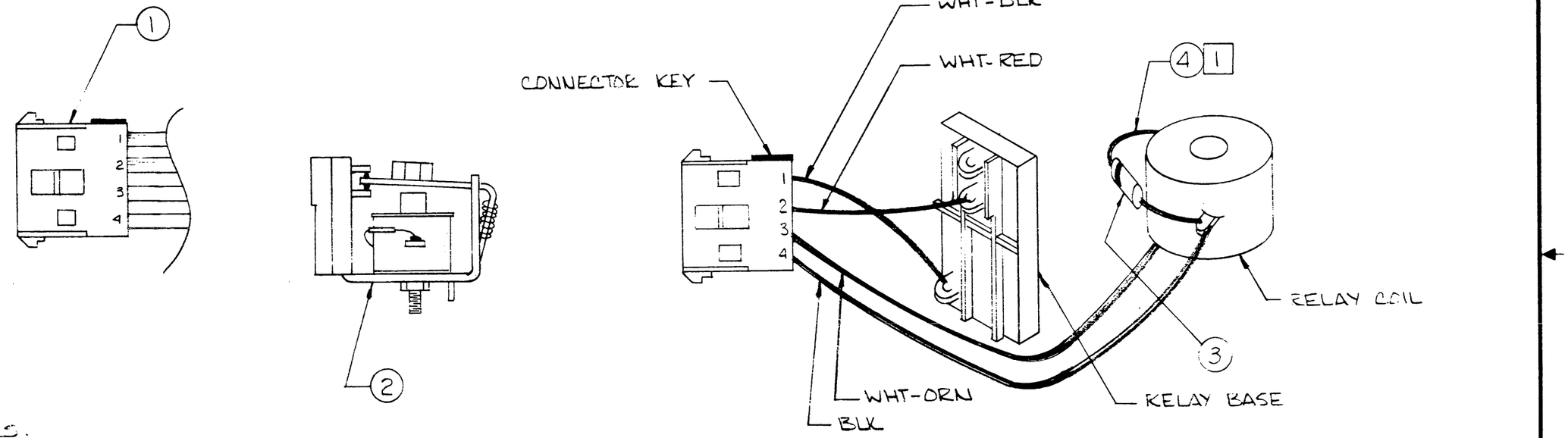
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	47											

SEPIA

SYM	REVISIONS	APPROVED	DATE
A	ECO [illegible]	[illegible]	[illegible]

B - 30070 - 60039 - 1



NOTES:

1. ATTACH WHT-ORN WIRE TO EDGE OF DIODE WITH STRIPE AS SHOWN

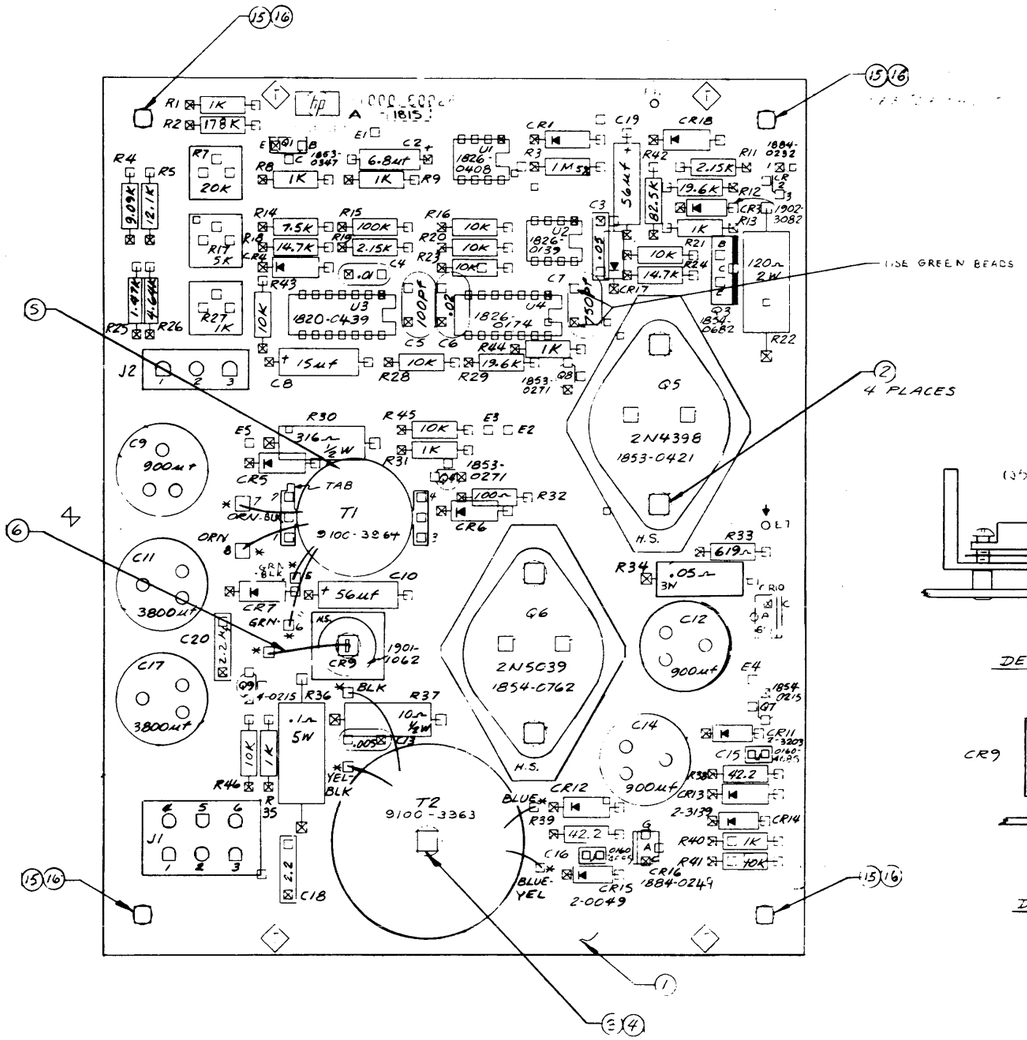
ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
4	A/R	TUBING	0890-0228		
3	1	DIODE	1901-0033		
2	1	RELAY	0490-1156		
1	1	CABLE ASSY.	30070-60088		

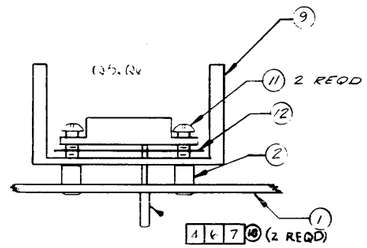
TITLE: ASSY - CABLE / RELAY	HEWLETT PACKARD
NEXT ASSEMBLY: 30070-60030	PART NUMBER: 30070-60039
FINISH: ———	SCALE: NONE
	B - 30070 - 60039 - 1

SHEET OF

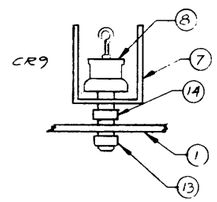
ENGINEERING RESPONSIBILITY	SEMA	ADJARD

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	C151 C16 WERE 0.06 CHANGED TO 0.1 PER ECR 31213A "N"		
C	ADDED NOTE 9 AND ITEM 17 PER ECR 31213A "P"		
D			

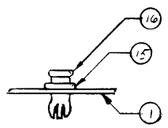




DETAIL A



DETAIL B



DETAIL C

NOTES:
1. UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ⅛W 1%.
ALL CAPACITANCE IN MICROFARADS
ALL DIODES ARE 1901-1065.

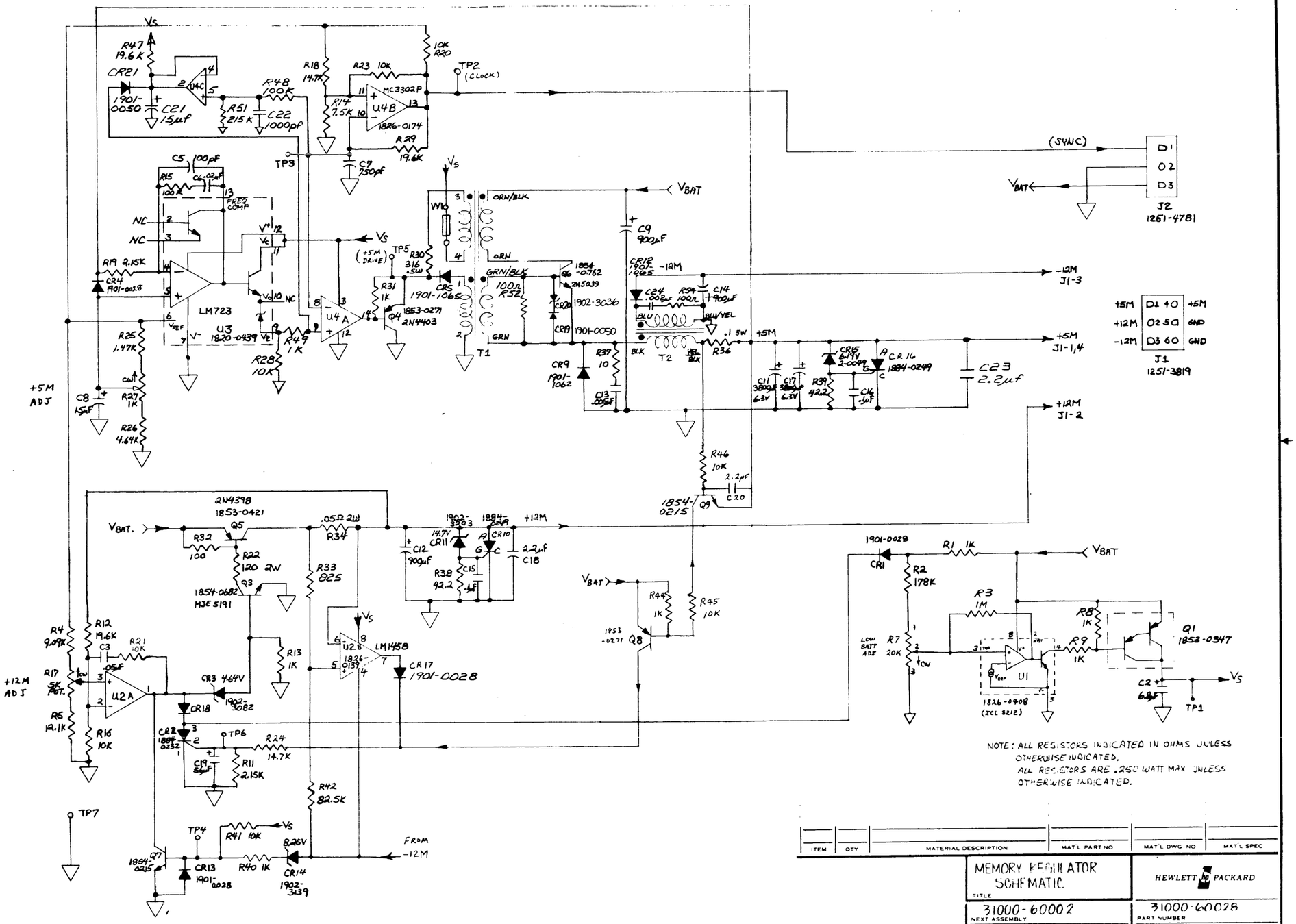
ITEM	QTY	MATERIAL/DESCRIPTION	MFG. PART NO.	MFG. NAME	MFG. SPEC
16	4	NYLATCH KLIK-IC	0380-0236		
15	4	NYLATCH GROMMET	0380-0360		
14	1	NUT IC 32	2740-0002		
13	1	NUT IC 32 W/LOCK	2740-0003		
12	2	THERMAL WASHER	0340-0815		
11	4	SCREW 6-32 .75	0360-0119		
10	4	XSTR SOCKET	1251-2913		
9	2	HEAT SINK	1205-0289		
8	1	DIODE	1901-1062		
7	1	HEAT SINK	02108-00028		
6	1	WIRE JUMPER 1/2 WHT	8150-2604		
5	1	XFMR T1	9100-3264		
4	1	XFMR T2	9100-3363		
3	1	HEAT SINK	1205-0201		
2	4	SPACER	0380-0342		
1	1	PC BOARD ETCHED	02108-60028		

HEWLETT-PACKARD

D

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED PCA7-2071	NM	9-2178

ENGINEERING RESPONSIBILITY — SEPIA — APERTURE CD



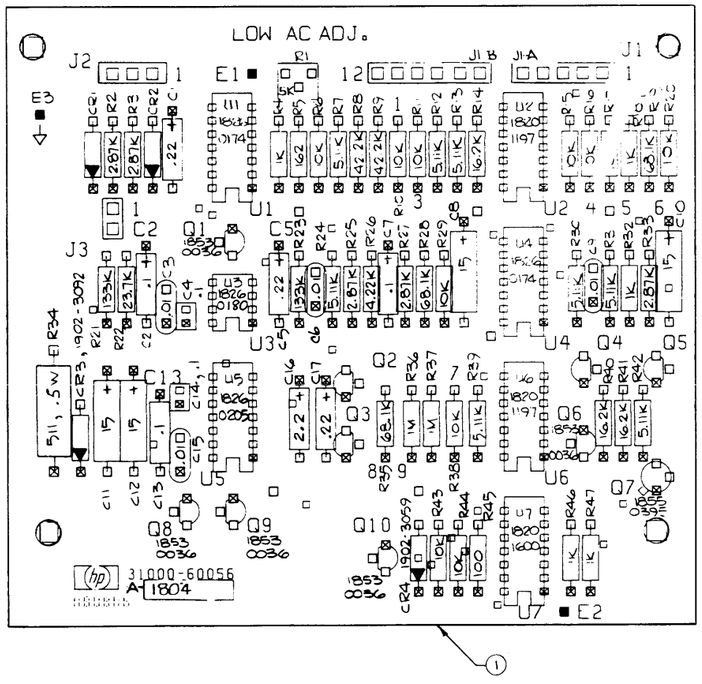
NOTE: ALL RESISTORS INDICATED IN OHMS UNLESS OTHERWISE INDICATED.
ALL RESISTORS ARE .25Ω WATT MAX UNLESS OTHERWISE INDICATED.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE: MEMORY REGULATOR SCHEMATIC	HEWLETT PACKARD
NEXT ASSEMBLY: 31000-60002	PART NUMBER: 31000-60028
FINISH / SCALE	C-31000-60028-16

SHEET 1 OF 1

STOCK NO. 5280-0003 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT



NOTES UNLESS OTHERWISE SPECIFIED

1. ALL RESISTANCE VALUES ARE IN OHMS ± 1%, 1/4W.
   ALL CAPACITANCE VALUES ARE IN MICROFARADS.
   ALL TRANSISTORS ARE 1854-0215
   ALL DIODES ARE 1901-0050

ENGINEERING RESPONSIBILITY	DEPT.

ITR	REVISIONS	APPROVED	DATE
A	AS ISSUED		1-26-78

D-31000-60056-1

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO.	MAT'L UNIT NO.	MAT'L SPEC
2		ASSY-MAINFRAME	7120-6830		
1		PC BOARD, ETCHED	31000-60056		

TITLE: ASSEMBLY - POWER CONTROL	HEWLETT PACKARD
NEXT ASSEMBLY: 31000-60002	PART NUMBER: 31000-60056
FINISH	SCALE: 2/1
	D-31000-60056-1
	SHEET OF

STOCK NO. 5060-0864 PRINTED ON DIEPO NO. 1030-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY	SIZE	APERATURE CODE
0 1 2 3 4 6 8 9 11 12 14 16		
18 17 19 21 22 23 25 29 30 32 33 38 43		
46 44 41 43 45 47 49 50		

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED A-1804	[illegible]	26 JAN 79
D	REVISED: DATE CODE WAS 1804, PLS7-2019 A-1840	KS	10-16-79

5061-31000-60056-6

1. ALL RESISTORS 1/4W, 1% UNLESS OTHERWISE SPECIFIED
2. ALL CAPACITANCE IN MICROFARADS
3. WHEN OPERATING THE HP300 SYSTEM WITH INPUT LINE VOLTAGES AT 100 VOLTS RMS OR LOWER, CERTAIN TIMING COMPONENTS ON THIS BOARD MUST BE CHANGED TO ALLOW PROPER SENSING OF LOW LINE CONDITIONS AND RESULTING POWER FAIL WARNING OPERATION. THE CHANGES REQUIRED ARE AS FOLLOWS:
   - RZ3 121K 0757-0461
   - RZ1 909K 0757-0464

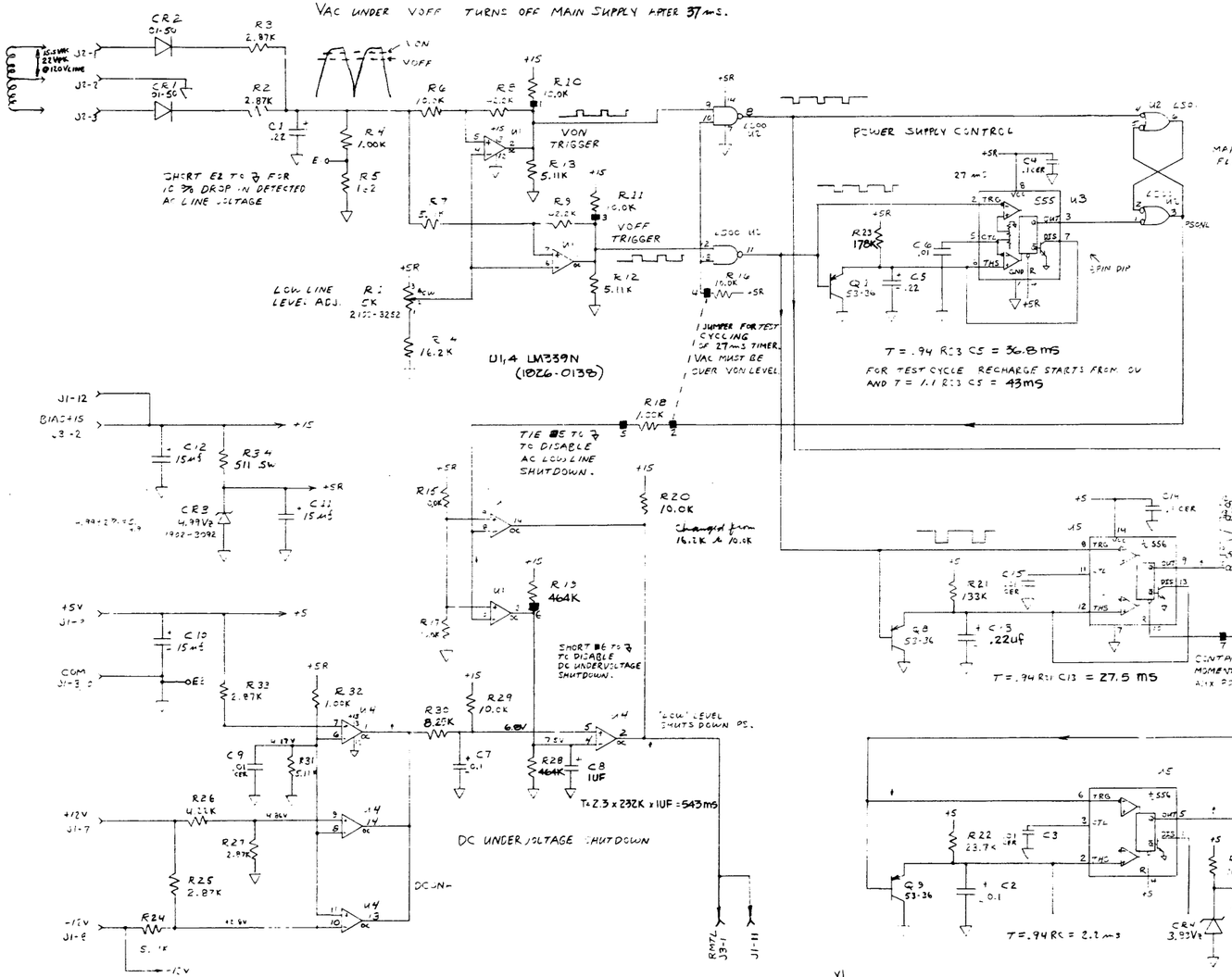
   CHECK WITH FACTORY SUPPORT PERSONNEL IF OPERATIONS UNDER THESE CONDITIONS ARE SUSPECTED.
4. THERE ARE OVERSIZE SQUARE RESISTOR PADS WITH NO OTHER TRACES UNDER THE RESISTOR LEAD ON THE COMPONENT SIDE. THESE POINTS ARE USED FOR CLIP LEADS DURING TEST ONLY.

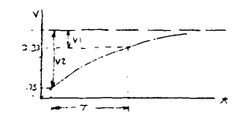
LOW LINE DETECTOR

VAC OVER VON TURNS MAIN SUPPLY ON AND ALLOWS PFWL AND LATER PONH TO GO 'HIGH'.

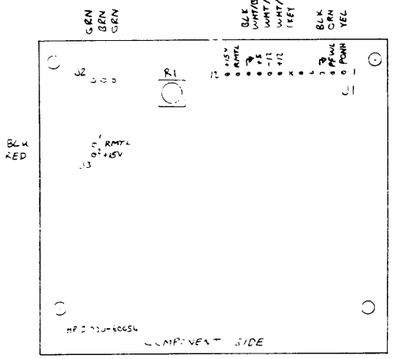
VAC UNDER VOFF CAUSES PFWL AND 2ms LATER PONH TO GO 'LOW'

VAC UNDER VOFF TURNS OFF MAIN SUPPLY AFTER 37ms.





$T = RC\left(-\ln\frac{.35}{V2}\right) = RC\left(-\ln\frac{.67}{4.5}\right) = .74RC$

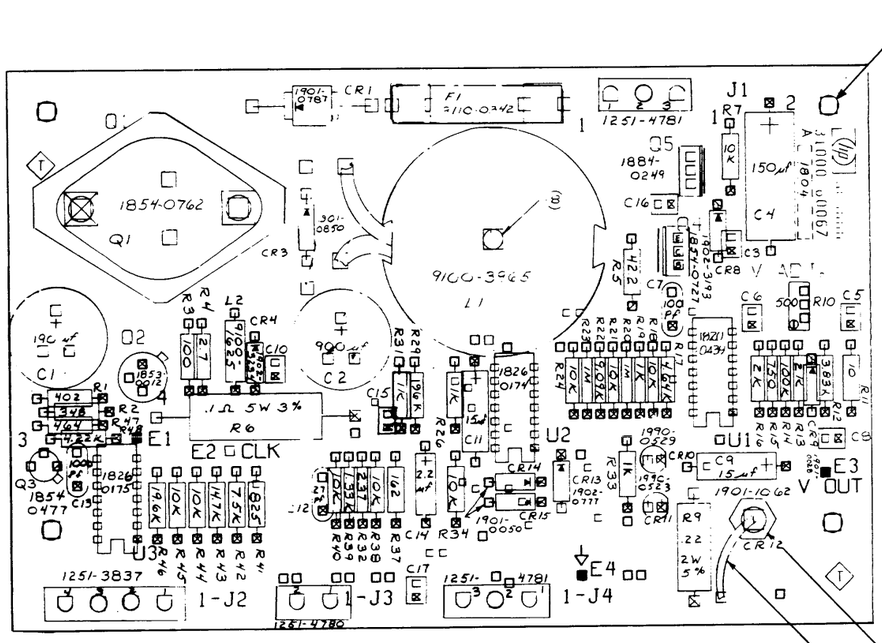


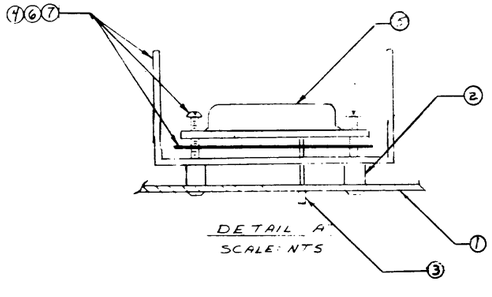
NOTES:
FOR TEST CYCLING OF PFWL & PONH,
i) TIE #5 TO 7 TO DISABLE LOW LINE SHUTDOWN, AND
ii) TIE E2 TO #4. [illegible] ABOVE VON.
FOR FASTER CYCLING, TIE #5 TO #9.
TO ACCURATELY MEASURE ONE-SHOT(S) T=MIN.:
SEE EXPONENTIAL WAVEFORM(S) ON T=1 VS
CAPS C5, C13, OR C2. ALL VALUES ARE ± 10%

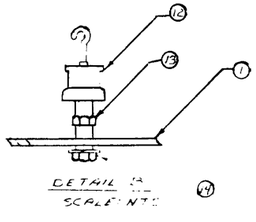
NOTE:
ARRIN & JE & [illegible] SIGNAL LEVELS AT NORMAL OPERATION

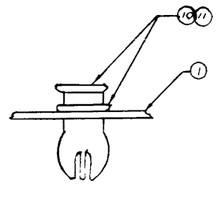
ITEM	QTY	MATERIAL DESCRIPTION	MATL MANUF	MATL DWG NO	MATL SPEC

[illegible]	HEWLETT PACKARD
[illegible]	PART NUMBER 31000-60056
[illegible]	D [illegible]









NOTES:

1. UNLESS OTHERWISE SPECIFIED:
   ALL RESISTANCE IN OHMS
   ALL RESISTORS 1/4 W, 1%
   ALL CAPACITANCE IN MICROFARADS
   ALL CAPACITORS .1 MICROFARADS

16	1	LABEL WARRANTY	7120-6830	
15	1	WIRE, JR PLUG 1½	P150 2664	
14	1	NUT, 6-32 w/LOCK	2740-0009	
13	1	NUT, 6-32	2740-0002	
12	1	DIODE CR 2	1901-1062	
11	4	SNAP IN GROMMET	0390-2366	
10	4	SNAP IN PLUNGER	0390-0365	
9	2	FUSE CL F 250 V 1.4	2110-0269	
8	1	NUT ¼-32 W/LK	2420-0001	
7	2	SCR #6-32 x .375 LG	0360-0117	
6	1	HEAT SINK	0340-0269	
5	1	TRANSISTOR	1854-0762	
4	1	WASHER	0340-0675	
3	1	[illegible]	[illegible]	
2	1	[illegible]	[illegible]	
1	1	PC BOARD ASSY	[illegible]	
ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DRG NO / MATL SPEC

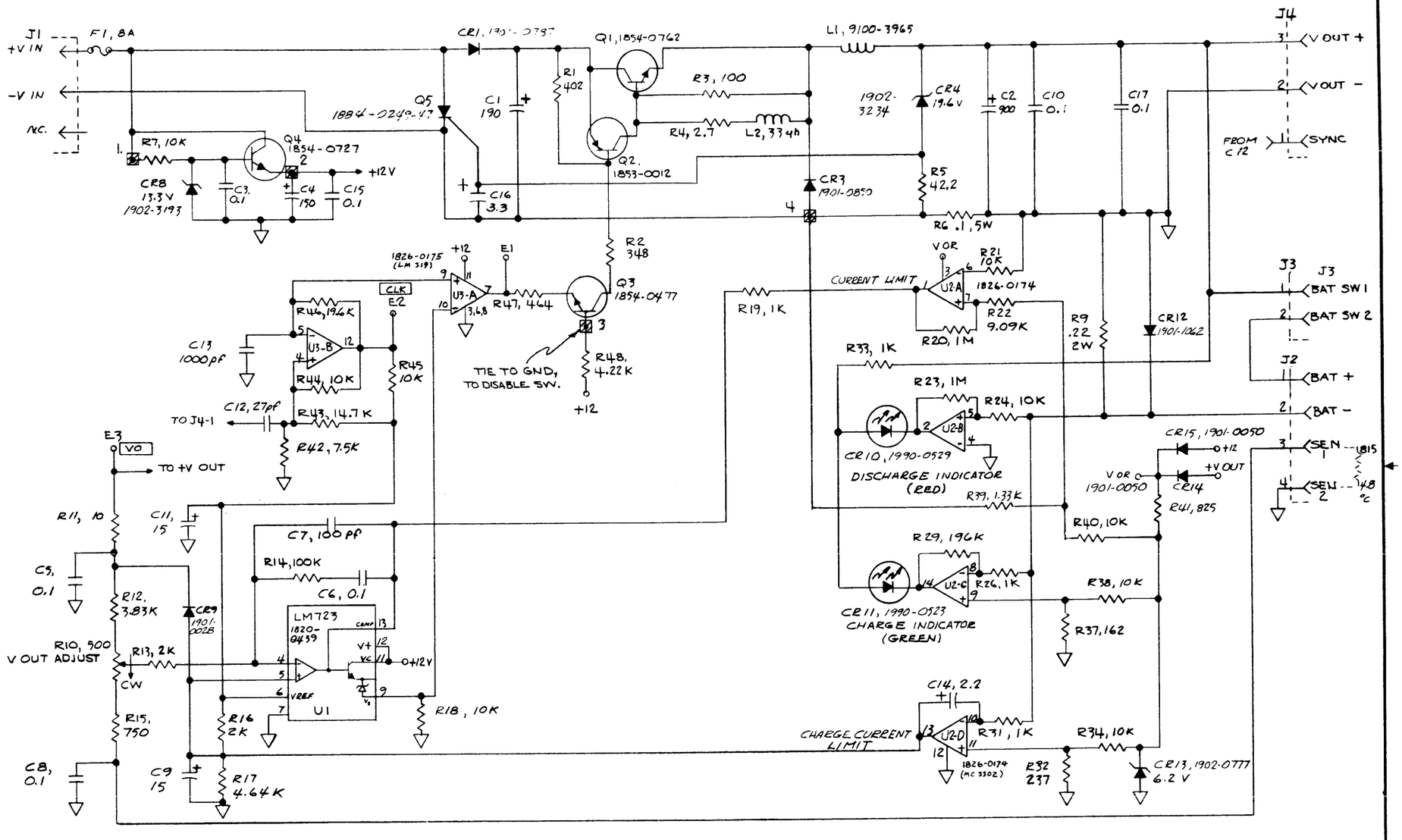
ENGINEERING RESPONSIBILITY	DEPT
0 1 2 3 4	6 8 10 12 14 16
16 17 18 31 32 33 35 36 50 52 53 54 43	
45 46 61 62 64	

ZONE	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	2-27-78
B	U1 MAY HAVE DIAG IN ERROR	KS/EM	4-6-78

31000-6004-7-1

HEWLETT PACKARD

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED A-1804		2-16-78
B	REVISED C16; DATE CODE WAS 1804 PCA7-2065 A-1833	KS	6-21-78



NOTE:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS 1/8 W ± 1%
ALL CAPACITANCE IN MICRO FARADS

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

MEMORY PREREGULATOR SCHEMATIC
TITLE

HEWLETT PACKARD

31000-60002
NEXT ASSEMBLY

31000 60067
PART NUMBER

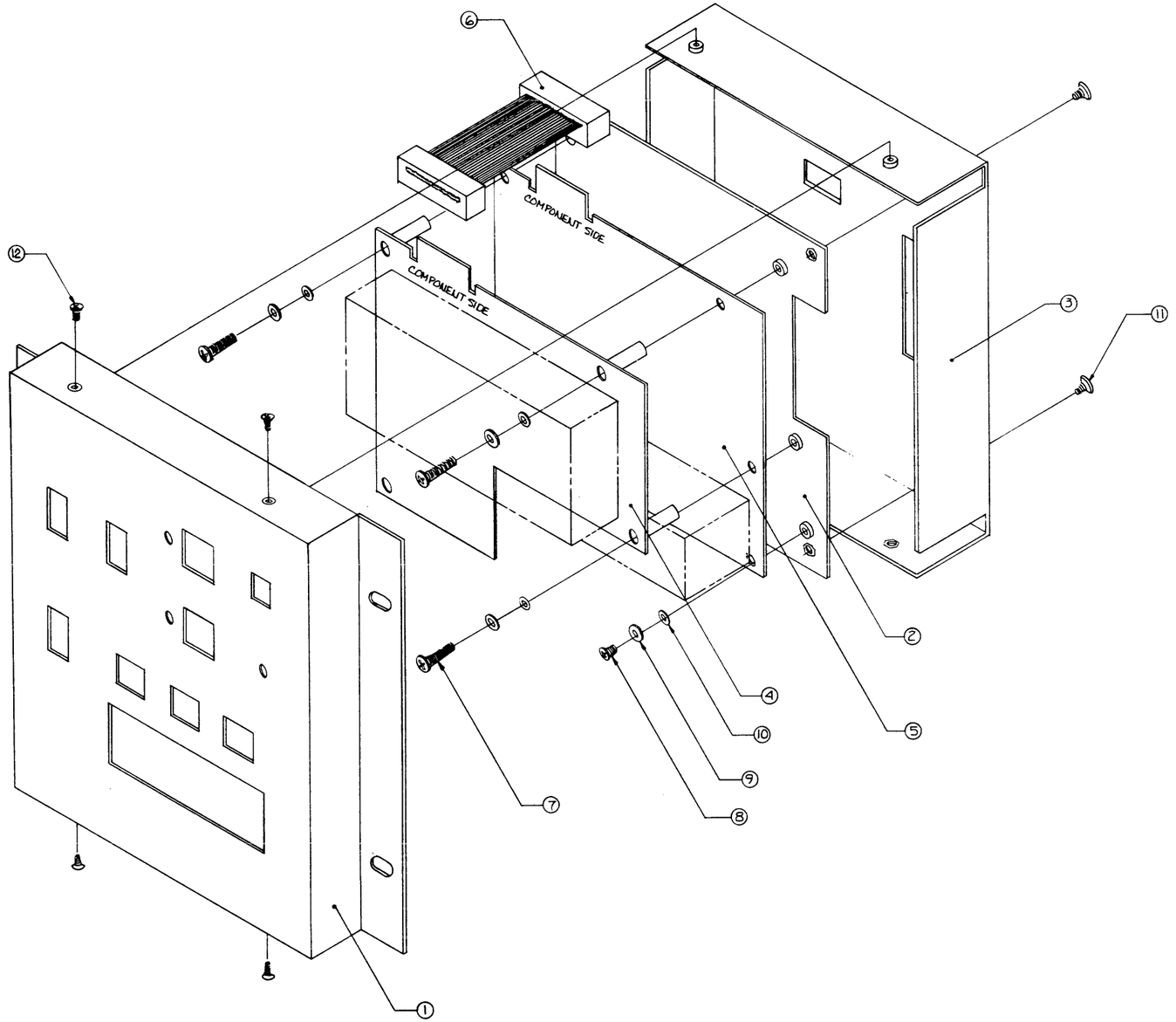
FINISH

SCALE NONE

C-31000-60067-6

SHEET 1 OF 1

STOCK NO 9280-0003 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT



ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
12	4	SCR FH 4-40 x .312 100°	2200-0142		
11	4	SCR 6-32 x .312 W/LOCK	2360-0115		
10	5	#4 FLAT WASHER	3050-0105		
9	5	#4 INT LOCK WASHER	2190-0004		
8	1	SCR 4-40 x .375	2200-0143		
7	4	SCR 4-40 x 1.250	2200-0123		
6	1	CABLE-JUMPER	30070-66029		
5	1	PCA-SCP LOGIC	30070-60009		
4	1	PCA-SCP SWITCH	30070-60010		
3	1	CHASSIS	30070-00053		
2	1	PLATE-ADJUSTMENT	30070-00023		
1	1	PANEL-SYSTEM CONTROL	30070-00024		

		SYSTEM CONTROL PANEL - ASSY	HEWLETT PACKARD
		30070-60065 NEXT ASSEMBLY	30070-60008 PART NUMBER
		FINISH / SCALE	D-30070-60008-1

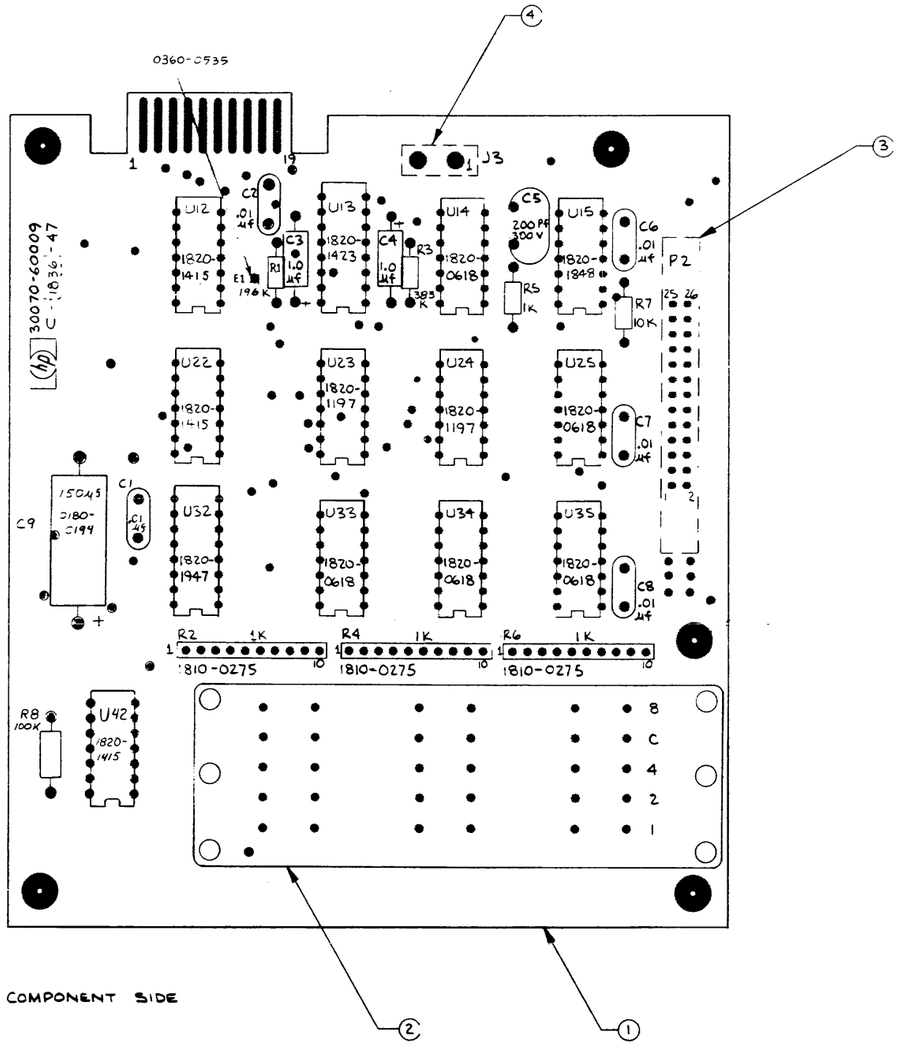
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY	SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63											

D-30070-60009-2

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	5/1/78
B	DATE CODE WAS 1810; PCO 47-1404	[illegible]	7/20/78
C	820-845 WAS 820-1199 REVISED NOTES 4 & 5 PL & DOC CHG	[illegible]	7/11/78
D	REVISED PER PCO 47-1466 (DATE CODE WAS 1813)	[illegible]	8-3-78



COMPONENT SIDE

NOTES:

1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE VALUES ARE IN OHMS
   ALL RESISTORS ARE .1/4 W ± 5%

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
4	1	CONNECTOR - J3	1251-4780		
3	1	CONNECTOR - P2	1251-3024		
2	1	SWITCH ASSY	3100-3458		
1	1	PCB-LOGIC	30070-80009		

TITLE: PCA-LOGIC ASSY		HEWLETT PACKARD
NEXT ASSEMBLY: 30070-60008		PART NUMBER: 30070-60009
FINISH: DRI-FILM	SCALE: 2:1	D-30070-60009-2

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY															
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	RK	7/1/78
B	PCO-47-1484 CIRCUIT CHG.	RK	7/28/78
C	ADDED J2-19 PER DOC. CHG. PCO-47-1966, CIRCUIT CHG. DATE CODE IS 1836	LF	9/13/78
D		cwy	10/6/78

B - 30070 - 60009 -51

FDBK

J2-19

FPDMP (FROM MI)

C1 .01μF

R7 10K +5

C5 200pF

U14

E1

U13

R1 196K

C3 1.0μF

RESET 1

FPRST P2-4

R2-7 1K

J2-6 RESET

J2-5 COLD LOAD

J2-1 WARM START

J2-3 MEM DUMP

U32

U12 U15 U22

RST

TRIGR

U23

LOAD 2

FPLD P2-5

R2-6 1K

U13

R3 383K

C4 1.0μF

LOAD 1

DMP 1

FPDMP P2-7

R2-5 1K

WARM START

MEMORY DUMP

COLD LOAD

THUMBWHEEL SWITCHES

CHL 1 DEV 2 CHL 3 DEV 4 CHL 5 DEV 6

R2, 1K R4, 1K R6, 1K

U33 U34 U35

U25

R6-3 1K

J2-4

U12 U24

R5 1K

WARM P2-6 (FROM MI)

FFLD (FROM MI)

FPLED P2-3

R6-2 1K

R6-7 1K

J2-11

J2-13

MSB DEV1 P2-11

DEV2 P2-12

DEV3 P2-13

MSB CHL1 P2-8

CHL2 P2-9

CHL3 P2-10

GND P2-21

GND P2-22

GND P2-23

GND P2-24

GND P2-25

GND P2-26

J2-14 R2-3 1K

J2-12 FFRUN P2-1

J2-8 FFHLT P2-2

J2-7 FPIO P2-17

J2-2 R2-2 1K ENMP P2-16

R2-4 1K OVERTMP P2-14

J2-9 J2-10 J2-18

J2-16 J2-17 +5V.

+5V. .01μF C2,6,7,8 DECOUPLING CAPACITORS

J3

U42

R8 100K C9 150μF

J2-15

+5V. P2-18

+5V. P2-19

+5V. P2-20

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

SYSTEM FRONT PANEL LOGIC BOARD

HEWLETT PACKARD

SHEET ASSEMBLY 30070-60008

PART NUMBER 30070-60009

D -30070-60009-51

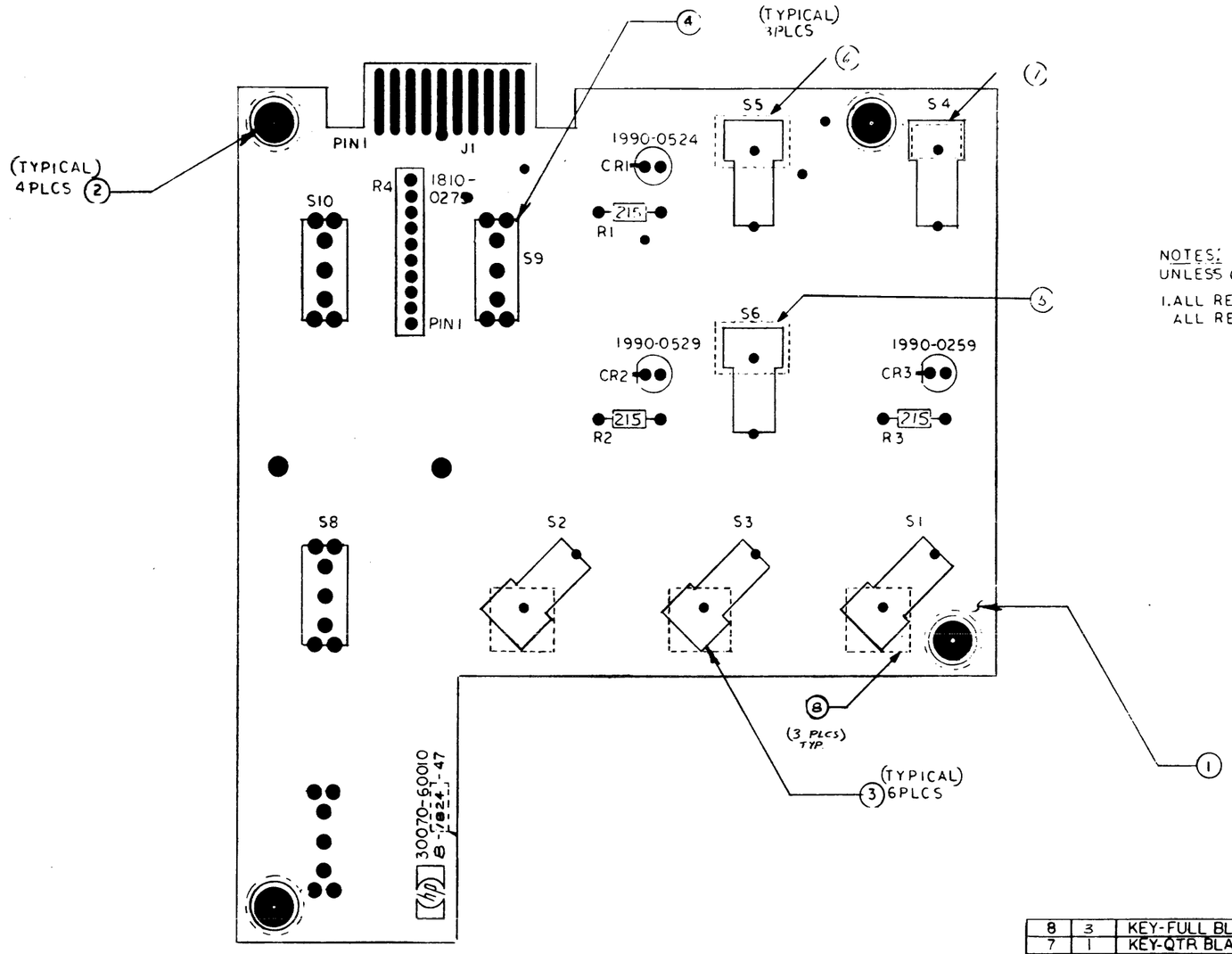
FINISH SCALE

SHEET 1 OF 1

STOCK NO 5300-0004 PRINTED ON DWG NO 1030-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY	SEPIA	C-30070-60010-4

SYM	REVISIONS	APPROVED	DATE
A	[illegible] PCO47 1435	[illegible]	[illegible]



NOTES:
UNLESS OTHERWISE SPECIFIED-

1. ALL RESISTANCE IN OHMS
   ALL RESISTORS ARE 1/4W 5% (0683-2215)

ITEM	QTY	DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
8	3	KEY-FULL BLANK	5041-0311		
7	1	KEY-QTR BLANK	5041-0309		
6	1	KEY-RUN	5041-1607		
5	1	KEY-HALT	5041-1608		
4	3	SWITCH-TOG.	3101-2294		
3	6	SWITCH PUSHBUTTON	5060-9436		
2	4	#4 SPACER .875 LENGTH	0380-0882		
1	1	P C BOARD - SWITCH	30070-60010		

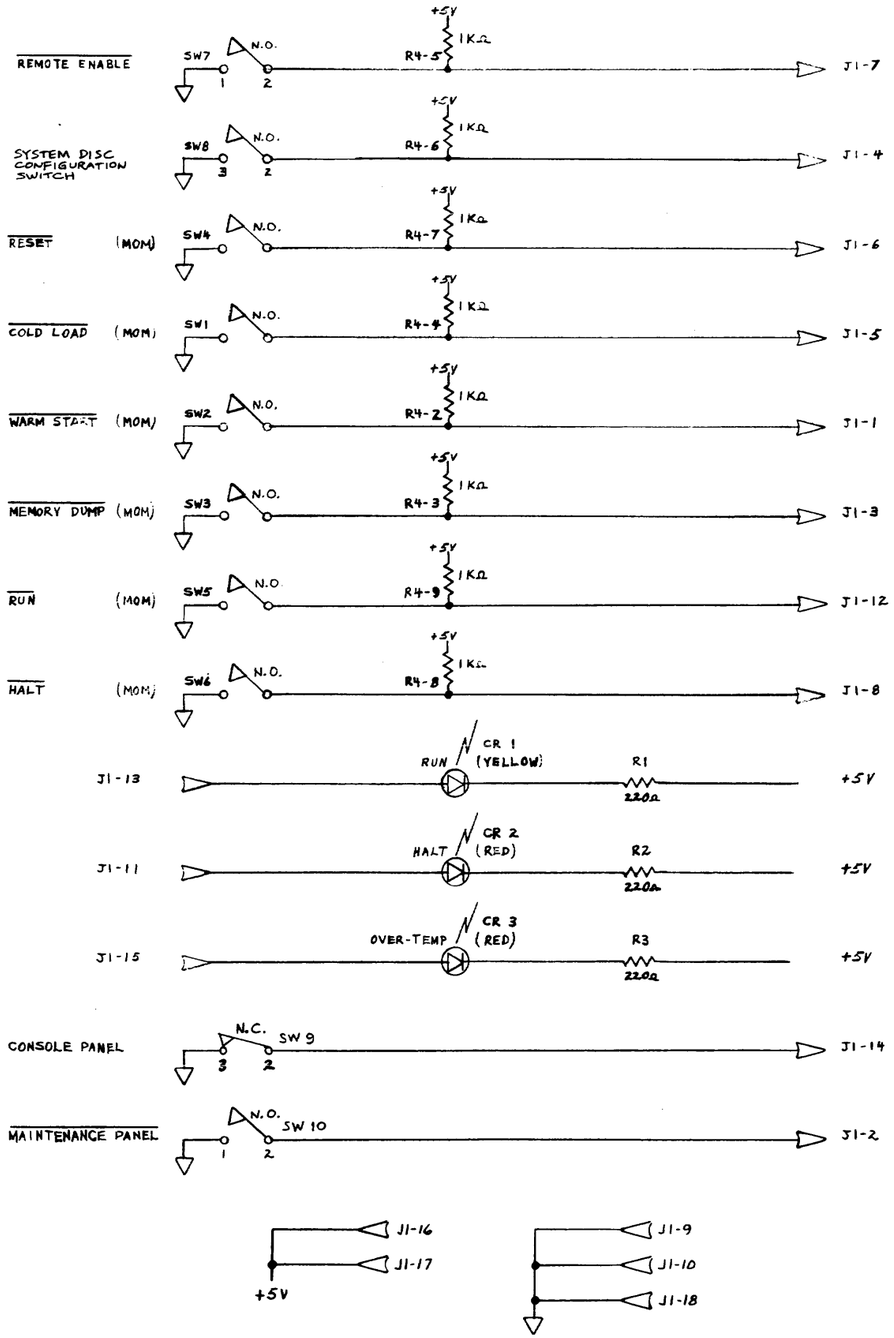
PCA - SWITCH ASSY DWG	HEWLETT PACKARD
30070-60008	30070-60010
2X	C-30070-60010-4

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY ■ SEPIA ▨

0	1	2	3	4		6	8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	47									

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	BSW	3-20-78

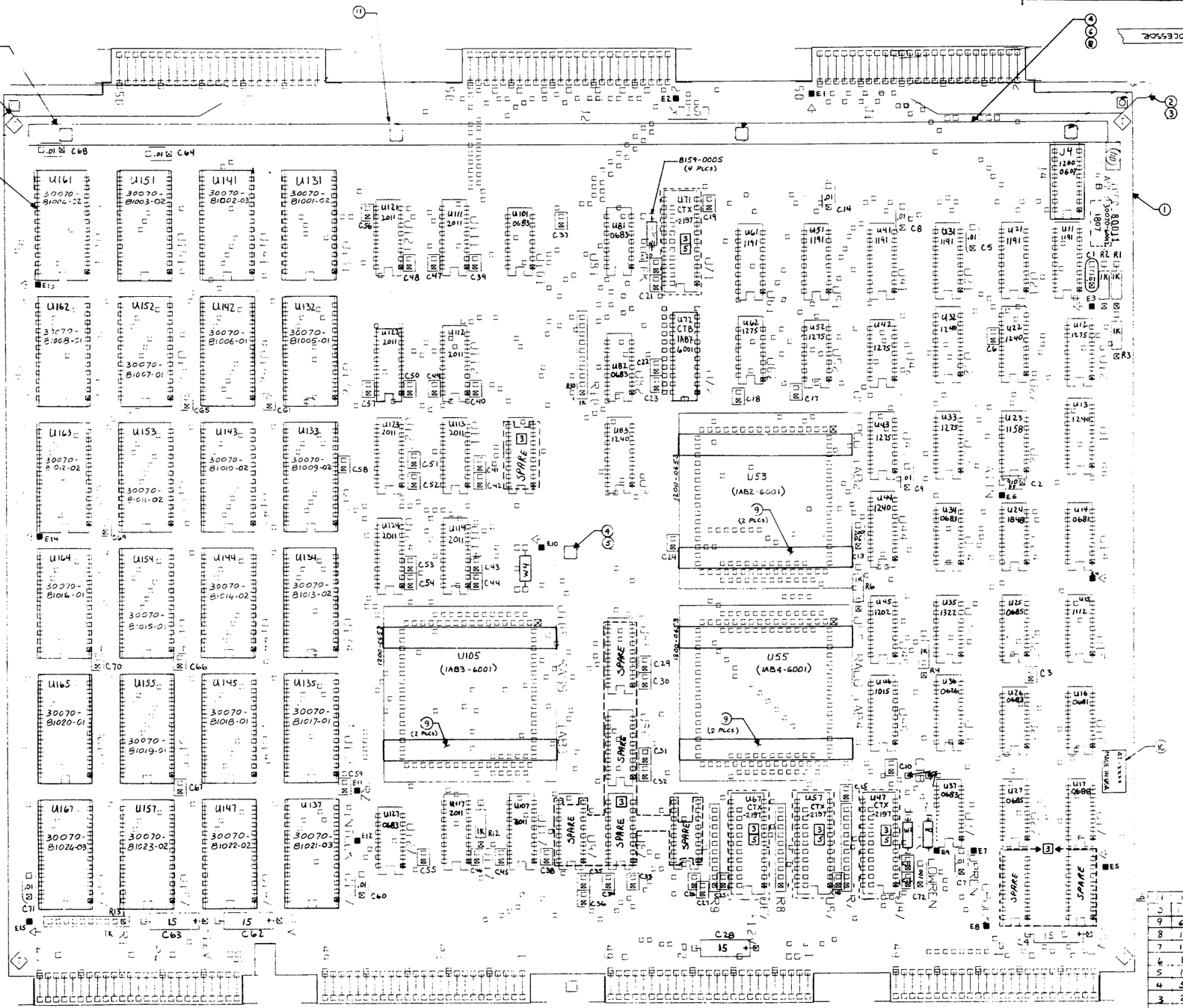


NOTES:
1. ALL 1KΩ RESISTORS ARE IN RES-NETWORK (1810-0275).
2. 220Ω RESISTORS ARE 1/4 W.
3. J1 IS 20-PIN EDGE-CARD CONNECTOR

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG NO	MAT'L-SPEC

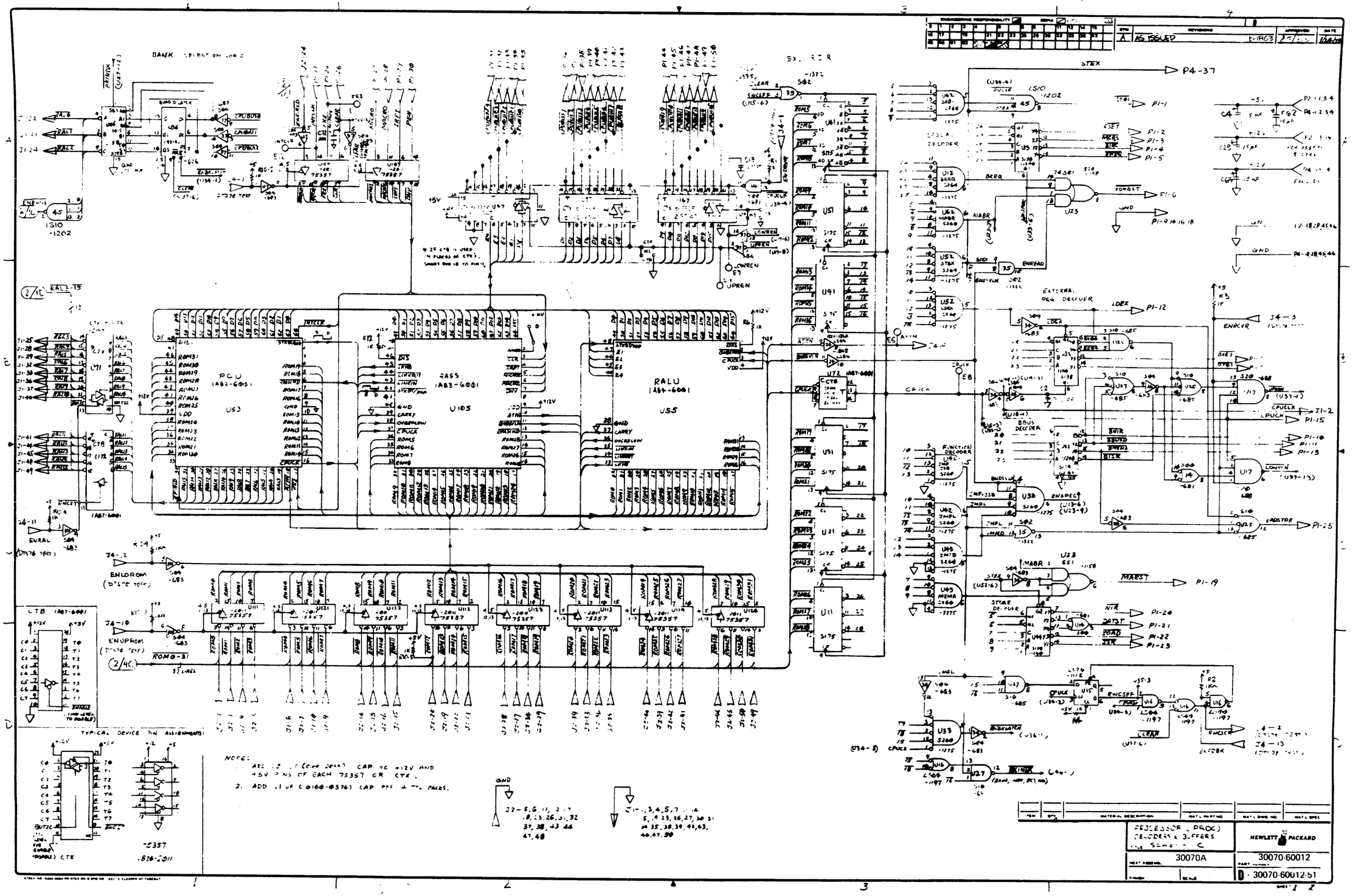
TITLE: SYSTEM FRONT PANEL SWITCH BOARD	HEWLETT-PACKARD
NEXT ASSEMBLY: 30070-60008	PART NUMBER: 30070-60010
FINISH: — SCALE: —	C-30070-60010-51

		F-30070-60012-1	
A	AS ISSUED	29 SEP 78	9:21 PM
B	ADDED NOTE 9 PER DOC CMD.	07 FEB 79	5:34 PM

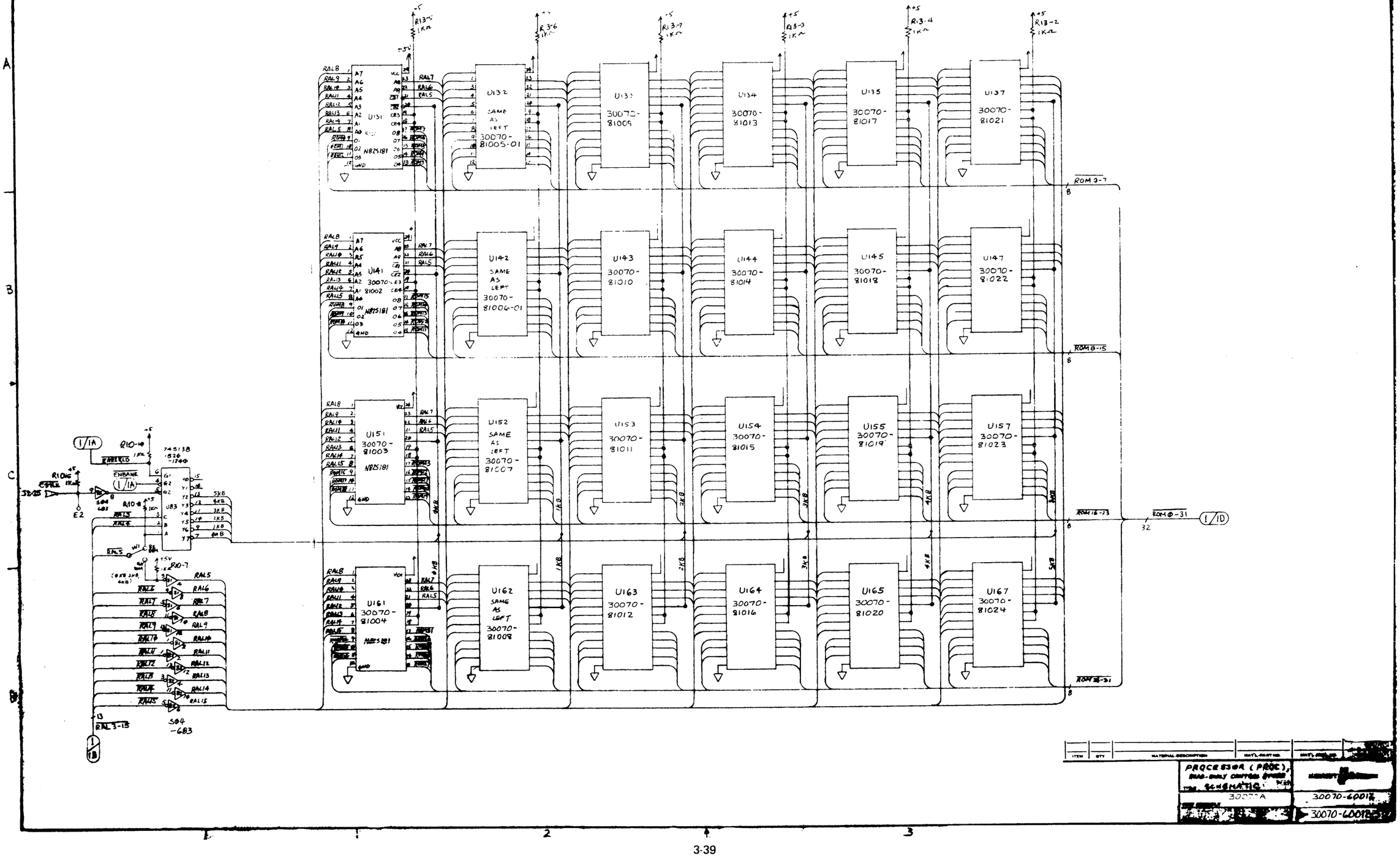


ITEM	QTY	PART NO	DESCRIPTION
1	1		LABEL, ROM VERSION
0	-		LABEL, WARRANTY
9	6		RETAINER
8	1		LABEL BLANK (SER NO.)
7	1		LABEL
6	1		BRACE
5	1		SPACER
4	5		SCREW 4-40 X .312
3	2		EXTRACTOR
2	2		PIN
1	1		PCA-CPU PROCESSOR

ASSEMBLY CPU PROCESSOR		HEWLETT-PACKARD	
30070 A		30010-60012	
SCALE	SHEET 2/1	F-30070-60012-1	


BANK SELECT ON LOG C
PCU (A82-6001) U53
RASS (A83-6001) U105
RALU (A84-6001) U55
LTB (A87-6001)
EXT. REF
P4-37
P1-1
P1-2
P1-3
P1-4
P1-5
P1-6
P1-9 10 16 18
P1-12
P1-15
P1-10
P1-11
P1-13
P1-19
P1-20
P1-21
P1-22
P1-23
P1-25
J4-1
J4-2
J4-3
J4-10
J4-11
J4-13
J2-5,6,11,12,17,18,23,26,31,32,37,38,43,44,47,48
J1-1,3,4,5,7,8,9,10,21,22,23,26,27,30,31,34,35,38,39,43,43,46,47,50
TYPICAL DEVICE PIN ASSIGNMENTS
NOTES:
1. ADD .1 UF (0160-0576) CAP FROM +12V AND +5V PINS OF EACH 75357 OR CTK.
2. ADD .1 UF (0160-0576) CAP PER 4 TTL PACKS.
PROCESSOR (PROC) DECODERS & BUFFERS
SIZE C
30070A
30070-60012
D - 30070-60012-51
NEWLETT PACKARD

REVISIONS		
SYM	DESCRIPTION	DATE
A	AS ISSUED	8.82
B	ADDED FAB NOS TO IC'S HER.	



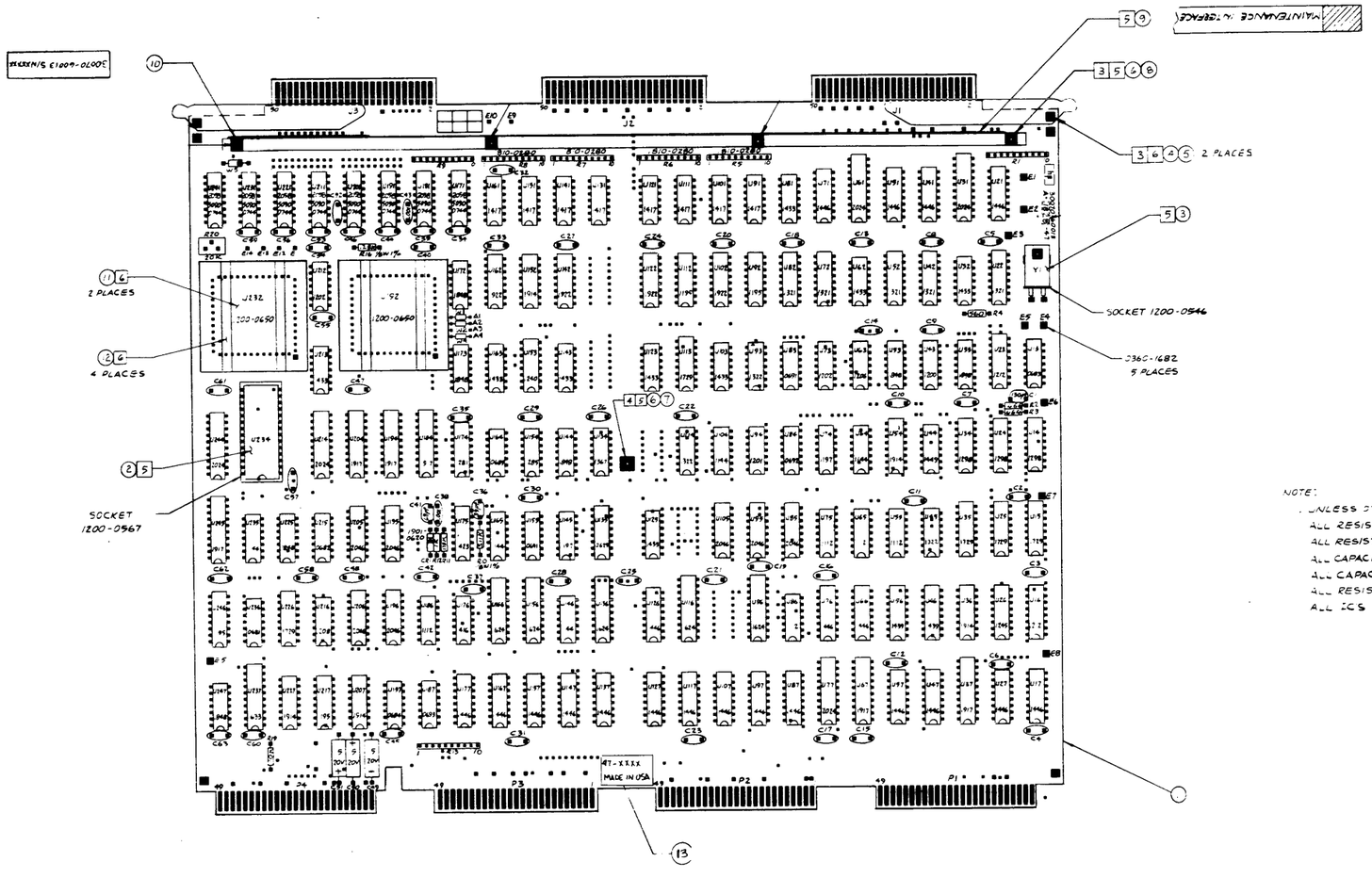
ITEM	QTY	MATERIAL DESCRIPTION	MFG'L PART NO.	MFG'L SOURCE

PROCESSOR (PROC), RAS-ONLY CONTROL BOARD
TITLE SCHEMATIC
30070A
30070-60018
30070-60018

ENGINEERING RESPONSIBILITY	SEPIA

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED 1803	BJGK	4-21-78
B	WAS WAS 1820-1194-97(1803) NOW WAS 1803	BJGK	4-21-78
C	ELIMINATE PROTOTYPE JOG PACER KIT	GK	7-6-78
D	REVISED PER ECR # 11 DATE CODE WAS 1803	GK	8-2-78

D-30070-60013-1

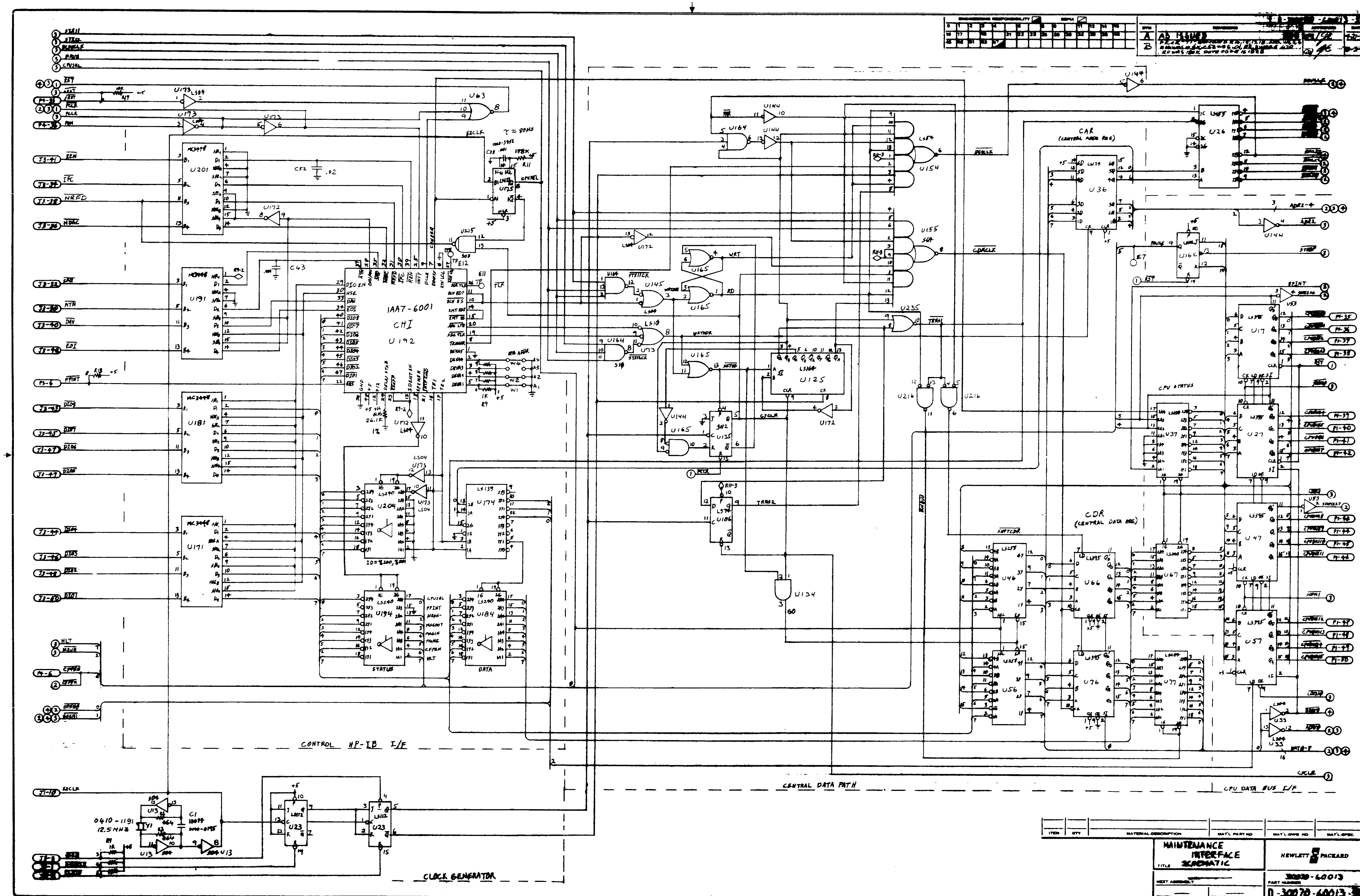


NOTE:
. UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS
ALL RESISTORS 4W, 5%
ALL CAPACITANCE IN MICROFARADS
ALL CAPACITORS .01 μF CER DISC
ALL RESISTOR NETWORKS 810-0275, (1)
ALL ICS 820-

ITEM	QTY	MATERIAL OR DESCRIPTION	MFG. PART NO.	MFG. NAME	MFG. SPEC
13	1	LABEL- WARRANTY	7120-6830		
12	4	SCREW 2			
	2	IC-[illegible] 232			
11	1	LABEL BLANK (SER. NO.)	7120-3766		
9	1	LABEL INFO	7120-1056		
8	1	BRACE PC BOARD	7040-6058		
7	1	SCREW	0520-1338		
6	5	SCREW	0520-0077		
5	1	EXTRACTOR	5040-6409		
4	2	PIN	1480-0116		
3	1	XTAL Y1 12.5 MHZ	2[illegible]-[illegible]91		
2	1	[illegible]ERO 40 PIN 1234	0[illegible]-6422		
1	1	PCB-MAINTENCE INTERFACE	30070-80013		

MAINTENANCE INTERFACE - PCA	HEWLETT PACKARD
NEXT ASSEMBLY 30070A	30070-60013
DO NOT SCALE DRAWING	D-30070-60013-1
FINISH COAT.	SCALE =U.C.

SHEET 1 OF 1


MAINTENANCE INTERFACE SCHEMATIC
HEWLETT PACKARD
30070-60013
D-30070-60013
SHEET 1 OF 1
CONTROL HP-IB I/F
CENTRAL DATA PATH
CPU DATA BUS I/F
CLOCK GENERATOR
CAR (CENTRAL ADDR REG)
CDR (CENTRAL DATA REG)
CPU STATUS
1AA7-6001 CHI U192
U201
U191
U181
U171
U204
U194
U184
U174
STATUS
DATA
U63
U125
U135
U134
U154
U155
U235
U216
U36
U26
U17
U27
U37
U47
U57
U46
U56
U66
U76
U67
U77
U23
U13
U186
0410-1191 12.5MHZ
A AS ISSUED
B

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED 1803		9-21-77
B	PER ECR 1" REMOVED C828 C44, ADD W5 R10 W&S 6.95K. DATE CODE 1820		8-2-78

FRONT PANEL I/F

SERIAL DATA SELECTOR

CLK DEMULTIPLEXING

BREAKPOINT LOGIC

IMB BF INDICATOR

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

MAINTENANCE INTERFACE SCHEMATIC

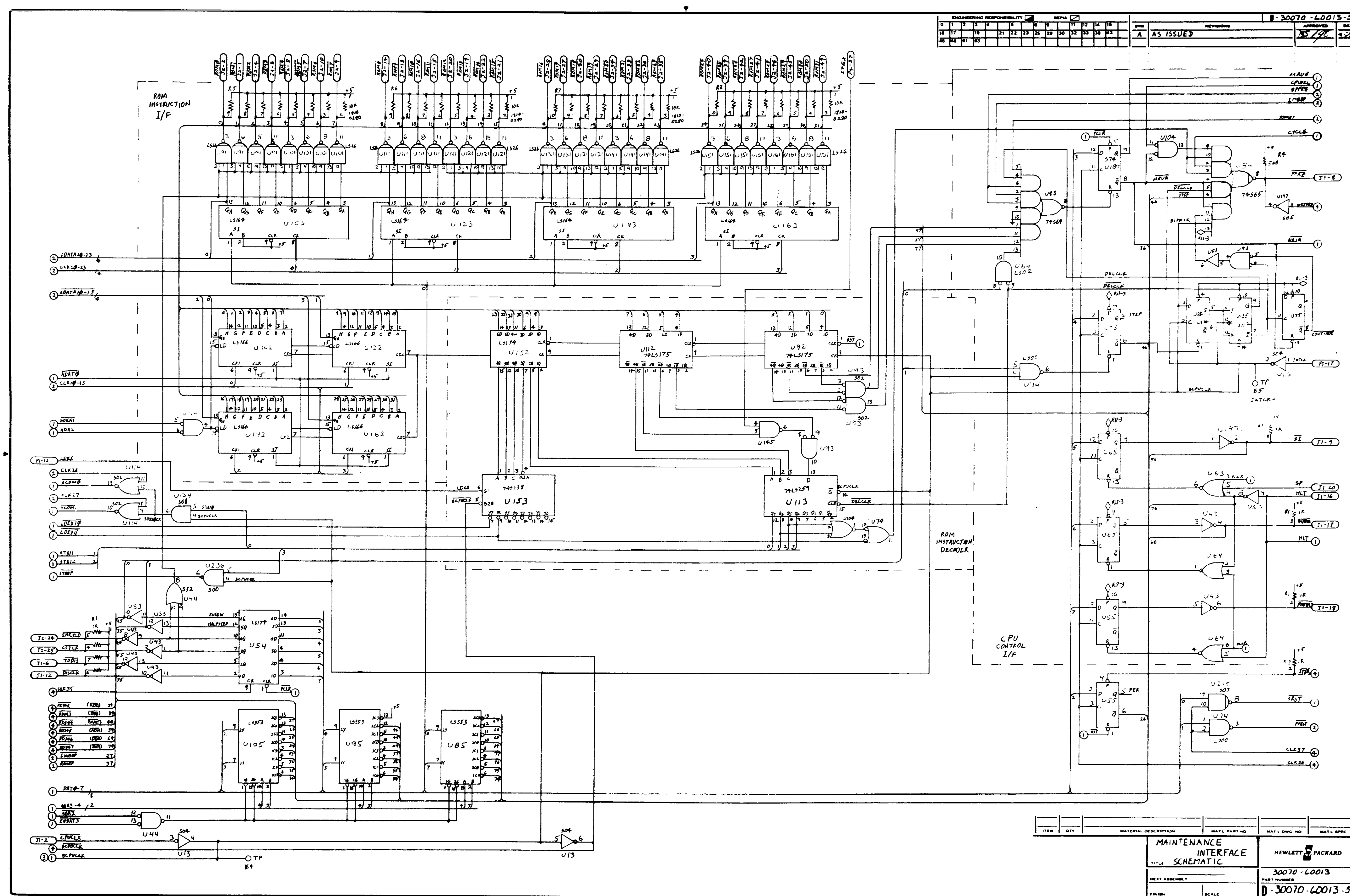
HEWLETT PACKARD

NEXT ASSEMBLY

30070-60013

D-30070-60013-52

SHEET 1 OF 1


D-30070-60013-53
A AS ISSUED
ROM INSTRUCTION I/F
ROM INSTRUCTION DECODER
CPU CONTROL I/F
U103 LS164
U123 LS164
U143 LS164
U163 LS164
U102 LS166
U122 LS166
U142 LS166
U162 LS166
U152 LS174
U112 74LS175
U92 74LS175
U153 74S138
U113 74LS259
U54 LS174
U105 LS353
U95 LS353
U85 LS353
U83 74S64
U84 74S65
U187 S74
U104
U64 LS02
SDATA20-23
CLK20-23
SDATA10-13
ADAT0
CLK10-13
GOEN1
ADR2
LDEX
CLK26
SCOM0
CLK27
SCOM1
LDEX10
LDEX11
STX11
STX12
STRBP
ENRWLD
CSTLR
TODIS
DISCLK
CLK35
IMBBP
DAT0-7
ADR3-4
ENDAT3
CPUCLK
BCPUCLK
MRUN
CPUSEL
BPFRZ
CYCLE
PCLR
PFRZ
DELCLK
STEP
CONTINUE
SI
SP
HLT
PER
SRST
PRST
CLK37
CLK36
INTCK
MAINTENANCE INTERFACE SCHEMATIC
HEWLETT PACKARD
30070-60013
D-30070-60013-53
SHEET 1 OF 1

TEST HP-IB I/F

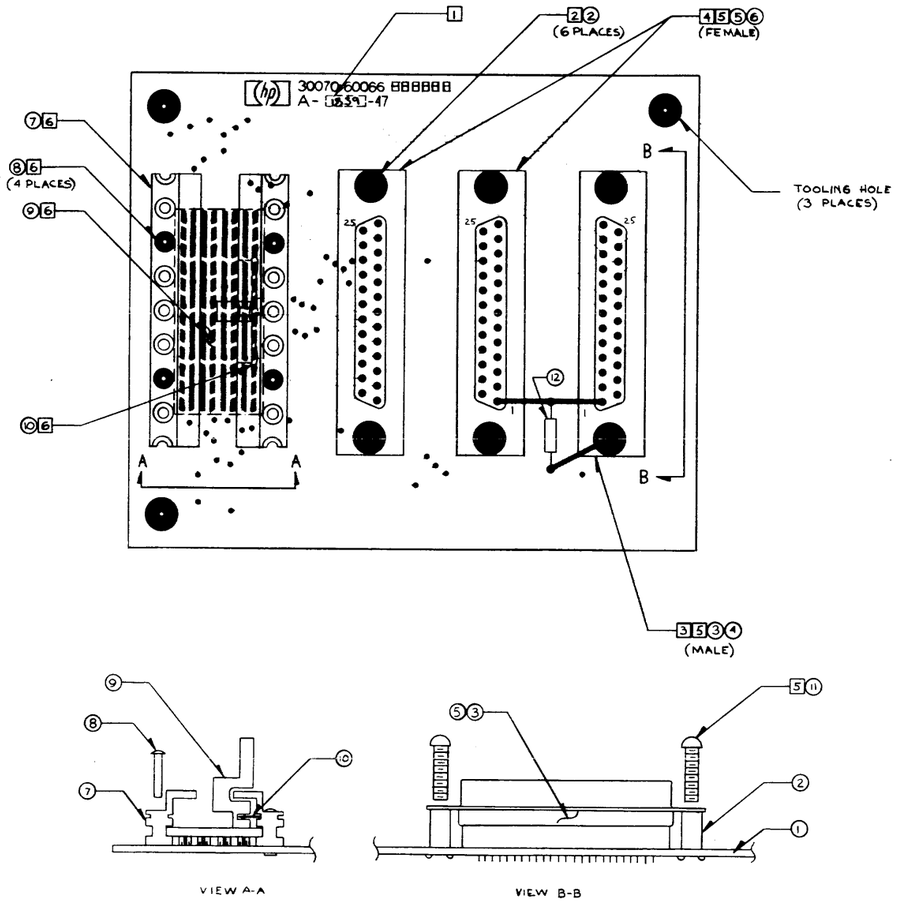
IMB I/F

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE: MAINTENANCE INTERFACE SCHEMATIC	HEWLETT PACKARD
NEXT ASSEMBLY	30070-60013 PART NUMBER
FINISH / SCALE	D-30070-60013-54 SHEET 1 OF 1

STOCK NO 5060-0064 PRINTED ON DIGITO NO 1820-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY	SIZE/A	D-30070-60066-1
	REVISIONS	APPROVED / DATE
	A AS ISSUED	DCN F0 9-21-87



ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
12		JUMPER	8159-0005		
11	6	SCREW 4-40 X .500	2200-0147		
10	1	DETENT SPRING	5020-3440		
9	1	SLIDER-SWITCH	30070-60074		
8	4	RIVET	0361-0028		
7	2	GUIDE-PLAST C	5020-7936		
6	50	CONNECTOR PIN- FEMALE	1251-3153		
5	2	CONNECTOR RCP- FEMALE	1251-2416		
4	25	CONNECTOR PIN- MALE	1251-3154		
3	1	CONNECTOR RCP- MALE	1251-2417		
2	6	SPACER-SWAGE 4-40 X .375	0380-0334		
1	1	BOARD-ETCHED	30070-80066		

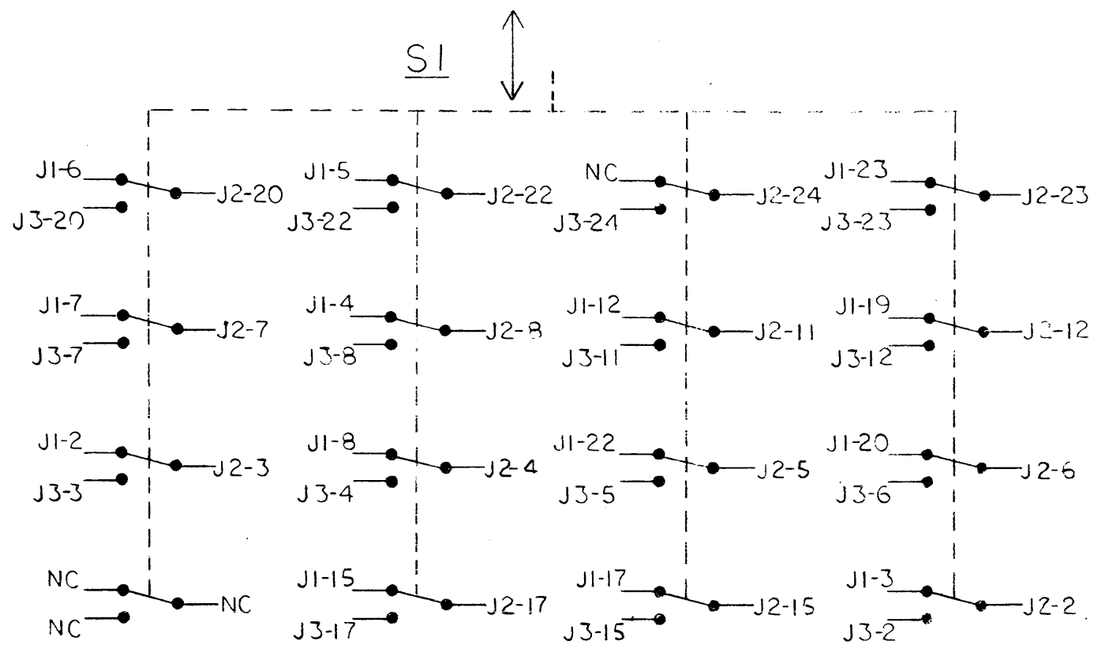
TITLE	SCF ASSY DWG
NEXT ASSEMBLY	30070-60067
FINISH	DO NOT DRI-FILM
SCALE	2:1
HEWLETT PACKARD	
PART NUMBER	30070-60066
	D-30070-60066-1

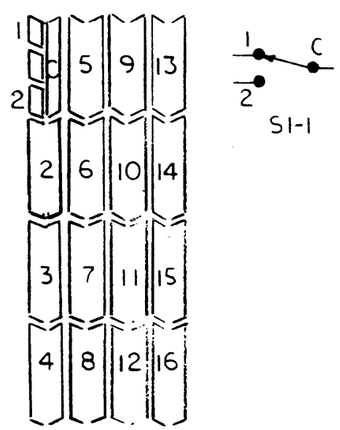
ENGINEERING RESPONSIBILITY															
0	1	2	3	4	5	6	7	8	9	10	11	12	14	15	
16	17	18	19	20	21	22			33	34	38		42	43	
		63			90			93							

SEPIA

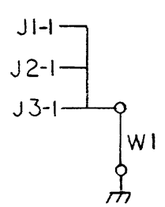
B-30070-60066-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED 1251	GS / DLH	9-27-78





SWITCH DETAIL
(TYP.)



NOTE:
S1 (16PDT) SHOWN IN "CONSOLE-TO-MODEM" POSITION.

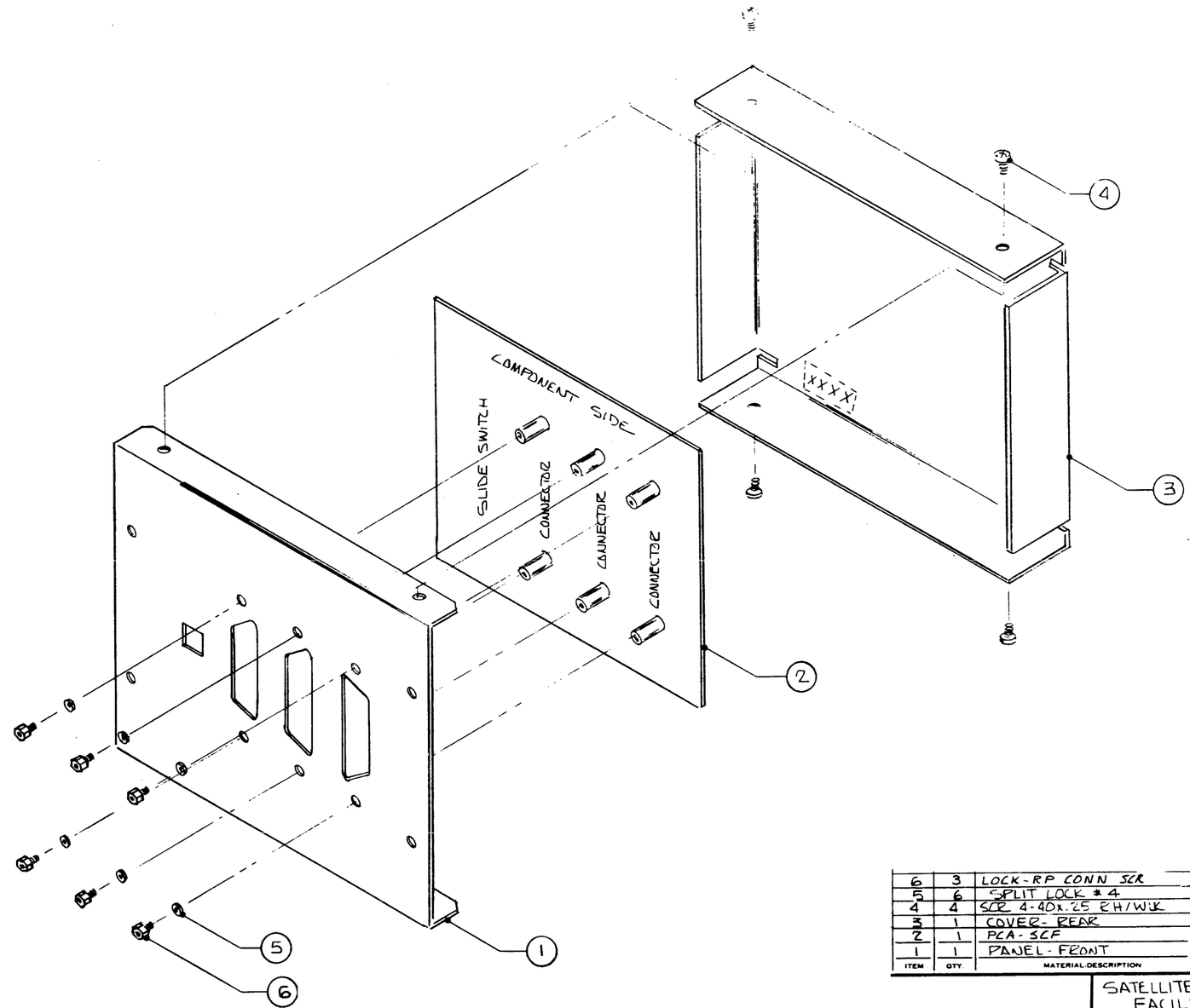
ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

TITLE SCHEMATIC	HEWLETT PACKARD
NEXT ASSEMBLY 30070-60067	PART NUMBER 30070-60066
FINISH — SCALE —	B-30070-60066-51

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY															SEPIA
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63												

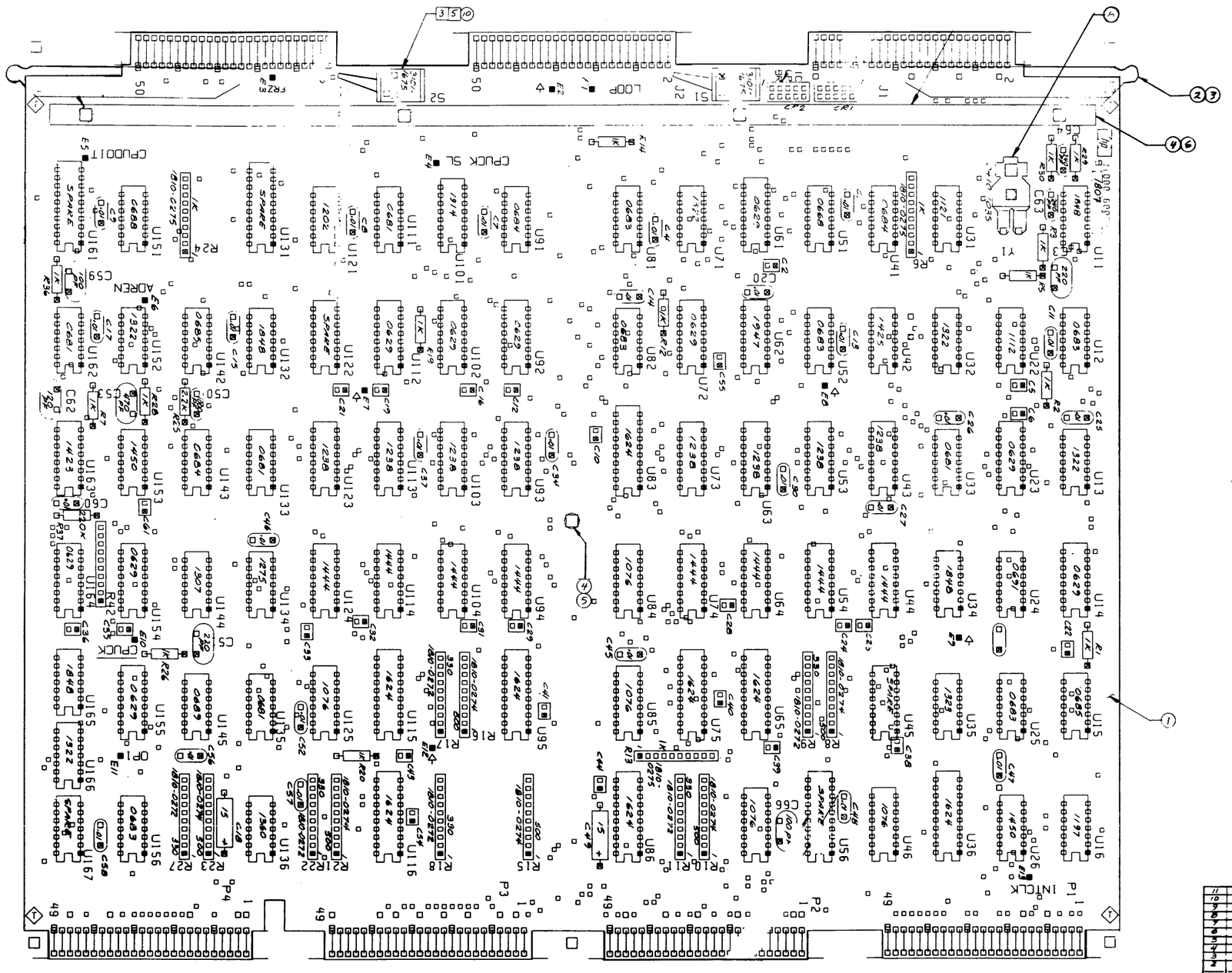
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		



ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
6	3	LOCK-RP CONN SCR	1251-1198		
5	6	SPLIT LOCK #4	2190-0109		
4	4	SCR 4-40x.25 PH/WSR	2200-0105		
3	1	COVER-REAR	30070-00123		
2	1	PCA-SCF	30070-60066		
1	1	PANEL-FRONT	30070-00122		

TITLE	HEWLETT PACKARD
SATELLITE CONSOLE FACILITY-ASS'Y.	
NEXT ASSEMBLY: 30070-60065	PART NUMBER: 30070-60067
FINISH: — SCALE: 1/1	C-30070-60067-1

SHEET 1 OF 1



NOTES:
1 UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS 1/4W 1%.
ALL CAPACITANCE IN MICROFARADS
ALL CAPACITORS .1 UF
ALL IC's ARE 1820-.

11	1	LABEL WARRANTY	7120-6830	
10	2	SWITCH SLIDE 3PDT	3101-1178	
9	2	LED ARRAY CHERRY	1990-0442	
8	1	SOCKET XTAL	1200-0346	
7	1	LABEL	7120-6803	
6	1	BRACE	5040-2068	
5	1	SPACER	5020-5378	
4	5	SCREW 4-40 X .31	0624-0077	
3	2	EXTRACTOR	5040-2029	
2	2	PIN	1988-0176	
1	1	PC BD ETCHED	31000-60033	

CPU BC ASSEMBLY

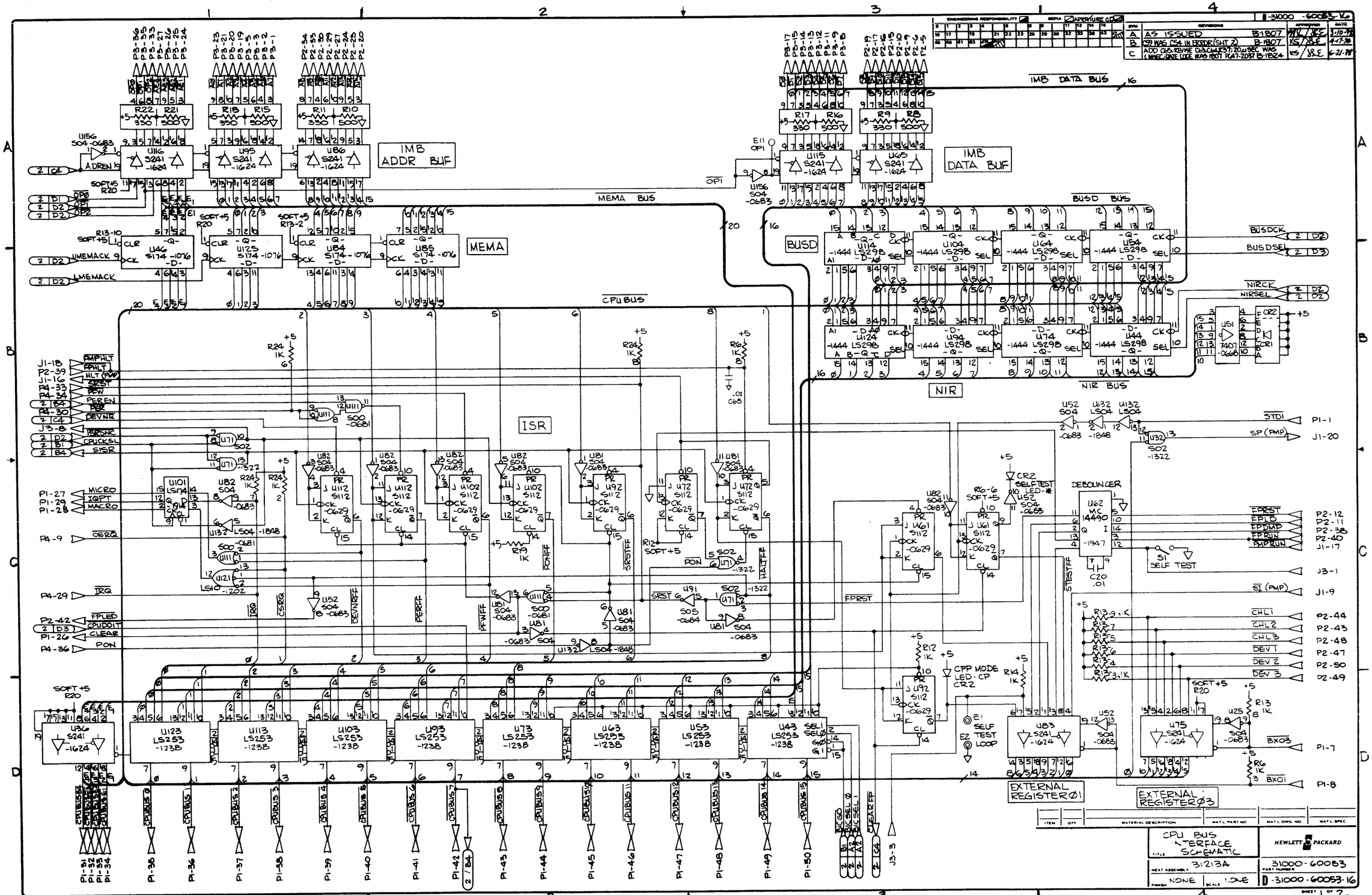
SIZE 5121 3A

31000-60053

SCALE 2:1

F-31000-60053-11

SILKSCREEN
COMPONENT SIDE


IMB ADDR BUF
IMB DATA BUF
MEMA
ISR
NIR
IMB DATA BUS
MEMA BUS
BUSD BUS
CPU BUS
NIR BUS
EXTERNAL REGISTERØ1
EXTERNAL REGISTERØ3
DEBOUNCER
CPU BUS INTERFACE SCHEMATIC
HEWLETT PACKARD
31213A
D-31000-60053-16
SHEET 1 OF 2

ENGINEERING RESPONSIBILITY	SCALE	APERTURE CARD
0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 43 44 45 46 47 48 49 50		

SYM	REVISIONS	APPROVED	DATE
	SEE SHEET 1 B-18-84		

B-31000 -60053-16

INTERNAL CLOCK CIRCUIT

MICROHALT, S2, R6 1K, +5, J3-10, J3-5, DISCK, C3 220PF, R3 1K, R5 1K, U12 S04 -0683, U31 8093 -1121, U22 LS74 -1112, U26 S37 -1450, U32 S00 -1322, INT CLK, P1-17, E13 INTCLK, R2 1K, Y1 11.2 MHZ, DISCK (PMP), J1-12, EXCLK (PMP), J1-10

5INS, 76NS, CPUCLK, CPUCKSL, NOTE: NON-SYMMETRICAL CLOCK SKEW

CPU CLOCK CIRCUIT

E10 CPUCK, P1-15, CPUCLK, J3-14, 1/B1, CPUCKSL, U41 -0684 S05, U42 LS132 -1425, U11 LS04 -1848, CPUCK, CPUCKSL, U13 S02 -1322

1/D3, P1-12, LDEX, U12 S04 -0683, U13 S02 -1322

SPECIAL CONTROL: P1-4 BIRC, P1-5 BWRQ, P1-6 RDRQST, P1-2 RSET, P1-3 MCRS

STORE: P1-22 LOAD, P1-19 MARST

ADDST, SETDOIT, U26 S37 -1450, U25 S04 -0683, U35 S30 -1323, U66 S174 -1076, SOFT +5 R13-10, 2NS, C66 100PF, CPUCK, CPUNK, U13 S02 -1322

U34 LS04 -1848, R29 1K, R30 1K, 66NS, C64 330PF, C63 330PF, U41 S05 -0684

U16 LS00 -1197, U14 S112 -0629, U23 S112 -0629, U22 LS74 -1112, U25 S04 -0683, CPUCKSL, U33 S00 -0681, U42 S00 -0685, U34 LS04 -1848, CR2 LED -IC INSTRUCTION CALL

BIRC, READRQ, ICLK, BCLK, R24 1K, J3-9, R18 330, DNV, P3-7, R15 500, R1 1K, U165 LS04 -1848, U135 S00 -0681

OPO, OPZ, OP1, 1/A1, J3-39, 1/A1

PEN, ISRSNC, P1-30, 1/B1, UNIMACK, 1/B1, J3-13, INTCK, 1/B4, UNIMAGE, 1/B1, J3-43, INTRSET, 1/B4, J3-7, J3-2

BUSD, CRC, J3-45, 1/A4, BUSD, SEL, J3-4, 1/B4, J3-25

IMB OP CODES

OP CODE	0	1	2	
0		1	1	1	MEM READ
1		1	1	0	MEM RD/SET
2		1	0	1	MEM WRITE
3		1	0	0	RESERVED
4		0	1	1	I/O READ
5		0	1	0	MEM STATUS
6		0	0	1	I/O WRITE
7		0	0	0	RESERVED

'STORE' CONTROL

P1-23 TSR, P1-25 EADSTOK, P1-21 DATST, P1-20 NTR, 1/D3, BICSEL0, 1/D3, BICSEL1

'BBUS' CONTROL

P1-1, P1-11, P1-10, BMEMA, BBUSD, BBUSI, J1-8, P1-24, PFR2, FRZ, E3 FRZ

U1151 S20 -0688, U1162 S00 -0681, U142 S10 -0685, ADDST, EDDOIT, U24 S64 -0691, DOPEND, ADREN, SETDOIT

J3-11, J3-41, J3-29, CPUCE, U1154 S112 -0629, DOPEND, +5 R26 1K 48NS, C51 220 PF, +5 R28 1K 15NS, C53 470 PF, U1132 LS04 -1848

CR2 LED - BR BUS REQUEST

U1135 S00 -0681, U1134 S260 -1275, U1136 8T09 -1360, U1135 S00 -0681, U1136 8T09 -1360, U1135 S00 -0681, U1136 8T09 -1360, +5 R42 1K, SOFT +5 R20

IMB CONTROL LINES

DDONE, ADONE, BRQ, WAIT, ADDIT, DDDIT

R27 33, R23 33, P4-27 DDONE, P4-21 ADONE, P4-15 BRQ, P4-19 WAIT, P4-23 ADDIT, P4-25 DDDIT

U1135 S00 -0681, U1136 8T09 -1360, U1135 S00 -0681, U1136 8T09 -1360, U1135 S00 -0681, U1136 8T09 -1360, U1135 S00 -0681, U1136 8T09 -1360

U1145 S22 -0689, U1143 S05 -0684, U1135 S00 -0681, U1136 8T09 -1360, U1135 S00 -0681, U1136 8T09 -1360, U1135 S00 -0681, U1136 8T09 -1360

CPUBUSY, 1/D2, J3-42, PEREN, 1/B1, J3-6, SISR, 1/B1, J3-18, J3-12, J3-32, E6 ADREN, 1/A1, J3-31, J3-27 DEVNR, 1/B1, CLEARFP, 1/D3, EPIO, P4-42, P2-41

U1156 S04 -0683, U1154 S112 -0629, U1166 S02 -1322, U1165 LS04 -1848, U1164 S112 -0629, U1166 S02 -1322, U1156 S04 -0683, U1154 S112 -0629, U1152 S02 -1322

OPCLR, U1162 S00 -0681, ES CPUDOIT, CPUDOIT, U1163 LS123 -1423, U1156 S04 -0683, 20 USEC TIME OUT, U1153 S37 -1450, U1133 LS00 -0681, U1143 S05 -0684, U1144 S132 -1307, U1142 S10 -0685, U132 LS04 -1848, TODIS (PMP), J3-37, J3-35, J3-20, P4-17, 1/C1, J3-33, BACK, CPUDOIT, R24 1K, R6 1K, R37 4.7K, R25 2.2K, C60 .01, C50 .001, 1.05μS, 40NS, R7 1K, C62 120 PF, C61 100 PF, 48NS, 30NS, CPUDOIT DLY, ADREN, CPUDIN, ADONE

CONTROL CIRCUIT

IMB HANDSHAKE CIRCUIT

E7 E8 E9 E12, +5 C49 15, C18 15, .01 (25 REQD), .1 (27 REQD), COM, GRD

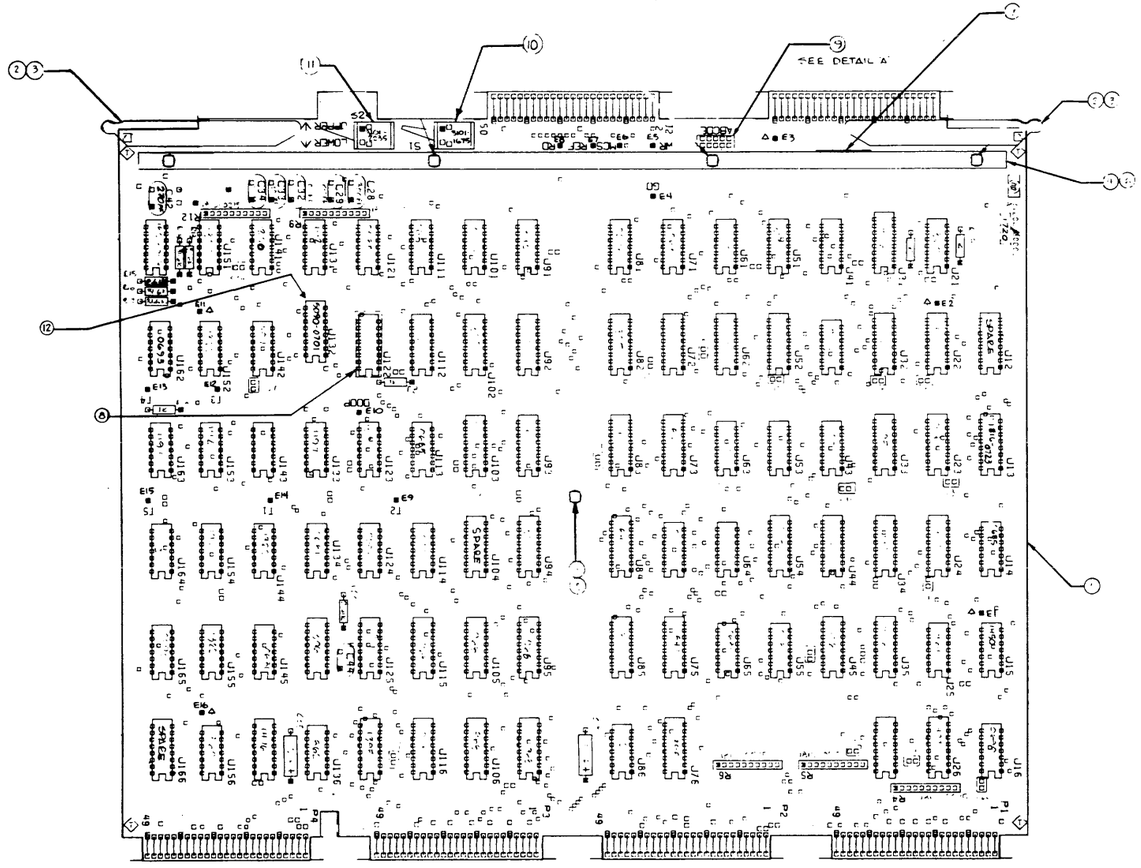
P1-9,4,6,18; P2-18,28,35,45,46; P3-4,10,16,22,28,34,37,49; P4-14,18,20,22,24,26,28,35,45,46; J1-13,5,7,11,15,9,23,26,27,30,31,34,35,38,39,42,43,46,47,50

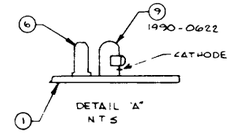
NOTES: UNLESS OTHERWISE SPECIFIED
1. SOFT +5 = CONNECTION TO A 1K PULLUP RESISTOR THAT MAY BE SHARED.
2. J3 CONNECTOR FOR DTS TO TEST ONLY.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE	CPU BUS INTERFACE SCHEMATIC
NEXT ASSEMBLY	3123A
FINISH	NONE
SCALE	NONE
	HEWLETT PACKARD
PART NUMBER	3000-60053
	D 31000-60053-16
	SHEET 2 OF 2

STOCK NO 5960-0004 PRINTED ON SHEPD NO 1020-10 CLEARPRINT PAPERCUT





NOTES:

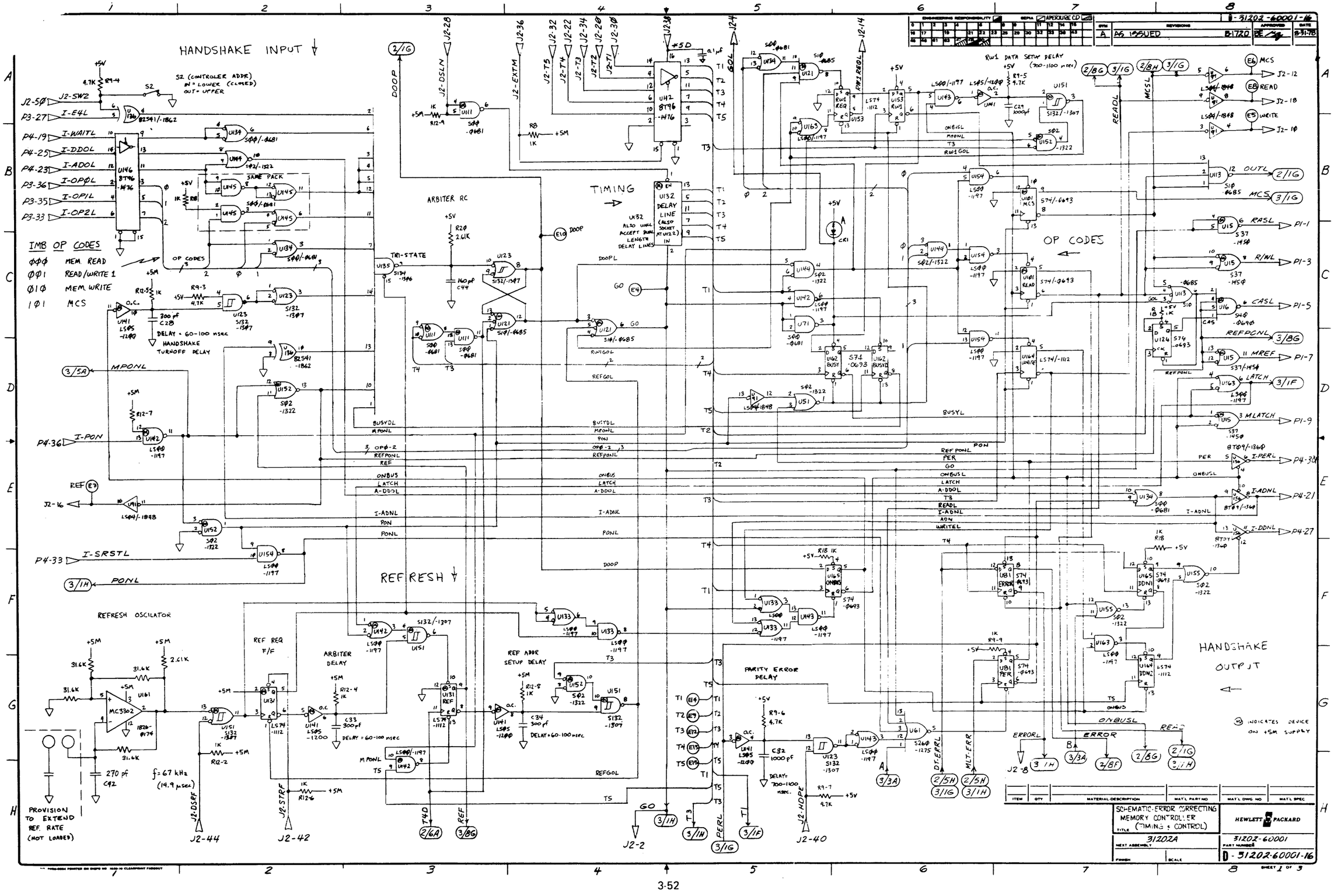
1. UNLESS OTHERWISE SPECIFIED
   ALL RESISTANCE IN OHMS
   ALL RESISTORS ¼ W ±1%
   ALL CAPACITANCE IN MICROFARADS
   ALL CAPACITORS ARE 0.1 UF MONOLITHIC CER
   ALL IC'S ARE 1820-

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
13	1	LABEL: WARRANTY	7120-6830		
12	1	C: DELAY LINE	5090-0701		
11	1	SW TGL 2 POS	3101-2235		
10	1	SW TGL DPST M	3101-1615		
9	1	LED ARRAY SEG-5	1990-0622		
8	1	SOCKET, 16 PIN	1200-0607		
7	1	LABEL	7120-6607		
6	1	HEAT [illegible]	[illegible]		
5	1	[illegible]	[illegible]		
4	5	[illegible]	[illegible]		
3	5	[illegible]	[illegible]		
2	[illegible]	[illegible]	[illegible]		
1	[illegible]	[illegible]	[illegible]		

ENGINEERING RESPONSIBILITY	SEPIA	MEDIUM
0 1 2 3 4 6 8 9 11 12 14 15 16 17 19 21 22 23 25 29 30 32 33 38 43 46 48 61 63		

SYM	REVISIONS	APPROVED	DATE
A	[illegible]	[illegible]	5-31-84
-	FROM B TO MAKE 5090-1112 AND [illegible]	[illegible]	9-7-77
C	ADD ITEMS 10,11 AND NOTE 7,8 AND ITEM 6 TO SHEET AND NOTE 2,4,5 AND ITEM 1 TO SHEET 2 PER MICO 4614	AW	10-82
D	ADD ITEM 13 PER ECO 4701	KS/[illegible]	12-9-83
E	REVISE NOTES 2 & 3 ADD NOTE 9 ITEM 13 PER 4720	KS/[illegible]	7-23-85

TITLE	[illegible] ASSY
31202A	
FINISH	SCALE
HEWLETT PACKARD	31202-60001
	D-31202-60001-1
	SHEET OF


HANDSHAKE INPUT
REFRESH
TIMING
OP CODES
HANDSHAKE OUTPUT
ARBITER RC
REFRESH OSCILATOR
IMB OP CODES
ΦΦΦ MEM. READ
ΦΦ1 READ/WRITE 1
Φ1Φ MEM. WRITE
1Φ1 MCS
S2 (CONTROLER ADDR) IN = LOWER (CLOSED) OUT = UPPER
DELAY = 60-100 nsec
HANDSHAKE TURNOFF DELAY
RW1 DATA SETUP DELAY (700-1100 nsec)
PARITY ERROR DELAY
REF REQ F/F
ARBITER DELAY
REF ADDR SETUP DELAY
PROVISION TO EXTEND REF. RATE (NOT LOADED)
f = 67 kHz (14.9 μsec)
SCHEMATIC-ERROR CORRECTING MEMORY CONTROLLER (TIMING & CONTROL)
HEWLETT PACKARD
31202A
31202-60001
D - 31202-60001-16
SHEET 1 OF 3
3-52

ENGINEERING RESPONSIBILITY — HEWLETT PACKARD APERTURE CD
STYLE | REVISIONS: SEE SHEET 1, B-1720 | APPROVED | DATE
B-31202-60001-16

DATA LATCHES AND DRIVERS

HAMMING TREES

IMB DATA LINES
MEMORY DATA LINES
MEMORY HAMMING LINES

IMB DATA DRVRS

CORRECTION CIRCUITS

1/3H

T4D

IMB DATA LINES

P3-17 I-D0L 0
P3-15 I-D1L 1
P3-14 I-D2L 2
P3-13 I-D3L 3
P3-12 I-D4L 4
P3-11 I-D5L 5
P3-9 I-D6L 6
P3-8 I-D7L 7
P2-19 I-D8L 8
P2-17 I-D9L 9
P2-16 I-D10L 10
P2-15 I-D11L 11
P2-14 I-D12L 12
P2-9 I-D13L 13
P2-6 I-D14L 14
P2-5 I-D15L 15

R4-6 R4-5 R4-4 R4-3 R4-2 R4-1 R4-8 R4-7 → 0 1 2 3 4 5 6 7 (+5V)
R6-7 R6-5 R6-4 R5-10 R5-9 R6-3 R5-8 R6-2 → 8 9 10 11 12 13 14 15 (+5V)

U102 3404 -1395
U103 8T95 -1477
U92 3404 -1395
U93 8T95 -1477
U82 3404 -1395
U83 8T95 -1477

DOOP
OUTL

U96 93548 -1968 (ODD)
U95 93548 -1968 (EVEN)
U105 93548 -1968 (ODD)
U104 93548 -1968 (EVEN)
U115 93548 -1968 (ODD)
U54 93548 -1969 (ODD)
U106 93548 -1968 (EVEN)
U116 93548 -1968 (EVEN)

U55 S00 -0681
U65 S00 -0681

READ

HAMMING LINE DRIVERS
R5-7 R5-6 R5-5 R5-3 R5-4 R5-3 → 0 1 2 3 4 5 (+5V)

U45 8T96 -1476
U22 8T95 -1477

SYNDROME LATCH
U44 LS174 -1914 (+5V, T4D)

ERROR DETECTION CKT.
U114A S260 -1275
U71 S00 -0681

U52 8T95 -1477
U62 8T95 -1477
U72 8T95 -1477
U32 8T96 -1476
U31 8T96 -1476
U21 BT04 -1364
U21 BT04 -1360

LS86 -1211
U64 U53 U53 U53 U64 U61 U64 U63 U63 U63 U74 U74 U74 U74

ON BUSL

C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15

U85 LS138 -1847
U84 LS138 -1847
U73 LS138 -1847
U75 LS138 -1847

ER0 ER1 C1 ER2 C2 C3 C4 ER3 C5 C6 ER4 C7 ER5 C8 ER6 C9 C10 C11 C12 ER7 ER8 C13 C14 ER9 C15

MEMORY HAMMING LINES

M0 → P1-43
M1 → P1-44
M2 → P1-46
M3 → P1-47
M4 → P1-48
M5 → P1-50

MEMORY DATA LINES

D0 → P1-22
D1 → P1-23
D2 → P1-24
D3 → P1-26
D4 → P1-27
D5 → P1-28
D6 → P1-30
D7 → P1-31
D8 → P1-32
D9 → P1-34
D10 → P1-35
D11 → P1-36
D12 → P1-38
D13 → P1-39
D14 → P1-41
D15 → P1-42

INDICATING HAMMING BIT ERRORS
H0 - U75.15
H1 - U84. 5
H2 - U73.15
H3 - U75.11
H4 - U75.13
H5 - U75.14

MCS IMB DATA DRVRS
S134 -1386 (U94)
MEM HAMMING LINES

ERROR 1/7H → U65 S00 -0681 → 3/4A

L-BIT → 3/8C
P-BIT → 3/8H
E-BIT → 3/E3
CNBUSL ← 1/7H
READL ← 1/3A 3/1G
MCSL ← 1/7A 3/1G

R1 1K +5V

1/3A DOOP
1/8B OUTL
1/8H 3/1H READ
3/6A ALTERNATE HAMMING BITS /6
3/4A D
3/4A DL

SYNDROME → 3/1G
DT-ERRL → 1/6H 3/1G
BD-PARL → 3/1G
MLT-ERR → 1/6H 3/1H
FERRL → 3/4A

+5V P2-1,2,34 P4-1,2,3,4 — 15μf T4B4 -1746 — .1μf Φ16G -0576 → +5V
+5V P2-25,26 — 15μf T4B4 -1746 — .1μf Φ16G -0576 → +5M
GND P2-18,28,35,45,46 P3-4,10,16,28,34,37,49 P4-16,18,20,22,24,26,28,35,45,46

P1-2,4,6,8,10,12,15,18,21,25,29,33,37,41,45,49
J2-1-49 (all odd # pins)

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

SCHEMATIC-ERROR CORRECTING MEMORY CONTROLLER (DATA PATHS)
TITLE
31202A
NEXT ASSEMBLY
FINISH | SCALE

HEWLETT PACKARD
31202-60001
PART NUMBER
D-31202-60001-16
SHEET 2 OF 3

STOCK NO 5060-6004 PRINTED ON D8090 NO 1030-16 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY — SIGMA APERTURE CD
SYM | REVISIONS | APPROVED | DATE
SEE SHEET 1 | B-1720
B - 31202-60001 -16

ADDRESS MUX. & REFRESH CNTR.

ADDRESS LATCH

IMB ADDRESS LINES

P3-26 I-E3L E3
P3-25 I-E2L E2
P3-24 I-E1L E1
P3-23 I-A0L Φ
P3-21 I-A1L 1
P3-20 I-A2L 2
P3-19 I-A3L 3
P3-5 I-A4L 4
P3-3 I-A5L 5
P3-2 I-A6L 6
P3-1 I-A7L 7
P2-34 I-A8L 8
P2-33 I-A9L 9
P2-30 I-A10L 10
P2-29 I-A11L 11
P2-27 I-A12L 12
P2-24 I-A13L 13
P2-23 I-A14L 14
P2-20 I-A15L 15

ALTERED-STATUS LATCH

ALTERNATE HAMMING LATCH

ERROR LOG CIRCUIT

MCS ADDR

ERROR ADDR

ROW ADDR

COLUMN ADDR

REF ADDR

MEMORY ADDRESS LINES
C-A6 P1-11
C-A5 P1-13
C-A4 P1-14
C-A3 P1-16
C-A2 P1-17
C-A1 P1-19
C-A0 P1-20

ERROR INDICATORS

1/5H T1
1/8D LATCH
1/5H PERL
1/8A 2/8G READL
2/5H SYNDROME
1/7A 2/8H MCSL
1/8B MCS
2/5H BD-PARL
1/6H 2/5H DT-ERRL
1/8H 2/16 READ
1/6H 2/5H MLT-ERR
ERRORL
1/7H GO
1/4H PONL
1/1F T3

EXT-RST C-26
REF 1/3H
REFPONL 1/8D
L-BIT 1/3F
E-BIT 2/15
P-BIT 2/15

RESET IN- RESET OUT- IDLE (LL)

Ⓜ INDICATES DEVICE ON +5M SUPPLY

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

SCHEMATIC ERROR CORRECTING MEMORY CONTROLLER (ADDRESS PAT-S)
TITLE

HEWLETT PACKARD

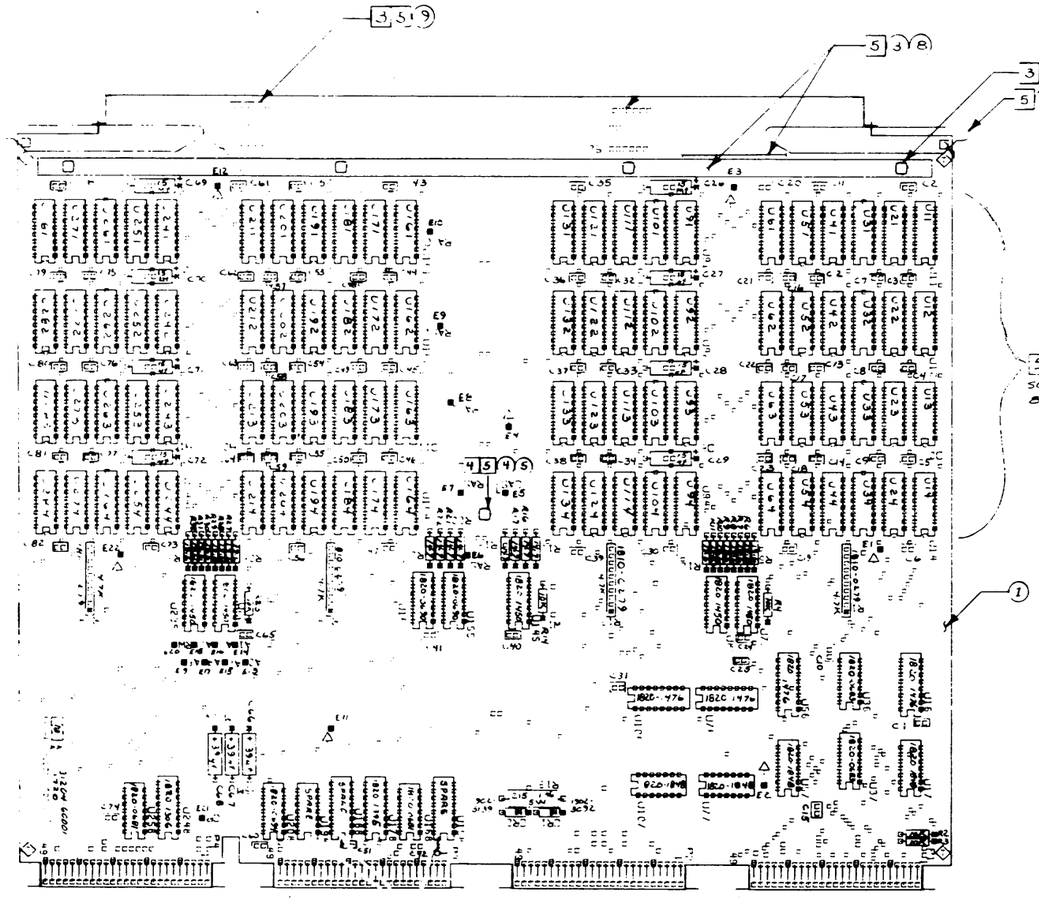
31202A
NEXT ASSEMBLY

31202-60001
PART NUMBER

FINISH | SCALE

D - 31202-60001 -16

SHEET 3 OF 3



NOTES:

1. UNLESS OTHERWISE SPECIFIED.
   ALL RESISTANCE IN OHMS
   ALL RESISTORS ARE 1/4 W 1%
   ALL CAPACITANCE IN MICROFARADS
2. ALL CAPACITORS .1uf 0160-
   ALL IC'S ARE 1818-03--

ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
11	1	LABEL-WARRANTY	7120-6830		
10	88	MK4116-3 16K RAM	1818-0341		
9	1	SW THWHL 0-7	3100-3395		
8	1	BRDCE-PC BOARD	5040-6058		
7	2	EXTRACTOR PC	5040-6009		
6	2	PIN GRV .062X.25	1480-0116		
5	5	SCR TAP 4-40 X.31	0624-0077		
4	1	SPACER	5020-7318		
3	1	LABEL	[illegible]		
2	88	SKT 16 DIP LOOS	1200-0607		
1	1	BOARD ETCHED	31040-60039		

TITLE: MEMORY ARRAY - 64 K ASSY. DRAWING		HEWLETT PACKARD
NEXT ASSEMBLY: 31204A		PART NUMBER: 31204-60001-1
FINISH	SCALE: 1:1	D 31204-60001-1
		SHEET 1 OF 1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED A-1720	WJS/RSE	2-14-78

MODULE ADDRESS

OCTAL THUMBWHEEL S1 -3100-3395

SETTING	4	2	1
0	H	H	H
1	H	H	L
2	H	L	H
3	H	L	L
4	L	H	H
5	L	H	L
6	L	L	H
7	L	L	L

RAS COMMON TO PIN 4 OF INDICATED ROW

CAS COMMON TO PIN 15 OF INDICATED ROW

[2] ALL ICS 1820- PREFIX EXCEPT RAM'S

[1] ALL R'S AND C'S IN OHMS AND MICROFARADS UNLESS NOTED

88 RAM CHIPS (4K OR 16K)

THESE SIGNALS COMMON TO ALL RAMS IN THE LOW ORDER HALF OF THE ARRAY

THESE SIGNALS COMMON TO ALL RAMS IN THE HIGH ORDER HALF OF THE ARRAY

TRI-STATE

P1-2,4,6,8,10,12,15,18,21 25,29,33,37,41,45,49

P2-18,28,35

P3-4,10,16,22,28,34,37,49

P4-18,20,22,24,26,28 35,45,46

E1-E4, E11, E12, E22

C1,20-23,25 31,51,60-64

C10,15,24,40-42,65,74

C2-5,11-14,35-38,43-46, 52-55,78-81

C6-9,16-19,30,32-34,39 47-50,56-59,73,75-77,82

0698-3041 R19 215

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

MEMORY ARRAY 128KB SCHEMATIC

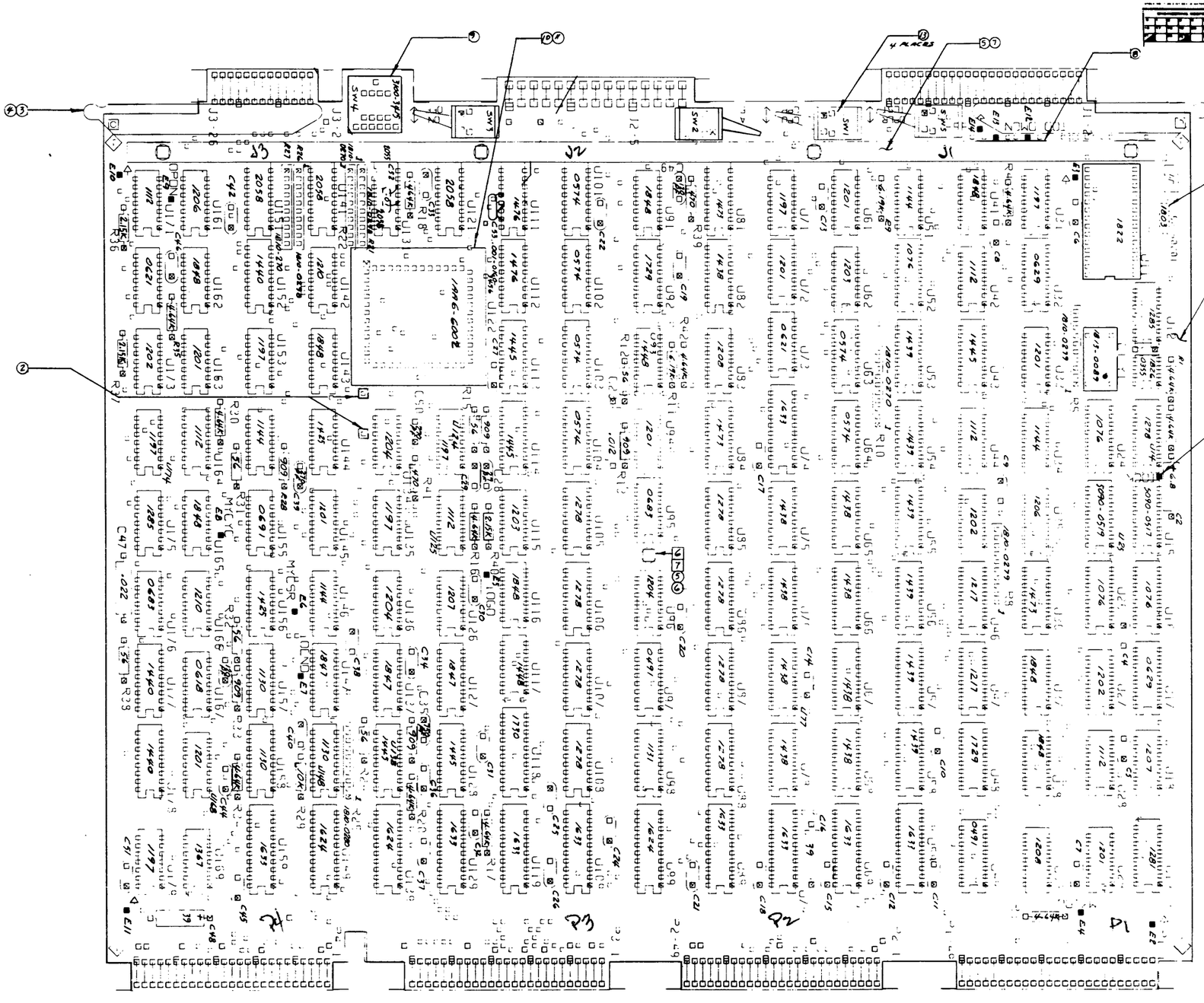
HEWLETT PACKARD

31204A

31204-60001

D-31204-60001-6

SHEET 1 OF 1



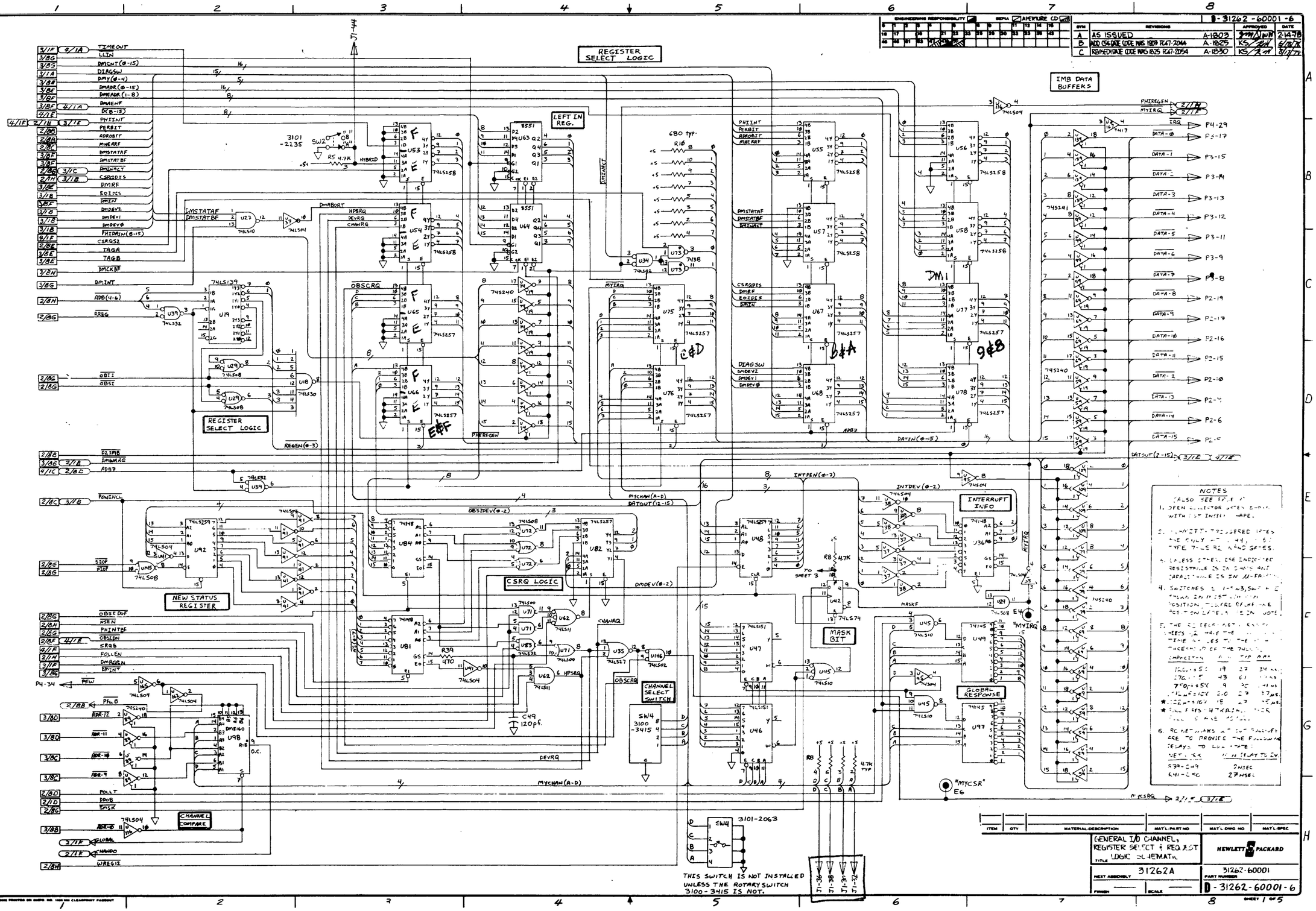
SILKSCREEN
COMPONENT SIDE
6 LAYER MULTILAYER SIDE
VIEW FROM THIS SIDE

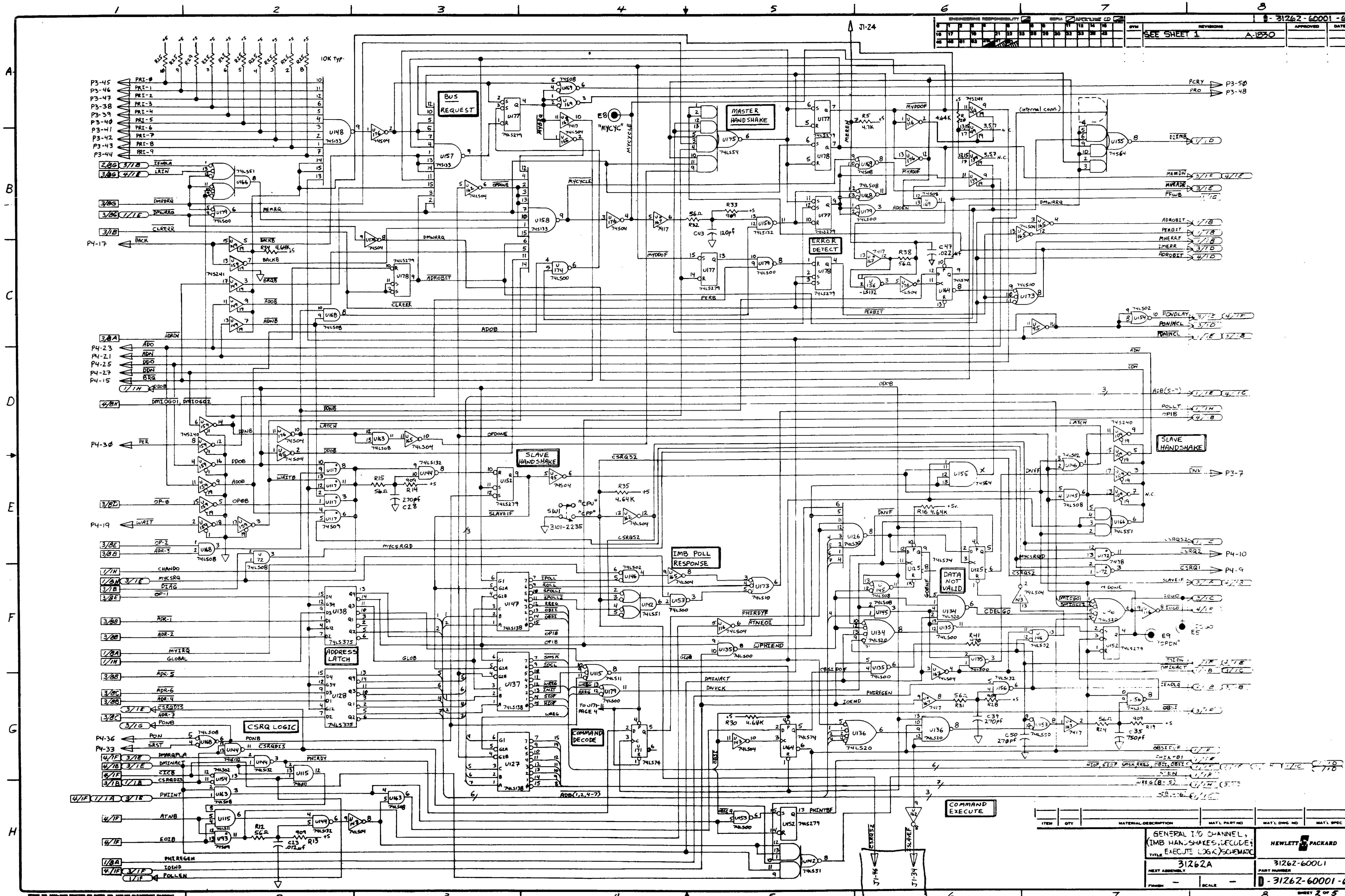
NOTES:
1. UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS
ALL RESISTORS 1/4 W 1% MF EXCEPT 56.1 & 470 ARE 5%
ALL CAPACITANCE IN MICRO FARADS
ALL CAPACITORS ARE .01 CER DISC.
ALL SWITCHES ARE 3101-2239
ALL IC'S ARE 1820-

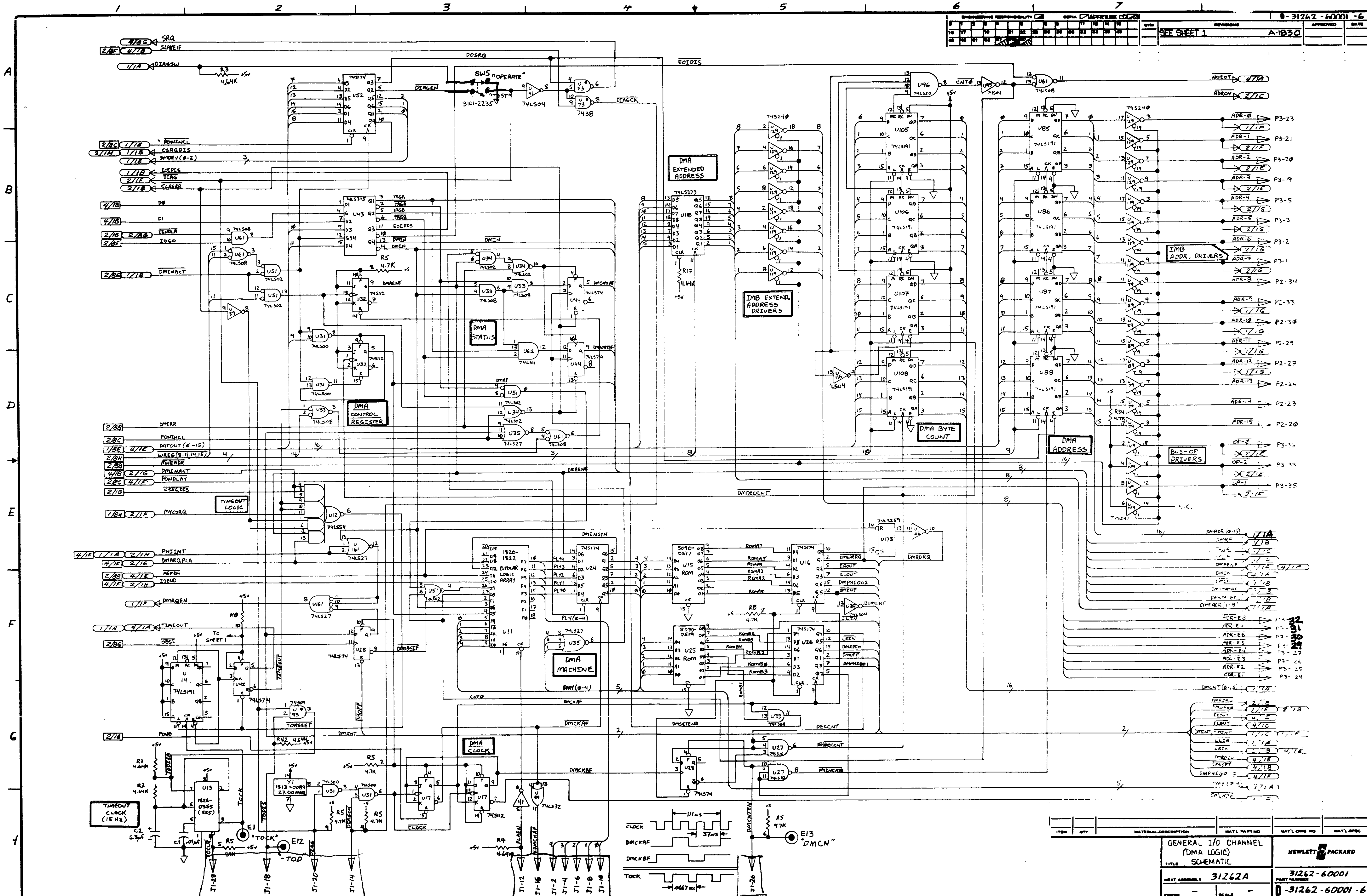
14	1	LABEL, WARRANTY	7020-6810		
13	4	SWITCH, TOGGLE DPDT	3101-2239		
12	1	DELETED			
11	1	PKT	1ARC-6002		
10	1	SOCKET, 48 PIN DS	1200-0650		
9	1	SWITCH, THMW, 16 POS	3100-3415		
8	1	LABEL	7120-6600		
7	1	BRACE, PC BD	5040-6058		
6	1	SPACER	5020-7518		
5	5	SCREW 4-40 X .31	0624-0077		
4	2	EXTRACTOR	5040-6009		
3	2	PIN GRV .062 X .250	1480-0116		
2	2	STUD, SOLDER TERMINAL	0360-1189		
1	1	BOARD ETCHED	31262-60001		

TITLE: GENERAL I/O CHANNEL		HEWLETT PACKARD	
SIZE: A	31262A	31262-60001	
SCALE: 2:1		F-31262-60001-1	

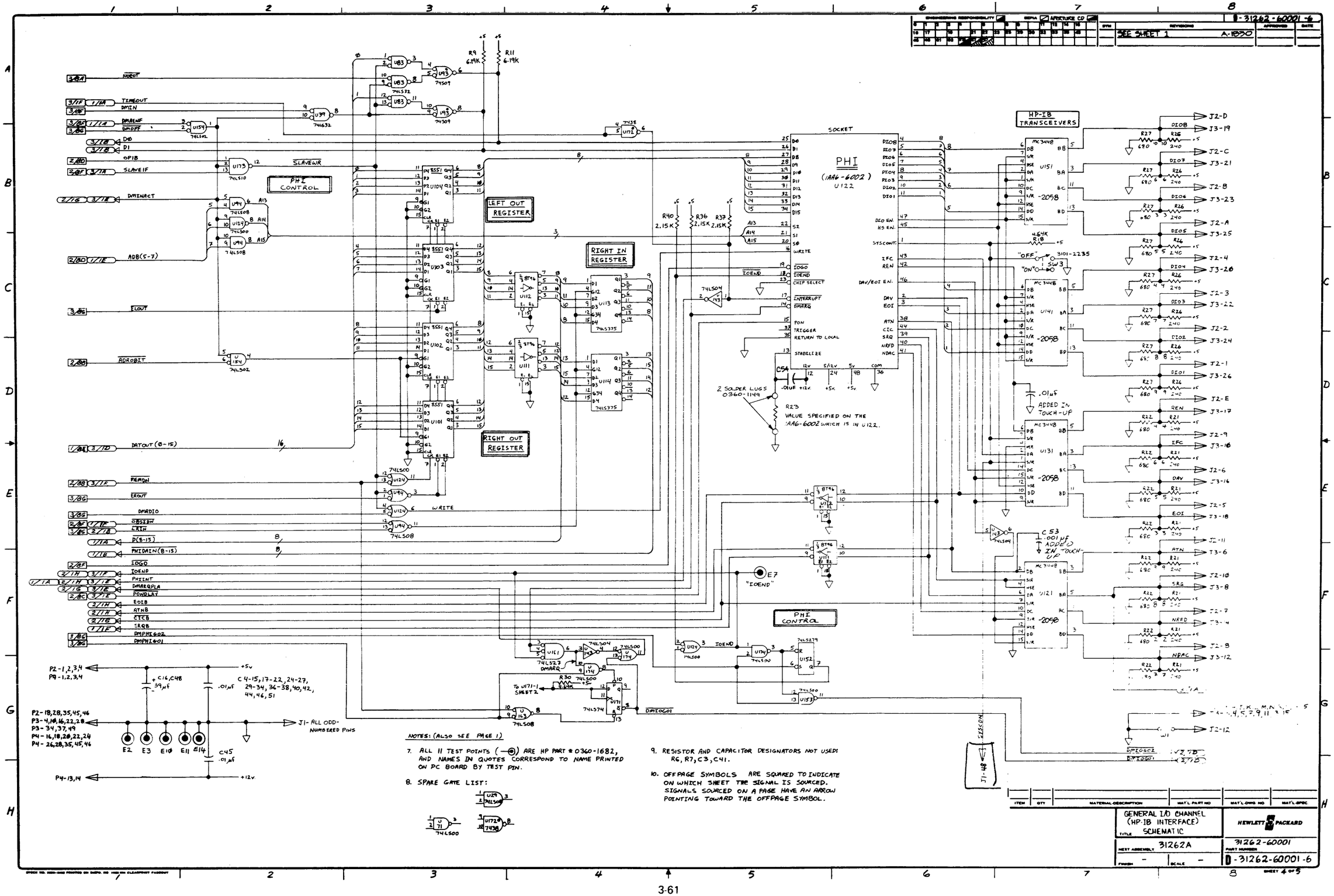
		REDRAWN — NO CHANGE	


REGISTER SELECT LOGIC
LEFT IN REG.
IMB DATA BUFFERS
INTERRUPT INFO
NEW STATUS REGISTER
CSRQ LOGIC
MASK BIT
GLOBAL RESPONSE
CHANNEL COMPARE
CHANNEL SELECT SWITCH
REGISTER SELECT LOGIC
TIMEOUT
LLIN
DMCNT(0-15)
DIAGSW
DMY(0-4)
DMABR(0-15)
DMAEAR(1-8)
DMAENF
DX(8-15)
PHINT
PERBIT
ADROBIT
MNERRF
DMSTATAF
DMSTATBF
DMINACT
CSRQDES
DMRF
EOIMCS
DMIEN
DMDEV2
DMDEV1
DMDEV0
PHIRDIN(8-15)
TAGA
TAGB
DMCKBF
DMINT
ADB(4-6)
RREG
OBTI
OBSI
DZIMB
DMAMRG
ADB7
PONINC
STOP
#STOP
OBSIDF
NSEN
PHINTDF
OBSIEN
SRQB
FOLLEN
DMRGEN
DRINT
PFW
PFLG
ADR-12
ADR-11
ADR-10
ADR-9
POLLT
DDOB
SMSK
ADR-8
GLOBAL
CHANDO
WREG12
REGEN(0-3)
DMABORT
HPSRQ
DEVRQ
CHANRQ
OBSCRQ
PHIREGEN
MYIRQ
MYCHAN(A-D)
DATOUT(12-15)
DMDEV(0-2)
INTPEN(0-7)
INTDEV(0-2)
DATIN(0-15)
MASKF
"MYIRQ"
"MYCSR"
"MRSRQ"
IRQ
DATA-0
DATA-1
DATA-2
DATA-3
DATA-4
DATA-5
DATA-6
DATA-7
DATA-8
DATA-9
DATA-10
DATA-11
DATA-12
DATA-13
DATA-14
DATA-15
DATOUT(2-15)
PHIREGEN
MYIRQ
SW2
3101-2135
R5 4.7K
HYBRID
680 TYP.
R10
R8 4.7K
R9 4.7K TYP
R39 470
C49 120pf.
SW4 3100-3415
SW4 3101-2063
THIS SWITCH IS NOT INSTALLED UNLESS THE ROTARY SWITCH 3100-3415 IS NOT.
J1-36
J1-38
J1-34
J1-32
TO SHEET 3
NOTES
(ALSO SEE TITLE 1)
1. OPEN COLLECTOR GATES SHOWN WITH DOT INSIDE GATE.
2. SCHOTTKY TRANSISTOR GATES ARE ONLY AVAILABLE IN 74LS TYPE TTL OR RZL NAND GATES.
3. UNLESS OTHERWISE INDICATED RESISTANCE IS IN OHMS ±5% CAPACITANCE IS IN MICROFARADS.
4. SWITCHES 1 THRU 3, SHOWN IN THEIR ENABLED POSITION, TOGETHER FORM THE BOARD ADDRESS SELECTION LOGIC.
5. THE FOLLOWING ABBREVIATIONS APPEAR ON SHEETS 1-4 AND THE TIMING NOTES TO THE RIGHT THEREOF ON THE TIMING DIAGRAMS:
IMPLICATION MIN TYP MAX
ACLO ↓ 5% 19 27 34 ns
ACLO ↑ 5% 43 61 77 ns
TOPS ↓ 5% 9 20 41 ns
TCLAS ↓ 5% 2.0 2.7 3.7 µs
★ TCEN ↓ 5% 15 27 45 ns
★ TALFPS ↓ 47K ±5% PULL UP RES TO +5
6. REMEMBER THAT THE FOLLOWING DELAYS TO LOW STATE:
NET - TYP 10 TTL LOAD
S38-S49 2 nsec
LS41-S50 27 nsec
GENERAL I/O CHANNEL, REGISTER SELECT & REQUEST LOGIC SCHEMATIC
HEWLETT PACKARD
31262A
31262-60001
D-31262-60001-6
SHEET 1 OF 5


BUS REQUEST
MASTER HANDSHAKE
ERROR DETECT
SLAVE HANDSHAKE
IMB POLL RESPONSE
DATA NOT VALID
ADDRESS LATCH
COMMAND DECODE
CSRQ LOGIC
COMMAND EXECUTE
"MYCYC"
"CPU"
"CPP"
SW1
3101-2235
"OPDN"
(internal conn.)
10K Typ.
P3-45 PRI-0
P3-46 PRI-1
P3-47 PRI-2
P3-38 PRI-3
P3-39 PRI-4
P3-40 PRI-5
P3-41 PRI-6
P3-42 PRI-7
P3-43 PRI-8
P3-44 PRI-9
P4-17 BACK
P4-23 ADO
P4-21 ADN
P4-25 DDO
P4-27 DDN
P4-15 BRQ
P4-30 PER
P4-19 WAIT
P4-36 PON
P4-33 SRST
PCRY P3-50
PRO P3-48
DNV P3-7
CSRQ2 P4-10
CSRQ1 P4-9
J1-24
J1-46
J1-34
SEE SHEET 1 A-1830
GENERAL I/O CHANNEL, (IMB HANDSHAKES, DECODE & EXECUTE LOGIC) SCHEMATIC
31262A
31262-60001
D-31262-60001-6
HEWLETT PACKARD
SHEET 2 OF 5


SW5 "OPERATE" "TEST"
3101-2235
DMA EXTENDED ADDRESS
IMB EXTEND. ADDRESS DRIVERS
DMA BYTE COUNT
DMA ADDRESS
IMB ADDR. DRIVERS
BUS-CP DRIVERS
DMA STATUS
DMA CONTROL REGISTER
TIMEOUT LOGIC
DMA MACHINE
DMA CLOCK
TIMEOUT CLOCK (15 Hz)
1820-1822 BIPOLAR LOGIC ARRAY
5090-0517 U15 ROM
5090-0519 U25 ROM
1813-0089 27.00 MHz
1826-0355 (555)
SRQ
SLAVEIF
DIAGSW
PONINCL
CSRQDIS
DMDEV(0-2)
EOIDIS
DIAG
CLRERR
D0
D1
IENDLA
IOGO
DMINACT
DMERR
DATOUT (0-15)
WREG (8-11,14,15)
MHEADR
PONDLAY
MYCSRQ
PHIINT
DMARQPLA
MEMON
IOEND
DMRQEN
TIMEOUT
OBST
PONB
DOSRQ
DIAGEN
DIAGCK
CNT0
NOEOT
ADROV
DMAENF
DMSTATAF
DMSTATBF
DMRF
DMIN
TAGA
TAGB
DMDECCNT
DMENSYN
PLY(0-4)
DMY(0-4)
DMCKAF
DMCKBF
DMSETEND
DECCNT
DMINCADR
DMWRRQ
DMRDRQ
EROUT
ELOUT
DMPHIGO2
DMINT
LLIN
LRIN
DMRDIO
DMOFF
DMPHIGO1
DMOBSIF
TORESET
TODIS
TOCK
DMCNTEN
ADR-0 P3-23
ADR-1 P3-21
ADR-2 P3-20
ADR-3 P3-19
ADR-4 P3-5
ADR-5 P3-3
ADR-6 P3-2
ADR-7 P3-1
ADR-8 P2-34
ADR-9 P2-33
ADR-10 P2-30
ADR-11 P2-29
ADR-12 P2-27
ADR-13 P2-24
ADR-14 P2-23
ADR-15 P2-20
OP-0 P3-36
OP-2 P3-33
OP-1 P3-35
ADR-E8 P3-32
ADR-E7 P3-31
ADR-E6 P3-30
ADR-E5 P3-29
ADR-E4 P3-27
ADR-E3 P3-26
ADR-E2 P3-25
ADR-E1 P3-24
DMADR (0-15)
DMCNT (0-15)
E1 "TOCK"
E12 "TOD"
E13 "DMCN"
J1-28 J1-18 J1-20 J1-14 J1-12 J1-16 J1-2 J1-4 J1-6 J1-8 J1-10 J1-26
CLOCK 111ns 37ns
DMCKAF
DMCKBF
TOCK .0667 sec
SEE SHEET 1 A-1830
GENERAL I/O CHANNEL (DMA LOGIC) SCHEMATIC
NEXT ASSEMBLY 31262A
PART NUMBER 31262-60001
D-31262-60001-6
HEWLETT PACKARD
SHEET 3 OF 5

ENGINEERING RESPONSIBILITY — SIEMA — APERTURE CD
REVISIONS — SEE SHEET 1 — A-1030
APPROVED — DATE
D-31262-60001-6



NOTES: (ALSO SEE PAGE 1)

7. ALL 11 TEST POINTS (—◎) ARE HP PART # 0360-1682, AND NAMES IN QUOTES CORRESPOND TO NAME PRINTED ON PC BOARD BY TEST PIN.

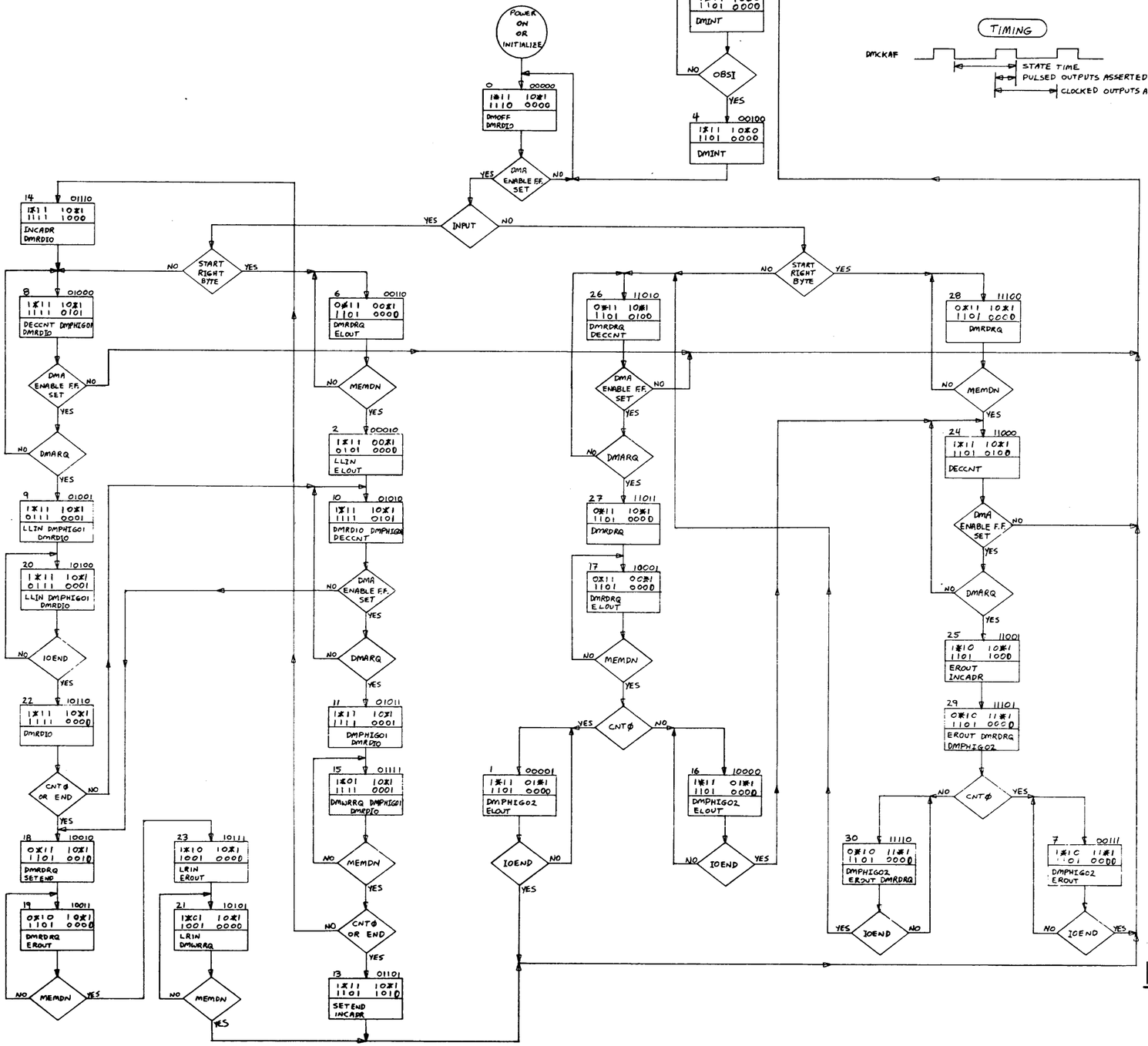
8. SPARE GATE LIST:

9. RESISTOR AND CAPACITOR DESIGNATORS NOT USED: R6, R7, C3, C41.

10. OFF PAGE SYMBOLS ARE SQUARED TO INDICATE ON WHICH SHEET THE SIGNAL IS SOURCED. SIGNALS SOURCED ON A PAGE HAVE AN ARROW POINTING TOWARD THE OFFPAGE SYMBOL.

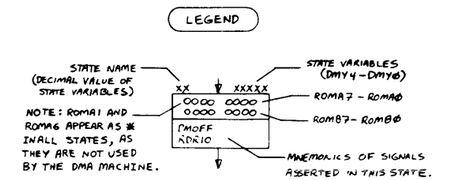
ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE	GENERAL I/O CHANNEL (HP-IB INTERFACE) SCHEMATIC
HEWLETT PACKARD	
NEXT ASSEMBLY	31262A
PART NUMBER	31262-60001
FINISH –	SCALE –
D-31262-60001-6	SHEET 4 OF 5



TIMING

LEGEND



MNEMONICS

- INPUTS

CNTØ	≡	BYTE COUNT REGISTER EQUALS ZERO.
DMARQ	≡	INPUT: INBOUND FIFO NOT EMPTY. OUTPUT: OUTBOUND FIFO NOT FULL.
IOEND	≡	PHI HANDSHAKE COMPLETED.
MEMDN	≡	MEMORY OPERATION COMPLETED.
OBSI	≡	IMB "OBSI" COMMAND HAS BEEN TRUE.
TAG	≡	TAG BITS D0,D1 OF PHI INDICATE END OF TRANSFER.

- OUTPUTS

DECCNT	≡	DECREMENT BYTE COUNT AND COMPLEMENT LEFT/RIGHT BIT ONCE IN THIS STATE.
DMINT	≡	ASSERT CSRQ + AFTER OBSI. CSRQ IS HELD OFF.
DMPHIGO1	≡	START WRITE TO PHI. THIS WILL PROVIDE A "FAST" PHI HANDSHAKE WHICH RELEASES IOGO AS SOON AS IOEND IS ASSERTED, ASYNCHRONOUS TO DMA MACHINE.
DMPHIGO2	≡	START READ FROM PHI. THIS PROVIDES A PHI HANDSHAKE WHICH RELEASES IOGO AS SOON AS MEMDN IS ASSERTED, ASYNCHRONOUS TO DMA MACHINE.
DMOFF	≡	DMA IS IDLE: RE-ENABLE ALL MSR'S AND ALLOW SLAVE ACCESS TO PHI.
DMRDIO	≡	SELECT PHI TO READ FIFO. IT IS SELECTED TO WRITE TO FIFO OTHERWISE. IN STATE Ø, THE SLAVE MAY OVERRIDE DMRDIO.
DMRDRQ	≡	REQUEST READ OF MEMORY.
DMWRRQ	≡	REQUEST WRITE TO MEMORY. THE CYCLE WILL NOT START UNTIL IOEND OR LRIN IS ASSERTED.
ELOUT	≡	GATE THE LEFT BYTE OUTPUT REGISTER TO THE PHI DATA LINES.
EROUT	≡	GATE THE RIGHT BYTE OUTPUT REGISTER TO THE PHI DATA LINES.
INCADR	≡	INCREMENT THE DMA ADDRESS REGISTER.
LLIN	≡	CLOCK PHI DATA LINES INTO LEFT BYTE INPUT REGISTER EACH STATE TIME AT DMCKAF↓.
LRIN	≡	LATCH PHI DATA LINES INTO RIGHT BYTE INPUT REGISTER.
SETEND	≡	SET DMA STATUS TO APPROPRIATE TERMINATION CODE.

NOTES

1. OUTPUTS OCCURRING IN CONSECUTIVE STATES DO NOT GLITCH BETWEEN STATES, EXCEPT LLIN, WHICH IS TAKEN DIRECTLY FROM THE DECODER ROM.
2. THESE INPUTS ARE ASYNCHRONOUS: IOEND, MEMDN, DMARQ, OBSI.
3. THE ONLY PULSED OUTPUTS ARE: DECCNT, SETEND.
4. BOTH OUTPUT DATA REGISTERS ARE LOADED AT OCCURRENCE OF MEMDN.
5. THE HP-IB "END" MESSAGE IS SENT IN STATES 7,16 UNLESS INHIBITED WITH A DMA CONTROL BIT.
6. MEMDN REMAINS ASSERTED UNTIL BOTH DMARDRQ AND DMARRQ ARE NOT ASSERTED.
7. ONCE DMRDRQ IS ASSERTED, THE MEMORY CYCLE WILL COMPLETE EVEN IF DMRDRQ IS REMOVED BEFORE MEMDN.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

GENERAL I/O CHANNEL (DMA MACHINE FLOWCHART) SCHEMATIC
TITLE

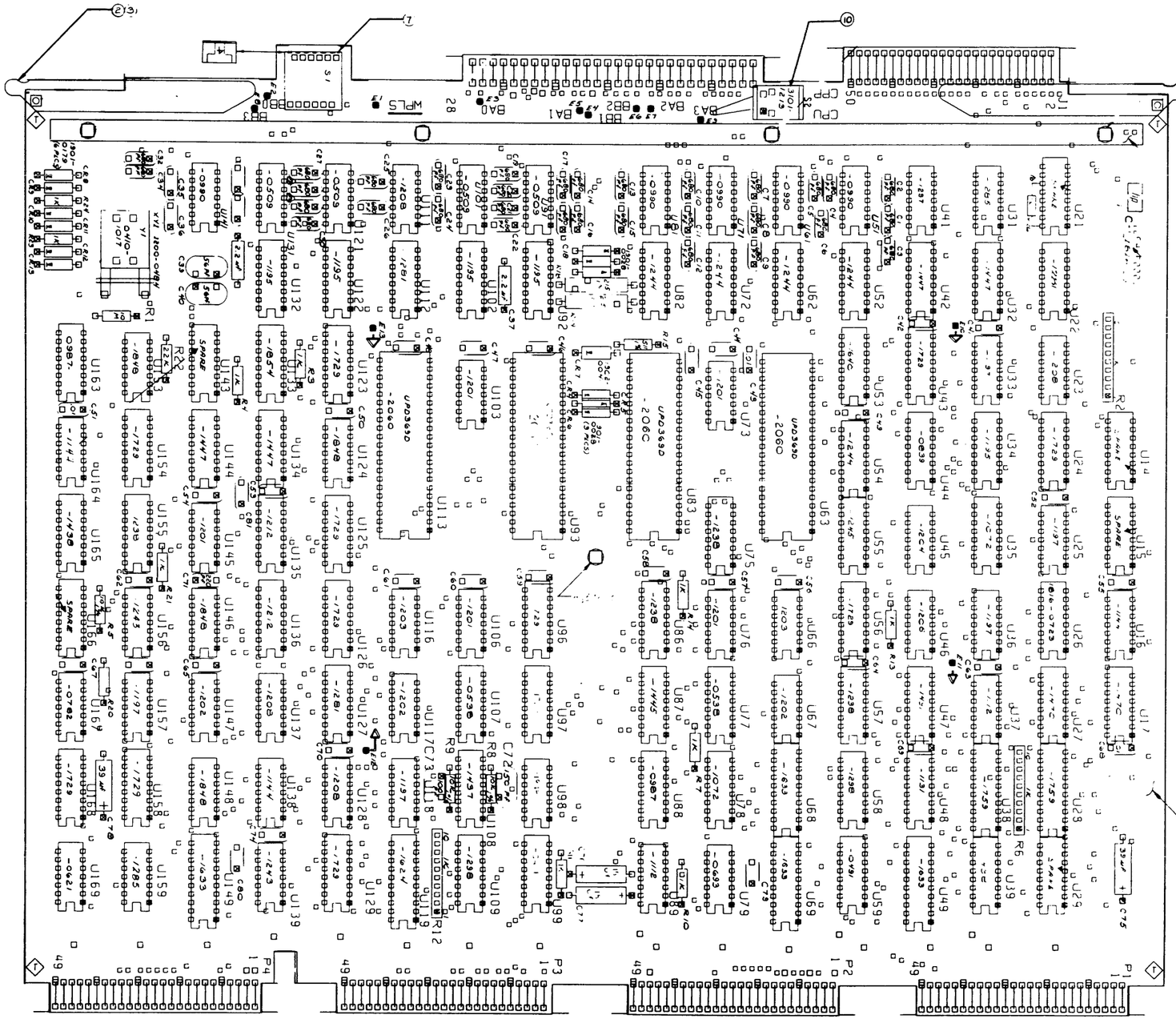
HEWLETT PACKARD

31262A
NEXT ASSEMBLY

31262-60001
PART NUMBER

FINISH - SCALE -

D-31262-60001-6
SHEET 5 OF 5



NOTES
1. UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/4W 5%
ALL CAPACITORS .01 MICRO FARADS
ALL IC'S ARE 1820-

..	1	LABEL: MANUALITY	7120-6890	
0	1	SW TGL S2	3101-1213	
9	1	LABEL	7120 6598	
8	.	XTAL 2.457M MHS	CRC-IC 7	
7	.	SWITCH-DEB. C-S 3	CRC 3324	
6	1	BRACE F. BOARD	CRC 6C58	
5	.	SPACER	SCDC-7318	
4	5	SCREW	CC24-0C74	
3	2	EXTR. TOOL	SCDC 6A6	
2	2	P/A	1820-C110	
		BOARD, P	31264-60001	

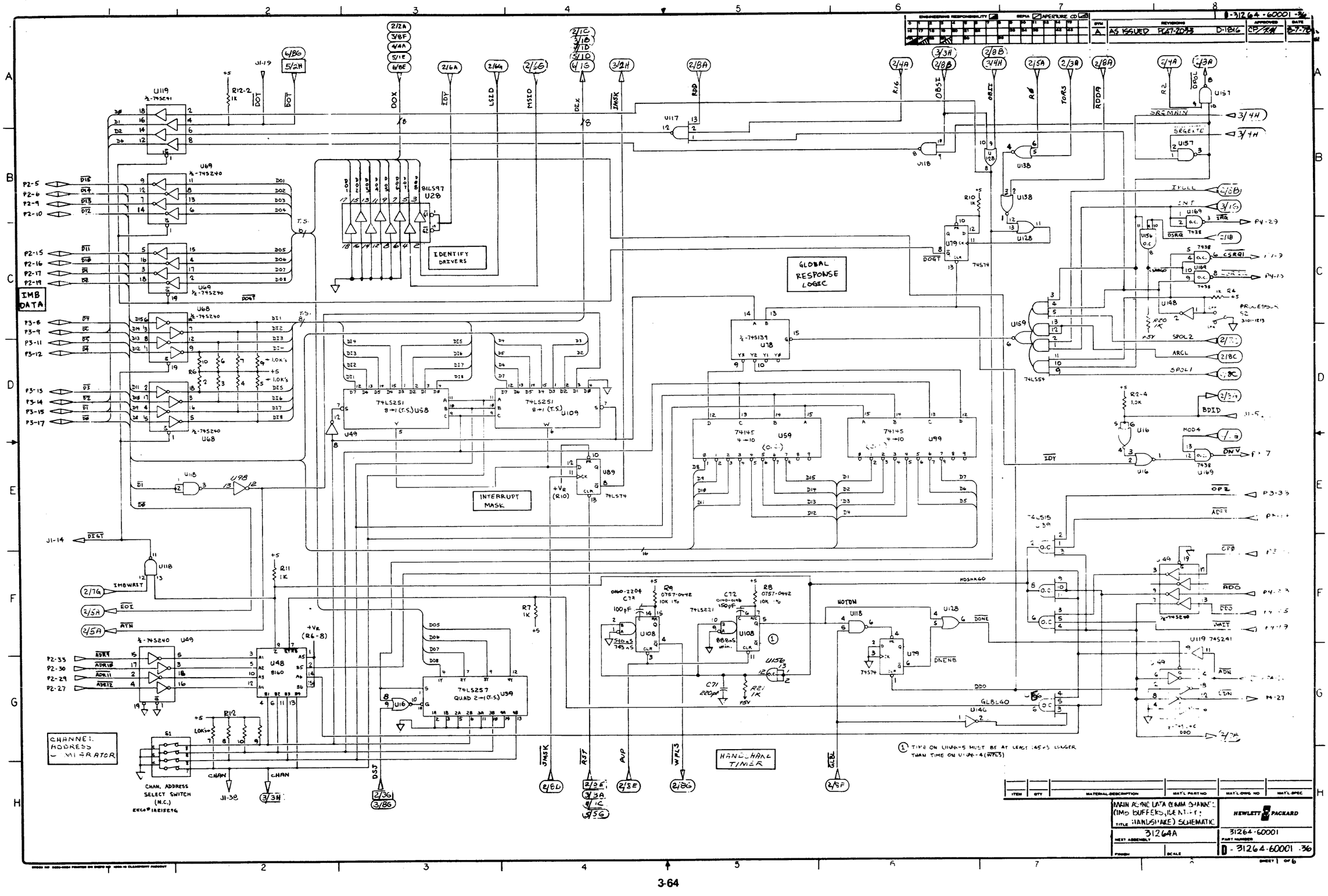
ADDC MAS MFG.

31264A

2/1

31264-60001

F-31264-60001-21


IMB DATA
GLOBAL RESPONSE LOGIC
IDENTIFY DRIVERS
INTERRUPT MASK
HANDSHAKE TIMER
CHANNEL ADDRESS SELECTOR
CHAN. ADDRESS SELECT SWITCH (N.C.)
74LS251 8→1 (T.S.) U58
74LS251 8→1 (T.S.) U109
74LS257 QUAD 2→1 (T.S.) U39
74145 4→10 U59
74145 4→10 U99
8T97 U29
8160 U48
74LS74
74LS04
74LS38
74LS54
74LS15
74LS241
74LS240
74LS139 U78
74LS221
MAIN ASYNC DATA CHANNEL (IMB BUFFERS, INTF. HANDSHAKE) SCHEMATIC
HEWLETT PACKARD
31264-60001
D-31264-60001 -36
31264A
SHEET 1 OF 6
(1) TIME ON U108-5 MUST BE AT LEAST 145nS LONGER THAN TIME ON U108-4 (WPLS)

REGISTERS 2 AND 16

REGISTER DECODER

CSRQ DISABLE

DEVICE ADDRESS LATCH

MODIFIER LATCH

MODIFIER DECODING

WRITE MODIFIERS:
- WMØ DATA
- WM1 UART CONTROL
- WM2 INTERFACE CONTROL
- WM3 SERVICE COND. MASKS
- WM4 CLEAR SPECIAL CHAR.
- WM5 SET SPECIAL CHAR.
- WM6 BAUD RATES SET
- WM7 STATUS REF/MASK

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

MAIN ASSEMBLY, DATA COMMUNICATIONS FUNCTION, PERIPHERAL INTERFACE

TITLE 12-MUX

HEWLETT PACKARD

31264A

NEXT ASSEMBLY

31264-60001

PART NUMBER

D-31264-60001-36

FINISH

SCALE

SHEET 2 OF 6

SERVICE CONDITION MASKS:

BIT #	CONDITION
0	XMIT BUFF NOT FULL
1	XMIT BUFF EMPTY
2	RCV BUFF NOT EMPTY
3	—

SERVICE CONDITION MASKS

SERVICE REQUEST LOGIC

BREAK DETECTION

INTERRUPT QUEUE

CHAN

PGT

DSJ

DST LOCS:
DST RETURN
READ 2
WRITE 1
STATUS 3
DEFAULT 3

MAIN ASYNC DATA COMM CHANNEL-POLL,DSJ,DBX1,INT SCHEMATIC

31264A

31264 60001

D - 31264-60001 -36

SHEET 3 OF 6

MODEM CONTROLS

UARTS

MC1488 POWER:
PIN 1 = -10V
PIN 7 = GND
PIN 14 = +10V

NOTE
WESTERN DIGITAL UARTS REQUIRE -12V ON PIN 2, DO NOT NEED -5 OR +12V.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

MAIN ASYNC DATA COMM CHANNEL JA23, MODEM CONTROL SCHEMATIC

HEWLETT PACKARD

31264A
NEXT ASSEMBLY

31264-60001
PART NUMBER

D-31264-60001-36

SHEET 4 OF 6

ENGINEERING RESPONSIBILITY: SDA ☑ ARSOURCE CP
8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36
SYM | REVISIONS | APPROVED | DATE
SEE SHEET 1 | D-1816
D - 31264 - 60001 - 36

BAUD RATE GENERATOR

BAUD RATE CODE DEFINITION

BAUD RATE CODE (BINARY)	BAUD RATE (BPS)	FREQUENCY (kHZ)
0000	(EXTERNAL)	—
0001	(EXTERNAL)	—
0010	50	0.8
0011	75	1.2
0100	134.5	2.133
0101	200	3.2
0110	600	9.6
0111	2400	38.4
1000	9600	153.6
1001	4800	76.8
1010	1800	28.8
1011	1200	19.2
1100	2400	38.4
1101	300	4.8
1110	150	2.4
1111	110	1.744

SPECIAL CHARACTER RAM

PROGRAM RUN LIGHT RESISTOR

(1) RB-13 ARE 1% 0179's

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE: MAIN ASYNC DATA COMM CHANNEL SPEC CHAR, BAUD GEN, HR, NS SCHEMATIC
NEXT ASSEMBLY: 31264A
FINISH | SCALE
NEWLETT PACKARD
PART NUMBER: 31264-60001
D - 31264 - 60001 - 36
SHEET 5 OF 6

RS-232 RECEIVERS

MODEM STATUS MONITOR

½-MC1489's

74LS153 DUAL MUX U82

74LS153 DUAL MUX U52

74LS153 DUAL MUX U72

74LS153 DUAL MUX U62

U53 74LS366 (T.S.)

74LS670 4X4 FILE T.S. U42

74LS670 4X4 FILE U32

U41 ¼-74LS266's

½-74LS139 U22

U31 74LS54

U123 74LS259 LATCH

U55 74LS253 DUAL MUX T.S.

STATUS REFERENCE

STATUS MASK

ALL C1-16 ARE 680pF

+V₂ (22-6)

1.0K 22-3

R2-9 1K +5V

R2-10 1K +5V

R2-8 1K +5V

R2-7 1K +5V

R3 1.0K

J1-40 CE0

J2-X J1-45 CE1

J2-R J1-48 CE2

J2-J J1-50 CE3

J2-26 SCF0

J2-19 SCF1

J2-M SCF2

J2-4 SCF3

J2-25 CF0

J2-16 CF1

J2-L CF2

J2-C CF3

J2-24 CC0

J2-15 CC1

J2-18 CC2

J2-2 CC3

J2-23 CB0

J2-14 CB1

J2-9 CB2

J2-B CB3

SCFREF CFREF CCREF CBREF

SCFMSK CFMSK CCMSK CBMSK

STCH3 STCH2 STCH1 STCH0 STCHX STCHM

SCFCH CFCH CCCH CBCH

BGQ2 BGQ1 BGQ0

N0 N1 WE7 LOADD

DI1 DI2 DI4 DI5 DI6

DOX DO0 DO1 DO2 DO3 DO4 DO5 DO6 DO7

BRK0 BRK1 BRK2 BRK3 BRKX

DMCE

3GT2 3GT1

J1-10 J1-6 J1-7 J1-9 J1-8 J1-2 J1-1 J1-3 J1-4

J1-46 J1-44

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

MAIN ACQ/CAL DATA CONTROL MICRO SYSTEM STATE SCHEMATIC

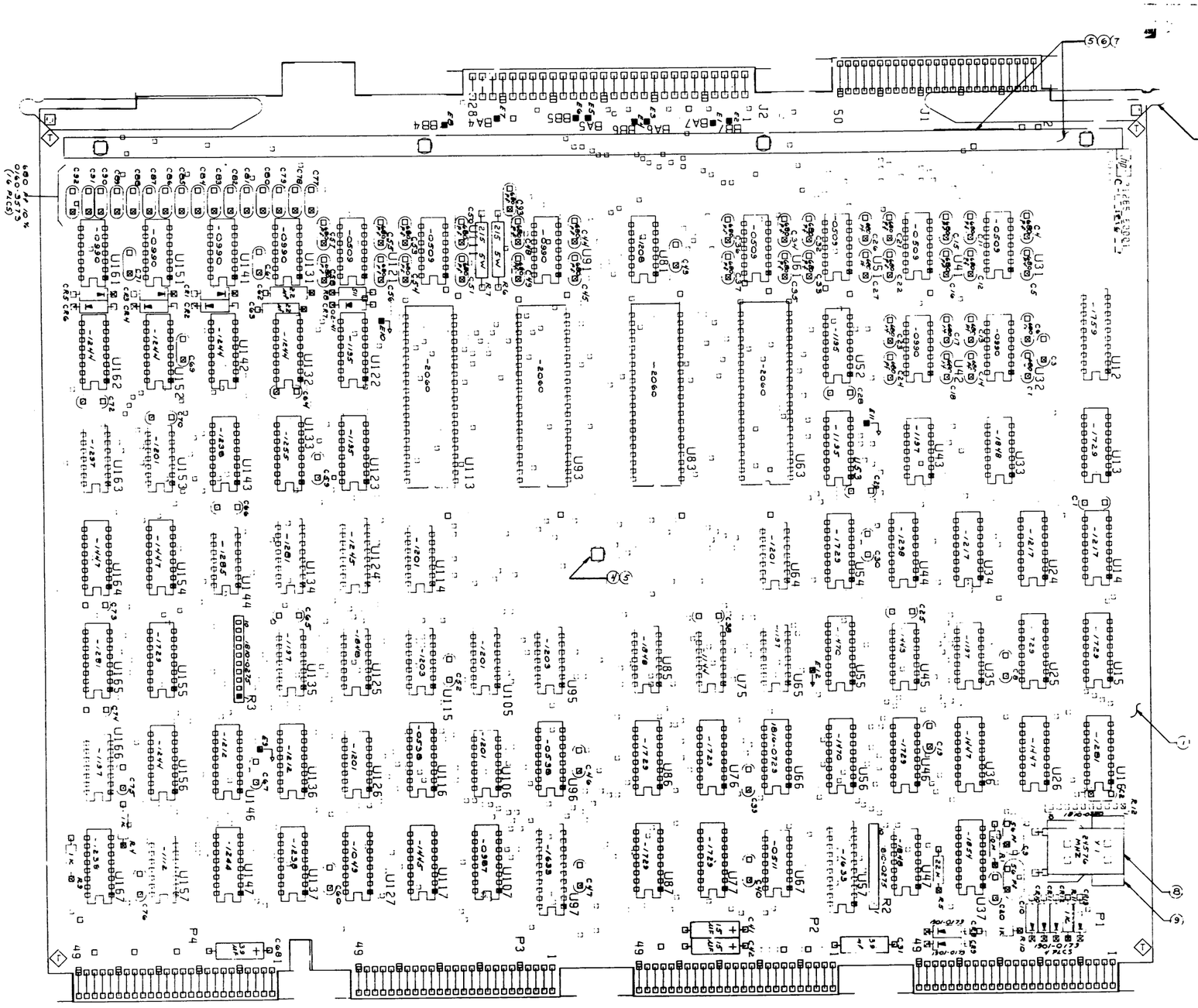
NEWLETT PACKARD

31264A

31264-60001

D-31264-60001-3/6

SHEET 6 OF 6



SILKSCREEN
COMPONENT SIDE

NOTES
1. UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS 1/4 W 1%
ALL CAPACITANCE IN MICRO FARADS
ALL CAPACITORS .01 CER DISC
ALL DIODES 1901-0028
ALL I.C.'S ARE 1820-

10	1	LABEL WARRANTY	7120-6890		
9	1	SOCKET CRYSTAL	200-1484		
8	1	CRYSTAL 24576 Y1	0410-1017		
7	1	LABEL	7120-6597		
6	1	GRACE, PC BOARD	5040-6458		
5	1	SPACER	5020-7318		
4	5	SCREW, TAP 4-40 X 3/1	0624-0077		
3	2	EXTRACTOR, P.C	5040-6009		
2	2	PIN, GROOVED	1480-0116		
	1	BOARD, ETCHED	3-1265-8001		

ADC EXTENDER ASSY	
3/1265A	3-1265-6000-
21	F-3-1265-6000-1-21

REVISIONS			
ECN		APPROVED	DATE
A	AS ISSUED C-1750	D. Hall	5-26-78
B	REMED: DATE CODE WAS 1750 PLUS 2096 C-1846	KS Hall	6-9-78
C	DATE CODE WAS 1846 PLUS 2096 C-1846	KS Hall	11-22-78

8-31265-60001-26

IMB DATA

OUTPUT DRIVERS

SPECIAL CHARACTER RAM

½ 74S240

½ 8L597

U55 74LS157 SELECT LOAD OR COMPARE

U56 74LS157 SELECT LOAD OR COMPARE

U66 93L415 1K RAM

R2 1K'S +5V

R12 10K'S +5V

R6 215Ω ½W J2-B +10V

R7 215Ω ½W J2-AA -10V

R8 511Ω -5V

CR1 CR3 CR5 CR2 CR4 CR6 1901-0028

CG1 CG2 CG3 15μf 20V 0180-1746

2.2μf 0180-0197

C31 C68 37μf 10V (TANT.) 0180-2355 (2)

(32) .01μf (CERAMIC) 0160-2055

TEST POINTS E9 E10 E11 E12

J1 5 10 24 30

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

EXTD ASYNC DATA COMM CHANNEL DRIVERS, RECEIVERS, SPEC CHAR

TITLE

HEWLETT PACKARD

NEXT ASSEMBLY 31265A

PART NUMBER 31265-60001

FINISH -0- SCALE -0-

D-31265-60001 26

SHEET 1 OF 3

BIT#	CONDITION
0	XMIT BUF NOT FULL
1	XMIT BUF EMPTY
2	RC BUF NOT EMPTY
3	——

SERVICE CONDITION MASKS

SERVICE REQUEST LOGIC

UART STATUS

BREAK DETECTION

DSJ LOGIC
DSJ RETURN
READ 0
WRITE 1
STATUS 2
DEFAULT 3

BREAK RQST. FF'S

DSJ CODE READ GATE

OBSI CODE READ GATE

RQST. PRIORITY ENCODER

RQST. LATCHES

SERVICE MASKS REG., DEVS. 4,5

SERVICE MASKS LOAD CONTROL

SERVICE MASKS REG., DEVS. 6,7

CHNL. PROG. HLT/RUN REG.

CHNL. PROG. NEW STATUS REG.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

EXTD ASYNC DATA COMM CHANNEL POLL, DSJ, OBSI, H/R, NS SCHEMATIC

NEWLETT PACKARD

31265A

31265-60001

D-31265-60001-26

SHEET 2 OF 5

ENGINEERING RESPONSIBILITY	REPRO	APERTURE CD

SYM	REVISIONS	APPROVED	DATE
	SEE SHEET 1 C-1846		

8-31265-60001-26

MODEM CONTROL

UARTS

MC1488 POWER:
PIN 1 = -10V
PIN 7 = GND
PIN 14 = +10

U113 MPD3690 UART DEVICE #4

U93 MPD3690 UART DEVICE #5

U83 MPD3690 UART DEVICE #6

U63 MPD3690 UART DEVICE #7

U54 74LS259 WRITE MOD.1 DECODER

U124 74LS155 WRITE MOD.0, READ MOD.0 DECODERS

U134 ½-74LS139 WRITE MOD.2 DECODER

U123 74LS175 DEV.#4 CMD. REG.

U122 74LS175 DEV.#5 CMD. REG.

U52 74LS175 DEV.#6 CMD. REG.

U53 74LS175 DEV.#7 CMD. REG.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L PART NO.	MAT'L SPEC NO	MAT'L SPEC.

EXTD ASYNC DATA COMM CHANNEL
UARTS, MODEM CONTROLS
TITLE SCHEMATIC

NEXT ASSEMBLY 31265A	HEWLETT PACKARD
FINISH - SCALE -	PART NUMBER 31265-60001
	D-31265-60001-26
	SHEET 3 OF 5

BAUD RATE GENERATOR

BAUD RATE CODE (BINARY)	BAUD RATE	FREQ (KHZ)
0000	EXTERNAL	
0001	EXTERNAL	
0010	50 BAUD	0.8 KHZ
0011	75	1.2 KHZ
0100	134.5	2.133 KHZ
0101	200	3.2 KHZ
0110	600	9.6 KHZ
0111	2400	38.4 KHZ
1000	9600	153.6 KHZ
1001	4800	76.8 KHZ
1010	1800	28.8 KHZ
1011	1200	19.2 KHZ
1100	2400	38.4 KHZ
1101	300	4.8 KHZ
1110	150	2.4 KHZ
1111	110	1.744 KHZ

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

EIA TD ASYNC DATA COMM CHANNEL
EUROPEAN MODEMS, BAUD GEN SCHEMATIC

NEXT ASSEMBLY: 31265A

HEWLETT PACKARD

PART NUMBER: 31265-60001

D - 31265-60001 26

SHEET 4 OF 5

R5-232 RECIEVERS

MODEM STATUS MONITOR

J2

MC1489's

U161 74LS368

U162 74LS153

U142 74LS153

U152 74LS153

U132 74LS153

U133 74LS368

U163 74LS266

U164 74LS670 STATUS REF. REG.

U154 74LS670 STATUS MASK REG.

U165 ½-74LS139

U144 74LS54

U155 74LS259

U143 74LS253

STATUS REF. & MASK LOAD CONTROL

NOTE: RAM, $\overline{BRKN}$ ARE "WIRE-AND'ED.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L SPEC NO	MAT'L SPEC

EXTD ASYNC DATA COMM CHANNEL
MODEM STATUS, READ STATUS
SCHEMATIC

HEWLETT PACKARD

31265A — 31265-60001

D-31265-60001-26

WIRING INFORMATION

SECTION IV

4-1. INTRODUCTION

The signal buses of the system interconnect the functional areas of the computer. The groups of signals making up the buses that interconnect the functional areas are listed in table 4-1. of this section.

4-2. INTER-MODULE CONNECTION

The Inter-module Bus (IMB) backplane is the data, control, and power path which interconnects the Memory, CPU, and I/O channels.

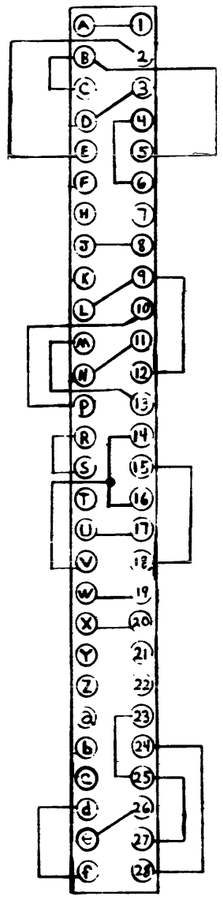
4-3. SYSTEM FLAT CABLES

The System´s flat ribbon cables and designator that list pin- by-pin the signals.

TABLE 4-1. WIRING INFORMATION INDEX

				5060-5563-1
A	AS ISSUED			3 7 77
B	REVISED PER PRCR "A"			6-21-77
C	ITEM 7 WAS 8150-2304 PL 41-2054	RS/0282		8-12-78
D	ADD 31000-67802 TO NEXT ASSY PL41-2061	RS		9-11-79

WIRING DIAGRAM



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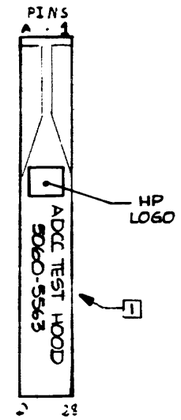

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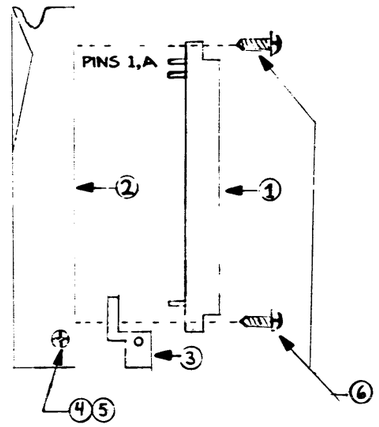
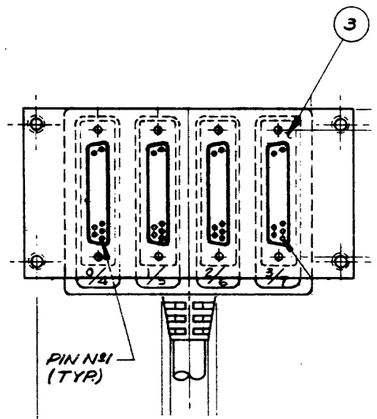


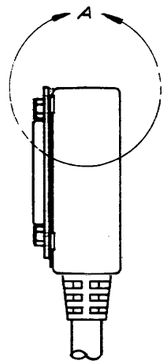
ITEM	QTY.	MATERIAL DESCRIPTION	MFG PART NO.	MFG NAME	MFG CODE
7	20 IN.	WIRE INS. BLK 24 AWG	8150-0447		
6	2	SCREW SELF-TAPPING POZI	0624-0098		
5	1	NUT #4-40 .187D	2760-0002		
4	1	SCREW #4-40 x .562L	2200-0091		
3	1	SUPPORT BLOCK	5040-7256		
2	1	HOOD CONNECTOR PC	5040-6071		
1	1	CONN PC 2 x 28 CONTACT	1251-4902		

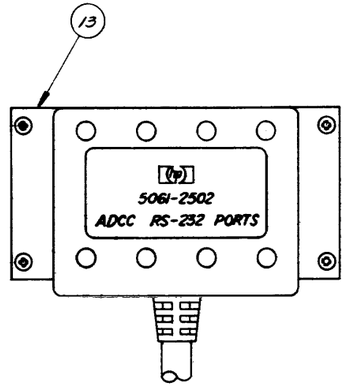
TITLE: ADCC TEST HOOD ASSEMBLY	HEWLETT-PACKARD
SIZE: 31000-67802, 30564, 31695A	DWG NO: 5060-5563
FINISH:	SCALE:
	REV: C-5060-5563-1

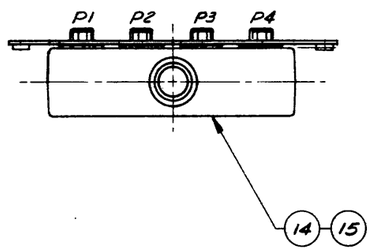
ENGINEERING RESPONSIBILITY	SEPIA

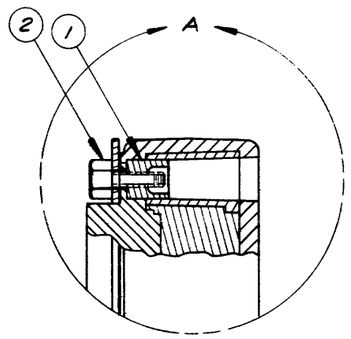
8-5061-2502-1			
BTH	REVISIONS	APPROVED	DATE
A	AS ISSUED		5-13-78
B	ADD NOTE 8 PER DCR ENG.		10-10-78



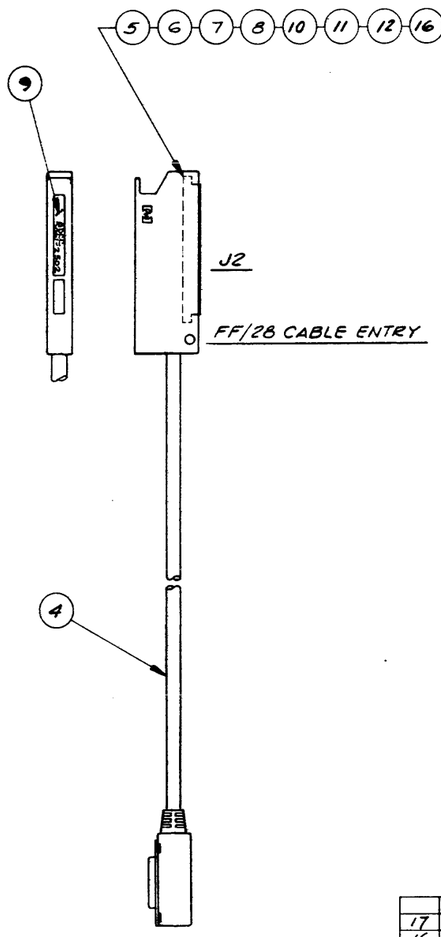








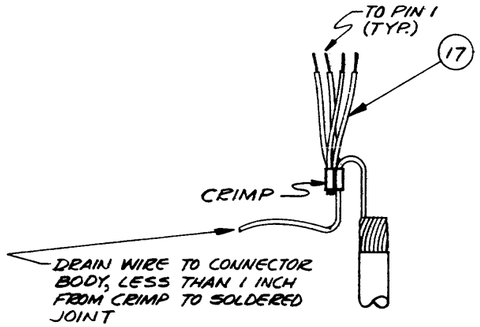
DETAIL A (2x)



WIRING INSTRUCTIONS

JUMPER LOCATIONS
- P1 : PIN 4 TO PIN 5
- P2 : PIN 4 TO PIN 5
- P3 : PIN 4 TO PIN 5
- P4 : PIN 4 TO PIN 5
- P1 : PIN 11 TO PIN 19
- P2 : PIN 11 TO PIN 19
- P3 : PIN 11 TO PIN 19
- P4 : PIN 11 TO PIN 19

FROM P1 THRU P4	TO J2 LOCATION			
PIN N°	P-1	P-2	P-3	P-4
1	DRAIN	DRAIN	DRAIN	DRAIN
2	FF	U	N	3
3	DD	17	11	D
4				
5	25	16	L	C
6	28	18	P	E
7	21	T	K	7
8	27	V	12	5
9				
10				
11	26	19	M	4
12	EE	W	13	6
13				
14				
15				
16				
17				
18				
19				
20	24	15	10	2
21				
22	23	14	9	B
23	20	S	8	A
24				
25	X	R	J	F



JUMPER WIRE CONNECTION DETAIL (NTS)

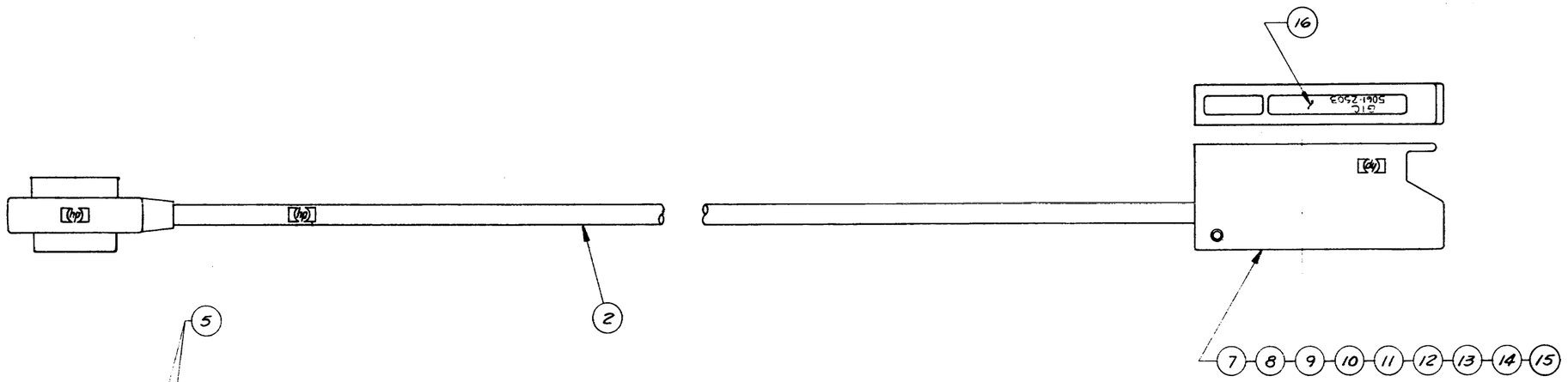
ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO.	MATL CONN. NO.	MATL SPEC
17	9"	WIRE, 22 AWG	8150-0005		
16	A/R	HOT MELT ADHESIVE	0470-0864		
15	A/R	HOT MELT ADHESIVE	0470-0850		
14	A/R	MOLDING COMPOUND	4093-0377		
13	1	PLATE, QUAD BOX	5001-1614		
12	3	CLAMP	5040-6055		
11	2	SCREW, TAPPING, 4-40 x .44	0624-0098		
10	2	SCREW, 4-48 x .375 FL HD	0624-0203		
9	1	LABEL	7120-7283		
8	1	HOOD, CONN.	5040-7265	B-1	
7	1	MOUNTING BLOCK	5040-6061	C-1	
6	1	CONN, PC BD., 56 PIN	1251-4902		
5	1	SCREW, SET, 6-32 x .50	3030-0143		
4	110"	CABLE	8120-2603		
3	4	CONN., SUB-D 25 PIN FEM	1251-0064		
2	8	JACKSOCKET, 4-40	1251-2294		
1	8	INSERT, THRD'D 4-40	5020-8168	A-1	

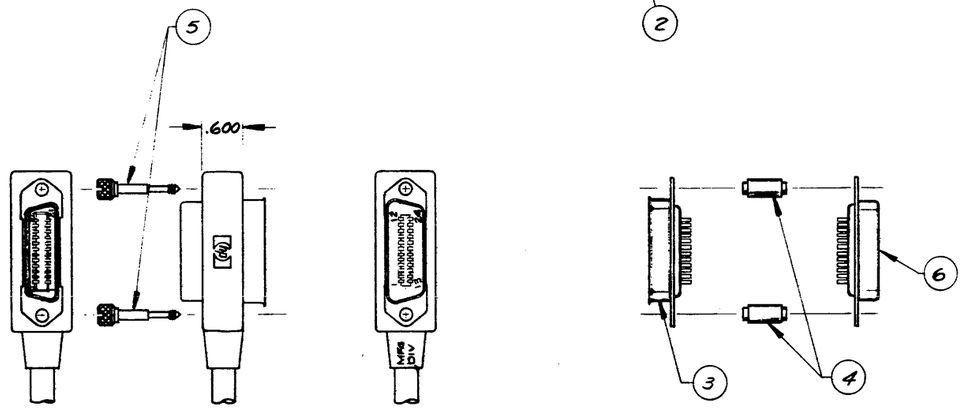
TITLE: CABLE ASSY. ADCC/TERM JPL	HEWLETT PACKARD	
NEXT ASSEMBLY: 30018A, 30070A	PART NUMBER: 5061-2502	
FINISH: FULL	SIZE: D	D-5061-2502-1

ENGINEERING RESPONSIBILITY	SEPIA

D-5061-2503-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	ADD NOTE 8 PER DCN 2H..		10-11-78





CONNECTOR ASSEMBLY DETAIL

P1

WHT/ORN	A	1	BRN
WHT/YEL	B	2	RED
WHT/GRN	C	3	ORN
WHT/BLU	D	4	YEL
WHT/VIO	E	5	GRN
WHT/GRA	F	6	BLU
WHT/BLK/BRN	H	7	VIO
WHT/BLK/RED	J	8	GRA
WHT/BLK/ORN	K	9	WHT
WHT/BLK/YEL	L	10	WHT/BLK
WHT/BLK/GRN	M	11	WHT/BRN
WHT/BLK/BLU	N	12	BLK
	P	13	
	R	14	
	S	15	

P1 CONNECTOR VIEWED FROM WIRING SIDE

FEMALE CONNECTOR

WHT/BLK/BLU	23	=	BLK
WHT/BLK/GRN			WHT/BRN
WHT/BLK/YEL	21	9	WHT/BLK
WHT/BLK/ORN			WHT
WHT/BLK/RED	19	7	GRA
WHT/BLK/BRN			VIO
WHT/GRA	17	5	BLU
WHT/VIO			GRN
WHT/BLU	15	3	YEL
WHT/GRN			ORN
WHT/YEL	13	1	RED
WHT/ORN			BRN

CABLE ENTRY CONNECTOR VIEWED FROM WIRING SIDE.

MALE CONNECTOR

BLK	23	=	WHT/BLK/BLU
WHT/BRN			WHT/BLK/GRN
WHT/BLK	21	9	WHT/BLK/YEL
WHT			WHT/BLK/ORN
GRA	19	7	WHT/BLK/RED
VIO			WHT/BLK/BRN
BLU	17	5	WHT/GRA
GRN			WHT/VIO
YEL	15	3	WHT/BLU
ORN			WHT/GRN
RED	13	1	WHT/YEL
BRN			WHT/ORN

CABLE ENTRY CONNECTOR VIEWED FROM WIRING SIDE.

CABLE ENTRY

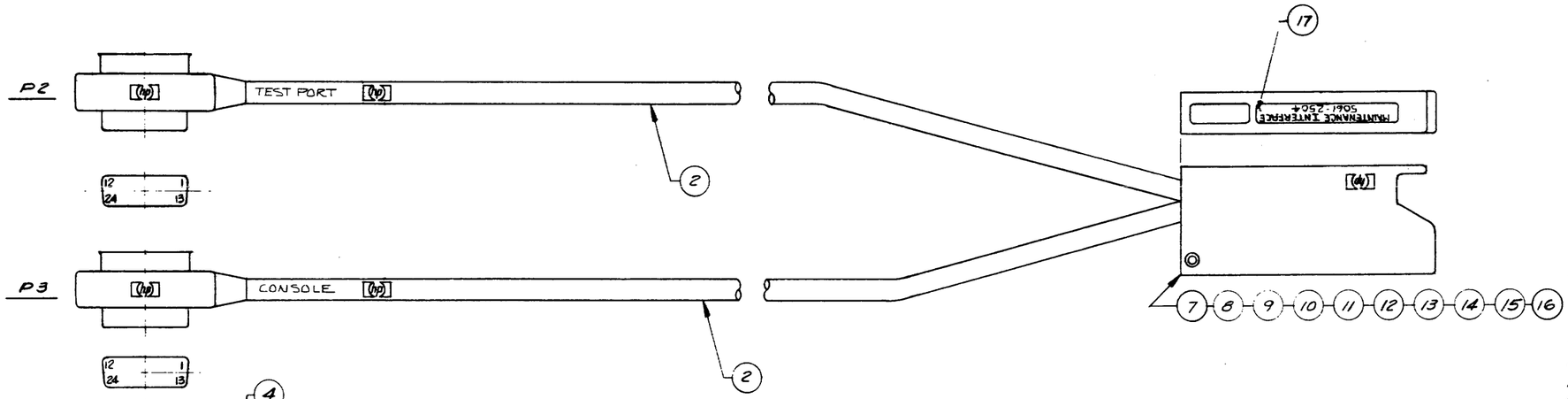
ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
17	A/R	WIRE, BLK, 22 AWG	8150-0005		
16	1	LABEL	7120-7284		
15	1	SCREW, *4-40×.25 FL.HD.	2200-0165		
14	1	SCREW, *4-40×.38 PN.HD.	2200-0145		
13	1	SCREW, SET	3030-0143		
12	1	SCREW, TAP	0624-0098		
11	3	CLAMP	5040-6055		
10	1	MOUNTING BLOCK	5021-0705		
9	1	CONNECTOR, 30 PIN	1251-0159		
8	1	HOOD	5040-7266		
7	A/R	ADHESIVE, HOT MELT	0470-0850		
6	1	CONN., 24 PIN FEMALE	1251-3283		
5	2	SCREW, MTG, METRIC	5021-0703		
4	2	SPACER, .500×.180 I.D.	0380-1031		
3	1	CONN., 24 PIN MALE	1251-3284		
2	6.0FT	CABLE	8120-1847		
1	A/R	MOLDING COMPOUND	4093-0376		

TITLE	CABLE ASSY.- GIC to HPIB JCTN. PANEL
NEXT ASSEMBLY	30070A, 30079A
FINISH	—
SCALE	NONE
HEWLETT PACKARD	
PART NUMBER	5061-2503
	D-5061-2503-1
SHEET	1 OF 1

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 15 4 8 9 17 18 9 10 11 12 14 18	
16 17 18 19 20 21 22 23 33 34 38 42 43	
82 83 90 93	

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	3/27/78
B	ADD NOTE 7 PER DOC CNG	[illegible]	12-11-78

5061-2504-1



ASSEMBLY DETAIL P2 & P3

TO		P1		TO
		A 1	1 B	
		2	2	
P2/16	WHT/BLU	3	3	YEL P2/4
P2/15	WHT/GRN	4	4	ORN P2/3
P2/14	WHT/YEL	5	5	RED P2/2
P2/13	WHT/ORN	6	6	BRN P2/1
P2/17	WHT/VIO	7	7	GRN P2/5
P2/18	WHT/GRA	8	8	BLU P2/6
P2/19	WHT/BLK/BRN	9	9	VIO P2/7
P2/20	WHT/BLK/RED	10	10	GRA P2/8
P2/21	WHT/BLK/ORN	11	11	WHT P2/9
P2/22	WHT/BLK/YEL	12	12	WHT/BLK P2/10
P2/23	WHT/BLK/GRN	13	13	WHT/BRN P2/11
P2/24 P3/24	WHT/BLK/BLU	14	14	BLK P2/12 P3/12
P3/23	WHT/BLK/GRN	15	15	WHT/BRN P3/11
P3/22	WHT/BLK/YEL	16	16	WHT/BLK P3/10
P3/21	WHT/BLK/ORN	17	17	WHT P3/9
P3/20	WHT/BLK/RED	18	18	GRA P3/8
P3/19	WHT/BLK/BRN	19	19	VIO P3/7
P3/18	WHT/GRA	20	20	BLU P3/6
P3/17	WHT/VIO	21	21	GRN P3/5
P3/16	WHT/BLU	22	22	YEL P3/4
P3/15	WHT/GRN	23	23	ORN P3/3
P3/14	WHT/YEL	24	24	RED P3/2
P3/13	WHT/ORN	A 25	25 B	BRN P3/1

CABLE ENTRY
CONNECTOR VIEWED FROM WIRING SIDE

TEST PORT

TO	P2		TO
P1/14B	BLK	WHT/BLK/BLU	P1/14A
P1/13B	WHT/BRN	WHT/BLK/GRN	P1/13A
P1/12B	WHT/BLK	WHT/BLK/YEL	P1/12A
P1/11B	WHT	WHT/BLK/ORN	P1/11A
P1/10B	GRA	WHT/BLK/RED	P1/10A
P1/9B	VIO	WHT/BLK/BRN	P1/9A
P1/8B	BLU	WHT/GRA	P1/8A
P1/7B	GRN	WHT/VIO	P1/7A
P1/3B	YEL	WHT/BLU	P1/3A
P1/4B	ORN	WHT/GRN	P1/4A
P1/5B	RED	WHT/YEL	P1/5A
P1/6B	BRN	WHT/ORN	P1/6A

CABLE ENTRY
CONNECTOR VIEWED FROM WIRING SIDE

CONSOLE

TO	P3		TO
P1/14B	BLK	WHT/BLK/BLU	P1/14A
P1/15B	WHT/BRN	WHT/BLK/GRN	P1/15A
P1/16B	WHT/BLK	WHT/BLK/YEL	P1/16A
P1/17B	WHT	WHT/BLK/ORN	P1/17A
P1/18B	GRA	WHT/BLK/RED	P1/18A
P1/19B	VIO	WHT/BLK/BRN	P1/19A
P1/20B	BLU	WHT/GRA	P1/20A
P1/21B	GRN	WHT/VIO	P1/21A
P1/22B	YEL	WHT/BLU	P1/22A
P1/23B	ORN	WHT/GRN	P1/23A
P1/24B	RED	WHT/YEL	P1/24A
P1/25B	BRN	WHT/ORN	P1/25A

CABLE ENTRY
CONNECTOR VIEWED FROM WIRING SIDE

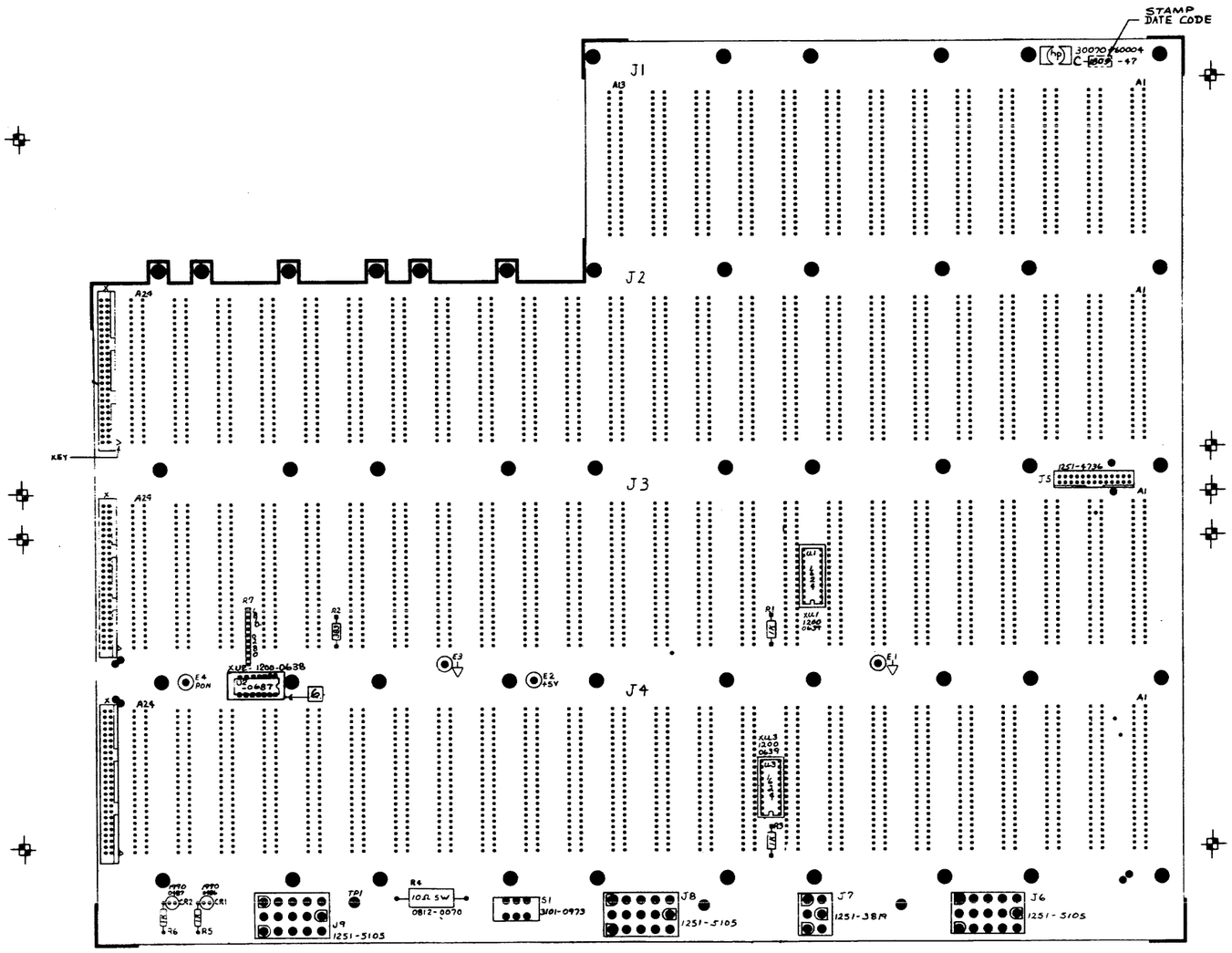
ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
17	1	LABEL	7120-7885		
16	2	SCREW, TAP 4-40 x .375 FL HD	0624-0203		
15	AR	ADHESIVE, HOT MELT	0470-0850		
14	2	SCREW, TAP 6-32 x .44 PN HD	0624-0098		
13	1	NUT, #4-40 x .187 D	2260-0002		
12	1	SCREW, #4-40 x .562 LG	2200-0091		
11	1	SET SCREW, #6-32 x .50	3030-0143		
10	2	CLAMP	5040-6055		
9	1	MOUNTING BLOCK	5040-6061		
8	1	HOOD	5040-6062		
7	1	CONN., PC 2x25 CONT.	1251-3106		
6	2	CONN., 24 PIN MALE	1251-3284		
5	2	SPACER, .500 x .180 I.D.	0380-1031		
4	4	SCREW, MTG - METRIC	5021-0703		
3	2	CONN., 24 PIN FEMALE	1251-3283		
2	6 FT	CABLE	8120-1847		
1	AR	MOLDING COMPOUND	4093-0376		

TITLE: CABLE ASSY MI TO HPIB JCTN. PANEL	HEWLETT PACKARD
NEXT ASSEMBLY: 30070A	PART NUMBER: 5061-2504
FINISH: —	SCALE: NONE
	D-5061-2504-1

SHEET 1 OF 1

TO BE SUPPLIED

TO BE SUPPLIED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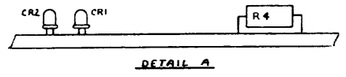
J1
J2
J3
J4
A13
A1
A24
A29
KEY
XU1 1200-0638
XU2 1200-0639
XU3 1200-0639
E1
E2 +5V
E3
E4 PON
R7
R2
R6 10Ω SW 0812-0070
S1 3101-0973
J8 1251-5105
J7 1251-3814
J6 1251-5105
J9 1251-5105
J5 1251-4736
TP1
CR1
CR2


CR2
CR1
R4

DETAIL A

ENGINEERING RESPONSIBILITY ▨ SEPIA ▨

0	1	2	3	4		6	8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	65									

C-30070-60004-51

SYM	REVISIONS	APPROVED	DATE
A	A3 ISSUED	[illegible]	1/13/82

J1

	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	
1					RA3							STBI		1
2					COM							RESET		2
3					R/W							RPAR		3
4					COM							BIRC		4
5					CAS							BWRQ		5
6					COM							BRRQ		6
7					REF							BX-Q3		7
8					COM							BX-Q1		8
9					LATCH							COM		9
10					COM							BXIR		10
11					C3							BBUSD		11
12					COM							LDBR		12
13					C-A0							BMEMA		13
14					C-A1							COM		14
15					COM							CPULLR		15
16					C-A2							COM		16
17					C-A3							INTCLR		17
18					COM							COM		18
19					C-A4							MARST		19
20					C-A5							NIR		20
21					COM							DATST		21
22					D0							IOAD		22
23					D1							ISR		23
24					D2							FRZ		24
25					COM							BUSEN		25
26					D3							CLR		26
27					D4							MICRO		27
28					D5							MACRO		28
29					COM							IRPT		29
30					D6							PEN		30
31					D7							CPU BUS E4		31
32					D8							E3		32
33					COM							E2		33
34					D9							E1		34
35					D10							E		35
36					D11							1		36
37					COM							2		37
38					D12							3		38
39					D13							4		39
40					D14							5		40
41					COM							6		41
42					D15							7		42
43					H0							8		43
44					H1							9		44
45					COM							10		45
46					H2							11		46
47					H3							12		47
48					H4							13		48
49					COM							14		49
50					H5							15		50
	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	

VIEWED FROM COMPONENT SIDE

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

PCA - BACKPLANE 1 SCHEMATIC (J1)
TITLE

HEWLETT PACKARD

30070-60003
NEXT ASSEMBLY

30070-60004
PART NUMBER

FINISH | SCALE

C-30070-60004-51

STOCK NO 9280-0003 PRINTED ON DIEPO NO 1020.10 CLEARPRINT FADEOUT

SHEET 1 OF 1

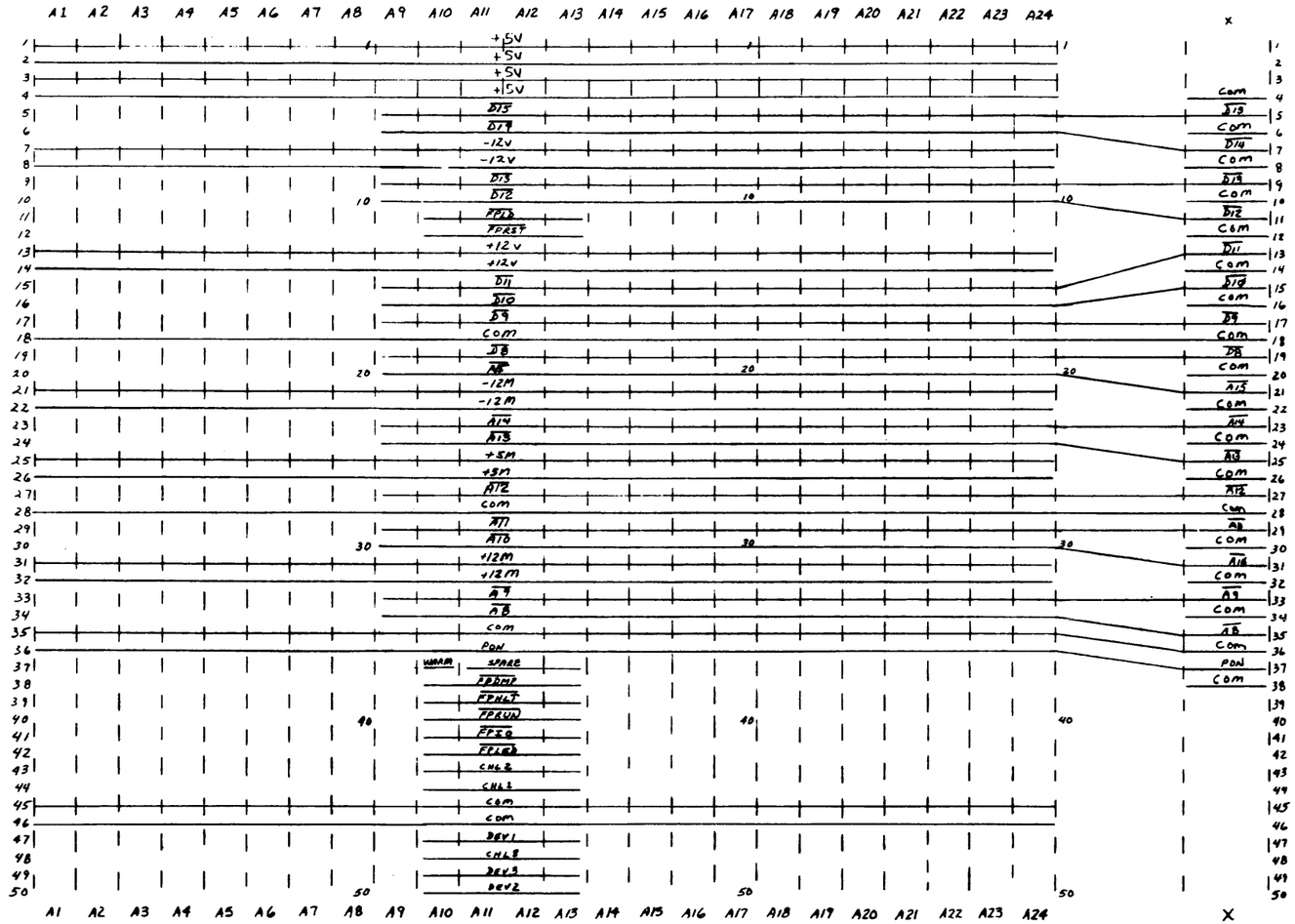
ENGINEERING RESPONSIBILITY — SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	26	29	30	32	33	38	43
45	46	61	63											

SYM	REVISIONS	APPROVED	DATE
A	AS 15506D	[illegible] 00	7/3/78
B	REVISED PER ECR CH63	QE	6/19/81

C-30070-60004-52

J2



VIEWED FROM THE COMPONENT SIDE

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO.	MAT'L DWG NO.	MAT'L SPEC.

TITLE: PCA-BACKPLANE 1 SCHEMATIC (J2)	HEWLETT PACKARD
NEXT ASSEMBLY: 30070-60003	PART NUMBER: 30070-60004
FINISH / SCALE	C-30070-60004-52

STOCK NO. 9280-0003 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT

SHEET 1 OF 1

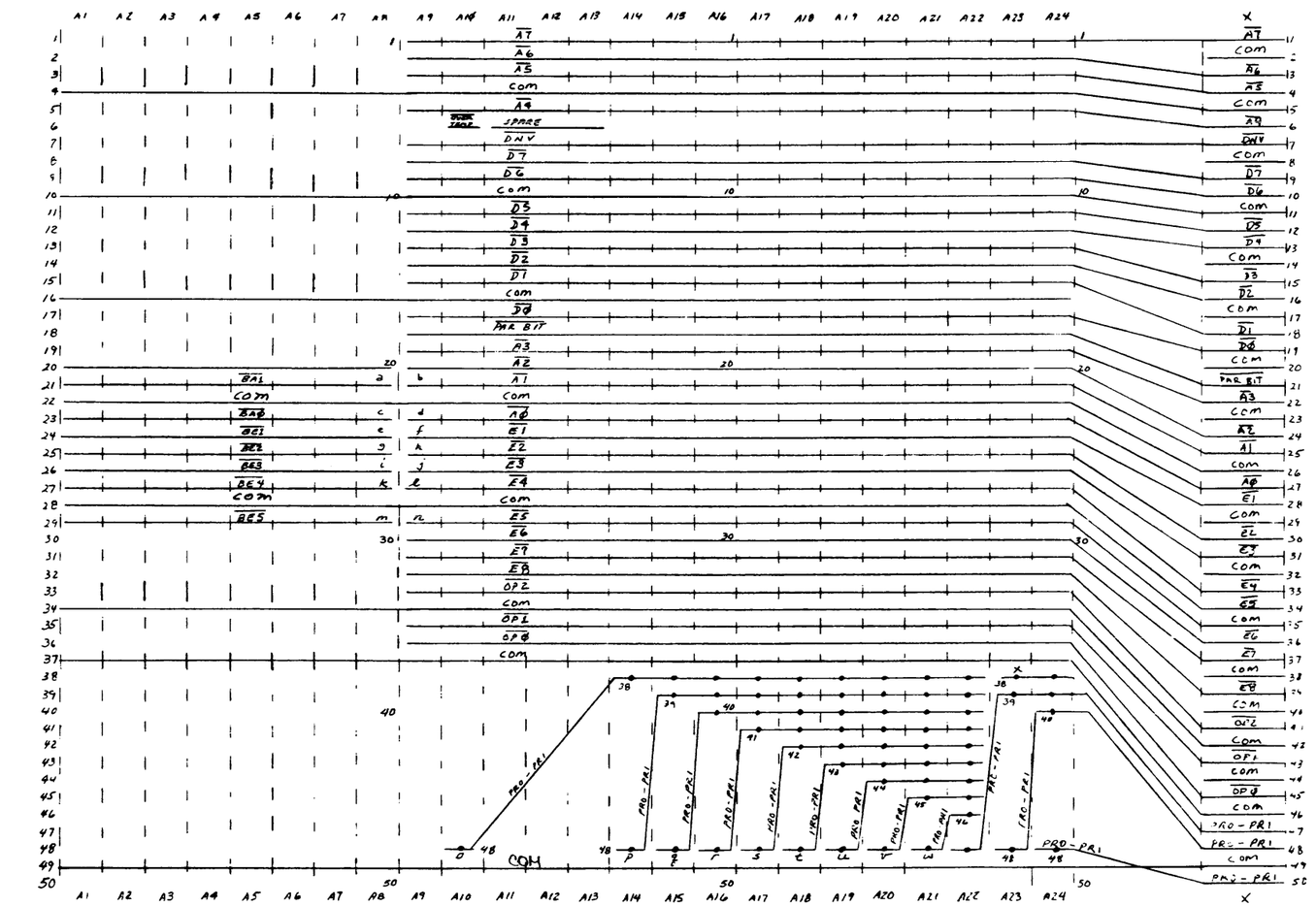
ENGINEERING RESPONSIBILITY — SCHEMA

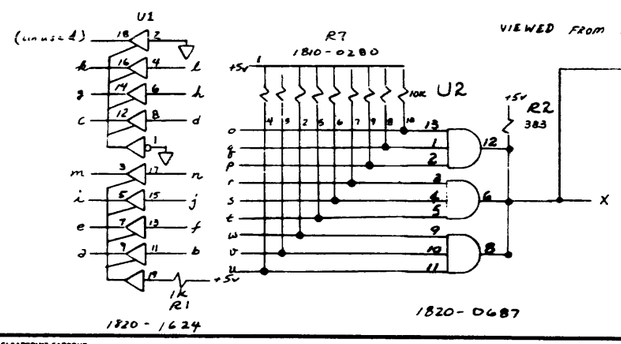
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	35	38	43
46	46	61	63	67										

E - 30070 - 60004 - 53

SYM	REVISIONS	APPROVED	DATE
A	AS 155469	DS / DB	1/13/78
B	REVISED TO PCA REV B	L.E	5/9/78
C	REVISED PER DOC. CHG.	L.E	6/19/78

J3





ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE: PCA - BACKPLANE 1 SCHEMATIC (J3)	HEWLETT PACKARD
NEXT ASSEMBLY: 30070-60003	PART NUMBER: 30070-60004
FINISH / SCALE	C - 30070 - 60004 - 53

STOCK NO 9280-0003 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT

SHEET 1 OF 1

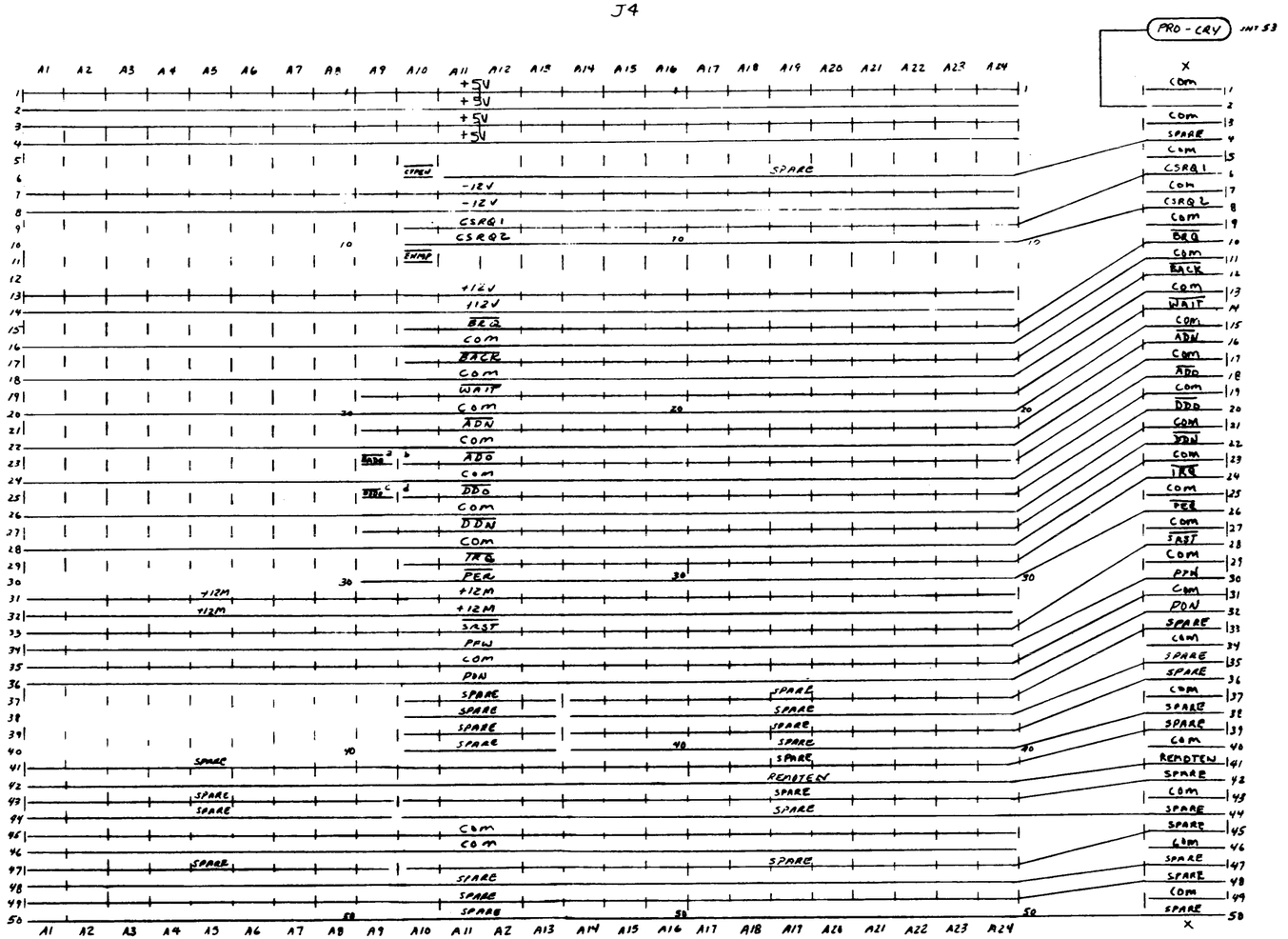
ENGINEERING RESPONSIBILITY — SEPIA

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	48	61	63	97										

E-30070-60004-54

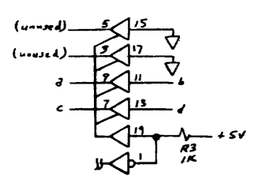
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	DS/DD	7/19/78
B	REVISED TO PCA REV B	DPE	5/4/79
C	REVISED PER ECL CHG.	DPE	6/19/79

J4



VIEWED FROM COMPONENT SIDE

U3



1820-1624

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG NO	MAT'L-SPEC.

TITLE: PCA-BACKPLANE 1 SCHEMATIC (J4)

HEWLETT PACKARD

NEXT ASSEMBLY: 30070-60003

PART NUMBER: 30070-60004

FINISH | SCALE

C-30070-60004-54

SHEET 1 OF 1

STOCK NO 9360 0003 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY ☑ SEPIA ☐

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
46	48	61	63	97										

C-30070-60004-55

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	GS/MA	7/13/78

J5

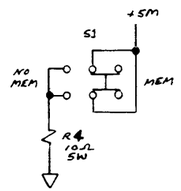
PIN		
1	FPRUN	J2-40
2	FPHLT	J2-39
3	FPLED	J2-42
4	FPRST	J2-12
5	FPLD	J2-11
6	WARM	J2-37
7	FPDMP	J2-38
8	CHL 1	J2-44
9	CHL 2	J2-43
10	CHL 3	J2-48
11	DEV 1	J2-47
12	DEV 2	J2-50
13	DEV 3	J2-49
14	OVERTEMP	J3-6
15	CFREN	J4-6
16	ENMB	J4-11
17	FPIO	J2-41
18	+5V	
19	+5V	
20	+5V	
21	COM	
22	COM	
23	COM	
24	COM	
25	COM	
26	COM	

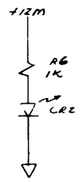
J6, J8, J9

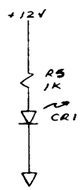
PIN→	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
J6	+5V	+5V	+5V	-12V	+5V	MEM	COM	COM	PON	+12V	11S	+12V	COM	COM	COM
J8	+5V	+5V	+5V	-12V	+5M	+5M	COM	COM	COM	+12V	-12V	+12S	COM	COM	COM
J9	+5V	+5V	+5V	-12V	+5V	—	COM	COM	COM	+12V	-12M	+12M	COM	COM	COM

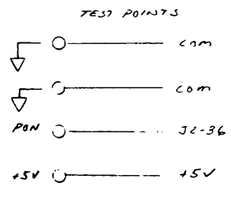
J7

PIN→	1	2	3	4	5	6
J7	—	COM	+12V	-12V	+5V	—









ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

PCA-BACKPLANE 1 SCHEMATIC (J5-J9)
TITLE

HEWLETT PACKARD

NEXT ASSEMBLY 30070 66003

PART NUMBER 30070-60004

FINISH | SCALE

C-30070-60004-55

SHEET 1 OF 1

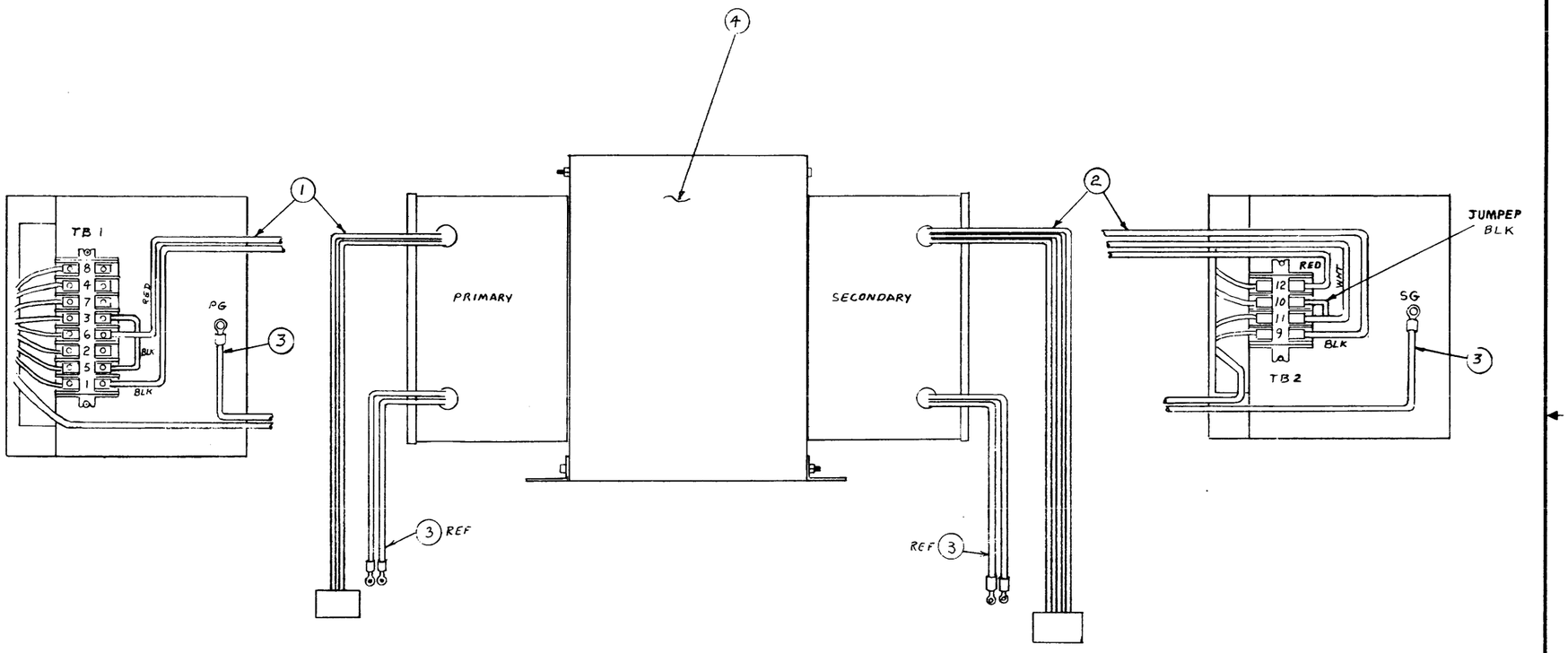
STOCK NO 9360-0003 PRINTED ON DIEPO NO 1030-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY														
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	67										

SEPIA

C-30070-60020-1

SYM	REVISIONS	APPROVED	DATE
A	[illegible]	JS/GJ	12/7/77
E	[illegible]	U/ES	9-7-78



VOLTAGE	WIRE BLACK	BLACK JUMPER		WIRE RED
200V	PIN 1	PIN 2	PIN 5	PIN 6
210V	" 1	" 3	" 5	" 6
220V	" 1	" 3	" 5	" 7
230V	" 1	4	" 5	" 7
240V	" 1	" 4	" 5	" 9

TABLE 1
PRIMARY VOLTAGE TAPPING

(NUMBERS IN TABLE REPRESENT TAPS ON ISOLATION TRANSFORMER)

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
4	1	TRANSFORMER - ISOLATION	9100-4062		
3	2	GRND STRAP	30070-60062		
2	1	CABLE - SECONDARY AC	30070-60022		
1	1	CABLE - PRIMARY AC	30070-60021		

ASSY. - ISOLATION TRANSFORMER
TITLE WIRING

HEWLETT PACKARD

NEXT ASSEMBLY 30070-60065

PART NUMBER 30070-60020

FINISH —

SCALE —

C-30070-60020-1

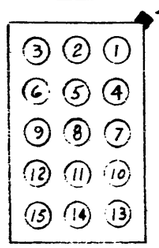
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY															SEPIA
0	1	2	3	4	5	6	7	8	9	10	11	12	14	15	
16	17	18	19	20	21	22			33	34	38		42	43	
47		63			90			93							

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	03/14	1/19/78

1 B-30070-60025-1

A



B

SAME AS "A"

PIN		AWG
1	BRN	14
2		14
3		14
4		14
5		22
6		22
7		14
8		22
9		22
10		14
11		22
12		22
13		14
14		14
15	BRN	14

POINT TO POINT

PIN		AWG
1	BRN	14
2		14
3		14
4		14
5		22
6		22
7		14
8		22
9		22
10		14
11		22
12		22
13		14
14		14
15	BRN	14

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
6	1	LABEL-BLANK	7120-1232		
5	1	MARKER-TIE	1400-0716		
4	14	CABLE TIE	1400-0493		
3	12	CONT CONN F	1251-5223		
2	2	CONN UTIL 15P	1251-5108		
1	18	CONT CONN F	1251-3818		

TITLE: ASSY-CABLE, DC PWR. BROWN	HEWLETT PACKARD
NEXT ASSEMBLY: 30070-60065, 30416A	PART NUMBER: 30070-60025
FINISH: —— SCALE: ——	B-30070-60025-1

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY ◪ SEPIA ▨

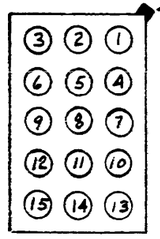
0	1	2	3	4	5	6	7	8	9	10	11	12	14	15
16	17	18	19	20	21	22			33	34	38		42	43
47		63			90			93						

1 B-30070 -60026 -1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	GS/CJ	7/9/78

A

KEY



PIN		AWG
1	ORN	14
2		14
3		14
4		14
5		14
6		14
7		14
8		14
9		14
10		14
11		22
12		22
13		14
14		14
15	ORN	14

← POINT TO POINT →

B

SAME AS "A"

PIN		AWG
1	ORN	14
2		14
3		14
4		14
5		14
6		14
7		14
8		14
9		14
10		14
11		22
12		22
13		14
14		14
15	ORN	14

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
6	1	LABEL-BLANK	7120-1232		
5	1	MARKER-TIE	1400-0716		
4	14	CABLE TIE	1400-0493		
3	4	CONT CONN F	1251-5223		
2	2	CONN UTIL 15P	1251-5108		
1	26	CONT CONN F	1251-3818		

TITLE: ASSY-CABLE, DC PWR
ORANGE

HEWLETT PACKARD

NEXT ASSEMBLY: 30070-60065, 30416A

PART NUMBER: 30070-60026

FINISH — SCALE —

B-30070-60026-1

SHEET 1 OF 1

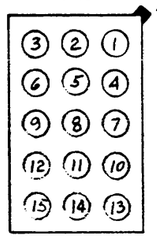
ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4	5	6	7	8	9	10	11	12	14	15
16	17	18	19	20	21	22			33	34	38		42	43
47 ◪		63			90			93						

1 B-30070-60027-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	05/05	1/19/78

A



B

SAME AS "A"

PIN		AWG
1	BLU	14
2		14
3		14
4		14
5		22
6		22
7		14
8		22
9		22
10		14
11		22
12		14
13		14
14		14
15	BLU	14

POINT TO POINT

PIN		AWG
1	BLU	14
2		14
3		14
4		14
5		22
6		22
7		14
8		22
9		22
10		14
11		22
12		14
13		14
14		14
15	BLU	14

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
6	1	LABEL-BLANK	7120-1232		
5	1	MARKER-TIE	1400-0716		
4	14	CABLE TIE	1400-0493		
3	10	CONT CONN F 22 GA	1251-5223		
2	2	CONN UTIL 15P	1251-5108		
1	20	CONT CONN F 14 GA	1251-3818		

ASSY-CABLE, DC PWR
BLUE
TITLE

HEWLETT PACKARD

30070-60065, 30416A
NEXT ASSEMBLY

30070-60027
PART NUMBER

FINISH —

SCALE —

B-30070-60027-1

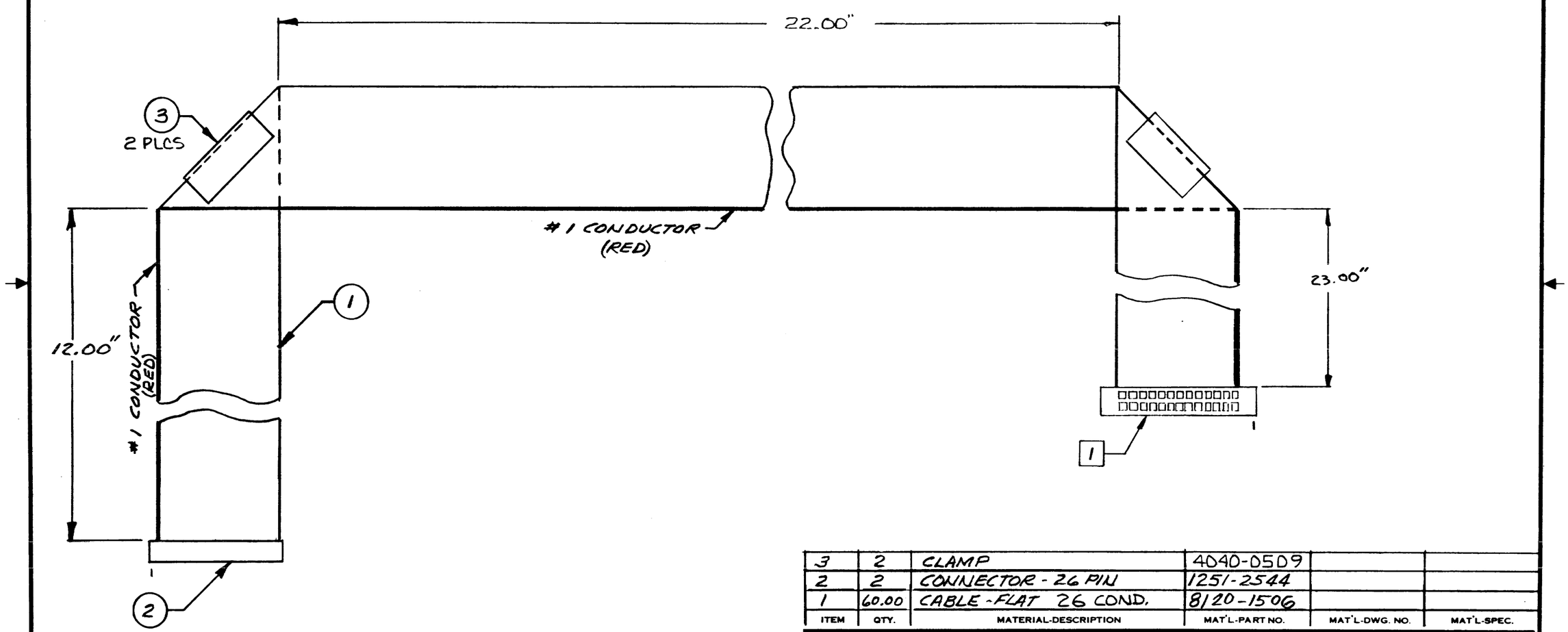
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	47											

SEPIA

B-30070-60030-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	BS/CH	11/10/77
B	ADD SECOND CLAMP & NOTE 2. PCD47-1462	JJ	7-28-78



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
3	2	CLAMP	4040-0509		
2	2	CONNECTOR - 26 PIN	1251-2544		
1	60.00	CABLE - FLAT 26 COND.	8120-1506		

TITLE: ASS'Y-CABLE SCP TO BP PERM. PRINT

HEWLETT PACKARD

NEXT ASSEMBLY: 30070-60028

FINISH:

SCALE:

PART NUMBER: 30070-60030

B-30070-60030-1

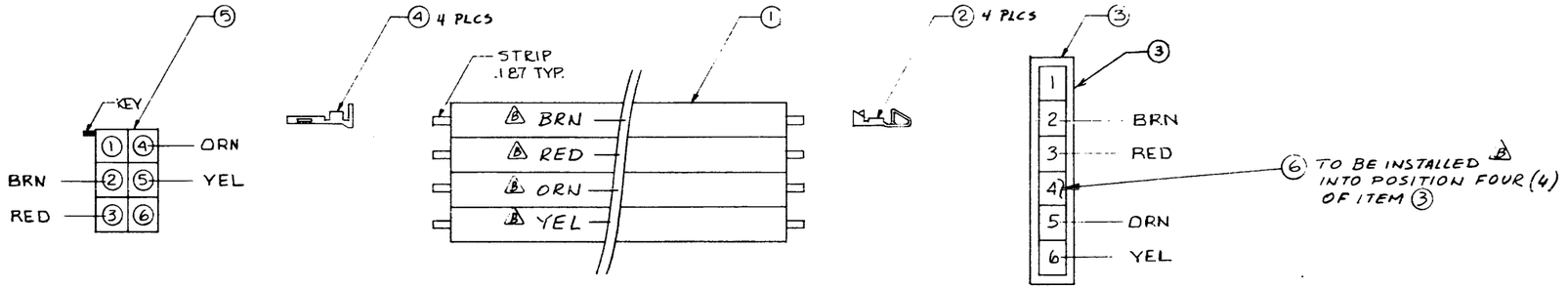
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	67										

C-30070-60034-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	12/2/77
B	PROD'R" ITEM 2 WAS 1251-0627, ITEM 4 WAS 1251-3818; ADD ITEM 6 AND LIST WIRE COLOR.	[illegible]	3-2-78
C	REMOVE CONDUCTOR #, ADD COLOR PR 047-1462 LF	[illegible]	7-28-78



ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
6	1	KEY-POST	1251-0627		
5	1	CONNECTOR 6 PIN MATE&LOCK	1251-3817		
4	4	CONTACT PIN-FEMALE	1251-3911		
3	1	CONNECTOR 6 PIN	1251-3275		
2	4	CONTACT	1251-3411		
1	56"	CABLE RIBBON-4 CONT. 28 AWG	8120-2647		

TITLE: CABLE-POWER DISC DC PERM. PRINT

NEXT ASSEMBLY: 30070-60026

FINISH: ---

SCALE:

HEWLETT PACKARD

PART NUMBER: 30070-60026

C-30070-60026

STOCK NO. 8280-0003 PRINTED ON DIEPO NO. 1020 10 CLEARPRINT FADEOUT

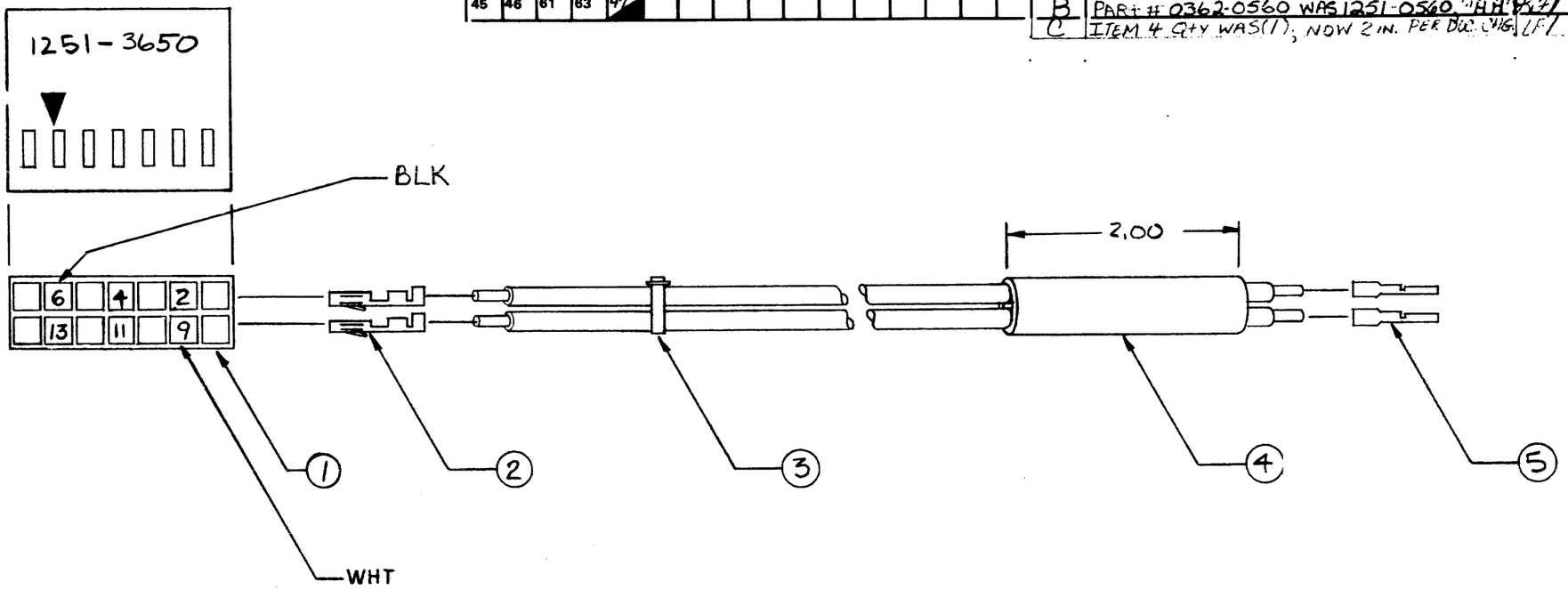
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	47 ◪											

B-30070-60035-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	12/22/77
B	PAR # 0362-0560 WAS 1251-0560, PREP HH	[illegible]	4-24-78
C	ITEM 4 QTY WAS (1), NOW 2 IN. PER DCC 0416	LF	9-25-78



ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.
5	2	LUG-CRIMP F	0362-0560		
4	2 IN.	TUBING-HS	0890-0029		
3	2	CABLE TIE	1400-0249		
2	6	CONTACT PIN	1251-5322		
1	1	CONNECTOR HOUSING	1251-3650		

ASS'Y.-CABLE
DISC STATUS LIGHT
TITLE

HEWLETT hp PACKARD

30070-60059
NEXT ASSEMBLY

30070-60035
PART NUMBER

FINISH —— SCALE ——

B-30070-60035-1

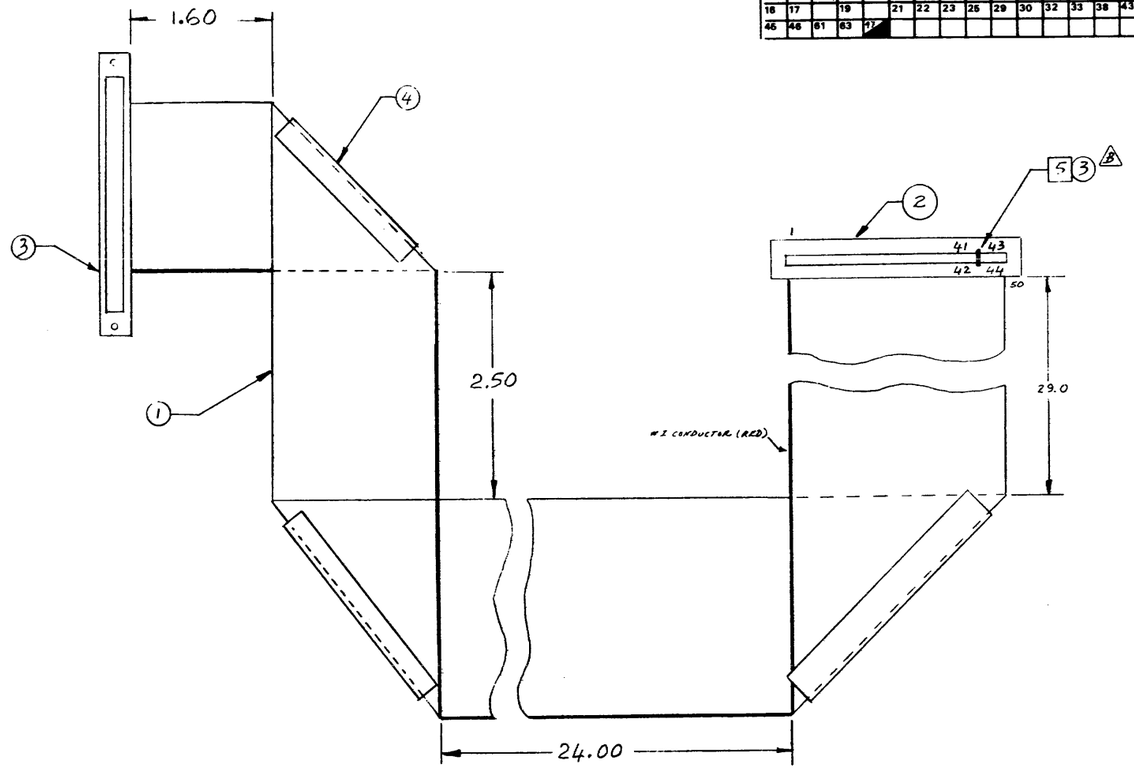
SHEET OF

ENGINEERING RESPONSIBILITY ☑ SEPIA ☐

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	97										

C-30070-60036-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	DS/DS	11/15/77
B	PER C-1" ADD KEY POST, ITEM 5, CHG. FOLDING PATTERN, ADD -0363	DS/DS	3-29-78



ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
B 5	1	KEY-POST	1251-5479		
4	3	CLAMP	4041-0509		
3	1	CONNECTOR - 50P	1251-2755		
2	1	CONNECTOR - 50P W/O MTG. EARS	1251-5504		
1	65.62	CABLE - FLAT 50 COND	8120-1595		

TITLE: ASSY - CABLE DISC TO CONTROLLER PERM. PRINT

NEXT ASSEMBLY: 30070-60028

FINISH: — SCALE: NONE

HEWLETT PACKARD

PART NUMBER: 30070-60036

C-30070-60036-1

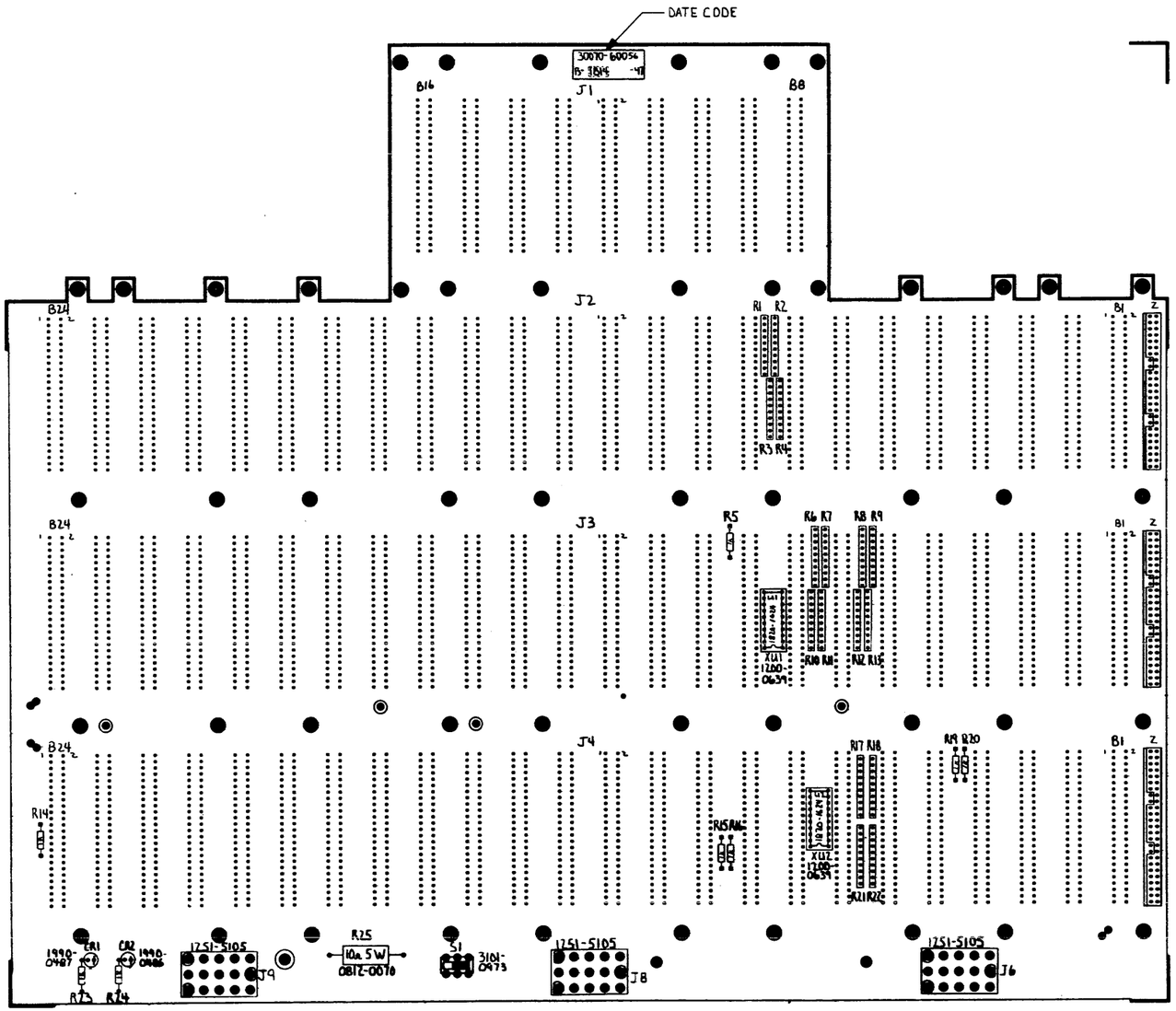
SHEET 1 OF 1

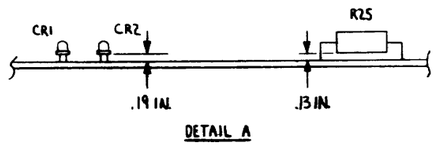
STOCK NO. 8483-0001 PRINTED ON CIE 90 NO. 1000 C BLUEPRINT FADELOUT

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 5 6 8 9 11 12 14 16	
16 17 18 21 22 23 25 29 30 32 33 36 43	
46 46 61 63 64	

30070-60056 -6

SYM	REVISIONS	APPROVED	DATE
A	AS 1534LD	CS/GE	5-8-78
B	ADDED NOTE 7 PER DOC. CHG.	LF/GE	6-14-78
C	CHG. NOTES PER PCO.47-1514	CSJ/TP	11-1-78





DETAIL A

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
1	1	PCB - BACKPLANE 2	30070-80056		

BACKPLANE 2 ASSEMBLY DRAWING CIRCUIT SIDE

30070A

DO NOT FINISH DRY-FILM SCALE FULL

PRINT HEWLETT PACKARD

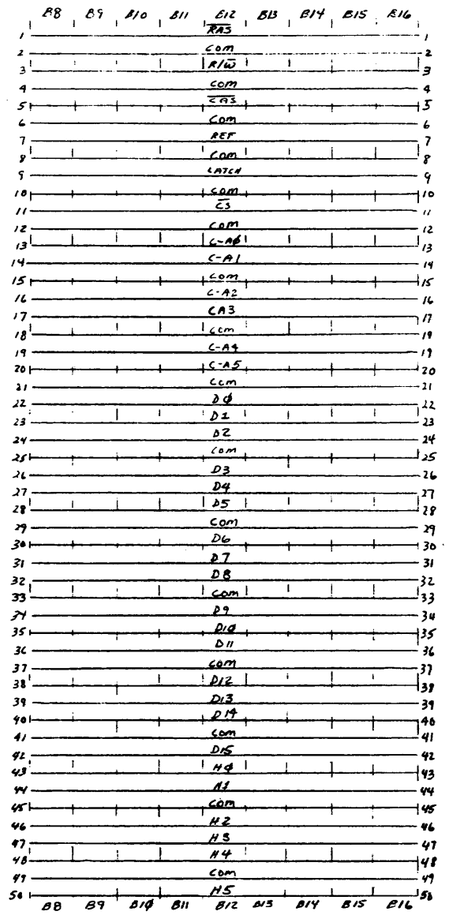
PART NUMBER 30070-60056

D - 30070 - 60056 - 6

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY								SEPIA							C-30070-60056-51		
0	1	2	3	4		6		8	9		11	12	14	15	SYM	REVISIONS	APPROVED / DATE
16	17		19		21	22	23	25	29	30	32	33	38	43	A	AS ISSUED	DS 4-19-82
45	46	61	63	97													

J1



VIEWED FROM THE COMPONENT SIDE

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

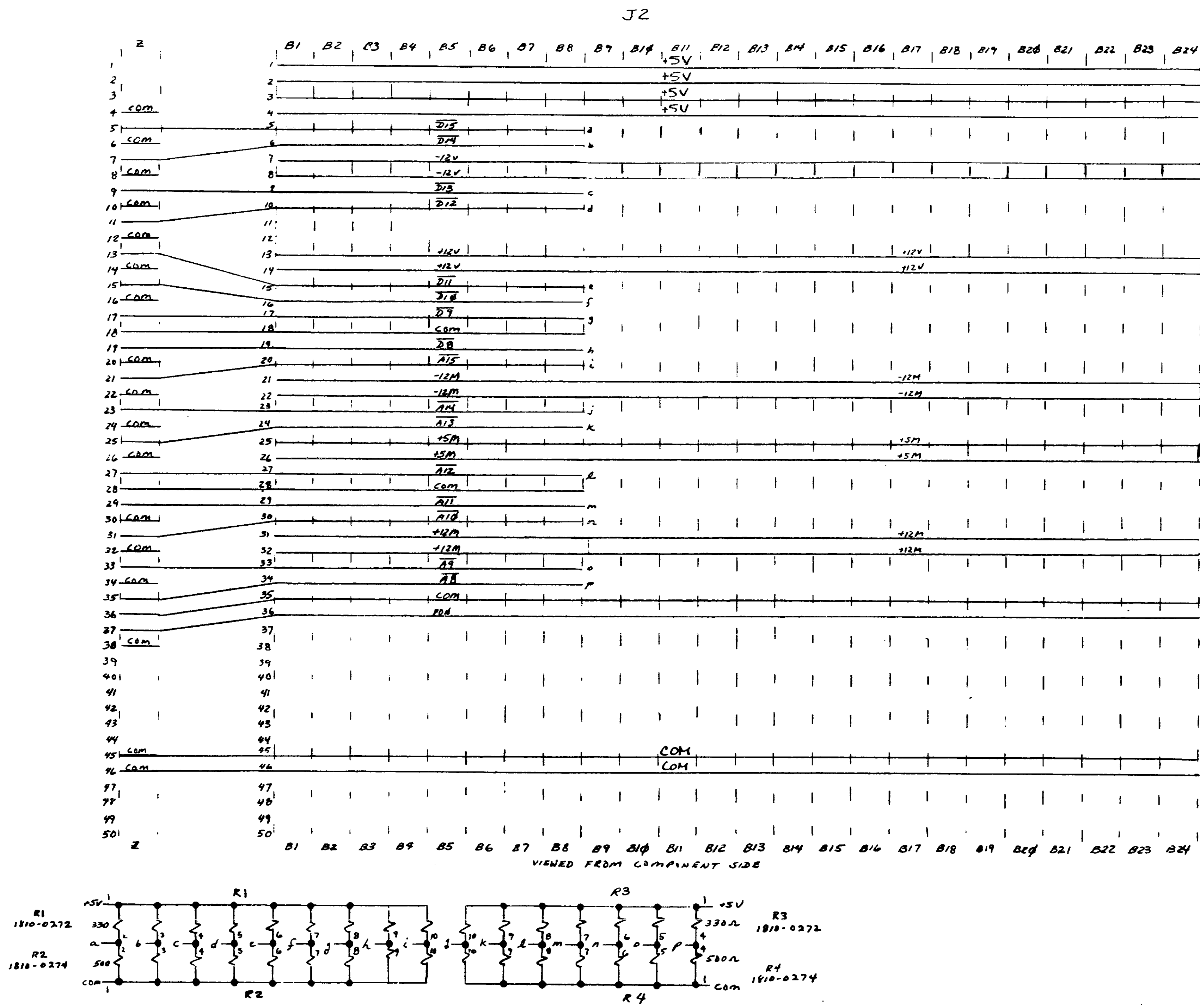
TITLE	BACK PLANE # 2 SCHEMATIC J1
NEXT ASSEMBLY	—
FINISH / SCALE	
PERM / DRINT	HEWLETT PACKARD
PART NUMBER	30070-60056
	C-30070-60056-51

SHEET 1 OF 1

ENGINEERING RESPONSIBILITY								SEPIA							
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	47											

C-30070-60056-52

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	5-9-78
B	REVISED PER DOC CHG.	JE	6-19-78



ALL Z location connector - 1251-4737

ALL other connectors - 1251-4573

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

PERM. PRINT

TITLE BACKPLANE #2 SCHEMATIC J2

HEWLETT PACKARD

NEXT ASSEMBLY —

PART NUMBER 30070-60056

FINISH | SCALE

C-30070-60056-52

SHEET 1 OF 1

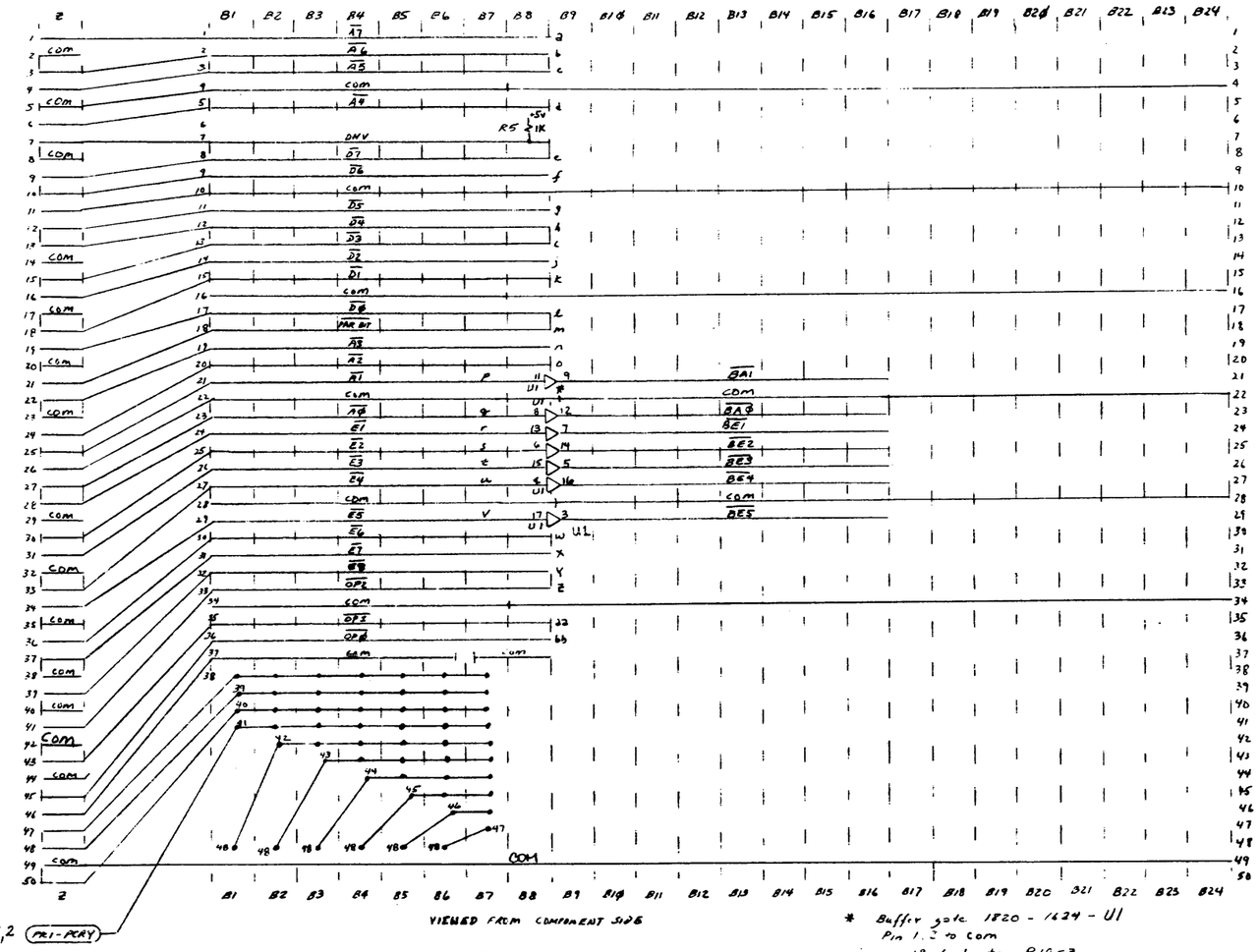
ENGINEERING RESPONSIBILITY														
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
46	48	61	63	97										

SEPIA

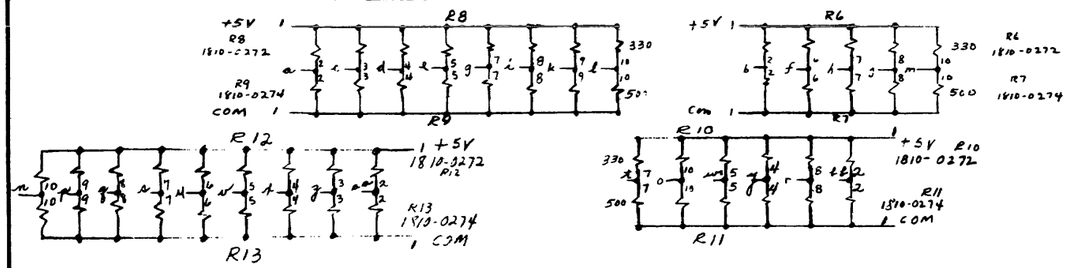
C-30070-60056-53

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	05/GE	5-9-78
B	REVISED PER ECR 1146	/GE	6-19-78

J3



* Buffer gate 1820 - 1624 - U1
Pin 1, 2 to com
pin 19 tied to R10-3



ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

PACKPLANE # 2 PERM PRINT
TITLE SCHEMATIC J3
HEWLETT PACKARD
NEXT ASSEMBLY —
PART NUMBER 30070-60056
FINISH SCALE
C-30070-60056-53

C-30070-60056-54

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	07	5-9-77
B	R15 WAS R19, R16 WAS R20		5-9-78
—	REVISED PER ECN [illegible]		6/19/79

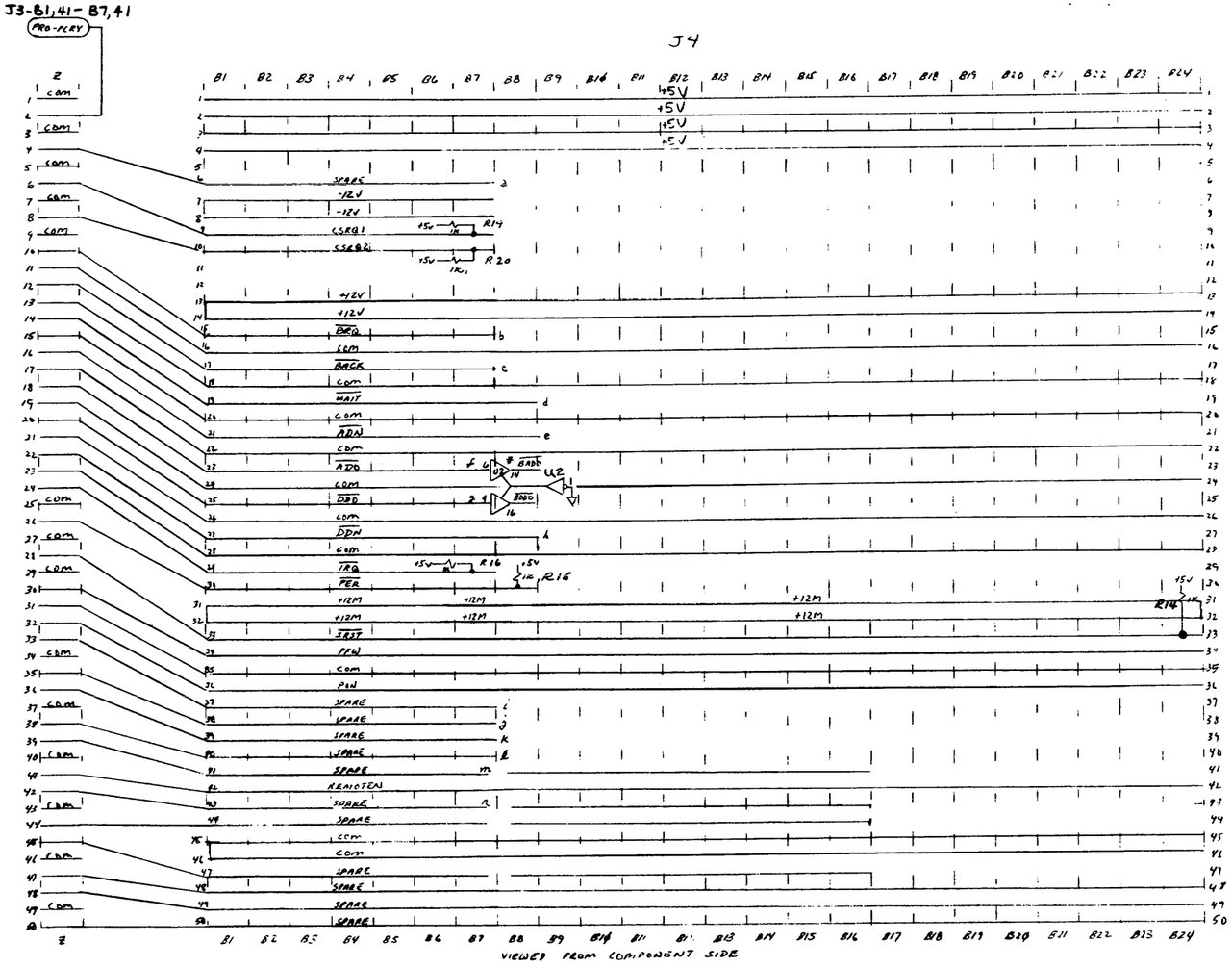
ENGINEERING RESPONSIBILITY / SEPIA

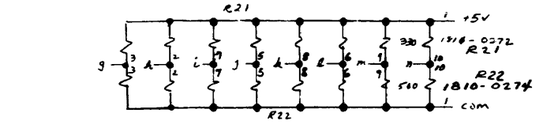
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	47										

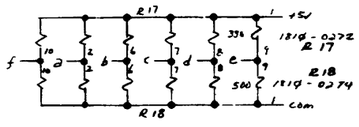
J3-B1,41-B7,41

PRO-PERY

J4







* BUFFER 1820-1624 145241
pin 19, 2, and 8 grounded

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

TITLE	BACKPLANE # 2 PERM SCHEMATIC J4
NEXT ASSEMBLY	—
FINISH	SCALE
PRINT	HEWLETT PACKARD
PART NUMBER	30070-60056
	C-30070-60056-54

SHEET 1 OF 1

STOCK NO 8280-0091 PRINTED ON DIEPO NO 4270 TO CLEARPRINT FADE-OUT

ENGINEERING RESPONSIBILITY | SEPIA

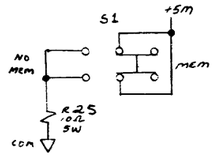
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	28	30	32	33	38	43
45	46	61	63	47										

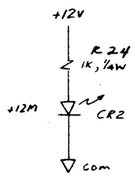
C-30070-60056-55

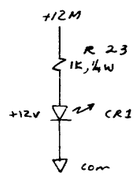
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	03/JE	5-9-78

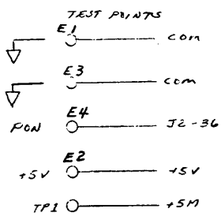
J6, J8, J9

PIN →	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
J6	+5V	+5V	+5V	-12V	+5S	PON	COM	COM	PON	+12V	-12S	+12V	COM	COM	COM
J8	+5V	+5V	+5V	+12V	+5M	+5M	COM	COM	COM	+12V	-12V	+12S	COM	COM	COM
J9	+5V	+5V	+5V	-12V	+5V	–	COM	COM	COM	+12V	-12M	+12M	COM	COM	COM









J5 and J7 not used

ITEM	QTY.	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC

PERM. PRINT

TITLE BACK PLANE #2 SCHEMATIC J5, J6, J7

HEWLETT PACKARD

NEXT ASSEMBLY

PART NUMBER 30070-60056

FINISH | SCALE

C-30070-60056-55

SHEET 1 OF 1

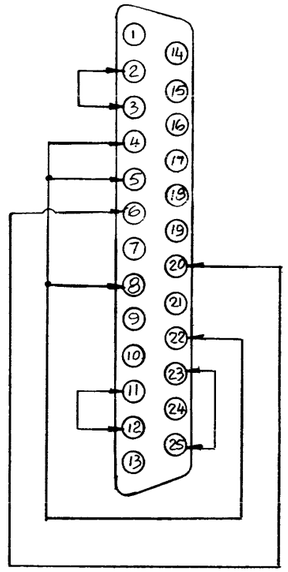
STOCK NO 9280 0003 PRINTED ON DIEPO NO 1020-10 CLEARPRINT FADEOUT

ENGINEERING RESPONSIBILITY ◪ SEPIA ◪

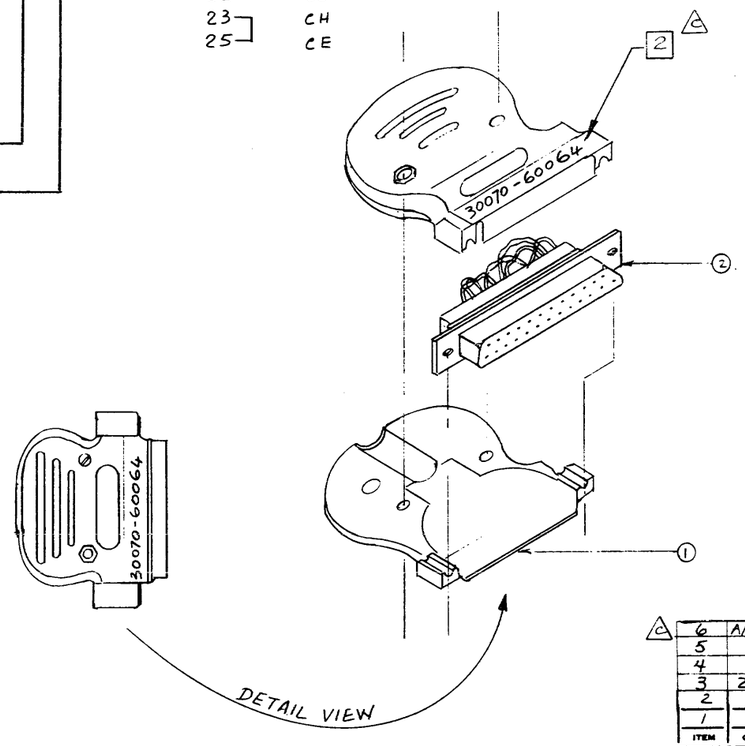
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	41										

C-30070-60064-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	CD	7/26/78
B	ADD ITEMS 3-6 + NOTE PER ECO #7-1429	CD	6/21/78
C	ADD. NOTE 2, ITEM 6 WAS 8150-2344 REVISED CONNECTOR PER DOC. CHG.	CD	7/25/78



PIN	SIGNAL NAME
2	BB
3	BA
4	CF
5	CF
6	CD
8	CA
11	SCF
12	SCA
20	CC
22	CB
23	CH
25	CE



NOTE:

1. ASSEMBLE CONNECTOR HOOD PER B-5951-7309-1
2. △C [2] STAMP 30070-60064 AS SHOWN.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO	MAT'L-DWG NO	MAT'L-SPEC
△C 6	A/R	WIRE BLK - 24 AWG	8150-0447		
5	2	SCREW 4-40 x .500	2220-0010		
4	2	NUT 4-40	2260-0001		
3	25	CONTACT CONN M	1251-3253		
2	1	CONN R-P M 25PIN	1251-2417		
1	2	HOOD - HALF CLAM SHELLS	1251-3320		

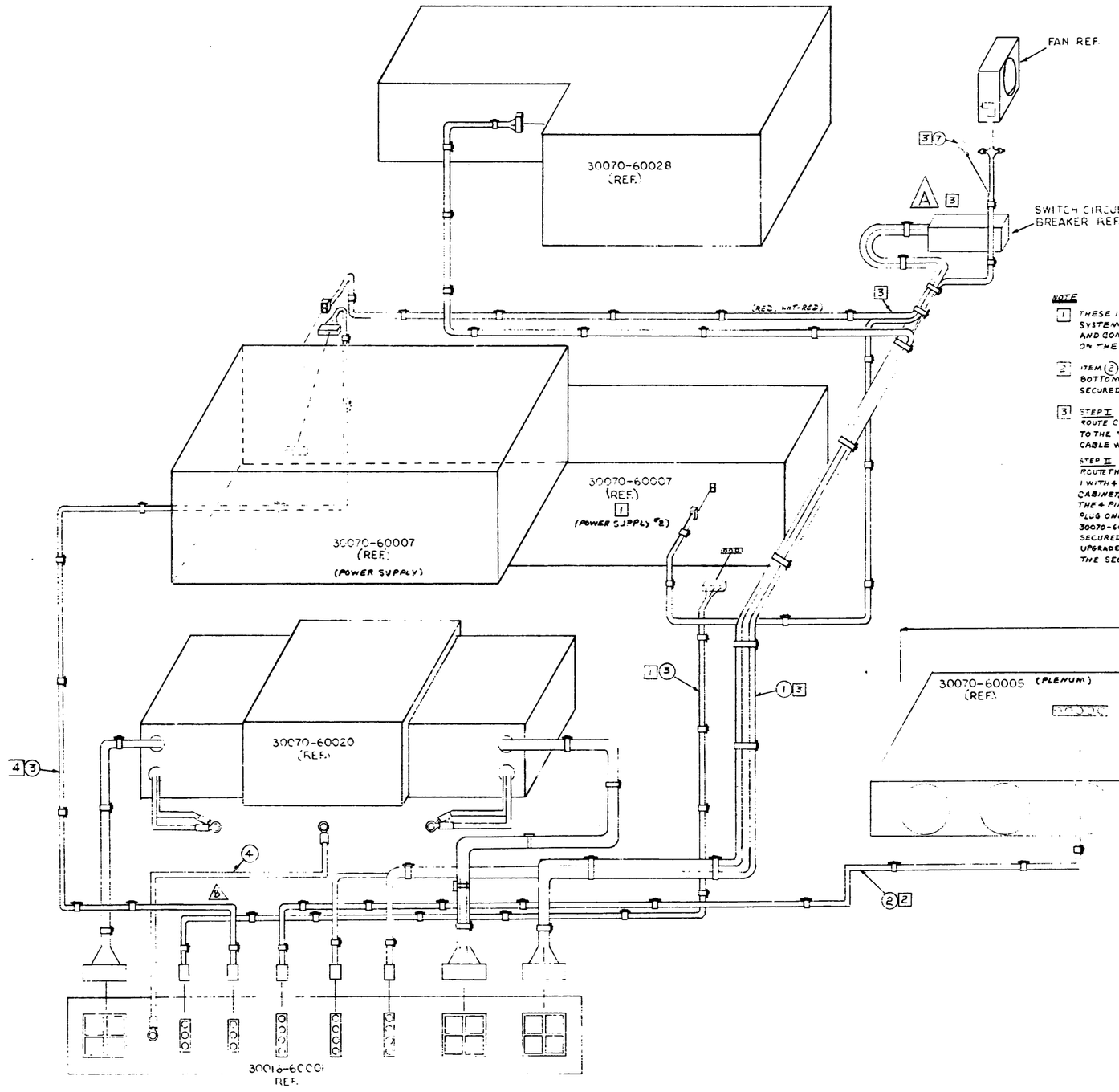
TITLE: LOOPBACK CONNECTOR PERM. PRINT	HEWLETT-PACKARD
NEXT ASSEMBLY: 30070-67001	PART NUMBER: C-30070-60064-1
FINISH	SCALE: —

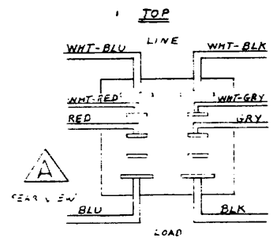
STOCK NO. 8120-0003 PRINTED ON DIEPO NO. 1030-10 CLEARPRINT FADEOUT

SHEET OF

SYM	REVISIONS	APPROVED	DATE
A	A3 ISSUED	DJ/SH	7/17/78
B	REVISED PER DRCR "22"	JC	4/14/81

30070-60065-B





NOTE

1. THESE ITEMS WILL BE INSTALLED ONLY WHEN SYSTEM IS UPGRADED TO 30416A, ALL CABLES AND COMPONENTS WILL BE CALLED OUT ON THE UPGRADE MATERIAL LIST.
2. ITEM (2) IS ROUTED ALONG THE BACK OF THE BOTTOM OF THE CARD CAGE CABINET AND IS SECURED IN PLACE BY THE SMALL "U" CLAMPS
3. STEP I
   ROUTE CABLE ITEM (1) UP SIDE OF CABINET TO THE MIDDLE THEN TO THE FRONT SECURE CABLE WITH 2 CABLE TIES ITEM (5)

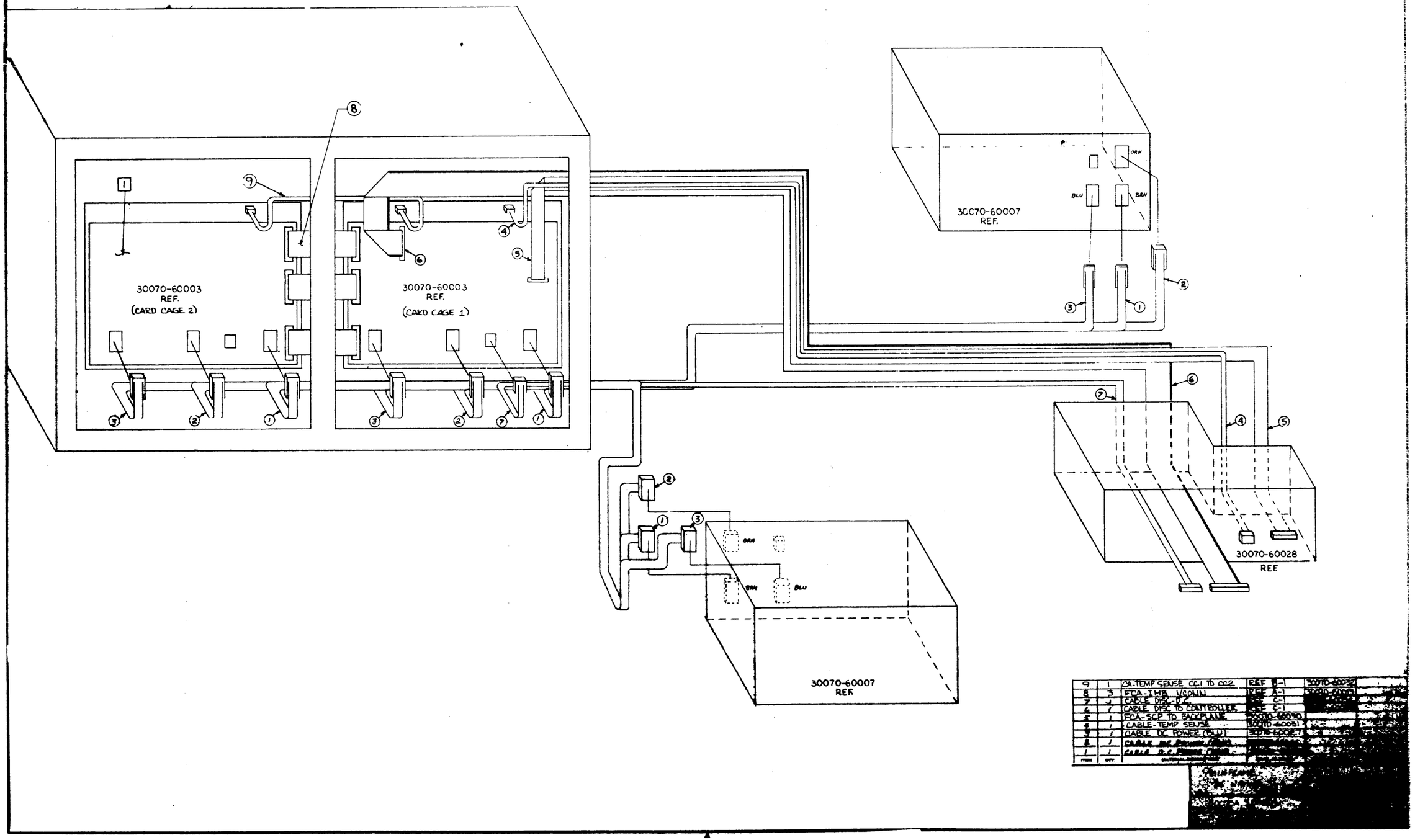
   STEP II
   ROUTE THE 3 BREAK OUTS, 2 WITH 2 PIN CONNECTORS 1 WITH 4 PIN CONNECTOR TO THE BOTTOM OF THE CABINET, SECURE WITH CABLE TIE, ITEM 5, PLUG THE 4 PIN CONNECTOR INTO THE 30070-60028. PLUG ONE OF THE 2 PIN CONNECTORS INTO THE TOP 30070-60007, THE REMAINDER IS COILED AND SECURED WITH CABLE TIE, ITEM (6) UNLESS IT IS AN UPGRADE TO A 30416A WHEN IT IS PLUGGED INTO THE SECOND 30070-60007

   STEP III
   THE BLU WIRES ARE INSERTED THROUGH THE CIRCUIT BREAKER COVER-THEN WIRED ACCORDING TO DIAGRAM "A"

   STEP IV
   THE FAN WIRES WITH CONNECTOR GO THROUGH THE GROMET AND ARE TIED IN 2 PLACES WITH ITEM (6) THE GREEN WIRE IS SECURED WITH ITEM (6) THE CONNECTOR IS SECURED TO THE FAN
4. ROUTE CABLE ITEM (3) DOWN LEFT SIDE OF CABINET SECURE WITH ITEM (1) (3) (5) (6) TO CENTER UPRIGHT.

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO.	MATL SPEC.
10	4	SCR PH 6-32 x .312	2360-0115	
9	4	WASHER FLT #6	3050-0227	
8	4	MT CABLE TIE	1400-0786	
7	1	NUT 6-32 x 250	2420-0561	
6	2	CABLE TIE	1400-0249	
5	3	CABLE TIE	1400-0433	
4	1	GND STRAP	30070-60061	
3	1	CA-PWR SUP AC	30070-60029	
2	1	CA-PWR TO PLENUM	30070-60051	
1	1	CA-AC PWR	30070-60019	

ELECTRONIC ASSEMBLY
FINAL PRINT
HEWLETT PACKARD
30070-60065-B
D 30070-60065



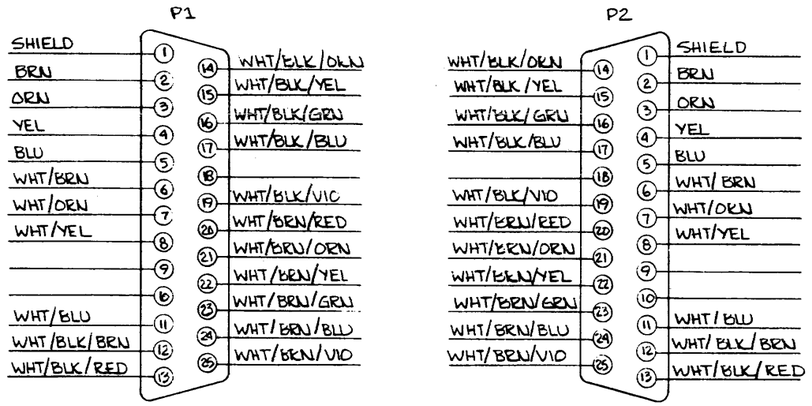
ITEM	QTY			
9	1	CA-TEMP SENSE CC1 TO CC2	REF B-1	30070-60028
8	3	FCA-IMB I/CONN	REF A-1	30070-60003
7	1	CABLE DISC-DC	REF C-1	
6	1	CABLE DISC TO CONTROLLER	REF C-1	
5	1	FCA-SCP TO BACKPLANE	30070-60020	
4	1	CABLE-TEMP SENSE	30070-60031	
3	1	CABLE DC POWER (BLU)	30070-60007	
2	1	CABLE DC POWER (ORN)		
1	1	CABLE DC POWER (BRN)		

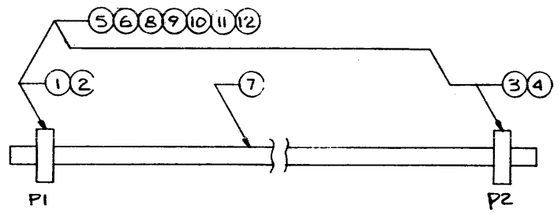
ENGINEERING RESPONSIBILITY														
0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22	23	25	29	30	32	33	38	43
45	46	61	63	41										

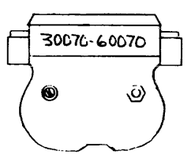
SEPIA

C-30070-60070-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	7/19/88







ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
14	4"	SHRINK TUBING	0890-0706		
13	4"	WIRE BLK-24 AWG	8150-0447		
12	4	LOCKWSHR	2190-0078		
11	4	SCR #4-40 x .687 P.H.	2200-0157		
10	4	NUT #4-40 x .250	2260-0001		
9	4	SCR FILISTER .500	2220-0010		
8	4	CLIP	1251-3328		
7	27"	CABLE, 21 CONN - 26AWG	8120-2777		
6	4"	SHRINK TUBING	0890-0291		
5	4	HOOD CLAMP .500	1251-3320		
4	22	PINS (F)	1251-3251		
3	1	CONN. BLOCK FEMALE	1251-2416		
2	22	PINS (M)	1251-3253		
1	1	CONN. BLOCK MALE	1251-2417		

TITLE	CABLE ASSY. - SCF PERM PRINT
NEXT ASSEMBLY	30070-60065
FINISH	—
SCALE	—
HEWLETT PACKARD	
PART NUMBER	30070-60070
	C-30070-60070-1
SHEET 1 OF 1	

HARDWARE ASSEMBLIES

SECTION V

5-1. INTRODUCTION

This section provides information to orient the reader to the HP 3000 series 33 hardware mainframe in order for him to better understand the system nomenclature.

5-2. HARDWARE NOMENCLATURE

The Cabinet sections of the Series 33 computer system derive their names from the respective hardware complement of the section. There are two basic names for the sections as follows:

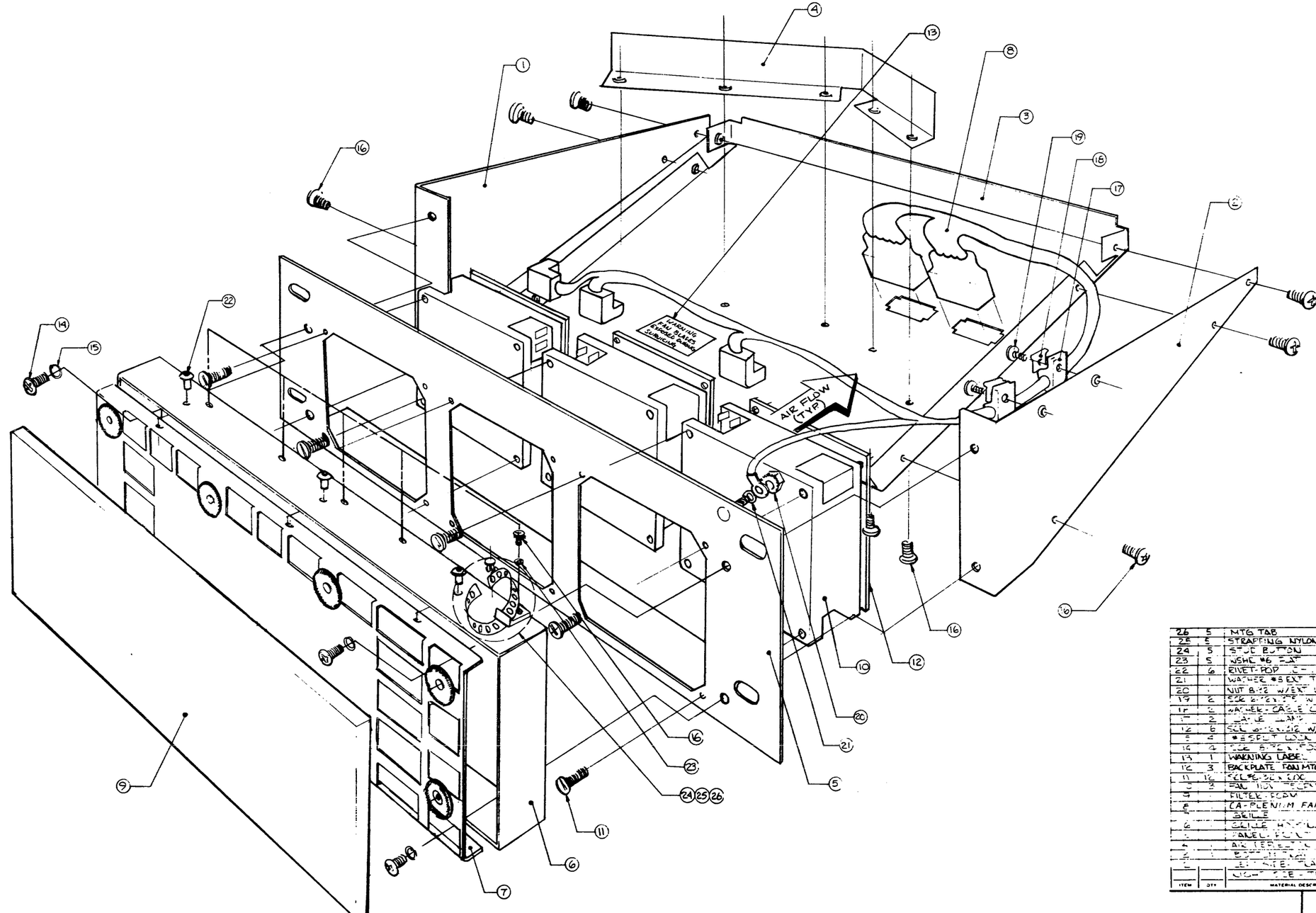
ELECTRONIC MAINFRAME

The Electronic Mainframe is devoted to the major DC and AC power components of the system, such as the Power Supply Unit, Isolation Transformer, and Power Control Module.

CARD CAGE MAINFRAME

The Card Cage Mainframe contains the inter-module Bus backplane which provides the housing for CPU, Memory, and I/O channels.

TABLE 5-1. HARDWARE ASSEMBLY INDEX



ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DWG NO	MATL SPEC
26	5	MTG TAB	[illegible]		
25	5	STRAPPING NYLON	[illegible]		
24	5	SNAP BUTTON	[illegible]		
23	5	WSHR #6 FLAT	[illegible]		
22	6	RIVET-POP [illegible]	[illegible]		
21	1	WASHER #8 EXT TOOTH	[illegible]		
20	1	NUT 8-32 W/EXT LOCK	[illegible]		
19	2	SCR [illegible]	[illegible]		
18	2	WASHER-CABLE CLAMP	[illegible]		
17	2	CABLE CLAMP	[illegible]		
16	6	SCR [illegible] W/EXT LOCK	[illegible]		
15	2	#8 SPLIT LOCK	[illegible]		
14	4	SCR 8-32 x .250	[illegible]		
13	1	WARNING LABEL	5040-7042		
12	3	BACKPLATE FAN MTG	5040-0012		
11	16	SCR #6-32 x [illegible]	[illegible]-1129		
10	3	FAN [illegible]	[illegible]-0327		
9	1	FILTER-FOAM	[illegible]		
8	1	CA-PLENUM FANS	[illegible]		
7	1	GRILLE	[illegible]		
6	1	GRILLE [illegible]	[illegible]		
5	1	PANEL [illegible]	[illegible]		
4	1	AIR [illegible]	[illegible]		
3	1	[illegible]	[illegible]		
2	1	[illegible]	[illegible]		
1	1	[illegible]	[illegible]		

ENGINEERING RESPONSIBILITY	SEPIA
0 1 2 3 4 6 8 9 11 12 14 16	
18 17 19 21 22 23 25 29 30 32 33 38 43	
45 46 51 53 57	

SYM	REVISIONS	APPROVED	DATE
A	AS 13503	[illegible]	7/11/78
B	ADD ITEMS 24,25,26 & 12 PER ECO [illegible]	[illegible]	8-11-78
C	ITEM 10 WAS 5180-0294 PER 47-1502	LF	12/5/78

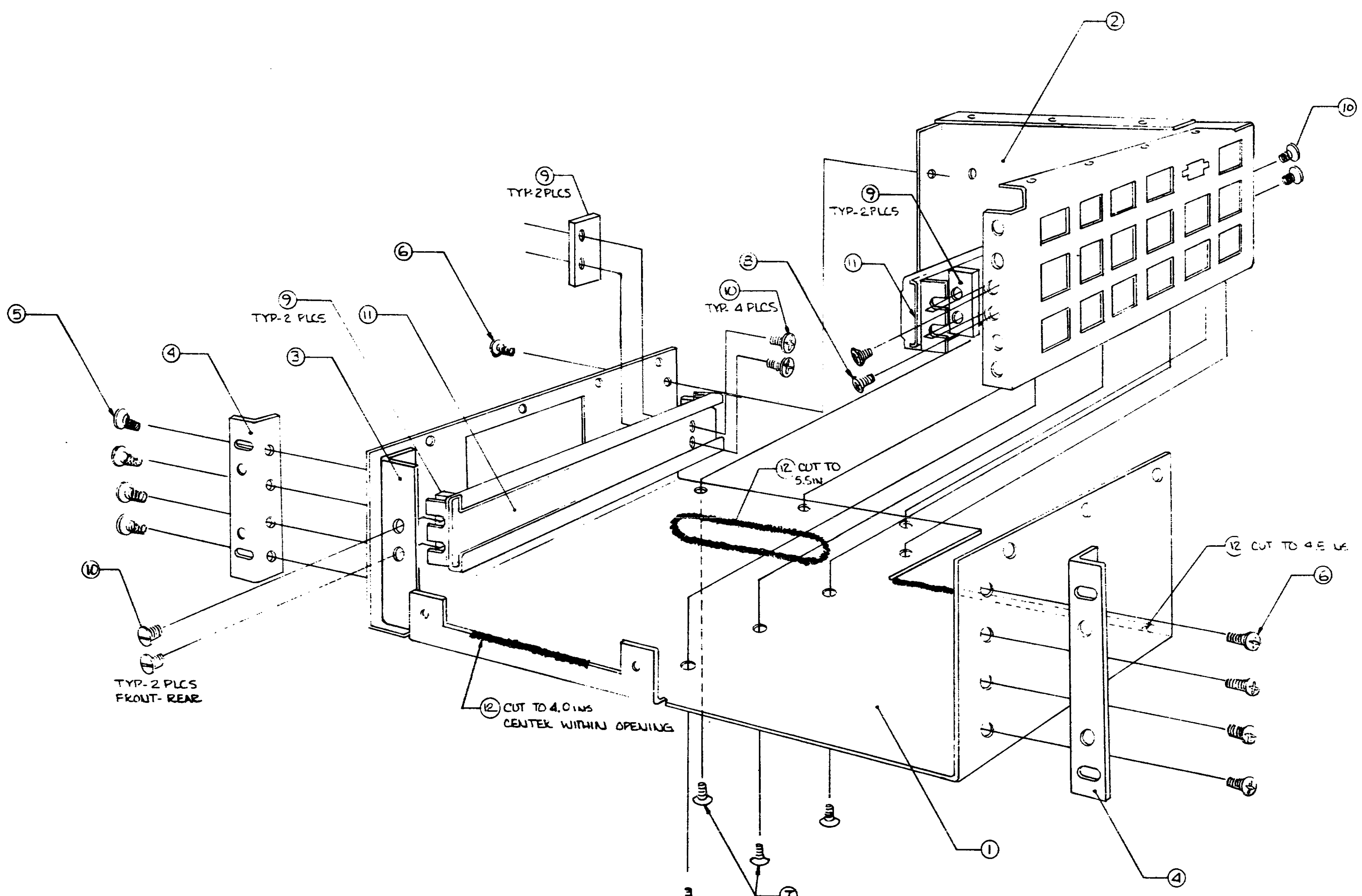
5180-6005-1

HEWLETT PACKARD

5-3

ENGINEERING RESPONSIBILITY		SEPIA	-30070-60028-1

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	[illegible]
B	ADD GROMMET CHAIN PRCR "55"	[illegible]	5-8-78

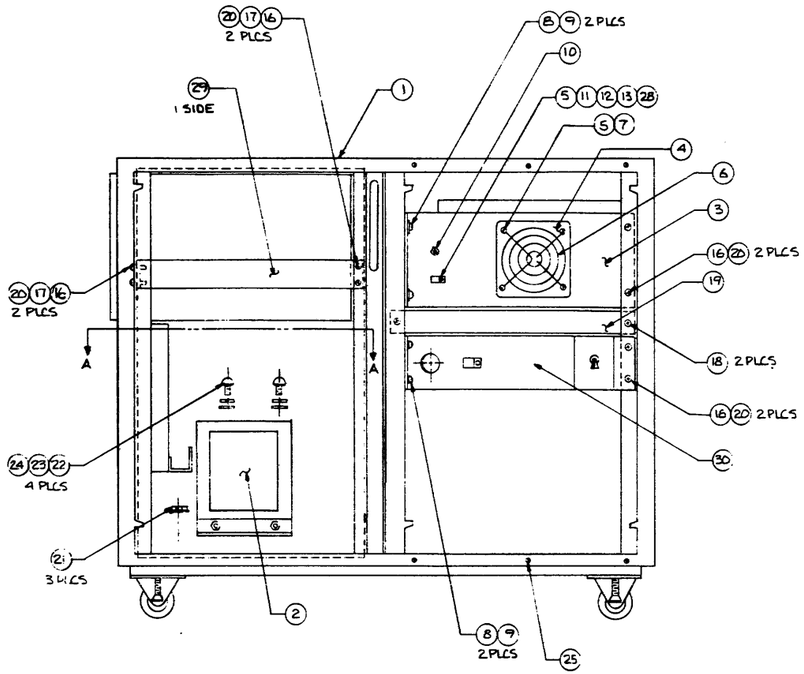


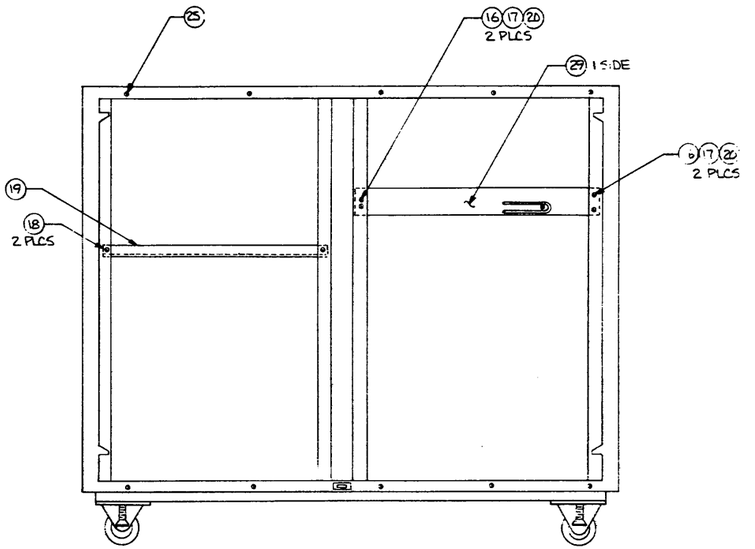
ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
12	IN	GROMMET CHAIN	[illegible]		
11	2	[illegible] OUTER SECTION	[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]		
9	[illegible]	NUT PLATE [illegible]	[illegible]		
8	2	[illegible]	[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]		
[illegible]	[illegible]	[illegible]	[illegible]		
[illegible]		[illegible] INTERNAL	[illegible]		
2	[illegible]	PANEL [illegible]/REAR	[illegible]		
1	1	[illegible]	[illegible]		

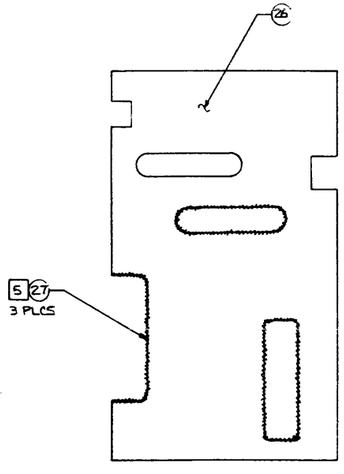
TITLE: ASSY– DISC/CONTROL PANEL	HEWLETT PACKARD
NEXT ASSEMBLY: [illegible]	PART NUMBER: [illegible]
FINISH	SCALE	D [illegible]

SHEET 1 OF 1

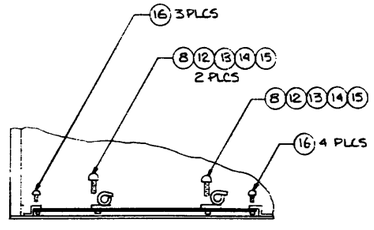
STOCK NO 9200-0014 PRINTED ON DIAPO NO 1026 10 CLEARPRINT FADEOUT







PANEL-PARTITION



SECTION A-A

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
30	1	ASSY-CIRCUIT BKR	REF	30070-60065	
29	1 PR	SLIDE-CHASSIS	[illegible] 0038		
28	1	SCR #6	[illegible] 0251		
27	3/FT	GROMMET-GASKET	[illegible] 0582		
26	1	PANEL-PARTITION	3177-0007		
25	6	BUTTON-GROUND	[illegible] 1037		
24	4	WSHR SPLK #4	[illegible] 0028		
23	4	WSHR FLAT #4	2190-0067		
22	4	SCR #4 x 62 x 62 NO MD	[illegible] 0697		
21	3	NUT HEX #10-32 SPAR WSHR	2740-0003		
20	12	WSHR FLAT #10	2190-0067		
19	2	RAIL SUPPORT	30070-00018		
18	4	SCR #10-32 x .500 PH	2200-0156		
17	8	WSHR #10 SPLIT	2190-0024		
16	15	SCR #10-32 x .375 PH	2200-0179		
15	8	WSHR #8 SPLIT	2190-0073		
14	3	WSHR #8	2190-0139		
13	4	CABLE TIE	1400-0493		
12	4	MOUNT-CABLE TIE	1400-0786		
11	1	SCR #6-32 x .375 PH	2200-0197		
10	1	NUT-HEX #6-32	2420-0001		
9	4	WSHR	3050-0001		
8	7	SCR #8-32 x .375 PH	2510-0103		
7	4	SCR #6-32 x 1.75 PH	2360-0137		
6	1	GRILLE-FAN	3160-0092		
5	5	WSHR	3050-0227		
4	1	FAN	3160-0327		
3	1	BRACKET-FAN	30070-00019		
2	1	ASSY-TRAYS	30070-60020		
1	1	ASSY-FRAME	30070-60071		

ITEM	QTY	REVISIONS	APPROVED	DATE
A		AS ISSUED	[illegible]	4-15-78
B		REVISED PER PCR 27	[illegible]	6-28-78
C		0360-1799 WAS 30070-20003 PCO 47-1449	[illegible]	7-24-78
D		ITEM 4 WAS 3160-0294 PCO 47-1502	[illegible]	10-27-78

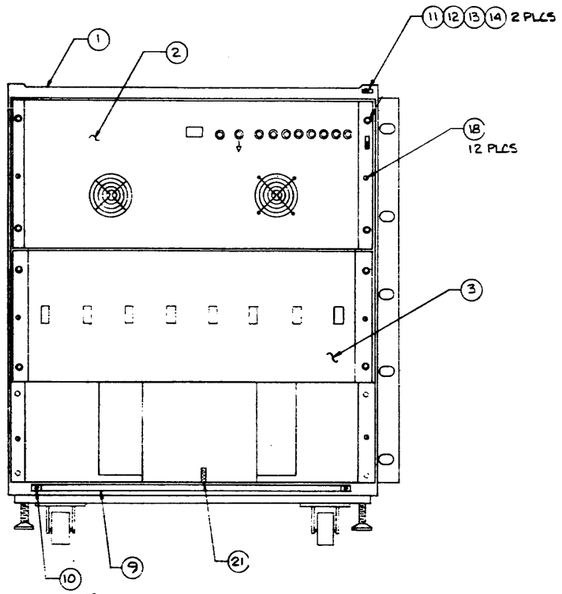
TITLE	SUB-ASSY MTG.
NEXT ASSEMBLY	30070A
FINISH	—
MATERIAL	—
HEWLETT-PACKARD	
PART NUMBER	D 30070-60065-2
SHEET 1 OF 1	

ENGINEERING RESPONSIBILITY																SEPA
0	1	2	3	4		18	20	9	11	12	14	16				
16	17		19		21	22	23	25	29	30	32	33	38	43		
45	46	61	63	67												

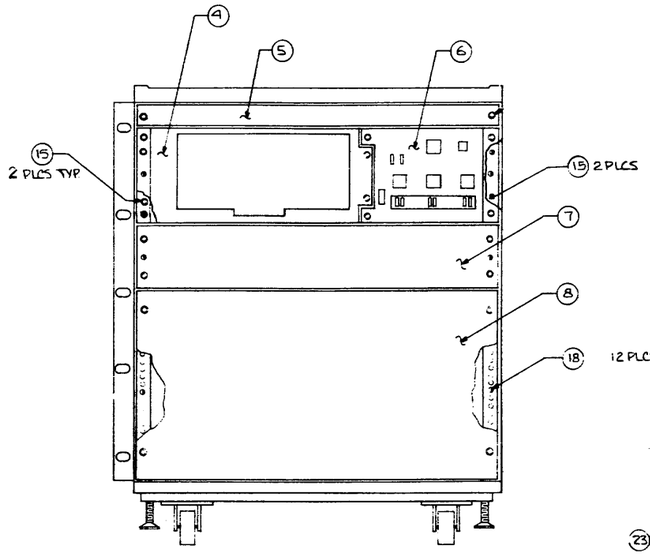
DASH	REVISIONS	APPROVED	DATE
A	AS ISSUED	BK	4-3-78
B	REVISED NOTE 3 PER PRICE "ZZ"	BK	4-28-78
C	ECO-1939 WAS 30070-30003 P.O. 47-1449	BK	7-24-78

8-30070-60065-3

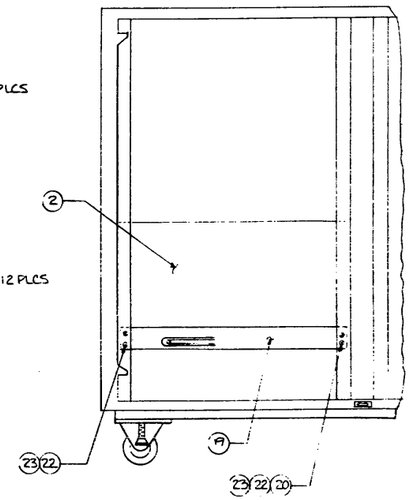
REAR VIEW

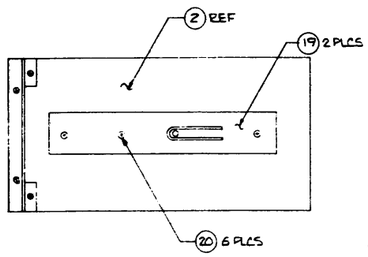


FRONT VIEW

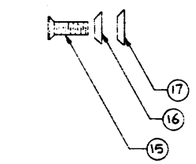


SIDE VIEW





POWER SUPPLY — SLIDE MOUNTING



MOUNTING HARDWARE — EXPLODED

ITEM	QTY	MATERIAL DESCRIPTION	MATL PART NO	MATL DRG NO	MATL SPEC
23	8	WSHR #10 FLAT	REF	3050-0079	
22	8	WSHR #10 SPLIT	REF	2190-0018	
21	1	GROUND LABEL	7120-7016		
20	6	SCR 10-32 X .375 PH	2680-0699		
19	PR	SLIDE-CHASSIS	REF	1494-0038	
18	24	GROUND BUTTON	0380-0930		
17	26	WSHR-FILLER	3050-0248		
16	20	WSHR-CUP	3050-0027		
15	30	SCR #10-32 FH .500	2680-0706		
14	12	WSHR #8	3050-0033		
13	2	SCR #8-32 X .250	2360-0119		
12	2	CABLE TIE	1400-0932		
11	2	MTG-CABLE TIE	1400-0796		
10	2	RIVET-POP 37.6 DIA x .125-.250	0361-0679		
9	1	PANEL-TRIM	30070-20002		
8	1	PANEL-BLANK 3.72 IN	12684-01002		
7	1	PANEL-BLANK 3.47 IN	12681-01002		
6	1	ASSY-SYS CONT PANEL	30070-60008		
5	1	PANEL-BLANK 1.72 IN	12680-01002		
4	1	ASSY-DISC CP ENCL	30070-60028		
3	1	ASSY-MPIB GUNG FNL	30070-60014		
2	1	ASSY-POWER SUPPLY	30070-60007		
1		ASSY-FLAME	REF	7101-0491	

SUB-ASSY MTG

30070A, 30416A

HEWLETT PACKARD

30070-[illegible]-3

D-30070-60065-3

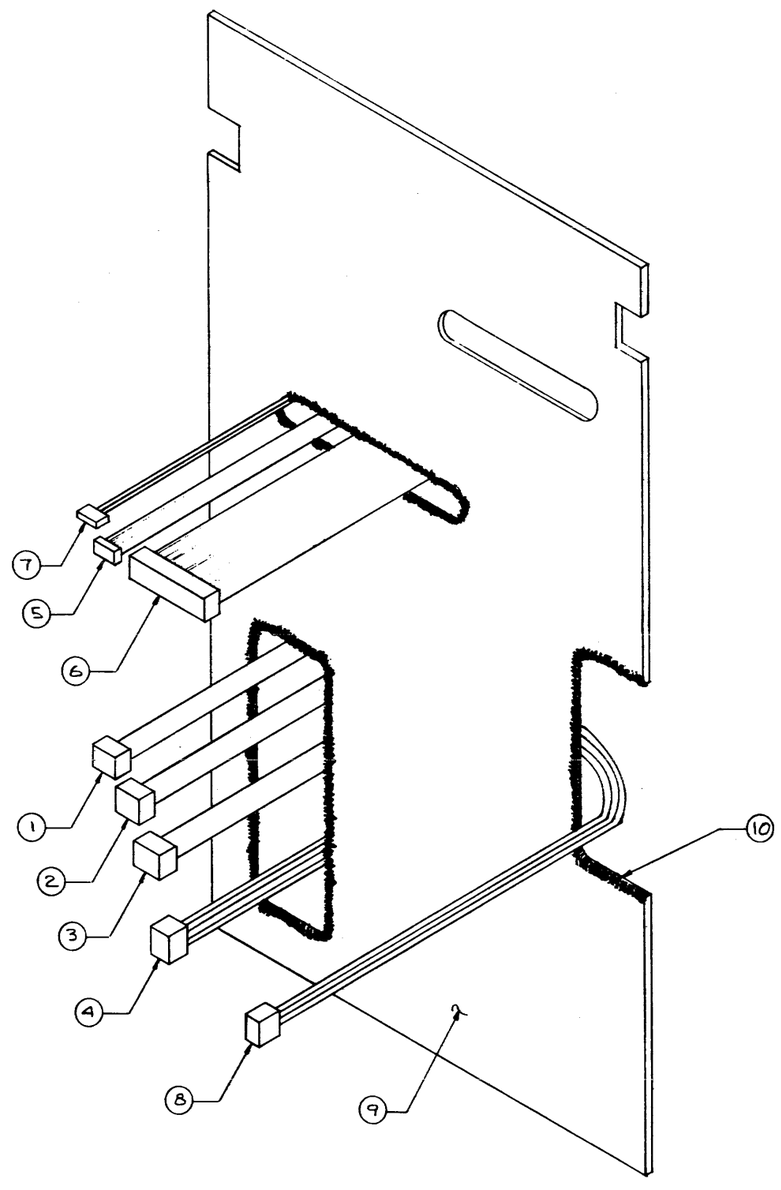
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	47											

SEPIA

C-30070-60065-4

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	LD	11/27/



NOTES:

1. DO NOT ROUTE ITEMS (5)(6) (SIGNAL CABLES) PARALLEL WITH POWER CABLES.

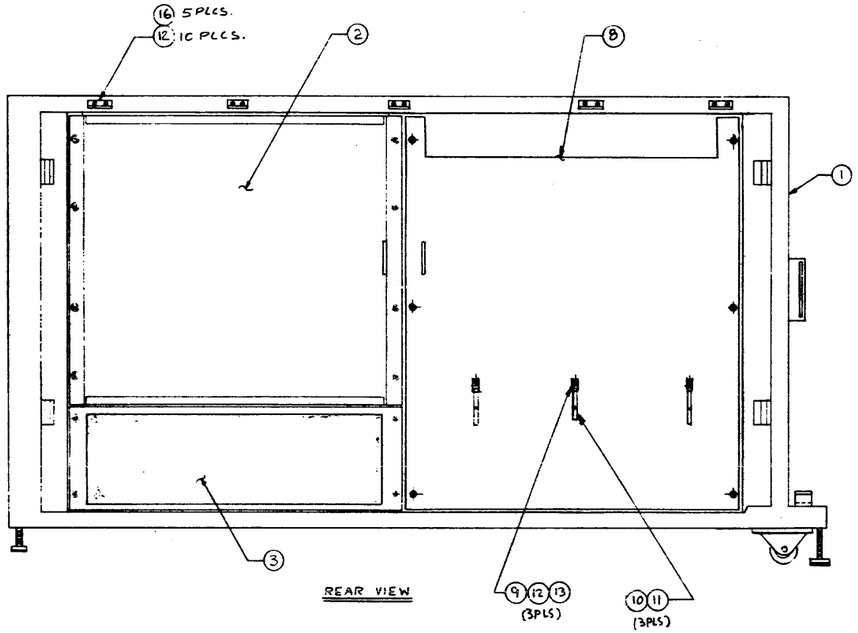
ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
10	A/R	GROMMET-GASKETING	REF	0400-0082	
9	1	PARTITION-PANEL	REF C-1	30070-60017	
8	1	CABLE PCM TO PLENUM	REF B-1	30070-60051	
7	1	CABLE-TEMP SENSE	REF B-1	30070-60031	
6	1	CABLE-DISC TO CONTROLLER	REF C-1	30070-60036	
5	1	PCA-SCP TO BACKPLANE	REF. B-1	30070-60030	
4	1	CABLE DISC-D.C. POWER	REF. C-1	30070-60034	
3	1	CABLE D.C. POWER (BLU)	REF B-1	30070-60027	
2	1	CABLE D.C. POWER (ORN)	REF B-1	30070-60026	
1	1	CABLE D.C. POWER (BRN)	REF B-1	30070-60025	

TITLE: PANEL-PARTITION-CABLE ROUTING	HEWLETT PACKARD
NEXT ASSEMBLY: 30070A	PART NUMBER: 30070-60065-4
FINISH: —— SCALE: ——	C-30070-60065-4

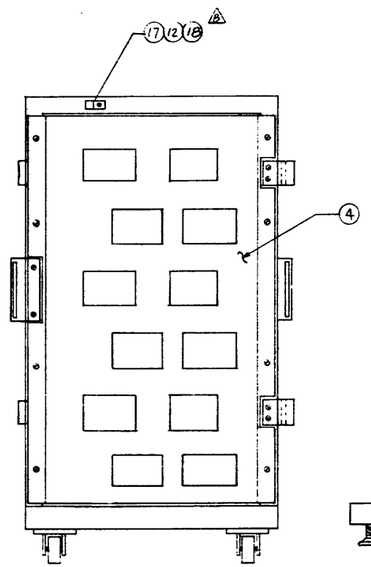
SHEET 1 OF 1

ENGINEERING RESPONSIBILITY	SIGMA
0 1 2 3 4 6 8 9 11 12 14 16	
16 17 18 21 22 23 26 29 30 32 33 38 43	
46 46 41 43 47	

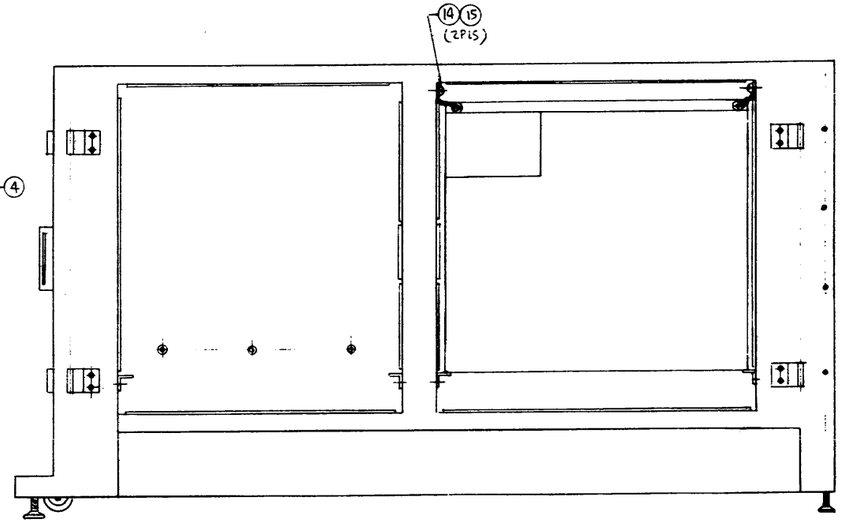
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	REQ-47-1024-ADD. ITEMS 7, 18; ITEM 12 QTY. WAS 3		5-24-78



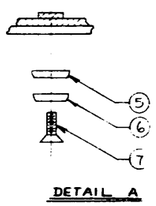
REAR VIEW



LEFT SIDE VIEW



FRONT VIEW



DETAIL A

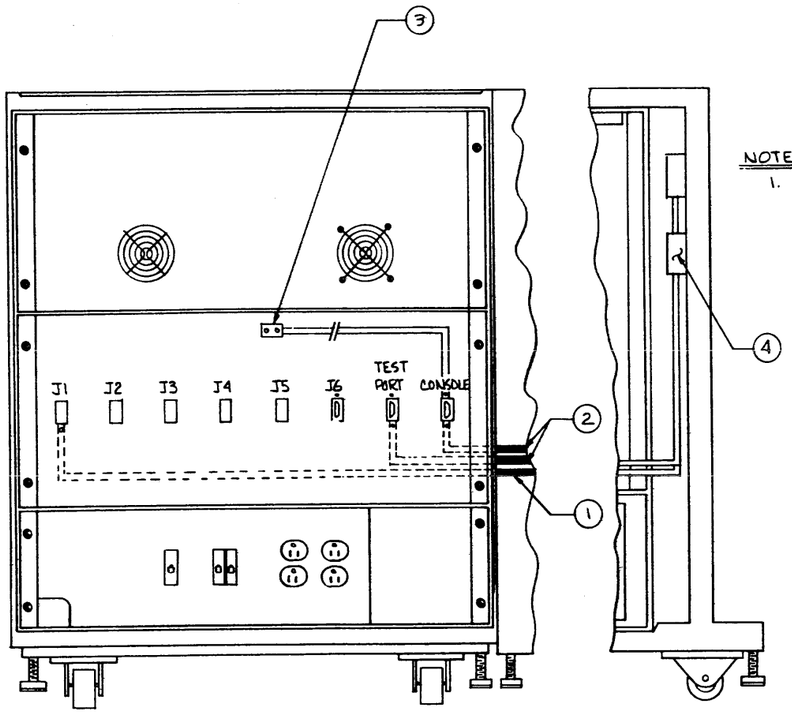
ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
18	1	CABLE TIE (REMOVABLE)	1400-3[illegible]		
17	1	CABLE TIE MOUNT	1400-3[illegible]		
16	5	CABLE CLAMP	[illegible]		
15	2	SCREW-#6-32x.375LG, PH	2510-3045		
14	2	GROUND STRP	30070-[illegible]		
13	3	WASHER-FLAT #6	3050-0227		
12	14	SCREW-#6-32x.375 LG, PH	2360-0117		
11	3	STUD BUTTON	1400-0943		
10	24 in.	STRAPPING-NYLON	1400-0944		
9	3	TAB-MOUNTING	1400-0945		
8	1	PANEL-BLANK, CC	30070-00008		
7	56	SCR FH #10x.50x.625	2683-0066		
6	26	WASHER-SQP	3050-0047		
5	56	WASHER-FILLER	3053-0348		
4	1	ASSY-TEEM FAN PNL	30070-60006		
3	1	ASSY-AIR PLENUM	30070-60005		
2	1	ASSY-CARD CAGE	30070-60002		
1	1	ASSY-FRAME, CC MTF	30070-60040		

TITLE	ASSY-[illegible] CARD CAGE [illegible] PLENUM
NEXT ASSEMBLY	30[illegible]
FINISH	—
QTY ALS	
HEWLETT PACKARD	
PART NUMBER	30070-60065
	D-30070-60065-B
	SHEET 1 OF 1

ENGINEERING RESPONSIBILITY															
0	1	2	3	4		6		8	9		11	12	14	15	
16	17		19		21	22	23	25	29	30	32	33	38	43	
45	46	61	63	47											

SEPIA

SYM	REVISIONS	APPROVED	DATE
A	RELEASED	[signature]	4-25-78
B	MOVED ITEM 1 TO J1 FROM J6 - PER PCO-47-1518	GD [signature]	11-3-78



REAR VIEW

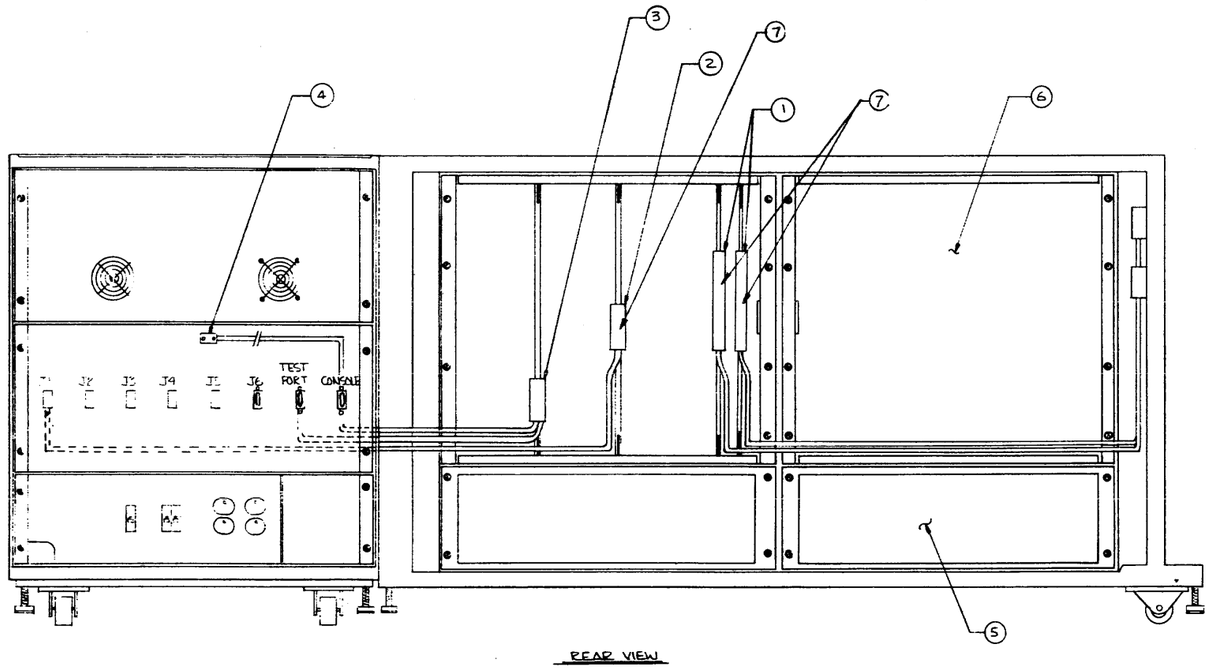
NOTES

1. ROUTE CABLES, ITEMS (1)(2), FROM CARD CAGE MAINFRAME TO ELEC. ENCLOSURE THRU PANEL PARTITION.

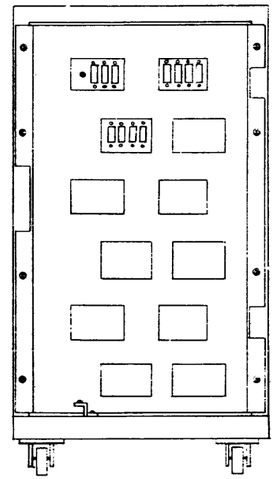
ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG NO.	MAT'L-SPEC.
4	2	CABLE - ADCC	5061-2502		
3	1	CABLE - HPIB (½ METER)	8120-2237		
2	1	CABLE - MI	5061-2504		
1	1	CABLE - GIC	5061-2503		

TITLE	ASSY - MI, GIC, ADCC, CABLES
NEXT ASSEMBLY	30070A
FINISH	—
SCALE	—
	HEWLETT PACKARD
PART NUMBER	30070-60065
	C-30070-60065-9

SHEET 1 OF 1



REAR VIEW



SIDE VIEW

NOTES:
1. ROUTE CABLES (2) (3) FROM CARD CAGE MAINFRAME TO ELECTRONIC ENCLOSURE THRU PARTITION.

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC	
7	3	LABEL STRIP, HOOD	7120-7854			
6	–	CARD CAGE 2, 1EA	REF D-1	30070-60057		
5	–	AIR PLENUM, 1EA	REF D-1	30070-60005		
4	–	CABLE - HPIB (½ METER) 1EA	REF D-1	8170-2237		
3	–	CABLE - MI, 1EA	REF D-1	5061-2504		
2	–	CABLE - GIC, 1EA	REF D-1	5061-2503		
1	–	CABLE - ADCC, 2EA	REF D-1	5061-2502		

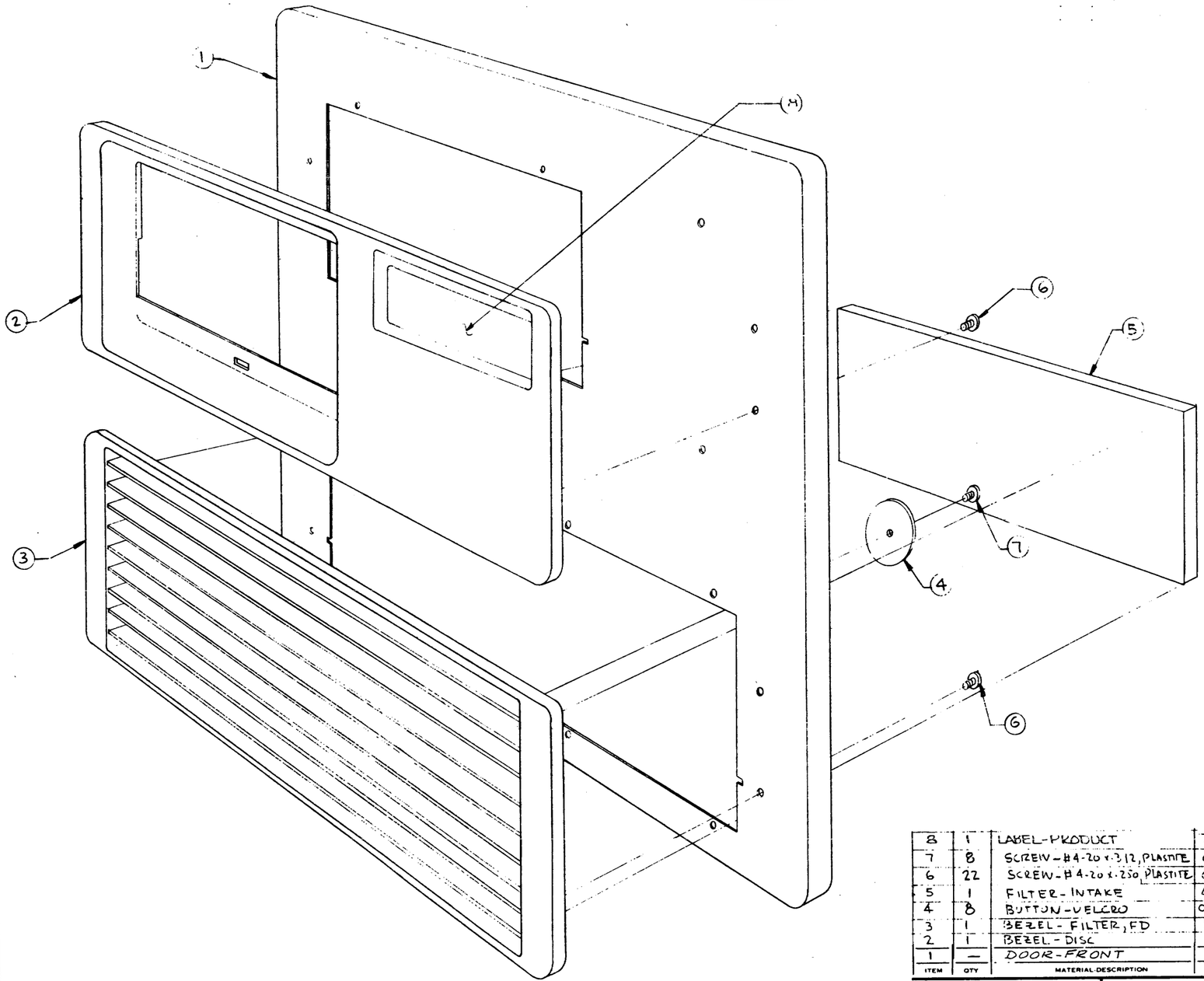
TITLE	CABLE ROUTING (MI GIC & ADCC)
NEXT ASSEMBLY	30070A, 30916A
FINISH	—
SCALE	—
HEWLETT PACKARD	
PART NUMBER	30070-90012-1
	D-30070-90012-1
SHEET 1 OF 1	

ENGINEERING RESPONSIBILITY ▰ SEPIA ▱

0	1	2	3	4		6		8	9		11	12	14	15
16	17		19		21	22		25	29	30	32	33	38	43
45	46	61	63	81										

C-30070-90012 2

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		3-1-78



ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
8	1	LABEL-PRODUCT	7120-7331		
7	8	SCREW-#4-20 x .312, PLASTITE	0624-0379		
6	22	SCREW-#4-20 x .250 PLASTITE	0624-0333		
5	1	FILTER-INTAKE	4208-0218		
4	8	BUTTON-VELCRO	0510-0589		
3	1	BEZEL-FILTER, FD	5040-9803		
2	1	BEZEL-DISC	5040-9802		
1	—	DOOR-FRONT	EFD-2	30070-90012	

TITLE: BEZEL INSTALATION-FRONT DOOR

HEWLETT PACKARD

NEXT ASSEMBLY: 30070A

PART NUMBER: 30070-90012 2

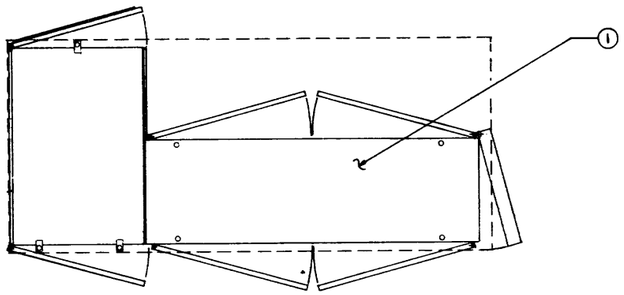
FINISH: — SCALE: —

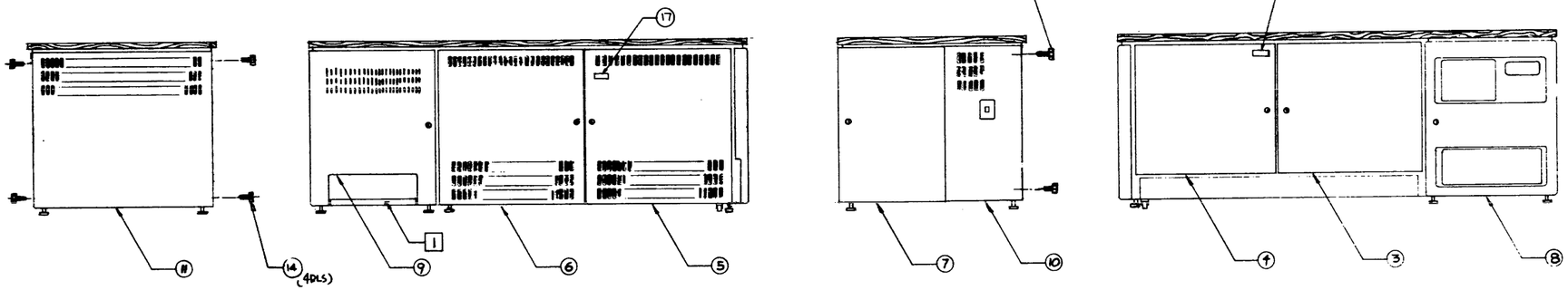
C-30070-90012-2

SHEET 1 OF 1

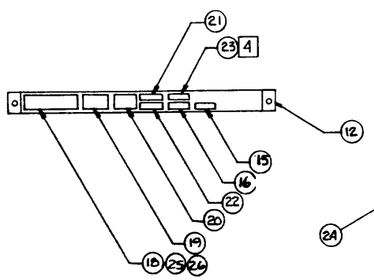
REVISIONS			
LTR		APPROVED	DATE
A	AS ISSUED	JS/DD	7/1/78
B	ADD 30070-60075, 30070-60076 PDD 47-1428		6-13-78
C	DEL 30070-60020 ADD 30070-60063 PER ECN 1247	LFJ	6-23-78
D	CHANGE WAS 30070-60071, 60072 TO 60075, 60076 PER ECN 1271	LFJ	8-28-78

1-30070-90012-3

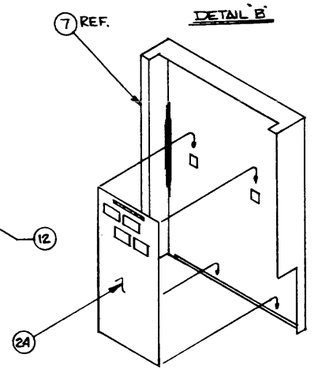




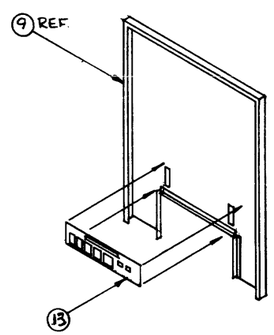
DETAIL A



DETAIL "B"



DETAIL "C"



NOTES:

1. SEE DETAIL "A" FOR LABEL PLACEMENT ON TRIM PANEL, (ITEM 12)
2. SEE DETAIL "B" FOR CHART PLACEMENT ON DOOR PANEL, (ITEM 7)
3. SEE DETAIL C. FOR CHART PLACEMENT ON DOOR PANEL, (ITEM 9)

ITEM	QTY	MATERIAL DESCRIPTION	MAT'L PART NO	MAT'L DWG NO	MAT'L SPEC
26	1	PLATE-ELECTRIC RATING	30070-00143		
25	1	PLATE-ELECTRIC RATING	30070-00142		
24	1	CHART IDENTIFICATION	30070-60075		
23	–	LABEL-VDE, IEA	REF [3]		
22	1	LABEL-CSA	7120-3428		
21	1	LABEL-UL	7120-6915		
20	1	LABEL-WARRANTY	7120-1135		
19	1	LABEL-INFO	7120-5524		
18	1	PLATE-ELECTRIC RATING	30070-00141		
17	2	LABEL-CAUTION	7120-3528		
16	–	LABEL-EI, IEA	REF [3]		
15	1	LABEL-NFPA TYPE II	7120-2568		
14	6	SCREW-#10-32 x .375 HEX W HD	2680-0244		
13	1	CHART IDENTIFICATION	30070-60076		
12	1	PANEL-TRIM	30070-60022		
11	1	ASSY-FULL PANEL	30070-00055		
10	1	ASSY-HALF PANEL	30070-00084		
9	1	ASSY-REAR DOOR	30070-00084		
8	1	ASSY-FRONT DOOR	30070-00083		
7	1	ASSY-SIDE DOOR	30070-00080		
6	1	ASSY-REAR DOOR (LH)	30070-00079		
5	1	ASSY-REAR DOOR (RH)	30070-00078		
4	1	ASSY-FRONT DOOR (LH)	30070-00077		
3	1	ASSY-FRONT DOOR (RH)	30070-00076		
2					
1	1	ASSY-MAINFRAME	30070-60065		

TITLE: MAINFRAME - FINAL ASSY

NEXT ASSEMBLY: 30070A

FINISH: —

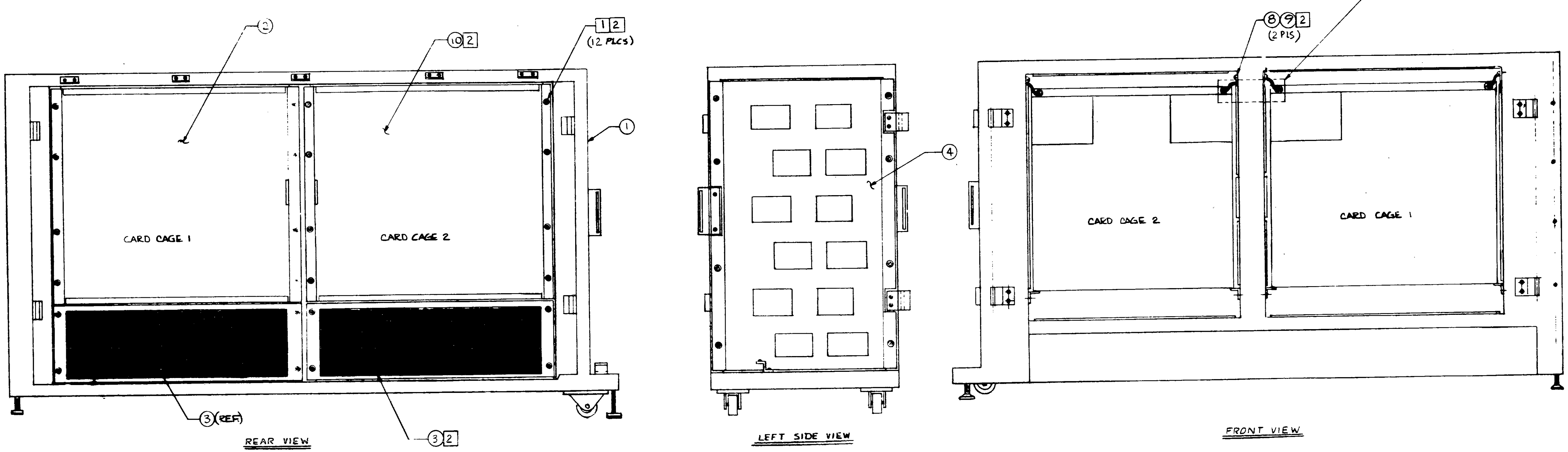
SCALE: —

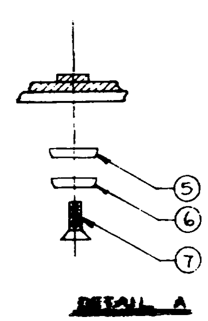
HEWLETT PACKARD

PART NUMBER: D-30070-90012-3

SHEET 1 OF 1

30070-90012 -4			
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	[illegible]	[illegible]





NOTES:

1. INSTALL ITEMS ⑤, ⑥ & ⑦ PER DETAIL A.
2. INSTALL ITEMS ONLY WHEN UPGRADING SYSTEM TO A 30416A.
3. INSTALL ITEM ⑪ USING EXISTING HARDWARE ON CARD CAGE 1.

ITEM	QTY	DESCRIPTION	PART NO.		
11	1	STRAP, GROUND	30070-00067		
10	1	ASSY CARD CAGE 2	30070-60057		
9	2	SCR 8-32 x .375 LG, PH	2510-0045		
8	2	GROUND STRP	30070-60060		
7	12	SCR F.H. [illegible] x .50 x 100°	[illegible]		
6	12	WASHER-CUP	[illegible]		
5	12	WASHER-FILLER	[illegible]		
4	-	ASSY-TERM IN PNL 1EA	REF D-1	[illegible]	
3	1	ASSY-A/C PLENUM	[illegible]		
2	-	ASSY-CARD CAGE 1 1EA	REF D-1	30070-60003	
1	-	ASSY-FRAME CCM/F 1EA	REF D-1	30070-600[illegible]	

ASSY SECOND CARD CAGE, PLENUM	
30416A	30070-90012
	30070-90012