

MAINTENANCE MANUAL

30115A

NINE-TRACK (NRZI-PE) MAGNETIC TAPE SUBSYSTEM

(FOR HP 3000 COMPUTER SYSTEMS)

Manual Part No. 30115-90001

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Printed-Circuit Assemblies:

30215-60002

30215-60006

Note

All references in this manual to part number 30215-60001 mag tape controller PCA are valid for application of part number 30215-60006 mag tape controller PCA.

Options Covered

This manual covers the basic subsystem and subsystem options -100, -200, -300, and -400.

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This manual provides subsystem-level coverage for the HP 30115A Nine-Trace (NRZI-PE) Magnetic Tape Subsystem, a part of the HP 3000 Computer System mass storage I/O facilities. The manual is effective for the overall basic subsystem and subsystem options -100, -200, -300, and -400.

This manual is intended for use by Hewlett-Packard Customer Engineers trained on the HP 3000 Series II or pre-Series II Computer Systems.

Contents of the manual include:

- a. A physical description of equipment and a subsystem parameter listing (Section I).
- b. HP 3000 Computer System control parameters for the magnetic tape subsystem (Section II).
- c. Subsystem theory of operation (Section III).
- d. Subsystem servicing and troubleshooting information (Section IV).

Refer to the following HP 3000 Series II or pre-Series II Computer System documentation for information on related hardware and software. The related documentation common to all HP 3000 Computer Systems includes the following:

- a. HP 7970B Digital Magnetic Tape Unit Operating and Service Manual, part no. 07970-90383.
- b. HP 7970E Digital Magnetic Tape Unit Operating and Service Manual, part no. 07970-90765.
- c. HP 13194A Multiunit Cable Accessory Kit Installation Manual, part no. 13194-90003.

The related documentation for the HP 3000 Series II Computer System includes the following:

- a. HP 3000 Series II Computer System Service Manual, part no. 30000-90018.
- b. HP 3000 Series II Computer System Signal and Power Distribution Manual, part no. 30000-90021.
- c. Stand-Alone HP 30115A Nine-Track Magnetic Tape Subsystem Diagnostic Manual, part no. 30115-90014.
- d. System Support Log, part no. 03000-90117.
- e. HP 3000 Series II Computer System Installation Manual, part no. 30000-90019.

The related documentation for the pre-Series II HP 3000 Computer System includes the following:

- a. HP 30035A Multiplexer Channel Maintenance Manual, part no. 30035-90001.
- b. HP 30001A Central Processor Unit/Input-Output Processor Maintenance Manual, part no. 30001-90003.
- c. HP 30005A/30006A Memory Subsystem Maintenance Manual, part no. 30005-90001.
- d. HP 30390A Cabinet Installation and Maintenance Manual, part no. 30390-90001.
- e. HP 30350A Auxiliary Control Panel and HP 30352A Hardware Maintenance Panel Operator's Manual, part no. 30352-90001.
- f. HP 3000 Manual of On-Line Diagnostics, On-Line HP 30115A Magnetic Tape Test, part no. 30115-90003.
- g. Systems Support Log, part no. 03000-90117.
- h. HP 3000 Computer System Installation Manual, part no. 03000-90032.
- i. Detailed Diagrams Manual, set numbers DD607 and DD608, Manual part no. 03000-90021.
- j. Illustrated Parts Breakdown Manual, part no. 03000-90021.

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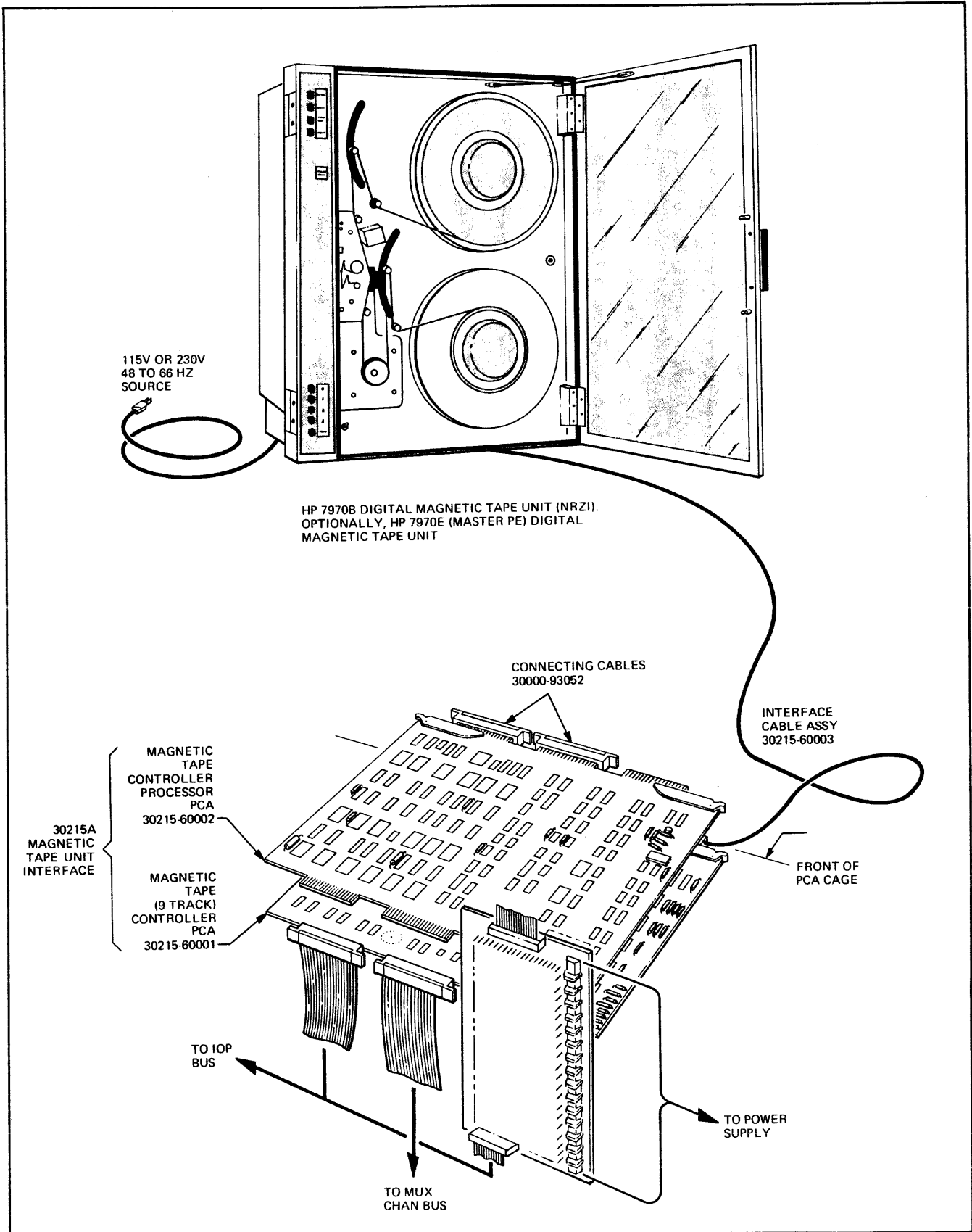
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Figure 1-1. HP 30115A Nine-Track (NRZI-PE) Magnetic Tape Subsystem Using a Single Tape Unit

1-1. INTRODUCTION.

1-2. This section describes important functional and physical features of the HP 30115A Nine-Track (NRZI-PE) Magnetic Tape Subsystem. Information on equipment components and options is included. Specifications and equipment identification data are also provided.

1-3. GENERAL DESCRIPTION.

1-4. The magnetic tape subsystem provides mass storage backup facilities to record and play back HP 3000 Computer System code and data segments to and from nine-track digital magnetic tape. An additional function of the magnetic tape subsystem is to provide the capability to cold-load the HP 3000 Computer System from magnetic tape. The non-return-to-zero-invert (NRZI) technique is used for subsystems utilizing HP 7970B Digital Magnetic Tape Units. The phase-encoded (PE) recording technique is used for subsystems using HP 7970E Digital Magnetic Tape Units. The HP 7970E Digital Magnetic Tape units are also capable of using a master-slave configuration. The above mentioned subsystems may be configured using a mix of these units. Certain constraints are imposed on configurations as outlined later in this section and in the maintenance section. Maximum data transfer rate is 36,000 bytes-per-second (18,000 words-per-second) when using NRZI tape units. The data transfer rate with phase-encoded recording units on-line is 72,000 bytes-per-second (36,000 words-per-second). Tape, reels, and recording format are in accordance with USA Standard (USAS) X3.22-1967, Recording Magnetic Tape for Information Interchange (800 cpi, NRZI) with NRZI recording. Phase-encoded recording is ANSI and industry compatible. Recording format and commands for the magnetic tape subsystem are discussed in Section II.

1-5. BASIC SUBSYSTEM.

1-6. Equipment for the basic HP 30115A Nine-Track (NRZI-PE) Magnetic Tape Subsystem, shown in figure 1-1, consists of:

- a. HP 7970B Digital Magnetic Tape Unit (NRZI), hereafter referred to as the tape unit.
- b. HP 30215A Magnetic Tape Unit Interface, hereafter referred to as the interface.
- c. This subsystem manual.

1-7. Each of the items listed above for the basic magnetic tape subsystem is comprised of a number of parts as outlined below.

a. The HP 7970B Digital Magnetic Tape Unit (NRZI) consists of the tape unit proper and:

- (1) Tape unit power cable assembly, approximately 8 feet (2.4 meters), part no. 8120-1395.

- (2) Tape reel (empty), 10-1/2 inches (267 mm) diameter, part no. 1490-0738.
 - (3) Tape reel (with approximately 2400 feet (731 meters blank tape), 10-1/2 inches (267 mm) diameter, part no. 9162-0025.
 - (4) Tape unit extender printed-circuit assembly (PCA) part no. 07970-60420 (not shown in figure 1-1).
 - (5) Head cleaner (not shown in figure 1-1).
 - (6) Mounting accessories (not shown in figure 1-1).
 - (7) *HP 7970B Digital Magnetic Tape Unit Operating and Service Manual*, part no. 07970-90383 (applicable for the HP 7970B).
- b. The HP 30215A Magnetic Tape Unit Interface consists of:
- (1) Magnetic tape (nine-track) controller printed-circuit assembly (PCA), part no. 30215-60001, hereafter referred to as the tape controller PCA.
 - (2) Magnetic tape controller processor printed-circuit assembly (PCA), part no. 30215-60002, hereafter referred to as the controller processor PCA.
 - (3) Connecting cable assembly, 1-1/2 inches (38 mm), part no. 30000-93052 (two required).
 - (4) Interface cable assembly, approximately 20 feet (6 meters), part no. 30215-60003.
- c. The magnetic tape subsystem manual data (not shown in figure 1-1) includes this maintenance manual, part no. 30115-90001, and Detailed Diagram sets, DD607, part no. 30215-90001, and DD608, part no. 30215-90003, for the *HP 3000 Computer System Detailed Diagrams Manual*, part no. 03000-90023.

1-8. SUBSYSTEM OPTIONS.

1-9. There are four option classifications to the basic magnetic tape subsystem. Note that the basic magnetic tape subsystem includes a single nine-track NRZI tape unit. Subsystem option—100 is effective if a single nine-track PE tape unit is installed instead of the NRZI unit. Option—100 consists of the HP 7970E Digital Magnetic Tape Unit (PE) Master proper and the following items:

- a. Tape unit power cable assembly, approximately 8 feet (2.4 meters), part no. 8120-1395.
- b. Tape reel (empty), 10-1/2 inches (267 mm) diameter, part no. 1490-0738.

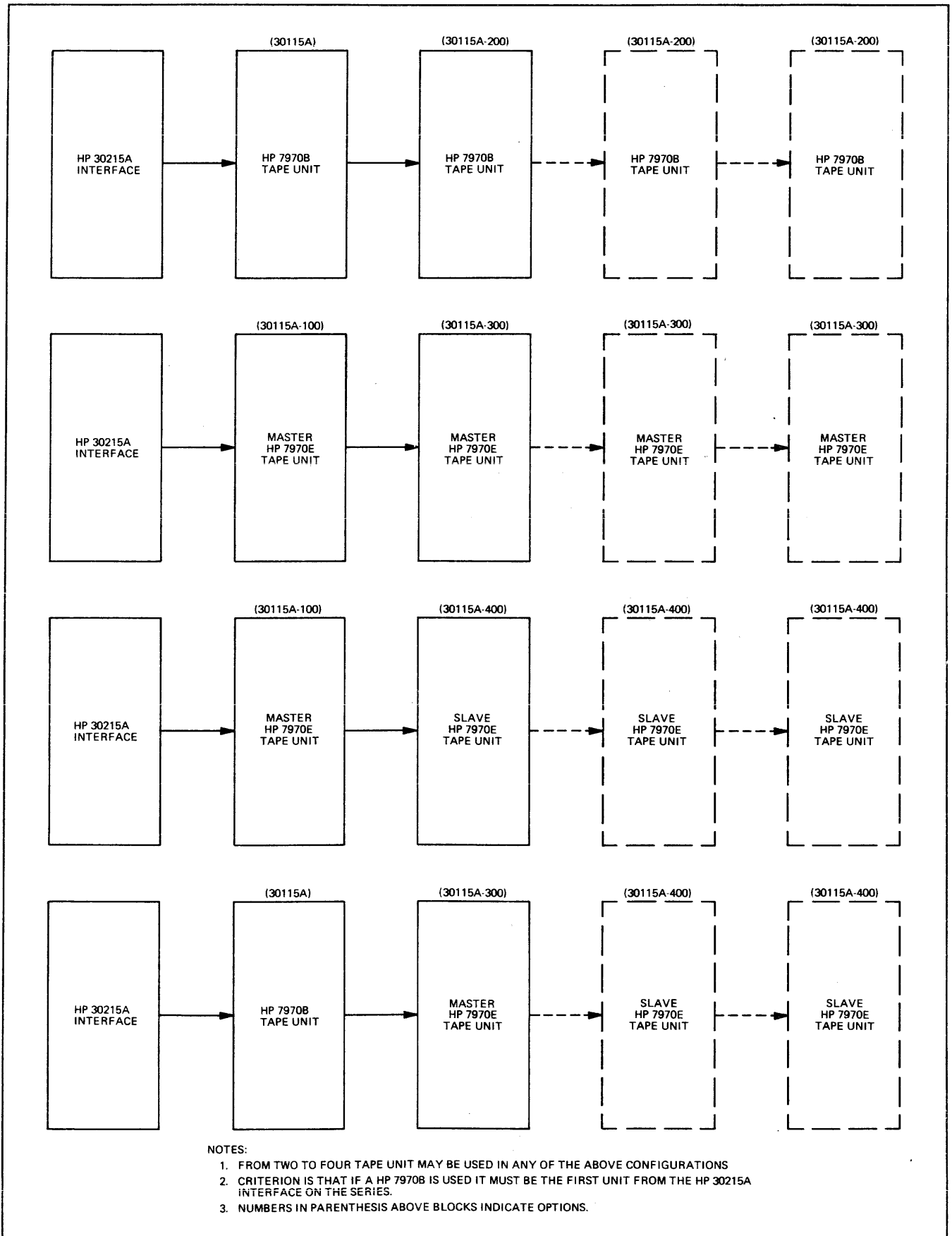
- c. Tape reel (with approximately 2400 feet (731 meters) blank tape), 10-1/2 inches (267 mm) diameter, part no. 9162-0025.
- d. Tape unit extender PCA, part no. 07970-60420.
- e. Head cleaner.
- f. Mounting accessories.
- g. *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual*, part no. 07970-90765 (applicable for the HP 7970E).

1-10. The HP 30115A Nine-Track (NRZI-PE) Magnetic Tape Subsystem may also be operated from a 230-Vac source. The computer system power control module (PCM) will distribute 230-volt, single-phase power to plug mold strips within the HP 30390A Cabinet in this case. The HP 7970B or HP 7970E Digital Magnetic Tape Units plug into the plug mold carrying 230 volts *after* the slide switch on the respective tape unit power module is moved to the 230-Vac position. (These steps are taken when the system is configured, and this data is included here for additional servicing information.) Power distributed to the HP 30215A Magnetic Tape Unit Interface PCA's from the HP 30310A Power Supply Modules remains unchanged. Instructions for 230-volt operation of the HP 30310A Power Supply Modules are contained in the *HP 30310A Power Supply Module Maintenance Manual*, part no. 30310-90003.

1-11. ADDITIONAL TAPE UNITS. Provisions for additional tape units (up to four units can be driven from the same interface) are included under options -200, -300, and -400. The options are described below. Appropriate tape unit operating and service manuals are included as options are adopted. Note that the tape controller PCA may drive a mix of HP 7970E and HP 7970B Digital Magnetic Tape Units on a sequenced basis. The phase-encoded tape units can be master and slave configurations provided that the slave units are driven by a master unit. Some representative connections are shown in figure 1-2. A total of 24 different option configurations are possible as explained in section IV. The HP 13194A or HP 13194A-001 Multiunit Cable is required when additional units are connected with options as outlined below. Note that the HP 13194A-001 Multiunit Cable is used only from a Master HP 7970E Digital Magnetic Tape Unit to a Slave HP 7970E Digital Magnetic Tape Unit.

- a. Option -200 adds one HP 7970B Digital Magnetic Tape Unit (NRZI) to the magnetic tape subsystem. With the basic magnetic tape subsystem installed, this option may be added three times (total of four tape units on one tape controller PCA). The HP 7970B Digital Magnetic Tape Unit (NRZI) must be the first unit from the interface if it is used in a mix configuration. The option includes:
 - (1) HP 7970B Digital Magnetic Tape Unit (NRZI).
 - (2) HP 13194A Multiunit Cable, approximately 20 feet (6 meters).
 - (3) Tape unit power cable assembly, approximately 8 feet (2.4 meters), part no. 8120-1395.
 - (4) Tape reel (empty), 10-1/2 inches (267 mm) diameter, part no. 1490-0738.

- (5) Tape reel (with 2400 feet (731 meters) blank tape), 10-1/2 inches (267 mm) diameter, part no. 9162-0025.
 - (6) Mounting accessories.
- b. Option -300 adds one HP 7970E Digital Magnetic Tape Unit to the magnetic tape subsystem. With the basic magnetic tape subsystem installed, this option may be added three times (total of four tape units on one tape controller PCA). In a mix configuration, HP 7970E Digital Magnetic Tape Units must be connected last in the series if HP 7970B Digital Magnetic Tape Units are used. If slave HP 7970E Digital Magnetic Tape Units (PE) are used they must follow the master unit in the series. The option includes:
- (1) Master HP 7970E Digital Magnetic Tape Unit (PE).
 - (2) HP 13194A Multiunit Cable, approximately 20 feet (6 meters).
 - (3) Tape unit power cable assembly, 8 feet (2.4 meters), part no. 8120-1395.
 - (4) Tape reel (empty), 10-1/2 inches (267 mm) diameter, part no. 1490-0738.
 - (5) Tape reel (with 2400 feet (731 meters) blank tape), 10-1/2 inches (267 mm) diameter, part no. 9162-0025.
 - (6) Mounting accessories.
- c. Option -400 adds one slave HP 7970E Digital Magnetic Tape Unit (PE) to the magnetic tape subsystem. This phase-encoded slave tape unit may only be used in conjunction with the master HP 7970E Digital Magnetic Tape Unit (PE). For example; if the basic magnetic tape subsystem includes Option -100, this option can be added three times. The option includes:
- (1) Slave HP 7970E Digital Magnetic Tape Unit (PE).
 - (2) HP 13194A-001 Multiunit Cable, approximately 20 feet (60 meters).
 - (3) Tape unit power cable assembly, 8 feet (2.4 meters), part no. 8120-1395.
 - (4) Tape reel (empty), 10-1/2 inches (267 mm) diameter, part no. 1490-0738.
 - (5) Tape reel (with 2400 feet (731 meters) blank tape), 10-1/2 inches (267 mm) diameter, part no. 9162-0025.
 - (6) Mounting accessories.



2180-20A

Figure 1-2. Example Subsystem Option Configuration Connections

1-12. **ADDITIONAL INTERFACES.** Additional interfaces may be included if it is necessary to split control of two or more tape units. These consist of only an HP 30215A Magnetic Tape Unit Interface. Contents of this interface are described in paragraph 1-7, step b.

1-13. **EQUIPMENT DESCRIPTION.**

1-14. The following paragraphs describe the peripheral devices, printed-circuit assemblies, and cables of the HP 30115A Nine-Track (NRZI-PE) Magnetic Tape Unit Subsystem.

1-15. **HP 7970B DIGITAL MAGNETIC TAPE UNIT (NRZI).**

1-16. The HP 7970B used in the basic magnetic tape unit subsystem has the specific options listed in steps below. Subsystem related details of the tape unit are condensed in the specifications paragraph. Refer to the tape unit operating and service manual for individual option identification numbers.

- a. Nine-track, read-after-write heads.
- b. Unit-select capability.
- c. Factory-wired for 800 characters-per-inch (cpi), (approximately 315 characters-per-centimeter) NRZI recording density.
- d. Forty-five (45) inches-per-second (114 centimeters-per-second) read only/read-after-write speed.

1-17. The HP 7970B Digital Magnetic Tape Unit is physically comprised of the tape transport proper, read assembly, write assembly, control and status assembly, and power assemblies. The fast-forward feature of the tape unit is not used when under system control. The unit may be operated off-line to facilitate maintenance. All manual operating controls and indicators for the magnetic tape subsystem are located on the tape unit. The system Auxiliary Control and Hardware Maintenance Panels are used to control the subsystem from the system. Refer to part I of the *HP 7970B Digital Magnetic Tape Unit Operating and Service Manual* for additional descriptions of the unit.

1-18. **MASTER HP 7970E DIGITAL MAGNETIC TAPE UNIT (PE).**

1-19. The master HP 7970E Digital Magnetic Tape Unit has the specific options listed below. Other details of the tape unit are condensed in the paragraph 1-30, Specifications. Refer to the *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual* for the individual option identification numbers. The specific options are as follows:

- a. Nine-track, read-after-write heads.
- b. Unit-select capability.
- c. Phase-encoded recording density 1600 characters-per-inch (cpi), (630 characters-per-centimeter).

- d. Master read module.
- e. Forty-five inches-per-second (ips) (114 centimeters-per-second) read/write speed.

1-20. The HP 7970E assemblies are described in the *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual*. This tape unit has more control over the actual read only/read-after-write operation, as far as error correcting capabilities are concerned, than does the HP 7970B. For that reason less control from the interface is necessary.

1-21. SLAVE HP 7970E DIGITAL MAGNETIC TAPE UNIT (PE).

1-22. The slave HP 7970E tape unit has specific options that are essentially the same as those for the HP 7970E master tape unit. The difference is that the slave tape unit contains a slave read module rather than a master read module. The *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual* also describes the slave tape unit features. Refer to that manual for further details. Note that the HP 13194A-001 Multiunit Cable is used to connect slave units and that different connectors in the tape units are used. Further details are included in section IV, Maintenance, of this manual.

1-23. HP 30215A MAGNETIC TAPE UNIT INTERFACE.

1-24. The HP 30215A Magnetic Tape Unit Interface is comprised of two printed-circuit assemblies (see table 1-1) that mount in a computer system PCA cage, two connecting cables between the printed-circuit-assemblies, and the interface cable between the printed-circuit-assemblies and tape unit. The basic functions of the interface are to supervise and control all operations called for by the computer system. The interface also signals the computer system if specific interrupt or error conditions occur. In the idle state, no Start Input/Output (SIO) program going on, the interface keeps monitoring the ready status of all tape units connected to it. Each PCA is described below.

1-25. MAGNETIC TAPE (NINE-TRACK) CONTROLLER PCA. The tape controller PCA interfaces the HP 3000 Computer System with the selected tape unit. The PCA contains integrated-circuit packs, components, and transistors grouped as follows:

- a. Bus interface logic and jumpers to interface and configure the subsystem with the HP 3000 Computer System. Printed-circuit assembly jumper position options and requirements are discussed in section IV, Maintenance.
- b. Tape unit interface logic to receive status, and to pass commands, data read from tape, data to be written on tape, to and from the selected tape unit.
- c. Status logic to check, register, and report subsystem conditions and signal status.
- d. Read-Only-Memory (ROM) integrated-circuit (I.C.) packs that contain the subsystem micro-program to control all subsystem functions.

- e. Controller processor interface logic to pass and receive commands and data to and from the controller processor PCA.
- f. PCA control logic, exercised by the controller processor, to control all tape controller PCA logic.

1-26. **MAGNETIC TAPE CONTROLLER PROCESSOR PCA.** The controller processor PCA controls overall subsystem operation by implementing instructions of the micro-program read from the tape controller PCA ROM I.C. packs. The PCA contains integrated-circuit packs, a transistor, and components grouped as follows:

- a. The internal clock logic and 9.216-MHz crystal that control overall subsystem timing.
- b. The 12-bit ROM address register (RAR) logic used to implement read-out of instructions from the ROM integrated-circuit packs on the tape controller PCA.
- c. The ROM output register (ROR) logic to hold and distribute 20-bit instruction words received from the ROM integrated-circuit packs.
- d. Decoding logic to decode instructions of the microprogram.
- e. Flag logic to initiate branching in the microprogram.
- f. Counter-register logic under control of microprogram instructions.
- g. Six general purpose and two dedicated (save and holding) registers. The registers are all used to implement instructions of the microcode. All control words and data handled by the subsystem pass through designated general purpose registers.
- h. The arithmetic and logic unit (ALU) performs functions as directed by the microprogram to control operation of the subsystem.
- i. The shift-rotate logic follows the ALU and performs directed functions for subsystem control.
- j. The PCA control logic to gate and enable all other controller processor PCA logic.

1-27. **CABLES.** The two short connecting cable assemblies supplied are 50-pin flat-ribbon types, part no. 30000-93052, that connect directly between the two PCA's of the HP 30215A Magnetic Tape Unit Interface as shown in section IV. The 20-foot (6 meter) cable, part no. 30215-60003, has one hooded connector on one end and three marked, hooded connectors on the other end. The single connector connects to the interface and the three connectors attach to the tape unit as shown in section IV.

1-28. STANDARD ACCESSORIES AND SERVICE ITEMS.

1-29. An I/O PCA extender supplied with the HP 3000 Computer System maintenance equipment is used for servicing PCA's of the HP 30215A Magnetic Tape Unit Interface. Accessories and service items supplied with the tape unit are described in the operating and service manual for the particular tape unit. Additional requirements for checkout and troubleshooting are described in section IV, Maintenance.

1-30. SPECIFICATIONS.

1-31. Pertinent specifications for the magnetic tape subsystem are listed in table 1-1.

1-32. IDENTIFICATION NUMBERS AND CODES.

1-33. Identification tag locations and codes used on the tape unit are described in the appropriate tape unit operating and service manual. Assembly and revision numbers for the PCA's of the HP 30215A Magnetic Tape Unit Interface are located on the outside corner of each board. Cable part numbers appear on hooded connectors.

Table 1-1. Magnetic Tape Subsystem Specifications

ITEM	SPECIFICATION
Recording Method	NRZI (with HP 7970B) Phase-Encoded (PE) (with HP 7970E). Read-after-write heads
Recording Channels	Eight data, one parity
Transfer Rates	36,000 bytes-per-second between interface and HP 7970B (max)
	18,000 words-per-second between interface and system using HP 7970B (max)
	72,000 bytes-per-second between interface and HP 7970E master or slave (max)
	36,000 words-per-second between interface and system using HP 7970E master or slave (max)

Table 1-1. Magnetic Tape Subsystem Specifications (Continued)

ITEM	SPECIFICATION
Tape Packing Density	800 characters-per-inch (cpi) (315 characters-per-centimeter) with HP 7970B 1600 characters-per-inch (cpi) (630 characters-per-centimeter) with HP 7970E
Character Type	Binary or ASCII
Tape	Certified 800 bits per-inch (bpi) (NRZI) Certified 3200 flux reversals per inch (frpi) (PE) Width: 0.5 in. (12.7 mm) Thickness: 1.5 mils
Tape Format	ANSI (USAS X3.22-1967) and industry compatible (800 cpi NRZI) ANSI- and industry compatible (1600 cpi PE)
Tape Start Time (Read)	8.33 milliseconds (max)
Tape Start Time (Write)	10.1 milliseconds (max)
Tape Stop Time	8.33 milliseconds (max)
Start Tape Travel (Read)	Approximately 0.187 in. (4.76 mm)
Start Tape Travel (Write)	Approximately 0.267 in. (6.8 mm)
Stop Tape Travel	Approximately 0.187 in. (4.76 mm)
Modes of Operation	
Forward Write	45 inches-per-second (ips) (114 centimeters-per-second)
Forward Read	45 ips (114 centimeters-per-second)
Reverse Read	45 ips (114 centimeters-per-second)
Rewind	160 ips (406 centimeters-per-second)
Load Point, beginning-of-tape (BOT) Search	Approximately 20 ips (50 centimeters-per-second)

Table 1-1. Magnetic Tape Subsystem Specifications (Continued)

ITEM	SPECIFICATION
Recording Accuracy Verification Methods	<p>Read-after-write character dropout detection (single-track error, self-correcting in PE tape unit) in read only mode</p> <p>Odd, lateral read/write parity</p> <p>Cyclic redundancy check (CRC) during read only and read-after-write modes (NRZI only)</p>
Storage Capacity	<p>Standard 10-1/2 in. (267 mm) diameter reels. Absolute max 2,500 ft (762 m) tape storage. Normal load 2,400 ft (731 m). Approximately 20 Megabyte storage capacity per reel. Actual value depends on record lengths, number of tape marks, etc.</p>
Power Requirements	
Tape Units	115 or 230 ($\pm 10\%$) Vac, 48 to 66 Hz, single phase. 400 volt-amperes (VA) maximum each
Controller Processor PCA	+ 5 volts, 6 amperes
Tape Controller PCA	+ 5 volts, 4 amperes
Common-Return Provisions	
Tape Units	Through three-prong power connector
Printed-Circuit Assemblies	Through power bus, power supplies, and system PCM
Environmental Requirements	
Operating Temperature	-5° to 55° C
Non-operating Temperature	-20° to 65° C
Relative Humidity	90% at 40° C (non-condensing)

Table 1-1. Magnetic Tape Subsystem Specifications (Continued)

ITEM	SPECIFICATION
Cooling Provisions	
Tape Units	Case vent holes
Printed-Circuit Assemblies	HP 3000 Computer System Cabinet Blowers
Heat Dissipation	
Tape Units	1365 BTU/hr (344 Kilo-calories-per-hour)
Printed-Circuit Assemblies	153 BTU/hr (38 Kilo-calories-per-hour)
	Cabinet cooling equipment should be capable of handling approximately 1500 BTU/hour (378 Kilo-calories-per-hour) additional heat output for basic subsystem.
Weights	
Tape Units	130 pounds (59 Kilograms)
Controller Processor PCA	24 ounces (680 Grams)
Tape Controller PCA	22-1/2 ounces (635 Grams)
Dimensions	
Tape Units	24 in. (610 mm) high 19 in. (483 mm) wide 12 in. (305 mm) deep
	Note: Tape units require 26-1/4 in. (667 mm) vertical mounting space which includes a 2-1/4 in. (57 mm) space below unit for blank panel.
Printed-Circuit Assemblies	1/16 in. (0.6 mm) thick 11-1/2 in. (292 mm) deep 13-11/16 in. (346 mm) wide

Table 1-1. Magnetic Tape Subsystem Specifications (Continued)

ITEM	SPECIFICATION
<p>Miscellaneous</p> <p>Controller Processor Crystal Frequency</p> <p>Record Protection Method</p> <p>Subsystem Tape Unit Capacity</p> <p>PCA Mount Facilities</p> <p>Interface Cable Length</p> <p>Tape Unit Mount Facilities</p> <p>Acetate/Polyester Tape Environmental Conditions:</p> <p> Temperature</p> <p> Relative Humidity</p>	<p>9.216 MHz (for 45 ips, 114 centimeters-per-second) tape travel.</p> <p>Write-enable Ring</p> <p>Four tape units from one tape controller subject to constraints of connection noted in maintenance section.</p> <p>HP 3000 Computer System PCA Module</p> <p>Approximately 20 ft (6 m)</p> <p>HP 3000 Computer System Cabinet within 20 ft (6 m) cable length of tape controller PCA.</p> <p>15.5° to 26.6°C (60° to 80°F)</p> <p>40 to 60%</p>
<p>Note: Unless otherwise indicated, specifications are applicable for the subsystem using 1600-cpi phase-encoded or 800-cpi NRZI tape units.</p>	



2-1. INTRODUCTION.

2-2. The scope of this section includes the following.

- a. An overview of HP 3000 Computer System I/O program control of the magnetic tape subsystem.
- b. Definitions of HP 3000 Computer System control and status parameters for the magnetic tape subsystem.
- c. Definitions of magnetic tape format and specifications.

2-3. I/O PROGRAM CONTROL.

2-4. Operation of the magnetic tape subsystem is closely tied to that of the computer system input/output processor (IOP) and multiplexer channel. For that reason, a brief discussion of subsystem related details of HP 3000 Computer System operation is presented in the following paragraphs. For detailed explanations of CPU/IOP and multiplexer channel operation, refer to the appropriate manuals. Details of software operating procedures may be found in system software documentation. Only a summary of the cold load and cold dump is presented in this manual. Microprogramming carried on within the magnetic tape subsystem interface is not directly under control of the computer system I/O program. However, commands to the subsystem may cause branching within the microprogram. Microprogramming is discussed in sections III and IV.

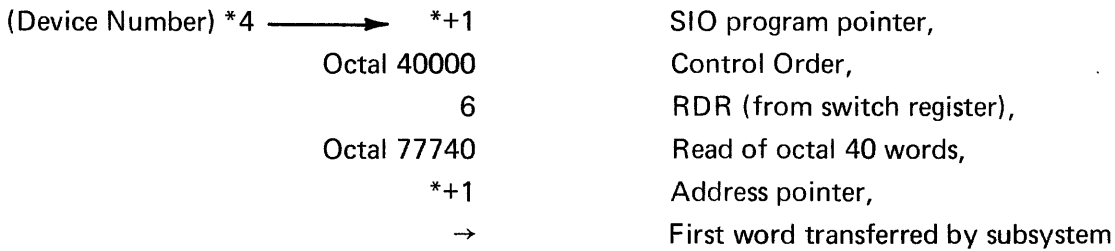
2-5. MAGNETIC TAPE SUBSYSTEM CONTROL METHODS.

2-6. All operating controls and indicators for the magnetic tape subsystem proper are on the tape unit. These are described in the applicable operating and service manual for the tape unit. HP 3000 Computer System controls that influence the magnetic tape subsystem in normal operation are located on the HP 30350A Auxiliary Control Panel Assembly. These controls are described in software procedures manuals. The tape units may also be operated in an off-line mode. This procedure is also described in the applicable tape unit and test accessory operating and service manuals. Parameters involved in single- and multiple-unit selection are described in paragraph 2-22. Information on the driver for the magnetic tape subsystem will be found in HP 3000 Computer System software documentation. Diagnostics for the subsystem are discussed in section IV. Information on the cold load and cold dump control methods is presented in paragraphs 2-7 through 2-12. The magnetic tape subsystem is also used for batch processing with up to four tape units driven by the HP 30215A Magnetic Tape Unit Interface.

2-7. COLD LOAD SEQUENCE. Cold load may be performed from tape unit number 0 (push button select) only. The switch register setting on the system auxiliary control panel should be as described below:

- a. Switch Register (0 through 7) := 6 (RDR Command Code),
- b. Switch Register (8 through 15) := Device Number.

2-8. For an explanation of magnetic tape subsystem commands refer to paragraph 2-22. Manually pushing the COLD LOAD push button (after pushing I/O RESET and CPU RESET) causes the CPU to generate an I/O Read program around the DRT entry for the magnetic tape subsystem, i.e.:



2-9. After setting up the I/O program, the CPU issues the Start Input/Output (SIO) command. The subsystem transfers 32 words read from block I on tape. These words further bootstrap the I/O program to read more blocks from tape. Thus any amount of core can be filled with data.

2-10. COLD DUMP SEQUENCE. The cold dump operation dumps the contents of system core in 4096-word blocks onto magnetic tape. This operation may be performed only on tape unit number 0 (pushbutton select) provided the tape reel has a write-enable ring in it. The switch register setting on the system auxiliary control panel should be as follows:

- a. Switch Register (0 through 7) := 4 (WRR Command Code),
- b. Switch Register (8 through 15) := Device Number.

CAUTION

A tape that is known to be good must be used for cold dumps. There will normally be only one chance for a dump. If the dump is not successful all information in the system may be lost.

2-11. Manually pushing the COLD DUMP button (after pushing I/O RESET and CPU RESET) causes the CPU to generate an I/O Write program around the DRT entry for the magnetic tape subsystem, i.e.:

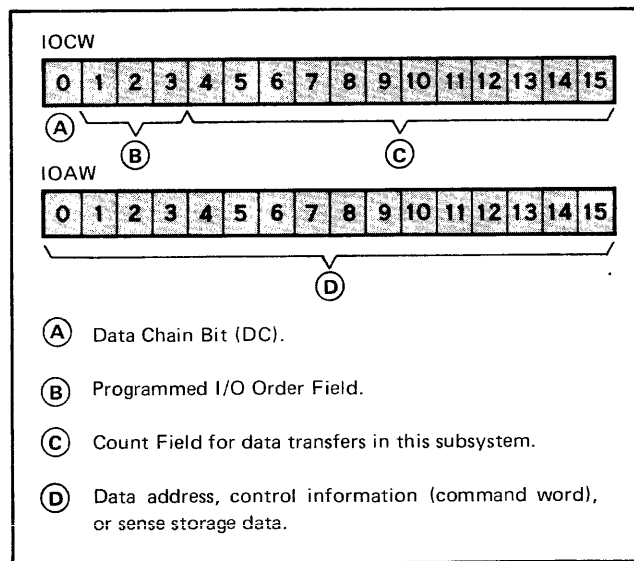
(Device Number) *4	→	*+1	SIO program pointer,
		Octal 40000	Control Order,
		4	WRR (from switch register),
		Octal 60000	Write of 4096 words,
		0	Starting Address.

2-12. After setting up the I/O program, the CPU issues an SIO command and the subsystem starts writing a block. The CPU monitors the SIO OK bit of the subsystem status word to determine whether a block is written or not. After completion of a block, the CPU updates the starting address and SIO program pointer to write the next block of 4096 words. The CPU also monitors the memory module interrupt to decide how much core the system actually has. When the cold dump is complete, the tape comes to a halt. The tape unit should be switched off line and rewound in the local mode to bring it to the load point.

2-13. SIO MODE CONTROL.

2-14. The magnetic tape subsystem operates in Start Input/Output (SIO) mode only. In this mode, the CPU executes an SIO instruction that transfers control of the I/O operation to the Input/Output Processor (IOP). The IOP controls the functions of the magnetic tape subsystem via the HP 30035A Multiplexer Channel. The multiplexer channel allows a total of 16 devices (subsystems) to operate simultaneously. The magnetic tape subsystem is one of the 16 devices served by the applicable multiplexer channel.

2-15. The I/O programs for this subsystem, as with other subsystems, are executed as a series of "double-words". That is, each command to control the subsystem is contained in appropriate portions of two sixteen-bit words. The first word is referred to as the Input-Output Command Word (IOCW). The second word is called the Input-Output Address Word (IOAW). Initial orders to the I/O structure and bus logic are contained in the IOCW. Read, write, and motion control function command words for the magnetic tape subsystem are contained in the IOAW. Figure 2-1 illustrates the IOCW/IOAW format.



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Figure 2-1. IOCW/IOAW Format

2-16. PROGRAMMED I/O ORDERS. Programmed I/O order bit patterns related to the magnetic tape subsystem are shown in table 2-1 and explained in table 2-2. These programmed I/O orders are contained in the IOCW. They are used by the multiplexer channel to control data transfers of the subsystem. The multiplexer channel issues appropriate strobes to the magnetic tape subsystem to control the read, write, and status acquisition functions based on receipt of these programmed I/O orders. The programmed I/O orders and the magnetic tape subsystem command words, described in paragraph 2-17, are issued on the 16-line I/O Data (IOD) bus. The orders and command words issued in the doublewords of an I/O program enable data transfer between memory and the magnetic tape subsystem of from one (minimum of two characters) to 4096 words without data chaining. With data chaining (bit 0 high) there is no limitation on the maximum number of words transferred except the length of tape on the reel and, during read operations, the amount of inter-block gap recorded. Additional discussions of the tape format and specifications are included in a later paragraph.

Table 2-1. Programmed I/O Order Bit Patterns

FIELD BIT PATTERN			PROGRAM I/O ORDER
1	2	3	
0	0	0	Jump
0	0	1	Return Residue
0	1	0	Interrupt
0	1	1	End
1	0	0	Control
1	0	1	Sense
1	1	0	Write
1	1	1	Read

Note: Field bit pattern numbers coincide with IOCW/IOAW bit position numbers that in turn coincide with IOD bus bit position numbers.

Table 2-2. Programmed I/O Order Definitions

PROGRAMMED I/O ORDER	DEFINITION
JUMP	Orders multiplexer channel (MUX CHAN) to jump to a memory address given in the second part of I/O program doubleword (IOAW) for a program. A conditional jump (bit 4 high) is treated as an unconditional jump (bit 4 low) in this subsystem.
RETURN RESIDUE	Causes the MUX CHAN to return word count residue, from a data transfer, to the CPU. Residue count is returned in the IOAW.

Table 2-2. Programmed I/O Order Definitions (Continued)

PROGRAMMED I/O ORDER	DEFINITION
INTERRUPT	Orders the subsystem (via MUX CHAN) to interrupt the CPU.
END	Notifies MUX CHAN of end of I/O program. If bit 4 is high, subsystem also interrupts CPU in addition to MUX CHAN. Subsystem status is returned to CPU in IOAW.
CONTROL	Notifies MUX CHAN that the following 16-bit word on the IOP data bus is a control word (in IOAW) for the magnetic tape subsystem. Count field in IOCW is stored in MUX CHAN.
SENSE	Orders magnetic tape subsystem, via MUX CHAN to output 16-bit status word on the IOP data (IOD) bus. Status is returned to CPU in the IOAW.
WRITE	Orders magnetic tape subsystem, via MUX CHAN, to transfer a block of data from memory to magnetic tape. Number of words to be transferred is contained in the COUNT field of the IOCW. MUX CHAN recognizes information in IOAW as starting address to get data.
READ	Orders magnetic tape subsystem, via MUX CHAN, to transfer a block of data from magnetic tape to memory. Number of words to be transferred is contained in the COUNT field of the IOCW. MUX CHAN recognizes information in IOAW as the starting data storage address.

2-17. **DIRECT I/O COMMANDS.** The subsystem will respond to the direct I/O command bit patterns shown in table 2-3. Table 2-4 explains the commands. These direct commands are issued by the CPU/IOP on a three-line bus directly to device controllers and to the multiplexer channel and are not in the IOCW/IOAW format even though the commands appear to be similar.

2-18. The direct I/O command TIO, shown in tables 2-3 and 2-4, may be issued at any time regardless of whether or not the magnetic tape unit interface is busy with other operations. The direct I/O command CIO, is also used to generate a programmed master clear (PMC) of the magnetic tape subsystem and for programmed clearing of an interrupt request from the magnetic tape subsystem. A particular data word bit pattern is expected to accomplish each of these operations. For example, a direct CIO command with a data word of 100000₈, will generate a PMC in the subsystem, i.e.:

if (S) := 100000 (octal),

and (S-K) := Device Number (S refers to the Stack pointer), then by issuing (CIO K), a PMC pulse is generated that forces the magnetic tape subsystem ROM microprogram to address 0000₈ (the START routine).

Table 2-3. Direct I/O Command Bit Patterns

CODE LINE BIT PATTERNS			MNEMONIC	DIRECT I/O COMMAND
2	1	0		
0	0	0	SIN	Set Interrupt
0	0	1	RESET INT	Reset Interrupt
0	1	0	SIO	Start Input Output (I/O)
0	1	1	SMSK	Set Mask
1	0	0	CIO	Control Input Output (I/O)
1	0	1	TIO	Test Input Output (I/O)

NOTES: 1. Since Direct Write I/O (110) and Read I/O (111) commands are not used by the magnetic tape subsystem, these commands are not listed.
 2. Field bit pattern numbers coincide with bit position numbers on the direct I/O command bus (part of the overall IOP bus).

Table 2-4. Direct I/O Command Definitions

MNEMONIC	DEFINITION
SIN	Commands magnetic tape subsystem to interrupt the CPU. See command word definitions for interrupt conditions.
RESET INT	Commands magnetic tape subsystem to clear interrupt logic.
SIO	Performs a TIO on magnetic tape subsystem, then transfers control from CPU to IOP. Starts I/O program doubleword fetch.
SMSK	Outputs 16-bit word on top-of-stack (TOS) as a mask word to the subsystem. The mask word alerts each subsystem in same mask group.
CIO	Outputs 16-bit word on top-of-stack (TOS) as a control word to the subsystem. (See text for further data on CIO).
TIO	Commands magnetic tape subsystem to return a 16-bit status word to TOS via IOP data bus.

2-19. When the START routine is entered, the selected tape unit will stop motion immediately and all interface PCA elements will be cleared. Any tape units that were rewinding will continue to the load point (BOT). Any non-selected tape units that were in the write mode will remain in that mode. The PMC will put the subsystem in tape-unit-number-zero mode.

2-20. A direct I/O command with a data word of 40000_8 will clear an interrupt request generated by the subsystem, i.e.:

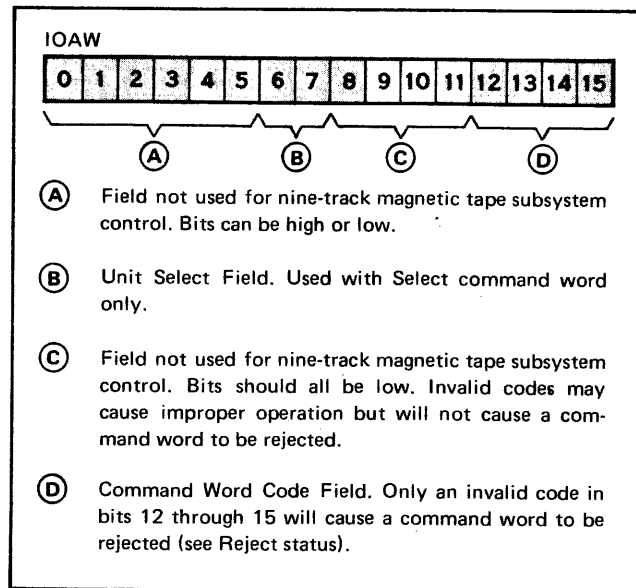
if (S) := 40000 (octal),
and (S-K) := Device number,
then by issuing (CIO K), the interrupt request (bit 2 of the Status Word) is cleared.

2-21. A power failure will force the magnetic tape subsystem to the CLEAR mode. Following a power failure, only a REW, RST, or BSR command word (in the IOAW) should be initially issued to the subsystem for each tape unit.

2-22. SUBSYSTEM COMMANDS.

2-23. The format of the IOAW for the magnetic tape subsystem is shown in figure 2-2. Table 2-5 shows the bit code patterns for the unit select field. Table 2-6 shows the bit code patterns for the command code field. The command code field carries the command words for the subsystem. Note that there are two commands that are used only for diagnostics and that there are three reserve codes. These are shown in table 2-7 and explained in table 2-9. The subsystem IOAW command code field entries are defined in table 2-8. Command words are grouped into three categories in the tables. These are:

- a. Read forward type: RDR, FSR, FSF and RDC.
- b. Read backward type: BSR, BSF.
- c. Write (forward only): WRR, WFM, GAP and WRZ.



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Figure 2-2. Magnetic Tape Subsystem IOAW Format

2-24. The Rewind, Rewind and Reset, and Select command words are also included in table 2-8. If a command word in an I/O program follows a command word in one of the same groups (previously listed) within 103 microseconds, tape motion will continue, interblock gap will be spaced over or written, and the new command word will be executed. If a command word follows one from a different group, tape motion will cease before the new command word is executed. In general, the system and I/O structure will not respond with a new command (of either groups mentioned) within 103 microseconds and tape motion will cease. If a tape unit is not ready and a command word other than a Select is issued, the new command word will be rejected.

Table 2-5. Unit Select Field Bit Patterns

FIELD BIT PATTERNS		MNEMONIC	FUNCTION
6	7		
0	0	CS0	Select unit number 0
0	1	CS1	Select unit number 1
1	0	CS2	Select unit number 2
1	1	CS3	Select unit number 3

NOTE: Field bit pattern numbers coincide with IOAW bit position numbers which in turn coincide with IOD bus bit position numbers.

Table 2-6. Command Code Field Bit Patterns

FIELD BIT PATTERNS				COMMAND WORD MNEMONIC	FUNCTION
12	13	14	15		
0	0	0	0	SEL	Select
0	1	1	0	RDR	Read Record
0	1	1	1	FSR	Forward Space Record
1	1	1	1	FSF	Forward Space File
1	0	1	0	BSR	Back Space Record
1	0	1	1	BSF	Back Space File
0	1	0	0	WRR	Write Record
1	1	0	1	WFM	Write (File) Tape Mark
0	1	0	1	GAP	Write Gap
1	0	0	0	REW	Rewind
1	0	0	1	RST	Rewind and Reset

NOTES: 1. Field bit pattern numbers coincide with IOAW bit position numbers which in turn coincide with IOD bus bit position numbers.

2. Bits 13 and 14 determine the command word group.

Table 2-7. Command Code Field Bit Patterns, Diagnostic and Reserved Commands

FIELD BIT PATTERNS				COMMAND WORD MNEMONIC	FUNCTION
12	13	14	15		
1	1	0	0	WRZ	Write Record With Zero Parity (800 cpi only)
1	1	1	0	RDC	Read Record With CRCC (800 cpi only)
0	0	0	1	—	Reserved code
0	0	1	0	—	Reserved code
0	0	1	1	—	Reserved code

NOTES: 1. Field bit pattern numbers coincide with IOAW bit position numbers which in turn coincide with IOD bus bit position numbers.
 2. Bits 13 and 14 determine the command word group.

Table 2-8. Magnetic Tape Subsystem Command Code Definitions

MNEMONIC	
SEL	The Select command is used to select the tape unit that will recognize all succeeding commands. Any commands following the SEL command will perform operations on the selected tape unit unless the command is rejected. A new tape unit may be selected at any time in an I/O program. Bits 6 and 7 of the IOAW are decoded only in this command. These bits are ignored in all other commands.
RDR	The Read Record command establishes the necessary conditions for a read operation on the selected tape unit. The order following the RDR command word must be a programmed I/O Read order. Forward motion of magnetic tape is not initiated until a programmed I/O Read order is encountered in the I/O program. The subsystem expects to receive at least two characters from tape, separated by no more than a 10.2 character spacing, within 25 ft (7.62 m) of tape. This must occur in order for the magnetic tape unit interface to treat the characters as part of a data block or tape mark. One character is considered noise and the magnetic tape unit interface begins searching for a data block starting from the noise character. If no data block or tape mark is encountered within 25 ft (7.62 m) of tape, the Tape Runaway encoded error (indicating an attempt to read blank tape) of the status word will be set and an interrupt will be generated.

Table 2-8. Magnetic Tape Subsystem Command Code Definitions (Continued)

MNEMONIC	DEFINITION
RDR (continued)	<p>If the character count of a data block read is odd, the Byte Count bit of the status word will be set. The right byte (bits 8 through 15) of the last word transferred to memory will be packed with zeros. If a tape mark is encountered, the corresponding status bit will be set and a following Return Residue Programmed I/O Order (if any) will indicate to the programmer that no data has been transferred.</p> <p>If data chaining (DC) is used with the read order (in the IOCW) for the RDR command and the data block is shorter than the programmed word count, a Command Reject encoded error of status will occur. The reason this will happen is that the magnetic tape unit interface expects a Control Programmed I/O Order after finishing reading a data block whereas the incoming order will be a Read. To avoid this problem, data chaining in the read mode should be used only when the block length on tape is well defined.</p> <p>Parity checks are made on each character and the CRCC is computed from the recovered characters. At the end of a data block the CRCC is read from tape and compared against the computed one. A good comparison ensures a good data block (800 cpi only).</p> <p>1600-cpi read electronics is self-correcting if a single track is in error. The data block is considered good as long as the tape unit does not indicate a Multiple Tracks in Error status.</p>
FSR	<p>The Forward Space Record (block) command spaces the tape forward until a tape mark or data block is found and passed. If a tape mark is read, the Tape Mark status bit is set. No parity checks are made. If no data block or tape mark is found within 25 ft (7.62 m) of tape, the Tape Runaway encoded error of the status word is set and an interrupt is generated.</p>
FSF	<p>The Forward Space File command spaces the tape forward until a tape mark is encountered and passed. No parity checks are made. The Tape Mark bit of the status word is set after spacing over a tape mark. If no tape mark or record is encountered within 25 ft (7.62 m) of tape, the Tape Runaway encoded error of the status word is set and an interrupt is generated.</p>

Table 2-8. Magnetic Tape Subsystem Command Code Definitions (Continued)

MNEMONIC	DEFINITIONS
BSR	<p>The Back Space Record command spaces the tape backward over a data block or tape mark until an interblock gap or beginning of tape (BOT) reflective marker is found. If a tape mark is back-spaced over, the Tape Mark bit of the status word will be set. No parity checks are made. If the tape is at the load point (BOT), the command will be ignored. If a backspace is performed after a write operation, the tape will move forward and 0.15 in. (3.81 mm) of tape will be erased before turning off the write current in the tape unit heads and initiating backward motion. This is done to avoid writing a noise character in the immediate gap when write current is switched off.</p> <p>During back-spacing, if a single character is found (no other character within 10 character spacings of it) it is considered a noise character. Tape motion continues in the reverse direction to search for a valid data block, tape mark, or load point (BOT) whichever comes first.</p>
BSF	<p>The Back Space File command will cause the tape to move backwards until a tape mark or BOT reflective marker, whichever comes first, is encountered and passed. No parity checks are made. The Tape Mark bit of the status word will be set if tape mark status is confirmed by the interface. If the tape is at the load point, (BOT) the command will be ignored. If a back-space is performed after a write operation, the tape will move forward and 0.15 in. (3.81 mm) of tape will be erased before current in the tape unit write heads is turned off and tape goes into reverse motion. This is done to avoid writing a noise character in the immediate gap when current in write heads is switched off.</p>
WRR	<p>The Write Record command establishes the necessary conditions for a write operation on the selected tape unit. Forward tape motion is not initiated until a programmed I/O Write order is encountered in the I/O program. If the tape is at the load point (BOT) a WRR operation will be automatically preceded by writing a 3.75 in. (95 mm) initial gap for 800-cpi tapes or writing a 2-in. (50 mm) identification burst followed by a 3.75-in. (95 mm) gap for 1600-cpi tapes.</p>

Table 2-8. Magnetic Tape Subsystem Command Code Definitions (Continued)

MNEMONIC	DEFINITION
<p>WRR (continued)</p>	<p>Since the I/O system is word oriented, the number of characters written on tape will always be even. When the end of the block is written on tape, the subsystem will request another command from the multiplexer channel and coast for 103 microseconds. If a new command of the same subgroup (WRR, WRZ, (800 cpi only) WFM, or GAP) is encountered during the coast the subsystem will space over the interblock gap and execute the new command. Any other command causes tape motion to halt first. The new command will be then acted upon. The coast time is short compared to system response time therefore, the tape motion will halt. The system cannot deliver the next command in time.</p> <p>Read-after-write parity checks are made on each character. The cyclic redundancy check character (CRCC) is computed from the recovered characters. The CRCC is compared with the CRCC read from the tape at the end of a data block. A good comparison ensures that the data block on tape is good (800 cpi only).</p> <p>Read-after-write operation in WRR command word execution also looks for two or more character dropout cases. One character dropout may go unnoticed because the magnetic tape standards allow 50% to 200% variation in the single character spacing. When character dropout is detected, the write operation is terminated; the tape is moved by a distance of the read/write head spacing, 0.15 in. (3.81 mm), before stopping. The Tape Error encoded error of the status word is set, and an interrupt is generated.</p> <p>There is no hardware restriction on minimum block length. Without data chaining (DC) in the I/O program, data block length may vary from one to 4096 words. With data chaining, there is no upper limit on data block length in the subsystem.</p>
<p>WFM</p>	<p>The Write (File) Tape Mark command establishes the necessary write conditions on the selected tape unit and causes a tape mark to be written on the tape. (Refer to the tape mark format information in text). The Tape Mark bit of the status word is set after the read-after-write operation confirms that a tape mark was indeed written on the tape. If the read-after-write operation does not confirm the validity of the tape mark, the Tape Error encoded error of the status word is set.</p>

Table 2-8. Magnetic Tape Subsystem Command Code Definitions (Continued)

MNEMONIC	DEFINITION
GAP	<p>The Write Gap command causes 3.75 in. (95 mm) of tape to be erased. Read-after-write operation during execution of this command will ensure that the erasure is noise-free. If the Tape Error encoded error of the status word is set during execution of the GAP command, it indicates that there was some noise left in the gap. An interrupt is generated. A reentry is not recommended because the back-spacing operation may skip over the noise character and move the tape past a good data block. The good data block may consequently get erased by the execution of the next GAP command.</p>
REW	<p>The Rewind command causes the selected tape unit to rewind and halt at the load point (BOT). Once this command is issued, the interface may select and command other tape units even before completion of the rewind operation on the commanded tape unit. If a new command is issued to a rewinding tape unit, the subsystem will reject the command and generate an interrupt (the exception is the SEL command which will not be rejected). When no SIO is going on, the interface monitors the status of the rewinding tape unit and generates an interrupt when the rewind operation is complete.</p>
RST	<p>The Rewind and Reset command is the same as the REW command, but in addition will cause the tape unit to go off-line (Local-not ready). When the rewind operation is complete there will be no interrupt because the tape unit is "not-ready". A manual intervention is required to bring the tape unit on-line and ready.</p>

Table 2-9. Diagnostic Command Code Definitions

MNEMONIC	DEFINITIONS
RDC	<p>The Read Record With CRCC command is used in 800-cpi operation only. The command is like the RDR command with the addition that at the end of a data block transfer, the Cyclic Redundancy Check Character (CRCC), as read from the tape, will also be transferred to memory. The CRCC transferred will be nine bits arranged in the data word as follows:</p> <ul style="list-style-type: none"> Bits 0 through 7-CRCC (0 = MSB), Bit 8-Parity of CRCC, Bits 9 through 15-packed with zeros.

Table 2-9. Diagnostic Command Code Definitions (Continued)

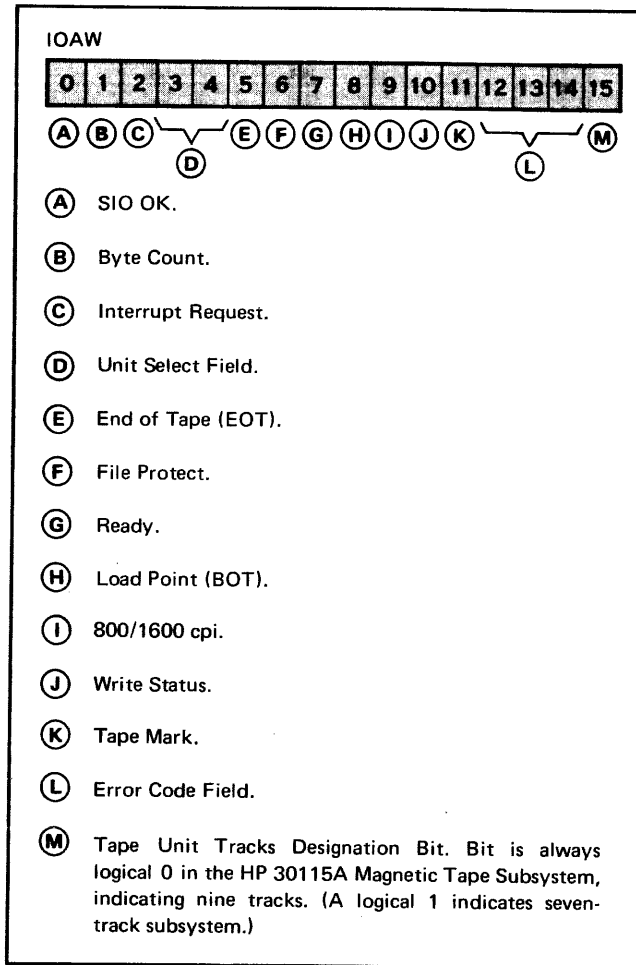
MNEMONIC	DEFINITION
RDC (continued)	To get this CRCC, the programmer must program for this extra word in the "word count" field of the IOCW. The Byte Count status information does not include the CRCC and refers only to the character count (odd or even) in the data block. In normal operation of the subsystem this command is not used. It is used in the on-line diagnostic environment.
WRZ	The Write Record With Zero Parity command is also used in 800-cpi operation only. The command is like the WRR command except while writing on tape, the parity of each character will be forced to logical 0. This feature enables the programmer to simulate character dropouts, error cases, or variable length gaps on tape in the diagnostic environment. In normal operation of the subsystem this command is not used.
RESERVED COMMAND CODES	There are three unused codes. Programming any one of these will cause the command to be rejected.

2-25. SUBSYSTEM STATUS.

2-26. Subsystem status is returned in the IOAW as a result of the Sense or End programmed I/O order or returned on the IOD bus because of a TIO, direct I/O command. Figure 2-3 illustrates the format of the status word. Table 2-10 explains the status word fields. The status word is a combination of tape controller PCA and tape unit status. "High" as mentioned in tables and figures refers to a high voltage level, (i.e., logic 1 condition) of the particular bit or bits mentioned, at the subsystem tape controller PCA Status Register input, (i.e., input pins of integrated circuit packs U166 and U167).

2-27. The tape unit status information, represented by all fields of the status word except the SIO OK, Interrupt Request, and the Error Code fields, is valid for the particular tape unit number represented by the unit select field. Table 2-11 defines the unit select field bit patterns. During the idle state, when no SIO program is being executed, the magnetic tape unit interface continuously selects one tape unit after the other to look for the Ready status. Thus, the tape unit status bits may be continuously changing as the selected tape unit field changes.

2-28. The SIO OK, Interrupt Request, and Error Code encoded error field represent the tape controller status. These fields of the status word are indicative of what happened in the last tape controller operation. The three bits of the encoded Error Code field represent:



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Figure 2-3. Magnetic Tape Subsystem Status Word Format

- a. A normal case.
- b. An error-free interrupt.
- c. Five different error-interrupt cases.
- d. One reserved code.

2-29. All error codes cause the subsystem to terminate the I/O program in progress and cause an interrupt. The entire field is cleared when a new command is given. To handle two or more interrupt conditions, a priority scheme is incorporated. The lowest octal value of the code (in bits 12, 13, 14) has the highest priority. Thus, Transfer Error (octal 1) has higher priority than Tape Error (octal 5) but lower priority than Unit

Interrupt (octal 0). In an instance where the tape controller detects both Timing Error (octal 4) and Tape Error (octal 5) the error code will indicate Timing Error. Thus, the error-interrupt code should be interpreted with the possibility of multiple errors.

2-30. Certain combinations like Tape Runaway and Tape Error should never occur. The former implies reading a blank tape while the latter can happen only if there is a tape with some data block information on it. All these error codes are cleared to the normal state (octal 7) whenever a new SIO program is issued. Each Error Code bit pattern is shown in table 2-12. Each code is explained in table 2-13.

Table 2-10. Subsystem Status Word Field Definitions

FIELD	DEFINITIONS
SIO OK	Field represents tape controller status. If bit 0 is high it indicates that SIO is permitted and currently there is no I/O program in progress.
BYTE COUNT	Field represents tape unit status. Bit 1 is high if an odd number of characters are read from a block on tape and transferred to memory with the lower half (bits 8 through 15) of the last word packed with zeros. The bit is low if an even number of characters are read from the tape. In the case of writing a block on tape, this bit will always be low. If an RDC command (800 cpi only) is executed, this status bit refers to the number of characters in the data block and does <i>not</i> include the CRC Character in the count. If part of the block is read, this bit will always be low since an even number of characters are read from the tape and transferred to memory. The bit goes low when a new command is issued.
INTERRUPT REQUEST	Field represents tape controller status. When bit 2 is high it indicates that in the last operation, the subsystem encountered an interrupt condition. One of the following constitutes an interrupt condition: <ul style="list-style-type: none"> a. A tape unit, not ready before, has become ready. b. Transfer Error is detected. c. Last SIO order is rejected. d. An attempt is made to read a blank reel of tape. e. Timing Error is detected. f. Tape Error is detected. Interrupt conditions b through f are error interrupts representing a malfunction. The only case of error-free interrupt condition is shown in a. Particular condition information is obtained from the Error

Table 2-10. Subsystem Status Word Field Definitions (Continued)

FIELD	DEFINITIONS
INTERRUPT REQUEST (continued)	Code encoded error field. The Interrupt Request bit is cleared by a Manual I/O Reset, a Programmed Master Clear, i.e., a direct CIO with a data word of 40000 ₈ , a programmed clear-interrupt, or Interrupt Active signal (indicating processing of an interrupt).
UNIT SELECT	Field represents tape unit status. The pattern of the bit 3 and 4 field indicates which of four possible tape units is currently selected. The rest of the tape unit status fields are valid only for that tape unit.
END OF TAPE	Field represents tape unit status. When bit 5 is high it indicates that the End-of-Tape (EOT) reflective marker was encountered during forward motion. The bit goes low only when the reflective marker is sensed and passed during reverse or rewind operations.
FILE PROTECT	Field represents tape unit status. When bit 6 is high it indicates that no write operation may be performed on the selected tape unit, i.e., the write enable ring is off the tape reel. The bit is low if the write enable ring is on the tape reel, indicating a write operation can be performed. The Write command will be rejected if a write operation is programmed when bit 6 of the status word is high.
READY	Field represents tape unit status. When bit 7 is high it indicates that the selected tape unit is on-line and ready. Attempting to command a tape unit that is not ready will cause the command to be rejected. A rewinding tape unit is in the not-ready state. The Ready status bit may be monitored by the I/O program to indicate whether or not a rewind operation is complete.
LOAD POINT (BOT)	Field represents tape unit status. When bit 8 is high it indicates that the selected tape unit is at the load point reflective marker (BOT) and ready to accept commands.
800/1600 BPI	Field represents tape unit status. Bit 9 indicates the read/write density capability of the selected tape unit. If this bit is low, it indicates 800 bits-per-inch, in a single track, or characters-per-inch (cpi), entire width of tape, density. If this bit is high, it indicates 1600 cpi density.

Table 2-10. Subsystem Status Word Field Definitions (Continued)

FIELD	DEFINITIONS
WRITE STATUS	Field represents tape unit status. When bit 10 is high it indicates that the last operation performed by the selected tape unit was a write operation. Current in the write heads is still on. The bit becomes low whenever a command other than that belonging to the Write group i.e., WRR, WFM, GAP, and WRZ is given to the subsystem.
TAPE MARK	Field represents tape unit status. If bit 11 is high it indicates that a tape mark was detected and passed during the last operation, which must have been a BSR, BSF, FSR, FSF, RDR, RDC or WFM. A new command will clear the EOF flip-flop making this test bit low at the Status Register.
ENCODED ERROR FIELD	Field represents tape controller status. Combinations of bits 12 through 14 represent five error states, one error-free (normal) state, one error-free interrupt case, and one reserved code.
TRACK DESIGNATION	Field represents drive status. Bit 15 is always low in HP 30115A Magnetic Tape Subsystem operation indicating nine-track tape units. A high represents a seven-track subsystem.
NOTE: Low/high levels refer to the level present at the input to the tape controller PCA status register, U166, U167.	

Table 2-11. Unit Select Field Status Bit Patterns

FIELD BIT PATTERNS		FUNCTION
3	4	
0	0	Unit Number 0 Selected
0	1	Unit Number 1 Selected
1	0	Unit Number 2 Selected
1	1	Unit Number 3 Selected
<p>NOTES: 1. Levels of status bits are shown at input to subsystem tape controller PCA Status Register.</p> <p>2. Field bit pattern numbers also coincide with IOAW bit position numbers which in turn coincide with IOD bus bit position numbers.</p>		

Table 2-12. Encoded Error Field Bit Patterns

FIELD BIT PATTERNS			FUNCTION
12	13	14	
0	0	0	Unit Interrupt (error free-highest priority)
0	0	1	Transfer Error
0	1	0	Command Reject
0	1	1	Tape Runaway
1	0	0	Timing Error
1	0	1	Tape Error (lowest priority)
1	1	0	Reserved Code
1	1	1	Error free (normal)

NOTES: 1. Status valid only for selected tape unit.
 2. Priority scheme, highest to lowest, is shown above. Scheme resolves priority for two or more errors occurring in one operation.
 3. Reserved code should never occur.
 4. Field bit pattern numbers coincide with IOAW bit position numbers which in turn coincide with IOD bus bit position numbers.

Table 2-13. Encoded Error Field Definitions

ERROR	DEFINITION
UNIT INTERRUPT	The Unit Interrupt is the only case where an interrupt is generated without an error condition existing. In the idle state (no SIO program going on), the magnetic tape unit interface continuously scans the status of the tape units. The tape unit "ready/not ready" information is stored in an internal register and keeps getting updated as the tape units go "not-ready" (because of removed tape reels or for rewinding operations), or become ready (rewind completed or new tape mounted). In the latter case an interrupt is generated, status bits 12 through 14 all go low (000), and the Unit Select field contains the information as to which tape unit just became ready, and selected.
TRANSFER ERROR	This error indicates that the system has detected a parity error going to or from memory or an out of bounds address. The subsystem will look for this error during each word transferred to the memory in the read mode. If a system parity error is detected, the subsystem will stop any data transfer to memory, stop the tape in the inter-block gap, clear the I/O interface logic, (to cause the SIO OK bit to

Table 2-13. Encoded Error Field Definitions (Continued)

ERROR	DEFINITION
TRANSFER ERROR (continued)	<p>go high), and generate an interrupt. Information, as to where in the SIO program chain this error was encountered, can be obtained by looking at the absolute memory address given by:</p> <p style="text-align: center;">ABSOLUTE (4* DEVICE NO.)-2.</p>
COMMAND REJECT	<p>This error code indicates that the current SIO program can not be executed for one of the following reasons:</p> <ol style="list-style-type: none"> a. A write type command was issued to a unit with a protected reel of tape (i.e., no write enable ring installed) (check File Protect status). b. An invalid command code in the IOAW, following a Control programmed I/O order (in the IOCW) was issued to the subsystem. c. An attempt has been made to command a not-ready or non-existing tape unit. A not-ready tape unit may, however, be issued a Select command. Check the ready status bit associated with the particular tape unit number (Unit Select field) in question. d. An I/O Read order has been encountered when the subsystem was expecting a Write or Control order (check I/O program). e. An I/O Write order has been encountered when the subsystem was expecting a Read or Control order (check I/O program). f. An I/O Control order has been encountered when the subsystem was expecting a Read or Write order. (check I/O program). g. A case has occurred where data chaining is programmed in a Read order and the block length on tape happens to be less than or equal to the word count present in all but the last Read order. When a command is rejected, the SIO program is terminated and an interrupt is generated. The absolute memory address of the rejected programmed I/O order is given by: <p style="text-align: center;">ABSOLUTE (4* DEVICE NO.) -2.</p>
TAPE RUNAWAY	<p>The magnetic tape recording standards specify that the maximum length of a gap on tape should be 25 ft (7.6 m). Tape Runaway error code status is present when, in a read forward operation, no block or tape mark is encountered for 25 ft (7.6 m) or more of tape. In this interface a one character block is considered a noise character and not a part of gap. The tape unit travel will be 25 ft (7.6 m) provided there is no noise character found. If a noise</p>

Table 2-13. Encoded Error Field Definitions (Continued)

ERROR	DEFINITION
<p>TAPE RUNAWAY (continued)</p>	<p>character is encountered, the interface attempts to find a valid block or tape mark within 25 ft (7.6 m) starting from the noise character. This error code indicates that the reel of tape being read is probably blank. The current I/O program will be terminated and an interrupt will be generated after setting the Tape Runaway status.</p>
<p>TIMING ERROR</p>	<p>This error code status is present when the I/O structure cannot service the subsystem at the data transfer rate of the magnetic tape subsystem. This can happen if certain high priority devices pre-empt the bandwidth required to service the magnetic tape subsystem. This error code status is present only after completing a read or write operation. The data transferred may not be valid. An interrupt is generated at the end of a read or write operation.</p>
<p>TAPE ERROR</p>	<p>This is the most common form of error code encountered during various operations of the subsystem. An interrupt is generated and the current I/O program is terminated for any of the conditions listed below. The reason for having only one status code representing all these types of errors is that the action taken by the programmer (re-trying, skipping over bad blocks, etc) can be the same for all cases.</p> <p>During WRR and WRZ command word execution:</p> <ol style="list-style-type: none"> a. A vertical parity error has been detected during read-after-write operation. b. The Cyclic Redundancy Check Character (CRCC) read from tape does not compare with the CRCC computed by recovering all read characters. A good compare ensures that the data block written on tape is good. (800 cpi only). c. Dropout of two or more adjacent characters is detected during read-after-write (800 cpi only). Dropout of one character may go unnoticed in this check mode (it will be caught by CRCC comparison) because the magnetic tape standards allow the single character spacing on tape to vary from 50% to 200% of the nominal spacing. The detection of character dropout while writing is important so that an undesired gap is not created in the same record. If the dropout is big enough, it can be mistaken for a valid interrecord gap and the reference of tape position is lost.

Table 2-13. Encoded Error Field Definitions (Continued)

ERROR	DEFINITION
TAPE ERROR (continued)	<p>d. On a 1600-cpi tape a single track or multiple tracks are found to be in error. The 1600-cpi tape unit read electronics is self-correcting if one of the nine tracks is found to have errors. It is possible to encounter a single-track error during writing or reading while the data transferred is good. In this subsystem the tape error code is set if a single-track error during write is encountered. This ensures that the tapes generated by this subsystem will be error-free in all nine tracks.</p> <p>During WFM command word execution: After writing the tape mark, the read-after-write operation tries to confirm the validity of the tape mark. The Tape Error code is set if a valid tape mark did not go on tape.</p> <p>During GAP command word execution: A noise character (or block in 1600-cpi operation) is detected in the 3.75-in. (95 mm) erased gap just written. A re-try is not recommended because during back-spacing, a tape may get positioned beyond a valid record (after skipping the noise character) and the execution of the GAP command may erase that record.</p> <p>During RDR and RDC command word execution:</p> <ol style="list-style-type: none"> a. A vertical parity error is detected in the record. b. The Cyclic Redundancy Check Character (CRCC) read from the tape does not match with the CRCC computed from read characters in the record (800-cpi only). c. In 1600 cpi, multiple tracks are found to be in error. A single track error is not indicated because the data transferred is valid. d. While reading only part of a record (word count < block length), cases a through c are still applied to the whole data block. There is no way to guarantee whether data transferred to memory is error-free or not.
RESERVED CODE	This code should never occur in any operation under any circumstances. The occurrence of this code implies a subsystem tape controller PCA malfunction.

Table 2-13. Encoded Error Field Definitions (Continued)

ERROR	DEFINITION
ERROR FREE CODE	This code represents normal subsystem operation during the last SIO program. The code also indicates, in the microprogram idle state, that no tape unit has become ready. An error-free operation will have octal 7 (code 111) present at the tape controller PCA Status Register input.

2-31. MAGNETIC TAPE FORMAT.

2-32. The magnetic tape specifications and format for the HP 30115A Magnetic Tape Subsystem are discussed in the following paragraphs and shown in figures 2-4 through 2-7.

2-33. TAPE FORMAT FOR 800-CPI TAPE UNITS.

2-34. Figure 2-4 represents the usable tape area and the constraints imposed for 800 cpi, NRZI tape unit operation. These constraints are set up to ease the interchangeability problems with tapes generated by different systems. The BOT and EOT reflective markers indicate the logical beginning and end of the recording area on tape. With this magnetic tape interface, a gap of 3.75 inches (95 mm) is written near the BOT.

2-35. TAPE FORMAT FOR 1600-CPI TAPE UNITS.

2-36. The physical characteristics of 1600-cpi tape, figure 2-5, are the same as those for 800-cpi tape. To distinguish between the two types, an identification burst (IDB) of 2 inches (51 mm) followed by a gap of 3.75 inches (95 mm) is written near the BOT marker. The IDB consists of consecutive flux reversals for the parity bit (1600 flux reversals-per-inch of tape) with all other tracks in the reference flux state. Thus, alternating logical 1's and 0's are written for 2 inches (51 mm) of tape in track 4.

2-37. In the read-after-write mode, the magnetic tape unit interface checks that the selected tape unit has 1600-cpi electronics and that the tape is at the BOT before writing the 2-inch (51 mm) IDB followed by a 3.75-inch (95 mm) gap.

2-38. TAPE MARK FORMATS.

2-39. Figure 2-6 shows the patterns of tape mark blocks for 800- and 1600-cpi tapes. Tape marks may be written any number of times on tape, subject to the constraints imposed by the tape mark command words and programmers choice. In 800-cpi operation, a tape mark record consists of writing octal 23 (bits 3, 6, 7) which goes on tape as logical 1's in tracks 2, 3 and 8. The remaining tracks are in the reference flux state. The tape mark LRC character occurs 8 bit spaces later.

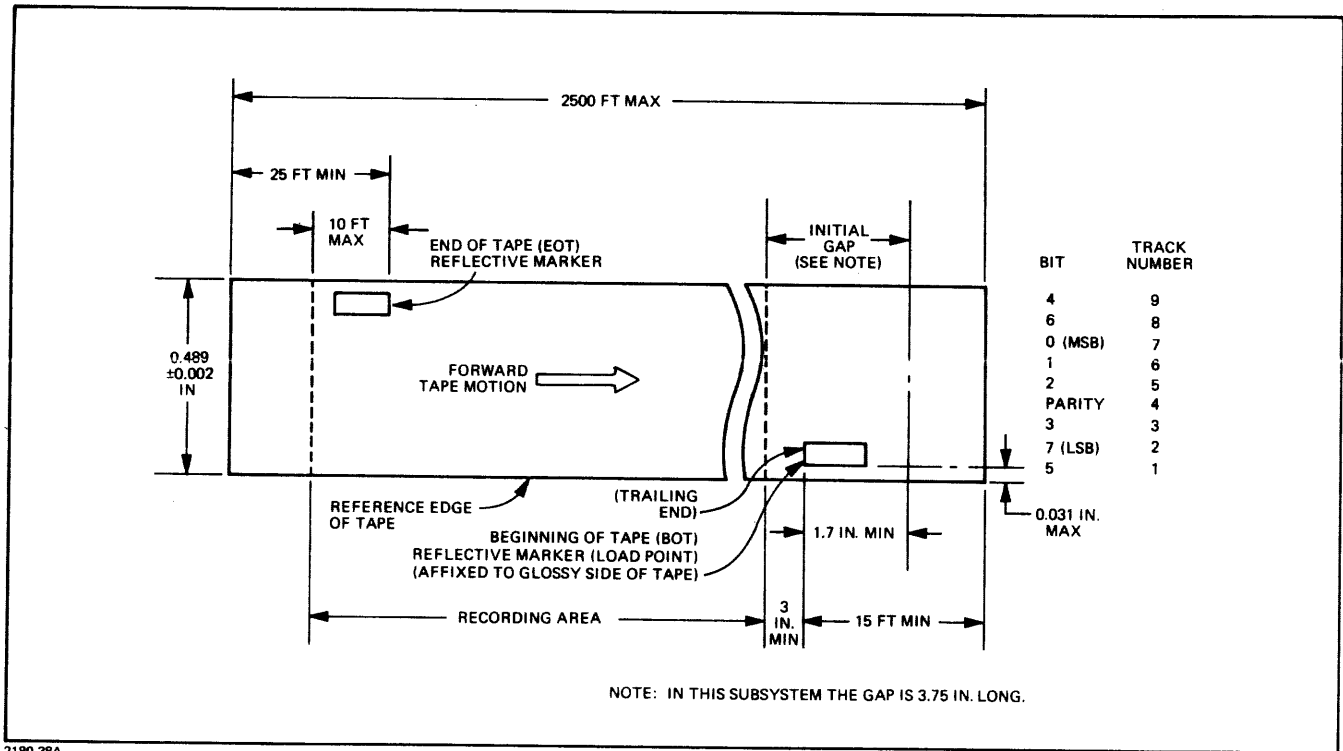
2-40. The tape mark for 1600-cpi tape consists of a written block of 80 flux reversals in tracks 1,2,4,5, 7,8 (octal 247) with other tracks in the reference flux state. A tape mark cannot be mistaken for a data block since all tracks have flux reversals in a valid data block.

2-41. BLOCK ORGANIZATION ON TAPE.

2-42. Magnetic tape recording has no restriction as to the length of data that can be written on tape except the physical length of tape. A typical tape may have variable-length records separated by a 0.5-inch nominal (± 0.1 inch) inter-block gap. In this subsystem, without data chaining, minimum data block length is 2 characters, maximum is 8198 characters. With data chaining continuous characters are written, until the END programmed I/O order, with no gaps between 8198 character blocks. Figure 2-7 illustrates data block format for 800-cpi and 1600-cpi tapes as transferred by the interface.

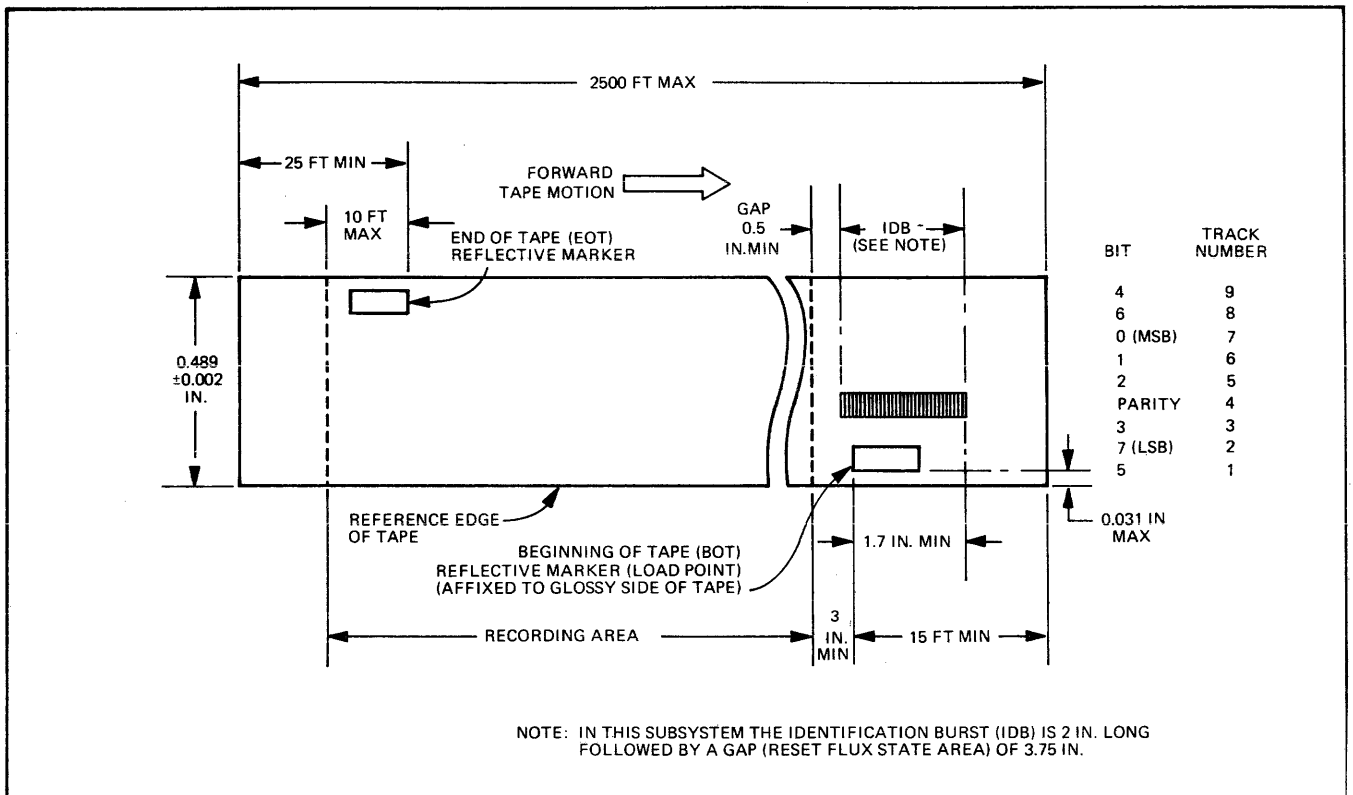
2-43. In 800-cpi operation a block on tape consists of the data block (information from the computer) plus a Cyclic Redundancy Check Character (CRCC) four character spaces later and a Longitudinal Redundancy Check Character (LRCC) four character spaces away from the CRCC. The CRCC is a unique character that is a function of the characters present in the data block. Its generation is explained in section III. The LRCC is written on tape by giving a write reset pulse to the tape unit. This makes the write amplifiers to go to a clear state. Each bit in the LRCC represents an even parity for that particular track's bits.

2-44. In 1600-cpi operation, a block on tape consists of the data block (information from the computer) preceded by a preamble and followed by a postamble (see figure 2-7). The preamble consists of 40 consecutive logical-0 characters (in all nine tracks) followed by a single, all-logical-1's character. The postamble consists of a single, all-logical-1's character followed by 40 consecutive logical-0 characters (in all nine tracks). In reverse tape motion, the postamble looks like the preamble and vice-versa.



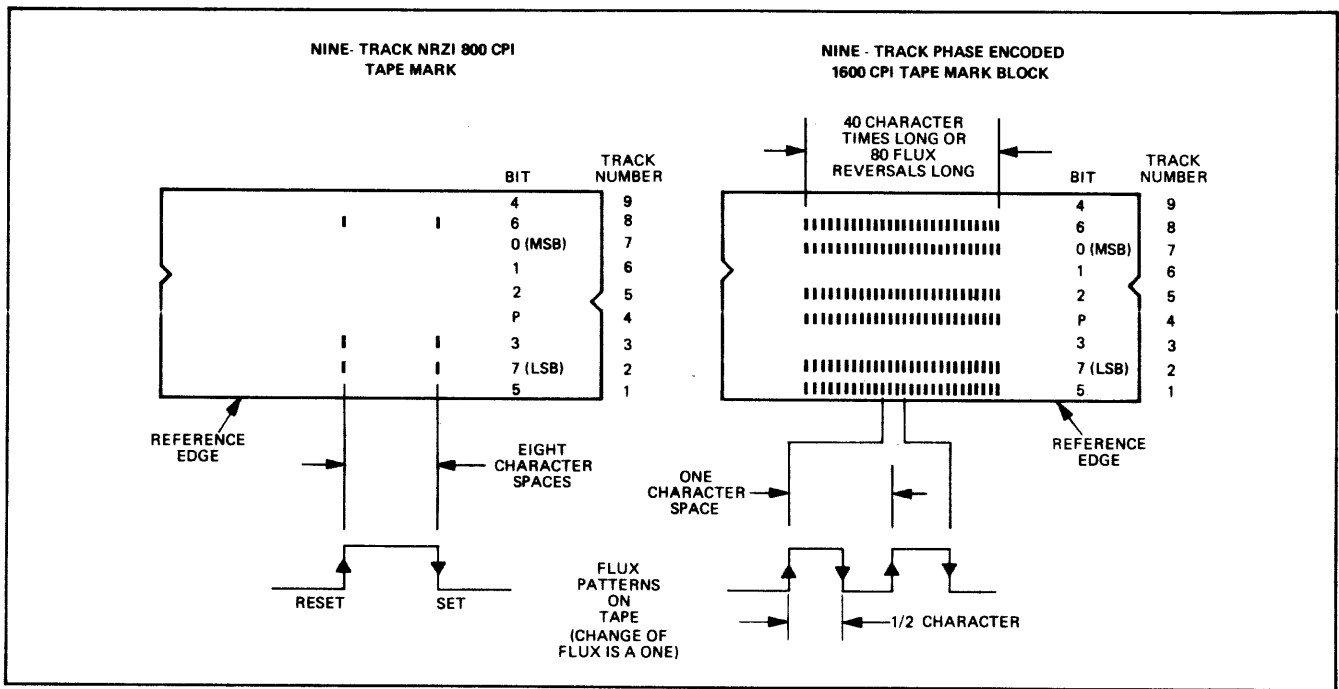
2180-38A

Figure 2-4. Tape Format for 800-cpi Tape



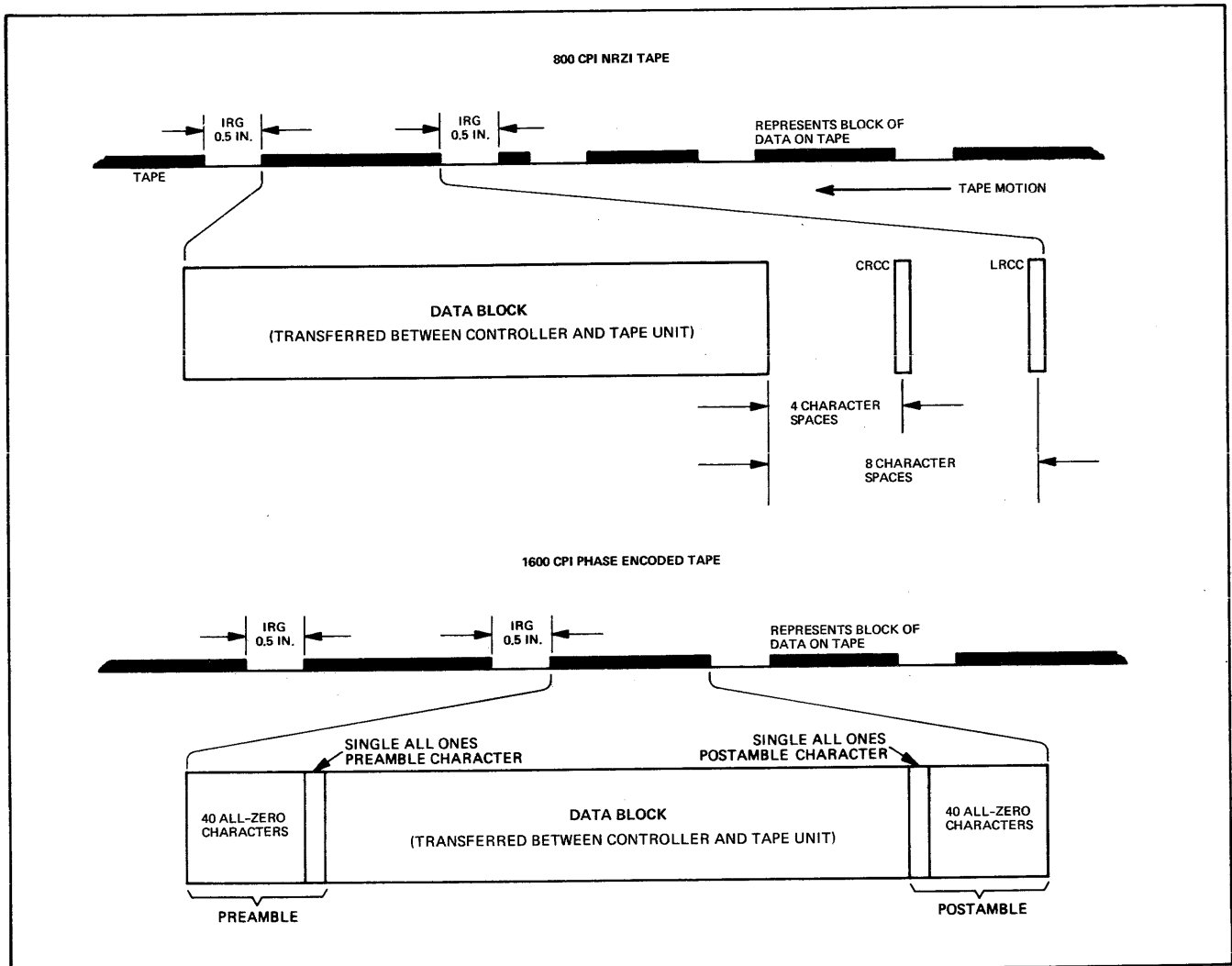
2180-39

Figure 2-5. Tape Format for 1600-cpi Tape



2180-40A

Figure 2-6. Tape Mark Formats, 800-cpi and 1600-cpi Tapes



2180-41A

Figure 2-7. Tape Data Block Organization, 800-cpi and 1600-cpi Tapes

3-1. INTRODUCTION.

3-2. This section includes an overall block diagram discussion of the magnetic tape subsystem and discussions of the interface printed-circuit assemblies (the tape controller PCA and controller processor PCA). In general, the basic magnetic tape subsystem is discussed (i.e., the interface and the nine-track NRZI tape unit). The interface discussion comprises the major portion of information. Applicable differences between phase encoded and NRZI operation are noted. The theory of operation for the NRZI tape unit will be found in the *HP 7970B Digital Magnetic Tape Unit Operating and Service Manual*. Theory of operation for the master and slave, phase-encoded tape units will be found in the *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual*.

3-3. Detailed microprogram flow charts, the microprogram listing, and timing diagrams discussed in this section are located in the maintenance section. This separation has been implemented to facilitate troubleshooting and maintenance of the subsystem.

3-4. SUBSYSTEM FUNCTIONAL SECTIONS.

3-5. The function of the magnetic tape subsystem is to provide the HP 3000 Computer System with a means to read and write system data to and from nine-track magnetic tape. The major sections of the subsystem that perform this function are the interface and the tape unit. These sections perform the following operations.

- a. Control movement of the magnetic tape through the selected tape unit.
- b. Unpack system data words passed to the magnetic tape subsystem and cause eight-bit parallel blocks of data to be written on magnetic tape in a selected tape unit.
- c. Read and pack data from magnetic tape into 16-bit parallel words for transmission to the HP 3000 Computer System.
- d. Cause appropriate checks to be made to ensure accurate recording and recovery of data from the magnetic tape.
- e. Cause appropriate identifying tape marks and gaps to be written on and read from the magnetic tape in response to I/O program commands.
- f. Report subsystem status to the system upon command.

3-6. An overall block diagram of the magnetic tape subsystem is shown in figure 3-1. The basic magnetic tape subsystem, using an NRZI tape unit, is shown as an example. A phase-encoded tape unit could just as well have been used. A single, additional tape unit, added as an option, is shown parallel-connected from unit 0. Up to four phase-encoded and NRZI tape units may be connected to the interface in any mix, subject to the constraints outlined in section I and shown in section IV. For simplicity, only a single additional unit is shown.

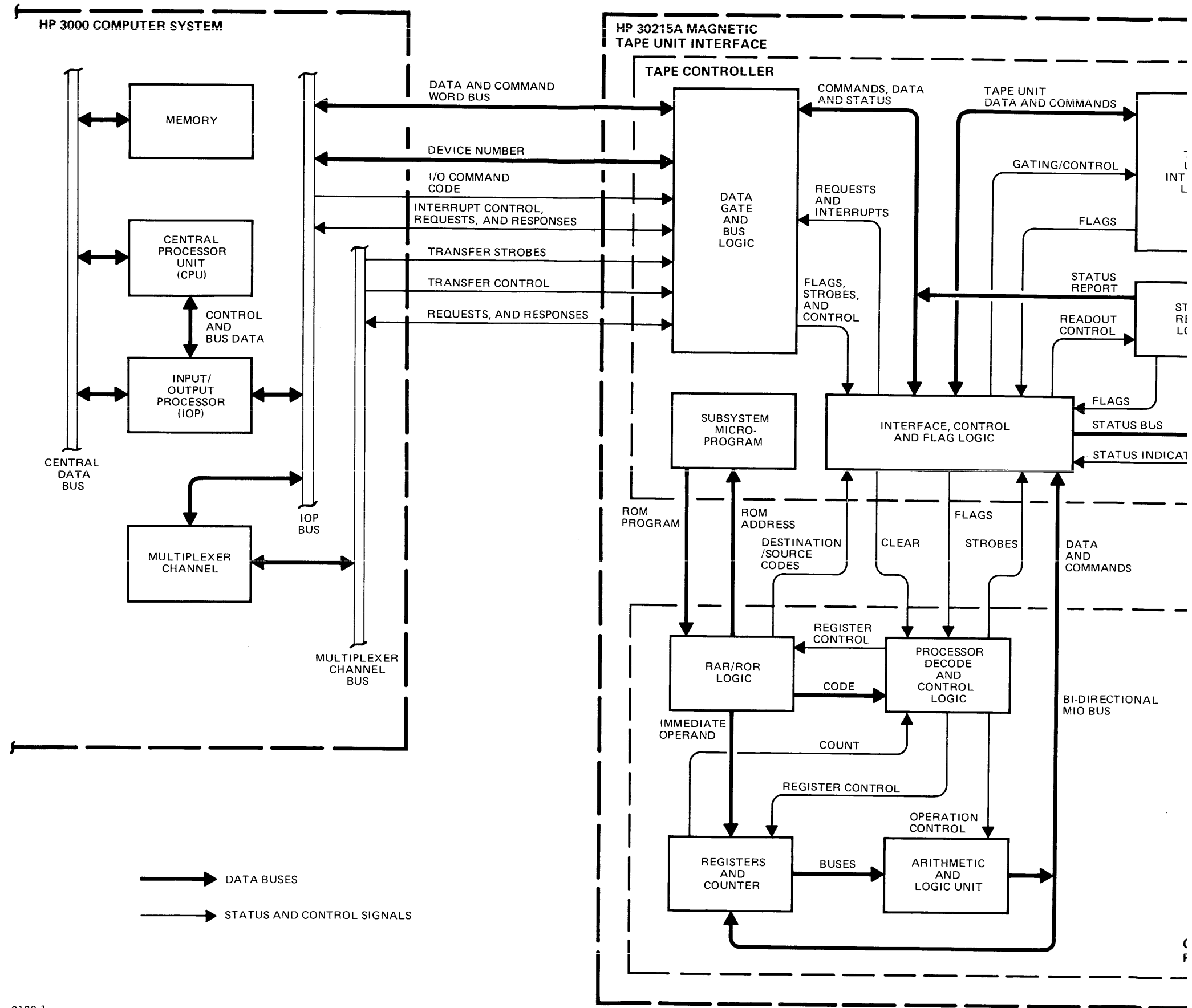
3-7. A discussion of the magnetic tape subsystem may be approached by identifying major logic portions and signal interface requirements. This is the case in the following paragraphs. First, the interface with the computer system is discussed. Secondly, interface between the tape unit and the tape controller PCA is discussed. The logic sections of the HP 30215A Magnetic Tape Unit Interface are then defined in paragraph 3-12.

3-8. COMPUTER SYSTEM INTERFACE SIGNALS.

3-9. Operation of the magnetic tape subsystem requires transfer of commands, data, and status information between the magnetic tape subsystem and the input/output processor (IOP) and multiplexer channel of the computer system. The magnetic tape subsystem is classed as a low-speed I/O device as far as I/O structure capability is concerned. Hence, control of data transmission is exercised by the multiplexer channel. The data gate and bus logic of the tape controller PCA in the interface provides all interface with the IOP and multiplexer channel via three major buses. These are the multiplexer channel (MUX CHAN) bus, IOP bus, and the power (PWR) bus. In the hardware, portions of the IOP bus signal grouping will be found mixed in the power bus grouping. Interface with the computer system is shown at the left in figure 3-1. Note in the diagram that only the IOP and multiplexer channel buses are shown. The data and command word bus, device number bus and the $\overline{\text{IODPRTY}}$ signal are in the IOP bus information group of signals. The I/O command code bus, shown in figure 3-1, is in the IOP bus control group of signals. All remaining signals for the IOP bus are grouped in the interrupt control, requests, and responses line shown on the diagram, which comprises the system status, and request responses groups of signals. IOP bus signals that are routed with the power bus grouping, as mentioned above, are shown here interfacing with the IOP bus in the interrupt control, requests, and responses bidirectional line. All interface shown with the computer system IOP bus is explained in more detail in table 3-1. All interface with the multiplexer channel bus is explained in more detail in table 3-2. Multiplexer channel bus signal groups shown in the diagram coincide with groups listed in table 3-2. The computer system buses contain more signals than listed in tables 3-1 and 3-2, but only signals used by the magnetic tape subsystem are listed. Sequences of signal occurrences are explained in the HP 30215A Magnetic Tape Unit Interface discussion.

3-10. TAPE UNIT INTERFACE SIGNALS.

3-11. Data, commands, and signals exchanged between the tape unit and interface are all exchanged via the subsystem interface cable. Routing is from the tape controller PCA, tape unit interface logic and the status report logic, as shown in figure 3-1, to three connectors that attach to the tape unit write, read, and motion control logic. The motion control logic controls forward, reverse, and rewind operations of the



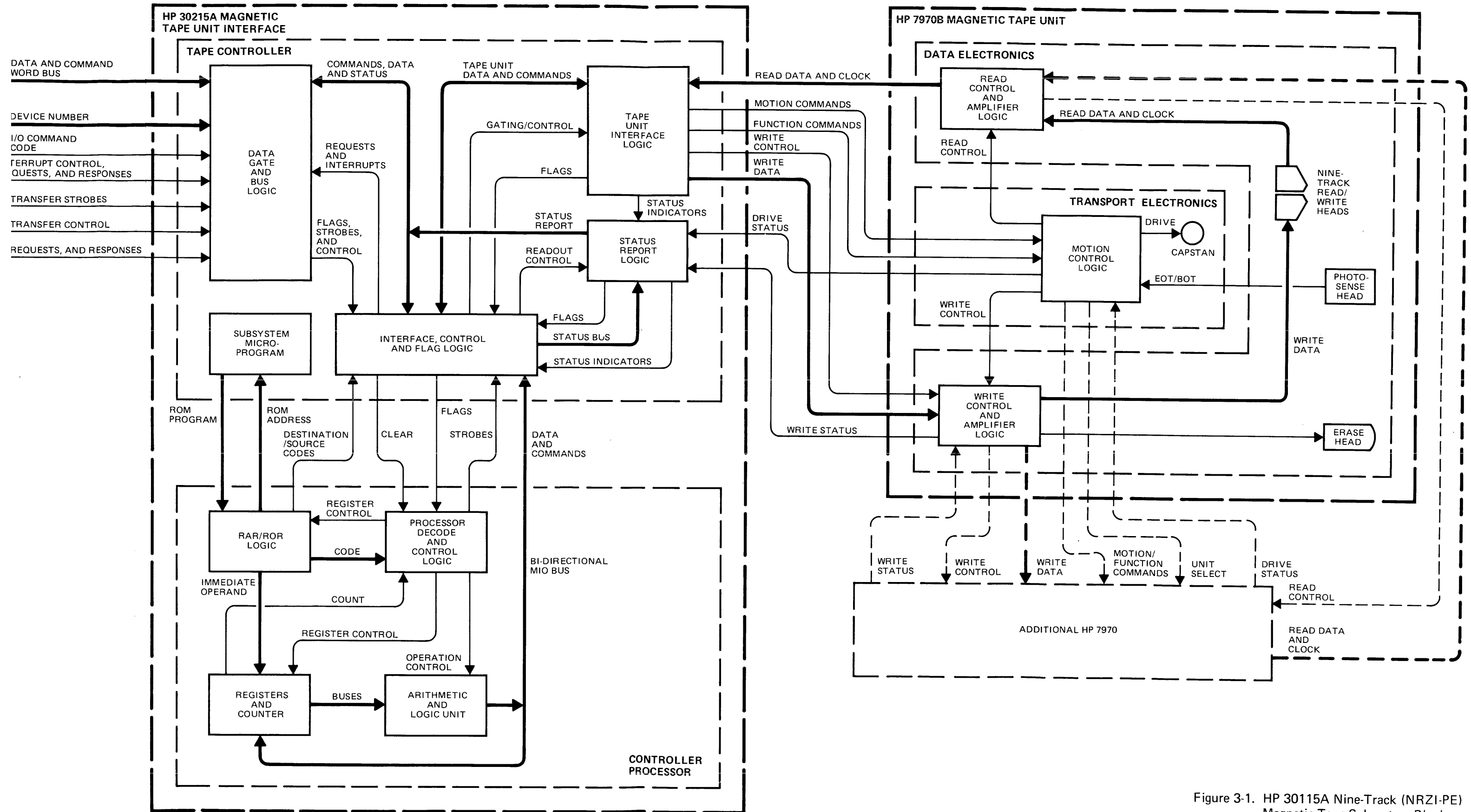


Figure 3-1. HP 30115A Nine-Track (NRZI-PE) Magnetic Tape Subsystem Block Diagram

tape unit upon command received from the tape controller. The read control and amplifier logic of the tape unit receives frames of data read by the heads and sends this data and a clock pulse to the tape controller. The write control and amplifier logic receives data and control signals from the tape controller for NRZI or PE recording on the tape via the write heads. Table 3-3 lists in more detail, and defines bus and signal lines routed between the tape controller and tape unit. Control of additional tape units is from the interface through the first tape unit. Additional tape units are parallel connected. See section IV for PE master-slave type connection details.

Table 3-1. Magnetic Tape Subsystem IOP Bus Interface Signals

NAME	MNEMONIC	DESCRIPTION
INFORMATION GROUP		
IOP DATA BUS	$\overline{\text{IOD 00:15}}$	<p>Sixteen-bit bi-directional bus. Inbound(to memory) active to IOP with $\overline{\text{SI}}$ signal low. Outbound (to subsystem) active with $\overline{\text{SO}}$ signal low. Bus carries:</p> <ul style="list-style-type: none"> a. All I/O data. b. Program command words to subsystem (in the IOAW). c. Subsystem status to IOP (in the IOAW). d. DRT address (device number) from magnetic tape subsystem to memory for I/O program execution.
DEVICE NUMBER BUS	$\overline{\text{DEVNO 00:07}}$	<p>Eight-bit bi-directional bus. Carries address (device number) of the subsystem that must interpret outbound commands and process data appearing on the IOP Data Bus. Bus also carries device interrupt number (address) for interrupt processing.</p>
DRT ADDRESS ODD PARITY	$\overline{\text{IODPRTY}}$	<p>Signal line to IOP carrying odd parity for DRT address transfer.</p>
CONTROL GROUP		
COMMAND OUT BUS	$\overline{\text{IOCMD 00:02}}$	<p>Three-bit bus. Carries Direct I/O commands to subsystem. Six of the eight direct I/O commands are used by the subsystem. These are:</p> <ul style="list-style-type: none"> a. Set Interrupt. b. Reset Interrupt. c. Start I/O. d. Set Mask. e. Control I/O. f. Test I/O.

Table 3-1. Magnetic Tape Subsystem IOP Bus Interface Signals (Continued)

NAME	MNEMONIC	DESCRIPTION
INTERRUPT CONTROL, REQUEST, AND RESPONSE GROUP		
INTERRUPT REQUEST	$\overline{\text{INT REQ 1}}$	Subsystem request to IOP for system software program interruption. IOP responds by causing the interrupt Poll to go high.
INTERRUPT ACKNOWLEDGE	$\overline{\text{INT ACK}}$	Subsystem response to Interrupt Poll with IOP with a low level signal. Subsystem interrupt number (address) is sent to IOP on device number bus simultaneously with this signal.
INTERRUPT POLL	INT POLL IN and INT POLL OUT	Interrupt Poll from IOP (in the Power Bus Grouping). Initiated in response to an Interrupt Request. Subsystem must cause the $\overline{\text{INT ACK}}$ signal to go low and gate its device interrupt number to the device number bus if the subsystem is requesting interrupt, or it must let the poll propagate. IOP accepts highest priority.
SERVICE OUT	$\overline{\text{SO}}$	Signal from the IOP (in the Power Bus Grouping) used as a direct I/O command validity signal for: <ul style="list-style-type: none"> a. Command Out Bus. b. Device Number Bus. c. IOP Data Bus. <p>In initialization sequence, $\overline{\text{SO}}$ causes magnetic tape subsystem to accept and respond to the data on the Command Out Bus and its device number. The magnetic tape subsystem will send a request for service to the multiplexer channel. $\overline{\text{SO}}$ is also used as IOP Data bus outbound validity signal.</p>
SERVICE IN	$\overline{\text{SI}}$	Subsystem acknowledge signal (in the Power Bus Grouping) to IOP for receipt of programmed strobes from the multiplexer channel.
SYSTEM STATUS GROUP		
POWER ON	PWR ON	Signal from Power Bus Grouping indicates HP 3000 Computer System Power Supplies ready. Enables Tape Unit Select Logic on tape controller PCA of interface.

Table 3-1. Magnetic Tape Subsystem IOP Bus Interface Signals (Continued)

NAME	MNEMONIC	DESCRIPTION
SYSTEM STATUS GROUP (Cont.)		
I/O RESET	IO RESET	Signal in Power Bus Grouping from I/O RESET button in HP 3000 Computer System. Acts as master clear for subsystem logic. Also sent at system power-up time.
NOTE: Only the signals used by the HP 30115A Magnetic Tape Subsystem are listed.		

Table 3-2. Magnetic Tape Subsystem Multiplexer Channel Bus Interface Signals

NAME	MNEMONIC	DESCRIPTION
TRANSFER CONTROL GROUP		
CHANNEL SERVICE OUT	$\overline{\text{CHAN SO}}$	Signal from multiplexer channel. Indicates multiplexer channel now receiving service for the subsystem from the IOP after subsystem has requested service from the multiplexer channel. Accompanied by SR line pulled low and DEVNO DB strobe during initialization.
CHANNEL ACKNOWLEDGE	$\overline{\text{CHAN ACK}}$	Signal from multiplexer channel. Acknowledges receipt of Device End signal from subsystem.
SIO ENABLE	$\overline{\text{SIO ENABLE}}$	Signal level (low) from multiplexer channel necessary to permit subsystem initialization and communication with the system
TOGGLE SERVICE REQUEST	$\overline{\text{TOGGLE SR}}$	Signal from multiplexer channel to clear Service Request after initialization sequence is complete. Signal also sets and clears Service Request during DRT Fetch operations.
TOGGLE SIO OK	TOGGLE SIO OK	Signal from multiplexer channel at the end of an entire SIO program. Puts subsystem into idle state ready for next I/O program
TOGGLE IN TRANSFER	TOGGLE IN XFER	Signal from multiplexer channel to prepare subsystem for sequence of data transfers to the system from magnetic tape. Clears the subsystem of the read mode at the end of each data transfer sequence <i>if</i> data chaining is not

Table 3-2. Magnetic Tape Subsystem Multiplexer Channel Bus Interface Signals (Continued)

NAME	MNEMONIC	- DESCRIPTION
TRANSFER CONTROL GROUP (Cont.)		
TOGGLE IN TRANSFER (Cont.)	TOGGLE IN XFER (Cont.)	in effect. Signal clears the read mode at the end of the entire data chaining transfer sequence if data chaining is in effect.
TOGGLE OUT TRANSFER	TOGGLE OUT XFER	Signal from multiplexer channel to prepare subsystem for a sequence of data transfers from memory to magnetic tape. Clears the subsystem write mode at end of each data transfer sequence <i>if</i> data chaining is not in effect. Signal clears the subsystem write mode at the end of the entire data chaining transfer sequence in this case.
END OF TRANSFER	$\overline{\text{EOT}}$	Signal from multiplexer channel, not used in the subsystem although received in the interface.
REQUEST AND RESPONSE GROUP		
SERVICE REQUEST	SR	Signal to multiplexer channel, one of 16 priority lines selected by jumper in the subsystem. Signal goes high for following conditions: <ul style="list-style-type: none"> a. When subsystem completes execution of last I/O Program Control Word. b. When subsystem has data for transfer to memory or requires more data from memory. c. When transfer has ended. d. After first I/O Program Control Word is received. <p>Service request line is pulled low by the multiplexer channel and Channel Service Out signal is sent to subsystem in answer to high Service Request signal to allow programmed strobes to be gated into subsystem.</p>
REQUEST	$\overline{\text{REQ}}$	Signal to multiplexer channel for SIO operation initialization. Generated once at the start of SIO. Subsystem is in priority line for service (priority is established by SR signal). Multiplexer channel generates Service-in signal to IOP and puts multiplexer channel in the DRT Fetch mode for this subsystem RAM address.

Table 3-2. Magnetic Tape Subsystem Multiplexer Channel Bus Interface Signals (Continued)

NAME	MNEMONIC	DESCRIPTION
REQUEST AND RESPONSE GROUP (Cont.)		
ACKNOWLEDGE SERVICE REQUEST	$\overline{\text{ACK SR}}$	Signal from multiplexer channel acknowledging receipt of a Service Request signal. Clears Device Service Request condition in the subsystem.
DEVICE END	$\overline{\text{DEV END1}}$	Signal to multiplexer channel causes termination of read operation for the subsystem at the multiplexer channel. Sent from subsystem as a result of end of data being processed.
TRANSFER ERROR	$\overline{\text{XFER ERROR}}$	Signal from memory through multiplexer channel due to one or more of the following: <ul style="list-style-type: none"> a. Parity error. b. Illegal address. c. System error.
TRANSFER STROBE GROUP		
DEVICE NUMBER DATA BASE	$\overline{\text{DEVNO DB}}$	Strobe from multiplexer channel at time of Channel Service Out and cancelled Service Request returned signals. Causes subsystem to gate DRT address to the IOP Data Bus. Multiplexer channel goes to DRT fetch phase for this subsystem RAM address and Service In is sent to the IOP.
PROGRAM COMMAND ONE	$\overline{\text{P CMD 1}}$	Strobe from multiplexer channel to strobe in the first I/O program Control Word for control of a subsystem. Occurs when the multiplexer channel decodes an I/O program word Control order and it is in the first I/O program word (IOCW) fetch phase. For this subsystem, the first I/O program word (IOCW) does not contain a Control Word, therefore, the subsystem simply returns a Service-In signal to the IOP and requests multiplexer channel service.
PROGRAMMED CONTROL STROBE	$\overline{\text{P CONT STB}}$	Strobe from multiplexer channel. Indicates contents of IOAW (on the IOP Data Bus) is an operation Control Word for the subsystem. The Control Word is gated into subsystem data register. Strobe is a result of the multiplexer channel being in the second I/O program word

Table 3-2. Magnetic Tape Subsystem Multiplexer Channel Bus Interface Signals (Continued)

NAME	MNEMONIC	DESCRIPTION
TRANSFER STROBE GROUP (Cont.)		
PROGRAMMED CONTROL STROBE (Cont.)	$\overline{\text{P CONT STB}}$ (Cont.)	(IOAW) fetch phase and decoding the I/O program word Control order.
PROGRAMMED WRITE STROBE	$\overline{\text{P WRITE STB}}$	Strobe from multiplexer channel. Indicates data on the IOP Data Bus is data to be written on magnetic tape by the subsystem. Data is gated into subsystem data register. Strobe results from multiplexer channel being in Data Transfer Phase, with a decoded I/O program word Write order, and not having a Device End condition present.
PROGRAMMED READ STROBE	$\overline{\text{P READ STB}}$	Strobe from multiplexer channel. Indicates data to be placed on the IOP Data Bus that has been read from magnetic tape by the subsystem. Data is strobed onto IOP Data Bus. Strobe results from multiplexer channel being in the Data Transfer Phase, with a decoded I/O program word Read order, and not having a Device End condition present.
PROGRAMMED STATUS STROBE	$\overline{\text{P STAT STB}}$	Strobe from multiplexer channel to obtain output from subsystem status register as IOAW (Status word) on the IOP Data Bus. Strobe is a result of the multiplexer channel decoding an I/O program word Sense or End order and being in the Fetch Second I/O Program Word (IOAW) phase.
SET INTERRUPT	$\overline{\text{SET INT}}$	Strobe from multiplexer channel to place subsystem in interrupt state. Strobe is a result of multiplexer channel being in the Fetch Second I/O Program Word (IOAW) phase and decoding an I/O program word End order with bit four of the IOCW set to cause an interrupt. Enables the subsystem to inform the IOP/CPU that operation has ended.

Table 3-3. Interface-to-Tape Unit Signals

NAME	MNEMONICS	DESCRIPTION
WRITE GROUP		
WRITE DATA BUS	$\overline{\text{WD 0:7}}$	Data levels to write module of tape unit. The logical state of each write data line of the bus at Write Clock time defines the character to be written on tape. For NRZI tape units, a low level on a write data bus line causes a change of flux to occur. (A logical 1 is written.) A high level on a write data bus line causes no change of flux on tape. (A logical 0 is written.) The state of erased NRZI tape flux is the same as the reference flux state. For PE tape units, a low level on a write data bus line is represented on tape as a flux change in the direction opposite to the sense of inter-block gap flux. (A logical 1 is written.) A high level on a write data bus line causes a flux change in the direction of inter-block gap flux. (A logical 0 is written.) Erased tape is represented by no flux change after the tape is brought to the inter-block gap flux state. (Reference flux state.)
WRITE DATA PARITY	$\overline{\text{WDP}}$	Data level to write module of tape unit. Same characteristics as Write Data Bus lines.
WRITE CLOCK	$\overline{\text{WC}}$	Pulse to write module of tape unit. A low causes flux polarity to be written on tape corresponding to the logical state of the individual write data lines and the write parity line for NRZI. Tape unit must be in the write condition. This pulse should be at least two (2) microseconds duration.
WRITE RESET	$\overline{\text{WRS}}$	Signal level to write module of tape unit. A transition to a low level causes longitudinal redundancy check (LRC) character to be written on tape provided the tape unit is in Write mode. This signal is not used in phase-encoded tape units. This pulse should be at least two (2) microseconds duration.
READ GROUP		
READ DATA BUS	$\overline{\text{RD 0:7}}$	Data levels from read module of tape unit. The bus transmits detected characters read from the tape.
READ DATA PARITY	$\overline{\text{RDP}}$	Data level from read module of tape unit. Same characteristics as Read Data Bus lines.
READ CLOCK	$\overline{\text{RC}}$	Pulse from read module of tape unit. Indicates that a character has been read from tape and is present on the Read Data Bus. The pulse is at least two (2) microseconds duration.
FUNCTION COMMANDS		
SELECT COMMAND	$\overline{\text{CS 0:3}}$	Four individual lines to motion control module of tape unit. Low level selects a particular on-line tape unit from a group connected to a common interface cable when subsystem options are used. Otherwise CS0 selects only tape unit 0.

Table 3-3. Interface-to-Tape Unit Signals (Continued)

NAME	MNEMONIC	DESCRIPTION
FUNCTION COMMANDS (Cont.)		
OFF-LINE COMMAND	\overline{CL}	Signal level to motion control module of tape unit. A low level of this signal clears the write condition and terminates the on-line condition of the selected tape unit.
SET WRITE COMMAND	\overline{WSW}	Signal level to motion control module of tape unit. Transition to a low level of the \overline{WSW} signal enables the setting of the selected and on-line tape unit's write condition, provided the tape unit is ready and write-enabled. High state of the signal enables the clearing of the tape unit's write condition.
MOTION COMMANDS		
FORWARD COMMAND	\overline{CF}	Signal level to motion control module of tape unit. Providing the tape unit is selected and ready, this command causes tape to be driven in the forward direction.
REVERSE COMMAND	\overline{CR}	Signal level to motion control module of tape unit. When at a low level, clears the Write condition and causes the tape to be driven in the reverse direction, provided that the tape unit is selected and ready. Load point status inhibits the response to this command.
REWIND COMMAND	\overline{CRW}	Signal level to motion control module of tape unit. Clears the Write command on the selected tape unit and initiates a rewind operation, provided that the tape unit is ready and not at load point. Tape is positioned at load point at the end of this operation.
STATUS		
WRITE STATUS	\overline{SW}	Signal level from write module of tape unit. Indicates that the selected tape unit is write-enabled and current is flowing in the write and erase heads. Tape flux is of inter-block gap polarity until a Write Clock pulse is received (NRZI).
READY STATUS	\overline{SR}	Signal level from motion control module of tape unit. Indicates that the tape unit is selected, is on-line, the initial loading sequence is complete, and the tape unit is not rewinding.

Table 3-3. Interface-to-Tape Unit Signals (Continued)

NAME	MNEMONIC	DESCRIPTION
STATUS (Cont.)		
LOAD POINT STATUS	$\overline{\text{SLP}}$	Signal level from motion control module of tape unit. A low level indicates that the tape unit is selected, is on-line, and the tape is positioned at the load point reflective marker.
FILE PROTECT STATUS	$\overline{\text{SFP}}$	Signal level from motion control module of tape unit. A low level indicates that the selected, and on-line unit is not write-enabled (write enable ring is not present in the tape reel).
END OF TAPE STATUS	$\overline{\text{SET}}$	Signal level from motion control module of tape unit. Indicates that an End-of-Tape reflective marker was detected by the photosensitive head of a selected and on-line tape unit. A low level is maintained until cancellation of the End-of-Tape condition by the passage of the reflective marker in the reverse direction.
PHASE ENCODED STATUS (800/1600 cpi)	$\overline{\text{SD16}}$	Signal level from tape unit. Indicates 800- or 1600-cpi density recording for the subsystem. Interface cable pin not connected at HP 7970B Digital Magnetic Tape Unit. Line tied high at input to tape controller PCA provides low input to tape controller status register when 800-cpi tape unit is selected. Line pulled low at tape controller PCA for 1600-cpi tape unit selected.
END OF BLOCK	$\overline{\text{EOB}}$	Pulse line from tape unit. Interface cable pin not connected at NRZI tape unit. For PE tape unit, indicates that a data block, tape mark or identification burst has been read. Strobes these signals to tape controller PCA. This pulse is at least two microseconds duration.
TAPE MARK	$\overline{\text{TM}}$	Signal level line from tape unit. Interface cable pin not connected at NRZI tape unit. For PE tape unit, indicates that block just read was tape mark if signal is low. This signal is valid only during the EOB pulse time.
IDENTIFICATION BURST	$\overline{\text{IDB}}$	Signal level line from tape unit. Interface cable pin not connected at NRZI tape unit. For PE tape unit, indicates that block just read from tape was an identification burst block if signal is low. Valid only during EOB pulse time.
MULTIPLE TRACK ERROR	$\overline{\text{MTE}}$	Signal level line from tape unit. Interface cable pin not connected at NRZI tape unit. For PE tape unit, if signal is low, indicates that an uncorrectable error situation was detected and the block must be re-read. Valid only during EOB pulse time.

Table 3-3. Interface-to-Tape Unit Signals (Continued)

NAME	MNEMONIC	DESCRIPTION
STATUS (Cont.)		
SINGLE TRACK ERROR	$\overline{\text{STE}}$	Signal level line from tape unit. Interface cable pin not connected at NRZI tape unit. Used only for PE. If signal is low, indicates single-track error condition was detected. If MTE is not low at EOB time in a read only mode, error condition was correctable. Block need not be re-read. Valid only during EOB pulse time.
<p>NOTES:</p> <ol style="list-style-type: none"> 1. Signals not routed to HP 30115A Magnetic Tape Subsystem from tape unit are not listed. 2. All signals are exchanged between tape controller of HP 30215A Magnetic Tape Unit Interface and selected tape unit. 		

3-12. HP 30215A MAGNETIC TAPE UNIT INTERFACE LOGIC SECTIONS.

3-13. The HP 30215A Magnetic Tape Unit Interface portion of the magnetic tape subsystem, controls and processes all signal and data exchanges between the HP 3000 Computer System and the selected tape unit. The interface is comprised on the tape controller and controller processor printed-circuit-assemblies. The tape controller may be viewed as the data logic portion of the interface, while the controller processor can be viewed as the interface control logic.

3-14. The major logic sections of the tape controller PCA, shown in figure 3-1, are the:

- a. Data gate and bus logic.
- b. Interface, control, and flag logic.
- c. Tape unit interface logic.
- d. Status report logic.
- e. Magnetic tape subsystem microprogram (ROM integrated-circuit packs).

3-15. The major logic sections of the controller processor PCA, shown in figure 3-1, are the:

- a. Register and counter.

- b. Arithmetic and Logic Unit (ALU).
- c. RAR/ROR logic.
- d. Decode and control logic.

3-16. Certain groups of signals are exchanged between the tape controller and controller processor to accomplish subsystem control and data handling. The signal groups, shown in figure 3-1, of the controller processor that are used in the HP 30115A Magnetic Tape Subsystem are the:

- a. Twenty-bit ROM program word bus.
- b. Twelve-bit ROM address word bus.
- c. Sixteen Flag lines to the controller processor.
- d. Five Destination/Source code control lines.
- e. Three strobe lines to the tape controller.
- f. Sixteen-bit bi-directional MIO bus.
- g. Clear line from the tape controller to the controller processor.

3-17. All timing and control for tape motion, reading, and writing operations in the magnetic tape subsystem is under supervision of the subsystem microprogram read out from the subsystem microprogram ROM IC packs. Readout of 20-bit ROM program words to the ROM Output Register (ROR) in the RAR/ROR logic normally occurs sequentially as directed by 12-bit ROM address words applied to the ROM IC packs from the ROM Address Register (RAR) in the RAR/ROR logic. The microprogram branches to appropriate subroutines or addresses, in response to magnetic tape I/O program commands from the HP 3000 Computer System, or sensed conditions on the Flag lines, to accomplish the desired results. Magnetic tape subsystem command words and the formats are explained in section II.

3-18. Figure 3-1 shows that all I/O program commands to the magnetic tape subsystem, and all data transferred through the subsystem is exchanged through the data gate and bus logic, and the interface logic of the interface, control, and flag logic blocks in the tape controller via the 16-bit data and command word buses. Data and commands incoming on the bus are routed to the controller processor registers via the 16-bit bi-directional MIO bus on the controller processor.

3-19. The commands or data are examined or operated on and passed through the registers or counter, see figure 3-1 controller processor portion, and the Arithmetic and Logic Unit (ALU) back to the MIO bus. The bus structure, registers, and ALU in the controller processor are so arranged that the lower or upper byte, or the entire 16 bits of the information may be utilized. Information on the MIO bus may be incoming to the controller processor, or may be output to the tape controller, or may be routed back to the registers or counter for storage, or information may be routed back for further operations to be performed depending upon the microprogram instructions.

3-20. Outgoing data from the HP 3000 Computer System, in the form of 16-bit words, is passed through tape controller PCA logic and unpacked to form two 8-bit bytes to be written on tape. The unpacking operation takes place in the controller processor under direction of the microprogram. Unpacked data is then passed from the controller processor to the tape unit via the upper byte of the 16-bit MIO bus and through the tape controller PCA interfacing logic. Data from the tape unit, inbound to the HP 3000 Computer System, is routed through tape controller and interface logic, via the lower byte of the MIO bus into the controller processor registers. Here two 8-bit frames read from tape are packed into a single 16-bit word in the controller processor registers by operations performed through the Arithmetic and Logic Unit. The 16-bit word is then routed through the ALU to the MIO bus and into tape controller interface logic as a full 16-bit word. This information from magnetic tape is input to the system upon receipt of appropriate commands and strobcs.

3-21 The subsystem status report logic, located on the tape controller PCA holds the coded conditions of appropriate tape unit and tape controller PCA status signals. The 16-bit status word is continuously available for readout on the Data and Command word bus upon command from the HP 3000 Computer System. Format and field explanations of the status word are discussed in section II.

3-22. The operations described in a general nature in preceding paragraphs are all implemented through registers and gates that are controlled by the control logic distributed throughout both HP 30215A Magnetic Tape Unit Interface printed-circuit-assemblies. As previously mentioned, all control logic is activated by the microprogram. Destination/source lines, and strobcs from the controller processor, and additional strobcs and commands from the HP 3000 Computer System, described in table 3-1, are all fed to the tape controller PCA to perform the desired operations. The exact nature and sequence of these "desired operations" is described in the tape controller PCA paragraphs. Generally, on the tape controller PCA, the signals involved in control operations are shown in figure 3-1 as the following lines. (See the tape controller in figure 3-1 and note the sources and destinations of these control signal groups.)

- a. Requests.
- b. Interrupts.
- c. Flags.
- d. Strobcs.
- e. Control signals.
- f. Gating signals.
- g. Readout Control signals.

3-23. The controller processor control logic decodes fields of the ROM program words output from the ROR. Timing of all control functions is under the influence of the crystal oscillator in the decode and control logic section of the controller processor. General groupings of the control signals on the controller processor PCA are shown in figure 3-1 as the following lines. (See the controller processor in figure 3-1 and note the sources and destinations of these control signal groups.)

- a. Register Control signals.
- b. Code bus.
- c. Immediate Operand bus.
- d. Count.
- e. Operation Control signals.

3-24. Once the logic and the signals of the interface are defined, the operation of the entire subsystem can be more easily understood by examining the microprogram. The prerequisite is an understanding of the controller processor microinstruction and word format repertoire, and commands for HP 30115A Magnetic Tape Subsystem control. As previously mentioned, further details on the microprogrammed operation of the subsystem are presented in the following paragraphs.

3-25. INTERFACE.

3-26. The HP 30215A Magnetic Tape Unit Interface is functionally comprised of the tape controller and controller processor printed-circuit-assemblies, and the two flat-ribbon connector cables from J2-to-J2 and from J3-to-J3 on the respective PCA's. The controller processor may be considered a "black-box" that provides "holding" type logic to implement commands and to process data through the tape controller. Flags to the controller processor from the tape controller; and strobes and destination codes to the tape controller from the controller processor cause subsystem operation to be carried out according to the microprogram held in the ROM integrated-circuit packs. The ROM integrated-circuit packs are physically located on the tape controller.

3-27. All logic used in the interface printed-circuit-assemblies is positive-true. The detailed diagrams manual contains information on the integrated-circuit packs, used in the interface, that should be referenced to understand simplified and detailed diagrams for the printed-circuit assemblies. Simplified logic diagrams that support the presentations and tables of tape controller and controller processor operation will be found in the simplified logic diagrams manual. The detailed logic diagrams will be found in the detailed diagrams manual. Logic conventions used in the tape units are described in the tape unit operating and service manuals. The following paragraphs describe the operation of the tape controller and controller processor in relation to the magnetic tape subsystem microprogram.

3-28. TAPE CONTROLLER PCA.

3-29. The functional operation of the magnetic tape subsystem is best described in the flow chart presentation of overall operation in paragraph 3-30. The microprogram for the subsystem resides in the ROM integrated-circuit packs physically present on the tape controller PCA. Flip-flops and registers on the tape controller PCA that are controlled by the microprogram are listed in table 3-3A. Where set and clear information is provided, the logic diagrams should also be referenced for clock signal information and additional source signal data. Accurate movement of tape and read/write gating of information written on or read from tape is the key to successful operation of the magnetic tape subsystem. Timing and tape movement is discussed in paragraphs 3-36 through 3-37. References to information in sections II and IV are made when appropriate.

3-30. **TAPE CONTROLLER MICROPROGRAM.** The overall subsystem operation is described in the general flow charts of figure 3-2. These flow charts, and the detailed flow charts of the listing mentioned later, are applicable for nine-track, 800-cpi (NRZI) and 1600-cpi (PE) tape units. As seen in the flow charts the tape controller is capable of driving a mix of up to four 800-cpi and 1600-cpi tape units.

3-31. Sheet one of the general flow charts shows the overall subsystem operation from the power-on or I/O reset initialization sequence that starts at ROM address 0000_g, through the command word decode sequences. Sheets two through seven show the scan, read forward 800 cpi and 1600 cpi, write forward 800 cpi and 1600 cpi, and read reverse sequences in general form. Sheet eight shows the stop sequence, reject and interrupt sequence, and algorithm to compute the CRCC. Most of the tape controller time is spent in the main (idle) loop. Note that less control from the interface is necessary with 1600-cpi (PE) operation due to the fact that the phase-encoded tape unit exercises more control over the tape than does the NRZI tape unit. Mnemonics for command words shown are defined in section II.

3-32. Detailed Flow Charts. Detailed flow charts of the microprogram discussed above are located in section IV, figure 4-10. Refer to figure 4-9A and table 4-1A for conventions and definitions of terms and symbols used in the detailed flow charts. The detailed flow charts fully describe the microprogram listing, table 4-4, which is discussed in paragraph 3-33. In addition, keep in mind the following when using the detailed flow charts.

- a. The list of flip-flops and registers in table 3-3A should also be used to understand PCA operation.
- b. Specific flip-flop setting or clearing is generally shown in the flow charts by indicating the flip-flop name, stage going to, and mode of that state. For example:

IN/OUT MODE FF ← 0 (OUT)

means that the flip-flop named In/Out Mode is being cleared and in the clear state it is in the "Out" mode.

- c. Controller processor general purpose registers RG0 through RG5, and the counter, are repeatedly assigned as temporary registers to perform particular functions such as: the unit history register, read CRCC register (CRCR), write CRCC register, status report register, character storage register, etc. These register names are effective only for the particular current function, thus, these names do not appear in table 3-3A.

- d. Bits are considered as bit "0" left, reading left (MSB)-to-right (LSB). When a single bit is of interest, for example, it is designated thus: "bit 15."

3-33. Listing. Introductory material for the listing is included in the first seven pages of the listing. The constants shown on page one are octal quantities that may be directly converted to the bit pattern shown in the applicable portion of the 20-bit ROM word. Whether the quantity is loaded into the upper or lower byte must also be considered. The binary quantity is loaded from the immediate operand into the controller processor counter or designated register, as applicable. The actual operation of the counter is to increment but because the sense of the MIO bus is reversed, the overall function of the counter logic is decrementing. Decrementing the counter towards all logical 1's with a quantity stored, provides the desired timing delays. Further information on timing calculation appears in table 4-1A. All logical zero's is the largest number the decrementing counter in the controller processor can hold. Tape controller command word codes are also shown on page one of the listing. The constants shown for the command words are in octal. These may be converted directly to binary to obtain the bit pattern for bits 12 through 15 of the IOAW, which carries the tape controller command word. For example: the Command RST is #11 thus bits 12 through 15 of the IOAW will be 1001. In the listing, quantities preceded by the number symbol (#) are octal quantities. Tape controller command words are all explained in section II of this manual along with their binary patterns. The Reference Coding Sheet for the controller processor shown on page two of the listing is included for reference only. Use the controller processor microcoding sheet, figure 4-11, and word format figure 3-13 included in the controller processor PCA description for complete information. Pages three through five of the listing provide reference tables for tape controller card pins and signals of jacks J1 through J3. Note that J2-36 (ROM Enable) and J3-49 (Run) are used only for maintenance. The Run signal is not used at all in the nine-track magnetic tape subsystem. Additional data, cabling, and maintenance information is included in section IV of this manual.

3-34. The destination and source codes shown on page six of the listing are octal numbers that may be converted to binary to obtain the bit pattern on the destination/source lines (ROR7 through 11). The code from the controller processor to the tape controller is valid at output or input strobe time. Consider, for example, a destination code of D03 for output. The bit pattern for ROR 7:11 presented at the destination/source decoder in the tape controller will be "00011," respectively. At output strobe time this will be decoded to gate the write register. The destination/source codes are used in IOC and OTI instructions. To easily find which registers, gates, and/or flip-flops are activated at the appropriate strobe time, refer to the coding sheet on page seven of the listing and to table 3-3A. The detailed logic diagrams must be used to locate the wiring and logic activated.

Table 3-3A. Magnetic Tape Controller PCA Flip-Flops and Registers

NAME	REFERENCE DESIGNATION	DESCRIPTION
FLIP-FLOPS		
BYTE CNT (Byte Count)	U161B	Status report logic JK FF. Provides tape odd/even byte count in bit 1 of subsystem status word. Set by MIO bus bit M9 for odd bytes. Cleared by MIO bus bit M8 for even bytes.
CMD ENB (Command Enable)	U94B	Flag logic JK FF. Provides flag signal F17 to microprogram. Flag low indicates programmed I/O order has been received (FF set). "Set CMD ENB FF" in microprogram indicates flag is high (FF cleared). Set by \overline{P} CONT STB from MUX CHAN. Cleared by D1x (ROR bit 8) and UOS or LOS.
Data FF	U84A	Flag logic JK FF. Provides flag signal F14 to microprogram. Flag high indicates data taken by system or provided to the subsystem. Set by \overline{P} READ STB or \overline{P} WRIT STB from MUX CHAN. Cleared by MIO bus bit M0 and UOS.
DEV END (Device End)	U182A	Bus logic interface logic JK FF. Provides Device End (\overline{DEV} END) Signal to MUX CHAN. Clear state is active state. Set by Acknowledge Service Request or Clear Interface Logic, or Master Reset signals. Cleared by MIO bus bit M4 and DO2 (ROR bit 10), and UOS.
DEV END (B) (Device End Buffer)	U16 B/C	Control logic gate FF. Provides signal to gate device address to IOD bus at end of SIO operation. Set by Device End (DEV END) signal from DEV END FF. Cleared by MUX CHAN signals.
DSR (Device Service Request)	U74B	Bus logic interface logic JK FF. Provides signal to issue Service Request to MUX CHAN for additional commands. Set by D2x (ROR 7) and either output strobe (UOS or LOS). Cleared by Acknowledge Service Request, or Clear Interface Logic, or Master Reset signals.

Table 3-3A. Magnetic Tape Controller PCA Flip-Flops and Registers (Continued)

NAME	REFERENCE DESIGNATION	DESCRIPTION
FLIP-FLOPS (Cont.)		
EOB FLAG FF (End of Block Flag)	U83B	Flag logic D FF. Provides flag signal F07 to microprogram. Flag high indicates 1600 cpi tape unit has sent End of Block (\overline{EOB}) signal. Set by EOB O.S. (one shot). Cleared by D1x (ROR bit 8) and UOS or LOS.
EOF (End of File)	U161A	Status report logic JK FF. Provides Tape Mark, bit 11, of subsystem status word. Set by MIO bus bit M10 to indicate tape mark found. Cleared by MIO bus bit M15.
ESR (Enable Service Request)	U26B	Request logic D FF. Flip-flop used to initiate Service Request to MUX CHAN. Set by decoded SIO command. Cleared by Clear Interface Logic (\overline{CLRIL}) signal.
FWD (Forward)	U142B	Tape unit control interface logic JK FF. Sends Forward (\overline{CF}) command to selected tape unit. Set by MIO bus bit M10. Cleared by MIO bus bit M9.
F0 (Flag Zero)	U182B	Flag logic JK FF. Provides flag signal F00 to microprogram. Used in microprogram as a memory element. Set by MIO bus bit M2. Cleared by MIO bus bit M3.
F1 (Flag One)	U162A	Flag logic JK FF. Provides flag signal F01 to microprogram. Used in microprogram as a memory element. Set by MIO bus bit M11. Cleared by MIO bus bit M10.
F2 (Flag Two)	U162B	Flag logic JK FF. Provides flag signal F02 to microprogram. Used in microprogram as a memory element. Set by MIO bus bit M9. Cleared by MIO bus bit M8.
In-Out	U172A	PCA control logic JK FF. Provides control signal for in or out parity reading and 1600 cpi tape unit status signal reading. Set by MIO bus bit M15 for in mode. Cleared by MIO bus bit M14 for out mode.

Table 3-3A. Magnetic Tape Controller PCA Flip-Flops and Registers (Continued)

NAME	REFERENCE DESIGNATION	DESCRIPTION
FLIP-FLOPS (Cont.)		
INT ACT (Interrupt Active)	U55A	Interrupt logic D FF. Provides Interrupt Active ($\overline{\text{INT ACK}}$) signal to IOP and PCA interrupt logic when interrupt pending. Set by controller requesting interrupt. Cleared by decoded Reset Interrupt Logic ($\overline{\text{RIL}}$) command (4).
Interrupt Request	U114A	Bus logic interface logic D FF. Provides Interrupt Request, bit 2, of subsystem status word and Interrupt Request ($\overline{\text{INT REQ}}$) signal to interrupt logic, and Interrupt, bit 3, for internal status word. Set by high signal from error status decoder (when any error condition occurs) and clocked by destination code D02, UOS, and MIO bus bit M7 or set by decoded Set Interrupt ($\overline{\text{SET INT}}$) command. Cleared by Reset Interrupt ($\overline{\text{RESET INT}}$) signal or Master Reset.
INT LATCH (Interrupt Latch)	U24D	Interrupt logic D FF. Stops Interrupt Poll and provides device address gating signal when set by Interrupt Active or Interrupt Request signals. Cleared by reverse of above conditions.
IN-XFER (In Transfer)	U86B	Flag logic JK FF. Provides flag signal F16 to microprogram. Flag high indicates system taking data from subsystem. Toggled by In Transfer signal from MUX CHAN and clocked by IOP and MUX CHAN. Cleared by Master Reset or Clear Interface Logic signals.
Mask	U55B	Interrupt logic D FF. Allows subsystem to respond or not respond to interrupts depending upon mask word from IOP. Set by proper bit connected through mask jumper and clocked by Set Mask from IOP. Cleared by Master Reset or Programmed Master Clear.
Odd/Even Parity	U152A	Tape unit write interface logic JK FF. Causes write parity generator to provide odd or even parity for write operation. Set by MIO bus bit M15 for odd parity. Cleared by MIO bus bit M14 for even parity.

Table 3-3A. Magnetic Tape Controller PCA Flip-Flops and Registers (Continued)

NAME	REFERENCE DESIGNATION	DESCRIPTION
FLIP-FLOPS (Cont.)		
Off-Line	U153B	Tape unit control interface logic JK FF. Sends Off-Line (\overline{CL}) command to selected tape unit when set. Set by MIO bus bit M6. Cleared by MIO bus bit M7.
OUT-XFER (Out Transfer)	U86A	Flag logic JK FF. Provides flag signal F12 to microprogram. Flag high indicates system sending data to subsystem. Toggled by Out Transfer signal from MUX CHAN and clocked by IOP and MUX CHAN. Cleared by Master Reset or Clear Interface Logic signals.
PAR ENB (Parity Enable)	U172B	Tape unit control interface logic JK FF. Enables parity to be written when set. Provides constant "0" in parity track when clear. Set by MIO bus bit M13 to enable parity (odd parity). Cleared by MIO bus bit M12 to suppress parity.
PAR ERR (Parity Error)	U83A	Flag logic D FF. Provides flag signal F11 to microprogram. Flag low indicates bad read parity. Set by read parity checker and clocked by read clock one shot. Cleared by Master Reset signal.
RD CLK FLAG (Read Clock Flag)	U84B	Flag logic JK FF. Provides flag signal F10 to microprogram. Flag high indicates read clock received from tape unit. Clocked to set by read clock one shot. Cleared by D04, $\overline{D03}$ and UOS or LOS.
RD PARITY (Read Parity)	U114B	Tape unit read interface logic D FF. Used to store the state of the read parity bit for use by flag F06. Clocked by Read Clock one shot.
Reject	U181A	Status report logic JK FF. Provides reject command status data to error status decoder for status error field bits 12, 13, 14 of subsystem status word. Set by MIO bus bit M14. Cleared by MIO bus bit M15.

Table 3-3A. Magnetic Tape Controller PCA Flip-Flops and Registers (Continued)

NAME	REFERENCE DESIGNATION	DESCRIPTION
FLIP-FLOPS (Cont.)		
REV (Reverse)	U142A	Tape unit control interface logic JK FF. Sends Reverse (\overline{CR}) command to selected tape unit. Set by MIO bus bit M11. Cleared by MIO bus bit M9.
REW (Rewind)	U153A	Tape unit control interface logic JK FF. Sends Rewind (\overline{CRW}) command to selected tape unit. Set by MIO bus bit M5. Cleared by MIO bus bit M7.
SIO OK	U96B	Service logic JK FF. Indicates SIO operation state. Set by decoded SIO direct command. Cleared by clear Interface Logic or Master Reset signals. Toggled by MUX CHAN Toggle SIO OK signal.
SR (B) (Service Request Buffer)	U26A	Service logic D FF. Indicates to controller logic that service request has been sent to MUX CHAN. Clocked by card control logic. Cleared by Programmed Master Clear or I/O Reset signals.
SR (Service Request)	U96A	Request logic JK FF. Initiates controller service request after receipt of SIO direct command. Set by decoded SIO direct command. Toggled by Toggle SR signal from MUX CHAN and clocked by card control logic. Cleared by Clear Interface Logic or Master Reset signals.
Tape Error	U171B	Status report logic JK FF. Provides tape error status data to error status decoder for status error field bits 12, 13, 14 of subsystem status word. Set by MIO bus bit M11. Cleared by MIO bus bit M15.
Tape Runaway	U181B	Status report logic JK FF. Provides tape runaway status data to error status decoder for status error field bits 12, 13, 14 of subsystem status word. Set by MIO bus bit M13. Cleared by MIO bus bit M15.

Table 3-3A. Magnetic Tape Controller PCA Flip-Flops and Registers (Continued)

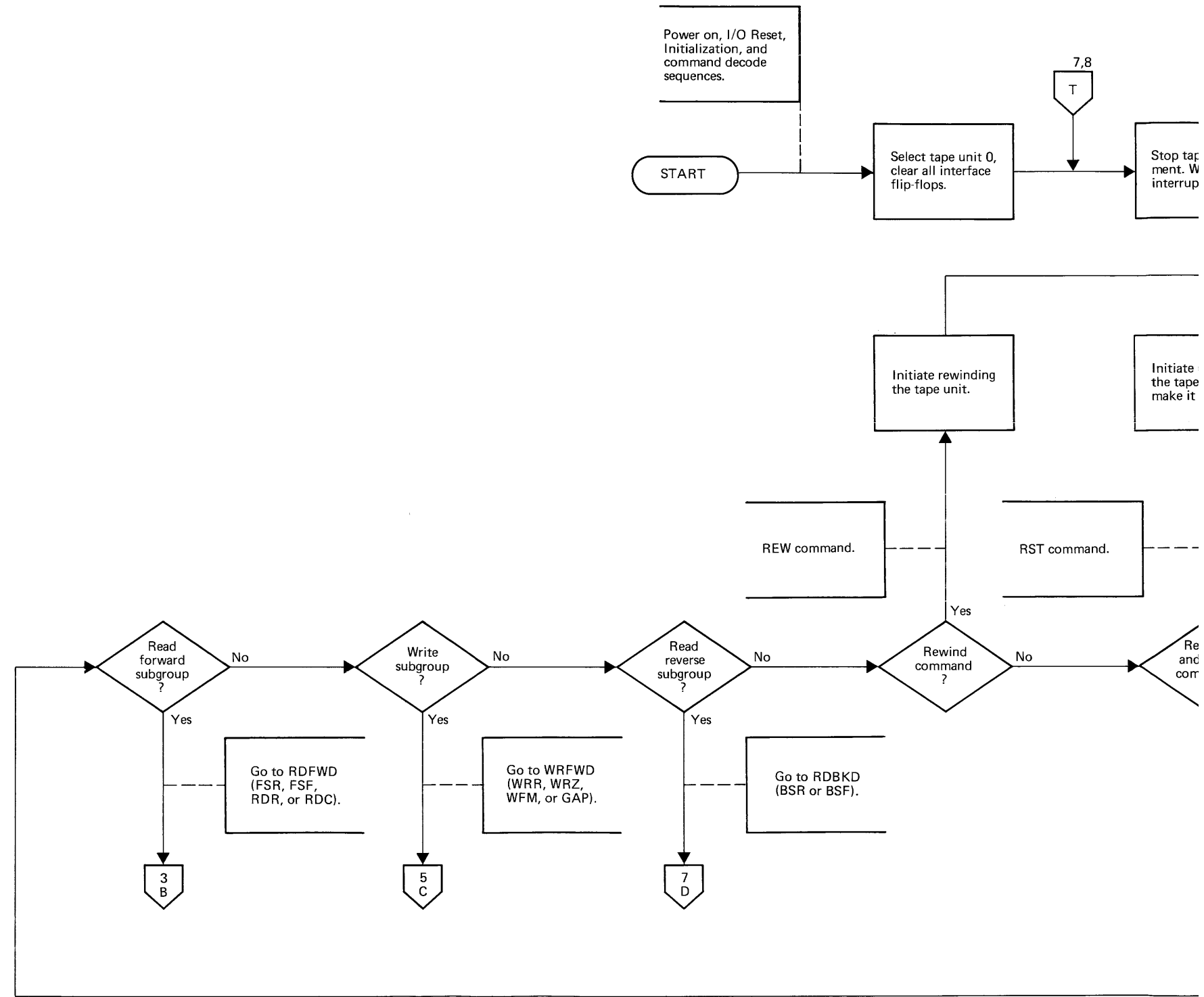
NAME	REFERENCE DESIGNATION	DESCRIPTION
FLIP-FLOPS (Cont.)		
Timing	U171A	Status report logic JK FF. Provides timing status data to error status decoder for status error field bits 12, 13, 14 of subsystem status word. Set by MIO bus bit M12. Cleared by MIO bus bit M15.
UNIT INT (Unit Interrupt)	U173A	Status report logic JK FF. Provides unit ready status to error status decoder for status error field bits 12, 13, 14 of subsystem status word. Set by MIO bus bit M1. Cleared by MIO bus bit M5.
UNIT SEL 1 (Unit Select One)	U151B	Unit select logic JK FF. Provides unit select internal status data, select decoder data, and unit select status bit 4 of subsystem status word. Set by MIO bus bit M6. Cleared by MIO bus bit M4.
UNIT SEL 2 (Unit Select Two)	U151A	Unit select logic JK FF. Provides unit select internal status data, select decoder data, and unit select status bit 3 of subsystem status word. Set by MIO bus bit M7. Cleared by MIO bus bit M5.
Write	U152B	Tape unit control interface logic JK FF. Sends Write (\overline{WSW}) command to selected tape unit. Set by MIO bus bit M13. Cleared by MIO bus bit M12.
XFER ERROR (Transfer Error)	U74A	Status report logic JK FF. Provides transfer error status data to error status decoder for status error field bits 12, 13, 14 of subsystem status word and signal to clear interrupt logic. Set by Transfer Error signal from MUX CHAN and clocked by Clock Transfer Error signal. Cleared by Master Reset signal.

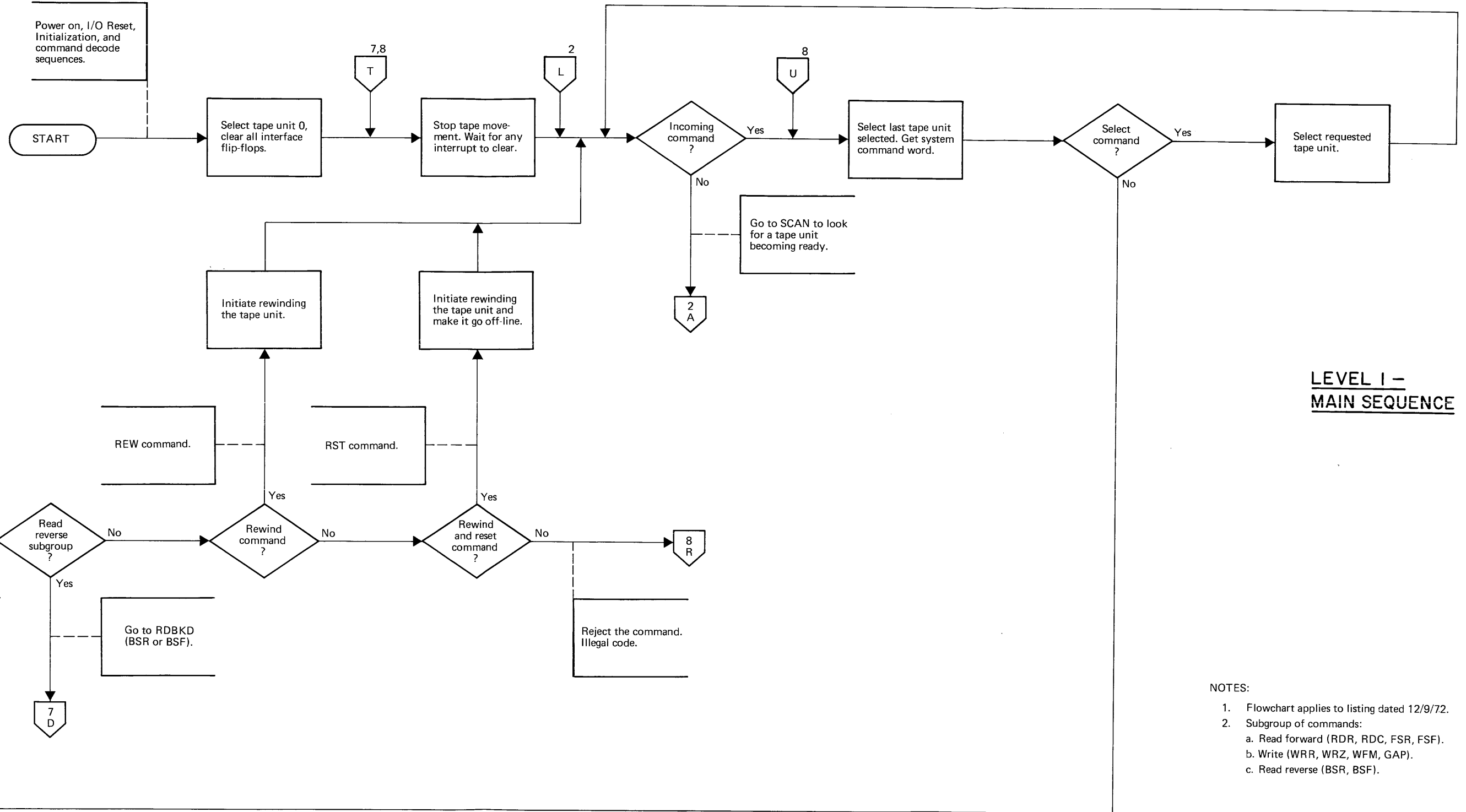
Table 3-3A. Magnetic Tape Controller PCA Flip-Flops and Registers (Continued)

NAME	REFERENCE DESIGNATION	DESCRIPTION
ONE-SHOTS (O.S.)		
EOB (End of Block)	U22A	Tape unit status interface logic one shot. Provides 1.25 microsecond pulse to clock EOB FLAG FF for flag F07 and clocks 1600 cpi Status Latch Register. Triggered by $\overline{\text{EOB}}$ signal from 1600 cpi tape unit.
RD CLK (Read Clock)	U22B	Tape unit read interface logic one shot. Provides 1.25 microsecond pulse to clock RD PARITY FF then PAR ERR FF and Read Data Register. Triggered by $\overline{\text{RD CLK}}$ signal from selected tape unit.
WRT CLK (Write Clock)	U143A	Tape unit write interface logic one shot. Provides 2.58 microsecond $\overline{\text{WC}}$ pulse to selected tape unit. Triggered by MIO bus bit M2, D00, and UOS.
WRT RESET (Write Reset)	U143B	Tape unit write interface logic one shot. Provides 2.58 microsecond $\overline{\text{WRS}}$ pulse to selected tape unit. Triggered by MIO bus bit M3, D00, and UOS.
REGISTERS		
AUX Status (Auxiliary Status)	U13	<p>Processor interface logic inverting gates acting as internal status register. Provides microprogram status on upper byte MIO bus bits as follows:</p> <p>M0 $\overline{\text{IDB}}$ (1600 cpi tape unit). M1 $\overline{\text{TM}}$ (1600 cpi tape unit). M2 $\overline{\text{MTE}}$ or $\overline{\text{STE}}$ (1600 cpi tape unit). M3 INT ACTIVE or Interrupt Request. M4 $\overline{\text{SIO OK}}$. M5 $\overline{\text{SFP}}$ (from tape unit). M6 and M7 (Tied low).</p> <p>Note: See Status Latch Register also for M0, M1, M2. Gated to bus by source codes D22 or D26 (ROR bits 10 and 7) and Input Strobe (INP STB).</p>

Table 3-3A. Magnetic Tape Controller PCA Flip-Flops and Registers (Continued)

NAME	REFERENCE DESIGNATION	DESCRIPTION
REGISTERS (Cont.)		
Data In	U184 U186	Processor interface logic upper (U186), lower (U184) byte latch registers. Hold 16-bit data word for input to system. Data latched in by D07 and UOS/LOS.
Data Out	U135 U165	Bus logic interface logic upper (U135), lower (U165) byte latch registers. Holds data and command words output from system. Data latched in by \overline{P} CONT STB or \overline{P} WRIT STB.
Read Data	U21	Tape unit read interface logic latch register. Holds eight bit byte received from tape unit read data lines. Byte latched in by Read Clock and one shot output.
Status Latch	U24	Tape unit status interface logic latch register. Holds 1600 cpi tape unit status for output to AUX status gates. Status latched in by pulse from EOB one shot.
Status	U166 U167	Status report logic gates that act as system status word register. See section II for status word bit and field definitions. Status gated by \overline{P} STAT STB or \overline{D} STAT STB signals.
Unit Status	U33	Processor interface logic gates that act as internal unit select status register. Status gated to MIO bus by D20 or D24 source code.
Write Data	U53	Tape unit write interface logic latch register. Holds eight bit byte to be sent to selected tape unit for writing on tape. Byte latched in by destination code D03.

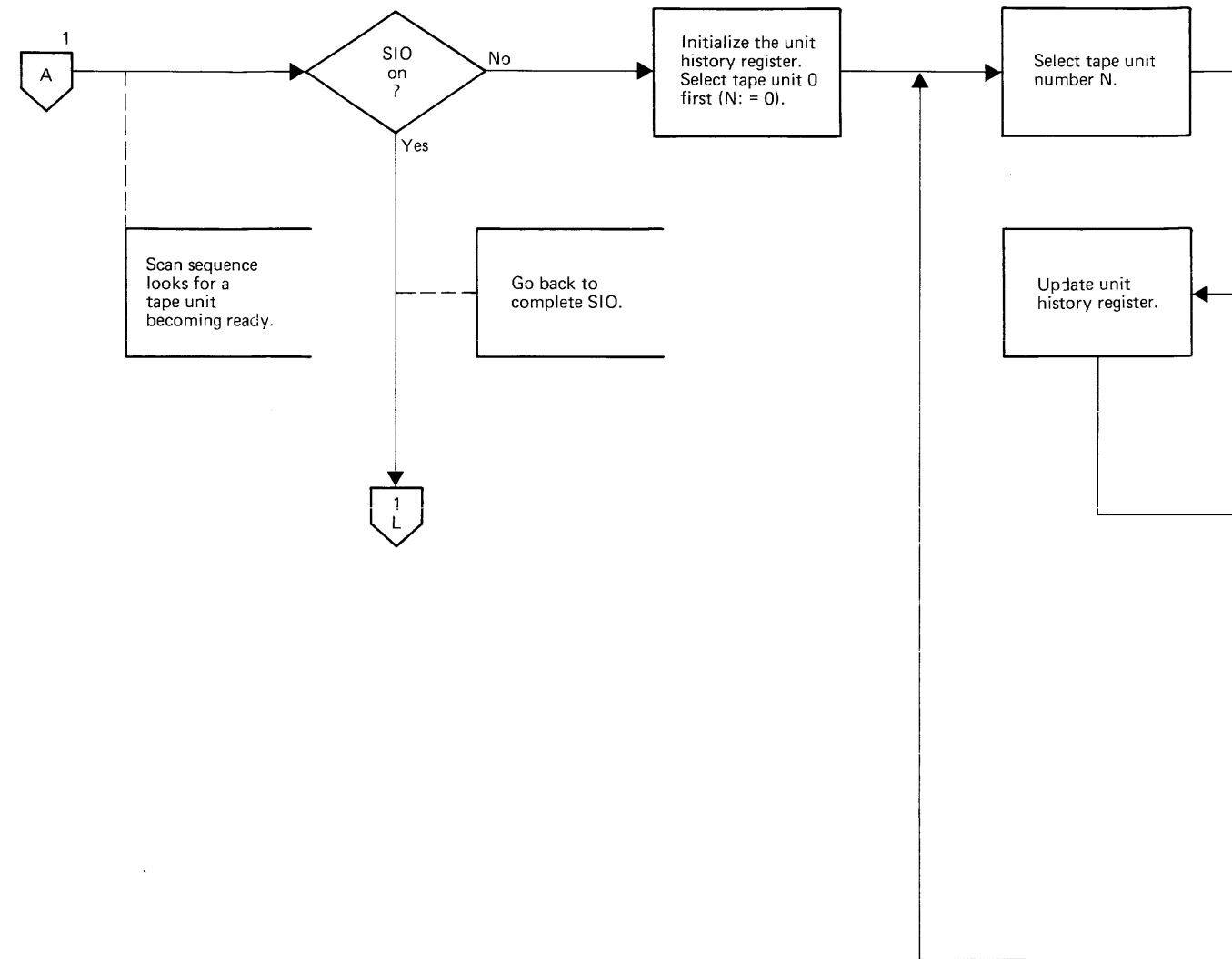


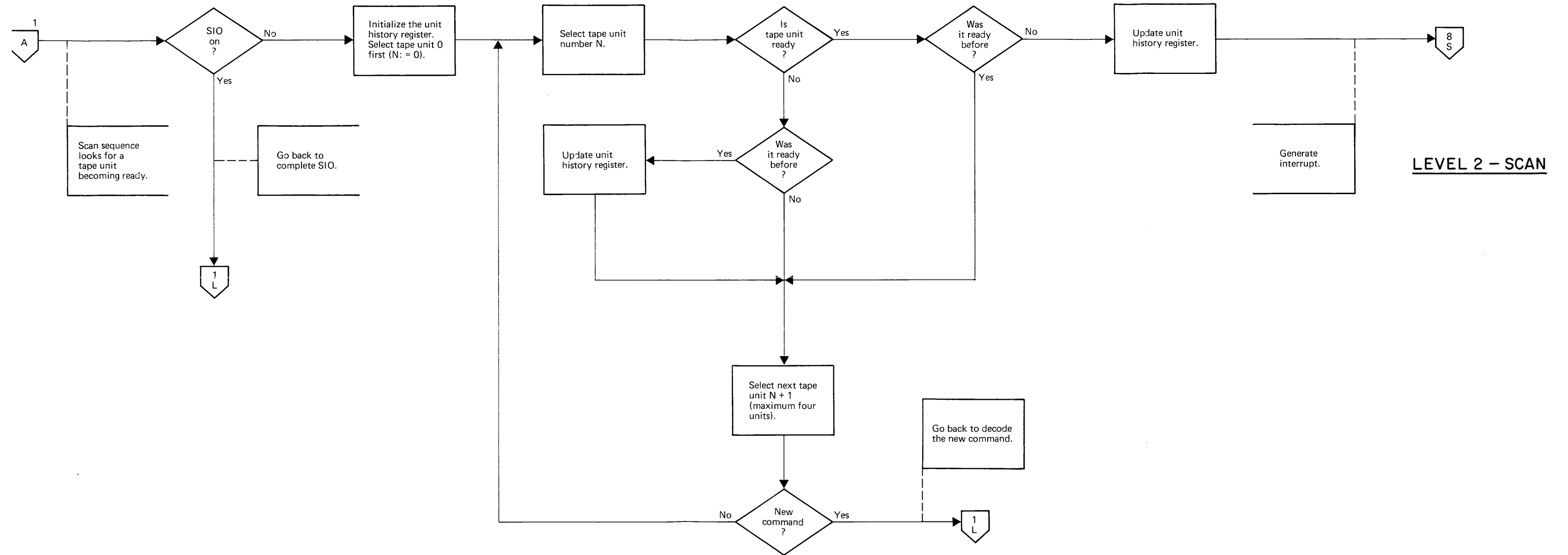


**LEVEL I –
MAIN SEQUENCE**

- NOTES:
1. Flowchart applies to listing dated 12/9/72.
 2. Subgroup of commands:
 - a. Read forward (RDR, RDC, FSR, FSF).
 - b. Write (WRR, WRZ, WFM, GAP).
 - c. Read reverse (BSR, BSF).

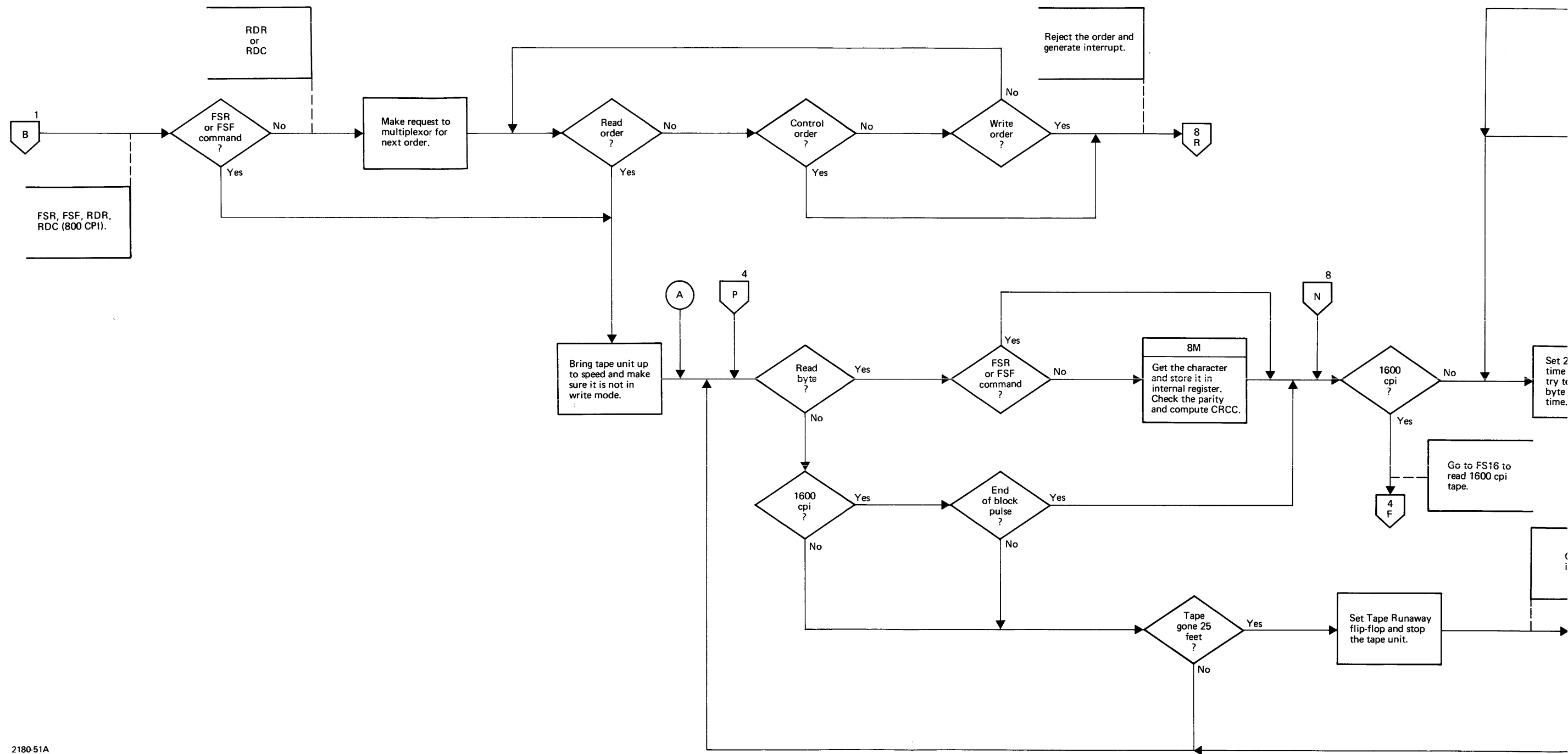
Figure 3-2. Tape Controller Overall Operation Flowchart (Sheet 1 of 8)

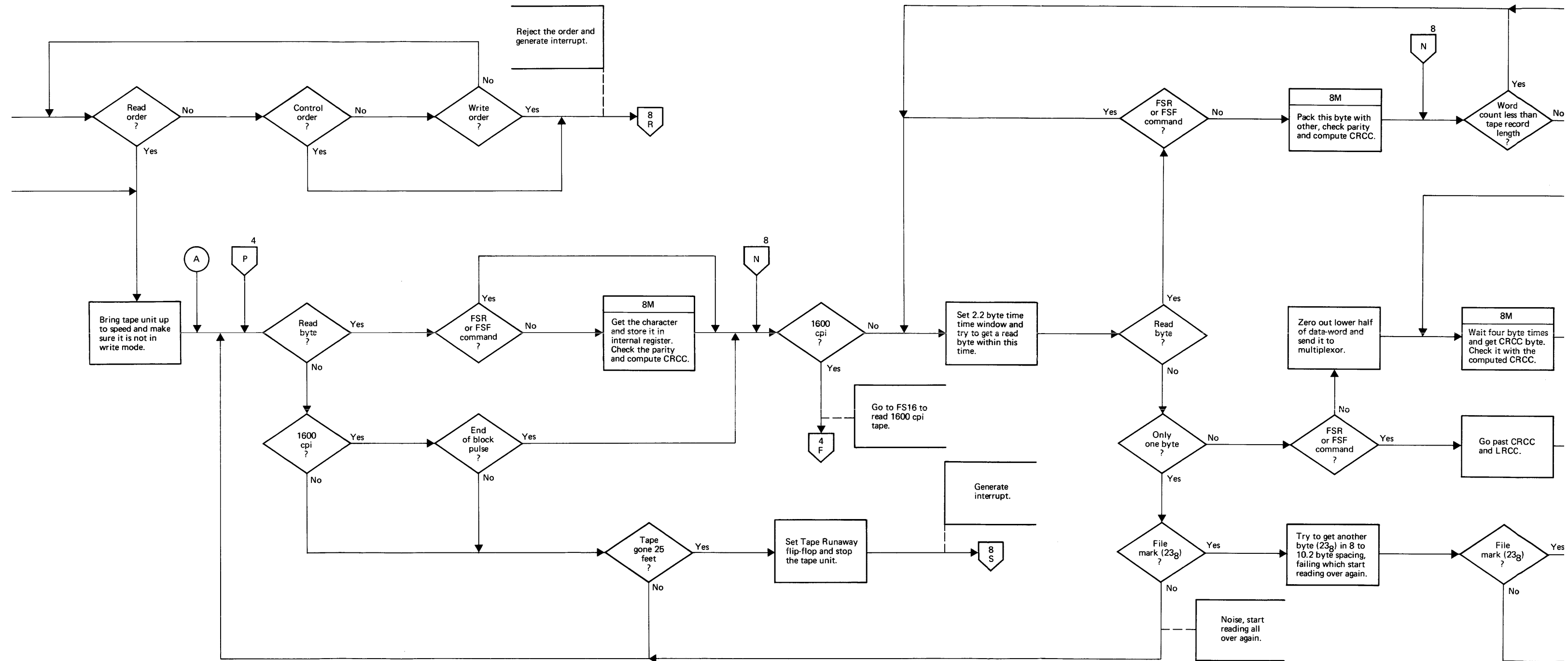




2180-50A

Figure 3-2. Tape Controller Overall Operation Flowchart (Sheet 2 of 8)





LEVEL 2 – READ FORWARD (RDFWD) 800 CPI

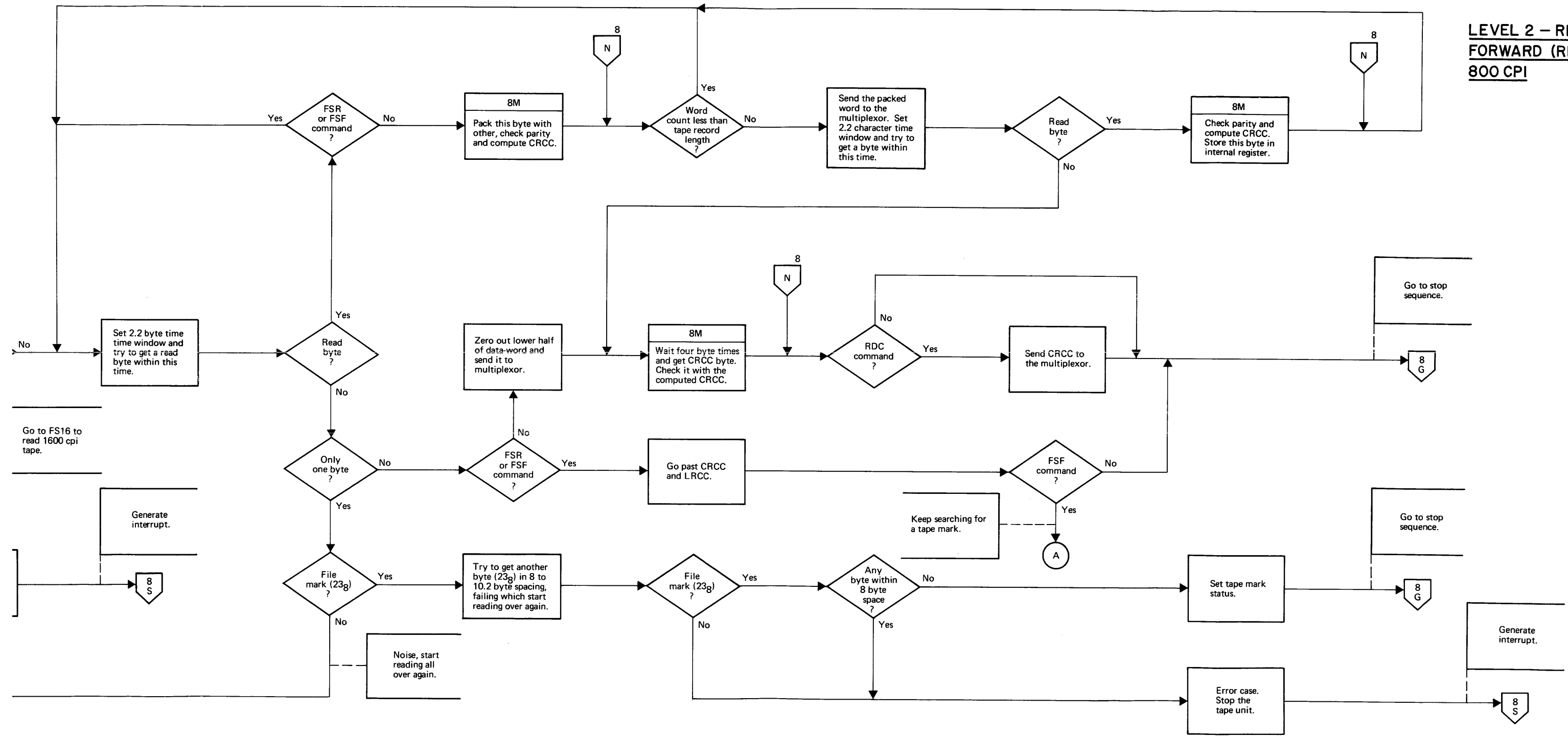
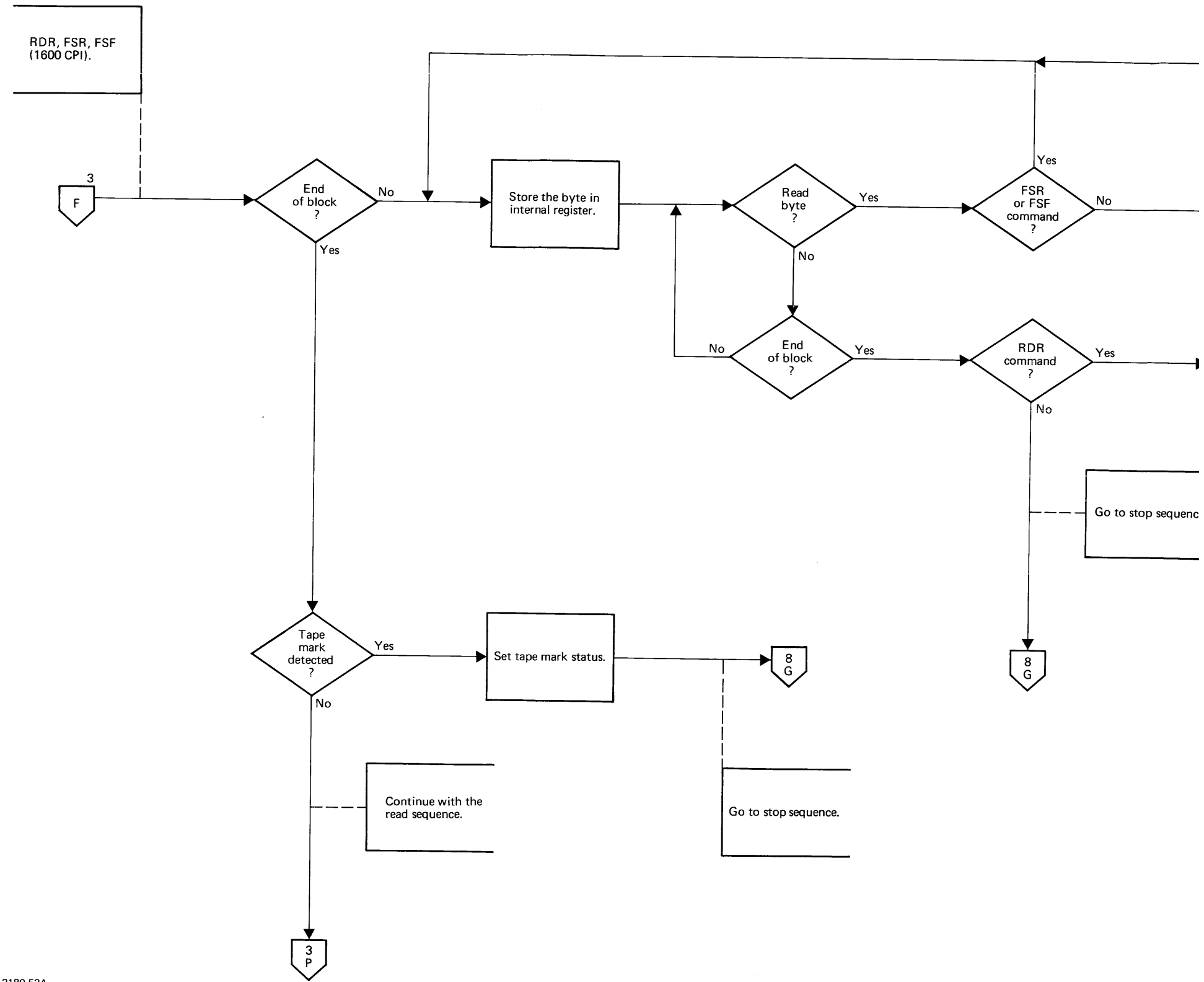


Figure 3-2. Tape Controller Overall Operation Flowchart (Sheet 3 of 8)



LEVEL 2—FS16.
READ FORWARD
1600 CPI.

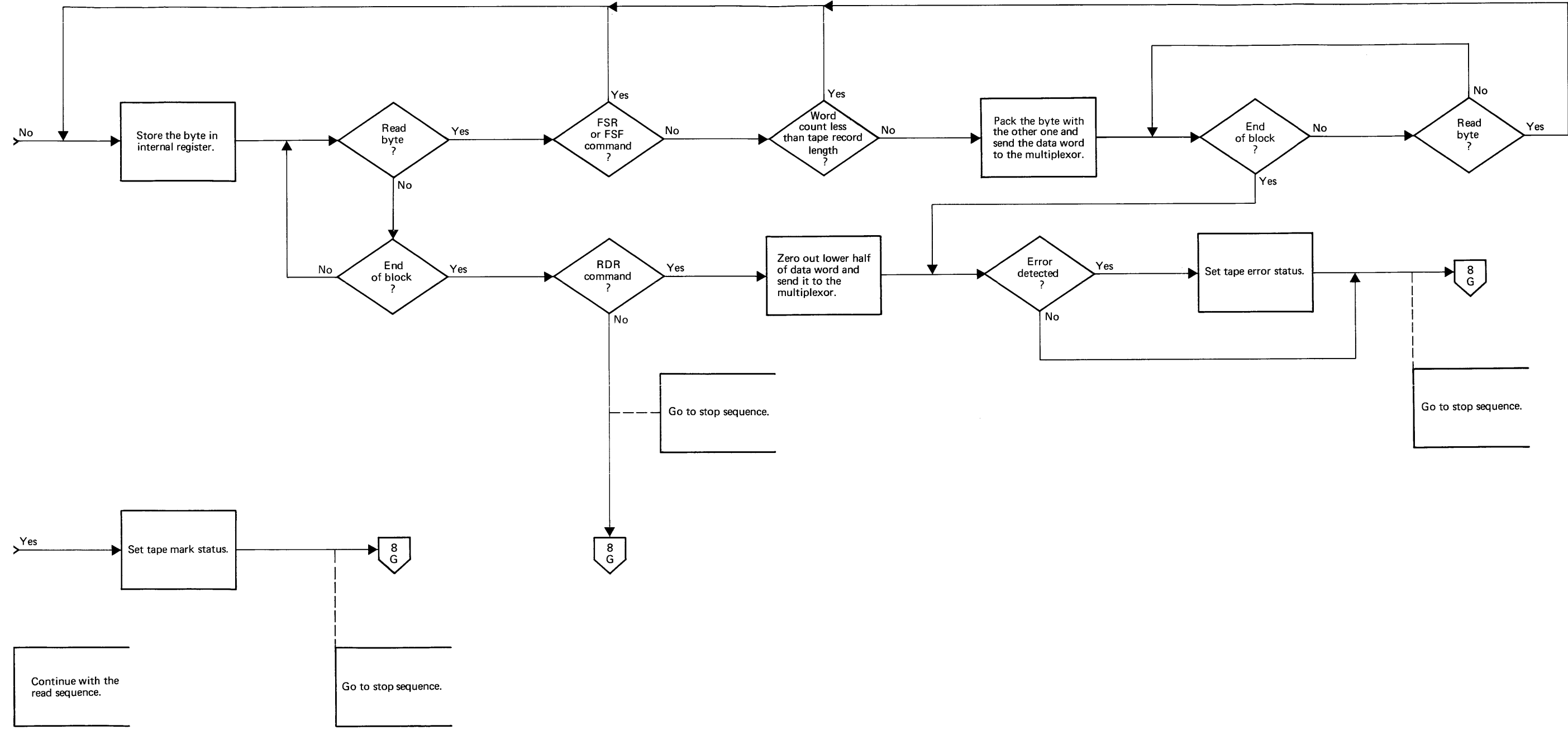
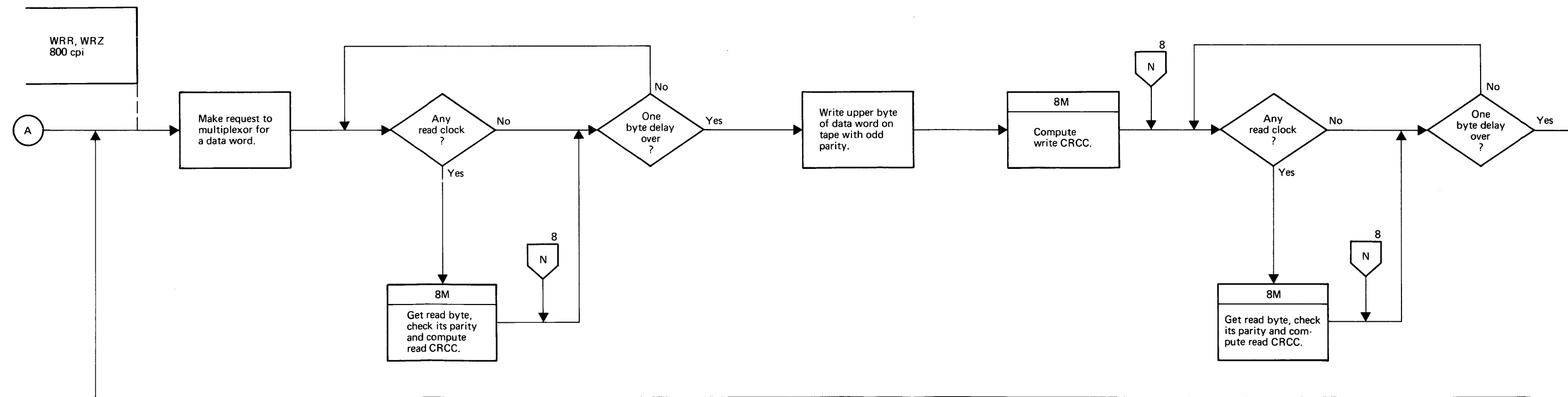
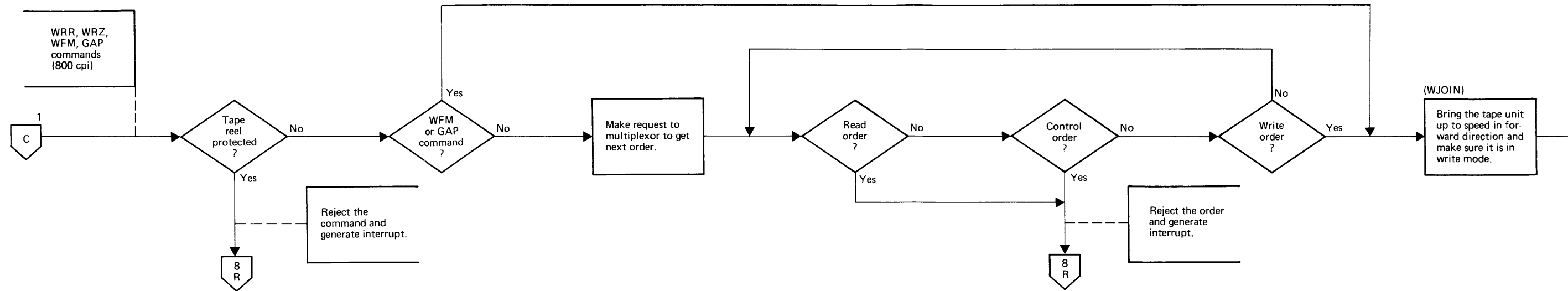
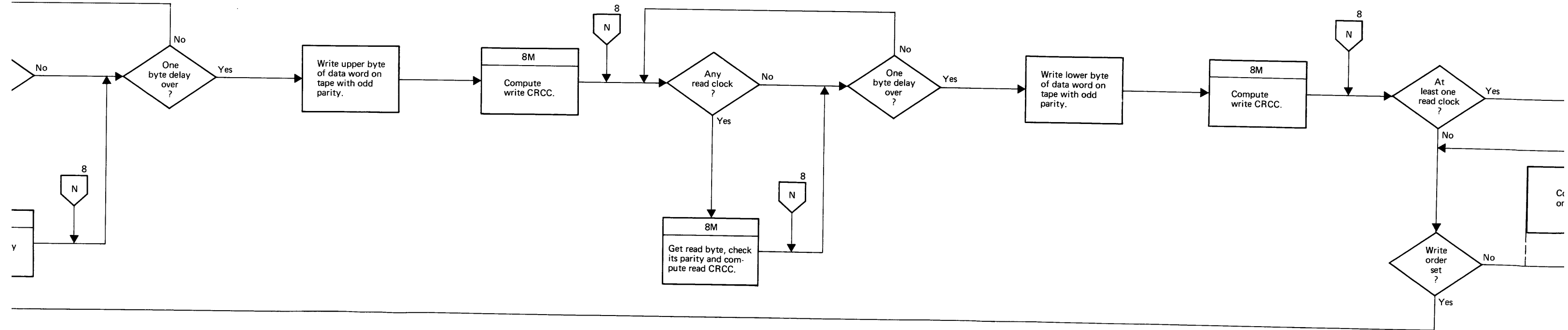
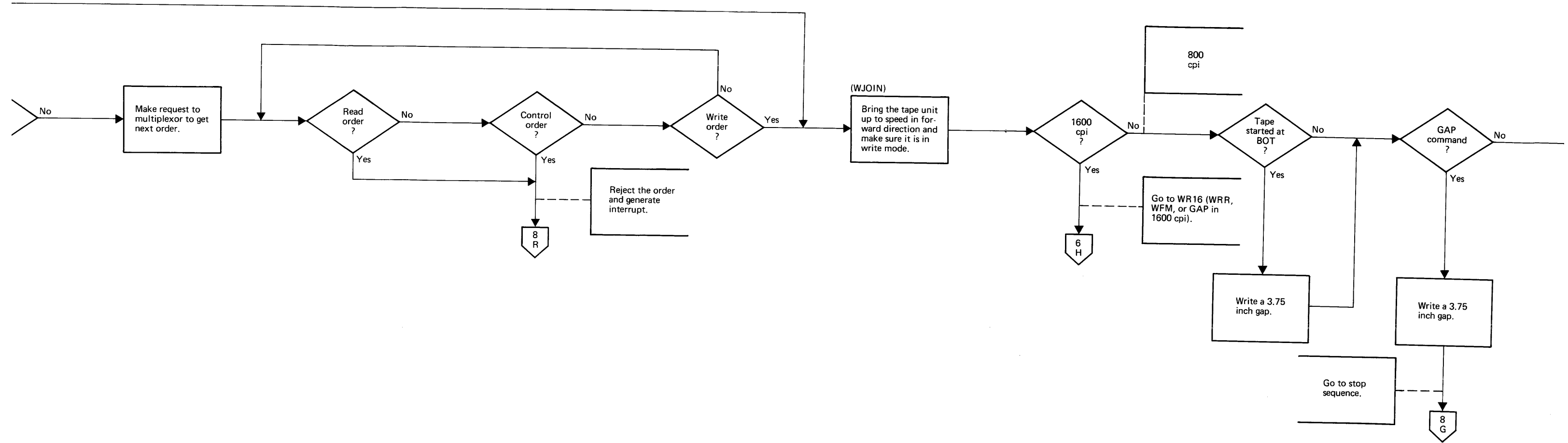


Figure 3-2. Tape Controller Overall Operation Flowchart (Sheet 4 of 8)





LEVEL 2 – WRITE FORWARD (WRFWD) 800 CPI

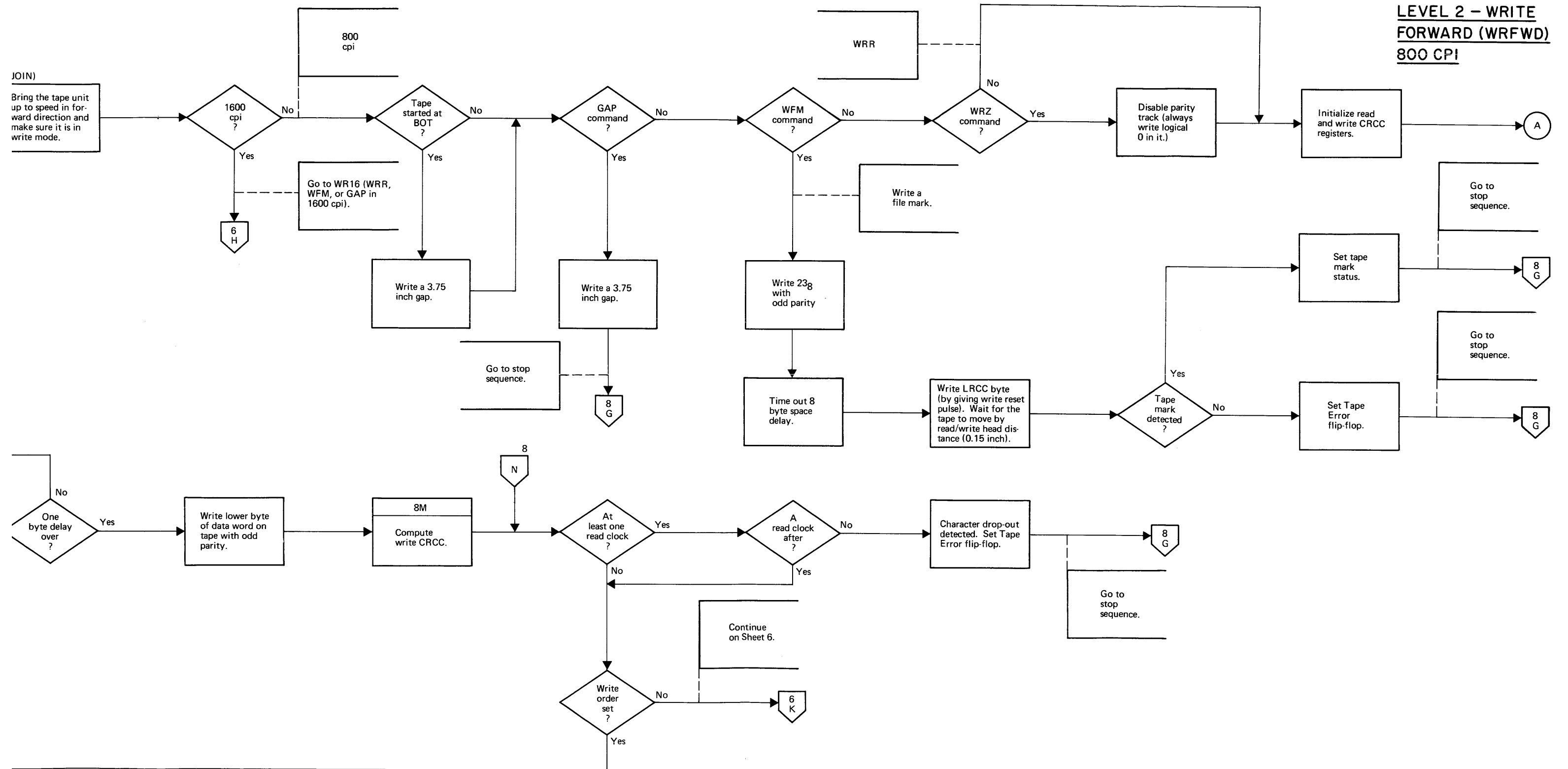
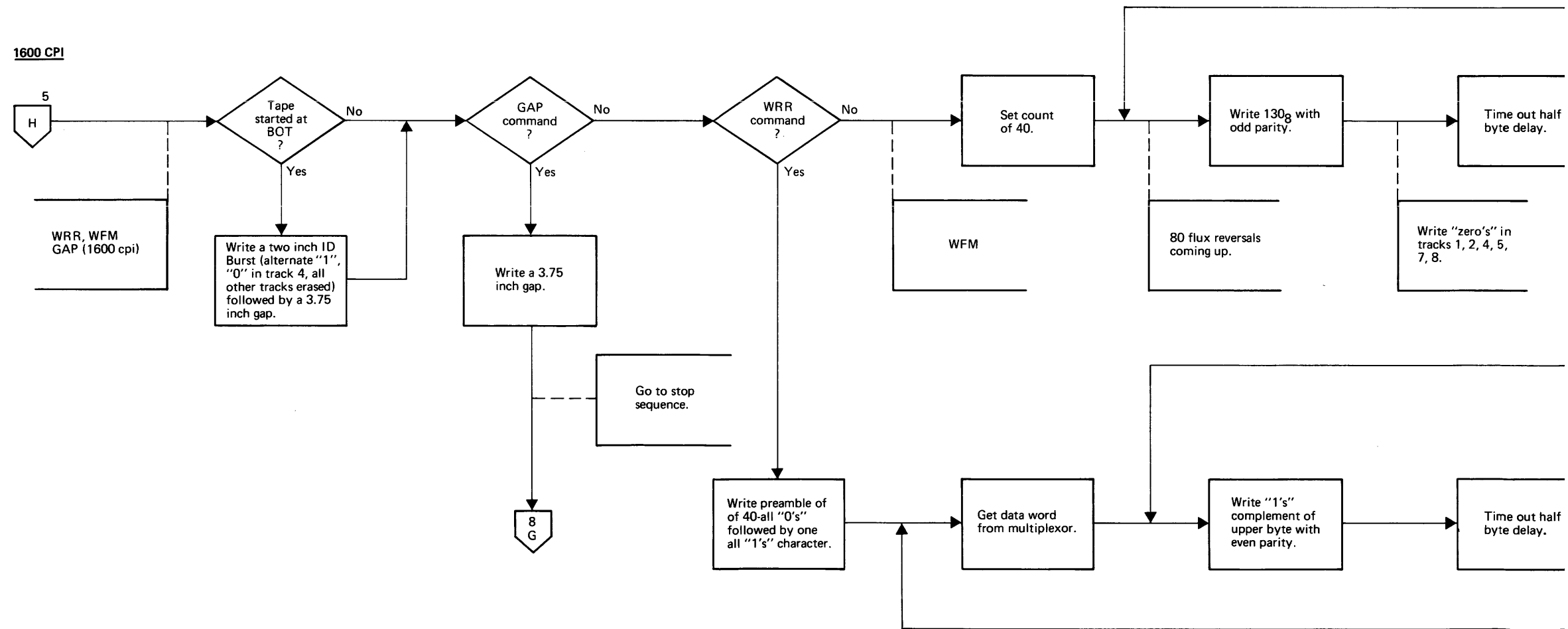
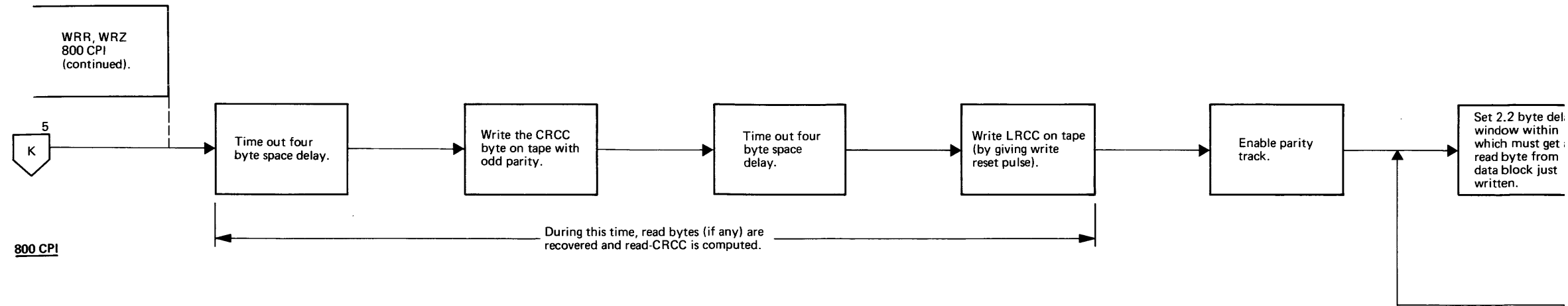
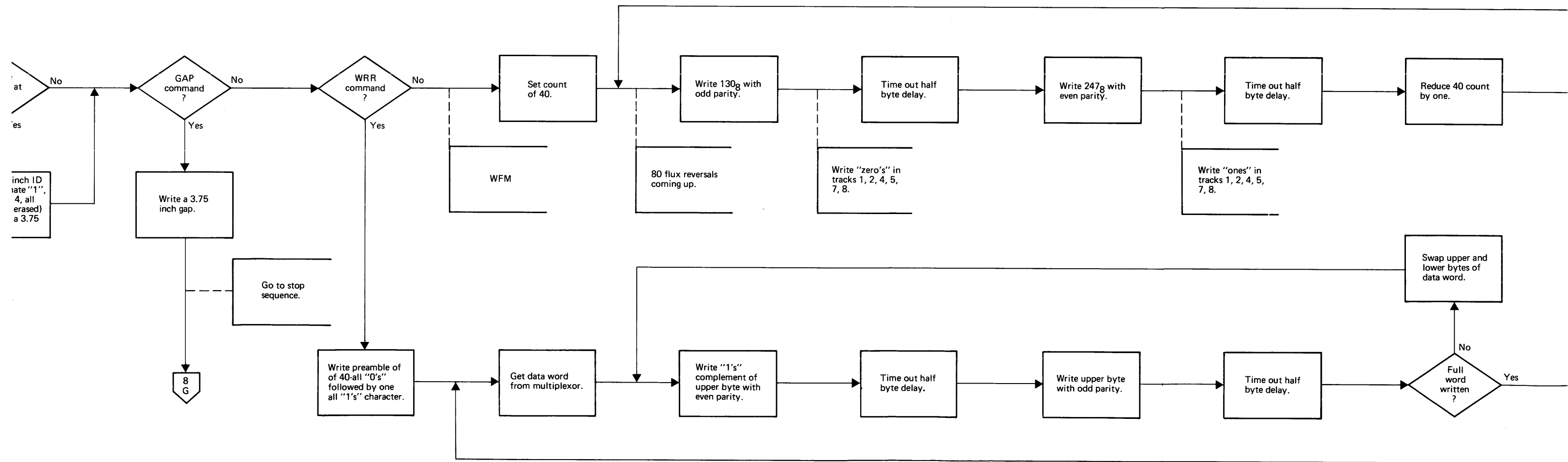
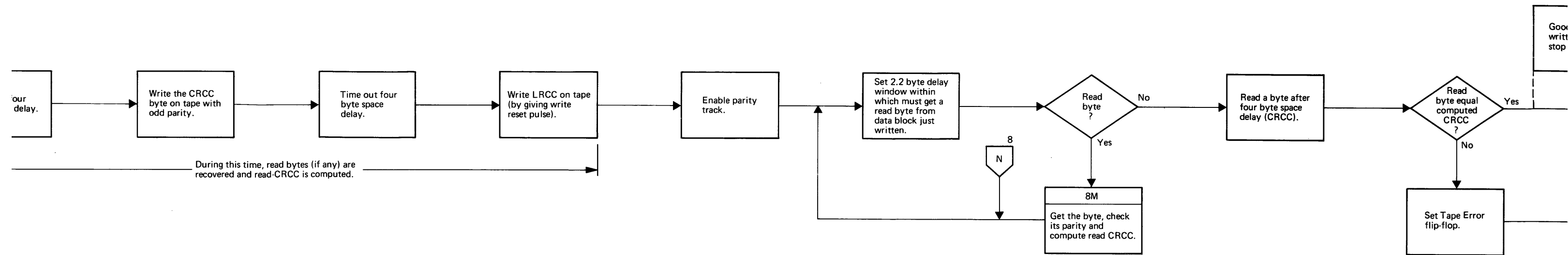
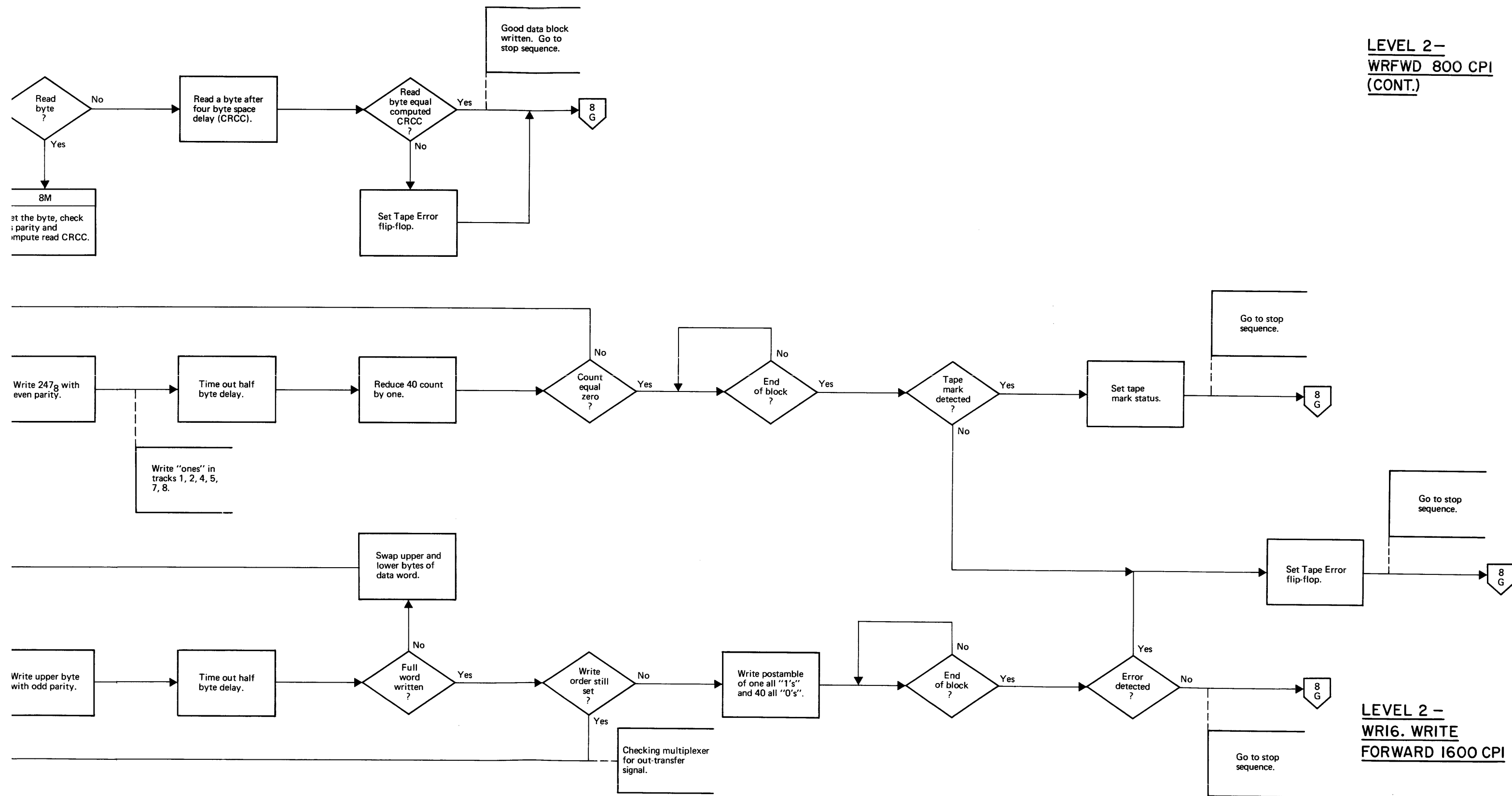


Figure 3-2. Tape Controller Overall Operation Flowchart (Sheet 5 of 8)



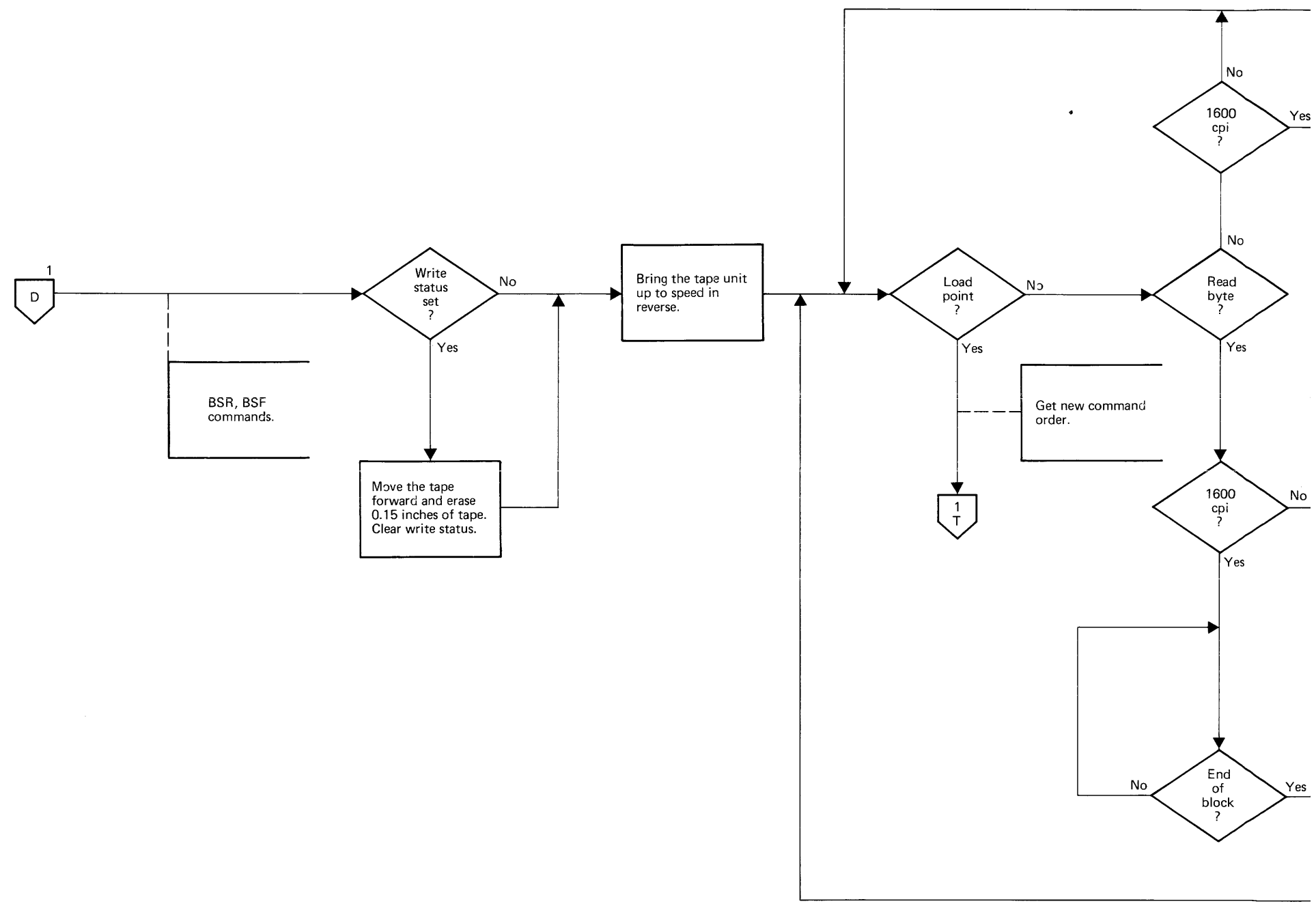


LEVEL 2 -
WRFWD 800 CPI
(CONT.)



LEVEL 2 -
WR16. WRITE
FORWARD 1600 CPI

Figure 3-2. Tape Controller Overall Operation Flowchart (Sheet 6 of 8)



**LEVEL 2 – READ
REVERSE (RDBKD)**

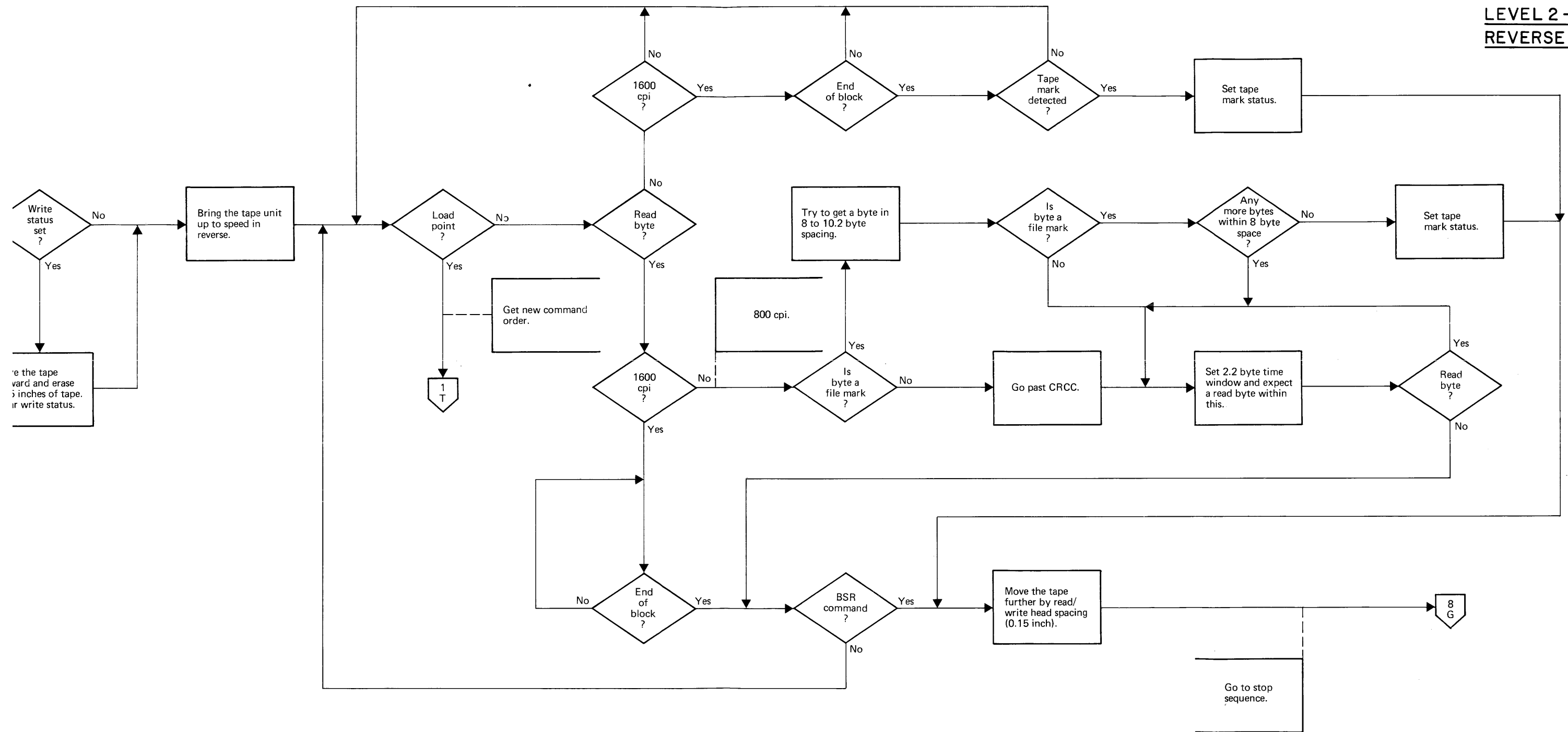
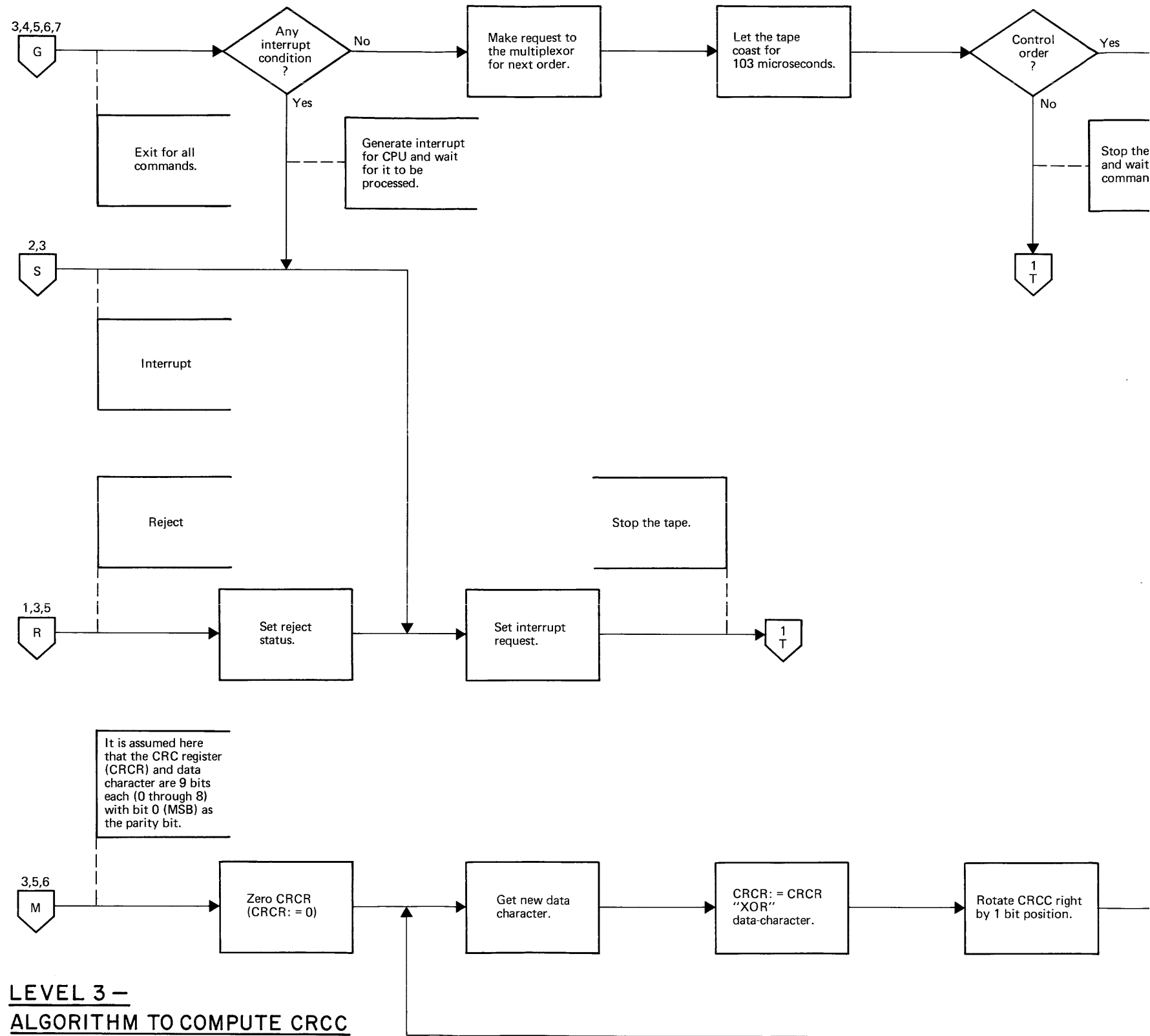


Figure 3-2. Tape Controller Overall Operation Flowchart (Sheet 7 of 8)

LEVEL 2 – STOP



**LEVEL 3 –
ALGORITHM TO COMPUTE CRCC**

LEVEL 2- STOP

REJECT AND INTERRUPT

CRCC

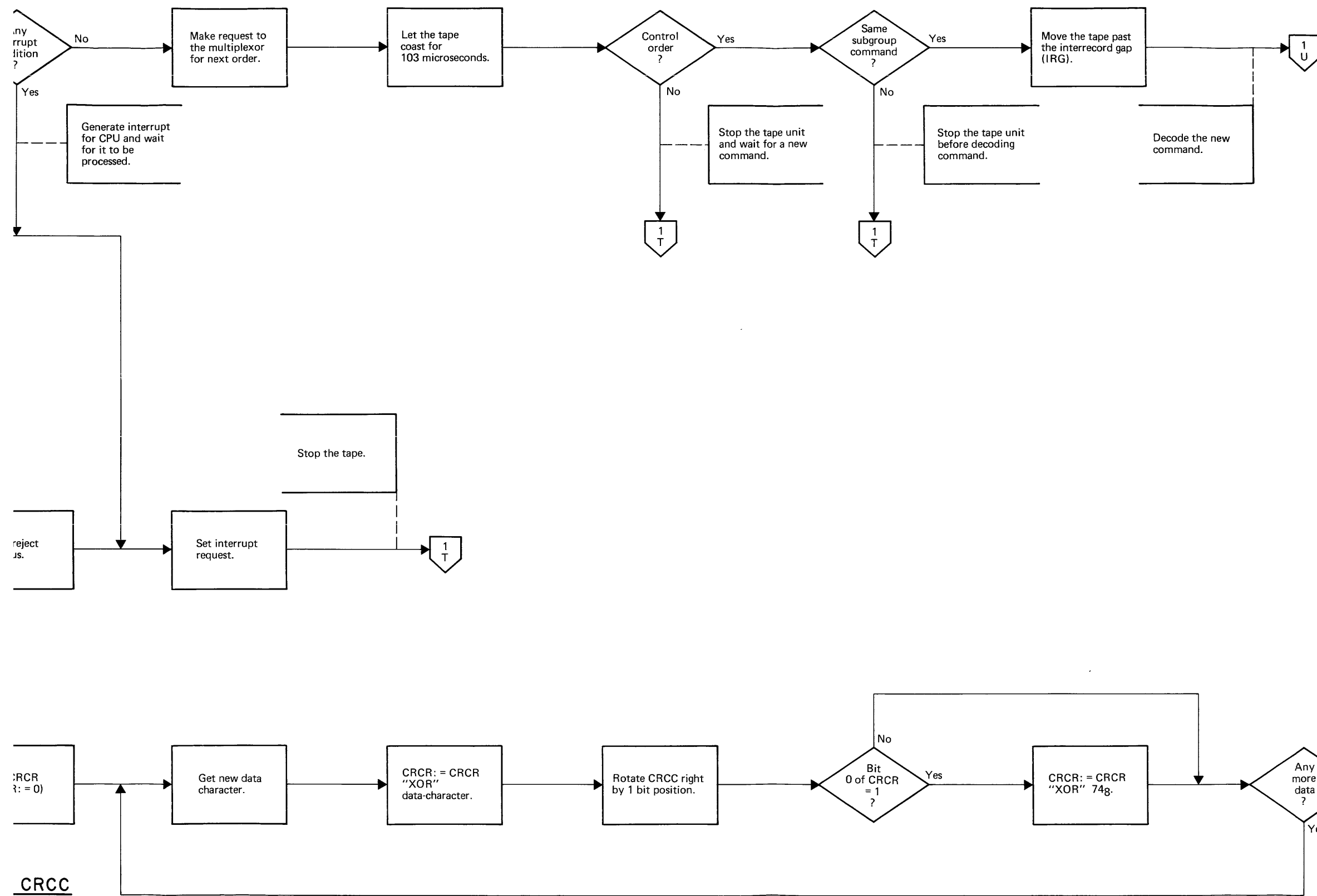


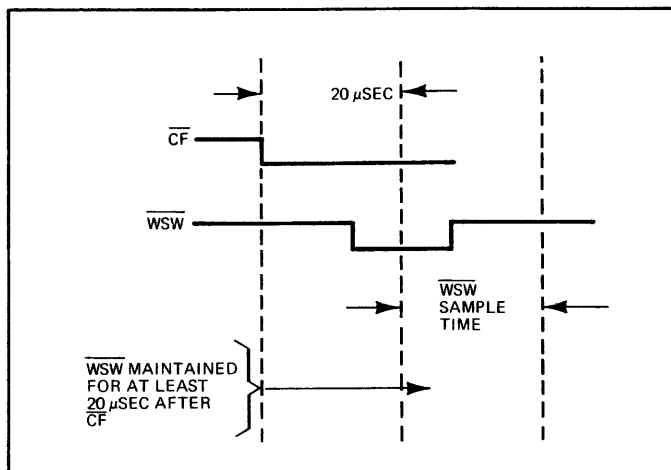
Figure 3-2. Tape Controller Overall Operation Flowchart (Sheet 8 of 8)

3-35. The actual microprogram begins at page eight of the listing. In the listing, the first group of numbers (reading left-to-right) are the sequence numbers (in decimal). These are followed by the ROM address numbers (in octal), which are followed by the 20-bit ROM data word (in binary). Labels for routines and sub-routines appear next (reading left-to-right). Labels are a maximum of six symbols long. The operation code (three letters) appears next. All operation codes and their meanings are listed in the controller processor PCA discussion. Operation codes indicate one of six word format types for field decoding. Applicable field mnemonics, references, and constants (if used) are listed next. Octal numbers shown are preceded by the number symbol (#). Remarks are shown last in the listing. If a line begins with an asterisk (*) the entire line is a comment. The comments, remarks, and flowcharts for the microprogram provide adequate information for understanding the overall operation of the subsystem.

3-36. TAPE CONTROLLER TIMING AND TAPE MOVEMENT. Figure 4-12 in section IV is an overall tape controller timing diagram for a typical write operation. Figure 4-13 shows a typical read operation. Both these diagrams illustrate NRZI writing as an example. Also, the following conditions apply to data transfers between the interface and the tape unit.

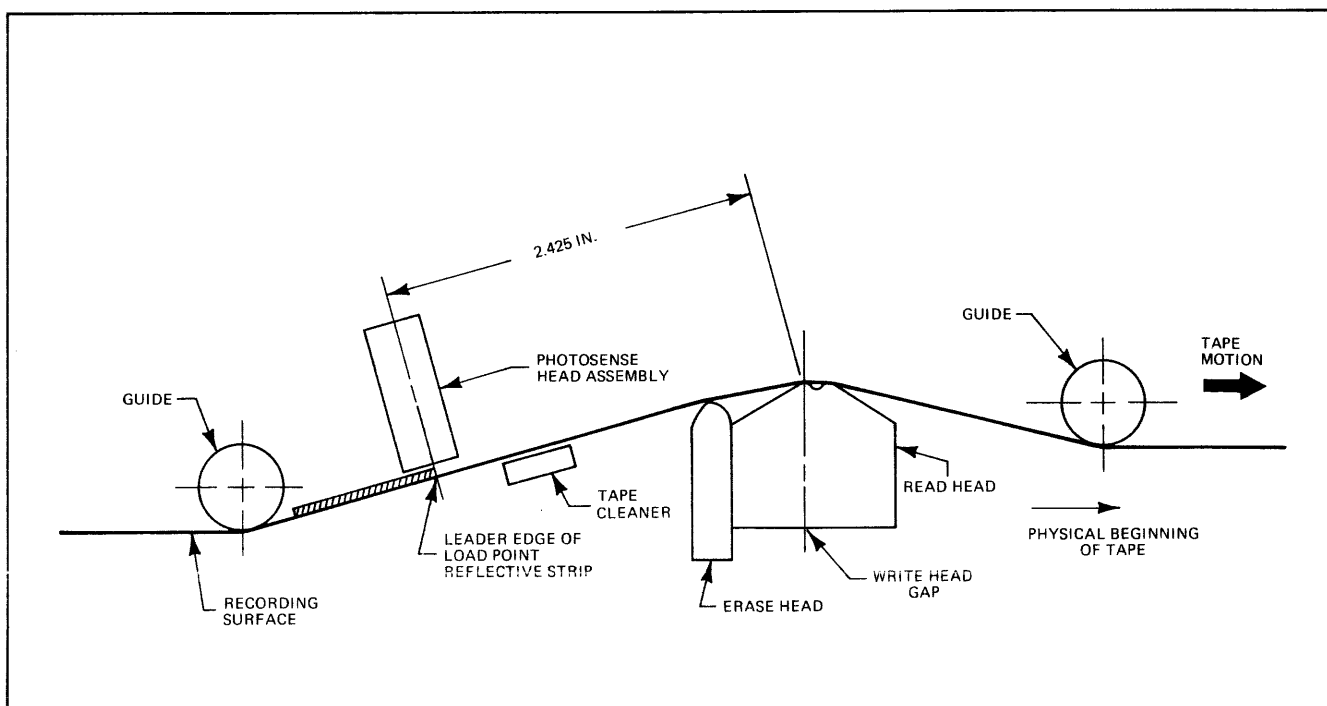
- a. For the write mode, the levels of the write data bus and write parity line ($\overline{WD\ 0:7}$ and \overline{WDP}) at the input to the tape unit receiver gates in the tape unit should be settled for 500 nanoseconds before and after the Write Clock (\overline{WC}) is received from the tape controller.
- b. For the read mode, the levels of the read data bus and read parity line ($\overline{RD\ 0:7}$ and \overline{RDP}) should be settled by the transition time (drop to low) of the Read Clock (\overline{RC}), and the levels remain settled until one microsecond (maximum), before the next Read Clock.
- c. The time for the following edge of the Read Clock (\overline{RC}) pulse to drop to a low is two microseconds minimum, three microseconds maximum.
- d. When the Forward (\overline{CF}) command is issued to the tape unit, the Set Write (\overline{WSW}) command is sampled by the tape unit following a 20-microsecond maximum delay period. The tape controller maintains the \overline{WSW} command at a low level for not less than 20 microseconds after it issues \overline{CF} to the tape unit. See figure 3-3.

3-37. Figure 3-4 represents the general physical orientation of tape unit transport heads and the photo-sense assembly. The orientation is the same for NRZI and PE tape units. Figures 3-5 through 3-7 represent typical tape movement past the heads during write and read operations, and for character drop-out detection. The diagrams generally represent NRZI and PE operations.



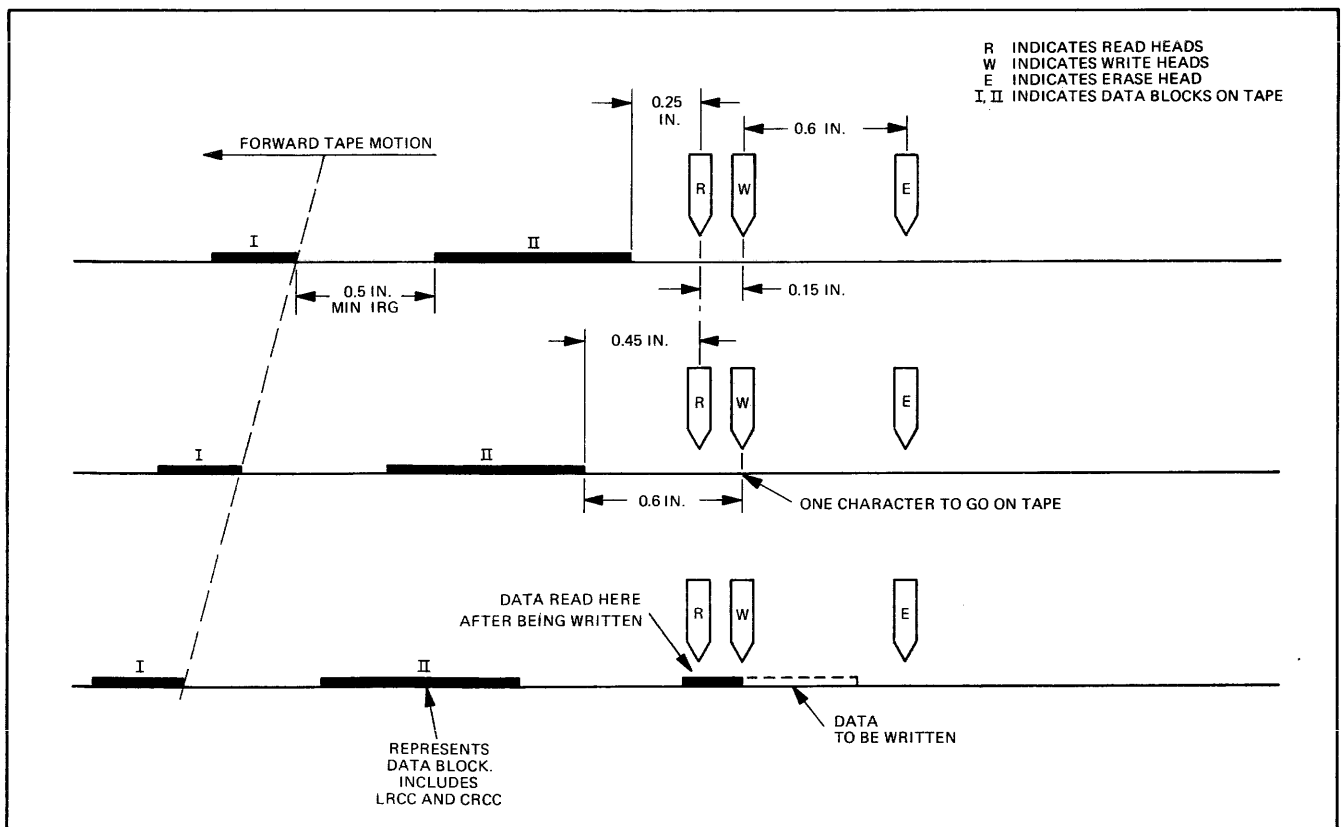
2180-43

Figure 3-3. \overline{WSW} , \overline{CF} Sequencing



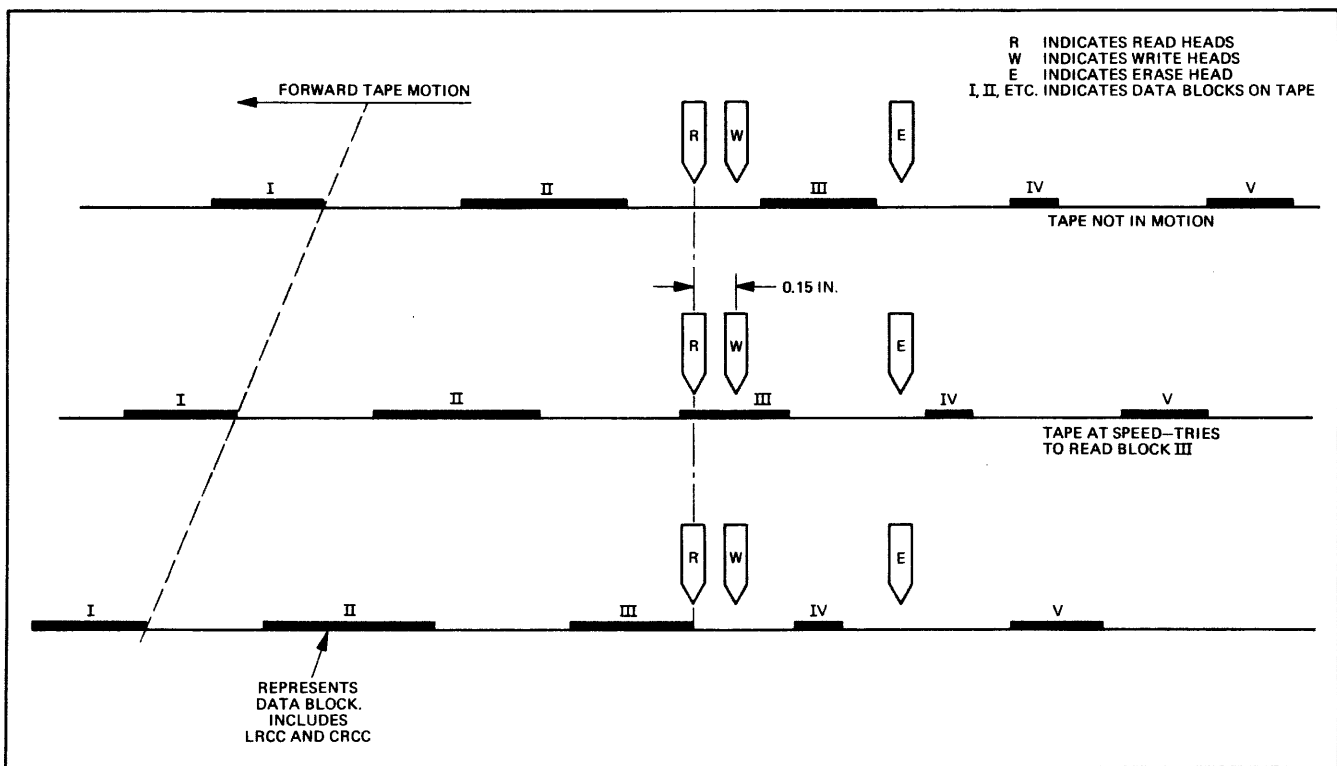
2180-44

Figure 3-4. Orientation of the Erase, Write, Read, and Photosense Head Assemblies



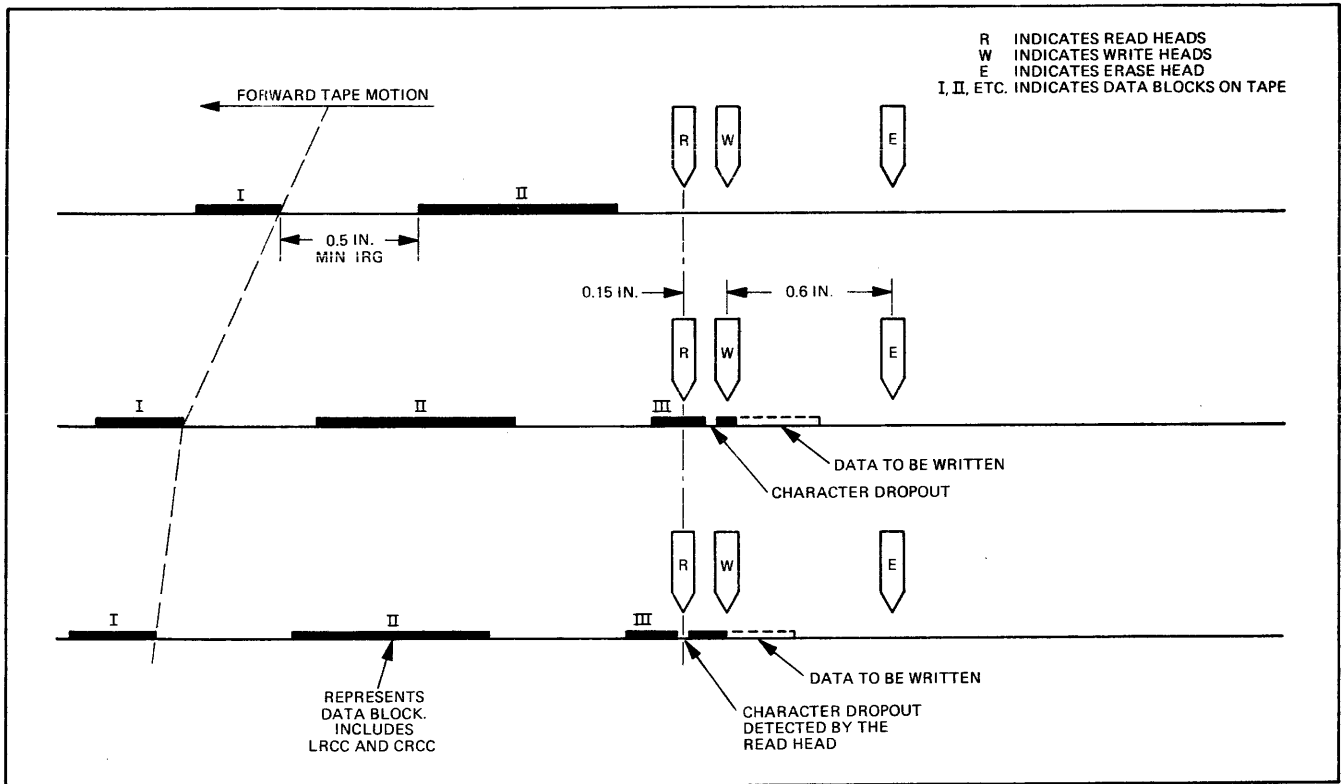
2180-45

Figure 3-5. Typical Write Operation, Tape Movement Diagram



2180-46A

Figure 3-6. Typical Read Operation, Tape Movement Diagram



2180-47

Figure 3-7. Detection of Character Dropout During Write Operation
Tape Movement Diagram

3-38. CONTROLLER PROCESSOR PCA.

3-39. In order to understand the details of the microprogram for the subsystem, it is necessary to understand logical sections and functional operating particulars of the controller processor PCA. Paragraphs 3-40 through 3-55 define the logical portions of the PCA. Paragraphs 3-56 through 3-69 describe the most important aspects of operation. The word formats and field definitions are primary points in the discussion. Refer also to the consolidated microcoding sheet and the timing diagram in section IV to fully understand controller processor operation.

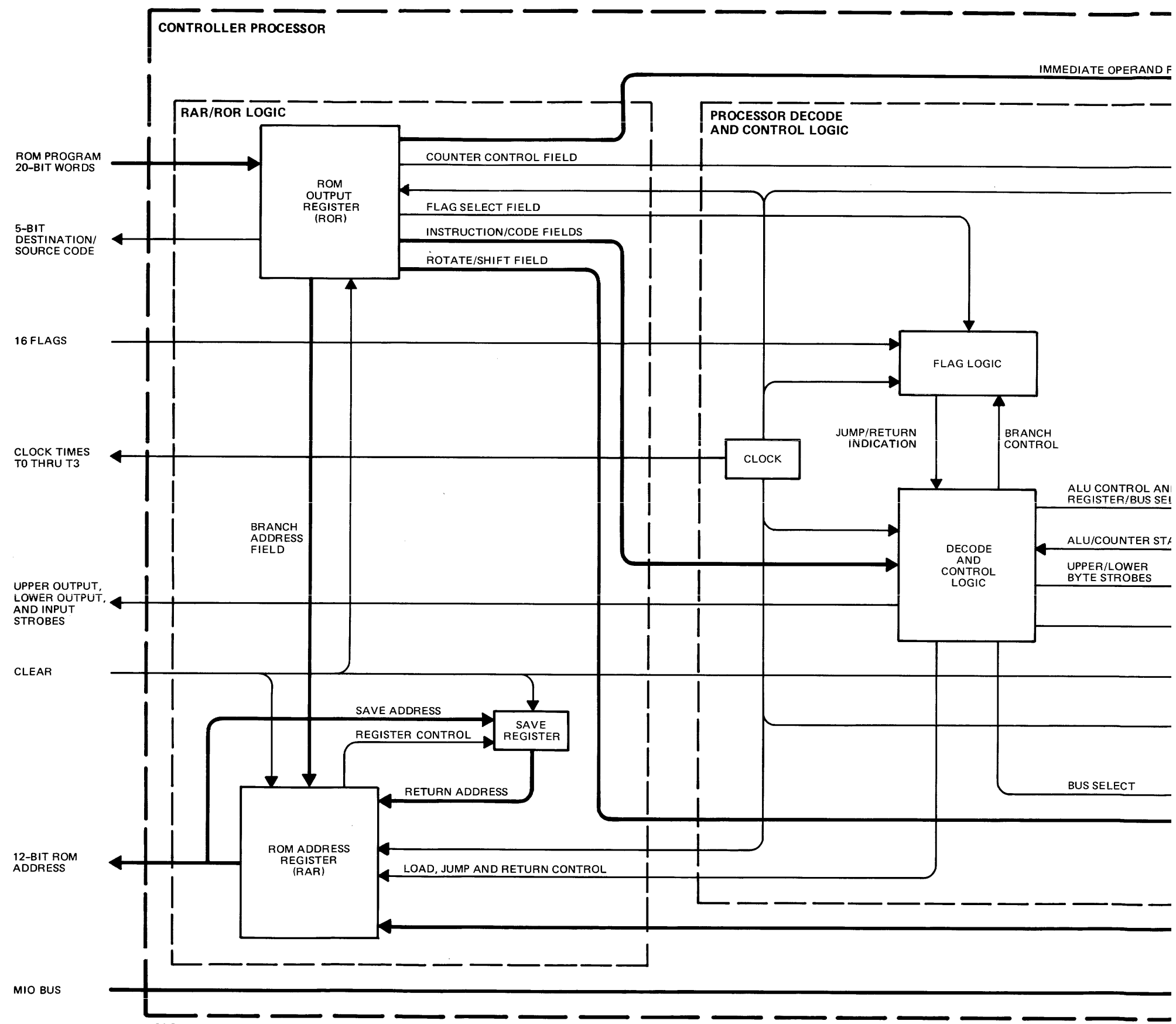
3-40. CONTROLLER PROCESSOR LOGICAL SECTIONS. The overall block diagram of the controller processor PCA is shown in figure 3-8. The primary function of the controller processor is to implement the microprogram for the subsystem. As shown in the diagram, four major logic sections of the PCA, listed below, accomplish this. They are:

- a. The RAR/ROR logic.
- b. Processor decode and control logic.
- c. Registers and counter.
- d. Arithmetic and Logic Unit (ALU).

3-41. Note that all programmed command input and data to and from the controller processor is routed via the MIO bus. Input data is loaded into the selected general purpose register. As directed by the microprogram, the data is processed through the ALU, via the A and B buses back to the MIO bus. The A bus is driven by the Immediate Operand field, the counter, and three of the general purpose registers. The B bus is driven by four of the general purpose registers. One register is common to both buses. The MIO bus is used for input/output and as the return path to the general purpose registers. The controller processor microinstruction set contains arithmetic and logical instructions and conditional branching microinstructions that control the ALU and rotate shift logic. Sixteen flag lines that permit selective branching on external conditions are also provided. Direct branching is possible by testing one of the 16 flag lines. All of the controller processor internal buses have the capability of being partially selected. That is, the option of selecting the upper byte, lower byte, or the whole word is provided. Also available is an external register select line which may be used to select an external register in place of any of the general purpose registers. This feature is not utilized in this subsystem, however.

3-42. Five destination/source bits are provided to select the source or destination desired when executing an input/output instruction.

3-43. The RAR/ROR logic addresses and controls the ROM readout, from the tape controller, to the ROR. The majority of ROR field readout in the controller processor is to the processor decode and control logic. The exception is the Immediate Operand field which is passed to the registers and counter section. The major sections of the controller processor may be subdivided into the logical blocks listed below. See figure 3-8, the overall block diagram. Descriptions of these logic blocks are contained in the following paragraphs.



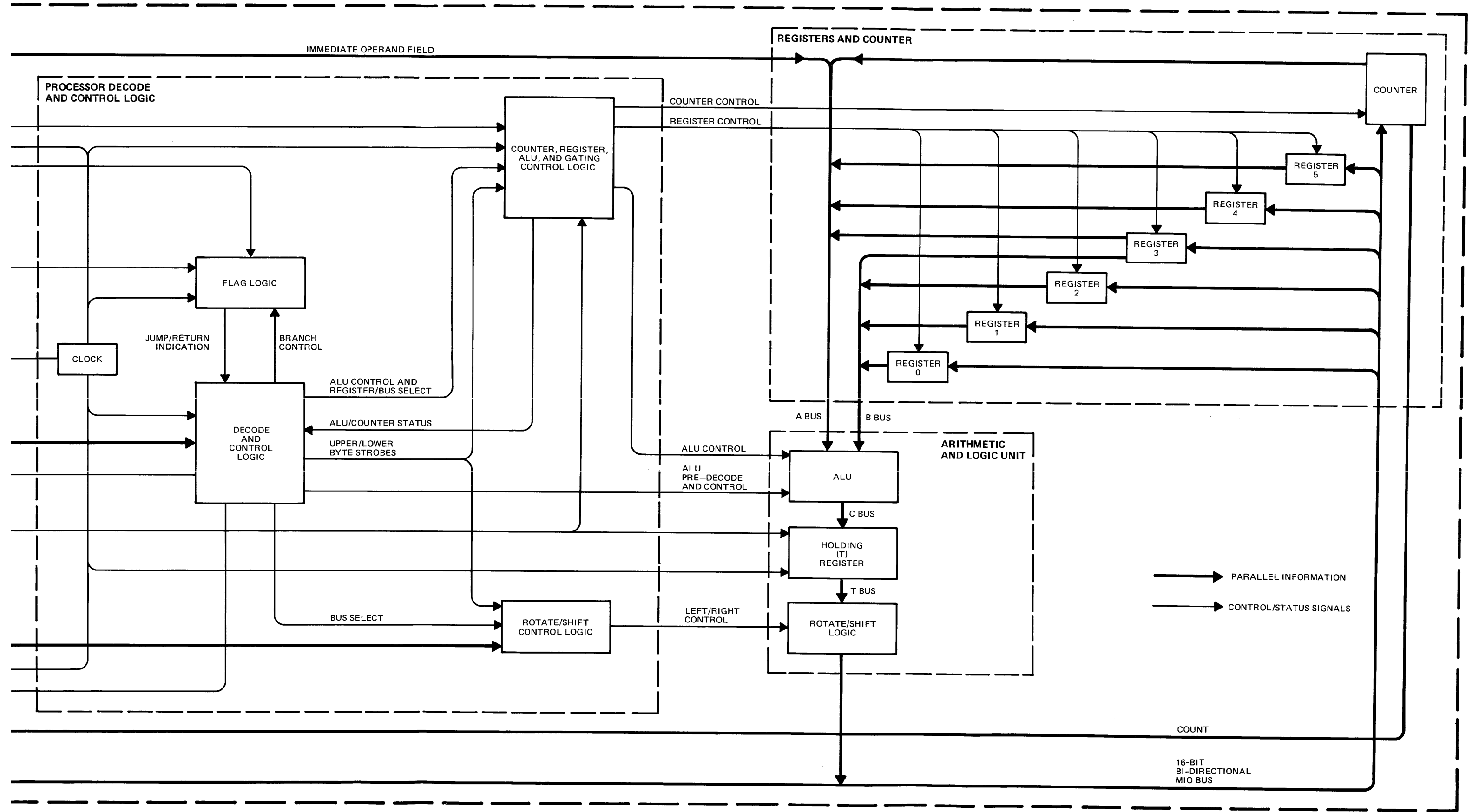
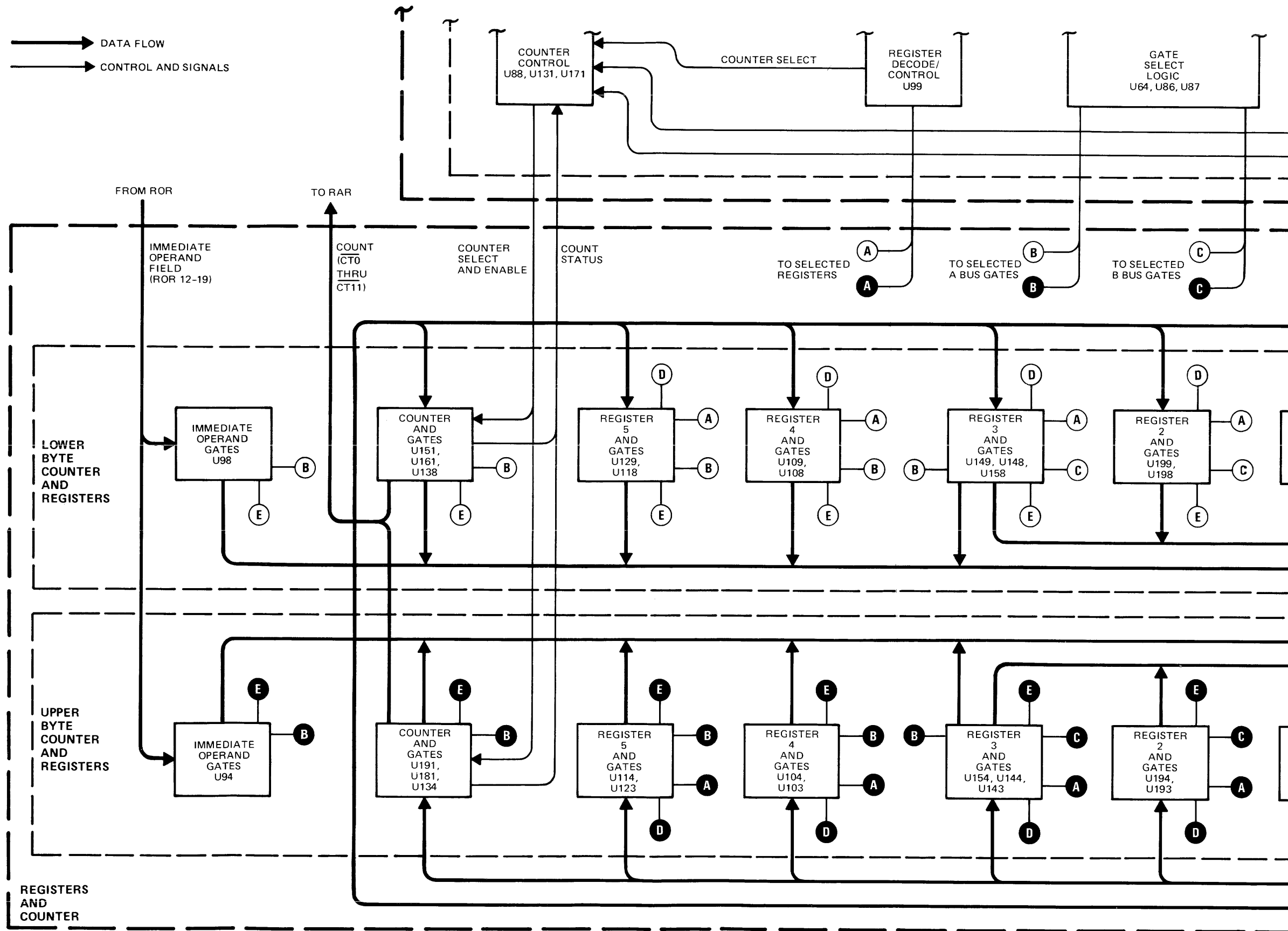
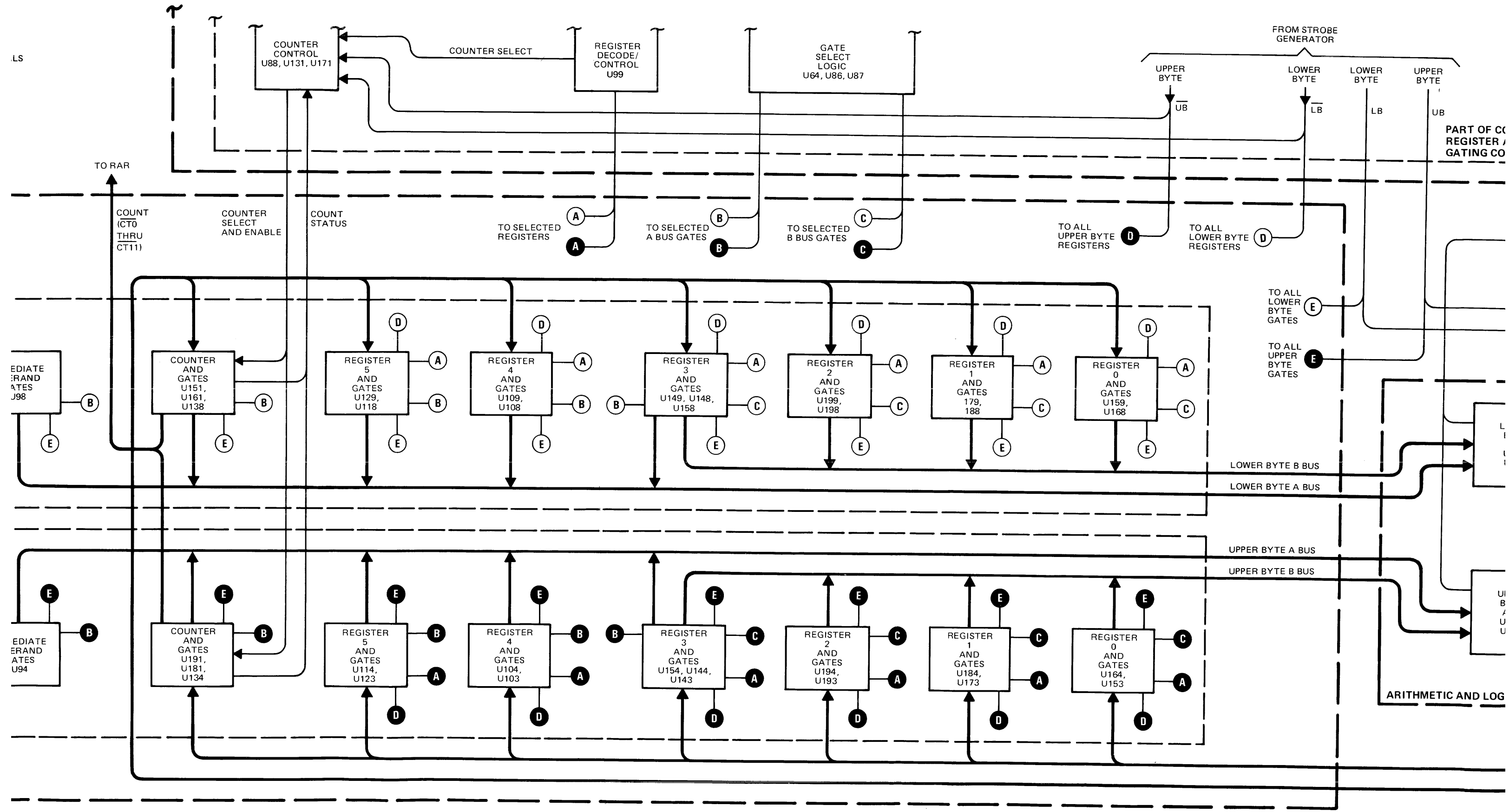


Figure 3-8. Controller Processor Overall Block Diagram

- a. Registers and counter.
 - (1) Six general purpose registers, RG0 through RG5.
 - (2) Counter.
- b. Arithmetic and Logic Unit.
 - (1) ALU.
 - (2) Holding (T) Register.
 - (3) Rotate/shift logic.
- c. RAR/ROR logic.
 - (1) ROM Address Register (RAR).
 - (2) Save Register.
 - (3) ROM Output Register (ROR).
- d. Processor decode and control logic.
 - (1) Flag logic.
 - (2) Clock.
 - (3) Rotate/shift control logic.
 - (4) Decode and control logic.
 - (5) Counter, register, ALU, and gating control logic.

3-44. Registers and Counter. There are six, 16-bit general purpose registers designated, RG0 through RG5. See the detailed block diagram, figure 3-9. Each register can be loaded from the MIO bus, and can drive the A and/or B bus. That is, it is possible to write into any one of the registers from the MIO bus while placing the contents of two registers onto the A bus and/or B bus. Registers RG0 through RG3 are connected to the B bus, while registers RG3 through RG5 are connected to the A bus. Register RG3 is connected to both buses. It should be noted here that the data being written into the registers may be from any source connected to the MIO bus. It is also possible to write into, or read from, the upper or lower byte independently from one another.





LS

COUNTER CONTROL
U88, U131, U171

REGISTER DECODE/
CONTROL
U99

GATE SELECT
LOGIC
U64, U86, U87

FROM STROBE
GENERATOR

UPPER
BYTE

LOWER
BYTE

LOWER
BYTE

UPPER
BYTE

PART OF C
REGISTER /
GATING CO

TO RAR

COUNT
(CT0
THRU
CT11)

COUNTER
SELECT
AND ENABLE

COUNT
STATUS

TO SELECTED
REGISTERS

TO SELECTED
A BUS GATES

TO SELECTED
B BUS GATES

TO ALL
UPPER BYTE
REGISTERS

TO ALL
LOWER BYTE
REGISTERS

TO ALL
LOWER
BYTE
GATES

TO ALL
UPPER
BYTE
GATES

IMMEDIATE
RANDOM
GATES
U98

COUNTER
AND
GATES
U151,
U161,
U138

REGISTER
5
AND
GATES
U129,
U118

REGISTER
4
AND
GATES
U109,
U108

REGISTER
3
AND
GATES
U149, U148,
U158

REGISTER
2
AND
GATES
U199,
U198

REGISTER
1
AND
GATES
179,
188

REGISTER
0
AND
GATES
U159,
U168

LOWER BYTE B BUS

LOWER BYTE A BUS

UPPER BYTE A BUS

UPPER BYTE B BUS

IMMEDIATE
RANDOM
GATES
U94

COUNTER
AND
GATES
U191,
U181,
U134

REGISTER
5
AND
GATES
U114,
U123

REGISTER
4
AND
GATES
U104,
U103

REGISTER
3
AND
GATES
U154, U144,
U143

REGISTER
2
AND
GATES
U194,
U193

REGISTER
1
AND
GATES
U184,
U173

REGISTER
0
AND
GATES
U164,
U153

ARITHMETIC AND LOG

U
B
/
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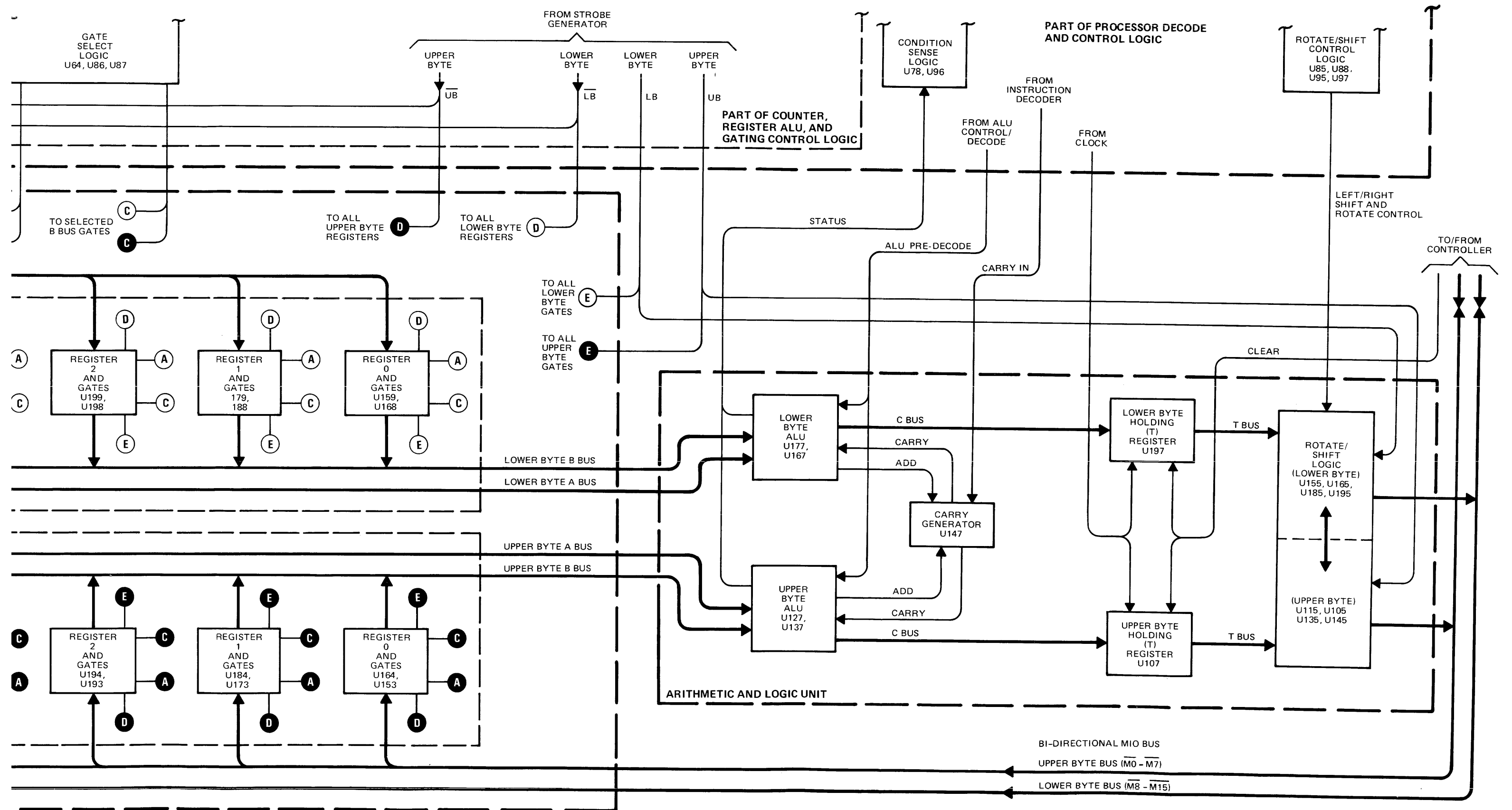


Figure 3-9. Counter, Registers, and ALU

3-45. The 16-bit binary counter is capable of being preset from the MIO bus, counted down, and gated onto the A bus. The counter may be decremented in every microinstruction. The counter can be used as a seventh register when it is not in use as a counter. It is possible to branch to the contents of the counter, thus, computed addressing is possible (described later). The counter can be decremented until a zero state is reached. It will then remain in the zero state until initialized again.

3-46. Arithmetic and Logic Unit. The Arithmetic and Logic Unit (ALU) is shown in the detailed block diagram, figure 3-9. The two inputs to the ALU are the A and B buses. The buses are driven only by the internal general purpose registers, the counter, and the Immediate Operand and are not directly accessed by the tape controller. The ALU is capable of performing the functions listed in table 3-4. Mnemonics and functions are explained in later paragraphs. Since the Rotate/shift logic follows the T-register, described next, any of the functions listed in table 3-4 may be performed, then the results shifted or rotated.

Table 3-4. ALU Functions

FUNCTION	MNEMONIC
A PLUS B	ADD
$A \cdot B$	AND
$A + B$	IOR
$A \oplus B$	XOR
A MINUS B	SUB
\overline{A}	CMA
\overline{B}	CMB
A	PSA
B	PSB
(IMMEDIATE OPERAND) PLUS B	ADI
(IMMEDIATE OPERAND) \cdot B	ANI
(IMMEDIATE OPERAND) + B	IOI
(IMMEDIATE OPERAND) \oplus B	XOI
(IMMEDIATE OPERAND)	PSI

3-47. The output of the ALU is latched into a holding (T) register, which serves to hold data for output on the MIO bus or for storage in a general purpose register. The T-register is a 16-bit latch. It serves as the master for the general purpose registers which act as slaves during recirculate instructions. It is also the output register for output instructions. The output of this holding register is fed into the rotate/shift logic.

3-48 The rotate/shift logic makes it possible to rotate or shift the data left one bit, right one bit, or left four bits. The rotate microinstructions are applicable to full 16-bit words only. When no rotate or shift operation is performed, data passes straight through the rotate/shift logic. The output of the rotate/shift logic is put onto the MIO bus.

3-49. RAR/ROR Logic. The ROM Address Register (RAR) is a 12-bit register that is incremented at $\overline{T0}$. See the detailed block diagram in figure 3-10. It can also be preset to the desired address from one of four sources during $\overline{T1}$, $\overline{T2}$. These are:

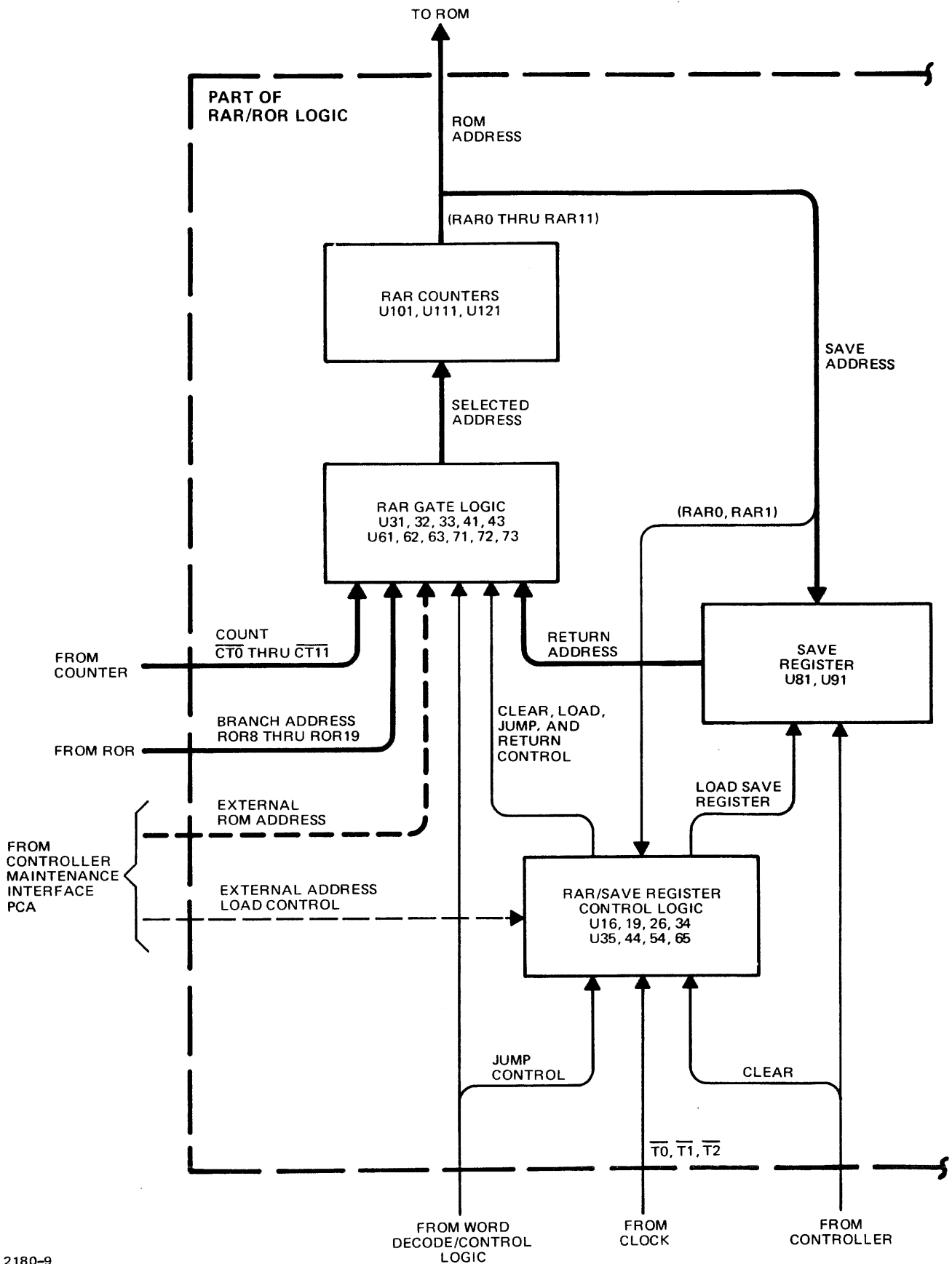
- a. The decrementing counter.
- b. The Save Register.
- c. The Branch field in the instruction word from the ROR.
- d. The address selected on the maintenance panel when it is connected.

3-50. The RAR feeds an address directly into the Read Only Memory (ROM), effective at $\overline{T3}$, to read out the desired word which is latched in the ROR at $\overline{T0}$. The ROM is contained on the tape controller PCA of the subsystem. The ROM memory is organized on a modular basis in three blocks of 256 words for this subsystem. (Addresses 0000 thru 0377, 0400 thru 0777, and 1000 thru 1400.) Readout from the ROM chips normally takes about 100 nanoseconds.

3-51. The 12-bit save register, shown in the detailed block, figure 3-10, saves the current address +1, at the end of $\overline{T0}$, on a call to subroutine instruction, thus providing single level jump to subroutine capability. Both the RAR and save registers are under control of the RAR/save register control logic. A return is made to the address in the save register on return from subroutine instructions.

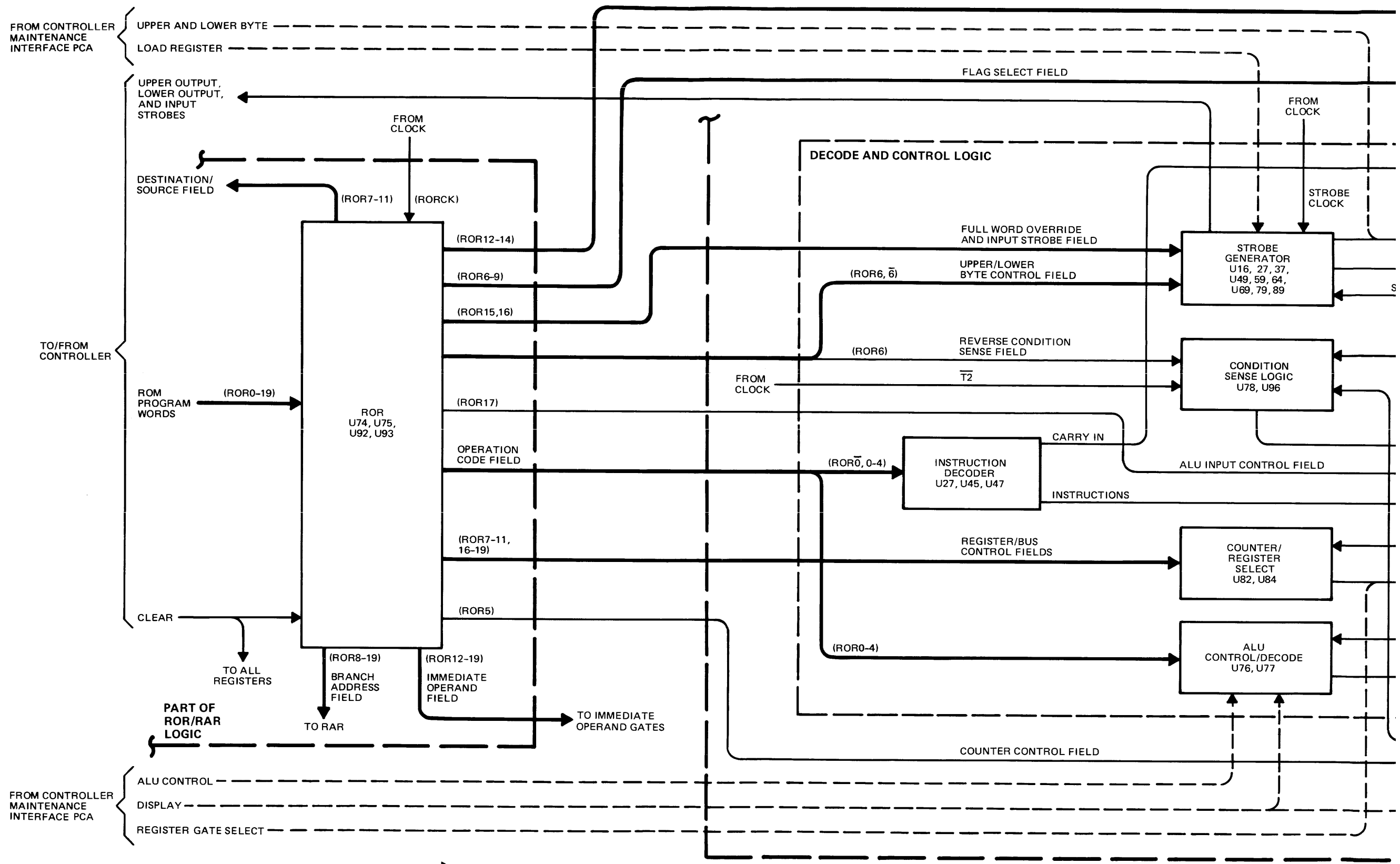
3-52. The ROM Output Register (ROR) is a 20-bit register that holds the current word from the ROM. See the detailed block diagram in figure 3-11. At the beginning of each cycle ($\overline{T0}$) the new ROM word is clocked into the register. The output fields are directed into the following logic of the decode and control logic in the processor decode and control logic section.

- a. Instruction decoder.
- b. ALU control decode.
- c. Counter/register select.
- d. Word decode/control.
- e. Condition sense.
- f. Strobe generator.



2180-9

Figure 3-10. Controller Processor RAR/Save Logic, Detailed Block Diagram



PARALLEL INFORMATION
 CONTROL AND SIGNALS

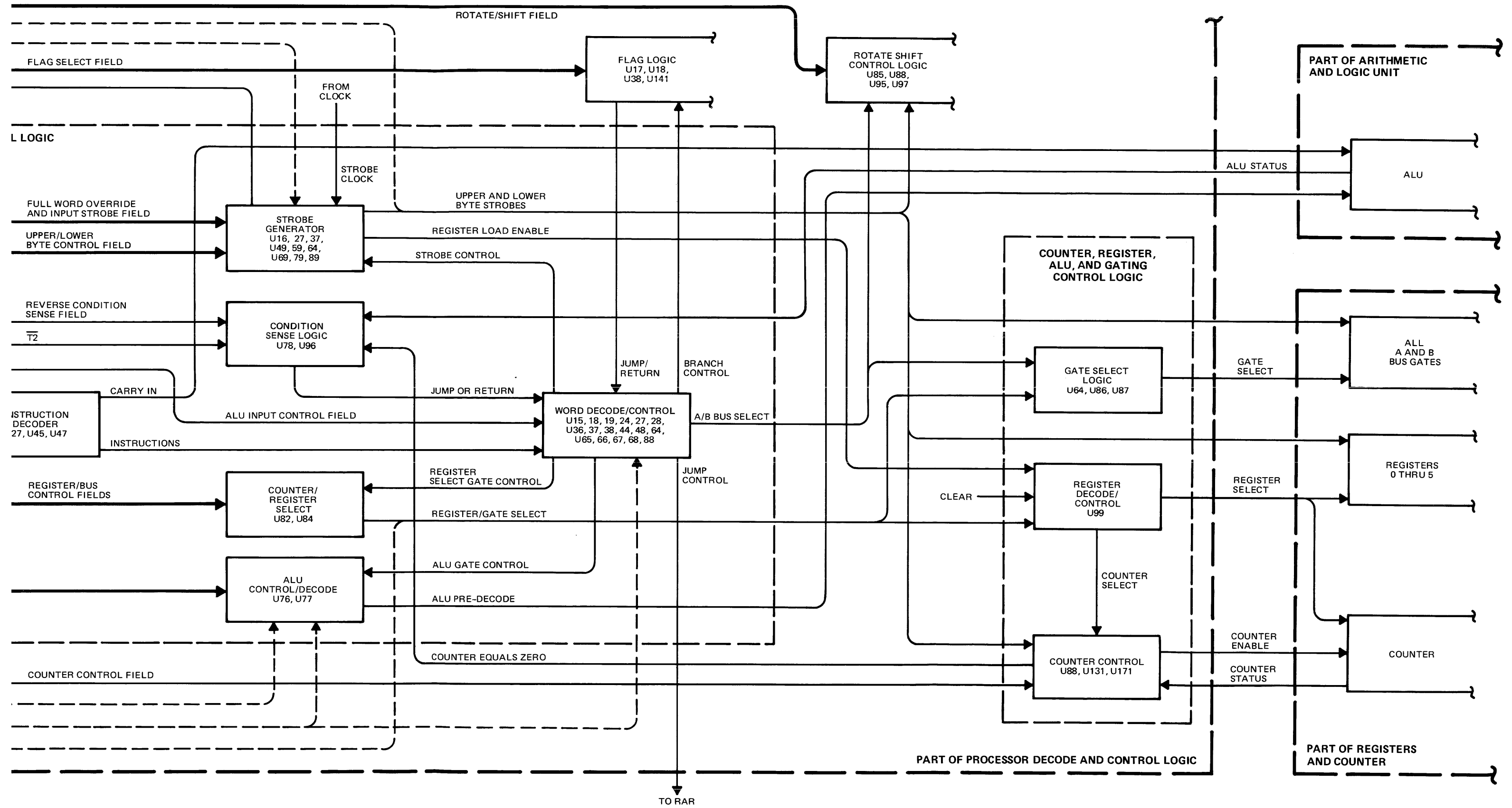


Figure 3-11. Controller Processor ROR, Decode, and Control Logic, Detailed Block Diagram

3-53. The ROR also has outputs fed to the flag logic and rotate/shift control logic in the processor decode and control logic section. The Counter Control field (ROR 5) is applied to the counter control logic in the counter, register, ALU, and gating control logic. The processor decode and control logic is explained in the next paragraph.

3-54. Processor Decode and Control Logic. See the processor decode and control logic in the overall block diagram, figure 3-8 and the detailed block diagram of control logic in figure 3-11. The blocks of logic listed below are expanded in the detailed figure.

- a. The ROR, flag logic, and rotate/shift control logic block (representations may be more easily viewed in the overall block).
- b. The decode and control logic.
- c. Counter, register, ALU, and gating control logic.

3-55. The controller processor clock is shown in the detailed diagram in figure 3-12. The processor cycle time is selected to fit the need of the tape controller card. The timing is determined by the 9.216-MHz crystal. Crystals up to 10 MHz may be used in the controller processor. The cycle consists of four evenly divided phases, each phase being 100 nanoseconds when the controller processor is run at the maximum clock rate of 10 MHz. For the HP 30115A Magnetic Tape Subsystem, each phase time is 108.5 nanoseconds cycle time is 434 nanoseconds. Four clock lines leave the controller processor, but these are not used in this subsystem. Each of the lines represents one of the phases. The AT clock lines and CTL1, CTL2 lines are used to control timing in maintenance mode.

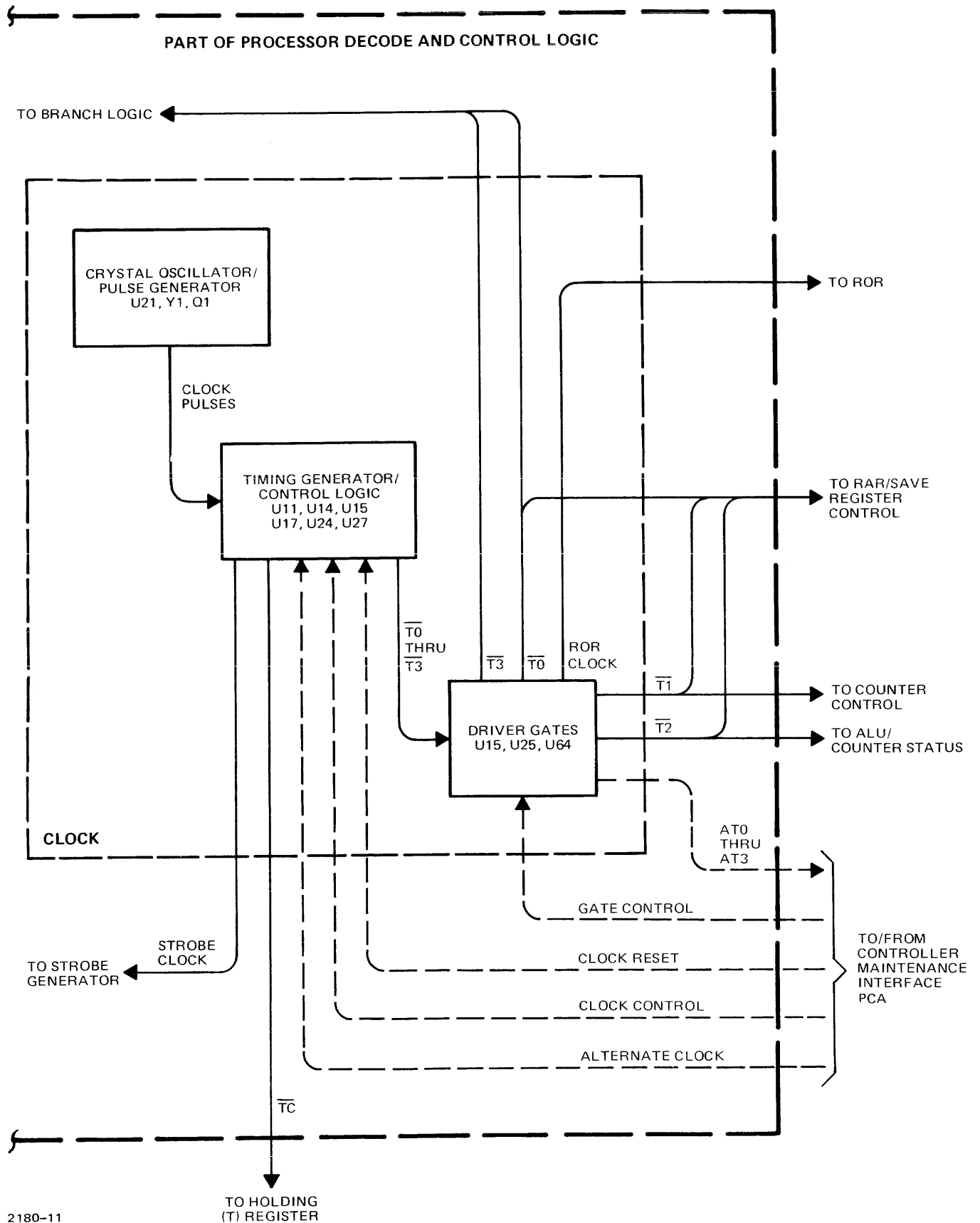
3-56. **CONTROLLER PROCESSOR OPERATION.** The controller processor operation discussion provides explanations of PCA logic operations, timing, and the microinstruction set. The discussion of the microinstruction set is the essential information to assimilate insofar as operation of the controller processor in the subsystem is concerned. Material concerning the microinstructions includes:

- a. The microinstruction list.
- b. Descriptions of the microinstructions.
- c. Descriptions of the word format fields.
- d. Field bit pattern information.

3-57. Although the controller processor may be thought of somewhat like a "black-box" when considering overall subsystem operation, it is necessary to understand the microinstructions, word formats, and internal operation of the controller processor if the specifics of the microprogram listing for the subsystem are to be understood.

3-58. Controller Processor Logic. Simplified logic diagrams that support the explanations of logic operation and data in the tables will be found in the *HP 3000 Computer System Simplified Diagrams Manual* under controller processor diagram set SD 163;

3-59. The general sequence of events in controller processor internal operation are that a general purpose register, and/or the counter, or immediate operand contents are placed on the A and B buses. The A and B buses are then fed into the ALU, the ALU output is stored in the T-register, which in turn feeds the rotate/shift



2180-11

Figure 3-12. Controller Processor Clock, Detailed Block Diagram

logic, which finally drives the MIO bus with data to be written into the selected target register or to be transferred from the PCA. If the counter is to be counted, it is not used as a source for data or an address in the same instruction. If a preset and a decrement of the counter happen to be microprogrammed in the same instruction, the preset will prevail. The counter will never be microprogrammed to decrement when its contents are to be used as the next address. The internal general purpose registers, RG0 through RG5, are implemented with latching type flip-flops. After an I/O Reset or Power-up sequence, the state of general purpose registers RG0 through RG5 will be all bits set to logical 1.

3-60. Rotate instructions in the controller processor have no meaning when used in conjunction with the byte instruction, U/L. Rotate is applicable to full words only. The output of the rotate/shift logic is driven by three-state driver gates capable of sourcing or sinking 40 milliamperes. Of this 40 milliamperes, 24 are available for the tape controller logic. Data on the MIO bus goes to the high state when the drivers are in the third (high impedance) state. That is, the bus is forced to a logical 1 when idle. (Keep in mind that MIO bus data is complemented.) Data is valid only when an input or output strobe is present. See the discussion on controller processor timing, paragraph 3-61. Destination/source line data is indicated by a high signal, logical 1, on the line. These lines are also only valid when an input or output strobe is present. The master clear of the controller processor occurs when the Clear line is low.

3-61. Controller Processor Timing. Figure 4-14 in section IV illustrates basic controller processor timing. Four timing periods, $\overline{T0}$ through $\overline{T3}$, are output from the clock logic. The magnetic tape subsystem requires the clock have a 9.216-MHz crystal installed for 45 inch-per-second operation.. This provides four phases approximately 108.5 nanoseconds long. Maximum clock rate of the controller processor is achieved with a 10-MHz crystal installed. Phases are only 100 nanoseconds long under these conditions.

3-62. The controller processor timing cycle starts with the leading edge of $\overline{T0}$, proceeds through $\overline{T1}$ and $\overline{T2}$ and ends with the trailing edge of $\overline{T3}$. Input data to the controller processor on the MIO bus is accepted in registers RG0 through RG5, or the counter only during input strobe time. The Input Strobe, (IS) one quarter cycle long, appears during the last quarter of the controller processor timing cycle, during $\overline{T3}$. Data input for the general purpose registers RG0 through RG5 should be present at least 50 nanoseconds before the end of the controller processor input strobe and must remain present for at least 10 nanoseconds past the end of the input strobe. During normal controller processor operation these conditions will be met. The T-register is loaded in the middle of the timing cycle. Approximately sixty nanoseconds after the loading, output data is valid on the MIO bus. In general, the data will always be valid during the last quarter of the controller processor timing cycle. It is during this time that the output strobes appear. An upper byte, Upper Output Strobe (UOS), and lower byte, Lower Output Strobe (LOS), strobe are provided. This information may be useful during troubleshooting. The five destination/source bits are valid only when an input or output strobe is present. The external select signal (not used in this subsystem), is used in conjunction with $\overline{T3}$. As shown in figure 4-14, flags must be present during the last part of phase $\overline{T0}$ to be accepted when checked. ROM address and data timing is also shown in figure 4-14. Note the following in regard to the ROM address validation and ROM data received at the controller processor:

- a. The ROM address is valid during $\overline{T3}$ and is always incremented at the beginning of $\overline{T0}$.
- b. ROM data is read out and available from 60 to 100 nanoseconds (maximum) after the ROM is addressed and the data is latched into the ROR by the RORCK signal occurring during $\overline{T0}$.
- c. The crossover in the ROM address timing line (in the controller processor timing diagram) immediately after $\overline{T3}$ indicates that the address (binary pattern) may or may not change state during this time depending upon previous instructions and internal states.
- d. At the end of $\overline{T0}$ the address is latched into the save register if required (by the operation code).
- e. From the beginning of $\overline{T1}$ through $\overline{T2}$ the address may or may not be changed.

3-63. Overall Controller Processor Microinstruction Set. Table 3-5 is a consolidated list of microinstructions available for use in the controller processor. The microinstruction set may be functionally described

Table 3-5. Controller Processor Microinstruction Operation Codes

MNEMONIC	DEFINITION
WORD TYPE ONE	
ADD	Addition operation code. The A bus is added to the B bus and the result is placed in the T-Register.
SUB	Subtraction operation code. The B bus is subtracted from the A bus and the results are placed in the T-Register. The subtraction is two's complement.
IOR	"Inclusive or" operation code. The A and B buses are "or"ed together and the results stored in the T-register.
XOR	"Exclusive or" operation code. The A and B buses are "exclusive or"ed together and the results are placed in the T-register.
AND	"And" operation code. The A and B buses are "and"ed and the results are placed in the T-register.
CMA	Complement A bus operation code. The complement of the A bus is placed in the T-register.
CMB	Complement B bus operation code. The complement of the B bus is placed in the T-register.
PSA	Pass A bus operation code. The A bus content is placed in the T-register.
PSB	Pass B bus operation code. The B bus content is placed in the T-register.
WORD TYPE TWO	
ADI	Addition to the immediate operand, operation code. The immediate operand is added to whichever byte is selected on the B bus and the results are placed in that byte of the T-register.
ANI	"And" with the immediate operand, operation code. The immediate operand is "and"ed with the selected B bus byte and the resulting byte is placed in the T-register.
XOI	"Exclusive or" with the immediate operand, operation code. The immediate operand is "Exclusive or"ed with the selected B bus byte and the resulting byte placed in the T-register.
IOI	"Inclusive or" with the immediate operand, operation code. The immediate operand is "or"ed with the selected B bus byte and the resulting byte is placed in the T-register.

Table 3-5. Controller Processor Microinstruction Operation Codes (Continued)

MNEMONIC	DEFINITION
WORD TYPE TWO (Cont.)	
PSI	Pass the immediate operand, operation code. The immediate operand is placed in the selected byte of the T-register.
WORD TYPE THREE	
OTI	Output immediate operand, operation code. The Immediate Operand field is placed on the selected byte of the MIO bus for output to the destination specified in the destination field.
WORD TYPE FOUR	
IOC	Input/output control operation code. The IOC instruction either sets up the path for data to be placed on the MIO bus from the selected register, or clocks data into the selected register from the MIO bus, depending on the I/O field bit. The data may also be rotated or shifted during the output phase in command execution.
WORD TYPE FIVE	
JMP	Jump operation code. This is an unconditional branch to the address specified in the branch address field. i.e. $RAR \leftarrow \text{BRANCH ADDRESS};$
JMX	Jump, operation code. This is an unconditional branch to the address specified in the lower order 12 bits of the counter. The Branch Address field and the higher order four bits of the counter are ignored. The counter has to be made positive-true before it is used as an address. i.e. $RAR (0:12) \leftarrow \text{COUNTER} (4:12);$
JMZ	Jump on T = 0 operation code. This is a branch to the address specified in the Branch Address field if the condition T-register equals zero is met, if not, the next instruction in sequence is executed. In all internal conditional branch instructions, the condition under test is the one that existed mid-cycle of the previous instruction, that is, the value being loaded into the T-register. i.e. $\text{IF } T = 0 \text{ THEN}$ $RAR \leftarrow \text{BRANCH ADDRESS}$ else $RAR \leftarrow RAR + 1;$
JXZ	Jump on counter = 0 operation code. The branch is taken if the condition, counter equals zero is met, otherwise, the next instruction in sequence is executed. Care should be used in interpreting this instruction as the test occurs <i>before</i> the counter is decremented. This instruction should not directly follow a preset of the counter since the counter will not have had

Table 3-5. Controller Processor Microinstruction Operation Codes (Continued)

MNEMONIC	DEFINITION
WORD TYPE FIVE (Cont.)	
JXZ (Cont.)	<p>time to complete preset. An undesired jump may occur if the counter is still 0.</p> <p>i.e. IF COUNTER = 0 THEN RAR ← BRANCH ADDRESS else RAR ← RAR + 1;</p>
JSZ	<p>Jump on Sign = 0 operation code. The branch is taken if the condition, sign equals zero is met, otherwise, the next instruction is executed.</p> <p>i.e., IF SIGN = 0 THEN RAR ← BRANCH ADDRESS else RAR ← RAR + 1;</p>
JOV	<p>Jump on overflow operation code. The branch is taken if the condition, Overflow of the ALU is met, otherwise the next instruction is executed.</p> <p>i.e., IF OVERFLOW THEN RAR ← BRANCH ADDRESS else RAR ← RAR + 1;</p>
CAL	<p>Call subroutine operation code. This is a branch to a subroutine while retaining the return address in the save register.</p> <p>i.e., BEGIN RAR ← RAR + 1; SAVE ← RAR; RAR ← BRANCH ADDRESS END</p>
CXZ	<p>Call subroutine on Counter = 0 operation code. If the counter is zero, the call to subroutine is made, otherwise the next instruction in sequence is executed.</p> <p>i.e., IF COUNTER = 0 THEN BEGIN RAR ← RAR + 1; SAVE ← RAR; RAR ← BRANCH ADDRESS; END else RAR ← RAR + 1;</p>

Table 3-5. Controller Processor Microinstruction Operation Codes (Continued)

MNEMONIC	DEFINITION
WORD TYPE FIVE (Cont.)	
RTN	<p>Return from subroutine operation code. This instruction is an absolute return from a subroutine. The next instruction executed is the one whose address is stored in the save register.</p> <p>i.e., $RAR \leftarrow SAVE$;</p>
RMN	<p>Return on $T \neq 0$ operation code. This instruction is a conditional return from a subroutine. If the condition, T-register not equal zero, is met, the return will occur; however, if the condition fails, a branch to the address indicated in the Branch Address field will occur. The next instruction in sequence will not implicitly be executed.</p> <p>i.e., IF $T \neq 0$ THEN $RAR \leftarrow SAVE$ else $RAR \leftarrow \text{BRANCH ADDRESS}$;</p>
CAX	<p>Call Subroutine operation code. This is a branch to a subroutine as explained in the CAL instruction except that the address of the subroutine is the lower order 12 bits of the counter. The counter contents must be positive true.</p> <p>i.e., BEGIN $RAR \leftarrow RAR + 1$; $SAVE \leftarrow RAR$; $RAR(0:12) \leftarrow \text{COUNTER}(4:12)$; END</p>
CMZ	<p>Call subroutine on $T = 0$ operation code. This is a branch to a subroutine if the condition, T-register equals zero is met. If it is not, the next instruction in sequence is executed.</p> <p>i.e., IF $T = 0$ THEN BEGIN $RAR \leftarrow RAR + 1$; $SAVE \leftarrow RAR$; $RAR \leftarrow \text{BRANCH ADDRESS}$; END else $RAR \leftarrow R + 1$;</p>

Table 3-5. Controller Processor Microinstruction Operation Codes (Continued)

MNEMONIC	DEFINITION
WORD TYPE FIVE (Cont.)	
RXN	<p>Return on Counter $\neq 0$ operation code. This instruction is a conditional return from a subroutine. If the condition, counter not equal to zero is met, the return will occur; if the condition fails, a branch to the address indicated in the Branch Address field will occur.</p> <p>i.e., IF COUNTER $\neq 0$ THEN RAR \leftarrow SAVE else RAR \leftarrow BRANCH ADDRESS;</p>
WORD TYPE SIX	
JFS	<p>Jump on Flag Set operation code. This is a branch to the address specified in the branch address field if the specified flag is present. If the flag is not present, the next instruction in sequence is executed.</p> <p>i.e., IF SELECTED FLAG = 1 THEN RAR \leftarrow BRANCH ADDRESS else RAR \leftarrow RAR + 1;</p>
RFS	<p>Return on Flag Set operation code. This instruction is similar to the conditional returns on internal conditions. If the specified flag is present, the return from subroutine is executed, if the flag is not present, the branch is taken.</p> <p>i.e., IF SELECTED FLAG = 1 RAR \leftarrow SAVE else RAR \leftarrow BRANCH ADDRESS;</p>

by examining the operation codes. The ROM instruction word is 20 bits wide, with the highest order five bits containing the operation code. The codes fall into three broad categories; arithmetic/logic codes, input/output codes, and branch codes which are discussed further in later paragraphs. These categories may be further divided into six types of word formats. These six formats are shown in figure 3-13.

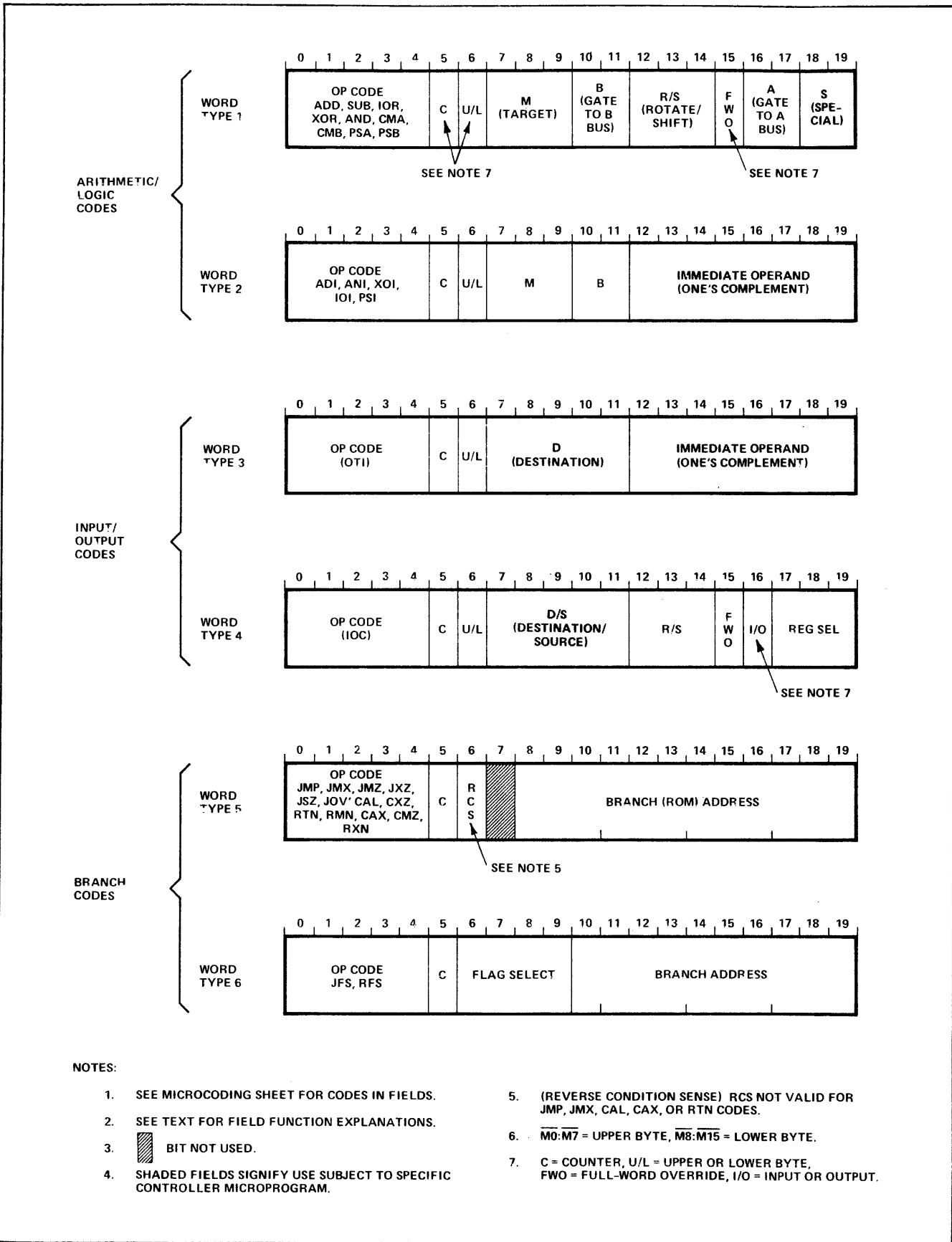
3-64. Word formats one and two are always decoded as arithmetic/logic instructions. Word formats three and four are decoded as input/output instructions and word formats five and six are decoded as branch instructions. A discussion of the word format fields follows. Some fields are common to two or more word types and explanations are not repeated in the following discussions. The consolidated coding sheet, figure 4-11, in section IV should be examined to determine bit patterns used for instructions in the various fields of each word type.

3-65. Arithmetic/Logic Instructions. The arithmetic/logic instructions utilize word type one or two, depending on whether or not an immediate operand is required. The fields of word type one are described in table 3-6. The Counter Control field (C) is common to all six word types.

3-66. Word type two is like word type one with the exception that the immediate operand replaces the Shift/Rotate field, A bus Register Select field, Special field, and the full-word override bit. Since the immediate operand is only 8-bits wide, it is necessary that it be specified in which byte the immediate operand is to be used by utilizing the U/L field. The immediate operand field is also described in table 3-6. The A bus Register Select field is not required in word type two because the immediate operand is placed on the A bus automatically (hard-wired). The B bus Select field is used in word type two to perform operations with the immediate operand. The target register field is available in word type two to specify a storage register.

3-67. Input/Output Instructions. There are only two types of input/output instructions. They are used *extensively* to control subsystem operation. The OTI instruction, word type three, has three fields; a C, U/L, and IMOP that were explained under word types one and two, and one new field, D, in lieu of the previously described fields for these bits. The new field is described in table 3-6. The IOC instruction, word type four, does not have the Immediate Operand field. The C and U/L fields are still used and the D (Destination) field becomes the D/S (Destination or Source) field. Two new fields, I/O and REG SEL, are also described in table 3-6.

3-68. Branch Instructions. The branch instructions utilize word types five and six. The two instructions JFS and RFS of word type six provide branching on external conditions. The remaining 13 operation codes of the total available, word type five, are used for branching unconditionally, or on internal conditions. Word type five has the Counter field and two new fields that replace previously described fields. These are the RCS and 12-bit Branch Address field described in table 3-6. Word type six uses the Counter field, a Flag Select field, described in table 3-6, and a 10-bit Branch Address field that allows a branch to anywhere in the present 1K (possible) memory of the microprogram. If the flag designated in the Flag Select field is set when this instruction is executed, a branch to the address indicated is made. Reiterating a few points made in the tables, the internal conditional branches or returns are always made on the results of the previous instruction.



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Figure 3-13. Controller Processor Microinstruction Word Formats

Table 3-6. Microinstruction Word Field Definitions

DESIGNATION	FIELD	DESCRIPTION
C	COUNTER	This is a one-bit field that determines whether the counter is to be decremented or not. A low, logical 0, in the field causes a decrement during the current instruction. The mnemonic is DEC. If no DEC is specified, a logical 1 is placed in the field. Bit 5, the C field, is used in all six word types.
U/L, FWO	UPPER BYTE/ LOWER BYTE, FULL-WORD OVERRIDE	This is a one-bit field for U/L, and a one-bit field for FWO. The options here are to select the upper byte, (MIO bits 0:7) the lower byte, (MIO bits 8:15) or the full word. If only one byte is selected, the other byte is left totally unaffected. The mnemonics are UPH and LWH. If no byte is specified, a full word is assumed. A logical 1 in the FWO field overrides the U/L field and allows a full word on the MIO bus.
M	TARGET	This is a three-bit field. The content of this field determines the place of storage for MIO bus data. The result of a calculation will be loaded into this target register. Any one of the six general purpose registers or the counter can be selected. The mnemonics are CTM, and ROM through R5M. An external register may be selected by this field also (all logical 1's in the field). The mnemonic is EXM for this selection. This last case is also the default selection.
B	B BUS REGISTER SELECT	This is a two-bit field used to select one of four possible general purpose registers to be gated onto the B bus for input to the ALU. The registers are RG0 through RG3. The mnemonics for the field are R0B, R1B, R2B, and R3B. If no specification is made R3B is selected (logical 1's in the field).
R/S	ROTATE/SHIFT	This is a three-bit field. As its name implies, this field invokes the rotate or shift option desired. The mnemonics are RL1, RR1, RL4, SL1, SR1, and SL4. If no rotate/shift is specified, the code for no action is set.
A	A BUS REGISTER SELECT	This is a two-bit field used to select one of four sources to be gated onto the A bus for input to the ALU. The four sources are: the counter, RG3, RG4, and RG5. The mnemonics are CTA, R3A, R4A, and R5A. R3A (all logical 1's) is selected if not other specification is made.

Table 3-6. Microinstruction Word Field Definitions (Continued)

DESIGNATION	FIELD	DESCRIPTION
S	SPECIAL	A two-bit field available for special functions of a microprogram. The field is valid only when word type one operation codes are active. The field is not used in this subsystem.
IMOP	IMMEDIATE OPERAND	This is an eight-bit field that contains a constant for the particular microprogram running. The constant is called from the address of storage as programmed.
D or D/S	DESTINATION or DESTINATION/SOURCE	This is a five-bit field used to specify an intended destination (for word type three) or destination or source (in word type four) for the data generated during this instruction. The output strobes (or the input strobe) indicate when the field is valid. The mnemonics are D00 through D37 (octal values).
I/O	INPUT/OUTPUT	This is a one-bit field used in word type four to determine whether an input or an output is being executed. The D/S field pattern specifies the destination or source. The mnemonics for this field are INP and OUT.
REG SEL	REGISTER SELECT	This is a three-bit field that determines which register (or the counter) internal to the controller processor is to be selected. Whether the register is the source of the data or the target depends on the state of the I/O field bit. The mnemonics are CTI, EXI, ROI, through R5I, for the counter, an external register, or registers RG0 through RG5 respectively.
RCS	REVERSE CONDITION SENSE	This one-bit field is to complement the sense of an internal condition when a conditional branch is being executed. The mnemonic is RCS. If no specification is made, the unaltered condition will prevail.
----	BRANCH ADDRESS	For word type five, this is a 12-bit field to allow direct branching anywhere within a <i>possible</i> 4K page of ROM. Bit seven is not used in word type five. For word type six, this field is 10-bits long and allows branching anywhere within a current 1K (possible) segment of the possible 4K page of ROM.
----	FLAG SELECT	This 4-bit field determines which of the 16 possible flags is under test. Only one of the 16 flags may be under test at any one time. Mnemonics for the flags are F00 ₈ through F17 ₈ .

When the branch is indirectly made through the counter, only the lower order 12 bits of the counter are used on counter branch instructions. The counter is always incremented after the test. The branch is only within the current 4K (possible) page of ROM. Also, the instruction sequentially following a return is not always executed without question.

3-69. Other Microinstruction Set Mnemonics. Other mnemonics that may be used in the microprogram listing are: END, (End); NOP, (No Operation); EQU, (Equate); and SKP, (Skip). These are defined as follows:

- a. The END mnemonic is the last entry in the microprogram.
- b. The NOP operation code performs no operation. The wiring for the decoded command is not connected in the controller processor. Logical 1's are loaded in all fields except the operation code field.
- c. The EQU mnemonic, if used in a listing, designates that the mnemonic shown with EQU represents the value of a particular constant. EQU is normally used only in the controller processor assembler.
- d. The SKP mnemonic in a microprogram spaces the listing to the following print-out sheet.

4-1. INTRODUCTION.

4-2. This section includes general servicing information, preventive maintenance instructions, troubleshooting data, and corrective maintenance procedures for the HP 30115A Magnetic Tape subsystem. Procedures presented assume that the service engineer performing maintenance has a thorough knowledge of the hardware gained through the use of previous sections of this manual, and thorough classroom training on the HP 3000 Computer System.

4-3. GENERAL SERVICING INFORMATION.

4-4. Ensure that printed-circuit assemblies of the HP 30215A Magnetic Tape Unit Interface remain firmly installed in their PCA module slots, as described later in this paragraph, with the extractor handles locked in place. All cables should also be firmly attached to connectors per instructions included in the following paragraphs. Refer to the HP 7970B or HP 7970E Operating and Service Manual for general servicing information applicable to the tape units. Additional general servicing information is outlined in paragraphs 4-5 through 4-20.

4-5. SAFETY PRECAUTIONS.

4-6. The primary safety precautions to be observed involve electrical systems as follows.

WARNING

Dangerous voltages are present in the HP 3000 Computer System Power Control Module and cabinet ac distribution system. Use caution when working on magnetic tape subsystem components and tape units installed in the cabinets. Observe all cautions and warnings stated in cabinet and tape unit maintenance documents.

4-7. Before pulling or installing printed-circuit assemblies (PCA) from a PCA cage, set the DC POWER switch for the computer system to STANDBY to remove power from the PCA connectors. Also follow this procedure for PCA extender assemblies and for the maintenance interface PCA. It is assumed that the maintenance personnel will perform proper system (software) shut down procedures before removing or installing any PCA in the HP 3000 Computer System.

4-8. When the interface cable is being connected to the tape controller PCA or to the tape unit, ensure that the tape unit ac power switch is off. Also turn off ac power switches on multiple tape units in the subsystem when removing or installing multiunit connector cables.

4-9. REQUIRED SERVICING EQUIPMENT.

4-10. Servicing equipment required for the HP 7970B or HP 7970E Digital Magnetic Tape Unit is listed in the operating and service manual for the applicable unit. Oscilloscopes, PCA extenders, voltmeters, logic probes, common hand tools, etc used for computer system servicing are also used for HP 30115A Magnetic Tape Subsystem and HP 30215A Magnetic Tape Unit Interface PCA servicing and maintenance. The equipment listed below is needed in addition to the items mentioned above. Refer to the *HP 3000 Computer System, Operator's Manual, 30350A Auxiliary Control Panel* and *30352A Hardware Maintenance Panel*, part no. 30352-90001, for the complete list of the equipment and instructions for the use of this equipment.

- a. HP 30350A Auxiliary Control Panel.
- b. HP 30351A Controller Processor Maintenance Panel Interface.
- c. HP 30352A Hardware Maintenance Panel.
- d. ROM Simulator ET 6710.

4-11. OPERATING CONTROLS AND INDICATORS.

4-12. Tape unit front panel controls are used when operating tape units in the off-line mode for maintenance. There are also maintenance switches within the tape unit. Refer to the operating and service manual on the applicable tape unit for a list of controls and their functions. Tape units used with the HP 30115A Magnetic Tape Subsystem have specific options included, as outlined in section I of this manual. Descriptions of controls (in the tape unit manual) that are not used with this subsystem should be ignored. There are no operating controls or indicators on the printed-circuit assemblies of the HP 30215A Magnetic Tape Unit Interface.

4-13. PRINCIPAL SERVICING POINTS.

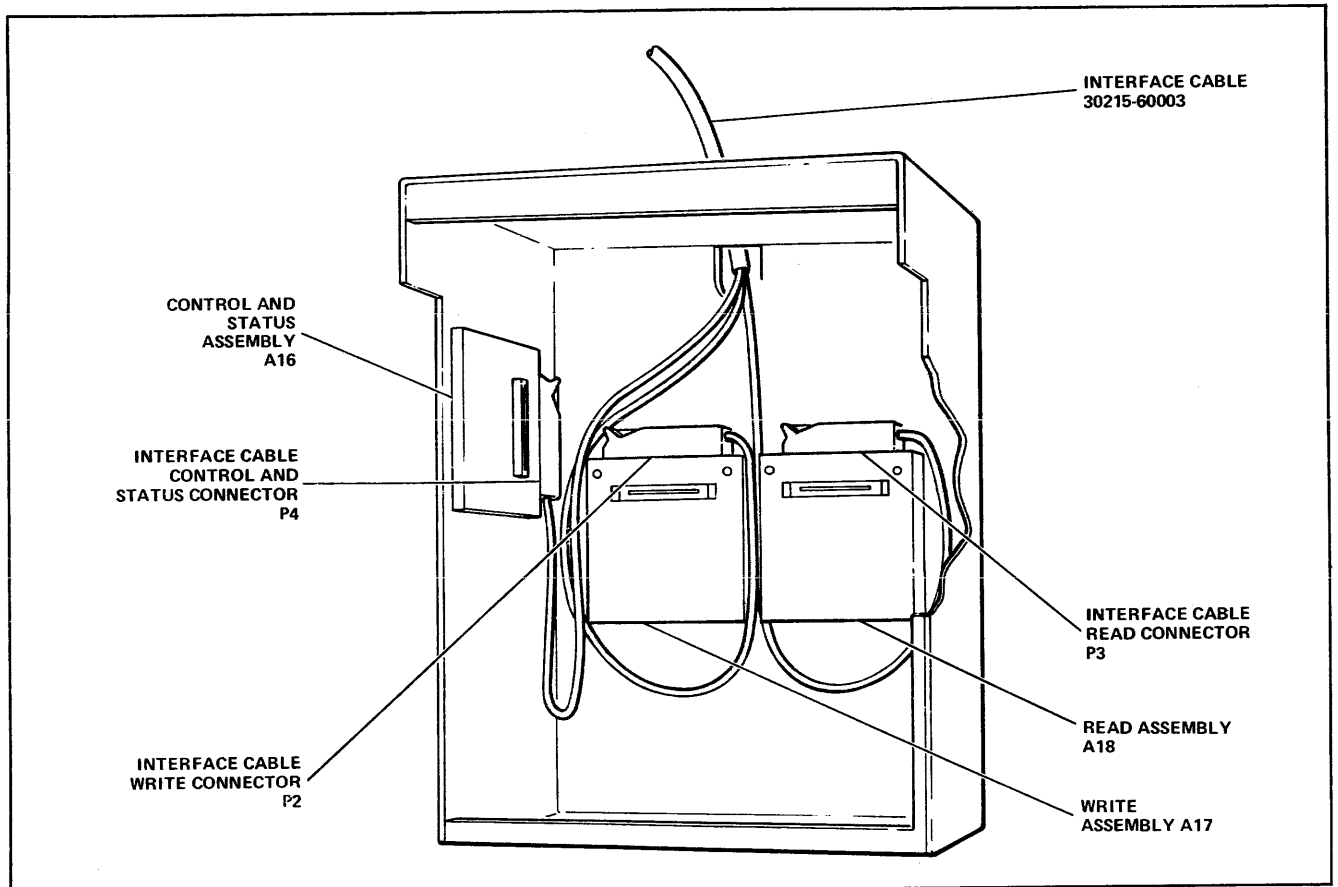
4-14. Test points and terminals used for signal measurement and waveform analysis in the tape unit are identified in the applicable tape unit operating and service manual. The status register gates, U166, and U167, various registers, and connectors on the printed-circuit assemblies in the HP 30215A Magnetic Tape Unit Interface are used as measurement points when the printed-circuit assemblies are placed on a PCA extender. These measurement points are identified in the appropriate procedures. Additional points used for servicing are the PCA connectors and tape unit connectors. Normal connections for the basic subsystem and for additional tape units are described in the following paragraphs.

4-15. BASIC SUBSYSTEM CONNECTIONS. Overall basic subsystem interface cable and PCA connector cabling connections are shown in figure 4-1. When maintenance and troubleshooting is performed, ensure that cables are replaced as shown in the diagram for basic subsystems. If there are any changes that are applicable to the installed subsystem, refer to the connection instructions in the next paragraph.

4-16. ADDITIONAL TAPE UNIT CONNECTIONS. The multiple unit connection instructions in the *HP 7970B Digital Magnetic Tape Unit Operating and Service Manual* should be referenced if additional HP 7970B Digital Magnetic Tape Units are used. Also refer to the *HP 13194A Multiunit Cable Accessory Kit Installation Manual*, part no. 13194-90003. Refer to multiple unit connection instructions in section II of the *HP 7970E Digital Magnetic Tape Unit Operating and Service Manual*, if HP 7970E Digital Magnetic Tape Units are used. See figure 4-2 for additional tape unit connection points. Constraints for optional additions are as follows:

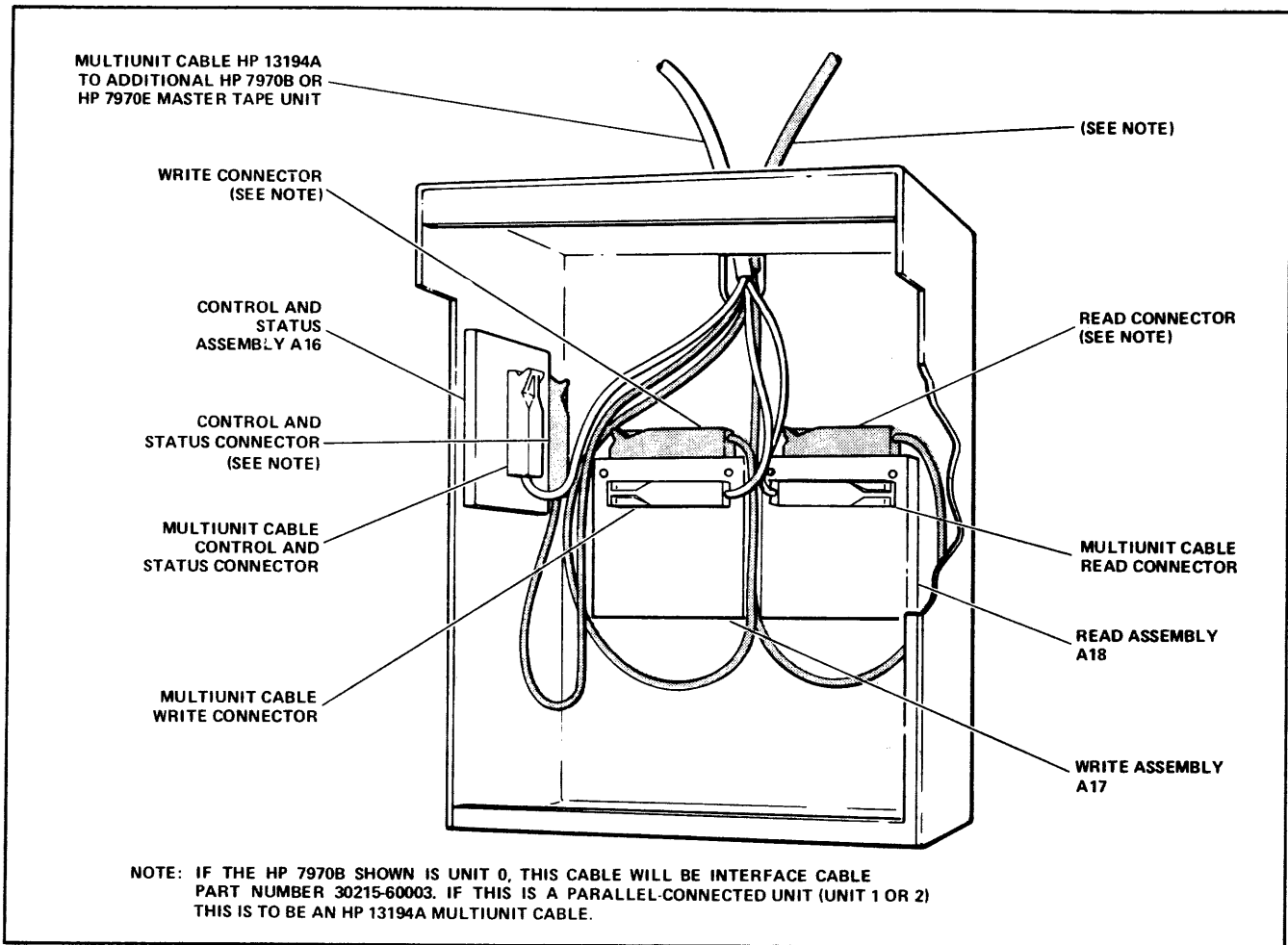
- a. Interface cable part no. 30215-60003 must be connected between the tape controller PCA and the basic subsystem tape unit regardless of the number of additional tape units used.
- b. In any parallel connections, the master or master/slave HP 7970E (if used) must be the last in the series if used in combination with the HP 7970B. Any HP 7970B tape units must be first in line from the tape controller PCA.
- c. A slave HP 7970E can not be used alone; it must be connected to a master tape unit.
- d. There can be no more than four tape units on one tape controller PCA.
- e. The HP 13194A Multiunit Cable is used for all additional tape unit connections *except* where an HP 7970E slave tape unit follows HP 7970E master tape unit in the series. In this last instance, the HP 13194A-001 Multiunit Cable must be used between the master and slave and between slave units. The HP 13194A-001 cable must be installed on the connectors provided specifically for that cable. See the example cable connection diagrams for additional tape units in figure 4-2. The table in figure 4-2 lists all 24 possible connections for the subsystem.

4-17. TAPE UNIT CONNECTOR LOCATIONS. Basic subsystem cabling connection points in the tape unit are shown in figure 4-3. The physical locations for connecting an HP 13194A Multiunit Cable from an HP 7970B to an additional HP 7970B or HP 7970E read-after-write (RAW) master tape unit are shown in figure 4-4. Physical locations on the HP 7970E RAW master tape unit for connecting the HP 13194A and HP 13194A-001 Multiunit Cables are shown in figure 4-5. The connection points for the HP 7970E RAW slave tape units are shown in figure 4-6.



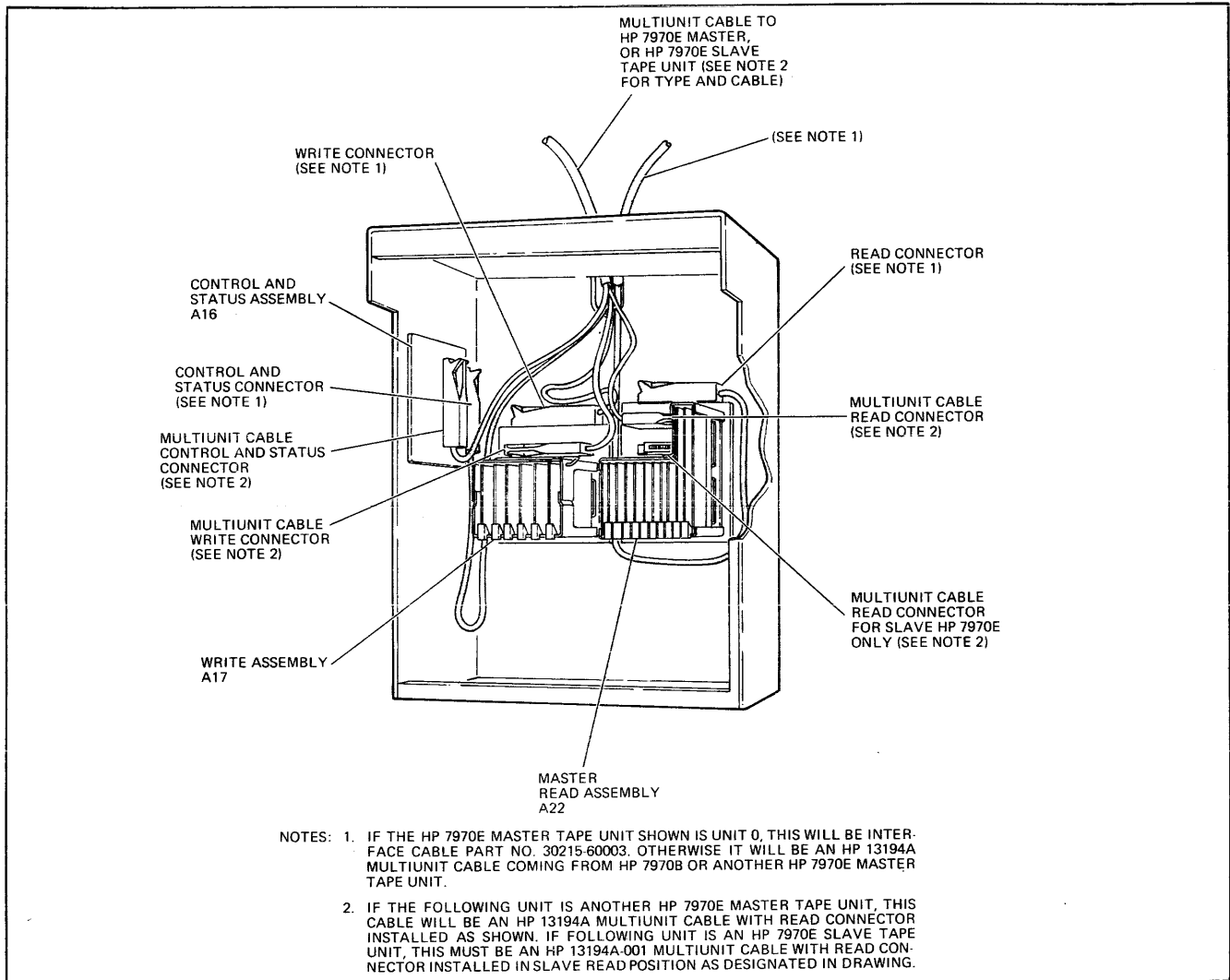
2180-16A

Figure 4-3. Basic Subsystem, HP 7970B Digital Magnetic Tape Unit
Interface Cable Connection Points



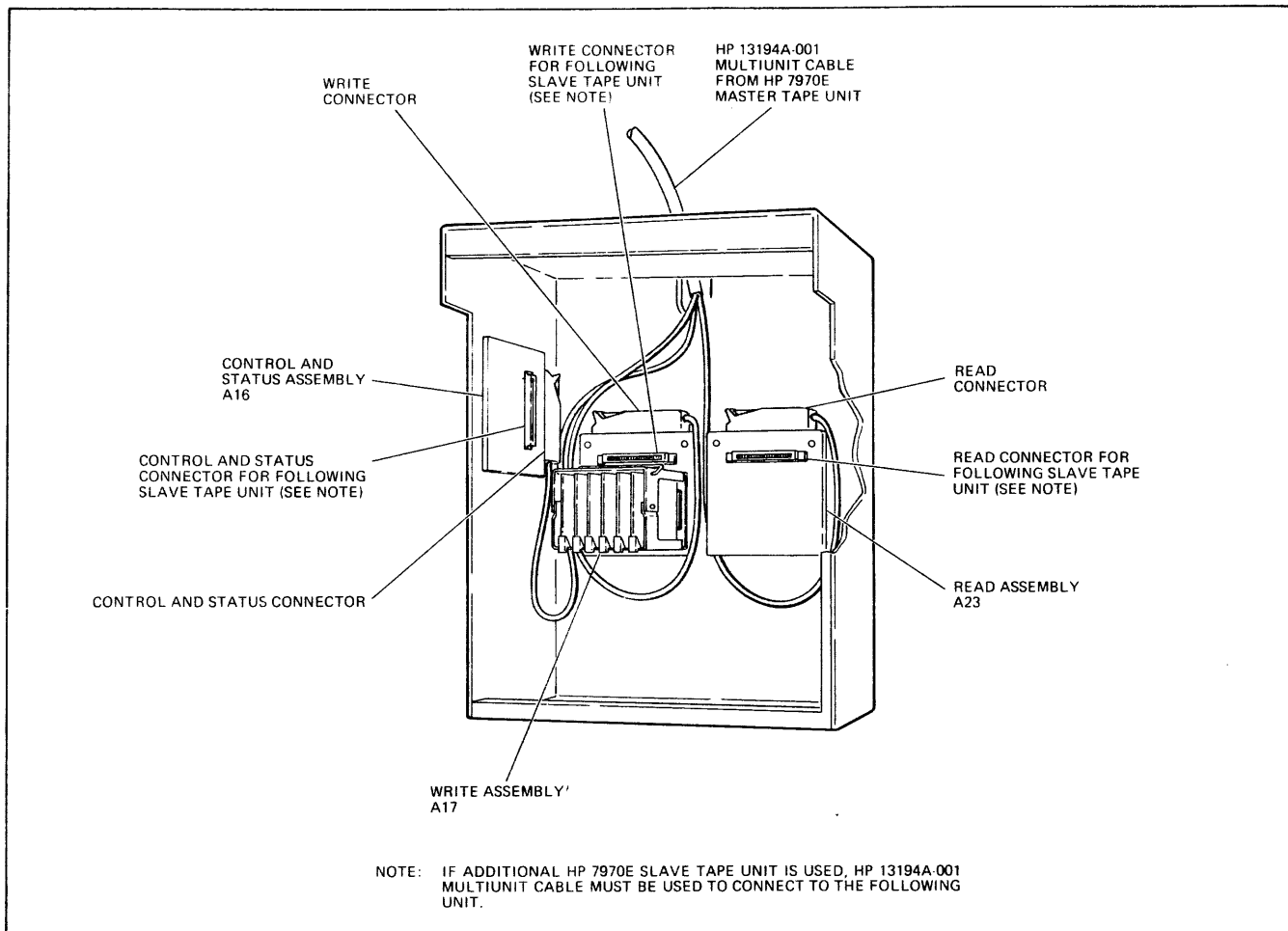
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Figure 4-4. Additional HP 7970B Digital Magnetic Tape Unit Cable Connection Points



2180-22A

Figure 4-5. Master HP 7970E Digital Magnetic Tape Unit (PE) Cable Connection Points



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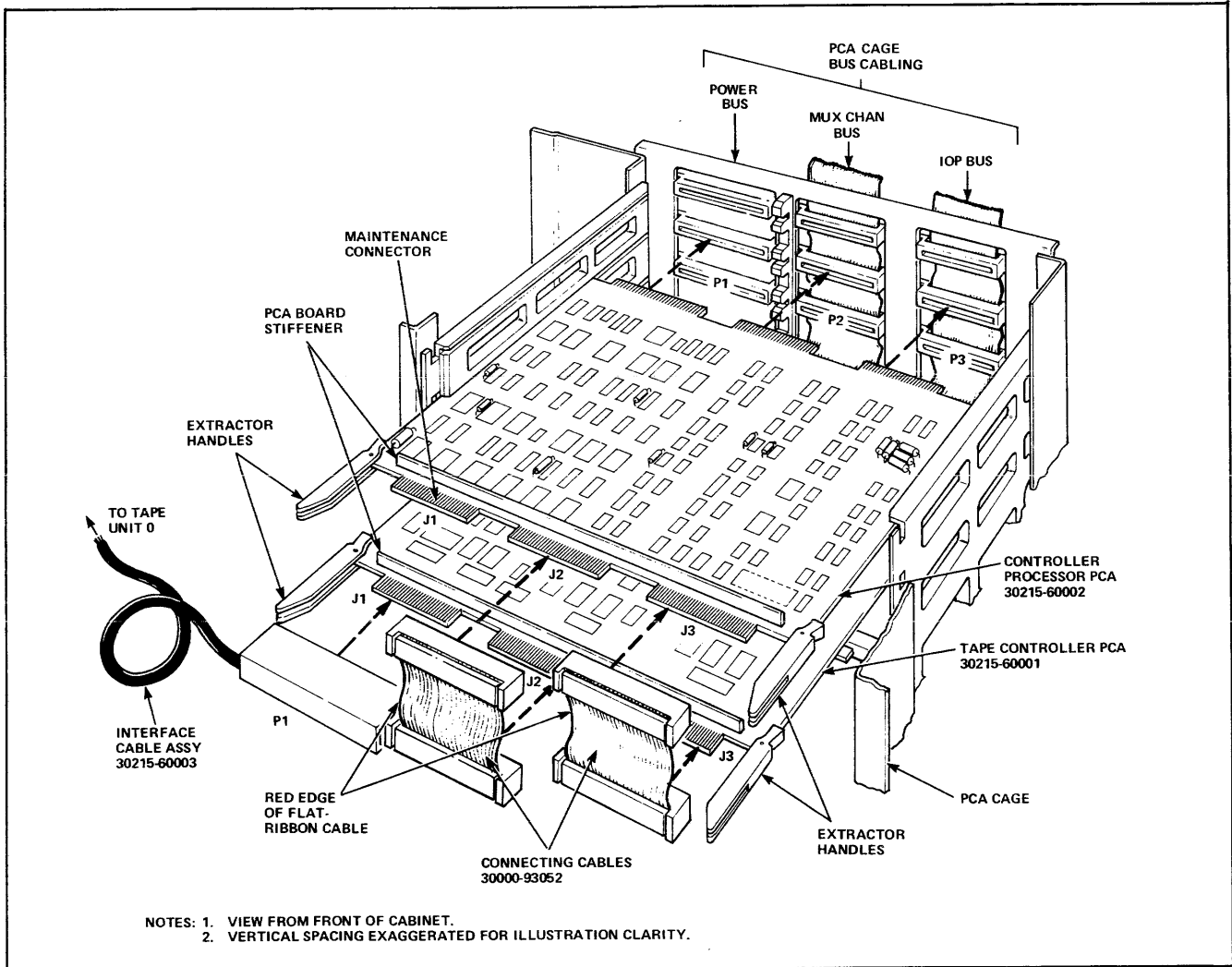
Figure 4-6. Slave HP 7970E Digital Magnetic Tape Unit (PE) Cable Connection Points

4-18. INTERFACE PCA POSITIONING AND CABLE CONNECTIONS. Figure 4-7 shows the normal position of the tape controller and controller processor printed-circuit assemblies in the system PCA cage. Ensure that these positions are maintained and cables connected as shown when performing preventive maintenance or troubleshooting procedures. The controller processor maintenance interface PCA may be installed in any vacant slot in the same PCA cage. The printed-circuit assemblies of the subsystem may be placed on extenders for maintenance and troubleshooting. When re-installing the subsystem printed-circuit assemblies, proceed as follows:

- a. Pull the extractor handles on the printed-circuit assemblies to the straight-out position as shown in figure 4-7.

CAUTION

Ensure that the plastic extractor handles are moved to the straight-out position before sliding the printed-circuit assemblies into final position. Otherwise handles may be broken or the PCA may be cracked.



2180-15

Figure 4-7. HP 30215A Magnetic Tape Unit Interface PCA Position and Connect Details

- b. Slide printed-circuit assemblies, component-side up, into two adjacent slots with the controller processor PCA in upper position.

CAUTION

Do not force or bend printed-circuit assemblies when re-installing. Slide straight in or damage to printed-circuit assemblies may result.

- c. Lock extractor handles into slots on either side of PCA module.

4-19. TAPE CONTROLLER PCA JUMPERS. The four areas for jumper installation on the tape controller PCA are shown in figure 4-8. See table 4-1 for explanations of jumper use. Jumpers should be in place in required positions to be compatible with the existing HP 3000 Computer System addressing and interrupt structure. Refer to HP 3000 Computer System Configuration Package to ensure compatibility if it becomes necessary to move these jumpers for maintenance purposes. The multiplexer channel service request jumper should not be in the same position as that occupied by a multiplexer channel service request jumper of another subsystem served by the same multiplexer channel PCA. Device number jumpers should not be installed in the same positions occupied by device number jumpers of any other subsystem in this computer system.

Table 4-1. Tape Controller PCA Jumper Descriptions

JUMPER NAME	ASSIGNED DESIGNATION	DESCRIPTION
Multiplexer Channel Service Request	W1	Selects one of a possible 16 service request lines to the multiplexer channel PCA when installed.
Interrupt Mask Group	W2	Assigns the subsystem to an HP 3000 Computer System interrupt mask group when installed in positions 0 through 15, or enables subsystem response to all Set Mask commands when installed in the ENABLE position, or disables subsystem response to all Set Mask commands when installed in DISABLE position.
DRT Address Odd Parity	W3	Used with device number jumpers, explained below, to ensure odd parity of the bit pattern representing the DRT address that is transmitted on the IOP data bus to memory.

Table 4-1. Tape Controller PCA Jumper Descriptions (Continued)

JUMPER NAME	ASSIGNED DESIGNATION	DESCRIPTION
Device Number	W5 thru W11	Bit pattern generated by absence or presence of jumper connections corresponds to the subsystem device number or device interrupt number. Also used to generate the DRT address for this device. When all jumpers are removed the device is number 127 (177 ₈) in the device reference table. (Entry 123 ₁₀ at address 774 ₈ .) The device number jumpers and the odd parity jumper, explained previously, comprise a total of nine* jumper positions. There must be an <i>even</i> number of jumpers installed in these total available positions including W4 position to cause odd parity in memory. Each vacant jumper position causes logical 1 in the DRT address in memory. In the example shown in figure 4-8, note that jumpers W10(2 ¹) and W9(2 ²) are removed. This identifies this subsystem as device number 6(6 ₈), fourth DRT entry, with the first of its four table entries located at address 30 ₈ .

*W4 position is designated Direct Command Flag. Use W5 as most significant bit.

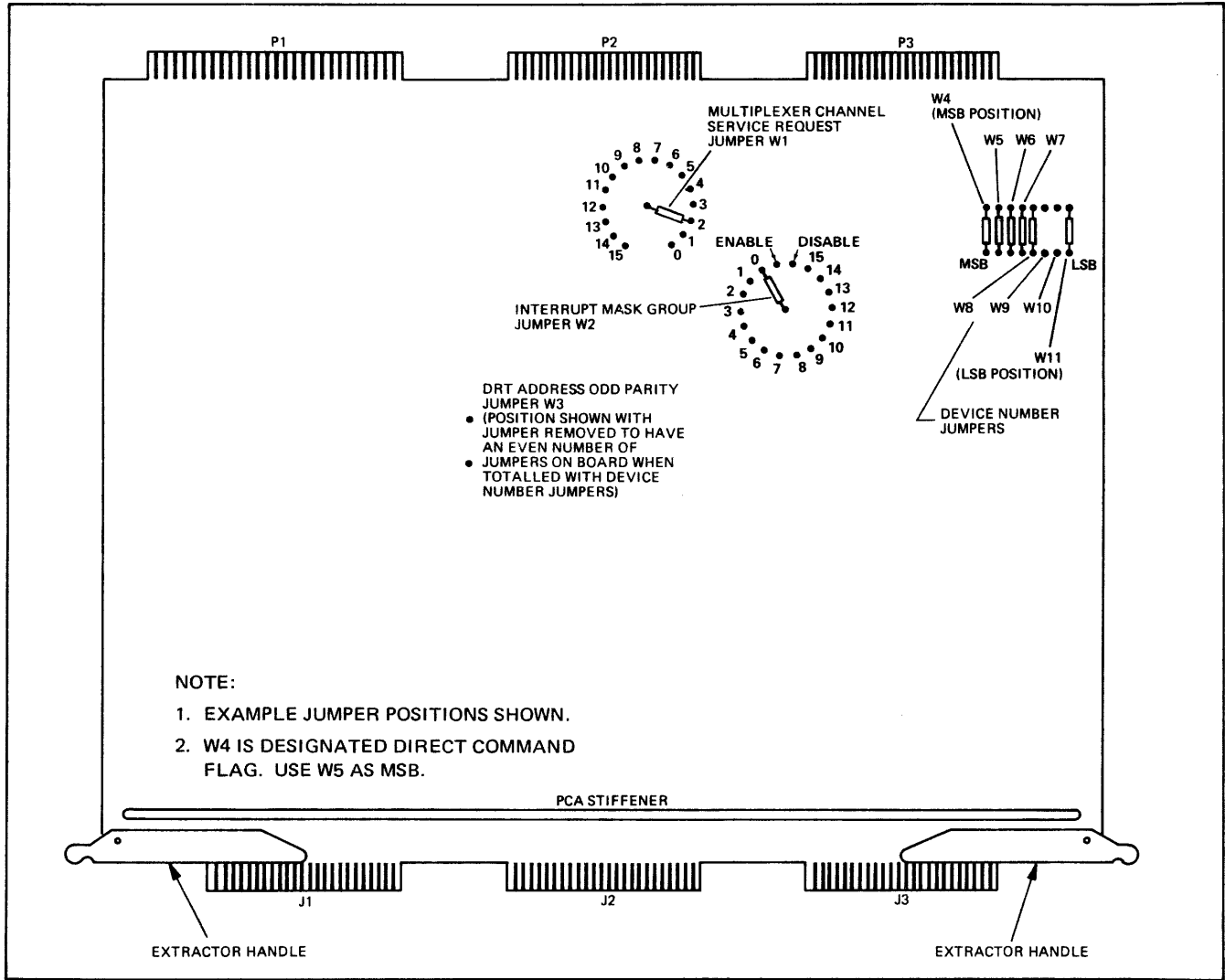
4-20. **CONTROLLER PROCESSOR PCA CRYSTAL LOCATION.** The 9.216-MHz crystal for nine track magnetic tape subsystem operation at 45 ips (114 cm/sec) is located as shown in figure 4-9. Installation of maintenance equipment makes it possible to override control established by the normal crystal oscillator. Ensure the proper crystal is installed if it is removed for any reason during maintenance.

4-21. PREVENTIVE MAINTENANCE.

4-22. Paragraph 4-23 provides scheduling information for preventive maintenance. Paragraph 4-25 outlines applicable routines.

4-23. SCHEDULED ITEMS.

4-24. Section III in part one of the tape unit operating and service manual contains schedules and procedures to be used for the tape unit(s). Insofar as possible preventive maintenance schedules for the subsystem should coincide with HP 3000 Computer System schedules. Preventive maintenance procedures for the HP 30215A Magnetic Tape Unit Interface printed-circuit assemblies should be performed at the same time that tape unit preventive maintenance is accomplished.



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Figure 4-8. Tape Controller PCA, Jumper Locations

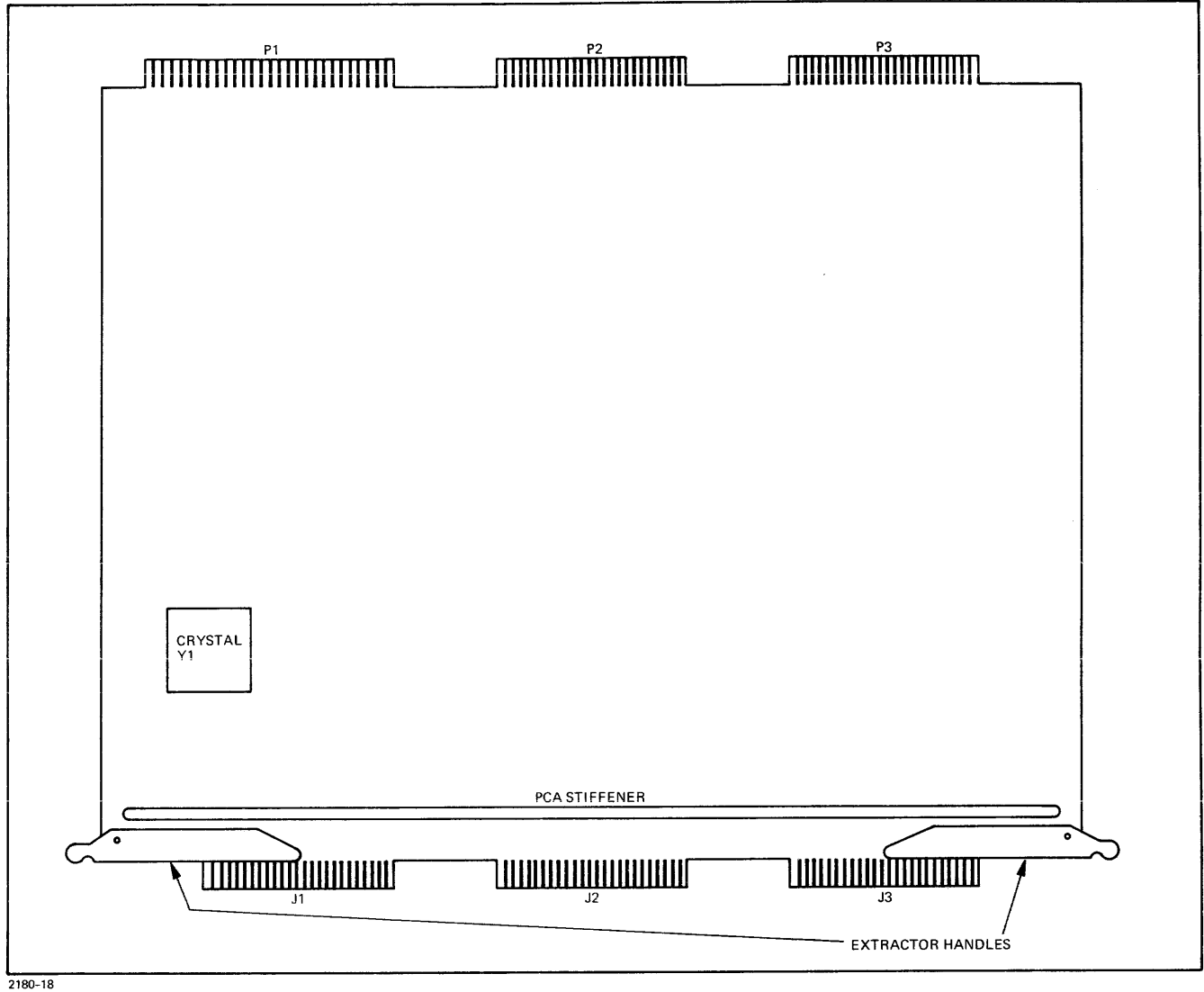


Figure 4-9. Controller Processor PCA, Crystal Location

4-25. SERVICING ROUTINES.

4-26. Preventive maintenance for the HP 30215A Magnetic Tape Unit Interface printed-circuit assemblies includes keeping them clean. Ensure that scraps of wire or other metal, accidentally dropped when other maintenance has been performed in the PCA, do not remain on either PCA. Ensure that interface cables, and cables between the PCA's are not subjected to excessive bending or wear, particularly at the connectors.

4-27. Tapes remaining stationary at the load point for considerable lengths of time when the tape unit is running may slip in one spot due to accumulation of tape lubricant on the capstan. To prevent this, keep the tape unit capstan clean in accordance with procedures outlined in the tape unit operating and service manual. It may also help to periodically change the position of the BOT reflective marker.

4-28. TROUBLESHOOTING.

4-29. The troubleshooting philosophy for the HP 30115A Magnetic Tape Subsystem is as follows:

- a. Ensure that the recording difficulties are not caused by a defective or worn magnetic tape.
- b. If it is available, check the system log for any past history occurrence of similar difficulty and any pertinent operator's comments.
- c. Analyze any results obtained from the on-line SDM test, part no. 30115-90003 in the HP 3000 Manual of On-Line Diagnostics.
- d. Run the microdiagnostics, described in the microdiagnostic program listings for the magnetic tape subsystem, and analyze the results.
- e. Use the information contained in this section to isolate the fault to a portion of the hardware, then to a replaceable component. Microdiagnostics should be used to at least isolate the fault to a PCA, cables, or to the tape unit. See the tape unit operating and service manual for further trouble-isolation procedures in that unit.

4-30. The remaining portion of this paragraph contains the reference information and test and analysis procedures needed to troubleshoot the overall HP 30115A Magnetic Tape Subsystem and the HP 30215A Magnetic Tape Unit Interface assemblies in particular.

4-31. REFERENCE INFORMATION.

4-32. The following reference information is needed to troubleshoot the subsystem in addition to on-line diagnostic and micro-diagnostic information.

- a. Logic diagrams.
- b. Connecting cable and PCA pin/signal information.
- c. The microprogram listing and flowcharts.

- d. Timing diagrams of subsystem operation.
- e. Integrated circuit pack information.

4-33. Simplified Diagrams for the magnetic tape subsystem printed-circuit assemblies are contained in set number SD-163, part no. 30115-90002, of the *HP 3000 Computer System Simplified Diagrams Manual*. Detailed logic diagrams are contained in set numbers DD-607 and DD-608, part no.'s 30215-90001 and 30215-90003 of the *HP 3000 Computer System Detailed Diagrams Manual*. The detailed diagrams manual also contains diagrams for integrated-circuit packs and part location data. Parts information for servicing and replacement, after trouble isolation, is contained in the *HP 3000 Computer System Illustrated Parts Breakdown Manual (IPB)*. As previously mentioned troubleshooting procedures for the HP 7970B Digital Magnetic Tape Unit will be found in operating and service manual part no. 07970-90383. Troubleshooting procedures for master and slave HP 7970E Digital Magnetic Tape Units will be found in operating and service manual part no. 07970-90765.

4-34. TEST PROCEDURES.

4-35. On-line diagnostics, run by the System Diagnostic Monitor (SDM), and microdiagnostics are the means employed for troubleshooting the magnetic tape subsystem. There are no stand-alone diagnostics for this subsystem. Procedures used for running the Controller Processor microdiagnostics are all included in the I/O microprocessor microdiagnostic program listings. Maintenance setup instructions for the equipment listed in paragraph 4-10 are included in *Operator's Manual, 30350A Auxiliary Control Panel and 30352A Hardware Maintenance Panel*, part no. 30352-90001. A cold dump of the HP 3000 Computer System must precede use of the microdiagnostics. Refer to software operating procedures and also see that cold dump summary in section II of this manual. After tests have been run, refer to trouble analysis information in paragraph 4-36.

4-36. TROUBLE ANALYSIS.

4-37. All mechanical and electrical functions of the subsystem should be checked under dynamic conditions where possible. Repair personnel must be able to recognize normal subsystem operation through the use of software routines and previous sections of this and the tape unit manual. With this background, malfunctions can be recognized and the trouble isolated to a function using the microdiagnostics in conjunction with the on-line diagnostics. The results of on-line and microdiagnostic tests should prove conclusively to repair personnel whether or not the subsystem is operating properly for data transfer modes and whether or not it is responding to all motion commands.

4-38. Analyze message printouts and the results of tests accomplished using the maintenance panels. If the subsystem will operate properly in diagnostic modes but will not perform correctly in normal operation, the ROM integrated-circuit packs holding the subsystem microprogram may have developed a fault. See the servicing data microprogram listing and flowcharts in the following paragraph. Status register integrated circuits U166 and U167 should be used in conjunction with appropriate sections of the microdiagnostic and status data in section II to isolate malfunctions. Do not overlook the interface cable and card connectors

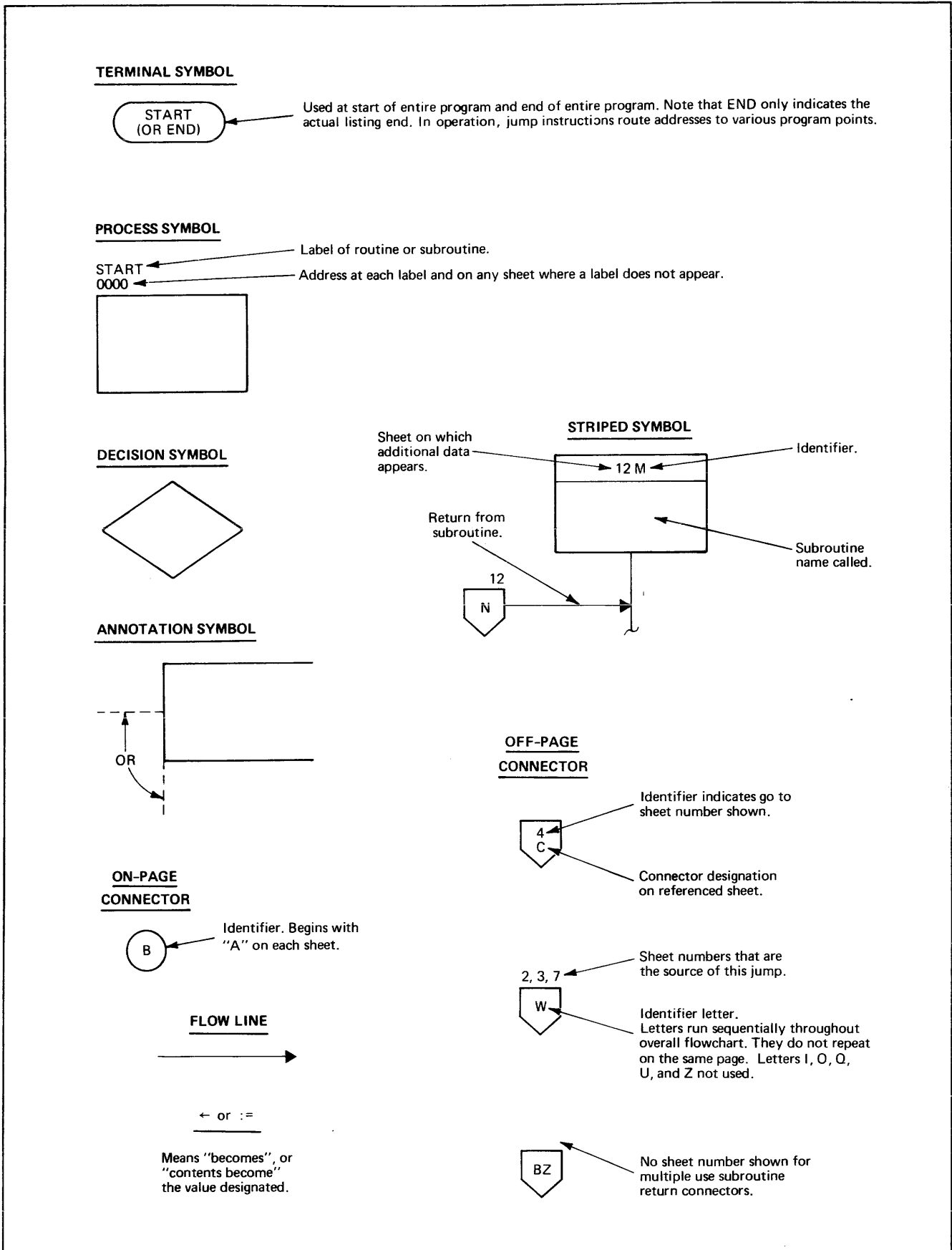
as a source of trouble. Troubleshooting usually requires that the PCA under test be placed on a PCA extender. Ensure that the extender is in good condition and supported from the PCA cage. Also ensure that a good maintenance interface PCA is being used. Refer to the servicing data included under paragraph 4-39 for pin and signal information.

4-39. SERVICING DATA.

4-40. The data listed below is included as an aid in isolating HP 30115A Magnetic Tape Subsystem faults. This data is also reference from other sections of the manual.

- a. Flowchart conventions, figure 4-9A.
- b. Table of flowchart conventions, table 4-1A.
- c. Microprogram flowcharts, figure 4-10.
- d. Consolidated microcoding sheet, figure 4-11.
- e. Microprogram Address-to-Label Index, table 4-2.
- f. Microprogram Label, Flowchart, Address, Subroutine Index, table 4-3.
- g. Microprogram listing, table 4-4.
- h. Timing diagrams, figures 4-12 through 4-14.
- i. Connector pin/signal tables, tables 4-5 through 4-8.
- j. Pin indexing information, figure 4-15.

4-41. Descriptive instructions for the microcoding information are included in section III. See paragraph 4-31 for additional data. Wiring information for cables is included in the repair paragraph.



2180-118

Figure 4-9A. Symbol Conventions Used in Flowcharts

Table 4-1A. Flow Chart Definitions and Conventions

ITEM	CHARACTERISTIC
DEFINITIONS	
AUX	Auxiliary.
CLK	Clock.
CMD	Command. See section II for a list of commands and definitions.
CNTR	Controller Processor counter.
Controller	The interface (PCAs).
CRCC	Cyclic Redundancy Check Character.
CRCR	Cyclic Redundancy Check Register.
DEC	Decrement the value stored in the counter by a count of one.
DSR	Device Service Request (FF).
ENB	Enable.
EOB	End of Block.
FF	Flip-Flop.
File Mark	Synonomous with tape mark. See section II for characteristics.
FLG (F0) thru F17)	Flags input to the Controller Processor. See listing for definitions.
FWD	Forward.
INT	Interrupt.
Lower Byte	MIO bus bits 8 through 15.
LRCC	Longitudinal Redundancy Check Character.
PAR	Parity.
RCS	Reverse Condition Sense (complement).
RD	Read.
RDBKD	Read reverse subgroup commands.
RDFWD	Read forward subgroup commands.
REV	Reverse.
REW	Rewind.

Table 4-1A. Flowchart Definitions and Conventions (Continued)

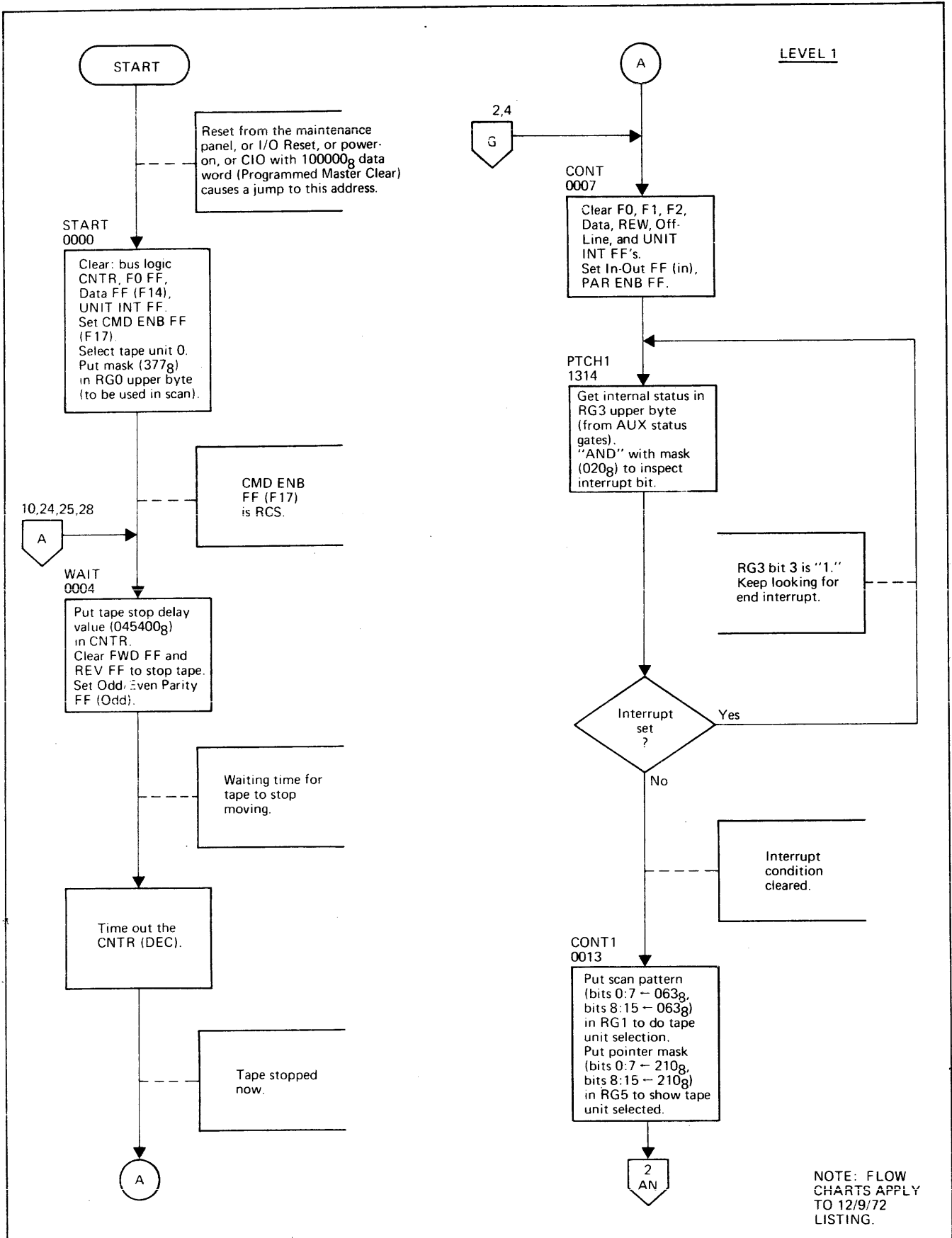
ITEM	CHARACTERISTIC												
DEFINITIONS (Cont.)													
RG0 thru RG5	Controller Processor registers.												
Tape Mark	Synonomous with File Mark. Tape Mark is generally used in this manual. See section II for characteristics.												
Upper Byte	MIO bus bits 0 through 7.												
WRFWD	Write forward subgroup commands.												
WRT	Write.												
XFER	Transfer.												
x:y	x through y (i.e. bits 12:15 or bits 0:7 (upper byte)).												
000012 ₈	Octal values of constants entered in the counter or register (full word).												
037 ₈	Octal value of constant entered in a register. In this case upper of lower byte must be specified.												
CONVENTIONS													
Address	Octal addresses appear at all labels. Addresses are also shown at the top of flowchart columns to avoid confusion when no label appears on the sheet. Addresses are also shown on the flowchart where operations depicted occurs at any address that is not sequential to the last operation.												
Annotations	Abbreviated decision information is generally amplified on one of the decision legs with the name of the flag, flip-flop, or use of F0, F1, or F2 for the particular decision. Off-page connectors are annotated with the label name of the jump location.												
Clearing	An "XOR" of register 3 (RG3) on the A and B buses is used frequently to clear registers and/or the counter. When RG3 is "XOR'd" with itself the bits will be a pattern match thus, logical 0's will be loaded in the target register.												
Connectors	Generally, off-page and on-page connectors are shown with the connectors to the right or bottom of the flow for exits. Entry points and returns to the flow are shown with connectors to the top or left.												
Micro-instructions	<p>Twenty one of the Controller Processor microinstructions are used for the nine-track magnetic tape microprogram. They are:</p> <table data-bbox="613 1801 1268 1923" style="margin-left: auto; margin-right: auto;"> <tbody> <tr> <td>ADD</td> <td>JFS</td> <td>OTI</td> </tr> <tr> <td>ADI</td> <td>JMP</td> <td>PSA</td> </tr> <tr> <td>AND</td> <td>JMZ</td> <td>PSB</td> </tr> <tr> <td>ANI</td> <td>JOV</td> <td>PSI</td> </tr> </tbody> </table>	ADD	JFS	OTI	ADI	JMP	PSA	AND	JMZ	PSB	ANI	JOV	PSI
ADD	JFS	OTI											
ADI	JMP	PSA											
AND	JMZ	PSB											
ANI	JOV	PSI											

Table 4-1A. Flowchart Definitions and Conventions (Continued)

ITEM	CHARACTERISTIC																																	
CONVENTIONS (Cont.)																																		
Micro-instructions (Cont.)	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 33%;">CAL</td> <td style="width: 33%;">JSZ</td> <td style="width: 33%;">RTN</td> </tr> <tr> <td>IOC</td> <td>JXZ</td> <td>XOI</td> </tr> <tr> <td>IOI*</td> <td>NOP</td> <td>XOR</td> </tr> </table> <p>*The IOI is not a true "inclusive OR" operation. The quantities called are actually "OR'ed" only.</p> <p>e.g.</p> <table border="1" style="margin-left: auto; margin-right: auto; text-align: center;"> <tr> <td></td> <td></td> <td style="border: none;">or</td> <td style="border: none;">or</td> </tr> <tr> <td style="border: none;">A</td> <td style="border: none;">B</td> <td style="border: none;">X</td> <td style="border: none;">X</td> </tr> <tr> <td style="border: 1px solid black;">0</td> <td style="border: 1px solid black;">0</td> <td style="border: 1px solid black;">0</td> <td style="border: 1px solid black;">1</td> </tr> <tr> <td style="border: 1px solid black;">0</td> <td style="border: 1px solid black;">1</td> <td style="border: 1px solid black;">1</td> <td style="border: 1px solid black;">0</td> </tr> <tr> <td style="border: 1px solid black;">1</td> <td style="border: 1px solid black;">0</td> <td style="border: 1px solid black;">1</td> <td style="border: 1px solid black;">0</td> </tr> <tr> <td style="border: 1px solid black;">1</td> <td style="border: 1px solid black;">1</td> <td style="border: 1px solid black;">1</td> <td style="border: 1px solid black;">1</td> </tr> </table>	CAL	JSZ	RTN	IOC	JXZ	XOI	IOI*	NOP	XOR			or	or	A	B	X	X	0	0	0	1	0	1	1	0	1	0	1	0	1	1	1	1
CAL	JSZ	RTN																																
IOC	JXZ	XOI																																
IOI*	NOP	XOR																																
		or	or																															
A	B	X	X																															
0	0	0	1																															
0	1	1	0																															
1	0	1	0																															
1	1	1	1																															
Operations	In general, the use of the word "get" in the flowcharts, means an external action to the Controller Processor. "Put" means an internal operation with the immediate operand or the registers.																																	
Output	An OTI microinstruction with an immediate operand of 377_8 indicates that only the destination code is used to control magnetic tape controller PCA logic. The octal value of the immediate operand is the complement of the actual binary pattern (i.e. $\overline{377}_8 = 000_8$).																																	
Status	The internal status word (obtained from the AUX Status gates) appears on the MIO bus upper byte in the following format: <table style="margin-left: 40px; margin-top: 10px;"> <tr> <td>M0</td> <td>\overline{IDB} (1600 cpi)</td> </tr> <tr> <td>M1</td> <td>\overline{TM} (1600 cpi)</td> </tr> <tr> <td>M2</td> <td>\overline{MTE} or \overline{STE} (1600 cpi)</td> </tr> <tr> <td>M3</td> <td>INT ACTIVE or Interrupt Request</td> </tr> <tr> <td>M4</td> <td>$\overline{SIO OK}$</td> </tr> <tr> <td>M5</td> <td>\overline{SFP} (File Protect Status)</td> </tr> <tr> <td>M6 and M7</td> <td>(Tied low)</td> </tr> </table>	M0	\overline{IDB} (1600 cpi)	M1	\overline{TM} (1600 cpi)	M2	\overline{MTE} or \overline{STE} (1600 cpi)	M3	INT ACTIVE or Interrupt Request	M4	$\overline{SIO OK}$	M5	\overline{SFP} (File Protect Status)	M6 and M7	(Tied low)																			
M0	\overline{IDB} (1600 cpi)																																	
M1	\overline{TM} (1600 cpi)																																	
M2	\overline{MTE} or \overline{STE} (1600 cpi)																																	
M3	INT ACTIVE or Interrupt Request																																	
M4	$\overline{SIO OK}$																																	
M5	\overline{SFP} (File Protect Status)																																	
M6 and M7	(Tied low)																																	
Timing Functions	<p>In the nine-track magnetic tape microprogram, the JXZ (Jump if the counter is zero) is always used with RCS. That is "Jump if the counter is <i>not</i> zero."</p> <p>Timing for any constant loaded into the counter (CNTR) may be calculated from information in the flowcharts since the octal value of the entire counter entry is always stated. The upper or lower byte need not be considered. The procedure is as follows:</p>																																	

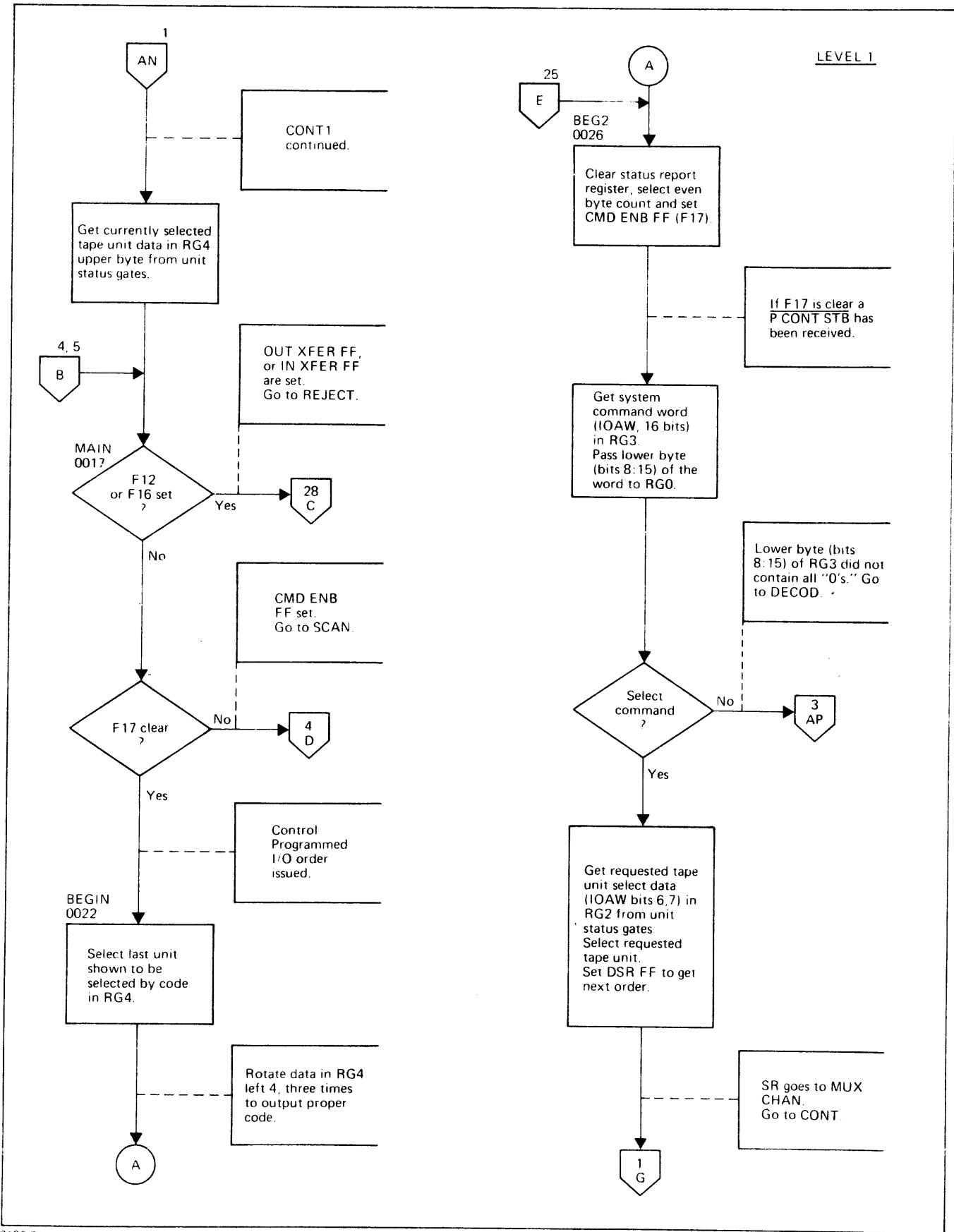
Table 4-1A. Flowchart Definitions and Conventions (Continued)

ITEM	CHARACTERISTIC																																																			
CONVENTIONS (Cont.)																																																				
Timing Functions (Cont.)	<p>a. Using the counter place value positions (shown below) calculate the number of cycles the counter must decrement. For example, if the value 000615_8 is shown to be loaded in the counter, total cycles to decrement equals 397.</p> <table border="1" data-bbox="505 562 1409 772"> <thead> <tr> <th></th> <th>BITS 0</th> <th>1</th> <th>2</th> <th>3</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> <th>8</th> <th>9</th> <th>10</th> <th>11</th> <th>12</th> <th>13</th> <th>14</th> <th>15</th> </tr> </thead> <tbody> <tr> <td>COUNTER VALUES</td> <td>32,768</td> <td>16,384</td> <td>8192</td> <td>4096</td> <td>2048</td> <td>1024</td> <td>512</td> <td>256</td> <td>128</td> <td>64</td> <td>32</td> <td>16</td> <td>8</td> <td>4</td> <td>2</td> <td>1</td> </tr> <tr> <td>VALUE LOADED (000615_8)</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>0</td> <td>0</td> <td>1</td> <td>1</td> <td>0</td> <td>1</td> </tr> </tbody> </table> <p>b. The product of total cycles and the cycle time for the Magnetic Tape Subsystem Controller Processor equals total time delay. For example, 397 cycles x 434 nanoseconds = 172.298 or 172 microseconds.</p> <p>c. Note, in timing considerations, that 64 (100_8) controller processor instruction times equal one 800 cpi character time.</p>		BITS 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	COUNTER VALUES	32,768	16,384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	VALUE LOADED (000615_8)	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1
	BITS 0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15																																				
COUNTER VALUES	32,768	16,384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1																																				
VALUE LOADED (000615_8)	0	0	0	0	0	0	0	1	1	0	0	0	1	1	0	1																																				



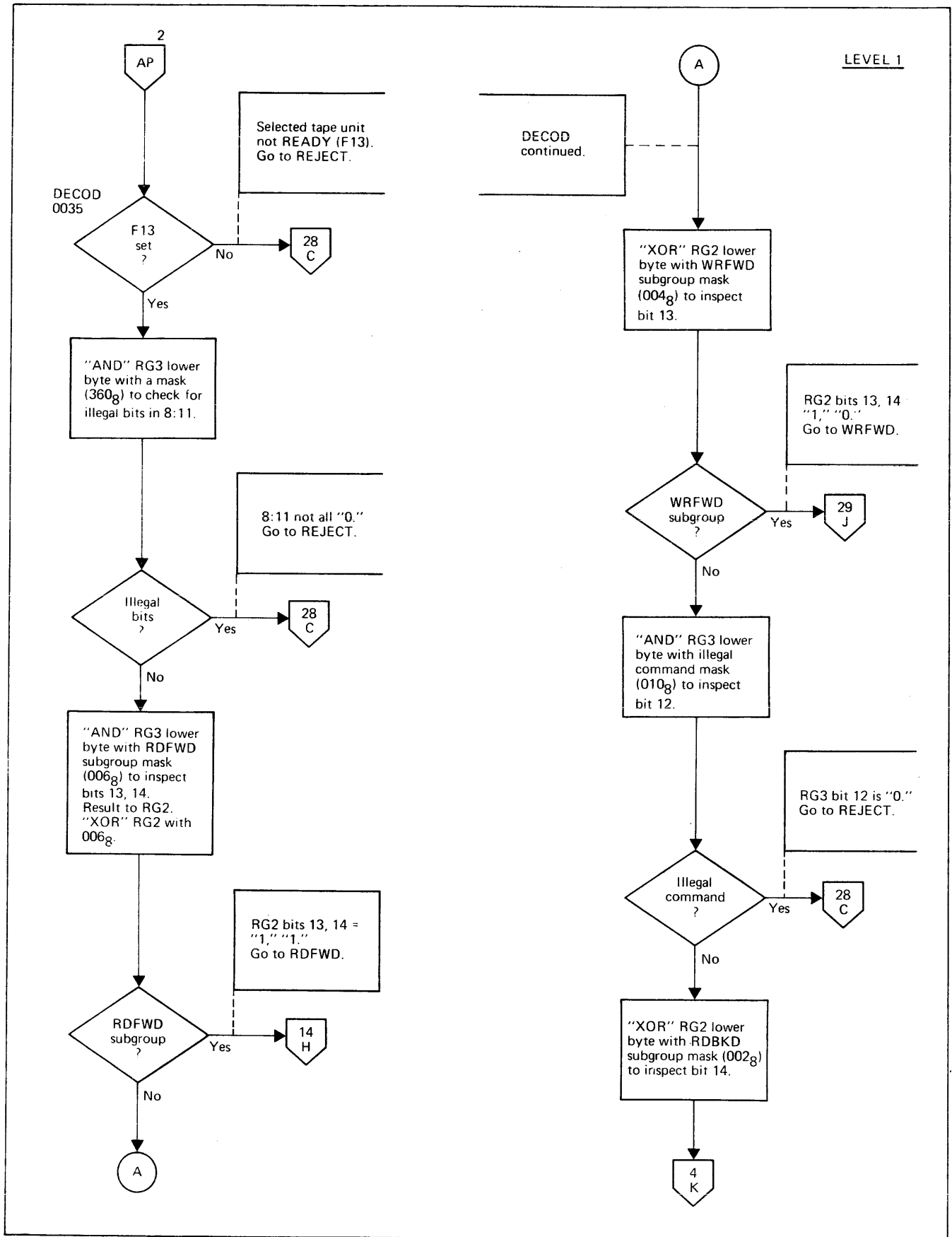
2180 24B

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 1 of 58)



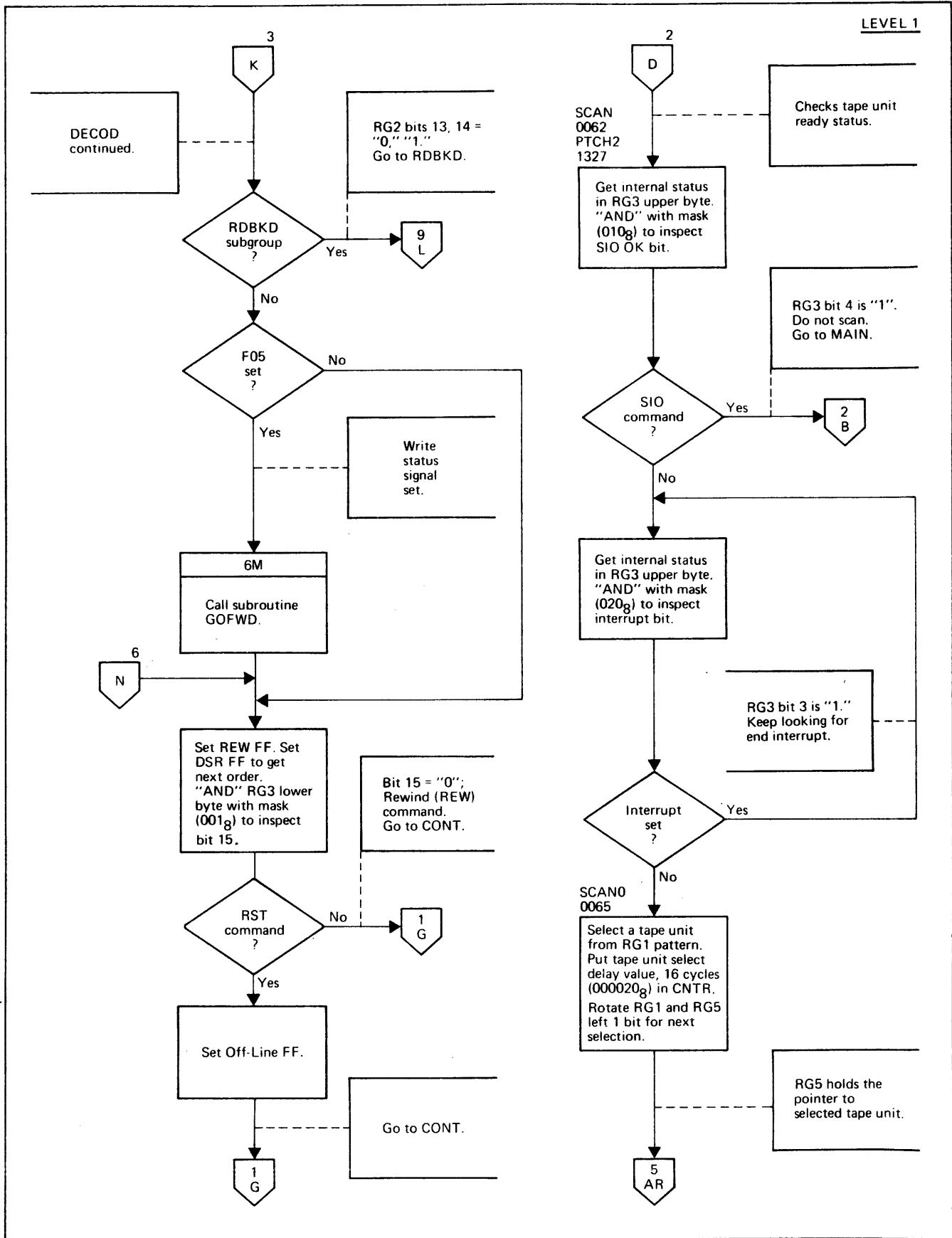
2180 61

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 2 of 58)



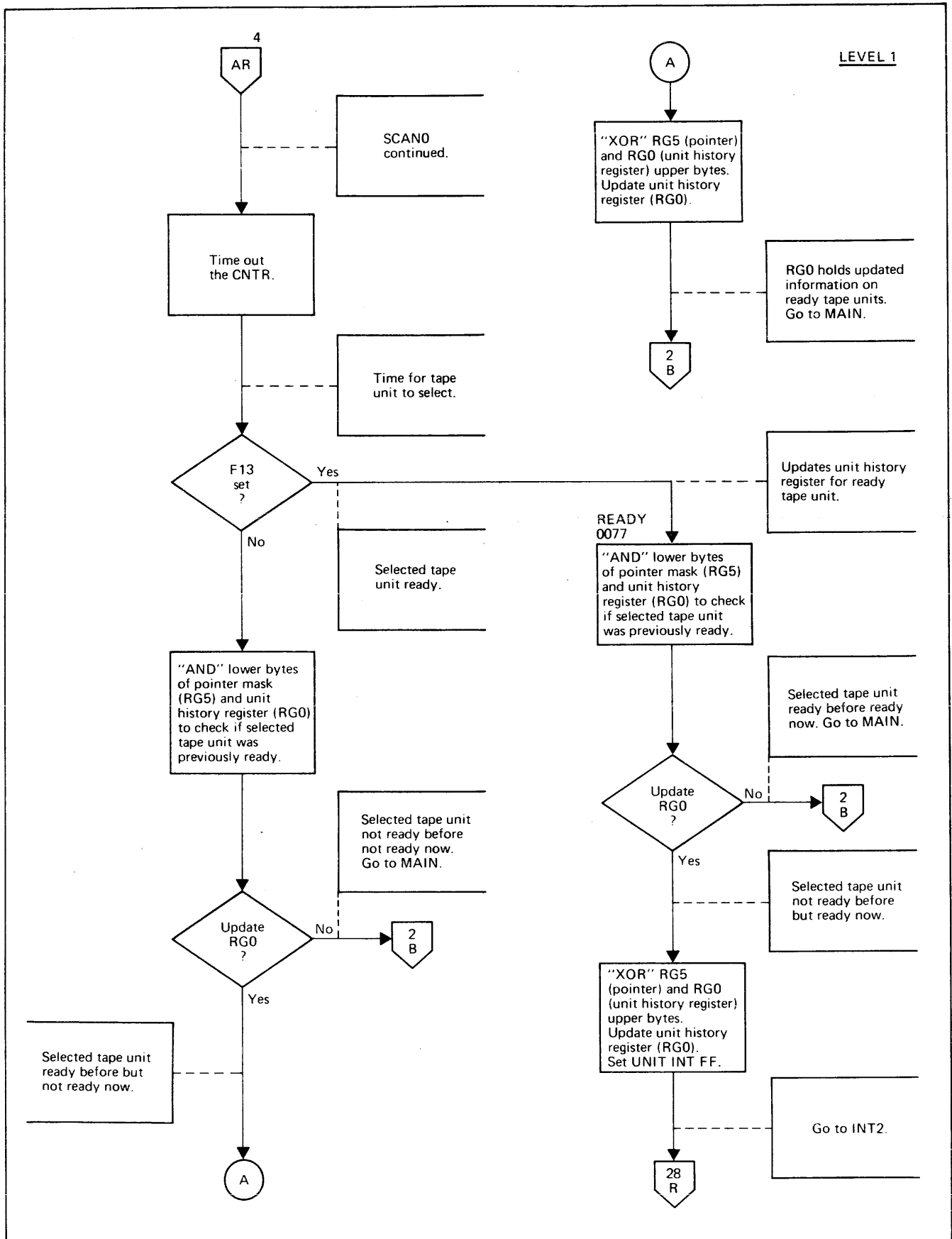
2180 62

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 3 of 58)



2180 63

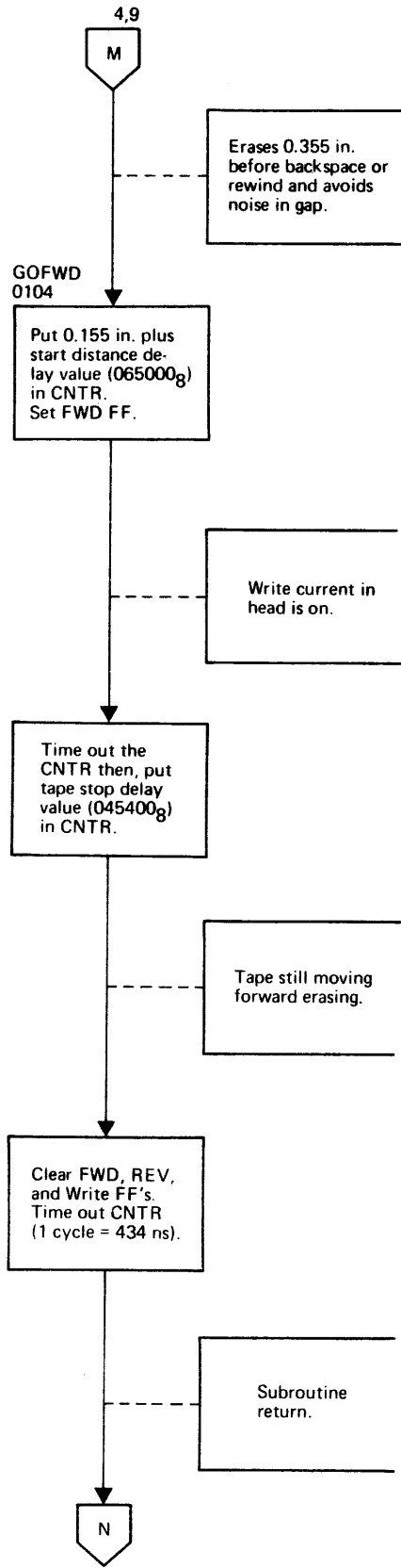
Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 4 of 58)



2180 64

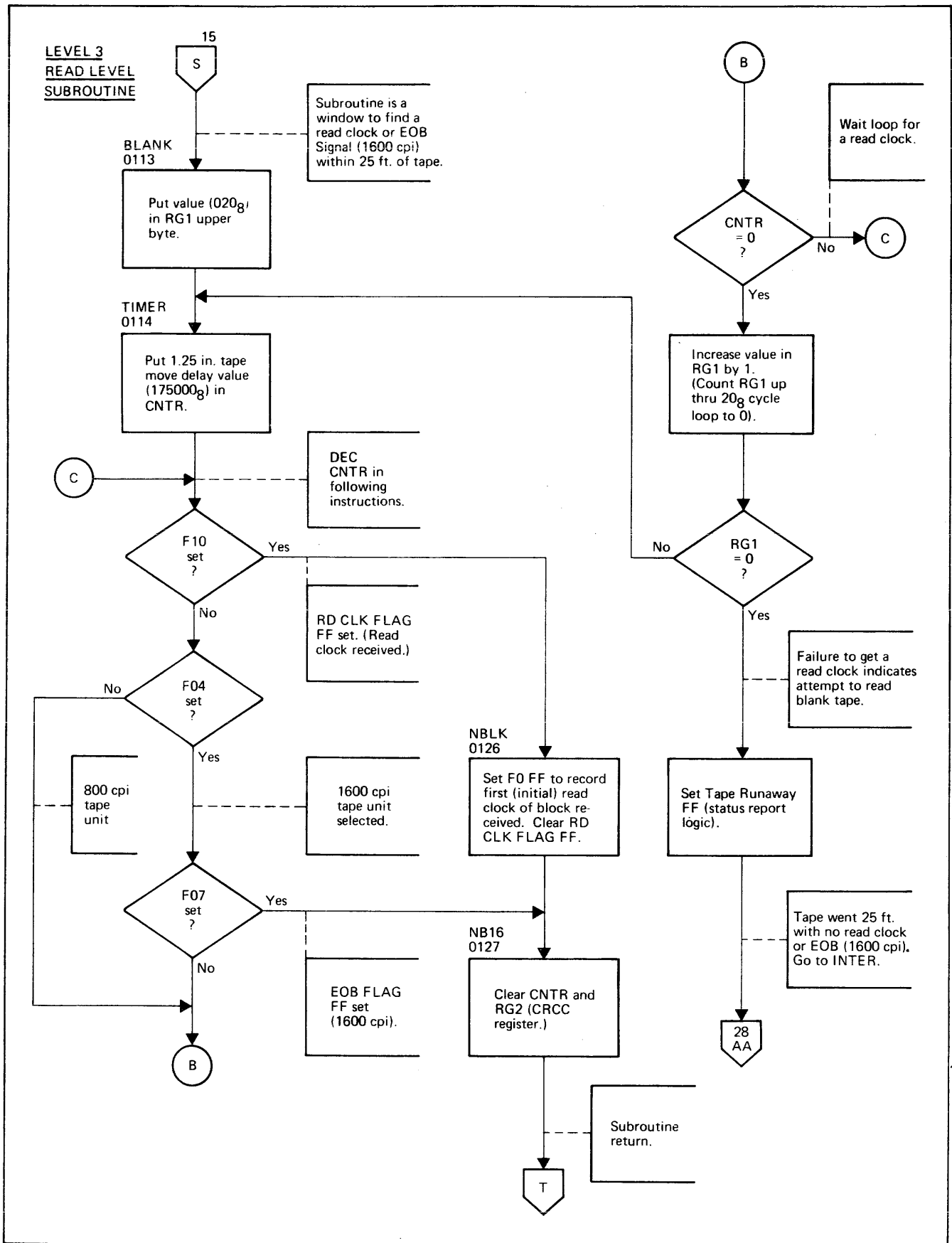
Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 5 of 58)

LEVEL 3
WRITE LEVEL
SUBROUTINE



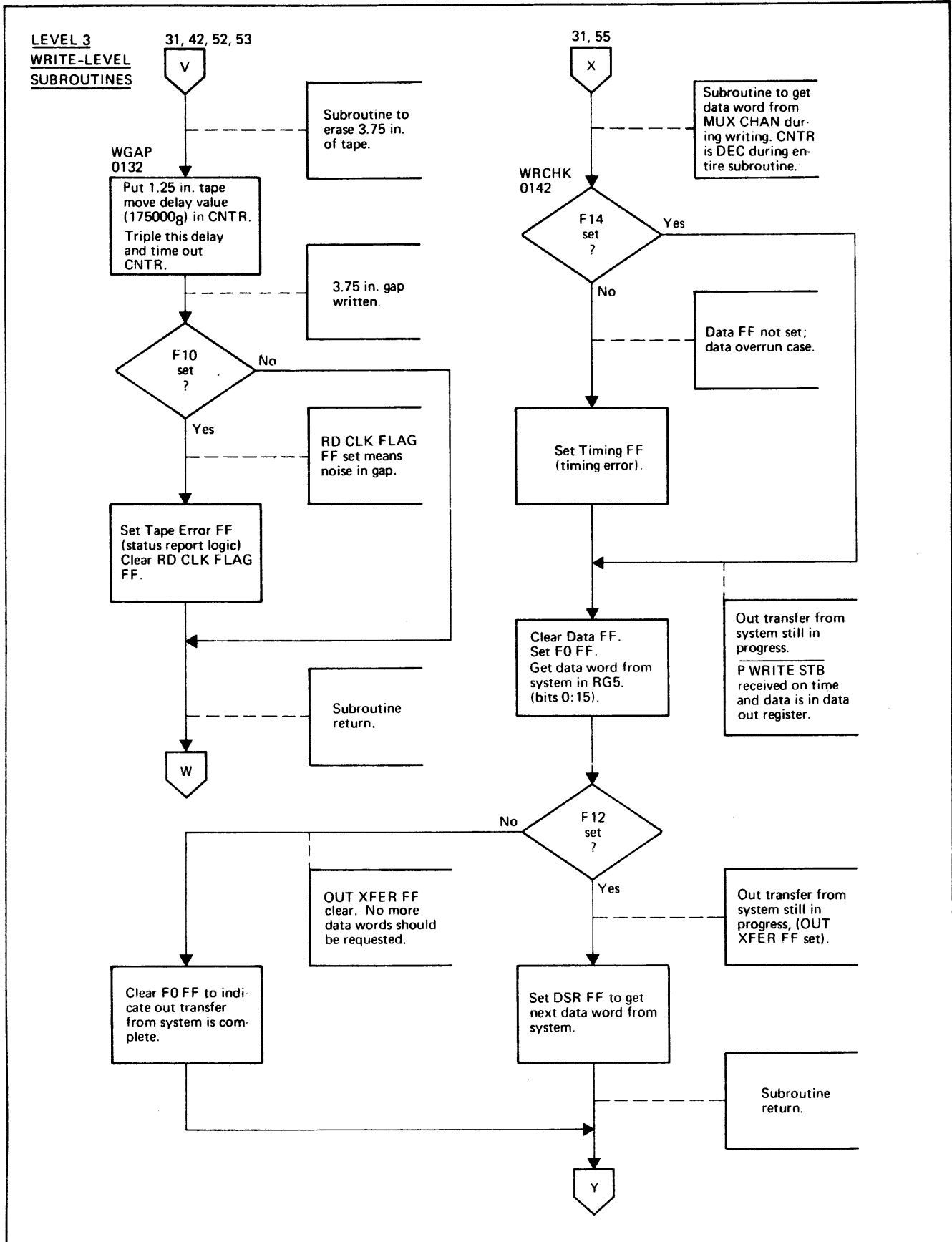
2180 65

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 6 of 58)



2180-66

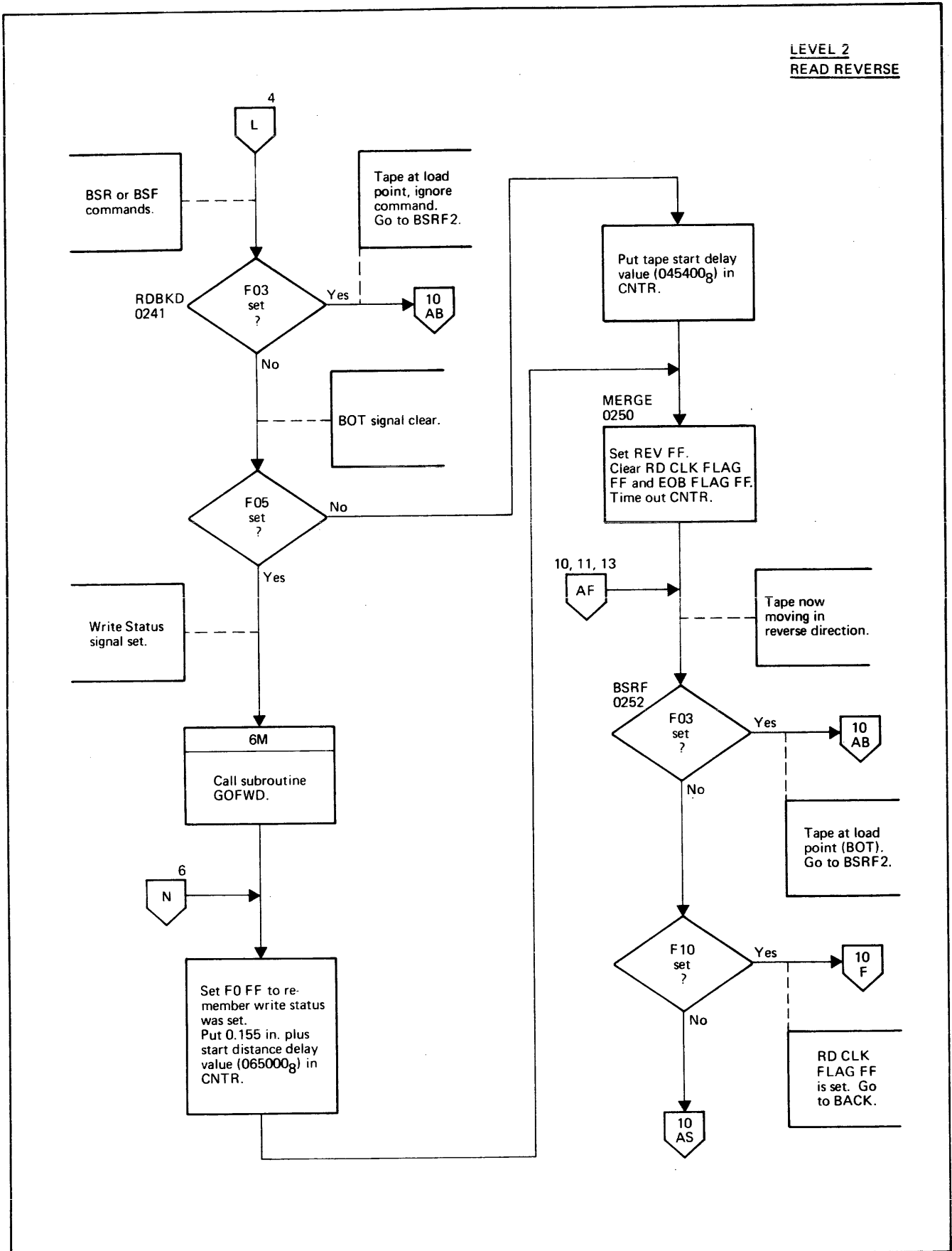
Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 7 of 58)



2186-67

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 8 of 58)

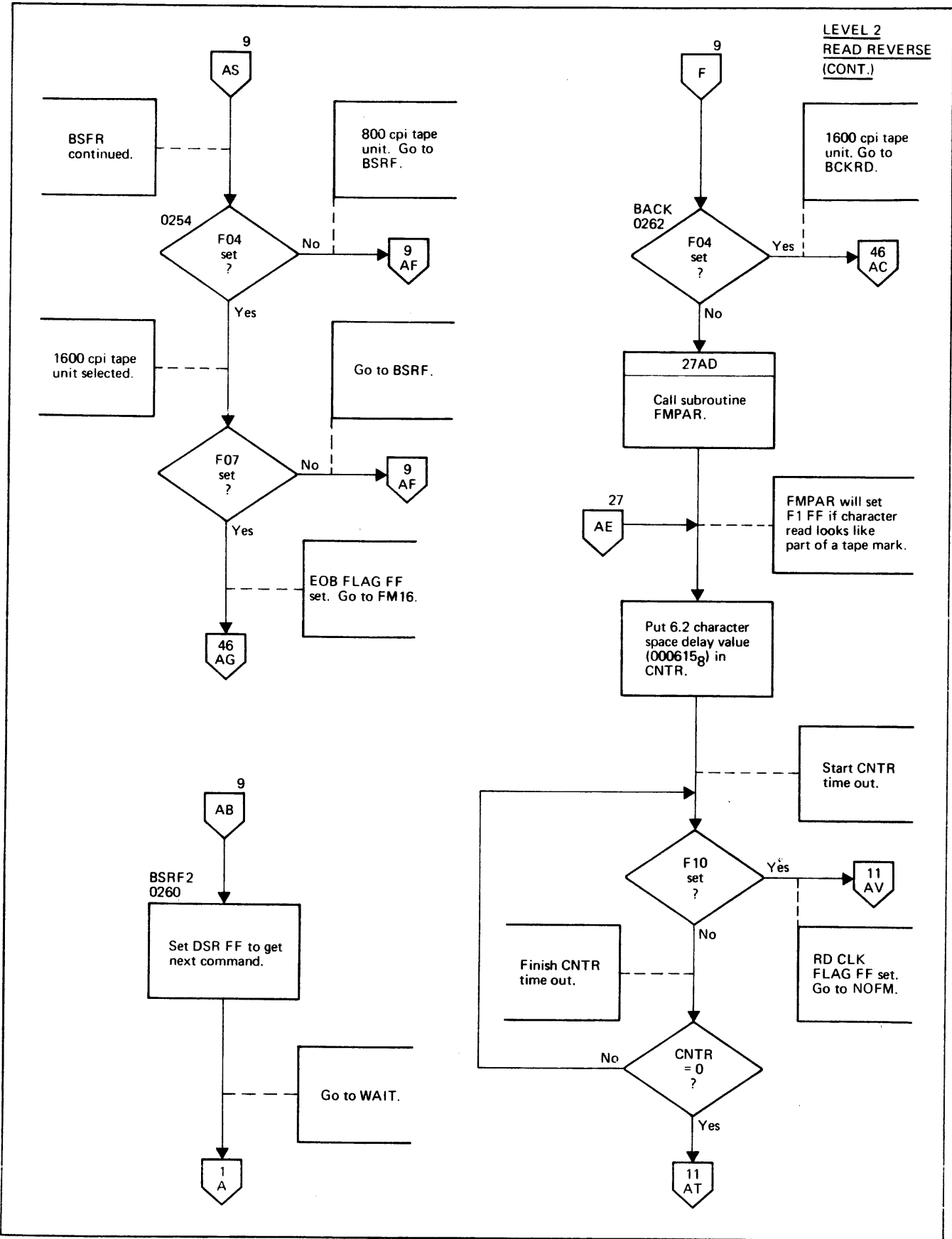
LEVEL 2
READ REVERSE



2186-68

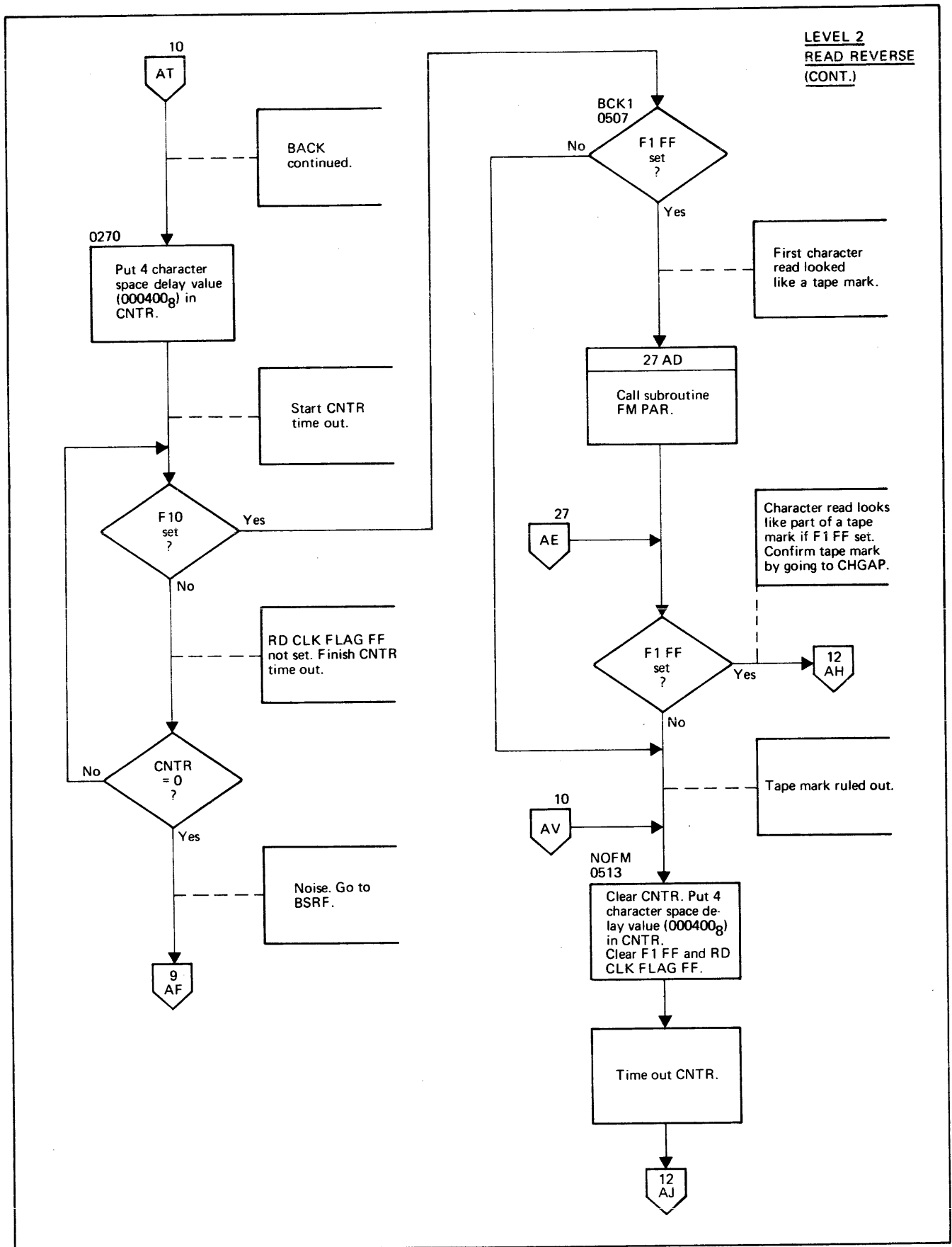
Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 9 of 58)

LEVEL 2
READ REVERSE
(CONT.)



7186 69

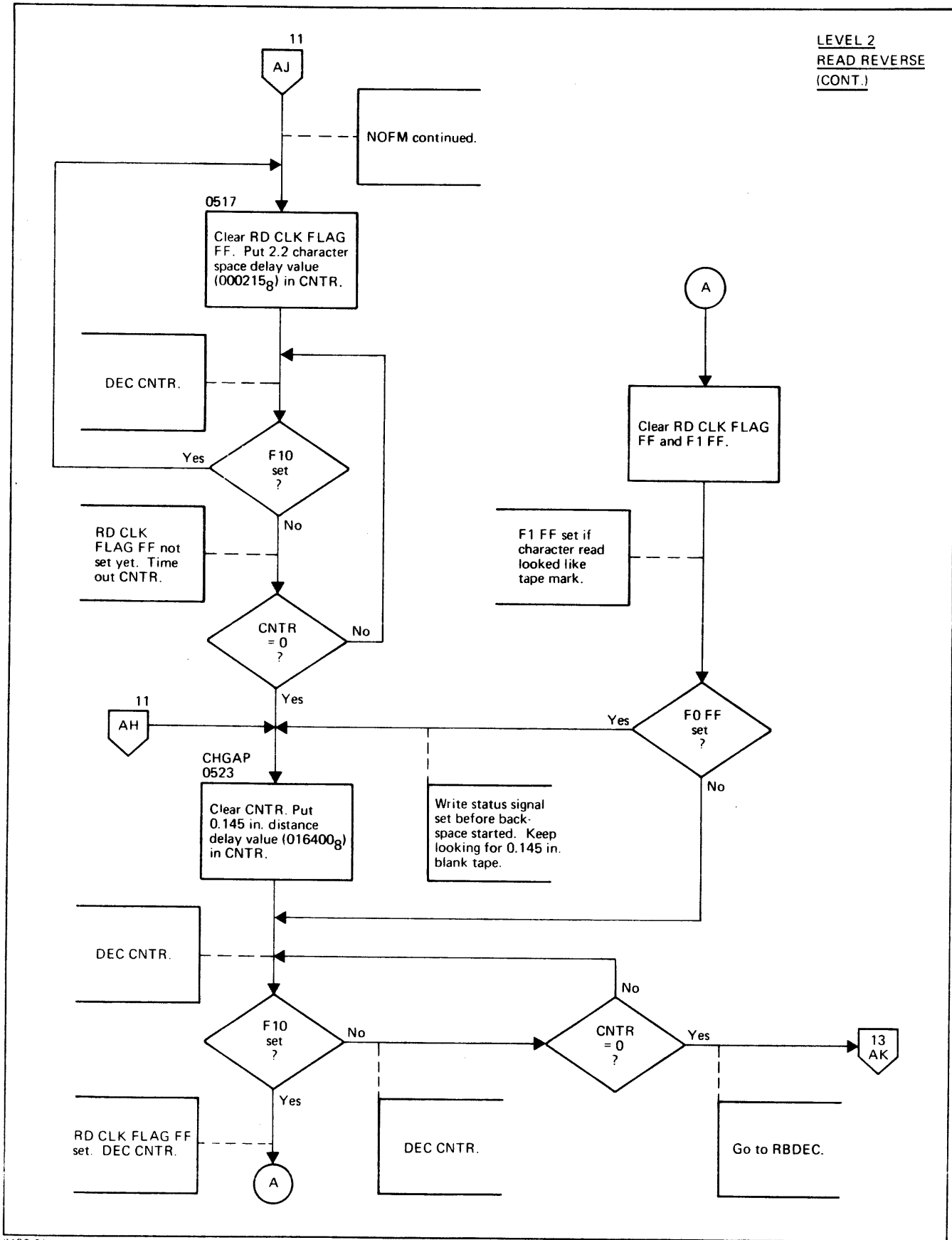
Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 10 of 58)



2186-70

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 11 of 58)

LEVEL 2
READ REVERSE
(CONT.)



2180 71

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 12 of 58)

LEVEL 2
READ REVERSE
(CONT.)

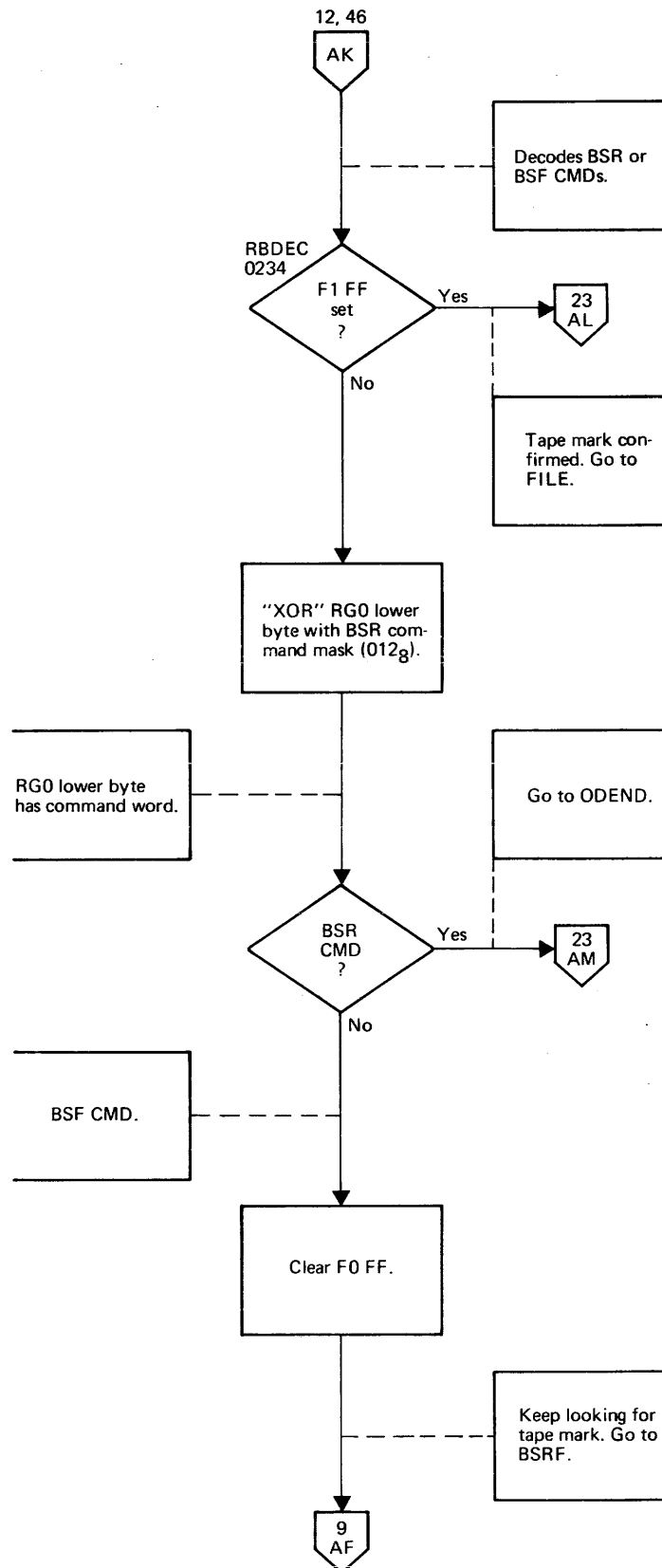
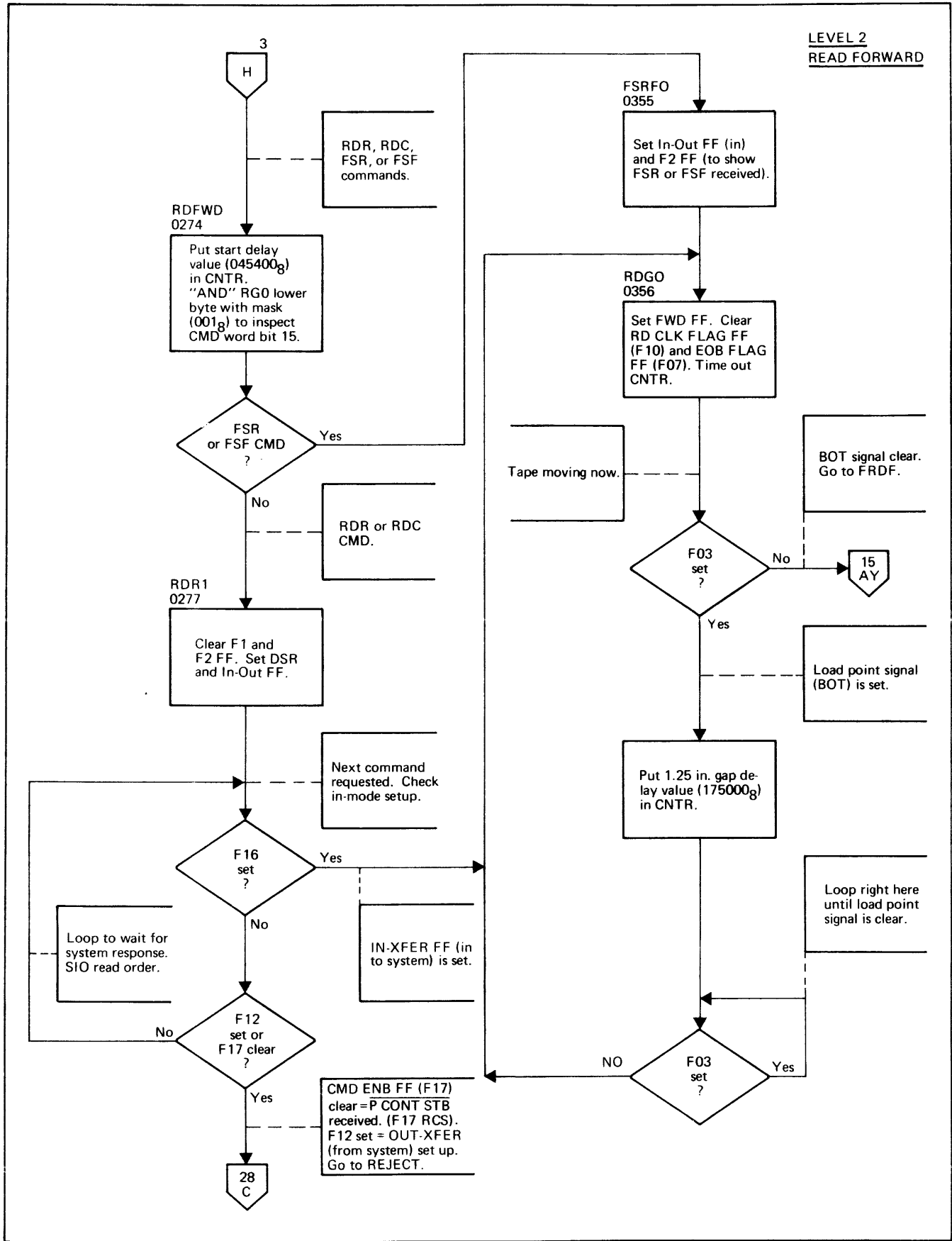
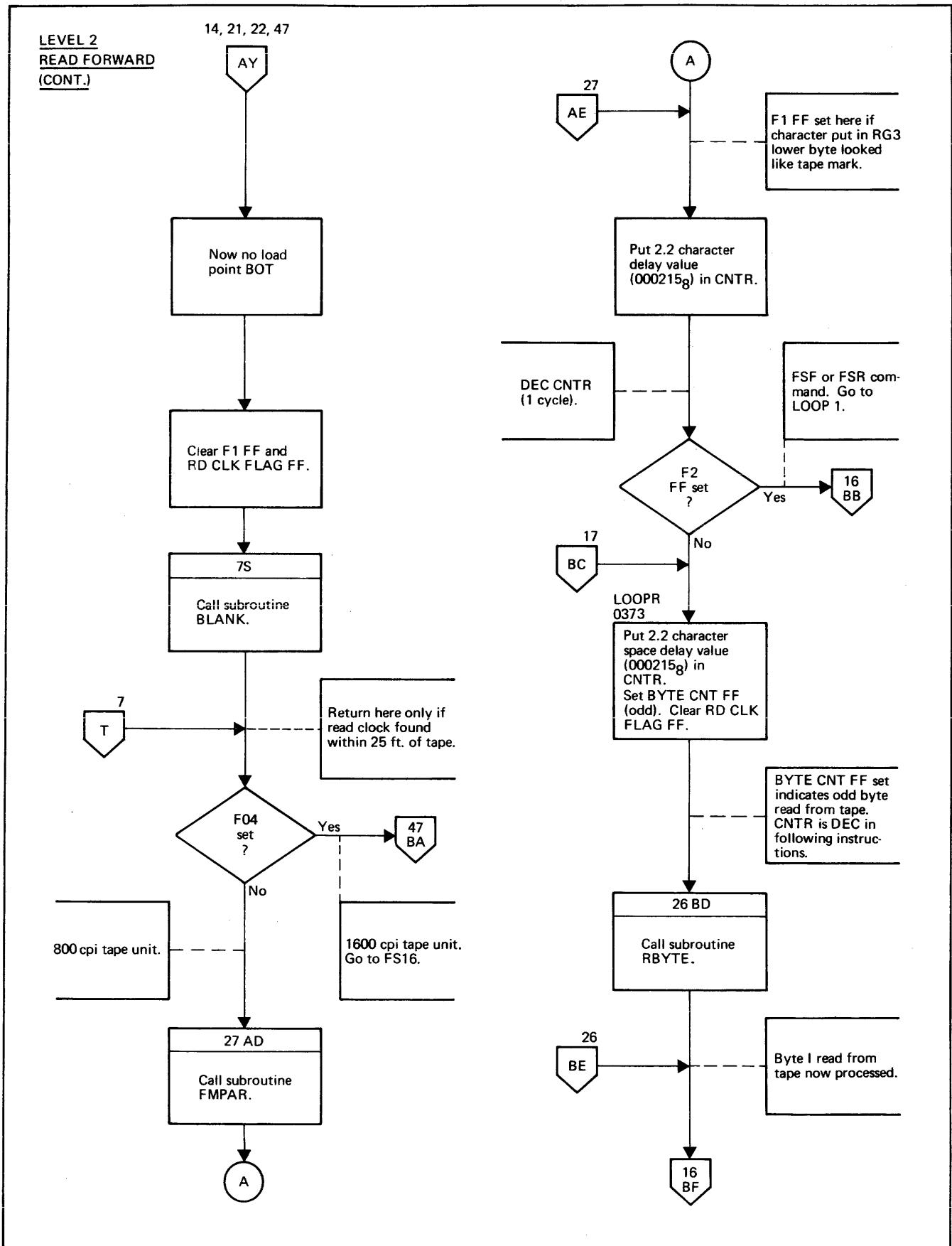


Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 13 of 58)



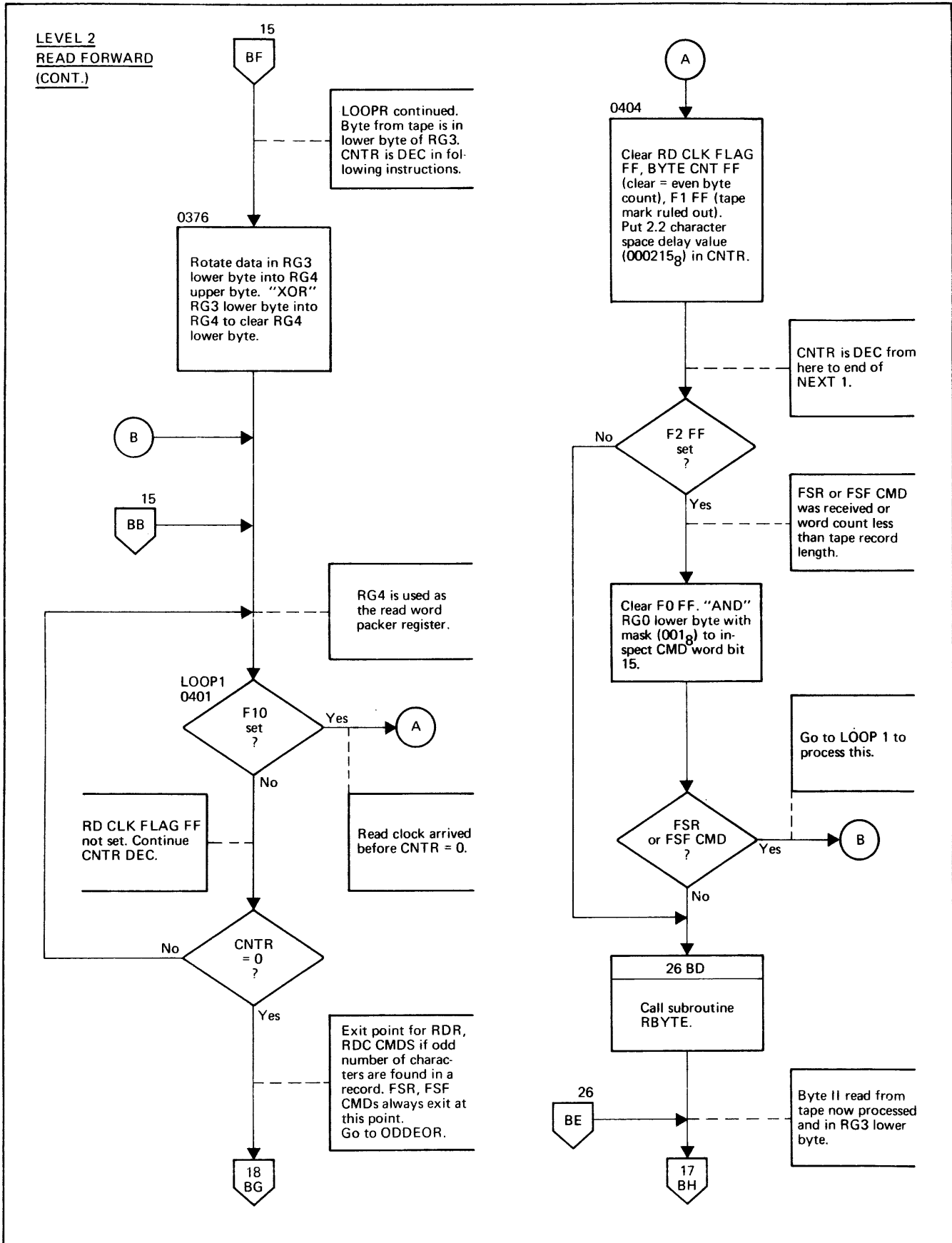
2180-73

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 14 of 58)



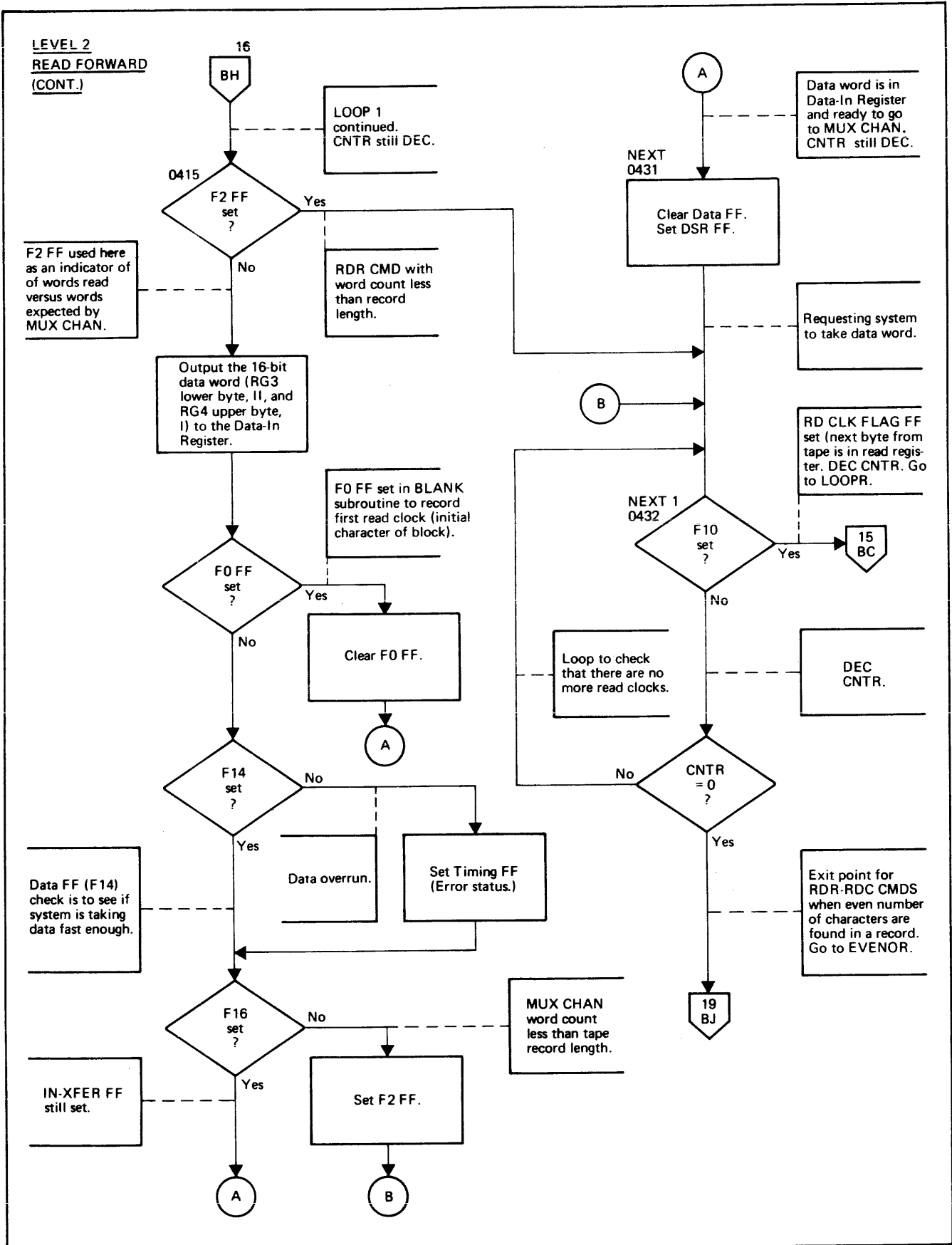
2180-74A

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 15 of 58)



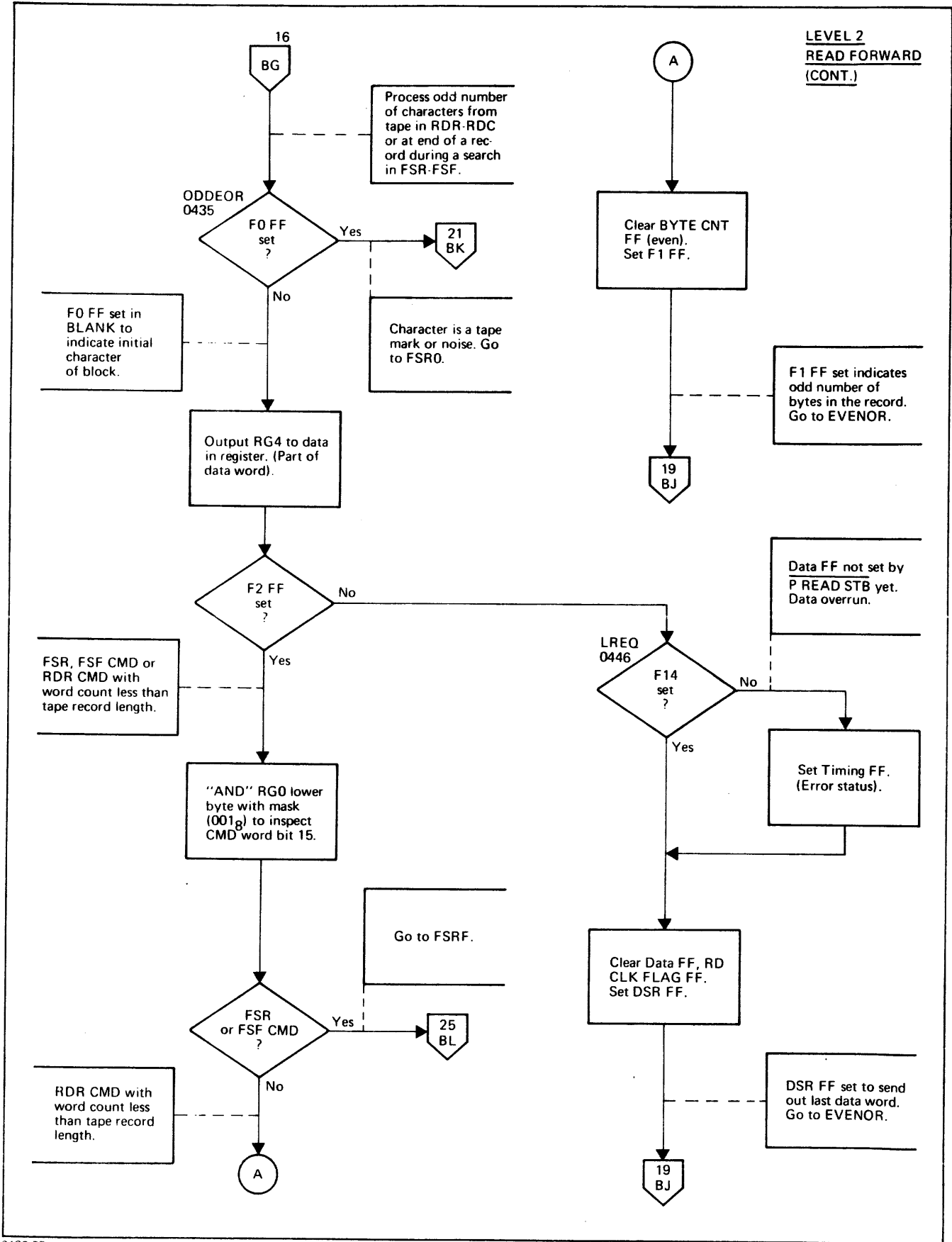
2180-75

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 16 of 58)



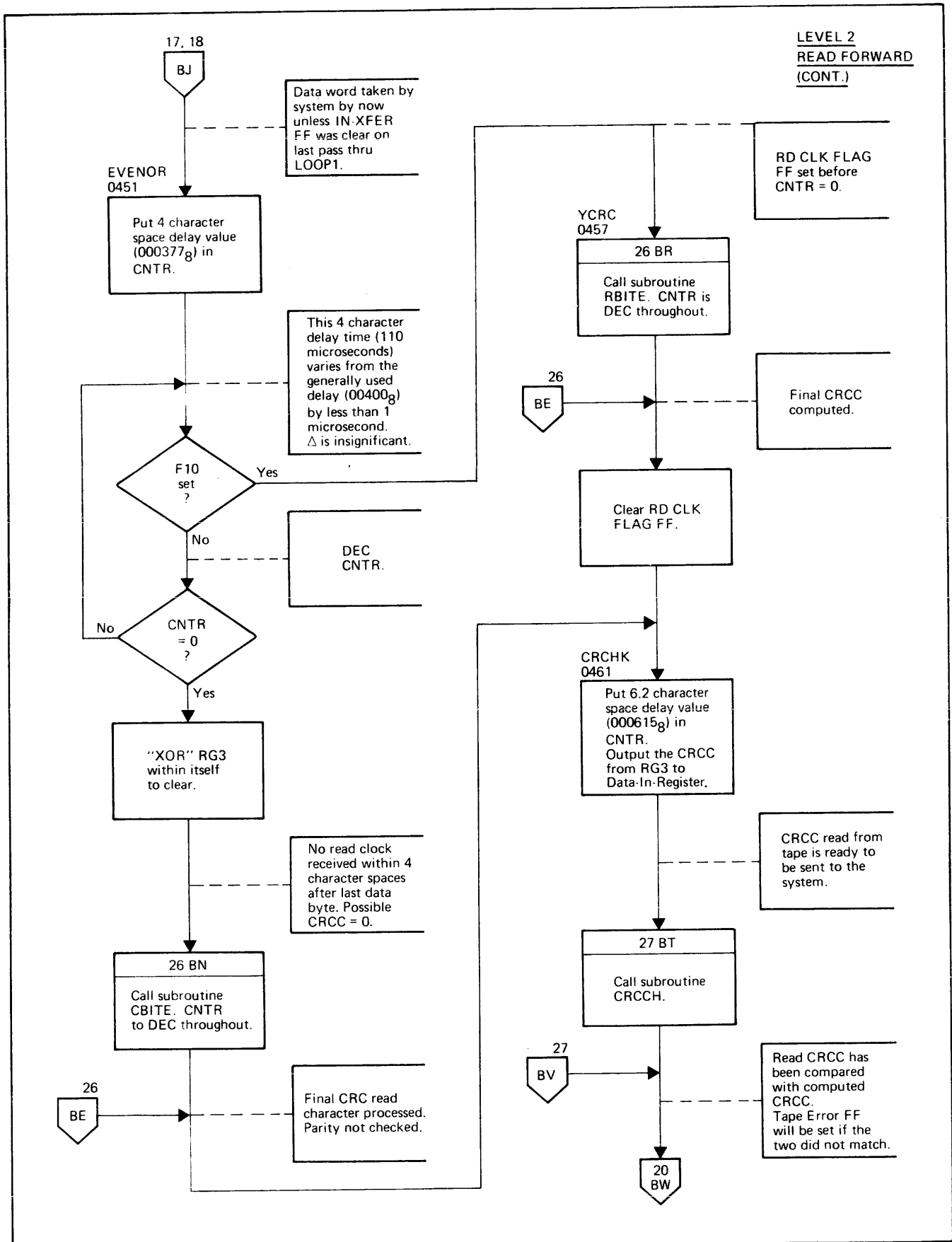
2180-76

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 17 of 58)



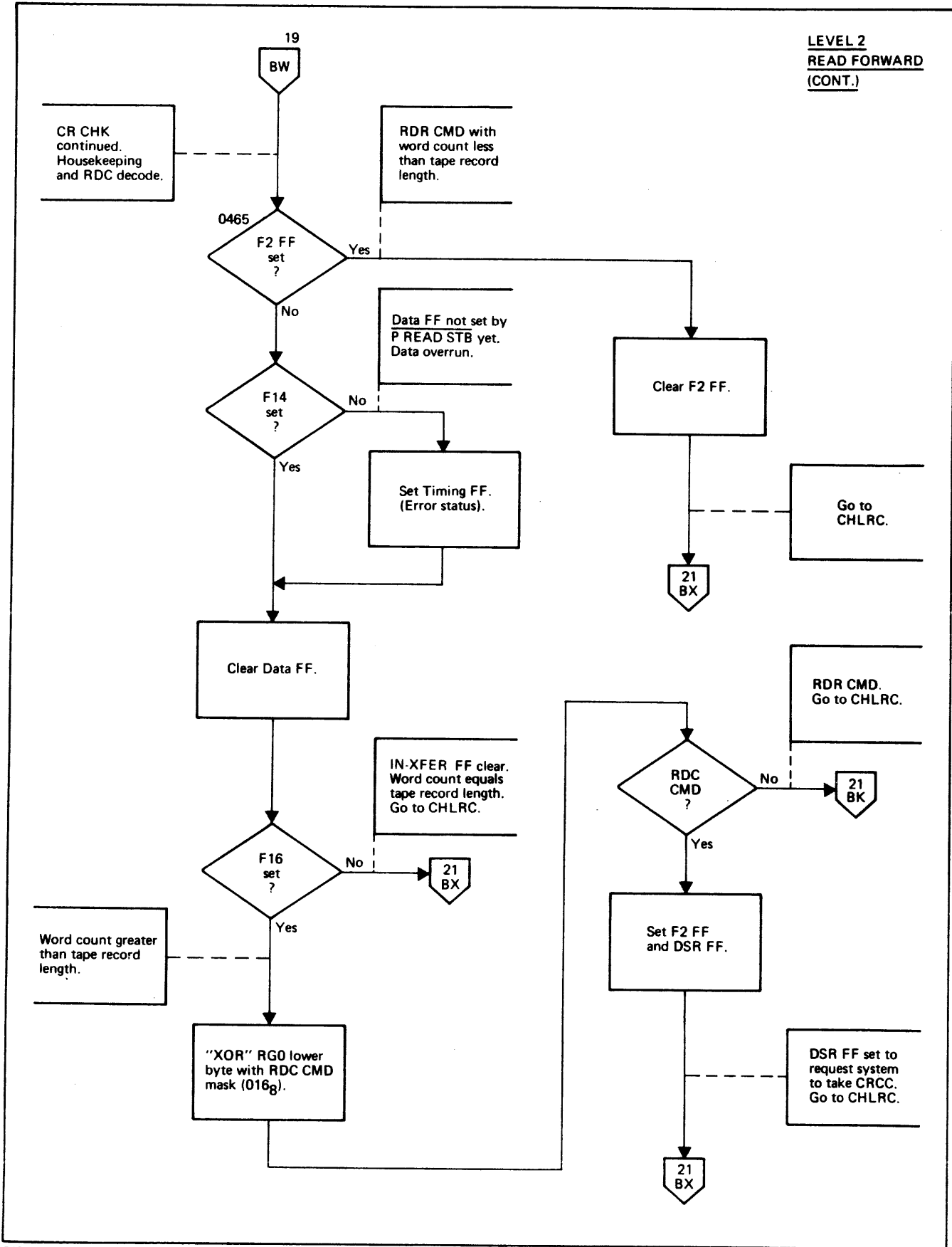
2180 77

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 18 of 58)



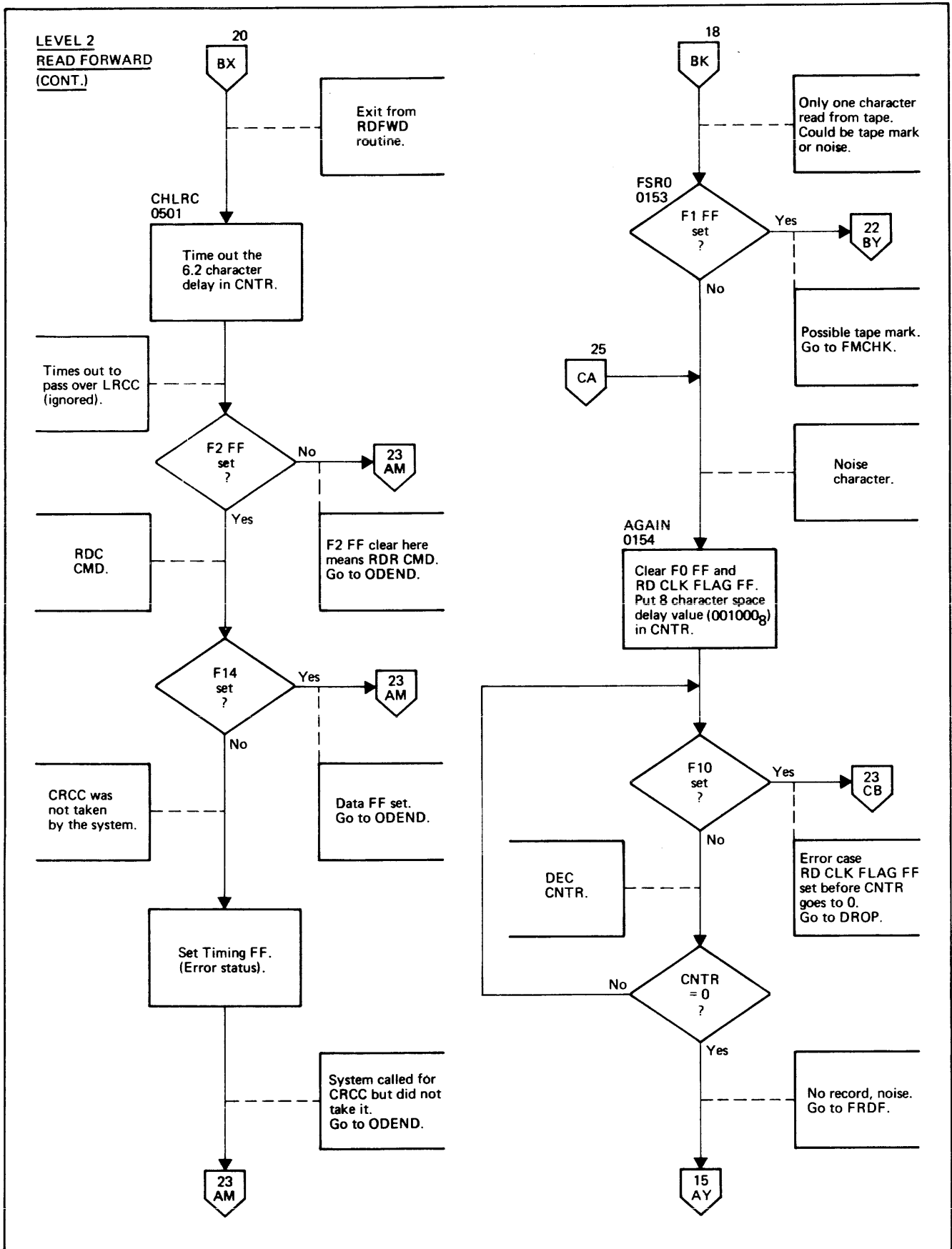
2180-78

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 19 of 58)



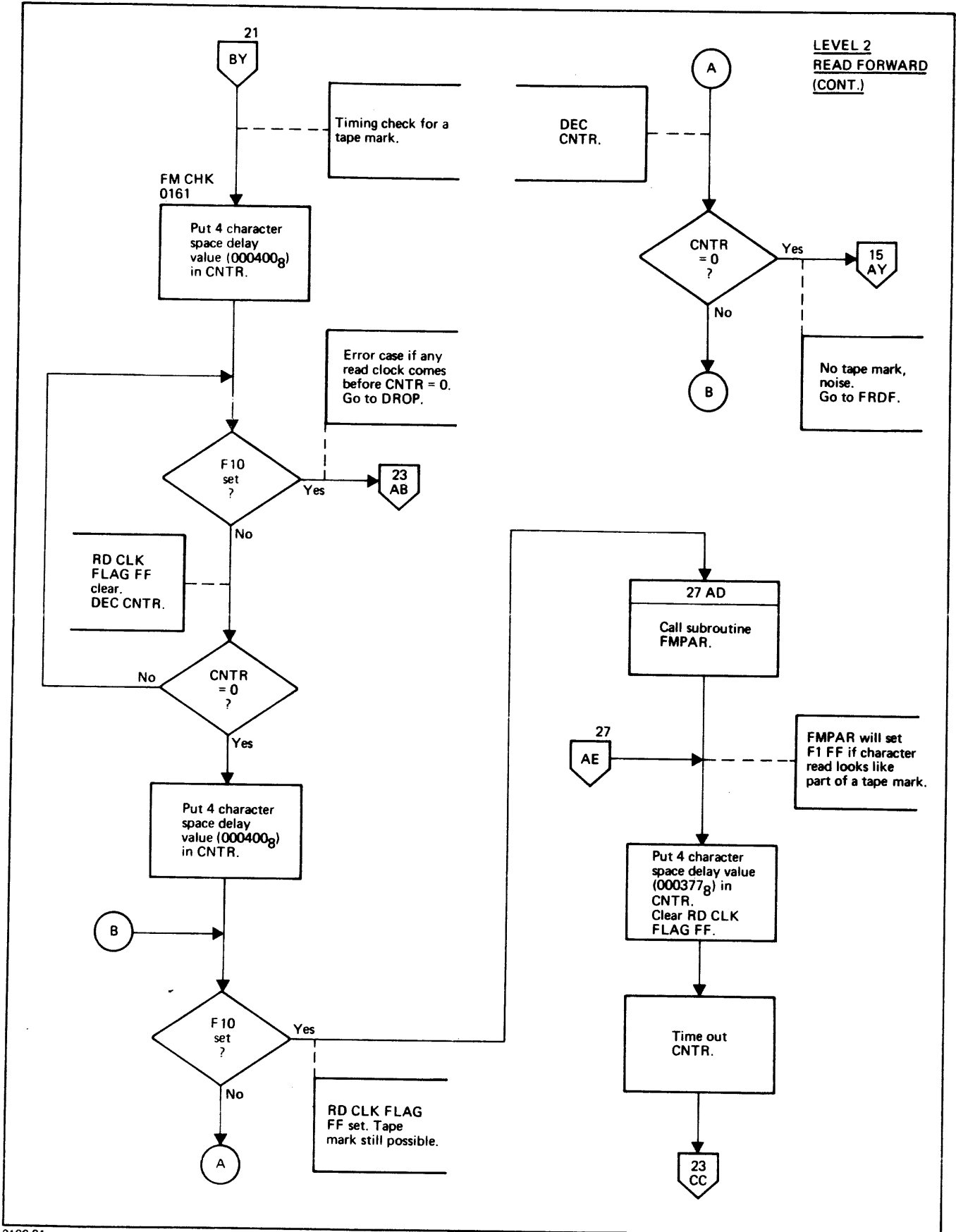
2180-79

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 20 of 58)



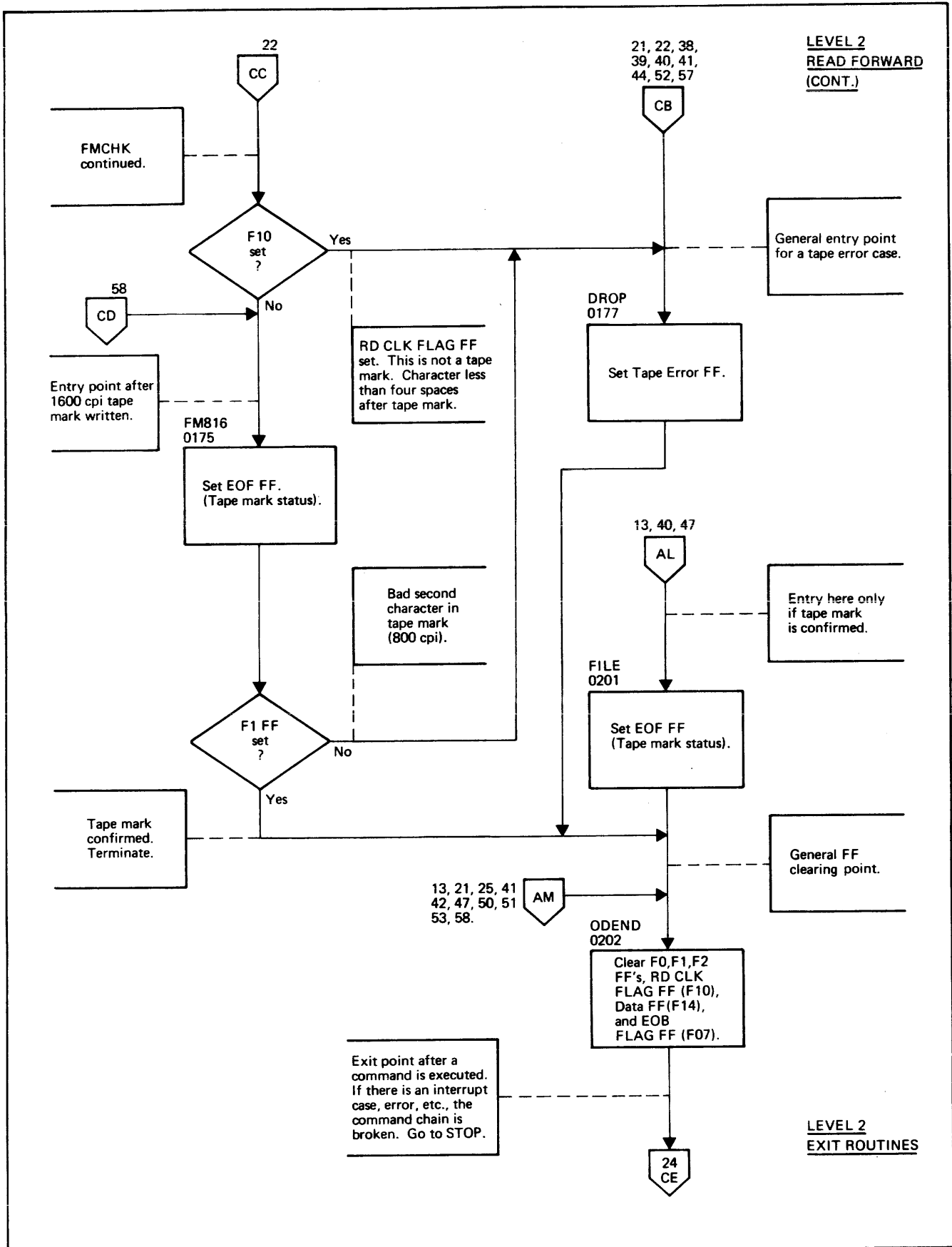
2180-80

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 21 of 58)



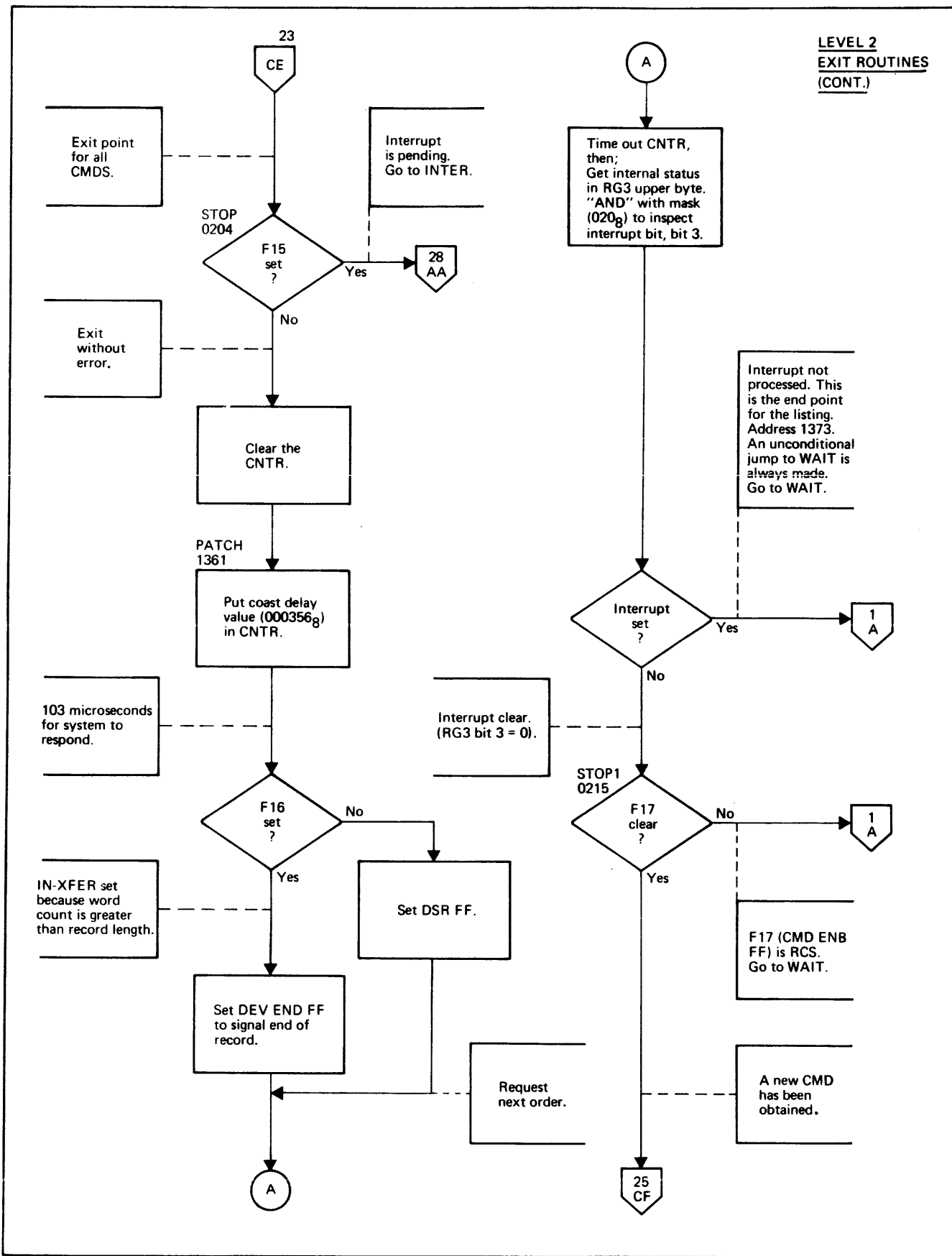
2180-81

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 22 of 58)



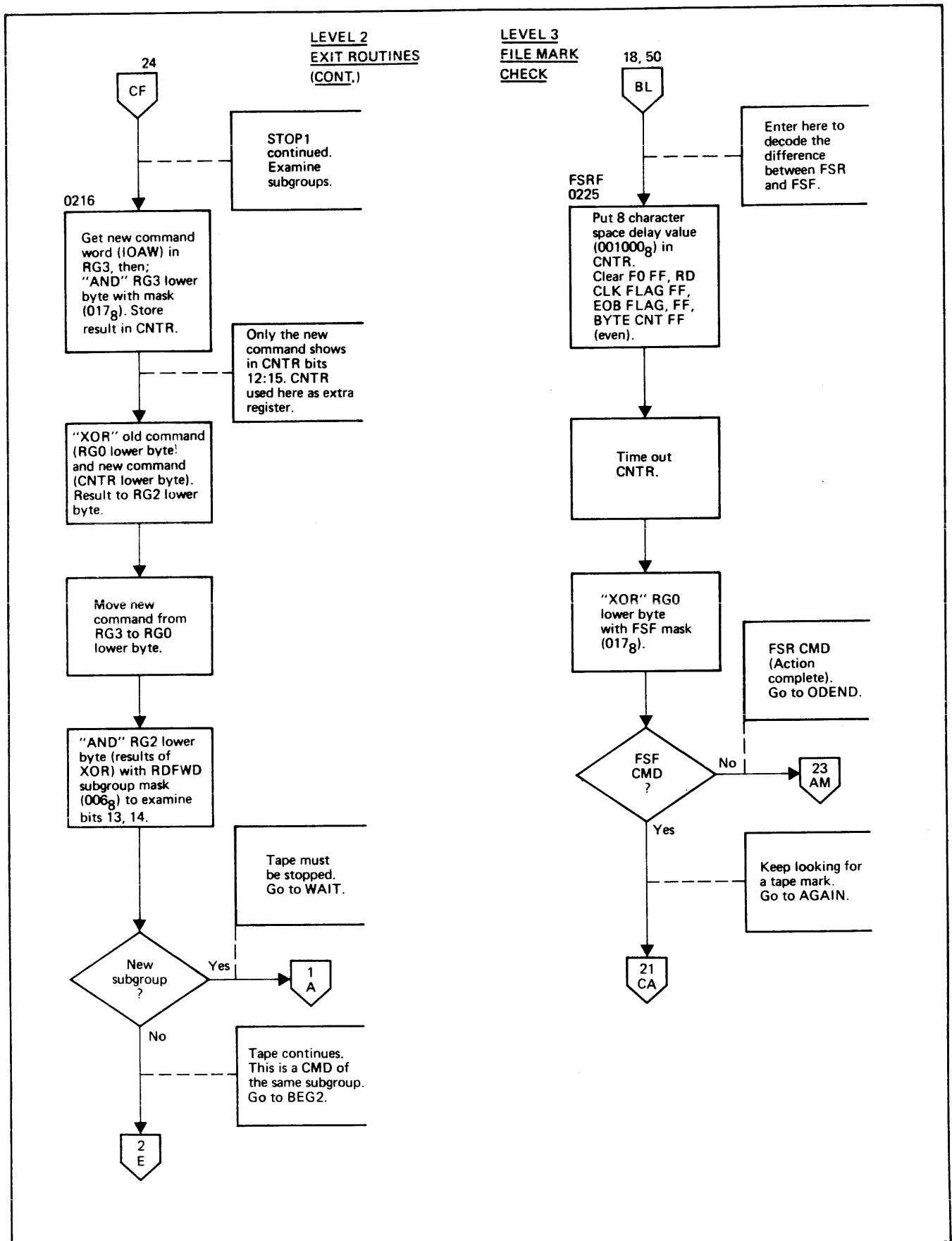
2180-82

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 23 of 58)



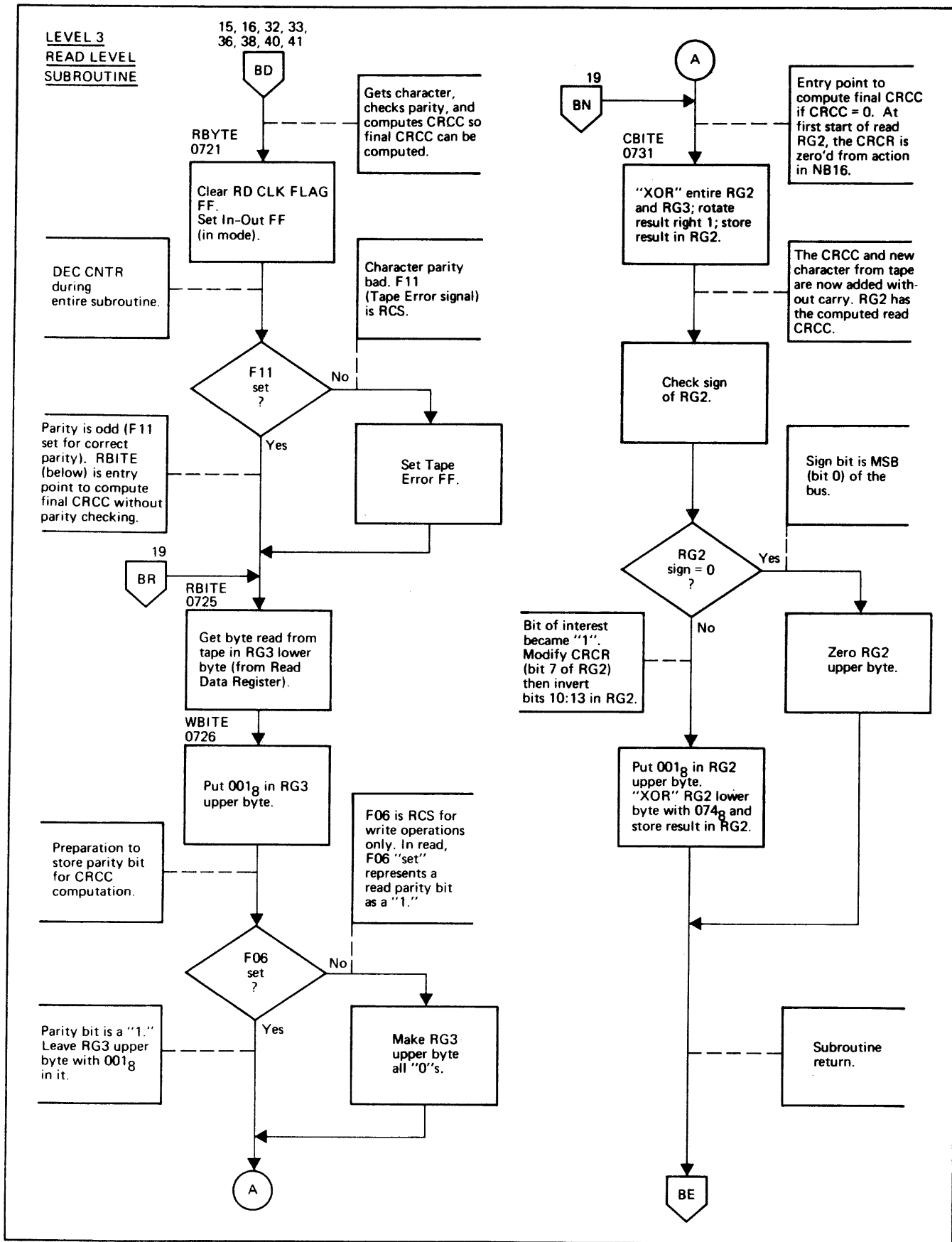
2180-83

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 24 of 58)



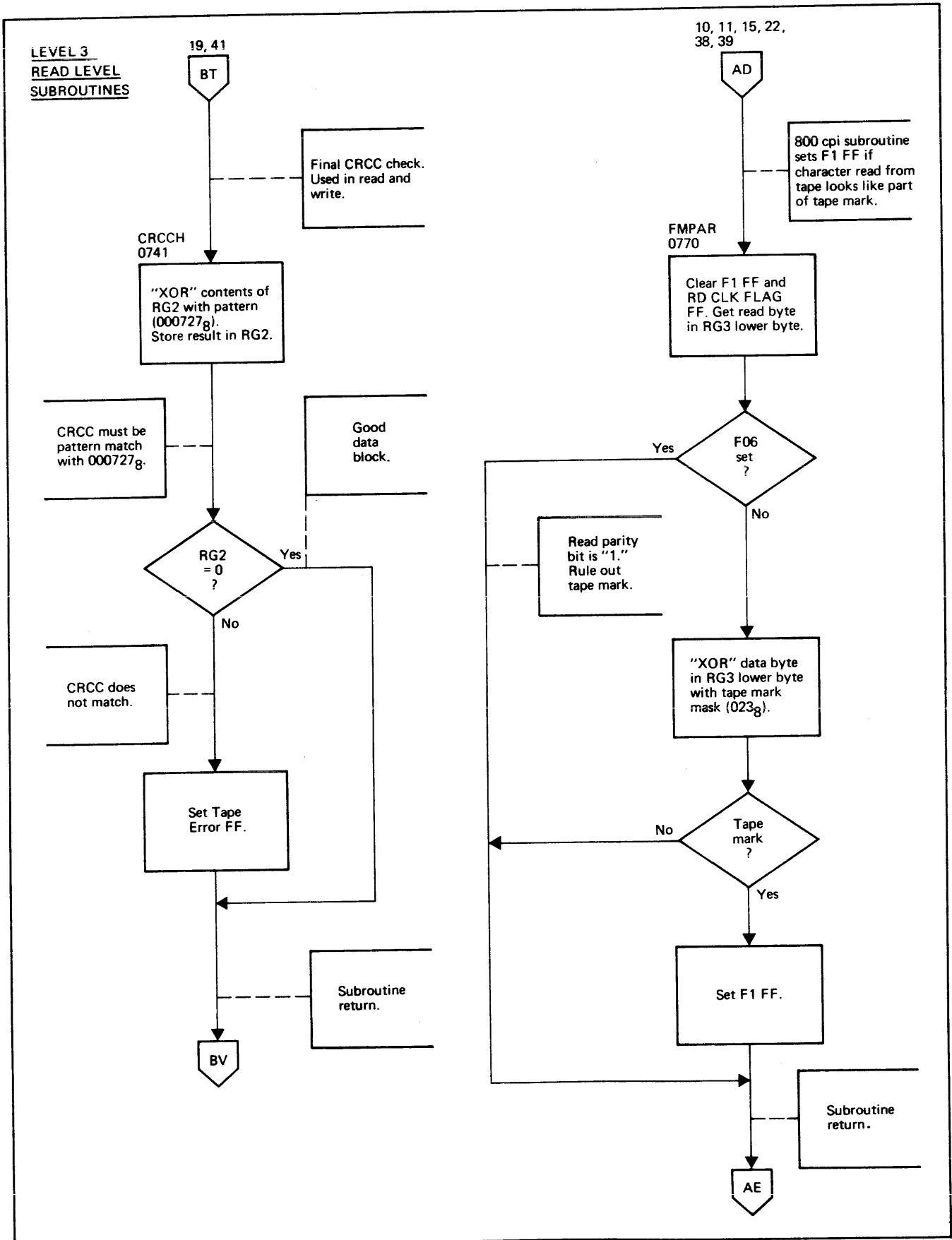
2180-84

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 25 of 58)



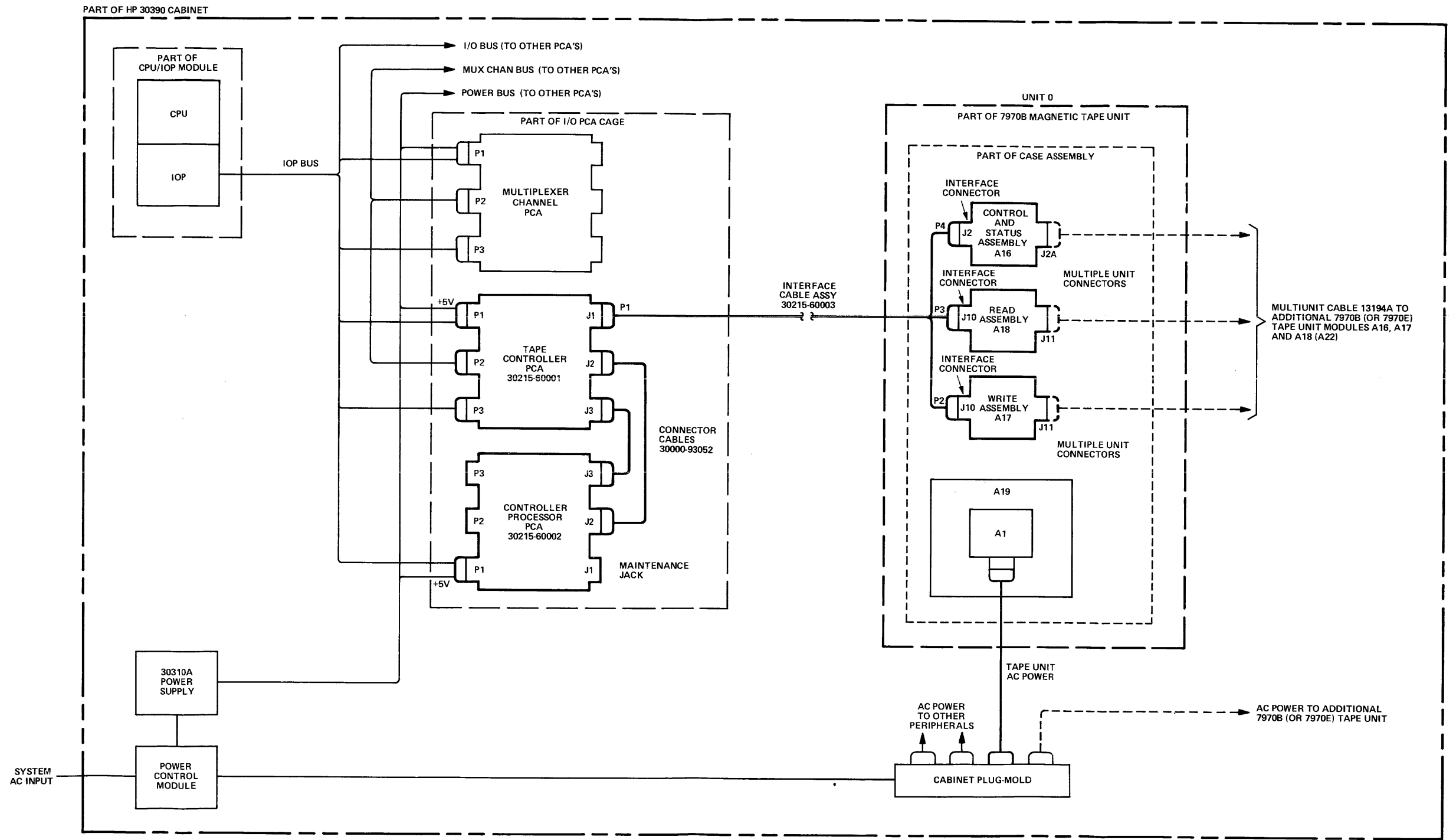
2180-85

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 26 of 58)



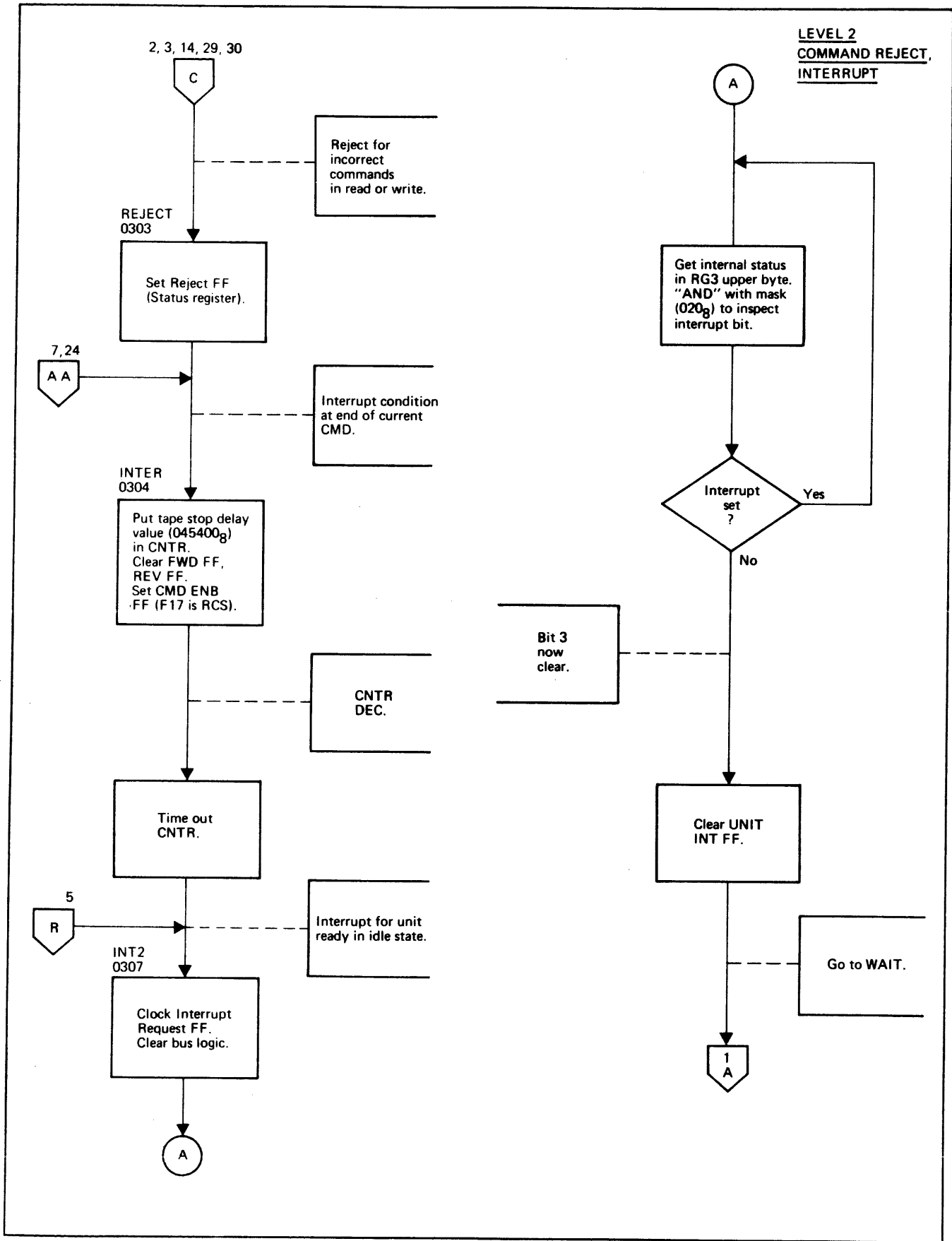
2180-86

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 27 of 58)



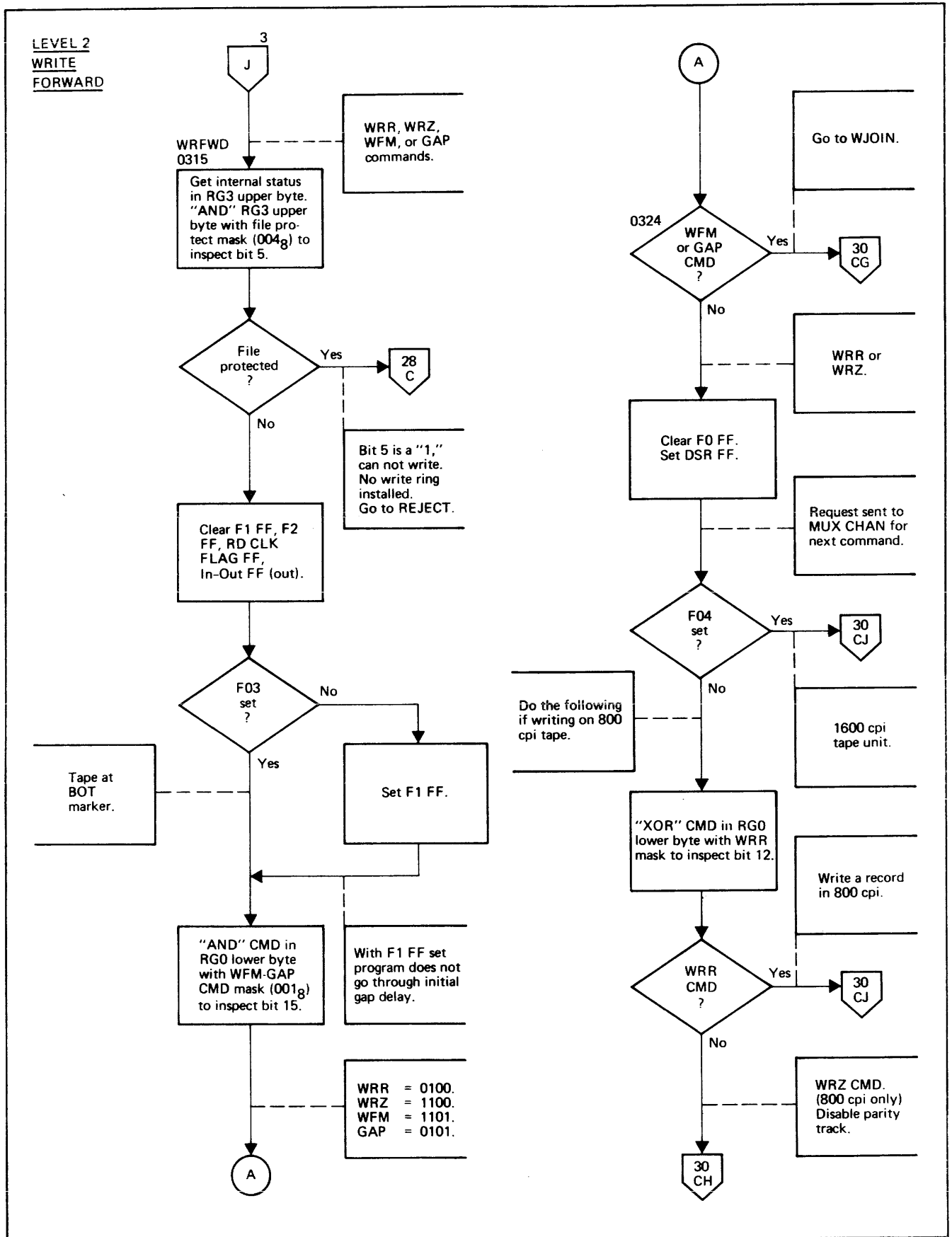
2180-7

Figure 4-1. Magnetic Tape Subsystem Example
Single Tape Unit Cabling Diagram



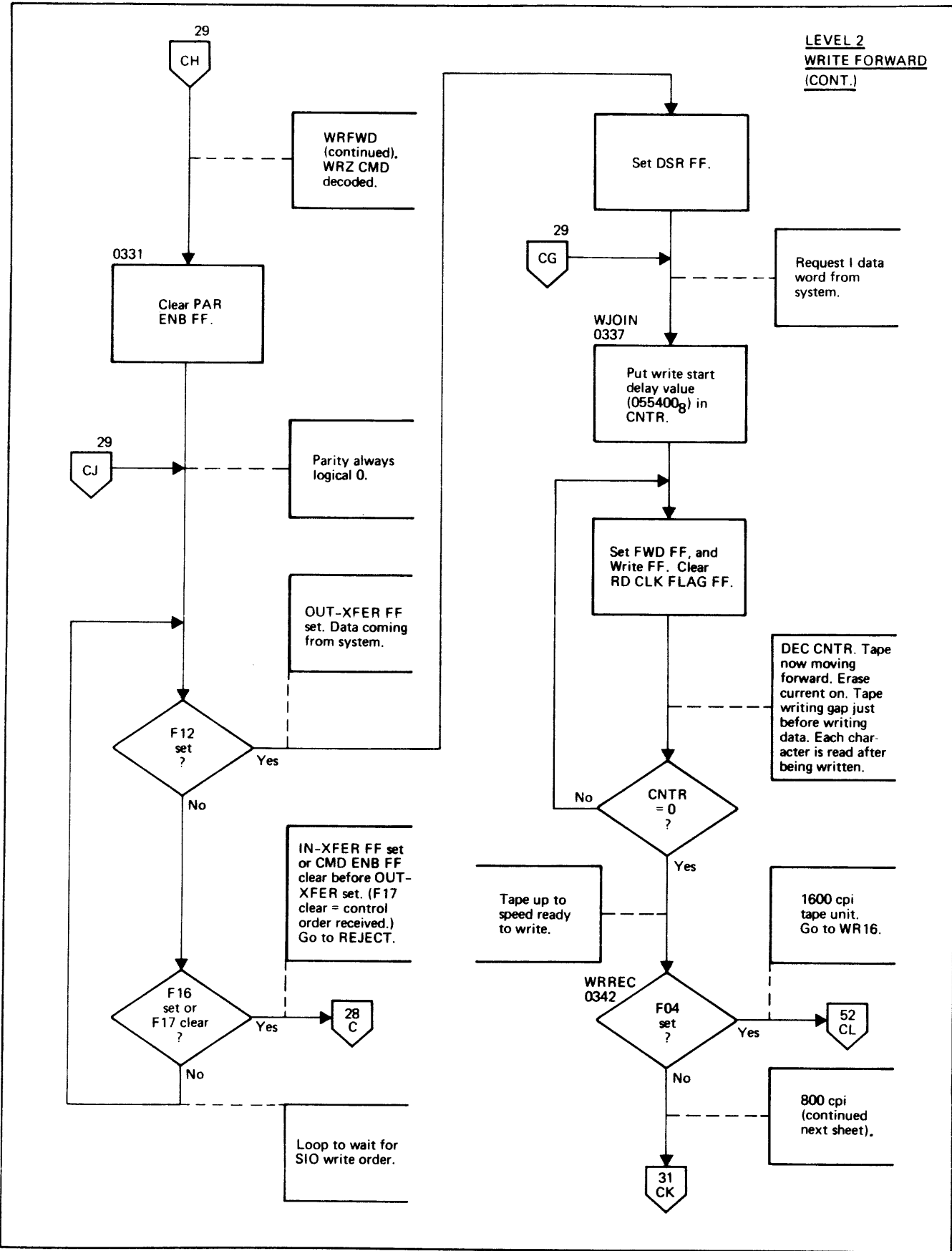
2180-87

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 28 of 58)



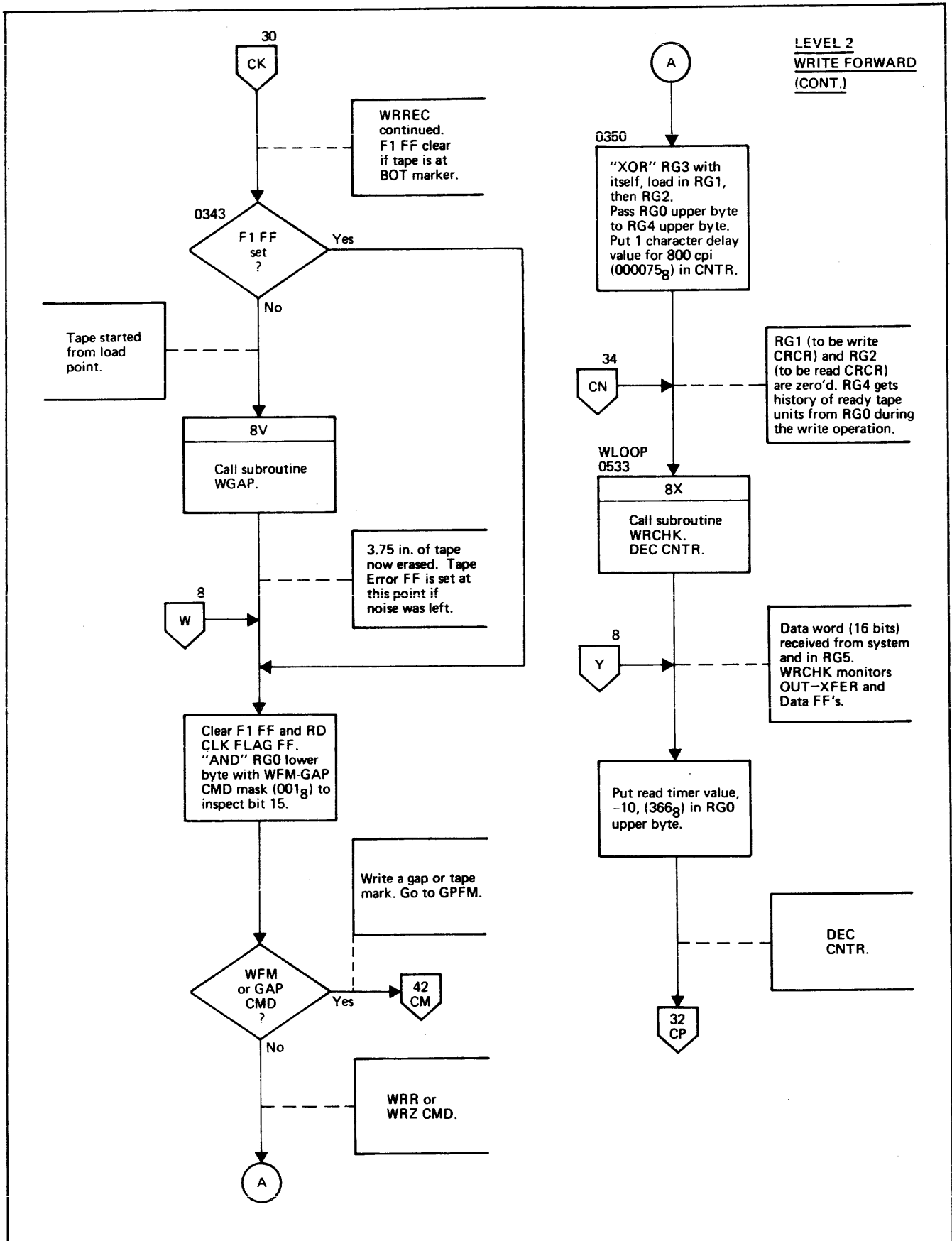
2180-88

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 29 of 58)



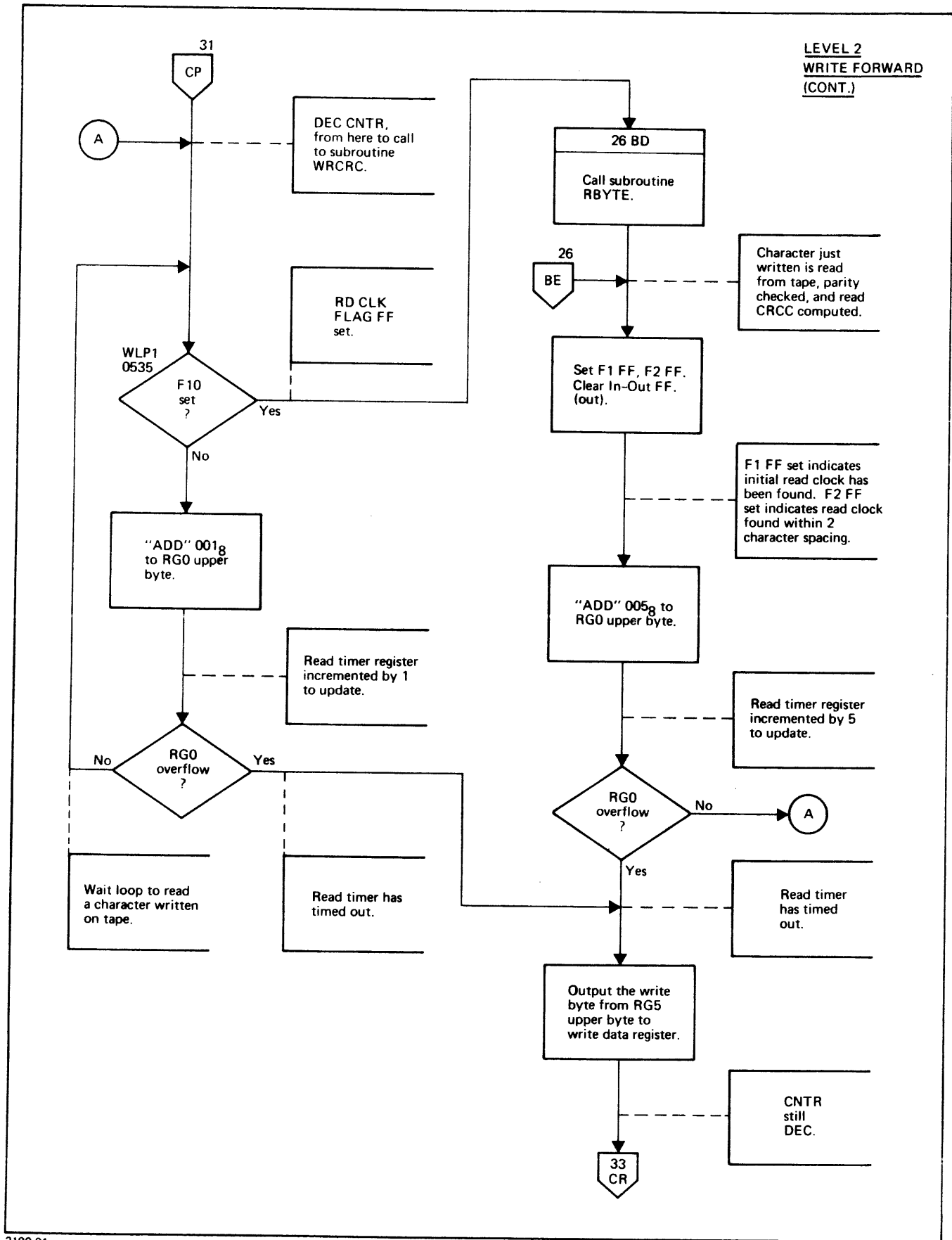
2180-89B

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 30 of 58)



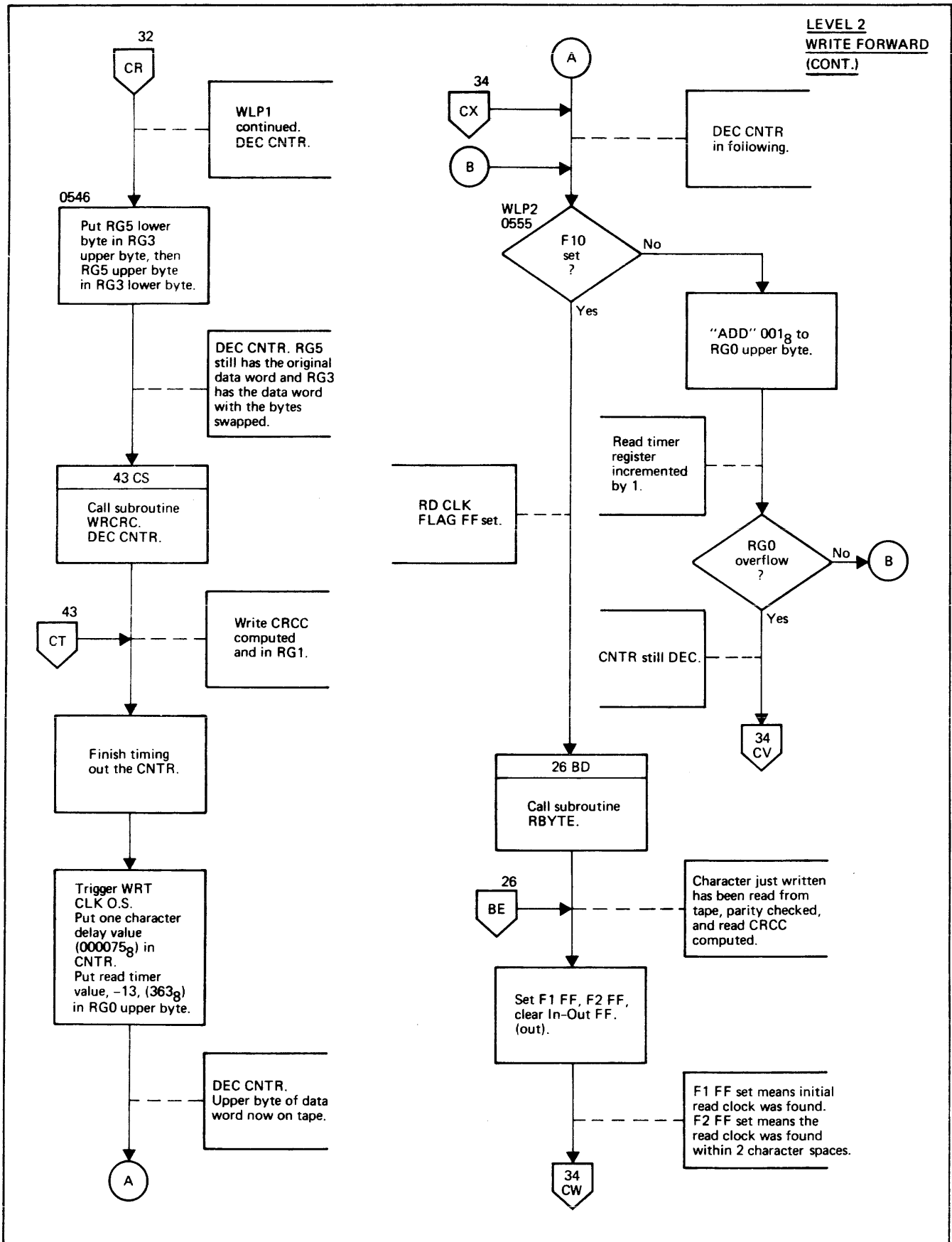
2180-90

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 31 of 58)



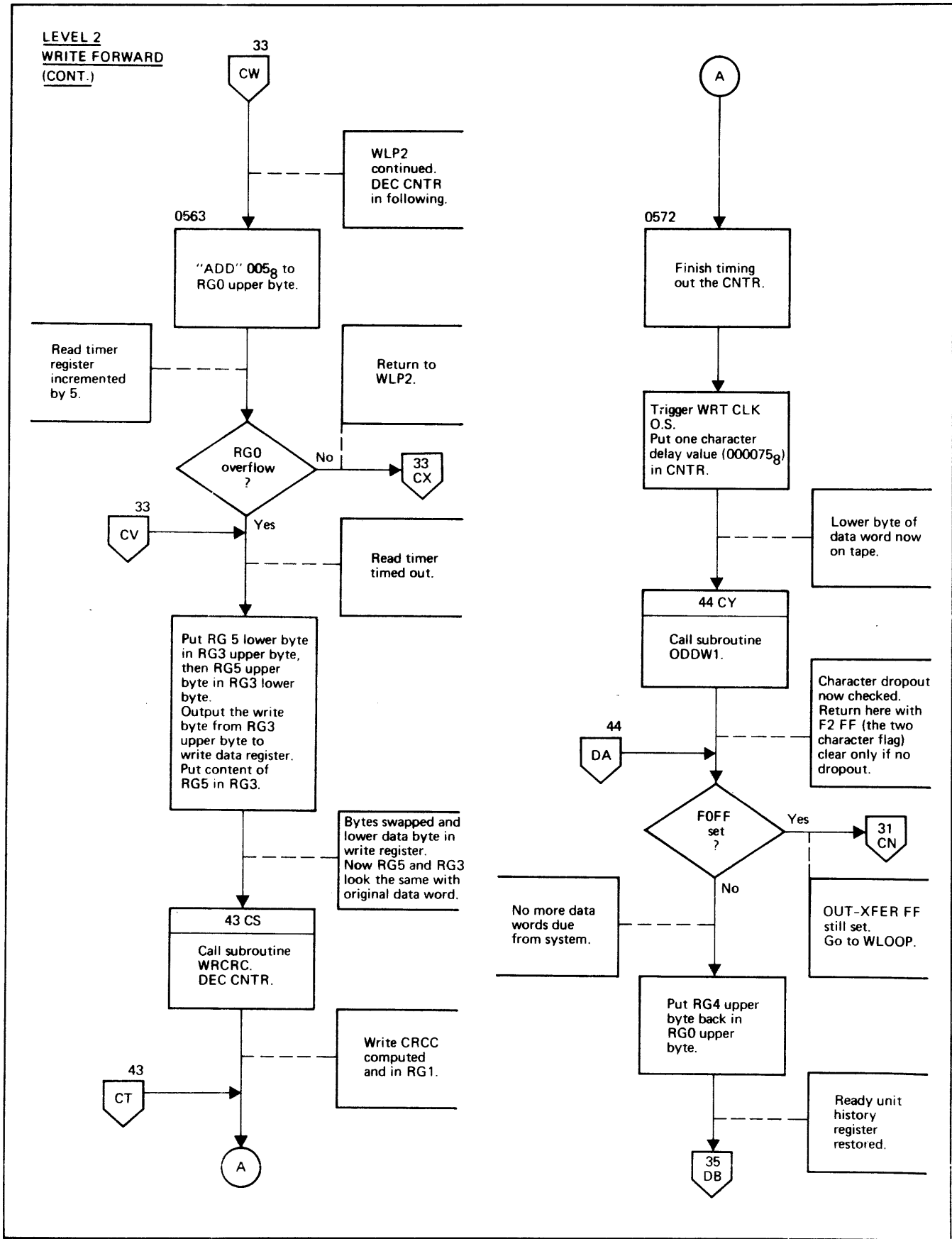
2180-91

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 32 of 58)



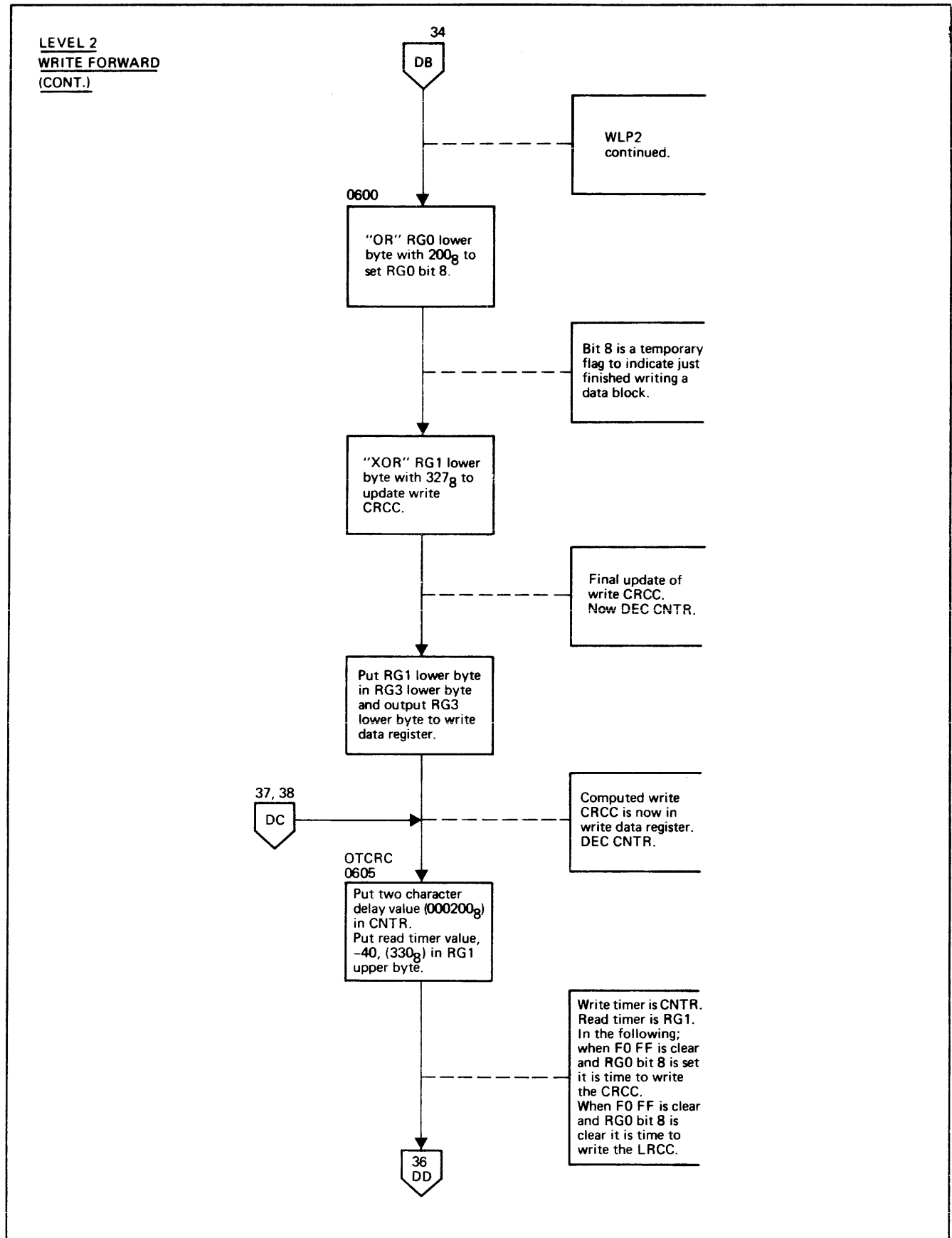
2180-92

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 33 of 58)



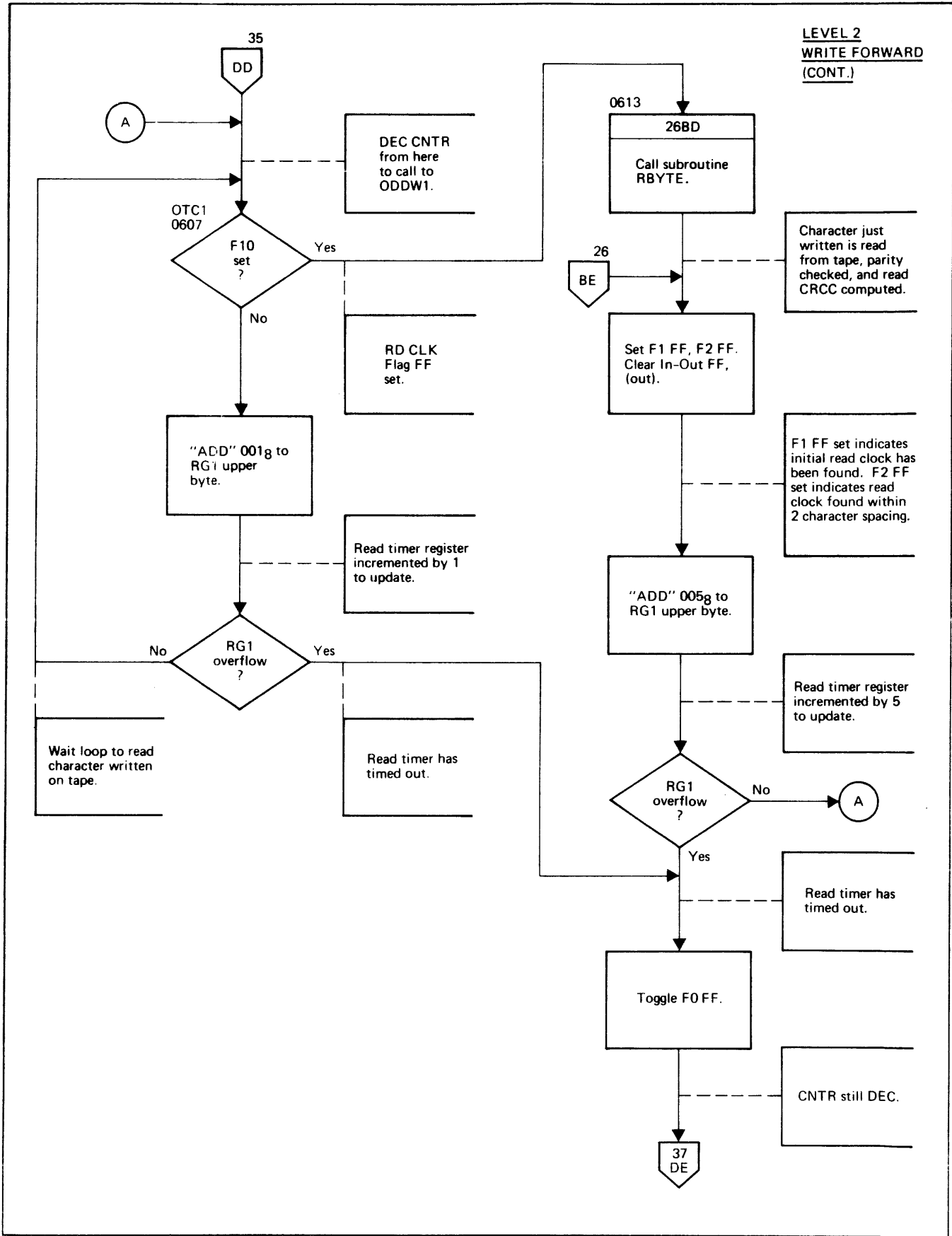
2180-93

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 34 of 58)



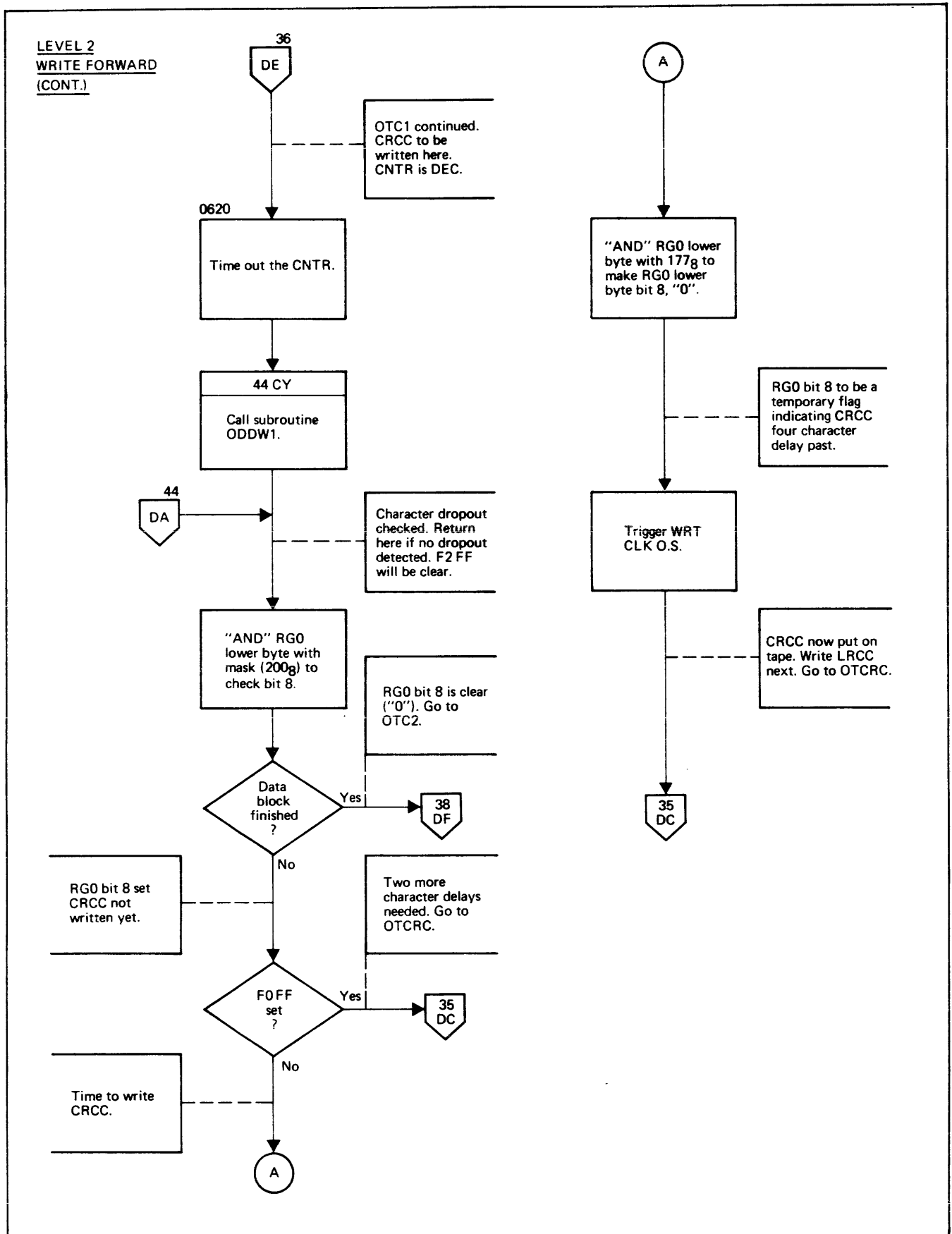
2180-94

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 35 of 58)



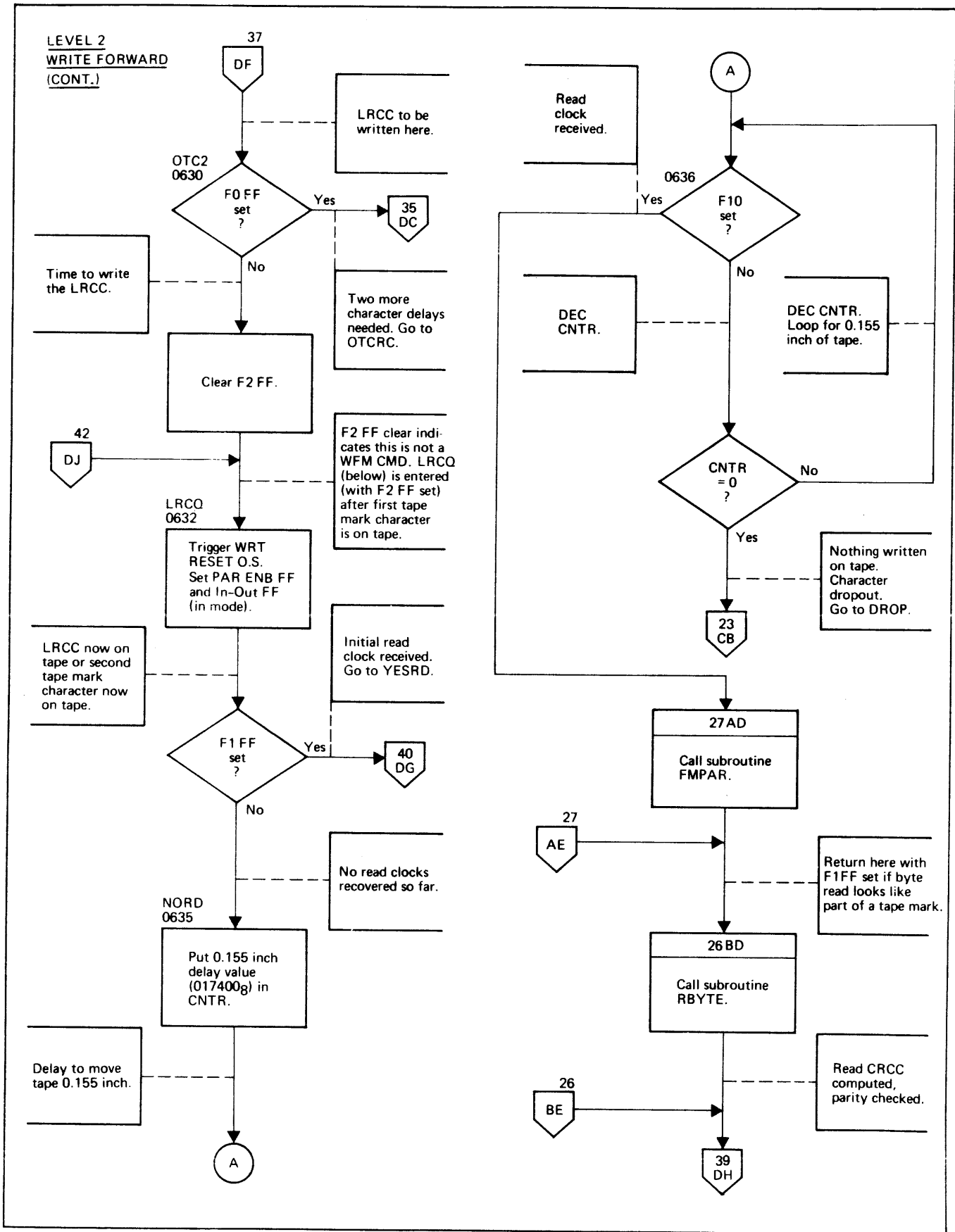
2180-95

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 36 of 58)



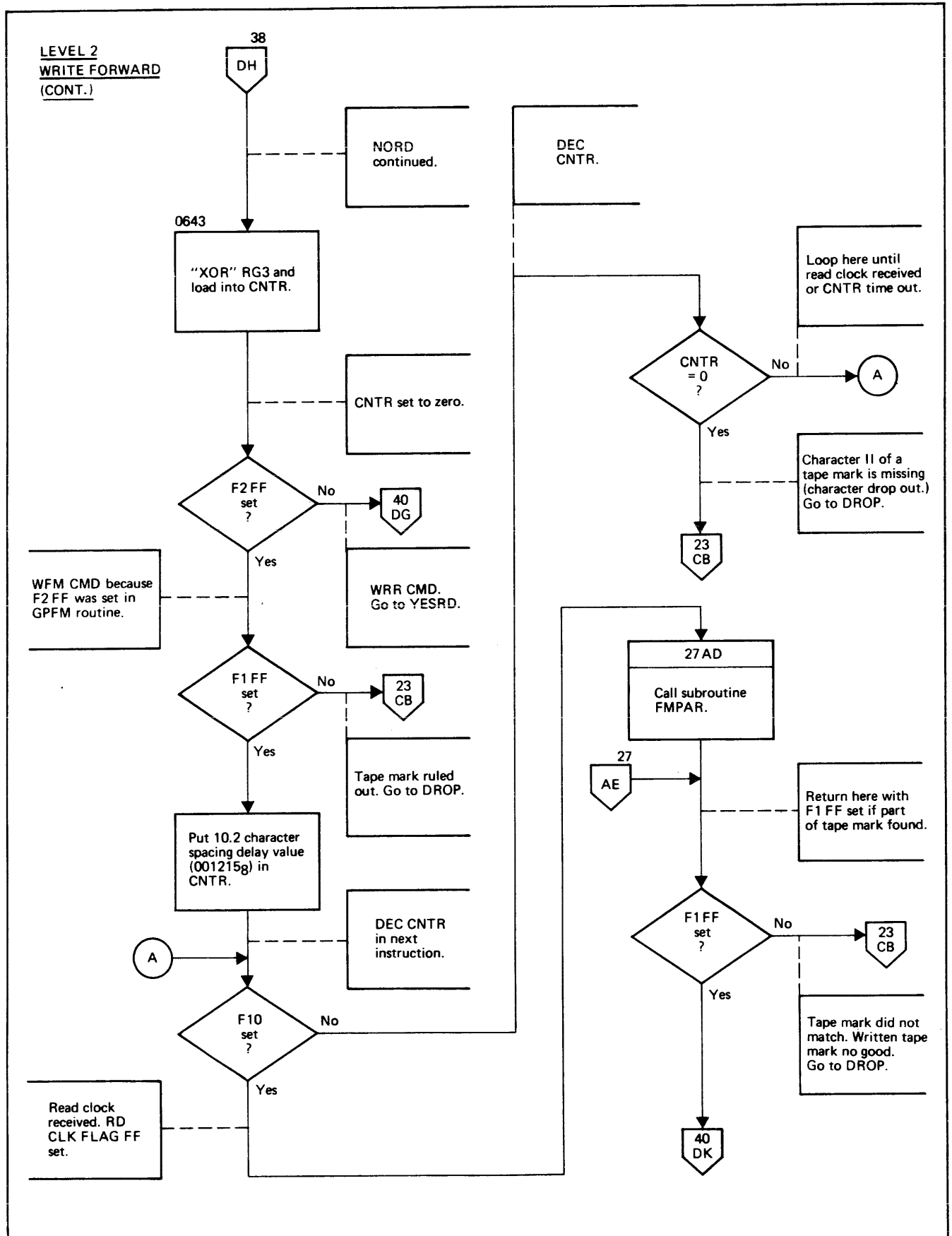
2180-96

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 37 of 58)



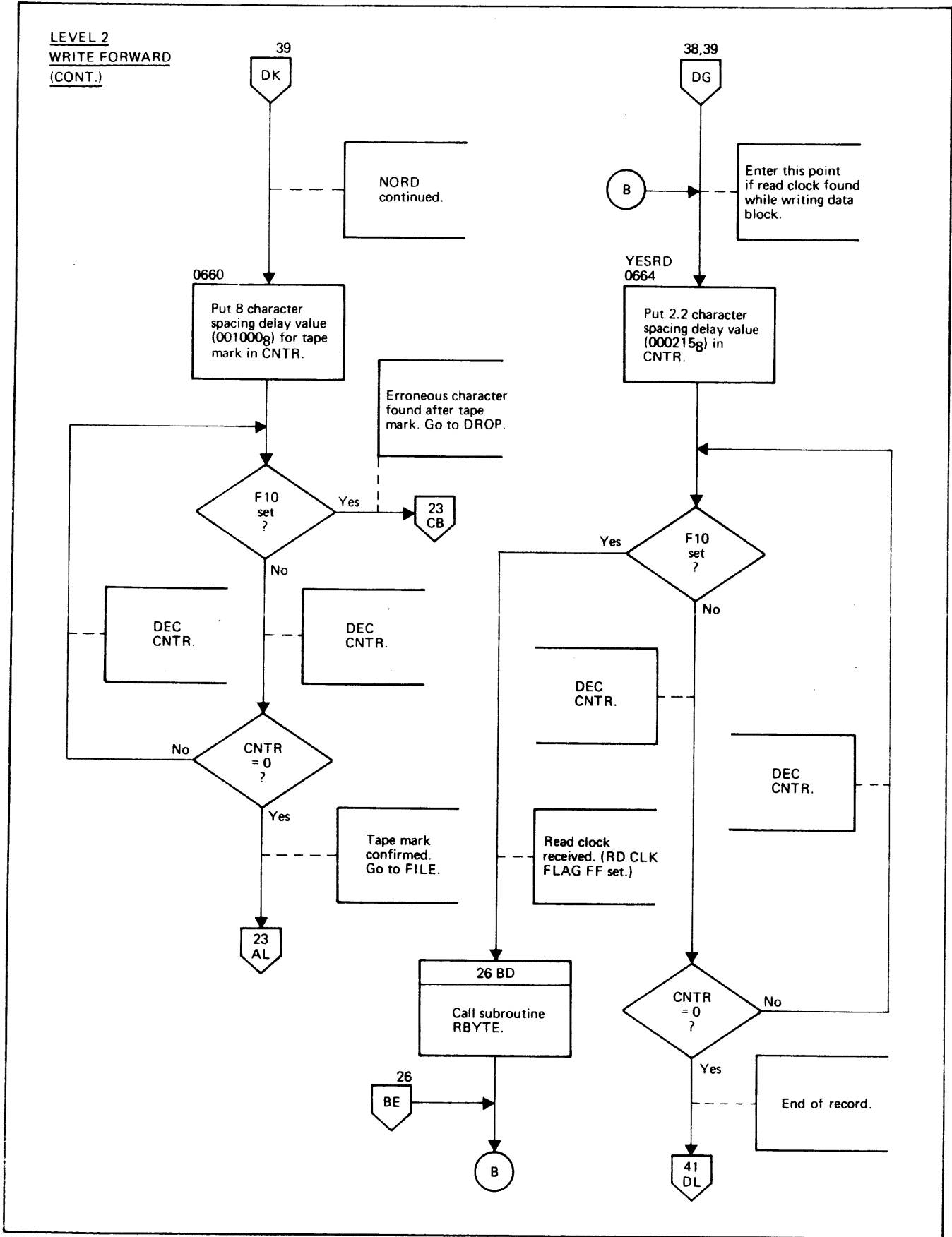
2180-97

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 38 of 58)



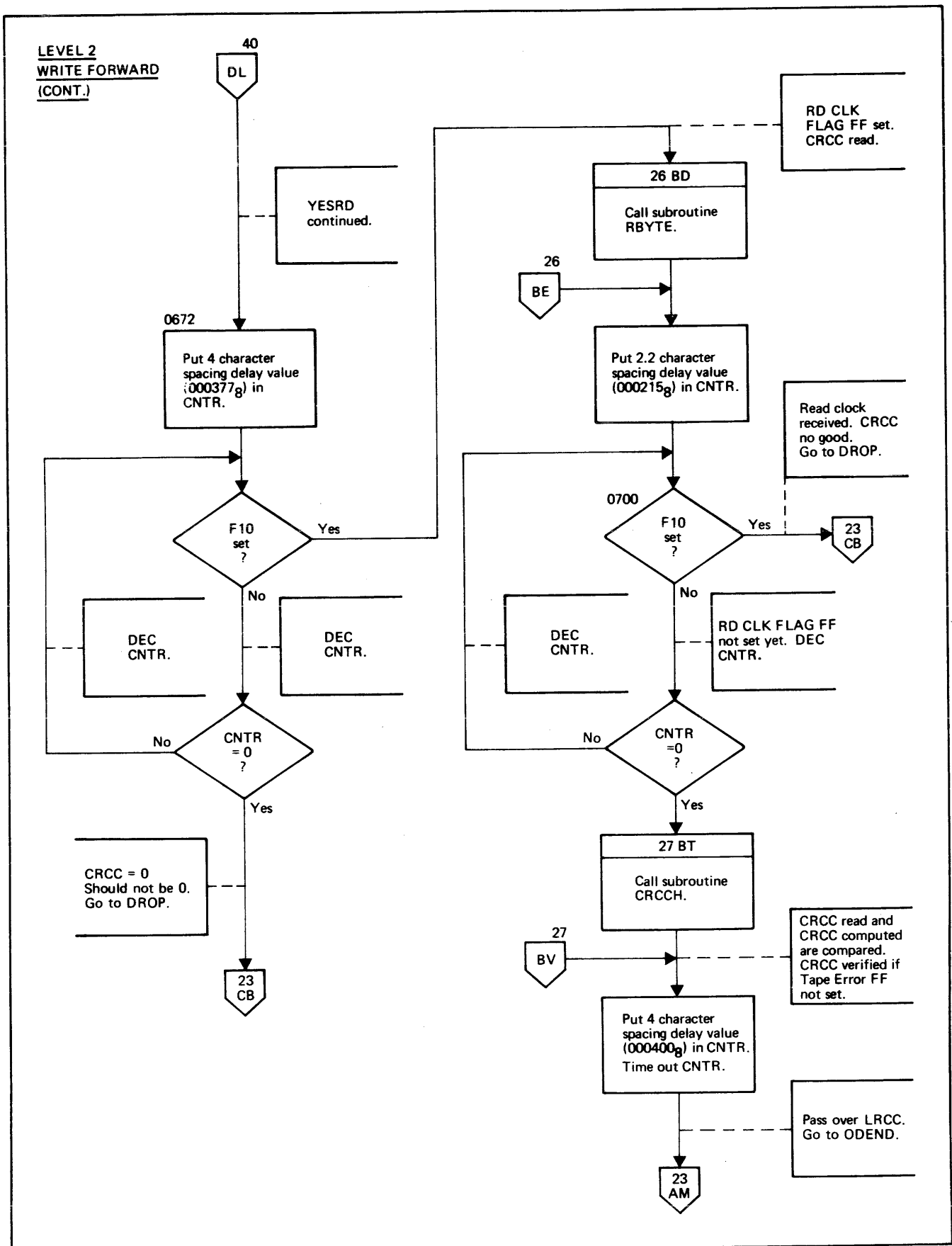
2180-98

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 39 of 58)



2180-99

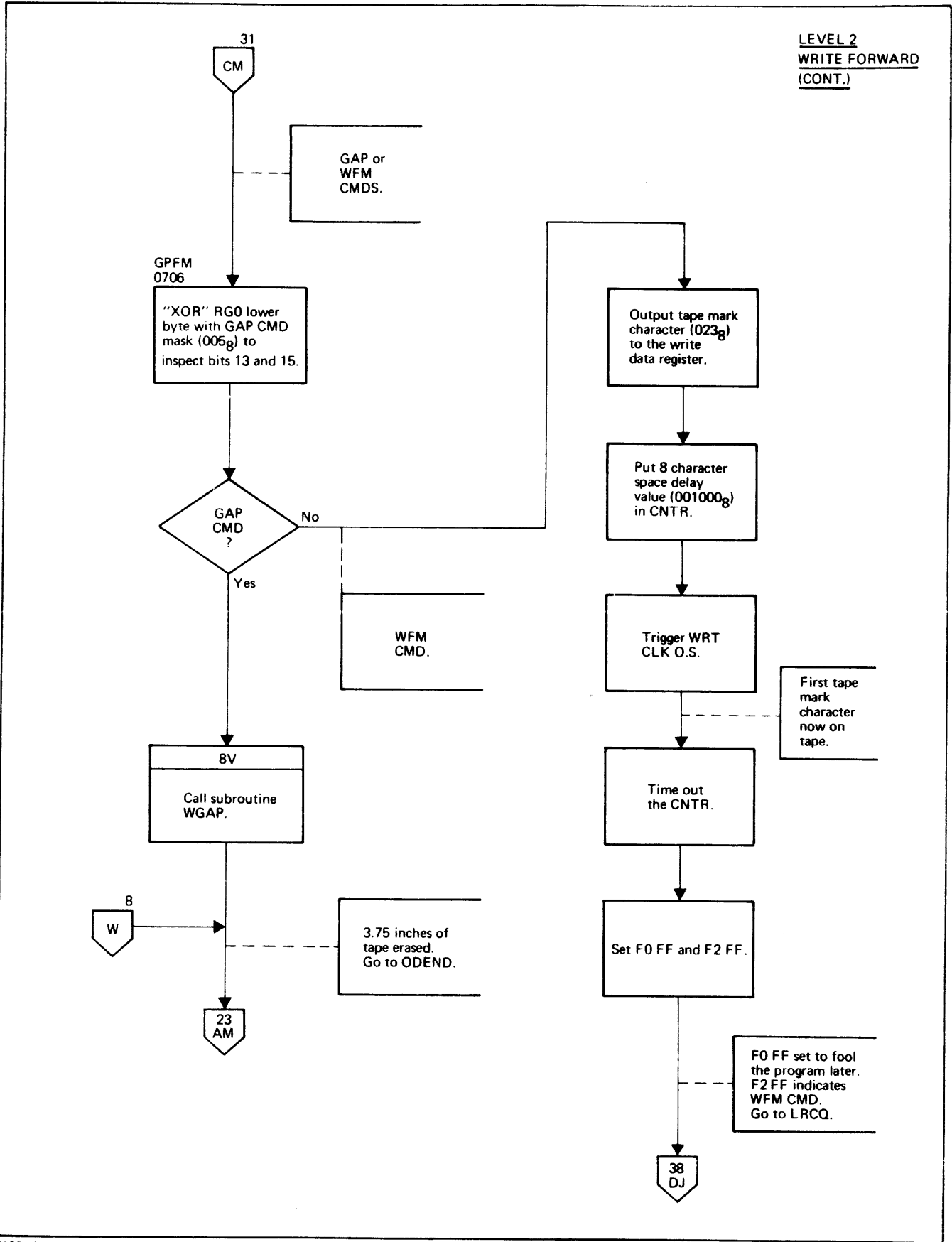
Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 40 of 58)



2180-100

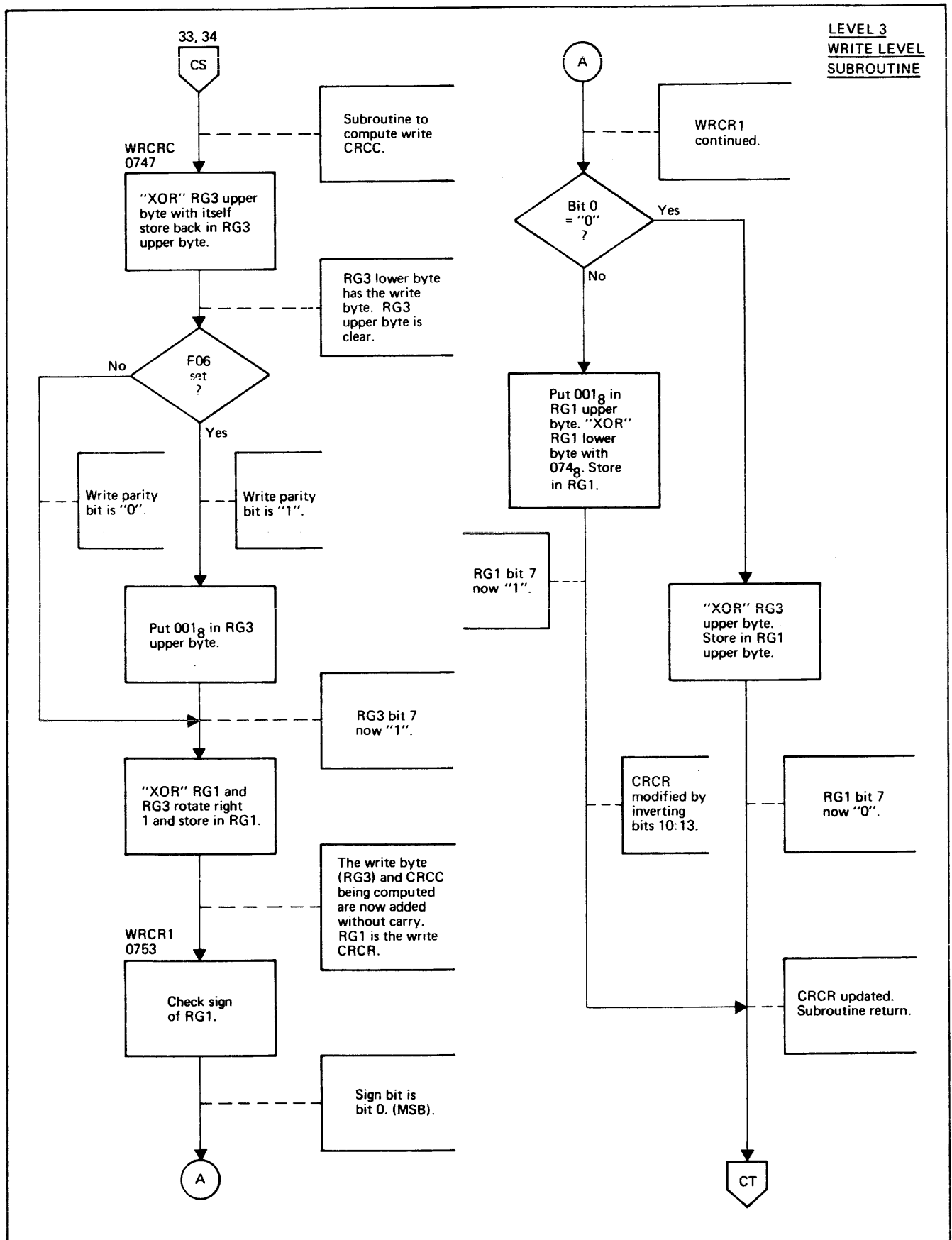
Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 41 of 58)

LEVEL 2
WRITE FORWARD
(CONT.)



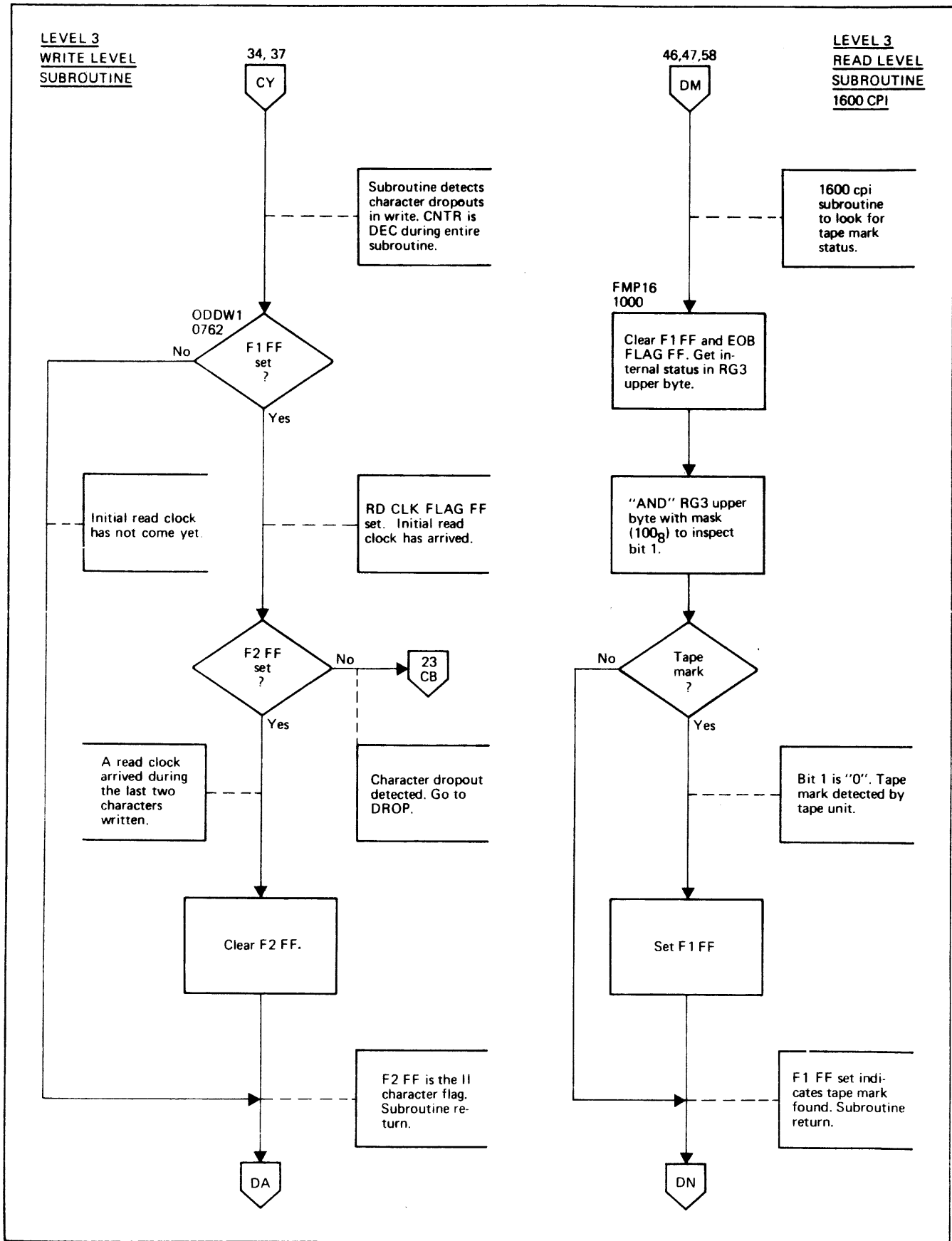
2180-101

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 42 of 58)



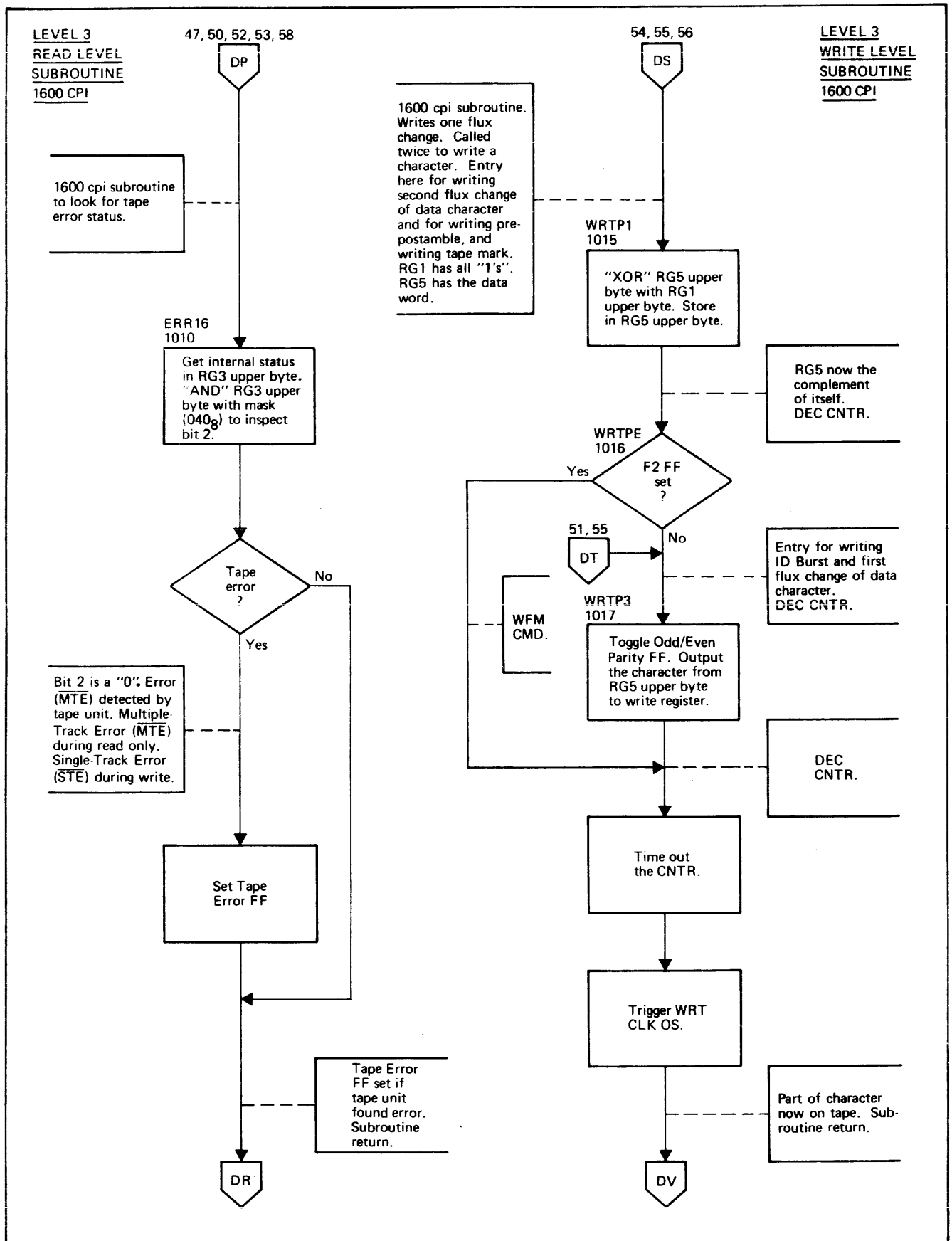
2180-102

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 43 of 58)



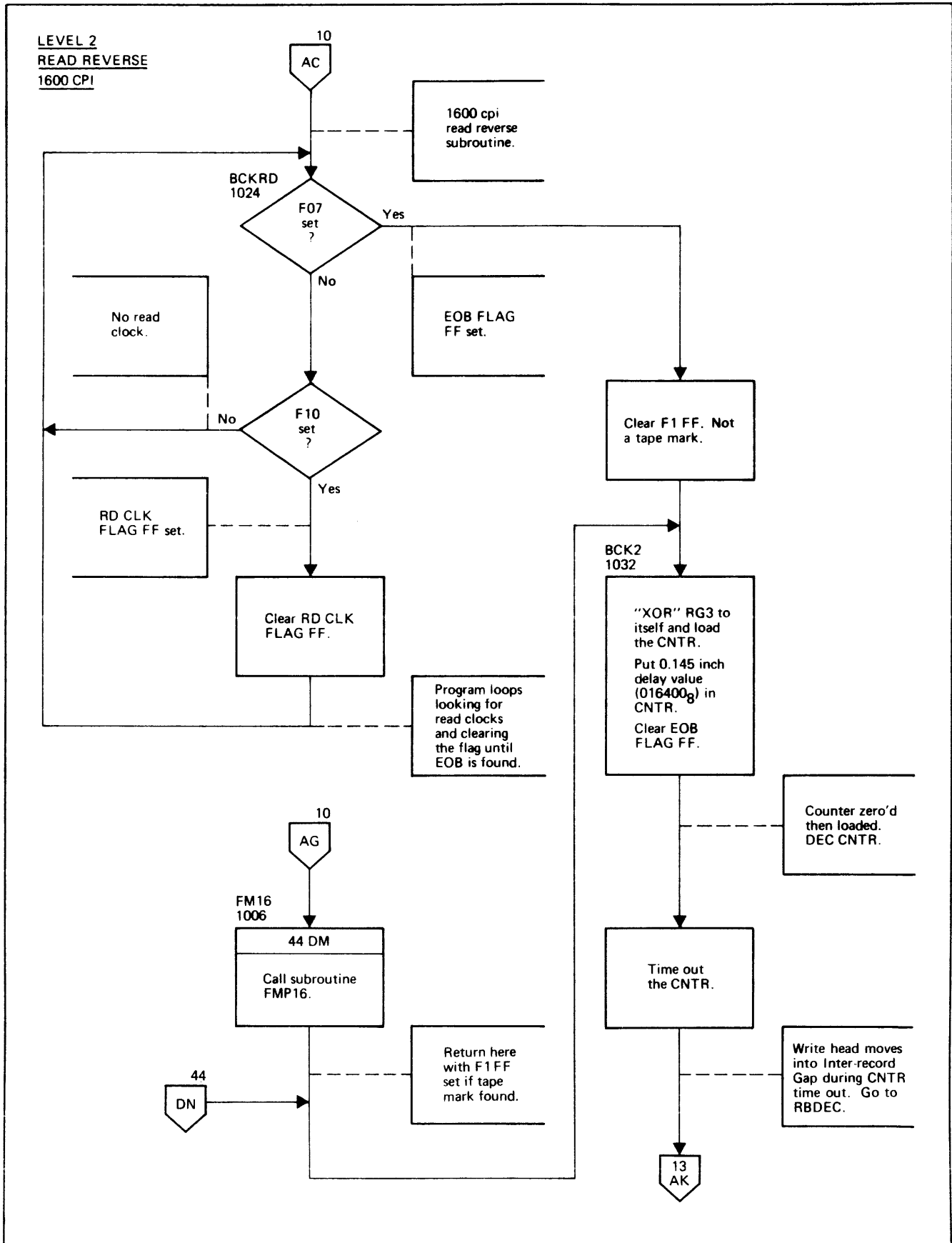
2180-103

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 44 of 58)



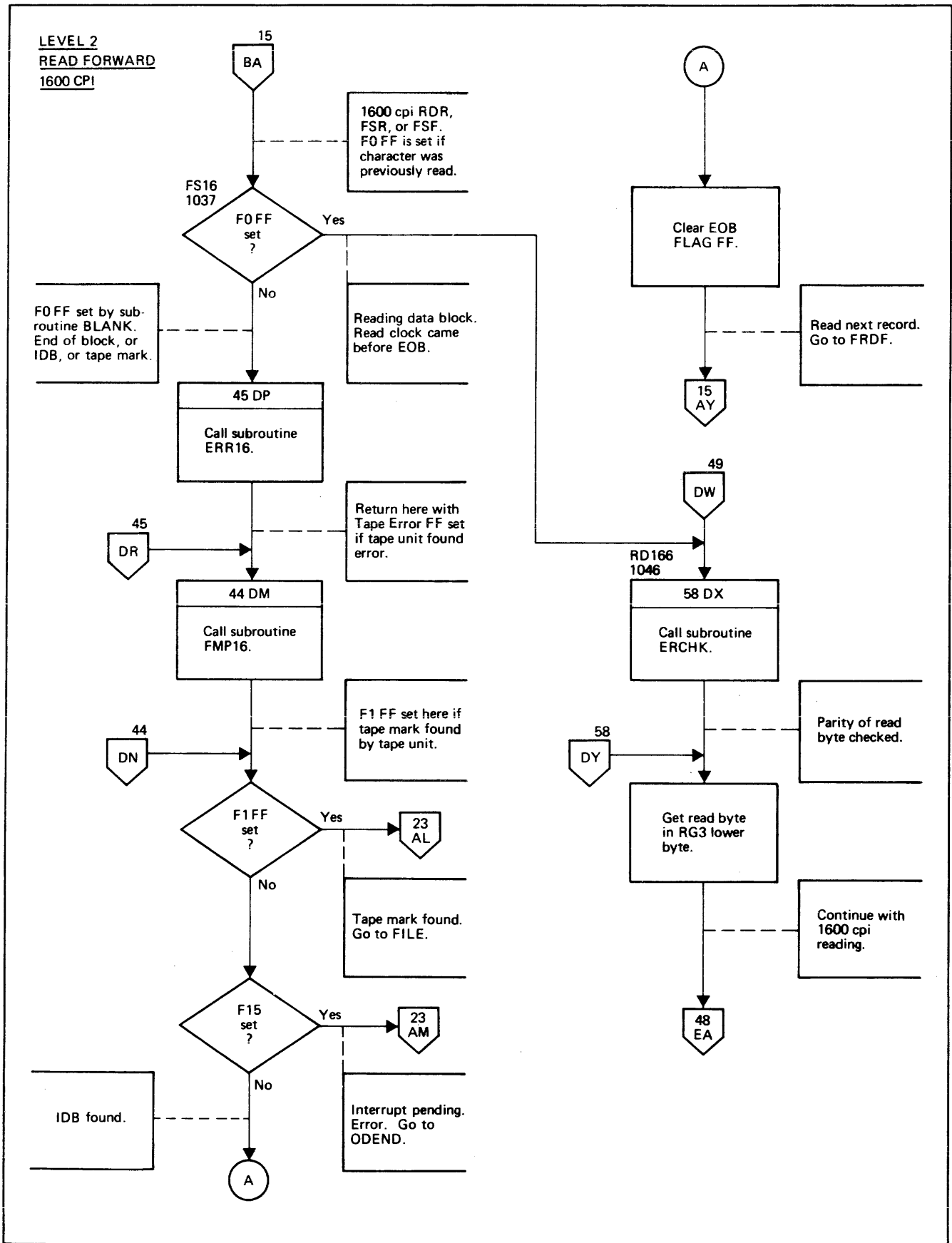
2180-104

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 45 of 58)



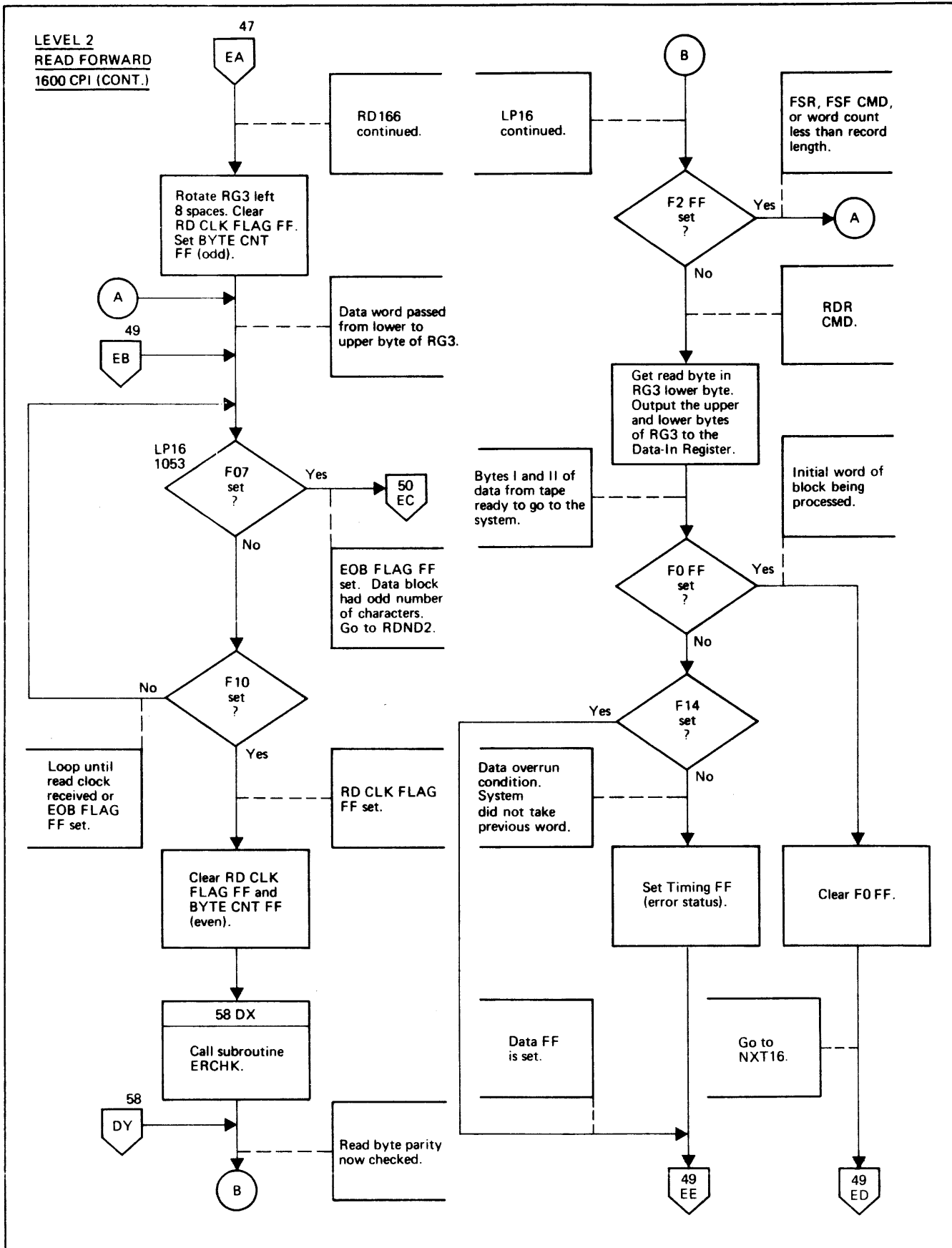
2180-105

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 46 of 58)



2180-106

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 47 of 58)



2180-107

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 48 of 58)

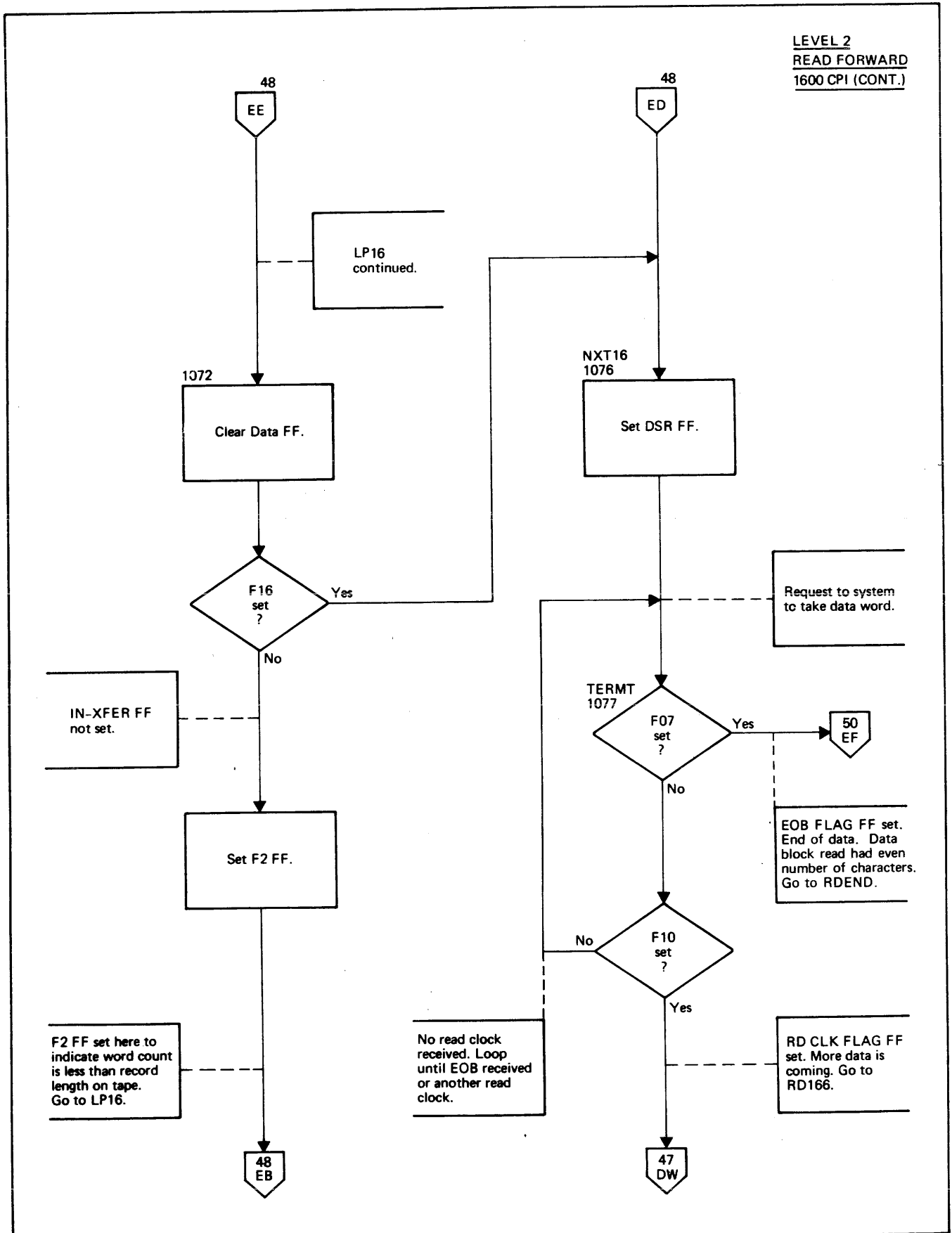
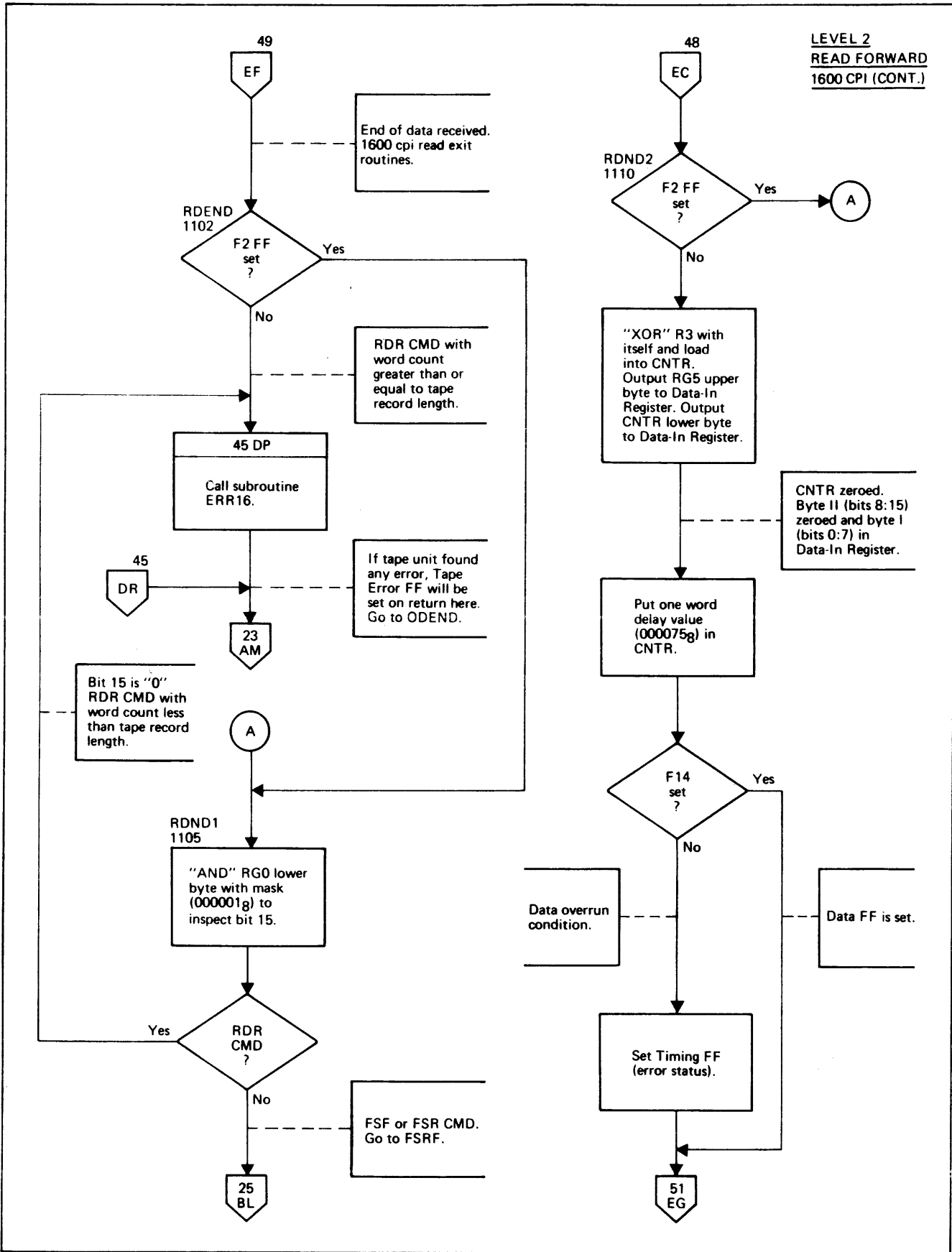


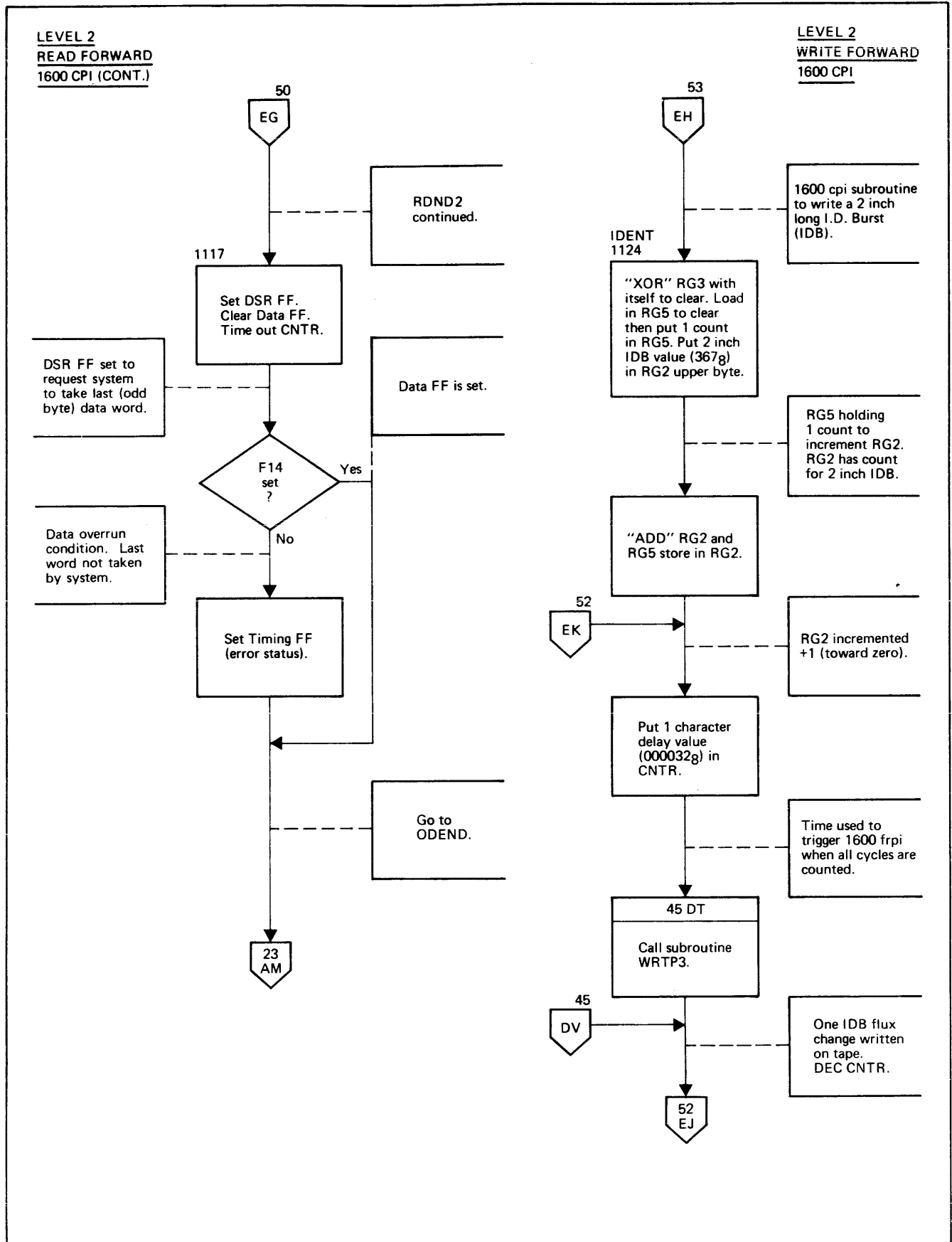
Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 49 of 58)

**LEVEL 2
READ FORWARD
1600 CPI (CONT.)**



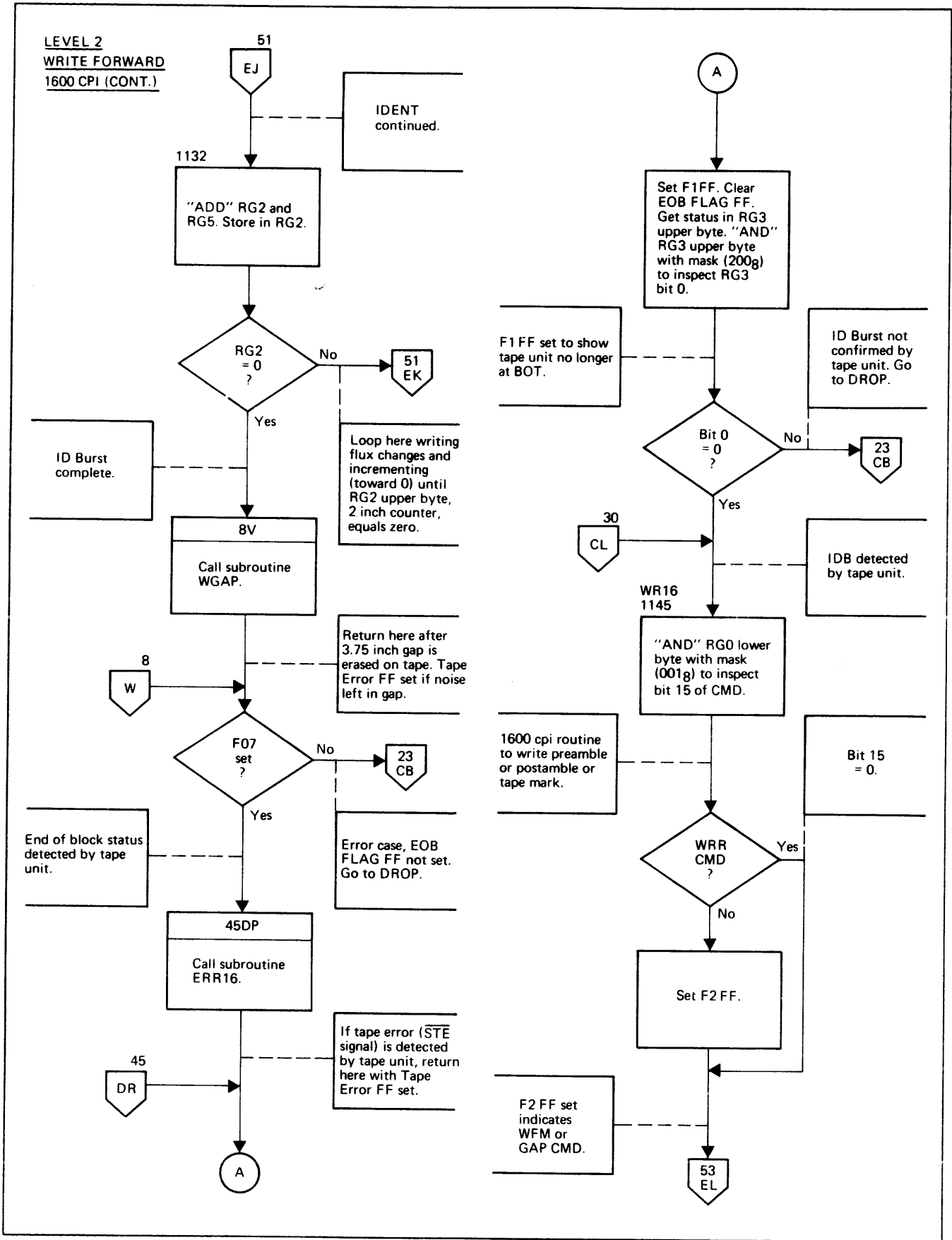
2180-109

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 50 of 58)



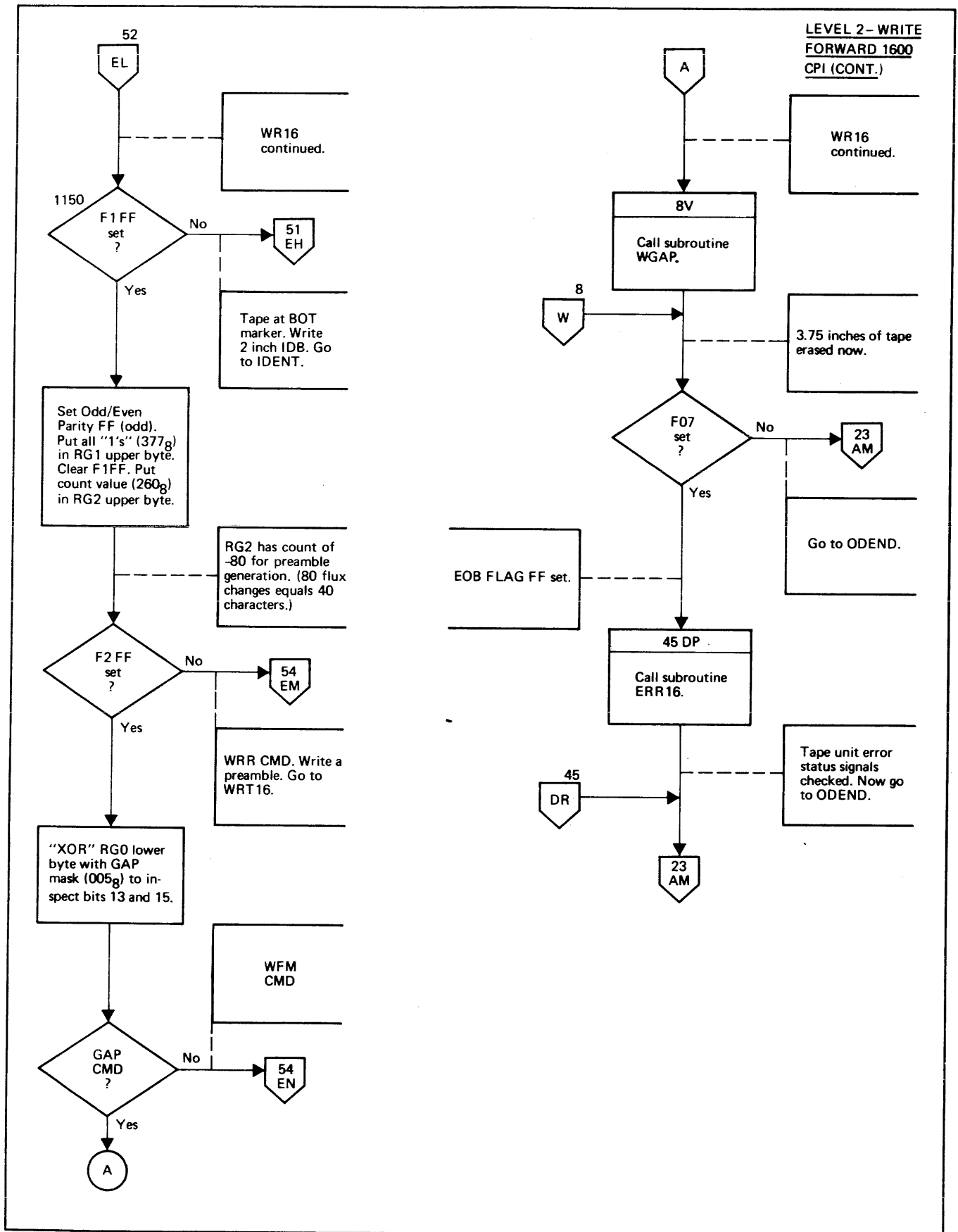
2180-110

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 51 of 58)



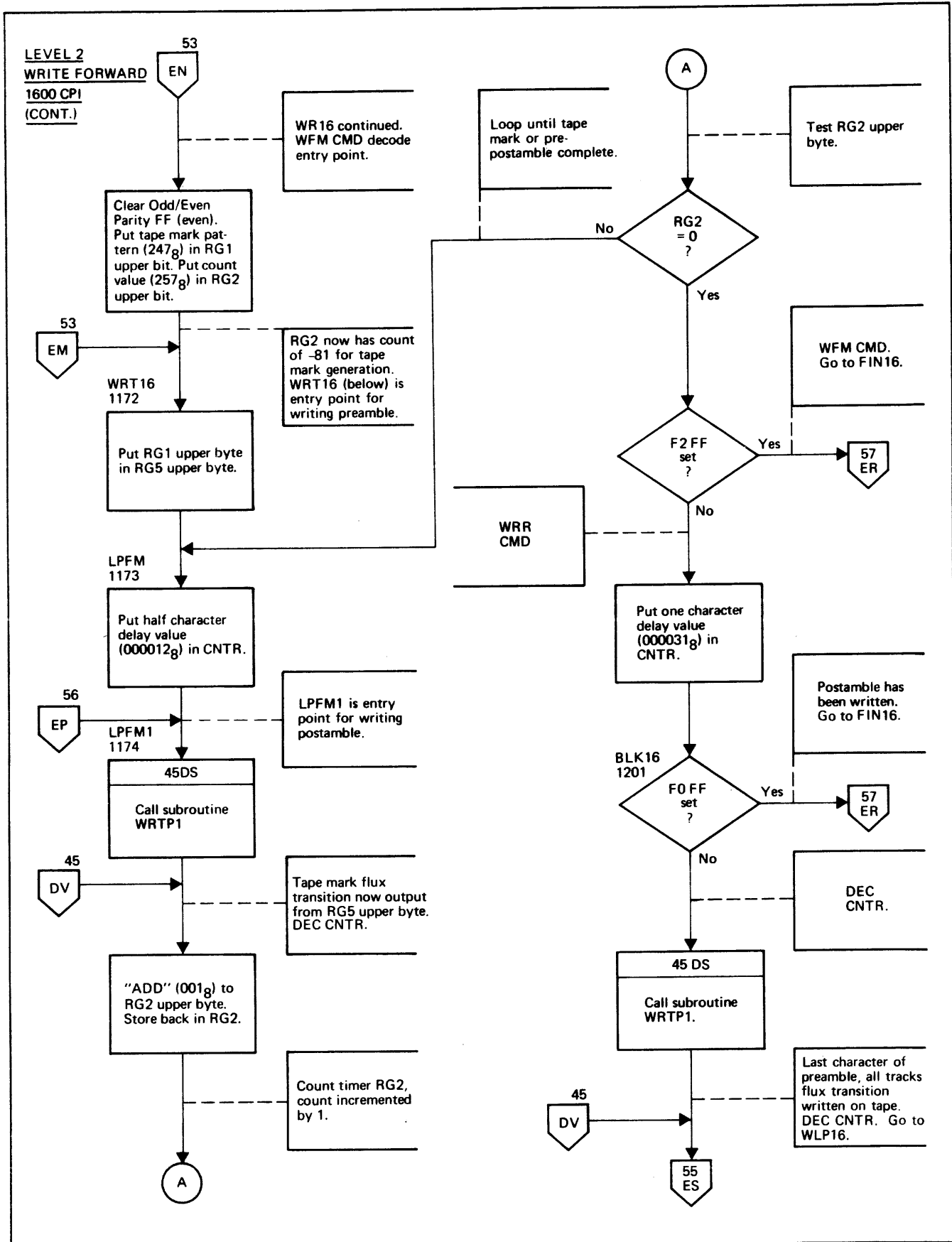
2180-111

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 52 of 58)



2180-112

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 53 of 58)

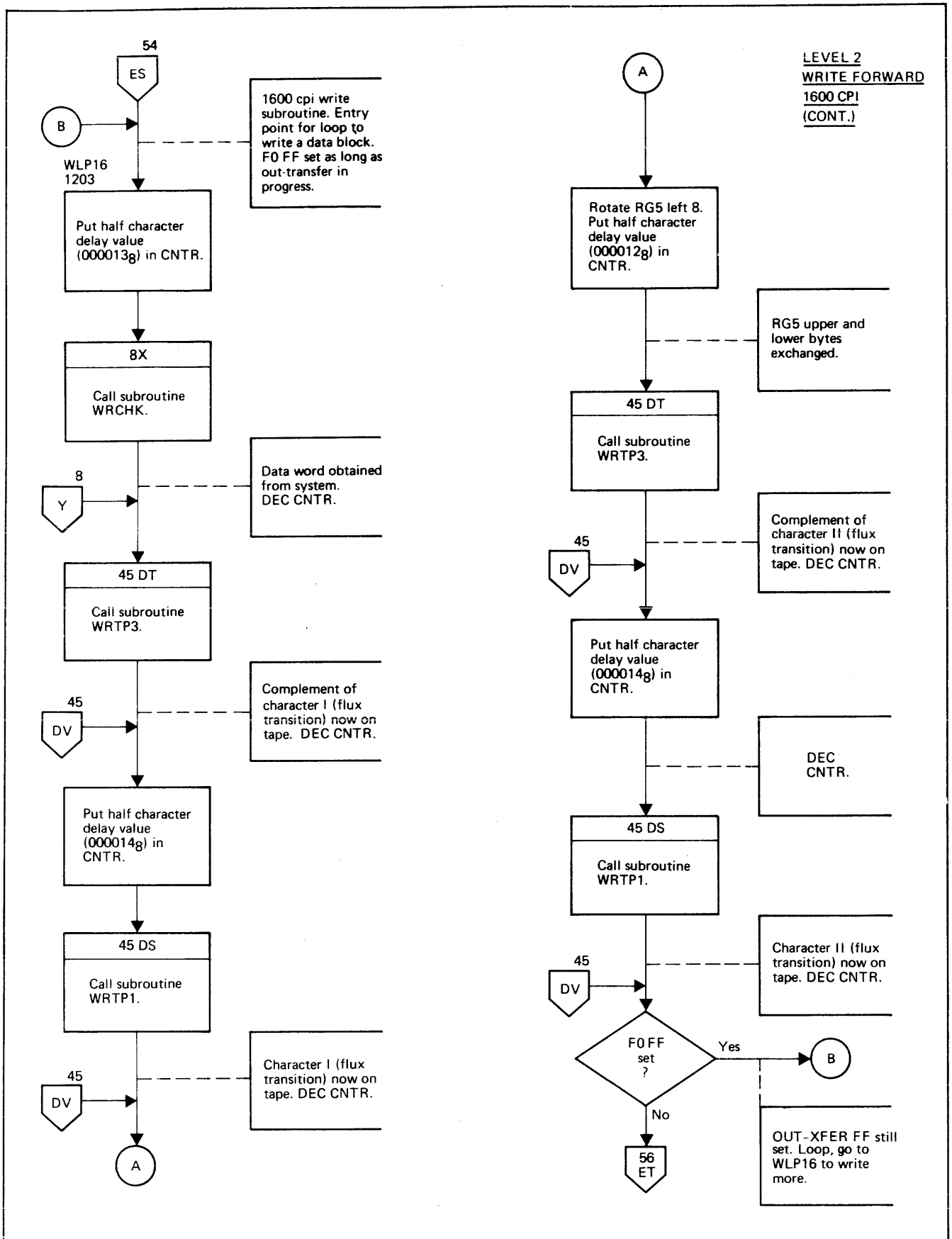


2180-113

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 54 of 58)

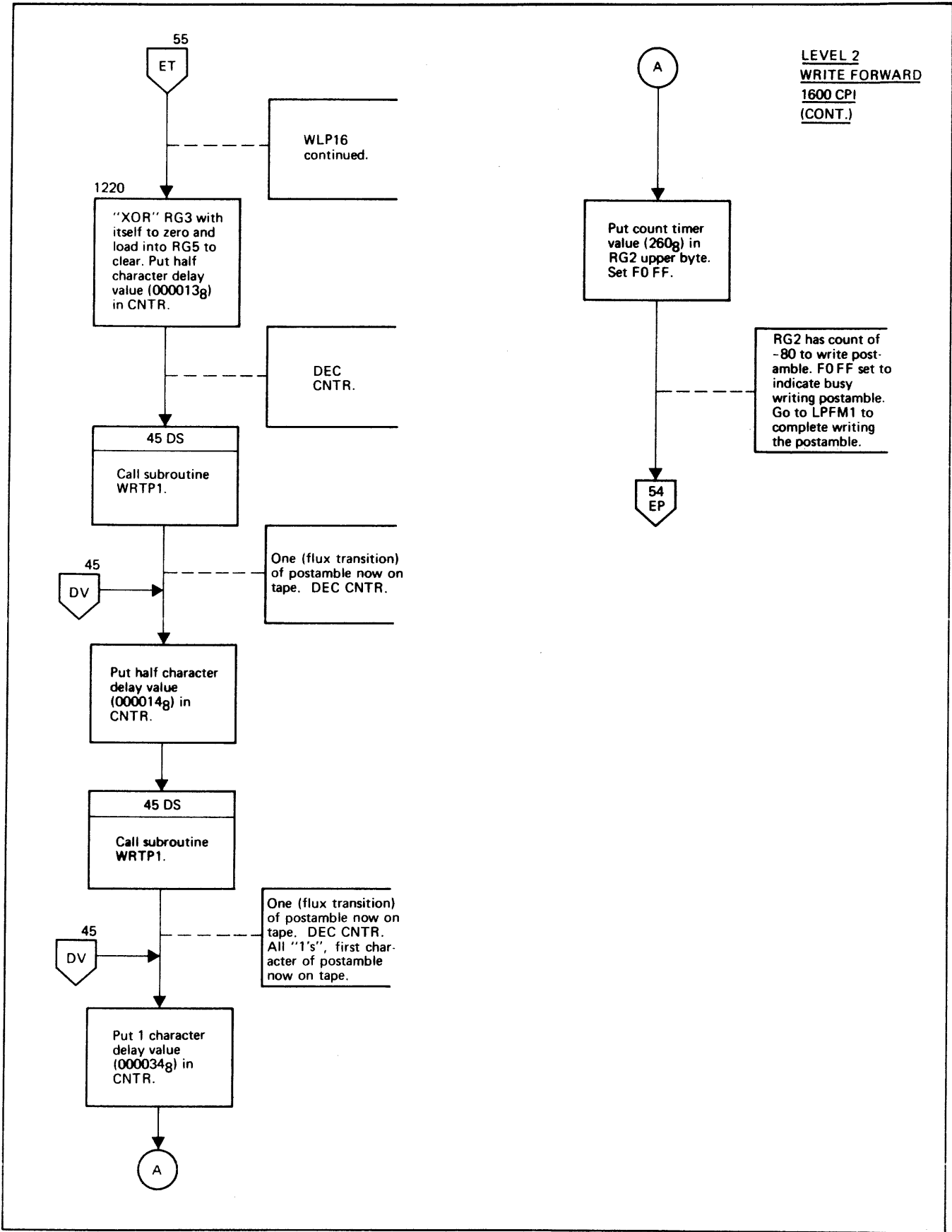
4-55AA

Changed 15 MAR 1973



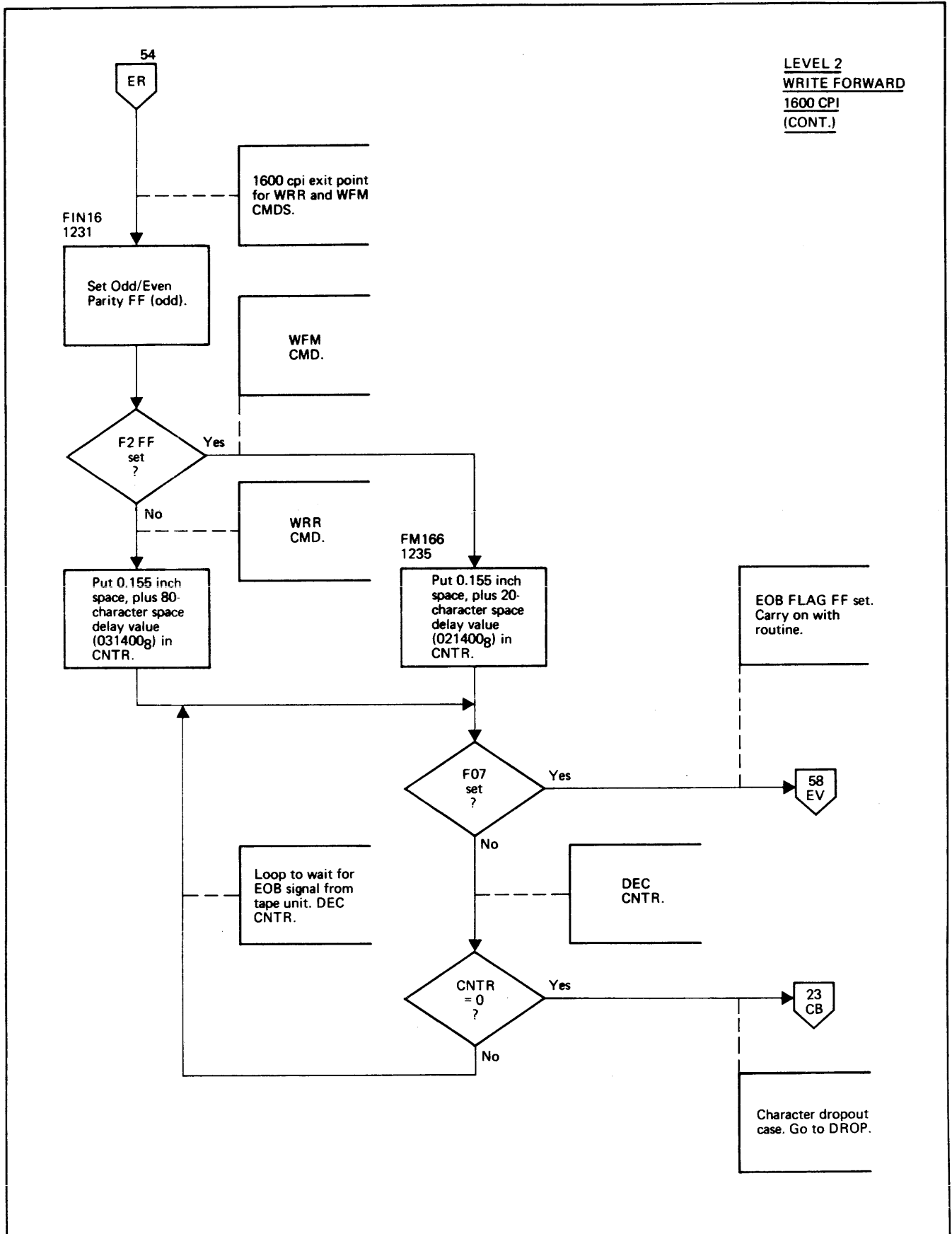
2180-114

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 55 of 58)



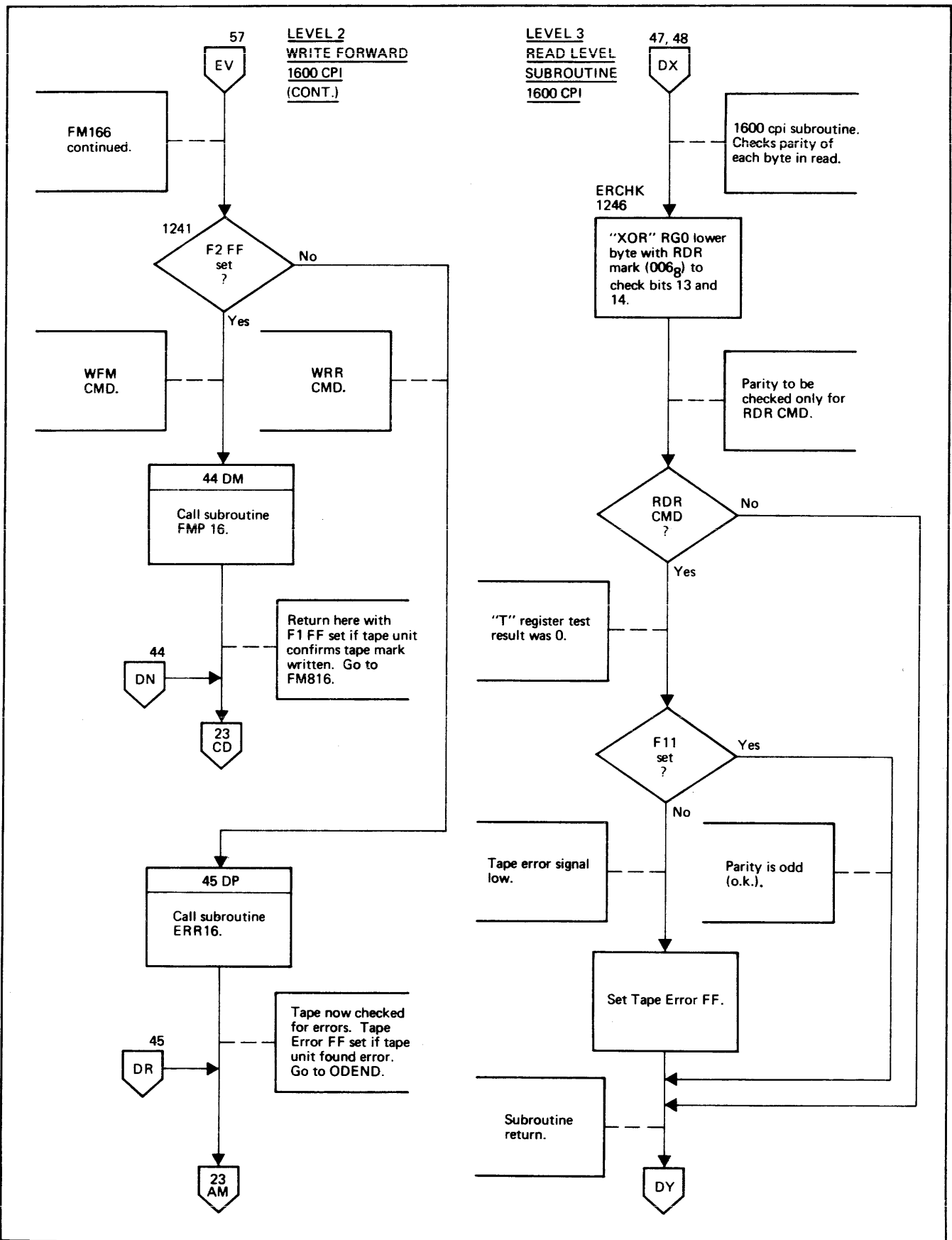
2180-115

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 56 of 58)



2180-116

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 57 of 58)



2180-117

Figure 4-10. Magnetic Tape Subsystem Microprogram Flowcharts (Sheet 58 of 58)

OP	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
IOC	0	0	0	1	0	DEC	U/L	DEST/SOURCE					FWO			I/O	REG SELECT			
ADD	0	1	0	0	1			CTM	000	R2B	00	RL1	001		CTA	00				
AND	1	1	1	1	0			R5M	001	R1B	01	RR1	010		R5A	01				
IOR	1	1	0	1	1			R4M	010	R0B	10	RL4	011		R4A	10				
XOR	1	1	0	0	1			R3M	011	R3B	11	PASS	100		R3A	11				
SUB	0	0	1	1	0			R2M	100			SL1	101							
CMA	1	0	0	0	0			R1M	101			SR1	110		(A)					SPECIAL
CMB	1	0	1	0	1			R0M	110			SL4	111							
PSA	1	1	1	1	1			EXM	111											
PSB	1	1	0	1	0	(C)				(M)	(B)		(R/S)							
ADI	0	0	0	0	1									IMMEDIATE OPERAND (ONES COMPLEMENT)						
ANI	1	0	1	1	0															
IOI	1	0	0	1	1															
XOI	1	0	0	0	1															
PSI	1	0	1	1	1															
OTI	0	0	1	1	1			DESTINATION												
JMP	0	0	0	0	0			BRANCH ADDRESS												
JMX	1	0	0	1	0															
JMZ	0	0	0	1	1			RCS												
JSZ	1	0	1	0	0															
CAL	0	1	1	1	0															
CAX	0	1	1	1	1															
CMZ	0	0	1	0	1			RCS												
CXZ	0	1	0	1	1															
JOV	1	1	0	0	0															
RMN	0	0	1	0	0															
RXN	0	1	1	0	0															
RTN	0	1	1	0	1															
JXZ	0	1	0	1	0			RCS												
RFS	1	1	1	0	1			FLAG SELECT			BRANCH ADDRESS									
JFS	1	1	1	0	0															
NOP	0	1	0	0	0															

- CTI 000
- R5I 001
- R4I 010
- R3I 011
- R2I 100
- R1I 101
- R0I 110
- EXI 111 (INPUT ONLY)

RCS = 0, reverse condition sense
 I/O = 0, output
 FWO = 0, byte op
 DEC = 0, decrement counter, else 1
 U/L = 0, lower half

2180-25

Figure 4-11. Controller Processor Consolidated Microcoding Sheet

Table 4-2. Microprogram Address-to-Label Index

ADDRESS	LABEL	ADDRESS	LABEL
0000	START	0304	INTER
0004	WAIT	0307	INT2
0007	CONT	0315	WRFWD
0013	CONT1	0337	WJOIN
0017	MAIN	0342	WRREC
0022	BEGIN	0355	FSRFO
0026	BEG2	0356	RDGO
0035	DECOD	0365	FRDF
0062	SCAN	0373	LOOPR
0065	SCAN0	0401	LOOP1
		0431	NEXT
0077	READY	0432	NEXT1
0104	GOFWD	0435	ODDEOR
0113	BLANK	0446	LREQ
0114	TIMER	0451	EVENOR
0126	NBLK	0457	YCRC
0127	NB16	0461	CRCHK
0132	WGAP	0501	CHLRC
0142	WRCHK	0507	BCK1
0153	FSRO	0513	NOFM
0154	AGAIN	0523	CHGAP
0161	FMCHK	0533	WLOOP
0175	FM816	0535	WLP1
0177	DROP	0555	WLP2
0201	FILE	0605	OTCRC
0202	ODEND	0607	OTC1
0204	STOP	0630	OTC2
0215	STOP1	0632	LRCQ
0225	FSRF	0635	NORD
0234	RBDEC	0664	YESRD
0241	RDBKD	0706	GPFM
0250	MERGE	0721	RBYTE
0252	BSRF	0725	RBITE
0260	BSRF2	0726	WBITE
0262	BACK	0731	CBITE
0274	RDFWD	0741	CRCCH
0277	RDR1	0747	WRCRC
0303	REJECT	0753	WRCR1

Table 4-2. Microprogram Address-to-Label Index (Continued)

ADDRESS	LABEL	ADDRESS	LABEL
0762	ODDWI	1105	RDND1
0770	FMPAR	1110	RDND2
1000	FMP16	1124	IDENT
1006	FM16	1145	WR16
1010	ERR16	1172	WRT16
1015	WRTP1	1173	LPFM
1016	WRTPE	1174	LPFM1
1017	WRTP3	1201	BLK16
1024	BCKRD	1203	WLP16
1032	BCK2	1231	FIN16
1037	FS16	1235	FM166
1046	RD166	1246	ERCHK
1053	LP16	1314	PTCH1
1076	NXT16	1327	PTCH2
1077	TERMT	1361	PATCH
1102	RDEND		

NOTE: Addresses and labels reflect listing dated 12/9/72.

Table 4-3. Microprogram Label, Flowchart, Address, Subroutine Index

LABEL	FLOW- CHART SHEET	ADDRESS	LEVEL (NOTE 2)	LABEL	FLOW- CHART SHEET	ADDRESS	LEVEL (NOTE 2)
AGAIN	21	0154	—	IDENT	51	1124	—
BACK	10	0262	—	INTER	28	0304	2
BCKRD	46	1024	2	INT2	28	0307	—
BCK1	11	0507	—	LOOPR	15	0373	—
BCK2	46	1032	—	LOOP1	16	0401	—
BEGIN	2	0022	—	LPFM	54	1173	—
BEG2	2	0026	1	LPFM1	54	1174	—
BLANK	7	0113	3	LP16	48	1053	—
BLK16	54	1201	—	LRCQ	38	0632	—
BSRF	9	0252	2	LREQ	18	0446	—
BSRF2	10	0260	—	MAIN	2	0017	1
CBITE	26	0731	3	MERGE	9	0250	—
CHGAP	12	0523	—	NBLK	7	0126	—
CHLRC	21	0501	—	NB16	7	0127	—
CONT	1	0007	1	NEXT	17	0431	—
CONT1	1	0013	—	NEXT1	17	0432	—
CRCCH	27	0741	3	NOFM	11	0513	—
CRCHK	19	0461	—	NORD	38	0635	—
DECOD	3	0035	—	NXT16	49	1076	—
DROP	23	0177	2	ODDEOR	18	0435	—
ERCHK	58	1246	3	ODDW1	44	0762	3
ERR16	45	1010	3	ODEND	23	0202	2
EVENOR	19	0451	—	OTCRC	35	0605	2
FILE	23	0201	2	OTC1	36	0607	—
FIN16	57	1231	—	OTC2	38	0630	—
FMCHK	22	0161	—	PATCH	24	1361	—
FMPAR	27	0770	3	PTCH1	1	1314	—
FMP16	44	1000	3	PTCH2	4	1327	—
FM16	46	1006	—	RBDEC	13	0234	2
FM166	57	1235	—	RBITE	26	0725	3
FM816	23	0175	2	RBYTE	26	0721	3
FRDF	15	0365	2	RDBKD	9	0241	2
FSRF	25	0225	2	RDEND	50	1102	—
FSRFO	14	0355	—	RDFWD	14	0274	2
FSRO	21	0153	—	RDGO	14	0356	—
FS16	47	1037	2	RDND1	50	1105	—
GOFWD	6	0104	3	RDND2	50	1110	—
GPFM	42	0706	—	RDR1	14	0277	—

Table 4-3. Microprogram Label, Flowchart, Address, Subroutine Index (Continued)

LABEL	FLOW- CHART SHEET	ADDRESS	LEVEL (NOTE 2)	LABEL	FLOW- CHART SHEET	ADDRESS	LEVEL (NOTE 2)
RD166	47	1046	—	WLP1	32	0535	—
READY	5	0077	—	WLP2	33	0555	—
REJECT	28	0303	2	WLP16	55	1203	—
SCAN	4	0062	—	WRCHK	8	0142	3
SCAN0	4	0065	—	WRCRC	43	0747	3
START	1	0000	1	WRCR1	43	0753	—
STOP	24	0204	—	WRFWD	29	0315	2
STOP1	24	0215	—	WRREC	30	0342	—
TERMT	49	1077	—	WRTPE	45	1016	—
TIMER	7	0114	—	WRTP1	45	1015	3
WAIT	1	0004	1	WRTP3	45	1017	3
WBITE	26	0726	—	WRT16	54	1172	—
WGAP	8	0132	3	WR16	52	1145	2
WJOIN	30	0337	—	YCRC	19	0457	—
WLOOP	31	0533	—	YESRD	40	0664	2

NOTES: 1. Addresses and labels reflect listing dated 12/9/72.
 2. Number indicates microprogram routine/subroutine level. Entry points only are numbered.

Table 4-4. Magnetic Tape Subsystem Microprogram Listing

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*
* XXXXX  XXXXX XXXXX X  X  X  X XXXXX XXXXX  XXXXX XXXXX XXXXX XXXXX
* X  X  X  X  X X X  XX XX X  X X  X  X  X  X  X  X  X  X
* X  X  X  X  X X X  X X X  X X  X  X  X  X  X  X  X
* XXXXX  X  XXXXX XX  X  X XXXXX X  X  XXXXX XXXXX XXXX
* X  X  X X X X X  X  X X  X X XX  X  X  X X  X
* X  X  X  X X X X  X  X X  X X X  X  X  X X X  X
* X  X  X  X X  X X X  X  X XXXXX X  X  X  X X  XXXXX
*
***** LISTING DATED 12/9/72 *****
*
*   CONSTANTS USED FOR TIMING CONTROL IN THE MAG. TAPE CONTROLLER
*
*****
****   **DATA XFER TIMING DELAYS**
T1 EQU #75 1 CHARACTER TIME(L)
T22 EQU #215 2.2 CHARACTER GATE FOR READING(L)
T4 EQU 1 4 CHARACTER SPACING FOR CRCC & LRCC(H)
T62 EQU #306 6.2 CHARACTER TIME(L)-SHOULD BF DOUBLED
T8 EQU 2 8 CHARACTER SPACING FOR FILE MARK(4)
T12 EQU 3 12 CHARACTER SPACING FOR BACKSPACING(H)
****   **START/STOP DELAYS OF CAPSTAN**
TCOST EQU #356 COAST DELAY FOR 103 USEC.
TSTRT EQU #113 START DELAY FOR .2 INCH(H)
TWSTR EQU #133 START DELAY FOR WRITE
TSTOP EQU #113 STOP DELAY FOR .2 INCH(H)
TIRG EQU #113 (START+STOP) COAST I/R DELAY FOR .4 INCH
****   **DELAYS RELATING TO R/W HEADS**
T145 EQU #35 MIN. & MAX. HEAD SPACING(H)
T155 EQU #37 DELAY AT FULL SPEED(H)
T15 EQU #74 NOM. HEAD SPACING DELAY AT HALF SPEED(H)
TS155 EQU #152 (MAX. HEAD + START) COAST DELAY(H)
TGAP EQU #372 DELAY FOR 1.25 INCH-(1/3 OF GAP) (H)
****
FM EQU #23 FILE/MARK CODE FOR 800 BPI
*****
*
*   COMMAND CODES FOR THE CONTROLLER
*
*****
SEL EQU 0 SELFCT THE UNIT
RDR EQU #6 READ RECORD
RDC EQU #16 READ RECORD WITH CRCC(800 BPI ONLY)
FSR EQU #7 FORWARD SPACE RECORD
FSF EQU #17 FORWARD SPACE FILE
WRR EQU #4 WRITE RECORD
WRZ EQU #14 WRITE RECORD WITH 0 PARITY(800 BPI ONLY)
WFM EQU #15 WRITE FILE-MARK
GAP EQU #5 WRITE A GAP
BSR EQU #12 BACK-SPACE RECORD
BSF EQU #13 BACK SPACE FILE
REW EQU #10 REWIND THE TAPE UNIT
RST EQU #11 REWIND & RESET
RDREV EQU #2 READ-REV. SUB GROUP
*****
SKP

```

- NOTES:
1. FILE-MARK AND TAPE MARK ARE SYNONYMOUS.
 2. CLEAR AND RESET ARE SYNONYMOUS.
 3. RO:R5 REFER TO CONTROLLER PROCESSOR REGISTERS R0:RG5.
 4. SEE TEXT FOR COMPLETE COPY OF CODING SHEET.

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

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*****
*
*           REFERENCE CODING SHEET FOR THE CONTROLLER PROCESSOR
*
*****
* OP * 0 1 * 2 3 4 * 5 6 7 * 8 9 10 * 11 12 13 * 14 15 16 * 17 18 19*
*****
* IOC * 0 0 * 0 1 0 *DEC*U/L*   DEST/SOURCE   *   *FWO*I/O*RFG SELECT*
* ADD * 0 1 * 0 0 1 *DEC*U/L*   CTM 000 * R2B 00* RL1 001 *FWO* CTA 00 *
* AND * 1 1 * 1 1 0 *   *   * R5M 001 * R1B 01* RR1 010 *   * P5A 01 *
* IOR * 1 1 * 0 1 1 *   *   * R4M 010 * R0B 10* RL4 011 *   * R4A 10 *
* XOR * 1 1 * 0 0 1 *   *   * R3M 011 * R3B 11* PASS 100 *   * R3A 11 * SPEC*
* SUR * 0 0 * 1 1 0 *   *   * R2M 100 *   *   * SL1 101 *   *   *
* CMA * 1 0 * 0 0 0 *   *   * R1M 101 *   *   * SR1 110 *   *   *
* CMP * 1 0 * 1 0 1 *   *   * ROM 110 *   *   * SL4 111 *   *   *
* PSA * 1 1 * 1 1 1 *   *   * EXM 111 *   *   *   *   *
* PSR * 1 1 * 0 1 0 *   *   *   *   *   *   *   *
*****
* ADI * 0 0 * 0 0 1 *DEC*U/L*   *   *   *
* ANI * 1 0 * 1 1 0 *   *   *   *   * IMMEDIATE
* IOI * 1 0 * 0 1 1 *   *   *   *   * OPERAND
* XOI * 1 0 * 0 0 1 *   *   *   *   * (ONES COMPLEMENT)
* PSI * 1 0 * 1 1 1 *   *   *   *   *
*****
* OTI * 0 0 * 1 1 1 *DEC*U/L*   DESTINATION * IMMEDIATE OPERAND
*****
* JMP * 0 0 * 0 0 0 *DEC* * * *   *   * BRANCH ADDRESS
* JMX * 1 0 * 0 1 0 *   * * * *   *   *
* JMZ * 0 0 * 0 1 1 *   * RCS* *   *   *
* JSZ * 1 0 * 1 0 0 *   * * * *   *   *
* CAL * 0 1 * 1 1 0 *   * * * *   *   *
* CAX * 0 1 * 1 1 1 *   * * * *   *   *
* CMZ * 0 0 * 1 0 1 *   * RCS* *   *   *
* CXZ * 0 1 * 0 1 1 *   * * * *   *   *
* JOV * 1 1 * 0 0 0 *   * * * *   *   *
* RMN * 0 0 * 1 0 0 *   * * * *   *   *
* RXN * 0 1 * 1 0 0 *   * * * *   *   *
* RTN * 0 1 * 1 0 1 *   * * * *   *   *
* JXZ * 0 1 * 0 1 0 *   * RCS* *   *   *
*****
* RFS * 1 1 * 1 0 1 *DEC*   FLAG *   * BRANCH
* JFS * 1 1 * 1 0 0 *   *   * SELECT *   * ADDRESS
*****
* RCS = 0*REVERSE CONDITION SFNSE
* I/O = 0*OUTPUT
* FWO = 0*BYTE OPERATION
* DEC = 0*DECREMENT COUNTER
* U/L = 0*LOWER HALF
*****
SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

108 *****
109 *
110 *   CONTROLLER PROCESSOR SIGNALS (CONNECTOR J2)
111 *
112 *****
113 *
114 * 1  GND      GROUND
115 * 2  GND      GROUND
116 * 48 RAR11   ROM ADDRESS BIT 11 (LSB)
117 * 47 RAR10   ROM ADDRESS BIT 10
118 * 46 RAR9    ROM ADDRESS BIT 9
119 * 45 RAR8    ROM ADDRESS BIT 8
120 * 44 RAR7    ROM ADDRESS BIT 7
121 * 43 RAR6    ROM ADDRESS BIT 6
122 * 42 RAR5    ROM ADDRESS BIT 5
123 * 41 RAR4    ROM ADDRESS BIT 4
124 * 40 RAR3    ROM ADDRESS BIT 3
125 * 39 RAR2    ROM ADDRESS BIT 2
126 * 38 RAR1    ROM ADDRESS BIT 1
127 * 37 RAR0    ROM ADDRESS BIT 0 (MSB)
128 * 33 ROM19   ROM OUTPUT BIT 19 (LSB)
129 * 31 ROM18   ROM OUTPUT BIT 18
130 * 29 ROM17   ROM OUTPUT BIT 17
131 * 27 ROM16   ROM OUTPUT BIT 16
132 * 25 ROM15   ROM OUTPUT BIT 15
133 * 23 ROM14   ROM OUTPUT BIT 14
134 * 21 ROM13   ROM OUTPUT BIT 13
135 * 19 ROM12   ROM OUTPUT BIT 12
136 * 17 ROM11   ROM OUTPUT BIT 11
137 * 15 ROM10   ROM OUTPUT BIT 10
138 * 13 ROM9    ROM OUTPUT BIT 9
139 * 11 ROM8    ROM OUTPUT BIT 8
140 * 9  ROM7    ROM OUTPUT BIT 7
141 * 7  ROM6    ROM OUTPUT BIT 6
142 * 5  ROM5    ROM OUTPUT BIT 5
143 * 3  ROM4    ROM OUTPUT BIT 4
144 * 34 ROM3    ROM OUTPUT BIT 3
145 * 32 ROM2    ROM OUTPUT BIT 2
146 * 30 ROM1    ROM OUTPUT BIT 1
147 * 28 ROM0    ROM OUTPUT BIT 0 (MSB)
148 * 36 ENB     ROM ENABLE
149 * 49 GND     GROUND
150 * 50 GND     GROUND
151 *
152 *****
153 SKP

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Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

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*****
*
*   CONTROLLER PROCESSOR SIGNALS (CONNECTOR J3)
*
*****
* 47 M0      MIO BUS BIT 0 (MSB)
* 45 M1      MIO BUS BIT 1
* 43 M2      MIO BUS BIT 2
* 41 M3      MIO BUS BIT 3
* 42 M4      MIO BUS BIT 4
* 44 M5      MIO BUS BIT 5
* 46 M#      MIO BUS BIT 6
* 48 M7      MIO BUS BIT 7
* 40 M8      MIO BUS BIT 8
* 38 M9      MIO BUS BIT 9
* 36 M10     MIO BUS BIT 10
* 34 M11     MIO BUS BIT 11
* 31 M12     MIO BUS BIT 12
* 33 M13     MIO BUS BIT 13
* 35 M14     MIO BUS BIT 14
* 37 M15     MIO BUS BIT 15 (LSB)
* 8  IS      INPUT STROBE
* 10 LOS     LOWER OUTPUT STROBE
* 7  UOS     UPPER OUTPUT STROBE
* 18 ROR7    DESTINATION BIT 7 (MSB)
* 6  ROR9    DESTINATION BIT 9
* 20 ROR10   DESTINATION BIT 10
* 15 ROR8    DESTINATION BIT 8
* 17 ROR11   DESTINATION BIT 11 (LSB)
* 1  GND     GROUND
* 2  CLR     CLEAR RAR TO 0
* 3  T0      CLOCK PHASE 0
* 4  T3      CLOCK PHASE 3
* 5  T2      CLOCK PHASE 2
* 39 T1      CLOCK PHASE 1
* 32 EXT SEL EXTERNAL SELECT
* 49 RUN     FROM MAINTENANCE PANEL
* 50 GND     GROUND
*****
SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

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*****
*
*   DEVICE CABLE CONNECTIONS (CONNECTOR J1)
*
*****
*   J1      WRT. RD.  C/S      NAME OF SIGNAL
*           (SIG/GND)
*
*****
*
*   33/27  L/10          WRITE DATA 0-WD0(MSB)
*   34/27  M/11          WRITE DATA 1-WD1
*   39/27  N/12          WRITE DATA 2-WD2
*   40/27  P/13          WRITE DATA 3-WD3
*   37/28  R/14          WRITE DATA 4-WD4
*   38/28  S/15          WRITE DATA 5-WD5
*   35/28  T/16          WRITE DATA 6-WD6
*   36/28  U/17          WRITE DATA 7-WD7(LSB)
*   10/28  K/9           WRITE DATA PARITY-WDP
*   11/28  F/6           WRITE STATUS-SW
*   30/27  J/8           WRITE CLOCK-WC
*   22/27  H/7           WRITE RESET-WRS
*
*   47/50          L/10   READ DATA 0-RD0(MSB)
*   48/50          M/11   READ DATA 1-RD1
*   45/50          N/12   READ DATA 2-RD2
*   46/50          P/13   READ DATA 3-RD3
*   43/49          R/14   READ DATA 4-RD4
*   44/49          S/15   READ DATA 5-RD5
*   41/49          T/16   READ DATA 6-RD6
*   42/49          U/17   READ DATA 7-RD7(LSB)
*   9/25           K/9    READ DATA PARITY-RDP
*   8/23           J/8    READ CLOCK-RC
*   7/23           BB/24  END OF BLOCK-FOB
*   12/26          V/18   800/1600 BPI STATUS-SD16
*   31/26          X/20   MULTIPLE TRACK IN ERROR-MTE
*   32/26          Y/21   TAPE MARK-TM
*   2/26           Z/22   SINGLE TRACK IN ERROR-STE
*   29/26          AA/23  IDENTIFICATION BURST-IDB
*   3/23           P/13   SELECT UNIT 0-CS0
*   4/23           N/12   SELECT UNIT 1-CS1
*   5/24           M/11   SELECT UNIT 2-CS2
*   6/24           L/10   SELECT UNIT 3-CS3
*   13/23          B/2    LOAD POINT(BOT)-SLP
*   16/23          D/4    END OF TAPE(EOT)-SET
*   14/24          E/5    READY-SR
*   15/24          F/6    FILE PROTECT-SFP
*   17/24          T/16   FORWARD-CF
*   21/24          R/14   REWIND-CRW
*   18/25          U/17   REVERSE-CR
*   20/25          S/15   OFF LINE-CL
*   19/25          W/19   SET WRITE-WSW
*
*****
*
*   SKP
*
*****

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

4-66
 Changed 31 JAN 1973

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*****
*
*           DESTINATION CODES FOR OUTPUT FUNCTIONS
*
*****
*   D00      7970                      RD. CLK. F/F
*   D01      STATUS                    IS NOT CHANGED
*   D02      XFACE                      IN D00,D01 & D02
*   D03      WRITE REGISTER
*   D04      7970 + RESET RD. CLK.F/F
*   D05      STATUS + RESET RD. CLK. F/F
*   D06      XFACE + RESET RD. CLK. F/F
*   D07      DATA-IN REGISTER
*   D1X      RESET CMD. ENB. F/F        X IS ANY OCTAL DIGIT-
*   D2X      SET SERV. REQ. F/F        THESE 3 PERFORM ANY OF
*   D3X      SET SERV. REQ. & RST. CMD. ENB. F/F ABOVE + D1X,D2X & D3X
*
*****
*
*           SOURCE CODES FOR INPUT FUNCTIONS
*
*****
*   D20,24   UNIT NO.
*   D11,15   LOW BYTE OF DATA-OUT
*   D21,25   HIGH BYTE OF DATA-OUT
*   D31,35   FULL WORD OF DATA-OUT
*   D12,16   8-BITS OF READ DATA (RD0 THRU RD7)
*   D22,D26  8-BITS OF STATUS
*   D32,36   RD. DATA & STATUS
*
*****
*
*           NAMES OF THE EXTERNAL FLAGS ARE AS FOLLOWS
*
*****
*   29 F00   FLAG0
*   30 F01   FLAG1
*   27 F02   FLAG2
*   28 F03   LOAD POINT(BOT)
*   25 F04   800/1600 RPI(800=0)
*   26 F05   WRITE STATUS
*   23 F06   RD/WRT PARITY(REV. SENSE FOR WRITE PARITY)
*   24 F07   END OF BLOCK F/F(USED IN 1600 BPI ONLY)
*   9  F10   READ CLOCK
*   22 F11   TAPE ERROR(REV. SENSE)
*   12 F12   OUT-XFER
*   21 F13   READY STATUS
*   11 F14   DATA F/F
*   14 F15   INTERRUPT CONDITION
*   13 F16   IN-XFER
*   16 F17   CMD. ENB.(REV. SENSE)
*
*****
*
*           SKP
    
```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

308 *****
309 *
310 *           THE FOLLOWING ARE IMMEDIATE OPERAND/REGISTER BIT
311 *           DEFINITIONS USED WITH OTI/IOC OP-CODES. CHECK
312 *           DESTINATION/SOURCE CODE FIELD (PREVIOUS PAGE)
313 *           & DETERMINE WHAT BIT CONFIGURATION IS USED.
314 *
315 *****
316 *           MIO BUS BITS
317 *
318 * 0 * 1 * 2 * 3 * 4 * 5 * 6 * 7 * 8 * 9 * 10 * 11 * 12 * 13 * 14 * 15 *
319 *****
320 * -7970- (OUTPUT)      (UPH)      *      (LWH)
321 *****
322 *RST * * SET*SET * * SET*SET *RST * *RST * SET* SET* RST* SET* SET* SET*
323 *DATA* * * WRT*WRT * * * REW*OFF *REW * * *FWD * FWD* REV* WRT* WRT*EVEN* ODD*
324 * F/F* * * STB*RST * * *LINE*%0.L * *REV * * * * * *
325 *****
326 * -STATUS- (OUTPUT)    (UPH)      *      (LWH)
327 *****
328 *RST * * * * *SET *SET *SET *SET *EVEN* ODD* SET*TAPE*TIM*TAPE* SET* CLR*
329 *DATA* * * * * *UNIT*UNIT*UNIT*UNIT*BYTE*BYTE* EOF*ERR-* ING*RUN-*REJ *STA *
330 * F/F* * * * *0,2 *0,1 *1,3 *2,3 * CNT* CNT* * OR*FRR *AWAY* ECT* TUS*
331 *****
332 * -XFACE- (OUTPUT)    (UPH)      *      (LWH)
333 *****
334 * RST*SET* SET* RST* SET* RST* CLR* CLK* RST* SET* RST* SET* SUP* ENB* SET* SET*
335 *DATA*UNIT* F0 * F0 * DEV*UNIT* RUS* INT* F2 * F2 * F1 * F1 * PAR* PAR* OUT* IN *
336 * F/F*INT* * * * END* INT*LOGC* F/F* * * * * * BIT* RIT*MODE*MODE*
337 *****
338 * -STATUS/RD DATA- (INPUT) (UPH) *      (LWH)
339 *****
340 * ID * TP*TAPE* INT* SIO*FILE* * * * R * R * R * R * R * R * K * W *
341 * BUR*MRK* FRR*PEND* OK *PROT* * * * * D * D * D * D * D * D * D * D *
342 * -ST * * -OR*-ING* * * * * * 0* 1* 2* 3* 4* 5* 6* 7*
343 *****
344 * -UNIT NO.- (INPUT, HIGH BYTE ONLY)
345 *****
346 *UNIT*UNIT*(UNIT*UNIT* SEL* SEL* SEL* SEL*
347 *--- *---* * *UNIT*UNIT*UNIT*UNIT*
348 *MSB *LSB* MSB* LSB* 0,2* 0,1* 1,3* 2,3*
349 *****
350 SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

351
352
353
354
355
356
357 0000 00 111 110 100 110 001 100 START OTI UPH D11 #163 RST DATA & CMD ENR F/F-SELECT UNIT #0
358 0001 11 001 110 001 110 011 111 XOR CTM R3B R3A REGISTER & THE COUNTER
359 0002 00 111 110 001 000 010 110 OTI UPH D02 #351 RST. F0.PUS-LOGIC & UNIT INT F/F
360 0003 10 111 111 101 100 000 000 PSI UPH ROM #377 RG(0:7):=ALL ONES
361 0004 10 111 110 001 110 110 100 WAIT PSI UPH CTM TSTOP CNTR := STOP DELAY
362 0005 00 111 000 000 001 000 001 OTI LWH D00 #276 DEC RESET FWD. REV. & SET ODD PARITY MODE
363 0006 01 010 001 000 000 000 110 JXZ RCS * DEC TIME OUT THE COUNTER
364 0007 00 111 100 011 010 100 101 CONT OTI LWH D06 #132 RST. F1.F2:ENABLE PARITY & IN-MODE
365 0010 00 111 110 000 010 000 001 OTI UPH D00 #176 RST DATA F/F, REWIND & OFF-LINE
366 0011 00 111 110 001 000 010 100 OTI UPH D02 #353 RESET F0 & UNIT INT. F/F
367 0012 00 000 111 001 011 001 100 JMP PTCH1 GOTO PTCH1 TO LOOK FOR END INTERRUPT
368 0013 10 111 101 011 111 001 100 CONT1 PSI LWH R1M #63 0011001100110011
369 0014 10 111 110 011 101 110 111 PSI UPH R5M #210 R5:=(SELECT THIS UNIT NOW)
370 0015 10 111 100 011 101 110 111 PSI LWH R5M #210 1000100010001000
371 0016 00 010 111 000 010 011 010 IOC INP R4I D20 GET PRESENT UNIT NO. IN R4
372
373
374
375
376
377
378
379
380 0017 11 100 111 100 011 000 011 MAIN JFS F16 REJECT REJECT IF IN-XFER
381 0020 11 100 110 100 011 000 011 JFS F12 REJECT OR OUT-XFER = 1
382 0021 11 100 111 110 000 110 010 JFS F17 SCAN GOTO SCAN IF NO CONTROL ORDER
383
384
385
386
387
388 0022 11 111 110 101 101 111 011 BEGIN PSA R4M R4A RL4 ROTATE R4 LEFT BY 4
389 0023 11 111 110 101 101 111 011 PSA R4M R4A RL4 ADJUST PROPER CODE FOR
390 0024 11 111 110 101 101 111 011 PSA R4M R4A RL4 LAST UNIT SELECTED AND
391 0025 00 010 110 000 110 000 010 IOC OUT UPH R4I D01 OUTPUT TO SELECT IT
392 0026 00 111 100 100 110 000 001 BEG2 OTI LWH D11 #176 RST. STATUS, CMD. ENR. & BYTE CNT.
393 0027 00 010 111 100 110 011 011 IOC INP R3I D31 GET COMMAND WORD IN R3
394 0030 11 010 101 101 110 001 111 PSR LWH ROM R3B PASS LOW HALF OF R3 IN R0
395 0031 00 011 101 000 000 011 101 JMZ RCS DECOD GOTO DECOD IF NOT A SELECT COMMAND
396 0032 00 010 111 000 010 001 100 IOC INP UPH R2I D20 SELECT THE PROPER
397 0033 00 010 111 000 110 000 100 IOC OUT UPH R2I D21 UNIT & SET SERV. REQ.
398 0034 00 000 111 000 000 000 111 JMP CONT GOTO CONT
399
400 SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

401
402
403
404
405
406 0035 11 100 110 110 000 011 111
407 0036 00 000 111 000 011 000 011
408 0037 10 110 101 111 100 001 111
409 0040 00 011 101 000 011 000 011
410 0041 10 110 101 001 111 111 001
411 0042 10 001 101 110 011 111 001
412 0043 00 011 111 000 010 111 100
413 0044 10 001 101 110 011 111 011
414 0045 00 011 111 000 011 001 101
415 0046 10 110 101 111 111 110 111
416 0047 00 011 111 000 011 000 011
417 0050 10 001 101 110 011 111 101
418 0051 00 011 111 000 010 100 001
419 0052 11 100 101 010 000 101 100
420 0053 00 000 111 000 000 101 101
421 0054 01 110 111 000 001 000 100
422 0055 00 111 111 000 000 000 100
423 0056 10 110 101 111 111 111 110
424 0057 00 011 111 000 000 000 111
425 0060 00 111 110 000 000 000 010
426 0061 00 000 111 000 000 000 111
427
428
429
430
431
432
433
434
435 0062 00 010 111 001 010 001 011
436 0063 00 000 111 001 011 010 111
437 0064 00 011 101 000 000 001 111
438 0065 00 010 110 000 110 000 101
439 0066 10 111 100 001 111 101 111
440 0067 11 010 111 010 100 111 111
441 0070 11 111 110 011 100 110 111
442 0071 01 010 001 000 000 111 001
443 0072 11 100 110 110 000 111 111
444 0073 11 110 111 111 010 000 111
445 0074 00 011 111 000 000 001 111
446 0075 11 001 111 101 010 000 111
447 0076 00 000 111 000 000 001 111
448 0077 11 110 111 111 010 000 111
449 0100 00 011 101 000 000 001 111
450 0101 11 001 111 101 010 000 111
451 0102 00 111 110 001 001 000 000
452 0103 00 000 111 000 011 000 111
453
454

```

*
* THE GIVEN COMMAND IS DECODED HERE TO LOOK FOR WHICH SUBGROUP IT BELONGS TO. *
*

```

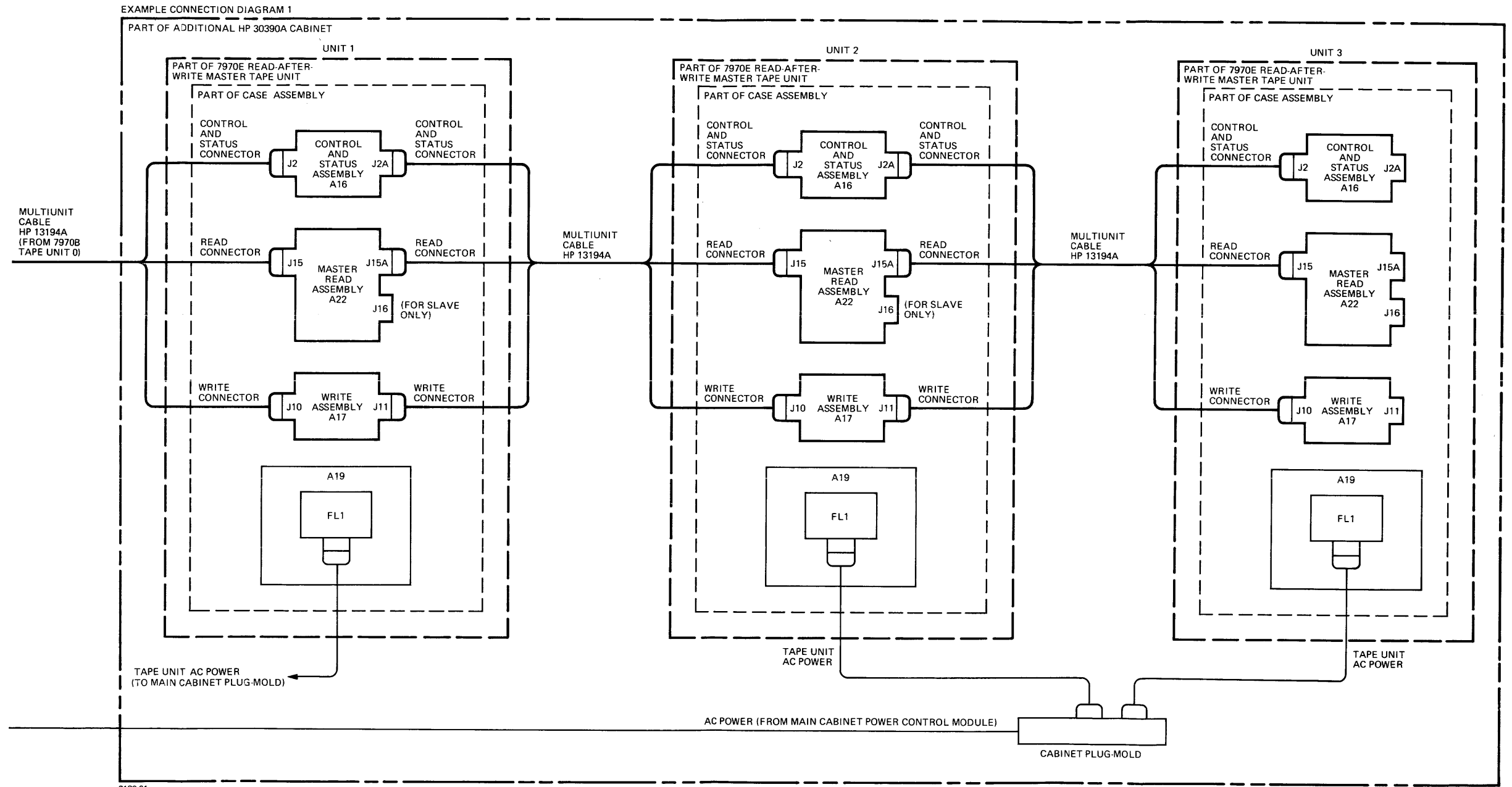
DECOD JFS F13 **2 REJECT THE COMMAND IF
      JMP REJECT TAPE UNIT IS NOT READY
      ANI LWH R3B #360 LOOK FOR ILLEGAL BITS IN R3
      JMZ RCS REJECT REJECT THE COMMAND IF ILLEGAL BITS IN R3
      ANI LWH R2M R3B RDR MASK OFF SUB-GROUP CMD. CODE IN R2
      XOI LWH R2B RDR GOTO RDFWD IF READ
      JMZ RDFWD FORWARD COMMAND
      XOI LWH R2B WRR GOTO WRDWD IF
      JMZ WRDWD WRITE COMMAND
      ANI LWH R3B #10 GOTO REJECT IF COMMAND IS
      JMZ RFJECT ANY OF THREE REMAINING ILLEGAL CODES
      XOI LWH R2B RDREV GOTO RDBKD IF READ
      JMZ RDBKD REVERSE TYPE COMMAND
      JFS F05 **2 SKIP NEXT IF WRT. STATUS=1
      JMP **2 SKIP NEXT INSTRUCTION
      CAL GDFWD SUB. CALL TO AVOID NOISE IN GAP
      OTI UPH D20 #373 SET REWIND & SERV. RFO
      ANI LWH R3B #1 LOOK FOR REW OR RST
      JMZ CONT GOTO CONT IF 'REW' COMMAND
      OTI UPH D00 #375 SET OFF-LINE F/F & GOTO
      JMP CONT CONT IF 'RST' COMMAND
*****
*
* 'SCAN' CONTINUOUSLY SELECTS A UNIT & LOOKS FOR ITS READY STATUS. THIS IS
* DONE ONLY IF CONTROLLER IS IN IDLE STATE(NO SIO GOING ON). UNIT INT-
* -ERRUPT F/F IS SET WHEN A UNIT, PREVIOUSLY 'NOT-READY' RECOMES
* READY. AN INTERRUPT IS GENERATED TO TELL THE CPU ABOUT IT.
*
*****
SCAN IOC INP R3I D22 UPH GET STATUS BYTE IN R3
      JMP PTCH2 GOTO PATCH THE PROGRAM
      JMZ RCS MAIN GOTO MAIN IF ALREADY IN SIO ROUTINE
SCAN0 IOC OUT UPH R1I D01 SELECT UNIT FROM R1
      PSI LWH CTM #20 PRESET CNTR TO 16 CYCLE DELAY
      PSB R1M R1B RL1 R1 & R5 ARE ROTATED
      PSA R5M R5A RL1 LEFT BY ONE BIT
      JXZ RCS DEC * TIME OUT THE COUNTER
      JFS F13 READY GOTO READY IF F13=1
      AND UPH ROB R5A WAS THIS UNIT READY BEFORE ?
      JMZ MAIN NOT RDY BEFORE; NOT RDY NOW-GOTO MAIN
      XOR UPH ROM ROB R5A RDY BEFORE; NOT RDY NOW-MODIFY R0
      JMP MAIN GOTO MAIN
READY AND UPH ROB R5A WAS THIS UNIT READY BEFORE ?
      JMZ RCS MAIN RDY BEFORE; RDY NOW-GOTO MAIN
      XOR UPH ROM ROB R5A NOT RDY BEFORE; RDY NOW-INT. CASE
      OTI UPH D02 #277 SET UNIT INTERRUPT F/F
      JMP INT2 GOTO INT?
*****
SKP

```

OPTION CONFIGURATION TABLE (SEE NOTES 1 AND 2)

UNIT 0	UNIT 1	UNIT 2	UNIT 3
B	B	B	B
E	E	E	E
B	E	E	E
E	S ³	S ³	S ³
B	B	E	E
E	E	S ³	S ³
B	E	S ³	S ³
B	B	B	E
B	B	E	S ³
E	E	E	S ³
B	E	E	S ³

- NOTES:
1. SUPERScript 3 IN THE TABLE SIGNIFIES NOTE 3 BELOW.
 2. LETTERS IN THE TABLE REPRESENT TAPE UNITS AS FOLLOWS: "B" MEANS 7970B, "E" MEANS MASTER 7970E, "S" MEANS SLAVE 7970E. UNIT 0 CAN BE A "B" OR "E" AS SHOWN IN SMALL OUTLINED BOX. ALL POSSIBLE COMBINATIONS USING TWO TAPE UNITS ARE SHOWN BY LETTER COMBINATIONS IN THE SECOND LARGEST OUTLINED BOX, ETC. ALL COMBINATIONS USING FOUR (MAXIMUM) UNITS IS SHOWN USING ENTIRE TABLE.
 3. MULTIUNIT CABLE HP 13194A-001 MUST BE USED AND FROM 7970E MASTER TO SLAVE TAPE UNIT AND FROM SLAVE TO SLAVE. SEE EXAMPLE CONNECTION DIAGRAM NUMBER 2.



2180-21

Figure 4-2. Magnetic Tape Subsystem, Example Multiple Tape Unit Cabling Diagram (Sheet 1 of 2)

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

4-70 Changed 31 JAN 1973

```

455 *****
456 *
457 * THIS SUBROUTINE MAKES THE TAPE GO FORWARD & ERASE SOME PART OF THE TAPE
458 * BEFORE EXECUTING A BACKSPACE OR REWIND TYPE COMMAND WHEN THE CURRENT
459 * IN WRITE HEADS WAS ON. THIS ENSURES THAT NOISE CHARACTER IS NOT
460 * WRITTEN IN THE GAP WHEN WRITE CURRENT IN HEADS IS SWITCHED.
461 *
462 *****
463 0104 10 111 110 001 110 010 101 GOFWD PSI UPH CTM TS155 CNTR:=-.155 INCH + START DELAY
464 0105 00 111 100 000 000 100 000 OTI LWH D00 #337 SET FWD F/F
465 0106 01 010 001 000 001 000 110 JXZ RCS DEC * TIME OUT THE COUNTER
466 0107 10 111 110 001 110 110 100 PSI UPH CTM TSTOP CNTR:=STOP DELAY
467 0110 00 111 000 000 001 001 000 OTI LWH D00 DEC #267 RST. FWD.-REV. F/F & WRITE F/F
468 0111 01 010 001 000 001 001 001 JXZ RCS DEC * TIME OUT THE COUNTER
469 0112 01 101 111 111 111 111 111 RTN SUBROUTINE RETURN
470 *****
471 *
472 * SUBROUTINE BLANK ATTEMPTS TO GET A READ CLOCK OR END-OF-BLOCK
473 * (IN 1600 BPI) WITHIN 25 FEET OF TAPE WHEN CONTROLLER HAS
474 * INITIATED A READ OPERATION. F0 IS SET IF RD. CLK. IS
475 * FOUND. IF RD. CLK. OR EOP IS NOT FOUND, TAPE-
476 * RUNAWAY F/F IS SET INDICATING AN ATTEMPT
477 * IS MADE TO READ BLANK TAPE.
478 *
479 *****
480 0113 10 111 111 011 111 101 111 BLANK PSI UPH RIM #20 R1:=-240 (IN UPPER HALF)
481 0114 10 111 110 001 100 000 101 TIMER PSI UPH CTM TGAP CNTR:=TIMER FOR 1.25" OF TAPE
482 0115 11 100 010 000 001 010 110 JFS F10 DEC NBLK GOTO NBLK IF RD. CLK.=1
483 0116 11 100 001 000 001 010 000 JFS F04 DEC **2 NO SKIP IF 800 BPI
484 0117 00 000 011 000 001 010 001 JMP **2 DEC SKIP NEXT INSTRUCTION
485 0120 11 100 001 110 001 010 111 JFS F07 DEC NB16 GOTO NB16 IF EOB=1
486 0121 01 010 001 000 001 001 101 JXZ RCS DEC **4 WAIT FOR CNTR TO TIME OUT
487 0122 00 001 111 010 111 111 110 ADI UPH RIM R1B 1 R1:=R1+1
488 0123 00 011 101 000 001 001 100 JMZ RCS TIMER STAY IN LOOP TILL TIMER NON-ZERO
489 0124 00 111 100 000 100 000 100 OTI LWH D01 #373 SET TAPE RUNAWAY BIT
490 0125 00 000 111 000 011 000 100 JMP INTER GOTO INTER
491 0126 00 111 110 011 000 100 000 NBLK OTI UPH D06 #337 SET F0 TO INDICATE I RD. CLK.
492 0127 11 001 110 001 110 011 111 NB16 XOR CTM R3B R3A ZERO OUT THE COUNTER
493 0130 11 001 111 001 110 011 111 XOR R2M R3B R3A ZERO OUT R2 (CRC REGISTER)
494 0131 01 101 111 111 111 111 111 RTN SUBROUTINE RETURN
495 *****
496 *
497 * SUBROUTINE WGAP ERASES 3.75 INCHES OF TAPE AND
498 * THEN CHECKS FOR ANY NOISE LEFT IN THE GAP
499 *
500 *****
501 0132 10 111 110 001 100 000 101 WGAP PSI UPH CTM TGAP PRESET CNTR. WITH 1.25 IN. TIMER
502 0133 01 000 111 111 111 111 111 NOP TIME OUT THREE
503 0134 01 000 111 111 111 111 111 NOP TIMES THE VALUE
504 0135 01 010 001 000 001 011 011 JXZ RCS DEC **2 OF THE COUNTER
505 0136 11 100 110 000 001 100 000 JFS F10 **2 SKIP NEXT IF RD CLK = 1
506 0137 00 000 111 000 001 100 001 JMP **2 DONE-RETURN
507 0140 00 111 100 010 100 010 000 OTI LWH D05 #357 SET TAPE-ERROR & RST RD CLK-NOISE IN GAP
508 0141 01 101 111 111 111 111 111 RTN RETURN
509 *****
510 SKP

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Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

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518 0142 11 100 011 000 001 100 100 WRCHK JFS F14 DEC **2 SKIP NEXT IF DATA F/F=1
519 0143 00 111 000 000 100 001 000 OTI LWH DEC D01 #367 SET TIMING ERROR IF DATA F/F = 0
520 0144 00 111 010 001 010 100 000 OTI UPH DEC D02 #137 RST DATA F/F & SET F0
521 0145 00 010 011 100 110 011 001 IOC INP DEC D31 R5I GET DATA OUT WORD IN R5
522 0146 11 100 010 100 001 101 001 JFS F12 DEC **3 SKIP 2 IF OUT-XFER=1
523 0147 00 111 010 001 000 010 000 OTI UPH DEC D02 #357 RST F0 INDICATING OUT-XFER = 0
524 0150 01 101 011 111 111 111 111 RTN DEC SUBROUTINE RETURN
525 0151 00 111 001 000 000 000 000 OTI LWH DEC D20 #377 SET SERV. REQ. TO GET NEXT WORD
526 0152 01 101 011 111 111 111 111 RTN DEC SUBROUTINE RETURN
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532 0153 11 100 100 010 001 110 001 FSR0 JFS F01 FMCHK GOTO FMCHK IF F1=1 (POSSIBLE FILE-MARK
533 0154 00 111 110 011 000 010 000 AGAIN OTI UPH D06 #357 RESFT F0 & RD. CLK.
534 0155 10 111 110 001 111 111 101 PSI UPH CTM T8 CNTR:=8 CHAR. DELAY
535 0156 11 100 010 000 001 111 111 JFS F10 DEC DROP ERROR CASE IF RD. CLK. COMFS
536 0157 01 010 001 000 001 101 110 JXZ RCS DEC *-1 IN BEFORE COUNTER GOES TO 0
537 0160 00 000 111 000 011 110 101 JMP FRDF GOTO FRDF TO CONTINUE NEXT RECORD
538 0161 10 111 110 001 111 111 110 FMCHK PSI UPH CTM T4 CNTR:=4 CHAR. DELAY
539 0162 11 100 010 000 001 111 111 JFS F10 DEC DROP ERROR CASE IF ANY RD. CLK. COMFS
540 0163 01 010 001 000 001 110 010 JXZ RCS DEC *-1 IN BEFORE COUNTER GOES TO ZERO
541 0164 10 111 110 001 111 111 110 PSI UPH CTM T4 CNTR:=T4.0
542 0165 11 100 010 000 001 111 000 JFS F10 DEC **3 LOOK FOR A RD. CLK.
543 0166 01 010 001 000 001 110 101 JXZ RCS DEC *-1 BEFORE COUNTER=0
544 0167 00 000 111 000 011 110 101 JMP FRDF NOISE: GOTO FRDF TO READ NEXT RECORD
545 0170 01 110 111 000 111 111 000 CAL FMPAR SUB. CALL TO LOOK FOR FILE-MARK
546 0171 10 111 100 001 100 000 000 PSI LWH CTM #377 CNTR:=4 CHAR. DELAY
547 0172 00 111 100 010 000 000 000 OTI LWH D04 #377 RESFT RD. CLK. F/F
548 0173 01 010 001 000 001 111 011 JXZ RCS DEC * TIME OUT THE COUNTER
549 0174 11 100 110 000 001 111 111 JFS F10 DROP GOTO DROP IF RD. CLK.=1
550 0175 00 111 100 000 110 100 000 FM816 OTI LWH D01 #137 SET EOF STATUS
551 0176 11 100 100 010 010 000 010 JFS F01 ODEND TERMINATE IF F1=1 (FILE-MARK CONFIRMED)
552 0177 00 111 100 000 100 010 000 DROP OTI LWH D01 #357 SET TAPE ERROR STATUS
553 0200 00 000 111 000 010 000 010 JMP ODEND GOTO ODEND
554 0201 00 111 100 000 110 100 000 FILE OTI LWH D01 #137 SET EOF STATUS
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560 0202 00 111 100 011 010 100 000 ODEND OTI LWH D06 #137 RST. F1,F2 & RD. CLK.
561 0203 00 111 110 101 010 010 000 OTI UPH D12 #157 RESET F0, DATA F/F & EOF FLAG
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Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

4-72 Changed 31 JAN 1973

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564
565
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568
*****
*
*           STOP ROUTINE IS THE EXIT POINT FOR ALL COMMANDS
*
*****
569 0204 11 100 111 010 011 000 100 STOP JFS F15 INTER          GOTO INTFR IF INTERRUPT FLAG=1
570 0205 11 001 110 001 110 011 111 XOR CTM R3B R3A          ZERO OUT THE COUNTER
571 0206 00 000 111 001 011 110 001 JMP PATCH              GOTO PATCH TO LOOK FOR END INTERRUPT
572 0207 11 100 111 100 010 001 001 JFS F16 **2           SKIP NEXT IF IN-XFER=1
573 0210 00 000 111 000 010 001 011 JMP **3              SKIP 2 INSTRUCTIONS
574 0211 00 111 110 001 000 001 000 OTI UPH D02 #367      SET DEVICE-END
575 0212 00 000 111 000 010 001 100 JMP **2              & SKIP NEXT INSTR.
576 0213 00 111 111 000 000 000 000 OTI UPH D20 #377      SET SERV. REQ.
577 0214 01 010 001 000 010 001 100 JXZ RCS * DEC        TIME OUT THE CNTR.
578 0215 11 100 111 110 000 000 100 STOP1 JFS F17 WAIT     GOTO WAIT IF NO CONTROL ORDER
579 0216 00 010 111 100 110 011 011 IOC INP R31 D31        GET COMMAND WORD IN R3
580 0217 10 110 100 001 111 110 000 ANI LWH CTM R3B #17   MASK OFF COMMAND CODFS IN CNTR
581 0220 11 001 101 001 010 000 011 XOR LWH R2M R0B CTA    R2 := R0 'XOR' R3
582 0221 11 111 101 101 110 001 111 PSA LWH R0M R3A      R0(LOWER):=R3(NEW COMMAND)
583 0222 10 110 101 110 011 111 001 ANI LWH R2B #6       GO TO WAIT IF NEW CMD. IS
584 0223 00 011 101 000 000 000 100 JMZ RCS WAIT         OF DIFFERENT SUB-GROUP
585 0224 00 000 111 000 000 010 110 JMP RFG2             GOTO BEG2
586
*****
587
588
589
590
*****
591 0225 10 111 110 001 111 111 101 FSRF PSI UPH CTM T8    CNTR:=T8.0
592 0226 00 111 010 011 000 010 000 OTI UPH DEC D06 #357   RESFT F0 & RD. CLK.
593 0227 00 111 000 100 110 000 000 OTI LWH DEC D11 #177  RST. EOB & SET EVEN PYTE CNT.
594 0230 01 010 001 000 010 011 000 JXZ RCS DEC *        TIME OUT THE COUNTER
595 0231 10 001 101 111 011 110 000 XOI LWH R0B FSF       GOTO AGAIN IF CMD.
596 0232 00 011 111 000 001 101 100 JMZ AGAIN           IS FSF - ELSE
597 0233 00 000 111 000 010 000 010 JMP ODEND          GOTO ODEND
598
*****
599
600
601
602
603
*****
604 0234 11 100 100 010 010 000 001 RBDEC JFS F01 FILE     GOTO FILE IF F1=1
605 0235 10 001 101 111 011 110 101 XOI LWH R0B BSR       GOTO ODEND
606 0236 00 011 111 000 010 000 010 JMZ ODEND          IF CMD IS BSR
607 0237 00 111 110 001 000 010 000 OTI UPH D02 #357      RESET F0
608 0240 00 000 111 000 010 101 010 JMP BSRF            GOTO BSRF TO CONTINUE BSF COMMAND
609
*****
610 SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

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611
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618
619 0241 11 100 100 110 010 110 000 RDBKD JFS F03 BSRF2 GOTO BSRF2 IF TAPE AT LOAD POINT
620 0242 11 100 101 010 010 100 101 JFS F05 **3 SKIP 2 IF WRITE STATUS=1
621 0243 10 111 110 001 110 110 100 PSI UPH CTM TSTRT PRESET COUNTER WITH TAPE
622 0244 00 000 111 000 010 101 000 JMP MERGE START DELAY & GOTO MERGE
623 0245 01 110 111 000 001 000 100 CAL GOFWD SUB. CALL TO AVOID NOISE IN GAP
624 0246 00 111 110 001 000 100 000 OTI UPH D02 #337 SET F0 TO REMEMBER WRT. STATUS WAS 1
625 0247 10 111 110 001 110 010 101 PSI UPH CTM TS155 CNTR:=.155" + START DELAY
626 0250 00 111 000 110 000 010 000 MERGE OTI LWH DEC D14 #357 SET REV.,RST. RD. CLK. &EOB F/F
627 0251 01 010 001 000 010 101 000 JXZ RCS DEC *-1 TIME OUT THE COUNTER
628
629
630
631
632
633
634 0252 11 100 100 110 010 110 000 BSRF JFS F03 BSRF2 GOTO BSRF2 IF BOT=1
635 0253 11 100 110 000 010 110 010 JFS F10 BACK GOTO BACK IF RD. CLK.=1
636 0254 11 100 101 000 010 101 110 JFS F04 **2 SKIP NEXT IF 1600 BPI
637 0255 00 000 111 000 010 101 010 JMP BSRF GO BACK TO BSRF
638 0256 11 100 101 111 000 000 110 JFS F07 FM16 GOTO FM16 IF EOB FLAG=1
639 0257 00 000 111 000 010 101 010 JMP BSRF GO BACK IN LOOP
640 0260 00 111 101 000 000 000 000 BSRF2 OTI LWH D20 #377 SET SERV.REQ. & GOTO
641 0261 00 000 111 000 000 000 100 JMP WAIT WAIT FOR NEW COMMAND
642
643
644
645
646
647 0262 11 100 101 001 000 010 100 BACK JFS F04 BCKRD GOTO BCKRD IF 1600 BPI
648 0263 01 110 111 000 111 111 000 CAL FMPAR SUB. CALL TO LOOK FOR FM CHARACTER
649 0264 10 111 100 001 101 110 010 PSI LWH CTM T22 PRESET THE CNTR
650 0265 10 111 110 001 111 111 110 PSI UPH CTM T4 WITH T6.2 DELAY
651 0266 11 100 010 000 101 001 011 JFS F10 DEC NOFM GOTO NOFM IF RD. CLK.
652 0267 01 010 001 000 010 110 110 JXZ RCS DEC *-1 CAME BEFORE CNTR = 0
653 0270 10 111 110 001 111 111 110 PSI UPH CTM T4 PRESET CNTR WITH T4
654 0271 11 100 010 000 101 000 111 JFS F10 DEC BCK1 GOTO BCK1 IF RD. CLK.
655 0272 01 010 001 000 010 111 001 JXZ RCS DEC *-1 CAME BEFORE CNTR = 0
656 0273 00 000 111 000 010 101 010 JMP BSRF NOISE CHARACTER-GOTO BSRF
657
658
        SKP
    
```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

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659
660
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663
664 0274 10 111 110 001 110 110 100 RDFWD PSI UPH CTM TSTRT CNTR:=START DELAY
665 0275 10 110 101 111 011 111 110 ANI LWH ROB 1 LOOK FOR SUBGROUP OF READ
666 0276 00 011 101 000 011 101 101 JMZ RCS FSRF0 FSR-FSF GROUP-GOTO FSR50
667 0277 00 111 101 001 010 100 001 RDR1 OTI LWH D22 #136 RST, F1,F2 & SET SERV. REQ.& IN MODE
668 0300 11 100 111 100 011 101 110 JFS F16 RDGO GOTO PDGO IF IN-XFER=1
669 0301 11 100 110 100 011 000 011 JFS F12 REJECT REJECT IF OUT-XFER OR
670 0302 11 100 111 110 011 000 000 JFS F17 *-2 CMD=1-OTHERWISE STAY IN LOOP
671
672
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676 0303 00 111 100 000 100 000 010 REJECT OTI LWH D01 #375 SET REJECT BIT OF STATUS
677
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688 0304 10 111 110 001 110 110 100 INTER PSI UPH CTM TSTOP PRESET CNTR. WITH TAPE STOP DELAY
689 0305 00 111 000 100 001 000 000 OTI LWH D10 #277 DEC RESET FWD,REV. & CMD. ENR.
690 0306 01 010 001 000 011 000 110 JXZ RCS * DEC TIME OUT THE CNTR.
691 0307 00 111 110 001 000 000 011 INT2 OTI UPH D02 #374 CLOCK INTERRUPT & CLR. BUS LOGIC
692 0310 00 010 111 001 010 001 011 IOC IMP R3I D22 UPH GET STATUS BYTE IN UPPER R3
693 0311 10 110 111 111 111 101 111 ANI UPH R3B #20 IS INT. FLAG=1?
694 0312 00 011 101 000 011 001 000 JMZ RCS *-2 YES, KEEP LOOKING AT THIS BIT
695 0313 00 111 110 001 000 000 100 OTI UPH D02 #373 RESET UNIT INT. F/F
696 0314 00 000 111 000 000 000 100 JMP WAIT NO, GO TO WAIT
697
698
    SKP
    
```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

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704 0315 00 010 111 001 010 001 011
705 0316 10 110 111 111 111 111 011
706 0317 00 011 101 000 011 000 011
707 0320 00 111 100 011 010 100 010
708 0321 11 100 100 110 011 010 011
709 0322 00 111 100 001 000 010 000
710 0323 10 110 101 111 011 111 110
711 0324 00 011 101 000 011 011 111
712 0325 00 111 111 001 000 010 000
713 0326 11 100 101 000 011 011 010
714 0327 10 001 101 111 011 111 011
715 0330 00 011 111 000 011 011 010
716 0331 00 111 100 001 000 001 000
717 0332 11 100 110 100 011 011 110
718 0333 11 100 111 100 011 000 011
719 0334 11 100 111 110 011 011 010
720 0335 00 000 111 000 011 000 011
721 0336 00 111 101 000 000 000 000
722 0337 10 111 110 001 110 100 100
723 0340 00 111 000 010 000 100 100
724 0341 01 010 001 000 011 100 000
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732 0342 11 100 101 001 001 100 101
733 0343 11 100 100 010 011 100 101
734 0344 01 110 111 000 001 011 010
735 0345 00 111 100 011 000 100 000
736 0346 10 110 101 111 011 111 110
737 0347 00 011 101 000 111 000 110
738 0350 11 001 111 011 110 011 111
739 0351 11 001 111 001 110 011 111
740 0352 11 010 110 101 010 001 111
741 0353 10 111 100 001 111 000 010
742 0354 00 000 011 000 101 011 011
743
744
*****
*
*   ENTRY FOR WRITE COMMAND - ANY ONE OF WRR, WRZ, WFM OR GAP
*
*****
WRFWD IOC INP R3I D22 UPH      GET 7970 STATUS IN R3
      ANI UPH R3B #4           REJECT THE COMMAND IF
      JMZ RCS REJECT          TAPE REEL IS PROTECTED
      OTI LWH D06 #135        RESET F1,F2,RD. CLK. & SFT OUT MODE
      JFS F03 **2            SKIP NEXT IF TAPE AT LOAD POINT
      OTI LWH D02 #357        SET F1 (ROT = 0)
      ANI LWH R0B 1           GOTO WJOIN IF
      JMZ RCS WJOIN          CMD IS WFM-GAP
      OTI UPH D22 #357        SET SERV. REQ. & RST. F0
      JFS F04 **4            SKIP 3 IF 1600 BPI
      XOI LWH R0B WRR         LOOK FOR WRZ COMMAND
      JMZ **2                SKIP NEXT IF WRR COMMAND
      OTI LWH D02 #367        WRZ CMD: DISABLE PARITY TRACK
      JFS F12 **4            SKIP 3 IF OUT-XFER=1
      JFS F16 REJECT          REJECT THE COMMAND IF
      JFS F17 *-2            CONTROL ORDER OR IN-XFER
      JMP REJECT              COMES BEFORE OUT-XFER
      OTI LWH D20 #377        SET SERV. REQ.
WJOIN PSI UPH CTM TWSTR        PRESET COUNTER WITH START DELAY
      OTI LWH DEC D04 #333    SET FWD., WRITE & RST. PD. CLK.
      JXZ RCS DEC *-1        TIME OUT THE COUNTER
*****
*
*   AT THIS POINT TAPE IS UP TO SPEED & READY TO DO WRITE OPERATIONS.
*
*   IF F0=1 THEN TAPE STARTED AT ROT. WRITE A 3.75" GAP FIRST.
*
*   IF F2=1 THEN COMMAND IS WFM OR GAP, OTHERWISE WRR OR WRZ.
*
*****
WRRFC JFS F04 WR16            GOTO WR16 IF 1600 BPI
      JFS F01 **2            WRITE A GAP IF
      CAL WGAP              TAPE WAS AT BOT
      OTI LWH D06 #337        RESET RD CLK & F1
      ANI LWH R0B 1           GOTO GPFM IF
      JMZ RCS GPFM          CMD IS WFM-GAP
      XOR R1M R3B R3A        ZERO OUT R1(WRITE CRC CHARACTER)
      XOR R2M R3B R3A        ZERO OUT R2(READ CRC CHARACTER)
      PSB UPH R4M R0B        STORE HISTORY OF UNITS IN R4
      PSI LWH CTM T1         CNTR:=1 CHAR. DELAY
      JMP DEC WLOOP          GOTO WLOOP
*****
SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

4-76 Changed 20 SEP 1975

```

745
746
747
748 0355 00 111 100 001 001 000 001 FSKFO UTI LWH D02 #276 SET F2 & IN-MODE
749 0356 00 111 100 110 000 101 000 RUGO UTI LWH D14 #327 RST. EUB,RD. CLK. & SET FWD
750 0357 01 010 001 000 011 101 111 JAZ RCS * DEC TIME OUT THE COUNTER
751 0360 11 100 100 110 011 110 010 JFS F03 **2 SKIP NEXT IF BOT STATUS=1
752 0361 00 000 111 000 011 110 101 JMP **4 SKIP 3 INSTRUCTIONS
753 0362 10 111 110 001 100 000 101 PSI UPH CTM TGAP CNTR:=1.25" DELAY
754 0363 11 100 100 110 011 110 011 JFS F03 * STAY HERE UNTIL BOT STATUS=0
755 0364 00 000 111 000 011 101 110 JMP RUGO BOT IS NO MORE - GOTO RUGO AGAIN
756 0365 00 111 100 011 000 100 000 FROF UTI LWH D06 #337 RST. RD. CLK. & F1
757 0366 01 110 111 000 001 001 011 CAL BLANK SUBROUTINE CALL TO BLANK
758 0367 11 100 101 001 000 011 111 JFS F04 FS16 GOTO FS16 IF 1600 BPT
759 0370 01 110 111 000 111 111 000 CAL FMPAK SUB. CALL TO SET F1 IF FM BYTE
760 0371 10 111 100 001 101 110 010 PSI LWH CTM T22 CNTR:=2.2 CHAR. DELAY
761 0372 11 100 000 100 100 000 001 JFS F02 DFC LOOP1 GOTO LOOP1 IF F2 = 1
762 0373 10 111 100 001 101 110 010 LOOPR PSI LWH CTM T22 PRESET COUNTER WITH T2.2
763 0374 00 111 000 010 101 000 000 UTI LWH DEC D05 #277 SET ODD BYTE COUNT & RST. RD. CLK.
764 0375 01 110 011 000 111 010 001 CAL DEC RBYTE SUB. CALL TO PROCESS 1 BYTE
765 0376 11 111 010 101 101 111 111 PSA R4M DEC R3A RL4 MOVE THE LOWER BYTE
766 0377 11 111 010 101 101 111 011 PSA R4M DEC R4A RL4 IN R3 INTO UPPER R4
767 0400 11 001 000 101 110 001 111 XOR LWH DEC R4M R3B R3A ZERO OUT LOW HALF OF R4
768 0401 11 100 010 000 100 000 100 LOOP1 JFS F10 DEC **3 GOTO ODDOR IF
769 0402 01 010 001 000 100 000 001 JAZ RCS DEC *-1 CNTR = 0 BEFORE
770 0403 00 000 111 000 100 011 101 JMP ODDOR A READ CLOCK COMES
771 0404 00 111 100 010 110 000 000 UTI LWH D05 #177 RST. RD. CLK. & SET EVEN BYTE CNT.
772 0405 00 111 100 001 000 100 000 UTI LWH D02 #337 RESET F1
773 0406 10 111 100 001 101 110 010 PSI CTM LWH T22 PRESET COUNTER WITH T2.2
774 0407 11 100 000 100 100 001 001 JFS **2 DEC F02 SKIP NEXT IF F2=1
775 0410 00 000 011 000 100 001 100 JMP **4 DEC SKIP NEXT 3 INSTRUCTIONS
776 0411 00 111 010 001 000 010 000 UTI UPH DEC D02 #357 RESET F0
777 0412 10 110 001 111 011 111 110 ANI LWH DEC R0B 1 GOTO LOOP1 IF
778 0413 00 011 001 000 100 000 001 JMZ RCS DEC LOOP1 CMU IS FSR=FSF
779 0414 01 110 011 000 111 010 001 CAL DEC RBYTE PROCESS THE BYTE
780 0415 11 100 000 100 100 011 010 JFS F02 DEC NEXT1 GOTO NEXT1 IF F2=1
781 0416 00 010 010 011 110 000 010 IOC OUT DFC UPH R4I D07 OUTPUT THE I-BYTE TO DATA-IN REG.
782 0417 00 010 000 011 110 000 011 IOC OUT DFC LWH R3I D07 OUTPUT THE BYTE IN DATA-IN REG.
783 0420 11 100 000 000 100 010 010 JFS **2 DEC F00 SKIP NEXT IF F0=1
784 0421 00 000 011 000 100 010 100 JMP **3 DEC SKIP 2 INSTRUCTIONS
785 0422 00 111 010 001 000 010 000 UTI UPH DEC D02 #357 RESET F0 (1 WORD)
786 0423 00 000 011 000 100 011 001 JMP NEXT UFC GOTO NEXT
787 0424 11 100 011 000 100 010 110 JFS **2 DEC F14 SKIP NEXT IF DATA F/F=1
788 0425 00 111 000 000 100 001 000 UTI LWH DEC D01 #367 SET TIMING ERROR STATUS
789 0426 11 100 011 100 100 011 001 JFS F16 DEC NEXT GOTO NEXT IF IN-XFER=1
790 0427 00 111 000 001 001 000 000 UTI LWH DEC D02 #277 SET F2 TO INDICATE WC<REC. LFNGTH
791 0430 00 000 011 000 100 011 010 JMP DEC NEXT1 GOTO NEXT1
792 0431 00 111 011 001 010 000 000 NEXT UTI UPH DEC D22 #177 RST. DATA F/F & SET SERV. REG.
793 0432 11 100 010 000 011 111 011 NEXT1 JFS F10 DEC LOOPR STAY IN LOOP TILL
794 0433 01 010 001 000 100 011 010 JAZ RCS DEC *-1 ALL RD CLKS ARE DUNE
795 0434 00 000 111 000 100 101 001 JMP EVENOR GOTO EVENOR
796
797
798
799
800
801
802
*****
* FU=1 IF EXACTLY ONE CHARACTER READ FROM TAPE *
* F1=1 IF THE CHARACTER READ LOOKS PART OF FILE-MARK(OCTAL 23) *
* F2=1 IF THE COMMAND IS FSR OR FSF - OR IN HDR, RUC *
* COMMAND, THE WORD COUNT < RECORD LENGTH *
*****
SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

803
804
805
806
807
808
809
810
811
812
813 0435 11 100 100 000 001 101 011 ODDEOR JFS F00 FSR0 GOTO FSR0 IF F0=1
814 0436 00 010 110 011 110 010 010 IOC OUT R4I D07 OUTPUT THE FULL WORD TO DATA-IN REG.
815 0437 11 100 100 100 100 100 001 JFS F02 **2 SKIP NEXT IF F2=1
816 0440 00 000 111 000 100 100 110 JMP LPEQ GOTO LREQ
817 0441 10 110 101 111 011 111 110 ANI LWH ROB 1 GOTO FSRF IF
818 0442 00 011 101 000 010 010 101 JMZ RCS FSRF FSR=FSF CMD.
819 0443 00 111 100 000 110 000 000 OTI LWH D01 #177 SET EVEN BYTE CNT.
820 0444 00 111 100 001 000 010 000 OTI LWH D02 #357 SET F1 TO INDICATE ODD# OF BYTES
821 0445 00 000 111 000 100 101 001 JMP EVENOR GOTO EVENOR
822 0446 11 100 111 000 100 101 000 LREQ JFS F14 **2 SKIP NEXT IF DATA F/F=1
823 0447 00 111 100 000 100 001 000 OTI LWH D01 #367 SET TIMING ERROR STATUS
824 0450 00 111 111 011 010 000 000 OTI UPH D26 #177 RST RD.CLK.& DATA F/F;SET SERV.REQ.
825 0451 10 111 100 001 100 000 000 EVENOR PSI LWH CTM #377 CNTR:=4 CHAR. DELAY
826 0452 11 100 010 000 100 101 111 JFS F10 DEC YCRC GOTO YCRC IF RD. CLK.=1
827 0453 01 010 001 000 100 101 010 JXZ RCS DEC *-1 BEFORE COUNTER = 0
828 0454 11 001 110 111 110 011 111 XOR R3M R3B R3A R3:=0(NULL CRC CHARACTER)
829 0455 01 110 111 000 111 011 001 CAL CRITE SUB. CALL TO PROCESS RD. CRCC
830 0456 00 000 111 000 100 110 001 JMP CRCHK GOTO CRCHK
831 0457 01 110 111 000 111 010 101 YCRC CAL RRITE SUB. CALL TO PROCESS CRCC
832 0460 00 111 100 010 000 000 000 OTI LWH D04 #377 RESET RD. CLK. F/F
833 0461 10 111 100 001 101 110 010 CRCHK PSI LWH CTM T22 PRESET CNTR. WITH
834 0462 10 111 110 001 111 111 110 PSI UPH CTM T4 6.2 CHAR. DELAY
835 0463 00 010 110 011 110 010 011 IOC OUT R3I D07 OUTPUT THE CRCC IN DATA-IN REG.
836 0464 01 110 111 000 111 100 001 CAL CRCCH SUB. CALL TO VERIFY CRCC
837 0465 11 100 100 100 100 110 111 JFS F02 **2 SKIP NEXT IF F2=1
838 0466 00 000 111 000 100 111 001 JMP **3 SKIP 2 INSTRUCTIONS
839 0467 00 111 100 001 010 000 000 OTI LWH D02 #177 RESET F2
840 0470 00 000 111 000 101 000 001 JMP CHLRC GOTO CHLRC
841 0471 11 100 111 000 100 111 011 JFS F14 **2 SKIP NEXT IF DATA=F/F=1
842 0472 00 111 100 000 100 001 000 OTI LWH D01 #367 SET TIMING ERROR STATUS
843 0473 00 111 110 001 010 000 000 OTI UPH D02 #177 RESET DATA F/F
844 0474 11 100 111 100 100 111 110 JFS **2 F16 SKIP NEXT IF IN-XFER=1
845 0475 00 000 111 000 101 000 001 JMP CHLRC GOTO CHLRC
846 0476 10 001 101 111 011 110 001 XOI LWH ROB RDC IF CMD. IS NOT RDC
847 0477 00 011 101 000 101 000 001 JMZ RCS CHLRC THEN GOTO CHLRC
848 0500 00 111 101 001 001 000 000 OTI LWH D22 #277 SET SERV. REQ. TO SEND CRCC & SET F2
849 0501 01 010 001 000 101 000 001 CHLRC JXZ RCS DEC * TIME OUT THE COUNTER
850 0502 11 100 100 100 101 000 100 JFS F02 **2 SKIP NEXT IF F2=1
851 0503 00 000 111 000 010 000 010 JMP ODEND GOTO ODEND
852 0504 11 100 111 000 010 000 010 JFS F14 ODEND GOTO ODEND IF DATA F/F=1
853 0505 00 111 100 000 100 001 000 OTI LWH D01 #367 SET TIMING ERROR STATUS
854 0506 00 000 111 000 010 000 010 JMP ODEND GOTO ODEND
855
856

```

SKP

Changed 31 JAN 1973

4-77

30115A

Maintenance

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

4-78
 Changed 31 JAN 1973

```

857 *****
858 *
859 * AT THE ENTRY OF BCK1 IT IS LIKELY THAT FILE-MARK IS FOUND *
860 *
861 *****
862 0507 11 100 100 010 101 001 001 BCK1 JFS F01 **2 SKIP NEXT IF F1=1
863 0510 00 000 111 000 101 001 011 JMP NOFM GOTO NOFM
864 0511 01 110 111 000 111 111 000 CAL FMPAR SUB. CALL TO LOOK FOR FM CHARACTER
865 0512 11 100 100 010 101 010 011 JFS F01 CHGAP GOTO CHGAP IF F1=1
866 *****
867 *
868 * AT THE ENTRY OF NOFM FILE-MARK IS RULED OUT *
869 *
870 *****
871 0513 11 001 110 001 110 011 111 NOFM XOR CTM R3B R3A ZERO OUT THE COUNTER
872 0514 10 111 110 001 111 111 110 PSI UPH CTM T4 CNTR:=4 CHARACTER DELAY
873 0515 00 111 000 011 000 100 000 OTI LWH DEC D06 #337 RST. RD. CLK. & F1
874 0516 01 010 001 000 101 001 110 JXZ RCS DEC * TIME OUT THE COUNTER
875 0517 00 111 100 011 000 000 000 OTI LWH D06 #377 RESET RD. CLK.
876 0520 10 111 100 001 101 110 010 PSI LWH CTM T22 CNTR:=2.2 CHARACTER DELAY
877 0521 11 100 010 000 101 001 111 JFS F10 DEC *-2 GO BACK 2 IF RD. CLK.
878 0522 01 010 001 000 101 010 001 JXZ RCS DEC *-1 CAME BEFORE COUNTER = 0
879 0523 11 001 110 001 110 011 111 CHGAP XOR CTM R3B R3A ZERO OUT THE COUNTER
880 0524 10 111 110 001 111 100 010 PSI UPH CTM T145 CNTR:=.145" DELAY
881 0525 11 100 010 000 101 011 000 JFS F10 DEC **3 SKIP 2 IF RD. CLK.
882 0526 01 010 001 000 101 010 101 JXZ RCS DEC *-1 CAME BEFORE CNTR = 0
883 0527 00 000 111 000 010 011 100 JMP RRDEC GOTO RBDEC TO SEPARATE BSR-BSF CMD.
884 0530 00 111 100 011 000 100 000 OTI LWH D06 #337 RESET RD. CLK. & F1
885 0531 11 100 100 000 101 010 011 JFS F00 CHGAP GOTO CHGAP IF F0=1(WPT. STATUS WAS 1)
886 0532 00 000 111 000 101 010 101 JMP *-5 GO BACK 5 INSTRUCTIONS
887 *****
888 *
889 * F0=1 IF THE WRITE STATUS WAS 1 BEFORE BACKSPACE STARTED *
890 * F1=1 IF THE CHARACTER READ LOOKS PART OF FILE-MARK(OCTAL 23) *
891 * F2 IS NOT USED IN THE BSR OR BSF COMMAND *
892 *
893 *****
894 SKP
    
```

Maintenance

30115A

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

895
896
897
898
899
900
901
902
*****
*
*           F0=1 AS LONG AS OUT-XFER=1 (DATA WORDS STILL COMMING)
*           F1=1 IF ATLEAST ONE READ CLOCK HAS COME
*           F2=1 IF ATLEAST ONE READ CLOCK IS FOUND
*           WITHIN TWO CHARACTER SPACING
*
*****
903 0533 01 110 011 000 001 100 010 WLOOP CAL DEC WRCHK SUB. CALL TO ASK FOR DATA WORD
904 0534 10 111 011 101 100 001 001 PSI UPH DEC ROM #366 R0(0:7):=-10
905 0535 11 100 010 000 101 100 001 WLP1 JFS F10 DEC **4 SKIP 3 IF RD. CLK.=1
906 0536 00 001 011 101 011 111 110 ADI UPH DEC ROM R0B 1 INCREMENT R0
907 0537 11 000 001 000 101 011 101 JOV RCS DEC WLP1 - GOTO WLP1 IF NO-OVERFLOW
908 0540 00 000 011 000 101 100 101 JMP **5 DEC SKIP 4 INSTRUCTIONS
909 0541 01 110 011 000 111 010 001 CAL DEC RBYTE SUB. CALL TO COMPUTE RD. CRCC & LRCC
910 0542 00 111 000 001 001 010 010 OTI LWH DEC D02 #255 SET F1,F2 & OUT MODE
911 0543 00 001 011 101 011 111 010 ADI UPH DEC ROM R0B #5 UPDATE R0 BY 5
912 0544 11 000 001 000 101 011 101 JOV RCS DEC WLP1 GOTO WLP1 IF NO-OVERFLOW
913 0545 00 010 010 001 110 000 001 IOC OUT DEC UPH R5I D03 OUTPUT THE WRITE BYTF
914 0546 11 111 010 111 101 110 111 PSA R3M DEC R5A RL4 SWOP UPPER & LOWER
915 0547 11 111 010 111 101 111 111 PSA R3M DEC R3A RL4 HALVES OF R5 IN R3
916 0550 01 110 011 000 111 100 111 CAL DEC WRCRC SUB. CALL TO COMPUTE WRITE CRCC
917 0551 01 010 001 000 101 101 001 JXZ RCS DEC * TIME OUT THE COUNTER
918 0552 00 111 110 000 000 100 000 OTI UPH D00 #337 SET WRITE STROBE
919 0553 10 111 100 001 111 000 010 PSI LWH CTM T1 CNTR:=1 CHAR. DELAY
920 0554 10 111 011 101 100 001 100 PSI UPH DEC ROM #363 R0(0:7):=-13
921 0555 11 100 010 000 101 110 001 WLP2 JFS F10 DEC **4 SKIP 3 IF RD. CLK.=1
922 0556 00 001 011 101 011 111 110 ADI UPH DEC ROM R0B 1 INCREMENT R0 BY 1
923 0557 11 000 001 000 101 101 101 JOV RCS DEC WLP2 GOTO WLP2 IF NO-OVERFLOW
924 0560 00 000 011 000 101 110 101 JMP **5 DEC SKIP 4 INSTRUCTIONS
925 0561 01 110 011 000 111 010 001 CAL DEC RBYTE SUB. CALL TO COMPUTE RD. CRCC & LRCC
926 0562 00 111 000 001 001 010 010 OTI LWH DEC D02 #255 SET F1,F2 & OUT MODE
927 0563 00 001 011 101 011 111 010 ADI UPH DEC ROM R0B #5 UPDATE R0 BY 5
928 0564 11 000 001 000 101 101 101 JOV RCS DEC WLP2 GOTO WLP2 IF NO-OVERFLOW
929 0565 11 111 010 111 101 110 111 PSA R3M DEC R5A RL4 SWOP UPPER & LOWER
930 0566 11 111 010 111 101 111 111 PSA R3M DEC R3A RL4 BYTES OF R5 IN R3
931 0567 00 010 010 001 110 000 011 IOC OUT DEC UPH R3I D03 OUTPUT WRT. BYTE
932 0570 11 111 010 111 110 010 111 PSA R3M DEC R5A PASS R5 IN R3
933 0571 01 110 011 000 111 100 111 CAL DEC WRCRC SUB. CALL TO COMPUTE WRT. CRCC
934 0572 01 010 001 000 101 111 010 JXZ RCS DEC * TIME OUT THE COUNTER
935 0573 00 111 110 000 000 100 000 OTI UPH D00 #337 SET WRITE STROBE
936 0574 10 111 100 001 111 000 010 PSI LWH CTM T1 CNTR:=1 CHAR. DELAY
937 0575 01 110 011 000 111 110 010 CAL DEC ODDW1 SUB. CALL TO FIND OUT CHAR. DROPOUT
938 0576 11 100 000 000 101 011 011 JFS F00 DEC WLOOP GOTO WLOOP IF F0=1
939 0577 11 111 111 101 110 001 011 PSA UPH ROM R4A MAKE R0 BACK TO WHAT IT WAS
940 0600 10 011 101 101 001 111 111 IOI LWH ROM R0R #200 SET BIT 8 IN R0 TO INDICATE CRCC BYTE
941 0601 10 001 001 010 100 101 000 XOI LWH DEC R1M R1B #327 UPDATE CRC CHARACTER
942 0602 11 010 010 110 101 111 111 PSB R3M DEC R1B RL4 OUTPUT
943 0603 11 111 010 111 101 111 111 PSA R3M DEC R3A RL4 CRC
944 0604 00 010 010 001 110 000 011 IOC OUT DEC UPH R3I D03 CHARACTER
945
946
*****
SKP

```


Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

947
948
949
950
951
952
953 0605 10 111 100 001 101 111 111 OTCRC PSI LWH CTM #200 CNTR:=2.0 CHAR. DELAY
954 0606 10 111 011 011 100 100 111 PSI UPH DEC R1M #330 R1(0:7):=-40
955 0607 11 100 010 000 110 001 011 OTC1 JFS F10 DEC **4 SKIP 3 IF RD. CLK.=1
956 0610 00 001 011 010 111 111 110 ADI UPH DEC R1M R1B 1 INCREMENT R1
957 0611 11 000 001 000 110 000 111 JOV RCS DEC OTC1 GOTO OTC1 IF NO-OVERFLOW
958 0612 00 000 011 000 110 001 111 JMP **5 DEC SKIP 4 INSTRUCTIONS
959 0613 01 110 011 000 111 010 001 CAL DEC RBYTF SUB. CALL TO COMPUTE RD. CRCC & LRCC
960 0614 00 111 000 001 001 010 010 OTI LWH DEC D02 #255 SET F1,F2 & OUT MODE
961 0615 00 001 011 010 111 111 010 ADI UPH DEC R1M R1B #5 UPDATE R1 BY 5
962 0616 11 000 001 000 110 000 111 JOV RCS DEC OTC1 GOTO OTC1 IF NO-OVERFLOW
963 0617 00 111 010 001 000 110 000 OTI UPH DEC D02 #317 TOGGLE F0
964 0620 01 010 001 000 110 010 000 JXZ RCS DEC * TIME OUT THE COUNTER
965 0621 01 110 111 000 111 110 010 CAL ONDWH1 SUB. CALL TO DETECT CHARACTER DROPOUT
966 0622 10 110 101 111 001 111 111 ANI LWH R0B #200 LOOK FOR BIT 8 OF R0
967 0623 00 011 111 000 110 011 000 JMZ OTC2 GOTO OTC2 IF R0(8)=0
968 0624 11 100 100 000 110 000 101 JFS F00 OTCRC GOTO OTCRC IF F0=1
969 0625 10 110 101 101 010 000 000 ANI LWH R0M R0B #177 MAKF BIT 8 OF R0 = 0
970 0626 00 111 110 000 000 100 000 OTI UPH D00 #337 SET WRITE STROBE (TO WRITE CRCC)
971 0627 00 000 111 000 110 000 101 JMP OTCRC GOTO OTCRC
972 0630 11 100 100 000 110 000 101 OTC2 JFS F00 OTCRC GOTO OTCRC IF F0=1
973 0631 00 111 100 001 010 000 000 OTI LWH D02 #177 RESET F2
974 0632 00 111 110 000 000 010 000 LRCC OTI UPH D00 #357 SET WRITE RESET PULSF
975 0633 00 111 100 001 000 000 101 OTI LWH D02 #372 ENABLE PARITY & SET IN-MODF
976 0634 11 100 100 010 110 110 100 JFS F01 YESRD GOTO YESRD IF F1=1
977 0635 10 111 110 001 111 100 000 NORD PSI UPH CTM T155 CNTR:=.155" DELAY
978 0636 11 100 010 000 110 100 001 JFS F10 DEC **3 SKIP 2 IF RD. CLK.=1
979 0637 01 010 001 000 110 011 110 JXZ RCS DEC *-1 BEFORE CNTR=0
980 0640 00 000 111 000 001 111 111 JMP DROP CHAR. DROPOUT-GO TO DROP
981 0641 01 110 111 000 111 111 000 CAL FMPAR SUB. CALL TO LOOK FOR FM BYTE
982 0642 01 110 111 000 111 010 001 CAL RRYTF SUB. CALL TO COMPUTE RD. CRCC
983 0643 11 001 110 001 110 011 111 XOR CTM R3B R3A ZERO OUT THE COUNTER
984 0644 11 100 100 100 110 100 110 JFS F02 **2 SKIP NEXT IF F2=1(WFM CMD.)
985 0645 00 000 111 000 110 110 100 JMP YESRD GOTO YESRD
986 0646 11 100 100 010 110 101 000 JFS F01 **2 SKIP NEXT IF F1=1
987 0647 00 000 111 000 001 111 111 JMP DROP GOTO DROP
988 0650 10 111 110 001 111 111 101 PSI UPH CTM T8 CNTR:=
989 0651 10 111 100 001 101 110 010 PSI LWH CTM T22 10.2 CHAR. DELAY
990 0652 11 100 010 000 110 101 101 JFS F10 DEC **3 SKIP 2 IF RD. CLK. = 1
991 0653 01 010 001 000 110 101 010 JXZ RCS DEC *-1 BEFORE CNTR 0
992 0654 00 000 111 000 001 111 111 JMP DROP CHAR. DROPOUT CASE-GOTO DROP
993 0655 01 110 111 000 111 111 000 CAL FMPAR SUB. CALL TO LOOK FOR FM BYTE
994 0656 11 100 100 010 110 110 000 JFS F01 **2 SKIP NEXT IF F1=1
995 0657 00 000 111 000 001 111 111 JMP DPOP FM DOES NOT MATCH-GOTO DROP
996 0660 10 111 110 001 111 111 101 PSI UPH CTM T8 CNTR:=8.0 CHAR. DELAY
997 0661 11 100 010 000 001 111 111 JFS F10 DEC DROP GOTO DROP IF RD. CLK.=1
998 0662 01 010 001 000 110 110 001 JXZ RCS DEC *-1 BEFORE CNTR=0
999 0663 00 000 111 000 010 000 001 JMP FILE GOTO FILE(IFM CONFIRMED)
1000
1001 SKP
    
```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

1002
1003
1004
1005
1006
1007
1008 0664 10 111 100 001 101 110 010
1009 0665 11 100 010 000 110 111 000
1010 0666 01 010 001 000 110 110 101
1011 0667 00 000 111 000 110 111 010
1012 0670 01 110 111 000 111 010 001
1013 0671 00 000 111 000 110 110 100
1014 0672 10 111 100 001 100 000 000
1015 0673 11 100 010 000 110 111 110
1016 0674 01 010 001 000 110 111 011
1017 0675 00 000 111 000 001 111 111
1018 0676 01 110 111 000 111 010 001
1019 0677 10 111 100 001 101 110 010
1020 0700 11 100 010 000 001 111 111
1021 0701 01 010 001 000 111 000 000
1022 0702 01 110 111 000 111 100 001
1023 0703 10 111 110 001 111 111 110
1024 0704 01 010 001 000 111 000 100
1025 0705 00 000 111 000 010 000 010
1026
1027
1028
1029
1030
1031 0706 10 001 101 111 011 111 010
1032 0707 00 011 101 000 111 001 010
1033 0710 01 110 111 000 001 011 010
1034 0711 00 000 111 000 010 000 010
1035 0712 00 111 110 001 111 101 100
1036 0713 10 111 110 001 111 111 101
1037 0714 00 111 110 000 000 100 000
1038 0715 01 010 001 000 111 001 101
1039 0716 00 111 110 001 000 100 000
1040 0717 00 111 100 001 001 000 000
1041 0720 00 000 111 000 110 011 010
1042
1043
*****
*
*   ENTRY AT YESRD ONLY IF A READ CLOCK IS ENCOUNTERED
*   DURING THE WRITING OF A DATA BLOCK
*
*****
YESRD PSI LWH CTM T22          CNTR:=2.2 CHAR. DELAY
      JFS F10 DEC **3          SKIP 2 IF RD. CLK.=1
      JXZ RCS DEC *-1          BEFORE CNTR = 0
      JMP **3                  SKIP 2 INSTRUCTIONS
      CAL RRYTE                SUB. CALL TO COMPUTE RD. CRCC
      JMP YFSRD                GO BACK TO YESRD
      PSI LWH CTM #377         CNTR:=4.0 CHAR. DELAY
      JFS F10 DEC **3          SKIP 2 IF RD. CLK.=1
      JXZ RCS DEC *-1          BEFORE CNTR=0
      JMP DPOP                  CRCC=0; GOTO DROP(CHAR. DROPOUT)
      CAL RRYTE                SUB. CALL TO COMPUTE CRCC
      PSI LWH CTM T22          CNTR:=2.2 CHAR. DELAY
      JFS F10 DEC DROP        GOTO DROP IF RD. CLK.=1
      JXZ RCS DEC *-1          BEFORE CNTR. = 0
      CAL CRCC                 SUB. CALL TO VERIFY READ CRCC
      PSI UPH CTM T4           CNTR:=4 CHAR. DELAY
      JXZ RCS DEC *            TIME OUT THE COUNTER
      JMP ODEND                GOTO ODEND
*****
*
*   ENTRY AT GPFM ONLY IF WFM OR GAP COMMAND
*
*****
GPFM XOI LWH ROB GAP          LOOK FOR GAP COMMAND
      JMZ RCS **3              SKIP 2 IF WFM COMMAND
      CAL WGAP                 WRITE A GAP OF 3.75 INCH
      JMP ODEND                FO TO ODEND
      OTI UPH D03 FM           OUTPUT THE FILE-MARK CHARACTER
      PSI UPH CTM T8           PRESET THE CNTR WITH T8.0 DELAY
      OTI UPH D00 #337         SET WRITE STROBE
      JXZ RCS DEC *            TIME OUT THE COUNTER
      OTI UPH D02 #337         SET F0
      OTI LWH D02 #277         SET F2 TO INDICATE WFM CMD.
      JMP LRCQ                 GOTO LRCQ
*****
SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

1044
1045
1046
1047
1048
1049
1050 0721 00 111 000 001 000 000 001 RBYTE OTI LWH DEC D02 #376 SET IN-MODE F/F
1051 0722 00 111 000 010 000 000 000 OTI LWH DEC D04 #377 RESET RD. CLK. F/F
1052 0723 11 100 010 010 111 010 101 JFS F11 DEC **2 SKIP NEXT IF PARITY OKAY
1053 0724 00 111 000 000 100 010 000 OTI LWH DEC D01 #357 SET TAPE ERROR BIT
1054 0725 00 010 000 101 010 001 011 RBITE IOC INP DEC LWH R3I D12 GET READ BYTE IN R3
1055 0726 10 111 010 111 111 111 110 WBYTE PSI UPH DEC R3M 1 R3(R):=1
1056 0727 11 100 001 100 111 011 001 JFS F06 DEC **2 SKIP NEXT IF READ PARITY = 1
1057 0730 11 001 010 111 110 001 111 XOR UPH DEC R3M R3B R3A ZERO OUT UPPER HALF OF R3
1058 0731 11 001 011 000 001 011 111 CBITE XOR R2M DEC R2B R3A RR1 CRCR:=(CRCR 'XOR' R3) ROTATED RT. 1
1059 0732 11 010 011 000 010 011 111 PSB R2M DEC R2R LOOK FOR SIGN OF R2
1060 0733 10 100 011 000 111 011 111 JSZ **4 DEC SKIP 3 IF SIGN = 0
1061 0734 10 111 011 001 111 111 110 PSI UPH DEC R2M 1 MODIFY CRCR-PIT SIGN IN BIT 7 OF R2
1062 0735 10 001 001 000 011 000 011 XOI LWH DEC R2M R2B #74 INVERT BITS 10-13 OF R2
1063 0736 01 101 011 111 111 111 111 RTN DEC SUBROUTINE RETURN
1064 0737 11 001 011 001 110 001 111 XOR UPH DEC R2M R3B R3A ZERO OUT UPPER HALF OF R2
1065 0740 00 000 011 000 111 011 110 JMP *-2 DEC GO BACK 2 INSTRUCTIONS
1066
1067
1068
1069
1070
1071
1072
1073
1074
1075 0741 10 001 101 000 000 101 000 CRCCH XOI LWH R2M R2B #327 UPDATE FINAL
1076 0742 10 001 111 000 011 111 110 XOI UPH R2M R2B #1 CRC CHARACTER
1077 0743 11 010 111 000 010 011 111 PSB R2M R2B R2 SHOULD BE 0 FOR GOOD DATA BLOCK
1078 0744 00 011 111 000 111 100 110 JMZ **2 SKIP NEXT IF CRCC CHCKS OUT
1079 0745 00 111 100 000 100 010 000 OTI LWH D01 #357 SET TAPE ERROR BIT
1080 0746 01 101 111 111 111 111 111 RTN SUBROUTINE RETURN
1081
1082

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

1083
1084
1085
1086
1087
1088
1089
1090 0747 11 001 010 111 110 001 111 WRRCR XOR UPH DEC R3M R3B R3A ZERO OUT UPPER HALF OF R3
1091 0750 11 100 001 100 111 101 010 JFS F06 DEC **2 SKIP NEXT IF WRITE PARITY = 0
1092 0751 10 111 010 111 111 111 110 PSI UPH DEC R3M 1 APPEND PARITY IN BIT 7 OF R3
1093 0752 11 001 011 010 101 011 111 XOR R1M DEC R1B R3A RR1 CRCR:=(CRCR 'XOR' R3) ROTATED RT. 1
1094 0753 11 010 011 010 110 011 111 WRRCR PSR R1M DEC R1B LOOK FOR SIGN OF R1
1095 0754 10 100 011 000 111 110 000 JSZ **4 DEC SKIP 3 IF SIGN=0
1096 0755 10 111 011 011 111 111 110 PSI UPH DEC R1M 1 MODIFY CRCR-PUT SIGN IN BIT 7 OF R1
1097 0756 10 001 001 010 111 000 011 XOI LWH DEC R1M R1B #74 INVERT BITS 10-13 OF R1
1098 0757 01 101 011 111 111 111 111 RTN DEC SUBROUTINE RETURN
1099 0760 11 001 011 011 110 001 111 XOR UPH DEC R1M R3B R3A ZERO OUT UPPER HALF OF R1
1100 0761 00 000 011 000 111 101 111 JMP *-2 DEC GO BACK 2 INSTRUCTIONS
1101
1102
1103
1104
1105
1106
1107
1108
1109 0762 11 100 000 010 111 110 100 ODDW1 JFS F01 DEC **2 SKIP NEXT IF I-CHAR. FLAG=1
1110 0763 00 000 011 000 111 110 111 JMP **4 DEC NO CHARACTER YET-GO BACK
1111 0764 11 100 000 100 111 110 110 JFS F02 DEC **2 SKIP NEXT IF II-CHAR. FLAG=1
1112 0765 00 000 011 000 001 111 111 JMP DEC DROP CHAR. DROPOUT CASE-GOTO DROP
1113 0766 00 111 000 001 010 000 000 OTI LWH DEC D02 #177 RESET F2 (II-CHAR. FLAG)
1114 0767 01 101 011 111 111 111 111 RTN DEC SUBROUTINE RETURN
1115
1116
1117
1118
1119
1120
1121
1122
1123 0770 00 111 100 011 000 100 000 FMPAR OTI LWH D06 #337 RESET F1 & RD. CLK. F/F
1124 0771 00 010 100 101 010 001 011 IOC INP LWH R3I D12 GET READ BYTE IN R3
1125 0772 11 100 101 100 111 111 110 JFS **4 F06 RETURN IF PARITY = 1
1126 0773 10 001 101 111 111 101 100 XOI LWH R3B FM SET F1 IF
1127 0774 00 011 101 000 111 111 110 JMZ RCS **2 THE READ BYTE
1128 0775 00 111 100 001 000 010 000 OTI LWH D02 #357 IS A FILE MARK
1129 0776 01 101 111 111 111 111 111 RTN DEC SUBROUTINE RETURN
1130
1131 0777 01 000 111 111 111 111 111 NOP
1132 SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

1133
1134
1135
1136
1137
1138 1000 00 111 100 101 000 100 000
1139 1001 00 010 111 001 010 001 011
1140 1002 10 110 111 111 110 111 111
1141 1003 00 011 101 001 000 000 101
1142 1004 00 111 100 001 000 010 000
1143 1005 01 101 111 111 111 111 111
1144
1145 1006 01 110 111 001 000 000 000
1146 1007 00 000 111 001 000 011 010
1147
1148
1149
1150
1151
1152
1153 1010 00 010 111 001 010 001 011
1154 1011 10 110 111 111 111 011 111
1155 1012 00 011 101 001 000 001 100
1156 1013 00 111 100 000 100 010 000
1157 1014 01 101 111 111 111 111 111
1158
1159
1160
1161
1162
1163
1164 1015 11 001 010 010 110 000 111
1165 1016 11 100 000 101 000 010 000
1166 1017 00 111 000 000 000 000 011
1167 1020 00 010 010 001 110 000 001
1168 1021 01 010 001 001 000 010 001
1169 1022 00 111 110 000 000 100 000
1170 1023 01 101 111 111 111 111 111
1171
1172
1173
1174
1175
1176 1024 11 100 101 111 000 011 001
1177 1025 11 100 110 001 000 010 111
1178 1026 00 000 111 001 000 010 100
1179 1027 00 111 100 011 000 000 000
1180 1030 00 000 111 001 000 010 100
1181 1031 00 111 100 001 000 100 000
1182 1032 11 001 110 001 110 011 111
1183 1033 10 111 110 001 111 100 010
1184 1034 00 111 000 100 000 000 000
1185 1035 01 010 001 001 000 011 101
1186 1036 00 000 111 000 010 011 100
1187
1188

*****
*
*           FMP16 SETS F1 IF FILE-MARK IS FOUND(1600 BPI).
*
*****
FMP16  OTI LWH D12 #337          RESET F1 & EOB FLAG
        IOC INP R3I D22 UPH      GET STATUS BYTE IN R3
        ANI UPH R3B #100         LOOK FOR TAPE MARK BIT
        JMZ RCS **2              SKIP NEXT IF TAPE MARK BIT = 0
        OTI LWH D02 #357         SET F1 TO INDICATE TAPE MARK
        RTN                       SUBROUTINE RETURN
*****
FMP16  CAL FMP16                SUB. CALL TO LOOK FOR TAPE MARK
        JMP RCK2                  GOTO BCK2
*****
*
*           SUBROUTINE ERR16 SETS TAPE ERROR F/F IF AN ERROR
*           IS DISCOVERED BY THE TAPE DRIVE(1600 BPI ONLY).
*
*****
ERR16  IOC INP UPH R3I D22      GET STATUS BYTE IN R3
        ANI UPH R3B #40         LOOK FOR TAPE ERROR
        JMZ RCS **2              SKIP NEXT IF TAPE ERROR=0
        OTI LWH D01 #357         SET TAPE ERROR BIT OF STATUS
        RTN                       SUBROUTINE RETURN
*****
*
*           SUBROUTINES WRTP1 & WRTP3 ARE CALLED TO OUTPUT
*           THE WRITE BYTE & SET WRITE STROBE(1600 BPI)
*
*****
WRTP1  XOR UPH DEC R5M R5A R1B  R5(UPPER):=R5 XOR R1
WRTP2  JFS **2 DEC F02          SKIP NEXT IF F2=1(WFM)
WRTP3  OTI LWH DEC D00 #374     TOGGLE ODD/EVEN F/F
        IOC OUT DEC UPH R5I D03 OUTPUT THE BYTE FROM R5
        JXZ RCS DEC *           TIME OUT THE COUNTER
        OTI UPH D00 #337        SET WRITE STROBE
        RTN                       SUBROUTINE RETURN
*****
*
*           BCKRD IS THE READ REV. 1600 BPI ROUTINE(F0=1 IF WRT. STATUS WAS 1)
*
*****
BCKRD  JFS F07 **5              SKIP 4 IF F0B=1
        JFS F10 **2              SKIP NEXT IF RD. CLK.=1
        JMP BCKRD                GOTO BCKRD
        OTI LWH D06 #377         RESET RD. CLK. F/F
        JMP BCKRD                GO BACK TO BCKRD
        OTI LWH D02 #337         RESET F1
BCK2   XOR CTM R3B R3A          ZERO OUT THE COUNTER
        PSI UPH CTM T145         CNTR:=.145 IN. DELAY
        OTI LWH DEC D10 #377     RESET EOB FLAG
        JXZ RCS DEC *           TIME OUT THE COUNTER
        JMP RBDEC                GOTO RBDEC
*****
SKP

```


Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

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```

1247 *****
1248 *
1249 *       AT IDENT 2" OF ID BURST IS WRITTEN AT LOAD POINT
1250 *
1251 *****
1252 1124 11 001 110 011 110 011 111 IDENT XOR R5M R3B R3A ZERO OUT R5
1253 1125 10 111 111 001 100 001 000 PSI R2M UPH #367 SET R2 WITH 2" ID-BURST COUNT
1254 1126 10 111 100 011 111 111 110 PSI R5M LWH #1 RS:=1
1255 1127 01 001 111 000 010 010 111 ADD R2M R2B R5A INCREMENT R2
1256 1130 10 111 100 001 111 100 101 PSI CTM LWH #32 PRESET THE COUNTER
1257 1131 01 110 011 001 000 001 111 CAL DFC WRTP3 SUBROUTINE CALL
1258 1132 01 001 111 000 010 010 111 ADD R2M R2B R5A R2:=R2+1
1259 1133 00 011 101 001 001 011 000 JMZ RCS *-3 GO BACK IN LOOP IF R2 IS NON-ZERO
1260 1134 01 110 111 000 001 011 010 CAL WGAP CALL TO WGAP TO WRITE A GAP
1261 1135 11 100 101 111 001 011 111 JFS F07 **2 SKIP NEXT IF EOB DETECTED BY DRIVE
1262 1136 00 000 111 000 001 111 111 JMP DROP NO EOB - ERROR CASE
1263 1137 01 110 111 001 000 001 000 CAL ERR16 SUB. CALL TO LOOK FOR TAPE ERROR
1264 1140 00 111 100 101 000 010 000 OTI LWH D12 #357 SET F1 & RESET EOB
1265 1141 00 010 111 001 010 001 011 IOC INP UPH R3I D22 GET 1600 STATUS IN R3
1266 1142 10 110 111 111 101 111 111 ANI UPH R3B #200 LOOK FOR ID-BURST STATUS
1267 1143 00 011 111 001 001 100 101 JMZ **2 ID-BURST CONFIRMED-SKIP NEXT INSTRUCTION
1268 1144 00 000 111 000 001 111 111 JMP DROP NO ID-BURST STATUS-ERROR CASE
1269 *****
1270 *       WR16 IS THE LOOP-ENTRY POINT FOR WRITING PREAMBLE,
1271 *       POSTAMBLE OR FILE-MARK BLOCK. (1600 BPI ONLY)
1272 *****
1273 1145 10 110 101 111 011 111 110 WR16 ANI LWH ROB 1 LOOK FOR SUBGROUP OF WRITE
1274 1146 00 011 111 001 001 101 000 JMZ **2 SKIP NEXT IF WRR CMD.
1275 1147 00 111 100 001 001 000 000 OTI LWH D02 #277 SET F2 TO INDICATE WFM OR GAP CMD.
1276 1150 11 100 100 011 001 101 010 JFS F01 **2 SKIP NEXT IF F1=1 (NOT BOT)
1277 1151 00 000 111 001 001 010 100 JMP IDENT GOTO IDENT TO WRITE ID-BURST
1278 1152 00 111 100 000 000 000 001 OTI LWH D00 #376 SET ODD F/F
1279 1153 10 111 111 011 100 000 000 PSI R1M UPH #377 FILL UPPER BYTE OF R1 WITH ALL 1'S
1280 1154 00 111 100 001 000 100 000 OTI LWH D02 #337 RESET F1
1281 1155 10 111 111 001 101 001 111 PSI R2M UPH #260 R2:=-80
1282 1156 11 100 100 101 001 110 000 JFS F02 **2 SKIP NEXT INSTRUCTION IF F2=1
1283 1157 00 000 111 001 001 111 010 JMP WRT16 WRR CMD.-GOTO WR16 TO WRITE PREAMBLE
1284 1160 10 001 101 111 011 111 010 XOI LWH ROB GAP LOOK FOR GAP COMMAND
1285 1161 00 011 101 001 001 110 111 JMZ RCS **6 SKIP 5 IF WFM COMMAND
1286 1162 01 110 111 000 001 011 010 CAL WGAP SUBROUTINE CALL TO WRITE 3.75" GAP
1287 1163 11 100 101 111 001 110 101 JFS F07 **2 SKIP NEXT IF EOB FLAG=1
1288 1164 00 000 111 000 010 000 010 JMP ODEND GOTO ODEND
1289 1165 01 110 111 001 000 001 000 CAL ERR16 SUB. CALL TO LOOK FOR TAPE ERROR
1290 1166 00 000 111 000 010 000 010 JMP ODEND GOTO ODEND
1291 1167 00 111 100 000 000 000 010 OTI LWH D00 #375 SET EVEN F/F
1292 1170 10 111 111 011 101 011 000 PSI R1M UPH #247 R1(UPPER):=FM CHARACTER
1293 1171 10 111 111 001 101 010 000 PSI R2M UPH #257 R2:=-81
1294 1172 11 010 110 010 110 001 111 WRT16 PSB R5M UPH R1B PASS UPPER BYTE OF R1 IN R5
1295 1173 10 111 100 001 111 110 101 LPFM PSI CTM LWH #12 PRESET THE COUNTER
1296 1174 01 110 011 001 000 001 101 LPFM1 CAL DEC WRTP1 SUBROUTINE CALL
1297 1175 00 001 111 000 011 111 110 ADI R2M UPH R2B #1 R2(UPPER):=R2+1
1298 1176 00 011 101 001 001 111 011 JMZ RCS LPFM GO IN LOOP IF R2 IS NON-ZERO
1299 1177 11 100 100 101 010 011 001 JFS F02 FIN16 GOTO FIN16 IF F2=1
1300 1200 10 111 100 001 111 100 110 PSI CTM LWH #31 PRESET THE COUNTER
1301 1201 11 100 000 001 010 011 001 BLK16 JFS F00 DEC FIN16 GOTO FIN16 IF F0=1 (POSTAMBLE WRITTEN)
1302 1202 01 110 011 001 000 001 101 CAL DEC WRTP1 SUBROUTINE CALL
1303 *****
1304 SKP

```

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

1305
1306
1307
1308
1309
1310 1203 10 111 100 001 111 110 100
1311 1204 01 110 011 000 001 100 010
1312 1205 01 110 011 001 000 001 111
1313 1206 10 111 100 001 111 110 011
1314 1207 01 110 011 001 000 001 101
1315 1210 11 111 110 011 101 110 111
1316 1211 11 111 110 011 101 110 111
1317 1212 10 111 100 001 111 110 101
1318 1213 01 110 011 001 000 001 111
1319 1214 10 111 100 001 111 110 011
1320 1215 01 000 011 111 111 111 111
1321 1216 01 110 011 001 000 001 101
1322 1217 11 100 100 001 010 000 011
1323 1220 11 001 010 011 110 011 111
1324 1221 10 111 100 001 111 110 100
1325 1222 01 110 011 001 000 001 101
1326 1223 10 111 100 001 111 110 011
1327 1224 01 110 011 001 000 001 101
1328 1225 10 111 100 001 111 100 011
1329 1226 10 111 011 001 101 001 111
1330 1227 00 111 010 001 000 100 000
1331 1230 00 000 011 001 001 111 100
1332
1333
1334
1335
1336
1337
1338
1339 1231 00 111 100 000 000 000 001
1340 1232 11 100 100 101 010 011 101
1341 1233 10 111 110 001 111 001 100
1342 1234 00 000 011 001 010 011 110
1343 1235 10 111 110 001 111 011 100
1344 1236 11 100 001 111 010 100 001
1345 1237 01 010 001 001 010 011 110
1346 1240 00 000 111 000 001 111 111
1347 1241 11 100 100 101 010 100 100
1348 1242 01 110 111 001 000 001 000
1349 1243 00 000 111 000 010 000 010
1350 1244 01 110 111 001 000 000 000
1351 1245 00 000 111 000 001 111 101
1352
1353
1354
1355 1246 10 001 101 111 011 111 001
1356 1247 00 011 101 001 010 101 010
1357 1250 11 100 110 011 010 101 010
1358 1251 00 111 100 000 100 010 000
1359 1252 01 101 111 111 111 111 111
1360
1361

*****
*          WLP16 IS THE LOOP-ENTRY POINT FOR WRITING THE
*          DATA-BLOCK. F0=1 AS LONG AS OUT-XFER=1.
*          (1600 BPI ONLY)
*****
WLP16 PSI CTM LWH #13          PRESET THE COUNTER
      CAL DEC WRCHK          SUBROUTINE CALL TO WFCHK
      CAL DEC WRTP3          SUBROUTINE CALL
      PSI CTM LWH #14          PRESET THE COUNTER
      CAL DEC WRTP1          SUBROUTINE CALL
      PSA R5M R5A RL4          LEFT ROTATE R5
                                BY 8-BITS IN R5
      PSI CTM LWH #12          PRESET THE COUNTER
      CAL DEC WRTP3          SUBROUTINE CALL
      PSI CTM LWH #14          PRESET THE COUNTER
      NOP DEC                NO-OPERATION
      CAL DEC WRTP1          SUBROUTINE CALL
      JFS F00 WLP16          GO IN THE WRITE LOOP IF F0=1
      XOR R5M DEC R3B R3A    ZERO OUT R5
      PSI CTM LWH #13          PRESET THE COUNTER
      CAL DEC WRTP1          SUBROUTINE CALL
      PSI CTM LWH #14          PRESET THE COUNTER
      CAL DEC WRTP1          SUBROUTINE CALL
      PSI CTM LWH #34          PRESET THE COUNTER
      PSI R2M DEC UPH #260    R2(UPPER):=-80
      OTI UPH DEC D02 #337    SET F0 TO INDICATE POSTAMBLE CASE
      JMP DEC LPFM1          GOTO WRITE POSTAMBLE
*****
*          *****
*          AN END OF BLOCK PULSE IS AWAITED AT FIN16 AFTER
*          WRITING OF DATA BLOCK OR FILE-MARK IS DONE.
*          TAPE ERROR OR FILE-MARK STATUS IS
*          CHECKED TO ENSURE SUCCESSFUL
*          WRITING(1600 BPI).
*          *****
FIN16 OTI LWH D00 #376        SET ODD F/F
      JFS F02 FM166          GOTO FM166 IF F2=1
      PSI UPH CTM #63        CNTR:=.155" + 80 CHARACTER DELAY
      JMP **2 DEC            SKIP NEXT INSTRUCTION
FM166 PSI UPH CTM #43        CNTR:=.155" + 20 CHARACTER DELAY
      JFS F07 DEC **3        SKIP 2 IF F0B=1
      JXZ RC5 DEC **1        STAY IN LOOP TILL CNTR. NON-ZERO
      JMP DROP              CHARACTER DROPOUT CASE
      JFS F02 **3          SKIP 2 IF WFM COMMAND
      CAL EPR16            SUB. CALL TO LOOK FOR TAPE ERROR
      JMP ODEND            GOTO ODEND
      CAL FMP16            SUB. CALL TO LOOK FOR TAPE MARK
      JMP FMB16            GOTO FMB16
*****
*          SUBROUTINE TO CHECK PARITY OF EACH BYTE IN RDR CMD.
*          *****
ERCHK XOI LWH R0B RDR        PERFORM PARITY CHECK ONLY
      JMZ RCS **3          IF THE COMMAND IS 'PDR'
      JFS F11 **2          SKIP NEXT IF PARITY OK
      OTI LWH D01 #357      SET TAPE ERROR F/F
      RTN                  SUBROUTINE RETURN
*****
SKP

```

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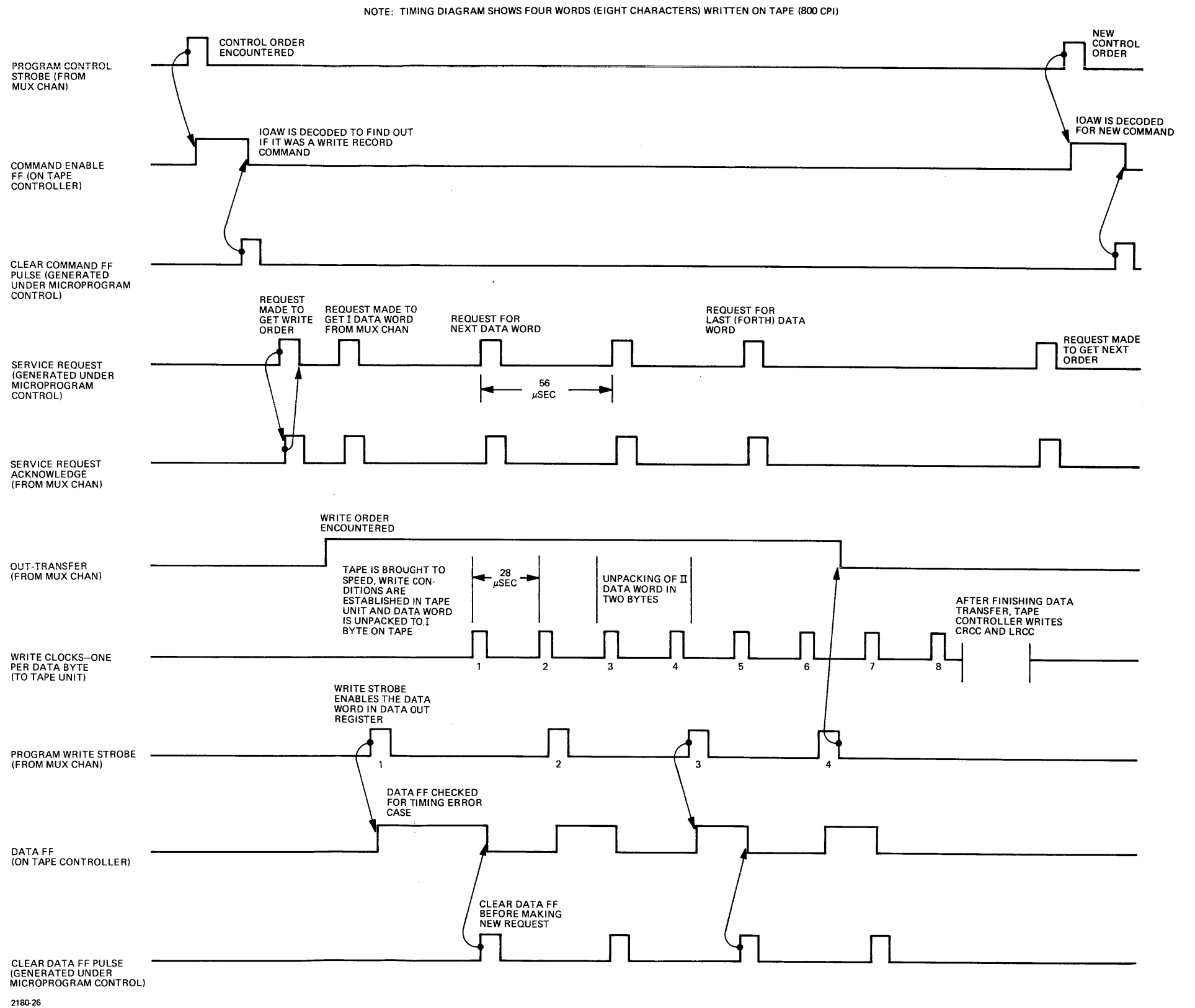
Maintenance

Table 4-4. Magnetic Tape Subsystem Microprogram Listing (Continued)

```

1362
1363
1364
1365
1366
1367 1314 00 010 111 001 010 001 011 PTCH1 IOC INP R3I D22 UPH GET STATUS BYTE IN UPPER R3
1368 1315 10 110 111 111 111 101 111 ANI UPH R3B #20 IS INT. FLAG=1?
1369 1316 00 011 101 001 011 001 100 JMZ RCS *-2 YES, KEEP LOOKING AT THIS BIT
1370 1317 10 111 111 011 111 001 100 PSI UPH R1M #63 R1:=(TRYING TO SELECT UNIT)
1371 1320 00 000 111 000 000 001 011 JMP CONT1 GOTO CONT1 TO CONTINUE WITH THE PROGRAM
1372
1373
1374
1375
1376
1377 1327 00 010 111 001 010 001 011 PTCH2 IOC INP R3I D22 UPH GET STATUS BYTE IN R3
1378 1330 10 110 111 111 111 110 111 ANI UPH R3B #10 LOOK FOR SIO OK BIT
1379 1331 00 011 101 000 000 001 111 JMZ RCS MAIN GOTO MAIN IF ALREADY IN SIO ROUTINE
1380 1332 00 010 111 001 010 001 011 IOC INP R3I D22 UPH GET STATUS BYTE IN R3
1381 1333 10 110 111 111 111 101 111 ANI UPH R3B #20 IS INT. FLAG=1?
1382 1334 00 011 101 001 011 011 010 JMZ RCS *-2 YES, KEEP LOOKING AT THIS BIT
1383 1335 00 000 111 000 000 110 101 JMP SCANO GO BACK TO SCANO
1384
1385
1386
1387
1388
1389 1361 10 111 100 001 100 010 001 PATCH PSI LWH CTM TCOST PRESET THE COUNTER WITH COAST DELAY
1390 1362 11 100 111 101 011 110 100 JFS F16 *-2 SKIP NEXT IF IN-XFER=1
1391 1363 00 000 111 001 011 110 110 JMP *-3 SKIP 2 INSTRUCTIONS
1392 1364 00 111 110 001 000 001 000 OTI UPH D02 #367 SET DEVICE-END
1393 1365 00 000 111 001 011 110 111 JMP *-2 SKIP NEXT INSTRUCTION
1394 1366 00 111 111 000 000 000 000 OTI UPH D20 #377 SET SERV. REQ.
1395 1367 01 010 001 001 011 110 111 JXZ RCS DEC * TIME OUT THE COUNTER
1396 1370 00 010 111 001 010 001 011 IOC INP R3I D22 UPH GET STATUS BYTE IN UPPER R3
1397 1371 10 110 111 111 111 101 111 ANI UPH R3B #20 IS INT. FLAG=1?
1398 1372 00 011 111 000 010 001 101 JMZ STOPI NO, GOTO STOPI
1399 1373 00 000 111 000 000 000 100 JMP WAIT INTERRUPT NOT YET PROCESSED, GOTO WAIT
1400
1401
    END
    
```

0 ERRORS



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Figure 4-12. Typical Write Operation, Tape Controller Timing Diagram

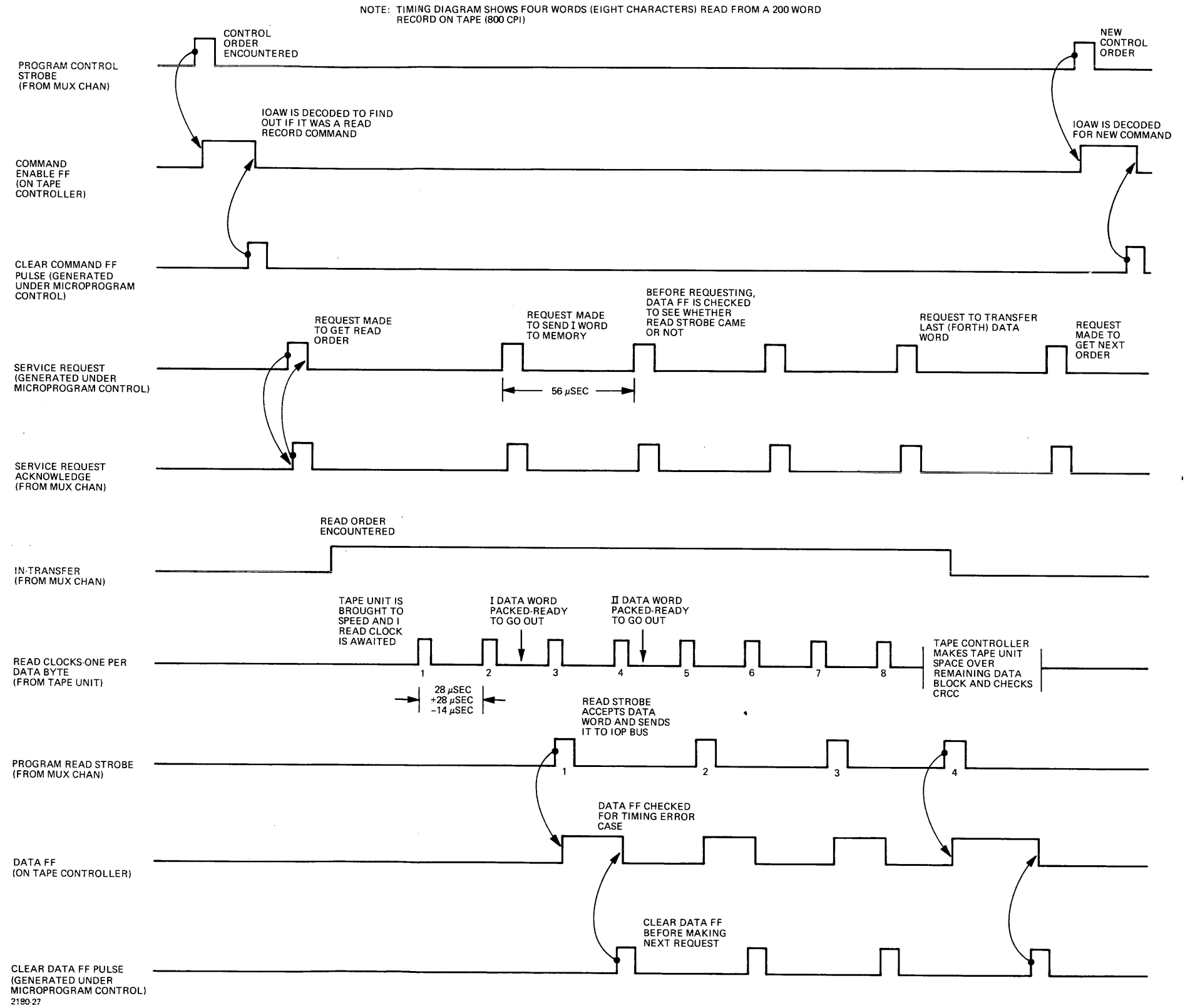


Figure 4-13. Typical Read Operation, Tape Controller Timing Diagram

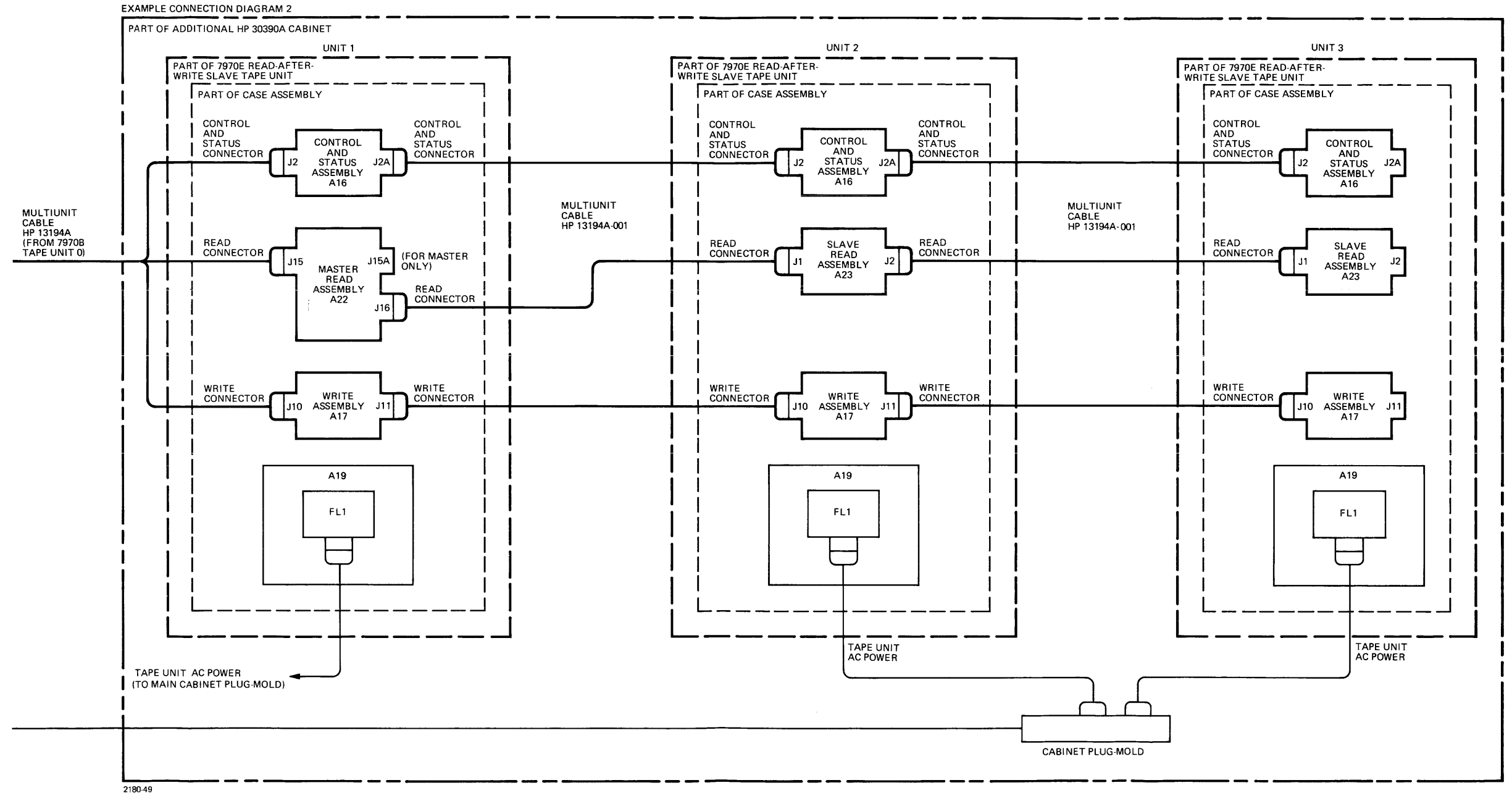
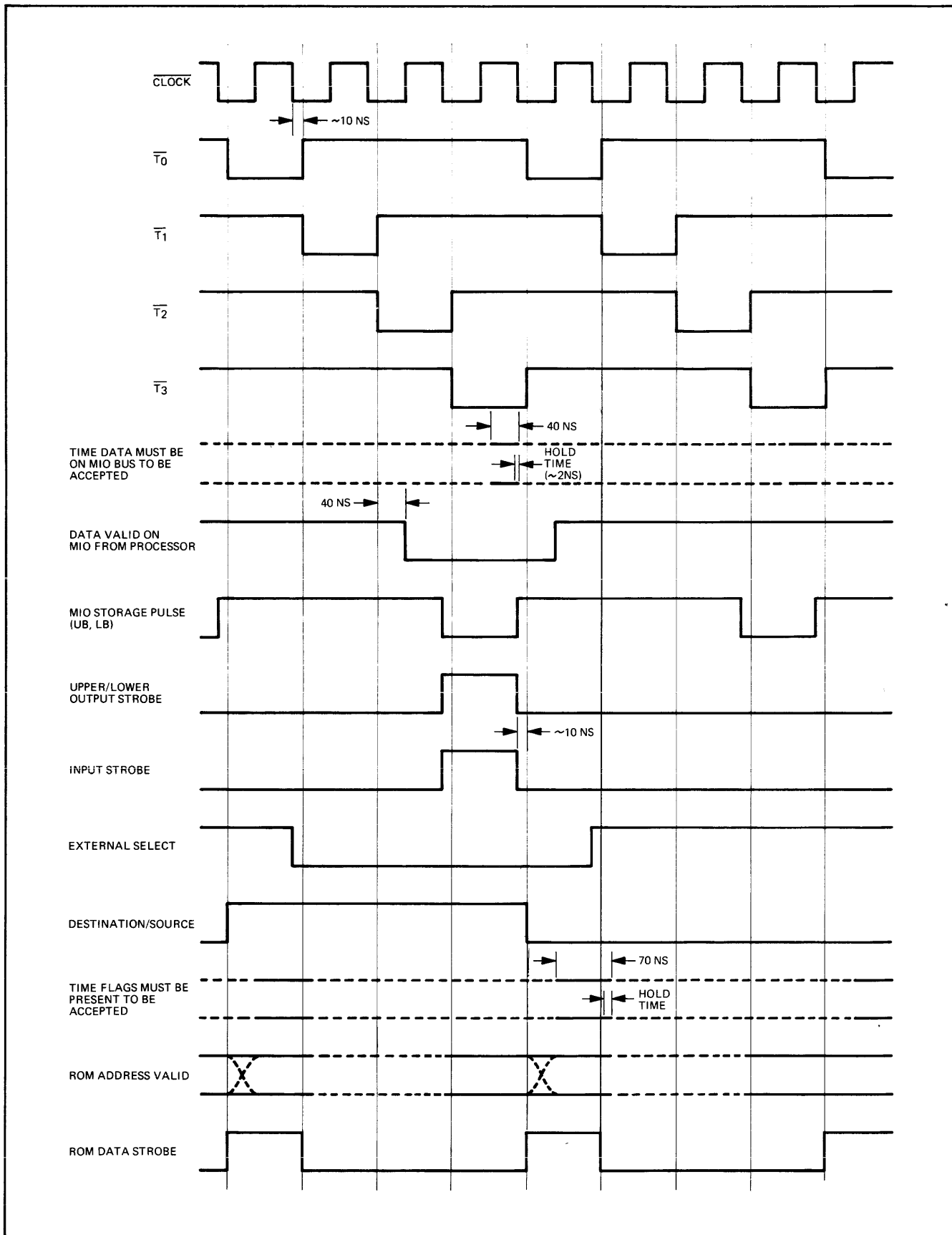


Figure 4-2. Magnetic Tape Subsystem, Example Multiple Tape Unit Cabling Diagram (Sheet 2 of 2)



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Figure 4-14. Controller Processor Basic Timing Diagram

Table 4-5. Controller Processor Maintenance Connector, J1, Pin/Signal List

J1 PIN	SIGNAL	J1 PIN	SIGNAL
1	COMMON	26	$\overline{\text{LB}}$
2	COMMON	27	AS 2
3	$\overline{\text{CLK RST}}$	28	AS 3
4	FLG SWRG*	29	AS 1
5	$\overline{\text{ALTCK}}$	30	AS 0
6	$\overline{\text{DISP}}$	31	V
7	$\overline{\text{CKCTL}}$	32	W
8	$\overline{\text{PANEL RESET}}$ *	33	T
9	ERA 7	34	U
10	—	35	ERA 1
11	$\overline{\text{LD ERA}}$	36	—
12	ERA 11	37	ERA 5
13	ERA 3	38	ERA 9
14	ERA 2	39	ERA 4
15	ERA 10	40	ERA 0
16	ERA 6	41	ERA 8
17	AT 0	42	—
18	CTL1	43	$\overline{\text{SIM RUN}}$ *
19	AT 3	44	$\overline{\text{SIM HALT}}$ *
20	AT 1	45	Z
21	AT 2	46	$\overline{\text{LDRG}}$
22	—	47	X
23	CTL2	48	Y
24	$\overline{\text{UB}}$	49	COMMON
25	AM	50	COMMON

NOTE: * appears only on maintenance interface card or ROM simulator buffer card.

Table 4-6. Power Bus/IOP Connector, P1, Pin/Signal List

56-PIN	20-PIN*	SIGNAL	56-PIN	20-PIN*	SIGNAL
1		+5V	31*		-20V
2		+5V	32*		-20V
3		+5V	33*		-20V
4		+5V	34*		-20V
5*	2	PF WARN	35*		+20V
6*	1	ENTIMER	36*		+20V
7*	4	(SPARE)	37*		+20V
8*	3	(SPARE)	38*		+20V
9	6	PWR ON	39*		+20V
10	5	PWR ON COMMON	40*		+20V
11	8	IORESET	41*	12	HSREQ
12	7	IORESET COMMON	42*	11	HSREQ COMMON
13*	10	MCUCLKS	43		INTPOLL OUT COMMON
14*	9	MCUCLKS COMMON	44		INTPOLL OUT
15		COMMON	45*	14	(SPARE)
16		COMMON	46*	13	(SPARE) COMMON
17*		-5V	47		INTPOLL IN COMMON
18*		-5V	48		INTPOLL IN
19		COMMON	49	16	S _I
20		COMMON	50	15	S _I COMMON
21*		+15V	51*		DATAPOLL OUT COMMON
22*		+15V	52*		DATAPOLL OUT
23*		+15V	53	18	S _O
24*		+15V	54	17	S _O COMMON
25*		-15V	55*		DATAPOLL IN COMMON
26*		-15V	56*		DATAPOLL IN
27*		-15V		20	MSKRTRN
28*		-15V		19	MSKRTRN COMMON
29		COMMON			
30		COMMON			

*Indicates not used in subsystem. Twenty-pin connector is used from PCA module-to-PCA module.

Table 4-7. Multiplexer Channel Bus Connector, P2, Pin/Signal List

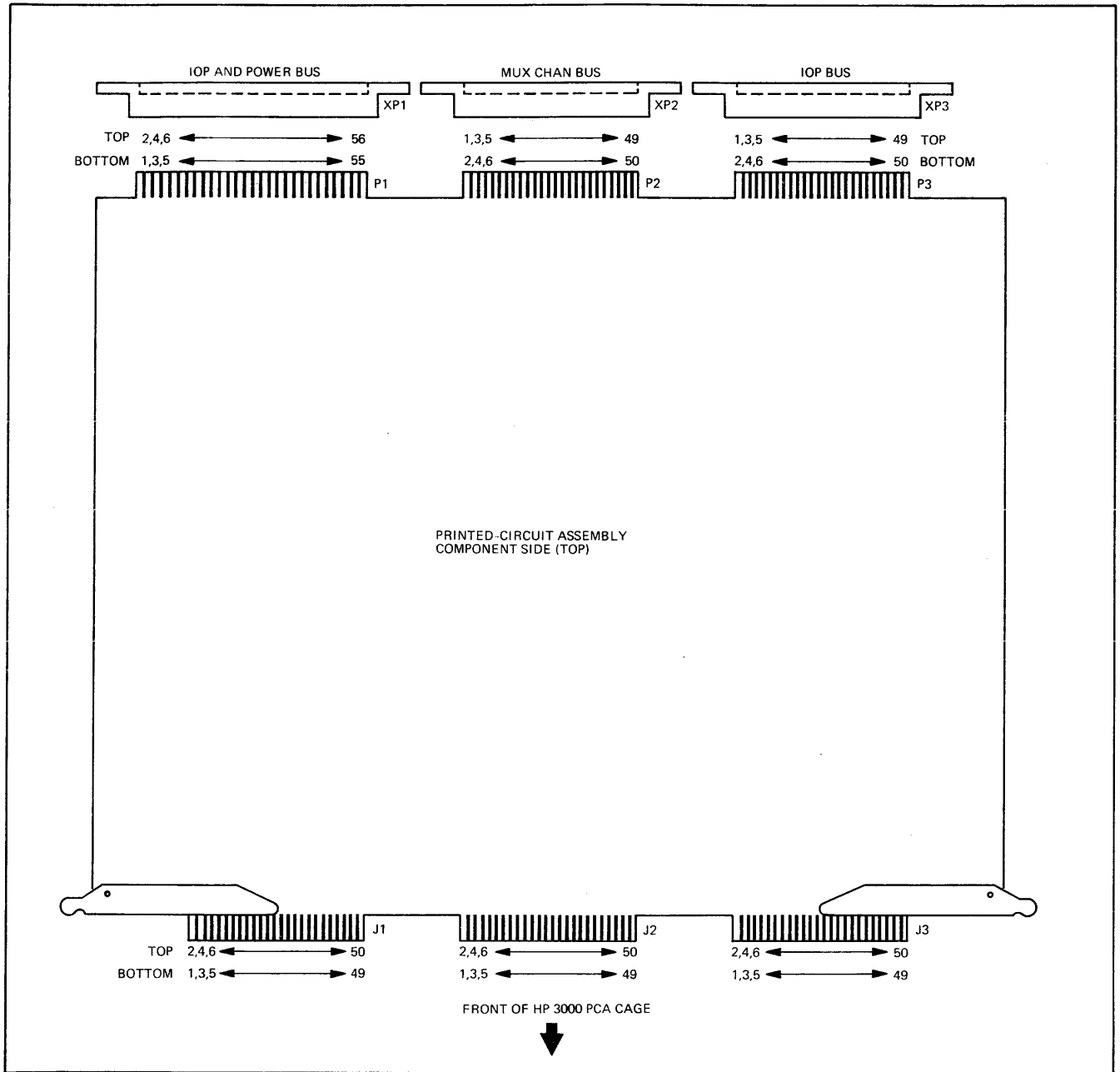
PIN	SIGNAL	PIN	SIGNAL
1	$\overline{\text{CHAN SO}}$	26	SR 13
2	COMMON	27	SR 12
3*	$\overline{\text{SR CLOCK}}$	28	SR 11
4	COMMON	29	SR 10
5	$\overline{\text{DEV END}}$	30	COMMON
6	COMMON	31	SR 9
7	$\overline{\text{ACK SR}}$	32	SR 8
8	COMMON	33	SR 7
9	$\overline{\text{CHAN ACK}}$	34	SR 6
10	COMMON	35	SR 5
11	$\overline{\text{DEVNO DB}}$	36	COMMON
12	$\overline{\text{SIO ENABLE}}$	37	SR 4
13	$\overline{\text{EOT}}$	38	SR 3
14*	$\overline{\text{JMP MET}}$	39	SR 2
15	COMMON	40	SR 1
16	TOGGLE INXFER	41	SR 0
17	$\overline{\text{TOGGLE SR}}$	42	COMMON
18	TOGGLE OUTXFER	43	$\overline{\text{P CMD 1}}$
19	TOGGLE SIO OK	44*	$\overline{\text{SET JMP}}$
20	COMMON	45	$\overline{\text{P STATUS STB}}$
21	$\overline{\text{XFER ERROR}}$	46	$\overline{\text{P CONT STB}}$
22	$\overline{\text{REQ}}$	47*	$\overline{\text{RD NEXT WD}}$
23	COMMON	48	$\overline{\text{P WRITE STB}}$
24	SR 15	49	$\overline{\text{SET INT}}$
25	SR 14	50	$\overline{\text{P READ STB}}$

*Indicates not used in subsystem.

Table 4-8. IOP Bus Connector, P3, Pin/Signal List

PIN	SIGNAL	PIN	SIGNAL
1	$\overline{\text{IODPRTY}}$	26	$\overline{\text{IOD 04}}$
2*	$\overline{\text{IOD PE}}$	27	$\overline{\text{IOD 05}}$
3	COMMON	28	COMMON
4	$\overline{\text{IOCMD 00}}$	29	$\overline{\text{IOD 06}}$
5	$\overline{\text{IOCMD 02}}$	30	$\overline{\text{IOD 07}}$
6	$\overline{\text{IOCMD 01}}$	31	COMMON
7	COMMON	32	$\overline{\text{IOD 08}}$
8	$\overline{\text{DEVNO 00}}$	33	$\overline{\text{IOD 09}}$
9	$\overline{\text{DEVNO 01}}$	34	COMMON
10	COMMON	35	$\overline{\text{IOD 10}}$
11	$\overline{\text{DEVNO 02}}$	36	$\overline{\text{IOD 11}}$
12	$\overline{\text{DEVNO 03}}$	37	COMMON
13	COMMON	38	$\overline{\text{IOD 12}}$
14	$\overline{\text{DEVNO 04}}$	39	$\overline{\text{IOD 13}}$
15	$\overline{\text{DEVNO 05}}$	40	COMMON
16	COMMON	41	$\overline{\text{IOD 14}}$
17	$\overline{\text{DEVNO 06}}$	42	$\overline{\text{IOD 15}}$
18	$\overline{\text{DEVNO 07}}$	43	COMMON
19	COMMON	44	$\overline{\text{INTREQ}}$
20	$\overline{\text{IOD 00}}$	45*	(SPARE)
21	$\overline{\text{IOD 01}}$	46	COMMON
22	COMMON	47*	(SPARE)
23	$\overline{\text{IOD 02}}$	48*	(SPARE)
24	$\overline{\text{IOD 03}}$	49	COMMON
25	COMMON	50	$\overline{\text{INTACK}}$

*Indicates not used in subsystem.



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Figure 4-15. Printed Circuit Assembly Connector Pin Indexing Diagram

4-42. CORRECTIVE MAINTENANCE.

4-43. Corrective maintenance for the subsystem consists of adjustment procedures and repair instructions for the tape unit and repair procedures for the HP 30215A Magnetic Tape Unit Interface. These items are discussed in the following paragraphs.

4-44. ADJUSTMENT PROCEDURES.

4-45. There are no adjustments to be made on the printed-circuit assemblies of the HP 30215A Magnetic Tape Unit Interface. Jumper connections are described in paragraph 4-19. All adjustments to be made on the tape unit are described in the operating and service manual for the applicable tape unit.

4-46. REPAIR PROCEDURES.

4-47. As previously mentioned, refer to the tape unit manual for repair instructions applicable to the tape transport and electronic assemblies in that unit, if it is found that they need repair. If trouble is isolated to a PCA or cable of the HP 30215A Magnetic Tape Unit Interface, refer to the following paragraphs.

4-48. **PRINTED-CIRCUIT ASSEMBLIES.** When trouble has been isolated to a component on a PCA of the interface, replace the component with an identical part number item using information in the *HP 3000 Computer System Illustrated Parts Breakdown Manual*. Integrated-circuit packs may be unsoldered from the PCA and replaced with a new part using a controlled heat, wide-tip soldering tool to unsolder all leads simultaneously. Replace other faulty components on the PCA's in a like manner. Refer to the following paragraph for interface and connector cable repair instructions.

4-49. **CABLE REPAIR.** Figures 4-16 and 4-17 illustrate signals and wiring for the tape controller-to-tape unit interface cable, part no. 30215-60003. Figures 4-18 and 4-19 are interface cable connector disassembly and repair illustrations. Figure 4-20 is a signal and pin diagram for connector cables, part no. 30000-93052, that are used between the PCA's of the HP 30215A Magnetic Tape Unit Interface. Refer to the illustrations and to the text in the following paragraphs for cable disassembly, repair, and connection data. The illustrations may also be used for troubleshooting since all signals and pins are listed from PCA-to-PCA or from PCA-to-tape unit for all plugs and jacks in the interface. The cabling information in the general servicing paragraph will also prove helpful for maintenance. Connector pin/signal lists for the controller processor maintenance connector, J1, and for PCA connectors P1 through P3 are provided in tables 4-5 through 4-8.

4-50. Connector P1 Repair. Figures 4-17 and 4-18 show details of interface cable 30215-60003 connector P1 wiring and repair. The procedure for wiring the 50-pin connector is as follows:

- a. Strip the outer jacket of each of the three cables back 3-½ inches (89 mm). Tag the cables to P2, P3, and P4 so that wires with the same color codes may be identified by connector destination.

- b. Trim wires to proper length and strip them back approximately $\frac{1}{4}$ inch (6 mm) as they are to be connected. See figure 4-17 for wire color connection sequence applicable to connector P1.
- c. Insert approximately 8 inches (203 mm) of cable into the P1 connector hood. Starting with the cables laid toward the cable entry point of the connector, attach and solder the white leads of the twisted pairs that will be attached to A2 through A7; to the 22 gauge bus wire. Install heat-shrink tubing as shown in figure 4-18 and attach the bus wire to A12. See the bus connection details in figure 4-18.
- d. Attach and solder the white leads of the twisted pairs that will be attached to B1 through B6; to the 22 gauge bus wire. Install heat-shrink tubing over leads as shown in figure 4-18 and attach the bus wire to B12 as shown in figure 4-18.
- e. Attach and solder the white leads of the twisted pairs that will be attached to A8 through A11; to the 22 gauge bus wire. Install heat-shrink tubing as shown in figure 4-18 and attach the bus wire to A13.
- f. Attach and solder the white leads of the twisted pairs that will be attached to B7 through B11; to the 22 gauge bus wire. Install heat-shrink tubing and attach the bus wire to B13.
- g. Follow the sequence established in steps c through f to attach all other white leads of twisted pairs to the bus wire and to the connector. The maximum is a group of six white wires. Be sure to see figures 4-17 and 4-18 for wiring details.
- h. See figure 4-17 and connect colored wires to the P1 connector. Observe tags installed in step a to ensure that proper P2, P3, or P4 connector is wired when duplicate colored wires are encountered. Insulate each connection with heat-shrink tubing as shown in figure 4-18.
- i. Install connector ends, hood, and clamps as shown in figure 4-18.

4-51. Connector P2, P3, P4 Repair. Figures 4-17 and 4-19 show details of interface cable 30215-60003 connector P2 through P4 wiring and repair. The procedure for wiring the 48-pin connectors is as follows:

- a. Insert approximately 10 inches (254 mm) of cable into the connector hood.
- b. Strip the outer jacket of the cable back 5 inches (127 mm).
- c. Fold back twisted pairs that will not be used. See figure 4-17 for applicable connector data.
- d. Cover cable and folded back twisted pairs with proper size heat-shrink tubing as shown in figure 4-19.
- e. Starting at the end of the 48-pin connector nearest pins BB and 24, connect the twisted pairs as follows:
 - (1) Strip the first pair of wires to be connected back approximately $\frac{1}{4}$ inch (6 mm). See figure 4-17 for wire color connection sequence applicable to connector being repaired.

- (2) Connect and solder the first pair of wires to their respective pins on the connector and insulate each pin with tubing as shown in figure 4-19. Note that the white wires in each pair connect to pins opposite their respective colored wire.
- f. Repeat steps (1) and (2) in the previous step with the remaining groups of wires until all wires are soldered to the connector and insulated. Follow the connection sequence in figure 4-17 for the connector being repaired.
- g. Install the wired 48-pin connector in the connector hood using the two self-tapping screws.
- h. Install the cable clamp and tighten it in place with the set screw.
- i. Insert keys, part no. 1251-1115, in connectors as follows:
 - (1) P2: between pins 18 and 19.
 - (2) P3: between pins 17 and 18.
 - (3) P4: between pins 5 and 6.
- j. First cable strap, part no. 1400-0249 is to be approximately 2 feet (61 cm) from the connector. Then installed clamps every 2 feet (61 cm).

4-52. Flat-Ribbon Cables. Figure 4-20 illustrates connecting cable 30000-93052 wiring and connectors as used between J2 of each PCA and between J3 of each PCA in the HP 30215A Magnetic Tape Unit Interface. The connectors on the flat-ribbon cables are fabricated to the cable when the system is configured. These cables cannot be disassembled. If it becomes necessary to repair the connector or cable, a new cable must be fabricated. Two special tools will be required to accomplish this. These are:

- a. The Scotchflex® Assembly Press manufactured by 3M Company, St. Paul, Minnesota. Used to press the Scotchflex® electronic connectors on to the 50-conductor flat-ribbon cable.
- b. The hand operated accessory cable shear. Used to trim excess flat-ribbon cable after fabricating the cables.

CAUTION

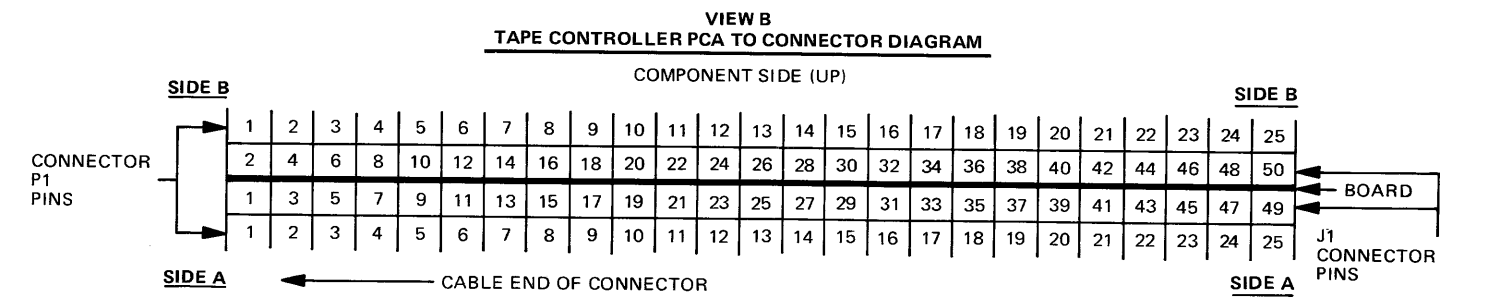
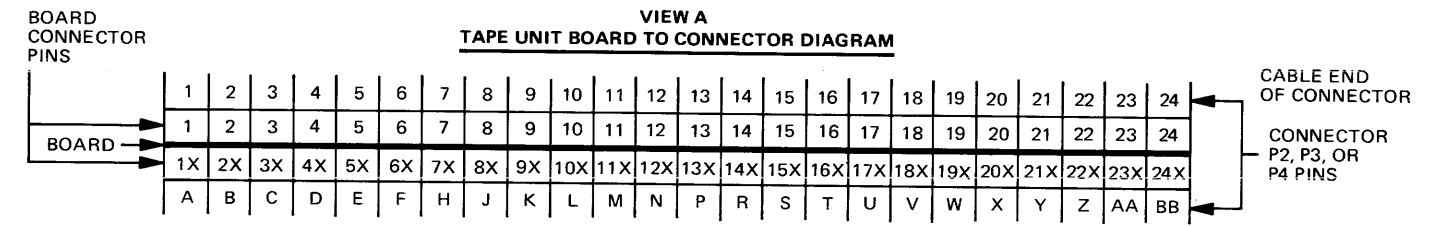
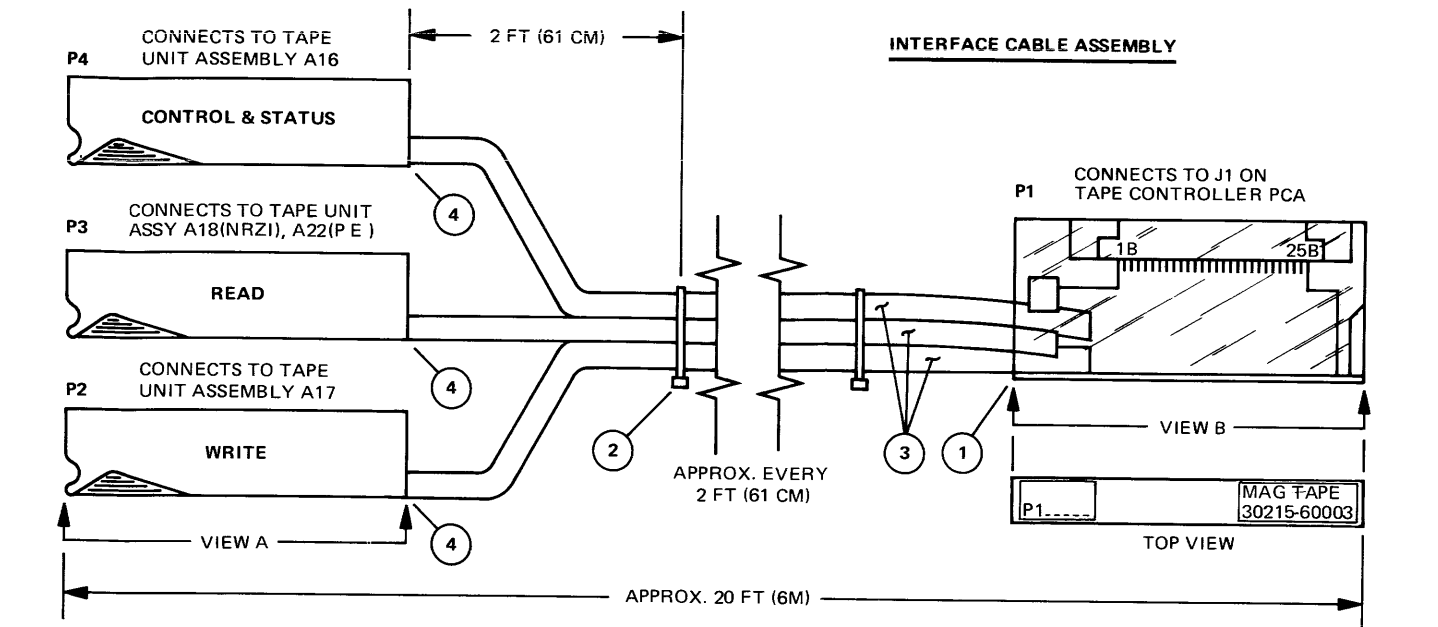
The use of cutting instruments such as a pocket knife, an X-Acto® knife, or other single-bladed device may exert force against the pins in the 50-pin connector, thus causing damage to the connector. Do not use these tools to cut flat-ribbon cable.

CONNECTOR PIN/SIGNAL LIST

TAPE CONTROLLER CARD		TAPE UNIT BOARD		SIGNAL	MNEMONIC (3)
J1-CARD PINS	P1-CONN. PINS(1)	P2-CONN. PINS(1)	WRITE BOARD PINS		
33/27	17A/14A	L/10	10X/10	WRITE DATA 0 (MSB)	WD0
34/27	17B/14A	M/11	11X/11	WRITE DATA 1	WD1
39/27	20A/14A	N/12	12X/12	WRITE DATA 2	WD2
40/27	20B/14A	P/13	13X/13	WRITE DATA 3	WD3
37/28	19A/14B	R/14	14X/14	WRITE DATA 4	WD4
38/28	19B/14B	S/15	15X/15	WRITE DATA 5	WD5
35/28	18A/14B	T/16	16X/16	WRITE DATA 6	WD6
36/28	18B/14B	U/17	17X/17	WRITE DATA 7 (LSB)	WD7
10/28	5B/14B	K/9	9X/9	WRITE DATA PARITY	WDP
11/28	6A/14B	F/6	6X/6	WRITE STATUS	SW
30/27	15B/14A	J/8	8X/8	WRITE CLOCK	WC
22/27	11B/14A	H/7	7X/7(5)	WRITE RESET	WRS

TAPE CONTROLLER CARD		TAPE UNIT BOARD		SIGNAL	MNEMONIC
J1-CARD PINS	P1-CONN. PINS(1)	P3-CONN. PINS(1)	READ BOARD PINS		
47/50	24A/25B	L/10	10X/10	READ DATA 0 (MSB)	RD0
48/50	24B/25B	M/11	11X/11	READ DATA 1	RD1
45/50	23A/25B	N/12	12X/12	READ DATA 2	RD2
46/50	23B/25B	P/13	13X/13	READ DATA 3	RD3
43/49	22A/25A	R/14	14X/14	READ DATA 4	RD4
44/49	22B/25A	S/15	15X/15	READ DATA 5	RD5
41/49	21A/25A	T/16	16X/16	READ DATA 6	RD6
42/49	21B/25A	U/17	17X/17	READ DATA 7 (LSB)	RD7
9/25	5A/13A	K/9	9X/9	READ DATA PARITY	RDP
8/23	4B/12A	J/8	8X/8	READ CLOCK	RC
7/23	4A/12A	BB/24	24X/24 (2)	END-OF-BLOCK	EOB
12/26	6B/13B	V/18	18X/18 (2)	800/1600 CPI STATUS (4)	SD16
31/26	16A/13B	X/20	20X/20 (2)	MULTIPLE TRACK ERROR	MTE
32/26	16B/13B	Y/21	21X/21 (2)	TAPE MARK	TM
29/26	15A/13B	AA/23	23X/23 (2)	IDENTIFICATION BURST	IDB
2/26	1B/13B	Z/22	22X/22 (2)	SINGLE TRACK ERROR	STE

TAPE CONTROLLER CARD		TAPE UNIT BOARD		SIGNAL	MNEMONIC
J1-CARD PINS	P1-CONN. PINS(1)	P4-CONN. PINS(1)	MOTION CONTROL BOARD PINS		
3/23	2A/12A	P/13	13X/13	SELECT UNIT 0	CS0
4/23	2B/12A	N/12	12X/12	SELECT UNIT 1	CS1
5/24	3A/12B	M/11	11X/11	SELECT UNIT 2	CS2
6/24	3B/12B	L/10	10X/10	SELECT UNIT 3	CS3
13/23	7A/12A	B/2	2X/2	LOAD POINT STATUS	SLP
16/23	8B/12A	D/4	4X/4	END-OF-TAPE STATUS	SET
14/24	7B/12B	E/5	5X/5	READY STATUS	SR
15/24	8A/12B	F/6	6X/6	FILE PROTECT STATUS	SFP
17/24	9A/12B	T/16	16X/16	FORWARD COMMAND	CF
21/24	11A/12B	R/14	14X/14	REWIND COMMAND	CRW
18/25	9B/13A	U/17	17X/17	REVERSE COMMAND	CR
20/25	10B/13A	S/15	15X/15	OFF-LINE COMMAND	CL
19/25	10A/13A	W/19	19X/19	SET WRITE COMMAND	WSW

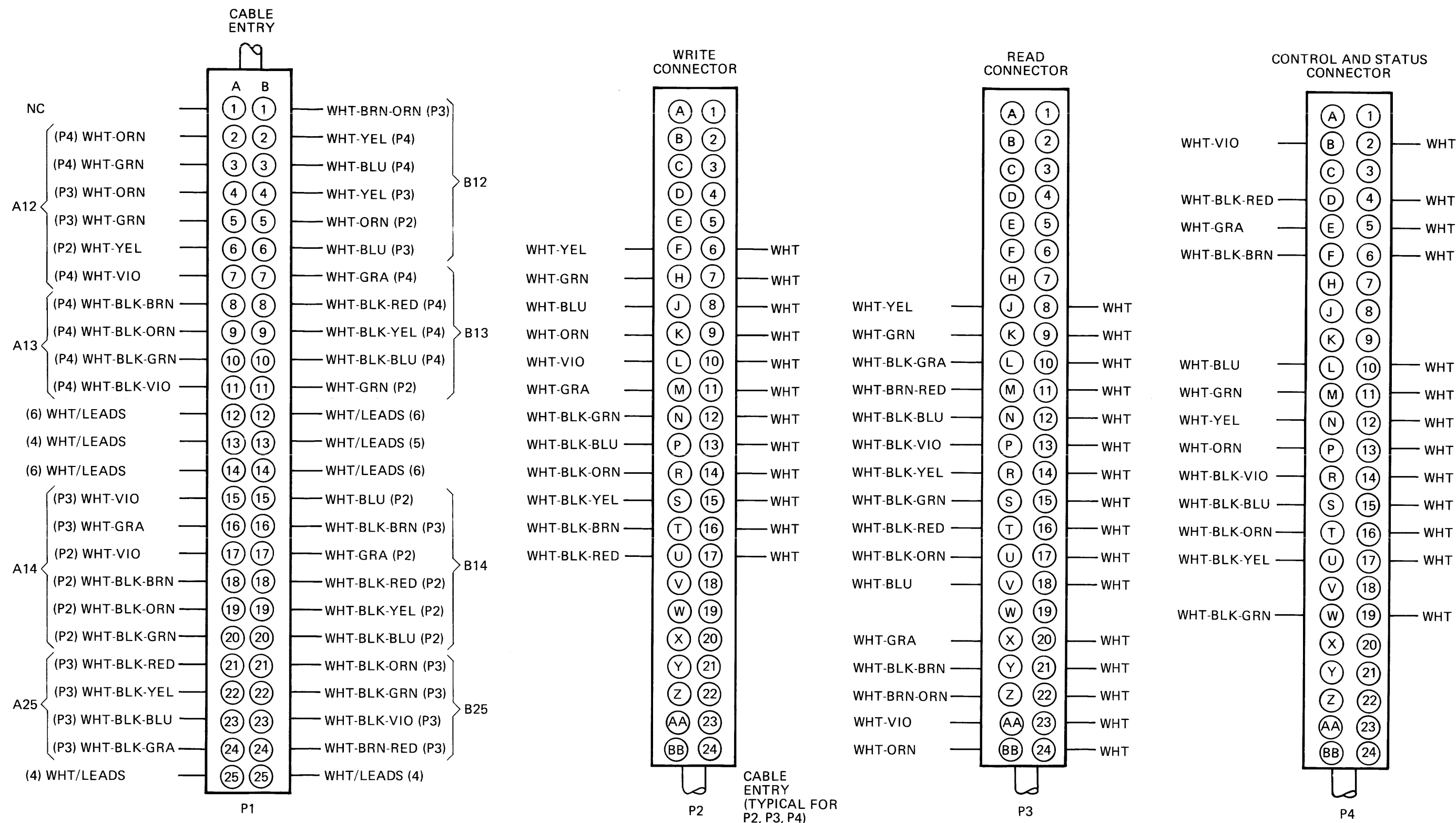


CABLE 30215-60003 PARTS

ITEM	QUANTITY	DESCRIPTION	PART NO.
1	1	50-PIN, P.C. KIT CONN. (6)	5060-8326
2	10	CABLE STRAP	1400-0249
3	60 FT (18M)	CABLE, 3-20 FT (6M) LENGTHS	8120-1863
4	3	48-PIN, P.C. CONNECTOR (7)	1251-2518

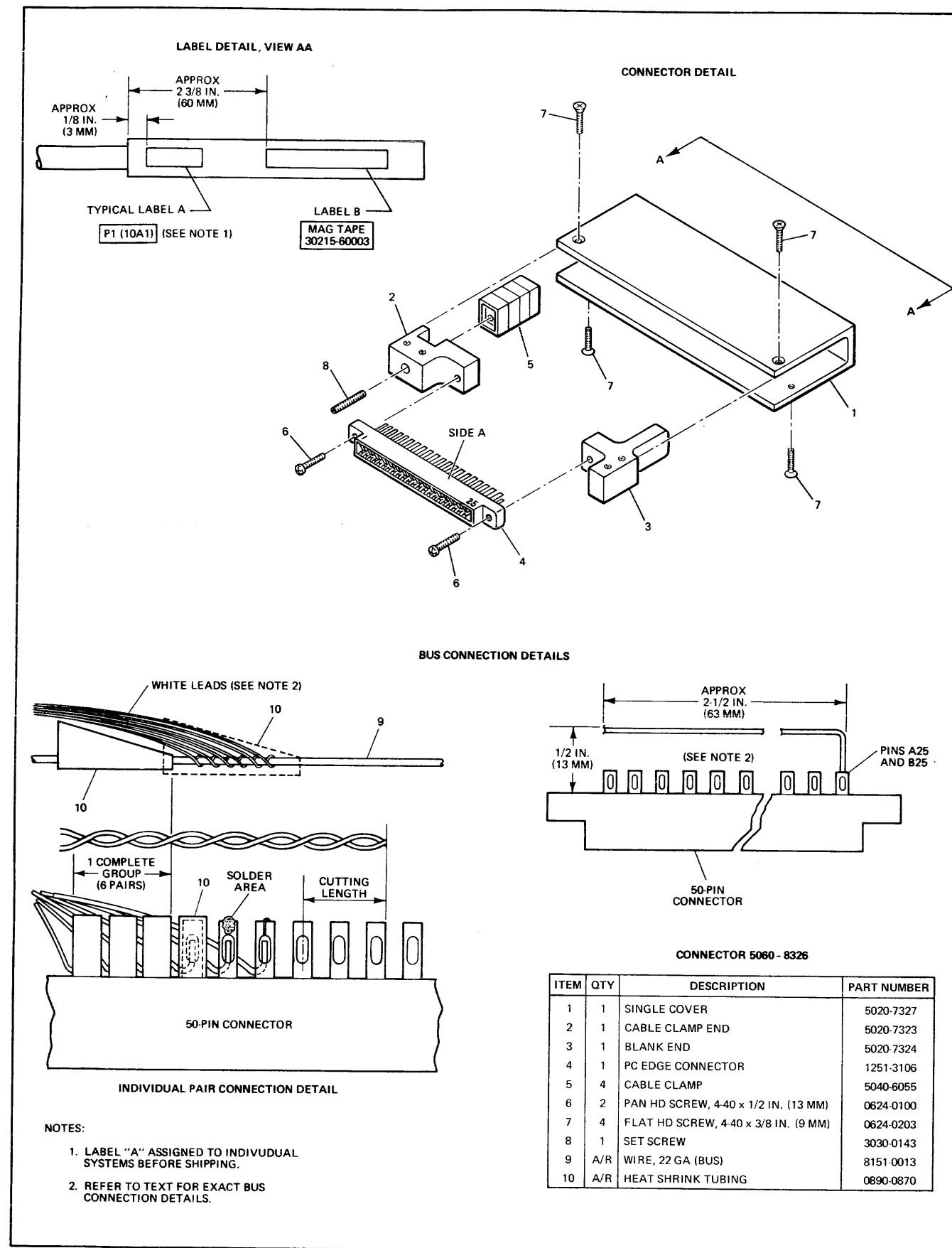
- NOTES:
1. CABLE COMPOSED OF TWISTED PAIRS. PIN CONNECTIONS DESIGNATED: SIGNAL LEAD/COMMON LEAD.
 2. SIGNALS NOT USED IN NINE TRACK NRZI UNITS.
 3. ALL SIGNALS GO LOW TO INDICATE CONDITION NAMED.
 4. 800 CPI IS NRZI, 1600 CPI IS PHASE ENCODED (PE) TAPE.
 5. SIGNAL NOT USED IN NINE TRACK PE UNITS.
 6. SEE CONNECTOR DISASSEMBLY DIAGRAM FOR DETAILS.
 7. ONLY THE CONNECTOR PART NUMBER IS LISTED. SEE CONNECTOR DISASSEMBLY DIAGRAM FOR COMPLETE DETAILS.

Figure 4-16. Interface Cable, Tape Controller-to-Tape Unit



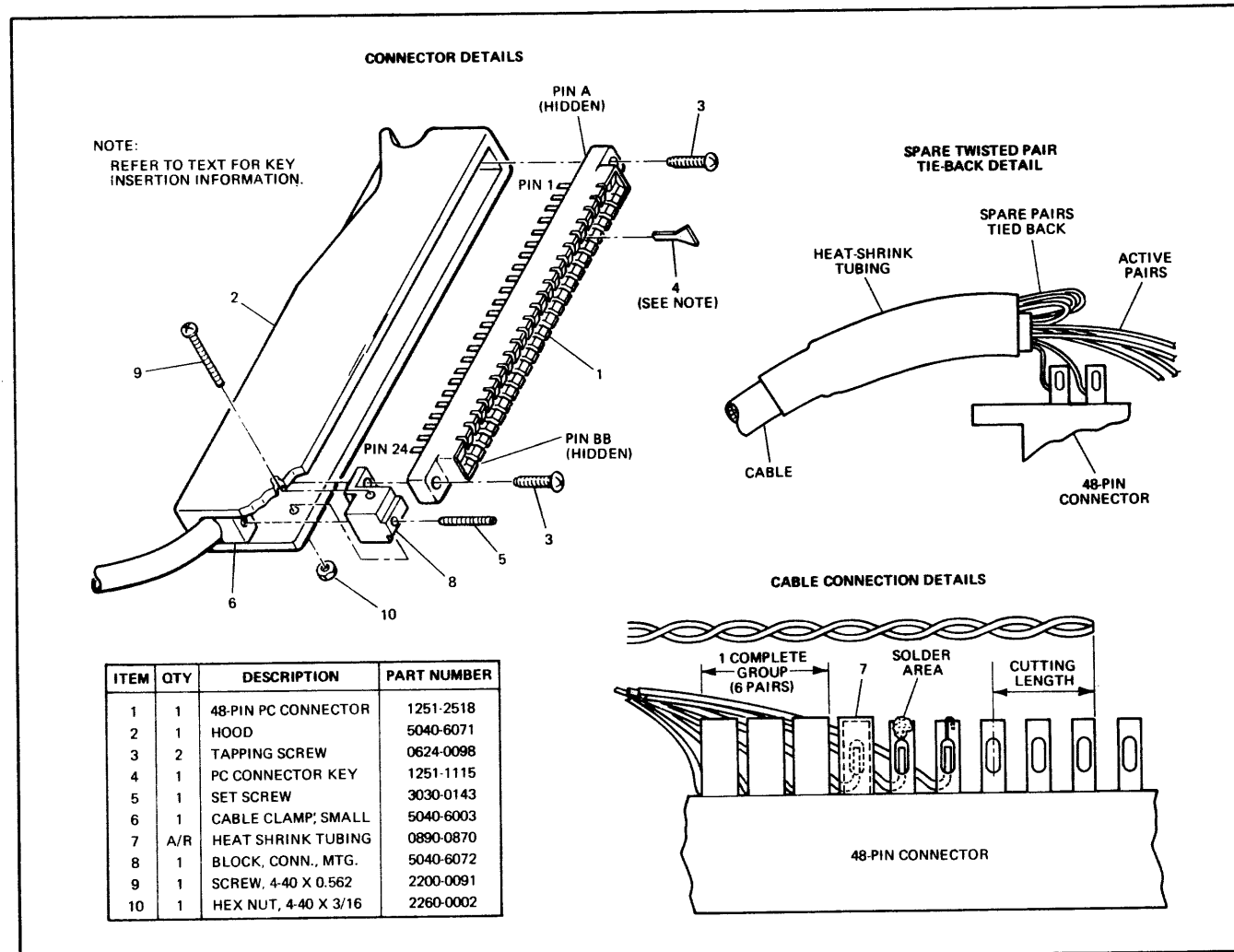
NOTE: PIN NUMBERS INDICATED BY BRACES ARE COMMON LEAD CONNECTIONS TO PIN INDICATED (SEE TEXT).

Figure 4-17. Interface Cable Connector Wiring



2180-33A

Figure 4-18. Interface Cable Connector P1, Disassembly and Repair Diagram



2180-34A

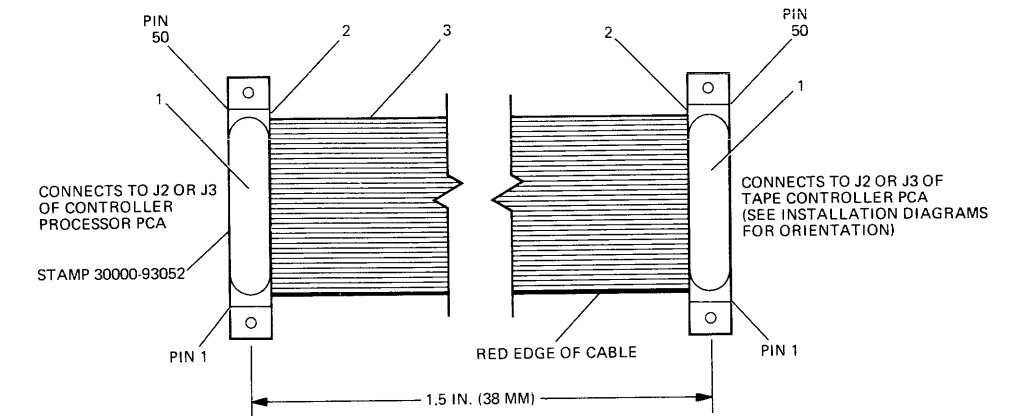
Figure 4-19. Interface Cable Connectors P2 through P4 Disassembly and Repair Diagram

CONNECTOR PIN/SIGNAL LIST
CONTROLLER PROCESSOR-TO-TAPE CONTROLLER

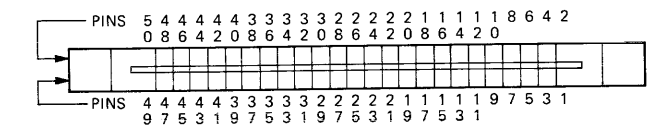
J2-TO-J2, ROM DATA			J3-TO-J3 CONTROL AND DATA		
J2 ⁽¹⁾ PIN	SIGNAL	MNEMONIC	J3 ⁽¹⁾ PIN	SIGNAL	MNEMONIC
1	COMMON	—	1	COMMON	—
2	COMMON	—	2	CLEAR	CLR
3	ROM OUTPUT BIT 4	ROM 4	3 ⁽²⁾	CLOCK PHASE 0	T0
4	BLANK	—	4 ⁽²⁾	CLOCK PHASE 3	T3
5	ROM OUTPUT BIT 5	ROM 5	5 ⁽²⁾	CLOCK PHASE 2	T2
6	BLANK	—	6	DESTINATION BIT 9	ROR 9
7	ROM OUTPUT BIT 6	ROM 6	7	UPPER OUTPUT STROBE	UOS
8	BLANK	—	8	INPUT STROBE	IS
9	ROM OUTPUT BIT 7	ROM 7	9	READ CLOCK	F10 ⁽³⁾
10	BLANK	—	10	LOWER OUTPUT STROBE	LOS
11	ROM OUTPUT BIT 8	ROM 8	11	DATA FF	F14 ⁽³⁾
12	BLANK	—	12	OUT XFER	F12 ⁽³⁾
13	ROM OUTPUT BIT 9	ROM 9	13	IN XFER	F16 ⁽³⁾
14	BLANK	—	14	INTERRUPT CONDITION	F15 ⁽³⁾
15	ROM OUTPUT BIT 10	ROM 10	15	DESTINATION BIT 8	ROR 8
16	BLANK	—	16	COMMAND ENABLE ⁽⁴⁾	F17 ⁽³⁾
17	ROM OUTPUT BIT 11	ROM 11	17	(LSB) DESTINATION BIT 11	ROR 11
18	BLANK	—	18	DESTINATION BIT 7 (MSB)	ROR 7
19	ROM OUTPUT BIT 12	ROM 12	19 ⁽²⁾	WORD TYPE ONE	WT1
20	BLANK	—	20	DESTINATION BIT 10	ROR 10
21	ROM OUTPUT BIT 13	ROM 13	21	READY STATUS	F13 ⁽³⁾
22	BLANK	—	22	TAPE ERROR ⁽⁴⁾	F11 ⁽³⁾
23	ROM OUTPUT BIT 14	ROM 14	23	READ/WRITE PARITY ⁽⁵⁾	F06 ⁽³⁾
24	BLANK	—	24	END OF BLOCK FF ⁽⁶⁾	F07 ⁽³⁾
25	ROM OUTPUT BIT 15	ROM 15	25	800/1600 ⁽⁷⁾	F04 ⁽³⁾
26	BLANK	—	26	WRITE STATUS	F05 ⁽³⁾
27	ROM OUTPUT BIT 16	ROM 16	27	FLAG 2	F02 ⁽³⁾
28	ROM OUTPUT BIT 0 (MSB)	ROM 0	28	LOAD POINT (BOT)	F03 ⁽³⁾
29	ROM OUTPUT BIT 17	ROM 17	29	FLAG 0	F00 ⁽³⁾
30	ROM OUTPUT BIT 1	ROM 1	30	FLAG 1	F01 ⁽³⁾
31	ROM OUTPUT BIT 18	ROM 18	31	MIO BUS BIT 12	M12
32	ROM OUTPUT BIT 2	ROM 2	32 ⁽²⁾	EXTERNAL SELECT	EXT SEL
33	ROM OUTPUT BIT 19 (LSB)	ROM 19	33	MIO BUS BIT 13	M13
34	ROM OUTPUT BIT 3	ROM 3	34	MIO BUS BIT 11	M11
35	BLANK	—	35	MIO BUS BIT 14	M14
36	ROM ENABLE	ENB	36	MIO BUS BIT 10	M10
37 ⁽²⁾	ROM ADDRESS BIT 0 (MSB)	RAR 0	37	MIO BUS BIT 15 (LSB)	M15
38 ⁽²⁾	ROM ADDRESS BIT 1	RAR 1	38	MIO BUS BIT 9	M9
39	ROM ADDRESS BIT 2	RAR 2	39 ⁽²⁾	CLOCK PHASE 1	T1
40	ROM ADDRESS BIT 3	RAR 3	40	MIO BUS BIT 8	M8
41	ROM ADDRESS BIT 4	RAR 4	41	MIO BUS BIT 3	M3
42	ROM ADDRESS BIT 5	RAR 5	42	MIO BUS BIT 4	M4
43	ROM ADDRESS BIT 6	RAR 6	43	MIO BUS BIT 2	M2
44	ROM ADDRESS BIT 7	RAR 7	44	MIO BUS BIT 5	M5
45	ROM ADDRESS BIT 8	RAR 8	45	MIO BUS BIT 1	M1
46	ROM ADDRESS BIT 9	RAR 9	46	MIO BUS BIT 6	M6
47	ROM ADDRESS BIT 10	RAR 10	47	MIO BUS BIT 0	M0
48	ROM ADDRESS BIT 11 (LSB)	RAR 11	48	MIO BUS BIT 7	M8
49	COMMON	—	49 ⁽²⁾	FROM MAINT. PANEL	RUN
50	COMMON	—	50	COMMON	—

2180-30

CONNECTOR CABLE ASSEMBLY



CONNECTOR DIAGRAM



CABLE 30000-93052 PARTS

ITEM	QUANTITY	DESCRIPTION	PART NO.
1	2	PLASTIC HANDLE	5040-6059
2	2	50 PIN PC CONN. WITH MTG. EARS	1251-2755
3	1.5 IN. (38 MM)	CABLE FLAT RIBBON	8120-1595

NOTES:

- CONNECTOR PIN NUMBERS ON PRINTED-CIRCUIT ASSEMBLIES MATCH CONNECTOR CABLE PIN NUMBERS AT BOTH ENDS.
- INDICATES SIGNAL NOT USED IN SUBSYSTEM OPERATION.
- LETTER "F" IN MNEMONIC INDICATES CONTROLLER PROCESSOR PCA FLAG INPUT.
- REVERSE SENSE; SIGNAL GOES LOW TO INDICATE CONDITION.
- REVERSE SENSE (LOW SIGNAL) FOR WRITE PARITY.
- USED IN 1600 CPI ONLY.
- LOW INDICATES 800 CPI.

Figure 4-20. Connector Cable, Tape Controller-to-Controller Processor ROM and Control and Data