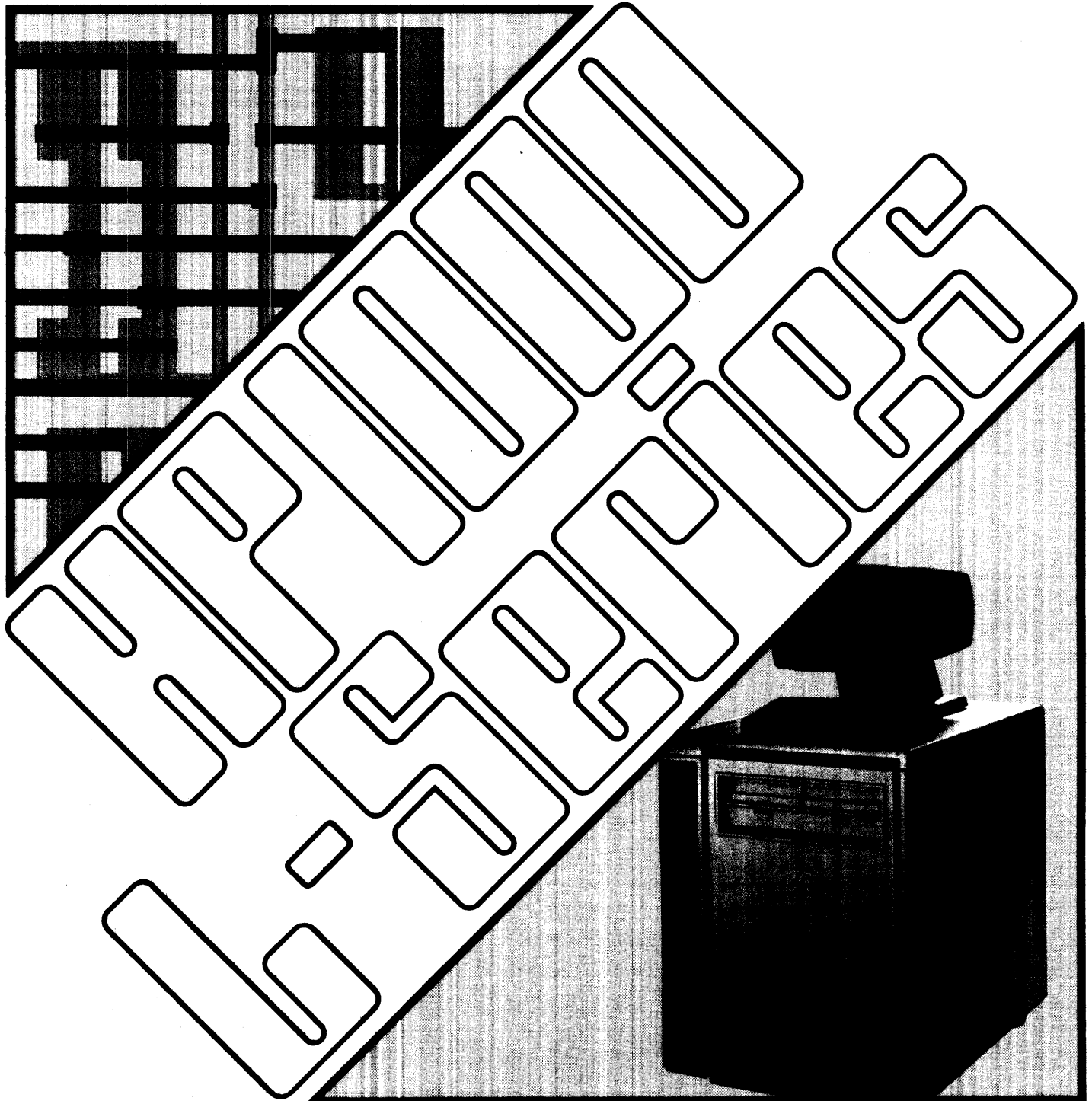


HP 1000 L-Series Computer

Engineering and Reference Documentation



HP 1000 L-SERIES COMPUTER ENGINEERING AND REFERENCE DOCUMENTATION



HEWLETT-PACKARD COMPANY
Data Systems Division
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Cupertino, California 95014

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PRINTING HISTORY

New editions are complete revisions of the manual. Update packages contain replacement pages or write-in instructions to be merged into the manual by the customer. Manuals will be reprinted as necessary to incorporate all prior updates. A reprinted manual is identical in content (but not in appearance) to the previous edition with all updates incorporated. No information is incorporated into a reprinting unless it appears as a prior update. The edition does not change.

First Edition Sep 1980

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SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS



Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.



Indicates hazardous voltages.



Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The **WARNING** sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a **WARNING** sign until the indicated conditions are fully understood and met.

CAUTION

The **CAUTION** sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a **CAUTION** sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous ways such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing static sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling the devices. Cautions are included through this manual where handling and maintenance involve static sensitive devices.

SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

NOTICE

Many of the schematic diagrams and parts lists in this document contain the generic number of IC packs. These are for your convenience in referring to pack diagrams and general operating conditions in semiconductor manufacturer's catalogs. The generic number, however, should not be used to order replacement parts. Many parts used in Hewlett-Packard equipment are purchased with special specifications and tolerances, or may undergo special testing and treatment (such as burn-in). Replacement parts therefore must be ordered using the Hewlett-Packard part number to insure that the replacement part will restore the equipment to its proper operating condition.

PREFACE

This document contains engineering and reference information for the Hewlett-Packard HP 1000 L-Series Computer.

The L-Series computer hardware is available as printed circuit cards, computer units (boxes containing several printed circuit cards), and computer systems (boxes containing several printed circuit cards plus peripheral devices). This document is intended to assist you in arranging any of the L-Series combinations into unique, special-purpose computing systems.

Information is provided for the processor card, memory, power supply, battery backup, and backplane. The input/output (I/O) interfaces (Parallel Interface, Asynchronous Serial Interface, etc.) are not covered in this document; information concerning these items is provided in separate manuals. See the HP 1000 Computer Reference Manual, part number 02103-90007, for a documentation map of all available L-Series manuals.

The content of this document is as follows:

- Section I - HP 1000 L-Series Computer
- Section II - Processor Card
- Section III - 64Kbyte Memory
- Section IV - Power Supply
- Section V - Battery Backup
- Section VI - Backplane
- Section VII - Point-of-Load Regulator
- Section VIII - Expanded Memory
- Appendix A - Self-Test, Loaders, and VCP Programs
- Appendix B - Application Information for 25 KHz Power
- Cross-Reference Index

PREFACE

Section I contains information covering the HP 1000 L-Series computer at the system level, the box level, and the card (printed circuit) level.

In addition, power, ventilation, and assembly information are provided for those customers who wish to purchase and assemble individual cards into unique, special-purpose systems.

The remaining sections contain specifications, theory of operation information, parts list, and parts location information. Block diagrams, schematic diagrams, and parts location diagrams are provided. Additional diagrams, such as photographs of each card or assembly, are provided as necessary.

Table of Contents

- 1 HP 1000 L-SERIES COMPUTER
 - 1.1 INTRODUCTION 1-1
 - 1.2 PHYSICAL DESCRIPTION 1-1
 - 1.3 ELECTRICAL DESCRIPTION 1-1
 - 1.4 SYSTEM SUPPORT FEATURES 1-5
 - 1.4.1 VIRTUAL CONTROL PANEL 1-5
 - 1.4.2 SELF-TEST CAPABILITY 1-6
 - 1.5 L-SERIES CARDS 1-7
 - 1.5.1 POWER REQUIREMENTS 1-7
 - 1.5.2 VENTILATION REQUIREMENTS 1-8
 - 1.5.3 CARD CAGE AND BACKPLANE ASSEMBLIES 1-8

- 2 PROCESSOR CARD
 - 2.1 INTRODUCTON 2-1
 - 2.2 OVERVIEW 2-1
 - 2.2.1 SYSTEM ENVIROMENT 2-3
 - 2.3 PROCESSOR CARD FUNCTIONAL THEORY OF OPERATION 2-3
 - 2.3.1 MEMORY ACCESSING 2-3
 - 2.3.2 INTERRUPT PROCESSING 2-6
 - 2.3.2.1 Interrupt Requests 2-6
 - 2.3.2.2 Interrupt Service 2-9
 - 2.3.3 I/O PROCESSING 2-11
 - 2.3.3.1 I/O Accessing 2-11
 - 2.3.3.2 Processor Card I/O Functions 2-12
 - 2.4 CPU CHIP FUNCTIONAL THEORY OF OPERATION 2-17
 - 2.4.1 CPU CHIP DATA PATHS 2-21
 - 2.4.2 CPU CHIP REGISTERS 2-23
 - 2.4.2.1 Instruction Register 2-23
 - 2.4.2.2 Page Register 2-23
 - 2.4.2.3 Control Word Register 2-25
 - 2.4.2.4 A and B Registers 2-25
 - 2.4.2.5 Extend (E) Register 2-26
 - 2.4.2.6 Overflow (O) Register 2-26
 - 2.4.2.7 T Register 2-26
 - 2.4.2.8 P Register 2-26
 - 2.4.2.9 PSAVE Register 2-27
 - 2.4.2.10 Memory Protect Fence Register 2-27
 - 2.4.3 ARITHMETIC LOGIC UNIT 2-28
 - 2.4.4 STATUS LOGIC 2-28
 - 2.4.5 CONTROL STRUCTURE 2-30
 - 2.4.6 NEXT STATE CLA 2-30
 - 2.4.7 NEXT STATE COUNTER/REGISTER 2-30
 - 2.4.8 OUTPUT CLA/OUTPUT CLA LATCHES 2-30
 - 2.4.9 INSTRUCTION REGISTER CLA 2-32
 - 2.4.10 CPU TIMING 2-32
 - 2.4.11 STATE DIAGRAM 2-33
 - 2.4.12 MEMORY PROTECT SYSTEM 2-42

| | | |
|---------|---|------|
| 2.5 | PROCESSOR CARD DETAILED THEORY OF OPERATION | 2-44 |
| 2.5.1 | MEMORY ACCESSING | 2-44 |
| 2.5.1.1 | Memory Data Read | 2-46 |
| 2.5.1.2 | Memory Write Initiated by the Processor Card | 2-46 |
| 2.5.1.3 | Instruction Fetch from Memory | 2-46 |
| 2.5.1.4 | Instruction Fetch from the A or B Registers | 2-46 |
| 2.5.1.5 | ROM Data Read | 2-49 |
| 2.5.1.6 | Instruction Fetch from ROM | 2-49 |
| 2.5.2 | PROCESSOR MEMORY ACCESS AND DMA | 2-49 |
| 2.5.3 | I/O STATE MACHINE | 2-51 |
| 2.5.4 | VIRTUAL CONTROL PANEL (SLAVE MODE) PROCESSING | 2-61 |
| 2.5.5 | POWER ON SELF-TEST AND BOOT LOADERS | 2-62 |
| 2.5.6 | L-SERIES CLOCKS | 2-63 |
| 2.6 | PARTS LOCATIONS | 2-65 |
| 2.7 | PARTS LIST | 2-65 |
| 3 | 64K BYTE MEMORY | |
| 3.1 | INTRODUCTION | 3-1 |
| 3.2 | OVERVIEW | 3-1 |
| 3.2.1 | SYSTEM ENVIRONMENT | 3-1 |
| 3.2.2 | BASIC MEMORY OPERATION | 3-3 |
| 3.2.2.1 | Write Cycle | 3-3 |
| 3.2.2.2 | Read Cycle | 3-5 |
| 3.2.2.3 | Refresh Cycle | 3-5 |
| 3.3 | SPECIFICATIONS | 3-7 |
| 3.3.1 | POWER REQUIREMENTS | 3-7 |
| 3.3.2 | MEMORY CYCLE TIME | 3-7 |
| 3.3.3 | MEMORY REFRESH PERIOD | 3-7 |
| 3.3.4 | DATA/ADDRESS LATCHES | 3-8 |
| 3.3.5 | PARITY GENERATION/DETECTION | 3-8 |
| 3.3.6 | PARITY SENSE | 3-9 |
| 3.3.7 | PARITY INDICATOR | 3-9 |
| 3.3.8 | STANDBY MODE | 3-10 |
| 3.3.9 | POWER SUPPLY CONFIGURATION | 3-10 |
| 3.4 | INTERFACE REQUIREMENTS | 3-11 |
| 3.4.1 | BACKPLANE INTERFACE | 3-11 |
| 3.4.1.1 | Main Handshake Signals | 3-11 |
| 3.4.1.2 | Handshake Inhibit Signals | 3-12 |
| 3.4.1.3 | Clock Signals | 3-12 |
| 3.4.1.4 | Initialization Signals | 3-15 |
| 3.4.1.5 | Power Sequencing Requirement | 3-15 |
| 3.5 | OPERATING CHARACTERISTICS | 3-15 |
| 3.5.1 | INITIALIZATION | 3-15 |
| 3.5.2 | INPUT DATA/ADDRESS SET-UP REQUIREMENT | 3-15 |
| 3.5.3 | WRITING DATA INTO MEMORY | 3-17 |
| 3.5.4 | READING DATA FROM MEMORY | 3-17 |
| 3.5.5 | RECOVERY FROM PARITY ERRORS | 3-18 |
| 3.6 | FUNCTIONAL THEORY OF OPERATION | 3-18 |
| 3.6.1 | INTERFACE BUFFERS | 3-18 |
| 3.6.2 | ADDRESS LATCH | 3-18 |
| 3.6.3 | DATA-IN LATCH | 3-20 |

| | | |
|---------|---|------|
| 3.6.4 | DATA-OUT BUFFER | 3-20 |
| 3.6.5 | PARITY GENERATOR/COMPARATOR | 3-20 |
| 3.6.6 | PARITY CONTROL | 3-20 |
| 3.6.7 | PARITY INDICATOR | 3-20 |
| 3.6.8 | ADDRESS MULTIPLEXER | 3-21 |
| 3.6.9 | DYNAMIC RAM ARRAY | 3-21 |
| 3.6.10 | TIMING AND CONTROL | 3-21 |
| 3.6.11 | REFRESH CONTROL | 3-21 |
| 3.7 | THEORY OF OPERATION | 3-22 |
| 3.7.1 | INTERFACE BUFFERS | 3-22 |
| 3.7.2 | ADDRESS LATCH | 3-22 |
| 3.7.3 | DATA-IN LATCH | 3-24 |
| 3.7.4 | DATA-OUT BUFFER | 3-24 |
| 3.7.5 | PARITY CIRCUIT | 3-25 |
| 3.7.5.1 | Parity Generation | 3-25 |
| 3.7.5.2 | Parity Detection | 3-26 |
| 3.7.6 | ADDRESS MULTIPLEXER | 3-27 |
| 3.7.7 | DYNAMIC RAM ARRAY | 3-28 |
| 3.7.8 | MEMORY REFRESH CIRCUIT | 3-29 |
| 3.7.9 | MAIN CONTROL CIRCUIT | 3-30 |
| 3.7.10 | MEMORY CYCLE SEQUENCE | 3-31 |
| 3.7.11 | MEMORY CYCLES OCCURRING DURING REFRESH CYCLES | 3-32 |
| 3.7.12 | REFRESH CYCLES OCCURRING DURING MEMORY CYCLES | 3-32 |
| 3.7.13 | PON INITIALIZATION | 3-35 |
| 3.7.14 | TEST POINTS AND DIAGNOSTIC FUNCTIONS | 3-35 |
| 3.8 | PARTS LOCATIONS | 3-36 |
| 3.9 | PARTS LIST | 3-36 |
| 4 | POWER SUPPLY | |
| 4.1 | INTRODUCTION | 4-1 |
| 4.2 | PHYSICAL CHARACTERISTICS | 4-1 |
| 4.2.1 | INPUT POWER CONNECTOR | 4-1 |
| 4.2.2 | BACKPLANE INTERFACE OUTPUT CONNECTOR | 4-3 |
| 4.2.3 | SINGLE-PHASE 25KHZ OUTPUT CONNECTOR | 4-3 |
| 4.2.4 | POWER CONTROL CONNECTOR | 4-4 |
| 4.2.5 | EXTERNAL FAN CONNECTOR | 4-4 |
| 4.2.6 | INDICATORS | 4-4 |
| 4.3 | SPECIFICATIONS | 4-5 |
| 4.4 | BINARY SIGNAL LEVELS | 4-10 |
| 4.5 | THEORY OF OPERATION | 4-11 |
| 4.5.1 | MOTHERBOARD (PART NUMBER 12035-60002) | 4-11 |
| 4.5.1.1 | Low Voltage Driver Supply | 4-11 |
| 4.5.1.2 | Input Crowbar, RFI Filter and Line Rectifier | 4-14 |
| 4.5.1.3 | Switching Regulator | 4-15 |
| 4.5.1.4 | Sine-Wave Inverter | 4-17 |
| 4.5.1.5 | Output Rectifiers, Post Regulators | 4-18 |
| 4.5.2 | DRIVER BOARD (PART NO. 12035-60003) | 4-18 |
| 4.5.2.1 | VCO and Phase-Locked Loop Synchronization | 4-19 |
| 4.5.2.2 | SCR Gate Drive | 4-19 |
| 4.5.2.3 | Switching Regulator Tri-Level Drive | 4-22 |
| 4.5.2.4 | Loop Regulator | 4-22 |

| | | |
|---------|--|------|
| 4.5.2.5 | Soft and Hard Fail Shutdown | 4-24 |
| 4.5.3 | LOGIC BOARD (PART NUMBER 12035-60004) | 4-25 |
| 4.5.3.1 | Under-Voltage Limit Comparators | 4-25 |
| 4.5.3.2 | Line Drop-Out Detector, SFS and HFS | 4-26 |
| 4.5.3.3 | LPU, PSU, PON, and PFW Logic | 4-28 |
| 4.6 | TROUBLE DIAGNOSIS | 4-29 |
| 4.7 | PARTS LOCATIONS | 4-30 |
| 4.8 | PARTS LIST | 4-30 |
| 5 | BATTERY BACKUP | |
| 5.1 | INTRODUCTION | 5-1 |
| 5.2 | OVERVIEW | 5-1 |
| 5.3 | SPECIFICATIONS | 5-3 |
| 5.4 | INTERFACE REQUIREMENTS | 5-5 |
| 5.4.1 | INTERFACE SIGNALS | 5-5 |
| 5.4.2 | EXTERNAL CONNECTOR | 5-5 |
| 5.4.3 | REMOTE/OFF/ON SWITCH | 5-5 |
| 5.4.4 | AUDIO ALARM | 5-6 |
| 5.4.5 | POWER SUPPLY INTERFACE | 5-6 |
| 5.4.6 | CENTRAL PROCESSOR UNIT INTERFACE | 5-6 |
| 5.5 | FUNCTIONAL THEORY OF OPERATION | 5-7 |
| 5.5.1 | BATTERY CHARGER | 5-7 |
| 5.5.2 | VOLTAGE REGULATORS | 5-7 |
| 5.5.3 | NORMAL OPERATION (AC LINE POWER PRESENT) | 5-7 |
| 5.5.4 | -12 VOLTS | 5-9 |
| 5.6 | THEORY OF OPERATION | 5-9 |
| 5.6.1 | BATTERY CHARGER | 5-9 |
| 5.6.2 | +5 VOLT REGULATOR | 5-9 |
| 5.6.3 | +12 VOLT REGULATOR | 5-10 |
| 5.6.4 | -12 VOLT OUTPUT | 5-11 |
| 5.6.5 | RELAY LOGIC | 5-11 |
| 5.6.6 | CONTROL SEQUENCE LOGIC | 5-12 |
| 5.6.7 | AUDIO ALARM/MLOST SIGNAL | 5-12 |
| 5.7 | PARTS LOCATIONS | 5-14 |
| 5.8 | PARTS LIST | 5-14 |
| 6 | BACKPLANE | |
| 6.1 | INTRODUCTION | 6-1 |
| 6.2 | OVERVIEW | 6-3 |
| 6.2.1 | SYSTEM ENVIRONMENT OVERVIEW | 6-3 |
| 6.2.2 | INTERNAL SPECIFICATIONS OVERVIEW | 6-5 |
| 6.2.3 | BACKPLANE INTERFACE HARDWARE | 6-9 |
| 6.2.3.1 | Processor Interface | 6-9 |
| 6.2.3.2 | Memory Interface | 6-9 |
| 6.2.3.3 | I/O Master Interface | 6-9 |
| 6.2.3.4 | Passive Interfaces | 6-9 |
| 6.3 | SPECIFICATIONS | 6-10 |
| 6.3.1 | GENERAL HARDWARE SPECIFICATIONS | 6-10 |
| 6.3.2 | POWER SUPPLY INTERCONNECT | 6-10 |
| 6.3.3 | CARD SOCKET INTERCONNECTS | 6-12 |
| 6.3.4 | BACKPLANE LOADING RULES | 6-12 |

| | | |
|---------|--|------|
| 6.3.4.1 | DC Loading | 6-12 |
| 6.3.4.2 | Actual Worst Case Loading | 6-15 |
| 6.3.4.3 | AC Loading | 6-16 |
| 6.3.4.4 | Data Bus | 6-16 |
| 6.3.4.5 | All Other Lines | 6-16 |
| 6.4 | INTERFACE REQUIREMENTS | 6-16 |
| 6.4.1 | MEMORY ACCESS PROTOCOL | 6-18 |
| 6.4.2 | MEMORY HANDSHAKE TIMING | 6-19 |
| 6.4.3 | INTERRUPT PROTOCOL | 6-19 |
| 6.4.4 | INTERRUPT LATENCY | 6-23 |
| 6.4.5 | REMOTE MEMORY ACCESS | 6-23 |
| 6.4.6 | EXPANDED MEMORY ACCESS | 6-23 |
| 6.4.7 | I/O TRANSFER PROTOCOL | 6-24 |
| 6.4.8 | I/O INSTRUCTION EXECUTION | 6-24 |
| 6.4.9 | SLAVE MODE TRANSFERS | 6-25 |
| 6.5 | SIGNAL TIMING SPECIFICATIONS | 6-28 |
| 6.5.1 | DUAL-SPEED CLOCK REFERENCES | 6-32 |
| 6.5.2 | INTERACTIVE TIMING EXAMPLES | 6-33 |
| 6.6 | SIGNAL DEFINITIONS | 6-61 |
| 6.7 | PARTS LOCATIONS | 6-81 |
| 6.8 | PARTS LIST | 6-81 |
| 7 | POINT-OF-LOAD REGULATOR | |
| 7.1 | INTRODUCTION | 7-1 |
| 7.2 | SPECIFICATIONS | 7-1 |
| 7.3 | THEORY OF OPERATION | 7-2 |
| 7.4 | PARTS LOCATIONS | 7-2 |
| 7.5 | PARTS LIST | 7-2 |
| 8 | EXTENDED MEMORY | |
| 8.1 | INTRODUCTION | 8-1 |
| 8.2 | OVERVIEW | 8-1 |
| 8.2.1 | SYSTEM ENVIRONMENT | 8-1 |
| 8.2.2 | BASIC MEMORY OPERATION | 8-3 |
| 8.2.3 | BASIC MAP CONTROL OPERATIONS | 8-4 |
| 8.2.4 | POWER REQUIREMENTS | 8-5 |
| 8.2.5 | POWER SUPPLY CONFIGURATION | 8-5 |
| 8.2.6 | PARITY | 8-6 |
| 8.3 | FUNCTIONAL THEORY OF OPERATION | 8-7 |
| 8.3.1 | BACKPLANE INTERFACE | 8-7 |
| 8.3.2 | MEMORY TIMING AND CONTROL LOGIC | 8-11 |
| 8.3.3 | MEMORY REFRESH LOGIC | 8-12 |
| 8.3.4 | MEMORY MAPPING OPERATION | 8-13 |
| 8.3.5 | MAPPING CONTROL LOGIC | 8-17 |
| 8.3.6 | FRONTPLANE SIGNALS | 8-17 |
| 8.3.7 | ARRAY BOARD CONTROL AND TIMING LOGIC | 8-20 |
| 8.4 | DETAILED THEORY OF OPERATION | 8-20 |
| 8.4.1 | MEMORY CONTROL LOGIC | 8-24 |
| 8.4.2 | MEMORY REFRESH LOGIC | 8-26 |
| 8.4.3 | MAPPING CONTROL LOGIC | 8-27 |
| 8.4.3.1 | INSTRUCTION RECOGNITION LOGIC | 8-27 |

| | | |
|---------|--|------|
| 8.4.3.2 | MAPPING CONTROL STATE MACHINES | 8-28 |
| 8.4.3.3 | ADDRESS PATH ENABLE LOGIC | 8-31 |
| 8.4.4 | ARRAY CARD CONTROL LOGIC | 8-33 |
| 8.4.5 | PARITY CIRCUITRY | 8-34 |
| 8.5 | PARTS LOCATIONS | 8-34 |
| 8.6 | PARTS LISTS | 8-34 |

A SELF-TEST, LOADER, AND VCP PROGRAMS

B APPLICATION INFORMATION FOR 25 KHz POWER

| | |
|---------------------------|-----------|
| HP 1000 L-SERIES COMPUTER | SECTION I |
|---------------------------|-----------|

1.1 INTRODUCTION

The HP 1000 L-Series Computer and Computer System are low-cost versions of the HP 1000 Computer family and, as such, are designed to deliver full minicomputer power to a variety of cost-critical applications.

1.2 PHYSICAL DESCRIPTION

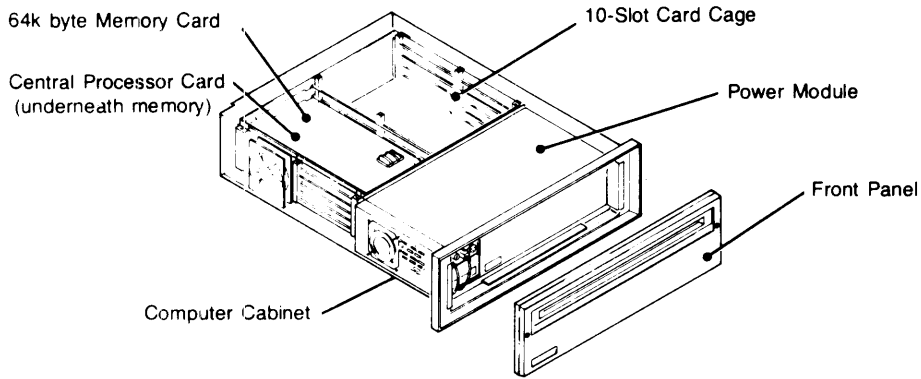
The L-Series computer hardware is available as printed circuit boards, computer units (boxes containing several printed circuit boards), and computer systems (boxes containing several printed circuit boards plus peripheral devices). This document is intended to assist you in arranging any of the L-Series combinations into unique, special-purpose computing systems.

Figure 1-1 illustrates L-Series boards, computers, and systems. Figure 1-2 contains a block diagram of the HP 1000 L-Series Computer.

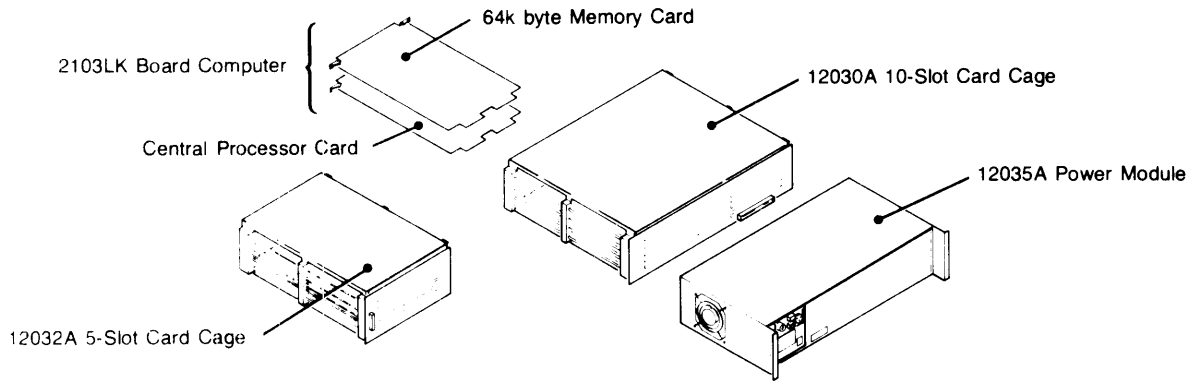
1.3 ELECTRICAL DESCRIPTION

The L-Series computer architecture is based on a "distributed intelligence" design using two custom silicon-on-sapphire (SOS) integrated circuit (IC) chips. The central processor unit (CPU) chip can execute most of the HP 1000 Computer Series instruction set (see the L-Series Computer Reference Manual, part no. 02103-90007). The CPU chip, in conjunction with other logic on the processor card, performs several system-level functions including memory protect, power fail/auto restart, time-base generation, parity error interrupt, and extensive self-tests.

2103L (box) Computer



2103LK Board Computer and Integration Accessories



I/O Interfaces, expanded memory, and other plug-in accessories

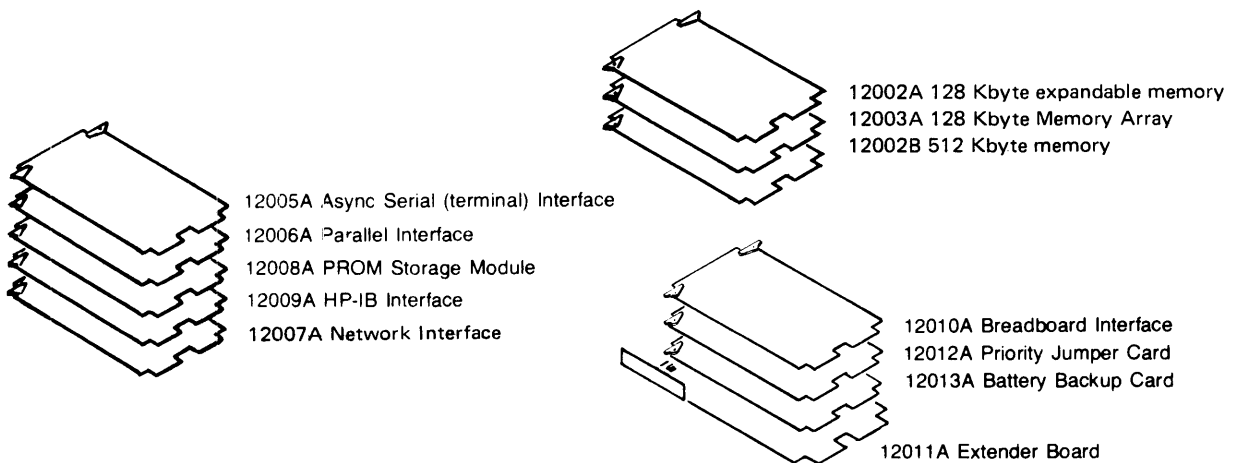


Figure 1-1. HP 1000 L-Series Computers (Sheet 1 of 2)

HP 1000 L-Series Computer Systems, Models 9 and 10

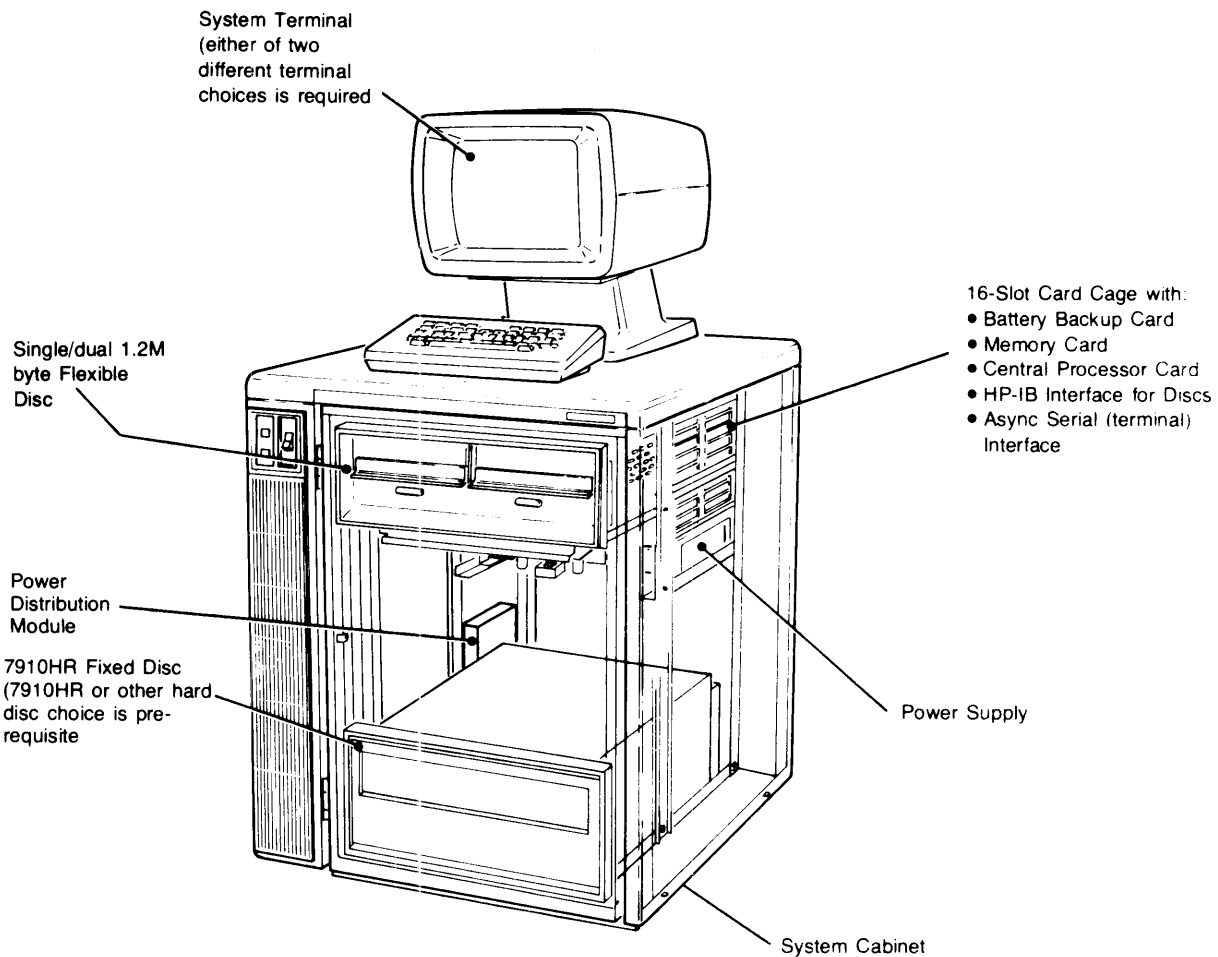
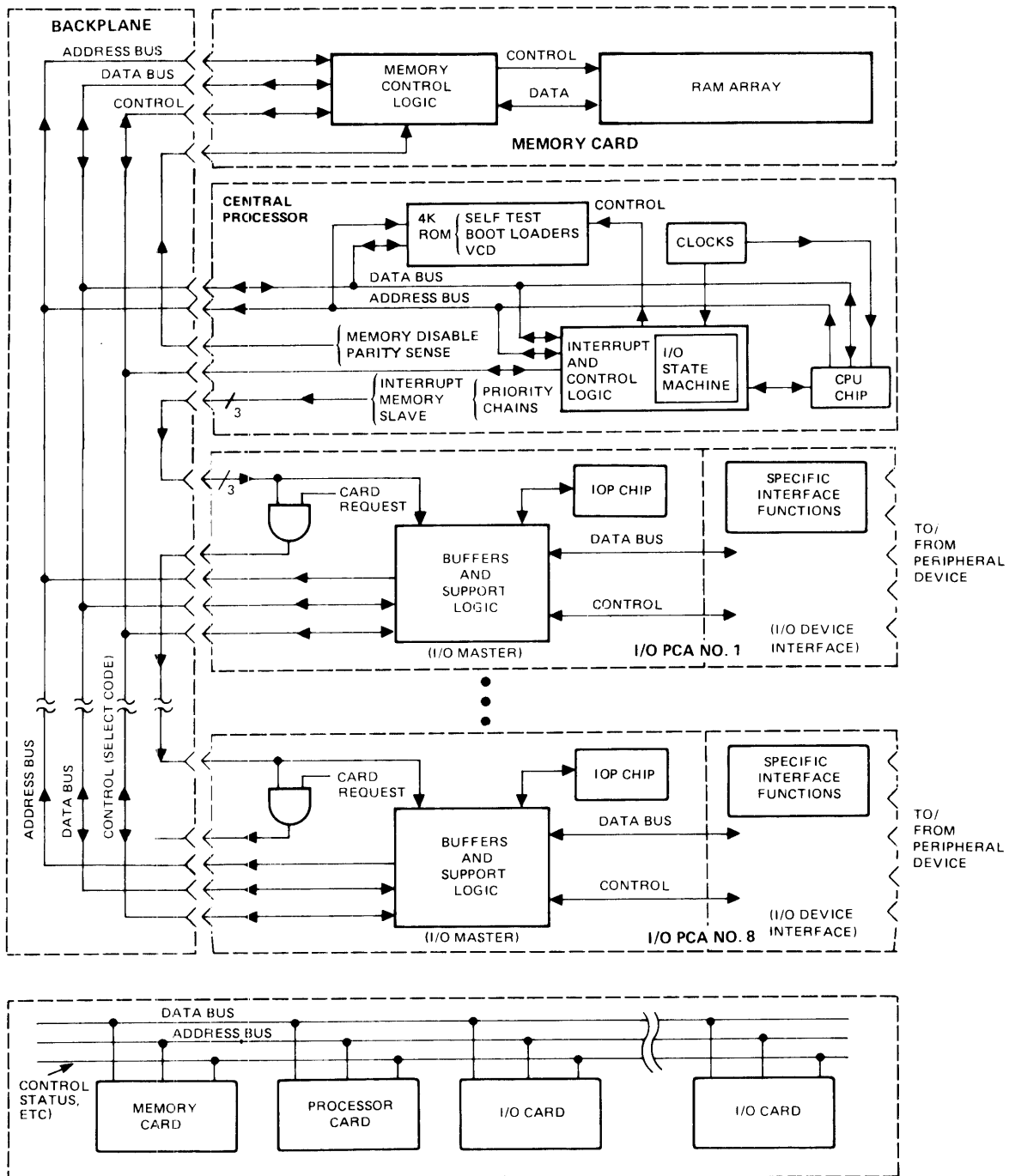


Figure 1-1. HP 1000 L-Series Computers (Sheet 2 of 2)



7700-459-1

Figure 1-2. HP 1000 L-Series Computer Block Diagram

All I/O instructions referencing select codes greater than octal 17 are executed by input/output processor (IOP) chips located on the individual I/O interface cards. A common backplane links the processor, memory, and I/O cards, allowing the IOP chips to monitor the flow of instructions over the backplane. They can, however, execute only those instructions that apply to I/O.

Because each I/O card is capable of operating independently of the processor, the L-Series can perform direct memory access (DMA) I/O transfers very efficiently. During DMA, an I/O card interacts with the processor card only on DMA initiation and completion; otherwise, the entire high-speed transfer is handled by the I/O card, leaving the processor card free to perform other tasks. This results in significant gains in overall system throughput.

1.4 SYSTEM SUPPORT FEATURES

1.4.1 VIRTUAL CONTROL PANEL

The Virtual Control Panel (VCP) is an interactive program located in a ROM (the VCP ROM) on the processor card. Because the L-Series does not have a conventional front panel, the VCP provides the capability of allowing a peripheral device, such as a terminal, to function as a virtual control panel (via an I/O interface card). In addition, when the L-Series is operating as an unattended, terminal-less node in a multi-computer network, a remote computer can function as a virtual control panel (again, via an I/O interface card).

The virtual control panel makes use of the L-Series slave mode feature. That is, the processor card is in slave mode when a device is operating as a virtual control panel.

The VCP program allows the peripheral device or remote computer to control execution of a program, access processor registers (A, B, P, etc.), examine or change memory, and then convey this information back to the remote device.

Slave, or VCP mode, can be entered in any one of three ways:

- a. After power up, when the boot loading program is directed to the VCP ROM in lieu of a boot routine.
- b. When an interface card requests slave mode.

c. Certain instructions can cause slave mode to be entered, as follows:

- 1) A HALT instruction causes an I/O interface card to do a Slave Request.
- 2) A CLC 3 instruction causes a Slave Request after four instructions are executed. The CLC 3 instruction is used by the VCP program to allow an operator (using the device connected to the I/O interface card) to single step through instructions.

The VCP ROM code is listed in Appendix A.

1.4.2 SELF-TEST CAPABILITY

The L-Series contains built-in self-test capability. Each time power comes up, the CPU chip, in conjunction with the processor card, executes a sequence that applies all possible combinations to the address bus, reads the address lines onto the data lines, reads the data lines back into the processor, and checks this input data against what was sent out. Any errors cause the processor to freeze, with the processor status lights indicating that the self-test has failed. The processor freeze is necessary because any failure of the data or address bus will prevent the computer from operating correctly, and thus must be repaired immediately.

Upon completion of the loop-back portion of the self-test built into the CPU chip, control is passed to the VCP ROMs, which contain the remainder of the self-test. Memory, all installed I/O interfaces, and much of the processor card circuitry is given a basic functional check.

The self-test procedure provides a reasonable probability that the minimum set of capabilities necessary to run a system is present when the system is booted in.

See the following manuals for a complete description of the self-test feature:

HP 1000 L-Series Computer System Installation and Service Manual, part number 02145-90003. (This manual covers the complete L-Series system, including peripheral devices.)

HP 1000 L-Series Computer Installation and Service Manual, part number 02103-90001. (This manual covers the L-Series computer only, excluding the peripheral devices.)

A listing of the self-test program contained in the ROMs on the processor card is given in Appendix A.

1.5 L-SERIES CARDS

The following information is of interest to customers who purchase L-Series cards. These customers will need to provide voltage, current, and ventilation as specified in the following paragraphs. Backplane information covering such items as connector pinouts, card cage layouts, and card cage assembly drawings is included in Section VI of this document.

1.5.1 POWER REQUIREMENTS

NOTE

Power requirements for I/O interface cards (Parallel Interface, Asynchronous Serial Interface, etc.) are provided in individual manuals covering these cards.

| <u>CARD</u> | <u>VOLTAGE</u> | <u>CURRENT</u> | | <u>POWER</u> | |
|----------------------|----------------|----------------|-----------|--------------|-----------|
| | | STANDBY | OPERATING | STANDBY | OPERATING |
| Processor Card | +5V | 0mA | 2962mA | 0W | 14.81W |
| | +5M | 250mA | 250mA | 1.28W | 1.28W |
| | +12V | 0mA | 36mA | 0W | .43W |
| Memory, 12002A | +5V | 0 | 2.4A | 0 | 12.4W |
| | +5M | 420mA | 630mA | 2.1W | 3.2W |
| Memory, 12002B | +5V | 0 | 2.4A | 0 | 12.4W |
| | +5M | 620mA | 1.0A | 3.2W | 5.1W |
| Memory Array, 12003A | +5V | 0 | 900mA | 0 | 4.6W |
| | +5M | 260mA | 500mA | 1.3W | 2.3W |
| Memory, 12004A | +5V | 0mA | 1300mA | 0W | 6.50W |
| | +5M | 757mA | 757mA | 3.79W | 3.79W |
| | +12M | 48mA | 273mA | 0.58W | 3.28W |
| | -12M | 20mA | 20mA | 0.24W | 0.24W |

REQUIRED REGULATION

+5 VOLTS +/- 0.25 VOLT (5%)

+12 VOLTS +/- 0.60 VOLT (5%)

-12 VOLTS +/- 1.2 VOLT (10%)

REGULATION SUPPLIED BY 12035A

DC voltages, Tolerances, and Periodic and Random Deviation
(No Load to Full Load):

| | | |
|-----------|--------|-----------------------|
| +5 VOLTS | +/- 2% | 50mV, nom., 300mV,max |
| +12 VOLTS | +/- 3% | 100mV, max. |
| -12 VOLTS | +/- 6% | 100mV, max. |

If memory is to be sustained during power failure, the "M" (memory) voltages must be isolated from the processor and I/O voltages. If this feature is not desired, the +5M, +12M, and -12M may be common with the +5V, +12V, and -12V, respectively.

Additional power requirement information may be obtained from the HP 1000 L-Series Product Data Book. The current edition of the data book can be obtained from your local Hewlett-Packard Sales and Service Office.

NOTE

The current requirements for planned additions to your computer should be considered when designing your power supply.

1.5.2 VENTILATION REQUIREMENTS

Air intake may be from either the left or right side of the card cage. Vents are provided in the sides of the various card cage assemblies for this purpose. See the appropriate assembly drawing in Section VI of this document for the type of card cage you are using.

Air flow requirements in cubic feet per minute (cfm) can be computed as follows:

$$\text{cfm required} = \text{watts} \times 0.22$$

where 0.22 is a constant to provide the total cfm required so that the temperature rise should not exceed 10 degrees Celsius from ambient, and where maximum ambient is 55 degrees Celsius.

1.5.3 CARD CAGE AND BACKPLANE ASSEMBLIES

Information for assembling cards into the three card cages available with the HP 1000 L-Series is provided in Section VI of this document.

| | |
|----------------|------------|
| PROCESSOR CARD | SECTION II |
|----------------|------------|

2.1 INTRODUCTON

The most important component on the processor card (figure 2-1) is a 64-pin silicon-on-sapphire (SOS) CMOS chip (CPU chip) that handles instruction execution, slave mode processing, and interrupt servicing functions. In this document, the terms "CPU chip" and "CPU" are used interchangeably and both terms refer to the CPU chip.

2.2 OVERVIEW

The CPU chip executes a major portion of the computer's instruction set pertaining to arithmetics and system control. The processor card also contains 4K of ROM firmware providing power up self-test, boot loader, and Virtual Control Panel (VCP) capabilities.

Four Field Programmable Logic Arrays (FPLA's) form the nucleus of a state machine which executes low select code I/O instructions and aids in handling interrupts.

Since the L-Series Computer is a synchronous machine, all of the clocks are generated on the processor card. The 40% duty cycle clocks are derived from a very stable crystal oscillator which doubles as an accurate time base for the time base generator.

Eight miniature LEDs are used to report operating or error status and eight switches allow easy selection of boot loaders and auto-restart options. Refer to the HP 1000 L-Series Computer Installation and Service Manual, part number 02103-90003 for a discussion of the LEDs and switches.

The balance of the processor card circuitry is composed of Schottky and low-power Schottky integrated circuits of the 7400 series TTL. These components are used to interface the CPU chip to the backplane and to the state machine on the processor card that handles the low select code I/O instructions.

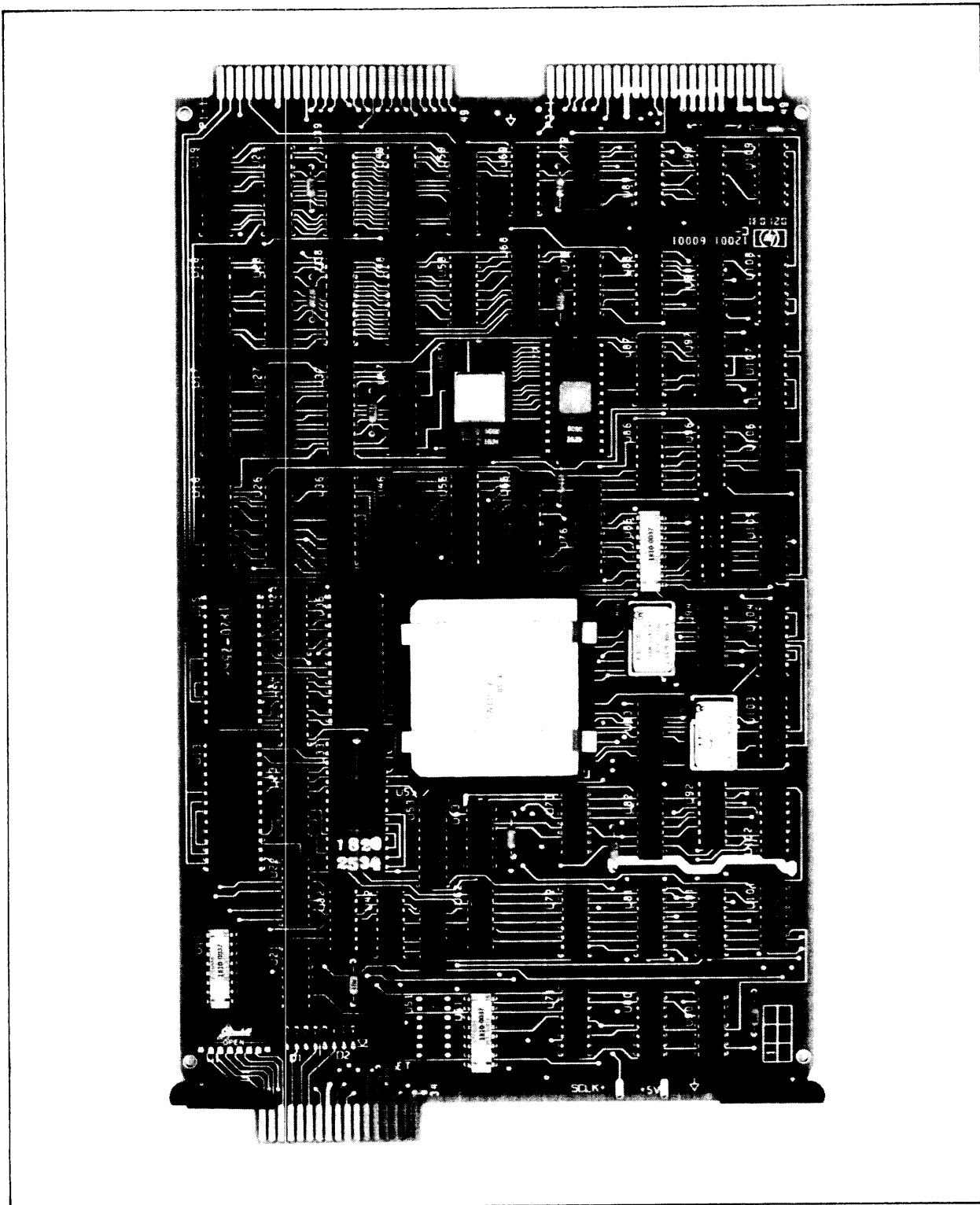


Figure 2-1. Processor Card (12001-60001)

2.2.1 SYSTEM ENVIROMENT

The system environment of the HP 1000 L-Series Computer is shown in figure 2-2. Note that the memory card is located immediately above the processor card and that all I/O cards are placed below the processor in descending interrupt and DMA priority. The processor card may go in any card slot as long as these rules are preserved. Empty slots between cards are not permitted in order to guarantee interrupt and DMA priority. See Section VI, figure 6-3, for card slot priorities.

Once plugged into the backplane, the processor card needs no further connection or cabling.

2.3 PROCESSOR CARD FUNCTIONAL THEORY OF OPERATION

The following paragraphs contain a functional description of the processor card. A functional description of the CPU chip is presented starting with paragraph 2.4.

A functional block diagram of the processor card is shown in figure 2-3.

2.3.1 MEMORY ACCESSING

All memory requests from the processor card, except for an interrupt trap cell fetch, are initiated by the CPU chip. The memory request may access either RAM on the memory card or ROM on the processor card. Since DMA operations by the I/O cards and memory requests by the processor card use the same protocols, RAM on the memory card may be accessed by all I/O channels and the processor. However, the ROM on the processor card can be accessed only by the CPU chip.

Because of the distributed intelligence concept of the HP 1000 L-Series, the processor card and all I/O cards latch the instruction off the data bus during each instruction fetch. The CPU chip and the processor card are responsible for the execution of their instruction set and, likewise, each I/O interface card must perform the I/O instructions pertaining to it. In addition, remote processors may reside as part of the L-Series system and execute those instructions not recognized by the CPU chip, the processor card, or any I/O interface card.

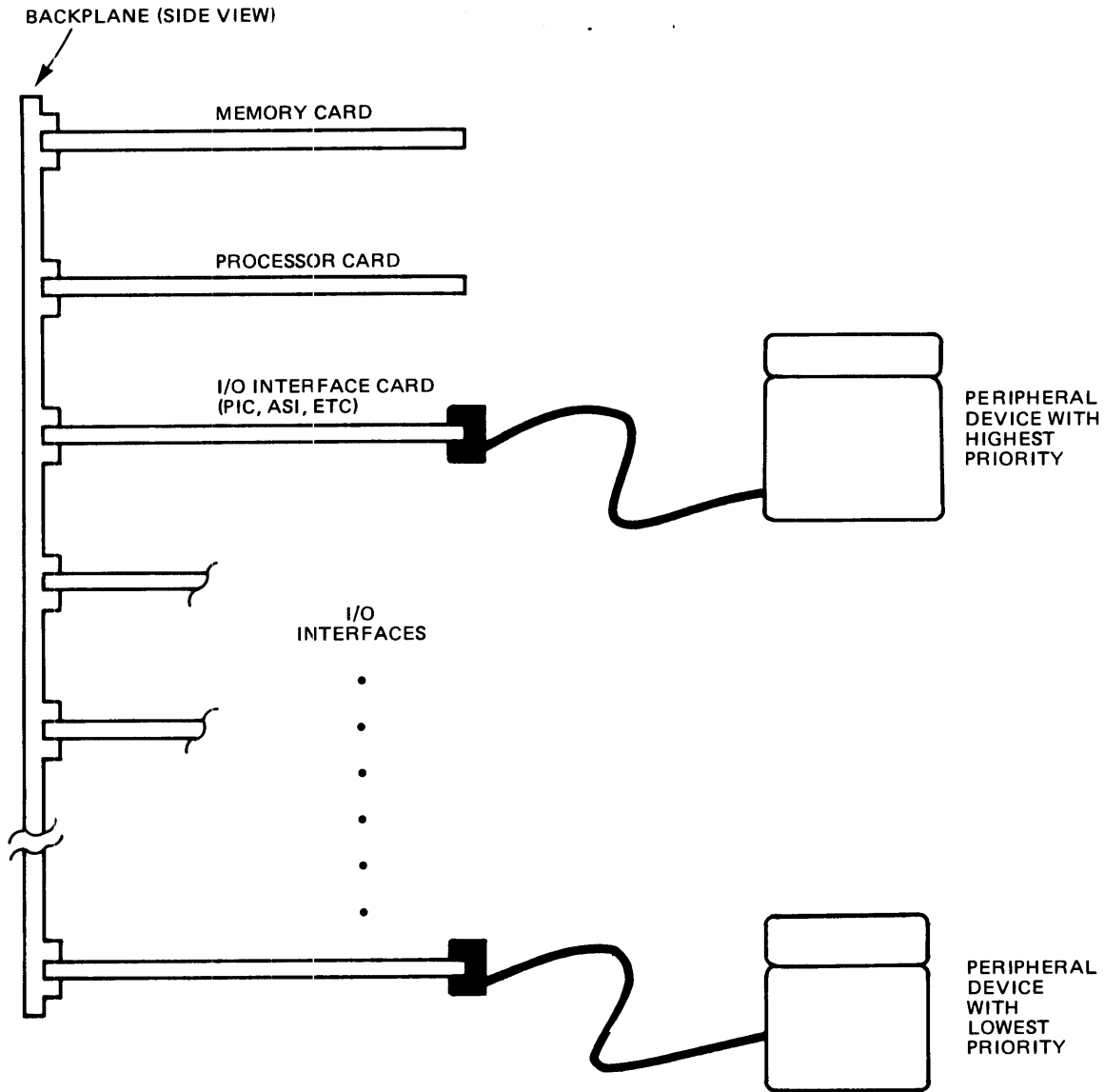
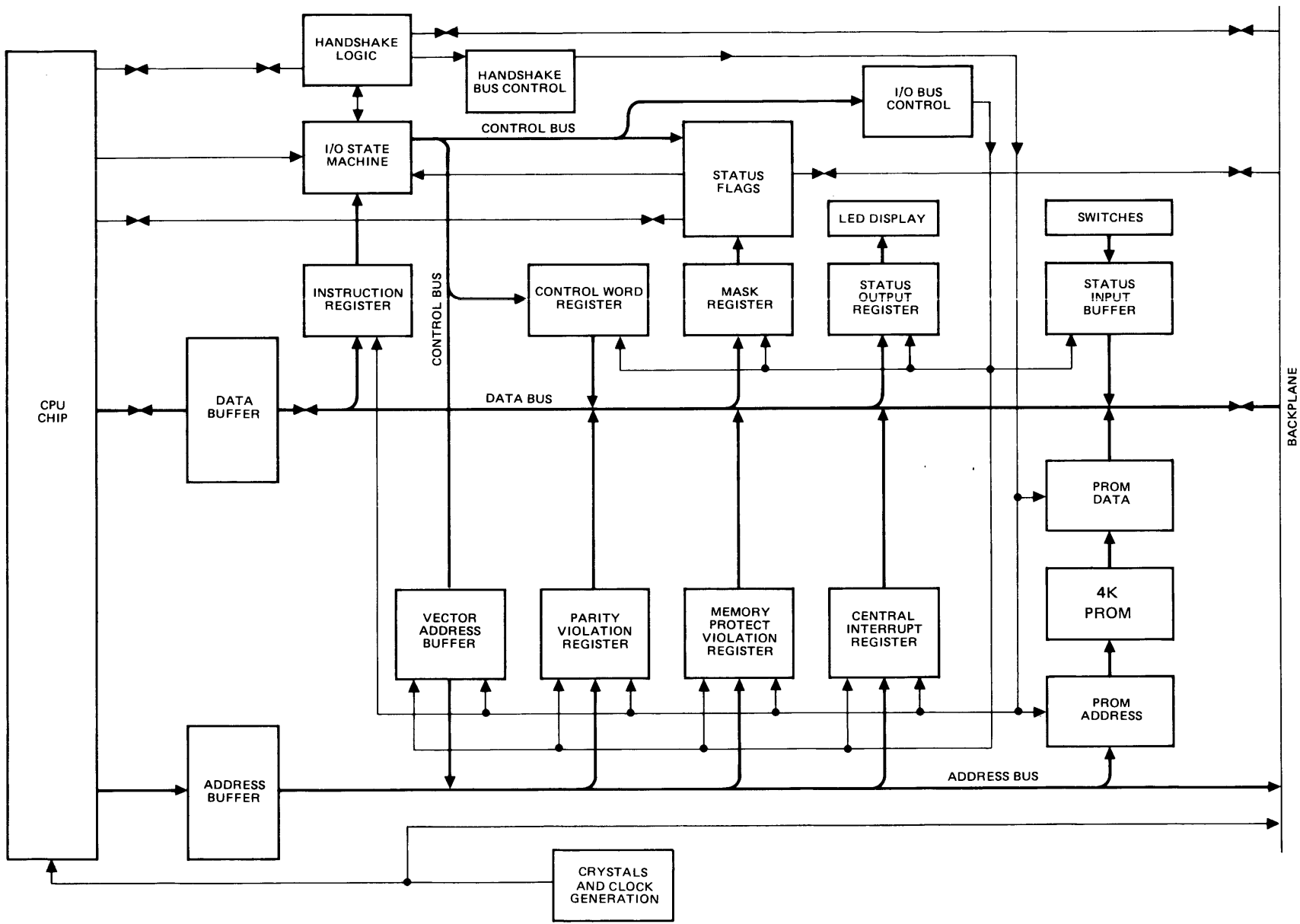


Figure 2-2. Processor Card in Typical System Environment

Figure 2-3. Processor Card Functional Block Diagram



Direct Memory Access (DMA) by the I/O cards is usually given higher priority than any memory access request from the CPU chip. If DMA is in process or pending, the processor card withholds the next CPU memory access until the current series of DMA is completed. The processor can momentarily suspend this hierarchy if the CPU chip was denied access to memory for thirty-two consecutive DMA memory accesses. This arrangement grants DMA nearly the full memory access bandwidth yet permits the processor to guarantee reasonable interrupt latency in DMA intensive environments.

When there are no active or pending DMA requests, the CPU initiates its memory request to the memory card. In a memory read transaction, the addressed data is returned at the end of the memory cycle. In the case of a memory write request, the data to be stored is sent to memory card at the same time as the address at the start of the memory cycle. A memory read request is distinguished from a write request by the sense of the most significant bit (AB15) in the address sent to the memory card.

ROM on the processor card is accessed by the CPU chip in relatively the same fashion, except that the memory card has been disabled and the ROMs have been enabled under program control or by the appropriate control word to the CPU chip during a slave transfer. This CPU access to ROM has no effect on DMA since the memory card is disabled only during the time it takes the CPU to access the memory card while the CPU is not in a memory cycle accessing ROM.

The A and B registers in the CPU chip are treated as physical memory locations 0 and 1, respectively, for instruction fetching. Any reference to those locations by the program counter is treated as an instruction fetch from the appropriate CPU chip register. When a program or DMA addresses the 0 or 1 memory location, it is addressing those memory locations and not the A or B register. Neither the program nor DMA should utilize these two memory locations since data stored there will be altered in the course of an instruction fetch from the A or B registers.

2.3.2 INTERRUPT PROCESSING

2.3.2.1 Interrupt Requests

There are two types of interrupt requests in the HP 1000 L-Series Computer. System level interrupts may be generated by the processor card to handle system level problems such as power fail and parity error. I/O interrupts may be requested by the individual I/O cards to cause processing to service the needs of that I/O channel.

The processor card receives all system level and I/O interrupt requests and determines which interrupt will be serviced. Three basic levels of importance define the relative priority of interrupt requests. A level one interrupt request has no restrictions in obtaining interrupt service. Level two and three requests are collectively enabled/disabled by a STC/CLC 4, the interrupt

inhibit flag. Level three interrupt requests may be further enabled/disabled by a STF/CLF 1, the interrupt system flag. In addition, interrupt masks are available to mask off any or all of the level three interrupt requests. A hardware signal from the CPU chip called Temporarily Disable Interrupt will cause one of the level two and all level three requests from interrupting following certain instructions and slave mode transfers.

The interrupt system flag is set/cleared with the STF/CLF 1 instruction, and affects level three interrupt requests. When the flag is set, the Time Base Generator (TBG) and any unmasked I/O interrupt request will receive service. The interrupt system flag allows the programmer to prevent TBG and I/O interrupts from interfering with selected portions of a program. This flag is cleared on power-up and in response to a CLC 0 instruction.

The Temporarily Disable Interrupt (TDI-) signal is utilized to resolve complications that would arise if an interrupt occurred while executing an indirect jump instruction. For the next instruction cycle following a jump, indirect (JMP,I); a jump to subroutine, indirect (JSB,I); an I/O group instruction; or enabling the bootstrap ROMs in slave mode processing; the processor will hold off the power fail interrupt request and all level three requests. Up to three levels of indirect jumps will keep these requests disabled. The power fail interrupt request is included in this group to simplify the power fail, auto-restart routine because it would not be necessary to save the status of an incomplete indirect jump sequence. The TDI- signal is asserted at power-up and de-asserted after the first instruction fetch unless that instruction falls into one of the above classifications.

The interrupt inhibit flag can disable all but the two highest priority interrupt requests: parity error and unimplemented instruction. The flag can be set/cleared by STC/CLC 4 in software. This feature can be used to prevent level two and three interrupt requests from delaying the preservation of system status in the event of power-down or from confusing system status restoration during power-up. The interrupt inhibit flag is automatically cleared on power-up. Typically, the flag should be set upon entering a power-up routine during auto-restart or at the start of a power-down routine at power fail. In addition, the interrupt inhibit flag should be set at the beginning of any interrupt service routine and not cleared until the central interrupt register has been recovered. Entry into the power-down routine via a power fail interrupt causes the interrupt inhibit flag to be set.

There are six system level interrupt requests. In order of priority, they are:

- a. Parity error.
- b. Unimplemented instruction.
- c. Memory protect.
- d. Special interrupt.

- e. Power fail.
- f. Time base generator.

There can be as many I/O interrupt requests as there are I/O interface cards in the system since each I/O card has interrupt capability. The priority of I/O interrupt requests among the I/O cards is a function of the card's physical placement from the processor; the closest card has the highest priority and cards below it have descending priority independent of the select codes assigned. I/O interrupt requests have lower priority than TBG and both are maskable.

A parity error interrupt request occurs when the memory card signals a parity error during a processor memory access if the parity system had been enabled. The parity system is enabled/disabled by a STC/CLC 5 command in software. The current sense of parity is made even/odd by STF/CLF 5 and the default at power-up is odd parity. Parity error takes precedence over other system level problems because incorrect data reaching the CPU chip may be construed erroneously as an unimplemented instruction or a memory protect violation. Therefore, any parity error occurring during a processor access to memory is considered catastrophic and is serviced immediately.

An unimplemented instruction interrupt request is made when the CPU chip signals that the last instruction fetched was not recognized by the chip or by any other system card. This interrupt provides a straightforward entry to software routines for the execution of instruction codes not recognized by the computer hardware. This request must receive immediate service in order to recover the instruction code that caused it. The unimplemented instruction interrupt is never inhibited and concedes priority only to a parity error.

A memory protect interrupt request is made when the CPU chip signals that the last instruction fetched has violated the memory protection rules while memory protect is enabled. The memory protect feature is enabled with a STC 7 instruction and an OTA/B 7 is used to load the memory protect fence from the A or B register. All memory locations below the fence address are considered protected and can not be written into. I/O instructions are also affected. Any I/O instruction except those referring to select code 1 but not including HALT 1, will trigger a memory protect interrupt request if memory protect is enabled. This will insure that a user program will not interfere with the operating system's handling of I/O. The memory protect interrupt request can only be inhibited by the interrupt inhibit flag.

A special interrupt request is a user-defined high priority interrupt request from either the backplane or the frontplane. This is the only general purpose system level interrupt whose application is assigned by the user. This interrupt request has lower priority than memory protect and can only be inhibited by the interrupt inhibit flag.

A power fail interrupt request is made after the power supply has signalled a power fail warning. This warning indicates that line power has been cut off and that regulated power will soon be lost. The power fail interrupt request

may be denied by either the interrupt inhibit flag or a temporary interrupt disable.

A time base generator (TBG) interrupt request is initiated every ten milliseconds to update any real time clocks in software. The TBG signal originates from the CPU chip and is accurate to within 4.3 seconds per day. This level three interrupt is maskable and requires the interrupt system to be enabled, that interrupts not be temporarily disabled, and that level two and three interrupts are not inhibited.

I/O interrupt requests come from the I/O interface cards. Collectively, these requests may be inhibited by the same signals which inhibit TBG interrupt requests. TBG commands higher priority than I/O requests when both request interrupt service. The interrupt mask is used to disable I/O requests by select code groups.

The following chart shows pictorially the relative priority and the qualifiers required by each interrupt request.

level 1

parity error during a CPU memory access
unimplemented instruction

*****interrupt inhibit flag (STC/CLC 4)

level 2

memory protect violation
special interrupt request

-----Temporarily Disable Interrupt (TDI-)

power fail

*****interrupt system flag (STF/CLF 0)

level 3

-----interrupt mask

time base generator
I/O interrupt requests

2.3.2.2 Interrupt Service

An interrupt is acknowledged by fetching an instruction from the memory location whose address matches the select code of the interrupt requestor. Service of simultaneous interrupt requests is accomplished on a priority basis. The highest priority system level interrupts are serviced first, before any I/O interrupts, which are serviced according to their location from the processor (see Section VI, figure 6-3 for an illustration of slot priority).

The CPU chip handles interrupts on a generalized basis without knowing which request it is servicing. The processor card receives all requests but only informs the CPU chip that there is an interrupt pending. At the end of the current instruction execution, the CPU will acknowledge the interrupt. All of

the normal protocols used for an instruction fetch are used except that the instruction address and MEMGO- are driven by the highest priority requesting device instead of the CPU. The processor card is responsible for providing the vector address if a system level interrupt is being serviced. Service of an I/O interrupt is accomplished by the requesting I/O card when it drives its select code onto the address bus as the vector address.

Interrupt servicing on the HP 1000 L-Series is performed by executing an instruction located in the trap cell accessed by the vector address. The vector address is the address at which interrupt servicing begins. System level interrupts are associated with vector addresses 4 through 17 octal while vector addresses 20 to 77 octal are reserved for all possible I/O card select codes. Therefore, the vector address is equivalent to the select code assigned to that I/O channel. The trap cell is the first instruction of each interrupt service routine and is stored in the vector address locations. A JSB instruction is normally found in the trap cells to cause program execution to branch to the appropriate service routine and then to return to the original program at the completion of the subroutine.

An I/O state machine on the processor card handles interrupts associated with I/O select codes and vector addresses 4, 5, 6, 7, 10, and 17. These are the power fail, parity error, time base generator, memory protect violation, unimplemented instruction, and special interrupts, respectively. For example, suppose the CPU chip detects the presence of an unimplemented instruction and informs the processor that such a condition exists. The state machine qualifies this as a valid interrupt request and asks the CPU chip for an interrupt. The CPU will acknowledge the interrupt and proceed to do an instruction fetch minus the instruction address and a MEMGO-. The I/O state machine will supply the vector address 10 octal and the MEMGO- to start the interrupt service with the instruction at that address.

An interrupt handled by the I/O interface cards begins with an interrupt request. The highest priority I/O request waits until it receives an interrupt acknowledge signal (IAK-) simultaneously with a deasserted ICHOD- on the backplane. ICHOD- is the interrupt chain disable output of the next higher priority interrupting device. Since all system level interrupts have priority over I/O interrupts, ICHOD- is deasserted by the processor card when there are no system level interrupt requests pending. The authorized I/O card will put its select code on the address bus as the vector address and begin the memory cycle with a MEMGO-.

The interrupt acknowledge signal IAK- normally occurs at the end of the current instruction cycle and before the next instruction fetch. Only in the case of an unimplemented instruction or a memory protect violation will the CPU chip behave differently. An unimplemented instruction has an instruction cycle which can not be completed, so the CPU chip will report that status to the processor and wait for an interrupt request. For an instruction which causes a memory protect violation, the CPU chip must immediately inform the processor that there is a violation. The processor will block any CPU attempts to write to memory during the current instruction cycle by converting

all memory writes to memory reads. This insures that no memory locations below the memory protect fence are destroyed before the interrupt is serviced. If the violation was due to the presence of an I/O instruction when memory protect is enabled, the instruction is not executed before the interrupt is serviced.

Interrupt latency is the time between the interrupt request and its acknowledgement. This time is normally less than the time it takes to execute the current instruction but may be lengthened by concurrent DMA intervention on the backplane. Since DMA has priority over the processor for memory accesses, any interrupt acknowledgement will also be delayed until current DMA is completed. Depending on DMA utilization of the backplane, interrupt latency can vary from microseconds (typical) to nearly a millisecond during complete DMA monopolization of the backplane. For applications where short latency times are desirable, DMA should be suspended or operated at lower transfer rates.

2.3.3 I/O PROCESSING

2.3.3.1 I/O Accessing

Most of the I/O group instructions are executed by the processor card I/O state machine or by the IOP chip on the interface cards. Instructions such as STC/CLC and STF/CLF can be executed by the appropriate interface card without interaction with the CPU chip. Other I/O instructions such as SFS/SFC, LIA/B, MIA/B, and OTA/B do affect the operation of the CPU and hence require a set of I/O protocols to handle this situation. A third set of I/O instructions involving the overflow bit in the CPU chip is executed solely by the CPU without involving the IOP chip.

I/O accessing to the appropriate I/O channel is made by select code. Select codes 20 to 77 octal are the valid codes for the interface cards. All lower select codes, 0 through 17 octal, are reserved for system level I/O processing, which includes the enable/disable interrupt system and output to the status register instructions. These low select code I/O instructions are generally handled by the processor I/O state machine or by the CPU chip.

Interaction between the various processors in the HP 1000 L-Series is facilitated by I/O handshakes. This effectively places the CPU chip into slave mode so that its internal registers may be read or altered by the I/O executor to accomplish the execution of the instruction. A single handshake is required for the I/O executor to inform the CPU chip to increment the program counter if the conditional skip is true. A double handshake is necessary if any data is passed into or out of the CPU. The first handshake passes a control word to the CPU chip to tell it how to process the data transfer which takes place during the second handshake. This allows the A or B registers to be loaded from or merged with an I/O buffer, or to be copied into an I/O buffer.

Suppose that an I/O interface card with select code 27 receives a SFS 27 instruction and that its flag had been previously set. That I/O card asserts IORQ- as soon as it has recognized the instruction and determined that the conditional skip is true. The CPU will eventually respond with an IOGO- assertion to affirm that it has received the I/O handshake request. The I/O card will de-assert IORQ- to signal that the control word will be available on the data bus on the second rising edge of SCLK-. That control word will contain the command to cause the CPU chip to increment the program counter again. The program counter is always incremented at the end of an instruction fetch to point to the next instruction; incrementing it once more during a conditional skip will effectively cause execution to pass over the next instruction.

If an LIA 27 instruction has appeared on the backplane, the affected I/O interface card will assert IORQ- and wait for IOGO- also. Upon releasing IORQ-, it informs the CPU that the next I/O handshake will require information on the data bus to be loaded into the A register. IORQ- is asserted again one state after its previous de-assertion to begin the second half of the double handshake. After the re-assertion of IOGO- to the second IORQ-, the interface card puts the data word on the backplane data bus. The CPU loads the A register with this data on the second rising edge of SCLK- after the de-assertion of the second IORQ-. Operation of the LIB, MIA/B, or OTA/B instructions is similar, except for the direction or destination of the data flow.

Like processor accesses to memory, the completion of an I/O handshake is subject to DMA action on the backplane. DMA is automatically suspended for an instruction fetch but may be resumed thereafter by I/O cards unaffected by the instruction. The affected I/O card will issue an IORQ- but the processor will be unable to respond with an IOGO- until all pending DMA is completed. At that time, the assertion of IOGO- will suspend DMA until the end of the current I/O access.

2.3.3.2 Processor Card I/O Functions

Six program-accessible registers are resident on the processor card:

- a. An input status register which provides information about which boot loader was selected by the processor card switches, the status of memory power, and the status of interrupt mask bit one. An LIA/B 1 or MIA/B 1 is used to load or merge the contents of the input status register into the A or B register.
- b. An output status register which drives seven of the processor card's eight status LEDs and a bank switching bit that selects which 1K of processor card ROM is in use. For processors equipped with 32K ROMs, an additional bank switching bit is provided in the output status register to account for the extra ROM addressing bit. An OTA/B 1 will place the contents of the A or B register into the output status register.

- c. A parity error register which records the address of any word read with a parity error. This register stores the address of every memory read initiated by the processor and holds the address when a parity error is signalled. The register may also be written to by an OTA/B 5 and read from via an LIA/B 5 or MIA/B 5.
- d. A memory protect violation register which records the address of the instruction that violated the memory protect rules. This register also stores the address of every instruction fetch and freezes that information when a memory protect violation occurs. Data may be placed into this register in software by an OTA 7,C or an OTB 7,C. Note that OTA/B 7 without the clear bit, writes to the memory protect fence and not to the violation register. LIA 7,C; LIB 7,C; MIA 7,C; MIB 7,C are used to read from the memory protect violation register.
- e. A central interrupt register which records the select code of the interrupt most recently serviced. This register can also be loaded by OTA/B 4 and read by LIA/B 4 or MIA/B 4 in software.
- f. An interrupt mask register which stores interrupt mask bit one which controls time base generator interrupts. Other bits of the interrupt mask register are on the I/O interface cards. This register is loaded by OTA/B 0 and read by LIA/B 0 or MIA/B 0 in software.

These registers allow many of the system features of the HP 1000 to be included as part of the processor rather than having them occupy separate I/O cards.

Several system level flags are maintained on the processor card:

- a. The interrupt system flag, when cleared, prohibits level three (time base generator and I/O) interrupts.
- b. The interrupt inhibit flag, when cleared, prohibits level two and three (priority, memory protect, power-fail, time base generator, and I/O) interrupts.
- c. The global register flag, when cleared, enables the use of the the global register on the I/O interface cards.
- d. The parity sense flag, when cleared, informs the memory card to use odd parity.
- e. The parity system flag, when set, enables parity interrupts.
- f. The time base generator flag, when set, indicates that 10 msec have elapsed since the last time base tick.

At power-up, the interrupt system, parity sense, parity system, and the time base generator flags are cleared while interrupt inhibit and the global register flags are automatically set.

The processor card registers may be accessed and the system level flags may be modified in software. The commands used are basically the low select code (0-7) I/O group instructions. The processor card I/O state machine utilizes the same protocols used by the I/O interface cards to handshake with the CPU chip. Table 2-1 lists the I/O instructions executed by the processor card.

Table 2-1. Processor Card Instructions

| INSTRUCTION | FUNCTION |
|---|--|
| CLC 0 (Clear Control 0) | Causes system reset (CRS-) |
| STF/CLF 0 (Set/Clear Flag 0) | Turn interrupt system on/off |
| SFS/SFC 0 (Skip if Flag Set/Clear 0) | Skip the next instruction if the interrupt system is on/off |
| OTA/B 0 (Output A/B 0) | Output the A or B register to the interrupt mask register |
| LIA/B 1 (Load Into A/B 1) | Load the A or B register with the contents of the input status register |
| MIA/B 1 (Merge Into A/B 1) | Merge the A or B register with the contents of the input status register |
| OTA/B 1 (Output A/B 1) | Output the A or B register to the output status register |
| STF/CLF 2 (Set/Clear Flag 2) | Disable/enable the global register |
| SFS/SFC 2 (Skip if Flag Set/Clear 2) | Skip the next instruction if the global register is disabled/enabled |
| OTA/B 2 (Output A/B 2) | Output the A or B register to the global register |
| STC/CLC 4 (Set/Clear Control 4) | Set/Clear interrupt inhibit flag |
| SFS/SFC 4 (Skip if Flag Set/Clear 4) | Skip the next instruction if the power is up/going down |
| LIA/B 4 (Load Into A/B 4) | Load the A or B register with the contents of the central interrupt register |

Table 2-1. Processor Card Instructions (Continued)

| INSTRUCTION | FUNCTION |
|---|--|
| MIA/B 4 (Merge Into A/B 4) | Merge the A or B register with the contents of the central interrupt register |
| OTA/B 4 (Output A/B 4) | Output the A or B register to the central interrupt register |
| STC/CLC 5 (Set/Clear Control 5) | Enable/disable parity interrupts |
| STF/CLF 5 (Set/Clear Flag 5) | Generate and detect even/odd parity |
| SFS/SFC 5 (Skip if Flag Set/Clear 5) | Skip the next instruction if even/odd parity is being generated and detected |
| LIA/B 5 (Load Into A/B 5) | Load the A or B register with the contents of the parity error register |
| MIA/B 5 (Merge Into A/B 5) | Merge the A or B register with the contents of the parity error register |
| OTA/B 5 (Output A/B 5) | Output the A or B register to the parity error register |
| CLC 6 (Clear Control 6) | Clear any pending time base generator interrupt request (Also shuts off TBG in chip) |
| STF/CLF 6 (Set/Clear Flag 6) | Set/clear the time base generator flag |
| SFS/SFC 6 (Skip if Flag Set/Clear 6) | Skip the next instruction if the time base generator flag is set/clear |
| LIA/B 7,C (Load Into A/B 7,C) | Load the A or B register with the contents of the memory protect violation register |

Table 2-1. Processor Card Instructions (Continued)

| INSTRUCTION | FUNCTION |
|--------------------------------|--|
| MIA/B 7,C (Merge Into A/B 7,C) | Merge the A or B register with the contents of the memory protect violation register |
| OTA/B 7,C (Output A/B 7,C) | Output the A or B register to the memory protect violation register |
| OTA/B 7 (Output A/B 7) | Output the A or B register to the memory protect fence |

2.4 CPU CHIP FUNCTIONAL THEORY OF OPERATION

The CPU chip handles the majority of the computer's instruction execution duties and provides control signals for the processor card. The names, whether they are input to or output from the chip, and the functions of all chip signals are presented in table 2-2.

Table 2-2. CPU Chip Signal Definitions

| | |
|------------|--|
| BCLK+ | (Input, high true) |
| FULL NAME: | CPU Clock |
| FUNCTION: | Master synchronizing clock for the CPU chip. |

Table 2-2. CPU Chip Signal Definitions (Continued)

| | |
|------------------|---|
| BTN- | (Output, low true) |
| FULL NAME: | Boot Enable |
| FUNCTION: | Asserted to indicate that, for the current memory reference, the CPU is accessing the ROM. |
| FCH- | (Output, low true) |
| FULL NAME: | Fetch |
| FUNCTION: | Asserted to indicate that the current memory access is an instruction fetch. |
| (IA0+) - (IA14+) | (Output, high true) |
| FULL NAME: | Internal Address bus 0 through 14 |
| FUNCTION: | A 15-bit bus used to transfer the address for all memory transfers. |
| (ID0+) - (ID15+) | (Bidirectional, high true) |
| FULL NAME: | Internal Data bus 0 through 15 |
| FUNCTION: | A 16-bit bus used to transfer data into or out of the CPU chip. |
| IIAK+ | (Output, high true) |
| FULL NAME: | Internal Interrupt Acknowledge |
| FUNCTION: | Asserted to indicate that the subsequent non-DMA memory access is an instruction fetch in response to an interrupt. |
| IIOGO+ | (Output, high true) |
| FULL NAME: | Internal Handshake Request Acknowledge |
| FUNCTION: | The I/O handshake request acknowledge signal generated by the CPU. |

Table 2-2. CPU Chip Signal Definitions (Continued)

| | |
|------------|---|
| IIORQ+ | (Input, high true) |
| FULL NAME: | Internal I/O Handshake Request |
| FUNCTION: | I/O handshake signal asserted to indicate that the processor card or an interface card requires CPU chip service. |
| INT+ | (Input, high true) |
| FULL NAME: | Interrupt Request |
| FUNCTION: | Asserted to signal that the processor should service an interrupt upon completion of the current instruction. |
| I/OG+ | (Output, high true) |
| FULL NAME: | I/O Group Instruction |
| FUNCTION: | Asserted after an instruction fetch to signal that the instruction is in the I/O group and references select codes 0, 2, 4, 5, 6, 7, or HLT 01. |
| IPON+ | (Input, high true) |
| FULL NAME: | Internal Power On |
| FUNCTION: | Asserted when all system power voltages have reached their prescribed levels. |
| MEM+ | (Output, high true) |
| FULL NAME: | Memory Request |
| FUNCTION: | Asserted to drive MEMGO- signal to indicate a memory request. |
| MGO- | (Output, low true) |
| FULL NAME: | Memory Go |
| FUNCTION: | Asserted to signal that a memory cycle may begin. |

Table 2-2. CPU Chip Signal Definitions (Continued)

| | |
|------------|--|
| MND+ | (Input, high true) |
| FULL NAME: | Memory End |
| FUNCTION: | When asserted, indicates that the memory cycle is complete. |
| MPF+ | (Output, high true) |
| FULL NAME: | Memory Protect Enabled |
| FUNCTION: | Asserted to indicate that the memory protect system is enabled. |
| MPV+ | (Output, high true) |
| FULL NAME: | Memory Protect Violation |
| FUNCTION: | Asserted to indicate that the current instruction is one that will cause a memory protect violation. |
| READ+ | (Output, high true) |
| FULL NAME: | Memory Read |
| FUNCTION: | Asserted to indicate that the CPU is reading data from the internal data bus (IDB); otherwise, the CPU is driving the internal data bus. |
| SLK- | (Output, low true) |
| FULL NAME: | Slave Acknowledge |
| FUNCTION: | Asserted to acknowledge that the CPU has entered the slave mode. |
| SLV+ | (Input, high true) |
| FULL NAME: | Slave Request |
| FUNCTION: | Driven by a SLAVE- signal from an I/O interface card which is requesting the CPU to enter the slave mode. |

Table 2-2. CPU Chip Signal Definitions (Continued)

| | |
|------------|---|
| TBT+ | (Output, high true) |
| FULL NAME: | Time Base Generator Tick |
| FUNCTION: | Asserted for one cycle of SCLK- to indicate that the time base generator circuitry has counted off 10 msec. |
| TDI- | (Output, low true) |
| FULL NAME: | Temporarily Disable Interrupts |
| FUNCTION: | Asserted to indicate that certain interrupts should be held off. |
| UIT+ | (Output, high true) |
| FULL NAME: | Unimplemented Instruction Trap |
| FUNCTION: | Asserted to indicate an unimplemented instruction has been detected. |

2.4.1 CPU CHIP DATA PATHS

A simplified block diagram of the CPU chip is shown in figure 2-4. The basic operation of the chip is structured around five buses. Internal Bus 2 is the primary data bus and is connected to the external data bus (ID0+ through ID15+). This bus provides one set of 16 input lines to the Arithmetic Logic Unit (ALU). Bus 3 is the internal address bus and is connected to the external address pins (IA0+ through IA14+). Bus 4 provides the other set of 16 inputs to the ALU. The output of the ALU, which is examined by the status logic, feeds the T register and is shown on the diagram as the A bus; the output of the T register is shown as the T bus.

The buses are controlled by the signals shown in figure 2-4. All connections shown in the figure are actually bidirectional transmission gates (some, however, are used only in one direction). B23 connects Bus 2 to Bus 3; this transmission may occur in either direction. B34 performs a similar function for Bus 3 and Bus 4. BT2 and BT4 enable the T bus onto Bus 2 or Bus 4, respectively. R/W (Read/Write) indicates the direction of the data bus drivers. A 1 signifies that the data is driven from the external bus to the internal data bus (Bus 2) and a 0 signifies that the data is driven from the internal bus to the external data bus. The internal address bus (Bus 3) drivers are always enabled to drive the lower 15 bits of this bus onto the external address bus. The signal ZB2 forces zeros on all lines of the internal data bus Bus 2.

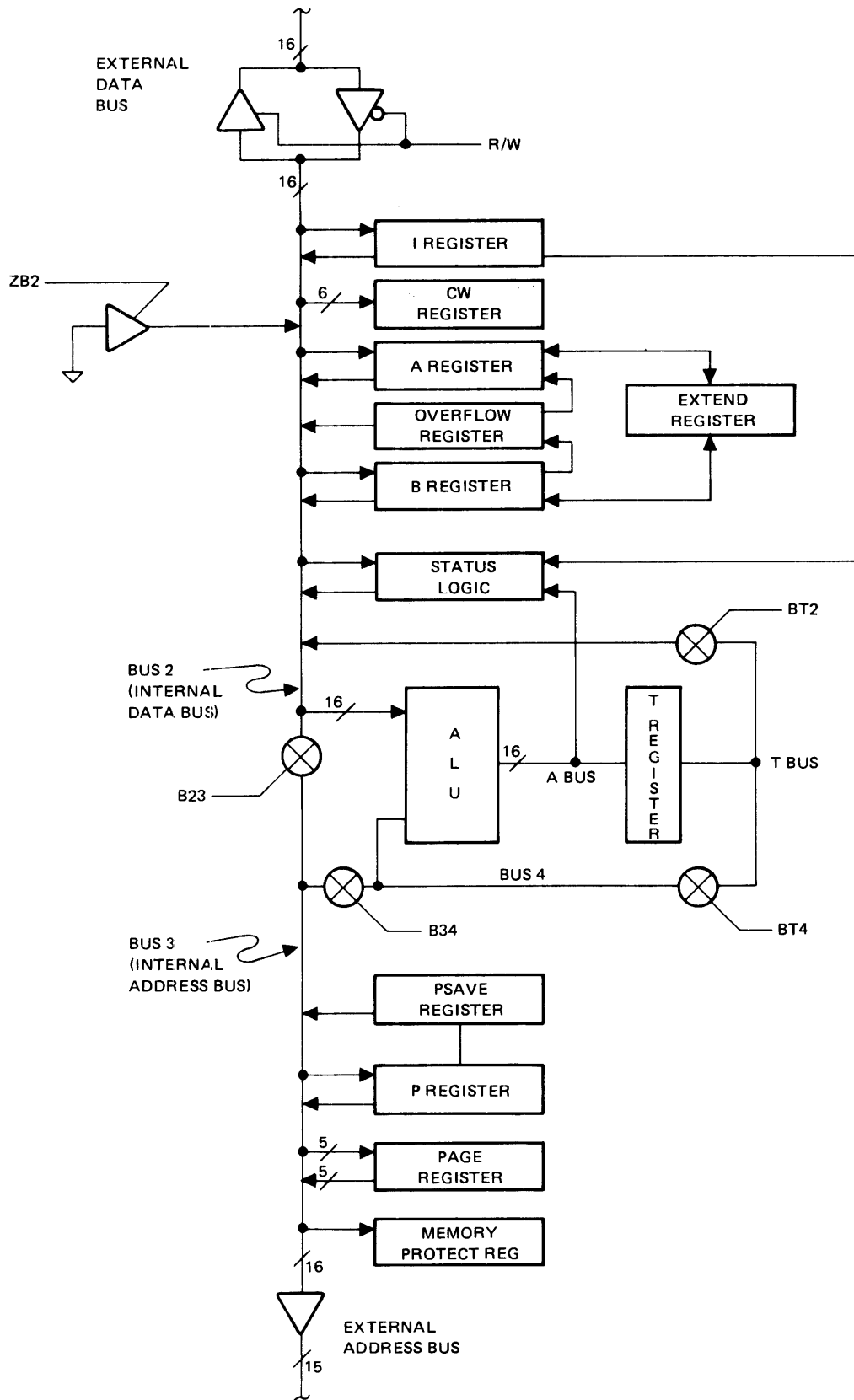


Figure 2-4. CPU Chip Functional Block Diagram

2.4.2 CPU CHIP REGISTERS

2.4.2.1 Instruction Register

The instruction, or I register, reads from and writes onto Bus 2. The I register is a 16-bit latch register which passes data on the signal LDI when the internal clock signal (INTCLK) is high. The four least significant bits of the I register (IR3 - IRO) form a down counter that counts when the signal CLKI is asserted. This 4-bit counter is used to keep track of the number of shifts in the double register shift operations and the number of iterations in the multiply and divide instructions. The I register is not accessible to the programmer.

All 16 bits of the I register go to the IR logic for instruction decoding. When the RDI signal is asserted, bit 15 (direct/indirect) and bits 0 through 9 (page address) of the I register are driven onto their respective bits of Bus 2, and IR10 is driven onto bits 10 through 14 of Bus 2. This allows the page offset in an MRG instruction to be ANDed with the page register (see next paragraph) to generate the effective memory reference address.

2.4.2.2 Page Register

The page register is a 5-bit D flip-flop register used to store the current page address. The five bits are from the program counter. This register is not accessible to the programmer.

In order to form the address desired by the instruction, it is necessary to merge the explicit page address (bits IR9 - IRO) with the page. This is accomplished by ANDing in the ALU, the page register contents and the address contained in the I register. For this reason, when the I register is read onto Bus 2, bit 10 (the bit that specifies zero or current page) is read onto Bus 2 bits 14 through 10 (which are the location of the page bits in the page register). If IR10 is a 1 (current page), the AND in the ALU results in a merge of the explicit and page address information. If IR10 is a 0 (page zero), the AND causes the page bits to be zeroed, resulting in an address which is on page zero.

The operations described above are demonstrated in figure 2-5.

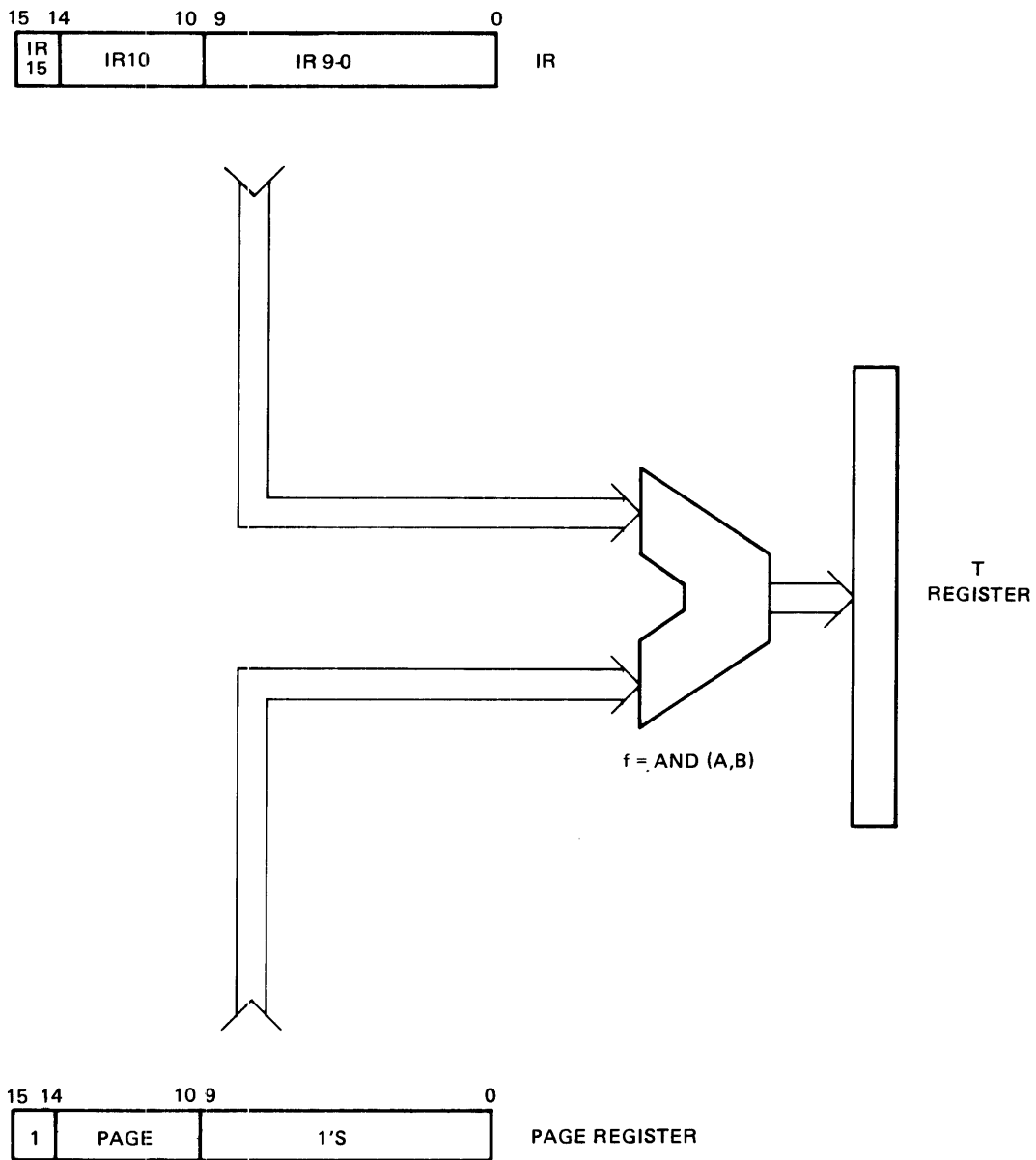


Figure 2-5. ANDing the Page Register and I Register Contents

2.4.2.3 Control Word Register

The control word (CW) register is a 5-bit register that holds the CPU Control Word when the CPU is in slave mode. The CW register bits CW0 through CW4 are loaded from Bus 2 bits 4 through 8, respectively. The CW register is not accessible to the programmer.

In a sense, the CW register is an auxiliary instruction register in that when the CPU is in slave mode, or has just decoded an I/O instruction, the CW register holds the word which specifies which of the I/O operations is to be executed. Additionally, the CW register indicates whether or not the CPU should do another cycle on completion of the current transfer.

Of the five bits in the CW register, four specify the current operation and one signifies looping. The register is loaded or cleared by the LDCW signal on the falling edge of INTCLK. The decision to load or clear depends on whether the signal IIORQ is asserted. If the CPU decodes an I/O instruction which requires interaction between, for example, an I/O card and the CPU, the requesting card generates the IIORQ signal (an I/O handshake signal) and the CW register is loaded. If the CPU decodes an I/O instruction which requires no interaction with the CPU (i.e., STF, CLF, etc.), no card asserts the IIORQ signal and the CW register is cleared.

All zeros in the CW register signify a NOP, no loop, and cause the CPU to fall through the I/O and slave processing states and continue execution.

2.4.2.4 A and B Registers

The A and B registers are the system accumulators. They are 16-bit, bidirectional shift registers which can perform four operations as follows:

- LOAD (from Bus 2)
- SHIFT LEFT 1
- SHIFT RIGHT 1
- SHIFT LEFT 4

Coupled with the shift logic, these four operations can perform all the shift functions required for the L-series instruction set. The A and B registers also serve as operand/accumulator registers for multiply and divide.

The A and B registers are clocked at the end of the state time by the signals ACLK and BCLK. They are enabled onto bus Bus 2 by the signals RDA and RDB.

The A register may be addressed as memory location 00000 (octal) by any Memory Reference Group or Extended Arithmetic Group instruction; the B register may be addressed as memory location 00001 (octal) by any Memory Reference Group or Extended Arithmetic Group instruction.

2.4.2.5 Extend (E) Register

The extend (E) register is a 1-bit register used to link the A and B registers by rotate instructions or to indicate a carry from the most significant bit (bit 15) of the A and B registers by certain arithmetic instructions.

The E register may be set, cleared, complemented, and tested under program control, and may be accessed in slave mode as bit 11 of the status register.

2.4.2.6 Overflow (O) Register

The overflow (O) register is a 1-bit register used to indicate that an arithmetic instruction has caused the A and B registers (accumulators) to exceed the maximum positive or negative number which can be contained in these registers.

The O register may be set, cleared, and tested under program control, and may be accessed in slave mode as bit 6 of the status register.

2.4.2.7 T Register

The T register is a 16-bit temporary holding register connected to the output of the ALU. Because the A and B registers read from and write to the same bus (Bus 2), the results must be stored temporarily to allow the bus to be turned around. This is the function of the T register.

The contents of the T register can be enabled directly onto Bus 2 and indirectly onto Bus 3. Bit 15 of the T register may be examined by the state machine in order to determine status conditions or for making state branches.

The T register is not accessible to the programmer.

2.4.2.8 P Register

The P register is a 16-bit register that holds the program counter during instruction fetches and the memory address for all memory reference instructions. It also provides temporary storage for operands in multiply and divide. The P register is capable of being loaded from Bus 3 and of

incrementing by one. Operation of the register is controlled by the LDINC signal. When LDINC = 1, the P register will drive the bus on the rising edge of CLKP. When LDINC = 0, the register increments (the register is a synchronous counter).

Associated with the P register is logic which notifies the CPU control section when the P register points to the A or B registers. This is important because the handling of references to A and B as memory locations 0 and 1, respectively, are handled differently from references to other memory locations.

2.4.2.9 PSAVE Register

The PSAVE register is a 15-bit register that acts as temporary storage for the current contents of the P register when P is used for other purposes. For example, the P register holds the effective memory address yielded by an MRG when the fetch of the operand occurs and the PSAVE register holds the old P (i.e., the next instruction fetch address). The PSAVE register is a transparent latch register which is loaded directly from the P register and can drive its output onto Bus 3. Because the information that the PSAVE register stores is an address, when reading PSAVE a 0 is driven onto Bus 3, bit 15.

The PSAVE register is not accessible to the programmer.

2.4.2.10 Memory Protect Fence Register

The memory protect fence register is used to define the first word of unprotected memory in the L-Series computer system. All locations greater than or equal to the address stored in the fence are unprotected. The fence is loaded from the A register by the instruction OTA 7 (note that this is specifically not OTA 7,C).

In the L-Series computer system, the fence consists of the 16-bit memory protect fence register and a comparator which looks at the contents of the register and the data on Bus 3. If the address on the bus is less than the value in the register, the signal ADVIO is generated. This signal is clocked into a storage flip-flop (BADVIO) whenever the P register is loaded. Thus, the output of this flip-flop indicates whether or not the address value currently in the P register is one which could potentially cause a violation.

2.4.3 ARITHMETIC LOGIC UNIT

The Arithmetic Logic Unit (ALU) is 16 bits wide and performs all the logical and arithmetic operations necessary for instruction execution. Operations are specified by control bits provided by the control structure and are as follows:

| C1 | C2 | C3 | C4 | C5 | CE | FUNCTION |
|----|----|----|----|----|----|--------------------------|
| 1 | 0 | 0 | X | 0 | 0 | PASS 2 (Pass Bus 2) |
| 0 | 0 | 1 | 0 | 0 | 0 | PASS 4 (Pass Bus 4) |
| 0 | 1 | 1 | X | 0 | 0 | NEGATE (Bus 4) |
| 1 | 0 | 1 | X | 1 | 0 | AND |
| 1 | 0 | 1 | 1 | 0 | 0 | OR |
| 1 | 0 | 1 | 0 | 0 | 0 | XOR |
| 1 | 0 | 1 | 0 | 0 | 1 | ADD |
| 1 | 1 | 1 | 0 | 0 | 1 | SUBTRACT (Bus 2 - Bus 4) |
| 0 | 0 | 1 | 0 | 0 | 1 | INCREMENT (Bus 4) |
| 1 | 1 | 0 | 0 | 0 | 1 | DECREMENT (Bus 2) |
| 0 | 1 | 1 | X | 0 | 1 | COMPLEMENT (2's - Bus 4) |

The ALU generates the Carry Out (COUT) signal if the operation (ADD, SUB, INC, DEC, COMP) generates a carry from the Most Significant Bit (MSB).

2.4.4 STATUS LOGIC

The status logic is random logic used to control the contents of the E and O registers, and to control incrementing of the P register as needed when executing instructions which cause a skip. In addition, the ALU generates the signals ONES and ZEROS if the ALU output is all ones (177777B) or all zeros (000000B), respectively. These are used by the status logic to cause ASG instructions and the ISZ instruction to skip as well as by the state machine for the DIV instruction.

The function to be loaded into the E register is determined by three encoded signals GE1, E2, and E3. These signals specify one of eight operations; they are decoded by the E register in the status area of the CPU. The functions specified by these signals are:

| GE1 | E2 | E3 | FUNCTION |
|-----|----|----|---|
| 0 | 0 | 0 | NOP |
| 0 | 0 | 1 | Load E register depending on IR bits 6 and 7 (PE3, CME, CLE, CCE in ASG). |
| 0 | 1 | 0 | Load E register with the appropriate bit of Bus 2 if an SRG shift with E. |
| 0 | 1 | 1 | Invalid code. |
| 1 | 0 | 0 | Load E register with carry out of ALU. |
| 1 | 0 | 1 | Load E register with control word register, bit 0. |
| 1 | 1 | 0 | Clear E register if IR5, otherwise a NOP. |
| 1 | 1 | 1 | Invalid code. |

The O register is controlled in a similar fashion by signals OVF1, OVF2, and OVF3. The functions specified are:

| OVF1 | OVF2 | OVF3 | FUNCTION |
|------|------|------|--|
| 0 | 0 | 0 | NOP |
| 0 | 0 | 1 | Clear overflow. |
| 0 | 1 | 0 | Invalid code. |
| 0 | 1 | 1 | Clear overflow. |
| 1 | 0 | 0 | Set O if current ALU operation causes an overflow. |
| 1 | 0 | 1 | Set overflow. |
| 1 | 1 | 0 | Set O if current ALU operation causes an overflow. |
| 1 | 1 | 1 | Set O if B215 + B214 is true, otherwise NOP. |

2.4.5 CONTROL STRUCTURE

The CPU control structure is implemented by a synchronous state machine (see figure 2-6). The machine consists of a next state Custom Logic Array (CLA) and associated next state register. These two elements maintain the state of the machine. Corresponding to each state are outputs which are generated by the output CLA. Instruction decoding is performed by the instruction register CIA and IR logic.

2.4.6 NEXT STATE CLA

The next state CLA computes the next state of the CPU based on the present state and various external inputs. The exact next state is generated in one of two forms: it is generated explicitly and loaded into the state register, or the signal INC is generated which causes the register to be incremented. Due to the circuit used to implement the CLA, terms cannot be shared among output functions. Thus, there is one CLA term required for every logic one in each output vector from the CLA. In the general case, then, if a state transition can be made from the present state by incrementing the value in the state register, then only one term is required for that function regardless of how many ones there are in the resulting vector.

2.4.7 NEXT STATE COUNTER/REGISTER

This 6-bit register provides the state storage for the machine. It is clocked on the falling edge of INTCLK and either loads or increments depending on the state of the signal INC. When enabled to increment, the register acts as a synchronous counter.

The carry in to the incrementer is normally high, and when selected the state gets incremented by one. In one case, however, it is necessary to stall the state counter for one state to accommodate a large propagate delay path. In this case, the carry in is zero, the increment adds zero, and the state does not change. The carry in to the incrementer is from a flip-flop clocked on the same edge as the state counter. This flip-flop outputs data ones from the next state CLA.

2.4.8 OUTPUT CLA/OUTPUT CLA LATCHES

The implementation of the output CLA is the same as that of the next state CLA, and, like the next state CLA, the output CLA does not share terms.

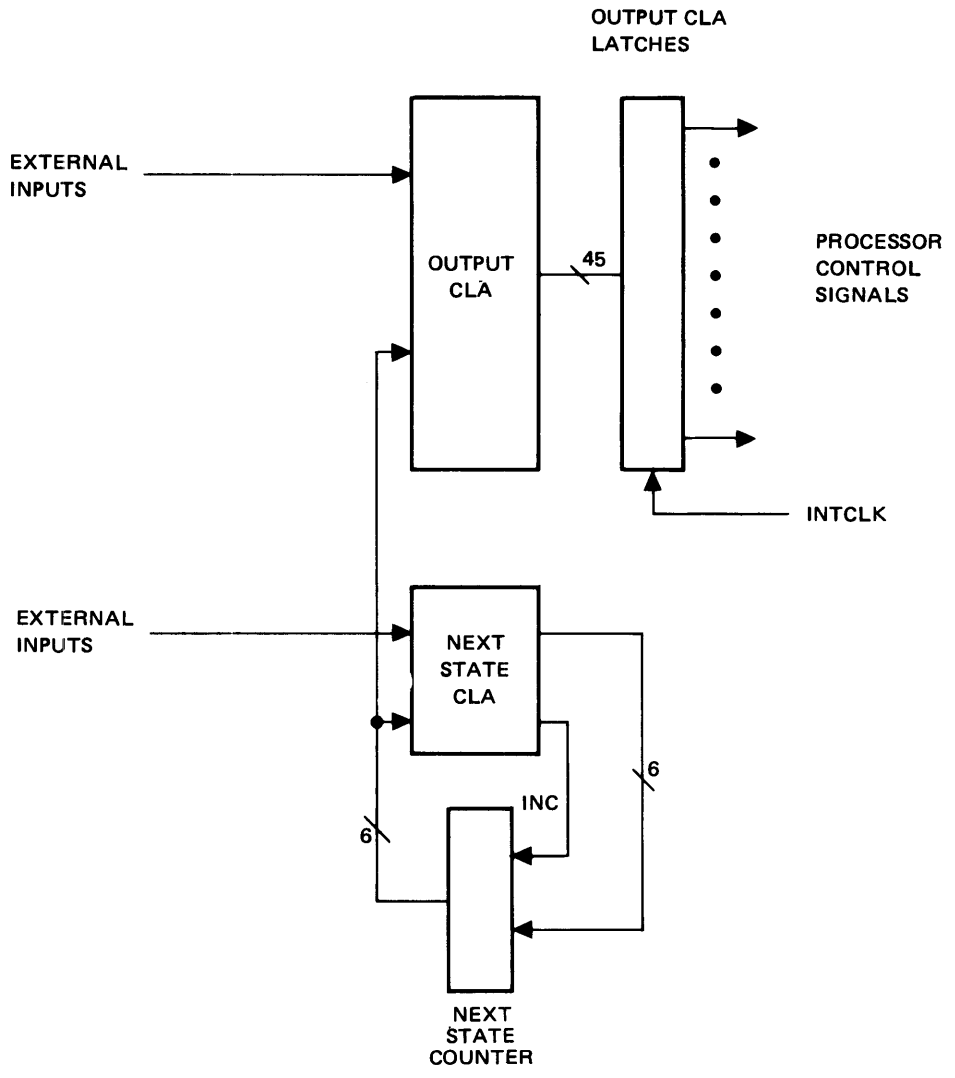


Figure 2-6. CPU Control Structure

The output CLA monitors the contents of the next state register and external (to the state machine) inputs and determines what control signals are necessary for the operation of the data path elements during the next state. The output CLA outputs are stored in latches in order to provide an orderly transition from one state's control signals to the next. The output CLA latches pass data when the INTCLK signal is high.

2.4.9 INSTRUCTION REGISTER CLA

The instruction register CLA performs high level instruction decoding by encoding into four blocks, as follows:

MRG (not A/B addressable)

MRG (A/B addressable)

ASG, SRG, I/O

Extended Arithmetic Unit (EAU)

The instruction register CLA also decodes certain low select code (0 - 7) I/O instructions which are used to control functions within the CPU (i.e., load memory protect fence, clear overflow, etc.).

2.4.10 CPU TIMING

The CPU timing is controlled by a 454 nsec period clock called INTCLK. INTCLK has a 40 percent duty cycle and is illustrated in figure 2-7. This clock defines the basic state time of the processor. Conceptually, a state starts with the rising edge of INTCLK and ends on the following rising edge. Due to the magnitude of the system delays, however, preparation for the current state occurs in the previous state (see figure 2-7).

In figure 2-7, point A marks the beginning of the previous state. The output CIA latches are transparent and the control signals for this state are asserted. Propagation delays through the next state CLA dictate that in order to make a state branch after the current state, all inputs to the next state CIA must be stable at this point.

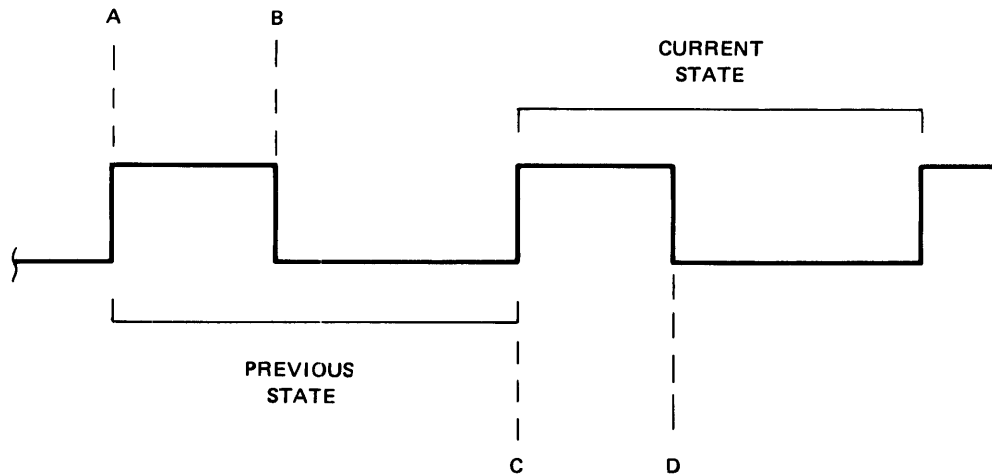


Figure 2-7. INTCLK Clock Timing Diagram

Point B marks the "middle" of the previous state. It is here that P, PSAVE, memory protect fence, and the control word register are clocked and the instruction register latches its data. Also, the next state CLA, given the values of the state variables corresponding to the previous state and the external inputs, has generated the appropriate signals to control the next state counter. Recall that this means that either the explicit values for the state variables corresponding to the current state or the signal INC have been generated. The falling edge of INTCLK loads the appropriate value into the next state counter. Note that the CPU still acts as if it is in the previous state because the defining signals (the outputs of the output CLA latches) remain unchanged. With the appearance of the new state variables at the next state counter's outputs, the output CLA begins generation of the control signals necessary to implement the current state. At this point, the synchronizing flip-flops for the signals PON, INT, and SLAVE are clocked. INT and SLAVE are not clocked in states A and B.

2.4.11 STATE DIAGRAM

The operation of the CPU is illustrated by the state diagram shown in figure 2-8. The basic blocks of this state diagram are shown in figure 2-9. Each state is represented by the rectangle shown in figure 2-9A. The state is denoted by one or two letters, which in the state diagram will replace *i* in figure 2-9A (e.g., state A is indicated by T_a). The rectangle is partitioned into four parts, corresponding to four groups of signals, and any signal that appears in the rectangle always occurs when the machine is in the state. The upper right partition contains all bus control signals, such as R/W, B23, etc. The lower right partition indicates all register controls, such as RDA, INCP, LDPS, etc.

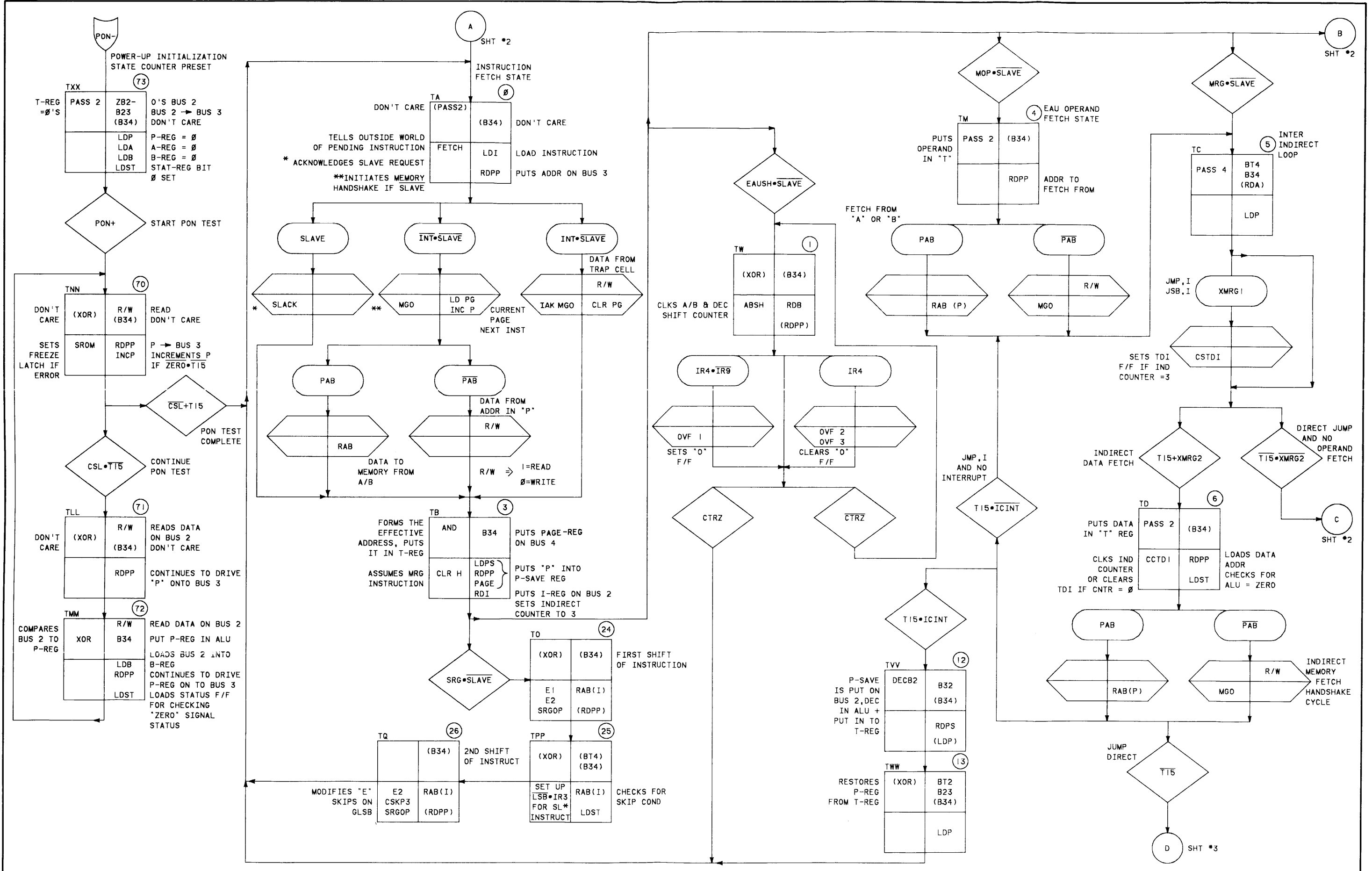


Figure 2-8. CPU Chip State Diagram (Sheet 1 of 3)

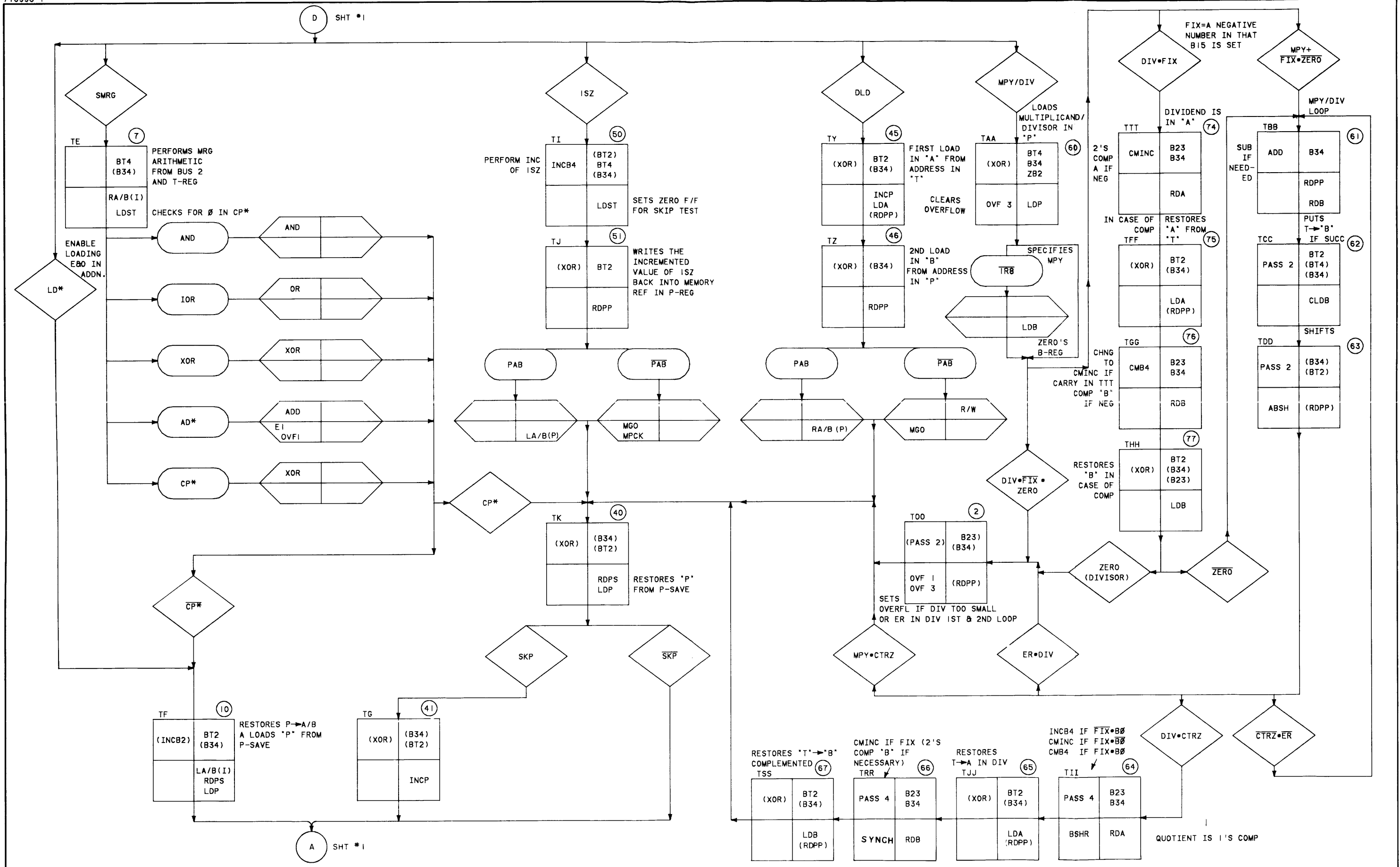


Figure 2-8. CPU Chip State Diagram (Sheet 3 of 3)

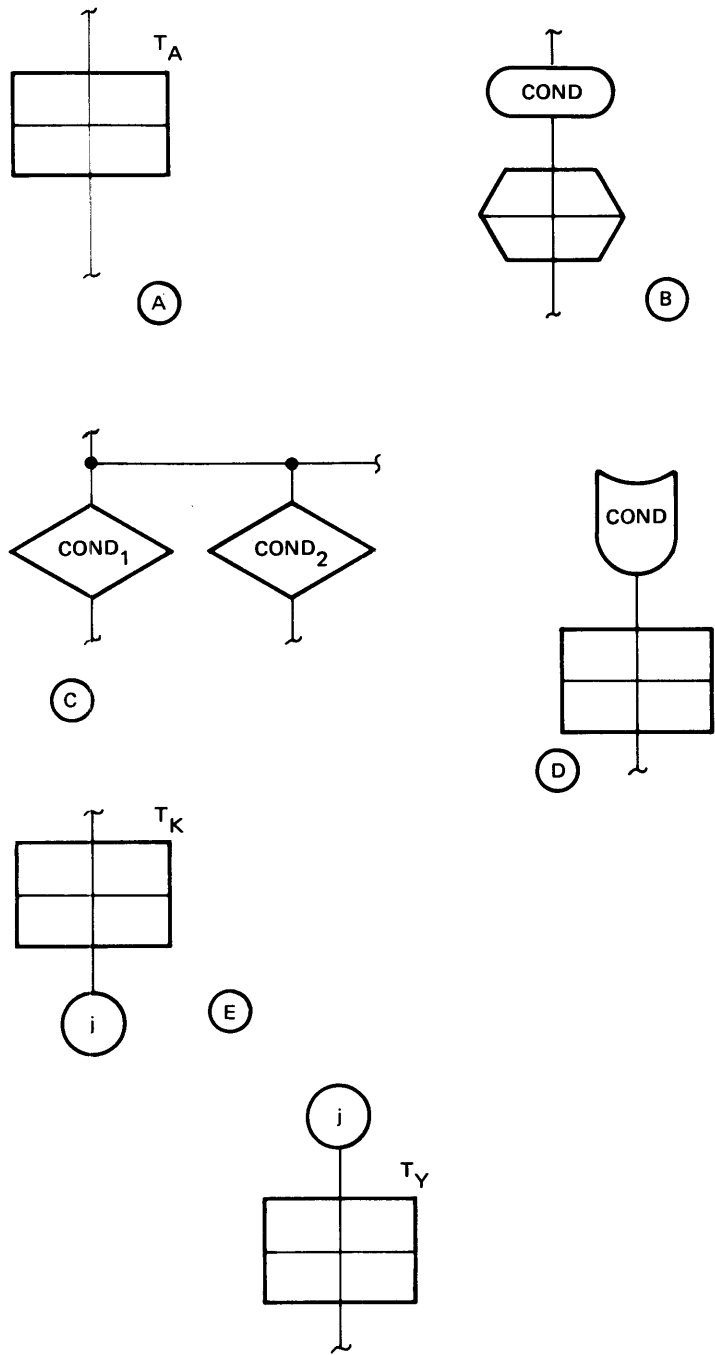


Figure 2-9. State Diagram Blocks

The lower left partition is for miscellaneous control signals; and the upper left partition indicates the ALU function in the state, which, if empty, is a don't care.

The hexagonal structure in figure 2-9B indicates signals that are active in a state only if the signal COND in the oval is true by point B (the middle) of the previous state. The structure in B always directly follows a rectangle, and its signals are conditional in the state of the rectangle so the hexagon has no state symbol. Note that although the hexagonal structures follow the rectangles in the state diagram, this in no way implies time sequencing; that is, conditional signals are asserted at the same time as control signals if their conditioning signal is true.

The diamond in figure 2-9C indicates a state branch condition from the state it follows. The branch is taken if the signal COND is true at point C of the state above the branch, and the set of branch conditions below any state must be mutually exclusive and collectively exhaustive.

Figure 2-9D shows a forcing condition. If COND is true, the state counter is forced to the state below the symbol. The machine remains in this state until the condition becomes false, at which time it enters the state following the forcing condition. All such structures must have conditions which are mutually exclusive.

The structure in figure 2-9E is used for connections from one part of the state diagram to another. There will be at least two such circles with the same letter for j, and they will thus be connected.

The state machine moves from state to state in the diagram as shown by the arrows, diverging at the branching points.

2.4.12 MEMORY PROTECT SYSTEM

The memory protect system provides the capability of protecting a selected block of memory of any size, from a settable fence address downward, against alteration by programmed instructions except those directly involving the A and B registers. Any programmed instruction except JMP may freely address the A and B registers as locations 00000 and 00001 (octal), respectively.

The memory protect logic, when enabled by an STC 07 instruction, also prohibits the execution of all I/O instructions except those referencing I/O select codes 01 and 03. This feature limits the control of I/O operations to interrupt control only. Thus, by programming the system to direct all I/O interrupts to an executive program residing in protected memory, the executive program can have exclusive control of the I/O system.

The memory protect logic is disabled automatically by any interrupt (except when the interrupt location contains an I/O instruction) and must be re-enabled by an STC 07 instruction at the end of each interrupt subroutine.

Programming rules pertaining to the use of memory protect are as follows (assuming that an STC 07 instruction has been given):

- a. Location 00002 is the lower boundary of protected memory. (Locations 00000 and 00001 are the A and B register addresses.)
- b. JMP instructions may not reference the A or B register directly; however, a JSB instruction may do so, and JMP A,I and JMP B,I are legal.
- c. The upper boundary (memory address) is loaded into the fence register from the A or B register by an OTA 07 or OTB 07 instruction, respectively. Memory locations below but not including this address are protected. To execute an OTA 07 or OTB 07, the external logic must perform an I/O handshake with the CPU and pass it the control word 1010 for OTA 07 and 1011 for OTB 07.
- d. Assertion of the signal MPV+ will occur if a JMP, JSB, ISZ, STA, STB, or DST instruction either directly or indirectly addresses a location in protected memory, or if any I/O instruction is attempted (excluding those addressing select codes less than 10 octal). It is up to the processor card logic to generate an interrupt upon assertion of MPV+.
- e. Any instruction not mentioned in step d above is legal even if the instruction directly references a protected memory address. In addition, indirect addressing through protected memory by those instructions listed in step d is legal provided that the ultimate effective address is outside the protected memory area.

The signal MPF+ is asserted whenever the memory protect system is enabled and is used by I/O processors to inhibit execution of I/O instructions. If the instruction causing the memory protect violation is a JMP or JSB, the program counter will be loaded with the new value, and a subsequent JSB will not reveal the address of the violating instruction. If the violating instruction attempts to store into protected memory, the CPU will attempt the write, and it is left to the external logic to insure that no memory contents are altered. The CPU will inhibit execution of any special I/O instruction which causes a memory protect violation.

2.5 PROCESSOR CARD DETAILED THEORY OF OPERATION

The following paragraphs contain detailed theory of operation information for the processor card. Refer, as necessary, to the schematic diagrams (drawing numbers 12001-60001-51, 12001-60001-52, 12001-60001-53, and 12001-60001-54) located at the end of this section.

The processor card acts as an interface between the CPU chip and the L-Series backplane. It plays the role of an arbiter in determining whether the CPU or the I/O interface cards have control of the backplane address and data busses at any given time. This applies to memory accessing as well as interrupt servicing.

2.5.1 MEMORY ACCESSING

The CPU chip initiates all processor accesses to memory. The CPU chip informs the processor by using the MEM+, MGO-, and READ+ memory request signals. The processor card then waits 318 nsec, from the edge which caused the assertion of MEM+, to the assertion of MEMGO- on the backplane. U89.6 is output of the buffer which converts the CPU MEM+ signal to a backplane MEMGO- signal. An open collector buffer was used because any I/O interface may also drive MEMGO- in initiating a DMA cycle. The memory cycle delay (U96 and U105 located at 22A of drawing 12001-60001-52) is necessary to allow time for the address and data busses to be valid on the backplane at the start of a memory cycle.

The CPU chip access of memory may be further delayed if a memory cycle is currently in process due to concurrent DMA activity. U107.13 (at 23B of drawing page 52) determines the go-ahead condition for the processor to start a new memory cycle. Whenever MRQ- or BUSY- are asserted on the backplane, the processor cannot gain control of the backplane busses.

MGO- is used by the processor to set the mycycle flip-flop (U104 located at 25B of drawing page 52) whenever a memory cycle is requested by the CPU chip. Since concurrent DMA may pre-empt a CPU memory request, the processor must keep track of which memory cycles are the result of a processor MEMGO-.

READ+ is used by the processor to control the direction of data flow between the CPU and the backplane. For READ+ de-asserted, a write to memory is desired. U97 (located at 24B of drawing page 52) is an AND-OR-INVERT gate which generates the signal WRITE- for the three cases when it is desired for the processor to drive data onto the backplane data bus. A memory write is one of those cases. The second case involves placing the A or B register

contents on the backplane data bus during the second half of an OTA/B double handshake. The third case is that of an A/B instruction fetch in which the instruction to be executed must be placed on the data bus from "memory" locations 0 or 1, corresponding to the A or B registers respectively.

MEMGO- is the backplane signal used by the memory card or the processor card ROMs to begin a new memory cycle. MEMGO- is asserted at the start of the long half cycle but may be aborted prior to the start of the next short half cycle. For example, the processor card requests a memory cycle with MEMGO-, but MRQ- may be asserted by an I/O interface card, on the same edge of the clock as the MEMGO- assertion, to signal that a DMA memory request is being made. The processor card must yield to DMA by de-asserting MEMGO- as soon as possible.

There are two types of memory accesses. Access to RAM memory on the memory card is mutually exclusive of access to processor card ROM memory. Both DMA and the CPU may utilize the memory on the memory card, but only the CPU has the means for using the processor card ROMs. A backplane signal named MEMDIS- is used by the processor to disable the memory card while accessing ROM. MEMDIS- is asserted only during a processor MEMGO- so that DMA may continue accessing the memory card when the CPU is not accessing memory. The CPU chip determines which memory accesses are referencing ROM by asserting BTN- (boot ROM enable) when MGO- is asserted. The processor card uses BTN- in generating MEMDIS- to disable the memory card, to cause a powered-down ROM to become active, to enable the ROM data buffers, and to allow the ROM memory handshake logic (simulates the memory card's BUSY- and VALID- signals) to begin its sequence.

A long half cycle after the assertion of MEMGO-, the memory card or the ROM handshake logic will respond with the assertion of BUSY- to signal that the memory request has been honored. BUSY- will be asserted by the memory card for two clock cycles, unless a refresh cycle occurs during the current memory access. Concurrent refreshing will add one or two extra states to the duration of BUSY-. In the case of processor ROM accessing, BUSY- is asserted for three clock cycles to allow sufficient time for the 450nsec devices to access data.

During the last clock cycle of BUSY-, a signal called VALID- is asserted to indicate the presence of valid data on the rising edge of VALID-. This is true for both a memory read or an instruction fetch from either the memory card or the processor ROMs. VALID- is used by the processor card to generate the signal to clock the data-in register, to cause the assertion of MND+ (CPU memory cycle end) to inform the CPU chip that the requested data is ready, and to turn off the mycycle flip-flop.

The basic memory cycle begins with MEMGO- and leads to a response of BUSY- and VALID- from the memory card controller or from the processor ROM accessing logic. With the assertion of several other control signals, such as WRITE- and MEMDIS-, during the memory reference, many variations of the basic memory cycle may be created. The following paragraphs and timing diagrams will describe each of these variations. It will be assumed that the processor accesses to memory will occur immediately following a DMA cycle to show how

DMA and the processor interleave memory cycles. In the absence of DMA, the portions of the given waveforms left of the assertion of MEMGO- should be in their de-asserted or tri-stated levels.

2.5.1.1 Memory Data Read

Figure 2-10 is a timing diagram of the backplane signals for a memory data read initiated by the processor card. The processor sends the address to the memory card during the assertion of MEMGO-. Note that WE- (write enable) is de-asserted during MEMGO- to inform the memory card that data is to come from the memory card. WE- is the buffered version of WRITE- discussed above. The requested data is available at the rising edge of VALID-. If a parity error occurs during this memory read, the PE- (parity error) signal will be asserted during the time that data is valid on the backplane.

2.5.1.2 Memory Write Initiated by the Processor Card

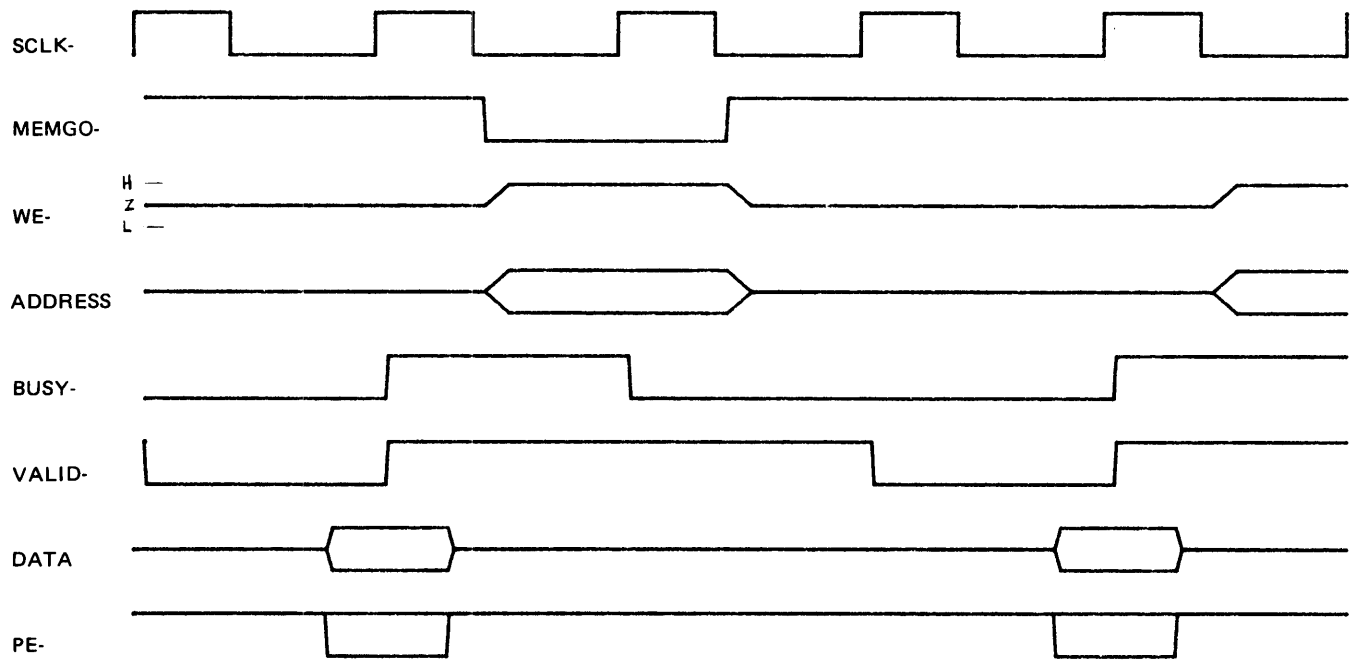
The backplane timing diagram for a memory write initiated by the processor card is shown in figure 2-11. In a memory write, the WE- signal is asserted and the data to be written into memory must be available on the backplane during MEMGO-.

2.5.1.3 Instruction Fetch from Memory

The backplane timing diagram for an instruction fetch from memory is shown in figure 2-12. The set of waveforms appear similar to that for a memory read except that the backplane signal RNI- (read next instruction) is asserted by the processor during the time that BUSY- is asserted. The RNI- signal is the bus-arbitrated form of the CPU chip's FCH- (instruction fetch) signal. Upon the assertion of RNI-, all I/O processors are forced to examine the data bus during that memory cycle to interpret the instruction.

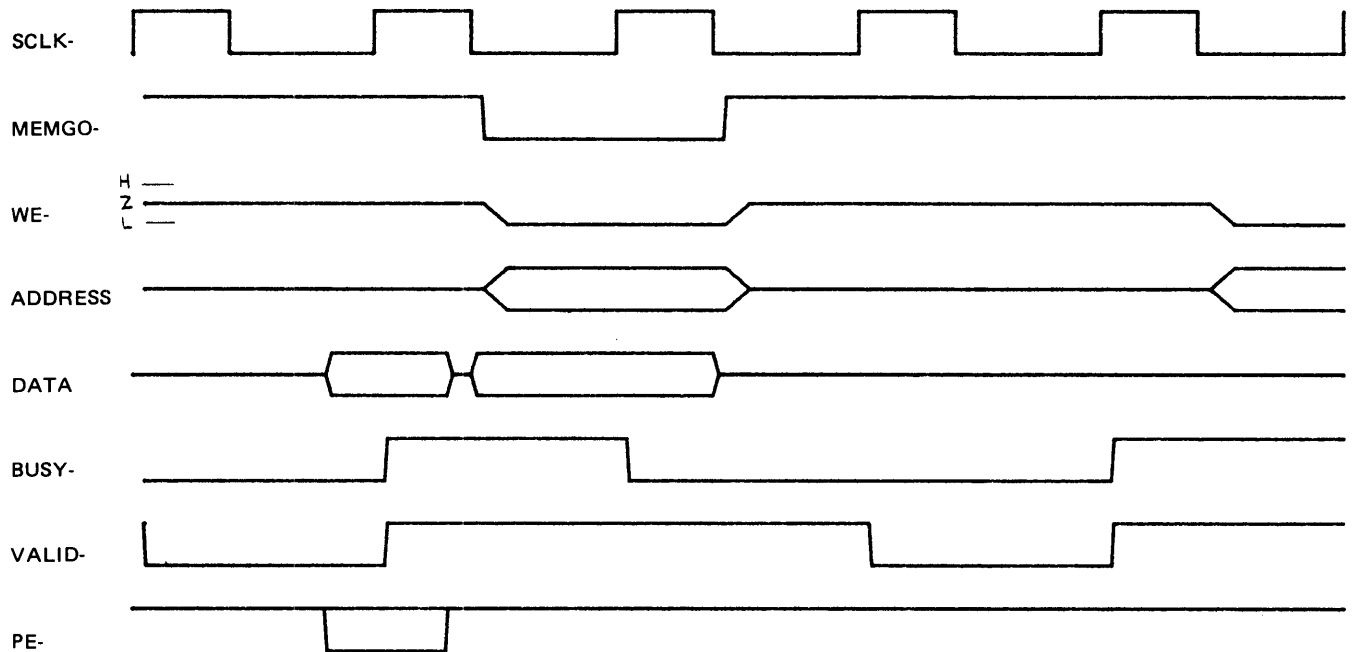
2.5.1.4 Instruction Fetch from the A or B Registers

Figure 2-13 contains the backplane timing diagram for an instruction fetch from the A or B registers. The A and B registers are treated as memory locations 0 and 1 respectively. If the program counter was pointing to either 0 or 1, the data in the A or B register will be treated as an instruction. In this case, neither the processor card ROMs nor the memory card is being



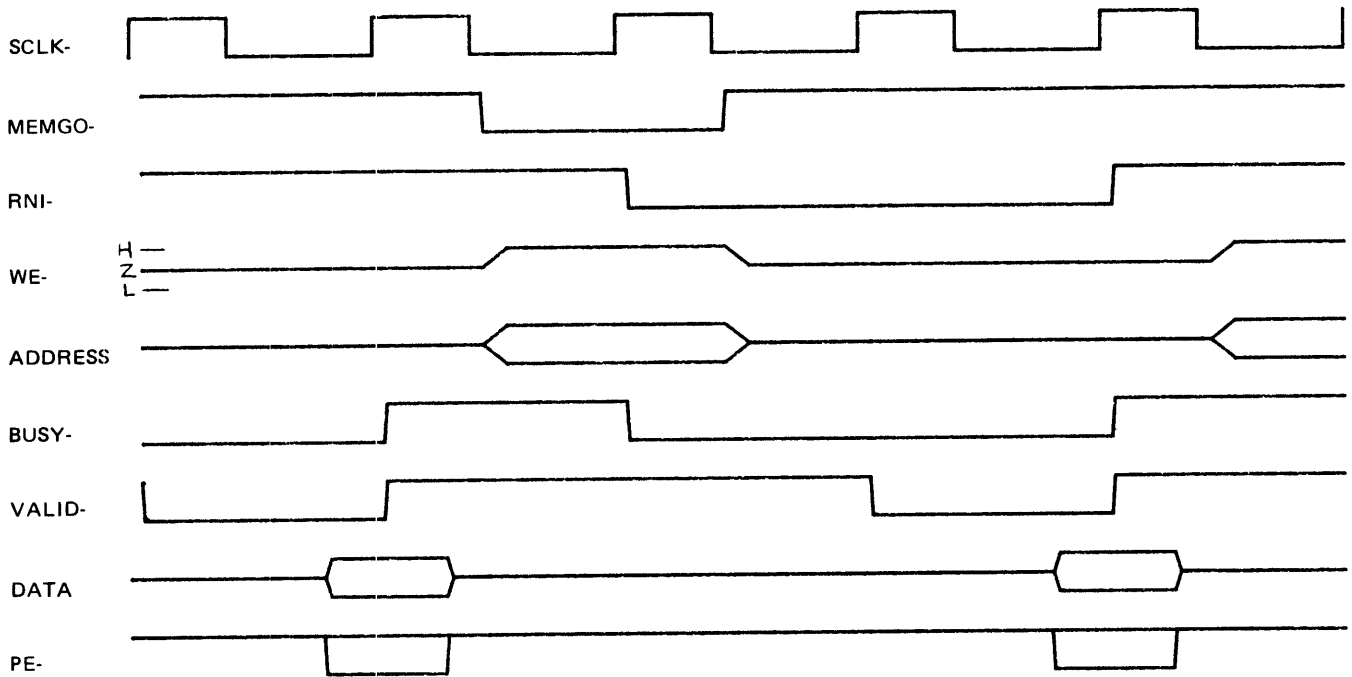
NOTES: MEMGO- occurs after completion of the current DMA cycle.
 WE- is HI during MEMGO-.

Figure 2-10. Memory Read Initiated by the Processor Card



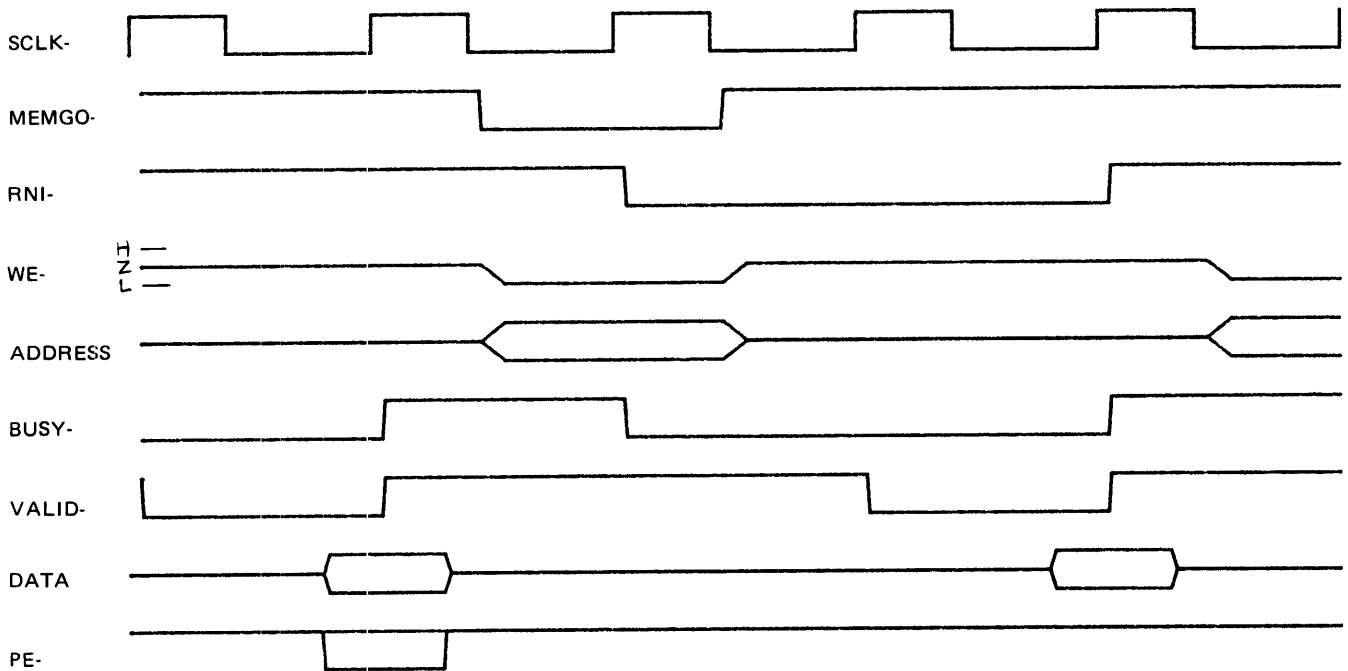
NOTES: MEMGO- occurs after completion of the current DMA cycle.
 WE- is asserted during MEMGO-.

Figure 2-11. Memory Write Initiated by the Processor Card



NOTES: MEMGO- occurs after completion of the current DMA cycle.
 RNI- asserted before and during VALID-.

Figure 2-12. Instruction Fetch from Memory



NOTES: MEMGO- occurs after completion of the current DMA cycle.
 WE- asserted during MEMGO-. RNI- asserted before and during VALID-.

Figure 2-13. Instruction Fetch from the A/B Register

accessed so the problem arises as to how a memory cycle can be generated such that the I/O processors can treat an A/B instruction fetch like any other instruction fetch. To signal that an A/B instruction fetch is occurring, the CPU chip leaves its READ+ signal de-asserted while asserting FCH-. This forces the processor card to initiate a memory write into the memory card's locations 0 or 1. This action causes the appropriate memory handshake to be generated. Since the memory card does not drive the data bus on the rising edge of VALID- for a memory write, the processor card will drive the contents of the A or B register onto the backplane data bus at that time. Since RNI- has been asserted during the entire memory cycle, the overall result appears just like a regular instruction fetch from memory.

2.5.1.5 ROM Data Read

Figure 2-14 contains the backplane timing diagram for a ROM data read. The backplane memory handshake resembles that of a memory read from RAM with the addition of the MEMDIS- signal. MEMDIS- prevents the memory card from responding to the current MEMGO-. The processor card generates MEMDIS- from the presence of BTN- at the CPU chip output.

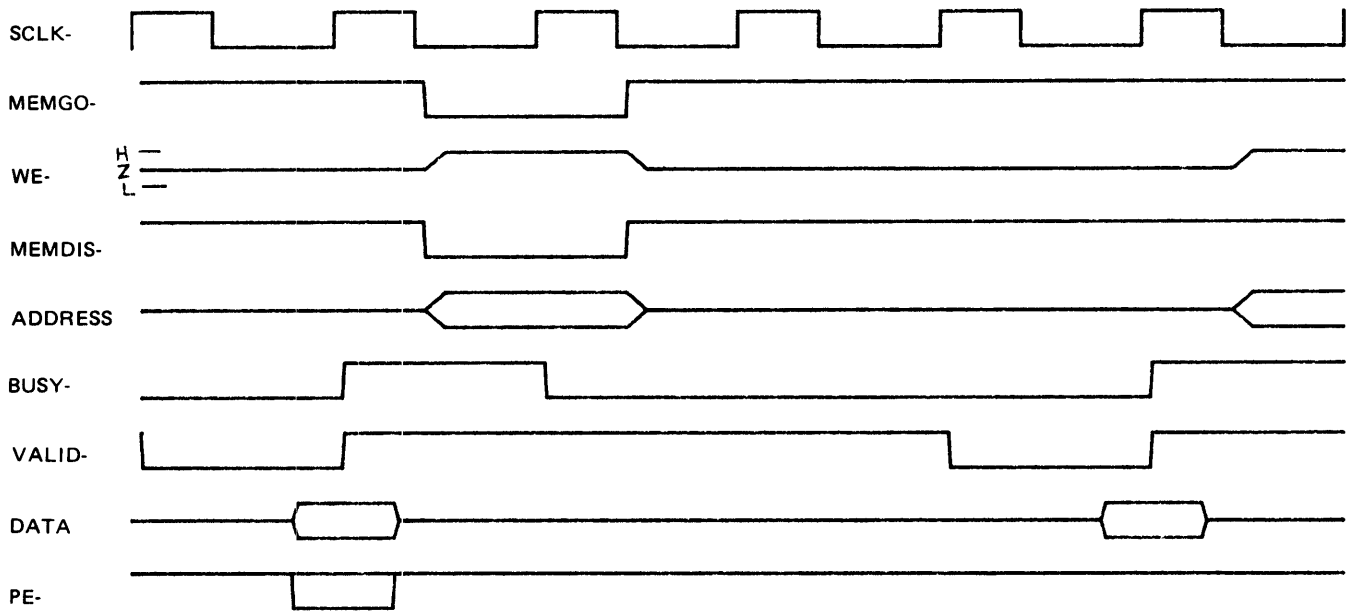
2.5.1.6 Instruction Fetch from ROM

The backplane timing diagram for an instruction fetch from ROM is shown in figure 2-15. The only difference between an instruction fetch from ROM and an instruction fetch from memory is the assertion of MEMDIS- during MEMGO-.

2.5.2 PROCESSOR MEMORY ACCESS AND DMA

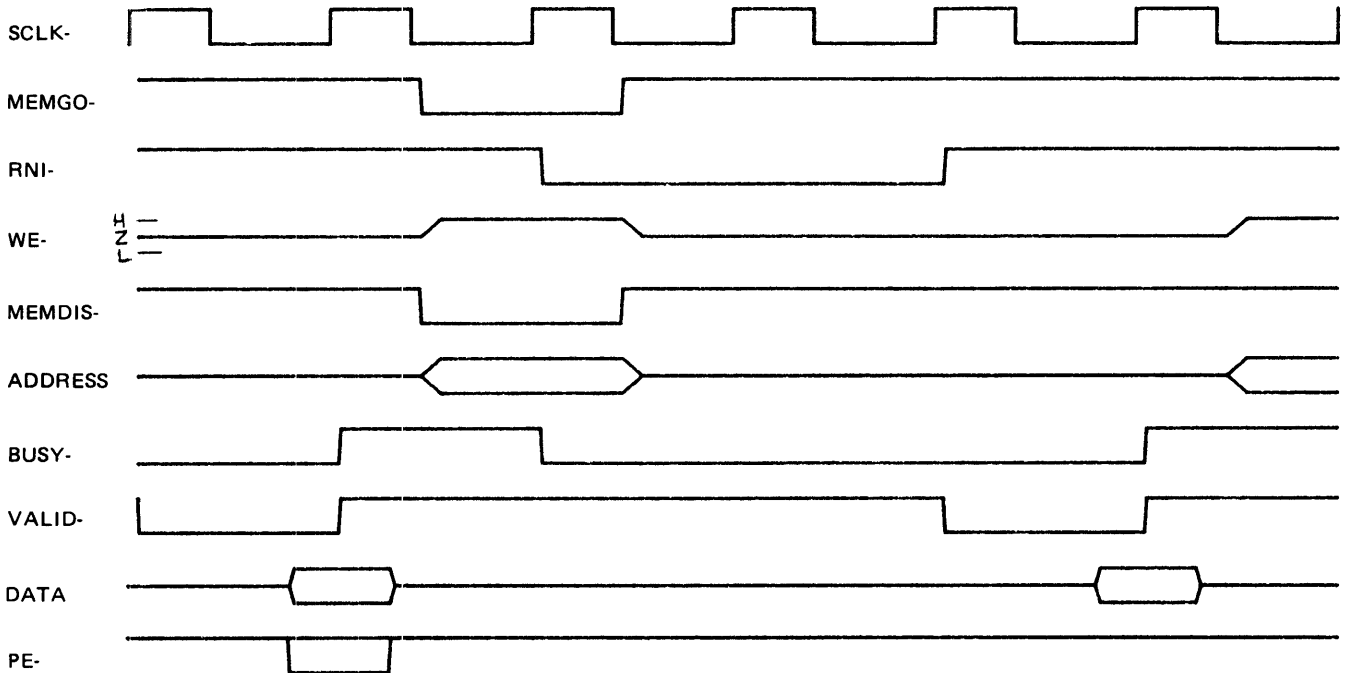
In normal operation, the processor card is the lowest priority memory requestor. It can only obtain a memory cycle when all pending DMA requests have been serviced. Thus, it is conceivable for the CPU to be frozen for long periods of time if considerable DMA activity was stealing every memory cycle from the CPU. Although no L-Series I/O interface card has a DMA bandwidth high enough to saturate the backplane memory bandwidth, several of these cards, each performing DMA, could monopolize the backplane. This condition is unfavorable in achieving reasonable interrupt latency or performing a power-fail routine before power goes down.

The processor card resolves this problem using a DMA memory cycle counter to force the I/O interfaces to give the CPU one memory cycle after a number of consecutive full-bandwidth DMA memory cycles. For example, suppose the CPU



NOTES: MEMGO- occurs after completion of the current DMA cycle.
MEMDIS- asserted during MEMGO-.

Figure 2-14. ROM Data Read



NOTES: MEMGO- occurs after completion of the current DMA cycle.
MEMDIS- asserted during MEMGO-. RNI- asserted before and during VALID-.

Figure 2-15. Instruction Fetch from ROM

just fetched an instruction not affecting the I/O interfaces. Shortly after the de-assertion of RNI-, the I/O cards will begin DMA memory cycle stealing. Suppose that every memory cycle was taken by DMA and that the processor wanted a memory cycle (for the operand of the current instruction or for the next instruction fetch) after the fifth DMA memory cycle. U73 (located at 25A of drawing number 12001-60001-52) is a dual four-bit binary counter hardwired to signal that thirty-two consecutive DMA memory cycles has occurred since the CPU desired a memory cycle. At that time, a signal called CPUTURN- is asserted on the backplane to command the I/O processors to grant a memory cycle to the CPU. The counter is reset after the CPU is granted the memory cycle. In addition to this special case, CPUTURN- is also asserted with every instruction fetch, at the same time as RNI-.

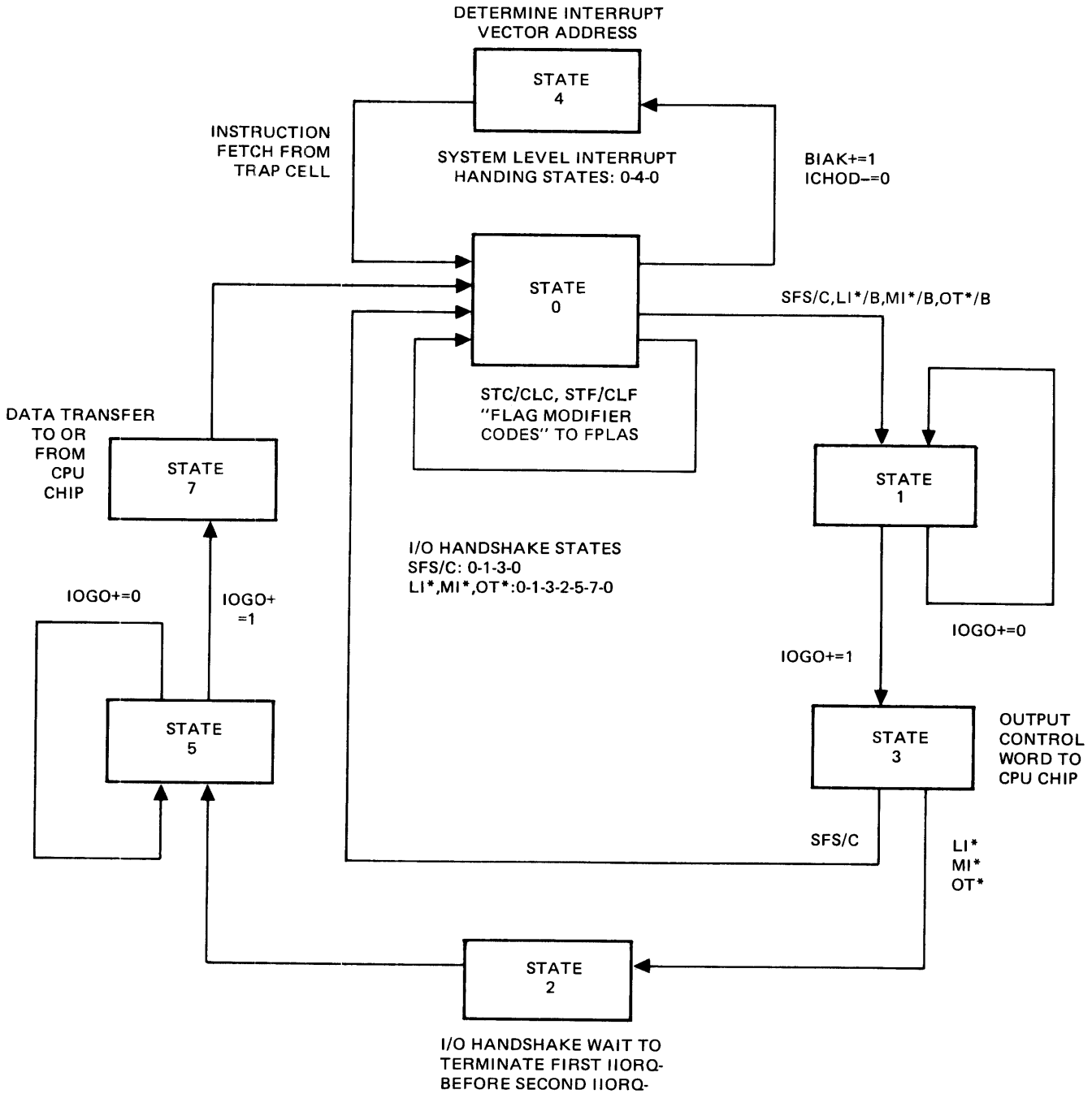
2.5.3 I/O STATE MACHINE

Management of many of the low select code I/O functions centers around four field programmable logic arrays (FPLA's). These IC's are U13, U15, U33, and U35 on drawing number D-12001-60001-53. U35 performs instruction decoding, determines interrupt priorities, generates the next machine state, and outputs commands to control other IC's. U33 and U13 form a large register which stores flag status information for the low select codes. The flags in these two FPLA's are changed generally in response to a "flag modifier code" generated by U35 and transmitted over the five bit processor I/O control bus (QD0-4). U15 is the interrupt status FPLA which determines if a pending interrupt may become an interrupt request.

The processor card has an eight bit instruction register which contains enough bits to identify the type of I/O instruction to be performed and the select code affected. Like the instruction register in the CPU chip and on the I/O interface cards, this register is updated with every instruction fetch. The instruction is passed to the master FPLA U35 through data selectors. The output of these data selectors is typically the contents of the instruction register except during interrupt processing. Thus, half of the inputs to the master FPLA are devoted to examination of the instruction.

While monitoring the instruction stream, the master FPLA determines whether a low select code flag is to be altered or an I/O handshake is required to interact with the CPU chip. Instruction decoding always occurs when the present state of the FPLA sequencer is in state zero (S2,S1,S0 state variables = 000). Register U53 is clocked with SCLK+, making the master FPLA U35 a synchronous state machine with three state variables and five output variables. This FPLA is coded such that the the odd states (where S0=1) are the I/O handshake states.

Suppose a STC/CLC or STF/CLF instruction appeared during the course of program execution. Since only the least significant three bits of the select code are revealed to the master FPLA, the state machine does not have the ability to



NOTES: IIORQ- IS ASSERTED DURING ODD STATES (1, 3, 5, 7)
 THE FPLA STATE MACHINE ON THE PROCESSOR CARD ONLY
 HANDLES CERTAIN INTERRUPTS AND I/O INSTRUCTIONS OF
 SELECT CODE 17 OCTAL OR LESS

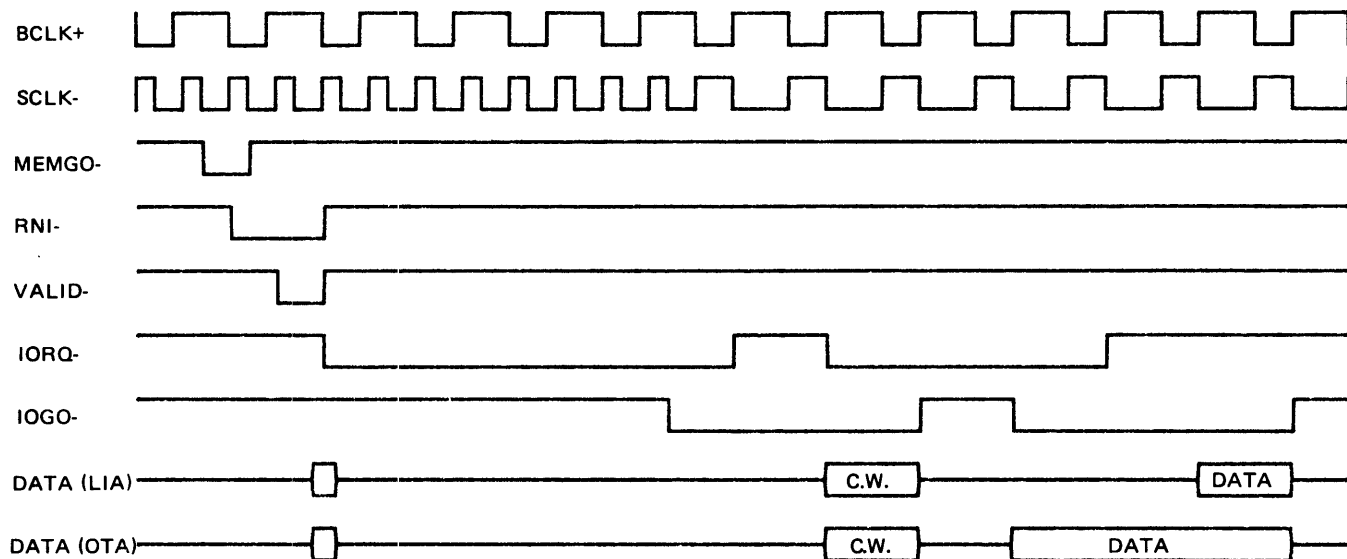
Figure 2-16. State Transition Diagram for FPLA U35

decipher whether or not the I/O instruction affected select codes 0-7 octal or 10-77 octal. Since the CPU chip has a complete 16-bit instruction register, it is able to identify whether select codes 0-7 are affected, and if so, it asserts the IOG+ control signal to the processor card I/O state machine. Following the assertion of IOG+, the state machine examines the STC/CLC or STF/CLF instruction and places a "flag modifier code" on the QD bus to update the appropriate status flag in the low select code flag status FPLA's U13 and U33. The state machine remains in state zero.

As soon as the master FPLA receives a SFS/SFC instruction, it requests flag status information from the flag status FPLA's. FPLA U13 responds by sending a logic "1" to the master FPLA via the FLG+ signal if the appropriate flag is set. The master FPLA utilizes this bit of information to determine if the conditional skip is true. If a skip is to be performed, the master FPLA makes a transition to state one after receipt of IOG+ from the CPU chip. Since state variable S0 is now a 1, IIORQ-, the I/O handshake request to the CPU, gets asserted. The state machine idles in state one until it receives IOGO-, the I/O handshake acknowledgement signal from the CPU chip. The state machine proceeds to state three, at which time it sends the "INC P" (increment program counter) control word to the CPU chip to implement the skip. The state three condition is decoded by a 3 to 8 decoder U52 and is used to enable the control word onto the data bus one cycle later. The state machine returns to state zero, which effectively removes IIORQ-.

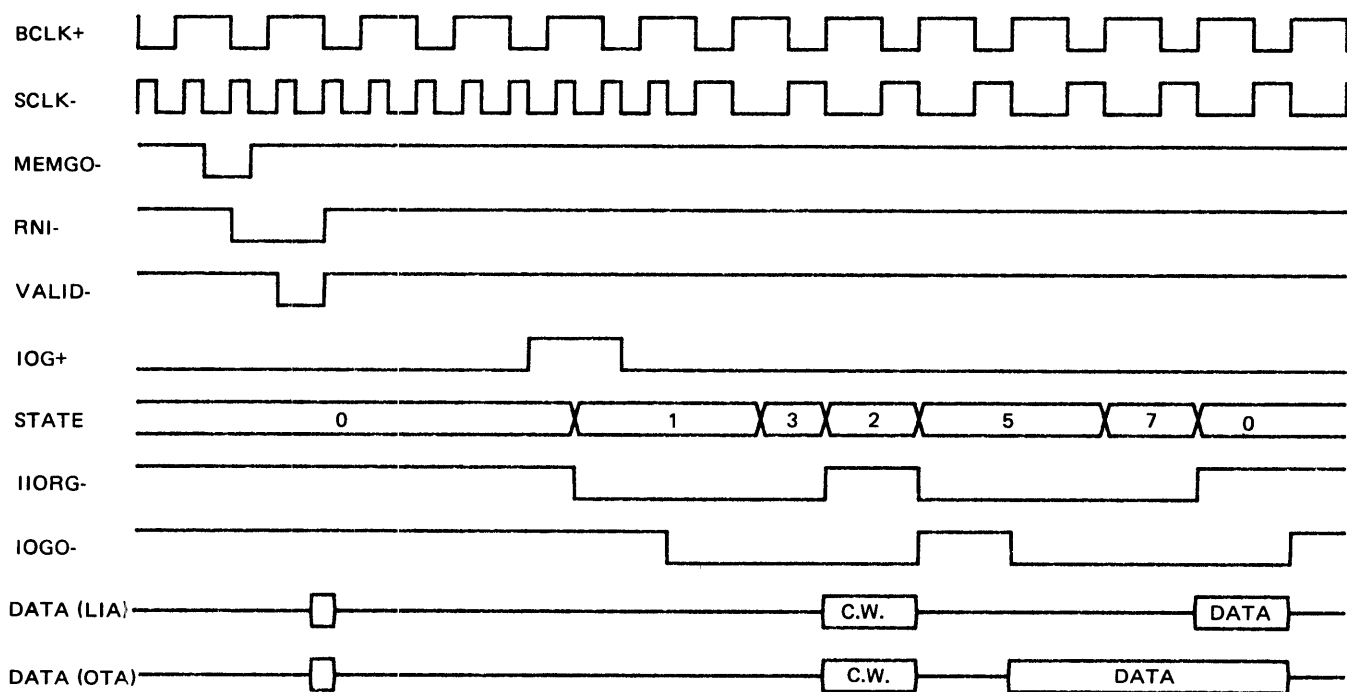
Instructions such as LIA/B, MIA/B, and OTA/B for the low select codes involve data transfers between the A or B registers in the CPU chip and data registers on the processor card or global registers on the I/O interface cards. For these instructions, the first IIORQ-/IOGO- handshake proceeds in the same fashion as for a true conditional skip except that a different control word is passed to the CPU chip. That control word will inform the CPU chip of the direction of the data transfer and what to do with the data if the A or B register is the destination of the transfer. To implement the double handshake, the state machine makes a transition from state three to state two instead of going to state zero. It remains in state two for one cycle of the clock before going on to state five to re-assert IIORQ-. After an IOGO-response is received, the state machine proceeds to state seven for one clock cycle before returning to state zero. If the instruction was an LIA/B or MIA/B, the master FPLA would direct the register selector U22 (3 to 8 decoder) to enable the output control of the appropriate register during the second half of the double handshake. For an OTA/B instruction, another 3 to 8 decoder (U23) serves to generate the latch signal for the appropriate processor card register to load data from the address bus at the end of the second I/O handshake.

Refer to figure 2-17 for a timing diagram showing the backplane I/O handshake protocols between an I/O interface card and the CPU. The state transition of the processor card I/O state machine is shown in the time domain in figure 2-18. The backplane protocols for an I/O handshake are the same for either case. Note how the state machine transitions relate to the other signals.



NOTES: For a true conditional skip, omit the second set of IORQ-/IOGO- handshakes.

Figure 2-17. I/O Handshake for an OTA/B, MIA/B, or LIA/B Instruction



NOTES: For a true conditional skip, omit the second set of IIORQ-/IOGO- handshakes.

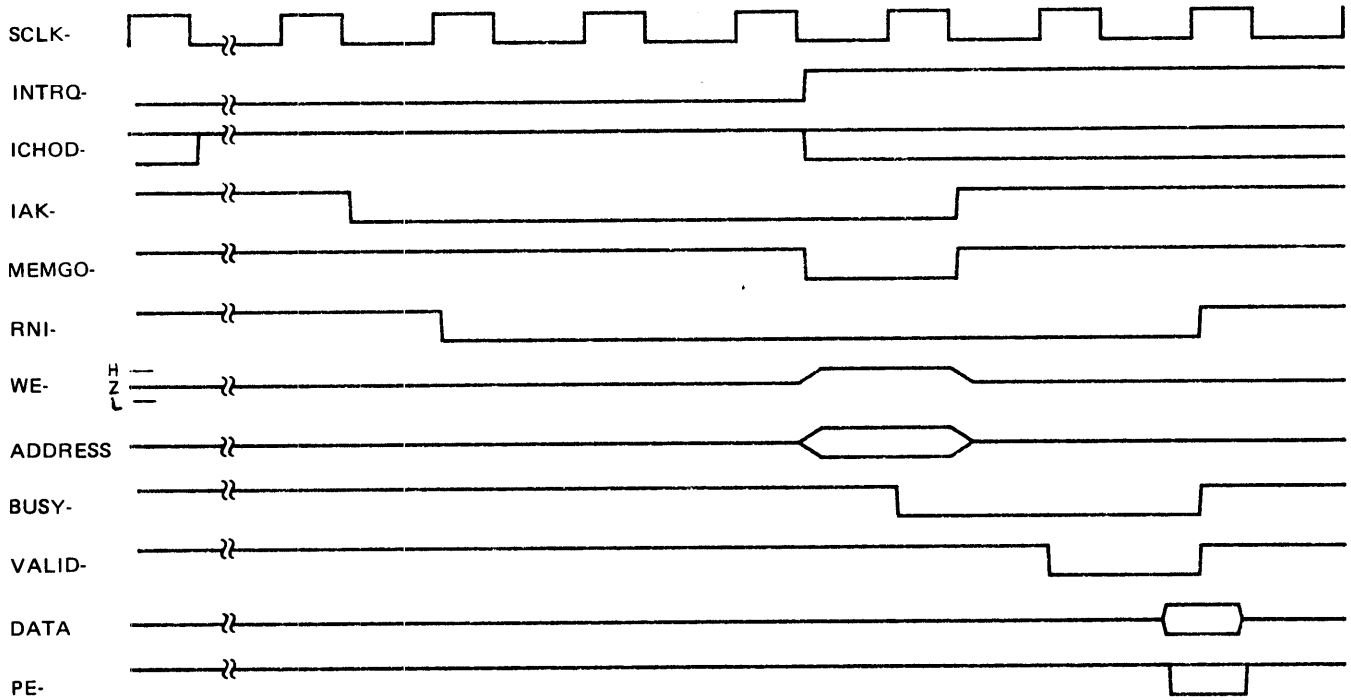
Figure 2-18. I/O Handshake for an I/O Instruction Handled by the Processor

During an I/O handshaking process, the backplane clocks SCLK- and FCLK- are reduced in frequency to match that of the CPU chip's clock. Since the CPU chip expects data transfers to occur relative to its own clock, all external clocks must be identical to the CPU chip's clock during the course of an I/O handshake. A detailed discussion of the L-Series clocks appear in section 2.5.6.

The master FPLA also handles interrupt processing for all system level requests. When an interrupt is acknowledged by the CPU, the master FPLA begins to examine the pending interrupts rather than interpret instructions. Data selectors U25 and U24 are used to switch between instruction and pending interrupt information. The state machine goes to state four to determine the highest priority pending interrupt and generate the vector address at which interrupt servicing begins. The presence of state four is detected by U52 (3 to 8 decoder) and is used to enable the interrupt address onto the backplane at buffers U19 and U28 (see drawing D-12001-60001-51) and to assert MEMGO- to begin the memory cycle. The state machine returns to state zero after one clock cycle at state four.

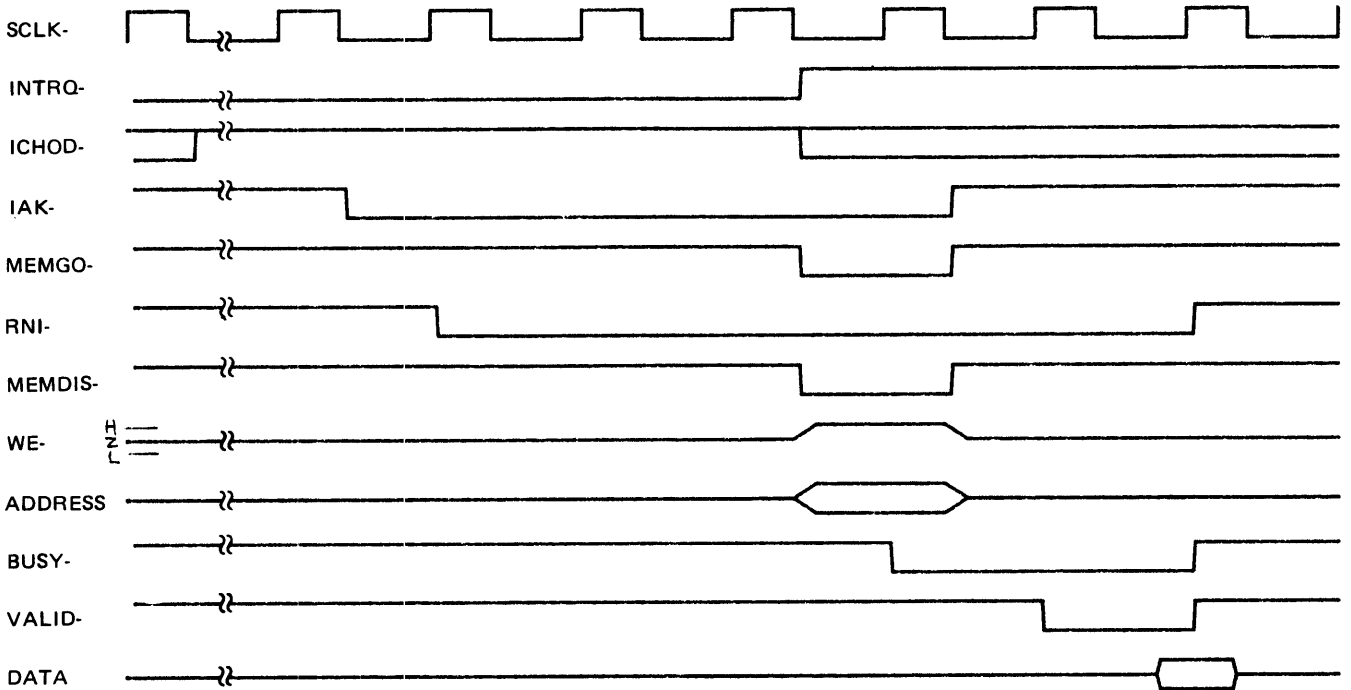
Figure 2-19 shows an I/O interrupt serviced with the trap cell fetch from main memory. INTRQ- (interrupt request) is asserted by an I/O interface card to request an interrupt. When IAK- (interrupt acknowledge) is received by the I/O card and ICHOD- (interrupt disable output of the next highest priority I/O card) is de-asserted, that I/O card will assert MEMGO- and drive its select code onto the address bus as the vector address of the trap cell fetch. This memory cycle is an instruction fetch because the processor card has provided for the assertion of RNI- on the backplane. Figure 2-20 is a timing diagram for an I/O interrupt service from processor card ROM. The only difference is that MEMDIS- is asserted on the backplane to disable main memory during this memory cycle.

Figure 2-21 is a timing diagram for service of a system level interrupt from main memory. There are no backplane interrupt requests because all of the system level interrupt requests are generated by the processor card. When IAK- appears on the backplane, it is accompanied with the assertion of ICHOD- by the processor card. This disables the highest priority I/O interface card from responding to IAK-, which in turn, effectively disables all I/O cards from responding because of the interrupt priority chain. One clock cycle after the master FPLA goes into state four, a signal called VAEN- (vector address enable) is asserted. State four is decoded by U52 (located at 32B of drawing 12001-60001-53), then delayed one clock cycle by U42 (located at 33B of the same drawing), then becomes VAEN-. The vector address is determined by the master FPLA during state four but is not available on the QD bus until the following clock cycle. The VAEN- signal is used to cause the assertion of MEMGO- and to simultaneously enable the vector address buffers onto the backplane address bus. The memory cycle is an instruction fetch since RNI- is also asserted. Figure 2-22 shows the timing diagram for the service of a system level interrupt from ROM.



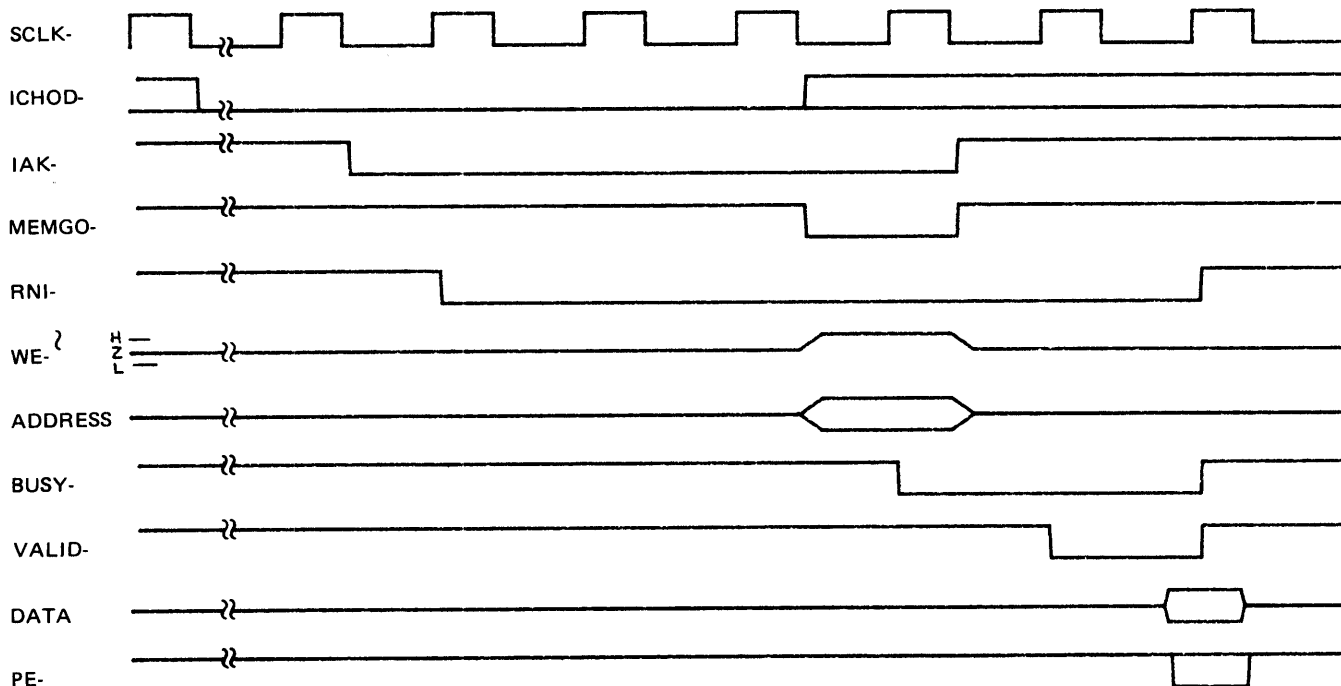
NOTES: ICHOD- is de-asserted so that the interrupting I/O card can assert MEMGO- and provide the vector address (its select code) following the assertion of IAK-.

Figure 2-19. Service of an I/O Interrupt



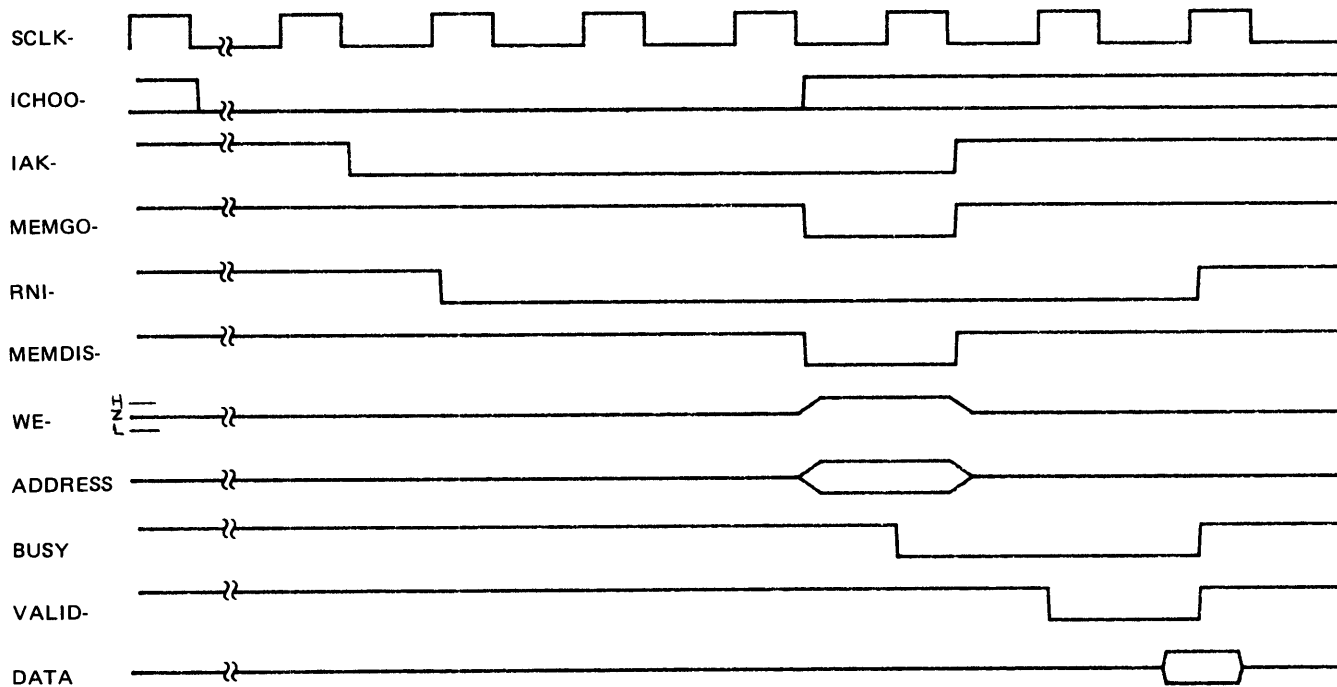
NOTES: Same as above except that MEMDIS- is asserted to select ROM.

Figure 2-20. Service of an I/O Interrupt in ROM



NOTES: ICHOD- is asserted to disable I/O cards from responding to IAK-. The processor card asserts MEMGO- and provides the vector address.

Figure 2-21. Service of a System Level Interrupt



NOTES: Same as above except that MEMDIS- is asserted to select ROM.

Figure 2-22. Service of a System Level Interrupt in ROM

FPLA's U33 and U13 contain the low select code flag status information. The master FPLA executes the STC/CLC and STF/CLF instructions by generating five-bit codes informing U33 and U13 how to modify one of their status flags. Flag status can only be altered during state one when EN+ is high, corresponding to the short half cycle of SCLK+. Some flags may be altered at any time in response to directly hardwired signals. A summary of the operation of the flag status FPLA's U33 and U13 appears below.

The flag information contained in U33 is:

- PSFF+ = parity system on or off
 - **ON by CLC 0 or STC 5
 - *OFF by CLC 5 or on power-up or immediately after parity error during CPU access to memory

- FRZM- = freeze memory protect violation address register
 - **OPEN LATCH by STC 7
 - *CLOSE LATCH by CLC 7 or on power-up or immediately after a memory protect violation that is not a result of a parity error

- PMPI+ = pending memory protect interrupt
 - *****SET by memory protect violation that is not a result of a parity error
 - *CLEARED on interrupt service to vector address 7 (memory protect violation servicing) or CLC 0 or on power-up

- IIFF- = interrupt inhibit flag
 - ***INHIBIT by CLC 4 or on interrupt service to vector address 4 (power fail interrupt servicing)
 - *UNINHIBIT by STC 4 or CLC 0 or on power-up

- PECF- = parity error on CPU access to memory
 - *****SET by parity error on CPU access to memory when the parity system is turned on
 - *CLEARED on interrupt service to vector address 5 (parity error servicing) or CLC 5 or on power-up

- UTIF+ = unimplemented instruction trap flag
 - *****SET when CPU chip signals UIT which is not a result of a parity error
 - *CLEARED on interrupt service to vector address 10 octal (unimplemented instruction servicing) or on power-up

- PCRS+ = control reset (used to generate CRS- on backplane)
 - ***ASSERTED only during CLC 0
 - *DE-ASSERTED otherwise

CSP+ = clear special interrupt
*HI only on interrupt service to vector address 17 octal
 (to service special interrupt) or CLC 0 or on power-up
*LO otherwise

The flag information contained in U13 is:

STATE+ = delayed power fail warning

GEN+ = global register flag
**GR ENABLED by CLF 2
*GR DISABLED by STF 2 or CLC 0 or on power-up

PTST- = part one of self test (checks address and data bus integrity)
**ON at power-up
*OFF on the first instruction fetch by the CPU

PS- = parity sense flag
*LO, EVEN PARITY by STF 5
**HI, ODD PARITY by CLF 5 or on power-up

PTBI+ = pending time base generator interrupt
****SET by STF 6 or TBT (time base tick from CPU every 10msec)
*CLEARED by interrupt service to vector address 6 (time base
 interrupt servicing) or CLC 0 or on power-up

PPFI+ = pending power fail interrupt
****SET by assertion of PFW- by power supply
*CLEARED by interrupt service to vector address 4 (power fail
 interrupt servicing) or on power-up

ISFF+ = interrupt system flag
**ENABLED by STF 0
*DISABLED by CLF 0 or CLC 0 or on power-up

FLG+ = low select code flag set/clear detection
*HI if a) ISFF+ is HI (interrupt system enabled) when
 conditional skip refers to flag 0
 or b) GEN+ is HI (GR enabled) when conditional skip
 refers to flag 2
 or c) PFW+ is LO (AC power is good) when conditional
 skip refers to flag 4
 or d) PS- is LO (even parity) when conditional skip
 refers to flag 5
 or e) PTBI+ is HI (pending time base interrupt) when
 conditional skip refers to flag 6
*LO if none of the above cases are satisfied

FPLA U15 is responsible for determining if a pending interrupt request may become a qualified interrupt. Interrupt requests may be inhibited, disabled or masked off.

INT+ = interrupt request to CPU chip

- *HI if a) PECF- is LO (parity error)
- or b) UTIF+ is HI (unimplemented instruction)
- or c) PMPI+ is HI (memory protect violation) and IIFF- is HI (level 2 and 3 interrupts uninhibited)
- or d) SPRQ- is LO (special interrupt request) and IIFF- is HI
- or e) PPF1+ is HI (power fail) and IIFF- is HI and TDI- is HI (interrupts not temporarily disabled)
- or f) PTBI+ is HI (time base interrupt request) and IIFF- is HI and TDI- is HI and ISFF+ is HI (level 3 interrupts enabled) and interrupt mask bit 1 is LO
- or g) INTRQ+ is HI (I/O interrupt request) and IIFF- is HI and TDI- is HI and ISFF+ is HI

*LO if none of the cases above are satisfied

SPINT+= the latched version of SPRQ- (special interrupt request)

*****SET by SPRQ-

*CLEARED by interrupt service to vector address 17 octal
(to service special interrupt)

ICHOD-= interrupt chain disable output

*HI if the interrupt to be serviced is an I/O interrupt

*LO if the interrupt to be serviced is a system level interrupt handled by the processor card. This signal disables all I/O cards from responding to the interrupt acknowledge

SLV+ = qualified slave request

- *HI if a) SLAVE+ is HI and PECF- is HI (parity error) and UTIF+ is LO (unimplemented instruction) and IIFF- is LO (level 2 and 3 interrupts inhibited)
- or b) SLAVE+ is HI and PECF- is HI (parity error) and UTIF+ is LO (unimplemented instruction) and PMPI+ is LO (memory protect violation) and SPINT+ is LO (special interrupt request)

*LO if none of the cases above are satisfied

PFIF+ = qualified power fail interrupt
MPIF+ = qualified memory protect violation interrupt
TBIF+ = qualified time base generator interrupt
SPIF+ = qualified special interrupt

2.5.4 VIRTUAL CONTROL PANEL (SLAVE MODE) PROCESSING

When the CPU is in slave mode, its internal registers are accessible to external devices through certain I/O interface cards. The Parallel Interface card, Asynchronous Interface card, and the HDLC (DS network) Interface card are the interface cards which may request slave mode processing. Since slave mode processing involves direct interaction between the requesting device and the CPU, the processor card merely provides buffering, signal timing, and bus arbitration for the handshake signals and data transfers.

Slave mode processing abides by the same protocols used for the execution of I/O instructions that require interaction between the I/O processors and the central processor. Whereas an instruction causes an I/O processor to initiate an I/O handshake, slave mode processing is performed in response to some external event not related to the program flow. The I/O handshake of an I/O instruction occurs during the execution of that instruction but the I/O handshake of slave mode processing occurs between instructions. Thus, slave mode uses IORQ- and IOGO-, but operates independently of the program.

A slave mode request, SLAVE-, is made over the backplane by the interface card configured for slave mode processing. Only one I/O interface card can be selected as the slave mode interface at any given time and that card must have its select code set to 20 (octal). As soon as the current instruction has been completed, the CPU chip will acknowledge the slave request and SCHOD- (slave chain output disable) will be deasserted to inform the slave requesting interface card to start the I/O handshake(s).

Any device with input/output capabilities and connected to an interface card configured to allow slave mode processing becomes the L-Series Computer's Virtual Control Panel. This device will provide the means to access the CPU registers and memory locations in a manner similar to a hardware front panel. If a terminal is the Virtual Control Panel device, the keyboard replaces the front panel switches for register selection and data entry, while the display replaces the hardware status and data output indicators. Unlike a hardware front panel, the Virtual Control Panel may be located remotely far away from the computer.

Operator interaction using a terminal is accomplished by a program located in the processor card ROMs. The code for this program is listed in Appendix A of

this document. See Section 1.4.1 for a description of the Virtual Control Panel.

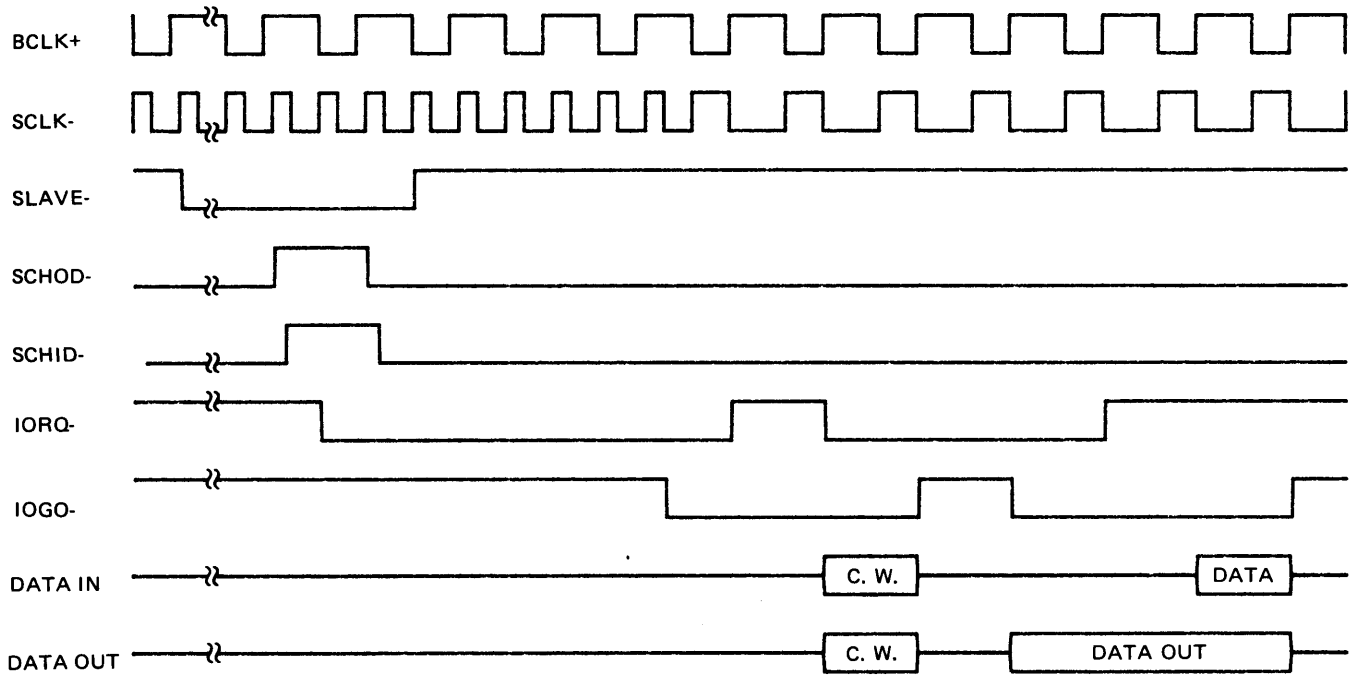
Refer to figure 2-23 for a timing diagram of the backplane protocol used during slave mode processing.

2.5.5 POWER ON SELF-TEST AND BOOT LOADERS

The CPU chip will initiate a bus integrity test for the processor card and backplane address and data buses at power up, as soon as DC power is at the proper voltages. This test will insure that the two buses are fully reliable before any processing begins. Beginning at address 0, the CPU chip drives the address bus. At power-up, before the first instruction fetch, the processor card drives the data bus with the same information that it receives on the address bus. The data bus is then read by the CPU chip to determine if the data bus is identical to the address bus. If the two buses agree, the CPU proceeds to the next address until all patterns on the address and data buses have been checked. If shorted printed circuit traces are present on either bus, the CPU freezes to prevent further processing. All of the status LEDs on the processor card remain on to indicate that the card is receiving DC power but fails the bus integrity test.

Part two of the power on self-test consists of system functionality tests. This portion of the self-test is executed from the processor card ROMs so that it is not necessary to assume that RAM memory is fully functional. If any part of the testing fails, the processor will freeze to prevent further processing and the status LEDs will indicate which subsystem was under test at the time of the failure. In chronological order, the self-test examines the RAM memory of the memory card, the CPU chip instruction set, the processor card I/O instructions and interrupt handling, and the I/O master section of all I/O interfaces installed in the backplane.

Following the successful completion of the self-test, the L-Series will automatically execute one of three power on options selectable via the processor card switches (positions 1 through 3). If the virtual control panel option is selected and a terminal is the peripheral device, the computer will output the CPU register status to the CRT and wait for a virtual control panel command from the keyboard. At this time, one of four boot loaders may be invoked (disc via HP-IB, network link, PROM I/O, or 264x/2671 cartridge tape). If the bootstrap loader is the option selected, the L-Series will automatically boot load from disc, network, or PROM I/O at the completion of self-test. If the auto-restart option is selected (assuming battery backup is installed), the computer will resume program execution beginning at the point it left off when power was removed. These power on options permit the L-Series to be used in a variety of applications ranging from a simple stand alone controller to a node in a complex network.



NOTES: Same handshake protocols as an I/O handshake.
 Some slave mode transfers require only one set of IORQ-/IOGO- handshakes.

Figure 2-23. Slave Transfer Protocols

See the HP 1000 L-Series Reference Manual, part number 02103-90007 for a discussion of the bootstrap loader; Section I of this document for a discussion of the Virtual Control Panel; and the HP 1000 L-Series Computer Installation and Service Manual, part number 02103-90003 for discussion of the power fail recovery procedure.

2.5.6 L-SERIES CLOCKS

The L-Series processor generates four different clocks for use by the memory and I/O interface cards.

FCLK- (Fast Clock) has a nominal frequency of 22.016 MHz (period=45 ns) and a duty cycle of 50%. It is used by the memory card to clock logic operating at frequencies higher than that required by the processor. Its frequency is reduced by a factor of two to 11.008 MHz (period=90 ns) during I/O or slave mode handshakes. For both frequencies, a rising edge of FCLK- accompanies every transition of RCLK+, SCLK-, and BCLK+.

RCLK+ (Refresh Clock) has a nominal frequency of 4.4 MHz (period=227ns) and a duty cycle of 60%. It is used by the memory card to time refresh cycles. Its frequency remains at 4.4 MHz during I/O handshakes.

SCLK- (System Clock) has a nominal frequency of 4.4 MHz (period=227ns) and a duty cycle of 40%. It is used by every L-Series card to synchronize all backplane transactions. All backplane timing guarantees and requirements are referenced to SCLK-. Its frequency is that of FCLK- divided by five. SCLK- is 2.2 MHz (period=454ns) during I/O handshakes. SCLK- is always phase locked to FCLK- and, most of the time, to RCLK+.

CCLK- (Communications Clock) has a nominal frequency of 14.7456 MHz (period=67.8ns) and a duty cycle of 50%. It is used by all serial interface cards, and by any interface requiring a fixed frequency for state machine or counting operations. This frequency is a convenient multiple (times 16) of the frequency used by the baud rate generator integrated circuits (see the Asynchronous Serial Interface Reference Manual, part number 12005-90001).

BCLK+ (CPU Clock) has a nominal frequency of 2.2 MHz (period=454ns) and a duty cycle of 60%. It is used only by the CPU chip and various processor board to CPU chip interface logic devices.

All of the clocks are derived from two crystal oscillators on the processor board. The backplane CCLK- is the buffered version of a 14.7456 MHz crystal oscillator. The output of a 22.016 MHz crystal oscillator is buffered and then divided down to create FCLK-, RCLK+, SCLK-, and BCLK+. Since the time base generator in the CPU chip is dependent on an accurate BCLK+, it is necessary for the 22.016 MHz oscillator to be as stable to its nominal frequency as possible. A device with 50 parts per million (0.005% variation) stability was chosen so that time may be kept to within 4.32 seconds per day.

A buffered version of the 22MHz oscillator is used in edge-triggering every flip-flop in the clock generation circuitry. This insures that the 22MHz clock is an integer multiple of any clock (except CCLK-) found on the processor or on the backplane. U71b and U72a,b form the nucleus of the clock generation logic. Collectively, they constitute a state machine implementation of a divide by five counter. The following chart shows the state transition for the three flip-flops:

| U72.5 Q1 | U71.9 Q2 | U72.9 Q3 |
|-------------|-------------|-------------|
| 0 | 0 | 0 |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 1 | 1 |
| 1 | 1 | 0 |

The next state after the fifth state (110) is the first state (000), so the counter repeats itself every 227.1 nsec given that the time between states is 45.4 nsec (22MHz clock). The Q output of U71b (pin 9) is LO for two states

the memory card as RCLK+ and to the clock selector circuitry. The clock select multiplexer U91 chooses between two pairs of clocks to output as the backplane FCLK- and SCLK- clock signals.

U81a is a JK flip-flop configured as a toggle flip-flop. It is clocked with the 22MHz clock so its output (pin 5) is 11MHz. U81b is used to generate a 2.2016 MHz version (half the frequency) of RCLK+. The Q output of U81b (pin 9) is called BCLK- and has a frequency of 2.2016 MHz and a duty cycle of 40%. BCLK- is synchronized to RCLK+ so that every rising edge of BCLK- is accompanied by a falling edge of RCLK+.

The clock select logic is essentially a flip-flop (U71a) that is set (Q=SEL=1) whenever a slower clock is required. When SEL=1, the data selector U91 selects a pair of half-speed clocks. On power-up, SEL=0 so that FCLK-=22MHz and SCLK-=4.4MHz. Following the assertion of IOGO- on the backplane, SEL becomes 1 and the data selector chooses the appropriate signals to make FCLK-=11MHz and SCLK-=2.2MHz. To distinguish between the two modes, FCLK[1]-=22MHz and FCLK[2]-=11MHz, and similarly for SCLK-. SEL returns to 0 following the assertion of MEMGO- or BUSY- on the backplane, or upon a hardware reset (PON+ low). All transitions between regular and half-speed clocks occur at the falling edge (or start of short half cycle) of BCLK- to maintain phase synchronization between BCLK- and SCLK-.

The CPU chip receives the 2.2MHz BCLK+ (inverted form of BCLK-) as its operational clock. The memory card utilizes RCLK+ to time its refresh counters. The backplane gets both FCLK- and SCLK-. The processor card runs on SCLK+, a buffered and inverted version of SCLK-.

2.6 PARTS LOCATIONS

Parts locations for the processor card are shown in figure 2-24.

2.7 PARTS LIST

The parts lists for the processor card is shown in table 2-3. Refer to table 6-39 for the names and addresses of manufacturers of the parts.

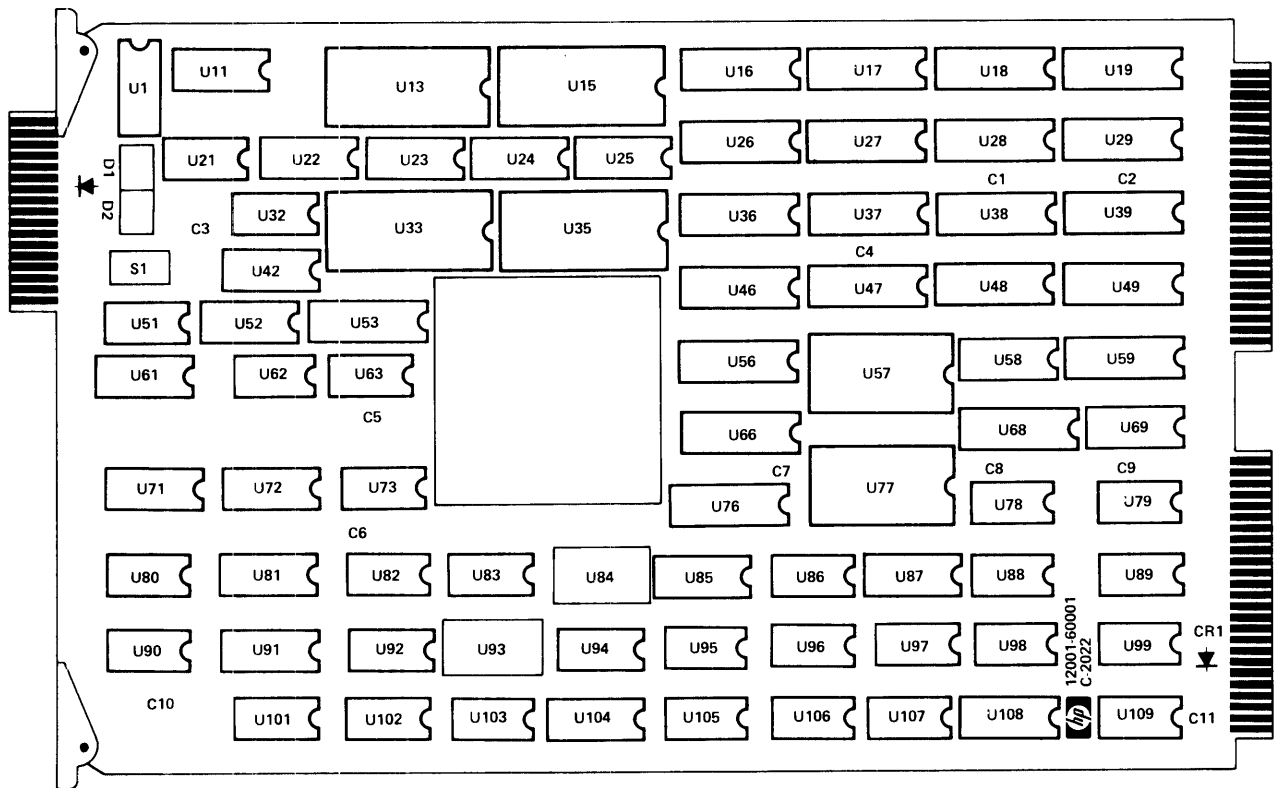


Figure 2-24. Processor Card Parts Locations

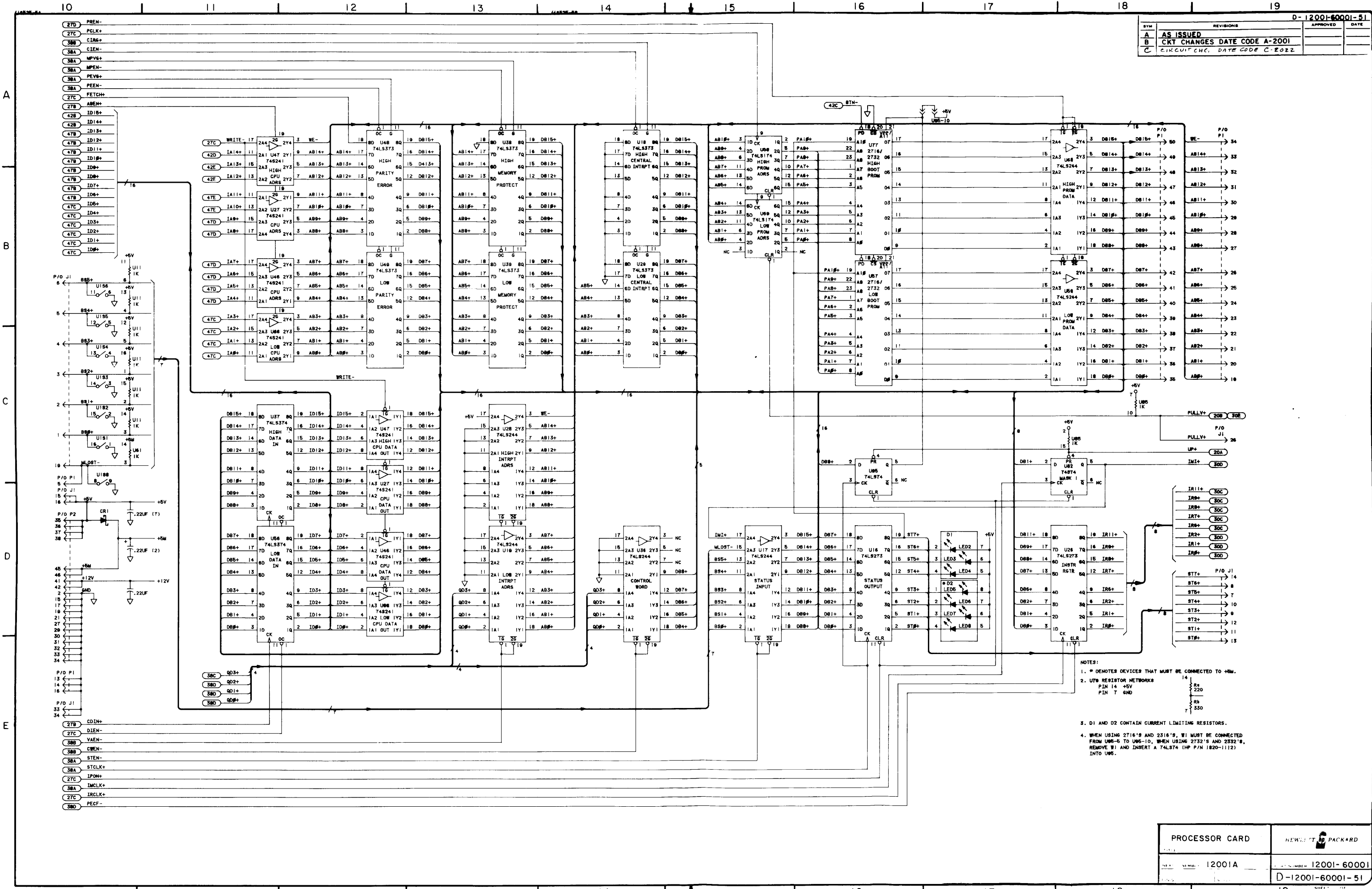
Table 2-3. Processor Card Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|--------------------|
| | 12001-60001 | 9 | 1 | ASSEMBLY-CPU | 28480 | 12001-60001 |
| C1-C11 | 0160-4842 | 6 | 34 | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| CR1 | 1901-1080 | 1 | 1 | DIODE-SCHOTTKY 1N5817 20V 1A | 28480 | 1901-1080 |
| D1 | 1990-0652 | 8 | 2 | LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX | 28480 | 1990-0652 |
| D2 | 1990-0652 | 8 | 2 | LED-VISIBLE LUM-INT=200UCD IF=5MA-MAX | 28480 | 1990-0652 |
| E1 | 0360-1682 | 0 | 2 | TERMINAL-STUD SGL-TUR PRESS-MTG | 28480 | 0360-1682 |
| E2 | 0360-1682 | 0 | 2 | TERMINAL-STUD SGL-TUR PRESS-MTG | 28480 | 0360-1682 |
| S1 | 3101-2155 | 9 | 1 | SWITCH-PB SPDT MOM .5A 120VAC | 28480 | 3101-2155 |
| U1 | 3101-2243 | 6 | 1 | SWITCH-DIP 8-ROCKER | 28480 | 3101-2243 |
| U11 | 1810-0037 | 3 | 3 | NETWORK-RES 16-DIP1.0K OHM X 8 | 11236 | 761-3-R1K |
| U13 | 1A20-2334 | 8 | 1 | IC MISC TTL 8 | 18324 | 8281001 PROGRAMMED |
| U15 | 1820-2568 | 0 | 1 | IC OSC HYBRID | 28480 | 1820-2568 |
| U16 | 1A20-1730 | 6 | 3 | IC FF TTL L8 D-TYPE POS-EDGE-TRIG COM | 01295 | 8N74L8273N |
| U17 | 1820-2024 | 3 | 6 | IC DRVR TTL L8 LINE DRVR OCTL | 01295 | 8N74L8244N |
| U18 | 1820-2102 | 8 | 6 | IC LCH TTL L8 D-TYPE OCTL | 01295 | 8N74L8373N |
| U19 | 1820-2024 | 3 | 6 | IC DRVR TTL L8 LINE DRVR OCTL | 01295 | 8N74L8244N |
| U21 | 1A20-0681 | 4 | 2 | IC GATE TTL 8 NAND QUAD 2-INP | 01295 | 8N74800N |
| U22 | 1820-1240 | 3 | 3 | IC DCDR TTL 8 3-TO-8-LINE 3-INP | 01295 | 8N748138N |
| U23 | 1A20-1240 | 3 | 2 | IC DCDR TTL 8 3-TO-8-LINE 3-INP | 01295 | 8N748138N |
| U24 | 1820-1015 | 0 | 2 | IC MUXR/DATA=8EL TTL 8 2-TO-1-LINE QUAD | 01295 | 8N748158N |
| U25 | 1A20-1015 | 0 | 2 | IC MUXR/DATA=8EL TTL 8 2-TO-1-LINE QUAD | 01295 | 8N748158N |
| U26 | 1820-1730 | 6 | 6 | IC FF TTL L8 D-TYPE POS-EDGE-TRIG COM | 01295 | 8N74L8273N |
| U27 | 1A20-1624 | 7 | 4 | IC BFR TTL 8 OCTL 1-INP | 01295 | 8N748241N |
| U28 | 1A20-2024 | 3 | 3 | IC DRVR TTL L8 LINE DRVR OCTL | 01295 | 8N74L8244N |
| U29 | 1A20-2102 | 8 | 3 | IC LCH TTL L8 D-TYPE OCTL | 01295 | 8N74L8373N |
| U32 | 1A20-0685 | 8 | 1 | IC GATE TTL 8 NAND TPL 3-INP | 01295 | 8N74810N |
| U33 | 1820-2534 | 0 | 1 | IC OSC HYBRID | 28480 | 1820-2534 |
| U35 | 1A20-2335 | 9 | 1 | IC MISC TTL 8 | 18324 | 8281001 PROGRAMMED |
| U36 | 1A20-2024 | 3 | 3 | IC DRVR TTL L8 LINE DRVR OCTL | 01295 | 8N74L8244N |
| U37 | 1A20-1997 | 7 | 2 | IC FF TTL L8 D-TYPE POS-EDGE-TRIG PRL-IN | 01295 | 8N74L8374N |
| U38 | 1A20-2102 | 8 | 3 | IC LCH TTL L8 D-TYPE OCTL | 01295 | 8N74L8373N |
| U39 | 1820-2102 | 8 | 3 | IC LCH TTL L8 D-TYPE OCTL | 01295 | 8N74L8373N |
| U42 | 1A20-1196 | 8 | 3 | IC FF TTL L8 D-TYPE POS-EDGE-TRIG COM | 01295 | 8N74L8174N |
| U46 | 1A20-1624 | 7 | 3 | IC BFR TTL 8 OCTL 1-INP | 01295 | 8N748241N |
| U47 | 1A20-1624 | 7 | 3 | IC BFR TTL 8 OCTL 1-INP | 01295 | 8N748241N |
| U48 | 1A20-2102 | 8 | 3 | IC LCH TTL L8 D-TYPE OCTL | 01295 | 8N74L8373N |
| U49 | 1820-2102 | 8 | 3 | IC LCH TTL L8 D-TYPE OCTL | 01295 | 8N74L8373N |
| U52 | 1A20-1240 | 3 | 3 | IC DCDR TTL 8 3-TO-8-LINE 3-INP | 01295 | 8N748138N |
| U53 | 1A20-1730 | 6 | 3 | IC FF TTL L8 D-TYPE POS-EDGE-TRIG COM | 01295 | 8N74L8273N |
| U55 | 1A85-6001 | 6 | 1 | 21 LC | 28480 | 1A85-6001 |
| U56 | 1A20-1997 | 7 | 1 | IC FF TTL L8 D-TYPE POS-EDGE-TRIG PRL-IN | 01295 | 8N74L8374N |
| U57 | 5090-1624 | 2 | 1 | IC-PTST-L | 28480 | 5090-1624 |
| U58 | 1A20-1196 | 8 | 3 | IC FF TTL L8 D-TYPE POS-EDGE-TRIG COM | 01295 | 8N74L8174N |
| U59 | 1A20-2024 | 3 | 3 | IC DRVR TTL L8 LINE DRVR OCTL | 01295 | 8N74L8244N |
| U61 | 1810-0037 | 3 | 3 | NETWORK-RES 16-DIP1.0K OHM X 8 | 11236 | 761-3-R1K |
| U62 | 1A20-0683 | 6 | 2 | IC INV TTL 8 HEX 1-INP | 01295 | 8N74804N |
| U63 | 1820-1273 | 2 | 1 | IC BFR TTL L8 NOR QUAD 2-INP | 01295 | 8N74L828N |
| U66 | 1A20-1624 | 7 | 3 | IC BFR TTL 8 OCTL 1-INP | 01295 | 8N748241N |
| U68 | 1A20-2024 | 3 | 3 | IC DRVR TTL L8 LINE DRVR OCTL | 01295 | 8N74L8244N |
| U69 | 1820-1196 | 8 | 3 | IC FF TTL L8 D-TYPE POS-EDGE-TRIG COM | 01295 | 8N74L8174N |
| U71 | 1A20-0629 | 0 | 5 | IC FF TTL 8 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U72 | 1820-0629 | 0 | 5 | IC FF TTL 8 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U73 | 1A20-1989 | 7 | 1 | IC CNTR TTL L8 BIN DUAL 4-BIT | 07263 | 74LS393PC |
| U76 | 1820-1633 | 8 | 1 | IC BFR TTL 8 INV OCTL 1-INP | 01295 | 8N748240N |
| U77 | 5090-1625 | 3 | 1 | IC-PTST-H | 28480 | 5090-1625 |
| U78 | 1A20-1450 | 7 | 3 | IC BFR TTL 8 NAND QUAD 2-INP | 01295 | 8N74837N |
| U79 | 1810-0182 | 9 | 1 | NETWORK-RES 14-DIP MULTI-VALUE | 28480 | 1810-0182 |
| U80 | 1820-1415 | 4 | 1 | IC SCHMITT-TRIG TTL L8 NAND DUAL 4-INP | 01295 | 8N74L813N |
| U81 | 1A20-0629 | 0 | 5 | IC FF TTL 8 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U82 | 1A20-0693 | 8 | 5 | IC FF TTL 8 D-TYPE POS-EDGE-TRIG | 01295 | 8N74874N |
| U83 | 1A20-0693 | 8 | 5 | IC FF TTL 8 D-TYPE POS-EDGE-TRIG | 01295 | 8N74874N |
| U84 | 1A13-0129 | 0 | 1 | IC OSC HYBRID | 34344 | K1100A |
| U85 | 1810-0037 | 3 | 3 | NETWORK-RES 16-DIP1.0K OHM X 8 | 11236 | 761-3-R1K |
| U86 | 1A20-0683 | 6 | 2 | IC INV TTL 8 HEX 1-INP | 01295 | 8N74804N |
| U87 | 1A20-1077 | 4 | 2 | IC MUXR/DATA=8EL TTL 8 2-TO-1-LINE QUAD | 01295 | 8N748157N |
| U88 | 1A20-1322 | 2 | 3 | IC GATE TTL 8 NOR QUAD 2-INP | 01295 | 8N74802N |
| U89 | 1A20-1451 | 8 | 1 | IC GATE TTL 8 NAND QUAD 2-INP | 01295 | 8N74838N |
| U90 | 1A20-0681 | 4 | 1 | IC GATE TTL 8 NAND QUAD 2-INP | 01295 | 8N74800N |
| U91 | 1A20-1077 | 4 | 1 | IC MUXR/DATA=8EL TTL 8 2-TO-1-LINE QUAD | 01295 | 8N748157N |
| U92 | 1820-1416 | 5 | 1 | IC SCHMITT-TRIG TTL L8 INV HEX 1-INP | 01295 | 8N74L814N |
| U93 | 1A13-0166 | 5 | 1 | IC OSC HYBRID | 34344 | K1145A-22.016MHZ |
| U94 | 1A20-1307 | 3 | 1 | IC SCHMITT-TRIG TTL 8 NAND QUAD 2-INP | 01295 | 8N748132N |
| U96 | 1A20-1210 | 7 | 1 | IC GATE TTL L8 AND-OR-INV DUAL 2-INP | 01295 | 8N74L851N |

Table 2-3. Processor Card Parts List (Continued)

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------|
| U97 | 1820-0691 | 6 | 1 | IC GATE TTL 8 AND-OR-INV | 01295 | 8N74864N |
| U98 | 1820-1367 | 5 | 2 | IC GATE TTL 8 AND QUAD 2-INP | 01295 | 8N74808N |
| U99 | 1820-1450 | 7 | | IC 8PR TTL 8 NAND QUAD 2-INP | 01295 | 8N74837N |
| U101 | 1820-1367 | 5 | | IC GATE TTL 8 AND QUAD 2-INP | 01295 | 8N74808N |
| U102 | 1820-1450 | 7 | | IC 8PR TTL 8 NAND QUAD 2-INP | 01295 | 8N74837N |
| U103 | 1820-1322 | 2 | | IC GATE TTL 8 NOR QUAD 2-INP | 01295 | 8N74802N |
| U104 | 1820-0629 | 0 | | IC FF TTL 8 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U105 | 1820-0693 | 8 | | IC FF TTL 8 D-TYPE POS-EDGE-TRIG | 01295 | 8N74874N |
| U106 | 1820-0693 | 8 | | IC FF TTL 8 D-TYPE POS-EDGE-TRIG | 01295 | 8N74874N |
| U107 | 1820-1322 | 2 | | IC GATE TTL 8 NOR QUAD 2-INP | 01295 | 8N74802N |
| U108 | 1820-0629 | 0 | | IC FF TTL 8 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U109 | 1820-0693 | 8 | | IC FF TTL 8 D-TYPE POS-EDGE-TRIG | 01295 | 8N74874N |
| | | | | MISCELLANEOUS PARTS | | |
| | 0403-0289 | 3 | 1 | EXTR=PC 8D RED POLYC .063=8D=THKNS | 28480 | 0403-0289 |
| | 1200-0541 | 1 | 2 | SOCKET=IC 24=CONT DIP DIP=8LDR | 28480 | 1200-0541 |
| | 1200-0638 | 7 | 1 | SOCKET=IC 14=CONT DIP DIP=8LDR | 28480 | 1200-0638 |
| | 1200-0845 | 8 | 2 | RETAINER=SUBSTRATE STEEL; NICKEL PLATE | 28480 | 1200-0845 |
| | 1200-0848 | 1 | 1 | SOCKET=888TR 64=CONT CERAMIC DIP=8LDR | 28480 | 1200-0848 |
| | 1200-0875 | 4 | 2 | SOCKET=IC 4=CONT DIP DIP=8LDR | 28480 | 1200-0875 |
| | 1258-0124 | 7 | 1 | PIN=PROGRAMING DUMPER .30 CONTACT | 91506 | 8136-47561 |

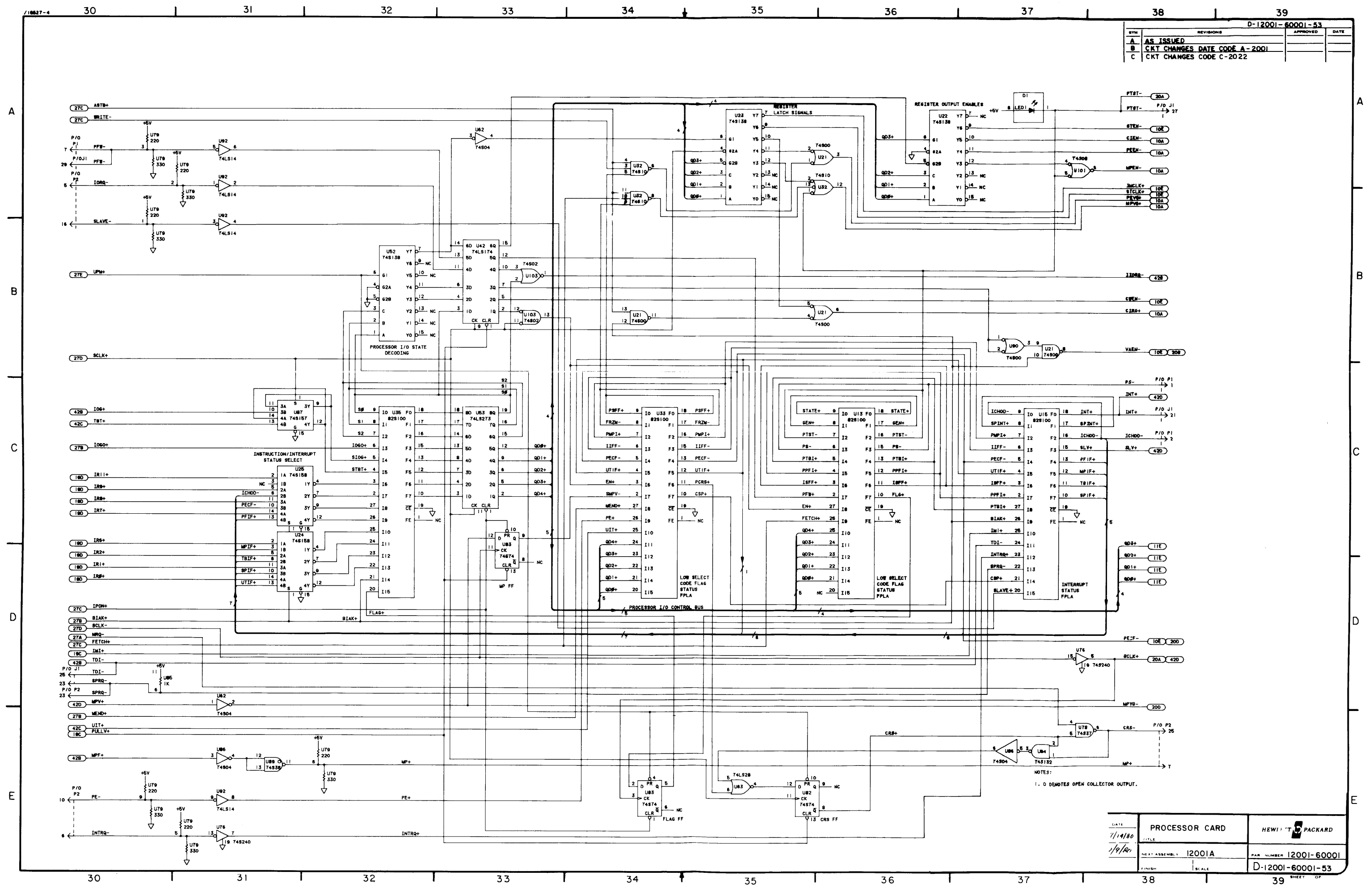
| REVISIONS | | APPROVED | DATE |
|-----------|-------------------------------|----------|------|
| A | AS ISSUED | | |
| B | CKT CHANGES DATE CODE A-2001 | | |
| C | CIRCUIT CHG. DATE CODE C-2022 | | |



- NOTES:
- * DENOTES DEVICES THAT MUST BE CONNECTED TO +5V.
 - U7B RESISTOR NETWORKS
PIN 14 +5V
PIN 7 GND
 - D1 AND D2 CONTAIN CURRENT LIMITING RESISTORS.
 - WHEN USING 2716'S AND 2316'S, W1 MUST BE CONNECTED FROM U96-5 TO U96-10, WHEN USING 2732'S AND 2832'S, REMOVE W1 AND INSERT A 74LS74 (HP P/N 1820-1112) INTO U96.

| | | | |
|------------------|--------|------------------|-------------|
| PROCESSOR CARD | | HEWLETT PACKARD | |
| SYM | 12001A | REV | 12001-60001 |
| D-12001-60001-51 | | D-12001-60001-51 | |

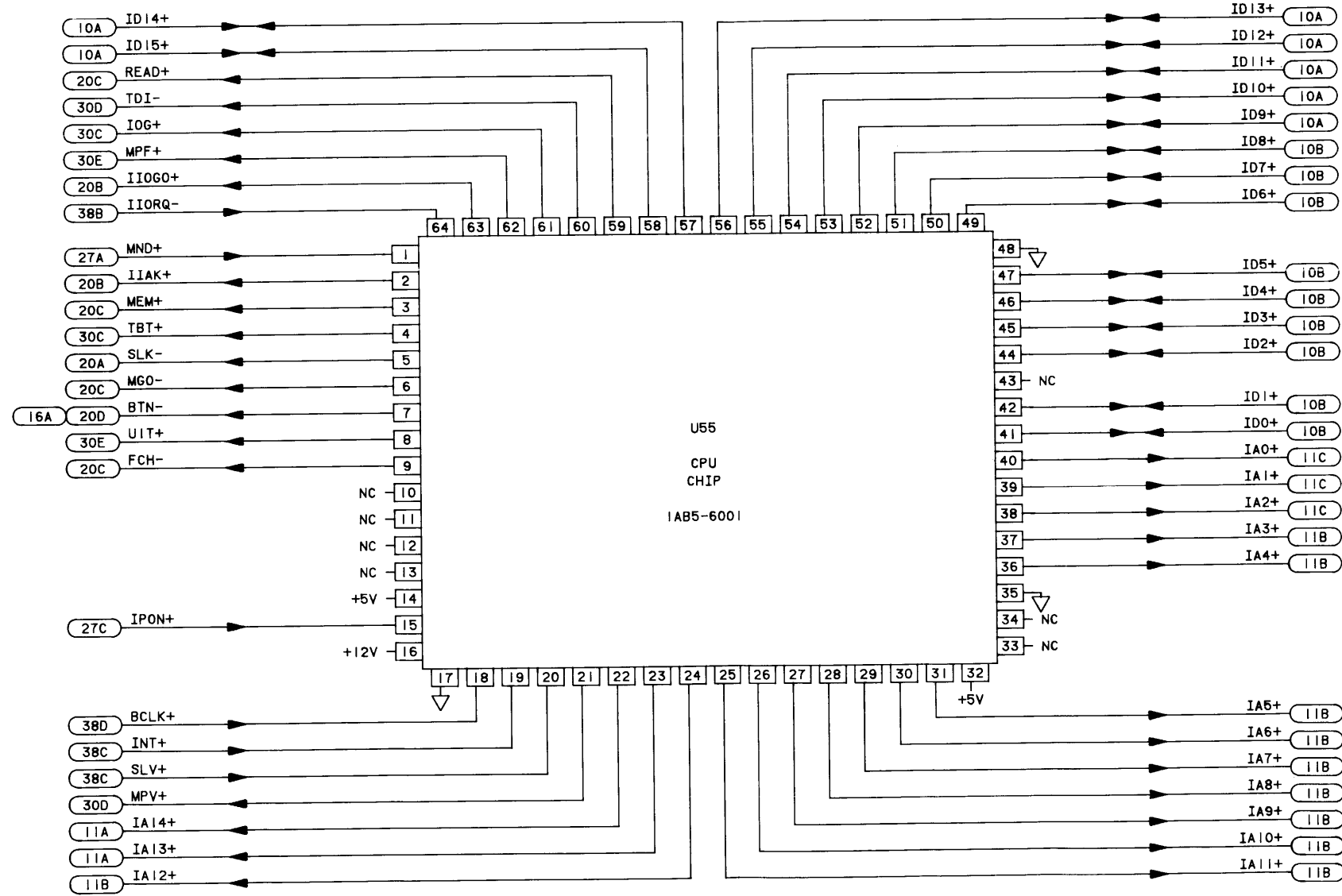
| REV | REVISIONS | APPROVED | DATE |
|-----|------------------------------|----------|------|
| A | AS ISSUED | | |
| B | CKT CHANGES DATE CODE A-2001 | | |
| C | CKT CHANGES CODE C-2022 | | |



NOTES:
1. O DENOTES OPEN COLLECTOR OUTPUT.

| | | |
|-----------------|----------------------|-------------------------|
| DATE 1/14/80 | PROCESSOR CARD | HEWLETT-PACKARD |
| 1/9/80 | NEXT ASSEMBLY 12001A | PAR. NUMBER 12001-60001 |
| | FINISH SCALE | D-12001-60001-53 |
| | | SHEET OF |

| | | | |
|-----|------------------------------|----------|------|
| SYM | REVISIONS | APPROVED | DATE |
| A | AS ISSUED | | |
| B | CKT CHANGES DATE CODE A-2001 | | |
| C | CKT CHANGES DATE CODE C-2022 | | |



| | | | |
|----------------|--------|-----------------|------------------|
| PROCESSOR CARD | | HEWLETT PACKARD | |
| MODEL | 12001A | SERIAL NUMBER | 12001-60001 |
| DATE | | SCALE | D-12001-60001-54 |

| | |
|-----------------|-------------|
| 64K BYTE MEMORY | SECTION III |
|-----------------|-------------|

3.1 INTRODUCTION

A 65,536 byte random access memory is the main memory for the HP 1000 L-Series Computer System. The memory system, which includes the memory control circuits as well as the memory array itself, is contained on one circuit card and plugs directly into the L-Series backplane. The circuit card is shown in figure 3-1.

3.2 OVERVIEW

3.2.1 SYSTEM ENVIRONMENT

The system environment of the HP 1000 L-Series Computer System is shown in Section II, figure 2-2. The memory card can be plugged into any slot in the L-Series backplane with two important restrictions:

- a. The memory card must be located immediately above the processor card.
- b. No input/output (I/O) cards can be located above the memory card.

The above suggests that the memory and processor cards will always occupy the highest priority card slots in the card cage. This is true, but it should be noted that ANY two slots may be occupied by the memory and processor as long as no I/O cards are plugged into the higher priority slots (see Section VI, figure 6-3 for slot priorities).

Once it is plugged into the backplane, the memory card needs no further For reliable data retention, the RAMs must be refreshed completely every 2 msec. The refresh function is accomplished by periodically generating a refresh read pulse internal to the memory controller. The refresh period is determined by a refresh counter which is clocked by SCLK.

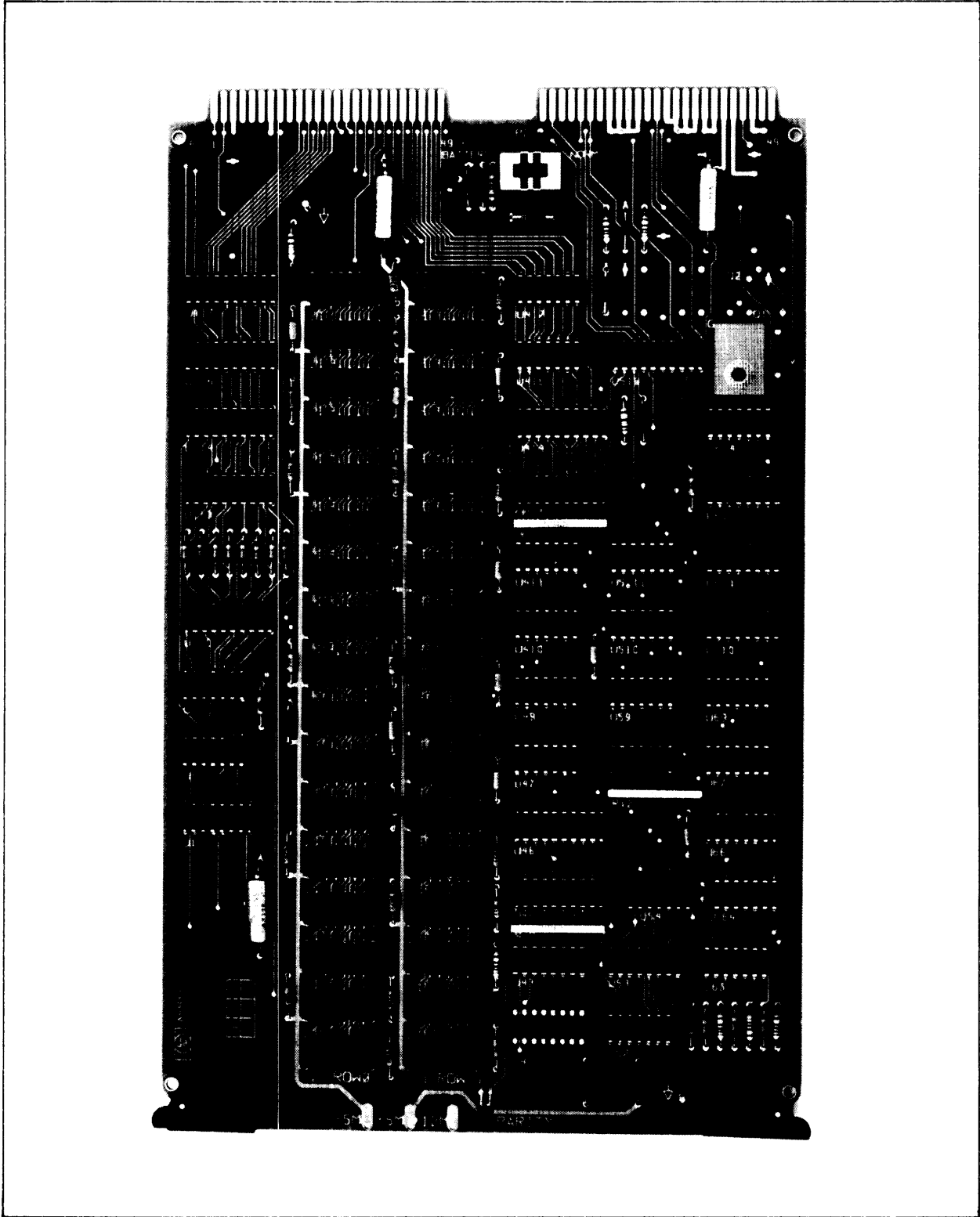


Figure 3-1. HP 1000 L-Series Memory Card

3.2.2 BASIC MEMORY OPERATION

There are three modes of operation of the memory:

- a. Write cycle.
- b. Read cycle.
- c. Refresh cycle.

Whenever the term "memory cycle" is used in this document, however, it will refer to either a read or a write cycle, and not to a refresh cycle. Memory cycles always are initiated by a stimulus external to the memory card; refresh cycles, on the other hand, are initiated by the memory itself. The memory may function in only one of the three modes at any given time.

3.2.2.1 Write Cycle

A basic write cycle is shown in figure 3-2. A write cycle is initiated when the memory controller receives a MEMGO pulse from the external interface along with the highest order bit of the address bus (Read/Write) cleared (low). At the beginning of the next short-half-cycle (SHC) of the SCLK, the memory controller will assert the BUSY control signal to hold off any other requests for a memory cycle. Shortly after this time, the controller will internally latch the data to be written and also the address to which it will be written.

The parity of the data to be written is generated from the data present on the backplane data bus and is set up to be written into memory along with the data. After the data and address are latched, the memory controller then writes the data into the memory array. At the beginning of the next SHC of SCLK, the memory controller asserts the VALID control line for one SCLK period to signal the completion of the write cycle. The BUSY signal is deasserted at the same time as VALID is deasserted and this completes the handshake.

The length of the write cycle is always three complete SCLK cycles, and because the controller needs no additional handshake overhead, the write cycle time of the memory is 3 times (1 SCLK period).

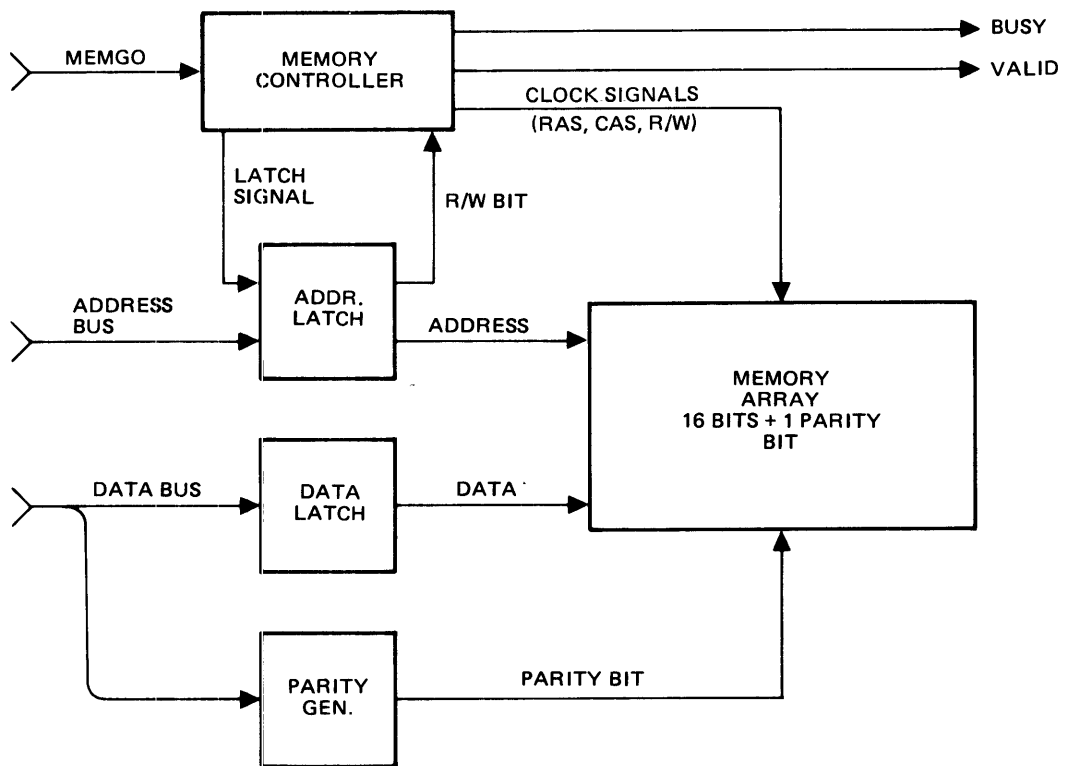


Figure 3-2. Basic Write Cycle

3.2.2.2 Read Cycle

A read cycle is shown in figure 3-3.

A read cycle is initiated when the memory controller receives a MEMGO- and the highest order bit of the address bus (Read/Write) is set (high). On the next short-half-cycle (SHC) of SCLK, the BUSY handshake signal is asserted to hold off any further requests for a memory cycle. A short time later, the address of the data to be read is latched into the address buffer. At the beginning of the next SHC, VALID is asserted to signal that the desired data is available on the backplane. The data becoming valid on the backplane is actually referenced to the trailing edge of the VALID pulse and it is this trailing edge that is used to clock the data out of memory.

While the data is valid on the backplane, the parity detector examines the data for correct parity and if it is found to be incorrect, a parity error is asserted by the memory controller. The BUSY handshake signal is de-asserted at the same time that VALID is de-asserted but the data is held on the backplane for one SHC of SCLK to satisfy data hold time requirements. The length of a read cycle is always three SCLK cycles, which is identical to the write cycle time.

3.2.2.3 Refresh Cycle

The dynamic random-access memory (RAM) elements require refreshing in order to retain data. Refresh is accomplished by issuing a read strobe pulse (RAS) to all the RAMs at regular intervals. The 16K RAMs are organized internally as a 128-by-128 matrix with the refresh function being accomplished one row at a time. The memory controller performs the refreshing by addressing each row separately and issuing a refresh read pulse. This refreshing occurs at all times that the memory has power applied to it.

Refresh cycles interleave with the memory cycles so that their function is transparent to the processor card. In the event that a memory cycle and a refresh cycle are attempted concurrently, the pending refresh cycle will hold off the requested external access cycle until the pending cycle completes. Because a refresh cycle also takes exactly three SCLK cycles to complete, the longest any requested cycle is held off is only three SCLK cycles.

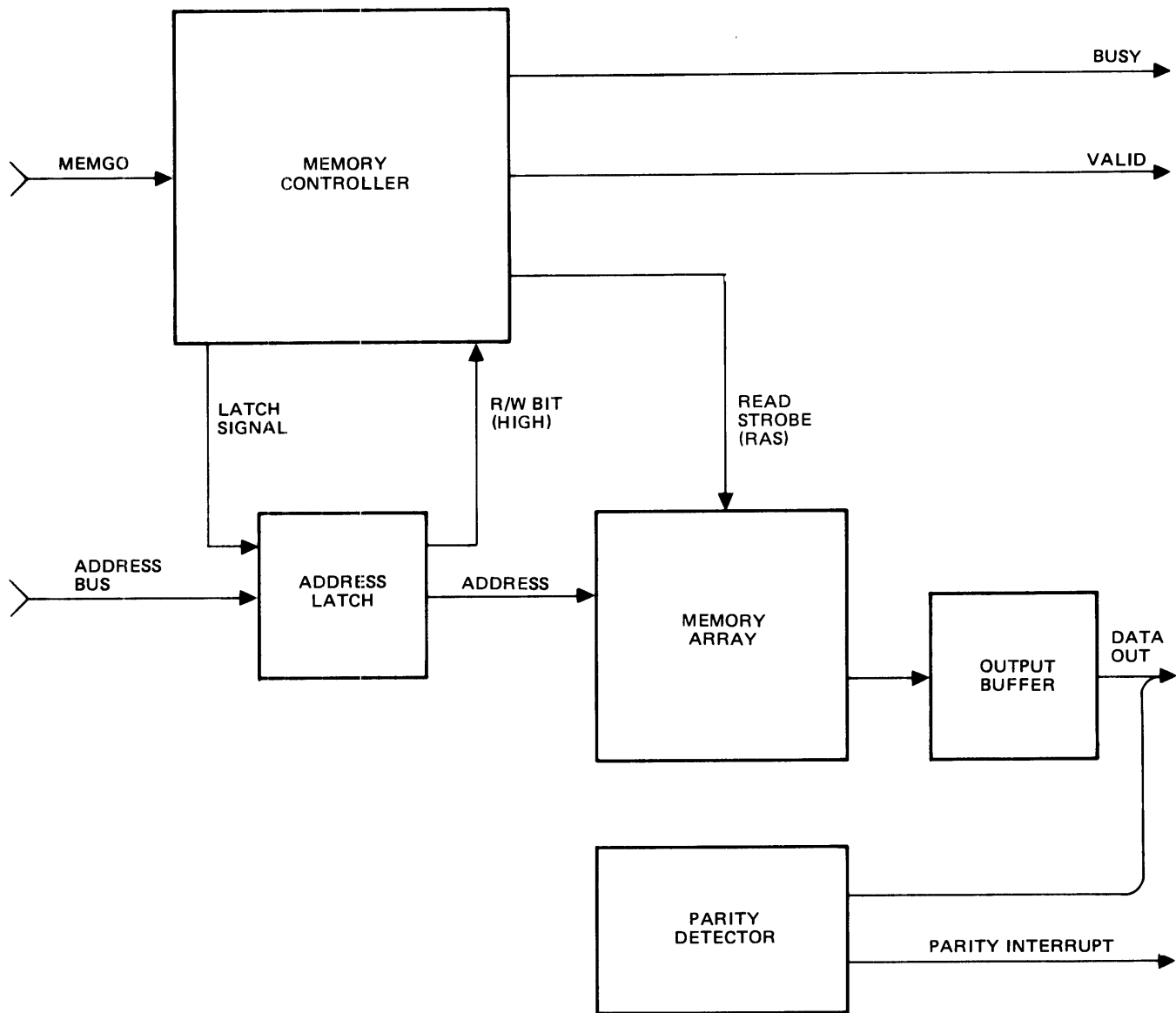


Figure 3-3. Basic Read Cycle

3.3 SPECIFICATIONS

3.3.1 POWER REQUIREMENTS

The worst case power requirements for the memory are listed below:

| VOLTAGE | CURRENT | | POWER | |
|---------|---------|-----------|---------|-----------|
| | STANDBY | OPERATING | STANDBY | OPERATING |
| +12M | 48mA | 273mA | 0.58W | 3.28W |
| -12M | 20mA | 20mA | 0.24W | 0.24W |
| +5M | 757mA | 757mA | 3.79W | 3.79W |
| +5V | 0mA | 1300mA | 0W | 6.50W |

The above current figures were obtained by calculating the RMS values as follows:

$$I_{\text{RMS}} = \sum I_{\text{typ}} + \sqrt{\sum (I_{\text{max}} - I_{\text{typ}})^2}$$

The +12M current is a measured worst case value (memory running at maximum access rate) plus 15 percent.

3.3.2 MEMORY CYCLE TIME

Memory cycles require three System Clock (SCLK) cycles for completion, thus the memory cycle time is 3 x (1 SCLK period). For a SCLK period of 227 nsec, therefore, the memory cycle time is 681 nsec. The memory card will operate with an SCLK period as short as 180 nsec without any modification.

3.3.3 MEMORY REFRESH PERIOD

For reliable data retention, the RAMs must be refreshed completely every 2 msec. The refresh function is accomplished by periodically generating a refresh read pulse internal to the memory controller. The refresh period is determined by a refresh counter which is clocked by SCLK.

Because the RAMs must be refreshed every 2 milliseconds, the refresh counter must count the correct number of SCLK cycles to refresh the 128 row addresses in these 2 milliseconds. If refreshing is done at a slower rate, data integrity is not guaranteed. If refreshing is done at a faster rate, memory is still maintained but the efficiency of the memory system decreases. This is due to the fact that memory cycles cannot occur when a refresh cycle is executing, thus, refresh cycles occurring too frequently decrease the amount of time available for memory cycles. Of course, any change in the SCLK period will produce a corresponding change in the refresh period.

3.3.4 DATA/ADDRESS LATCHES

Data and addresses sent to the memory are latched into buffers before any memory cycle begins. This is necessary because memory cycles may be attempted while a refresh cycle is in progress. In this case, addresses and data may be present only while the MEMGO pulse is asserted on the backplane. Because the memory cycle will be suspended while the refresh cycle is executed, there must be a way to store the address and data for the attempted memory cycle. The address and data latches serve this purpose. In this way, when the refresh cycle completes, the necessary data will be available for servicing the requested memory cycle. Although the latches are not really necessary for memory cycles occurring during the absence of refresh cycles, they still perform the latching function. This assures, however, that the data is held at the RAM inputs during a write cycle.

3.3.5 PARITY GENERATION/DETECTION

A parity generator/detector circuit is used to generate parity information for data that is stored into memory and to check for correct parity for data being accessed from memory. The parity circuit monitors the data bus directly without any buffering, thus parity of data being accessed from memory is checked directly on the backplane.

On a write cycle, parity is generated at the time the address/data latches are frozen. When the 16 data bits are written into memory a short time later, a 17th bit (parity bit) also is stored. This parity bit is either set or cleared, depending on the data pattern. The sense of parity is set ODD under normal operating conditions, that is, the sum of all SET bits in the data word AND the parity bit is equal to an odd decimal number.

On a read cycle, the parity of the accessed data as it appears on the backplane is checked. If the parity is not ODD, the parity detector will generate a parity error (PE-) signal on the backplane which may be received by both the processor and the I/O cards. This informs the card which is requesting data from memory that the data presently on the backplane contains an error.

The memory will complete the data transfer regardless of whether a parity error occurs or not. That is, memory will continue to perform read (or write) cycles as long as they are requested by the processor or an I/O card. It is up to the card receiving the PE- signal to determine what action will be taken.

3.3.6 PARITY SENSE

Although the parity sense is set to ODD under normal operating conditions, it may be changed to EVEN sense under program control. This provides a means by which the parity generation/detection function may be tested for diagnostic purposes.

The sense of parity at any time is determined by the PS- line on the backplane. The PS- line is driven only by the processor. Parity sense is set to EVEN if the PS- line is low, and to ODD if the line is high.

The function of the parity circuit may be verified by writing a data location with a given parity, then changing the parity sense and accessing the same data location. The PE- line should go low during the access to signify that a parity error has occurred.

It is obvious, then, that assuming there are no hardware malfunctions, data can be accessed from memory without parity errors only if the parity sense during the access of data is the same as when that data was written into memory.

3.3.7 PARITY INDICATOR

A green LED is located on the front edge of the memory card and indicates the status of the parity checking operation of the memory. At power-on, the LED is turned on and will remain on under normal operating conditions. If, during any memory access (read cycle), a parity error is detected in the accessed data, the LED will be turned off when the PE- signal occurs. The PE- signal actually resets a flip-flop which drives the LED so that the LED will remain off after the PE signal occurs.

Operation of memory is not interrupted when the parity indicator LED is off so that it is possible for memory operation to continue. The LED is meant only to be an indication that a parity error has occurred sometime in the past. The LED may be reset under program control, or by performing a system power-on.

3.3.8 STANDBY MODE

When AC line power to the computer is interrupted, data stored in the RAM memory array is lost. If it is desired that data be retained during power interruptions, then power must be maintained on the memory card.

The memory card requires four source voltages for normal operation:

- +12M
- 12M
- +5M
- +5V

Only those voltages designated with an "M" are necessary for the memory to sustain data. The +5V source is necessary only for data transfers to and from memory. Whenever the +5V source is removed, the memory will automatically assume a standby mode and will maintain any stored data as long as the memory (M) voltages are present.

When +5V is re-applied after a power interruption, the memory automatically assumes fully operational status.

3.3.9 POWER SUPPLY CONFIGURATION

The memory card works with the power supply and battery backup option to route the necessary memory voltages to the memory and processor cards. A slide switch located at the rear of the memory card is used to select two modes of power supply operation: BATTERY and NORM.

With the slide switch set to NORM, the +12M and +5M voltages are connected directly to the +12V and +5V voltages, respectively. The -12M voltage is connected to -12V through a diode (cathode to -12V). Also, the MLOST- line on the backplane is shorted to ground. This assumes that the battery backup option is not installed in the computer so that memory voltages are derived directly from the main voltages. Thus, when AC line power fails, memory power also fails because there is no battery backup to sustain memory.

With the slide switch set to BATTERY, the memory voltages are separated from the main voltages and it is assumed that the battery backup option is installed in the computer. Also, the MLOST- line is no longer shorted to ground. Thus, when AC line power fails, memory power is sustained by the battery pack.

During normal operation (no power failure) with the battery backup option installed, the memory voltages still are derived from the main voltages but the connection between them is on the battery backup board. The batteries then are in a charge mode. See Section V of this document for more information about the battery backup board.

3.4 INTERFACE REQUIREMENTS

3.4.1 BACKPLANE INTERFACE

The memory card interacts with the rest of the computer system solely through the rear backplane connectors which carry all control signals, clock signals, data, and power.

The control signals can be divided into three main groups: handshake signals, handshake inhibit signals, and initialization signals. These signals are responsible for the initiation and termination of memory cycles, as well as the operational status of the memory card.

The clock signals, Fast Clock (FCLK), Refresh Clock (RCLK), and Slow Clock (SCLK) synchronize memory operation to the computer system and drive the refresh circuit counter.

Finally, although the memory card uses power, it also furnishes power to the memory voltages on the backplane whenever the battery backup option is not installed in the computer system. This is accomplished by a switch that connects the processor voltages directly to the memory voltages.

3.4.1.1 Main Handshake Signals

The main handshake signals consist of MEMGO-, BUSY-, and VALID-. MEMGO- is asserted by the processor or an I/O card to request a memory cycle. BUSY- is asserted by the memory to acknowledge receipt of MEMGO- and also to hold off any further memory requests until the pending cycle completes. VALID- is asserted by the memory to signify that the requested data is presently available on the backplane (read cycle), or that the data sent to memory has been written (write cycle). See figure 3-4 for timing details of these signals.

3.4.1.2 Handshake Inhibit Signals

The memory card can be inhibited from acknowledging memory requests initiated by MEMGO-. This is necessary when the processor executes virtual control panel code or self-test code directly from ROM's on the processor card, or when data transfers are requested from a remote memory.

Two signals are used to inhibit memory operation: REMEM- and MEMDIS-. The inhibit function is accomplished by asserting either inhibit signal at the same time that MEMGO- is asserted.

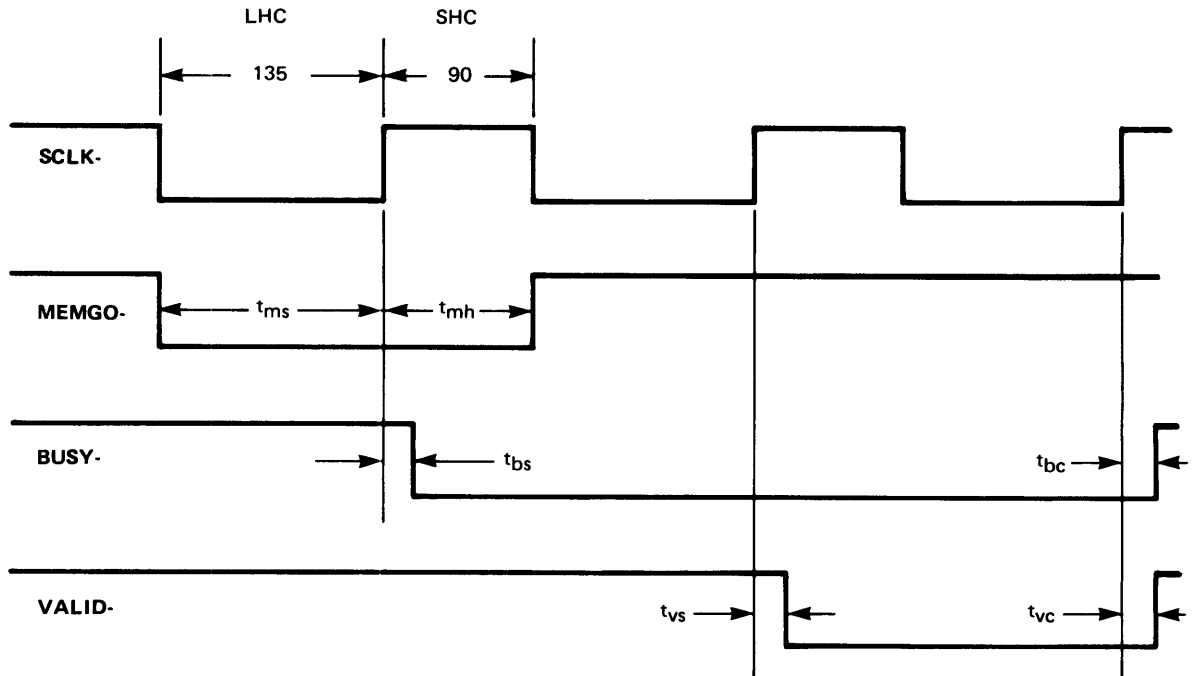
Figure 3-5 shows the timing of the inhibit signals, MEMGO-, and SCLK-. The only restriction on using either inhibit signal is that it must be active at the rising edge of SCLK- whenever MEMGO- is asserted.

3.4.1.3 Clock Signals

The memory requires the two system clocks, FCLK- and SCLK-, for memory cycle and refresh cycle timing. There are four restrictions that must be observed on these clock signals for proper memory operation:

- a. FCLK- must be exactly five times the rate of SCLK-.
- b. SCLK- must be synchronous with FCLK such that all transitions of SCLK- occur on the rising edge of FCLK-.
- c. SCLK- must have a waveform that is high for two FCLK- cycles and low for three FCLK- cycles (40 percent duty cycle).
- d. The period of FCLK- must not be less than 36 nsec. This produces an SCLK- period of not less than 180 nsec.

Please note that if the above restrictions are observed, memory speed can be altered merely by changing clock speed. If the SCLK- period is changed from 227 nsec, then the refresh counter must be modified to correct the refresh rate. (See paragraphs 3.3.3 and 3.7.8). There is no upper limit imposed on the FCLK- period.



MEMGO--SET UP TIME
 $t_{ms} > 10ns$

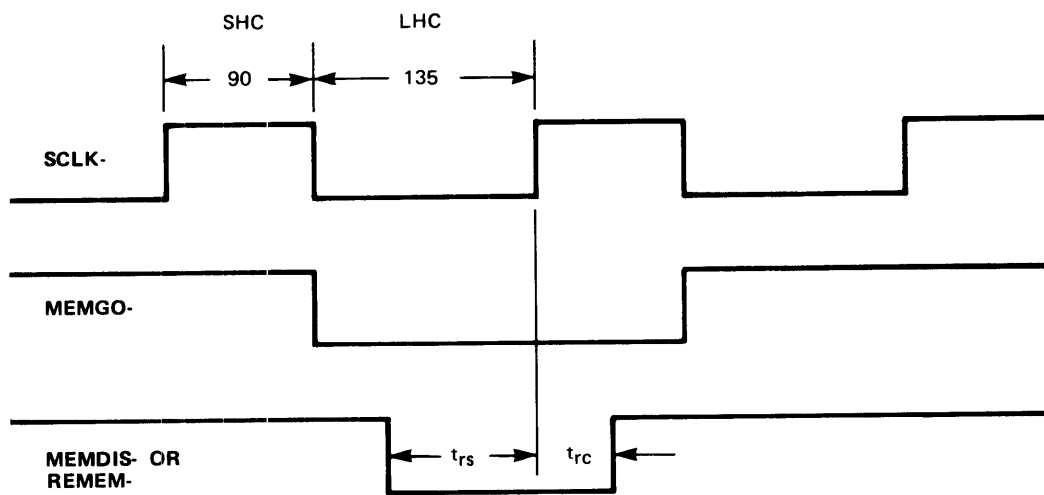
MEMGO- HOLD TIME
 $120ns < t_{mh} < 225ns$

BUSY- ASSERTION, CLEAR
 $0ns < t_{bs} < 70ns$

VALID- ASSERTION, CLEAR
 $0ns < t_{vs} < 49ns$

ALL TIMING RELATIVE TO
 SCLK- ON BACKPLANE

Figure 3-4. Handshake Timing



DISABLE SET-UP TIME
 $t_{rs} > 30\text{ns}$

DISABLE HOLD TIME
 $0 < t_{rc} < \text{SHC}$

Figure 3-5. Handshake Disable Timing

3.4.1.4 Initialization Signals

The memory monitors two control signals on the backplane for initialization purposes: PON+ (Power On) and CRS- (Control Reset).

PON+ is received by the memory through a D-type flip-flop. While this control signal is false (low), the memory will ignore any requests for a memory cycle. If the memory voltages are still present, however, memory refresh will still function and retain data stored in memory.

When the CRS- line is asserted (low), the parity valid indicator (LED) will be turned on.

3.4.1.5 Power Sequencing Requirement

Because of the type of RAMs used in memory, it is necessary that -5M be present at the RAMs before +12M is applied.

3.5 OPERATING CHARACTERISTICS

3.5.1 INITIALIZATION

When the memory card is installed in the computer system and power is applied (PON high), the memory array must be initialized by writing data into every location. This is necessary because the data bits in the memory array assume random states on an initial power turn-on so that incorrect parity will exist in many locations. It is the responsibility of the processor to write data (any data) into all memory locations so that correct parity is established in all locations.

3.5.2 INPUT DATA/ADDRESS SET-UP REQUIREMENT

When data is to be written to (or read from) memory, it is necessary to supply the address of the location where the data is to be written (or accessed). Also, in the case of a write, the data to be stored must be supplied on the data bus. A certain set-up requirement must be observed to guarantee proper memory operation under all conditions. See figure 3-6 for timing details.

3.5.3 WRITING DATA INTO MEMORY

To write data into memory, the memory requires four items from the external environment:

- a. A MEMGO⁻ signal to initiate the memory write cycle.
- b. The address of the memory location to which the data will be stored.
- c. Address bus bit 15 (R/W) cleared (low).
- d. The data to be written.

In response, the memory will assert the following signals:

- a. A BUSY⁻ signal to acknowledge the receipt of MEMGO⁻ and to hold off any further requests for a memory cycle.
- b. A VALID⁻ signal to signify that the data has been accepted and the write cycle is complete.

The above sequence of events is detailed in figure 3-6. It should be noted that the write cycle is the same whether it is a processor or DMA write.

3.5.4 READING DATA FROM MEMORY

To read data from memory, the memory requires three items from the external environment:

- a. A MEMGO⁻ signal to initiate the memory read cycle.
- b. The address of the memory location from which the data will be read.
- c. Address bus bit 15 (R/W) set (high).

In response, the memory will perform the following:

- a. Assert the BUSY⁻ signal to acknowledge the receipt of MEMGO⁻ and to hold off any further requests for a memory cycle.
- b. Assert the VALID⁻ signal to signify that the requested data is available on the backplane data bus.
- c. The memory drives the requested data onto the backplane data bus. The data is available +/- 50 nsec referenced to the trailing edge of VALID⁻.

(assuming an SCLK period of 180 nsec). The set-up and hold time increase with increases in the SCLK period.

The above sequence of events is detailed in figure 3-6. It should be noted that the read cycle is the same whether it is a processor or DMA read.

3.5.5 RECOVERY FROM PARITY ERRORS

Whenever a parity error occurs in data that is accessed from memory, the memory will notify the card requesting the memory cycle that a parity error has occurred by asserting the PE- signal on the backplane. Also, the parity indicator LED on the memory card will be reset (turned off). The memory is still able to perform any subsequent memory cycles without any resetting. The only resetting that should be done, as far as the memory is concerned, is to reset the parity indicator LED. This can be done under program control by issuing a CLC to select code 0. The indicator can also be reset by turning off and re-applying AC power to the system, regardless of the presence or absence of the battery back-up option.

3.6 FUNCTIONAL THEORY OF OPERATION

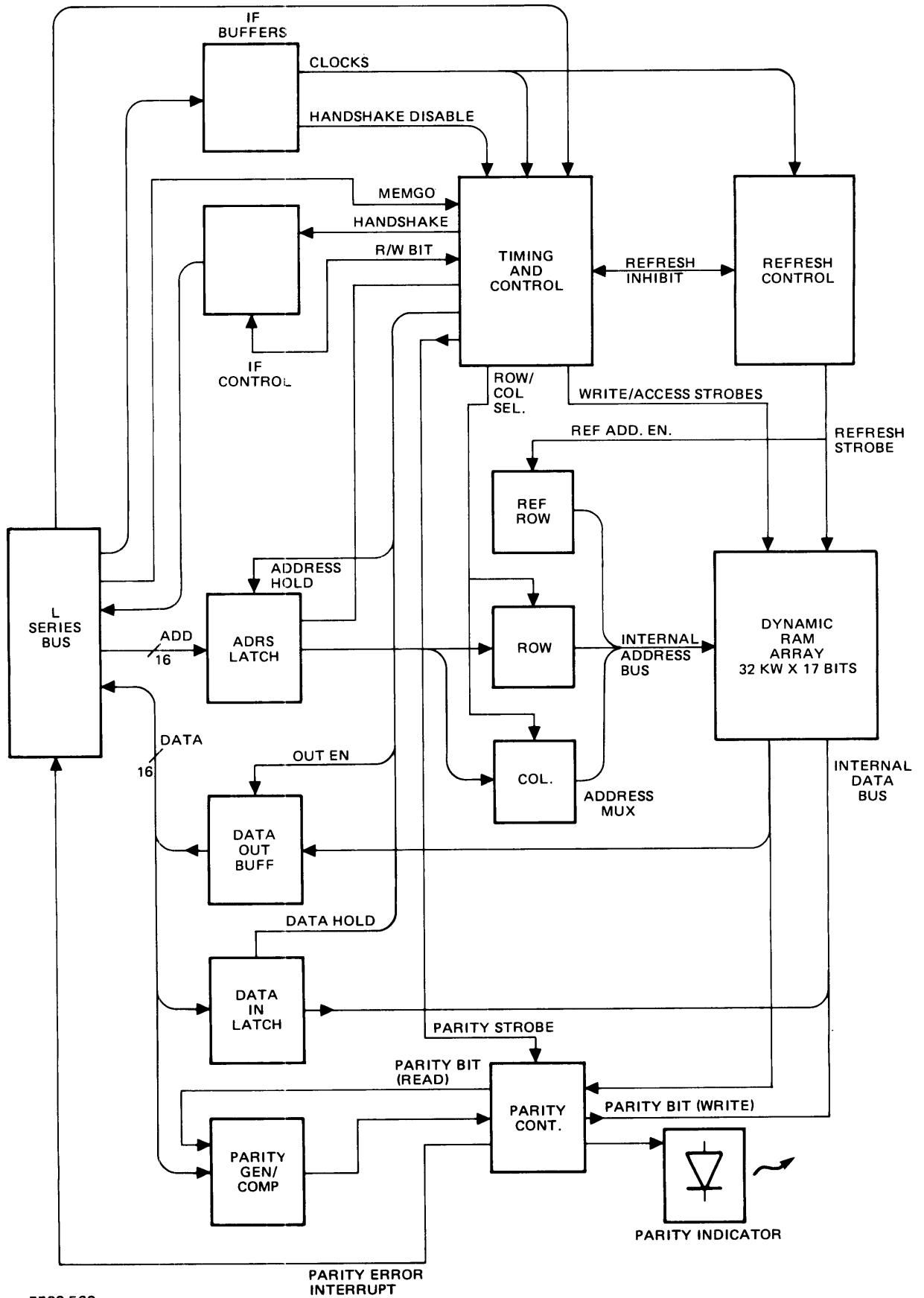
A functional block diagram of the memory card is shown in figure 3-7. The following paragraphs describe the function of each block.

3.6.1 INTERFACE BUFFERS

The interface buffers are composed of two sections of an S240 and are used to receive the clock signals (SCLK-, RCLK+, and FCLK-) and the handshake disable signal (REMEM-) from the backplane. They also are used to assert the handshake signals VALID- and BUSY- on the backplane during memory cycles.

3.6.2 ADDRESS LATCH

The address latch, composed of two S373 transparent latches, receives the address bits and the R/W bit (bit 15 of the address bus) from the backplane. The primary function of this latch is to store the address bits of a requested memory cycle while a refresh cycle is executing.



7700-560

Figure 3-7. Memory Functional Block Diagram

3.6.3 DATA-IN LATCH

The data-in latch, composed of two S374 latches, receives the data bits from the backplane to be stored in memory. The primary function of this latch is to store the data bits of a requested memory cycle while a refresh cycle is executing.

3.6.4 DATA-OUT BUFFER

The data-out buffer, composed of two S241 bus drivers, drives the backplane data bus with the requested data during read cycles.

3.6.5 PARITY GENERATOR/COMPARATOR

The parity generator/comparator is composed of two S280 parity detectors and is used to detect correct parity of data being accessed. Also, working in conjunction with the parity control circuit, the generator/comparator generates the parity bit to be stored with data on write cycles.

3.6.6 PARITY CONTROL

The parity control circuit is used to control:

- a. The writing of generated parity bits during write cycles.
- b. The presenting of parity bits for comparison on read cycles.
- c. The parity indicator LED.

3.6.7 PARITY INDICATOR

The parity indicator LED indicates if a parity error has occurred. If the LED is ON, the parity is valid; if OFF, a parity error has occurred.

3.6.8 ADDRESS MULTIPLEXER

The address multiplexer is composed of three 240-type bus drivers and is used to present the row and column addresses to the RAMs during memory cycles, and the refresh row address during refresh cycles.

3.6.9 DYNAMIC RAM ARRAY

The dynamic RAM array is the main memory array used for the storage of data. It is composed of 34 16K-bit RAMs ($K = 1024$) which store the 16 bits of each data word plus a parity bit for a total of 32,768 words of memory.

3.6.10 TIMING AND CONTROL

Timing and control is a general term and refers to all the circuitry needed to:

- a. Control the actions of storing and retrieving data.
- b. Latching in data and addresses.
- c. Issuing the parity error signal.
- d. Controlling row-to-column multiplexing for the RAMs.
- e. Supplying read/write strobes to memory.
- f. Supplying the handshake control signals.

3.6.11 REFRESH CONTROL

The refresh control circuitry generates refresh row addresses and periodic refresh cycles for the retention of data in the RAMs.

3.7 THEORY OF OPERATION

The following paragraphs contain detailed theory of operation for the memory. Refer to the schematic diagram (drawing numbers D-12004-60001-51 and D-12004-60001-52, located at the rear of this section), as necessary.

3.7.1 INTERFACE BUFFERS

The interface buffers consist of two sections of a 74S240 line driver (U516). One section (permanently enabled by a ground connection at U516-19) receives REMEM- and the three clock signals FCLK-, RCLK+ and SCLK- from the backplane and buffers these signals for use on the memory card.

The other section of the buffer drives the BUSY- and VALID- handshake signals to the backplane. This buffer normally presents a high impedance to the backplane. When the handshake signals are to be asserted on the backplane, the IBUSY+ signal occurs first and gates itself onto the backplane through U52-6. When BUSY- and VALID- are de-asserted, the buffer is held enabled by CAS+ (U52-5), which is de-asserted one SHC later. The reason for this is that when BUSY- and VALID- are de-asserted, the backplane is driven to the inactive states for these signals much faster than if it were allowed to return to the inactive state by the pull-up on the processor alone.

These signals are shown in the timing diagram in figure 3-8.

3.7.2 ADDRESS LATCH

The address latch consists of two 74S373 transparent latches (U116 and U117). These latches are frozen at the beginning of every requested memory cycle, whether a refresh cycle is in progress or not. That is, whenever a memory cycle is requested, the address latch will latch the address bits while they are available on the backplane regardless of whether the memory is idle or performing a refresh.

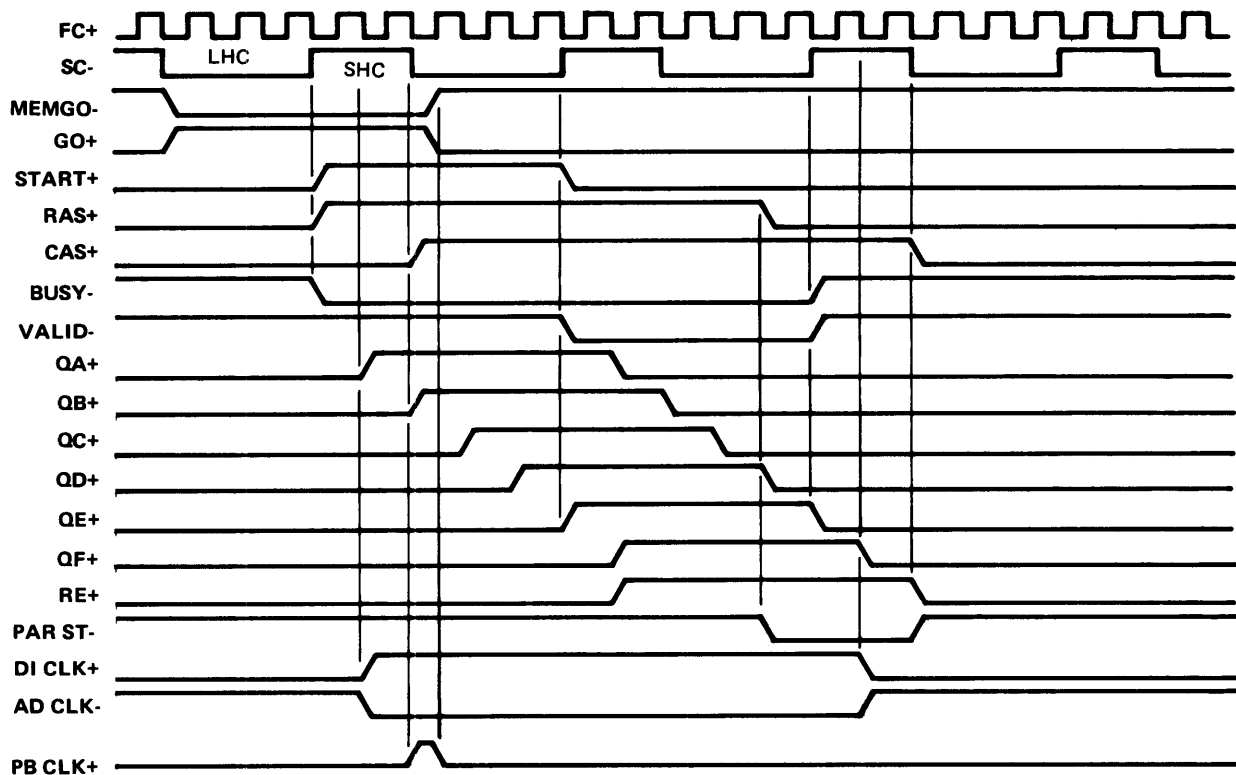


Figure 3-8. Memory Cycle Timing

The sequence of events is as follows: a MEMGO- pulse is received at U49-11 and appears inverted at U49-13. The resulting MEMGO+ signal appears at the J input of the BUSY flip-flop, U53-11. On the falling edge of SCLK+, the BUSY flip-flop sets (U53-9 goes high), which asserts BUSY- on the backplane and also sets the J input of the DI flip-flop (U43-11) high. On the falling edge of FCLK+, which occurs one FCLK cycle after the falling edge of SCLK+, the output of the DI flip-flop sets (U43-9 high, U43-7 low). The AD CLK- line, coming from U43-7, goes low and freezes the address latches at this point.

The K input to the DI flip-flop (U43-12) is connected to the complementary output of the BUSY flip-flop (U53-7). As a result, since the DI flip-flop is clocked by FCLK+, its output will follow the corresponding output of the BUSY flip-flop delayed by one FCLK cycle. The AD CLK- line, therefore, will be asserted (low) one FCLK cycle after BUSY is asserted and will be de-asserted one FCLK cycle after BUSY is de-asserted.

3.7.3 DATA-IN LATCH

The data-in latch consists of two 74S374 latches (U46 and U414). These latches are controlled by the DI CLK+ signal from the DI flip-flop (U43, described in paragraph 3.7.2).

The data-in latch receives the data bits from the backplane to be stored in memory. The operation is the same as the address latch, described in paragraph 3.7.2.

3.7.4 DATA-OUT BUFFER

The data-out buffer consists of two 74S241 line drivers (U44 and U413), and drives the requested data onto the backplane data bus during read cycles. The buffer is enabled to drive the backplane by both the RE+ and RE- control signals from the RE flip-flop at U43-5 and U43-6, respectively. These outputs only occur during read cycles and are generated as described in the following paragraphs.

A MEMGO- pulse is sent to the memory card to initialize a read cycle. At the next falling edge of SCLK+, the BUSY flip-flop (U53) is set. One FCLK later, the DI flip-flop (U43) sets, latching in the address of the requested data. Note that bit 15 (R/W) of the address bus is used to signify whether the requested memory cycle is a write or read cycle. In the case of a read cycle, this line is asserted high. This line is routed to the "out enable" AND gate (U417-4), which enables the RE flip-flop for operation during this memory cycle.

On the falling edge of FCLK+, corresponding with the next falling edge of SCLK+, the VALID flip-flop (U610) sets (enabled by QD from the shift register at U66). The IVALID+ signal appears at U417-5, setting the "out enable" AND gate high, enabling the RE flip-flop. One FCLK cycle later, the RE flip-flop sets and the data-out buffers drive the requested data onto the backplane.

The RE flip-flop remains set as long as the DI flip-flop remains set. When the BUSY flip-flop is reset towards the end of the memory cycle, its complementary output (U53-7) goes high, enabling the K input on the DI flip-flop (U43-12). On the next falling edge of FCLK+, the DI flip-flop resets and its complementary output (U43-7) goes high, enabling the K input of the RE flip-flop (U43-2). The next falling edge of FCLK+ resets the RE flip-flop and the data-out buffer is disabled.

Thus, the data-out buffer is disabled two FCLK cycles after the reset of BUSY and one FCLK cycle after the reset of DI CLK+.

Note that RE is de-asserted two FCLK cycles after VALID- is de-asserted. Because the trailing edge of VALID- is used to clock data from the memory, the data is held on the backplane for these two FCLK cycles to satisfy data hold-time requirements.

3.7.5 PARITY CIRCUIT

The general term "parity circuit" refers to all the circuitry necessary for the memory card to perform the parity generation and detection function, the writing of correct parity into memory during write cycles, and the control of the parity indicator LED.

The main part of the circuit consists of two 74S280 parity generator/detector circuits (U47 and U416). These circuits monitor data on the backplane constantly; and create the necessary information for checking the parity of accessed data and writing the parity bit for stored data. The following paragraphs describe the parity generation and detection sequence; figure 3-8 shows the timing.

3.7.5.1 Parity Generation

The parity generator circuit generates the parity bit which is stored with the data during any write cycle. When the PS- line (U47-4) is low, the sense of the parity generator is said to be EVEN, that is, the generator will insure that the summation of all set data bits in a data word PLUS the corresponding parity bit will equal an even decimal number in any given location in memory. The two S280 parity generators each have two outputs, labeled E (even) and O (odd). These outputs are true (high) whenever the parity of the data on the inputs is even or odd, respectively. Because each generator monitors eight

data lines, the four outputs of the generators (two E and two O outputs) must be combined to generate parity for the 16-bit data word.

The E output of either generator will be true whenever there is an even number of ones at their respective data inputs. Note that the PS line forms one input for the parity generator at U47. Since this line is high for normal operation, the only way the E output will be high on this generator is if there are an ODD number of data bits on its remaining inputs. Therefore, if both E outputs are true, this signifies that there is an odd number of data bits set (an even number on U416 and an odd number on U47). This is the condition for ODD parity, and as a result, the parity generator must not set the parity bit.

A similar argument holds for the O outputs, U416 will have its O output set if there an odd number of bits set. U47 will have its O output set only if there are an EVEN number of data bits set (because the PS line also is high). This again is the condition for ODD parity and the parity bit must not be set.

Because the occurrence of either pair of outputs being true signifies that the parity bit should be clear, or, in Boolean terms,

$$\begin{pmatrix} E & \cdot & E \\ A & & B \end{pmatrix} + \begin{pmatrix} O & \cdot & O \\ A & & B \end{pmatrix} := \bar{P}$$

this function is implemented by a 74S51 (U411). The output at U411-6 is false (low) whenever the data has odd parity and true for even parity. The parity bit written into memory is set whenever the data has even parity, thus preserving the odd parity requirement. Note that the PS- line is high for odd parity, which is normal operation.

When a MEMGO- pulse is received by the memory card, the data to be written is available after the beginning of the next SHC of SCLK. Data must be valid on the backplane by the falling edge of FCLK+ occurring midway into the SHC. It is at this point that the data is latched into the input buffers. The next FCLK cycle is used to allow the parity generator to perform the comparison and present the parity bit at U411-6. On the next rising edge of SCLK+, the PB CLK+ line (U417-8) goes high, clocking the D flip-flop at U57-11. The parity bit that was generated is now latched at U57-9 and is available at the parity RAM input.

3.7.5.2 Parity Detection

When data is driven onto the backplane by the memory, it is monitored by the parity detector circuits for correct parity. The parity comparison described under parity generation (starting with paragraph 3.7.5.1) for a write cycle, is the same as the parity detection performed on a read cycle (described here) with one important exception: The parity bit in memory on a write cycle is presented to the detector at U416-4; the parity bit on a read cycle is enabled to the detector by RE+ at U417-1.

As discussed under parity generation, the parity bit is set when the two generators detect different summation senses, that is, the E output is true on one generator when the O output is true on the other generator, and vice versa. On a read out of memory of stored data, if the senses are opposite, the parity bit presented to U416 will be set and change its sense to match that of U47. Thus, the output of U411-6 will go low during the data access.

Similarly, if the senses are the same during the access, the parity bit will be low when presented to U416 and will not change its sense. The output at U411-6 will again be low.

This output is used to generate the PE- signal. U411-6 will always be low when the parity of accessed data is correct.

During a data access from memory, the RE+ signal is asserted to enable the data-out buffers (U44, U413). This signal also enables the parity interrupt circuit at U59-13 and U63-13. The data will have settled by the time the row-address-strobe (RAS+) pulse is de-asserted and this event is used to generate the parity strobe (PAR ST-). The PAR ST- signal comes from U410-6, being initiated by the trailing edge of RAS+ and terminated by the trailing edge of CAS-.

If the parity of the output data is incorrect, U411-6 will be high and U59-11 will be low. On the leading edge of PAR ST-, the output at U49-10 will go high and be gated onto the backplane at P2-10 (PE-). Also, the parity indicator flip-flop (U49-6) will be reset, turning off the parity indicator LED.

On the trailing edge of the PAR ST- signal, the PE- signal will be de-asserted but the parity indicator flip-flop (U49) will stay reset. This flip-flop can only be reset by U64-11 going high by either a CRS- or PON-.

3.7.6 ADDRESS MULTIPLEXER

The address multiplexer is composed of two 74S240 drivers (U113 and U114) and one LS240 driver (U110). These drivers provide the refresh row address, and the row and column address to the RAM address lines. The triple, 3-input NAND gate (U17) provides an interlock to prevent more than one driver from driving the RAM address bus simultaneously.

During refresh cycles, the row and column address drivers are disabled by the RC- signal appearing at U17-2 and U17-5. The RC+ signal enables the refresh row address driver to drive the bus with the refresh address from U19.

At times other than during refresh cycles, the row and column address drivers are enabled (not simultaneously) to drive the address bus. The selection of which driver is enabled is done by the CAS+ and CAS signals. At all times

that CAS is not asserted, the row address driver is enabled. During a memory cycle, as the address of the desired memory location appears on the backplane, the low-order seven bits (bits 0-6) appear directly at the RAM array through the enabled row address driver. When the CAS signal is asserted, the row address driver is disabled and the column driver is enabled, presenting the next seven bits of the memory address (bits 7-13) and the CAS- signal to the RAM array. The cross coupling on U17 at U17-3, U17-12, U17-1, and U17-6 is an interlock preventing the enabling of one driver until the other driver is disabled.

3.7.7 DYNAMIC RAM ARRAY

The dynamic array is composed of 34 RAM elements which are the storage elements on the memory card. Each RAM is a 16K x 1 array, thus 16 of them form a 16K times 16 or a 16K, 16-bit word memory array. Because a parity bit is needed for each word, a 17th RAM is needed for 16K words plus 16K parity bits. As a result, 17 RAM elements are needed for each 16K words of memory.

The array is arranged in two rows of 17 RAMs each, thus each row contains 16K words of memory. The address multiplexer can only address 16K words of memory (14 bits), however, so there must be a way of selecting which row is being addressed during memory cycles. This is accomplished by address bus bit 14. This bit appears at U54-1 and U59-1. When refresh cycles are not occurring, this bit controls the selection of the two memory rows. When bit 14 is clear, the input at U63-4 is high, enabling the RAS signal to row 0. When bit 14 is set, the input at U63-1 is high, enabling the RAS signal to row 1. See paragraph 3.7.8 for operation during refresh cycles.

For the reading or writing of data in memory, the RAM elements require the address bits of the desired location, the row address strobe (RAS), column address strobe (CAS), and the write enable signal (WE).

The address bits are supplied to the RAM elements as described in paragraph 3.7.6. The RAS signal occurs during every memory cycle, being generated by U54-11 by the ORing of the START pulse and the QD output of shift register U66. This signal is routed to either row as described in the previous paragraph. The CAS signal is generated by U53-5 during memory cycles and occurs one SHC after RAS. CAS is presented to the RAMs by U114-3. The write enable signal is derived from address bus bit 15 and appears as a positive true signal at U63-10. This signal is set up at the time the address is valid on the backplane. It must be valid at the RAMs by the time CAS- is presented to the RAMs. The write enable signal is disabled from the RAMs during refresh cycles by U63-9 being low. If the write enable signal is not asserted, the RAM array defaults to read mode.

3.7.8 MEMORY REFRESH CIRCUIT

The refresh circuit provides refresh row addresses and refresh pulses at regular intervals to sustain data in memory.

The refresh intervals are generated by a 74LS390 (U16). The RAM elements must be refreshed every two milliseconds and because there are 128 row addresses in each memory row, the refresh circuit must produce 128 refresh cycles every two milliseconds. (During refresh cycles, corresponding RAMs in each memory row are refreshed simultaneously.) The 128 refresh cycles every two msec necessitates a refresh cycle every 16 microseconds. Since the refresh counter is clocked by RCLK (U16-1), and RCLK has a period of 227 nsec, a divide-by-70 count is required. The outputs of U16 are monitored by U510-12 and 13 for the correct count and a reset is generated through U54-8. The output at U16-13 then has a positive transition every 16 usec, and this edge is used to initiate refresh cycles at the Refresh Pending (RP) flip-flop at U611-13.

Refer to figure 3-9 for the following discussion.

When a negative edge occurs at U611-13, the RP flip-flop sets and, if BUSY is not asserted, a high will appear at the input to the Refresh Start (RS) flip-flop at U613-11. On the next falling edge of SCLK-, the RS flip-flop sets and immediately sets the Refresh Cycle (RC) flip-flop. In addition, a pulse is sent from U59-8 to enable the START flip-flop to start the shift register sequence.

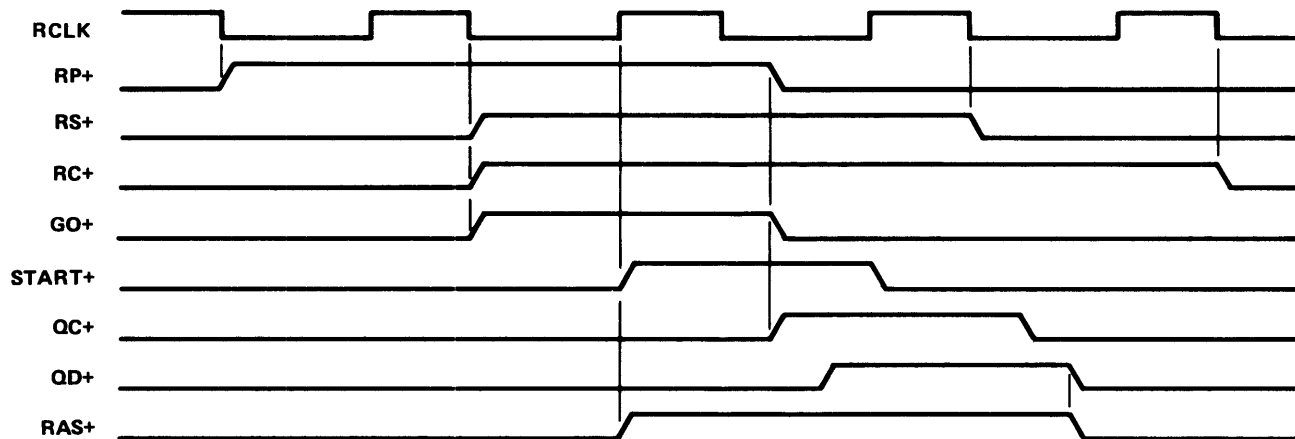


Figure 3-9. Memory Refresh Cycle

Once the RC flip-flop sets, the memory is inhibited from performing memory cycles by the following inhibit points: U53-15 and U610-15 asserted low and U69-9 asserted high. RC+ also goes to U17-10 to clock the Refresh Address counter (U19) and enable the Refresh Row address driver. Note that the occurrence of each refresh cycle increments U19.

As the START pulse occurs and progresses through the shift register at U66 (clocked by FCLK), the RAS+ pulse is generated at U54-11 and appears at both memory rows through U63. When the Qc output of the shift register occurs, it resets the Refresh Pending flip-flop at Q11-14. This sets up the inputs of the Refresh Start flip-flop to be reset on the next falling edge of SCLK-. After this occurs, the K input of the Refresh Cycle flip-flop gets set and on the next falling edge of SCLK-, the RC flip-flop resets, ending the refresh cycle.

Note that the output of NAND gate U64-8 normally stays high at all times. This insures that the refresh circuit attains the proper state on the initial power turn-on.

3.7.9 MAIN CONTROL CIRCUIT

All cycles of the memory, whether memory or refresh cycles, are initiated by the AND-OR invert gate U64. The Boolean equation below will aid in understanding the combinational function of this gate.

$$(\overline{\text{MEMGO-}} + \overline{\text{MEGO-}} + \overline{\text{PONB+}} + \overline{\text{RS-}}) \cdot (\overline{\text{REMEM+}} + \overline{\text{PONB+}} + \overline{\text{RS-}}) \cdot (\overline{\text{RCB+}} + \overline{\text{RS-}}) \cdot (\overline{\text{PONB-}} + \overline{\text{RS-}}) = \text{GO+}$$

The + or - at the end of each term signifies the active state of that signal at the input of U64.

The appearance of the Refresh Signal (RS-) in all groups in the equation indicates that when a refresh cycle starts, the GO+ signal is asserted regardless of the condition of the other signals (including the power-on signal PONB).

The PONB- signal in term four prevents any cycles except refresh cycles from occurring during power down.

The REMEM+ signal in the second term prevents any memory cycles from occurring while it is asserted.

Memory cycles are initiated by MEMGO- (in term one in the above equation) under normal conditions, and by MEGO- (also in term one) when a memory cycle is held off by a refresh cycle (this is explained in paragraph 3.7.11).

When a GO+ signal is received by the START flip-flop at U610-11, START+ will be asserted on the next falling edge of SCLK+, enabling the input of the shift register at U66-3. The shift register, which is clocked by FCLK-, produces shifted pulses which are used to generate the RAS signal, enable the inputs of the various control flip-flops, and provide resets for the refresh circuit, the START flip-flop, and the MEGO flip-flop.

3.7.10 MEMORY CYCLE SEQUENCE

When a memory access is initiated, an I/O card or the processor card asserts MEMGO-, which appears at U69-12. If no refresh cycle is occurring, then GO+ appears at U69-8 and enables the START flip-flop. On the rising edge of the next SHC, the START flip-flop sets and enables shift register U66. At this time, the address for the desired memory location is valid on the backplane and is set up through U116, U117, and U113 to the inputs of the RAMs.

When the START+ signal is asserted, the RAS+ signal appears at U54-11 and then, through U63, is asserted at the RAMs, strobing in the row address. BUSY- is asserted on the same SCLK+ edge as START+, being enabled by MEMGO- through U49-13.

One FCLK cycle later, the DI+ and AD CLK- signals are asserted, latching in the data and address and holding them for the duration of the memory cycle. On the falling edge of SCLK-, the parity bit is clocked to the parity RAM at U57-9 and CAS+ is generated by U53. This signal then disables U113 and enables U114, presenting the column address and the CAS- signals to the RAMs.

When the QE signal appears at the shift register (U66) output, the START flip-flop is reset. At the same time, VALID- is asserted on the backplane to signify that data is about to become valid (on the backplane). One FCLK cycle later, RE+ is asserted, enabling the accessed data to the backplane. When the QD output of the shift register resets, the RAS+ signal is released, causing the PAR ST- signal to be asserted at U410-6. This signal will cause a parity interrupt to be generated if data parity is incorrect.

BUSY- is released on the next SHC of SCLK. The VALID- signal also is released, clocking data out of the memory card. RE+ and CAS+ are released one SHC later to satisfy data hold time requirements.

3.7.11 MEMORY CYCLES OCCURRING DURING REFRESH CYCLES

Refer to figure 3-10 for timing information concerning the signals in the following discussion.

Whenever a refresh cycle is in progress, the memory cannot service a request for a memory cycle. Instead, the memory card must store the data and address for the requested memory cycle, allow the refresh cycle to complete, and then perform the suspended memory cycle.

When a refresh cycle is in progress, the MEGO flip-flop (U611) is enabled to monitor requests for memory cycles. This results from U410-10 being low, allowing SCLK+ to clock the MEGO flip-flop. When a MEMGO- is received, the MEGO flip-flop is set and it immediately sets the BUSY flip-flop. This prevents any subsequent requests for memory cycles until the present cycle is serviced.

As in a normal memory cycle, the DI+ and AD CLK- signals occur one FCLK cycle after BUSY is set and latch in the data and address.

After the refresh cycle completes, a memory cycle is initiated immediately (U69-11 goes low because the MEGO flip-flop (U611) is set). The memory cycle proceeds in normal fashion, with the MEGO flip-flop being reset on the QD pulse from the shift register (U66). Note that QD could not reset MEGO during the refresh cycle because U59-4 was held low at this time.

3.7.12 REFRESH CYCLES OCCURRING DURING MEMORY CYCLES

When a memory cycle is in progress, refresh cycles are held off. This results from the BUSY- signal appearing at U510-1, disabling the RP signal from appearing at the Refresh Start flip-flop (U613).

When the BUSY signal is released at the end of the memory cycle, RS and RC are asserted at the next falling edge of SCLK- so that a refresh cycle can start immediately.

Refresh cycles can only be held off for one memory cycle by the above sequence, and thus cannot be held off indefinitely by recurring memory cycles.

See figure 3-11 for timing details of refresh cycles occurring during memory cycles.

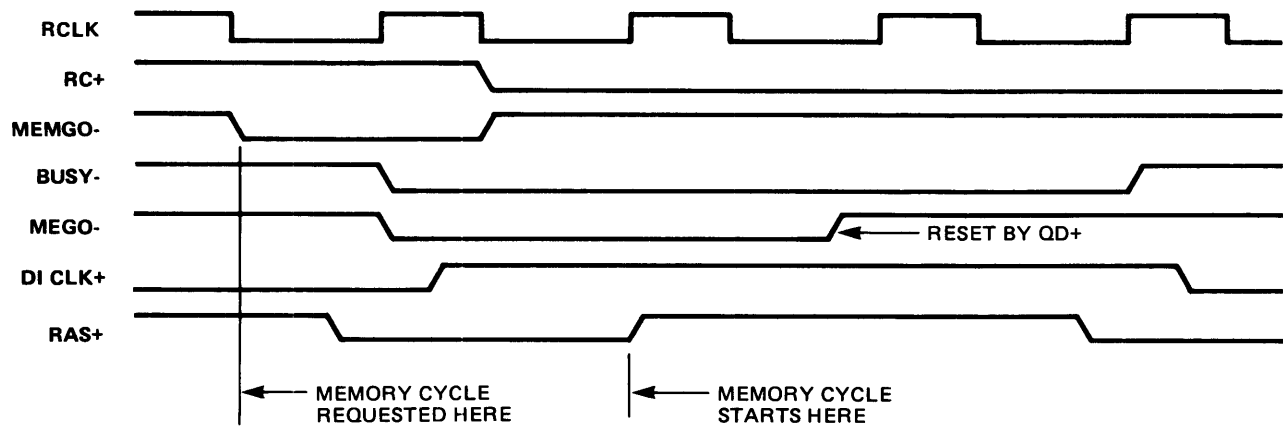


Figure 3-10. Refresh Cycle Holding off Memory Cycle

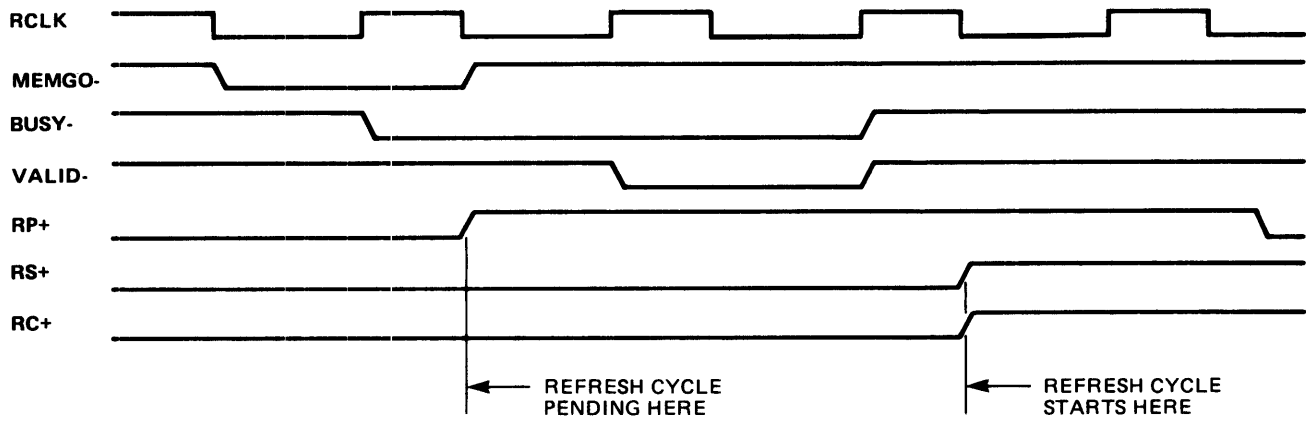


Figure 3-11. Memory Cycle Holding Off Refresh Cycle

3.7.13 PON INITIALIZATION

The PON+ signal is received by the memory card through a D type flip-flop (U57). When power is initially applied to the memory card, an RC time delay consisting of R12, C2, and U64 insures that the PON flip-flop initializes to the clear state.

Before PON+ appears on the backplane, the memory card is held in a reset state, that is, memory cycles cannot be initiated. Refresh cycles are performed, however, and will continue to do so in the absence of PON+ as long as +5M is present.

When PON+ appears on the backplane, it is clocked into the memory card by the refresh signal at U57-3. This enables the memory card for normal operation.

3.7.14 TEST POINTS AND DIAGNOSTIC FUNCTIONS

The memory card contains three power supply test points to verify the status of the -5M, +5M, and +12M voltages. These test points are located at the front of the memory card (see figure 3-12) and are isolated by series resistors to prevent accidental loading of the supply voltages.

TTL signals may be applied to the four locations listed below to check the refresh circuit function on the memory card.

| LOCATION | DESIGNATION | DESCRIPTION |
|----------|-------------|--|
| U54-1 | REF DIS- | A ground on this test point will cause the refresh circuit to stop functioning. Used with EXT RO- to vary refresh oscillator rate. |
| U510-4 | EXT RO- | An external oscillator may be applied at this point (with a ground connected to REF DIS-). The external oscillator will then be considered the refresh oscillator by the memory. |
| U17-9 | OSC- | A ground on this point will not stop refresh cycles but will prevent the generation of incremental row addresses. |
| U67-3 | INIT- | A ground on this point will reset the refresh counter and refresh generator to their initial state. |

3.8 PARTS LOCATIONS

Parts locations for the memory card are shown in figure 3-12.

3.9 PARTS LIST

The parts list for the memory board is shown in table 3-1. Refer to table 6-39 for the names and addresses of manufacturers of the parts.

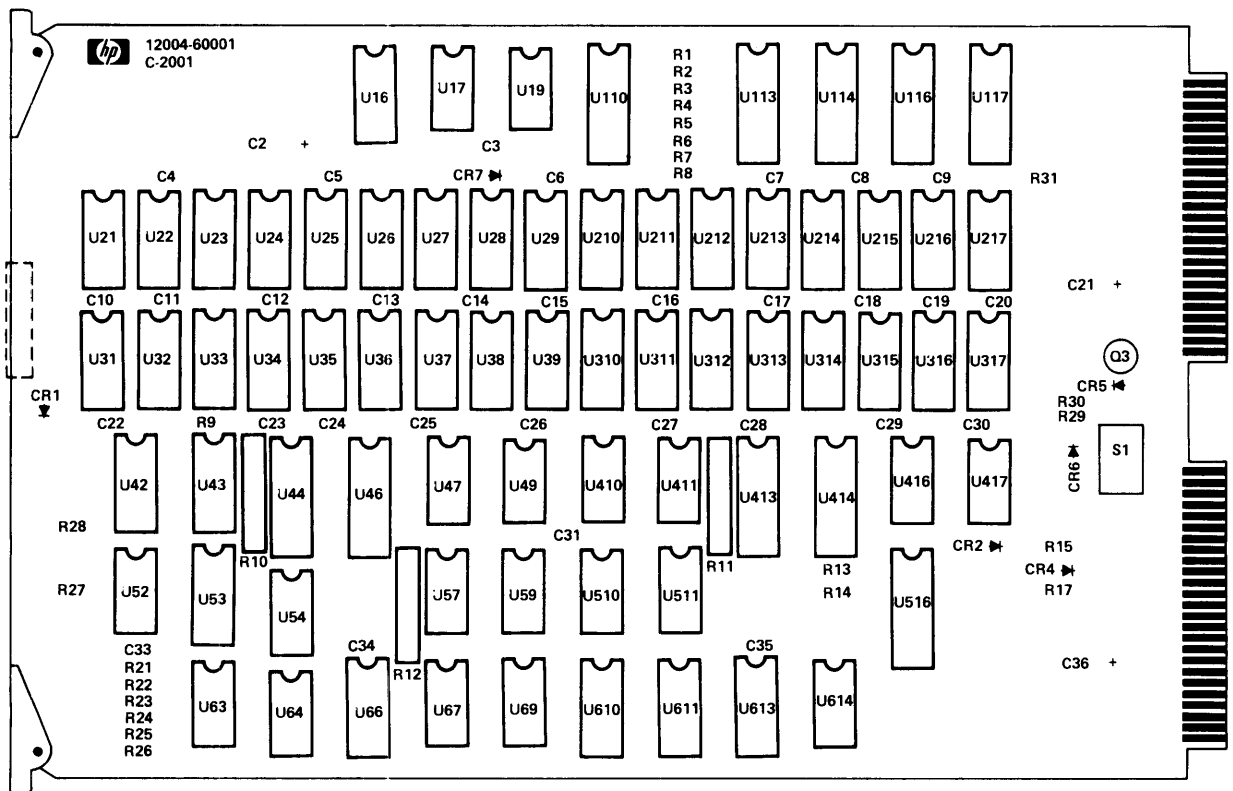
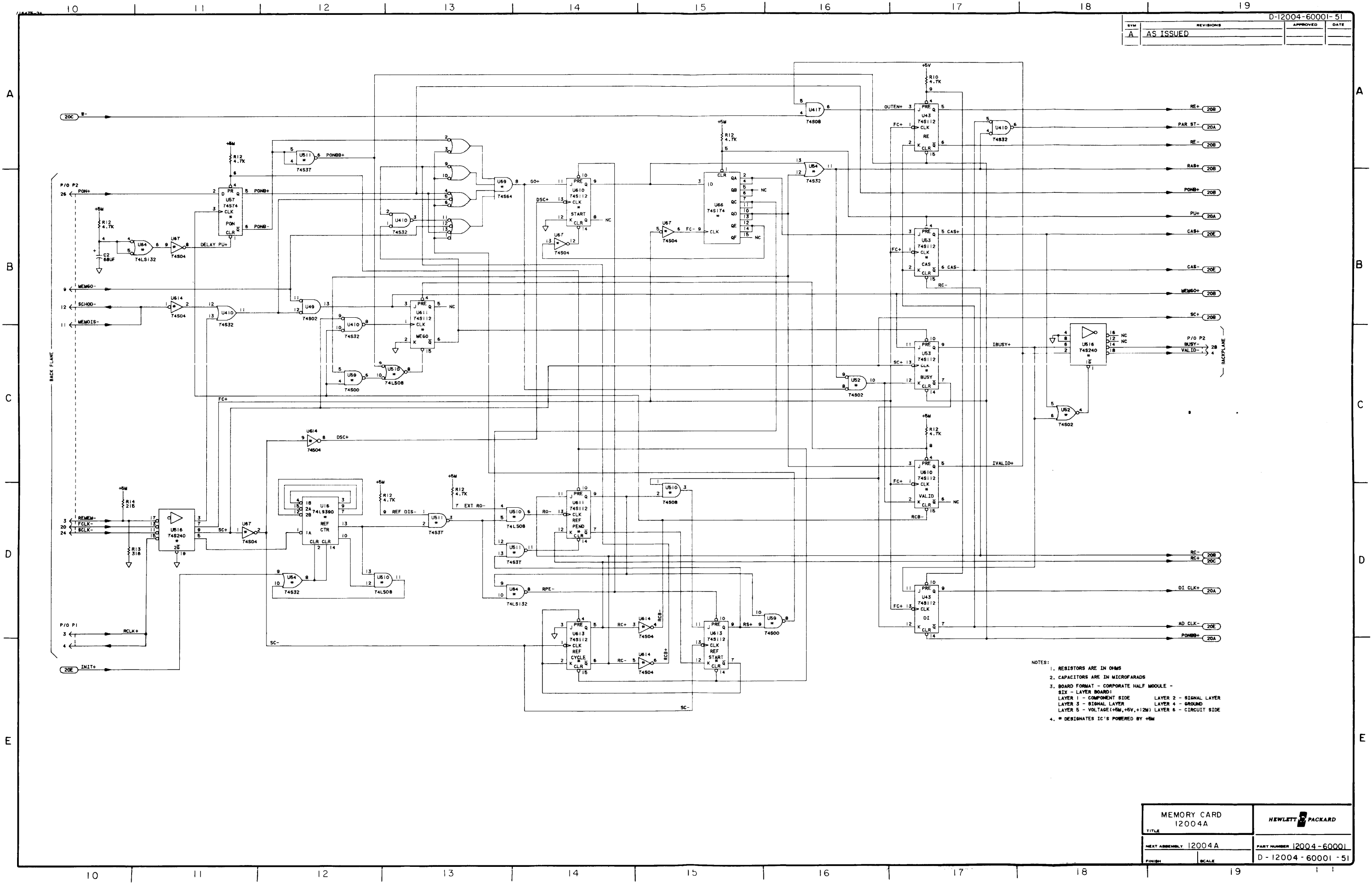


Table 3-1. Memory Card Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|---|----------|-------------------|
| | 12004-64001 | 2 | 1 | ASSEMBLY-64KB MEMORY | 28480 | 12004-64001 |
| C3 | 0160-4842 | 6 | 31 | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C4 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C5 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C6 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C7 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C8 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C9 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C10 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C11 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C12 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C13 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C14 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C15 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C16 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C17 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C18 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C19 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C20 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C22 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C23 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C24 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C25 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C26 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C27 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C28 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C29 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C30 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C31 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C33 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C34 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C35 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| CR1 | 1990-0485 | 5 | 1 | LED-VISIBLE LUM-INTE=800UCD IF=30MA=MAX | 28480 | 5082-4984 |
| CR2 | 1901-0731 | 7 | 1 | DIODE-PWR RECT 400V 1A | 28480 | 1901-0731 |
| CR4 | 1902-3105 | 7 | 1 | DIODE-ZNR 5.62V 2% DO-35 PD= 4W | 28480 | 1902-3105 |
| CR5 | 1902-3114 | 8 | 1 | DIODE-ZNR 6.19V 2% DO-35 PD= 4W | 28480 | 1902-3114 |
| CR7 | 1901-1080 | 1 | 1 | DIODE-SCHOTTKY 1N5617 20V 1A | 28480 | 1901-1080 |
| Q3 | 1A54-0215 | 1 | 1 | TRANSISTOR NPN SI PD=350MA FT=300MHZ | 04713 | 2N3904 |
| R1 | 0757-0294 | 9 | 11 | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R2 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R3 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R4 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R5 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R6 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R7 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R8 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R9 | 069B-3447 | 4 | 6 | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R10 | 1A10-0279 | 5 | 3 | NETWORK-RES 10-S1P4.7K OHM X 9 | 01121 | 210A472 |
| R11 | 1A10-0279 | 5 | | NETWORK-RES 10-S1P4.7K OHM X 9 | 01121 | 210A472 |
| R12 | 1A10-0279 | 5 | | NETWORK-RES 10-S1P4.7K OHM X 9 | 01121 | 210A472 |
| R13 | 069B-3444 | 1 | 1 | RESISTOR 316 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-316R-F |
| R14 | 069B-3441 | 8 | 2 | RESISTOR 215 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-215R-F |
| R15 | 069B-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R17 | 069B-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R21 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R22 | 069B-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R23 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R24 | 069B-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R25 | 0757-0294 | 9 | | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R26 | 069B-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R27 | 0757-0280 | 3 | 2 | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| R28 | 0757-0280 | 3 | | RESISTOR 1K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1001-F |
| R29 | 0757-0417 | 8 | 1 | RESISTOR 562 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-562R-F |
| R30 | 069B-3441 | 8 | | RESISTOR 215 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-215R-F |
| R31 | 069B-3155 | 1 | 1 | RESISTOR 4.64K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-4641-F |

Table 3-1. Memory Card Parts List (Continued)

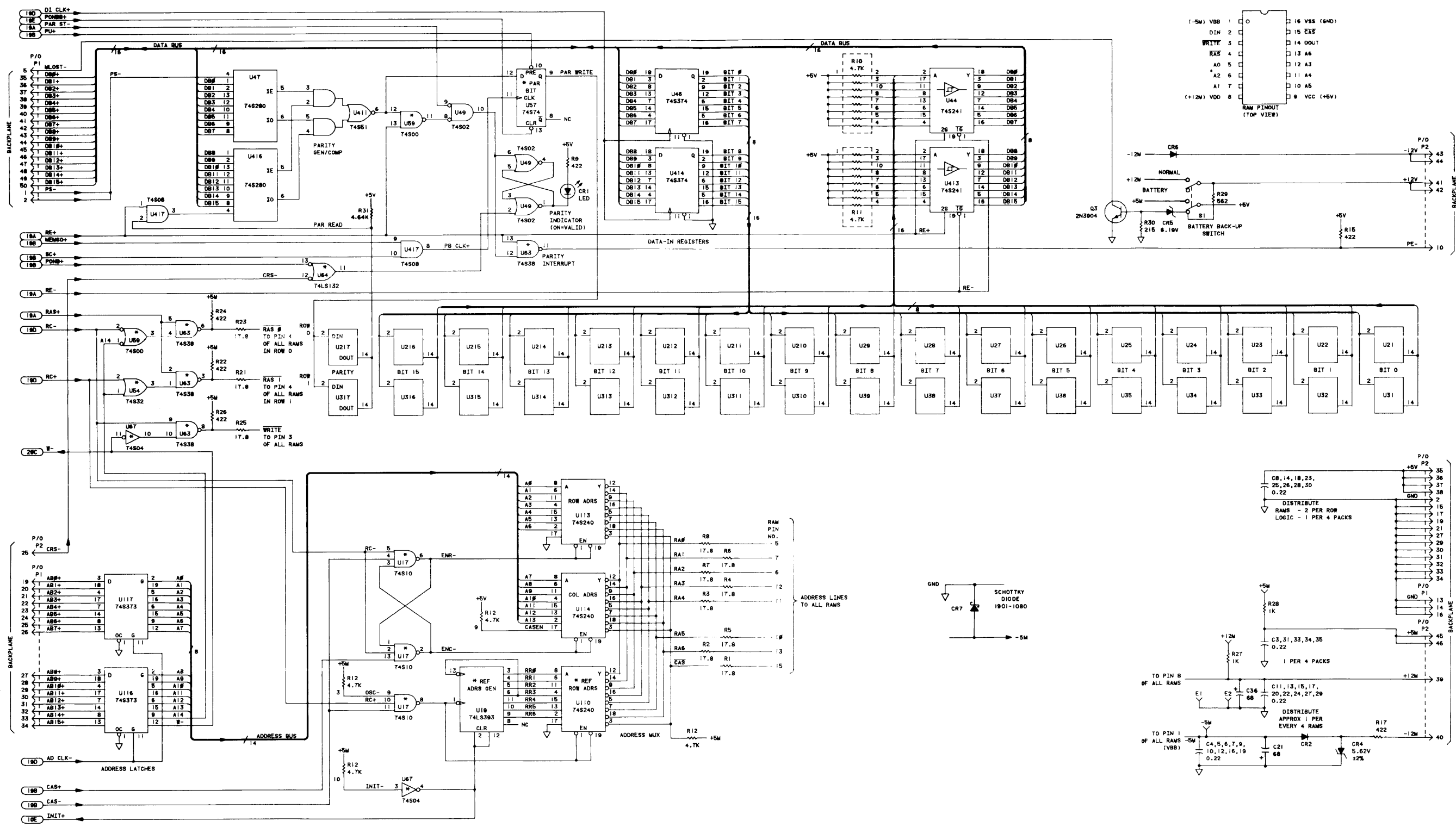
| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------|
| S1 | 3101-0642 | 5 | 1 | SWITCH=SLIDE, DPDT | 28480 | 3101-0642 |
| U16 | 1A20-1991 | 1 | 1 | IC CNTR TTL LS DECD DUAL 4-BIT | 01295 | 8N74LS390N |
| U17 | 1A20-0685 | 8 | 1 | IC GATE TTL 3 NAND TPL 3-INP | 01295 | 8N74810N |
| U19 | 1A20-1989 | 7 | 1 | IC CNTR TTL LS BIN DUAL 4-BIT | 07263 | 74LS393PC |
| U21 | 1A1A-0341 | 8 | 34 | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U22 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U23 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U24 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U25 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U26 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U27 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U28 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U29 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U31 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U32 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U33 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U34 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U35 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U36 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U37 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U38 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U39 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U43 | 1A20-0629 | 0 | 5 | IC FF TTL 3 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U44 | 1A20-1624 | 7 | 2 | IC RFR TTL 3 OCTL 1-INP | 01295 | 8N748241N |
| U46 | 1A20-1677 | 0 | 2 | IC FF TTL 3 D-TYPE OCTL | 01295 | 8N748374N |
| U47 | 1A20-1638 | 3 | 2 | IC GEN TTL 3 PAR GEN 9-BIT | 01295 | 8N748280N |
| U49 | 1A20-1322 | 2 | 2 | IC GATE TTL 3 NOR QUAD 2-INP | 01295 | 8N74802N |
| U52 | 1A20-1322 | 2 | | IC GATE TTL 3 NOR QUAD 2-INP | 01295 | 8N74802N |
| U53 | 1A20-0629 | 0 | | IC FF TTL 3 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U54 | 1A20-1449 | 4 | 2 | IC GATE TTL 3 OR QUAD 2-INP | 01295 | 8N74832N |
| U57 | 1A20-0693 | 8 | 1 | IC FF TTL 3 D-TYPE POS-EDGE-TRIG | 01295 | 8N74874N |
| U59 | 1A20-06A1 | 4 | 1 | IC GATE TTL 3 NAND QUAD 2-INP | 01295 | 8N74800N |
| U63 | 1A20-1451 | 8 | 1 | IC GATE TTL 3 NAND QUAD 2-INP | 01295 | 8N74838N |
| U64 | 1A20-1425 | 6 | 1 | IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP | 01295 | 8N74LS132N |
| U66 | 1A20-1076 | 3 | 1 | IC FF TTL 3 D-TYPE POS-EDGE-TRIG CLEAR | 01295 | 8N748174N |
| U67 | 1A20-06A3 | 6 | 2 | IC INV TTL 3 HEX 1-INP | 01295 | 8N74804N |
| U69 | 1A20-0691 | 6 | 1 | IC GATE TTL 3 AND-OR-INV | 01295 | 8N74864N |
| U110 | 1A20-1917 | 1 | 1 | IC RFR TTL LS LINE DRVR OCTL | 01295 | 8N74LS240N |
| U113 | 1A20-1633 | 8 | 3 | IC RFR TTL 3 INV OCTL 1-INP | 01295 | 8N748240N |
| U114 | 1A20-1633 | 8 | | IC RFR TTL 3 INV OCTL 1-INP | 01295 | 8N748240N |
| U116 | 1A20-2184 | 6 | 2 | IC LCM TTL 3 OCTL | 50364 | 748373N |
| U117 | 1A20-21A4 | 6 | | IC LCM TTL 3 OCTL | 50364 | 748373N |
| U210 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U211 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U212 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U213 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U214 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U215 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U216 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U217 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U310 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U311 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U312 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U313 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U314 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U315 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U316 | 1A1B-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U317 | 1A1A-0341 | 8 | | IC NMOS 16384-BIT RAM DYN 200-NS 3=8 | 0003J | UPD4160-2 |
| U410 | 1A20-1449 | 4 | | IC GATE TTL 3 OR QUAD 2-INP | 01295 | 8N74832N |
| U411 | 1A20-115A | 2 | 1 | IC GATE TTL 3 AND-OR-INV DUAL 2-INP | 01295 | 8N74851N |
| U413 | 1A20-1624 | 7 | | IC RFR TTL 3 OCTL 1-INP | 01295 | 8N748241N |
| U414 | 1A20-1677 | 0 | | IC FF TTL 3 D-TYPE OCTL | 01295 | 8N748374N |
| U416 | 1A20-1638 | 3 | | IC GEN TTL 3 PAR GEN 9-BIT | 01295 | 8N748280N |
| U417 | 1A20-1367 | 5 | 1 | IC GATE TTL 3 AND QUAD 2-INP | 01295 | 8N74808N |
| U510 | 1A20-1201 | 6 | 1 | IC GATE TTL LS AND QUAD 2-INP | 01295 | 8N74LS08N |
| U511 | 1A20-1450 | 7 | 1 | IC RFR TTL 3 NAND QUAD 2-INP | 01295 | 8N74837N |
| U516 | 1A20-1633 | | | IC BFR TTL 3 INV OCTL 1-INP | 01295 | 8N748240N |
| U610 | 1A20-0629 | | | IC FF TTL 3 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U611 | 1A20-0629 | | | IC FF TTL 3 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U613 | 1A20-0629 | | | IC FF TTL 3 J-K NEG-EDGE-TRIG | 01295 | 8N748112N |
| U614 | 1A20-06A3 | | | IC INV TTL 3 HEX 1-INP | 01295 | 8N74804N |



- NOTES:
1. RESISTORS ARE IN OHMS
 2. CAPACITORS ARE IN MICROFARADS
 3. BOARD FORMAT - CORPORATE HALF MODULE - SIX - LAYER BOARD:
 LAYER 1 - COMPONENT SIDE LAYER 2 - SIGNAL LAYER
 LAYER 3 - SIGNAL LAYER LAYER 4 - GROUND
 LAYER 5 - VOLTAGE (+5M, +5V, +12M) LAYER 6 - CIRCUIT SIDE
 4. * DESIGNATES IC'S POWERED BY +5M

| | | | |
|-----------------------|--------|------------------|-------------|
| MEMORY CARD 12004A | | HEWLETT-PACKARD | |
| TITLE | 12004A | PART NUMBER | 12004-60001 |
| NEXT ASSEMBLY | 12004A | FINISH | SCALE |
| | | D-12004-60001-51 | |

| REV | REVISIONS | APPROVED | DATE |
|-----|-----------|----------|------|
| A | AS ISSUED | | |



| | | | |
|-----------------------|--------|-----------------|------------------|
| MEMORY CARD 12004A | | HEWLETT PACKARD | |
| TITLE | 12004A | PART NUMBER | 12004-60001 |
| FINISH | | SCALE | D-12004-60001-52 |

4.1 INTRODUCTION

The Hewlett-Packard HP 12035A Power Supply provides the necessary regulated voltages and power control logic signals for the HP 1000 L-Series Computer System.

4.2 PHYSICAL CHARACTERISTICS

The HP 12035A Power Supply consists of three assemblies, as follows:

| | | |
|------|------------------|-------------------|
| A1 | D-12035-60002-51 | 250W Mother Board |
| A1A1 | D-12035-60003-51 | Driver Board |
| A1A2 | D-12035-60004-51 | Logic Board |

In addition to the assemblies listed above, the L-Series Computer System includes a battery back-up card. This assembly is covered in Section V of this document.

The power supply slides into the front of a 5-1/4 inch high rack as shown in figure 4-1. A male connector on the rear of the power supply mates with female connectors on the computer backplane. A front power panel contains a power cord receptacle (J1), a fuse post (F1), line selector switch (S2), a 25kHz output jack, an external fan power jack (J3), and the power control logic connector (J4).

4.2.1 INPUT POWER CONNECTOR

The input power connector (J1) is a standard 3-pin power cord receptacle. The connector is UL/CSA listed and is rated at 15 amperes.

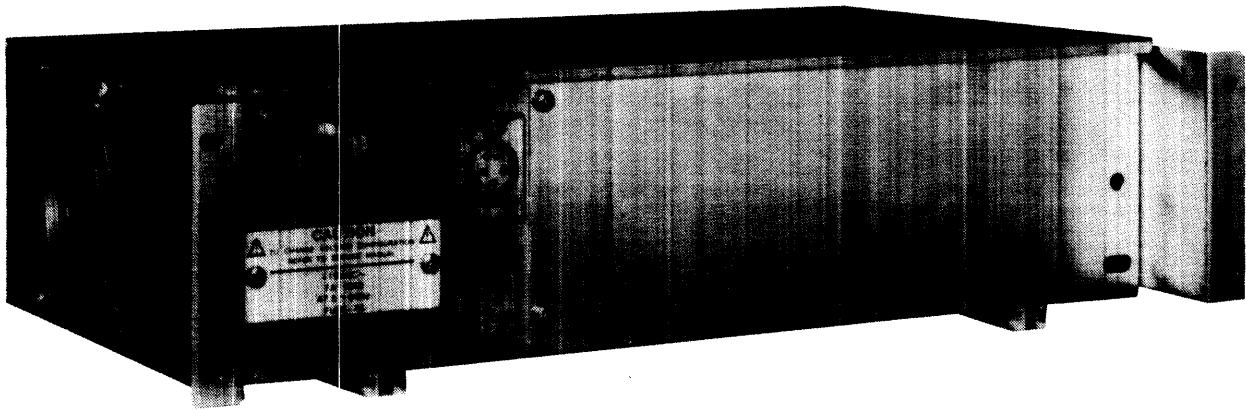


Figure 4-1. HP 12035A Power Supply

4.2.2 BACKPLANE INTERFACE OUTPUT CONNECTOR

The backplane interface connector is a dual male connector designed to mate with one 20-pin female connector one 4-pin female connector.

Pin assignments for the backplane interface connector are as follows:

| PIN | SIGNAL NAME | |
|-----|---------------------------------|---|
| 1 | -12V MEMORY VOLTAGE SENSE | |
| 2 | +12V MEMORY VOLTAGE SENSE | |
| 3 | +12V LOGIC (4A MAX) | |
| 4 | -12V LOGIC (2A MAX) | |
| 5 | +5V MEMORY VOLTAGE SENSE | |
| 6 | NOT USED | |
| 7 | NOT USED | |
| 8 | POWER ON (PON) SIGNAL | |
| 9 | POWER FAIL WARNING (PFW) SIGNAL | |
| 10 | } | |
| 11 | | |
| 12 | | +5V LOGIC (30A) |
| 13 | | |
| 14 | | |
| 15 | } | |
| 16 | | |
| 17 | | |
| 18 | | |
| 19 | | DC COMMON, 25kHz COMMON, AND CHASSIS GROUND |
| 20 | | |
| 21 | | |
| 22 | | |
| 23 | 25kHz PHASE 2, 14VRMS (TO GND) | |
| 24 | 25kHz PHASE 1, 14VRMS (TO GND) | |

4.2.3 SINGLE-PHASE 25KHZ OUTPUT CONNECTOR

The front-panel mounted, single-phase 25kHz output connector (J13) is a 3-pin connector (part number 1251-2164) rated at 15 amperes. For best regulation, shielded 14 gauge, twisted pair wire is recommended.

4.2.4 POWER CONTROL CONNECTOR

The power control connector (J4) is used for the external logic signals Line Power Up (LPU), Power Supply Up (PSU), and the SYNC signal used when power supplies are connected in parallel for both CPU's and peripherals. The pin assignments are as follows:

| PIN | SIGNAL NAME |
|-----|------------------------------|
| 1 | N/C |
| 2 | N/C |
| 3 | 100kHz SYNCHRONIZATION INPUT |
| 4 | LOGIC GROUND |
| 5 | LINE POWER UP (LPU) |
| 6 | N/C |
| 7 | POWER SUPPLY UP (PSU) |
| 8 | SHIELD GROUND |
| 9 | N/C |

4.2.5 EXTERNAL FAN CONNECTOR

The external fan connector (J3) provides 115V -25%/+10%, 15 watts maximum, for an external fan. Phasing is unnecessary.

4.2.6 INDICATORS

Three LED indicators are located at the lower right hand corner of the front of the power supply and can be observed through an oval aperture. These indicators indicate the status of the power supply under normal and malfunctioning conditions, as shown on the next page.

NOTE

A lit indicator is shown as an asterisk, an unlit indicator is shown as a zero.

| LINE (GREEN) | FAULT (RED) | OPER. (GREEN) | |
|-----------------|----------------|------------------|--|
| 0 | 0 | 0 | No line voltage. Check for blown fuse, no line cord, poor line cord connection, or dead line voltage circuit. |
| * | 0 | 0 | AC line voltage but no DC voltage at the output of the supply. Check to see if the Test-Operate switch is in the OPER position. If OK, replace the drive board or the logic board. |
| * | * | 0 | Line voltage present but a fault has occurred such as an over voltage or over current condition. Check the line voltage versus the line voltage range selected. Also check for shorted outputs. The AC switch must be cycled (turned OFF then back ON) to restore normal operation after the fault is corrected. |
| * | 0 | * | Normal operation. All six DC voltages and maximum load currents are within specified limits. |

4.3 SPECIFICATIONS

Specifications for the HP 12035A Power Supply are listed in table 4-1.

Table 4-1. Specifications

| |
|--|
| <p>INPUT VOLTAGE: 2 ranges, selectable at power supply front panel.</p> <p>115V Selector Position: 86 to 127 VRMS, 47 to 66 Hz</p> <p>230V Selector Position: 195 to 253 VRMS, 47 to 66 Hz</p> |
| <p>POWER FACTOR:</p> <p>0.65, full load</p> |
| <p>SURGE CURRENT:</p> <p>Less than 15 amperes from cold start. Less than 20 amperes after one minute down time, then restart.</p> |
| <p>INPUT CURRENT, FUSING:</p> <p>3AG normal blow; 7.0 amperes for 115V range, 3.0 amperes for 230V range.</p> |
| <p>POWER INPUT, NO LOAD:</p> <p>Less than 40 watts (includes internal fan).</p> |
| <p>EXTERNAL FAN POWER:</p> <p>Up to 15 watts @ 86 to 127 VRMS.</p> |

Table 4-1. Specifications (Continued)

TRANSIENT SUSCEPTIBILITY:

Positive or negative spikes on the differential or common mode of up to 1KV with 30 nsec rise and 375 nsec duration, at a repetition rate of once per hour, will not cause damage nor interruption to operation.

Longer transients of up to 500V with rise time of 250 nsec and duration of up to 50 usec at repetition rates not to exceed 10 per year will not cause damage. Hard shutdown may occur; this can be reset by cycling the power switch.

CONDUCTED RFI BACK ON LINE INPUT:

Below Level A VDE conducted and radiated RFI specifications.

POWER INTERRUPTIONS:

Line voltage detector monitors the peak-to-peak value of line voltage. At nominal line voltage on either range, the Power Fail Warning (PFW low) will be generated if the line voltage drops to zero for 20 msec or greater (approximately one cycle).

At other line voltages, the minimum dropout times to PFW are as follows:

86VAC: greater than 5 msec

195VAC: greater than 10 msec

230VAC: greater than 25 msec

LINE VOLTAGE SAG:

An instantaneous drop in line voltage within the allowable range may cause PFW to go low, but Power On (PON) will not be pulled low. Such a sag must exceed -30% drop to generate PFW. Steady state sags below minimum range will generate PFW continuously low, although a critical boundary condition can cause PFW to cycle at a 3 msec low minimum and a maximum repetition rate of 120 pps. Under these conditions, PON will remain high.

Table 4-1. Specifications (Continued)

LINE VOLTAGE SURGE:

Surge voltages of up to 1.5 times the 115V or 230V range for 0.5 cycle every 5 seconds will not disturb normal operation, and will not generate power fail warning signals.

LINE OVER-VOLTAGE:

Application of line voltage of 2 times nominal for more than one second will blow the input fuse. The power supply can withstand this malfunction for up to 100 times during its life before component failure, if not repeated at less than one hour intervals. This feature is primarily to protect against inadvertent application of a 220/230V line while configured to 115V range.

OUTPUT VOLTAGES, CURRENTS, TOLERANCES, AND PARD:

(PARD = Periodic And Random Deviation, 10Hz to 500kHz, measured with differential probes (HP 1806A/180, or equivalent) at output connector.)

DC OUTPUT VOLTAGES, TOLERANCES, AND PARD:

+5V +/-2% PARD 50mV nominal; 300mV maximum

+12V +/-6% PARD 100mV maximum

-12V +/-6% PARD 100mV maximum

AC OUTPUTS: 25kHz SINE-WAVE POWER:

1. SPLIT PHASE, 3 pins on rear connector, 19.5VRMS +/-8% each phase with conditional output up to 5ARMS maximum.
2. SINGLE PHASE, 2 pins on front connector, 27VRMS +/-8% conditionally up to 12ARMS maximum (one line is chassis ground).

NOTE: Refer to appendix B for application information.

Table 4-1. Specifications (Continued)

| |
|--|
| <p>MAXIMUM POWER/CURRENT OUTPUT RATINGS:</p> <p>HP 2103L: +5V @ 25 ADC +12V @ 4 ADC -12V @ 2 ADC 25kHz (either port or sum of both) 70 watts</p> <p>HP 1000 L-Series System: +5V @ 30 ADC +12V @ 3 ADC -12V @ 1.5 ADC 25kHz (either port or sum of both) 140 watts</p> |
| <p>INLET TEMPERATURE:</p> <p>HP 2103L: 0 to 55 degrees Centigrade to 15,000 feet (4572 metres)</p> <p>HP 1000 L-Series System: 0 to 55 degrees Centigrade to 10,000 feet (3048 metres), with linear derating to 45 degrees Centigrade at 15,000 feet (4572 metres).</p> |
| <p>MINIMUM INLET AIR FLOW RATE:</p> <p>Minimum flow rate of 20 CFM @ 200 feet/minute velocity (43 BTU/hour)</p> |
| <p>SYNCHRONIZATION INPUT:</p> <p>1 to 12V peak-to-peak, 100nsec minimum pulse width at 100kHz +/-1% synchronizes internal switching frequency to external clock.</p> |
| <p>POWER CONTROL LOGIC SIGNALS (INPUTS):</p> <p>LPU (Line Power Up), High True. Can be connected in parallel with other supplies in system (+5V logic level).</p> <p>PSU (POWER SUPPLY UP), High True. Can be connected in parallel with other supplies in system (+5V logic level).</p> |

Table 4-1. Specifications (Continued)

LOGIC SIGNALS FOR CPU USE (OUTPUTS):

PFW (Power Fail Warning), Low True; warns CPU of failing power. All voltages are held within specified tolerance for 5 msec after this signal goes low. 100mA sink capability, open collector TTL. Rise and fall times less than 50 nsec.

PON (POWER ON), High True; goes high after all DC voltages are up and within regulation. Stays high for 5 msec after PFW goes low at which time all output voltages must be within their tolerances. 100mA sink capability, open collector TTL. Rise and fall times less than 50 nsec.

SHORT CIRCUIT PROTECTION:

All DC and AC power outputs are fault protected for short circuits. Supply will shut down, lighting the FAULT light, if the output is shorted. To reset, the AC power switch must be cycled (turned OFF for 5 seconds, then ON). If the output short persists upon re-turn on, the FAULT light will come back on.

OUTPUT UNDER-VOLTAGE AND OVER-VOLTAGE PROTECTION:

+5V output is sensed for over voltage. If +5V exceeds 6.5V, supply will shut down. (This can occur if the Vout potentiometer setting is too high.) To reset, the AC power switch must be turned OFF, then ON.

4.4 BINARY SIGNAL LEVELS

Most of the logic used in the power supply is implemented with standard CMOS or Schottky TTL devices. Schottky TTL high logic levels are approximately +2.5 to +4.5 Vdc; low logic levels are approximately 0.0 to +0.8 Vdc. CMOS levels are less than 1 Vdc (logic low) or greater than 11 Vdc (logic high). The actual values measured will vary due to the type of device, the load, and the condition of the device. When using positive logic, a high is "true" and a low is "false".

4.5 THEORY OF OPERATION

The HP 12035A power supply provides three DC output voltages for DC power to the backplane, and two sine-wave high frequency (25kHz) power output ports to power the system peripherals. The power supply operates from 50 to 60 Hz primary power over a wide range of input voltages (see table 4-1) selected by a two-position selector switch on the front panel.

A functional block diagram of the power supply is shown in figure 4-2. Also see the schematic diagram, drawings 12035-60002, 12035-60003, and 12035-60004, located at the rear of this section.

The basic operation is described in the following paragraphs (refer to the mother board schematic diagram, 12035-60002).

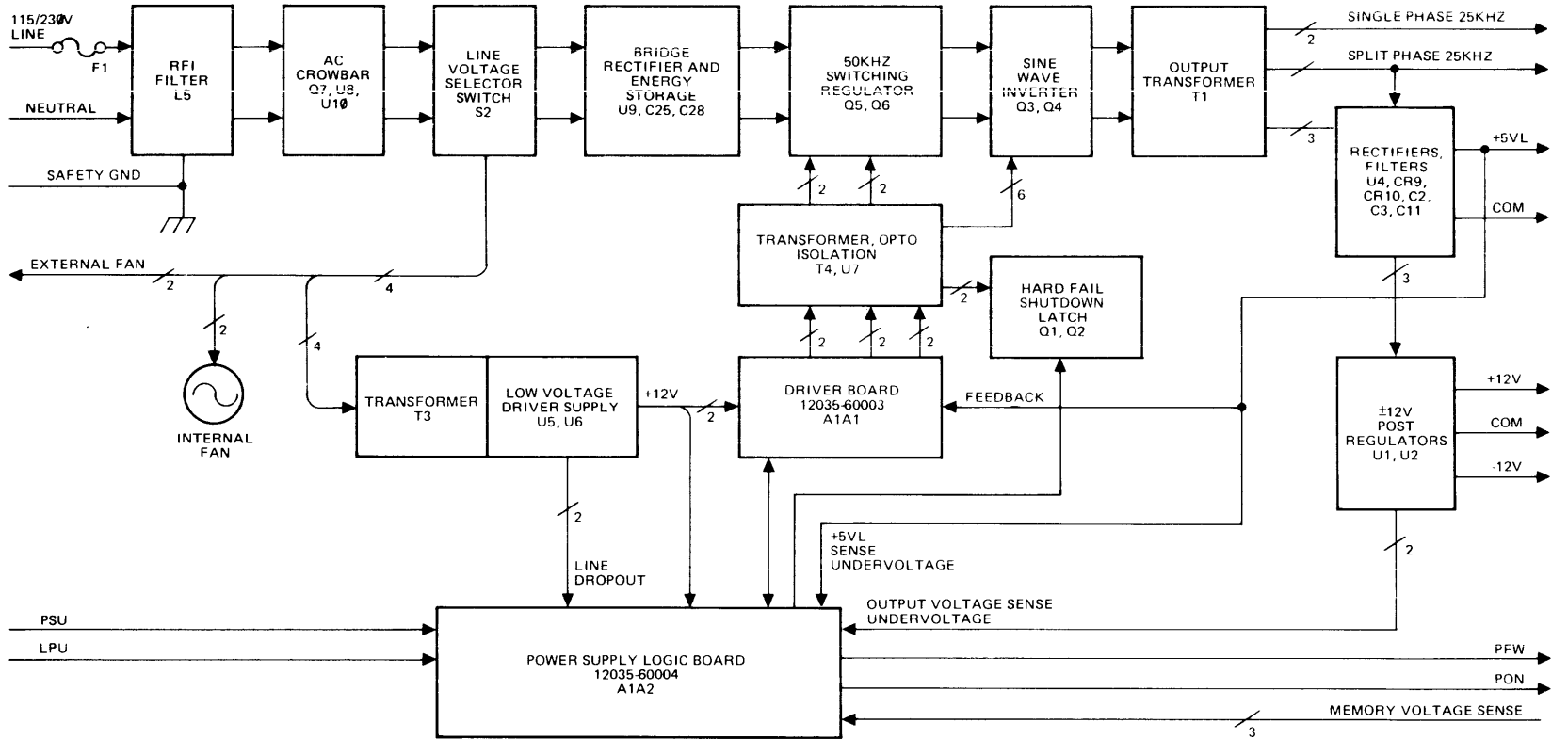
4.5.1 MOTHERBOARD (PART NUMBER 12035-60002)

The schematic diagram for the motherboard is shown in drawing 12035-60002. A photograph of the motherboard is shown in figure 4-3. The motherboard contains a low voltage driver supply, RFI filter, input AC crowbar, bridge rectifier, 50kHz switching regulator, sine-wave inverter, and an output rectification section consisting of rectifiers, filters, and post regulators.

4.5.1.1 Low Voltage Driver Supply

The low voltage driver supply powers the drivers and regulation loop so that this circuitry can be referenced to system ground (i.e., isolated from the line and neutral). The dual primary step-down transformer, T3, also functions as a 2-to-1 step-down auto transformer for operating 115V fans when operating on 195 to 253 VRMS line potentials. It is designed to power the internal 115V fan and one external fan of equal power (+/-5 watts) for cooling the card cage.

Figure 4-2. HP 12035 Power Supply Functional Block Diagram



7700-561

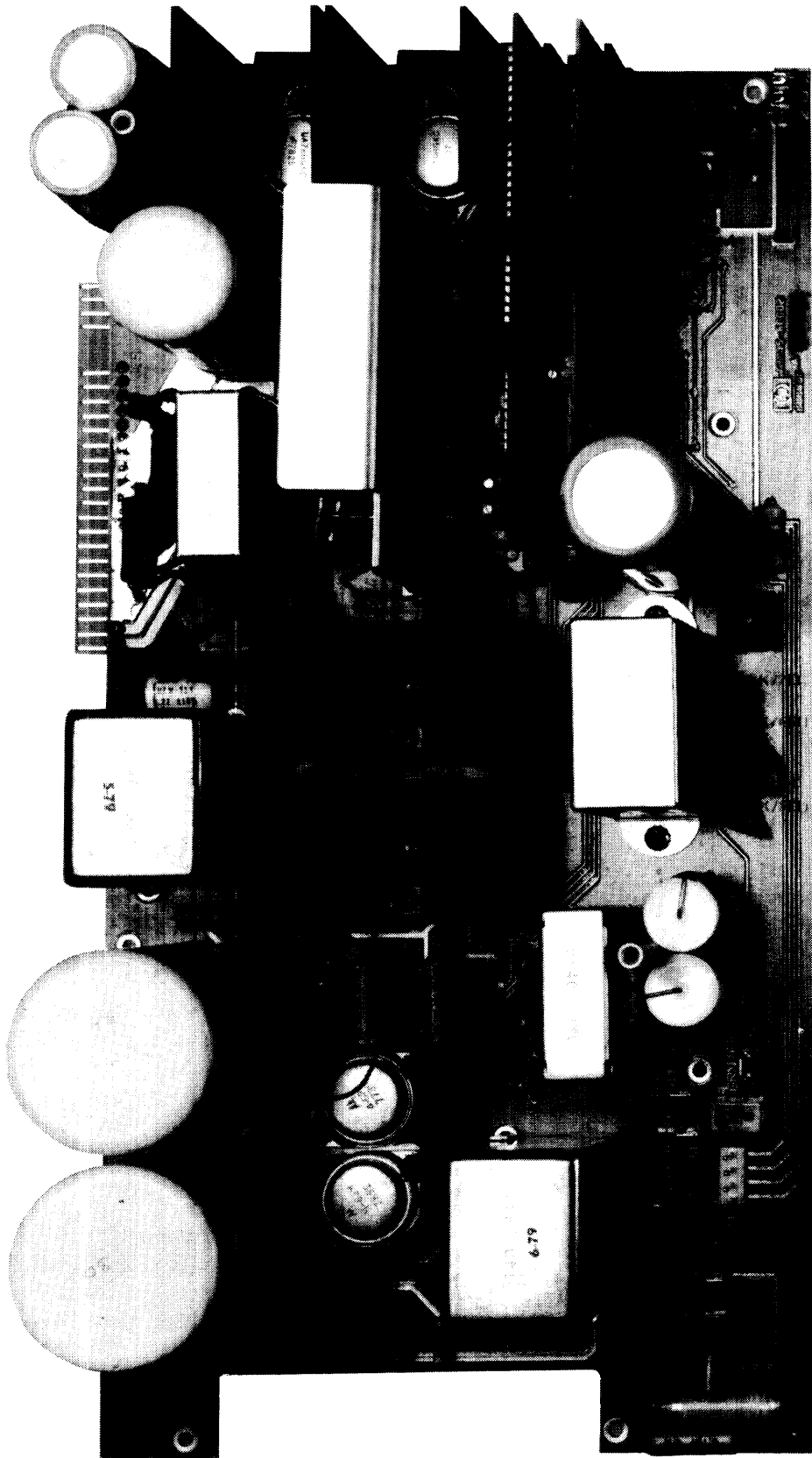


Figure 4-3. Motherboard (12035-60002)

The design is a conventional capacitive input bridge supply with one exception: A sensor is required for the computer to recognize power cycle dropouts and low line conditions. An additional single rectifier diode, CR5, combined with a capacitor, C14, and circuitry on the logic card provide this detection. The differential voltage is sensed across C14 with a discharge time constant of 55 msec with the discharge path on the logic card. As long as 50/60 Hz is present, the full-wave rectifier will charge the capacitive input filter, C17, with 100/120 Hz pulses of current through CR5 in parallel with C14. If a cycle should drop out, C14 will be discharged. Reverse polarity across C14 will turn on a differential comparator on the logic board, thus providing a warning signal, Soft Fail Shutdown (SFS), to the CPU.

The output of the capacitive input filter is 17 to 35 VDC over the line variations, which feeds a +12V three-terminal regulator U5. The current consumption of the driver and logic board from this supply is approximately 250 mA.

4.5.1.2 Input Crowbar, RFI Filter and Line Rectifier

The principle of a line switching power supply uses direct rectification of the line voltage without an input transformer to reduce size and weight of the supply. To utilize the two line ranges of nominally 115V and 230V RMS, a bridge rectifier is switched from a full-wave bridge to a full-wave doubler into a pair of electrolytic input filter capacitors (C25, C28). Switch S2 provides this switching function as well as the switching of the primaries of T3 from series to parallel for the two ranges. This results in nominally 300 VDC across the two large energy storage electrolytic capacitors C25 and C28 in series. The switching regulator uses this voltage as the input to transform down to +150 by pulse-width modulation at 50 kHz. This 50 kHz load current flows through C25 and C28. Because their 50 kHz impedance consists mostly of the equivalent series resistance at that frequency (which is not particularly low), some 50 kHz voltage (ripple) appears across these storage capacitors. To keep this high frequency ripple from conducting back into the mains, a differential RFI filter is incorporated. This consists of a dual choke, L5, and a capacitor, C29, across the input. Two capacitors (C30, C31) from line and neutral to case ground also are used to attenuate the common mode capacitively-coupled high frequency.

An AC crowbar consisting of a triac (Q7) and a pulse-rated (watt-second) resistor (R31) in series is connected across the line to neutral. The triac is triggered by an opto-coupled SCR (U8) through bridge rectifier U10, to provide full-wave triggering of the triac, thus providing 1/2 cycle response (8.33 to 10 ms for 60/50 Hz, respectively) time.

The purpose of the AC crowbar is to blow the input fuse (normal blow 3AG) upon sensing an over-voltage condition across the two storage capacitors or into the sine-wave inverter. (See paragraphs 4.5.1.3 and 4.5.1.4). The worst case fuse is the 7 ampere fuse used on the 115V line which must hold for low line of 86 VRMS and full power output (approximately 7.0 amperes RMS). This 7 ampere

3AG normal blow fuse will blow in approximately 70 msec at a nominal voltage of 230 VRMS. The peak blowing current is 46 amperes with the triac actuated. With the normal drops via the input line impedance, the voltage is dropped significantly to stop charging the storage capacitors to a voltage that would exceed their surge voltage rating, thus protecting against capacitor failures. The over voltage is sensed by two 200V zener diodes (CR16, CR18) which limit the voltage to an absolute maximum of 420V. The 200V zener diodes the SCR opto diode (U8) to allow isolation and power gain so that small diodes can be used. This circuit thus protects against inadvertent application of 230 VRMS at the input to the supply while on the 115V selected range.

Another mode of over voltage is encountered if the switching regulator transistors (Q5, Q6) fail to turn off (shorted emitter to collector). This causes the inverter input voltage to increase by a factor of about 2, which would cause the +5 volt logic voltage to increase to approximately 10 volts, causing severe damage to the logic loads. Another zener diode of 200V (CR17) is used back to the opto SCR from the output of the switching regulator. Because this failure could happen under normal operation due to a defective transistor, a transient over voltage of the +5V logic could be possible, even though the fuse will be blown. For this reason, pulse-rated ("Transorb") zener diodes are used on all cards with the +5V logic voltage.

4.5.1.3 Switching Regulator

The switching regulator consists of the high voltage power switching transistors Q5 and Q6, diode CR13, inductor L4 and two series 5uf output capacitors C24 and C27. The driver transformer (T4) is a dual unit which isolates the drive circuitry on the driver board from the line-operated power switches, and provides the base currents with variable on and off times. Diodes CR14 and CR15 are used across the base-to-emitter junctions of the power transistor switches (Q5, Q6) to provide a bi-directional termination for the driver transformer(s) to sink the turn off current (IB2) after the stored charge has been removed from Q5 and Q6. The primary of the driver transformer is driven by a tri-level waveform which consists of a turn-on base current of 250mA minimum for a period of time between zero and ten microseconds, determined by the feedback control voltage. At the end of the "on" period the drive current reverses (in less than 100 nsec) to an equal current for a nearly equal amount of time in the reverse polarity direction. This allows -250mA minimum to flow from the switching transistor base to remove the minority carriers stored, and turn the transistor off quickly. This takes between 1.0 to 2.5 microseconds to accomplish, depending on transistor characteristics and the particular loading conditions of the supply. The turn-off time is made slightly longer than the turn on time in the driving tri-level waveform to assure proper turn off.

The areas of the turn-on and turn-off waveforms are approximately the same and of opposite polarity, such that when passed through the driver transformer they do not cause appreciable residual flux, which would lower the transformer's permeability. The net result of using this tri-level waveform is to allow suitable drive to the switching transistors while maintaining low transient losses, and also allowing small driver transformers to be used. Small transformers help to reduce common mode EMI coupling by maintaining a low primary-to-secondary capacitance.

At full control voltage, the drive waveform to each switching transistor is a square wave with equal on and off times. This allows each switching transistor to provide a 0 to 50 percent duty cycle to control the input-voltage-to-output-voltage ratio of infinite step down up to 2-to-1 step down. To allow up to 1-to-1 transformation, however, the switching transistors are in parallel and are driven 180 degrees out of phase, such that when one unit is fully off, the other is fully on, and vice versa. This causes the switching rate to increase to 50kHz, yet each device is only operating at 25kHz. The parallel combination and the 180 degrees drive relationship then provide a switching regulator capable of a 0 to 100 percent duty cycle (or 1:0 to 1:1 transformation of V_{in}/V_{out}). This allows regulation over a very large variation in input line voltage.

The ratio for the 115V range is 86V to 127V or 1.48 to 1, and for the 230V range 195 to 253V or 1.30 to 1. Zero to full load variations add to this ratio requirement of the switching regulator to make it necessary to regulate over a 2 to 1 range of input voltage to output voltage.

The energy storage elements for the switching regulator are the inductor L4, and the two series-connector capacitors C24 and C27. The input of L4 is switched to +300V during the on-time and released during the off-time. When released, L4 tries to hold the current constant by producing counter EMF (reversing the polarity of voltage across L4), and causing CR13 to conduct. CR13, called a "catch diode", is a fast-recovery rectifier which conducts the inductor current during the off time. The load is taken off the output capacitors C24 and C27. Bleeder resistors across each of these capacitors minimize capacitive and load imbalances to provide a centertapped voltage supply for the half-bridge inverter that follows. The voltage across this center-tapped capacitor output will be about 150 to 170 VDC depending on load conditions and will have a few volts of 50kHz ripple under full load. The capacitors are of polypropylene dielectric construction to provide the low losses required for this application. Ripple currents of up to 4 amperes peak flow through these capacitors at 25kHz (full sine wave, 60 percent duty cycle).

For prevention of over current of the switching transistors while in the on-state, and of the SCR's in the sine-wave inverter (see paragraph 4.5.1.4) a parallel combination of two current sensing resistors, R20 and R21, is provided in the common leg, sensing the inductor current during the turn-on portion of the duty cycle. If this peak current flowing through the parallel sense resistors exceeds the forward voltage required to turn on the LED of the opto-isolator U7, the opto transistor is driven, which removes the drive to

the T4 primaries, and lights the FAULT LED (red). This condition is latched by Q1 and Q2, which requires the +12 volt low voltage bias supply to be turned off to release the latch (AC input switch recycling).

4.5.1.4 Sine-Wave Inverter

The sine-wave inverter consists of Q3 and Q4, which are high-frequency switching integrated thyristor rectifiers (ITR's, which are SCR's with integral reverse rectifiers across them) dual resonator inductor L3; resonator capacitor C19; current limiting capacitor C18; the output transformer T1; and the driver trigger transformer T2. The ITR's are triggered with a 7.5 to 8.5 usec trigger pulse of greater than 50mA, typically 100mA at 25kHz repetition rate, synchronized with the 50kHz switching regulator driver.

The frequency of resonance is set at about 1.35 times for ITR self-commutation turn off and to prevent excess dissipation.

The inverter is triggered immediately upon AC line turn on with the +12V bias supply. The switching regulator drive is delayed and ramped up at a rate of approximately six volts per millisecond. At turn off the drive is ramped down to provide a down ramp of 30 volts per millisecond from the switching regulator. This degausses the output transformer, so that upon subsequent turn on the output transformer will not be driven into saturation. The turn on "ramp-up" reduces the output surge current required to charge the rectifier-filter sections for +5 and +/-12 volt outputs. In addition to the ramp-up, C18 provides current limiting on the sine-wave inverter. Capacitors C20 and C22, and R16 and R19 are networks across the ITR's which limit the rate of voltage rise so as not to exceed 750 volts per usec.

The rate of current rise is a sine function limited by the resonance of the L3 inductor and C19, the resonating capacitor. The "Q" of the dual inductor L3 is in excess of 5 at the operating frequency to maintain low losses and good waveform purity.

Gate trigger current can be measured by utilizing the T2 transformer secondary loops and a clip-on current oscilloscope probe. External synchronization using test point E5 on the driver board should be used to observe the phase relationship between the two SCR triggers.

CAUTION

When making these measurements make sure that exposed metal of the current probe does not touch the SCR heat sink or circuit components. This circuitry is NOT ISOLATED from the primary line voltage.

4.5.1.5 Output Rectifiers, Post Regulators

Two secondary windings on T1, the output transformer, provide the AC voltages required for +5V and +/-12V rectification. A third winding provides a 25kHz sine-wave output port at about 27 VRMS for external point of load rectification and regulation. This winding is available at a front panel connector (J13). The single-phase output is grounded on one side for safety reasons. A twisted, shielded pair of 18 to 14 gauge wire is recommended for the transmission cable to minimize voltage drops and losses in regulation.

The +5V logic voltage is capable of providing 30 amperes output (150 watts), and uses Schottky rectifiers (CR9, CR10) for the highest possible efficiency. A center-tapped, full-wave rectifier circuit is used to minimize drops and the number of rectifiers required.

The forward voltage drops of the Schottky rectifiers, which vary with the +5V load current, are compensated by the loop feedback to the regulator and compared with a voltage reference. The loop then increases the inverter AC output to compensate for forward drops in the Schottky rectifiers and other DC drops in the 5V, 30 amp DC output circuit. The AC output and the rectified DC output from the U4 bridge rectifier vary as a function of +5VDC loading. For this reason and to reduce +/-12 volt load regulation and ripple variations, post regulators are used to regulate the +12 and -12 volt outputs. U1 and U2, two terminal fixed voltage regulators, regulate the +12 volt and -12 volt logic outputs, respectively.

The input voltage to the +12 and -12 volt regulators is rectified with a bridge rectifier used as two center-tapped rectifiers of opposite polarity. The winding feeding the bridge has its center tap terminated to the horizontal mounting frame of T1, which is +5V common ground. The positive and negative outputs of the bridge feed choke input filters to maintain 180 degrees conduction of the rectifiers and maintain a sine-wave with low harmonic content. Output surge current limiting at turn on is controlled by the current limiting capacitor C18 on the output of the inverter, and the ramp-up rate controlled by the driver board circuitry.

4.5.2 DRIVER BOARD (PART NO. 12035-60003)

The schematic diagram for the driver board is shown in drawing 12035-60003. A photograph of the driver board is shown in figure 4-4. The driver board contains a phase-lock type of oscillator (U14) operating at approximately 96kHz (adjustable by R5); a divide-by-4 counter stage (U24), a tri-level trigger generator and driver for the ITR's; a two-phase, tri-level waveform generator, duty cycle control and drivers for the switching regulator; and a

voltage regulator loop with low time constant reference and adjustment (R6) for the +5V.

4.5.2.1 VCO and Phase-Locked Loop Synchronization

A CMOS 4046 voltage controlled oscillator (VCO) and phase locked loop integrated circuit (U14) is used to provide a temperature stable frequency oscillator (approximately 0.03 percent per degree Centigrade), which is adjustable from 93 to 130kHz with potentiometer R5. Normally, this is set to about 96 kHz and is divided by 4 by counter U24 and connected to square-wave buffer (U23). The output of the square wave buffer is available at test point E2, and normally reads 24kHz, one fourth of the VCO frequency. Synchronization is provided by the phase-locked loop phase detector input to U24. The pre-amplifier into the detector accepts inputs from 300mV to the Vdd supply (12V) as a lockable input source. The loop filter consists of R23, C12, R8 and C13. The lock-up range is about 2:1; far in excess of what is necessary. It is designed to synchronize on a crystal-derived clock in the 100kHz range, and yet free run at an adjusted frequency approximately 5 percent below the synchronized input frequency.

4.5.2.2 SCR Gate Drive

The SCR gate drive circuit is used for triggering the ITR's. The square wave from U14 is divided by a divide-by-four (U24). The Q outputs from U24 (see figure 4-5) are buffered by U23 and drive differentiator capacitors C4 and C5, and the 22K ohm resistors in U43. (The time (T) is 16.5 usec.) The differentiators are set to zero by CR1 and CR5 at the end of each cycle. Each differentiator feeds an input of two voltage comparators (U21A, U21B) which are referenced on the opposite inputs with approximately 7.1 VDC. The sharp-rising waveform from the differentiator turns on the comparator output for a period equal to about 0.5T, at which time the voltage on the differentiator output decays to the 7.1 volt level. This forms a pulse at each output for each transition of the 25kHz square wave, which are equal and opposite in phase. These pulses are fed to the complementary CMOS drivers (U31, U41) which drive each end of the SCR trigger transformer (T2, located on the mother board). This results in a tri-level waveform as shown in figure 4-5. Each SCR will trigger only with positive current pulses. Therefore, each SCR will trigger on alternate polarities of the tri-level waveform.

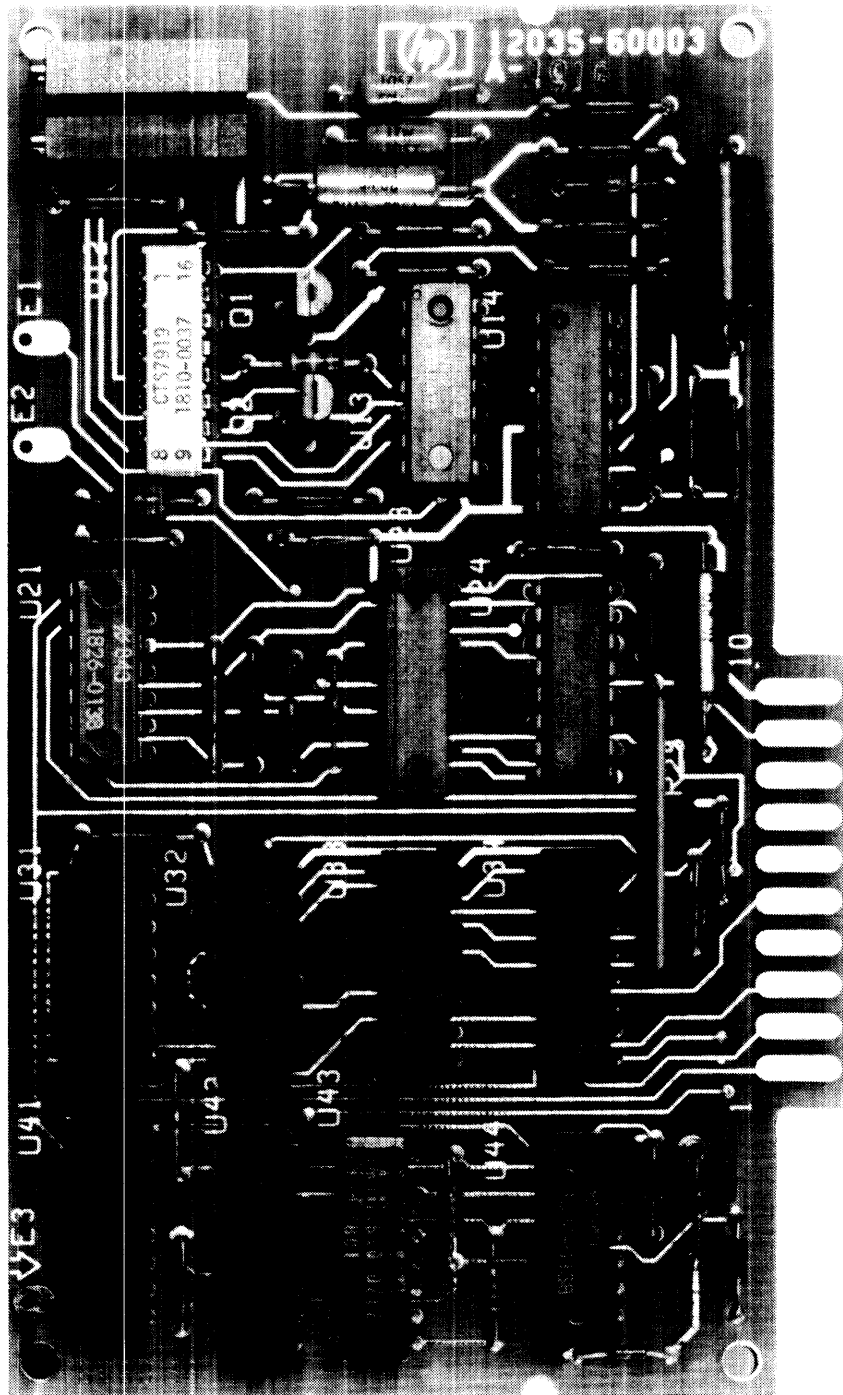


Figure 4-4. Driver Board (12035-60003)

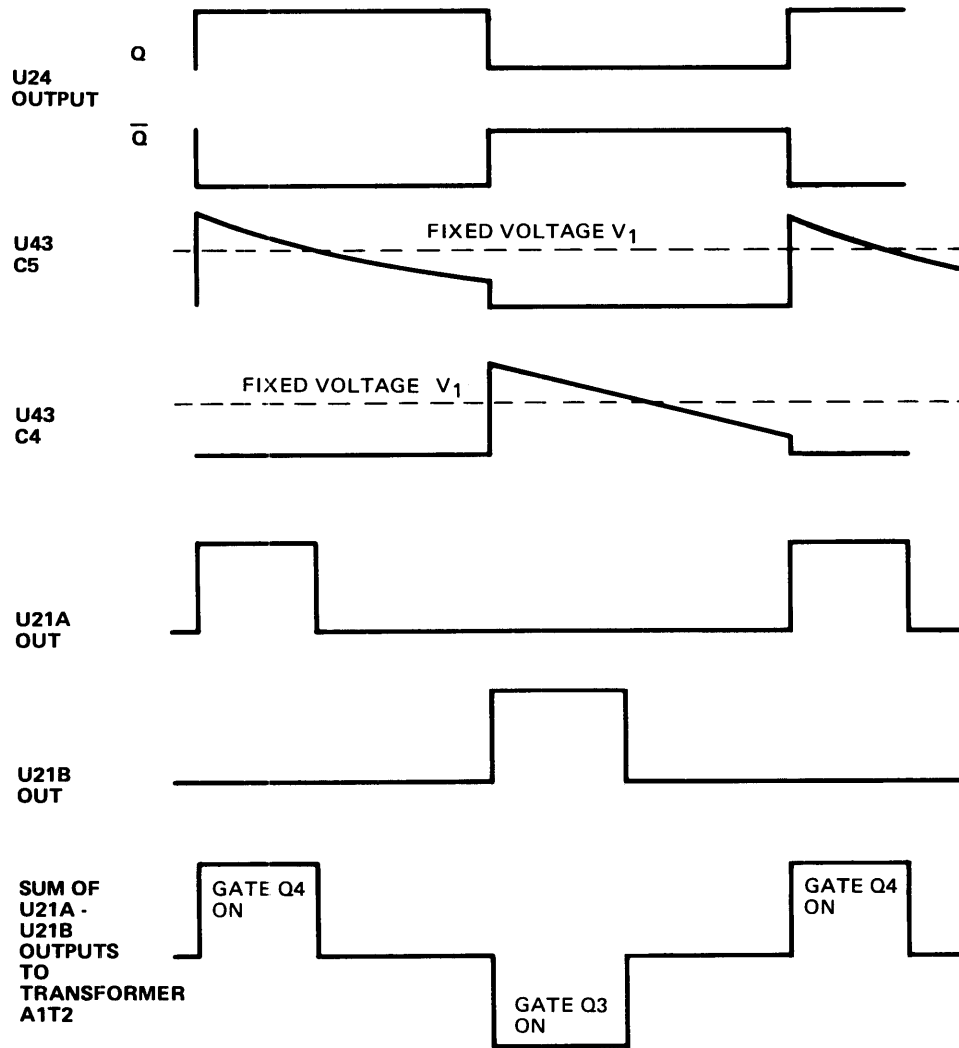


Figure 4-5. SCR Drive Waveforms

4.5.2.3 Switching Regulator Tri-Level Drive

The switching regulator transistors (Q5 and Q6 on the mother board) require a pulse-width controlled waveform that will provide a forward base current for a controlled period of time followed immediately with a reverse base current to turn the device off quickly by pulling out the minority carrier stored charge in the base region. In order to couple this drive to the bases of the switching transistors with small transformers, the time on must be approximately equal to the time off, or, in other words, the waveform must be symmetrically about zero volts to eliminate DC magnetizing current in the core and prevent core saturation.

To generate these waveforms both integrating and differentiating networks are used. In contrast to the SCR drive, the integrating networks provide the "on" time while the differentiating networks provide the "off" time. The same voltage reference is used on all comparators. Figure 4-6 shows the waveform generation.

In order to provide 0 to 100 percent duty cycle, each drive will provide 0 to 50 percent duty cycle phased 180 degrees out of phase at 25kHz with the other. Each switching transistor operates at 25kHz, yet the overall switching rate for the circuit is 50kHz. Storage time in the high-voltage switching transistors in this circuit is unimportant because the control will compensate for storage time and there is a complete one-half cycle to turn the device off in the worst case.

The value of L4 is 1.0 mHenrys at 3 amperes DC. This limits the peak current to less than 3 amperes for the "worst case" off time. Both of the switching transistors Q5 and Q6 must conduct this current as well as the "catch diode" CR13.

Polypropylene capacitors C21 and C27 are used for the switching regulator output to maintain low losses with large current charges at high frequencies.

4.5.2.4 Loop Regulator

To provide the loop gain and the stabilized reference voltage, a μ A723 voltage regulator integrated circuit (U13) is used. The internal reference voltage is 7.15V nominally. A potentiometer (R6) is used to reduce this reference down to +5V and to eliminate production variations. The 723 differential amplifier then amplifies the difference between the +5V (25 ampere) logic output to the adjusted reference divider by the gain (approximately 1000) of U13. The output of U13 then feeds a two-stage transistor amplifier (Q1, Q2) to provide a low output impedance on the control line at the proper voltage level and range of voltage swing. C6 and R17 form a noise filter to prevent "impulse" type noise on the control line of the waveform generator.

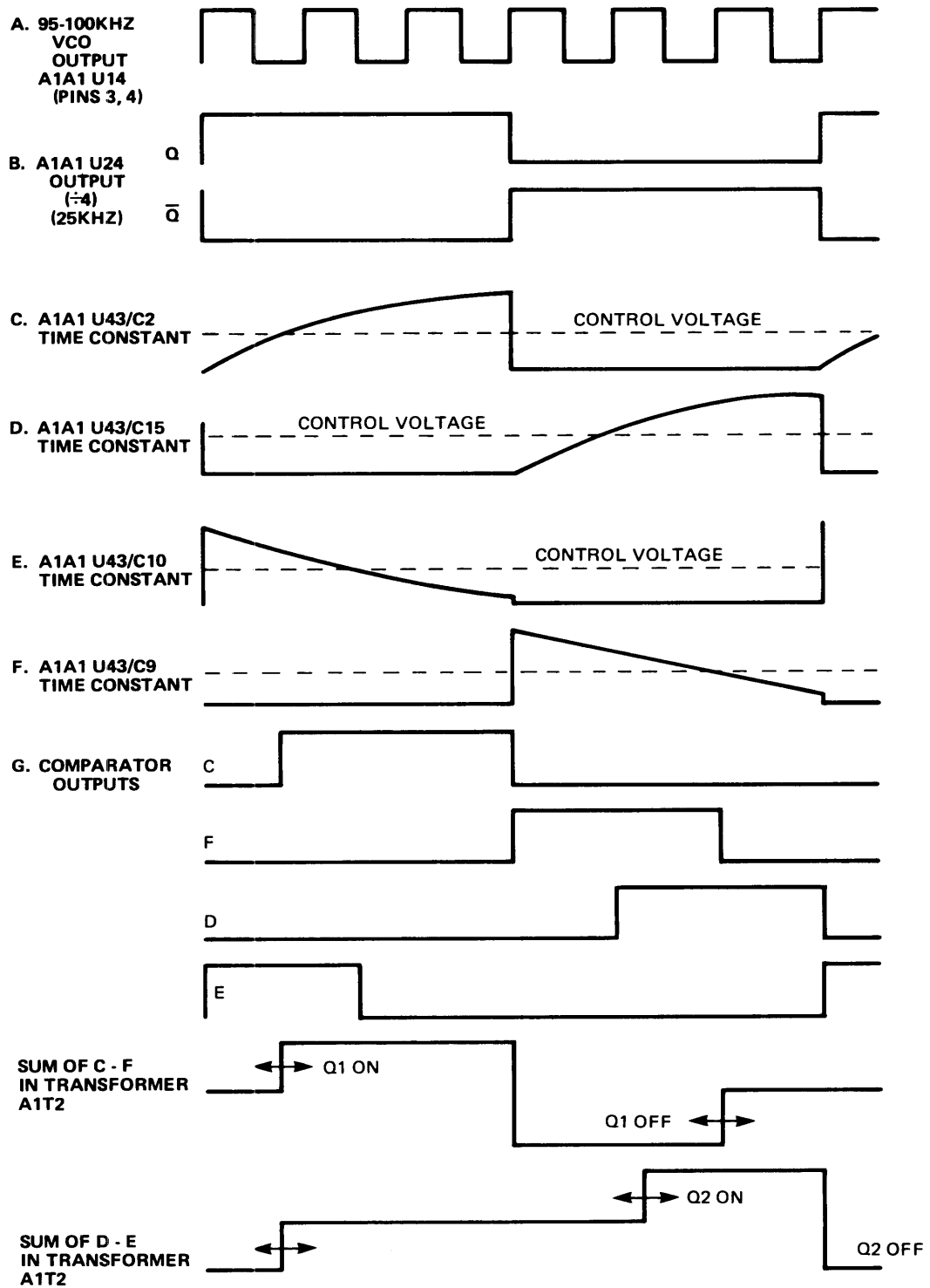


Figure 4-6. Two-Phase Switching Regulator Waveforms

A major loop roll-off corner frequency is formed by the output capacitor and choke input filter on the Schottky rectifier output of the +5V logic output. With load, this corner frequency changes considerably. At no load, the corner frequency is approximately 0.5Hz and at full load moves up to approximately 30Hz. To stabilize the loop, a 22uf capacitor (C8) in series with a 215-ohm resistor (R18) at the high impedance compensation node of U13, starts to roll the loop gain off at about .01Hz and is taken out at about 10Hz by R18. The final post amplifier roll-off is accomplished by the +5V output filter (L6 and C11 on the mother board in parallel with the load on the +5VDC output.)

The open-loop DC gain is in excess of 70db, which provides the very tight regulation of the +5V to within 10mV from no load to full load, typically when measured at the output capacitor on the copper strips.

4.5.2.5 Soft and Hard Fail Shutdown

Soft fail shutdown is an organized shutdown wherein the battery backup system and a power-fail software routine save the memory information. The stored charge in the input line rectifier capacitors allow the supply output to carry over the regulated voltage for a minimum of 5msec after the loss of primary power to allow the execution of the power-fail routine. The power supply will recover from a soft fail shutdown by itself without operator intervention. Once the condition causing soft fail shutdown has returned within limits the supply will ramp up to within specifications and issue the Power On (PON) logic signal.

The soft fail shutdown line is a normally high (+12V) level and goes low upon shutdown, staying low until released by the sensor pulling it down. Sensors on the soft fail shut down include line drop out and brown out level sensing, as well as Line Power Up (LPU), an external peripheral power supply sense input.

Hard fail shutdown is sudden and abrupt. It is used for catastrophic component failures or human-induced failures that would damage hardware if shutdown was not done immediately. Over-current on the inverter or switching regulator, over-voltage on the +5V logic bus, or undervoltage on the post regulated outputs (including short circuits) will cause hard fail shutdown. Hard fail shutdown lights a red LED at the right lower corner of the front panel of the supply. The hard fail shutdown is a latched condition. If the cause is well known, such as accidentally shorting out a DC output supply, then the AC switch can be recycled immediately to set the supply in operation again. If the cause is not known, the supply should be separated from the load before recycling the switch. If one of the outputs has been shorted or held low by the load, the supply will come up after removing the load, and cycling the AC power switch. The loads then can be resistance checked with an ohmmeter to find the shorted load. If the loop has gone out of control, the +5V output will ramp up to 6.5V maximum then quickly issue a hard fail shutdown, which causes the output to go to zero and the red light to light. Internal component failures of Schottky rectifiers, post regulators and other

components can also cause hard fail shutdown. The fast shutdown prevents further over stress and damage to other components.

Two other LED light sources are at the front panel lower right corner. A green one on the left of the hard fail shutdown red LED, indicates that AC power is present and that the +12V internal supply is operating. The green LED to the right of the red hard fail FAULT light, indicates that the PON logic signal has been issued and the supply is up and regulating.

4.5.3 LOGIC BOARD (PART NUMBER 12035-60004)

The schematic diagram for the logic board is shown in drawing 12035-60004. A photograph of the logic board is shown in figure 4-7. The logic board contains under-voltage limit comparators, line drop-out detector, Soft Fail Shutdown and Hard Fail Shutdown; and the Line Power Up, Power Supply Up, Power On, and Power Fail Warning logic.

The logic board monitors the line voltage and drop-out condition; the output DC voltages for under-voltage conditions; and the conditions of other supplies in a system interconnection. It then outputs the Power On Signal (PON); and the Power Fail Warning (PFW) signal.

Built in timing on this card provides the carry over time between PFW and PON going low and PON going true at turn on. It provides this delay to allow variations in the output to settle down before the computer is turned on.

4.5.3.1 Under-Voltage Limit Comparators

Two quad comparator packages, U8 and U9, provide the comparison of six output voltages with low limit references. One comparator in U9 provides accurate thresholding for the carry-over time constant, and the other comparator in U8 provides the line drop-out detector function. To make the low limit comparison reasonably accurate, a reference voltage is required for each voltage to be checked. In addition, negative output voltages must be checked with positive quadrant comparators, which require DC translation. U1 and reference diode CR2 with its associated resistors form the stable reference voltage from which all the references are derived. Potentiometer R1 allows adjustment to 4.8V via test point E1 to E7 (Gnd). This sets up one of the reference voltages used for the +/-12V supplies. The -12V supply uses CR10, a two-percent zener diode to translate the voltage into a positive voltage that can be compared by the unipolar comparator.

A voltage divider from E1 to ground in resistor package U7R provides the various positive voltages needed for the lower limits of +5L, +5M, +12L, and +12M. A resistive voltage divider consisting of a 1K resistor in U4 and

resistors R17 and R18 are used to translate the -12V memory bias voltage.

Outputs of comparators on the + and -12VL, +12VM, -5VM, and +5VM are open collector ORed and pulled up by a 3.16K resistor in U4R. This line is called DCC and is available at test point E5. The comparator on the +5VL line feeds a 100K pull-up resistor (U4R) and a 1 uf capacitor (C2) to ground forming, a 100msec a 100ms time constant on the rising waveform into NAND gate U5. The other input to the NAND is DCC. After inversion through another cell of U5 acting as an inverter, the signal becomes DCU. This signal goes true (high) when all supply outputs have exceeded their limits and settled out (which is provided by the 100 msec time delay).

4.5.3.2 Line Drop-Out Detector, SFS and HFS

The detection of line drop-outs is provided by an RC time constant on the motherboard in the +12INT supply and a differential amplifier (U8) on the logic card. The RC time constant as described in paragraph 4.5.3.1 is detected by the differentially-connected operational amplifier U8 on the logic board. The resistor network for the differential connection is incorporated in the U7 package. The absolute value of the voltage on the filter capacitor in the low voltage supply causes an imbalance in the differential amplifier under minimum line voltage conditions which also produces an output. The output is a "soft fail" shutdown described in paragraph 4.5.2.5. Capacitor C6 around the operational amplifier in the form of positive feedback provides dynamic hysteresis and forms a one-shot multivibrator when the differential threshold is exceeded. This causes the output low SFS pulse width to always be greater than 2 msec. At power supply turn on, SFS goes high as soon as the +12VINT supply comes up.

The logic formed by U5 and U6 gate packages and the discrete diode logic "OR" gate generates the soft fail and hard fail shutdown (described in paragraph 4.5.2.5) from the DCC (E5) and line dropout detector (LDD) signals. To prevent hard fail shutdown occasionally with soft fail shutdown, a delayed disable signal is required to the switching regulator drivers to provide a more controlled soft fail shutdown. This is provided by U5 which generates the disable signal from the line dropout detector.

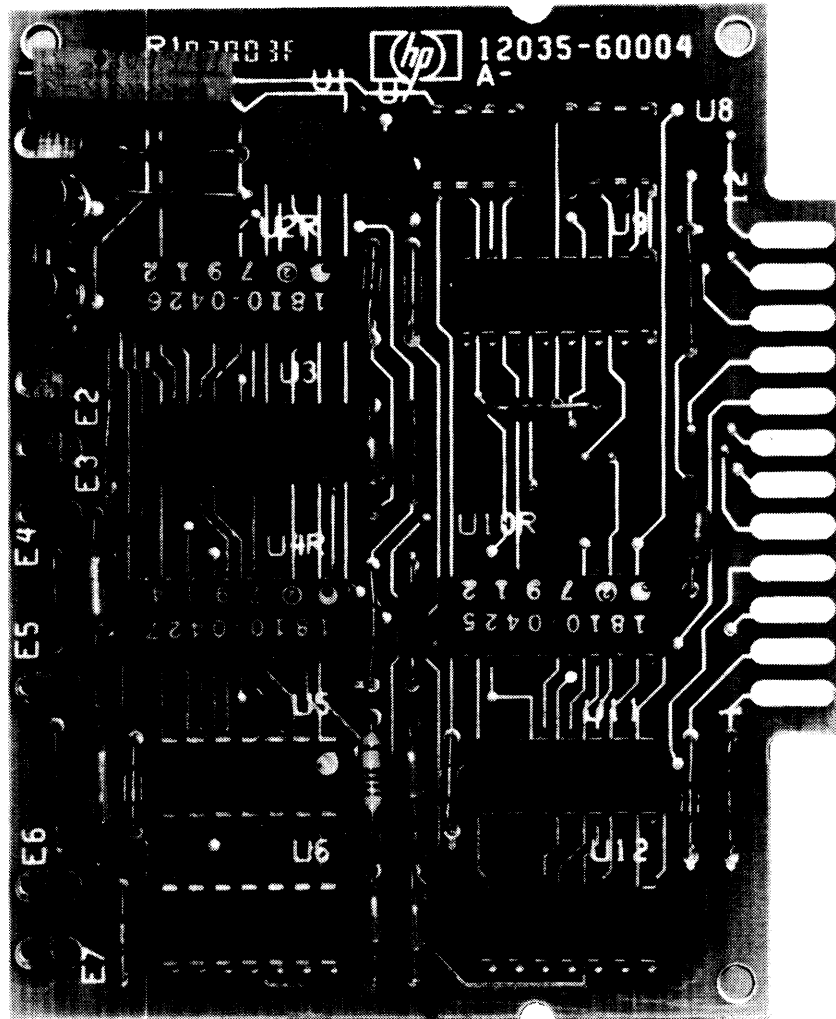


Figure 4-7. Logic Board (12035-60004)

4.5.3.3 LPU, PSU, PON, and PFW Logic

The LPU (Line Power Up) and PSU (Power Supply Up) signals are provided for an ANDing function if several supplies are used in a system. If this option is used, and if any supply in the system is without primary power none of the supplies in the system will come up (Soft fail shutdown). LPU provides this function. It is an open-collector line requiring 2mA maximum sink current, and can be ORed with similar lines. It is a bi-directional line and can be "daisy chained" to several system power supplies. When the primary power is turned off or removed from the input, the line will sink up to 6mA.

Under the conditions where an external supply sinks the LPU line, SFS (Soft Fail Shutdown, low true) will be pulled low and PFW (Power Fail Warning) will be held low at the CPU backplane. LPU is a TTL-compatible level (0.4V maximum, low; 2.2V minimum, high). PFW is an open-collector output with the pull-up resistor on the CPU. A sink capability of 100mA is provided at standard TTL levels on PFW. The rise and fall times must be less than 50 nsec and they must be free of noise. To provide this feature, U3, a Schmitt trigger, and the corresponding RC networks are used. SFS is also pulled low by the line dropout detector as described in paragraph 4.5.2.5, which in turn pulls PFW low. Upon PFW going low, the carry-over time is generated by R11, C8, and U9. This pulls DCC low causing DCU and PSU to go low. PSU warns external power supplies that the CPU power is off and the logic I/O buses will be unreliable. In turn, PON will be pulled low which turns the CPU off.

In the time between PFW low and PON going low, the CPU has had time to execute the power fail routine (guaranteed 5msec from PFW to PON going low). PON is conditioned to maintain less than 50 nsec rise and fall time, with up to 100mA sink current at TTL levels with no noise. Again, the Schmitt trigger (U3) with corresponding RC time constants perform this feature. An external low on PSU will also halt the CPU by pulling PON low. The electrical characteristics of PSU are similar to LPU. If primary power is not present on the power supply, PSU will also be held low, sinking up to 6mA (200 ohms maximum).

4.6 TROUBLE DIAGNOSIS

| SYMPTOM | POSSIBLE FAULT |
|-----------------------------------|--|
| Blows fuse (3AG, 7A) | Line voltage selector switch (A1S2) set to wrong range. Shorted A1Q5 or A1Q6. Shorted A1CR13. Defective A1Q3 or A1Q4. Connector J3, or A1Q1, A1Q2, A1Q3, or A1Q4 pin jack open. Shorted triac A1Q7. Shorted opto-isolator A1U7. Shorted A1U10. Defective driver board (12035-60003). |
| FAULT light comes on upon turn on | Shorted Schottky rectifier, A1CR9 or A1CR10. +5VL shorted to ground. ITR's A1Q3 or A1Q4 shorted. Bridge rectifier A1U4 shorted. 25kHz outputs shorted. +5V ADJ set too high. |

| SYMPTOM | POSSIBLE FAULT |
|--|--|
| LINE light does not come on | <p>Line voltage not getting to unit.</p> <p>Check driver board loading 12VINT (A1U5).</p> <p>Check logic board loading 12VINT (A1U5).</p> <p>A1CR5 open.</p> <p>A1U6 open.</p> |
| OPER light does not come on | <p>LPU is being held low (logic board).</p> <p>DC voltages did not come up.</p> |
| FAULT light comes on after power supply has operated long enough to warm up. | <p>Leaky Schottky rectifier A1CR9 or A1CR10.</p> <p>Slow turn off of A1Q5 or A1Q6.</p> <p>Overloaded output(s).</p> <p>Output loads increase with operating time.</p> <p>Defective driver board.</p> |

4.7 PARTS LOCATIONS

Parts locations for the HP 12035A power supply are shown in figures 4-8 through 4-10.

4.8 PARTS LIST

The parts lists for the power supply are shown in tables 4-2 through 4-5. Refer to table 6-39 for the names and addresses of manufacturers of the parts.

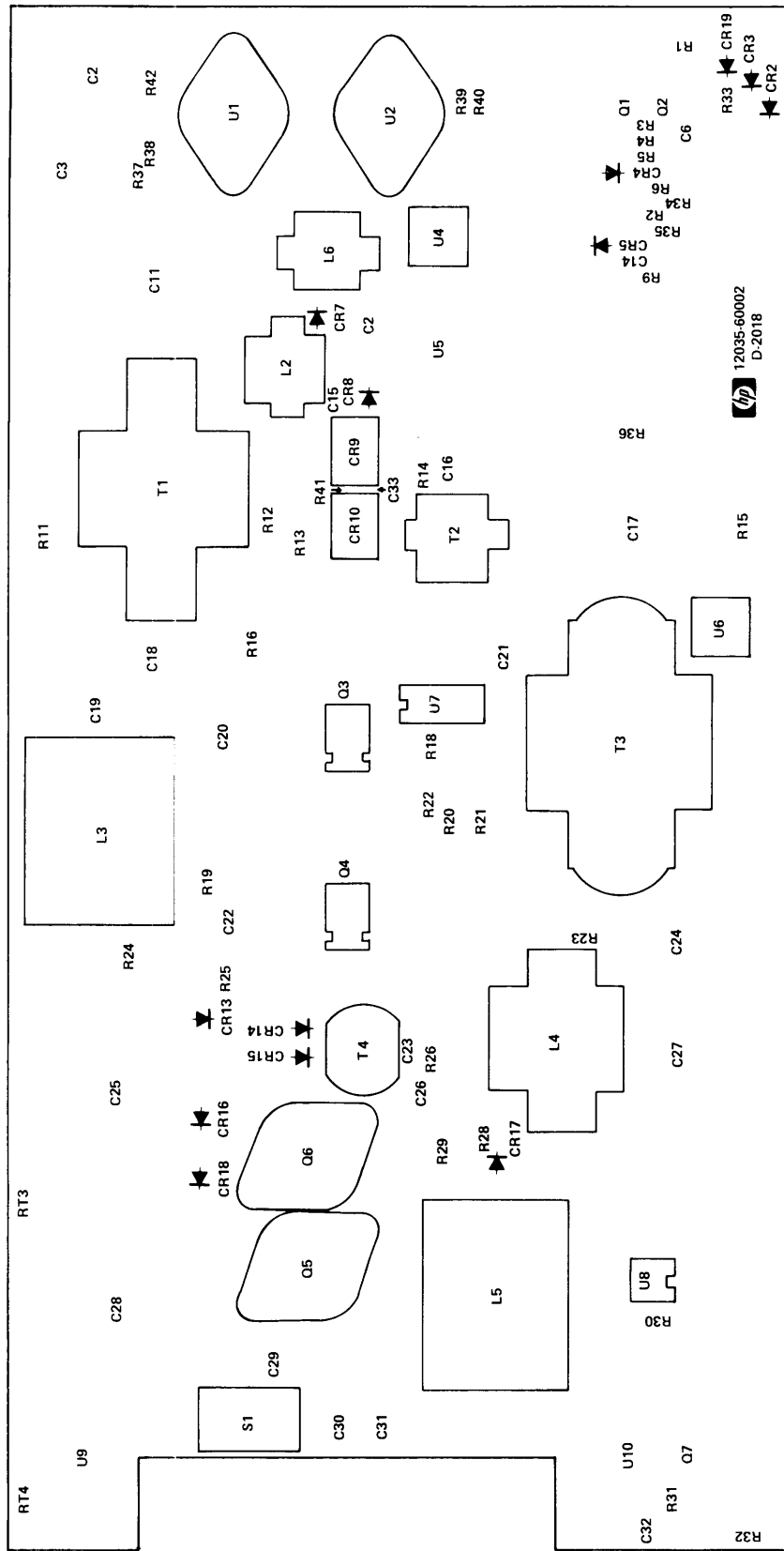


Figure 4-8. Motherboard Parts Locations

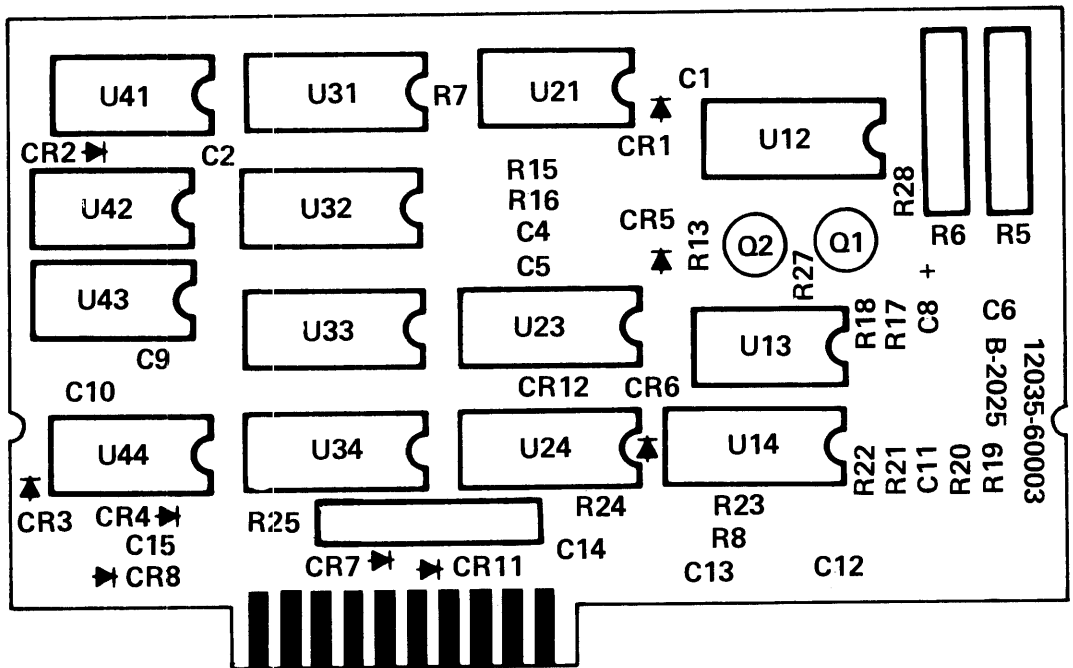


Figure 4-9. Driver Board Parts Locations

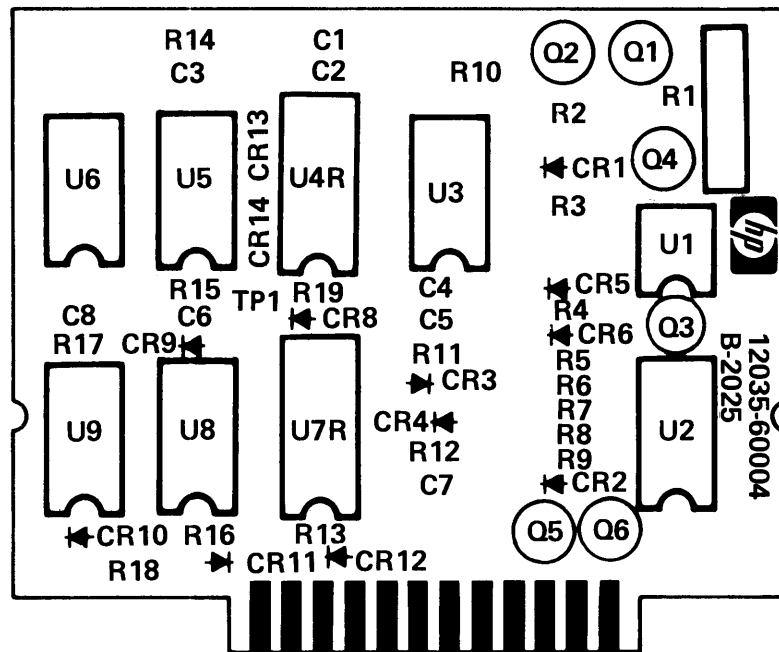


Figure 4-10. Logic Board Parts Locations

Table 4-2. Power Supply Replaceable Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------|
| C1 D1 | 12035-60005 | 3 | 1 | POWER-I/O PANEL | 28480 | 12035-60005 |
| | 0160-3451 | 1 | 1 | CAPACITOR=FXD .01UF +80=20% 100VDC CER | 28480 | 0160-3451 |
| | 0362-0561 | 6 | 3 | CONNECTOR=8GL CONT QDISC=FEM TAB | 28480 | 0362-0561 |
| | 1251-3812 | 2 | 1 | CONNECTOR 9=PIN M MINTR RECT | 28480 | 1251-3812 |
| | 1251-4687 | 1 | 2 | CONTACT=CONN U/W=UTIL FEM CRP | 28480 | 1251-4687 |
| | 1251-5227 | 7 | 1 | CONNECTOR 2=PIN UTILITY | 28480 | 1251-5227 |
| | 1251-5361 | 0 | 5 | CONTACT=CONN U/W=MINTR=RECT FEM CRP | 28480 | 1251-5361 |
| | 1251-5910 | 5 | 1 | CONNECTOR 4=PIN F POST TYPE | 28480 | 1251-5910 |
| | 1251-5917 | 2 | 4 | CONTACT=CONN U/W=POST-TYPE FEM CRP | 28480 | 1251-5917 |
| | 2110-0564 | 8 | 1 | FUSEHOLDER BODY 12A MAX FOR UL | H9027 | 031-1657 |
| | 2110-0565 | 9 | 1 | FUSEHOLDER CAP 12A MAX FOR UL | 28480 | 2110-0565 |
| | 2110-0569 | 3 | 1 | | 28480 | 2110-0569 |
| | 2110-0614 | 9 | 1 | FUSE 7A 250V NTD 1.25X.25 UL | 28480 | 2110-0614 |
| | 12035-60006 | 4 | 1 | FAN ASSEMBLY | 28480 | 12035-60006 |
| | 1251-3656 | 2 | 1 | CONNECTOR 2=PIN F UTILITY | 28480 | 1251-3656 |
| | 1251-4341 | 4 | 2 | CONTACT=CONN U/W=UTIL FEM CRP | 28480 | 1251-4341 |
| | 3160-0340 | 4 | 1 | FAN=TBAX 36=CFM 115V 50/60=HZ 1.5KV=DIEL | 28480 | 3160-0340 |

Table 4-3. Motherboard Replaceable Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------|
| | 12035-60002 | 0 | 1 | POWER SUPPLY MOTHER BOARD ASSEMBLY | 28480 | 12035-60002 |
| C2 | 0180-2727 | 4 | 2 | CAPACITOR-FXD 1900UF+75-10% 40VDC AL | 00853 | 300M8192U040B |
| C3 | 0180-2727 | 4 | 2 | CAPACITOR-FXD 1900UF+75-10% 40VDC AL | 00853 | 300M8192U040B |
| C11 | 0180-2932 | 3 | 1 | CAPACITOR-FXD .015F+75-0% 7.5VDC AL | 28480 | 0180-2932 |
| C14 | 0180-0128 | 3 | 1 | CAPACITOR-FXD 2.2UF +/-20% 50VDC CER | 28480 | 0180-0128 |
| C16 | 0180-0576 | 5 | 3 | CAPACITOR-FXD .1UF +/-20% 50VDC CER | 28480 | 0180-0576 |
| C17 | 0180-2180 | 3 | 1 | CAPACITOR-FXD 2600UF+75-10% 50VDC AL | 00853 | 500262U050A82A |
| C18 | 0180-4573 | 0 | 2 | CAPACITOR-FXD .22UF +/-10% 400VDC | 28480 | 0180-4573 |
| C19 | 0180-4573 | 0 | 2 | CAPACITOR-FXD .22UF +/-10% 400VDC | 28480 | 0180-4573 |
| C20 | 0180-4183 | 8 | 2 | CAPACITOR-FXD 1000PF +/-20% 250VAC(RMS) | 28480 | 0180-4183 |
| C22 | 0180-4183 | 8 | 2 | CAPACITOR-FXD 1000PF +/-20% 250VAC(RMS) | 28480 | 0180-4183 |
| C23 | 0180-0576 | 5 | 3 | CAPACITOR-FXD .1UF +/-20% 50VDC CER | 28480 | 0180-0576 |
| C24 | 0180-4785 | 6 | 2 | CAPACITOR-FXD .1UF +/-20% 50VDC CER | 28480 | 0180-4785 |
| C25 | 0180-0431 | 3 | 2 | CAPACITOR-FXD 1150UF+75-10% 200VDC AL | 00853 | 5001151U200882A |
| C26 | 0180-0576 | 5 | 3 | CAPACITOR-FXD .1UF +/-20% 50VDC CER | 28480 | 0180-0576 |
| C27 | 0180-4785 | 6 | 2 | CAPACITOR-FXD .1UF +/-20% 50VDC CER | 28480 | 0180-4785 |
| C28 | 0180-0431 | 3 | 2 | CAPACITOR-FXD 1150UF+75-10% 200VDC AL | 00853 | 5001151U200882A |
| C29 | 0180-4065 | 5 | 2 | CAPACITOR-FXD .1UF +/-20% 250VAC(RMS) | 28480 | 0180-4065 |
| C30 | 0180-4281 | 7 | 2 | CAPACITOR-FXD 2200PF +/-20% 250VAC(RMS) | C0633 | PME271Y422 |
| C31 | 0180-4281 | 7 | 2 | CAPACITOR-FXD 2200PF +/-20% 250VAC(RMS) | C0633 | PME271Y422 |
| C32 | 0180-4065 | 5 | 2 | CAPACITOR-FXD .1UF +/-20% 250VAC(RMS) | 28480 | 0180-4065 |
| C33 | 0180-0161 | 4 | 1 | CAPACITOR-FXD .01UF +/-10% 200VDC POLYE | 28480 | 0180-0161 |
| CR2 | 1990-0485 | 5 | 2 | LED-VISIBLE LUM=INT=800UCD IF=30MA=MAX | 28480 | 5082-4984 |
| CR3 | 1990-0486 | 6 | 1 | LED-VISIBLE LUM=INT=1MCD IF=20MA=MAX | 28480 | 5082-4684 |
| CR9 | 1901-0884 | 1 | 2 | DIODE-PWR RECT 35V DO-5 | 28480 | 1901-0884 |
| CR10 | 1901-0884 | 1 | 2 | DIODE-PWR RECT 35V DO-5 | 28480 | 1901-0884 |
| CR13 | 1901-1087 | 8 | 1 | DIODE-PWR RECT 600V 3A 200NS | 04713 | MR856 |
| CR19 | 1990-0485 | 5 | 2 | LED-VISIBLE LUM=INT=800UCD IF=30MA=MAX | 28480 | 5082-4984 |
| J2A | 1251-5666 | 8 | 1 | CONNECTOR 4-PIN M POST TYPE | 28480 | 1251-5666 |
| J2B | 1251-5665 | 7 | 2 | CONNECTOR 10-PIN M POST TYPE | 28480 | 1251-5665 |
| J2C | 1251-5665 | 7 | 2 | CONNECTOR 10-PIN M POST TYPE | 28480 | 1251-5665 |
| J3 | 1251-5843 | 3 | 1 | CONNECTOR-PC EDGE 10-CONT/ROW 2-ROWS | 28480 | 1251-5843 |
| J4 | 1251-5908 | 1 | 1 | CONNECTOR 2-PIN M UTILITY | 28480 | 1251-5908 |
| J5 | 1251-5841 | 1 | 1 | CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS | 28480 | 1251-5841 |
| J6 | 1251-5153 | 8 | 6 | CONNECTOR-SGL CONT QD18C=M .25-IN=88C-8Z | 28480 | 1251-5153 |
| J7 | 1251-5153 | 8 | 6 | CONNECTOR-SGL CONT QD18C=M .25-IN=88C-8Z | 28480 | 1251-5153 |
| J8 | 1251-5153 | 8 | 6 | CONNECTOR-SGL CONT QD18C=M .25-IN=88C-8Z | 28480 | 1251-5153 |
| J9 | 1251-5153 | 8 | 6 | CONNECTOR-SGL CONT QD18C=M .25-IN=88C-8Z | 28480 | 1251-5153 |
| J10 | 1251-5153 | 8 | 6 | CONNECTOR-SGL CONT QD18C=M .25-IN=88C-8Z | 28480 | 1251-5153 |
| J12 | 1251-3305 | 8 | 1 | CONNECTOR 4-PIN M POST TYPE | 28480 | 1251-3305 |
| J22 | 1251-5153 | 8 | 6 | CONNECTOR-SGL CONT QD18C=M .25-IN=88C-8Z | 28480 | 1251-5153 |
| L1 | 9140-0326 | 0 | 2 | INDUCTOR 50UH 10% .875DX1.125LG | 28480 | 9140-0326 |
| L2 | 9140-0326 | 0 | 2 | INDUCTOR 50UH 10% .875DX1.125LG | 28480 | 9140-0326 |
| L3 | 9140-0337 | 3 | 1 | INDUCTOR-FIXED DUAL TOROID; 100 UH+/-10% | 28480 | 9140-0337 |
| L4 | 9140-0336 | 2 | 1 | INDUCTOR-FIXED SWITCHING INDUCTOR; 1.0 | 28480 | 9140-0336 |
| L5 | 9140-0346 | 4 | 1 | INDUCTOR-FIXED DUAL TOROID; 1.0 MM PER | 28480 | 9140-0346 |
| L6 | 9140-0342 | 0 | 1 | INDUCTOR 25UH 1.7DX.8LG | 28480 | 9140-0342 |
| Q1 | 1A53-0036 | 2 | 1 | TRANSISTOR PNP SI PD=310MW FT=250MHZ | 28480 | 1A53-0036 |
| Q2 | 1A54-0467 | 5 | 1 | TRANSISTOR NPN 2N4401 SI TO=92 PD=310MW | 03508 | 2N4401 |
| Q3 | 1A84-0287 | 0 | 2 | THYRISTOR-SCR | 28480 | 1A84-0287 |
| Q4 | 1A84-0287 | 0 | 2 | THYRISTOR-SCR | 28480 | 1A84-0287 |
| Q5 | 1A54-0855 | 5 | 2 | TRANSISTOR NPN TO-3 PD=150W | 28480 | 1A54-0855 |
| Q6 | 1A54-0855 | 5 | 2 | TRANSISTOR NPN TO-3 PD=150W | 28480 | 1A54-0855 |
| Q7 | 1A84-0277 | 8 | 1 | THYRISTOR-TRIAC TO-220AB | 03508 | 8C141M5 |
| R11 | 0811-3570 | 6 | 1 | RESISTOR 6.8 5% 5W PW TC=0+-50 | 28480 | 0811-3570 |
| R15 | 0764-0042 | 0 | 1 | RESISTOR 2.2K 5% 2W MO TC=0+-200 | 28480 | 0764-0042 |
| R20 | 0811-1553 | 1 | 1 | RESISTOR .68 5% 2W PW TC=0+-800 | 75042 | BWH2=11/16-J |
| R21 | 0A11-1552 | 0 | 1 | RESISTOR .56 5% 2W PW TC=0+-800 | 75042 | BWH2=9/16-J |
| R24 | 0764-0040 | 8 | 2 | RESISTOR 39K 5% 2W MO TC=0+-200 | 28480 | 0764-0040 |
| R25 | 0764-0040 | 8 | 2 | RESISTOR 39K 5% 2W MO TC=0+-200 | 28480 | 0764-0040 |
| R26 | 0757-0401 | 0 | 3 | RESISTOR 100 1% .125W F TC=0+-100 | 24546 | C4=1/8-T0=101-F |
| R27 | 0757-0401 | 0 | 3 | RESISTOR 100 1% .125W F TC=0+-100 | 24546 | C4=1/8-T0=101-F |
| R31 | 0A11-3108 | 6 | 1 | RESISTOR 2 10% PWH | 28480 | 0811-3108 |
| R32 | 0757-0401 | 0 | 3 | RESISTOR 100 1% .125W F TC=0+-100 | 24546 | C4=1/8-T0=101-F |
| R41 | 2100-3154 | 7 | 1 | RESISTOR-TRMR 1K 10% C SIDE=ADJ 17-TRM | 02111 | 43P102 |
| RY3 | 0A37-0208 | 5 | 2 | | 28480 | 0837-0208 |
| RY4 | 0A37-0208 | 5 | 2 | | 28480 | 0837-0208 |

Table 4-3. Motherboard Replaceable Parts List (Continued)

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|---|----------|-----------------|
| S1 | 3101-2373 | 3 | 1 | SWITCH=SLIDE DP2T PC | 28480 | 3101-2373 |
| T1 | 9100-4126 | 4 | 1 | TRANSFORMER INVERTER, 106 V 25 KHZ | 28480 | 9100-4126 |
| T2 | 9100-4126 | 2 | 1 | TRANSFORMER SCR GATE TRIGGER, 4 VRMS 25 | 28480 | 9100-4126 |
| T3 | 9100-4127 | 3 | 1 | TRANSFORMER=POWER 115/230V 50-60HZ | 28480 | 9100-4127 |
| T4 | 9100-4125 | 1 | 1 | TRANSFORMER DUAL DRIVER, PC MTG, 20 KHZ | 28480 | 9100-4125 |
| U1 | 1813-0123 | 4 | 1 | IC 78HG V RGLTR TO-3 | 07263 | UA78HGKC |
| U2 | 1813-0127 | 8 | 1 | | 28480 | 1813-0127 |
| U4 | 1906-0079 | 6 | 1 | DIODE-FW BRDG 100V 10A | 27777 | VJ148X |
| U5 | 1826-0147 | 9 | 1 | IC 7812 V RGLTR TO-220 | 04713 | MC7812CP |
| U6 | 1906-0062 | 7 | 2 | DIODE-FW BRDG 600V 6A | 28480 | 1906-0062 |
| U7 | 1990-0664 | 2 | 1 | OPTO-ISOLATOR LED-PXSTR IF#40MA=MAX | 28480 | 1990-0664 |
| U8 | 1990-0680 | 2 | 1 | OPTO-ISOLATOR LED-PHOTOSCR IF#60MA=MAX | 03508 | H11C6 |
| U9 | 1906-0062 | 7 | | DIODE-FW BRDG 600V 6A | 28480 | 1906-0062 |
| U10 | 1906-0226 | 5 | 1 | DIODE-FW BRDG 800V 1A | 28480 | 1906-0226 |
| W1 | 8159-0005 | 0 | 2 | WIRE 22AWG W PVC 1X22 80C | 28480 | 8159-0005 |
| W2 | 8159-0005 | 0 | | WIRE 22AWG W PVC 1X22 80C | 28480 | 8159-0005 |

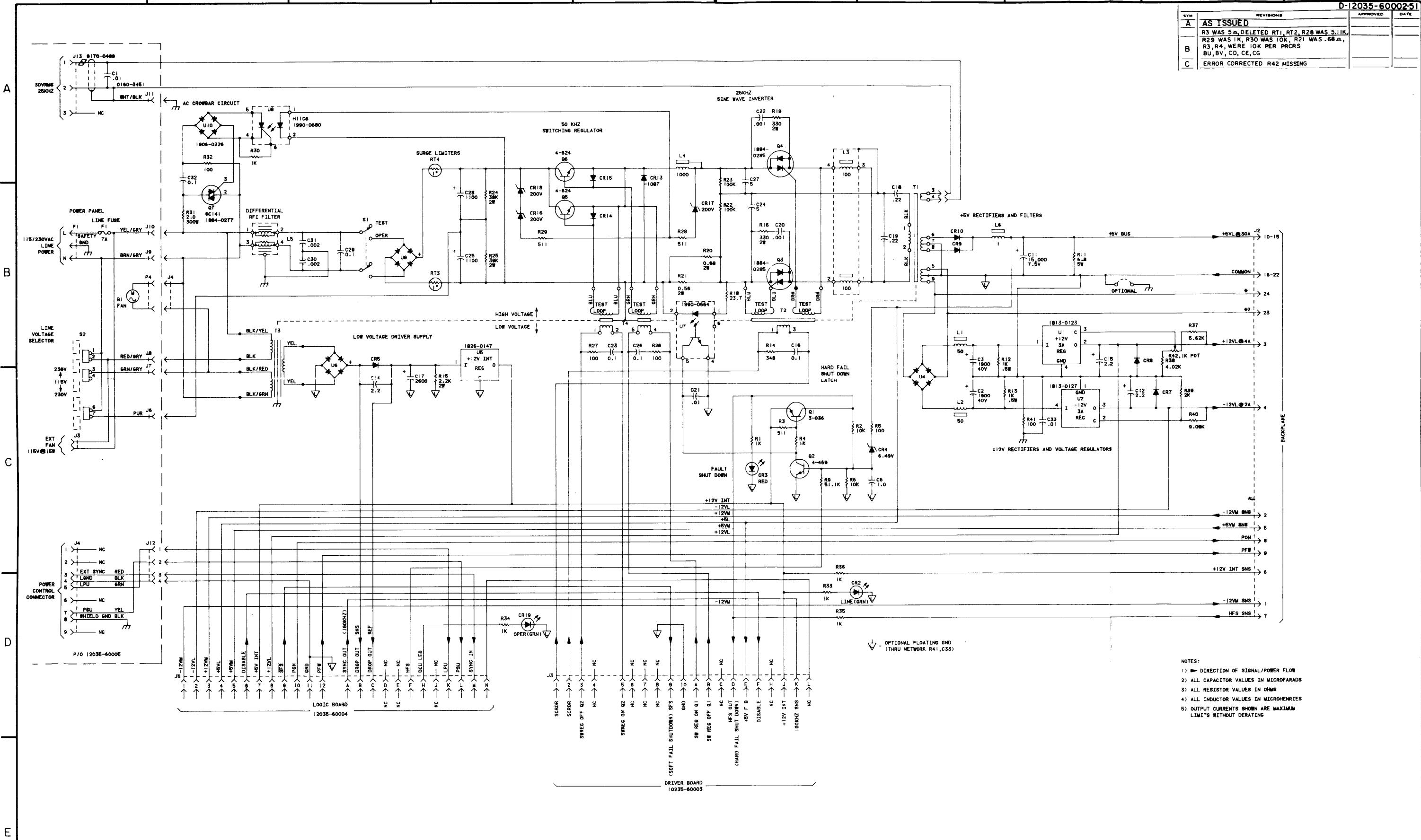
Table 4-4. Driver Board Replaceable Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-----------------|
| | 12035-60003 | 1 | 1 | POWER SUPPLY DRIVER BOARD | 28480 | 12035-60003 |
| C12 | 0160-0164 | 7 | 1 | CAPACITOR-FXD .039UF +/-10% 200VDC POLYE | 28480 | 0160-0164 |
| Q1 | 1854-0215 | 1 | 2 | TRANSISTOR NPN SI PD=350MW FT=300MHZ | 04713 | 2N3904 |
| Q2 | 1854-0215 | 1 | 1 | TRANSISTOR NPN SI PD=350MW FT=300MHZ | 04713 | 2N3904 |
| R5 | 2100-3161 | 6 | 1 | RESISTOR-TRMR 20K 10% C SIDE=ADJ 17-TRN | 02111 | 43P203 |
| R6 | 2100-3109 | 2 | 1 | RESISTOR-TRMR 2K 10% C SIDE=ADJ 17-TRN | 02111 | 43P202 |
| R25 | 1810-0125 | 0 | 1 | NETWORK-RES 8-SIP4.7K OHM X 7 | 28480 | 1810-0125 |
| U12 | 1810-0040 | 8 | 1 | NETWORK-RES 16-DIP MULTI-VALUE | 28480 | 1810-0040 |
| U13 | 1820-0439 | 0 | 1 | IC V RGLTR 14-DIP=P | 07263 | 723PC |
| U14 | 1820-1188 | 8 | 1 | IC PL LOOP 16-DIP=P | 01928 | CD4046AP |
| U21 | 1826-0138 | 8 | 2 | IC COMPARATOR GP QUAD 14-DIP=P | 01295 | LM339N |
| U23 | 1820-1266 | 3 | 7 | IC BFR CMOS NON-INV HEX | 07263 | 40097PC |
| U24 | 1820-1964 | 8 | 1 | IC FF CMOS J-K POS-EDGE-TRIG DUAL | 01928 | CD4027BE |
| U31 | 1820-1266 | 3 | | IC BFR CMOS NON-INV HEX | 07263 | 40097PC |
| U32 | 1820-1266 | 3 | | IC BFR CMOS NON-INV HEX | 07263 | 40097PC |
| U33 | 1820-1266 | 3 | | IC BFR CMOS NON-INV HEX | 07263 | 40097PC |
| U34 | 1820-1266 | 3 | | IC BFR CMOS NON-INV HEX | 07263 | 40097PC |
| U41 | 1820-1266 | 3 | | IC BFR CMOS NON-INV HEX | 07263 | 40097PC |
| U42 | 1820-1266 | 3 | | IC BFR CMOS NON-INV HEX | 07263 | 40097PC |
| U43 | 1810-0212 | 6 | 1 | NETWORK-RES 16-DIP22.0K OHM X 8 | 01121 | 3168223 |
| U44 | 1826-0138 | 8 | | IC COMPARATOR GP QUAD 14-DIP=P | 01295 | LM339N |

Table 4-5. Logic Board Replaceable Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|--------|-----|---|----------|-----------------|
| | 12035-60004 | 2 | 1 | POWER SUPPLY LOGIC | 28480 | 12035-60004 |
| Q1 | 1855-0421 | 3 | 2 | TRANSISTOR J-FET 2N5114 P-CHAN D-MODE | 17856 | 2N5114 |
| Q2 | 1A55-0421 | 3 | | TRANSISTOR J-FET 2N5114 P-CHAN D-MODE | 17856 | 2N5114 |
| Q3 | 1854-0467 | 5 | 4 | TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW | 03508 | 2N4401 |
| Q4 | 1854-0467 | 5 | | TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW | 03508 | 2N4401 |
| Q5 | 1854-0467 | 5 | | TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW | 03508 | 2N4401 |
| Q6 | 1854-0467 | 5 | | TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW | 03508 | 2N4401 |
| R1 | 2100-3154 | 7 | 1 | RESISTOR-TRMR 1K 10% C 8IDE-ADJ 17-TRN | 02111 | 43P102 |
| U1 | 1826-0346 | 0 | 1 | IC OP AMP GP DUAL 8-DIP-P | 27014 | LM358N |
| U2 | 1820-1778 | 2 | 2 | IC SCHMITT-TRIG CMOS HEX | 27014 | MM74C914N |
| U3 | 1A20-177A | 2 | | IC SCHMITT-TRIG CMOS HEX | 27014 | MM74C914N |
| U4 | 1810-0427 | 5 | 1 | NETWORK-RES 16-DIP MULTI-VALUE | 28480 | 1810-0427 |
| U5 | 1820-1747 | 5 | 1 | IC GATE CMOS NAND QUAD 2-INP | 04713 | MC14011UCP |
| U6 | 1820-1965 | 9 | 1 | IC GATE CMOS NOR TPL 3-INP | 04713 | MC140258CP |
| U7 | 1810-0425 | 3 | 1 | NETWORK-RES 16-DIP MULTI-VALUE | 28480 | 1810-0425 |
| U8 | 1826-0138 | 8 | 2 | IC COMPARATOR GP QUAD 14-DIP-P | 01295 | LM339N |
| U9 | 1826-0138 | 8 | | IC COMPARATOR GP QUAD 14-DIP-P | 01295 | LM339N |

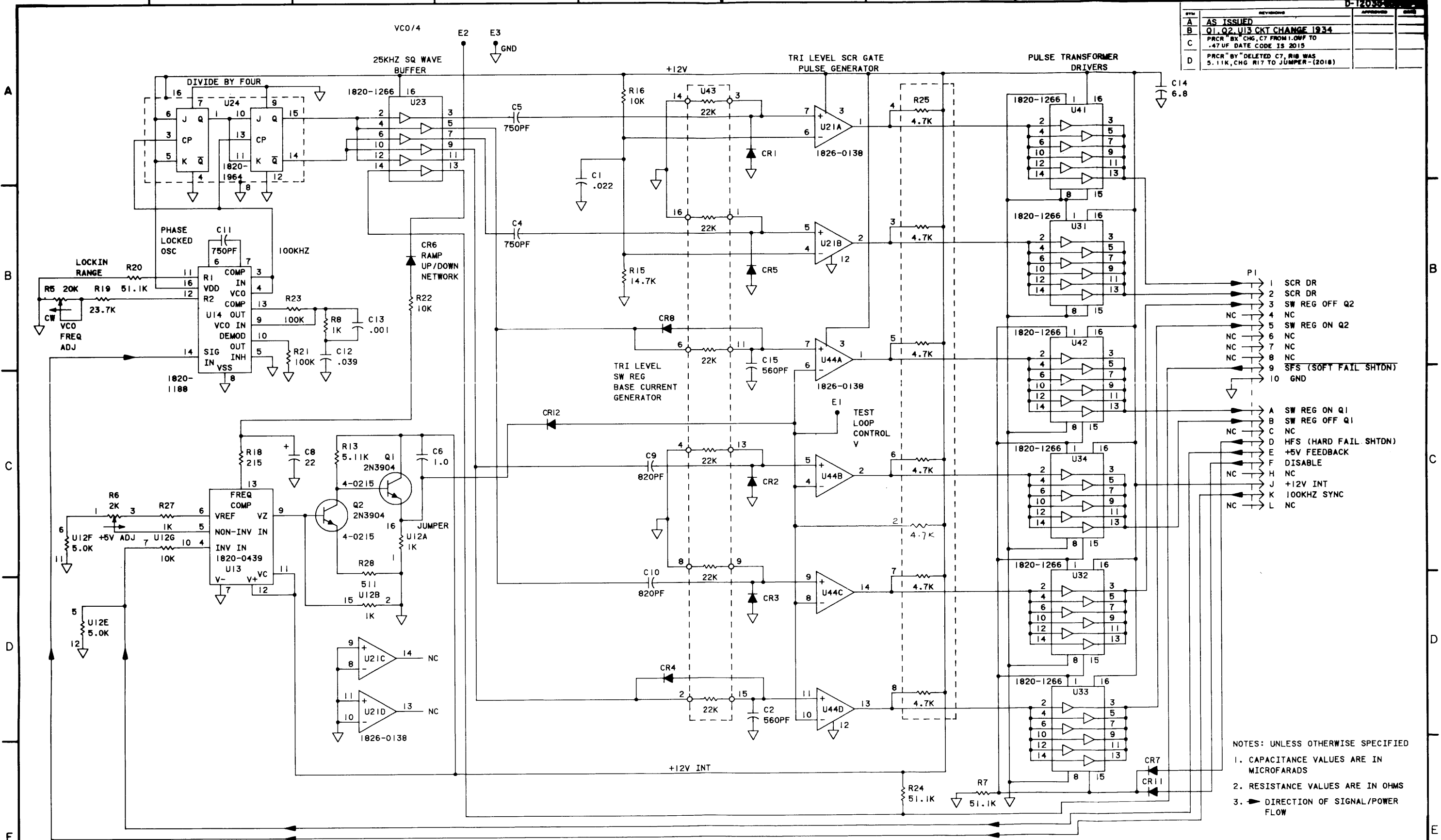
| REV | DESCRIPTION | APPROVED | DATE |
|-----|---|----------|------|
| A | AS ISSUED | | |
| B | R3 WAS 5.0, DELETED RT1, RT2, R28 WAS 5.1K, R29 WAS 1K, R30 WAS 10K, R21 WAS .68, R3, R4, WERE 10K PER PRCRS BU, BV, CD, CE, CG | | |
| C | ERROR CORRECTED R42 MISSING | | |



- NOTES:
- 1) DIRECTION OF SIGNAL/POWER FLOW
 - 2) ALL CAPACITOR VALUES IN MICROFARADS
 - 3) ALL RESISTOR VALUES IN OHMS
 - 4) ALL INDUCTOR VALUES IN MICROHENRIES
 - 5) OUTPUT CURRENTS SHOWN ARE MAXIMUM LIMITS WITHOUT DERATING

| | | | |
|--|--------|----------------------|-------------|
| HP 12035A POWER SUPPLY MOTHERBOARD | | HEWLETT PACKARD | |
| TITLE | 12035A | PART NUMBER | 12035-60002 |
| NEXT ASSEMBLY | | FINISH | SCALE |
| | | D-12035 - 60002 - 51 | |

| | | |
|-----|---|------|
| REV | DESCRIPTION | DATE |
| A | AS ISSUED | |
| B | Q1, Q2, U13 CKT CHANGE 1934 | |
| C | PRCR BY CHG C7 FROM 1.0UF TO .47UF DATE CODE IS 2015 | |
| D | PRCR BY DELETED C7, R18 WAS 5.11K, CHG R17 TO JUMPER-(2018) | |



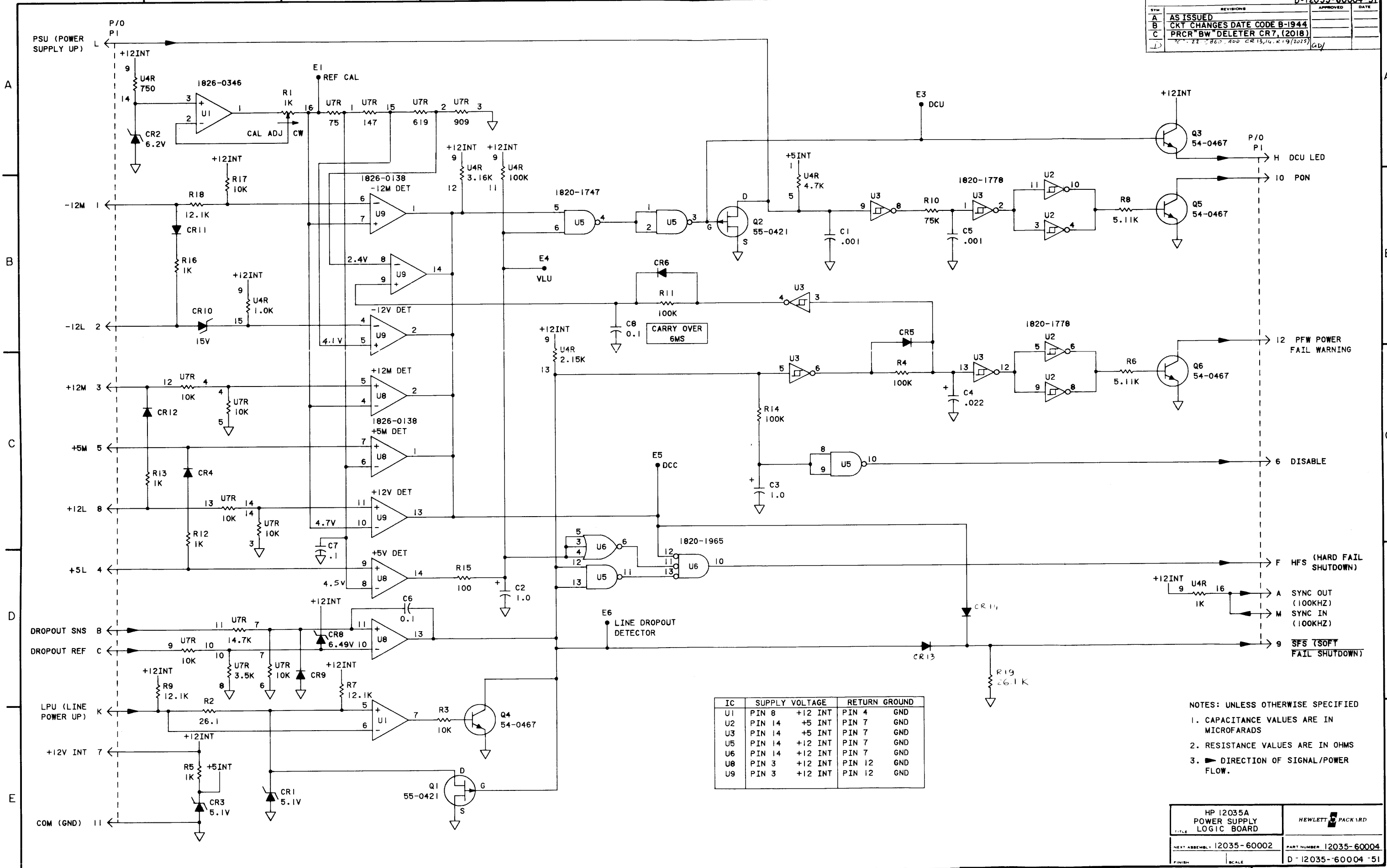
- PI
- 1 SCR DR
 - 2 SCR DR
 - 3 SW REG OFF Q2
 - 4 NC
 - 5 SW REG ON Q2
 - 6 NC
 - 7 NC
 - 8 NC
 - 9 SFS (SOFT FAIL SHTDN)
 - 10 GND
- A SW REG ON Q1
 B SW REG OFF Q1
 C NC
 D HFS (HARD FAIL SHTDN)
 E +5V FEEDBACK DISABLE
 F NC
 J +12V INT
 K 100KHZ SYNC
 L NC

NOTES: UNLESS OTHERWISE SPECIFIED

1. CAPACITANCE VALUES ARE IN MICROFARADS
2. RESISTANCE VALUES ARE IN OHMS
3. ► DIRECTION OF SIGNAL/POWER FLOW

| | | |
|-------------------------------------|---------------------------|-------------------------|
| HP 12035A POWER SUPPLY DRIVER BOARD | | HEWLETT-PACKARD |
| TITLE | NEXT ASSEMBLY 12035-60002 | PART NUMBER 12035-60003 |
| FINISH | SCALE | D-12035-60003-51 |

| REV | DESCRIPTION | DATE |
|-----|-------------------------------------|------|
| A | AS ISSUED | |
| B | CKT CHANGES DATE CODE B-1944 | |
| C | PRCR "BW" DELETER CR7, (2018) | |
| D | 2018.11.06, ADD CR13,14, R19 (2018) | |



| IC | SUPPLY VOLTAGE | RETURN GROUND |
|----|----------------|---------------|
| U1 | PIN 8 +12 INT | PIN 4 GND |
| U2 | PIN 14 +5 INT | PIN 7 GND |
| U3 | PIN 14 +5 INT | PIN 7 GND |
| U5 | PIN 14 +12 INT | PIN 7 GND |
| U6 | PIN 14 +12 INT | PIN 7 GND |
| U8 | PIN 3 +12 INT | PIN 12 GND |
| U9 | PIN 3 +12 INT | PIN 12 GND |

NOTES: UNLESS OTHERWISE SPECIFIED
 1. CAPACITANCE VALUES ARE IN MICROFARADS
 2. RESISTANCE VALUES ARE IN OHMS
 3. ► DIRECTION OF SIGNAL/POWER FLOW.

| | | |
|--|-------------------------|--------------------|
| HP 12035A POWER SUPPLY LOGIC BOARD | | HEWLETT PACKARD |
| NEXT ASSEMBLY 12035-60002 | PART NUMBER 12035-60004 | |
| FINISH | SCALE | D-12035-60004-51 |

| | |
|----------------|-----------|
| BATTERY BACKUP | SECTION V |
|----------------|-----------|

5.1 INTRODUCTION

The Hewlett-Packard HP 12013A Battery Backup system is a non-interruptible power supply that provides memory voltages to maintain data during the absence of AC line power. The battery backup system is contained on one circuit card and plugs directly into the L-Series backplane (i.e., the battery backup card is not part of the power supply). The circuit card is shown in figure 5-1.

5.2 OVERVIEW

The purpose of a memory support battery backup system is to act as a non-interruptible power supply and protect computer memory from AC line power disturbances.

The following kinds of AC line power disturbances exist:

- a. Voltage sag, which is a drop in AC line voltage longer than 5 msec but not longer than 5 seconds.
- b. Power interruption, which is a complete loss of power for longer than 5 msec but not longer than 0.5 second.
- c. Power outage, which is a complete loss of power for more than 0.5 second.

All the components of the battery backup (six batteries, battery regulators, and control logic) are on one circuit card.

The batteries contain enough power to support memory for one hour. Because the memory 5 volt supply range is 4.75 to 5.25 volts, and the batteries provide 6.0 to 7.5 volts, regulation of the battery voltage is required. Linear regulation is used, because it provides noise-free regulation which is necessary in the card cage.

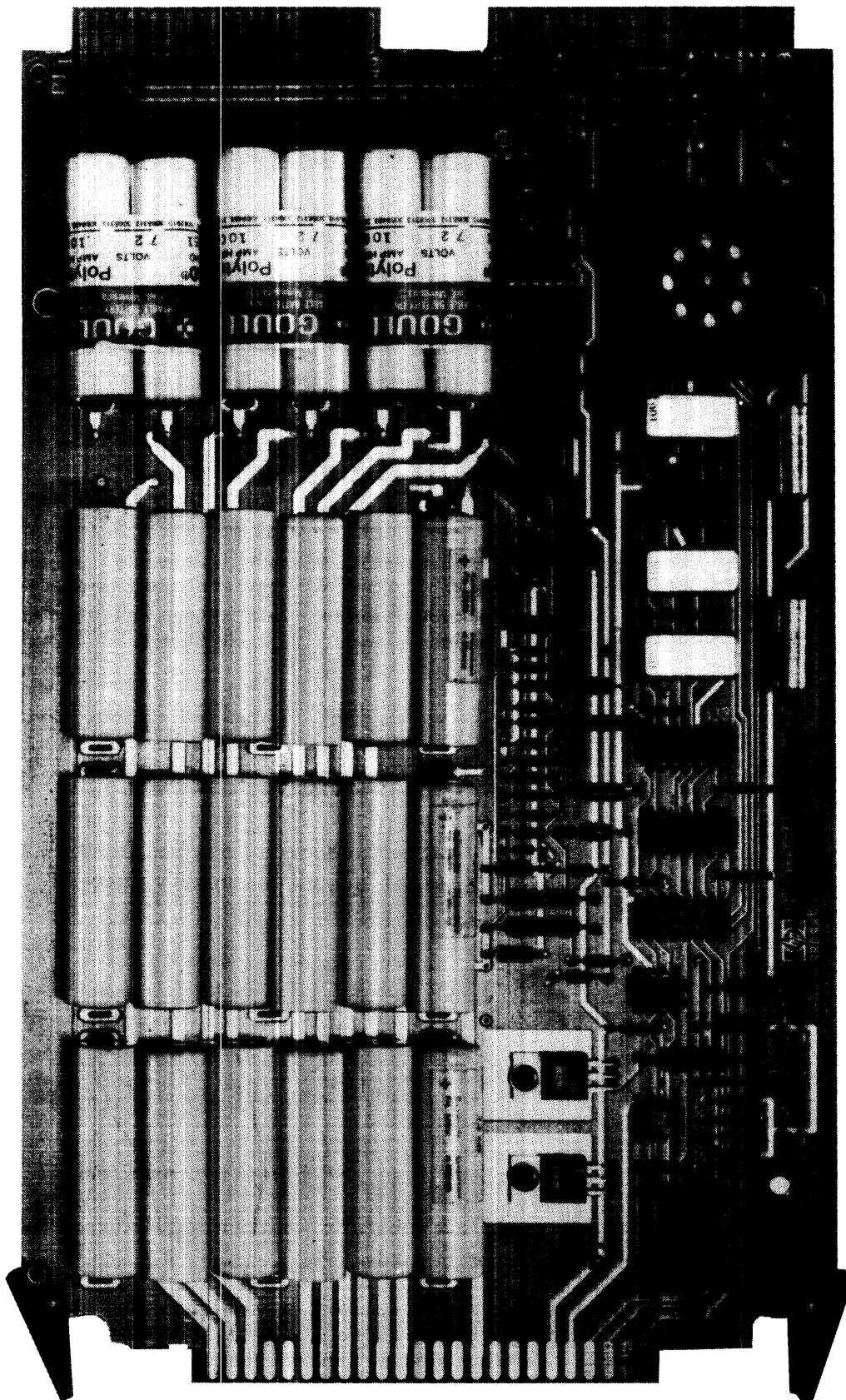


Figure 5-1. HP 1000 L-Series Battery Backup Card

When AC line power is present, the batteries are being charged and the memory voltages are supplied by the main power supply. A relay is used to control this connection. After two cycles of AC line power loss, the main power supply causes the processor to execute a power fail sequence, and causes the battery backup card to supply power to memory. After the battery regulator circuit is enabled, the relay opens and memory now is supported from batteries.

5.3 SPECIFICATIONS

Specifications for the battery backup card are listed in table 5-1.

Table 5-1. Specifications

| |
|--|
| <p>OUTPUT VOLTAGES</p> <p>+5M: 5.25 to 4.75 volts +12M: 11.4 to 12.6 volts -12M: -6.0 to -8.4 volts</p> |
| <p>OUTPUT CURRENT</p> <p>+5M: 1500 mA maximum +12M: 500 mA maximum -12M: 110 mA maximum</p> |
| <p>OVER-VOLTAGE LIMITS</p> <p>+5M: 7 volts maximum +12M: 15 volts maximum -12M: -15 volts maximum</p> |
| <p>ACTUAL LOAD - MEMORY OPERATIONAL</p> <p>+5 volts: 750 mA maximum (memory board) 250 mA maximum (CPU board) 50mA maximum (power supply logic) TOTAL 1050 mA maximum</p> <p>+12 volts: 290 mA maximum (memory board)</p> <p>-12 volts: 20 mA maximum (memory board)</p> |

Table 5-1. Specifications (Continued)

| | | |
|---|---------------------|--------------------|
| ACTUAL LOAD - MEMORY IN STANDBY | | |
| +5 volts: | 1050 mA maximum | |
| +12 volts: | 72 mA maximum | |
| -12 volts: | 20 mA maximum | |
| MEMORY SUPPORT TIME - MAXIMUM LOAD | | |
| <u>Configuration</u> | <u>Support Time</u> | <u>Memory Size</u> |
| 12002A | 1 hr 56 min | 128KB |
| 12002A and one 12003A | 1 hr 23 min | 256KB |
| 12002A and two 12003A | 1 hr 4 min | 384KB |
| 12002A and three 12003A | 53 min | 512KB |
| 12002B | 1 hr 29 min | 512KB |
| 12004A | 1 hr 9 min | 64KB |
| BATTERY CAPACITY | | |
| 7.2 volts: | 1500 mAh | |
| 14.4 volts: | 110 mAh | |
| -7.2 volts: | 110 mAh | |
| BATTERY CHARGE CURRENT | | |
| 7.2 volts: | 150 mA from +12V | |
| 14.4 volts: | 22 mA from +12V | |
| -7.2 volts: | 11 mA from -12V | |
| BATTERY CHARGE POWER | | |
| +12V: | 2.17 watts | |
| -12V: | 0.13 watts | |
| BATTERY CHARGE TIME | | |
| Batteries must charge 14 minutes for every 1 minute of discharge (15 minute discharge requires 210 minute recharge, 60 minute discharge requires 840 minute recharge, etc.) | | |

5.4 INTERFACE REQUIREMENTS

5.4.1 INTERFACE SIGNALS

The L-Series backplane provides all interface signal lines needed for operation of the battery backup, as follows:

| SIGNAL | CONNECTOR AND PIN NUMBER |
|--------|---------------------------------|
| PFW | P1, PIN 7 |
| MLOST | P1, PIN 5 |
| +12M | P2, PIN 39 |
| +5M | P2, PINS 45, 46 |
| -12M | P2, PIN 40 |
| +12V | P2, PINS 41, 42 |
| +5V | P2, PINS 35, 36, 37, 38 |
| -12V | P2, PINS 43, 44 |
| GROUND | P2, PINS 29, 30, 31, 32, 33, 34 |

5.4.2 EXTERNAL CONNECTOR

Interface connector J1 is used for fast charge of batteries or to connect the batteries to external devices. The battery backup connections to J1 are as follows:

| BATTERY NUMBER AND VOLTAGE | J1 PIN NUMBER |
|----------------------------|---------------|
| 1 - +5 volts | 2 |
| 2 - +12 volts | 4 |
| 3 - +5 volts | 6 |
| 4 - +12 volts | 8 |
| 5 - +12 volts | 10 |
| 6 - -7.2 volts | 12 |

5.4.3 REMOTE/OFF/ON SWITCH

A REMOTE/OFF/ON switch is located on the battery backup card (see figure 5-1).

In the REMOTE position, the remote input is connected to the battery backup card control circuits so that memory is not sustained if power is turned off.

In the OFF position, the relays and regulators are disabled and the memory voltages are a subset of the processor voltages. If AC line power is lost with the switch in the OFF position, memory voltages will not be sustained and data in memory will be lost.

In the ON position, the battery board is enabled upon loss of AC line power, memory voltages are sustained and data in memory is not lost.

5.4.4 AUDIO ALARM

An audio alarm is used to indicate that the memory is on the battery backup system (AC line power lost), and to indicate when the MLOST signal is low (memory or CPU configured incorrectly).

When the memory is on battery backup, the alarm sounds for one second on and 9 seconds off. If the computer is configured incorrectly, the alarm sounds continuously.

Additionally, a two-second alarm is sounded upon power-up if memory data has been lost.

5.4.5 POWER SUPPLY INTERFACE

When AC line power is lost, the HP 12035A Power Supply asserts the PFW (Power Fail Warning) signal. This signal indicates that there is a minimum of 5 msec of regulated DC power. The PFW signal is used to turn on the battery backup and to separate memory power from the CPU power.

5.4.6 CENTRAL PROCESSOR UNIT INTERFACE

If memory voltages fall below the regulation level, the MLOST signal is asserted by the battery backup. The MLOST signal will be asserted for one second after PON is valid. MLOST is used by the CPU to determine if memory data has been lost. If data has not been lost, an auto restart is performed; if data has been lost, memory is cleared and the boot program is entered.

5.5 FUNCTIONAL THEORY OF OPERATION

A functional block diagram of the battery backup is shown in figure 5-2.

5.5.1 BATTERY CHARGER

The HP 12013A Battery Backup card contains six nickel-cadmium batteries: three of 7.2 volt, 500 mAh, and three of 7.2 volt, 100 mAh.

The batteries are charged at a 0.1C rate. This charge rate is low enough so that the batteries can withstand the overcharge rate indefinitely, yet is high enough to provide an "overnight" charge. Five of the battery charge currents are limited by a series resistor to the power supply +12 volts through connector J2, pins 41 and 42. The sixth battery charge current is limited by a series resistor to the power supply -12 volts through connector J2, pins 43 and 44.

5.5.2 VOLTAGE REGULATORS

The battery backup card contains two voltage regulators. One regulates +5 volts, the other +12 volts. Both regulators are designed to operate with a 500 mvolt Vin/Vout differential, and are enabled upon loss of AC line power.

There are no adjustments for the regulators; the reference for each regulator is 2.5 volts +/- 25 mvolts.

5.5.3 NORMAL OPERATION (AC LINE POWER PRESENT)

During normal operation, AC line power is present and the battery backup is in a charge mode. The regulators are disabled and relays short +5M to +5V (J2, pins 45 and 46 to J2, pins 35, 36, 37 and 38), and +12M to +12V (J2, pin 39 to J2, pins 41 and 42). Upon PFW going low, the regulators are enabled and the relays open (removing the shorts).

When PFW goes high (AC line power returns), the regulators are disabled and the relays close, shorting +5M to +5V and +12M to +12V again.

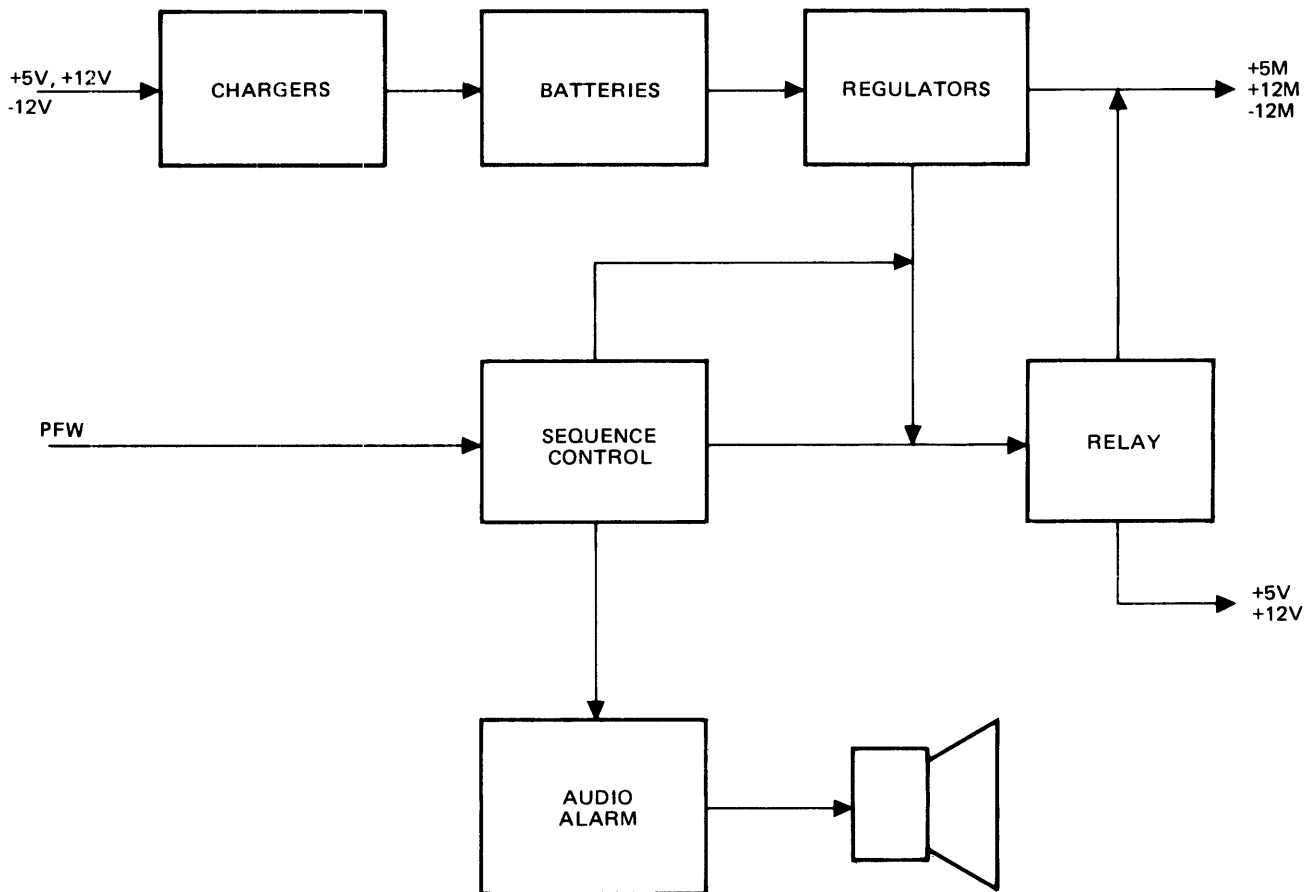


Figure 5-2. Battery Backup Functional Block Diagram

5.5.4 -12 VOLTS

The -12 volts is supplied through a diode to -12 volts on the CPU card, or to -7.2 volts on the battery backup card. This voltage is re-regulated on the memory board down to -5 volts.

5.6 THEORY OF OPERATION

The following paragraphs contain a detailed theory of operation for the battery backup. All components referred to in these paragraphs are shown on the schematic diagram located at the end of this section.

5.6.1 BATTERY CHARGER

Batteries BT4, BT5, and BT6 for the +5 volt regulators are charged through resistor/diode combinations to +12M. For example, BT6 is charged through R26 and CR14 (see the schematic diagram). The resistor limits the current to 61 mA when the battery is fully charged to 7.2 volts. The diode prevents the battery from being discharged through the resistor when the battery backup and the computer are both turned off. Batteries BT4 and BT5 are charged in the same manner using the combinations R29/CR16 and R13/CR11, respectively. Diodes CR13, CR15, and CR12 are used to isolate the batteries so that each is charged individually.

Batteries BT2 and BT3 for the +12 volt regulator also are charged through resistor/diode combination to +12M. BT2 charges through R7 and CR6; BT3 charges through R8 and CR10. While the batteries are charging, relay K3 configures the batteries in parallel (7.2 volts). Resistors R7 and R8 limit the charging current to 17 mA. When operational, relay K3 configures the batteries in series for 14.4 volts.

Battery BT1 output is used for -12 volts and is not regulated. This battery is charged through CR1 and R1 from -12M. Resistor R1 limits the charging current to 17 mA.

5.6.2 +5 VOLT REGULATOR

Operational amplifier U7 and transistors Q3 and Q4 are used for the +5 volt regulation. U7 is used as the error amplifier; pin 3 is the 2.5 volt reference input. The output of the regulator (from Q3) is divided by R30 and R32; this voltage is the negative feedback and is applied to U7, pin 2. The

error amplifier adjusts its output (U7, pin 1) to control the base drive transistor Q4 and series pass transistor Q3. The output of U7 (pin 1) will drive Q4 and Q3 until U7, pin 2 is equal to the reference voltage (U7, pin 3). At this point, the collector of Q3 is at +5 volts and U7 pins 2 and 3 are both 2.5 volts.

The output of the error amplifier (U7, pin 1) is used to turn on the base drive transistor Q4. The higher the output at pin 1, the more Q4 turns on, lowering its collector voltage, and raising the collector voltage of Q3. The base current of Q4 is limited by R33 to a maximum of 1.0 mA. Under minimum voltage conditions, Q4 may go into saturation.

Transistor Q4 controls the base drive of the series pass transistor Q3. The base current of Q3 is limited by R31 to 60 mA. The output of Q3 is the +5 volt regulator output. This output is filtered by capacitor C3.

Over-voltage protection is provided by the 5-volt Transorb CR8. CR8 will limit the output voltage to a safe level (7.0 volts) if there is a component failure or if there is an external over-voltage condition. If the power level exceed 1500 watts for more than 8 msec, CR8 will fail (shorts).

Over-current protection is provided by current sense resistor R11 and comparator U3 (pins 8, 9, and 14). U3, pin 8 monitors the current of batteries BT4, BT5, and BT6. If the voltage into U3, pin 3 from the voltage divider R21/R22 exceeds 160 mvolts, then U3, pin 14 lowers +5 volt regulator reference voltage at U7, pin 3, and the regulator will turn off.

5.6.3 +12 VOLT REGULATOR

Operational amplifier U7 and transistors Q2 and Q5 are used for the +12 volt regulation. U7 is used as the error amplifier; pin 5 is the 2.5 volt reference input. The output of the regulator (from Q2) is divided by R35 and R36; this voltage is the negative feedback and is applied to U7, pin 6. The error amplifier adjusts its output (U7, pin 7) to control the base drive transistor Q5 and series pass transistor Q2. The output of U7 (pin 7) will drive Q2 and Q5 until U7, pin 6 is equal to the reference voltage (U7, pin 5). At this point, the collector of Q2 is at +12 volts and U7 pins 5 and 6 are both 2.5 volts.

The output of the error amplifier (U7, pin 7) is used to turn on the base drive transistor Q5. The higher the output at pin 7, the more Q5 turns on, lowering its collector voltage, and raising the collector voltage of Q2. The base current of Q5 is limited by R34 to a maximum of 1.0 mA. Under minimum voltage conditions, Q5 may go into saturation.

Transistor Q5 controls the base drive of the series pass transistor Q2. The base current of Q2 is limited by R37 to 60 mA. The output of Q2 is the +12 volt regulator output. This output is filtered by capacitor C2.

Over-voltage protection is provided by the 12-volt Transorb CR9. CR9 will limit the output voltage to a safe level (15.0 volts) if there is a component failure or if there is an external over-voltage condition. If the power level exceed 1500 watts for more than 8 msec, CR9 will fail (short).

Over-current protection is provided by current sense resistor R9 and comparator U3 (pins 10, 11, and 13). U3, pin 10 monitors the current of batteries BT2, and BT3. If the voltage into U3, pin 11 from the voltage divider R17/R18 exceeds 160 mvolts, then U3, pin 13 lowers +12 volt regulator reference voltage at U7, pin 5, and the regulator will turn off.

5.6.4 -12 VOLT OUTPUT

Negative 7.2 volts is provided for the memory -12M voltage. Transistor Q1 is used as a switch. If +12M is present, diode CR3 will have 9.0 volts across it and Q1 base/emitter resistor R2 will have 10 volts across it (10 mA base drive). Transistor Q1 will turn on. If +12 volts is not present, the voltage across CR3 and R2 will be lower and Q1 will turn off. This switching circuit is necessary to prevent the battery from being discharged when the computer is turned off.

5.6.5 RELAY LOGIC

Relays K1, K2, and K3 are momentary type relays and are normally closed (pin 4 to 1). Relay K3 is used to connect batteries BT2 and BT3 in series or parallel (see paragraph 5.6.1).

Relay K1 is used to provide a path for the computer power supply to provide memory with +12 volts. Relay K1 is used for the power supply to provide memory with +5 volts.

All three relays (K1, K2, and K3) are driven by U5.

Switch S1 is used to switch the battery backup to ON, OFF, or REMOTE. When S1 is ON, the relays are connected to CR7 and R5. If power is lost, CR7 is used to power the relays; R5 limits the current and holds the relays on. The relays will not activate unless 12 volts is present. Thus, the battery backup will stay off, even if S1 is ON, if the card is plugged into a computer with its power off.

5.6.6 CONTROL SEQUENCE LOGIC

The battery backup card uses the PFW signal to control the operation of the regulator, relays, and audio alarm.

Table 5-2 shows a power down sequence and table 5-3 shows a power up sequence. CR21, R24, and C9 provide an RC time delay of 3 msec for relays K1 and K2 (table 5-2, step 6). CR22, R16, and C6 provide 3 msec delay (table 5-3, step 4) to keep regulators on until primary regulation of the power is restored. U3, pins 1 and 2 form an OR gate. If PFW (U3-1) or the batteries are less than 1 volt per cell (U3-2), then relay K3 is opened. This turns the 12-volt regulator off, relays K1 and K2 lose power (+12M), and the battery backup turns off.

The data path formed by P1-7, U3-6, U4-12, U5-1, and K3 is used to enable the regulators. Data path P1-7, U4-9, U4-3, U5-2, K2, and K1 is used to connect power supply voltages to the memory.

Logic levels for sequence control are 0 to +12 volts; 2.5 volts is the threshold.

When AC line power is present, the regulators on the battery backup card are disabled. Diodes CR17 (5 volt regulator) and CR19 (12 volt regulator) are grounded by relay K3, the anodes of the diodes clamp the voltage of the base drive transistors (Q4 and Q5) to approximately 1.0 volts. Because of diodes CR15 and CR20, greater than 2 volts is required to turn on the base drive transistors.

5.6.7 AUDIO ALARM/MLOST SIGNAL

The audio alarm (DS1) is driven by U1. When the battery backup is operating, U5, pin 11 enables the timing components C1, R3, and R4. The timer is on for 1 second, off for 9.

The reset on U1 (pin 4) is used to produce a continuous tone if the MLOST signal or the MLOST timer is low. U2 is the MLOST timer. If the +5M voltage drops to less than 4.66 volts, the MLOST timer goes low and the continuous tone is produced. The timer resets itself after about 2 seconds.

Table 5-2. AC Line Power Down Sequence

1. Power Fail Warning (PFW) goes low.
2. Delay of 100 usec.
3. Alarm timer is enabled; alarm will sound in 9 seconds.
4. Relay K3 configures BT2 and BT3 in series (14.4 volts). One msec to complete.
5. Regulators are enabled.
6. Delay of 3 msec.
7. Relays K1 and K2 disconnect memory load from processor load. Three msec to complete.
8. Battery backup is enabled.

Table 5-3. AC Line Power Up Sequence

1. Power Fail Warning (PFW) goes high.
2. Delay of 100 usec.
3. Relays K1 and K2 connect memory load to processor load.
4. Delay of 3 msec.
5. Alarm timer is disabled.
6. Relay K3 configures BT2 and BT3 in parallel for charge operation.
7. Regulators are disabled.
8. Memory is now powered from HP 12035A Power Supply (AC primary power).

5.7 PARTS LOCATIONS

Parts locations for the HP 12013A Battery Backup are shown in figure 5-3.

5.8 PARTS LIST

The parts list for the battery backup is shown in table 5-4. Refer to table 6-39 for the names and addresses of manufacturers of the parts.

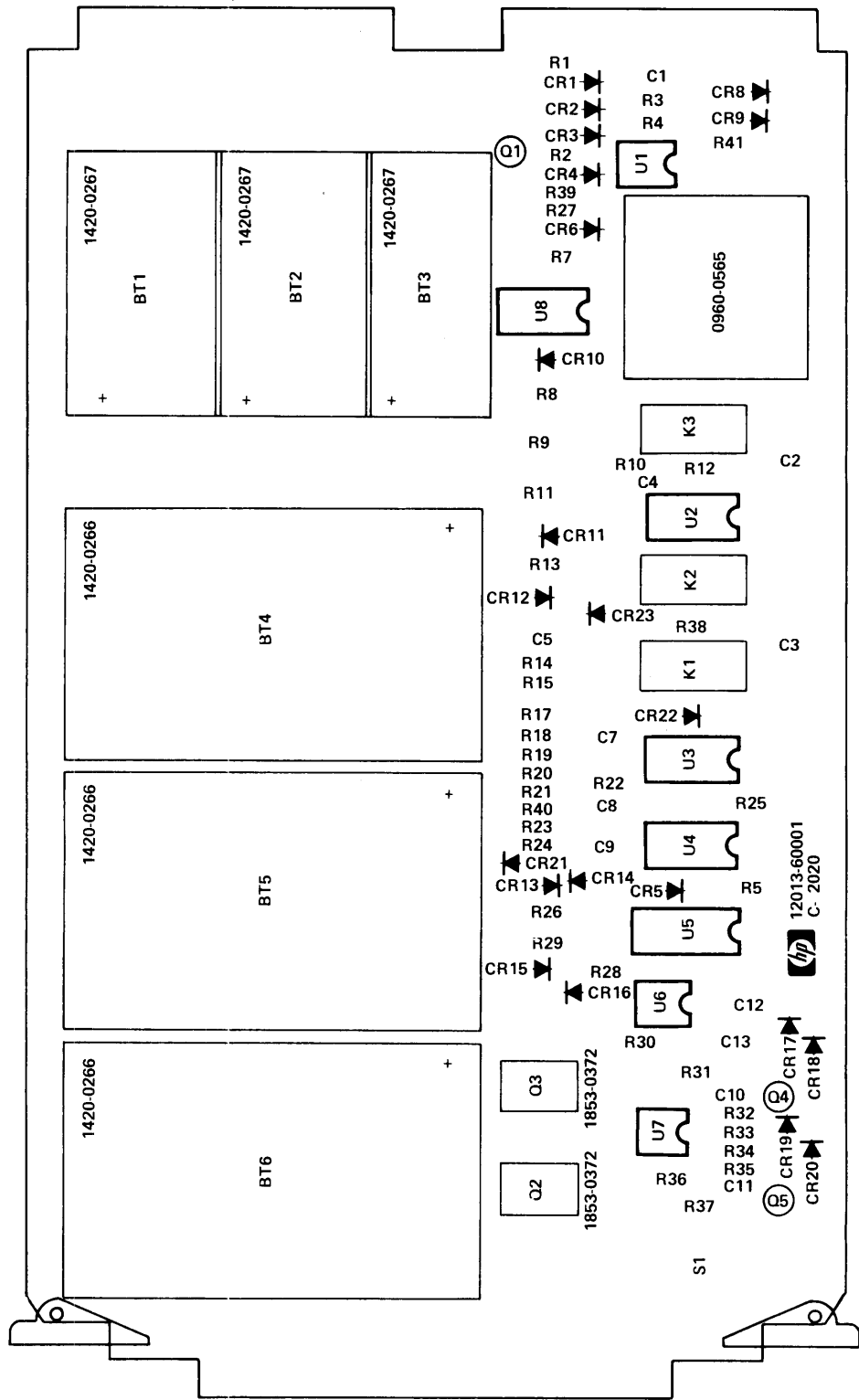
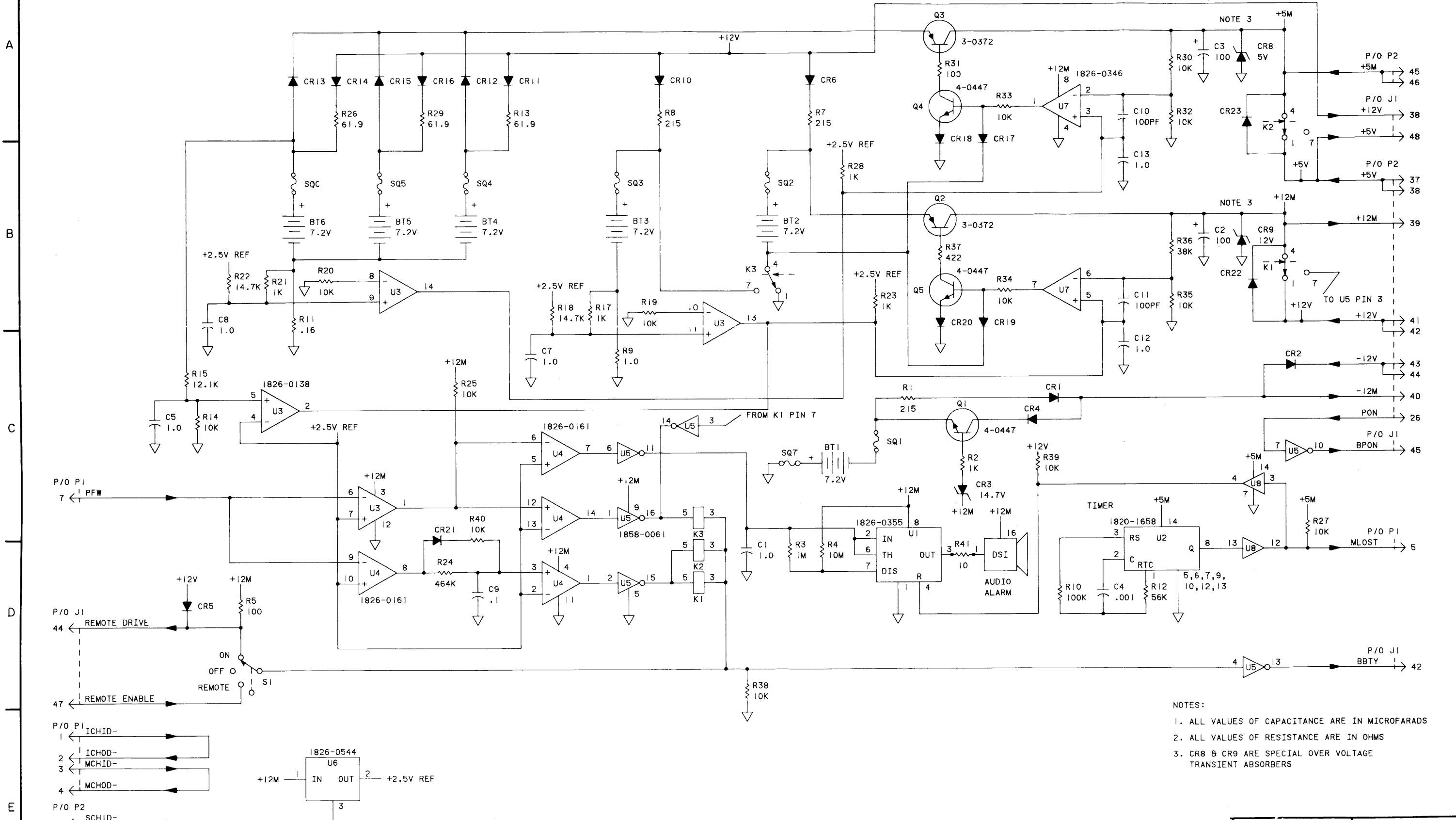


Figure 5-3. HP 12013A Battery Backup Parts Locations

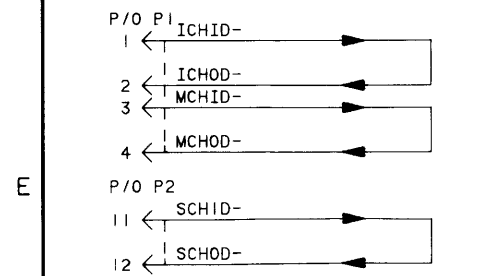
Table 5-4. Battery Backup Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|---|----------|-----------------|
| | 12013-60001 | 3 | 1 | BATTERY BACKUP | 28480 | 12013-60001 |
| C2 | 0180-2374 | 7 | 2 | CAPACITOR=FXD 100UF+/-10% 20VDC TA | 56289 | 150D107X9020X2 |
| C3 | 0180-2374 | 7 | 2 | CAPACITOR=FXD 100UF+/-10% 20VDC TA | 56289 | 150D107X9020X2 |
| CR8 | 1902-0939 | 9 | 1 | DIODE-ZNR 5V P _D =5W T _C +0.06% I _R =300UA | 11961 | 1N5908 |
| CR9 | 1902-0941 | 3 | 1 | DIODE-ZNR 12V P _D =5W T _C +0.084% I _R =2UA | 11961 | 1.58E15A |
| CR12 | 1901-1080 | 1 | 5 | DIODE-SCHOTTKY 1N5817 20V 1A | 28480 | 1901-1080 |
| CR13 | 1901-1080 | 1 | 1 | DIODE-SCHOTTKY 1N5817 20V 1A | 28480 | 1901-1080 |
| CR15 | 1901-1080 | 1 | 1 | DIODE-SCHOTTKY 1N5817 20V 1A | 28480 | 1901-1080 |
| CR22 | 1901-1080 | 1 | 1 | DIODE-SCHOTTKY 1N5817 20V 1A | 28480 | 1901-1080 |
| CR23 | 1901-1080 | 1 | 1 | DIODE-SCHOTTKY 1N5817 20V 1A | 28480 | 1901-1080 |
| K1 | 0490-0694 | 7 | 3 | RELAY-REED 1C 1A 30VDC 12VDC-COIL | 28480 | 0490-0694 |
| K2 | 0490-0694 | 7 | 3 | RELAY-REED 1C 1A 30VDC 12VDC-COIL | 28480 | 0490-0694 |
| K3 | 0490-0694 | 7 | 3 | RELAY-REED 1C 1A 30VDC 12VDC-COIL | 28480 | 0490-0694 |
| Q1 | 1854-0477 | 7 | 3 | TRANSISTOR NPN 2N2222A 8I TO-18 P _D =500MW | 04713 | 2N2222A |
| Q2 | 1853-0372 | 9 | 2 | TRANSISTOR PNP 8I TO-220AB P _D =60W | 04713 | MJE5195 |
| Q3 | 1853-0372 | 9 | 2 | TRANSISTOR PNP 8I TO-220AB P _D =60W | 04713 | MJE5195 |
| Q4 | 1854-0477 | 7 | 3 | TRANSISTOR NPN 2N2222A 8I TO-18 P _D =500MW | 04713 | 2N2222A |
| Q5 | 1854-0477 | 7 | 3 | TRANSISTOR NPN 2N2222A 8I TO-18 P _D =500MW | 04713 | 2N2222A |
| R1 | 0698-3401 | 0 | 3 | RESISTOR 215 1% .5W F TC ₀ +/-100 | 28480 | 0698-3401 |
| R7 | 0698-3401 | 0 | 3 | RESISTOR 215 1% .5W F TC ₀ +/-100 | 28480 | 0698-3401 |
| R8 | 0698-3401 | 0 | 3 | RESISTOR 215 1% .5W F TC ₀ +/-100 | 28480 | 0698-3401 |
| R9 | 0811-1666 | 7 | 1 | RESISTOR 1 5% 2W PW TC ₀ +/-800 | 75042 | 8WH2-1R0-J |
| R11 | 0811-3291 | 8 | 1 | RESISTOR .12 5% 2W PW TC ₀ +/-800 | 28480 | 0811-3291 |
| R13 | 0757-1002 | 9 | 3 | RESISTOR 61.9 1% .5W F TC ₀ +/-100 | 28480 | 0757-1002 |
| R26 | 0757-1002 | 9 | 3 | RESISTOR 61.9 1% .5W F TC ₀ +/-100 | 28480 | 0757-1002 |
| R29 | 0757-1002 | 9 | 3 | RESISTOR 61.9 1% .5W F TC ₀ +/-100 | 28480 | 0757-1002 |
| R31 | 0757-0198 | 2 | 1 | RESISTOR 100 1% .5W F TC ₀ +/-100 | 28480 | 0757-0198 |
| R37 | 0698-3405 | 4 | 1 | RESISTOR 422 1% .5W F TC ₀ +/-100 | 28480 | 0698-3405 |
| S1 | 3101-1513 | 1 | 1 | SWITCH-TOGGLE 3-POSITION 2 PC | 28480 | 3101-1513 |
| U1 | 1820-2466 | 7 | 1 | IC TIMER CMOS | 32293 | ICM75551PA |
| U2 | 1820-1658 | 8 | 1 | IC TIMER CMOS | 04713 | MC14541BCP |
| U3 | 1826-013A | 8 | 1 | IC COMPARTOR GP QUAD 14-DIP-P | 01295 | LM339N |
| U4 | 1826-0161 | 7 | 1 | IC OP AMP GP QUAD 14-DIP-P | 04713 | MLM324P |
| U5 | 1858-0061 | 3 | 1 | TRANSISTOR ARRAY 16-PIN PL3TC DIP | 13606 | ULN-2004A |
| U6 | 1826-0544 | 0 | 1 | V REF 8-DIP-C | 04713 | MC1403U |
| U7 | 1826-0346 | 0 | 1 | IC OP AMP GP DUAL 8-DIP-P | 27014 | LM358N |
| U8 | 1820-0668 | 7 | 1 | IC BFR TTL NON-INV HEX 1-INP | 01295 | 8N7407N |
| | | | | MISCELLANEOUS PARTS | | |
| | 0403-0289 | 3 | 1 | EXTR-PC RD RED POLYC .063-8D=THKNS | 28480 | 0403-0289 |
| | 0960-0565 | 8 | 1 | AUDIO INDICATOR | 28480 | 0960-0565 |
| | 1420-0266 | 3 | 3 | BATTERY | 28480 | 1420-0266 |
| | 1420-0267 | 4 | 3 | BATTERY | 28480 | 1420-0267 |
| | | | | 1420-0266 | | |
| | | | | 7.2v .45A-1R2 | MICD | |
| | | | | 1420-0267 | | |
| | | | | 7.2v .1A-1R2 | MICD | |

| REV | DESCRIPTION | DATE |
|-----|--|------|
| A | AS ISSUED | |
| B | PFW CKT CHANGES | |
| C | PRCR "BS", CIRCUIT CHG R15 WAS 13.3K(B-2020) | |



- NOTES:
1. ALL VALUES OF CAPACITANCE ARE IN MICROFARADS
 2. ALL VALUES OF RESISTANCE ARE IN OHMS
 3. CR8 & CR9 ARE SPECIAL OVER VOLTAGE TRANSIENT ABSORBERS



| | | | |
|---------------------------|--------|------------------|-------------|
| BATTERY BACK-UP 12013A | | HEWLETT-PACKARD | |
| NEXT ASSEMBLY | 12013A | PART NUMBER | 12013-60001 |
| FINISH | SCALE | - 12013-60001-51 | |

| | |
|-----------|------------|
| BACKPLANE | SECTION VI |
|-----------|------------|

6.1 INTRODUCTION

The L-series backplane provides a link between the L-Series Computer System processor, memory, interface cards and power supply.

In this document, the backplane will be viewed from two different aspects: physical and logical.

Physically, the backplane is merely a mother board for the processor, memory and interface cards. It is a printed circuit card, on which the traces carry the power, ground and interconnecting signals between all the cards in an L-Series Computer System. See figure 6-1 for the physical layouts of the one-by-five and two-by-five backplanes.

The logical backplane defines protocols for the communications between all cards in the system. The definition, function, and timing of the backplane signals, and the protocols for their interaction are all considered to be part of the logical backplane.

Thus, the physical backplane houses a set of communications channels, whereas the logical backplane defines protocols for that communication.

This section covers both aspects of the L-Series backplane, and is intended to provide all the information needed to design a hardware interface to the backplane and thereby successfully integrate a design of arbitrary function into the L-Series computer.

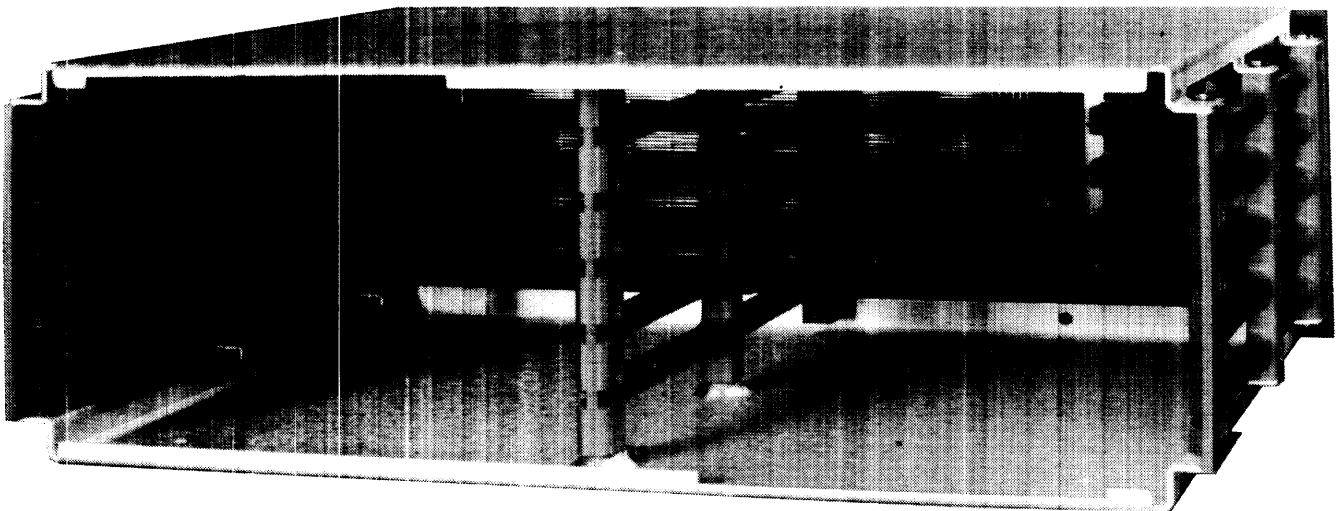
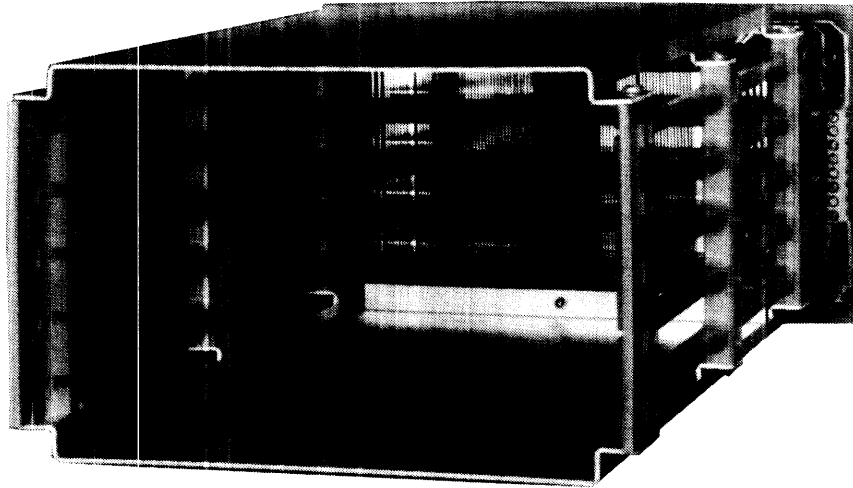


Figure 6-1. HP 1000 L-Series Backplanes

6.2 OVERVIEW

6.2.1 SYSTEM ENVIRONMENT OVERVIEW

An L-Series backplane (side view) is shown in figure 6-2 integrated into a system environment. Note that there are two types of connections to the backplane, labeled A and B. These are used as follows:

A. POWER SUPPLY CONNECTOR

A 24-pin socket which accepts control signals and voltages from the power supply.

B. CARD SLOTS

Each card plugs into a set of dual 50-pin sockets, for a total of 100 connections. These pins carry signals, power, and ground connections between the card and the backplane. The backplane shown in figure 6-2 has a total of 16 card slots.

Details on these interconnections are presented in paragraph 6.3, SPECIFICATIONS.

L-Series cards can be plugged into any backplane card slot subject to the following constraints.

- a. The battery backup card must go in a top slot to give the batteries adequate clearance.
- b. The memory card must go directly above the processor card.
- c. All I/O cards must go below the processor card.
- d. Any unused slot between two cards must be filled with a priority jumper card.

The terms "above" and "below" are not to be taken quite literally here. The term "above" refers to a higher priority slot and "below" refers to a lower priority slot. The backplane slots are numbered from XA1, the highest priority slot in order down to XAn, the nth highest priority slot. (See figure 6-3 for slot priority information.)

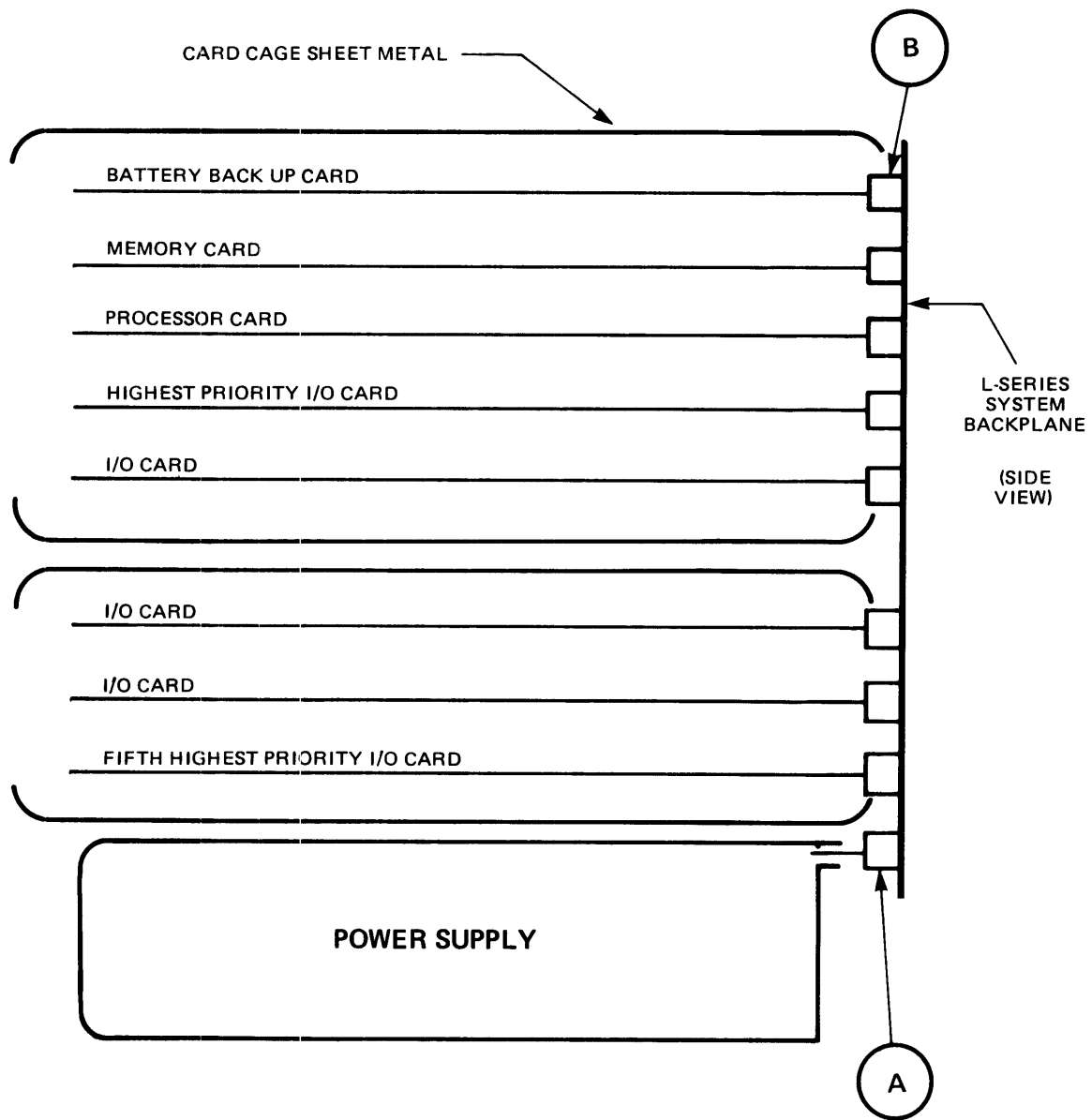


Figure 6-2. Backplane in Typical System Environment

6.2.2 INTERNAL SPECIFICATIONS OVERVIEW

The L-Series backplane is currently offered in three different configurations as shown in figures 6-3, 6-4, and 6-5.

The backplane in figure 6-3 is arranged in two stacks of eight slots, called a "2-by-8" configuration and is designed for the L-Series system. Figure 6-4 shows the "2-by-5" configuration which is designed for the 5-1/4 inch 2103L box. Figure 6-5 shows the "1-by-5" configuration which is designed for small controller type applications.

The three diodes on each backplane are on the +5V, +12V and -12V lines from the HP 12035A Power Supply. They are transient voltage suppressors, with a clamping action response of one picosecond, and the capability of handling a surge current of 50 amperes. They serve to protect the components on the cards plugged into the backplane from any power supply over-voltage or transient spike.

The physical backplane distinguishes between four types of traces.

- a. Bus line: This line is common to the same pin on each set of card sockets. Examples are WE- and CRS-.
- b. Power Supply line: This line comes from the power supply and runs to the same pin on each set of card sockets. Examples are PFW and PON+.
- c. Ground and Voltage lines: This line comes from the power supply and typically has two or more pin assignments on each set of card sockets. Grounds and voltages are typically carried on much wider traces than other signals. Examples are +5V and +12V.
- d. Chained lines: This is a set of lines which connect every pair of adjacent card sockets. Each of these lines is common to exactly two sockets. Examples are ICHID-, ICHOD-, SCHID-, and SCHOD-.

The distinction between these four types of lines is important when determining backplane compatibility.

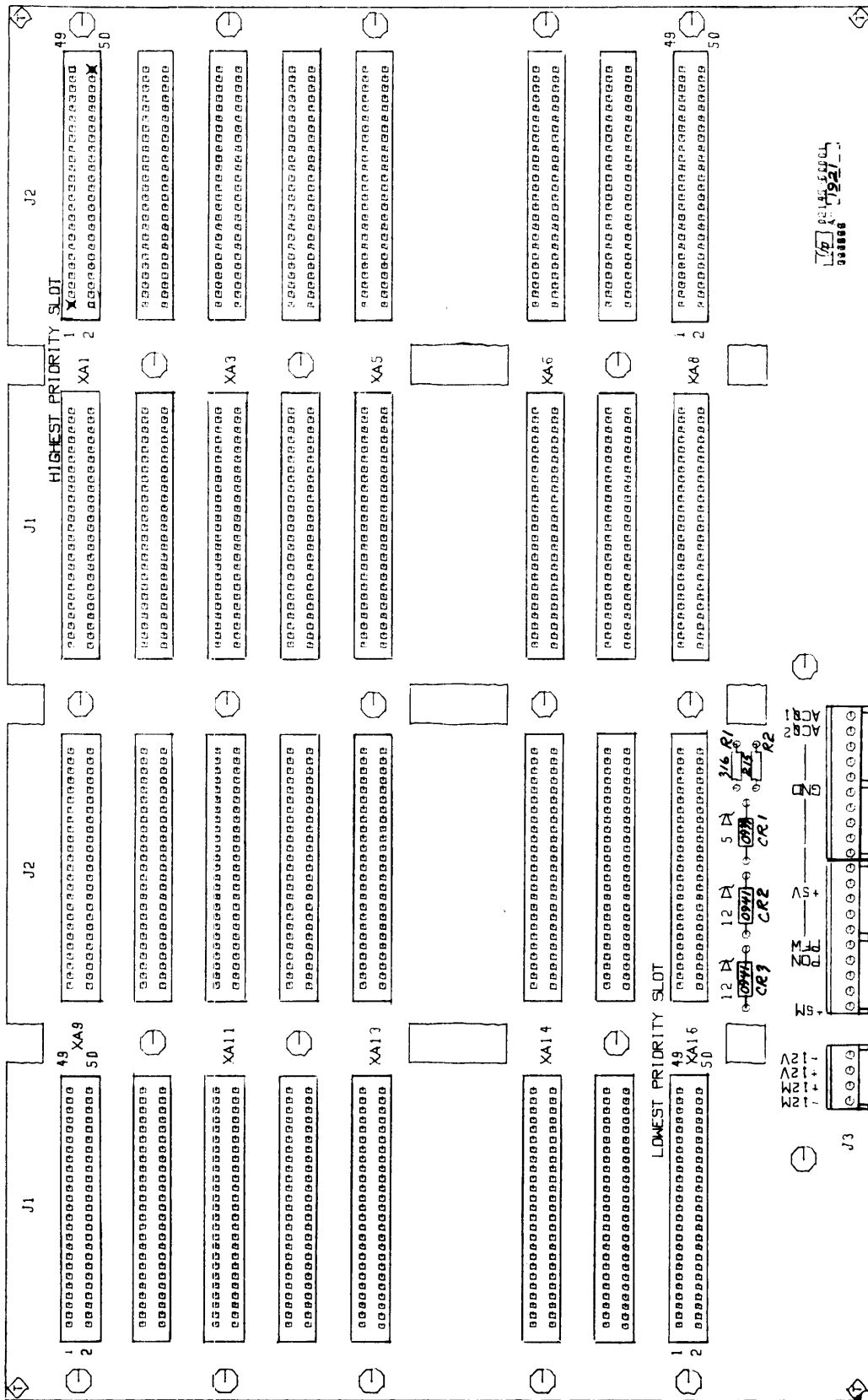
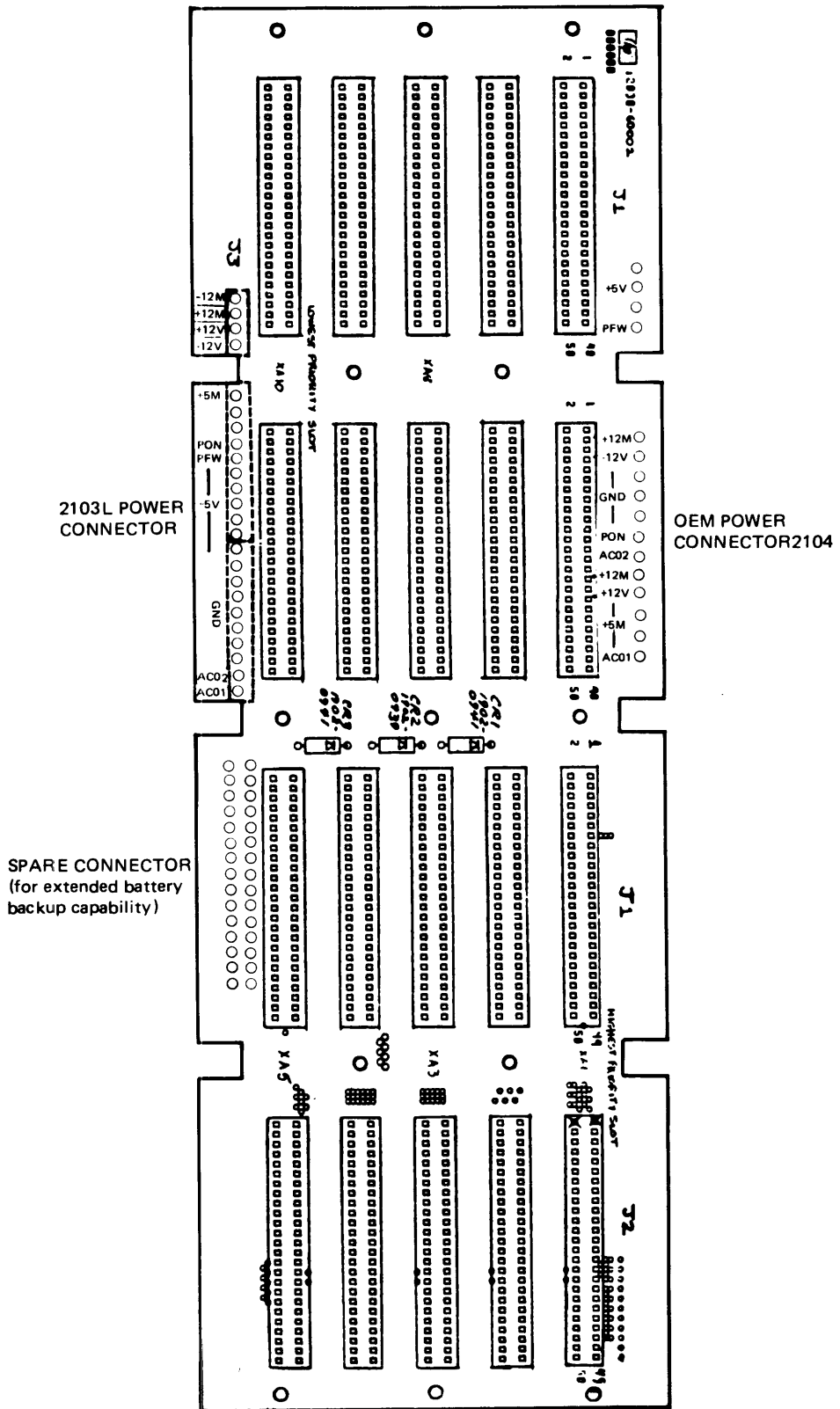
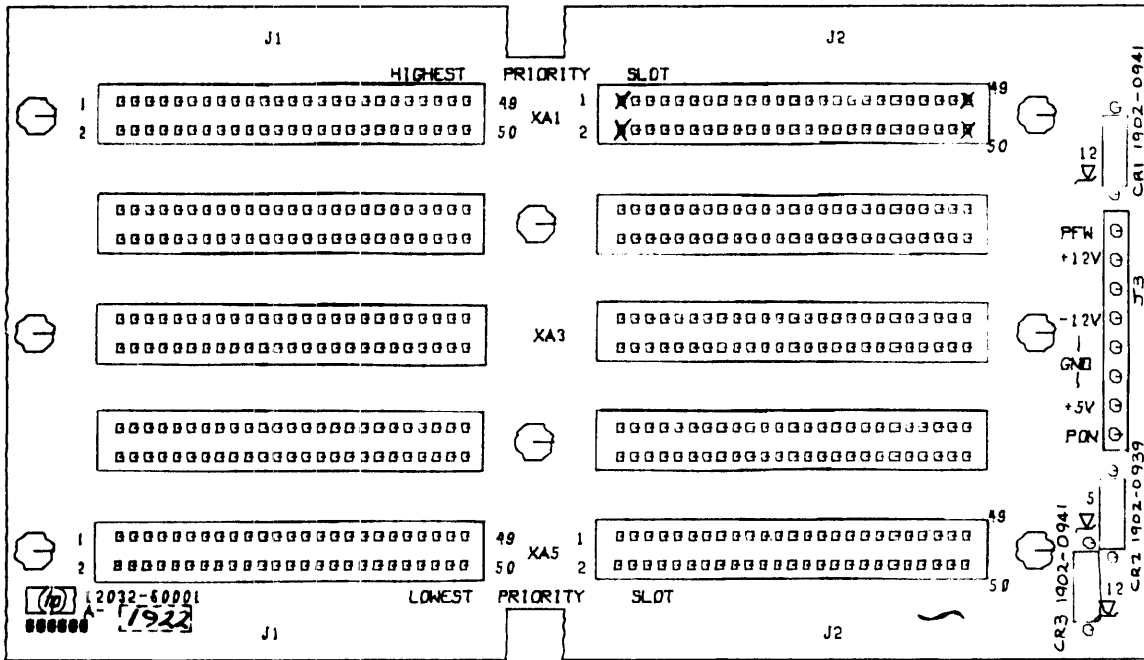


Figure 6-3. Two-by-Eight Backplane



7700-562-1

Figure 6-4. Two-by-Five Backplane



COMPONENT SIDE INK GRAPHICS

Figure 6-5. One-by-Five Backplane

6.2.3 BACKPLANE INTERFACE HARDWARE

All backplane interface hardware can be broken down into four categories as listed below. It may be helpful to become familiar with one or more of these categories.

6.2.3.1 Processor Interface

This interface is responsible for generating all backplane clocks, and, in addition, such signals as RNI (Read Next Instruction) and IAK (Interrupt Acknowledge). The processor interface information is presented in Section II of this document.

6.2.3.2 Memory Interface

This interface is responsible for generating such signals as PE (memory Parity Error) and VALID (data bus Valid). The memory interface information is presented in Section III.

6.2.3.3 I/O Master Interface

The I/O Master interface consists of an IOP chip and its support logic. This circuitry is located on every L-series I/O card and serves to standardize the I/O interface to the backplane by performing all the functions (I/O instruction recognition and execution, interrupt processing, DMA control) common to all I/O cards.

6.2.3.4 Passive Interfaces

Passive interfaces include those that supply, monitor or use power lines, or monitor signals without ever generating signals or interacting on the backplane. These interfaces include the L-series Interface for Logic Analyzers and the Battery Backup card.

6.3 SPECIFICATIONS

6.3.1 GENERAL HARDWARE SPECIFICATIONS

The 2 by 5 and 2 by 8 backplanes use a six-layer printed circuit card. One +5V plane and a ground plane minimize signal crosstalk and permit the traces to maintain a consistent characteristic impedance throughout their length. Most of the logic used to drive the backplane signals is Schottky TTL, and because of the high switching speeds characteristic of this logic family, good noise immunity is necessary for the backplane.

The use of the four remaining layers is roughly as follows: One layer is used for the set of signals running vertically between the five slots in each stack; two are used for the set of signals running horizontally to connect the stacks; and the last layer is used for the miscellaneous voltages. This layout provides all the signal traces with a steady characteristic impedance of 47 to 51 ohms. This provides a good match with the output impedances of the backplane drivers, which are in the range of 25 to 100 ohms. That is, all impedances are matched within a 2 to 1 ratio.

The 1 by 5 backplane uses a two-layer printed circuit card. The complexity of this physical backplane is reduced considerably because the two layers used to interconnect the two stacks in the 2 by 5 configuration are eliminated in the 1 by 5 configuration. Due to the maximum trace length of 3.2 inches on this backplane, no noise problems are encountered.

6.3.2 POWER SUPPLY INTERCONNECT

A 24-pin connector is used to connect to the power supply for the 2 by 5 and 2 by 8 configurations. The female connector is soldered along the bottom of the backplane. The male connector is rigidly attached to the power supply module in such a manner that it plugs in as the power supply module is slid into place. The connectors are rated at 7 amperes/pin. Pin assignments for the power supply connector are as shown in table 6-1.

The paths on the backplane extending from the power supply connector carry relatively high currents, and therefore must be as broad as possible. Ground and +5V, the most used levels, are transferred over whole planes. Other voltages are carried on traces as much as 200 mils wide. The width of each trace was selected so that it could withstand relatively large current surges without much voltage fluctuation (inductance is the key parameter here) and so that it would experience a temperature rise of less than 10 degrees C at the maximum current rating of the power supply.

Table 6-1. Power Supply Connector Pin Assignments

| PIN NUMBER | SIGNAL NAME |
|------------|---------------------------------|
| 1 | -12V MEMORY VOLTAGE SENSE |
| 2 | +12V MEMORY VOLTAGE SENSE |
| 3 | +12V LOGIC (4A MAX) |
| 4 | -12V LOGIC (2A MAX) |
| 5 | +5V MEMORY VOLTAGE SENSE |
| 6 | NOT USED |
| 7 | NOT USED |
| 8 | POWER ON (PON) SIGNAL |
| 9 | POWER FAIL WARNING (PFW) SIGNAL |
| 10 | } +5V LOGIC (30A) |
| 11 | |
| 12 | |
| 13 | |
| 14 | |
| 15 | } DC COMMON, 25kHz COMMON |
| 16 | |
| 17 | |
| 18 | |
| 19 | |
| 20 | |
| 21 | |
| 22 | |
| 23 | 25kHz PHASE 2, 14VRMS (TO GND) |
| 24 | 25kHz PHASE 1, 14VRMS (TO GND) |

6.3.3 CARD SOCKET INTERCONNECTS

Each card in the L-Series has two 50-pin tongues, P1 and P2, which plug into a set of 50 pin sockets on the backplane, J1 and J2 respectively. The card cage is constructed with card guides, in such a manner that the cards will slide in and then snap into place in the backplane connectors. The cards must be inserted component side up as shown in figure 6-6. The odd numbered fingers will then be on the top, and the even numbered ones on the bottom. The pin assignments for these 100 connections are given in figure 6-7. For signal definitions, see table 6-37.

6.3.4 BACKPLANE LOADING RULES

Backplane loading rules were established in order to provide guidelines for the selection of bus drivers and backplane signal drivers, and in order to insure that these drivers are not overloaded. These rules take into account the drive capabilities and loading of certain industry standard parts such as the S and LS 240 and 241. Because there may be a maximum of 18 I/O interface cards in any given system, each card must adhere strictly to the rules in order to prevent possible overloading. These loading rules were established assuming a maximum of 20 cards in a system. Note that the I/O Master is designed such that all backplane lines except the data bus are buffered and cannot be used in the unbuffered form by I/O interface logic external to the I/O Master.

6.3.4.1 DC Loading

DC loading rules are made to insure that a device driving any given backplane line can handle sufficient current to keep all the inputs connected to that line at the required voltage level. Low state load on a given line is the sum of I_{IL} maximum for all receivers plus I_{OZL} for all tri-state drivers. High state load is the sum of I_{IH} for all receivers plus I_{OZH} for all tri-state drivers.

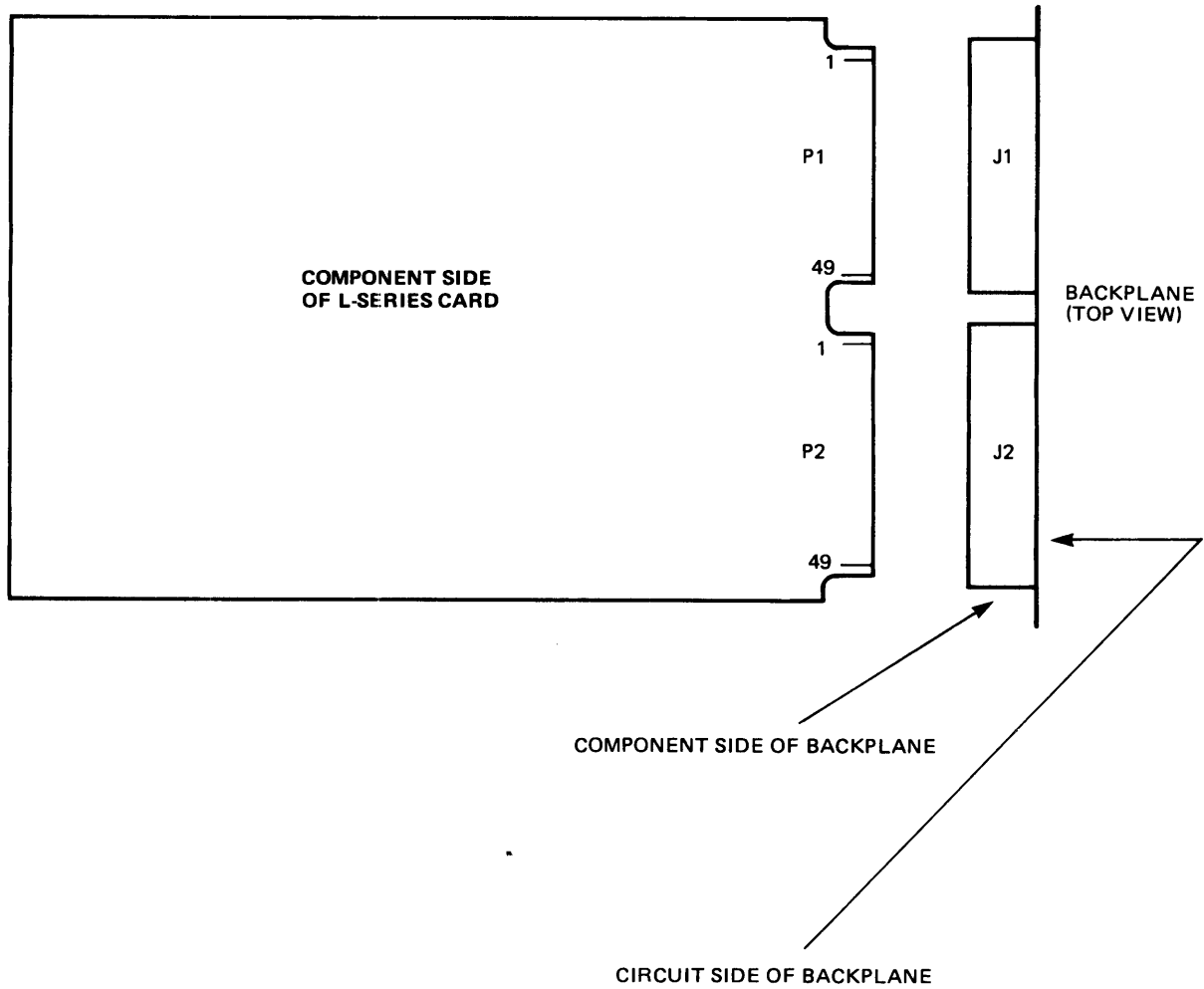


Figure 6-6. Card Socket Interconnects

| J1 | | | | J2 | | | |
|----|----------|----------|----|----|-----------|----------|----|
| 1 | * ICHID- | ICHOD- | 2 | 1 | CPUTURN- | ISOGND | 2 |
| 3 | **MCHID- | MCHOD- | 4 | 3 | REMEM- | VALID- | 4 |
| 5 | MLOST- | MCHODOC- | 6 | 5 | IORQ- | INTRQ- | 6 |
| 7 | PFW- | SPARE 1 | 8 | 7 | MP+ | RNI- | 8 |
| 9 | SC0+ | SC1+ | 10 | 9 | MEMGO- | PE- | 10 |
| 11 | SC2+ | SC3+ | 12 | 11 | ***SCHID- | SCHOD- | 12 |
| 13 | GND | GND | 14 | 13 | IAK- | IOGO- | 14 |
| 15 | COTURN- | GND | 16 | 15 | ISOGND | SLAVE- | 16 |
| 17 | SC4+ | SC5+ | 18 | 17 | ISOGND | MRQ- | 18 |
| 19 | AB0+ | AB1+ | 20 | 19 | ISOGND | FCLK- | 20 |
| 21 | AB2+ | AB3+ | 22 | 21 | ISOGND | CCLK- | 22 |
| 23 | AB4+ | AB5+ | 24 | 23 | SPRQ- | SCLK- | 24 |
| 25 | AB6+ | AB7+ | 26 | 25 | CRS- | PON+ | 26 |
| 27 | AB8+ | AB9+ | 28 | 27 | ISOGND | BUSY- | 28 |
| 29 | AB10+ | AB11+ | 30 | 29 | GND | GND | 30 |
| 31 | AB12+ | AB13+ | 32 | 31 | GND | GND | 32 |
| 33 | AB14+ | WE- | 34 | 33 | GND | GND | 34 |
| 35 | DB0+ | DB1+ | 36 | 35 | +5V | +5V | 36 |
| 37 | DB2+ | DB3+ | 38 | 37 | +5V | +5V | 38 |
| 39 | DB4+ | DB5+ | 40 | 39 | +12M | -12M | 40 |
| 41 | DB6+ | DB7+ | 42 | 41 | +12V | +12V | 42 |
| 43 | DB8+ | DB9+ | 44 | 43 | -12V | -12V | 44 |
| 45 | DB10+ | DB11+ | 46 | 45 | +5M | +5M | 46 |
| 47 | DB12+ | DB13+ | 48 | 47 | 25kHz 02 | 25kHz 02 | 48 |
| 49 | DB14+ | DB15+ | 50 | 49 | 25kHz 01 | 25kHz 01 | 50 |

* - Above the processor card, this signal is called PS-.
 ** - Above the processor card, this signal is called RCLK+.
 *** - Above the processor card, this signal is called MEMDIS-.

Figure 6-7. Card Slot Pinouts

6.3.4.2 Actual Worst Case Loading

Actual worst case loading for the address bus, select code bus 0-4, and the data bus is as follows:

ADDRESS BUS, AND SELECT CODE BUS 0 - 4:

| | Low State Load | High State Load |
|-----------------------|----------------|-----------------|
| 64Kbyte dynamic RAM | .4mA | 20uA |
| L-series Processor | 1.7mA | 150uA |
| I/O Master (times 18) | 7.2mA | 360uA |
| | ----- | ----- |
| TOTAL | 9.3mA | 530uA |

DATA BUS:

| | Low State Load | High State Load |
|-----------------------|----------------|-----------------|
| 64Kbyte dynamic RAM | 2.5mA | 150uA |
| L-series Processor | 3.4mA | 280uA |
| I/O Master (times 18) | 17.5mA | 1800uA |
| | ----- | ----- |
| TOTAL | 23.4mA | 2.23mA |

The design rules and guidelines are shown in table 6-2.

Table 6-2. Design Rules/Guidelines

| ! Design Rules/Guidelines | !Address Bus, !SC Bus 0-4 | ! Data Bus | ! All Other ! Bussed ! Lines | ! Chained ! Lines |
|--|------------------------------|------------|------------------------------------|----------------------|
| ! Maximum allowable load ! per card - high state | ! 130uA | ! 250uA | ! 60uA | ! 400uA |
| ! Maximum allowable load ! per card - low state | ! 1.2mA | ! 1.2mA | ! 1mA | ! 10mA |
| ! Minimum allowable drive ! capability - high state | ! 2.6mA | ! 5.0mA | ! 1.2mA | ! 1mA |
| ! Minimum allowable drive ! capability - low state | ! 24mA | ! 24mA | ! 20mA | ! 20mA |

6.3.4.3 AC Loading

Every connection made to any given line places a capacitive load on that line due to PC board trace capacitance and due to the integrated circuit input or output capacitance. Care must be taken to insure that any given line is not capacitively overloaded as this results in slowing its switching speed down below a tolerable point. Typical delays are in the range of 2ns/50pF for a line driven by an LS240/241 and 4ns/50pF for an LS373/374.

The AC loading specifications, as with the DC loading rules, should be strictly adhered to for the I/O interfaces, but can be used merely as guidelines for processor and memory cards. Signal timing calculations are made considering actual worst case loads as shown in table 6-3. Again, a 20-slot system is assumed.

6.3.4.4 Data Bus

Each card may not exceed 60pF load per line.

6.3.4.5 All Other Lines

Each card may not exceed 25pF load per line.

6.4 INTERFACE REQUIREMENTS

The following paragraphs deal exclusively with the logical backplane. The protocols and conventions used by all L-Series cards to interact over the backplane are classified and described. An important feature of the L-Series computer is its distributed intelligence. Every interface card in the system has the capability of handling its own memory accesses (DMA), of decoding its own instructions, and of forcing the central processor into slave mode processing. Each of these three capabilities and the protocols with which they are implemented are described. You may find it helpful, while working through each handshake protocol, to refer to the glossary of signal definitions in table 6-37.

Table 6-3. Capacitance Data on 20-Slot System

| PIN | SIGNAL | C IN pF L |
|--------------------|--------------|--------------|
| J1 - 1,2 | ICHID, ICHOD | 40 |
| J1 - 3,4 | MCHID, MCHOD | 25 |
| J1 - 5 | MLOST | 200 |
| J1 - 6 | MCHODOC | 850 |
| J1 - 7 | PFW | 200 |
| J1 - 9,10,11,12,17 | SC0 - SC4 | 400 |
| J1 - 18 | SC5 | 900 |
| J1 - 19,20,...,34 | ADDRESS BUS | 500 |
| J1 - 35,36,...,50 | DATA BUS | 1300 |
| J2 - 1 | CPUTURN | 400 |
| J2 - 3 | REMEM | 600 |
| J2 - 4 | VALID | 550 |
| J2 - 5 | IORQ | 580 |
| J2 - 6 | INTRQ | 650 |
| J2 - 7 | MP | 500 |
| J2 - 8 | RNI | 500 |
| J2 - 9 | MEMGO | 550 |
| J2 - 10 | PE | 500 |
| J2 - 11,12 | SCHID, SCHOD | 30 |
| J2 - 13 | IAK | 500 |
| J2 - 14 | IOGO | 500 |
| J2 - 16 | SLAVE | 740 |
| J2 - 18 | MRQ | 550 |
| J2 - 20 | FCLK | 500 |
| J2 - 22 | CCLK | 620 |
| J2 - 23 | SPRQ | 250 |
| J2 - 24 | SCLK | 500 |
| J2 - 25 | CRS | 500 |
| J2 - 26 | PON | 550 |
| J2 - 28 | BUSY | 400 |

NOTE: All capacitances shown are worst case figures.

6.4.1 MEMORY ACCESS PROTOCOL

Every card that accesses memory uses the same handshake protocol. This approach greatly simplifies the operation of multichannel DMA. The DMA feature of every L-Series I/O interface allows input or output operations to proceed without processor intervention, significantly easing the processing requirements on the CPU. The processor is the lowest-priority DMA device because if any other card pulls on the open-collector line MRQ (Memory Request), the processor is held off from doing a memory cycle. The processor may be locked out entirely for up to 72 usec by high speed interfaces using adjacent memory cycles. In order to prevent being locked out entirely, the processor can assert the CPUTURN- signal which informs the interface cards not to reassert MRQ after their current memory request is satisfied. For more information on CPUTURN-, refer to the definition in table 6-37.

A priority scheme is used in the L-Series to resolve contention between interfaces wanting memory cycles. An interface wanting a memory cycle will assert MRQ-, MCHOD-, and MCHODOC-. The first signal, MRQ-, will disable the processor from taking the next memory cycle. MCHOD- is part of a priority chain which will ripple down, disabling all lower-priority interfaces. MCHODOC- is a look-ahead on this chain. It is used as the top of the chain for the stack of lowest-priority slots. Although MRQ- may be asserted by one or more interfaces at any given time, MEMGO- may only be asserted by the one interface that gets the memory cycle. An interface determines if it is entitled to a memory cycle (to assert MEMGO-) by monitoring certain backplane signals. It can initiate a memory cycle on any falling edge of SCLK- when BUSY- is high, its MCHID- is high, and its MRQ- has been asserted for at least one cycle. This stipulation means that contention among I/O cards for memory always has one cycle of SCLK in which to be resolved, namely, the cycle which occurs just before the assertion of MEMGO-.

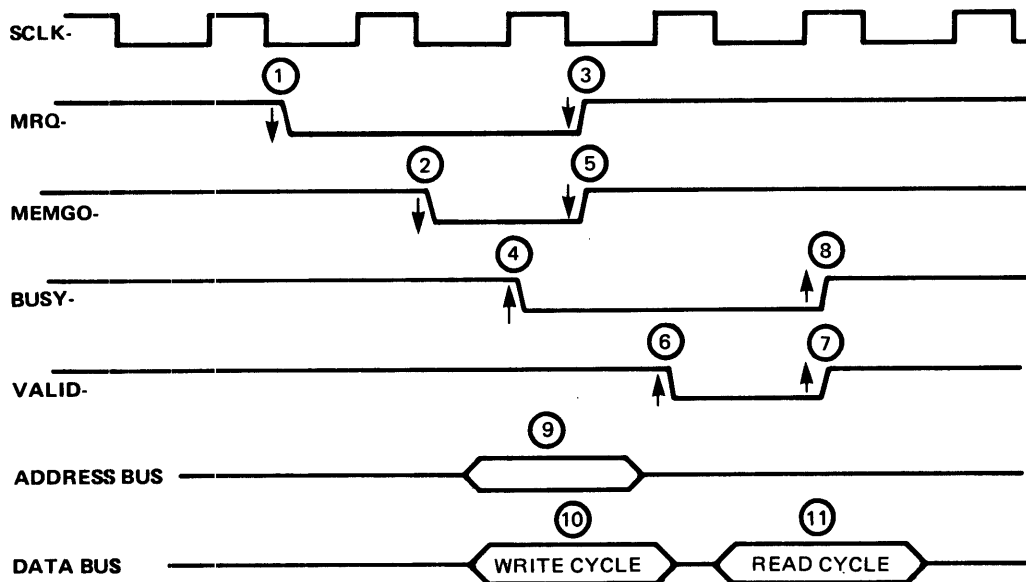
The processor card begins its access to memory by asserting MEMGO $\bar{}$ on the falling edge of SCLK $\bar{}$. If an I/O interface card desiring a DMA transfer asserts MRQ $\bar{}$ on that same edge, the processor card must immediately relinquish its claim to accessing memory by releasing MEMGO $\bar{}$ prior to the next rising edge of SCLK $\bar{}$. Therefore, contention between the processor and any I/O interface for memory is resolved during the long half cycle between the falling and rising edges of SCLK $\bar{}$. MEMGO $\bar{}$ will be asserted at the completion of all current DMA requests. Refer to table 6-18 for the aborted MEMGO $\bar{}$ timing specifications.

6.4.2 MEMORY HANDSHAKE TIMING

Memory handshake timing is shown in figure 6-8.

6.4.3 INTERRUPT PROTOCOL

The L-series interrupt system is identical in function to that of its predecessor 2100-series computers, with a multi-level vectored system. In the L-Series, interrupt priority is determined by physical proximity to the processor on the interrupt priority chain only, similar to the 2100-series convention. There is a difference, however; in the 2100-series, the physical slot location determines a device's select code (and hence its interrupt vector address), whereas in the L-Series the select code is independent of a card's physical location. The select code is determined by setting six switches, one per select code bit, on each I/O interface.



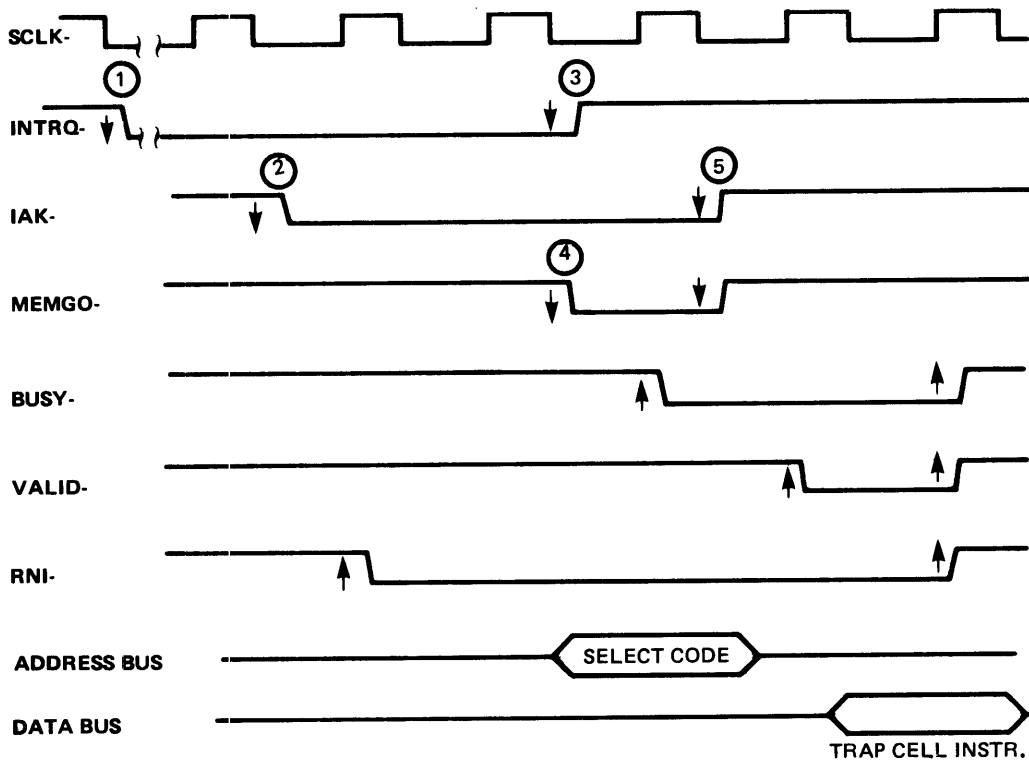
1. An interface card asserts MRQ- to request a memory cycle. (MCHOD- and MCHODOC- are asserted simultaneously to hold off all lower priority cards).
2. An interface card asserts MEMGO-, if one cycle after the assertion of MRQ-, it still has priority; i.e., its MCHID- is high. If MRQ- is not asserted, the MEMGO- is from the processor card, or an interface card during an interrupt cycle.
3. An interface card releases MRQ- at the end of the short half cycle when MEMGO- is released.
4. The memory asserts BUSY-, once MEMGO- has been asserted, in order to hold off other memory cycles until this cycle can be completed.
5. MEMGO- is released one cycle after being asserted.
6. The memory asserts VALID- during the last cycle of BUSY-.
7. The release of VALID- signals that data is valid on backplane.
8. The release of BUSY- signals that a new memory cycle can begin.
9. The address bus is driven by the interface card during the assertion of MEMGO-.
10. In the case of a memory write cycle, the interface data is valid on the backplane shortly after the address bus.
11. In the case of a memory read cycle, the memory guarantees valid data on the rising edge of VALID-.

Figure 6-8. Memory Handshake Timing

An interrupt request occurs when a card's CONTROL flip-flop is set and the FLAG flip-flop gets set by either the interface itself or the execution of an STF instruction. This will cause the interface to assert the interrupt-requesting signal INTRQ- on the backplane. INTRQ- is a common signal (open collector, wired-OR) used by all interfaces to notify the processor that any one of the interfaces would like an interrupt. An interrupt acknowledgement, IAK-, from the processor card, is triggered by an interrupt request from any of the I/O interfaces. When the CPU chip reaches the state where it is ready to fetch the next instruction, and if the interrupt system is enabled and interrupts are not temporarily being held off, then the processor will assert IAK-.

Because interrupt servicing is accomplished with the help of a memory cycle, the handshake in figure 6-9 is similar to that in figure 6-8. Since it is transparent to the memory whether or not an interrupt is being serviced, BUSY- and VALID- have exactly the same function in the two timing diagrams. MEMGO- has the same function as in a normal memory cycle except that during its assertion, the address bus is driven with the interface card's select code. The data which is read from this location in memory is used as the next instruction executed by the processor. This instruction will normally be a jump (JSB, I) to the location of some interrupt service routine. When an interface card asserts INTRQ-, it also pulls on ICHOD-. ICHOD- will disable all lower-priority cards from requesting interrupt service. If a high-priority card preempts the request, ICHID- will go low, disabling the requesting card. The lower-priority card should maintain its request until its ICHID- goes back up and the card can be serviced.

If any contention exists between an IAK- assertion and an MRQ- assertion, the DMA request will win. Both IAK- and MRQ- assertions may occur simultaneously on the falling edge of SCLK-, but IAK- will be deasserted prior to the next rising edge of SCLK-. The assertion of IAK will be permitted at the completion of all current DMA requests. Refer to table 6-11 for the aborted IAK- timing specifications.



1. An interface card pulls on INTRQ- to request interrupt service.
2. When the processor has reached the appropriate state and if the interrupt system is enabled, and interrupts are not temporarily being held off, then it will acknowledge the interrupt request by asserting IAK-.
3. As soon as the interface card asserts MEMGO, it knows its interrupt will be serviced so it releases INTRQ-.
4. The interface card asserts MEMGO- to initiate a memory cycle, and during the one cycle of SCLK it holds MEMGO- low, it drives the lower 6 bits of the address bus with its select code, and the upper 9 bits with zeros.
5. The processor releases IAK- upon the assertion of BUSY-.

Figure 6-9. Interrupt Timing

6.4.4 INTERRUPT LATENCY

For this discussion, interrupt latency is defined as the time from the user's interrupt request to the assertion of IAK by the processor. In the best case, the interrupt can be serviced as soon as it is received, which with a 227 SCLK is 880 nsec. Generally, the interrupt cannot be serviced until a DMA cycle completes or until an instruction has finished executing. In addition, interrupts are temporarily held off for one instruction time after a JMP,I, JSB,I, or I/O instruction is executed. Therefore, worst case interrupt latency is highly dependent on the software which is running at the time of the interrupt. Assuming no more than three channels of DMA self-configure at once, and no more than three adjacent instructions that hold off interrupts are executed back-to-back, the maximum interrupt latency is 830 usec.

| MINIMUM | TYPICAL | MAXIMUM |
|-----------|----------|----------|
| ----- | ----- | ----- |
| 0.88 usec | 1.6 usec | 830 usec |

6.4.5 REMOTE MEMORY ACCESS

All I/O interface cards have the capability of accessing a remote memory (i.e., a memory other than that plugged into the backplane directly above the processor card). In order to access the remote memory, an interface card must assert REMEM- with MEMGO-. The assertion of REMEM- will signal the local memory to ignore MEMGO-. Instead, a cycle with the remote memory will be initiated. This function is reserved for use by future processors. It is not currently used in the L-Series.

6.4.6 EXPANDED MEMORY ACCESS

To facilitate DMA access to expanded memory, each L-Series I/O card has been designed with a 5-bit Address Extension Bus (SC0-4) that is driven onto the backplane simultaneously with the address bus during a memory access.

6.4.7 I/O TRANSFER PROTOCOL

The L-Series I/O structure is such that I/O instructions are not executed by the CPU; instead, they are decoded by the interface card to which they apply, then executed by that interface card in conjunction with the CPU. The instruction decoding and executing capability of the interface card is provided by a Silicon-On-Sapphire (SOS) chip, the IOP chip, located on each interface card. The I/O handshake uses the two signals IORQ-, I/O request by an interface card, and IOGO-, go ahead signal from the processor card.

The processor card's IOGO- may be preempted by concurrent DMA activity. Both IOGO- and MRQ- are asserted on the falling edge of SCLK-; thus the processor may come into contention with an I/O interface card if both signals occur simultaneously. The DMA activity has higher priority than the processor so that IOGO- must be deasserted prior to the next rising edge of SCLK-. When all concurrent DMA has completed, then IOGO- may be asserted on the backplane to complete the I/O handshake. Figure 6-10 illustrates a normal I/O handshake. For more information on a preempted I/O handshake and aborted IOGO-, refer to the timing specifications in table 6-14.

6.4.8 I/O INSTRUCTION EXECUTION

The I/O instructions may be broken down into three groups in terms of their execution requirements, as follows:

A. Data Transfer I/O instructions - OTA/B, LIA/B, MIA/B

This group requires a double handshake as shown in figure 6-10. In the first half of the handshake, a control word is transferred from the interface card to the processor card. In the second half of the handshake, the data is transferred either into or out of the A or B register, according to which of the six instructions above is being executed. I/O transfers over the backplane have lower priority than DMA transfers, and can be preempted. DMA transfers can occur while an I/O instruction is in the process of being executed, i.e., between the two halves of the handshake.

B. Status Sensing Instructions - SFS, SFC

This group requires, at most, a single handshake during which a control word from the interface card to the processor (signaling the program counter) is transferred. If no skip is required, no handshake occurs.

C. Status Altering Instructions - STC, CLC, STF, CLF

This group requires no interaction with the CPU. The interface card executes these instructions itself, and never needs to assert IORQ-.

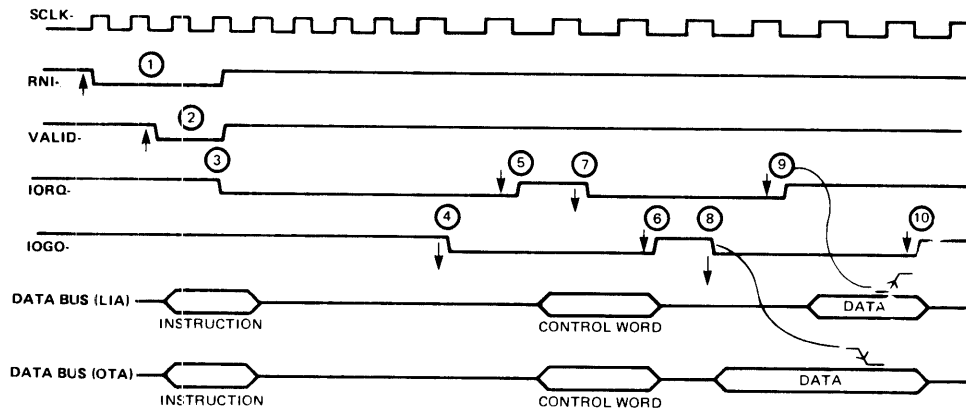
6.4.9 SLAVE MODE TRANSFERS

An interface card may force the processor card to enter an I/O handshake by pulling down the open-collector line SLAVE-. Once in slave mode, the interface has the capability of accessing the internal CPU registers, and does so with the use of the same handshake signals as in the I/O transfer protocol as illustrated in figure 6-11. Once the slave mode has been entered, an interface card may keep the processor in that mode as long as desired by setting a bit in the control word (transferred during the first half of the handshake) which signals that another double handshake will occur. Note that the slave chain (SCHID-, SCHOD-) operates differently from the other chains in that its quiescent state is low or disabled. It is enabled only for one cycle at a time, during which the highest priority interface card pulling on SLAVE- must assert IORQ-, thereby entering slave mode. See figure 6-11 for slave mode operation.

The control words which are sent to the CPU by an interface card during an I/O instruction (requiring a handshake), and during all slave mode processing are made up of five bits using bits 8 through 4 of the data bus. These control words are defined below:

| | Data Bus Bit | | | | |
|---------------------------|--------------|---|---|---|---|
| | 8* | 7 | 6 | 5 | 4 |
| NOP | X | 0 | 0 | 0 | 0 |
| Load Program Counter | X | 0 | 0 | 0 | 1 |
| Load A | X | 0 | 0 | 1 | 0 |
| Load B | X | 0 | 0 | 1 | 1 |
| Clear O | X | 0 | 1 | 0 | 0 |
| Set O | X | 0 | 1 | 0 | 1 |
| OR into A/B | X | 0 | 1 | 1 | 0 |
| Increment Program Counter | X | 0 | 1 | 1 | 1 |
| Read E and O | X | 1 | 0 | 0 | 0 |
| Enable ROMs | X | 1 | 0 | 0 | 1 |
| Read A | X | 1 | 0 | 1 | 0 |
| Read B | X | 1 | 0 | 1 | 1 |
| Clear E | X | 1 | 1 | 0 | 0 |
| Set E | X | 1 | 1 | 0 | 1 |
| Read P | X | 1 | 1 | 1 | 0 |
| Read and Increment P | X | 1 | 1 | 1 | 1 |

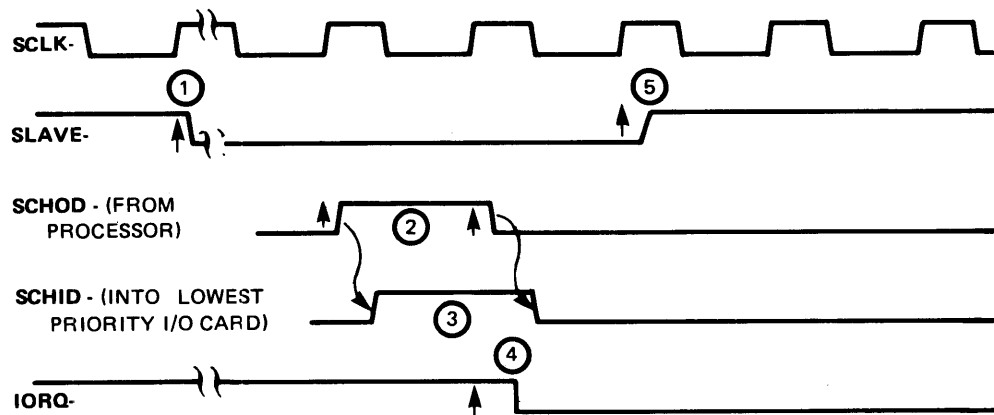
* Loop for next control word if X=1; last handshake if X=0.



7700 564

1. Processor asserts RNI- to inform all system cards that an instruction is being fetched from memory.
2. Memory asserts VALID- to inform all system cards that data on the backplane will soon be valid. Each interface should now latch the instruction off the data bus, and decode it to see if it is an I/O instruction to its select code.
3. An interface card pulls on IORQ- to signal that it recognized the I/O instruction and needs the CPU in order to execute it.
4. The processor asserts IOGO- to indicate that it is ready to receive a command from the interface card.
5. The interface card releases IORQ- to signal the processor that the control word will be available on the data bus on the second rising edge of SCLK-.
6. The processor releases IOGO- when it has clocked the command off the backplane.
7. The interface card reasserts IORQ- one cycle after it was released if another handshake is needed in order to transfer a data word.
8. The processor reasserts IOGO- in order to indicate that it is ready to receive an operand in the case of an input operation, or that data will be valid on next falling edge in the case of an output operation.
9. The interface card releases IORQ- to indicate that it has latched an operand off the backplane in the case of an output operation, or that an operand will be valid on the backplane on second rising edge in the case of an input operation.
10. The processor releases IOGO- to indicate that it has clocked data off the backplane in the case of an input operation, or that the handshake is complete in the case of an output operation.

Figure 6-10. I/O Handshake



1. An interface card asserts SLAVE- to request the processor to enter slave mode.
2. When the processor has completed executing the current instruction, it acknowledges the assertion of SLAVE- by de-asserting SCHOD- for one cycle.
3. Worse case, the SCHID/SCHOD priority chain has propagated down to the lowest-priority interface card by the end of that cycle, so that the last SCHID- will go high for one cycle.
4. The interface card received the enabling signal when its SCHID- signal went high, and can now pull on IORQ- in order to initiate the I/O handshake. The rest of the I/O handshake can then proceed exactly as shown in figure 6-10.
5. The interface card de-asserts SLAVE- once it has asserted IORQ-.

Figure 6-11. Slave Mode Timing

6.5 SIGNAL TIMING SPECIFICATIONS

The L-Series cards can be categorized into four types for backplane timing: memory, processor, analysis interface, and I/O Master. Each of these four types of cards has its timing requirements for the signals it receives and its timing guarantees for the signals it generates. In order to insure the basic integrity of all backplane interactions, it is necessary only to ascertain that all requirements are satisfied by the guarantees. All timing guarantees take into account the signal propagation delay due to line length and loading.

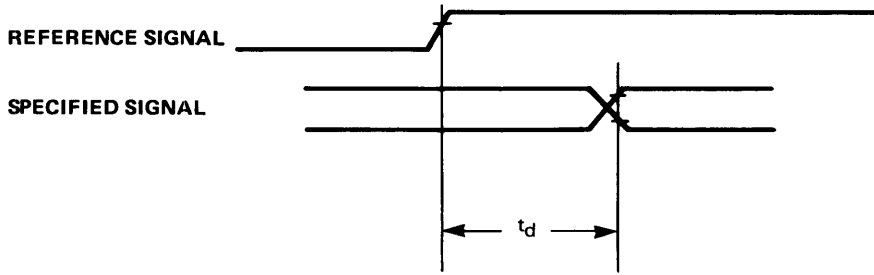
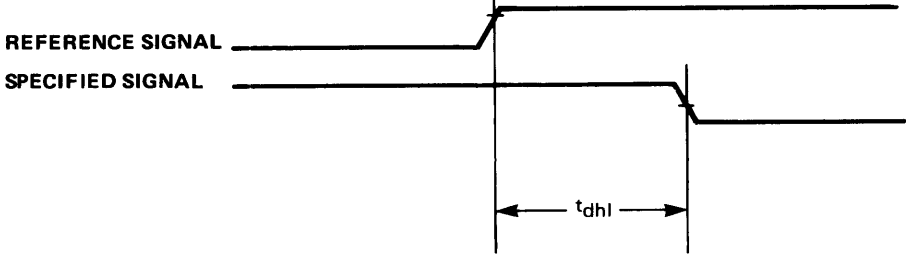
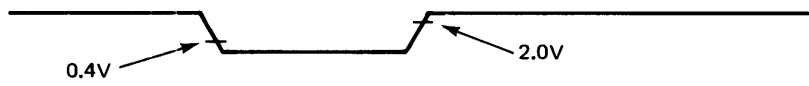
In tables 6-4 through 6-36, timing specifications are given in terms of both requirements and guarantees. All backplane signals are listed in alphabetical order.

Please make note of the following abbreviations which are used. All times are given in nanoseconds unless otherwise indicated.

DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS

| | |
|-----|--|
| AI | - Analysis Interface 10285A Interface between the L-Series computer and a logic analyzer. |
| BB | - Battery Backup The L-series Battery Back-Up Card (part number 12013-60001). |
| C | - Cycle One cycle of Slow Clock (SCLK). |
| f | - Frequency The number of cycles per unit time of a given signal. |
| I/O | - I/O Master The L-series I/O Master consists of an SOS IOP chip and some TTL logic which together performs all the backplane I/O interfacing functions in the L-Series computer. |
| LHC | - Long Half Cycle The Long Half Cycle refers to the time period when SCLK- is low. |
| M | - Memory The L-series 64Kbyte dynamic RAM card (12004A). |
| P | - Processor The 12001A processor card with SOS central processor unit (CPU) chip. |

DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS

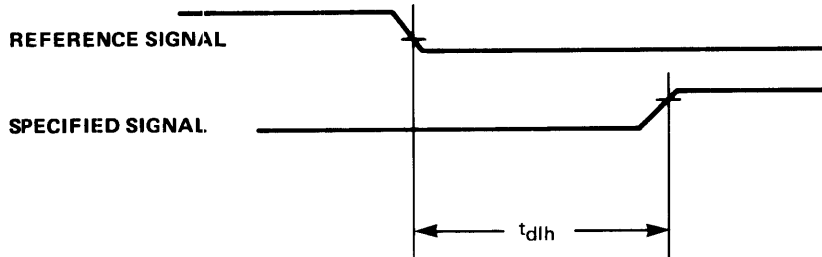
| |
|--|
| <p>PS - Power Supply (HP 12035A)</p> |
| <p>SHC - Short Half Cycle</p> <p>The Short Half Cycle refers to the time period when SCLK- is high.</p> |
| <p>^t D - Delay time</p> <p>The time interval from a signal edge used as a reference point to the point in time when the specified signal is guaranteed to be stable on the backplane.</p>  |
| <p>^t DHL- Delay time high to low</p> <p>The time interval from a signal edge used as a reference point, to the point in time when the specified signal is guaranteed to be low if in fact it is going low.</p>  |
| <p>NOTE</p> <p>In these timing diagrams, a high notch is 2.0 volts and a low notch is 0.4 volts as shown below.</p>  |

DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS (CONTINUED)

t

DLH- Delay time low to high

The time interval from a signal edge used as a reference time to the point in time when the specified signal is guaranteed to be high if in fact it is going high.



t

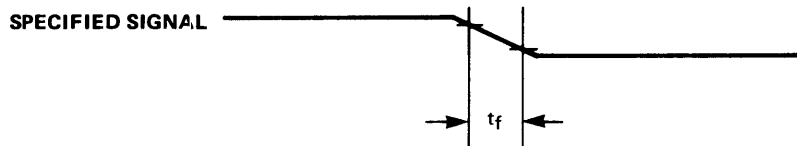
DZ Delay time to high impedance

The time interval from a signal edge used as reference to the point in time when the specified signal will no longer be actively driven.

t

F - Fall time

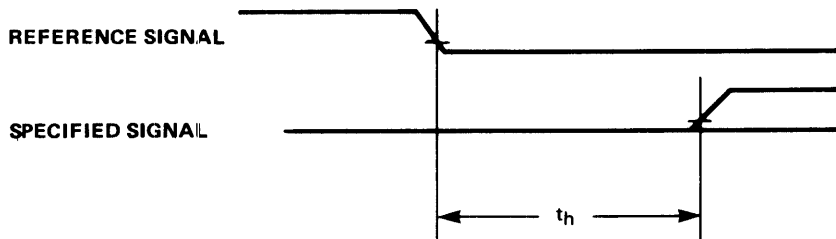
The time interval during which a signal is in transition from high to low.



t

H - Hold time

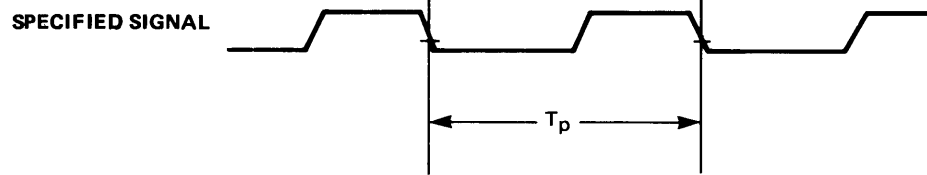
The period of time during which a specified signal must remain stable at its logic level after a certain reference edge.



DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS (CONTINUED)

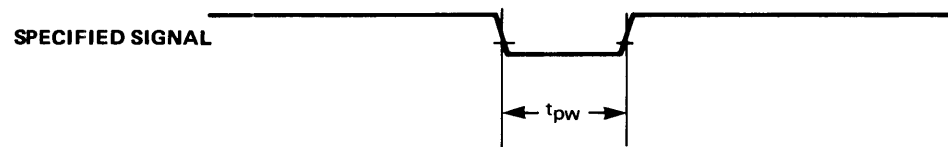
T
p - Period

The duration of one cycle of a periodic signal.



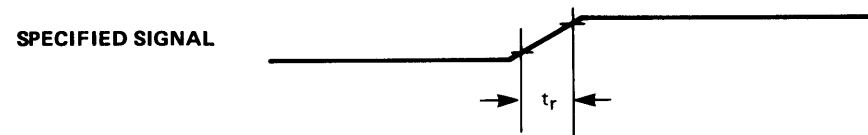
t
pw - Pulse width time

The time interval between the leading and trailing edge of a pulse. Specifically, for a normally high signal, t_{pw} is the time when that signal is low. For a normally low signal, t_{pw} is the time when that signal is high.



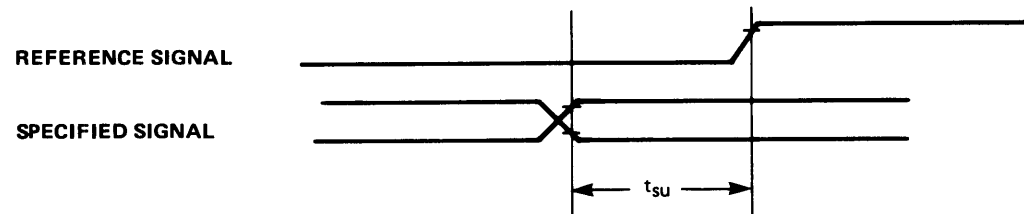
t
r - Rise time

The time interval during which a signal is in transition from low to high.



t
su - Set-up time

The time interval a specified signal must be at a stable logic level before a given edge of a reference signal.

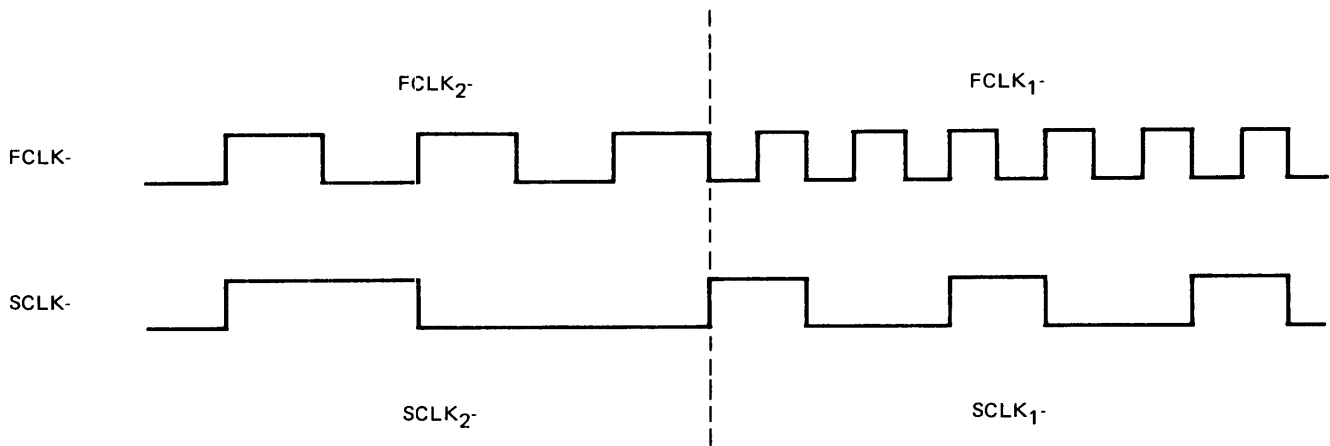


DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS (CONTINUED)

XLM - Expanded Memory
Any memory subsystem of 128 to 512 Kbytes.

6.5.1 DUAL-SPEED CLOCK REFERENCES

FCLK- and SCLK- are dual-speed clocks. Although their nominal frequencies are 22.016 MHz and 4.4032 MHz, respectively, they slow down to half this speed during the assertion of IOGO- on the backplane. All timing references to these clocks, when not specified, are valid for either of the frequencies. When it is necessary to distinguish between the frequencies, the subscript 1 is used for the faster and 2 for the slower frequency.



6.5.2 INTERACTIVE TIMING EXAMPLES

Previous timing examples have shown handshakes or protocols by type of interaction. In actuality, however, transactions may start only to be preempted by other higher priority transactions and held off for an indefinite period of time. Figures 6-12 and 6-13 show various transactions over the backplane which begin, are preempted, and then later are allowed to complete.

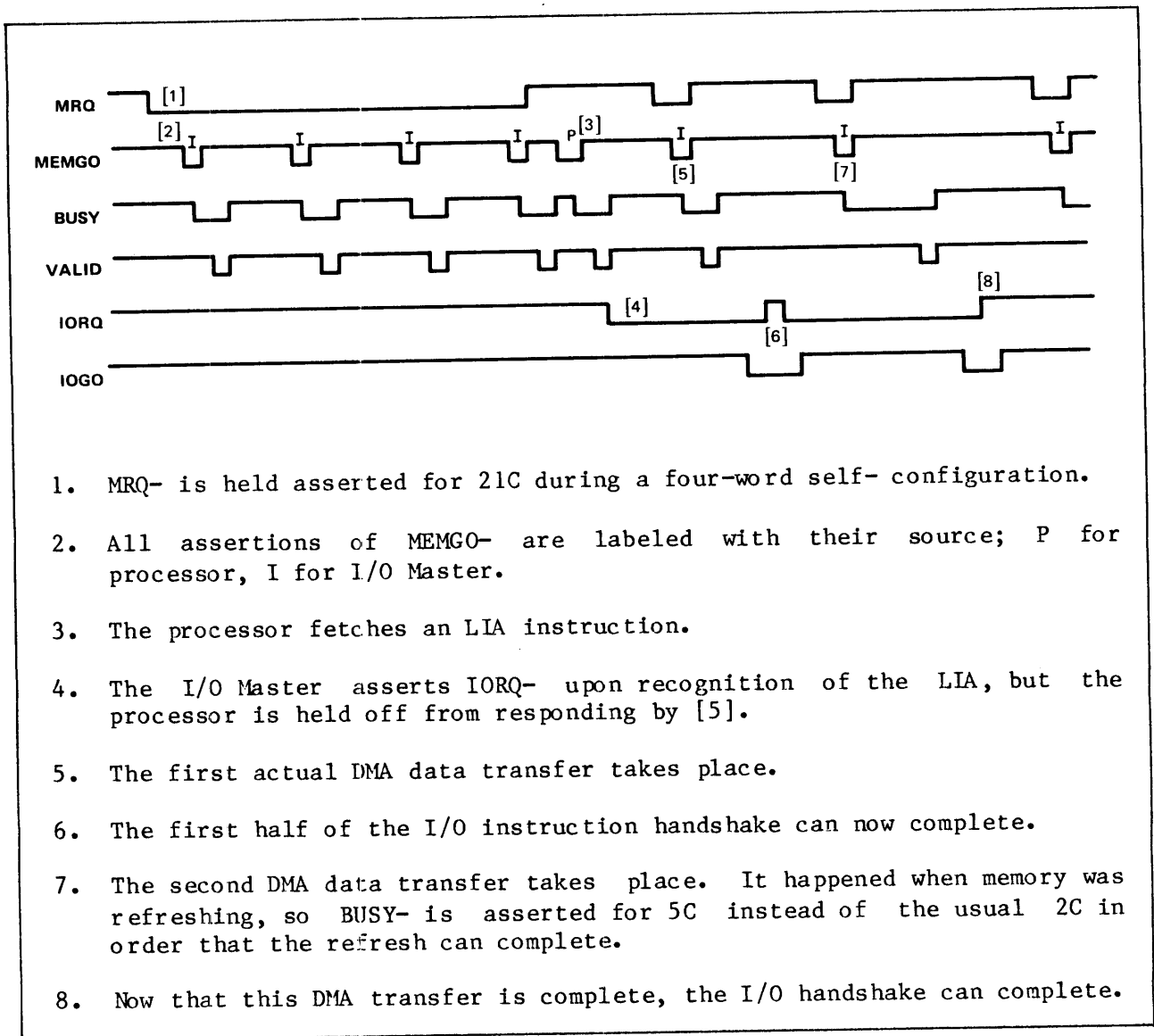
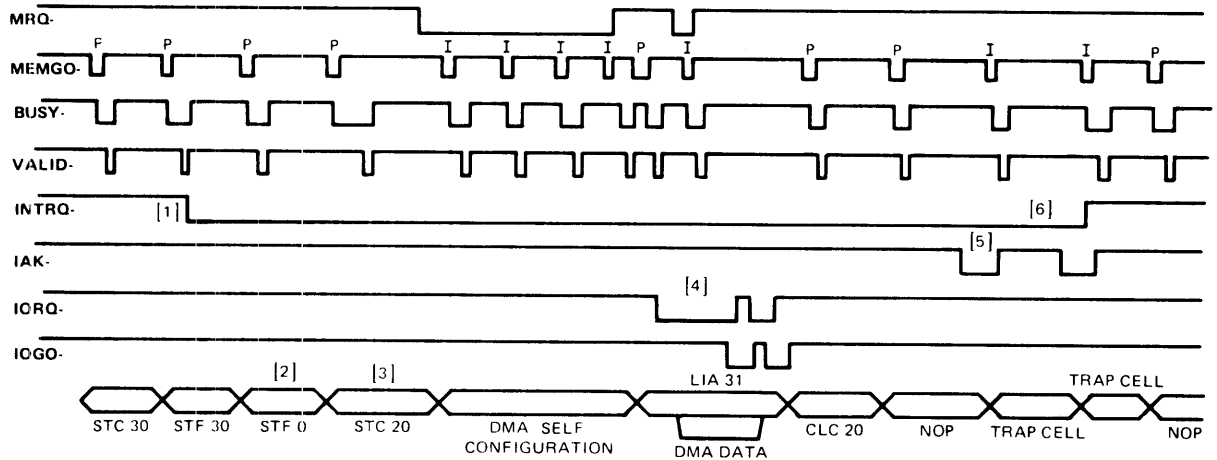


Figure 6-12. Interactive DMA and I/O Instruction Timing



7700-563

1. The Flag and Control flip-flops are set, so the I/O Master attempts to interrupt.
2. Interrupt system is turned on with an STF 0 but processor must not respond until after the next instruction if current is an I/O instruction.
3. Self-configuring DMA is started, set up for a one-word transfer.
4. An LIA is executed, interleaved with DMA as in figure 6-12.
5. After the NOP instruction is fetched, the processor can respond to the interrupt caused by Flag 30.
6. The I/O Master does not release INTRQ, because it now also has a DMA completion interrupt pending.

Figure 6-13. Interactive DMA, I/O Instruction, and Interrupt Timing

Table 6-4. Timing Specifications for ABO - 14

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|-----------|--|---------|----------|-----|-----|-----|
| t _{su} | SCLK-↑ | Edges that occur during MEMGO | | M | 0 | | |
| t _{su} | SCLK-↑ | During Processor MEMGO | | XLM | 25 | | |
| t _{su} | SCLK-↑ | During DMA MEMGO | | XLM | -20 | | |
| t _h | SCLK-↑ | Edge that occurs during MEMGO- | | M,XLM | 67 | | |
| t _D | SCLK-↓ | Edge that causes MEMGO-↓ | I/O | | | | 100 |
| t _h | SCLK-↓ | Edge that causes MEMGO-↑ | I/O | | 20 | | |
| t _{su} | SCLK-↑ | Edge that occurs during MEMGO-↓ | P | | 220 | | |
| t _h | SCLK-↓ | Edge that causes MEMGO-↑ | P | | 20 | | |
| t _D | SCLK-↓ | 1st after BUSY-↑ following MRQ-↑ | P | | | | 70 |
| t _{DZ} | MRQ-↓ | CPU can be held off by MRQ- from any interface | P | | 10 | | 45 |
| t _{DZ} | SCLK-↓ | Due to MRQ-↓ | P | | | | 95 |
| t _H | SCLK-↑ | Edge that causes IAK-↓ | P | | | | 185 |
| t _{su} | SCLK-↑ | Edge that occurs during MEMGO- in interrupt cycle. | | P | 0 | | |
| t _H | SCLK-↑ | Same edge | | P | 100 | | |

Table 6-4. Timing Specifications for ABO - 14 (Continued)

| | | | | | | | |
|-----------------|--------|--|--|----|-----|--|--|
| t _{su} | SCLK-↑ | Edge that occurs during MEMGO | | AI | -45 | | |
| t _h | SCLK-↑ | Edge that occurs during MEMGO | | AI | 106 | | |
| t _{su} | SCLK-↑ | Edge that occurs during MEMGO in interrupt cycle | | AI | -45 | | |
| t | SCLK-↓ | Edge that causes MEMGO-↑ during interrupt cycle | | AI | 25 | | |

Table 6-5. Timing Specifications for BUSY-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-----------|--|---------|----------|------------|-----|-----|
| t _{DHL} | SCLK-↑ | Edge that occurs during MEMGO- | M,XLM | | 0 | | 44 |
| t _{DLH} | SCLK-↑ | 2C later if memory was not doing refresh | M,XLM | | 0 | | 44 |
| t _{DLH} | SCLK-↑ | 3C-5C later if memory was doing refresh when MEMGO- occurred | M,XLM | | 0 | | 44 |
| t _{SU} | SCLK-↓ | In order to hold off MEMGO- | | I/O | 5 | | |
| t _h | SCLK-↓ | | | I/O | 5 | | |
| t _{DHL} | SCLK-↑ | During MEMGO- for boot ROM access | P | | | | 65 |
| t _{DLH} | SCLK-↑ | 3C later | P | | | | 40 |
| t _{su} | SCLK-↓ | Any falling edge | | P | 5 | | |
| t _H | SCLK-↓ | Same edge | | P | 10 | | |
| t _{pw} | | Longer than 2C when doing refresh. | M | | 2C-50 nsec | 2C | 5C |
| t _{pw} | | Longer than 2C when doing refresh. | XLM | | 2C-50 nsec | 2C | 4C |
| t _{su} | SCLK-↓ | Any falling edge | | AI | 1 | | |
| t _H | SCLK-↓ | Same edge | | AI | 7 | | |

Table 6-6. Timing Specifications for CCLK-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------|--------------|--------------------------------|------------|-------------|-------------|-------------|-------------|
| f | asynchronous | To all other backplane signals | P | | 14.7441 MHz | 14.7456 MHz | 14.7471 MHz |
| Duty cycle | | | P | | 30% | 50% | |

Table 6-7. Timing Specifications for CPUTURN-/COTURN-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|----------------------|-----------|-------------------------------|------------|-------------|-----|-----|-----|
| CPUTURN- t DHL | SCLK-↓ | That causes MEMGO-↓ | P | | | | 210 |
| t DHL | SCLK-↓ | | P | | | | 120 |
| CPUTURN- t SU | SCLK-↓ | To inhibit MRQ- | | I/O | 25 | | |
| t H | SCLK-↓ | Same edge | | I/O | -5 | | |
| COTURN- t SU | SCLK-↑ | Edge that occurs during MEMGO | | XLM | 90 | | |
| t H | SCLK-↑ | Edge that occurs during MEMGO | | XLM | 67 | | |

Table 6-3. Timing Specifications for CRS-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------|--------------|----------------------|------------|-------------|-----|-----|-----|
| t_{pw} | asynchronous | | | M | 20 | | |
| t_{pw} | | | | XLM | 1C | | |
| t_{pw} | SCLK-↓ | | | I/O | 1C | | |
| t_{SU} | | | | I/O | -30 | | |
| t_{DHL} | SCLK-↓ | No concurrent DMA | P | | | | 35 |
| t_{DHL} | SCLK-↓ | End of DMA | P | | | | 117 |
| t_{DLH} | Next SCLK-↓ | | P | | | | 50 |

Table 6-9. Timing Specifications for DB0 - 15

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|--|-----------|--|---------|----------|-----|-----|-----|
| t _D | SCLK-↑ | During MEMGO- | | M | | | 23 |
| t _D | SCLK-↑ | During MEMGO | | XLM | | | 4 |
| t _h | SCLK-↑ | Same edge | | M,XLM | 90 | | 227 |
| t _{SU} | SCLK-↑ | That causes VALID-↑ | M | | 126 | | |
| t _{SU} | SCLK-↑ | That causes VALID-↑ | XLM | | 20 | | |
| t _H | SCLK-↑ | That causes VALID-↑ | M,XLM | | 91 | | |
| t _{SU} | VALID-↑ | All cases | M,XLM | | 50 | | |
| t _h | VALID-↑ | Same edge | M,XLM | | 50 | | |
| t _D | SCLK-↓ | Edge that causes MEMGO-↓ (DMA) | I/O | | | | 140 |
| t _H | SCLK-↓ | Edge that causes MEMGO-↑ (DMA) | I/O | | 35 | | |
| t _D | SCLK-↓ | First SCLK-↓ after IOGO-↓* (I/O instruction) | I/O | | | | 315 |
| t _H | SCLK-↑ | Third SCLK-↑ during IOGO- (I/O instruction) | I/O | | 65 | | |
| t _{su} | VALID-↑ | DMA read | | I/O | 50 | | |
| t _H | VALID-↑ | DMA read | | I/O | 50 | | 180 |
| t _{su} | SCLK-↓ | Second SCLK-↓* during IOGO- (I/O instr) | | I/O | 10 | | |
| *Provided IOGO-↓ met 10-nsec set-up time to previous SCLK-↑. | | | | | | | |

Table 6-9. Timing Specifications for DB0 - 15 (Continued)

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|--|-------------|--|---------|----------|-----|-----|-----|
| t _H | SCLK-↑ | Third SCLK-↑* during IOGO- (I/O instr) | | I/O | 40 | | 227 |
| t _{SU} | SCLK-↑ | Edge that causes VALID-↑ (memory read) | | P | 20 | | |
| t _H | SCLK-↑ | Same edge (memory read) | | P | 15 | | |
| t _{su} | SCLK-↑ | Second SCLK-↑ after SCLK-↓ which causes IORQ-↑ (I/O instr) | | P | 20 | | |
| t _H | SCLK-↑ | Same edge (I/O instr) | | P | 15 | | 227 |
| t _{D1} | SCLK-↑ 1 | Edge that causes MEMGO-↓ (memory write) | P | | | | 120 |
| t _H | SCLK-↓ | Edge that causes MEMGO-↑ (memory write) | P | | 25 | | |
| t _D | SCLK-↑ | Edge that precedes SCLK-↓ which causes IOGO-↓ (I/O write) | P | | 30 | | 110 |
| t _H | SCLK-↑ | Edge that precedes SCLK-↓ which causes IOGO-↑ (I/O write) | P | | 15 | | |
| t _D | SCLK-↓ | During VALID- (boot ROM fetch) | P | | | | 50 |
| t _{D2} | SCLK-↓ 2 | Following an I/O handshake | P | | | | 210 |
| *Provided IOGO-↓ met 10-nsec set-up time to previous SCLK-↑. | | | | | | | |

Table 6-9. Timing Specifications for DBO - 15 (Continued)

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|-----------|--|---------|----------|-----|-----|-----|
| t _h | SCLK-↓ | Edge that follows VALID-↑ (boot ROM fetch) | P | | 20 | | |
| t _D | SCLK-↓ | First after BUSY-↑ following MRQ-↑ | P | | | | 120 |
| t _{DZ} | MRQ-↓ | Assertion of MRQ- will cause CPU to stop driving DB | P | | 20 | | 65 |
| t _{DZ} | SCLK-↓ | Due to MRQ-↓ | P | | | | 145 |
| t _D | SCLK-↓ | During VALID- (A/B instr fetch) | P | | | | 110 |
| t _H | SCLK-↓ | First after VALID-↑ (A/B instr fetch) | P | | 20 | | |
| t _D | SCLK-↑ | That occurs during MEMGO | | AI | | | 40 |
| t _H | SCLK-↑ | Same edge | | AI | 90 | | |
| t _{su} | SCLK-↑ | That causes VALID-↑ | | AI | 0 | | |
| t _H | SCLK-↑ | Same edge | | AI | 15 | | |
| t _{su} | SCLK-↑ | Second after SCLK-↓ which causes IORQ-↑ during I/O instr | | AI | 0 | | |
| t _H | SCLK-↑ | Same edge | | | 15 | | |

Table 6-10. Timing Specifications for FCLK-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|------------------------|-------|---------|----------|----------------|---------------|----------------|
| T P | | | | M | 36 | | |
| T P | | | | XLM | 45 | | |
| f | | | | M | | | 27.7778 MHz |
| f | | | | XLM | | | 22.0171 MHz |
| f 1 | While IOGO- is high | | P | | 22.0149 MHz | 22.016 MHz | 22.0171 MHz |
| duty cycle 1 | While IOGO- is high | | P | | 29% | 50% | 71% |
| f 2 | While IOGO- is low | | P | | 11.0074 MHz | 11.008 MHz | 11.0086 MHz |
| duty cycle 2 | While IOGO- is low | | P | | 41% | 50% | 59% |
| T P | | | | AI | 45 | | |
| f | | | | AI | | | 22.0171 MHz |

Table 6-11. Timing Specifications for IAK-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-------------|------------------------------------|---------|----------|-----|-----|-----|
| t _{SU} | SCLK-↑ | | | I/O | 10 | | |
| t _H | SCLK-↑ | Same edge | | I/O | 25 | | |
| t _{PW} | | | | I/O | 2C | | 3C |
| t _{SU} | SCLK-↓ | To inhibit MRQ | | I/O | 25 | | |
| t _H | SCLK-↓ | Same edge | | I/O | 0 | | |
| t _{D1} | SCLK-↓ 1 | | P | | | | 55 |
| t _{D2} | SCLK-↑ 2 | Following an I/O handshake | P | | | | 145 |
| t _H | SCLK-↓ | First after BUSY-↓ | P | | 15 | | |
| t _D | SCLK-↓ | First after BUSY-↑ following MRQ-↑ | P | | | | 60 |
| t _{DLH} | MRQ-↓ | | P | | 10 | | 55 |
| t _{DLH} | SCLK-↓ | Due to MRQ-↓ | P | | | | 90 |
| t _{SU} | SCLK-↑ | | | AI | 3 | | |
| t _H | SCLK-↑ | Same edge | | AI | 20 | | |
| t _{PW} | | | | AI | 2C | | |
| t _{pw} | | | | XLM | 1C | | |

Table 6-12. Timing Specifications for ICHID-/ICHOD-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|--------------------|-------------------|--|---------|----------|-----|-----|-----|
| ICHID- t SU | SCLK-↓ | Second SCLK-↓* during IAK- | | I/O | 10 | | |
| ICHID- t H | SCLK-↓ | Third SCLK-↓* during IAK- | | I/O | 50 | | |
| t D | Asynch- ronous | ICHID-↓ to ICHOD-↓ | I/O | | | 5 | 7.5 |
| ICHOD- t DHL | SCLK-↑ | Edge that causes INTRQ-↓ | I/O | | | | 200 |
| ICHOD- t H | IAK-↑ | ICHOD- is held low during the entire assertion of IAK- | I/O | | SHC | | |
| ICHOD- t DHL | IAK-↓ | | P | | | | 50 |
| ICHOD- t H | IAK-↑ | | P | | 0 | | |

Table 6-13. Timing Specifications for INTRQ-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------|-----------|-----------------------------|---------|----------|-----|-----|-----|
| t DHL | SCLK-↓ | | I/O | | | | 200 |
| t DLH | SCLK-↓ | Third SCLK- after IAK-↓* | I/O | | | | 300 |
| t su | SCLK-↓ | | | P | 15 | | |
| t H | IAK-↓ | | | P | 0 | | |

*Provided IAK- met 10-nsec set-up time to previous SCLK-↑.

Table 6-14. Timing Specifications for IOGO-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-----------|---|---------|----------|----------|-----|-----|
| t _{SU} | SCLK-↑ | During IORQ- | | I/O | 10 | | |
| t _h | SCLK-↑ | Same edge | | I/O | 25 | | |
| t _{pw} | | 3↑ of SCLK- | | I/O | 2C + LHC | | |
| t _{SU} | SCLK-↓ | To inhibit MRQ | | I/O | 25 | | |
| t _H | SCLK-↓ | Same edge | | I/O | 0 | | |
| t _{DHL} | SCLK-↓ | | P | | | | 50 |
| t _{DLH} | SCLK-↑ | Second SCLK-↑ after SCLK-↓ that caused IORQ-↑ | P | | | | 40 |
| t _{DLH} | SCLK-↑ | Second SCLK-↑ after SCLK-↓ that caused IORQ-↑ | | AI | | | 100 |
| t _{DLH} | SCLK-↓ | SHC later | | AI | 5 | | |
| t _{DHL} | SCLK-↓ | Second after BUSY-↑ following MRQ-↑ | P | | | | 50 |
| t _{DLH} | MRQ-↓ | | P | | | | 50 |
| t _{DLH} | SCLK-↓ | Due to MRQ-↓ | P | | | | 85 |
| t _{su} | SCLK-↑ | | | AI | 10 | | |
| t _H | SCLK-↑ | | | AI | 25 | | |

Table 6-15. Timing Specifications for IORQ-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|---|-------------------------------|--|---------|----------|-----|-----|-----|
| t DHL1 | Data bus valid during VALID-* | 1 refers to first handshake request after RNI-↓ | I/O | | | | 325 |
| t DHL2 | SCLK-↓ | 2 refers to second SCLK-↓ after** IOGO-↓ (double handshake only) | I/O | | | | 145 |
| t DHL3 | SCLK-↑ | SCLK-↑ following SCHID-↑ (3 refers to initial IORQ-↓ on slave cycle) | I/O | | | | 45 |
| t DLH | SCLK-↓ | First SCLK-↓ after IOGO-↓** | I/O | | | | 210 |
| t SU | SCLK-↓ | 5C+SHC after SCLK-↑ which causes RNI-↑ or VALID-↑ | | P | 50 | | |
| t h | SCLK-↓ | Same edge | | P | 10 | | |
| t SU | SCLK-↓ | 1C after edge which caused second assertion of IORQ- | | P | 50 | | |
| t h | SCLK-↓ | Same edge | | P | 10 | | |
| t SU | SCLK-↓ | Following any release of IORQ | | P | 50 | | |
| t h | SCLK-↓ | Same edge | | P | 10 | | |
| <p>* During VALID-, there could be false assertions of IORQ- due to the data bus being in transition. This will not affect system operation, however, because the processor does not check IORQ- until two states after RNI-↑ when IORQ- is guaranteed to be valid.</p> <p>** Provided IOGO-↓ met 10-nsec set-up time to previous SCLK-↑.</p> | | | | | | | |

Table 6-15. Timing Specifications for IORQ- (Continued)

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|-----------|----------------------------|---------|----------|-----|-----|-----|
| t _{SU} | SCLK-↓ | First SCLK-↓ after SCHOD-↓ | | P | 50 | | |
| t _h | SCLK-↓ | Same edge | | P | 10 | | |

Table 6-16. Timing Specifications for MCHID-/MCHOD-, MCHODOC-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|--------------------------|-----------|------------------------|---------|----------|-----|-----|-----|
| MCHID-t _{SU} | SCLK-↓ | | | I/O | 5 | | |
| MCHID-t _h | SCLK-↓ | Same edge | | I/O | 20 | | |
| t _{DHL} | | MCHID-↓ to MCHOD-↓ | I/O | | | 5 | 7 |
| MCHOD-t _{DHL} | SCLK-↓ | Edge that causes MRQ-↓ | I/O | | | | 30 |
| MCHODOC-t _{DHL} | SCLK-↓ | Edge that causes MRQ-↓ | I/O | | | | 55 |
| MCHODOC-t _{DLH} | SCLK-↓ | Edge that causes MRQ-↑ | I/O | | | | 165 |

Table 6-17. Timing Specifications for MEMDIS-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------|-------------|------------------------------------|------------|-------------|-----|-----|-----|
| t SU | SCLK-↑ | Edge that occurs during MEMGO- | | M,XLM | 30 | | |
| t h | SCLK-↑ | Same edge | | M,XLM | 0 | | |
| t DHL | SCLK-↓ | Edge that causes MEMGO-↓ | P | | | | 30 |
| t DHL | SCLK-↑ 2 | Following an I/O handshake | P | | | | 120 |
| t DLH | SCLK-↓ | First SCLK-↓ after BUSY-↓ | P | | | | 30 |
| t DHL | SCLK-↓ | First after BUSY-↓ following MRQ-↑ | P | | | | 30 |
| t DLH | MRQ-↓ | | P | | | | 25 |
| t DLH | SCLK-↓ | Due to MRQ- | P | | | | 70 |

Table 6-18. Timing Specifications for MEMGO-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-------------|---|---------|----------|-----|-----|-----|
| t _{SU} | SCLK-↑ | | | M,XLM | 10 | | |
| t _h | SCLK-↑ | Same edge | | M | SHC | | 215 |
| t _h | SCLK-↑ | Same edge | | XLM | 0 | | |
| t _{DHL} | SCLK-↓ | | I/O | | | | 45 |
| t _{DLH} | SCLK-↓ | Next edge | I/O | | 30 | | 110 |
| t _{DHL} | SCLK-↓ | | P | | | | 40 |
| t _{DHL} | SCLK-↑ 2 | Following an I/O handshake | P | | | | 130 |
| t _{DLH} | SCLK-↓ | First SCLK-↓ after BUSY-↓ | P | | | | 100 |
| t _{DHL} | SCLK-↓ | First after BUSY-↑ following MRQ-↑ | P | | | | 45 |
| t _{DLH} | MRQ-↓ | | P | | | | 95 |
| t _{DLH} | SCLK-↓ | MEMGO- aborted by MRQ- from edge which caused MEMGO | P | | | | 125 |
| t _{su} | SCLK-↑ | | AI | | 4 | | |
| t _h | SCLK-↑ | Same edge | AI | | 15 | | |

Table 6-19. Timing Specifications for MLOST-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|--|-----------|-------|---------|----------|-------------|-----|-------|
| t _r , t _f | | | BB | | | | 50 |
| t _{su} | PON↑ | | BB | | 500 usec | | |
| t _h | PON↑ | | BB | | 10 msec | | 1 sec |
| t _h | PON↑ | | SW* | | 5 msec | | |
| <p>* Processor does not latch MLOST-. During the pretest, the state of this line is used by the software to determine whether or not to initialize memory.</p> | | | | | | | |

Table 6-20. Timing Specifications for MP+

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|-----------|---|---------|----------|-----|-----|-----|
| t _{SU} | VALID↑ | | | I/O | 0 | | |
| t _H | SCLK↑ | Second SCLK↑ after VALID↑ (non-I/O instr). Second SCLK↑ after last IOGO↑ (I/O instr) | | I/O | 0 | | |
| t _D | SCLK↑ | 1C+SHC before SCLK↓ that causes MEMGO↓ | P | | | | 205 |

Table 6-21. Timing Specifications for MRQ-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-----------|----------------------------------|------------|-------------|-----|-----|-----|
| t _{DHL} | SCLK-↓ | | I/O | | | | 50 |
| t _{DLH} | SCLK-↓ | Edge that causes MEMGO-↑ | I/O | | 30 | | 110 |
| t _{SU} | SCLK-↑ | | | P | 30 | | |
| t _H | SCLK-↑ | Edge that causes BUSY-↓ | | P | 15 | | |
| t _{su} | SCLK-↑ | | | AI | 4 | | |
| t _H | SCLK-↑ | Same edge | | AI | 16 | | |
| t _{su} | SCLK-↑ | Edge that occurs during MEMGO | | XLM | 90 | | |
| t _H | SCLK-↑ | Edge that occurs during MEMGO | | XLM | 67 | | |

Table 6-22. Timing Specifications for PE-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|---------------------|--|---------|----------|-----|-----|-----|
| t _{pw} | asynchronous | 1C=227.1 nsec | M | | 86 | | |
| t _{pw} | | | XLM | | 60 | | |
| t _{DHL} | VALID-↑ | Actually caused by edge of FCLK- | M | | -71 | | 3 |
| t _{DHL} | VALID-↑ | | XLM | | -40 | | 30 |
| t _{pw} | | Must occur during window | | I/O | 50 | | |
| t _{SU} | Start window SCLK-↓ | First edge after edge that causes RNI-↓ (instr fetch window) | | I/O | 0 | | |
| t _h | End window SCLK-↑ | First edge after VALID-↑ (instr fetch window) | | I/O | 0 | | |
| t _{SU} | Start window SCLK-↓ | First edge after edge that causes VALID-↓ (DMA window) | | I/O | 0 | | |
| t _h | End window SCLK-↓ | Second edge after edge that causes VALID-↑ (DMA window) | | I/O | 0 | | |
| t _{pw} | | Must occur during window | | P | 50 | | |
| t _{su} | Start window SCLK-↓ | First edge after VALID-↓ | | P | 0 | | |
| t _{su} | End window SCLK-↓ | First edge after VALID-↑ | | P | 0 | | |

Table 6-23. Timing Specifications for PFW-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|---------------------------------|-----------|--|---------|----------|---------|-----|-----|
| t _{SU} | PON+↓ | | PS | | 5 msec | | |
| t _{SU} | PON+↑ | | PS | | 10 msec | | |
| t _r , t _f | | | PS | | | | 50 |
| t _{su} | PON+↑ | | | P | 50 | | |
| t _{su} | PON+↓ | Software requires time for power down routine to execute | | SW | 5 msec | | |

Table 6-24. Timing Specifications for PON+

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|---------------------------------|-----------|--|---------|----------|---------|---------|----------|
| t _D | | Supplies up and within regulation | PS | | 50 msec | 65 msec | 100 msec |
| t _r , t _f | | | PS | | | | 50 nsec |
| t _{pw} | | Time required to fully initialize CPU chip | | P | 2C | | |
| t _{pw} | | | | AI | 2C | | |

Table 6-25. Timing Specifications for PS-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|-----------|---|---------|----------|-----|-----|-----|
| All | | Same as data bus requirements for all memory writes | | M,XLM | | | |
| t _{SU} | SCLK-↓ | Edge that causes MEMGO-↓ | P | | | | 0 |
| t _h | SCLK-↑ | First edge after VALID-↑ | P | | 0 | | |

Table 6-26. Timing Specifications for RCLK+

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------|-----------|-------|---------|----------|---------|-----------|---------|
| f | | | P | | -0.005% | 4.403 MHz | +0.005% |
| duty cycle | | | P | | 37% | 40% | 43% |

Table 6-27. Timing Specifications for REMEM-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-----------|---------------------------------|---------|----------|-----|-----|-----|
| t _{su} | SCLK-↑ | SCLK- that occurs during MEMGO- | | M,XLM | 30 | | |
| t _h | SCLK-↑ | Same edge | | M,XLM | 0 | | |
| t _{DHL} | SCLK-↓ | | I/O | | | | 45 |
| t _{DLH} | SCLK-↓ | Next edge | I/O | | 30 | | 110 |

Table 6-28. Timing Specifications for RNI-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-----------|-----------------------------------|---------|----------|--------------------|-----|-----|
| t _{SU} | SCLK-↓ | That occurs during VALID- | | I/O | 25 | | |
| t _H | SCLK-↓ | Same edge | | I/O | 30 | | |
| t _{DHL} | SCLK-↑ | First edge after MEMGO-↓ from CPU | P | | | | 45 |
| t _{DLH} | SCLK-↑ | Edge that causes VALID-↑ | P | | | | 45 |
| t _{pw} | | | P | | | 2C | |
| t _{pw} | | | | I/O | 1C-t _{su} | 1C | |
| t _{su} | SCLK-↓ | | | AI | 4 | | |
| t _h | SCLK-↓ | | | AI | 11 | | |
| t _{pw} | | | | XLM | 1C | | |

Table 6-29. Timing Specifications for SC0 - SC4

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|-----------|--------------------------------|---------|----------|-----|-----|-----|
| t _D | SCLK-↓ | Edge that causes MEMGO-↓ | I/O | | | | 90 |
| t _H | SCLK-↓ | Edge that causes MEMGO^ | I/O | | 20 | | |
| t _{su} | SCLK-↑ | Edge that occurs during MEMGO- | | XLM | 35 | | |
| t _H | SCLK-↑ | Edge that occurs during MEMGO- | | XLM | 67 | | |

Table 6-30. Timing Specifications for SC5

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-----------|--------------------------------|---------|----------|-----|-----|-----|
| t _{DHL} | SCLK-↓ | Edge that causes MEMGO-↓ | I/O | | | | 80 |
| t _H | SCLK-↓ | Edge that causes MEMGO↑ | I/O | | 40 | | 180 |
| t _{su} | SCLK-↑ | Edge that occurs during MEMGO- | | XLM | 56 | | |
| t _H | SCLK-↑ | Edge that occurs during MEMGO- | | XLM | 67 | | |

Table 6-31. Timing Specifications for SCHID-/SCHOD-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-------------------------|-----------|--------------------------|---------|----------|-----|-----|-----|
| t _D | | SCHID-↓ to SCHOD-↓ | I/O | | | 5 | 7.5 |
| SCHOD-t _{DHL*} | SCLK-↑ | Edge that caused SCHID-↑ | I/O | | | | 25 |
| SCHID-t _{SU} | SCLK-↑ | | | I/O | 0 | | |
| SCHID-t _H | SCLK-↑ | Same edge | | I/O | 15 | | |
| t _{DLH} | SCLK-↑ | | P | | | | 15 |
| t _{DHL} | SCLK-↑ | Next edge | P | | | | 15 |

* If a low priority interface asserts SLAVE-, a higher priority interface can get the slave cycle if the higher priority interface lowers SCHOD- at any time up until 1c-169 nsec after the SCLK- which caused SCHID-.

Table 6-32. Timing Specifications for SCLK-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-------------------------|---------------------|-------|---------|----------|---------|-------|---------|
| f ₁ | While IOGO- is high | | P | | -0.005% | 4.403 | +0.005% |
| Duty cycle ₁ | While IOGO- is high | | P | | 33% | 40% | 47% |
| t _D | FCLK-↑ | | | M,XLM | 1 | | 21 |
| f ₂ | While IOGO- is low | | P | | -0.005% | 2.202 | +0.005% |
| Duty cycle ₂ | While IOGO- is low | | P | | 36% | 40% | 44% |

Table 6-33. Timing Specifications for SLAVE-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|------------------|-----------|--------------------------|---------|----------|-----|-----|-----|
| t _{DHL} | SCLK-↑ | | I/O | | | | 45 |
| t _{DLH} | SCLK-↑ | First edge after SCHID-↓ | I/O | | | | 130 |
| t _{SU} | SCLK-↓ | | | P | 0 | | |
| t _h | SCLK-↑ | Edge that causes SCHOD-↑ | | P | 0 | | |

Table 6-34. Timing Specifications for SPRQ-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|-----------|-------|---------|----------|-----|-----|-----|
| t _H | IAK-↓ | | | P | 0 | | |
| t _{SU} | SCLK-↓ | | | P | 15 | | |

Table 6-35. Timing Specifications for VALID-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------|-----------|---|---------|----------|--------------------|-----|-----|
| t DHL | SCLK-↑ | First SCLK-↑ after BUSY-↓, no refresh. Second to fourth SCLK-↑ after BUSY-↓ with refresh. | M, XLM | | 0 | | 43 |
| t DLH | SCLK-↑ | Second SCLK-↑ after BUSY-↓, no refresh. Third to fifth SCLK-↑ after BUSY-↓, with refresh. | M, XLM | | 0 | | 43 |
| t SU | SCLK-↓ | | | I/O | 10 | | |
| t h | SCLK-↓ | Same edge | | I/O | 30 | | |
| t SU | SCLK-↓ | | | P | 10 | | |
| t h | SCLK-↓ | Same edge | | P | 10 | | |
| t DHL | SCLK-↑ | Second SCLK-↑ after BUSY-↓ (boot ROM access) | P | | | | 55 |
| t DLH | SCLK-↑ | Next edge | P | | | | 55 |
| t pw | | | | I/O | 1C-t _{su} | 1C | |
| t DHL | SCLK-↑ | | | AI | | | 50 |
| t DLH | SCLK-↑ | | | AI | 0 | | 50 |

Table 6-36. Timing Specifications for WE-

| PARAMETER | REFERENCE | NOTES | GUAR BY | REQ'D BY | MIN | TYP | MAX |
|-----------------|-------------|--|---------|----------|-----|-----|-----|
| t _{SU} | SCLK-↑ | That occurs during MEMGO | | M | 0 | | |
| T _{SU} | SCLK-↑ | That occurs during MEMGO | | XLM | 25 | | |
| t _H | SCLK-↑ | Same edge | | M,XLM | 67 | | |
| t _D | SCLK-↓ | That causes MEMGO-↓ | I/O | | | | 100 |
| t _H | SCLK-↓ | That causes MEMGO-↑ | I/O | | 20 | | |
| t _{D1} | SCLK-↓ 1 | That causes MEMGO-↓ | P | | | | 65 |
| t _{D2} | SCLK-↑ 2 | Following an I/O handshake | P | | | | 155 |
| t _H | SCLK-↓ | That causes MEMGO↑ | P | | 20 | | |
| t _D | SCLK-↓ | After BUSY-↑ for MRQ-↑ | P | | | | 70 |
| t _{DZ} | MRQ-↓ | | P | | 10 | | 45 |
| t _{DZ} | SCLK-↓ | Due to MRQ-↓ | P | | | | 95 |
| t _H | SCLK-↑ | That causes IAK-↓ | P | | | | 185 |
| t _{SU} | SCLK-↑ | That occurs during MEMGO- during interrupt cycle | | P | 0 | | |
| t _H | SCLK-↑ | Same edge | | P | 100 | | |

6.6 SIGNAL DEFINITIONS

Table 6-37 lists all L-Series backplane signals. The signals are listed in alphabetical order, along with their definitions, where they originated, where they go, functions, and general timing specifications. Timing values, when given, are nominal. For specific timing values, see tables 6-4 through 6-36.

Table 6-37. Backplane Signal Definitions

| | |
|--------------|--|
| (A0+)-(A14+) | |
| FULL NAME: | Address Bus 0-14 (Tri-state, high true) |
| DRIVEN BY: | The processor card or the I/O Master during a DMA transfer or while receiving interrupt service. (In the case of interrupt service, the card drives A0 - A5 with its select code and A6 - A14 with zeros.) |
| RECEIVED BY: | Memory and processor card. |
| FUNCTION: | The address bus is used to transfer a 15-bit absolute address to the memory, of which A0 is the least significant bit. The processor will latch the address in case a parity error or memory protect violation occurs. (Won't check for these during DMA.) |
| TIMING: | The address bus is driven with the assertion of MEMGO- during a DMA transfer and during an interrupt cycle. In addition, the processor drives the address bus and asserts MEMGO when accessing the boot ROM. |
| NOTE: | The default address bus driver is the processor card, which drives the address bus at all times except the following: <ol style="list-style-type: none">1) During the assertion of IAK-.2) During the assertion of MRQ-.3) From the assertion of BUSY- until the first SCLK-↓ after the release of BUSY-. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|---------------------|--|
| <p>BUSY-</p> | |
| FULL NAME: | Memory Busy (Tri-state, low true) |
| DRIVEN BY: | Processor and Memory cards |
| RECEIVED BY: | Processor and interface cards |
| FUNCTION: | BUSY- is asserted by the memory to indicate that it is unable to begin a new cycle. BUSY- is asserted by the processor when an instruction is being fetched from the boot ROM. |
| TIMING: | BUSY- is asserted after the rising edge of SCLK-, following the assertion of MEMGO-. BUSY- is released following the rising edge of SCLK- that precedes the next possible memory cycle by one cycle of SCLK-. BUSY- is asserted by the processor during a boot ROM access. |
| <p>CCLK-</p> | |
| FULL NAME: | Communications Clock (low true) |
| DRIVEN BY: | Processor card |
| RECEIVED BY: | Interface cards |
| FUNCTION: | This clock provides a fixed frequency which may be used to drive a state machine, or which may be divided down for baud rate generation. |
| TIMING: | 14.7456 MHz clock with a 50-percent duty cycle. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|---|
| COTURN- | |
| FULL NAME: | Coprocessor Turn |
| DRIVEN BY: | A coprocessor such as a microprocessor interfaced to an L-Series backplane. |
| RECEIVED BY: | Expanded (XL) Memory Controller |
| FUNCTION: | Asserted during MRQ to tell the memory card to use the the processor map. COTURN- may be asserted while MRQ- is high to tell the memory card to use the DMA relocation registers. |
| TIMING: | COTURN must be asserted one state before MEMGO- and released with MEMGO. |
| CPUTURN- | |
| FULL NAME: | Processor Turn |
| DRIVEN BY: | Processor Card |
| RECEIVED BY: | All interface cards |
| FUNCTION: | Asserted during RNI- and in addition, in order to signal that the processor card requests backplane priority. The assertion of CPUTURN- inhibits all interface cards from reasserting MRQ- once all current requests are satisfied. |
| TIMING: | When the processor wants to get out on the backplane for any one of three reasons (accessing memory, acknowledging an interrupt, or participating in an I/O handshake) but is held off by DMA, a counter counts 32 MEMGOs before asserting CPUTURN. CPUTURN stays asserted until the processor starts its transaction on the backplane. |

Table 6-37. Backplane Signal Definitions (Continued)

CRS-

FULL NAME: Control Reset (low true)

DRIVEN BY: Processor Card

RECEIVED BY: All cards

FUNCTION: The assertion of CRS- completely resets the I/O system. All of the following will occur:

1. All interface control flip-flops will be cleared.
2. All interface flag flip-flops will be cleared.
3. All pending interrupts will be cleared except power fail.
4. The interrupt system will be turned off.
5. The global register will be disabled.
6. Power fail interrupts will be enabled.
7. Parity interrupts will be enabled.
8. TBC flag and control will be cleared and any pending TBC interrupt will be cleared.
9. Memory protect will be turned off and any pending memory protect interrupts will be cleared (this is only important in the boot mode, where memory protect interrupts are suppressed).
10. Parity valid LED on memory card will be turned on.

In addition, each interface card interprets CRS- to perform its own various test functions.

TIMING: CRS- is asserted for one cycle of SCLK- when a CLC 0 instruction is executed.

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|----------------|---|
| (DB0+)-(DB15+) | |
| FULL NAME: | Data Bus 0-15 (Tri-state, high true) |
| DRIVEN BY: | Any memory or interface card or the processor card. |
| RECEIVED BY: | Any memory or interface card or the processor card. |
| FUNCTION: | DB0 to 15, of which DB0+ is the least significant bit, are used for all system data transfers. |
| TIMING: | An interface card will drive the data bus during the assertion of MEMGO- on a DMA write. The RAM card drives the data bus on a read cycle for one cycle, during the assertion of VALID-. The processor card drives the data bus with the assertion of MEMGO- on a memory write (STA), with IOGO- on an I/O write (OTA), and with VALID- clocked by start of long half-cycle on A or B fetch or Boot Read. |
| FCLK- | |
| FULL NAME: | Fast clock |
| DRIVEN BY: | Processor card |
| RECEIVED BY: | Memory card |
| FUNCTION: | FCLK- is exactly five times the frequency of SCLK- and is used by the memory to synchronize various backplane functions. |
| TIMING: | FCLK- is a 50-percent duty cycle clock with a maximum frequency of 22.016 MHz. FCLK- is in synchronization with SCLK- such that a positive edge of FCLK- accompanies every transition of SCLK-. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|--|
| IAK- | |
| FULL NAME: | Interrupt Acknowledge (low true) |
| DRIVEN BY: | Processor card |
| RECEIVED BY: | Any interrupting card |
| FUNCTION: | Asserted to signal that an interrupt request is about to be serviced and to freeze the interrupt priority chain. |
| TIMING: | IAK- is asserted by the processor card following the start of the short half cycle of SCLK-. It is held until after the trap cell instruction has commenced. (BUSY-↓ causes IAK-↑.) |
| ICHID- | |
| FULL NAME: | Interrupt Chain In Disable (low true) |
| DRIVEN BY: | The next higher priority card, to whom this signal is ICHOD-. |
| RECEIVED BY: | All interface cards |
| FUNCTION: | See ICHOD- |
| TIMING: | See ICHOD- |
| NOTE: | See ICHOD- |
| ICHOD- | |
| FULL NAME: | Interrupt Chain Out Disable (low true) |
| DRIVEN BY: | All interface cards, and the processor card (which is the top of the chain). |
| RECEIVED BY: | The next lower priority card, to whom this signal is ICHID-. |
| FUNCTION: | Asserted to disable lower priority cards from interrupting. A high on this line keeps interrupt generation enabled. ICHOD- is part of the ICHID-/ICHOD- daisy chain, used to determine interrupt priority. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--|---|
| <p>TIMING:</p> | <p>Asserted by an interface card when its ICHID line goes low, or when its FLAG and CONTROL flip-flops get set. De-asserted when ICHID⁻ goes high, and on either a CLF, CLC or PON⁺. Asserted by processor card on power fail, memory protect, parity error, UIT or TBG interrupts.</p> |
| <p>INTRQ⁻</p> <p>FULL NAME:</p> <p>DRIVEN BY:</p> <p>RECEIVED BY:</p> <p>FUNCTION:</p> <p>TIMING:</p> | <p>Interrupt Request (open-collector, low true)</p> <p>All interface cards</p> <p>Processor card</p> <p>Asserted to signal an interrupt request, and held low until the interrupt gets service, until PON⁺ goes low, or until a CLC 0 is executed.</p> <p>Asserted by an interface card when both its CONTROL and FLAG flip-flops are set and its ICHID⁻ signal is high. De-asserted when the CONTROL or FLAG flip-flop is cleared, or 2 cycles after the assertion of IAK⁻ while ICHID⁻ is high.</p> |
| <p>ILOGO⁻</p> <p>FULL NAME:</p> <p>DRIVEN BY:</p> <p>RECEIVED BY:</p> <p>FUNCTION:</p> <p>TIMING:</p> <p>NOTE:</p> | <p>I/O Handshake Request Acknowledge (low true)</p> <p>Processor card</p> <p>All interface cards</p> <p>Asserted to signal that the processor card is ready to receive a command or send or receive an operand from an interface card. De-asserted when the transfer has been completed.</p> <p>Pulled low when the data bus is available for transfers and released as soon as the data has been clocked off the backplane.</p> <p>For some types of I/O transfers, this signal will participate in a double handshake. See paragraph 6.4.2.</p> |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|--|
| IORQ- | |
| FULL NAME: | I/O Handshake Request (open collector, low true) |
| DRIVEN BY: | All interface cards |
| RECEIVED BY: | Processor card |
| FUNCTION: | Asserted to signal that an interface requires processor service, and de-asserted when being serviced. |
| TIMING: | Asserted within 2 cycles after the rising edge of RNI-, or, in slave mode (see paragraph 6.4.8) on the next rising edge of SCLK- after SCHID- goes high. De-asserted to signal that data will be valid on the second rising edge of SCLK-, or during an input, to signal that data has just been latched. See paragraph 6.4.7. |
| NOTE: | For some types of I/O transfers, this signal will participate in a double handshake. See paragraph 6.4.7. |
| MCHID- | |
| FULL NAME: | Memory Chain In Disable (low true) |
| DRIVEN BY: | The next higher priority card, to whom this signal is MCHOD-. |
| RECEIVED BY: | All interface cards |
| FUNCTION: | Asserted to disable initiation of a memory cycle. |
| TIMING: | MCHID- is asserted a maximum of one cycle after MRQ- goes low. Released as soon as memory cycle of higher priority device is complete. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|--|
| MCHOD- | |
| FULL NAME: | Memory Chain Out Disable (low true) |
| DRIVEN BY: | All interface cards and processor card. |
| RECEIVED BY: | The next lower priority card, to whom this signal is MCHID-. |
| FUNCTION: | Asserted to disable all lower priority cards from initiating a memory cycle. |
| TIMING: | An interface card wanting a DMA cycle asserts MCHOD- at the end of the short half cycle of SCLK-. MCHOD- is de-asserted at the end of the short half cycle, following the assertion of BUSY-. The processor card is the top of this priority chain. MCHOD- is tied high on the processor card. |
| NOTE: | All cards not using the memory priority chain must connect MCHOD- to MCHID-. |
| MCHODOC- | |
| FULL NAME: | Memory Chain Out Disable Open Collector (open collector, low true) |
| DRIVEN BY: | All interface cards |
| RECEIVED BY: | Head of priority chain on lower priority stack. |
| FUNCTION: | Used as look-ahead for the memory priority chain. If any interface card in the higher priority stack asserts MCHODOC-, all interface cards in the lower priority stack will become disabled from initiating a memory cycle. |
| TIMING: | An interface card wanting a DMA cycle asserts MCHODOC- at the end of the short half cycle of SCLK-. MCHODOC- is released at the end of the short half cycle, following the assertion of BUSY-. |
| NOTE: | As far as the output of any given interface card is concerned, MCHODOC- is logically identical to MCHOD-. |
| | The pull-up resistor on this line is located on the 2 by 8 backplane. The two smaller backplane configurations are not large enough to require look-ahead in the memory priority chain, so this line is not terminated in these smaller configurations. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|--|
| MEMDIS- | |
| FULL NAME: | Memory Disable (low true) |
| DRIVEN BY: | Processor card |
| RECEIVED BY: | Memory card |
| FUNCTION: | To disable memory during a boot access. |
| TIMING: | Asserted with MEMGO-. |
| NOTE: | MEMDIS- is not bussed up and down the backplane, instead, it runs above the SLAVE- chain (see PS- signal). |
| MEMGO- | |
| FULL NAME: | Memory Cycle Initiation (open collector, low true) |
| DRIVEN BY: | Processor and interface cards. |
| RECEIVED BY: | Memory, processor, and interface cards. |
| FUNCTION: | Pulled low to signal a memory request and released once service begins. |
| TIMING: | MEMGO- may be asserted by the card wishing to initiate a memory cycle after the falling edge of SCLK- that follows the release of BUSY-. MEMGO- is released by the processor card after the assertion of BUSY-. MEMGO- is released by an interface card after being held low for one cycle of SCLK-. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|---|
| MLOST- | |
| FULL NAME; | Memory Lost (open collector, low true) |
| DRIVEN BY: | Processor, memory, and battery back-up card |
| RECEIVED BY: | Processor card |
| FUNCTION: | MLOST- is asserted by the battery back-up card to indicate that memory power was lost when system power last went down. Memory will then be cleared on the next power up. In a case where there is no back-up supply for the memory, MLOST- can be grounded. This may be accomplished by a switch setting on the processor card which grounds MLOST-, or by a switch setting on the memory card which shorts +5V to +5M and grounds MLOST-. |
| TIMING: | Asserted as soon as memory power fails. Released 10 msec after the rising edge of PON+. |
| MP+ | |
| FULL NAME: | Memory Protect (open collector, high true) |
| DRIVEN BY: | Processor card |
| RECEIVED BY: | All interface cards |
| FUNCTION: | MP+ is asserted to indicate that the memory protect system is on. When MP+ is high, all I/O interface cards are inhibited from recognizing I/O instructions. DMA is not affected. |
| TIMING: | MP+ is asserted after an STC 05 instruction. It is released when IAK- is asserted, but re-asserted if an I/O group instruction is in the trap cell. MP+ is always in the proper state before RNI- is asserted and does not change until the next instruction fetch is initiated. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|------|---|
| MRQ- | <p>FULL NAME: Memory Request (open collector, low true)</p> <p>DRIVEN BY: All interface cards</p> <p>RECEIVED BY: Processor card</p> <p>FUNCTION: Asserted to indicate that an interface card performing DMA has requested a memory cycle. When MRQ- is low, the processor card is inhibited from requesting a memory cycle.</p> <p>TIMING: An interface card wanting a DMA cycle asserts MRQ- at the start of the long half cycle of SCLK-. MRQ- is de-asserted on the falling edge of SCLK- after the assertion of BUSY-.</p> |
| PE- | <p>FULL NAME: Parity Error (open collector, low true)</p> <p>DRIVEN BY: Memory card.</p> <p>RECEIVED BY: Processor and interface cards.</p> <p>FUNCTION: Asserted if last memory read produced a parity error.</p> <p>TIMING: PE- is asserted for one short half cycle after the release of VALID-.</p> |
| PFW- | <p>FULL NAME: Power Fail Warning (open collector, low true)</p> <p>DRIVEN BY: Power supply</p> <p>RECEIVED BY: Processor card and battery back-up card</p> <p>FUNCTION: Asserted to signal an AC line voltage failure.</p> <p>TIMING: Asserted at least 5 msec before the fall of PON+. Released before the rise of PON+.</p> <p>NOTE: The pull-up resistor on this open collector line is located on the processor card.</p> |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|---|
| PON+ | |
| FULL NAME: | Power On (open collector, high true) |
| DRIVEN BY: | Power supply and processor. |
| RECEIVED BY: | All cards in system. |
| FUNCTION: | PON+ is asserted by the power supply shortly after all power supply voltages are stable, to allow time for initialization on individual system cards. It is also pulsed low by a momentary switch located on the processor card in order to reset the computer. |
| TIMING: | Asserted 1 msec after all power supplies are stable. De-asserted if any supply falls below a tolerable level. |

Table 6-37. Backplane Signal Definitions (Continued)

PS-

FULL NAME: Parity Sense

DRIVEN BY: Processor card.

RECEIVED BY: Memory card.

FUNCTION: A high level on PS- causes memory to generate and detect odd parity. A low on PS- causes memory to generate and detect even parity.

TIMING: The level of PS- is selected by flag 5. An STF 5 selects even parity and a CLF 5 selects odd parity.

NOTE: On power up, PS- is set for odd parity. Also note that PS- is not bussed up and down the backplane. Instead, it is sent by the processor card only to the memory card located above it. See figure below.

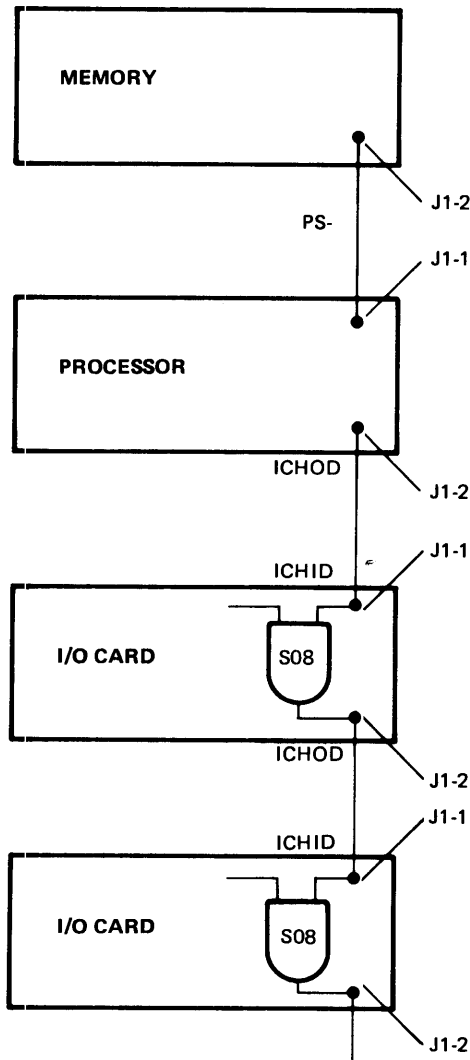


Table 6-37. Backplane Signal Definitions (Continued)

| | |
|---|--|
| RCLK+ | |
| FULL NAME: | Refresh Clock |
| DRIVEN BY: | Processor card |
| RECEIVED BY: | Memory |
| FUNCTION: | RCLK+ is a fixed frequency clock, in synchronization with SCLK-. RCLK+ is used by the refresh counter on the memory card to determine how often to refresh. |
| TIMING: | RCLK+ is the complement of SCLK-, when SCLK- has a 227 nsec cycle. |
| NOTE | |
| RCLK+ is not bussed up and down the backplane; instead, it is above the MCHOD priority chain. | |
| REMEM- | |
| FULL NAME: | Remote Memory (open collector, low true) |
| DRIVEN BY: | Interface cards |
| RECEIVED BY: | Memory |
| FUNCTION: | REMEM- is asserted to indicate that the simultaneous MEMGO- which occurs should initiate a memory cycle with the remote memory. Any memory card in the system should ignore MEMGO- if it occurs with REMEM-. |
| TIMING: | REMEM- is asserted and released with MEMGO-. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|-----------------|--|
| RNI- | |
| FULL NAME: | Read Next Instruction (low true) |
| DRIVEN BY: | Processor card. |
| RECEIVED BY: | All interface cards. |
| FUNCTION: | RNI- is asserted to indicate that the current memory cycle is a fetch and that an instruction will be on the data bus. |
| TIMING: | RNI- is asserted with the fetch address. It is released after the start of the short half cycle of SCLK- after VALID- is asserted. |
| NOTE: | The instruction is to be latched on the trailing (rising) edge of RNI-. |
| (SC0+) - (SC4+) | |
| FULL NAME: | Address Extension Bus 0 - 4 |
| DRIVEN BY: | Interface Cards |
| RECEIVED BY: | XL Memory Controller |
| FUNCTION: | The SC bus is used by I/O interfaces performing DMA to select one of thirty-two DMA relocation (offset) registers of the XL mapped extended memory controller. |
| TIMING: | The Address Extension Bus is driven simultaneously with ABO - AB14. |
| SC5 | |
| FULL NAME: | Self Configure |
| DRIVEN BY: | Interface Cards |
| RECEIVED BY: | XL Memory Contgroller |
| FUNCTION: | SC5+ is asserted to indicate that DMA self-configuration is occurring. The XL memory controller disables the DMA relocation registers during DMA self-configuration. |
| TIMING: | SC5+ is driven simultaneously with ABO - AB14. |

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|---|
| SCHID- | |
| FULL NAME: | Slave Chain In Disable (low true) |
| DRIVEN BY: | The next higher priority card, to whom this signal is SCHOD-. |
| RECEIVED BY: | All interface cards |
| FUNCTION: | See SCHOD- |
| TIMING: | See SCHOD- |
| SCHOD- | |
| FULL NAME: | Slave Chain Out Disable (low true) |
| DRIVEN BY: | All interface cards |
| RECEIVED BY: | The next lower priority card, to whom this signal is SCHID-. |
| FUNCTION: | SCHOD- is asserted to disable lower priority cards from entering slave mode. SCHOD- is part of the SCHID-/SCHOD- priority chain, used to settle conflicts for slave mode processing (see paragraph 6.4.8). |
| TIMING: | SCHOD- is asserted with SLAVE-, or if a higher priority card pulls on SCHID-, and is held as long thereafter as it takes the daisy chain to ripple down. Likewise, SCHOD- is released with SLAVE- or SCHID-. |
| NOTE: | The top of the priority chain is the processor card. Whenever SLAVE- is asserted, and the processor card has completed executing the current instruction, SCHOD- goes high for one cycle of SCLK-. |
| | There must be exactly one non-inverting Schottky gate on each card between SCHID- and SCHOD-. Example: |
| | <p>The diagram shows a 74S08 Schottky gate symbol. A horizontal line labeled 'SCHID-' enters the gate from the left. Another horizontal line labeled 'SCHOD-' exits the gate to the right. The gate symbol is a D-shaped component with a small circle on its left side, indicating a Schottky gate. Below the gate symbol is the text '74S08'.</p> |

Table 6-37. Backplane Signal Definitions (Continued)

SCLK-

FULL NAME: Slow clock

DRIVEN BY: Processor card

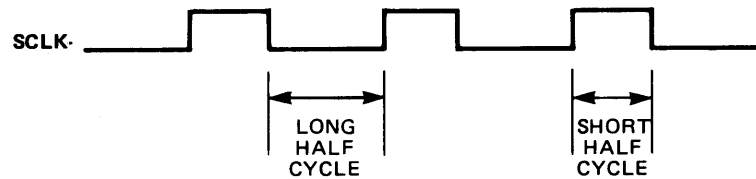
RECEIVED BY: All system cards

FUNCTION: SCLK- is used to synchronize many diverse system signal interactions.

TIMING: SCLK- is a derivative of FCLK. It is generated with a divide-by-5 circuit which produces a signal with a minimum of a 227.1 nsec period and a 40-percent duty cycle.

NOTE 1: In all timing descriptions, the term "short half-cycle" refers to the time ($2/5$ period) when SCLK- is high. The "long half-cycle" refers to the $3/5$ period when SCLK- is low.

So as to minimize clock skew, all cards are required to receive SCLK- into an S240.



NOTE 2: Although SCLK- typically has a 227.1 nsec period, it slows to 454.2 nsec during the assertion of IOG0- on the backplane, in order to permit the processor to handshake with the interface cards.

Table 6-37. Backplane Signal Definitions (Continued)

| | |
|--------------|--|
| SLAVE- | |
| FULL NAME: | Slave Request (open collector, low true) |
| DRIVEN BY: | Interface cards |
| RECEIVED BY: | Processor card |
| FUNCTION: | SLAVE- is asserted to request the processor to enter slave mode, i.e., to force the processor to enter an I/O handshake. |
| TIMING: | SLAVE- is held asserted until the start of the long half cycle of SCLK- following the release of SCHID-. |
| | |
| SPRQ- | |
| FULL NAME: | Special Interrupt |
| DRIVEN BY: | 64kByte RAM/ROM/STACK card for HP 1000 A-Series Automation Processor. |
| RECEIVED BY: | Processor card |
| FUNCTION: | SPRQ- is asserted in order to request an interrupt. This interrupt has higher priority than I/O interrupts or power fail interrupt. Its priority is only exceeded by parity error and unimplemented instruction trap interrupts. |

Table 6-37. Backplane Signal Definitions (Continued)

| |
|---|
| <p>VALID-</p> <p>FULL NAME: Data Valid (Tri-state, low true)</p> <p>DRIVEN BY: Processor and memory cards</p> <p>RECEIVED BY: Processor and interface cards</p> <p>FUNCTION: VALID- is asserted to signal that the data on the data bus is about to become valid during a memory read cycle.</p> <p>TIMING: On a read cycle, the memory will assert VALID- after the rising edge of SCLK- that precedes the appearance of valid data on the backplane by one cycle. VALID- will be held low for one cycle and then released on the rising edge of SCLK- right after data becomes valid. The processor card asserts VALID- during a boot ROM read for one cycle synchronized to the start of the short half cycle. VALID- is also asserted during write.</p> |
| <p>WE-</p> <p>FULL NAME: Write Enable (Tri-state, low true)</p> <p>DRIVEN BY: Any card accessing memory</p> <p>RECEIVED BY: Memory card</p> <p>FUNCTION: WE- is asserted to signal a memory write, and held high to signal a memory read.</p> <p>TIMING: WE- is asserted and released with (AB0+)-(AB14+).</p> |

6.7 PARTS LOCATIONS

Parts locations for the backplanes are shown in figures 6-3 through 6-5.

6.8 PARTS LIST

The parts list for the backplanes is shown in table 6-38. Refer to table 6-39 for the names and addresses of manufacturers of the parts.

Table 6-38. Backplane Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--------------------------------------|----------|------------------|
| | 02145-60001 | 1 | 1 | 16-gLOT BACKPLANE | 20480 | 02145-60001 |
| CR1 | 1902-0939 | 9 | 1 | DIODE-ZNR 5V PD=5W TC=+.06% IR=300UA | 11961 | 1N5908 |
| CR2 | 1902-0941 | 3 | 2 | DIODE-ZNR 12V PD=5W TC=+.084% IR=2UA | 11961 | 1.58E15A |
| CR3 | 1902-0941 | 3 | 3 | DIODE-ZNR 12V PD=5W TC=+.084% IR=2UA | 11961 | 1.58E15A |
| R1 | 0698-3444 | 1 | 1 | RESISTOR 310 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-310H-F |
| R2 | 0698-3441 | 8 | 1 | RESISTOR 215 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-215R-F |
| | 1251-4573 | 4 | 32 | CONNECTOR-PC EDGE 25-CONT/ROW 2-ROW8 | 20480 | 1251-4573 |
| | 1251-5668 | 0 | 2 | CONNECTOR 10-PIN F POST TYPE | 20480 | 1251-5668 |
| | 1251-5670 | 4 | 1 | CONNECTOR 4-PIN F POST TYPE | 20480 | 1251-5670 |
| | 12030-60002 | 5 | 1 | C.C. BACKPLANE | 20480 | 12030-60002 |
| CR1 | 1902-0941 | 3 | 2 | DIODE-ZNR 12V PD=5W TC=+.084% IR=2UA | 11961 | 1.58E15A |
| CR2 | 1902-0939 | 9 | 1 | DIODE-ZNR 5V PD=5W TC=+.06% IR=300UA | 11961 | 1N5908 |
| CR3 | 1902-0941 | 3 | 3 | DIODE-ZNR 12V PD=5W TC=+.084% IR=2UA | 11961 | 1.58E15A |
| | 1251-4573 | 4 | 20 | CONNECTOR-PC EDGE 25-CONT/ROW 2-ROW8 | 20480 | 1251-4573 |
| | 1251-5668 | 0 | 2 | CONNECTOR 10-PIN F POST TYPE | 20480 | 1251-5668 |
| | 1251-5670 | 4 | 1 | CONNECTOR 4-PIN F POST TYPE | 20480 | 1251-5670 |
| | 12032-60001 | 6 | 1 | C.C. BACKPLANE | 20480 | 12032-60001 |
| CR1 | 1902-0941 | 3 | 2 | DIODE-ZNR 12V PD=5W TC=+.084% IR=2UA | 11961 | 1.58E15A |
| CR2 | 1902-0939 | 9 | 1 | DIODE-ZNR 5V PD=5W TC=+.06% IR=300UA | 11961 | 1N5908 |
| CR3 | 1902-0941 | 3 | 3 | DIODE-ZNR 12V PD=5W TC=+.084% IR=2UA | 11961 | 1.58E15A |
| J3 | 0360-1970 | 9 | 1 | BARRIER BLOCK 8-TERM PC BOARD NYL | 89020 | 888408 |
| | 1251-4573 | 4 | 10 | CONNECTOR-PC EDGE 25-CONT/ROW 2-ROW8 | 20480 | 1251-4573 |

Table 6-39. Manufacturer's Code List

| The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements. | | | | | |
|--|--|-----------------------|----------|-------------------------------------|-------------------------|
| CODE NO. | MANUFACTURER | ADDRESS | CODE NO. | MANUFACTURER | ADDRESS |
| C0633 | Aktiebolaget Rifa | Bromma, SE | 17856 | Siliconix Inc. | Santa Clara, CA 95054 |
| H9027 | Schurter A G H | Luzern, SW | 18324 | Signetics Corp. | Sunnyvale, CA 94086 |
| 0003J | Nippon Electric Co. | | 24546 | Corning Glass Works (Bradford) | Bradford, PA 16701 |
| 00853 | Sangamo Elec. Co. South Carolina Div. | Pickens, SC 29671 | 27014 | National Semiconductor Corp. | Santa Clara, CA 95051 |
| 01121 | Allen-Bradley Co. | Milwaukee, WI 53204 | 27777 | Varo Semiconductor Inc. | Gardland, TX 75040 |
| 01295 | Texas Instr Inc. Semiconductor CMPNT Div. | Dallas, TX 75222 | 28480 | Hewlett-Packard Co. Corporate Hq | Palo Alto, CA 94304 |
| 0192B | RCA Corp Solid State Div. | Sommerville, NJ 08876 | 32293 | Intersil Inc. | Cupertino, CA 95014 |
| 02111 | Spectrol Electronics Corp. | City Of Ind, CA 91745 | 34344 | Motorola Inc. | Franklin Park, IL 60131 |
| 03508 | GE Co. Semiconductor Prod. Dept. | Syracuse, NY 13201 | 50364 | Monolithic Memories Inc | Sunnyvale, CA 94086 |
| 04713 | Motorola Semiconductor Products | Phoenix, AZ 85062 | 56289 | Sprague Electric Co. | North Adams, MA 01247 |
| 07263 | Fairchild Semiconductor Div. | Mt. View, CA 94042 | 75042 | TRW Inc. Philadelphia Div. | Philadelphia, PA 19108 |
| 11236 | CTS Of Berne Inc. | Berne, IN 46711 | 89020 | Amerace Corp Control Prod. Div. | Union, NJ 07086 |
| 11961 | Semicon Inc. | Burlington, MA 01803 | 91506 | Augat Inc. | Attleboro, MA 02703 |
| 13606 | Sprague Elect Co. Semiconductor Div. | Concord, NH 03301 | | | |

| | |
|-------------------------|-------------|
| POINT-OF-LOAD REGULATOR | SECTION VII |
|-------------------------|-------------|

7.1 INTRODUCTION

The point-of-load regulator (part no. 02145-60002) in the HP 1000 L-Series computer system provides dc voltages for the HP 7902A Flexible Disc Drive. The input to the point-of-load regulator is a 25-kHz output voltage of the system power supply.

7.2 SPECIFICATIONS

REGULATION:

| | |
|------|-------|
| +5V | +/-5% |
| +12V | +/-5% |
| -12V | +/-6% |

OUTPUT CURRENT (MAX.):

| | |
|------|--------|
| +5V | 4 Amps |
| +12V | 3 Amps |
| -12V | 3 Amps |

OVER VOLTAGE PROTECTION: +20%

OVER CURRENT PROTECTION: 5 Amps

7.3 THEORY OF OPERATION

A general discussion of typical circuits that can be used to develop dc voltages from the system power supply's 25-kHz voltage is given in Appendix B of this document.

The schematic diagram of the point-of-load regulator is located at the rear of this section. Transformer T1 receives the 25-kHz voltage from the system power supply and provides three outputs which are rectified and applied to three voltage regulators. The +12-Vdc regulator, U2, does not have a reference input and requires a +15-Vdc input in order to provide a regulated output of +12 Vdc. High-speed zener diode CR11 clamps the output of U2 at +12 Vdc. The circuitry for the +5-Vdc regulated output is essentially the same as that for the +12-Vdc output. (Note that the input to U1 must be +8 Vdc.) Voltage regulator U3, however, does have a reference input and the reference voltage is provided via the divider consisting of resistors R1 and R2. Normally, the voltage supplied by T1 to U3 is -15 Vdc. Zener diode CR9 clamps the output of U3 at -12 Vdc.

7.4 PARTS LOCATIONS

Parts locations for the point-of-load regulator are shown in figure 7-1.

7.5 PARTS LIST

The parts list for the point-of-load regulator is given in table 7-1. Refer to table 6-39 for the names and addresses of manufacturers of the parts.

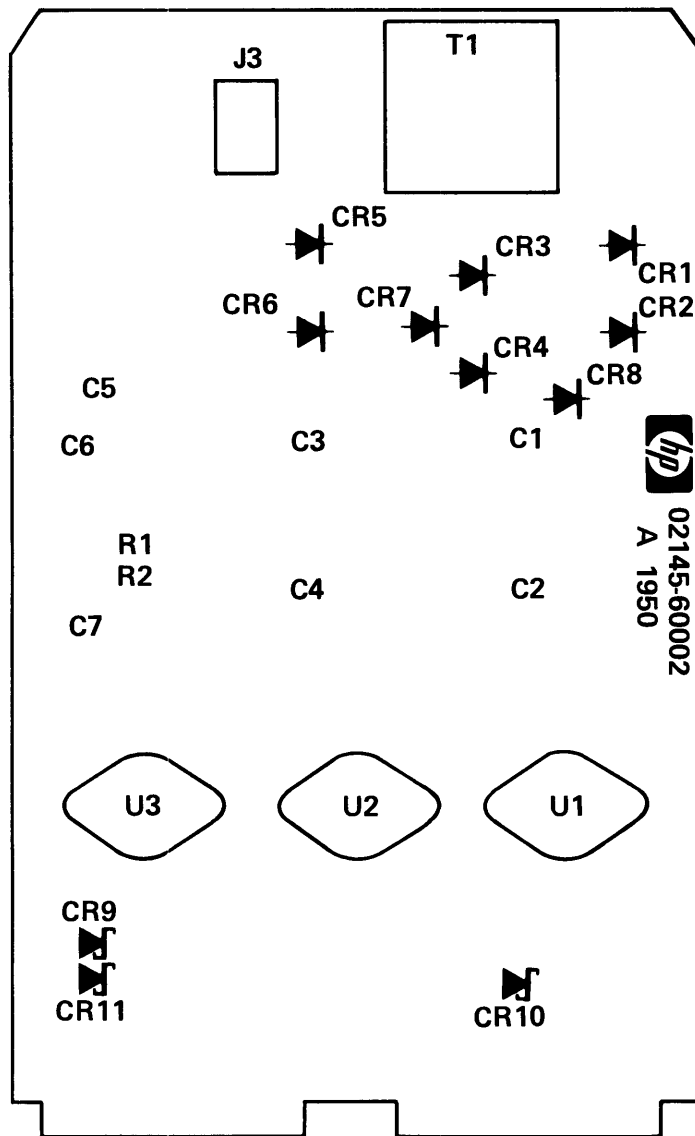
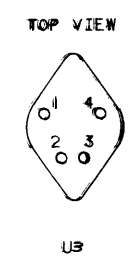
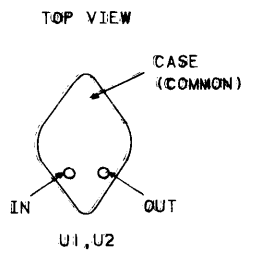
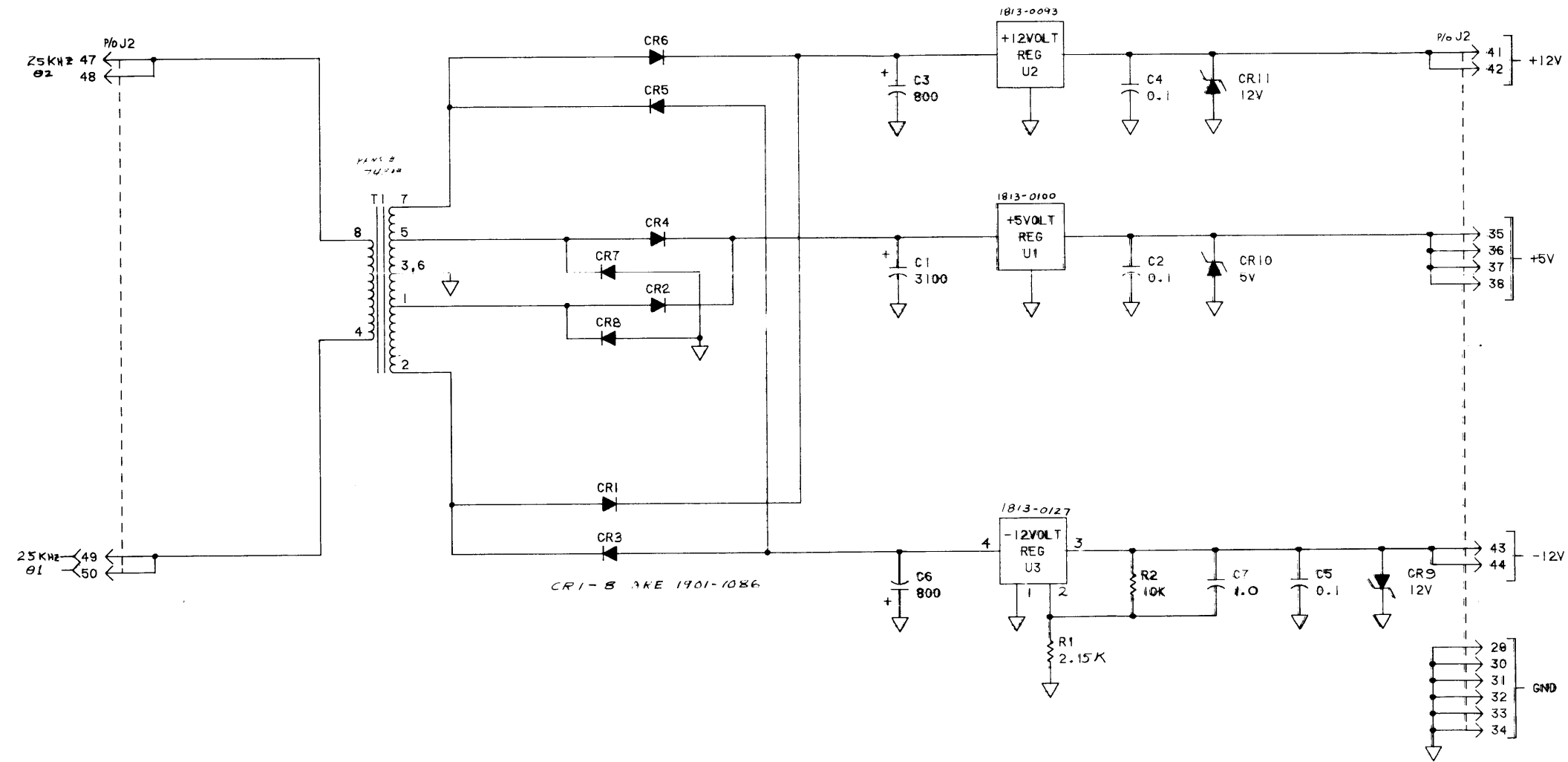


Figure 7-1. Point-of-Load Regulator Parts Locations

Table 7-1. Point-of-Load Regulator Parts List

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|---------------------------------------|----------|------------------|
| | 02145-00002 | 2 | 1 | PNT OF LOAD REGISTER | 28480 | 02145-00002 |
| C1 | 0180-2706 | 9 | 1 | CAPACITOR=FXD 3100UF+75-10% 16VDC AL | 00853 | 300JJ312U016B |
| C2 | 0160-4835 | 7 | 3 | CAPACITOR=FXD .1UF +/-10% 50VDC CER | 28480 | 0160-4835 |
| C3 | 0180-2724 | 3 | 2 | CAPACITOR=FXD 800UF+75-10% 40VDC AL | 00853 | 300MJ801U040B |
| C4 | 0160-4835 | 7 | | CAPACITOR=FXD .1UF +/-10% 50VDC CER | 28480 | 0160-4835 |
| C5 | 0160-4835 | 7 | | CAPACITOR=FXD .1UF +/-10% 50VDC CER | 28480 | 0160-4835 |
| C6 | 0180-2724 | 3 | | CAPACITOR=FXD 800UF+75-10% 40VDC AL | 00853 | 300MJ801U040B |
| C7 | 0160-4844 | 8 | 1 | CAPACITOR=FXD 1UF +/-80-20% 50VDC CER | 28480 | 0160-4844 |
| CR1 | 1901-1086 | 7 | 8 | DIODE=PNR RECT 50V 5A 200NS | 04713 | MR820 |
| CR2 | 1901-1086 | 7 | | DIODE=PNR RECT 50V 5A 200NS | 04713 | MR820 |
| CR3 | 1901-1086 | 7 | | DIODE=PNR RECT 50V 5A 200NS | 04713 | MR820 |
| CR4 | 1901-1086 | 7 | | DIODE=PNR RECT 50V 5A 200NS | 04713 | MR820 |
| CR5 | 1901-1086 | 7 | | DIODE=PNR RECT 50V 5A 200NS | 04713 | MR820 |
| CR6 | 1901-1086 | 7 | | DIODE=PNR RECT 50V 5A 200NS | 04713 | MR820 |
| CR7 | 1901-1086 | 7 | | DIODE=PNR RECT 50V 5A 200NS | 04713 | MR820 |
| CR8 | 1901-1086 | 7 | | DIODE=PNR RECT 50V 5A 200NS | 04713 | MR820 |
| CR9 | 1902-0941 | 3 | 2 | DIODE=ZNR 12V PD=5W TC=+.084% IR=2UA | 11961 | 1.58E15A |
| CR10 | 1902-0939 | 9 | 1 | DIODE=ZNR 5V PD=5W TC=+.06% IR=300UA | 11961 | 1N5908 |
| CR11 | 1902-0941 | 3 | | DIODE=ZNR 12V PD=5W TC=+.084% IR=2UA | 11961 | 1.58E15A |
| J3 | 1251-3819 | 9 | 1 | CONNECTOR 6-PIN M UTILITY | 28480 | 1251-3819 |
| R1 | 0698-0084 | 9 | 1 | RESISTOR 2.15K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-2151-F |
| R2 | 0757-0442 | 9 | 1 | RESISTOR 10K 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-1002-F |
| T1 | 9100-2626 | 3 | 1 | TRANSFORMER INVERTER; PRI; 14 TURNS | 28480 | 9100-2626 |
| U1 | 1813-0100 | 7 | 1 | IC V RGLTR TO-3 | 07263 | UA78H05KC |
| U2 | 1813-0093 | 7 | 1 | IC V RGLTR TO-3 | 07263 | UA78H12KC |
| U3 | 1813-0127 | 8 | 1 | | 28480 | 1813-0127 |



| | | | |
|-------------------------|-----------|-----------------|---------------------|
| POINT OF LOAD REGULATOR | | HEWLETT PACKARD | |
| TITLE | 12000 D/E | PART NUMBER | 02145 - 60002 |
| NEXT ASSEMBLY | | SCALE | 0-02145 - 60002 -51 |

| | |
|-----------------|--------------|
| EXTENDED MEMORY | SECTION VIII |
|-----------------|--------------|

8.1 INTRODUCTION

The Expanded Memory hardware, or XL memory, for the 1000 L-Series Computers and Computer Systems consists of three circuit cards, the 12002A, the 12003A, and the 12002B. The 12002A contains the XL memory controller and a 128 Kbyte RAM array. The 12003A is an array board containing a 128 Kbyte RAM array which is controlled by the signals from the 12002A over the frontplane connector. Up to three 12003A cards may be used with the 12002A in order to provide up to 512 Kbytes of main memory in 128 Kbyte increments.

The 12002B is the XL memory controller with a 512 Kbyte RAM array. This high memory density on a card is achieved with the use of 64K RAM chips. The circuit cards are shown in figure 8-1. The 12002A and 12002B are identical in appearance except for jumper placement.

8.2 OVERVIEW

8.2.1 SYSTEM ENVIRONMENT

The system environment of the HP 1000 L-Series Computer system is shown in Section II, figure 2-2. The Extended Memory controller (12002A or 12002B) is subject to the same slot restrictions as the 64 Kbyte 12004A memory card:

- a. The XL memory controller card must be located in the next higher priority slot above the processor card.
- b. No I/O cards may be located above the XL memory controller.

Thus, the memory and processor occupy the highest priority slots in the backplane. These slots do not, however, need to be the highest slots in the backplane. Any slots can be used by the processor and memory as long as no I/O cards are located above the memory card(s). (See Section VI, figure 6-3 for slot priorities.)

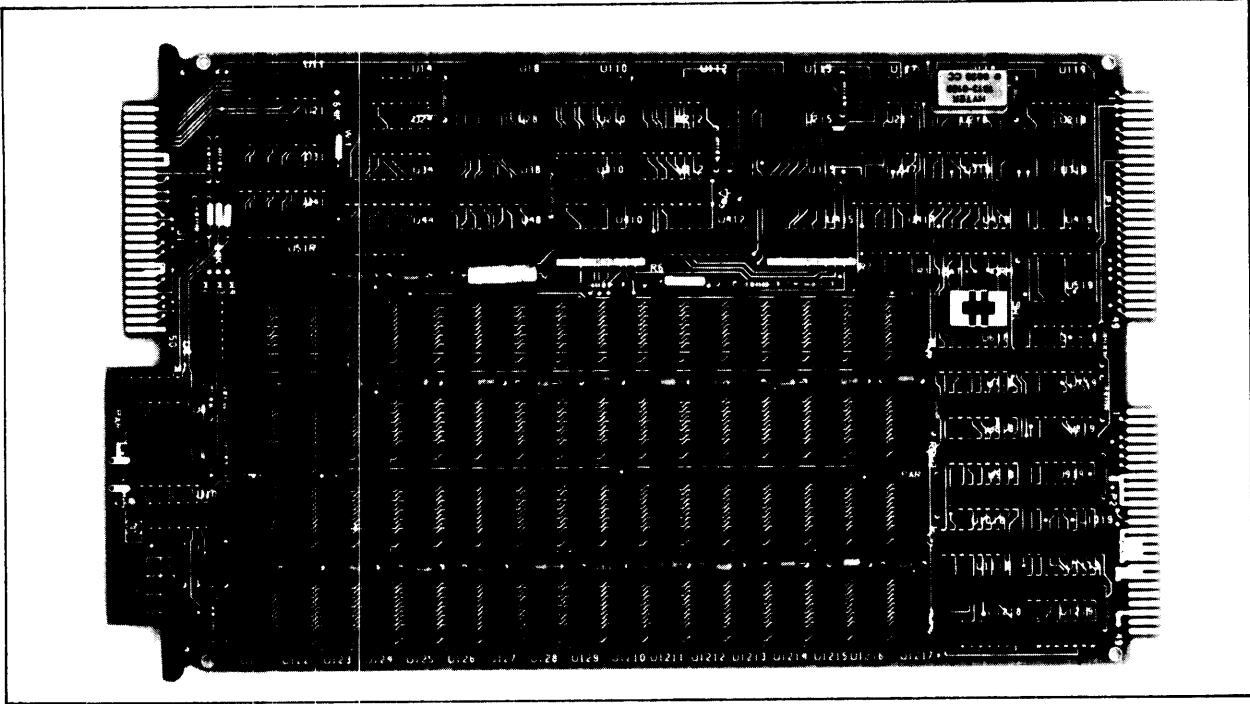


Figure 8-1A. 12002A Memory Card

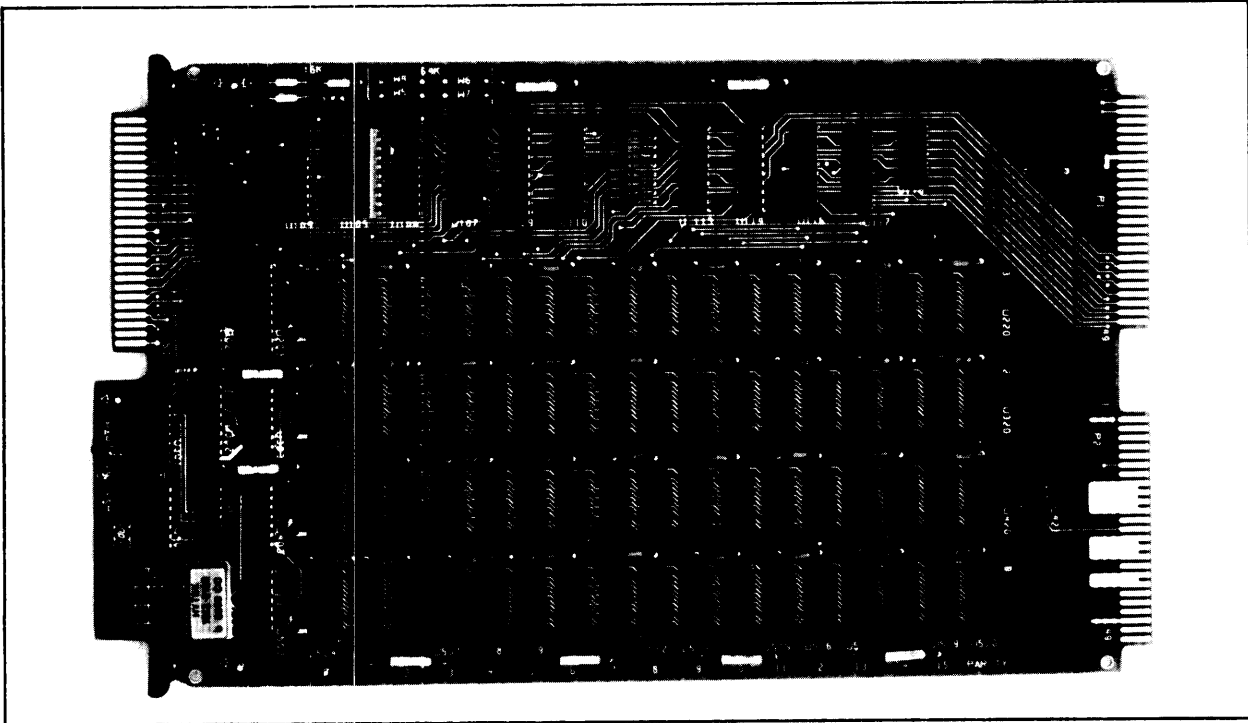


Figure 8-1B. 12003A Memory Card

The XL array cards (12003A) must occupy the backplane slots directly above the XL controller. If multiple array cards are used, they must occupy consecutive slots above the XL controller. When array cards are used, they must be connected to the XL memory controller by a frontplane connector. No modifications are needed to any of the array cards to select their relative position above the XL controller. All array cards operate in any position above the controller.

There are three frontplane connectors available. The 12028A is a two-connector frontplane used with 256 Kbytes of memory (one 12002A and one 12003A). The 12028B is a three-connector frontplane used with 384 Kbytes of memory (one 12002A and two 12003As). The 12028C is a four-connector frontplane used with 512K bytes of memory (one 12002A and three 12003As). The physical limitation of the frontplane connectors require that the XL memory controller and the XL memory array boards be located on the same side of the backplane when a side-by-side backplane, such as in the 2103L box, is used.

8.2.2 BASIC MEMORY OPERATION

The memory in the L-Series is always operating in one of four modes at any time; write cycle, read cycle, refresh cycle, or standby mode.

All memory accesses are either read cycles or write cycles and are initiated by an external device. When the backplane signal MEMGO- is asserted at the rising edge of SCLK-, the memory will initiate a memory access. For all accesses the XL controller card asserts BUSY- on the backplane to prevent other devices from requesting memory access. The controller also asserts VALID- on the backplane for one state at the completion of the access for all read cycles and write cycles. The rising edges of VALID- and BUSY- tell the cards in the system that the memory access has completed.

A read cycle is initiated when the backplane signal MEMGO- is asserted and the signal write enable (WE-) is not asserted at the rising edge of SCLK-. When BUSY- is asserted, the address bus is latched from the backplane and the memory controller starts a memory read cycle. The actual physical memory location accessed is determined by the latched backplane address, the latched extended address bus (SC0-SC4), the contents of the controller's map RAMs, and whether the access was initiated by the processor or by an I/O card.

At the end of the read cycle, the addressed memory card drives the backplane data bus with the requested data. The data is valid on the backplane at the rising edge of VALID-. If a parity error has occurred the controller card will also drive the PE- line on the backplane.

A write cycle is initiated when the backplane signals MEMGO- and Write Enable (WE-) are both asserted at the rising edge of SCLK-. When these conditions are met, the controller will initiate a memory write cycle. BUSY- is asserted, and the controller latches the address and data buses and proceeds to write the data to the correct memory location. The actual physical memory location to be accessed is determined in precisely the same manner as for a

read cycle, described above. VALID- is asserted on the backplane at the completion of the write cycle.

Refresh cycles are always initiated by the memory controller. All cards in the memory system perform a refresh at the same time. The controller card resolves all conflicts between memory accesses and refresh cycles and properly sequences the refreshing of all memory cards.

The memory can perform only one of the above operations at a time. When the memory is not being accessed or refreshed it is in the standby mode.

8.2.3 BASIC MAP CONTROL OPERATIONS

The XL memory is a mapped memory system. The XL controller has the capability of extending the 15-bit backplane address into an 18-bit physical address which can access up to 256K words of main memory.

The XL controller has two basic operating modes for processor memory accesses which are physical mode (unmapped) and logical mode (mapped). When the controller is in physical mode it allows the processor to access only the lowest 32K words in main memory. The exact address accessed is determined by the backplane address bus.

When the controller is in logical mode it allows the processor to access 32K words in memory, but the location of the 32K words in main memory is determined by the backplane address and the contents of the map RAMs.

The controller card contains the logic to recognize instructions which control the operating mode for processor accesses.

I/O accesses typically occur to main memory relative to a Relocation Register. The I/O card selects a specific Relocation Register to use for the DMA transfer. The contents of the Relocation Register have been previously loaded for use by the I/O card. This Relocation Register points to a position in main memory. From this position the I/O card then has access to the next higher 32K word contiguous block of memory. The exact address accessed is determined by the result of the addition of the backplane address to the contents of the selected Relocation Register.

I/O accesses will not occur relative to a Relocation Register under two conditions. If the I/O card asserts the Self Configure line (SC5) on the backplane the I/O transfer will occur to physical memory. If the I/O card drives the extended address bus (SC0-SC4) all low during an access, the transfer will occur to physical memory. In both cases the exact location in physical memory is determined directly by the backplane address bus.

The controller card provides the mechanism to write to the map RAMs located on the controller card. The map RAMs contain the 32 processor maps and the 32 Relocation Registers.

Section 8.3.4 contains a detailed description of the mapping operations on the XL controller.

8.2.4 POWER REQUIREMENTS

The XL memory hardware operates on +5V and +5M voltages only. The worst case power requirements for each card are listed below. The standby power requirements are valid during battery backup operation. The operating power requirements are for full bandwidth memory accessing.

| | | CURRENT | | POWER | |
|--------|-----|-----------|---------|-----------|---------|
| | | Operating | Standby | Operating | Standby |
| 12002A | +5V | 2.43A | 0.00 | 12.4W | 0.0 |
| | +5M | 0.63A | 0.42A | 3.2W | 2.1W |
| 12002B | +5V | 2.43A | 0.00 | 12.4W | 0.0 |
| | +5M | 1.00A | 0.62A | 5.1W | 3.2W |
| 12003A | +5V | 0.91A | 0.00 | 4.6W | 0.0 |
| | +5M | 0.46A | 0.26A | 2.3W | 1.3W |

8.2.5 POWER SUPPLY CONFIGURATION

The XL memory hardware operates with the power supply and battery backup options to provide the necessary memory voltages to the memory and processor cards. A slide switch, located near the back of the XL controller card, is used to select between NORMAL operation and BATTERY backup operation.

With the slide switch set to NORMAL, the switch connects the +5V voltage trace directly to the +5M voltage trace. This allows operation with no battery backup card in the system. The switch also grounds the MLOST- line on the backplane which signals the processor that memory is not retained during a loss of power.

With the slide switch set to BATTERY backup, the memory voltage +5M is separated from the main voltage +5V, and MLOST- is not grounded. In this configuration it is assumed that the battery backup card is installed in the backplane to provide the +5M voltage to the system backplane. During normal operation with the battery backup card in the backplane, the connection between the memory voltages is made on the battery backup card. Section V of this document contains more information about the battery backup card.

The following is a table of battery backup hold time vs. the XL memory configuration. All times are calculated for the the 12013A battery backup card under worst case conditions over temperature.

BACKUP TIME VERSUS CONFIGURATION

| CONFIGURATION | BACKUP TIME |
|------------------------------|-------------|
| 12002A 128K bytes | 1 hr 56 min |
| 12002A 256K bytes | 1 hr 23 min |
| 12003A (1) | |
| 12002A 384K bytes | 1 hr 4 min |
| 12002A (2) | |
| 12002A 512K bytes | 53 min |
| 12003A (3) | |
| 12002B 512K bytes | 1 hr 29 min |

8.2.6 PARITY

The XL memory contains the logic and memory to generate and store a parity check bit during each write cycle at all memory locations and to check for correct parity on each read from memory. The parity circuit, located on the XL controller, monitors the backplane data bus directly without any buffering to ensure correct backplane data parity.

On a write cycle the parity check bit is generated when the backplane data bus is driven by the card accessing memory. The parity bit is then latched and written into memory at the same time the data is written into memory. The controller card also passes the parity bit up the frontplane for an array card to store if the access is to memory on an array card. All memory locations contain a 17th RAM to store the parity bit.

The sense of the parity bit stored in the parity RAM is determined by the PS- line on the backplane. Normally the PS- line on the backplane is deasserted (high) indicating odd parity. When the PS- line is asserted (low) even parity will be stored in the parity RAM.

On a read cycle the parity RAM is accessed along with the row of data RAMs. The parity bit is checked against the parity of the valid backplane data. If the access is from an array card, the parity check bit is available on the frontplane for the controller to use in checking the backplane data parity.

If the parity is in error, the controller card will assert PE- on the backplane for one short half cycle of SCLK-. The memory card will complete the memory cycle and continue to perform memory accesses. It is the responsibility of the card performing the memory read to take appropriate action on a parity error.

Each memory card has a green parity LED. This LED is lit to indicate good parity. If a parity error is encountered, the parity LED on the card generating the bad parity will turn off and stay off until reset.

The parity LED on every XL memory card is reset (turned on) by performing a system power-on (when PON+ is low) or under program control by the execution of a CLC 0 instruction.

8.3 FUNCTIONAL THEORY OF OPERATION

A block diagram of the XL memory controller is shown in figure 8-2. The following section describes the operation of the XL memory system.

8.3.1 BACKPLANE INTERFACE

The XL memory interacts with all the other cards in the computer system through the backplane connectors. This backplane interface contains five groups of signals:

- clocks
- address and data buses
- handshake lines
- control lines
- status lines

CLOCKS (FCLK-, SCLK-, RCLK+)

The FCLK- and SCLK- clock lines are used to synchronize and sequence all memory operations. RCLK+ is used to drive the primary refresh counter which determines when a refresh cycle is required.

ADDRESS and DATA BUSES (A0-A14, SC0-SC4, D0-D)

The address bus, extended address bus, and data bus are latched off the backplane on every memory access. The data bus is driven by the selected memory card on a read cycle.

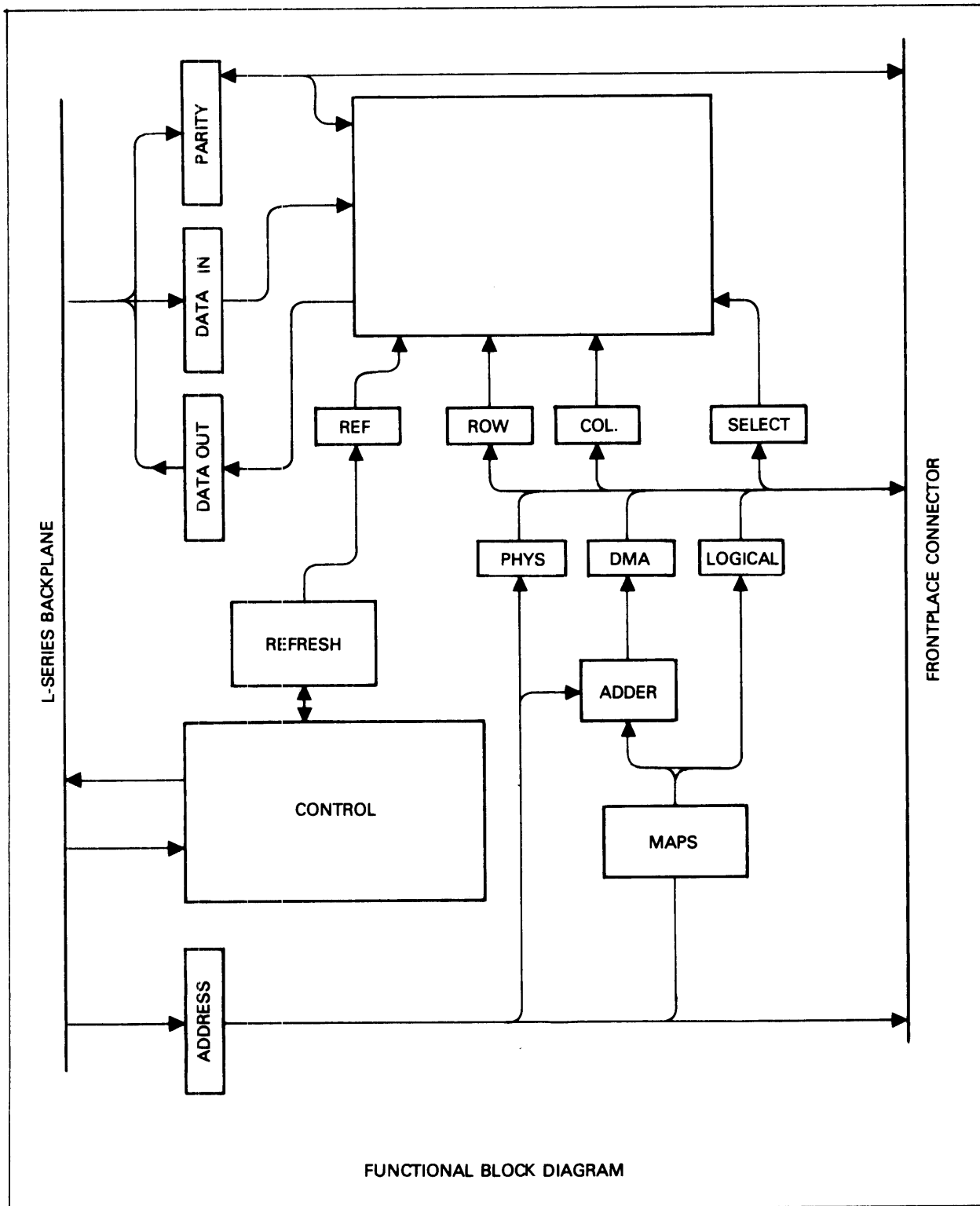


Figure 8-2. Block Diagram of the XL Memory Controller

HANDSHAKE LINES (MEMGO-, BUSY-, VALID-, MEMDIS

The main backplane memory handshake signals are MEMGO-, BUSY-, and VALID-. MEMGO- is asserted by the processor card or the I/O cards to request a memory access. The XL controller asserts BUSY- to acknowledge the receipt of MEMGO- and to prevent other devices from requesting memory accesses until the current memory access is complete. No card can assert MEMGO- while BUSY- is asserted. At the end of every memory access the controller will assert VALID- to indicate that the requested data is available on the backplane (for memory reads), or that the data has been written to memory (for memory writes). See figure 8-3 for timing details of these signals.

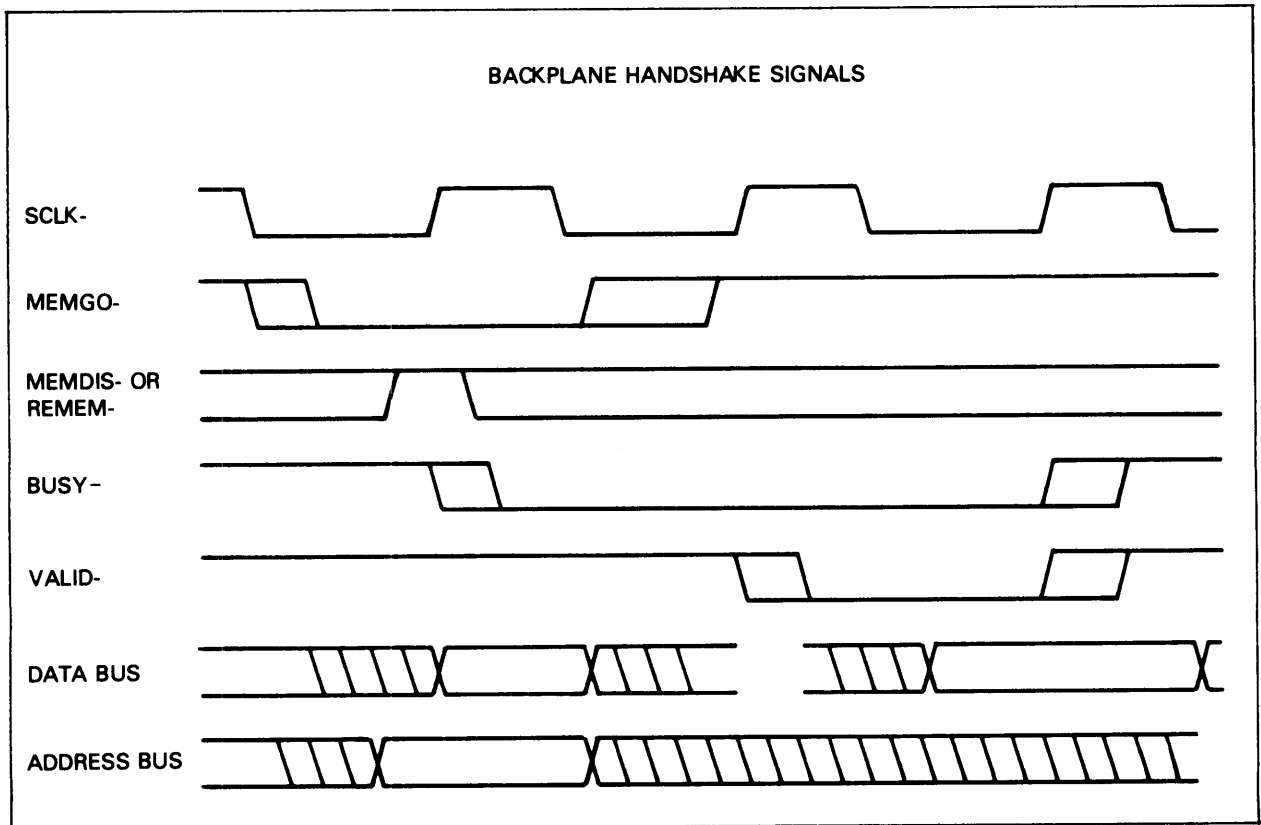


Figure 8-3. Timing of Handshake Signals

The main memory can be inhibited from responding to a memory request by the assertion of either MEMDIS- or REMEM- during the assertion of MEMGO-. MEMDIS- is used by the processor card when it is accessing virtual control panel code or self-test code directly from the ROM on the processor card. During these accesses, the processor card will assert the memory handshake lines BUSY- and VALID- because the controller card is not performing the memory access. REMEM- is asserted by I/O cards when accessing remote memory. Figure 8-3 shows the timing of the inhibit signals.

CONTROL LINES (MRQ-, RNI-, IAK-, COTRN-, CRS)

These five lines control operations on the XL controller card. MRQ- and COTRN- are used by the controller to distinguish between processor accesses and I/O accesses. MRQ- is asserted by all I/O cards when requesting memory access. When MRQ- is asserted with MEMGO-, the controller card will use the Relocation Register selected by the I/O card in performing the memory access. If MRQ- is not asserted with MEMGO-, the controller card will use the processor maps in performing the access. COTRN- can be used to invert the effect MRQ- has in determining the type of access to perform. When COTRN- is asserted with MRQ- the controller will perform the access as if it were a processor access. When COTRN- is asserted without MRQ- the controller will process the access as if it were an I/O access.

RNI- is asserted by the processor card to signify that the current memory access is the fetch of an instruction. This line is used on the controller to aid in recognizing the mapping control instructions used by the controller.

IAK- is asserted by the processor to acknowledge an interrupt. This signal has the effect of resetting the controller's mapping state machines to an unmapped, physical state. This allows the processor to execute the interrupt service routine program which resides in physical memory. CRS-, control reset, is driven by the processor to hard reset the I/O system. This line also has the effect of resetting the controller's mapping state machines to an unmapped, physical state.

STATUS LINES (PS-, MP+, PON+, PE-, MLOST-)

These five lines are backplane status lines. PS- indicates the current sense of the parity system. When PS- is deasserted (high), the controller will generate and store odd parity. When asserted (low), the controller will generate and store even parity.

MP+ is asserted by the processor to indicate that the memory protect fence within the processor card is enabled. This line, when enabled, is used by the controller to prevent a cross store instruction from writing data into main memory or into the controllers map RAMS. This prevents a user's mapped program from destroying system memory or the system maps.

PON+ is driven high by the power supply when the backplane voltages are within specification. This line is used as a clear line on the memory controller. When deasserted, this line causes a hard clear of all the non-refresh logic on the controller, and allows only refresh cycles to occur on the memory cards. No memory requests will be serviced while the PON+ line is low.

PE- is the parity error line on the backplane. The memory controller asserts this line if a parity error is detected during a read cycle. See section 8.2.6 for more details.

MLOST- is an open collector line driven low by the controller card, the processor card, or the battery backup card when the system is not configured to sustain battery backup voltages on a power outage. This line indicates to the processor on a power-up whether the memory voltages have been sustained, thereby preserving the contents of main memory. When the BATTERY backup/NORMAL switch on the controller card is set to NORMAL, the MLOST- line is asserted (grounded) to indicate that memory will be lost if power is interrupted. When the battery switch is set to BATTERY backup, the state of the MLOST- line is determined by the processor and battery backup cards.

8.3.2 MEMORY TIMING AND CONTROL LOGIC

The memory timing and control logic provides the interface between the backplane signals and the main memory dynamic RAM chips. This logic generates the signals required to 1) control the access and refresh of the dynamic RAMs, 2) supply the correct backplane handshake signals, and 3) provide the frontplane control signals.

In a typical memory access the first function of the controller after receiving MEMGO- is to assert BUSY- on the backplane to prevent other devices from requesting memory cycles. One FCLK period later, the control logic latches the backplane address bus, extended address bus, and the data bus into S/LS373 transparent latches. The parity generator circuitry, composed primarily of two S280s, uses the backplane data bus to generate a parity check bit. This check bit is also clocked into a flip-flop at the same time and then routed to the parity RAMs for storage.

The control circuitry presents the lower bits of the address to all the RAMs in the memory system. A small delay is then required for the mapping logic to generate the upper bits of the physical address. The control logic decodes the upper address bits to determine which one row of RAMs on which memory card will be accessed. This selected row then receives a row address strobe (RAS) signal and a column address strobe (CAS) signal. On a write cycle the latched data bus is presented to the RAMs and the RAM write line is asserted. The data is then written into the addressed memory location. On a read cycle the RAM write line is not asserted and the data stored in the addressed RAMs is read.

The control circuitry enables the backplane data bus drivers on memory read cycles, and the requested data is then driven on the system backplane. The parity circuitry checks the parity of the data against the stored parity bit. On a miscompare, the PE- line will be asserted signaling a parity error, and the parity LED circuit will set and turn off the LED.

VALID- is asserted on the backplane on all memory accesses to signal the end of the cycle. BUSY- and VALID- are then both deasserted enabling further memory accesses.

The control logic also manages the sequencing of refresh signals to the RAMs. When refresh cycles and memory cycles coincide, this logic arbitrates the

cycles allowing one to complete before starting the other. During a refresh cycle the correct row refresh address is presented to the RAMs and a "RAS only" cycle is initiated.

8.3.3 MEMORY REFRESH LOGIC

The main memory on the XL controller and XL array boards use dynamic Random Access Memory chips. These dynamic RAMs require periodic refreshing to ensure data retention. The XL controller arbitrates conflicts between refresh cycles and memory access cycles and initiates the refreshing of all memory in the system.

The controller card contains the primary refresh counter which is used to count RCLK cycles on the backplane. When 68 RCLK cycles have occurred, the counter indicates to the control logic that a refresh cycle is needed. This allows all memory to be refreshed within the required period.

During a refresh cycle, the control logic on each card presents a refresh address to the RAMs and a "RAS only" cycle occurs. This cycle refreshes one row of memory within the RAM chips. At the completion of the cycle, the refresh address counter is incremented by one to prepare for the next refresh cycle. All 128 rows (or 256 rows on the 12002B) of the RAM are guaranteed to be refreshed in a period of 2 milliseconds (or 4 milliseconds on the 12002B).

Memory accesses can occur asynchronously with respect to refresh cycles. An uninhibited refresh cycle requires 2 SCLK periods to complete. When a refresh cycle is required at the same time a memory access is requested, the refresh cycle occurs first immediately followed by the memory cycle. Logic on the controller card latches the necessary backplane information needed to do the memory access, and starts the backplane handshake signals. The actual access occurs after the refresh cycle completes. From the backplane this memory cycle appears to take 5 SCLK periods; two for the refresh and three for the memory access.

When a memory cycle is requested during the second half of a refresh cycle, the necessary backplane information is latched and the memory cycle is started when the refresh cycle completes. This memory cycle takes 4 SCLK cycles to complete.

When a refresh cycle is requested during a memory cycle, the refresh cycle is postponed until the third cycle of the memory access. The first cycle of the refresh is overlaid on the third cycle of the memory access to reduce the potential interference between memory cycles and refresh cycles. This allows an effective one-cycle refresh cycle during heavy memory accessing. A memory cycle is not lengthened when a refresh is requested during a memory cycle, and requires its normal 3 SCLK cycles to complete.

8.3.4 MEMORY MAPPING OPERATION

The mapping circuitry on the XL memory controller contains the logic necessary to extend the address range of the L-Series computer from 32K words (available on the 12004A) to 256K words. To achieve this addressing capability requires an address bus width of 18 bits. To generate an 18-bit address, the XL controller performs an address mapping. The 18-bit memory address is only available on the frontplane connector of the XL memory cards and not on the computer backplane.

The controller card logic contains the map RAMs used in extending the addressing range of the system. There are 32 map locations (processor maps) used when the processor is accessing memory, and 32 map locations (Relocation Registers) used when the I/O cards are accessing memory. These map RAMs are 'memory mapped' in the computers address space. Memory locations 100-137 address the 32 processor maps, and locations 140-177 address the 32 I/O Relocation Registers. The map RAMs contain a copy of the lower 8 bits of memory locations 100-177. When a write is performed to main memory at locations 100-177 a copy of the data is also stored into the map RAMs. This data is then used in generating the 18-bit address used in the XL memory.

The XL controller has four separate methods of generating an 18-bit address: two methods for processor memory accesses, and two methods for I/O accesses. The controller logic senses the state of MRQ- on the backplane to determine whether the access is initiated by the processor card or by an I/O card.

All processor accesses, although identical on the backplane, occur when the XL controller is operating in one of two modes: physical (unmapped) or logical (mapped). The mode used for processor accesses is controlled by logic on the controller card. This logic recognizes and executes backplane instructions which instruct the control logic when to operate in physical or logical mode. All processor memory accesses while the controller is in physical mode allow the processor to access the lowest 32K words of physical memory only. Processor memory accesses while the controller is in logical mode allow the processor to access 32K words of memory. The location of this logical memory in physical memory is determined by the contents of the map RAMs on the controller card.

When the controller is operating in physical mode the 18-bit address is obtained by appending three "0" bits to the front of the 15-bit backplane address. This allows access to the lowest 32K words in main memory.

When the controller is operating in the logical mode the controller's map RAMs help determine the 18-bit address. Main memory locations 100-137 are reserved for the processor maps. The map RAMs on the controller contain a copy of the lower 8 bits of these 32 locations. Each of the 32 map locations corresponds to a 1K word block in logical memory.

The map at location 100 corresponds to the first 1K of logical program memory. The map location at 137 corresponds to the last 1K of logical program memory. The physical memory which responds to a logical address is determined by the contents of the corresponding map location. The map at location 100 points to the 1K page of physical memory that will respond to logical addresses in the range 00000-01777, or the first 1K page of logical program memory. The map at location 101 points to the 1K page of physical memory that will respond to the logical address in the range 02000-03777, or the second page of logical program memory, etc.

The 18-bit address is generated by mapping the 5 most significant bits of the backplane address (A10-A14) into the controller's map RAMs. These address bits select one location of the map RAMs which produces an 8-bit output. These 8 bits determine which page in the entire memory will respond to that page of logical address. The 8 bits from the map RAMs are appended to the low 10 bits of the backplane address (A0-A9) to produce the required 18-bits. Figure 8-4 shows how this address is generated.

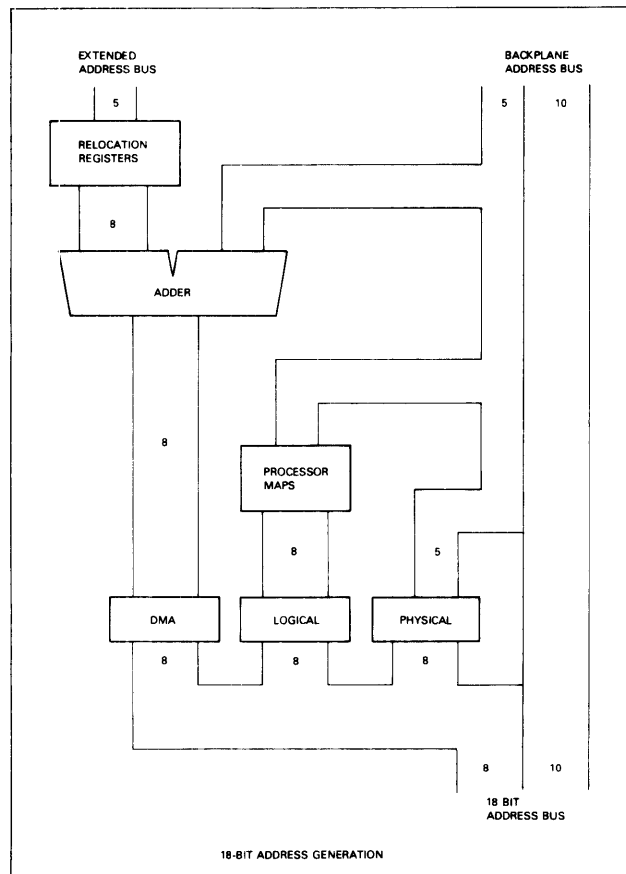


Figure 8-4. Methods Of Address Generation

The controller card contains three state machines which determine the mode of operation, and therefore, which method to use for generating an 18-bit address for processor accesses. Logic on the controller card recognizes instructions to control these state machines. There are six mapping control instructions that are recognized by the XL controller logic in order to determine the state of mapping for processor accesses. They are:

- 1- STC 11 enable logical mode after the completion of the next JMP instruction
- 2- CLC 11 enable physical mode after the completion of the next JMP instruction
- 3- CLC 13 immediately invoke an override of logical mode and force operation in physical mode
- 4- STC 13 immediately suspend the override of logical mode and resume operation in the mode defined by 1 and 2 above
- 5- XST temporarily toggle the state of mapping to perform a cross store instruction (XST 104413)
- 6- XLD temporarily toggle the state of mapping to perform a cross load instruction (XLD 104213)

In addition to the above mapping control instructions, the state of mapping is also affected by the backplane signals PON+, IAK-, and CRS-. When IAK- or CRS- are asserted or when PON+ is deasserted the state machines are immediately reset to an unmapped, physical state.

The cross load and cross store instructions are interpreted by the processor to be double load and double store instructions (DLD, DST). A memory controller state machine determines when to toggle the state of mapping to allow the load or store to occur in the alternate state. Only the A-register is cross loaded or cross stored before the state of mapping is returned to its original state. No indirect addresses are allowed in the DEF for these two instructions unless the indirect is through either the A or B register which then contains a direct address.

I/O accesses to memory occur through two mechanisms on the XL controller. The access is either to physical memory, which accesses the lowest 32K words of main memory only, or the access is to main memory relative to an offset or Relocation Register.

The L-Series I/O cards have the capability of driving the backplane extended address bus (SC0-SC4). This bus is actively driven by an I/O card during all I/O accesses to main memory.

I/O accesses to physical memory occur when either the Self Configure bit

(SC5-) is asserted or when an I/O card drives the extended address bus all low during an access. The exact location in physical memory is then determined directly by the backplane address bus. The 18-bit address is obtained by appending three '0' bits to the front of the backplane address as is done for processor accesses to physical memory. This allows access to the lowest 32K words of memory.

Accesses to memory relative to a Relocation Register occur when neither of the above two conditions are met. To generate an 18-bit address, the XL controller uses the extended address bus (SC0-SC4) to determine which Relocation Register to use for the I/O transfer. The 32 Relocation Registers are located in main memory locations 140-177. The Relocation Register at location 141 is selected when the extended address bus is 01. The Relocation Register at location 177 is selected when the extended address bus is 37. The Relocation Registers are 8 bits wide and point to a page boundary in main memory. The specific page is determined by the contents of the Relocation Register. If a Relocation Register contains 000 it will point to the lowest page in memory. If the Relocation Register contains 377 it will point to the highest page in memory.

The Relocation Register is used as a base pointer from which the I/O card has access to the next higher 32K words. The exact page in memory to be accessed is determined by adding the five most significant bits of the backplane address bus (A10-A14) to the 8-bit Relocation Register. The entire 18-bit address is then generated by appending these 8 bits to the 10 least significant bits of the backplane address bus. Figure 8-4 shows the generation of this address.

A method exists in the XL controller logic to allow I/O accesses which are accompanied by the assertion of SC5- to select a Relocation Register for use in the transfer and not to be forced to access only physical memory. This capability is provided as a diagnostic aid to assist in testing the operation of the memory controller. The execution of a STC 13,C will mask off the effect of the SC5 line and allow I/O operating under diagnose mode-three to test the Relocation Register circuitry. The execution of either a STC 13 or a CLC 13 will reset this mask. The mask is also reset by IAK-, PON+, or CRS-.

The processor maps and I/O Relocation Registers are locations 100-177 in main memory. The map RAMs actually contain a copy of the lower 8 bits of these memory locations. The map RAMs at these locations can be written by the processor only when the controller is in the physical mode. Processor writes to locations 100-177 while the controller is in the logical mode will write to main memory but will not write to the map RAMs. Memory reads from locations 100-177 will always produce the data stored in main memory and not the data in the map RAMs. The data stored in the map RAMs is only used by the controller logic when determining the extended address bits. The map RAMs can also be written by an I/O card using Relocation Register 140 and addressing memory locations 100-177.

8.3.5 MAPPING CONTROL LOGIC

The mapping control logic on the XL controller centers around three PAL (programmable array logic) devices. Internally these devices are an AND-OR array of gates which are programmed to the required combinational logic patterns.

The first device, PAL14H4 (instruction decoder), monitors the backplane data bus and is programmed to recognize the seven instructions which control the state of mapping on the controller. These seven instructions are encoded on three of the PALs output lines and feed directly to the second device, PAL16R8. A portion of PAL14H4 assists in preventing a cross store instruction from writing data into memory when MP+ is enabled.

The second device, PAL16R8 (state machine), contains all of the state machines used to determine the state of mapping. This PAL has eight internal flip/flops which are fed by its AND-OR array. The inputs to this PAL are the three encoded instruction lines from the first PAL, two backplane data bus lines, and three control lines. The two data bus lines assist the state machines in resolving indirect addresses and in distinguishing the STC 13 and STC 13,C instructions. The three control lines 1) distinguish instructions from data, 2) distinguish processor accesses from I/O accesses, and 3) reset all the state machines.

The third device, PAL12L6 (address path enable), contains the logic to control and enable the correct address paths in determining the 18-bit address for physical, logical, and I/O accesses to memory. This PAL also determines when the map RAMs are being written into and controls the flow of data into them.

8.3.6 FRONTPLANE SIGNALS

A frontplane connector is used to connect the 12003A array cards to the 12002A controller. This connector carries the control signals and the 18-bit frontplane address required for expanded memory operation. A list of the signals on the frontplane connector is shown in Figure 8-5.

| PIN | SIGNAL | SIGNAL | PIN |
|-----|---------|---------|-----|
| 1 | GND | GND | 2 |
| 3 | A10- | A11- | 4 |
| 5 | A12- | A13- | 6 |
| 7 | A14- | A15- | 8 |
| 9 | A16- | A17- | 10 |
| 11 | A18- | A19- | 12 |
| 13 | MIO | MO0 | 14 |
| 15 | MI1 | MO1 | 16 |
| 17 | A0+ | A1+ | 18 |
| 19 | A2+ | A3+ | 20 |
| 21 | A4+ | A5+ | 22 |
| 23 | A6+ | A7+ | 24 |
| 25 | GND | GND | 26 |
| 27 | A8+ | A9+ | 28 |
| 29 | SPARE 1 | SPARE 2 | 30 |
| 31 | PAR- | RAS- | 32 |
| 33 | WRITE+ | DRIVE- | 34 |
| 35 | MI2 | MO2 | 36 |
| 37 | MI3 | MO3 | 38 |
| 39 | LATCH+ | CASEN- | 40 |
| 41 | PDSBL- | PCK- | 42 |
| 43 | COUNT+ | XTND- | 44 |
| 45 | REF+ | ACK- | 46 |
| 47 | +5V | +5V | 48 |
| 49 | GND | GND | 50 |

Figure 8-5. Expanded Memory Frontplane Signals

These signals can be grouped into four types:

- address lines
- memory board configure lines
- control lines
- array board response lines

ADDRESS LINES (A0-A19)

The frontplane contains 20 dedicated address lines, the lower 18 of which are used by the XL controller. These lines determine which word of the 256K words in main memory is being accessed.

MEMORY BOARD CONFIGURE LINES (MIO-MI3,MOO-M

These four chained lines are used by each array card to determine which position within the memory array the card occupies. This tells the array card to which 64K word block of address space it will respond. The 12002A controller card always responds to addresses representing the lowest 64K word block in memory. The MOO-MO3 lines driven by the controller tell the array card directly above the controller to respond to the second 64K word block. This array card adds to the MOO-MO3 count and passes it up to the next array card. Each array card uses the MIO-MI3 lines to determine its location in memory space, and uses the MOO-MO3 lines to tell the next higher card its position in memory space.

CONTROL LINES (PAR-,RAS-,WRITE+,DRIVE-,LATCH+,C

The eight control lines passed up the frontplane are generated on the XL controller card and used on both the controller card and all the array cards to control memory accessing and refreshing on each card. These lines are as follows:

1. LATCH- is the control signal used on all memory cards to latch the backplane address bus and data bus.
2. WRITE+ is asserted when the current memory access is a write cycle.
3. PAR- is the parity bit generated for the backplane data on a write cycle. This bit is stored into memory along with the data.
4. RAS- is a control line used to start the access of the memory RAMs on read, write and refresh cycles.
5. CASEN- is used to allow the memory to perform a complete memory access on memory reads and writes. This line is not enabled for refresh cycles.
6. DRIVE- controls the output data bus drive buffers. When asserted, the memory card containing the memory location being read will allow the data bus drivers on its card to drive the backplane.
7. REF+ is asserted during a memory refresh cycle.
8. COUNT+ signals the refresh row address counter to count to the next address.

RESPONSE LINES (PDSBL-,PCK-,XTND-,ACK-)

These four open collector lines are driven by the array card responding to the memory access. They are the following:

1. PCK- is the parity check bit of the addressed memory location. It is used by the controller to determine whether a parity error has occurred.
2. ACK- is driven by an array card to signal the controller that a memory card is responding to the address. If no ACK- is received, the controller will drive the backplane data bus.
3. XTND- and PDSBL- are for use by a ROM array card to extend the memory cycle (allowing for the use of slower access PROMs) and to disable the generation of a parity error by the controller card if no parity check bit is available.

8.3.7 ARRAY BOARD CONTROL AND TIMING LOGIC

The 12003A array board contains the logic to access and refresh the RAM array on the card. This logic uses the frontplane signals to direct the timing of the signals on the card.

Each array card latches the data from the backplane and drives the backplane data bus directly. The memory address is obtained from the frontplane connector. The address decoding circuitry determines whether the card is being accessed and which row of RAMS on the card corresponds to the address. If the card is to be accessed, the control logic will assert ACK- on the frontplane to tell the controller that an array card is responding to the memory location. The control logic then uses the frontplane signals to sequence the assertion of the row address strobe (RAS) and column address strobe (CAS) lines.

On write cycles the parity check bit is obtained over the frontplane connector and presented to the parity RAM. The backplane data bus is latched on the array card and presented to the data RAMs. On a read cycle the array card drives the backplane data bus directly. The parity check bit is read from the parity RAM and returned to the controller card for checking against backplane parity. If a parity error is detected, the array card will see PE- asserted on the backplane and will know that the access was from its array and will extinguish its parity LED.

8.4 DETAILED THEORY OF OPERATION

The following paragraphs contain the detailed theory of operation for the XL memory controller. Refer to the schematic diagrams (drawing numbers D-12002-90003-51, D-12002-90003-52, and D-12003-60001-51) located at the rear of this section as necessary. Figures 8-6A, 8-6B, and 8-6C are detailed timing diagrams including many of the signals discussed in this section.

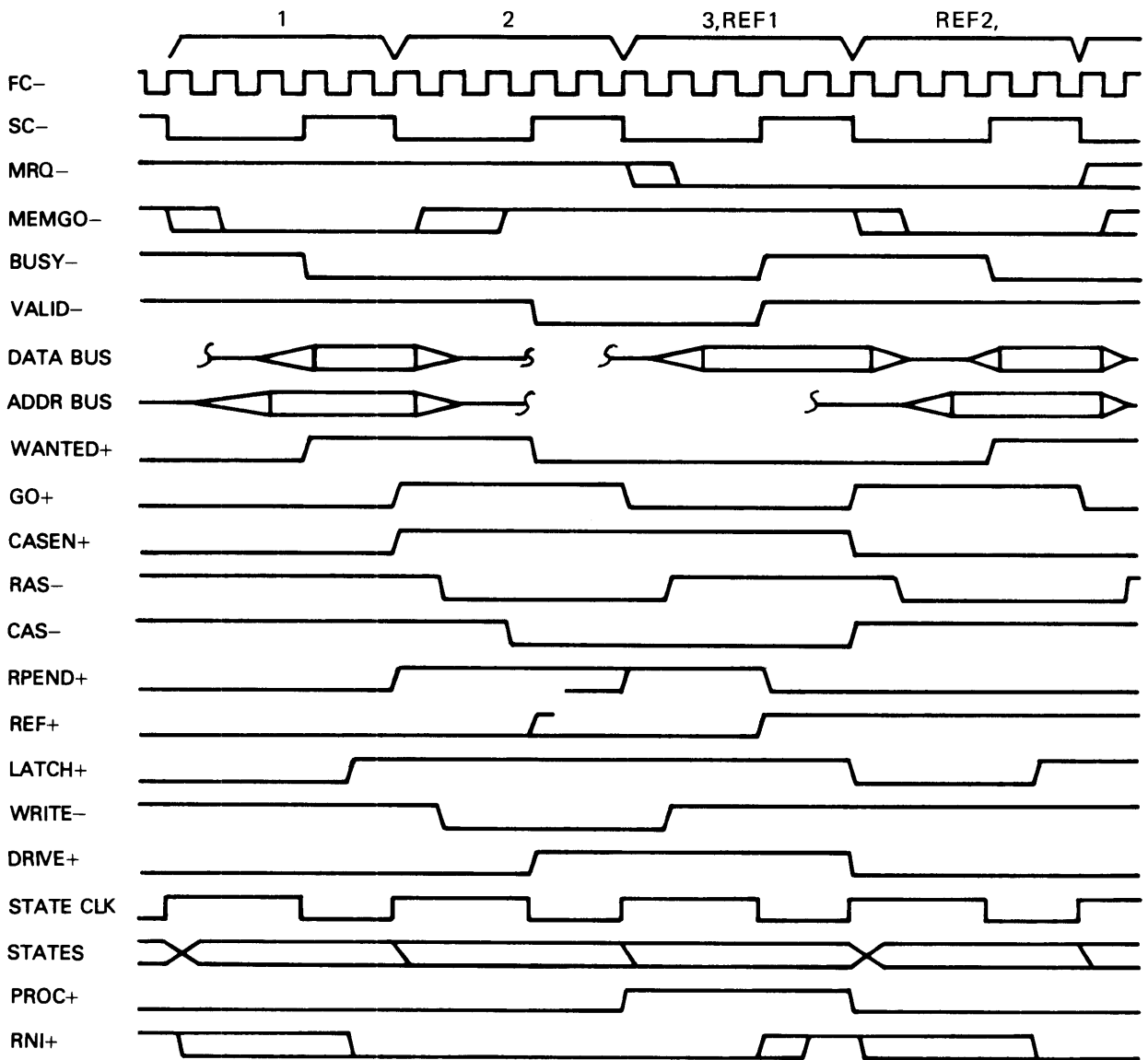


Figure 8-6A. Timing Diagram For 3-Cycle Access

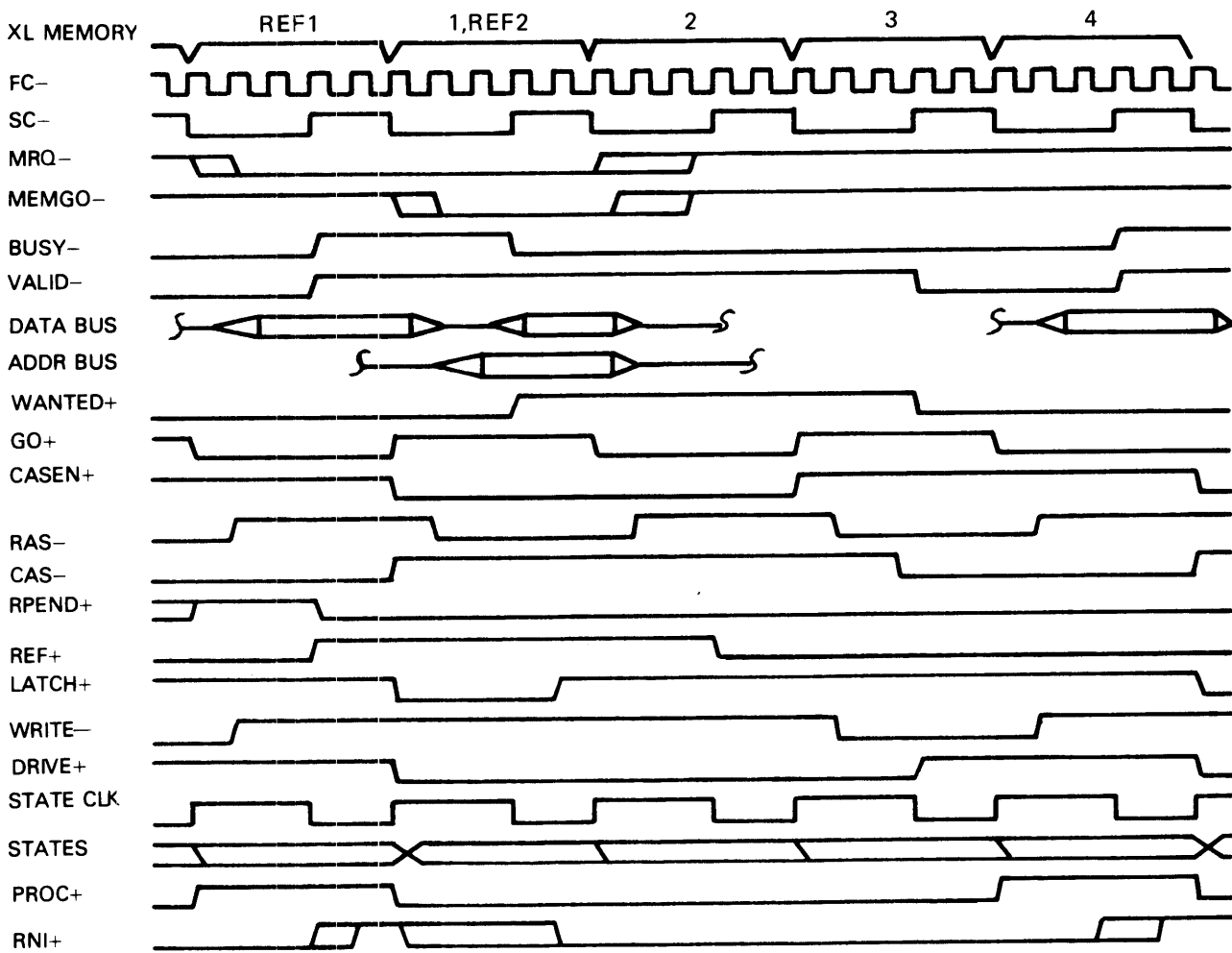


Figure 8-6B. Timing Diagram For 4-Cycle Access

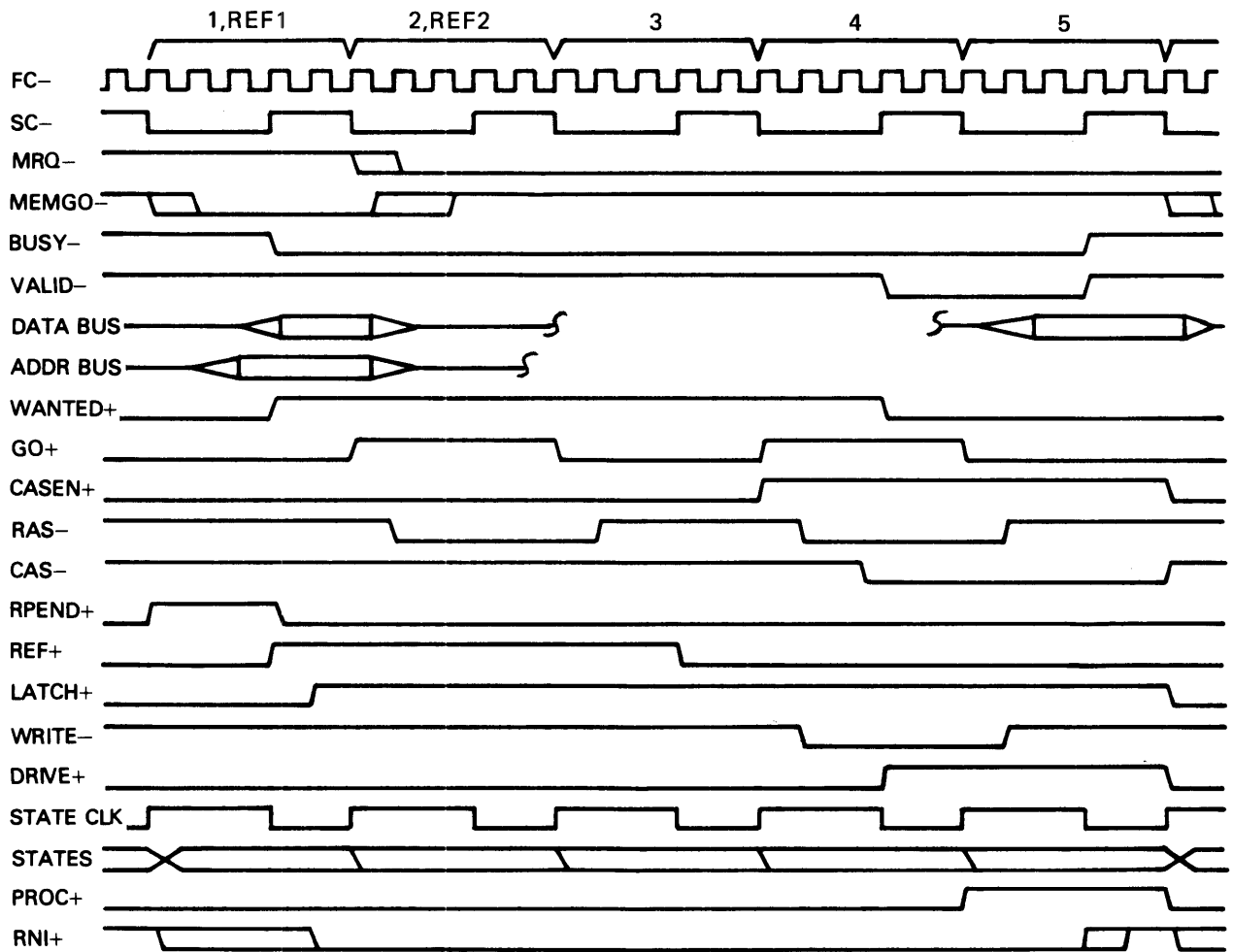


Figure 8-6C. Timing Diagram For 5-Cycle Access

8.4.1 MEMORY CONTROL LOGIC

To perform a memory access, the requesting device asserts MEMGO- on the backplane. On the XL controller card this signal is received at U719-12 where it is qualified with both MEMDIS- and REMEM- to ensure that main memory access is requested.

If the conditions are met at the falling edge of SCLK+ the memory card will start a memory cycle. The WANTED flip-flop (U1119-9) becomes set to start the sequence of timing signals required for accessing the RAMs. At the same edge of SCLK+ the BUSY flip-flop (U718-9) also gets set and starts the backplane handshake sequence. The BUSY+ signal at U718-9 enables the S240 (U1019-1) to drive the backplane BUSY- line.

The WANTED+ signal performs four functions: 1) it inhibits a refresh cycle from occurring during the memory access by disabling gate U1118-10; 2) it enables the GO flip-flop (U818-9) to become set which will then allow the RAS control signal to reach the selected row of RAMs; 3) it enables the CASEN flip-flop (U618-5) to become set which will then allow the CAS control signal to reach the RAMs; 4) it qualifies the enabling of the backplane data bus drivers (U317-12).

When the BUSY flip-flop becomes set, it enables the LATCH flip-flop (U618-9) to set at the next falling edge of FCLK+. The LATCH signal is used by the controller and the array cards to latch the address bus, extended address bus, the WE- bit, and the data bus off the backplane. This signal is routed to the LS/S373 transparent latch gates which control the flow of the backplane buses. When LATCH+ is asserted the backplane information is frozen at the outputs of the latches. This signal also clocks the READ flip-flop (U117-9) which saves the read/write backplane signal WE-.

The GO+ signal is asserted for one SCLK period when either a memory access is requested or when a refresh cycle is required. The GO+ signal allows the RAS+ flip-flop (U818-5) to set. The RAS+ (Row Address Strobe) signal is also one SCLK period long and is interpreted by the RAMs to mean the row address bits at the RAMs address pins are now valid. The delay from the setting of the WANTED flip-flop to the setting of the RAS flip-flop is required to allow 1) the row address to become valid at the RAM address pins, and 2) to allow the decode logic to determine which one row of RAMs in the XL memory will receive a RAS pulse.

The 18-bit address generated by the mapping logic is presented to four gates on the controller: U21, U31, U7, and U310-6. Gate U310-6 receives the two most significant bits of the 18-bit address. These two bits are used to determine whether memory on the XL controller card or memory on one of the array cards is to be accessed. U310-6 will go low when both A16+ and A17+ are low. This enables the 12002A to respond to the lower 128 Kbytes in memory address space. When U310-6 is asserted the outputs of U7 will become active. Gate U7 is a 2-to-4 bit decoder. The two inputs (A14 and A15 on the 12002A)

determine which one row of RAMs on the card is to be accessed. The outputs of U7 are fed thru U9 and are presented to the RAS drivers, U10. During a memory access, only one of the drivers will be enabled to pass the RAS signal from the RAS flip-flop. When a refresh cycle occurs, the REF- line will enable all outputs of U9 and all the RAS drivers will be enabled allowing all RAMs to be refreshed.

On the 12002B the four jumpers, W1-W4, are loaded in their alternate positions marked as 64K. These jumpers direct the flow of the four most significant address bits A14-A17. Jumper W4 permanently enables the controller card to respond to all address locations by enabling U7. All main memory is contained on the 12002B controller card.

The CASEN flip-flop (U618-5) is allowed to set during all memory accesses, but is not allowed to set during a refresh cycle. The CASEN signal enables the CAS- (Column Address Strobe) signal to reach all the RAMs. This signal is interpreted by the RAMs to mean the column address bits at the RAMs address pins are now valid.

The CASEN- signal becomes inverted at U417-12 and then allows the CAS flip-flop (U218-9) to clock at the correct time as determined by the outputs of the delay line (U118). The delay line works with U819-8, U819-6, and the CAS flip-flop to allow the following sequence of events:

- 1) present the row address to the RAMs by enabling U21 (S240)
- 2) provide a RAS- pulse to the selected row of RAMs through U10 (S37)
- 3) present the column address to the RAMs by enabling U31 (S240)
- 4) provide a CAS- pulse to the RAMs through U6 (S37)

The CASEN flip-flop provides the signal to reset the WANTED flip-flop (through U918-11), and to set the VALID flip-flop. The VALID- signal is asserted on the backplane through U1019 (S240) for one SCLK period. The rising edge of VALID- signals the other cards in the backplane that the data bus is valid. The VALID and BUSY flip-flops both reset at the same time completing the memory handshake.

The backplane signal PON+ is used on the controller card to hold many of the flip-flops in a known state. When the backplane voltages are out of regulation, the power supply will drive PON+ low. This signal is inverted twice on the controller card (U1118-4 and U1019-9) and is used to reset flip-flops on the card. This puts the controller into a known state when power is first applied to the system backplane.

When the battery backup card is installed in the backplane, the +5M memory voltage will be powered by the battery card to sustain main memory. The switch, SW1, on the controller card should be positioned to the BATTERY

position to allow the battery backup card to drive the +5V and +5M voltage lines separately.

When PON+ is deasserted under these conditions, the BPON+ signal on the controller will only allow refresh cycles to occur and will prevent any external cards from accessing memory by resetting the WANTED flip-flop (U1119-9). This retains memory for use when power is reapplied to the backplane.

8.4.2 MEMORY REFRESH LOGIC

To guarantee that memory is retained within the RAM chips a refresh cycle is required every 68 RCLK cycles. The primary refresh counter, LS390 (U1218), determines when a refresh cycle is required by counting RCLK edges received through U1118-13. When 68 cycles have occurred the output of U1219-8 goes high which clears the counter.

During each count cycle, the RPEND (refresh pending) flip-flop gets one clock pulse. The REF flip-flop (U1119-5) and the COUNT flip-flop (U919-5) then set at the first opportunity when there is not a memory access occurring. The REF and COUNT signals do the following: 1) allow U41 (LS240) to present the next refresh address to the RAMs; 2) allow U9 (S00) to enable RAS to occur to all RAMs; 3) allow the GO flip-flop (U818-9) to set thus allowing the RAS flip-flop (U818-5) to set generating a RAS- pulse to the RAMs; 4) prevent the CASEN flip-flop (U618-5) from setting; and 5) clock the refresh address counter U8 (LS373).

The refresh address counter (U8) determines which row of cells within the RAM chips is to be refreshed. This counter counts through all rows within the required 2 milliseconds.

Under normal operation a memory cycle takes three SCLK periods and a refresh cycle takes two periods. When both a refresh cycle and a memory access are requested during the same time, gates U1118-10 and U1118-1 determine the correct sequencing of the two operations.

Memory refresh cycles can coincide with memory access cycles in three situations. When refresh is required at the same edge of SCLK that a memory access is requested (REF+ flip-flop gets set at the same time as the WANTED flip-flop) the refresh cycle will occur first followed by the memory access. The refresh cycle will take two SCLK periods and the memory access will take three SCLK periods to give a total access time of five SCLK periods under this condition. The backplane handshake signal BUSY- will be asserted when the memory access is requested and will stay asserted through both the refresh cycle and the memory access. BUSY- is then asserted for two SCLK periods longer than a normal memory cycle (see Figure 8-6C).

When a refresh cycle is required one SCLK before a memory access, the memory access will start at the completion of the refresh cycle. A memory access under these conditions will take four SCLK periods to complete and BUSY- will

be asserted for one SCLK period longer than a normal memory cycle (see Figure 8-6B).

When a refresh cycle is required during a memory cycle, the memory cycle will complete as usual. The refresh cycle will start during the last SCLK period of the memory access and take two SCLK periods. The length of assertion of the BUSY- signal will not be affected in this case (see Figure 8-6A).

8.4.3 MAPPING CONTROL LOGIC

The mapping control logic includes the logic to recognize the specific mapping control instructions, determine the state of operation of the XL controller, and enable the correct address path for the specific memory access.

8.4.3.1 INSTRUCTION RECOGNITION LOGIC

To implement mapping, the XL controller recognizes instructions which determine the specific mode of operation. On the controller U317-8, U312-6, U318-13, and most of U315 (PAL14H4) monitor the backplane data bus for the specific mapping instructions. Three outputs of PAL14H4 contain an encoded version of the mapping instructions. Below is a table defining the output combinations for each instruction and a description of the function of each instruction.

| <u>PAL14H4</u> <u>OUTPUTS</u> | | | <u>INSTRUCTION</u> | |
|----------------------------------|----|----|--------------------|---|
| E2 | E1 | E0 | | |
| 0 | 0 | 0 | | Any instruction other than those listed below |
| 0 | 0 | 1 | JMP | |
| 0 | 1 | 0 | XLD | Used to cross load data from the alternate state |
| 0 | 1 | 1 | XST | Used to cross store data from the alternate state |
| 1 | 0 | 0 | STC 11 | Used to enable operation in logical mode |
| 1 | 0 | 1 | CLC 11 | Used to enable operation in physical mode |
| 1 | 1 | 0 | STC 13 | Used to suspend the override of logical mode |
| 1 | 1 | 1 | CLC 13 | Used to invoke an override of logical mode |

Note that the distinction between STC 13 and STC 13,C is made in U215 (PAL16R8).

The three encoded outputs from PAL14H4 are fed directly to PAL16R8 (U215) and

are used to determine the next state of the state machines within PAL16R8.

8.4.3.2 MAPPING CONTROL STATE MACHINES

To implement the mapping functions, the XL controller contains four state machines to determine the mode of operation. The state machines reside within U215 (PAL16R8). This PAL contains an internal AND-OR gate array and eight internal flip-flops with a common clock (U215-1).

PAL16R8 has eight signal inputs:

PCYCLE+ (U215-3) is a line used to differentiate I/O memory accesses from processor memory accesses. This line is generated at U117-6 and is asserted for one SCLK period at the completion of a processor-initiated memory access.

RST- (U215-4) is a reset line to the state machines within the PAL. This line is asserted when either IAK- or CRS- are asserted or when PON+ is deasserted on the backplane. This line has the effect of immediately resetting all state machines within the PAL to an unmapped, physical state.

DB9+ (U215-9) is the backplane data bus line used to distinguish between the STC 13 and STC 13,C instructions.

RNIL+ (U215-8) is a latched version of the backplane RNI- (Read Next Instruction) signal which signifies that the current memory access is an instruction fetch.

E2, E1, E0 (U215-5,-6,-7) are the encoded version of the mapping instructions recognized by the controller.

DB15+ (U215-2) is a backplane data bus line used by the state machines to determine direct/indirect memory fetches and allows for the resolution of indirect addresses.

The first state machine within PAL16R8 uses outputs Y1-, Y2-, and Y3- (U215-15,-17,-18). This state machine determines the basic physical/logical operating mode of the controller from the STC 11 and CLC 11 instructions. Below is a table of the six states of this state machine.

| PAL16R8 | | | STATE | STATE DESCRIPTION |
|---------|-----|-----|-------|---|
| OUTPUTS | | | | |
| Y1- | Y2- | Y3- | | |
| 1 | 1 | 1 | A | Physical mode, reset state |
| 1 | 1 | 0 | B | Received STC 11 (enable mapping) instruction, prepare to change to logical mode on next JMP |
| 1 | 0 | 1 | C | Received an indirect JMP instruction, stay in this state until the indirect is resolved |
| 0 | 1 | 0 | D | Logical mode, operating under mapped condition |
| 0 | 1 | 1 | E | Received CLC 11 (disable mapping) instruction, prepare to change to physical mode on next JMP |
| 0 | 0 | 1 | F | Received an indirect JMP instruction, stay in this state until the indirect is resolved |

Note that output Y1- determines the actual mode of operation: Y1- is high for physical operation, Y1- is low for logical operation.

The second state machine within PAL16R8 uses outputs Y4-, Y5-, Y6- (U215-19,-14,-13). This state machine determines when to toggle the state of mapping for the cross store (XST) and cross load (XLD) instructions. The XST and XLD instructions are recognized by the processor to be double store (DST) and double load (DLD) instructions. The processor will load or store the A and B registers during these instructions. The controller card will only toggle the state of mapping for the first of the loads or stores (the A register). Thus, the XLD and XST instructions are a single single cross load or cross store.

Below is a table of the six states of this state machine and a description of each state.

| PAL16R8 | | | STATE | STATE DESCRIPTION |
|---------|-----|-----|-------|---|
| OUTPUTS | | | | |
| Y4- | Y5- | Y6- | | |
| 1 | 1 | 1 | A | Idle mode, waiting for instruction. |
| 1 | 1 | 0 | B | Received XLD instruction. |
| 0 | 1 | 1 | C | Have received one more processor memory access to get the DEF for the XLD instruction, can now toggle state of mapping. |
| 1 | 0 | 1 | D | Have cross loaded or cross stored the data from the A register into memory, can now return the state of mapping to previous state |
| 1 | 0 | 0 | E | Received XST instruction |
| 0 | 0 | 0 | F | Have received one more processor memory access to get the DEF for the XST instruction, can now toggle state of mapping. |

Note that output Y4- determines when to toggle the state of mapping.

To prevent the store of the B register into memory during a XST instruction (the second store of the double store instruction) a portion of PAL14H4 (U315) is used to prevent the memory from being written to. During state D, when the A register has been cross stored, WDSBL+ (U315-17) will be asserted to prevent the processor from writing into memory. Additionally, PAL14H4 will also prevent the XST instruction from writing the A register to memory if Memory Protect (MP+) on the backplane is asserted. This prevents a users program from cross storing data into restricted areas of memory. During states E and F PAL14H4 will assert the WDSBL+ line to prevent all cross stores when MP+ is asserted.

The third state machine within PAL16R8 uses output Y7- (U215-16). This state machine determines when to force operation in physical mode, overriding the mode determined by the first state machine. This state machine recognizes the STC 13 and CLC 13 instructions, and will assert the OVRD+ line as shown below.

| PAL16R8 | | STATE | STATE DESCRIPTION |
|---------|---|---|-------------------|
| OUTPUTS | | | |
| Y7- | | | |
| 0 | A | Received STC 13 instruction or the RST signal, normal operating mode, no override in effect | |
| 1 | B | Received CLC 13 instruction, override in effect, operation forced to be in physical mode | |

The fourth state machine within PAL16R8 uses output MASK+ (U215-12), and determines when to mask the effect of the Self-Configure bit (SC5-). The Self-Configure line will normally force I/O accesses to occur to physical memory and not to use a Relocation Register. If a STC 13,C is executed, the MASK+ line is asserted which will allow the I/O card to select a Relocation Register to use in the transfer and not be limited to physical memory only. This mode is reset by executing either a STC 13 or a CLC 13 instruction or by the RST line. This feature is included as a diagnostic aid to be used when operating under diagnose mode three.

| PAL16R8 | | |
|----------------|--------------|--|
| <u>OUTPUTS</u> | <u>STATE</u> | <u>STATE DESCRIPTION</u> |
| MASK+ | | |
| 0 | A | Received STC 13, CLC 13 or RST signal, normal operating mode, no masking |
| 1 | B | Received STC 13,C instruction, mask of Self Configure bit in effect |

8.4.3.3 ADDRESS PATH ENABLE LOGIC

The XL controller has three separate methods of generating the required 18-bit address; one method for physical addresses, one method for logical addresses, and another method for DMA accesses. In all cases the lower 10 bits of the backplane address bus are left unmodified.

During accesses to physical memory, the upper eight bits of the 18-bit address bus are generated by appending three "0" bits to the front of the five upper backplane address bits (A10-A14). This is accomplished by U44 (S240).

During processor accesses to logical memory, the upper eight bits are determined by the contents of the two map RAMs (U18 and U28) which are addressed by the upper five bits of the backplane address bus through U110. These map RAMs contain an 8-bit wide word which is appended to the lower 10 bits of the backplane address by U34 (S240) to generate the 18-bit address.

During I/O accesses to memory using a Relocation Register, the upper eight bits of the 18-bit address are generated by adding the 8-bit Relocation Register, stored in the map RAMs and selected by the extended address bus (U112), to the upper five bits of the backplane address bus (A10-A14). Adder chips U14 and U24 perform this addition and U11 (S240) enables the 8-bit result.

PAL12L6 (U115) is used to control the flow of the address paths on the controller card. The inputs to PAL12L6 are listed below:

1. DMACC+ (U115-12) is the line which indicates whether the access is from the processor card or from an I/O card.
2. WDSBL+ (U115-5) is asserted to disable a write to memory from occurring during a cross store instruction. The second store of the XST instruction is always disabled. The first write is disabled if MP+ is asserted on the backplane.
3. READL+ (U115-1) is a latched version of the backplane write enable (WE-) signal.
4. SELFC+ (U115-11) is the line indicating that the I/O access is a self-configure access and therefore accesses physical memory only.
5. RR140+ (U115-8) is a line indicating that an I/O card has selected Relocation Register 140 to use in the memory transfer. All transfers using this Relocation Register will be forced to access physical memory. This is to ensure that all code written for the L-Series computer using the 12004A memory card will be compatible with expanded memory.
6. LBSY+ (U115-19) and RAS- (U115-6) are timing control signals which define the assertion window for some of the PAL outputs.
7. PHYS+ (U115-9) is the line which indicates whether the processor is operating in physical or logical mode.
8. U115-2, U115-7, U115-3, U115-4 are address lines which are used in deciding when a write to memory should also write to the controllers map RAMs (which are memory mapped at locations 100 - 177 in main memory).

The six outputs of PAL12L6 are described below:

1. LOGICAL- is a signal which enables the address paths required for an access to occur to logical mode. Asserted during a processor access in logical memory.
2. DMARR- is a signal which enables the address paths required for an access to occur to memory via a Relocation Register. Asserted during an I/O access when SELFC+ and RR140 are not asserted.
3. PHYSICAL- is a signal which enables the address paths required for an access to occur to physical memory. Asserted during a processor access in physical mode, or an I/O access when either SELFC+ or RR140+ is asserted.
4. MAPW- is a line which controls the writing of data into the map RAMs. It is asserted for a processor access in physical mode to locations 100-177 or an I/O access to physical memory 100-177.
5. MAPEN- is a line which enables U38 (LS244) to present the lower eight bits of the data bus to the map RAMs.

6. WRITE- is a line which is asserted during all I/O writes to memory and during all processor writes to memory that are not disabled by WDSBL+.

8.4.4 ARRAY CARD CONTROL LOGIC

The array card, 12003A, contains a subsection of the control logic on the controller card. The array card uses the frontplane signals generated on the controller card to direct operation of the array (see Figure 8-5).

The array card latches the backplane data bus directly off the backplane. The LATCH+ signal is directed to the LS373 transparent latches (U114, and U117). These latches drive the RAMs on the array card with the backplane data. The 18-bit address is available to the array card over the frontplane connector. The controller drives the address throughout the entire memory access so no latching is required on the array card. Buffers U107, U109, and U203 receive the address.

Each array card uses the upper two bits of the 18-bit address to determine whether it is being selected. The card compares these two bits against the M10-M13 address chained lines. The M10-M13 lines are driven by the memory card immediately below, and determine the address range the array card will respond to. Each array card uses an adder (U105) to alter the M10-M13 lines and sends out M00-M03 lines to the next higher array card. When a positive compare is made by gates U104 and U106, the BOARD+ line on the selected array card will be asserted and will enable the control signals to pass to the RAMs.

The RAS- line is received into U503 and is used to start the sequence of timing signals required to access the RAMs. The delay line (U502) and the flip-flop (U402-5) are used to generate the timing for the RAS and CAS signals to the RAMs.

A two-to-four decoder (U202) uses address lines A14 and A15 to determine which one row of RAMs on the card is to be accessed. The outputs of this gate are fed through U302 and enable one of the RAS drivers in U303.

If the access to the array card is a read, the frontplane DRIVE- signal will combine with the BOARD+ signal to enable the data bus drivers on the card (U113 and U116) to drive the backplane data bus with the requested data. The parity check bit stored with the data is returned over the frontplane through the open collector gate (U301-3) to the controller for checking against the parity of the backplane data bus parity.

REF+ and COUNT+ are used on the array card to enable the refreshing of the RAMs. Each array card contains a refresh counter which keeps track of the rows needing to be refreshed on each card. When a refresh is required the refresh address is presented to the RAMs through U110. The refresh counter is then updated for the next refresh cycle.

8.4.5 PARITY CIRCUITRY

Two S280 parity generator chips (U418 and U419) on the controller card are used to generate a parity bit on all write cycles and to check parity on all read cycles.

During write cycles, the S280s determine the backplane parity bit while the backplane data bus is still actively driven by the device performing the memory write. The parity bit, determined by EX-ORing the even sum outputs (U418-5 and U419-5) from the S280s, is clocked into the PARITY flip-flop (U218-5) with the LATCH+ signal. The parity bit is then presented to the parity RAMs for storage along with the data bits.

On a read cycle the S280s monitor the backplane data bus, which is driven by the XL memory. The parity of the backplane data bus is compared against the parity check bit available on U318-3. The parity of the backplane data should always be the same as the sense of the parity check bit. This is checked at the output of U519-3 (ERROR), which should always be low if no error has occurred. If an error occurs, the ERROR signal is gated on the backplane as PE- by U217-6, an open collector gate. This PE- signal will also turn off the parity LED on the controller card (through U1018-8, U310-8, and U310-11) if memory on the controller card was selected.

8.5 PARTS LOCATIONS

Parts locations for the extended memory cards are shown in figure 8-7 and in figure 8-8, where figure 8-7 is for the 12002A and 12002B cards and figure 8-8 is for the 12003A card.

8.6 PARTS LISTS

The parts lists for the cards are provided in tables 8-1 and 8-2, where table 8-1 is for the 12002A and 12002B and table 8-2 is for the 12003A. The 12002A and 12002B cards are identical except for the type of RAM; therefore, the same parts list is given for both with the RAM part number differences indicated.

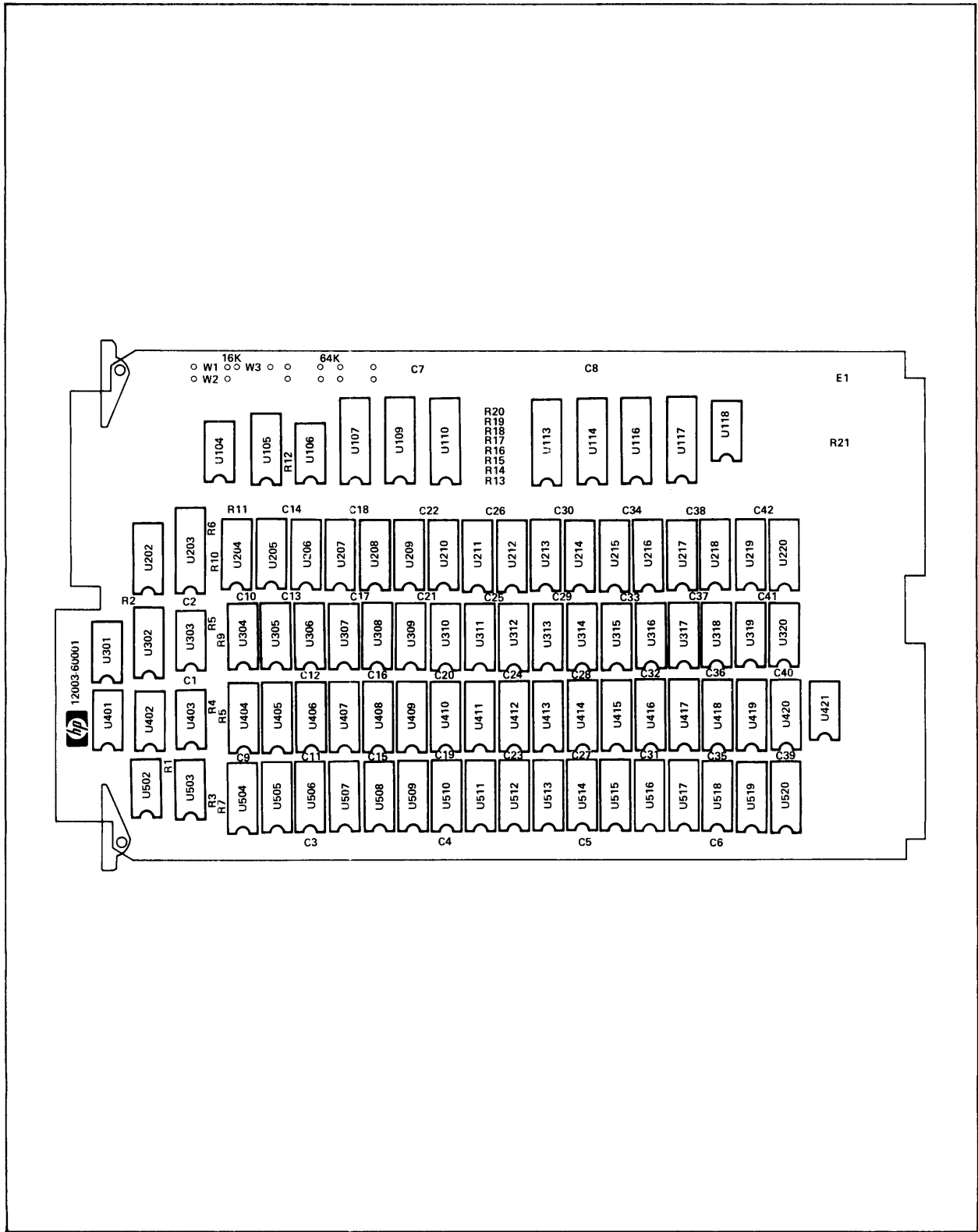


Figure 8-7. 12002A and 12002B Parts Locations

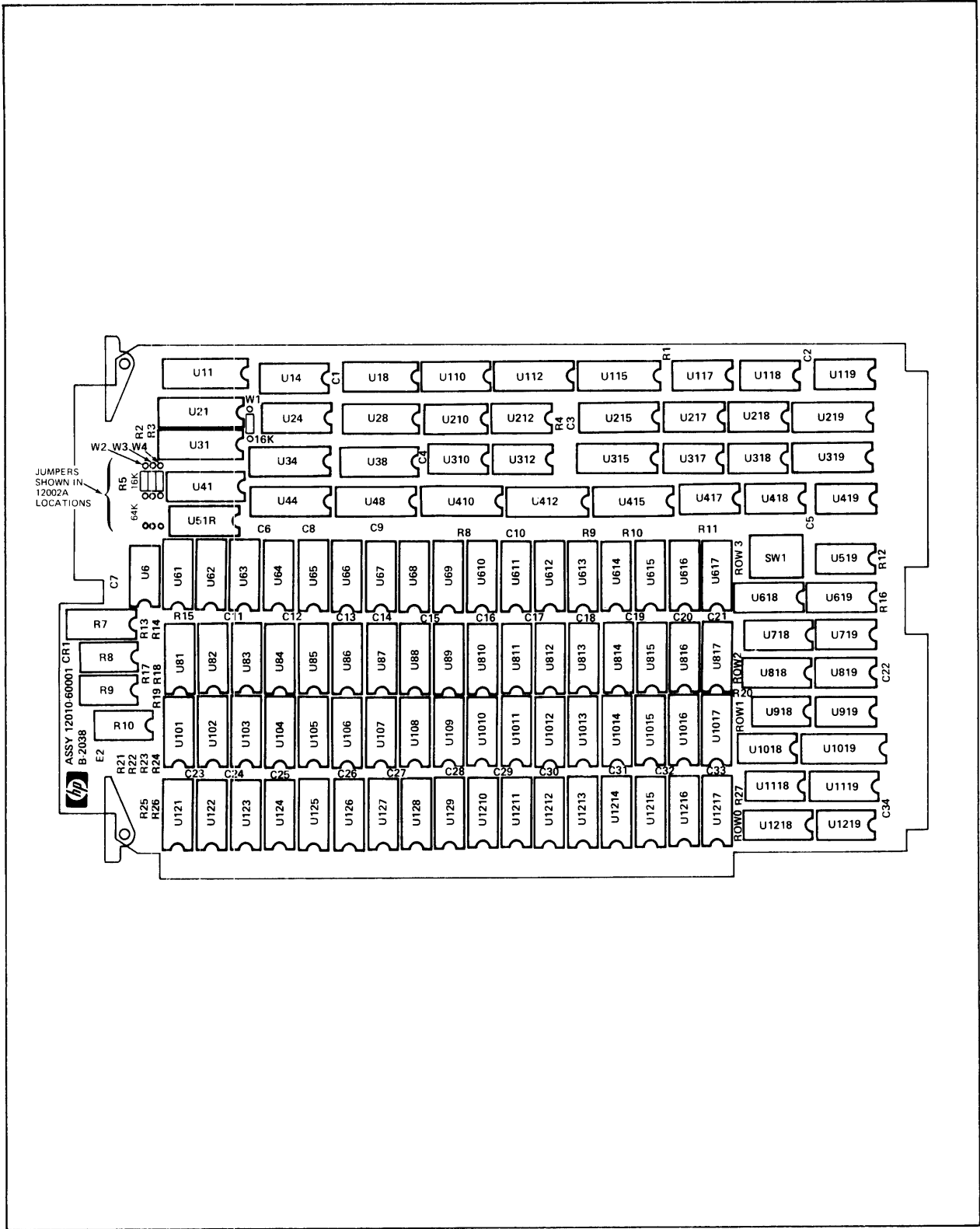


Figure 8-8. 12003A Parts Locations

Table 8-1. 12002A and 12002B Memory Parts List (Continued)

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|--|----------|-------------------|
| | 12002-60001 | 0 | 1 | AUTO SEQUENCING ASSEMBLY | 28480 | 12002-60001 |
| C1 | 0160-4842 | 6 | 34 | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C2 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C3 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C4 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C5 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C6 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C7 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C8 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C9 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C9 | 0180-0137 | 6 | 1 | CAPACITOR-FXD 100UF+-20% 10VDC TA | 56289 | 150D107X0010R2 |
| C10 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C10 | 0180-0393 | 6 | 1 | CAPACITOR-FXD 39UF+-10% 10VDC TA | 56289 | 150D396X9010R2 |
| C11 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C12 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C13 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C14 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C15 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C16 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C17 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C18 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C19 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C20 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C21 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C22 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C23 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C24 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C25 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C26 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C27 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C28 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C29 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C30 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C31 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C32 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C33 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| C34 | 0160-4842 | 6 | | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| CR1 | 1990-04B5 | 5 | 1 | LED-VISIBLE LUM-INT=800UCD IF=30MA-MAX | 28480 | 5082-4984 |
| E1 | 0360-1682 | 0 | 2 | TERMINAL-STUD SGL-TUR PRESS-MTG | 28480 | 0360-1682 |
| E2 | 0360-1682 | 0 | | TERMINAL-STUD SGL-TUR PRESS-MTG | 28480 | 0360-1682 |
| R1 | 0698-3447 | 4 | 13 | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R2 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R3 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R4 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R5 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R6 | 1810-0280 | 8 | 2 | NETWORK-RES 10-SIP10.0K OHM X 9 | 01121 | 210A103 |
| R7 | 1810-0280 | 8 | | NETWORK-RES 10-SIP10.0K OHM X 9 | 01121 | 210A103 |
| R8 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R9 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R10 | 0757-0294 | 9 | 1 | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF4C1/8-T0-17R8-F |
| R11 | 1810-0278 | 4 | 2 | NETWORK-RES 10-SIP3.3K OHM X 9 | 01121 | 210A332 |
| R12 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R13 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R14 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R15 | 0698-3435 | 0 | 8 | RESISTOR 36.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-36R3-F |
| R16 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R17 | 0698-3435 | 0 | | RESISTOR 36.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-36R3-F |
| R18 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R19 | 0698-3435 | 0 | | RESISTOR 36.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-36R3-F |
| R20 | 0683-2215 | 1 | 1 | RESISTOR 220 5% .25W FC TC=-400/+600 | 01121 | CB2215 |
| R21 | 0698-3435 | 0 | | RESISTOR 36.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-36R3-F |
| R22 | 0698-3435 | 0 | | RESISTOR 36.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-36R3-F |
| R23 | 0698-3435 | 0 | | RESISTOR 36.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-36R3-F |
| R24 | 0698-3435 | 0 | | RESISTOR 36.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-36R3-F |
| R25 | 0698-3447 | 4 | | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R26 | 0698-3435 | 0 | | RESISTOR 36.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-36R3-F |
| R27 | 1810-0278 | 4 | | NETWORK-RES 10-SIP3.3K OHM X 9 | 01121 | 210A332 |
| S1 | 3101-0642 | 5 | 1 | SWITCH-SL DPDT MINTR .5A 125VAC/DC PC | 28480 | 3101-0642 |
| U6 | 1820-1450 | 7 | 2 | IC BFR TTL S NAND QUAD 2-INP | 01295 | SN74S37N |
| U7 | 1820-1072 | 9 | 1 | IC DCDR TTL S 2-T0-4-LINE DUAL 2-INP | 01295 | SN74S139N |
| U8 | 1820-1989 | 7 | 1 | IC CNTR TTL LS BIN DUAL 4-BIT | 07263 | 74LS393PC |
| U9 | 1820-0681 | 4 | 3 | IC GATE TTL S NAND QUAD 2-INP | 01295 | SN74S00N |
| U10 | 1820-1450 | 7 | | IC BFR TTL S NAND QUAD 2-INP | 01295 | SN74S37N |

Table 8-1. 12002A and 12002B Memory Parts List (Continued)

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|-----------------------------------|----------|-----------------|
| U11 | 1820-1633 | 8 | 6 | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S240N |
| U14 | 1820-1871 | 6 | 2 | IC ADDR TTL S BIN FULL ADDR 4-BIT | 01295 | SN74S283N |
| U18 | 5180-0126 | E | 2 | IC-MAPPER | 28480 | 5180-0126 |
| U21 | 1820-1633 | 8 | | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S240N |
| U24 | 1820-1871 | 6 | | IC ADDR TTL S BIN FULL ADDR 4-BIT | 01295 | SN74S283N |
| U28 | 5180-0126 | 8 | | IC-MAPPER | 28480 | 5180-0126 |
| U31 | 1820-1633 | 8 | | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S240N |
| U34 | 1820-1633 | E | | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S240N |
| U38 | 1820-2024 | 3 | 1 | IC DRVR TTL LS LINE DRVR OCTL | 01295 | SN74LS244N |
| U41 | 1820-1917 | 1 | 1 | IC BFR TTL LS LINE DRVR OCTL | 01295 | SN74LS240N |
| U44 | 1820-1633 | 8 | | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S240N |
| U48 | 1820-2102 | E | 3 | IC LCH TTL LS D-TYPE OCTL | 01295 | SN74LS373N |
| U51 | 1810-0533 | 4 | 1 | NETWORK-RES 16-DIP33.0 OHM X 8 | 28480 | 1810-0533 |
| U61 | | | | | | |
| U62 | | | | | | |
| U63 | | | | | | |
| U64 | | | | | | |
| U65 | | | | | | |
| U66 | | | | | | |
| U67 | | | | | | |
| U68 | | | | | | |
| U69 | | | | | | |
| U81 | | | | | | |
| U82 | | | | | | |
| U83 | | | | | | |
| U84 | | | | | | |
| U85 | | | | | | |
| U86 | | | | | | |
| U87 | | | | | | |
| U88 | | | | | | |
| U89 | | | | | | |
| U101 | | | | | | |
| U102 | | | | | | |
| U103 | | | | | | |
| U104 | | | | | | |
| U105 | | | | | | |
| U106 | | | | | | |
| U107 | | | | | | |
| U108 | | | | | | |
| U109 | | | | | | |
| U110 | 1820-1641 | 8 | 2 | IC DRVR TTL LS BUS DRVR HEX 1-INP | 01295 | SN74LS365AN |
| U112 | 1820-1676 | 9 | 2 | IC LCH TTL S D-TYPE OCTL | 01295 | SN74S373N |
| U115 | 5180-0128 | 0 | 1 | | 28480 | 5180-0128 |
| U117 | 1820-1112 | 8 | 2 | IC FF TTL LS D-TYPE POS-EDGE-TRIG | 01295 | SN74LS74AN |
| U118 | 1813-0199 | 4 | 1 | | 28480 | 1813-0199 |
| U119 | 1820-1206 | 1 | 1 | IC GATE TTL LS NOR TPL 3-INP | 01295 | SN74LS27N |
| U121 | | | | | | |
| U122 | | | | | | |
| U123 | | | | | | |
| U124 | | | | | | |
| U125 | | | | | | |
| U126 | | | | | | |
| U127 | | | | | | |
| U128 | | | | | | |
| U129 | | | | | | |
| U210 | 1820-1641 | 8 | | IC DRVR TTL LS BUS DRVR HEX 1-INP | 01295 | SN74LS365AN |
| U212 | 1820-0683 | 6 | 2 | IC INV TTL S HEX 1-INP | 01295 | SN74S04N |
| U215 | 5180-0129 | 1 | 1 | IC-STATE MACH | 28480 | 5180-0129 |
| U217 | 1820-0689 | 2 | 1 | IC GATE TTL S NAND DUAL 4-INP | 01295 | SN74S22N |
| U218 | 1820-0693 | 8 | 1 | IC FF TTL S D-TYPE POS-EDGE-TRIG | 01295 | SN74S74N |
| U219 | 1820-2102 | 8 | | IC LCH TTL LS D-TYPE OCTL | 01295 | SN74LS373N |
| U310 | 1820-0681 | 4 | | IC GATE TTL S NAND QUAD 2-INP | 01295 | SN74S00N |
| U312 | 1820-1275 | 4 | 1 | IC GATE TTL S NOR DUAL 5-INP | 01295 | SN74S260N |
| U315 | 5180-0127 | 9 | 1 | IC-INST ENC | 28480 | 5180-0127 |
| U317 | 1820-0685 | 8 | 1 | IC GATE TTL S NAND TPL 3-INP | 01295 | SN74S10N |
| U318 | 1820-1322 | 2 | 2 | IC GATE TTL S NOR QUAD 2-INP | 01295 | SN74S02N |
| U319 | 1820-1676 | 9 | | IC LCH TTL S D-TYPE OCTL | 01295 | SN74S373N |
| U410 | 1820-1624 | 7 | 2 | IC BFR TTL S OCTL 1-INP | 01295 | SN74S241N |
| U412 | 1820-2102 | 8 | | IC LCH TTL LS D-TYPE OCTL | 01295 | SN74LS373N |
| U415 | 1820-1624 | 7 | | IC BFR TTL S OCTL 1-INP | 01295 | SN74S241N |
| U417 | 1820-0683 | 6 | | IC INV TTL S HEX 1-INP | 01295 | SN74S04N |
| U418 | 1820-1638 | 3 | 2 | IC GEN TTL S PAR GEN 9-BIT | 01295 | SN74S280N |
| U419 | 1820-1638 | 3 | | IC GEN TTL S PAR GEN 9-BIT | 01295 | SN74S280N |
| U502 | 1813-0189 | 2 | 1 | IC MISC TTL S | 0791F | HY-5002 |
| U519 | 1820-0694 | 9 | 1 | IC GATE TTL S EXCL-OR QUAD 2-INP | 01295 | SN74S86N |

Table 8-1. 12002A and 12002B Memory Parts List

| Reference Designation | HP Part Number | C | D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|---|---|-----|------------------------------------|----------|-----------------|
| U610 | * | | | | | | |
| U611 | * | | | | | | |
| U612 | * | | | | | | |
| U613 | * | | | | | | |
| U614 | * | | | | | | |
| U615 | * | | | | | | |
| U616 | * | | | | | | |
| U617 | * | | | | | | |
| U618 | 1820-0629 | 0 | | 5 | IC FF TTL S J-K NEG-EDGE-TRIG | 01295 | SN74S112N |
| U619 | 1820-0629 | 0 | | | IC FF TTL S J-K NEG-EDGE-TRIG | 01295 | SN74S112N |
| U718 | 1820-0629 | 0 | | | IC FF TTL S J-K NEG-EDGE-TRIG | 01295 | SN74S112N |
| U719 | 1820-1322 | 2 | | | IC GATE TTL S NOR QUAD 2-INP | 01295 | SN74S02N |
| U810 | * | | | | | | |
| U811 | * | | | | | | |
| U812 | * | | | | | | |
| U813 | * | | | | | | |
| U814 | * | | | | | | |
| U815 | * | | | | | | |
| U816 | * | | | | | | |
| U817 | * | | | | | | |
| U818 | 1820-0629 | 0 | | | IC FF TTL S J-K NEG-EDGE-TRIG | 01295 | SN74S112N |
| U819 | 1820-0681 | 4 | | | IC GATE TTL S NAND QUAD 2-INP | 01295 | SN74S00N |
| U918 | 1820-1201 | 6 | | 1 | IC GATE TTL LS AND QUAD 2-INP | 01295 | SN74LS08N |
| U919 | 1820-1112 | 8 | | | IC FF TTL LS D-TYPE POS-EDGE-TRIG | 01295 | SN74LS74AN |
| U1010 | * | | | | | | |
| U1011 | * | | | | | | |
| U1012 | * | | | | | | |
| U1013 | * | | | | | | |
| U1014 | * | | | | | | |
| U1015 | * | | | | | | |
| U1016 | * | | | | | | |
| U1017 | * | | | | | | |
| U1018 | 1820-1208 | 3 | | 1 | IC GATE TTL LS OR QUAD 2-INP | 01295 | SN74LS32N |
| U1019 | 1820-1633 | 8 | | | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S248N |
| U1118 | 1820-1144 | 6 | | 1 | IC GATE TTL LS NOR QUAD 2-INP | 01295 | SN74LS02N |
| U1119 | 1820-0629 | 0 | | | IC FF TTL S J-K NEG-EDGE-TRIG | 01295 | SN74S112N |
| U1210 | * | | | | | | |
| U1211 | * | | | | | | |
| U1212 | * | | | | | | |
| U1213 | * | | | | | | |
| U1214 | * | | | | | | |
| U1215 | * | | | | | | |
| U1216 | * | | | | | | |
| U1217 | * | | | | | | |
| U1218 | 1820-1991 | 1 | | 1 | IC CNTR TTL LS DECD DUAL 4-BIT | 01295 | SN74LS390N |
| U1219 | 1820-1203 | 8 | | 1 | IC GATE TTL LS AND TPL 3-INP | 01295 | SN74LS11N |
| W1 | 8159-0005 | 0 | | 4 | WIRE 22AWG W PVC 1X22 80C | 28480 | 8159-0005 |
| W2 | 8159-0005 | 0 | | | WIRE 22AWG W PVC 1X22 80C | 28480 | 8159-0005 |
| W3 | 8159-0005 | 0 | | | WIRE 22AWG W PVC 1X22 80C | 28480 | 8159-0005 |
| W4 | 8159-0005 | 0 | | | WIRE 22AWG W PVC 1X22 80C | 28480 | 8159-0005 |
| | 0403-0289 | 3 | | 2 | EXTR-PC BD RED POLYC .063-BD-THKNS | 28480 | 0403-0289 |
| | 7120-6830 | 9 | | 1 | LABEL-USA | 28480 | 7120-6830 |
| | | | | 68 | | | |
| | 1480-0116 | 8 | | 2 | PIN-GRV .062-IN-DIA .25-IN-LG STL | 28480 | 1480-0116 |

* The 12002A (part no. 12002-60001) and 12002B (part no. 12002-60002) are identical except for the IC parts in the above lists which are described with the asterisk (*) footnote reference. These IC parts are as follows:

12002A: HP Part Number 5180-0121, Qty = 68

12002B: HP Part Number 5180-0133, Qty = 68

Table 8-2. 12003A Memory Parts List

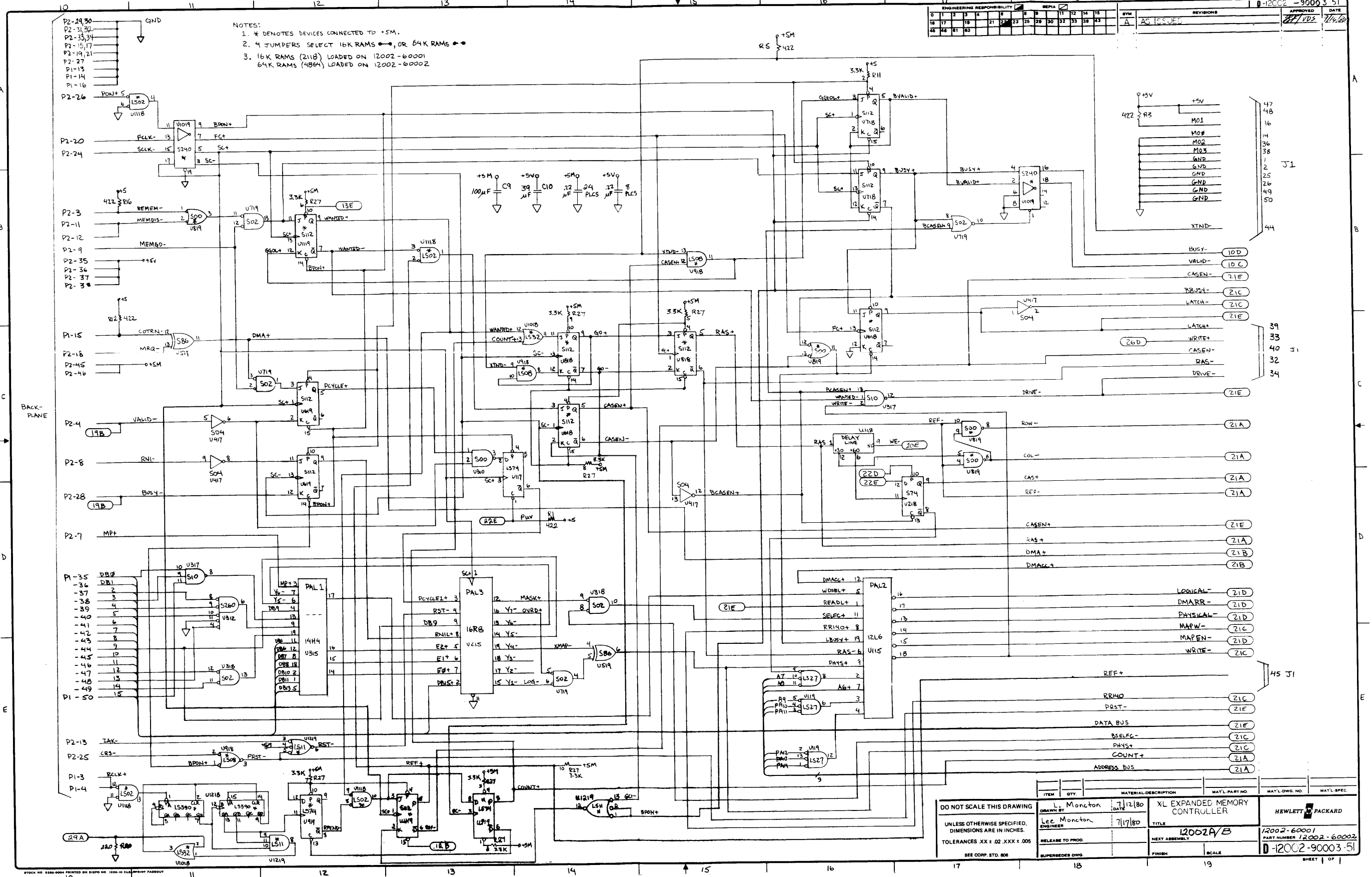
| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|---|----------|-------------------|
| A2 | 12003-60001 | 1 | 1 | PCA-XL MEMO | 28480 | 12003-60001 |
| C1- | | | | | | |
| C8 | 0180-0374 | 3 | 8 | CAPACITOR-FXD 10UF+-10% 20VDC TA | 56289 | 150D106X9020B2 |
| C9- | | | | | | |
| C42 | 0160-4842 | 6 | 34 | CAPACITOR-FXD .22UF +80-20% 50VDC CER | 28480 | 0160-4842 |
| CR1 | 1990-0485 | 5 | 1 | LED-VISIBLE LUM-INT=000UCD IF=30MA-MAX | 28480 | 5082-4984 |
| R1 | 1810-0277 | 3 | 2 | NETWORK-RES 10-SIP2.2K OHM X 9 | 01121 | 210A222 |
| R2 | 0698-3447 | 4 | 1 | RESISTOR 422 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-422R-F |
| R3- | | | | | | |
| R6 | 0757-0316 | 6 | 4 | RESISTOR 42.2 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-42R2-F |
| R7- | | | | | | |
| R10 | 0690-3435 | 0 | 4 | RESISTOR 38.3 1% .125W F TC=0+-100 | 24546 | C4-1/8-T0-38R3-F |
| R11 | 0757-0294 | 9 | 9 | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF401/8-T0-17R8-F |
| R12 | 1810-0277 | 3 | 1 | NETWORK-RES 10-SIP2.2K OHM X 9 | 01121 | 210A222 |
| R13- | | | | | | |
| R20 | 0757-0294 | 9 | 1 | RESISTOR 17.8 1% .125W F TC=0+-100 | 19701 | MF401/8-T0-17R8-F |
| R21 | 0683-2215 | 1 | 1 | RESISTOR 220 5% .25W FC TC=-400/+600 | 01121 | CB2215 |
| U104 | 1820-0694 | 9 | 1 | IC GATE TTL S EXCL-OR QUAD 2-INP | 01295 | SN74S86N |
| U105 | 1820-1441 | 6 | 1 | IC ADDR TTL LS BIN FULL ADDR 4-BIT | 01295 | SN74LS283N |
| U106 | 1820-0691 | 6 | 1 | IC GATE TTL S AND-OR-INV | 01295 | SN74S64N |
| U107 | 1820-1633 | 8 | 3 | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S240N |
| U109 | 1820-1633 | 8 | 1 | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S240N |
| U110 | 1820-1917 | 1 | 1 | IC BFR TTL LS LINE DRVR OCTL | 01295 | SN74LS240N |
| U113 | 1820-1624 | 7 | 2 | IC BFR TTL S OCTL 1-INP | 01295 | SN74S241N |
| U114 | 1820-2102 | 8 | 2 | IC LCH TTL LS D-TYPE OCTL | 01295 | SN74LS373N |
| U116 | 1820-1624 | 7 | 1 | IC BFR TTL S OCTL 1-INP | 01295 | SN74S241N |
| U117 | 1820-2102 | 8 | 1 | IC LCH TTL LS D-TYPE OCTL | 01295 | SN74LS373N |
| U118 | 1820-1989 | 7 | 1 | IC CNTR TTL LS BIN DUAL 4-BIT | 07263 | 74LS393PC |
| U202 | 1820-1072 | 9 | 1 | IC DCDR TTL S 2-T0-4-LINE DUAL 2-INP | 01295 | SN74S139N |
| U203 | 1820-1633 | 8 | 1 | IC BFR TTL S INV OCTL 1-INP | 01295 | SN74S240N |
| U204 | 5180-0121 | 3 | 68 | * | 28480 | 5180-0121 |
| U205 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U206 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U207 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U208 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U209 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U210 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U211 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U212 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U213 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U214 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U215 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U216 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U217 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U218 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U219 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U220 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U301 | 1820-0682 | 5 | 1 | IC GATE TTL S NAND QUAD 2-INP | 01295 | SN74S03N |
| U302 | 1820-1015 | 0 | 1 | IC MUXR/DATA-SEL TTL S 2-T0-1-LINE QUAD | 01295 | SN74S158N |
| U303 | 1820-1450 | 7 | 2 | IC BFR TTL S NAND QUAD 2-INP | 01295 | SN74S37N |
| U304 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U305 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U306 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U307 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U308 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U309 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U310 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U311 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U312 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U313 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U314 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U315 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U316 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U317 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U318 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U319 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U320 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U401 | 1820-1197 | 9 | 1 | IC GATE TTL LS NAND QUAD 2-INP | 01295 | SN74LS00N |
| U402 | 1820-0693 | 8 | 1 | IC FF TTL S D-TYPE POS-EDGE-TRIG | 01295 | SN74S74N |
| U403 | 1820-1450 | 7 | | IC BFR TTL S NAND QUAD 2-INP | 01295 | SN74S37N |
| U404 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |
| U405 | 5180-0121 | 3 | | * | 28480 | 5180-0121 |

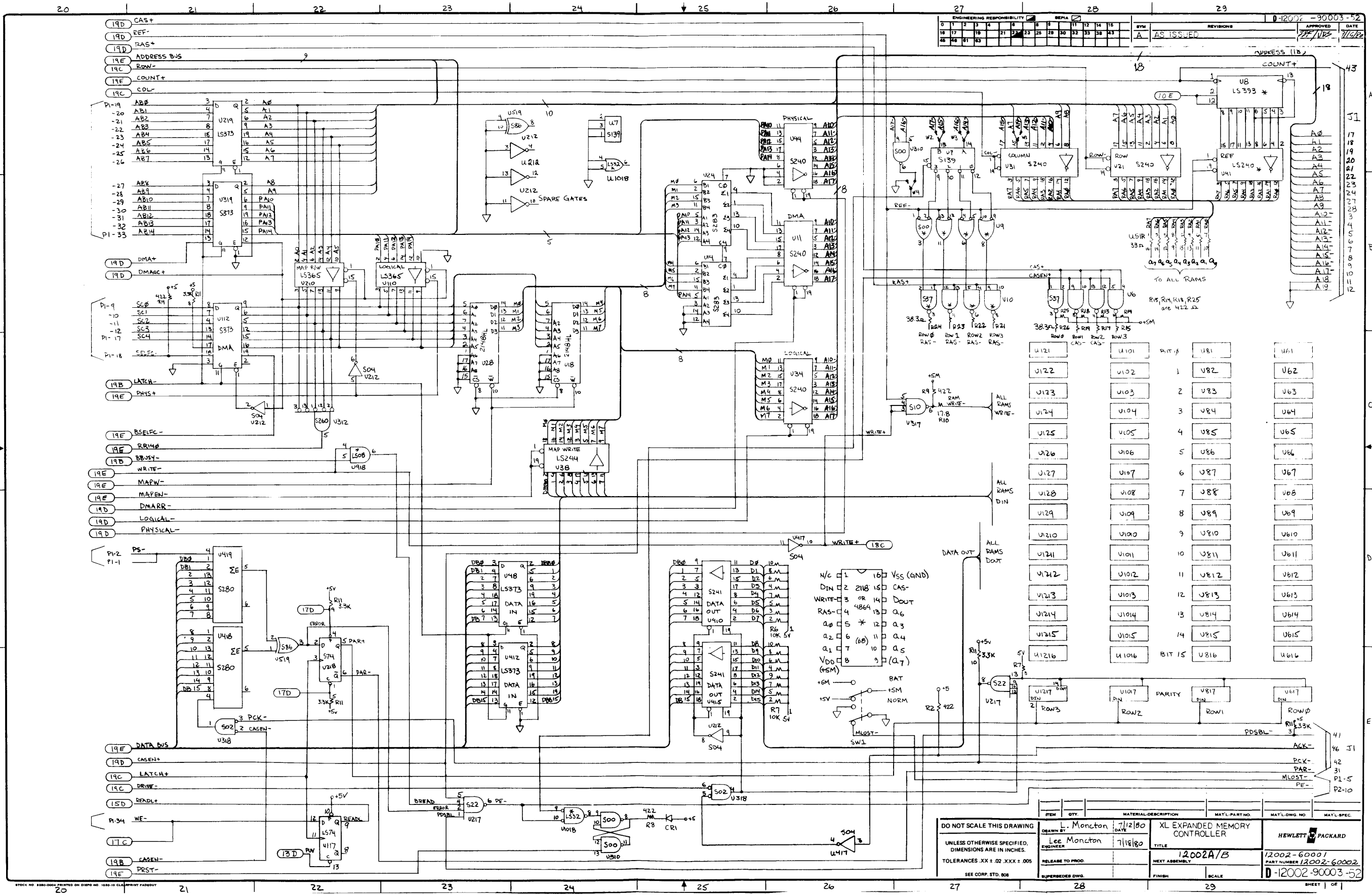
Table 8-2. 12003A Memory Parts List (Continued)

| Reference Designation | HP Part Number | C D | Qty | Description | Mfr Code | Mfr Part Number |
|-----------------------|----------------|-----|-----|-------------------------------|-----------|-----------------|
| U406 | 5180-0121 | 3 | | ↓ * | 28480 | 5180-0121 |
| U407 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U408 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U409 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U410 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U411 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U412 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U413 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U414 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U415 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U416 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U417 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U418 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U419 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U420 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U421 | 1820-1414 | 3 | 1 | IC GATE TTL LS NAND TPL 3-INP | 01295 | SN74LS12N |
| U503 | 1820-0681 | 4 | 1 | IC GATE TTL S NAND QUAD 2-INP | 01295 | SN74S00N |
| U504 | 5180-0121 | 3 | | ↑ * | 28480 | 5180-0121 |
| U505 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U506 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U507 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U508 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U509 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U510 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U511 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U512 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U513 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U514 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U515 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U516 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U517 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U518 | 5180-0121 | 3 | | | 28480 | 5180-0121 |
| U519 | 5180-0121 | 3 | | 28480 | 5180-0121 | |
| U520 | 5180-0121 | 3 | | 28480 | 5180-0121 | |
| W1 - W3 | 8159-0005 | 0 | 3 | WIRE 22AWG W PVC 1X22 80C | 28480 | 8159-0005 |

* HP PART NO. 5180-0121: 16,384X1 DYNAMIC RAM

| | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------------|---|---|---|---|---|---|---|---|---|----|----|----|----|----|---------|----|----|----|----|---------|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|----|
| ENGINEERING RESPONSIBILITY | | | | | | | | | | | | | | | REVISED | | | | | DATE | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | 35 | 36 | 37 | 38 | 39 | 40 | 41 | 42 | 43 | 44 | 45 | 46 | 47 | 48 | 49 | 50 |
| L. Mancton | | | | | | | | | | | | | | | 7/12/80 | | | | | 7/19/80 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

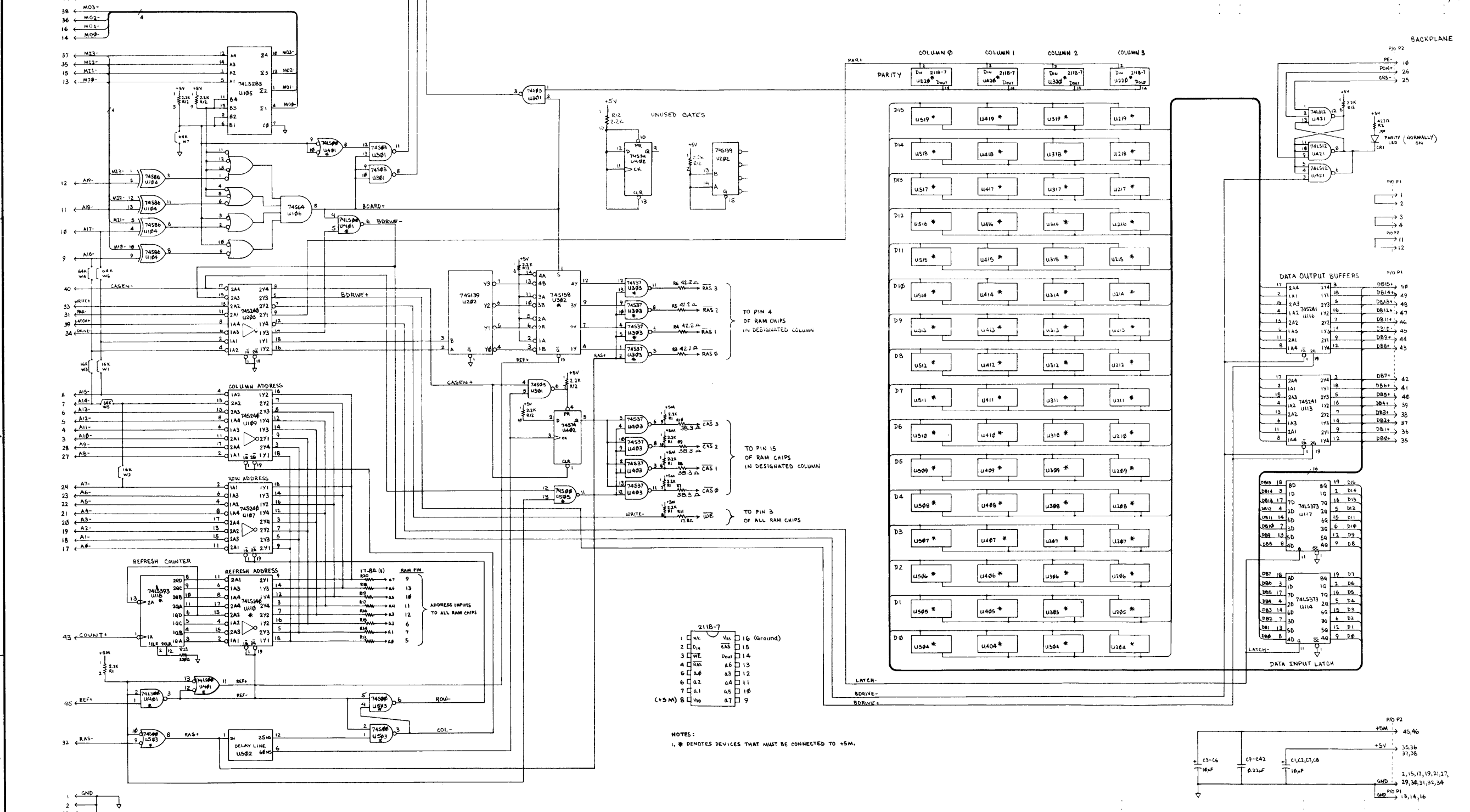




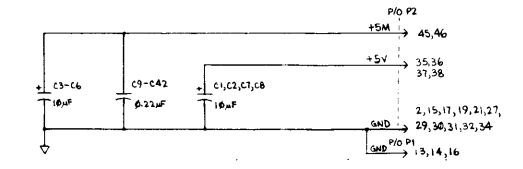
| ENGINEERING RESPONSIBILITY | | | | | | | | | | | | REVISIONS | | | | | | | | | | | | APPROVED | | DATE | |
|----------------------------|---|---|---|---|---|---|---|---|----|----|----|-----------|---|---|---|---|---|---|---|---|----|----|----|----------|---------|------|--|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | DATE | DATE | | |
| | | | | | | | | | | | | | | | | | | | | | | | | 7/12/80 | 7/12/80 | | |

| ITEM | QTY. | MATERIAL DESCRIPTION | MATL. PART NO. | MATL. DWG. NO. | MATL. SPEC. |
|------|------|----------------------|----------------|----------------|-------------|
| U101 | 1 | RAM | | | |
| U102 | 1 | RAM | | | |
| U103 | 2 | RAM | | | |
| U104 | 3 | RAM | | | |
| U105 | 4 | RAM | | | |
| U106 | 5 | RAM | | | |
| U107 | 6 | RAM | | | |
| U108 | 7 | RAM | | | |
| U109 | 8 | RAM | | | |
| U110 | 9 | RAM | | | |
| U111 | 10 | RAM | | | |
| U112 | 11 | RAM | | | |
| U113 | 12 | RAM | | | |
| U114 | 13 | RAM | | | |
| U115 | 14 | RAM | | | |
| U116 | 15 | RAM | | | |

| | | | | | | | |
|---|--|-----------------------|---------------|-------------------------------|--|--------------------------|--|
| DO NOT SCALE THIS DRAWING | | DRAWN BY: L. Moncton | DATE: 7/12/80 | XL EXPANDED MEMORY CONTROLLER | | HEWLETT PACKARD | |
| UNLESS OTHERWISE SPECIFIED, DIMENSIONS ARE IN INCHES. | | ENGINEER: Lee Moncton | DATE: 7/18/80 | TITLE: 12002A/B | | PART NUMBER: 12002-60002 | |
| TOLERANCES: .XX ± .02, .XXX ± .005 | | RELEASE TO PROD. | | NEXT ASSEMBLY: | | 12002-60001 | |
| SEE CORP. STD. 008 | | SUPERSEDES DWG. | | FINISH: | | D-12002-90003-52 | |



NOTES:
 1. * DENOTES DEVICES THAT MUST BE CONNECTED TO +5M.



| ITEM | QTY | MATERIAL DESCRIPTION | MAT'L PART NO | MAT'L DWG NO | MAT'L SPEC |
|---------------------------|-----|----------------------|---------------|-------------------------------|------------|
| DO NOT SCALE THIS DRAWING | | | | | |
| DRAWN BY Albert Chun | | DATE 1 July 1980 | | XL EXPANDED MEMORY ARRAY CARD | |
| ENGINEER Albert Chun | | DATE 10 July 1980 | | TITLE | |
| RELEASE TO PROD. | | NEXT ASSEMBLY | | PART NUMBER | |
| SEE CORP. STD. 808 | | SUBMITTED DWG. | | FINISH SCALE | |
| | | | | D-12003A-60001-51 | |

| | |
|-------------------------------------|------------|
| SELF-TEST, LOADER, AND VCP PROGRAMS | APPENDIX A |
|-------------------------------------|------------|

This appendix contains a listing of the self-test, loader, and the Virtual Control Panel programs contained in the HP 12001B processor card ROM.

The 4k ROM code is identified by HP part numbers 5180-0123 and 5180-0124 contained in ICs PTST-LB and PTST-HB, respectively. (The obsolete 2K ROM code is identified by HP part numbers 5090-1624 and 5090-1625). Refer to figure A-1 for the 4k ROM program layout.

It is suggested that users who create their own loaders implement them in PROM on the HP 12008A PROM Storage Module.

A user who intends to change the processor ROM code for any reason should keep in mind the following points.

1. A method was developed using standard coding to allow access to both RAM and ROM. The RAM area is necessary for storage and the ROM area is for instructions and constants. This method is referred to as A addressable and B addressable. If the instruction is A addressable, data is returned from ROM; if B addressable, the data is read from RAM. At the beginning of the ROM code listing is a reference for instructions and ROM versus RAM.
2. The ROM code space is not addressed as continuous pages but 1k pages that overlay the same 1k of RAM area (see figure A-1). This is done so that programs on any page can access the same storage area. The control bits for page selection are bit 7 and 8 with an OT* 1. The OT* also controls the processor LED's. When crossing over pages the area on both pages must be considered. Also, the listing is assembled starting at 4000 octal but the program can be set to execute on any 1k page.
3. The common storage area was set up for the last 64 words a 1K page. These are used by all three sections. When using these storage locations, make sure there is no interference or destruction of data from another area. This is important when writing loaders. This storage area can be on either the base page (page 0) for a computer with extended memory or the last page for a computer with only 32k words.
4. The area at the end of each page must be the same to allow a break to enter and go to the VCP code correctly.

5. The JSB usage is set up so that a JSB goes to the ROM area above the common storage area and there it is followed by a JMP routine. Note that this allows doubling up of address space and does not waste ROM area. The normal NOP used for the return address is used in ROM as the JMP instruction for the previous JSB.
6. All loaders must use the JSB S.SC call to set up the parameters for a load. This includes the select code, file number, unit, and subchannel. The file number is stored on the I/O chip in register 25 octal and is used for continuation (sequential) loads.
7. The temporary storage areas are set up at the same 1k address space, allowing cross communication between pages. When writing a loader, the storage areas are used as follows, where n in Pn is the page number:

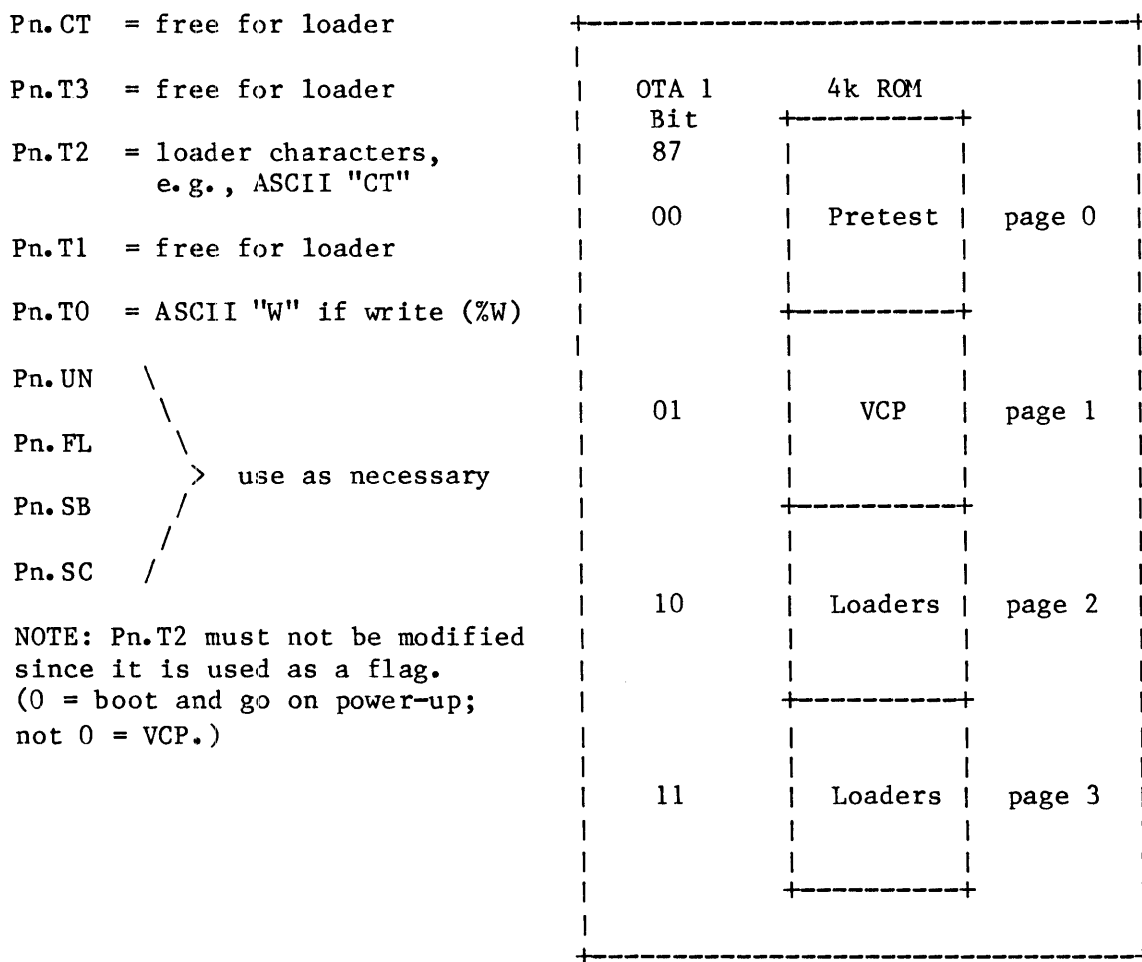


Figure A-1. Processor ROM Code Layout

The following pages contain an example 4k ROM listing. ROM firmware is subject to change; therefore, later versions will contain minor differences from this listing. (Note: There is a Cross Reference Symbol Table at the end of the listing.)

*

```

0001          ASMB,A,B,L,C          4K VERSION OF PROCESSOR PROMS
0003 00000          ORG 0
0004* *****
0005* * (C) COPYRIGHT HEWLETT-PACKARD COMPANY 1980. ALL RIGHTS *
0006* * RESERVED. NO PART OF THIS PROGRAM MAY BE PHOTOCOPIED, *
0007* * REPRODUCED OR TRANSLATED TO ANOTHER PROGRAM LANGUAGE WITHOUT *
0008* * THE PRIOR WRITTEN CONSENT OF HEWLETT-PACKARD COMPANY. *
0009* *****
0010*
0011* SOURCE: 24397-18001
0012*
0013*
0014*
0015* THE PROGRAMS IN THIS LISTING ARE IN THE FOLLOWING ORDER
0016*
0017* I. PRETEST (FOR CPU, MEMORY, AND I/O) PAGE 0
0018* II. VIRTUAL CONTROL PANEL (VCP) PAGE 1
0019* III. BOOT LOADERS PAGE 2 & 3
0020*
0021* DURING THE EXECUTION OF THE PROM PROGRAM THE FOLLOWING
0022* INSTRUCTION RULES APPLY FOR ACCESSING ROM VERSES RAM:
0023*
0024* AND >
0025* XDR >
0026* IOR > OPERAND IS
0027* LDA > FROM ROM ONLY
0028* CPA >
0029* ADA >
0030*
0031* ISZ >
0032* ADB > OPERAND IS
0033* LDB > FROM RAM ONLY
0034* CPR >
0035*
0036* JSB > RETURN ADDRESS IS WRITTEN TO RAM
0037* JMP ,I> ADDRESS IS FROM RAM
0038* STA/B > ALWAYS WRITTEN TO RAM
0039*
0040* ALL EAU INSTRUCTIONS GENERATE ROM ENABLE FOR THE SECOND WORD
0041* AND ALL OPERANDS ARE FROM ROM.
0042*
0043* THE RULE IS: ROM ENABLE = FETCH + (READ . IR11-) + EAU

```

0045* CPU STATUS IS OBTAINED BY A LIA/B 1
0046* SW 1 BIT 8 = ROOT SELECT 0
0047* 2 9 = ROOT SELECT 1
0048* 3 10 = ROOT SELECT 2
0049* 4 11 = ROOT SELECT 3
0050* 5 12 = SELECT ALTERNATE VCP DRIVER
0051* 6 13 = RESERVED
0052* - 14 = MEMORY LOST (LOW TRUE)
0053* 8 15 = INTERRUPT MASK BIT 1 FOR PROCESSOR BOARD
0054*
0055* SWITCH 7 IS RESERVED ON THE PROCESSOR FOR INT/EXT CLOCK
0056*
0057*
0058* CPU CONTROL OUTPUT BY AN OTA/B 1
0059* BIT 0-7 = STATUS LIGHT 0-7

*

```

0061 04000          ORG 4000B
0062                SUP
0063 00000          A    EQU 0          A-REG. REFERENCE
0064 00001          B    EQU 1          B-REG. REFERENCE
0065 04000          P0   EQU *          PAGE 0 REFERENCE
0066 00001          CPUT EQU 1          CPU STATUS REGISTER
0067 00030          DR   EQU 30B        DRIVER SC FOR DATA I/O
0068 00031          CTL  EQU 31B        " " " CONTROL
0069 00032          STS  EQU 32B        " " " STATUS
0070*
0071*      I.  PRETEST
0072*      THE PRETEST IS USED TO VRFIFY EXECUTION OF THE BASIC
0073*      INSTRUCTIONS USED IN THE BOOT LOADERS.  THE ASUMPTION IS
0074*      MADE THAT THE JMP INSTRUCTION IS FUNCTIONAL AND WILL BE
0075*      USED TO STOP EXECUTION.  THE PRETEST IS NOT ENTENDED TO
0076*      BE A COMPLETE CHECK OF THE CPU BUT ONLY THAT THE INSTRUCTIONS
0077*      USED IN THE BOOT APE FUNCTIONAL SO THAT A BOOT LOAD MAY BE
0078*      POSSIABLEF.
0079*
0080 04000 000000  ZERO  NOP          CONSTANT
0081 04001 004000  REV   OCT 4000    REVISION LEVEL 4K VERSION

0083*      ENTRY POINT AFTER POWER UP SELFTTEST SEQUENCE
0084 04002 024100  OCT 24100    MOVE IO START OF PRE-TEST
0085 04003 026514  JMP MTST+2    START WITH MEMORY
0086 04004 026711  JMP IPF      POWER FAIL INTERRUPT SO STOP
0087 04005 026652  JMP IPRTY   PARITY ERROR INTERRUPT
0088 04006 026460  JMP ITPG    TBG INTERRUPT
0089 04007 000000  NOP        IGNORE INTERRUPT
0090 04010 000000  NOP
0091                REP 7          ILLEGAL INTERRUPT LOCATIONS
0092 04011 027470  JMP ILINT
0092 04012 027470  JMP ILINT
0092 04013 027470  JMP ILINT
0092 04014 027470  JMP ILINT
0092 04015 027470  JMP ILINT
0092 04016 027470  JMP ILINT
0092 04017 027470  JMP ILINT

```

*

| 0094 | | REP 48 | I/O INTERRUPTS |
|------|-------|--------|----------------|
| 0095 | 04020 | 027317 | JMP IOINT |
| 0095 | 04021 | 027317 | JMP IOINT |
| 0095 | 04022 | 027317 | JMP IOINT |
| 0095 | 04023 | 027317 | JMP IOINT |
| 0095 | 04024 | 027317 | JMP IOINT |
| 0095 | 04025 | 027317 | JMP IOINT |
| 0095 | 04026 | 027317 | JMP IOINT |
| 0095 | 04027 | 027317 | JMP IOINT |
| 0095 | 04030 | 027317 | JMP IOINT |
| 0095 | 04031 | 027317 | JMP IOINT |
| 0095 | 04032 | 027317 | JMP IOINT |
| 0095 | 04033 | 027317 | JMP IOINT |
| 0095 | 04034 | 027317 | JMP IOINT |
| 0095 | 04035 | 027317 | JMP IOINT |
| 0095 | 04036 | 027317 | JMP IOINT |
| 0095 | 04037 | 027317 | JMP IOINT |
| 0095 | 04040 | 027317 | JMP IOINT |
| 0095 | 04041 | 027317 | JMP IOINT |
| 0095 | 04042 | 027317 | JMP IOINT |
| 0095 | 04043 | 027317 | JMP IOINT |
| 0095 | 04044 | 027317 | JMP IOINT |
| 0095 | 04045 | 027317 | JMP IOINT |
| 0095 | 04046 | 027317 | JMP IOINT |
| 0095 | 04047 | 027317 | JMP IOINT |
| 0095 | 04050 | 027317 | JMP IOINT |
| 0095 | 04051 | 027317 | JMP IOINT |
| 0095 | 04052 | 027317 | JMP IOINT |
| 0095 | 04053 | 027317 | JMP IOINT |
| 0095 | 04054 | 027317 | JMP IOINT |
| 0095 | 04055 | 027317 | JMP IOINT |
| 0095 | 04056 | 027317 | JMP IOINT |
| 0095 | 04057 | 027317 | JMP IOINT |
| 0095 | 04060 | 027317 | JMP IOINT |
| 0095 | 04061 | 027317 | JMP IOINT |
| 0095 | 04062 | 027317 | JMP IOINT |
| 0095 | 04063 | 027317 | JMP IOINT |
| 0095 | 04064 | 027317 | JMP IOINT |
| 0095 | 04065 | 027317 | JMP IOINT |
| 0095 | 04066 | 027317 | JMP IOINT |
| 0095 | 04067 | 027317 | JMP IOINT |
| 0095 | 04070 | 027317 | JMP IOINT |
| 0095 | 04071 | 027317 | JMP IOINT |
| 0095 | 04072 | 027317 | JMP IOINT |
| 0095 | 04073 | 027317 | JMP IOINT |
| 0095 | 04074 | 027317 | JMP IOINT |
| 0095 | 04075 | 027317 | JMP IOINT |
| 0095 | 04076 | 027317 | JMP IOINT |
| 0095 | 04077 | 027317 | JMP IOINT |

*

0097* THE FOLLOWING INSTRUCTIONS CHECK THE CPU CHIP ONLY

0098*

| | | | | | | | | | |
|------|-------|--------|-------|-----------------|---------------------------|----------|-----|-----|------|
| 0099 | 04100 | 002701 | START | CLA,CCE,RSS | A=000000 | B=XXXXXX | E=1 | O=X | +SKP |
| 0100 | 04101 | 026101 | JMP * | | RSS FAILED | | | | |
| 0101 | 04102 | 006440 | | CLP,SEZ | A=000000 | B=000000 | E=1 | O=X | -SKP |
| 0102 | 04103 | 002102 | | CLE,SZA | A=000000 | B=000000 | E=0 | O=X | +SKP |
| 0103 | 04104 | 026104 | JMP * | | CCE-SEZ OR CLA-SZA FAILED | | | | |
| 0104 | 04105 | 003041 | | CMA,SEZ,RSS | A=177777 | B=000000 | E=0 | O=X | -SKP |
| 0105 | 04106 | 006202 | | CME,SZB | A=177777 | B=000000 | E=1 | O=X | +SKP |
| 0106 | 04107 | 026107 | JMP * | | CCE OR CLB-SZB FAILED | | | | |
| 0107 | 04110 | 007040 | | CMB,SEZ | A=177777 | B=177777 | E=1 | O=X | -SKP |
| 0108 | 04111 | 006003 | | SZB,RSS | | | | | +SKP |
| 0109 | 04112 | 026112 | JMP * | | CME OR CMB FAILED | | | | |
| 0110 | 04113 | 050001 | | CPA B | | | | | -SKP |
| 0111 | 04114 | 002414 | | CLA,SLA,INA | A=000001 | B=177777 | E=1 | O=X | +SKP |
| 0112 | 04115 | 026115 | JMP * | | CMA-CPA B-SLA,INA FAILED | | | | |
| 0113 | 04116 | 002002 | | SZA | | | | | -SKP |
| 0114 | 04117 | 002020 | | SSA | | | | | +SKP |
| 0115 | 04120 | 026120 | JMP * | | INA OR SSA FAILED | | | | |
| 0116 | 04121 | 006400 | | CLB | A=000001 | B=000000 | E=1 | O=X | |
| 0117 | 04122 | 003420 | | CCA,SSA | A=177777 | B=000000 | | | -SKP |
| 0118 | 04123 | 002003 | | SZA,RSS | | | | | +SKP |
| 0119 | 04124 | 026124 | JMP * | | CCA-SSA OR SZA,RSS FAILED | | | | |
| 0120 | 04125 | 000010 | | SLA | | | | | -SKP |
| 0121 | 04126 | 002131 | | CLF,SSA,SLA,RSS | A=177777 | B=000000 | E=0 | O=X | +SKP |
| 0122 | 04127 | 026127 | JMP * | | SLA OR SSA,SLA,RSS FAILED | | | | |
| 0123 | 04130 | 102101 | | STO | A=177777 | B=000000 | E=0 | O=1 | |
| 0124 | 04131 | 102201 | | SOC | | | | | -SKP |
| 0125 | 04132 | 102301 | | SOS | | | | | +SKP |
| 0126 | 04133 | 026133 | JMP * | | STO-SOC-SOS FAILED | | | | |
| 0127 | 04134 | 103101 | | CLO | A=177777 | B=000000 | E=0 | O=0 | |
| 0128 | 04135 | 102301 | | SOS | | | | | -SKP |
| 0129 | 04136 | 102201 | | SOC | | | | | +SKP |
| 0130 | 04137 | 026137 | JMP * | | CLO-SOS-SOC FAILED | | | | |

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| | | | | | | | | |
|------|-------|--------|----------|-----------------------------|----------|-----|-----|------|
| 0132 | 04140 | 063573 | LDA ALT1 | A=125252 | R=000000 | E=0 | O=0 | |
| 0133 | 04141 | 006003 | SZB,RSS | | | | | |
| 0134 | 04142 | 050001 | CPA B | | | | | +SKP |
| 0135 | 04143 | 026143 | JMP * | CPA B OR CLB-SZB,RSS FAILED | | | | |
| 0136 | 04144 | 053573 | CPA ALT1 | | | | | -SKP |
| 0137 | 04145 | 070001 | STA B | A=125252 | R=125252 | E=0 | O=0 | |
| 0138 | 04146 | 063573 | LDA ALT1 | | | | | |
| 0139 | 04147 | 054000 | CPB A | | | | | +SKP |
| 0140 | 04150 | 003401 | CCA,RSS | A=177777 | B=125252 | E=0 | O=0 | +SKP |
| 0141 | 04151 | 026151 | JMP * | CPA-STA-CPR FAILED | | | | |
| 0142 | 04152 | 013572 | AND ALTO | A=052525 | R=125252 | E=0 | O=0 | |
| 0143 | 04153 | 053572 | CPA ALTO | | | | | -SKP |
| 0144 | 04154 | 002001 | RSS | | | | | +SKP |
| 0145 | 04155 | 026155 | JMP * | AND-CPA FAILED | | | | |
| 0146 | 04156 | 013573 | AND ALT1 | A=000000 | R=125252 | E=0 | O=0 | |
| 0147 | 04157 | 002002 | SZA | | | | | +SKP |
| 0148 | 04160 | 026160 | JMP * | AND FAILED | | | | |
| 0149 | 04161 | 063544 | LDA B24 | A=000024 | B=125252 | E=0 | O=0 | |
| 0150 | 04162 | 033572 | IOR ALTO | A=052525 | R=125252 | E=0 | O=0 | |
| 0151 | 04163 | 053572 | CPA ALTO | | | | | -SKP |
| 0152 | 04164 | 003401 | CCA,RSS | A=177777 | B=125252 | E=0 | O=0 | +SKP |
| 0153 | 04165 | 026165 | JMP * | XOR FILED | | | | |
| 0154 | 04166 | 023573 | XOR ALT1 | A=052525 | R=125252 | E=0 | O=0 | |
| 0155 | 04167 | 053572 | CPA ALTO | | | | | -SKP |
| 0156 | 04170 | 002440 | CLA,SEZ | A=000000 | R=125252 | E=0 | O=0 | +SKP |
| 0157 | 04171 | 026171 | JMP * | IOR-XOR FAILED | | | | |
| 0158 | 04172 | 043573 | ADA ALT1 | A=125252 | R=125252 | E=0 | O=0 | |
| 0159 | 04173 | 053573 | CPA ALT1 | | | | | -SKP |
| 0160 | 04174 | 002040 | SEZ | | | | | +SKP |
| 0161 | 04175 | 026175 | JMP * | CLA OR ADA FAILED | | | | |
| 0162 | 04176 | 043572 | ADA ALTO | A=177777 | R=125252 | E=0 | O=0 | |
| 0163 | 04177 | 102301 | SOS | | | | | -SKP |
| 0164 | 04200 | 003002 | CMA,SZA | A=000000 | B=125252 | E=0 | O=0 | +SKP |
| 0165 | 04201 | 026201 | JMP * | ADA FAILED | | | | |
| 0166 | 04202 | 003440 | CCA,SEZ | A=177777 | B=125252 | E=0 | O=0 | +SKP |
| 0167 | 04203 | 026203 | JMP * | ADA FAILED | | | | |
| 0168 | 04204 | 043567 | ADA M1 | A=177776 | R=125252 | E=1 | O=0 | |
| 0169 | 04205 | 053570 | CPA M2 | | | | | -SKP |
| 0170 | 04206 | 002041 | SEZ,PSS | | | | | +SKP |
| 0171 | 04207 | 026207 | JMP * | ADA FAILED | | | | |
| 0172 | 04210 | 102301 | SOS | | | | | -SKP |
| 0173 | 04211 | 002101 | CLE,RSS | A=177776 | R=125252 | E=0 | O=0 | +SKP |
| 0174 | 04212 | 026212 | JMP * | ADA FAILED | | | | |
| 0175 | 04213 | 034000 | ISZ A | A=177777 | R=125252 | E=0 | O=0 | -SKP |
| 0176 | 04214 | 034000 | ISZ A | A=000000 | R=125252 | E=0 | O=0 | +SKP |
| 0177 | 04215 | 026215 | JMP * | ISZ FAILED | | | | |

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|------|-------|--------|-------------|---------------------|----------|-----|-----|------|
| 0179 | 04216 | 063566 | LDA B100K | A=100000 | B=125252 | E=0 | O=0 | |
| 0180 | 04217 | 043567 | ADA M1 | A=077777 | B=125252 | E=1 | O=1 | |
| 0181 | 04220 | 102201 | SOC | | | | | -SKP |
| 0182 | 04221 | 002141 | SEZ,CLE,RSS | A=077777 | B=125252 | E=0 | O=1 | +SKP |
| 0183 | 04222 | 026222 | JMP * | ADA FAILED | | | | |
| 0184 | 04223 | 103101 | CLO | A=077777 | R=125252 | E=0 | O=0 | |
| 0185 | 04224 | 002004 | INA | A=100000 | R=125252 | E=0 | O=1 | |
| 0186 | 04225 | 053566 | CPA B100K | | | | | -SKP |
| 0187 | 04226 | 002040 | SEZ | | | | | +SKP |
| 0188 | 04227 | 026227 | JMP * | ADA FAILED | | | | |
| 0189 | 04230 | 060001 | LDA B | A=125252 | B=125252 | E=0 | O=1 | |
| 0190 | 04231 | 053573 | CPA ALT1 | | | | | -SKP |
| 0191 | 04232 | 103301 | SOS C | A=125252 | B=125252 | E=0 | O=0 | +SKP |
| 0192 | 04233 | 026233 | JMP * | B-REG. WAS MODIFIED | | | | |

0194* THE FOLLOWING SEQUENCE IS USED TO CHECK

0195* JSR, JMP X,I, AND STA X,I

0196*

| | | | | |
|------|-------|--------|----------------------|-----------------------------|
| 0197 | 04234 | 062255 | LDA PTJPR | GET RETURN IN B-REG. |
| 0198 | 04235 | 064000 | LDB A | CHANGE HANDS |
| 0199 | 04236 | 014000 | JSR 0 | |
| 0200 | 04237 | 026237 | JMP * | JSR FAILED |
| 0201 | 04240 | 052254 | PTRT0 CPA PTDF1 | CORRECT RETURN ADDRESS? |
| 0202 | 04241 | 002301 | CCE,RSS | YES |
| 0203 | 04242 | 026242 | JMP * | NO |
| 0204 | 04243 | 062253 | LDA PTDF0 | SET PAGE ADDRESS |
| 0205 | 04244 | 173533 | STA B1,I | PUT IT IN B-REG. INDIRECTLY |
| 0206 | 04245 | 050001 | CPA B | |
| 0207 | 04246 | 162253 | LDA PTDF0,I | |
| 0208 | 04247 | 006004 | INB | |
| 0209 | 04250 | 052256 | CPA PTJMP | INDIRECT OK? |
| 0210 | 04251 | 024000 | JMP 0 | YES EXECUTE B-REG. |
| 0211 | 04252 | 026252 | JMP * | |
| 0212 | 04253 | 000256 | PTDF0 DEF *+3-P0 | |
| 0213 | 04254 | 000237 | PTDF1 DEF PTRT0-P0-1 | |
| 0214 | 04255 | 026240 | PTJPR JMP PTRT0 | |
| 0215 | 04256 | 124001 | PTJMP JMP 1,I | |

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| | | | | B-REG. | E | A-REG. |
|------|-------|--------|-------------|------------------|---|------------------|
| 0217 | 04257 | 063574 | LDA SRGP1 | | | |
| 0218 | 04260 | 064000 | LDB A | 1000100100100111 | 1 | |
| 0219 | 04261 | 063575 | LDA SRGP2 | | 1 | 1001100000100000 |
| 0220 | 04262 | 005025 | BLS,ERB | 1100100100100111 | 0 | |
| 0221 | 04263 | 005661 | ELB,CLE,BRS | 1100100100100111 | 0 | |
| 0222 | 04264 | 001124 | ARS,ALP | | 0 | 0001100000100000 |
| 0223 | 04265 | 005026 | BLS,ELB | 0100100100100111 | 0 | |
| 0224 | 04266 | 005523 | ERB,RBP | 0100100100100111 | 0 | |
| 0225 | 04267 | 001720 | ALF,ALS | | 0 | 1000010000000010 |
| 0226 | 04270 | 005124 | BRS,BLR | 0100100100100110 | 0 | |
| 0227 | 04271 | 001330 | RAR,SLA,ALS | | 0 | 0000010000000010 |
| 0228 | 04272 | 005221 | RBL,BRS | 1100100100100110 | 0 | |
| 0229 | 04273 | 002300 | CCE | | 1 | |
| 0230 | 04274 | 001726 | ALF,ELA | | 0 | 1000000001000001 |
| 0231 | 04275 | 001522 | ERA,RAL | | 1 | 1000000001000000 |
| 0232 | 04276 | 005427 | BLR,BLF | 0010010011000001 | 1 | |
| 0233 | 04277 | 001122 | ARS,RAL | | 1 | 1000000001000001 |
| 0234 | 04300 | 005220 | RBL,BLS | 0001001100000100 | 1 | |
| 0235 | 04301 | 001135 | ARS,SLA,ERA | | 0 | 1110000000010000 |
| 0236 | 04302 | 026302 | JMP * | SLA FAILED | | |
| 0237 | 04303 | 001623 | ELA,RAR | | 1 | 0110000000010000 |
| 0238 | 04304 | 005327 | RBR,BLF | 1001100000100000 | | |
| 0239 | 04305 | 002040 | SEZ | CHECK E-REG. | | |
| 0240 | 04306 | 001460 | ALR,CLF,ALS | | | 0000000001000000 |
| 0241 | 04307 | 053576 | CPA SRGP3 | | | |
| 0242 | 04310 | 102201 | SUC | | | |
| 0243 | 04311 | 026311 | JMP * | SRG INST A-REG. | | |
| 0244 | 04312 | 060001 | LDA B | CHANGE HANDS | | |
| 0245 | 04313 | 053575 | CPA SRGP2 | | | |
| 0246 | 04314 | 006640 | CLB,SEZ,CMF | | | |
| 0247 | 04315 | 026315 | JMP * | SRG INST B-REG. | | |

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|------|-------|--------|-----------|---------------------------|----------|-----|-----|
| 0249 | 04316 | 102101 | STO | START WITH 0 SET | | | |
| 0250 | 04317 | 063600 | LDA BEAUS | SET B=130272 | | | |
| 0251 | 04320 | 064000 | LDB A | AND | | | |
| 0252 | 04321 | 063577 | LDA AEAUS | A=076310 | E=1 | | |
| 0253 | 04322 | 101021 | ASR 1 | A=037144 | B=154135 | E=1 | O=0 |
| 0254 | 04323 | 102301 | SOS | | | | |
| 0255 | 04324 | 100117 | RRL 15 | A=066056 | R=117462 | E=1 | O=0 |
| 0256 | 04325 | 100022 | ASL 2 | A=130270 | R=176311 | E=1 | O=1 |
| 0257 | 04326 | 102201 | SOC | | | | |
| 0258 | 04327 | 101100 | RRR 16 | A=176311 | R=130270 | | |
| 0259 | 04330 | 100041 | LSL 1 | A=174622 | R=060561 | | |
| 0260 | 04331 | 101025 | ASR 5 | A=107714 | B=001413 | | O=0 |
| 0261 | 04332 | 053601 | CPA ASR.0 | CHECK PRLIMINARY RESULTS | | | |
| 0262 | 04333 | 102201 | SOC | | | | |
| 0263 | 04334 | 026334 | JMP * | EAU SHIFT FAILED | | | |
| 0264 | 04335 | 101040 | LSR 16 | A=01413 | R=0 | | |
| 0265 | 04336 | 006002 | SZB | INSURE B WAS CLEARED | | | |
| 0266 | 04337 | 026337 | JMP * | WASN'T EAU SHIFT FAILED | | | |
| 0267 | 04340 | 102101 | STO | | | | |
| 0268 | 04341 | 100020 | ASL 16 | A=0 | R=001413 | | |
| 0269 | 04342 | 102301 | SOS | | | | |
| 0270 | 04343 | 100026 | ASL 6 | A=0 | R=041300 | | |
| 0271 | 04344 | 102201 | SOC | | | | |
| 0272 | 04345 | 101100 | RRR 16 | A=041300 | R=0 | | |
| 0273 | 04346 | 053602 | CPA ASR.1 | FINAL OK? | | | |
| 0274 | 04347 | 006002 | SZB | | | | |
| 0275 | 04350 | 026350 | JMP * | NO EAU SHIFT FAILED | | | |
| 0276 | 04351 | 063565 | LDA B76K | A=076000 | R=XXXXXX | E=X | O=X |
| 0277 | 04352 | 102101 | STO | | | | O=1 |
| 0278 | 04353 | 100200 | MPY B6412 | A=154000 | R=003120 | E=X | O=0 |
| 0279 | 04355 | 102201 | SOC | | | | |
| 0280 | 04356 | 026356 | JMP * | O WAS NOT CLEARED BY MPY | | | |
| 0281 | 04357 | 100400 | DIV ALT1 | A=166416 | R=020264 | | |
| 0282 | 04361 | 100200 | MPY MU2 | A=156224 | R=002046 | | |
| 0283 | 04363 | 100400 | DIV B7777 | A=041161 | R=007405 | | |
| 0284 | 04365 | 100101 | RRL 1 | A=102342 | R=017012 | | |
| 0285 | 04366 | 100200 | MPY ALTO | A=024412 | R=15336 | | |
| 0286 | 04370 | 100400 | DIV B76K | A=125507 | R=142412 | | |
| 0287 | 04372 | 100200 | MPY ALT1 | A=161446 | R=016075 | | |
| 0288 | 04374 | 102101 | STO | | | | O=1 |
| 0289 | 04375 | 100400 | DIV DV4 | A=126760 | B=006606 | | |
| 0290 | 04377 | 053605 | CPA RESUA | RESULT IN A | | | |
| 0291 | 04400 | 102201 | SOC | O=0 | | | |
| 0292 | 04401 | 026401 | JMP * | MPY OR DIV FAILED | | | |
| 0293 | 04402 | 101100 | RRR 16 | CHANGE HANDS | | | |
| 0294 | 04403 | 053606 | CPA RESUB | RESULT IN B | | | |
| 0295 | 04404 | 026406 | JMP **2 | | | | |
| 0296 | 04405 | 026405 | JMP * | MPY OR DIV ERROR | | | |
| 0297 | 04406 | 100400 | DIV B1 | TRY OVER FLOW | | | |
| 0298 | 04410 | 102301 | SOS | WAS IT ? | | | |
| 0299 | 04411 | 026411 | JMP * | NO | | | |
| 0300 | 04412 | 100400 | DIV ZERO | TRY ZERO TO SET OVER FLOW | | | |
| 0301 | 04414 | 102301 | SOS | WAS IT ? | | | |
| 0302 | 04415 | 026415 | JMP * | NO | | | |

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0304*      BASIC I/O ON CPU BOARD
0305*
0306 04416 106705      CLC 5          TURN OF PARITY SYSTEM
0307 04417 002404      CLA,INA      INDICAT (IF POSSIABLE) IN IO TEST
0308 04420 102601      OTA CPUST
0309 04421 063572      LDA ALTO      CHECK OT* AND LI*
0310 04422 064000      LDB A        CHANGE HANDS
0311 04423 063573      LDA ALT1      AND VIOLATION - PARITY REGISTERS
0312 04424 102605      OTA 5
0313 04425 107607      OTB 7,C
0314 04426 002400      CLA
0315 04427 103507      LIA 7,C
0316 04430 106505      LIB 5
0317 04431 020001      XOR B
0318 04432 003000      CMA
0319 04433 001665      ELA,CLF,ERA
0320 04434 002002      SZA          SHOULD COME OUT ZERO
0321 04435 027466      JMP PROER    OT* LI* FAILED (OR REGISTER 5.7)
0322 04436 102300      SFS 0        CHECK INTERRUPT FF
0323 04437 102200      SFC 0
0324 04440 027466      JMP PROER    INTERRUPT FF ERROR
0325 04441 102202      SFC 2        CHECK GLOBAL REG.
0326 04442 102302      SFS 2        SHOULD BE OFF (FLAG SET)
0327 04443 027466      JMP PROER    GLOBAL REG. ERROR
0328 04444 107706      CLC 6,C      INSURE TBG IS OFF
0329 04445 102100      STF 0        TURN ON INTERRUPTS
0330 04446 102200      SFC 0        CHECK IT
0331 04447 102300      SFS 0
0332 04450 027466      JMP PROER    INTERRUPTS NOT ON

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|-------|-------|--------|------|-----------|------------------------------------|
| 0334 | 04451 | 106501 | | LIB CPUT | SAVE TBG MASK BIT |
| 0335 | 04452 | 102600 | | OTA 0 | CLEAR INTERRUPT MASK |
| 0336 | 04453 | 102604 | | OTA 4 | CLEAR INTERRUPT REGISTER |
| 0337 | 04454 | 103706 | | STC 6,C | TRY TIME BASE TIC |
| 0338 | 04455 | 002006 | | INA,SZA | NOW WAIT FOR TIC |
| 0339 | 04456 | 026455 | | JMP *-1 | |
| 0340 | 04457 | 027466 | | JMP PROER | LONG ENOUGH NOW ERROR |
| 0341* | | | | | |
| 0342 | 04460 | 103100 | ITBG | CLF 0 | TURN OF INTERRUPTS |
| 0343 | 04461 | 107706 | | CLC 6,C | TURN OFF TIC |
| 0344 | 04462 | 102504 | | LIA 4 | CHECK CENTRAL INTERRUPT |
| 0345 | 04463 | 053540 | | CPA B6 | WAS IT THE TBG? |
| 0346 | 04464 | 102206 | | SFC 6 | FLAG SHOULD STAY CLEAR |
| 0347 | 04465 | 027466 | | JMP PROER | NOT SO ERROR (OR CIR NOT = 6) |
| 0348 | 04466 | 102501 | | LIA CPUT | |
| 0349 | 04467 | 002020 | | SSA | DID IT STAY CLEAR? |
| 0350 | 04470 | 027466 | | JMP PROER | NO PROCESSOR ERROR |
| 0351 | 04471 | 063534 | | LDA B2 | NOW SET MASK BIT |
| 0352 | 04472 | 102600 | | OTA 0 | |
| 0353 | 04473 | 102501 | | LIA CPUT | GET MASK BIT |
| 0354 | 04474 | 002021 | | SSA,RSS | DID IT SET |
| 0355 | 04475 | 027466 | | JMP PROER | NO THEN ERROR |
| 0356 | 04476 | 002400 | | CLA | NOW RESTORE MASK BIT |
| 0357 | 04477 | 006021 | | SSB,RSS | |
| 0358 | 04500 | 102600 | | OTA 0 | IT WAS ORIGINALLY CLEAR |
| 0359 | 04501 | 102501 | | LIA CPUT | CHECK TO SKIP MEMORY AND I/O TESTS |
| 0360 | 04502 | 001727 | | ALF,ALF | |
| 0361 | 04503 | 013542 | | AND B17 | |
| 0362 | 04504 | 053540 | | CPA B6 | GO STRAIGHT TO VCP? |
| 0363 | 04505 | 002001 | | RSS | |
| 0364 | 04506 | 026512 | | JMP MTST | NO DO IT ALL |
| 0365 | 04507 | 002400 | | CLA | |
| 0366 | 04510 | 102603 | | OTA 3 | CLEAR REGISTER |
| 0367 | 04511 | 027757 | | JMP DONE | GO TO VCP SECTION |

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0369*   START MEMORY ACCESS FOR FIRST TIME
0370*   CLEAR MEMORY IF IT WAS LOST DURING POWER DOWN
0371*   AND CHECK MEMORY BUT DON'T DESTROY ANY DATA IF NOT LOST
0372*
0373 04512 102501  MTST  LIA CPUST   GET CPU STATUS
0374 04513 001600          ELA       SAVE VCP TEST FLAG
0375 04514 002020          SSA       WAS MEMORY SAVED ANYWAY
0376 04515 002300          CCE       YES
0377 04516 106704          CLC 4     TURN OFF THE WORLD
0378 04517 063534          LDA B2    INDICATE IN MEMORY TEST
0379 04520 102601          OTA CPUST
0380*
0381*   ENABLE BREAK MODE DURING PRETEST
0382*
0383 04521 063532          LDA VCPD   ASSIGN BREAK ADDRESS TO I/O
0384 04522 103603          OTA 3,C    INCASE BREAK IS ENTERED
0385 04523 006400          CLB       NOW VERIFY THE OUTPUT
0386 04524 107503          LIB 3,C    GET IT BACK
0387 04525 006002          SZB       IF NOTHING THEN OK
0388 04526 050001          CPA B     DO THEY AGREE
0389 04527 026532          JMP *+3
0390 04530 063537          LDA B5    ERROR SO REPORT IT
0391 04531 027476          JMP IOER
0392 04532 062537          LDA POJPO  GET RETURN AFTER REENABLE
0393 04533 064000          LDB A
0394 04534 062540          LDA POCL2  GET REENABLE
0395 04535 102702          STC 2    DISABLE ROMS
0396 04536 024000          JMP 0    NOW EXECUTE REENABLE
0397*
0398 04537 026541  POJPO  JMP POC00
0399 04540 106702  POCL2  CLC 2
0400*
0401 04541 006400  POC00  CLB       CLEAR PARITY ADDRESS
0402 04542 107607          OTB 7,C  IT'S SAVED IN MP REG.
0403 04543 063534          LDA B2    SET STARTING ADDRESS
0404 04544 103101  MTST0  CLO       INDICATE FIRST TIME NO ERRORS
0405 04545 102705          STC 5    TURN ON PARITY DETECTION INTERRUPT
0406 04546 006440          CLB,SEZ  IF MEMORY WAS LOST SKIP LOADING DATA
0407 04547 164000          LDB A,I  GET CURRENT CONTENTS
0408 04550 007000          CMB       COMPLEMENT THE DATA
0409 04551 174000          STB A,I  PUT IT BACK IN THE LOCATION
0410 04552 154000          CPB A,I  DID IT STORE?
0411 04553 007001          CMB,RSS  YES - COMPLEMENT DATA BACK
0412 04554 026560          JMP MTSTE  NO - REPORT ERROR
0413 04555 174000          STB A,I  RESTORE ORIGINAL DATA
0414 04556 154000          CPB A,I  DID IT RESTORE?
0415 04557 026700          JMP MTST1  YES - MOVE TO NEXT ADDRESS

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0417*      MEMORY ERROR ROUTINE
0418*
0419 04560 106705 MTSTE CLC 5      TURN OFF PARITY INTERRUPTS
0420 04561 102200      SFC 0      CHECK IF MAPPED
0421 04562 102711      STC 11B     YES TURN THEM BACK ON
0422 04563 026564      JMP *+1
0423 04564 164000      LDB A,I     GET MEMORY DATA
0424 04565 106711      CLC 11B     TURN OFF MAPS
0425 04566 102301      SOS        IF PARITY ERROR THEN FAILURE
0426 04567 007002      CMB,SZB    CHECK IF END OF MEMORY
0427 04570 026576      JMP *+6     NOT SO ERROR
0428 04571 070001      STA B       SAVE ORIGINAL ADDRESS
0429 04572 013560      AND B1777   MASK UPPER PAGE BITS
0430 04573 002003      SZA,RSS    WAS IT ON PAGE BOUNDARY?
0431 04574 027002      JMP MTST3   YES - ASSUME END OF MEMORY
0432 04575 060001      LDA B       NO - RESTOR ORIGINAL ADDRESS
0433 04576 102200      SFC 0      CHECK IF IN EXTENDED MEMORY
0434 04577 026642      JMP EMERR   YES REPORT IT AS SUCH
0435 04600 070001      STA B       PUT ADDRESS IN B REG
0436 04601 063572      LDA ALTO   START WITH ALTERNATING PATTERN
0437 04602 101100      RRR 16     SWAP A & B
0438 04603 174000      STB A,I    STORE TEST PATTERN
0439 04604 164000      LDB A,I    GET IT BACK
0440 04605 101100      RRR 16     SWAP A & B
0441 04606 023572      XOR ALTO   ELIMINATE GOOD BITS
0442 04607 002002      SZA        WAS THERE ANY BAD BITS?
0443 04610 026617      JMP *+7     YES - DISPLAY IT
0444 04611 063573      LDA ALT1   USE OPPOSITE PATTERN
0445 04612 101100      RRR 16     SWAP A & B
0446 04613 174000      STB A,I    STORE TEST PATTERN
0447 04614 164000      LDB A,J    GET IT BACK
0448 04615 101100      RRR 16     SWAP A & B
0449 04616 023573      XOR ALT1   ELIMINATE GOOD DATA
0450 04617 103101      CLO        SET FOR UPPER LOWER ADDRESS
0451 04620 005200      RBL        SAVE UPPER/LOWER 16K BIT
0452 04621 006020      SSB
0453 04622 102101      STO        UPPER HALF
0454 04623 101100      RRR 16     SWAP A & B
0455 04624 002401      CLA,RSS    START WITH BIT 0
0456 04625 002004      INA        COUNT FOR BIT POSITION
0457 04626 053543      CPA B20    END OF BIT CHECK
0458 04627 026635      JMP *+6     YES - MUST BE PARITY
0459 04630 004075      CLE,SLB,ERB NO CHECK FOR BIT AND ROTATE REGISTER
0460 04631 026633      JMP *+2     BAD BIT SO DISPLAY IT
0461 04632 026625      JMP *-5     NO SO TRY NEXT BIT
0462 04633 006002      SZB        CHECK IF MULTI BIT ERROR
0463 04634 033543      IOR B20    YES
0464 04635 102201      SOC        CHECK FOR UPPER LOWER
0465 04636 033546      IOR BITS5  IT'S UPPER
0466 04637 001727      ALF,ALF    PUT DATA IN UPPER HALF
0467 04640 033534      IOR B2     INDICATE MEMORY ERROR
0468 04641 027500      JMP DSPLY   DISPLAY THE ERROR

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0470*      EXTENDED MEMORY ERROR DISPLAY
0471*
0472 04642 064137  EMERR LDB 137B      GET 16K BLOCK ADDRESS
0473 04643 060001      LDA B
0474 04644 001121      ARS,ARS      DIVIDE BY 16
0475 04645 001121      ARS,ARS
0476 04646 013545      AND B37      MASK OFF UPPER BITS
0477 04647 001727      ALF,ALF     PUT IT IN UPPER HALF
0478 04650 033540      IOR B6      ADD EXTENDED MEMORY SECTION
0479 04651 027500      JMP DSPLY   GO DISPLAY IT
0480*
0481*      PARITY INTERRUPT ROUTINE
0482*      A SOFT ERROR WILL NO CAUSE CPU TO STOP
0483*
0484 04652 106705  TPRTY CLC 5      TURN OFF PARITY DETECTION
0485 04653 002020      SSA          PARITY TEST?
0486 04654 027014      JMP MTST4   YES END OF MEMORY TEST
0487 04655 102201      SOC          WAS THERE A PREVIOUS ERROR
0488 04656 026560      JMP MTSTE   YES REPORT FAILURE
0489 04657 102101      STO          INDICATE PARITY ERROR
0490 04660 107507      LIB 7,C     WAS THERE A PREVIOUS ADDRESS
0491 04661 006002      SZB          ??
0492 04662 026671      JMP *+7     YES PREVIOUS ADDRESS SKIF UPDATE
0493 04663 102300      SFS 0      IS THIS EXTENDED
0494 04664 026670      JMP *+4     NO
0495 04665 064137      LDR 137B   YES GET BLOCK ADDRESS
0496 04666 107607      OTB 7,C   UPDATE ERROR
0497 04667 026671      JMP *+2
0498 04670 103607      OTA 7,C   NO SO SAVE THIS ONE
0499 04671 102200      SFC 0     CHECK IF MAPS WERE ON
0500 04672 102711      STC 11B   YES THEN RFSTOR THEM
0501 04673 026674      JMP *+1   AND TURN THEM ON
0502 04674 006400      CLB          CLEAR DATA
0503 04675 074004      STB 4     AND RESTART CONDITION
0504 04676 174000      STB A,I   WRITE GOOD PARITY
0505 04677 026545      JMP MTST0+1 TRY IT AGAIN

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|------|-------|--------|-------|-----------|---------------------------------------|
| 0507 | 04700 | 102204 | MIST1 | SFC 4 | IS POWER GOING DOWN? |
| 0508 | 04701 | 026715 | | JMP MTST2 | NO |
| 0509 | 04702 | 002400 | | CLA | CLEAR INCASE NO RESPONSE TO I/O |
| 0510 | 04703 | 103507 | | LIA 7,C | YES CHECK IF THERE |
| 0511 | 04704 | 002003 | | SZA,RSS | WAS A PARITY ERROR |
| 0512 | 04705 | 026710 | | JMP *+3 | NO |
| 0513 | 04706 | 102105 | | STF 5 | YES - CHANGE PARITY SENSE |
| 0514 | 04707 | 174000 | | STB A,I | WRITE AN ERROR |
| 0515 | 04710 | 103105 | | CLF 5 | PUT PARITY BACK |
| 0516 | 04711 | 102304 | IPF | SFS 4 | WAIT FOR POWER TO GO DOWN |
| 0517 | 04712 | 026711 | | JMP *-1 | |
| 0518 | 04713 | 107700 | | CLC 0,C | TURN OFF MACHINE |
| 0519 | 04714 | 024002 | | JMP 2 | DIDN'T GO ALL THE WAY SO RESTART |
| 0520 | 04715 | 034000 | MTST2 | ISZ A | MOVE TO NEXT LOCATION |
| 0521 | 04716 | 064000 | | LDR A | SAVE ADDRESS |
| 0522 | 04717 | 002021 | | SSA,RSS | END OF MEMORY TEST? |
| 0523 | 04720 | 026544 | | JMP MTST0 | NO |
| 0524 | 04721 | 102200 | | SFC 0 | CHECK IF MAPPED |
| 0525 | 04722 | 026766 | | JMP MTSTM | YES |
| 0526 | 04723 | 064137 | | LDB 137B | SAVE MAP REGISTER |
| 0527 | 04724 | 002400 | | CLA | SET MAP TO POINT TO SAME PAGE |
| 0528 | 04725 | 070137 | | STA 137B | |
| 0529 | 04726 | 063557 | | LDA B1776 | GET UPPER ADDRESS |
| 0530 | 04727 | 033565 | | IOR B76K | |
| 0531 | 04730 | 102711 | | STC 11B | ENABLE MAPS |
| 0532 | 04731 | 026732 | | JMP *+1 | TURN THEM ON |
| 0533 | 04732 | 174000 | | STB A,I | SAVE MAP |
| 0534 | 04733 | 002004 | | INA | |
| 0535 | 04734 | 106713 | | CLC 13B | TEMP DISABLE MAPS |
| 0536 | 04735 | 067777 | | LDB PO.CT | |
| 0537 | 04736 | 007000 | | CMB | |
| 0538 | 04737 | 102713 | | STC 13B | REENABLE |
| 0539 | 04740 | 174000 | | STB A,I | |
| 0540 | 04741 | 106713 | | CLC 13B | |
| 0541 | 04742 | 063557 | | LDA B1776 | |
| 0542 | 04743 | 033565 | | IOR B76K | |
| 0543 | 04744 | 057777 | | CPB PO.CT | DID IT GO INTO BASE PAGE? |
| 0544 | 04745 | 013560 | | AND B1777 | YES THEN USE BASE PAGE THERE ARE MAPS |
| 0545 | 04746 | 164000 | | LDB A,I | RESTOR MAPS |
| 0546 | 04747 | 074137 | | STB 137B | |
| 0547 | 04750 | 006400 | | CLB | |
| 0548 | 04751 | 053557 | | CPA B1776 | WAS THERE MAPS |
| 0549 | 04752 | 026754 | | JMP *+2 | |
| 0550 | 04753 | 027002 | | JMP MTST3 | NO |
| 0551 | 04754 | 102100 | | STF 0 | YES - THEN INDICATE MAPS TEST |
| 0552 | 04755 | 063540 | | LDA B6 | INDICATE EXTENDED MEMORY TEST |
| 0553 | 04756 | 102601 | | OTA CPUTS | PUT IT ON LEDS |
| 0554 | 04757 | 064137 | | LDB 137B | SAVE MAP |
| 0555 | 04760 | 077776 | | STB PO.T3 | |
| 0556 | 04761 | 063546 | | LDA B40 | START WITH LOWEST MAPPED PAGE |
| 0557 | 04762 | 070137 | | STA 137B | |
| 0558 | 04763 | 063565 | | LDA B76K | AND ADDRESS FOR CORRECT MAPPING |
| 0559 | 04764 | 102713 | | STC 13B | ENABLE MAPS |
| 0560 | 04765 | 026544 | | JMP MTST0 | |

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|-------|-------|--------|-------|-----|-------|---------------------------|
| 0562 | 04766 | 106711 | MTSTM | CLC | 11B | |
| 0563 | 04767 | 106713 | | CLC | 13B | DISABLE MAPPING |
| 0564 | 04770 | 064137 | | LDB | 137B | CHECK IF END OF MEMORY |
| 0565 | 04771 | 034137 | | ISZ | 137B | MOVE TO NEXT BLOCK |
| 0566 | 04772 | 060001 | | LDA | B | |
| 0567 | 04773 | 006400 | | CLB | | |
| 0568 | 04774 | 053553 | | CPA | B377 | IS IT? |
| 0569 | 04775 | 027002 | | JMP | MTST3 | YES |
| 0570 | 04776 | 063565 | | LDA | B76K | NO - DO NEXT ONE |
| 0571 | 04777 | 102711 | | STC | 11B | RE-ENABLE MAPPING |
| 0572 | 05000 | 102713 | | STC | 13B | |
| 0573 | 05001 | 026544 | | JMP | MTST0 | |
| 0574* | | | | | | |
| 0575 | 05002 | 060001 | MTST3 | LDA | B | NOW TEST PARITY DETECTION |
| 0576 | 05003 | 033566 | | IOR | B100K | |
| 0577 | 05004 | 064002 | | LDB | 2 | GET DATA |
| 0578 | 05005 | 102105 | | STF | 5 | CHANGE PARITY SENSE |
| 0579 | 05006 | 074002 | | STB | 2 | ESTABLISH BAD PARITY |
| 0580 | 05007 | 103105 | | CLF | 5 | REVERSE SENSE |
| 0581 | 05010 | 102705 | | STC | 5 | FNABLE PARITY |
| 0582 | 05011 | 064002 | | LDB | 2 | READ BAD PARITY |
| 0583 | 05012 | 063534 | | LDA | B2 | INTERRUPT SHOULD OCCUR |
| 0584 | 05013 | 026560 | | JMP | MTSTE | IT DIDN'T SO ERROR |

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|------|-------|--------|-------|-------------|-----------------------------------|
| 0586 | 05014 | 074002 | MTST4 | STB 2 | RESTORE GOOD PARITY TO LOCATION 2 |
| 0587 | 05015 | 102200 | | SFC 0 | IF MAPPED |
| 0588 | 05016 | 063566 | | LDA B100K | SET P=77777 |
| 0589 | 05017 | 005600 | | ELB | SAVE MEM LOST FLAG |
| 0590 | 05020 | 043567 | | ADA M1 | BACK ADDRESS UP ONE |
| 0591 | 05021 | 005500 | | ERB | |
| 0592 | 05022 | 001665 | | ELA,CLE,ERA | CLEAR BIT 15 |
| 0593 | 05023 | 107507 | | LIB 7,C | GET PARITY ADDRESS |
| 0594 | 05024 | 006002 | | SZB | SET MEMLOST IF PARITY ERROR |
| 0595 | 05025 | 002101 | | CLF,RSS | AND DISPLAY THE PARITY ADDRESS |
| 0596 | 05026 | 064000 | | LDB A | OTHERWISE DISPLAY MEMORY SIZE |
| 0597 | 05027 | 106603 | | OTB 3 | |
| 0598 | 05030 | 006400 | | CLB | CLEAT MP REG |
| 0599 | 05031 | 107607 | | OTB 7,C | |
| 0600 | 05032 | 102300 | | SFS 0 | CHECK FOR MAPS |
| 0601 | 05033 | 027042 | | JMP MTST5 | NO MAPS |
| 0602 | 05034 | 064137 | | LDB 137B | INDICATE HIGHEST MAP |
| 0603 | 05035 | 060001 | | LDA B | |
| 0604 | 05036 | 103607 | | OTA 7,C | |
| 0605 | 05037 | 067776 | | LDB P0.T3 | RESTOR MAP REGISTER |
| 0606 | 05040 | 074137 | | STB 137B | |
| 0607 | 05041 | 002400 | | CLA | |
| 0608 | 05042 | 103100 | MTST5 | CLF 0 | RESET THINGS |
| 0609 | 05043 | 102704 | | STC 4 | REFENABLE ALSO |
| 0610 | 05044 | 013565 | | AND B76K | SAVE PAGE |
| 0611 | 05045 | 070001 | | STA B | |
| 0612 | 05046 | 033532 | | IOR VCPD | SET VCP ADDRESS |
| 0613 | 05047 | 103603 | | OTA 3,C | FOR BREAK |
| 0614 | 05050 | 060001 | | LDA B | |
| 0615 | 05051 | 033053 | | IOR *+2 | PUT SELF ON PAGE |
| 0616 | 05052 | 124000 | | JMP A,I | |
| 0617 | 05053 | 001054 | | DEF *+1-P0 | |
| 0618 | 05054 | 063531 | | LDA IOLP | SET POINTER FOR I/O TABLE |
| 0619 | 05055 | 030001 | | IOR B | ADD PAGE |
| 0620 | 05056 | 073773 | | STA P0.T0 | |
| 0621 | 05057 | 002004 | | INA | |
| 0622 | 05060 | 073774 | | STA P0.T1 | SAVE PAGE ADDRESS |
| 0623 | 05061 | 103507 | | LIA 7,C | GET MEMORY SIZE |
| 0624 | 05062 | 107607 | | OTB 7,C | SAVE PAGE ADDRESS |
| 0625 | 05063 | 003006 | | CMA,INA,SZA | DECREMENT BLOCK |
| 0626 | 05064 | 003000 | | CMA | |
| 0627 | 05065 | 001727 | | ALF,ALF | PUT IN UPPER PORTION |
| 0628 | 05066 | 001323 | | RAR,RAR | |
| 0629 | 05067 | 073772 | | STA P0.A | OF A REGISTER |
| 0630 | 05070 | 104200 | | DLD REV | SET REVISION |
| 0631 | 05072 | 073771 | | STA P0.B | IN B REGISTER |

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0633*      START OF I-O INTERFACE CHIP TESTS
0634*
0635*      USE DIAG. MODE 1 TO BUILD A SELECT CODE TABLE
0636*
0637 05073 063535      LDA B3      INDICATE IN IO INTERFACES
0638 05074 102601      OTA CPUTS
0639 05075 102102      STF 2      INSURE GLOBAL REGISTER IS OFF
0640 05076 002404      CLA,INA      SET TEST MODE 1 (PROIRIETY RESPONSE)
0641 05077 102602      OTA 2      GIVE MODE TO CHIPS
0642 05100 002400      IOL0 CLA      INCASE OF NO RESPONSE
0643 05101 037773      ISZ P0.T0
0644 05102 067773      LDB P0.T0      GET TABLE POINTER
0645 05103 170001      STA B,I      SET END OF TABLE
0646 05104 102502      LIA 2      GET SELECT CODE
0647 05105 002003      SZA,RSS      ANY SELECT CODE
0648 05106 027134      JMP IONO      NO END-OF-IO CHIPS
0649 05107 013547      AND SCM      YES - USE SELECT CODE ONLY
0650 05110 170001      STA B,J      PUT IT IN TABLE
0651 05111 001665      FLA,CLE,FRA
0652 05112 043571      ADA M20      SUBTRACT 20B
0653 05113 002020      SSA      IS IT A VALID SELECT CODE?
0654 05114 027132      JMP IOF4      NO - INDICATE ERROR 4 ON LEDS
0655 05115 067774      LDB P0.T1      CHECK FOR DUPLICATE SELECT CODES
0656 05116 060001      LDA B
0657 05117 064000      IOL1 LDB A      CHANGE HANDS
0658 05120 057773      CPB P0.T0      END OF TABLE?
0659 05121 027100      JMP IOL0      YES MOVE TO NEXT IO CHIP
0660 05122 164000      LDB A,I      GET SC FROM TABLE
0661 05123 005665      ELB,CLE,FRR
0662 05124 157773      CPR P0.T0,I      IS IT THE SAME AS THE NEW SC?
0663 05125 027130      JMP *+3      YES - DUPLICATE SELECT CODES ERROR 3
0664 05126 002004      INA
0665 05127 027117      JMP IOL1      NO DO NEXT ENTRY
0666*
0667 05130 063535      LDA B3
0668 05131 027476      JMP IOFR
0669 05132 063536      IOE4 LDA B4
0670 05133 027476      JMP IOER

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0672*      CHECK IF ANY SELECT CODES DID NOT RESPOND TO MODE 1
0673*      IF THEY DIDN'T PRIORITY CHAIN IS BROKEN
0674*
0675 05134 102102 TON0 STF 2      INSURE GLOBAL REGISTER IS OFF
0676 05135 002400      CLA      TURN OFF DIAGNOSE MODE
0677 05136 102602      OTA 2
0678 05137 063542      LDA B17      START WITH FIRST SELECT CODE -1
0679 05140 073777      STA P0.CT
0680 05141 037777 TOL2 ISZ P0.CT      MOVE TO NEXT SC
0681 05142 067774      LDR P0.T1      CHECK IF IN TABLE
0682 05143 060001      LDA B      CHANGE HANDS
0683 05144 164000 TOL3 LDB A,I      GET SC FROM TABLE
0684 05145 006003      SZB,RSS      END OF TABLE?
0685 05146 027154      JMP ION1      YES
0686 05147 005665      FLB,CLE,FRB
0687 05150 057777      CPR P0.CT      NO IS SC IN TABLE?
0688 05151 027141      JMP IOL2      YES
0689 05152 002004      INA
0690 05153 027144      JMP IOL3      NO MOVE TO NEXT ENTRY
0691 05154 067777 TON1 LDB P0.CT      GET SC
0692 05155 060001      LDA B      CHANGE HANDS
0693 05156 053551      CPA R100      END OF SC'S
0694 05157 027167      JMP ION2      YES
0695 05160 102602      OTA 2      NO TRY IT
0696 05161 002400      CLA
0697 05162 102502      LIA 2
0698 05163 002003      SZA,RSS      DID IT COME BACK?
0699 05164 027141      JMP IOL2      NO MOVE TO NEXT ONE
0700 05165 063534      LDA B2      YES - INDICATE ERROR 2
0701 05166 027476      JMP IOFR

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0703* CHECK INDIVIDUAL I/O CHIPS

0704*

| | | | | | |
|------|-------|--------|------|-------------|---|
| 0705 | 05167 | 167774 | ION2 | LDB PO.T1,J | START IO CHECK WITH FIRST ENTRY |
| 0706 | 05170 | 002400 | | CLA | |
| 0707 | 05171 | 006003 | | SZB,RSS | WERE THERE ANY ENTRIES? |
| 0708 | 05172 | 027476 | | JMP IOER | NO IO CHIPS PRESENT ERROR 0 |
| 0709 | 05173 | 067774 | | LDB PO.T1 | GET SC TABLE POINTER |
| 0710 | 05174 | 077773 | | STB PO.T0 | SET POINTER |
| 0711 | 05175 | 167773 | IOL4 | LDB PO.T0,I | GET SELECT CODE |
| 0712 | 05176 | 006103 | | CLE,SZB,RSS | END OF TABLE? |
| 0713 | 05177 | 027354 | | JMP ION3 | YES CKECK FOR BREAK ENABLE |
| 0714 | 05200 | 005623 | | ELB,RBR | SAVE SELF TEST FLAG |
| 0715 | 05201 | 107602 | | OTB 2,C | SET THE GLOBAL REGISTER AND ENABLE IT |
| 0716 | 05202 | 002400 | | CLA | CLEAR INCASE NO RESPONSE |
| 0717 | 05203 | 102502 | | LIA 2 | GET GLOBAL REG. |
| 0718 | 05204 | 050001 | | CPA B | DID IT COME BACK? |
| 0719 | 05205 | 002001 | | RSS | |
| 0720 | 05206 | 027474 | | JMP IOESC | NO DISPLAY SELECT CODE WITH ERROR |
| 0721 | 05207 | 002041 | | SEZ,RSS | DOES THIS INTERFACE HAVE SELFTEST? |
| 0722 | 05210 | 027225 | | JMP ION2A | NO - THEN DONT WAIT |
| 0723 | 05211 | 063571 | | LDA M20 | YES THEN WAIT 10 SECONDS FOR SELF TEST |
| 0724 | 05212 | 102230 | | SFC DR | |
| 0725 | 05213 | 027221 | | JMP *+6 | |
| 0726 | 05214 | 034001 | | ISZ B | |
| 0727 | 05215 | 027212 | | JMP *-3 | |
| 0728 | 05216 | 034000 | | ISZ A | |
| 0729 | 05217 | 027212 | | JMP *-5 | |
| 0730 | 05220 | 027474 | | JMP IOESC | TIME OUT SO FRROR |
| 0731 | 05221 | 103530 | | LIA DR,C | GET SELF TEST STATUS AND CLEAR THE FLAG |
| 0732 | 05222 | 002020 | | SSA | WAS IT GOOD? |
| 0733 | 05223 | 000010 | | SLA | |
| 0734 | 05224 | 027474 | | JMP IOESC | NU SO ERROR |

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|-------|-------|--------|----------------|--|
| 0736 | 05225 | 063572 | TON2A LDA ALTO | USE ALTERNATING PATTERN |
| 0737 | 05226 | 102623 | OTA 23B | TO CHECK I/O CHIP BUS UPPER |
| 0738 | 05227 | 001300 | RAR | AND OPPOSITE PATTERN |
| 0739 | 05230 | 102624 | OTA 24B | FOR I/O CHIP BUS LOWER |
| 0740 | 05231 | 007400 | CCB | CLEAR INCASE NO RESPONSE |
| 0741 | 05232 | 002400 | CLA | |
| 0742 | 05233 | 102625 | OTA 25B | SET FILE # TO 0 INCASE OF AUTO EXECUTION |
| 0743 | 05234 | 102523 | LIA 23B | READ PATTERNS BACK |
| 0744 | 05235 | 106524 | LIB 24B | |
| 0745 | 05236 | 005200 | RBL | |
| 0746 | 05237 | 050001 | CPA B | DO PATTERNS AGREE |
| 0747 | 05240 | 006401 | CLB,RSS | YES |
| 0748 | 05241 | 027474 | JMP IOESC | NO - I/O CHIP BUS ERROR |
| 0749 | 05242 | 102624 | OTA 24B | REVERSE PATTERN AND |
| 0750 | 05243 | 001300 | RAR | CHECK BUS AGAIN |
| 0751 | 05244 | 102623 | OTA 23B | |
| 0752 | 05245 | 102524 | LIA 24B | |
| 0753 | 05246 | 106523 | LIB 23B | |
| 0754 | 05247 | 005200 | RBL | |
| 0755 | 05250 | 050001 | CPA B | DO PATTERNS AGREE? |
| 0756 | 05251 | 102230 | SFC 30B | YES CHECK FLAG |
| 0757 | 05252 | 027474 | JMP IOESC | BUS OR FLAG ERROR |
| 0758 | 05253 | 102130 | STF 30B | SET THE I O FLAG |
| 0759 | 05254 | 102230 | SFC 30B | DID IT GET SET? |
| 0760 | 05255 | 102330 | SFS 30B | |
| 0761 | 05256 | 027474 | JMP IOESC | NO I/O FLAG ERROR |
| 0762 | 05257 | 103130 | CLF 30B | NOW CLEAR IT |
| 0763 | 05260 | 102330 | SFS 30B | DID IT GET CLEARED |
| 0764 | 05261 | 102230 | SFC 30B | |
| 0765 | 05262 | 027474 | JMP IOESC | NO I/O FLAG ERROR |
| 0766* | | | | |
| 0767 | 05263 | 106723 | CLC 23B | RESET DMA MACHINE |

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0769*      CHECK DMA AND INTERRUPTS
0770*
0771 05264 103507      LIA 7,C      GET PAGE NO.
0772 05265 033352      IOR DMACF     INCLUDE DMA ADDRESS
0773 05266 102620      OTA 20R      PASS IT TO SELF CONFIGURATION REG
0774 05267 073761      STA DMA+1    AND PLACE IN TRIPLET
0775 05270 063351      LDA DMACW    GET DMA CONTROL WORD
0776 05271 073760      STA DMA
0777 05272 063353      LDA DMACW+2      AND COUNT
0778 05273 073762      STA DMA+2
0779 05274 063541      LDA B7      DISABLE SRQ INTERRUPTS
0780 05275 102602      OTA 2
0781 05276 103720      STC 20B,C   DO SELFCONFIGURATION
0782 05277 102324      SFS 24R     DID IT COMPLETE
0783 05300 027474      JMP IOFSC    NO SO ERROR
0784 05301 102521      LIA 21R     CHECK CONTROL WORD
0785 05302 053351      CPA DMACW
0786 05303 002001      RSS
0787 05304 027474      JMP IOESC    BAD SO ERROR
0788 05305 102523      LIA 23B     CHECK COUNT
0789 05306 053353      CPA DMACW+2
0790 05307 002001      RSS
0791 05310 027474      JMP IOESC    NO GOOD SO ERROR
0792 05311 063535      LDA B3      NOW USE DIAG. MODE 3
0793 05312 102602      OTA 2
0794 05313 102100      STF 0       TURN ON INTERRUPTS
0795 05314 002006      INA,SZA    WAIT FOR IT
0796 05315 027314      JMP *-1
0797 05316 027474      JMP IOESC    NO GOOD
0798*
0799 05317 102202      IOINT SFC 2  IS THIS A LEGAL INTERRUPT
0800 05320 027470      JMP ILINT   NO ILLEGAL
0801 05321 102504      LIA 4       CHECK CENTRAL INTERRUPT
0802 05322 106502      LIB 2       AGAINST GLOBAL REGISTER
0803 05323 050001      CPA B       WEILL?
0804 05324 002001      RSS
0805 05325 027474      JMP IOESC   CARD ERROR
0806 05326 103507      LIA 7,C     GET BLOCK ADDRESS
0807 05327 033331      IOR **2     PUT SELF BACK ON PAGE
0808 05330 124000      JMP 0,I
0809 05331 001332      DEF **1-P0

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0811 05332 103507      LIA 7,C      GET ADDRESS AGAIN
0812 05333 033352      TOR DMACF
0813 05334 043537      ADA B5      MOVE TO CONFIGURATION ADDRESS
0814 05335 064000      LDB A
0815 05336 057762      CPB DMA+2   DID IT STORE
0816 05337 102224      SFC 24B    AND DID IT TURN OFF
0817 05340 027474      JMP IOESC   NO SO ERROR
0818 05341 102523      LIA 23B    CHECK COUNT IS ZERO
0819 05342 002002      SZA
0820 05343 027474      JMP IOFSC
0821 05344 107720      CLC 20B,C  INSURE DMA IS OFF
0822 05345 107721      CLC 21B,C
0823 05346 037773      ISZ P0.T0  MOVE TO NEXT ENTRY
0824 05347 037772      ISZ P0.A   COUNT THIS I/O CARD
0825 05350 027175      JMP IOL4   AND DO IT
0826*
0827 05760              DMA EQU 1760B+P0
0828 05351 000200      DMACW OCT 200
0829 05352 001760      DMACF DEF DMA-P0
0830 05353 177775      DEC -3

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0832* CHECK THAT ONLY ONE INTF. HAS A BREAK ENABLE

0833* NONE IS OK

0834*

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0835 05354 063534      ION3 LDA B2      USE DIAGNOSE MODE 2
0836 05355 067774      LDR P0.T1   SET POINTER FOR SELECT CODE
0837 05356 077773      STB P0.T0
0838 05357 006400      CLB
0839 05360 077775      STB P0.T2   CLEAR SC FLAG
0840 05361 102102      STF 2       TURN OFF GLOBAL REGISTER
0841 05362 102602      OTA 2
0842 05363 002400      IOL5 CLA        CLEAR IN CASE OF NO RESPONSE
0843 05364 102502      LIA 2       GET PARAMETERS
0844 05365 002002      SZA        DONE WITH I O
0845 05366 027371      JMP ION4    NO
0846 05367 102602      OTA 2       TURN OFF DIAG.MODE 2
0847 05370 027402      JMP ION5    YES NOW CHECK IF VCP OR LOADER
0848 05371 001710      ION4 ALF,SLA CHECK BREAK ENABLE BIT
0849 05372 027375      JMP **3
0850 05373 037773      ISZ P0.T0  MOVE TO NEXT ONE
0851 05374 027363      JMP IOL5
0852 05375 002744      CLA,SEZ,CCE,INA WAS THERE A PREVIOUS ONE
0853 05376 027476      JMP IOER    YES SO ERROR 1
0854 05377 067773      LDB P0.T0  NO OK SAVE THIS ONE
0855 05400 077775      STB P0.T2
0856 05401 027363      JMP IOL5    NOW TRY NEXT ONE

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| | | | | | |
|-------|-------|--------|------|-------------|---------------------------------|
| 0858 | 05402 | 067775 | ION5 | LDB PO.T2 | CHECK IF THERE IS ONE |
| 0859 | 05403 | 077773 | | STR PO.T0 | |
| 0860 | 05404 | 006003 | | SZB,RSS | WAS THERE ONE? |
| 0861 | 05405 | 027455 | | JMP ION6 | NO THEN SKIP ALL TEST |
| 0862 | 05406 | 167773 | | LDB PO.T0,I | CHECK VCP CARD |
| 0863 | 05407 | 006020 | | SSB | IF IT HAS A SELF TEST FORGET IT |
| 0864 | 05410 | 027455 | | JMP ION6 | IT DOES |
| 0865 | 05411 | 107602 | | OTB 2,C | NO OUTPUT IT AND ENDABLE |
| 0866 | 05412 | 002404 | | CLA,INA | NOW USE DIAGNOSE MODE TO GET ID |
| 0867 | 05413 | 102602 | | OTA 2 | |
| 0868 | 05414 | 102502 | | LIA 2 | |
| 0869 | 05415 | 013550 | | AND IDM | USE ONLY ID |
| 0870 | 05416 | 002002 | | SZA | IS IT A TIC |
| 0871 | 05417 | 027455 | | JMP ION6 | NO SKIP TEST |
| 0872 | 05420 | 102501 | | LIA CPUT | SAVE %T FLAG |
| 0873 | 05421 | 107700 | | CLC 0,C | RESET DIAGNOSE MODE 7 |
| 0874 | 05422 | 107602 | | OTB 2,C | REESTABLISH GLOBAL REGISTER |
| 0875 | 05423 | 006404 | | CLB,INB | RESTORE %T FLAG |
| 0876 | 05424 | 006004 | | INB | |
| 0877 | 05425 | 002021 | | SSA,RSS | |
| 0878 | 05426 | 006400 | | CLB | |
| 0879 | 05427 | 106600 | | OTB 0 | |
| 0880 | 05430 | 002404 | | CLA,INA | ESTABLISH DIAG ON CARD |
| 0881 | 05431 | 102632 | | OTA STS | |
| 0882 | 05432 | 063572 | | LDA ALTO | |
| 0883 | 05433 | 102630 | | OTA DR | USE ALTO |
| 0884 | 05434 | 063561 | | LDA B3004 | TELL IT TO TRANSMITT |
| 0885 | 05435 | 102631 | | OTA CTL | |
| 0886 | 05436 | 103730 | | STC DR,C | START TRANSMISSION |
| 0887 | 05437 | 006400 | | CLB | |
| 0888 | 05440 | 002400 | | CLA | SET FOR TIMEOUT |
| 0889 | 05441 | 102230 | | SFC DR | CHECK FLAG |
| 0890 | 05442 | 027447 | | JMP *+5 | NOW CHECK DATA |
| 0891 | 05443 | 002006 | | INA,SZA | TIMED OUT? |
| 0892 | 05444 | 027441 | | JMP *-3 | NO |
| 0893 | 05445 | 102632 | | OTA STS | CLEAR DIAGNOSE MODE ON CARD |
| 0894 | 05446 | 027474 | | JMP IOESC | AND REPORT ERROR |
| 0895 | 05447 | 106632 | | OTB STS | CLEAR DIAGNOSE MODE |
| 0896 | 05450 | 103530 | | LIA DR,C | GET DATA |
| 0897 | 05451 | 023572 | | XOR ALTO | NOW CHECK DATA |
| 0898 | 05452 | 013553 | | AND B377 | ONLY LOWER BYTE |
| 0899 | 05453 | 002002 | | SZA | |
| 0900 | 05454 | 027474 | | JMP IOESC | NO GOOD |
| 0901* | | | | | |
| 0902 | 05455 | 002400 | ION6 | CLA | CLEAR DIAGNOSE MODE |
| 0903 | 05456 | 102602 | | OTA 2 | |
| 0904 | 05457 | 106501 | | LIB CPUT | CHECK IF VCP TEST |
| 0905 | 05460 | 006021 | | SSB,RSS | |
| 0906 | 05461 | 027757 | | JMP DONE | NO NORMAL EXIT |
| 0907 | 05462 | 107700 | | CLC 0,C | RESET THE WORLD |
| 0908 | 05463 | 102600 | | OTA 0 | YES CLEAR TEST FLAG |
| 0909 | 05464 | 063554 | | LDA B207 | AND RETURN TO VCP |
| 0910 | 05465 | 027761 | | JMP DONE+2 | |

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0912*      ERROR REPORTING TO PROCESSOR LEDES
0913*
0914  05466 002404  PROER CLA,INA      INDICATE PROCESSOR ERROR
0915  05467 027500          JMP DSPLY
0916*
0917  05470 102504  ILINT LIA 4B      GET CENTRAL INTERRUPT REGISTER
0918  05471 001727          ALF,ALF    PUT IT IN DATA
0919  05472 002004          INA        INDICATE ILLEGAL INTERRUPT
0920  05473 027500          JMP DSPLY
0921*
0922  05474 167773  IOESC LDB P0.TO,I  GET SELECT CODE FOR DISPLAY
0923  05475 060001          LDA B      CHANGE HANDS
0924  05476 001727  IOER  ALF,ALF    PUT DATA IN UPPER HALF
0925  05477 033535          IOR B3   INDICATE IO TEST ERROR
0926*
0927*      DISPLAY LOWER BYTE (SECTION)
0928*      THEN UPPER BYTE (DATA )
0929*      THEN BACK TO LOWER BYTE
0930*
0931  05500 070001  DSPLY STA B      SAVE DATA AND SECTION
0932  05501 002300          CCE        SET TO DO SECOND PART
0933  05502 013552          AND B177
0934  05503 102601          OTA CPUST
0935  05504 034000          ISZ A
0936  05505 027504          JMP *-1
0937  05506 034000          ISZ A
0938  05507 027506          JMP *-1
0939  05510 034000          ISZ A
0940  05511 027510          JMP *-1
0941  05512 034000          ISZ A
0942  05513 027512          JMP *-1
0943  05514 002041          SEZ,RSS
0944  05515 027522          JMP PRTLP
0945  05516 060001          LDA B
0946  05517 001767          ALF,CLE,ALF
0947  05520 033551          IOR BIT6
0948  05521 027502          JMP DSPLY+2  UPPER HALF DATA
0949  05522 102501  PRTLP LIA CPUST  CHECK IF LOOP
0950  05523 001727          ALF,ALF
0951  05524 013541          AND B7
0952  05525 002003          SZA,RSS    ??
0953  05526 026713          JMP TPF+2  YES LOOP ON ERROR
0954  05527 060001          LDA B
0955  05530 027501          JMP DSPLY+1

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0957* CONSTANTS

0958*

| | | | | | | |
|-------|-------|--------|-------|-----|----------------|--------------------------------|
| 0959 | 05531 | 001677 | IOLP | DEF | P0.CT-77B-P0-1 | |
| 0960 | 05532 | 001763 | VCPD | DEF | POVCP-P0 | START OF RFP ONLY ON THIS PAGE |
| 0961 | 05533 | 000001 | B1 | OCT | 1 | |
| 0962 | 05534 | 000002 | B2 | OCT | 2 | |
| 0963 | 05535 | 000003 | B3 | OCT | 3 | |
| 0964 | 05536 | 000004 | B4 | OCT | 4 | |
| 0965 | 05537 | 000005 | B5 | OCT | 5 | |
| 0966 | 05540 | 000006 | B6 | OCT | 6 | |
| 0967 | 05541 | 000007 | B7 | OCT | 7 | |
| 0968 | 05542 | 000017 | B17 | OCT | 17 | |
| 0969 | 05543 | 000020 | B20 | OCT | 20 | |
| 0970 | 05544 | 000024 | B24 | OCT | 24 | |
| 0971 | 05545 | 000037 | B37 | OCT | 37 | |
| 0972 | 05546 | 000040 | B40 | OCT | 40 | |
| 0973 | 05547 | 100077 | SCM | OCT | 100077 | |
| 0974 | 05550 | 077000 | IDM | OCT | 077000 | ID ONLY NO SC OR REV. |
| 0975 | 05551 | 000100 | B100 | OCT | 100 | |
| 0976 | 05552 | 000177 | B177 | OCT | 177 | |
| 0977 | 05553 | 000377 | B377 | OCT | 377 | |
| 0978 | 05554 | 000207 | B207 | OCT | 207 | |
| 0979 | 05555 | 000604 | B604 | OCT | 604 | |
| 0980 | 05556 | 001000 | B1000 | OCT | 1000 | |
| 0981 | 05557 | 001776 | B1776 | OCT | 1776 | |
| 0982 | 05560 | 001777 | B1777 | OCT | 1777 | |
| 0983 | 05561 | 003004 | B3004 | OCT | 3004 | |
| 0984 | 05562 | 006412 | B6412 | OCT | 6412 | |
| 0985 | 05563 | 007777 | B7777 | OCT | 7777 | |
| 0986 | 05564 | 036000 | B16K | OCT | 36000 | |
| 0987 | 05565 | 076000 | B76K | OCT | 76000 | |
| 0988 | 05566 | 100000 | B100K | OCT | 100000 | |
| 0989 | 05567 | 177777 | M1 | OCT | -1 | |
| 0990 | 05570 | 177776 | M2 | OCT | -2 | |
| 0991 | 05571 | 177760 | M20 | OCT | -20 | |
| 0992 | 05546 | | BIT5 | EQU | B40 | |
| 0993 | 05551 | | BIT6 | EQU | B100 | |
| 0994 | 05572 | 052525 | ALT0 | OCT | 052525 | |
| 0995 | 05573 | 125252 | ALT1 | OCT | 125252 | |
| 0996 | 05574 | 104447 | SRGP1 | OCT | 104447 | 1000100100100111 |
| 0997 | 05575 | 114040 | SRGP2 | OCT | 114040 | 1001100000100000 |
| 0998 | 05576 | 000100 | SRGP3 | OCT | 000100 | 0000000001000000 |
| 0999 | 05577 | 076310 | AEAUS | OCT | 076310 | |
| 1000 | 05600 | 130272 | BEAUS | OCT | 130272 | |
| 1001 | 05601 | 107714 | ASR.0 | OCT | 107714 | |
| 1002 | 05602 | 041300 | ASR.1 | OCT | 041300 | |
| 1003 | 05603 | 143746 | MU2 | OCT | 143746 | |
| 1004 | 05604 | 123746 | DV4 | OCT | 123746 | |
| 1005 | 05605 | 126760 | RESUA | OCT | 126760 | |
| 1006 | 05606 | 006606 | RESUB | OCT | 006606 | |
| 1007* | | | | | | |
| 1008 | 05607 | | FOP0 | EQU | * | END OF PAGE 0 |
| 1009 | 05757 | | | ORG | 5757B | |
| 1010 | 00150 | | RAPO | EQU | *-FOP0 | |

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1012*      CROSS OVER TO OTHER PAGE
1013*
1014  05757 063555  DONE  LDA B604      GET SWITCH FOR LOADER PAGE 3
1015  05760 006400      CLB
1016  05761 102601      OTA CPUST     MAKE SWITCH
1017  05762 024100      JMP 100B      LOOP ON PRETEST IF ERROR
1018*
1019*      BREAK ENTRY POINT (SAME ON ALL PAGES)
1020*
1021  05763 103105  POVCP CLF 5      INSURE PARITY SENSE
1022  05764 106713      CLC 13B      DISABLE MAPPING
1023  05765 103300      OCT 103300    SFS 0,C CHECK INTERRUPTS
1024  05766 027772      JMP *+4      THERE OFF
1025  05767 073772      STA PO.A    SAVE THE A REG.
1026  05770 003400      CCA        INDICATE INTS ON
1027  05771 027774      JMP *+3
1028  05772 073772      STA PO.A
1029  05773 002400      CLA
1030  05774 073764      STA PO.I
1031  05775 063554      LDA B207    GET SWITCH TO VCP PAGE
1032  05776 102601      OTA CPUST     MAKE SWITCH
1033  05777 027763      JMP POVCP    LOOP IF ERROR
1034*
1035*      COMMON STORAGE LOCATIONS
1036*
1037  05777      PO.CT EQU 1777B+P0
1038  05776      PO.T3 EQU 1776B+P0
1039  05775      PO.T2 EQU 1775B+P0
1040  05774      PO.T1 EQU 1774B+P0
1041  05773      PO.T0 EQU 1773B+P0
1042  05772      PO.A  EQU 1772B+P0
1043  05771      PO.B  EQU 1771B+P0
1044  05770      PO.E  EQU 1770B+P0
1045  05767      PO.O  EQU 1767B+P0
1046  05766      PO.GF EQU 1766B+P0
1047  05765      PO.M  EQU 1765B+P0
1048  05764      PO.I  EQU 1764B+P0
1049  05763      PO.EM EQU 1763B+P0
1050  05762      PO.DF EQU 1762B+P0
1051  05761      PO.UN EQU 1761B+P0
1052  05760      PO.FL EQU 1760B+P0
1053  05757      PO.SB EQU 1757B+P0
1054  05756      PO.SC EQU 1756B+P0

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|-------|-------|--------|-----------|---------------------------------|
| 1056 | 06000 | | ORG 6000B | |
| 1057 | 06000 | P1 | EQU * | PAGE 1 REFERENCE |
| 1058* | | | | |
| 1059 | 06000 | 000000 | NOP | SPACE HOLDERS |
| 1060 | 06001 | 000000 | NOP | B REG. |
| 1061 | 06002 | 124000 | JMP A,I | RETURN FROM DIAGNOSE MODE READS |
| 1062 | 06003 | 000000 | NOP | |
| 1063 | 06004 | 000000 | NOP | POWER FAIL INT |
| 1064 | 06005 | 000000 | NOP | PARITY ERROR |
| 1065 | 06006 | 000000 | NOP | TBG |
| 1066 | 06007 | 000000 | NOP | MP |
| 1067 | 06010 | 000000 | NOP | UIT |

1069* III. ASCII FRONT PANEL PROGRAM

1070*

| | | | | | |
|------|-------|--------|-----|-----------|-------------------------------|
| 1071 | 06011 | 077771 | VCP | STB P1.B | SAVE B-REG. |
| 1072 | 06012 | 002440 | | CLA,SEZ | |
| 1073 | 06013 | 003400 | | CCA | |
| 1074 | 06014 | 073770 | | STA P1.E | SAVE E-REG. |
| 1075 | 06015 | 102201 | | SOC | |
| 1076 | 06016 | 003401 | | CCA,RSS | |
| 1077 | 06017 | 002400 | | CLA | |
| 1078 | 06020 | 073767 | | STA P1.O | SAVE O-REG. |
| 1079 | 06021 | 002400 | | CLA | SET IF NO RESPONSE TO LIA 2 |
| 1080 | 06022 | 102502 | | LIA 2 | GET GLOBAL REG. |
| 1081 | 06023 | 102302 | | SFS 2 | IS GLOBAL REGISTER ENABLED? |
| 1082 | 06024 | 033434 | | IOR .100K | ADD BIT 15 IF TURNED ON |
| 1083 | 06025 | 073766 | | STA P1.GF | SAVE GLOBAL FLAG |
| 1084 | 06026 | 006400 | | CLB | |
| 1085 | 06027 | 102102 | | STF 2 | DISBLE GLOBAL REGISTER |
| 1086 | 06030 | 106602 | | OTB 2 | INSURE DIAG. MODE IS DISABLED |
| 1087 | 06031 | 063426 | | LDA .2100 | SAVE DATA ON SECOND PAGE |
| 1088 | 06032 | 164000 | | LDB A,I | |
| 1089 | 06033 | 077773 | | STB P1.T0 | |
| 1090 | 06034 | 007400 | | CCB | NOW MAKE LOCATION -1 |
| 1091 | 06035 | 174000 | | STB A,I | |
| 1092 | 06036 | 064100 | | LDR 100B | NOW SAVE MAP DATA |
| 1093 | 06037 | 077774 | | STB P1.T1 | |
| 1094 | 06040 | 002404 | | CLA,INA | POINT MAP TO SECOND PAGE |
| 1095 | 06041 | 070100 | | STA 100B | |
| 1096 | 06042 | 102713 | | STC 13B | RE ENABLE MAPS |
| 1097 | 06043 | 064100 | | LDR 100B | GET DATA |
| 1098 | 06044 | 006021 | | SSB,RSS | IF NEGATIVE THEN MAPS ON |
| 1099 | 06045 | 006400 | | CLB | OTHERWISE MAPS OFF |
| 1100 | 06046 | 106711 | | CLC 11B | NOW TURN MAPPING OFF |
| 1101 | 06047 | 026050 | | JMP *+1 | DO IT |
| 1102 | 06050 | 077763 | | STB P1.EM | SAVE FLAG |
| 1103 | 06051 | 063426 | | LDA .2100 | NOW RESTOR DATA AND MAP REG. |
| 1104 | 06052 | 067773 | | LDB P1.T0 | DATA |
| 1105 | 06053 | 174000 | | STB A,I | |
| 1106 | 06054 | 067774 | | LDB P1.T1 | AND MAP |
| 1107 | 06055 | 074100 | | STB 100B | |

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| | | | | | |
|------|-------|--------|-------|-------------|------------------------------------|
| 1109 | 06056 | 063404 | VCP0 | LDA .207 | INDICATE IN VCP |
| 1110 | 06057 | 102601 | | OTA CPUST | |
| 1111 | 06060 | 017743 | | JSR RP.SC | SET FOR SYSTEM CONSOLE |
| 1112 | 06061 | 107723 | | CLC 23B,C | TURN OFF DMA |
| 1113 | 06062 | 106532 | | LIB STS | CLEAR BREAK FLAG |
| 1114 | 06063 | 005226 | | RBL,ELB | PUT BREAK BIT IN E REG. |
| 1115 | 06064 | 107503 | | LIB 3,C | GET SINGLE CYCLE FLAG BIT |
| 1116 | 06065 | 102503 | | LIA 3 | SET M = TO P-1 |
| 1117 | 06066 | 006061 | | SEZ,SSB,RSS | IF HALT ONLY |
| 1118 | 06067 | 043435 | | ADA .M1 | |
| 1119 | 06070 | 001665 | | ELA,CLE,ERA | |
| 1120 | 06071 | 073765 | | STA P1.M | |
| 1121 | 06072 | 005665 | | ELB,CLE,ERB | CLEAR SINGLE |
| 1122 | 06073 | 107603 | | OTB 3,C | |
| 1123 | 06074 | 063337 | | LDA DFI | OUT PUT BASIC REGISTERS |
| 1124 | 06075 | 073762 | | STA P1.DF | |
| 1125 | 06076 | 102502 | | LIA 2 | GET GLOBAL REG |
| 1126 | 06077 | 053410 | | CPA .20 | NORMAL CONSOLE |
| 1127 | 06100 | 026111 | | JMP VCP1 | YES - SKIP DS CLEAN UP |
| 1128 | 06101 | 002006 | | INA,SZA | ALLOW TIME FOR SET UP |
| 1129 | 06102 | 026101 | | JMP *-1 | |
| 1130 | 06103 | 062107 | | LDA CSVCP | NOW CLEAN UP DS CARD |
| 1131 | 06104 | 017746 | | JSR CS.FT | |
| 1132 | 06105 | 026206 | | JMP PRST | NO MORE TRY RESETTING THE COMPUTER |
| 1133 | 06106 | 017745 | | JSR CS.CM | TELL CARD TO GO INTO VCP MODE |
| 1134 | 06107 | 067400 | CSVCP | OCT 67400 | |
| 1135 | 06110 | 026741 | | JMP CRLF | |
| 1136 | 06111 | 063425 | VCP1 | LDA .1000 | SET TRANSMITT |
| 1137 | 06112 | 102632 | | OTA STS | TAKE IT OUT OF DIAG MODE |
| 1138 | 06113 | 102631 | | OTA CTL | |
| 1139 | 06114 | 102630 | | OTA DR | TRANS. A NULL |
| 1140 | 06115 | 103730 | | STC DR,C | |
| 1141 | 06116 | 002400 | | CLA | |
| 1142 | 06117 | 002007 | | INA,SZA,RSS | |
| 1143 | 06120 | 026206 | | JMP PRST | TIMED OUT SO RESET COMPUTER |
| 1144 | 06121 | 102330 | | SFS DR | |
| 1145 | 06122 | 026117 | | JMP *-3 | |
| 1146 | 06123 | 026741 | | JMP CRLF | |

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| | | | | | |
|------|-------|--------|-------|-------------|--------------------------------|
| 1148 | 06124 | 103503 | EXITS | LIA 3,C | SET SINGLE CYCLE FLAG |
| 1149 | 06125 | 033434 | | IOR .100K | |
| 1150 | 06126 | 103603 | | OTA 3,C | |
| 1151 | 06127 | 006401 | | CLB,RSS | |
| 1152 | 06130 | 007400 | EXIT | CCB | SET RUN |
| 1153 | 06131 | 077773 | | STB P1.T0 | |
| 1154 | 06132 | 102503 | | LIA 3 | GET RUN (SINGLE CYCLE) ADDRESS |
| 1155 | 06133 | 073774 | | STA P1.T1 | |
| 1156 | 06134 | 063423 | | LDA .377 | SET VCP FLAG AND PROG IN EXC. |
| 1157 | 06135 | 102601 | | OTA CPUST | |
| 1158 | 06136 | 003500 | | CCA,CLE | |
| 1159 | 06137 | 102624 | | OTA 24B | |
| 1160 | 06140 | 102603 | | OTA 3 | CLEAR AUTO FLAG |
| 1161 | 06141 | 102102 | | STF 2 | TURN OFF GLOBAL REG. |
| 1162 | 06142 | 067766 | | LDB P1.GF | GET GLOBAL REG. AND FLAG |
| 1163 | 06143 | 005621 | | ELB,BRS | MOVE FLAG TO E REG. |
| 1164 | 06144 | 006002 | | SZB | DID GR HAVE A VALUE |
| 1165 | 06145 | 106602 | | OTB 2 | |
| 1166 | 06146 | 002040 | | SEZ | |
| 1167 | 06147 | 103102 | | CLF 2 | TURN IT ON IF PREVIOUSLY ON |
| 1168 | 06150 | 067770 | | LDB P1.E | SET UP E-REG. |
| 1169 | 06151 | 005500 | | FRB | |
| 1170 | 06152 | 103101 | | CLO | |
| 1171 | 06153 | 067767 | | LDR P1.0 | AND O-REG. |
| 1172 | 06154 | 006020 | | SSB | |
| 1173 | 06155 | 102101 | | STO | |
| 1174 | 06156 | 067764 | | LDB P1.1 | REVERSE INTERRUPT SENSE |
| 1175 | 06157 | 007000 | | CMB | |
| 1176 | 06160 | 077764 | | STB P1.I | |
| 1177 | 06161 | 067763 | | LDB P1.EM | AND MAP FLAG |
| 1178 | 06162 | 007000 | | CMB | |
| 1179 | 06163 | 077763 | | STR P1.EM | |
| 1180 | 06164 | 067772 | | LDR P1.A | RESTORE A & B REGISTERS |
| 1181 | 06165 | 060001 | | LDA B | |
| 1182 | 06166 | 067771 | | LDR P1.B | |
| 1183 | 06167 | 037773 | | ISZ P1.T0 | SINGLE CYCLE? |
| 1184 | 06170 | 026177 | | JMP EXITN | YES |
| 1185 | 06171 | 037763 | | ISZ P1.EM | WAS EXTENDED MEMORY ON? |
| 1186 | 06172 | 102711 | | STC 11B | YES THEN TURN IT ON |
| 1187 | 06173 | 037764 | | ISZ P1.I | |
| 1188 | 06174 | 102100 | | STF 0 | TURN ON INTERRUPTS |
| 1189 | 06175 | 102702 | | STC 2 | TURN OFF ROM |
| 1190 | 06176 | 127774 | | JMP P1.T1,I | START EXECUTION |
| 1191 | 06177 | 037763 | EXITN | ISZ P1.EM | WAS EXTENDED MEMORY ON? |
| 1192 | 06200 | 102711 | | STC 11B | YES TURN IT ON |
| 1193 | 06201 | 037764 | | ISZ P1.I | |
| 1194 | 06202 | 102100 | | STF 0 | |
| 1195 | 06203 | 106703 | | CLC 3 | |
| 1196 | 06204 | 102702 | | STC 2 | |
| 1197 | 06205 | 127774 | | JMP P1.T1,I | |

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1199*
1200 06206 107700 PRST CLC 0,C      GENERATE CRS
1201 06207 002400      CLA          CLEAR INTERRUPTS
1202 06210 073764      STA P1.I
1203 06211 102600      OTA 0          AND MASK REGISTER
1204 06212 073763      STA P1.EM      AND MAPPS
1205 06213 067766      LDB P1.GF      CLEAR GLOBAL REG. ENABLE
1206 06214 005665      ELB,CLE,ERB
1207 06215 077766      STB P1.GF
1208 06216 026056      JMP VCP0
1209*
1210 06217 063403 CLMEM LDA .2      GET STARTING ADDRESS
1211 06220 006400      CLB
1212 06221 106603      OTB 3          CLEAR P REGISTER
1213 06222 174000      STB A,I        CLEAR MEMORY
1214 06223 154000      CPB A,I        DID IT STORE?
1215 06224 002005      INA,RSS       YES
1216 06225 026206      JMP PRST      NO THEN END OF MEMORY
1217 06226 002021      SSA,RSS       DONE ALL OF MEMORY
1218 06227 026222      JMP *-5       NO DO NEXT LOCATION
1219 06230 102711      STC 11B      TURN MAPS ON AND
1220 06231 026232      JMP *+1
1221 06232 106713      CLC 13B
1222 06233 063413      LDA .40      NOW CLEAR EXTENDED MEMORY
1223 06234 070137 CLM0 STA 137B
1224 06235 102713      STC 13B
1225 06236 063432      LDA .76K     LAST PAGE
1226 06237 007400      CCB          IS MAPPING THERE
1227 06240 174000      STB A,I
1228 06241 106713      CLC 13B
1229 06242 154000      CPB A,I        ??
1230 06243 026264      JMP CLM2      NO
1231 06244 102713      STC 13B
1232 06245 006400      CLB
1233 06246 174000 CLM1 STB A,I
1234 06247 164000      LDB A,I        CHECK IF STORED
1235 06250 006002      SZB
1236 06251 026264      JMP CLM2      NO THEN END OF MEMORY
1237 06252 002004      INA
1238 06253 002021      SSA,RSS
1239 06254 026246      JMP CLM1
1240 06255 106713      CLC 13B      DISABLE MAPS
1241 06256 064137      LDB 137B     MOVE TO NEXT PAGE
1242 06257 101100      RRR 16
1243 06260 053423      CPA .377     END OF MEMORY?
1244 06261 026264      JMP *+3
1245 06262 002004      INA          NO MOVE TO NEXT LOCATION
1246 06263 026234      JMP CLM0
1247 06264 106713 CLM2 CLC 13B     DISABLE MAPS
1248 06265 006400      CLB
1249 06266 174000      STB A,I
1250 06267 074137      STR 137B     CLEAR MAPS
1251 06270 026206      JMP PRST     YES NOW PRESET THE REST

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|------|-------|--------|----------------|---------------------------------|
| 1253 | 06271 | 063423 | EXECU LDA .377 | INDICATE |
| 1254 | 06272 | 102601 | OTA CPUST | PROGRAM IN EXECUTION |
| 1255 | 06273 | 003400 | CCA | |
| 1256 | 06274 | 102603 | OTA 3 | CLEAR AUTO FLAG |
| 1257 | 06275 | 006400 | CLB | NO PARAMETERS |
| 1258 | 06276 | 102702 | STC 2 | TURN OFF ROM |
| 1259 | 06277 | 024002 | JMP 2 | AND START PROGRAM AT LOCATION 2 |
| | | | | |
| 1261 | 06300 | 017747 | LOAD JSB IN1C | GET NEXT CHR FOR LOADER TYPE |
| 1262 | 06301 | 001727 | ALF,ALF | |
| 1263 | 06302 | 073775 | STA P1.T2 | |
| 1264 | 06303 | 017747 | JSB IN1C | |
| 1265 | 06304 | 067775 | LDB P1.T2 | |
| 1266 | 06305 | 030001 | IOR R | |
| 1267 | 06306 | 073775 | STA P1.T2 | |
| 1268 | 06307 | 103503 | LIA 3,C | GET CURRENT PAGE |
| 1269 | 06310 | 013432 | AND .76K | MASK LOWER BITS |
| 1270 | 06311 | 033430 | IOR .1700 | ADD POINTER |
| 1271 | 06312 | 073762 | STA P1.DF | SAVE IT |
| 1272 | 06313 | 006500 | CLB,CLE | |
| 1273 | 06314 | 174000 | STR A,I | CLEAR LOCATION |
| 1274 | 06315 | 001200 | RAL | MAKE IT BYTE ADDRESS |
| 1275 | 06316 | 073776 | STA P1.T3 | SAVE IT |
| 1276 | 06317 | 063441 | LDA .N20 | SET MAX INPUT |
| 1277 | 06320 | 073777 | STA P1.CT | |
| 1278 | 06321 | 017754 | JSB IN.N | |
| 1279 | 06322 | 067773 | LDB P1.T0 | CHECK IF LOAD AND GO |
| 1280 | 06323 | 101100 | RRR 16 | SWAP REGISTERS |
| 1281 | 06324 | 053354 | CPA SL | IS IT A LOAD ONLY |
| 1282 | 06325 | 026360 | JMP LOAD2 | YES |
| 1283 | 06326 | 053362 | CPA SW | IS THIS A WRITE |
| 1284 | 06327 | 026360 | JMP LOAD2 | YES THEN NO FILE NAME |
| 1285 | 06330 | 101100 | RRR 16 | NO SWAP REGISTERS AGAIN |
| 1286 | 06331 | 073773 | STA P1.T0 | SAVE CHR |
| 1287 | 06332 | 053406 | CPA .15 | IF RETURN ONLY |
| 1288 | 06333 | 026365 | JMP LOADC | THEN DEFAULT |
| 1289 | 06334 | 026341 | JMP LOAD1 | PROCESS THE CHR |

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| | | | | | |
|-------|-------|--------|-------|-----------|---------------------------------------|
| 1291 | 06335 | 017747 | LOAD0 | JSB IN1C | GET A CHARACTER |
| 1292 | 06336 | 073773 | | STA P1.T0 | SAVE IT |
| 1293 | 06337 | 053406 | | CPA .15 | END OF INPUT? |
| 1294 | 06340 | 026365 | | JMP LOADC | YES DO BOOT |
| 1295 | 06341 | 067776 | LOAD1 | LDB P1.T3 | PUT CHR IN BUFFER |
| 1296 | 06342 | 004065 | | CLE,ERB | ADDR. UPPER/LOWER |
| 1297 | 06343 | 060001 | | LDA B | CHANGE HANDS |
| 1298 | 06344 | 164000 | | LDB A,I | |
| 1299 | 06345 | 047773 | | ADB P1.T0 | |
| 1300 | 06346 | 002041 | | SEZ,RSS | |
| 1301 | 06347 | 005727 | | BLF,BLF | |
| 1302 | 06350 | 174000 | | STB A,I | |
| 1303 | 06351 | 006400 | | CLB | CLEAR NEXT LOCATION |
| 1304 | 06352 | 002004 | | INA | |
| 1305 | 06353 | 174000 | | STB A,I | |
| 1306 | 06354 | 102101 | | STD | INDICAT TEXT HAS STARTED |
| 1307 | 06355 | 037776 | | ISZ P1.T3 | |
| 1308 | 06356 | 037777 | | ISZ P1.CT | OVER |
| 1309 | 06357 | 026335 | | JMP LOAD0 | NO DO ANOTHER CHR |
| 1310 | 06360 | 101100 | LOAD2 | RRR 16 | SWAP REGISTERSLT |
| 1311 | 06361 | 053406 | | CPA .15 | WAS IT A CR? |
| 1312 | 06362 | 002401 | | CLA,RSS | YES PROCEED |
| 1313 | 06363 | 026735 | | JMP INQ!? | NO |
| 1314 | 06364 | 073762 | | STA P1.DF | |
| 1315 | 06365 | 063415 | LOADC | LDA .6412 | DO CRLF |
| 1316 | 06366 | 017751 | | JSB OUT2C | |
| 1317 | 06367 | 107700 | | CLC 0,C | |
| 1318 | 06370 | 067775 | | LDB P1.T2 | GET ASCII CHARACTERRS |
| 1319 | 06371 | 027760 | | JMP CRSP3 | GO TO LOADERS |
| 1320* | | | | | |
| 1321 | 06372 | 006002 | LDRTN | SZB | VCP START? |
| 1322 | 06373 | 026056 | | JMP VCP0 | YES |
| 1323 | 06374 | 017743 | | JSB RP.SC | RESET GLOBAL REG |
| 1324 | 06375 | 053410 | | CPA .20 | NORMAL CONSOLE? |
| 1325 | 06376 | 026402 | | JMP *+4 | YES |
| 1326 | 06377 | 062107 | | LDA CSVCP | GET VCP MODE COMMAND |
| 1327 | 06400 | 017746 | | JSB CS.FT | NO - THEN TELL DS TO GO INTO VCP MODE |
| 1328 | 06401 | 026056 | | JMP VCP0 | ERROR |
| 1329 | 06402 | 063376 | LDRTC | LDA \$LC | CHECK IF LOAD COMPLETE OR ERROR |
| 1330 | 06403 | 067755 | | LDB P1ERR | GET FLAG |
| 1331 | 06404 | 006002 | | SZB | |
| 1332 | 06405 | 026410 | | JMP *+3 | ERROR |
| 1333 | 06406 | 017751 | | JSB OUT2C | OUTPUT RESULTS |
| 1334 | 06407 | 026737 | | JMP INQLF | |
| 1335 | 06410 | 063377 | LDRTE | LDA \$ER | INDICATE ERROR |
| 1336 | 06411 | 017751 | | JSB OUT2C | |
| 1337 | 06412 | 063413 | | LDA .40 | AND SPACE |
| 1338 | 06413 | 017752 | | JSB OUT1C | |
| 1339 | 06414 | 067755 | | LDB P1ERR | NOW ERROR ADDRESS |
| 1340 | 06415 | 000040 | | CLE | FULL 16 BITS |
| 1341 | 06416 | 017753 | | JSB OUT.N | |
| 1342 | 06417 | 026737 | | JMP INQLF | |

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1344*      SET UP MAPS
1345*
1346 06420 017754  MAPST JSB IN.N      GET STARTING MAP
1347 06421 053406          CPA .15      IS THAT RIGHT?
1348 06422 026424          JMP **2
1349 06423 026735          JMP INQ!?      NO
1350 06424 067774          LDB P1.T1      YES
1351 06425 063417          LDA .100
1352 06426 174000          STB A,I
1353 06427 002004          INA
1354 06430 053470          CPA .140
1355 06431 026737          JMP INQLF
1356 06432 006004          INB
1357 06433 026426          JMP *-5
1358*
1359 06434 107700  PTST  CLC 0,C      RESET SYSTEM
1360 06435 063403          LDA .2
1361 06436 102600          OTA 0      SET VCP PRETEST FLAG BIT
1362 06437 002400          CLA
1363 06440 027761          JMP CRSP3+1  DO IT
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|------|-------|--------|------|-----------|---------------------------------------|
| 1365 | 06441 | 067762 | INQ | LDB P1.DF | CHECK FOR FIRST ENTRY |
| 1366 | 06442 | 006003 | | SZB,RSS | |
| 1367 | 06443 | 026461 | | JMP INQ. | |
| 1368 | 06444 | 160001 | | LDA B,I | GET PARAMETER |
| 1369 | 06445 | 006004 | | INB | MOVE TO NEXT |
| 1370 | 06446 | 053344 | | CPA DFL. | END OF TRANSFER |
| 1371 | 06447 | 006400 | | CLB | YES |
| 1372 | 06450 | 077762 | | STB P1.DF | |
| 1373 | 06451 | 067763 | | LDB P1.EM | CHECK IF MAPS ARE ON |
| 1374 | 06452 | 006003 | | SZB,RSS | |
| 1375 | 06453 | 026456 | | JMP *+3 | NO |
| 1376 | 06454 | 053344 | | CPA \$T | YES - IF DISPLAYING T THEN USE U |
| 1377 | 06455 | 063356 | | LDA \$U | |
| 1378 | 06456 | 073773 | | STA P1.TO | SAVE CHARACTER |
| 1379 | 06457 | 017752 | | JSB OUT1C | OUTPUT PARAMETER |
| 1380 | 06460 | 026543 | | JMP INQ.1 | NOW PRINT THE VALUE |
| 1381 | 06461 | 002400 | INQ. | CLA | TELL DS TO TRANSMITT AND GET A BUFFER |
| 1382 | 06462 | 017744 | | JSB CS.TR | ONLY IF IT IS REALLY DS |
| 1383 | 06463 | 017747 | | JSB IN1C | NOW GET INPUT |
| 1384 | 06464 | 073773 | | STA P1.TO | SAVE FIRST CHARACTER |
| 1385 | 06465 | 053363 | | CPA \$% | CONTROL FUNCTION? |
| 1386 | 06466 | 002001 | | RSS | |
| 1387 | 06467 | 026517 | | JMP INQ.0 | NO |
| 1388 | 06470 | 017747 | | JSB IN1C | GET NEXT CHARACTER |
| 1389 | 06471 | 073773 | | STA P1.TO | SAVE THE CHR |
| 1390 | 06472 | 053357 | | CPA \$R | IS THIS A RUN COMMAND? |
| 1391 | 06473 | 026130 | | JMP EXIT | YES |
| 1392 | 06474 | 053360 | | CPA \$S | IS THIS A SINGLE CYCLE? |
| 1393 | 06475 | 026124 | | JMP EXITS | YES |
| 1394 | 06476 | 053340 | | CPA \$P | IS THIS A PRESET? |
| 1395 | 06477 | 026206 | | JMP PRST | YES |
| 1396 | 06500 | 053352 | | CPA \$C | CLEAR MEMOPY? |
| 1397 | 06501 | 026217 | | JMP CLMEM | YES |
| 1398 | 06502 | 053346 | | CPA \$E | EXECUTE AT 4 |
| 1399 | 06503 | 026271 | | JMP EXECU | YES |
| 1400 | 06504 | 053354 | | CPA \$L | LOAD? |
| 1401 | 06505 | 026300 | | JMP LOAD | YES |
| 1402 | 06506 | 053342 | | CPA \$B | BOOT (LOAD AND GO)? |
| 1403 | 06507 | 026300 | | JMP LOAD | YES |
| 1404 | 06510 | 053362 | | CPA \$W | WRITE. |
| 1405 | 06511 | 026300 | | JMP LOAD | YES |
| 1406 | 06512 | 053343 | | CPA \$M | MAP SET UP? |
| 1407 | 06513 | 026420 | | JMP MAPST | YES |
| 1408 | 06514 | 053344 | | CPA \$T | SELF TEST? |
| 1409 | 06515 | 026434 | | JMP PTST | YES |
| 1410 | 06516 | 026735 | | JMP INQ!? | NONE SO ERROR |

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|------|-------|--------|-------|-----------|------------------------|
| 1412 | 06517 | 053357 | INQ.0 | CPA SR | I/O REGISTERS |
| 1413 | 06520 | 002001 | | RSS | YES |
| 1414 | 06521 | 026527 | | JMP **6 | NO |
| 1415 | 06522 | 017747 | | JSB IN1C | GET NEXT NUMBER |
| 1416 | 06523 | 067773 | | LDB P1.T0 | NOW PUT THFM TO GETHER |
| 1417 | 06524 | 005727 | | BLF,BLF | |
| 1418 | 06525 | 030001 | | IOR B | |
| 1419 | 06526 | 073773 | | STA P1.T0 | SAVE IT |
| 1420 | 06527 | 102502 | | LIA 2 | CHECK IF DS |
| 1421 | 06530 | 053410 | | CPA .20 | |
| 1422 | 06531 | 026543 | | JMP INQ.1 | NO |
| 1423 | 06532 | 067773 | INQ# | LDB P1.T0 | YES ECHO CHR |
| 1424 | 06533 | 060001 | | LDA B | |
| 1425 | 06534 | 001727 | | ALF,ALF | |
| 1426 | 06535 | 013422 | | AND .177 | |
| 1427 | 06536 | 002002 | | SZA | OUTPUT UPPER? |
| 1428 | 06537 | 017752 | | JSB OUT1C | YES |
| 1429 | 06540 | 067773 | | LDB P1.T0 | |
| 1430 | 06541 | 060001 | | LDA B | |
| 1431 | 06542 | 017752 | | JSB OUT1C | NOW LOWER |

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|------|-------|--------|-------|-------------|-----------------------------------|
| 1433 | 06543 | 063413 | INQ.1 | LDA .40 | OUTPUT A SPACE |
| 1434 | 06544 | 017752 | | JSB OUT1C | |
| 1435 | 06545 | 067773 | | LDB P1.TC | GET CHARACTER AGAIN |
| 1436 | 06546 | 060001 | | LDA B | CHANGE HANDS |
| 1437 | 06547 | 000040 | | CLE | |
| 1438 | 06550 | 067772 | | LDB P1.A | |
| 1439 | 06551 | 053341 | | CPA SA | IS IT A-REG. ? |
| 1440 | 06552 | 026745 | | JMP CH.OK | YES |
| 1441 | 06553 | 067771 | | LDB P1.B | |
| 1442 | 06554 | 053342 | | CPA SB | IS IT B-REG. ? |
| 1443 | 06555 | 026745 | | JMP CH.OK | YES |
| 1444 | 06556 | 106503 | | LIR 3 | |
| 1445 | 06557 | 053340 | | CPA SP | IS IT P-REG. ? |
| 1446 | 06560 | 026745 | | JMP CH.OK | YES |
| 1447 | 06561 | 107507 | | LIR 7,C | |
| 1448 | 06562 | 053361 | | CPA SV | IS IT THE VIOLATION REG.? |
| 1449 | 06563 | 026745 | | JMP CH.OK | YES |
| 1450 | 06564 | 106504 | | LIR 4 | |
| 1451 | 06565 | 053352 | | CPA SC | IS IT THE CENTRAL INTERRUPT REG.? |
| 1452 | 06566 | 026745 | | JMP CH.OK | YES |
| 1453 | 06567 | 067770 | | LDB P1.E | |
| 1454 | 06570 | 053346 | | CPA SE | IS IT E-REG. ? |
| 1455 | 06571 | 026744 | | JMP CH.OK-1 | YES |
| 1456 | 06572 | 067767 | | LDB P1.O | |
| 1457 | 06573 | 053347 | | CPA SO | IS IT O-REG. ? |
| 1458 | 06574 | 026744 | | JMP CH.OK-1 | YES |
| 1459 | 06575 | 067764 | | LDB P1.I | |
| 1460 | 06576 | 053350 | | CPA SI | IS IT INTERRUPT STATUS ? |
| 1461 | 06577 | 026744 | | JMP CH.OK-1 | YES |
| 1462 | 06600 | 067763 | | LDB P1.EM | |
| 1463 | 06601 | 053351 | | CPA SK | EXTENDED MEMORY FLAG |
| 1464 | 06602 | 026744 | | JMP CH.OK-1 | YES |
| 1465 | 06603 | 067766 | | LDR P1.GF | |
| 1466 | 06604 | 053345 | | CPA SG | IS IT GLOBAL-REG. ? |
| 1467 | 06605 | 026745 | | JMP CH.OK | YES |
| 1468 | 06606 | 067765 | | LDB P1.M | |
| 1469 | 06607 | 053343 | | CPA SM | IS IT MEMORY ? |
| 1470 | 06610 | 026745 | | JMP CH.OK | YES |
| 1471 | 06611 | 005100 | | BRS | CHECK IF A OR B ADDRESSABLE |
| 1472 | 06612 | 006003 | | SZB,RSS | |
| 1473 | 06613 | 026627 | | JMP INQ.2 | YES |
| 1474 | 06614 | 167765 | | LDB P1.M,I | |
| 1475 | 06615 | 053344 | | CPA ST | IS IT DATA FROM MEMORY |
| 1476 | 06616 | 026745 | | JMP CH.OK | YES |
| 1477 | 06617 | 067765 | | LDB P1.M | GET ADDRESS |
| 1478 | 06620 | 102711 | | STC 11B | TURN ON MAPS |
| 1479 | 06621 | 026622 | | JMP *+1 | ENABLE THEM |
| 1480 | 06622 | 164001 | | LDB R,J | GET DATA |
| 1481 | 06623 | 106711 | | CLC 11B | NOW TURN THEM OFF |
| 1482 | 06624 | 026625 | | JMP *+1 | |
| 1483 | 06625 | 053356 | | CPA SU | CROSS MAP LOAD? |
| 1484 | 06626 | 026745 | | JMP CH.OK | YES |

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1486*      CHECK FOR I/O REGISTERS
1487*
1488 06627 067766  INQ.2 LDB P1.GF  GET GLOBAL REGISTER
1489 06630 107602      OTB 2,C  YES SET IT UP AND ENABLE IT
1490 06631 006400      CLB      CLEAR INCASE NO RESPONSE
1491 06632 106502      LIB 2    CHECK IF THERE IS A CARD
1492 06633 006003      SZB,RSS
1493 06634 026715      JMP INQRX NO CARD SO ERROR
1494 06635 006400      CLB
1495 06636 106500  LIB  LIB 0    GET INTERRUPT MASK
1496 06637 053401      CPA SRM  IS THIS IT?
1497 06640 026733      JMP INQ.3 YES
1498 06641 106520      LIB 20B GET SELF-CONFIGURATION REGISTER
1499 06642 053364      CPA SR0  IS THIS IT?
1500 06643 026733      JMP INQ.3 YES
1501 06644 106521      LIB 21B GET CONTROL REGISTER
1502 06645 053365      CPA SR1  IS THIS IT?
1503 06646 026733      JMP INQ.3 YES
1504 06647 106522      LIB 22B GET ADDRESS REGISTER
1505 06650 053366      CPA SR2  IS THIS IT?
1506 06651 026733      JMP INQ.3 YES
1507 06652 106523      LIB 23B GET COUNT REGISTER
1508 06653 053367      CPA SR3  IS THIS IT?
1509 06654 026733      JMP INQ.3 YES
1510 06655 053370      CPA SRD  DATA REGISTER
1511 06656 026726      JMP INQRD YES
1512 06657 053371      CPA SRC  CONTROL REGISTER
1513 06660 026730      JMP INQRC YES
1514 06661 053372      CPA SRS  STATUS REGISTER
1515 06662 026732      JMP INQRS YES
1516 06663 006404      CLB,INB GET READY FOR DIAG. MODE 1
1517 06664 053373      CPA SRI  IS IT?
1518 06665 026717      JMP INQDM YES
1519 06666 006004      INB     HOW ABOUT DIAG.2
1520 06667 053374      CPA SRX  DIAG. MODE 2?
1521 06670 026717      JMP INQDM YES
1522 06671 006400      CLB     CHECK FLAGS
1523 06672 102220      SFC 20B SELF DMA?
1524 06673 006004      INB
1525 06674 005723      BLF,RBR MOVE OVER 3
1526 06675 102221      SFC 21B
1527 06676 006004      INB
1528 06677 005723      BLF,RBR
1529 06700 102222      SFC 22B
1530 06701 006004      INB
1531 06702 005723      BLF,RBR
1532 06703 102223      SFC 23B
1533 06704 006004      INB
1534 06705 005723      BLF,RBR
1535 06706 102224      SFC 24B
1536 06707 006004      INB
1537 06710 005723      BLF,PBR
1538 06711 102230      SFC 30B
1539 06712 006004      INB
1540 06713 053375      CPA SRF  FLAGS REQUEST?

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|------|-------|--------|-------|-----------|---------------------------------------|
| 1541 | 06714 | 026733 | | JMP INQ.3 | YES |
| 1542 | 06715 | 017743 | INQRX | JSB RP.SC | RESET GLOBAL REGISTER |
| 1543 | 06716 | 026735 | | JMP INQ!? | NONE SO ERROR |
| 1544 | 06717 | 102502 | INQDM | LIA 2 | GET SELECT CODE |
| 1545 | 06720 | 013416 | | AND .77 | |
| 1546 | 06721 | 032636 | | ICR LIB | BUILD LIA INSTRUCTION FOR SELECT CODE |
| 1547 | 06722 | 106602 | | OTB 2 | OUTPUT DIAGNOSE MODE |
| 1548 | 06723 | 064000 | | LDB A | |
| 1549 | 06724 | 014000 | | JSB 0 | EXECUTE INSTRUCTION |
| 1550 | 06725 | 026733 | | JMP INQ.3 | DIASPLAY DATA |
| 1551 | 06726 | 106530 | INQRD | LIB 30B | GET DATA REGISTER |
| 1552 | 06727 | 026733 | | JMP INQ.3 | |
| 1553 | 06730 | 106531 | INQRC | LIB 31B | GET CONTROL REGISTER |
| 1554 | 06731 | 026733 | | JMP INQ.3 | |
| 1555 | 06732 | 106532 | INQRS | LIB STS | GET STATUS REGISTER |
| 1556 | 06733 | 017743 | INQ.3 | JSB RP.SC | RESET GLOBAL REGISTER |
| 1557 | 06734 | 026745 | | JMP CH.OK | |
| 1559 | 06735 | 063400 | INQ!? | LDA \$!? | NONE OF THE ABOVE |
| 1560 | 06736 | 017751 | | JSB OUT2C | THEN TELL OPERATOR |
| 1561 | 06737 | 002400 | INQLF | CLA | |
| 1562 | 06740 | 073762 | | STA P1.DF | DON'T CONTINUE STRING |
| 1563 | 06741 | 063415 | CRLF | LDA .6412 | CARRIAGE RETURN LINE FEED |
| 1564 | 06742 | 017751 | | JSB OUT2C | |
| 1565 | 06743 | 026441 | | JMP INQ | |
| 1567 | 06744 | 002300 | | CCE | ONLY ONE DIGIT |
| 1568 | 06745 | 017753 | CH.OK | JSB OUT.N | OUTPUT NUMBER OUTPUT |
| 1569 | 06746 | 067762 | | LDB P1.DF | CHECK IF STRING OUTPUT |
| 1570 | 06747 | 006002 | | SZB | |
| 1571 | 06750 | 026441 | | JMP INQ | YES |
| 1572 | 06751 | 077776 | | STB P1.T3 | CLEAR INC-DEC FLAG |

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|------|-------|--------|------|-------------|------------------------------------|
| 1574 | 06752 | 017744 | | JSB CS.TR | TELL DS TO XMIT AND GET BUFFFR |
| 1575 | 06753 | 017754 | | JSB IN.N | INPUT A NUMBER |
| 1576 | 06754 | 053406 | | CPA .15 | IS THAT ALL? |
| 1577 | 06755 | 026765 | | JMP ST.N | YES |
| 1578 | 06756 | 053355 | | CPA SN | INCREMENT MEMORY LOCATION? |
| 1579 | 06757 | 027072 | | JMP ST.NO | YES CHECK IF T ENTRY |
| 1580 | 06760 | 053353 | | CPA SD | DECREMENT MEMORY LOCATION |
| 1581 | 06761 | 027072 | | JMP ST.NO | YES |
| 1582 | 06762 | 102201 | | SOC | WAS THERE A NUMBER? |
| 1583 | 06763 | 026735 | | JMP INQ!? | NO |
| 1584 | 06764 | 026464 | | JMP INQ.+3 | YES |
| 1585 | 06765 | 067773 | ST.N | LDB P1.TO | GET ORIGINAL CHARACTER |
| 1586 | 06766 | 060001 | | LDA B | CHANGE HANDS |
| 1587 | 06767 | 067774 | | LDB P1.I1 | GET DATA THAT WAS INPUT |
| 1588 | 06770 | 102301 | | SOS | ANY INPUT? |
| 1589 | 06771 | 026741 | | JMP CRLF | NO GO ASK FOR SOME |
| 1590 | 06772 | 006042 | | SEZ,SZB | IF ONLY ONE CHARACTER |
| 1591 | 06773 | 007400 | | CCB | AND A 1 THEN -1 FOR WORD |
| 1592 | 06774 | 053361 | | CPA SV | WAS IT THE VIOLATION REG. |
| 1593 | 06775 | 107607 | | OTB 7,C | YES |
| 1594 | 06776 | 053352 | | CPA SC | WAS IT THE CENTRAL INTERRUPT |
| 1595 | 06777 | 106604 | | OTB 4 | YES |
| 1596 | 07000 | 053341 | | CPA SA | WAS IT A-REG. ? |
| 1597 | 07001 | 077772 | | STB P1.A | YES |
| 1598 | 07002 | 053342 | | CPA SB | WAS IT B-REG. ? |
| 1599 | 07003 | 077771 | | STB P1.B | YES |
| 1600 | 07004 | 053346 | | CPA SE | WAS IT E-REG. ? |
| 1601 | 07005 | 077770 | | STB P1.E | YES |
| 1602 | 07006 | 053347 | | CPA SO | WAS IT O-REG. ? |
| 1603 | 07007 | 077767 | | STR P1.O | YES |
| 1604 | 07010 | 053350 | | CPA SI | WAS IT THE INTERRUPT SYSTEM? |
| 1605 | 07011 | 077764 | | STB P1.I | YES |
| 1606 | 07012 | 053351 | | CPA SK | MAPS ON/OFF |
| 1607 | 07013 | 077763 | | STB P1.EM | YES |
| 1608 | 07014 | 053345 | | CPA SG | WAS IT THE GLOBAL-REG. ? |
| 1609 | 07015 | 077766 | | STB P1.GF | YES |
| 1610 | 07016 | 067774 | | LDB P1.T1 | RESTOR B REG |
| 1611 | 07017 | 053344 | | CPA ST | WAS IT MEMORY DATA CHANGE? |
| 1612 | 07020 | 177765 | | STB P1.M,I | YES |
| 1613 | 07021 | 053356 | | CPA SU | CROSS MAP? |
| 1614 | 07022 | 002001 | | RSS | |
| 1615 | 07023 | 027033 | | JMP *+8 | |
| 1616 | 07024 | 060001 | | LDA B | |
| 1617 | 07025 | 067765 | | LDB P1.M | GET ADDRESS |
| 1618 | 07026 | 102711 | | STC 11B | TURN ON MAPS |
| 1619 | 07027 | 027030 | | JMP *+1 | ENABLE THEM |
| 1620 | 07030 | 170001 | | STA B,I | |
| 1621 | 07031 | 106711 | | CLC 11B | MAPS OFF |
| 1622 | 07032 | 027064 | | JMP ST.NA | CONTINUE |
| 1623 | 07033 | 005665 | | ELB,CLE,ERB | CAN'T HAVE AN INDIRECT M OR P REG. |
| 1624 | 07034 | 053343 | | CPA SM | WAS IT MEMORY ADDRESS? |
| 1625 | 07035 | 077765 | | STB P1.M | YES |
| 1626 | 07036 | 053340 | | CPA SP | WAS IT PROGRAM ADDRESS? |
| 1627 | 07037 | 106603 | | OTB 3 | YES |

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1629* CHECK I/O REG.

1630*

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|------|-------|--------|-----------------|---------------------------|
| 1631 | 07040 | 067766 | LDB P1.GF | GET GLOBAL REG |
| 1632 | 07041 | 107602 | OTB 2,C | |
| 1633 | 07042 | 067774 | LDB P1.T1 | RESTOR B |
| 1634 | 07043 | 053401 | CPA SRM | INTERRUPT MASK REGISTER? |
| 1635 | 07044 | 106600 | OTB 0 | YES |
| 1636 | 07045 | 053364 | CPA SR0 | SELF-CONFIGURATION REG.? |
| 1637 | 07046 | 106620 | OTB 20B | YES |
| 1638 | 07047 | 053365 | CPA SR1 | CONTROL REG.? |
| 1639 | 07050 | 106621 | OTB 21B | YES |
| 1640 | 07051 | 053366 | CPA SR2 | ADDRESS? |
| 1641 | 07052 | 106622 | OTB 22B | YES |
| 1642 | 07053 | 053367 | CPA SR3 | COUNT? |
| 1643 | 07054 | 106623 | OTB 23B | YES |
| 1644 | 07055 | 053370 | CPA SRD | DITA REGISTER |
| 1645 | 07056 | 106630 | OTB 30B | YES |
| 1646 | 07057 | 053371 | CPA SRC | CONTROL REGISTER |
| 1647 | 07060 | 106631 | OTB 31B | YES |
| 1648 | 07061 | 053372 | CPA SRS | STATUS REGISTER |
| 1649 | 07062 | 106632 | OTB STS | YES |
| 1650 | 07063 | 017743 | JSB RP.SC | RESET GLOBAL REG. |
| 1651 | 07064 | 067773 | ST.NA LDB P1.T0 | RESTOR A AND B REG |
| 1652 | 07065 | 060001 | LDA B | CHANGE HANDS |
| 1653 | 07066 | 067776 | LDB P1.T3 | CHECK IF INC-DEC FLAG SET |
| 1654 | 07067 | 006002 | SZB | |
| 1655 | 07070 | 027106 | JMP ST.N1 | YES |
| 1656 | 07071 | 027123 | JMP ST.N2 | PRINT RESULT |

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| | | | | | |
|------|-------|--------|-------|------------|---------------------------|
| 1658 | 07072 | 067773 | ST.N0 | LDB P1.T0 | CHECK IF ENTRY IS A T? |
| 1659 | 07073 | 073776 | | STA P1.T3 | SET INC-DEC FLAG |
| 1660 | 07074 | 101100 | | RRR 16 | CHANGE HANDS |
| 1661 | 07075 | 053344 | | CPA ST | IS IT? |
| 1662 | 07076 | 027104 | | JMP **6 | |
| 1663 | 07077 | 053356 | | CPA SU | |
| 1664 | 07100 | 027104 | | JMP **4 | |
| 1665 | 07101 | 053343 | | CPA SM | |
| 1666 | 07102 | 002001 | | RSS | |
| 1667 | 07103 | 026735 | | JMP INQ!? | |
| 1668 | 07104 | 102201 | | SOC | ANY NUMBER? |
| 1669 | 07105 | 026765 | | JMP ST.N | YES STORE NUMBER |
| 1670 | 07106 | 101100 | ST.N1 | RRR 16 | |
| 1671 | 07107 | 007400 | | CCB | DECREMENT? |
| 1672 | 07110 | 047765 | | ADB P1.M | GET MEMORY LOCATION |
| 1673 | 07111 | 053353 | | CPA SD | DECREMENT? |
| 1674 | 07112 | 027115 | | JMP **3 | YES |
| 1675 | 07113 | 067765 | | LDB P1.M | NO INCREMENT |
| 1676 | 07114 | 006004 | | INB | YES |
| 1677 | 07115 | 101100 | | RRR 16 | SWAP HANDS |
| 1678 | 07116 | 053402 | | CPA .1 | IF ONE USE 77777 |
| 1679 | 07117 | 063433 | | LDA .77NK | |
| 1680 | 07120 | 002020 | | SSA | CANT GO INDIRECT |
| 1681 | 07121 | 063403 | | LDA .2 | START WITH 2 AGAIN |
| 1682 | 07122 | 073765 | | STA P1.M | RESTORE M |
| 1683 | 07123 | 102501 | ST.N2 | LIA CPUTST | SKIP CRLF IF DS |
| 1684 | 07124 | 001710 | | ALF,SLA | |
| 1685 | 07125 | 026532 | | JMP INQ# | |
| 1686 | 07126 | 063415 | | LDA .6412 | CARRIAGE RETURN LINE FEED |
| 1687 | 07127 | 017751 | | JSB OUT2C | |
| 1688 | 07130 | 026532 | | JMP INQ# | DO NEXT LOCATION |

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| | | | | | |
|------|-------|--------|-------|-------------|-----------------------------|
| 1690 | 07131 | 002400 | IN%N | CLA | CLEAR NUMBER |
| 1691 | 07132 | 073774 | | STA P1.T1 | |
| 1692 | 07133 | 103101 | | CLO | CLEAR NUMBER FLAG |
| 1693 | 07134 | 017747 | IN%NO | JSB IN1C | GET A CHARACTER |
| 1694 | 07135 | 053406 | | CPA .15 | IS THAT ALL? |
| 1695 | 07136 | 127754 | | JMP IN.N,I | YES |
| 1696 | 07137 | 064000 | | LDB A | CHANGE HANDS |
| 1697 | 07140 | 013421 | | AND .170 | NO CHECK IF IT'S A NUMBER |
| 1698 | 07141 | 053414 | | CPA .60 | IS IT? |
| 1699 | 07142 | 027145 | | JMP *+3 | YES |
| 1700 | 07143 | 060001 | | LDA B | CHANGE HANDS |
| 1701 | 07144 | 127754 | | JMP IN.N,I | RETURN |
| 1702 | 07145 | 060001 | | LDA B | CHANGE HANDS |
| 1703 | 07146 | 013405 | | AND .7 | NO MASK OFF UPPER BITS |
| 1704 | 07147 | 067774 | | LDB P1.T1 | GET PREVIOUS INPUT |
| 1705 | 07150 | 001640 | | EIA,CLE | SAVE E AND CLEAR IT |
| 1706 | 07151 | 005666 | | ELB,CLE,ELB | POSITION BIT |
| 1707 | 07152 | 004066 | | CLE,ELB | NEXT BIT |
| 1708 | 07153 | 000065 | | CLE,ERA | RESTOR E |
| 1709 | 07154 | 030001 | | IOR B | ADD NEW INPUT |
| 1710 | 07155 | 073774 | | STA P1.T1 | SAVE RESULT |
| 1711 | 07156 | 102101 | | STO | SET NUMBER FLAG |
| 1712 | 07157 | 027134 | | JMP IN%NO | DO ANOTHER CHARACTER |
| | | | | | |
| 1714 | 07160 | 003441 | OUT%N | CCA,SEZ,RSS | |
| 1715 | 07161 | 063436 | | LDA .M6 | SET COUNT FOR OUTPUT |
| 1716 | 07162 | 073777 | | STA P1.CT | |
| 1717 | 07163 | 002404 | | CLA,INA | SET MASK FOR BIT 15 |
| 1718 | 07164 | 005200 | OUTNO | RBL | POSITION BITS |
| 1719 | 07165 | 077774 | | STB P1.T1 | SAVE RESULT |
| 1720 | 07166 | 010001 | | AND B | MASK OFF UNWANTED BITS |
| 1721 | 07167 | 033414 | | IOR .60 | MAKE IT AN ASCII NUMBER |
| 1722 | 07170 | 017752 | | JSB OUT1C | OUTPUT THE NUMBER |
| 1723 | 07171 | 067774 | | LDB P1.T1 | GET NEXT NUMBER |
| 1724 | 07172 | 005222 | | RBL,RBL | POSITION IT |
| 1725 | 07173 | 063405 | | LDA .7 | GET MASK |
| 1726 | 07174 | 037777 | | ISZ P1.CT | IS THAT ALL THE CHARACTERS? |
| 1727 | 07175 | 027164 | | JMP OUTNO | NO DO NEXT CHARACTER |
| 1728 | 07176 | 063413 | | LDA .40 | OUTPUT A SPACE |
| 1729 | 07177 | 017752 | | JSB OUT1C | |
| 1730 | 07200 | 127753 | | JMP OUT.N,I | RETURN |

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|-------|-------|--------|-------|-------------|----------------------------|
| 1733 | 07201 | 102501 | IN1C% | LIA CPUST | CHECK WHICH CARD |
| 1734 | 07202 | 001710 | | ALF,SLA | |
| 1735 | 07203 | 027217 | | JMP IN1C0 | |
| 1736 | 07204 | 063335 | | LDA TCCWI | GET INPUT CONTROL WORD |
| 1737 | 07205 | 102631 | | OTA CTL | |
| 1738 | 07206 | 017750 | | JSB I.O | GET DATA |
| 1739 | 07207 | 013422 | | AND .177 | MASK UPPER BYTE |
| 1740 | 07210 | 053422 | | CPA .177 | WAS IT A DELETE? |
| 1741 | 07211 | 026735 | | JMP INQ!? | YES |
| 1742 | 07212 | 073751 | | STA OUT2C | SAVE CHARACTER |
| 1743 | 07213 | 017752 | | JSB OUT1C | FCHO IT |
| 1744 | 07214 | 067751 | | LDB OUT2C | RESTOR CHR |
| 1745 | 07215 | 060001 | | LDA B | |
| 1746 | 07216 | 127747 | | JMP IN1C,I | RETURN |
| 1747 | 07217 | 017745 | IN1C0 | JSB CS.CM | ASK FOR INPUT |
| 1748 | 07220 | 061000 | | OCT 61000 | |
| 1749 | 07221 | 013423 | | AND .377 | USE LOWER BYTE |
| 1750 | 07222 | 127747 | | JMP IN1C,I | RETURN |
| 1751* | | | | | |
| 1752 | 07223 | 073747 | OU%2C | STA IN1C | SAVE A-REG. |
| 1753 | 07224 | 001727 | | ALF,ALF | |
| 1754 | 07225 | 017752 | | JSB OUT1C | OUTPUT UPPER HALF |
| 1755 | 07226 | 067747 | | LDB IN1C | |
| 1756 | 07227 | 060001 | | LDA B | CHANGE HANDS |
| 1757 | 07230 | 017752 | | JSB OUT1C | OUTPUT LOWER HALF |
| 1758 | 07231 | 127751 | | JMP OUT2C,I | RETURN |
| 1759* | | | | | |
| 1760 | 07232 | 013423 | OU%1C | AND .377 | MASK UPPER HALF OFF |
| 1761 | 07233 | 106501 | | LIB CPUST | CHECK WHICH INTERFACE |
| 1762 | 07234 | 005710 | | BLF,SLB | |
| 1763 | 07235 | 027244 | | JMP *+7 | DS TYPE |
| 1764 | 07236 | 013423 | | AND .377 | MASK UPPER HALF |
| 1765 | 07237 | 064000 | | LDB A | CHANGE HANDS |
| 1766 | 07240 | 063336 | | LDA TCCWO | GET OUTPUT CONRTEL WORD |
| 1767 | 07241 | 102631 | | OTA CTL | |
| 1768 | 07242 | 017750 | | JSB I.O | OUTPUT IT |
| 1769 | 07243 | 127752 | | JMP OUT1C,I | |
| 1770 | 07244 | 033431 | | IOR .60K | DS PUT BYTE REQUEST |
| 1771 | 07245 | 064000 | | LDB A | |
| 1772 | 07246 | 017750 | | JSB I.O | |
| 1773 | 07247 | 127752 | | JMP OUT1C,I | |
| 1774* | | | | | |
| 1775 | 07250 | 106630 | I%0 | OTR DR | OUTPUT DATA |
| 1776 | 07251 | 103730 | | STC DR,C | START TRANSFER |
| 1777 | 07252 | 102230 | I%0.0 | SFC DR | DATA READY? |
| 1778 | 07253 | 027261 | | JMP I%0.1 | YES |
| 1779 | 07254 | 102532 | | LIA STS | CHECK IF BREAK WAS ENTERED |
| 1780 | 07255 | 001200 | | RAL | IT'S BIT 14 OF STATUS |
| 1781 | 07256 | 002020 | | SSA | |
| 1782 | 07257 | 026206 | | JMP PRST | IT WAS HIT |
| 1783 | 07260 | 027252 | | JMP I%0.0 | |
| 1784 | 07261 | 102530 | I%0.1 | LIA DR | GET DATA |
| 1785 | 07262 | 127750 | | JMP I.O,I | RETURN |

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|-------|-------|--------|-------|-------------|---------------------------------|
| 1787 | 07263 | 102102 | RP%SC | STF 2 | TURN OFF GLOBAL REGISTER |
| 1788 | 07264 | 002400 | | CLA | |
| 1789 | 07265 | 102602 | | OTA 2 | TURN OFF DIAGNOSE MODE |
| 1790 | 07266 | 102501 | | LIA CPUST | GET COMPUTER STATUS |
| 1791 | 07267 | 001710 | | ALF,SLA | CHECK WHICH VCP SC |
| 1792 | 07270 | 027273 | | JMP **+3 | |
| 1793 | 07271 | 063410 | | LDA .20 | STANDARD SO 20 |
| 1794 | 07272 | 027274 | | JMP **+2 | |
| 1795 | 07273 | 063412 | | LDA .24 | ALTERNATE (DS) |
| 1796 | 07274 | 103602 | | OTA 2,C | LOAD AND ENABLE GLOBAL REGISTER |
| 1797 | 07275 | 127743 | | JMP RP.SC,I | RETURN |
| 1798* | | | | | |
| 1799 | 07276 | 106501 | CS%TR | LIB CPUST | CHECK IF DS |
| 1800 | 07277 | 005710 | | BLF,SLB | |
| 1801 | 07300 | 002001 | | RSS | |
| 1802 | 07301 | 127744 | | JMP CS.TR,I | NO JUST RETURN |
| 1803 | 07302 | 001727 | | ALF,ALF | PUT REQUEST IN UPPER BYTE |
| 1804 | 07303 | 033423 | | IOR .377 | ADD RUB OUT |
| 1805 | 07304 | 017751 | | JSB OUT2C | |
| 1806 | 07305 | 017745 | | JSB CS.CM | TELL CARD TO TRANSMITT |
| 1807 | 07306 | 060400 | | OCT 60400 | |
| 1808 | 07307 | 017745 | | JSB CS.CM | NOW ASK FOR A BUFFER |
| 1809 | 07310 | 061400 | | OCT 61400 | |
| 1810 | 07311 | 127744 | | JMP CS.TR,I | RETURN |
| 1811* | | | | | |
| 1812 | 07312 | 067745 | CS%CM | LDB CS.CM | GET COMMAND |
| 1813 | 07313 | 160001 | | LDA R,I | |
| 1814 | 07314 | 064000 | | LDB A | |
| 1815 | 07315 | 017750 | | JSB I.O | |
| 1816 | 07316 | 037745 | | ISZ CS.CM | |
| 1817 | 07317 | 064000 | | LDB A | |
| 1818 | 07320 | 127745 | | JMP CS.CM,I | |
| 1819* | | | | | |
| 1820 | 07321 | 102630 | CS%FT | OTA DR | |
| 1821 | 07322 | 103730 | | STC DR,C | |
| 1822 | 07323 | 063442 | | LDA .N64 | GET TIME OUT |
| 1823 | 07324 | 102230 | | SFC DR | |
| 1824 | 07325 | 027333 | | JMP **+6 | |
| 1825 | 07326 | 034001 | | ISZ B | |
| 1826 | 07327 | 027324 | | JMP *-3 | |
| 1827 | 07330 | 034000 | | ISZ A | |
| 1828 | 07331 | 027324 | | JMP *-5 | |
| 1829 | 07332 | 127746 | | JMP CS.FT,I | RETURN TIME OUT |
| 1830 | 07333 | 037746 | | ISZ CS.FT | NO SKIP TIME OUT |
| 1831 | 07334 | 127746 | | JMP CS.FT,I | |

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1833* CONSTANTS

1834*

| | | | | | |
|-------|-------|--------|-------|-----|--------|
| 1835 | 07335 | 002400 | TCCWI | OCT | 002400 |
| 1836 | 07336 | 001000 | TCCWO | OCT | 001000 |
| 1837* | | | | | |
| 1838 | 07337 | 007340 | DFL | DEF | **+1 |
| 1839 | 07340 | 000120 | SP | OCT | 120 |
| 1840 | 07341 | 000101 | SA | OCT | 101 |
| 1841 | 07342 | 000102 | SB | OCT | 102 |
| 1842 | 07343 | 000115 | SM | OCT | 115 |
| 1843 | 07344 | | DFL. | EQU | * |
| 1844 | 07344 | 000124 | ST | OCT | 124 |
| 1845 | 07345 | 000107 | SG | OCT | 107 |
| 1846 | 07346 | 000105 | SE | OCT | 105 |
| 1847 | 07347 | 000117 | SO | OCT | 117 |
| 1848 | 07350 | 000111 | SI | OCT | 111 |
| 1849 | 07351 | 000113 | SK | OCT | 113 |
| 1850 | 07352 | 000103 | SC | OCT | 103 |
| 1851 | 07353 | 000104 | SD | OCT | 104 |
| 1852 | 07354 | 000114 | SL | OCT | 114 |
| 1853 | 07355 | 000116 | SN | OCT | 116 |
| 1854 | 07356 | 000125 | SU | OCT | 125 |
| 1855 | 07357 | 000122 | SR | OCT | 122 |
| 1856 | 07360 | 000123 | SS | OCT | 123 |
| 1857 | 07361 | 000126 | SV | OCT | 126 |
| 1858 | 07362 | 000127 | SW | OCT | 127 |
| 1859 | 07363 | 000045 | \$% | OCT | 45 |
| 1860 | 07364 | 051060 | \$R0 | ASC | 1,R0 |
| 1861 | 07365 | 051061 | \$R1 | ASC | 1,R1 |
| 1862 | 07366 | 051062 | \$R2 | ASC | 1,R2 |
| 1863 | 07367 | 051063 | \$R3 | ASC | 1,R3 |
| 1864 | 07370 | 051104 | \$RD | ASC | 1,RD |
| 1865 | 07371 | 051103 | \$RC | ASC | 1,RC |
| 1866 | 07372 | 051123 | \$RS | ASC | 1,RS |
| 1867 | 07373 | 051111 | \$RI | ASC | 1,RI |
| 1868 | 07374 | 051130 | \$RX | ASC | 1,RX |
| 1869 | 07375 | 051106 | \$RF | ASC | 1,RF |
| 1870* | | | | | |
| 1871 | 07376 | 046103 | \$LC | ASC | 1,LC |
| 1872 | 07377 | 042522 | \$EP | ASC | 1,EP |
| 1873 | 07400 | 020477 | \$!? | ASC | 1,!? |
| 1874 | 07401 | 051115 | \$RM | ASC | 1,PM |

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1876 07402 000001 .1 OCT 1
1877 07403 000002 .2 OCT 2
1878 07404 000207 .207 OCT 207
1879 07405 000007 .7 OCT 7
1880 07406 000015 .15 OCT 15
1881 07407 000017 .17 OCT 17
1882 07410 000020 .20 OCT 20
1883 07411 000021 .21 OCT 21
1884 07412 000024 .24 OCT 24
1885 07413 000040 .40 OCT 40
1886 07414 000060 .60 OCT 60
1887 07415 006412 .6412 OCT 6412
1888 07416 000077 .77 OCT 77
1889 07417 000100 .100 OCT 100
1890 07420 000140 .140 OCT 140
1891 07421 000170 .170 OCT 170
1892 07422 000177 .177 OCT 177
1893 07423 000377 .377 OCT 377
1894 07424 000604 .604 OCT 604
1895 07425 001000 .1000 OCT 1000
1896 07426 002100 .2100 OCT 2100
1897 07427 001777 .1777 OCT 1777
1898 07430 001700 .1700 OCT 1700
1899 07431 060000 .60K OCT 60000
1900 07432 076000 .76K OCT 76000
1901 07433 077777 .77NK OCT 77777
1902 07434 100000 .100K OCT 100000
1903 07435 177777 .M1 OCT -1
1904 07436 177772 .M6 OCT -6
1905 07437 177766 .M12 OCT -12
1906 07440 177760 .M20 OCT -20
1907 07441 177754 .N20 DEC -20
1908 07442 177700 .N64 DEC -64

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1909*

1910 07443 EOP1 EQU * END OF PAGE 1

1911*

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1912 07743 ORG 7743R
1913 00300 RAP1 EQU *-EOP1
1914 07743 000000 RP.SC NOP
1915 07744 027263 CS.TR JMP RP%SC
1916 07745 027276 CS.CM JMP CS%TR
1917 07746 027312 CS.FT JMP CS%CM
1918 07747 027321 IN1C JMP CS%FT
1919 07750 027201 I.O JMP IN1C%
1920 07751 027250 OUT2C JMP I%O
1921 07752 027223 OUT1C JMP OU%2C
1922 07753 027232 OUT.N JMP OU%1C
1923 07754 027160 IN.N JMP OUT%N
1924 07755 027131 P1ERR JMP IN%N
1925 07756 000000 NOP
1926 07757 000000 NOP

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REMAINING AREA FOR PAGE 1

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1928*      CROSS OVER TO LOWER PAGE
1929*
1930 07760 063424 CRSP3 LDA .604
1931 07761 102601      OTA CPUST
1932 07762 026372      JMP LDPTN      RETURN FROM LOADER
1933*
1934*      VCP BREAK ENTRY POINT (SAME ON ALL PAGES)
1935*
1936 07763 103105      CLF 5          INSURE PARITY SENSE
1937 07764 106713      CLC 13B       DISABLE MEMORY MAPS
1938 07765 103300      OCT 103300     SFS 0,C CHECK INTERRUPTS
1939 07766 027772      JMP *+4      THERE OFF
1940 07767 073772      STA P1.A     SAVE THE A REG.
1941 07770 003400      CCA          INDICATE INTS ON
1942 07771 027774      JMP *+3
1943 07772 073772      STA P1.A
1944 07773 002400      CLA
1945 07774 073764      STA P1.I
1946 07775 063404      LDA .207     INSURE UPPER PAGE
1947 07776 102601      OTA CPUST
1948 07777 026011      JMP VCP      CONTINUE FRONT PANNEL ROUTINE
1949*
1950*      COMMON STORAGE
1951*
1952 07777      P1.CT EQU 1777B+P1
1953 07776      P1.T3 EQU 1776B+P1
1954 07775      P1.T2 EQU 1775B+P1
1955 07774      P1.T1 EQU 1774B+P1
1956 07773      P1.T0 EQU 1773B+P1
1957 07772      P1.A  EQU 1772B+P1
1958 07771      P1.B  EQU 1771B+P1
1959 07770      P1.E  EQU 1770B+P1
1960 07767      P1.O  EQU 1767B+P1
1961 07766      P1.GF EQU 1766B+P1
1962 07765      P1.M  EQU 1765B+P1
1963 07764      P1.I  EQU 1764B+P1
1964 07763      P1.EM EQU 1763B+P1
1965 07762      P1.DF EQU 1762B+P1
1966 07761      P1.UN EQU 1761B+P1
1967 07760      P1.FL EQU 1760B+P1
1968 07757      P1.SR EQU 1757B+P1
1969 07756      P1.SC EQU 1756B+P1

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|-------|--------------|----|--|-----------------------------------|
| 1971 | 10000 | | ORG 10000B | |
| 1972 | 10000 | P2 | EGU * | PAGE 2 REFERENCE |
| 1973* | | | | |
| 1974* | | | CONTINUATION LOAD | |
| 1975* | | | | |
| 1976* | | | RAM USER CODE MUST SET GLOBAL REGISTER | |
| 1977* | | | | |
| 1978* | LDA 400B | | SET CORRECT PAGE | |
| 1979* | OTA 1 | | FOR CONTINUATION LOAD | |
| 1980* | CLA,INA(CCE) | | INDICATE DISC CALL BACK + SUSPEND | |
| 1981* | CLC 2 | | ENABLE ROM | |
| 1982* | JSB 1 | | GO TO DRIVER | |
| 1983* | ... | | HPIB BUS ADDRESS | |
| 1984* | ... | | DEVICE UNIT NO. (HEAD FOR 7906) | |
| 1985* | ... | | ABSOLUTE STARTING SECTOR | |
| 1986* | ... | | CYLINDER OFFSET | |
| 1987* | | | | |
| 1988 | 10000 000000 | | NOP | |
| 1989 | 10001 000000 | | NOP | |
| 1990 | 10002 107700 | | CLC 0,C | TURN OFF THE WORLD |
| 1991 | 10003 103102 | | CLF 2 | RE ENABLE GLOBAL REGISTER |
| 1992 | 10004 000000 | | NOP | IGNORE POWER FAIL |
| 1993 | 10005 000000 | | NOP | IGNORE IBG |
| 1994 | 10006 000000 | | NOP | IGNORE PARITY ERRORS |
| 1995 | 10007 000000 | | NOP | IGNORE MEMORY PROTECT |
| 1996 | 10010 000000 | | NOP | IGNORE UNIMPLEMENTED INST. |
| 1997* | | | | |
| 1998 | 10011 053104 | | CPA #1 | IS THIS A DISC CALL BACK |
| 1999 | 10012 026015 | | JMP *+3 | |
| 2000 | 10013 102702 | | STC 2 | NO RETURN TO CALLER |
| 2001 | 10014 124001 | | JMP B,I | |
| 2002* | | | | |
| 2003 | 10015 063140 | | LDA #404 | SET LEDS |
| 2004 | 10016 102601 | | OTA CPUST | |
| 2005 | 10017 060001 | | LDA B | |
| 2006 | 10020 164000 | | LDB A,I | GET BUS ADDRESS |
| 2007 | 10021 077757 | | STB P2.SB | SAVE IT |
| 2008 | 10022 002004 | | INA | |
| 2009 | 10023 164000 | | LDB A,I | GET UNIT NO. |
| 2010 | 10024 077761 | | STB P2.UN | SAVE IT |
| 2011 | 10025 002004 | | INA | |
| 2012 | 10026 164000 | | LDB A,I | GET ABSOLUTE SECTOR COUNT |
| 2013 | 10027 077760 | | STB P2.FL | SAVE IT |
| 2014 | 10030 002004 | | INA | |
| 2015 | 10031 164000 | | LDB A,I | GET CYLINDER OFFSET |
| 2016 | 10032 077741 | | STB P2C+1 | SAVE IT |
| 2017 | 10033 002400 | | CLA | |
| 2018 | 10034 073773 | | STA P2.T0 | NO WRITE |
| 2019 | 10035 073775 | | STA P2.T2 | AUTO EXECUTE (NOT VCP) |
| 2020 | 10036 002004 | | INA | |
| 2021 | 10037 073762 | | STA P2.DF | CLEAR SUSPEND FLAG INDICATE CONT. |
| 2022 | 10040 003440 | | CCA,SEZ | NO RETRIES (SUSPEND REQUEST?) |
| 2023 | 10041 073762 | | STA P2.DF | SET SUSPEND FLAG |
| 2024 | 10042 073777 | | STA P2.CT | |
| 2025 | 10043 026064 | | JMP DCLD1 | EXECUTE LOADER |

| | | | | | |
|-------|----------------------|--------|-------|-----------|-----------------------------------|
| 2027 | 10044 | 060001 | LDP2 | LDA B | CHANGE HANDS |
| 2028 | 10045 | 053104 | | CPA #1 | DISC LOADER |
| 2029 | 10046 | 026052 | | JMP DCLD. | YES |
| 2030 | 10047 | 002404 | | CLA,INA | NO DEVICE |
| 2031 | 10050 | 073755 | | STA P2ERR | |
| 2032 | 10051 | 027757 | | JMP RTNP3 | NONE OF THE ABOVE SO ERROR |
| | | | | | |
| 2034* | HP-IB DISC LOADER | | | | |
| 2035* | | | | | |
| 2036 | 10052 | 063152 | DCLD. | LDA @M40 | SET RETRY COUNTER |
| 2037 | 10053 | 067775 | | LDB P2.T2 | CHECK IF VCP |
| 2038 | 10054 | 006002 | | SZB | IF IT IS FROM VCP THEN |
| 2039 | 10055 | 063145 | | LDA @M2 | ALLOW ONE RETRY |
| 2040 | 10056 | 073777 | | STA P2.CT | |
| 2041* | | | | | |
| 2042 | 10057 | 067760 | | LDB P2.FL | MPY FILE BY 256 |
| 2043 | 10060 | 005727 | | BLF,RLF | |
| 2044 | 10061 | 077760 | | STB P2.FL | |
| 2045 | 10062 | 002400 | | CLA | CLEAR CYLINDER OFFSET |
| 2046 | 10063 | 073741 | | STA P2C+1 | |
| 2047 | 10064 | 017752 | DCLD1 | JSB DCFR | SET ERROR RETURN ADDRESS |
| 2048 | 10065 | 026324 | | JMP DCERX | |
| 2049 | 10066 | 017742 | | JSB DC.IN | INITIALIZE AND GET DISC TYPE |
| 2050* | | | | | |
| 2051* | DETERMINE IF L OR XL | | | | |
| 2052* | | | | | |
| 2053 | 10067 | 067742 | | LDB DC.IN | SETUP PAGE |
| 2054 | 10070 | 060001 | | LDA B | CHECK FOR PAGE |
| 2055 | 10071 | 013142 | | AND @76K | ONLY UPPER ADDRESS |
| 2056 | 10072 | 002003 | | SZA,RSS | |
| 2057 | 10073 | 026106 | | JMP DCLMP | NEW MAPPED |
| 2058 | 10074 | 023142 | | XOR @76K | MAKE COUNT |
| 2059 | 10075 | 033112 | | IOR @100 | AND DO A 32K-64 WORD TRANSFER |
| 2060 | 10076 | 067743 | | LDB DC.RW | OLD SYSTEM SO CHANGE CYLINDER NO. |
| 2061 | 10077 | 077754 | | STB P2.HC | |
| 2062 | 10100 | 006700 | | CLB,CCE | AND CLEAR HEAD SECTOR |
| 2063 | 10101 | 077753 | | STB P2.ST | |
| 2064 | 10102 | 005500 | DCLD2 | ERB | SET BIT 15 FOR NON MAPPED |
| 2065 | 10103 | 017743 | | JSB DC.RW | READ OR WRITE DATA |
| 2066 | 10104 | 073755 | | STA P2ERR | CLEAR ERROR |
| 2067 | 10105 | 027757 | | JMP RTNP3 | RETURN TO PAGE 3 |

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|------|-------|--------|-----------------|------------------------------------|
| 2069 | 10106 | 067773 | DCLMP LDR P2.T0 | CHECK IF READ OR WRITE |
| 2070 | 10107 | 060001 | LDA B | |
| 2071 | 10110 | 053156 | CPA \$2W | IF W WAS ENTERED THEN WRITE |
| 2072 | 10111 | 026113 | JMP **2 | |
| 2073 | 10112 | 026147 | JMP DCLM. | |
| 2074 | 10113 | 064101 | LDB 101B | SAVE MAP LOCATION |
| 2075 | 10114 | 106624 | OTB 24B | IN THE I/O CHIP |
| 2076 | 10115 | 002400 | CLA | |
| 2077 | 10116 | 070101 | STA 101B | |
| 2078 | 10117 | 067772 | LDB P2.A | GET A REGISTER DATA |
| 2079 | 10120 | 102711 | STC 11B | FNABLE MAPS |
| 2080 | 10121 | 026122 | JMP **1 | TURN THEM ON |
| 2081 | 10122 | 063121 | LDA @2000 | GO TO MAPPED PAGE |
| 2082 | 10123 | 174000 | STB A,I | |
| 2083 | 10124 | 002004 | INA | |
| 2084 | 10125 | 106713 | CLC 13B | DISABLE MAPS |
| 2085 | 10126 | 067771 | LDB P2.B | |
| 2086 | 10127 | 102713 | STC 13B | RE ENABLE MAPS |
| 2087 | 10130 | 174000 | STB A,I | |
| 2088 | 10131 | 106711 | CLC 11B | |
| 2089 | 10132 | 026133 | JMP **1 | |
| 2090 | 10133 | 106524 | LIB 24B | RESTOR MAP REG. |
| 2091 | 10134 | 074101 | STB 101B | |
| 2092 | 10135 | 067772 | LDB P2.A | CHECK IF MAPPED WRITE OR OLD STYLE |
| 2093 | 10136 | 006020 | SSB | |
| 2094 | 10137 | 026251 | JMP DCLMW | OLD STYLE |
| 2095 | 10140 | 060001 | LDA B | |
| 2096 | 10141 | 067771 | LDB P2.B | |
| 2097 | 10142 | 006002 | SZB | COUNT PARTIAL |
| 2098 | 10143 | 002004 | INA | |
| 2099 | 10144 | 043150 | ADA @M11 | |
| 2100 | 10145 | 002021 | SSA,RSS | OVER 8? |
| 2101 | 10146 | 026251 | JMP DCLMW | YES THEN OLD STYLE |

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|------|-------|--------|----------------|---------------------------------------|
| 2103 | 10147 | 063067 | DCLM. LDA TR1K | GET COUNT FOR 1K -64 |
| 2104 | 10150 | 006700 | CLB, CCF | NON MAPPED |
| 2105 | 10151 | 005500 | ERB | |
| 2106 | 10152 | 017743 | JSB DC.RW | NOW READ IT |
| 2107 | 10153 | 003400 | CCA | NO MORE RETRIES |
| 2108 | 10154 | 073777 | STA P2.CT | |
| 2109 | 10155 | 067760 | LDB P2.FL | ADD 8 SECTRS |
| 2110 | 10156 | 060001 | LDA B | |
| 2111 | 10157 | 043111 | ADA @10 | |
| 2112 | 10160 | 073760 | STA P2.FL | |
| 2113 | 10161 | 017742 | JSB DC.IN | REEINITIALIZE BUSS |
| 2114 | 10162 | 067760 | LDB P2.FL | MOVE FILE COUNT BACK |
| 2115 | 10163 | 060001 | LDA B | |
| 2116 | 10164 | 043147 | ADA @M10 | |
| 2117 | 10165 | 073760 | STA P2.FL | |
| 2118 | 10166 | 063070 | LDA TR31K | COUNT FOR 31K TRANSFER |
| 2119 | 10167 | 064000 | LDB A | |
| 2120 | 10170 | 017743 | JSB DC.RW | READ IT |
| 2121 | 10171 | 064101 | LDB 101B | SAVE MAP |
| 2122 | 10172 | 077743 | STB DC.RW | |
| 2123 | 10173 | 002400 | CLA | |
| 2124 | 10174 | 070101 | STA 101B | MAP PAGE 1 TO PAGE 0 |
| 2125 | 10175 | 102711 | STC 11B | TURN ON MAPPING |
| 2126 | 10176 | 026177 | JMP *+1 | ENABLE THEM |
| 2127 | 10177 | 063122 | LDA @2101 | TRY MAPPING INCASE XL BOOT AND L MEM. |
| 2128 | 10200 | 007400 | CCB | |
| 2129 | 10201 | 174000 | STB A,I | |
| 2130 | 10202 | 063121 | LDA @2000 | |
| 2131 | 10203 | 164000 | LDB A,I | SHOULD GET PHY. LOC. 0 |
| 2132 | 10204 | 101100 | RRR 16 | SWAPP A & B |
| 2133 | 10205 | 006004 | INB | MOVE TO PHY. LOC. 1 |
| 2134 | 10206 | 164001 | LDB B,I | |
| 2135 | 10207 | 106711 | CLC 11B | TURN MAPS OFF |
| 2136 | 10210 | 026211 | JMP *+1 | |
| 2137 | 10211 | 034101 | ISZ 101B | DID IT STORE |
| 2138 | 10212 | 026224 | JMP DCLMU | NO THEN XL BOOTX ON L MEMORY |
| 2139 | 10213 | 073772 | STA P2.A | SAVE A & B |
| 2140 | 10214 | 077771 | STB P2.B | |

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|------|-------|--------|-----------------|--------------------------------------|
| 2142 | 10215 | 002021 | SSA,RSS | IS THIS OLD OR NEW? |
| 2143 | 10216 | 026255 | JMP DCLM1 | NEW |
| 2144 | 10217 | 106501 | DCLM0 LIB CPUST | CHECK IF MEMLOST IS UP |
| 2145 | 10220 | 005600 | ELB | |
| 2146 | 10221 | 063131 | LDA @40 | THEN |
| 2147 | 10222 | 006020 | SSR | |
| 2148 | 10223 | 026322 | JMP DCLMX+1 | CAN'T LOAD |
| 2149 | 10224 | 063136 | DCLMU LDA @1700 | OK THEN MOVE SAVE AREA |
| 2150 | 10225 | 073742 | STA DC.IN | USE AS STORAGE |
| 2151 | 10226 | 033142 | IOR @76K | AND EXECUTION TO LAST PAGE |
| 2152 | 10227 | 167742 | LDB DC.IN,I | |
| 2153 | 10230 | 174000 | STB A,I | |
| 2154 | 10231 | 037742 | ISZ DC.IN | |
| 2155 | 10232 | 002004 | INA | |
| 2156 | 10233 | 002021 | SSA,RSS | |
| 2157 | 10234 | 026227 | JMP *-5 | |
| 2158 | 10235 | 103503 | LIA 3,C | RESET BREAK ADDRESS |
| 2159 | 10236 | 033142 | IOR @76K | |
| 2160 | 10237 | 103603 | OTA 3,C | |
| 2161 | 10240 | 063142 | LDA @76K | NOW MOVE EXECUTION TO THAT ADDRESS |
| 2162 | 10241 | 032243 | IOR *+2 | |
| 2163 | 10242 | 124000 | JMP A,I | |
| 2164 | 10243 | 000244 | DEF *+1-P2 | |
| 2165 | 10244 | 063142 | LDA @76K | UPDATE STRING POINTER |
| 2166 | 10245 | 067762 | LDB P2.DF | |
| 2167 | 10246 | 006002 | SZB | IF NOT ZERO |
| 2168 | 10247 | 044000 | ADB A | |
| 2169 | 10250 | 077762 | STB P2.DF | |
| 2170 | 10251 | 017742 | DCLMW JSB DC.IN | RE INITIALIZE BUS |
| 2171 | 10252 | 063112 | LDA @100 | DO 32K - 64 WORDS |
| 2172 | 10253 | 006700 | CLB,CCE | SET FOR NORMAL DMA TRANSFER |
| 2173 | 10254 | 026102 | JMP DCLD2 | GO DO IT |
| 2174 | 10255 | 067743 | DCLM1 LDB DC.RW | RESTORE MAP LOCATION |
| 2175 | 10256 | 074101 | STB 101B | |
| 2176 | 10257 | 002003 | SZA,RSS | ANY MORE BLOCKS? |
| 2177 | 10260 | 026321 | JMP DCLMX | NO |
| 2178 | 10261 | 067771 | LDB P2.B | RESTORE B REG |
| 2179 | 10262 | 006002 | SZB | MUST BE A MAPPED FILE |
| 2180 | 10263 | 002004 | INA | IF PARTIAL THEN DO ONE MORE FULL ONE |
| 2181 | 10264 | 043144 | ADA @M1 | MOVE IT BACK ONE |
| 2182 | 10265 | 070001 | STA R | |
| 2183 | 10266 | 043147 | ADA @M10 | CHECK IF OLD GENERATOR TYPE |
| 2184 | 10267 | 002021 | SSA,RSS | IF OVER 8 |
| 2185 | 10270 | 026217 | JMP DCLM0 | YES THEN MOVE TO OTHER PAGE |

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|-------|----------------|--------|-------|------------|----------------------------|
| 2187 | 10271 | 002400 | | CLA | |
| 2188 | 10272 | 073740 | | STA P2C | CLEAR MAP POINTER |
| 2189 | 10273 | 060001 | | LDA B | RESTORE A REG. |
| 2190 | 10274 | 043144 | DCLM2 | ADA @M1 | |
| 2191 | 10275 | 002020 | | SSA | |
| 2192 | 10276 | 026321 | | JMP DCLMX | |
| 2193 | 10277 | 102624 | | OTA 24R | SAVE BLOCK COUNT |
| 2194 | 10300 | 102525 | | LIA 25B | SET NEXT FILE NUMBER |
| 2195 | 10301 | 002004 | | INA | |
| 2196 | 10302 | 102625 | | OTA 25B | MOVED TO NEXT FILE |
| 2197 | 10303 | 067760 | | LDB P2.FL | POINT TO NEXT FILE AREA |
| 2198 | 10304 | 060001 | | LDA B | |
| 2199 | 10305 | 043066 | | ADA @D256 | |
| 2200 | 10306 | 073760 | | STA P2.FL | |
| 2201 | 10307 | 017742 | | JSB DC.IN | SET UP BUS |
| 2202 | 10310 | 067740 | | LDB P2C | UPDATE MAPE POINTER |
| 2203 | 10311 | 060001 | | LDA B | |
| 2204 | 10312 | 043131 | | ADA @40 | NEXT 32K BLOCK |
| 2205 | 10313 | 073740 | | STA P2C | SAVE IT |
| 2206 | 10314 | 070001 | | STA B | AND PASS IT AS A PARAMETER |
| 2207 | 10315 | 002400 | | CLA | |
| 2208 | 10316 | 017743 | | JSB DC.RW | READ DATA |
| 2209 | 10317 | 102524 | | LIA 24R | CHECK IF DONE |
| 2210 | 10320 | 026274 | | JMP DCLM2 | |
| 2211 | 10321 | 002400 | DCLMX | CLA | |
| 2212 | 10322 | 073755 | | STA P2FRR | |
| 2213 | 10323 | 027757 | | JMP RTNP3 | |
| 2214* | | | | | |
| 2215* | | | | | |
| 2216 | 10324 | 067755 | DCERX | LDB P2ERR | SAVE CURRENT ERROR |
| 2217 | 10325 | 063111 | | LDA @10 | START ALL OVER |
| 2218 | 10326 | 073755 | | STA P2ERP | |
| 2219 | 10327 | 037777 | | ISZ P2.CT | CHECK IF RETRY |
| 2220 | 10330 | 026064 | | JMP DCLD1 | YES |
| 2221 | 10331 | 077755 | | STB P2ERR | RESTOR ERROR |
| 2222 | 10332 | 027757 | | JMP RTNP3 | RETURN TO PAGE 3 |
| 2223* | | | | | |
| 2224* | INITIALIZE BUS | | | | |
| 2225* | | | | | |
| 2226 | 10333 | 063111 | DC%IN | LDA @10 | SET ERROR 10 |
| 2227 | 10334 | 073755 | | STA P2ERR | |
| 2228 | 10335 | 017747 | | JSB PHI | |
| 2229 | 10336 | 070200 | | OCT 070200 | PHI ON-LINE |
| 2230 | 10337 | 017747 | | JSB PHI | |
| 2231 | 10340 | 060063 | | OCT 060063 | REN,IFC,WRITE,FLUSH FIFO |
| 2232 | 10341 | 063065 | | LDA N250 | ABOUT A 1 MILLISEC DELAY |
| 2233 | 10342 | 002006 | | INA,SZA | |
| 2234 | 10343 | 026342 | | JMP *-1 | |
| 2235 | 10344 | 073776 | | STA P2.T3 | CLEAR HEAD NUMBER |
| 2236 | 10345 | 017751 | | JSB PHIFL | FLUSH PHI FIFO'S |

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2238*      READ AND SET DISC TYPE
2239*
2240  10346 037755      ISZ P2ERR      SET ERROR 11
2241  10347 017745      JSB PHI.L      TELL PHI TO LISTEN WITH
2242  10350 000537      OCT 537      A SECONDARY OF UNTALK
2243  10351 067757      LDB P2.SB    BUILD SECONDARY WITH HPIB ADD
2244  10352 060001      LDA B
2245  10353 033071      TOR TLK
2246  10354 033072      TOR LSN
2247  10355 017750      JSB HPIB
2248  10356 017747      JSB PHI
2249  10357 001002      OCT 1002
2250  10360 017746      JSB PHI.I    GET DISC TYPE
2251  10361 001727      ALF,ALF
2252  10362 073745      STA PHI.L    SAVE DATA
2253  10363 017746      JSB PHI.I
2254  10364 067745      LDB PHI.L    ADD PREVIOUS BYTE
2255  10365 044000      ADB A
2256  10366 077743      STB DC.RW    SAVE DISC TYPE
2257*
2258*      DO A UNIVERSAL DEVICE CLEAR AND
2259*      READ STATUS
2260*
2261  10367 037755      ISZ P2ERR    SET ERROR 12
2262  10370 017744      JSB PHI.T    PHI TALK
2263  10371 000424      OCT 424     UNIVERSAL DEVICE CLEAR
2264  10372 017744      JSB PHI.T    PHI TLK
2265  10373 000550      OCT 550
2266  10374 017747      JSB PHI
2267  10375 000003      OCT 3       READ STATUS
2268  10376 067761      LDB P2.UN
2269  10377 060001      LDA B
2270  10400 033113      TOR BIT9    ADD BIT9
2271  10401 017750      JSB HPIB    PASS IT TO CARD
2272  10402 017745      JSB PHI.L    PHI LSN
2273  10403 000550      OCT 550
2274  10404 017747      JSB PHI
2275  10405 001003      OCT 1003    TRANSFER 3 BYTES
2276  10406 017746      JSB PHI.I    GET BYTE
2277  10407 037755      ISZ P2ERR    SET ERROR 13
2278  10410 002002      SZA         CHECK FOR FRROR
2279  10411 127752      JMP DCER,I   YES RETURN WITH AN ERROR
2280  10412 017746      JSB PHI.I    SKIP NEXT BYTE
2281  10413 017746      JSB PHI.I    READ DISC TYPE
2282  10414 001300      RAR         ELIMINATE BIT 0
2283  10415 013126      AND @17     USE 4 BITS FOR ID
2284  10416 073751      STA PHIFL   SAVE FOR CONVERSION

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2286*      TAKE DISC TYPE AND CONVERT TO DISC PARAMETERS
2287*
2288 10417 063075      LDA DCTYP      GET POINTER TO DISC TYPE
2289 10420 073745      STA PHI.L
2290 10421 067743      LDB DC.RW      RETRIEVE DISC TYPE
2291 10422 060001      LDA B
2292 10423 053117      CPA @204      MINI FLOPPY?
2293 10424 026471      JMP DTYPE      YES
2294 10425 037745      ISZ PHI.L      NO MOVE TO NEXT TYPE
2295 10426 053116      CPA @201      88020 FLOPPY
2296 10427 026471      JMP DTYPE
2297 10430 037745      ISZ PHI.L
2298 10431 053104      CPA @1        7910 FIXED DISC
2299 10432 026471      JMP DTYPE
2300 10433 037745      ISZ PHI.L      MOVE TO NEXT ENTRY
2301 10434 053106      CPA @3        INTEGRATED DISC CONTROLLER?
2302 10435 026443      JMP *+6       YES
2303 10436 063132      DTYER LDA @60  DISC NOT IDENTIFIED
2304 10437 067760      LDB P2.FL     CHECK IF FILE NO. IS ZERO
2305 10440 006002      SZB          IF SO THEN GO AHEAD
2306 10441 026322      JMP DCLMX+1   NO RETURN ERROR
2307 10442 026457      JMP DCFM      USE CYLINDER MODE
2308 10443 067751      LDB PHIFL    GET ID FROM CONTROLLER
2309 10444 060001      LDA B
2310 10445 053104      CPA @1        7920?
2311 10446 026457      JMP DCFM      YES DO FILE MASK FIRST
2312 10447 037745      ISZ PHI.L
2313 10450 053106      CPA @3        7925?
2314 10451 026457      JMP DCFM      YES DO A FILE MASK FIRST
2315 10452 037745      ISZ PHI.L
2316 10453 002002      SZA          7906?
2317 10454 026436      JMP DTYER
2318 10455 007400      CCB
2319 10456 077776      STB P2.T3    INDICATE UNIT = HEAD
2320*
2321*      SEND FILE MASK
2322*
2323 10457 037755      DCFM ISZ P2ERR  SET ERROR 14
2324 10460 017744      JSB PHI.T     SEND FILE MASK TO 7906
2325 10461 000550      OCT 550
2326 10462 017747      JSB PHI
2327 10463 000017      OCT 17        SET FILE MASK
2328 10464 063114      LDA @1005     ENABLE AUTO TRACK INCREMENT AND SPARING
2329 10465 067776      LDB P2.T3     IS THIS A 7906?
2330 10466 006003      SZB,RSS
2331 10467 033105      IOR @2        NO THEN CYLINDER MODE
2332 10470 017750      JSB HPIB

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2334*      CONVERT FILE NO. TO CYLINDER-HEAD-SECTOR
2335*
2336 10471 067745  DTYPE LDB PHI.L      GET POINTER
2337 10472 160001      LDA B,I      SET NO. OF SECTRS PER TRACK
2338 10473 013135      AND @377     GET SECTRS PER TRACK
2339 10474 003004      CMA,INA     MAKE IT NEG
2340 10475 073753      STA P2.ST    SAVE IT
2341 10476 160001      LDA B,I      SET NO. OF HEADS PER CYLINDER
2342 10477 001727      ALF,ALF
2343 10500 013126      AND @17
2344 10501 003004      CMA,INA
2345 10502 073754      STA P2.HC
2346 10503 160001      LDA B,I      SET OLD STYLE OF FILE / CYLINDER
2347 10504 001700      ALF
2348 10505 013126      AND @17
2349 10506 003004      CMA,INA
2350 10507 073774      STA P2.T1    SAVE AS COUNT
2351 10510 067760      LDB P2.FL
2352 10511 101050      LSR 8
2353 10512 002400      CLA
2354 10513 040001      ADA B
2355 10514 037774      ISZ P2.T1
2356 10515 026513      JMP *-2
2357 10516 073743      STA DC.RW    SAVE LODF STYLE
2358 10517 002400      CLA
2359 10520 067760      LDB P2.FL    NOW GET NO SECTRS
2360 10521 077774      STB P2.T1
2361 10522 047753      ADB P2.ST
2362 10523 006020      SSB
2363 10524 026527      JMP *+3
2364 10525 002004      INA
2365 10526 026521      JMP *-5
2366 10527 067774      LDB P2.T1    REMAINDER IS THE SECTOR OFF SET
2367 10530 077753      STB P2.ST    SAVE IT
2368 10531 064000      LDB A        NOW GET NUMBER OF CYLINDERS
2369 10532 002400      CLA
2370 10533 077774      STB P2.T1
2371 10534 047754      ADB P2.HC
2372 10535 006020      SSB
2373 10536 026541      JMP *+3
2374 10537 002004      INA
2375 10540 026533      JMP *-5
2376 10541 073754      STA P2.HC    SAVE CYLINDER
2377 10542 067774      LDB P2.T1    NOW ADD HEAD TO SECTR WORD
2378 10543 005727      RLF,BLF
2379 10544 047753      ADB P2.ST
2380 10545 077753      STB P2.ST
2381 10546 127742      JMP DC.IN,I  NOW RETURN

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2383*      SEEK  READ/WRITE  DSJ
2384*
2385  10547 000066  DC&RW  CLE,ELA      MPY COUNT BY 2 FOR BYTE COUNT
2386  10550 102623          OTA 23B      PASS COUNT TO INTERFACE
2387  10551 103101          CLO          SET READ
2388  10552 060001          LDA B
2389  10553 067773          LDB P2.TO    NOW CHECK IF WRITE
2390  10554 101100          RRR 16
2391  10555 053156          CPA S2W      IS IT A WRITE?
2392  10556 102101          STO          YES
2393  10557 063074          LDA DCDCW   GET DMA CONTROL WORD
2394  10560 006021          SSB,RSS    IS THIS MAPPED
2395  10561 002004          INA          YES USE MAP REGISTER 1
2396  10562 102301          SOS          READ / WRITE
2397  10563 033115          IOR @200   READ
2398  10564 102621          OTA 21P    PASS IT TO DMA
2399  10565 060001          LDA R      STARTING ADDRESS
2400  10566 006021          SSB,RSS    IS THIS ADDRESS OR MAPPED
2401  10567 006400          CLB          MAPPED THEN 0 ADDRESS
2402  10570 106622          OTB 22B
2403  10571 064141          LDB 141B   SAVE MAP CONTENTS
2404  10572 077742          STB DC.IN
2405  10573 106521          LIB 21B   NEED MAPPING?
2406  10574 004010          SLB
2407  10575 070141          STA 141B   YES-NOW SET MAP
2408  10576 063125          LDA @15    SET ERROR 15
2409  10577 073755          STA P2ERR
2410  10600 017744          JSB PHI.T  PHI TLK
2411  10601 000550          OCT 550    SECONDARY
2412  10602 017747          JSB PHI
2413  10603 000002          OCT 2      SEEK
2414  10604 067776          LDB P2.T3  CHECK FOR UNIT HEAD SWAP
2415  10605 060001          LDA B
2416  10606 006400          CLB
2417  10607 002003          SZA,RSS    IS THERE A SWAP
2418  10610 067761          LDR P2.UN  NO - GET UNIT
2419  10611 060001          LDA B
2420  10612 017750          JSB HPIB
2421  10613 067754          LDR P2.HC  SET UPPER CYLINDER
2422  10614 047741          ADB P2C+1  ADD CYLINDER OFFSET
2423  10615 060001          LDA B
2424  10616 001727          ALF,ALF
2425  10617 013135          AND @377
2426  10620 017750          JSB HPIB
2427  10621 067754          LDB P2.HC  GET CYLINDER NUMBER
2428  10622 047741          ADB P2C+1  ADD CYLINDER OFFSET
2429  10623 060001          LDA B      SET LOWER CYLINDER
2430  10624 013135          AND @377
2431  10625 017750          JSB HPIB

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|------|-------|--------|-----------|--------------------------|
| 2433 | 10626 | 067753 | LDB P2.ST | SET HEAD |
| 2434 | 10627 | 060001 | LDA B | |
| 2435 | 10630 | 001727 | ALF,ALF | |
| 2436 | 10631 | 013135 | AND @377 | |
| 2437 | 10632 | 067776 | LDB P2.T3 | CHECK FOR UNIT HEAD SWAP |
| 2438 | 10633 | 006002 | SZB | |
| 2439 | 10634 | 067761 | LDB P2.UN | |
| 2440 | 10635 | 030001 | IOR B | |
| 2441 | 10636 | 017750 | JSB HPIB | |
| 2442 | 10637 | 067753 | LDB P2.ST | SET SECTOR |
| 2443 | 10640 | 060001 | LDA B | |
| 2444 | 10641 | 013135 | AND @377 | |
| 2445 | 10642 | 033113 | IOR BIT9 | SET SECTOR + EOI |
| 2446 | 10643 | 017750 | JSB HPIB | |

2448* READ OR WRITE

2449*

| | | | | |
|------|-------|--------|-----------|-------------------|
| 2450 | 10644 | 037755 | ISZ P2ERR | SET ERROR 16 |
| 2451 | 10645 | 017744 | JSB PHI.T | PHI TLK |
| 2452 | 10646 | 000550 | OCT 550 | SECONDARY |
| 2453 | 10647 | 102201 | SOC | READ OR WRITE? |
| 2454 | 10650 | 026654 | JMP **4 | |
| 2455 | 10651 | 017747 | JSB PHI | |
| 2456 | 10652 | 000005 | OCT 5 | READ |
| 2457 | 10653 | 026656 | JMP **3 | |
| 2458 | 10654 | 017747 | JSB PHI | |
| 2459 | 10655 | 000010 | OCT 10 | WRITE |
| 2460 | 10656 | 067761 | LDB P2.UN | GET UNIT |
| 2461 | 10657 | 060001 | LDA B | |
| 2462 | 10660 | 033113 | IOR BIT9 | ADD EOI |
| 2463 | 10661 | 017750 | JSB HPIB | PASS IT TO CARD |
| 2464 | 10662 | 102301 | SOS | READ OR WRITE? |
| 2465 | 10663 | 026667 | JMP **4 | |
| 2466 | 10664 | 017744 | JSB PHI.T | WRITE |
| 2467 | 10665 | 000540 | OCT 540 | |
| 2468 | 10666 | 026675 | JMP **7 | |
| 2469 | 10667 | 017745 | JSB PHI.L | PHI LSN |
| 2470 | 10670 | 000540 | OCT 540 | SECONDARY |
| 2471 | 10671 | 017747 | JSB PHI | |
| 2472 | 10672 | 001400 | OCT 1400 | UNCOUNTED XFER |
| 2473 | 10673 | 017747 | JSB PHI | |
| 2474 | 10674 | 060040 | OCT 60040 | TELL PHI TO INPUT |

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2476*      SET UP DAM TRANSFER AND START IT
2477*
2478  10675 063073      LDA CMDF      SET PHI FOR DMA INPUT BYTE PACKED
2479  10676 102201      SOC
2480  10677 001665      FLA,CLE,ERA  MAKE IT OUTPUT
2481  10700 102631      OTA CTL
2482  10701 103721      STC 21B,C    START DMA
2483  10702 037755      ISZ P2ERR    SET ERROR 17
2484  10703 063151      LDA @M20
2485  10704 073747      STA PHI      START TIME OUT
2486  10705 034000      DCLO ISZ A
2487  10706 026717      JMP DCSFS
2488  10707 037747      ISZ PHI
2489  10710 026717      JMP DCSFS
2490  10711 107721      CLC 21B,C    SHUT DOWN DMA
2491  10712 067742      LDR DC.IN    RESTORE MAP DATA
2492  10713 102521      LIA 21B      WAS THIS MAPPED
2493  10714 000010      SLA
2494  10715 074141      STB 141B     YES RESTOR 141
2495  10716 127752      JMP DCER,I   TIMED OUT SO ERROR
2496  10717 102323      DCSFS SFS 23B IS IT READY
2497  10720 026705      JMP DCLO     NO CHECK TIME OUT
2498  10721 107721      CLC 21B,C    YES SHUT DOWN THE REST OF DMA
2499  10722 067742      LDR DC.IN    RESTORE MAPP
2500  10723 102521      LIA 21B      WAS THIS MAPPED?
2501  10724 000010      SLA
2502  10725 074141      STB 141B     YES RESTOR 141
2503  10726 037755      ISZ P2ERR    SET ERROR 20
2504  10727 102222      SFC 22B     CHECK FOR PARITY ERROR
2505  10730 127752      JMP DCER,I   YES SO ERROR
2506  10731 037755      ISZ P2ERR    SET ERROR 21
2507  10732 062756      LDA UNL
2508  10733 102201      SOC          ONLY IF IT'S A WRITE
2509  10734 017750      JSB HPIB     YES OUTPUT IT
2510  10735 102301      SOS
2511  10736 017751      JSB PHIFL    FLUSH PHI FIFOS
2512*
2513*  DSJ REQUEST
2514*
2515  10737 037755      ISZ P2ERR    SET ERROR 22
2516  10740 017745      JSB PHI.L    PHI LSN
2517  10741 000560      OCT 560     SECONDARY (DSJ)
2518  10742 017747      JSB PHI
2519  10743 001001      OCT 1001    COUNTED XFER OF 4
2520  10744 017746      JSB PHI.I    GET BYTE
2521  10745 037755      ISZ P2ERR    SET ERROR 23
2522  10746 002002      SZA          WAS THERE AN ERROR
2523  10747 127752      JMP DCER,I   REPORT ERROR
2524  10750 127743      JMP DC.RW,I  RETURN

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2526*      TELL PHI TO TALK AND DISC TO LISTEN
2527*      AND PASS A SECONDARY
2528*
2529 10751 017747  PHI&T JSB PHI
2530 10752 031002      OCT 31002      PHI OUTPUT COMMAND
2531 10753 017747      JSB PHI
2532 10754 000537      OCT 537      UNT
2533 10755 017747      JSB PHI
2534 10756 000477  UNL  OCT 477      UNL
2535 10757 017747      JSB PHI
2536 10760 000536      OCT 536      CTRLR LSN
2537 10761 067757      LDB P2.SB      GET DISC ADDRESS
2538 10762 060001      LDA B
2539 10763 033072      IOR LSN      ADD LISTEN BIT
2540 10764 017750      JSB HPIB
2541 10765 067744      LDB PHI.T
2542 10766 160001      LDA B,I      GET DATA
2543 10767 017750      JSB HPIB      PASS IT TO CARD
2544 10770 037744      ISZ PHI.T      ADJUST RETRUN
2545 10771 127744      JMP PHI.T,I      RETURN
2546*
2547*      TELL PHI TO LISTEN AND DISC TO TALK
2548*      AND PASS A SECONDARY
2549*
2550 10772 017747  PHI&L JSB PHI
2551 10773 031002      OCT 31002      PHI OUTPUT COMMAND
2552 10774 017747      JSB PHI
2553 10775 000537      OCT 537      UNT
2554 10776 017747      JSB PHI
2555 10777 000477      OCT 477      UNL
2556 11000 017747      JSB PHI
2557 11001 000476      OCT 476      CTRLR LSN
2558 11002 067757      LDB P2.SB      GET DISC ADDRESS
2559 11003 060001      LDA B
2560 11004 033071      IOR TLK      ADD TALK BIT
2561 11005 017750      JSB HPIB
2562 11006 067745      LDB PHI.L
2563 11007 160001      LDA B,I      GET DATA
2564 11010 017750      JSB HPIB      PASS IT TO CARD
2565 11011 037745      ISZ PHI.L      ADJUST RETRUN
2566 11012 127745      JMP PHI.L,I      RETURN
2567*
2568 11013 063054  PHI&I LDA PIN      GET INPUT COMMAND
2569 11014 017750      JSB HPIB      PASS IT TO CARD
2570 11015 017747      JSB PHI
2571 11016 100000      OCT 100000    TELL CARD TO INPUT
2572 11017 102530      LIA DR      AND THEN GET DATA
2573 11020 013135      AND @377    MASK OFF UPPER BYTE
2574 11021 127746      JMP PHI.I,I      RETURN

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|-------|-------|--------|-------|-------------|--|
| 2576 | 11022 | 067747 | PHI% | LDR PHI | |
| 2577 | 11023 | 160001 | | LDA B,I | GET DATA |
| 2578 | 11024 | 102630 | | OTA DR | PASS IT TO CARD |
| 2579 | 11025 | 103730 | | STC DR,C | PASS TO PHI |
| 2580 | 11026 | 037747 | | ISZ PHI | ADJUST RETURN |
| 2581 | 11027 | 127747 | | JMP PHI,I | AND RETURN |
| 2582* | | | | | |
| 2583 | 11030 | 102630 | HPTB% | OTA DR | |
| 2584 | 11031 | 103730 | | STC DR,C | |
| 2585 | 11032 | 063145 | | LDA @M2 | WAIT FOR IT |
| 2586 | 11033 | 034001 | | ISZ B | |
| 2587 | 11034 | 027040 | | JMP **+4 | |
| 2588 | 11035 | 034000 | | ISZ A | |
| 2589 | 11036 | 027040 | | JMP **+2 | |
| 2590 | 11037 | 127752 | | JMP DCER,I | WAITED LONG ENOUGH |
| 2591 | 11040 | 102330 | | SFS DR | |
| 2592 | 11041 | 027033 | | JMP *-6 | |
| 2593 | 11042 | 127750 | | JMP HPIB,I | |
| 2594* | | | | | |
| 2595 | 11043 | 063073 | PHIF% | LDA CMDF | ENABLE FLAG |
| 2596 | 11044 | 102631 | | OTA CTL | |
| 2597 | 11045 | 017747 | | JSB PHI | |
| 2598 | 11046 | 060043 | | OCT 60043 | FLUSH OUTBOUND FIFO |
| 2599 | 11047 | 017747 | | JSB PHI | |
| 2600 | 11050 | 031002 | | OCT 31002 | |
| 2601 | 11051 | 017747 | | JSB PHI | |
| 2602 | 11052 | 000537 | | OCT 537 | TELL DISC TO SHUT UP |
| 2603 | 11053 | 017747 | | JSB PHI | |
| 2604 | 11054 | 031004 | PIN | OCT 31004 | SET FLAG WHEN FIFO HAS DATA |
| 2605 | 11055 | 063073 | | LDA CMDF | GET FLAG ENABLE |
| 2606 | 11056 | 102631 | | OTA CTL | |
| 2607 | 11057 | 063151 | | LDA @M20 | SET MAX LOOP |
| 2608 | 11060 | 002006 | | INA,SZA | |
| 2609 | 11061 | 102330 | | SFS DR | ANY DATA |
| 2610 | 11062 | 127751 | | JMP PHIFI,I | NO EXIT |
| 2611 | 11063 | 103730 | | STC DR,C | YES EMPTY IT |
| 2612 | 11064 | 027060 | | JMP *-4 | TRY AGAIN |
| 2613* | | | | | |
| 2614 | 11065 | 177406 | N250 | DEC -250 | 1 MS DELAY COUNT |
| 2615 | 11066 | 000400 | @D256 | DEC 256 | |
| 2616 | 11067 | 176100 | TR1K | OCT 176100 | |
| 2617 | 11070 | 102000 | TR31K | OCT 102000 | |
| 2618 | 11071 | 000500 | TLK | OCT 500 | |
| 2619 | 11072 | 000440 | LSN | OCT 440 | |
| 2620 | 11073 | 103004 | CMDF | OCT 103004 | |
| 2621 | 11074 | 060000 | DCDCW | OCT 60000 | |
| 2622 | 11075 | 011076 | DCTYP | DEF **+1 | OLD ** HEADS PER CYL / SECTORS PER TRA |
| 2623 | 11076 | 101020 | | OCT 101020 | 8 2/16 MINI FLOPPY |
| 2624 | 11077 | 051036 | | OCT 051036 | 5 2/30 88010-20 |
| 2625 | 11100 | 041040 | | OCT 041040 | 4 2/32 7910 |
| 2626 | 11101 | 022460 | | OCT 022460 | 2 5/48 7920 |
| 2627 | 11102 | 014500 | | OCT 014500 | 1 9/64 7925 |
| 2628 | 11103 | 060460 | | OCT 060460 | 6 1/48 7906 |

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| 2630* | CONSTANTS | | | |
|-------|-----------|--------|-------|------------|
| 2631* | | | | |
| 2632 | 11104 | 000001 | @1 | OCT 1 |
| 2633 | 11105 | 000002 | @2 | OCT 2 |
| 2634 | 11106 | 000003 | @3 | OCT 3 |
| 2635 | 11107 | 000004 | @4 | OCT 4 |
| 2636 | 11110 | 000006 | @6 | OCT 6 |
| 2637 | 11111 | 000010 | @10 | OCT 10 |
| 2638 | 11112 | 000100 | @100 | OCT 100 |
| 2639 | 11113 | | RIT9 | EQU * |
| 2640 | 11113 | 001000 | @1000 | OCT 1000 |
| 2641 | 11114 | 001005 | @1005 | OCT 1005 |
| 2642 | 11115 | 000200 | @200 | OCT 200 |
| 2643 | 11116 | 000201 | @201 | OCT 201 |
| 2644 | 11117 | 000204 | @204 | OCT 204 |
| 2645 | 11120 | 000207 | @207 | OCT 207 |
| 2646 | 11121 | 002000 | @2000 | OCT 2000 |
| 2647 | 11122 | 002101 | @2101 | OCT 2101 |
| 2648 | 11123 | 000007 | @7 | OCT 7 |
| 2649 | 11124 | 000012 | @12 | OCT 12 |
| 2650 | 11125 | 000015 | @15 | OCT 15 |
| 2651 | 11126 | 000017 | @17 | OCT 17 |
| 2652 | 11127 | 000021 | @21 | OCT 21 |
| 2653 | 11130 | 000024 | @24 | OCT 24 |
| 2654 | 11131 | 000040 | @40 | OCT 40 |
| 2655 | 11132 | 000060 | @60 | OCT 60 |
| 2656 | 11133 | 000170 | @170 | OCT 170 |
| 2657 | 11134 | 000177 | @177 | OCT 177 |
| 2658 | 11135 | 000377 | @377 | OCT 377 |
| 2659 | 11136 | 001700 | @1700 | OCT 1700 |
| 2660 | 11137 | 037700 | @3770 | OCT 37700 |
| 2661 | 11140 | 000404 | @404 | OCT 404 |
| 2662 | 11141 | 000604 | @604 | OCT 604 |
| 2663 | 11142 | 076000 | @76K | OCT 76000 |
| 2664 | 11143 | 100000 | @100K | OCT 100000 |
| 2665 | 11144 | 177777 | @M1 | OCT -1 |
| 2666 | 11145 | 177776 | @M2 | OCT -2 |
| 2667 | 11146 | 177772 | @M6 | OCT -6 |
| 2668 | 11147 | 177770 | @M10 | OCT -10 |
| 2669 | 11150 | 177767 | @M11 | OCT -11 |
| 2670 | 11151 | 177760 | @M20 | OCT -20 |
| 2671 | 11152 | 177740 | @M40 | OCT -40 |
| 2672 | 11153 | 177754 | @N20 | DEC -20 |
| 2673 | 11154 | 177700 | @N64 | DEC -64 |

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2675*
2676 11155 000123 $2S OCT 123
2677 11156 000127 $2W OCT 127
2678*
2679 11157 060001 P2C% LDA B SAVE DATA
2680 11160 067741 LDB P2C+1 GET ADDRESS
2681 11161 101100 RRR 16 SWAP A&B
2682 11162 013154 AND @N64
2683 11163 101100 RRR 16 SWAP BACK
2684 11164 007004 CMB,INB MAKE IT NEGATIVE
2685 11165 047773 ADB P2.T0 NOW ADD STORE ADDRESS
2686 11166 101100 RRR 16 SWAP A&B
2687 11167 002020 SSA IF NEGATIVE THEN OK
2688 11170 127740 JMP P2C,I OK STORE CONTENTS
2689 11171 043154 ADA @N64 PAST 64 LOCATIONS?
2690 11172 002020 SSA
2691 11173 037740 ISZ P2C NO SKIP STORE
2692 11174 127740 JMP P2C,I RETURN
2693*
2694 11175 FOP2 EQU * END OF PAGE 2
2695*
2696 11740 ORG 11740B
2697 00543 RAP2 EQU *-FOP2 REMAINING ARFA FOR PAGE 2
2698 11740 000000 P2C NOP
2699 11741 017741 JSB * SET CURRENT ADDRESS
2700 11742 027157 DC.IN JMP P2C% GO CHECK ADDRESS
2701 11743 026333 DC.RW JMP DC%IN
2702 11744 026547 PHI.T JMP DC%RW
2703 11745 026751 PHI.L JMP PHI%T
2704 11746 026772 PHI.I JMP PHI%L
2705 11747 027013 PHI JMP PHI%I
2706 11750 027022 HPTB JMP PHI%
2707 11751 027030 PHIFL JMP HPIB%
2708 11752 027043 DCER JMP PHIF%
2709 11753 067752 P2.ST LDB DCER
2710 11754 006004 P2.HC INB
2711 11755 124001 P2FRR JMP B,I
2712 11756 000000 NOP

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2714*      RETURN TO PAGE 3
2715*
2716 11757 063141 RTNP3 LDA @604
2717 11760 007400      CCB
2718 11761 102601      OTA CPUST
2719 11762 026044      JMP LDP2      ENTRY FROM LOADER SECTION
2720*
2721*      RFP ENTRY POINTBREAK ENTRY POINT (SAME ON OTHER PAGE)
2722*
2723 11763 103105 P2VCP CLF 5      INSURE PARITY SENSE
2724 11764 106713      CLC 13B      DISABLE MAPING
2725 11765 103300      OCT 103300    SFS 0,C CHECK INTERRUPTS
2726 11766 027772      JMP *+4      THERE OFF
2727 11767 073772      STA P2.A     SAVE THE A REG.
2728 11770 003400      CCA         INDICATE INTS ON
2729 11771 027774      JMP *+3
2730 11772 073772      STA P2.A
2731 11773 002400      CLA
2732 11774 073764      STA P2.I
2733 11775 063120 P2VCO LDA @207    INSURE UPPER PAGE
2734 11776 102601      OTA CPUST
2735 11777 027775      JMP P2VCO   LOOP IF ERROR
2736*
2737*      COMMON STORAGE
2738 11777      P2.CT EQU 1777B+P2
2739*
2740 11776      P2.T3 EQU 1776B+P2
2741 11775      P2.T2 EQU 1775B+P2
2742 11774      P2.T1 EQU 1774B+P2
2743 11773      P2.T0 EQU 1773B+P2
2744 11772      P2.A  EQU 1772B+P2
2745 11771      P2.B  EQU 1771B+P2
2746 11770      P2.E  EQU 1770B+P2
2747 11767      P2.O  EQU 1767B+P2
2748 11766      P2.GF EQU 1766B+P2
2749 11765      P2.M  EQU 1765B+P2
2750 11764      P2.I  EQU 1764B+P2
2751 11763      P2.EM EQU 1763B+P2
2752 11762      P2.DF EQU 1762B+P2
2753 11761      P2.UN EQU 1761B+P2
2754 11760      P2.FL EQU 1760B+P2
2755 11757      P2.SB EQU 1757B+P2
2756 11756      P2.SC EQU 1756B+P2

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2758 12000          ORG 12000B
2759 12000          P3   EQU *           PAGE 3 REFERENCE
2760*
2761*
2762*      RE-ENTRY TO LOADERS FOR CONTINUATION
2763*
2764*      CCA
2765*      OIA 1
2766*      CLC 2
2767*      JSB 1
2768*
2769*      THIS SEQUENCE WILL RE-ENABLE THE ROMS AND
2770*      LOAD THE NEXT CONSECUTIVE PROGRAM
2771*
2772 12000 000000    NOP
2773 12001 000000    NOP
2774 12002 107700    CLC 0,C           TURN OFF THE WORLD
2775 12003 002400    CLA                LOAD NEXT PROGRAM
2776 12004 000000    NOP                IGNORE POWER FAIL
2777 12005 000000    NOP                IGNORE PARITY ERRORS
2778 12006 000000    NOP                IGNORE TBG
2779 12007 000000    NOP                IGNORE MEMORY PROTECT
2780 12010 000000    NOP                IGNORE UNIMPLEMENTED INST.
2781 12011 102503    LIA 3              GET FLAG
2782 12012 002021    SSA,RSS           IS IT AUTO MODE?
2783 12013 026020    JMP LDR+2        YES - DO NEXT LOAD
2784 12014 102702    STC 2            NOT CONTINUE SO
2785 12015 124001    JMP B,I          RETURN TO PROGRAM

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2787*      II.  BOOT LOADERS SECTION
2788*      DETERMINE WHICH LOADER TO USE
2789*
2790 12016 107700 LDR   CLC 0,C          RESET THE WORLD
2791 12017 006501      CLB,CLE,RSS
2792 12020 006700      CLB,CCE          SET FOR SEQUENTIAL LOADING
2793 12021 077773      STB P3.T0
2794 12022 077775      STB P3.T2          INDICATE POWER UP BOOTING
2795 12023 077762      STB P3.DF
2796 12024 077756      STB P3.SC
2797 12025 077755      STB P3ERR        CLEAR ANY ERRORS
2798 12026 063547      LDA #604          INDICATE IN LOADER
2799 12027 102601      OTA CPUST
2800 12030 102501      LIA CPUST        GET CPU STATUS
2801 12031 001727      ALF,ALF          POSITION LOADER BITS
2802 12032 002011      SLA,RSS          SPECIAL OPTIONS?
2803 12033 026072      JMP SPCL          YES
2804 12034 002040      SEZ              CONTINUATION?
2805 12035 026224      JMP LDCON          YES
2806 12036 064004      LDB 4              NO CHECK IF THERE IS SOMETHING TO RESTAR
2807 12037 006003      SZB,RSS
2808 12040 026043      JMP LDRC          NO THEN LOAD
2809 12041 063522      LDA #4           YES - SO RESTART IT
2810 12042 026127      JMP LDRCX
2811 12043 001310 LDRC  RAR,SLA      DETERMINE BOOT
2812 12044 026062      JMP LDRC1
2813 12045 001310      RAR,SLA
2814 12046 026057      JMP LDRC0
2815 12047 001210      RAL,SLA
2816 12050 026212      JMP LDRER        UNDEFINED LOADER (1)
2817 12051 002041      SEZ,RSS          IF CONT USE CARTRIDGE TAPE
2818 12052 026134      JMP CRSP1        GO TO VIRTUAL CONTROL PANEL
2819 12053 102501      LIA CPUST        GET STATUS
2820 12054 001710      ALF,SLA          IF DS FRONT PANNEL
2821 12055 026553      JMP DSLD          USE THE DS LOADER OTHERWISE (4)
2822 12056 026264      JMP CTLD          GO TO CARTRIDGE TAPE LOAD (0)
2823 12057 001210 LDRCO RAL,SLA
2824 12060 026212      JMP LDRER        UNDEFINED LOADER (3)
2825 12061 026762      JMP RMLD          PROM CARD LOADER (2)
2826 12062 001310 LDRC1 RAR,SLA
2827 12063 026067      JMP LDRC2
2828 12064 001310      RAR,SLA
2829 12065 026212      JMP LDRER        UNDEFINED LOADER (5)
2830 12066 026553      JMP DSLD          DISTRIBUTED LINK LOAD (4)
2831 12067 001310 LDRC2 RAR,SLA
2832 12070 026212      JMP LDRER        UNDEFINED LOADER (7)
2833 12071 027276      JMP DCLD          DISC CARTRIDGE LOAD (6)

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|-------|-------|--------|-------|-----------------|-------------------------------|
| 2835 | 12072 | 001310 | SPCL | RAR,SLA | DETERMINE SPECIAL |
| 2836 | 12073 | 026107 | | JMP SPCL1 | |
| 2837 | 12074 | 001310 | | RAR,SLA | |
| 2838 | 12075 | 026101 | | JMP SPCL0 | |
| 2839 | 12076 | 001310 | | RAR,SLA | |
| 2840 | 12077 | 026212 | | JMP LDRER | UNDEFINED SPECIAL |
| 2841 | 12100 | 026105 | | JMP TST | LOOP ON PRETEST |
| 2842 | 12101 | 001310 | SPCL0 | RAR,SLA | |
| 2843 | 12102 | 026212 | | JMP LDRER | UNDEFINED SPECIAL |
| 2844 | 12103 | 006006 | | INB,SZB | DELAY BEFORE LOOP |
| 2845 | 12104 | 026103 | | JMP *-1 | |
| 2846 | 12105 | 002400 | TST | CLA | RETURN TO PAGE 0 FOR PRETEST |
| 2847 | 12106 | 027761 | | JMP CRSP2+1 | |
| 2848 | 12107 | 001310 | SPCL1 | RAR,SLA | |
| 2849 | 12110 | 026114 | | JMP SPCL2 | |
| 2850 | 12111 | 001310 | | RAR,SLA | |
| 2851 | 12112 | 026117 | | JMP EXRM | USER DEFINED EXTENDED ROM |
| 2852 | 12113 | 026126 | | JMP LDRSX-1 | START MAC 2250 ROM CODE |
| 2853 | 12114 | 001310 | SPCL2 | RAR,SLA | |
| 2854 | 12115 | 026212 | | JMP LDRER | UNDEFINED SPECIAL |
| 2855 | 12116 | 026134 | | JMP CRSP1 | GO TO VIRTUAL CONTROL PANEL |
| 2856* | | | | | |
| 2857 | 12117 | 063545 | EXRM | LDA #377 | SET LAST PAGE |
| 2858 | 12120 | 070137 | | STA 137B | AND MAP LAST LOGICAL |
| 2859 | 12121 | 106705 | | CLC 5 | TURN OFF PARITY |
| 2860 | 12122 | 106704 | | CLC 4 | AND ANY OTHER INTERRUPTS |
| 2861 | 12123 | 102711 | | STC 11B | TURN ON MAPS |
| 2862 | 12124 | 003500 | | CCA,CLE | |
| 2863 | 12125 | 001675 | | ELA,CLE,SLA,ERA | MAKE ADDRESS |
| 2864 | 12126 | 062133 | | LDA RMADR | GO START ROM PROGRAM |
| 2865 | 12127 | 007400 | LDRSX | CCB | INDICATE PROGRAM IN EXECUTION |
| 2866 | 12130 | 106601 | | OTR CPUST | |
| 2867 | 12131 | 102702 | | STC 2 | EXIT LOADER |
| 2868 | 12132 | 124000 | | JMP A,I | |
| 2869 | 12133 | 040002 | RMADR | OCT 40002 | |

| | | | | | |
|-------|-------|--------|-------|-------------|---------------------------------|
| 2871 | 12134 | 007401 | CRSP1 | CCB,RSS | |
| 2872 | 12135 | 006400 | | CLB | |
| 2873 | 12136 | 063525 | | LDA #207 | |
| 2874 | 12137 | 027761 | | JMP CRSP2+1 | |
| | | | | | |
| 2876 | 12140 | 002400 | LDEX | CLA | NO ERRORS |
| 2877 | 12141 | 073755 | | STA P3ERR | |
| 2878 | 12142 | 063542 | | LDA #100 | UPDATE MAPS INCASE OF DMA LOAD |
| 2879 | 12143 | 164000 | | LDB A,I | |
| 2880 | 12144 | 174000 | | STB A,I | |
| 2881 | 12145 | 002004 | | INA | |
| 2882 | 12146 | 053544 | | CPA #177 | |
| 2883 | 12147 | 007401 | | CCB,RSS | |
| 2884 | 12150 | 026143 | | JMP *-5 | |
| 2885 | 12151 | 106624 | | OTB 24B | INDICATE INTERFACE HAS CHANGED |
| 2886 | 12152 | 067775 | | LDB P3.T2 | WAS THIS FROM THE VCP? |
| 2887 | 12153 | 006003 | | SZB,RSS | ?? |
| 2888 | 12154 | 026160 | | JMP **4 | NO |
| 2889 | 12155 | 067762 | | LDB P3.DF | |
| 2890 | 12156 | 006003 | | SZB,RSS | YES - LOAD AND GO? |
| 2891 | 12157 | 026135 | | JMP CRSP1+1 | NO RETURN TO VCP |
| 2892 | 12160 | 067755 | | LDB P3ERR | WAS THERE AN ERROR? |
| 2893 | 12161 | 006002 | | SZB | |
| 2894 | 12162 | 026212 | | JMP LDREP | YES THEN REPORT IT |
| 2895 | 12163 | 067762 | | LDB P3.DF | |
| 2896 | 12164 | 007002 | | CMB,SZB | TERMINATE AFTER SECONDARY LOAD? |
| 2897 | 12165 | 026177 | | JMP LDEX0 | NO |
| 2898 | 12166 | 062176 | | LDA HLT77 | YES SO HALT AFTER LOAD |
| 2899 | 12167 | 071700 | | STA 1700B | |
| 2900 | 12170 | 062211 | | LDA JMP.2 | SET CONTINUATION |
| 2901 | 12171 | 071701 | | STA 1701B | |
| 2902 | 12172 | 003400 | | CCA | |
| 2903 | 12173 | 006400 | | CLB | |
| 2904 | 12174 | 102702 | | SIC 2 | EXIT TO HALT |
| 2905 | 12175 | 025700 | | JMP 1700B | |
| 2906* | | | | | |
| 2907 | 12176 | 102077 | HLT77 | HLT 77B | |
| 2908* | | | | | |
| 2909 | 12177 | 003700 | LDEX0 | CCA,CCF | NO START PROGRAM |
| 2910 | 12200 | 102601 | | OTA CPUST | INDICATE ALL'S WELL |
| 2911 | 12201 | 005500 | | ERR | MAKE B -1 IF LOAD CALL BACK |
| 2912 | 12202 | 007003 | | CMB,SZB,RSS | |
| 2913 | 12203 | 026207 | | JMP LDEX1 | YES |
| 2914 | 12204 | 067756 | | LDB P3.SC | GET INTERFACE USED |
| 2915 | 12205 | 060001 | | LDA B | CHANGE HANDS |
| 2916 | 12206 | 067762 | | LDB P3.DF | INDICATE AUTO BOOT OR POWER UP |
| 2917 | 12207 | 102603 | LDEX1 | OTA 3 | SET AUTO FLAG |
| 2918 | 12210 | 102702 | | SIC 2 | DISABLE PROM |
| 2919 | 12211 | 024002 | JMP.2 | JMP 2 | NOW START PROGRAM |

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| | | | | | |
|-------|-------|--------|-------|------------------------|--------------------------------|
| 2921 | 12212 | 002400 | LDRER | CLA | CHECK FOR FRONT PANEL |
| 2922 | 12213 | 103503 | | LIA 3,C | |
| 2923 | 12214 | 002002 | | SZA | |
| 2924 | 12215 | 026135 | | JMP CRSP1+1 | YES SO GO TO VCP |
| 2925 | 12216 | 063547 | | LDA #604 | INDICAT LOAD ERROR |
| 2926 | 12217 | 002004 | | INA | |
| 2927 | 12220 | 102601 | | OTA CPUST | |
| 2928 | 12221 | 002006 | | INA,SZA | DELAY TO SHOW DISPLAY |
| 2929 | 12222 | 026221 | | JMP *-1 | |
| 2930 | 12223 | 026016 | | JMP LDP | TRY AGAIN |
| 2931* | | | | | |
| 2932* | | | | CONTINUATION LOADING | |
| 2933* | | | | | |
| 2934 | 12224 | 106503 | LDCON | LIB 3 | IS THERE A VCP REGISTER |
| 2935 | 12225 | 006003 | | SZB,RSS | |
| 2936 | 12226 | 026043 | | JMP LDRC | NO THEN USE DEFAULT SWITCHES |
| 2937 | 12227 | 102503 | | LIA 3 | GET DEVICE |
| 2938 | 12230 | 001700 | | ALF | |
| 2939 | 12231 | 013524 | | AND #7 | ONLY |
| 2940 | 12232 | 002003 | | SZA,RSS | CARTRIDGE TAPE? |
| 2941 | 12233 | 026264 | | JMP CTLD | YES |
| 2942 | 12234 | 053521 | | CPA #2 | PROM LOAD? |
| 2943 | 12235 | 026762 | | JMP RMLD | YES |
| 2944 | 12236 | 053522 | | CPA #4 | DISTRIBUTED LINK? |
| 2945 | 12237 | 026553 | | JMP DSLD | YES |
| 2946 | 12240 | 053523 | | CPA #6 | DISC LOAD? |
| 2947 | 12241 | 027276 | | JMP DCLD | YES |
| 2948 | 12242 | 026212 | | JMP LDRER | NONE SO ERROR |
| 2949* | | | | | |
| 2950* | | | | ENTRY FROM OTHER PAGES | |
| 2951* | | | | | |
| 2952 | 12243 | 006003 | LDRR | SZB,RSS | POWER UP? |
| 2953 | 12244 | 026016 | | JMP LDR | YES |
| 2954 | 12245 | 006020 | | SSB | VCP OR LOADER |
| 2955 | 12246 | 026142 | | JMP LDEX+2 | RETURN FROM OTHER LOADER PAGE |
| 2956 | 12247 | 002504 | | CLA,CLE,INA | NO ERRORS AND NOT CONTINUATION |
| 2957 | 12250 | 073755 | | STA P3ERR | |
| 2958 | 12251 | 060001 | | LDA B | VCP LOADER SELECTION |
| 2959 | 12252 | 067774 | | LDB P3.T1 | GET PARAMETERS |
| 2960 | 12253 | 053576 | | CPA S3CT | IS IT CATRTIDGE TAPE? |
| 2961 | 12254 | 026264 | | JMP CTLD | YES |
| 2962 | 12255 | 053577 | | CPA S3RM | IS IT ROM I/O? |
| 2963 | 12256 | 026762 | | JMP RMLD | YES |
| 2964 | 12257 | 053600 | | CPA S3DC | IS IT DISC CARTRIDGE? |
| 2965 | 12260 | 027276 | | JMP DCLD | YES |
| 2966 | 12261 | 053601 | | CPA S3DS | DISTRIBUTED LINK? |
| 2967 | 12262 | 026553 | | JMP DSLD | YES |
| 2968 | 12263 | 026142 | | JMP LDEX+2 | NONE SO LOAD ERPOR |

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2970*      HP-2644/5 CARTRIDGE TAPE LOADER ROUTINE
2971 12264 017743 CTLD JSB S.SC      SET SELECT CODE
2972 12265 000020 #20  OCT 20      DEFAULT SELECT CODE AND FILE
2973 12266 037761      ISZ P3.UN      MAKE UNIT 0 LEFT DRIVE
2974 12267 067760      LDB P3.FL      IF NO FILE # THEN SKIP FIND
2975 12270 006003      SZB,RSS
2976 12271 026325      JMP CTLD.
2977 12272 062542 CTLDF LDA $ESC&      FIND FILE
2978 12273 017754      JSB CTO.W
2979 12274 062543      LDA $.P0
2980 12275 067761      LDB P3.UN
2981 12276 030001      IOR B
2982 12277 017754      JSB CTO.W
2983 12300 067760      LDB P3.FL      GET FILE NUMBER
2984 12301 060001      LDA B
2985 12302 006400      CLB
2986 12303 100400      DIV #12      DIVIDE BY 10
2987 12305 077774      STB P3.T1
2988 12306 032547      IOR $.U0      ADD COMMAND
2989 12307 017754      JSB CTO.W
2990 12310 067774      LDB P3.T1      DO SECOND NUMBER
2991 12311 060001      LDA B
2992 12312 033540      IOR #60      MAKE IT A NUMBER
2993 12313 017753      JSB CTO.B      GIVE IT TO THE TERMINAL
2994 12314 062543      LDA $.P0
2995 12315 033521      IOR #2
2996 12316 017754      JSB CTO.W
2997 12317 062552      LDA SCDC1
2998 12320 017754      JSB CTO.W
2999 12321 017751      JSB CTI.B
3000 12322 053574      CPA $3S      OK?
3001 12323 002001      RSS
3002 12324 026142      JMP LDEX+2      NO
3003 12325 037755 CTLDF ISZ P3ERR      SET ERROR 11
3004 12326 067773      LDB P3.T0
3005 12327 060001      LDA B
3006 12330 053575      CPA $3W      READ OR WRITE
3007 12331 026406      JMP CTDW      WRITE

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|-------|-------|--------|-------|------------|-------------------------------------|
| 3009 | 12332 | 002400 | | CLA | CLEAR RECORD FLAG |
| 3010 | 12333 | 073760 | | STA P3.FL | |
| 3011 | 12334 | 062542 | CTLDO | LDA \$ESC& | OUTPUT "ESC &" |
| 3012 | 12335 | 017754 | | JSB CTO.W | |
| 3013 | 12336 | 062543 | | LDA \$P0 | P'2 |
| 3014 | 12337 | 067761 | | LDB P3.UN | |
| 3015 | 12340 | 030001 | | TOR B | |
| 3016 | 12341 | 017754 | | JSR CTO.W | |
| 3017 | 12342 | 062550 | | LDA \$S0 | |
| 3018 | 12343 | 033521 | | TOR #2 | |
| 3019 | 12344 | 017754 | | JSB CTO.W | |
| 3020 | 12345 | 062544 | | LDA \$RDC1 | R (DC1) |
| 3021 | 12346 | 017754 | | JSB CTO.W | |
| 3022 | 12347 | 017750 | | JSR CTI.W | |
| 3023 | 12350 | 060001 | | LDA B | CHANGE HANDS |
| 3024 | 12351 | 052541 | | CPA CTR | END OF FILE? |
| 3025 | 12352 | 026401 | | JMP CTLDX | YES |
| 3026 | 12353 | 017750 | | JSB CTI.W | LOAD COUNT WORDS |
| 3027 | 12354 | 017751 | | JSR CTI.B | |
| 3028 | 12355 | 063535 | | LDA #21 | TELL TERM. TO TRANSMIT |
| 3029 | 12356 | 073760 | | STA P3.FL | INDICATE RECORD READ |
| 3030 | 12357 | 017753 | | JSB CTO.B | |
| 3031 | 12360 | 017751 | | JSB CTI.B | READ FIRST BYTE |
| 3032 | 12361 | 003004 | | CMA,INA | MAKE COUNT NEG. |
| 3033 | 12362 | 073777 | | STA P3.CT | SAVE COUNT |
| 3034 | 12363 | 017751 | | JSB CTI.B | GET SECOND BYTE |
| 3035 | 12364 | 017750 | | JSB CTI.W | GET LOAD ADDRESS |
| 3036 | 12365 | 077773 | | STB P3.T0 | SAVE LOAD ADDRESS |
| 3037 | 12366 | 077774 | | STB P3.T1 | AND START CHECKSUM |
| 3038 | 12367 | 017750 | CTLDL | JSB CTI.W | GET DATA |
| 3039 | 12370 | 017732 | | JSB P3C | CHECK FOR MEMORY LIMIT AND STORE IT |
| 3040 | 12371 | 047774 | | ADB P3.T1 | ADD TO CHECKSUM |
| 3041 | 12372 | 077774 | | STB P3.T1 | |
| 3042 | 12373 | 037777 | | ISZ P3.CT | DONE WITH RECORD |
| 3043 | 12374 | 026367 | | JMP CTLDL | NO |
| 3044 | 12375 | 017750 | | JSB CTI.W | GET CHECKSUM FROM TAPE |
| 3045 | 12376 | 057774 | | CPB P3.T1 | DOES CHECKSUM AGREE? |
| 3046 | 12377 | 026334 | | JMP CTLDO | YES DO NEXT RECORD |
| 3047 | 12400 | 026142 | | JMP LDEX+2 | NO RETURN WITH ERROR |
| 3048* | | | | | |
| 3049 | 12401 | 067760 | CTLDX | LDB P3.FL | WAS THERE A RECORD READ? |
| 3050 | 12402 | 006002 | | SZB | |
| 3051 | 12403 | 026140 | | JMP LDEX | YES ALL'S WELL |
| 3052 | 12404 | 037755 | | TSZ P3ERR | SET FRROR 12 |
| 3053 | 12405 | 026142 | | JMP LDEX+2 | NO THEN ERROR |

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|------|-------|--------|-------|--------------|----------------------------------|
| 3055 | 12406 | 062265 | CTDP | LDA #20 | SET WRITE ERROR 20 |
| 3056 | 12407 | 073755 | | STA P3ERR | |
| 3057 | 12410 | 067757 | | LDB P3.SB | SET ADDRESS |
| 3058 | 12411 | 005727 | | BLF, BLF | |
| 3059 | 12412 | 005700 | | BLF | |
| 3060 | 12413 | 077773 | | STB P3.T0 | |
| 3061 | 12414 | 063573 | | LDA BLK | SET NUMBER OF BLOCKS |
| 3062 | 12415 | 073776 | | STA P3.T3 | |
| 3063 | 12416 | 067776 | CTDPO | LDB P3.T3 | END OF WRITE |
| 3064 | 12417 | 006003 | | SZB, RSS | |
| 3065 | 12420 | 026140 | | JMP LDEX | YES |
| 3066 | 12421 | 062542 | | LDA \$ESCB | OUTPUT "ESC & |
| 3067 | 12422 | 017754 | | JSB CTO.W | |
| 3068 | 12423 | 062543 | | LDA \$.P0 | .P UNIT |
| 3069 | 12424 | 067761 | | LDR P3.UN | |
| 3070 | 12425 | 030001 | | TOR B | |
| 3071 | 12426 | 017754 | | JSB CTO.W | |
| 3072 | 12427 | 062545 | | LDA \$.D1 | |
| 3073 | 12430 | 017754 | | JSB CTO.W | |
| 3074 | 12431 | 062546 | | LDA \$34 | 3 4 |
| 3075 | 12432 | 017754 | | JSB CTO.W | |
| 3076 | 12433 | 062551 | | LDA SWENO | W (ENQ) |
| 3077 | 12434 | 017754 | | JSB CTO.W | |
| 3078 | 12435 | 017751 | | JSB CTI.B | WAIT FOR ACKNOWLEDGE |
| 3079 | 12436 | 053523 | | CPA #6 | WAS IT AN ACKNOWLEDGE |
| 3080 | 12437 | 002001 | | RSS | YES |
| 3081 | 12440 | 026416 | | JMP CTDPO | NO TRY BLOCK AGAIN |
| 3082 | 12441 | 063573 | | LDA BLK | SET FOR ONE BLOCK |
| 3083 | 12442 | 073777 | | STA P3.CT | |
| 3084 | 12443 | 003004 | | CMA, INA | |
| 3085 | 12444 | 001727 | | ALF, ALF | PUT POSITIVE COUNT IN UPPER HALF |
| 3086 | 12445 | 017754 | | JSB CTO.W | |
| 3087 | 12446 | 067773 | | LDB P3.T0 | GET ADDRESS |
| 3088 | 12447 | 060001 | | LDA B | |
| 3089 | 12450 | 073774 | | STA P3.T1 | START CHECKSUM |
| 3090 | 12451 | 017754 | | JSB CTO.W | |
| 3091 | 12452 | 067772 | CTDPL | LDB P3.A | GET A & B REG |
| 3092 | 12453 | 060001 | | LDA B | |
| 3093 | 12454 | 067771 | | LDB P3.B | |
| 3094 | 12455 | 167773 | | LDR P3.T0, I | GET DATA |
| 3095 | 12456 | 060001 | | LDA B | |
| 3096 | 12457 | 047774 | | ADB P3.T1 | ADD DATA TO CHECKSUM |
| 3097 | 12460 | 077774 | | STB P3.T1 | |
| 3098 | 12461 | 017754 | | JSB CTO.W | OUTPUT WORD |
| 3099 | 12462 | 037773 | | ISZ P3.T0 | MOVE TO NEXT LOCATION |
| 3100 | 12463 | 037777 | | ISZ P3.CT | DONE WITH BLOCK |
| 3101 | 12464 | 026452 | | JMP CTDPL | NO |
| 3102 | 12465 | 067774 | | LDR P3.T1 | YES OUTPUT CHECKSUM |
| 3103 | 12466 | 060001 | | LDA B | |
| 3104 | 12467 | 017754 | | JSB CTO.W | |
| 3105 | 12470 | 037776 | | ISZ P3.T3 | NO DO ANOTHER BLOCK? |
| 3106 | 12471 | 000000 | | NOP | NO |

| | | | | |
|-------|-------|--------|------------------|-------------------------|
| 3108 | 12472 | 063535 | LDA #21 | OUTPUT DC1 |
| 3109 | 12473 | 017753 | JSB CTO.R | |
| 3110 | 12474 | 017751 | JSB CTI.B | GET RESULTS |
| 3111 | 12475 | 053574 | CPA S3S | WAS IT GOOD? |
| 3112 | 12476 | 026416 | JMP CTDPO | YES |
| 3113 | 12477 | 026142 | JMP LDEX+2 | NO |
| 3115 | 12500 | 017751 | CTI%W JSB CTI.P | GET A BYTE |
| 3116 | 12501 | 001727 | ALF,ALF | PUT IT IN UPPER HALF |
| 3117 | 12502 | 073754 | STA CTO.W | SAVE FIRST BYTE |
| 3118 | 12503 | 017751 | JSB CTI.B | GET LOWER BYTE |
| 3119 | 12504 | 067754 | LDB CTO.W | GET UPPER BYTE |
| 3120 | 12505 | 044000 | ADB A | PUT IN B-REG. |
| 3121 | 12506 | 127750 | JMP CTI.W,I | RETURN |
| 3122* | | | | |
| 3123 | 12507 | 062537 | CTI%B LDA CTCWI | GET INPUT CONTROL WORD |
| 3124 | 12510 | 102631 | OTA CTL | |
| 3125 | 12511 | 017752 | JSB CTIO | GET DATA |
| 3126 | 12512 | 013545 | AND #377 | MASK OFF UNWANTED BYTE |
| 3127 | 12513 | 127751 | JMP CTI.B,I | RETURN |
| 3128* | | | | |
| 3129 | 12514 | 013545 | CTO%B AND #377 | MASK UPPER HALF OFF |
| 3130 | 12515 | 064000 | LDR A | |
| 3131 | 12516 | 062540 | LDA CTCWD | GET OUTPUT CONTROL WORD |
| 3132 | 12517 | 102631 | OTA CTL | |
| 3133 | 12520 | 017752 | JSB CTIO | OUTPUT IT |
| 3134 | 12521 | 127753 | JMP CTO.R,I | RETURN |
| 3135* | | | | |
| 3136 | 12522 | 073750 | CTO%W STA CTI.W | SAVE A-REG. |
| 3137 | 12523 | 001727 | ALF,ALF | |
| 3138 | 12524 | 017753 | JSB CTO.B | OUTPUT UPPER HALF |
| 3139 | 12525 | 067750 | LDB CTI.W | |
| 3140 | 12526 | 060001 | LDA R | CHANGE HANDS |
| 3141 | 12527 | 017753 | JSB CTO.B | OUTPUT LOWER HALF |
| 3142 | 12530 | 127754 | JMP CTO.W,I | RETURN |
| 3143* | | | | |
| 3144 | 12531 | 106630 | CTIO% OTB DR | OUTPUT DATA |
| 3145 | 12532 | 103730 | STC DR,C | START TRANSFER |
| 3146 | 12533 | 102330 | SFS DR | WAIT FOR IT |
| 3147 | 12534 | 026533 | JMP *-1 | |
| 3148 | 12535 | 102530 | LIA DR | GET DATA |
| 3149 | 12536 | 127752 | JMP CTIO,I | RETURN |
| 3150* | | | | |
| 3151 | 12537 | 002400 | CTCWI OCT 002400 | |
| 3152 | 12540 | 001000 | CTCWD OCT 001000 | |
| 3153 | 12541 | 017015 | CTRS OCT 17015 | |
| 3154 | 12542 | 015446 | \$ESCG OCT 15446 | |
| 3155 | 12543 | 070060 | \$.PO OCT 70060 | |
| 3156 | 12544 | 051021 | \$RDC1 OCT 51021 | |
| 3157 | 12545 | 062061 | \$.D1 OCT 62061 | |
| 3158 | 12546 | 031464 | \$34 ASC 1,34 | |
| 3159 | 12547 | 072460 | \$.U0 OCT 72460 | |
| 3160 | 12550 | 071460 | \$.S0 OCT 71460 | |
| 3161 | 12551 | 053405 | \$WENQ OCT 53405 | |
| 3162 | 12552 | 041421 | \$CDC1 OCT 41421 | |

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3164*   DISTRIBUTED SYSTEMS LINK LOADER
3165*
3166   12553 017743  DSLD  JSB S.SC      SET SELECT CODE
3167   12554 040024          OCT 40024    DEFAULT SELECT CODE & DEVICE 4
3168   12555 017742          JSB DS.WF    WAIT FOR DS
3169   12556 026142          JMP LDEX+2   TIMED OUT
3170   12557 037755          ISZ P3ERR   MOVE TO 12
3171   12560 037755          ISZ P3ERR
3172   12561 067773          LDB P3.T0   CHECK IF THIS IS A DUMP
3173   12562 060001          LDA B       CHANGE HANDS
3174   12563 053575          CPA S3W    READ OR WRITE?
3175   12564 026654          JMP DSWR   IT'S A WRITE!!
3176   12565 063732          LDA DSDNL  ASK FOR A DOWN LOAD
3177   12566 017741          JSB DS.FT  WAIT FOR COMPLETION OF REQUEST
3178   12567 026142          JMP LDEX+2  TIMED OUT
3179   12570 037755          ISZ P3ERR  SET ERROR 13
3180   12571 067760          LDB P3.FL  GET FILE NUMBER
3181   12572 107630          OTB DR,C   PASS IT TO THE CARD
3182   12573 017742          JSB DS.WF  WAIT FOR IT TO COMPLETE
3183   12574 026142          JMP LDEX+2  TIMED OUT SO ERROR
3184   12575 007400          CCR        SET TO READ A FRAME
3185   12576 077777          STB P3.CT  (FRAME COUNT TO -1)
3186*
3187   12577 017740  DSRD  JSR DS.GT    GET WORD COUNT
3188   12600 101050          LSR 8      POSITION COUNT IN B
3189   12601 007007          CMB,INB,SZR,RSS MAKE COUNT NEG. (DONE?)
3190   12602 026622          JMP DSDUN  YES
3191   12603 077774          STB P3.T1  SAVE COUNT
3192   12604 017740          JSB DS.GT  GET LOAD ADDRESS
3193   12605 077773          STB P3.T0  SAVE LOAD ADDRESS
3194   12606 077776          STB P3.T3  AND START CHECKSUM
3195   12607 017740  DSRDL JSR DS.GT    GET WORD REQUEST
3196   12610 017732          JSR P3C    CHECK MEMORY LIMIT
3197   12611 047776          ADB P3.T3  ADD TO CHECKSUM
3198   12612 077776          STB P3.T3
3199   12613 037774          ISZ P3.T1  DONE WITH RECORD
3200   12614 026607          JMP DSPDL  NO
3201   12615 017740          JSB DS.GT  GET CHECKSUM
3202   12616 057776          CPB P3.T3  DOES CHECKSUM AGREE?
3203   12617 026577          JMP DSRD   YES DO NEXT RECORD
3204   12620 063527          LDA #11   SET CHECK SUM ERROR
3205   12621 026626          JMP DSEX   NO RETURN WITH ERROR
3206*
3207   12622 017740  DSDUN JSB DS.GT    GET ADDRESS AS FLAG
3208   12623 006003          SZB,RSS   GOOD OR BAD
3209   12624 026140          JMP LDEX   GOOD COMPLETED
3210   12625 063532          LDA #14
3211   12626 073755  DSEX  STA P3ERR   SET ERROR RETURN
3212   12627 026142          JMP LDEX+2

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|------|-------|--------|-------|-------------|--------------------------------|
| 3214 | 12630 | 037777 | DS%GT | ISZ P3.CT | TIME FOR NEW FRAME? |
| 3215 | 12631 | 026646 | | JMP DS%GO | NO JUST READ A WORD |
| 3216 | 12632 | 063533 | | LDA #15 | SET ERROR 15 |
| 3217 | 12633 | 073755 | | STA P3ERR | |
| 3218 | 12634 | 062673 | | LDA DSINR | GET RUFFER REQUEST |
| 3219 | 12635 | 017741 | | JSB DS.FT | GIVE IT TO CARD |
| 3220 | 12636 | 026142 | | JMP LDEX+2 | TIMED OUT |
| 3221 | 12637 | 037755 | | ISZ P3ERR | SET ERROR 16 |
| 3222 | 12640 | 106530 | | LIB DR | NO GET BUFFER COUNT |
| 3223 | 12641 | 060001 | | LDA B | SAVE COUNT |
| 3224 | 12642 | 007004 | | CMB,INB | MAKE FRAME COUNT NEGATIVE |
| 3225 | 12643 | 077777 | | STR P3.CT | SAVE IT |
| 3226 | 12644 | 017741 | | JSB DS.FT | TELL CARD HOW MUCH TO TRANSFER |
| 3227 | 12645 | 026142 | | JMP LDEX+2 | TIMED OUT |
| 3228 | 12646 | 063534 | DS%GO | LDA #17 | SET ERROR 17 |
| 3229 | 12647 | 073755 | | STA P3ERR | |
| 3230 | 12650 | 017742 | | JSB DS.WF | WAIT FOR FLAG |
| 3231 | 12651 | 026142 | | JMP LDEX+2 | IT DID SO ERROR |
| 3232 | 12652 | 107530 | | LIB DR,C | OK GET DATA |
| 3233 | 12653 | 127740 | | JMP DS.GT,I | RETURN |

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3235*      THIS ROUTINE DUMPS A MEMORY IMAGE TO A REMOTE COMPUTER
3236*
3237 12654 062265 DSWR LDA #20      SET ERROR 20
3238 12655 073755      STA P3ERR
3239 12656 062761      LDA DSVCP      TELL INTF TO GO INTO VCP MODE
3240 12657 017741      JSB DS.FT
3241 12660 026142      JMP LDEX+2    TIMED OUT
3242 12661 037755      ISZ P3ERR      SET ERROR 21
3243 12662 006400      CLB          SET STARTING ADDRESS
3244 12663 077773      STB P3.T0    SAVE IT
3245 12664 002404 DSWR0 CLA,INA    1 PLUS RUBOUT
3246 12665 017736      JSB DS.B     OUTPUT 1 BYTE
3247 12666 063545      LDA #377    NOW RUBOUT
3248 12667 017736      JSB DS.B
3249 12670 017737      JSB DS.CM    TRANSMITT BUFFFR
3250 12671 060400      OCT 60400
3251 12672 017737      JSB DS.CM    ASK FOR BUFFER
3252 12673 061400 DSWNR OCT 61400
3253 12674 017737      JSB DS.CM    ASK FOR BYTE
3254 12675 061000      OCT 61000
3255 12676 053545      CPA #377    CAN IT BE ACCEPTED?
3256 12677 026722      JMP DSWEX    NO SO ERROR
3257 12700 002003      SZA,RSS     DONE?
3258 12701 026140      JMP LDEX     YES
3259 12702 003004      CMA,INA    MAKE IT NEGATIVE
3260 12703 073777      STA P3.CT  SAVE AS COUNTER
3261 12704 067772 DSWR1 LDB P3.A  GET A AND B REGISTERS
3262 12705 060001      LDA B
3263 12706 067771      LDB P3.B
3264 12707 167773      LDB P3.T0,I GET DATA
3265 12710 060001      LDA B
3266 12711 001727      ALF,ALF
3267 12712 017736      JSB DS.B     TRANSFER CHARACTER
3268 12713 167773      LDB P3.T0,I
3269 12714 060001      LDA B
3270 12715 017736      JSB DS.B
3271 12716 037773      ISZ P3.T0    MOVE ADDRESS UP ONE
3272 12717 037777      ISZ P3.CT    DONE WITH THIS ONE?
3273 12720 026704      JMP DSWR1    NO
3274 12721 026664      JMP DSWR0    YES THEN MOVE TO NEXT TRANSFER
3275*
3276 12722 063536 DSWEX LDA #22    SET ERROR 22
3277 12723 026626      JMP DSEX     RETURN

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|-------|-------|--------|-------|-------------|-----------------------|
| 3279 | 12724 | 013545 | DS%B | AND #377 | |
| 3280 | 12725 | 033557 | | IOR #60K | DS PUT BYTE REQUEST |
| 3281 | 12726 | 017741 | | JSB DS.FT | WAIT FOR FLAG |
| 3282 | 12727 | 026142 | | JMP LDEX+2 | TIMED OUT |
| 3283 | 12730 | 102530 | | LIA DR | GET DATA |
| 3284 | 12731 | 127736 | | JMP DS.B,I | RETURN |
| 3285* | | | | | |
| 3286 | 12732 | 067737 | DS%CM | LDB DS.CM | GET COMMAND |
| 3287 | 12733 | 160001 | | LDA B,I | |
| 3288 | 12734 | 017741 | | JSB DS.FT | WAIT FOR FLAG |
| 3289 | 12735 | 026142 | | JMP LDEX+2 | TIMED OUT |
| 3290 | 12736 | 102530 | | LIA DR | GET DATA |
| 3291 | 12737 | 037737 | | ISZ DS.CM | |
| 3292 | 12740 | 064000 | | LDB A | |
| 3293 | 12741 | 127737 | | JMP DS.CM,I | |
| 3294* | | | | | |
| 3295 | 12742 | 102630 | DS%FT | OTA DR | |
| 3296 | 12743 | 103730 | | STC DR,C | |
| 3297 | 12744 | 063573 | | LDA BLK | GET TIME OUT |
| 3298 | 12745 | 102230 | | SFC DR | |
| 3299 | 12746 | 026754 | | JMP *+6 | |
| 3300 | 12747 | 034001 | | ISZ B | |
| 3301 | 12750 | 026745 | | JMP *-3 | |
| 3302 | 12751 | 034000 | | ISZ A | |
| 3303 | 12752 | 026745 | | JMP *-5 | |
| 3304 | 12753 | 127741 | | JMP DS.FT,I | RETURN TIME OUT |
| 3305 | 12754 | 037741 | | ISZ DS.FT | NO SKIP TIME OUT |
| 3306 | 12755 | 127741 | | JMP DS.FT,I | |
| 3307* | | | | | |
| 3308 | 12756 | 067742 | DS%WF | LDB DS.WF | CHANGE RETURN ADDRESS |
| 3309 | 12757 | 077741 | | STB DS.FT | |
| 3310 | 12760 | 026744 | | JMP DS%FT+2 | SKIP OUTPUT JUST FLAG |
| 3311* | | | | | |
| 3312 | 12761 | 067400 | DSVCP | OCT 67400 | |

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3314* UV PROM LOADER

3315*

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|------|-------|--------|-------|-------------|---------------------------------------|
| 3316 | 12762 | 017743 | RMLD | JSB S.SC | SET SELECT CODE |
| 3317 | 12763 | 020022 | | OCT 20022 | DEFAULT SELECT CODE DEVICE 2 |
| 3318 | 12764 | 067760 | | LDB P3.FL | MAKE FILE # NEG |
| 3319 | 12765 | 007000 | | CMB | MAKE NUMBER NEGATIVE |
| 3320 | 12766 | 077760 | | STB P3.FL | SAVE PROGRAM NUMBER |
| 3321 | 12767 | 002400 | | CLA | START WITH FIRST LOCATION IN ROM |
| 3322 | 12770 | 073773 | RMLD0 | STA P3.T0 | SAVE IT |
| 3323 | 12771 | 002021 | | SSA,RSS | IF ADDRESS GOES NEGATIVE THEN NEXT SC |
| 3324 | 12772 | 027000 | | JMP RMLD1 | |
| 3325 | 12773 | 017735 | | JSB RMNSC | MOVE TO NEXT SELECT CODETER |
| 3326 | 12774 | 067773 | | LDB P3.T0 | GET REMAINING COUNT |
| 3327 | 12775 | 060001 | | LDA B | |
| 3328 | 12776 | 001665 | | ELA,CLF,ERA | ELIMINATE BIT 15 |
| 3329 | 12777 | 026770 | | JMP RMLD0 | |
| 3330 | 13000 | 102631 | RMLD1 | OTA CTL | PASS ADDRESS TO ROM BOARD |
| 3331 | 13001 | 102730 | | STC DR | READ LOCATION IN ROM |
| 3332 | 13002 | 003400 | | CCA | |
| 3333 | 13003 | 102530 | | LIA DR | GET DATA FROM ROM |
| 3334 | 13004 | 073777 | | STA P3.CT | SAVE COUNT |
| 3335 | 13005 | 053563 | | CPA #M1 | END OF PROGRAMS? |
| 3336 | 13006 | 027075 | | JMP RMLD3 | YES THEN ERROR RETURN |
| 3337 | 13007 | 002021 | | SSA,RSS | IS THIS EXTENDED LOAD? |
| 3338 | 13010 | 027077 | | JMP RMLD4 | YES |
| 3339 | 13011 | 003004 | | CMA,INA | MOVE UP ONE LOCATION |
| 3340 | 13012 | 067773 | | LDB P3.T0 | GET PREVIOUS ADDRESS |
| 3341 | 13013 | 040001 | | ADA B | MOVE TO NEXT PROGRAM |
| 3342 | 13014 | 043521 | | ADA #2 | |
| 3343 | 13015 | 037760 | | ISZ P3.FL | WAS THIS IT? |
| 3344 | 13016 | 026770 | | JMP RMLD0 | NO TRY NEW ONE |
| 3345 | 13017 | 102730 | | STC DR | MOVE TO LOCATION IN MEMORY |
| 3346 | 13020 | 102530 | | LIA DR | |
| 3347 | 13021 | 073773 | | STA P3.T0 | SAVE IT |
| 3348 | 13022 | 067743 | | LDB S.SC | CHECK IF ON UPPER PAGE |
| 3349 | 13023 | 101100 | | RRR 16 | |
| 3350 | 13024 | 013561 | | AND #76K | |
| 3351 | 13025 | 002002 | | SZA | |
| 3352 | 13026 | 027060 | | JMP RMLD2 | YES SHIP CHECK |

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|-------|-------|--------|---------------|-----------------------------|
| 3354 | 13027 | 005121 | BRS,RRS | IS ADDRESS GREATER THAN 3 |
| 3355 | 13030 | 006002 | SZB | |
| 3356 | 13031 | 027060 | JMP RMLD2 | YES SKIP MOVE |
| 3357 | 13032 | 102501 | LIA CPUST | |
| 3358 | 13033 | 001200 | RAL | |
| 3359 | 13034 | 002021 | SSA,RSS | |
| 3360 | 13035 | 027040 | JMP *+3 | |
| 3361 | 13036 | 063537 | RMLDE LDA #40 | CAN'T DO IT |
| 3362 | 13037 | 026141 | JMP LDEX+1 | |
| 3363 | 13040 | 063550 | LDA #1700 | SET FROM ADDRESS |
| 3364 | 13041 | 073743 | STA S.SC | |
| 3365 | 13042 | 033561 | IOR #76K | |
| 3366 | 13043 | 167743 | LDB S.SC,I | |
| 3367 | 13044 | 174000 | STB A,I | |
| 3368 | 13045 | 037743 | ISZ S.SC | |
| 3369 | 13046 | 002004 | INA | |
| 3370 | 13047 | 002021 | SSA,RSS | |
| 3371 | 13050 | 027043 | JMP *-5 | |
| 3372 | 13051 | 103503 | LIA 3,C | CHANGE BREAK ADDRESS |
| 3373 | 13052 | 033561 | IOR #76K | |
| 3374 | 13053 | 103603 | OTA 3,C | |
| 3375 | 13054 | 063561 | LDA #76K | |
| 3376 | 13055 | 033057 | IOR *+2 | |
| 3377 | 13056 | 124000 | JMP A,I | |
| 3378 | 13057 | 001060 | DEF *+1-P3 | |
| 3379 | 13060 | 102730 | RMLD2 STC DR | NOW TRANSFER DATA |
| 3380 | 13061 | 102531 | LIA CTL | CHECK IT HASN'T ROLLED OVER |
| 3381 | 13062 | 002021 | SSA,RSS | |
| 3382 | 13063 | 027070 | JMP *+5 | NO - CONTINUE |
| 3383 | 13064 | 017735 | JSB RMNSC | MOVE TO NEXT SELECT CODE |
| 3384 | 13065 | 002400 | CLA | START WITH NEW |
| 3385 | 13066 | 102631 | OTA CTL | ADDRESS ON CARD |
| 3386 | 13067 | 027060 | JMP RMLD2 | |
| 3387 | 13070 | 106530 | LIB DR | GET DATA |
| 3388 | 13071 | 017732 | JSB P3C | CHECK IF STORABLE |
| 3389 | 13072 | 037777 | ISZ P3.CT | END OF TRANSFER |
| 3390 | 13073 | 027060 | JMP RMLD2 | NO |
| 3391 | 13074 | 026140 | JMP LDEX | YES |
| 3392* | | | | |
| 3393 | 13075 | 063530 | RMLD3 LDA #12 | SET ERROR 12 |
| 3394 | 13076 | 026141 | JMP LDEX+1 | |

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3396*      EXTENDED LOAD
3397*
3398  13077 103730 RMLD4 STC DR,C      MOVE TO PARTIAL
3399  13100 106531      LIB CTL      RESET FLAG SKIP
3400  13101 106631      OTB CTL
3401  13102 106530      LIB DR      GET PARTIAL
3402  13103 006002      SZB          IS THERE ANY
3403  13104 002004      INA          YES COUNT IT
3404  13105 043567      ADA #M11     IS IT OVER 8
3405  13106 002020      SSA          ??
3406  13107 027114      JMP *+5      NO THEN NEW FORMAT
3407  13110 067777      LDB P3.CT
3408  13111 060001      LDA B
3409  13112 003004      CMA,INA
3410  13113 027004      JMP RMLD1+4
3411  13114 102531      LIA CTL
3412  13115 043563      ADA #M1      BACK UP ONE
3413  13116 067777      LDB P3.CT   GET PARTIAL
3414  13117 006003      SZB,RSS     IF PARTIAL ONLY THEN OK
3415  13120 027141      JMP RMLD5
3416  13121 002002      SZA
3417  13122 027075      JMP RMLD3   NOT THEN MUST BE ON CARD BOUNDRY
3418  13123 037760      ISZ P3.FL   NOT SO ERROR
3419  13124 027126      JMP *+2     IS THIS THE FILE
3420  13125 027157      JMP RMLX    YES THEN LOAD IT
3421  13126 102530      LIA DR      GET PARTIAL
3422  13127 073773      STA P3.TO   SAVE IT
3423  13130 017735      JSB RMNSC   MOVE TO NEXT SELECT CODE
3424  13131 007400      CCB
3425  13132 047777      ADB P3.CT
3426  13133 077777      STB P3.CT
3427  13134 006002      SZB
3428  13135 027130      JMP *-5
3429  13136 067773      LDB P3.TO   GET PARTIAL
3430  13137 060001      LDA B
3431  13140 026770      JMP RMLD0
3432  13141 106530 RMLD5 LIB DR      PARTIAL ONLY
3433  13142 047773      ADB P3.TO
3434  13143 060001      LDA B
3435  13144 037760      ISZ P3.FL   IS THIS THE FILE
3436  13145 026770      JMP RMLD0   NO SKIP IT
3437  13146 002400      CLA        SET STARTING ADDRESS
3438  13147 073773      STA P3.TO
3439  13150 102530      LIA DR      GET PARTIAL
3440  13151 003004      CMA,INA     MAKE IT NEG
3441  13152 073777      STA P3.CT
3442  13153 102531      LIA CTL     BACK UP ONE
3443  13154 043563      ADA #M1
3444  13155 102631      OTA CTL
3445  13156 027060      JMP RMLD2   GO DO TRANSFER

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|------|-------|--------|-------|-----------|----------------------------------|
| 3447 | 13157 | 103503 | RMLX | LIA 3,C | CHECK IF ON BASE PAGE |
| 3448 | 13160 | 013561 | | AND #76K | IF NOT |
| 3449 | 13161 | 002002 | | SZA | |
| 3450 | 13162 | 027036 | | JMP RMLDE | THEN CAN'T DO IT |
| 3451 | 13163 | 102530 | | LIA DR | GET PARTIAL AGAIN |
| 3452 | 13164 | 073774 | | STA P3.T1 | SAVE IT |
| 3453 | 13165 | 063273 | | LDA RM1K | TRANSFER BASE PAGE UNDER DMA |
| 3454 | 13166 | 006700 | | CLB,CCE | SET BIT 15 |
| 3455 | 13167 | 005500 | | ERR | |
| 3456 | 13170 | 017734 | | JSR RM.TR | MAKE TRANSFER |
| 3457 | 13171 | 063274 | | LDA RM31K | SECOND PORTION COUNT AND ADDRESS |
| 3458 | 13172 | 064000 | | LDB A | |
| 3459 | 13173 | 017734 | | JSR RM.TR | TRANSFER IT |
| 3460 | 13174 | 067774 | | LDB P3.T1 | GET PARTIAL, |
| 3461 | 13175 | 006002 | | SZB | IF PARTIAL COUNT AS WHOLE |
| 3462 | 13176 | 037777 | | ISZ P3.CT | |
| 3463 | 13177 | 006400 | | CLB | |
| 3464 | 13200 | 077732 | | STB P3C | CLEAR MAP REG |
| 3465 | 13201 | 007400 | RMLX0 | CCB | DECREMENT COUNT |
| 3466 | 13202 | 047777 | | ADB P3.CT | |
| 3467 | 13203 | 077777 | | STB P3.CT | |
| 3468 | 13204 | 006002 | | SZB | |
| 3469 | 13205 | 006020 | | SSB | DONE |
| 3470 | 13206 | 026140 | | JMP LDEX | YES EXIT |
| 3471 | 13207 | 017735 | | JSR RMNSC | NO - MOVE TO NEXT SC |
| 3472 | 13210 | 006400 | | CLB | |
| 3473 | 13211 | 106502 | | LIB 2 | CHECK IF THERE |
| 3474 | 13212 | 050001 | | CPA B | |
| 3475 | 13213 | 002001 | | RSS | |
| 3476 | 13214 | 027075 | | JMP RMLD3 | NO SO ERROR |
| 3477 | 13215 | 067732 | | LDB P3C | USE MAPS |
| 3478 | 13216 | 060001 | | LDA B | |
| 3479 | 13217 | 043537 | | ADA #40 | MOVE UP ONE MAP |
| 3480 | 13220 | 073732 | | STA P3C | SAVE IT |
| 3481 | 13221 | 064000 | | LDB A | |
| 3482 | 13222 | 063562 | | LDA #100K | DO ALL OF IT |
| 3483 | 13223 | 017734 | | JSR RM.TP | |
| 3484 | 13224 | 027201 | | JMP RMLX0 | DO NEXT BLOCK |

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|-------|-------|--------|-------|-------------|--------------------------|
| 3486 | 13225 | 102623 | RM&TR | OTA 23B | PASS COUNT OUT |
| 3487 | 13226 | 063272 | | LDA RMCW | GET CONTROL WORD |
| 3488 | 13227 | 006021 | | SSB,RSS | |
| 3489 | 13230 | 002004 | | INA | |
| 3490 | 13231 | 102621 | | OTA 21B | CONTROL |
| 3491 | 13232 | 060001 | | LDA B | |
| 3492 | 13233 | 006021 | | SSB,RSS | ADDRESS OR MAPPED |
| 3493 | 13234 | 006400 | | CLB | MAPPED SO ADDR 0 |
| 3494 | 13235 | 106622 | | OTB 22B | |
| 3495 | 13236 | 005665 | | ELB,CLF,FRB | ELIMINATE BIT 15 |
| 3496 | 13237 | 106631 | | OTB 31B | AND CARD ADDRESS |
| 3497 | 13240 | 064141 | | LDB 141B | SAVE MAP CONTENT |
| 3498 | 13241 | 077774 | | STB P3.T1 | |
| 3499 | 13242 | 103130 | | CLF DR | AND ANY FLAGS |
| 3500 | 13243 | 070141 | | STA 141B | SET NEW MAP REG |
| 3501 | 13244 | 103721 | | STC 21B,C | START TRANSFER |
| 3502 | 13245 | 002400 | | CLA | |
| 3503 | 13246 | 102223 | | SFC 23B | DONE |
| 3504 | 13247 | 027254 | | JMP *+5 | |
| 3505 | 13250 | 002006 | | INA,SZA | |
| 3506 | 13251 | 027246 | | JMP *-3 | |
| 3507 | 13252 | 063531 | | LDA #13 | TIME OUT |
| 3508 | 13253 | 026141 | | JMP LDEX+1 | |
| 3509 | 13254 | 106721 | | CLC 21B | |
| 3510 | 13255 | 067774 | | LDB P3.T1 | RESTORE MAP REG |
| 3511 | 13256 | 074141 | | STB 141B | |
| 3512 | 13257 | 127734 | | JMP RM.TR,I | RETURN |
| 3513* | | | | | |
| 3514 | 13260 | 102502 | RM&SC | LIA 2 | MOVE TO NEXT SELECT CODE |
| 3515 | 13261 | 002004 | | INA | |
| 3516 | 13262 | 053542 | | CPA #100 | NOT OVER |
| 3517 | 13263 | 027075 | | JMP RMLD3 | YEP |
| 3518 | 13264 | 103602 | | OTA 2,C | OK |
| 3519 | 13265 | 002400 | | CLA | SEE IF IT IS THERE |
| 3520 | 13266 | 102502 | | LIA 2 | |
| 3521 | 13267 | 002003 | | SZA,RSS | |
| 3522 | 13270 | 027075 | | JMP RMLD3 | NO SO ERROR |
| 3523 | 13271 | 127735 | | JMP RMNSC,I | OK RETURN |
| 3524* | | | | | |
| 3525 | 13272 | 040200 | RMCW | OCT 40200 | STC + INPUT |
| 3526 | 13273 | 176100 | RM1K | OCT 176100 | |
| 3527 | 13274 | 102000 | RM31K | OCT 102000 | |
| 3528 | 13275 | 002000 | RMADX | OCT 2000 | |

3530* HP-IB DISC LOADER

3531*

| | | | | | |
|------|-------|--------|------|-----------|---------------------|
| 3532 | 13276 | 017743 | DCLD | JSB S.SC | SET SELECT CODE |
| 3533 | 13277 | 062027 | | OCT 62027 | DEFAULT SELECT CODE |
| 3534 | 13300 | 006404 | | CLB,INB | INDICATE DISC ROOT |
| 3535 | 13301 | 027760 | | JMP CRSP2 | GO TO OTHER PAGE |

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3537*      SET SELECT CODE
3538*
3539 13302 103101 S%SC CLO
3540 13303 063521 LDA #2      SET SELECT CODE ERROR
3541 13304 073755 STA P3ERR
3542 13305 002440 CLA,SEZ      CLEAR FILE NO. (CONTINUE)
3543 13306 027322 JMP S%SC0    YES USE DEFAULT
3544 13307 073760 STA P3.FL
3545 13310 006003 SZB,RSS      WAS THIS A DEFAULT?
3546 13311 027325 JMP S%SC1    YES
3547 13312 060001 LDA B        NO FILE # ONLY?
3548 13313 013570 AND #M20     MASK OFF FILE
3549 13314 101100 RRR 16      CHANG HANDS
3550 13315 006002 SZB          ?
3551 13316 027330 JMP S%SC2
3552 13317 073760 STA P3.FL    YES FILE ONLY
3553 13320 102101 STO          INDICATE FILE SET
3554 13321 027325 JMP S%SC1
3555 13322 102503 S%SC0 LIA 3    GET PREVIOUS DATA
3556 13323 002002 SZA
3557 13324 027327 JMP S%SC2-1
3558 13325 067743 S%SC1 LDB S.SC  PICK UP DEFAULT SC
3559 13326 160001 LDA B,I
3560 13327 013554 AND #7777    NO FILE NUMBER
3561 13330 073756 S%SC2 STA P3.SC  SAVE SELECT CODE USED
3562 13331 013540 AND #60      MUST BE OVER 20 OCT
3563 13332 002003 SZA,RSS
3564 13333 026142 JMP LDEX+2   NOT SO ERROR
3565 13334 067756 LDB P3.SC   RESTOR A REG
3566 13335 060001 LDA B
3567 13336 013541 AND #77
3568 13337 103602 OTA 2,C      SET AND ENAGLE GLOBAL REG.
3569 13340 002400 CLA          CHECK FOR RESPONSE
3570 13341 103502 LIA 2,C
3571 13342 002003 SZA,RSS
3572 13343 026142 JMP LDEX+2
3573 13344 067756 LDB P3.SC
3574 13345 005700 RLF          SET FILE #
3575 13346 074000 STB A
3576 13347 013534 AND #17
3577 13350 067760 LDB P3.FL
3578 13351 002040 SEZ          CONTINUE?
3579 13352 102525 LIA 25B     YES GET FILE #
3580 13353 102201 SOC          ONLY IF NOT PREVIOUSLY SFT
3581 13354 101100 RRR 16      IT WAS
3582 13355 073760 STA P3.FL
3583 13356 002004 INA          MOVE TO NEXT FILE NO
3584 13357 102625 OTA 25B     SET FOR NEXT LOAD

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| | | | | |
|------|-------|--------|------------|---------------------------|
| 3586 | 13360 | 067756 | LDB P3.SC | |
| 3587 | 13361 | 005700 | BLF | |
| 3588 | 13362 | 005723 | BLF,RBP | MOVET TO BUS ADDRESS |
| 3589 | 13363 | 060001 | LDA B | |
| 3590 | 13364 | 013524 | AND #7 | |
| 3591 | 13365 | 073757 | STA P3.SB | AND SET IT |
| 3592 | 13366 | 005723 | BLF,RBR | |
| 3593 | 13367 | 060001 | LDA B | |
| 3594 | 13370 | 013524 | AND #7 | |
| 3595 | 13371 | 073761 | STA P3.UN | UNIT NO |
| 3596 | 13372 | 067743 | LDB S.SC | GET DEVICE NO. |
| 3597 | 13373 | 106624 | OTB 24B | SAVE CURRENT PAGE |
| 3598 | 13374 | 160001 | LDA B,I | |
| 3599 | 13375 | 013560 | AND #70K | |
| 3600 | 13376 | 067756 | LDB P3.SC | GET CURRENT DEVICE |
| 3601 | 13377 | 101100 | RRR 16 | |
| 3602 | 13400 | 013554 | AND #7777 | |
| 3603 | 13401 | 030001 | IOR B | |
| 3604 | 13402 | 073756 | STA P3.SC | |
| 3605 | 13403 | 025404 | JMP **1-P3 | PUT SELF ON BASE PAGE |
| 3606 | 13404 | 064137 | LDB 137B | SAVE MAP FOR CHECK |
| 3607 | 13405 | 002400 | CLA | |
| 3608 | 13406 | 070137 | STA 137B | SET TO MAP TO PAGE 0 |
| 3609 | 13407 | 063561 | LDA #76K | |
| 3610 | 13410 | 033551 | IOR #1776 | SET ADDRESS FOR LAST PAGE |
| 3611 | 13411 | 102711 | STC 11B | ENABLE MAPS |
| 3612 | 13412 | 027413 | JMP **1 | TURN THEM ON |
| 3613 | 13413 | 174000 | STB A,I | PUT DATA IN UPPER PAGE |
| 3614 | 13414 | 154000 | CPR A,I | DID IT STORE? |
| 3615 | 13415 | 002005 | INA,RSS | YES |
| 3616 | 13416 | 027436 | JMP S%SC4 | NO ONLY 16K |
| 3617 | 13417 | 067777 | LDB P3.CT | GET NEW DATA |
| 3618 | 13420 | 007000 | CMB | |
| 3619 | 13421 | 174000 | STB A,I | TRY CROSS PAGE |
| 3620 | 13422 | 106711 | CLC 11B | DISABLE MAPS |
| 3621 | 13423 | 027424 | JMP **1 | TURN THEM OFF |
| 3622 | 13424 | 002400 | CLA | |
| 3623 | 13425 | 057777 | CPR P3.CT | DID IT STORE IN BASE PAGE |
| 3624 | 13426 | 027433 | JMP S%SC3 | YES THEN MAPPED SYSTEM |
| 3625 | 13427 | 063561 | LDA #76K | SET FOR 16K |
| 3626 | 13430 | 033432 | IOR **2 | |
| 3627 | 13431 | 124000 | JMP A,I | PUT SELF ON PAGE |
| 3628 | 13432 | 001433 | DEF **1-P3 | |

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| | | | | | |
|------|-------|--------|-------|------------|-----------------------|
| 3630 | 13433 | 067776 | S%SC3 | LDR P3.T3 | RESTOR LOCATION |
| 3631 | 13434 | 074137 | | STB 137B | |
| 3632 | 13435 | 027442 | | JMP *+5 | |
| 3633 | 13436 | 063555 | S%SC4 | LDA #36K | ONLY 16K FOR MAX |
| 3634 | 13437 | 033441 | | IOR *+2 | |
| 3635 | 13440 | 124000 | | JMP A,I | |
| 3636 | 13441 | 001442 | | DEF *+1-P3 | |
| 3637 | 13442 | 013561 | | AND #76K | USE PAGE |
| 3638 | 13443 | 107503 | | LIB 3,C | GET ON PAGE ADDRESS |
| 3639 | 13444 | 101100 | | RRR 16 | |
| 3640 | 13445 | 013552 | | AND #1777 | |
| 3641 | 13446 | 030001 | | IOR B | |
| 3642 | 13447 | 103603 | | OTA 3,C | |
| 3643 | 13450 | 102524 | | LIA 24B | GET PREVIOUS ADDRESS |
| 3644 | 13451 | 013561 | | AND #76K | SET FOR MOVE |
| 3645 | 13452 | 033550 | | IOR #1700 | |
| 3646 | 13453 | 102624 | | OTA 24B | FROM ADDRESS |
| 3647 | 13454 | 063550 | | LDA #1700 | |
| 3648 | 13455 | 030001 | | IOR B | |
| 3649 | 13456 | 102626 | | OTA 26B | TO ADDRESS |
| 3650 | 13457 | 102524 | S%SC5 | LIA 24B | *DO MOVE |
| 3651 | 13460 | 164000 | | LDR A,I | |
| 3652 | 13461 | 002004 | | INA | |
| 3653 | 13462 | 102624 | | OTA 24B | |
| 3654 | 13463 | 102526 | | LIA 26B | |
| 3655 | 13464 | 174000 | | STB A,I | |
| 3656 | 13465 | 002004 | | INA | |
| 3657 | 13466 | 102626 | | OTA 26B | |
| 3658 | 13467 | 013552 | | AND #1777 | |
| 3659 | 13470 | 002002 | | SZA | DONE? |
| 3660 | 13471 | 027457 | | JMP S%SC5 | NO |
| 3661 | 13472 | 067743 | | LDR S.SC | SET RETURN ADDRESS |
| 3662 | 13473 | 060001 | | LDA B | |
| 3663 | 13474 | 013552 | | AND #1777 | |
| 3664 | 13475 | 101100 | | RRR 16 | |
| 3665 | 13476 | 102526 | | LIA 26B | |
| 3666 | 13477 | 043563 | | ADA #M1 | |
| 3667 | 13500 | 013561 | | AND #76K | |
| 3668 | 13501 | 030001 | | IOR B | |
| 3669 | 13502 | 073743 | | STA S.SC | |
| 3670 | 13503 | 013561 | | AND #76K | UPDATE STRING POINTER |
| 3671 | 13504 | 067762 | | LDB P3.DF | |
| 3672 | 13505 | 006003 | | SZB,RSS | IF NOT DEFINED |
| 3673 | 13506 | 027513 | | JMP *+5 | THEN SKIP UPDATE |
| 3674 | 13507 | 101100 | | RRR 16 | |
| 3675 | 13510 | 013552 | | AND #1777 | |
| 3676 | 13511 | 030001 | | IOR B | |
| 3677 | 13512 | 073762 | | STA P3.DF | |
| 3678 | 13513 | 037743 | | ISZ S.SC | ADJUST RETURN |
| 3679 | 13514 | 063526 | | LDA #10 | SET DEVICE ERROR |
| 3680 | 13515 | 073755 | | STA P3ERR | |
| 3681 | 13516 | 127743 | | JMP S.SC,I | AND RETURN |

| 3683* CONSTANTS | | | | |
|---------------------------|-------|--------|-------|--------------|
| 3684 | 13517 | 001763 | VCPD3 | DEF P3VCP-P3 |
| 3685* | | | | |
| 3686 | 13520 | 000001 | #1 | OCT 1 |
| 3687 | 13521 | 000002 | #2 | OCT 2 |
| 3688 | 13522 | 000004 | #4 | OCT 4 |
| 3689 | 13523 | 000006 | #6 | OCT 6 |
| 3690 | 13524 | 000007 | #7 | OCT 7 |
| 3691 | 13525 | 000207 | #207 | OCT 207 |
| 3692 | 13526 | 000010 | #10 | OCT 10 |
| 3693 | 13527 | 000011 | #11 | OCT 11 |
| 3694 | 13530 | 000012 | #12 | OCT 12 |
| 3695 | 13531 | 000013 | #13 | OCT 13 |
| 3696 | 13532 | 000014 | #14 | OCT 14 |
| 3697 | 13533 | 000015 | #15 | OCT 15 |
| 3698 | 13534 | 000017 | #17 | OCT 17 |
| 3699 | 13535 | 000021 | #21 | OCT 21 |
| 3700 | 13536 | 000022 | #22 | OCT 22 |
| 3701 | 13537 | 000040 | #40 | OCT 40 |
| 3702 | 13540 | 000060 | #60 | OCT 60 |
| 3703 | 13541 | 000077 | #77 | OCT 77 |
| 3704 | 13542 | 000100 | #100 | OCT 100 |
| 3705 | 13543 | 000170 | #170 | OCT 170 |
| 3706 | 13544 | 000177 | #177 | OCT 177 |
| 3707 | 13545 | 000377 | #377 | OCT 377 |
| 3708 | 13546 | 000404 | #404 | OCT 404 |
| 3709 | 13547 | 000604 | #604 | OCT 604 |
| 3710 | 13550 | 001700 | #1700 | OCT 1700 |
| 3711 | 13551 | 001776 | #1776 | OCT 1776 |
| 3712 | 13552 | 001777 | #1777 | OCT 1777 |
| 3713 | 13553 | 037700 | #3770 | OCT 37700 |
| 3714 | 13554 | 007777 | #7777 | OCT 7777 |
| 3715 | 13555 | 036000 | #36K | OCT 36000 |
| 3716 | 13556 | 040000 | #40K | OCT 40000 |
| 3717 | 13557 | 060000 | #60K | OCT 60000 |
| 3718 | 13560 | 070000 | #70K | OCT 70000 |
| 3719 | 13561 | 076000 | #76K | OCT 76000 |
| 3720 | 13562 | 100000 | #100K | OCT 100000 |
| 3721 | 13563 | 177777 | #M1 | OCT -1 |
| 3722 | 13564 | 177776 | #M2 | OCT -2 |
| 3723 | 13565 | 177772 | #M6 | OCT -6 |
| 3724 | 13566 | 177770 | #M10 | OCT -10 |
| 3725 | 13567 | 177767 | #M11 | OCT -11 |
| 3726 | 13570 | 177760 | #M20 | OCT -20 |
| 3727 | 13571 | 177740 | #M40 | OCT -40 |
| 3728 | 13572 | 177754 | #N20 | DEC -20 |
| 3729 | 13573 | 177700 | BLK | DEC -64 |
| 3730* | | | | |
| 3731 | 13574 | 000123 | \$3S | OCT 123 |
| 3732 | 13575 | 000127 | \$3W | OCT 127 |
| 3733 | 13576 | 041524 | \$3CT | ASC 1,CT |
| 3734 | 13577 | 051115 | \$3RM | ASC 1,RM |
| 3735 | 13600 | 042103 | \$3DC | ASC 1,DC |
| 3736 | 13601 | 042123 | \$3DS | ASC 1,DS |

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| | | | | | |
|-------|-------|--------|-------|-------------|---------------------------|
| 3738 | 13602 | 060001 | P3C% | LDA B | SAVE DATA |
| 3739 | 13603 | 067733 | | LDB P3C+1 | GET ADDRESS |
| 3740 | 13604 | 101100 | | RRR 16 | SWAP A&B |
| 3741 | 13605 | 013573 | | AND BLK | |
| 3742 | 13606 | 101100 | | RRR 16 | SWAP BACK |
| 3743 | 13607 | 007004 | | CMB,INB | MAKE IT NEGATIVE |
| 3744 | 13610 | 047773 | | ADB P3.TO | NOW ADD STORE ADDRESS |
| 3745 | 13611 | 101100 | | RRR 16 | SWAP A&B |
| 3746 | 13612 | 002020 | | SSA | IF NEGATIVE THEN OK |
| 3747 | 13613 | 027617 | | JMP *+4 | OK STORE CONTENTS |
| 3748 | 13614 | 043573 | | ADA BLK | PAST 64 LOCATIONS? |
| 3749 | 13615 | 002020 | | SSA | |
| 3750 | 13616 | 027627 | | JMP P3C%0 | NO SKIP STORE |
| 3751 | 13617 | 060001 | | LDA B | |
| 3752 | 13620 | 067773 | | LDB P3.TO | CHECK IF A OR B |
| 3753 | 13621 | 101100 | | RRR 16 | |
| 3754 | 13622 | 002003 | | SZA,RSS | IS IT A REG REF? |
| 3755 | 13623 | 077772 | | STB P3.A | YEP |
| 3756 | 13624 | 053520 | | CPA #1 | HOW ABOUT B REG REF |
| 3757 | 13625 | 077771 | | STB P3.B | |
| 3758 | 13626 | 177773 | | STB P3.TO,I | THEN MEMORY |
| 3759 | 13627 | 037773 | P3C%0 | ISZ P3.TO | MOVE TO NEXT LOCATION |
| 3760 | 13630 | 127732 | | JMP P3C,I | RETURN |
| 3761* | | | | | |
| 3762 | 13631 | | FOP3 | EQU * | END OF PAGE 3 |
| 3763* | | | | | |
| 3764 | 13732 | | | ORG 13732B | |
| 3765 | 00101 | | RAP3 | EQU *-FOP3 | REMAINING AREA FOR PAGE 3 |
| 3766 | 13732 | | DSDNL | EQU * | |
| 3767 | 13732 | 161001 | P3C | OCT 161001 | |
| 3768 | 13733 | 017733 | | JSB * | SET CURRENT ADDRESS |
| 3769 | 13734 | 027602 | RM.TR | JMP P3C% | GO CHECK ADDRESS |
| 3770 | 13735 | 027225 | RMNSC | JMP RM%TR | |
| 3771 | 13736 | 027260 | DS.B | JMP RM%SC | |
| 3772 | 13737 | 026724 | DS.CM | JMP DS%B | |
| 3773 | 13740 | 026732 | DS.GT | JMP DS%CM | |
| 3774 | 13741 | 026630 | DS.FT | JMP DS%GT | |
| 3775 | 13742 | 026742 | DS.WF | JMP DS%FT | |
| 3776 | 13743 | 026756 | S.SC | JMP DS%WF | |
| 3777 | 13744 | 063750 | | LDA CTI.W | GET RETURN JUMP |
| 3778 | 13745 | 073750 | | STA *+3 | |
| 3779 | 13746 | 102702 | | STC 2 | DISABLE ROM |
| 3780 | 13747 | 106702 | | CLC 2 | ENABLE ROM |
| 3781 | 13750 | 027302 | CTI.W | JMP S%SC | |
| 3782 | 13751 | 026500 | CTI.B | JMP CTI%W | |
| 3783 | 13752 | 026507 | CTIO | JMP CTI%B | |
| 3784 | 13753 | 026531 | CTO.B | JMP CTIO% | |
| 3785 | 13754 | 026514 | CTO.W | JMP CTO%B | |
| 3786 | 13755 | 026522 | P3ERR | JMP CTO%W | |
| 3787 | 13756 | 026140 | | JMP LDEX | |
| 3788 | 13757 | 000000 | | NOP | |

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3790*      CROSS OVER TO LOWER PAGE
3791*
3792 13760 063546 CRSP2 LDA #404      BITS FOR PAGE 2 LOADERS
3793 13761 102601      OTA CPUST
3794 13762 026243      JMP LDRR      ENTRY FROM OTHER PAGES
3795*
3796*      RFP ENTRY POINTBREAK ENTRY POINT (SAME ON OTHER PAGE)
3797*
3798 13763 103105 P3VCP CLF 5      INSURE PARITY SENSE
3799 13764 106713      CLC 13B      DISABLE MAPING
3800 13765 103300      OCT 103300    SFS 0,C CHECK INTERRUPTS
3801 13766 027772      JMP **4      THERE OFF
3802 13767 073772      STA P3.A      SAVE THE A REG.
3803 13770 003400      CCA      INDICATE INTS ON
3804 13771 027774      JMP **3
3805 13772 073772      STA P3.A
3806 13773 002400      CLA
3807 13774 073764      STA P3.I
3808 13775 063525 P3VCO LDA #207    INSURE UPPER PAGE
3809 13776 102601      OTA CPUST
3810 13777 027775      JMP P3VCO    LOOP IF ERROR
3811*
3812*      COMMON STORAGE
3813*
3814 13777      P3.CT EQU 1777B+P3
3815 13776      P3.T3 EQU 1776P+P3
3816 13775      P3.T2 EQU 1775R+P3
3817 13774      P3.T1 EQU 1774R+P3
3818 13773      P3.T0 EQU 1773R+P3
3819 13772      P3.A EQU 1772B+P3
3820 13771      P3.B EQU 1771R+P3
3821 13770      P3.E EQU 1770B+P3
3822 13767      P3.O EQU 1767B+P3
3823 13766      P3.GF EQU 1766R+P3
3824 13765      P3.M EQU 1765R+P3
3825 13764      P3.I EQU 1764B+P3
3826 13763      P3.EM EQU 1763R+P3
3827 13762      P3.DF EQU 1762R+P3
3828 13761      P3.UN EQU 1761B+P3
3829 13760      P3.FL EQU 1760R+P3
3830 13757      P3.SR EQU 1757B+P3
3831 13756      P3.SC EQU 1756B+P3
3832*
3833*
3834      END
** NO ERRORS *TOTAL **RTE ASMB 92067-16011**

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PAGE 0091
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| #1 | 03686 | 03756 | | | | | |
| #10 | 03692 | 03679 | | | | | |
| #100 | 03704 | 02878 | 03516 | | | | |
| #100K | 03720 | 03482 | | | | | |
| #11 | 03693 | 03204 | | | | | |
| #12 | 03694 | 02986 | 03393 | | | | |
| #13 | 03695 | 03507 | | | | | |
| #14 | 03696 | 03210 | | | | | |
| #15 | 03697 | 03216 | | | | | |
| #17 | 03698 | 03228 | 03576 | | | | |
| @#170 | 03705 | | | | | | |
| #1700 | 03710 | 03363 | 03645 | 03647 | | | |
| #177 | 03706 | 02882 | | | | | |
| #1776 | 03711 | 03610 | | | | | |
| #1777 | 03712 | 03640 | 03658 | 03663 | 03675 | | |
| #2 | 03687 | 02942 | 02995 | 03018 | 03342 | 03540 | |
| #20 | 02972 | 03055 | 03237 | | | | |
| #207 | 03691 | 02873 | 03808 | | | | |
| #21 | 03699 | 03028 | 03108 | | | | |
| #22 | 03700 | 03276 | | | | | |
| #36K | 03715 | 03633 | | | | | |
| #377 | 03707 | 02857 | 03126 | 03129 | 03247 | 03255 | 03279 |
| @#3770 | 03713 | | | | | | |
| #4 | 03688 | 02809 | 02944 | | | | |
| #40 | 03701 | 03361 | 03479 | | | | |
| #404 | 03708 | 03792 | | | | | |
| @#40K | 03716 | | | | | | |

PAGE 0092

CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| #6 | 03689 | 02946 | 03079 | | | | |
| #60 | 03702 | 02992 | 03562 | | | | |
| #604 | 03709 | 02798 | 02925 | | | | |
| #60K | 03717 | 03280 | | | | | |
| #7 | 03690 | 02939 | 03590 | 03594 | | | |
| #70K | 03718 | 03599 | | | | | |
| #76K | 03719 | 03350 | 03365 | 03373 | 03375 | 03448 | 03609 |
| | 03625 | 03637 | 03644 | 03667 | 03670 | | |
| #77 | 03703 | 03567 | | | | | |
| #7777 | 03714 | 03560 | 03602 | | | | |
| #M1 | 03721 | 03335 | 03412 | 03443 | 03666 | | |
| @#M10 | 03724 | | | | | | |
| #M11 | 03725 | 03404 | | | | | |
| @#M2 | 03722 | | | | | | |
| #M20 | 03726 | 03548 | | | | | |
| @#M40 | 03727 | | | | | | |
| @#M6 | 03723 | | | | | | |
| @#N20 | 03728 | | | | | | |
| \$!? | 01873 | 01559 | | | | | |
| \$% | 01859 | 01385 | | | | | |
| \$.D1 | 03157 | 03072 | | | | | |
| \$.P0 | 03155 | 02979 | 02994 | 03013 | 03068 | | |
| \$.S0 | 03160 | 03017 | | | | | |
| \$.U0 | 03159 | 02988 | | | | | |
| @\$2S | 02676 | | | | | | |
| \$2W | 02677 | 02071 | 02391 | | | | |
| \$34 | 03158 | 03074 | | | | | |
| \$3CT | 03733 | 02960 | | | | | |

PAGE 0093

CROSS-REFERENCE SYMBOL TABLE

| | | | | | |
|--------|-------|-------|-------|-------|-------|
| \$3DC | 03735 | 02964 | | | |
| \$3DS | 03736 | 02966 | | | |
| \$3RM | 03734 | 02962 | | | |
| \$3S | 03731 | 03000 | 03111 | | |
| \$3W | 03732 | 03006 | 03174 | | |
| \$A | 01840 | 01439 | 01596 | | |
| \$B | 01841 | 01402 | 01442 | 01598 | |
| \$C | 01850 | 01396 | 01451 | 01594 | |
| \$CDC1 | 03162 | 02997 | | | |
| \$D | 01851 | 01580 | 01673 | | |
| \$E | 01846 | 01398 | 01454 | 01600 | |
| \$ER | 01872 | 01335 | | | |
| \$ESC& | 03154 | 02977 | 03011 | 03066 | |
| \$G | 01845 | 01466 | 01608 | | |
| \$I | 01848 | 01460 | 01604 | | |
| \$K | 01849 | 01463 | 01606 | | |
| \$L | 01852 | 01281 | 01400 | | |
| \$LC | 01871 | 01329 | | | |
| \$M | 01842 | 01406 | 01469 | 01624 | 01665 |
| \$N | 01853 | 01578 | | | |
| \$O | 01847 | 01457 | 01602 | | |
| \$P | 01839 | 01394 | 01445 | 01626 | |
| \$R | 01855 | 01390 | 01412 | | |
| \$R0 | 01860 | 01499 | 01636 | | |
| \$R1 | 01861 | 01502 | 01638 | | |
| \$R2 | 01862 | 01505 | 01640 | | |
| \$R3 | 01863 | 01508 | 01642 | | |
| \$RC | 01865 | 01512 | 01646 | | |

PAGE 0094
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| \$RD | 01864 | 01510 | 01644 | | | | |
| \$RDC1 | 03156 | 03020 | | | | | |
| \$RF | 01869 | 01540 | | | | | |
| \$RI | 01867 | 01517 | | | | | |
| \$RM | 01874 | 01496 | 01634 | | | | |
| \$RS | 01866 | 01514 | 01648 | | | | |
| \$RX | 01868 | 01520 | | | | | |
| \$S | 01856 | 01392 | | | | | |
| \$T | 01844 | 01376 | 01408 | 01475 | 01611 | 01661 | |
| \$U | 01854 | 01377 | 01483 | 01613 | 01663 | | |
| \$V | 01857 | 01448 | 01592 | | | | |
| \$W | 01858 | 01283 | 01404 | | | | |
| \$WENQ | 03161 | 03076 | | | | | |
| **ORG | ***** | 00003 | 00061 | 01009 | 01056 | 01912 | 01971 |
| | 02696 | 02758 | 03764 | | | | |
| .1 | 01876 | 01678 | | | | | |
| .100 | 01889 | 01351 | | | | | |
| .1000 | 01895 | 01136 | | | | | |
| .100K | 01902 | 01082 | 01149 | | | | |
| .140 | 01890 | 01354 | | | | | |
| .15 | 01880 | 01287 | 01293 | 01311 | 01347 | 01576 | 01694 |
| @.17 | 01881 | | | | | | |
| .170 | 01891 | 01697 | | | | | |
| .1700 | 01898 | 01270 | | | | | |
| .177 | 01892 | 01426 | 01739 | 01740 | | | |
| @.1777 | 01897 | | | | | | |
| .2 | 01877 | 01210 | 01360 | 01681 | | | |
| .20 | 01882 | 01126 | 01324 | 01421 | 01793 | | |

PAGE 0095
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|----------------|-------|-------|-------|-------|-------|-------|
| .207 | 01878 | 01109 | 01946 | | | | |
| @.21 | 01883 | | | | | | |
| .2100 | 01896 | 01087 | 01103 | | | | |
| .24 | 01884 | 01795 | | | | | |
| .377 | 01893 01804 | 01156 | 01243 | 01253 | 01749 | 01760 | 01764 |
| .40 | 01885 | 01222 | 01337 | 01433 | 01728 | | |
| .60 | 01886 | 01698 | 01721 | | | | |
| .604 | 01894 | 01930 | | | | | |
| .60K | 01899 | 01770 | | | | | |
| .6412 | 01887 | 01315 | 01563 | 01686 | | | |
| .7 | 01879 | 01703 | 01725 | | | | |
| .76K | 01900 | 01225 | 01269 | | | | |
| .77 | 01888 | 01545 | | | | | |
| .77NK | 01901 | 01679 | | | | | |
| .M1 | 01903 | 01118 | | | | | |
| @.M12 | 01905 | | | | | | |
| @.M20 | 01906 | | | | | | |
| .M6 | 01904 | 01715 | | | | | |
| .N20 | 01907 | 01276 | | | | | |
| .N64 | 01908 | 01822 | | | | | |
| @1 | 02632 | 01998 | 02028 | 02298 | 02310 | | |
| @10 | 02637 | 02111 | 02217 | 02226 | | | |
| @100 | 02638 | 02059 | 02171 | | | | |
| @@1000 | 02640 | | | | | | |
| @1005 | 02641 | 02328 | | | | | |
| @@100K | 02664 | | | | | | |
| @@12 | 02649 | | | | | | |

PAGE 0096

CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|--|
| @15 | 02650 | 02408 | | | | | | |
| @17 | 02651 | 02283 | 02343 | 02348 | | | | |
| @@170 | 02656 | | | | | | | |
| @1700 | 02659 | 02149 | | | | | | |
| @@177 | 02657 | | | | | | | |
| @2 | 02633 | 02331 | | | | | | |
| @200 | 02642 | 02397 | | | | | | |
| @2000 | 02646 | 02081 | 02130 | | | | | |
| @201 | 02643 | 02295 | | | | | | |
| @204 | 02644 | 02292 | | | | | | |
| @207 | 02645 | 02733 | | | | | | |
| @@21 | 02652 | | | | | | | |
| @2101 | 02647 | 02127 | | | | | | |
| @@24 | 02653 | | | | | | | |
| @3 | 02634 | 02301 | 02313 | | | | | |
| @377 | 02658 | 02338 | 02425 | 02430 | 02436 | 02444 | 02573 | |
| @@3770 | 02660 | | | | | | | |
| @@4 | 02635 | | | | | | | |
| @40 | 02654 | 02146 | 02204 | | | | | |
| @404 | 02661 | 02003 | | | | | | |
| @@6 | 02636 | | | | | | | |
| @60 | 02655 | 02303 | | | | | | |
| @604 | 02662 | 02716 | | | | | | |
| @@7 | 02648 | | | | | | | |
| @76K | 02663 | 02055 | 02058 | 02151 | 02159 | 02161 | 02165 | |
| @D256 | 02615 | 02199 | | | | | | |
| @M1 | 02665 | 02181 | 02190 | | | | | |

PAGE 0097
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| @M10 | 02668 | 02116 | 02183 | | | | |
| @M11 | 02669 | 02099 | | | | | |
| @M2 | 02666 | 02039 | 02585 | | | | |
| @M20 | 02670 | 02484 | 02607 | | | | |
| @M40 | 02671 | 02036 | | | | | |
| @@M6 | 02667 | | | | | | |
| @@N20 | 02672 | | | | | | |
| @N64 | 02673 | 02682 | 02689 | | | | |
| A | 00063 | 00139 | 00175 | 00176 | 00198 | 00218 | 00251 |
| | 00310 | 00393 | 00407 | 00409 | 00410 | 00413 | 00414 |
| | 00423 | 00438 | 00439 | 00446 | 00447 | 00504 | 00514 |
| | 00520 | 00521 | 00533 | 00539 | 00545 | 00596 | 00616 |
| | 00657 | 00660 | 00683 | 00728 | 00814 | 00935 | 00937 |
| | 00939 | 00941 | 01061 | 01088 | 01091 | 01105 | 01213 |
| | 01214 | 01227 | 01229 | 01233 | 01234 | 01249 | 01273 |
| | 01298 | 01302 | 01305 | 01352 | 01548 | 01696 | 01765 |
| | 01771 | 01814 | 01817 | 01827 | 02006 | 02009 | 02012 |
| | 02015 | 02082 | 02087 | 02119 | 02129 | 02131 | 02153 |
| | 02163 | 02168 | 02255 | 02368 | 02486 | 02588 | 02868 |
| | 02879 | 02880 | 03120 | 03130 | 03292 | 03302 | 03367 |
| | 03377 | 03458 | 03481 | 03575 | 03613 | 03614 | 03619 |
| | 03627 | 03635 | 03651 | 03655 | | | |
| AF AUS | 00999 | 00252 | | | | | |
| ALTO | 00994 | 00142 | 00143 | 00150 | 00151 | 00155 | 00162 |
| | 00285 | 00309 | 00436 | 00441 | 00736 | 00882 | 00897 |
| ALT1 | 00995 | 00132 | 00136 | 00138 | 00146 | 00154 | 00158 |
| | 00159 | 00190 | 00281 | 00287 | 00311 | 00444 | 00449 |
| ASR.0 | 01001 | 00261 | | | | | |
| ASR.1 | 01002 | 00273 | | | | | |
| B | 00064 | 00110 | 00134 | 00137 | 00189 | 00206 | 00244 |
| | 00317 | 00388 | 00428 | 00432 | 00435 | 00473 | 00566 |
| | 00575 | 00603 | 00611 | 00614 | 00619 | 00645 | 00650 |
| | 00656 | 00682 | 00692 | 00718 | 00726 | 00746 | 00755 |
| | 00803 | 00923 | 00931 | 00945 | 00954 | 01181 | 01266 |
| | 01297 | 01368 | 01418 | 01424 | 01430 | 01436 | 01480 |
| | 01586 | 01616 | 01620 | 01652 | 01700 | 01702 | 01709 |
| | 01720 | 01745 | 01756 | 01813 | 01825 | 02001 | 02005 |
| | 02027 | 02054 | 02070 | 02095 | 02110 | 02115 | 02134 |
| | 02182 | 02189 | 02198 | 02203 | 02206 | 02244 | 02269 |
| | 02291 | 02309 | 02337 | 02341 | 02346 | 02354 | 02388 |
| | 02399 | 02415 | 02419 | 02423 | 02429 | 02434 | 02440 |

PAGE 0098

CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|----------------|-------|-------|-------|-------|-------|-------|
| | 02443 | 02461 | 02538 | 02542 | 02559 | 02563 | 02577 |
| | 02586 | 02679 | 02711 | 02785 | 02915 | 02958 | 02981 |
| | 02984 | 02991 | 03005 | 03015 | 03023 | 03070 | 03088 |
| | 03092 | 03095 | 03103 | 03140 | 03173 | 03223 | 03262 |
| | 03265 | 03269 | 03287 | 03300 | 03327 | 03341 | 03408 |
| | 03430 | 03434 | 03474 | 03478 | 03491 | 03547 | 03559 |
| | 03566 | 03589 | 03593 | 03598 | 03603 | 03641 | 03648 |
| | 03662 | 03668 | 03676 | 03738 | 03751 | | |
| B1 | 00961 | 00205 | 00297 | | | | |
| B100 | 00975 | 00693 | 00993 | | | | |
| B1000 | 00980 | | | | | | |
| B100K | 00988 | 00179 | 00186 | 00576 | 00588 | | |
| B16K | 00986 | | | | | | |
| B17 | 00968 | 00361 | 00678 | | | | |
| B177 | 00976 | 00933 | | | | | |
| B1776 | 00981 | 00529 | 00541 | 00548 | | | |
| B1777 | 00982 | 00429 | 00544 | | | | |
| B2 | 00962 00835 | 00351 | 00378 | 00403 | 00467 | 00583 | 00700 |
| B20 | 00969 | 00457 | 00463 | | | | |
| B207 | 00978 | 00909 | 01031 | | | | |
| B24 | 00970 | 00149 | | | | | |
| B3 | 00963 | 00637 | 00667 | 00792 | 00925 | | |
| B3004 | 00983 | 00884 | | | | | |
| B37 | 00971 | 00476 | | | | | |
| B377 | 00977 | 00568 | 00898 | | | | |
| B4 | 00964 | 00669 | | | | | |
| B40 | 00972 | 00556 | 00992 | | | | |
| B5 | 00965 | 00390 | 00813 | | | | |
| B6 | 00966 | 00345 | 00362 | 00478 | 00552 | | |
| B604 | 00979 | 01014 | | | | | |
| B6412 | 00984 | 00278 | | | | | |

PAGE 0099
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|--|--|--|--|---|---|---|
| B7 | 00967 | 00779 | 00951 | | | | |
| B76K | 00987 00610 | 00276 | 00286 | 00530 | 00542 | 00558 | 00570 |
| B7777 | 00985 | 00283 | | | | | |
| BEAUS | 01000 | 00250 | | | | | |
| BIT5 | 00992 | 00465 | | | | | |
| BIT6 | 00993 | 00947 | | | | | |
| BIT9 | 02639 | 02270 | 02445 | 02462 | | | |
| BLK | 03729 | 03061 | 03082 | 03297 | 03741 | 03748 | |
| CH.OK | 01568 01458 01557 | 01440 01461 | 01443 01464 | 01446 01467 | 01449 01470 | 01452 01476 | 01455 01484 |
| CLM0 | 01223 | 01246 | | | | | |
| CLM1 | 01233 | 01239 | | | | | |
| CLM2 | 01247 | 01230 | 01236 | | | | |
| CLMEM | 01210 | 01397 | | | | | |
| CMDF | 02620 | 02478 | 02595 | 02605 | | | |
| CPUST | 00066 00379 01016 01761 02718 02927 | 00308 00553 01032 01790 02734 03357 | 00334 00638 01110 01799 02799 03793 | 00348 00872 01157 01931 02800 03809 | 00353 00904 01254 01947 02819 | 00359 00934 01683 02004 02866 | 00373 00949 01733 02144 02910 |
| CRLF | 01563 | 01135 | 01146 | 01589 | | | |
| CRSP1 | 02871 | 02818 | 02855 | 02891 | 02924 | | |
| CRSP2 | 03792 | 02847 | 02874 | 03535 | | | |
| CRSP3 | 01930 | 01319 | 01363 | | | | |
| CS%CM | 01812 | 01917 | | | | | |
| CS%FT | 01820 | 01918 | | | | | |
| CS%TR | 01799 | 01916 | | | | | |
| CS.CM | 01916 01818 | 01133 | 01747 | 01806 | 01808 | 01812 | 01816 |

PAGE 0100
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|-------------------------|-------------------------|-------------------------|-------------------------|----------------|----------------|----------------|
| CS.FT | 01917 | 01131 | 01327 | 01829 | 01830 | 01831 | |
| CS.TR | 01915 | 01382 | 01574 | 01802 | 01810 | | |
| CSVCP | 01134 | 01130 | 01326 | | | | |
| CTCWI | 03151 | 03123 | | | | | |
| CTCWO | 03152 | 03131 | | | | | |
| CTDP | 03055 | 03007 | | | | | |
| CTDPO | 03063 | 03081 | 03112 | | | | |
| CTDPL | 03091 | 03101 | | | | | |
| CTI%B | 03123 | 03783 | | | | | |
| CTI%W | 03115 | 03782 | | | | | |
| CTI.B | 03782 03115 | 02999 03118 | 03027 03127 | 03031 | 03034 | 03078 | 03110 |
| CTI.W | 03781 03136 | 03022 03139 | 03026 03777 | 03035 | 03038 | 03044 | 03121 |
| CTIO | 03783 | 03125 | 03133 | 03149 | | | |
| CTIO% | 03144 | 03784 | | | | | |
| CTL | 00068 02606 03400 | 00885 03124 03411 | 01138 03132 03442 | 01737 03330 03444 | 01767 03380 | 02481 03385 | 02596 03399 |
| CTLD | 02971 | 02822 | 02941 | 02961 | | | |
| CTLD. | 03003 | 02976 | | | | | |
| CTLDO | 03011 | 03046 | | | | | |
| CTLDF | 02977 | | | | | | |
| CTLDL | 03038 | 03043 | | | | | |
| CTLDX | 03049 | 03025 | | | | | |
| CTO%B | 03129 | 03785 | | | | | |
| CTO%W | 03136 | 03786 | | | | | |
| CTO.B | 03784 | 02993 | 03030 | 03109 | 03134 | 03138 | 03141 |
| CTO.W | 03785 03016 | 02978 03019 | 02982 03021 | 02989 03067 | 02996 03071 | 02998 03073 | 03012 03075 |

PAGE 0101

CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|----------------|----------------|----------------|----------------|----------------|----------------|-------|
| | 03077 03142 | 03086 | 03090 | 03098 | 03104 | 03117 | 03119 |
| CTRS | 03153 | 03024 | | | | | |
| DC%IN | 02226 | 02701 | | | | | |
| DC%RW | 02385 | 02702 | | | | | |
| DC.IN | 02700 02170 | 02049 02201 | 02053 02381 | 02113 02404 | 02150 02491 | 02152 02499 | 02154 |
| DC.RW | 02701 02208 | 02060 02256 | 02065 02290 | 02106 02357 | 02120 02524 | 02122 | 02174 |
| DCDCW | 02621 | 02393 | | | | | |
| DCER | 02708 02709 | 02047 | 02279 | 02495 | 02505 | 02523 | 02590 |
| DCERX | 02216 | 02048 | | | | | |
| DCFM | 02323 | 02307 | 02311 | 02314 | | | |
| DCL0 | 02486 | 02497 | | | | | |
| DCLD | 03532 | 02833 | 02947 | 02965 | | | |
| DCLD. | 02036 | 02029 | | | | | |
| DCLD1 | 02047 | 02025 | 02220 | | | | |
| DCLD2 | 02064 | 02173 | | | | | |
| DCLM. | 02103 | 02073 | | | | | |
| DCLM0 | 02144 | 02185 | | | | | |
| DCLM1 | 02174 | 02143 | | | | | |
| DCLM2 | 02190 | 02210 | | | | | |
| DCLMP | 02069 | 02057 | | | | | |
| DCLMU | 02149 | 02138 | | | | | |
| DCLMW | 02170 | 02094 | 02101 | | | | |
| DCLMX | 02211 | 02148 | 02177 | 02192 | 02306 | | |
| DCSFS | 02496 | 02487 | 02489 | | | | |
| DCTYP | 02622 | 02288 | | | | | |
| DFL | 01838 | 01123 | | | | | |

PAGE 0102
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DFL. | 01843 | 01370 | | | | | |
| DMA | 00827 | 00774 | 00776 | 00778 | 00815 | 00829 | |
| DMACF | 00829 | 00772 | 00812 | | | | |
| DMACW | 00828 | 00775 | 00777 | 00785 | 00789 | | |
| DONE | 01014 | 00367 | 00906 | 00910 | | | |
| DR | 00067 | 00724 | 00731 | 00883 | 00886 | 00889 | 00896 |
| | 01139 | 01140 | 01144 | 01775 | 01776 | 01777 | 01784 |
| | 01820 | 01821 | 01823 | 02572 | 02578 | 02579 | 02583 |
| | 02584 | 02591 | 02609 | 02611 | 03144 | 03145 | 03146 |
| | 03148 | 03181 | 03222 | 03232 | 03283 | 03290 | 03295 |
| | 03296 | 03298 | 03331 | 03333 | 03345 | 03346 | 03379 |
| | 03387 | 03398 | 03401 | 03421 | 03432 | 03439 | 03451 |
| | 03499 | | | | | | |
| DS%B | 03279 | 03772 | | | | | |
| DS%CM | 03286 | 03773 | | | | | |
| DS%FT | 03295 | 03310 | 03775 | | | | |
| DS%GO | 03228 | 03215 | | | | | |
| DS%GT | 03214 | 03774 | | | | | |
| DS%WF | 03308 | 03776 | | | | | |
| DS.B | 03771 | 03246 | 03248 | 03267 | 03270 | 03284 | |
| DS.CM | 03772 | 03249 | 03251 | 03253 | 03286 | 03291 | 03293 |
| DS.FT | 03774 | 03177 | 03219 | 03226 | 03240 | 03281 | 03288 |
| | 03304 | 03305 | 03306 | 03309 | | | |
| DS.GT | 03773 | 03187 | 03192 | 03195 | 03201 | 03207 | 03233 |
| DS.WF | 03775 | 03168 | 03182 | 03230 | 03308 | | |
| DSDNL | 03766 | 03176 | | | | | |
| DSDUN | 03207 | 03190 | | | | | |
| DSEX | 03211 | 03205 | 03277 | | | | |
| DSINR | 03252 | 03218 | | | | | |
| DSL D | 03166 | 02821 | 02830 | 02945 | 02967 | | |
| DSPLY | 00931 | 00468 | 00479 | 00915 | 00920 | 00948 | 00955 |

PAGE 0103
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| DSRD | 03187 | 03203 | | | | | |
| DSRDL | 03195 | 03200 | | | | | |
| DSVCP | 03312 | 03239 | | | | | |
| DSWEX | 03276 | 03256 | | | | | |
| DSWR | 03237 | 03175 | | | | | |
| DSWR0 | 03245 | 03274 | | | | | |
| DSWR1 | 03261 | 03273 | | | | | |
| DTYER | 02303 | 02317 | | | | | |
| DTYPE | 02336 | 02293 | 02296 | 02299 | | | |
| DV4 | 01004 | 00289 | | | | | |
| EMERR | 00472 | 00434 | | | | | |
| EOP0 | 01008 | 01010 | | | | | |
| EOP1 | 01910 | 01913 | | | | | |
| EOP2 | 02694 | 02697 | | | | | |
| EOP3 | 03762 | 03765 | | | | | |
| EXECU | 01253 | 01399 | | | | | |
| EXIT | 01152 | 01391 | | | | | |
| EXITN | 01191 | 01184 | | | | | |
| EXITS | 01148 | 01393 | | | | | |
| EXRM | 02857 | 02851 | | | | | |
| HLT77 | 02907 | 02898 | | | | | |
| HPIB | 02706 | 02247 | 02271 | 02332 | 02420 | 02426 | 02431 |
| | 02441 | 02446 | 02463 | 02509 | 02540 | 02543 | 02561 |
| | 02564 | 02569 | 02593 | | | | |
| HPIB% | 02583 | 02707 | | | | | |
| I%0 | 01775 | 01920 | | | | | |
| I%0.0 | 01777 | 01783 | | | | | |
| I%0.1 | 01784 | 01778 | | | | | |
| I.0 | 01919 | 01738 | 01768 | 01772 | 01785 | 01815 | |

PAGE 0104
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|-------------------------|-------------------------|-------------------------|----------------|----------------|----------------|----------------|
| IDM | 00974 | 00869 | | | | | |
| ILINT | 00917 | 00092 | 00800 | | | | |
| IN%N | 01690 | 01924 | | | | | |
| IN%NO | 01693 | 01712 | | | | | |
| IN.N | 01923 | 01278 | 01346 | 01575 | 01695 | 01701 | |
| IN1C | 01918 01693 | 01261 01746 | 01264 01750 | 01291 01752 | 01383 01755 | 01388 | 01415 |
| IN1C% | 01733 | 01919 | | | | | |
| IN1C0 | 01747 | 01735 | | | | | |
| INQ | 01365 | 01565 | 01571 | | | | |
| INQ!? | 01559 01741 | 01313 | 01349 | 01410 | 01543 | 01583 | 01667 |
| INQ# | 01423 | 01685 | 01688 | | | | |
| INQ. | 01381 | 01367 | 01584 | | | | |
| INQ.0 | 01412 | 01387 | | | | | |
| INQ.1 | 01433 | 01380 | 01422 | | | | |
| INQ.2 | 01488 | 01473 | | | | | |
| INQ.3 | 01556 01550 | 01497 01552 | 01500 01554 | 01503 | 01506 | 01509 | 01541 |
| INQDM | 01544 | 01518 | 01521 | | | | |
| INQLF | 01561 | 01334 | 01342 | 01355 | | | |
| INQRC | 01553 | 01513 | | | | | |
| INQRD | 01551 | 01511 | | | | | |
| INQRS | 01555 | 01515 | | | | | |
| INORX | 01542 | 01493 | | | | | |
| IOE4 | 00669 | 00654 | | | | | |
| IOER | 00924 | 00391 | 00668 | 00670 | 00701 | 00708 | 00853 |
| IOESC | 00922 00765 00820 | 00720 00783 00894 | 00730 00787 00900 | 00734 00791 | 00748 00797 | 00757 00805 | 00761 00817 |

PAGE 0105
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| IOINT | 00799 | 00095 | | | | | |
| IOL0 | 00642 | 00659 | | | | | |
| IOL1 | 00657 | 00665 | | | | | |
| IOL2 | 00680 | 00688 | 00699 | | | | |
| IOL3 | 00683 | 00690 | | | | | |
| IOL4 | 00711 | 00825 | | | | | |
| IOL5 | 00842 | 00851 | 00856 | | | | |
| IOLP | 00959 | 00618 | | | | | |
| ION0 | 00675 | 00648 | | | | | |
| ION1 | 00691 | 00685 | | | | | |
| ION2 | 00705 | 00694 | | | | | |
| ION2A | 00736 | 00722 | | | | | |
| ION3 | 00835 | 00713 | | | | | |
| ION4 | 00848 | 00845 | | | | | |
| ION5 | 00858 | 00847 | | | | | |
| ION6 | 00902 | 00861 | 00864 | 00871 | | | |
| IPF | 00516 | 00086 | 00953 | | | | |
| IPRTY | 00484 | 00087 | | | | | |
| ITBG | 00342 | 00088 | | | | | |
| JMP.2 | 02919 | 02900 | | | | | |
| LDCON | 02934 | 02805 | | | | | |
| LDEX | 02876 | 02955 | 02968 | 03002 | 03047 | 03051 | 03053 |
| | 03065 | 03113 | 03169 | 03178 | 03183 | 03209 | 03212 |
| | 03220 | 03227 | 03231 | 03241 | 03258 | 03282 | 03289 |
| | 03362 | 03391 | 03394 | 03470 | 03508 | 03564 | 03572 |
| | 03787 | | | | | | |
| LDEX0 | 02909 | 02897 | | | | | |
| LDEX1 | 02917 | 02913 | | | | | |
| LDP2 | 02027 | 02719 | | | | | |

PAGE 0106

CROSS-REFERNCE SYMBOL TABLE

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| LDR | 02790 | 02783 | 02930 | 02953 | | | |
| LDRC | 02811 | 02808 | 02936 | | | | |
| LDRC0 | 02823 | 02814 | | | | | |
| LDRC1 | 02826 | 02812 | | | | | |
| LDRC2 | 02831 | 02827 | | | | | |
| LDRER | 02921 | 02816 | 02824 | 02829 | 02832 | 02840 | 02843 |
| | 02854 | 02894 | 02948 | | | | |
| LDRR | 02952 | 03794 | | | | | |
| LDRSX | 02865 | 02810 | 02852 | | | | |
| @LDRTC | 01329 | | | | | | |
| @LDRTE | 01335 | | | | | | |
| LDRTN | 01321 | 01932 | | | | | |
| LTB | 01495 | 01546 | | | | | |
| LOAD | 01261 | 01401 | 01403 | 01405 | | | |
| LOAD0 | 01291 | 01309 | | | | | |
| LOAD1 | 01295 | 01289 | | | | | |
| LOAD2 | 01310 | 01282 | 01284 | | | | |
| LOADC | 01315 | 01288 | 01294 | | | | |
| LSN | 02619 | 02246 | 02539 | | | | |
| M1 | 00989 | 00168 | 00180 | 00590 | | | |
| M2 | 00990 | 00169 | | | | | |
| M20 | 00991 | 00652 | 00723 | | | | |
| MAPST | 01346 | 01407 | | | | | |
| MTST | 00373 | 00085 | 00364 | | | | |
| MTST0 | 00404 | 00505 | 00523 | 00560 | 00573 | | |
| MTST1 | 00507 | 00415 | | | | | |
| MTST2 | 00520 | 00508 | | | | | |
| MTST3 | 00575 | 00431 | 00550 | 00569 | | | |

PAGE 0107
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|----------------------------------|-------------------------|
| MTST4 | 00586 | 00486 | | | | | |
| MTST5 | 00608 | 00601 | | | | | |
| MTSTE | 00419 | 00412 | 00488 | 00584 | | | |
| MTSTM | 00562 | 00525 | | | | | |
| MU2 | 01003 | 00282 | | | | | |
| N250 | 02614 | 02232 | | | | | |
| OU%1C | 01760 | 01922 | | | | | |
| OU%2C | 01752 | 01921 | | | | | |
| OUT%N | 01714 | 01923 | | | | | |
| OUT.N | 01922 | 01341 | 01568 | 01730 | | | |
| OUT1C | 01921 01729 | 01338 01743 | 01379 01754 | 01428 01757 | 01431 01769 | 01434 01773 | 01722 |
| OUT2C | 01920 01742 | 01316 01744 | 01333 01758 | 01336 01805 | 01560 | 01564 | 01687 |
| OUTNO | 01718 | 01727 | | | | | |
| P0 | 00065 00959 01042 01049 | 00212 00960 01043 01050 | 00213 01037 01044 01051 | 00617 01038 01045 01052 | 00809 01039 01046 01053 | 00827 01040 01047 01054 | 00829 01041 01048 |
| P0.A | 01042 | 00629 | 00824 | 01025 | 01028 | | |
| P0.B | 01043 | 00631 | | | | | |
| P0.CT | 01037 00959 | 00536 | 00543 | 00679 | 00680 | 00687 | 00691 |
| @P0.DF | 01050 | | | | | | |
| @P0.E | 01044 | | | | | | |
| @P0.EM | 01049 | | | | | | |
| @P0.FL | 01052 | | | | | | |
| @P0.GF | 01046 | | | | | | |
| P0.T | 01048 | 01030 | | | | | |
| @P0.M | 01047 | | | | | | |
| @P0.O | 01045 | | | | | | |

PAGE 0108
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|----------------|----------------|
| @P0.SB | 01053 | | | | | | |
| @P0.SC | 01054 | | | | | | |
| P0.T0 | 01041 00711 00922 | 00620 00823 | 00643 00837 | 00644 00850 | 00658 00854 | 00662 00859 | 00710 00862 |
| P0.T1 | 01040 | 00622 | 00655 | 00681 | 00705 | 00709 | 00836 |
| P0.T2 | 01039 | 00839 | 00855 | 00858 | | | |
| P0.T3 | 01038 | 00555 | 00605 | | | | |
| @P0.UN | 01051 | | | | | | |
| POCL2 | 00399 | 00394 | | | | | |
| POCO0 | 00401 | 00398 | | | | | |
| POJPO | 00398 | 00392 | | | | | |
| POVCP | 01021 | 00960 | 01033 | | | | |
| P1 | 01057 01958 01965 | 01952 01959 01966 | 01953 01960 01967 | 01954 01961 01968 | 01955 01962 01969 | 01956 01963 | 01957 01964 |
| P1.A | 01957 | 01180 | 01438 | 01597 | 01940 | 01943 | |
| P1.B | 01958 | 01071 | 01182 | 01441 | 01599 | | |
| P1.CT | 01952 | 01277 | 01308 | 01716 | 01726 | | |
| P1.DF | 01965 01569 | 01124 | 01271 | 01314 | 01365 | 01372 | 01562 |
| P1.E | 01959 | 01074 | 01168 | 01453 | 01601 | | |
| P1.EM | 01964 01373 | 01102 01462 | 01177 01607 | 01179 | 01185 | 01191 | 01204 |
| @P1.FL | 01967 | | | | | | |
| P1.GF | 01961 01609 | 01083 01631 | 01162 | 01205 | 01207 | 01465 | 01488 |
| P1.I | 01963 01605 | 01174 01945 | 01176 | 01187 | 01193 | 01202 | 01459 |
| P1.M | 01962 01625 | 01120 01672 | 01468 01675 | 01474 01682 | 01477 | 01612 | 01617 |
| P1.O | 01960 | 01078 | 01171 | 01456 | 01603 | | |

PAGE 0109
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|-------|-------|-------|-------|-------|-------|-------|
| @P1.SB | 01968 | | | | | | |
| @P1.SC | 01969 | | | | | | |
| P1.T0 | 01956 | 01089 | 01104 | 01153 | 01183 | 01279 | 01286 |
| | 01292 | 01299 | 01378 | 01384 | 01389 | 01416 | 01419 |
| | 01423 | 01429 | 01435 | 01585 | 01651 | 01658 | |
| P1.T1 | 01955 | 01093 | 01106 | 01155 | 01190 | 01197 | 01350 |
| | 01587 | 01610 | 01633 | 01691 | 01704 | 01710 | 01719 |
| | 01723 | | | | | | |
| P1.T2 | 01954 | 01263 | 01265 | 01267 | 01318 | | |
| P1.T3 | 01953 | 01275 | 01295 | 01307 | 01572 | 01653 | 01659 |
| @P1.UN | 01966 | | | | | | |
| P1ERR | 01924 | 01330 | 01339 | | | | |
| P2 | 01972 | 02164 | 02738 | 02740 | 02741 | 02742 | 02743 |
| | 02744 | 02745 | 02746 | 02747 | 02748 | 02749 | 02750 |
| | 02751 | 02752 | 02753 | 02754 | 02755 | 02756 | |
| P2.A | 02744 | 02078 | 02092 | 02139 | 02727 | 02730 | |
| P2.B | 02745 | 02085 | 02096 | 02140 | 02178 | | |
| P2.CT | 02738 | 02024 | 02040 | 02108 | 02219 | | |
| P2.DF | 02752 | 02021 | 02023 | 02166 | 02169 | | |
| @P2.F | 02746 | | | | | | |
| @P2.EM | 02751 | | | | | | |
| P2.FL | 02754 | 02013 | 02042 | 02044 | 02109 | 02112 | 02114 |
| | 02117 | 02197 | 02200 | 02304 | 02351 | 02359 | |
| @P2.GF | 02748 | | | | | | |
| P2.HC | 02710 | 02061 | 02345 | 02371 | 02376 | 02421 | 02427 |
| P2.I | 02750 | 02732 | | | | | |
| @P2.M | 02749 | | | | | | |
| @P2.O | 02747 | | | | | | |
| P2.SB | 02755 | 02007 | 02243 | 02537 | 02558 | | |
| @P2.SC | 02756 | | | | | | |
| P2.ST | 02709 | 02063 | 02340 | 02361 | 02367 | 02379 | 02380 |

PAGE 0110
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|----------------------------------|----------------------------------|----------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
| | 02433 | 02442 | | | | | |
| P2.T0 | 02743 | 02018 | 02069 | 02389 | 02685 | | |
| P2.T1 | 02742 | 02350 | 02355 | 02360 | 02366 | 02370 | 02377 |
| P2.T2 | 02741 | 02019 | 02037 | | | | |
| P2.T3 | 02740 | 02235 | 02319 | 02329 | 02414 | 02437 | |
| P2.UN | 02753 | 02010 | 02268 | 02418 | 02439 | 02460 | |
| P2C | 02698 02428 | 02016 02680 | 02046 02688 | 02188 02691 | 02202 02692 | 02205 | 02422 |
| P2C% | 02679 | 02700 | | | | | |
| P2ERR | 02711 02227 02483 | 02031 02240 02503 | 02066 02261 02506 | 02212 02277 02515 | 02216 02323 02521 | 02218 02409 | 02221 02450 |
| P2VCO | 02733 | 02735 | | | | | |
| @P2VCP | 02723 | | | | | | |
| P3 | 02759 03815 03822 03829 | 03378 03816 03823 03830 | 03605 03817 03824 03831 | 03628 03818 03825 | 03636 03819 03826 | 03684 03820 03827 | 03814 03821 03828 |
| P3.A | 03819 | 03091 | 03261 | 03755 | 03802 | 03805 | |
| P3.B | 03820 | 03093 | 03263 | 03757 | | | |
| P3.CT | 03814 03225 03425 03623 | 03033 03260 03426 | 03042 03272 03441 | 03083 03334 03462 | 03100 03389 03466 | 03185 03407 03467 | 03214 03413 03617 |
| P3.DF | 03827 | 02795 | 02889 | 02895 | 02916 | 03671 | 03677 |
| @P3.E | 03821 | | | | | | |
| @P3.EM | 03826 | | | | | | |
| P3.FL | 03829 03318 03577 | 02974 03320 03582 | 02983 03343 | 03010 03418 | 03029 03435 | 03049 03544 | 03180 03552 |
| @P3.GF | 03823 | | | | | | |
| P3.I | 03825 | 03807 | | | | | |
| @P3.M | 03824 | | | | | | |

PAGE 0111
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|---|---|---|----------------------------------|----------------------------------|----------------------------------|----------------------------------|
| AP3.0 | 03822 | | | | | | |
| P3.SB | 03830 | 03057 | 03591 | | | | |
| P3.SC | 03831 03600 | 02796 03604 | 02914 | 03561 | 03565 | 03573 | 03586 |
| P3.T0 | 03818 03099 03322 03438 | 02793 03172 03326 03744 | 03004 03193 03340 03752 | 03036 03244 03347 03758 | 03060 03264 03422 03759 | 03087 03268 03429 | 03094 03271 03433 |
| P3.T1 | 03817 03045 03452 | 02959 03089 03460 | 02987 03096 03498 | 02990 03097 03510 | 03037 03102 | 03040 03191 | 03041 03199 |
| P3.T2 | 03816 | 02794 | 02886 | | | | |
| P3.T3 | 03815 03202 | 03062 03630 | 03063 | 03105 | 03194 | 03197 | 03198 |
| P3.UN | 03828 | 02973 | 02980 | 03014 | 03069 | 03595 | |
| P3C | 03767 03739 | 03039 03760 | 03196 | 03388 | 03464 | 03477 | 03480 |
| P3C% | 03738 | 03769 | | | | | |
| P3C%0 | 03759 | 03750 | | | | | |
| P3ERR | 03786 03056 03229 | 02797 03170 03238 | 02877 03171 03242 | 02892 03179 03541 | 02957 03211 03680 | 03003 03217 | 03052 03221 |
| P3VCO | 03808 | 03810 | | | | | |
| P3VCP | 03798 | 03684 | | | | | |
| PHI | 02705 02412 02518 02554 02599 | 02228 02455 02529 02556 02601 | 02230 02458 02531 02570 02603 | 02248 02471 02533 02576 | 02266 02473 02535 02580 | 02274 02485 02550 02581 | 02326 02488 02552 02597 |
| PHI% | 02576 | 02706 | | | | | |
| PHI%I | 02568 | 02705 | | | | | |
| PHI%L | 02550 | 02704 | | | | | |
| PHI%T | 02529 | 02703 | | | | | |
| PHI.I | 02704 02574 | 02250 | 02253 | 02276 | 02280 | 02281 | 02520 |

PAGE 0112
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PHI.L | 02703 | 02241 | 02252 | 02254 | 02272 | 02289 | 02294 |
| | 02297 | 02300 | 02312 | 02315 | 02336 | 02469 | 02516 |
| | 02562 | 02565 | 02566 | | | | |
| PHI.T | 02702 | 02262 | 02264 | 02324 | 02410 | 02451 | 02466 |
| | 02541 | 02544 | 02545 | | | | |
| PHIF% | 02595 | 02708 | | | | | |
| PHIFL | 02707 | 02236 | 02284 | 02308 | 02511 | 02610 | |
| PIN | 02604 | 02568 | | | | | |
| PRDER | 00914 | 00321 | 00324 | 00327 | 00332 | 00340 | 00347 |
| | 00350 | 00355 | | | | | |
| PRST | 01200 | 01132 | 01143 | 01216 | 01251 | 01395 | 01782 |
| PRTL | 00949 | 00944 | | | | | |
| PTDF0 | 00212 | 00204 | 00207 | | | | |
| PTDF1 | 00213 | 00201 | | | | | |
| PTJMP | 00215 | 00209 | | | | | |
| PTJPR | 00214 | 00197 | | | | | |
| PTRT0 | 00201 | 00213 | 00214 | | | | |
| PTST | 01359 | 01409 | | | | | |
| ORAP0 | 01010 | | | | | | |
| ORAP1 | 01913 | | | | | | |
| ORAP2 | 02697 | | | | | | |
| ORAP3 | 03765 | | | | | | |
| RESUA | 01005 | 00290 | | | | | |
| RESUB | 01006 | 00294 | | | | | |
| REV | 00081 | 00630 | | | | | |
| RM%SC | 03514 | 03771 | | | | | |
| RM%TR | 03486 | 03770 | | | | | |
| RM.TR | 03769 | 03456 | 03459 | 03483 | 03512 | | |
| RM1K | 03526 | 03453 | | | | | |
| RM31K | 03527 | 03457 | | | | | |

PAGE 0113
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|-------------------------|----------------|----------------|----------------|----------------|----------------|----------------|
| RMADR | 02869 | 02864 | | | | | |
| ARMADX | 03528 | | | | | | |
| RMCW | 03525 | 03487 | | | | | |
| RMLD | 03316 | 02825 | 02943 | 02963 | | | |
| RMLD0 | 03322 | 03329 | 03344 | 03431 | 03436 | | |
| RMLD1 | 03330 | 03324 | 03410 | | | | |
| RMLD2 | 03379 | 03352 | 03356 | 03386 | 03390 | 03445 | |
| RMLD3 | 03393 | 03336 | 03417 | 03476 | 03517 | 03522 | |
| RMLD4 | 03398 | 03338 | | | | | |
| RMLD5 | 03432 | 03415 | | | | | |
| RMLDE | 03361 | 03450 | | | | | |
| RMLX | 03447 | 03420 | | | | | |
| RMLX0 | 03465 | 03484 | | | | | |
| RMNSC | 03770 | 03325 | 03383 | 03423 | 03471 | 03523 | |
| RP%SC | 01787 | 01915 | | | | | |
| RP.SC | 01914 | 01111 | 01323 | 01542 | 01556 | 01650 | 01797 |
| RTNP3 | 02716 | 02032 | 02067 | 02213 | 02222 | | |
| S%SC | 03539 | 03781 | | | | | |
| S%SC0 | 03555 | 03543 | | | | | |
| S%SC1 | 03558 | 03546 | 03554 | | | | |
| S%SC2 | 03561 | 03551 | 03557 | | | | |
| S%SC3 | 03630 | 03624 | | | | | |
| S%SC4 | 03633 | 03616 | | | | | |
| S%SC5 | 03650 | 03660 | | | | | |
| S.SC | 03776 03368 03681 | 02971 03532 | 03166 03558 | 03316 03596 | 03348 03661 | 03364 03669 | 03366 03678 |
| SCM | 00973 | 00649 | | | | | |

PAGE 0114
 CROSS-REFERENCE SYMBOL TABLE

| | | | | | | | |
|--------|----------------|----------------|-------|-------|-------|-------|-------|
| SPCL | 02835 | 02803 | | | | | |
| SPCL0 | 02842 | 02838 | | | | | |
| SPCL1 | 02848 | 02836 | | | | | |
| SPCL2 | 02853 | 02849 | | | | | |
| SRGP1 | 00996 | 00217 | | | | | |
| SRGP2 | 00997 | 00219 | 00245 | | | | |
| SRGP3 | 00998 | 00241 | | | | | |
| ST.N | 01585 | 01577 | 01669 | | | | |
| ST.N0 | 01658 | 01579 | 01581 | | | | |
| ST.N1 | 01670 | 01655 | | | | | |
| ST.N2 | 01683 | 01656 | | | | | |
| ST.NA | 01651 | 01622 | | | | | |
| @START | 00099 | | | | | | |
| STS | 00069 01649 | 00881 01779 | 00893 | 00895 | 01113 | 01137 | 01555 |
| TCCWI | 01835 | 01736 | | | | | |
| TCCWO | 01836 | 01766 | | | | | |
| TLK | 02618 | 02245 | 02560 | | | | |
| TR1K | 02616 | 02103 | | | | | |
| TR31K | 02617 | 02118 | | | | | |
| TST | 02846 | 02841 | | | | | |
| UNL | 02534 | 02507 | | | | | |
| VCP | 01071 | 01948 | | | | | |
| VCP0 | 01109 | 01208 | 01322 | 01328 | | | |
| VCP1 | 01136 | 01127 | | | | | |
| VCPD | 00960 | 00383 | 00612 | | | | |
| @VCPD3 | 03684 | | | | | | |
| ZERO | 00080 | 00300 | | | | | |

| | |
|--|------------|
| APPLICATION INFORMATION FOR 25 KHz POWER | APPENDIX B |
|--|------------|

This appendix provides application information on the 25 kHz sine-wave output of the HP 12035A Power Supply.

Introduction

HP 1000 L-Series Computers and Systems utilize the Model 12035A Power Module as their power supply. An important design factor in the 12035A Power Module is the inversion of 50/60 Hz ac power to a regulated 25 kHz sine wave that is stepped down and rectified to provide the outputs shown in Figure 1. A bonus of this design for the OEM or end user with unique power requirements that are not met by the standard dc voltages is the availability of 25 kHz ac power at the backplane of L-Series card cages, computers, and systems and at a connector on the front of the power module. At the 25 kHz frequency, power transformers and filtering components (capacitors and chokes) can be small and lightweight enough to make possible on-interface power supplies.

Uses of 25 kHz backplane power

25 kHz backplane power can be used when designing special interfaces on the 12010A Breadboard Interface to provide ac input power for compact, lightweight on-interface dc power supplies to meet any of the following requirements:

1. Provision of dc voltages in addition to those supplied by the 12035A Power Module.
2. Provision of dc supplies whose analog grounds are isolated from the computer ground.
3. Provision of multichannel isolated power to digital communication circuits to eliminate ground noise paths and maximize the reliability of serial data transfers.
4. Low voltage, high current power for supplying large arrays of integrated circuits.

Use of 25 kHz power from the power module front connector

25 kHz power is conveniently available from the power module front connector for powering circuits that are separate from the computer or system backplane. Uses might include signal conditioning power to external sensors (such as strain gauges) or power for logic circuits external to the computer backplane. Use of the power module's 25 kHz ac output can eliminate the need for separate, 50/60 Hz power supplies where external power requirements are small, minimizing costs, space requirements, and weight.

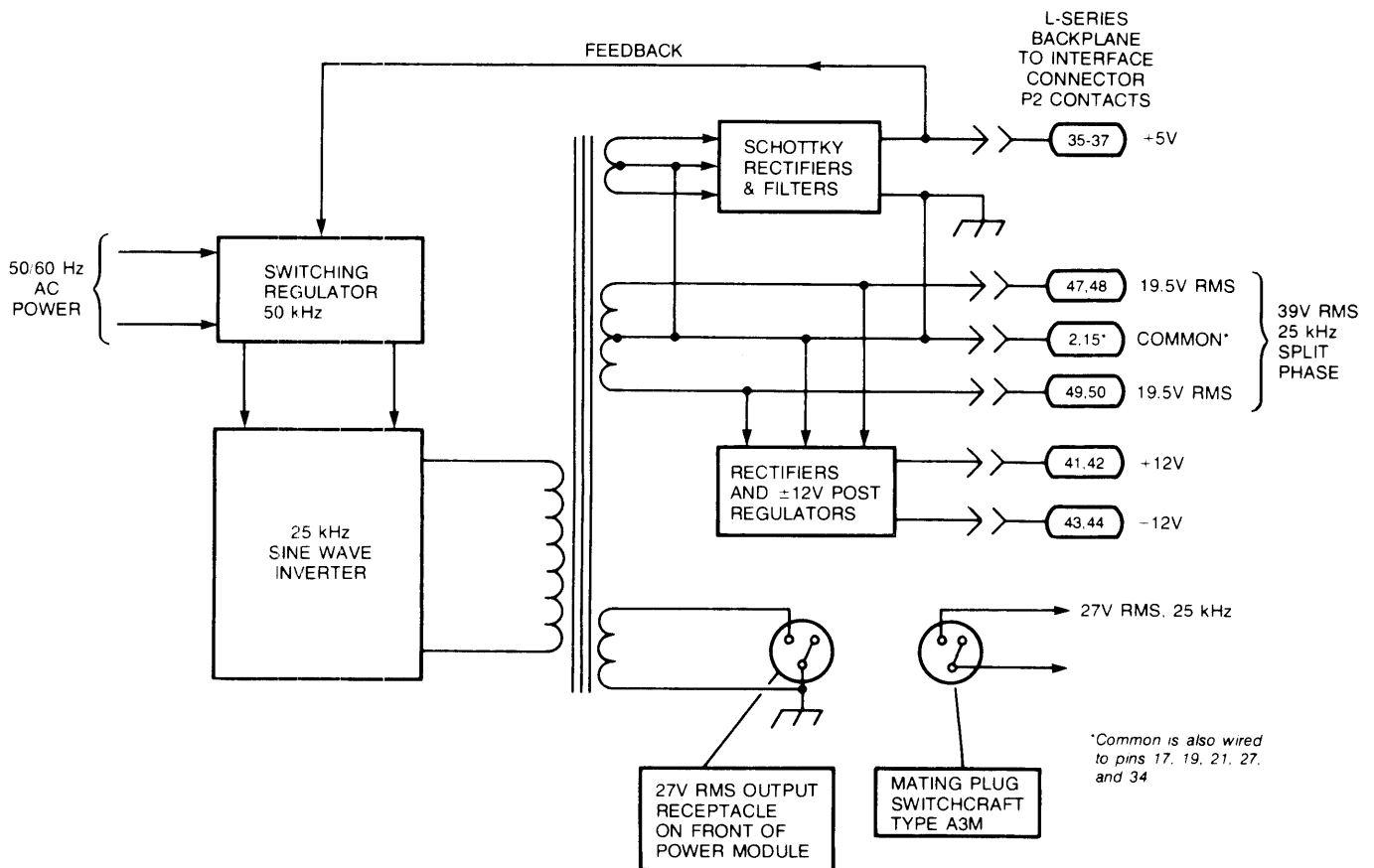


Figure 1. 12035A Power Module, Simplified

25 kHz ac power specifications of the 12035A Power Module

39V rms split-phase backplane output: The power module's output to the backplane of L-Series card cages, computers, and systems includes 39V rms split phase across pins 47/48 and 49/50 of interface card printed circuit plug P2 with a center tap connected to common (pins 2, 15, 17, 19, 21, 27, 29, and 34 of P2), as shown in Figure 1. With respect to common, the voltages at pins 47/48 and 49/50 of plug P2 are 19.5V rms. This backplane output is conveniently available for powering small on-interface dc power supplies.

27V rms front connector output: A separate transformer winding provides a 27V rms single-phase output to a connector on the front of the power module. This output can be used for signal conditioning power to external sensors or for other small external power supply uses. A Switchcraft type A3M plug is the required mating connector for this output.

Regulation: Within $\pm 8\%$ of nominal.

Available power: 25 kHz power available from either output or total available from both outputs depends on usage of dc current from the 12035A Power Module, as follows:

| AC Power | +5Vdc | +12Vdc | -12Vdc |
|----------|-------|--------|--------|
| 70 Watts | 25A | 4.0A | 2.0A |

NOTE: Alternate ac power and dc current output combinations are possible within the 250W to 319W maximum total power output, provided that no more than the highest power or current listed above is drawn from any output. However, because of complex thermal interactions within the power module you cannot rely upon directly trading all of the power not used in one or more dc outputs for additional ac power.

On-interface dc power supplies

Non-isolated, series-regulated dc power supply (Use 1 from page 1)

Purpose and basic design. Where additional +7.5V to +12V dc at up to 1 amp is needed for interface circuits, the 25 kHz backplane power can be used to provide a non-isolated positive regulated power supply as shown in Figure 2. The 19.5V rms potential on either side of common provides at least +14.5V dc after rectification and filtering. An adjustable, off-the-shelf, three-terminal integrated circuit voltage regulator, National Semiconductor Series LM117 or equivalent, can be used to set the regulated output voltage within the range of +7.5V to +12V dc. The regulated voltage output is dependent upon the values of resistors R2 and R3. A negative output voltage supply similar to the

positive supply shown in Figure 2 can be made by reversing polarities of the rectifiers and using a negative adjustable regulator, National Semiconductor Series LM137 or equivalent.

Preserving purity of the 25 kHz ac input sine wave. To maintain the purity of the input 25 kHz sine wave, near 180 degree conduction should be provided in the rectification process, which necessitates the use of a choke input filter. This filter also limits the surge current at turn-on if the requirements for L_{min} are met. The equation for L_{min} with a 25% safety factor is given by:

$$L_{min} \text{ (in henries)} = (K/fs) \times R_L$$

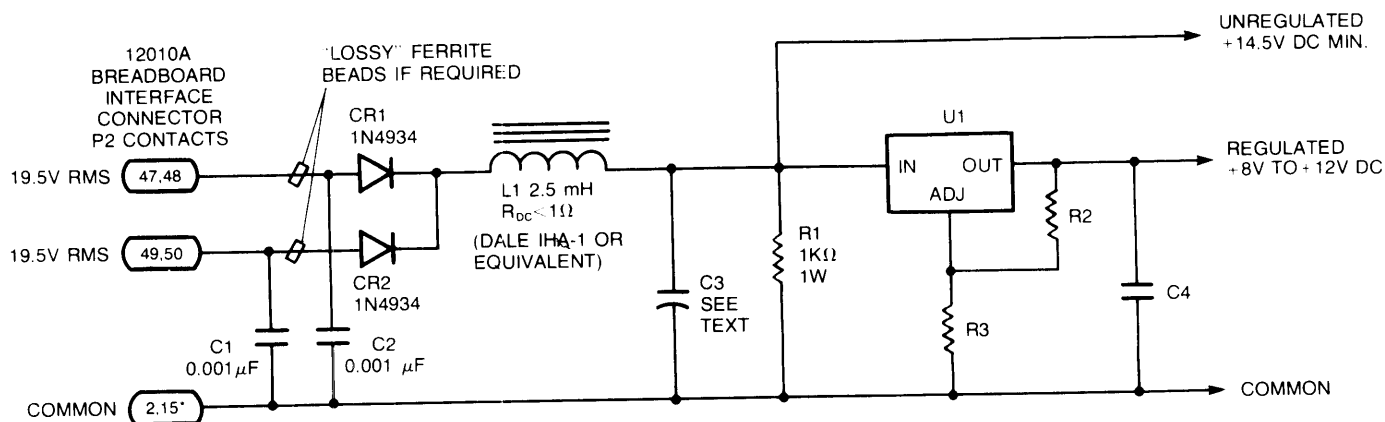
Where: $f_s = 25 \text{ kHz}$

$R_L = \text{Minimum load resistance}$

$K = 0.06 \text{ for full wave rectifiers}$

This implies the need for a minimum load. If the circuits to be powered allow the load current to go to zero, a preloading bleeder resistor is required. The final value of L_{min} would then be determined by the allowed power loss (dissipation) of the preloading resistor. When the L_{min} requirement is met, the surge current will be acceptable and sine wave distortion will be minimized.

Selection of rectifiers. Rectifiers used with 25 kHz input power must be of the fast recovery type with less than 200 nanosecond recovery time. Allowing for possible transients from leakage inductances, overshoot, and MTBF derating, the rectifiers should also have 100V peak inverse voltage rating.



NOTES: U1 is a National Semiconductor type LM117 Series or equivalent adjustable regulator.
Values of C4, R2, and R3 should be selected in accordance with instructions in U1 manufacturer's data sheet.

Figure 2. On-interface regulated power supply with up to 1A output using 25 kHz ac input from L-Series backplane

Keeping noise off the 25 kHz ac input lines.

During rectifier recovery, the removal of stored charge in the rectifiers will appear as spikes on the rectifier inputs. These spikes should be suppressed to keep them from travelling along the 25 kHz ac input lines in the backplane. Small 0.001 to 0.1 microfarad ceramic capacitors (C1 and C2 in Figure 2) will usually damp out these spikes, with the required capacitor value dependent upon the magnitude of stored charge being removed. If underdamped ringing is present because of leakage inductance, small ferrite beads, tubes, or toroids can be threaded onto the rectifier leads to provide a "lossy" inductive reactance at high frequencies to effectively dissipate undesirable recovery currents.

Input filtering. The value of C3 is determined by the amount of ripple voltage that can be tolerated at the input of integrated circuit regulator U1. The Vin-Vout differential of 3 volts must be met for any chosen output voltage as noted in Reference 2. The Ripple factor r for a full-wave rectifier circuit is given by:

$$r = (0.83 / (L_1 \times C_1)) \times 5.76 \times 10^{-6}$$

The case size and construction of capacitor C3 must be capable of conducting the ripple current without excessive dissipation. Ripple current will be at 2 fs and will be sinusoidal when Lmin requirements are met. The rms ripple current in amps is given by:

$$I_R = V_{RMS} / (4\pi \times f_s \times L_1)$$

Where: VRMS is the input voltage phase to common

$$f_s = 25 \text{ kHz}$$

$$L_1 \geq L_{min}$$

The minimum inductive value of L1 must be present with the dc current flowing through it over the complete load current range. This requires an inductor with gaps in the magnetic circuit, either fixed or distributed, such as in powdered iron cores, or solenoid-wound inductors over ferrite rods (available from Reference 9).

Regulator dissipation. Since the regulator is a linear series pass type, the difference between the voltage developed across C3

at the regulator input and the desired output at the load current must be dissipated in the regulator. This dissipation is given by:

$$P_{diss} = (V_{in} - V_{out}) \times (I_L + V_{in} I_q)$$

Where: Iq = the quiescent current of the regulator.

Case to junction thermal resistances are given in the regulator manufacturer's data sheet. The dominant thermal resistance will be the case to air stream, which is usually available on heat sink manufacturer's data as a function of air velocity. You can assume a minimum 200 ft/min flow across the board with a maximum air temperature on the exit side of 66°C under worst case conditions. For low power on-card dc supplies, the copper foil on the printed circuit board can be used as a heat sink. However, the suitability of this arrangement should be checked carefully with thermocouples to confirm that the temperature rise of the regulator is not excessive.

Isolated or "floating" dc power supplied (Uses 2 and 3, page 1)

A major advantage of the 25 kHz backplane power is its ease of use for isolated power supplies that can have separate analog grounds, thereby reducing the effects of ground-conducted noise as discussed in References 3 and 4. Isolation is provided by an on-interface transformer, as shown in Figure 3. The use of 25 kHz ac input makes it possible for the isolation transformer to be very small and inexpensive. Toroidal printed circuit mounting types or "P" core (Reference 7)

shielded printed circuit mounting types generally offer the best price-performance combination. However, small E-E types can also be used at lower cost with some sacrifice in electromagnetic and electrostatic shielding. High permeability ferrite materials having low losses at 25 kHz are readily available with matching bobbins and mounting hardware from References 6 through 10.

Primary-to-secondary isolation of both dc and high frequency can be somewhat complex. References 3 and 4 describe single and double shielded transformers. It is possible to achieve high isolation with small ferrite cores and proper interwinding shield design. Simple copper foil interwinding shields are relatively inexpensive and are effective in decreasing primary-to-secondary electrostatic coupling at frequencies from 100 Hz to about 100 kHz. For higher frequencies, "link" coupling of two cores or other techniques may be required (Reference 3, p 117).

The ground isolation provided by the multi-channel +10V power supply circuits depicted in Figure 3 eliminates errors caused by ground-induced noise. In analog voltage measurement applications, power supply isolation minimizes common mode noise, improving measurement accuracy. With respect to digital data transmission uses, power supply isolation allows data terminals to operate at greater distances from the local system with fewer data errors than would otherwise be possible. When the power supply is not isolated, noise in the 50/60 Hz mains power distribution and grounding system supplying the computer can cause current noise loops that degrade signal integrity.

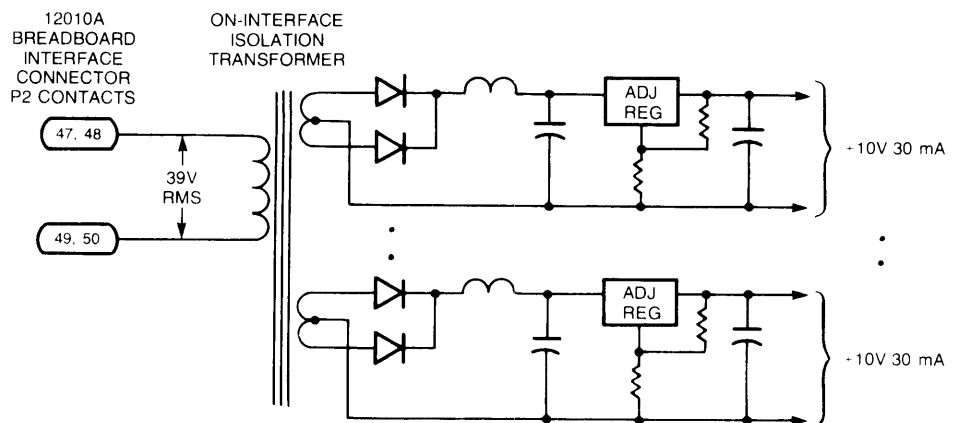


Figure 3. Multiple, isolated, on-interface +10V/30 mA power supplies

High-efficiency, on-interface low-voltage, high current power supply (Use 4, page 1)

Heat dissipation is often the main factor limiting the current output of on-interface power supplies. This is particularly true for lower voltage, high current supplies, such as required for many digital integrated circuit families. For example, at the +5V used for TTL families of integrated logic circuits, even the dissipation of the rectifiers can be a significant 14% to 20% of total power, because of the inherent 0.7V to 1.0V forward drop across silicon rectifiers, and heat sinking may be required at 3-5 Amp currents. Use of hot carrier or Schottky junction rectifiers, which have a lower forward drop presenting a power loss of only 4%-5% of the total power output, have peak inverse voltage ratings that are suitable for lower voltage power supplies and may not require heat sinks because of their lower power dissipation.

At low output voltages, the 2-3 volt drop required across most three-terminal adjustable integrated circuit series regulators for proper regulation can account for 40%-60% of the total power output, which is lost in the regulator and must be

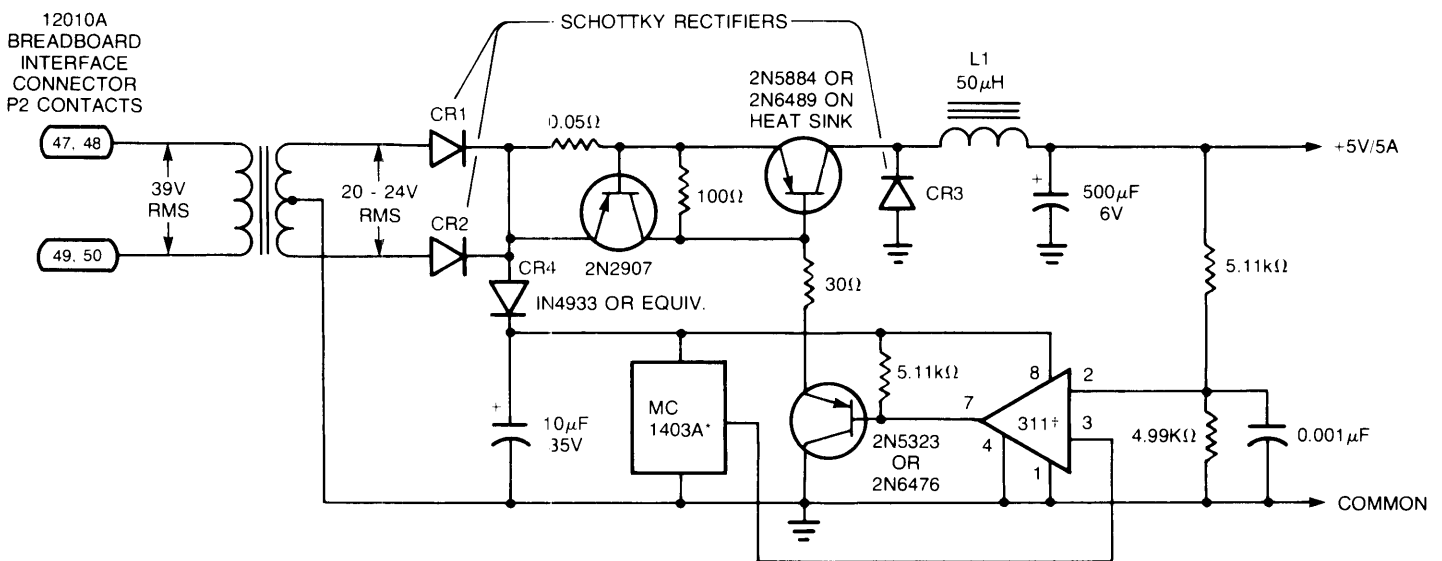
dissipated. Regulator heat sinking becomes difficult for even 1-3 Amp current outputs and impossible for the higher current levels that larger three-terminal regulators are able to pass. Because of these efficiency and dissipation problems, a more efficient circuit approach has evolved, as shown in Figure 4.

The circuit of Figure 4 uses a driven switching regulator for more efficient delivery of low voltage, high current output. This circuit regulates on the basis of the conduction angle of the pulsating rectified, unfiltered dc from the on-interface Schottky rectifiers. The result is efficiencies of 70%-85% with 1 Amp to 5 Amp loads. The duty cycle control is uniform over the half sine wave and the instantaneous energy is low at the switching transitions, which minimizes waveform distortion and RFI emission. Because the regulator operates on the incoming frequency as a driven circuit, it also eliminates the generation of other frequencies that would be a problem if an on-interface switching regulator integrated circuit were used. The circuit of Figure 4 eliminates sum and difference noise frequencies and a host of non-repetitive noise problems, while optimizing efficiency.

External supplies using 25 kHz power from the power module front connector

Power supplies for logic circuits or sensor signal conditioning circuits external to the computer or system card cage can also use 25 kHz power from the 12035A Power Module as the primary ac input. In fact, ac input power to the logic circuits power supply for the flexible disc in HP 1000 L-Series Systems is taken from the front 25 kHz connector of the 12035A Power Module. Similar use can be made by the OEM or end user in systems assembled from HP 1000 L-Series components. It is important to note, however, that physical clearance for the mating plug is not sufficient in the 2103L (box) Computer to permit use of 25 kHz power from the power module front connector in that configuration.

The design of 25 kHz-driven external power supplies is essentially the same as for on-interface power supplies, as previously discussed. However, less-stringent space constraints can be expected to simplify layout and make heat dissipation easier in the external supplies, so less design effort should be required to achieve the desired result.



CR1, CR2, and CR3 are International Rectifier 80SQ10 5A Schottky rectifiers.
 *Motorola MC1403A or equivalent 2.5V low TC reference source.
 †National Semiconductor LM 311 or equivalent Comparator.
 L1 is a Dale type IH5 or equivalent solenoid choke coil.

Figure 4. High efficiency on-interface, low voltage, high current 25 kHz driven switching power supply

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A

- A register, 2-25
- AB0-AB14 signals, 6-61
- AC crowbar, 4-14
- AC line power down sequence, 5-13
- AC line power up sequence, 5-13
- ACLK signal, 2-25
- Address buffer, 3-5
- Address bus, 2-21, 8-7
- Address latch, 3-18, 3-22
- Address multiplexer, 3-21, 3-27
- ADVIO signal, 2-27
- Air flow requirements, 1-8
- ALU, 2-21, 2-28
- Architecture, 1-1
- Arithmetic logic unit, 2-21, 2-28
- ASG instruction, 2-28, 2-32
- Audio alarm, 5-6, 5-12

B

- B register, 2-25
- Backplane
 - AC loading, 6-16
 - capacitance data, 6-17
 - card cage, 6-12
 - card slot pinouts, 6-14
 - card slots, 6-3
 - card socket interconnects, 6-12
 - configurations, 6-5
 - DC loading, 6-12
 - design rules/guidelines, 6-15
 - interface hardware, 6-9
 - interface requirements, 6-16
 - loading rules, 6-12
 - logical description, 6-1
 - memory access protocol, 6-18
 - memory handshake timing, 6-19
 - overview, 6-3
 - physical description, 6-1
 - power supply connector, 6-3
 - power supply interface connector, 4-3
 - specifications, 6-5, 6-10
 - worst case loading, 6-15
- Backup system, 5-1
- BADVIO flip-flop, 2-27

- Battery backup, 5-1
 - +12 volt regulators, 5-10
 - +5 volt regulators, 5-9
 - 12 volt output, 5-11
 - AC line power down sequence, 5-13
 - AC line power up sequence, 5-13
 - audio alarm, 5-6, 5-12
 - battery charger, 5-7
 - capacity, 5-4
 - charge current, 5-4
 - charge power, 5-4
 - charge time, 5-4
 - CPU interface, 5-6
 - description, 5-1
 - external connector, 5-5
 - functional theory of operation, 5-7
 - interface requirements, 5-5
 - interface signals, 5-5
 - interface to power supply, 5-6
 - load, memory in standby, 5-4
 - load, memory operational, 5-3
 - memory support time, 5-4
 - MLOST signal, 5-12
 - output current, 5-3
 - output voltages, 5-3
 - over-voltage limits, 5-3
 - overview, 5-1
 - parts list, 5-14
 - parts locations, 5-14
 - power down sequence, 5-12
 - power interruption, 5-1
 - power outage, 5-1
 - power up sequence, 5-12
 - regulation, 5-1
 - relay logic, 5-11
 - REMOTE/OFF/ON switch, 5-5
 - sequence logic, 5-12
 - specifications, 5-3
 - theory of operation, 5-9
 - voltage regulators, 5-7
 - voltage sag, 5-1
- Battery charger, 5-7, 5-9
- BCLK signal, 2-17, 2-25
- Block diagram
 - memory, 3-19
 - power supply, 4-12
- Block diagrams CPU chip, 2-21
- BTN signal, 2-18
- BUSY flip-flop, 3-24
- BUSY handshake, 3-5
- BUSY signal, 6-62

C

- Card slot pinouts, 6-14
- Card slot priorities, 6-3
- Card slots, 6-3
- Card socket interconnects, 6-12
- Cards L-Series, 1-7
- Catch diode, 4-16
- CCLK signal, 6-62
- Central interrupt register, 2-13
- CLA, 2-30
- CLKI signal, 2-23
- CLKP signal, 2-27
- Clocks, 2-63
 - speed, 3-12
 - system, 3-7
- Concurrent memory cycles, 3-32
- COND signal, 2-42
- Connectors
 - 25kHz, 4-3
 - external battery, 5-5
 - external fan, 4-4
 - power control, 4-4
 - power supply backplane interface, 4-3
 - power supply input power, 4-1
- CONTROL flip-flop, 6-21
- Control panel, virtual, 1-5
- Control sequence logic, 5-12
- Control structure, 2-30
- Control word register, 2-25
- Controller memory, 3-3
- COTURN signal, 6-63
- COUT signal, 2-28
- CPU
 - battery backup interface, 5-6
 - state diagram, 2-33
 - timing, 2-32
- CPU and CPU chip, 2-1
- CPU chip
 - block diagram, 2-21
 - buses, 2-21
 - data paths, 2-21
 - functional theory of operation, 2-17
 - registers, 2-23
 - signals, 2-17
- CPUTURN signal, 6-63
- CRS signal, 6-64
- Custom logic array, 2-30
- Cycle sequence, 3-31
- Cycle time, 3-7

D

- D flip-flop, 3-26
- Data reading from memory, 3-17
- Data bus, 2-21, 8-7
- Data-in latch, 3-20, 3-24
- Data-out buffer, 3-20, 3-24
- Data/address latches, 3-8
- DB0-DB15 signals, 6-65
- Description
 - battery backup, 5-1
 - electrical, 1-1
 - physical, 1-1
- Detailed theory of operation processor card, 2-44
- DI flip-flop, 3-24
- Diagnostics memory, 3-35
- Driver board, 4-20
- DST instruction, 2-43
- Dynamic RAM array, 3-21

E

- E register, 2-26
- E2 signal, 2-29
- E3 signal, 2-29
- EAU instructions, 2-32
- Electrical description, 1-1
- Environment system, 2-3
- Error amplifier, 5-9, 5-10
- Expanded memory access, 6-23
- Extend register, 2-26
- External fan power, 4-1

F

- Fast clock, 3-11
- FCH signal, 2-18
- FCLK signal, 6-65
- Fence register, 2-27
- Field programmable logic arrays, 2-1
- Flag
 - global register, 2-13
 - interrupt inhibit, 2-13
 - interrupt system, 2-13
 - parity sense, 2-13
 - parity system, 2-13
 - time base generator, 2-13
- FLAG flip-flop, 6-21

Flip-flop
 CASEN, 8-24
 COUNT, 8-26
 GO, 8-24
 LATCH, 8-24
 RAS, 8-25
 REF, 8-26
 VALID, 8-25
 WANTED, 8-24
Flip-flops
 BADVIO, 2-27
 BUSY, 3-24, 8-24
 CONTROL, 6-21
 D, 3-26
 DI, 3-24
 FLAG, 6-21
 MEGO, 3-31
 parity indicator, 3-27
 PON, 3-35
 RC, 3-30
 RE, 3-24
 RP, 3-29
 RS, 3-29
 START, 3-29
 VALID, 3-25
FPLA's, 2-1
FPLA, master, 2-51
Frontplane, 8-3
FRZM-, 2-58
Functional theory of operation
 battery backup, 5-7
 CPU chip, 2-17
 memory, 3-18
 power supply, 4-11
 processor card, 2-3
Fuse post, 4-1

G

GEI signal, 2-29
Global register flag, 2-13

H

Handshake, 6-18
Hard fail shutdown, 4-24

I

I/O accessing, 2-11
I/O functions processor card, 2-12
I/O handshake, 6-26
I/O instruction execution, 6-24
I/O interrupt, 2-9
I/O processing, 2-11
I/O state machine, 2-10, 2-51
I/O transfer protocol, 6-24
IA signals, 2-18
IAK signal, 6-66
ICHID signal, 6-66
ICHOD signal, 6-66
ID signals, 2-18
IIAK signal, 2-18
IIOGO signal, 2-18
IIORQ signal, 2-19
INC signal, 2-30
IND signal, 2-25
Indicators power supply, 4-4
Inhibit memory, 3-12
Initialization
 memory, 3-15
 PON, 3-35
 signals, 3-15
Input crowbar, 4-14
Input data/address set-up, 3-15
Input power connector, 4-1
Input status register, 2-12
Instruction
 fetch from A or B register, 2-46
 fetch from ROM, 2-49
Instruction register, 2-23
Instruction register CLA, 2-32
Instructions
 ASG, 2-28, 2-32
 CLC 0, 2-15
 CLC 4, 2-15
 CLC 5, 2-16
 CLC 6, 2-16
 CLF 0, 2-15
 CLF 2, 2-15
 CLF 5, 2-16
 CLF 6, 2-16
 DLD, 8-15
 DST, 2-43, 8-15
 EAU, 2-32
 ISZ, 2-43
 JMP, 2-42

JSB, 2-43
LIA 1, 2-15
LIA 4, 2-15
LIA 5, 2-16
LIA 7,C, 2-16
LIB 1, 2-15
LIB 4, 2-15
LIB 5, 2-16
LIB 7,C, 2-16
MIA 1, 2-15
MIA 4, 2-16
MIA 5, 2-16
MIA 7,C, 2-17
MIB 1, 2-15
MIB 4, 2-16
MIB 5, 2-16
MIB 7,C, 2-17
MRG, 2-32
OTA 0, 2-15
OTA 07, 2-43
OTA 1, 2-15
OTA 2, 2-15
OTA 4, 2-16
OTA 5, 2-16
OTA 7, 2-17
OTA 7,C, 2-17
OTB 0, 2-15
OTB 07, 2-43
OTB 1, 2-15
OTB 2, 2-15
OTB 4, 2-16
OTB 5, 2-16
OTB 7, 2-17
OTB 7,C, 2-17
SFC 0, 2-15
SFC 2, 2-15
SFC 4, 2-15
SFC 5, 2-16
SFC 6, 2-16
SFS 0, 2-15
SFS 2, 2-15
SFS 4, 2-15
SFS 5, 2-16
SFS 6, 2-16
SRG, 2-32
STA, 2-43
STB, 2-43
STC 07, 2-42
STC 4, 2-15
STC 5, 2-16
STF 0, 2-15
STF 2, 2-15

- STF 5, 2-16
- STF 6, 2-16
- INT signal, 2-19, 2-33
- INTCLK signal, 2-23, 2-25, 2-30, 2-32
- Integrated thyristor rectifiers, 4-17
- Interface buffers, 3-18, 3-22
- Interface hardware, 6-9
- Interface requirements battery backup, 5-5
- Interrupt
 - I/O, 2-9
 - memory protect, 2-8
 - parity error, 2-8
 - power fail, 2-8
 - processing, 2-6
 - requests, 2-6
 - special, 2-8
 - system flag, 2-7
 - time base generator, 2-9
 - unimplemented instruction, 2-8
- Interrupt inhibit flag, 2-7, 2-13
- Interrupt latency, 2-11
- Interrupt levels, 2-6
- Interrupt mask register, 2-13
- Interrupt service, 2-9
- Interrupt system flag, 2-7, 2-13
- Interrupts, 6-19
 - latency, 6-23
 - system level, 2-6
 - timing, 6-22
- INTRQ signal, 6-67
- IOG signal, 2-19
- IOGO signal, 6-67
- IORQ signal, 6-68
- IPON signal, 2-19
- IR logic, 2-23
- ISZ instruction, 2-43

J

- JMP instruction, 2-42
- JSB instruction, 2-43

L

- L-Series memory, 3-1
- LDCW signal, 2-25
- LDINC signal, 2-27
- Levels interrupt, 2-6
- Line drop-out detector, 4-26
- Line power failure, 3-10

- Index-8

Line power up logic, 4-28
Line rectifier, 4-14
Line selector switch, 4-1
Logic Board, 4-27
Long half cycle, 6-28
Loop regulator, 4-22
Low voltage driver supply, 4-11

M

Main control circuit, 3-30
Main handshake signals, 3-11
Master FPLA, 2-51
MCHID signal, 6-68
MCHOD signal, 6-69
MCHODOC signal, 6-69
MEGO flip-flop, 3-31
MEM signal, 2-19
MEMDIS signal, 6-70
MEMGO signal, 6-70
Memory
 accessing, 2-44
 address latch, 3-18, 3-22
 address multiplexer, 3-21, 3-27
 addresses, 3-15, 8-13
 altering protected area, 2-42
 array card control logic, 8-33
 backplane interface, 3-11, 8-7
 basic operation, 3-3
 battery backup, 3-10
 card, 3-2
 concurrent cycles, 3-5
 control and timing logic, 8-20
 control signals, 3-11
 controller, 3-3
 controller (XL), 8-1
 cycle, 3-3
 cycle sequence, 3-31
 cycle time, 3-7
 data read, 2-46
 data-in latch, 3-20, 3-24
 data-out buffer, 3-20, 3-24
 data/address latches, 3-8
 detailed theory of operation (XL), 8-20
 diagnostic functions, 3-35
 dynamic RAM array, 3-21
 expanded (XL), 8-1
 frontplane signals, 8-17
 frontplane signals, address lines, 8-18
 frontplane signals, configure lines, 8-19
 frontplane signals, control lines, 8-19

frontplane signals, response lines, 8-19
functional block diagram, 3-19, 8-9
functional theory of operation, 3-18
functional theory of operation (XL), 8-7
handshake timing, 6-19, 8-9
inhibit signal timing, 8-9
inhibiting operation, 3-12
initialization, 3-15
input data/address set-up, 3-15
instruction fetch, 2-46
interface buffers, 3-18, 3-22
M voltages, 3-10
main control circuit, 3-30
maintaining power, 3-10
mapping, 8-4, 8-13
mapping control, 8-27, 8-28
mapping control logic, 8-17
memory cycles occurring during refresh cycles, 3-32
operating characteristics, 3-15
overview, 3-1
parity circuit, 8-6, 3-25, 8-34
parity detection, 3-26, 8-34
parity generation, 3-25
parity generator/comparator, 3-20
parts list, 3-36, 8-34
parts locations, 3-36, 8-34
power requirements, 3-7
power sequencing, 3-15
protect system, 2-42
read cycle, 3-5
reading data from, 3-17
recovery from parity errors, 3-18
refresh circuit, 3-29
refresh control, 3-21, 8-12
refresh cycle, 3-5, 8-26
refresh cycles occurring during memory cycles, 3-32, 8-12
refresh period, 3-7
remote access, 6-23
restrictions, 3-1
row and column addresses, 3-27
selecting row addresses, 3-28
size, 3-1
slide switch, 3-10
source voltages, 3-10
speed, 3-12
standby mode, 3-10
support time, 5-4
test points, 3-35
theory of operation, 3-22
timing and control, 3-21, 8-11
timing diagrams, 8-21
violation, 2-43

- write by processor card, 2-46
- write cycle, 3-3
- writing data into, 3-17
- XL Address Generation, 8-31
- Memory access protocol, 6-18
- Memory accessing, 2-3
- Memory controller, 3-3
- Memory locations 0 and 1, 2-6
- Memory protect fence register, 2-27
- Memory protect interrupt, 2-8
- Memory protect system, 2-42
- Memory protect violation register, 2-13
- MGO signal, 2-19
- MLOST signal, 5-12, 6-71
- MND signal, 2-20
- Motherboard, 4-13
- MP signal, 6-71
- MPF signal, 2-20, 2-43
- MPV signal, 2-20, 2-43
- MRG instruction, 2-32
- MRQ signal, 6-72

N

- Next state CLA, 2-30
- Next state counter/register, 2-30
- Next state register, 2-30

O

- O register, 2-26
- ONES signal, 2-28
- Opto-coupled SCR, 4-14
- OTA 07 instruction, 2-43
- OTB 07 instruction, 2-43
- Output CLA, 2-30
- Output CLA latches, 2-30
- Output rectifiers, 4-18
- Output status register, 2-12
- Over-current protection, 5-10, 5-11
- Over-voltage protection, 5-10
- Overflow register, 2-26
- Overview
 - battery backup, 5-1
 - processor card, 2-1
- OVF1 signal, 2-29
- OVF2 signal, 2-29
- OVF3 signal, 2-29

P

P register, 2-26
Page register, 2-23
Parity
 bit, 3-8
 circuit, 3-25
 control, 3-20
 detection, 3-8, 3-26
 detector, 3-5
 error, 3-9
 generation, 3-8, 3-25
 generator/comparator, 3-20
 indicator, 3-9
 read cycle, 3-9
 recovery from errors, 3-18
 sense, 3-9
 strobe, 3-27
 write cycle, 3-8
 written data, 3-3
Parity error interrupt, 2-8
Parity error register, 2-13
Parity indicator flip-flop, 3-27
Parity sense flag, 2-13
Parity system flag, 2-13
Parts list
 battery backup, 5-14
 memory, 3-36
 point-of-load regulator, 7-2
 power supply, 4-30
 processor card, 2-65
Parts locations
 battery backup, 5-14
 memory, 3-36
 point-of-load regulator, 7-2
 power supply, 4-30
 processor card, 2-65
PE signal, 6-72
PFW signal, 6-72
Phase-locked loop synchronization, 4-19
Physical description, 1-1
 backplane, 6-1
PMPI+, 2-58
Point-of-load regulator, 7-1
 parts list, 7-2
 parts locations, 7-2
 specifications, 7-1
PON flip-flop, 3-35
PON initialization, 3-35
PON signal, 2-33, 6-73

- Post regulators, 4-18
- Power cord receptacle, 4-1
- Power down sequence, 5-12
- Power fail interrupt, 2-8
- Power fail warning logic, 4-28
- Power interruption, 3-10, 5-1
- Power on logic, 4-28
- Power outage, 5-1
- Power panel, 4-1
- Power requirements, 1-7
 - memory, 3-7
 - power supply, 4-6
 - XL memory, 8-5
- Power sequencing, 3-15
- Power supply
 - 25-kHz power application, 66-1
 - AC crowbar, 4-14
 - AC outputs, 4-8
 - backplane interface output connector, 4-3
 - block diagram, 4-12
 - catch diode, 4-16
 - driver board, 4-18
 - fault indicators, 4-5
 - functional theory of operation, 4-11
 - hard fail shutdown, 4-24
 - indicators, 4-4
 - input crowbar, 4-14
 - integrated thyristor rectifiers, 4-17
 - interface to battery backup, 5-6
 - line drop-out detector, 4-26
 - line power up logic, 4-28
 - line rectifier, 4-14
 - logic board, 4-25
 - loop regulator, 4-22
 - low voltage driver supply, 4-11
 - motherboard, 4-11
 - opto-coupled SCR, 4-14
 - output rectifiers, 4-18
 - parts list, 4-30
 - parts locations, 4-30
 - phase-locked loop synchronization, 4-19
 - physical characteristics, 4-1
 - post regulators, 4-18
 - power factor, 4-6
 - power fail warning logic, 4-28
 - power on logic, 4-28
 - power requirements, 4-6
 - power supply up logic, 4-28
 - RFI filter, 4-14
 - Schottky rectifiers, 4-18
 - SCR gate drive, 4-19
 - signal levels, 4-10

- sine-wave inverter, 4-17
- soft fail shutdown, 4-24
- specifications, 4-5
- switching regulator, 4-15
- switching regulator tri-level drive, 4-22
- theory of operation, 4-11
- trouble diagnosis, 4-29
- under-voltage limit comparators, 4-25
- voltage controlled oscillator, 4-19

Power supply up logic, 4-28

Power up sequence, 5-12

Priorities, 6-3

Priority order, 2-7

Processor

- battery backup interface, 5-6
- memory access and DMA, 2-49

Processor card

- detailed theory of operation, 2-44
- I/O functions, 2-12
- parts lists, 2-65
- parts locations, 2-65

Processor card functional theory of operation, 2-3

Processor card overview, 2-1

PS signal, 6-74

PSAVE register, 2-27

PSFF+, 2-58

R

- RAM elements, 8-1
- RAM elements, 3-5
- RC flip-flop, 3-30
- RCLK signal, 6-75
- RDA signal, 2-25
- RDB signal, 2-25
- RDI signal, 2-23
- RE flip-flop, 3-24
- Read cycle, 3-5
- Read cycle parity, 3-9
- READ signal, 2-20
- Read strobe pulse, 3-5
- Reading data from memory, 3-17
- Recovery from parity errors, 3-18
- Refresh cycle, 8-4
- Refresh circuit, 3-29
- Refresh control, 3-21
- Refresh cycle, 3-5
- Refresh period, 3-7

Register

- central interrupt, 2-13
- input status, 2-12

- interrupt mask, 2-13
- memory protect violation, 2-13
- output status, 2-12
- parity error, 2-13
- Registers
 - A, 2-25
 - B, 2-25
 - control word, 2-25
 - CPU chip, 2-23
 - double register shift operations, 2-23
 - E, 2-26
 - Extend, 2-26
 - fence, 2-27
 - instruction, 2-23
 - memory protect fence, 2-27
 - next state, 2-30
 - O, 2-26
 - overflow, 2-26
 - P, 2-26
 - page, 2-23
 - PSAVE, 2-27
 - T, 2-26
- Regulator point-of-load, 7-1
- Relay logic, 5-11
- REMEM signal, 6-75
- Remote memory access, 6-23
- REMOTE/OFF/ON battery backup switch, 5-5
- RFI filter, 4-14
- RNI signal, 6-76
- ROM data read, 2-49
- ROM code layout, 65-2
- ROM firmware, 2-1
- ROM listing, 65-1
- ROM loaders listing, 65-1
- Row-address strobe, 3-27
- RP flip-flop, 3-29
- RS flip-flop, 3-29

S

- SCHID signal, 6-77
- SCHOD signal, 6-77
- Schottky rectifiers, 4-18
- SCLK signal, 6-78
- SCR gate drive, 4-19
- Select code, 6-19
- Self test, 1-6
- Self-test listing, 65-1
- Short half cycle, 3-5
- Short-half-cycle, 3-3

Signals

AB0-AB14, 6-61
ACLK, 2-25
ADVIO, 2-27
battery backup interface, 5-5
BCLK, 2-17, 2-25
BTN, 2-18
BUSY, 8-3, 8-9, 8-24, 6-62
CCLK, 6-62
CLKI, 2-23
CLKP, 2-27
COND, 2-42
COTRN, 8-10
COTURN, 6-63
COUT, 2-28
CPU chip, 2-17
CPUTURN, 6-63
CRS, 6-64, 8-10
DB0-DB15, 6-65
definitions, 6-61
E2, 2-29
E3, 2-29
fast clock, 3-11
FCH, 2-18
FCLK, 6-65, 8-7
GE1, 2-29
IA0 - IA14, 2-18
IAK, 6-66, 8-10
ICHID, 6-66
ICHOD, 6-66
ID0 - ID15, 2-18
IIAK, 2-18
IIOGO, 2-18
IIORQ, 2-19
INC, 2-30
IND, 2-25
INT, 2-19, 2-33
INTCLK, 2-23, 2-25, 2-30, 2-32
INTRQ, 6-67
IOG, 2-19
IOGO, 6-67
IORQ, 6-68
IPON, 2-19
LDCW, 2-25
LDINC, 2-27
main handshake, 3-11
MCHID, 6-68
MCHOD, 6-69
MCHODOC, 6-69
MEM, 2-19
MEMDIS, 8-9, 8-24, 6-70
MEMGO, 8-3, 8-9, 8-24, 6-70

MGO, 2-19
MLOST, 5-12, 8-11, 6-71
MND, 2-20
MP, 6-71, 8-10
MPF, 2-20, 2-43
MPV, 2-20, 2-43
MRQ, 6-72, 8-10
ONES, 2-28
OVF1, 2-29
OVF2, 2-29
OVF3, 2-29
PE, 8-6, 8-10, 6-72
PFW, 6-72
PON, 8-10, 2-33, 6-73
PS, 8-6, 8-10, 6-74
RCLK, 6-75, 8-7
RDA, 2-25
RDB, 2-25
RDI, 2-23
READ, 2-20
REMEM, 8-9, 8-24, 6-75
RNI, 6-76, 8-10
SCHID, 6-77
SCHOD, 6-77
SCLK, 6-78, 8-7
SLAVE, 2-33, 6-79
SLK, 2-20
SLV, 2-20
SPRQ-, 6-79
system clock, 3-11
TBT, 2-21
TDI, 2-21
timing specifications, 6-28
UIT, 2-21
VALID, 8-3, 8-9
VALID-, 6-80
WE, 6-80
ZEROS, 2-28
Silicon-on-sapphire, 1-1
Sine-wave inverter, 4-17
Slave mode, 1-5
 entry, 1-6
Slave mode timing, 6-27
Slave mode transfers, 6-25
SLAVE signal, 2-33, 6-79
SLK signal, 2-20
SLV signal, 2-20
Soft fail shutdown, 4-24
SOS, 2-1
Special interrupt, 2-8

Specifications
 backplane, 6-10
 battery backup, 5-3
 memory, 3-7
 point-of-load regulator, 7-1
 power supply, 4-5
 signal timing, 6-28
SPRQ- signal, 6-79
SRG instruction, 2-32
STA instruction, 2-43
START flip-flop, 3-29
State diagram, 2-33
State machine, 2-51
 synchronous, 2-30
Status Logic, 2-28
STB instruction, 2-43
STC 07 instruction, 2-42
Support features, 1-5
Switching regulator, 4-15
Switching regulator tri-level drive, 4-22
Synchronous state machine, 2-30
System clock, 3-7
System environment, 2-3
System level interrupt priority, 2-7
System level interrupts, 2-6, 2-9
System reset, 2-15

T

T register, 2-26
TBT signal, 2-21
TDI signal, 2-21
Temporarily Disable Interrupt signal, 2-7
Theory of operation
 battery backup, 5-9
 memory, 3-22
 power supply, 4-11
Time base generator flag, 2-13
Time base generator interrupt, 2-9
Timing
 CPU, 2-32
 interrupts, 6-22
 memory handshake, 6-19
 slave mode, 6-27
 specifications, 6-28
Transparent latch, 3-22

U

UIT signal, 2-21
Under-voltage limit comparators, 4-25
Unimplemented instruction interrupt, 2-8

V

VALID flip-flop, 3-25
VALID- signal, 6-80
VCP program listing, 65-1
Vector address, 2-10
Ventilation requirements, 1-8
Virtual control panel, 1-5
 entry, 1-6
Voltage controlled oscillator, 4-19
Voltage regulators, 5-7, 5-9, 5-10
Voltage sag, 5-1

W

WE- signal, 6-80
Write address, 3-3
Write cycle, 3-3
Writing data into memory, 3-17

Z

ZEROS signal, 2-28

