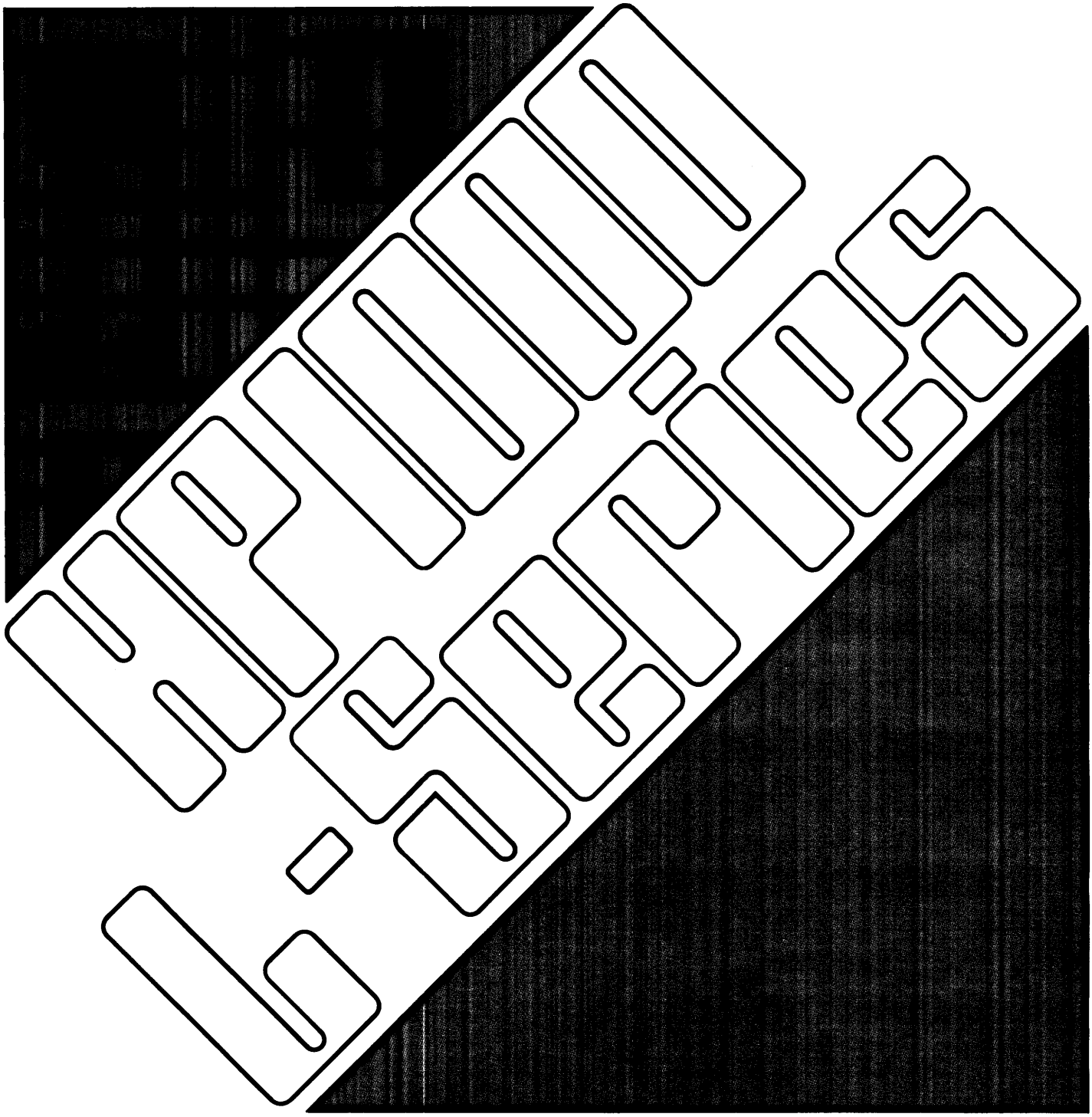
HEWLETT PACKARD

HP 12009A HP-IB Interface

Reference Manual



HEWLETT PACKARD

REFERENCE MANUAL

HP 12009A
HP-IB INTERFACE

Manual Part No. 12009-90001
Printed in U.S.A. JAN 1980

Card Assembly: 12009-60001
Date Code: A-2001, B-2001

HEWLETT PACKARD COMPANY
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

Manual Part No. 12009-90001
September 1982

PRINTING HISTORY

New editions are complete revisions of the manual. Update packages contain replacement pages or write-in instructions to be merged into the manual by the customer. Manuals will be reprinted as necessary to incorporate all prior updates. A reprinted manual is identical in content (but not in appearance) to the previous edition with all updates incorporated. No information is incorporated into a reprinting unless it appears as a prior update. The edition does not change.

First Edition ..... Jan 1980
Update 1 ..... March 1982
Update 2 ..... September 1982
Reprint ..... September 1982

SAFETY CONSIDERATIONS

GENERAL - This product and relation documentation must be reviewed for familiarization with safety markings and instructions before operation.

SAFETY SYMBOLS

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal (sometimes used in manual to indicate circuit common connected to grounded chassis).

WARNING

The WARNING sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a WARNING sign until the indicated conditions are fully understood and met.

CAUTION

The CAUTION sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a CAUTION sign until the indicated conditions are fully understood and met.

CAUTION

STATIC SENSITIVE DEVICES

When any two materials make contact, their surfaces are crushed on the atomic level and electrons pass back and forth between the objects. On separation, one surface comes away with excess electrons (negatively charged) while the other is electron deficient (positively charged). The level of charge that is developed depends upon the type of material. Insulators can easily build up static charges in excess of 20,000 volts. A person working at a bench or walking across a floor can build up a charge of many thousands of volts. The amount of static voltage developed depends on the rate of generation of the charge and the capacitance of the body holding the charge. If the discharge happens to go through a semiconductor device and the transient current pulse is not effectively diverted by protection circuitry, the resulting current flow through the device can raise the temperature of internal junctions to their melting points. MOS structures are also susceptible to dielectric damage due to high fields. *The resulting damage can range from complete destruction to latent degradation.* Small geometry semiconductor devices are especially susceptible to damage by static discharge.

The basic concept of static protection for electronic components is the prevention of static build-up where possible and the quick removal of already existing charges. The means by which these charges are removed depend on whether the charged object is a conductor or an insulator. If the charged object is a conductor such as a metal tray or a person's body, grounding it will dissipate the charge. However, if the item to be discharged is an insulator such as a plastic box/tray or a person's clothing, ionized air must be used.

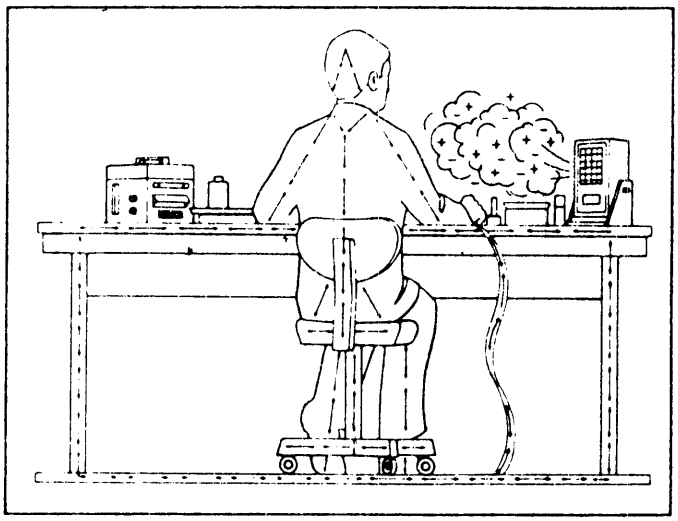
Effective anti-static systems must offer start-to-finish protection for the products that are intended to be protected. This means protection during initial production, in-plant transfer, packaging, shipment, unpacking and *ultimate use.* Methods and materials are in use today that provide this type of protection. The following procedures are recommended:

1. All semiconductor devices should be kept in "antistatic" plastic carriers. Made of transparent plastics coated with a special "antistatic" material which might wear off with excessive use, these inexpensive carriers are designed for short term service and should be discarded after a period of usage. *They should be checked periodically to see if they hold a static charge greater than 500 volts in which case they are rejected or recoated.* A 3M Model 703 static meter or equivalent can be used to measure static voltage, and if needed, carriers (and other non-conductive surfaces) can be recoated with "Staticide" (from Analytical Chemical Laboratory of Elk Grove Village, Ill.) to make them "antistatic."

2. Antistatic carriers holding finished devices are stored in transparent static shielding bags made by *3M Company.* Made of a special three-layer material (nickle/polyester/polyethylene) that is "antistatic" inside and highly conductive outside, they provide a Faraday cage-like shielding which protects devices inside. "Antistatic" carriers which contain semiconductor devices should be kept in these shielding bags during storage or in transit.

Individual devices should only be handled in a static safeguarded work station.

3. A typical static safeguarded work station is shown below including grounded conductive table top, wrist strap, and floor mat to discharge conductors as well as ionized air blowers to remove charge from nonconductors (clothes). Chairs should be metallic or made of conductive materials with a grounding strap or conductive rollers.



SAFETY EARTH GROUND - This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

BEFORE APPLYING POWER - Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

SERVICING

WARNING

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

WARNING

EYE HAZARD

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

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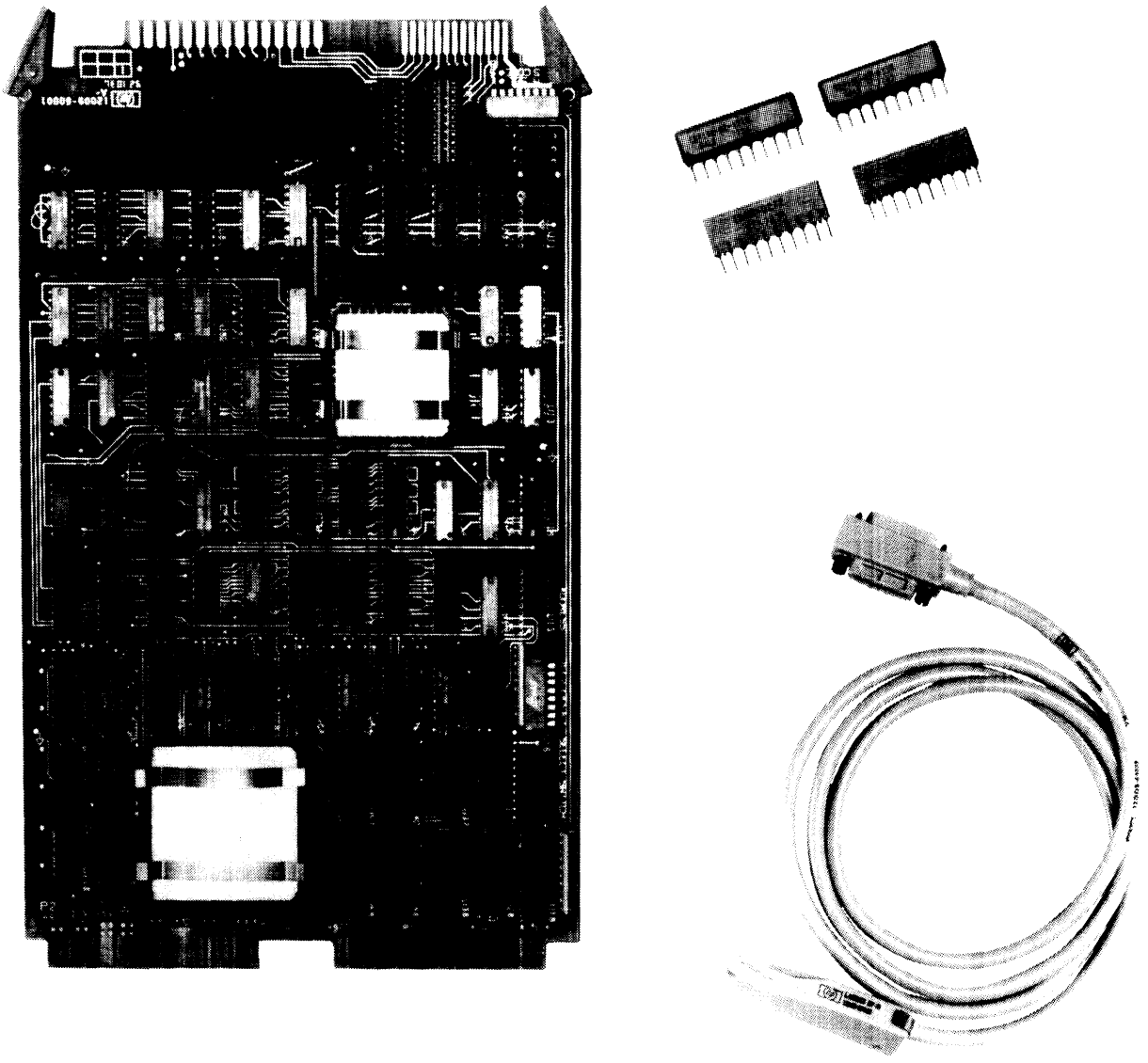

Figure 1-1. HP 12009A HP-IB Interface

INTRODUCTION

SECTION I

1-1. INTRODUCTION

This manual provides general information, installation instructions, programming instructions, theory of operation, maintenance instructions, replaceable parts information, and service diagrams for the HP 12009A HP-IB Interface.

This section contains general information concerning the HP 12009A HP-IB Interface, including a description and specifications.

1-2. DESCRIPTION

The Hewlett-Packard Interface Bus (HP-IB) is Hewlett-Packard's implementation of the IEEE Standard 488-1978.

The HP 12009A (see Figure 1-1) provides an interface between the HP 1000 L-Series computers and systems and an HP-IB system of up to 14 devices. Several such HP-IB systems can be interfaced to the L-Series computer, each system requires a separate interface card. The HP-IB card plugs into a single slot in the L-Series Backplane (see Figure 1-2) and is assigned only one select code. The HP-IB card is connected by cable to the HP-IB device or system. To the L-Series computer, this card is an I/O card and is under its software control at all times. To the HP-IB system, this card may or may not be a system controller depending on the setting of a switch selectable option.

The HP-IB card has the capability of handling its own Direct Memory Access (DMA) and of decoding its own instructions from the CPU. These features are performed by the I/O Master located on the HP-IB card. Figure 1-3 shows the HP-IB card in a typical L-Series system environment.

The interfaces to the L-Series backplane and to the HP-IB devices are provided by two LSI SOS integrated circuit chips. The first integrated circuit chip, the I/O processor (IOP) chip, manages all I/O functions of the L-Series computers. The second chip, the PHI (Processor to HP-IB Interface) chip performs all data and control signal interactions with the HP-IB devices. Through the use of these two chips, the HP 12009A HP-IB Interface relieves the CPU of most of the HP-IB protocol processing.

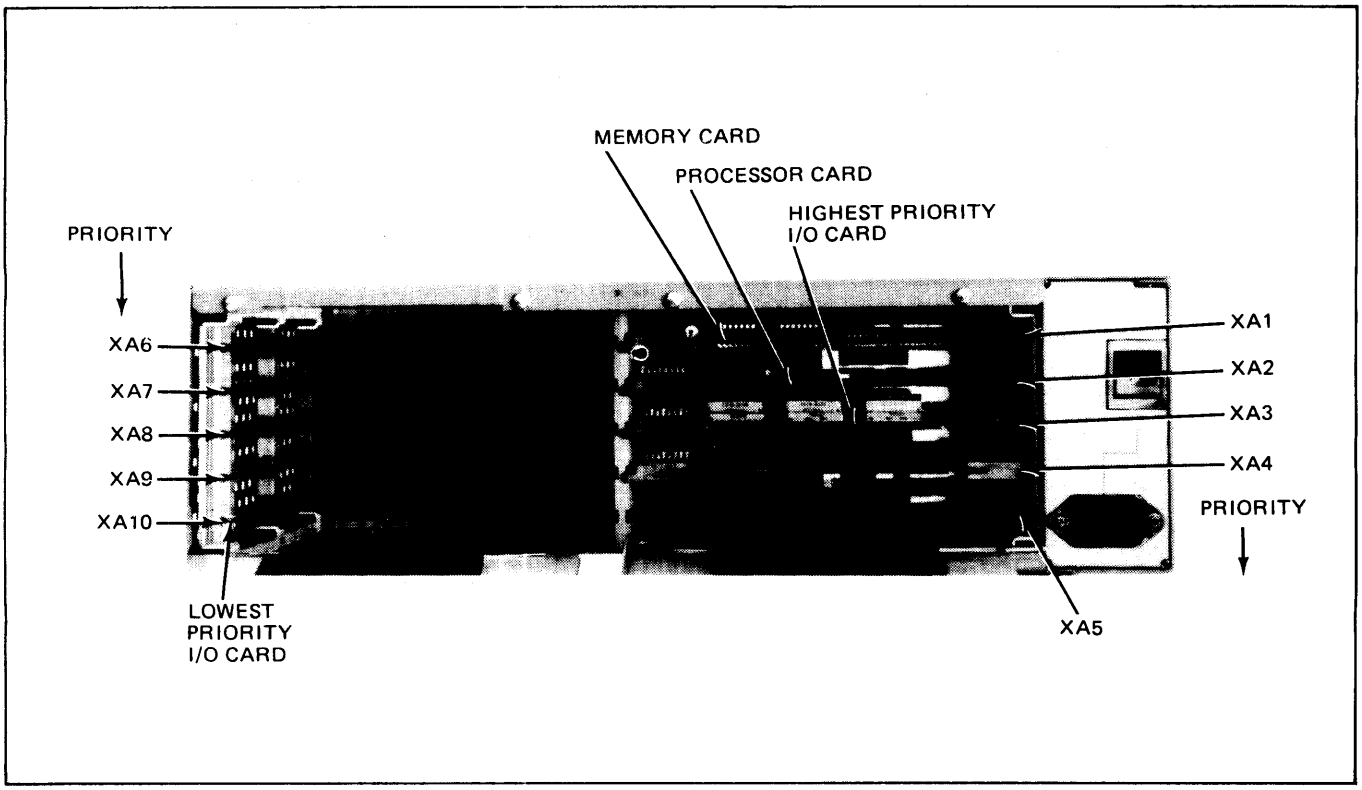

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Figure 1-2. Typical L-Series Card Cage Layout

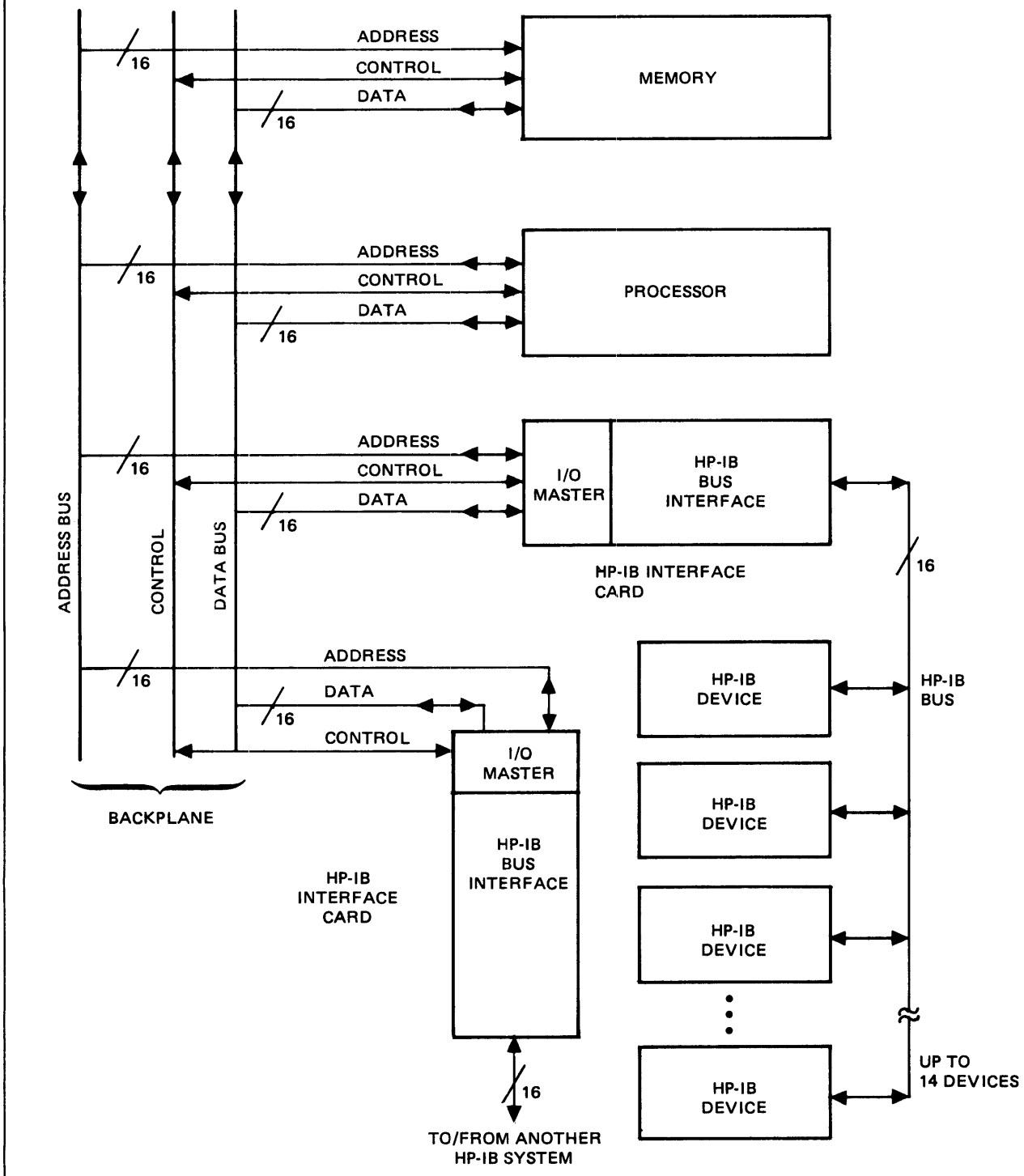


Figure 1-3. HP-IB Interface in a Typical L-Series System Environment

The HP-IB Interface can support either high speed (IEEE Std 488-1978 paragraph 5.2.3) or standard speed devices. The selection of either high or standard speed operation is determined by the setting of switch U1S2. The speed of operation depends on the type of device connected to the card.

1-3. EQUIPMENT SUPPLIED

The HP 12009A HP-IB Interface consists of the following items (see Figure 1-1):

a. HP-IB Interface Card, part no. 12009-60001.

b. Interconnecting cable, part no. 12009-60007.

c. HP-IB Interface Reference Manual, part no. 12009-90001 (not shown).

d. High Speed Operation Card (not shown).

e. Load Resistor Packs (R11, R12, R13, and R14).

1-3.1. OPTIONS AVAILABLE

Option D01: Substitutes interconnecting cable, part number 12009-60007, with a 1.25 meter cable, part number 12009-60009. This option is used in A-Series system configurations only.

1-4. IDENTIFICATION

Five digits and a letter (12009A in this case) are used to identify Hewlett-Packard products used with HP computers. The five digits identify the product and the letter indicates the revision level of the product.

The interface card is further identified by a part number marked on the card. In addition, a letter and a date code consisting of four digits (e.g., A-1926) are placed below the part number. The letter identifies the version of the etched circuit on the card. The date code (four digits following the letter) identifies the electrical characteristics of the assembled card. Thus, the complete part number on the HP-IB Interface Card could be as follows:

12009-60001
A-1926A

If the date code stamped on the HP-IB Interface Card is not listed with the date code on the title page of this manual, then there are differences between that card and the card described in this manual. The differences are described in manual supplements available at the nearest HP Sales and Service Office (listed in the back of this manual).

1-5. REFERENCE MANUAL

The manual supplied with the interface card is identified by its title and part number. The part number, 12009-90001, is printed on the title page. The publication date also is printed on the title page. If the manual is revised, the publications date is changed. The Print History and List of Effective Pages will reflect the revision date.

1-6. SPECIFICATIONS

Table 1-1 lists the specifications of the HP 12009A HP-IB Interface

Table 1-1. Specifications

ELECTRICAL CHARACTERISTICS	
HP-IB Bus Signal Lines: The Bus consists of the following 16 lines:	
DIO1	Data Input/Output 1
•	
•	
•	
DIO8	Data Input/Output 8
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify
Logic Levels:	High > 2.4V Low < 0.4V
All signals are Low = True except NRFD and NDAC.	

Table 1-1. Specifications (Continued)

ELECTRICAL CHARACTERISTICS (Continued)

Line Termination: Each of the 16 Bus signal lines is terminated with 2.3k ohm to Vcc and 4.7k ohm to logic common without the optional load resistors.

Line Drivers: Each of the 16 Bus signal lines are driven with a circuit having the following typical characteristics:

Type: Tri-state, Open Collector
Output Voltage Low State: < 0.4V @ 48 mA
Output Voltage High State: 2.5V @ −5.2 mA

Line Receivers: Each of the 16 Bus signal lines is received with a circuit having the following typical characteristics:

Type: Schmitt Trigger
Threshold Positive Transition: 1.75V
Threshold Negative Transition: 1.1V
Input Current Low State: −1.3 mA @ 0.4V
Input Current High State: 0.7 mA @ <5.5V

DMA Transfer Rates:

Standard Speed: 500 KBytes
[1]High Speed:
Random Instruction Mix: 930 KBytes
- Worst Case Instruction Mix: 734 KBytes
- Worst Case: A JMP* (a Jump Instruction who's target address is it's own address).

Maximum Cable Length:

Standard Operation: 2 metres per device connected with a 20m maximum length and a settling time of greater than 500 ns.

[2]High Speed Operation: 2 metres per device connected with a 15m maximum length and a settling time of less than 350 ns.

Operating Temperature: 0 to +55 Degrees Celsius.

Power Requirements: This card requires the following amounts of power from the computer's power supply at 25 degrees Celsius:

	CURRENT		POWER DISSIPATED	
Voltage	**W/O Load Resistors**	**W/Load Resistors**	**W/O Load Resistors**	**W/Load Resistors**
+ 5V	2.02 A	2.10 A	10.61 watts	11.03 watts
+12V	32 mA	84 mA	0.40 watts	1.06 watts
		Total Power	11.01 watts	12.09 watts

PHYSICAL CHARACTERISTICS

Card Dimensions:

Width: 17.15cm (6.750 in.)
Length: 28.91cm (11.380 in.)

Connector: 30-pin printed circuit board edge connector (cable supplied has standard Bus connector on outboard end).

[1]HP-IB Interface must be in the highest priority I/O slot in Backplane.
[2]Refer to Section II, paragraph 2-18 for further information.

1-7. HEWLETT-PACKARD INTERFACE BUS (HP-IB) CAPABILITIES

HP-IB provides the capability of connecting from one to 14 compatible devices to the computer via one interface card. Data is transferred over the HP-IB bidirectionally in 8-bit bytes. Data can be transferred from a device to the computer and other devices simultaneously or from the computer to one or more devices simultaneously or from one device to other devices under the direction of the computer.

Some HP-IB features must be used while other features are optional. For example, all devices must be capable of being addressed, but they may or may not be capable of being operated by remote control. A system may have some devices operating under remote control while other devices obey their front and rear panel controls (LOCAL). The same pins of all HP-IB connectors of all devices are connected in parallel making a parallel communication network. This permits information to flow in any direction on the bus and allows any device to talk directly with another device without going through a central control unit.

1-8. HP-IB SUPPORTED FUNCTIONS

The interface card is designed to support the following HP-IB Interface Functions as defined by the IEEE Standard 488, 1978. The HP-IB Interface is Hewlett-Packard's implementation of the IEEE Standard 488-1978. These functions are fully supported by the HP 12009A unless otherwise noted.

Controller Functions

C1 System Controller
C2 Send Interface Clear and Take Charge
C3 Send Remote Enable
C4 Respond to Service Request
C5 Send Interface Messages, Receive Control, Pass Control, Pass Control to Self, Parallel Poll, Take Control Synchronously

Controlled Device Functions

SR1	Service Request
RL2	Remote Local
PP1	Parallel Poll (see Section III, paragraph 3-49)
DC1	Device Clear
DT1	Device Trigger

The following utility functions are proviced to support the above functions.

SH1	Source Handshake
AH1	Acceptor Handshake
T5	Basic Talker,Serial Poll, Talk Only, Unaddress if My Listener Address
TE5	Basic Extended Talker, Serial Poll, Talk Only, Unaddress if My Listener Address and My Secondary Address
L3	Basic Listener, Listen Only Mode, Unaddress if My Talk Address
LE3	Basic Extended Listener, Listener Only Mode, Unaddress if My Secondary Address and Talker Primary Addressed State

1-9. ADDRESSING-TALKING-LISTENING-HANDSHAKING

A technique of addressing is used to determine which device is to "talk" and those devices that are to "listen". Data is sent from one device to another device in a bit parallel byte serial format using an interlocked "Handshake" technique. This technique assures that the sender does not remove data before the receiver has finished using the data. It also ensures that data is not lost when devices having inherently different speeds communicate on the same bus.

1-10. FUNCTIONS OF DEVICES ON THE HP-IB

Devices connected to the bus must be addressed by the Controller before they can function in one or more of the following ways:

TALKER — Any device that is capable of sending or transmitting information on the bus. There can be only one talker at a time on the bus.

LISTENER — Any device that is capable of receiving or accepting information on the bus is a listener. There may be up to 14 listeners at the same time on the bus.

TALKER-LISTENER — An device that has the capablility of both sending and receiving information on the bus as defined previously is both a talker and listener. For example, a counter is a talker when sending data and a listener when it is being programmed.

CONTROLLER — Any device that has been programmed to have the responsibility of managing the flow of information between devices connected to the bus is a controller. It is capable of addressing one of the devices as a talker and one or more of the others as listeners. The HP-IB permits a system to have more than one controller, but only one controller may be active at a time. (The Controller-in-Charge may be the System Controller.)

SYSTEM-CONTROLLER — The system designer must designate one device as the System Controller at the time

the system is configured. The device performs all the functions of a Controller plus it has the ability to gain absolute control of the HP-IB for programming device modes (asserting IFC and REN), collecting and processing data, etc.

1-11. HP-IB BUS LINES

The HP-IB structure consisting of 16 signal lines is shown in Figure 1-4. There are eight additional bus conductors: one ground, one cable shield, and six twisted pair commons for six of the signal lines.

All 16 signal lines have been given names and mnemonic acronyms that describe the message being carried on that line. There are three types of lines: Data (8), Transfer (handshake) (3), and Control (management) (5).

1-12. CONTROL LINES

NOTE

All devices connected to the bus, including the controller, must conform to these descriptions.

The five control lines are used to manage the flow of information over the data and transfer lines. They communicate control and status information between the active controller and the devices connected to the bus. All devices must use ATN and IFC. A device may or may not use REN, SRQ, and EOI.

ATN (Attention) is driven by the active controller to place the bus in either the COMMAND (low) or DATA (high) mode. All other devices must monitor ATN at all times.

When the controller sets ATN to its low state, the bus is in the Command Mode. The primary purpose of the Command Mode is to permit the controller to send commands or address those devices that are to communicate when the bus is placed in the Data Mode. Also, the controller may send "universal commands" while the bus is in the Command Mode.

When the controller sets ATN to its high state, the bus is in the Data Mode. The device that was addressed to talk and those that were addressed to listen will now communicate on the Data Lines.

ATN may be set low or high at any time by a controller, however, it is usually at the end of a transfer (handshake) cycle so that data is not lost. Timing of the transfer lines with respect to ATN is given in paragraph 1-14.

IFC (Interface Clear) is used by the system controller to initialize the bus. Only the system controller can drive IFC and it must be monitored by all other devices on the bus. When the system controller sets IFC low for at least 100 us the following takes place: all talkers and listeners are stopped, serial poll mode is disabled, and control is returned to the HP-IB controller. When IFC is high it has no effect on the bus operation. The system controller may set IFC low at any time.

REN (Remote Enable) is one of the conditions for operating devices under Remote Control. Only devices capable of remote operation use REN and monitor it at all times. Devices that do not use REN terminate the line in a resistive load. Only the system controller may assert REN and may change its state at any time.

SRQ (Service Request) is driven to its low state by a device to indicate that it wants the attention of the controller. SRQ may be set low by a device at any time except when IFC is in the low state. Only the controller senses SRQ. Some devices do not use SRQ but terminate it in a resistive load.

EOI (End or Identify) may be used to indicate the end of a devices character string. When the bus is in the Data Mode (ATN is high), the addressed talker may indicate the end of its data by setting EOI low at the same time it places the last byte on the Data Lines.

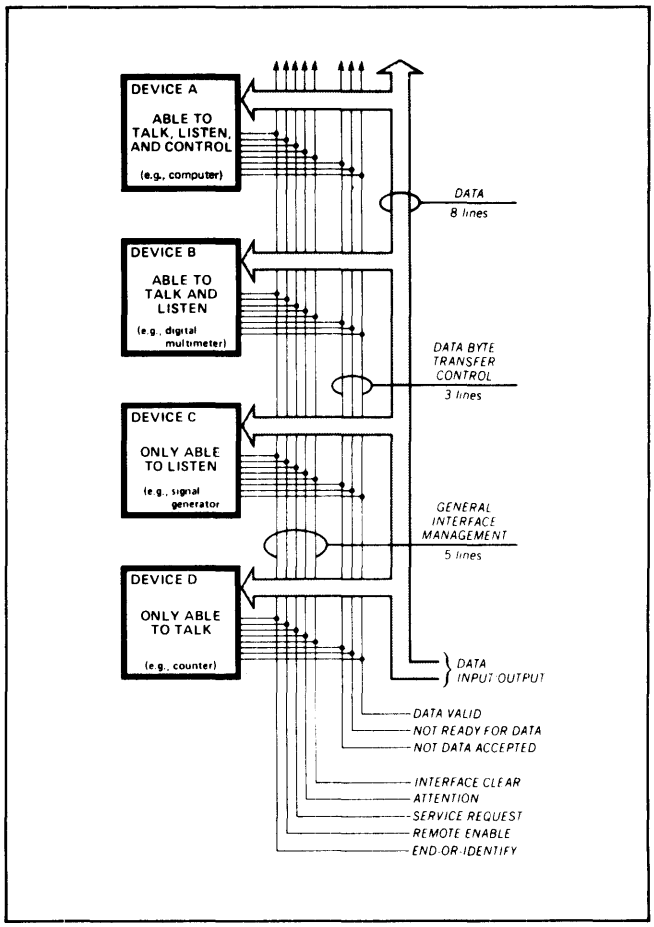


Figure 1-4. HP-IB Bus Structure

1-13. DATA LINES (DIO1-DIO8)

The Data Lines are used to communicate all data including input, output, program codes, addresses, and control and status information between devices connected to the bus. This data is passed character (byte) at a time (i.e., byte serial and bit parallel) under control of the Transfer Lines. Unused data lines terminate in a resistive load in the HP-IB Transceiver chips.

1-14. TRANSFER LINES

Three Transfer (handshake) Lines are used to execute the transfer of each byte of information on the data lines. All devices use these lines and employ an interlocked "handshake" technique to pass information. This allows asynchronous data transfer without timing restrictions being placed on any device connected to the bus. The transfer of each byte is accomplished at the speed of the slowest device. The three transfer lines are: NRFD, NDAC, and DAV.

NRFD (Not Ready for Data) is the transfer (handshake) line that indicates all listeners are ready to accept information on the data lines. NRFD is driven by all the listeners (all devices when ATN is low and only by those devices addressed to listen when ATN is high). It is sensed by talkers: the controller when ATN is low, and the device addressed to talk when ATN is high.

When NRFD is high, all listeners are unconditionally ready for data. The talker may, at its own time, put a byte of information on the data lines and set DAV low. When NRFD is low, one or more listeners are not ready for data.

When the controller sets ATN low, all devices must set NRFD to its high state within 200 ns, i.e., if a device is "Ready for Data" it places NRFD to its high state and if it is "Not Ready for Data" it sets NRFD to its low state. When the controller sets ATN high, all devices that have not been addressed to listen will not drive NRFD, those addressed to listen will set NRFD to its high state within 200 ns.

A listener must not set NRFD low until it senses DAV is low. It may do so before or at the same time that it sets NDAC high. It must not return NRFD to its high state until it senses DAV is high and may do so after, or at the same time that it sets NDAC low.

NDAC (Not Data Accepted) is the transfer line that indicates the acceptance of information on the data lines. NDAC is driven by all listeners. That is, all devices when ATN is low and only those devices addressed to listen when ATN is high. It is sensed by the talker and the controller when ATN is low and by the device addressed to talk when ATN is high.

When NDAC is high, all listeners have unconditionally accepted the byte of information that is on the data lines and no longer need it. The talker may, at its own time set DAV high, remove that byte of information and continue. When NDAC is low, one or more listeners have not accepted the information on the data lines.

When the controller sets ATN low, each device must set NDAC to its high state within 200 ns. When the controller sets ATN high, the devices that have not been addressed to listen will not drive NDAC, those addressed to listen will set NDAC to its high state within 200 ns.

A listener must not set NDAC low until it senses DAV is high. It may do so before or at the same time that it sets NRFD high. It must not return NDAC high until it senses DAV is low and it may do so after or at the same time that it sets NRFD low.

DAV (Data Valid) is the transfer line that indicates the validity of information on the data lines. DAV is driven by the talkers: the controller when ATN is low and the device addressed to talk when ATN is high. ATN is sensed by the listeners and by all devices if ATN is low and by those devices addressed to listen when ATN is high.

When DAV is low, the states of data lines DIO1 through DIO8 are unconditionally valid and may be accepted by all listeners at their own time. DAV can only be driven low if NRFD and IFC are high. When DAV is high, the information on the data lines is not valid. DAV cannot be set high unless NDAC is high and NRFD is low.

The talker has the responsibility of allowing enough time for cable rise time and ringing. It does this with DAV. After placing the bus in the Address Mode (setting ATN low), the controller must wait at least one microsecond before setting DAV low. Of course it must not do so unless NRFD is high. In either the Address or Data Mode, a talker designed with open-collector circuits must not set DAV low for at least two microseconds after placing valid data at its output connector. Those designed with tri-state logic must wait at least 500 ns.

The previous conditions are summarized in Tables 1-2 and 1-3.

1-15. DATA TRANSFER

The transfer of data on the bus is asynchronous and therefore, places no restrictions on the data rates of devices connected to the bus. The timing and levels required to transfer a byte of data on the data lines are shown in Figure 1-5. The transfer is under the control of three lines DAV, NRFD, and NDAC. The talker (sender of data) drives the Data Lines and DAV (Data Valid) and the listeners (acceptors of data) drive both NRFD (Not Ready for Data) and NDAC (Not Data Accepted).

The transfer of a byte of data is initiated by all listeners signifying they are ready for data by setting NRFD high.

Table 1-2. Relation of ATN and Transfer (Handshake) Lines (NRFC, NDAC, and DAV)

MODE	ATN	NRFD		NDAC		DAV	
		LOW	HIGH	LOW	HIGH	LOW	HIGH
COMMAND	LOW	One or more units not ready for data	All units ready for data	One or more units have not accepted data	All units have accepted data	Controller has valid data on DIO lines	Controllers data is not valid
		1. Driven by all units except controller 2. Sensed by controller 3. All units set NRFD and NDAC to valid state within 200 nanoseconds after ATN goes LOW				1. Driven by controller 2. Sensed by listeners 3. See DAV above for timing	
DATA	HIGH	One or more listeners not ready for data	All addressed listeners ready for data	One or more listeners have not accepted data	All addressed listeners have accepted the data	The addressed talker has valid data on lines	The addressed talker data is not valid
		1. Driven by all units addressed to listen. 2. Sensed by the unit addressed to talk. 3. All units not addressed will not drive. 4. All addressed listeners set both NRFD and NDAC to valid within 200 nanoseconds after ATN goes HIGH.				1. Driven by the devices addressed to TALK. 2. Sensed by all devices addressed to LISTEN 3. See DAV above for timing.	

Table 1-3. Summary of Bus Timing

IFC INTERFACE CLEAR	The System Controller must set IFC low for at least 100 microseconds to clear the bus.
TRANSFER LINES WITH RESPECT TO ATN	When sending an Address or a Universal Command the controller may set DAV low only after sensing that NRFD is high, and ATN has been low for at least one microsecond. When a controller changes ATN from its high to the low state or from low to high, all Listeners (all devices when ATN is low and those addressed to Listen when ATN is high) put both NRFD and NDAC to their high state in less than 200 nanoseconds.
TRANSFER LINES WITH RESPECT TO THE DATA	After changing the information on one or more Data Lines, the *talker* (the Controller when ATN is low or the device addressed to talk when ATN is high) must wait before setting DAV low. It waits 2 μs if designed with open-collector circuits and 500ns if designed with tri-state integrated circuits at standard speed. It must wait 350ns if operated at high speed.

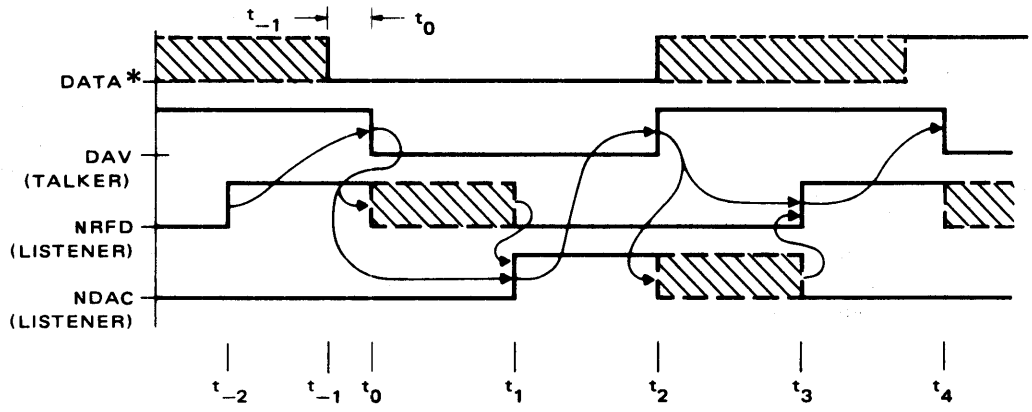
When the talker recognizes NRFD is high and has placed valid data on the data lines, then it sets DAV low. When the listeners sense that DAV is low and have finished using the data, they set NDAC high. Notice that the assertive or active state of both NRFD and NDAC is high. Since all devices on the bus have their corresponding lines connected together (e.g. NRFD), all listeners must be in a high state before that line goes high. This wired-AND condition allows a talker to recognize when the slowest listener has accepted a byte of data and is ready for the next byte.

Figure 1-5 also shows the timing of the transition to the non-assertive state of these lines. A listener may set NRFD low as soon as it recognizes that DAV has been set low and must do so before or at the same time it sets NDAC high. The talker may return DAV to its high state after it detects that NDAC is high. A listener may set NDAC low as soon as it recognizes that DAV is high and must do so before or at the same time it sets NRFD to its high state.

1-16. HP-IB ELECTRICAL CHARACTERISTICS

All 16 bus lines are designed to be compatible with TTL integrated circuits. Each line is terminated within the

SEQUENTIAL REQUIREMENTS OF THE THREE WIRE TRANSFER



EVENTS

t_{-2} : Listener becomes ready to accept data.

t_{-1} : Talker has put data on the lines.

t_0 : Indicates data is valid.

t_1 : Listener has accepted the data and no longer requires it held valid.

t_2 : Talker indicates the data is no longer valid and may change it.

t_3 : Listener indicates it is ready for new data.

t_4 : A new cycle begins (equivalent to t_0).

t_{-1} to t_0 : Time that data is put on lines before DAV is set low.

* A composite of the DIO1 through DIO7 lines for illustrative purposes. The curved lines indicate transfer (handshake) signal sequence.

Figure 1-5. Transfer Timing

Transceiver chips into a resistive network consisting of a 2.3 kohm resistor to +5V and a 4.7 kohm resistor to logic common. Typically, the required bus terminations are internally provided by the Transceiver chips. Optional load resistors (R11, R12, R13, and R14) form an external divider consisting of a 330 ohm resistors to +5V and 680 ohm resistors to logic common that can be used to provide the drive for seven additional loads. Load resistors of other values may be required if the optional load resistors do not supply sufficient drive for specific applications. The selection of these resistors is covered in Section II.

Each driver/receiver pair (see Figure 1-6) forms a complete interface between the bus and a device. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive (S/R) input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver to be operated in an open collector or active pull-up configuration. The receivers have input hysteresis to improve the noise margin and their input loading follows the bus standard.

The driver/receiver pairs provide the following:

Driver: When a talker, it is capable of sinking 48 mA at 0.4V.

Receiver: When a listener, it requires −1.3 mA at 0.4V to drive.

1-17. HP-IB PHYSICAL CHARACTERISTICS

Bus cables are available for connecting devices into a system. These have one overall shield to reduce susceptibility to external noise. The cables use a mixture of individual wires and twisted pairs to reduce crosstalk. The connectors on both ends of the cables are identical as they are terminated in two 24-pin piggy back connectors; one male and one female. The pin connections of these connectors are shown in Figure 1-7.

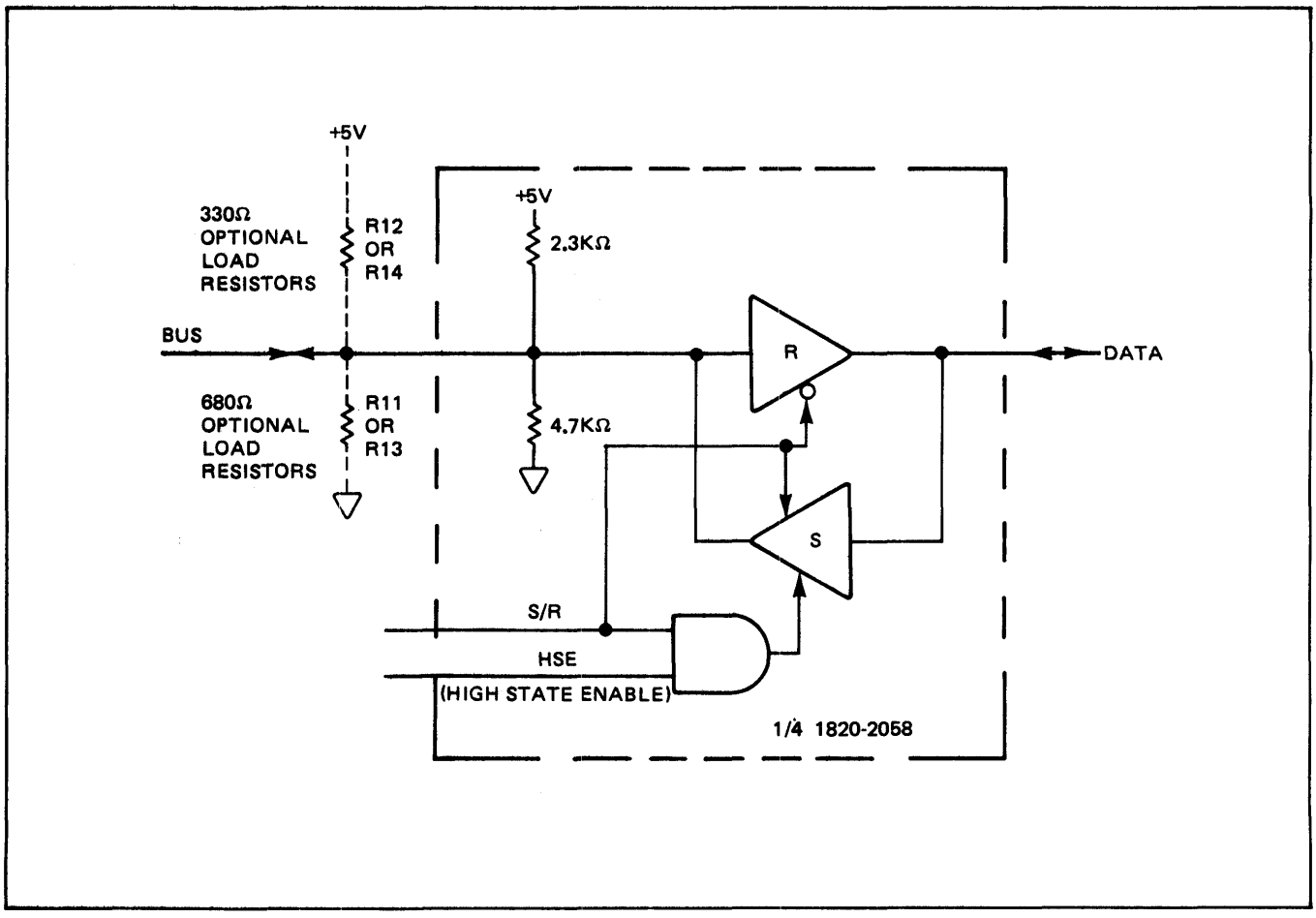


Figure 1-6. Typical HP-IB Transceiver (Driver/Receiver) Circuit

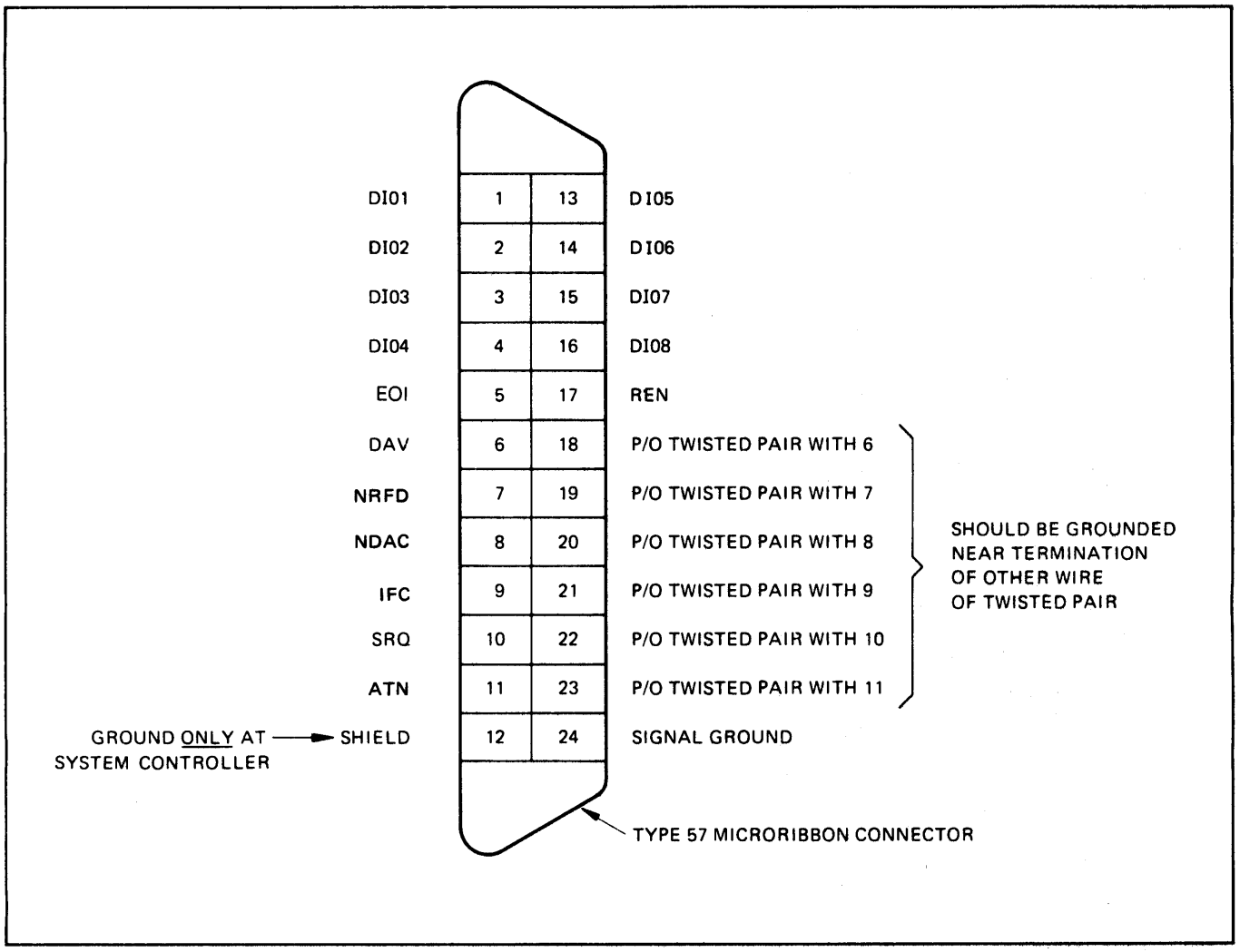


Figure 1-7. HP-IB Cable Connector Pin Connections

SECTION II
INSTALLATION

2-1. INTRODUCTION

This section provides information on unpacking, inspecting, installing, and checking the operation of the HP 12009A HP-IB Interface.

2-2. UNPACKING AND INSPECTION

CAUTION

STATIC SENSITIVE DEVICES
Use Antistatic handling procedures when handling the printed circuit assemblies.

If the HP-IB Interface is ordered with a computer, the card is installed in the computer at the factory. When this is the case, it is necessary only to check the operation of the peripheral device and the HP-IB Interface, after the peripheral device and the computer are installed. Checkout instructions are furnished in paragraph 2-13. If the HP-IB Interface is ordered separately, inspect the carton containing the card before opening it. If there is evidence of damage, if water stains are visible, or if the box rattles, request that the carrier's agent be present when the box is opened.

Inspect each portion of the package as the parts are unpacked. Look for such damage as cracks, dents, broken components, detached parts, corrosion, water damage, etc. If any part of the package is damaged, retain the carton, packing material, and shipping papers, and immediately notify the carrier and the nearest HP Sales and Service Office. The Sales and Service Office will arrange for repairs or replacement of the damaged parts without waiting for settlement of claims against the carrier. The HP Sales and Service Offices are listed in the back of this manual.

After inspecting all parts and components, refer to paragraph 1-3 to insure that the package is complete. Also, check the part numbers listed on the title page against the part numbers on the components in the package. If the package is incomplete, or if an incorrect component has been supplied, notify the nearest HP Sales and Service Office.

2-3. PREPARATION FOR INSTALLATION

2-4. COMPUTATION OF POWER REQUIREMENTS

The HP-IB Interface obtains its operating power from the computer's power supply through the backplane. Before installing the card, it is necessary to determine whether the additional current drain will overload the power supply. If the card was installed at the factory, the required calculations have been made and it has been determined that an overload will not occur. The current and voltage requirements for the HP-IB Interface are listed in Table 1-1.

2-5. INTERFACE REQUIREMENTS

2-6. BACKPLANE TO HP-IB INTERFACE

All interaction between the HP-IB Interface, the Processor Card, and the Memory Card occurs on the backplane. Connections from the backplane to the HP-IB Interface are listed in Tables 2-1 and 2-2.

2-7. SWITCH SELECTABLE OPTIONS

The switch selectable options are as follows: the Select Code (6-bits), the HP-IB Address (8-bits), HP-IB System Controller (1-bit), and the Settling Time Selection (1-bit). The locations of the two DIP switches (U1 and U16) are shown in Figure 2-1. Each DIP switch assembly contains eight independent switches. U16 is labelled from 0 to 7 for the Address Select Bits (see Figure 2-2). The last six switches on U1 (U1S3-S8) determine the Select Code for the card (see Figure 2-3).

2-8. HP-IB ADDRESS SELECTION

Switches U16S1 through U16S8 (see Figure 2-2) determine the HP-IB address and related control functions when loaded into the PHI Chip's Register 7 under software control. The switch functions are as follows:

Switch U16S1 (Bit 7)— Puts the PHI Chip "online" when set to the open (up) position.

Table 2-1. Backplane Connections, Connector P1

P1-	SIGNAL NAME	SIGNAL DEFINITION
1	ICHID-	Interrupt Chain In Disable
2	ICHOD-	Interrupt Chain Out Disable
3	MCHID-	Memory Chain In Disable
4	MCHOD-	Memory Chain Out Disable
5	MLOST-	Memory Lost
6	MCHODOC-	Memory Chain Out Disable Open Collector
7	PFW-	Power Fail Warning
8	SPARE 1	
9	SC0	Address Extension Bus Bit 0
10	SC1	Address Extension Bus Bit 1
11	SC2	Address Extension Bus Bit 2
12	SC3	Address Extension Bus Bit 3
13	GND	
14	GND	
15	SPARE 2	
16	GND	
17	SC4	Address Extension Bus Bit 4
18	SC5	Self Configure
19	AB0	Address Bus Bit 0
20	AB1	Address Bus Bit 1
21	AB2	Address Bus Bit 2
22	AB3	Address Bus Bit 3
23	AB4	Address Bus Bit 4
24	AB5	Address Bus Bit 5
25	AB6	Address Bus Bit 6
26	AB7	Address Bus Bit 7
27	AB8	Address Bus Bit 8
28	AB9	Address Bus Bit 9
29	AB10	Address Bus Bit 10
30	AB11	Address Bus Bit 11
31	AB12	Address Bus Bit 12
32	AB13	Address Bus Bit 13
33	AB14	Address Bus Bit 14
34	WE-	Write Enable
35	DB0	Data Bus Bit 0
36	DB1	Data Bus Bit 1
37	DB2	Data Bus Bit 2
38	DB3	Data Bus Bit 3
39	DB4	Data Bus Bit 4
40	DB5	Data Bus Bit 5
41	DB6	Data Bus Bit 6
42	DB7	Data Bus Bit 7
43	DB8	Data Bus Bit 8
44	DB9	Data Bus Bit 9
45	DB10	Data Bus Bit 10
46	DB11	Data Bus Bit 11
47	DB12	Data Bus Bit 12
48	DB13	Data Bus Bit 13
49	DB14	Data Bus Bit 14
50	DB15	Data Bus Bit 15

Table 2-2. Backplane Connections, Connector P2

P2-	SIGNAL NAME	SIGNAL DEFINITION
1	CPUTURN-	Processor Turn
2	GND	
3	REMEM-	Remote Memory
4	VALID-	Data Valid
5	IORQ-	I/O Handshake Request
6	INTRQ-	Interrupt Request
7	MP	Memory Protect
8	RNI-	Read Next Instruction
9	MEMGO-	Memory Cycle Initiation
10	PE-	Parity Error
11	SCHID-	Slave Chain In Disable
12	SCHOD-	Slave Chain Out Disable
13	IAK-	Interrupt Acknowledge
14	IOGO-	I/O Handshake Request Acknowledge
15	GND	
16	SLAVE-	Slave Request
17	GND	
18	MRQ-	Memory Request
19	GND	
20	FCLK-	Fast Clock
21	GND	
22	CCLK-	Communications Clock
23	PINT-	Priority Interrupt
24	SCLK-	System Clock
25	CRS-	Control Reset
26	PON	Power On
27	GND	
28	BUSY-	Memory Busy
29	GND	
30	GND	
31	GND	
32	GND	
33	GND	
34	GND	
35	+5V	
36	+5V	
37	+5V	
38	+5V	
39	+12M	
40	−12M	
41	+12V	
42	+12V	
43	−12V	
44	−12V	
45	+5M	
46	+5M	
47	AC∅2	
48	AC∅2	
49	AC∅1	
50	AC∅1	

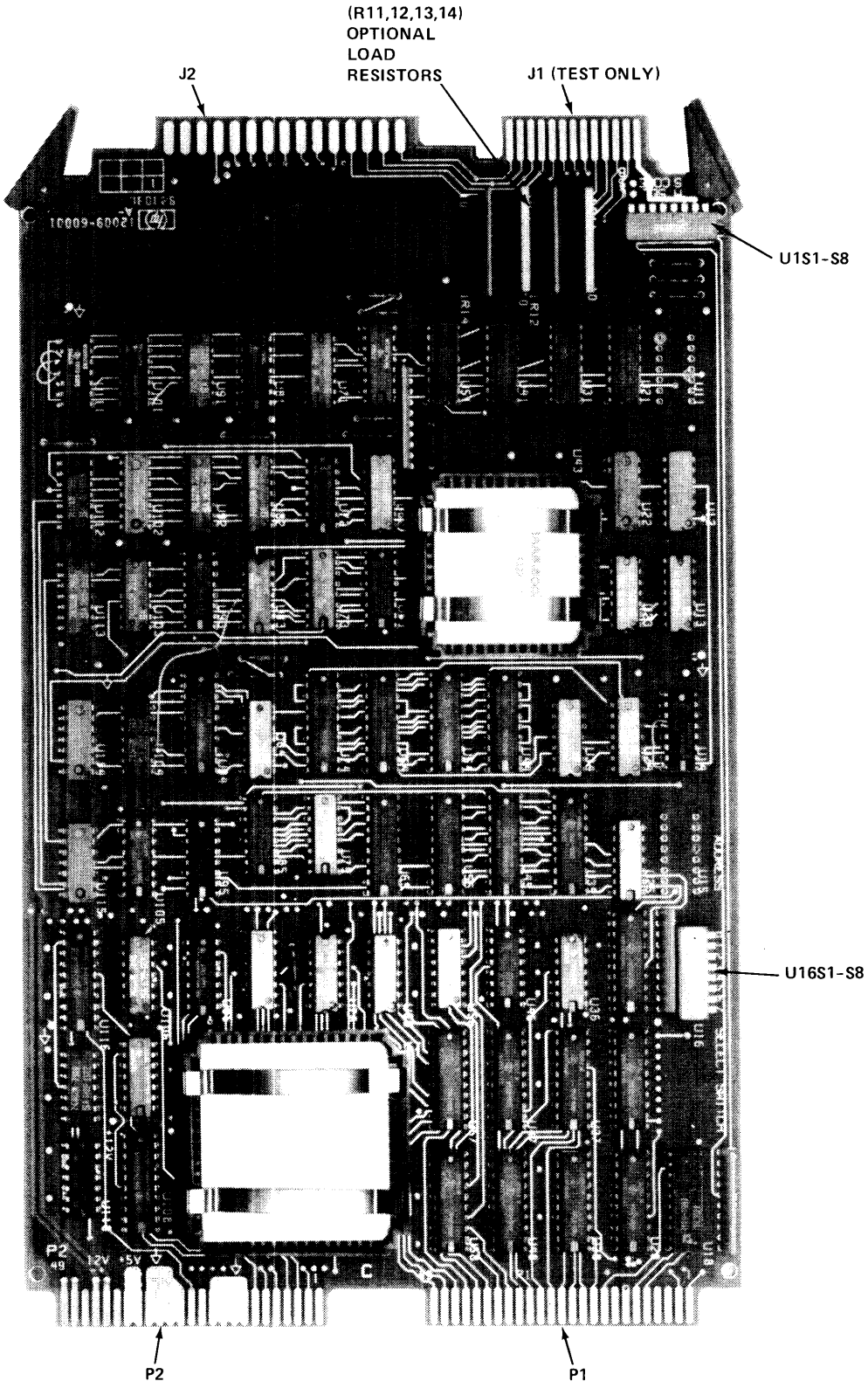


Figure 2-1. HP-IB Interface Card HP 12009-60001

Switch U16S2 (Bit 6)— Puts the PHI Chip into the "TALK ALWAYS" mode when the switch is in the open (up) position.

Switch U16S3 (Bit 5)— Puts the PHI Chip into the "LISTEN ALWAYS" mode when the switch is in the open (up) position.

Switches U16S4 through U16S8 (Bits 4 through 0)- The value of these five bits determine the HP-IB address to which the PHI Chip will respond.

2-9. SELECT CODE SELECTION

Switches U1S3 through U1S8 (see Figure 2-3) determine the select code for the HP-IB Interface. An open switch represents a logic 1 and a closed switch represents a logic 0. U1S3 represents the Most Significant Bit (MSB) and U1S8 represents the Least Significant Bit (LSB).

2-10. SYSTEM CONTROLLER SELECTION

The switch U1S1 (see Figure 2-3) determines if the HP-IB Card will be the system controller for the bus. If the switch is put in the open (up) position, the card will function as the system controller.

2-11. DATA SETTLING TIME SELECTION

The switch U1S2 (see Figure 2-3) determines the time delay between the assertion of the data on the bus and the assertion of the data valid signal (DAV). With the switch in the normal open (up) position, a delay of approximately 500 ns is realized. When the switch is placed in the closed (down) position, the delay is reduced to approximately 350 ns. This delay time satisfies the IEEE Standard 488-1978 for fast settling time required for high speed operation (refer to paragraph 2-18 for further information on high speed operation).

2-12. INSTALLATION

CAUTION

STATIC SENSITIVE DEVICES
Use antistatic handling procedures when handling the printed circuit assemblies.

Figure 2-2. U16S1-U16S8 HP-IB Address Selector Switches

After ensuring that the computer's power supply can handle the added load, (see paragraph 2-4), perform the following steps:

a. Set switch U1S1 opened or closed depending on whether or not the HP-IB Interface is going to operate as a system controller (see paragraph 2-10).

b. Set switch U1S2 opened or closed depending on whether or not the HP-IB Interface is going to require the normal or the fast settling time mode of operation (see paragraphs 2-11 and 2-18). All high speed devices should be appropriately labelled. High and standard speed devices cannot be connected to the same bus.

c. Set the select code for the HP-IB Interface with switches U1S3 through U1S8 (see paragraph 2-9).

d. Set the HP-IB Address for the HP-IB Interface with switches U16S4 through U16S8 (see paragraph 2-8).

e. Turn off the power to the computer and the I/O device. Insert the HP-IB Interface into the desired slot in the backplane. Make sure that the components on the card are on the same side as the other interface cards in the backplane. When installing the card, use care not to damage the card or any adjacent cards. Press the card firmly into place.

f. Connect the appropriate cable from the bus to the card. There are two connectors (J1 and J2) on the back edge of the card (see Figure 2-1). Connector J2 connects to the HP-IB cable. Connector J1 is only for test purposes.

2-13. CHECKOUT

To verify operation of the HP-IB Interface, refer to Section V, paragraph 5-6, steps 1, 2, and 3.

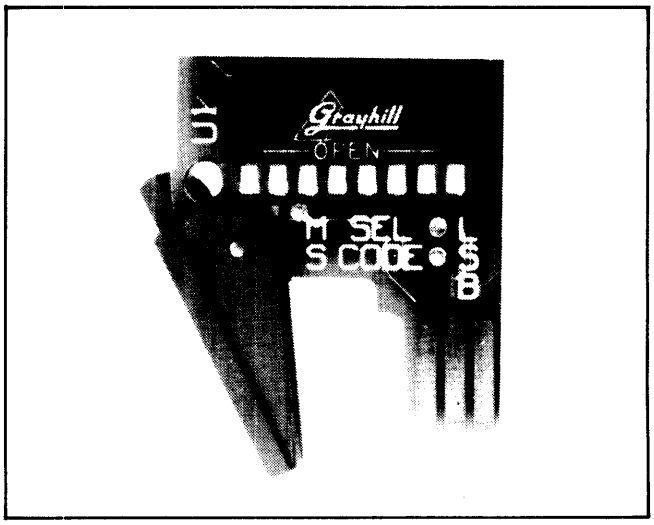


Figure 2-3. U1S3-U1S8 Card Select Code Switches

2-14. INTERCONNECTING CABLES

2-15. INTERFACE CARD CABLE

A two metre cable (part no. 12009-60007) is supplied with the card. The cable has a 30-contact printed circuit edge connector on one end and a standard piggy-back HP-IB connector on the other end. The printed circuit edge connector is to be connected to J2 (see Figure 2-1). The pin connections for the interconnecting cable are shown in Table 2-3.

The HP-IB connector end is connected to the peripheral device. Other devices may be added to the bus by using the standard HP-IB cables (not supplied), that are listed in Table 2-4.

2-16. CABLING LENGTH RESTRICTIONS

2-17. NORMAL OR LOW SPEED OPERATION (U1S2 OPEN). In order to ensure proper operation of the bus, two rules must be observed regarding the total length of bus cables being used. These rules are as follows:

a. All devices on the bus must be the same speed (see paragraph 2-12b).

b. The total length of cable permitted to be used with one interface card must be less than or equal to two metres times the number of device connected together. The interface card is counted as one device.

c. The total maximum length of cable must not exceed 20 metres.

Rule (b) implies that there may be up to 4 metres of cable between the first two devices (2 units X 2m/device = 4m). Additional units may be added using 2 metre cables up to a total of 10 units (10 units X 2m/device = 20m); e.g., using one 4m and eight 2m cables (4+[8X2] = 20). If more than 10 devices are to be connected together, cables shorter than two metres must be used between some of the devices. For example, 15 devices can be connected together using one 4m cable and 13 one-metre cables (4+[13X1] = 17). Other combinations may be used as long as the requirements of rules (b) and (c) are met. In making the calculations, remember to count the interface card as one device.

2-18. HIGH SPEED OPERATION (U1S2 CLOSED). To achieve the maximum possible data transfer rate (nominally 930 kbytes per second) within a system, the following guidelines should be followed:

a. All devices expected to talk at the higher rates must use a settling time of 350 nanoseconds or less..

b. All devices expected to operate at the higher rates should use 48 mA three-state drivers.

Table 2-3. HP-IB Interface to Bus Connector (J2)

J1 (TEST ONLY)		J2 (HP-IB)	
PIN	**NAME**	**PIN**	**NAME**
1	GET–	1	DIO1
2	+5V	2	DIO2
3	CMN	3	DIO3
4	NC	4	DIO4
5	CMN	5	EOI
6	ATN	6	DAV
7	CMN	7	NRFD
8	SRQ	8	NDAC
9	CMN	9	IFC
10	IFC	10	SRQ
11	CMN	11	ATN
12	NDAC	12	NC
13	CMN	13	NC
14	NRFD	14	NC
15	CMN	15	NC
16	DAV	A	DIO5
17	REN	B	DIO6
18	EOI	C	DIO7
19	DIO8	D	DIO8
20	DIO5	E	REN
21	DIO7	F	CMN
22	DIO3	H	CMN
23	DIO6	J	CMN
24	DIO2	K	CMN
25	DIO5	L	CMN
26	DIO1	M	CMN
		N	CMN
		P	CMN
		R	CMN
		S	NC

Table 2-4. Accessory HP-IB Bus Cables

LENGTH	ACCESSORY NUMBER
1 metre	10833A
2 metres	10833B
4 metres	10833C
0.5 metres	10833D

c. The device capacitance on each lead (REN and IFC excepted) should be less than 50 pF per device. In a system configuration the total device capacitance should be no more than 50 pF for each equivalent resistive load in the system.

d. Interconnecting cable links should be as short as possible with a maximum of 15 m total length per system.

e. There must be at least one equivalent load for each metre of cable. Using the following information, determine the value of load resistors required for your system.

m = metres of cable; load = Device Load Equivalents

Case 1. m− load = N ≤ 0

As long as N remains less than or equal to 0, the optional load resistor packs are not required.

Case 2. m− load = N > 0 and less than eight devices are required.

Install optional load resistor packs provided with the card into the sockets provided. Be sure the resistor packs are properly oriented (see Figure 2-1). This will provide the drive for seven equivalent loads. The system is now limited to eight devices on the bus.

Case 3. m− load = N > 0 and more than eight devices are required.

The optional resistors provided with the card will not meet the requirements for this system. Therefore, the following formulas will have to be used to determine the correct values of the load resistors to be used. Follow the rules closely or the card may be damaged.

$$\text{R12 or R14} = \frac{2.3 \text{ kohms}}{N}; \quad \text{R11 or R13} = \frac{4.7 \text{ kohms}}{N}$$

If the power applied to the HP-IB Interface card is lost while the optional resistors are being used, the HP-IB Bus will be pulled down.

Figure 2-5 illustrates four systems, two that illustrate Case 1, one that illustrates Case 2, and one that illustrates Case 3 in selecting the value of the load resistors.

When the HP-IB Card is configured for high speed operation, the High Speed Operation Card (see Figure 2-4) must be attached to the device end of the HP-IB Interface Cable. This card is supplied with the HP-IB Interface (see Section I, paragraph 1-3).

2-19. CABLING CONFIGURATIONS

It is recommended that no more than three or four piggyback connectors be stacked together on one device. The resulting structure can exert great force on the panel of the device where the connector is mounted and could cause mechanical damage.

The configuration may be linear (all cables connected end to end) or in a star (all cables branching out from a central point) or any combination of both configurations.

2-20. RESHIPMENT

If an item of the package or the complete package is to be returned to the nearest Hewlett-Packard Sales and Service Office for repair, attach a tag to the item identifying the owner and indicating the service to be performed.

Pack the item in the original factory packing material, if available. If the original material is not available, an equivalent type of commerical packaging material should be used. Reliable commerical packing and shipping companies have the facilities and materials to adequately repack the item.

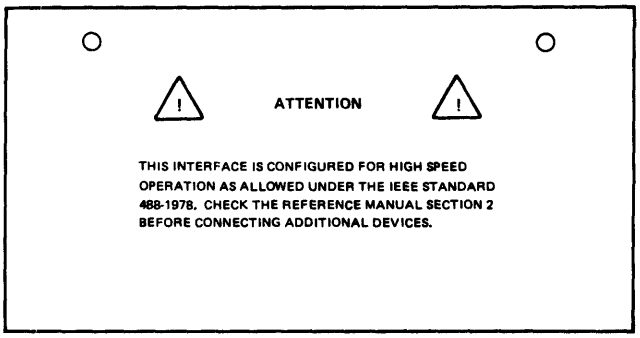


Figure 2-4. HP-IB High Speed Operation Card

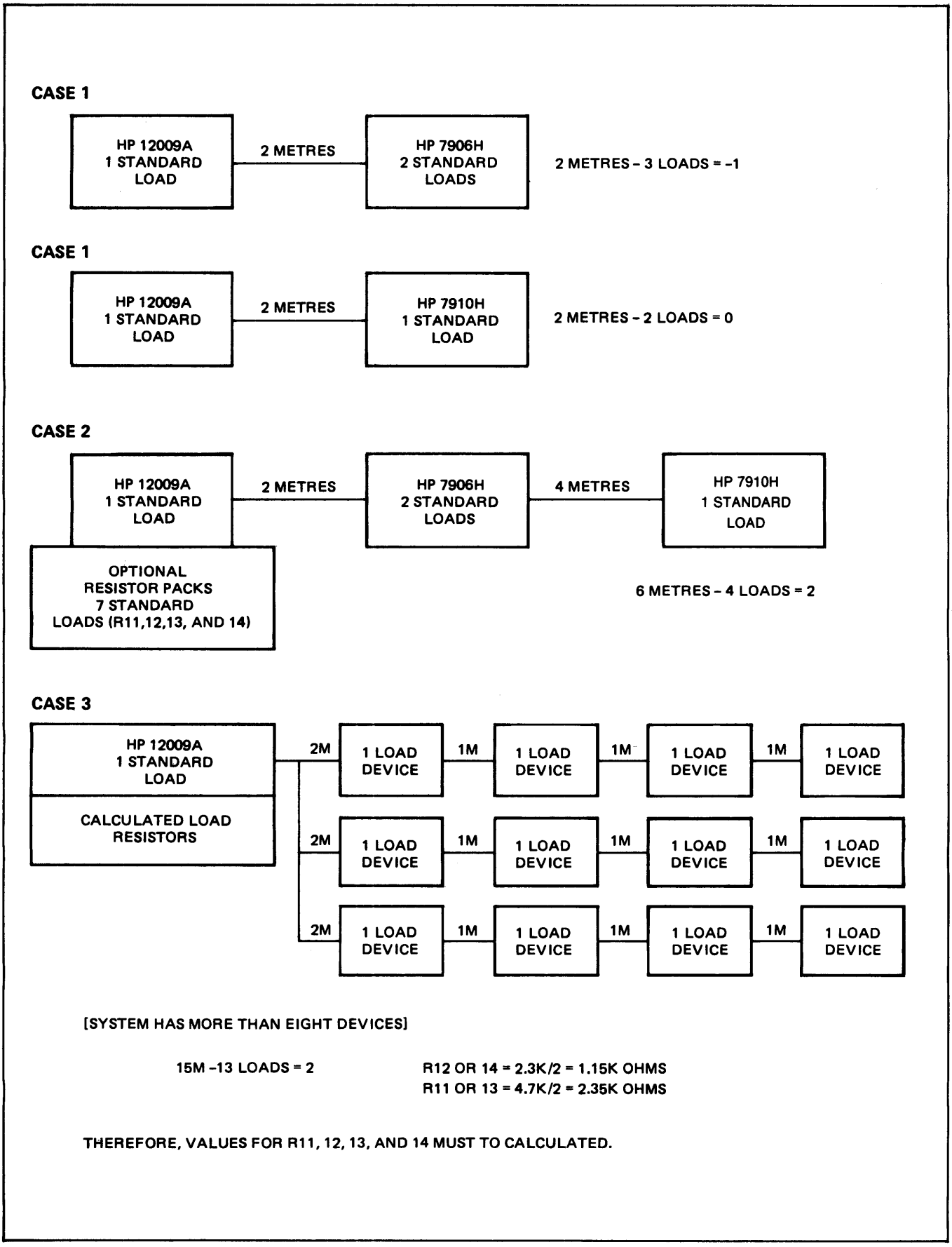


Figure 2-5. HP-IB System Examples

PROGRAMMING

SECTION III

3-1. INTRODUCTION

This section provides assembly-language programming procedures for the HP-IB Interface. For information on assembly-language programming, refer to the HP 1000 L-Series Reference Manual, part number 02103-90007.

This card has many capabilites such as handling its own Direct Memory Access (DMA), decoding its own instructions from the processor, byte packing and unpacking, and supporting fully the HP-IB functions listed in Section I, paragraph 1-8.

NOTE

It is recommended that the L-Series user begin driver development utilizing the HP supported driver, part number 92070-16095.

3-2. USE OF THE GLOBAL REGISTER

Every L-Series Interface card is comprised of two sections : an I/O Master Section and a Peripheral Device Section. The I/O Master Section performs all of the I/O processing functions for the computer. These functions include I/O instruction recognition and execution, and direct memory accessing (DMA). The I/O Master consists of the I/O Processor (IOP) Chip and its associated logic circuitry. The Global Register (GR) is located in the I/O Processor Chip and is a six-bit register that contains a select code. See Figure 3-1 for a simplified block diagram of the I/O Processor Chip (U67).

All global registers on all interface cards are controlled by the CPU, thus all global registers contain the same select code. The global register may be loaded with an OTA 2 or OTB 2 I/O instruction, enabled with a CLF 2 I/O instruction, and disabled with an STF 2 I/O instruction. When the global register is enabled, any I/O instruction that is executed by the CPU automatically applies to the card whose select code is in the global register. For the HP-IB card for example, if the global register contains the HP-IB card's select code, the current I/O instruction is decoded and executed by the HP-IB card. Using the global register to store the select code frees the six least significant bits of the I/O instructions. These bits do not need to store the select code of the I/O card to receive the I/O instruction. Thus, these six bits can be used to address a register on the I/O interface cards. On the HP-IB card, there are three such registers: one for data, one for status, and one for control, in addition to registers which are internal to the I/O Processor Chip.

Data may be transferred to and from the HP-IB card with or without the global register enabled. To access the card's control and status registers, however, the global register must be enabled.

3-3. I/O INSTRUCTION SET

The I/O Master executes the following twelve I/O instructions:

CLC	Clear Control
CLF	Clear Flag
LIA	Load Into A
LIB	Load Into B
MIA	Merge Into A
MIB	Merge Into B
OTA	Output A
OTB	Output B
SFC	Skip if Flag Clear
SFS	Skip if Flag Set
STF	Set Flag
STC	Set Control

The six-bit global register allows a maximum of 64 (decimal) select codes. The I/O Master, however, executes only a portion of these. Select code 00 through 17 (octal) are reserved for the CPU, leaving 20 through 77 (octal) available for the I/O system. For further information on the I/O instruction set, refer to the L-Series Reference Manual, part number 02103-90007.

3-4. INSTRUCTION USAGE SUMMARY

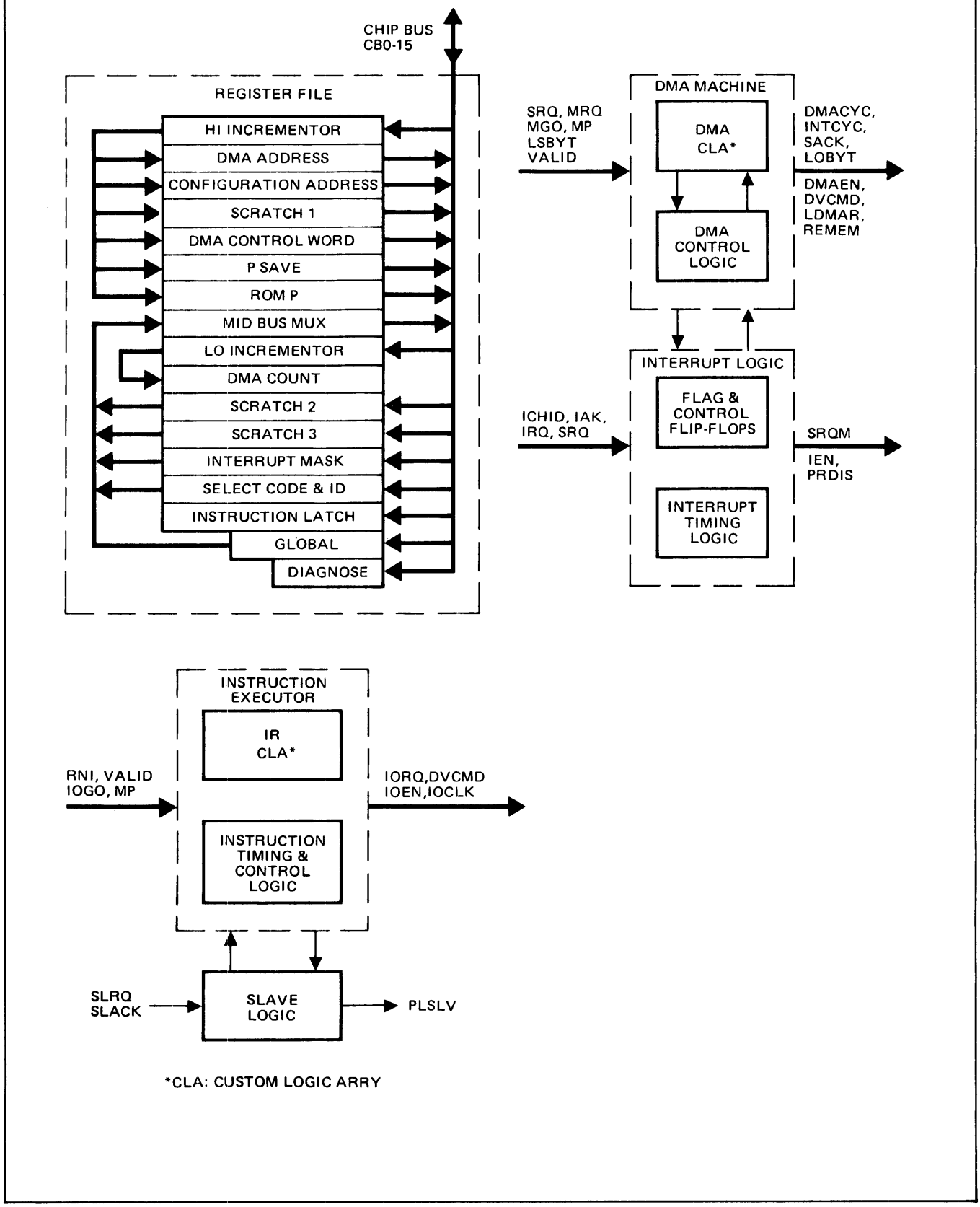
Table 3-1 lists all ot the instructions recognized by the I/O Processor Chip by their select code. There are three conditions relevent to the instruction's execution. These conditions are as follows:

a. Is the global register (GR) enabled?

b. Do the contents of the GR equal the I/O Processor Chip's select code, (GR=SC)?

c. Do the lower six bits of the instruction equal the I/O Processor Chip's select code, (IR=SC)?

This summary indicates which conditions must be met for instruction execution by listing in each column: Y for yes, N for no, and X for don't care.



7700-464

Figure 3-1. IOP Chip (U67) Block Diagram

3-5. HP-IB CAPABILITY

The HP-IB capability of the card is based on the use of the PHI Chip (Processor to HP-IB Interface). To facilitate control of the PHI Chip (U43) and the card, and to reduce the software operating system overhead required to service the card, the direct memory access (DMA) capability provided by the L-Series computer's architecture is utilized. Figure 7-2 is a block diagram of the HP-IB card showing data paths, data and control registers, and the required control functions.

3-6. PHI CHIP

HP-IB operations are directed by the sequence of control words sent to the PHI Chip's registers. HP-IB data or status may be read from the PHI Chip's registers. Figure 3-2 shows a block diagram of the PHI Chip.

The PHI Chip's eight internal registers are accessed through a common 10-bit bus (PHI Bus). The desired PHI register is selected through the three register select inputs (A13,A14, and A15). A read/write input (WRITE, U43 pin 16) selects the direction of the data flow. The PHI Chip's register numbers and functions are given in the following table:

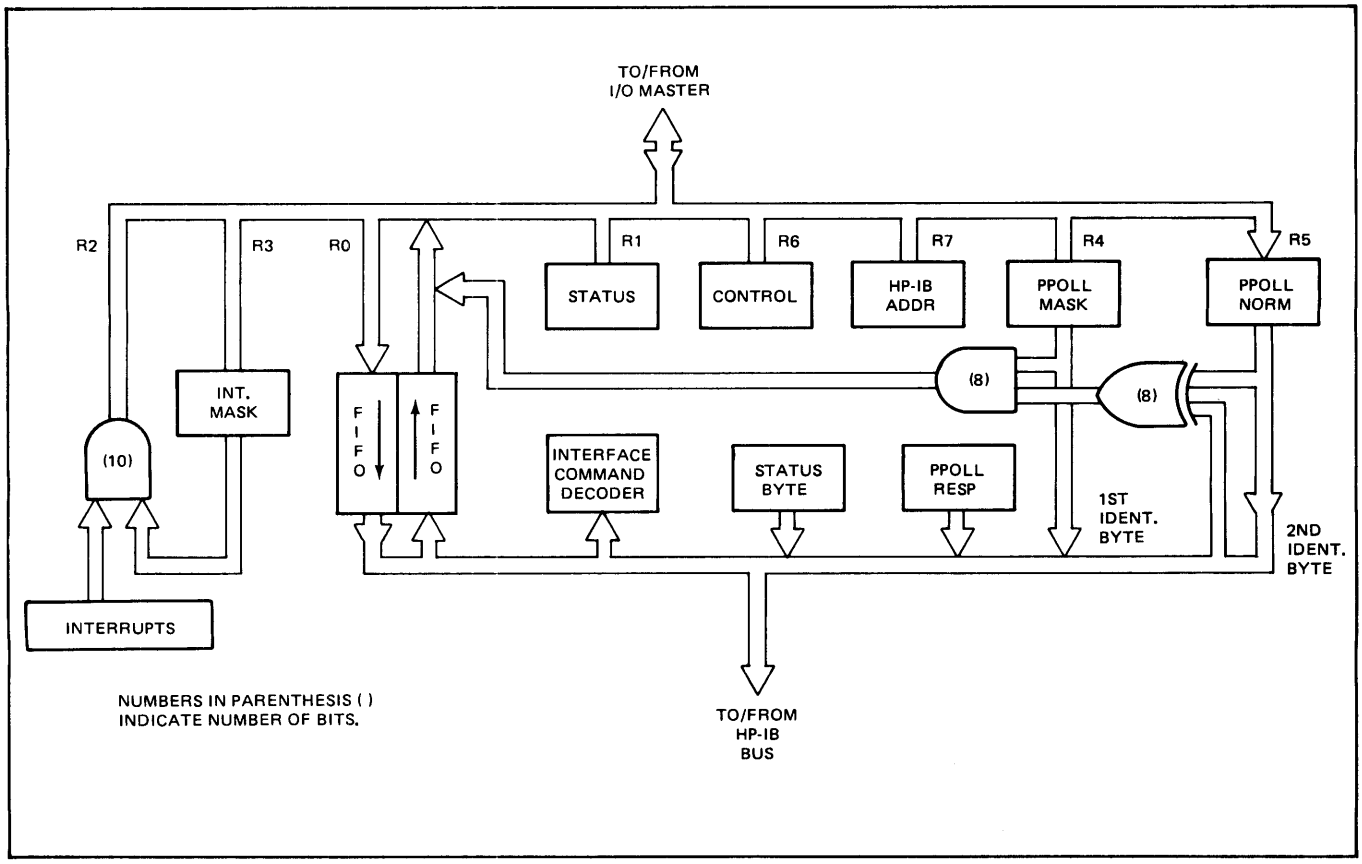
SOFTWARE NO.	FUNCTION
0	HP-IB FIFOs
1	PHI Chip Status
2	PHI Chip Interrupts
3	PHI Chip Interrupt Mask
4	Parallel Poll Mask
5	Parallel Poll Sense
6	HP-IB Control
7	HP-IB Address

The 16-bit format of words written to the PHI Chip is as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
--	A13	A14	A15	--	--	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	COMPUTER BIT NO. / PHI CHIP BIT NO.
R/W	PHI REGISTER SELECT			0	0	PHI DATA BUS										

1 = READ FROM PHI CHIP
0 = WRITE TO PHI CHIP

In the case of a PHI register read, the PHI REG SELECT and READ bits of the input word are copies of those specified in the output word that selected the register to be read. For example:



7700-485

Figure 3-2. PHI Chip (U43) Block Diagram

Table 3-1. IOP Chip Instructions By Select Code

INSTRUCTION	FUNCTION	GR ON	GR=SC	IR=SC	NOTES
LI* 0	Read interrupt mask	X	Y	X	
MI* 0	Merge interrupt mask	X	Y	X	
OT* 0	Write interrupt mask	X	X	X	
CLF 2	Enable GR	X	X	X	
STF 2	Disable GR	X	X	X	
LI* 2 [,C]	Read GR	X	Y	X	1, 9
MI* 2 [,C]	Merge GR	X	Y	X	1, 9
OT* 2 [,C]	Write GR	X	X	X	
STC 2 [,C]	Enable Slave logic	X	X	X	1, 2
[,C]	Enable GR				
CLC 3	"BREAK" to front panel	X	X	X	2
HLT XX	"BREAK" to front panel	X	X	X	2
LI* 3	Read P SAVE	X	X	X	2
MI* 3	Merge P SAVE	X	X	X	2
OT* 3	Write P SAVE	X	X	X	2
LI* 3,C	Read ROM P	X	X	X	2
MI* 3,C	Merge ROM P	X	X	X	2
OT* 3,C	Write ROM P	X	X	X	2
SFC 20	Skip if FLG 20 clear	Y	Y	X	3
SFS 20	Skip if FLG 20 set	Y	Y	X	
CLF 20	Clear FLG 20 and FLG 21	Y	Y	X	
STF 20	Set FLG 20	Y	Y	X	
STC 20 [,C]	Enable DMA self configuration	Y	Y	X	
CLC 20 [,C]	Disable DMA self configuration	Y	Y	X	
LI* 20 [,C]	Read DMA configuration address	Y	Y	X	
MI* 20 [,C]	Merge DMA configuration address	Y	Y	X	
OT* 20 [,C]	Write DMA configuration address	Y	Y	X	
[,C]	Clear FLG 20 and FLG 21				
SFC 21	Skip if FLG 21 clear	Y	Y	X	4
SFS 21	Skip if FLG 21 set	Y	Y	X	
CLF 21	Clear FLG 21	Y	Y	X	
STF 21	Set FLG 21	Y	Y	X	
STC 21 [,C]	Enable DMA transfers	Y	Y	X	
CLC 21 [,C]	Disable DMA transfers	Y	Y	X	
LI* 21 [,C]	Read DMA Control word	Y	Y	X	
MI* 21 [,C]	Merge DMA Control word	Y	Y	X	
OT* 21 [,C]	Write DMA Control word	Y	Y	X	
[,C]	Clear FLG 21				
SFC 22	Skip if FLG 22 clear	Y	Y	X	5
SFS 22	Skip if FLG 22 set	Y	Y	X	
CLF 22	Clear FLG 22	Y	Y	X	
STF 22	Set FLG 22	Y	Y	X	
CLC 22 [,C]	Force DMA reconfiguration	Y	Y	X	
LI* 22 [,C]	Read DMA address	Y	Y	X	
MI* 22 [,C]	Merge DMA address	Y	Y	X	
OT* 22 [,C]	Write DMA address	Y	Y	X	
[,C]	Clear FLG 22				
SFC 23	Skip if FLG 20, FLG 21, AND FLG 22 ALL Clear	Y	Y	X	6
SFS 23	Skip if FLG 20 OR FLG 21 OR FLG 22 Set (inclusive OR)	Y	Y	X	
CLF 23	Clear FLG 20, FLG 21, and FLG 22	Y	Y	X	
CLC 23 [,C]	Terminate DMA operation	Y	Y	X	
LI* 23 [,C]	Read DMA Count	Y	Y	X	
MI* 23 [,C]	Merge DMA Count	Y	Y	X	
OT* 23 [,C]	Write DMA Count	Y	Y	X	
[,C]	Clear FLG 20, FLG 21, and FLG 22				

Table 3-1. IOP Chip Instructions By Select Code (Continued)

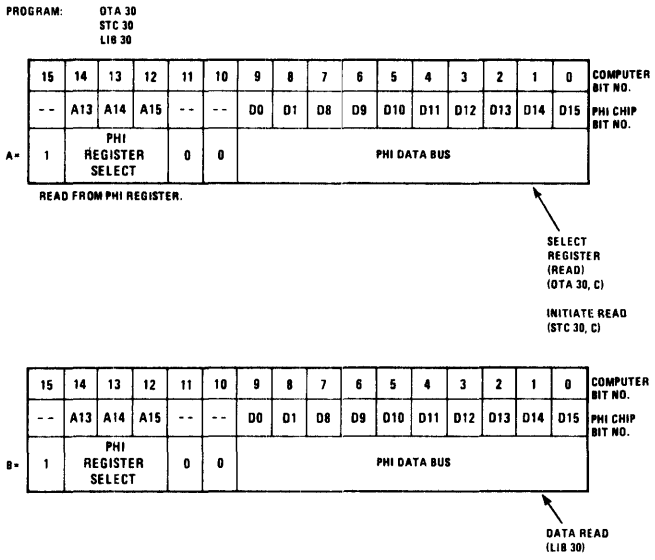
INSTRUCTION	FUNCTION	GR ON	GR =SC	IR =SC	NOTES
SFC 24	Skip if DMA disabled (DMAEN — asserted)	Y	Y	X	
SFS 24	Skip if DMA enabled (DMAEN — not asserted)	Y	Y	X	
LI* 24	Read Scratch 1	Y	Y	X	
MI* 24	Merge Scratch 1	Y	Y	X	
OT* 24	Write Scratch 1	Y	Y	X	
LI* 25	Read Scratch 2	Y	Y	X	
MI* 25	Merge Scratch 2	Y	Y	X	
OT* 25	Write Scratch 2				
LI* 26	Read Scratch 3	Y	Y	X	
MI* 26	Merge Scratch 3	Y	Y	X	
OT* 26	Write Scratch 3	Y	Y	X	
SFC 30	Skip if FLG 30 clear	Y	Y	X	7
SFS 30	Skip if FLG 30 set	Y	Y	X	
CLF 30	Clear FLG 30	Y	Y	X	
STF 30	Set FLG 30	Y	Y	X	
STC 30 [,C]	Set CNTRL 30 and issue DVCMD	Y	Y	X	
CLC 30 [,C]	Clear CNTRL 30	Y	Y	X	
LI* 30 [,C]	Read device data	Y	Y	X	
MI* 30 [,C]	Merge device data	Y	Y	X	
OT* 30 [,C]	Write device data	Y	Y	X	
[,C]	Clear FLG 30				
LI* 31	Read interface control word	Y	Y	X	
MI* 31	Merge interface control word	Y	Y	X	
OT* 31	Write interface control word	Y	Y	X	
LI* 32	Read interface status	Y	Y	X	8
MI* 32	Merge interface status	Y	Y	X	
OT* 32	Reset interface status	Y	Y	X	9
SFC SC	Skip if FLG 30 clear	N	X	Y	7
SFS SC	Skip if FLG 30 set	N	X	Y	
CLF SC	Clear FLG 30	N	X	Y	
STF SC	Set FLG 30	N	X	Y	
STC SC [,C]	Set CNTRL 30 and issue DVCMD	N	X	Y	8
CLC SC [,C]	Clear CNTRL 30	N	X	Y	
LI* SC [,C]	Read device data	N	X	Y	10
MI* SC [,C]	Merge device data	N	X	Y	10
OT* SC [,C]	Write device data	N	X	Y	
[,C]	Clear FLG 30				

SC = Interface select code

Notes:

1. The [,C] is always executed even if the primary instruction is not.
2. The SLAVE logic must be enabled; i.e., SLRQ LOW at power up.
3. FLG 20 is set by DMA upon completion of self configured DMA block transfer which is not to be followed by another self configuration.
4. FLG 21 is set by DMA upon completion of any block transfer which is not to be followed by a self configuration.
5. FLG 22 is set by DMA if a parity error occurs during a DMA read.
6. FLG 23 is the logical OR of flags 20 through 22.
7. FLG 30 and CNTRL 30 are controlled by the Flag and Control flip-flops located in the IOP chip.
8. The IOP chip indicates only that the select code is in the range 32 to 77, it is up to the user to decode any specific select code.
9. Serial I/O cards, by convention, use this instruction as a card reset.
10. When the IOP chip is in diagnose mode, these instructions fetch the following:

    Diagnose mode 1 — the interface's select code and ID word.
    Diagnose mode 2 — the global register and IOP chip status bits.



3-7. PROGRAMMED INPUT/OUTPUT

Address the card through the global register and proceed as follows:

OTA/B 30 sends commands and data over HP-IB and
STC 30,C programs PHI Chips registers

STC 30,C reads commands and data from HP-IB and
LIA/B 30 reads back PHI Chip register contents from a previously specified register

OTA/B 31 program card control register

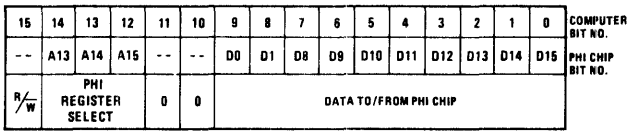
LIA/B 31 read back card control register

LIA/B 32 read card status register

OTA/B 32 clears Secondary Address Bit in status word

3-8. DATA REGISTER (OT*/LI* 30)

The data register holds data to be written into or read from the PHI Chip. This includes HP-IB data and commands. The data word includes the Read/Write bit, three PHI register select bits, and 10 bits of PHI register data. This word is shown as follows:



To Write a Word:

(1) OTA 30 write select bit (Bit 15=0), PHI register selected, 10 bits of data placed in write data holding register.

(2) STC 30 handshakes 10 bits of data from holding register into selected PHI register. A copy is also written into the read data register.

To Read a Word:

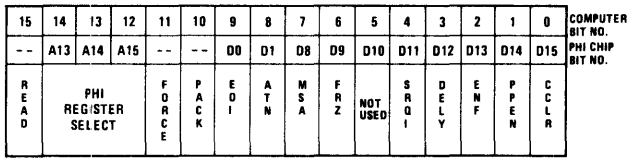
(1) OTA 30 read bit set, PHI register selected, lower bits have no meaning.

(2) STC 30 handshake 10 bits from the selected PHI register into the read data holding register.

(3) LIA 30 pick up 10 bits of data from card along with PHI register number and read bit.

3-9. CONTROL REGISTER (OT*/LI* 31)

The upper four bits duplicate the corresponding bits of the data register. This allows read/write and PHI register selection during byte mode DMA. If set, the bits have the following meaning:



BIT NO.	MEANING
15	1 = READ, 0 = WRITE
14, 13, 12	PHI register select.
11	Forced read on inbound FIFO flush.
10	Byte packing mode.
9	Send last HP-IB byte out tagged with EOI or terminate input DMA on End of Record (EOI or LF).
8	Set ATN on HP-IB bytes sent out, or terminate input DMA if My Secondary Address is received.
7	Enable interrupt on My Secondary Address detection.
6	Freeze DMA on interrupt.
5	NOT USED
4	Enable SRQ interrupt (independent detection outside of PHI Chip).

3	Delay start of DMA data transfer until interrupt condition exists (before masking by bit 2).
2	Enable card flag to be set (no effect on DMA completion interrupt).
1	Do Parallel Poll at end of current DMA operation (output only).
0	Clear card (except PHI).

3-10. STATUS REGISTER (LI*/OT* 32)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
--	A13	A14	A15	--	--	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
PPEN	GET	EOI	MSA	FINT	FRZ	SRQ	DMARQ	U16 S1	U16 S2	U16 S3	U16 S4	U16 S5	U16 S6	U16 S7	U16 S8	

BIT NO.	MEANING
15	Parallel Poll in effect for at least 7 microseconds.
14	Group Execute Trigger (GET) received.
13	End of Record (EOI or Line Feed) received.
12	My Secondary Address (MSA) received.
11	PHI interrupt request.
10	DMA operation frozen.
9	HP-IB service request (SRQ).
8	PHI requesting transfer (DMARQ).
7-0	Reflects the setting of HP-IB Address Select Switches, U16S1 thru U16S8.

When an OT* 32 is executed, the MSA bit (bit 12) is cleared but all other bits remain unchanged.

3-11. DIRECT MEMORY ACCESS (DMA) FUNCTION

In addition to data transfers, DMA allows complete control of the interface card and the HP-IB. DMA operation offers the following advantages:

a. Two control words can be sent: a DMA control word and a card control word.

b. Transmission log (i.e. actual number of bytes/words transferred) can be automatically returned to the user at the completion of a DMA operation.

c. The card control word specifies initial conditions and alternate terminating conditions besides the exhausted count.

d. Multiple DMA operations can be stacked and executed in sequence without further software intervention.

e. The DMA completion interrupt occurs only at the end of a series of stacked DMA operations.

f. The card can terminate the sequential execution of stacked operations upon error detection.

g. If so specified in the card control word of the DMA quadruplet, the card is allowed to conduct a Parallel Poll at the completion of the current DMA operation, before allowing the DMA program to proceed. If a selected interrupt occurs, DMA operation can be frozen by the card.

Any given card has a maximum DMA rate at which it is capable of running. In order to achieve this maximum rate however, there can be no other requests on the backplane. Typically, there are other transactions on the backplane which degrade the maximum possible DMA rate. When the processor decides to fetch an instruction at the same time as an interface card is preparing for DMA, that DMA cycle can be held off for 908 ns. If an interface card is in the highest priority slot, it can be held off by the processor, or, in addition by a lower priority card doing DMA for a worst case of 454 ns per transfer. All DMA rate specifications given in Table 1-1 assume the card in question is plugged into the highest priority slot. When plugged into a lower priority slot, DMA rates can not be guaranteed when the additive rates of the higher priority cards are capable of consuming the total backplane bandwidth (2.72 Mbytes). Typically, however, even in a busy system, the backplane is only fully congested for very short periods of time, so that even the lowest priority I/O cards transfer at rates very close to their nominal specifications.

3-12. DMA CONTROL AND STATUS WORDS

Software DMA set-up and control involves seven different control and status words, each of which is associated with a different register. Four of these registers (20 through 23) are located in the I/O Processor Chip and the other three (30, 31,and 32) are on the circuit board. The seven register's numbers and functions are as follows:

DMA Register Number 20, DMA Self-Configuration Register, In or Out

DMA Register Number 21, DMA Control Register, In or Out

DMA Register Number 22, DMA Address Register, In or Out

DMA Register Number 23, Word/Byte Count Register, In or Out

DMA Register Number 30, Data Register, In or Out

DMA Register Number 31, Card Control Word Register, In or Out

DMA Register Number 32, Card Status Word Register, In

3-13. DMA SELF-CONFIGURATION, REGISTER 20

The DMA self-configuration register contains the address of the DMA triplets or quadruplets. A DMA triplet (see Figure 3-3) is of the form: control bits, transfer address,

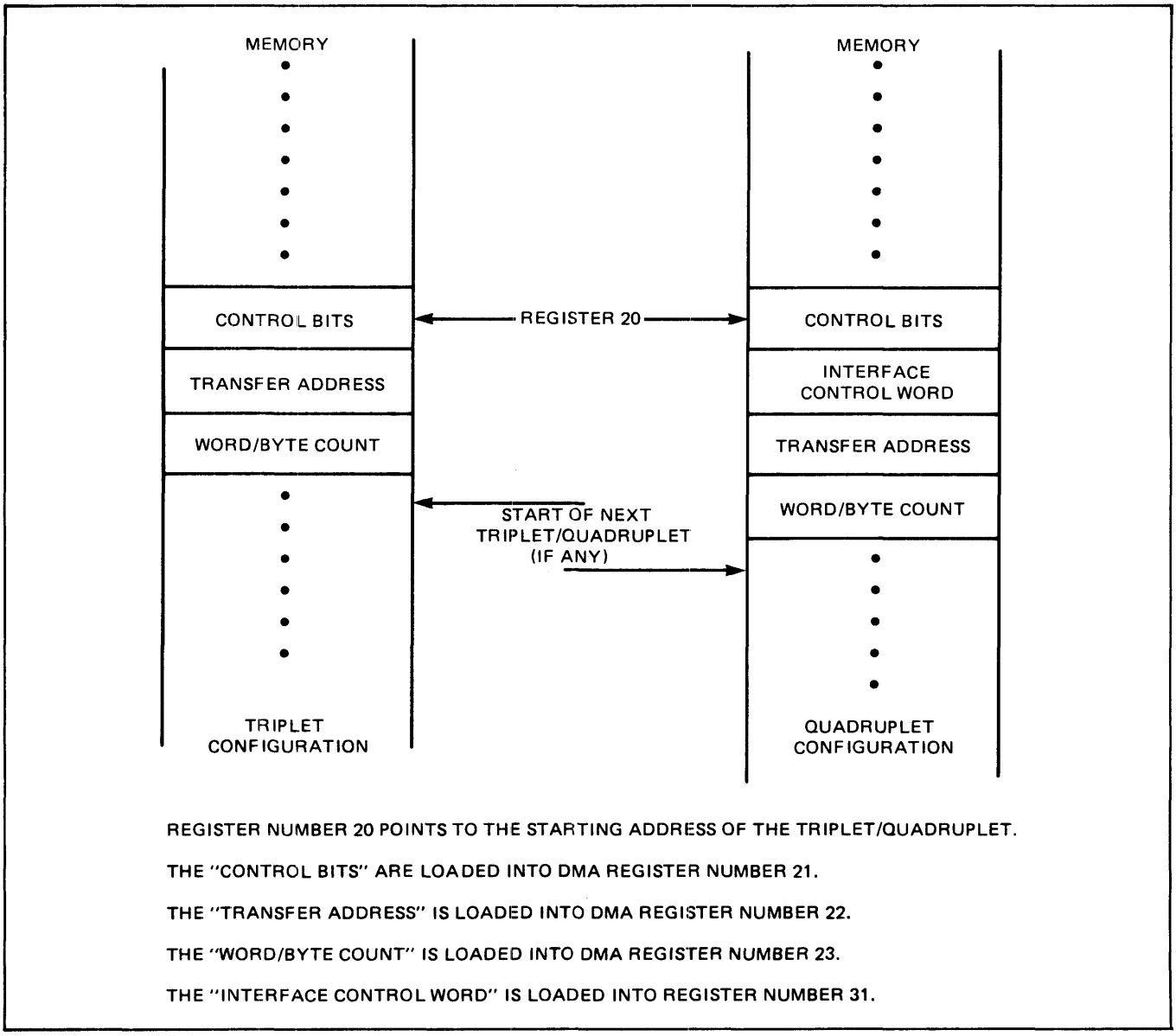
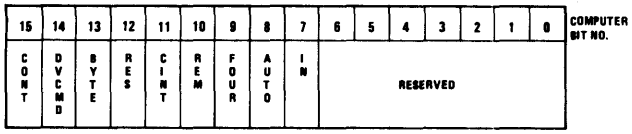


Figure 3-3. DMA Self-Configuration Formats

and word/byte count. The triplet words are the words to be used in registers 21,22, and 23, respectively. A DMA quadruplet (see Figure 3-3) is of the form: control bits, card control word, transfer address, and word/byte count. These quadruplet words are to be put into registers 21, 31, 22, and 23, respectively.

3-14. DMA CONTROL WORD 1, Register 21

The bit definitions for the DMA control word 1 are as follows:



Bits 0-6: Reserved

Bit 7: IN
- 1= Indicates that the direction of the data transfer is from the HP-IB Card to memory.
- 0= Indicates that the direction of the data transfer is from memory to the HP-IB Card.

Bit 8: AUTO — AUTO has different meanings depending on whether bit 7 (IN) is set.
- 1= Last input transfer will be followed by a DVCMD pulse.
- 0= The last DVCMD pulse will be suppressed.

Bit 9: FOUR
- 1= Indicates that there are four words to be fetched for the current DMA configuration. Loads Register 31 as part of the DMA quadruplet.
- 0= Indicates that there are three DMA control words to be fetched for the current DMA configuration. Register 31 must be loaded separately prior to triplet.

Bit 10: REM — Remote Memory
- 1= All memory requests will be accomplished by the REMEM (Remote Memory) signal, that disables standard memory and enables remote memory.
- 0= Remote memory not enabled.

Bit 11: CINT — Completion Interrupts
- 1= Inhibits DMA transfer completion interrupts.
- 0= Completion interrupt is to be requested by DMA logic when word/byte count rolls over (goes from −1 to 0).

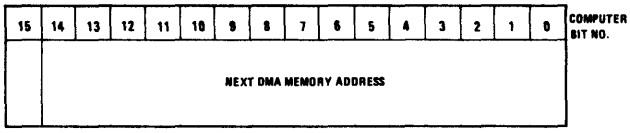
Bit 12: RES — Residue
- 1= If set, and if DMA is enabled to self-configure, i.e., a STC 20 has been executed, DMA will write its word/byte count residue into the location from which it read the word/byte count.
- 0= Word/byte count is not written.

Bit 13: BYTE
- 1= Indicates that the DMA transfer is to be conducted in byte mode, i.e., each data transfer is counted as one byte. Byte mode transfers are packed, two bytes per word, with the left byte (bits 15-9 of the data word) being transferred first.
- 0= Each data transfer will be a full 16-bit word.

Bit 14: DVCMD — Device Command
- 1= DMA control logic will issue a Device Command (DVCMD) signal immediately following each data transfer from the interface logic.
- 0= Device Command is not issued.

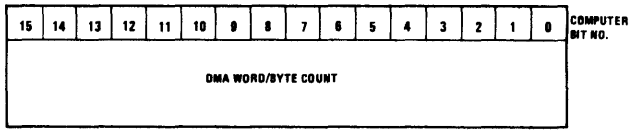
Bit 15: CONT — Control
- 1= If set and an STC 20 has been executed, then at the end of a DMA transfer the I/O Processor Chip will fetch the next set of DMA control words and reconfigure itself to start a new transfer.
- 0= DMA will stop at the end of the current transfer.

3-15. DMA ADDRESS, REGISTER 22



DMA control word 2 is the 15-bit (bits 0-14) address of the next memory location to be accessed by DMA. The most significant bit (bit 15) cannot be controlled by OTA 22 or OTB 22 and will be the complement of control word 1, bit 7 (IN) when fetched by an LIA 22.

3-16. DMA WORD/BYTE COUNT, REGISTER 23



The word/byte count register, register 23, is a 16-bit register whose value is the two's complement of the number of data elements to transfer. A data element may be either a word or a byte, as indicated by bit 13 (BYTE) of the DMA control word, contained in register number 21.

The end of a data transfer is indicated by the transition of the word/byte count register's value from −1 to 0. Rollover from 177777 octal to 000000 occurs at this same time. This allows up to 65,536 data elements to be transferred at any one time. The memory size (32,768 words maximum) limits a word transfer to a length of 32,768 words or 65,536 bytes. The hardware does not detect this, however, so it is up to the programmer not to exceed this limit.

3-17. DMA TRANSFER OPERATION

A DMA transfer is started by configuring the DMA control register, DMA address register, word/byte count register, and the output control word register, and then issuing a STC instruction to register 21 (DMA Control Register).

3-18. DMA INPUT TRANSFER

A DMA input transfer is defined as being from the HP-IB card to memory. If the transfer is in word mode, a Device Command (DVCMD) signal and a memory access signal are generated immediately. If the transfer is in byte mode, the DMA control logic responds to the HP-IB card with only a DVCMD signal. When the second byte transfer is requested, the memory write request is generated. The memory request goes directly to the backplane where memory access priority is determined by the location of the requesting card in respect to the processor card (the closer the card is to the processor, the higher the card's priority). When the memory access request is granted, the data is transferred, the DMA word/byte count, and DMA address registers are incremented, and the DMA control logic is ready to accept another data transfer request.

3-19. DMA OUTPUT TRANSFER

A DMA output transfer is defined as being from memory to the HP-IB card. For an output transfer, a memory access request is generated immediately. As soon as the data is available from memory, it is passed to the HP-IB card. The data is followed by a Device Command (DVCMD) signal. In byte mode, the byte indicator signal is changed and another DVCMD signal is generated when the PHI Chip indicates that it is ready to accept more data.

3-20. DMA TRANSFER TERMINATION

A DMA data transfer continues as described in paragraphs 3-18 and 3-19 until a terminating condition is detected. The terminating conditions are as follows:

a. Word count transition from −1 to 0. (Rollover from 177777 octal to 000000 occurs.) This indicates that all the data elements that were to be transferred have been transferred.

b. Detection of a Control Reset (CRS) signal. This signal is generated by the procesor card during its power-up sequencing, or by execution of a CLC 0 instruction.

c. Parity error indication from memory.

d. Assertion of LSBYT.

3-21. DMA SELF-CONFIGURATION FEATURE

Available in the I/O Processor Chip is circuitry that enables the DMA registers (discussed in the preceding paragraphs) to be loaded directly from sequential memory locations. Upon completion of each successive DMA operation, the contents of register 20 are used as a pointer to the location in memory containing the next set of values to be loaded into registers 21, 22, and 23. As each register is loaded,the contents of register 20 are incremented, leaving register 20 pointing to the values to be used for the next transfer.

3-22. DMA SELF-CONFIGURATION INITIALIZATION

The DMA self-configuration feature is initialized by setting the value of register 20 to the memory address of the first word of a list of DMA triplets or quadruplets. A triplet is of the form: control bits, transfer address, and word/byte count. The triplet words are the words to be used in registers 21, 22, and 23, respectively. A quadruplet is of the form: control bits, card control, transfer address, and word/byte count. The quadruplet words are to be loaded into registers 21, 31, 22, and 23, respectively. Bit 8 of the control word is used with both the triplet and quadruplet. Figure 3-3 illustrates the formats of both the triplets and quadruplets.

Once the DMA self-configuration feature is initialized by setting the value of register 20 equal to the memory address of the first word of a list of DMA triplets or quadruplets, an STC to register 20 starts the feature. This STC instruction to register 20 has the effect of simultaneously setting the control on registers 20 and 21 to achieve an initial state for full execution.

3-23. DMA SELF-CONFIGURATION OPERATION

After receiving the STC instruction from register 20, the self-configuration control logic fetches the word addressed by the contents of register 20 and loads this word into register 21. Assume bit 7 of this word is set, signifying a

quadruplet. The contents of register 20 are incremented during the memory access. The new value of register 20 is used as the address of the next memory read. This next word is loaded into the control register on the HP-IB card by means of a virtual OTA 31 generated by the I/O Processor Chip. Then register 20 is incremented for the next read and this new data is loaded into register 22. Register 20 is again incremented. The new value of register 20 is used to address the fourth word of the current quadruplet. This fourth word is loaded into register 23. The value of register 20 is again incremented, pointing to the beginning of the next triplet/quadruplet. The DMA operation just loaded is then started as soon as the interface is ready (see paragraph 3-18 or 3-19). When the DMA operation terminates (see paragraph 3-20),if bit 11 of register 21 is clear, an interrupt request is generated. If the DMA operation terminates due to either an end-of-transfer indication from the interface or a word/byte count transition from −1 to 0, and bit 12 of register 21 is set, the DMA self-configuration logic writes the word-count residue into the location formerly occupied by the current DMA operation's word/byte count. Operation of the self-configuration feature is continued, as previoulsy noted, for the next triplet/quadruplet.

3-24. DMA SELF-CONFIGURATION TERMINATION

The operation of the DMA self-configuration feature continues as described in paragraph 3-23 until one of the following events occurs:

a. A CLC instruction to register 20 is executed. This serves to inhibit the self-configuration logic from advancing its pointer to the next triplet, while still allowing the current DMA to continue. An STC instruction to register 20 allows the self-configuration feature to continue.

b. A CLC instruction to register 21 is executed. This stops the current DMA operation at its present state of operation.

c. A CLC instruction to register 22 is executed. This aborts the current DMA operation and causes the self-configuration logic to advance to the next triplet/quadruplet. No interrupt is generated by the aborted transfer.

d. A CLC instruction to register 23 is executed. This stops the operation of the self-configuration logic and aborts the transfer in progress.

e. The first word of a triplet is read with CONT bit 15 (DMA Control Word 1) clear, indicating that there are no more DMA triplets. This sets the flag on register 20, which generates an interrupt request if the control flip-flop of register 20 is set.

3-25. TYPES OF DMA TRANSFERS

WRITES

a. word mode: allows programming of PHI Chip directly and sending over the HP-IB.

b. byte mode: allows sending bytes over the HP-IB in the data or command mode as specified by the card control word. EOI can be automatically appended to the last byte.

READS

a. word mode: immediate or delayed read of the PHI register specified in the DMA control word. A delayed read is initiated only when a PHI interrupt is detected by the card.

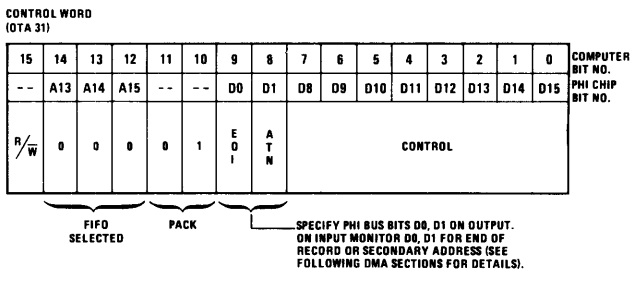
The lower 10 bits of the computer word correspond to the PHI bus. The corresponding PHI register address along with the READ/WRITE bit are in the most significant bits of the computer word.

b. byte mode: reads data from the HP-IB. The two high order bits of the PHI bus are monitored for data termination conditions (EOI or Line Feed) or ATN. The card control word specifies the termination conditions.

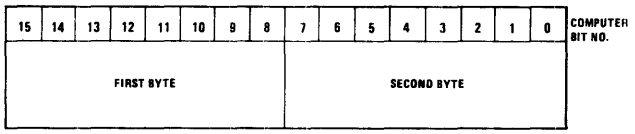
The lower eight bits of the PHI bus are packed 2 bytes/computer word. First byte is the high order byte.

3-26. BYTE MODE DMA INPUT

When sending or receiving data or commands over the HP-IB, it is desirable to pack two 8-bit bytes per computer word. As the PHI bus and FIFO's are 10 bits wide, provision must be made to specify the two higher bits not included in the 8-bit byte on output and to monitor these two bits on input. The handling of these two extra bits is specified in the PHI control byte of the card control word.



REGISTER 38
PACKED DATA WORD



a. [EOI,ATN] = 00

PHI bits D8 to D15 are written into memory without monitoring D0, D1. End of Record (D0, D1 = 11) and My Secondary Address (D0, D1 = 01) will not be detected.

b. [EOI,ATN] = 10

Upon detecting an End of Record (D0, D1 = 11), the DMA input operation is terminated.

c. [EOI,ATN] = 01

Upon detecting a Secondary Address, the input DMA operation is terminated.

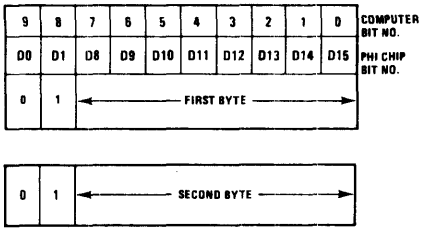
d. [EOI,ATN] = 11

Terminates input DMA operation on last byte or Secondary Address.

3-27. BYTE MODE DMA OUTPUT

Depending on the value of the two least significant bits (Bit 9 EOI or Bit 8 ATN) of the first control byte, the unpacked data words are output on the PHI bus as follows:

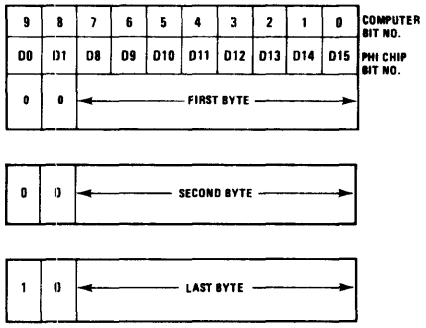
a. [EOI,ATN] = 01



NOTE

If addressing the outbound FIFO, the bytes packed in memory are sent as command bytes (ATN = true) over the HP-IB.

b. [EOI,ATN] = 10



NOTE

The last data byte will be tagged with EOI.

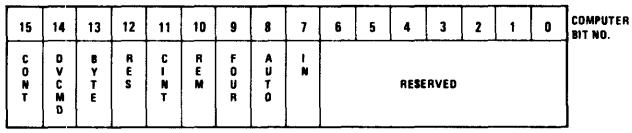
c. [EOI,ATN] = 00

PHI bits 0 and 1 will be output as zero. Last byte will not be tagged with EOI. The bytes will be output as HP-IB data.

d. [EOI,ATN] = 11

As shown in part a, PHI bit 1 will be set and as shown in part b, bit 0 will be set on the last byte. Note that in this case, bytes would go out as commands over the HP-IB, and the last one would be interpreted as a byte count by the PHI Chip (see 3-43, PHI Register 0: Outbound FIFO, Byte Transfer Enable).

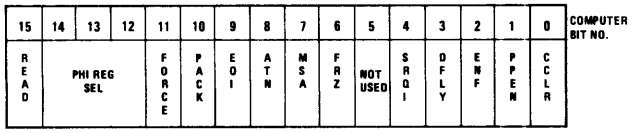
3-28. DMA CONTROL WORD 1 (LI* 21 or OT* 21)



The Device Command (bit 14) must ALWAYS BE SET (DVCMD=1). The DMA will then automatically issue Device Commands equivalent to the STC ,C instruction of programmed I/O.

The AUTO (bit 8) must ALWAYS BE CLEAR (AUTO=0). The card will request the first data output transfer when ready.

3-29. CARD CONTROL WORD AND DMA



The Card Control Word also affects DMA operation.

Byte mode:

If byte packing is used (BYTE: bit 13 = 1 in DMA CONTROL WORD 1), the card control word must have the PACK bit set (bit 10 = 1).

Start delay:

If the Delayed Start bit 3 of the card control word is set, the first data exchange of a DMA operation is delayed until an unmasked "interrupt" condition occurs on the card such as:

a. INT from PHI Chip (positive P.P. response, SRQ, status change, Outbound FIFO empty, etc.)

b. Group Execute Trigger.

c. SRQ detected on the HP-IB Bus.

NOTE

Bit 2, which enables setting the card's flag, need not be set.

EOI (bit 9 of card control word):

If set and a byte tagged with EOI or a Line Feed character (if its detection was enabled in PHI) is read into memory, the DMA input operation is terminated irrespective of byte/word count. On output, this bit simply specifies that the last byte sent should be tagged with EOI.

ATN (bit 8 of card control word):

If set and a Secondary Address is read into memory, the input DMA operation is terminated irrespective of the byte/word count. On output, the bytes are sent out as commands (ATN set).

Freeze DMA on Interrupt (bit 6):

If set and an unmasked PHI Chip interrupt, SRQ, Secondary Address or a Group Execute Trigger is received, DMA operation will freeze (cease without terminating). Interrupts should be enabled to flag the user. The Freeze condition is reflected in the card status word (LIA 32).

Forced Read (bit 11):

Allows an 8 byte DMA read to flush the Inbound FIFO even if fewer bytes are present. It can be used after data inputs uncounted by the PHI which might have left an unknown number (0-8) of unwanted bytes in the Inbound FIFO.

Do Parallel Poll (bit 1):

If set, a Parallel Poll is allowed to take place for about 7.5 microseconds prior to terminating an output DMA operation. This opens windows during self-configured multiple DMA operations to allow PP response detection. Be careful not to use this bit if an uncounted request will be left in the Outbound FIFO preventing the execution of PP.

3-30. PHI FIFO DMA PROGRAMMING

To properly manage the DMA transfers into the PHI's Inbound or Outbound FIFO's, the PHI's Control Register (Register 6) FIFO select bit must be programmed as follows:

i.e.	0	6	0	0	0	2	(OCTAL) PRIOR TO OUTPUT.
	0	6	0	0	0	0	(OCTAL) PRIOR TO INPUT.

For performing other functions, other bits may have to be programmed.

For a DMA programming example, see Table 3-3.

3-31. HP-IB INTERFACE CARD PROGRAMMING CHARACTERISTICS

3-32. INITIALIZATION (POWER ON AND I/O CLEAR)

On initial power-up, or in response to CRS/CLC 0, the interface card goes OFFLINE from the HP-IB, i.e., it does not interact at all with the HP-IB network. The other results of power up or I/O Clear are as follows:

a. The card is not a Controller, Talker, or Listener

b. DMA: idle

c. Card Control Word: all zeros

d. PHI Interrupt Mask: all zeros (no interrupts)
Parallel Poll Mask: all zeros (no response)
Parallel Poll Sense: all zeros
FIFO Buffer Contents: undefined

3-33. SYSTEM CONTROLLER AND CONTROLLER-IN-CHARGE

NOTE

By definition, an operating system is the executive of a computer, supervising and controlling all internal and external processes; and the I/O is one of these processes. Therefore, when interfacing with the HP-IB, RTE assumes the role of being the controller of the interface bus in order to properly coordinate with several possible on-going I/O functions on other interfaces. In this respect, RTE prohibits the use of "pass control" on its HP-IB interface.

The System Controller switch (U1S1) on the card must be set prior to power up if the card is to be programmed as a System Controller of the HP-IB. If the switch is set later, then CRS/CLC 0 or PON must be sent to the card, or the PHI chip must be programmed OFFLINE, then ONLINE again (Register 7). Register 1 bit 11 can be read to verify that the PHI Chip is acting as System Controller.

If the System Controller switch (U1S1) is set, to become Controller-in-Charge, the software must first program the PHI Chip ONLINE by setting bit 8 in Register 7. The IFC (Interface Clear) message must then be sent over the HP-IB for at least 100 microseconds to clear the bus and make the card the Controller-in-Charge. This is accomplished by setting bit 11 of Register 6. (Refer to the programming example, Table 3-2.)

3-34. BUS CONTROLLER DEVICE

Prior to placing the card ONLINE, the HP-IB address should be written into Register 7. The address may be found in the lower eight bits of the Status Register. The card may then be placed ONLINE. The default address is 36.

The software should enable the card interrupts to be alerted if:

a. A Device Clear or Group Execute Trigger Command is received.

b. The PHI status changes (Take Control Message is received).

c. A byte is received in the Inbound FIFO.

3-35. INTERRUPTS

Interrupts vector to the memory location corresponding to the select code programmed by the Select Code switches, U1S3 through U1S8, for the card. The interrupt requests may be generated from the following four areas:

a. I/O Chip DMA completion.

b. Reception of a Group Execute Trigger from the HP-IB.

c. An HP-IB SRQ (Service Request) detected independently of the PHI.

d. One of nine maskable PHI Chip status conditions:

   1. An affirmative response to a Parallel Poll exists.

   2. An HP-IB device is requesting service through an SRQ.

   3. A DEVICE CLEAR interface message has been received from the HP-IB controller.

   4. The REMOTE/LOCAL or CONTROLLER-IN-CHARGE status of the PHI Chip has been changed by the System Controller.

   5. A parity error was detected in an HP-IB command received over the bus.

   6. The Outbound FIFO is not full.

   7. The Inbound FIFO is not empty.

   8. Both FIFOs are idle and Outbound FIFO is empty.

   9. An attempt to write into a full FIFO or to read from an empty FIFO.

3-36. CARD FLAG INTERRUPTS

If bit 2 of the Card Control Word is set, the card's flag will be set if:

a. A Group Execute Trigger is received when the card is not the controller-in-charge.

b. SRQI (bit 4) of the Card Control Word is set and an SRQ exists on the bus.

c. MSA (bit 7) of the Card Control Word is set or a secondary address is read into the computer.

d. A PHI interrupt occurs. (These are maskable within the PHI Chip.)

The HP-IB card's flag may be tested by SFS/SFC select code/30. If the Interrupt System and Mask are on and the card's control is (STC s.c./30), setting the flag generates an interrupt.

If the flag is set, software can ascertain the cause by reading the Status Register (LIA32), and if necessary the PHI's interrupt register (Register 2).

3-37. PROGRAMMING EXAMPLES

3-38. NON-DMA TRANSFER EXAMPLE (TABLE 3-2)

The following programming example initializes the card, asserts Remote Enable, and leaves the PHI Chip in the Parallel Poll state. This is performed by means of a non-DMA I/O transfer.

3-39. DMA TRANSFER EXAMPLE (TABLE 3-3)

The following programming example gives the self-configuring DMA quadruplets and buffers required to perform a Status and DSJ read from the 7902 disc. This sequence must be performed after turning on thhe 7902 or inserting the cartridge.

3-40. WORD FORMAT SUMMARY

Figure 3-4 contains a reference guide to all control and data word formats for the HP-IB card.

3-41. PHI CHIP REGISTER DEFINITIONS

The eight addressable registers within the PHI Chip perform the following functions:

REGISTER 0: FIFO's — Two First-In-First-Out queues used for transferring bytes over the HP-IB. One FIFO is for inbound data transfer and the other is for outbound data transfer.

REGISTER 1: STATUS — A register that contains the values of non-interrupting internal PHI Chip status conditions.

Table 3-2. Non-DMA Transfer Example

```
 PAGE 0009 #01                          6:32 PM  FRI., 19  JAN., 1979
    INITIALIZATION OF CARD AS A CONTROLLER


0150  02000                ORG 2000B
0151*SET-UP HP-IB
0152  02000 062026  START  LDA SC
0153  02001 103602         OTA 2,C      SET UP GLOBAL REGISTER FOR HP-IB CARD
0154  02002 107723         CLC DMACT,C   RESET DMA MACHINE
0155  02003 062027         LDA ONL       PLACE CARD ON-LINE
0156  02004 102630         OTA DREG
0157  02005 103730         STC DREG,C
0158  02006 062030         LDA AIFC      ASSERT
0159  02007 102630         OTA DREG        IFC
0160  02010 103730         STC DREG,C
0161  02011 060103         LDA M100            FOR
0162  02012 002006         INA,SZA               >100
0163  02013 026012         JMP *-1                   MICROSEC.
0164  02014 062031         LDA SETUP  REMOVE IFC,ASSERT REN
0165  02015 102630         OTA DREG
0166  02016 103730         STC DREG,C
0167  02017 062032         LDA SETUP+1   PROGRAM PARRALEL POLL MASK FOR LINE D101
0168  02020 102630         OTA DREG
0169  02021 103730         STC DREG,C
0170  02022 062033         LDA SETUP+2   PROGRAM INTERRUPT MASK FOR PP & SRQ
0171  02023 102630         OTA DREG
0172  02024 103730         STC DREG,C
0173  02025 026052         JMP STOP




0175  02026 000037  SC     ABS SCODE
0176  02027 070200  ONL    ABS WRITE+ADRS+ONLIN
0177  02030 060021  AIFC   ABS WRITE+CNTRL+IFC
0178  02031 060040  SETUP  ABS WRITE+CNTRL+REN
0179  02032 040001         ABS WRITE+PPMSK+PPR0
0180  02033 031060         ABS WRITE+IMSK+INTON+PPR+SRQ
```

Table 3-3. DMA Transfer Example

```
 PAGE 0017 #01                          6:32 PM  FRI., 19  JAN., 1979
    DSJ & STATUS


0441  02500                ORG 2500B
0442*DSJ & STATUS REQUEST
0443*DMA PROGRAM : 4 QUADRUPLETS
0444  02500 002501  DSJP DEF *+1
0445  02501 141000        ABS CONT+CONT+DVCMD+WORD+FOUR+OUT
0446  02502 000000        ABS WRITE
0447  02503 002540        DEF DSJ
0448  02504 177770        ABS DSJ-RDDSJ
0449*
0450  02505 161200        ABS CONT+CONT+DVCMD+BYTE+FOUR+IN
0451  02506 102000        ABS READ+READ+PACK
0452  02507 002550        DEF RDDSJ
0453  02510 177777        DEC -1
0454*
0455  02511 141000        ABS CONT+CONT+DVCMD+WORD+FOUR+OUT
0456  02512 000000        ABS WRITE
0457  02513 002551        DEF STATS
0458  02514 177762        ABS STATS-RDSTS
0459*
0460  02515 061200        ABS DVCMD+BYTE+FOUR+IN
0461  02516 102000        ABS READ+READ+PACK
0462  02517 002567        DEF RDSTS
0463  02520 177774        DEC -4
0464*



0466  02540                ORG 2540B
0467*DSJ & STATUS REQUEST
0468*HP-IB & CARD PROGRAM
0469  02540 060042  DSJ    ABS WRITE+CNTRL+DMAOT
0470  02541 000476        ABS WRITE+FIFO+MLA
0471  02542 000507        ABS TLKA+FLPYA
0472  02543 000560        ABS MSA+20B
0473  02544 001001        ABS RCVRQ+1
0474  02545 000537        ABS UNT
0475  02546 000477        ABS UNL
0476  02547 060040        ABS WRITE+CNTRL+DMAIN
0477  02550 000000  RDDSJ NOP                      RETURNED DSJ IN UPPER BYTE
0478  02551 060042  STATS ABS WRITE+CNTRL+DMAOT
0479  02552 000536        ABS WRITE+FIFO+MTA
0480  02553 000447        ABS LSTNA+FLPYA
0481  02554 000550        ABS MSA+10B
0482  02555 000003        ABS STATD
0483  02556 001000        ABS UNIT0+EOI
0484  02557 000477        ABS UNL
0485  02560 000476        ABS MLA
0486  02561 000507        ABS TLKA+FLPYA
0487  02562 000550        ABS MSA+10B
0488  02563 001004        ABS RCVRQ+4
0489  02564 000537        ABS UNT
0490  02565 000477        ABS UNL
0491  02566 060040        ABS WRITE+CNTRL+DMAIN
0492  02567 000000  RDSTS NOP
0493  02570 000000        NOP       4 STATUS BYTES RETURNED
```

REGISTER 2: INTERRUPTING CONDITIONS — A register that contains the values of nine interrupting status conditions plus a tenth bit which is the "OR" of the others. When this tenth bit is a "1", the host processor is interrupted by the PHI Chip.

REGISTER 3: INTERRUPT MASK — A register whose bits are used to mask off (force to "0") corresponding bits of Register 2.

REGISTER 4: PARALLEL POLL MASK/ FIRST ID BYTE — Within an HP-IB Controller, the bits of this register mask corresponding DIO line responses to a Parallel Poll. Within a non-controller, they are used as the first byte of a two-byte sequence which optionally can be used to identify the type of device that contains the PHI Chip.

REGISTER 5: PARALLEL POLL SENSE/SECOND ID BYTE — Within an HP-IB Controller,

DATA REGISTER 30

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
--	A13	A14	A15	--	--	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
R/W	PHI REGISTER SELECT			0	0	PHI DATA BUS										

1 = READ FROM PHI CHIP
0 = WRITE TO PHI CHIP

CONTROL REGISTER
REGISTER 31 (OT*/LI*31)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
--	A13	A14	A15	--	--	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
READ	PHI REGISTER SELECT			FORCE	PACK	EOI	ATN	MSA	FRZ	NOT USED	SRQI	DELY	ENF	PPEN	CCLR	

STATUS REGISTER
REGISTER 32 (LIA 32)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
--	A13	A14	A15	--	--	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
PPEN	GET	EOI	MSA	FINT	FRZ	SRQ	DMARQ	U16 S1	U16 S2	U16 S3	U16 S4	U16 S5	U16 S6	U16 S7	U16 S8	

DMA CONTROL WORD 1
REGISTER 21

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
CONT	D* VCMD	B* YTE	RES	CINT	REM	FOUR	A* UTO	IN	RESERVED							

*BIT 14 MUST BE A 1 AND BITS 8 AND 13 MUST BE 0.

DMA ADDRESS
REGISTER 22

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
	NEXT DMA MEMORY ADDRESS															

DMA WORD/BYTE COUNT
REGISTER 23

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
DMA WORD/BYTE COUNT																

Figure 3-4. Word Format Reference Summary

the bits of this register inform the PHI Chip which assertion level is being used on each DIO line to indicate a need for service during a Parallel Poll. Within a non-controller, they are used as the second byte of a two-byte sequence which optionally can be used to identify the type of device that contains the PHI Chip.

REGISTER 6: CONTROL — A register that contains control bits accessable to the host processor that allow it to determine internal PHI Chip states.

REGISTER 7: ADDRESS — A register through which the host processor can inform the PHI Chip which HP-IB address to use while communicating over the HP-IB, as well as a few other essentials.

The basic structure of the PHI Chip is shown in Figure 3-2. More detailed information about these eight registers is contained in the following pages.

3-42. REGISTER 0: OUTBOUND FIFO/ INBOUND FIFO

3-43. OUTBOUND FIFO

Each write into Register 0 causes a word to be placed into an eight-word-long Outbound FIFO queue. This FIFO holds data bytes waiting to be sent over the HP-IB to other devices. Within HP-IB Controllers, it is also used to hold Interface Commands as well as control words which regulate the sending of data bytes by other devices on the HP-IB.

If the Outbound FIFO is full during any attempt to write into it, the handshake with the host processor will be completed without destroying any data already in the FIFO, and the PROCESSOR HANDSHAKE ABORT bit (bit 9) in Register 2 will be set. An aborted attempt to write into the Outbound FIFO can be repeated if desired until the word is finally accepted by the PHI Chip.

As each word reaches the HP-IB end of the Outbound FIFO, it is interpreted by the PHI Chip to allow one or more bytes to be transferred over the HP-IB. It is automatically removed from the FIFO at the completion of this transfer allowing the next word sequence to be interpreted.

If a non-controlling device containing a PHI Chip is addressed to Talk and is expected to send data bytes but its Outbound FIFO is empty, the HP-IB will remain idle until the host processor places a data byte into the FIFO. If either the DATA FREEZE bit in Register 1 or the DEVICE CLEAR bit in Register 2 is set, the PHI Chip will refuse to send data bytes, even if they exist in the Outbound FIFO, until the host processor resets that bit.

Within an HP-IB Controller, the DATA FREEZE and DEVICE CLEAR bits cannot be set. However, if either bit happens to already be set within a device at the time it becomes the HP-IB Controller, the PHI Chip will not allow any byte transfer over the HP-IB until the host processor resets that bit.

When the Outbound FIFO within the HP-IB Controller is empty, the PHI Chip automatically conducts a continuous Parallel Poll on the HP-IB. This poll terminates as soon as the next word is placed into the Outbound FIFO by the host processor. The PARALLEL POLL RESPONSE interrupt (bit 10) in Register 2 alerts the host processor that at least one device is indicating a need for service during this poll. See the definition for Register 2 bit 10 for more details.

The PHI Chip provides two interrupts for the host processor to help it coordinate Outbound FIFO activity. One indicates when the FIFO has room for more words to be written into it. The other interrupt indicates when the FIFO is completely empty.

The Outbound FIFO is initialized to an empty state when the PON input pin is set to a low value and whenever a "1" is written into the INITIALIZE OUTBOUND FIFO bit (bit 15) in Register 6.

If, within an HP-IB Controller, the INITIALIZE OUTBOUND FIFO bit is used at a time when the ATN line is false on the HP-IB, it will force the ATN line to be asserted asynchronously, possibly while a data byte is being sent, causing one or more devices to see a "phantom" Interface Command. Since this situation requires that the HP-IB Controller bring all HP-IB devices to a known state by sending a long string of Interface Commands, it should be avoided whenever possible. At all other times when ATN is asserted by the PHI Chip, its assertion is synchronized with the preceeding data transfer, effectively eliminating the chance of "phantom" Interface Commands.

Within a non-controlling device, all words written into the Outbound FIFO contain a single data byte to be sent over the HP-IB. Within an HP-IB Controller, however, a word written into the Outbound FIFO can be one of three types:

a. A DATA BYTE to be sent over the HP-IB.

b. An INTERFACE COMMAND to be send over the HP-IB.

c. A BYTE TRANSFER ENABLE to allow another device to send bytes over the HP-IB.

DATA BYTE:

10	9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D2	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
END	0	DATA BYTE VALUE									

When a DATA BYTE code reaches the HP-IB end of the Outbound FIFO, it is sent over the HP-IB along with its associated END bit value to all currently addressed listeners.

Within a non-controlling device, data bytes are sent over the HP-IB only if the device is addressed to Talk and the HP-IB Controller has allowed a byte transfer to take place. If these two conditions are not met when a data byte reaches the end of the FIFO, it is held there until they are met.

Within an HP-IB Controller, the data byte will be sent over the HP-IB as soon as it reaches the end of the FIFO. However, the host processor must guarantee that it is addressed to Talk at this time and not in Serial Poll Mode. Otherwise, the DATABYTE code will be erroneously interpreted as a BYTE TRANSFER ENABLE.

INTERFACE COMMAND:
(HP-IB CONTROLLERS ONLY)

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
0	1	0	INTERFACE COMMAND CODE							

When this word reaches the HP-IB end of the Outbound FIFO, the Interface Command byte is sent over the HP-IB to all devices on the bus. During this transfer, the PHI Chip automatically sets the value of DIO8 to generate odd parity on the HP-IB.

BYTE TRANSFER ENABLES:
(HP-IB CONTROLLERS ONLY)

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
LF INH	0	BYTE COUNT								

UNCOUNTED TRANSFER ENABLE: (See Note 2)

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
1	1	0	0	0	0	0	0	0	0	

After addressing another device to talk, the host processor should place a BYTE TRANSFER ENABLE into its own Outbound FIFO to remove the ATN signal form the HP-IB and allow bytes to be sent to all addressed listeners. The PHI Chip will automatically terminate this transfer when:

a. A byte is sent with its accompanying END bit.

b. An ASCII Line Feed Character (hex 0A) is sent during a counted transfer whose LF INH (Line Feed Inhibit) bit is "0".

c. The number of bytes specified by a BYTE COUNT field have been sent. An all-zero BYTE COUNT field is used to specify a 256-byte transfer.

An HP-IB Controller must guarantee that either it is not addressed to Talk or it is in Serial Poll Mode when a BYTE TRANSFER ENABLE reaches the end of the FIFO. Otherwise, it will be erroneously interpreted as a DATA BYTE.

NOTE

1. An HP-IB Controller can also use a BYTE TRANSFER ENABLE to obtain its own Serial Poll response byte or Identification Code bytes if desired for self diagnosis.

2. If bits 8 through 15 of an UNCOUNTED TRANSFER contain a non-zero value, they will be interpreted as a BYTE COUNT field and counting will be performed in spite of the high-order "11" code.

3-44. INBOUND FIFO

Each read from Register 0 retrieves one word from an eight-word-long Inbound FIFO queue. This FIFO is used by the PHI Chip to hold data bytes and Secondary Addresses that have arrived from the HP-IB and are waiting to be read by the host processor.

If the Inbound FIFO is empty during any attempt to read from it, one of the two following situations will occur:

a. If the device containing the PHI Chip is the HP-IB Controller and has been conducting a Parallel Poll for at least two microseconds (the Outbound FIFO has been empty for at least two microseconds), the read from Register 2 will receive the DIO line responses of the eight polling devices, masked and normalized by Registers 4 and 5. This word will have the following format:

PARALLEL POLL RESPONSES:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
0	0	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	

It is recommended that the host processor attempt to obtain these responses only when servicing the provided PARALLEL POLL RESPONSE interrupt.

b. In all other cases, the read form Register 0 will obtain a word of indeterminate value and the HANDSHAKE ABORT bit (bit 9) in Register 2 will be set.

An aborted attempt to read from the Inbound FIFO can be repeated, if desired, until a valid word is finally obtained.

Data bytes enter the Inbound FIFO from the HP-IB only if the device containing the PHI Chip is addressed to Listen while they are being sent. Secondary Addresses enter the

Inbound FIFO only if the preceeding Interface Command sent over the HP-IB was the device's primary Talk or Listen Address.

If the PHI Chip is in the process of receiving a data byte or a Secondary Address from the HP-IB but either the Inbound FIFO is full or the DEVICE CLEAR bit in Register 2 is set, the HP-IB handshake will be held off until the host processor reads a word from the FIFO or clears the DEVICE CLEAR bit. An interrupt is provided by the PHI Chip to notify the host processor when the Inbound FIFO contains one or more words for it to read.

The Inbound FIFO is initialized to an empty state only when the PON input pin has a low value.

When a word enters the Inbound FIFO, its two high order bits (D0,D1) are set to indicate whether it is a Secondary Address, a standard data byte, or the last data byte of a record or requested sequence.

DATA BYTE:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
0	0	DATA BYTE VALUE								

This format is used for any received data byte that is not the last byte of a subgroup or record as defined below.

LAST BYTE OF SUB GROUP:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
1	0	DATA BYTE VALUE								

This format is used only within HP-IB Controllers for a data byte that caused the byte count of a BYTE TRANSFER ENABLE to expire, but which is not the last byte of the record as defined below.

LAST BYTE OF RECORD:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
1	1	DATA BYTE VALUE								

This format is used for a received data byte that is the last byte of a record and will occur in either of the following two cases:

a. The END bit that accompanied the data byte on the HP-IB was set to a "1".

b. Within HP-IB Controllers only, the data byte is an ASCII Line Feed character that was received in response to a BYTE TRANSFER ENABLE which requested Line Feed detection.

SECONDARY ADDRESS:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
0	1	0	0	TLK	SECONDARY ADDRESS					

This format contains the five-bit address field (DIO5-DIO1) of a Secondary Talk Address or Secondary Listen Address received from the HP-IB.

After an HP-IB Controller sends a Primary Talk or Listen Address to instruct a device to participate in the next byte transfer, it can send a Secondary Talk or Listen Address to further define the source or destination of the bytes within the device. When a PHI Chip receives a Secondary Address from the HP-IB Controller, it is placed into the Inbound FIFO for evaluation by the host processor.

The TLK bit is set to a "1" if the preceeding Primary Interface Command was the Talk address of the device containing the PHI Chip. The TLK bit is set to a "0" if the preceeding Primary Interface Command was the device's Listen address.

3-45. REGISTER 1: STATUS

REGISTER FORMAT:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
--	--	HI ORDER ACCESS		REM	HPIB CTRL	SYST CTRL	TLK/IDF	LTN	DATA FRZ	

Register 1 can be read at any time by the host processor to obtain the values of eight status conditions within the PHI Chip. A write into this register can affect only bits 8,9, and 15 as defined below:

BIT DEFINITIONS:

Bits 0,1 — UNASSIGNED:

Always will have a zero value when read.

Bits 8,9 — HIGH-ORDER BIT ACCESS:

These bits are intended to act as a substitute for pins D0 and D1 in applications where only an eight-bit data path is available for communication between the PHI Chip and its host processor. Whenever any PHI register other than Register 1 is read by the host processor, these two bits are set to the values being sent out of the PHI Chip on pins D0 and D1 for later access by the processor. Reading from Register 1 does not cause any change in the value of these bits.

Conversely, if the "8 BIT PROCESSOR" bit in Register 6 is set while any PHI register other than Register 1 is being written into by the host procesor, these two bits are used

instead of pins D0 and D1 as the source of high-order bit data for the register.

These bits can be altered directly by a write to Register 1 and if bit 15 is written as a "0", this write operation will not have any other effect on the state of the PHI Chip. These bits are useful in some 10-bit data path applications since they provide a "second chance" to access the high-order bits of the Inbound FIFO after a read from Register 0.

Bit 10 — REMOTE:

This bit has a "1" value if the device containing the PHI Chip is in the Remote state as defined in the HP-IB Interface Standard. It is mainly for use within devices that can be programmed either from their front panel or via the HP-IB.

Bit 11 — HP-IB CONTROLLER:

This bit has a "1" value whenever the device containing the PHI Chip is the current HP-IB Controller. It is set when any one of the following conditions are met:

a. A "Take Control" Interface Command is received from the current HP-IB Controller.

b. The IFC line of the HP-IB is asserted (within System Controllers only).

This bit is cleared when any one of the following conditions are met:

a. The PON input pin is brought low.

b. The PHI Chip goes from the "offline" to the "online" state.

c. A "Take Control" Interface Command is sent to another device on the HP-IB.

d. The IFC line of the HP-IB is asserted (within non-System Controllers only).

Bit 12 — HP-IB SYSTEM CONTROLLER:

This bit has a "1" value when the device containing the PHI Chip is the System Controller of the HP-IB (its SCTRL pin is high) or when the PHI Chip is offline.

The HP-IB System Controller is the only device in a system that can assert the IFC or REN lines of the HP-IB.

When a device is offline, the IFC and REN lines are asserted only within the PHI Chip and not on the actual HP-IB. This feature is very useful in offline diagnostics since it allows any device to set IFC while it is offline to locally become its own HP-IB Controller. It can then send itself Interface Commands and test its response to them offline without interfering with the operation of the real HP-IB.

Bit 13 — ADDRESSED TO TALK OR IDENTIFY:

This bit has a "1" value whenever the device containing the PHI Chip is addressed to Talk or to send Identification Bytes over the HP-IB, whether or not a Serial Poll is being conducted.

Bit 14 — ADDRESSED TO LISTEN:

This bit has a "1" value whenever the device containing the PHI Chip is addressed to Listen to bytes sent over the HP-IB.

Bit 15 — OUTBOUND DATA FREEZE:

This bit becomes set within an non-controlling device whenever a byte enters its Inbound FIFO from the HP-IB (not from its own Outbound FIFO). While it is set, it prevents data from leaving the Outbound FIFO over the HP-IB to give the host processor a chance to read the byte that arrived and possibly change its mind about sending any data that is already in the Outbound FIFO. The host processor can reset this bit by writing a "1" into its bit position, but only if the Inbound FIFO is empty, i.e., no other byte has arrived from the HP-IB.

3-46. REGISTER 2: INTERRUPTING CONDITIONS

REGISTER FORMAT:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
INT PEND	PRTY ERR	STAT CHNG	PROC ABRT	PP RESP	SERV RQST	FIFO ROOM	FIFO BYTE	FIFO IDLE	DEV CLR	

Register 2 is provided for use by the host processor in identifying the cause of an interrupt generated by the PHI Chip. Each bit in this register is associated with a particular interrupting condition as defined below. But the bits can be unconditionally forced to a "0" value (masked off) over and above its definition by assigning a "0" value to the corresponding bit in Register 3 (INTERRUPT MASK). Whenever a bit is masked "off", it loses the ability to cause an interrupt of the host processor.

Bits D10 through D14 represent the states of the PHI Chip. Unless they are masked off by Register 3, they are read as "1" values and continuously cause an interrupt condition as long as their associated states exist. Writes to Register 2 have absolutely no effect on their values.

Bits D1,8,9, and 15 are set when particular events occur and are reset only when the host processor writes a "1" into their bit positions in Register 2. Writing "0"s into the bit positions in Register 2 has no effect on their values. These bits are initialized to "0" whenever the PON line is low.

BIT DEFINITIONS:

Bit 0 — INTERRUPT PENDING:

This bit is the logical "OR" of the nine enabled low order bits which are enabled by corresponding bits of Register 3. When the value of this bit is a "1" after being enabled by bit 0 of Register 3, the PHI Chip provides a continuous interrupt to the host processor by grounding the INT line. Writing into Register 2 affects the value of this bit only when the value of the event recognition bits included in the "OR" function are changed.

Bit 1 — PARITY ERROR:

This bit is set whenever an Interface Command is received without odd parity. It is cleared when the host processor writes a "1" into its bit position.

Bit 8 — STATUS CHANGE:

This bit is set whenever there is a change in the value of the REMOTE bit in Register 1 while the PHI Chip is a non-controller, or whenever there is a change in the value of the HP-IB CONTROLLER bit in Register 1. It is cleared when the host processor writes a "1" into its bit position.

Bit 9 — PROCESSOR HANDSHAKE ABORT:

This bit is set whenever there is a read from the Inbound FIFO while it is full. It does not get set within HP-IB Controllers that have been conducting a Parallel Poll for at least 2 microseconds. If the host processor desires to repeat the read or write until it is normally completed, the PHI Chip guarantees that data will not be lost. This bit is cleared when the host processor writes a "1" into its bit position.

Bit 10 — PARALLEL POLL RESPONSE
(for HP-IB Controllers only):

A "1" value in this bit position indicates that a Parallel Poll is being conducted and one or more devices are indicating a need for service. Specifically, this interrupt occurs as long as all the following conditions are true:

a. The Outbound FIFO is empty and hence a Parallel Poll is being performed.

b. The Parallel Poll has been performed for at least 2 microseconds to provide time for the bus DIO lines to settle.

c. The Inbound FIFO is also empty so that the host processor will not obtain data when it reads from Register 0 in response to this interrupt.

d. One of the devices on the HP-IB is indicating a need for service by asserting a DIO line which has been masked "ON" by Register 4. The level of assertion depends on the corresponding bit in Register 5.

Bit 11 — SERVICE REQUEST
(for HP-IB Controllers only):

A "1" value in this bit position indicates that one or more devices are requesting service via the bus SRQ line.

Bit 12 — FIFO ROOM AVAILABLE:

A "1" value in this bit position indicates that the Outbound FIFO is not full and can accept writes without aborting.

Bit 13 — FIFO BYTES AVAILABLE:

A "1" value in this bit position indicates that the Inbound FIFO contains one or more bytes that can be read by the host processor.

Bit 14 — FIFO IDLE:

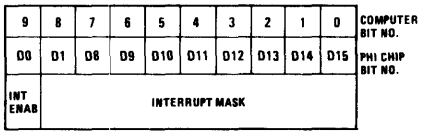
A "1" value in this bit position indicates that the Outbound FIFO is empty. Within HP-IB Controllers, this situation always causes a continuous Parallel Poll to be performed.

Bit 15 — DEVICE CLEAR:

This bit is set whenever a "Device Clear" Interface Command is received via the HP-IB while the PHI Chip is a non-controller. While it is set, it blocks all transfers between the FIFO's and the HP-IB so that they can be cleared by the host processor without losing data. The host processor can then clear this bit by writing a "1" into its bit position.

3-47. REGISTER 3: INTERRUPT MASK

REGISTER FORMAT:



A "0" value in any bit position of Register 3 causes the corresponding bit in Register 2 to always read as "0" and prevents that bit from causing an interrupt to the host processor. Since the INTERRUPT ENABLE (INT ENAB) bit can hold off all interrupts by directly masking bit 0 in Register 2, the host processor can view all interrupting conditions without getting an interrupt by setting it to "0" and setting all other mask bits to "1".

Register 3 can be read or written by the host processor at any time and is initialized to all zeros whenever the PON line is low.

3-48. REGISTER 4: PARALLEL POLL MASK / FIRST ID BYTE

REGISTER FORMAT:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
MASK BITS/FIRST ID BYTE										

Register 4 can be read or written at any time within an HP-IB Controller to provide a mask for incoming Parallel Poll responses. Within a non-controlling device, it is used by the host processor to specify the first byte of a two-byte product type Identification Code as define below. All bits are initialized to "0" whenever the PON input has a low value.

Within an HP-IB Controller:

Each bit in this register that has a "0" value masks "OFF" (forces to zero) the Parallel Poll response arriving via its corresponding DIO line whenever a Parallel Poll is being conducted (see Register 5 for further information on responses from the DIO lines). Only those responses that are not masked "OFF" are included in the determination of the Parallel Poll Response interrupt.

Within a non-controlling device:

This register and Register 5 can optionally participate in an identification sequence through which the HP-IB Controller can find out what kind of device exists at each HP-IB address. If it is desired to use this feature, the host processor should perform the following set-up:

a. Before going online, Registers 4 and 5 should be loaded with a 16-bit device type Identification Code assigned to the product and the "Respond to Parallel Poll" bit in Register 6 should be set.

b. The PHI Chip should be placed online while the "Respond to Parallel Poll" bit is still set, causing it to indicate a need for service during a Parallel Poll conducted by the HP-IB Controller.

c. After the HP-IB Controller has acknowledged that it has seen the Parallel Poll Response, the "Respond to Parallel Poll" bit can be cleared.

After the above set-up has been performed, circuitry within the PHI Chip is enabled to allow it to respond to a special Primary/Secondary address pair separate from its normal HP-IB address, without any interaction with the host processor. Whenever the PHI Chip receives Talk Address 31 followed by a Secondary Address containing a 5-bit HP-IB ADDRESS specified in Register 7, first it will sent the contents of Register 4 and then the contents of Register 5 as data bytes, marking the contents of Register 5 with an accompanying END bit as it is sent. The secondary adddressing used obeys all the rules of an "Extended Talker" defines in the IEEE Standard 488-1978.

If this feature is not dsesired, the "Respond to Parallel Poll" bit should have a "0" value at the time the PHI Chip goes online. This causes all of the special address pair recognition circuitry to be disabled.

3-49. REGISTER 5: PARALLEL POLL / SECOND ID BYTE

REGISTER FORMAT:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
SENSE BITS/SECOND ID BYTE										

Register 5 can be read or written at any time within an HP-IB Controller to specify the assertion levels of the incoming Parallel Poll responses. Within a non-controlling device, it is used by the host processor to specify the second byte of a two-byte product type Identification Code as defined below. All bits are initialized to "0" whenever the PON input has a low value.

Within an HP-IB Controller:

Each bit in this register is "Exclusive-OR'ed" with the Parallel Poll response arriving via its corresponding DIO line whenever a Parallel Poll is being conducted. A particular bit should be set to a "1" only if it is known that the device responding via its corresponding DIO line is using a "0" value to indicate its need for service. Multiple devices can be programmed to use a "0" value on the same DIO line to indicate readiness for some operation and the Controller will see the interrupt only after they are all ready.

Within a non-controlling Device:

This register and Register 4 can optionally participate in an identification sequence through which the HP-IB Controller can find out what type of device exists at each HP-IB address. Complete details of this sequence are contained in the description of Register 4.

3-50. REGISTER 6: CONTROL

REGISTER FORMAT:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
--	--	8 BIT PROC	PRTY FRZ	REN	IFC	RSPD PP	RQST SRVC	FIFO SEL	INIT FIFO	

Register 6 can be read or written at any time by the host processor to access control bits within the PHI Chip. All bits are initialized to "0" whenever the PON pin is low.

BIT DEFINITIONS:

Bit 0 — RESERVED:

This bit always has a "0" value when read and must never be written as a "1".

Bit 1 — RESERVED:

This bit always has a "0" value when read and must never be written as a "1".

Bit 8 — 8-BIT PROCESSOR:

A "1" value in this bit position indicates to the PHI Chip that the host processor wishes to use an 8-bit data path instead of the standard 10-bit path. Specifically, during a write to any register except Register 1, the PHI Chip uses the current values of bits 8 and 9 of Register 1 instead of data which would normally arrive via the D0 and D1 lines. D0 and D1 lines can be left untied if only 8-bit communication is desired (bit 8 will always be set. However, during reads form the PHI Chip, D0 and D1 always contain valid high-order bit values, even if bit 8 is set, and may prove useful in some applications.

Bit 9 — PARITY FREEZE:

Whenever this bit has a "1" value, the PHI Chip will refuse to accept or interpret any Interface Command (including device addresses) that does not have odd parity. This will force the HP-IB to remain frozen with DAV asserted and the erroneous Interface Command held on the bus DIO lines until the HP-IB Controller aborts the transfer by removing DAV. This bit does not affect in any way the "PARITY ERROR" interrupt bit in Register 2.

Bit 10 — REN VALUE (System Controllers only):

If the device containing the PHI Chip is the System Controller of the HP-IB, this bit determines the value of the bus REN line.

Whenever this line is asserted, it must remain asserted for at least 100 microseconds to meet the IEEE Std 488-1978 specifications.

A System Controller can assert the REN line at any time to allow programmable devices tied to the HP-IB to be remotely programmed in lieu of using their front panel controls.

When the PHI Chip is "offline", this bit can be used locally in diagnostics whether or not the device is the System Controller.

Bit 11 — IFC VAUE (System Controllers only):

If the device containing the PHI Chip is the System Controller of the HP-IB, this bit determines the value of the bus IFC line.

Whenever this line is asserted, it must remain asserted for at least 100 microseconds to meet the IEEE Std 488-1978 specifications.

A System Controller can assert the IFC line at any time to initialize the HP-IB interfaces within all devices connected to the HP-IB. Note that the devices themselves are not initialized, only their HP-IB interfaces. Assertion of this line also has the effect of forcing the System Controller to be the HP-IB Controller no matter which device previously had this capability (see Register 1, HP-IB Controller bit). As a result, the System Controller need not follow the normal "Take Control" Interface Command protocol when it wishes to regain control of the HP-IB after it has passed it away or when it has just gone "online".

When the PHI Chip is "offline", this bit can be used locally in diagnostics whether or not the device is the System Controller.

Bit 12 — RESPOND TO PARALLEL POLL:

Whenever this bit has a "1" value, the PHI Chip will indicate a need for service during any Parallel Poll if it has Parallel Poll response capability (refer to the description of HP-IB ADDRESS in Register 7).

Bit 13 — REQUEST SERVICE:

Whenever this bit has a "1" value, the PHI Chip will use the HP-IB SRQ line and Serial Poll facility to request service from the HP-IB Controller in accordance with the rules of the HP-IB Interface Standard:

a. It begins asserting the SRQ line as soon as this bit is set.

b. When it is first polled by the HP-IB Controller during a Serial Poll, it stops asserting the SRQ line and responds to this poll and all subsequent ones with a hex 40 (DIO 7 ="1").

c. The host processor should keep this bit set until service is obtained from the HP-IB Controller.

d. After the host processor clears this bit, the PHI Chip will respond to all Serial Polls with a hex 80 (DIO 7="0" and odd parity).

Bit 14 — DMA FIFO SELECT:

Whenever this bit has a "1" value, the DMARQ pin of the PHI Chip will be asserted (low) whenever the Outbound FIFO is ready for a write operation. If this bit has a "0" value, the DMARQ pin will be asserted whenever the Inbound FIFO is ready for a read operation.

Bit 15 — INITIALIZE OUTBOUND FIFO:

Any time a "1" value is written into this bit position, the Outbound FIFO will be forced empty but not necessarilly unfrozen (see Register 1 bit 15). If the empty FIFO is in an HP-IB Controller a continuous Parallel Poll will be executed (see Register 0 Outbound FIFO section). No actual storage location corresponds to this bit position and it always has a "0" value when read.

3-51. REGISTER 7: HP-IB ADDRESS

REGISTER FORMAT:

9	8	7	6	5	4	3	2	1	0	COMPUTER BIT NO.
D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	PHI CHIP BIT NO.
--	--	ONL	TA	LA	HP-IB ADDRESS					

Register 7 can be read or written at any time by the host processor to specify an HP-IB Address and related control information to the PHI Chip. All bits in this register are initialized to zero whenever the PON line is low.

BIT DEFINITIONS:

Bit 0 — RESERVED:

This bit always has a "0" value when read and must never be written as a "1".

Bit 1 — RESERVED:

This bit always has a "0" value when read and must never be written as a "1".

Bit 8 — ONLINE:

Whenever this bit has a "1" value, the PHI Chip is "online" and will interact normally with the HP-IB. If it is a "0" value, the PHI Chip is "offline" and will not interact in any way with the HP-IB. When this bit becomes set, the PHI Chip waits for a period equal to the width of IOGO before actually going online. During this period, the PHI Chip initializes its interface circuitry to the HP-IB so that it does not start out as a Talker, Listener, or Controller. This performs the function of the "pon" message defined in the IEEE Standard. If other bits in Register 7 were set simultaneously with the ONLINE bit, they are also given a chance to settle during this time.

Bit 9 — TALK ALWAYS:

This bit is included for communication between devices in systems without a controller and should not be set when a controller is present except in diagnostics. When the bit is set, the PHI Chip assumes that it is continually addressed to Talk unless the bus IFC line is being asserted. When it is cleared by the host processor, the PHI Chip continues to be addressed to Talk until the IFC line is asserted, the Talk address of another device is received, or the PON line is brought low.

Bit 10 — LISTEN ALWAYS:

This bit is included for communication between devices in systems without a controller and should not be set when a controller is present except in diagnostics. When the bit is set, the PHI Chip assumes that it is continually addressed to Listen unless the bus IFC line is being asserted. When it is cleared by the host processor, the PHI Chip continues to be addressed to Listen until the IFC line is asserted, the Unlisten command is received, or the PON line is brought low.

Bits 11 to 15 — HP-IB ADDRESS:

Within a non-controlling device, the values of these five bits determine the HP-IB address to which the PHI Chip will respond. Any address between 0 and 29 can be used but addresses 30 and 31 should be avoided. If the address specified is between 0 and 7, the PHI Chip will assume that it can respond to Parallel Polls initiated by the HP-IB Controller and will use a DIO line corresponding to its address. DIO 8 through DIO 1 correspond to address 0 through 7, respectively. The other addresses are not assigned initial Parallel Poll response capability but may be assigned it by the HP-IB Controller.

Within an HP-IB Controller, the PHI Chip always responds to Address 30 for Talking and Listening, not to the address specified by these bits. This feature allows constrants to be used for self-addressing within the Controller software.

3-52. OFFLINE DIAGNOSTICS

As long as bit 8 of Register 7 has a "0" value, the PHI Chip remains offline. This is also the state to which the PHI Chip is initialized. While the PHI Chip is offline, it is completely isolated from the HP-IB (see Figure 3-5). In this condition, the PHI Chip circuitry can be diagnosed by the host processor without interferring with the normal HP-IB operation.

Although the PHI Chip is isolated from the external HP-IB, its complete set of interface functions are still tied together internally and interact normally with each other via an internal copy of the HP-IB. It is important to note here that the circuitry used to do this is not special offline circuitry but the same circuitry used when the PHI Chip is online. All timing and sequencing satisfy all HP-IB specifications and regulations. All HP-IB programming protocols are required (i.e., Talk, Listen, etc).

Most diagnostics which can be performed offline require that the PHI Chip be the Controller of its internal HP-IB so that it can send itself Interface Commands. Since only an HP-IB System Controller can use the IFC line to take control of the HP-IB, an offline PHI Chip will assume System Controller status in spite of the value of its "SCTRL" pin.

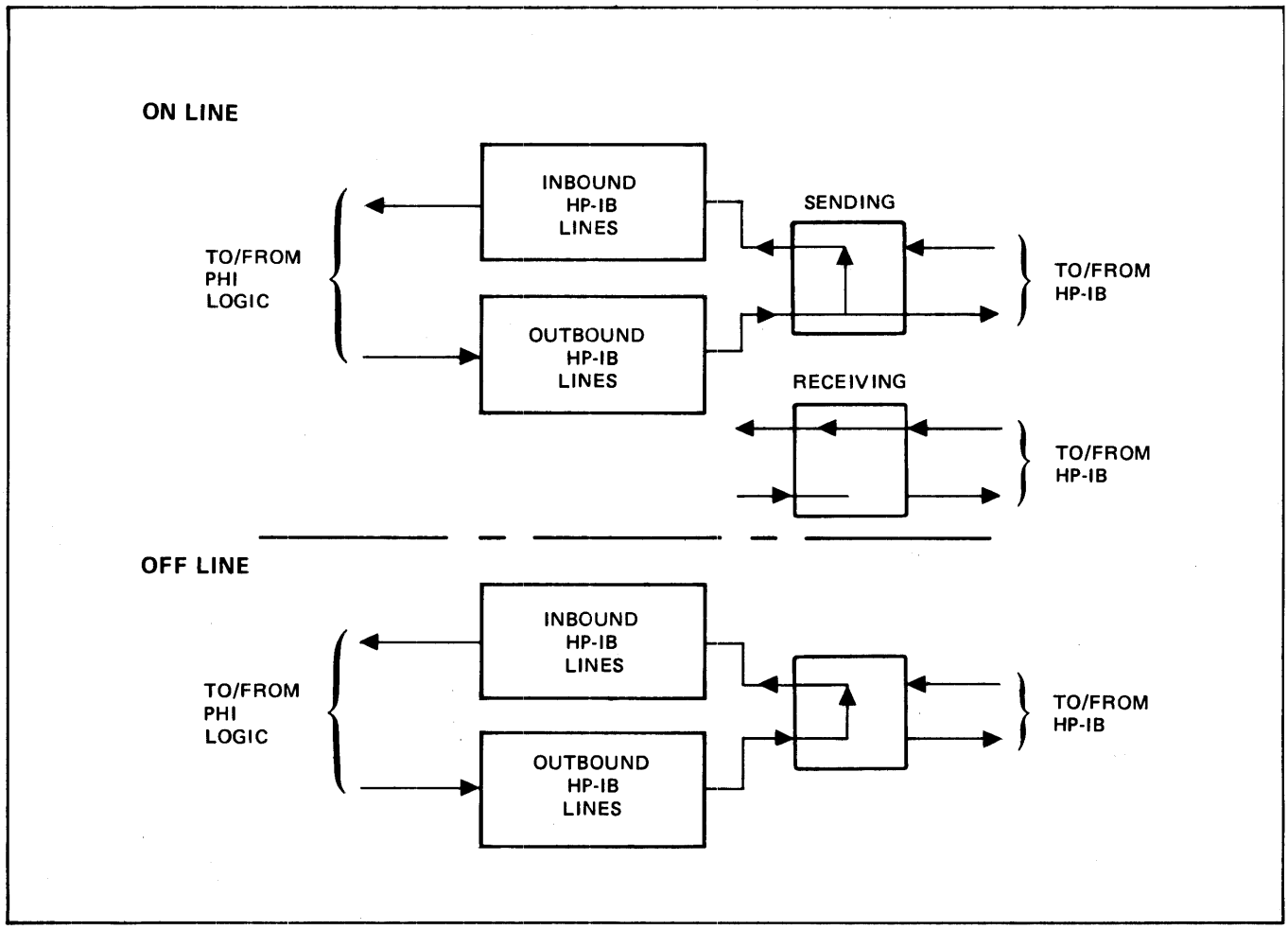


Figure 3-5. HP-IB Transceiver's On-line and Off-line States

SECTION IV
THEORY OF OPERATION

4-1. INTRODUCTION

This section provides information on the theory of operation of the HP-IB Interface, first at the block level (overview) and then at the functional level. The theory will cover individual components only when they serve a unique purpose.

In order to achieve a complete understanding of the HP-IB Interface, a copy of the IEEE Std 488-1978 and the HP 1000 L-Series Interfacing Guide, part number 02103-90005 should be available. The Interfacing Guide provides a detailed theory of operation for the I/O Master.

4-2. GENERAL DESCRIPTION

The HP 12009A HP-IB Interface provides a complete hardware interface between an L-Series computer and an HP-IB system of up to 14 devices. Several such HP-IB systems can be interfaced to an L-Series computer, each system requires a separate interface card.

Figure 4-1 shows the card in a typical L-Series system. As shown in the figure, the card can be installed in any I/O slot below the processor card unless the HP-IB Card is configured for high speed operation. When the card is configured for high speed operation, it must be installed in the first slot below the processor card (highest priority I/O slot). The HP-IB Card is then connected to the HP-IB system through the cable supplied with the kit.

To the L-Series computer, this card is an I/O card and is under its software control at all times. To the HP-IB system, this card may or may not be a System Controller, depending on the setting of the System Controller Select switch, U1S1.

The operation of the card is under control of the L-Series processor. Control words may be passed to the card and data exchanged through the system data bus by I/O instructions. Alternately, the processor may program the card's DMA machine which then reads from system memory the interface card's control words, HP-IB control messages, and exchanges data between the HP-IB and memory. Figure 4-2 shows a simplified block diagram of the HP-IB Interface Card.

As noted in Section I, the interface contains an I/O Master section and an HP-IB Bus Interface section. The I/O Master section gives the card the capability of handling its own Direct Memory Access (DMA), and of decoding its own instructions. The I/O Master section is composed of the I/O Processor Chip (U67) and its associated logic circuitry and performs all of the functions necessary for interfacing with the L-Series Backplane. The HP-IB Bus Interface section is composed of the PHI Chip (U43) and its associted logic circuitry. This interface provides the card with its HP-IB capability consisting of the following functions:

a. System Controller capability.

b. The ability to respond as a bus controlled device with proper L-Series programming.

c. Eight levels deep buffering of command and data bytes between the HP-IB and the card for both input and output.

d. Automatic handling of HP-IB handshakes.

e. Parallel Poll response mask and Service Request interrupt mask.

f. Facilities for DMA operation with the processor.

g. Simple electrical interface to the HP-IB through four transceiver chips and LS TTL interfacing to the I/O Master section.

h. Fast response to support the peak HP-IB throughput of 930 kbytes per second.

i. Automatic response to bus issued universal and addressed commands.

A six-bit select code for the card is set by a DIP switch (U1S3-S8) located on the card. This select code is used only as a means of addressing the card (I/O Master) and bears no relation to the DMA interrupt or priority of the card. The DMA interrupt and priority are determined solely by the physical location of the interface card from the processor card in the card cage. The card slots are marked from XA1 (highest priority) to XA10 or XA16 (lowest priority). The number of slots depends on the size of the backplane.

4-3. THEORY OF OPERATION OVERVIEW

The simplified block diagram shown in Figure 4-2 illustrates the basic operation of the HP-IB Interface Card in the L-Series system.

The main flow of data can be from the HP-IB system to the backplane through the HP-IB Bus Interface and the I/O Master or it can be from the backplane to the HP-IB system through the I/O Master and the HP-IB Bus Interface.

In some cases the data transfers may not include the I/O Master and the HP-IB data would only proceed as far as the PHI Chip. When the card is running a diagnostic, the PHI Chip can close off the external HP-IB lines and the signals go only as far as the PHI Chip (refer to Figure 3-5).

In the case of data going from the computer to the HP-IB system, the Data Bus Buffers take data from the Backplane's Data Bus and drives it onto the Buffered Data Bus. The Byte Packing Buffer takes the data off the Buffered Data Bus and converts the 16-bit data words into two 8-bit bytes (bit 0 through 7 Upper Byte and bit 0 through 7 Lower Byte). Two more bits (bits 8 and 9) are produced by the Control Register and are driven onto the PHI Data Bus (PHI Tag Bits). The Control Register also provides four other bits, derived from the Buffered Data Bus, bits 12 through 15, to the PHI Chip as the PHI Register Select bits A13,A14, and A15 and the PHI Chip's WRITE signal. The PHI Chip produces the HP-IB's 8-bits of data (DIO1-DIO8) and 8-bits of control to the HP-IB Transceivers. The HP-IB Transceivers drive these signals onto the HP-IB lines.

When data is to go from the HP-IB system to the computer's Backplane it follows this path. The HP-IB system applies its signals to the HP-IB Transceivers. The HP-IB Transceivers drive the data into the PHI Chip. The PHI Chip drives 10-bits (D0,D1, and D8-D15) onto the PHI Data Bus. The Byte Packing Buffers take two 8-bit bytes (upper and lower) and produces 16-bit words for the computer. It drives these words onto the Buffered Data Bus.The two PHI Tag Bits, D0 and D1, are applied to the Buffered Data Bus as bits 8 and 9 via the Control Register. The PHI Select Bus provides four bits (bit 0, 1,2, and 3) to the Control Register (upper byte). These four bits are driven onto the Buffered Data Bus as bits 12-15. The Data Bus Buffers take the 16-bit words and drives them onto the Backplane Data Bus as bits DB0 through DB15.

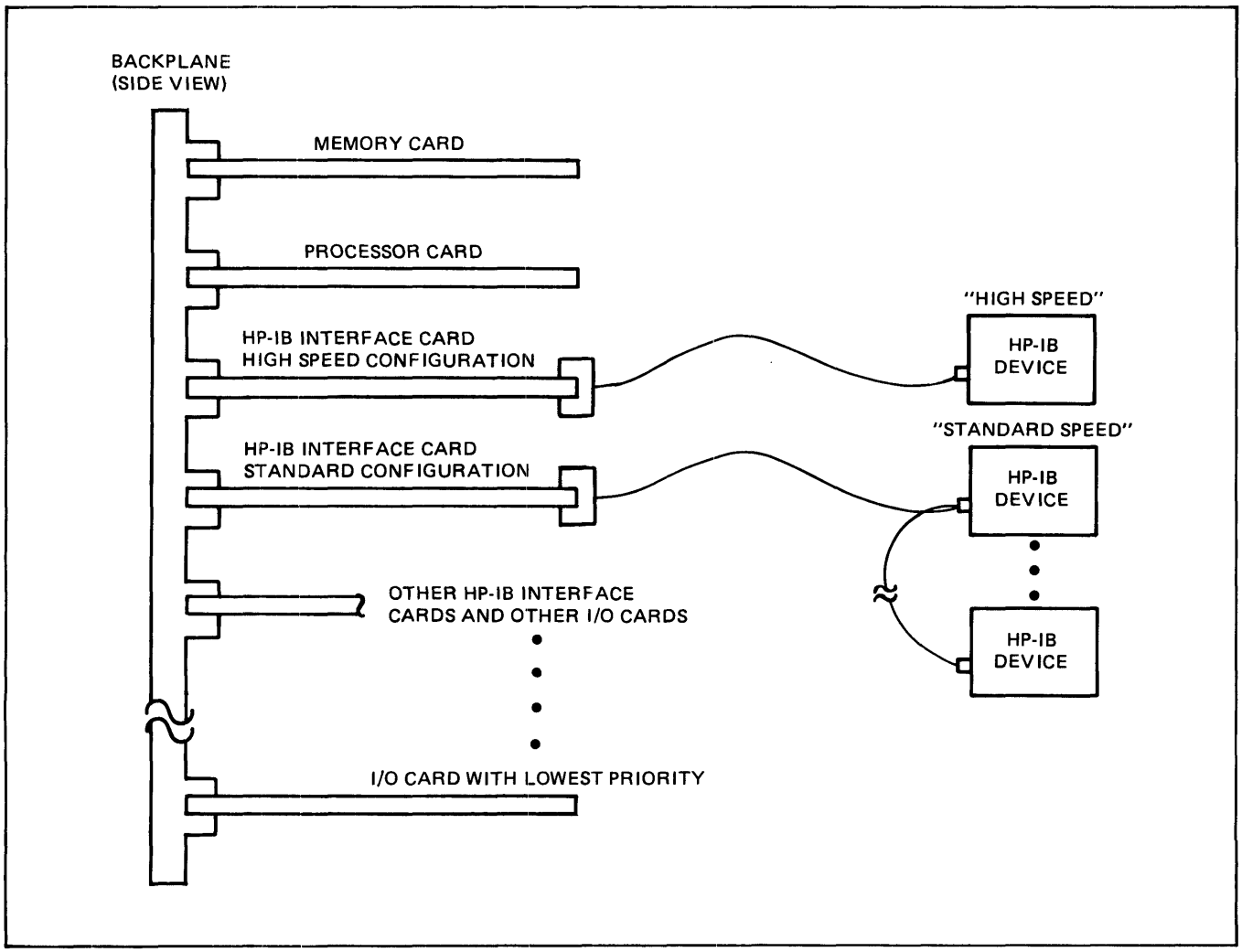


Figure 4-1. Typical L-Series System

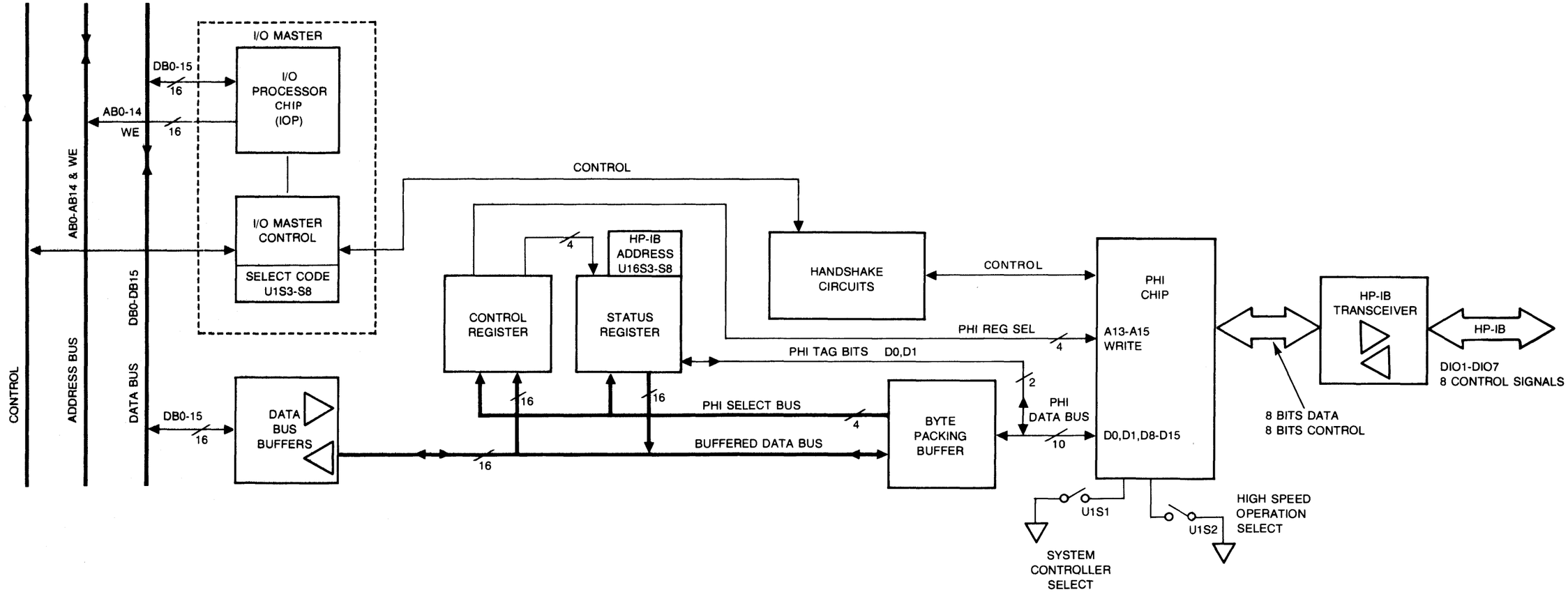


Figure 4-2. HP 12009A HP-IB Interface Simplified Block Diagram

7700-490

The PHI Chip has two switch selectable options: High Speed Operation Select and System Controller Select. If the System Controller Select option is selected, the HP-IB Interface Card will act as the System Controller. If the High Speed Operation Select option is selected, the HP-IB Interface Card will operate at approximately 930 kbytes per second.

The Handshake circuitry allows the PHI Chip and the I/O Master to work together. It allows the data and control exchanges to take place between these two major blocks.

4-4. FUNCTIONAL THEORY OF OPERATION

It is necessasry to refer to the three schematic logic diagrams (Figure 7-4) and to the Overall Functional Block Diagram (Figure 7-2) to be found in Section VII when reading this portion of the manual. It may be necessary to refer to the IEEE STD 488-1978 and the HP 1000 L-Series Interfacing Guide, part number 02103-90005 to achieve a full understanding of the theory of operation for this card. Integrated circuit base diagrams and function tables are provided in Figure 7-1 for all IC's and two SOS chips that are used on this card.

To simplify locating components on the three schematics, the following scheme is used. There are ten numbers across the top and bottom border of the schematics going from 10 to 19, 20 to 29, and 30 to 39. The first number indicates the sheet number, 1, 2, or 3, and the second number is the vertical column. A set of five alphabetical letters, A-E, are on the left and right borders of the schematics. This provides 50 easy to locate areas. To make the coordinates easy to find in the text, they are set off in brackets [ ]. For example, [25C] would be found on the second sheet, column numbered 5, and horizontal row C. The Secondary Address Latch flip-flop U23 is to be found at this location.

The descriptions of the various functions are highly interdependent. Therefore, the description of one function will be related to other functions. The four main functions are as follows:

a. Non-DMA Transfers
paragraphs 4-5 through 4-11

b. DMA Transfers
paragraphs 4-12 through 4-22

c. Control Word Transfers
paragraphs 4-23 through 4-25

d. Status Word Transfers
paragraphs 4-26 and 4-27

4-5. NON-DMA TRANSFERS

4-6. OUTPUT TRANSFER

4-7. LOADING THE CARD DATA REGISTER (OT* 30). The low byte (lower eight bits, bits 0-7) is clocked into U54 [32B], a 74LS373 by BCS1- and CKDAT- through the NAND gate U23 [31B], a 74LS02. The lower four bits of the upper byte (bits 8-11) are clocked into U85 [24B], a 74LS175 by CLK+. This signal is produced at U81 pin 6 [21B], a 74LS132 by BCS1-,CKDAT-, and LOBYT-. The four upper bits of the upper byte (bits 12-15) are clocked into U63 [34B], a 74LS175 by CLK+.

Bit 15 via U63 pins 6 and 7 controls the direction of the PHI Data Bus. When bit 15 is low, U63 pin 6 is high and pin 7 is low. The low on pin 7 enables U94 [25B], a 74LS244 to put PHI Tag bits D0 and D1 on the PHI Data Bus. The high on U63 pin 6 enables the lower eight bits (bits 0-7) from the Buffered Data Bus to be put on the PHI Data Bus via U54 [32B], a 74LS373. The 10 bits (0-9) on the PHI Data Bus are labeled by the PHI Chip U43 [35B] as bits D0,D1, and D8 through D15. The following table should clarify the bit labeling.

DATA WORD BIT	PHI DATA BUS BIT
0	D15
1	D14
2	D13
3	D12
4	D11
5	D10
6	D9
7	D8
8	D1
9	D0

Bits 14 through 12 via U63 select into which of the eight PHI Chip registers the PHI data will be loaded. Bit 14 is input A13 to the PHI Chip (high order bit), bit 13 is input A14, and bit 12 is input A15. Table 4-1 shows the PHI registers selected by the various codes.

Table 4-1. PHI Chip Register Selection Code and Names

PHI REGISTER SELECT CODE A13	A14	A15	PHI REGISTER NUMBER	SELECTED PHI CHIP REGISTER NAME
0	1	0	0	FIFO
0	1	1	1	STATUS
0	0	0	2	INTERRUPT
0	0	1	3	INTERRUPT MASK
1	1	0	4	PARALLEL POLL MASK
1	1	1	5	PARALLEL POLL SENSE
1	0	0	6	HP-IB CONTROL
1	0	1	7	HP-IB ADDRESS

Buffered Data Bus bits 10 and 11 do not apply to a data word transfer and must be a "0" at all times.

4-8. PROCESSING THE DATA WORD INSTRUCTION: STC 30,C. The STC 30,C instruction generates the signal DVCMD (Device Command) out of the I/O Processor Chip U67 pin 37 [16B]. DVCMD− is ANDed with SCLK+ via U91 pin 13 [21D], and U91 pin 1, a 74S02. This signal clocks the PHI Command F-F U112 [21E], a 74S74, causing U112 pin 5 to go high. The high output (GO+) of the PHI Command F-F initiates a PHI Chip handshake by asserting the IOGO pin on the PHI Chip, U43 pin 19 [35C], via U72 [33C], a 74S10, if DMA is not enabled or other conditions that will be explained in the DMA Transfer section. The PHI Command F-F remains set until the PHI Chip completes the handshake by asserting IOEND U43 pin 18. This signal is also referred to as FIND+ and FIND−. FIND+ is delayed through two 74S04 inverters, U83 [25D], to insure sufficient set up and hold times for the PHI Command F-F, U112 and is labeled DELFIND+. A test of the flag sense should not be performed because Flag 30 in the I/O Processor Chip will not be set by the data transfer.

4-9. INPUT TRANSFER

4-10. PROCESSING THE INPUT DATA WORD INSTRUCTION: OT* 30 or OT* 31 STC 30,C. The OT* instruction transfers a word into the Outbound Register, U44 and U74,[33B] or into the Control Word Register. This word is used to select the PHI Chip register that will be the source of the input transfer.

Bit 15 (WRITE) of the Buffered Data Bus is used to tell the PHI Chip that this will be an inbound transfer (bit 15=1) from the register selected by bits 14,13, and 12. This information need not be reestablished between successive transfers from the same register. STC 30,C provides a device command that initiates a PHI handshake as described in paragraph 4-8. FIGO− and DELFIND+ are gated through a 74LS27, U24 [32B], to latch the lower eight bits (8 through 15) of the PHI Data Bus into a 74LS373, U44 [33B], which requires no set up time (see Figure 4-3). The PHI Tag Bits, D0 and D1, are latched into a 74S157, U95 [27B], by the PHI handshake (FIGO− and FIND+) gated through a 74S02, U104 [27D], which requires 4.5 ns set up time. The timing for this latch is the same as for U24 and is shown in Figure 4-3.

The 74LS157, U95 [27B], latches the data by passing its output back into input A. When the select line, pin 1, is high, the data on input B is passed to the output and back into input A. When the select line changes, the input A is passed to the output and the data is latched.

4-11. LOADING THE INPUT DATA WORD INSTRUCTION: LIA 30. The data word is loaded into the computer by an LIA 30 instruction. The I/O Master generates a Bus Select Code (BCS5−) that enables the 10 bits of the PHI Data Bus onto the Bufferd Data Bus via U94 [27B] and U44 [33B]. U94 drives the data word onto the Buffered Data Bus when U84 pin 11 [25A] goes low. U94 also insures that input data word bits 10 and 11 will be "0". The upper four bits (bits 12-15) label the input data word with the direction and register number from which the word was read. They are enabled onto the Buffered Data Bus by U73 [25B], a 74LS258. This multiplexer with its select input (pin 1) driven by BCS7-(LDSTAT), passes the PHI Select Bus (read/write and the register select bits) whenever either the data or control register is read. U101 pin 12 [21A] and U103 [25B] provide an output control to the multiplexer whenever BCS5,BCS6, or BCS7 are present without "BYTE". This is a DMA signal that will be discussed in the DMA Transfer section, paragraph 4-12 through 4-22.

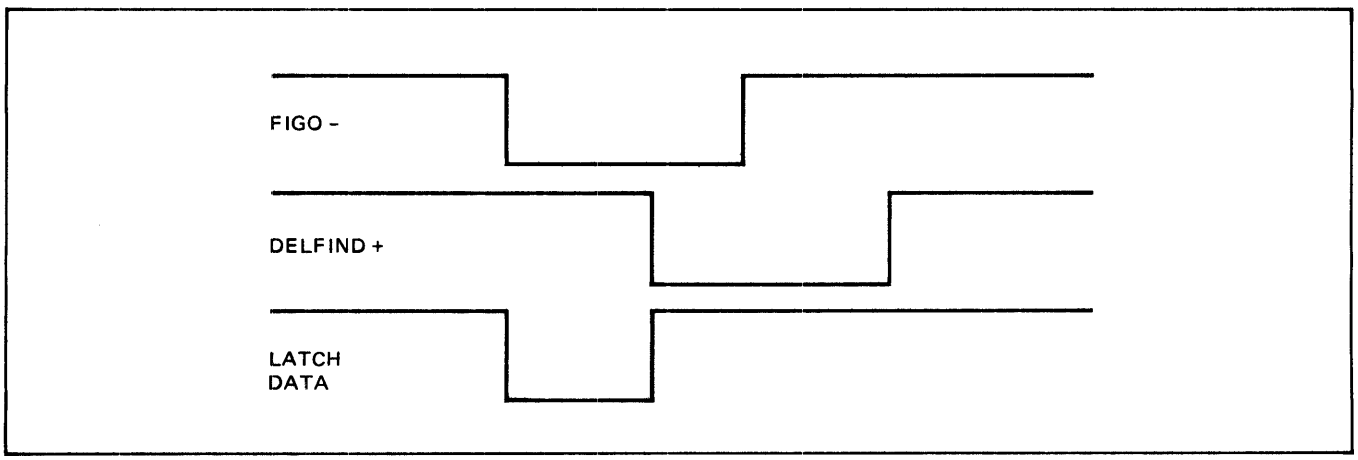


Figure 4-3. FIGO− and DELFIND+ Timing Diagram

4-12. DMA TRANSFER

The HP-IB Interface Card requires that the Card Control Word (Register 31) be loaded to indicate the direction of the transfer and the PHI Chip register that will be accessed by the Byte Mode transfer. The rest of the control word affects the setting of the Device Flag and the termination of the DMA transfer. Each bit of the card control word is discussed in detail in Section III PROGRAMMING of this manual.

4-13. DMA WORD MODE TRANSFERS

4-14. DMA OUTPUT TRANSFER. The DMA data transfer is identical to the non-DMA transfer covered is paragraph 4-7 except that the handshake is provided by the DMA machine. The Device Command bit being set in the DMA control word generates a FIGO handshake as previously covered in paragraph 4-8. The FIGO from a DMA transfer is held off by U72 [33C], a 74S10, until the PHI Chip is ready for a word (DMARQ). If the FIFO is selected, then it is a DMA transfer. The signal (FIFO+) at U24 pin 12 to U72 pin 2 prevents overrunning the FIFO, as this would destroy data already in the FIFO.

4-15. DMA INPUT TRANSFER. The input transfer is processed in the same manner as previously covered in paragraph 4-10 except that the Device Command is provided by the DMA machine. The data paths are identical to those described in paragraph 4-11 and the handshake is described in paragraph 4-14.

4-16. DMA BYTE MODE TRANSFERS

4-17. DMA BYTE MODE OUTPUT TRANSFER. The DMA control word (register 21) initiates the byte mode pack mode. The I/O Master sends one DVCMD− command for each byte and therefore, one FIGO- is generated for each byte transfer. The I/O Master generates the byte packing signal, low byte (LOBYT−)[18B] that is passed through U14 [31B], a 74LS375, to generate both senses of LOBYT which when gated with the WRITE- bit (bit 15 of the Buffered Data Bus) of the control word enables the data byte, upper or lower, of the Buffered Data Bus onto the PHI Data Bus. The "Q" output of U14 [31B] is gated with WRITE− via U34 pin 3 [31B], a 74LS00, to enable U64 [31B], a 74LS373, to drive the upper eight bits (bits 8-15) onto the PHI Data Bus. The "$\overline{Q}$" output from U14 pin 14 [31B] gated through U34 pin 11 enables U54 [32B], a 74LS373, to drive the lower eight bits (bits 0-7) onto the PHI Data Bus. PHI Data Bus bits 0 and 1 are driven onto the bus by U94 [26B,27B], a 74LS244. D1 is provided whenever bit 8 (ATN) of the control word is set. D0 is provided if on the last byte transferred (DMAEN not asserted), bit 9 (EOI) is set in the control word. This gating is accomplished by two gates of U62 [24B,25B), a 74LS02. The NAND gate (U62) at [24B] determines if the transfer is a word mode transfer or if DMA enable (BDMA−) has gone away and, if so, it drives U62 pin 8 [25B] low. U62 pin 10 then drives U94 pin 8 high, if the EOI bit is set.

4-18. DMA BYTE MODE INPUT TRANSFER. The I/O Master provides the DVCMD− signal that initiates the PHI handshake thus providing the storage signal to the data latches as noted in paragraph 4-10. The first byte (bits 8-15) that is transferred out of the PHI Chip is stored into both of U44 and U74 [33B, 343B], 74LS373's, by U24 [32B], a 74LS27. When the I/O Master changes the LOBYT− signal, U14 disables the section of U24 that latches the upper byte of data into U74. The next FIGO− stores the next byte of data into the lower byte latch U44. U74 and U44 will be read by DMA when it is ready. PHI data bits D0 and D1 are latched into U95 as covered in paragraph 4-10. Since in the byte mode, these bits can not be read, the hardware must check these bits for special functions and meanings. The Tag Bit Decoder, U105 [26C], a 74S138, detects two special messages from the PHI FIFO, end of record (EOR−) and my secondary address (MSA−). Bit 9 of the control word enables "EOR" through two of U104's gates [23C,24C],a 74S02's, to assert the signal last byte (LSBYT−) that terminates the DMA transfer. Bit 8 of the control word enables "MSA" through two of U104's gates [23C,24C], a 74S02, to assert LSBYT− and terminate the DMA transfer. The Secondary Address Latch, U23 [25C], a 74LS74, is set when a secondary address is received to flag the data transfer if the termination bit is not enabled. Both EOR− and MSA− are checked as status bits 13 and 12.

4-19. DMA I/O MASTER HANDSHAKE

The basic I/O Master data transfer handshake involves the device setting the service request (SRQ−) and the I/O Master returning the service acknowledge (SACK−). The discussion of the handshake will be covered in three parts:

a. Starting DMA,

b. During DMA, and

c. Terminating DMA.

4-20. STARTING DMA. If the DMA transfer is an output transfer, the first SRQ− is issued when U92 [23D], a 74LS27, connected as a cross-coupled latch, sets U92 pin 12 to a "1". This puts a "1" on U93 pin 3 [22D], a 74S153, and provides a clock to U112 [21C], a 74S74, that pulls SRQ− low. U92 pin 5 reads bit 3 of the control word via U115 [22B], a 74LS04, and delays DMA operations until an interrupt occurs causing U114 pin 8 [23C], a 74LS20, to go to a "1". If U92 is set, the DMA start-up is held off until U114 indicates that one of the interrupt conditions exists. The interrupt conditions are: an SRQ from the bus, receiving a secondary address, a PHI interrupt, or receiving a "Group Execute Trigger". If control word bit 3 is not set, then the SRQ is generated as soon as DMAEN− [19B] is asserted. If the transfer is an input, the first SRQ is generated by FIND+ applied to the C0 and C1 inputs (pins 5 and 6) of U93.

4-21. DURING DMA. During the DMA data transfer, the output SRQ's are provided by FIGO+ applied to the C2 input (pin 4) of U93. The input SRQ's are provided by FIND+ applied to the C0 and C1 inputs of U93.

4-22. TERMINATING DMA. The last SRQ for an output transfer is called the N+1 SRQ and is transmitted by the device and indicates that the processing of the last word is complete. It is generated when U102 [23D], 74LS74, is set by FIND− after DMAEN+ is no longer asserted. It is gated through U92 [23D], a 74LS27, with the "Q" output of U102 [21D] to ensure that a DMA transfer was just completed and PPDONE via U103 [24E] and U115 [23E] to ensure that adaquate time was allowed to complete a parallel poll, if the Do Parallel Poll bit (bit 1) was set. This signal (ENDEN) is then gated through U72 [21C], a 74S10, to ensure that it was indeed an output operation and that the control word has not requested a freeze on interrupt conditions. U72 pin 8 [21C], a 74S10, presets the flip-flop U112 [21C], a 74S74, causing the N+1 SRQ signal. The last SRQ for an input transfer is generated by FIND− for the last data transfer applied to the C0 and C1 inputs of U93 [22D].

4-23. CONTROL WORD TRANSFER

The card control word provides the HP-IB Interface Card with the configuration information necessary to process data through the PHI Chip and the backplane.

4-24. WRITING THE CONTROL WORD INSTRUCTION: OTA 31

The control word is clocked into U63 [34B] and U85 [24B] by the CLK+ signal generated by U81 pin 6 [21B]. The control word is loaded into the control register U63 [34B], U85 [24B], and U35 [22B]. U63 and U85 are the same register used for the upper eight bits of the word mode transfer as covered in paragraph 4-7. The control register must be used because the BYTE+ bit must be used if a DMA transfer is to be accessed. The lower eight bits of the control word are stored into U35 [22B], a 74LS273, and provide the following functions:

BIT 0 — CARD CLEAR WHEN SET TO A "1"

Bit 0 triggers U61[23A], a 74LS221, the one shot produces the card reset pulse. The output of U61 pin 12 is gated with RST- in U71 [23A], a 74LS00, to provide the card with a universat reset pulse CLR-. This pulse initializes the card without effecting the rest of the system and clears the control register that clears bit 0.

BIT 1 — DO A PARALLEL POLL

When bit 1 is set to a "1", it holds off the generation of the N+1 SRQ signal until U12 and U13 [33E], a 74LS393 and a 74LS00, the 5 us Parallel Poll Timer generates a "0" at U13 pin 8. This circuit counts approximately 23 SCLK+ periods to generate the 5 us delay for PPDONE−. This is the minimum time to ensure a valid response to a parallel poll. PPDONE− is applied to U103 pin 4 [24E].

BIT 2 — INTERRUPT REQUEST ENABLE (IRQEN+)

When bit 2 is set, it allows any of the following interrupting conditions to generate an IRQ− through U114 [22C], a 74LS20, into the I/O Master that sets the device flag (flag 30) and generates an interrupt if the interrupt systen is enabled and control 30 is set. The interrupt conditions are as follows:

a. A bus SRQ (if enabled)
b. A secondary address (if enabled)
c. A PHI Chip interrupt
d. A Group Execute Trigger

BIT 3 — DELAY DMA UNTIL AN INTERRUPT CONDITION EXISTS

When bit 3 is set to a "1", it disables the start-up latch U92 [23D] holding off the start-up of a DMA transfer until one of the four interrupt conditions listed previously exists. Refer to paragraph 4-12 for more details.

BIT 4 — ENABLE SRQ FROM THE BUS

When bit 4 is set to a "1", it enables a bus SRQ to be one of the interrupting conditions discussed in BIT 2. U34 [23C], a 74LS00 gates this bit and BUSRQ+ from the bus receivers to provide the signal SRQINT−.

BIT 5 — NOT USED

BIT 6 — FREEZE DMA

When bit 6 is set to a "1", it allows the interrupt conditions to freeze the DMA transfer wherever the interrupt occurs. This bit is gated through U71 [22C], a 74S00, to disable the N+1 SRQ signal and through U113 [21D], a 74S02, to disable SACK− and DMAEN− to stop DMA in the exact state at which the interrupt occurred.

BIT 7 — ENABLE MY SECONDARY ADDRESS

When bit 7 is set to a "1", it allows the reception of a secondary address to be considered as on of the interrupting conditions discussed in BIT 2. Bit 7 is gated with the "Q" output of the secondary address latch U23 pin 9 [25C], a 74LS74, through U34 [23C], a 74LS00.

Bits 8 through 11 are stored in U85 [24B], a 74LS175, and provide the following functions for DMA byte mode transfers.

BIT 8 — ATTENTION (ATN)

When bit 8 is set to a "1" during an output transfer (bit 15=1), it tags each byte transferred with ATN through U94 [25B] as discussed under the word mode transfer.

When bit 8 is set to a "1" during an input transfer, it asserts the signal LSBYT− into the I/O Master through U104 [23C,24C], a 74S02, if the byte being read from the FIFO is a secondary address.

BIT 9 — END OF RECORD

When bit 9 is set to a "1" during an output transfer, it tags the last byte transferred with EOI indicating an end of record. When gated through U62 [25B], a 74LS02, bit 9 drives the EOI bit through U94 [25B] when DMAEN- goes high during the last byte of the transfer. U62 [24B, 25B], a 74LS02, provides the drive for U94.

When bit 9 is set to a "1" during an input transfer, it allows the end of record detected by the Tag Bit Decoder U105 [26C], a 74S138, to terminate the DMA transfer. These signals are gated through U104 [23C,24C] a 74S02, to assert the signal LSBYT−.

BIT 10 — BYTE MODE

When bit 10 is set to a "1", it indicates that the forthcoming transfer is a byte mode transfer (BYTE+). When bit 10 is set to a "0", it indicates that the forthcoming transfer is a word mode transfer (WORD+).

BIT 11 — FORCED READ

When bit 11 is set to a "1", it enables the FIFO to be flushed by a DMA transfer signal (FORCE−). It modifies the input to U24 [33C], a 74LS27, via U82 [34C], a 74LS00, to indicate that the read is from other than the FIFO.

BITS 12 THROUGH 15

These bits indicate the PHI Chip register that will be referenced by the byte mode transfer. The bits are loaded into U63 [34B], a74LS175, and are discussed in detail in paragraph 4-7.

4-25. READING THE CONTROL WORD INSTRUCTION: LI* 32.

The lower eight bits (bits 0 through 7) are read out of the control register U35 [22B], a 74LS273, by U45 [21B, a 74LS244, and driven onto the Buffered Data Bus during the time that bus control state 6 (BCS6−) is asserted. Bits 8 through 11 of the control word are read from U85 [24B], a 74LS175, by a multiplexer U75 [23B], a 74LS258, and driven onto the Buffered Data Bus by BCS6− (LDCNTRL). The select function of the multiplexer is performed by applying BCS7− to select the input (U75 pin 1). BCS7− is high when the control word is to be loaded, thus selecting the "B" inputs. The output enable signal is the product of U103 (pin 11) [21B], a 74LS00, gating BCS6− or BCS7− that enables U75 to drive bits 8 through 11 onto the Buffered Data Bus whenever status or control is to be loaded. Bits 12 through 15 are stored in U63 [34], a 74LS175, and are read back by U73 [25], another 74LS258, in the same manner as U75 functions. The only difference is the enabling signal to drive bits 12 through 15 onto the Buffered Data Bus. It is a NOR function of BCS5−, BCS6−, and BCS7−.

4-26. STATUS WORD TRANSFER

The status register reflects the present state of the interface and the bus. The status register is cleared by removing the condition which caused the bit to be set. The exception to this is the secondary address bit (bit 12). It requires that the status register be loaded (OT* 32). The state of the other bits in the status register are not effected by this operation, no matter what data pattern is transmitted. The individual meanings of the status bits is defined in paragraph 3-9, Status Register.

4-27. READING THE STATUS REGISTER INSTRUCTION: LI* 32. The status registers U73,U75, and U26 [25B, 23B, and 28B], two 74LS258's and a 74LS244, are enabled onto the data bus by BCS7− (LDSTAT). U73 [25B], drives the upper four bits (bits 12 through 15) of status selected by BCS7− applied to the select input (pin 1) of U73. The next four bits (bits 8 through 11) are driven through U75 [23B], a 74LS258, which also has BCS7− as its select input signal. The lower eight bits (bit 0 through 7) of the status register are the product of the eight switches making up U16, HP-IB Address Select. These eight bits are dirven onto the Buffered Data Bus by U26 [27B], a 74LS244, that is also enabled by BCS7−. The switches are labeled 0 through 7 which corresponds to bits 0 through 7 on the Buffered Data Bus.

4-28. CONCLUSION

Now that the descriptions of the four main functions have been covered, this would be a good time to go back and review them one more time to increase your understanding of their operation and interdependence.

4-29. HP-IB BUS OPERATION

The HP-IB bus interface is accomplished through the PHI Chip, U43 [35B] and the bus transceivers, U21,U31, U41, and U51 [37B,37C, and 37D].

4-30. HP-IB TRANSCEIVER OPERATION

The HP-IB Transceiver's (U21,31,41, and 51) [36 and 37B,C,D] consists of four quad tri-state driver/receiver IC's. The PHI Chip outputs bits DIO1- through DIO8- to U41 and U51 and the eight HP-IB control signals to transceivers U21 and U31. The PHI Chip's output HSE (High State Enable) is applied to U41, U51, and part of U31 It is asserted whenever the DIOn, DAV, or EOI lines are required by the HP-IB system. When HSE inputs are high, they activate an internal pull-up network. The DIOEN output (pin 47) of the PHI Chip is used to drive the S/R inputs of U41 and U51. This output drives the signals out onto the HP-IB lines when it is high and receives the signals off the lines when it is low. The optional pull-up and pull-down resistors, R11 through R14, are to increase

the drive for the HP-IB system lines. Refer to Section II, paragraph 2-18 for further information about these resistors.

The various other HP-IB control line descriptions are covered in Section VII, Figure 7-1, under the descriptions of the PHI Chip (1AA6-6004) and the transceiver (1820-2058).

4-31. PHI CHIP OPTIONS

a. Stabilization Resistor (R15 and R3). The resistor capacitor combination (R15C1) connected to the PHI Chip U43 pin 13 selects the time delay between the assertion of the data on the bus and the assertion of data valid. This switch, U1S2, is normally open providing a 500 nanoseconds settling time. This settling time satisfies the requirements for the IEEE Standard 488-1978. Some peripherasls require a faster settling time of 350 nanoseconds. This speed can be achieved by closing the switch, U1S2, thus connecting R15 and R3.

b. System Controller Select (U1S1). The switch, U1S1 [34D], determines if the card will or will not be the system controller. If the switch is closed, the card will be the system controller. Setting the switch to the closed position puts a "0" on pin 1 (SYS CNTRL) and pulls REN and IFC low.

MAINTENANCE

SECTION V

5-1. INTRODUCTION

This section provides maintenance information for the HP 12009A HP-IB Interface. Included are preventive maintenance instructions and troubleshooting information.

5-2. PREVENTIVE MAINTENANCE

Preventive maintenance for the HP-IB Interface is performed at the same intervals as for the computer system.

CAUTION

STATIC SENSITIVE DEVICES
Use antistatic handling procedures when handling the printed circuit assemblies.

Preventive maintenance consists of inspecting the card for burned or broken components, or the presence of foreign material. The cable and connectors that connect the card to the bus should also be checked for damaged insulation, bent or broken pins, etc. After any damage has been repaired, run the system self-test. (Refer to the HP 1000 L-Series System Installation and Service Manual part no. 02145-90003 or the L-Series Computer Installation and Service Manual, part no. 02103-90003.) If it is determined that the card is malfunctioning, perform the troubleshooting procedures listed in paragraph 5-6.

5-3. REMOVAL AND INSTALLATION PROCEDURES FOR THE I/O PROCESSOR CHIP (U67) AND THE PHI CHIP (U43)

The removal and installion procedures for the two SOS chips used on the HP-IB Interface Card are exactly the same. The only physical difference in the chips is their physical size. The same precautions as to eye hazards and antistatic hazards should be taken in handling both devices.

WARNING

OBSERVE EYE HAZARD SAFETY PRECAUTIONS. Wear safety glasses when removing or installing the retaining clips on the SOS chip sockets.

CAUTION

STATIC SENSITIVE DEVICE
Use antistatic handling procedures while removing or installing the SOS chips.

5-4. REMOVING THE SOS CHIP FROM ITS SOCKET

The chip is removed from the socket in the following manner:

1. With the card removed from the computer, place the card on a flat surface with the component side up.
2. While pressing down on one of the retaining clips with a thumb, insert the flat blade of a screwdriver or similar instrument between the retaining clip and the side of the socket (A) (see Figure 5-1).
3. Twist the bottom portion of the blade away from the socket to free the retaining clip from the bottom edge of the socket (B).
4. When the retaining clip is free, lift it up and over the chip. Keep the clips for use when installing a new chip.
5. Remove the second retaining clip by following steps 2 through 4.
6. Carefully tip the card on edge and remove the chip. Observe the antistaic handling precautions while handling the chip.
7. Do not put retaining clips back on an empty socket as it will distort the socket's contacts.

5-5. INSTALLING THE SOS CHIP IN ITS SOCKET

The chip is installed in the socket in the following manner:

1. Observe all the antistatic handling precautions while handling the chip.
2. Place the HP-IB Interface Card on a flat surface with the component side up.
3. Locate both retaining clips.

4. Place the chip in the socket, locating the two flat corners (C) of the socket facing the two flat corners of the chip (see Figure 5-1). The trace side of the SOS chip package must be on the bottom side when the chip is placed in the socket.

5. Place the retaining clips in the two places provided for them in the side of the socket.

6. Press down with a thumb on the retaining clip and press the retaining clip over the edge of the socket until it snaps under bottom edge of the socket (B).

7. Install the second retaining clip in the same manner, following steps 4 through 6.

5-6. TROUBLESHOOTING

To troubleshoot the HP-IB Interface perform the following steps:

1. Run the computer self-test. Refer to the HP 1000 L-Series Computer Installation and Service Manual, part number 02103-90003, or the HP 1000 L-Series Computer System Installation and Service Manual, part no. 02145-90003.

2. Run the kernel diagnostic. Refer to the Kernal Diagnostic Operating Manual, part no. 24397-90002.

3. Run the HP-IB interface diagnostic. Refer to the HP-IB Interface Diagnostic Operating Manual, part no. 24397-90009.

4. If the interface is defective, contact the nearest Hewlett-Packard Sales and Service Office for information on repair or replacement of the interface card. The Sales and Service Offices are listed in the back of this manual.

5. Further isolation to a defective component may be performed, if necessary, using an oscilloscope or logic analyzer. Refer to Section VII, Figure 7-1 for integrated circuit pin connections and logic functions, to Figure 7-2 for a functional block diagram, to Figure 7-3 for a component location diagram, and to Figure 7-4 for the schematic logic diagram. Refer to Section VI, Table 6-3 for replaceable parts information.

Refer to Section II, Table 2-1 for Interface to HP-IB cable connections.

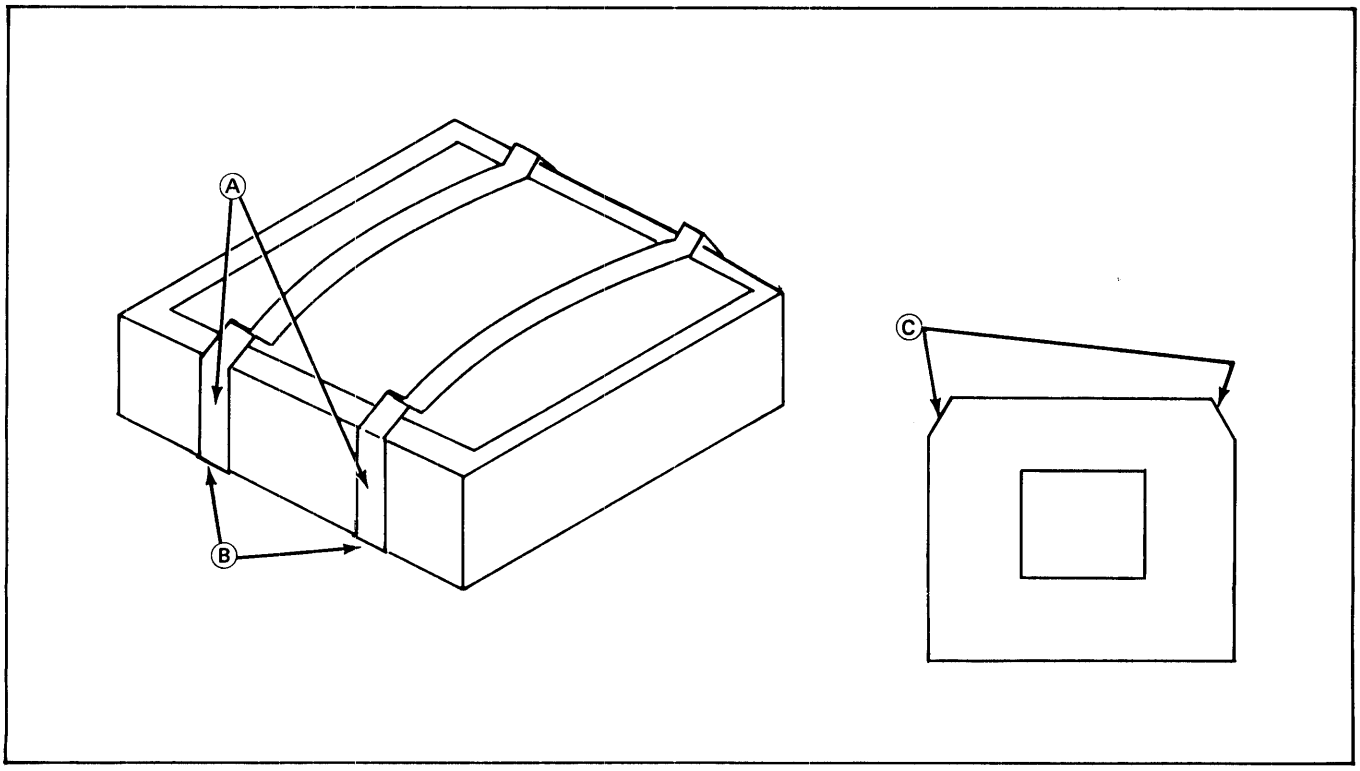


Figure 5-1. SOS Socket with Chip and Retaining Clips

REPLACEABLE PARTS

SECTION VI

6-1. INTRODUCTION

This section contains information for ordering replaceable parts for the HP 12009A HP-IB Interface. Table 6-1 is a list of exchange board part numbers, Table 6-2 lists the meanings of the reference designations and abbreviations used in Table 6-3, Table 6-3 is the list of replaceable parts, and Table 6-4 contains the names and addresses of manufacturers of the parts.

Table 6-1. Exchange Board Part Numbers

EXCHANGE CARD WITHOUT IOP CHIP (U67)	NEW CARD WITH IOP CHIP
12009-69001	12009-60001

6-2. REPLACEABLE PARTS

Table 6-3 contains the list of parts in reference designation order. The following information is listed for each part:

a. Reference designation of the part. Refer to Table 6-2 for an explanation of the abbreviations used in the "Reference Designation" column.

b. The Hewlett-Packard part number.

c. Part number check digit (CD).

d. Total quantity (QTY).

e. Description of the part.

f. A five-digit manufacturer's code number of a typical manufacturer of the part.

g. The manufacturer's part number.

6-3. ORDERING INFORMATION

To order replacement parts or to obtain information on parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Service Office (a list of Sales and Service Offices is given in the back of this manual).

To order a part listed in the replaceable parts list, give the Hewlett-Packard part number with the check digit, and indicate the quanity required. The check digit will ensure accurate and timely processing of the order.

To order a part that is not listed in the replaceable parts list, specify the following information:

a. Indentification of the product containing the part (refer to Section I, paragraph 1-4).

b. Description and function of the part.

c. Quantity required.

Table 6-2. Reference Designations and Abbreviations

REFERENCE DESIGNATIONS

A	= assembly	K	= relay	TB	= terminal board
B	= motor, synchro	L	= inductor	TP	= test point
BT	= battery	M	= meter	U	= integrated circuit, non-repairable assembly
C	= capacitor	P	= plug connector	V	= vacuum tube, photocell, etc.
CB	= circuit breaker	Q	= semiconductor device other than diode or integrated circuit	VR	= voltage regulator
CR	= diode	R	= resistor	W	= jumper wire
DL	= delay line	RT	= thermistor	X	= socket
DS	= indicator	S	= switch	Y	= crystal
E	= Misc electrical parts	T	= transformer	Z	= tuned cavity, network
F	= fuse				
FL	= filter				
J	= receptacle connector				

ABBREVIATIONS

A	= amperes	gra	= gray	PCA	= printed-circuit assembly
ac	= alternating current	grn	= green	PWB	= printed-wiring board
Ag	= silver			phh	= phillips head
Al	= aluminum	H	= henries	pk	= peak
ar	= as required	Hg	= mercury	p-p	= peak-to-peak
adj	= adjust	hr	= hour(s)	pt	= point
assy	= assembly	Hz	= hertz	prv	= peak inverse voltage
		hdw	= hardware	PNP	= positive-negative-positive
b	= base	hex	= hexagon, hexagonal	pwv	= peak working voltage
bp	= bandpass			porc	= porcelain
bpi	= bits per inch	ID	= inside diameter	posn	= position(s)
blk	= black	IF	= intermediate frequency	pozi	= pozidrive
blu	= blue	in.	= inch, inches		
brn	= brown	I/O	= input/output	rf	= radio frequency
brs	= brass	int	= internal	rdh	= round head
Btu	= British thermal unit	incl	= include(s)	rms	= root-mean-square
Be Cu	= beryllium copper	insul	= insulation, insulated	rwv	= reverse working voltage
		impgrg	= impregnated	rect	= rectifier
cpi	= characters per inch	incand	= incandescent	r/min	= revolutions per minute
coll	= collector	ips	= inches per second	RTL	= resistor-transistor logic
cw	= clockwise				
ccw	= counterclockwise	k	= kilo (10^3), kilohm	s	= second
cer	= ceramic			SB, TT	= slow blow
com	= common	lp	= low pass	Se	= selenium
crt	= cathode-ray tube			Si	= silicon
CTL	= complementary-transistor logic	m	= milli (10^{-3})	scr	= silicon controlled rectifier
		M	= mega (10^6), megohm	sst	= stainless steel
cath	= cathode	My	= Mylar	stl	= steel
Cd pl	= cadmium plate	mfr	= manufacturer	spcl	= special
comp	= composition	mom	= momentary	spdt	= single-pole, double-throw
conn	= connector	mtg	= mounting	spst	= single-pole, single-throw
compl	= complete	misc	= miscellaneous		
		met. ox.	= metal oxide		
dc	= direct current	mintr	= miniature		
dr	= drive			Ta	= tantalum
DTL	= diode-transistor logic	n	= nano (10^{-9})	td	= time delay
depc	= deposited carbon	nc	= normally closed or no connection	Ti	= titanium
dpdt	= double-pole, double-throw			tgl	= toggle
dpst	= double-pole, single-throw	Ne	= neon	thd	= thread
		no.	= number	tol	= tolerance
em	= emitter	n.o.	= normally open	TTL	= transistor transistor logic
ECL	= emitter-coupled logic	np	= nickel plated		
ext	= external	NPN	= negative-positive-negative		
encap	= encapsulated	NPO	= negative-positive zero (zero temperature coefficient)	U(μ)	= micro (10^{-6})
elctlt	= electrolytic	NSR	= not separately replaceable		
		NRFR	= not recommended for field replacement	V	= volt(s)
F	= farads			var	= variable
FF	= flip-flop			vio	= violet
flh	= flat head	OD	= outside diameter	Vdcw	= direct current working volts
flm	= film	OBD	= order by description		
fxd	= fixed	orn	= orange	W	= watts
filh	= fillister head	ovh	= oval head	ww	= wirewound
		oxd	= oxide	wht	= white
G	= giga (10^9)			WIV	= working inverse voltage
Ge	= germanium	p	= pico (10^{-12})		
gl	= glass	PC	= printed circuit	yel	= yellow
gnd	= ground(ed)				

Table 6-3. Replaceable Parts

Reference Designation	HP Part Number	CD	Qty	Description	Mfr Code	Mfr Part Number
	12009A	2		HP-IB INTERFACE	28480	12009A
	12009-60001	7	1	ASSEMBLY-HP-IB	28480	12009-60001
C1	0160-4832	4	1	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0160-4801	7	2	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C3	0160-4801	7		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C4	0160-4808	4	1	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
E1	0360-1682	0	3	TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E2	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
E3	0360-1682	0		TERMINAL-STUD SGL-TUR PRESS-MTG	28480	0360-1682
R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	1810-0280	8	3	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R3	0757-0459	8	1	RESISTOR 56.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-5622-F
R4	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R5	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R6	0698-3155	1	2	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R7	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R8	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
R9	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
R10	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R11♦	1810-0270	6	2	NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
R12♦	1810-0272	8	2	NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
R13♦	1810-0270	6		NETWORK-RES 10-SIP680.0 OHM X 9	01121	210A681
R14♦	1810-0272	8		NETWORK-RES 10-SIP330.0 OHM X 9	01121	210A331
R15	0698-3159	5	1	RESISTOR 26.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2612-F
R16	1810-0280	8		NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
U1	3101-2243	6	2	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U12	1820-2096	5	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393N
U13	1820-1197	9	5	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U14	1820-1445	0	1	IC LCH TTL LS 4-BIT	01295	SN74LS375N
U16	3101-2243	6		SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U1A	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U21	1820-2058	3	4	IC MISC TTL S QUAD	28480	1820-2058
U22	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U23	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U24	1820-1206	1	2	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U25	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U26	1820-2024	3	7	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U27	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U31	1820-2058	3		IC MISC TTL S QUAD	28480	1820-2058
U34	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U35	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U36	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-2102	8	8	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U3A	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U41	1820-2058	3		IC MISC TTL S QUAD	28480	1820-2058
U43	1AA6-6004	0	1	PHI 279 EEE	28480	1AA6-6004
U44	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U45	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U46	1820-1240	3	2	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U51	1820-2058	3		IC MISC TTL S QUAD	28480	1820-2058
U54	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U55	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U56	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U57	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U58	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U61	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U62	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U63	1820-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U64	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U65	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U66	1820-1322	2	5	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U67	1AF5-6001	7	1	I/O PROCESSOR (IOP)CHIP	28480	1AF5-6001
U71	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U72	1820-0685	6	2	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U73	1820-1439	2	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN
U74	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U75	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258AN

See introduction to this section for ordering information
*Indicates factory selected value
♦ Indicates usage is optional, see Section II, paragraph 2-1

Table 6-3. Replaceable Parts (Continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U76	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U81	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
U82	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U83	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U84	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U85	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U86	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U91	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U92	1820-1206	1		IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U93	1820-0998	6	1	IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN74S153N
U94	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U95	1820-1077	4	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U96	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U101	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U102	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U103	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U104	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U105	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U106	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U107	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U112	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U113	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U114	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U115	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U116	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U117	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U119	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
				MISCELLANEOUS PARTS		
	0403-0289	3	3	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1200-0639	8	2	SOCKET-IC 20-CONT DIP-SLDR	28480	1200-0639
	1200-0844C	9	2	RET SPRING CLIP	28480	1200-0844C
	1200-0845C	0	2	RET SPRING CLIP	28480	1200-0845C
	1200-0847C	2	1	SOCKET-48-PIN (U43)	28480	1200-0847C
	1200-0848C	3	1	SOCKET-64-PIN (U67)	28480	1200-0848C
	1480-0116	8	2	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116
	12009-60002	8	1	ASSEMBLY, CABLE 2M HP-IB	28480	12009-60002
				MISCELLANEOUS PARTS		
	0624-0098	0	2	SCREW-TPG 4-40 .438-IN-LG PAN-HD-POZI	28480	0624-0098
	0890-0291	8		TUBING-HS .375-D/.187-RCVD .025-WALL	00000	ORDER BY DESCRIPTION
	1251-0159	4	1	CONNECTOR-PC EDGE 15-CONT/ROW 2-ROWS	28480	1251-0159
	1600-0863	8	1	GROUNDING SPRING	28480	1600-0863
	2200-0091	7	1	SCREW-MACH 4-40 .562-IN-LG PAN-HD-POZI	00000	ORDER BY DESCRIPTION
	2260-0002	6	1	NUT-HEX-DBL-CHAM 4-40-THD .062-IN-THK	00000	ORDER BY DESCRIPTION
	3030-0143	0	1	SCREW-SET 6-32 .5-IN-LG SMALL CUP-PT ALY	00000	ORDER BY DESCRIPTION
	8120-1835	5		CABLE ASSY 24AWG 24-CNDCT JGK-JKT	28480	8120-1835
	5040-6004	7	1	CLAMP-CABLE-SMALL	28480	5040-6004
	5040-6072	9	1	MOUNTING BLOCK	28480	5040-6072
	5040-6086	5	1	HOOD, CONNECTOR	28480	5040-6086

See introduction to this section for ordering information
*Indicates factory selected value

Table 6-4. Manufacturer's Code List

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements.

CODE NO.	MANUFACTURER	ADDRESS
00000	Any Satisfactory Supplier	
01121	Allen-Bradley Co.	Milwaukee, WI 53204
01295	Texas Instr Inc. Semiconductor CMPNT Div	Dallas, TX 75222
07263	Fairchild Semiconductor Div.	Mt. View, CA 94042
24546	Corning Glass Works (Bradford)	Bradford, PA 16701
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA 94304

SERVICE DIAGRAMS

SECTION VII

7-1. INTRODUCTION

This section contains the service diagrams for the HP-IB Interface Card. Base diagrams of the integrated circuits used on this card are shown in Figure 7-1. A component location diagram is shown in Figure 7-3. A list of diagrams to be found in this section is given below:

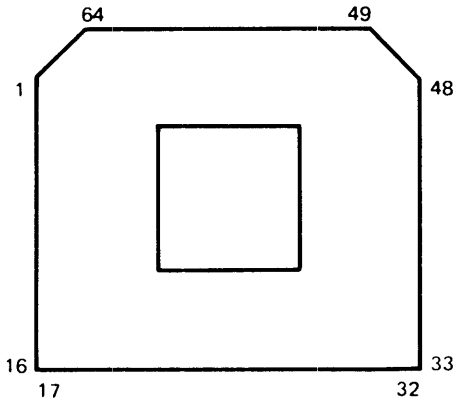
Figure 7-1. Integrated Circuit Base Diagrams

Figure 7-2. HP-IB Interface Functional Block Diagram

Figure 7-3. HP 12009A HP-IB Interface Card Component Location Diagram

Figure 7-4. HP 12009-60001 HP-IB Interface Card Schematic Logic Diagram

IAF5-6001
U67

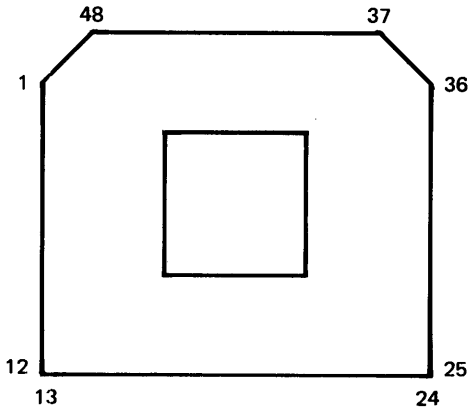


1AF5-6001 I/O PROCESSOR (IOP) CHIP OUTLINE (COMPONENT SIDE)

PIN DEFINITIONS

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
1	DMACYC–	17	GND	33	BRNI+	49	VCC
2	LDMAR+	18	VDD	34	CRS +	50	GND
3	SCEN–	19	CW1 –	35	IEN –	51	VDD
4	REMOTE–	20	BCW2 +	36	DIAG –	52	CB7 +
5	INTCYC +	21	BCW1 +	37	DVCMD –	53	CB8 +
6	DMAEN –	22	BCW0 +	38	PLSLV+	54	CB9 +
7	LOBYT –	23	BVALID+	39	PON +	55	CB10 +
8	SACK –	24	BIOGO+	40	SLACK +	56	CB11 +
9	NC	25	ICHID–	41	SLRQ+	57	CB12 +
10	SCLK +	26	BIAK+	42	CB0 +	58	CB13 +
11	LSBYT –	27	CFF–	43	CB1 +	59	CB14 +
12	BPE+	28	PULIOR–	44	CB2 +	60	CB15 +
13	BMP–	29	IOEN –	45	CB3 +	61	MEMGO+
14	CHSRQ–	30	IOCLK +	46	CB4 +	62	MRQ +
15	IRQ –	31	PRDIS –	47	CB5 +	63	NC
16	VCC	32	GND	48	CB6 +	64	GND

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 1 of 9)



1 AA6-6004 PHI CHIP OUTLINE (COMPONENT SIDE)

PIN	SIGNAL	NAME	DESCRIPTION
1	SYS CNTRL	System Controller	When asserted, this signal provides the PHI Chip with System Controller capabilities as defined by the HP-IB standard. It can drive the HP-IB's IFC and REN lines. Only one device in any system should have this pin asserted.
2	DAV–	Data Valid	This bidirectional pin ties to the HP-IB DAV line via a transceiver.
3	EOI–	End or Identify	This bidirectional pin ties to the HP-IB EOI line via a transceiver.
4-11	DIO8– thru DIO1–	Data I/O Bit 8 through Bit 1	These bidirectional pins tie to the HP-IB DIO lines via eight transceivers.
12	VDD	Power Supply Pin	This pin supplies VDD (+12V) to the PHI Chip.
13	STAB	Delay Stabilizing Resistor	This pin should be tied through a resistor to a ground point located as close as possible to pin 36. Also, it should be tied through at least a 0.01 μF capacitor to a VDD point located as close as possible to pin 13. Refer to Section II for a description of the use of this resistor.
14	DMARQ–	DMA Request	This signal can be used to request DMA cycles to transfer data to the Outbound FIFO or from the Inbound FIFO depending on the value of the DMA FIFO Select bit in Register 6.
15	PON	Power-On (Initialize)	Whenever this signal is brought low, it initializes all circuits within the PHI Chip. It must be held low for at least 500 ns.
16	WRITE	Write	When this signal is asserted, it specifies that a Register Write rather than a Register Read is being performed by the host processor.
17	INT–	Interrupt	This signal, which is independent of chip select, should be used to cause a host processor interrupt whenever it is asserted.

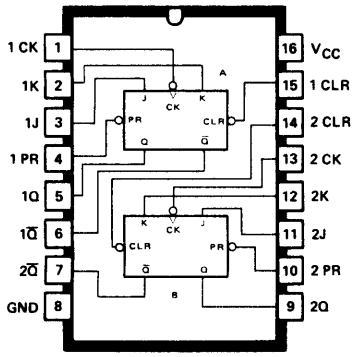
Figure 7-1. Integrated Circuit Base Diagrams (Sheet 2 of 9)

PIN	SIGNAL	NAME	DESCRIPTION
18	IOEND–	I/O End	This signal is used to handshake all PHI Register Reads and Writes by a host processor within an asynchronous system. It can be ignored within a synchronous system.
19	IOGO–	I/O Go	This signal is used to cause a read from or a write to a specified register within the PHI Chip.
20-22	A15-A13	Address Bit 15 through Bit 13	These input signals are used to specify the number of a register being read from or written into. A13 is the high-order bit.
23	CHIP SELECT–	Chip Select	When this input signal is asserted, it allows the PHI Chip to respond to Register Read or Write cycles initiated by the host processor's IOGO-line.
24	VDC	Power Supply Pin	This pin should be tied to the VCC pin when the PHI Chip is interfacing to a LS TTL compatible I/O system.
25-31	D0-D15	Processor Data Bits D0, D1, and D8 through D15	These bidirectional pins carry data during reads from and writes to the PHI Chip by the host processor.
35	RTL	Return to Local	This input signal carries the "rtl" message for the REMOTE/LOCAL interface function as defined in the IEEE Standard 488-1978. Within devices utilizing this function, it should be tied to a pushbutton switch. Within all others, it should be tied low.
36	GND	Ground	This pin supplies the ground reference for all three power supply pins.
37	TRIG	Trigger	This output signal is asserted with a minimum 60 ns pulse any time the device containing the PHI Chip is triggered via the HP-IB's Group-Execute-Trigger Interface Command. The maximum assertion time is equal to the assertion time of DAV–.
38	ATN–	Attention	This bidirectional pin ties to the HP-IB ATN line via a transceiver.
39	SRQ–	Service Request	This bidirectional pin ties to the HP-IB SRQ line via a transceiver.
40	RFD	Ready For Data	This bidirectional pin ties to the HP-IB NRFD line via a transceiver.
41	DAC	Data Accepted	This bidirectional pin ties to the HP-IB NDAC line via a transceiver.
42	REN–	Remote Enable	This bidirectional pin ties to the HP-IB REN line via a transceiver.
43	IFC–	Interface Clear	This bidirectional pin ties to the HP-IB IFC line via a transceiver.
44	CIC	Controller in Charge	This output signal is asserted when the device containing the PHI Chip is the current HP-IB Controller. It is used to enable the ATN line when true, and to enable the SRQ line when false.
45	HSE	High State Enable	This output signal is asserted whenever the DIOn, DAV, or EOI lines are required by the HP-IB to have active, rather than passive, pullups. It should be tied to the high-state enable pins of the appropriate transceivers.
46	DAV/ EOI EN	DAV/EOI Enable	This output signal is asserted whenever the device containing the PHI Chip is supposed to drive either the DAV or EOI line. It is used to enable the corresponding line drivers when true.
47	DIOE	DIO Enable	This output signal is asserted whenever the device containing the PHI Chip is supposed to drive one or more of the DIOn lines. It is used to enable the DIOn line drivers when true.
48	VCC	Power Supply Pin	This pin supplies +5V to the PHI Chip.

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 3 of 9)

1820-0629
U56,86

Dual J-K Negative-Edge-Triggered Flip-Flops with Preset and Clear



FUNCTION TABLE

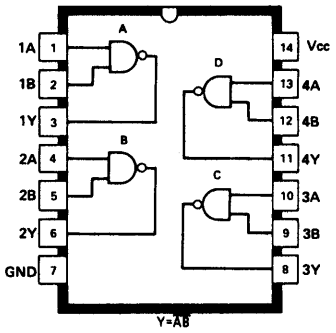
INPUTS					OUTPUTS	
PRESENT	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

*Non-stable condition exists only while both preset and clear inputs are low.

1820-0681
U71,76,106

1820-1197
U13,34,82,84,103

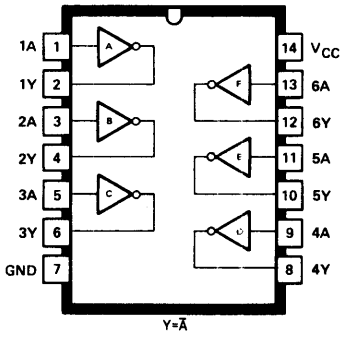
Quadruple 2-Input Positive-NAND Gates



1820-0683
U83,111

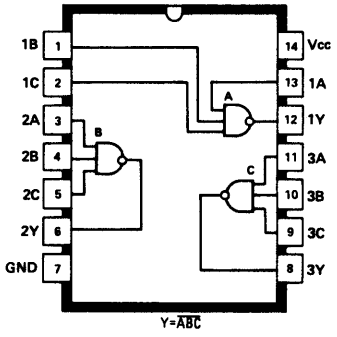
1820-1199
U22,115

Hex Inverters



1820-0685
U72,101

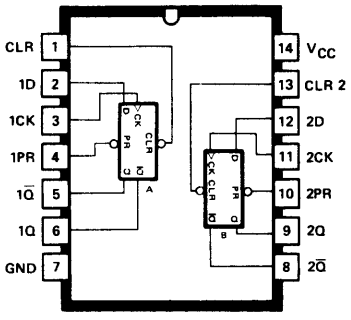
Triple 3-Input Positive-NAND Gates



1820-0693
U112

1820-1112
U25,102

Dual D-Type Positive-Edge-Triggered Flip-Flops with Preset and Clear



FUNCTION TABLE

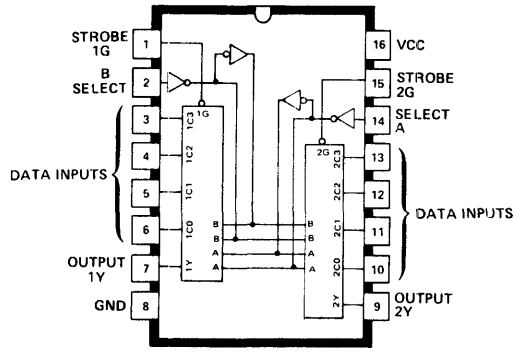
INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

*Non-stable condition exists only while both preset and clear inputs are low.

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 4 of 9)

1820-0998
U93

Dual 4-Line to 1-Line
Data Selectors/Multiplexers



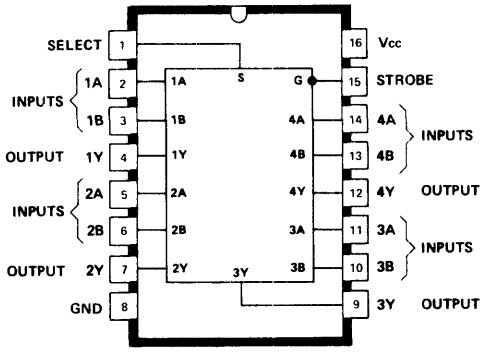
FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Select inputs A and B are common to both sections.
H = high level
L = low level
X = irrelevant

1820-1077
U95

Quad 2- to 1-Line Data Selectors/Multiplexers
Noninverted Data Outputs



FUNCTION TABLE

INPUTS				OUTPUT Y
STROBE	SELECT	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

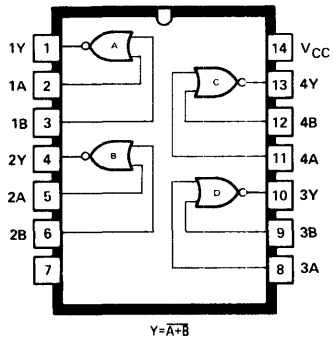
H = high level
L = low level
X = irrelevant

1820-1112
U25,102
(See 1820-0693)

1820-1144
U23,62

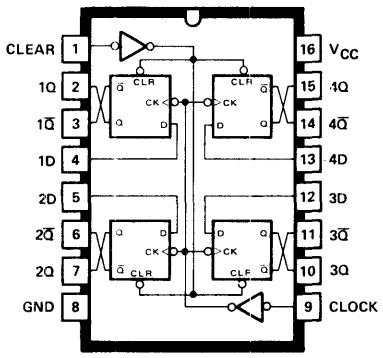
1820-1322
U66,91,104,113,117

Dual 4-Input
Positive-NOR Gates



1820-1195
U63,85

Quad D-Type Flip-Flops
Complementary Outputs
Common Direct Clear



FUNCTION TABLE
(Each Flip-Flop)

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	Q̄
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady state input conditions were established

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 5 of 9)

1820-1197

U13,34,82,84,103
(See 1820-0681)

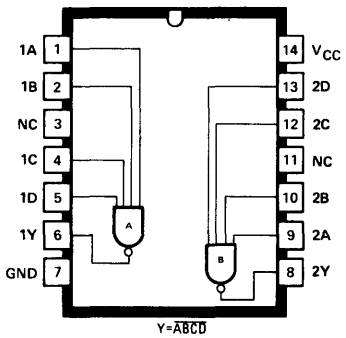
1820-1199

U22,115
(See 1820-0683)

1820-1204

U114

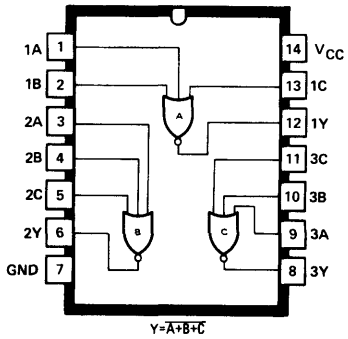
Dual 4-Input
Positive-NAND Gates



1820-1206

U24,92

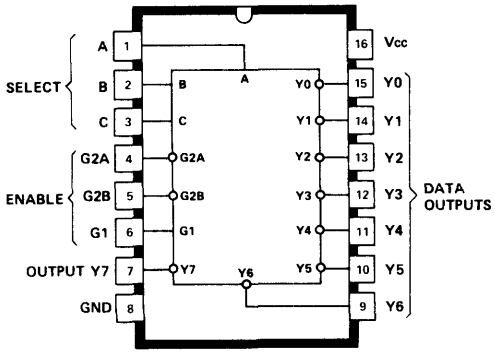
Triple 3-Input
Positive-NOR Gates



1820-1240

U46,105

3 To 8 Line Decoders/Multipilexers



FUNCTION TABLE

INPUTS					OUTPUTS							
ENABLE		SELECT										
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

*G2 = G2A + G2B
H = high level
L = low level
X = irrelevant

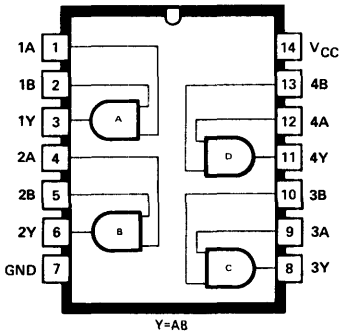
1820-1322

U66,91,104,113,117
(See 1820-1144)

1820-1367

U36

Quadruple 2-Input
Positive-AND Gates



1820-1425

U81

Quadruple 2-Input Positive-NAND
Schmitt Triggers

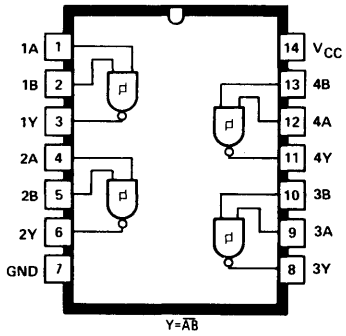
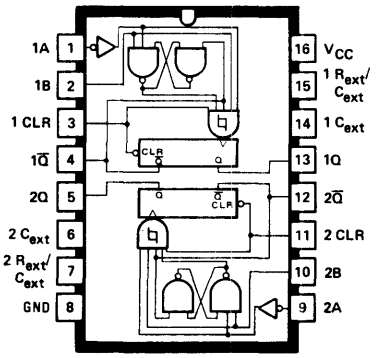


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 6 of 9)

1820-1437
U61
Dual Monostable Multivibrators

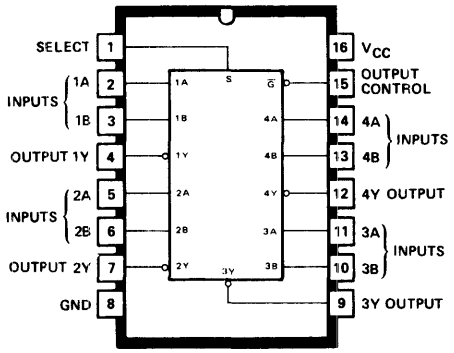


FUNCTION TABLE
(Each Monostable)

INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Also see description and switching characteristics

1820-1439
U73,75
Quad Data Selectors/Multiplexers
Inverted 3-State Outputs

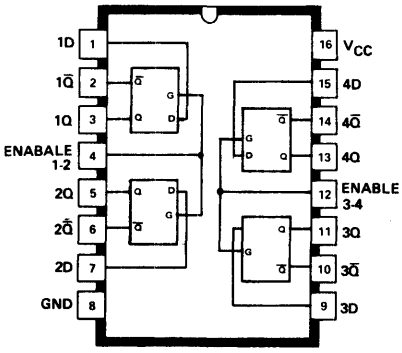


FUNCTION TABLE

INPUTS				OUTPUT Y
OUTPUT CONTROL	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

1820-1445
U14
4-Bit Bistable Latches

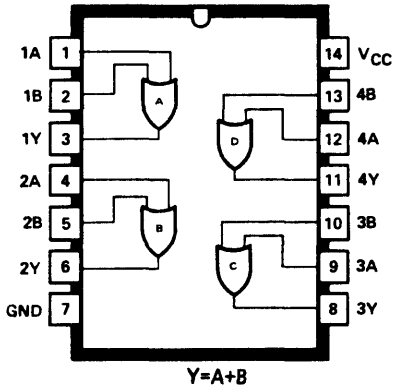


FUNCTION TABLE
(EACH LATCH)

INPUTS		OUTPUTS	
D	G	Q	Q̄
L	H	L	H
H	H	H	L
X	L	Q_0	$\bar{Q}_0$

H = high level
L = low level,
X = irrelevant
Q0 = the level of Q before the high-to-low transition of G.

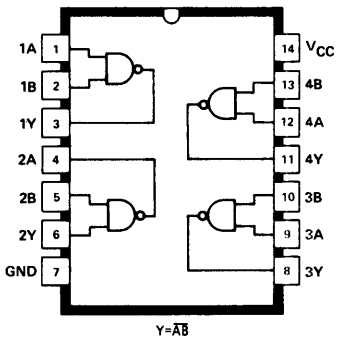
1820-1449
U107
Quad 2-Input
Positive-OR Gates



Y=A+B

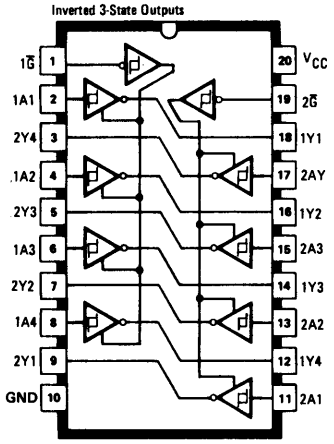
Figure 7-1. Integrated Circuit Base Diagrams (Sheet 7 of 9)

1820-1451
U96,118
Quadruple 2-Input
Positive-NAND Buffers
With Open-Collector Outputs

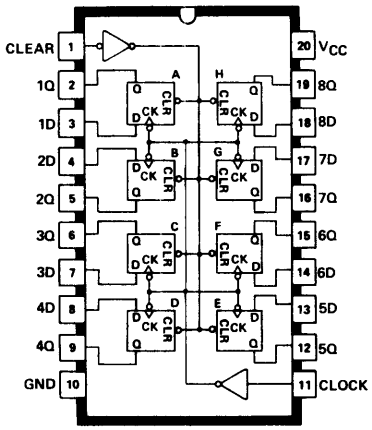


Y=$\overline{AB}$

1820-1633
U108,116
Octal Buffers/Line Drivers/Line Receivers
Inverted 3-State Outputs



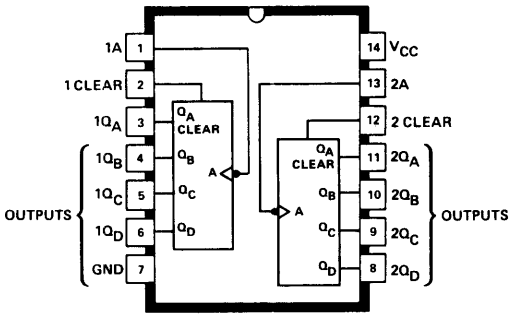
1820-1730
U35
Octal D-Type Flip-Flops
Common Clock
Single-Rail Outputs



FUNCTION TABLE
(Each Flip-Flop)

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

1820-1989
U12
Dual 4-Bit Binary Counters

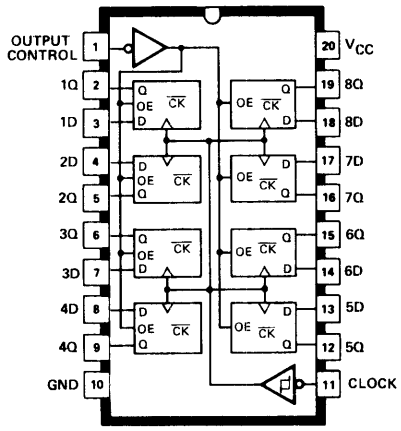


COUNT SEQUENCE
(Each Counter)

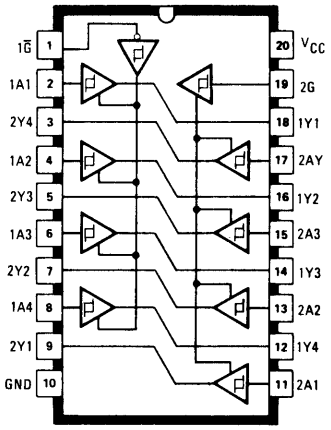
COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 8 of 9)

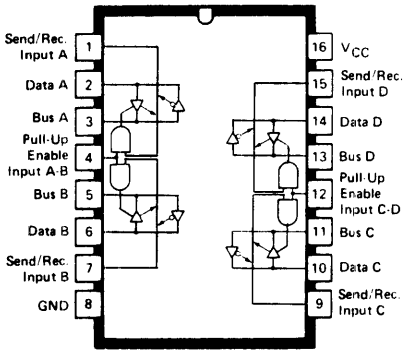
1820-1997
U18
Octal D-Type Flip-Flops
Common Output Control
Common Clock



1820-2024
U26,27,28,45,47,48,94
Octal Buffers/Line Drivers/Line Receivers
Non inverted 3-State Outputs



1820-2058
U21,31,41,51
Quad 3-State Bus Transceiver
with Termination Networks

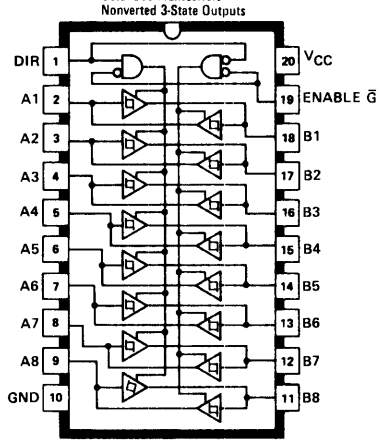


TRUTH TABLE

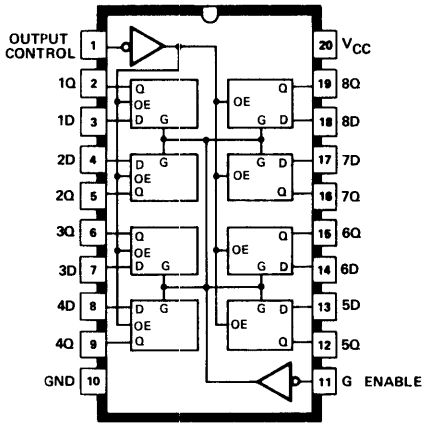
SEND/REC.	ENABLE	INFO. FLOW	COMMENTS
0	X	BUS → DATA	–
1	1	DATA → BUS	ACTIVE PULL UP
1	0	DATA → BUS	OPEN COL.

X = DON'T CARE

1820-2075
U55,65
Octal Bus Transceivers
Nonverted 3-State Outputs



1820-2102
U37,38,44,54,57,58,64,74
Octal D-Type Latches
3-State Outputs
Common Output Control
Common Enable



FUNCTION TABLE

OUTPUT CONTROL	ENABLE G	D	OUTPUT
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 9 of 9)

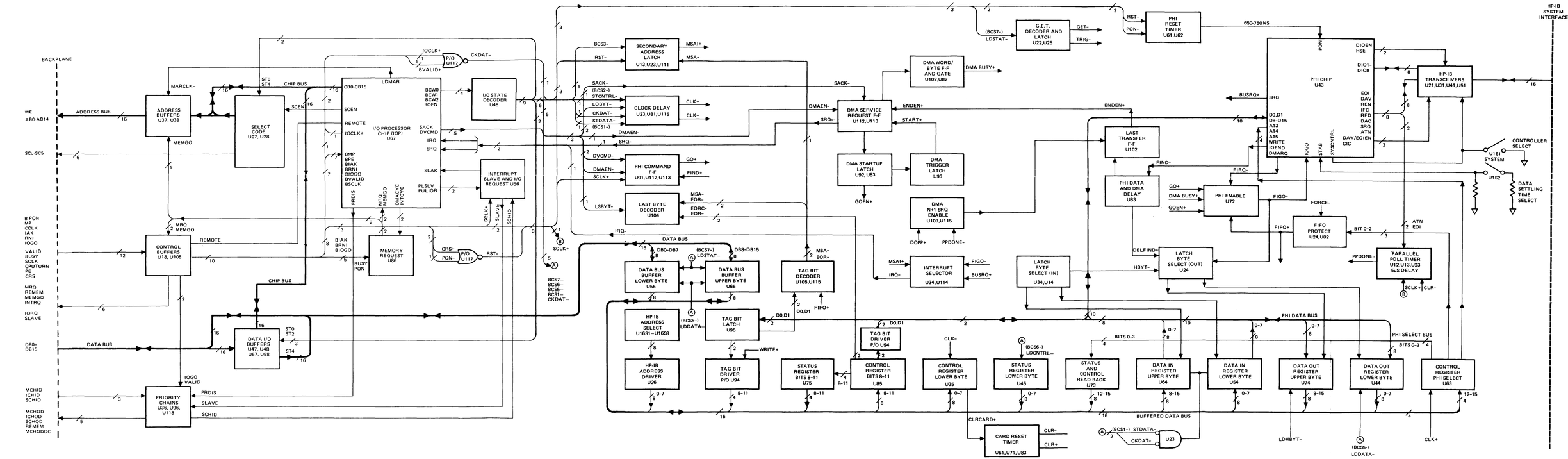


Figure 7-2. HP-IB Interface Functional Block Diagram

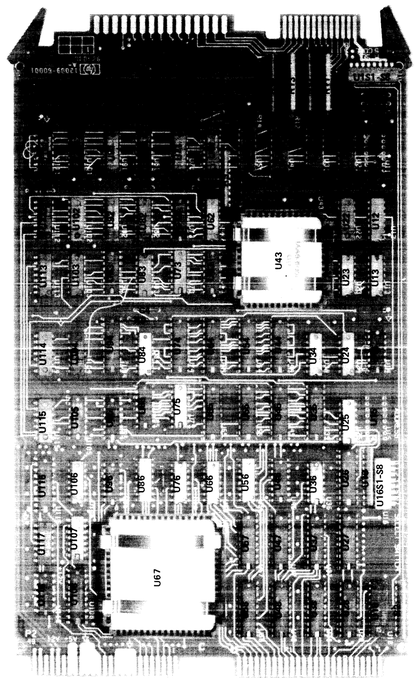


Figure 7-3. HP 12009A HP-IB Interface Card Component Location Diagram

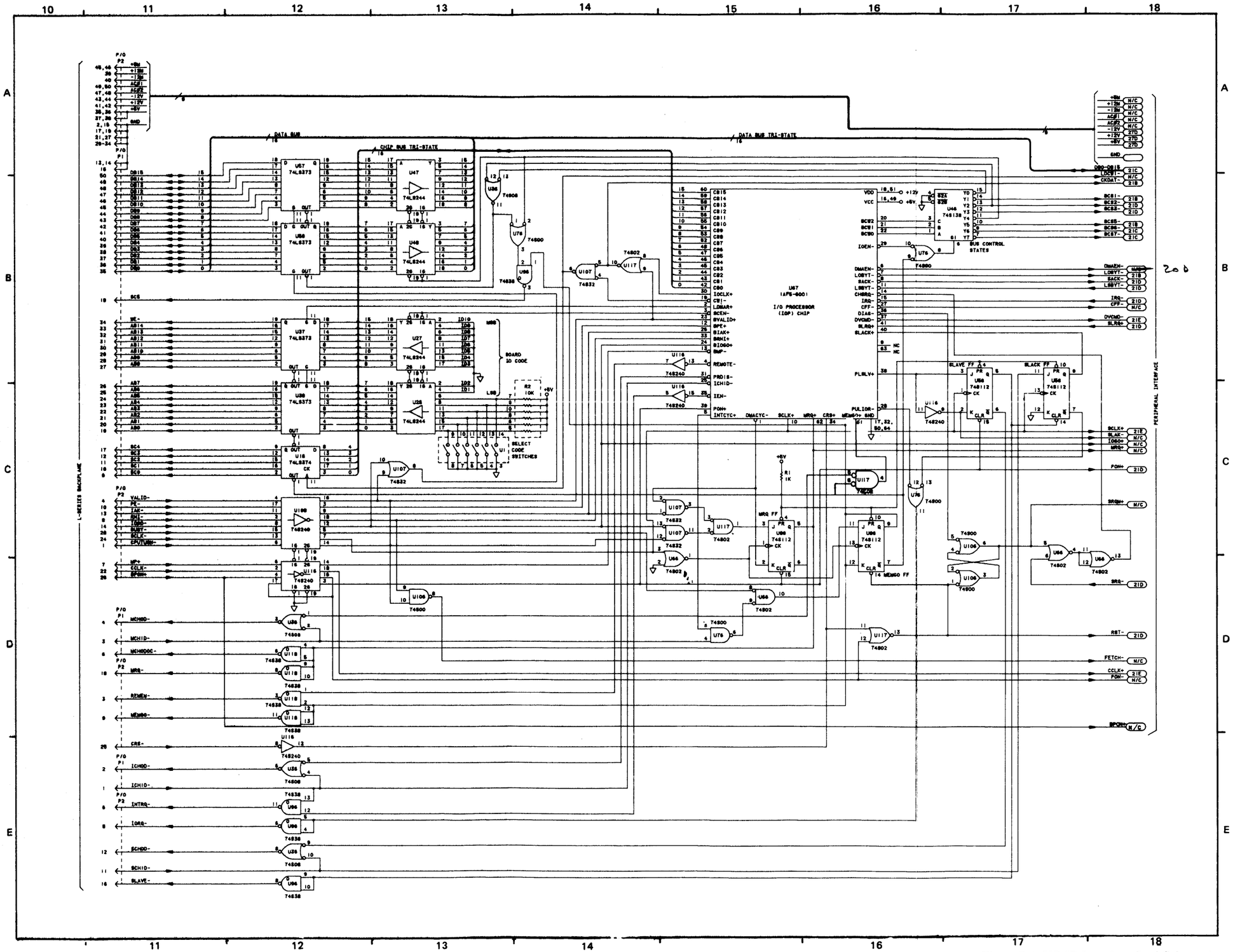


Figure 7-4. HP-IB Interface Card Schematic Logic Diagram (Sheet 1 of 3)

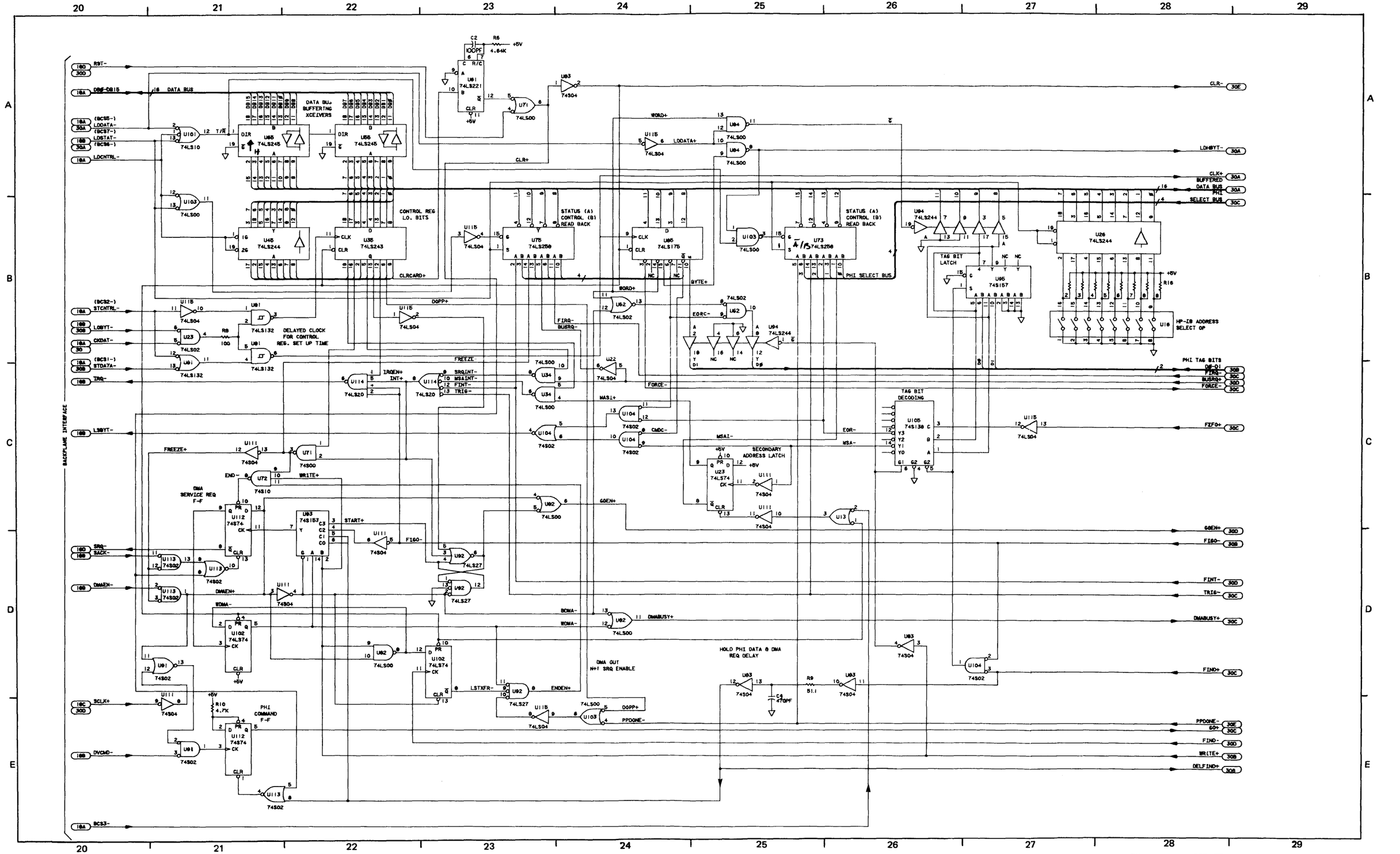


Figure 7-4. HP-IB Interface Card Schematic Logic Diagram (Sheet 2 of 3)

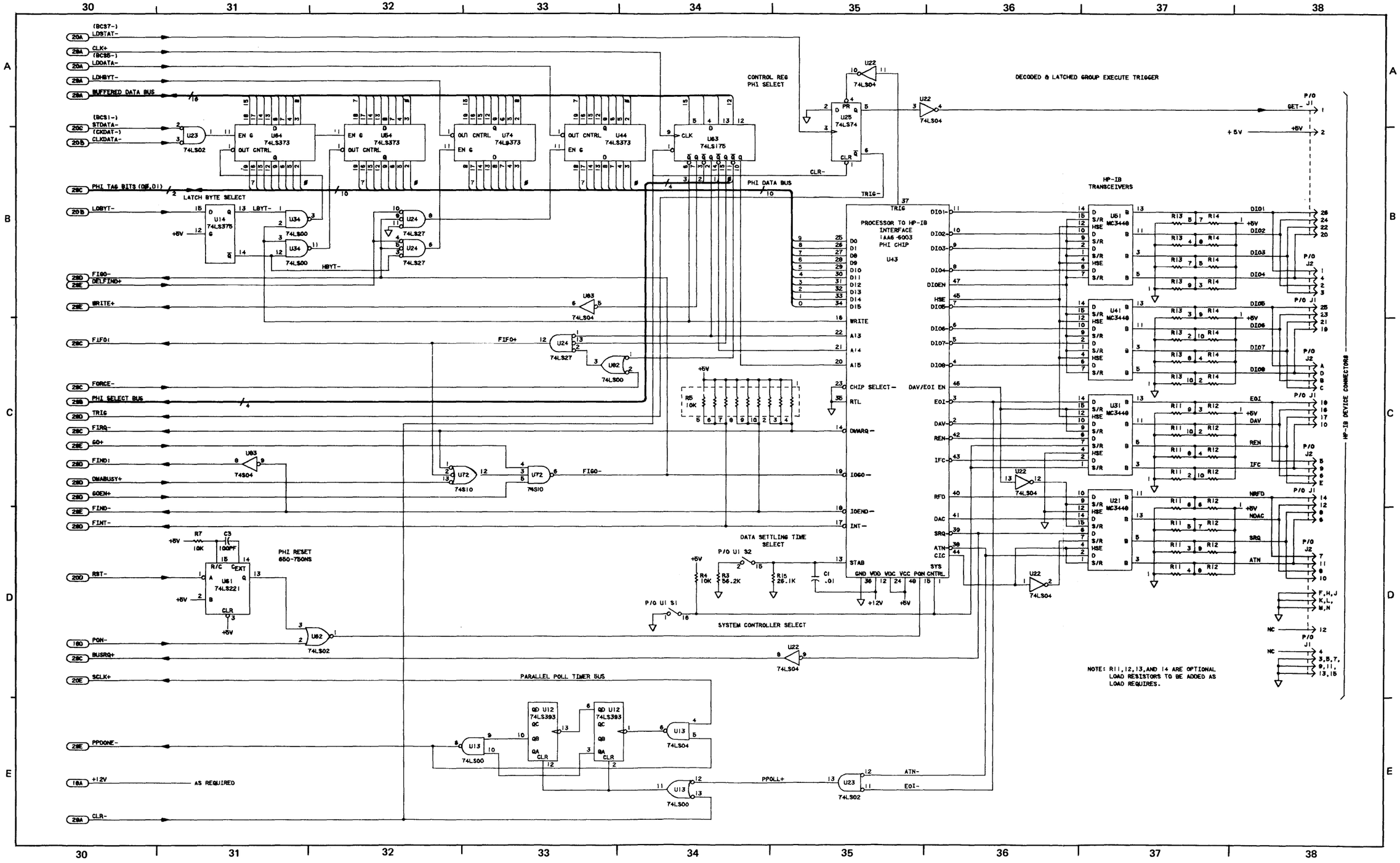


Figure 7-4. HP-IB Interface Card Schematic Logic Diagram (Sheet 3 of 3)

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