HP 1000 A-Series Computer Systems

HP 12009A
HP-IB Interface

Reference Manual

Hewlett-Packard Company
Roseville Networks Division
8000 Foothills Boulevard
Roseville, California 95678

Manual Part Number: 12009-90001
E1288
Printed in U.S.A.
December 1988

Printing History

New editions are complete revisions of the manual. Update packages, which are issued between editions, contain additional and replacement pages to be merged into the manual by the customer. The dates on the title page change only when a new edition or a new update is published. No information is incorporated into a reprinting unless it appears as a prior update; the edition does not change when an update is incorporated.

A software code may be printed before the date; this indicates the version level of the software product at the time the manual or update was issued. Many product updates and fixes do not require manual changes and, conversely, manual corrections may be done without accompanying product changes. Therefore, do not expect a one-to-one correspondence between product updates and manual updates.

Edition 1 . . . . . January 1980
Edition 2 . . . . . July 1984
Edition 3 . . . . . December 1988

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Safety Considerations

General

This product and related documentation must be reviewed for familiarization with safety markings before operation.

Safety Symbols

Instruction manual symbol: the product will be marked with this symbol when it is necessary for the user to refer to the instruction manual in order to protect the product against damage.

Indicates hazardous voltages.

Indicates earth (ground) terminal. This symbol is sometimes used in the manual to indicate circuit common connected to a grounded chassis.

Warning

The warning sign denotes a hazard. It calls attention to a procedure, practice, or the like, which, if not correctly performed or adhered to, could result in injury. Do not proceed beyond a warning sign until the indicated conditions are fully understood and met.

Caution

The caution sign denotes a hazard. It calls attention to an operating procedure, practice, or the like, which, if not correctly performed or adhered to, could result in damage to or destruction of part or all of the product. Do not proceed beyond a caution sign until the indicated conditions are fully understood and met.

Caution

Static Sensitive Devices.

Some of the semiconductor devices used in this equipment are susceptible to damage by static discharge. Depending on the magnitude of the charge, device substrates can be punctured or destroyed by contact or mere proximity to a static charge. These charges are generated in numerous way such as simple contact, separation of materials, and normal motions of persons working with static sensitive devices.

When handling or servicing equipment containing sensitive devices, adequate precautions must be taken to prevent device damage or destruction. Only those who are thoroughly familiar with industry accepted techniques for handling static sensitive devices should attempt to service the cards with these devices. In all instances, measures must be taken to prevent static charge buildup on work surfaces and persons handling and devices. Cautions are included throughout this manual where handling and maintenance involve static sensitive devices.

Safety Earth Ground

This is a safety class I product and is provided with a protective earthing terminal. An uninterruptible safety earth ground must be provided from the main power source to the product input wiring terminals, power cord, or supplied power cord set. Whenever it is likely that the protection has been impaired, the product must be made inoperative and be secured against any unintended operation.

Before Applying Power

Verify that the product is configured to match the available main power source per the input power configuration instructions provided in this manual.

If this product is to be energized via an auto-transformer (for voltage reduction) make sure the common terminal is connected to the earth terminal of the main power source.

Servicing

Warning

Any servicing, adjustment, maintenance, or repair of this product must be performed only by qualified personnel.

Adjustments described in this manual may be performed with power supplied to the product while protective covers are removed. Energy available at many points may, if contacted, result in personal injury.

Capacitors inside this product may still be charged even when disconnected from its power source.

To avoid a fire hazard, only fuses with the required current rating and of the specified type (normal blow, time delay, etc.) are to be used for replacement.

Warning

Eye Hazard

Eye protection must be worn when removing or inserting integrated circuits held in place with retaining clips.

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1 Introduction

This manual provides general information, installation instructions, programming instructions, theory of operation, maintenance instructions, parts information, and service diagrams for the HP 12009A Hewlett-Packard Interface Bus (HP-IB) Interface Card.

Functional Description

The Hewlett-Packard Interface Bus (HP-IB) is Hewlett-Packard's implementation of the IEEE Standard 488-1978 and Supplement 488-1978A-1980.

The HP-IB card provides an interface between HP 1000 A-Series computer systems and HP-IB compatible peripheral devices such as disk drives, tape drives, printers, and plotters. Up to 14 peripheral devices can connect to one HP-IB card. The peripheral devices connected to the card comprise an HP-IB system. Several systems can interface to the A-Series computer.

The HP-IB card plugs into a single slot in the A-Series backplane and is assigned a unique select code. The HP-IB card connects by cable to the HP-IB device or system. To the A-Series computer, this card is an I/O card under its software control. To the HP-IB system, this card might be a System Controller depending on the setting of a switch-selectable option. (See "Device Functions" in this chapter for a description of System Controller.) Figure 1-1 shows the HP-IB card in a typical A-Series system environment.

Two integrated circuits on the card are used to interface the card to the computer backplane and the card to the peripheral devices. The I/O Processor manages I/O functions. The HP-IB Interface Controller performs data and control signal interactions with the HP-IB devices. Through these two integrated circuits, the HP-IB card relieves the CPU of most HP-IB protocol processing.

The HP-IB card supports either high speed (IEEE Std 488-1978, paragraph 5.2.3) or low speed devices.

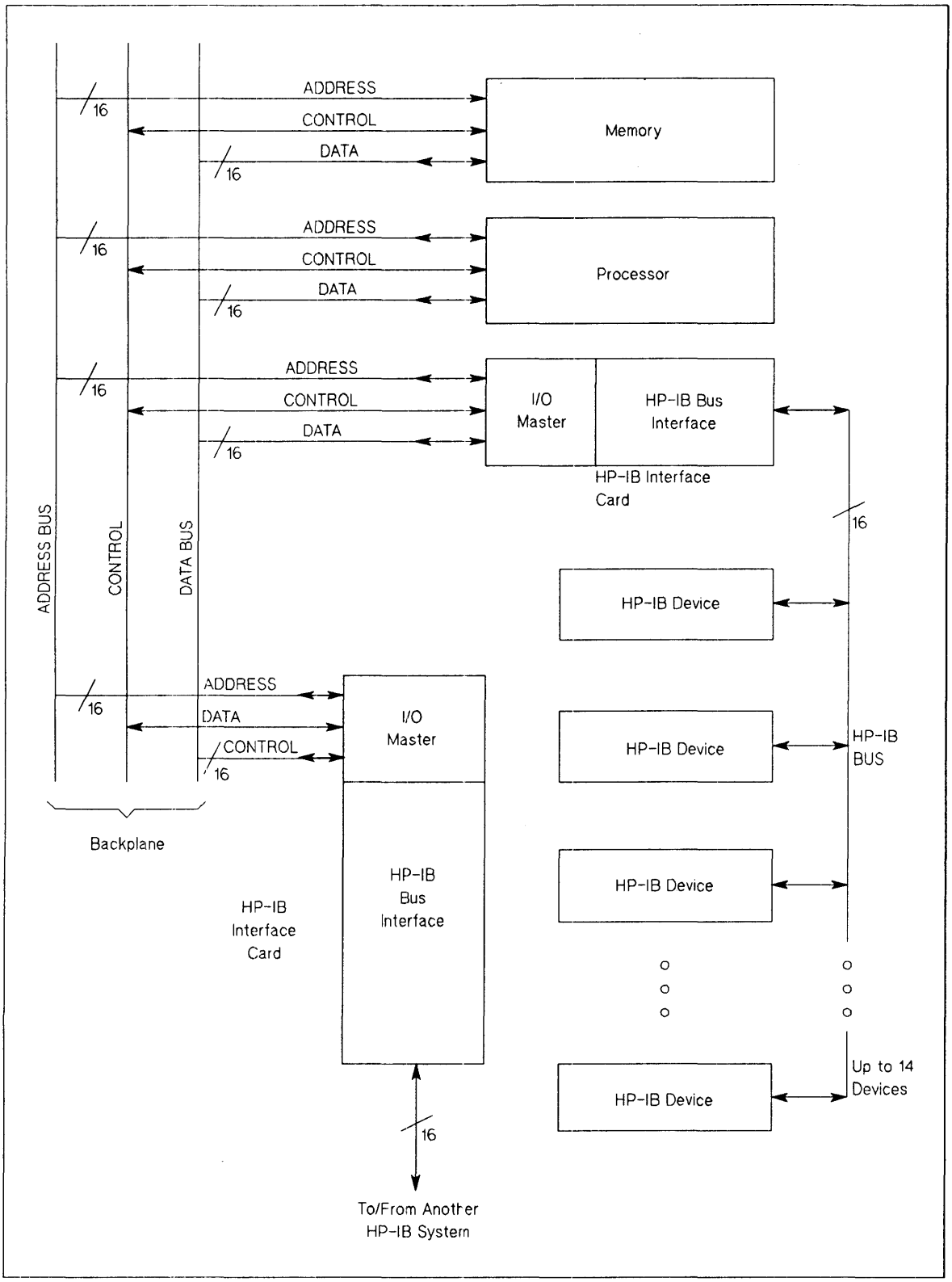


Figure 1-1. HP-IB Interface in a Typical Computer System Environment

Equipment Supplied

The standard HP 12009A HP-IB Interface Card consists of the following items:

Description	Part Number
HP-IB Interface Card	12009-60020
Interconnecting Cable	12009-60014
HP-IB Interface Reference Manual	12009-90001
High-Speed Operation Tag	

Options Available

Option 001 replaces interconnecting cable, part number 12009-60014, with a 4-meter cable, part number 12009-60015.

Identification

Five digits and a letter (12009A in this case) identify Hewlett-Packard products used with HP computers. The five digits identify the product and the letter shows the revision level of the product.

A part number marked on the card identifies the HP-IB interface card. A letter and a four digit date code (for example, E-2420) appear with the part number. The letter identifies the version of the etched circuit on the card. The date code identifies the electrical characteristics of the assembled card.

A name and part number identify the manual. The name, part number, and publication date appear on the title page. If the manual is revised, the publication date changes.

Specifications

Electrical Characteristics

HP-IB Bus Signal Lines

DIO1	Data Input/Output 1
.	.
.	.
DIO8	Data Input/Output 8
DAV	Data Valid
NRFD	Not Ready for Data
NDAC	Not Data Accepted
IFC	Interface Clear
ATN	Attention
SRQ	Service Request
REN	Remote Enable
EOI	End or Identify

Logic Levels

High > 2.4 V
Low < 0.4 V
For all signals, Low = True

Line Termination

Each of the bus signal lines is terminated with 2.3 KΩ to Vcc, and 4.7 KΩ to logic common (digital ground) without the load resistor pack.

Line Drivers

Each of the bus signal lines is driven with a circuit with the following typical characteristics:

Type: Tri-state, Open Collector
Output Voltage Low State: < 0.4 V at 48 mA
Output Voltage High State: 2.5 V at –5.2 mA

Line Receivers

Each of the bus signal lines is received with a circuit having the following typical characteristics:

Type: Schmitt Trigger
Threshold Positive Transition: 1.75 V
Threshold Negative Transition: 1.1 V
Input Current Low State: –1.3 mA at 0.4 V
Input Current High State: 0.7 mA at 5.5 V

DMA Transfer Rates

Low Speed: 500 Kbytes
High Speed:
Random Instruction Mix: 930 Kbytes
Worst Case Instruction Mix: 735 Kbytes

(Worst Case is a Jump Instruction in which the target address is its own address.)

Maximum Cable Length

Standard Operation: 2 meters per device connected with a 20-meter maximum length and a settling time of more than 500 nanoseconds.

High Speed Operation: 2 meters per device connected with a 15-meter maximum length and a settling time of less than 350 nanoseconds.

Operating Temperature

0°C to 55°C

Power Requirements (at 25°C)

	Current		Power Dissipated	
Voltage	**w/o Load Resistors**	**w/Load Resistors**	**w/o Load Resistors**	**w/Load Resistors**
+ 5 V	2.02 A	2.10 A	10.61 W	11..03 W
+ 12 V	32 mA	84 mA	0.40 W	1.06 W
		Total power:	11.01 W	12.09 W

Physical Characteristics

Card Dimensions

Width: 17.15 cm (6.75 in.)
Length: 28.91 cm (11.38 in.)

Connector

30-pin printed circuit board edge connector (cable supplied has standard HP-IB connector on the device end)

Capabilities

The HP-IB card can handle its own direct memory access (DMA) and can decode instructions from the CPU. Data moves over the HP-IB bidirectionally in 8-bit bytes. Data can be simultaneously transferred in three ways: (1) from a device to the computer and other devices, (2) from the computer to one or more devices, and (3) from one device to other devices under the direction of the computer.

A device may be capable of remote control operation. A system may have some devices operating under remote control, while other devices obey their front and rear panel controls (LOCAL). All devices must be addressable.

Corresponding pins of the HP-IB connectors of all devices are connected in parallel, making a parallel communication network. This permits information to flow in any direction on the bus and allows any device to talk directly with another device without going through a central control unit.

Supported Functions

The interface card supports the following functions as defined by the IEEE Standard 488-1978.

Controller Functions

C1	System Controller
C2	Send Interface Clear and Take Charge
C3	Send Remote Enable
C4	Respond to Service Request
C5	Send Interface Messages, Receive Control, Pass Control, Pass Control to Self, Parallel Poll, Take Control Synchronously

Controlled Device Functions

SR1	Service Request
RL2	Remote Local
PP1	Parallel Poll (see Section 3)
DC1	Device Clear
DT1	Device Trigger

Utility Functions

SH1	Source Handshake
AH1	Acceptor Handshake
T1	Basic Talker, Serial Poll, Talk Only
TE1	Basic Extended Talker, Serial Poll Talk Only
L1	Basic Listener, Listen Only Mode
LE1	Basic Extended Listener, Listener Only Mode

Handshaking

Devices connected to the bus must be addressed by the controller before they can function. Addressing determines which device "talks" and which devices "listen." Data moves in a bit parallel, byte serial format using an interlocked handshake technique. This technique assures that the talker does not remove data before the listener has finished using the data. It also ensures that data is not lost when devices having different speeds communicate on the same bus.

Device Functions

Devices connected to the bus can function in one or more of the following ways:

Talker – Any device that is capable of sending or transmitting information on the bus. There can be only one talker at a time on the bus.

Listener – Any device that can receive or accept information on the bus. There may be up to 14 listeners at the same time.

Talker-Listener – Any device that can both send and receive information on the bus. For example, a counter is a talker when sending data and a listener when it is being programmed.

Controller – Any device programmed to manage the flow of information between devices connected to the bus. The controller can address one of the devices as a talker and one or more of the others as listeners. A system can have more than one controller, but only one controller may be active at a time. (The Controller-in-Charge may be the System Controller.)

System Controller – At the time the system is configured, the system designer must designate one device as the System Controller. This device performs all the functions of a controller and can gain absolute control of the HP-IB.

Bus Lines

The HP-IB structure consists of 16 signal lines shown in figure 1-2. There are eight additional bus conductors: one ground, one cable shield, and six twisted-pair commons for six of the signal lines.

Each signal line has a name and mnemonic acronym that describes the message being carried on that line. There are three types of lines: Control (management), Data, and Transfer (handshake).

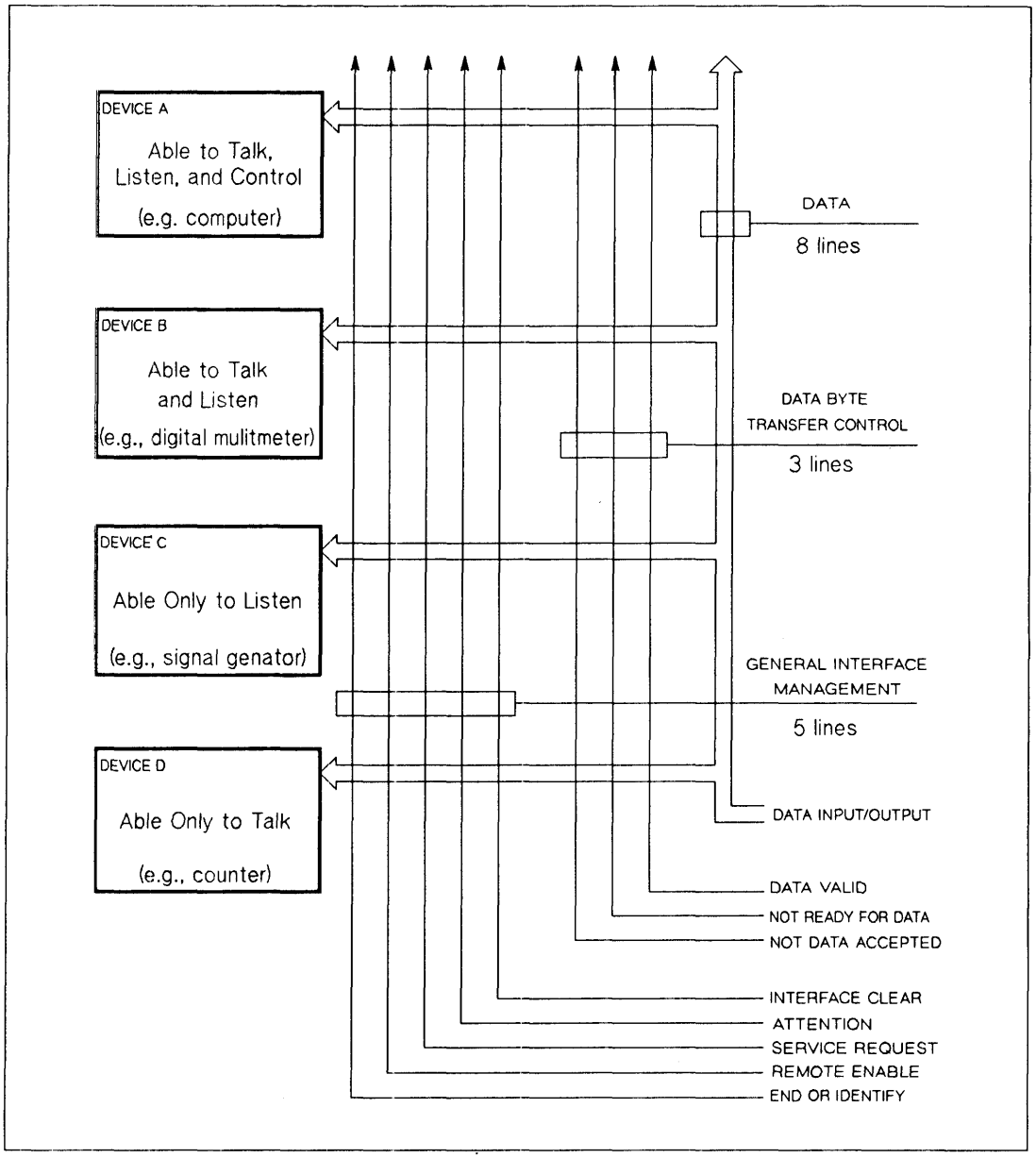


Figure 1-2. HP-IB Bus Structure

Control Lines

Note All devices connected to the bus, including the controller, must conform to these descriptions.

Five control lines manage the flow of information over the data and transfer lines. They communicate control and status information between the active controller and the devices connected to the bus. All devices must use ATN and IFC. A device may or may not use REN, SRQ, and EOI.

ATN (Attention) is driven by the active controller. All other devices must monitor ATN at all times.

When the controller sets ATN to its low (active or true) state, the bus is in Command Mode. In Command Mode, the controller is the talker and all devices are listeners. The controller may send commands or address those devices that are to communicate. The controller may also send "universal commands" while the bus is in Command Mode..

When the controller sets ATN to its high (inactive or false) state, the bus is in Data Mode. The device addressed to talk and those addressed to listen now communicate on the Data Lines.

The controller may set ATN any time but it is usually at the end of a transfer (handshake) cycle so that data is not lost.

The System Controller uses IFC (Interface Clear) to initialize the bus. Only the System Controller can drive IFC and it must be monitored by all other devices on the bus. When the System Controller sets IFC low (active or true) for at least 100 microseconds, the following takes place: (1) all talkers and listeners stop, (2) serial poll mode is disabled, and (3) control returns to the HP-IB controller. When IFC is high, it has no effect on the bus operation. The System Controller may set IFC low at any time.

REN (Remote Enable) is for operating devices under remote control. Only devices capable of remote operation use REN and monitor it at all times. Devices that do not use REN terminate the line in a resistive load. Only the System Controller may assert REN and may change its state at any time.

A device sets SRQ (Service Request) low (active or true) to indicate that it wants the attention of the controller. Only the controller senses SRQ. SRQ may be set low by a device at any time except when IFC is in the low state. Some devices do not use SRQ but terminate it in a resistive load.

EOI (End or Identify) indicates the end of a character string. When the bus is in Data Mode (ATN high), the addressed talker may indicate the

end of its data by setting EOI low (active or true) at the same time it places the last byte on the Data Lines.

Data Lines (DIO1-DIO8)

Eight Data Lines transfer data such as input, output, program code, addresses, control information, and status information. This data is passed one character (byte) at a time under control of the Transfer Lines.

Transfer Lines

Three Transfer (handshake) Lines execute the transfer of information on the data lines. All devices use these lines. An interlocked handshake technique allows asynchronous data transfer without timing restrictions on any device connected to the bus. The transfer of each byte occurs at the speed of the slowest device. The three transfer lines are: NRFD, NDAC, and DAV.

NRFD (Not Ready For Data) shows that all listeners are ready to accept data. NRFD is controlled by the listeners and sensed by the talker. When NRFD is high (inactive or false), all listeners are unconditionally ready for data and the talker may put a byte of information on the data lines.

When the controller sets ATN low (active or true), all devices must respond within 200 nanoseconds. If a device is "Ready for Data" it sets NRFD high, otherwise it sets NRFD low. When the controller sets ATN high, only those devices addressed to listen will respond.

NDAC (Not Data Accepted) indicates the acceptance of information on the data lines. NDAC is controlled by listeners and sensed by the talker. When NDAC is high (inactive or false), all listeners have accepted the byte of information on the data lines and the talker may remove that byte of information.

When the controller sets ATN low (active or true), all devices must set NDAC high within 200 nanoseconds. When the controller sets ATN high, devices addressed to listen will set NDAC high within 200 nanoseconds.

DAV (Data Valid) indicates that the information on the data lines is valid. DAV is driven by the talkers and sensed by the listeners. When DAV is low (active or true), the states of data lines DI01 through DI08 are valid and may be accepted by all listeners.

After placing the bus in Command Mode (setting ATN low), the controller must wait at least one microsecond before setting DAV low. In either Command or Data Mode, a talker designed with open-collector circuits must not set DAV low for at least two microseconds after placing valid data at its output connector. Those designed with tri-state logic must wait at least 500 nanoseconds if operating at low speed and 350 nanoseconds if operating at high speed.

Table 1-1 summarizes these conditions.

Table 1-1. Transfer Line Conditions

	ATN Low (Command Mode)	ATN High (Data Mode)
NRFD	LOW: One or more units not ready for data. HIGH: All units ready for data	LOW: One or more listeners not ready for data HIGH: All addressed listeners ready for data
NDAC	LOW: One or more units have not accepted data HIGH: All units have accepted data	LOW: One or more listeners have not accepted data HIGH: All addressed listeners have accepted data
DAV	LOW: Controller has valid data on DIO lines HIGH: Controller's data is not valid	LOW: The addressed talker has valid data on lines HIGH: The addressed talker data is not valid

*** Note: Low = active or true; High = inactive or false**

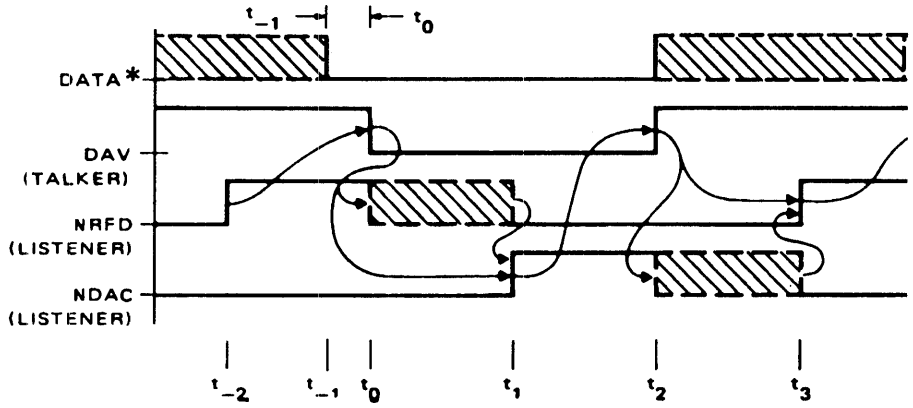
Data Transfer Timing

The transfer of data on the bus is asynchronous and therefore places no restrictions on the data rates of devices connected to the bus. The transfer is under the control of three lines, DAV, NRFD, and NDAC. The talker drives the Data Lines and DAV (Data Valid). The listeners drive NRFD (Not Ready for Data) and NDAC (Not Data Accepted).

The assertive, or active, state of both NRFD and NDAC is low. Since all devices on the bus have their corresponding lines connected together (for example, NRFD), all listeners must be in a high state before the line goes high. This wired-AND condition allows a talker to recognize when the slowest listener has accepted a byte of data and is ready for the next byte.

Figure 1-3 shows the timing and levels required to transfer a byte of data. The transfer is initiated by all listeners signifying they are ready for data by setting NRFD high (t_{-2}). When the talker recognizes NRFD is high and has placed valid data on the data lines, it sets DAV low (t_0). When the listeners sense that DAV is low and have finished using the data, they set NDAC high (t_1).

Sequential Requirements of the Three Wire Transfer



Events

t_{-2} : Listener becomes ready to accept data.

t_{-1} : Talker has put data on the lines.

t_0 : Indicates data is valid.

t_1 : Listener has accepted the data and no longer requires it held valid.

t_2 : Talker indicates the data is no longer valid and may change it.

t_3 : Listener indicates it is ready for new data.

t_4 : A new cycle begins (equivalent to t_0).

t_{-1} to t_0 : Time that data is put on lines before DAV is set low.

* A composite of the DIO1 through DIO8 lines for illustrative purposes.
The curved lines indicate transfer (handshake) signal sequence.

Figure 1-3. Transfer Timing

A listener may set NRFD low when it recognizes that DAV is low and must do so before or at the same time it sets NDAC high. The talker may return DAV to its high state after it detects that NDAC is high (t_2). When it recognizes that DAV is high, a listener may set NDAC low and must do so before or at the same time it sets NRFD to its high state (t_3).

Electrical Characteristics

All 16 bus lines are compatible with TTL integrated circuits. Each line is terminated within the transceiver circuits into a resistive network consisting of a 2.3 K ohm resistor to +5 V and a 4.7 K ohm resistor to logic common. Typically, the required bus terminations are internally provided by the transceiver circuits. An optional load resistor, U119 (storage location U79) forms an external divider consisting of 330 ohm resistors to +5 V and 680 ohm resistors to logic common that can be used to provide the drive for high speed operation.

Each driver/receiver pair (see figure 1-4) forms a complete interface between the bus and a device. Either the driver or the receiver of each channel is enabled by its corresponding Send/Receive (S/R) input with the disabled output of the pair forced to a high impedance state. An additional option allows the driver to be operated in an open-collector or active pull-up configuration. The receivers have input hysteresis to improve the noise margin and their input loading follows the bus standard.

Cable Characteristics

In addition to the cable assemblies shipped with HP 12009A products, bus cables are available for connecting devices into a system. These have an overall shield to reduce susceptibility to external noise, and use a mixture of individual wires and twisted pairs to reduce crosstalk. The connectors on both ends of the cables are identical, terminated in two 24-pin connectors, one male and one female. The pin connections of these connectors are shown in figure 1-5.

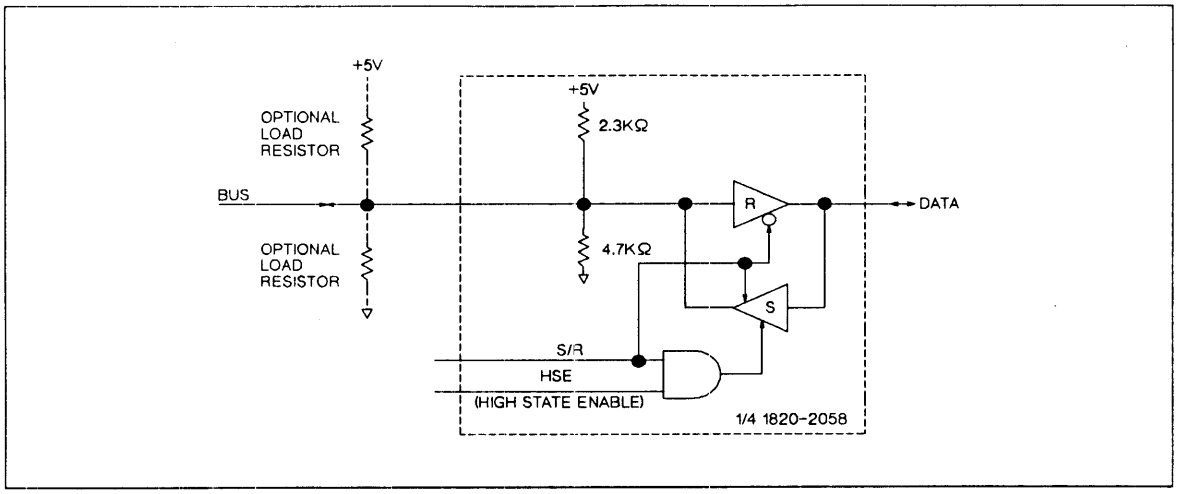


Figure 1-4. Typical HP-IB Transceiver (Driver/Receiver) Circuit

The driver/receiver pairs provide the following:
Driver: When a talker, it is capable of sinking 48 mA at 0.4 V
Receiver: When a listener, it requires –1.3 mA at 0.4 V to drive

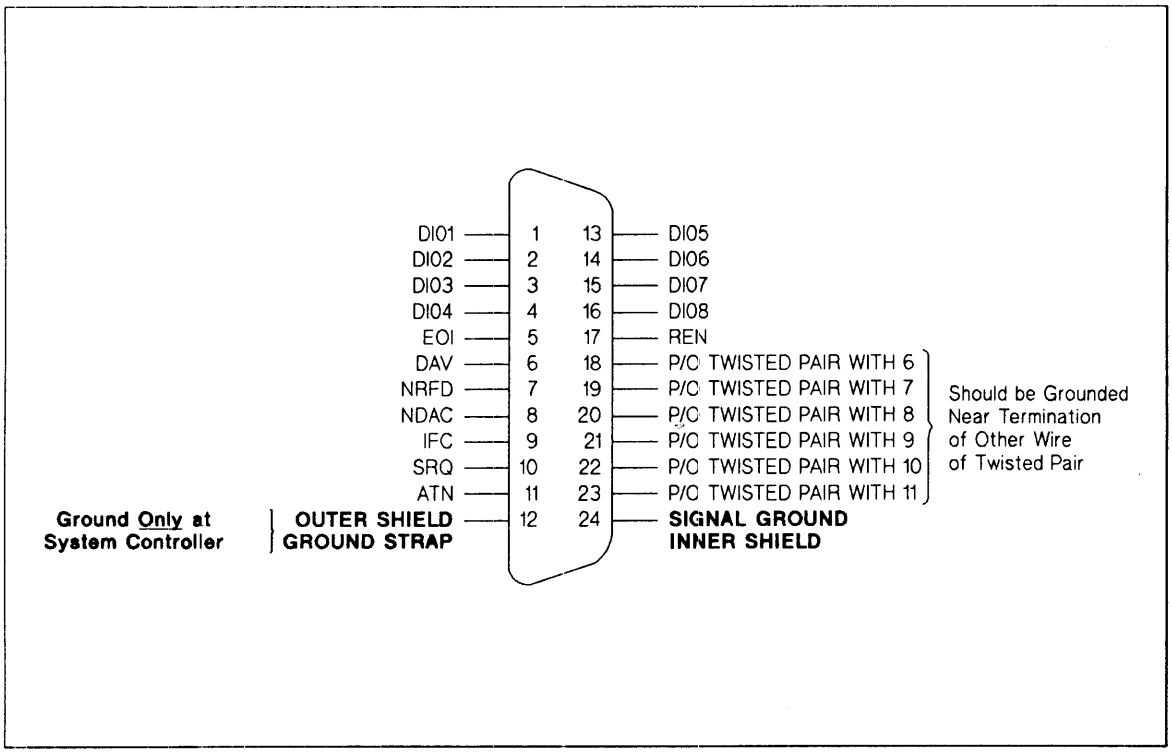


Figure 1-5. HP-IB Cable Connector Pin Connections

2 Installation

This section gives information about installing and checking the operation of the HP 12009A HP-IB card.

Requirements

Power Requirements

The HP-IB card gets its operating power from the computer's power supply through the backplane. Before installing the card, determine if the additional current drain will overload the power supply. If the card was installed at the factory, the required calculations have been made and an overload will not occur. See "Specifications" in chapter 1 for the current and voltage requirements for the HP-IB card.

Interface Requirements

Backplane to HP-IB Card

All interactions between the HP-IB card, the central processor card, and the memory card occur on the backplane through either of two connectors, P1 or P2. Tables 2-1 and 2-2 list connections from the backplane to the HP-IB card.

Switch Selectable Options

Two Dual In-line Package (DIP) switches (U1 and U144) set switch selectable options. Figure 2-1 shows the locations of the two DIP switches. Each DIP switch assembly contains eight independent switches. Switches S1 through S8 on U144 correspond to Address Select Bits 0 through 7. Switches S3 through S8 on U1 determine the select code for the card.

Table 2-1. Backplane Connections, Connector P1

P1–	Signal Name	Signal Definition
1	ICHID–	Interrupt Chain In Disable
2	ICHOD–	Interrupt Chain Out Disable
3	MCHID–	Memory Chain In Disable
4	MCHOD–	Memory Chain Out Disable
5	MLOST–	Memory Lost
6	MCHODOC–	Memory Chain Out Disable Open Collector
7	PFW–	Power Fail Warning
8	SPARE 1	Reserved
9	SC0	Address Extension Bus Bit 0
10	SC1	Address Extension Bus Bit 1
11	SC2	Address Extension Bus Bit 2
12	SC3	Address Extension Bus Bit 3
13	GND	Ground
14	GND	Ground
15	SPARE 2	Reserved
16	GND	Ground
17	SC4	Address Extension Bus Bit 4
18	SC5	Self Configure
19	AB0	Address Bus Bit 0
.	.	.
.	.	.
.	.	.
33	AB14	Address Bus Bit 14
34	WE–	Write Enable
35	DB0	Data Bus Bit 0
.	.	.
.	.	.
.	.	.
50	DB15	Data Bus Bit 15

Table 2-2. Backplane Connection, Connector P2

P2–	Signal Name	Signal Definition
1	CPUTURN–	Processor Turn
2	GND	Ground
3	Remem–	Remote Memory
4	VALID–	Data Valid
5	IORQ–	I/O Handshake Request
6	INTRQ–	Interrupt Request
7	MP	Memory Protect
8	RNI–	Read Next Instruction
9	MEMGO–	Memory Cycle Initiation
10	PE–	Pairty Error
11	SCHID–	Slave Chain In Disable
12	SCHOD–	Slave Chain Out Disable
13	IAK–	Interrupt Acknowledge
14	IOGO–	I/O Handshake Request Acknowledge
15	GND	Ground
16	SLAVE–	Slave Request
17	GND	Ground
18	MRQ–	Memory Request
19	GND	Ground
20	FCLK–	Fast Clock
21	GND	Ground
22	CCLK–	Communications Clock
23	PINT–	Priority Interrupt
24	SCLK–	System Clock
25	CRS–	Control Reset
26	PON	Power On
27	GND	Ground
28	BUSY–	Memory Busy
30	GND	Ground
.	.	.
.	.	.
34	GND	Ground
35	+5 V	
36	+5 V	
37	+5 V	
38	+5 V	
39	+12 M	
40	–12 M	
41	+12 V	
42	+12 V	
43	+12 V	
44	–12 V	
45	+5 M	
46	+5 M	
47	AC02	
48	AC02	
49	AC01	
50	AC01	

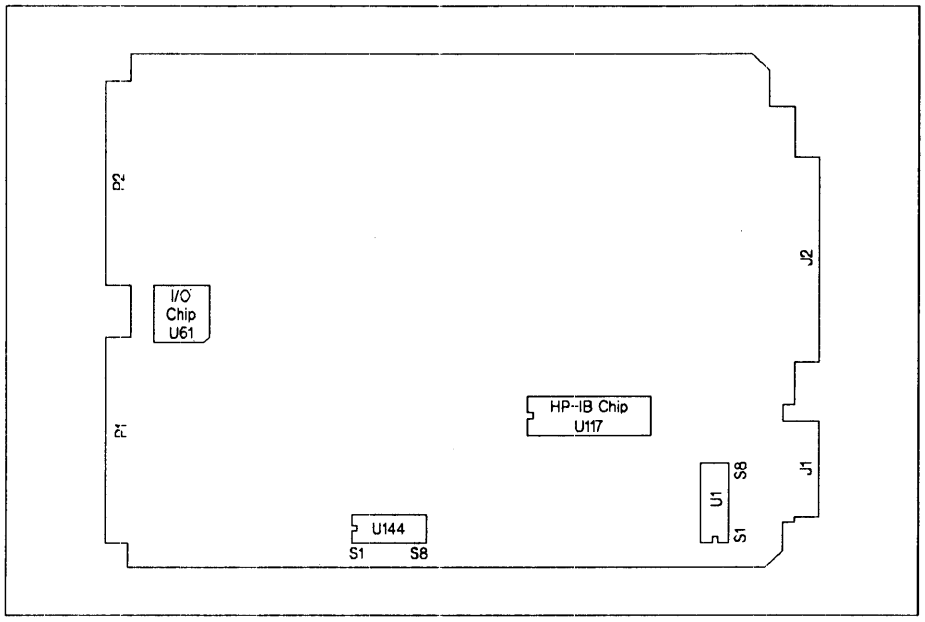


Figure 2-1. Major Component Locations

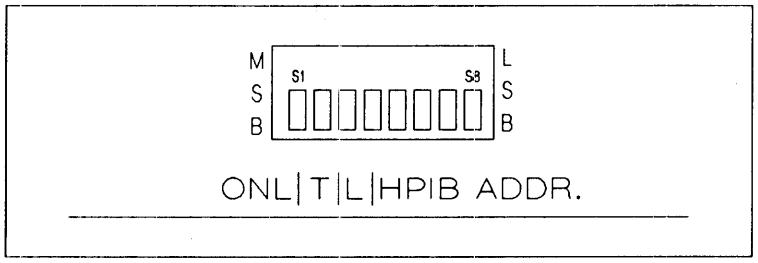


Figure 2-2. Switches U144S1 through U144S8

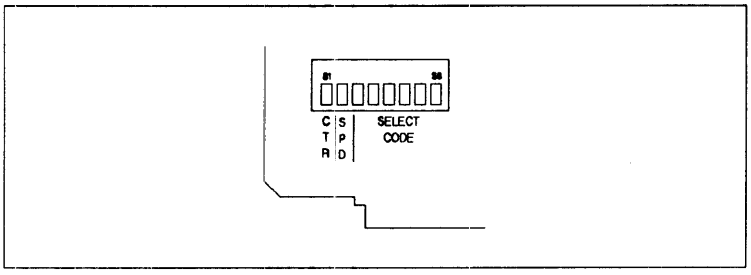


Figure 2-3. Switches U1S1 through U1S8

HP-IB Address Selection

When loaded into the HP-IB Chip's Register 7 under software control, switches U144S1 through U144S8 (see figure 2-2) determine the HP-IB address and related control functions. Switch functions are:

Switch U144S1 (Bit 7) – Puts the HP-IB Chip online when set to the open (up) position.

Switch U144S2 (Bit 6) – Puts the HP-IB Chip into the "Talk Always" mode when set to the open (up) position.

Switch U144S3 (Bit 5) – Puts the HP-IB Chip into "Listen Always" mode when set to the open (up) position.

Switches U144S4 through U144S8 (Bits 4 through 0) – The value of these five bits determines the HP-IB address to which the HP-IB Chip will respond. An open switch represents a logic 1 and a closed switch represents a logic 0. U144S4 is the Most Significant Bit (MSB) and U144S8 is the Least Significant Bit (LSB).

Select Code Selection

Switches U1S3 through U1S8 (see figure 2-3) determine the select code for the HP-IB card. An open switch represents a logic 1 and a closed switch represents a logic 0. U1S3 is the Most Significant Bit (MSB) and U1S8 is the Least Significant Bit (LSB).

System Controller Selection

Switch U1S1 (see figure 2-3) determines if the HP-IB card will be the System Controller for the bus. If the switch is set to the open (up) position, the card will function as the System Controller.

Data Settling Time Selection

Switch U1S2 (see figure 2-3) determines the time delay between the assertion of the data on the bus and the assertion of the data position. If the switch is set to the open (up) position, the delay is about 500 nanoseconds. When the switch is set to the closed (down) position, the delay is about 350 nanoseconds. This delay time satisfies IEEE Standard 488-1978 for fast settling time required for high-speed operation.

Installation

Caution Some of the components used on the printed circuit card are susceptible to damage by static discharge. Refer to the safety considerations at the front of this manual before handling the card.

Make sure that the computer's power supply can handle the added load. Then follow these steps:

1. Set switch U1S1 up if the HP-IB card will be a System Controller, down if not.

2. Set switch U1S2 according to mode of operation. Set it up for slow settling time, down for fast settling time. Label all high speed devices. Do not connect high and low speed devices to the same bus.

3. Set the select code for the card with switches U1S3 through U1S8. (See "Select Code Selection" earlier in this chapter.)

4. Set the address for the card with switches U144S4 through U144S8. (See "HP-IB Address Selection" earlier in this chapter.)

Caution Do not remove jumpers by desoldering unless you have experience and training in this procedure. You can seriously damage the board if you desolder a jumper incorrectly.

5. If you require detection of the DAC high/RFD high HP-IB bus error condition (see chapter 4), remove jumper W1 (located between U79 and U119). You can remove the jumper with wire cutters or by desoldering. Do this *after* an initial checkout. Removal of the jumper causes the HP-IB interface diagnostic to fail unless a peripheral device is connected to the card and powered on.

6. Turn off the power to the computer and the I/O device. Insert the HP-IB card into the desired slot in the backplane. Make sure that the components on the card are on the same side as the other interface cards in the backplane. Be careful not to damage the card or any adjacent cards. Press the card firmly into place.

7. Connect the appropriate cable from the bus to the card. There are two connectors (J1 and J2) on the edge of the card (see figure 2-1). Connector J2 connects to the HP-IB cable.

Checkout

Perform these steps to verify correct operation of the HP-IB card:

1. Run the computer self-test. Refer to the *HP 1000 Model 26, 27 and 29 Computer System Installation and Service Manual*, part number 02196-90002, or the *Micro 1000 Computer System Installation and Service Manual*, part number 02430-90001.

2. Run the kernel diagnostic. Refer to the *Diagnostic Manual*, part number 24612-90011.

3. Run the HP-IB interface diagnostic. Refer to the *Diagnostic Manual*, part number 24612-90011. Note that if jumper W1 has been removed, the diagnostic will fail the on-line test unless a peripheral device is connected to the interface card.

4. If the HP-IB card does not operate correctly, contact the nearest Hewlett-Packard Sales and Support Office for information. See the Sales and Support Offices listed with your system documentation.

Load Resistor Pack

Caution If you install or remove the load resistor incorrectly, you may damage the card.

For low speed operation, remove the load resistor pack. This resistor pack is an 18-pin DIP (Dual Inline Package), and is installed at the factory at location U119. For low speed operation move the resistor pack to U79, a storage location. Pin one of the resistor pack goes in the receptacle just above the "U" of "U79" silk-screened on the printed circuit board.

For high speed operation, leave the resistor pack in location U119. When the HP-IB card is configured for high speed operation, attach the high speed operation tag (figure 2-4) to the device end of the HP-IB cable. You can do this by wrapping a twist tie around the cable and through the holes in the tag.

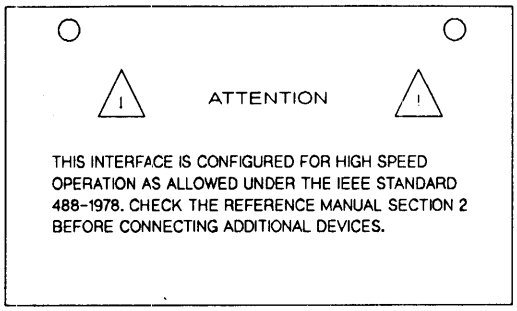


Figure 2-4. HP-IB High-Speed Operation Tag

Interconnecting Cables

The cable supplied with the card has a 30-contact circuit edge connector on one end and a standard HP-IB connector on the other end. Connect the printed circuit edge connector to J2 (see figure 2-1). Table 2-3 shows the pin connections for the interconnecting cable.

Connect the HP-IB connector end to the peripheral device. Other devices may be added to the bus by using the standard HP-IB cables listed in table 2-4. The cables must be ordered separately.

Cabling Length Restrictions

Low-Speed Operation (U1S2 OPEN).

For low speed operation, follow these rules:

- All devices on the bus must be low speed devices.
- The total length of cable for one card must be less than or equal to 2 meters times the number of devices connected together. The HP-IB card counts as one device.
- The total length of cable must not exceed 20 meters.

You may have up to 4 meters of cable between the first 2 devices (2 units times 2 meters per device = 4 meters). You may add units using 2-meter cables up to a total of 10 units (10 units times 2 meters per device = 20 meters). For example, you could have one 4-meter and eight 2-meter cables (4 + [8X2] = 20). If you want to connect more than 10 devices, you must use cables shorter than 2 meters between some of the devices. For example, 15 devices can be connected using one 4-meter cable and 13 one-meter cables (4 + [13X1] = 17). You can use other combinations as long as you meet the above rules. Remember to count the HP-IB card as one device.

Table 2-3. HP-IB Interface to Bus Connector (J2)

J1			J2		
Pin		Name	Pin		Name
1	B	GET–	1	T	DI01
2	T	+5 V	2	T	DI02
3	B	COMMON	3	T	DI03
4	T	—	4	T	DI04
5	B	COMMON	5	T	EOI
6	T	ATN	6	T	DAV
7	B	COMMON	7	T	NRFD
8	T	SRQ	8	T	NDAC
9	B	COMMON	9	T	IFC
10	T	IFC	10	T	SRQ
11	B	COMMON	11	T	ATN
12	T	NDAC	12	T	—
13	B	COMMON	13	T	—
14	T	NRFD	14	T	—
15	B	COMMON	15	T	—
16	T	DAV	A	B	DI05
17	B	REN	B	B	DI06
18	T	EOI	C	B	DI07
19	B	DI08	D	B	DI08
20	T	DI05	E	B	REN
21	B	DI07	F	B	COMMON
22	T	DI03	H	B	COMMON
23	B	DI06	J	B	COMMON
24	T	DI02	K	B	COMMON
25	B	DI05	L	B	COMMON
26	T	DI01	M	B	COMMON
			N	B	COMMON
			P	B	—
			R	B	—
			S	B	—

B = bottom
C = top

Table 2-4. Accessory HP-IB Bus Cables

Length	Accessory Number
1 meter	10833A
2 meters	10833B
4 meters	10833C
0.5 meters	10833D

High Speed Operation (U1S2 CLOSED)

For maximum data transfer rate (nominally 930 K bytes per second), follow thses rules:

- All devices expected to talk at the higher rates must use a settling time of 350 nanoseconds or less.
- All devices expected to operate at the higher speeds should use 48 mA three-state drivers.
- The device capacitance on each lead (REN and IFC excepted) should be less than 50 pF per device. In a system configuration, the total device capacitance should be no more than 50 pF for each equivalent resistive load in the system.
- Keep cable links as short as possible according to table 2-4.

Table 2-4. Cabling Guidelines for High Speed Operation

Number of External Devices	Maximum Total Cable Length (meters)	Maximum Average Cable Length Between Devices (meters)
1	9	9
2	10	5
3	11	3
4	12	3
5	13	2
6	14	2
7	15	2

- Normally, no more than eight high speed devices can be in the system (the HP-IB card counts as one device). A normal maximum system is composed of the HP-IB card with its high-speed resistor pack and up to seven peripherals (See case 2 in figure 2-5). Note that the optional load resistor pack adds the equivalent of 7 loads to the outputs to increase drive to external devices.
- All devices on the bus should be powered on.

Note

If power to the HP-IB card fails while the load resistor pack is installed, the HP-IB bus will be pulled down. That is, the output drive circuitry of any talker on the bus will not be able to bring any bus line to a logic-high state. To the drive circuitry, the unpowered HP-IB card is a low resistance path to ground.

- The following information is provided if you have specialized knowledge and the equipment to verify the correct operation of the system. Use this for high speed configurations with more than eight device load equivalents (usually seven peripherals) and more than eight meters of cable.

1. Calculate N as:

   M = meters of cable
   load = device load equivalents
   N = M – load

2. If N > 0 and more than eight devices are present in the HP-IB system, the optional resistor pack supplied with the card will not meet the requirements for the system. Use the following formulas to determine the resistance values:

   $$\text{Resistance to Vcc} = \frac{2.3\ \text{K}\Omega}{\text{N}}$$

   $$\text{Resistance to logic common} = \frac{4.7\ \text{K}\Omega}{\text{N}}$$

3. Once you have calculated the correct values for the load resistors you must have a custom resistor pack manufactured. Hewlett-Packard does not manufacture custom resistor packs for this product.

   In high speed operation, stray resistance and capacitance may adversely affect the settling time of the control and data lines on the HP-IB bus. The result may be intermittent failures and loss of data. If you are using a configuration similar to cases 1 and 3 in figure 2-5 verify the proper operation of the system.

Other Cabling Considerations

Do not stack more than four HP-IB connectors on one device. If you do, force will be exerted on the panel of the device and may cause damage. A daisy chain configuration will avoid this.

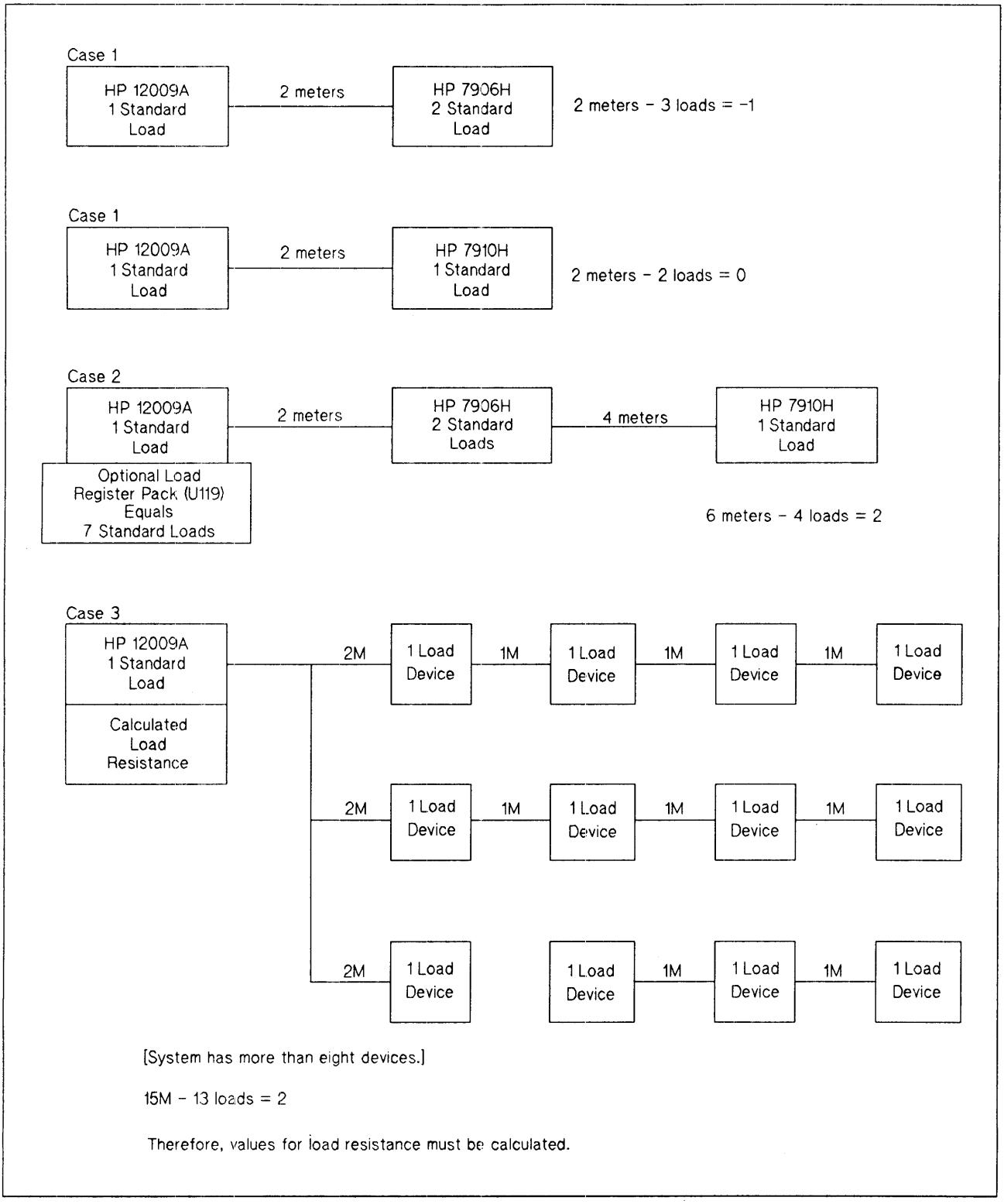


Figure 2-5. HP-IB System Examples

Reshipment

If you need to ship the HP-IB to Hewlett-Packard for any reason, attach a tag identifying the owner and giving the reason for shipment. Include the part number of the HP-IB.

Caution

Be sure the packer observes anti-static precautions.

Pack the HP-IB in the original factory packing material, if available. If the original material is not available, use good commercial packing material. Reliable commercial packing and shipping companies have the facilities and materials to repack the item.

3 Programming

This card can handle its own Direct Memory Access (DMA), decode its own instructions from the central processor, pack and unpack bytes, and support the HP-IB functions listed in chapter 1 of this manual. If the standard interface driver, ID.37, does not provide sufficient control of the above capabilities, you may write your own Interface Driver in assembly language. This chapter provides specific assembly language information about the HP-IB Interface. This chapter is not a tutorial on HP 1000 A-Series assembly language or on the design of interface drivers. Your local Hewlett-Packard Sales and Support office can help you determine what additional manuals you may need.

For additional information, see the *RTE-A Programmers Reference Manual*, part number 92077-90007.

If you intend to use a high-level language to control the HP-IB Interface, consult the language's user manual for information.

Note

If your HP 12009A has had the NDAC-NRFD error detection feature enabled (jumper W1 has been cut) you must set up a finite time-out. Have the driver call it on exit.

Overview

The A-Series Interface card has two sections, an I/O Master section and an HP-IB Bus Interface section.

I/O Master Section

The I/O Master section performs all I/O processing functions for the computer. These functions include I/O instruction recognition and execution and direct memory access (DMA). The I/O Master consists of an I/O Processor (IOP) Chip and associated logic circuitry. See figure 3-1 for a simplified block diagram of the I/O Processor Chip.

Global Register

The Global Register (GR) is a 6-bit register located in the I/O Processor Chip and controlled by the CPU. This register may be loaded with an OTA 2 (Output A) or OTB 2 (Output B) I/O instruction, enabled with a CLF 2 (Clear Flag) I/O instruction, and disabled with an STF 2 (Set Flag) I/O instruction. When the Global Register is enabled, any I/O instruction that is executed by the CPU automatically applies to the card whose select

code is in the Global Register. If the HP-IB card is selected, the current I/O instruction is decoded and executed by the HP-IB card.

Using the Global Register to store the select code frees the six least significant bits of the I/O instructions so they can be used to address registers on the HP-IB card. There are three such registers, a Data Register, a Status Register, and a Control Register, in addition to registers which are internal to the I/O Processor Chip.

Data may be transferred to and from the HP-IB card with or without the Global Register enabled. The Global Register must be enabled to access the card's Control and Status registers.

I/O Instruction Set

The I/O Master executes the following twelve I/O instructions:

CLC	Clear Control
CLF	Clear Flag
LIA	Load Into A
LIB	Load Into B
MIA	Merge Into A
MIB	Merge Into B
OTA	Output A
OTB	Output B
SFC	Skip if Flag Clear
SFS	Skip if Flag Set
STF	Set Flag
STC	Set Control

The 6-bit Global Register allows a maximum of 64 (decimal) select codes. The I/O Master executes a portion of these. Select codes 00 through 17 (octal) are reserved for the CPU, leaving 20 through 77 (octal) available for the I/O system. For further information about the I/O instruction set, refer to the Reference Manual for your computer.

Instruction Usage Summary

Table 3-1 lists all of the I/O Processor instructions. These are recognized by their select codes. There are three conditions relevant to the instruction's execution:

- Is the Global Register (GR) enabled?
- Do the contents of the GR equal the I/O Processor Chip's select code?
- Do the lower six bits of the instruction equal the I/O Processor Chip's select code (IR = SC)?

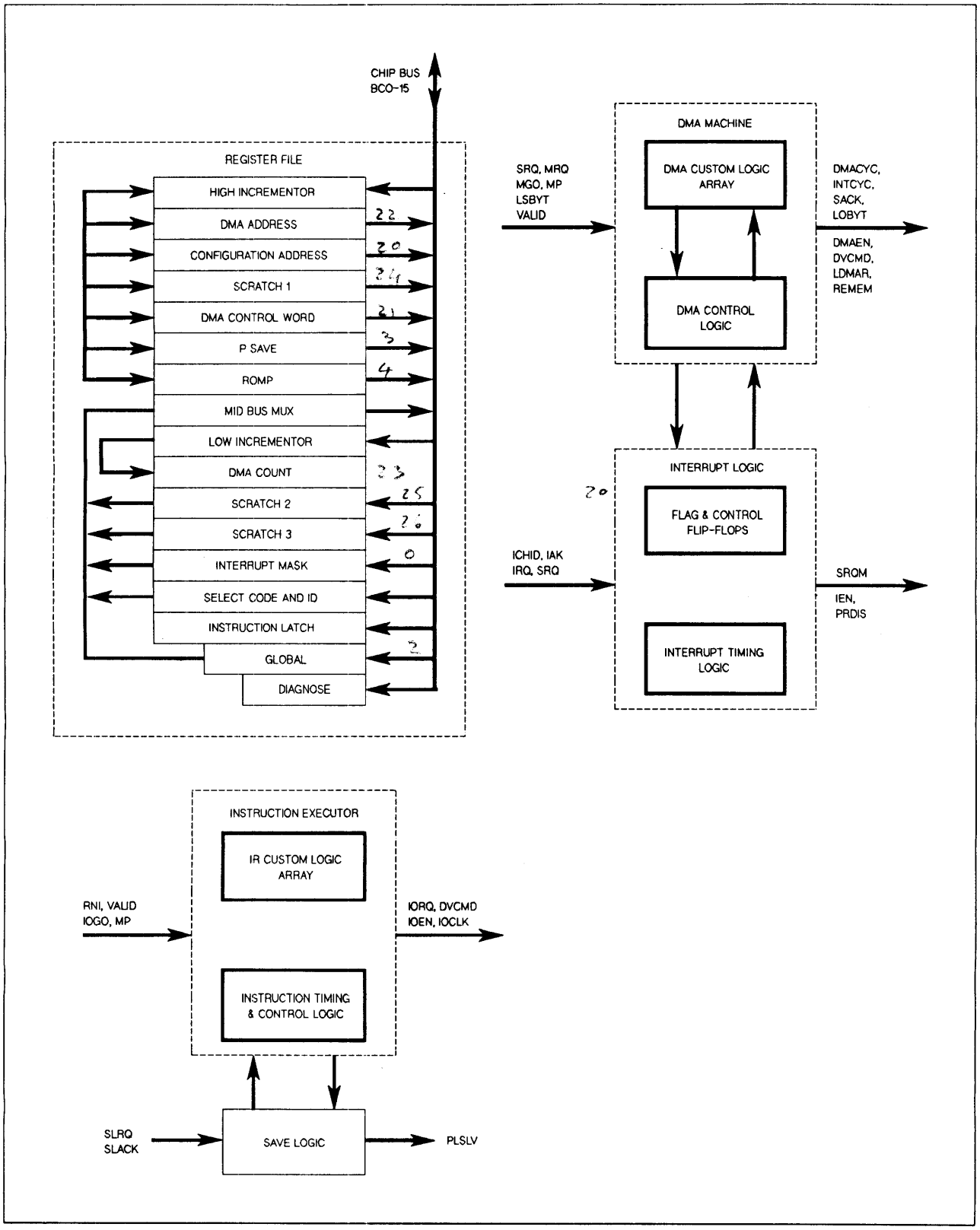


Figure 3-1. I/O Processor Chip (U61) Block Diagram

Table 3-1. I/O Processor Chip Instructions by Select Code

Instruction	Function	GR ON	GR = SC	IR = SC	Notes
LI* 0	Read interrupt mask	X	Y	X	
MI* 0	Merge interrupt mask	X	Y	X	
OT* 0	Write interrupt mask	X	X	X	
CLF 2	Enable GR	X	X	X	
STF 2	Disable GR	X	X	X	
LI* 2 [,C]	Read GR	X	Y	X	1,9
MI* 2 [,C]	Merge GR	X	Y	X	1,9
OT* 2 [,C]	Write GR	X	X	X	
STC 2 [,C]	Enable Slave logic	X	X	X	1,2
[,C]	Enable GR				
CLC 3	"BREAK" to front panel	X	X	X	2
HLT XX	"BREAK" to front panel	X	X	X	2
LI* 3	Read P SAVE	X	X	X	2
MI* 3	Merge P SAVE	X	X	X	2
OT* 3	Write P SAVE	X	X	X	2
LI* 3,C	Read ROM P	X	X	X	2
MI* 3,C	Merge ROM P	X	X	X	2
OT* 3,C	Write ROM P	X	X	X	2
SFC 20	Skip if FLG 20 clear	Y	Y	X	3
SFS 20	Skip if FLG 20 set	Y	Y	X	
CLF 20	Clear FLG 20 and FLG 21	Y	Y	X	
STF 20	Set FLG 20	Y	Y	X	
STC 20 [,C]	Enable DMA self-configuration	Y	Y	X	
CLC 20 [,C]	Disable DMA self-configuration	Y	Y	X	
LI* 20 [,C]	Read DMA configuration address	Y	Y	X	
MI* 20 [,C]	Merge DMA configuration address	Y	Y	X	
OT* 20 [,C]	Write DMA configuration address	Y	Y	X	
[,C]	Clear FLG 20 and FLG 21				
SFC 21	Skip if FLG 21 clear	Y	Y	X	4
SFS 21	Skip if FLG 21 set	Y	Y	X	
CLF 21	Clear FLG 21	Y	Y	X	
STF 21	Set FLG 21	Y	Y	X	
STC 21 [,C]	Enable DMA transfers	Y	Y	X	
CLC 21 [,C]	Disable DMA transfers	Y	Y	X	
LI* 21 [,C]	Read DMA Control word	Y	Y	X	
MI* 21 [,C]	Merge DMA Control word	Y	Y	X	
OT* 21 [,C]	Write DMA Control word	Y	Y	X	
[,C]	Clear FLG 21	Y	Y	X	
SFC 22	Skip if FLG 22 clear	Y	Y	X	5
SFS 22	Skip if FLG 22 set	Y	Y	X	
CLF 22	Clear FLG 22	Y	Y	X	
STF 22	Set FLG 22	Y	Y	X	
CLC 22 [,C]	Force DMA reconfiguration	Y	Y	X	
LI* 22 [,C]	Read DMA address	Y	Y	X	
MI* 22 [,C]	Merge DMA address	Y	Y	X	
OT* 22 [,C]	Write DMA address	Y	Y	X	
[,C]	Clear FLG 22				

Table 3-1. I/O Processor Chip Instructions by Select Code (continued)

Instruction	Function	GR ON	GR = SC	IR = SC	Notes
SFC 23	Skip if FLG 20, FLG 21, and FLG 22 all clear	Y	Y	X	6
SFS 23	Skip if FLG 20 or FLG 21 or FLG 22 set (inclusive OR)	Y	Y	X	
CLF 23	Clear FLG 20, FLG 21, and FLG 22	Y	Y	X	
CLC 23 [,C]	Terminate DMA operation				
LI* 23 [,C]	Read DMA count	Y	Y	X	
MI* 23 [,C]	Merge DMA count	Y	Y	X	
OT* 23 [,C]	Write DMA count	Y	Y	X	
[,C]	Clear FLG 20, FLG 21, and FLG 22				
SFC 24	Skip if DMA disabled (DMAEN asserted)	Y	Y	X	
SFS 24	Skip if DMA enabled (DMAEN not asserted)	Y	Y	X	
LI* 24	Read Scratch 1	Y	Y	X	
MI* 24	Merge Scratch 1	Y	Y	X	
OT* 24	Write Scratch 1	Y	Y	X	
LI* 25	Read Scratch 2	Y	Y	X	
MI* 25	Merge Scratch 2	Y	Y	X	
OT* 25	Write Scratch 2	Y	Y	X	
LI* 26	Read Scratch 3	Y	Y	X	
MI* 26	Merge Scratch 3	Y	Y	X	
OT* 26	Write Scrath 3	Y	Y	X	
SFC 30	Skip if FLG 30 clear	Y	Y	X	7
SFS 30	Skip if FLG 30 set	Y	Y	X	
CLF 30	Clear FLG 30	Y	Y	X	
STF 30	Set FLG 30	Y	Y	X	
STC 30 [,C]	Set CNTRL 30 issue DVCMD	Y	Y	X	
CLC 30 [,C]	Clear CNTRL 30	Y	Y	X	
LI* 30 [,C]	Read device data	Y	Y	X	
MI* 30 [,C]	Merge device data	Y	Y	X	
OT* 30 [,C]	Write device data	Y	Y	X	
[,C]	Clear FLG 30				
LI* 31	Read interface control word	Y	Y	X	
MI* 31	Merge interface control word	Y	Y	X	
OT* 31	Write interface control word	Y	Y	X	
LI* 32	Read interface status	Y	Y	X	8
MI* 32	Merge interface status	Y	Y	X	
OT* 32C	Reset interface status	Y	Y	X	9

Table 3-1. I/O Processor Chip Instructions by Select Code (Continued)

Instruction	Function	GR ON	GR = SC	IR = SC	Notes
SFC SC	Skip if FLG 30 clear	N	X	Y	7
SFS SC	Skip if FLG 30 set	N	X	Y	
CLF SC	Clear FLG 30	N	X	Y	
STF SC	Set FLG 30	N	X	Y	
STC SC [,C]	Set CNTRL 30 and issue DVCMD	N	X	Y	8
CLC SC [,C]	Clear CNTRL 30	N	X	Y	
LI* SC [,C]	Read device data	N	X	Y	10
MI* SC [,C]	Merge device data	N	X	Y	10
OT* SC [,C]	Write device data	N	X	Y	
[,C]	Clear FLG 30				

SC = Interface select code Y = yes N = no X = don't care

Notes:

1. The [,C] is always executed even if the primary instruction is not.
2. The SLAVE logic must be enabled; i.e., SLRQ LOW at power up.
3. FLG 20 is set by DMA upon completion of self-configured DMA block transfer which is not to be followed by another self-configuration.
4. FLG 21 is set by DMA upon completion of any block transfer which is not to be followed by a self-configuration.
5. FLG 22 is set by DMA if a parity error occurs during a DMA read.
6. FLG 23 is the logical OR of flags 20 through 22.
7. FLG 30 and CNTRL 30 are controlled by the Flag and Control flip-flops located in the I/O Processor chip.
8. The IOP chip indicates only that the select code is in the range 32 to 77; it is up to the user to decode any specific select code.
9. Serial I/O cards, by convention, use this instruction as a card reset.
10. When the IOP chip is in diagnose mode, these instructions fetch the following:
    Diagnose mode 1 – the interface's select code and ID word.
    Dagnose mode 2 – the Global Register and IOP Chip status bits.

HP-IB Bus Interface Section

The Interface Controller Chip (HP-IB Chip) is in the Bus Interface Section. This provides a high-speed interface between the I/O Processor Chip and the HP-IB bus. The sequence of control words sent to the HP-IB Chip's registers directs HP-IB operations. HP-IB data or status may be read from the HP-IB Chip's registers. Figure 3-2 shows a block diagram of the HP-IB Chip.

The HP-IB Chip's eight internal registers are accessed through a common 10-bit bus (HP-IB bus). The three register select inputs A13, A14, and A15 select the desired HP-IB Chip register. See "HP-IB Chip Register Definitions" at the end of this chapter for descriptions of these registers. A read/write input (WRITE, U117 pin 16) selects the direction of the data flow.

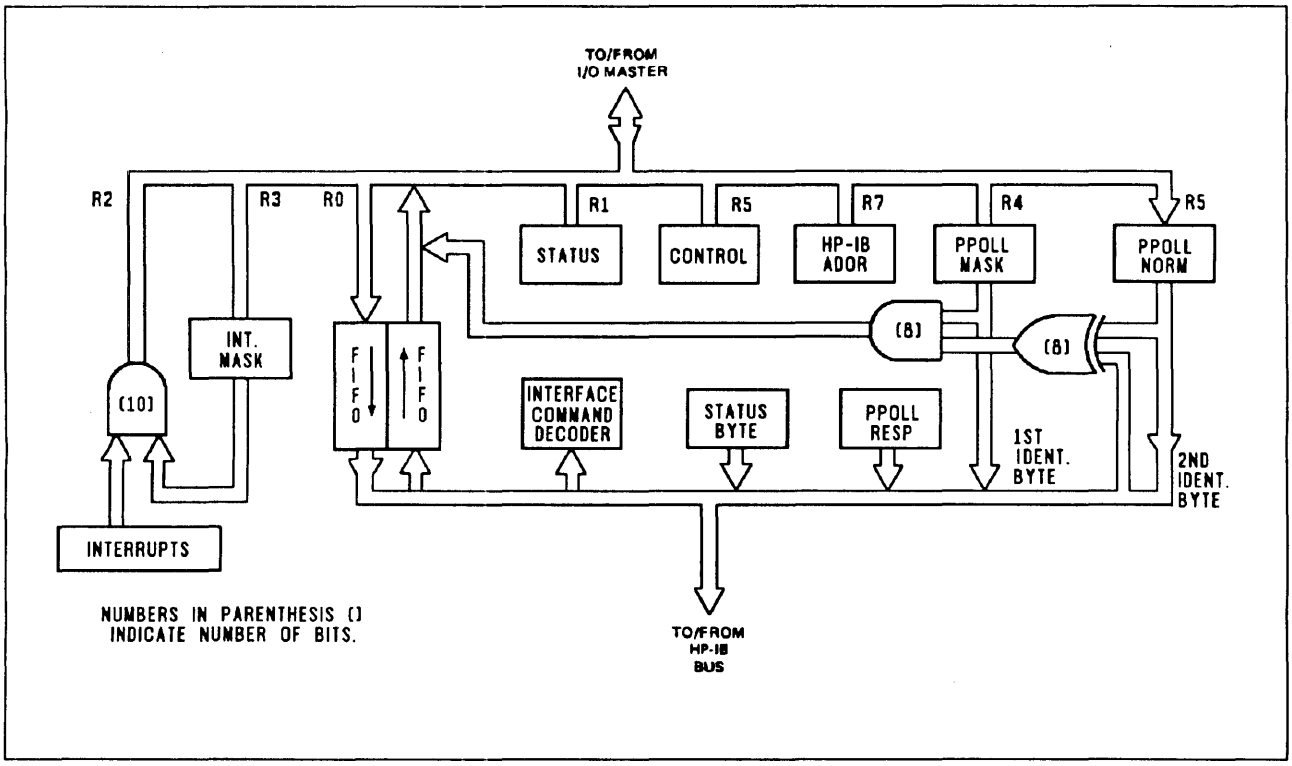


Figure 3-2. HP-IB Chip (U117) Block Diagram

This is the 16-bit format of words written to the HP-IB Chip:
(for bit 15, 1 = read from HP-IB Chip and 0 = write to HP-IB Chip)

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	R / W	HP-IB CHIP REGISTER SELECT			0	0	HP-IB CHIP DATA BUS									

Example

For a HP-IB REG SELECT and READ, bits of the input word are copies of those specified in the output word that selected the register to be read.

Program: OTA 30
STC 30
LIB 30

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
A =	1	HP-IB CHIP REGISTER SELECT			0	0	HP-IB CHIP DATA BUS									

SELECT REGISTER
(READ)
(OTA 30,C)

INITIATE READ
(STC 30,C)

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
B =	1	HP-IB CHIP REGISTER SELECT			0	0	HP-IB CHIP DATA BUS									

DATA READ
(LIB 30)

Register Descriptions

Registers 20 through 23 are located in the I/O Processor Chip and registers 30 through 32 are on the circuit board. The following lists the function of each register.

Data Register, Register 30 (OT*/LI*30)

The Data Register holds data to be written to or read from the HP-IB Chip. This includes HP-IB data and commands. The data word includes the read/write bit, three HP-IB Chip register select bits, and 10 bits of HP-IB Chip register data.

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	R / W	HP-IB CHIP REGISTER SELECT			0	0	DATA TO/FROM HP-IB CHIP									

To write a word:

1. OTA 30 – write select bit (bit 15 = 0), HP-IB Chip register selected, 10 bits of data placed in Write Data Holding Register.

2. STC 30 – handshake 10 bits of data from holding register into selected HP-IB Chip register. A copy is also written into the Read Data Register.

To read a word:

1. OTA 30 – read bit set, HP-IB Chip register selected, lower bits have no meaning.

2. STC 30 – handshake 10 bits from the selected HP-IB Chip register into the Read Data Holding Register.

3. LIA 30 – pick up 10 bits of data from card along with HP-IB Chip register number and read bit.

Control Register, Register 31 (OT*/LI*31)

Note

Do not try to change bits 11 and 12 of register 31 on the same write. Use consecutive writes to change these bits. Otherwise one of the bits may be latched in the wrong state.

The upper four bits duplicate the corresponding bits of the Data Register. This allows read/write and HP-IB Chip register selection during byte mode DMA.

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	READ	HP-IB CHIP REGISTER SELECT			FORCE	PACK	EOI	ATN	MSA	FRZ	NOT USED	SRQI	DELY	ENF	PPEN	CCLR

If set, the bits have the following meanings:

Bit No.	Meaning
15	1 = READ, 0 = WRITE
14–12	HP-IB Chip register select
11	Forced read on inbound FIFO flush
10	Byte packing mode
9	Send last HP-IB byte out tagged with EOI or terminate input DMA on End of Record (EOI or LF).
8	Set ATN on HP-IB bytes sent out, or terminate input DMA if My Secondary Address is received
7	Enable interrupt on My Secondary Address detection
6	Freeze DMA on interrupt
5	NOT USED
4	Enable SRQ interrupt (independent detection outside of HP-IB chip)
3	Delay start of DMA data transfer until interrupt condition exists (before masking by bit 2)
2	Enable card flag to be set (no effect on DMA completion interrupt)
1	Do parallel poll at end of current DMA operation (output only)
0	Clear card (except HP-IB Chip)

Status Register, Register 32 (LI*/OT*32)

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	PPEN	GET	EOI	MSA	FINT	FRZ	SRQ	DMARQ	U16 S1	U16 S2	U16 S3	U16 S4	U16 S5	U16 S6	U16 S7	U16 S8

If set, the bits have the following meanings:

Bit No.	Meaning
15	Parallel poll in effect for at least 7 microseconds
14	Group Execute Trigger (GET) received
13	End of Record (EOI or Line Feed) received
12	My Secondary Address (MSA) received
11	HP-IB Chip interrupt request
10	DMA operation frozen
9	HP-IB service request (SRQ)
8	HP-IB Chip requesting transfer (DMARQ)
7–0	Reflects the setting of HP-IB address select switches, U144S1 through U144S8

When an OT* 32 is executed, the MSA bit (bit 12) is cleared but all other bits remain unchanged.

DMA Self-Configuration, Register 20

The DMA Self-Configuration Register contains the address of the DMA triplets or quadruplets. If bit 7 is set, it indicates a quadruplet, otherwise it is a triplet. A DMA triplet (see figure 3-3) is of the form: controls bits, transfer address, and word/byte count. The triplet words are the words to be used in registers 21, 22, and 23, respectively. A DMA quadruplet (see figure 3-3) is of the form: control bits, card control word, transfer address, and word/byte count. These quadruplet words are to be put into registers 21, 31, 22, and 23, respectively.

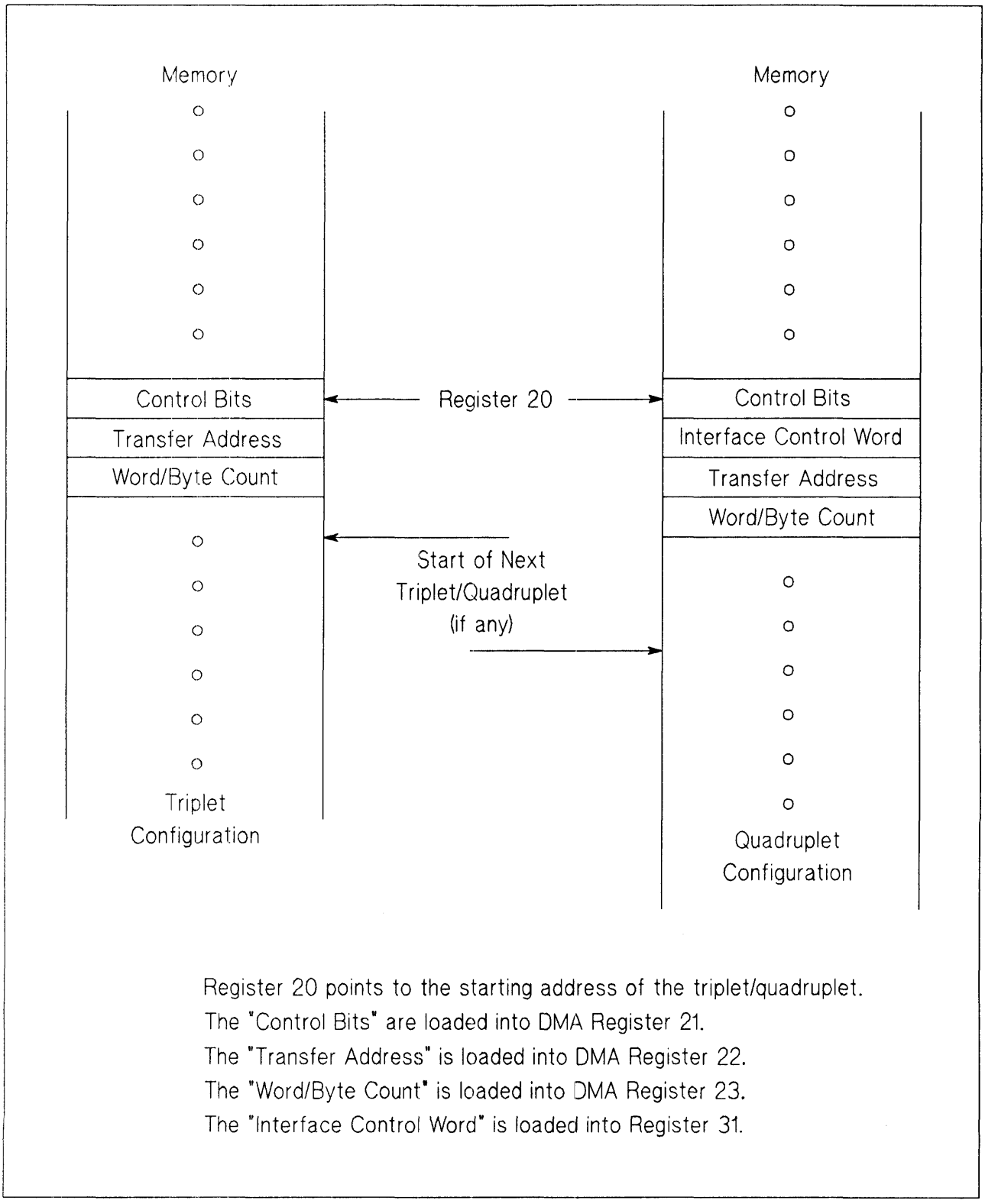


Figure 3-3. DMA Self-Configuration Formats

DMA Control Word 1, Register 21

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CONT	DVCMD	BYTE	RES	CINT	REM	FOUR	AUTO	IN	RESERVED						

The bits have the following meanings:

Bits 0-6: Reserved

Bit 7: IN

1 = The direction of the data transfer is from the HP-IB card to memory.

0 = The direction of the data transfer is from memory to the HP-IB card.

Bit 8: AUTO

Meaning is based on the setting of bit 7 (IN) .

1 = Last input transfer will be followed by a DVCMD pulse.

0 = The last DVCMD pulse will be suppressed.

Bit 9: FOUR

1 = There are four words to be fetched for the current DMA configuration. Loads register 31 as part of the DMA quadruplet.

0 = There are three DMA Control Words to be fetched for the current DMA configuration. Register 31 must be loaded before triplet.

Bit 10: REM Remote Memory

Note

HP 1000 A-Series computers do not have remote memory. Attempts to use it may cause loss of data.

1 = All memory requests will be accomplished by the REMEM (Remote Memory) signal, which disables standard memory and enables remote memory.

0 = Remote memory not enabled.

Bit 11: CINT Completion Interrupts

1 = Inhibits DMA transfer completion interrupts.

0 = Completion interrupt is to be requested by DMA logic when work/byte count rolls over (goes from –1 to 0).

Bit 12: RES Residue

1 = If DMA is enabled to self-configure (a STC 20 has been executed), DMA will write its word/byte count residue into the location from which it read the word/byte.

0 = Word/byte count is not written.

Bit 13: BYTE

1 = The DMA transfer is to be conducted in byte mode. Each data transfer is counted as one byte. Byte mode transfers are packed, two bytes per work, with the left byte (bits 15-9 of the data word) transferred first.

0 = Each data transfer will be a full 16-bit word.

Bit 14: DVCMD Device Command

1 = DMA control logic will issue a Device Command (MVCMD) signal immediately following each data transfer from the interface logic.

0 = Device Command is not issued.

Bit 15: CONT Control

1 = If an STC 20 has been executed, then at the end of a DMA transfer the I/O Processor Chip will fetch the next set of DMA control words and reconfigure itself to start a new transfer.

0 = DMA will stop at the end of the current transfer.

DMA Address, Register 22

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		NEXT DMA MEMORY ADDRESS														

DMA Control Word 2 is the 15-bit (bits 0-14) address of the next memory location to be accessed by DMA. The most significant bit (bit 15) cannot be controlled by OTA 22 or OTB 22 and will be the complement of control word 1, bit 7 (IN) when fetched by an LIA 22.

DMA Word/Byte Count, Register 23

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DMA WORD/BYTE COUNT															

The Word/Byte Count Register is a 16-bit register whose value is the two's complement of the number of data elements to transfer. A data element may be either a word or a byte, as indicated by bit 13 (BYTE) of the DMA Control Word, contained in register number 21.

The end of a data transfer is indicated by the transition of the word/byte count register's value from –1 to 0. Rollover from 177777 octal to 000000 occurs at this same time. This allows up to 65,536 data elements to be transferred at once. The memory size (32,768 words maximum) limits a word transfer to a length of 32,768 words or 65,536 bytes. The hardware does not detect this, however, so it is up to the programmer not to exceed this limit.

Summary

Figure 3-4 is a summary of these word formats.

Data Register, Register 30

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Computer Bit Number
---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	HP-IB Chip Bit Number
R/W	HP-IB REGISTER SELECT			0	0	HP-IB DATA BUS										

1 = read from HP-IB Chip

2 = write to HP-IB Chip

Control Register, Register 31 (OT*/LI*31)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Computer Bit Number
---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	HP-IB Chip Bit Number
READ	HP-IB REGISTER SELECT			FORCE	PACK	EOI	ATN	MSA	FRZ	not USED	SRQI	DELY	ENF	PPEN	CCLR	

Status Register, Register 32 (LIA 32)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Computer Bit Number
---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15	HP-IB Chip Bit Number
PPEN	GET	EOI	MSA	FINT	FRZ	SRQ	DMARQ	U16 S1	U16 S2	U16 S3	U16 S4	U16 S5	U16 S6	U16 S7	U16 S8	

DMA Control Word 1, Register 21 (Bit 14 must be 1 and bits 8 and 13 must be 0)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Computer Bit Number
CONT	DVCMD	BYTE	RES	CINT	REM	FOUR	AUTO	IN	RESERVED							

DMA Address, Register 22

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Computer Bit Number
	NEXT DMA MEMORY ADDRESS															

DMA Word/Byte Count, Register 23

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Computer Bit Number
DMA WORD/BYTE COUNT																

Figure 3-4. Word Format Reference Summary

Programmed Input/Output

For programmed input and output, address the card through the Global Register and proceed as follows:

OTA/B STC	30 30,C	Send commands and data over HP-IB and program HP-IB Chip's registers.
STC LIA/B	30,C 30	Read commands and data from HP-IB and read back HP-IB Chip register contents from a previously specified register.
OTA/B LIA/B	31 31	Program card Control Register. Read back card Control Register.
LIA/B	32	Read card Status Register.
OTA/B	32	Clear secondary address bit in status word.

Direct Memory Access (DMA)

DMA allows complete control of the interface card and the HP-IB. DMA operation offers the following advantages:

- Two control words can be sent, a DMA Control Word and a Card Control Word.
- Transmission log (the actual number of bytes/words transferred) can be automatically returned to the user at the completion of a DMA operation.
- The Card Control Word specifies initial conditions and alternate terminating conditions besides the exhausted count.
- Multiple DMA operations can be stacked and executed in sequence without further software intervention.
- The DMA completion interrupt occurs only at the end of a series of stacked DMA operations.
- The card can terminate the sequential execution of stacked operations upon error detection.
- If so specified in the Card Control Word of the DMA quadruplet, the card can conduct a parallel poll at the completion of the current DMA operation before allowing the DMA program to proceed. If a selected interrupt occurs, DMA operation can be frozen by the card.

Any given card has a maximum DMA rate. In order to achieve this maximum rate, there can be no other requests on the backplane. Usually there are other transactions on the backplane which degrade the maximum DMA rate. When the processor decides to fetch an instruction while an interface card is preparing for DMA, that DMA cycle can be held off for 908 nanoseconds. If an interface card is in the highest priority slot, it can be held off by the processor or by a lower priority card doing DMA. The worst case is 454 milliseconds per transfer. All DMA rate specifications given in chapter 1 assume the card is plugged into the highest priority slot. When plugged into a lower priority slot, DMA rates cannot be guaranteed when the additive rates of the higher priority cards are capable of consuming the total backplane bandwidth (2.72 Mbytes). Usually, however, even in a busy system, the backplane is only fully congested for very short periods of time, so that even the lowest priority I/O cards transfer at rates close to their nominal specifications.

Types of DMA Transfers

Direct Memory Transfer is implemented in either word or byte mode. In word mode, each data transfer uses a full 16-bit word. In byte mode, transfers are packed, two bytes per word.

Output (writes):

Word mode allows direct programming of the HP-IB Chip and transfer over the HP-IB.

Byte mode allows the transfer of bytes over the HP-IB in the Data or Command Mode as specified by the Card Control Word. EOI can be automatically appended to the last byte.

Input (reads):

In word mode, immediate or delayed read of the HP-IB Chip register is specified in the DMA Control Word. A delayed read is initiated only when an HP-IB Chip interrupt is detected by the card.

Byte mode reads data from the HP-IB. The two high order bits of the HP-IB bus are monitored for data termination conditions (EOI or Line Feed) or ATN. The Card Control Word specifies the termination conditions.

DMA Control and Status Words

Software DMA set-up and control involves seven control and status words. The following registers are used:

DMA Register Number 20, DMA Self-Configuration Register, In or Out
DMA Register Number 21, DMA Control Register, In or Out
DMA Register Number 22, DMA Address Register, In or Out
DMA Register Number 23, Word/Byte Count Register, In or Out
DMA Register Number 30, Data Register, In or Out
DMA Register Number 31, Card Control Word Register, In or Out
DMA Register Number 32, Card Status Word Register, In

See "Register Descriptions" in this chapter for full descriptions of these registers.

DMA Transfer Operation

Start a DMA transfer by configuring the DMA Control Register, DMA Address Register, Word/Byte Count Register, and the Output Control Word Register. Then issue an STC instruction to the DMA Control Register.

DMA Input Transfer

A DMA input transfer moves data from the HP-IB card to memory. If the transfer is in word mode, a Device Command (DVCMD) Signal and a Memory Access Signal are generated immediately. If the transfer is in byte mode, the DMA control logic responds to the HP-IB card only with a DVCMD signal. When the second byte transfer is requested, the memory write request is generated. The memory request goes directly to the backplane where memory access priority is determined by the location of the requesting card with respect to the processor card (the closer the card is to the processor, the higher the card's priority). When the memory access request is granted, the data is transferred, the DMA Word/Byte Count, and DMA Address Registers are incremented, and the DMA control logic is ready to accept another data transfer request.

DMA Output Transfer

A DMA output transfer moves data from memory to the HP-IB card. For an output transfer, a memory access request is generated immediately. As soon as the data is available from memory, it is passed to the HP-IB card. The data is followed by a Device Command (DVCMD) Signal. In byte mode, the byte indicator signal is changed and another DVCMD signal is generated when the HP-IB Chip indicates that it is ready to accept more data.

DMA Transfer Termination

A DMA data transfer continues until one of the following terminating condition is detected:

- Word count transition from –1 to 0. (Rollover from 177777 octal to 000000.) This indicates that all the data elements have been transferred.
- Detection of a Control Reset (CRS) Signal. This signal is generated by the processor card during its power-up sequence, or by execution of a CLC 0 instruction.
- Parity error indication from memory.
- Assertion of LSBYT.

DMA Self-Configuration Feature

DMA registers can be loaded directly from sequential memory. Upon completion of each successive DMA operation, register 20 is used as a pointer to the location in memory containing the next set of values to be loaded. As each register is loaded, register 20 is incremented so it will point to the next value to be loaded.

DMA Self-Configuration Initialization

Initialize the DMA self-configuration feature by setting the value of register 20 to the memory address of the first word of a list of DMA triplets or quadruplets. Figure 3-3 illustrates the formats of both the triplets and quadruplets. Bit 8 of the Control Word is used with both.

Start the feature with an STC to register 20. This STC instruction will simultaneously set the control on registers 20 and 21 to achieve an initial state for full execution.

DMA Self-Configuration Operation

After receiving the STC instruction from register 20, the self-configuration control logic fetches the word addressed by the contents of register 20 and loads this word into register 21.

Assume bit 7 of this word is set. This signifies a quadruplet. The contents of register 20 are incremented during the memory access. The new value of register 20 is used as the address of the next memory read. This next word is loaded into the Control Register with a virtual OTA 31 generated by the I/O Processor chip. Then register 20 is incremented for the next read and this new data is loaded into register 22. Register 20 is again incremented. The new value of register 20 is used to address the fourth word of the current quadruplet. This fourth word is loaded into register 23. The value of register 20 is again incremented, pointing to the beginning of the next triplet/quadruplet.

As soon as the interface is ready, the DMA operation starts. If bit 11 of register 21 is clear when the DMA operation terminates, an interrupt request is generated. If the DMA operation terminates due to an end-of-transfer indication from the interface or a word/byte count transition from –1 to 0, and bit 12 of register 21 is set, the DMA self-configuration logic writes the word-count residue into the location formerly occupied by the current DMA operation's word/byte count. Operation of the self-configuration feature is continued for the next triplet/quadruplet.

DMA Self-Configuration Termination

The operation of the DMA self-configuration feature continues until one of the following occurs:

- A CLC instruction to register 20 is executed. This stops the self-configuration logic from advancing its pointer to the next triplet while allowing the current DMA to continue. An STC instruction to register 20 allows the self-configuration feature to continue.
- A CLC instruction to register 21 is executed. This stops the current DMA operation at its present state of operation.
- A CLC instruction to register 22 is executed. This aborts the current DMA operation and causes the self-configuration logic to advance to the next triplet/quadruplet. No interrupt is generated by the aborted transfer.
- A CLC instruction to register 23 is executed. This stops the operation of the self-configuration logic and aborts the transfer in progress.
- The first word of a triplet is read with CONT bit 15 (DMA Control Word 1) clear, indicating that there are no more DMA triplets. This sets the flag on register 20, which generates an interrupt request if the control flip-flop of register 20 is set.

Byte Mode Transfers

Card Control Word for Byte Mode Transfers

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	---	A13	A14	A15	---	---	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	R/W	0	0	0	0	1	EOI	ATN	CONTROL							

FIFO SELECTED PACK

Specify HP-IB bus bits D0 and D1 on output. On input, monitor D0 and D1 for end of record or secondary address.

Byte Mode DMA Input

[EOI,ATN] = 00. HP-IB bits D8 to D15 are written into memory without monitoring D0, D1. End of Record (D0, D1 = 11) and My Secondary Address (D0, D1 = 01) will not be detected.

[EOI,ATN] = 10. Upon detecting an End of Record (D0, D1, = 11), the DMA input operation is terminated.

[EOI,ATN] = 01. Upon detecting a secondary address, the input DMA operation is terminated.

[EOI,ATN] = 11. Terminates input DMA operation on last byte or secondary address.

To input data, the lower 8 bits of the HP-IB bus are packed, two bytes per computer word. The first byte is the first order byte.

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FIRST BYTE								SECOND BYTE							

Byte Mode DMA Output

Depending on the value of the two least significant bits (Bit 9 EOI or Bit 8 ATN) of the first control byte, the unpacked data words are output on the HP-IB bus as follows:

[EOI,ATN] = 01

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	0	1	FIRST BYTE							

0	1	SECOND BYTE

Note If addressing the outbound FIFO, the bytes packed in memory are sent as command bytes (ATN = true) over the HP-IB.

[EOI,ATN] = 10

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	0	0	FIRST BYTE							

0	1	SECOND BYTE

1	0	LAST BYTE

The last data byte will be tagged with EOI.

[EOI,ATN] = 00

HP-IB bits 0 and 1 will be output as zero. Last byte will not be tagged with EOI. The bytes will be output as HP-IB data.

[EOI,ATN] = 11

HP-IB bit 1 will be set. Bit 0 will be set on the last byte. Note that in this case, bytes go out as commands over the HP-IB, and the last one is interpreted as a byte count by the HP-IB Chip (see "Register 0, Outbound FIFO, Byte Transfer Enable" near the end of this chapter).

Word Mode Transfers

In word mode, the lower 10 bits of the computer word correspond to the HP-IB bus. The corresponding HP-IB register address along with the READ/WRITE bit are the most significant bits of the computer word.

Since the HP-IB bus and FIFOs are 10 bits wide, provision must be made to specify the two higher bits not included in the 8-bit byte on output and to monitor these two bits on input. The handling of these two extra bits is specified in the HP-IB control byte of the Card Control Word. (See "DMA Control, Card Control Word" in this chapter.)

DMA Control

DMA Control Word 1 (LI* 21 or OT* 21)

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CONT	DVCMD	BYTE	RES	CINT	REM	FOUR	AUTO	IN	RESERVED						

The DEVICE COMMAND (bit 14) must always be set (DVCMD = 1). The DMA will then automatically issue device commands equivalent to the STC,C instruction of programmed I/O.

The AUTO (bit 8) must always be clear (AUTO = 0). The card will request the first data output transfer when ready.

Card Control Word

Computer Bit No.	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ	HP-IB CHIP REGISTER SELECT			FORCE	PACK	EOI	ATN	MSA	FRZ	NOT USED	SRQI	DELY	ENF	PPEN	CCLR

The card control word also affects DMA operation.

Byte mode (bit 10):

If byte packing is used (BYTE bit = 1 in DMA Control Word 1), the card control word must have the PACK bit set (bit 10 = 1).

Start delay (bit 3):

If the DELAYED START of the Card Control Word is set, the first data exchange of a DMA operation is delayed until an unmasked interrupt condition occurs on the card as follows:

1. INT from HP-IB Chip (positive paralle poll response, SRQ, status change, outbound FIFO empty, etc.)
2. Group Execute Trigger.
3. SRQ detected on the HP-IB bus.

Note Bit 2, which enables setting the card's flag, need not be set.

EOI (bit 9):

If set and a byte tagged with EOI or a Line Feed character (if its detection was enabled in the HP-IB Chip) is read into memory, the DMA operation is terminated regardless of byte/word count. On output, this bit specifies that the last byte sent should be tagged with EOI.

ATN (bit 8):

If set and a secondary address is read into memory, the input DMA operation is terminated regardless of the byte/word count. On output, the bytes are sent out as commands (ATN set).

Freeze DMA on Interrupt (bit 6):

If set and an unmasked HP-IB Chip interrupt, SRQ, secondary address or a Group Execute Trigger is received, DMA operation will freeze (cease without terminating). Interrupts should be enabled to flag the user. The freeze condition is reflected in the card status word (LIA 32).

Forced Read (bit 11):

Allows an 8 byte DMA read to flush the inbound FIFO even if fewer bytes are present. It can be used after data inputs uncounted by the HP-IB Chip which might have left an unknown number (0-8) of unwanted bytes in the inbound FIFO.

Do Parallel Poll (bit 1):

If set, a parallel poll is allowed to take place about 7.5 microseconds prior to terminating an output DMA operation. This opens windows during self-configured multiple DMA operation to allow PP response detection. Be careful not to use this bit if an uncounted request will be left in the out-bound FIFO preventing the execution of PP.

HP-IB Chip FIFO DMA Programming

To properly manage the DMA transfers into the HP-IB Chip's inbound or outbound FIFOs, the HP-IB Chip's Control Register (register 6) FIFO select bit must be programmed as follows:

i.e.	2	6	0	0	0	2	(Octal) Prior to Output
	0	6	0	0	0	0	(Octal) Print to Input

For performing other functions, other bits may have to be programmed.

Example

For a DMA programming example, see table 3-3 in a following section entitled "Programming Examples".

HP-IB Card Programming Characteristics

Initialization (Power On and I/O Clear)

On initial power-up, or in response to CRS/CLC 0, the following occurs:

- The interface card goes offline from the HP-IB.
- The card is not a controller, talker, or listener.
- DMA: idle
- Card Control Word: all zeros
- HP-IB Interrupt Mask: all zeros (no interrupts)
- Parallel Poll Mask: all zeros (no response)
- Parallel Poll Sense: all zeroes
- FIFO Buffer Contents: undefined.

System Controller and Controller-In-Charge

Note

An operating system is the executive of a computer, supervising and controlling all internal and external processes. The I/O is one of these processes. When interfacing with the HP-IB, RTE becomes the controller of the interface bus in order to properly coordinate with several possible on-going I/O functions on other interfaces. In this respect, RTE prohibits the use of "pass control" on its HP-IB interface.

The System Controller switch (U1S1) on the card must be set before power up if the card is to be programmed as a System Controller of the HP-IB. If the switch is set later, then CRS/CLC 0 or PON must be sent to the card, or the HP-IB Chip must be programmed OFFLINE, then ON-LINE again (register 7). Register 1, bit 11 can be read to verify that the HP-IB Chip is acting as System Controller.

If the System Controller switch (U1S1) is set, indicating Controller-in-Charge, the software must first program the HP-IB chip ONLINE by setting bit 8 in register 7. The IFC (Interface Clear) message must then be sent over the HP-IB for a least 100 microseconds to clear the bus and make the card the Controller-in-Charge. This is accomplished by setting bit 11 of register 6. (Refer to the programming example, table 3-2.)

Bus Controller Device

Before placing the card online, the HP-IB address should be written into register 7. The address may be found in the lower eight bits of the Status Register. The default address is 36.

The software should enable the card interrupts to be alerted if:

- A Device Clear or Group Execute Trigger Command is received.
- The HP-IB Chip status changes (Take Control Message is received).
- A byte is received in the inbound FIFO.

Interrupts

Interrupts vector to the memory location corresponding to the select code programmed by the select code switches, U1S3 through U1S8. The interrupt requests may be generated from the following areas:

- I/O Chip DMA completion.
- Reception of a Group Execute Trigger from the HP-IB.
- An HP-IB SRQ (Service Request) detected independently of the HP-IB chip.
- One of nine maskable HP-IB Chip status conditions:
  - An affirmative response to a parallel poll exists.
  - An HP-IB device is requesting service through an ARQ.
  - A DEVICE CLEAR interface message has been received from the HP-IB controller.
  - The REMOTE/LOCAL or CONTROLLER-IN-CHARGE status of the HP-IB Chip has been changed by the System Controller.
  - A parity error was detected in an HP-IB command received over the bus.
  - The outbound FIFO is not full.
  - The inbound FIFO is not empty.
  - Both FIFOs are idle and outbound FIFO is empty.
  - There was an attempt to write into a full FIFO or to read from an empty FIFO.

Card Flag Interrupts

If bit 2 of the Card Control Word is set, the card's flag will be set when:

- A Group Execute Trigger is received when the card is not the Controller-In-Charge.
- SRQI (bit 4) of the Card Control Word is set and an SRQ exists on the bus.
- MSA (bit 7) of the Card Control Word is set or a secondary address is read into the computer.
- An HP-IB Chip interrupt occurs. (These are maskable within the HP-IB Chip.)

The HP-IB card's flag may be tested by SFS/SFC select code/30. If the Interrupt System and Mask are on and the card's control is STC s.c./30, setting the flag generates an interrupt.

If the flag is set, software can find the cause by reading the Status Register (LIA32) and if necessary the HP-IB Chip's Interrupt Register (register 2).

Programming Examples

Non-DMA Transfer Example

The program shown in table 3-2 initializes the card, asserts remote enable, and leaves the HP-IB Chip in the parallel poll state. This is done with a non-DMA I/O transfer.

DMA Transfer Example

The example shown in table 3-3 gives the self-configuring DMA quadruplets and buffers required to do a Status and DSJ read from the HP 7902 Disc. This sequence must be performed after turning on the HP 7902 or inserting the cartridge.

Table 3-2. Non-DMA Transfer Example

```
PAGE 0009 #01                                        6:32 PM FRI., 19 JAN., 1979
     INITIALIZATION OF CARD AS A CONTROLLER

0150    02000                    ORG 2000B
0151*SET-UP HP-IB
0152    02000  062026  START     LDA SC
0153    02001  103602            OTA 2,C          SET UP GLOBAL REG. FOR HP-IB CARD
0154    02002  107723            CLC DMACT,C      RESET DMA MACHINE
0155    02003  062027            LDA ONL          PLACE CARD ON-LINE
0156    02004  102630            OTA DREG
0157    02005  103730            STC DREG,C
0158    02006  062030            LDA AIFC         ASSERT
0159    02007  102630            OTA DREG            IFC
0160    02010  103730            STC DREG,C
0161    02011  060103            LDA M100            FOR
0162    02012  002006            INA,SZA               >100
0163    02013  026012            JMP *-1                 MICROSEC.
0164    02014  062031            LDA SETUP        REMOVE IFC, ASSERT REN
0165    02015  102630            OTA DREG
0166    02016  103730            STC DREG,C
0167    02017  062032            LDA SETUP+1      PROGRAM PARALLEL POLL MASK FOR DI01
0168    02020  102630            OTA DREG
0169    02021  103730            STC DREG,C
0170    02022  062033            LDA SETUP+2      PROGRAM INTERRUPT MASK FOR PP & SRQ
0171    02023  102630            OTA DREG
0172    02024  103730            STC DREG,C
0173    02025  026052            JMP STOP

0175    02026  000037  SC        ABS SCODE
0176    02027  070200  ONL       ABS WRITE+ADRS+ONLIN
0177    02030  060021  AIFC      ABS WRITE+CNTRL+IFC
0178    02031  060040  SETUP     ABS WRITE+CNTRL+REN
0179    02032  040001            ABS WRITE+PPMSK+PPRO
0180    02033  031060            ABS WRITE+INTON+PPR+SRQ
```

Table 3-3. DMA Transfer Example

```
PAGE 0017 #01                                        6:32 PM FRI., 19 JAM., 1979
    DSJ & STATUS

0441    02500                   ORG 2500B
0442*DSJ & STATUS REQUEST
0443*DMA PROGRAM : 4 QUADRUPLETS
0444    02500   002501  DSJP    DEF * +1
0445    02501   141000          ABS CONT+CONT+DVCMD+WORD+FOUR+OUT
0446    02502   000000          ABS WRITE
0447    02503   002540          DEF DSJ
0448    02504   177770          ABS DSJ-RDDSJ
0449*
0450    02505   161200          ABS CONT+CONT+DVCMD+BYTE+FOUR+IN
0451    02506   102000          ABS READ+READ+PACK
0452    02507   002550          DEF RDDSJ
0453    02510   177777          DEC -A
0454*
0455    02511   141000          ABS CONT+CONT+DVCMD+WORD+FOUR+OUT
0456    02512   000000          ABS WRITE
0457    02513   002551          DEF STATUS
0458    02514   177762          ABS STATS-RDSTS
0459*
0460    02515   061200          ABS DVCMD+BYTE+FOUR+IN
0461    02516   102000          ABS READ+READ+PACK
0462    02517   002567          DEF RDSTS
0463    02520   177774          DEC -4
0464*
0466    02540                   ORG 2540B
0467*DSJ & STATUS REQUEST
0468*HP-IB & CARD PROGRAM
0469    02540   060042  DSJ     ABS WRITE+CNTRL+DMAOT
0470    02541   000476          ABS WRITE+FIFO+MLA
0471    02542   000507          ABS TLKA+FLPYA
0472    02543   000560          ABS MSA+20B
0473    02544   001001          ABS RCVRQ+1
0474    02545   000537          ABS UNT
0475    02546   000477          ABS UNL
0476    02547   060040          ABS WRITE+CNTRL+DMAIN
0477    02550   000000  RDDSJ   NOP                  RETURNED DSJ IN UPPER BYTE
0478    02551   060042  STATS   ABS WRITE+CNTRL+DMAOT
0479    02552   000536          ABS WRITE+FIFO+MTA
0480    02553   000447          ABS LSTNA+FLPYA
0481    02554   000550          ABS MSA+10B
0482    02555   000003          ABS STATD
0483    02556   001000          ABS UNITO+EOI
0484    02557   000477          ABS UNL
0485    02560   000476          ABS MLA
0486    02561   000507          ABS TLKA+FLPYA
0487    02562   000550          ABS MSA+10B
0488    02563   001004          ABS RCVRQ+4
0489    02564   000537          ABS UNT
0490    02565   000477          ABS UNL
0491    02566   060040          ABS WRITE+CNTRL+DMAIN
0492    02567   000000  RDSTS   NOP
0493    02570   000000          NOP      4 STATUS BYTES RETURNED
```

HP-IB Chip Register Definitions

The eight addressable registers within the HP-IB Chip perform the following functions:

Register 0: FIFO's

Two First-In-First-Out queues used for transferring bytes over the HP-IB. One FIFO is for inbound data transfer and the other is for outbound data transfer.

Register 1: Status

Contains the values of non-interrupting internal HP-IB Chip status conditions.

Register 2: Interrupting Conditions

Contains the values of nine interrupting status conditions plus a tenth bit which is the "OR" of the others. When this tenth bit is a "1", the host processor is interrupted by the HP-IB Chip.

Register 3: Interrupt Mask

A register whose bits are used to mask off (force to "0") corresponding bits of register 2.

Register 4: Parallel Poll Mask/First ID Byte

Within an HP-IB controller, the bits of this register mask corresponding DIO line responses to a parallel poll. Within a non-controller, they are used as the first byte of a two-byte sequence which optionally can be used to identify the type of device that contains the HP-IB Chip.

Register 5: Parallel Poll Sense/Second ID Byte

Within an HP-IB controller, bits of this register inform the HP-IB Chip which assertion level is being used on each DIO line to indicate a need for service during a parallel poll. Within a non-controller, they are used as the second byte of a two-byte sequence which optionally can be used to identify the type of device that contains the HP-IB Chip.

Register 6: Control

Contains the control bits accessible to the host processor that allow it to determine internal HP-IB Chip states.

Register 7: Address

A register through which the host processor can inform the HP-IB Chip which HP-IB address to use for communication, as well as a few other essentials.

The basic structure of the HP-IB Chip is shown in figure 3-2. More detailed information about these eight registers follows.

Register 0, Outbound FIFO/Inbound FIFO

Outbound FIFO

With a write to register 0, a word is placed into an eight-word-long outbound FIFO queue. This FIFO holds data bytes waiting to be sent over the HP-IB to other devices. Within HP-IB controllers, it is also used to hold interface commands and control words that regulate the sending of data bytes by other devices on the HP-IB.

If the outbound FIFO is full during any attempt to write into it, the handshake with the host processor will be completed without destroying any data already in the FIFO, and the PROCESSOR HANDSHAKE ABORT bit (bit 9) in register 2 will be set. An aborted attempt to write into the outbound FIFO can be repeated until the word is finally accepted by the HP-IB Chip.

As each word reaches the HP-IB end of the outbound FIFO, it is interpreted by the HP-IB Chip to allow one or more bytes to be transferred over the HP-IB. It is automatically removed from the FIFO at the completion of this transfer allowing the next word sequence to be interpreted.

If a non-controlling device containing a HP-IB Chip is addressed to talk and is expected to send data bytes but its outbound FIFO is empty, the HP-IB will remain idle until the host processor places a data byte into the FIFO. If either the DATA FREEZE bit in register 1 or the DEVICE CLEAR bit in register 2 is set, the HP-IB Chip will refuse to send data bytes, even if they exist in the outbound FIFO, until the host processor resets that bit.

Within an HP-IB controller, the DATA FREEZE and DEVICE CLEAR bits cannot be set. If either bit happens to already be set within a device at the time it becomes the HP-IB controller, the HP-IB Chip will not allow any byte transfer over the HP-IB until the host processor resets that bit.

Within the HP-IB controller, if the PARALLEL POLL RESPONSE INTERRUPT MASK (bit 10 in register 3) is set and the controller's outbound FIFO is empty, the HP-IB Chip conducts a continuous parallel poll. Polling continues until a "0" is written into bit 10 of register 3 or a word is placed in the outbound FIFO by the host processor. This poll terminates as soon as the next word is placed into the outbound FIFO by the host processor. The PARALLEL POLL RESPONSE interrupt (bit 10) in register 2 alerts the host processor that at least one device is indicating a need for service during this poll. See the definition for register 2, bit 10 for more details.

The HP-IB Chip provides two interrupts to help the host processor coordinate outbound FIFO activity. One interrupt indicates that the FIFO has room for more words. The other interrupt shows when the FIFO is completely empty.

The outbound FIFO is initialized to an empty state when the PON input pin is set to a low value and whenever a "1" is written into the INITIALIZE OUTBOUND FIFO bit (bit 15) in register 6.

Within an HP-IB controller, if bit 10 of register 3 is a "1", and the INITIALIZE OUTBOUND FIFO bit is used while the ATN line is false on the HP-IB, the ATN line will be asserted asynchronously. If this occurs while a data byte is being sent, one or more devices may interrupt the data as a "phantom" Interface Command. This situation should be avoided since it requires that the HP-IB controller bring all HP-IB devices to a known state by sending a long string of interface commands. In all other situations, the HP-IB Chip will assert ATN synchronously following any data transfer, eliminating the chance for a "phantom" Interface Command.

Within a non-controlling device, all words written into the outbound FIFO contain a single data byte to be sent over the HP-IB. Within an HP-IB controller, a word written into the outbound FIFO can be one of three types:

- A Data Byte to be sent over the HP-IB.
- An Interface Command to be sent over the HP-IB.
- A Byte Transfer Enable to allow another device to send bytes over the HP-IB.

Data Byte:

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	END	0	DATA BYTE VALUE							

When a data byte code reaches the HP-IB end of the outbound FIFO, it is sent over the HP-IB along with its associated END bit value to all currently addressed listeners.

Within a non-controlling device, data bytes are sent over the HP-IB only if the device is addressed to talk and the HP-IB controller has allowed a byte transfer to take place. If these two conditions are not met when a data byte reaches the end of the FIFO, it is held there until they are met.

Within an HP-IB controller, the data byte will be sent over the HP-IB as soon as it reaches the end of the FIFO. The host processor must guarantee that it is addressed to talk at this time and is not in Serial Poll Mode. Otherwise, the data byte code will be erroneously interpreted as a Byte Transfer Enable.

Interface Command: (HP-IB controller only)

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	0	1	0	INTERFACE COMMAND CODE						

When this word reaches the HP-IB end of the outbound FIFO, the Interface Command byte is sent over the HP-IB to all devices on the bus. During this transfer, the HP-IB Chip automatically sets the value of DIO8 to generate the correct odd or even parity on the HP-IB, depending on the value of bit 1 in register 7 ("0" = odd and "1" = even).

Byte Transfer Enable: (HP-IB controller only)

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	LF INH	0	BYTE COUNT							

Note

An HP-IB controller can also use a Byte Transfer Enable to obtain its own Serial Poll response byte or Identification Code bytes for self-diagnosis.

Uncounted Transfer Enable:

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	1	1	0	0	0	0	0	0	0	0

After addressing another device to talk, the host processor should place a Byte Transfer Enable into its own outbound FIFO to remove the ATN signal from the HP-IB and allow bytes to be sent to all addressed listeners. The HP-IB Chip will automatically terminate this transfer when:

- A byte is sent with its accompanying END bit.
- An ASCII Line Feed Character (hex 0A) is sent during a counted transfer whose LF INH (Line Feed Inhibit) bit is "0".
- The number of bytes specified by a BYTE COUNT field have been sent. An all-zero BYTE COUNT field is used to specify a 256-byte transfer.

An HP-IB controller must guarantee either that it is not addressed to talk or that it is in Serial Poll Mode when a Byte Transfer Enable reaches the end of the FIFO. Otherwise, it will be erroneously interpreted as a data byte.

Note

If bits 8 through 15 of an Uncounted Transfer contain a non-zero value, they will be interpreted as a Byte Count field and counting will be performed in spite of the higher-order "11" code.

Inbound FIFO

Each read from register 0 retrieves one word from an eight-word-long inbound FIFO queue. The FIFO is used by the HP-IB Chip to hold data bytes and secondary addresses that have arrived from the HP-IB and are waiting to be read by the host processor. If the inbound FIFO is empty during any attempt to read from it, one of the following will occur:

1. If the device containing the HP-IB Chip is the HP-IB controller and has been conducting a parallel poll for at least two microseconds (bit 10 in register 3 is set and the outbound FIFO has been empty for at least two microseconds), the read from register 2 will receive the DIO line responses of the eight polling devices, masked and normalized by registers 4 and 5. This word will have the following format:

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	0	0	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

   It is recommended that the host processor attempt to obtain these responses only when servicing the provided PARALLEL POLL RESPONSE interrupt.

2. In all other cases, the read from register 0 will obtain a word of indeterminate value and the HANDSHAKE ABORT bit (bit 9) in register 2 will be set.

   An aborted attempt to read from the inbound FIFO can be repeated, if desired, until a valid word is finally obtained.

Data bytes enter the inbound FIFO from the HP-IB only if the device containing the HP-IB Chip is addressed to listen. Secondary addresses enter the inbound FIFO only if the preceding Interface Command sent over the HP-IB was the device's primary talk or listen address.

If the HP-IB Chip is in the process of receiving a Data Byte or a secondary address from the HP-IB, but either the Inbound FIFO is full or the DEVICE CLEAR bit in register 2 is set, the HP-IB handshake will be held off until the host processor reads a word from the FIFO or clears the DEVICE CLEAR bit. An interrupt is provided by the HP-IB Chip to notify the host processor when the inbound FIFO contains one or more words to read.

The inbound FIFO is initialized to an empty state only when the PON input pin has a low value.

When a word enters the inbound FIFO, its two high order bits (D0,D1) are set to show whether it is a standard data byte, the last data byte of a subgroup, the last byte of a record, or a secondary address.

Data Byte:

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	0	0	DATA BYTE VALUE							

This format is used for any received data byte that is not the last byte of a subgroup or record.

Last Byte Of Subgroup:

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	1	0	DATA BYTE VALUE							

This format is used only within HP-IB controllers for a data byte that caused the byte count of a Byte Transfer Enable to expire, but which is not the last byte of the record.

Last Byte Of Record:

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	1	1	DATA BYTE VALUE							

This format is used for a received data byte that is the last byte of a record and will occur in either of the following two cases:

- The END bit that accompanied the data byte on the HP-IB was set to "1".

- Within HP-IB controllers only, the data byte is an ASCII Line Feed character that was received in response to a BYTE TRANSFER ENABLE which requested Line Feed detection.

Secondary Address:

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	0	1	0	0	TLK	SECONDARY ADDRESS				

This format contains the five-bit address field (DIO5- DIO1) of a secondary talk address or secondary listen address received from the HP-IB.

After an HP-IB controller sends a primary talk or listen address instructing a device to participate in the next byte transfer, it can send a secondary address to further define the source or destination of the bytes within the device. When an HP-IB Chip receives a secondary address from the controller, the address is placed in the inbound FIFO for evaluation by the host processor. However, if the CRC function is enabled and the secondary address received was 21 (octal), it will not be placed in the inbound FIFO. Refer to the description of CRC functions in the paragraph "Register 7, HP-IB Address" for more details.

The TLK bit is set to a "1" if the preceding Primary Interface Command was the Talk address of the device containing the HP-IB Chip. The TLK bit is set to a "0" if the preceding Primary Interface Command was the device's listen address.

Register 1, Status

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	---	---	HIGH ORDER ACCESS		REM	HPIB CTRL	SYST CTRL	TLK/ IDF	LTN	DATA FRZ

Register 1 can be read at any time by the host processor to obtain the values of eight status conditions within the HP-IB Chip. A write into this register can affect only bits 8, 9, and 15.

Bit Definitions:

Bits 0,1 – UNASSIGNED

Always will have a "0" value when read.

Bits 8, 9 – HIGH-ORDER BIT ACCESS

These bits act as a substitute for pins D0 and D1 in applications where only an eight-bit data path is available for communication between the HP-IB Chip and its host processor. Whenever any HP-IB Chip register other than register 1 is read by the host processor, these two bits are set to the values being sent out of the HP-IB Chip on pins D0 and D1 for later access by the processor. Reading from register 1 does not cause any change in the value of these bits.

If the "8 BIT PROCESSOR" bit in register 6 is set while any HP-IB Chip register other than register 1 is being written into by the host processor, these two bits are used instead of pins D0 and D1 as the source of high-order bit data for the register.

These bits can be altered directly with a write to register 1 and if bit 14 is written as a "0", this write operation will not have any other effect on the state of the HP-IB Chip. These bits are useful in some 10-bit data path applications since they provide a "second chance" to access the high-order bits of the inbound FIFO after a read from register 0.

Bit 10 – REMOTE

This bit has a "1" value if the device containing the HP-IB Chip is in the remote state as defined in the HP-IB Interface Standard. It is mainly used within devices that can be programmed either from their front panel or through the HP-IB.

Bit 11 – HP-IB CONTROLLER

This bit has a "1" value whenever the device containing the HP-IB Chip is the current HP-IB controller. It is set when one of the following conditions are met:

- A "Take Control" Interface Command is received from the current HP-IB controller.
- The IFC line of the HP-IB is asserted (within System Controllers only).

This bit is cleared when one of the following conditions are met:

- The PON input pin is brought low.
- The HP-IB Chip goes from offline to online.
- A "Take Control" Interface Command is sent to another device on the HP-IB.
- The IFC line of the HP-IB is asserted (within non-System Controllers only).

Bit 12 – HP-IB SYSTEM CONTROLLER

This bit has a "1" value when the device containing the HP-IB Chip is the System Controller of the HP-IB (its SCTRL pin is high) or when the HP-IB chip is offline.

The HP-IB System Controller is the only device in a system that can assert the IFC or REN lines of the HP-IB.

When a device is offline, the IFC and REN lines are asserted only within the HP-IB Chip and not on the actual HP-IB. This feature is useful in offline diagnostics since it allows any device to set IFC while it is offline to locally become its own HP-IB controller. It can then send itself Interface Commands and test its response to them offline without interfering with the operation of the real HP-IB.

Bit 13 – ADDRESSED TO TALK OR IDENTIFY

This bit has a "1" value whenever the device containing the HP-IB Chip is addressed to talk or to send Identification Bytes over the HP-IB, whether or not a serial poll is being conducted.

Bit 14 – ADDRESSED TO LISTEN

This bit has a "1" value whenever the device containing the HP-IB Chip is addressed to listen to bytes sent over the HP-IB.

Bit 15 – OUTBOUND DATA FREEZE

This bit is set within a non-controlling device whenever a byte enters its Inbound FIFO from the HP-IB (not from its own outbound FIFO). While it is set, it prevents data from leaving the outbound FIFO over the HP-IB to give the host processor a chance to read the byte that arrived and possibly change its mind about sending any data that is already in the outbound FIFO. The host processor can reset this bit by writing a "1" into its bit position, but only if the inbound FIFO is empty (no other byte has arrived from the HP-IB)

Register 2, Interrupting Conditions

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	INT PEND	PRTY ERR	STAT CHNG	PROC ABRT	PP RESP	SERV RQST	FIFO R O O M	FIFO BYTE	FIFO IDLE	DEV CLR

Register 2 used by the host processor to identify the cause of an interrupt generated by the HP-IB Chip. Each bit in this register is associated with a particular interrupting condition as defined below. The bits can be unconditionally forced to a "0" value (masked off) over and above its definition by assigning a "0" value to the corresponding bit in Register 3 (INTERRUPT MASK). Whenever a bit is masked "off", it loses the ability to cause an interrupt of the host processor.

Bits D10 through D14 represent the states of the HP-IB Chip. Unless they are masked off by register 3, they are read as "1" values and continuously cause an interrupt condition as long as their associated states exist. Writes to register 2 have no effect on their values.

Bits D1, 8, 9, and 15 are set when particular events occur and are reset only when the host processor writes a "1" into their bit positions in register 2. Writing "0"s into the bit positions in register 2 has no effect on their values. These bits are initialized to "0" whenever the PON line is low.

Bit Definitions:

Bit 0 – INTERRUPT PENDING

This bit is the logical "OR" of the nine enabled low order bits which are enabled by corresponding bits of register 3. When the value of this bit is a "1" after being enabled by bit 0 of register 3, the HP-IB Chip provides a continuous interrupt to the host processor by grounding the INT line. Writing into register 2 affects the value of this bit only when the value of the event recognition bits included in the "OR" function are changed.

Bit 1 – PARITY ERROR

This bit is set whenever an Interface Command is received without odd parity. It is cleared when the host processor writes a "1" into its bit position.

Bit 8 – STATUS CHANGE

This bit is set whenever there is a change in the value of the REMOTE bit in register 1 while the HP-IB Chip is a non-controller, or whenever there is a change in the value of the HP-IB CONTROLLER bit in register 1. It is cleared when the host processor writes a "1" into its bit position.

Bit 9 – PROCESSOR HANDSHAKE ABORT

This bit is set whenever there is a read from the inbound FIFO while it is empty. It is not set within HP-IB controllers that have been conducting a parallel poll for at least 2 microseconds. If the host processor wants to repeat the read or write until it is normally completed, the HP-IB Chip guarantees that data will not be lost. This bit is cleared when the host processor writes a "1" into its bit position.

Bit 10 – PARALLEL POLL RESPONSE

A "1" indicates that a parallel poll is being conducted and one or more devices need service. This interrupt occurs as long as all of the following conditions are true:

- Bit 10 in register 3 is "1" and the outbound FIFO is empty. Therefore a parallel poll is performed.
- The parallel poll has been performed for at least 2 microseconds to provide time for the bus DIO lines to settle.
- The inbound FIFO is empty so that the host processor will not obtain data when it reads from register 0 in response to this interrupt.
- One of the devices on the HP-IB is indicating a need for service by asserting a DIO line which has been masked "ON" by register 4. The level of assertion depends on the corresponding bit in register 5.

Bit 11 – SERVICE REQUEST (for HP-IB controllers Only)

A "1" indicates that one or more devices are requesting service via the bus SRQ line.

Bit 12 – FIFO ROOM AVAILABLE

A "1" indicates that the outbound FIFO is not full and can accept writes without aborting.

Bit 13 – FIFO BYTES AVAILABLE

A "1" indicates that the inbound FIFO contains one or more bytes that can be ready by the host processor.

Bit 14 – FIFO IDLE

A "1" indicates that the outbound FIFO is empty. Within HP-IB controllers, this will cause parallel polling to be conducted if bit 10 in register 3 is set. Otherwise, the HP-IB controller will go to the Controller Standby Hold State.

Bit 15 – DEVICE CLEAR

This bit is set whenever a "Device Clear" Interface Command is received through the HP-IB while the HP-IB Chip is a non-controller. While it is set, it blocks all transfers between the FIFOs and the HP-IB controller will go to the Controller Standby Hold State without losing data. The host processor can then clear this bit by writing a "1" into its bit position.

Register 3, Interrupt Mask

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	INT ENAB	INTERRUPT MASK								

A "0" in any bit position of register 3 causes the corresponding bit in register 2 to read as 0 and prevents that bit from causing an interrupt to the host processor. A "0" in bit 10 also prevents the HP-IB controller from conducting a parallel poll. Since the INTERRUPT ENABLE (INT ENAB) bit can hold off all interrupts by directly masking bit 0 in register 2, the host processor can view all interrupting conditions without getting an interrupt by setting it to "0" and setting all other mask bits to "1". For the HP-IB controller, a "1" must be written into bit 10 to enable the parallel poll feature. It is possible to toggle the parallel poll on and off by writing a "1" or "0" to this bit.

Register 3 can be read or written to by the host processor at any time and is initialized to all zeros whenever the PON line is low.

Register 4, Parallel Poll Mask/First ID byte

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
MASK BITS/FIRST ID BYTE										

Register 4 can be read or written to at any time within an HP-IB controller to provide a mask for incoming parallel poll responses. Within a non-controlling device, it is used by the host processor to specify the first byte of a two-byte product type Identification Code as defined below. All bits are initialized to "0" whenever the PON input has a low value.

Within an HP-IB Controller:

Each bit in this register that has a "0" masks "OFF" (forces to zero) the Parallel Poll Response arriving via its corresponding DIO line whenever a parallel poll is being conducted (see register 5 for further information about responses from the DIO lines). Only those responses that are not masked "OFF" are included in the determination of the Parallel Poll Response interrupt.

Within a Non-Controlling Device:

This register and register 5 can optionally participate in an identification sequence through which the HP-IB controller can find out what type of device exists at each HP-IB address. To use this feature, have the host processor perform the following setup:

1. Before going online, load registers 4 and 5 with a 16-bit device type Identification Code assigned to the product and set the "Respond to Parallel Poll" bit in register 6.

2. Place the HP-IB Chip online while the "Respond to Parallel Poll" bit is still set, showing a need for service during a parallel poll conducted by the HP-IB controller.

3. After the HP-IB controller has acknowledged that it has seen the Parallel Poll Response, the "Respond to Parallel Poll" bit can be cleared.

After the above set-up is performed, circuitry within the HP-IB Chip is enabled to allow it to respond to a special primary/secondary address pair separate from its normal HP-IB address, without any interaction with the host processor. Whenever the HP-IB Chip receives talk address 31 followed by a secondary address containing a 5-bit HP-IB ADDRESS specified in register 7, it will send the contents of register 4 and then the

contents of register 5 as data bytes, marking the contents of register 5 with an accompanying END bit as it is sent. The secondary addressing obeys all the rules of an "Extended Talker" defined in the IEEE Standard 488-1978.

To turn off this feature, set the "Respond to Parallel Poll" bit to "0" at the time the HP-IB Chip goes online. This causes all of the special address pair recognition circuitry to be disabled.

Register 5, Parallel Poll/Second ID Byte

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
SENSE BITS/SECOND ID BYTE										

Register 5 can be read or written to at any time within an HP-IB controller to specify the assertion levels of the incoming parallel poll responses. Within a non-controlling device, the host processor uses it to specify the second byte of a two-byte product type Identification Code as defined below. All bits are initialized to "0" whenever the PON input has a low value.

Within an HP-IB Controller:

Each bit in this register is "Exclusive-OR'ed" with the Parallel Poll Response arriving via its corresponding DIO line whenever a parallel poll is being conducted. Set a bit to "1" only if it is known that the device responding via its corresponding DIO line is using a "0" to indicate its need for service. Multiple devices can be programmed to use a "0" on the same DIO line to indicate readiness for some operation and the controller will see the interrupt only after they are all ready.

Within a Non-Controlling Device:

This register and register 4 can optionally participate in an identification sequence through which the HP-IB controller finds out what type of device exists at each HP-IB address. Complete details of this sequence are contained in the description of register 4.

Register 6, Control

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	POLL HLDF	DHSK DLY	8 BIT PROC	PRTY FRZ	R E N	I F C	RSPD PP	RQST SRVC	FIFO SEL	INIT FIFO

Register 6 can be read or written to at any time by the host processor to access control bits within the HP-IB Chip. All bits are initialized to "0" whenever the PON pin is low.

Bit Definitions:

Bit 0 – POLL HOLDOFF

A "1" will prevent the HP-IB Chip from responding affirmatively to a parallel poll if OUTBOUND DATA FREEZE is active. If the RESPOND TO PARALLEL POLL bit is set and OUTBOUND DATA FREEZE is active, the HP-IB Chip will not respond affirmatively to a parallel poll. A "0" will remove the OUTBOUND DATA FREEZE restriction on a parallel poll response.

Bit 1 – DATA HANDSHAKE DELAY

A "1" will require that NDAC and NRFD remain continuously false for a period of time before they can be sensed false by the Source Handshake interface function on data transfers. This will prevent improper handshakes resulting from the transmission line properties of the interface bus when multiple acceptors are active. A "0" in this position does not delay the value of NDAC or NRFD to the Source Handshake circuitry. The delay of NRFD and NDAC is enabled for command handshakes regardless of the state of the DATA HANDSHAKE DELAY bit.

Bit 8 – 8-BIT PROCESSOR

A "1" indicates to the HP-IB Chip that the host processor wishes to use an 8-bit data path instead of the standard 10-bit path. During a write to any register except register 1, the HP-IB Chip uses the current values of bits 8 and 9 of register 1 instead of data which would normally arrive via the D0 or D1 lines. D0 and D1 lines can be left untied if only 8-bit communication is desired (bit 8 will always be set). However, during reads from the HP-IB Chip, D0 and D1 always contain valid high-order bit values, even if bit 8 is set, and may prove useful in some applications.

Bit 9 – PARITY FREEZE

Whenever this bit has a "1" value, the HP-IB Chip will refuse to accept or interpret any Interface Command (including device addresses) that does not have odd parity. This will force the HP-IB to remain frozen with DAV asserted and the erroneous Interface Command held on the bus DIO lines until the HP-IB controller aborts the transfer by removing DAV. This bit does not affect in any way the "PARITY ERROR" interrupt bit in register 2.

Bit 10 – REN VALUE (System Controllers only)

If the device containing the HP-IB Chip is the System Controller of the HP-IB, this bit determines the value of the bus REN line.

Whenever this line is asserted, it must remain asserted for at least 100 microseconds to meet the IEEE Std 488-1978 specifications.

A System Controller can assert the REN line at any time to allow programmable devices tied to the HP-IB to be remotely programmed instead of using their front panel controls.

When the HP-IB Chip is offline, this bit can be used locally in diagnostics whether or not the device is the System Controller.

Bit 11 – IFC VALUE (System Controllers only)

If the device containing the HP-IB Chip is the System Controller of the HP-IB, this bit determines the value of the bus IFC line.

Whenever this line is asserted, it must remain asserted for at least 100 microseconds to meet the IEEE Std 488-1978 specifications.

A System Controller can assert the IFC line at any time to initialize the HP-IB interfaces within all devices connected to the HP-IB. Note that the devices themselves are not initialized, only their HP-IB interfaces. Assertion of this line also has the effect of forcing the System Controller to be the HP-IB controller no matter which device previously had this capability (see register 1, HP-IB Controller bit). As a result, the System Controller need not follow the normal "Take Control" Interface Command protocol when it wishes to regain control of the HP-IB after it has passed it away or when it has just gone online.

When the HP-IB chip is offline, this bit can be used locally in diagnostics whether or not the device is the System Controller.

Bit 12 – RESPOND TO PARALLEL POLL

Whenever this bit has a "1" value, the HP-IB Chip will indicate a need for service during any Parallel Poll if it has Parallel Poll response capability (refer to the description of HP-IB ADDRESS in register 7).

Bit 13 – REQUEST SERVICE

Whenever this bit as a "1" value, the HP-IB Chip will use the HP-IB SRQ line and serial poll facility to request service from the HP-IB Controller in accordance with the rules of the HP-IB Interface Standard.

It begins asserting the SRQ line as soon as this bit is set.

When it is first polled by the HP-IB controller during a serial poll, it stops asserting the SRQ line and responds to this poll and all subsequent ones with a hex 40 (DIO 7 = "1").

The host processor should keep this bit set until service is obtained from the HP-IB controller.

After the host processor clears this bit, the HP-IB Chip will respond to all serial polls with a hex 80 (DIO 7 = "0" and odd parity).

Bit 14 – DMA FIFO SELECT

Whenever this bit has a "1" value, the DMARQ pin of the HP-IB Chip will be asserted (low) whenever the outbound FIFO is ready for a write operation. If this bit has a "0" value, the DMARQ pin will be asserted whenever the inbound FIFO is ready for a read operation.

Bit 15 – INITIALIZE OUTBOUND FIFO

Any time a "1" value is written into this bit position, the outbound FIFO will be forced empty but not necessarily unfrozen (see register 1, bit 15). If the empty FIFO is in an HP-IB controller a continuous parallel poll will be executed (see "Register 0, Outbound FIFO" in this chapter). No actual storage location corresponds to this bit position and it always has a "0" value when read.

Register 7, HP-IB Address

Computer Bit No.	9	8	7	6	5	4	3	2	1	0
HP-IB Chip Bit No.	D0	D1	D8	D9	D10	D11	D12	D13	D14	D15
	CRCE	EPAR	ONL	TA	LA	HP-IB ADDRESS				

Register 7 can be read or written to at any time by the host processor to specify an HP-IB address and related control information to the HP-IB Chip. All bits in this register are initialized to zero whenever the PON line is low. The lower 8 bits correspond to switches U144 S1-8. See "HP-IB Address Selection" in chapter 2.

Bit Definitions:

Bit 0 – CRC ENABLE

A "1" value in this bit position enables the CRC capabilities in the HP-IB Chip. These capabilities are:

- If the secondary talk or listen address, 21 (octal), is received over the HP-IB, it is not allowed to enter the inbound FIFO.
- Whenever the HP-IB Chip receives its talk address followed by the secondary address, 21 (octal), it will send as data bytes the contents of the CRC generator in a two-byte sequence. The first byte will be the most significant byte of the CRC remainder. The second byte will be the least significant byte of the CRC remainder tagged with EOI.
- Whenever the HP-IB Chip receives its listen address followed by the secondary address, 21 (octal), it will reset the contents of the CRC generator to 0 (octal).
- Any data handshaked by the HP-IB Chip will be operated on by the CRC generator. The only exception to this is when the HP-IB Chip is sending its own CRC remainder. The CRC generator uses the CRC-16 polynomial $X16 + X15 + X2 + 1$. The CRC generator operates on a data byte as if DIO8 was received first.

A "0" disables all CRC capabilities in the HP-IB chip.

Bit 1 – EVEN PARITY

A "1" will force even parity on HP-IB commands originating from the outbound FIFO. A "0" will force odd parity on HP-IB commands originating from the outbound FIFO.

Bit 8 – ONLINE

Whenever this bit has a "1" value, the HP-IB Chip is online and will interact normally with the HP-IB. If it is a "0" value, the HP-IB Chip is offline and will not interact in any way with the HP-IB. When this bit is set, the HP-IB Chip waits for a period equal to the width of IOGO before going online. During this period, the HP-IB Chip initializes its interface circuitry to the HP-IB so that it does not start out as a talker, listener, or controller. This performs the function of the "pon" message defined in the IEEE Standard. If other bits in register 7 were set simultaneously with the ONLINE bit, they are also given a chance to settle during this time.

Bit 9 – TALK ALWAYS

This bit is for communication between devices in systems without a controller and should not be set when a controller is present except in diagnostics. When the bit is set, the HP-IB Chip assumes that it is continually addressed to talk unless the bus IFC line is being asserted. When it is cleared by the host processor, the HP-IB Chip continues to be addressed to talk until the IFC line is asserted, the talk address of another device is received, or the PON line is brought low.

Bit 10 – LISTEN ALWAYS

This bit is for communication between devices in systems without a controller and should not be set when a controller is present except in diagnostics. When the bit is set, the HP-IB Chip assumes that it is continually addressed to listen unless the bus IFC line is being asserted. When it is cleared by the host processor, the HP-IB Chip continues to be addressed to listen until the IFC line is asserted, the Unlisten command is received, or the PON line is brought low.

Bits 11 to 15 – HP-IB ADDRESS

Within a non-controlling device, the values of these five bits determine the HP-IB address to which the HP-IB Chip will respond. Any address between 0 and 29 can be used but avoid addresses 30 and 31. If the address specified is between 0 and 7, the HP-IB Chip will assume that it can respond to parallel polls initiated by the HP-IB controller and will use a DIO line corresponding to its address. DIO 8 through DIO 1 correspond to addresses 0 through 7, respectively. The other addresses are not assigned initial parallel poll response capability but it may be assigned by the HP-IB controller.

Within an HP-IB controller, the HP-IB Chip always responds to Address 30 for talking and listening, not to the address specified by these bits. This feature allows constraints to be used for self-addressing within the controller software.

Offline Diagnostics

As long as bit 8 of register 7 has a "0" value, the HP-IB Chip remains offline. This is also the initialized state of the HP-IB Chip. While the HP-IB chip is offline, it is isolated from the HP-IB (see figure 3-5). In this condition, the host processor can diagnose HP-IB Chip circuitry without interfering with the normal HP-IB operation.

While offline, the complete set of interface functions are tied together internally and interact normally using an internal copy of the HP-IB. Note that the circuitry used to do this is not special offline circuitry but is the same circuitry used when the HP-IB Chip is online. Timing and sequencing satisfy all HP-IB specifications and regulation. All HP-IB programming protocols are required (i.e., talk, listen, etc.).

Most diagnostics performed offline require that the HP-IB Chip be the controller of its internal HP-IB so that it can send itself Interface Commands. Since only an HP-IB System Controller can use the IFC line to take control of the HP-IB, an offline HP-IB Chip will assume System Controller status in spite of the value of its "SCTRL" pin.

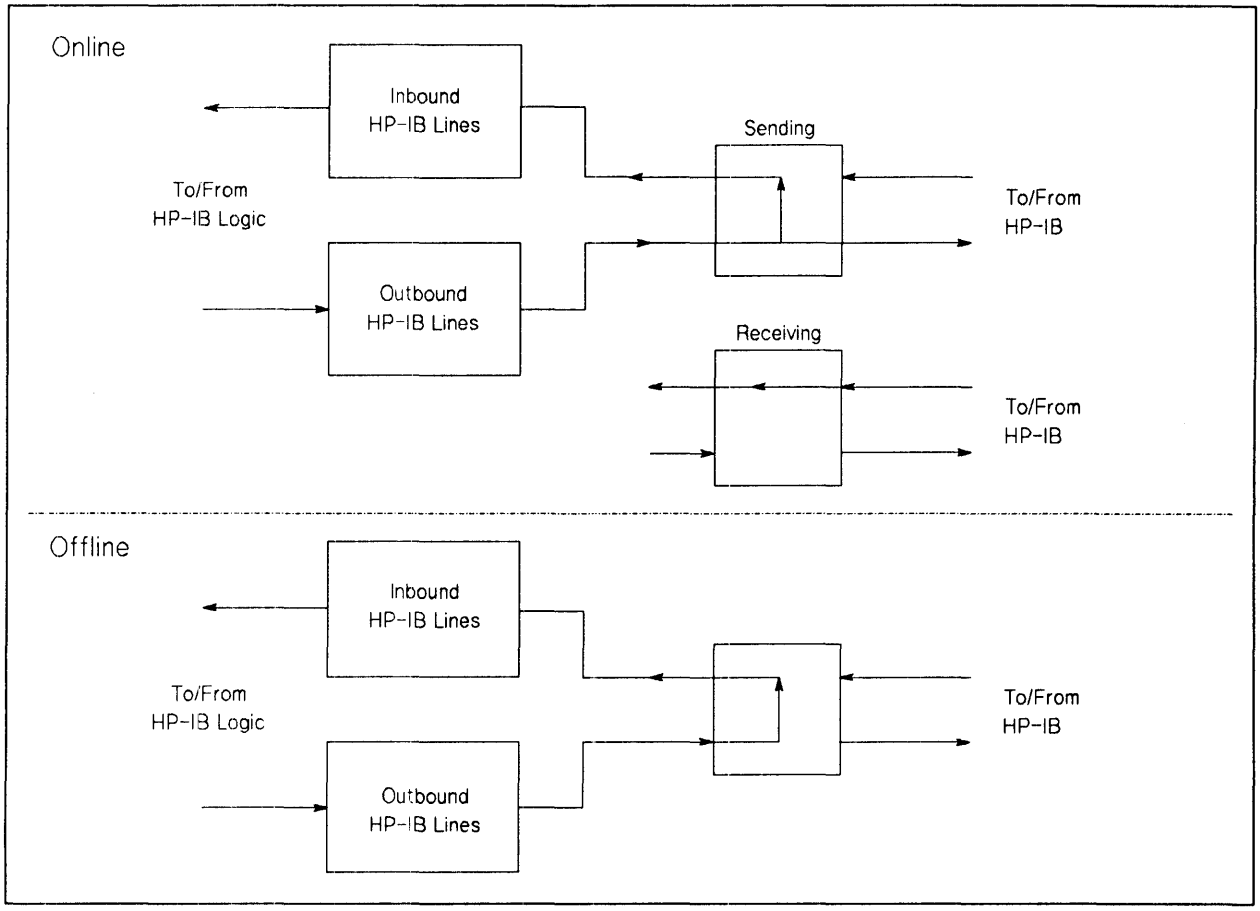


Figure 3-5. HP-IB Transceiver's Online and Offline States

4 Theory of Operation

This chapter provides information about the theory of operation of the HP-IB Interface at the block level and at the functional level. The theory will cover individual components when they serve a unique purpose.

For more information, see the IEEE Std 488-1978 and the *HP 1000 I/O Interfacing Guide*, part number 02103-90005. The Interfacing Guide provides a detailed theory of operation for the I/O Master.

General Description

The HP 12009A HP-IB Interface provides a complete hardware interface between an A-Series computer and an HP-IB system of up to 14 devices. Several such HP-IB systems can be interfaced to an A-Series computer. Each system requires a separate interface card.

Figure 4-1 shows the card in a typical A-Series system. As shown in the figure, the card must be installed in the first slot below the processor card (highest priority I/O slot) when it is configured for high speed operation. If it is not configured for high speed operation, it can be installed in any I/O slot below the processor card. The HP-IB card is connected to the HP-IB system through the cable supplied with the kit.

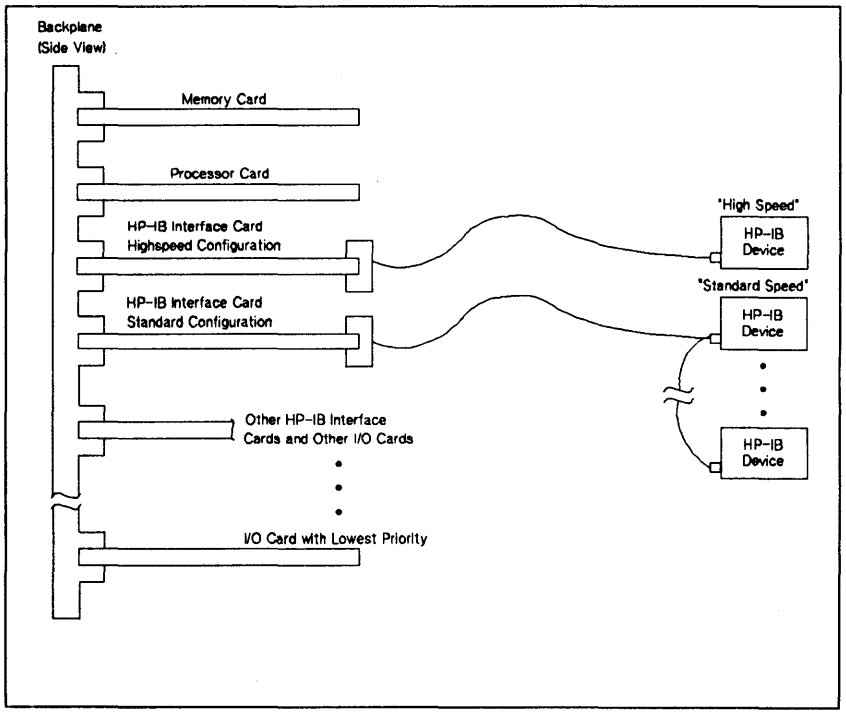


Figure 4-1. Typical A-Series System

To the A-Series computer, this card is an I/O card and is under its software control at all times. To the HP-IB system, this card may or may not be a System Controller, depending on the setting of the System Controller Select switch, U1S1.

The operation of the card is under control of the A-Series processor. Control words may be passed to the card and data exchanged through the system data bus by I/O instructions. Alternately, the processor may program the card's DMA machine which then reads from system memory the interface card's control words and HP-IB control messages, and exchanges data between the HP-IB and memory. Figure 4-2 shows a simplified block diagram of the HP-IB interface card.

The card contains an I/O Master section and an HP-IB Bus Interface section. The I/O Master section handles Direct Memory Access (DMA) and the decoding of its own instructions. The I/O Master section is composed of the I/O Processor chip (U61) and its associated logic circuitry. It performs all the functions necessary for interfacing with the A-Series backplane. The HP-IB Bus Interface section is composed of the HP-IB chip (U117) and its associated logic circuitry. This interface provides the card with its HP-IB capability consisting of the following functions:

- System Controller capability.
- The ability to respond as a bus controlled device with proper A-Series programming.
- Eight level buffering of command and data bytes between the HP-IB and the card for both input and output.
- Automatic handling of HP-IB handshakes.
- Parallel Poll response mask and Service Request interrupt mask.
- Facilities for DMA operation with the processor.
- Simple electrical interface to the HP-IB through three transceiver chips, and LS TTL interfacing to the I/O Master section.
- Fast response to support peak HP-IB throughput of 930 Kbytes per second.
- Automatic response to bus-issued universal and addressed commands.

A six-bit select code for the card is set by a DIP switch (U1S3-S8) located on the card. This select code is used only as a means of addressing the card (I/O Master) and bears no relation to the DMA priority of the card. The DMA priority is determined by physical location relative to the processor card in the card cage.

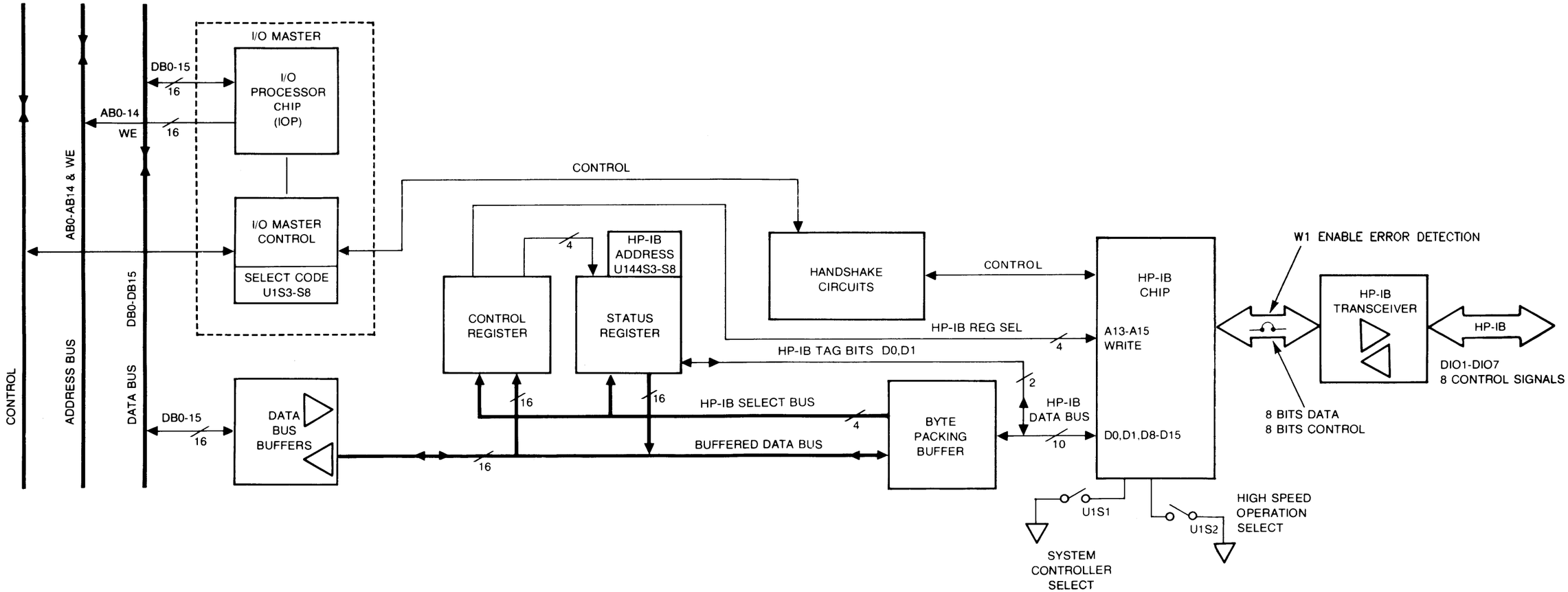


Figure 4-2. HP 12009A Interface Simplified Block Diagram

Block View

The simplified block diagram shown in figure 4-2 illustrates the basic operation of the HP-IB card in the A-Series system.

The main flow of data can be from the HP-IB system to the backplane through the HP-IB bus interface and the I/O Master, or it can be from the backplane to the HP-IB system through the I/O Master and the HP-IB Bus Interface.

In some cases, the data transfers may not include the I/O Master. When the card is running a diagnostic, the HP-IB Chip can close off the external HP-IB lines and the signals will go only as far as the HP-IB Chip (refer to figure 3-5).

When data moves from the computer to the HP-IB system, the data bus buffers take data from the backplane's data bus and drive it onto the buffered data bus. The byte packing buffer takes the data off the buffered data bus and converts the 16-bit data words into two 8-bit bytes (a bit 0 through 7 upper byte and a bit 0 through 7 lower byte). Two more bits (bits 8 and 9) are produced by the Control Register and are driven onto the HP-IB data bus (HP-IB tag bits). The Control Register also provides four other bits (derived from the buffered data bus), bits 12 through 15, to the HP-IB Chip as the HP-IB Chip register select bits A13, A14, and A15 and the HP-IB Chip's WRITE signal. The HP-IB Chip produces the HP-IB's eight bits of data (DIO1-DIO8) and eight bits of control, which the HP-IB Transceivers drive onto the HP-IB lines.

When data moves from the HP-IB system to the computer's backplane, the HP-IB system applies its signals to the HP-IB transceivers. The HP-IB transceivers drive the data into the HP-IB Chip. The HP-IB Chip drives 10-bits (D0, D1, and D8-D15) onto the HP-IB data bus. The byte packing buffers take two 8-bit bytes (upper and lower) and produce 16-bit words for the computer. These words are driven onto the buffered data bus. The two HP-IB tag bits, D0 and D1, are applied to the buffered data bus as bits 8 and 9 via the Control Register. The HP-IB select bus provides four bits (bits 0, 1, 2, and 3) to the Control Register (upper byte). These four bits are driven onto the buffered data bus as bits 12-15. The data bus buffers take the 16-bit words and drive them onto the backplane data bus as bits DB0 through DB15.

The HP-IB Chip has two switch selectable options: High Speed Operation Select, and System Controller Select. If the System Controller Select option is selected, the HP-IB Interface Card will act as the System Controller. If the High Speed Operation Select option is selected, the HP-IB Interface Card will operate at about 930 Kbytes per second.

The handshake circuitry allows the HP-IB Chip and the I/O Master to work together. It allows the data and control exchanges to take place between these two major blocks.

Functional View

Figure 7-4 shows the schematic logic diagram and figure 7-2 shows the overall functional block diagram. See the IEEE STD 488-1978 and the HP 1000 I/O Interfacing Guide, part number 02103-90005, for further information. Integrated circuit base diagrams and function tables are shown in figure 7-1 for the I/O Processor Chip and the HP-IB Bus Interface Chip.

To simplify locating components on the three schematics, the following scheme is used: There are ten numbers across the top and bottom border of the schematic's three sheets, going from 10 to 18, 20 to 29, and 30 to 39, respectively. The first number indicates the sheet number, 1, 2, or 3, and the second number is the vertical column. A set of five alphabetic letters, A–E, are on the left and right borders of the schematics. This references 50 areas. To make the coordinates easy to find in the text, they are set off in brackets [ ]. For example, [25C] would be found on the second sheet, column 5, and horizontal row C. The Secondary Address Latch flip-flop U136 is found at this location.

The four main functions are as follows:

- Non-DMA Transfers
- DMA Transfers
- Control Word Transfers
- Status Word Transfers

Non-DMA Transfers

Output Transfers

Loading the Card Data Register: (OT* 30)

The low byte (lower eight bits, bits 0-7) is clocked into U114 [32A], a 74LS373, by BCS1– and CKDAT– through the NAND gate U78 [31A], a 74LS02. The lower four bits of the upper byte (bits 8–11) are clocked into U45 [24B], a 74LS175, by CLK+. This signal is produced at U48 pin 6 [21B], a 74LS132, by BCS1–, CKDAT–, and LOBYT–. The four upper bits of the upper byte (bits 12–15) are clocked into U76 [34A], a 74LS175, by CLK+.

Bit 15 via U76 pins 6 and 7 controls the direction of the HP-IB data bus. When bit 15 is low, U76 pin 6 is high and pin 7 is low. The low on pin 7 enables U44 [25B], a 74LS244, to put HP-IB tag bits D0 and D1 on the HP-IB data bus. The high on U76 pin 6 enables the lower eight bits (bits 0–7) from the buffered data bus to be put on the HP-IB data bus via U114 [32A], a 74LS373. The 10 bits (0–9) on the HP-IB data bus are labeled on the HP-IB Chip U117 [35B] as bits D0,D1, and D8 through D15. Table 4-1 summarizes the bit labeling.

Table 4-1. Bit Labeling Summary, Data Word and HP-IB Data Bus

Data Word Bit	HP-IB Data Bus Bit
0	D15
1	D14
2	D13
3	D12
4	D11
5	D10
6	D9
7	D8
8	D1
9	D0

Bits 14 through 12 via U114 select which of the eight HP-IB Chip registers the HP-IB data will be loaded into. Bit 14 is input A13 to the HP-IB Chip (higher order bit), bit 13 is input A14, and bit 12 is input A15. Table 4-1 shows the HP-IB Chip registers selected by the various codes.

Buffered data bus bits 10 and 11 do not apply to a data word transfer and must be "0" at all times.

Table 4-2. HP-IB Chip Register Selection Code and Names

HP-IB Chip Register Select Code			HP-IB Chip Register Number	Selected HP-IB Chip Register Name
A13	A14	A15		
0	1	0	0	FIFO
0	1	1	1	STATUS
0	0	0	2	INTERRUPT
0	0	1	3	INTERRUPT MASK
1	1	0	4	PARALLEL POLL MASK
1	1	1	5	PARALLEL POLL SENSE
1	0	0	6	HP-IB CONTROL
1	0	1	7	HP-IB ADDRESS

Processing the Data Word Instruction: STC 30, C

The STC 30, C instruction generates the signal DVCMD (Device Command) out of the I/O Processor Chip, U61 pin 37 [16B]. DVCMD– is ANDed with SCLK + via U38 pin 13 [21D], and U38 pin 1, a 74S02. This signal clocks the HP-IB Command flip-flop, U17 [21E], a 74S74, causing U17 pin 5 to go high. The high output (GO +) of the HP-IB Command flip-flop initiates an HP-IB Chip handshake by asserting the IOGO pin on the HP-IB Chip, U117 pin 19 [35C], via U67 [33C], a 74S10, if DMA is not enabled or other conditions exist which will be explained in the DMA Transfer chapter. The HP-IB Command flip-flop remains set until the HP-IB Chip completes the handshake by asserting IOEND, U117 pin 18. This signal is also referred to as FIND + and FIND–. FIND + is delayed through two 74S04 inverters, U46 [25D], to insure sufficient set-up and

hold times for the HP-IB Command flip-flop, U17 and is labeled DELFIND+. A test of the flag sense should not be performed because Flag 30 in the I/O Processor Chip will not be set by the data transfer.

Input Transfers

Processing the Input Data Word Instruction: OT*30 or OT*31 STC 30,C

The OT* instruction transfers a word into the Outbound Register, U124 and U75, [33A] or into the Control Word Register. This word is used to select the HP-IB Chip register that will be the source of the input transfer.

Bit 15 (WRITE) of the buffered data bus tells the HP-IB Chip that this will be an inbound transfer (bit 15 = 1) from the register selected by bits 14,13, and 12. This information need not be reestablished between successive transfers from the same register. STC 30, C provides a device command that initiates an HP-IB handshake as described in the paragraph "Processing the Data Word Instruction". FIGO– and DELFIND+ are gated through a 74LS27, U135 [33B], to latch the lower eight bits (8 through 15) of the HP-IB data bus into a 74LS373, U124 [33A], which requires no set-up time (figure 4-2). The HP-IB tag bits, D0 and D1, are latched into a 74S157, U34 [27B], by the HP-IB handshake (FIFO– and FIND+) gated through a 74S02, U25 [27D], which requires 4.5 nanoseconds set-up time. The timing for this latch is the same as for U135 and is shown in figure 4-3.

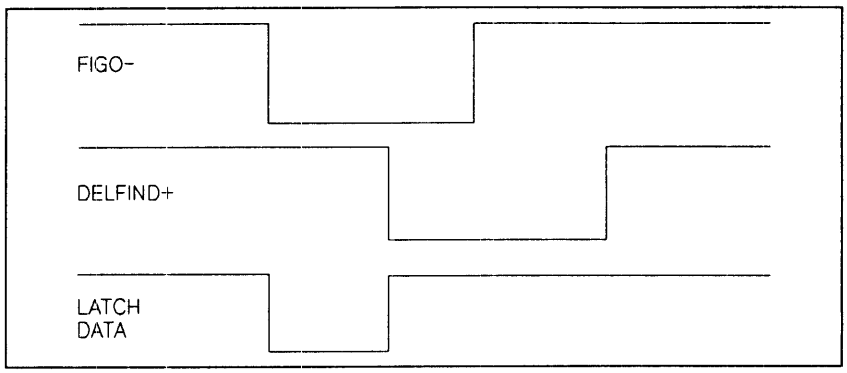


Figure 4-3. FIGO– and DELFIND+ Timing Diagram

The 74LS157, U34 [27B], latches the data by passing its output back into input A. When the select line, pin 1, is high, the data on input B is passed to the output and back into input A. When the select line changes, the input A is passed to the output and the data is latched.

Loading the Input Data Word Instructions: LIA 30.

The data word is loaded into the computer by an LIA 30 instruction. The I/O Master generates a Bus Select Code (BCS5–) that enables the 10 bits of the HP-IB data bus onto the buffered data bus via U44 [27B] and U124 [33A]. U44 drives the data word onto the buffered data bus when U35 pin 11 [25A] goes low. U44 also insures that input data word bits 10 and 11 will be "0". The upper four bits (bits 12–15) label the input data word with

the direction and register number from which the word was read. They are enabled on the buffered data bus by U66 [25B], a 74LS258. This multiplexer with its select input (pin 1) driven by BCS7– (LDSTAT), passes the HP-IB select bus (read/write and the register select bits) whenever either the Data or Control register is read. U28 pin 12 [21A] and U26 [25B] provide an output control to the multiplexer whenever BCS5,BCS6, or BCS7 are present without "BYTE". This is a DMA signal that will be discussed in the DMA Transfer section.

DMA Transfers

The HP-IB Interface Card requires that the Card Control Word (Register 31) be loaded to indicate the direction of the transfer. The rest of the control word affects the setting of the Device Flag and the termination of the DMA transfer. Each bit of the Card Control Word is discussed in detail in chapter 3 of this manual. The HP-IB Chip register that will be accessed by the byte mode transfer must also be loaded.

DMA Word Mode Transfers

DMA Output Transfer

The DMA data transfer is identical to the non-DMA transfer except that the handshake is provided by the DMA machine. The DEVICE COMMAND bit set in the DMA control word generates a FIGO handshake. The FIGO from a DMA transfer is held off by U67 [33C], a 74S10, until the HP-IB chip is ready for a word (DMARQ). If the FIFO is selected, then it is a DMA transfer. The signal (FIFO +) at U135 pin 12 to U67 pin 2 prevents overrunning the FIFO, since this would destroy data already in the FIFO.

DMA Input Transfer

DMA input transfer is processed in the same way as non-DMA input transfer except that the Device Command is provided by the DMA machine. The data paths are identical to those described for an input transfer and the handshake is the same as described for DMA input transfer.

DMA Byte Mode Transfers

DMA Byte Mode Output Transfer

The DMA Control Word (register 21) initiates the byte pack mode. The I/O Master sends one DVCMD– command for each byte and therefore one FIGO– is generated for each byte transfer. The I/O Master generates the byte packing signal, low byte (LOBYT–) [18B] that is passed through U145 [31B], a 74LS375, to generate both senses of LOBYT which when gated with the WRITE- bit (bit 15 of the buffered data bus) of the control word enables the data byte, upper or lower, of the buffered data bus onto the HP-IB data bus. The "Q" output of U145 [31B] is gated with WRITE- via U125 pin 3 [31B], a 74LS00, to enable U64 [31B], a 74LS373, to drive the upper eight bits (bits 8–15) onto the HP-IB data bus. The "Q" output from U145 [31B] gated through U125 pin 11 enables U114 [32B], a 74LS373, to drive the lower eight bits (bits 0–7) onto the HP-IB data bus.

HP-IB data bus bits 0 and 1 are driven onto the bus by U44 [26B, 27B], a 74LS244. D1 is provided whenever bit 8 (ATN) of the control word is set. D0 is provided if, on the last byte transferred (DMAEN not asserted), bit 9 (EOI) is set in the control word. This gating is accomplished by two gates of U77 [24B, 25B], a 74LS02. The NAND gate (U77) at [24B] determines if the transfer is a word mode transfer or if DMA enable (BDMA-) has gone away and, if so, it drives U77 pin 8 [25B] low. U77 pin 10 then drives U44 pin 8 high, if the EOI is set.

DMA Byte Mode Input Transfer

The I/O Master provides the DVCMD– signal that initiates the HP-IB handshake, thus providing the storage signal to the data latches. The first byte (bits 8–15) that is transferred out of the HP-IB Chip is stored into both U124 and U75 [33A, 34A], 74LS373s, by U135 [33B], a 74LS27. When the I/O Master changes the LOBYT– signal, U145 disables the section of U135 that latches the upper byte of data into U75. The next FIGO– stores the next byte of data into the lower byte latch U124. U75 and U124 will be read by DMA when it is ready. HP-IB data bits D0 and D1 are latched into U34. Since, in the byte mode, these bits cannot be read, the hardware must check these bits for special functions and meanings. The Tag Bit Decoder, U24 [26C], a 74S138, detects two special messages from the HP-IB chip FIFO, End Of Record (EOR–) and My Secondary Address (MSA–). Bit 9 of the control word enables EOR through two of U25's gates [23C, 24C], a 74S02, to assert the signal Last Byte (LSBYT–), which terminates the DMA transfer. Bit 8 of the control word enables MSA through two of U25's gates [23C, 24C], a 74S02, to assert LSBYT– and terminate the DMA transfer. The Secondary Address Latch, U136 [25C], a 74LS74, is set when a secondary address is received to flag the data transfer if the termination bit is not enabled. Both EOR– and MSA– are checked as status bits 13 and 12.

DMA I/O Master Handshake

For basic I/O Master data transfer handshake the device asserts the Service Request (SRQ–) and the I/O Master responds with the Service Acknowledge (SACK–).

Starting DMA

If the DMA transfer is an output transfer, the first SRQ– is issued when U37 [23D], a 74LS27 connected as a cross-coupled latch, sets U37 pin 12 to a ":". This puts a "1" on U36 pin 3 [22D], a 74S153, and provides a clock to U17 [21C], a 74S74, that pulls SRQ– low. U37 pin 5 reads bit 3 of the control word via U14 [22B], a 74LS04. If bit 3 of the control word is set, DMA operation is delayed until an interrupt occurs causing U15 pin 8 [23C], a 74LS20, to go to a "1". The interrupt conditions are: an SRQ from the bus, receiving a secondary address, an HP-IB interrupt, or receiving a "Group Execute Trigger". If control word bit 3 is not set, then the SRQ is generated as soon as DMAEN– [19B] is asserted. If the transfer is an input, the first SRQ is generated by FIND + applied to the C0 and C1 inputs (pins 5 and 6) of U36.

During DMA

During the DMA data transfer, the output SRQs are provided by FIGO + applied to the C2 input (pin 4) of U36. The input SRQs are provided by FIND + applied to the C0 and C1 inputs (pins 5 and 6) of U36.

Terminating DMA

The last SRQ for an output transfer is called the N + 1 SRQ This SRQ is transmitted by the device and indicates that the processing of the last word is complete. It is generated when U27 [23D] 74LS74, is set by FIND– after DMAEN + is no longer the "Q" output of U27 [21D] to ensure that a DMA transfer was just completed, and PPDONE via U26 [24E] and U14 [23E] to ensure that adequate time was allowed to complete a parallel poll, if the DO PARALLEL POLL BIT (bit 1) was set. This signal (ENDEN) is then gated through U67 [21C], a 74S10, to ensure that it was indeed an output operation and that the control word has not requested a freeze on interrupt conditions. U67 pin 8 [21C], a 74S10, presets the flip-flop U17 [21C], a 74S74, causing the N + 1 SRQ signal. The last SRQ for an input transfer is generated by FIND– for the last data transfer applied to the C0 and C1 inputs (pins 5 and 6) of U36 [22D].

Control Word Transfers

The Card Control Word provides the HP-IB Interface Card with the configuration information necessary to process data through the HP-IB Chip and the backplane.

Writing the Control Word Instruction: OTA 31

The Control Word is clocked into U76 [34A] and U45 [24B] by the CLK + signal generated by U48 pin 6 [21B]. The control word is loaded into the Control register U76 [34A], U45 [24B], and U14 [22B]. U76 and U45 are the same register used for the upper eight bits of the word mode transfer. The Control Register must be used because the BYTE + bit is necessary if a DMA transfer is to be accessed. The lower eight bits of the control word are stored into U115 [22B], a 74LS273, and provide the following functions.

Bit 0 – CARD CLEAR WHEN SET TO "1"

Bit 0 triggers U49 [23A], a 74LS221, and the one-shot produces the card reset pulse. The output of U6l pin 12 is gated with RST– in U68 [23A], a 74LS00, to provide the card with a universal reset pulse CLR–. This pulse initializes the card without affecting the rest of the system and clears the Control Register, resetting bit 0.

Bit 1 – DO A PARALLEL POLL

When bit 1 is set to a "1", it holds off the generation of the N + 1 SRQ signal until U147 and U146 [33E], a 74LS393 and a 74LS00 (the 5 micro-second Parallel Poll Timer), generate a "0" at U146 pin 8. This circuit counts approximately 23 SCLK + periods to generate the 5 micosecond delay for PPDONE–. This is the minimum time to ensure a valid response to a Parallel Poll. PPDONE- is applied to U26 pin 4 [24E].

Bit 2 – INTERRUPT REQUEST ENABLE (IRQEN +)

When bit 2 is set, it allows any of several interrupting conditions to generate an IRQ– through U15 [22C], a 74LS20, into the I/O Master that sets the device flag (flag 30). This generates an interrupt if the interrupt system is enabled and control 30 is set. The interrupt conditions are as follows:

- A bus SRQ (if enabled)
- A secondary address (if enabled)
- An HP-IB Chip interrupt
- A Group Execute Trigger

Bit 3 – DELAY DMA UNTIL AN INTERRUPT CONDITION EXISTS

When bit 3 is set to "1", it disables the DMA start-up latch U37 [23D], holding off the start-up of a DMA transfer until one of the four interrupt conditions listed previously exists.

Bit 4 – ENABLE SRQ FROM THE BUS

When bit 4 is set to "1", it enables a bus SRQ to be one of the interrupting conditions discussed in the description of BIT 2. U125 [23C], a 74LS00, gates this bit and BUSRQ + from the bus receivers to provide the signal SRQINT–.

Bit 5 – NOT USED

Bit 6 – FREEZE DMA

When bit 6 is set to a "1", a DMA transfer will be frozen when an interrupt condition occurs. This bit is gated through U68 [22C], a 74LS00, to disable the N + 1 SRQ signal and through U16 [21D], a 74S02, to disable SACK- and DMAEN– to stop DMA in the exact state at which the interrupt occurred.

Bit 7 – ENABLE MY SECONDARY ADDRESS

When bit 7 is set to a "1", it allows the reception of a secondary address to be considered as one of the interrupting conditions discussed in the description of BIT 2. Bit 7 is gated with the "Q" output of the secondary address latch U78 pin 9 [25C], a 74LS74, through U125 [23C], a 74LS00.

Bits 8 through 11 are stored in U45 [24B], a 74LS175, and provide the following functions for DMA byte mode transfers.

Bit 8 – ATTENTION (ATN)

When bit 8 is set to a "1" during an output transfer (bit 15 = 1), it tags each byte transferred with ATN through U44 [25B] as discussed in the Word Mode Transfer section.

When bit 8 is set to a "1" during an input transfer, it asserts the signal LSBYT– into the I/O Master through U25 [23C, 24C], a 74S02, if the byte being read from the FIFO is a secondary address.

Bit 9 – END OF RECORD

When bit 9 is set to a "1" during an output transfer, it tags the last byte transferred with EOI indicating an end of record. When gated through U77 [25B], a 74LS02, bit 9 drives the EOI bit through U44 [25B] when DMAEN– goes high during the last byte of the transfer.

When bit 9 is set to a "1" during an input transfer, it allows the end of record detected by the Tag Bit Decoder U24 [26C], a 74S138, to terminate the DMA transfer. These signals are gated through U25 [23C, 24C], a 74S02, to assert the signal LSBYT–.

Bit 10 – BYTE MODE

When bit 10 is set to a "1", it indicates that the forthcoming transfer is a byte mode transfer (BYTE+). When bit 10 is set to a "0", it indicates that the forthcoming transfer is a word mode transfer (WORD+).

Bit 11 – FORCED READ

When bit 11 is set to a "1", it enables the FIFO to be flushed by a DMA transfer signal (FORCE-). It modifies the input to U135 [33C], a 74LS27, via U47 [34C], a 74LS00, to indicate that the read is from other than the FIFO.

Bits 12 through 15

These bits indicate the HP-IB Chip register that will be referenced by the byte mode transfer. The bits are loaded into U76 [34A]. Bit 15 indicates the direction of data flow. If set to a "1", data is being read from the register selected by bits 12–14. A "0" indicates a write operation to the selected register.

Reading the Control Word Instruction: LI* 31

The lower eight bits (bits 0 through 7) are read out of the Control Register U115 [22B], a 74LS273, by U85 [21B], and driven onto the buffered data bus during the time that bus control state 6 (BCS6–) is asserted. Bits 8 through 11 of the Control Word are read from U45 [24B], by a multiplexer U65 [23B], a 74LS258, and driven onto the buffered data bus by BCS6– (LDCNTRL). The select function of the multiplexer is performed by applying BCS7– to select the input (U65 pin 1). BCS7– is high when the control word is to be loaded, thus selecting the 'B' inputs. The enable signal is the product of U26 (pin 11) [21B], a 74LS00, gating BCS6– or BCS7– that enables U65 to drive bits 8 through 11 onto the buffered data bus whenever status or control is to be loaded. Bits 12 through 15 are stored in U76 [34A], a 74LS175, and are read back by U66 [25B], in the same manner as U65 functions. The only difference is the enabling signal that drives bits 12 through 15 onto the buffered data bus. It is a NOR function of BCS5–, BCS6–, and BCS7–.

Status Word Transfers

The Status Register reflects the present state of the interface and the bus. The Status Register is cleared by removing the condition which caused the bit to be set. The exception to this is the secondary address bit (bit 12), which can be cleared only by executing an OT* 32 instruction. The state of the other bits in the Status Register are not affected by this operation no matter what data pattern is transmitted. The individual meanings of the status bits are defined in chapter 3 under "Status Register".

Reading the Status Register Instruction: LI* 32

The Status Registers U66, U65, and U34 [25B, 23B, and 28B], two 74LS258's and a 74LS244, are enabled onto the data bus by BCS7– (LDSTAT). U66 [25B], drives the upper four bits (bits 12 through 15) of status selected by BCS7– applied to the select input (pin 1) of U66. The next four bits (bits 8 through 11 are driven through U65 [23B], a 74LS258, which also has BCS7– as its select input signal. The lower eight bits (bit 0 through 7) of the Status Register are the product of the eight switches making up U144, the HP-IB Address Select switch. These eight bits are driven onto the buffered data bus by U134 [27B], a 74LS244, which is also enabled by BCS7–. The switches are labeled 1 through 8, corresponding to bits 7 through 0 on the buffered data bus.

HP-IB Bus Operation

Communication on the HP-IB bus interface is accomplished by the HP-IB Interface Controller Chip (referred to as the HP-IB Chip), U117 [35B], and the bus transceivers, U87, U88, and U128 [37B, C, D]. Circuitry to detect an HP-IB system bus error condition includes U127 [36D] and a portion of U68 [37d].

Transceiver Operation

The HP-IB transceivers (U87, U88, and U128) [36 and 37B, C, D] consist of one octal and two quad driver/receiver ICs. The HP-IB Chip's output HSE (High State Enable) is applied to U128 and part of U87. It is asserted whenever the DIOn, DAV, or EOI lines are required by the HP-IB system. When HSE inputs are high, they activate an internal pull-up network. The DIOE output (pin 9) of the HP-IB Chip is used to drive the TE input of U128. This output drives the signals out onto the HP-IB lines when it is high and receives the signals off the lines when it is low. The optional pull-up and pull-down resistor pack, U119, increases the drive for the HP-IB system lines. Refer to chapter 2 for further information about this resistor pack.

The HP-IB Chip's Data Lines (DIO1– through DIO8–) are connected to U128, and the eight HP-IB Control Signals are driven and received by U87 and U88. The other HP-IB Control Line descriptions are covered in chapter 7, figure 7-1.

HP-IB Chip Options

Speed of Operation (U1S2).

The resistor capacitor combination (R7, C20) connected to the HP-IB Chip (U117, pin 42) selects the time delay between the assertion of the data on the bus and the assertion of data valid. If this switch, U1S2, is open, it provides a 500-nanosecond settling time. This settling time satisfies the requirements for the IEEE Standard 488-1978. Some peripherals require a faster settling time of 350 nanoseconds. This speed is achieved by closing the switch U1S2, which connects R7 and R8 in parallel, reducing the effective resistance from U117, pin 42 to ground, thus reducing the settling time delay.

System Controller Select (U1S1).

The switch U1S1 [34D], determines whether the card will be the System Controller. If the switch is open, the card will be the System Controller. Setting the switch to the open position puts a "1" on pin 7 (SCTRL) and pulls REN and IFC low.

HP-IB Error Detection

Jumper-selectable circuitry (U127 [36D] and part of U68 [37D]) allows detection of a particular HP-IB error condition as defined in IEEE Standard 488-1978, Appendix B. This condition (NDAC and NRFD both high preceding application of data on the DIO lines) can exist if a listening device has been powered down or taken off line, allowing NDAC and NRFD to float. If jumper W1 is removed, and if both NDAC and NRFD are sensed as high preceding a data transfer, the error detection circuit will cause the HP-IB Chip to have a low value on its RFD input (U117 pin 16). With RFD low and DAC high, no data transfer will occur until DAC goes low (at which time RFD to the HP-IB Chip will go high). If both NDAC and NRFD on the HP-IB bus remain high, an error at the software driver level will occur, assuming that a finite timeout value has been specified. With W1 installed, the error detection circuitry is disabled, but system operation is not degraded.

Responding to an HP-IB Error

Normal Reconnection

After detecting an NRFD-NDAC error, inspect your HP-IB to find the device that has been disconnected from the bus. Once you find the device, follow the shut-down procedures for the device and the computer where the HP-IB interface is installed. When everything is turned off, re-attach the HP-IB cable to the device and follow the normal power-up procedures for the device and the computer.

Emergency Reconnection

The following information will help you design an emergency reconnection procedure for your operation. This is not a tutorial on emergency procedures but is intended to start you thinking about your need for an emergency reconnection plan and the resources required to make it work.

The procedure listed below is very general. You will need to design your own to suit your installation and resources.

Warning

The metal case of the HP-IB connector is grounded. DO NOT touch the case with one hand and a voltage source with any other part of your body or you may receive a shock.

Caution

This procedure describes making a connection with the power turned on. Keep wires or other conductors from coming in contact with the pins inside the HP-IB connector or a short-circuit may occur.

Note Hewlett-Packard Company assumes no responsibility for the correctness of the procedure listed below in your particular situation or installation.

General Procedure

1. Locate the disconnected cable.
2. Turn off the power to the disconnected HP-IB device.
3. Run a program that will bring the HP-IB to a quiescent state.
4. Turn the HP-IB device back on.
5. Pick up the loose end of disconnected cable by the HP-IB connector.
6. Align the connector in your hand with the connector it was attached to. Then push your connector into the other and secure the knurled screws. When both mounting screws are secured, put down the cable.
7. Run the initialization or recovery program written for the device you have just re-attached. This concludes the procedure.

5 Maintenance

This chapter gives maintenance information for the HP 12009A HP-IB Interface.

Preventive Maintenance

Check the HP-IB Interface when you check your computer system.

Caution

Some of the components used in this product are susceptible to damage by static discharge. Refer to the safety considerations at the front of this manual before handling the card.

Inspect the card for burned or broken components or foreign material. Check the cable and connectors that connect the card to the bus for damaged insulation, bent or broken pins, etc. After any damage has been repaired, run the system self-test. (Refer to the appropriate System Installation and Service Manual.) If the card is malfunctioning, perform the troubleshooting procedures listed below.

Troubleshooting

To troubleshoot the HP-IB Interface:

1. Run the computer self-test. Refer to the *HP 1000 Model 26, 27 and 29 Computer System Installation and Service Manual,* part number 02196-90002, or the *Micro 1000 Computer System Installation and Service Manual*, part number 02430-90001.

2. Run the kernel diagnostic. Refer to the *Diagnostic Manual*, part number 24612-90011.

3. If jumper W1 has been removed, make sure a peripheral device is connected to the card and powered on. Then run the HP-IB interface diagnostic. Refer to the *HP-IB Interface Diagnostic Operating Manual*, part number 24397-90009.

Note

If jumper W1 has been removed, the interface diagnostic will fail unless a peripheral device is connected to the card and powered on.

4. If the interface is defective, contact the nearest Hewlett-Packard Sales and Support Office for information. Sales and Support Offices are listed with your system manuals.

5. Further isolation to a defective component may be performed, if necessary, using an oscilloscope or logic analyzer. See chapter 7 for integrated circuit pin connections and logic functions, a component location diagram, a functional block diagram, and the schematic logic diagram. Refer to table 6-3 for replaceable parts information and table 2-1 for interface to HP-IB cable connections.

6 Replaceable Parts

This chapter contains information for ordering replaceable parts for the HP 12009A HP-IB Interface.

Caution Any unauthorized repair of this product will invalidate the warranty.

Description	Part Number
Printed Circuit Assembly	12009-60020
Interconnecting Cable	12009-60014
Load Resistor	1810-0081

Component Parts

Table 6-2 is the list of component parts in reference designation order. Table 6-1 lists the meanings of the reference designations and abbreviations used in table 6-2. Table 6-3 contains the names and addresses of the manufacturers of the parts.

The following is listed for each part:

- Reference designation of the part. Table 6-1 gives explanations of the abbreviations used in the "Reference Designation" column.
- The Hewlett-Packard part number.
- Part number check digit (CD).
- Total quantity (QTY).
- Description of the part.
- A five-digit manufacturer's code number of a typical manufacturer of the part.
- The manufacturer's part number.

Ordering Information

To order replacement parts or to obtain information about parts, address the order or inquiry to the nearest Hewlett-Packard Sales and Support Office (listed in your systems manual).

To order a part listed in the replaceable parts list, give the Hewlett-Packard part number with the check digit to your Hewlett-Packard Sales Representative and indicate the quantity required. The check digit will ensure accurate and timely processing of your order.

To order a part that is not listed in the replaceable parts table, specify the following information:

1. Identification of the product containing the part (refer to chapter 1).
2. Description and function of the part.
3. Quantity required.

Table 6-1. Reference Designations and Abbreviations

Reference Designations

A = assembly	K = relay	TB = terminal board
B = motor, synchro	L = inductor	TP = test point
BT = battery	M = meter	U = integrated circuit, non-repairable assembly
C = capacitor	P = plug connector	
CB = circuit breaker	Q = semiconductor device other than diode or integrated circuit	V = vacuum tube, photocell, etc.
CR = diode		VR = voltage regulator
DL = delay line	R = resistor	W = jumper wire
DC = indicator	RT = thermistor	X = socket
E = Misc electrical parts	S = switch	Y = crystal
F = fuse	T = transformer	Z = tuned cavity, network
FL = filter		
J = receptacle connector		

Abbreviations

A = amperes	gra = gray	PC = printed circuit
ac = alternating current	grn = green	PCA = printed-circuit assembly
Ag = silver		PWB = printed-wiring board
Al = aluminum	H = henries	phh = phillips head
ar = as required	Hg = mercury	pk = peak
adj = adjust	hr = hour(s)	p-p = peak-to-peak
assy = assembly	Hz = Hertz	pt = point
	hdw = hardware	prv = peak inverse volage
b = base	hex = hexagon, hexagonal	PNP = positive-negative-positive
bp = bandpass		pwv = peak working voltage
bpi = bits per inch	ID = inside diameter	porc = porcelain
blk = black	IF = intermediate frequency	posn = position(s)
blu = blue	in. = inch, inches	pozi = pozidrive
brn = brown	I/O = input/output	
brs = brass	int = internal	rf = radio frequency
Btu = British thermal unit	incl = include(s)	rdh = round head
Be Cu = beryllium copper	insul = insulation, insulated	rms = root-mean-square
	impgrg = impregnated	rwv = reverse working voltage
cpi = characters per inch	incand = incandescent	rect = rectifier
coll = collector	ips = inches per second	r/min = revolutions per minute
cw = clockwise		RTL = resistor-transistor logic
ccw = counterclockwise	k = kilo (10^3), kilohm	
cer = ceramic		s = second
com = common	lp = low pass	SB, TT = slow blow
crt = cathode-ray tube		Se = selenium
CTL = complementary-transistor logic	m = milli (10^{-3})	Si = silicon
	M = mega (10^6), megohm	scr = silicon controlled rectifier
cath = cathode	My = Mylar	
Cd pl = cadmium plate	mfr = manufacturer	sst = stainless steel
comp = composition	mom = momentary	stl = stl
conn = connector	mtg = mounting	spcl = special
compl = complete	misc = miscellaneous	spdt = single-pole, double-throw
	met.ox. = metal oxide	spst = single-pole, single-throw
dc = direct current	mintr = miniature	
dr = drive		Ta = tantalum
DTL = diode-transistor logic	n = nano (10^{-9})	td = time delay
depc = deposited carbon	nc = normally closed or no connection	Ti = titanium
dpdt = double-pole, double-throw		tgl = toggle
dpst = double=pole, single-throw	Ne = neon	thd = thread
	no. = number	tol = tolerance
em = emitter	n.o. = normally open	TTL = transistor-transistor logic
ECL = emitter-coupled logic	np = nickel plated	
ext = external	NPN = negative-positive-negative	
encap = encapsulated	NPO = negative-positive zero (zero temperature coefficient)	U(μ) = micro (10^{-6})
elctit = electrolytic		
		V = volt(s)
F = farads	NSR = not separately replaceable	var = variable
FF = flip-flop	NRFR = not recommended for field replacement	vio = violet
flh = flat head		Vdcw = direct current working volts
flm = film		
fxd = fixed	OD = outside diameter	
filh = fillister head	OBD = order by description	W = watts
	orn = orange	ww = wirewound
G = giga (10^9)	ovh = oval head	wht = white
Ge = germanium	oxd = oxide	WIV = working inverse voltage
gl = glass		
gnd = ground(ed)	P = pico (10^{-12})	yel = yellow

Table 6-2. HP 12009A Component Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12009-60020	0	1	PCA-A/L HPIB	28480	12009-60020
C1	0160-6500	7	27	CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C2	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C3	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C4	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C5	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C6	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C7	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C8	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C9	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C10	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C11	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C12	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C13	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C14	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C15	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C16	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C17	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C18	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C19	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C21	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C22	0160-4808	4	1	CAPACITOR-FXD 470PF +-5% 100VDC CER	28480	0160-4808
C23	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C24	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C25	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C26	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C27	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C28	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
C29	0160-4801	7	2	CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C30	0160-4801	7		CAPACITOR-FXD 100PF +-5% 100VDC CER	28480	0160-4801
C31	0160-6500	7		CAPACITOR-FXD .01UF +-10% 100VDC CER	02802	CAC02X7R103K100C
R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	0698-4266	7	3	RESISTOR 3.3K 5% .125W F TC=0+-100	24546	C4-1/8-T0-3301-J
R3	0698-4266	7		RESISTOR 3.3K 5% .125W F TC=0+-100	24546	C4-1/8-T0-3301-J
R4	0757-0394	0	1	RESISTOR 51.1 1% .125W F TC=0+-100	24546	C4-1/8-T0-51R1-F
R5	0698-4266	7		RESISTOR 3.3K 5% .125W F TC=0+-100	24546	C4-1/8-T0-3301-J
R6	0757-0442	9	3	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R7	0757-0199	3	1	RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R8	0698-3162	0	1	RESISTOR 46.4K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4642-F
R9	0698-3155	1	2	RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R10	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
R11	0698-3155	1		RESISTOR 4.64K 1% .125W F TC=0+-100	24546	C4-1/8-T0-4641-F
R12	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R13	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
U1	3101-2243	6	2	SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U11	1820-1322	2	5	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U12	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U13	1820-1240	3	2	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U14	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N

Table 6-2. HP 12009A Component Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U15	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U16	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U17	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U18	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U21	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U22	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U24	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U25	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U26	1820-1197	9	5	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U27	1820-1112	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U28	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U31	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U32	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U34	1820-1077	4	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U35	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U36	1820-0998	6	1	IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN74S153N
U37	1820-1206	1	2	IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U38	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U41	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U42	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U44	1820-2024	3	7	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U45	1820-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U46	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U47	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U48	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
U49	1820-1437	0	1	IC MV TTL LS MONOSTBL DUAL	01295	SN74LS221N
U51	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U52	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U61	1TL2-0002	4	1	BICKS	28480	1TL2-0002
U62	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U64	1820-2102	8	8	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U65	1820-1439	2	2	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258BN
U66	1820-1439	2		IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE	01295	SN74LS258BN
U67	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U68	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U72	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U74	1820-2075	4	2	IC TRANSCEIVER TTL LS BUS OCTL	01295	SN74LS245N
U75	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U76	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U77	1820-1144	6	2	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U78	1820-1144	6		IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U84	1820-2075	4		IC TRANSCEIVER TTL LS BUS OCTL	01295	SN74LS245N
U85	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U87	1820-2058	3	2	IC TRANSCEIVER TTL S INSTR-BUS IEEE 488	04713	MC3448AL
U88	1820-2058	3		IC TRANSCEIVER TTL S INSTR-BUS IEEE-488	04713	MC3448AL
U101	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U102	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U111	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N

Table 6-2. HP 12009A Component Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U112	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U114	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U115	1820-1730	6	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U117	1TL1-0005	5	1	HP-IB INTERFACE CONTROLLER	28480	1TL1-0005
U119	1810-0081	7	1	NETWORK-RES 18-DIP MULTI-VALUE	28480	1810-0081
U122	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U123	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U124	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U125	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U127	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U128	1820-2485	0	1	IC TRANSCEIVER TTL LS INSTR-BUS IEEE-488	01295	SN75160AN
U132	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U133	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U134	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U135	1820-1206	1		IC GATE TTL LS NOR TPL 3-INP	01295	SN74LS27N
U136	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U137	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U142	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	34335	AM74LS374AP
U143	1810-0286	4	1	NETWORK-RES 16-DIP10.0K OHM X 15	01121	316A103
U144	3101-2243	6		SWITCH-RKR DIP-RKR-ASSY 8-1A .05A 30VDC	28480	3101-2243
U145	1820-1445	0	1	IC LCH TTL LS 4-BIT	01295	SN74LS375N
U146	1820-1197	9		IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U147	1820-2096	9	1	IC CNTR TTL LS BIN DUAL 4-BIT	01295	SN74LS393N
W1	0811-3716	2	1	RESISTOR ZERO OHM	28480	0811-3716
XU61	1200-1011	2	1	SOCKET-IC 64-CONT SQUARE DIP-SLDR	28480	1200-1011
XU79	1200-0539	7	2	SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
XU119	1200-0539	7		SOCKET-IC 18-CONT DIP DIP-SLDR	28480	1200-0539
	0403-0289	3	2	EXTR-PC BD RED POLYC .063-BD-THKNS	28480	0403-0289
	1480-0116	8	1	PIN-GRV .062-IN-DIA .25-IN-LG STL	28480	1480-0116

Table 6-3. Code List of Manufacturers

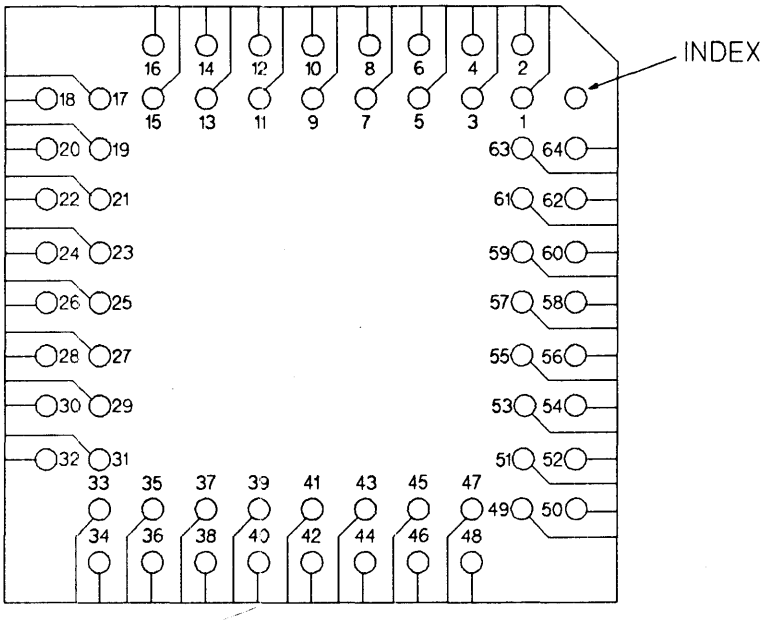
Code	Manufacturer	Location	
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instruments Inc	Dallas, TX	75265
02802	American Safety Razor Co Div Philip	Staunton, VA	24401
04713	Motorola Inc Semi-conductor Prod	Phoenix, AZ	85008
24546	Corning Electronics	Santa Clara, CA	95050
27014	National Semiconductor Corp	Santa Clara, CA	95052
28480	Hewlett-Packard Co Corporate Hq	Palo Alto, CA	94304
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086

7 Service Diagrams

This chapter contains the following service diagrams for the HP-IB Interface Card:

- Figure 7-1. Integrated Circuit Base Diagrams
- Figure 7-2. HP-IB Interface Card Component Location Diagram
- Figure 7-3. HP-IB Interface Card Functional Block Diagram
- Figure 7-4. HP-IB Interface Card Schematic Logic Diagram

Base diagrams of the integrated circuits used on the card are shown in figure 7-1. A component location diagram is shown in figure 7-3.



I/O Chip Outline (Component Side)

Pin Definitions – I/O Processor Chip

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	DMACYC–	17	GND	33	BRNI +	49	VCC
2	LDMAR +	18	VDD	34	CRS +	50	GND
3	SCEN–	19	CW1–	35	IEN–	51	VDD
4	REMOTE–	20	BCW2 +	36	DIAG–	52	CB7 +
5	INTCYC +	21	BCW1 +	37	DVCMD–	53	CB8 +
6	DMAEN–	22	BCW0 +	38	PLSLV +	54	CB9 +
7	LOBYT–	23	BVALID +	39	PON +	55	CB10 +
8	SACK–	24	BIOGO +	40	SLACK +	56	CB11 +
9	NC	25	ICHID–	41	SLRQ +	57	CB12 +
10	SCLK +	26	BIAK +	42	CB0 +	58	CB13 +
11	LSBYT–	27	CFF–	43	CB1 +	59	CB14 +
12	BPE +	28	PULIOR–	44	CB2 +	60	CB15 +
13	BMP–	29	IOEN–	45	CB3 +	61	MEMGO +
14	CHSRQ–	30	IOCLK +	46	CB4 +	62	MRQ +
15	IRQ–	31	PRDIS–	47	CB5 +	63	NC
16	VCC	32	GND	48	CB6 +	64	GND

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 1 of 5)

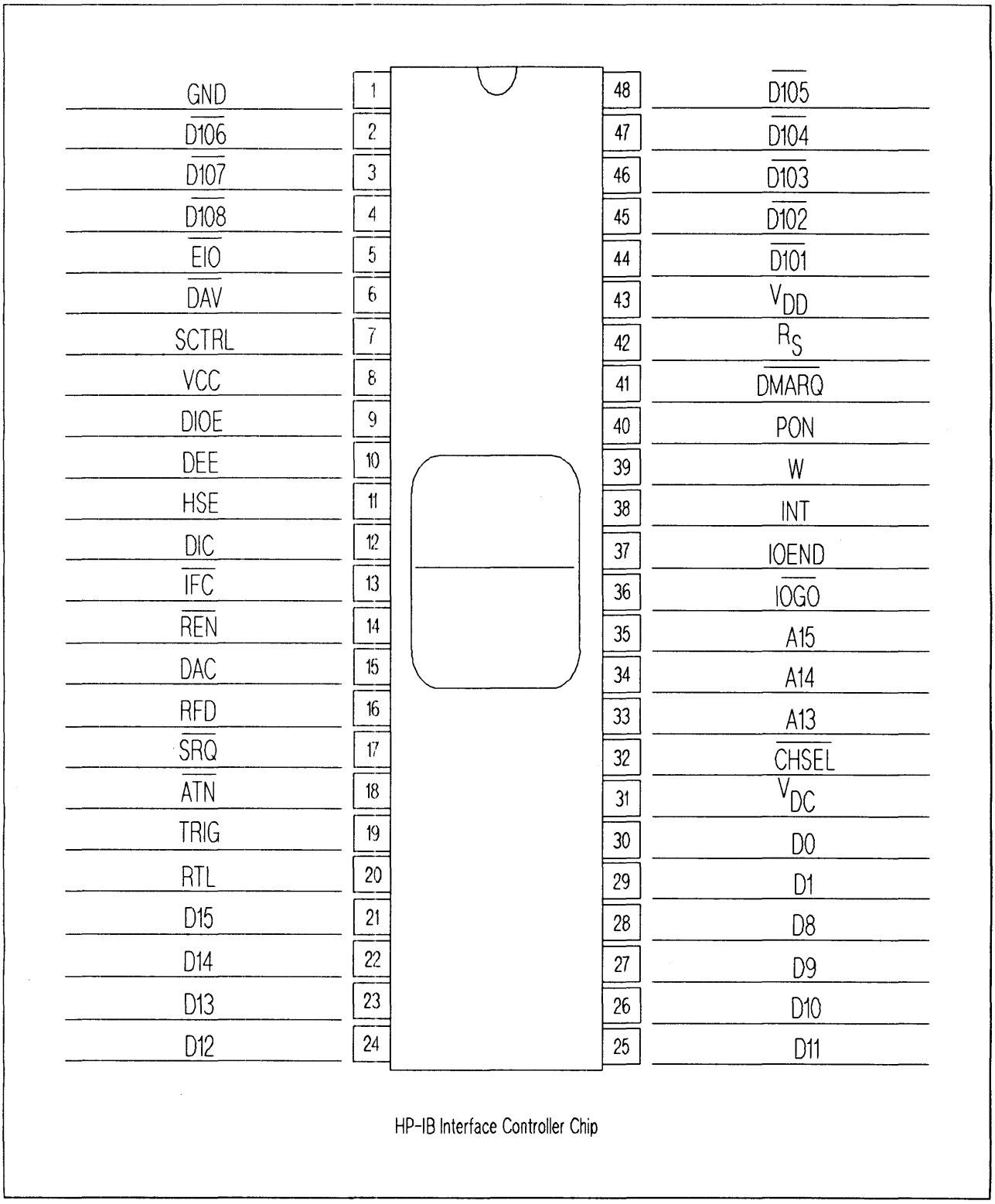


Figure 7-1. Integrated Circuit Base Diagrams (Sheet 2 of 5)

HP-IB Data Lines - low true			
Pin No.	**Mnemonic**	**Type**	**Description**
44	DI01–	B	Data Input/Output, Bit 1 - low true
45	DI02–	B	.
46	DI03–	B	.
47	DI04–	B	.
48	DI05–	B	.
2	DI06–	B	.
3	DI07–	B	.
4	DI08–	B	Data Input/Output, Bit 8 - low true

HP-IB Handshake Lines			
Pin No.	**Mnemonic**	**Type**	**Description**
18	ATN–	B	Attention
16	RFD	B	Ready for Data
15	DAC	B	Data Accepted

HP-IB Bus Management Lines - low true			
Pin No.	**Mnemonic**	**Type**	**Description**
6	DAV–	B	Data Available
5	EOI–	B	End or Identify
14	REN–	B	Remote Enable
13	IFC–	B	Interface Clear
17	SRQ–	B	Service Request

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 3 of 5)

Internal Data Lines			
Pin No.	**Mnemonic**	**Type**	**Description**
30 29	D0 D1	B B	These two bits indicate the following conditions when read from register 2: D0 D1 — — 0 0 Normal data 0 1 Secondary Address 1 0 Last byte of subgroup 1 1 Last byte of record
28	D8	B	Data Bus, Bit 7
27	D9	B	Data Bus, Bit 6
26	D10	B	Data Bus, Bit 5
25	D11	B	Data Bus, Bit 4
24	D12	B	Data Bus, Bit 3
23	D13	B	Data Bus, Bit 2
22	D14	B	Data Bus, Bit 1
21	D15	B	Data Bus, Bit 0
33	A13	I	Address Bit 13
34	A14	I	Address Bit 14
35	A15	I	Address Bit 15
7	SCTRL	I	Makes HP-IB card System Controller
40	PON	I	Power On – when low, initializes HP-IB chip for >500 nsec
39	W	I	Write enable, read disable
36	IOGO–	I	Initiates a register read/write
32	CHSEL–	I	Enables IOGO–

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 4 of 5)

Internal Data Lines (continued)			
Pin No.	**Mnemonic**	**Type**	**Description**
41	DMARQ–	O	DMA request, indicating that the HP-IB chip FIFO register is ready
38	INT–	O	Requests interrupt
37	IOEND–	O	Handshake complete
19	TRIG	O	Pulse generated when HP-IB card gets Group Execute Trigger (GET)
12	CIC	O	Enables ATN driver when true and SRQ driver when false
11	HSE	O	Transceivers use active pullups (vs open collector)
10	DEE	O	DAV/EOI enable (send DAV and EOI, vs receive)
9	DIOE	O	DIO enable (send data, vs receive)
43	VDD	P	+12V
1	GND	P	Ground
8	VCC	P	+5V
31	VDC	P	+5V
42	RS	T	Delay stabilizing resistor
20	RTL	I	Return to local (tied permanently false)

Line types: B = Bidirectional
I = Input
O = Output
P = Power
T = Timing

Figure 7-1. Integrated Circuit Base Diagrams (Sheet 5 of 5)

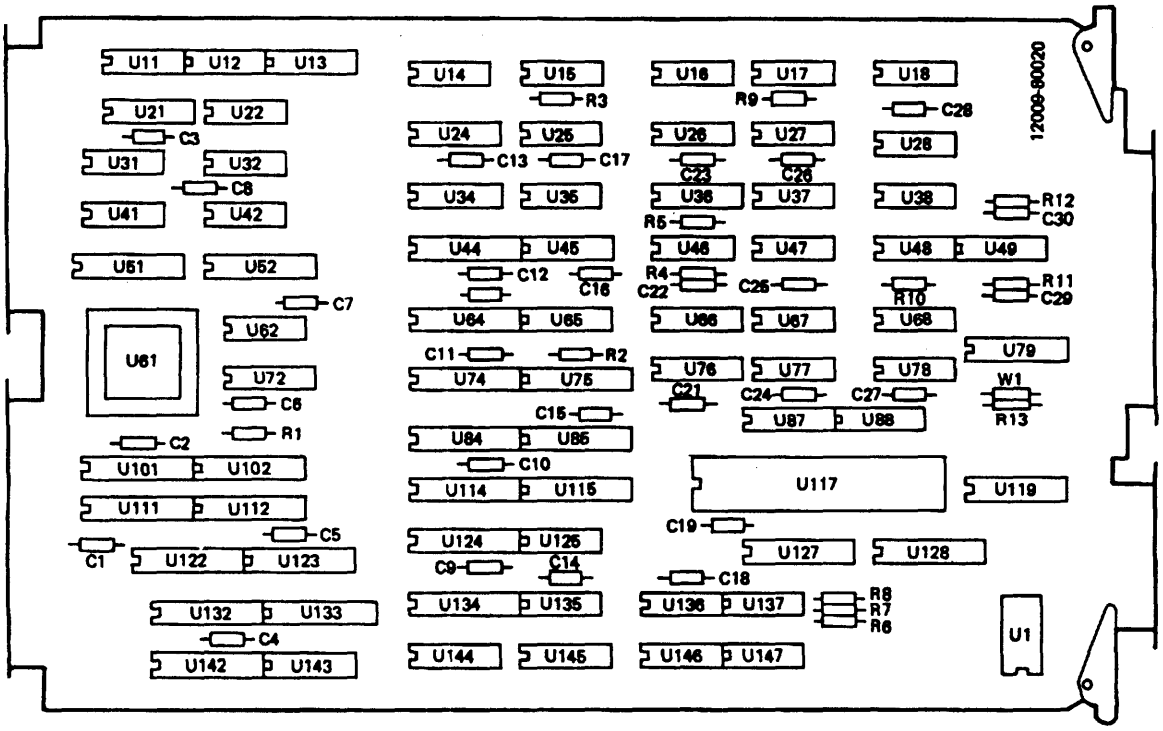


Figure 7-2. HP-IB Interface Card Component Location Diagram

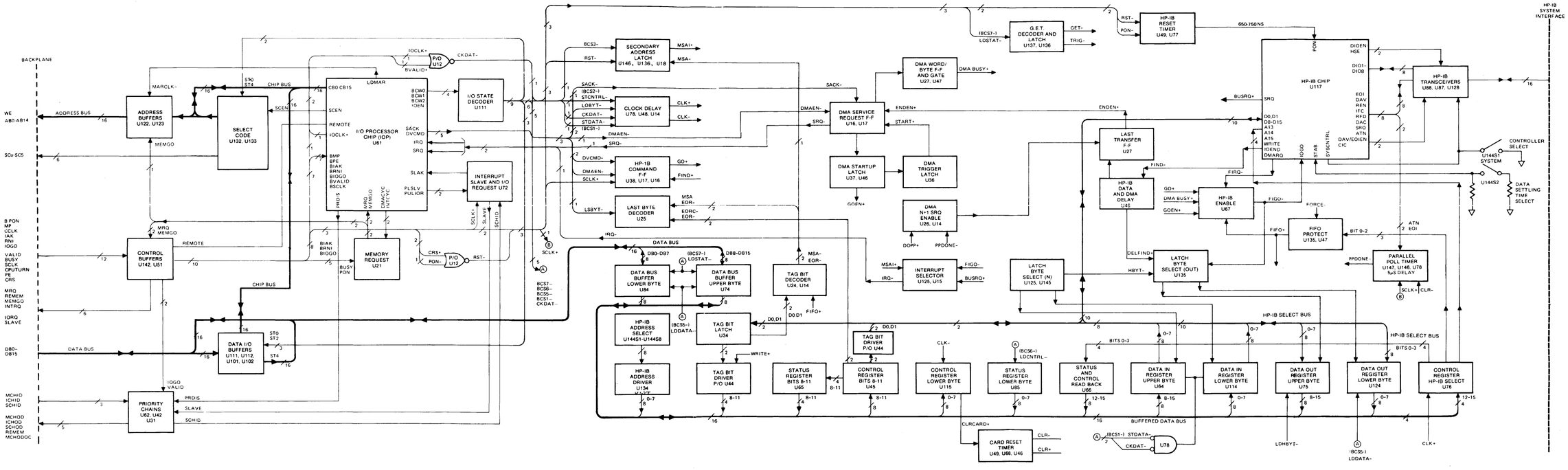


Figure 7-3. HP-IB Interface Card Functional Block Diagram

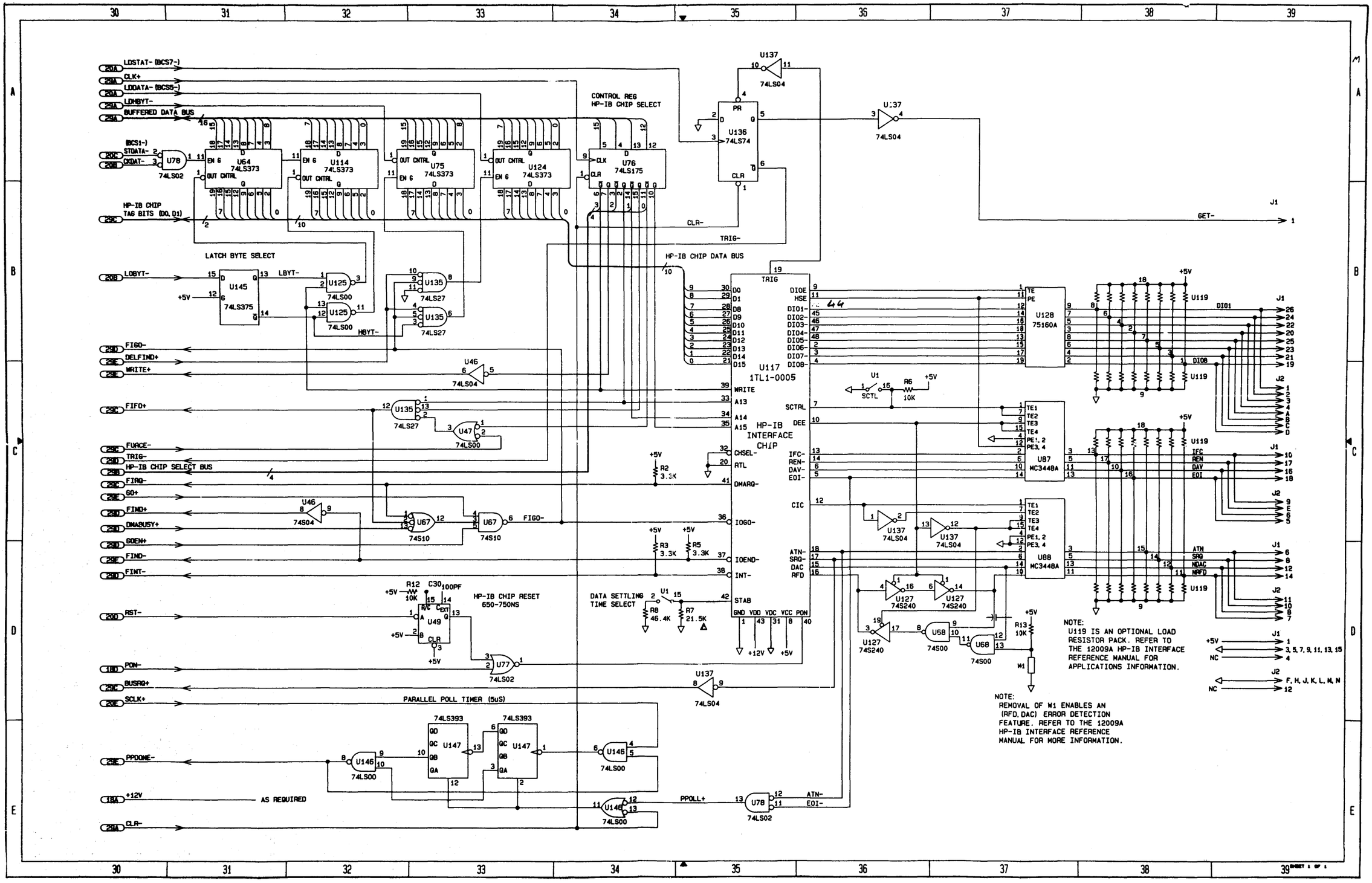


Figure 7-4. HP-IB Interface Card Schematic Logic Diagram (Sheet 1 of 3)

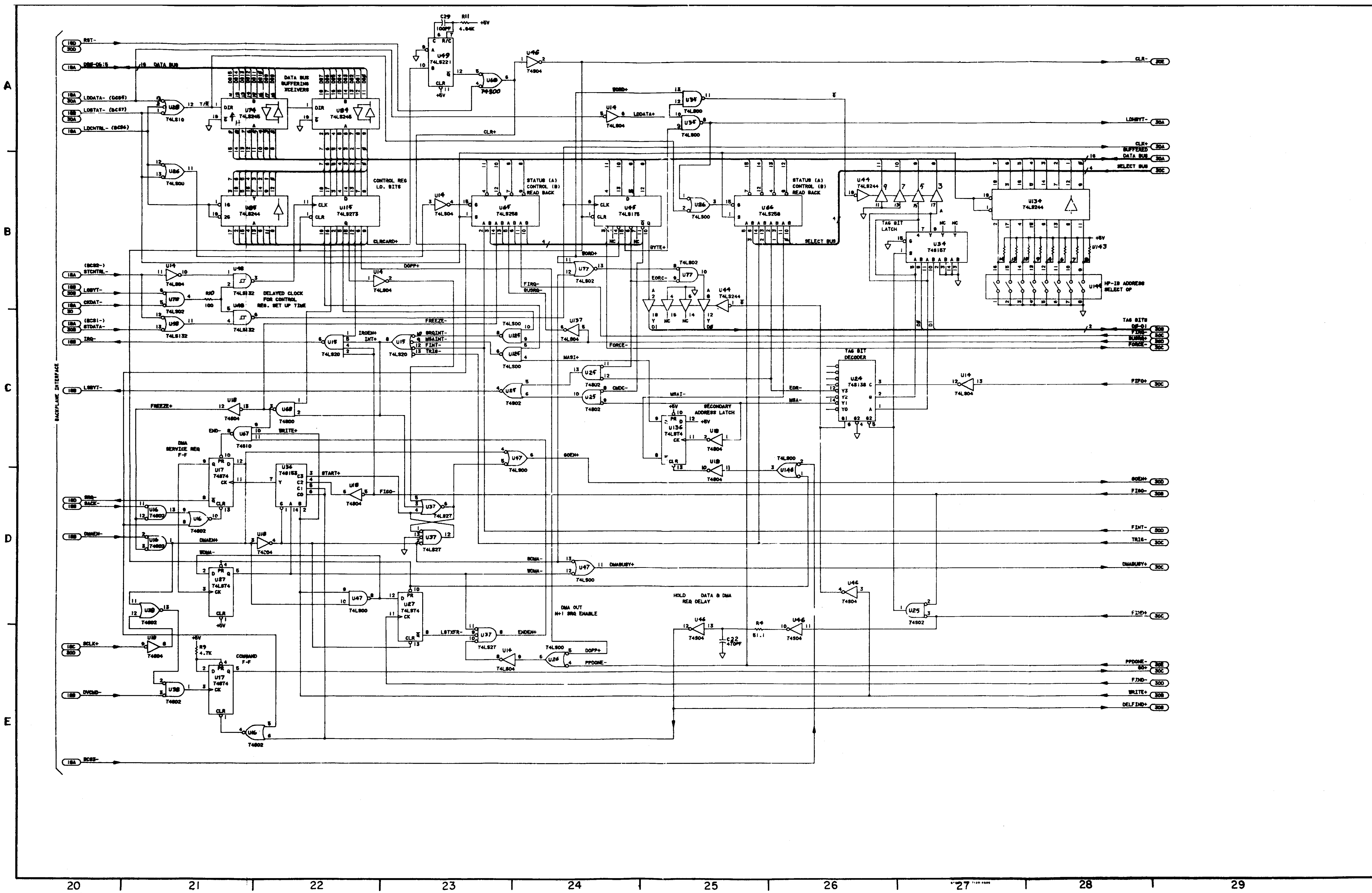


Figure 7-4. HP-IB Interface Card Schematic Logic Diagram (Sheet 2 of 3)

Figure 7-4. HP-IB Interface Card Schematic Logic Diagram (Sheet 3 of 3)

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Manual Part Number: 12009-90001
Edition 3 E1288
Printed in U.S.A., December 1988

HEWLETT PACKARD