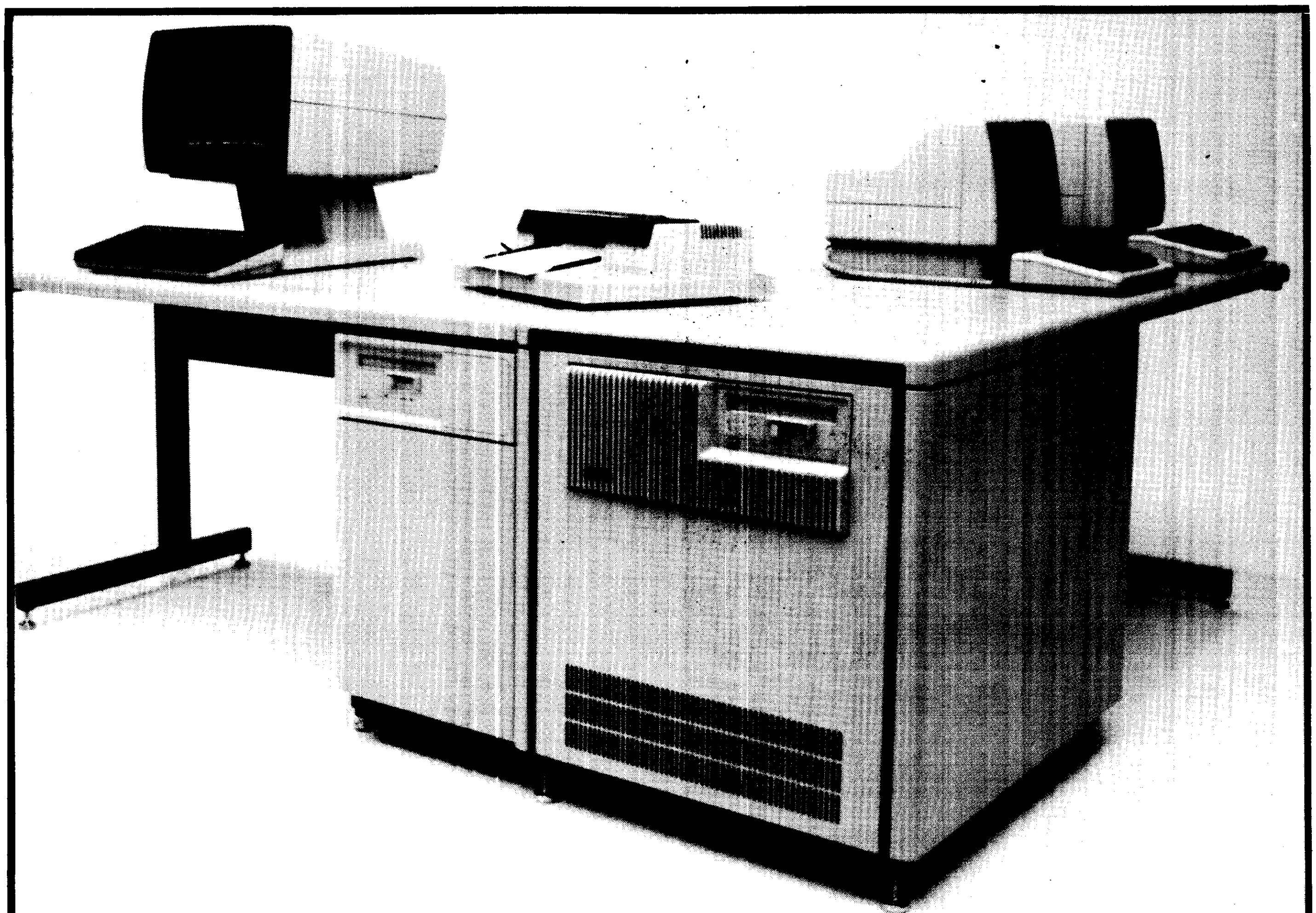
HEWLETT PACKARD

HP 1000 A700 Computer

Engineering and Reference Documentation

HP1000 A-Series



HP 1000 A700 Computer

Engineering and Reference Documentation

HEWLETT
PACKARD

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PRINTING HISTORY

The Printing History below identifies the Edition of this Manual and any Updates that are included. Periodically, Update packages are distributed which contain replacement pages to be merged into the manual, including an updated copy of this Printing History page. Also, the update may contain write-in instructions.

Each reprinting of this manual will incorporate all past Updates, however, no new information will be added. Thus, the reprinted copy will be identical in content to prior printings of the same edition with its user-inserted update information. New editions of this manual will contain new information, as well as all Updates.

To determine what software manual edition and update is compatible with your current software revision code, refer to the appropriate Software Numbering Catalog, Software Product Catalog, or Diagnostic Configurator Manual.

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NOTICE

Many of the schematic diagrams and parts lists in this document contain the generic number (manufacturer's number) of the IC packs. These are for your convenience when referring to pack diagrams and general operating conditions in semiconductor manufacturer's catalogs. The generic number, however, should not be used to order replacement parts from Hewlett-Packard. Many parts used in Hewlett-Packard equipment are purchased with special specifications and tolerances, or may undergo special testing and treatment (such as burn-in). Replacement parts therefore must be ordered using the Hewlett-Packard part number to insure that the replacement part will restore the equipment to its proper operating condition.

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PREFACE

Engineering and Reference information for the Hewlett-Packard HP 1000 A700 computer is contained in this document. The HP 1000 A700 computer is available as the HP 2137 rack-mountable computer, the Model 17 computer system, and as the HP 2107AK board computer.

Information is provided in this manual for the processor cards, memory array cards, memory controller card, error correcting array card, writable control store card, PROM control store card, floating point processor card, frontplane and backplane. Input/output (I/O) interfaces are not covered in this document since the detailed information is provided in other manuals. Refer to the HP 1000 A700 Computer Reference Manual, part no. 02137-90001, for a documentation map of all available HP A700 Computer manuals.

Microprogramming information and a base set listing for the HP A700 Computer are provided in the HP 92045A Microprogramming Package Reference Manual, part no. 92045-90001.

NOTE

The power supplies used with the HP 1000 A700 computer are covered in a separate manual.

This manual contains the following sections:

Section I - HP 1000 A-700 Computer System

Section II - A700 Processor System

Section III - Lower Processor Card

Section IV - Upper Processor Card

Section V - Memory Array System

Section VI - Memory Controller

Section VII - Memory Error Correcting Assembly

Section VIII - Control Store Cards

Section IX - Floating Point Processor

Section X - Backplane (Including I/O Requirements and Signal Timing)

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1.1 INTRODUCTION

The HP 1000 A700 (here after referred to as the A700 computer) computer is a user microprogrammable computer that offers the user exceptional operating flexibility. The microinstruction word is 32-bits wide which provides a larger instruction repertoire than available with lesser word widths. The writing of microprograms for this computer by the user is facilitated by a free-format language called the paraphraser. The efficiency of arithmetic operations is increased for higher speed calculations by the Floating Point Processor.

The microprogram memory control store of the A700 computer can be expanded to address up to 16k words using the writable control store card, the PROM control store card, and the floating point processor card.

1.2 PHYSICAL DESCRIPTION

The A700 computer is available in a rack-mounted HP 2137A packaged version, the HP Model 17 system version, and the HP 2107AK Board Computer. The HP 2137A and Model 17 include a 20-slot card cage where the numbered slots run from right to left and the cards are mounted in the slots side-by-side (i.e., the cards are vertical). HP Model 17 is available in two versions: the HP 2197A in a 56-inch cabinet and the HP 2197B in a 23-inch cabinet.

Figure 1-1 illustrates the HP 2107AK, the HP 2137A, the HP 2197A and the HP 2197B.

1.3 SYSTEM ENVIRONMENT

The system environment of the A700 processor is shown in Figure 1-2. The computer cards plug into a backplane which carries the logic signals, clock signals, and dc power. I/O cards also plug into the backplane. The frontplane provides internal bus signal interconnections between the processor cards, the memory controller card, the control store cards, and the optional floating point card.

The memory controller card and memory array cards are located immediately above the two processor cards and that all I/O cards and control store cards are placed below the processor in descending interrupt and DMA priority. The processor cards may go in any continguous card slots as long as these rules are preserved. Empty slots between cards are not permitted in order to guarantee interrupt and DMA priority chains. Refer to Section X, paragraph 10.2, for card slot priorities.

1.4 DESCRIPTION OF OPERATION

The basic A700 processor consists of two processor cards, memory controller card, and memory array card.

The A700 computer is designed for user microprogramming which is easier and more versatile than most other computers. Microprograms are stored in the processor's internal control store that can be expanded using any combination of one or more HP 12153A Writeable Control Store (WCS) cards, HP 12155A PROM Control Store (PCS) cards, and one only 12156A Floating Point Processor (FPP) card.

In operation, the ALU and sequence logic of the processor carries out the commands of the microinstructions of microprograms stored in the control store. These microprograms may be the standard base set of the processor or user microprograms. Most of the HP 1000 Computer Series instruction set are executed by microroutines of the base set. Microprogramming information and the base set listing are provided in the HP 92045A Microprogramming Package Reference Manual, part no. 92045-90001.

The memory controller, other than containing external registers usable by the processor, provides memory mapping. Any main memory reference from the processor or I/O card (except a boot memory access) selects one of 32 maps. Mapping expands the 32k words of logical address space to 16 megawords of physical memory. The microcode has access to the individual map registers over the frontplane. The available memory array cards contain 64k, 128k, 256k, and 512k words, and the physical address space is 16,384k words (the product initially released limits the number of array cards to four). The memory array cards automatically configure themselves in ascending address order as they are installed on the backplane. Optional 256k-word Error Correcting Assembly (ECA) cards are available which correct all single-bit errors and detect all double-bit errors and most multiple-bit errors.

An I/O read or write over the backplane can occur in any cycle. When the backplane is free, an I/O handshake is performed upon a request for a handshake from an I/O card. The I/O instructions are executed by I/O chips on the I/O cards; thus, each I/O card is capable of operating independently of the processor and provides efficient direct memory access (DMA) I/O transfers.

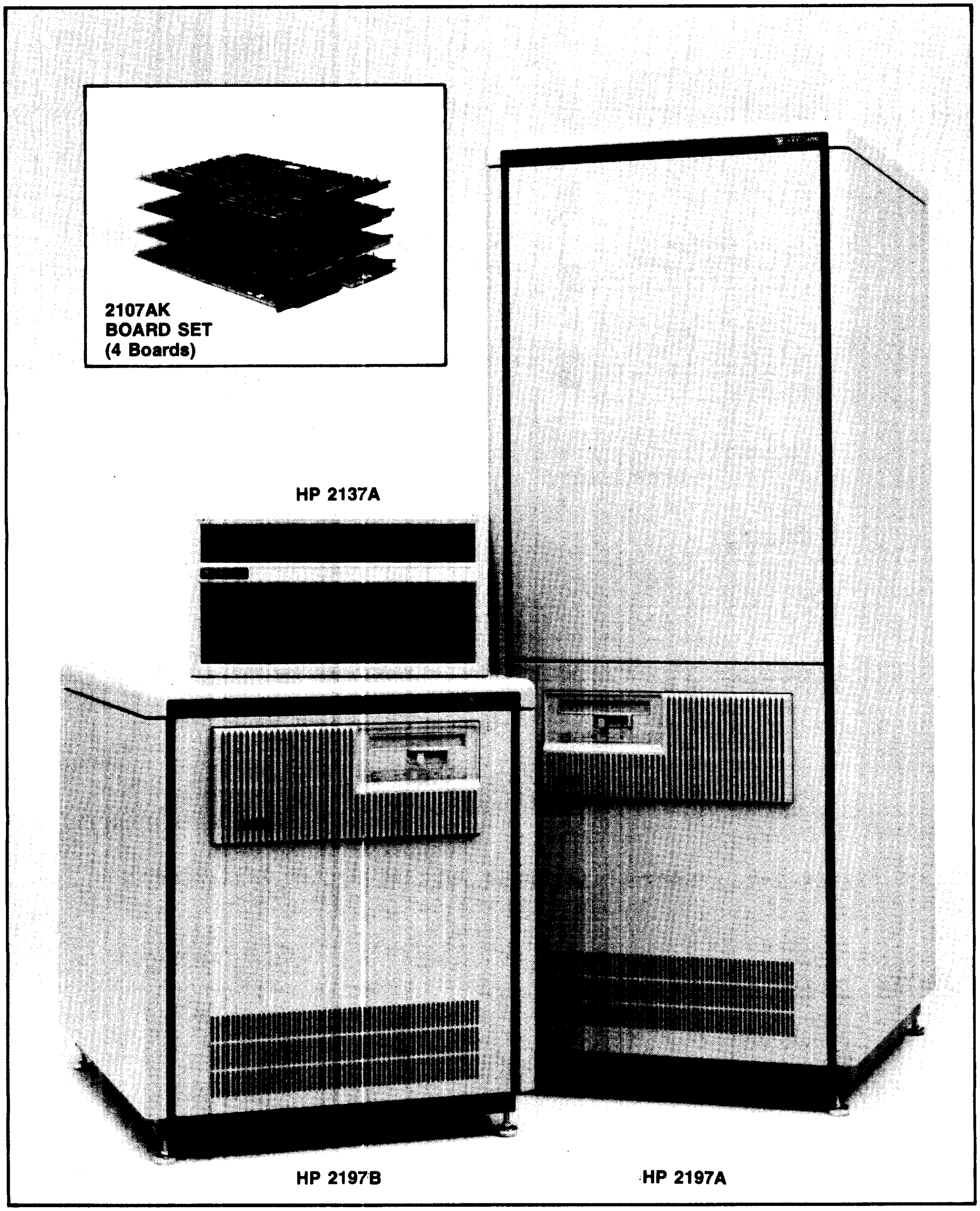


Figure 1-1. HP 1000 A700 Computers

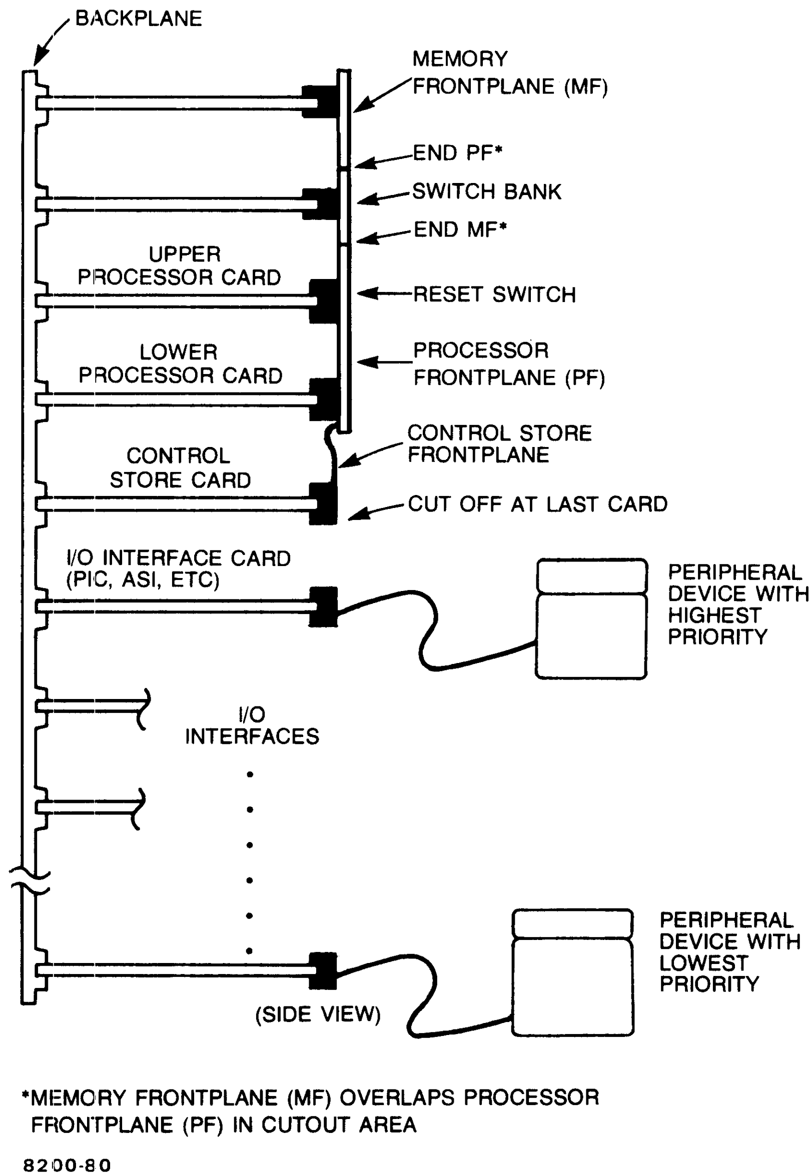


Figure 1-2. Processor Cards in Typical System Environment

1.5 SYSTEM SUPPORT FEATURES

1.5.1 VIRTUAL CONTROL PANEL

The Virtual Control Panel (VCP) is an interactive program located in a portion of the boot memory ROM located on the Memory Controller card. The VCP takes the place of a conventional control panel. Using the VCP, an operator can access internal and external registers, examine or change memory contents, and control execution of a program or load and initiate execution of the operating system or diagnostics.

The ROM code for the VCP is listed in Appendix A.

1.5.2 SELF-TEST CAPABILITY

The A-700 computer contains firmware microcode for self testing. The self-test is performed each time the power is turned on or the computer is reset.

Sixteen miniature LEDs on the frontplane are used to report operating or error status and 16 switches allow easy selection of boot loaders and auto-restart options. Refer to the HP 1000 A700 Computer Installation and Service Manual, part number 02137-90002 for a description of the LEDs and switches.

Any error during the microcoded self-test processor stops program execution with the status LEDs on the frontplane indicating the section at which the self-test failed. Failures are identified to the card level. The processor freeze is necessary since any failure of the data or address bus will prevent the computer from operating correctly. The individual LEDs will flash on consecutively in between loops of the self-test if looping is selected by the switch register (SR).

In operation the lower processor is tested first and can be the only card in the backplane. If this card passes, then the lower and the upper processors can be tested together; and if they both pass then the two processor cards followed by the memory controller card and floating point card (if installed) can be tested. Refer to the following manuals for a description of the self-test feature:

HP 1000 Models 16 and 17 Computer System Installation and Service Manual, part no. 02196-90001.

HP 1000 A700 Computer Installation and Service Manual, part no. 02137-90002.

A listing of the self-test program contained in the ROMs on the memory controller is given in Appendix A of this manual.

1.5.3 DC POWER REQUIREMENTS

DC power requirements for A700 computer cards are given in Table 1-1.

Backplane information covering items such as connector pinouts, the card cage layout, and the card cage assembly drawing is included in Section X of this document.

NOTE

Power requirements for I/O interface cards are provided in the individual manuals covering these cards.

1.6 REGULATION PROVIDED BY POWER SUPPLY

DC voltages, tolerances, and periodic and random deviation (no load to full load) specifications for the power supplies used with the A700 computer are covered in a separate power supply manual.

1.7 COOLING REQUIREMENTS

There are no external cooling requirements for the computer. Internal fans should be used to provide adequate ventilation to maintain operation within the environmental limitations specified in Table 1-1.

1.8 ENVIRONMENTAL SPECIFICATIONS

Environmental specifications are given in Table 1-2.

Table 1-1. Power Specifications

CARD	VOLTAGE	CURRENT STANDBY	CURRENT OPERATE	POWER STANDBY	POWER OPERATE
Lower Processor	+5V	--	6.2A	--	31W nom.
Upper Processor	+5V	--	5.0A	--	25W nom.
Memory Controller	+5V	0.0	4.37A	0.0	21.85W
	+5M	0.36A	0.36A	1.8W	1.8W
	TOTAL:			1.8W nom.	23W nom.
128k-Byte Array*	+5V	0.0	1.05A	0.0	5.25W
	+5M	0.45	0.99A	2.25W	4.95W
	TOTAL:			2.25W nom.	10W nom.
256k-Byte Array*	+5V	0.0	1.05A	--	5.25W
	+5M	0.50A	1.04A	2.50W	5.20W
	TOTAL:			2.50W	10W
512k-Byte Array*	+5V	0.0	1.05A	0.0W	5.25W
	+5M	0.59A	1.13A	3.01W	5.65W
	TOTAL:			3W	11W
1M-Byte Array*	+5	0.0	1.30A	0.0	6.5W
	+5M	0.87	1.41A	4.35W	7.05W
				4W nom.	13W nom.
ECA, 12104A* (512k-byte)	+5V	0.0	1.46A	0.0	7.30W
	+5M	0.63A	1.33A	3.15W	6.65W
	TOTAL:			3W nom.	14W nom.
12153A WCS	+5V	--	4.07A	--	20W nom.
12155A PCS	+5V	--	6.30A	--	32W nom.
12156A FPP	+5V	--	4.0A	--	20W nom.

* The operating power specification is not cumulative when adding additional array cards since power consumption is proportional to access rate and only one card is accessed at any one time (only one card at a time is operating). When a card is being accessed, all other cards dissipate standby power.

1.9 AC POWER REQUIRED

The AC power requirements given below apply to the power supply input.

Line Voltage	86-138 Vac (115 Vac -25%/+20% standard) 178-276 Vac (230 Vac -23%/+20% option 015)
Line Frequency	47.5 to 66 Hz.
Maximum Power Required	700 Watts

Table 1-2. Environmental Specifications

AMBIENT TEMPERATURE:	
Operating:	0 degrees to 55 degrees C (32 degrees to 131 degrees F) up to 3048 metres (10,000 ft)
	0 degrees to 45 degrees C (32 degrees to 113 degrees F) up to 4572 metres (15,000 ft)
Non-operating:	-40 degrees to 75 degrees C (-40 degrees to 167 degrees F)
RELATIVE HUMIDITY:	
5% to 95%, without condensation	
ALTITUDE:	
Operating:	to 4.6 km (15,000 ft)
Non-operating:	15.3 km (50,000 ft)
VIBRATION AND SHOCK:	
HP 1000 A700-Series products are type tested for normal shipping and handling shock and vibration. (Contact factory for review of any application that requires operation under continuous vibration.)	

1.10 CARD CAGE AND BACKPLANE ASSEMBLIES

Information on assembling the cards into the card cage is provided in Section X of this document.

2.1 INTRODUCTION

This section describes the overall characteristics of the A700 processor cards. It gives gives a user's description of the processor along with descriptions on the Interrupt System, I/O ARDS System, and the Virtual Control Panel.

2.2 BLOCK DIAGRAM

The lower processor card functions with the upper processor card to form the complete A700 Processor when used with a memory controller and memory array. Figure 2-1 shows a functional block diagram of the A700 Processor indicating which portions are contained on each of the two cards.

The lower processor holds the micromachine which includes the clock generation, the microprogram sequencer (mfg. type AM2911A chips) and control store, the bit-slice ALU chips (mfg. type AM2903), the condition register, and the counter. (These micromachine chips are referred to as the 2911 and 2903 in the remainder of this manual.) The upper processor, lower processor, and memory controller communicate over the frontplane. The frontplane is an extension of the processor's internal Y-bus and B-bus. The frontplane also interconnects the processor with the memory controller.

The lower processor card relies on the upper processor card for the interface to the backplane. The lower processor makes use of the upper processor for additional register files used by the microcode. The lower procesor also accesses the external ALU of the upper processor. (Details of the backplane signals are covered in Section X and the frontplane signals in Section XI.)

The circuitry of the processors cards is composed of Schottky and low-power Schottky integrated circuits of the 7400 series TTL type which support the TTL LSI micromachine components. The ICs are referenced by U-numbers and schematic locations. For example, U69 (13-C) means chip U69 on schematic sheet no. 1 is located by schematic grid locators 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc. and on sheet no. 2 it is numbered 20, 21, etc.

2.3 ABBREVIATIONS AND SIGNALS

The following abbreviations are used in this manual.

FPP Floating Point Processor card

MC Memory Controller card
PCS PROM Control Store card

PL Lower Processor card

PU Upper Processor card

WCS Writable Control Store card

Some general conventions used in signal names are the following:

PU_[signalname]	Indicates that signal is only on PU; this is implied in Section IV on the upper processor for any names that have no other prefix.
PL_[signalname]	Indicates that signal is only on PL; this is implied In Section III on the lower processor for any names that have no other prefix.
FP_[signalname]	Indicates that signal passes over the frontplane.
BP_[signalname]	Indicates that signal passes over the backplane.
LY[register]	Load Y-Bus into register.
E[register]B	Enable register onto the B-Bus.
MIR[n]	MicroInstruction Register bit n.
[microorder]	Decoded microorder.

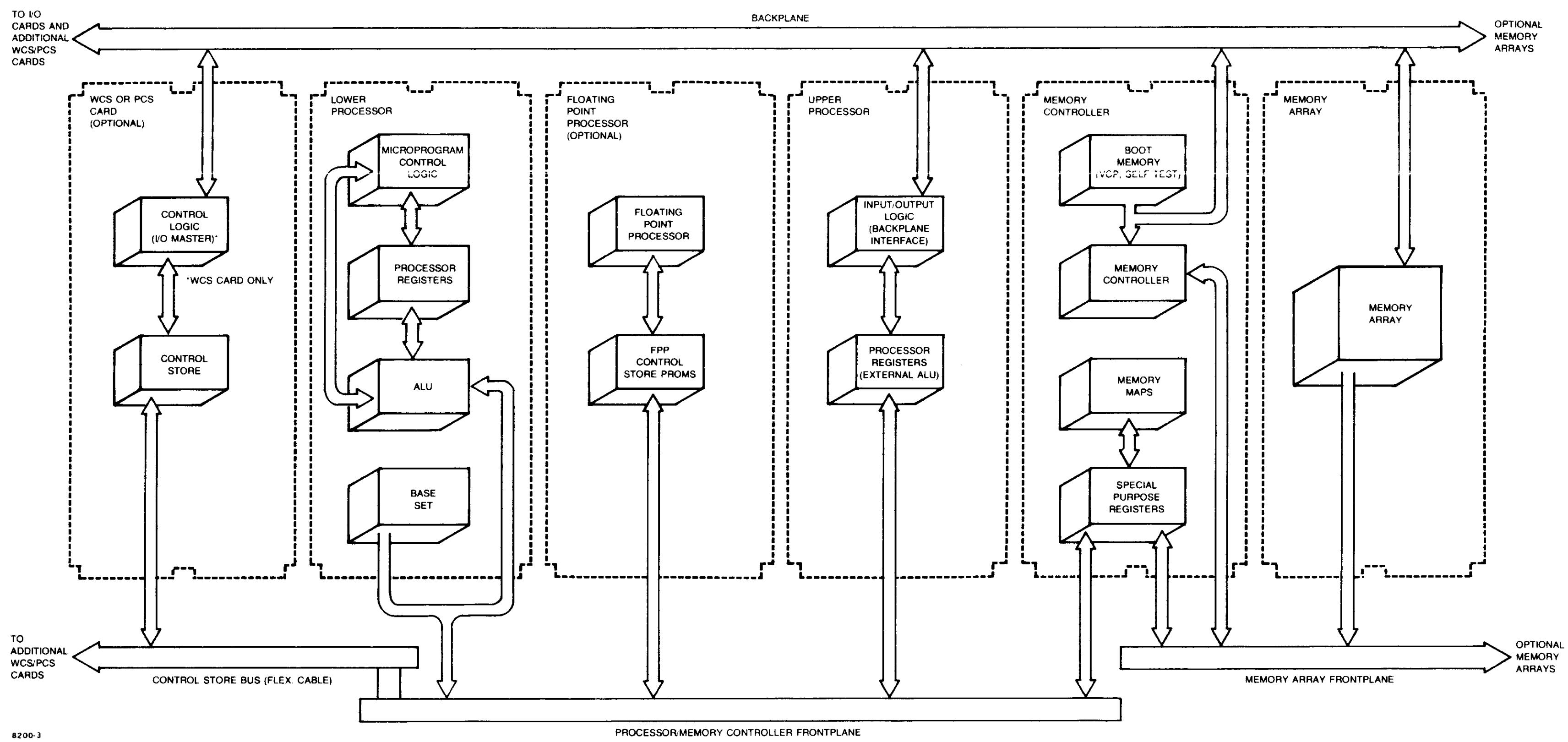


Figure 2-1. A700 Functional Block Diagram

2.4 A700 INTERRUPT OPERATION

2.4.1 GENERAL DESCRIPTION

Interrupt requests can be classed as two types: system level and I/O. The upper processor card receives all interrupt requests and determines which interrupt will be serviced.

Three basic levels of importance define the relative priority of interrupt requests (refer to paragraph 2.4.3.3). A level one interrupt request has no restrictions in obtaining interrupt service. Level two and level three requests are collectively enabled/disabled by an STC/CLC 4, the interrupt inhibit flag. Level three interrupt requests may be further enabled/disabled by an STF/CLF 0, the interrupt system flag. In addition, interrupt masks are available to mask off any or all of the level three interrupt requests. A hardware signal from the processor called Temporarily Disable Interrupt (PU_TDI-) will prevent one of the level two and all level three requests from interrupting following certain instructions and slave mode transfers.

2.4.2 INTERRUPT FLAGS

The interrupt system flag is set/cleared with the STF/CLF 0 instruction, and affects level three interrupt requests. When the flag is set, the Time Base Generator (TBG) and any unmasked I/O interrupt request will receive service. The interrupt system flag allows the programmer to prevent TBG and I/O interrupts from interfering with selected portions of a program. This flag is cleared on power-up and in response to a CLC 0 instruction.

The PU_TDI- signal is utilized to resolve complications that would arise if an interrupt occurred while executing an indirect jump instruction. For the next instruction cycle following a jump, indirect (JMP,I); a jump to subroutine, indirect (JSB,I); an I/O group instruction; or enabling the bootstrap ROMs in slave mode processing; the processor will hold off the power fail interrupt request and all level three requests. Up to three levels of indirect jumps will keep these requests disabled. The power fail interrupt request is included in this group to simplify the power fail, auto-restart routine because it is not necessary to save the status of an incomplete indirect jump sequence. The TDI- signal is asserted at power-up and de-asserted after the first instruction fetch unless that instruction falls into one of the above classifications.

The interrupt inhibit flag can disable all but the three highest priority interrupt requests: parity error, unimplemented instruction, and memory protect. The flag can be set/cleared by STC/CLC 4 in software. This feature can be used to prevent level two and three interrupt requests from delaying the preservation of system status in the event of power-down or from confusing system status restoration during power-up. The interrupt inhibit flag is automatically cleared on power-up. Typically, the flag should be set upon entering a power-up routine during auto-restart or at the start of a power-down routine at power fail. In addition, the interrupt inhibit flag should be set at the beginning of any interrupt service routine and not cleared until the central interrupt register has been recovered. Entry into the power-down routine via a power fail interrupt causes the interrupt inhibit flag to be set.

2.4.3 SYSTEM LEVEL AND I/O INTERRUPT REQUESTS

2.4.3.1 System Level Interrupt Requests

There are five system level interrupt requests. In order of priority, they are:

a. Parity error.

b. Unimplemented instruction.

c. Memory protect.

d. Power fail.

e. Time base generator.

A parity error interrupt request occurs when the memory card signals a parity error during a processor memory access if the parity system had been enabled. The parity system is enabled/disabled by a STC/CLC 5 command in software. The current sense of parity is made even/odd by STF/CLF 5 and the default at power-up is odd parity. Parity error takes precedence over other system level problems because incorrect data reaching the micromachine may be construed erroneously as an unimplemented instruction or a memory protect violation. Therefore, any parity error occurring during a processor access to memory is considered catastrophic and is serviced immediately.

An unimplemented instruction interrupt request is made when the micromachine signals that the last instruction fetched was not recognized by it or by any other system card. This interrupt provides a straightforward entry to software routines for the execution of instruction codes not recognized by the computer hardware. This request must receive immediate service in order to recover the instruction code that caused it. The unimplemented instruction interrupt is never inhibited and concedes priority only to a parity error.

A memory protect interrupt occurs when a user programmed instruction attempts to enter selected pages of memory that are protected, except those involving the A- or B-register. Memory protect also prohibits execution of all I/O instructions except those referencing I/O select code 01 (the processor status register and overflow register). Execution of all HLTs is prohibited. The I/O instruction feature limits control of I/O operations to interrupt control only. Thus, an executive program residing in protected memory can have exclusive control of the I/O system.

The memory protect logic is enabled by an STC 07 instruction. It is disabled automatically by any interrupt. Memory protect can also be enabled with a XJMP instruction.

A power-fail interrupt request is made after the power supply has signalled a power fail warning. This warning indicates that line power has been cut off and that regulated power will soon be lost. The power fail interrupt request may be denied by either the interrupt inhibit flag or a temporary interrupt disable.

A time base generator (TBG) interrupt request is initiated every ten milliseconds to update any real time clocks in software. The TBG signal generated on the upper processor card is accurate to within 2.16 seconds per day. This level three interrupt is maskable and requires the interrupt system to be enabled, that interrupts not be temporarily disabled, and that level two and three interrupts are not inhibited.

2.4.3.2 I/O Interrupt Requests

There can be as many I/O interrupt requests as there are I/O interface cards in the system since each I/O card has interrupt capability. The priority of I/O interrupt requests among the I/O cards is a function of the card's physical placement from the processor; the closest card has the highest priority and cards below it have descending priority independent of the select codes assigned. I/O interrupt requests have lower priority than TBG and both are maskable.

I/O interrupt requests come from the I/O interface cards. Collectively, these requests may be inhibited by the same signals which inhibit TBG interrupt requests. TBG commands higher priority than I/O requests when both request interrupt service. The interrupt mask is used to disable I/O requests by select code groups.

2.4.3.3 Interrupt Priority

The following chart shows pictorially the relative priority and the qualifiers required by each interrupt request. An interrupt service priority line pointing downward encloses the lower priorities it supercedes. The horizontal (***) lines are program instructions and horizontal (---) lines are processor signals.

```
Level 1
   parity error during a micromachine memory access
   unimplemented instruction
   memory protect violation

***************************************interrupt inhibit flag (STC/CLC 4)
*
* Level 2
* ------------------------------Temporarily Disable Interrupt (PU_TDI-)
* ¦  power fail
* ¦
* ¦ ***********************************interrupt system flag (STF/CLF 0)
*   *
* ¦ * Level 3
* ¦ * ---------------------------------------------------interrupt mask
* ¦ * ¦  time base generator
▼ ▼ ▼ ▼  I/O interrupt requests
```

An interrupt is serviced when an interrupt is acknowledged by fetching an instruction from the memory location whose address matches the select code of the interrupt requestor. Service of simultaneous interrupt requests is accomplished on a priority basis. The highest priority system level interrupts are serviced first, before any I/O interrupts, which are serviced according to their location from the processor see Figure 1-2 in Section I for an illustration of slot priority).

An interrupt caused by an I/O interface card begins with an interrupt request. The highest priority I/O request waits until it receives an interrupt acknowledge signal (IAK-) simultaneously with a deasserted ICHOD- on the backplane. ICHOD- is the interrupt chain disable output of the next higher priority interrupting device. The authorized I/O card will put its select code on the address bus as the vector address and begin the memory cycle with a MEMGO-.

2.5 I/O PROCESSING

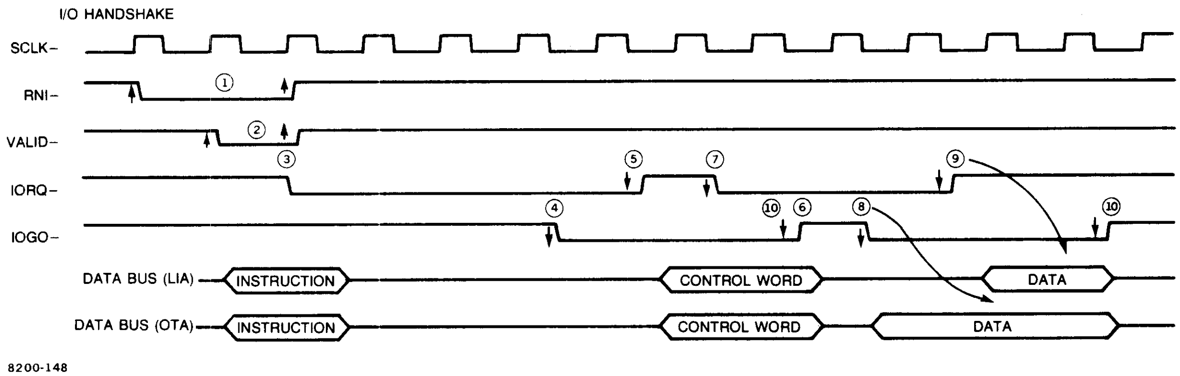
I/O accessing to the appropriate I/O channel is made by select code. Select codes 20 to 77 octal are the valid codes for the interface cards. All lower select codes, 0 through 17 octal, are reserved for system level I/O processing, which includes the enable/disable interrupt system and output to the status register instructions. These low select code I/O instructions are handled by microcode in the base set.

Interaction between I/O processors (CPU vs. I/O master) and the CPU in the HP 1000 A700 Computer is facilitated by I/O handshakes. I/O Handshake timing is shown in Figure 2-2. This effectively places the micromachine into the slave mode so that its internal registers may be read or altered by the I/O executor to accomplish the execution of the instruction. A single handshake is required for the I/O executor to inform the micromachine to increment the program counter if the conditional skip is true. A double handshake is necessary if any data is passed into or out of the micromachine. The first handshake passes a control word to the micromachine to tell it how to process the data transfer which takes place during the second handshake. This allows the A- or-B registers to be loaded from or merged with an I/O buffer, or to be copied into an I/O buffer.

Suppose that an I/O interface card with select code 27 receives an SFS 27 instruction and that its flag had been previously set. That I/O card asserts IORQ- as soon as it has recognized the instruction and determined that the conditional skip is true. The micromachine will eventually respond with an IOGO- assertion to affirm that it has received the I/O handshake request. The I/O card will de-assert IORQ- to signal that the control word will be available on the data bus on the second rising edge of SCLK-. That control word will contain the command to cause the micromachine to increment the program counter again. The program counter is always incremented at the end of an instruction fetch to point to the next instruction; incrementing it once more during a conditional skip will effectively cause execution to pass over the next instruction.

If an LIA 27 instruction has appeared on the backplane, the affected I/O interface card will assert IORQ- and wait for IOGO- also. Upon releasing IORQ-, it informs the micromachine that the next I/O handshake will require information on the data bus to be loaded into the A-register. IORQ- is asserted again one state after its previous de-assertion to begin the second half of the double handshake. After the re-assertion of IOGO- to the second IORQ-, the interface card puts the data word on the backplane data bus. The micromachine loads the A-register with this data on the second rising edge of SCLK- after the de-assertion of the second IORQ-. Operation of the LIB, MIA/B, or OTA/B instructions is similar, except for the direction or destination of the data flow.

Like processor accesses to memory, the completion of an I/O handshake is subject to DMA action on the backplane. DMA is automatically suspended for an instruction fetch but may be resumed thereafter by I/O cards unaffected by the instruction. The affected I/O card will issue an IORQ- but the processor will be unable to respond with an IOGO- until all pending DMA is completed. At that time, the assertion of IOGO- will suspend DMA until the end of the current I/O access.



NOTES:

1. Processor asserts RNI- to inform all system cards that an instruction is being fetched from memory.
2. Memory asserts VALID- to inform all system cards that data on backplane will soon be valid. Each interface should now latch the instruction OFF the data bus, and decode it to see if it is an I/O instruction to its select code.
3. An interface card pulls on IORQ- to signal that it recognized the I/O instruction and needs the CPU in order to execute it.
4. The processor asserts IOGO- to indicate that it is ready to receive a command from the interface card.
5. The interface card releases IORQ- to signal the processor that the control word will be available on the data bus on the second rising edge of SCLK-.
6. The processor releases IOGO- when it has clocked the command off the backplane.
7. The interface card asserts IORQ- if another handshake is needed in order to transfer a data word.
8. The processor reasserts IOGO- in order to indicate that it is ready to receive an operand in the case of an input operation, or that data will be valid on next falling edge in the case of an output operation.
9. The interface card releases IORQ- to indicate that it has latched the operand off the backplane in the case of an output operation, or that an operand will be valid on the backplane on the second rising edge in the case of an input operation.
10. The processor releases IOGO- to indicate that it has clocked data off the backplane in the case of an input operation, or that the handshake is complete in the case of an output operation.

Figure 2-2. I/O Handshake Timing Diagram

2.6 VIRTUAL CONTROL PANEL (SLAVE MODE) PROCESSING

When the processor is in slave mode, its internal registers are accessible to external devices through certain I/O interface cards. The Asynchronous Interface card, the HDLC (DS network) Interface card , and the Parallel Interface card (PIC) are the interface cards which may request slave mode processing. In order to use the PIC as VCP, the user must supply code since HP VCP code does not support the PIC interface.

Because slave mode processing involves direct interaction between the requesting device and the processor, the processor card merely provides buffering, signal timing, and bus arbitration for the handshake signals and data transfers.

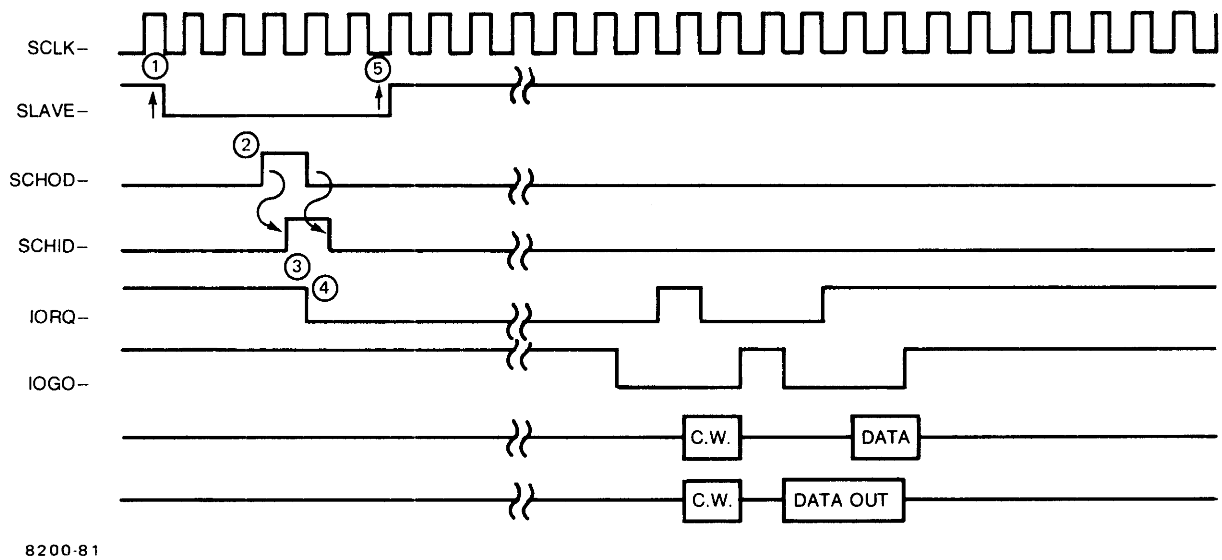
Slave mode processing abides by the same protocols used for the execution of I/O instructions that require interaction between the I/O processors and the central processor. Whereas an instruction causes an I/O processor to initiate an I/O handshake, slave mode processing is performed in response to some external event not related to the program flow. The I/O handshake of an I/O instruction occurs during the execution of that instruction but the I/O handshake of slave mode processing occurs between instructions. Thus, slave mode uses IORQ- and IOGO-, but operates independently of the program.

A slave mode request, BP_SLAVE-, is made over the backplane by the interface card configured for slave mode processing. Only one I/O interface card can be selected as the slave mode interface at any given time. As soon as the current instruction has been completed, the processor will acknowledge the slave request and SCHOD- (slave chain output disable) will be deasserted to inform the slave requesting interface card to start the I/O handshake.

Any device with input/output capabilities and connected to an interface card configured to allow slave mode processing becomes the virtual control panel (VCP). This device will provide the means to access the processor registers and memory locations in a manner similar to a hardware front panel. If a terminal is the VCP device, the keyboard replaces the front panel switches for register selection and data entry, while the display replaces the hardware status and data output indicators. Unlike a hardware front panel, the VCP may be located away from the computer at a remote location.

Operator interaction using a terminal is accomplished by a program located in VCP ROMs on the memory controller card. The code for this program is listed in Appendix A of this document.

See Figure 2-3 for a timing diagram of the backplane protocol for slave mode processing.



NOTES: Same handshake protocols as an I/O handshake. Some slave mode transfers require only one set of IORQ–/IOGO– handshakes.

1. An interface card asserts SLAVE- to request the processor to enter slave mode.

2. When the processor has completed executing the current instruction, it acknowledges the assertion of SLAVE- by de-asserting SCHOD- for one cycle.

3. Worse case, the SCHID/SCHOD priority chain has propogated down to the lowest priority interface card by the end of that cycle, so that the last SCHID- will go high for one cycle.

4. The interface card received the enabling signal when its SCHID- signal went high and can now pull on IORQ- in order to initiate the I/O handshake. The rest of the I/O handshake can then procede exactly as shown in Figure 2-2.

5. The interface card de-asserts SLAVE- once it has asserted IORQ-.

Figure 2-3 . Slave Transfer Protocols

3.1 INTRODUCTION

This section describes the internal characteristics of the A700 Computer lower processor card. The 92045A Microprogramming Manual, part no. 92045-90001, gives a user's description of the processor along with a complete microcode description. The lower processor card is described here in terms of how it implements the microorders; therefore, a good understanding of the microcode is a prerequisite for reading this material. The lower processor card is shown in Figure 3-1.

The lower processor card functions with the upper processor card to form the complete A700 Processor when used with a memory controller and memory array. (Refer to Section II for an overall description.)

The lower processor holds the micromachine which includes the clock generation, the microprogram sequencer (mfg. type AM2911A chips) and control store, the bit-slice ALU chips (mfg. type AM2903), the condition register, and the counter. The lower processor relies on the upper processor card for most of the interface to the memory controller and backplane. It also accesses the upper processor for additional registers used by the microcode,and an external ALU.

3.2 ABBREVIATIONS AND SIGNALS

The following abbreviations are used in Sections 2 and 3 of this manual.

FPP Floating Point Processor card
MC Memory Controller card
PCS PROM Control Store card
PL Lower Processor card
PU Upper Processor card
WCS Writable Control Store card

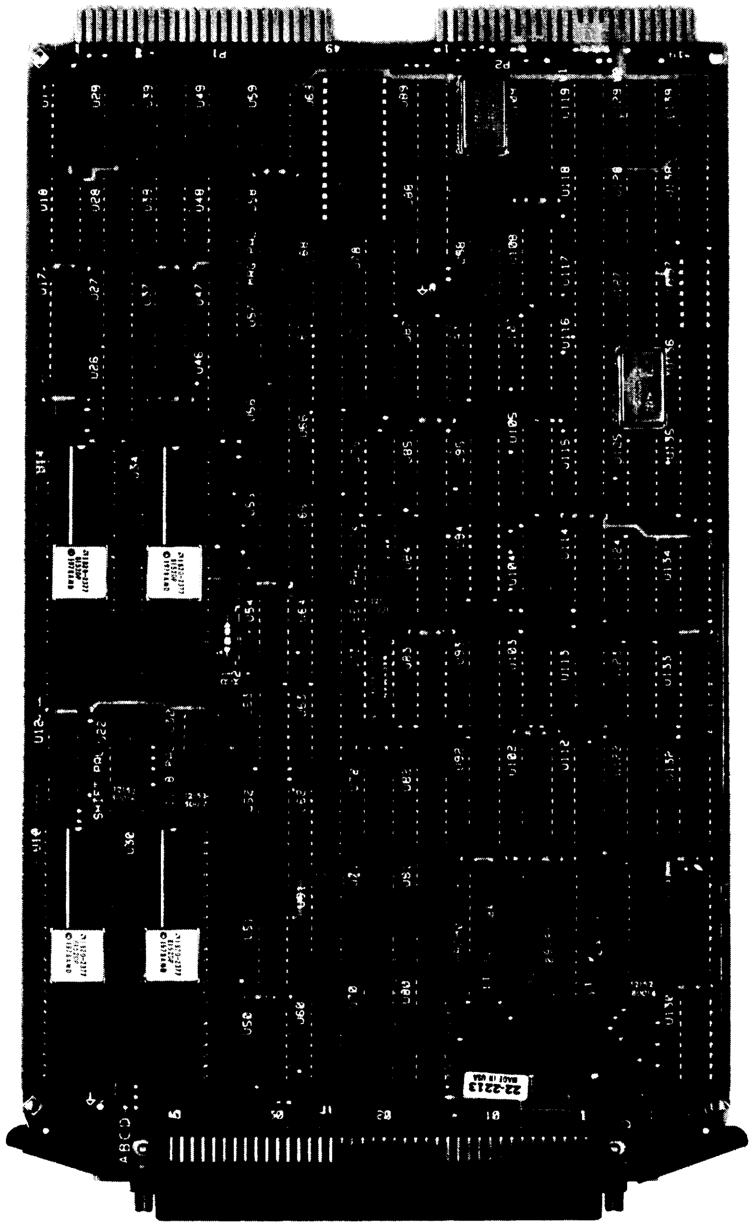


Figure 3-1. Lower Processor Card (12152-60002)

Following are some general conventions used in signal names:

PL_[netname]	: Indicates that net is only on PL; this is implied on any netnames that have no other prefix
FP_[netname]	: Indicates that net passes over the frontplane
BP_[netname]	: Indicates that net passes over the backplane
LY[register]	: Load Y-bus into register
E[register]B	: Enable register to B-bus
MIR[n]	: MicroInstruction Register bit n
[microorder]	: Decoded microorder
[signal name]'	: Signal negated

ICs are referenced by U-numbers and schematic locations. For example: (U69, 13-C) means chip U69 on schematic sheet no. 1 is located by schematic grid locators 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc. and on sheet no. 2 it is numbered 20, 21, etc.

3.3 BLOCK DIAGRAM DESCRIPTION

3.3.1 GENERAL ORGANIZATION

A Micromachine Block Diagram of the A700 processor which is mainly contained on the lower processor card is shown in Figure 3-2. The lower card circuitry can be divided into six functional blocks which are shown in Figure 3-3. These blocks are the following:

- Clock Generation Circuit
- Microinstruction Register and Decoder
- Sequencer and Control Store
- Arithmetic Unit and Control Logic
- Condition Register
- Counter

The functional blocks are described first in a general manner and their logical operations (theory of operation) are then described in the paragraphs under 3.4.

The major controlling element of the lower processor card (hereafter referred to as PL) is the microinstruction. The PL function is to determine the Word Type and then implement the microorders. Refer to Table 3-1 for a summary of microinstruction word-type binary formats (a summary of microorders is provided in Table 3-3).

The 32 bits of microinstruction are latched in the microinstruction register (MIR) each cycle. The information in the MIR is used to control the rest of the processor during the cycle. Many of the fields are directly decoded to generate signals corresponding to the microorders (for example, the SPECIAL, B and STOR-Fields).

Table 3-1. Microinstruction Word-Type Binary Format Summary

<table>
<tr><th>BIT</th><th>31</th><th>30</th><th>29</th><th>28</th><th>27</th><th>26</th><th>25</th><th>24</th><th>23</th><th>22</th><th>21</th><th>20</th><th>19</th><th>18</th><th>17</th><th>16</th><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th></tr>
<tr><td>WORD TYPE 1</td><td colspan="5">OP1</td><td colspan="4">ABUS</td><td colspan="5">SP0</td><td colspan="4">SP2</td><td colspan="4">ALU</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 2</td><td colspan="5">OP2</td><td colspan="4">ABUS</td><td colspan="5">SP0</td><td colspan="4">CNDX</td><td colspan="4">ALU</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 3</td><td colspan="4">OP3</td><td colspan="7">ADRS</td><td colspan="3">SP1</td><td colspan="4">CNDX</td><td colspan="4">ALU</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 4</td><td colspan="4">OP4</td><td colspan="7">ADRS</td><td colspan="3">SP1</td><td colspan="4">SP2</td><td colspan="4">ALU</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 5</td><td colspan="4">OP5</td><td colspan="14">ADRL (LONG BRANCH ADDRESS)</td><td colspan="4">ALU</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 6</td><td colspan="2">OP6</td><td colspan="16">DAT (IMMEDIATE DATA)</td><td colspan="4">ALU</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 1S</td><td colspan="5">OP1</td><td colspan="4">ABUS</td><td colspan="5">ALUS*</td><td colspan="4">SP2</td><td colspan="4">SPEC</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 2S</td><td colspan="5">OP2</td><td colspan="4">ABUS</td><td colspan="5">ALUS*</td><td colspan="4">CNDX</td><td colspan="4">SPEC</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 3S</td><td colspan="4">OP3</td><td colspan="7">ADRS</td><td colspan="3">ALUS*</td><td colspan="4">CNDX</td><td colspan="4">SPEC</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 4S</td><td colspan="4">OP4</td><td colspan="7">ADRS</td><td colspan="3">ALUS*</td><td colspan="4">SP2</td><td colspan="4">SPEC</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
<tr><td>WORD TYPE 5S</td><td colspan="4">OP5</td><td colspan="14">ADRL (LONG JUMP TABLE ADDRESS)</td><td colspan="4">SPEC</td><td colspan="5">BBUS</td><td colspan="5">STOR</td></tr>
</table>

*Special microorder in ALUS field when ALU field is coded SPEC.

8200-4

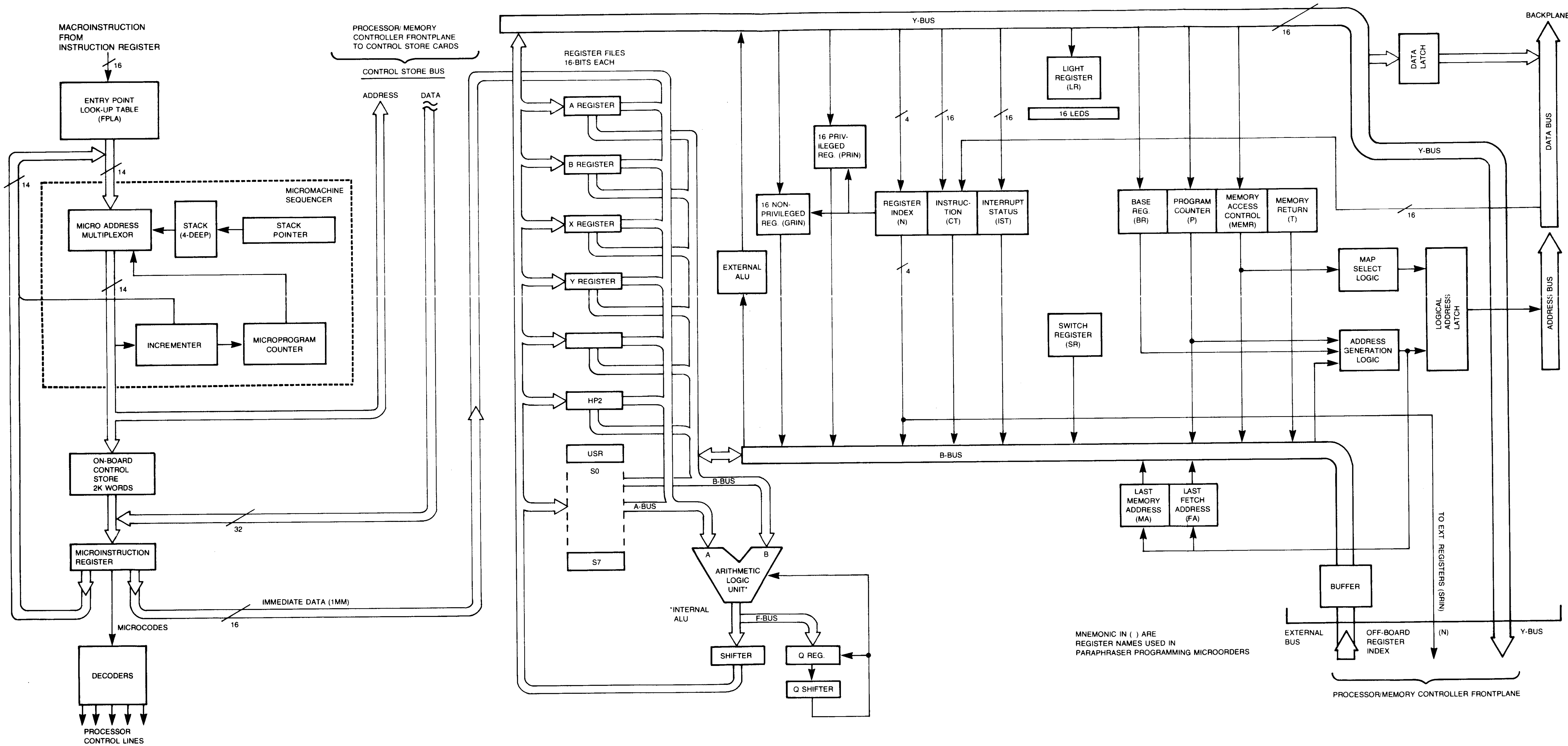


Figure 3-2. A700 Micromachine Block Diagram

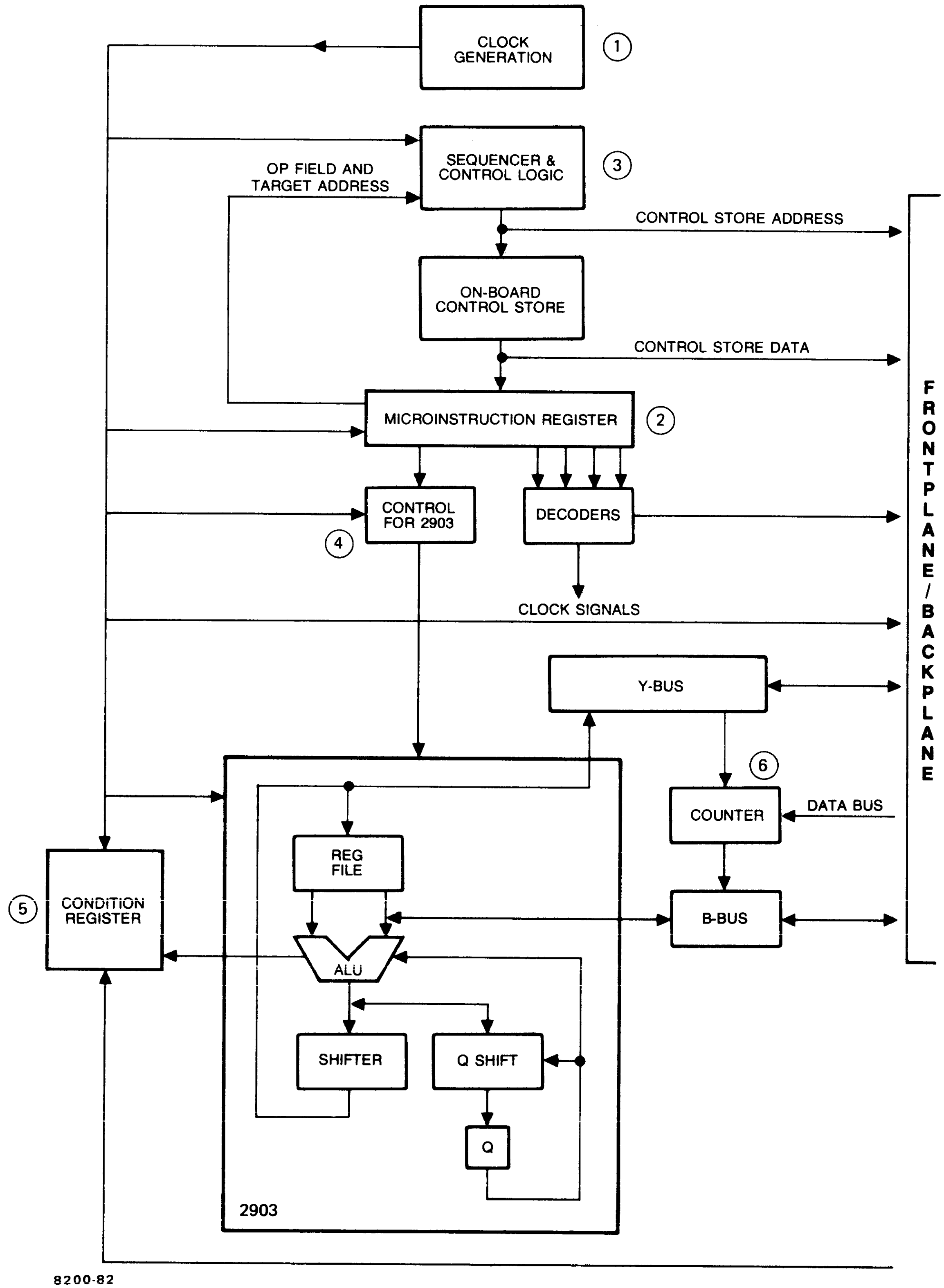


Figure 3-3. Six Functional Blocks of the Lower Processor

The OP and TARGET fields of the MIR are used by the sequencer and control logic block to generate the next Control Store Address (CSA). A lookup table (refer to JTAB microorder) translates a macroinstruction in the counter into a CSA. The CSA is used to address the 2k-words of on-card control store and is received by any WCS, PCS, or FPP cards over the frontplane. The data received from either on- or off-card control store is latched into the MIR at the end of the microcycle.

The usage of the 2903 Bit-Slice Processor does not provide a direct relation between the control inputs of the 2903s and the A700 microorders. Thus, a block of hardware is neccessary to translate these microorders and other processor information into the 2903 control signals. Some of the control signals generated by this block are: ten instruction bits, register file source and destination addresses, carry-in, shift linkage bits and output enables. Some of the MIR information is used directly by the 2903s.

Status information, generated in the ALU and other places on the processor card, is saved in the condition register. The condition register serves two purposes: 1) It saves status information to be used during the next cycle for conditional microorders and 2) It holds status information which may be used during the next or subsequent cycles for other purposes (for example, the double-word bit).

The operation of the counter, which also serves as a macroinstruction register, is controlled mainly by decoded signals from the MIR. The counter is loaded from the Y-bus and also from the backplane data bus during macroinstruction fetches. The counter also serves as a lookup table for the sequencer control logic.

3.3.2 CLOCK GENERATION

The clock generation block diagram and signals are shown in Figure 3-4. The clock generation logic generates the system clocks which are driven onto the backplane. It then receives and qualifies these signals to generate the clocks used on both processor cards. PL generates and drives CCLK- (communications clock), FCLK- (fast clock), and SCLK- (system clock). FCLK- and SCLK- are used to generate the clocks used by both processor cards.

The processor cards use three main internal clocks. SC is a card version of the backplane SCLK (system clock). It has a cycle of 250 nanoseconds and a duty cycle of 40 percent. Processor clock (PC) is equivalent to SC except that it may be frozen under certain conditions. A freeze will be seen only by the processor cards and will not affect the backplane SCLK or any other cards. A freeze will cause the short half-cycle of PC to be stretched for an integral number of cycles until the freezing condition goes away.

A freeze is generated from the PU if a microorder cannot be executed or if certain required interface logic is busy. LC (Latch Clock) is generated from the PC but will be asserted typically for only 75 nanoscends (one and one half FCLK cycles) at the end of the cycle. Since LC is generated from the PC, LC will not be asserted if a freeze condition exists.

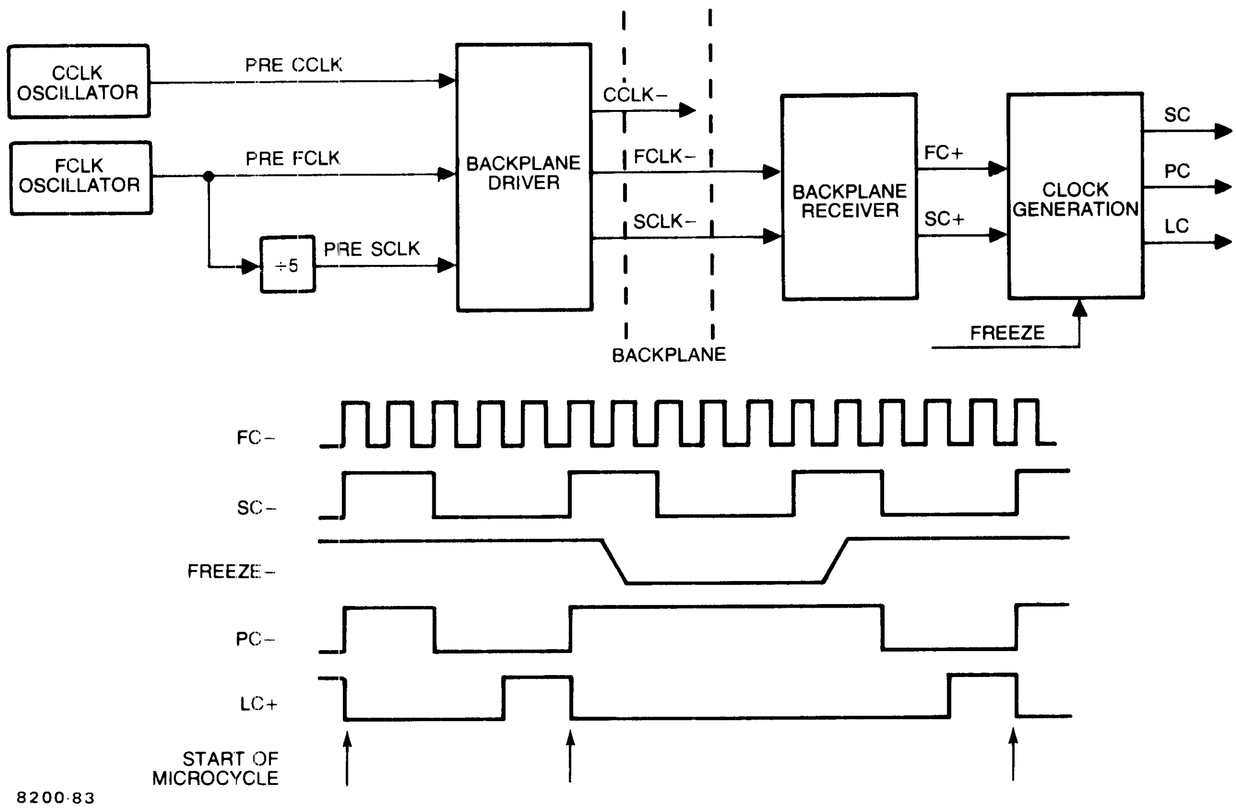


Figure 3-4. Clock Generation Block Diagram and Clock Signals

3.3.3 MICROINSTRUCTION REGISTER AND DECODERS

The MIR latches the microinstruction at the beginning of the microcycle and drives the 32 bits of information during the cycle. (The block diagram for the MIR and decoders is shown in Figure 3-5.) Thus, most of the control of PL comes directly from the MIR. The following table shows the physical format of the MIR:

FIELD	LSB ---> MSB
OP	MIR27 - MIR31
ADDRESS (lower 6 bits)	MIR22 - MIR27
BLOCK ADDRESS (upper 8 bits)	MIR14 - MIR21
CNDX	MIR14 - MIR17
SP2	MIR14 - MIR17
SPO	MIR18 - MIR22
SP1	MIR18 - MIR21
IMMEDIATE	MIR14 - MIR29
A BUS	MIR23 - MIR26
ALU	MIR10 - MIR13
B BUS	MIR5 - MIR9
STOR	MIRO - MIR4

The Word Type and OP Decode block serves mainly to identify sets of word types used by other MIR decoders. For example, this block of combinational logic will identify: Word Type 5 or 6 (WT56), or Word Type 2 or 3 (WT23) or OPs SPOT or SPOF, or the JTAB OP.

The condition encoder multiplexer (MUX) receives a total of 16 signals either from the condition register or from the upper processor card. These signals correspond to the conditions available in the CNDX-Field. The condition MUX looks at the 16 condition signals and the four bits of the CNDX-Field to produce CNDSPEC- which is the (negative) sense of the condition specified. In the OP-Field, MIR bit 28 differentiates between the OP microorders conditional on the true or false sense. MIR bit 28 is combined with CNDSPEC- to generate the TEST+ signal to indicate that the condition sense specified in the OP field has been met.

The SP2-Field is decoded in a straightforward manner, generating a signal corresponding to each special microorder. OP-Field information is used to determine if the SP2-Field is present for the currently executing Word Type and to enable the decoders as needed.

The SP0/SP1-Field of the MIR is used by other blocks of the processor, both before and after decoding. The SP1-Field is actually the lower half of the SP0-Field; i.e, in terms of coding (refer to Table 3-3). The upper two bits of this field are qualified by the Word Type and other information for two purposes: 1) If the Word Type contains an SP1, the upper bit is zeroed so that it can be treated as the SP0 field; and 2) If the Word Type does not allow an SP0 or SP1, the SP0/SP1 decoders will be disabled. The SP0 decoders use these qualified signals and the MIR bus to generate a signal corresponding to most of the special microorders in the SP0/SP1-Field. The decoders may be disabled if the OP is a conditional special operation (SPOC) and the condition sense is not met (TEST+). The lower three bits of the SP0/SP1-Field are driven (after buffering) to the upper processor card for external ALU execution.

The B-field (not including R0 through R15) is decoded in a straightforward manner directly from the MIR, generating a signal corresponding to each B-field microorder. These signals are then used to enable the contents of the appropriate register onto the B-bus.

The STOR-Field (not including R0 through R15) is also decoded in a straightforward manner directly from the MIR, generating a signal corresponding to each STOR microorder. These signals are used to indicate at what destination to store the Y-bus at the end of the cycle. A STOR-Field enable signal (STEN), generated from the SP0 decoders, will detect a conditional special operation (SPOT or SPOF) with STOR in the SP0-Field and will disable the STOR decoders if the condition is not met.

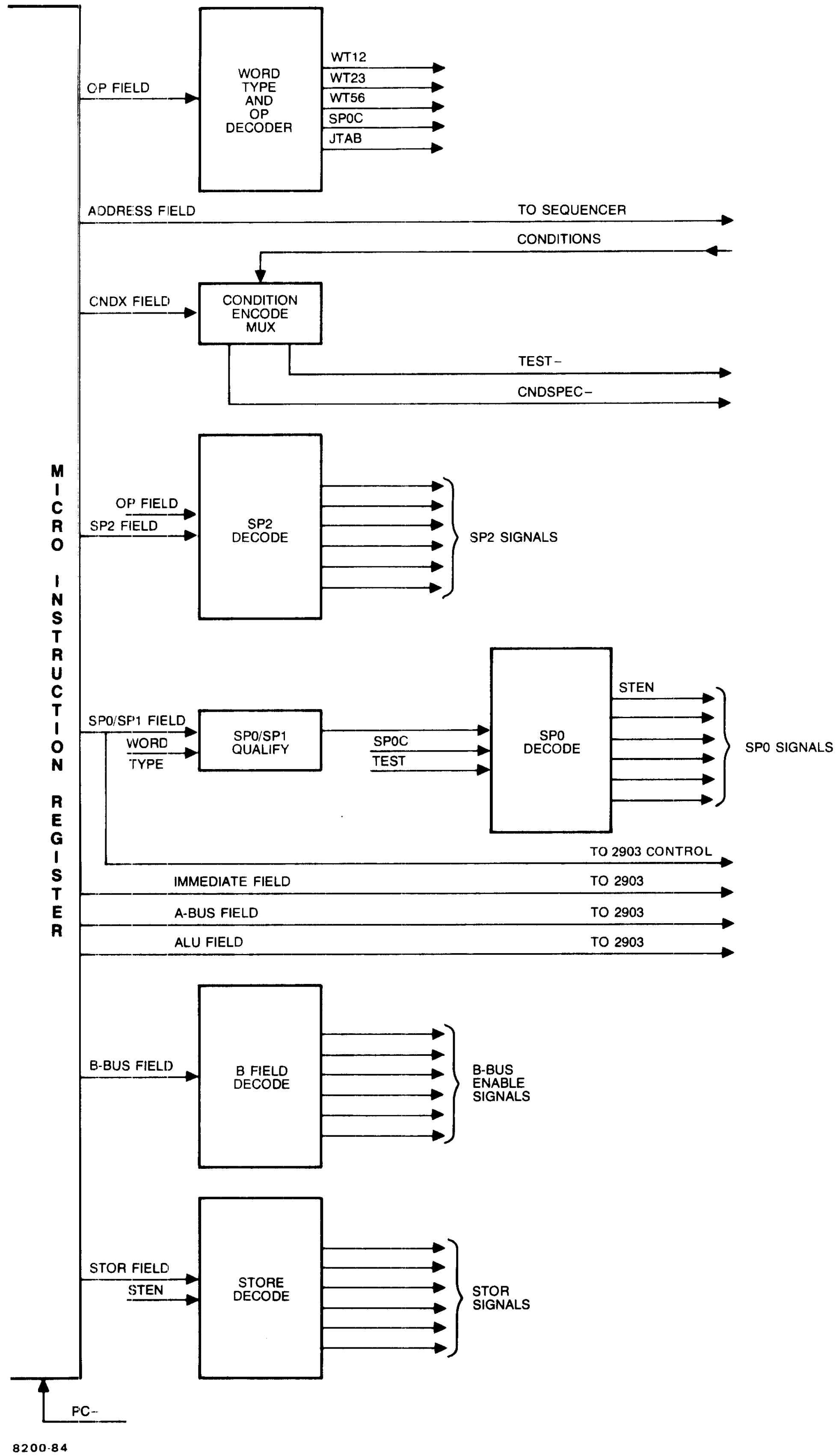


Figure 3-5. Block Diagram of MIR and Decoders

3.3.4 SEQUENCER AND CONTROL STORE

Many of the sequencer functions occur internal to the 2911 bit slice sequencer. The sequencer and control-store block diagram is shown in Figure 3-6. The 2911 allows a control store address to be selected from one of three sources: direct address inputs to the sequencer, the top address on the microprogram stack, or the contents of the microprogram counter. Every cycle, the control store address is incremented; (the carry-in is tied to "1") and stored in the microprogram counter. On a jump to subroutine, the stack pointer is incremented and then the microprogram counter is pushed onto a (4 deep) stack. On a return from subroutine, the top of the stack is selected by the 2911 multiplexer and the stack pointer is decremented.

Four bits determine the selection of the MUX and the control of the stack. These bits are provided by the sequencer control Programmable Array Logic chip (a Programmable Logic Array) which generates them directly from the OP-Field and TEST+ (from the Condition Encoder). TEST+ indicates whether the condition, specified in the CNDX-Field, and the condition sense, specified in the OP-Field, have been met. Certain processor conditions may force the CSA to zero: power on, addressing non-existent micromemory, or microcode timeout.

The direct address bus (DAB), which is the direct input to the 2911s, is generated from a number of sources external to the 2911. The lookup table uses the counter data to generate a direct vector address which is selected when the JTAB microorder is executed. When the SP2-Field contains CT30 or CT74, counter bits 3-0 or 7-4, respectively, will be selected for the lower four bits of the DAB. Counter bits 3-0 are also selected if a Word Type 5 (JMPL or JSBL) has SPEC in the ALU-field. For any other jump or jump to subroutine microorders, the TARGET field of the MIR will be enabled onto the DAB.

The CSA from the output of the sequencers is driven directly to the frontplane. The CSA bus is buffered and driven to the on card control-store PROMs. On card control-store will be enabled only if the CSA is in the lower 2k address space (or the address space configured by jumpers).

Any other control-store card may disable the processor control-store by pulling on a control-store priority chain line. The processor receives two control-store input disable signals: FP_CSIDWC- coming from the bottom of the WCS/PCS priority chain, and FP_CSIDFP- coming from the optional floating point card.

If the control-store address is greater than the on-card address space and no control-store card responds by pulling the priority line, then the control store data (CSD) bus will be driven by the unimplemented microinstruction (UMI) buffer. The microinstruction driven by the UMI buffer is effectively a NOP, i.e., it assures that no system status register or other important information will be overwritten. The FP_UMI- signal will force the sequencer address to zero during the next cycle.

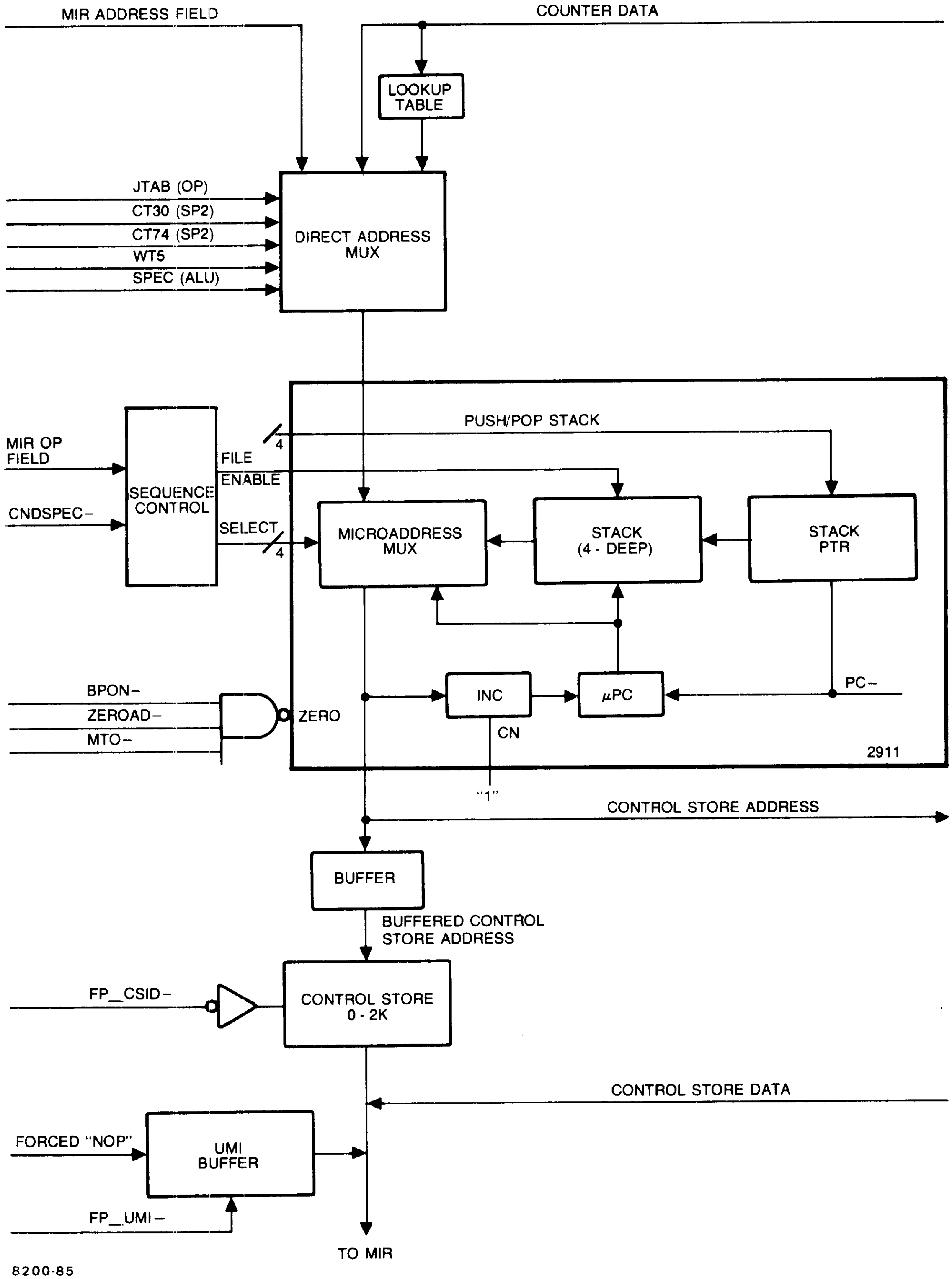


Figure 3-6. Sequencer and Control-Store Block Diagram

3.3.5 2903 AND 2903 CONTROL LOGIC

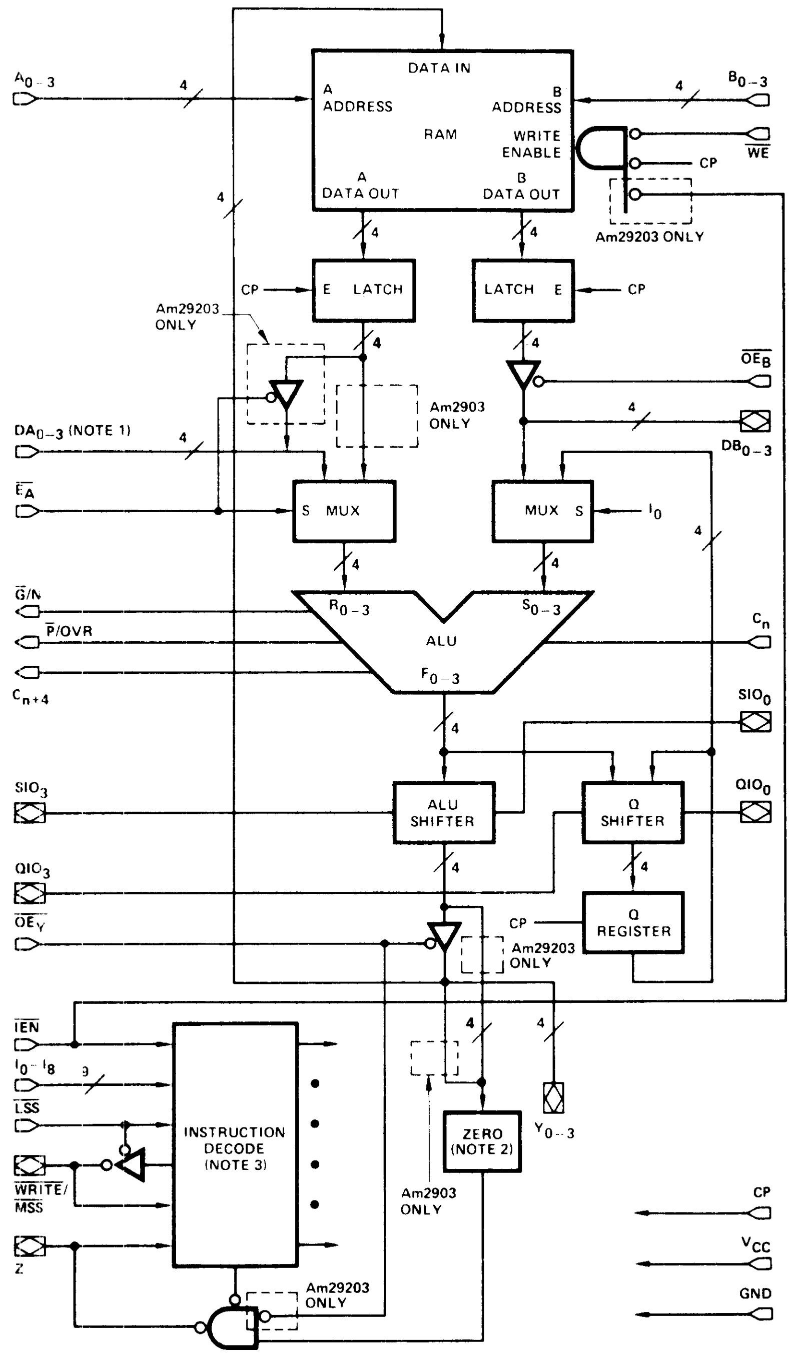
The heart of the A700 processor is four 2903 4-bit slice processors. A block diagram of the 2903 processor is shown in Figure 3-7, and the control logic of the 2903 processor is shown in Figure 3-8. Each 2903 contains a 16-word register file, an ALU with a post shifter and an additional separate register, Q, with a preshifter. For a functional description of the 2903, the reader should refer to the AM2900 Family Data Book (1979), American MicroDevices Inc, Sunnyvale, Calif.

There is not always a direct relation between the microorders and the 2903 control signals. The 2903 inputs for DA, EA- and I1-I4 are received directly from the MIR bits in the IMM Field, OP-Field, and ALU-field respectively. The other 2903 control inputs require a moderate degree of qualification and decoding. Not all the functions provided by the 2903 are used.

The A-address comes from the MIR A-field, but certain bits of the address may be forced to a zero or one depending on other conditions. If the OP-Field does not contain a Word Type 1 or 2, the A address will always be forced to address "4" to access the accumulator (R04). If the OP-Field contains JTAB and counter bit 11 is zero, then the lower bit of the A address will be forced to zero. (The JTAB line should always have B in the A-field). This will serve the function of conditionally (on bit 11 of the instruction) enabling the A or B macroregisters onto the A-Bus for MRG execution.

The B-field and STOR-Field, along with some corresponding control signals (for A/B memory addressing), are multiplexed such that the B-field (source) is selected for the first half cycle and the STOR-Field (destination) is selected for the second half cycle. Combinational logic, which functions as a multiplexer, selects either this result (BA), the A register, the B register, the X register, or the Y register. The selection is based on the contents of the B- or STOR-Fields (for example CAB, CXY), Counter bits 11 and 3, and the control signals which indicate a main memory read or write accessing A or B. The 2903 B-bus will be enabled by the signal OEB if the B-field contains: R0-R15, CAB, CXY, or if the B-field contains T and the last memory read was from A or B (FP_LRAB).

In addition to providing the correct B address, the Write Enable signal (WE-) must be asserted in order to write to the 2903 internal register file. A write will occur if the STOR-Field contains: R0-R15, CAB, CXY, or a main memory write and the memory address is either A or B (FP_ABWR-). The write is further qualified by STEN, so that it is disabled if the OP is SPOT or SPOF and the condition is not met. It is also qualified by the clock signal, LC+, so that WE- is only asserted for about one-third of the cycle near the end of the cycle.



NOTES:
1. $DA_{0\text{-}3}$ is input only on Am2903, but is I/O port on Am29203.
2. On Am2903, zero logic is connected to Y, after the OE_Y buffer.
3. On Am2903 IEN controls WRITE.On Am29203 WRITE is not affected by IEN.

Figure 3-7. Am2903 Processor Block Diagram
(Source: AMD 2900 Family Data Book, AM-PUB003)

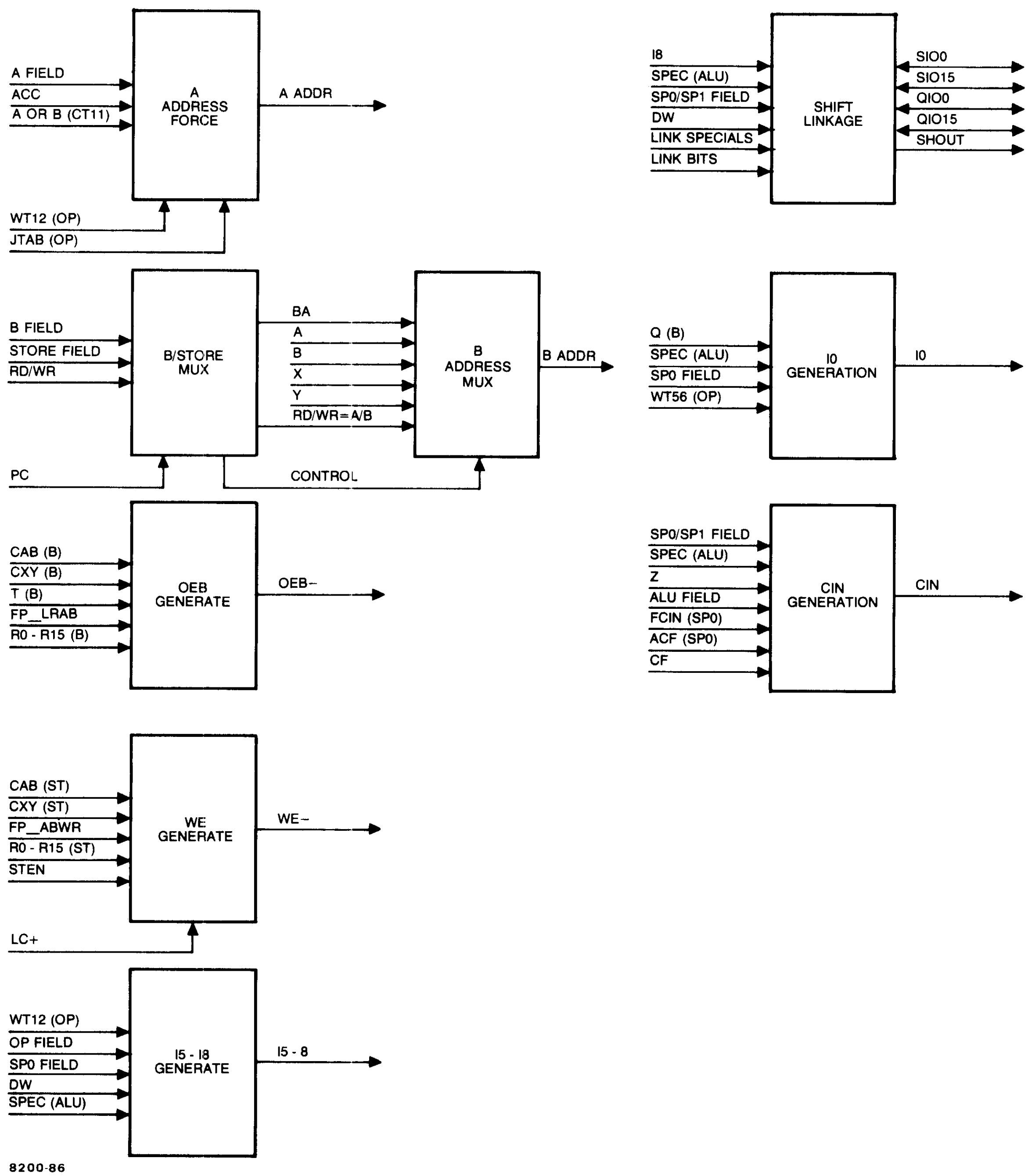


Figure 3-8. Am2903 Control Logic Block Diagram

Control signals I5 through I8 provide 2903 destination control (ALU post shifter, Q, and Q pre-shifter) and define the special ALU functions. The microorders controlling these functions are in the SP0/SP1-Field. Thus, the I5-8 generation block requires these inputs: the SP0-Field, the OP-Field (for SP0 qualification), SPEC (indicating SPEC in the ALU-field) and the double-word bit (DW). The outputs generated go directly to the 2903 I5-I8 control lines. A shift enable signal (SHEN), which indicates to other blocks of logic that a shift function is being executed in the current cycle, is generated from I5-8.

Instruction bit I0 serves two purposes. It is used when Q is in the B-field to select Q as an ALU operand (refer to Table 1: ALU Operand Sources in the AM2900 Family Data Book under the 2903 description). If SPEC (all zeros) is in the ALU Field and there will be no 2903 ALU operation (for example, External Special ALU operation), then I0 is forced high causing the ALU output to be all ones. This insures that the Carry Flag (CF) and ALU Overflow (ALOV) will both be cleared at the end of the cycle, and that the Z output of the 2903s represents the Y-bus being all zeros.

The shift linkage logic provides the link between the shift inputs and outputs of the least significant and the most significant slices of the 2903 (QIO0, QIO15, SIO0, SIO15). These bits are bidirectional on both the 2903s and the Shift Linkage Logic. I8 determines the direction of the shift ("1" for left, "0" for right) and enables the driving of the appropriate pair.

In operation, the shift linkage looks at a variety of information, including the 2903 shift outputs, to determine what to drive onto the shift inputs. SPEC is used to differentiate between standard and special shift functions. The MIR bus (SP0/SP1-Field) determines what type of shift or which special ALU function is to be executed. Shift link specials, shift link bits (E or F) and the double-word bit (DW) are also used. The shift linkage logic also determines the bit shifted out (SHOUT) which is loaded into the shift flag (SF) and may be loaded into E or F.

The 2903 provides look-ahead carry-generation signals, G (generate) and P (propagate). These signals are used by the 74S182 lookahead carry generator to provide carry inputs to the upper three slices of the 2903s. The least significant carry input to the 2903 is generated from a number of different signals. In the absence of any forcing specials, the carry in (borrow-) must be zero for add operations and one for subtract operations. Thus the CIN logic looks at the ALU-field directly and also the FCIN (force carry-in) special to determine the sense of the carry-in. The ACF (ALU with carry flag) special signal, when asserted, will determine the sense of CIN with the Carry Flag (CF). In the event of an ALU special, CIN is determined from the contents of the SP0 or SP1 field. In this case CIN may be either "0", "1", or Z (2903 Z output).

The 2903s may be enabled or disabled from driving the Y-bus with the output enable signal, OEY-. The 2903 Y-bus is disabled only when an external ALU Special is executed (distinguished by bit 3 of the SP0- or SP1-Field). Then the 2903s will receive the Y-bus for storing into the register file, and Z will be generated from the Y-bus which is driven from the external source.

3.3.6 CONDITION REGISTER

The condition register block diagram is shown in Figure 3-9. The condition register provides 14 of the 16 processor conditions which are testable in the CNDX-Field. Some of these conditions are used elsewhere in the processor. The other two processor conditions are supplied by the upper processor card. Of the 14 conditions, eight are received directly from other parts of the processor or the backplane and are only latched by the register. The signals for conditions Y15 and B15 are taken directly from the Y- and buses, respectively. The signals for YZ, ALOV and CF are obtained directly from the 2903 Z, OVR, and COUT outputs, respectivly. CTZ and CTZ4 are latched from counter signals PCTZ and PCTZ4. MP is latched directly from the backplane.

The backplane PON (power on) signal is received from the backplane and clocked twice to obtain BPON, the card power on signal. BPON is clocked once more to obtain the CNDX-Field power on (CPON). The backplane IORQ (I/O request) is latched from the backplane in the middle of the microcycle and then latched again at the end of the microcycle (CIORQ) to synchronize it.

To generate the O condition, which is also the macro-overflow (O) register, the condition register must look at STO and CLO and ENOE from the SPO-Field and the 2903 OVR output. The E condition, which is the macro-extend register, may be generated from CLE and STE in the SPO/SP1-Fields and also from ENOE in the SPO-Field and the 2903 COUT output. In the case of a shift function, E may be generated from LWE in the SP2-Field, SHOUT (the bit shifted out) and SHEN (shift enable). The F condition or general-purpose flag generated from STF and CLF in the SP2-Field and JTAB in the OP-Field. For a shift function, F may be generated from LWF in the SP2-Field, SHOUT (the bit shifted out) and SHEN (shift enable). The condition SF or shift flag is generated from SHOUT (the bit shifted out) and SHEN (shift enable).

The condition register contains two signals relating to processor status which are not in the CNDX-Field. The double-word bit (DW) is used to indicate that shift functions will perform double word shifts. DW is generated from CMDW in the SP2-Field and JTAB in the OP-Field. The Unimplemented MicroInstruction signal (FP_UMI) is latched in the condition register to become ZEROAD, which forces the microaddress to zero.

3.3.7 COUNTER

The counter is a relatively simple block of logic which is shown in Figure 3-10. The counter's main component is a 16-bit counter. The counter primarily functions as an instruction register in that it selects instructions on the backplane to pass on to the B-bus. In operation the counter MUX passes either the Y-bus or the backplane data bus to the counter data inputs. This MUX is selected by the signal FP_TCNT- driven by PU. When asserted, FP_TCNT- indicates that, during the current cycle, the data available on the backplane is an instruction, and the data bus will be selected. The counter contents are enabled to the B-bus when the microorder CT appears in the B-Field.

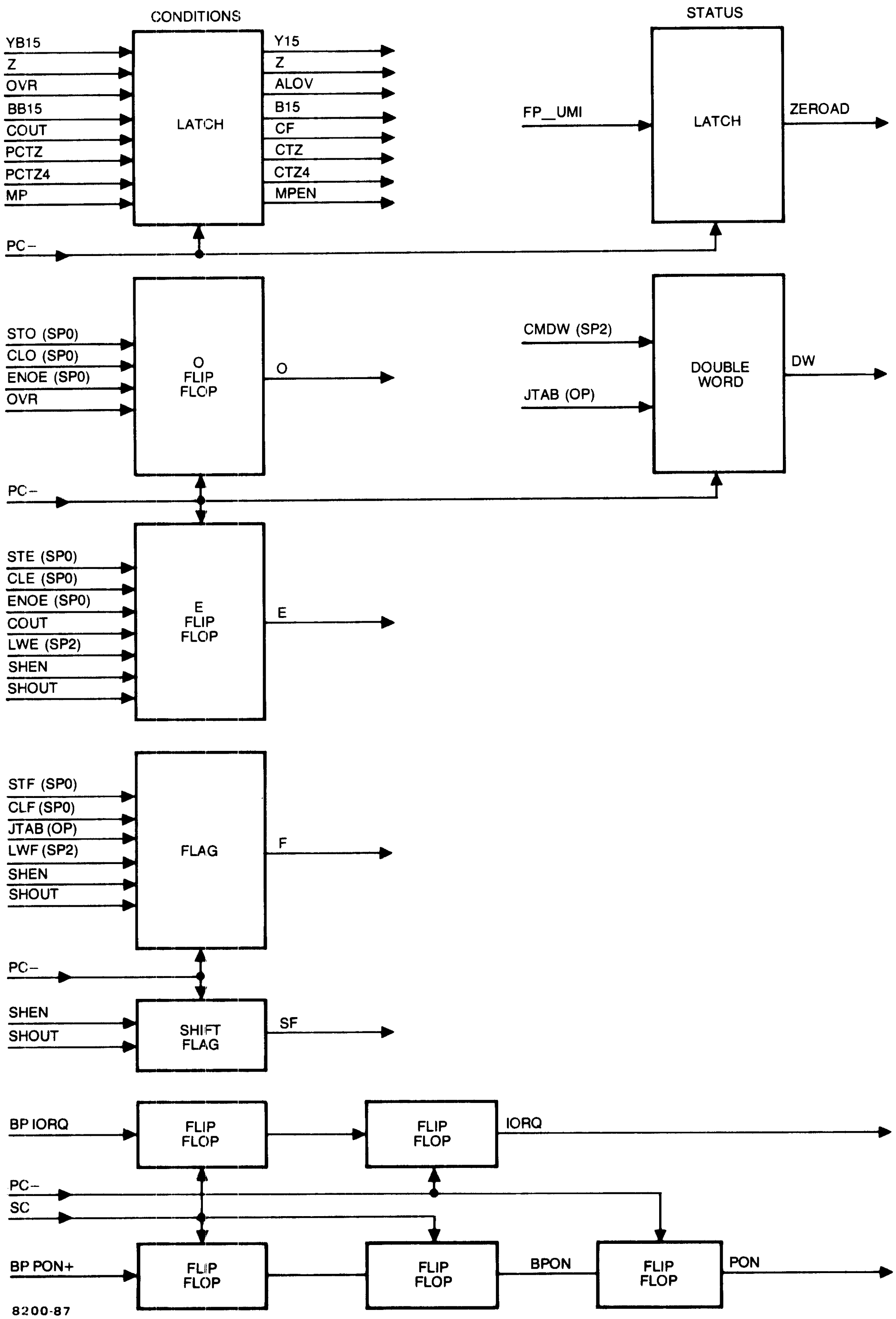


Figure 3-9. Condition Register Block Diagram

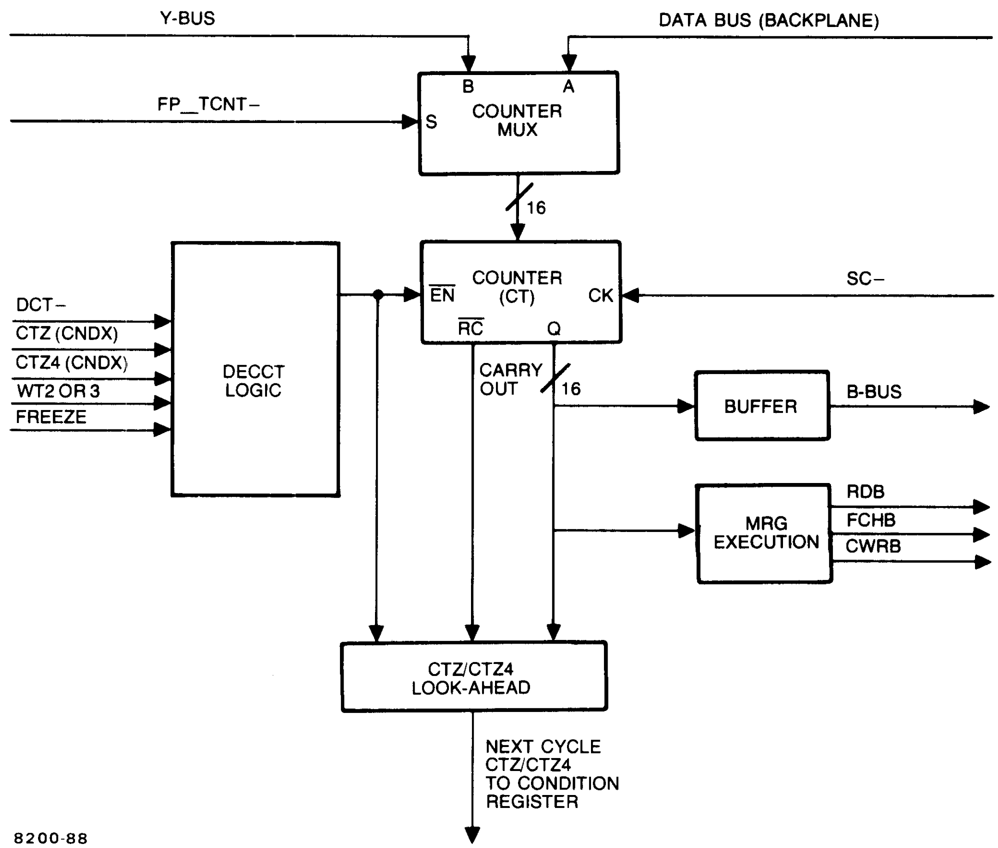


Figure 3-10. Counter Block Diagram

The DECCT logic looks at various decoded microorders in order to generate a signal to decrement the counter. This involves the following conditions: DCT microorder, CTZ or CTZ4 used in the CNDX-Field with Word Type 2 or 3, and the processor clock FREEZE; i.e., no decrement if the clock is frozen.

Another logic block looks ahead to determine if the lower four bits or all 16 bits of the counter will be all zeros (CTZ4 or CTZ) next cycle.

When a JTAB OP is executed, the counter is used for MRG Execution. This involves the initiation of one of three memory access microorders (RDB, FCHB, or CWRB) according to the instruction contained in the counter. No memory access is initiated if the instruction is not an MRG.

3.4 THEORY of OPERATION

For the following logical operation descriptions, refer to the micromachine block diagram of Figure 3-2, the lower processor functional block diagram of Figure 3-3 and the lower processor schematics located at the end of this section. These descriptions are for the six functional circuit areas of the lower processor card as described in general terms under the block diagram description, paragraph 3.3.

3.4.1 CLOCK GENERATION

Clock generation is based on two oscillators: 14.7456 MHz for the communications clock U99 (31-A) and 20.0 MHz for the fast clock U126 (31-B). The oscillators are hybrid crystal oscillator packages. For diagnostic purposes, the output of the fast clock oscillator (ICLK) may be disabled and an external clock signal (ECLK) used. The signal CLOCK from OR gate U127 (32-C) is passed by buffer U109 (33-A) to become the backplane FCLK- signal.

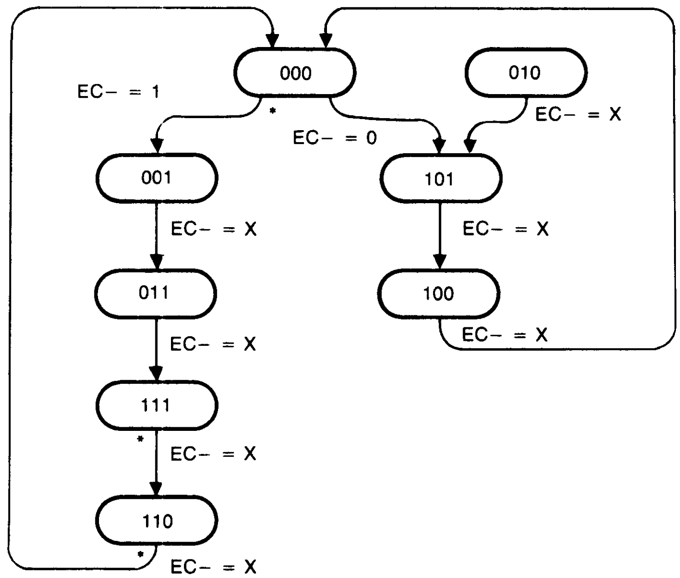
U119 and U128 (located at 33-B,34-B, and 36-B) provide three J-K flip flops which comprise a divide-by-five circuit which reduces CLOCK to the pre-buffered system clock signal (PRESCLK) of 250 nanoseconds PRESCLK is then driven through buffer U109 to become the backplane SCLK- with a 40% duty cycle. The output of the communications crystal oscillator (PRECCLK) is driven through the same buffer to become the backplane CCLK.

The clock state machine is shown in Figure 3-11. It has seven valid states and comprises the error correction signal from the memory array cards (EC-). EC- is asserted when error correction is required during a memory read. When EC- is not asserted, the state machine will loop through a sequence of five states, generating the normal 40/60 SCLK. When EC- is asserted, the short half-cycle of SCLK will be extended by three additional FCLK cycles. That is, following the cycle where memory data was corrected, the short half-cycle of SCLK will be 250 nanoseconds followed by a normal length long half-cycle.

The clock-generation state sequence with error correction is shown in Figure 3-12. A state table is shown in Table 3-2. The state variables correspond to the Q outputs of the flip-flops. Thus:

Q0 = U119-5
Q1 = U119-9
Q2 = U128-9

STATES ARE WRITTEN AS: $Q_0Q_1Q_2$



X = DON'T CARE
* = STATES IN WHICH EC- MAY BE ASSERTED

8200-89

Figure 3-11. Clock-Generator State Machine

A state is referenced as "Q0 Q1 Q2". The J-K inputs shown in the state table refer to the corresponding flip-flop inputs. Although EC- is actually a don't care for all states except state 000, it would only be asserted (if an error correction is required) during states 111, 110, or 000. The state machine is not initialized at power-up, but will self correct to a valid state sequence. There is one invalid state (010) which will go to a valid sequence in three FCLK cycles.

Table 3-2. Clock Generation State Machine

PRESENT STATE				FLIP FLOP INPUTS						NEXT STATE		
Q0	Q1	Q2	EC-	J0	K0	J1	K1	J2	K2	Q0	Q1	Q2
0	0	0	0	1	1	0	1	1	0	1	0	1
0	0	0	1	0	1	0	1	1	0	0	0	1
0	0	1	0	0	0	1	0	1	0	0	1	1
0	0	1	1	0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	1	1	0	1	0	1
0	1	0	1	1	1	0	1	1	0	1	0	1
0	1	1	0	1	0	1	0	1	0	1	1	1
0	1	1	1	1	0	1	0	1	0	1	1	1
1	0	0	0	1	1	0	1	0	1	0	0	0
1	0	0	1	0	1	0	1	0	1	0	0	0
1	0	1	0	0	0	0	0	0	1	1	0	0
1	0	1	1	0	0	0	0	0	1	1	0	0
1	1	0	0	1	1	0	1	0	1	0	0	0
1	1	0	1	1	1	0	1	0	1	0	0	0
1	1	1	0	1	0	0	0	0	1	1	1	0
1	1	1	1	1	0	0	0	0	1	1	1	0

Two data clocks are generated to be used for clocking read data from the frontplane. PL_DC- is used by the counter circuitry, and FP_DC- is sent over the frontplane to be used by PU. Both these clocks are equivalent to the state variable Q0-. DC-, effectively, provides a rising edge at every transition to state 000.

This gives a rising-edge data clock pulse at every rising edge of SCLK-. If the short half cycle is extended by an error correction, there will be an additional rising edge of DC- three FCLK cycles into the short half-cycle. Thus, following the rising edge of DC- there is a full 250 nanoseconds left in the cycle. The counter, for example, will clock data in twice if an error correction occurs, the first one being extraneous.

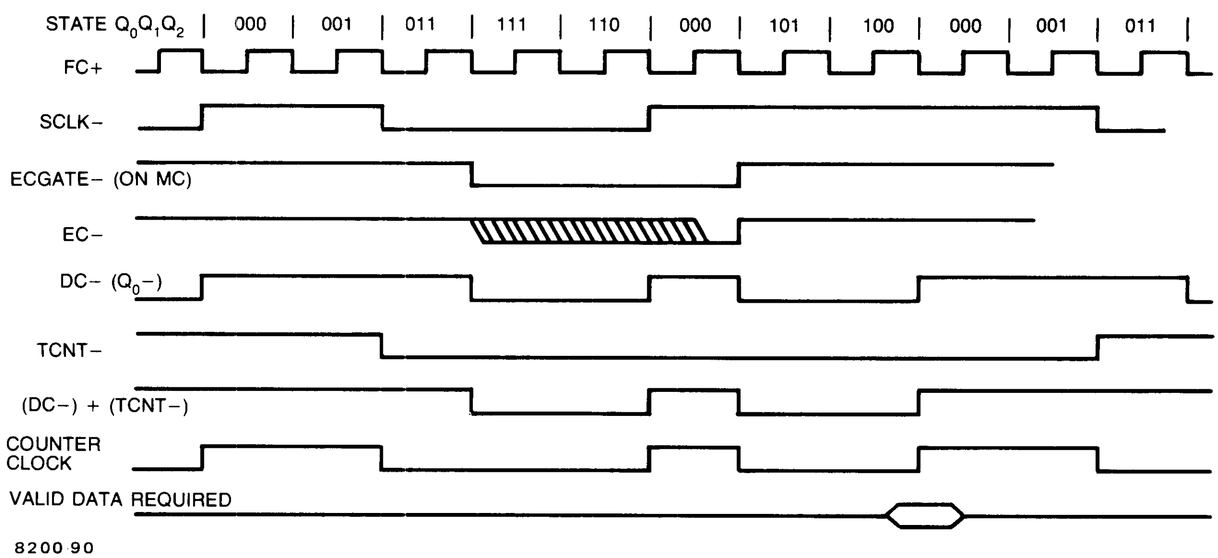


Figure 3-12. Clock-Generation With Error Correction

To minimize clock skew with other cards, PL receives SCLK- and FCLK- from the backplane, through U109 before using it on the card. The outputs of this buffer are FC+ and SC+ which are the on card fast clock and system clock signals, respectively. These signals, however, are used only by the clock generation logic and need further qualifying or buffering before they are sent to the rest of the processor cards.

U138 (33-D) drives PC- (Processor Clock) and SC- (System Clock) which are used elsewhere. SC+ is an input to each of the NAND gates of U138. The other input of the SC- driver is tied high. The other gates drive three copies of PC-, referred to as PL_PC-, BP_PC-, and FP_PC-. The other input of these drivers is FP_FREEZE-, so that when low, PC- will never go low. Multiple copies of PC- are used to reduce loading on U138 and reduces skew between the clock signals.

The lower processor card uses PL_PC-, while the upper card uses FP_PC- and BP_PC-. Both cards use the same copy of SC-. PL_PC- is inverted to obtain PL_PC+ which is used only on PL.

A timing diagram for the LC Generation circuit is shown in Figure 3-13. The PRELC- signal is gated with PL_PC- so that it will be de-asserted soon after the rising edge of PL_PC-. This also assures that it is not asserted in a frozen cycle.

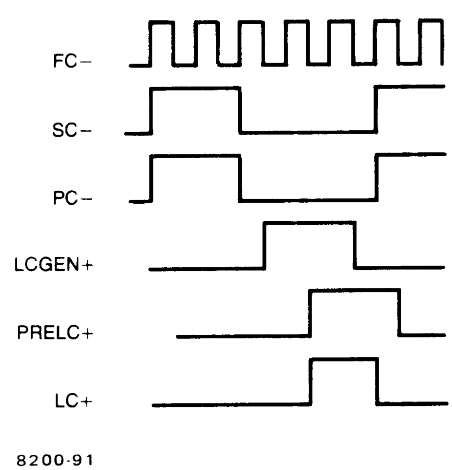


Figure 3-13. Timing Diagram of LC Generation

3.4.2 MICROINSTRUCTION REGISTER AND DECODERS

This portion of the PL is covered in schematic sheets 2 and 4. Also refer to Table 3-3 which shows the binary codes assigned to the A700 microorders.

The microinstruction register (MIR) is comprised of four S374 latches U92, U102, U112, U122 (located at 21-A, B, C, and D). These latches receive the control store data bus (CSD) and drive the MIR bus. The latches are clocked on the rising edge of PL_PC- which is thus designated the beginning or end of the microcycle.

3.4.3 OP-Field

MIR bits 27-31 of U122 are decoded by a block of combinational logic to provide information on Word Types and OP field to the MIR decoders and other places on PL. Following is a summary of the logic equations used:

WT12	= MIR31 AND MIR30	(Word Type 1 or 2)
WT56	= (MIR29′ OR MIR30′) AND MIR31′	(Word Type 5 or 6)
WT23	= (MIR29 OR MIR30′) AND MIR31	(Word Type 2 or 3)
JTAB	= WT12+ AND (MIR28′ AND MIR29′)	(JTAB OP)
SPOC	= WT12+ AND MIR29 AND MIR27	(SPOT or SPOF OP).

3.4.3.1 CNDX Field

The condition encoder consists of two 8-to-1 tristate multiplexers. Each MUX receives eight condition signals as data inputs and the lower three bits of the CNDX field to select one of the conditions. If the upper bit of the CNDX-Field is "1" then U62 (25-A) is enabled; if the upper bit is "0" then U103 (25-D) is enabled. The inverting outputs are tied together to create the signal, CNDSPEC-, which is the negative sense of the condition specified. MIR28, which indicates true or false on conditional OPs (1=true, 0=false), further qualifies CNDSPEC- to get TEST+. TEST+ is a "1" when the sense of the condition specified is met:

TEST = CNDSPEC XOR MIR28.

Note that none of these signals indicate whether or not there is a conditional OP.

Table 3-3. Summary of Microorders by Field

FIELD										
CODE	**OP**	**CNDX**	**SP0**	**SP1**	**SP2**	**ALUS**	**ALU**	**ABUS**	**BBUS**	**STOR**
00000	IMM	SF	NOP*	NOP*	NOP*	UMPY	SPEC	A	A	A
00001	IMM	F	LDQ	LDQ	CMDW	TMPY	SBAC	B	B	B
00010	IMM	ALOV	RR1	RR1	DCT	SM2C	SBBC	X	X	X
00011	IMM	CF	RL1	RL1	CLF	RMLC	ADDC	Y	Y	Y
00100	IMM	YZ	LR1	LR1	STF	DNRM	ADBC	ACC*	ACC*	ACC
00101	IMM	Y15	LL1	LL1	IP	SNRM	CMBC	HP1**	HP1**	HP1**
00110	IMM	B15	AR1	AR1	LWF	DIV	ADAC	HP2**	HP2**	HP2**
00111	IMM	INTF	AL1	AL1	LWE	DIV1	CMAC	USR**	USR**	USR**
01000	JMPL	IORQ	RDP	RDP	CMID	SWAP	ZERO*	S0	S0	S0
01001	JMPL	PON	IN	IN	RDP	SWZU	CAND	S1	S1	S1
01010	JSBL	MPEN	RDB	RDB	WRIO	SWZY	XNOR	S2	S2	S2
01011	JSBL	O	STE	STE	DN	ZUY	XOR	S3	S3	S3
01100	JMP	E	CLE	CLE	FCHP	ZLY	AND	S4	S4	S4
01101	JMP	INTP	FCIN	FCIN	RDIO	SRG	INOR	S5	S5	S5
01110	JSB	CTZ4	ACF	ACF	CT30	RL4	NAND	S6	S6	S6
01111	JSB	CTZ	IP	IP	CT74	ASG	IOR	S7	S7	S7
10000	JMPF		STOR						GRIN	GRIN
10001	JMPF		—						FA	WRP
10010	JMPT		—						SRIN	SRIN
10011	JMPT		—						P	P
10100	JSBF		—						Q	NOP*
10101	JSBF		—						T	WRB
10110	JSBT		—						IST	IST
10111	JSBT		—						N	N
11000	JTAB		IFCH						PRIN	PRIN
11001	—		BFB						MA	CWRB
11010	RTN		CK2						MEMR	MEMR
11011	NOP*		ENOE						CT	CT
11100	RTNF		STO						SR	LR
11101	SPOF		CLO						MAP	MAP
11110	RTNT		FCHB						CAB	CAB
11111	SPOT		LDBR						CXY	CXY

OP Field Divisions:

OP1=JTAB	OP2=SPOT	OP3=JMPF	OP4=JMP	OP5=JMPL	OP6=IMM
NOP	SPOF	JMPT	JSB	JSBL	
RTN	RTNT	JSBF			
	RTNF	JSBT			

* Default Microorder.

**Reserved register for Hewlett-Packard (HP1 and HP2) and user (USR).

3.4.3.2 SP0, SP1 And SP2 Fields

The SP2-Field is decoded by two 3-to-8 decoders. Each decoder receives the lower three bits of the SP2-Field as data and generates eight decoded signals each of which corresponds to an SP2 microorder. U61 (27-C) is enabled if the upper bit of the SP2-Field is a "0"; U60 (27-D) is enabled if it is a "1". The decoders are further enabled by signals from the OP field such that the SP2 signals are asserted only if the SP2-Field is present in the current Word Type:

SP2 DECODER ENABLE = MIRQ1 AND MIR30

where MIRQ1 = MIR29 XOR MIR31.

This enables the SP2 decoders only for Word Types 1 or 4.

Each SP0/SP1 decoder receives the lower three bits of the SP0/SP1-Field as data and generates eight decoded signals, each of which corresponds to an SP0 or SP1 microorder. The upper bit of the SP0/SP1-Field must be forced to zero for Word Types 3 and 4, since only the SP1-Field is available for these. (Remember that the SP1-Field is a subset of the SP0-Field with the upper bit always zero). Thus, the upper bit (4) of the SP0/SP1-Field is forced to zero except during Word Types 1 or 2:

SP0F4- = (MIR22 AND WT12+).

U77 (42-A) is the SP0 decoder; i.e., it decodes the lower part of the SP0-Field which is not shared by the SP1-Field. U87 (42-B) is the SP0/SP1 decoder; i.e., it decodes the portion shared by the SP0- and SP1-Fields:

SP0 DECODER ENABLED = SP0F3Q AND DISSP0- AND SP0F4+

where SP0F3Q = MIR21 AND SPEC- ,and DISSP0- = TEST+ OR SP0C-;

SP0/SP1 DECODER ENABLED = SP0F4- and DISSP0- AND SP0F3+

where SP0F3+ = SP0F3Q AND WT56- ,and DISSP0- = TEST+ OR SP0C- .

also where SPEC indicates SPEC in the ALU-field, and DISSP0- indicates a conditional SP0 OP where the condition was not met.

A Store Enable Signal (STEN) is always asserted except when the SP0-Field contains STOR with a conditional SP0 OP-code and the condition is not met. The equation for STEN takes into account certain don't care conditions, such as the unused SP0 OP-codes. Taking this into account:

STEN+ = (SP0F4 AND MIR21′ AND (TEST+)′ AND SP0C)′

3.4.3.3 B- and STOR-Fields

The B-field is decoded by two 3-to-8 decoders. Each decoder receives the lower three bits of the B-field as data and generates eight decoded signals each of which corresponds to a B-field microorder. A signal of the form E[register]B- is generated for each B-field microorder excluding R0 through R15.

U64 (42-D) is enabled if the fourth bit (MIR8) of the B-field is a "0"; U65 (42-E) is enabled if it is a "1". Both decoders are enabled only if the fifth bit (MIR9) is a "1".

The STOR-Field is decoded by two 3-to-8 decoders. Each decoder receives the lower three bits of the STOR-Field as data and generates eight decoded signals each of which corresponds to a STOR-Field microorder (one of these is a no-connect corresponding to a NOP microorder). A signal of the form LY[register]- is generated for each STOR-Field microorder excluding R0 through R15.

U72 (27-B) is enabled if the fourth bit (MIR3) of the STOR-Field is a "0"; U82 (27-A) is enabled if it is a "1". Both decoders are enabled only if the fifth bit (MIR4) is a "1" and STEN- is true (low).

3.4.4 SEQUENCER AND CONTROL STORE

For the following description, refer to the schematic diagram, sheets 1 and 9 at the end of this section. The reader should refer to the AM2900 Family Data Book for a detailed desciption of the 2911 microprogram sequencer slice.

3.4.4.1 Sequencer

The 2911s are configured to provide a 14-bit microaddress which allows the microprogrammer to specify a 14-bit or six-bit jump address. To accomplish this the sequencer slices are logically divided into the two least significant slices (six bits) and the two most significant slices (eight bits). Each pair of slices receives different control signals. The least significant slice (U80, 17-B) acts as two-bit slice. This is done by using only the two lower input and output bits. The effective carry-out from this slice is determined using an AND-gate on the two address outputs:

SQCN+2 = BCSA0 AND BCSA1

where BCSA0 and BCSA1 are the buffered Control Store Address bus and the carry-in to this slice always equals one.

The sequencer-control PAL (generically a PLA) with the U83 OR gates generate the six control signals used by the 2911s:

CONTROL SIGNAL	2911 INPUT	SLICE PAIR
SQ0	FE-	LSS, MSS
SQ1	PUP	LSS, MSS
	S0	LSS
SQ2	S0	MSS
SQ3	qualifies other control signals	
S1LSS	S1	LSS
S1MSS	S1	MSS

To generate these signals, the sequencer Control PAL looks at the entire OP-Field (MIR27- MIR31) and TEST+ from the Condition encoder. Refer to Table 3-4 for the Sequencer PAL coding.

The direct inputs for sequencer bits 0 through 9 are provided by the Direct Address Bus (DAB). The direct inputs for bits 10 through 13 come directly from the Address Field (MIR18 - MIR21) since the only functions that specify these bits are the long jumps. DAB bits 0 through 9 may come from the Counter, the Address Field or the Lookup Table under the control of signals WT12 and SP2CT. WT12 indicates that the OP-Field might contain JTAB. SP2CT indicates a jump modify (using CT) in the SP2-Field or a Word Type 5 jump modify (JMPCT30); i.e., Word Type 5 with SPEC in the ALU-field.

If a jump will not occur in the current cycle, the contents of the DAB are a don't card. The CT/DAB MUX (U59, 11-B), when enabled, will drive DAB bits 0 through 3. If CT74- (CT74 in the SP2-Field) is asserted, CT4 through CT7 is selected; otherwise CT0 through CT3 is selected. The following table shows how WT12 and SP2CT determine the contents of the DAB:

FUNCTION	WT12+	SP2CT+	DAB3-0	DAB7-4	DAB9-8
Jump or don't care	0	0	MIR	MIR	MIR
Jump w/ modify	0	1	CT	MIR	MIR
JTAB	1	0	LUT	LUT	"01"
JTAB	1	1	LUT	LUT	"01"

Note that the only jump available in Word Types 1 or 2 is JTAB. A jump modify special cannot be used with JTAB.

The ZEROSQ- signal will force the sequencer address to all zeros if any of these conditions occur: power up (BPON), the previous state had an unimplemented microinstruction (ZEROAD-), or a microcode timeout has occurred (FP_MTO-). A JTAB microorder also forces address bits 10 through 13 (the most significant slice) to all zeros, so that a jump through the LookUp Table always lands in the address space between 0X0100 and 0X01FF (hex).

Table 3-4. Sequencer Control PAL Coding

INPUTS			OUTPUTS				RESULTING SEQUENCER INPUTS					
OP	MIR 31<=>27	TEST+	FE+	SQ1	SQ2	SQ3	FE-	PUP	MSS S1	MSS S0	LSS S1	LSS S0
IMM	00	-	0	0	0	0	1	(0)	0	0	0	0
JSBT/F	101	0	0	0	0	0	1	(0)	0	0	0	0
	101	1	1	1	0	0	0	1	0	0	1	1
JMPT/F	100	0	0	0	0	0	1	(0)	0	0	0	0
	100	1	0	1	0	0	1	(1)	0	0	1	1
RTNT/F	111-0	0	0	0	0	0	1	(0)	0	0	0	0
	111-0	1	1	0	0	1	0	0	1	0	1	0
JMPL	0100-	-	0	1	1	( )	1	(1)	1	1	1	1
JSBL	0101-	-	1	1	1	( )	0	1	1	1	1	1
RTN	11010	-	1	0	0	1	0	0	1	0	1	0
SPOT/F	111-1	-	0	0	0	0	1	(0)	0	0	0	0
NOP	11011	-	0	0	0	0	1	(0)	0	0	0	0
JTAB	11000	-	1	1	1	( )	0	1	1	1	1	1
JMP	0110-	-	0	1	0	0	1	(1)	0	0	1	1
JSB	0111-	-	1	1	0	0	0	1	0	0	1	1

- = don't care inputs
( )= don't care outputs

3.4.4.2 Control Store

The sequencers drive the Control Store Address (CSA) directly over the frontplane to Writable or PROM Control Store cards and to the (optional) floating point card. Before being used on-card, the CSA-Bus is buffered (U131 and U130, 91-A,B). The Buffered CSA-Bus (BCSA) is then driven to the four 2k by eight-bit PROMs which comprise on-card control store. These PROMs directly drive the Control Store Data Bus (CSD) which is also received from the frontplane. FP_CSIDWC- is the bottom of the Control Store Priority chain driven by the lowest priority WCS or PCS card, or tied high in the absence of any of these cards.

FP_CSIDWC- is passed to the floating point card which drives an additional disable signal to be received by PL, FP_CSIDFP-. Either of these signals, when asserted, will disable on card control store PROMS and the UMI Buffer from driving the CSD Bus.

The control store PROMs may be either 2k, 4k or 8k by eight-bit PROMs. Currently, 2k PROMs are used with no immediate plans to expand the control store space. PL is configured for the correct PROM size with jumpers W1 and W2. When neither jumper is inserted (2k), PROM chip selects CS2 (A11) and CS3 (A12) are always high. When W1 (4k or 8k) is inserted, BCSA11 is passed to CS2 (A11). When W2 (8k) is inserted, BCSA12 is passed to CS3 (A12).

An Unimplemented MicroInstruction (UMI) occurs when the CSA does not address on-card control store and control store is not disabled by a higher priority card.

UMI = CSONBD- AND CSID-

where CSID- = FP_CSIDWC- AND FP_CSIDFP-
CSONBD- = (BCSA11 AND ONBD2K+) OR (BCSA12 AND ONBD8K-) OR BCSA13;

and where
ONBD2K is configured for 2k PROMs, and
ONBD8K is configured for 8k PROMs.

Note: A 4k PROM configuration is indicated by (ONBD2K+)' AND ONBD8K-

In the event of a UMI, Control Store PROM 3 (bits 0 through 3 and 28 through 31) is disabled. These bits are then driven by the UMI buffer:

CSD bits	UMI Buffer
31-28	0000
3-0	0100

Bits 4 through 27 will still be driven by the Control Store PROMs. Thus, on a UMI the following microinstruction is executed:

OP/IMM DATA/? B/? ALU/? STOR/NOP or ACC

where ?= unknown microorder driven by Control Store PROMs (bits 4-27).

In this way we assure that a UMI will not affect system status. The only affect of a UMI is that the accumulator may be overwritten and the processor conditions may change.

3.4.5 2903 AND 2903 CONTROL LOGIC

Refer to the schematic diagram sheets 4, 5, and 8 for the Control Logic. For a description of the operation of the 2903, refer to the AM2900 Family Data Book. The generation of all the 2903 control signals is described in the following paragraphs.

3.4.5.1 A-Bus

The 2903 A-Address will come from the A-field of the MIR for Word Types 1 or 2, excluding JTAB. For JTAB the A-Address is the A-field with the lowest bit forced to zero if Counter bit 11 is a zero (a CAB microorder). For Word Types 3, 4 and 5 the A-Address will be the accumulator (R04). For Word Type 6 the A-Address is a don't card, but will default to the accumulator. The A-field is MIR26 (msb) through MIR23 (lsb).

Thus, the logic equations for the A-field are:

A3 = MIR26 AND WT12+
A2 = MIR25 OR WT12-
A1 = MIR24 AND WT12+
A0 = MIR23 AND WT12+ AND (PJTAB AND CT11-)'

where PJTAB is a pre-JTAB signal which, when ANDed with WT12+ indicates a JTAB microorder.

Actually a buffered version of WT12+ (BWT12+) is used here.

The DA inputs of the 2903 are driven directly by the MIR Immediate Data Field (MIR14 - MIR29). The 2903 EA- input selects the MUX for the "R" input of the ALU. For Word Types 1 through 5, register data is selected; for Word Type 6, DA is selected:

EA- = IMM = MIR30' AND MIR31'

3.4.5.2 B-Bus

Two levels of multiplexing generate the 2903 B-Address. The first level (U55 and U56 , 46-C,D) selects the MIR B-field during the first half of the cycle (PC+ =0) and the MIR STOR-Field during the second half of the cycle. This multiplexer also selects FP_LRMAB0 (last read memory address bus bit 0) during the first half-cycle and FP_MAB0 (current memory address bus bit 0) during the last half-cycle. The outputs of U55 and U56 are used as control signals to obtain the B Address:

BA4+	BA1+	BA0+	B FIELD	STOR FIELD	B3	B2	B1	B0
0	-	-	R0-R15	R0-R15	B/S	B/S	B/S	B/S
1	0	1	T or dc	WRP,WRB,CWRB or dc	0	0	0	BAB
1	1	0	CAB	CAB	0	0	0	CT11
1	1	1	CXY	CXY	0	0	1	CT3

where: dc = don't care microorder
B/S= the appropriate B- or STOR-Field bit
BAB= FP_LRMAB0 or FP_MAB0 depending on which half cycle it is in.

The second level of multiplexing is done with combinational logic (U67 , et al, 47-C) according to the following equations:

```
B0 = {(CT3- AND BA4+ AND BA1+ AND BA0+)
      OR (BAB- AND BA4+ AND BA1-)
      OR (BA4- AND BA0-)
      OR (CT11- AND BAQ0)}'
B1 = (BA1- OR BAQ0)'
B2 = BA4- AND BA2+
B3 = BA4- AND BA3+
```

where BAQ0 = BA0- AND BA4+.

Note that, in order to get the correct B-destination address for the JTAB MRG Execution (if a CWRB should be decoded), it is neccessary to code CWRB in the STOR-Field. This will insure that the B-destination address generated is either A or B based on FP_MAB0.

The B-bus (2903 DB) will be driven by the 2903 if the B-bus source is one of the 2903 RAM registers or if the B-bus source is T and the last read was from A or B (FP_LRAB). Otherwise, DB will be an input and the B-bus will be driven from some other source:

```
OEB- = MIR9' OR ECABB OR ECXYB OR (ETABB AND LRAB)
```

The Y-bus will be stored into the 2903 Register File if the STOR-Field destination is one of the 2903 registers, or if the STOR-Field destination is a memory write and the memory address is either A or B (FP_ABWR). The expressions are:

```
STRF+ = MIR4' OR FP_ABWR OR LYCAB OR LYCXY
WE-   = STRF+ AND STEN+ AND LC+
```

where: STRF+ = store to register file
       STEN+ = store enable (from SP0 decode).

Gating with LC+ insures that WE- is not asserted until the B-destination address and the other qualifying signals have settled.

3.4.5.3 Instruction Bits I0 - I8

The 2903 instruction bits I1 - I4 come directly from the MIR ALU-field. SPEC is decoded from this field to indicate Special ALU functions to other blocks of control logic:

```
SPEC+ = MIR10' AND MIR11' AND MIR12' AND MIR13'
```

The generation of instruction bits I5 - I8 is handled entirely by a programmable aray logic chip U32 (53-A), a PAL (generically a PLA). I5 - I8 perform the execution of LDQ, all standard shift functions and 2903 Special ALU functions. The microcode does not allow conditional operation of any of these microorders, so the hardware does not check for conditions being met. Information on the PALs can be found in the Monolithic Memories Inc. Bipolar LSI Data Book.

Because of timing considerations, it was necessary that there be no more than two gate delays between PC- and the PAL inputs or one gate delay between the MIR output and the PAL inputs. Thus the PAL must look directly at some OP-Field information in order to determine the Word Type. WT12 is used to distinquish between the SP0- and SP1-Fields (i.e., it indicates if MIR22 is a don't-care). Expressions MIR31NOR30 and MIR31NOR29, when ANDed together in the PAL, indicate whether the Word Type is 5 or 6:

WT56- = (MIR31 NOR MIR30)' AND (MIR31 NOR MIR29)'

SPEC (Special ALU function) and DW (Double Word bit) are also used in the generation of I5 - I8. This is summarized in Table 3-5.

A shift enable signal, SHEN, is generated whenever a single-bit shift function is executed. The single bit shift functions are standard shifts and 2903 Special ALU operations, excluding SM2C. SHEN is used by the condition register to indicate when to update the shift flag and (in the case of a shift link) other conditions. An examination of Table 3-5 shows the following relation between I5-8 and shift functions: SHEN+ = (I5)' OR (I7)'.

Instruction bit I0 must be high when Q is in the B-field (ENQB) or when SPEC is in the ALU-field and no 2903 ALU operation will be performed. The latter occurs when an External Special (MIR21=1) is in the SP0/SP1-Field or when the OP-Field contains a Word Type 5 or 6 (WT56). The latter also prevents the overwriting of Q on a unimplemented microinstruction. The expressions for this are:

I0 = ENQB OR JMPCT30 OR EXSPEC
EXSPEC = MIR21 AND SPEC+ AND WT56-

This assures, when the ALU-field contains SPEC and no 2903 Special ALU function occurs, that CF and ALOV will be cleared at the end of the microcycle and that Q will not be overwritten.

3.4.5.4 Shift Linkage

All the linkage is contained in the Shift Linkage PAL which executes the shift functions as defined in the microcode description. (See 92045A Microprogramming Manual, part no. 92045-90001.)

The PAL16L8 (U22, 52-C) has bidirectional input/outputs which are used to receive and drive the 2903 shift linkage bits: SIO0, SIO15, QIO0, and QIO15. Examination of the I5-I8 generation table and Tables 3 (ALU Destination Control) and 4 (Special Functions) in the AM2900 Family Data Book will show that I8 always indicates the direction of the shift (including don't card conditions):

I8	SHIFT	PAL DRIVES (ENABLES)	PAL RECEIVES (DISABLES)
1	LEFT	SI00, QI00	SI015, QI015
0	RIGHT	SI015, QI015	SI00, QI00

With the appropriate pairs being driven, the PAL uses its other inputs to determine what to drive onto the shift lines. For no shift, it makes no difference what is driven onto the shift lines. SPEC, DW and the lower three bits of the SP0/SP1-Field are used to distinguish what special or standard shift is to be performed. Only the lower three bits of the SP0/SP1-Field are needed since there are separate groups for the standard shifts and the 2903 ALU Specials.

The Shift Linkage PAL uses LWE (link with E), E, LWF (link with F) and FLAGN-1 if a shift link is specified in the SP2-field. The N output of the most significant 2903 bit (equivalent to the sign bit) is used for arithmetic right shifts. Table 3-6 shows the desired shift linkage functions.

Table 3-5. I5 - I8 Generation Logic Table

INPUTS						OUTPUTS			
FUNCTION	WT12+	WT56-	MIR 22<=>18	DW+	SPEC+	I8	I7	I6	I5
NOP	1	-	00000	-	0	1	1	1	1
	0	1	-0000	-	0	1	1	1	1
LDQ	1	-	00001	-	0	0	1	1	1
	0	1	-0001	-	0	0	1	1	1
single: RR1	1	-	00010	0	0	0	0	0	1
	0	1	-0010	0	0	0	0	0	1
RL1	1	-	00011	0	0	1	0	0	1
	0	1	-0011	0	0	1	0	0	1
LR1	1	-	00100	0	0	0	0	0	1
	0	1	-0100	0	0	0	0	0	1
LL1	1	-	00101	0	0	1	0	0	1
	0	1	-0101	0	0	1	0	0	1
AR1	1	-	00110	0	0	0	0	0	0
	0	1	-0110	0	0	0	0	0	0
AL1	1	-	00111	0	0	1	0	0	0
	0	1	-0111	0	0	1	0	0	0
double: RR1	1	-	00010	1	0	0	0	1	1
	0	1	-0010	1	0	0	0	1	1
RL1	1	-	00011	1	0	1	0	1	1
	0	1	-0011	1	0	1	0	1	1
LR1	1	-	00100	1	0	0	0	1	1
	0	1	-0100	1	0	0	0	1	1
LL1	1	-	00101	1	0	1	0	1	1
	0	1	-0101	1	0	1	0	1	1
AR1	1	-	00110	1	0	0	0	1	0
	0	1	-0110	1	0	0	0	1	0
AL1	1	-	00111	1	0	1	0	1	0
	0	1	-0111	1	0	1	0	1	0
other	1	-	-1	-	0	1	1	1	1
	0	1	-1	-	0	1	1	1	1
(SPEC): UMPY	-	1	-0000	-	1	0	0	0	0
TMPY	-	1	-0001	-	1	0	0	1	0
SM2C	-	1	-0010	-	1	0	1	0	1
TMLC	-	1	-0011	-	1	0	1	1	0
DNRM	-	1	-0100	-	1	1	0	1	0
SNRM	-	1	-0101	-	1	1	0	0	0
DIV	-	1	-0110	-	1	1	1	0	0
DIV1	-	1	-0111	-	1	1	0	1	0
other	-	1	-1	-	1	1	1	1	1

Table 3-6. Shift Linkage Functions

INPUTS						OUTPUTS		
FUNCTION		LWE-	LWF-	SPEC	DW	SIO SHIFT	QIO SHIFT	SHOUT
Single	RR1	1	1	0	0	SIO0 =>SIO15	X	SIO0
	RL1	1	1	0	0	SIO15=>SIO0	X	SIO15
	LR1	1	1	0	0	0 =>SIO15	X	SIO0
	LL1	1	1	0	0	0 =>SIO0	X	SIO15
	AR1	1	1	0	0	N =>SIO15	X	SIO0
	AL1	1	1	0	0	0 =>SIO0	X	SIO15
single,link	RR1	0	1	0	0	E =>SIO15	X	SIO0
		1	0	0	0	F =>SIO15	X	SIO0
	RL1	0	1	0	0	E =>SIO0	X	SIO15
		1	0	0	0	F =>SIO0	X	SIO15
	LR1	0	1	0	0	E =>SIO15	X	SIO0
		1	0	0	0	F =>SIO15	X	SIO0
	LL1	0	1	0	0	E =>SIO0	X	SIO15
		1	0	0	0	F =>SIO0	X	SIO15
	AR1	0	1	0	0	E =>SIO15	X	SIO0
		1	0	0	0	F =>SIO15	X	SIO0
	AL1	0	1	0	0	E =>SIO0	X	SIO15
		1	0	0	0	F =>SIO0	X	SIO15
double	RR1	1	1	0	1	QIO0 =>SIO15	SIO0 =>QIO15	QIO0
	RL1	1	1	0	1	QIO15=>SIO0	SIO15=>QIO0	SIO15
	LR1	1	1	0	1	0 =>SIO15	SIO0 =>QIO15	QIO0
	LL1	1	1	0	1	0 =>SIO0	0 =>QIO0	SIO15
	AR1	1	1	0	1	N =>SIO15	SIO0 =>QIO15	QIO0
	AL1	1	1	0	1	0 =>SIO0	0 =>QIO0	SIO15
double,link	RR1	0	1	0	1	E =>SIO15	SIO0 =>QIO15	QIO0
		1	0	0	1	F =>SIO15	SIO0 =>QIO15	QIO0
	RL1	0	1	0	1	QIO15=>SIO0	E =>QIO0	SIO15
		1	0	0	1	QIO15=>SIO0	F =>QIO0	SIO15
	LR1	0	1	0	1	E =>SIO15	SIO0 =>QIO15	QIO0
		1	0	0	1	F =>SIO15	SIO0 =>QIO15	QIO0
	LL1	0	1	0	1	QIO15=>SIO0	E =>QIO0	SIO15
		1	0	0	1	QIO15=>SIO0	F =>QIO0	SIO15
	AR1	0	1	0	1	E =>SIO15	SIO0 =>QIO15	QIO0
		1	0	0	1	F =>SIO15	SIO0 =>QIO15	QIO0
	AL1	0	1	0	1	QIO15=>SIO0	E =>QIO0	SIO15
		1	0	0	1	QIO15=>SIO0	F =>QIO0	SIO15
	UMPY	-	-	1	-	internal	SIO0 =>QIO15	QIO0
	TMPY	-	-	1	-	internal	SIO0 =>QIO15	QIO0
	SM2C	-	-	1	-	x	x	x
	TMLC	-	-	1	-	internal	SIO0 =>QIO15	QIO0
	DNRM	-	-	1	-	QIO15=>SIO0	0 =>QIO0	SIO15
	SNRM	-	-	1	-	x	0 =>QIO0	QIO15
	DIV	-	-	1	-	QIO15=>SIO0	SIO15=>QIO0	SIO15
	DIV1	-	-	1	-	QIO15=>SIO0	SIO15=>QIO0	SIO15

x = don't care, no shift occurs. Internal = shift linkage is internal to the Am2903 (see Advanced Micro Devices Inc. Data Book, AM-PUB003.

3.4.5.5 Carry-In

The microcode description allows carry-in to be generated as a function of several different fields. The logical implementation of carry-in uses a 74S64 (U66 , 55-D) and looks at two different cases: Special ALU operations and non-Special ALU operations. If no 2903 ALU operation is performed, then carry-in is a don't care.

Carry-in for 2903 Special ALU functions when SPEC is in the ALU field can be used for multiply, divide, and floating point algorithms. Each function may include an arithmetic operation and a shift. The conditions CF, ALOV, YZ, and SF may be used represent different conditions for these specials. (External ALU Specials are logical operations performed outside the 2903 and CF and ALOV are cleared.

SPECIAL ALU	CARRY-IN
UMPY	0
TMPY	0
SM2C	Z
TMLC	Z
DNRM	0
SNRM	1
DIV	Z
DIV1	0

where Z is the Z output of the 2903 during the current cycle.

Thus,

CIN = Z if SPEC+ AND MIR19 AND (MIR20 NAND MIR18)
CIN = 1 if SPEC+ AND (MIR20 NAND MIR18) NOR MIR19.

For non-Special ALU operations, carry-in defaults to "0" for addition operations and "1" for subtraction operations. The microorder FCIN (force carry-in) causes the carry-in to be the opposite of the default state. An ACF (ALU with carry flag) will force carry-in to the state of CF regardless of the type of ALU operation. Note that FCIN and ACF cannot be asserted if SPEC is asserted. The carry-ins for non-Special ALU operations are the following:

	CARRY-IN	
ALU FIELD	NO FCIN	FCIN
SPEC	see above	
SBAC	1	0
SBBC	1	0
ADDC	0	1
ADBC	0	1
CMBC	0	1
ADAC	0	1
CMAC	0	1
ZERO	don't care	
CAND	don't care	
XNOR	don't care	
XOR	don't care	
AND	don't care	
NOR	don't care	
NAND	don't care	
IOR	don't care	

Thus,

CIN = 1 if (FCIN- XOR SUBOP-) AND ACF- AND SPEC-
CIN = CF if ACF+
otherwise CIN = 0

where SUBOP- is generated in the Sequencer Control PAL:

SUBOP- = MIR12 OR (MIR11 AND MIR10).

The 2903 ALU generates carry Generate (G) and Propagate (P) outputs for all but the most significant slice. These are standard functions and are used with a 74S182 chip look ahead carry generator to create carry-in signals for the three most significant 2903 slices. The ALU of the most significant 2903 slice generates N, the sign bit, CN+4, the carry-out (COUT), and OVR (a true two's complement overflow indication). These signals may represent different functions for 2903 ALU Specials.

3.4.5.6 Other Control Signals

The 2903s drive the Y-bus for both Standard ALU functions and 2903 Special ALU functions. For External ALU Specials, the 2903 Y-bus outputs are disabled and the Y-bus is driven by the upper processor card. The expression for external ALU Specials is:

OEY- = (EXSPEC-)'
EXSPEC- = (SPEC+ AND MIR21 AND WT56-)'

where EXSPEC- is used on PU to enable the External ALU PROMs.

The Z output is generated directly from the Y-bus regardless of the source, except for 2903 Special ALU operations where Z may represent a different function. For External ALU Specials, I0 will be high, so that Z will indicate all zeros on the Y-bus.

Although IEN- (Instruction Enable) is not used for any control purpose, it is necessary to strobe this signal to allow for the I5-I8 setup time required. (Refer to timing Table IIIB for the AM 2903 in the Advanced Micro Devices 2900 Family Data Book, AM-PUB003.) The IEN expression is:

IEN- = (LC+)′

The WRITE- output of the 2903 is not used.

3.4.6 CONDITION REGISTER

For the condition register theory of operation, refer to schematic sheets 3 and 6).

3.4.6.1 Conditions

Latches U93 and U52 (68-A,C) latch the following signals directly from other parts of PL as follows:

SIGNAL LATCHED	LATCH OUTPUT	CNDX MICROORDER
YB15 (Y-bus bit 15)	CY15	Y15
BB15 (B-bus bit 15)	CB15	B15
Z (2903 Z output)	CYZ	YZ
OVR (2903 OVR output)	ALOV	ALOV
COUT (2903 CN+4 output)	CF	CF
PCTZ (look ahead for CT all zeros)	CTZ	CTZ
PCTZ4 (look ahead for lower 4 bits of CT all zeros)	CTZ4	CTZ4
MP+	CMP+	MPEN

The backplane PON (power on) signal is clocked twice by U139 (123-E) in order to reduce the likelihood of an unstable output problem. This creates BPON, a card power-on signal, which is used for initialization on both processor cards. Since power-on is one of three conditions which may force a jump to microlocation zero, it is necessary for the microcode to be able to determine when such a force was caused by powering-up. Thus, BPON is latched one more time to become CPON (condition PON) which will be "0" (false) only during the first executed cycle after power-up (i.e., during the execution of location zero).

The timing of IORQ is such that it must be clocked on the falling edge of SC-. It is clocked once here and then clocked again at the rising edge of PC- in order to keep it synchronized with the rest of the micromachine.

The integer overflow register, 0, may be generated by a variety of conditions. STO and CLO will unconditionally set and clear 0, respectively. ENOE will set 0 according to OVR. In the absence of these specials, the state of 0 will not be changed. STO, CLO and ENOE are mutually exclusive. The expressions for overflow conditions are the following:

SETOFF = STO OR (ENOE AND OVR)
CLROFF = CLO.

The macro-extend register, E, is also generated from a number of conditions. STE and CLE will set and clear E, respectively. ENOE will set E according to COUT. LWE, when used with a shift function (SHEN) will set or clear E according to SHOUT. In the absence of these specials, the state of E will not be changed. STE, CLE and ENOE are mutually exclusive since they are in the same field. These specials can not occur with a shift function since shift functions are always in the SP0/SP1 field. The expressions for the extend condition are the following:

SETEFF = STE OR (ENOE AND CORBOR) OR (LWE AND SHEN AND SHOUT)
CLREFF = CLE OR (LWE AND SHEN AND SHOUT-)

where CORBOR is COUT for add operations, and COUT- for subtract operations,

CORBOR = SUBOP XOR COUT.

The general-purpose flag, F, may be set or cleared, respectively, by STF or CLF. LWF, when used with a shift function (SHEN), will set or clear F according to SHOUT. JTAB will always clear F. If none of these micoorders occurs, the state of F will not change. STF, CLF and LWF are mutually exclusive. JTAB may occur with any of these, although under normal conditions it will not. No priority is defined here, but in hardware, if there are microorders for both setting and clearing, F will be set. The expressions for the general-purpose flag are the following:

FLAGN+ = (FLAG0)′ OR (FLAG1)′ OR STF
(FLAG0)′= FLAGN-1 AND JTAB- AND CLF- AND (LWF AND SHEN)
(FLAG1)′= LWF AND SHEN AND SHOUT

where FLAGN-1 = F set at end of previous cycle
FLAGN+ = F which will be latched at end of current cycle.

The shift flag, SF, is set and cleared according to SHOUT when a shift function is executed (SHEN); otherwise, the state of SF is not changed. The shift flag expression is:

PSF = (SHEN+ AND SHOUT+) OR (SHEN- AND SF)

where PSF = pre-shift flag to be latched at end of current cycle
SF = shift flag latched at end of previous cycle.

The updating of certain conditions (Y15, B15, YZ, OVR, CF, and SF) is held off when the ALU-field contains ZERO. This is done by qualifying the clock input to U93 with ZERO as follows:

(CNDCK)′ = (PC-)′ AND ZERO-

where ZERO+ is generated by the Sequencer Control PAL; and
ZERO+ = MIR13 AND MIR12′ AND MIR11′ AND MIR10′.

3.4.6.2 Status

The condition register encompasses two status bits which affect processor operation, but are not accessible in the CNDX-Field. FP_UMI- (Unimplemented MicroInstruction) is latched directly from the control store logic. The result is ZEROAD- which, when asserted, forces the microaddress to zero.

The double word bit, DW, is complemented by CMDW and cleared by JTAB. If both microorders occur together, then DW will be cleared. The expression is:

PDW+ = (DW+ XOR CMDW-) NOR JTAB+

where PDW+ = pre-double word bit to be latched at end of current cycle; and
DW+ = double word bit latched at end of previous cycle.

The state of DW is not directly available to the microcode. (Note: the power-up state of DW is undefined.)

3.4.7 COUNTER

Refer to schematic sheets 4 and 7 for the counter. The counter multiplexers will pass either the backplane data bus or the Y-bus to the counter data inputs. When FP_TCNT- is low, indicating that the data available on the backplane is an instruction, then the data bus will be selected. Otherwise, the Y-bus is selected.

The counter is implemented with four type 74S169 up/down counters which are always in count down mode. The counters are clocked by:

Counter Clock = SCLK- AND (DC- OR TCNT-).

That is, they are clocked every SCLK cycle so that they may be clocked while the processor is frozen. This is done to eliminate clock skew with the counter. If the counters are clocked on a frozen cycle, the control signals will be held off so that the state of the counter will not be altered until the end of a non-frozen cycle.

Thus, the counter is loaded during a non-frozen cycle by LYCT- or during any cycle by FP_TCNT-. The counter is decremented only during a non-frozen cycle by DCT- or by a conditional Word Type (WT23) with CTZ or CTZ4 in the CNDX-Field. The expression for CTZ and CTZ4 is:

CTZ or CTZ4 in CNDX-Field = MIR15 AND MIR16 AND MIR17.

If the short half cycle of SCLK is extended due to an error correction on an instruction fetch (FCHB or FHCP), then the counter will be clocked again three FCLK cycles into the short half cycle. This allows the counter to pick up the corrected data. Note that there is still a full 250 nanoseconds left in the cycle after the counter clocks the data. (See Figure 3-13 and the paragraph of Clock Generation for more detail.)

The enable inputs and ripple carry outputs are configured in a non-standard manner so that the CTZ/CTZ4 look-ahead can be done with a minimum of logic. The look-ahead works only on what is currently in the counter, so that when the counter is loaded, CTZ and CTZ4 will not be valid the next cycle. DECCT indicates that the counter is to be decremented at the end of the current SC cycle. Holding the ENT- input of U28 (74-C) low allows the RC- output of the most significant counter (U48) to be interpreted as: counter bits 4 through 15 are all zeros. The RC- output of the least significant counter (U18) is externally gated with DECCT to generate the enable for the other three counters.

CT0 is exclusive ORed with DECCT to determine CT0 for the next cycle (NEXTCT0). Thus, by looking at the RC- output of U48, NEXTCT0, and CT1 through CT3, it can be determined if the lower four bits of the counter or the whole counter will be all zeros next cycle. The expressions for this are:

PCTZ4 = NEXTCT0 AND CT1_3Z
PCTZ = PCTZ4 AND CT4_15Z+

where CT1_3Z = (CT1 OR CT2 OR CT3)′
CT4_15Z+ = counter bits 4 through 15 are all zeros.

When CT is in the B-field (ECTB), the counter will be enabled onto the B-bus.

3.4.7.1 MRG Execution

MRG Execution involves counter bits 11 through 15. The decoding of the MRG instruction is done in PAL12L6 (U58, 44-B) according to the definition of the JTAB microorder. The PAL generates a signal of the form DBAS[memory access] for each memory access which might be initiated by JTAB: RDB, FCHB, CWRB. In the case of RDB, two signals are generated (DBASRDB0 and DBASRDB2) because this access requires more terms than can be handled by one PAL output. The PAL outputs are multiplexed (U57, 46-C) with the corresponding special or store signals in order to generate just one signal for each memory access, except for the RDB, which requires two. (RDB2 has no corresponding special). When JTAB is asserted, the MRG signals are selected; otherwise the specials are selected.

3.5 INTERFACE

3.5.1 BACKPLANE

Most of the interface between the processor and the backplane is handled on the upper processor card. The lower processor card, however, drives the backplane clocks and receives the Data Bus plus a few control signals. A summary of the backplane signals driven and received by PL along with the specifications for these signals are provided in Section X.

3.5.2 FRONTPLANE

The lower processor card interfaces to the upper processor card, the memory controller and writable control store over a high density connector called the frontplane. The frontplane is described in Section X of this manual.

3.6 DIAGNOSTICS

The major diagnostic feature which is provided by the hardware is the ability to diagnose the lower processor card without any other cards in the system, then just the two processor cards, and then both processor cards with the memory controller. This is necessary to be able to isolate faults down to a single card. The microcoded self-test diagnostics will stored be in firmware located in the processor on-card control store. The self-test is described in Section I of this document.

Because of the sequential nature of the self-test, the lower processor (PL) must be able to execute a subset of microcode by itself. This was accomplished by the functional division of the two processor cards; no one specific feature makes this possible. It does require that PL receives a minimum of signals from the upper processor (PU), all of which can be tied high, such that PL can operate with sufficient capability without PU. Most of the signals that PU drives to PL are active low so that they become inactive in the absence of PU. Two signals, however, are driven active high: FP_INT+ and FP_INTP+. These are also tied high on PL, such that in the absence of PU, the microcode always sees these interrrupt conditions asserted.

For debugging and diagnosing, the FCLK oscillator output can be disabled by tying FP_CKDIS- low and the CLOCK signal can be driven by an external source on FP_ECLK.

The control store address bus drivers can be disabled by typing FP CSADIS- low. This allows a test device to read a location in on-card control store (for example, to perform a checksum). A buffered version of the internal clock (FP_TESTSC-) is also provided on a test output so that the test device can read control store while the processor is operating. This is done by tying FP_FFRZ- input to the PU card low to freeze the clock while the test device is reading control store.

3.7 PARTS LOCATIONS

The parts locations for the lower processor are shown in Figure 3-14.

3.8 REPLACEABLE PARTS LIST

The replaceable parts list for the upper processor are listed in Table 3-7. Refer to Table 3-8 for the names and addresses of the manufacturers of the parts in the Manufacturer's Code List.

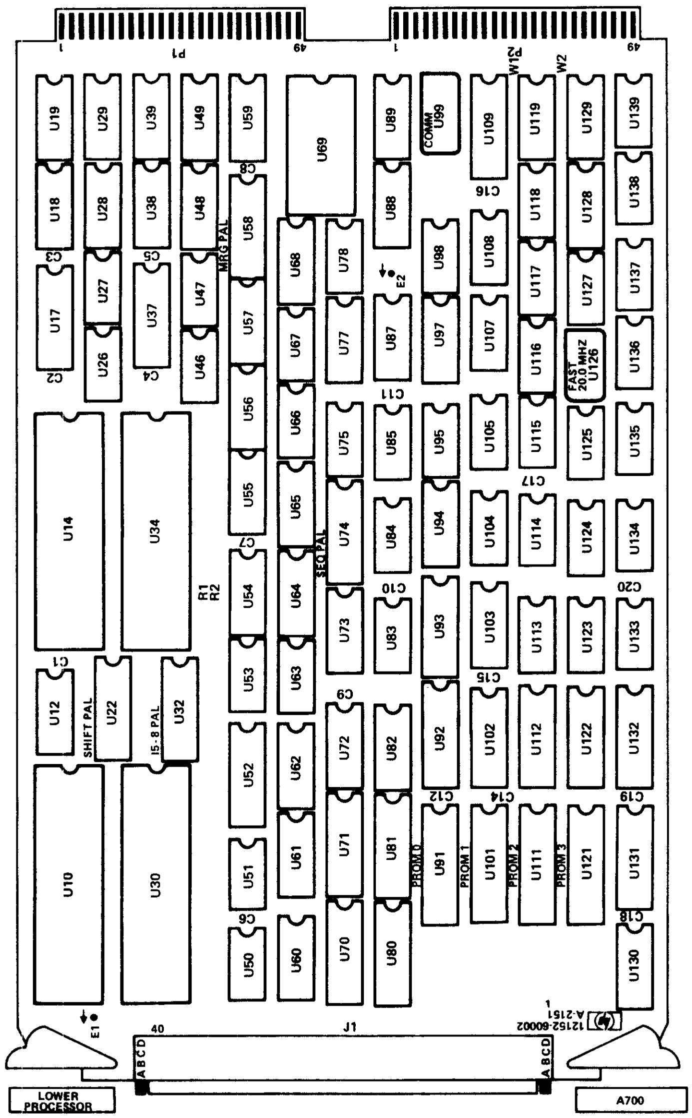


Figure 3-14. Lower Processor Parts Locations

Table 3-7. Lower Processor Replaceable Parts List

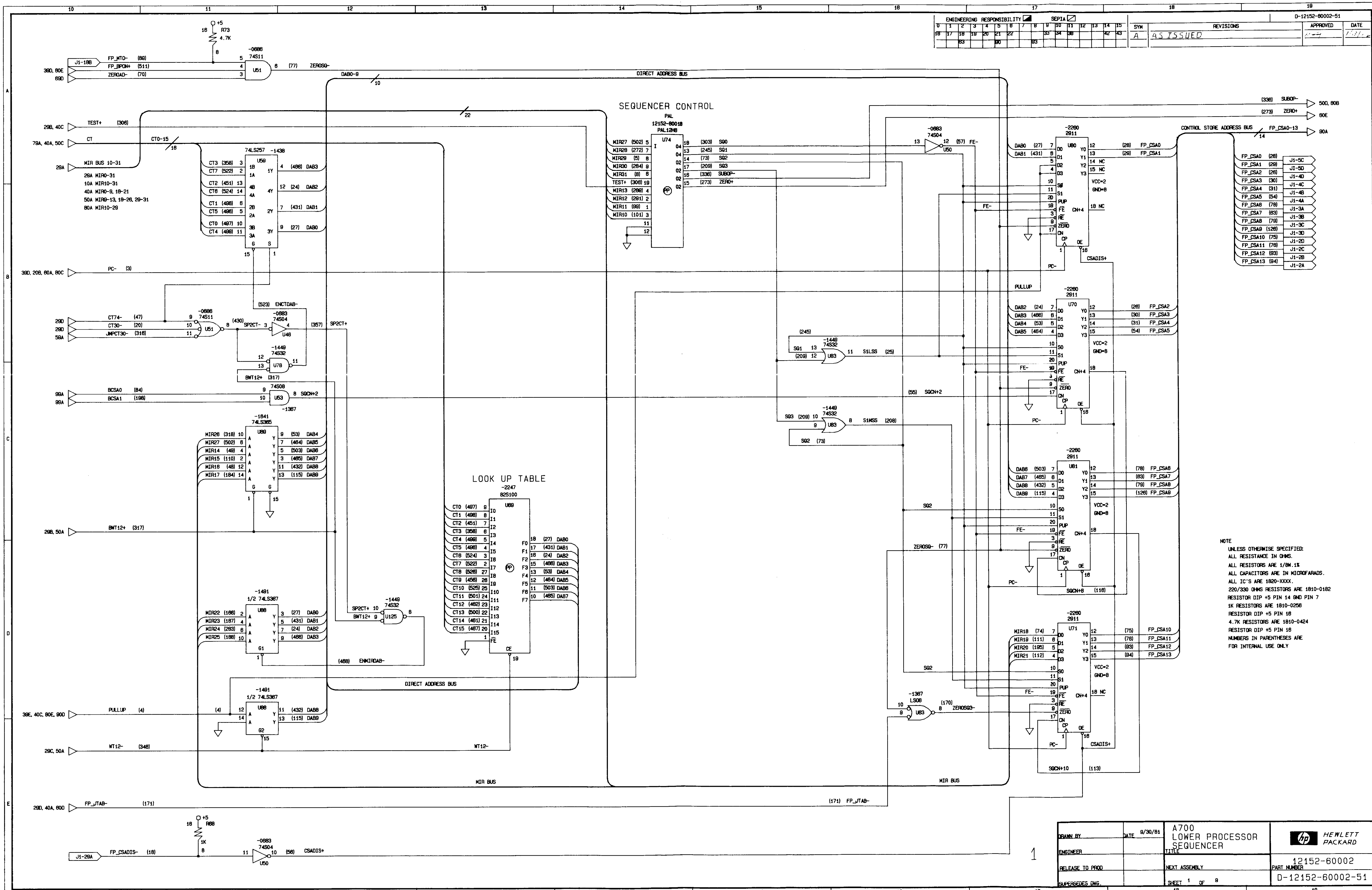
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	12152-60002	2	1	PCA-LOWER PROCESSOR PART OF 12152-60002	28480	12152-60002
	12152-64002	0	1	ASSEMBLY-AUTO INSERT	28480	12152-64002
C1	0160-4832	4	19	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0160-4832	4		CAPACITOR FXD .01UF +-10% 100VDC CER	28480	0160-4832
C3	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C4	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0160-4832	4		CAPACITOR FXD .01UF +-10% 100VDC CER	28480	0160-4832
C7	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C8	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C9	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C10	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C11	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C12	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C14	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C15	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C16	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C17	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C18	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C19	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C20	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
R1	0698-0082	7	1	RESISTOR 464 1% .125W F TC=0+-100	24546	C4-1/8-T0-4640-F
R2	0698-3444	1	1	RESISTOR 316 1% .125W F TC=0+-100	24546	C4-1/8-T0-316R-F
U10	1820-2377	9	4	IC-2903	28480	1820-2377
U12	1820-1305	1	1	IC GEN TTL S LOOK-AHD-CRY	01295	SN74S182N
U14	1820-2377	9		IC-2903	28480	1820-2377
U17	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U18	1820-1455	2	4	IC CNTR TTL S BIN UP/DOWN SYNCHRO	01295	SN74S169N
U19	1820-1077	4	6	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U22	12152-80016	0	1	IC-ROM, SHIFT PAL	28480	12152-80016
U26	1820-1367	5	5	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U27	1820-1449	4	7	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U28	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U28	1820-1455	2		IC CNTR TTL S BIN UP/DOWN SYNCHRO	01295	SN74S169N
U29	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U30	1820-2377	9		IC-2903	28480	1820-2377
U32	12152-80017	1	1	IC-ROM, 15-8 PAL	28480	12152-80017
U34	1820-2377	9		IC-2903	28480	1820-2377
U37	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U38	1820-1455	2		IC CNTR TTL S BIN UP/DOWN SYNCHRO	01295	SN74S169N
U39	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U46	1820-0683	6	6	IC INV TTL S HEX 1-INP	01295	SN74S04N
U47	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U48	1820-1455	2		IC CNTR TTL S BIN UP/DOWN SYNCHRO	01295	SN74S169N
U49	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U50	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U51	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U52	1820-1677	0	6	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U53	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U54	1820-0629	0	4	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U55	1820-1015	0	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U56	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U57	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U58	12152-80015	9	1	IC-ROM, MRG PAL	28480	12152-80015
U59	1820-1438	1	1	IC MUXR/DATA-SEL TTL LS 2-TO-1-LINE QUAD	01295	SN74LS257AN
U60	1820-1240	3	8	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U61	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U62	1820-1302	8	2	IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S251N
U63	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U64	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U65	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U66	1820-0691	6	2	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U67	1820-0691	6		IC GATE TTL S AND-OR-INV	01295	SN74S64N
U68	1810-0256	8	1	RESISTIVE NETWORK-DIP	01121	316A102
U69	12152-80022	8	1	IC-ROM, LUT	28480	12152-80022
U70	1820-2260	9	4	IC-2911	27014	IMD2911ANC
U71	1820-2260	9		IC-2911	27014	IMD2911ANC
U72	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U73	1810-0424	2	1	RESISTIVE NETWORK-DIP	11236	761-1-R4.7K
U74	12152-80018	2	1	IC-ROM, SEQ PAL	28480	12152-80018
U75	1820-0685	8	3	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U77	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U80	1820-2260	9		IC-2911	27014	IMD2911ANC
U81	1820-2260	9		IC-2911	27014	IMD2911ANC

Table 3-7. Lower Processor Replaceable Parts Lists (continued)

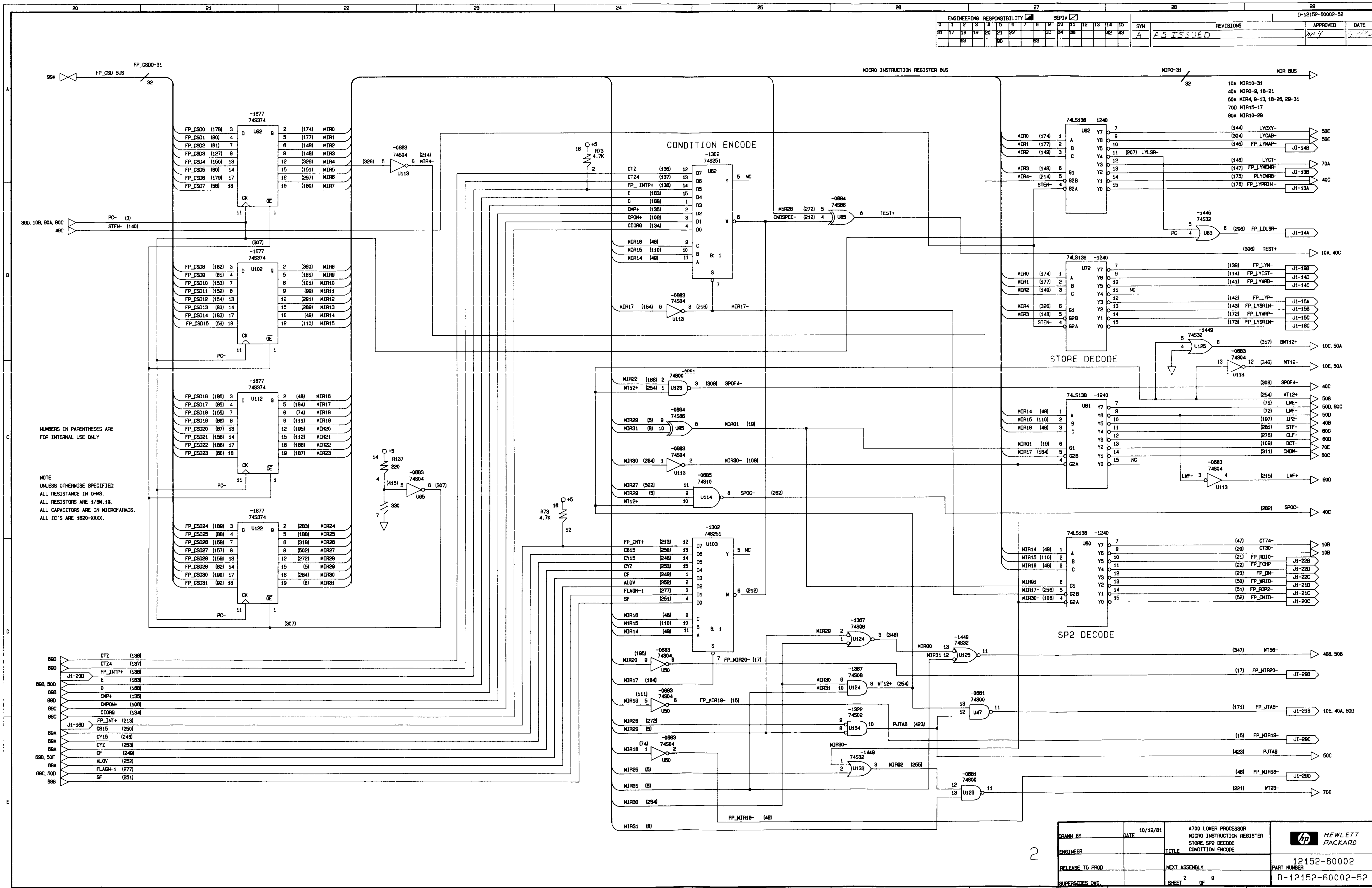
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U82	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U83	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U84	1820-0688	1	1	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U85	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U87	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U88	1820-1491	6	2	IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
U89	1820-1641	8	1	IC DRVR TTL LS BUS DRVR HEX 1-INP	01295	SN74LS365AN
U91	12152-80031	9	1	IC-ROM, CSRM0	28480	12152-80031
U92	1820-1677	0		IC FF TTL S D TYPE OCTL	01295	SN74S374N
U93	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U94	1820-1275	4	1	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U95	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U97	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U98	1820-1209	4	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS38N
U99	1813-0196	1	1	CRYSTAL OSCILLATOR 14.7456 MHZ	28480	1813-0196
U101	12152-80032	0	1	IC-ROM, CSRM1	28480	12152-80032
U102	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U103	1820-1302	8		IC MUXR/DATA-SEL TTL S 8-TO-1-LINE 8-INP	01295	SN74S251N
U104	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U105	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U107	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U108	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U109	1820-1633	8	1	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	12152-80033	1	1	IC-ROM, CSRM2	28480	12152-80033
U112	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U113	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U114	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U115	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U116	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U117	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U118	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U119	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U121	12152-80034	2	1	IC-ROM, CSRM3	28480	12152-80034
U122	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U123	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U124	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U125	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U126	1813-0285	9	1	OSCILLATOR 20 MHZ	28480	1813-0285
U127	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U128	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U129	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U130	1820-1491	6		IC BFR TTL LS NON-INV HEX 1-INP	01295	SN74LS367AN
U131	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U132	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U133	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U134	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U135	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U136	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U137	1810-0182	9	1	RESISTIVE NETWORK-DIP	28480	1810-0182
U138	1820-1450	7	1	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U139	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN

Table 3-8. Manufacturer's Code List

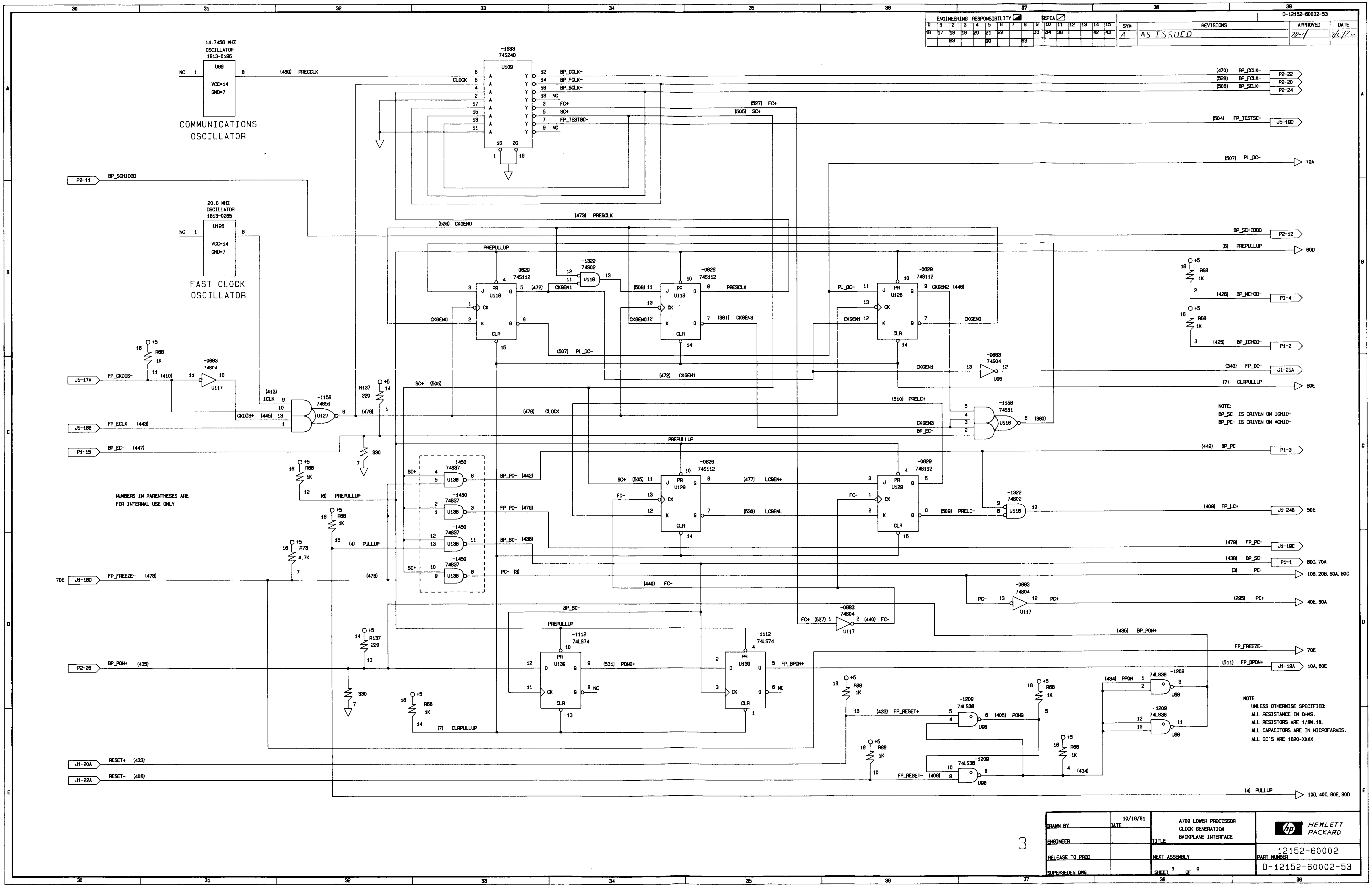
MFR NO.	MANUFACTURER NAME	ADDRESS		ZIP CODE
00000	ANY SATISFACTORY SUPPLIER			
01121	ALLEN-BRADLEY CO	MILWAUKEE	WI	53204
01295	TEXAS INSTR INC SEMICOND CMPNT DIV	DALLAS	TX	75222
03888	K D I PYROFILM CORP	WHIPPANY	NJ	07981
04713	MOTOROLA SEMICONDUCTOR PRODUCTS	PHOENIX	AZ	85008
07263	FAIRCHILD SEMICONDUCTOR DIV	MOUNTAIN VIEW	CA	94042
07910	TELEDYNE SEMICONDUCTOR	HAWTHORNE	CA	90250
11236	CTS OF BERNE INC	BERNE	IN	46711
11961	SEMICON INC	BURLINGTON	MA	01803
14936	GENERAL INSTR CORP SEMICON PROD GP	HICKSVILLE	NY	11802
19701	MEPCO/ELECTRA CORP	MINERAL WELLS	TX	76067
24546	CORNING GLASS WORKS (BRADFORD)	BRADFORD	PA	16701
27014	NATIONAL SEMICONDUCTOR CORP	SANTA CLARA	CA	95051
28480	HEWLETT-PACKARD CO CORPORATE HQ	PALO ALTO	CA	94304
32293	INTERSIL INC	CUPERTINO	CA	95014
34335	ADVANCED MICRO DEVICES INC	SUNNYVALE	CA	94086
34649	INTEL CORP	MOUNTAIN VIEW	CA	95051
50088	MOSTEK CORP	CARROLLTON	TX	75006
50364	MONOLITHIC MEMORIES INC	SUNNYVALE	CA	94086
56289	SPRAGUE ELECTRIC CO	NORTH ADAMS	MA	01247

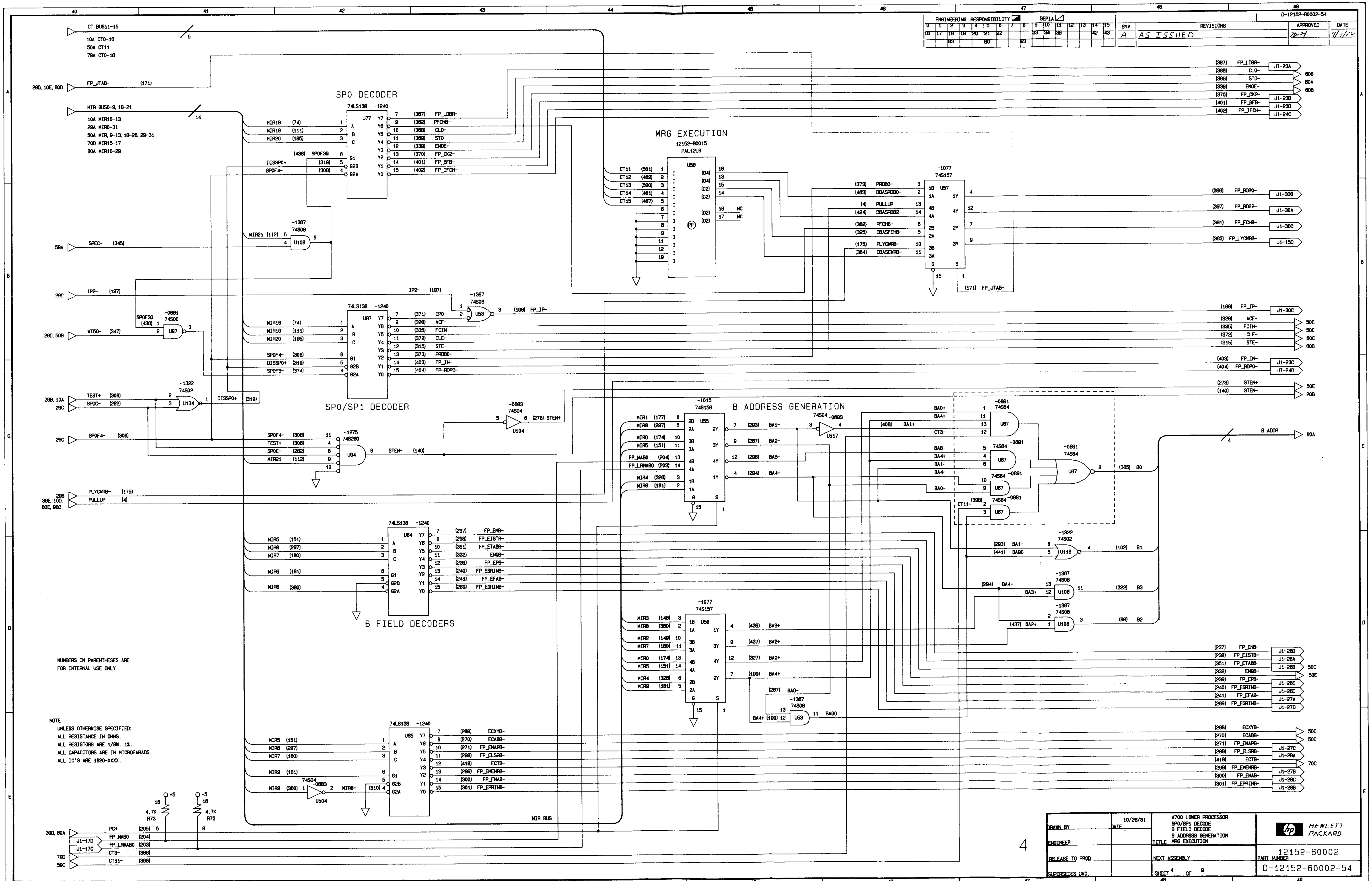


SEQUENCER CONTROL
PAL 12152-80018 PAL12H6
LOOK UP TABLE
-2247 82S100
DIRECT ADDRESS BUS
CONTROL STORE ADDRESS BUS
MIR BUS
MIR BUS 10-31
29A MIR0-31
10A MIR10-31
40A MIR0-9, 18-21
50A MIR0-13, 18-26, 29-31
80A MIR10-29
74LS257 -1438
74S11 -0886
74S04 -0683
74S32 -1449
74S08
74LS365 -1641
1/2 74LS367 -1491
LS08 -1367
-2260 2911
VCC=2
GND=8
ZEROSQ-
ENCTDAB-
SP2CT+
BWT12+
SQCN+2
ENMIRDAB-
PULLUP
WT12-
FP_UTAB-
FP_CSADIS-
CSADIS+
SUBOP-
ZERO+
FP_CSA0-13
NOTE
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W.1%
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
220/330 OHMS RESISTORS ARE 1810-0182
RESISTOR DIP +5 PIN 14 GND PIN 7
1K RESISTORS ARE 1810-0256
RESISTOR DIP +5 PIN 16
4.7K RESISTORS ARE 1810-0424
RESISTOR DIP +5 PIN 16
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
SYM
APPROVED
DATE
A
AS ISSUED
D-12152-60002-51
DRAWN BY
DATE 9/30/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
A700
LOWER PROCESSOR
SEQUENCER
TITLE
NEXT ASSEMBLY
SHEET 1 OF 8
HEWLETT PACKARD
12152-60002
PART NUMBER
D-12152-60002-51
1

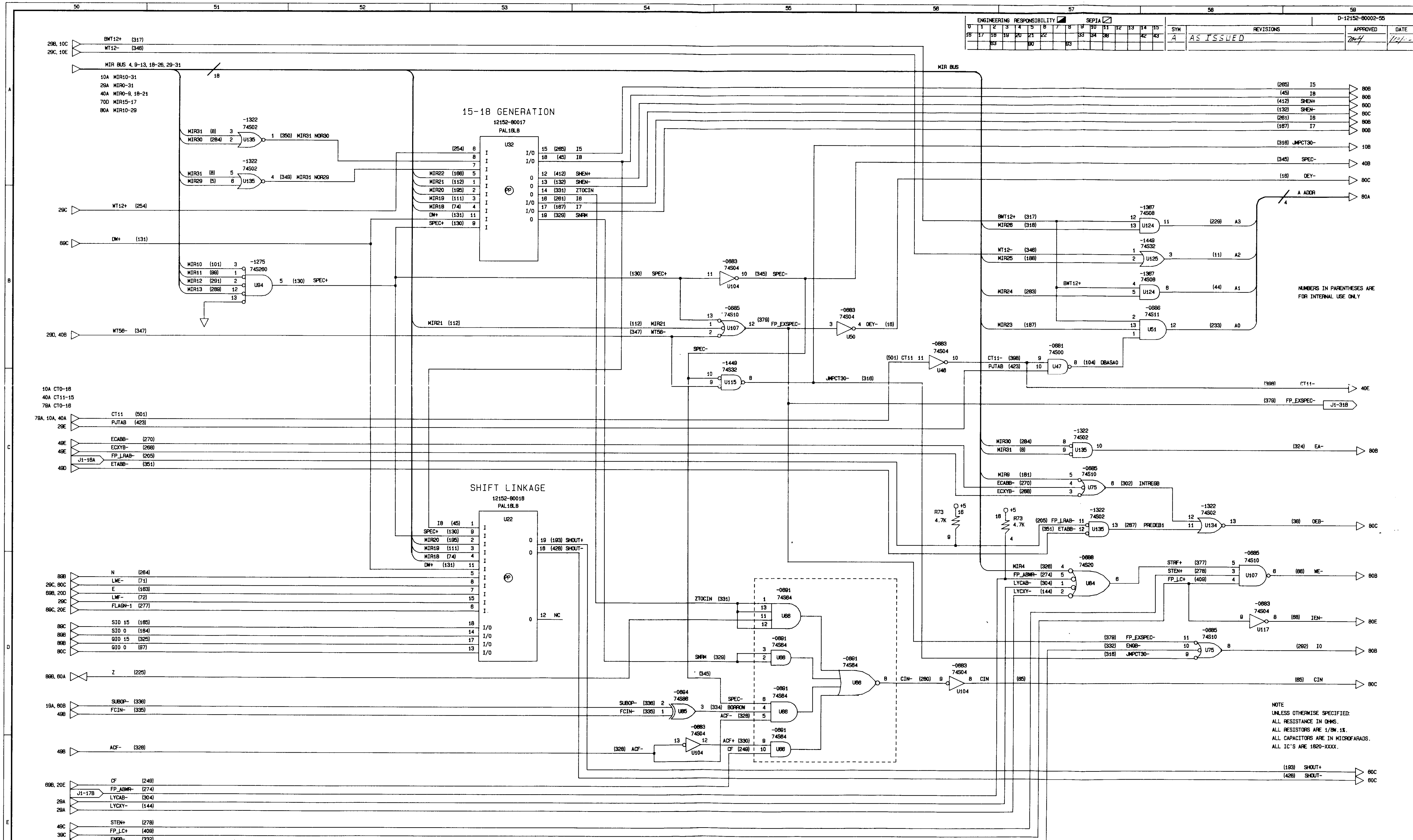


MICRO INSTRUCTION REGISTER BUS
MIR BUS
FP_CSD BUS
FP_CSD0-31
MIR0-31
10A MIR10-31
40A MIR0-8, 18-21
50A MIR4, 9-13, 18-26, 29-31
70D MIR15-17
80A MIR10-29
CONDITION ENCODE
STORE DECODE
SP2 DECODE
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
NOTE
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W.1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
APPROVED
DATE
A AS ISSUED
D-12152-60002-52
DRAWN BY
DATE 10/12/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
TITLE A700 LOWER PROCESSOR MICRO INSTRUCTION REGISTER STORE, SP2 DECODE CONDITION ENCODE
NEXT ASSEMBLY
SHEET 2 OF 9
HEWLETT PACKARD
12152-60002
PART NUMBER
D-12152-60002-52


A700 LOWER PROCESSOR
CLOCK GENERATION
BACKPLANE INTERFACE
HEWLETT PACKARD
12152-60002
D-12152-60002-53
COMMUNICATIONS OSCILLATOR
FAST CLOCK OSCILLATOR
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
NOTE: BP_SC- IS DRIVEN ON ICHID- BP_PC- IS DRIVEN ON MCHID-
NOTE UNLESS OTHERWISE SPECIFIED: ALL RESISTANCE IN OHMS. ALL RESISTORS ARE 1/8W.1%. ALL CAPACITORS ARE IN MICROFARADS. ALL IC'S ARE 1820-XXXX
ENGINEERING RESPONSIBILITY
REVISIONS
A AS ISSUED
DRAWN BY
DATE 10/16/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
TITLE
NEXT ASSEMBLY
SHEET 3 OF 8
PART NUMBER
3



SP0 DECODER
MRG EXECUTION
12152-80015
PAL12L6
SP0/SP1 DECODER
B ADDRESS GENERATION
B FIELD DECODERS
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY
NOTE
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
MIR BUS
B ADDR
A AS ISSUED
A700 LOWER PROCESSOR
SP0/SP1 DECODE
B FIELD DECODE
B ADDRSS GENERATION
MRG EXECUTION
10/28/81
HEWLETT PACKARD
12152-60002
D-12152-60002-54
SHEET 4 OF 8

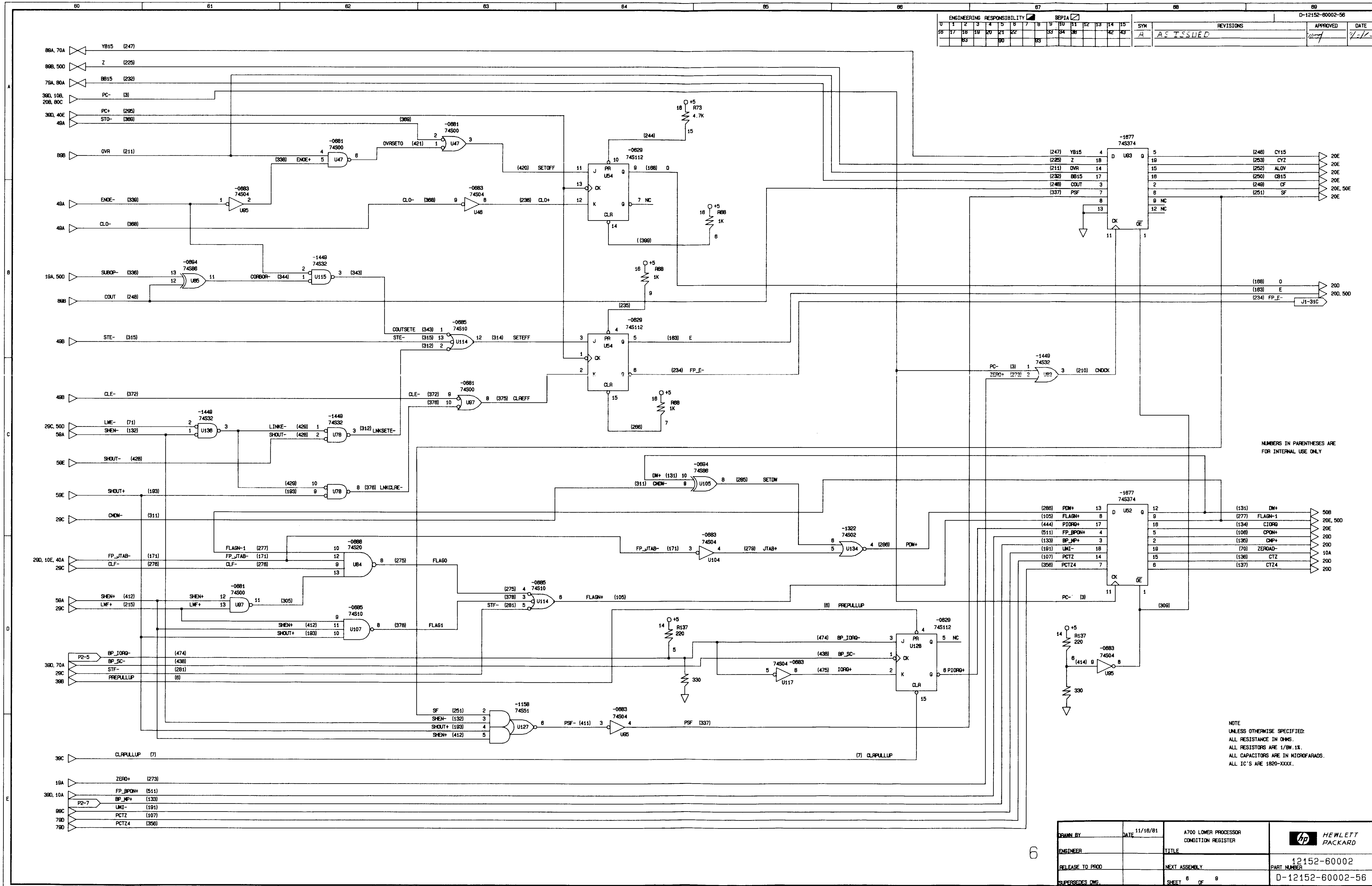


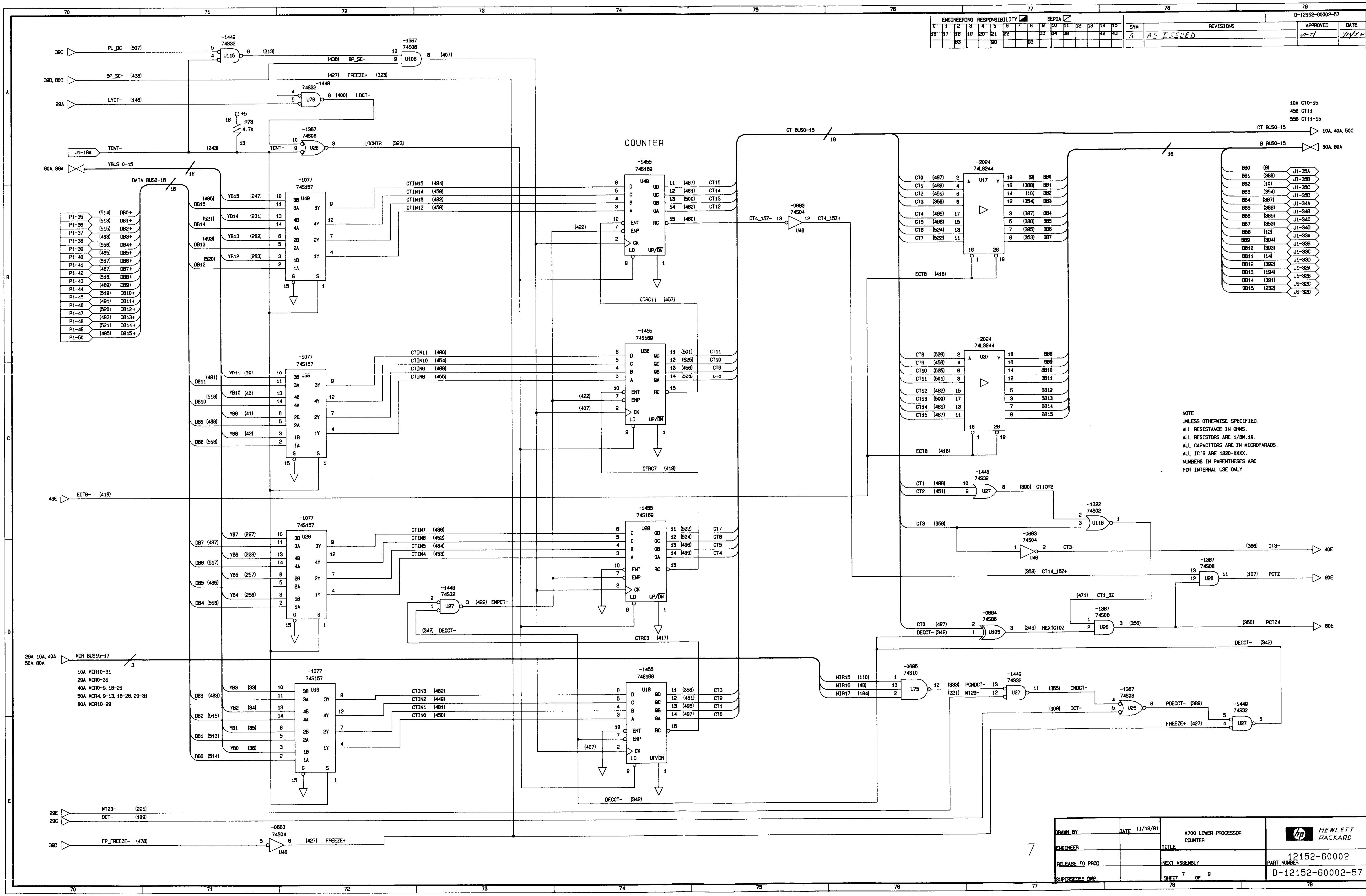
NOTE
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W,1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

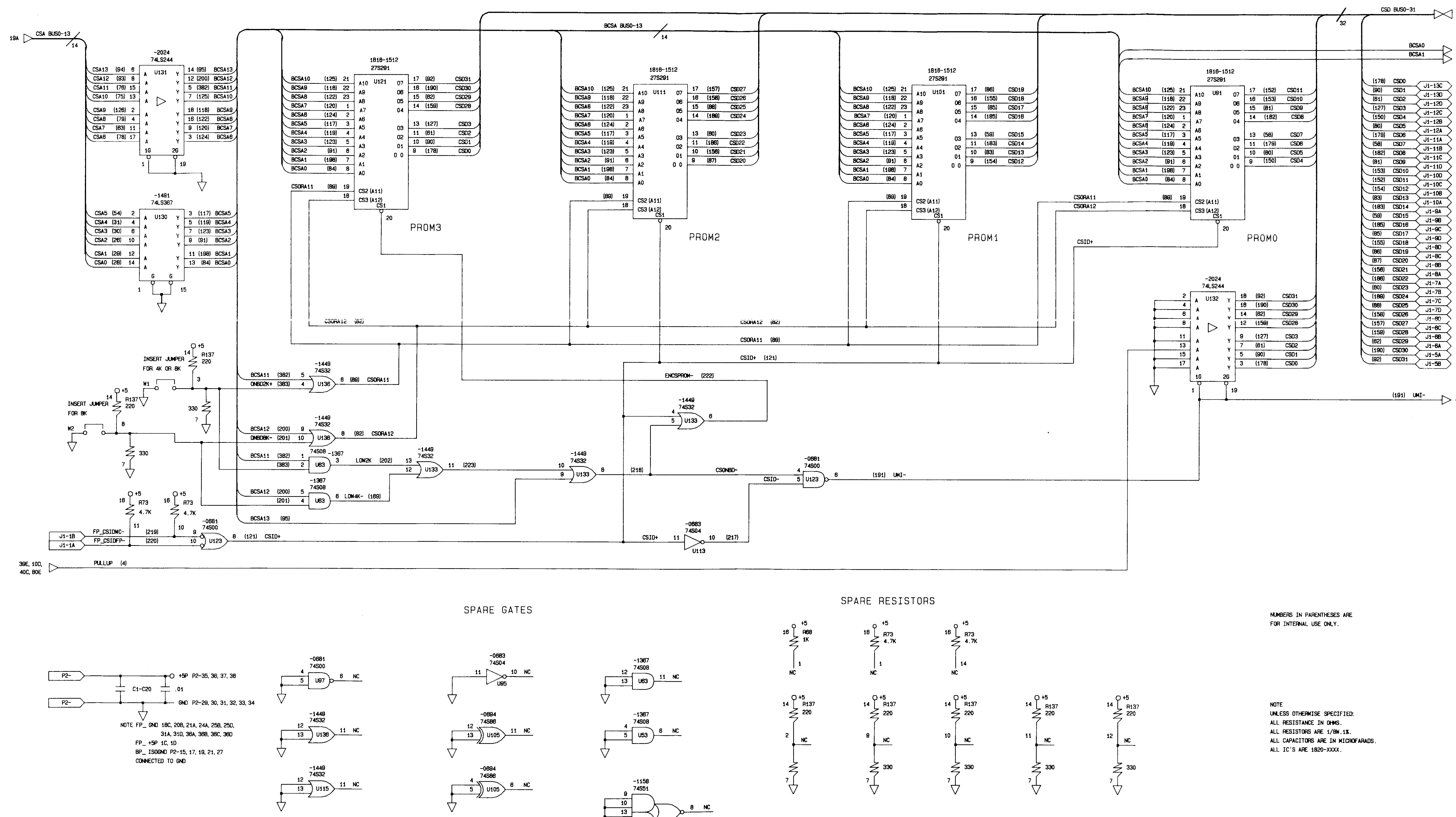
5

DRAWN BY	DATE 10/30/81	TITLE A700 LOWER PROCESSOR I5-I8 GENERATION SHIFT LINKAGE A ADDRESS GENERATION OEB, WE, IO, CIN, EA, IEN	HEWLETT PACKARD
ENGINEER			
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER 12152-60002
SUPERSEDES DWG.		SHEET 5 OF 9	D-12152-60002-55


D-12152-60002-56
ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
A
AS ISSUED
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
NOTE
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W.1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
DRAWN BY
DATE 11/18/81
A700 LOWER PROCESSOR
CONDITION REGISTER
ENGINEER
TITLE
RELEASE TO PROD
NEXT ASSEMBLY
SUPERSEDES DWG.
SHEET 6 OF 9
HEWLETT PACKARD
12152-60002
PART NUMBER
D-12152-60002-56
6


COUNTER
NOTE
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W.1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
A AS ISSUED
DRAWN BY
DATE 11/19/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
TITLE
A700 LOWER PROCESSOR
COUNTER
NEXT ASSEMBLY
SHEET 7 OF 9
HEWLETT PACKARD
12152-60002
PART NUMBER
D-12152-60002-57

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		

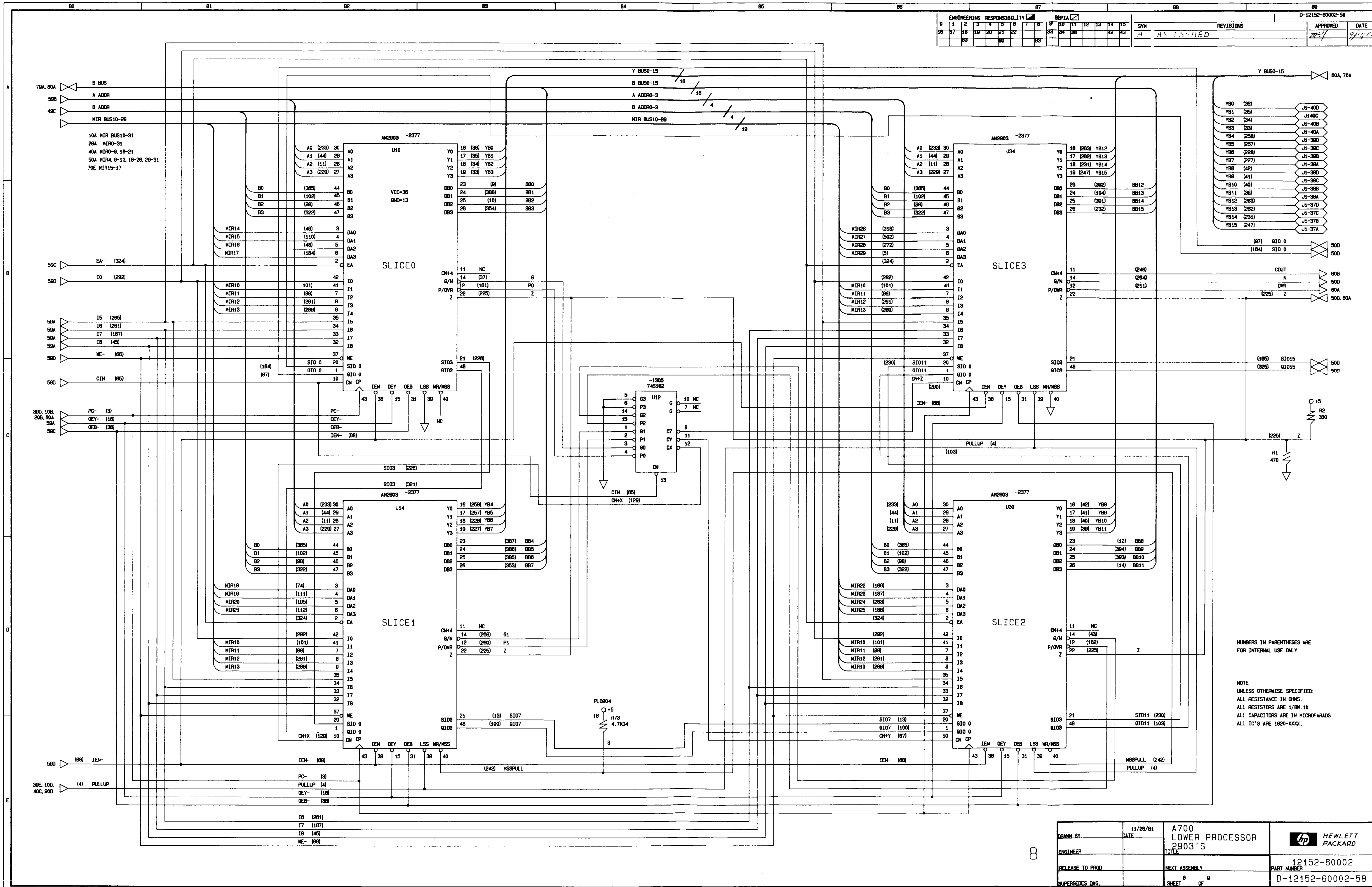


NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.

NOTE
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W.1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

DRAWN BY	DATE 11/30/81	TITLE A700 LOWER PROCESSOR CONTROL STORE SPARE GATES & RESISTORS
ENGINEER		
RELEASE TO PROD		NEXT ASSEMBLY
SUPERSEDES DWG.		SHEET 9 OF 9

HEWLETT PACKARD
PART NUMBER 12152-60002
D-12152-60002-59



NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

NOTE
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W.1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

8

DRAWN BY	11/26/81 DATE	A700 LOWER PROCESSOR 2903'S TITLE	HEWLETT PACKARD
ENGINEER			
RELEASE TO PROD		NEXT ASSEMBLY	12152-60002 PART NUMBER
SUPERSEDES DWG.		SHEET 8 OF 9	D-12152-60002-58

UPPER PROCESSOR CARD	SECTION IV

4.1 INTRODUCTION

This section covers the block diagram description and theory of operation of the upper processor card of the A700 computer. Figure 4-1 is a block diagram of the upper processor card which is shown in Figure 4-2.

The signal name conventions and abbreviations used in this section are the same as those used in Section II; therefore, refer to Section II, paragraph 2-2 for a list of them.

4.2 BLOCK DESCRIPTION

4.2.1 GENERAL ORGANIZATION

All of the memory and I/O microorders are executed on the upper processor, as are the external ALU operations. The upper card of the A700 processor can be divided into six functional blocks (Figure 4-1). These blocks are the following:

- External ALU Operations
- Register Files
- Address Generation Logic
- Interrupt System
- Time-Base Generator
- Memory and I/O State Machine

A simplified block diagram of the complete two card processor is provided in Section II, Figure 2-2.

The functional blocks are described first in a general manner and their logical operations (theory of operation) are described second in the paragraphs under 4.4.

4.2.2 EXTERNAL ALU OPERATIONS

There are eight functions, not performed in the ALU of the 2903 micromachine chips, and are described under External ALU operations, paragraph 4.3.1. These are microcoded by SPEC in the ALU field and microorders SWAP, SWZU, SWZL, ZUY, ZLY, ASG, SRG, or RL4 in the ALUS field.

When these functions are microcoded, the external ALU on the PU drives the Y-bus rather than the ALU on the PL. Control for these functions comes directly from the PL. ASG and SRG aid in the execution of the ASG and SRG microorders. RL4 does four-bit left rotate, and the other microorders do various byte swap and zero byte operations.

4.2.3 REGISTER FILES

Two register files of 16 registers each are provided for microcode use. One is the general-purpose (GRIN) register and is used by the base set and user microcode for storage of temporary results. The other is the privileged register file (PRIN) which is reserved for use by the base set.

4.2.4 MEMORY ACCESSING

A memory address is required any time the processor reads or writes a word to memory. The memory referencing microorders are RDP, RDPC, RDB, FCHP, FCHB, BFB, WRB, WRP, and CWRB.

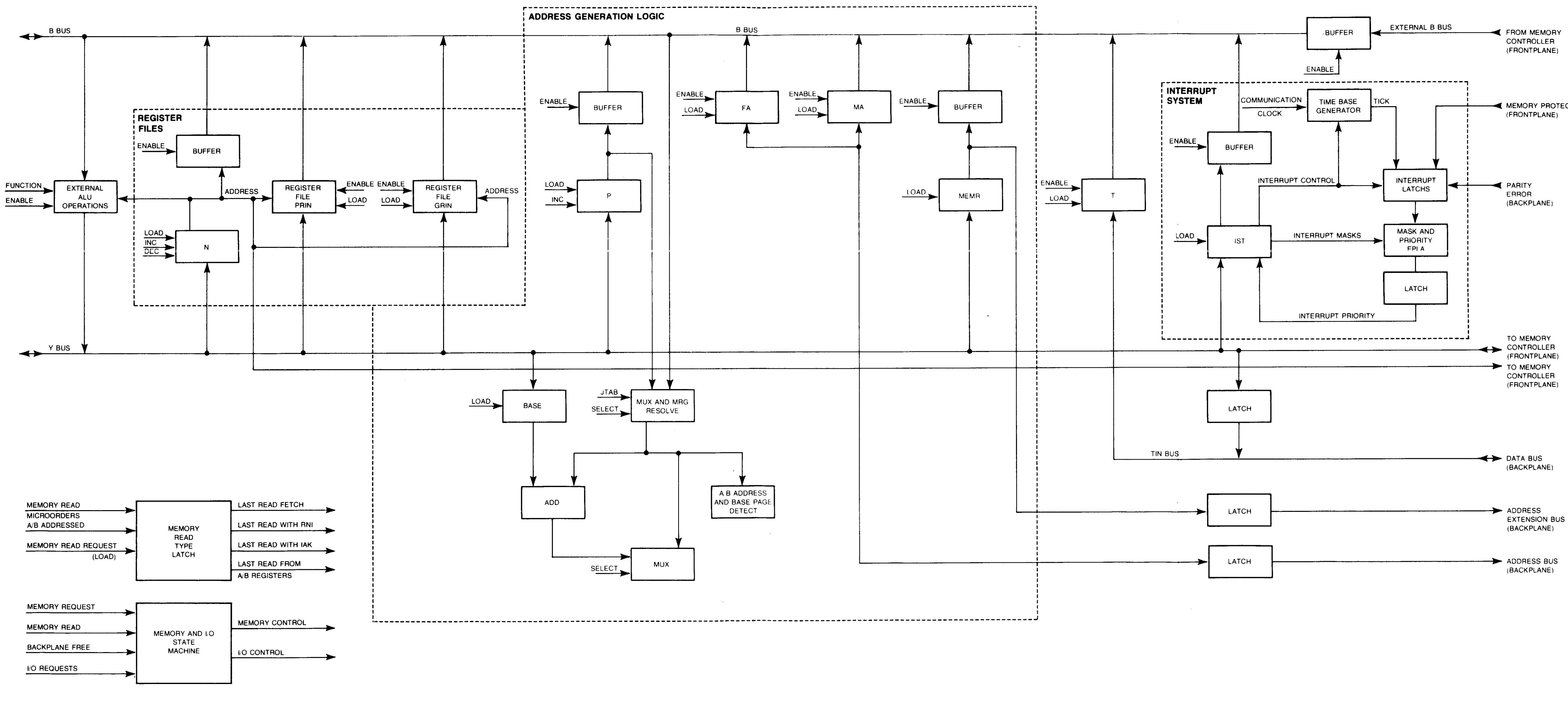


Figure 4-1. Upper Processor Card Block Diagram

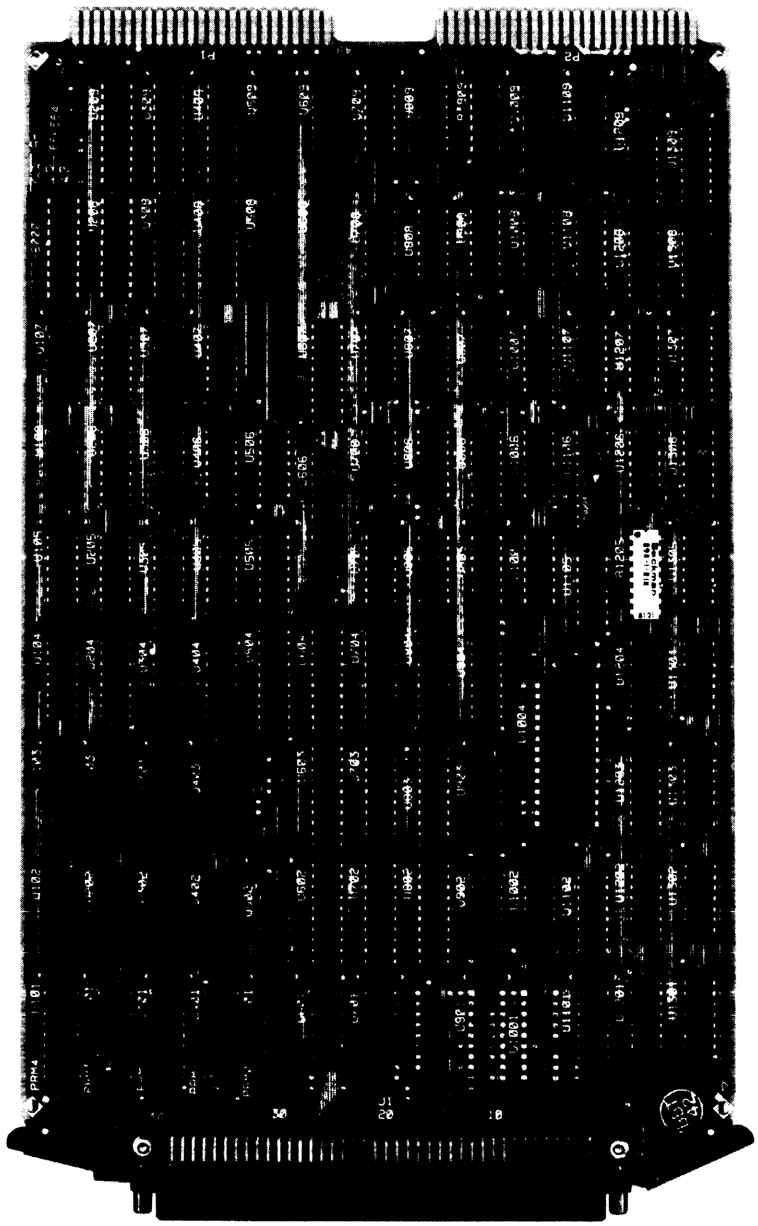


Figure 4-2. Upper Processor Card (12152-60001)

4.2.4.1 Direct Memory Access (DMA)

Direct memory access (DMA) by the I/O cards is usually given higher priority than any memory access request from the processor. If DMA is in process or pending, the next processor memory access is withheld until the current series of DMA is completed. The processor can momentarily suspend this hierarchy if it has denied access to memory for 32 consecutive DMA memory accesses. This arrangement grants DMA nearly the full memory access bandwidth yet permits the processor to guarantee reasonable interrupt latency in DMA intensive environments.

When there are no active or pending DMA requests, the processor initiates its memory request to the memory card. In a memory read transaction, the addressed data is returned at the end of the memory cycle. In the case of a memory write request, the data to be stored is sent to the memory card at the same time as the address at the start of the memory cycle. A memory read request is distinguished from a write request by the sense of the write enable bit (WE-) sent to the memory card.

4.2.4.2 Address Generation Logic

A memory address consists of a 15-bit logical address, a five-bit map number, and the MEMDIS bit which forces boot memory to be used. The entire memory address is latched at the time that the memory reference microorder is executed. When the backplane is not busy, the memory reference occurs. The map number is taken from MEMR register (bits 0-4), as is MEMDIS (bit 5). When a memory write occurs the data to be written and the address are latched at the same time.

RDP, RDPC, FCHP, and WRP specify that the logical address originates in the P-register. Otherwise, the address originates on the B-bus. This address is then transformed by the address generation logic to form the logical address that is latched for sending over the backplane.

During a JTAB line execution, the address source is MRG resolved (the MRG instruction presented is changed to an address). If base relative mode is enabled (BASE bit 15 is a one) and the address source (after MRG resolution) is in the base page, the base register is added to the address.

If base-relative mode is enabled and the microorder is either FCHB, FCHP, BFB, or RDPC, and the address source is not in the base page, the low order bit of the map number is forced to be a one. Forcing the low-order bit of the map number to one determines that it is a code-map reference. If the low-order bit of the map number is a zero, it is a data-map reference and the microorder is either RDB, WRB, WRP, or CWRB.

The final logical address is always latched in the MA register. FCHP and FCHB cause the final logical address to be latched in the FA register also.

Data from a memory read which does not address A- or B-registers is returned in the T-register. The T-register is not modified except by a processor memory read.

4.2.5 INTERRUPT SYSTEM.

There are two types of interrupt requests in the HP 1000 A700 Processor. System level interrupts may be generated by the processor card to handle system level problems such as power fail and parity error. I/O interrupts may be requested by the individual I/O cards to cause processing to service the needs of that I/O channel. Interrupts at the micromachine level (INTF pending) are described under interrupt system theory of operation, paragraph 4.3.4.

4.2.5.1 System Level and I/O Interrupts

The upper processor card receives all system level and I/O interrupt requests and determines which interrupt will be serviced. Three basic levels of importance define the relative priority of interrupt requests. A level one interrupt request has no restrictions in obtaining interrupt service. Level two and level three requests are collectively enabled/disabled by a STC/CLC 4, the interrupt inhibit flag. Level three interrupt requests may be further enabled/disabled by a STF/CLF 0, the interrupt system flag. In addition, interrupt masks are available to mask off any or all of the level three interrupt requests. A hardware signal from the processor called Temporarily Disable Interrupt (PU_TDI-) will prevent one of the level two and all level three requests from interrupting following certain instructions and slave mode transfers.

4.2.5.2 Micromachine Interrupt Level

The interrupt micromachine hardware synchronizes and qualifies the interrupt sources. The highest priority interrupt is determined and the INTP condition is generated if an interrupt is pending. The INTF condition is generated when a fetch is held off by the hardware due to a pending interrupt.

The IST-register is the interface between the interrupt system and the microcode. It contains those interrupt bits which are only set by the microcode and all the interrupt mask and enable bits. It is used to read the output of the priority encoder and to set or clear the interrupt latches.

4.2.6 TIME BASE GENERATOR

The time-base generator circuitry provides a one PC (Processor Clock) cycle long pulse to the interrupt system every 10.00 milliseconds. If the previous pulse has not been acknowleged, a microcode time out is generated. The time-base generator can be turned off, and its first pulse will be generated 10 milliseconds after it is turned back on.

previous pulse has not been acknowleged, a microcode time out is generated. The time-base generator can be turned off, and its first pulse will be generated 10 milliseconds after it is turned back on.

4.2.7 MEMORY AND I/O STATE MACHINE

The Memory and I/O (MIO) state machine of the processor generates control signals for the memory address logic. One pending memory reference can be held in the address and data latches if the backplane is busy. The memory state machine determines when backplane control signals are asserted and when address and data are latched. The I/O microorders are WRIO and RDIO. The MIO state machine controls the backplane signals to perform an I/O handshake when one of these microorders is executed. The following three figures show the signal timing for memory and I/O backplane signals initiated by the MIO state machine. Figure 4-3 shows memory read, Figure 4-4 shows memory write, and Figure 4-5 shows I/O instruction broadcast.

4.2.7.1 Freeze Logic

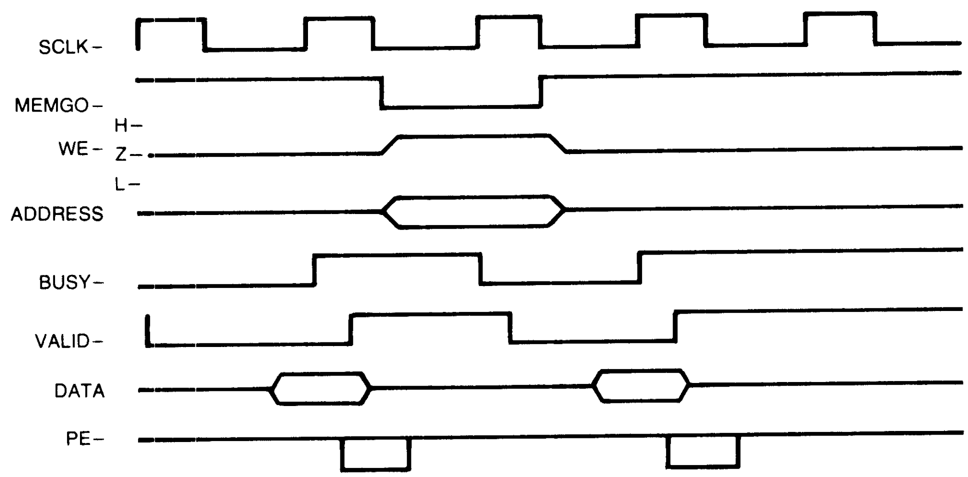
If a memory or I/O access is attempted and the address and data latches have useful information in them the processor clock is frozen until the latches are empty. A freeze can also occur if the microcode tries to read the T-register and data is not yet back from the most recent memory read, or if the processor tries to access the map RAMs and the memory controller is using them for a memory cycle. The freeze logic generates a clock freeze signal using the microorder inputs and status signals from the memory and I/O state machine.

4.3 THEORY OF OPERATION

The A700 Computer upper processor card theory of operation is covered in the following paragraphs. The reference diagrams for this material are the block diagram of Figure 4-1 and the schematic at the rear of this section of the manual. The integrated circuit packages (chips) are referenced by U-numbers and schematic locations. For example, U69 (12-C) means chip U69 on schematic sheet no. 1 is located by coordinates 12 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc. and on sheet no. 2 it is numbered 20, 21, etc.

4.3.1 EXTERNAL ALU OPERATIONS

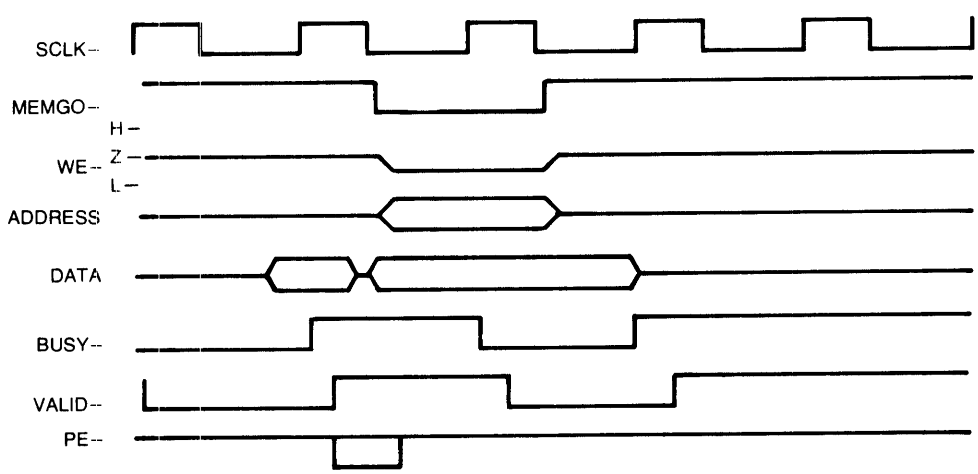
The external ALU consists of five 1k by four ROMs at chip locations U101, U201, U301, U401, and U501 (see parts locations diagram Figure 4-11). The transformation from the B-bus to the Y-bus performed by each of the external ALU operations is described in Table 4-1.



NOTE: MEMGO– occurs after completion of the current DMA cycle. WE– is high during MEMGO–.

8200-92

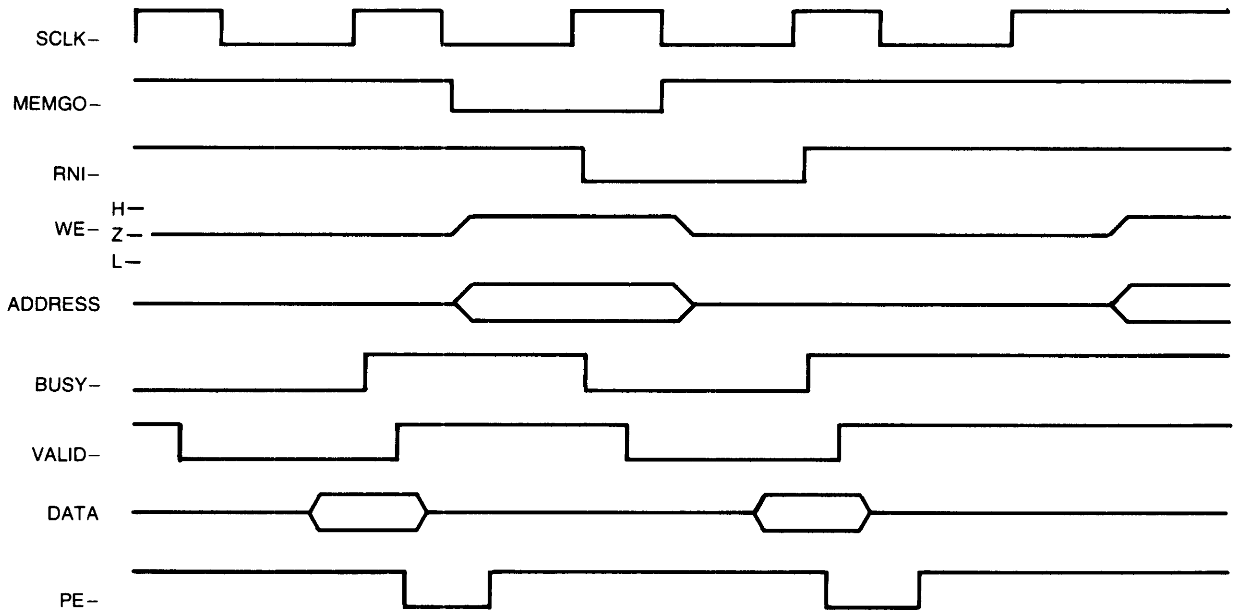
Figure 4-3. Backplane Signals for Memory Read



NOTE: MEMGO– occurs after completion of the current DMA cycle. WE– is asserted during MEMGO–.

8200-93

Figure 4-4. Backplane Signals for Memory Write



NOTE: MEMGO- occurs after completion of the current DMA cycle. WE- is asserted before and during VALID-.

8200-94

Figure 4-5. I/O Instruction Broadcast

The external ALU conditions are the following:

SRG: The state of bit 10 (BB10) of the B-bus when SRG is coded provides one of the following transformations:

BB10 is zero, SRG0 is selected (an SRG instruction);
BB10 is one, SRG1 is selected (an IOG instruction).

ASG: If SETE (SET E) bit is high (1), the microcode will set the E bit. The new E value is based on the old E value and the CLE, CCE, CME bits (bits 6 and 7) in the macroinstruction according to the equation:

B7 * B6 + E′ * B7 + E * B7′ * B6′

where E, B6, and B7 are the old values and E′, B6′, and B7′ are the new values.

Table 4-1. Transformation from the B-Bus to the Y-Bus

MICROORDER	swap	swzu	swz1	zuy	z1y	r14	srg0	asg	srg1
Y-Bus Gets 0	B8	B8	0	B0	0	B12	B8	B8	B0
1	B9	B9	0	B1	0	B13	B9	SKP	B1
2	B10	B10	0	B2	0	B14	B6	SETE	B2
3	B11	B11	0	B3	0	B15	B7	B9	B3
4	B12	B12	0	B4	0	B0	B0	B0	B8
5	B13	B13	0	B5	0	B1	B1	B1	B6 and (B8 OR B9)
6	B14	B14	0	B6	0	B2	B2	B2	B7
7	B15	B15	0	B7	0	B3	B4	B3	0
8	B0	0	B0	0	B8	B4	0	0	0
9	B1	0	B1	0	B9	B5	0	0	0
10	B2	0	B2	0	B10	B6	0	0	0
11	B3	0	B3	0	B11	B7	B11	B11	B11
12	B4	0	B4	0	B12	B8	0	0	0
13	B5	0	B5	0	B13	B9	0	0	0
14	B6	0	B6	0	B14	B10	B5	0	B6
15	B7	0	B7	0	B15	B11	B3	0	B9

Notes: The B bit (e.g., B10) is the B-bus bit to be passed.
0 means make that bit zero (undefined for the user).
SKP and SETE are conditions.

The SKP bit is entirely coded by U301 (103D) which is only enabled for the ASG operation by a three-input NAND gate U1204 (103-E). SKP high (1) indicates that a skip will definitely occur. It does not include the effects of INA and SZA in the macroinstruction. If an INA or SZA is included in the instruction the microcode must decide whether to skip (including the effects of RSS on SZA). SKP is a function of the B-bus bits (which have the ASG instruction to be transformed), the old E bit, and N0 and N1 which are bits of the N (index) register. Prior to executing the ASG special the microcode loads these bits with bits 0 and 15 of the A= or B-register with microinstruction N := RL1(CAB)

The expressions for SKP are the following:

```
B0'*[ B5 * E' +
    B4 * ( B9' * B8 + N0' * B9' * B8' + N0 * B9 * B8') +
    B3 * ( B9' * B8 + N1' * B9' * B8' + N1 * B9 * B8') ] +
B0 *[ B5 * E  +
    B4 * B3'* ( B9 * B8 + N0 * B9'* B8'+ N0'* B9 * B8 ) +
    B4'* B3 * ( B9 * B8 + N1 * B9'* B8'+ N1'* B9 * B8') +
    B4 * B3 * ( B9 * B8 + N0 * N1 * B9'* B8'+ N0'* N1'* B9 * B8') +
    B5'* B4'* B3' *B1']
```

The external ALU operations are implemented with five 1k-by-4 ROMs (type 7644-5). Each ROM determines four bits of the Y-bus. These ROMs appear on sheet no. 10 of the schematic. Four of the ROMs are enabled to drive the Y-bus whenever FP_EXSPEC- is asserted. The MIR bits (FP_MIR18 to FP_MIR20) originate in the SPO-Field and indicate which operation is to be performed. The Y-bus outputs are distributed among the ROMs so that each ROM only needs ten inputs. ROM inputs and outputs are given below:

ROM INPUTS				
U501	U401	U301	U201	U101
PROM0	PROM1	PROM2	PROM3	PROM4
MIR20	MIR20	BB0	MIR20	MIR20
MIR19	MIR19	BB1	MIR19	MIR19
MIR18	MIR18	BB3	MIR18	MIR18
BB2	BB1	BB4	BB0	BB3
BB5	BB5	BB5	BB4	BB4
BB6	BB9	BB8	BB8	BB7
BB7	BB13	BB9	BB12	BB9
BB10	BB6	N0	BB10	BB11
BB14	BB8	N1		BB15
OLDE	BB10	OLDE		BB10
ROM OUTPUTS				
YB2	YB1	YB1	YB0	YB3
YB6	YB5	YB5	YB4	YB7
YB10	YB9	YB9	YB8	YB11
YB14	YB13	YB13	YB12	YB15

ROM2 is enabled if the operation is an ASG. That is if the MIR bits are all ones. The additional ROM is needed because the ASG SKIP condition needs ten inputs all by itself. The other external operations for these four bits are performed in ROM1, which is enabled if the operation is not an ASG.

4.3.2 REGISTER FILES

The register files is included on sheet no. 3 of the upper processor schematics located at the end this section. Each register file consists of four 85S68 edge-triggered RAMs. The PRIN register file is U102, U103, U202, and U203. GRIN is U302, U303, U402, and U403.

These RAMs have 16-word by four-bit organization with an internal transparent latch to allow reading and writing in the same cycle. The tri-state ouputs come directly from the internal transparent latch which is transparent when the OS' input is low.

The latch holds the previously read data when OS′ is high. The outputs of the RAMs are enabled to the B-bus by the FP_EPRINB- and FP_EGRINB- signals which feed directly to the OD input of the RAMs. When OD is low the RAMs drive the B-bus.

The address to the RAMs comes from the N-register. The contents of the addressed location is always read and latched in the internal latch at the end of the short half-cycle. OS′ is driven with an inverted version of the processor clock (PU_BPC1). The latch is thus open during the short half-cycle (first half-cycle) and closed during the long half-cycle. A write is signaled by FP_LYPRIN- and FP_LYGRIN-, and occurs during the long half-cycle with data coming from the Y-bus. These signals feed the WE′ inputs directly. These parts are edge triggered so the data is written when a rising edge occurs on the clock input while WE′ is low. Data is clocked into the register file by the rising edge of PC- (the processor clock).

The N register is a four-bit counter shown on sheet no. 2 of the schematic. It consists of a 74S169 four-bit up/down counter at U502 (25-C) and two 74LS244 buffers at U602 (28-C) and U603 (28-D) to drive the B-bus. One of the buffers is shared with MEMR. MEMR is an eight-bit register, so the upper eight bits of the B-bus are driven by the same buffer for both the N and MEMR registers. 12 bits of internal status are available on the other 12 bits of the N-register.

The buffers are enabled with the FP_ENB- signal. The buffer for the high order eight bits is also enabled with the FP_EMEMRB- signal. The special DN (decrement N) causes the signal FP_DN-. DN- goes directly to the UP/DN′ input and the counter is enabled if IN- or DN- is low. The counter is loaded from the Y-bus with the signal FP_LYN-.

<u>N-Register Status Bits</u>

0	N0	
1	N1	
2	N2	
3	N3	
4	UNUSED	
5	UNUSED	
6	UNUSED	
7	UNUSED	
15	PU_TDI	1 if interrupts held off
14	PU_PFWFF-	0 if power fail warning asserted on backplane
13	PU_IMLOST	1 if MLOST asserted on backplane
12	PU_MTO	1 if microcode timeout occurred
11	PU_ABFTCH-	0 if last fetch was A/B addressed
10	PU_PEINT	1 if parity error interrupt pending
9	PU_SLAVEFF-	0 if slave asserted on the backplane
8	UNUSED	
8	UNUSED	

4.3.3 TIME-BASE GENERATOR AND MICROCODE TIME-OUT

When reading the time-base generator (TBG) theory of operation, see sheet no. 5 of the schematic diagrams. In operation, the TBG generates a pulse with a 10 millisecond period with a pulse width equal to one PC- cycle on the signal line PU_TICK-. This pulse sets the TBGT flip-flop which is the source of the TBGT interrupt.

If the TBGT flip-flop is already set, the tick (clock pulse) sets the MTO flip-flop instead, indicating that a micocode time out has occurred. The tick also asserts the FP_MTO- line to force the sequencer to execute the next instruction from location zero. The TBGT flip-flop and MTO flip-flop are on sheet no. 4 of the schematic.

The input to the TBG is the communications clock signal that is to divided down to the required clock frequencies. The communications clock is divided by 2exp14 with type 74LS393 8-bit counters U1005 (51-D) and U1105 (52-D), then divided by nine with a type 74LS161 four-bit counter U1108 (53-D) to provide a signal with a 10 millisecond period. The output of U1108 is a signal (TBGD5) having a 10.00 millisecond period and a width of 1.111 millisecond.

The rising edge of TBGD5 clocks a "1" into the TBGQ6 flip-flop U1208 (55-D). The output of this flip-flop is clocked twice by PC- into the TBGQ7 and TICK flip-flops U1208 and U1308 (56-D and 58-D) to synchronize it with PC-. TICK- then clears the TBGQ6 and TBGQ7 flip-flops so that TICK becomes a pulse equalling one cycle of PC-.

When the TBG is turned off, U1005, U1105, and U1108 are held clear so that when TBG is turned back on, 10 milliseconds will go by before the first interrupt. The MTO flip-flop can be cleared with a write to the IST.

4.3.4 INTERRUPT SYSTEM

When reading the theory of operation of the interrupt system, see sheet no. 4 of the schematic diagrams. The interrupt system latches, masks and prioritizes the interrupt inputs. It generates two conditions: INTP and INTF. INTP indicates to the microcode that an interrupt is pending and microroutines should check INTP if they are to be interruptable. The INTF condition corresponds to the hardware signal PU_INT.

Every microroutine must end with a fetch microorder (FCHB or FCHP). If INTP is true when the fetch microorder is executed the fetch will not occur and the INT signal is set. Also, INT is set if INTP is false and the fetch is A/B addressed (no backplane memory cycle occurs). The INTF condition is tested immediately before any microinstruction line with a JTAB on it.

If INT is set, the interrupt service microcode must be executed before the JTAB subroutine since there is not a valid instruction in the counter.

The masking and prioritization of the interrupt sources and the generation of INTP and INT are done by U1004 (47-C), a Signetics 82S100 Field Programmable Logic Array (FPLA). The FPLA coding is provided in Figure 4-6. Refer to the manufacture's literature on the FPLA for a detailed explanation.

4.3.4.1 Interrupt Status

The interrupt status register (IST) is the interface between the microcode and the interrupt system. The bits of the IST, referenced by microorder IST, are the following:

0-3	interrupt control
4	PEE
5	PFWE
6	MRGIE
7	MIM
8	INTRQM
9	FLTO
10	TBGON
11	PS-
12	MP-
13	SCHOD-
14	CRS
15	TBGF

The upper 12 bits of the IST are contained in U902 and U903 (42-C and 42-D), which are 74LS378 type latches. Two 74LS244 type buffers, U803 and U802 (43-D and 43-C), enable the IST onto the B-bus when the EISTB- signal is asserted. The low four bits to drive the B-bus come from U1102 (48-B), a type 74LS174 latch, which buffers the output of U1004 (47-C). These four bits indicate the highest priority interrupt pending. When LYIST- is asserted to load the IST, the low four bits of the Y-bus are enabled through U1002 (42-B), a 3-to-8 decoder (74S138), to generate set and clear signals to each of the interrupt-latch flip-flops. This path is one of the worst-case setup time paths on the Y-bus. The status bits are defined as follows:

PEE is parity enable which is used with the parity error interrupt source.

PFWE is the enable bit for power-fail interrupts which is sent directly into U1004.

MRGIE is provided to allow base page links in a future development. It is not used and should always be zero.

MIM is the master interrupt mask which disables all interrupts when high.

INTRQM is the interrupt request enable mask which masks I/O interrupts when high.

ROW	PRODUCT TERMS (AND): INPUT LINES*																OUTPUT FUNC. (OR)**							
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	H 7	H 6	L 5	H 4	L 3	L 2	L 1	L 0
0						L					L							A	A					
1					L						L							A	A					
2	H						L				L							A	A					
3											L			L				A	A					
4	H									H	L		L					A	A					
5	H										L	H						A	A					
6											L					H		A	A					
7	H		H								L				H			A	A					
8						L		H			L						A							
9					L			H			L						A							
10	H						L	H			L						A							
11								H			L			L			A							
12	H							H		H	L		L				A							
13	H							H			L	H					A							
14								H			L					H	A							
15	H		H					H			L				H		A							
16		L						H			L						A							
17									L															A
18																						A	A	
19					L				H														A	
20	H						L		H												A	A	A	
21									H														A	
22	H				H				H	H			L	H								A		
23					H				H					H		H						A		
24					L	H			H												A			
25	H					H			H	H			L	H							A			
26	H					H			H			H		H		L					A			
27																								
28																								
29																								
30																								
31																								

* Product Terms by Input Bit:

15	PU_TDI-	7	PU_ABFTCH
14	PU_MABAB-	6	PU_PFWE
13	PU_IINTRQ	5	PU_MIM
12	UNUSED	4	PU_TBGF
11	PU_MPINT-	3	PU_PFWFF-
10	PU_PEINT-	2	PU_SLAVEFF-
9	PU_TBGT-	1	PU_INTRQM
8	PU_PFTCH-	0	PU_FLTO

** Output Functions by Output Bit:

7	PU_SENTINT
6	PU_INTP
5	PU_INTP-
4	UNUSED
3	PU_PPR0
2	PU_PPR1
1	PU_PPR2
0	PU_PPR3

Figure 4-6. FPLA Interrupt System for the Upper Processor

FLTO is the floating point overflow interrupt source (may be unused).

TBGON is the ON/OFF bit for the time base generator.

PS-, MP-, SCHOD-, and CRS drive backplane lines directly. They are used as defined in Section X on the backplane.

TBGF is the TBG flag interrupt source. I/O interrupts (BP_INTRQ).

4.3.4.2 Interrupt Sources

The interrupt sources which the hardware recognizes in priority order are the following:

A/B fetch
TBG tick
Parity Error
Memory Violation (Memory Protect)
Slave
Power-Fail Warning
Floating point overflow
TBG flag
I/O interrupt

Parity error, memory protect, and TBG tick are signalled to the interrupt system by pulses and so they must be latched until the microcode services them. This is done with type 74S112 J-K flip-flops U904 (42-B) and U1202 (46-B). Parity error interrupt source is qualified with PEE (parity error enable) status and PU_ENDMRDP1. This is then synchronized in U1308 (45-C), a D flip-flop, before being used to set the parity error interrupt flop. ENDMRDP1 is true the cycle after the end of a memory read by the processor. If the PE line on the backplane is asserted at any other time (for example following a DMA read) the processor will ignore it.

Slave (BP_SLAVE-), and power fail (BP_PFW-) remain asserted on the backplane until they are serviced so they need only be synchronized before being input to U1004. This is done using bits in U1309 (66-D), a 74S174 type latch.

Unimplemented instruction, privileged instruction interrupts, and single instruction step are handled entirely by the microcode with no hardware assist.

The three interrupt flip-flops are settable and clearable by the microcode through the low four bits of the IST register. A write to the IST register enables U1002 ((42-B) if Y-bus bit no. 3 is low. Six of the outputs of U1002 are used to set and clear the three flip-flops. One other bit is used to clear the microcode time-out flip-flop.

Any write to the IST register will clear the INT flip-flop. The spare U1002 output is not used because it corresponds to one of the priority values which could be read from the IST register. The interrupt flip-flops and INT must be cleared in the interrupt service microcode. The microcode is allowed to set these flip-flops for diagnostic purposes. A read from the IST register provides the code of the highest priority interrupt pending in the low four bits. This code is generated in U1004 (47-C) and then latched in a type 74S174 chip since it is not generated fast enough. The previous list of interrupt sources is in priority order.

The TDI bit indicates that certain interrupts (TBG flag, power fail, and I/O interrupts) are to be held off. If they are asserted they will not cause an interrupt at the end of this instruction. This bit is cleared by FP_JTAB- and is toggled by FP_CMID-. TDI is generated by U1203 (45-D), a type 74S112 chip. The inputs to U1004 are:

Interrupt Sources	Description
PU_MPINT-	Memory Protect (Memory Violation)
PU_PEINT-	Parity Error
PU_TBGT-	Time-base Generator Tick
PU_FLTO	Floating-Point Overflow
PU_SLAVEFF	Slave
PU_IINTRQ	I/O Interrupt
PU_TBGF	Time-base Generator Flag Set
PU_PFWFF	Power-Fail Warning
PU_ABFTCH-	A/B Fetch

Masks and Enables	Description
PU_TDI-	Temporary Disable Interrupts
PU_PFWE	Power-Fail Enable
PU_INTRQM	I/O Interrupt Enable
PU_MIM	Master Enable

Other	Description
PU_MABAB-	A/B Addressed this cycle
PU_PFTCH-	Fetch occurring

The outputs are the four bits of the code for the highest priority interrupt (PPR0 to PPR3), both senses of INTP, the signal (SINT) which sets the INT flip-flop.

IINTRQ (interrupt request) is synchronized twice since the backplane specification does not guarantee setup or hold times to the latches used.

The interrupt source and mask inputs are combined to form the INTP condition (PU_INTP and PU_INTP-) and the four priority lines PU_PPR0 to PU_PPR3. PU_MABAB- is asserted if the current memory access is A or B addressed. PU_PFTCH is true if FP_FCHB- or FP_FCHP- are asserted. If INTP is true or MABAB and PFTCH are true the PU_SINT output of U1004 is asserted to set the INT flip-flop. The priority lines and INTP are latched so as to be valid early in the cycle. (See Figure 4-6 for the coding.)

The version of INTP before the latch is used to hold off the fetch signal (PU_FTCH-). The output of the priority latch can be read back onto the B-bus by IST in the B-Field as the low four bits of the IST. If a parity error interrupt is pending, or will be pending next cycle the signal PU_NOWRT- is asserted to change any memory write microorders to memory reads.

4.3.5 ADDRESS GENERATION LOGIC

4.3.5.1 MAB Generation

Memory addresses originate in either the B-bus or the P-register as specified by the microorder. The P-register normally holds the program counter which is shown on sheet no. 1 of the schematic. The P-register consists of four type-74LS163 counter chips (U104,U204,U304,U404).

The signal FP_LYP- causes the P-register to be loaded from the Y-bus, and FP_IP- enables the counter to increment. The P-register and B-bus address sources are multiplexed together to generate the memory address bus (MAB) by four type-74S157 Quad 2-to-1 multiplex chips (U105,U205,U305,U405) shown on schematic sheet no. 5. MRG resolution is also accomplished by these multiplexers with some additional gates for the upper five bits.

When JTAB is executed (FP_JTAB- asserted) the address on the B-bus, if a memory reference is requested, is really a memory reference group instruction. The ten low-order bits are address bits and B-bus bit-10 (BB10) selects either the base page or the current page. If BB10 is 0, the base page is selected and the upper 5 bits are set to zero. If BB10 is 1, the current page is selected and the upper five bits of MAB come from the P-register. The complete address is formed as follows:

BITS	INPUT	B-BUS SOURCE OUTPUT		P-REG. SOURCE OUTPUT
		BB10=0	BB10=1	
0-9	MRG address	BB0-BB9	BB0-BB9	P0 - P9
10	C/Z bit	0	P10	P10
11-14	Instruction	0	P11-P14	P11 - P14

The G-Strobe input of the MUX, used for the high-order four bits of U105 (52-B) forces zero outputs if BB10 is low and FP_JTAB- is low. The Select-S input to this MUX is altered so that the P-register is always selected when FP_JTAB- is asserted. The B-bus bit-10 input to the next MUX is modified with two gates so that the B-bus input to bit 10 is correct for MRG instructions. The expresssion for this is:

MUX10 input (PMAB10) = (P10 + JTAB') * BB10

MAB contains the memory address unmodified by the base register. MAB0 is sent to the lower processor card to determine whether to write to the A or B register if ABWR (A/B write) is asserted. If MAB1 through MAB14 are all zero and A/B addressability is enabled (PU_ABAB- is low) PU_MABAB- is asserted indicating that the memory reference is to the A- or B-register. PU_ABAB- is a bit in MEMR. The all zero condition is determined by the 5-Input NAND gates at U505 (57-C) and U506 (57-B). If MAB references the base page and not the A- or B-registers, and the base register logic is enabled (Base register bit 15 is 1), PU_BASEPG is asserted.

4.3.5.2 Base Register Logic

The base register is added to all addresses except 0 and 1 in the base page if it is enabled.

The base register logic is shown on sheet no. 6 of the schematic diagrams. The 15 low bits of the base register are always added to MAB by four 74S283 four-bit adders (U106,U306,U107,U307). If bit 15 of the base register is a one and the reference is to base page (PU_BASEPG asserted), four 74S157 multiplexer chips (U206,U406,U207,U407) put the output of the adders onto the MAB2-bus. Otherwise the MAB-bus is passed unchanged to the MAB2-bus.

When the base register is enabled (BR15 is a "1") the hardware distinguishes between memory references to code and to data and sends them to different maps. This logic is shown on sheet no. 8 of the schematic diagrams (84-A, 85-A). The low bit of the address extension bus (map number) is forced to "1" indicating a code map in either one of two cases: If the memory reference is begun by an MRG instruction that does not reference the base page; or if the microorder executed is FCHB, FCHP, BFB, or RDPC.

The base register itself is shown on sheet no. 1 of the schematic diagrams. It consists of two 74LS377 eight-bit register chips (U804,U704). It is loaded with the signal FP_LDBR-. The base register bits are as follows:

Bit	Explanation
15	0 = base register disabled
14-0	don't care
15	1 = base register mode
14-0	base register value

4.3.6 MEMORY ADDRESS AND DATA LATCHES

4.3.6.1 Address Latches

The memory address latches are shown on sheet no. 8 of the schematics. The final resolved address on the MAB2-bus is latched in three places. Whenever there is not a memory request pending (PU_MRP), the transparent latches that drive the backplane address-bus switch to "open" during the long half-cycle. The latches are U208 (84-C) and U209 (84-D). The signal that gates the latches is the following:

MALCK = MRP' * PC-'.

If a memory request is pending, the memory address and data latches already hold address and data waiting to be sent over the backplane. A new memory microorder at this time will cause a clock freeze, and the MAB2-bus will not change until after there is no longer a memory request pending.

Every memory address is latched in the MA-register U408 (43-B) and U409 (43-B). A memory microorder is signaled by PU_MEMRQ which causes MA to be clocked. This register is necessary so that the microcode can recover the resolved address to get sequential addresses for multiple word operands.

If a fetch is executed (FCHP or FCHB), the signal PU_FTCH- causes FA to be be clocked. The MAB2-bus is stored in register FA so that the microcode can recover the address of the last fetch if a violation occurs (memory protect to overflow). Register FA consists of U308 (82-D) and U309 (82-D).

The memory address latch is enabled to the backplane address bus whenever nothing else is driving that bus. This is done for timing reasons since it is too late to decide to drive the address bus after it is known that a processor memory cycle will occur. The I/O master is allowed to drive the address bus while it has signal MRQ asserted. It will also drive the backplane while signal IAK is asserted.

The memory address latch is enabled to the backplane by:

PU_OEAD- = MRQ + IAK

When signal PU_OEAD- is low the latch is enabled.

The address extension bus latch U108 (86-D) is opened and enabled with the same signals as the memory address latch. The map number which goes onto the address extension bus originates in the MEMR-register. The MEMR-register contains memory related control signals which the microcode has direct access to it. MEMR is U606 (26-B), a type 74LS377 chip. The format of MEMR is:

BIT	CONTENTS	DESCRIPTION
0	MAEB0	Address Extension Bus Bit Zero.
1	MAEB1	
2	MAEB3	
3	MAEB4	
4	MAEB5	
5	ABAB	A/B Addressibilty Enable.
6	MEMDIS	Memory Disable (backplane line to enable boot memory).
7	MCD	Memory System Disable.
8-15	---	Refer to N-register description (bits are shared with N

If MCD is high the upper processor will not perform any memory cycle on the backplane. This allows the microcoded self test to test the memory addressing logic without assuming that the memory controller works.

4.3.6.2 Data Latch

The data latch is U608 (87-B) and U609 (86-B) consisting of a pair of 74S374 type chips. They latch the Y-bus at the end of the processor cycle in which a WRIO or a memory write (MEMWR) occur. The LC+ clock is used to generate the latch signal (MDLCK) because MEMWR is not valid before the trailing edge of PC-. Data from the latch must be enabled onto the backplane data bus while the processor is driving MEMGO for a memory write and during the last two cycles of an I/O write handshake.

U709 (83-A), a 74S51 chip, is used to generate POEDAT which indicates the data be driven and continue to be driven into the first half of the next cycle. A transparent latch is used to extend this signal into the next half cycle.

4.3.7 MEMORY STATE-MACHINE AND CONTROL LOGIC

This memory state-machine and control logic is contained on sheet no. 7 of the schematics.

Memory accessing microorders are the following:

WRP (FP_LYWRP-)	Memory write with address in the P-register. Data comes from the Y-bus.
WRB (FP_LYWRB-)	Memory write with address on B-bus. Data comes from the Y-bus.
CWRB (FP_LYCWRB-)	Conditional read/write. A memory access will occur with the address on the B-bus. If B-bus bit 15 is low a write will occur with the data on the Y-bus. If BB15 is high a read will happen. This microorder aids in the resolution of indirects which will be followed by a store.
RDP2 (FP_RDP2-)	RDP in the SP2 field. Memory read with address from P register.
RDP0 (FP_RDP0-)	RDP in the SP0 field. Memory read with address from P register.
RDB2 (FP_RDB2-)	RDB generated by the JTAB logic. Memory read with address on B-bus.

RDBO (FP_RDBO-) RDB in the SPO field. Memory read with address on B-bus.

FCHB (FP_FCHB-) Fetch with B. Fetch next instruction with address on B-bus. This microorder will not be executed if an interrupt is pending. Register FA is updated if it is executed.

FCHP (FP_FCHP-) Fetch with P. Fetch next instruction with address in the P-register. This microorder will not be executed if an interrupt is pending. FA is updated if it is executed.

BFB (FP_BFB-) Broadcast fetch with B. A memory read is done with the address on the B-bus. RNI is asserted during this access so that I/O masters and slave devices will pick up the instruction. FA is not updated.

IFCH (FP_IFCH-) Interrupt fetch. IAK is asserted on the backplane and a memory read is done. No address is driven on the backplane since IAK is asserted. RNI is not asserted, and the I/O master will provide the address. FA is not updated, and MA is updated but it will not hold the address from which the read occurred. The read address is latched in the CIL register.

FCHP and FCHB are qualified in the interrupt logic and combined into the signal PU_FTCH- which is asserted to cause a memory fetch.

All of the memory signals are combined in U906 (72-A), a 13-input NAND gate, to form the signal PU_MEMRQ. This signal is asserted to mean that a memory access microorder is being executed. The expression for generation of PU_MEMWR is the following:

PU_PMEMWR = WRP + WRB + (CWRB * BB15′).

PU_PMEMWR is true if a memory write is being executed. It is qualified with PU_NOWRT- (asserted means a parity error occurred) to form PU_MEMWR-.

PU_MABAB- is true if the address on the MAB-bus is zero or one. This means that the access of this cycle is to the A- or B-registers. MABAB- and MEMWR- make FP_ABWR-, the signal that is sent to the lower processor to direct it to write to the A- or B-registers.

PU_MEMAC indicates that a memory access over the backplane is being executed this cycle. It is asserted if PU_MEMRQ is asserted and the processor is not frozen and the address does not refer to the A- or B-register. (A memory cycle must already be held in the address and data latches to be started while the processor is frozen.) RDPO, RDBO, WRP, and FCHP are ORed together to form PU_ENPMAB that is used to select the MUX which puts the P-register or the B-bus onto MAB.

4.3.7.1 Memory and I/O State Machine

The memory and I/O state machine (MIOSM) consists of a programmable array logic (PAL) chip U1106 (74-D), a Monolithic Memories PAL16R6. These chips are generically PLAs (programmable logic arrays).

This PAL has eight inputs, two ordinary outputs, and six registered outputs. The registers are cleared by FP_BPON so that it powers up in state zero. The outputs of the MIOSM are the following:

PU_MRP-, PU_MAIP-, PU_TFRZ-, PU_MRIOIP-,PU_IAIPRP-, PU_MGO-, PU_IOGO-.

The state machine keeps track of the memory and I/O accesses. It controls the assertion of MEMGO and the determination of when to freeze the processor. It also controls the assertion of IOGO. See Figures 4-7 for a memory timing diagram and Figure 4-8 for the memory and I/O state machine diagram.

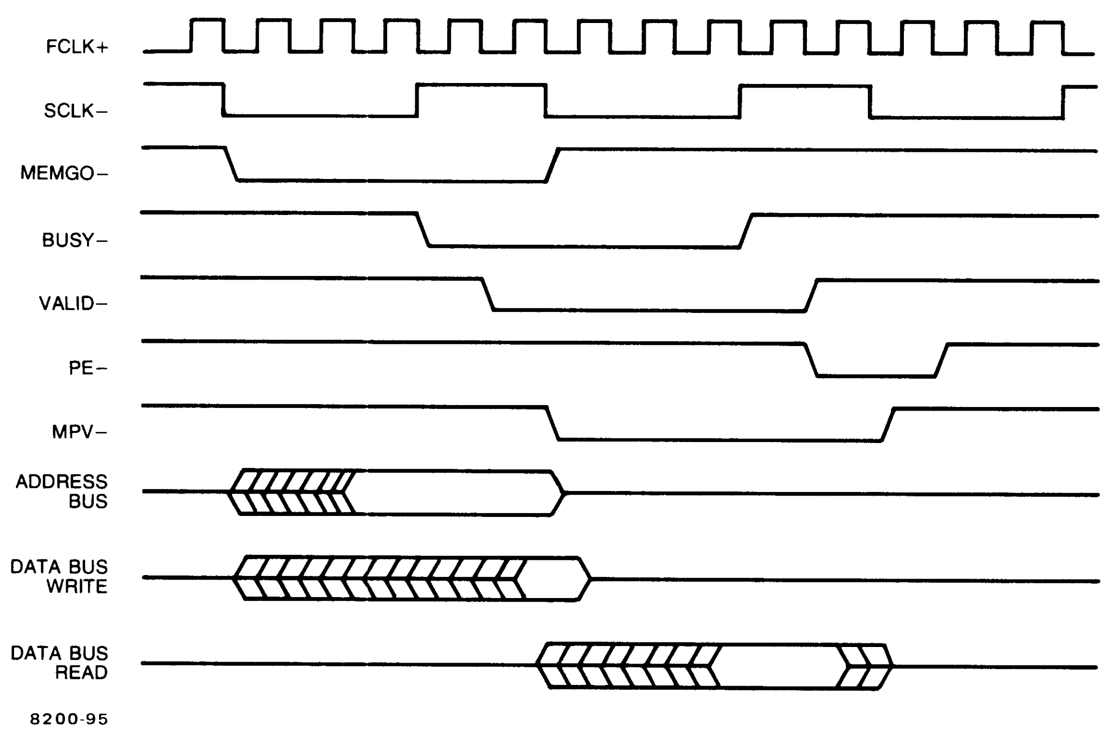


Figure 4-7. A700 Processor Memory Timing Diagram

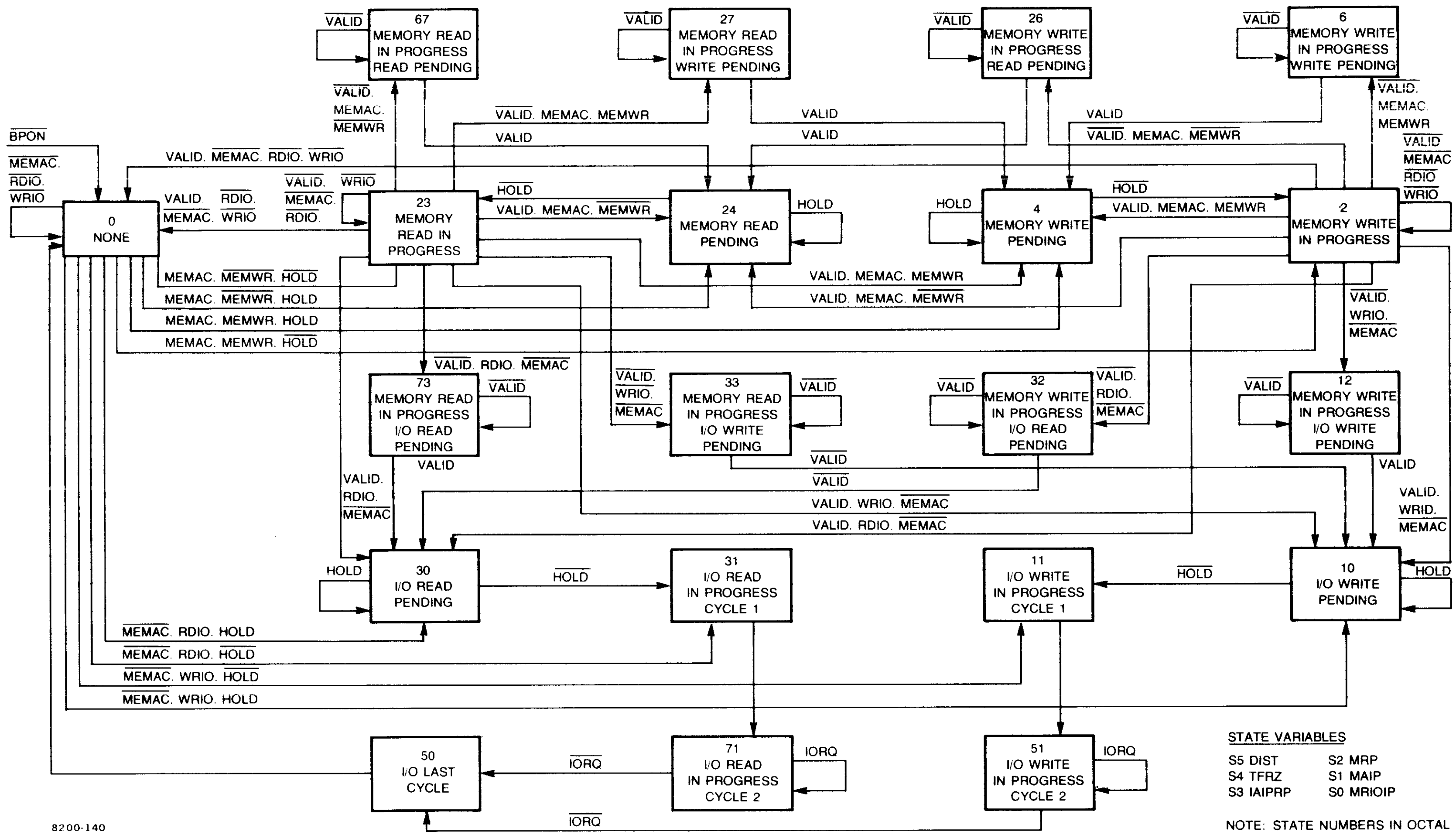


Figure 4-8. Memory and I/O State-Machine State Diagram

The MIOSM outputs have the following conditions:

a. MRP is asserted if a memory request is pending. The backplane was busy when the last memory microorder was executed and the address and data (for a write) were latched. The access will happen when the backplane is no longer busy.

b. MAIP is asserted if a memory request is in progress. MEMGO has been asserted and the memory circuitry is currently busy.

c. TFRZ is asserted if the T-register is not valid. The processor will freeze if it attempts to access the T-register while TFRZ is asserted.

d. MRIOIP is true if a memory read or any I/O access is in progress.

e. IAIPRP is asserted if an I/O access is in progress or pending.

f. MGO indicates the first cycle of a memory access and MEMGO should be asserted on the backplane if possible (no DMA in progress).

g. IOGO is true if IOGO should be asserted on the backplane.

MEMAC and MEMWR are described in the paragraph above under memory state-machine and control logic.

The HOLD signal indicates that the backplane is busy. A memory cycle may not be started this cycle. HOLD is the OR of PU_IBUSY, PU_IMRQ. A memory cycle can't be started if another memory cycle is in progress (IBUSY), if DMA is requesting a memory cycle (IMRQ).

The MIOSM powers up in state 0, and MEMAC or RDIO or WRIO must be asserted in order for it to leave state 0. If HOLD is true the next state will be one with MRP asserted. When HOLD becomes false a transition will be made to a state with MAIP.

The signal PU_IVALID originates on the memory controller and is asserted for one cycle during the last cycle of any memory access. IVALID indicates to the state machine that the memory access in progress is over. MEMAC will never be asserted if MRP is true since another memory access while one is being held in the latches will cause the processor to freeze, and signal FREEZE holds off MEMAC. The MEMWR signal at the time of the memory access microorder determines whether the following states will include MRIOIP or TFRZ.

RDIO and WRIO cause entry to states with IAIPRP asserted. RDIO in addition causes TFRZ to be asserted.

4.3.7.2 MEMGO Circuitry

In order to get maximum speed out of the memory system a memory cycle is begun in the cycle in which it is requested by the microcode, if possible (MRQ is not asserted). The start of a memory cycle is signalled to the memory controller by the assertion of MEMGO on the backplane. MEMGO is asserted at the middle of the cycle so the processor must assert it while the state machine is still in state zero. The basic condition for asserting MEMGO is that the current state does not assert MAIP and the next state will assert MAIP. The memory cycle actually begins with the assertion of MEMGO one-half cycle before MAIP is asserted.

If an I/O device asserts MRQ in the same cycle as the processor asserts MEMGO the MRQ prevails and MEMGO must be deasserted before the end of the cycle and not reasserted until the DMA cycle is over. MRQ comes valid very late in the cycle. It is early enough that its assertion will cause the next state to be MRP rather than MAIP, but late enough that MAIP will not be deasserted early enough to prevent MEMGO from being asserted. Therefore, MRQ bypasses the state machine and is an input to the gate which generates PMEMGO. During an interrupt fetch (IFCH) the address and MEMGO are driven by the I/O master so IFCH and IAKP both hold of MEMGO also.

PMEMGO is passed through one bit of transparent latch U1307 (78-D), a 74S157 2-to-1 multiplexer, to become QIMEMGO. This latch is open during the last half of each cycle and serves to hold MEMGO through the first half cycle.

Microorders FTCH, BFB, and IFCH need additional hardware outside of the state machine. As far as the state machine is concerned these are ordinary memory reads. They are distinguished through signals latched in U1206 (75-C), a 74S174 D-type flip-flop. This latch is clocked every time there is a memory read. It is clocked with clock signal LC since MEMWR is not valid early enough in the cycle to use PC. The same latch is used to remember whether the last read accessed the A- or B-register. The latch must be cleared by RDIO since I/O read data is returned to the T-register. However, if the last read was from either the A- or B-register, a T-microorder enables the A- or B-register onto the B-bus and not the T-register.

Signal PU_ENDMRD is asserted during the last cycle of a processor memory read. It is generated with PU_MRIOIP and PU_IVALID. When a fetch is executed, the signal FP_TCNT- must be asserted during the last cycle of the read to signal the lower processor to latch the instruction into the counter.

Signal TCNT must remain asserted until VALID is released. During an error correction VALID is stretched due to a pause in the backplane clock. TCNT is qualified by MEMCE which is true during the last PC cycle of a memory cycle and remains true after that until VALID goes away.

Signal MRIP is asserted during a memory read. It is true if a memory access is in progress (MAIP) and a memory read or I/O access is in progress (MRIOIP).

Using microorder BFB differs from an ordinary read in that RNI is asserted on the backplane during the memory cycle. RNI must be asserted while BUSY is asserted by the memory controller. RNI is asserted with RNIP and MRIP.

Using microorder IFCH differs from an ordinary read in that IAK is asserted on backplane, MEMGO is not asserted, and the address bus is not driven. IAK is asserted with MRIP and IAKP. IAKP is IFCH latched by U1206 (75-C), type 74S174, IFCH or IAKP hold off MEMGO. On its way to the backplane, IAK is used to disable the address drivers.

A read should not be in progress when any of these four microorders (FCHB, FCHP, BFB, and IFCH) are executed or the read will clock the latch and change the type of read being executed. It can be assured that any previous read is finished by executing microorder T (B-Field in a previous cycle or the same cycle as the FTCH, BFB, or IFCH). In addition a freeze will occur if any memory cycle is in progress and a fetch (FCHB or FCHP) is executed.

4.3.7.3 A/B Fetch

Signal ABFTCH is true if the last memory read was a fetch and the last memory read addressed either the A- or B-register. Both of these signals (PTCNT and LRAB) are available from the last memory read latch U1206 (75-C). ABFTCH becomes an input to the interrupt prioritizer and it is a status bit available as a bit of the N-register. The status bit is used in I/O broadcasting since an instruction cannot be broadcast from the A- or B-register directly. Note that the ABFTCH status bit is only valid until the next memory read.

4.3.7.4 T-Register

Data returned from a memory read or an I/O read is latched in the T-register. This register is U508 (22-C) and U509 (22-B). It consists of two type 74S374 8-bit latches. The generated clock for this register (TCK-) is shown on sheet 9 of the schematic diagrams.

The T-register is clocked at the end of each cycle during which TFRZ is asserted. This signal indicates that a memory read or I/O read is in progress or pending. Since it is impossible for the micromachine to read the T-register while this signal is asserted (the processor clock would freeze), it does not matter that T could be clocked more than once. Since valid data is always returned during the last cycle of the read, the data that ends up in register T will be correct.

A memory read may reference the A- or B-register. There is no data path to put these registers into the T-register since they are in the micromachine register file. The T microorder in the B-Field will enable either register T or A or B to the B-bus depending on the last memory read. LRAB and LRMABO are saved in the last memory read latch U1206 (75-C). LRAB indicates that the last read was from the A- or B-register. Its data is MABAB.

LRMABO latches the MABO bit of each read to distinguish between the A- and B-registers. These two signals are sent to the lower processor card. When ETABB- is asserted, the T-register will be enabled to the B-bus only if the last read was not A or B addressed. If it was A or B addressed the lower processor enables register A or B to the B-bus depending on LRMABO. LRMAB must be cleared when an I/O read occurs so that the processor can access the data returned to T.

4.3.8 FREEZE LOGIC

The freeze logic is shown on sheet no. 9 of the schematic diagrams, and the freeze logic timing diagram is provided in Figure 4-9.

There are four basic conditions that can cause the processor clock to freeze. These freeze conditions are the following:

1. An attempt to read the T-register before data has been returned from the last memory or I/O read.

2. An attempt to do a memory or I/O operation while there is still valid data in the memory address latch and memory data latch.

3. An attempt to access the map RAMS on the memory controller card while the memory controller needs them for a memory cycle.

4. An attempt to execute a FCHB or FCHP microorder while a memory access is in progress.

These conditions generate signal FP_FREEZE- which is gated with SCLK+ to make PC- the processor clock. FREEZE must be valid by about 90 nanoseconds into the cycle in order to hold-off the clock properly so no more than two levels of gating are allowed between the microorder signals and the freeze signal. The generation of this signal is one of the critical time paths. The FREEZE- signal is generated by U701 (93-B), a type 74S64 chip.

The first freeze condition is expressed by

FP_ETABB-' * PU_TFRZ-

where TFRZ is provided by the MIOSM to indicate that a read is in progress or pending and that the TAB microorder (ETABB signal) should cause a freeze to wait for returned data.

The second freeze condition is generated by 13-input NAND gate U601 (97-B) which ORs together all of the memory and I/O referencing signals to make signal PU_BPAC. If a memory request is pending or an I/O request is pending or in progress the memory data and address latches hold useful information. This condition generates signal PU_MEMP which is the OR of MRP and IAIPRP. The freeze occurs if signals BPAC and MEMP are both true at the same time. A freeze could occur for one cycle when a memory reference addresses the A- or B-registers even though this reference will not use the memory latches since the information that the address is A or B comes too late in the cycle to prevent the freeze.

For the third freeze condition, the memory controller accesses the map registers while MEMGO is asserted and the map RAMs when MEMGO is not asserted. The processor uses the map RAMs in the memory access cycles during the first half of the first clock cycle and the second half of the second clock cycle until the next access starts. (See the Map RAM Access Timing Diagram of Figure 4-10.) The output of the RAMS is latched at the end of the first half cycle and is available throughout the cycle. Thus a map read can occur during cycles 1 or 3, but not cycle 2. The processor must freeze during cycle 2 if it tries to read the map RAMs. This freeze condition expression is: BUSY * EMAPB. The write to the map RAMs occurs at the end of the cycle; therefore, the processor can write to the RAMs during cycles 2 and 3. The processor must freeze if it tries to write to the map RAMs during cycle 1.

The map write freeze condition expression is: BUSY′ * LYMAP * (MRP + SMRQ) where SMRQ is an asynchronized version of MRQ which is true during cycles 1 and 2 during DMA accesses. The condition (BUSY′ * SMRQ) distinguishes cycle 1 for DMA cycles. If BUSY is not asserted and MRQ is not asserted the processor will start a memory cycle so (BUSY′ * MRP) distinguishes cycle 1 for processor accesses. The freeze conditions are combined in U701 (type 74S64).

The fourth freeze condition is expressed by the following:

(FCHB + FCHP) * BUSY.

This condition is generated in the same gates as the third freeze condition described above.

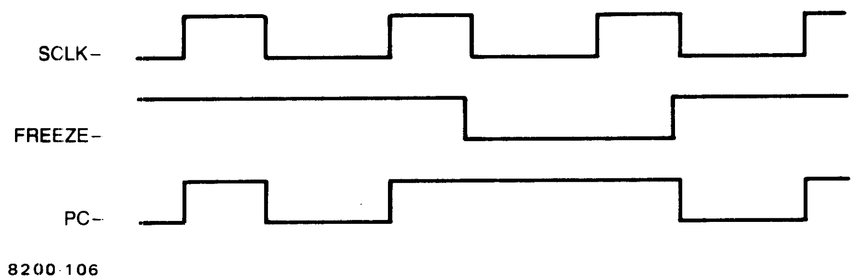


Figure 4-9. Freeze Logic Timing Diagram

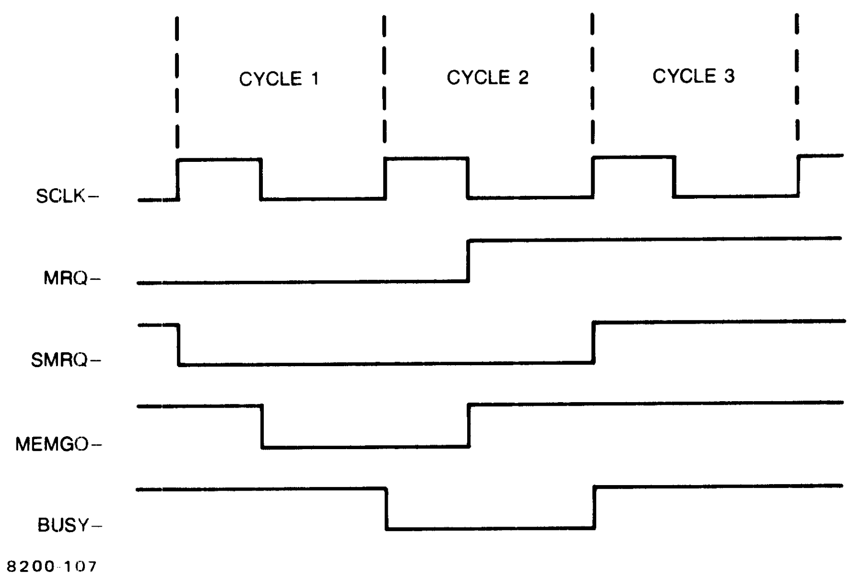


Figure 4-10. Map RAM Access Timing Diagram

4.4 PARTS LOCATIONS

The parts locations for the upper processor are shown in Figure 4-11.

4.5 REPLACEABLE PARTS LIST

The replaceable parts for the upper processor are listed in Table 4-2. Refer to Table 3-8 for the names and addresses of the manufacturers of the parts in the Manufacturer's Code List.

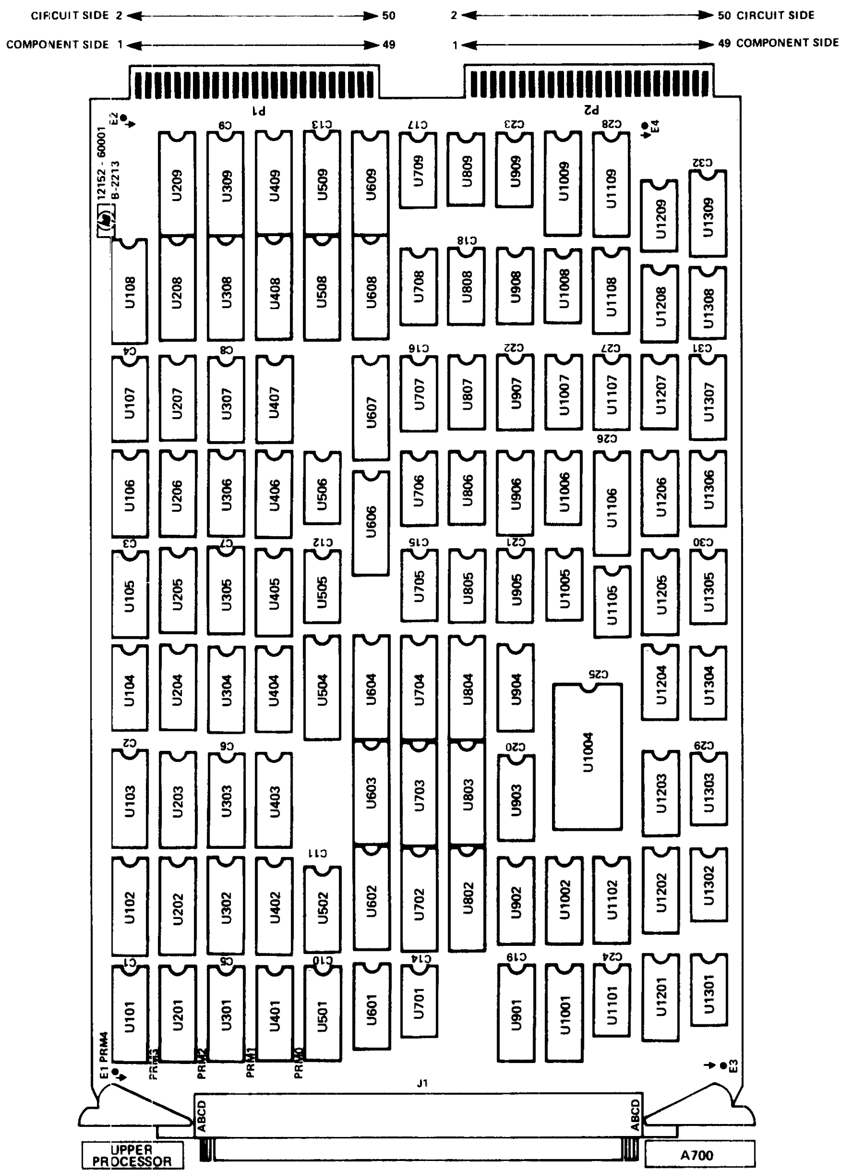


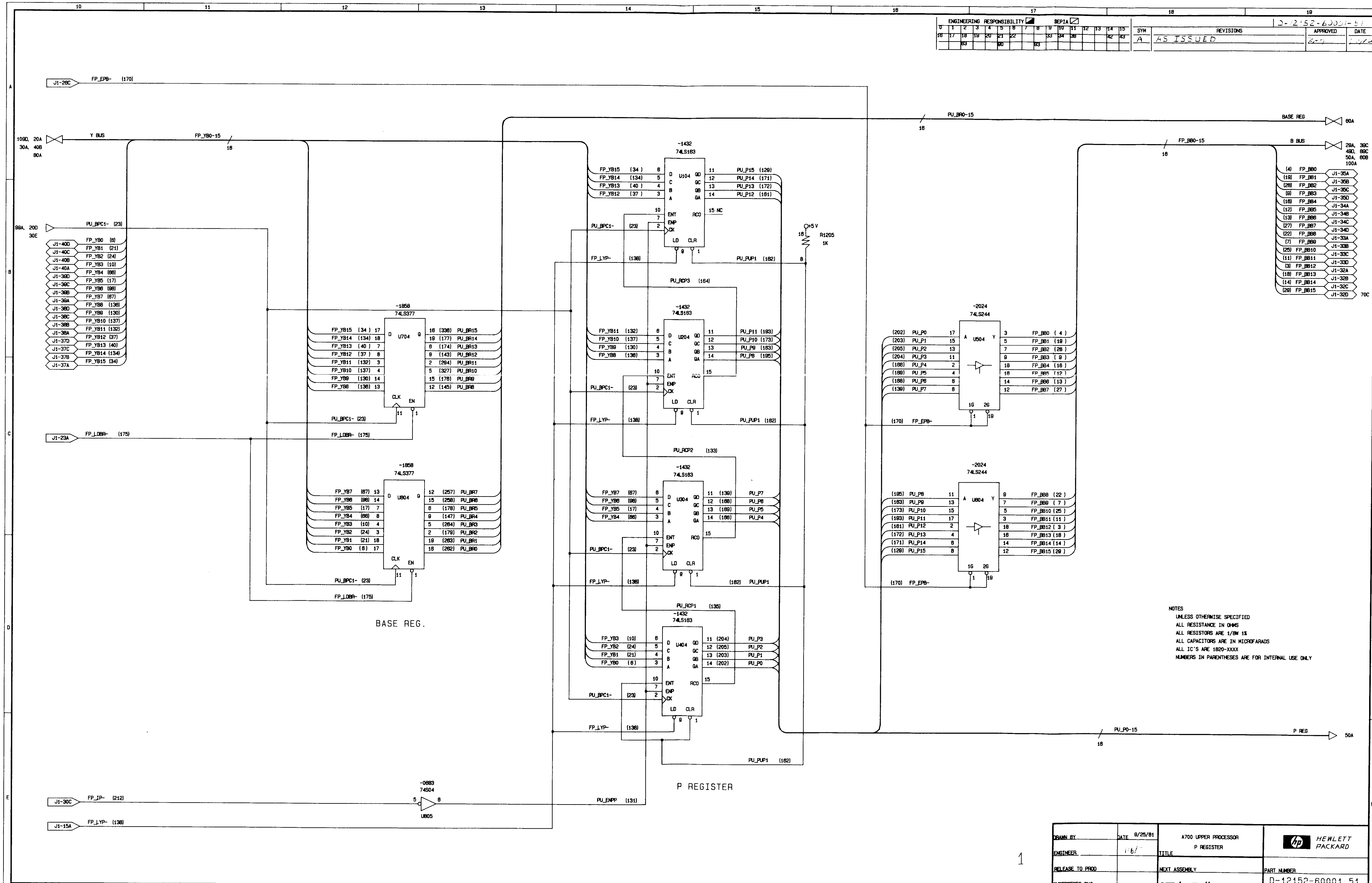
Figure 4-11. Upper Processor Parts Locations

Table 4-2. Upper Processor Replaceable Parts List

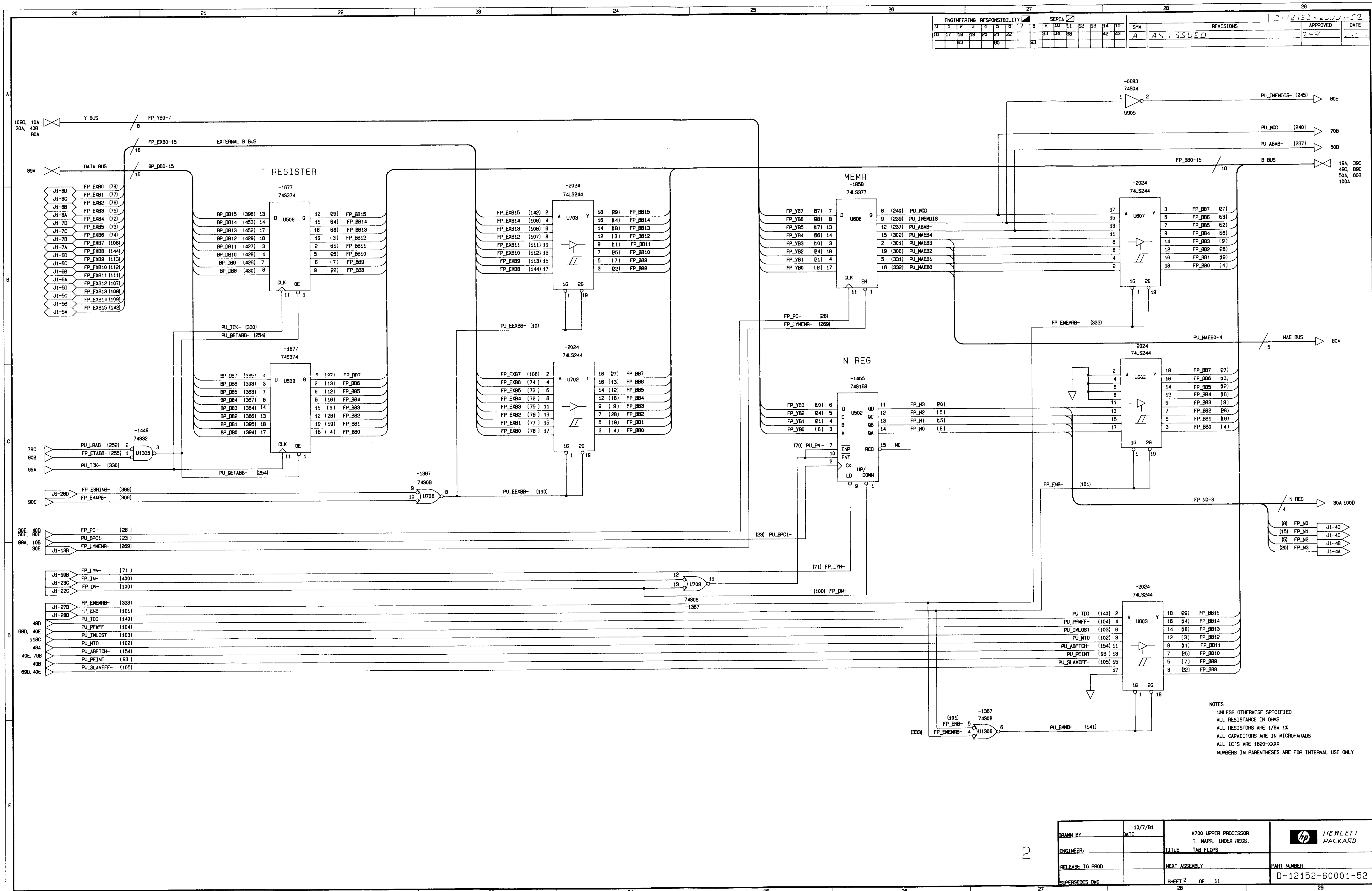
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12152-60001	1	1	PCA-UPPER PROCESSOR	28480	12152-60001
	12152-64001	9	1	ASSEMBLY-AUTO INSERT PART OF 12152-60001	28480	12152-64001
C1	0160-4832	4	32	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C3	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C4	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C7	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C8	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C9	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C10	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C11	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C12	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C13	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C14	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C15	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C16	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C17	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C18	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C19	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C20	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C21	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C22	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C23	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C24	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C25	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C26	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C27	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C28	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C29	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C30	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C31	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C32	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
U101	12152-80009	1	1	IC-ROM, XALU-4	28480	12152-80009
U102	1820-1985	3	8	IC RGTR TTL S D-TYPE	27014	DM85S68J
U103	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U104	1820-1432	5	4	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U105	1820-1077	4	9	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U106	1820-1871	6	4	IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U107	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U108	1820-2184	6	3	IC LCH TTL S OCTL	50364	74S373N
U201	12152-80008	0	1	IC-ROM, XALU-3	28480	12152-80008
U202	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U203	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U204	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U205	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U206	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U207	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U208	1820-2184	6		IC LCH TTL S OCTL	50364	74S373N
U209	1820-2184	6		IC LCH TTL S OCTL	50364	74S373N
U301	12152-80007	9	1	IC-ROM, XALU-2	28480	12152-80007
U302	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U303	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U304	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U305	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U306	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U307	1820-1871	6		IC ADDR TTL S BIN FULL ADDR 4-BIT	01295	SN74S283N
U308	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U309	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U401	12152-80006	8	1	IC-ROM, XALU-1	28480	12152-80006
U402	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U403	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U404	1820-1432	5		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS163AN
U405	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U406	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U407	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U408	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U409	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U501	12152-80005	7	1	IC-ROM, XALU-0	28480	12152-80005
U502	1820-1455	2	1	IC CNTR TTL S BIN UP/DOWN SYNCHRO	01295	SN74S169N
U504	1820-2024	3	9	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U505	1820-1275	4	2	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U506	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N

Table 4-2. Upper Processor Replaceable Parts List (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U508	1820-1677	0	4	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U509	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U601	1820-1130	0	2	IC GATE TTL S NAND 13-INP	01295	SN74S133N
U602	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U603	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U604	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U606	1820-1858	9	3	IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U607	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U608	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U609	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U701	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U702	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U703	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U704	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U705	1820-1449	4	4	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U706	1820-0681	4	5	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U707	1820-0685	8	3	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U708	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U709	1820-1158	2	1	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U802	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U803	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U804	1820-1858	9		IC FF TTL LS D-TYPE OCTL	01295	SN74LS377N
U805	1820-0683	6	6	IC INV TTL S HEX 1-INP	01295	SN74S04N
U806	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U807	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U808	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U809	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U902	1820-2056	1	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS378N
U903	1820-2056	1		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS378N
U904	1820-0629	0	4	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U905	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U906	1820-1130	0		IC GATE TTL S NAND 13-INP	01295	SN74S133N
U907	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U908	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U909	1810-0182	9	1	RESISTIVE NETWORK-DIP	28480	1810-0182
U1002	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U1004	12152-80021	7	1	IC-ROM, INT SYS	28480	12152-80021
U1005	1820-1989	7	3	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U1006	1820-0688	1	1	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U1007	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1008	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U1009	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1101	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U1102	1820-1196	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U1105	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U1106	12152-80010	4	1	IC-ROM, MIOSM	28480	12152-80010
U1107	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U1108	1820-1430	3	1	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U1109	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1201	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1202	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1203	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1204	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U1205	1810-0256	8	1	RESISTIVE NETWORK-DIP	01121	316A102
U1206	1820-1076	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG CLEAR	01295	SN74S174N
U1207	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U1208	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U1209	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U1301	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U1302	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U1303	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U1304	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U1305	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U1306	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U1307	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U1308	1820-0693	8	1	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U1309	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N



BASE REG.
P REGISTER
74LS377
74LS163
74LS244
74S04
U704
U804
U104
U204
U304
U404
U504
U604
U805
R1205 1K
+5 V
Y BUS
BASE REG
B BUS
P REG
NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
SYM
APPROVED
DATE
A
AS ISSUED
DRAWN BY
DATE 9/25/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
A700 UPPER PROCESSOR
P REGISTER
TITLE
NEXT ASSEMBLY
SHEET 1 OF 11
PART NUMBER
D-12152-60001 51
HEWLETT PACKARD



ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
A
AS ISSUED
T REGISTER
-1677
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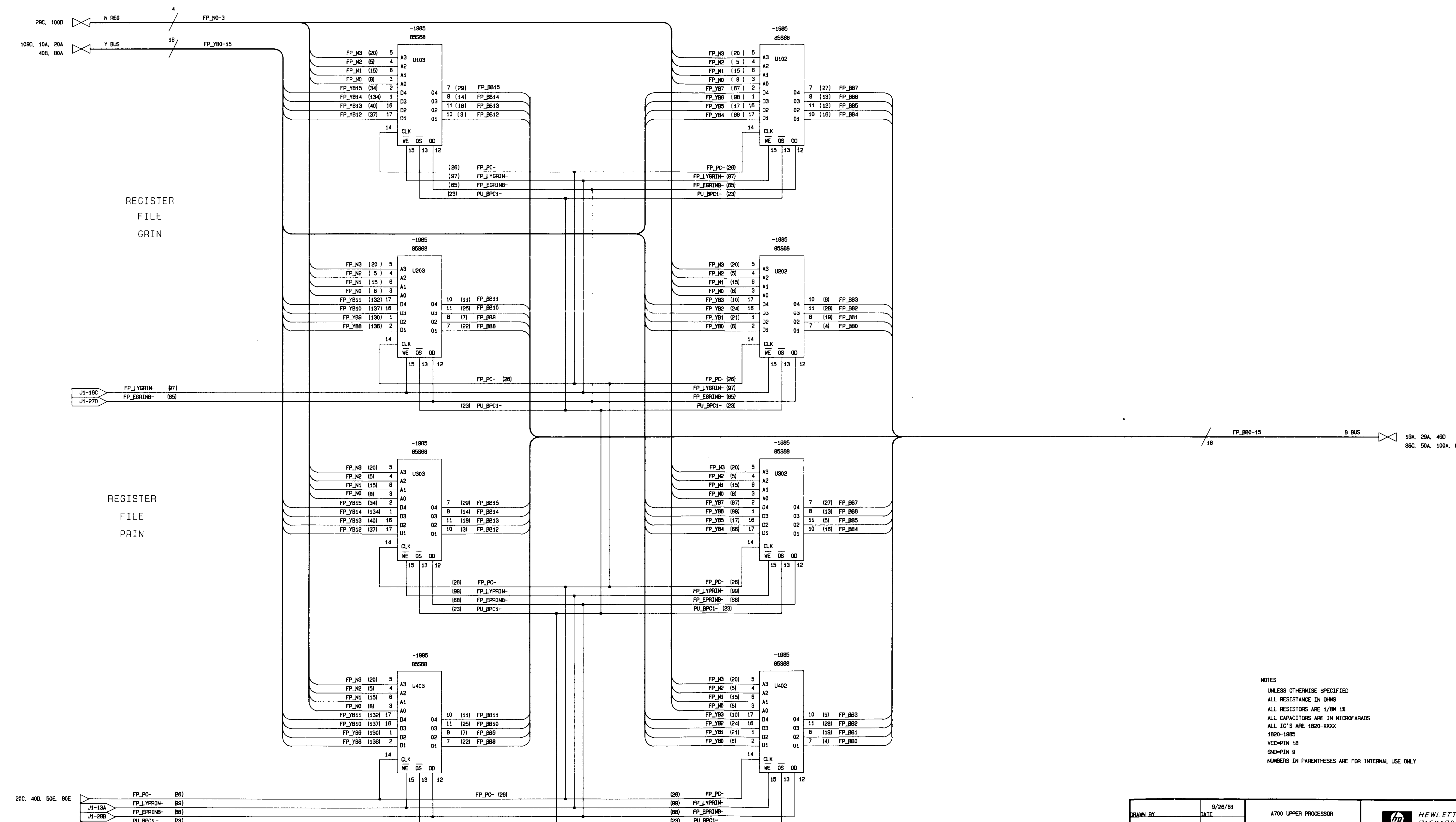
U509
U508
MEMR
-1858
74LS377
U606
N REG
-1455
74S169
U502
-2024
74LS244
U703
U702
U607
U602
U603
-0883
74S04
U905
-1449
74S32
U1305
-1367
74S08
U708
U1308
Y BUS
FP_YB0-7
EXTERNAL B BUS
FP_EXB0-15
DATA BUS
BP_DB0-15
B BUS
FP_BB0-15
MAE BUS
PU_MAEB0-4
N REG
FP_N0-3
PU_IMEMDIS- (245)
PU_MCD (240)
PU_ABAB- (237)
PU_TCK- (330)
PU_GETABB- (254)
PU_EEXBB- (110)
PU_LRAB (252)
FP_ETABB- (255)
FP_ESRINB- (369)
FP_EMAPB- (309)
FP_PC- (26)
PU_BPC1- (23)
FP_LYMEMR- (269)
FP_LYN- (71)
FP_IN- (400)
FP_DN- (100)
FP_EMEMRB- (333)
FP_ENB- (101)
PU_TDI (140)
PU_PFWFF- (104)
PU_IMLOST (103)
PU_MTO (102)
PU_ABFTCH- (154)
PU_PEINT (93)
PU_SLAVEFF- (105)
PU_EMNB- (141)
NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
DRAWN BY
DATE 10/7/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG
A700 UPPER PROCESSOR
T, MAPR, INDEX REGS.
TITLE TAB FLOPS
NEXT ASSEMBLY
SHEET 2 OF 11
HEWLETT PACKARD
PART NUMBER
D-12152-60001-52

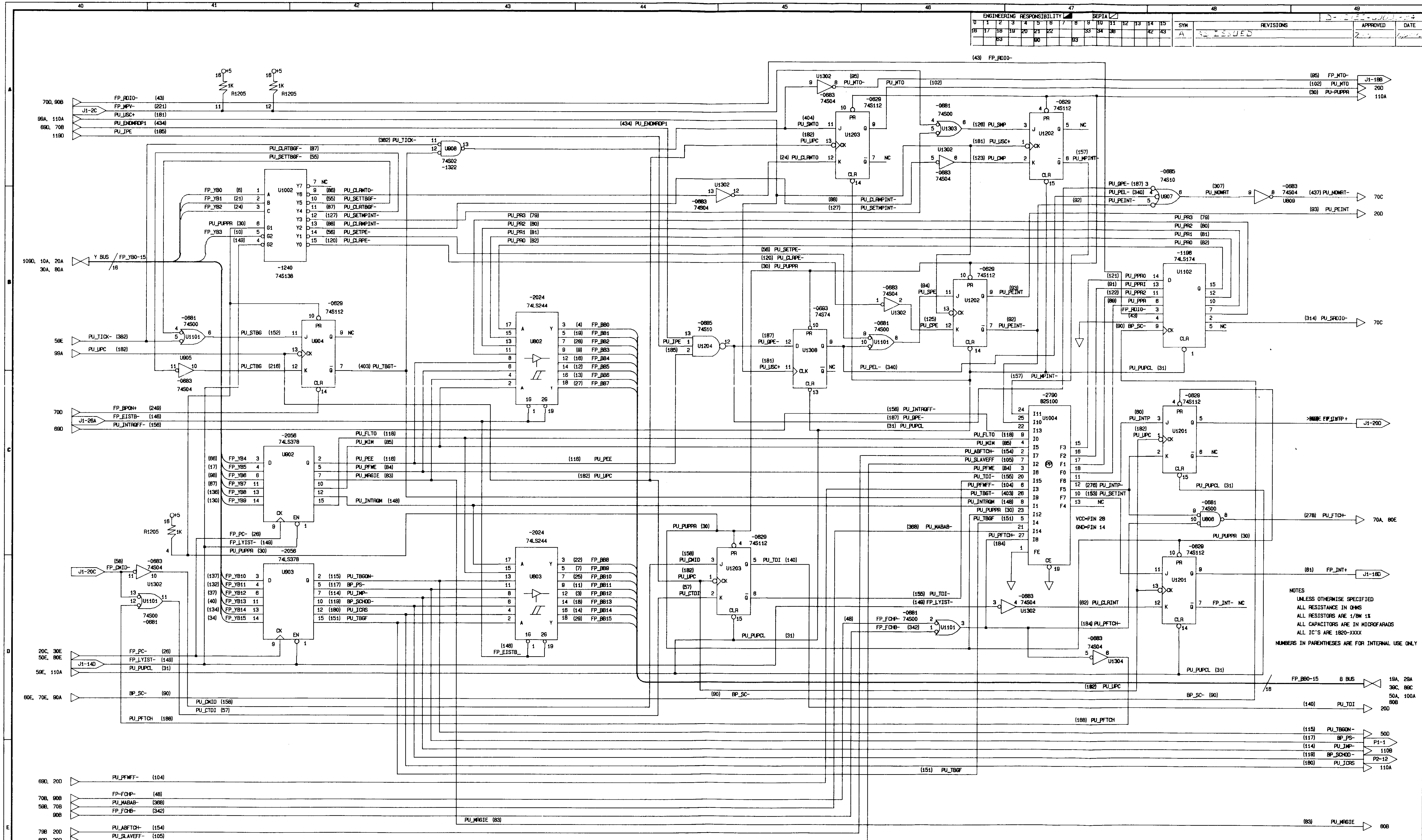


NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
1820-1985
VCC=PIN 16
GND=PIN 8
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		

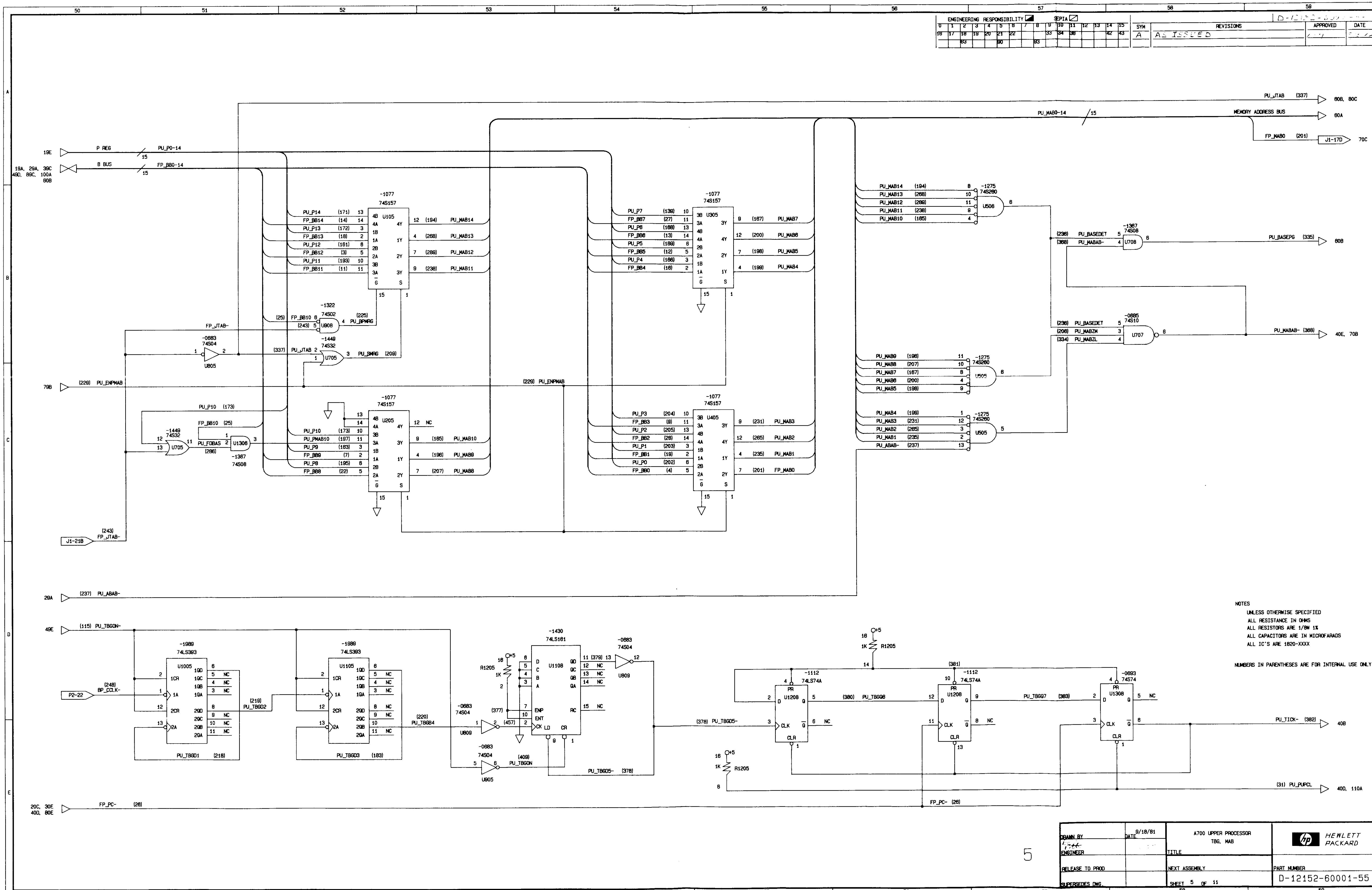
3

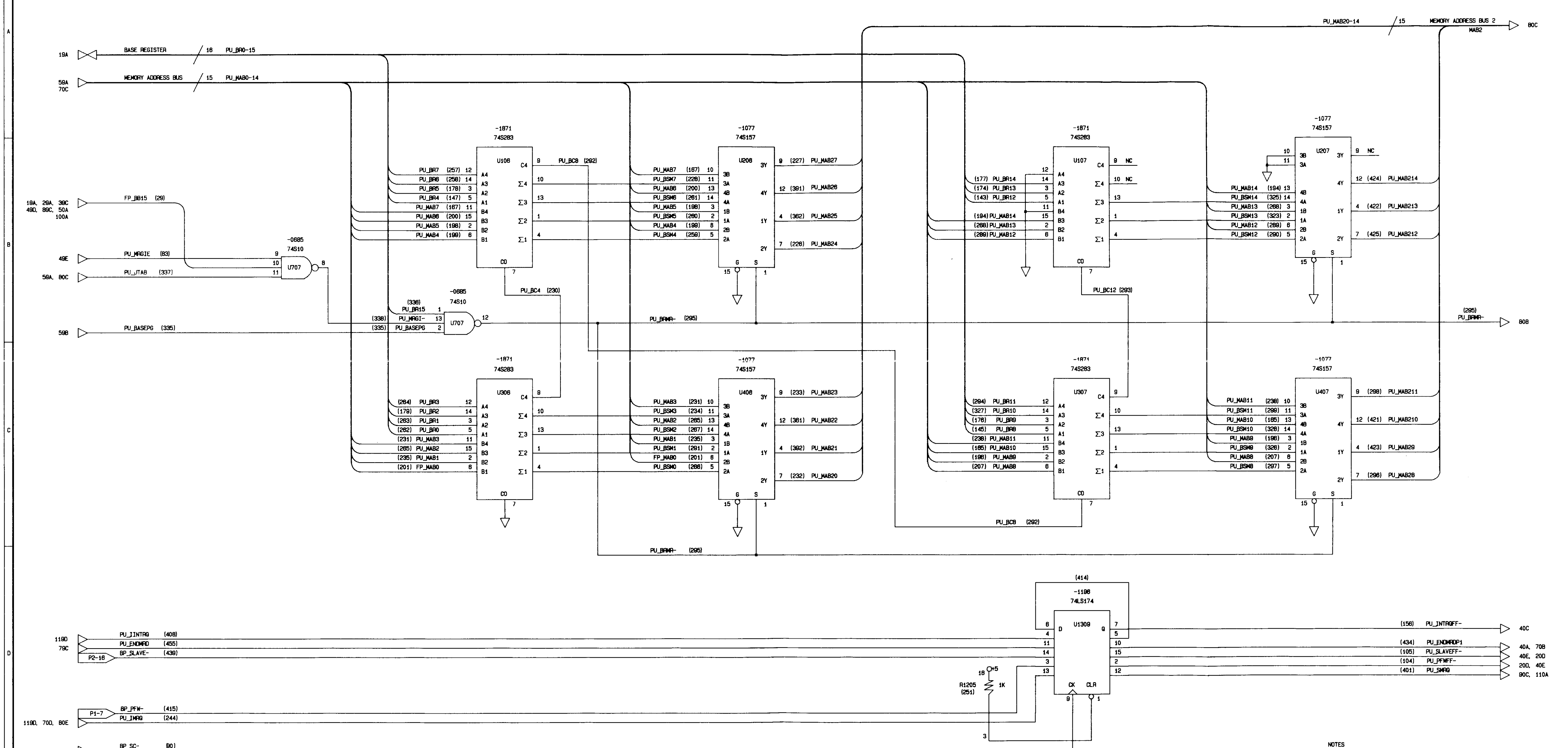
DRAWN BY	DATE 9/28/81	TITLE A700 UPPER PROCESSOR REGISTER FILES	HEWLETT PACKARD
ENGINEER		NEXT ASSEMBLY	PART NUMBER D-12152-60001-53
RELEASE TO PROD		SHEET 3 OF 11	
SUPERSEDES DWG.			



4

DRAWN BY	DATE 10/19/81	TITLE A700 UPPER PROCESSOR IST, TDI, INTP	HEWLETT PACKARD
ENGINEER			
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG.		SHEET 4 OF 11	D-12152-60001-54


NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
APPROVED
DATE
A AS ISSUED
MEMORY ADDRESS BUS
A700 UPPER PROCESSOR
TBG, MAB
DRAWN BY
DATE 9/18/81
ENGINEER
TITLE
RELEASE TO PROD
NEXT ASSEMBLY
SUPERSEDES DWG
SHEET 5 OF 11
PART NUMBER
D-12152-60001-55
HEWLETT PACKARD
5

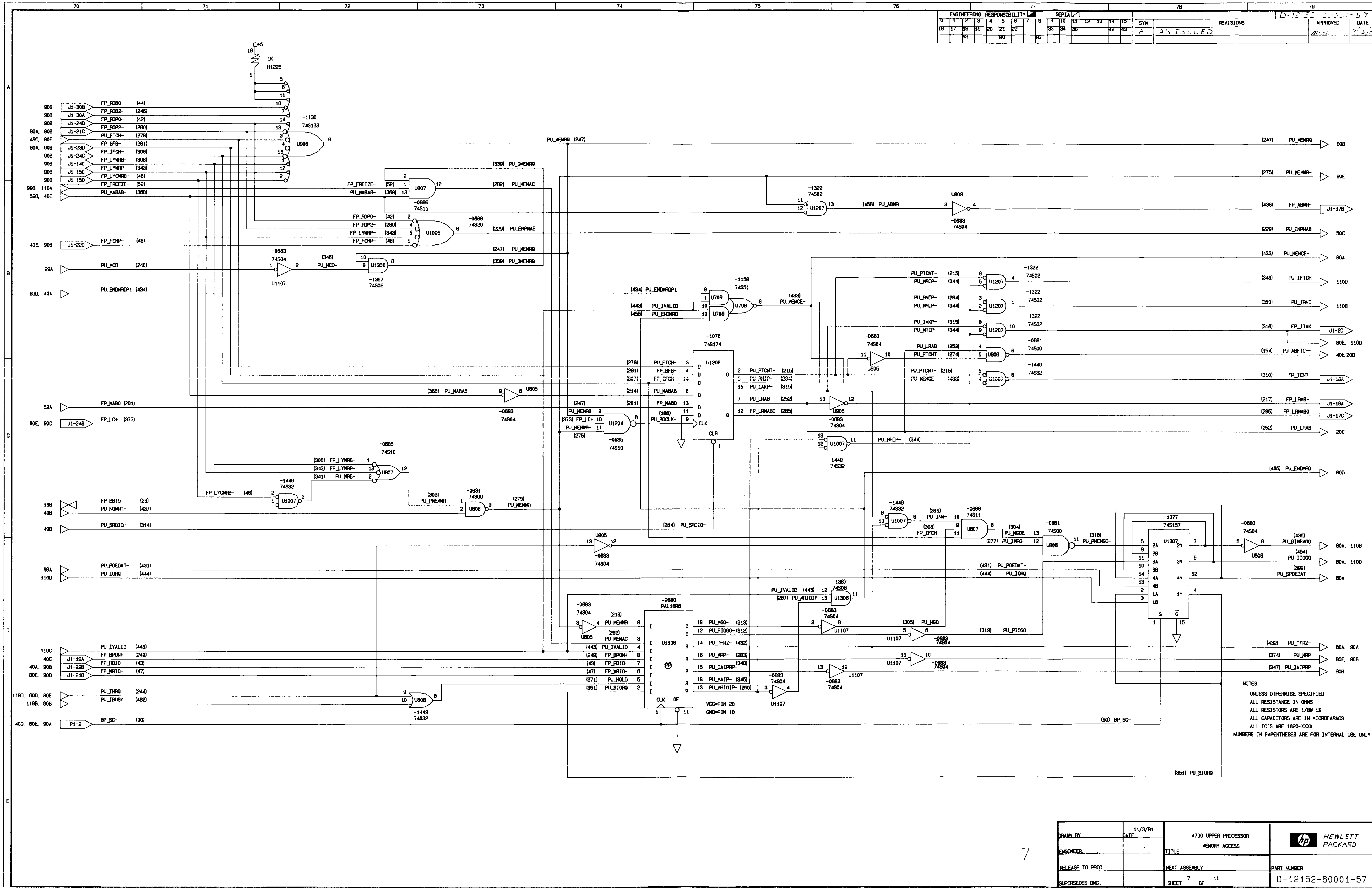


NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		

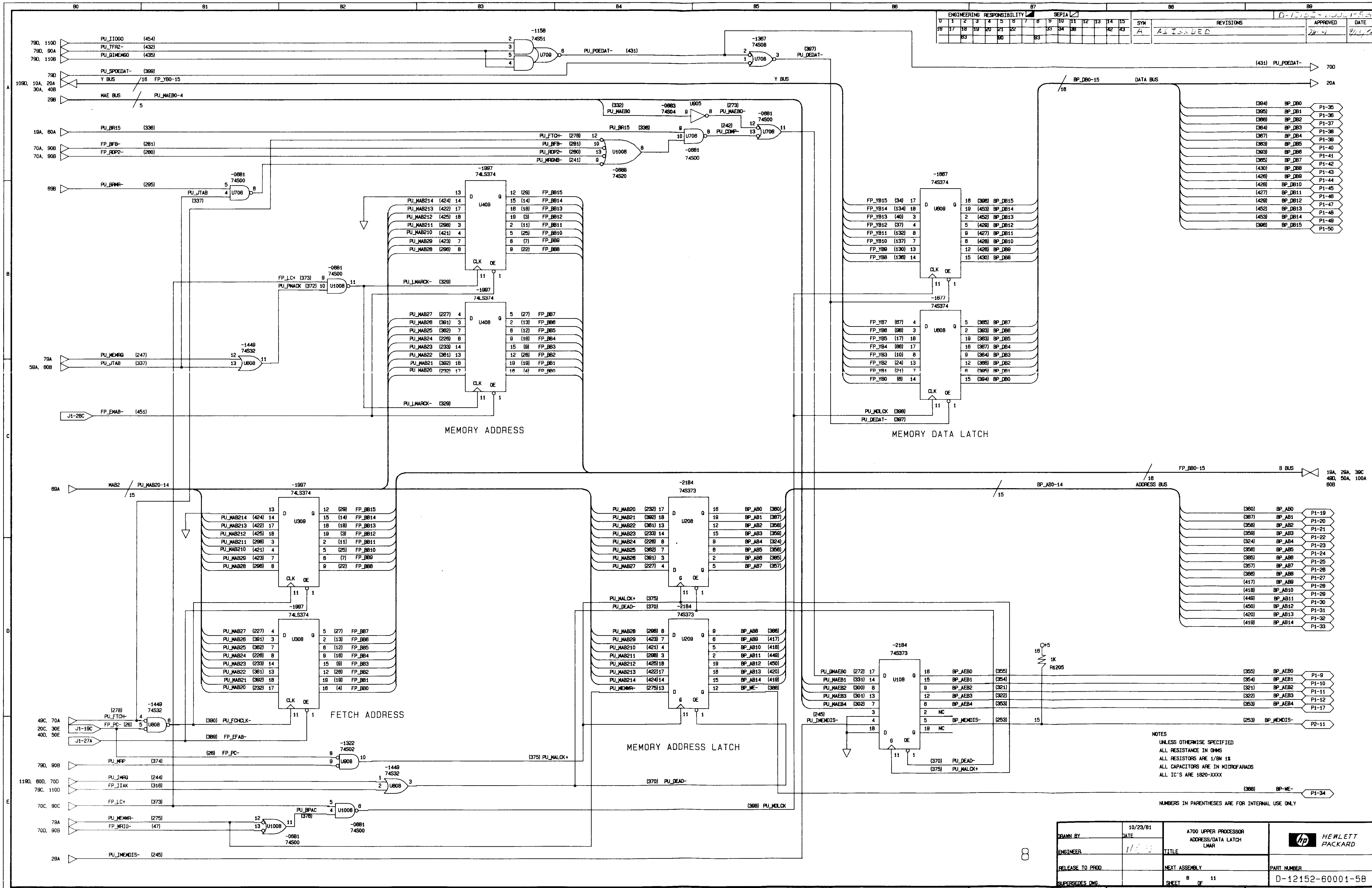
DRAWN BY	DATE 10/13/81	TITLE A700 UPPER PROCESSOR MAB2 GENERATION	HEWLETT PACKARD
ENGINEER			
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG.		SHEET 8 OF 11	D-12152-60001-56

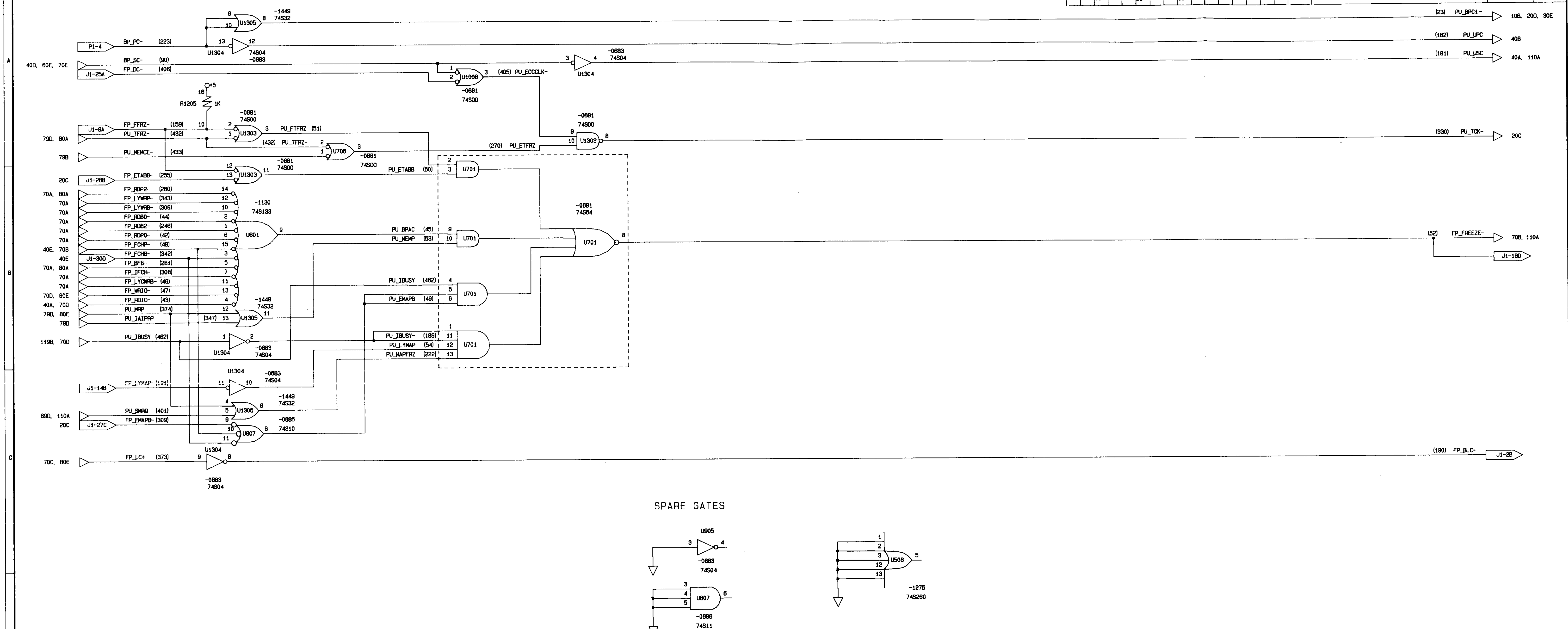
6



ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
A
AS ISSUED
D-12152-60001-57
-1130
74S133
U906
PU_MEMRQ
-0686
74S11
U807
-0688
74S20
U1006
-1322
74S02
U1207
U809
-0683
74S04
-1158
74S51
U709
-1078
74S174
U1208
-0681
74S00
U806
-1449
74S32
U1007
-0685
74S10
U907
U1204
-1367
74S08
U1306
-2880
PAL16R8
U1106
-1077
74S157
U1307
U1107
U805
U808
NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PAPENTHESES ARE FOR INTERNAL USE ONLY
VCC=PIN 20
GND=PIN 10
DRAWN BY
DATE 11/3/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
A700 UPPER PROCESSOR
MEMORY ACCESS
TITLE
NEXT ASSEMBLY
SHEET 7 OF 11
HEWLETT PACKARD
PART NUMBER
D-12152-60001-57

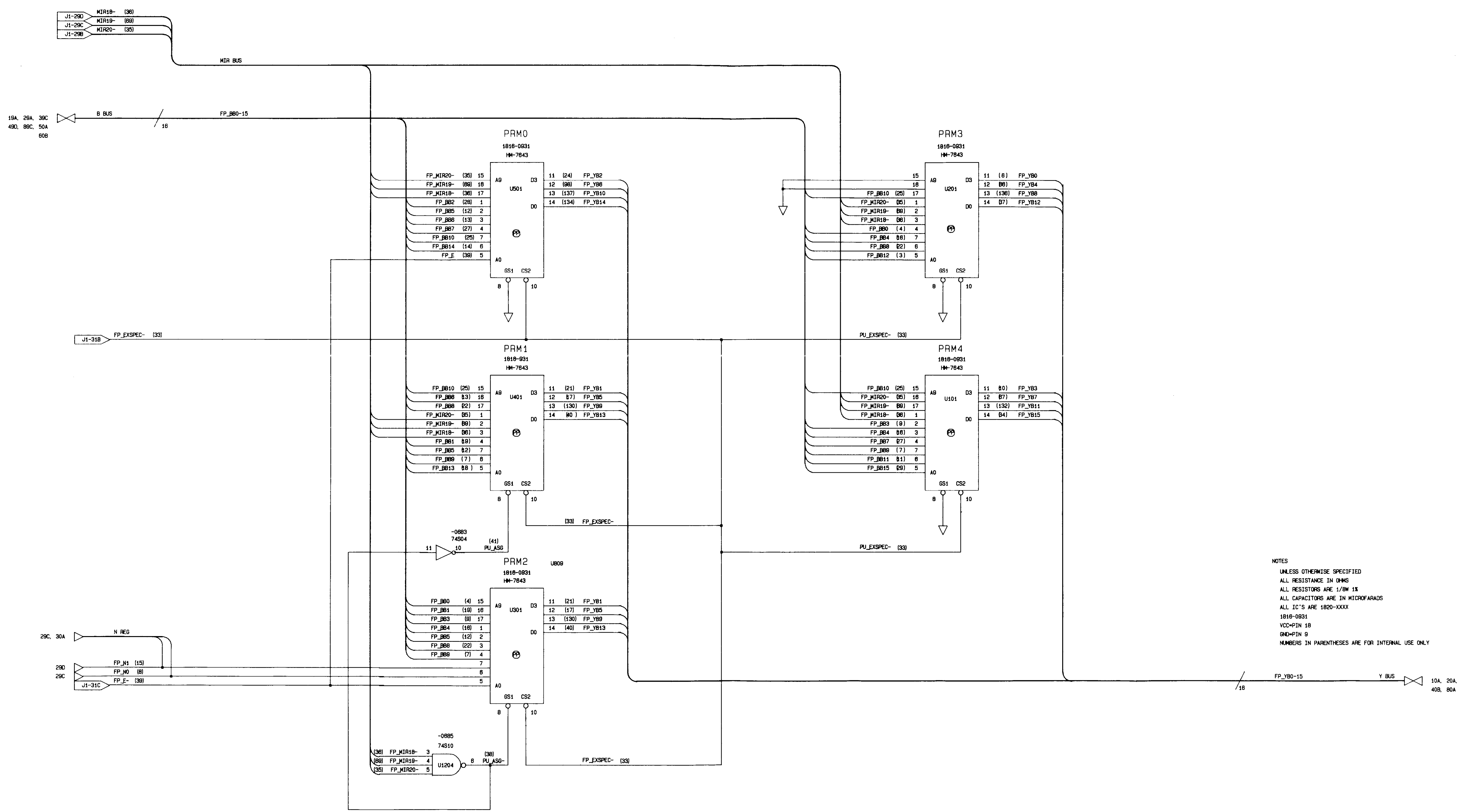
7


MEMORY ADDRESS
MEMORY DATA LATCH
FETCH ADDRESS
MEMORY ADDRESS LATCH
Y BUS
DATA BUS
MAE BUS
ADDRESS BUS
B BUS
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
APPROVED
DATE
A AS ISSUED
NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
DRAWN BY
DATE 10/23/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
TITLE
A700 UPPER PROCESSOR
ADDRESS/DATA LATCH
LMAR
NEXT ASSEMBLY
SHEET 8 OF 11
PART NUMBER
D-12152-60001-58
HEWLETT PACKARD
8



NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

DRAWN BY	DATE 10/25/81	A700 UPPER PROCESSOR TCK, FREEZE	HEWLETT PACKARD
ENGINEER		TITLE	
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER D-12152-60001-59
SUPERSEDES DWG.		SHEET 9 OF 11	



NOTES
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ALL IC'S ARE 1820-XXXX
1816-0931
VCC=PIN 18
GND=PIN 9
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		

DRAWN BY | DATE 10/8/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.

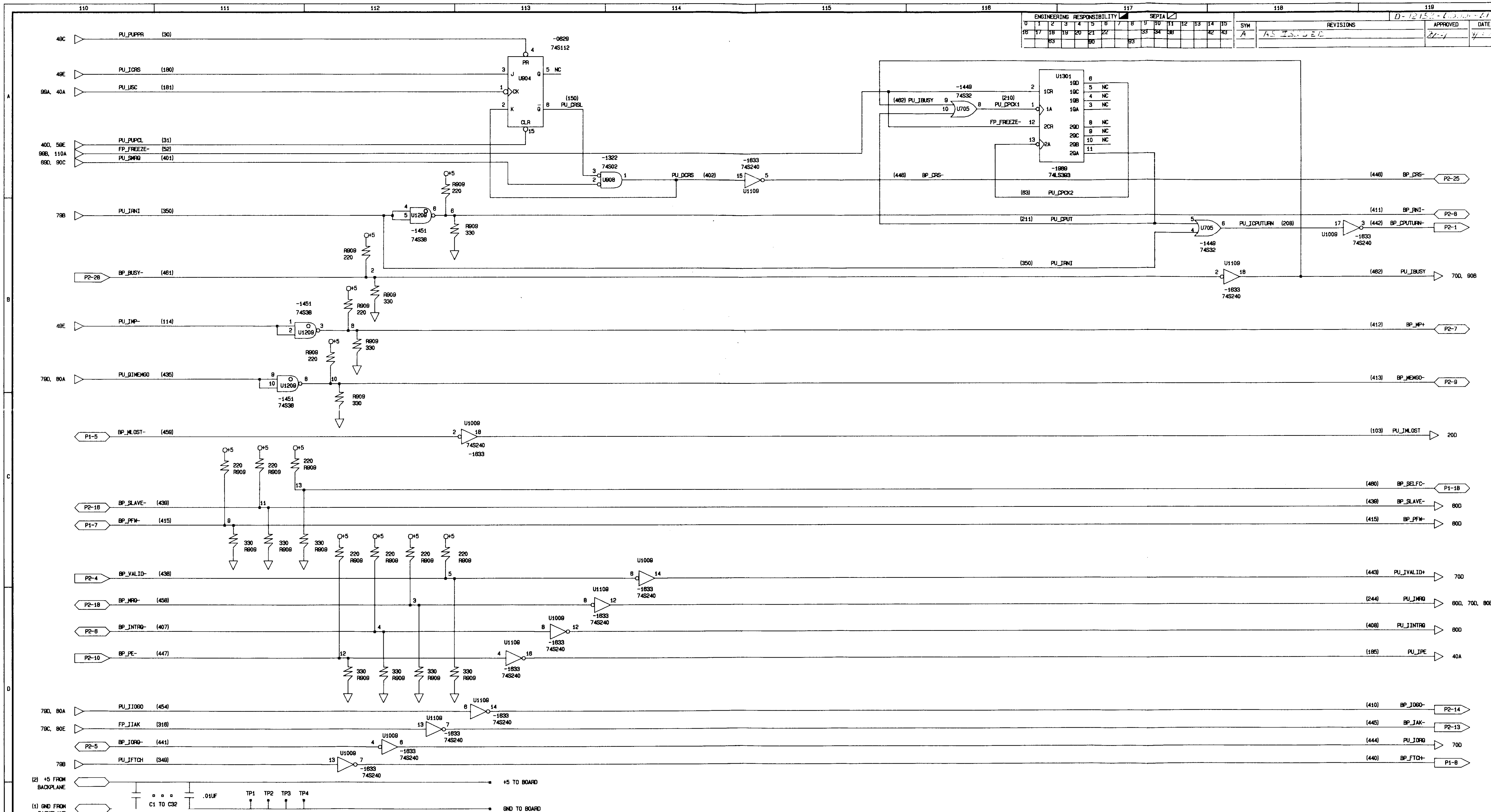
TITLE: A700 UPPER PROCESSOR EXTERNAL ALU OPS.

NEXT ASSEMBLY
SHEET 10 OF 11

HEWLETT PACKARD

PART NUMBER
D-12152-60001-60

10



NOTE 74S240 GATES HAVE ENABLES 1G AND 2G TIED TO GROUND.

BACKPLANE CONNECTOR

NO CONNECT	P1-3	P2-24
	P1-6	P2-23
	P1-15	P2-26
	P2-3	P2-39 THRU P2-44
	P2-20	P2-45 THRU P2-50
GND	P1-13	P2-17
	P1-14	P2-19
	P1-16	P2-21
	P2-2	P2-27
	P2-15	P2-29 THRU P2-34

+5V P2-35 THRU P2-38
220/330 OHMS RESISTORS ARE 1810-0182
RESISTOR DIP +5 PIN 14 GND PIN 7
1K RESISTORS ARE 1810-0256
RESISTOR DIP +5 PIN 16
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

11

DRAWN BY	DATE 10/28/81	TITLE A700 UPPER PROCESSOR BACKPLANE INTERFACE	HEWLETT PACKARD
ENGINEER			
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG.		SHEET 11 OF 11	D-12152-60001-61

5.1 INTRODUCTION

This section covers the memory controller card for the A700 memory system which is also briefly described. The 12103 series memory array cards are covered in Section VI and the 12104A error correcting array is covered in Section VII. To understand the interaction of the memory system with the processor and I/O, refer to Sections II, IV, and X of this manual.

The portion of this section under paragraph 5.2 provides a description of the memory system and its physical characteristics. Electrical requirements of the memory system are provided in Section I of this document. The functional and operational characteristics of the memory system are described under paragraphs 5.3 and 5.4, respectively, and the remainder of the section covers the memory controller card.

5.2 MEMORY SYSTEM DESCRIPTION

The A700 memory system consists of a controller and one or more memory array cards. A minimum memory system would include the memory controller plus one array card. Additional array cards can provide a larger memory capacity. The memory controller card is installed in the A700 backplane immediately above the upper processor card, and the memory array cards are installed above the memory controller card (see Figure 1-2 in Section I). A frontplane is used to connect the address bus between the array cards and controller.

For the frontplane connection, the controller card has two 50-pin connectors and the array cards have one 50-pin connector located at the front. For the backplane connection all cards have two 50-terminal edge connectors located at the rear.

In all cards of the memory system, the signals and data are Schottky-TTL levels and comply with Schottky TTL design rules. The memory controller card (part no. 12152-60003) is shown in Figure 5-1.

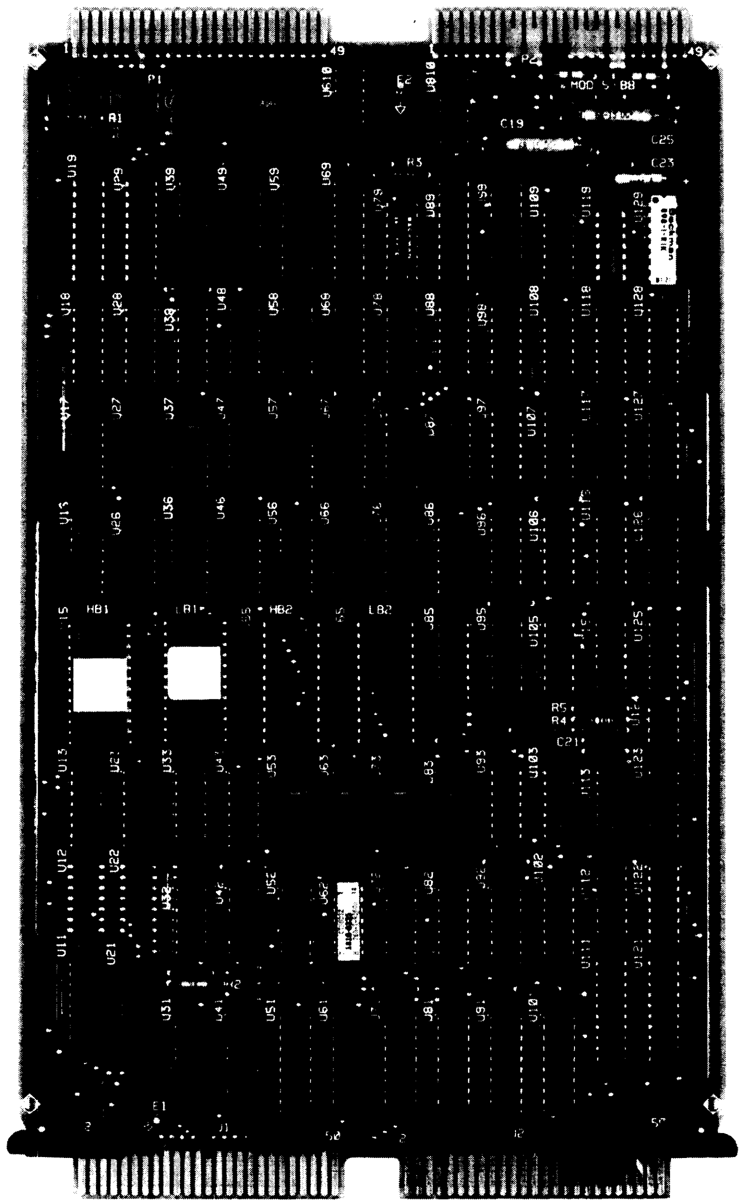


Figure 5-1. Memory Controller Card (12152-60003)

5.3 MEMORY SYSTEM FUNCTIONAL CHARACTERISTICS

5.3.1 BASIC OPERATION

The memory system serves as the main memory of the A700 computer. The memory is dynamically mapped, which provides the ability to store more than 32k words of 16-bit data. Map RAMs on the controller card are used to generate the physical address of data to be accessed during a memory cycle. Mapping extends the 15-bit address bus (which can access up to 32k words of memory) to a 24-bit address bus to access up to 16 Mwords (32 Mbytes) of memory. The memory array cards are word addressable.

Memory accesses can be initiated by either the processor or by an I/O device using DMA. Accesses can be read or write protected by two bits which are stored in the map RAMs. Thus, a processor access to protected memory will cause an interrupt to occur and the access will be stopped and memory protected.

An I/O device using DMA can access protected memory, however. This is true for either a read or write access.

5.3.2 DATA CAPACITY

The format of the data stored in memory is 16-bit words. When data is read, 16 bits at a time are transferred directly to the backplane from the array cards.

Memory system capacity is a function of the number of address lines available. Since there are 24 address lines, 32M byte of memory can be addressed. The amount of memory present in the system depends on the number and type of array cards installed. Due to physical limitations, four array cards can be used in the memory system. Thus, the maximum memory system size using the 1M byte dynamic RAM card is 4M byte of main memory.

5.3.3 MEMORY MODULE ADDRESSING

When adding array cards to the memory system, there is no need to physically identify the array cards (i.e., jumper or switch settings) when installing them in the system. The arrays incorporate a module self-configuring scheme which automatically designates the array card next to the memory controller as the first module and successively designates the remaining modules in ascending order going away from the memory controller. The beginning of memory is, therefore, on the array card closest to the controller and the end of memory is on the array card farthest from the controller.

It is possible to use partially loaded array cards as long as the total memory on the array is either 128k-, 256k-, 512k-, or 1M-bytes. The partially loaded arrays can be incorporated into the module self-configuring scheme. There can be any number of partial array cards in the system.

5.3.4 DATA TRANSFER RATE

A complete memory access to main memory occurs within two SCLK (clock signal) cycles. Therefore, the data transfer rate is dependent on the maximum frequency of SCLK. The shortest period of SCLK possible for proper memory operation in the A700 computer is 250 nanoseconds. The fastest data transfer rate possible, taking into account refresh cycles, is the result of the following expression:

$$\text{ACCESS RATE} = \frac{\text{28 Word Accesses}}{\text{14.5 us}} = \text{1.93M word/s} = \text{3.86M byte/s}$$

5.3.5 MEMORY ARRAY/CONTROLLER INTERFACE

5.3.5.1 Interface to Processor

The interface to the processor is achieved partially on the frontplane and consists of the B-bus and Y-bus, which are used to transmit map information to and from the memory controller.

The processor also interfaces over the backplane to the memory system. Handshake signals transmitted over the backplane are used to initiate memory cycles, provide memory protect and parity error interrupt, and provide data transfer.

5.3.5.2 Memory Data Transfer to I/O

All data transfers to an I/O card occur over the backplane. The memory cycle is initiated by the I/O card and the handshake occurs on the backplane. The 15-bit address sent by I/O is mapped by the memory controller so that I/O can access anywhere in the physical memory space. If a parity error occurs during a memory read access, the parity error interrupt signal is asserted on the backplane and is received by the I/O card. If I/O accesses protected memory, the memory protect interrupt is not asserted and the access is allowed to continue (both read and write). This is not true of memory accesses by the processor.

5.4 MEMORY SYSTEM OPERATING CHARACTERISTICS

5.4.1 HANDSHAKE, DATA AND ADDRESS FORMAT

Before the memory system can be used, the map RAMs on the memory controller must be initialized by the processor. This is necessary since the 15-bit address appearing on the backplane is converted to a 24-bit address by using the address extension bus and map RAMs. The information in the map RAMs can be altered by the processor over the frontplane Y-bus.

All data transfers to memory are handled over the backplane. Data flow to the memory system occurs directly from the data bus to the array cards (i.e., data does not pass through the memory controller to the array card during data transfers). The transfers are controlled by the handshake signals MEMGO, BUSY, and VALID which are also sent over the backplane.

5.4.2 REFRESH OPERATIONS

The characteristics of the dynamic RAMs require memory refreshing for maintaining data. This refreshing must be performed every two milliseconds and be interleaved between requested memory cycles. The refresh operation is transparent in the sense that no handshake signals are asserted (i.e., BUSY) when a refresh is executing unless a memory cycle is requested by the assertion of MEMGO. All rows of memory RAMs are refreshed at one time.

5.4.3 POWER FAIL CONSIDERATIONS

Whenever power is removed from memory, data present in memory will be lost. Under AC power failure with battery backup operation, the +5M backplane voltage must be applied to the memory for retention of data. Under this condition the refresh oscillator on the controller schedules refresh operations so that clock inputs from the processor are not required to maintain the refresh operation. Therefore, for battery back-up operation, only the memory system need be supplied with battery power (i.e., the +5M voltage).

5.4.4 TEST FEATURES

The memory system has access points for production testing. These provide a means for initializing all state devices on the controller and array cards. On the controller, four signal lines are brought to the J1 connector. These connections are located at J1-1-17,19,31,33 (see the the 12152A memory controller schematic at the end of this section).

On parity check memory array cards (except the 1Mb card), a test socket at U213 connects to two test points. (Refer to the memory array card schematic in Section VI). These test points allow the intialization of certain state devices for diagnostic purposes.

On the parity-check memory array card, a green light indicates the parity checking system status. It is lit under normal conditions (no parity error) and is extinguished if a parity error occurs during a memory access. On the ECA card, single-bit errors are automatically corrected, and the green light is extinguished when an uncorrectable double-bit error occurs during a memory access.

For the ECA card, once the light is extinguished it will remain out until reset by the processor. In this way the error event is latched so that field service personnel can identify where the error occurred.

5.4.5 CONTROL SIGNALS

The following control signals are needed for memory operation:

FCLK, SCLK - Processor clocks which are needed to operate the memory cycles synchronously. FCLK (fast clock) is five times the frequency of SCLK (system clock). SCLK must be synchronous with FCLK.

PON - Power on signal. This is necessary to initialize memory properly and to determine standby or normal mode of operation.

CRS - Control reset. Needed to reset the parity LEDs.

MEMGO - Needed to initialize memory cycles (see timing diagram, Figure 5-3).

MRQ - Needed to distinguish between processor or DMA accesses.

MEMDIS - Needed to distinguish between accesses to main memory and the controller ROM.

R/W - Used to select read or write mode.

MP - Used to enable memory protect function of controller.

PS - Used to establish odd or even parity generation (standard array). (It is used on the ECA to inhibit writing of check word data.)

REMEM - Used to inhibit controller during a remote memory access.

5.4.6 INTERRUPT CONDITIONS

The memory controller asserts two types of interrupts; memory protect and parity error. Whenever the processor attempts to access memory that is read protected, the memory protect interrupt will be asserted and the access will be stopped. The normal handshake sequence will be allowed to complete, however, with the memory system outputting all "ones" onto the backplane data bus.

If a memory write is attempted by the processor to protected memory, the interrupt will be asserted, memory will not be altered and the handshake will be allowed to complete. Whenever DMA accesses memory, the access will not be inhibited, whether or not it is to protected memory.

Whenever data is accessed from a standard array module and the parity of data is not correct, the parity error interrupt will be asserted.

In the case of a data access from an error correction array card, the parity interrupt will occur if a double-bit (non-correctable) error is detected. Single bit errors do not cause parity interrupts since the error is automatically corrected by the ECA card.

5.5 CONTROLLER CARD OPERATION

The controller card contains several sections including the external registers of the processor, mapping system, map RAMs, read-write protect, boot RAM and ROM, timing and control, parity generator and comparitor, and dynamic RAM refresh circuitry. These circuit areas are shown in the block diagram of the controller, shown in Figure 5-2.

5.5.1 EXTERNAL REGISTERS

The special-purpose external registers of the processor are located in the memory controller and communicate with the processor over the frontplane bus when executing microorder SRIN in a microinstruction.

The registers are defined as follows:

0 MPAR: Map address register which can be written to and read from. It contains the 10-bit address presented to the map RAMs for processor access to the map registers. Any read or write to the maps increments MPAR. (Bits 10 - 15 are always zero.)

1 PEL1: parity error latch is a 16-bit read-only register containing the low 16 bits of physical address where the last parity error occurred. It is updated even if parity interrupts are disabled. Addresses are latched for both DMA and processor errors.

2 PEL2: parity error latch 16-Bit read-only register containing the high 8-bits of physical address of the last parity error. This address is stored in the low eight bits of the register, and the remaining 8 bits are always 0.

3 CIL: central interrupt latch read-only register containing the trap cell address of the last I/O interrupt. The microcode uses this address to update the central interrupt register located in the register file (controlled by base set microcode).

4 - B Reserved for HP.

C - F Reserved, access to the floating point processor.

5.5.2 MAPPING SYSTEM

The mapping system is the means by which the memory controller can provide a physical address equal to the maximum possible size of main memory array. The map system is composed of 16 high-speed static RAMs which convert (or map) the logical address received from the backplane into a 24-bit address. There are 32 maps with 32 address locations that can address up to 32 Mbytes of physical memory as described in paragraph 5.6.1.1.

In the address mapping operation, a 15-bit logical address word is divided so the lower-order bits are used directly where bit 0 of the backplane logical address is bit 0 of the physcal address. The upper-order five bits of the backplane address are used in combination with five bits from the address extension bus to select a map RAM location containing the upper-order 14 bits of the extended physical address of the memory location to be accessed. The 24-bit address is sent to the array cards over the frontplane.

The map RAMs are loaded from the processor Y-bus under control of the processor only. The memory accesses are timed so that the processor may access (or change) the map addresses during memory cycles.

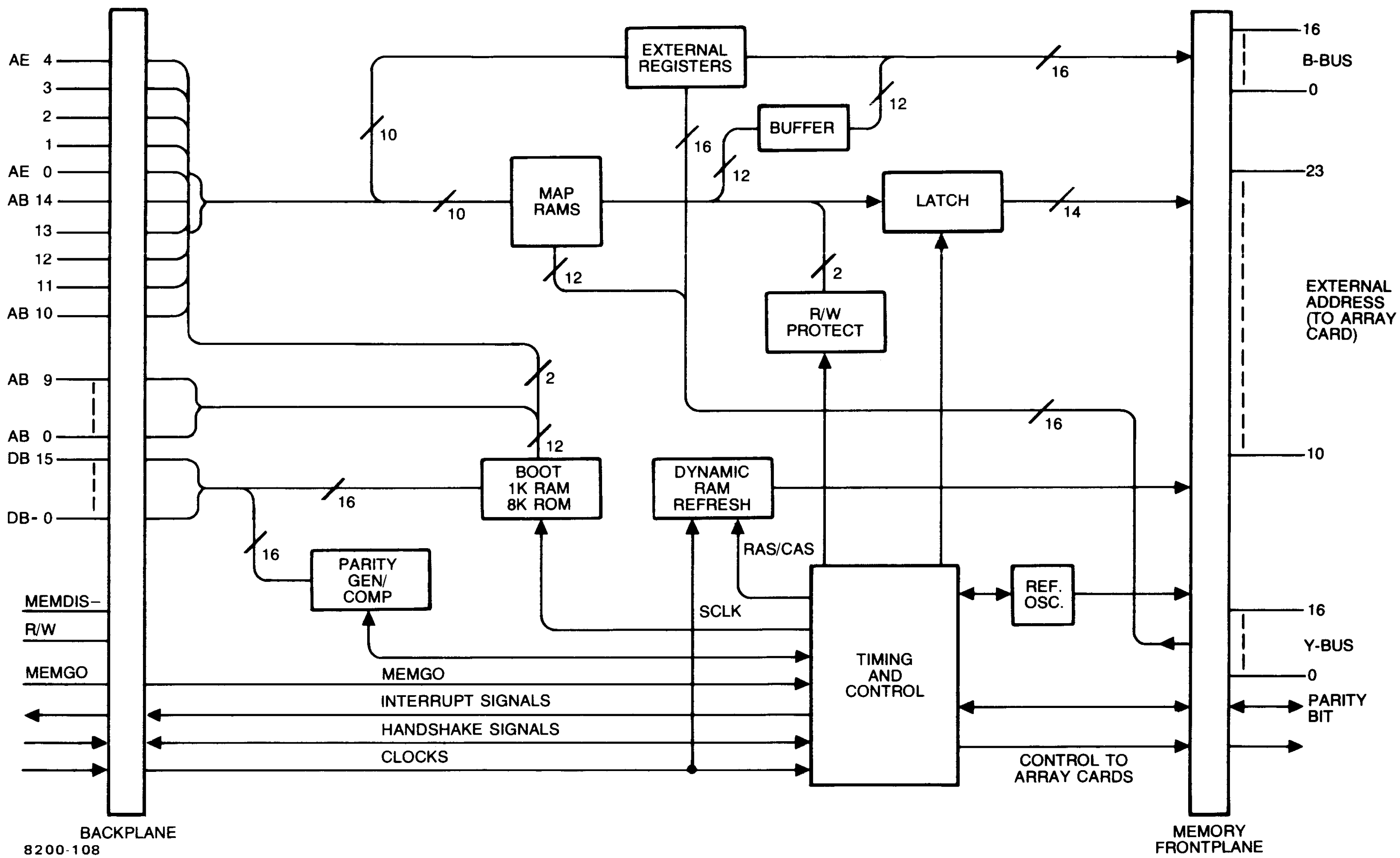


Figure 5-2. Memory Controller Functional Block Diagram

5.5.2.1 Map Address Latch

During a normal memory access, (i.e., an access with no hold-offs due to refresh) the logical address on the backplane accesses the map RAMs and the extended address is sent to the array cards. After the assertion of MEMGO- is complete, the logical address is no longer valid, but the extended address must remain valid for the remainder of the memory cycle. This is necessary to keep the appropriate array card selected for driving the requested data onto the backplane. The extended address is, thus, latched on the memory controller at the end of MEMGO so that the memory access can complete. At the same time, this frees the map RAMs so that they can be accessed by the processor during the pending memory cycle if so desired. It is in this way that the processor can modify the contents of the map RAMs during a pending memory cycle.

5.5.2.2 Read-Write Protect

Two of the map RAMs are used to store the read-write protect status bits which control the access of protected areas of memory. These RAMs are written to at the same time as the address map RAMs and are accessed in the same manner. During any processor access to memory, these bits, if set, will prevent a memory access from occurring.

The mechanism by which this occurs is as follows: As the logical address accesses the map address RAMs, it also accesses the read-write protect bit RAMs. If either bit is set, then the requested read or write is inhibited. In the case of a write cycle, the aborted write will not cause any change of data in main memory. In the case of a read cycle, the aborted read will cause the memory controller to drive all "ones" (octal 177777) on the backplane data bus. However, a read can occur from write protected memory and a write can occur to read protected memory. In the case of a DMA access by a peripheral device, the protect bits are ignored.

5.5.3 CONTROLLER ROM AND RAM

The memory controller contains 1k-words of static RAM (refresh not needed) and 8k-words of ROM space. The ROM is used for the storage of front panel code, and for the storage of boot loaders.

The RAM is used for bootstrap loading, diagnostic purposes, and for the storage of error syndrome codes from the ECA cards.

The 1k-words of static RAM is accessed by the assertion of MEMDIS- on the backplane and the assertion of a base page address (0-1777, octal) on the address bus. Reading or writing of data into the RAMs is controlled by the R/W bit on the backplane.

The 8k-words of ROM space is accessed by asserting MEMDIS- on the backplane along with an address greater than 8k but less than 16k (20000 to 30000, octal) on the address bus. The sense of the R/W bit is unimportant in this case.

Memory accesses to the controller ROM and RAM are the same as those to main memory with the exception of the assertion of MEMDIS- on the backplane. Also, since the address may select one of the array cards in the main memory array, the controller inhibits any array card from driving the backplane data bus during a boot access.

The memory controller performs the access to either ROM or RAM in three SCLK cycles instead of two. This is necessary since the ROMs have slower access time than that of the main memory.

5.5.4 PARITY GENERATION AND DETECTION

Parity bit generation is performed by the memory controller for both read and write. In write operations, the parity generators monitor the data on the backplane during every write cycle. The parity bit is then generated and sent to every array card over the frontplane shortly after the data is valid on the backplane.

As the write cycle continues, the appropriate main memory array card is selected and the parity check bit is written into the parity RAM along with the 16-bit data word on the same array card. (In the case of an ECA card, the parity check bit is generated but is not used by that card.)

Read parity detection is done using the same set of parity generators as used for write. As the array card drives the requested data onto the backplane, the parity generators monitor it for correctness. At the same time, the parity check bit from the array card is sent to the memory controller over the frontplane. The parity generators compare the check bit with the data on the backplane to insure proper parity. If an error has occurred, the error condition is latched and the parity error signal, PE-, is asserted on the backplane after the release of VALID-. Also, the parity LED on the array card which was responsible for the parity error is extinguished.

In the case of an ECA card access for a read, the parity detectors still monitor the accessed data on the backplane but since the ECA card does not return a parity bit to the controller, the controller is inhibited from flagging a parity error interrupt. However, when a non-correctable (double-bit) error occurs on the ECA card, the ECA card informs the controller to assert a parity error interrupt.

To summarize, the memory controller asserts a parity error interrupt whenever a parity error occurs on a standard array card and when a double-bit error occurs on an ECA card. Both these occurrences indicate that accessed data is in error. The faulty array card will have its green parity indicator light extinguished.

5.5.5 REFRESH CIRCUITRY

The main memory array is composed of dynamic RAMs which require periodic refreshing for the retention of data. The memory controller schedules and performs the refresh function on all array cards simultaneously.

While AC power is applied to the computer system, the controller derives the refresh period by dividing the system clock using a counter. Thus, when a refresh is due, it is performed synchronously. If a memory cycle is in progress when a refresh cycle becomes due, the refresh waits until the pending memory cycle completes. On the other hand, if a refresh is executing and a memory cycle is requested, the memory cycle is held-off until the refresh completes. The requested memory cycle is then executed.

When AC power is removed from the computer system and there is a battery back-up system installed, the memory controller still refreshes memory by generating its own refresh clock. This is accomplished by an oscillator which is started the moment that standby status is achieved. In this manner, the memory controller can do synchronous refresh cycles during power-up and not depend on the system clock for refresh scheduling during power-down.

5.5.6 TIMING AND CONTROL

Timing and control refers to the circuitry necessary for the complete function of the memory controller. It is responsible for the following functions:

1. Generate handshake signals for backplane (BUSY, VALID).
2. Latch data and address during memory cycles.
3. Generate interrupt signals (MPV, PE).
4. Arbitrate memory and refresh cycles.
5. Generate read strobes for array cards.
6. Protect memory during illegal accesses.
7. Store error syndrome information in boot RAM.
8. Access loader and front panel firmware.
9. Inhibit array cards during protected accesses.
10. Inform the processor to extend the backplane clock during error correction cycles.
11. Maintain memory data during power failures.
12. Verify that physical address indeed accesses an extant array card and if not, drive all "ones" onto the backplane.
13. Determine whether the requested memory cycle should occur in two or three SCLK cycles.

The circuitry is composed of seven flip-flops and several gates. Figure 5-3 shows the sequence of events for a typical memory cycle which illustrates the following:

1. MEMGO is received from the backplane.

2. BUSY and CYCLE flip-flops are set at the beginning of the short-half cycle of SCLK. CYCLE immediately sends the RAS signal and to the array cards. BUSY is set on the backplane.

3. One FCLK cycle later, the data IN A DMA cycle at the memory array is latched by DLATCH. (for a processor write, the latching occurs two FCLK cycles later.)

4. Also, at this time, VALID is asserted on the backplane. (Two cycle access)

5. One FCLK cycle later, the output buffers on the selected array card are enabled by OUTEN- to drive data onto the backplane (read cycle). If a memory protect violation occurs, the memory protect signal MPV- is asserted and held for one system clock cycle.

6. One FCLK cycle later, the CAS enable signal CASEN- is sent to the array card. (write cycle).

7. One FCLK cycle later, accessed data is about to become valid on the backplane. If error correction is required, the EC- signal is generated and SCLK is extended (Figure 5-4).

8. On the leading edge of the next short-half-cycle of SCLK, both BUSY and CYCLE are de-asserted. This starts the ending sequence with valid data on the backplane.

9. One FCLK cycle later, the trailing edge of VALID occurs, completing the handshake. If a parity error is present in the accessed data, the PE- signal is asserted here for two FCLK cycles.

10. One FCLK later, the output buffers are disabled (OUTEN- is de-asserted). If a parity error has not occurred, the cycle completes at this point.

11. In the case of a parity error, the PE signal asserted in step 8 is asserted for the FCLK cycle following the normal termination at step 9.

12. In the case of error correction, the backplane SCLK is extended and the error syndrome code is written into the boot RAM at the trailing edge of the extended VALID signal.

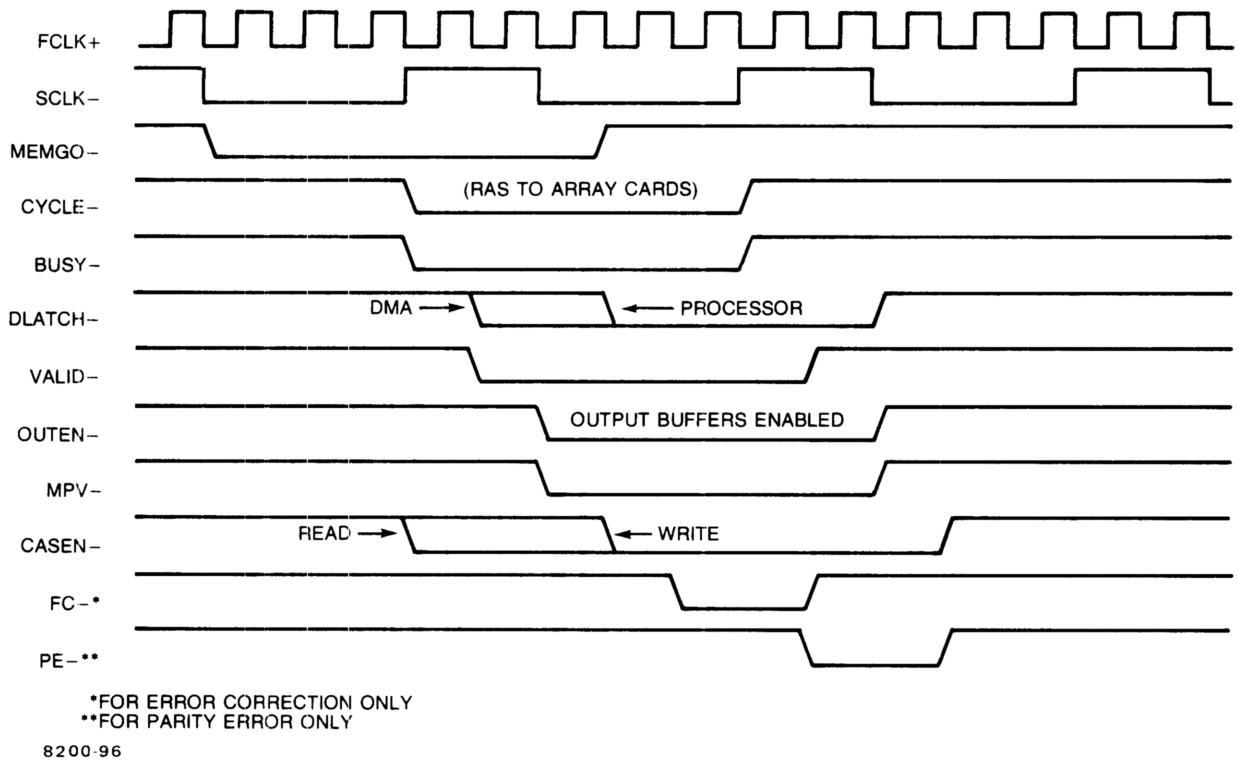


Figure 5-3. Memory Controller Timing Control

5.6 CONTROLLER CARD THEORY OF OPERATION

The A700 computer memory controller card theory of operation is covered in the following paragraphs (see Figure 5-2 and the schematic of the memory controller at the rear of this section of the manual). The integrated circuits (chips) are referenced by their U-numbers and schematic locations. For example, U69 (13-C) means chip U69 on schematic sheet no. 1 is located by coordinates 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc. and on sheet no. 2 it is numbered 20, 21, etc.

5.6.1 MAPPING SYSTEM

5.6.1.1 Page Address Generation

The mapping system of the A700 memory controller is the means by which the physical address sent to the array cards is generated. It converts the backplane address bus and the backplane address extension bus into the upper-order 14 bits of the physical address. The lower-order 10 bits of address are used directly from the backplane address bus where Bit 0 the logical address equals Bit 0 of the physical address.

The map system is implemented using sixteen 1k x 1 static RAMs. These map RAMs are accessed in parallel so that 1k of 16-bit words are stored in them. The lower-order 14 bits are used as the map address while the remaining two bits are the read and write protect bits (see read-write protect in paragraph 5.6.1.3).

Data consisting of the desired physical addresses is stored in the map RAMs from the processor Y-bus during system initialization. This data is really the physical memory address (upper-order bits) that is sent to the array cards. In this way, the processor can assign (map) a given backplane address to an arbitrary physical address in the main memory array. This assignment can be easily changed by changing the contents of its map RAM location.

A map is composed of 32 16-bit word locations in the map RAMs. The upper-order five bits of the backplane address bus (bits 10-14) select one of the 32 locations within the map. The five bits of the address extension bus select one of 32 maps. Thus, the 1k storage in the map RAMs is divided into map and map location selection to provide physical addressing from 32 maps each containing 32 words. Since the 14 bits stored in the map RAMs are used as the upper order bits of the physical address, each map word corresponds to a page (1k block) of physical memory.

The map RAMs are U16 through U86, and U17 through U87 on the controller card.

The address to the RAMs can be derived from either the backplane address and address extension busses or from the memory address register which is also located on the controller card. This is accomplished by U18, U28, U38 (31-B, -C, -D) type 74S158 multiplexers and U98 (31-C), a type 74S51 gate used as a multiplexer.

For any main memory access, the multiplexers select the backplane addresses. Whenever the processor changes or verifies the contents of the map RAMs, the address is selected from the map address register. The multiplexer is switched by the GMGO+ signal, so that whenever GMGO+ is asserted (during a main memory access) the multiplexer selects the backplane address. At all other times the multiplexer selects the map address register to the map RAMs.

The GMGO+ signal is generated by U106-3 (19-A). When a main memory access is in progress, MEMGO- is asserted on the backplane which is routed through U99-5 to U106-2. The OUTEN- signal is sent to U106-1 to gate the MEMGO+ signal. This is needed to make the trailing edge of GMGO+ occur at a definite time since the trailing edge of MEMGO+ is not tightly controlled. (MEMGO- on the backplane is driven by an open-collector driver.)

5.6.1.2 Mapped Address Latch

As the map RAMs are accessed during a main memory cycle, the contents of the RAMs are sent to the array cards as the upper part of the physical address described earlier. This part of the physical address is used to select the desired array card. The array card must remain selected for the length of the memory cycle. However, the output of the map RAMs is valid only when their input addresses are valid; i.e., the time MEMGO- is asserted on the backplane. Therefore, the output of the map RAMs must be latched and held for the length of the memory cycle. This is the function of the Mapped Address Latches U13, U23, U33, U43 (36-D, -C, -B, -A). These are 74S157 type multiplexers connected as latches where the outputs are fed back to one of the inputs.

The latch is controlled by the ALATCH+ address latch signal (refer to Address Latch Signal, paragraph 5.6.6.4). The Mapped Address Latch is a transparent latch so that as soon as the mapped address is available it is sent to the array cards; i.e., no clocking is necessary. The output of the latch is sent to the frontplane address drivers U21 (37-C) and U41 (37-D).

Once the mapped address is latched, the map RAMs can be accessed by the processor for either changing or verifying their contents. This is true even though the controller is in the process of accessing main memory. The output of the map RAMs is connected to drivers which connect to the processor's external B-bus (on the frontplane). These drivers are U51 (38-B) and U61 (38-B) and their selection is controlled by the EMAPB- signal.

5.6.1.3 Read-Write Protect

The Read and Write Protect status bits are stored in two separate map RAMs providing 1024-words of read-write capability. The RAMs used are U16 (32-A) and U26 (33-A) for read and write protect, respectively. Their function is to store the status of map addresses as either read or write protected (or both) so that the processor can tell the read-write protect status during every processor access to main memory. They are stored in the map RAMs in the same manner as the map addresses and are changed, verified and latched the same as the mapped addresses described in the previous section. For a description of the read-write protect interrupt function, refer to paragraph 5.6.6.12 on timing and control.

5.6.1.4 Selection of Map Zero

When an interrupt occurs from a peripheral device, it is necessary to process the interrupt through memory map 0. The interrupting devices are forced to map 0 by allowing the self configuring bit on the backplane to select map 0 whenever it is asserted. This is accomplished by routing the SELFC- from the backplane to the enable inputs of U18 (31-B) and U28 (31-C) multiplexers. This signal (MP0+ on the controller) when asserted high, causes the outputs of the MUXs to go to the high state which corresponds to zeros on the map RAM address bus.

This happens on map address bits A15-A19 which are the map selection bits derived from the backplane address extension bus. Thus, regardless of what is present on the backplane address extension bus, the assertion of the SELFC- signal during a memory access causes the access to occur through map 0.

5.6.2 BOOT RAM AND BOOT ROM ACCESSES

5.6.2.1 Selection of Boot Mode

The boot mode of the memory system is selected by the assertion of the MEMDIS- signal during a memory access cycle. The MEMDIS- signal informs the controller that the present memory access will be made to either the controller RAM or controller ROM instead of the main memory array. In this case, the main memory array cards are inhibited from driving the backplane data bus and the data driven onto the data bus will come from either the boot RAM or ROM (read cycle). If the required boot access is a write, then the data on the backplane will be written into the boot RAM.

While in boot mode, the selection of either RAM or ROM access for a read is determined by the backplane address bus. (For the ROM access, a write is meaningless.) If the address on the backplane references the base page,(i.e. <1777 octal) then the access will be to boot RAM. If the address references locations between 8k and 16k (20000 to 30000 octal), then the access will be to boot ROM. To distinguish between the RAM and ROM modes, address decoding is done. The backplane address is used to select locations in both boot RAM and ROM and is also used to select between the two modes; i.e., mapping is not done in the boot mode.

5.6.2.2 Boot Address Latch

The backplane address must be latched for the entire boot cycle. For the lower order 10 bits, this is done in the latches U19 (25-B) and U29 (25-A). For address bits 10,11,12 and 13 this is done at the quad flip-flop chip U48 (22-A). The lower order bits are sent to both the RAM and ROM and are used to select 1k locations. Bits 10 and 11 are also sent to the ROMs since they have 4k of storage. Bit 13 (the 8k bit) is used to determine if the access is to ROM or RAM. If this bit is set, then U48-13 (22-A) is low, disabling the RAM select gate at U103-1 (23-B).

The ROM mode is enabled by U48-14 (22-A) which, in turn, enables the ROM gates at U58-4 and U58-10. Also, bit 12 is used to distinguish between which 4k set of ROM is being accessed by enabling gates U58-5 (23-A) and U58-9 (23-A) exclusive to each other. Thus, the latch forms a hardware interlock so that no matter what address appears on the backplane, only one set of RAM or ROM is selected at one time. The latch at U48 (22-A) is controlled by ALATCH-. (Refer to paragraph 5.5.6 for timing details.)

The output at U58-6 selects the lower 4k of boot ROM. The output at U58-8 selects the upper 4k. The boot RAM is selected by the output at U103-12. The select signal goes indirectly to the chip select inputs of two of the boot RAMs through AND gate U105-5 (24-B). The other input of the gate, U105-4, receives the SYWR- signal.

The SYWR- signal is asserted when an error syndrome code is written into boot RAM during an error correction cycle.

The "write enable" inputs are similarly gated to allow error code storage as well as normal boot RAM writes from the processor.

5.6.3 CONTROLLER DATA BUS

The controller has an internal data bus which is used for both input and output of data to the backplane. The backplane data is received through latches U49 (21-D) and U59 (21-C) which then drive the data onto this bus to the boot RAM and to the parity generator/detectors. This bus is also received by two buffers, U69 (27-D) and U89 (27-C), which then drive the backplane data bus. Thus, this internal data bus is bidirectional in that it can receive data from the backplane and also drive data onto the backplane. To illustrate this, the different operating modes will be described.

First, when an access to main memory takes place, the internal data bus is set up to receive data from the backplane. In this case, latches U49(21-D) and U59 are enabled on to the bus and buffers U69 and U89 are disabled from driving the backplane data bus.

For a read from main memory, data appears on the backplane and appears on the internal data bus to be presented to the parity circuits for parity checking. For a write to main memory, data appears on the backplane from the processor or I/O device and appears again at the parity circuits for generation of parity to be stored into memory. Refer to paragraph 5.6.4.1 for a detailed discussion of the parity circuit.

Next, when boot mode is selected, data to be written into boot RAM appears on the backplane data bus and appears on the internal bus at the input of the boot RAMs. If a read is desired, then latches U49 and U59 are disabled and the buffers U69 and U89 are enabled onto the backplane by the RM+ signal. Data from the boot RAM or ROM is then routed onto the backplane to be read by the processor.

Lastly, when error codes from an ECA card are stored into the boot RAM, they are driven onto the bus by driver U31 (28-B).

5.6.4 PARITY CHECKING

The controller utilizes parity checking to verify the integrity of data stored in the memory system. The circuitry used to generate and check parity is located on the controller while the parity bit itself is stored in main memory along with the corresponding data bits (standard memory only).

During a write to main memory, the controller monitors the data to be written into memory and generates the appropriate parity bit to be stored with this data. During a read access, accessed data is monitored to verify that the accessed parity bit is indeed correct. If it is not correct, then a parity interrupt is generated by controller.

5.6.4.1 Parity Generation

During a write access to main memory, data is sent by the processor or I/O device over the backplane data bus. The data bus is received on the controller card by U49 (21-D) and U59 (21-C). These transparent latches then pass the data to the controller internal data bus which is monitored by two parity generation circuit chips, U68 (11-A) and U78 (11-B). These chips are 9-input parity generator/detectors, so two are required to determine parity for a 16-bit data word. Each chip receives eight data bits from the bus. The ninth bit on one chip is used to receive the parity sense signal from the backplane and the ninth bit on the other is used to receive the parity bit from the array card during a read access. It is always low during a write access.(parity generation)

The parity generators each have two outputs; one designated E and the other designated O. These outputs are true (high) if the number of set inputs is an even or odd number, respectively. For example, if the octal number 377 is present on the input, (eight bits set; assume the ninth is low) the E output will be set, signifying that an even number of bits are set. Similarly, if the octal number 111 is present on the inputs, then the O output will be set. All zeros on the input will produce the O output since zero is considered an even number. Based on this, the parity bit generation is described below.

5.6.4.2 Parity Bit Generation

The parity mode for the memory system is odd parity. This means that any data word written into memory plus its corresponding parity bit must have an odd number of bits set. At the time data is stored into memory, it must be determined if the parity bit should be set or cleared to produce this odd number. Eight inputs of U68 (11-A) receive bits 0 through 7 of the data word. The ninth input is used to receive the parity bit stored in memory during a read access to memory and is always low during a write.

Eight inputs of U78 (11-B) are used to receive bits 8 through 15 of the data word and the ninth bit is used to receive the parity sense signal from the processor. This bit is normally high. If the number of bits set in the data is odd, one set of data lines must have an odd number of bits set and the other must have an even number of bits set. In this case, either the two generators will have both E outputs set or both O outputs set. If the number of bits in the data word is even, then each set of data lines must have an odd number of bits set or an even number of bits set. In this case, the outputs of the two generators will be opposite (i.e., the E output of one will be set and the O output of the other will be set, or vice versa).

The previous description shows that when the outputs of the generators agree, the parity of the data word is already odd and the parity bit need not be set. At all other times the parity bit should be set.

A Boolean equation for the parity bit can be written:

$$(E1 * E2) + (O1 * O2) = P- \quad \text{(complement of P)}$$

This function is readily implemented by a 74LS51 type 'and-or invert' gate U88 (11-B). Thus, the outputs of the parity generators are combined by this gate and the output U88-6 is used as the parity bit to be stored into memory. This bit is sent out over the frontplane to all the array cards to input U32-8 (19-A).

5.6.4.3 Parity Detection

Parity detection is performed on every read access from a standard array card. As data appears on the backplane from an array card, this data is received by the transparent latches U49 (21-D) and U59 (21-C) which then send it to parity detectors U68 (11-A) and U78 (11-B). Also, the parity bit stored in memory is sent to the controller via the frontplane as the PCK- signal and is received by U106-10 (12-A). Since this is a read access, the RE+ signal is true which enables AND gate U106-9 presenting the parity bit as the ninth input to U68.

The parity of the data word plus parity bit must be odd indicating that accessed data is correct. The parity bit is inverted when it reaches the input of the parity detector; therefore, data is correct if the number of bits set is an even number. As previously explained, an even number of bits set into the parity detectors will cause the detector outputs to be the opposite and produce a high at the output of the parity bit gate U88-6 (12-B). Thus, the condition for correct data is that this output should be high during a memory access.

The parity error flip-flop U126 (12-B) monitors the parity bit gate output through the AND/OR invert gate U88 (11-B) which inverts it. When the trailing edge of the VALID- signal occurs, it latches the parity check status. If the parity check status is low at U88-6, meaning parity error, the output at U126-9 will go high enabling the parity error signal from U116-1 (19-B).

The physical address of the parity error is stored in parity error latches U71, U81, U91 (47-A, -B, -C).

5.6.4.4 Parity Disable

When an error correcting array (ECA) card is accessed by the controller, the controller parity function is not used for either read or write. During write accesses to an ECA card, the parity generator produces a parity bit but it is not used by the ECA card. During read accesses from an ECA card, the parity detection function is disabled on the controller. This is caused by the parity disable signal sent by the ECA card to the controller. This signal is received on the controller by U32-1 and -2 (11-B) and is sent inverted to U88-1 and -13 (11-B). This forces the output at U88-8 low, so that the parity error flip-flop cannot be clocked high, thus inhibiting any parity interrupt.

5.6.5 ERROR LOGGING

When an ECA card is installed in the system, the controller stores error codes (syndrome codes) in the boot RAM area. These codes are sent to the controller by the ECA card performing the correction after the controller sends the proper control signals to the ECA card to retrieve the error codes. Also, since the correction process requires extra time than is available during a normal cycle, the processor extends the backplane SCLK to provide this time. This clock extension occurs only during a correction cycle and the controller must compensate by extending the VALID- signal on the backplane.

In operation, when a single-bit error occurs, the ECA card asserts the EC- (error correction) signal on the backplane, informing the processor to extend the short-half-cycle of SCLK. The controller also receives this line on U810-1 (21-C). The EC- signal then resets the shift register at U610-1 (22-C) to start the extension sequence necessary for extending VALID. Note on the schematic that the EC- signal is gated with VALID to prevent glitches on the EC- line from erroneously resetting the shift register.

The EC- signal remains asserted until one FCLK cycle after the rising edge of SCLK-. When it is released by the ECA card, the shift register starts setting its outputs in sequential fashion. The result is a series of shifted pulses spaced by one FCLK cycle apart and occurring during the SCLK clock extension period. These pulses are used for various timing purposes as will be presently described.

5.6.5.1 Syndrome Code Storage

See Figure 5-4 for the following theory of operation on the error logging operation of the error correction cycle. When the shift register is reset, the control signals it produces immediately set up the controller for the error logging operation. The EX4+ signal at U610-14 appears on U39-13 to disable the backplane data receivers. This is necessary since the syndrome code will soon be received from the ECA card on the controller data bus. The EX4+ signal also disables address driver U19 (25-B).

The EX4 signal enables driver U11 (27-B), to present the upper eight bits of the latched physical address to appear at the lower eight address inputs of the boot RAM. These physical address bits, PA16 through PA23, represent 64k blocks of main memory. Therefore, if the address is incremented by one, the main memory address is incremented by 64k (i.e., to the next block).

Since this address (PA16 - PA23) is being used to select the location of boot RAM to which the syndrome code will be stored, the location in boot RAM corresponds to a unique 64k word block of main memory. (Since the RAMs used on the ECA card are 64k RAMs, this corresponds to one row of memory on the ECA card.) Any syndrome code stored in a given address in boot RAM indicates an error in a unique row of main memory.

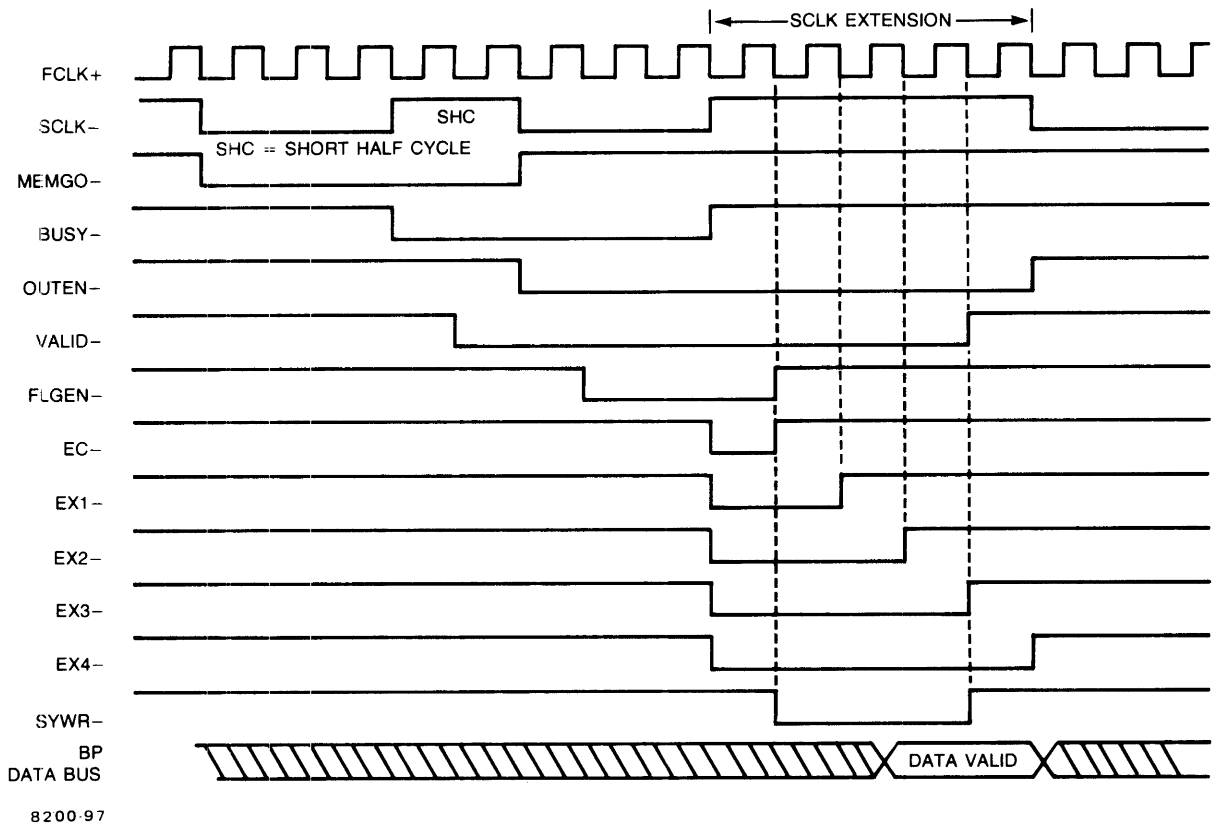


Figure 5-4. Error Correction Cycle

The EX4+ signal disables address driver U41 (37-D) to allow the ECA card to send the syndrome code to the controller on address lines PA10 thru PA15. (This physical address is not necessary at the ECA card now since data has already been accessed from the main memory RAMs.) The EX4- signal enables driver U31 (28-B) to receive the incoming error code. The EX4+ signal also sends the SYNRQ- signal from U32-11 (38-D) to the ECA card to request the syndrome information.

The EX4+ signal sets bits 8 and 9 of the address bus to the RAMs at U39-6 and -3. This forces the syndrome access to occur in the upper 256 locations of the 1k boot RAM area. That is, syndrome codes are stored in address locations 1400 thru octal 1777 in the boot RAM.

When the EC- signal is released on the backplane, the output at U810-3 goes high, enabling the shift register to set itself again. Signal EC- also appears at U103-4 where it is gated with EX3+ and the PDSABL signal from the ECA card. All signals are now high which causes the syndrome write SYWR- signal to appear at U105-1 and -4 selecting the boot RAMs for syndrome writing. Note in the schematic that U105-6 only goes to the lower order boot RAMs (U53 and U63). Thus, only the lower order eight bits of the data in a given location can be written with an error code.

As the shift register goes through its setting sequence, EX3+ is reset, terminating the boot RAM write signal. The delayed VALID- signal also terminates at this time. The VALID signal has been extended by the EX2- signal appearing at U108-4. It also extended the DI and OUTEN signals by holding U118-10 reset. The EX4 signal is the last signal to reset and is coincident with the end of the short-half-cycle of SCLK.

5.6.5.2 Double-Bit Error Detection

When a double-bit error is detected by the ECA card, the ECA card forces the controller to assert a parity error interrupt. The ECA card releases the signal PDSABL- (parity disable) at the same time the EC- signal is asserted so that the input at U88-1 and -13 (11-B) goes low. Also, since the shift register has been reset, the EX3- signal appears low at U88-10 (11-B). These two signals force the output at U88-8 high which is the signal SWDIS+ (Syndrome Write DISable). Thus, when VALID clocks the parity error flip-flop at the end of the memory cycle, a parity interrupt will be asserted.

Note in the schematic that the PDSABL+ signal goes to U103-5. When it is released (low) for a double-bit error, it immediately prevents the writing of the error syndrome code into the boot RAM. Therefore, when a double-bit error occurs, a syndrome code is not stored in the boot RAM. Syndrome codes for double-bit errors are meaningless since the EDAC chip on the ECA card cannot correct double-bit errors.

5.6.6 TIMING AND CONTROL CIRCUIT

The main control circuit is a hardware sequencer that provides the necessary control signals for performing memory cycles. The operation of the circuit is described in terms of the various operations it implements including backplane handshake and drive enable signals, data and address latch signals address strobes, and internal memory and interrupt protect signals. Refer to the timing diagrams in Figure 5-5 and 5-6 for the timing details of each of these main control functions.

5.6.6.1 Backplane Handshake Signals

All memory cycles are initiated by the assertion of the MEMGO- signal on the backplane. The memory controller always responds by setting the BUSY- signal at the beginning of the following short-half-cycle (SHC) of SCLK.

In the case of a two cycle (main memory) access without a conflicting refresh cycle, BUSY- is held for one SCLK cycle and is reset at the beginning of the next SHC. In the case of a three-cycle access to boot ROM or RAM without a conflicting refresh cycle, BUSY- is held for two SCLK cycles and is reset at the beginning of the second SHC of SCLK. (For the case of conflicting refresh cycles, refer to paragraph 5.6.7.3.)

5.6.6.2 Two-Cycle Main Memory Access

The two-cycle main memory access to the memory array cards is shown in the timing diagram of Figure 5-5. In operation, the VALID- signal is asserted one FCLK cycle after BUSY- is asserted and is reset one FCLK cycle after BUSY- is reset. the assertion of VALID- is held off for one SCLK cycle so that it is asserted for only one SCLK cycle towards the end of the BUSY- signal. It is still reset one FCLK cycle after BUSY- is reset. This is necessary to satisfy I/O master requirements of VALID- being asserted for only one SCLK cycle.

When the MEMGO- signal appears on the backplane, it is received by U99-15 and is sent to U106-13 where it is gated with REMEM-. If REMEM- is asserted, the MEMGO signal will not proceed to the control circuitry. The result is that the controller will ignore the request for a memory cycle. If REMEM- is not set, the signal goes directly to the J-input of the BUSY flip-flop U118 (13-B).

The BUSY flip-flop sets on the next falling edge of SCLK+. The output of the BUSY flip-flop at U118-6 then goes to U97-5 (14-C). If there is no refresh cycle in progress, U97-6 will be low and the BUSY- will produce a high at the J-input of the VALID flip-flop.

The VALID flip-flop sets on the next falling edge of FCLK+. This causes a reset signal to appear at the K-input of the BUSY flip-flop (U118-2) so that on the next falling edge of SCLK+ the BUSY flip-flop will be reset. Thus, BUSY will be asserted for one SCLK cycle. When BUSY resets, a reset signal appears at the K-input of the VALID flip-flop so that one FCLK cycle after BUSY resets, VALID is reset. This completes the two cycle backplane handshake.

5.6.6.3 Three-Cycle Boot Memory Access

The three-cycle boot access timing is shown in the diagram of Figure 5-6, If an access to boot RAM or ROM on the memory controller card is initiated, the MEMDIS- signal will be asserted with MEMGO-. MEMDIS- inputs to U116-5 (13-C). The output at U116-6 goes low and asserts the XTND- signal which is used to select the three cycle mode. Note in the schematic that the CYCLE flip-flop U128 (14-C) is also set the same time as BUSY flip-flop U118 (13-B), provided that refresh is not in progress.

The CYCLE flip-flop will always toggle on and off for one SCLK cycle since its Q output is connected back to the K input. The CYCLE- signal is used with the XTND- signal to hold off the assertion of VALID- during a three-cycle memory access. This is done at U107-9 and -10. Since the LBT- signal is low for the entire cycle (latched at U29) the output at U107-8 will be low when the CYCLE- signal is present.

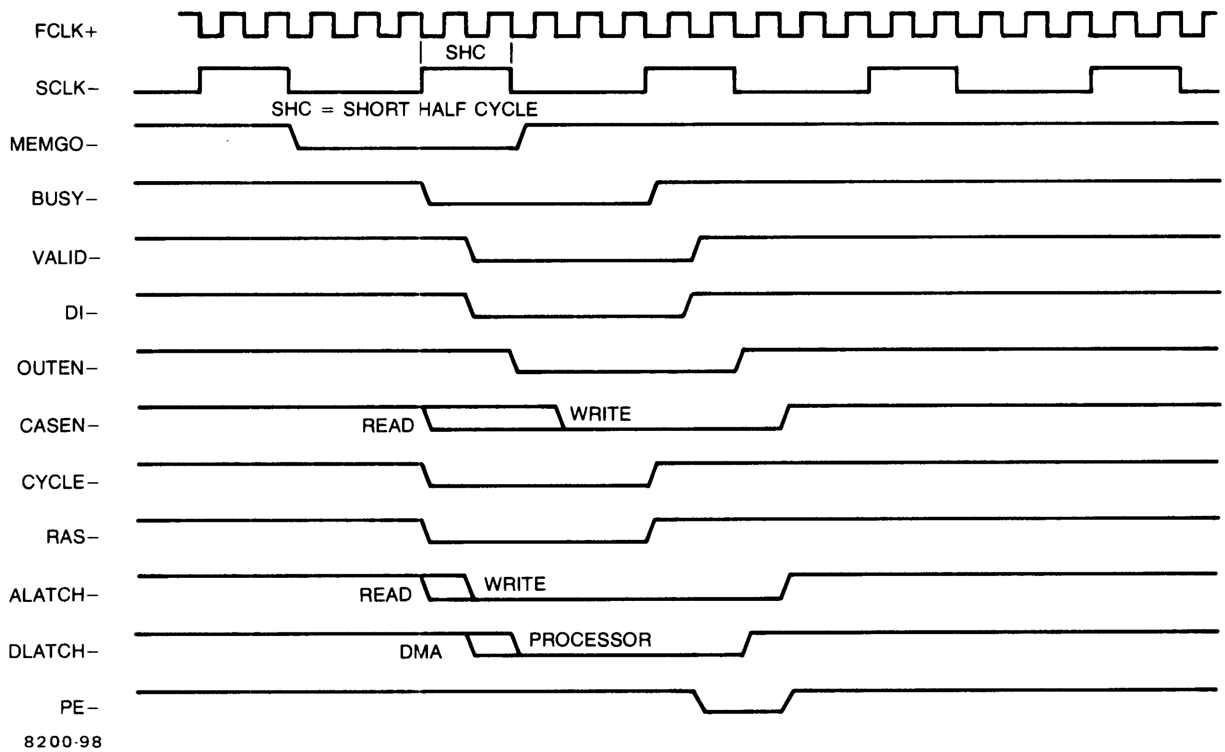


Figure 5-5. Two-Cycle Main Memory Access

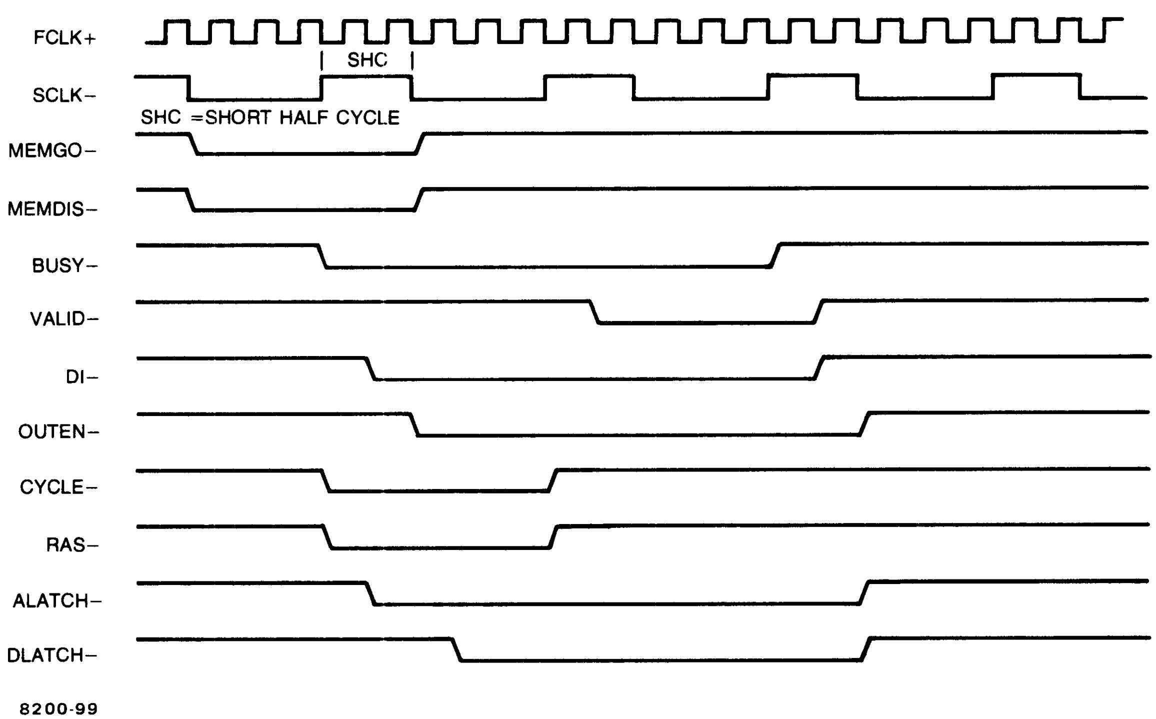


Figure 5-6. Three-Cycle Boot Memory Access

CYCLE and XTND- hold the VALID flip-flop clear. When the CYCLE signal resets, the clear is removed and VALID is set on the next falling of FCLK+.

When VALID is set, BUSY resets on the next falling edge of SCLK+ and VALID resets one FCLK cycle later as before. Thus, BUSY is asserted for two SCLK cycles and VALID is asserted for one cycle.

Since VALID is not asserted during the CYCLE signal, reset is not sent to the BUSY flip-flop, preventing it from resetting after one SCLK cycle.

The extended two-cycle BUSY+ signal is gated with VALID- through U93-1 and -2 (12-C). This prevents the BUSY signal from affecting the input of the CYCLE flip-flop at the end of memory cycles when VALID is asserted; otherwise, the CYCLE flip-flop would resets after one SCLK cycle and cause the controller to initiate a delayed memory cycle. (Refer to paragraph 5.6.7.5 on Memory Cycles with Pending Refresh Cycles.)

The XTND- signal goes through the frontplane to the array cards for enabling the three cycle mode on these cards in the event that this is desirable in future array card designs.

5.6.6.4 Address Latch Signal

At the beginning of every memory cycle, the address of the memory location to be accessed is latched using signal ALATCH. The lower order 10 bits are latched on each array card directly from the backplane while the mapped address is latched on the controller in four 74S157 type transparent latches (refer to Page Address Generation in paragraph 5.6.1.1.).

The latching is necessary since the address for the requested memory cycle is only valid on the backplane during the assertion of MEMGO- but the addresss are needed on the cards for the whole cycle. This is to assure that if a parity error (or double-bit error) occurs on the access, the selected memory array card will ready to store the accessed address into the parity error latch. The address that is latched is the physical address sent to the array cards, not the logical address on the backplane.

The address latch signal is generated one FCLK cycle after the BUSY signal is asserted in response to MEMGO-. When BUSY is set, the inputs to the DI signal flip-flop U118-11 and -12 (14-B) are immediately qualified. On the next falling edge of FCLK+, the DI flip-flop toggles and sets the input of U107-12 high. This in turn sets the input of U97-11 high which then drives the ALATCH- signal to the address latches.

There are two levels of gating to produce ALATCH-. The first level of gating at U107-12 and -13 is used to generate the proper length latch signal during boot cycles when CASEN+ is totally absent.

The second level of gating using U97-11 and -12 effectively allows either the FLCH+ or the CASEN+ signal to generate ALATCH-. During a boot access, the CASEN+ signal is not asserted (refer to Protected Memory Access, paragraph 5.6.6.10.) so that the latching function is done by DI+. During a write memory access, the CASEN+ signal is not asserted until after the assertion of OUTEN+. Since this is not soon enough to catch the address while it is valid, the overlap of the DI+ signal and the CASEN+ signal provide the correct latch signal. The CASEN+ signal is primarily used to extend the end of the latch signal to cover the complete memory cycle. (Refer to paragraph 5.6.6.7 for additional information on the CASEN signal).

5.6.6.5 Data Latch Signal

The data latch signal DLATCH- is generated only during write cycles since it is only then that the memory controller stores data from the data bus. DLATCH- is generated at two different times depending on whether the processor or an I/O device is writing data into memory. This results from the fact that data from an I/O device is available on the backplane much sooner than data from the processor. Also, data from the processor is held much longer than data from an I/O device.

The DLATCH- signal is generated at U113-6 (16-A). It is routed to U49-11 and U59-11 to latch data on the controller and it also goes to U42-12, where it is sent out over the frontplane to the array cards. The SLCH+ signal at U113-4 (slow latch signal) determines if the latch signal is asserted early or late.

During a DMA cycle, (I/O device) the MRQ- signal is asserted on the backplane. This signal is used to immediately set the SLCH+ signal so that as soon as the FLCH+ signal occurs, the data latch signal is asserted early. If MRQ- is not asserted, the processor is performing the access and the SLCH+ signal is held off at U93-12 (11-D) by the MEMGO+ signal. Only after the delay of the MEMGO+ signal does the SLCH+ signal get asserted. Note that the FLCH+ signal is asserted at the same time each memory cycle. It is a composite of the DI+ and OUTEN+ signals to give it the correct length to cover the whole cycle. The W+ signal at U113-3 insures that the DLATCH- signal is asserted only during a write cycle.

The DLATCH signal to the array cards does both address and data latching on the array card. Since the backplane address latched on the array cards is guaranteed only to be valid during the SCLK cycle during MEMGO, the latch signal must not be delayed beyond the end of the short-half-cycle of SCLK during MEMGO.

The SLCH signal is set when MEMGO terminates but the MEMGO trailing edge can be delayed excessively beyond this point because it being pulled high by a resistor and not a gate output. The delayed pulse edge is acceptable for data latching on the memory controller during processor writes since the processor holds data valid during the long-half-cycle after MEMGO. However, it is not acceptable for latching the backplane ADDRESS on the array cards. To overcome this, the DLATCH signal to the array cards must not occur later than the OUTEN signal for any cycle. Therefore, the OUTEN- signal is sent to the frontplane driver at U42-13 to accomplish this.

5.6.6.6 RAS Generation

The RAS (Row Address Strobe) is the signal used to start the array card memory access. For either a read or write cycle, RAS is sent to the array cards and is used to strobe in the row address for the memory array. This signal is generated from the CYCLE- signal.

When a memory cycle is initiated, the CYCLE flip-flop is set at the same time BUSY is set (provided there a refresh cycle is not already in progress). When CYCLE- occurs, it is routed directly to the frontplane driver at U42-4 and -5. The output of this driver is the RAS- signal sent to all array cards. Thus, RAS is generated directly from the CYCLE signal.

5.6.6.7 CAS Generation and Memory Access Control

The CAS (Column Address Strobe) signal on the array cards is generated through the use of a delay line on each array card from the RAS signal. The CAS signal is the main signal controlling the access to the main memory array. In operation, the CAS signal is enabled on the controller by the CASEN signal before being asserted on the RAM chips.

The CASEN- signal provides memory access control so that the controller can perform a refresh cycle, boot cycle, main memory cycle, or protect the main memory array from an illegal access. These functions are accomplished by controlling the CASEN flip-flop U128 (15-B). by the 'and-or-invert' gate located at U117 (13-D). This gate is the means by which the controller protects the access of main memory.

5.6.6.8 Normal Main Memory Access

In a normal (non-protected) access to main memory for either a read or write, the CASEN+ signal must be sent to U32-4 and U32-5 (19-B) in order to be sent to the array card for the access to complete. Therefore, the CMP- signal to U128-14 (15-B), the clear input, must not be asserted for the duration of the cycle. In the case of a normal write access, the shift register sequence of the BUSY, DI, OUTEN and CASEN flip-flops proceeds over the period of four FCLK+ cycles. The CASEN flip-flop sets at the fourth cycle, asserting the late CAS enable signal to the array cards and effectively writing the data into the memory array.

The CAS enable signal is a late signal since the delay line version of CAS on the array cards is already asserted but is not presented to the RAMs. This late CAS enable is necessary during a write cycle to allow sufficient time for parity bit generation. (In the case of an ECA card write, this time, plus a little more provided by the ECA card itself, is necessary for check word generation.)

When a normal read cycle occurs, it is desired that the CAS signal to the RAMs occur as quickly as possible, i.e., as soon as it becomes available from the array card delay line. Therefore, the CASEN+ signal is preset at the same time the CYCLE signal set at the beginning of the memory cycle, and remains set for the whole cycle. This presetting of the CASEN flip-flop is accomplished by the signal at U113-12 (14-D).

In operation, provided that the CMP- signal is not asserted and also that it is a read cycle, the output at U113-12 will go low when the CYCLE+ signal occurs. This immediately sets the CASEN flip-flop. There can never be a conflicting preset and clear. to the CASEN flip-flop since the CMP- signal goes to U113-13. For both a normal read and write cycle, CASEN is reset at the end of the shift register sequence initiated by the reset of BUSY.

5.6.6.9 Boot Memory Access

In the case of a boot memory access, the memory system is being requested to send data from either the boot RAM or ROM on the controller and NOT from the main memory array. Therefore, the controller must not access the array cards. This is accomplished by inhibiting the CASEN signal for the duration of the cycle.

A boot cycle is initiated by the assertion of the backplane MEMDIS- signal during MEMGO-. The MEMDIS- signal is latched at U29-12 (11-C) by LBT-, and it is held for the entire memory cycle. This signal appears inverted at U117-9 and 10 (13-D) which directly asserts the CMP- signal. Since CMP- is held for the entire cycle, CASEN- is held reset for the whole boot cycle. This has no affect on the generation of RAS; therefore, RAS is asserted at the RAMs but not CAS. This is the equivalent to a refresh cycle where data is not written to or read from the main memory. Only one row on the arbitrarily selected array card is refreshed.

5.6.6.10 Protected Memory Access

In the case of a protected access of main memory, the memory controller must prevent any data from being written into or read out of the array cards. The way a protected access is detected is through the read and write protect bits stored in the map RAMs at U16 (32-A) and U26 (33-A), respectively.

At the beginning of a memory cycle during the assertion of MEMGO-, the backplane address selects the proper location in the map RAMs to obtain the mapped physical address. The corresponding locations of the read and write protect RAMs are accessed to get the read and write protect status information for this particular address. If either of these bits are set high then the corresponding protect function must take place. The read and write protect bits are latched, along with the mapped address, at U43-12 and 9 (36-A) respectively. These signals are monitored by the memory protect gate at U117 (13-D).

The signal from U106-6 (12-D) is used to enable the read-write protect function at U117-4 and -11. This signal is derived from the backplane memory protect signal, MP+. It is gated with MRQ- at U106 to allow DMA accesses to override the memory protect function. Note that the read protect bit is also enabled by the W- line at U117-5.

Thus, the read protect function can occur during only a read cycle. Similar reasoning applies to the write protect function. It should be obvious that the read protect function cannot occur during a write cycle and vice versa. The memory is protected by the assertion of the CMP- signal at U117-8 for the duration of the memory cycle.

Lastly, in the case of a refresh cycle, the contents of main memory must not be altered, only refreshed. Refresh is accomplished by a RAS only cycle to the array cards. Therefore, when a refresh cycle is initiated, RAS must be generated but CAS must be inhibited. This is easily done by preventing the assertion of CASEN during the refresh cycle. A refresh cycle can, therefore, be visualized as a memory protected cycle where only RAS is asserted. RAS is sent to all RAMs on all array cards in the main memory array during a refresh cycle.

5.6.6.11 Backplane Drive Enable Signals

During a memory cycle, the controller must send the proper handshake signals to either the processor or I/O device. It also must enable the proper array card to drive data onto the backplane during a main memory cycle or enable itself to drive the backplane during a boot access. The main handshake signals, BUSY and VALID, are driven onto the backplane at U99-14 (11-D) and U99-12. The enable signal for this driver is generated at U97-1 (12-D). This signal is derived from the BUSY and OUTEN signals. Thus, when BUSY is asserted in response to MEMGO, it immediately gates itself onto the backplane. The OUTEN signal is used to extend the enable signal to the end of the memory cycle.

When accessing main memory during a read cycle, the controller generates a read enable signal (RE+) which is sent to all array cards. This signal is used only by the selected array card to enable its backplane drivers to output data onto the backplane data bus. RE+ is generated at U96-8 (17-B) in the following way:

First, RE+ must only be asserted during a read cycle, so the W- signal appears at U96-11 as an enable signal. The gating signal is provided by the OUTEN signal at U96-10. This signal provides the proper time for enabling the backplane drivers. The last enable signal, CEN-, is derived in a rather complicated way. This signal is normally high, enabling the RE+ gate, except under two conditions: when a read access to protected memory is attempted and when an access to non-extant main memory is attempted.

In the case of a protected memory access, the controller memory protect signal is generated (CMP-). This causes the output at U97-10 (16-B) to go low, disabling the RE gate. This happens before the assertion of the OUTEN signal so that U96-8 never goes high during the cycle. Thus, the array cards are inhibited from driving the data bus during a protected cycle. The CEN- signal is inverted at U109-12 (17-B) and sent to the input of the RM gate at U96-3.

The RM+ signal is used to enable the controller's data bus drivers in the case of a boot access. Since the inputs at U96-4 and -5 are the same as those for the RE gate, the CEN- signal determines whether the controller or an array card drives the backplane data bus. In this protected main memory access, the controller, not an array card, drives the data bus. Since the boot RAM or ROM are not enabled at this time, the controller's internal data bus is pulled high by resistors R3 and R79. Therefore, the enabled drivers U69 (27-D) and U89 (27-C) drive all ones (octal 177777) onto the backplane. So, for a protected main memory read access, the addressed location is not accessed and the controller outputs octal 177777 onto the backplane data bus.

In the case of a main-memory read access to non-extant memory, it is obvious that the memory system cannot supply meaningful data to the bus. The controller is informed of this condition, however, by the ACK- signal at U97-9 (16-B). ACK- is asserted low whenever an array card is selected.

The selected array card sends ACK- over the frontplane to the controller. If this signal is not asserted during a memory read cycle, the controller assumes that a memory card is not driving data onto the bus, and so it will send all ones onto the bus as in a read protected access. The CEN- signal at U97-10 will be low under this condition. Therefore with no memory array cards installed in the backplane, all read accesses to main memory will produce octal 177777 on the data bus.

5.6.6.12 Memory Protect Interrupt

In the event of an attempt to access protected memory, the processor is alerted to this fact by the memory protect interrupt MPV- signal. MPV- IS generated at U116-11 (18-B) and sent onto the processor frontplane. The timing of MPV- on the frontplane is determined by the gating of VALID at U116-13. The interrupt condition is set up at U116-12 by the memory violation signal (MV+) generated at U96-12 (17-C). The MV+ signal is derived from the controller memory protect signal, CMP-. Recall that the protect signal is asserted not only during a protected access, but also during a boot cycle and a refresh cycle. Obviously, the processor memory protect signal should not be asserted during a refresh or boot cycle, so these events are gated out of the controller protect signal CMP- at U96-1 and -2. Thus, the violation signal at U96-12 is only present during a true protected memory access.

5.6.7 REFRESH CIRCUIT

The dynamic RAMs used in the main memory array must be clocked at a regular interval in order to maintain the data stored in them. The clock used is the RAS pulse normally used for memory accesses. Internal to the RAMs, the RAS signal is used to enable a word line in the cell matrix. There are 128 word lines in each RAM, and the one that is enabled by RAS is the one that is selected by the address present at the RAM pins at that time. This is the refresh address.

The RAMs require that all rows (word lines) be accessed (refreshed) every 2 milliseconds. Therefore, every 15.6 microseconds a different row is refreshed. This is the rate that the refresh cycles are generated by the controller. A normal main memory access effectively causes a refresh to occur since RAS is asserted for the access. This refresh occurs at only one row of RAMs, however. A program that causes a sufficient number of memory accesses and random address selection can self-refresh the memory independently of the refresh circuit but this is a rare occurrence. The refresh circuit guarantees that memory is maintained regardless of whether the system is idling or executing programs.

The refresh circuit operates in two different modes. One is the operational mode where AC power is applied to the computer system and the system is fully functional. The other is when AC power is removed and the the memory system is in standby mode where battery power is used to sustain the memory power supply and refresh operation. The latter may occur during AC line power failures and it is desired that the contents of main memory are not lost. No memory accesses are done in this mode and only refreshing takes place.

5.6.7.1 Operational Mode

See Figure 5-7 for the timing of signals used in the operational mode of memory refresh. Under the operational mode the refresh circuit schedules refresh cycles by counting cycles of the system clock, SCLK. This is done by the 74LS390 type counter U85 (16-D). The SCLK+ signal appears at U123-9 (16-E) which inverts it and drives the counter input at U85-1. The counter output is monitored by four-input AND gate U95 (17-E) to detect a count of 55 SCLK cycles. When this occurs, the output U95-6 goes high and gates off the clock at U123-8. This prevents the counter from incrementing so that it holds the present count.

The output at U95-6 is the refresh pending (RP+) signal and is now effectively latched until the counter is reset. If there is no pending memory cycle taking place, the BSY- signal at U95-13 is high enabling the RP+ signal to the refresh flip-flop at U126 (18-D). This is the Refresh Go signal (RGO+). On the next rising edge of SCLK+, the refresh flip-flop is set, initiating a refresh cycle. The counter is reset by the Refresh Cycle (RC+) signal so that the refresh pending signal is reset also.

When the RC- signal occurs, it appears at U113-10 (13-C), enabling the J-input of the CYCLE flip-flop. A memory cycle is thus initiated, and RAS is sent to the array cards in the same way as before. The RC+ signal appears at U117-3 (13-D) which forces the CMP- (Controller Memory Protect) signal. This prevents the assertion of CASEN which disables the assertion of CAS at the RAMs on the array card. In this way, a RAS only refresh cycle is generated. The refresh address to the RAMs is generated on the array cards themselves.

Note on the schematic that CASEN- is gated with RC+ at U117-2 and -3 so that RC+ will not assert CMP- to the CASEN flip-flop and reset it during the previous memory cycle (CASEN terminates normally). This circuit prevents a held off refresh cycle from truncating the CASEN signal when the refresh cycle is initiated by RGO+, since CASEN is extended beyond the end of the memory cycle to hold addresses valid.

Since the RP+ signal is removed immediately upon the setting of the RC signal, the input at U126-2 (18-D) goes low. For proper refreshing the refresh signal is asserted for two SCLK cycles. To accomplish this, the RC-signal is gated with the CYCLE- signal at U123-5 and -6 (16-D) producing a refresh hold signal at U123-3 (see Figure 5-7). This causes the output at U123-1 to go low holding the refresh flip-flop set during the CYCLE signal.

After CYCLE completes, the preset is removed and the refresh flip-flop will reset on the next clock edge of SC+. The RC signal is thus held for two SCLK cycles. Upon the reset of RC+, the counter is enabled to start counting again and the cycle repeats.

NOTE

A 250 nanosecond system clock and a 14.6 microsecond refresh interval calculates to produce a refresh every 58 clock cycles. However, the counter output is decoded for the count of 55. This difference results from the fact that the counter is held latched for one cycle during the refresh pending time and is held clear during the two cycles of the refresh cycle time. These three cycles of refresh overhead are added to the 55 count to form the 58 SCLK cycle refresh interval.

5.6.7.2 Standby Mode

See Figure 5-8 for refresh circuit timing in the standby mode. The controller switches to standby mode when the PON+ signal on the backplane goes low. The controller will not acknowledge any requests for memory cycles when the PON+ signal is low. While in this mode, only refresh cycles are performed and the scheduling of refresh cycles is done in a differently. While in standby, the controller uses its own oscillator instead of the backplane clock to initiate refresh cycles.

The CYCLE flip-flop U128 (14-C) and REFRESH flip-flop U126 (18-D) are directly driven by their preset and clear inputs. When the PON- signal is high, the logic gates at U125-5 (13-E) and U125-9 (15-E) are enabled to drive the clear inputs of the flip-flops. Also, the refresh oscillator U124 (13-E) is enabled. The refresh oscillator directly sets and resets the CYCLE flip-flop through the two NAND gates at U125. The STRAS/2 flip-flop U127 (15-E) directly sets and resets the REFRESH flip-flop through the gates at U125 and U123. The refresh oscillator runs at twice the refresh rate and clocks the STRAS/2 flip- flop. This flip-flop divides the oscillator output by two and allows refreshing to occur every other oscillator cycle.

In operation, assume that the STRAS/2 flip-flop is clear. The gate at U125-1 is disabled and the REFRESH flip-flop is forced to reset by U125-8. Note that the set inputs to CYCLE and REFRESH flip-flops are high. When the oscillator waveform goes high, it cannot set the CYCLE flip-flop since U125-1 is disabled.

When the waveform goes low, it clocks the STRAS flip-flop which causes it to go to the set state. (Note that the STRAS/2 flip-flop is configured in a toggle mode.) This causes the REFRESH flip-flop to set. Also, the gate at U125-1 is enabled. The next time the oscillator waveform goes high, the CYCLE flip-flop sets which then sends the RAS signal onto the frontplane to the array cards. When the oscillator goes low, it resets the CYCLE flip-flop and also clocks the STRAS/2 flip-flop to a reset state. This resets the REFRESH flip-flop and finishes the cycle. The cycle repeats as long as the PON- signal is high.

The reason that the controller does not use the backplane clock to schedule refreshes during standby is that battery power only goes to the memory system during standby. Therefore, the clocks on the processor are not running and cannot be used by the refresh circuit.

5.6.7.3 Arbitration between Memory and Refresh Cycles

The refresh function must occur periodically, and very frequently it is attempted simultaneously with normal memory accesses. Obviously, both cannot take place at the same time so some method of interleaving of the two processes must exist. This is achieved by initiating refresh operations and memory accesses on opposite edges of SCLK, i.e. memory cycles are initiated on the falling edge of SCLK+ and refresh cycles are initiated on the rising edge of SCLK+. Once a cycle is initiated, it is allowed to complete. If an opposing cycle is attempted while the initiated cycle is pending, the opposing cycle is simply held off until the pending cycle completes. Therefore, neither type of cycle is given priority over the other and cycles are serviced on a first come, first serve basis.

5.6.7.4 Refresh Cycles with Pending Memory Cycles

See Figure 5-9 for the timing diagram of refresh cycles with pending memory cycles. In this case, the memory cycle was the first to get the attention of the memory controller. For either a normal or boot access, the BUSY- signal is asserted at U95-13 (17-D) and inhibits the refresh pending signal (RP+) from appearing at the input of the REFRESH flip-flop. When the BUSY signal is reset near the end of the memory cycle, it immediately allows the RP+ signal to pass to the REFRESH flip-flop input. On the next rising edge of SCLK+, the REFRESH flip-flop is set and the refresh cycle is initiated. Note that this is always true even if there is a request for a memory cycle immediately following the present one. In this manner, refresh cycles cannot be held off indefinitely by back-to-back memory cycles.

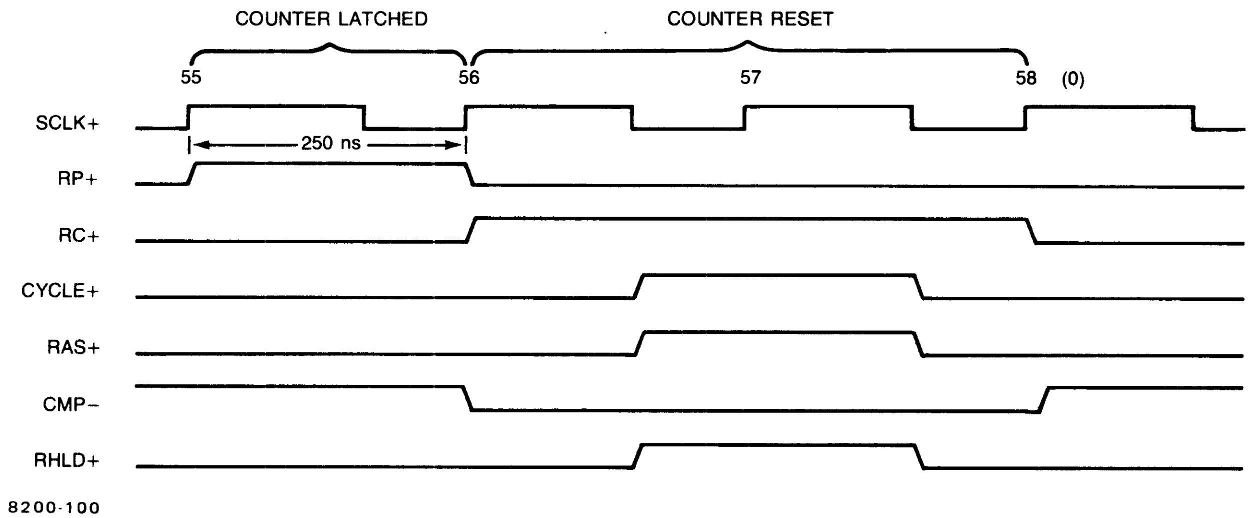


Figure 5-7. Refresh Circuit Timing (Operational Mode)

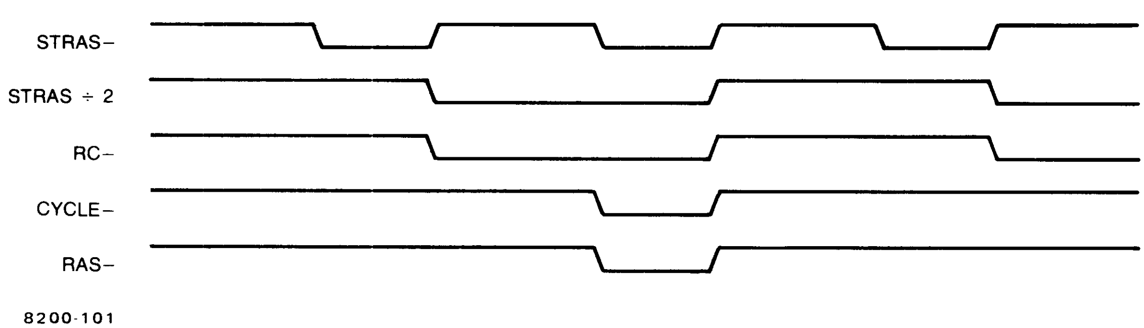


Figure 5-8. Refresh Circuit Timing (Standby Mode)

5.6.7.5 Memory Cycles with Pending Refresh Cycles

See Figure 5-10 for the timing diagram of two-cycle access with pending refresh cycle. In this case, the refresh cycle was the first to get the attention of the memory controller. The controller will set the BUSY- signal on the backplane in response to the MEMGO- signal as if there were no pending refresh cycle. The shift register sequence consisting of the BUSY, DI and OUTEN will also proceed as normal. (CASEN is held reset by the CMP- signal generated by the RC- signal) The ALATCH and DLATCH signals are asserted in the usual manner, latching the data and address while they are available on the backplane. The CYCLE signal, however, may already be asserted due to the refresh cycle or just completed at the end of the refresh cycle. In either case, the memory cycle MEMGO signal cannot initiate the CYCLE signal until the CYCLE flip-flop is reset after the refresh cycle. This is a direct result of the CYCLE flip-flop being configured in the toggle mode. For example, if the MEMGO signal occurs during the first half of the refresh cycle, the CYCLE signal is already asserted and cannot be set again. If the MEMGO signal occurs during the last half of the refresh cycle, it sets the J-input of the CYCLE flip-flop but the K-input of the flip-flop is also high so the flip-flop is reset regardless of MEMGO.

The VALID signal is not allowed to be set during a refresh cycle. The RC- signal appears at the gate input at U93-5 (19-C) and is used to inhibit the assertion of the valid set (VS) signal at U93-6. If the VS- is false (high) at U97-6 (14-C), the J-input of the VALID flip-flop remains low so that VALID cannot be asserted. Therefore, VALID can only be set if a memory cycle is initiated and a refresh cycle is not taking place. Note that the SCLK- signal gates the RC- signal at U93-4. This is so the assertion of VALID always occurs in the middle of the short-half-cycle of SCLK.

Since the BUSY flip-flop reset is qualified by the setting of VALID, the reset of BUSY is delayed until VALID is asserted after the refresh cycle. Therefore, BUSY is extended until the refresh cycle and then the delayed memory cycle complete. BUSY is reset in the normal manner at the end of the delayed memory cycle. The holding of BUSY during a pending refresh cycle is used to initiate the delayed memory cycle after the refresh cycle completes. When BUSY is high, the input at U93-1 is enabled and a low appears at U113-11. This qualifies the J-input of the CYCLE flip-flop to initiate the delayed memory cycle.

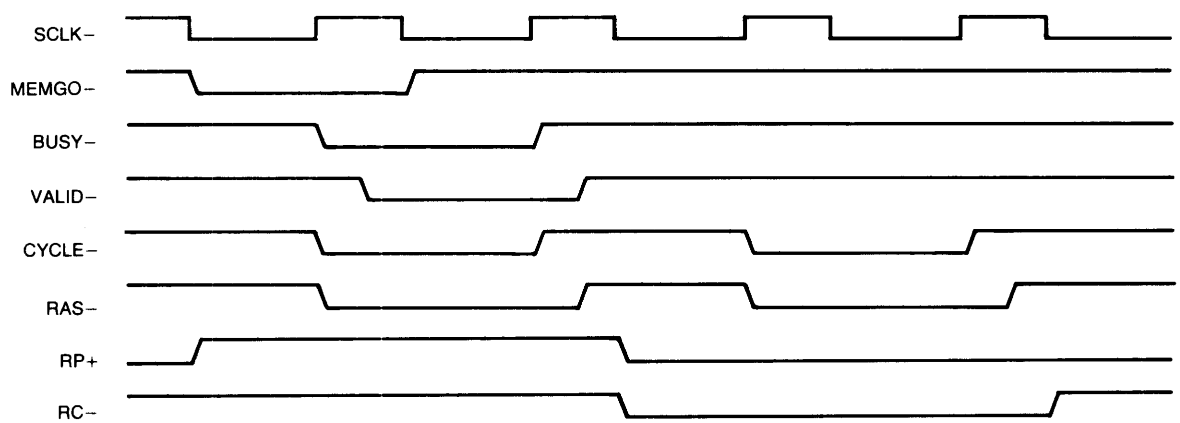


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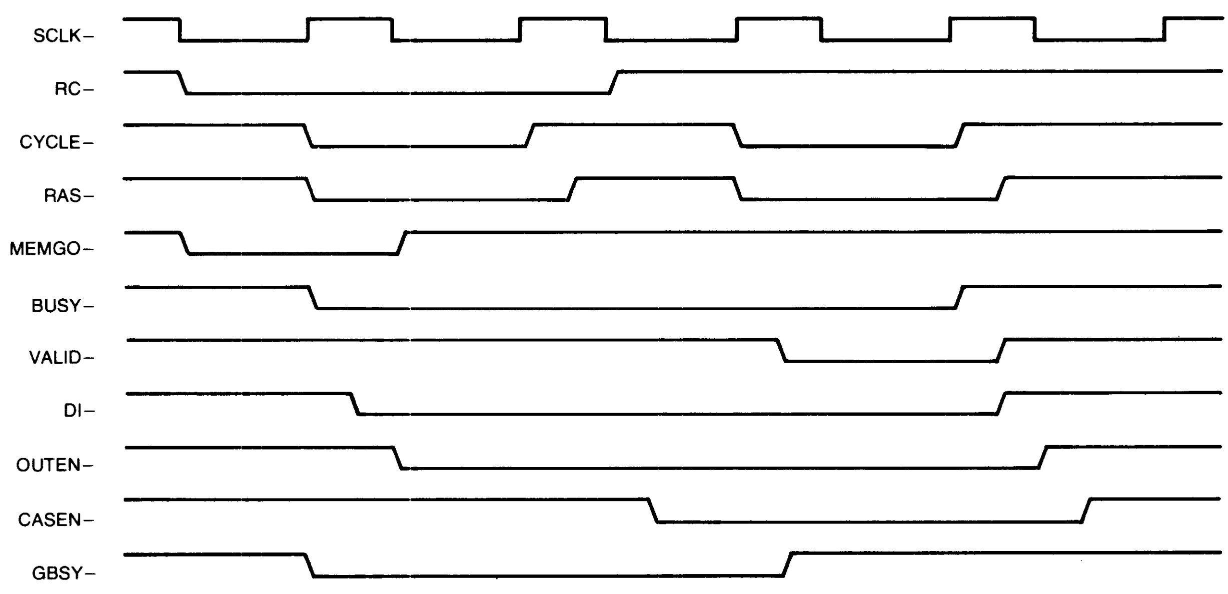
Figure 5-9. Timing Of Refresh Cycles With Pending Memory Cycle



8200-103

Figure 5-10. Timing Of Two-Cycle Access With Pending Refresh Cycle

5.6.7.6 Power Cycling

When AC power is removed from the computer system, the contents of the memory system are lost unless the a battery back-up option is installed in the system. In the latter case, the contents of memory are retained as long as battery power is available. In the event of a power down with a battery option in the system, the controller switches from operational to standby mode when the PON+ signal on the backplane goes false. As described under Operational Mode and Standby Mode paragraphs 5.6.7.1 and 5.6.7.2, respectively, the controller uses its own oscillator to schedule refresh cycles when in standby mode and uses the system clock while in operational mode. The transition between these two modes must be closely controlled so that proper memory refreshing is not interrupted. In the following paragraph is a description of the sequence of events during the power transitions.

5.6.7.7 Power-Down Sequence

The signal timing for the power-down sequence is shown in Figure 5-11. The PON+ signal is received onto the controller by the D flip-flop at U127-2 (14-E). This flip-flop (PON) is clocked by the RC- signal so that the PON signal on the controller is synchronized with refresh cycles. In particular, the PON flip-flop is clocked at the end of each refresh cycle to make sure that the transition between operational and standby modes cannot occur during refresh cycles.

Assume that the backplane PON+ signal is low and a refresh cycle just finished. The PON- line at U127-6 is clocked high which then causes the following events that switch the controller to the standby mode:

1. PON- appears at U116-9 and 10 (16-C). This holds the BUSY and DI flip-flops in a reset state so the controller now ignores any requests for memory cycles.

2. The PON- signal enables gates U125-9 (15-E) and U125-5 (13-E) which allow the CYCLE and REFRESH flip-flops to be directly driven by their preset and clear inputs.

3. The PON- signal enables the refresh oscillator U124 (13-E) to generate the standby RAS signal. This is done by directly driving the CYCLE flip-flop.

When the oscillator is enabled in step 3 by PON-, a high signal is asserted at U125-2 but the signal at U125-1 is not enabled since the STRAS/2 flip-flop is not set; therefore, the CYCLE flop-flop is not set and an unwanted RAS pulse is not gated out upon oscillator start up.

5.6.7.8 Power-Up Sequence

The timing of the power-up sequence is shown in Figure 5-12. When the PON signal is clocked high by the refresh signal, it reverses the three steps of the previous section. Note that the oscillator is cleanly turned off (i.e., its output is already low when the reset signal at U124-4 goes low). Also, with the assertion of the on-board PON signal all refresh related signals (STRAS, CYCLE, RC) as well as the refresh counter are correctly initialized for the operational refresh mode.

5.6.8 POWER SUPPLY JUMPERS

The A700 memory controller has locations for two wire jumpers. These locations are located at the rear of the card near connector P2. Whenever the A700 computer card set is used in a system that does not provide the +5M voltage separately (and does not have a battery back-up option) the two jumpers must be soldered in place.

Jumper W2 connects the +5V supply to the +5M supply. Jumper W1 connects the MLOST signal to ground.

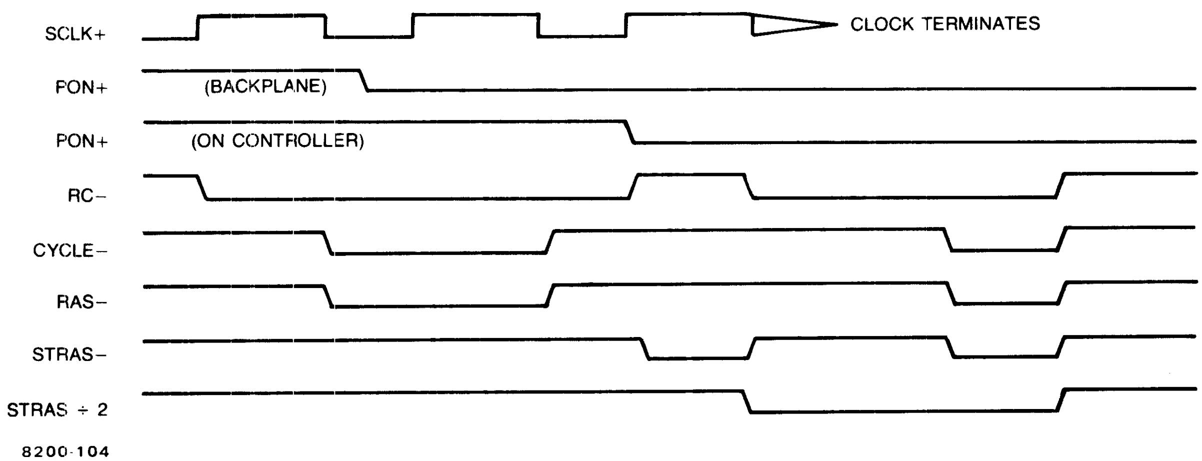


Figure 5-11. Timing Of The Power-Down Sequence

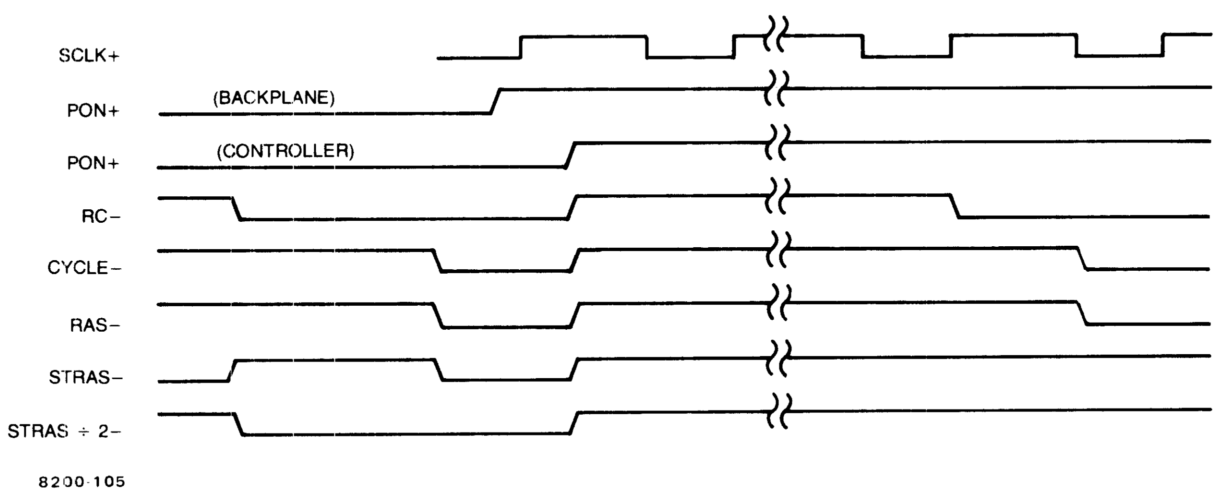


Figure 5-12. Timing Of The Power-Up Sequence

5.7 PARTS LOCATIONS

The parts locations for the memory controller are shown in Figure 5-13.

5.8 REPLACEABLE PARTS LIST

The replaceable parts for the memory controller are listed in Table 5-1. Refer to Table 3-8 for the names and addresses of the manufacturers of the parts in the Manufacturer's Code List.

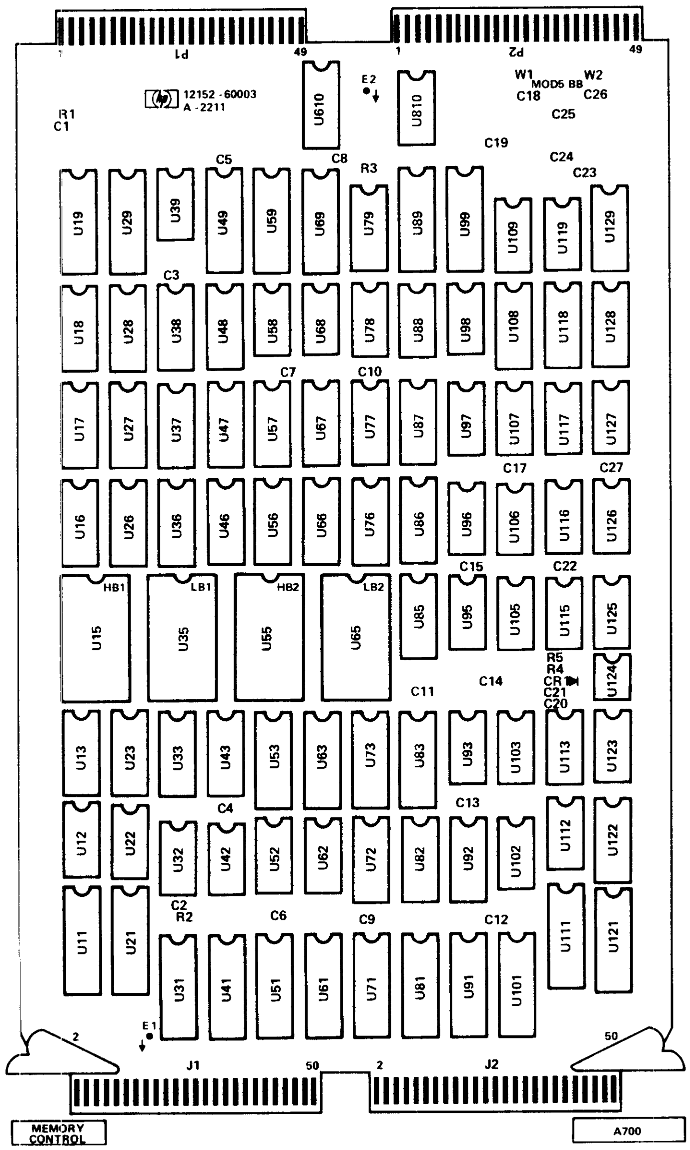


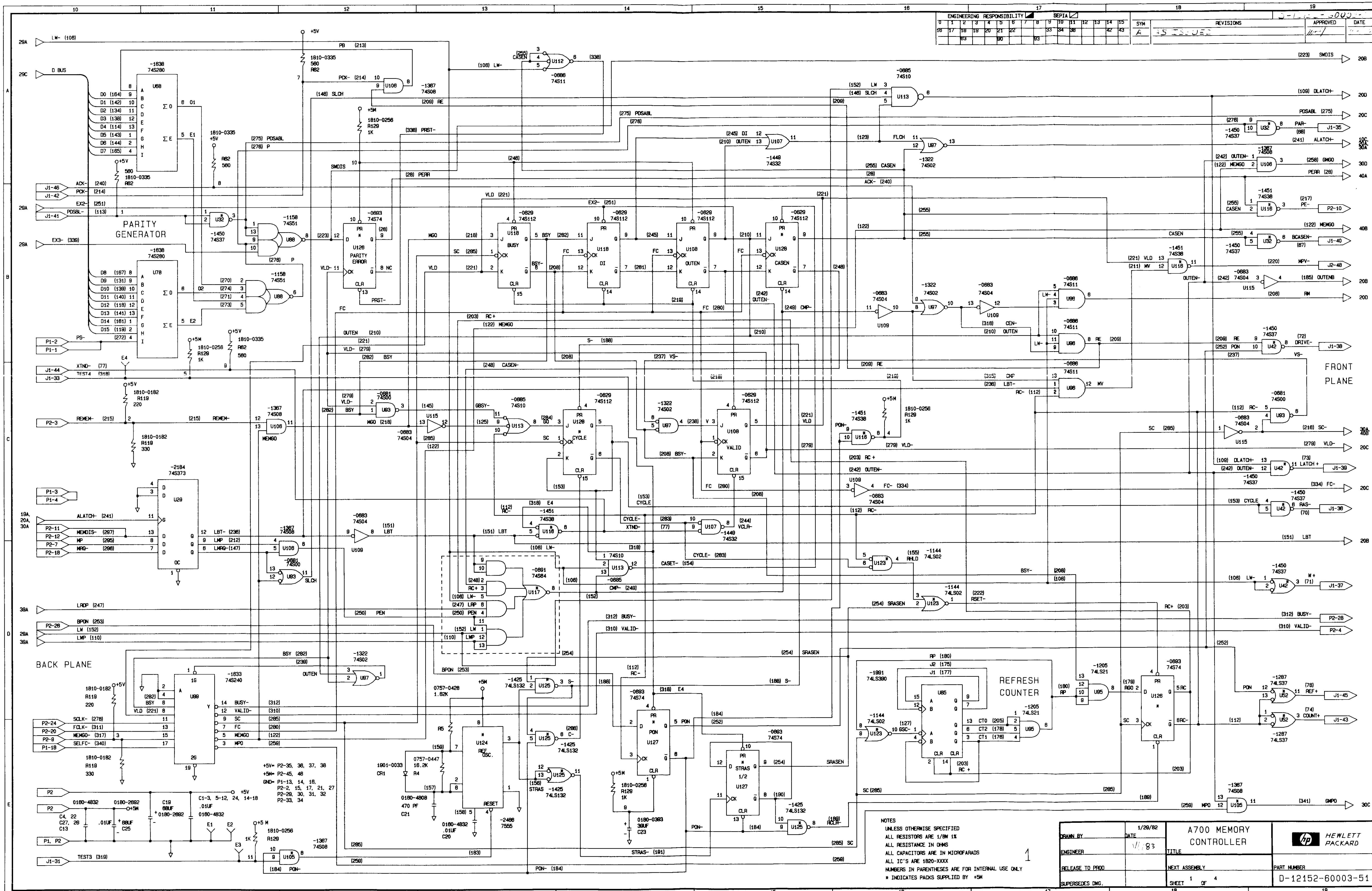
Figure 5-13. Memory Controller Parts Locations

Table 5-1. Memory Controller Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12152-60003	3	1	PCA-MEMORY CONTROL PART OF 12152-60003	28480	12152-60003
	12152-64003	1	1	ASSEMBLY-AUTO INSERT	28480	12152-64003
C1	0160-4832	4	22	CAPACITOR-FXD .01 UF	28480	0160-4832
C2	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C3	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C4	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C5	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C6	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C7	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C8	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C9	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C10	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C11	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C12	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C13	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C14	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C15	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C17	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C18	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C19	0180-2692	2	2	CAPACITOR-FXD 68UF 15VDC TA	56289	150D686X9015RS
C20	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C21	0160-4808	4	1	CAPACITOR-FXD 470 PF 5%	28480	0160-4808
C22	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C23	0180-0393	6	1	CAPACITOR-FXD 39UF+-10% 10VDC TA	56289	150D396X9010B2
C24	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C25	0180-2692	2		CAPACITOR-FXD 68UF 15VDC TA	56289	150D686X9015RS
C26	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C27	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
CR1	1901-0033	2	1	DIODE-GEN PRP 180V 200MA DO-7	28480	1901-0033
R1	0683-4725	2	3	RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R2	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R3	0683-4725	2		RESISTOR 4.7K 5% .25W FC TC=-400/+700	01121	CB4725
R4	0757-0447	4	1	RESISTOR 16.2K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1622-F
R5	0757-0428	1	1	RESISTOR 1.62K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1621-F
U11	1820-1918	2	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS241N
U13	1820-1077	4	4	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U15	5180-0189	3	1	IC-ROM	28480	5180-0189
U16	1818-1663	9	16	IC-D2125H-1	34649	D2125H-1
U17	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U18	1820-1015	0	3	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U19	1820-2184	6	2	IC LCH TTL S OCTL	50364	74S373N
U21	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U23	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U26	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U27	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U28	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U29	1820-2184	6		IC LCH TTL S OCTL	50364	74S373N
U31	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U32	1820-1450	7	2	IC BFR TTL S NAND QUAD 2 INP	01295	SN74S37N
U33	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U35	5180-0190	6	1	IC-ROM	28480	5180-0190
U36	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U37	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U38	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U39	1820-1449	4	3	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U41	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U42	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U43	1820-1077	4		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S157N
U46	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U47	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U48	1820-1445	0	1	IC LCH TTL LS 4-BIT	01295	SN74LS375N
U49	1820-2102	8	4	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U51	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U52	1820-1287	8	1	IC BFR TTL LS NAND QUAD 2-INP	01295	SN74LS37N
U53	5180-0126	8	4	IC-RAM 2148 HL	28480	5180-0126
U56	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U57	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U58	1820-1204	9	1	IC GATE TTL LS NAND DUAL 4-INP	01295	SN74LS20N
U59	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N

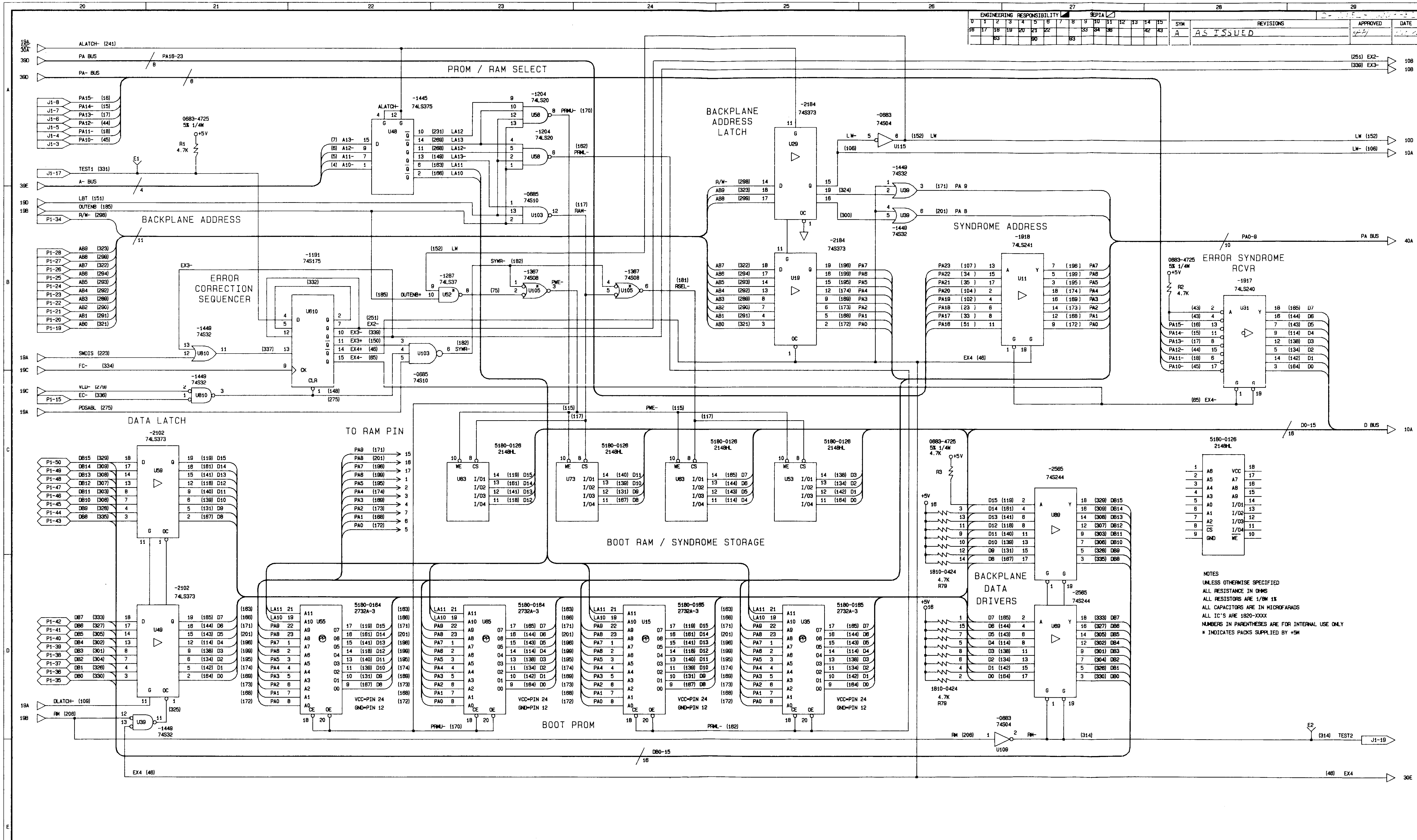
Table 5-1. Memory Controller Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U61	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U62	1810-0335	4	1	RESISTIVE NETWORK-DIP	01121	314A561
U63	5180-0126	8		IC-RAM 2148 HL	28480	5180-0126
U66	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U67	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U68	1820-1638	3	2	IC GEN TTL S PAR GEN 9-BIT	01295	SN74S280N
U69	1820-2565	7	2	IC BFR TTL S LINE DRVR OCTL	34335	AM74S244N
U71	1820-1997	7	4	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U72	1820-1430	3	3	IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U73	5180-0126	8		IC-RAM 2148 HL	28480	5180-0126
U76	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U77	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U78	1820-1638	3		IC GEN TTL S PAR GEN 9 BIT	01295	SN74S280N
U79	1810-0424	2	1	RESISTIVE NETWORK-DIP	11236	761-1-R4.7K
U81	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U82	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U83	5180-0126	8		IC-RAM 2148 HL	28480	5180-0126
U85	1820-1991	1	1	IC CNTR TTL LS DECD DUAL 4 BIT	01295	SN74LS390N
U86	1818-1663	9		IC D2125H-1	34649	D2125H-1
U87	1818-1663	9		IC-D2125H-1	34649	D2125H-1
U88	1820-1158	2	2	IC GATE TTL S AND OR-INV DUAL 2-INP	01295	SN74S51N
U89	1820-2565	7		IC BFR TTL S LINE DRVR OCTL	34335	AM74S244N
U91	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U92	1820-1430	3		IC CNTR TTL LS BIN SYNCHRO POS-EDGE-TRIG	01295	SN74LS161AN
U93	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U95	1820-1205	0	1	IC GATE TTL LS AND DUAL 4-INP	01295	SN74LS21N
U96	1820-0686	9	2	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U97	1820-1322	2	1	IC GATE TTL S NOR QUAD 2 INP	01295	SN74S02N
U98	1820-1158	2		IC GATE TTL S AND OR-INV DUAL 2 INP	01295	SN74S51N
U99	1820-1633	8		IC BFR TTL S INV OCTL 1 INP	01295	SN74S240N
U101	1820-1997	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U102	1820-1275	4	1	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U103	1820-0685	8	2	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U105	1820-1367	5	2	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U106	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U107	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U108	1820-0629	0	3	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U109	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U111	1820-2024	3	2	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U112	1820-0686	9		IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U113	1820-0685	8		IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U115	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U116	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U117	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U118	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U119	1810-0182	9	1	RESISTIVE NETWORK-DIP	28480	1810-0182
U121	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U122	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U123	1820-1144	6	1	IC GATE TTL LS NOR QUAD 2-INP	01295	SN74LS02N
U124	1820-2466	7	1	IC TIMER CMOS	32293	ICM7555IPA
U125	1820-1425	6	1	IC SCHMITT-TRIG TTL LS NAND QUAD 2-INP	01295	SN74LS132N
U126	1820-0693	8	2	IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U127	1820-0693	8		IC FF TTL S D-TYPE POS-EDGE-TRIG	01295	SN74S74N
U128	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U129	1810-0256	8	1	RESISTIVE NETWORK-DIP	01121	316A102
U610	1820-1191	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG COM	01295	SN74S175N
U810	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N



NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5M

DRAWN BY	DATE 1/29/82	A700 MEMORY CONTROLLER	HEWLETT PACKARD
ENGINEER		TITLE	
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG.		SHEET 1 OF 4	D-12152-60003-51



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RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER
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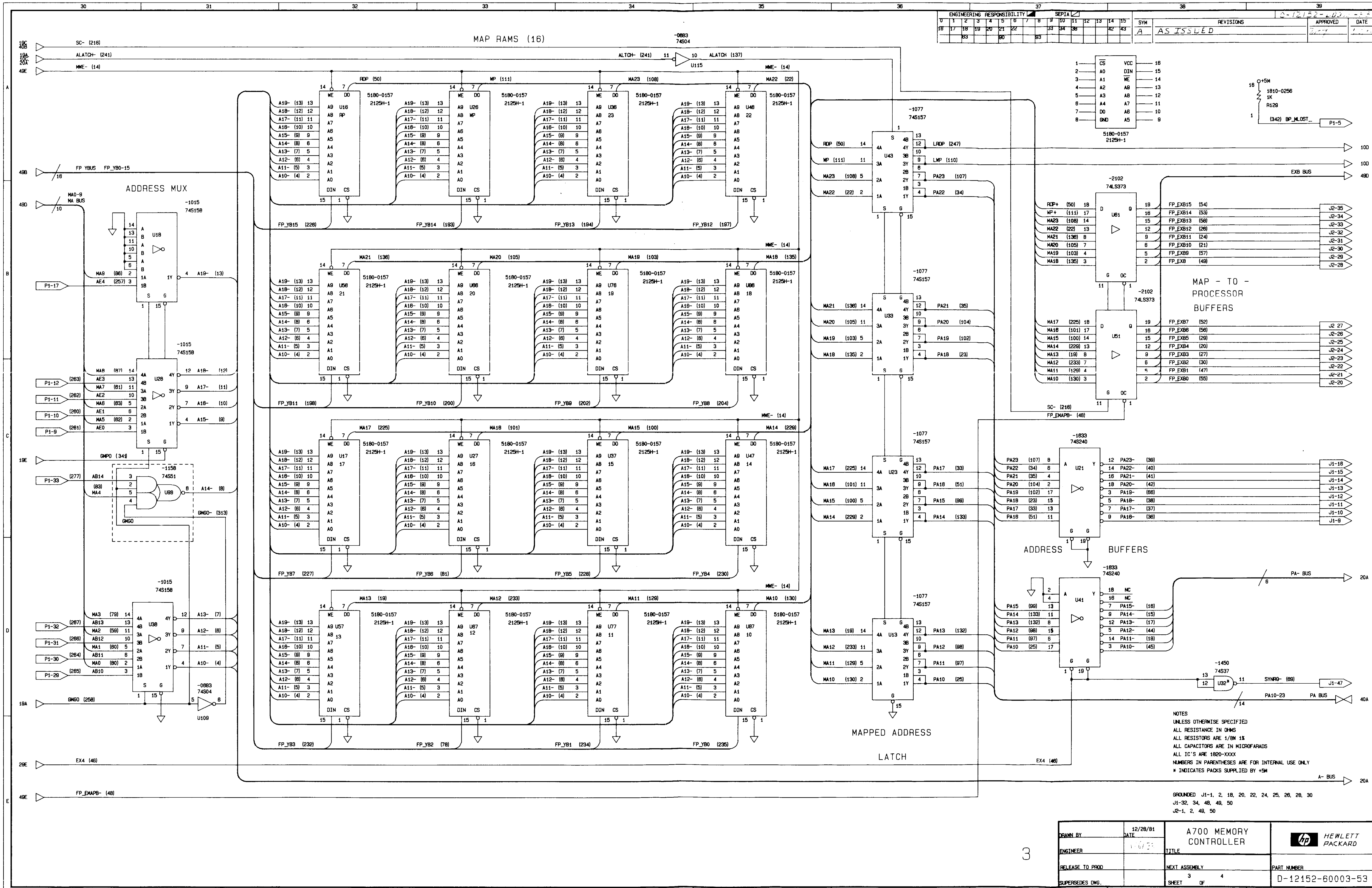
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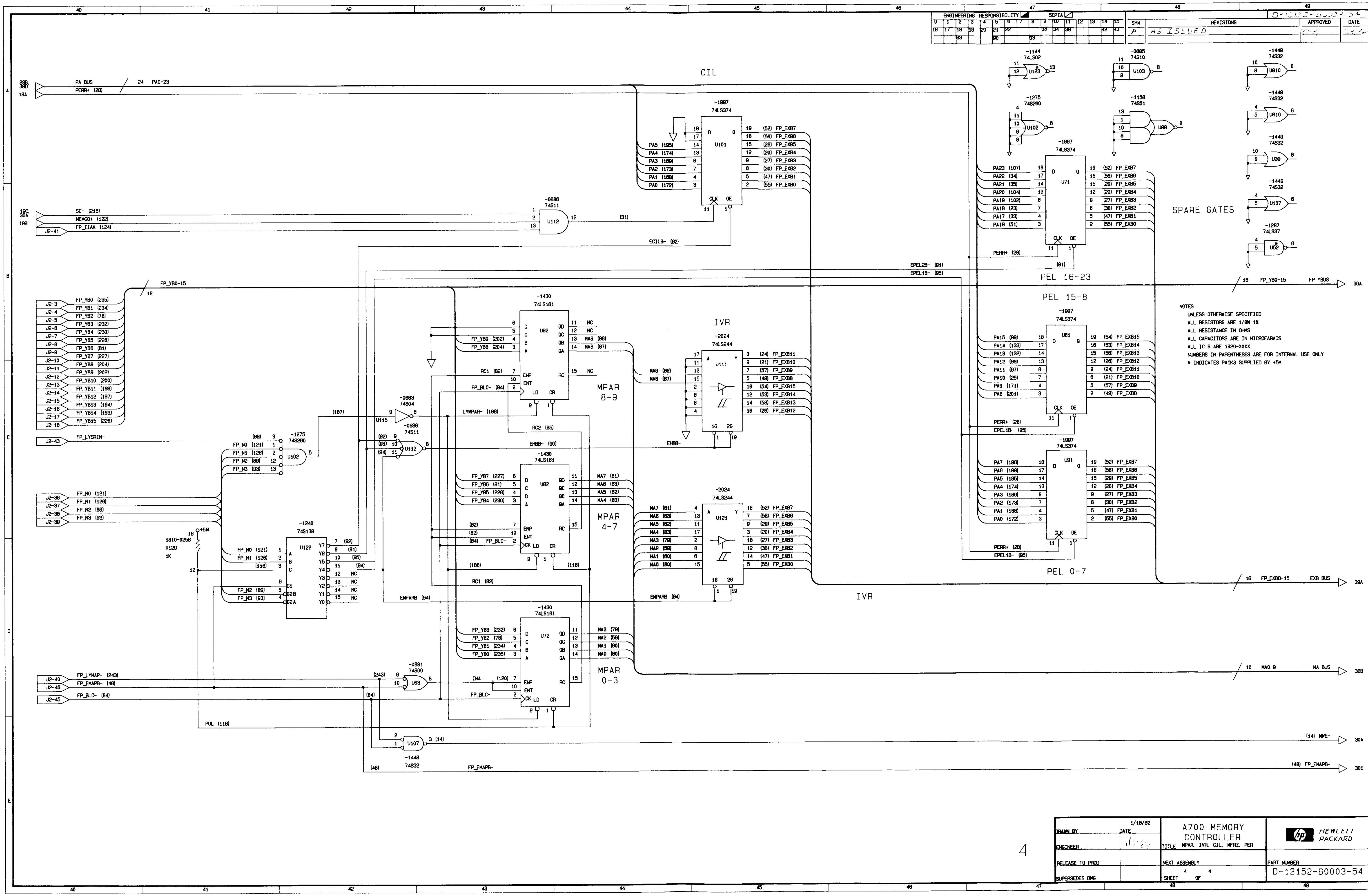
ADDRESS MUX
MAPPED ADDRESS
LATCH
MAP - TO - PROCESSOR BUFFERS
ADDRESS BUFFERS
5180-0157
2125H-1
74S158
74S157
74LS373
74S240
74S51
74S04
74S37
SC- (216)
ALATCH- (241)
MME- (14)
FP YBUS FP_YB0-15
MA0-9 MA BUS
EXB BUS
PA- BUS
PA BUS
A- BUS
SYNRQ- (69)
EX4 (46)
FP_EMAPB- (48)
GMG0 (258)
1810-0256
1K
R129
(342) BP_MLOST_
NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5M
GROUNDED J1-1, 2, 18, 20, 22, 24, 25, 26, 28, 30
J1-32, 34, 48, 49, 50
J2-1, 2, 48, 50
ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
A
AS ISSUED
DRAWN BY
DATE 12/28/81
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
A700 MEMORY CONTROLLER
TITLE
NEXT ASSEMBLY
SHEET 3 OF 4
PART NUMBER
D-12152-60003-53
HEWLETT PACKARD
3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PEL 0-7
IVR
MPAR 8-9
MPAR 4-7
MPAR 0-3
SPARE GATES
PA BUS
PERR+ (28)
24 PA0-23
SC- (218)
MEMGO+ (122)
FP_IIAK (124)
ECILB- (92)
EPEL2B- (91)
EPEL1B- (95)
FP_YB0-15
16 FP_YB0-15 FP YBUS 30A
16 FP_EXB0-15 EXB BUS 39A
10 MA0-9 MA BUS 30B
(14) MWE- 30A
(48) FP_EMAPB- 30E
FP_LYSRIN-
FP_LYMAP- (243)
FP_EMAPB- (48)
FP_BLC- (84)
EMPARB (84)
EHBB- (90)
LYMPAR- (186)
PUL (116)
1810-0256
R129
1K
-1997 74LS374
-1430 74LS161
-2024 74LS244
-1240 74S138
-1275 74S260
-0686 74S11
-0683 74S04
-0681 74S00
-1449 74S32
-1144 74LS02
-0685 74S10
-1156 74S51
-1287 74LS37
NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5M
DRAWN BY
DATE 1/18/82
ENGINEER
RELEASE TO PROD
SUPERSEDES DWG.
A700 MEMORY CONTROLLER
TITLE MPAR, IVR, CIL, MFRZ, PER
NEXT ASSEMBLY
SHEET 4 OF 4
HEWLETT PACKARD
PART NUMBER
D-12152-60003-54
4

6.1 INTRODUCTION

This section covers the HP 12103-series memory array cards. The HP 12103A, HP 12103B, and HP 12103C are identical except for the number of the RAM chips installed on them. The HP 12103D has a different parts layout to accomodate twice the number of RAMs as the HP 12103C array card. These memory array cards are described as though there were one basic card but the differences on them are mentioned wherever a difference exists.

The memory array cards described in this section include parity checking and they are considered to be standard memory cards as compared to the HP 12104A Error Correcting Memory Card covered in Section VII of this manual.

The parity-check type memory array cards for A700 Computers are the following:

HP 12103A: 128 Kilobyte Memory Array Card, part no. 12103-60001

HP 12103B: 256 Kilobyte Memory Array Card, part no. 12103-60002

HP 12103C: 512 Kilobyte Memory Array Card, part no. 12103-60003

HP 12103D: 1024 Kilobyte Memory Array Card, part no. 12103-60004

6.2 PHYSICAL CHARACTERISTICS

The memory array cards are installed in the A700 backplane above the memory controller card (see Figure 1-2 in Section I). Additional array cards are added in successive fashion with the memory frontplane connecting each array card.

All signals and data are Schottky-TTL levels and comply with Schottky TTL design rules. The HP 12103B memory array card is shown in Figure 6-1. The HP 12103A, HP 12103B, and HP 12103C are identical except for differing amounts of 64 kilobyte RAMs. The HP 12103D one megabyte memory array is shown in Figure 6-2.

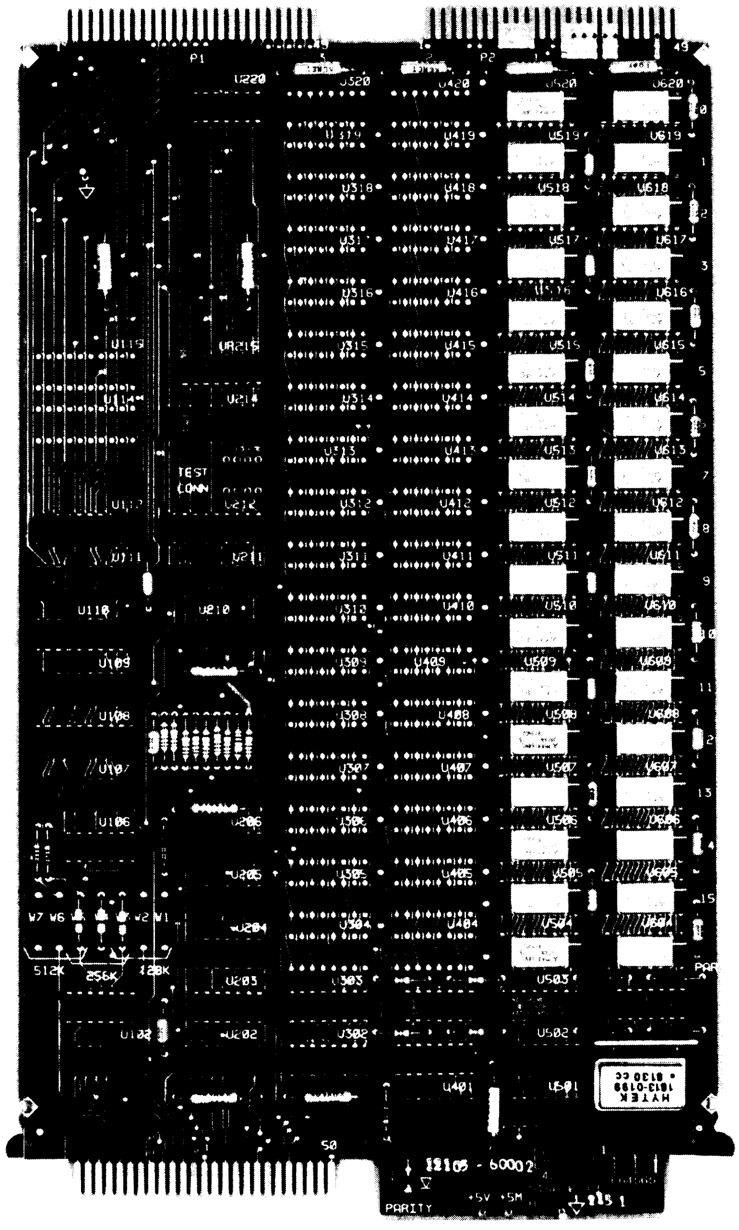


Figure 6-1. HP 12103B 256kb Memory Array Card

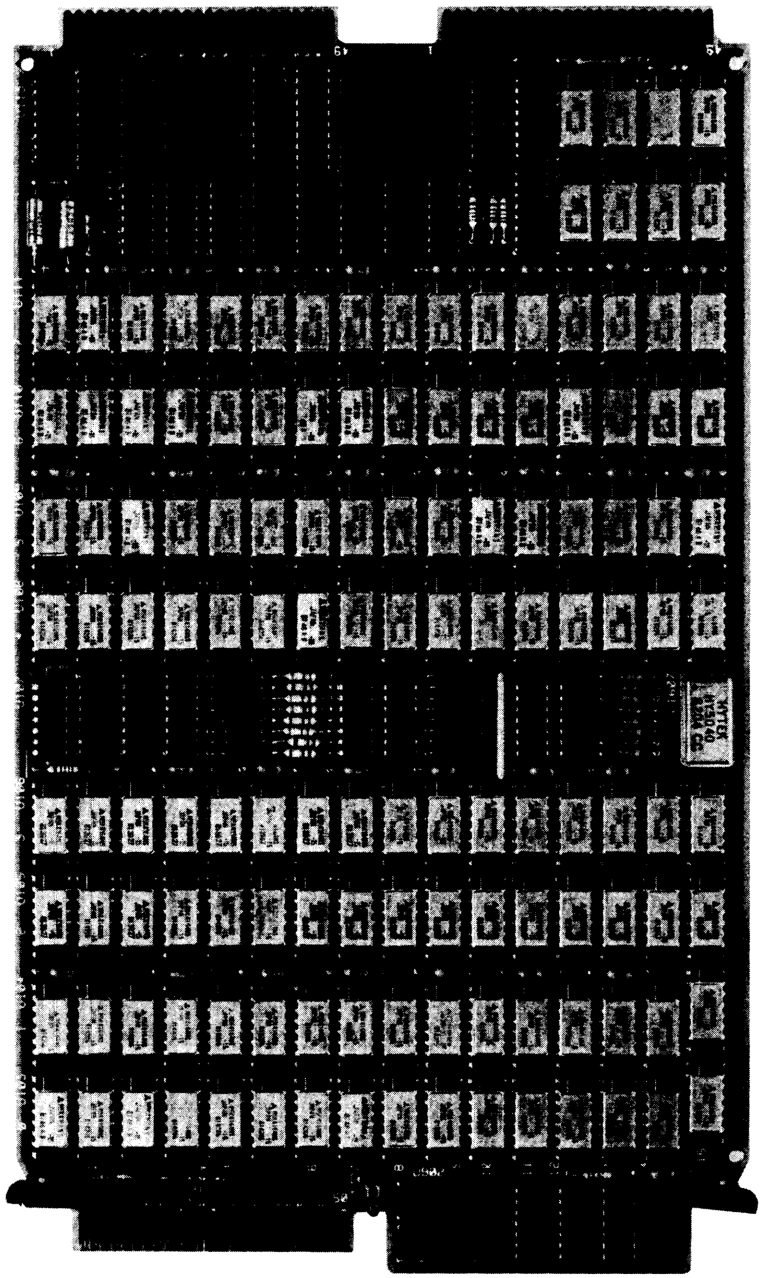


Figure 6-2. HP 12103D 1Mb Memory Array Card

No jumper or switch settings are necessary for configuring the array cards for insertion into the system (jumpers on the cards are preset at the factory for the size of the memory on the card.

The power supply specifications for the cards are covered in Section I of this manual. The total operating power is not the summation of each card's operating power specification. This results from the fact that power consumption is proportional to the access rate and only one card is accessed at any one time; therefore, only one card at a time is operating. Meanwhile, all other array cards dissipate standby power.

6.3 MEMORY ARRAY CARD OPERATION

6.3.1 MODULE CONFIGURATION CIRCUIT

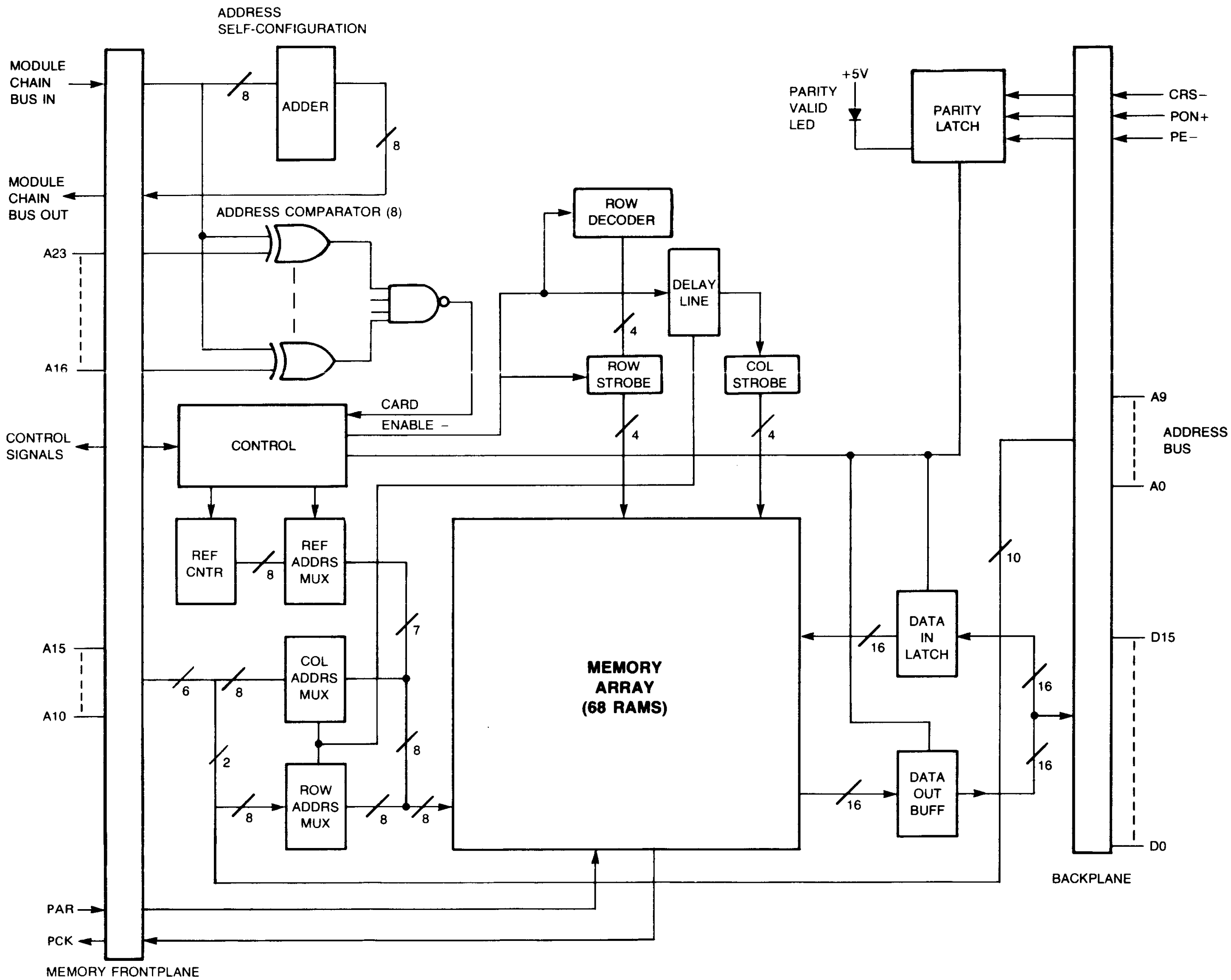
The memory array cards in the A700 memory system are where the actual data is stored in the memory system. Operation of the memory array cards is described below. Refer to the block diagram provided in Figure 6-3.

Each array card, when installed, occupies a unique address space so that the controller may access it by address only. To accomplish this, each array card has an adder that takes a chained address from the previous card, adds the number of rows of RAMs on the card, and passes this incremented address over the frontplane to the next higher array card on the backplane. These incremented addresses are essentially the starting address for each array card and, when compared to the physical address (on the frontplane), form a basis for selecting the array cards. The main memory address into the first card above the controller is 0000 (octal).

Since each array card sends an incremented number equal to the number of rows of RAMs on the card to the next array card on the backplane, the array cards automatically configure themselves in an ascending address order. Thus, if two cards are interchanged, they automatically reconfigure themselves to form the ascending address sequence. The advantage of this scheme is that identical memory modules become unique in the address space of the computer without the aid of manually selected switch or jumper settings unique to the location or dedicated backplane locations.

6.3.2 ARRAY CARD SELECT

Each memory array card receives the physical address sent by the memory controller over the frontplane. Using XOR gates, the cards compare the physical address with the incremented address (see previous paragraph). When a match is encountered on a card, the outputs of all its XOR gates go high causing its card select line to go true (This can happen on only one array card at a time). When a card select line is true that card is enabled for access to the RAM array.



8200-150

Figure 6-3. Memory Array Card Block Diagram

6.3.3 RAM ARRAY

The RAM array consists of dynamic MOS memory elements in 16-pin DIP packages with 64k bits per package. The RAMs are arranged on the 128-, 256-, and 512-kilobyte array cards in rows of 17 to provide sixteen data bits plus one parity bit. The 128-kilobyte card has one row of RAMs, the 256 kilobyte card has two rows of RAMs, and the 512-kilobyte card has four rows of RAMs. The 1-megabyte card has eight rows of RAMs

Each word of data written into memory is stored in one row of the array. Thus, during any access only one row of RAMs is activated. (This is not true of refresh cycles which access all rows of all array cards simultaneously.) When an array card is not selected, all RAMs on that card are in standby mode. This greatly reduces power requirements on a system scale.

6.3.4 ROW DECODER

Row decoding is used to select a row of the RAM array for access. Bits 16 and 17 of the physical address on the frontplane are routed to the decoder which performs a four-out-of-two decoding function. The outputs of the decoder are then fed through the card select multiplexer to the row address strobe (RAS) buffer of the appropriate row. The RAS signal to the RAMs performs the chip select function. On the 1-megabyte card, address bit 18 is used to select a bank of four rows of RAMs with bits 16 and 17 selecting a row within the bank.

6.3.5 CLOCK GENERATION

The RAM elements need two clock signals to allow access to the array. This is necessary since the RAM elements are organized into a 64k x 1 matrix and thus require a 16-bit address to identify each memory cell. Since the RAM is housed in a 16-pin DIP package, there is an insufficient number of pins to allow direct addressing. Therefore, the 16-bit address is split into two groups of eight which are the lower-order address and the upper-order address (ROW and COLUMN).

The procedure for accessing the RAM cell is as follows:

1. Set up ROW address at RAM input.
2. Apply RAS clock to RAM.
3. Set up COLUMN address at RAM input.
4. Apply CAS clock to RAM.

The timing of these two clocks is critical to efficient memory timing. Therefore, a delay line is incorporated on each array card to ensure a tightly controlled time spacing between the RAS and CAS signals. Thus, when the RAS pulse arrives from the memory controller and is asserted at the RAMs, the CAS pulse occurs a precise time later at the RAMs.

6.3.6 ADDRESS MULTIPLEXER

Equally as critical as the timing of the RAS and CAS pulses is the timing of the multiplexer switching of the ROW and COLUMN addresses. To insure the correct timing between clocks and address switching, the same delay line is used to switch the multiplexer from ROW address to COLUMN address. This signal occurs from an intermediate tap on the delay line.

A third group of address bits is the refresh address needed for the memory refresh operation. Only seven bits of address are needed by the RAMs since refreshing is done by rows in the RAM elements. This address is switched to the RAMs during every refresh cycle. Control of the refresh multiplexer is handled from the memory controller by the RC- signal over the frontplane.

6.3.7 DATA LATCH

During a write cycle, data is latched on each array card at the beginning of the memory cycle. The latch signal is generated on the memory controller and is routed to all array cards over the frontplane. The latching function occurs on all array cards even though the data is only being written to one particular card. The latch signal occurs at different times depending on whether the memory write is occurring from the processor or a peripheral device using DMA.

In the case of a DMA write, the data is latched while it is valid on the backplane during MEMGO. In the case of a processor write, the data is latched on the leading edge of OUTEN. The processor holds data valid on the backplane for the long half cycle of the system clock following MEMGO.

6.3.8 PARITY STATUS LED

The green parity error LED is controlled by a NAND-latch circuit on each array card which monitors the PE signal on the backplane and the card select signal. Thus, when a parity error occurs, the memory controller asserts the PE signal and the appropriate LED is turned off.

The latch circuit can be reset by asserting a CRS (Control Reset) signal on the backplane (execution of a CLC 0 instruction). Also, the latch is initialized during system turn-on by the PON signal.

6.4 THEORY OF OPERATION

The integrated circuit packages (chips) are referenced by their U-numbers and schematic locations. For example, U69 (13-C) means chip 69 on schematic sheet no. 1 is located by coordinates 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc, and on sheet no. 2 it is numbered 20, 21, etc. In the text all chip references for the 12103A/B/C cards are followed by a chip reference for the 12130D in brackets [ ], if it is different. The schematic locations are included in the same way (see Figure 6-3 and the schematics for these cards located at the rear of this section).

6.4.1 MODULE ADDRESSING CIRCUIT

The module addressing circuit is used to automatically configure the array cards into the address space of the A700 Computer. This is accomplished by using eight chained lines on the memory frontplane to allow the passing of unique addresses to each array card. Each array card uses the address sent to it as the starting address of its address space.

The array card sends an address to the array card above it which has been incremented by the number of rows of RAMs on the card. This address is used as the starting address of that next array card. In this manner, each array card is located on a unique address boundary in the memory address space. Also, each array card is in sequence with the others; the beginning of memory is located on the array card next to the controller and the end of memory is on the array card farthest from the controller.

The module addressing circuit is implemented by using two 4-bit full adders U102 (23-B) and U202 (23-A). These adders are connected in cascade to perform full eight-bit addition. Jumpers located at W1, W4 and W7 determine the capacity of the array card by setting the number to be added to the incoming address to form the outgoing address to the next array card. The 1-megabyte card adds eight bits to the memory chain address using an additional four-bit adder U113 (12-A).

The memory capacity of each array card is determined by the number of RAMs loaded. The 12130A/B/C card has a maximum of four rows of 17 RAMs of capacity. Since 64k RAMs are used, the capacity of each row is 64k words or 128k bytes of memory. Three configurations are allowed: 128k, 256k and 512k corresponding to one, two, or four rows of RAMs loaded, respectively. At the time of manufacture, the desired number of rows are loaded and the jumpers set accordingly. The card will then send the correct incremented address to the next array card when installed in a system. The 12103D 1Mb card cannot be partially loaded, and therefore it has no jumper options.

In operation, the eight bits of chained address are compared to the upper eight bits of physical address present on the memory frontplane. (The lower order 16 bits are used to address locations in the RAM chips themselves.) These eight bits are used to determine which card is to be selected when a given address is present. The card select signal is generated by the NAND-gate U204 (23-C) [U1402 at 12-B]

This eight input gate receives the outputs of the XOR-gates at U103 (22-D) and U203 (22-C) [U1202 at 11-C and U1302 at 11-B]. In operation, the outputs of all the XOR-gates must be high for the card to be selected in the following way:

The physical address is low true while the chained address is high true so that the comparison of these two signals is equal when one is low and the other is high. The output of the XOR gates under the equal condition is, therefore, high.

The following is a detailed explanation of how the card select circuit operates in the 12103A/B/C for the three memory card configurations mentioned above: Consider the case of one row of RAMs loaded on the card. The capacity of the card is 128kb. In this case, address bits 16 and 17 do not need to select the row of RAMs to be accessed. Jumpers W5 and W6 are not present and the select lines to U402 (13-D) are pulled high by R1 and R2 so that row 0 is always selected. Also, jumpers W2 and W3 are present since only one combination of the A16 or A17 address lines represents an address on this array card. Jumper W1 is present to add a one to the chain address so that the next array card will respond to an address that is one greater than the address to which the present array card will respond. (Note that this address would have been on the present array card if more than one row of RAMs were installed.)

When two rows are loaded, (capacity = 256kb) bit 16 of the physical address is ignored by the card select circuit. This results from the fact that A17 and A16 select the row of RAMs to be accessed on the card. Bit 16 is the least significant bit and it selects either row 0 or row 1. Since both rows are on the same card, the card select signal must remain true regardless of the state of A16. Therefore, jumper W2 is not present and the corresponding input to U204 is pulled high by the 2.2k ohm resistor at UR-215-9 (28-D). Jumper W6 is not present so that row 2 and row 3 can never be selected since there are no RAMs in those rows. Jumper W5 is present to allow row 0 and row 1 selection. Jumper W4 is present to add a two to the chain address so that the next array card will respond to an address that is two greater than the one to which the present array will respond.

In the case of a fully loaded card, (capacity = 512 kilobyte) jumpers W5 and W6 are both present to allow address decoding to select all four rows of the array card. Jumpers W2 and W3 are both absent and the corresponding inputs of U204 are pulled high so that the card select circuit ignores bits A16 and A17. Thus, the card remains selected while bits A16 and A17 select the desired row of RAMs. Jumper W7 is present to add a four to the chain address. (Note: The 12103D has no jumper options.)

An important restriction must be placed on the position of partially loaded array cards in the computer system. All cards MUST be located on an address boundary where the starting address for the card can be evenly divided by the memory capacity of the card. That is, a 512k-byte card can only be installed where its starting address would be an even multiple of 512k bytes and so on. (Note that a 128k-byte card can never be installed on an incorrect boundary.) An example of an incorrect installation would be to have one 128k-byte card as the first card in the system followed by a 512k-byte card. The correct installation would be to reverse the array cards. However, the preferred way of installing array cards in the system is to install them in order of decreasing size since this always ensures proper placement. (Any card can be installed on the zero, or first, address location) The following example illustrates the order of memory array card placement:

MEMORY ARRAY PLACEMENT IN COMPUTER BACKPLANE

(Incorrectly installed card indicated by >)

WRONG	WRONG	WRONG	CORRECT	CORRECT	CORRECT PREFERRED	CORRECT PREFERRED
512k	128k	512k	512k	1M	128k	128k
128k	> 256k	> 1M	128k	256k	128k	128k
> 256k	> 512k	128k	128k	256k	256k	512k
128k	128k	128k	256k	512k	512k	1M
*	*	*	*	*	*	*

* Controller card.

The reason for the restriction is that the jumper scheme assumes that row selection on a 512 kilobyte card occurs with address bits 16 and 17 going through the sequence of 00, 01, 10, 11 with NO CHANGE on address bit 18, and thus is located on a 512 kilobyte boundary in the address space. If address bit 18 did change, the card could not remain selected.

Similarly, the 1 megabyte card only looks at address bits A19-A24 for board selection, and assumes that memory chain bits MIO, 1, and 2 are all low, which only happens on 1 megabyte boundaries.

Also similarly, for a 256 kilobyte card, address bit 17 is assumed to be stationary while bit 16 selects either row 0 or row 1. This condition is only met on a 256 kilobyte boundary. This restriction does not apply to 128 kilobyte cards since all outputs of the XOR gates are examined for equality and row 0 is forced to be selected by the absence of jumpers W5 and W6.

6.4.2 RAS GENERATION

The RAS pulse is used to initiate every access and to perform refreshes to the RAM array.

The RAS (Row Access) pulse is generated on the memory controller and is sent to all array cards via the memory frontplane. It is received by U502-5 (14-B) [U107-5 at 13-C in the 12103D] and is routed to RAS drivers U403 (16-E) [U807 at 25-D and U907 at 26-D in the 12103D]. The RAS path is enabled through gate U502 since the LTNG- line is high at U502-6. The RAS path is always enabled on the 12103D.

When the RAS pulse occurs, the proper row of RAMs to be accessed has already been determined, and the appropriate RAS driver is enabled by U303 (15-D) [U307 at 23-D or U407 at 24-D on the 12103D]. RAS then passes through to the selected row.

6.4.3 ROW SELECTION

The proper row of memory to be accessed is determined by physical address bits 16 and 17. These bits are routed to multiplexer U402-3 and -6 (13-E) [U1213-3 and -6 at 13-C]. The B inputs of this multiplexer are selected so that the address bits pass through to U302-3 and -2 (14-E) [U207 at 12-D] which is a one-of-four decoder. This decoder determines which row to enable from the binary code on the address lines and sets the appropriate line high to the RAS drivers of U403 [U807 and U907].

During refresh cycles, all four outputs of the multiplexer are high to enable RAS to all rows simultaneously. This occurs by asserting the BREF+ signal at U303-15 (15-D) [U307-15 at 23-D and U407-15 at 24-D] high for the duration of the refresh cycle.

6.4.4 CARD SELECT CONTROL

When the correct address is present on the frontplane, the card select circuitry enables the card as described in paragraph 6.4.1. The card is enabled by the card select signal BDSEL generated at U204-8 (23-C) [U1402-8 at 12-B]. This signal enables the card for a memory access in several ways.

First, the BDSEL (Board Select) line is sent to NAND gate U210 (14-15-D) [U812 at 26-E]. At U210-9 [U812-12], the DRIVE signal is enabled so that the array card may drive the backplane if the present cycle is a read access. In the case of a write access, the W+ signal at U210-13 [U107-9] is enabled to the RAMs. Next, the BDSEL- line is routed to U303-1 (15-D) which switches the multiplexer to select the proper row as described in paragraph 6.4.3.

On the 12103D, the BDSEL line is decoded with A18 by U812 (22-E) to produce bank select signals BDSELL and BDSELH. BDSELL goes to U307-1 and DBSELH goes to U407-1, which allows the proper row of RAMs to be selected.

When the card is not selected, the multiplexer at U303 [U307 and U407] has the B inputs selected. These inputs are all high since the LTNG- signal at U302-15 [U207-15] is high. Therefore, when the array card is not selected, all RAS driver inputs at U403 [U807 and U907] are disabled.

The row address to U303 [U307 and U407] is set up before the BDSEL- signal switches the multiplexer. Thus, when the RAS pulse occurs, only one row of RAMs is allowed to receive the RAS signal.

6.4.5 CAS GENERATION

The CAS (Column Access) pulse is used to strobe the second half of the address into the RAMs during a memory access. The CAS pulse to the RAMs is generated from the RAS pulse through the use of a delay line located at U601 (15-C) [U1607 at 24-E]. The delay inserts the minimum time required for the RAM address bus to switch from the row address to the column address.

The CAS pulse is sent to CAS drivers U603 (16-B, C) [U1207 at 26-D and U1307 at 27-D]. Note on the schematic that the CAS pulse only appears at the RAMs if the CASEN (CAS Enable) signal is asserted. In the case of a read access, the CASEN signal will be asserted BEFORE the delay line CAS is asserted, so that the RAS-CAS sequence occurs as quickly as possible.

In the event of a write cycle, the CASEN signal occurs AFTER the delay line CAS occurs so that the write is delayed to allow for the parity bit to be generated and sent from the memory controller. Also, since the delay line signal CAS occurs every time the RAS pulse occurs, the CASEN signal is used to inhibit unwanted CAS cycles during memory refreshes and memory protect violations. For more information on this subject, refer to paragraph 5.6.6.8 in Section V on Normal Main Memory Access.

Since the CAS pulse holds the accessed data valid at the output of the memory RAMs during a read cycle, CAS at the RAMs remains asserted until the memory cycle completes. This is done by latching RAS, which holds CAS (otherwise it would terminate 60 nanoseconds after the controller RAS signal terminates).

In operation, the CASEN and VALID signals are gated by U501-1 and -2 (13-C) [U912-5 and -4 at 12-C], and present a latched RAS signal to U502-4 (14-C) [U107-1 and -2 at 13-C].

Thus, RAS to the RAMs is extended to the end of the VALID signal and the delay line CAS is correspondingly extended. This provides sufficient extra time for the delay line CAS to hold data valid until the end of the memory cycle.

6.4.6 ADDRESS MULTIPLEXER

The addresses used by the memory RAMs are controlled by the address multiplexer chips U107 (12-A), U108 (12-B), and U109 (12-C). For the 12103D the multiplexer chips are U213 (21-A), U902 (21-B), and U413 (21-B) for the high bank; and U313 (21-C), U901 (21-D, and U513 (21-D) for the low bank.

The address multiplexer presents the row and column addresses as well as the refresh addresses to the RAMs. Latch U109 [U413 and 513] is used to latch the lower-order eight bits of physical address directly from the backplane. The output of this latch is used as the row address to the RAMs. After the RAS pulse occurs and the address hold time at the RAMs is satisfied, the delay line asserts the COLEN signal at U401-13 (11-C) and U501-9 (12-C) [U512-2 at 22-D and U912-10 at 22-D] which disables the output of the row driver U109 [U413 and U513] and enables the output of column driver U108 [U901 and 902].

After the column address has had sufficient time to settle, the CAS pulse is asserted at the RAMs.

When a refresh cycle is initiated, the REF+ signal appears at U401-12 [512-1] and inverted at U501-10 [912-9]. This signal disables the outputs of both the row and column address drivers U109 (12-C) and U108 (12-B) [U413, U513, U901, and U902] and enables the refresh address driver U107 (12-A) [U213 at 21-A and U313 at 21-C]. This presents the refresh address to the RAMs.

6.4.7 ADDRESS LATCH

The lower order ten bits of physical address are latched directly from the backplane. Bits 0-7 are latched by U109 [U413 and U513] and are presented to the RAMs as the row address. Bits 8 and 9 are latched by U214 (11-E) [U1013 at 11-D]. These two bits are then sent to U402-10 and -13 [U1213-10 and -13] from which they are routed to U108-15 and -17 [U901 and U902 -2 and -4] to be used as the first two bits of the column address.

6.4.8 DATA LATCH

Data is latched directly from the backplane using U111 (18-B) and U211 (18-A) [U813 at 29-B and U913 at 29-A]. These latches are transparent so that as data becomes available on the backplane, it is sent to the RAMs before the LATCH signal freezes the latch. These latches hold the input data at the RAMs during every write cycle.

6.4.9 BACKPLANE DATA DRIVERS

Data is driven onto the backplane by two octal drivers U112 (18-C) and U212 (18-C) [U613 at 29-D and U713 at 29-C]. The outputs of these drivers are enabled by the BDRIVE signal whenever the card is selected and the memory access is a read cycle.

6.4.10 PARITY LED LATCH

Whenever the parity of data being accessed from the card is not correct, the controller asserts a parity interrupt signal to the processor and memory array. This is the PE- (Parity Error) signal line. A memory array card must be enabled to monitor the PE- signal. The PE- signal is received at U220-13 (18-E) [U512-12 at 13-E] and if the BDRIVE- signal is asserted at U220-11 [U512-13], latch U220 [U912 and 612] will be reset, turning off the parity LED. This will identify this card as causing the parity error. The latch can be set again by issuing a CRS- (Control Reset) signal or by turning the system off and then on again.

6.4.11 REFRESH COUNTER

Refresh addresses are generated on the array card. Counter U106 (11-A) [U312 at 20-A] is used to count in a binary sequence to generate the 128 row addresses needed for refresh cycles. Note that eight bits are generated and sent to the RAMs but only seven are needed. The counter is clocked by the COUNT+ signal from U210 (15-C) [U412-1 at 21-A] which is a gated form of the REF signal. The counter is clocked at the end of each refresh cycle so that the refresh address is set up in time for the next refresh cycle.

6.4.12 FRONTPLANE HANDSHAKE SIGNALS

There are two signals passed over the frontplane from the standard array card to the memory controller whenever a memory access takes place. These are the acknowledge and parity check signals. Both signals are sent to the controller by the open collector driver U206 (24, 25-D) [U612 at 14-B]. The driver is enabled when the card is selected.

The acknowledge signal is sent as soon as the card is enabled to inform the controller that the address on the frontplane does indeed access an existent array card. The parity check bit is sent at the time that the parity bit has been accessed from the parity RAM. This is used by the controller in the parity checking process.

6.4.13 STAND-BY OPERATION

The standard array card maintains stored data when the +5V power supply is removed, provided that the +5M power supply is maintained and the memory controller continues to schedule refresh cycles. Since not all of the circuitry on the array card is necessary for refreshing, only that circuitry needed for refreshes is powered by +5M. All circuit chips designated by an asterisk (*) on the array card schematic receive +5M voltage. These are the only chips that are active when the array card is in standby mode during battery backup operation.

6.5 PARTS LOCATIONS

The parts locations for the 12103C memory array are shown in Figure 6-4. The 12103A and 12103B are identical except for the omission of rows U304-U320, U404-U420 and U504-U520 in the 12103A, and rows U304-U320 and U404-U420 in the 12103B.

The parts locations for the 12103D memory array are shown in Figure 6-5.

6.6 REPLACEABLE PARTS LIST

The replaceable parts for the 12103A, 12103B, and 12103C memory arrays are listed in Table 6-1 and the replaceable parts for the 12103D memory array are listed in Table 6-2. Refer to Table 3-8 for the names and addresses of the manufacturers of the parts in the Manufacturer's Code List.

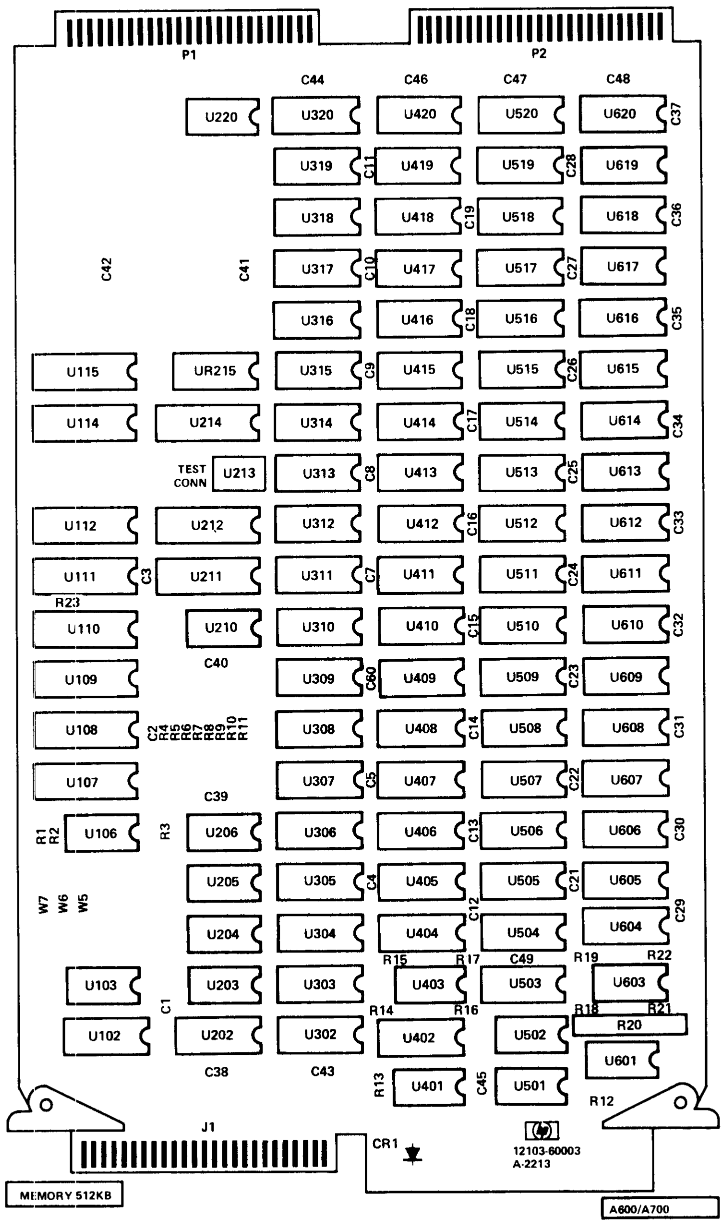


Figure 6-4. 12103C Parts Locations (12103A and 12103B are the same except for omitted RAMs and bypass capacitors)

12103A (12103-60001) Parts List - Sheet 1 of 2

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103-60001	2	1	PCA-ARRAY CARD	28480	12103-60001
C1	0160-4842	6	20	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C2	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C26	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C27	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C28	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C31	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C32	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C33	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C34	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C35	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C36	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C37	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C38	0180-0374	3	11	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C39	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C40	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C41	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C42	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C43	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C44	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C45	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C46	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C47	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C48	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C49	0160-4818	6	1	CAPACITOR-FXD 47 PF 10%	28480	0160-4818
CR1	1990-0598	1	1	LED-VISIBLE	28480	5082-4190
R1	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
R4	0757-0346	2	9	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R5	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R9	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R12	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R13	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R14	0757-0294	9	4	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R15	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R16	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R17	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R18	0698-3430	5	4	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R19	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R20	1810-0277	3	1	RESISTIVE NETWORK 9 X 2.2K OHM	01121	210A222
R21	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R22	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R23	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
U102	1820-1441	6	2	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U103	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U106	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U107	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U109	1820-1676	9	1	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U110	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U112	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U202	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U203	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U204	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U205	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U206	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U210	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N

Table 6-1. 12103A/B/C Replaceable Parts (continued)

12103A (12103-60001) Parts List - Sheet 2 of 2

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U211	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U212	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U214	1820-2786	4	1	IC-74F533PC	28480	1820-2786
U215	1810-0235	3	1	RESISTIVE NETWORK-DIP	01121	316A222
U220	1820-1414	3	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS12N
U302	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U303	1820-1015	0	2	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U401	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U402	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U403	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U501	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U502	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U503	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U601	1813-0199	4	1	IC-DELAY HY-5003	07910	HY-5003
U603	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U604	5180-0156	4	17	IC-RAM, 64K 75 NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U607	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U611	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U612	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U613	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U614	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U615	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U616	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U617	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U618	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U619	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U620	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
W1	0811-3587	5	3	RESISTOR-FXD 0 OHM	28480	0811-3587
W2	0811-3587	5		RESISTOR-FXD 0 OHM	28480	0811-3587
W3	0811-3587	5		RESISTOR-FXD 0 OHM	28480	0811-3587

Table 6-1. 12103A/B/C Replaceable Parts (continued)

12103B (12103-60002) Parts List - Sheet 1 of 2

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103-60002	3	1	PCA-ARRAY CARD	28480	12103-60002
C1	0160-4842	6	20	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C2	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C26	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C27	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C28	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C31	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C32	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C33	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C34	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C35	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C36	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C37	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C38	0180-0374	3	11	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C39	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C40	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C41	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C42	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C43	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C44	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C45	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C46	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C47	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C48	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
CR1	1990-0598	1	1	LED-VISIBLE	28480	5082-4190
R1	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
R4	0757-0346	2	9	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R5	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R9	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R12	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R13	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R14	0757-0294	9	4	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R15	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R16	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R17	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R18	0698-3430	5	4	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R19	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R20	1810-0277	3	1	RESISTIVE NETWORK 9 X 2.2K OHM	01121	210A222
R21	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R22	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
U102	1820-1441	6	2	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U103	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U106	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U107	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U109	1820-1676	9	2	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U110	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U112	1820-2699	8	2	IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U202	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U203	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U204	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U205	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U206	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U210	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N

Table 6-1. 12103A/B/C Replaceable Parts (continued)

12103B (12103-60002) Parts List - Sheet 2 of 2

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U211	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U212	1820-2699	8		IC DRVR TTL F LINE DRVR OCTL	07263	74F241PC
U214	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U215	1810-0235	3	1	RESISTIVE NETWORK-DIP	01121	316A222
U220	1820-1414	3	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS12N
U302	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U303	1820-1015	0	2	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U401	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U402	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U403	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U501	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U502	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U503	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE TRIG	01295	SN74S112N
U504	5180-0156	4	34	IC-RAM, 64K 75 NS	28480	5180-0156
U505	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U506	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U507	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U508	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U509	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U510	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U511	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U512	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U513	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U514	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U515	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U516	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U517	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U518	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U519	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U520	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U601	1813-0199	4	1	IC-DELAY HY-5003	07910	HY-5003
U603	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U604	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U607	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U611	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U612	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U613	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U614	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U615	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U616	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U617	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U618	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U619	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U620	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
W3	0811-3587	5	3	RESISTOR-FXD 0 OHM	28480	0811-3587
W4	0811-3587	5		RESISTOR-FXD 0 OHM	28480	0811-3587
W5	0811-3587	5		RESISTOR-FXD 0 OHM	28480	0811-3587

12103C (12103-60003) Parts List - Sheet 1 of 3

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103-60003	4	2	PCA-ARRAY CARD	28480	12103-60003
	12103-60003	4		ASSEMBLY-AUTO INSERT	28480	12103-60003
C1	0160-4842	6	37	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C2	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C4	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C5	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C6	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C7	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C8	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C9	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C10	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C11	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C12	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C13	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C14	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C15	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C16	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C17	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C18	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C19	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C20	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C26	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C27	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C28	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C31	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C32	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C33	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C34	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C35	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C36	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C37	0160-4842	6		CAPACITOR-FXD .22 UF +80-10%	28480	0160-4842
C38	0180-0374	3	11	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C39	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C40	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C41	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C42	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C43	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C44	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C45	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C46	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C47	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C48	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C49	0160-4818	6	1	CAPACITOR-FXD 47 PF 10%	28480	0160-4818
CR1	1990-0598	1	1	LED-VISIBLE	28480	5082-4190
R1	0757-0442	9	2	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R2	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R3	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
R4	0757-0346	2	9	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R5	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R9	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R10	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R11	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R12	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R13	0698-3447	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F
R14	0757-0294	9	4	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R15	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R16	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R17	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R18	0698-3430	5	4	RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R19	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R20	1810-0277	3	1	NETWORK-RES 10-SIP2.2K OHM X 9	01121	210A222

12103C (12103-60003) Parts List - Sheet 2 of 3

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R21	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R22	0698-3430	5		RESISTOR 21.5 1% .125W F TC=0+-100	03888	PME55-1/8-T0-21R5-F
R23	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
U102	1820-1441	6	2	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U103	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U106	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U107	1820-1917	1	1	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U109	1820-1676	9	1	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U110	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U112	1820-2699	8	2	IC-74F241PC	07263	74F241PC
U202	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U203	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U204	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U205	1820-0683	6	1	IC INV TTL S HEX 1-INP	01295	SN74S04N
U206	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U210	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U211	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U212	1820-2699	8		IC-74F241PC	07263	74F241PC
U214	1820-2786	4	1	IC-74F533 PC	28480	1820-2786
U215	1810-0235	3	1	RESISTIVE NETWORK DIP	01121	316A222
U220	1820-1414	3	1	IC GATE TTL LS NAND TPL 3-INP	01295	SN74LS12N
U302	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U303	1820-1015	0	2	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U304	5180-0156	4	65	IC-RAM, 64K 75 NS	28480	5180-0156
U305	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U306	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U307	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U308	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U309	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U310	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U311	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U312	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U313	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U314	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U315	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U316	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U317	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U318	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U319	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U401	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U402	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U403	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U404	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U405	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U406	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U407	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U408	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U409	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U410	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U411	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U412	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U413	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U414	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U415	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U416	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U417	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U418	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U419	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U501	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U502	1820-0691	6	1	IC GATE TTL S AND-OR-INV	01295	SN74S64N
U503	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U504	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U505	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U506	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U507	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U508	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U509	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U510	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U511	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U512	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U513	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U514	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U515	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U516	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U517	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U518	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156

Table 6-1. 12103A/B/C Replaceable Parts (continued)

12103C (12103-60003) Parts List - Sheet 3 of 3

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U519	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U520	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U601	1813-0199	4	1	IC-DELAY HY-5003	07910	HY-5003
U603	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U604	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U607	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U611	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U612	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U613	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U614	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U615	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U616	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U617	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U618	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U620	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
W5	0811-3587	5	3	RESISTOR-FXD 0 OHM	28480	0811-3587
W6	0811-3587	5		RESISTOR-FXD 0 OHM	28480	0811-3587
W7	0811-3587	5		RESISTOR-FXD 0 OHM	28480	0811-3587

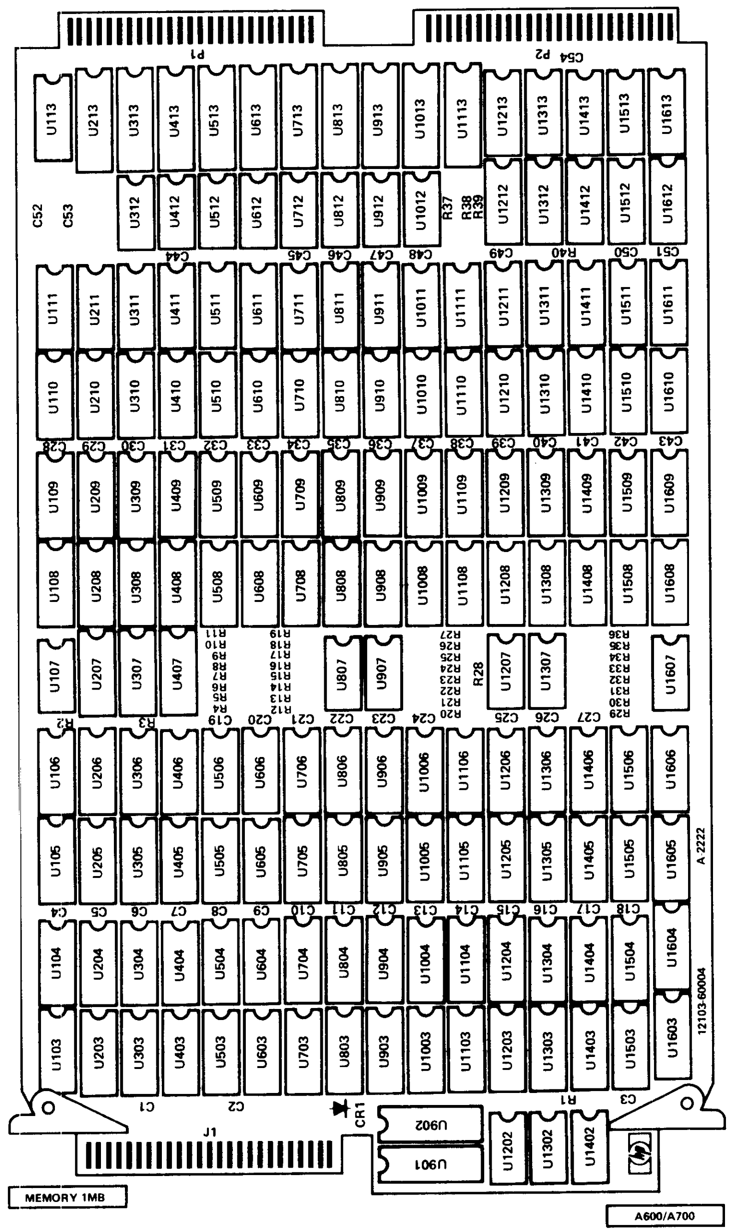


Figure 6-5. 12103D Parts Locations

Table 6-2. 12103D Replaceable Parts (sheet 1 of 4)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12103-60004	5	1	PCA-1 MEGABYTE ARRAY	28480	12103-60004
C1	0180-0229	7	5	CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C2	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C3	0160-5148	7	48	CAPACITOR	28480	0160-5148
C4	0160-5148	7		CAPACITOR	28480	0160-5148
C5	0160-5148	7		CAPACITOR	28480	0160-5148
C6	0160-5148	7		CAPACITOR	28480	0160-5148
C7	0160-5148	7		CAPACITOR	28480	0160-5148
C8	0160-5148	7		CAPACITOR	28480	0160-5148
C9	0160-5148	7		CAPACITOR	28480	0160-5148
C10	0160-5148	7		CAPACITOR	28480	0160-5148
C11	0160-5148	7		CAPACITOR	28480	0160-5148
C12	0160-5148	7		CAPACITOR	28480	0160-5148
C13	0160-5148	7		CAPACITOR	28480	0160-5148
C14	0160-5148	7		CAPACITOR	28480	0160-5148
C15	0160-5148	7		CAPACITOR	28480	0160-5148
C16	0160-5148	7		CAPACITOR	28480	0160-5148
C17	0160-5148	7		CAPACITOR	28480	0160-5148
C18	0160-5148	7		CAPACITOR	28480	0160-5148
C19	0160-5148	7		CAPACITOR	28480	0160-5148
C20	0160-5148	7		CAPACITOR	28480	0160-5148
C21	0160-5148	7		CAPACITOR	28480	0160-5148
C22	0160-5148	7		CAPACITOR	28480	0160-5148
C23	0160-5148	7		CAPACITOR	28480	0160-5148
C24	0160-5148	7		CAPACITOR	28480	0160-5148
C25	0160-5148	7		CAPACITOR	28480	0160-5148
C26	0160-5148	7		CAPACITOR	28480	0160-5148
C27	0160-5148	7		CAPACITOR	28480	0160-5148
C28	0160-5148	7		CAPACITOR	28480	0160-5148
C29	0160-5148	7		CAPACITOR	28480	0160-5148
C30	0160-5148	7		CAPACITOR	28480	0160-5148
C31	0160-5148	7		CAPACITOR	28480	0160-5148
C32	0160-5148	7		CAPACITOR	28480	0160-5148
C33	0160-5148	7		CAPACITOR	28480	0160-5148
C34	0160-5148	7		CAPACITOR	28480	0160-5148
C35	0160-5148	7		CAPACITOR	28480	0160-5148
C36	0160-5148	7		CAPACITOR	28480	0160-5148
C37	0160-5148	7		CAPACITOR	28480	0160-5148
C38	0160-5148	7		CAPACITOR	28480	0160-5148
C39	0160-5148	7		CAPACITOR	28480	0160-5148
C40	0160-5148	7		CAPACITOR	28480	0160-5148
C41	0160-5148	7		CAPACITOR	28480	0160-5148
C42	0160-5148	7		CAPACITOR	28480	0160-5148
C43	0160-5148	7		CAPACITOR	28480	0160-5148
C44	0160-5148	7		CAPACITOR	28480	0160-5148
C45	0160-5148	7		CAPACITOR	28480	0160-5148
C46	0160-5148	7		CAPACITOR	28480	0160-5148
C47	0160-5148	7		CAPACITOR	28480	0160-5148
C48	0160-5148	7		CAPACITOR	28480	0160-5148
C49	0160-4818	6	1	CAPACITOR-FXD 47 PF 10%	28480	0160-4818
C50	0160-5148	7		CAPACITOR	28480	0160-5148
C51	0160-5148	7		CAPACITOR	28480	0160-5148
C52	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C53	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
C54	0180-0229	7		CAPACITOR-FXD 33UF+-10% 10VDC TA	56289	150D336X9010B2
CR1	1990-0485	5	1	LED-LAMP LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
R1	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R2	0698-0084	9	4	RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R3	0757-0294	9	17	RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R4	0698-3432	7	16	RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R5	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R6	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R7	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R8	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R9	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R10	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R11	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R12	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R13	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R14	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R15	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F

Table 6-2. 12103D Replaceable Parts (sheet 2 of 4)

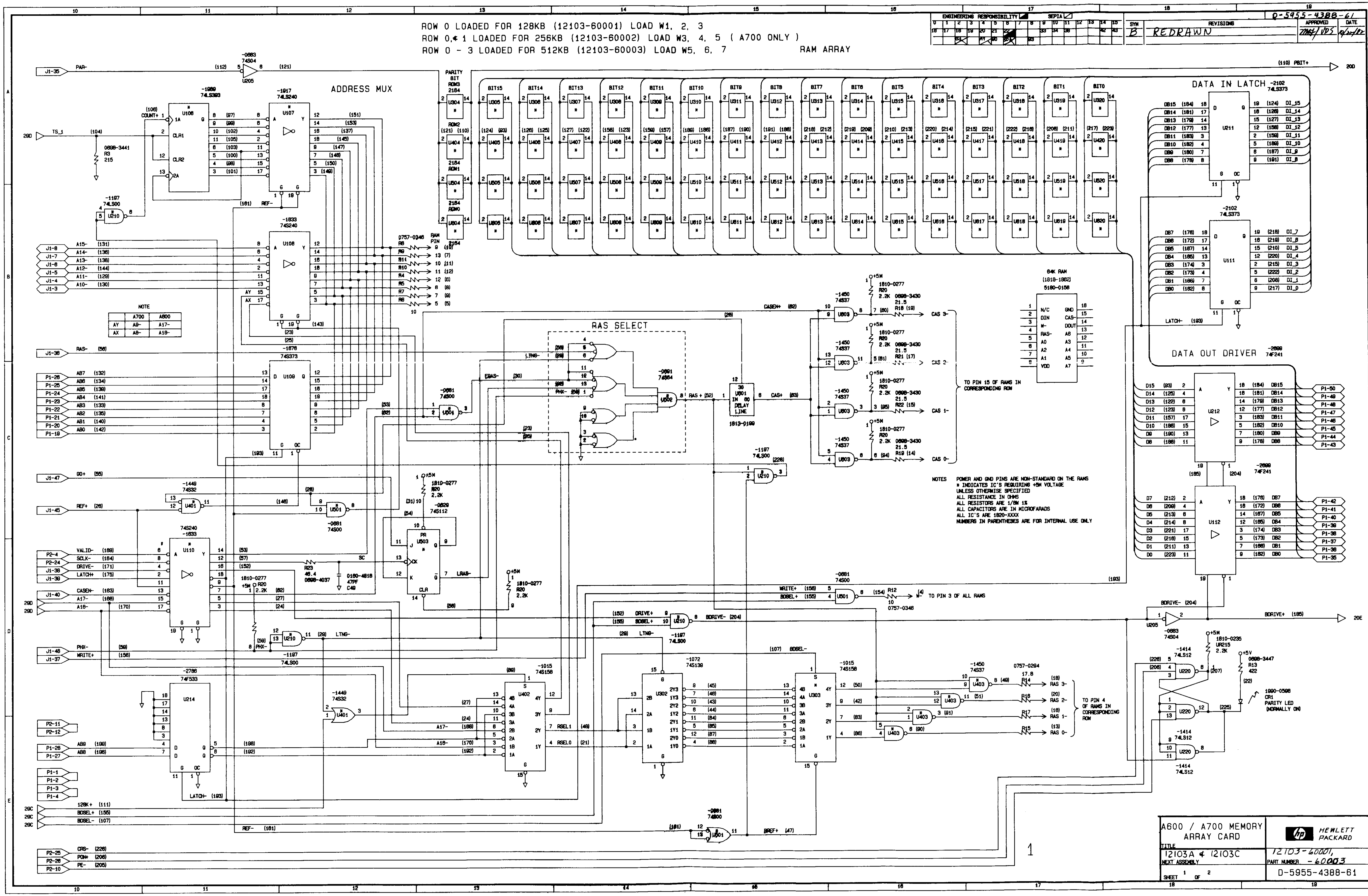
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R16	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R17	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R18	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R19	0698-3432	7		RESISTOR 26.1 1% .125W F TC=0+-100	03888	PME55-1/8-T0-26R1-F
R20	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R21	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R22	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R23	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R24	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R25	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R26	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R27	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R28	1810-0277	3	1	RESISTIVE NETWORK- 9 X 2.2K OHM	01121	210A222
R29	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R30	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R31	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R32	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R33	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R34	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R35	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R36	0757-0294	9		RESISTOR 17.8 1% .125W F TC=0+-100	19701	MF4C1/8-T0-17R8-F
R37	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R38	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
R39	0698-4037	0	1	RESISTOR 46.4 1% .125W F TC=0+-100	24546	C4-1/8-T0-46R4-F
R40	0698-0084	9		RESISTOR 2.15K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2151-F
U103	5180-0156	4	136	IC-RAM, 64K 75NS	28480	5180-0156
U104	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U105	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U106	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U107	1820-0690	5	1	IC BFR TTL S NAND DUAL 4-INP	01295	SN74S40N
U108	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U109	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U110	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U111	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U113	1820-1441	6	1	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U203	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U205	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U206	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U207	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U208	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U209	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U210	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U211	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U213	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U303	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U305	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U306	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U307	1820-1015	0	3	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U308	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U309	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U310	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U311	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U312	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U313	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U403	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U405	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U406	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U407	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U408	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U409	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U410	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U411	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U412	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U413	1820-1676	9	2	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U503	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U505	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U506	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U508	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U509	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U510	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U511	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156

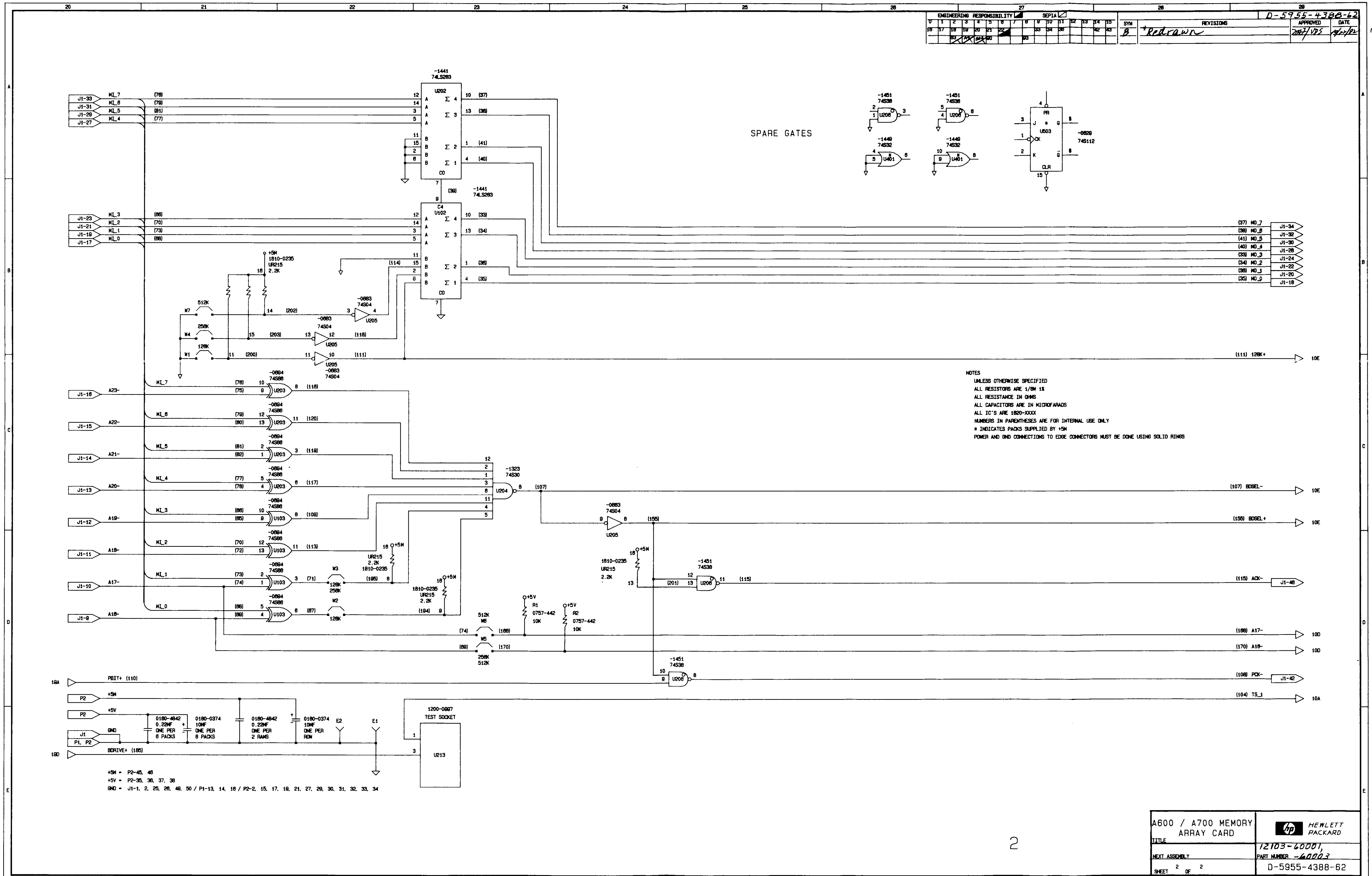
Table 6-2. 12103D Replaceable Parts (sheet 3 of 4)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U512	1820-1449	4	1	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U513	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U603	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U611	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U612	1820-1451	8	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U613	1820-2699	8	2	IC-74F241 PC	07263	74F241PC
U703	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U704	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U705	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U706	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U708	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U709	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U710	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U711	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U712	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U713	1820-2699	8		IC-74F241 PC	07263	74F241PC
U803	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U804	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U805	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U806	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U807	1820-1450	7	4	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U808	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U809	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U810	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U811	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U812	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U813	1820-2102	8	2	IC LCH TTL LS D TYPE OCTL	01295	SN74LS373N
U901	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U902	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U903	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U904	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U905	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U906	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U907	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U908	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U909	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U910	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U911	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U912	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U913	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U1003	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1004	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1005	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1006	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1008	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1009	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1010	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1011	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1012	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U1013	1820-2786	4	1	IC-74F533 PC	28480	1820-2786
U1103	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1104	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1105	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1106	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1108	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1109	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1110	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1111	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1113	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U1202	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U1203	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1204	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1205	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1206	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1207	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U1208	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1209	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1210	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1211	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156

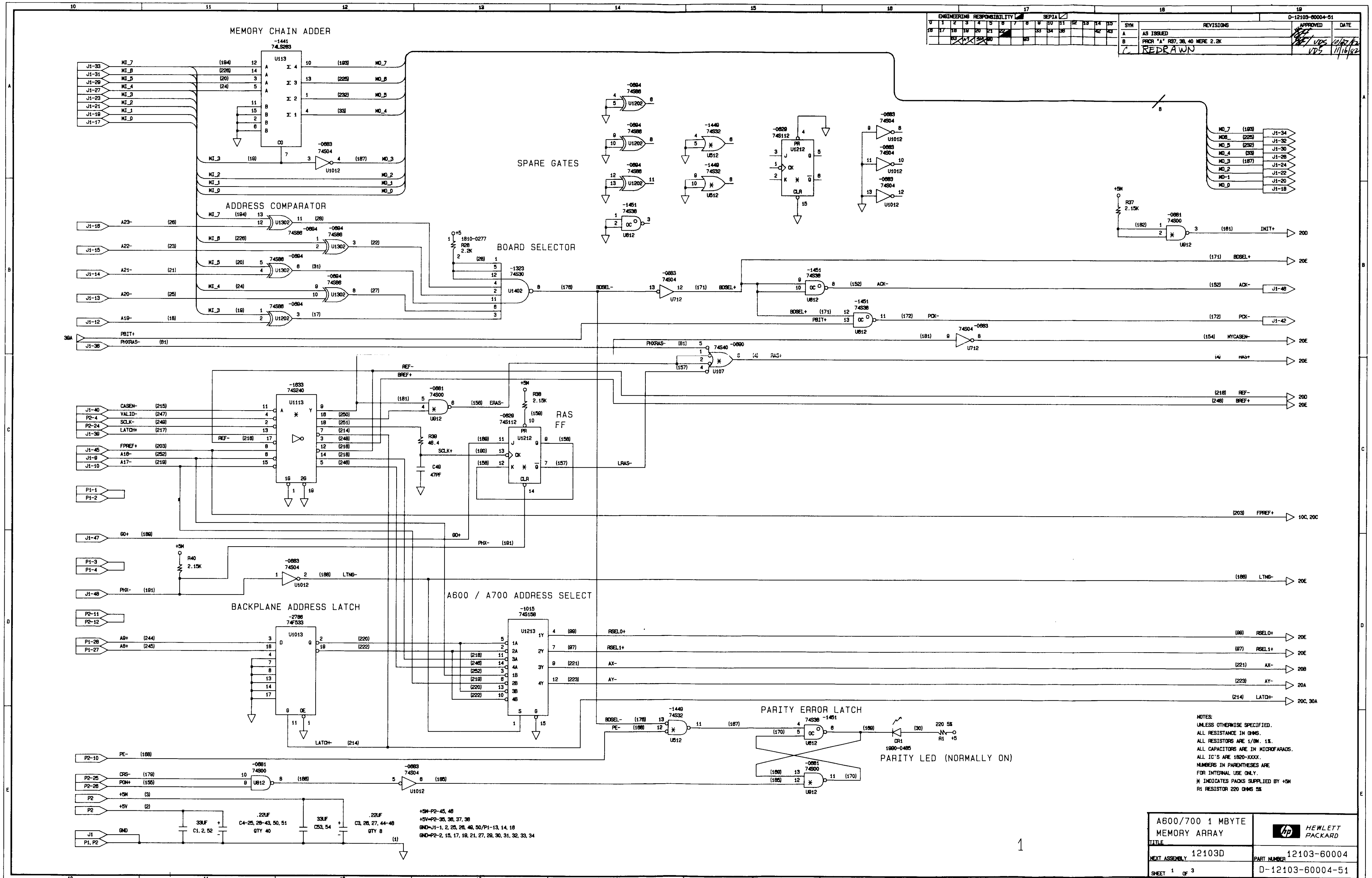
Table 6-2. 12103D Replaceable Parts (sheet 4 of 4)

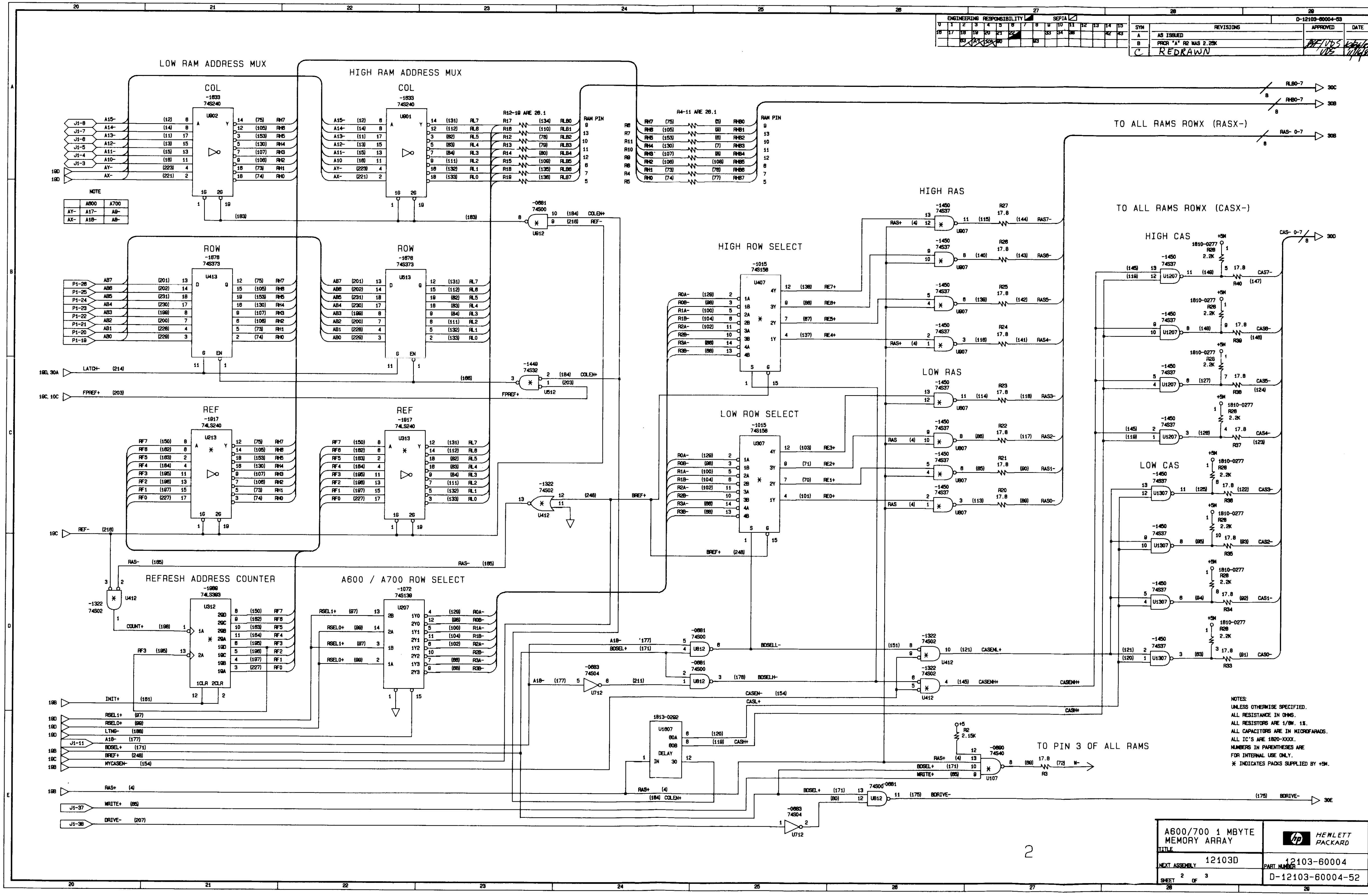
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U1212	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U1213	1820-1015	0		IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U1302	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U1303	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1304	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1305	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1306	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1307	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U1308	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1309	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1310	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1311	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1312	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1313	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1402	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U1403	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1404	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1405	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1406	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1408	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1409	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1410	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1411	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1412	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1413	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1503	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1504	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1505	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1506	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1508	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1509	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1510	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1511	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1512	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1513	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1603	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1604	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1605	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1606	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1607	1813-0292	8	1	IC-DELAY LINE	28480	1813-0292
U1608	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1609	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1610	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1611	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1612	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156
U1613	5180-0156	4		IC-RAM, 64K 75NS	28480	5180-0156


ROW 0 LOADED FOR 128KB (12103-60001) LOAD W1, 2, 3
ROW 0,& 1 LOADED FOR 256KB (12103-60002) LOAD W3, 4, 5 (A700 ONLY)
ROW 0 - 3 LOADED FOR 512KB (12103-60003) LOAD W5, 6, 7
RAM ARRAY
ADDRESS MUX
DATA IN LATCH
RAS SELECT
DATA OUT DRIVER
64K RAM (1818-1862) 5180-0156
TO PIN 15 OF RAMS IN CORRESPONDING ROW
TO PIN 3 OF ALL RAMS
TO PIN 4 OF RAMS IN CORRESPONDING ROW
NOTES
POWER AND GND PINS ARE NON-STANDARD ON THE RAMS
* INDICATES IC'S REQUIRING +5M VOLTAGE
UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
PARITY LED (NORMALLY ON)
REVISIONS
B REDRAWN
D-5955-4388-61
A600 / A700 MEMORY ARRAY CARD
HEWLETT PACKARD
12103A & 12103C
NEXT ASSEMBLY
12103-60001, -60003
PART NUMBER
SHEET 1 OF 2
D-5955-4388-61


D-5955-4388-62
REVISIONS
B Redrawn
SPARE GATES
NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5M
POWER AND GND CONNECTIONS TO EDGE CONNECTORS MUST BE DONE USING SOLID RINGS
+5M = P2-45, 46
+5V = P2-35, 36, 37, 38
GND = J1-1, 2, 25, 26, 49, 50 / P1-13, 14, 16 / P2-2, 15, 17, 19, 21, 27, 29, 30, 31, 32, 33, 34
1200-0607 TEST SOCKET
A600 / A700 MEMORY ARRAY CARD
TITLE
NEXT ASSEMBLY
SHEET 2 OF 2
HEWLETT PACKARD
12103-60001,
PART NUMBER -60003
D-5955-4388-62

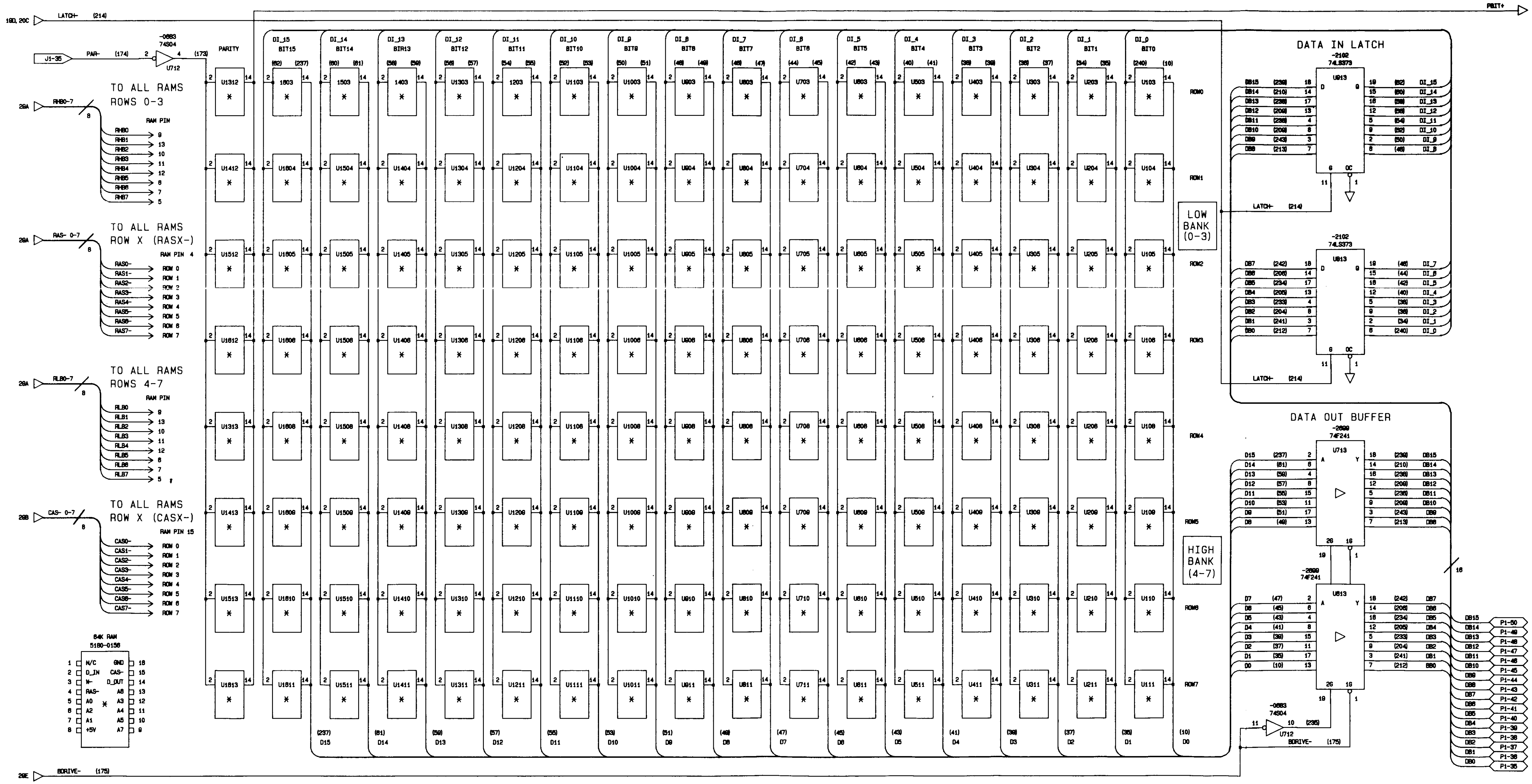
2


MEMORY CHAIN ADDER
SPARE GATES
ADDRESS COMPARATOR
BOARD SELECTOR
RAS FF
A600 / A700 ADDRESS SELECT
BACKPLANE ADDRESS LATCH
PARITY ERROR LATCH
PARITY LED (NORMALLY ON)
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
APPROVED
DATE
A AS ISSUED
B PRIOR "A" R37, 38, 40 WERE 2.2K
C REDRAWN
D-12103-60004-51
NOTES:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
✻ INDICATES PACKS SUPPLIED BY +5M
R1 RESISTOR 220 OHMS 5%
+5M=P2-45, 46
+5V=P2-35, 36, 37, 38
GND=J1-1, 2, 25, 26, 49, 50/P1-13, 14, 16
GND=P2-2, 15, 17, 19, 21, 27, 29, 30, 31, 32, 33, 34
A600/700 1 MBYTE
MEMORY ARRAY
TITLE
NEXT ASSEMBLY 12103D
PART NUMBER 12103-60004
SHEET 1 OF 3
D-12103-60004-51
HEWLETT PACKARD
1



LOW RAM ADDRESS MUX
HIGH RAM ADDRESS MUX
COL
ROW
REF
TO ALL RAMS ROWX (RASX-)
TO ALL RAMS ROWX (CASX-)
HIGH RAS
LOW RAS
HIGH CAS
LOW CAS
HIGH ROW SELECT
LOW ROW SELECT
REFRESH ADDRESS COUNTER
A600 / A700 ROW SELECT
TO PIN 3 OF ALL RAMS
REDRAWN
NOTES:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
✱ INDICATES PACKS SUPPLIED BY +5M.
A600/700 1 MBYTE
MEMORY ARRAY
HEWLETT PACKARD
12103D
12103-60004
D-12103-60004-52
SHEET 2 OF 3
2

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	PRCR "A" R2 WAS 2.25K	VDS	
C	REDRAWN	VDS	11/16/82



NOTES:
UNLESS OTHERWISE SPECIFIED,
RAM POWER AND GND PINS ARE NON-STANDARD
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.
* INDICATES PACKS SUPPLIED BY +5M

3

A600/A700 1 MBYTE MEMORY ARRAY
TITLE
NEXT ASSEMBLY 12103D
SHEET 3 OF 3
HEWLETT PACKARD
PART NUMBER 12103-60004
D-12103-60004-53

7.1 INTRODUCTION

This section covers the 12104A Error Correction Array (ECA) memory card. The ECA card contains 512 kilobytes of RAM memory that will correct single-bit errors and give a parity-error interrupt on double-bit errors. It does not have parity-error checking as described for the standard memory cards in Section VI.

7.2 PHYSICAL CHARACTERISTICS

The ECA card is installed in the A700 backplane in the same locations as allowed for the standard 512 kilobyte memory array card. It includes the same self-configuration feature as used in the standard array cards; i.e., no jumper or switch settings are necessary for configuring the card into the system. The memory cards are installed in the backplane above the controller card as shown in Figure 1-2 in Section I.

The power supply specifications for the card are covered in Section I. When the card is not being accessed (operating state) its power consumption is that given for the standby state.

All signals and data are Schottky-TTL levels and comply with Schottky TTL design rules. The HP 12104A ECA card is shown in Figure 7-1.

7.3 OPERATION OF ECA CARD

7.3.1 MODULE CONFIGURATION CIRCUIT

The Error Correcting Array Card in the A700 memory system is used in the main memory system where the actual data is stored. This card can be used exclusively or in conjunction with the parity-check memory array cards described Section VI of this manual. The circuit areas included in this description of operation are shown in the block diagram of Figure 7-2.

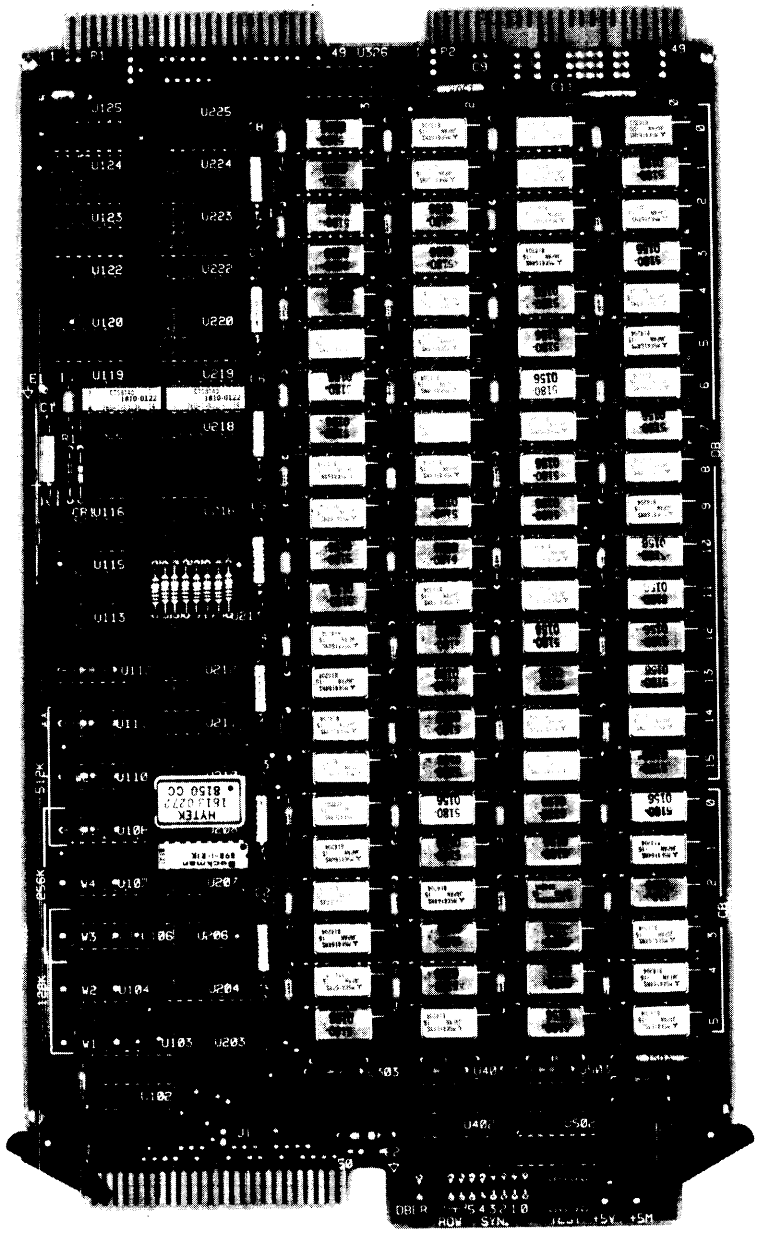


Figure 7-1. HP 12104A Error Correcting Array

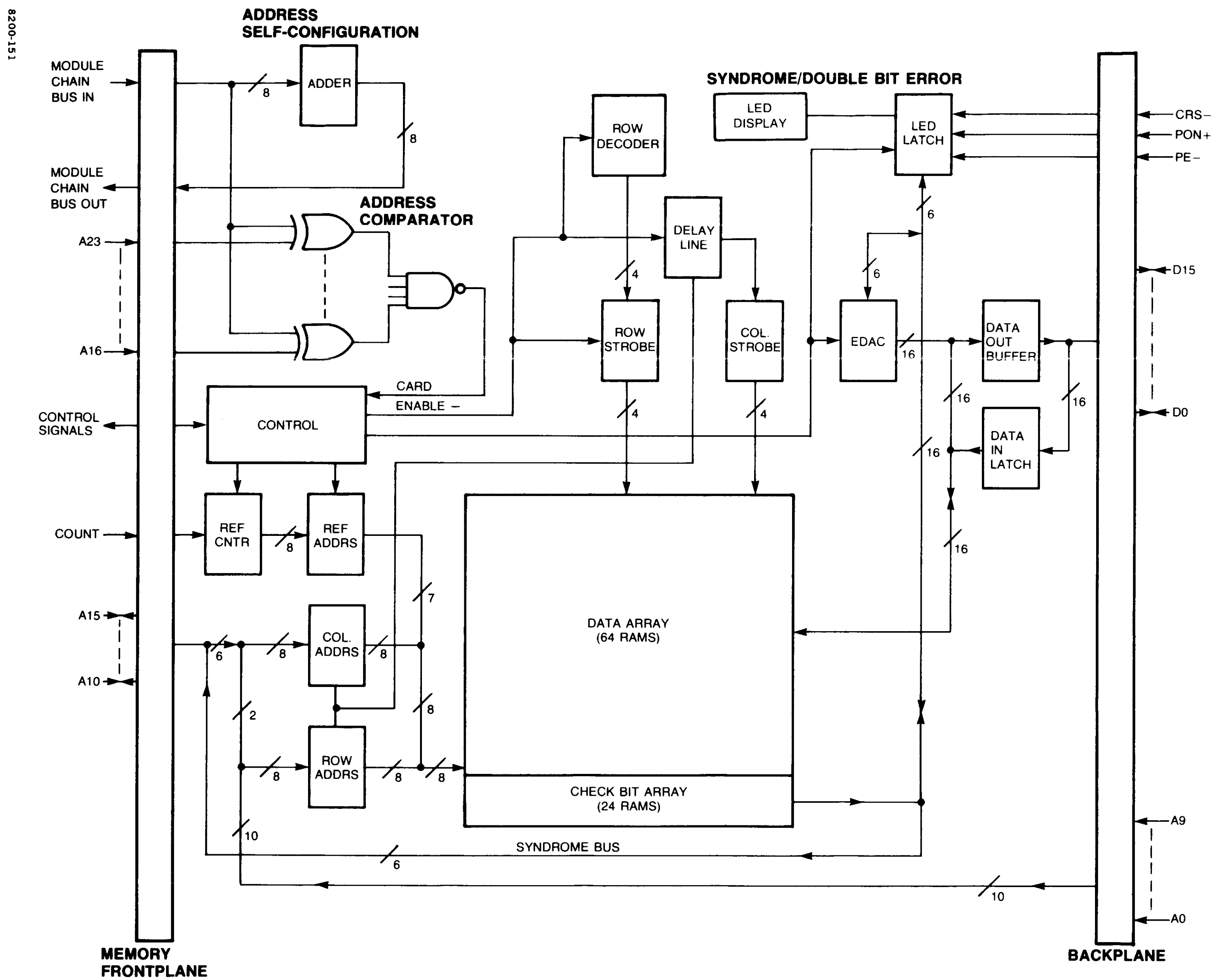


Figure 7-2. ECA Card Block Diagram

Each ECA card, when installed, occupies a unique address space so that the controller may access it by address only. To accomplish this, each memory card has an adder that takes a totalled address from the previous card, adds the number of bytes of RAM on the card, and passes this incremented address over the frontplane to the next higher memory card on the backplane. These incremented addresses are essentially the starting address for each array card and, when compared to the physical address (on the frontplane), form a basis for selecting the cards. The main memory address into the first card above the controller is 0000 (octal).

Since each array card sends an incremented number equal to the number of bytes on the card to the next array card on the backplane, the array cards automatically configure themselves in an ascending address order. Thus, if two cards are interchanged, they automatically reconfigure themselves to form the ascending address sequence. The advantage of this scheme is that identical memory modules become unique in the address space of the computer without the aid of manually selected switch or jumper settings unique to the location or dedicated backplane locations.

7.3.2 ARRAY CARD SELECT

Each memory array card receives the physical address sent by the memory controller over the frontplane. Using eight XOR-gates, the cards compare the physical address with the incremented address (see previous paragraph). When a match is encountered on a card, the outputs of all its XOR-gates go high causing its card select line to go true (This can happen on only one array card at a time). When a card select line is true that card is enabled for access to the RAM array.

7.3.3 RAM ARRAY

The RAM array consists of 88 dynamic MOS memory elements. Each element is housed in a 16-pin DIP package. The RAMs are arranged in four rows of 22 bits each to provide 16 data bits plus six check bits. Each 16-bit word of data written into memory is stored in one row of the array to which is added the six check bits. Thus, during any access only one row of RAMs is activated. (This is not true of refresh cycles which access all rows of all array cards simultaneously.) When an array card is not selected, all RAMs on that card are in standby mode.

7.3.4 ROW MULTIPLEXER

Row multiplexing is used to select each row of the RAM array for access. Bits 16 and 17 of the physical address on the frontplane are routed to the multiplexer which performs a four-out-of-two decoding function. The outputs of the decoder are then fed through the card select multiplexer to the row address strobe (RAS) buffer of the appropriate row. The RAS signal to the RAMs performs the chip select function.

7.3.5 CLOCK GENERATION

A delay line is used to generate the RAS and CAS signals in the same manner as for a standard array card. However, the error correction process requires additional clocks that must have tight timing tolerances. Therefore, the delay line on the ECA card has two additional taps used for controlling the error correction process.

7.3.6 ADDRESS MULTIPLEXER

Equally as critical as the timing of the RAS and CAS pulses is the timing of the multiplexer switching of the ROW and COLUMN addresses. To insure the correct timing between clocks and address switching, the same delay line is used to switch the multiplexer from ROW address to COLUMN address. This signal occurs from an intermediate tap on the delay line.

A third group of address bits is the refresh address needed for the memory refresh operation. Only seven bits of address are needed by the RAMs since refreshing is done by rows in the RAM elements. This address is switched to the RAMs during every refresh cycle. Control of the refresh multiplexer is handled from the memory controller by the RC- signal over the frontplane.

7.3.7 DATA LATCH

During a write cycle, data is latched on each array card at the beginning of the memory cycle. The latch signal is generated on the memory controller and is routed to all array cards over the frontplane. It should be noted that the latching function occurs on all array cards even though the data is only being written to one particular card. The latch signal occurs at different times depending on whether the memory write is occurring from the processor or a peripheral device using DMA.

In the case of a DMA write, the data is latched while it is valid on the backplane during MEMGO. In the case of a processor write, the data is latched on the leading edge of OUTEN. It should be noted that the processor holds data valid on the backplane for the long half cycle of the system clock following MEMGO.

7.3.8 ERROR LOGGING

Error information from the error correction process is stored on the memory controller in the boot RAM area. Six bits of syndrome code are sent from the ECA card to the controller via the memory frontplane whenever an error occurs.

The location of the syndrome code storage in the controller boot RAM area corresponds to the row of memory on the ECA card containing the error where each row of memory on the card contains 64k words of data.

Since the maximum memory capacity possible in the system is 16M words (32M bytes) and with 64k words per row, there can be a maximum of 256 rows (16M-words/64k-words = 256). Thus, there are 256 locations in boot RAM reserved for error logging which allows all cards in the memory array to be ECA cards.

NOTE

A physical memory capacity of four array cards limits the number of rows actually used to 16.

The error logging space corresponds to the upper 256 addresses in the 1k address space of the boot RAM. (Starting address = 1400 octal.) Each of these locations in boot RAM will contain the last error to occur in the corresponding row of main memory. Thus, the boot RAM must be periodically read and initialized to obtain time log information.

The syndrome code stored in the boot RAM locations identifies which bit of data is in error, including the check bits themselves. It should be clear that a syndrome code in a given location of boot RAM identifies a specific RAM on an array card as defective. (There is only one RAM element at a given bit location in a given row.) Thus, with error logging it is possible to isolate memory errors down to the chip level. Table 7-1 associates the syndrome codes for single-bit errors with the bit that is in error.

7.3.9 ERROR SYNDROME AND DOUBLE-BIT ERROR LATCH

The ECA card has an eight-bit LED display used to identify the faulty bit when an error correction operation is executed. The display is located at the front of the card for easy viewing while installed in the system. Under normal operation, the syndrome display (red LEDS) are off and the double-bit error LED (green) is on. When a single bit error occurs, the ECA card corrects the data error and lights the display in the following format:

```
                        543210 --- check bit
                   o  oo oooooo
                  /   '--'------'
double bit           /    /
error LED          row  syndrome (on = 1)
 (green)             (red)
```

Each group is read in binary fashion, that is, the possible row designations are 00, 01, 10, 11 corresponding to errors in rows 0, 1, 2 and 3, respectively. Similarly, the syndrome bits are decoded into two octal digits with the MSB located to the left. Using this display, service personnel and the customer can identify which row had the error and which bit in that row was in error. Only the last error to occur on the card is represented in the LED display.

To read the display, refer to the table on the following page. Note in the table that all single-bit data errors result in three LEDs on and three off. For a single check-bit error, one LED is off which is the LED corresponding to that check bit.

Double-bit errors cannot be corrected by the ECA card, so that when they do occur, the memory system asserts a parity-error interrupt. In this case, the green LED on the ECA card is extinguished to signify that a double-bit error has occurred on that card. The syndrome display will have some LEDs lit, but most likely it will not represent a valid syndrome code.

The display is initialized when the system is powered on or when a control reset is issued.

7.4 ECA CARD TESTING

7.4.1 DATA BIT ERRORS

To test the error correcting function of the ECA card, it is necessary to be able to force single- and double-bit errors programmatically. This can be done by controlling the PS- line on the backplane. This line is high (normal operation), the CWEN+ signal (check write enable) is high at U115-10 enabling the write line to the check RAMs. In this mode, every time that data is stored on the ECA card, the appropriate check word is also stored.

If the PS- line is low during a write access, the check word cannot be written to the check RAMs. Thus, data in the main memory array can be altered without affecting check bit information.

Therefore, to force a single data-bit error, the program must write data into memory in the normal fashion (PS- high), storing the data with the proper check word. Then, the PS- line can be set low and the data written again but this time with one bit different than the first time. In this way, the check word will still be the original version while the data will have one bit changed. The memory location now contains a single-bit error relative to the original check word, and any access of that location will cause single-bit error correction to take place.

Double data-bit errors can be established in exactly the same manner, except that two bits must be different on the second write.

7.4.2 CHECK BIT ERRORS

It is not quite as easy to establish single-bit check-bit errors. There is no way to write directly into the check bit RAMs as there is for writing into the data RAMs. However, a method does exist for forcing single bit errors in the check RAMs.

Table 7-1. Syndrome Codes versus Error Bits

LEDS	ERROR SYNDROME (OCTAL)	BIT IN ERROR	
110 100	64	DB 0	data bits
110 010	62	DB 1	
110 001	61	DB 2	
101 100	54	DB 3	
101 010	52	DB 4	
101 001	51	DB 5	
100 101	45	DB 6	
100 011	43	DB 7	
011 100	34	DB 8	
011 010	32	DB 9	
010 110	26	DB 10	
010 101	25	DB 11	
010 011	23	DB 12	
001 110	16	DB 13	
001 101	15	DB 14	
001 011	13	DB 15	
111 110	76	CB 0	check bits
111 101	75	CB 1	
111 011	73	CB 2	
110 111	67	CB 3	
101 111	57	CB 4	
011 111	37	CB 5	
000 000	00	NO ERROR	

Table 7-2 contains data patterns versus check bit patterns and the procedure to force error correction cycles. Next to each pattern in the table is the corresponding check bit pattern which is normally stored along with the data during a write cycle. By using the feature of disabling the writing into the check RAMs (refer to paragraph 7.4.1), single-bit check-bit errors can be established on the ECA card. By using the data patterns in the table, any check bit can be forced to be in error.

Table 7-2. Forcing Check-Bit Errors

CHECK WORD BITS CB 5 0	DATA WORD (OCTAL)
000000	000505
000001	000412
000010	000414
000100	000417
001000	000502
010000	000513
100000	000103
111111	000006
111110	000111
111101	000117
111011	000114
110111	000001
101111	000010
011111	000400

EXAMPLE PROCEDURE:

NOTE: Data patterns are in octal notation.

1. Write data pattern 505 into memory: Establishes a check word that equals 000000.

2. Change parity sense. (STF 5): Inhibits writing into the check word.

3. Write data pattern 412 into the same memory location: Check word 000000 remains but the correct check word is really 000001.

4. Change parity sense back (CLF 5): Leaves a single bit check bit error in memory.

5. Access the memory location: Causes an error correction cycle to be executed.

7.5 THEORY OF OPERATION

When reading this theory of operation, refer to the block diagram of the ECA card given previously in Figure 7-2 and to the schematic for this card at the rear of this section of the manual.

The integrated circuit packages (chips) are referenced by their U-number designation and schematic location. For example, U69 (13-C) means chip 69 on schematic sheet no. 1 is located by coordinates 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11 etc, and on sheet no. 2 it is numbered 20, 21, etc.

7.5.1 MODULE ADDRESSING CIRCUIT

The module addressing circuit is used to automatically configure the array cards into the address space of the A700 Computer. This is accomplished by using eight chained lines on the memory frontplane to allow the passing of unique addresses to each array card. Each array card uses the address sent to it as the starting address of its address space. The array card sends an incremented address to the array card above it which is used as the starting address of that next array card. In this manner, each array card is located on a unique address boundary in the memory address space. Also, each array card is in sequence with the others; the beginning of memory is located on the array card next to the controller and the end of memory is on the array card farthest from the controller.

The number added to the starting address equals the memory capacity of the card which is determined by the number of RAMs loaded on it. The ECA card has four rows of 22 RAMs where six RAMs are used for check-bit information and 16 RAMs are for actual data storage. Since 64k RAMs are used, the capacity of each row is 64k words or 128k bytes of memory, and the four rows provide 512k bytes of memory.

The module addressing circuit is implemented by using two four-bit full adders U203 (13-A) and U207 (13-B). These adders are connected in cascade to perform full eight-bit addition. The variation in the number to be added to the starting address for the different array cards is determined by jumpers W1, W2, and W7. Jumper W7 is installed on the ECA card to add four to the input address to correspond with its 512k bytes capacity.

In operation, the eight bits of chained address are compared in quadruple two-input exclusive OR (XOR)-gates U103 (12-B) and U102 (12-B) to the upper eight bits, A16 through A23, of physical address present on the memory frontplane. These eight bits determine which card is to be selected when a given address is present. (The lower order 16 bits, A0 through A15, are used to address locations in the RAM chips themselves.)

The card select signal is generated by eight-input NAND-gate U106 (13-B) that receives the outputs of the XOR-gates. The outputs of all the XOR-gates must be high for the card to be selected.

NOTE

> The physical address is low true while the chained address is high true so that the comparison of these two signals is equal when one is low and the other is high. The output of the XOR-gates under the equal condition is, therefore, high.

The outputs of the XOR-gates for the lower two bits for address lines A17 and A16 are disabled by leaving out jumpers W2 and W3 and their inputs to U106 are pulled high by resistors (U104 resistor network) which permanently sets these lines in the selected condition. Thus, the card select circuit of U106 ignores these bits so that the card remains selected while A16 and A17 select the proper row of RAMs using U206 for the address decoding.

The row address bus with A16 and A17 go to buffers U204-4 and U204-8 (21-D) then to decoder U108 (21-D) where the row decoding occurs (refer to Row Selection below).

Following is a detailed explanation of how the card select circuit operates for the ECA card:

All ECA cards must be located on an address boundary where the starting address for the card can be evenly divided by 512k bytes. For details on this subject refer to Section VI, paragraph 6.4.1 on the module address circuit.

The reason for the restriction is that it assumes that row selection on a 512k byte card occurs with address bits 16 and 17 going thru the sequence of 00, 01, 10, 11 with no change on address bit 18. If address bit 18 did change, then the card could not remain selected. The only time that the above condition is met occurs when the card is located on a 512k byte boundary in the address space.

7.5.2 RAS GENERATION

The RAS pulse is used to initiate every access and to perform refreshes to the RAM array. The RAS pulse from the memory controller is received at U111-5 (23-C) and is sent to quadruple two-input RAS drivers U403 (24-C) and U503 (24-D). The proper row of RAMs to be accessed has already been determined at this time, and the appropriate-gate at U403 and U503 is enabled by U206 (23-D). RAS then passes through to the selected row.

7.5.3 ROW SELECTION

The proper row of memory to be accessed is determined by physical address bits 16 and 17 (A16 and A17). These bits are routed to U108-13 and -14 (22-D). U108 performs a four-out-of-two decoding function to determine the proper row to access. The selected row signal is then set up at the multiplexer input at U206. The card select signal switches this multiplexer to the A-input, allowing the row select signal to enable the proper gate at U403 and U503. When the card select is false, the multiplexer's B-inputs are selected which disables all RAS driver gates.

During refresh cycles, all rows are selected. The RAS pulse is sent to all rows simultaneously. The multiplexor is forced to enable all rows by asserting the signal at U206-15 high. This signal occurs every refresh cycle. The BCASEN+ signal is gated with the REF- signal to produce the enable signal. This is to prevent both RAS and CAS from being asserted at the RAMs when a suspended refresh cycle initiates after a memory cycle.

7.5.4 CAS GENERATION

The CAS pulse to the RAMs is generated from the RAS pulse through the use of a delay line located at U210 (23-C). The CAS pulse strobes the second set of addresses into the RAMs during a memory access. A delay line is used to ensure a tight tolerance between the RAS and CAS signals. The delay provides the minimum time for the RAM address bus to switch from the row address to the column address.

The CAS pulse is sent to CAS drivers U403 and U503. The CAS signal appears at the RAMs only if the CASEN- signal is low. This is true since a high CASEN- signal holds flip-flop U124 (23-C) in the reset state which, in turn, holds the BCASEN+ signal to the CAS drivers low.

In the case of a read access, the CASEN- signal will be asserted before the delay line CAS is asserted, so that the RAS-CAS sequence occurs as quickly as possible. In the event of a write cycle, the CASEN- signal occurs after the delay line CAS occurs so that the write is delayed to allow for the generation of the check bits. These check bits are stored in the check bit RAMs at the same time as the data is stored in the main memory RAMs.

Also, since the CAS from the delay line occurs every time the RAS pulse occurs, the CASEN- signal is used to inhibit unwanted CAS cycles during refreshes and memory protect violations. For additional details, refer to Section V, paragraph 5.6.6.7 concerning CAS generation.

Since the CAS pulse is used to hold accessed data valid at the output of the memory RAMs during a read cycle, it is necessary that CAS at the RAMs remain asserted until the memory cycle completes. However, CAS would be removed 65 nanoseconds after RAS terminated, (delay line time) if CAS were not somehow latched. The solution used is to extend the assertion of RAS beyond that of the controller RAS signal. This is accomplished by gating the CASEN+ and VALID+ signals at U111-1 and -2 (22-C), and presenting a latched RAS signal to U111-4. Thus, RAS to the RAMs is extended to the end of the VALID signal and the delay line CAS is correspondingly extended. This provides sufficient extra time for the delay line CAS to hold data valid until the end of the memory cycle.

7.5.5 ADDRESS MULTIPLEXER

The addresses used by the memory RAMs are controlled by the address multiplexer located at U212 (13-D), U213 (13-C), and U216 (13-E). This MUX presents the row and column addresses as well as the refresh addresses to the RAMs. The latch at U216 (13-E) is used to latch the lower-order eight bits of physical address directly from the backplane.

The output of this latch is used as the row address to the RAMs. After the RAS pulse occurs and the address hold time at the RAMs is satisfied, the delay line asserts the COLEN+ signal at U115-1 (12-D) . The U115 NAND-gates form an interlock which disables the row address driver and enables the output of the column driver U212 (13-D).

After the column address has had sufficient time to settle, the CAS pulse is asserted at the RAMs.

When a refresh cycle is initiated, the REF- signal appears at U115-2 and -4 (12-D). This signal disables the outputs of both the row and column address drivers U212 (13-D) and U216 (13-E) and enables the refresh address driver U213 (13-C). U213 presents the refresh address to the RAMs.

7.5.6 ADDRESS LATCH

The lower-order 10 bits of physical address are latched directly from the backplane. Bits 0-7 are latched by U216 (13-E) and are presented to the RAMs as the row address. Bits 8 and 9 are latched at U211 (16-D). These two bits are then sent to U212-8 and -11 (13-D) where they are used as the first two bits of the column address.

7.5.7 DATA LATCH

Data is latched directly from the backplane at U222 (28-A) and U224 (28-B). These latches are transparent so that as data becomes available on the backplane, it is sent to the RAMs before the LATCH signal freezes the latch. These latches hold the input data at the RAMs during every write cycle.

7.5.8 BACKPLANE DATA DRIVERS

Data is driven onto the backplane by two octal drivers located at U220 (28-C) and U223 (28-D). The outputs of these drivers are enabled by the BDRIVE signal whenever the card is selected and the memory access is a read cycle.

7.5.9 ERROR SYNDROME LATCH

The error syndrome latch is composed of two type 74LS175 latches U402 (25-E) and U502 (26-E). The latch is clocked whenever a single- or double-bit error is detected by the EDAC chip.
The BDRIVE+ signal enables the clock line at U120-9 (25-E). This insures that the latch can only be clocked when the card is enabled for a read access. When the controller requests the error syndrome during a correction cycle, the SYNRQ+ appears at U120-10. The trailing edge of the SYNRQ+ actually clocks the latch. The information stored in the latch are the error syndrome bits appearing at the output of the EDAC and the row of memory presently being accessed.

7.5.10 DOUBLE-BIT ERROR LATCH

This latch is identical in function to the parity LED latch on the standard array card. When a double-bit error occurs, the PE- signal (parity error) is asserted by the controller. The PE- signal is received at U125-13. A low at this input causes the output at U125-11 (16-C) to go high, turning off the DB ERR LED. The cross-coupling of the U125 NAND-gates latch the LED off. The latch can be reset by either a CRS- or a PON- signal.

7.5.11 REFRESH COUNTER

Refresh addresses are generated on the array card. A counter located at U113 (11-C) is used to count in a binary sequence to generate the 128 row addresses needed for refresh cycles. Note that eight bits are generated and sent to the RAMs but only seven are needed. The counter is clocked by the COUNT+ signal from the memory controller which is just a gated form of the REF signal. The counter is clocked at the end of each refresh cycle so that the refresh address is set up in plenty of time for the next refresh cycle.

7.5.12 STANDBY OPERATION

The array card maintains stored data when the +5V power supply is removed, provided that the +5M power supply is maintained and the memory controller continues to schedule refresh cycles. Since not all of the circuitry on the array card is necessary for refreshing, only that circuitry needed for refreshes is powered by +5M. All circuit chips designated by an asterisk (*) on the array card schematic receive +5M voltage. These are the only chips that are active when the array card is in standby mode during battery backup operation.

7.5.13 FRONTPLANE HANDSHAKE SIGNALS

There are two signals passed over the frontplane from the ECA card to the memory controller whenever a memory access takes place. These are the Acknowledge and Parity Disable signals. Both signals are sent to the controller by the open collector driver U110 (15-B). This driver is enabled when the card is selected.

The Acknowledge signal is sent as soon as the card is enabled to inform the controller that the address on the frontplane has accessed an existing array card.

The Parity Disable signal is sent to the controller at the time of card selection to inhibit the controller from asserting a parity error interrupt whenever the ECA card is accessed. This is necessary since a parity bit is not returned to the controller such as the bit returned during an access to a parity-check array card.

When a double-bit error occurs, the ECA card de-asserts the Parity Disable signal to the controller and, in this way, forces the controller to generated a parity error. (See Double-Bit Error Detection, paragraph 7.5.19.)

7.5.14 ECA CARD DATA PATHS

The ECA card, unlike the parity-check array card, has a common input/output data bus on the card. All data transfers on the card occur over this bus, whether the access is a read or write cycle. Connected to this bus are the following circuit elements: Backplane Receivers; Backplane Drivers; EDAC (data pins); RAM inputs; and RAM Outputs. EDAC (data pins); RAM inputs; and RAM outputs.

Data transfers on the data bus are carried out in three different modes as follows:

a. Data is written into memory from the backplane. The backplane receivers drive the data onto the bus. (The backplane drivers are disabled.) The EDAC monitors the received data and generates the check bit information to be stored in the check bit array. The received data is then written into the RAMs.

b. Data is accessed from the memory RAMs, thus, the RAMs drive the bus. The backplane receivers are disabled. The backplane drivers are enabled to drive the accessed data onto the backplane. The EDAC monitors the accessed data for correctness. (The EDAC generates a check word from the data and compares it to the check word accessed from the check bit array.) If no error is present, the backplane is driven with the accessed data and the transfer completes.

c. This mode is the same as (b) above except that an error is detected. In this case, the RAMs are disabled from driving the bus, and the EDAC drives the bus with the corrected data. It is this corrected data, from the EDAC chip, that is driven onto the backplane.

The ECA also has a check-word bus which transfers the check word bits between the following destinations: check Bit RAM inputs; check bit RAM outputs; EDAC chip (check bit pins); error syndrome latch; and syndrome code frontplane driver.

The check-word bus also has three different modes, corresponding to the modes (a, b, and c above) for the data bus. In mode (a), a check word is generated by the EDAC to be stored in the check bit RAMs. In mode (b), the check word is accessed from the check RAMs, and is monitored by the EDAC for error checking. In mode (c), the check bit RAMs are disabled, and the EDAC outputs the error syndrome. The error syndrome is to be latched in the error syndrome latch and sent to the memory controller over the frontplane as the error log information.

7.5.15 EDAC CHIP CONTROL

The error correction process is performed completely by the error detection and correction (EDAC) chip U218 (27-B). It operates in four different modes determined by the state of the control inputs S0 and S1 located at U218-25 and -26 (26-C). Table 7-3 summarizes the function of the EDAC:

Table 7-3. Functions of Error Detection and Control Chip

MEMORY CYCLE	CONTROL S1 S0	EDAC FUNCTION	DATA I/O	CHECK WORD I/O	FLAGS SEF DEF
Write	L L	Generate Check Word	Input Data	Output Check Word	L L
Read	L H	Read Data and Check Word	Input Data	Input Check Word	L L
Read	H H	Latch and Flag Errors	Latch Data	Latch Check Word	Enabled
Read	H L	Correct Data & Generate Syn- drome Bits	Output Correct Data	Output Syndrome Bits	Enabled

7.5.16 WRITE CYCLE

During a write cycle, the backplane receivers are enabled to drive the internal data bus. This is done by gating the BUSY+ signal with the W+ signal at U115-12 and -13 (28-B). As the data becomes valid on the backplane, it is immediately set up at the data RAMs. Also, the data is monitored by the EDAC for generation of the check word to be stored into the check bit RAMs. The EDAC is set into this check word generation mode by driving its control inputs at S0 and S1 to the low state. This is done by the WRITE signal asserting low the gate outputs of U123-3 (26-C) and U116-13 (26-C).

As in the case of a write cycle to the parity-check array card, the CASEN- signal from the controller is used to present CAS to the RAMs. However, since it takes extra time for generation of the check word, CASEN- must be delayed beyond that needed for the parity-check array card. This is accomplished by asserting the CASEN+ line on flip-flop U124-14 (23-C).

When the CASEN- signal is received from the controller, it releases the clear input of the flip-flop. It is not until the next FCLK cycle that the flip-flop gets set and asserts CAS at the RAMs. During this additional delay time, the EDAC generates the check word. When CAS is finally asserted, both data and check words are written into memory simultaneously.

7.5.17 NORMAL READ CYCLE

The board drive signal is derived by the gating of the BDSEL+ and the DRIVE+ signals at U123-11 (21-E). This signal enables the backplane drivers U220 (28-C) and U223 (28-D). RAS and CAS occur in the normal fast fashion. (CASEN is set early in the cycle on the controller and since W- is high for the read cycle at U120-1 (22-C), the CAS flip-flop at U124 (22-C) sets early in the cycle, enabling BCASEN+ to the RAM drivers.)

The cycle proceeds in the same fashion as for the parity-check array card; i.e., data is driven onto the backplane as soon as it is output from the RAMs. Since no error correction is needed, the EDAC asserts no error flags. Also, CAS is extended by the latching of the RAS signal at U111-4 using VALID+ and CASEN+. Thus, for non-correction cycles, the ECA card cycles at the same rate as the standard array card, providing no system speed degradation.

7.5.18 SINGLE-BIT ERROR CORRECTION

The signal timing of the following description is illustrated in Figure 7-3.

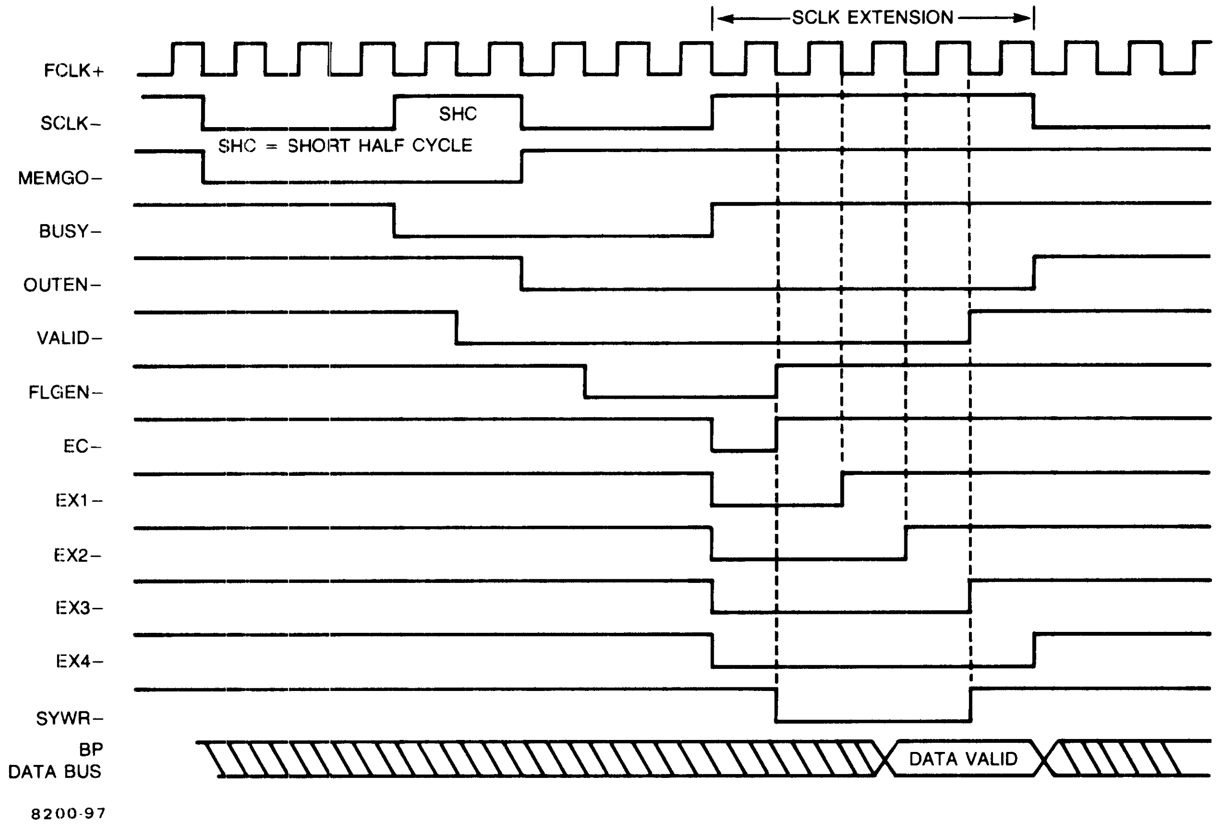


Figure 7-3. Error Correction Cycle

The read access proceeds exactly as that for a normal cycle until data is output from the RAMs and an error is detected. The EDAC is clocked by the CRCT+ signal from the delay line at U210-6 (23-C). This appears at the S1 control input as a high. Note that S0 is also high. This control mode causes the EDAC to latch the RAM data and test it for errors. The single error flag (SEF) line from the EDAC is enabled at this point. A short time later (20 ns) the ONGATE+ signal from the delay line enables the two AND-gates at U122 (27-C).

The following describes the SEF and ONGATE+ relationship:
When the CRCT+ signal occurs, data is assumed to be valid at the RAM outputs and, therefore, ready for inspection by the EDAC. The CRCT+ signal causes the EDAC to latch the data and test it. Although the SEF flag is enabled, there is no guarantee that it will be stable at this time; i.e., there may be glitches present. This is due to propagation delays in the EDAC for the several parity trees. When the ONGATE+ signal occurs, the SEF signal has settled and is assumed valid. Thus, the ONGATE+ signal actually gates out glitches on the SEF line.

At the same time, the other inputs of the AND-gates (U122-5 and -11) are enabled. This is true since the FLGEN+ is derived from the BDRIVE+ and the VALID+ signals at U123-6 (22-C). FLGEN+ is the flag enable signal used to provide the proper window for testing the EDAC error flags. As shown in Figure 7-3, the window is the long-half-cycle of SCLK during VALID, delayed by one FCLK cycle. Also, it occurs only during a read cycle. (Error correction is not done on write cycles.) It is only during the period of time defined by the gating of ONGATE+ and FLGEN+ that the SEF flag can be assumed valid.

Since a single-bit error is present, the SEF flag sets. The signal EC+ at the output of U122-6 goes high and is output to the processor over the backplane via U326-3 (21-B). This signals to the processor that extra time is needed for the error correction process. The processor responds by extending the short-half-cycle of SCLK from two to five FCLK cycles in length.

Also, the SEF flag starts the correction process by asserting the OFCAS+ signal at U122-8. This signal turns off CAS to the RAMs at U116-4 (23-D). The RAMs stop driving the data bus. The OFCAS+ signal appears at U116-11 which causes the S0 input of the EDAC to go low. This changes the mode of the EDAC chip to the correction mode so that the EDAC outputs corrected data onto the bus. Thus, as soon as the EDAC detects a single-bit error the SEF flag is gated back to switch it to the correction mode. The SEF flag remains set during the correction process.

The EC- signal on the backplane is de-asserted one FCLK after the leading of the short half-cycle of SCLK. This is done by resetting the flip-flop at U124-5 (27-D). The memory controller has noticed the clock extension and has delayed the VALID signal accordingly. (Refer to Error Logging in Section V, paragraph 5.6.5., for additional theory of operation.)

By the time the delayed VALID signal occurs, the backplane has settled with the corrected data.

Since the FLGEN+ signal resets with VALID, and since VALID resets one FCLK cycle before the end of the memory cycle, the input of the AND-gate at U122-11 will go low before the end of the memory cycle. This would cause CAS to be re-asserted at the RAMs and cause them to drive the data bus again, corrupting the corrected data. To prevent this, the SYNEN- signal derived from the SYNRQ- signal from the memory controller is gated at U120-12 (25-D) to insure that the OFCAS+ signal remains asserted during the correction cycle.

At the same time the EDAC chip outputs corrected data, it also outputs the error syndrome code identifying the bit in error. This code appears on the check word bus and is received by the Error Syndrome Latch and by the frontplane driver located at U303 (17-C). The SYNEN+ signal clocks the error latch and enables the frontplane drivers to send the error code to the controller. The controller stores the syndrome code in the log RAM.

7.5.19 DOUBLE-BIT ERROR DETECTION

When the EDAC detects a double-bit error, the double-bit error flag (DEF) as well as the SEF is set. The SEF flag still switches the EDAC to correction mode but double-bit errors cannot be corrected. Therefore, the output data from the EDAC is meaningless and the error code sent to the controller is not used. The invalid code is latched in the error syndrome latch, however. Most likely, the error code will not be any of the 22 valid codes.

The DEF flag produces the double-bit error signal (DBERR-) at U120-6 (27-C) which releases the 'parity disable' signal (PDSBL-) on the frontplane. This informs the controller that the ECA card cannot correct the data error. The controller then asserts the parity interrupt signal (PE-) since data from the memory access is in error. (Refer to Double-Bit Error Detection in Section V, paragraph 5.6.5.2).

7.6 PARTS LOCATIONS

The parts locations for the ECA are shown in Figure 7-4.

7.7 REPLACEABLE PARTS LIST

The replaceable parts for the ECA are listed in Table 7-4. Refer to Table 3-8 for the names and addresses of the manufacturers of the parts in the Manufacturer's Code List.

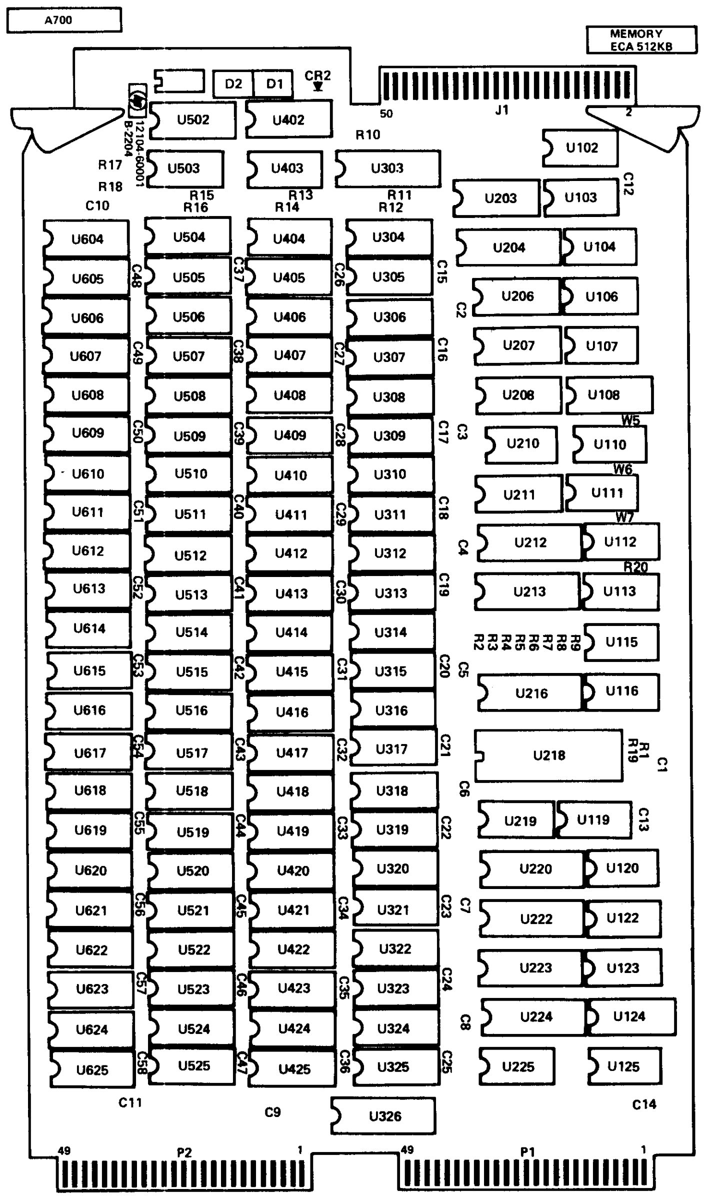


Figure 7-4. 12104A Parts Locations

Table 7-4. 12104A Replaceable Parts

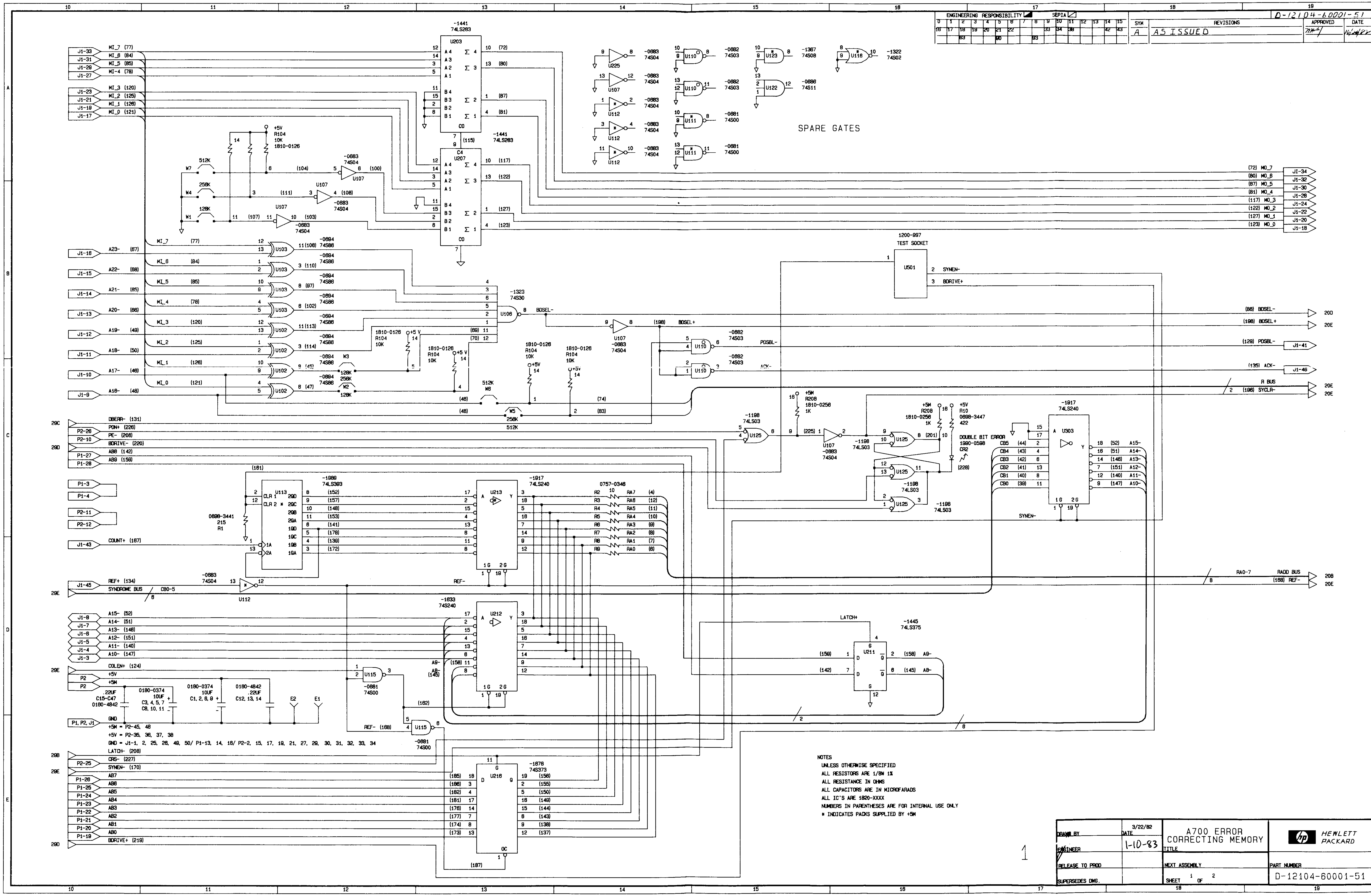
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12104-60001	3	1	PCA-ECA, 512KB	28480	12104-60001
	12104-64001	1	1	ASSEMBLY-AUTO INSERT (P/O 12104-60001)	28480	12104-64001
C1	0180-0374	3	11	CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C2	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C3	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C4	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C5	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C6	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C7	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C8	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C9	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C10	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C11	0180-0374	3		CAPACITOR-FXD 10UF+-10% 20VDC TA	56289	150D106X9020B2
C12	0160-4842	6	47	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C13	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C14	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C15	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C16	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C17	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C18	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C19	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C20	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C22	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C23	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C24	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C25	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C26	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C27	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C28	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C29	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C30	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C31	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C32	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C33	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C34	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C35	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C36	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C37	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C38	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C39	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C40	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C41	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C42	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C43	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C44	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C45	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C46	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C47	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C48	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C49	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C50	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C51	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C52	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C53	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C54	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C55	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C56	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C57	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C58	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
CR2	1990-0598	1	1	LED-VISIBLE	28480	5082-4190
D1	1990-0652	8	2	LED-VISIBLE	28480	1990-0652
D2	1990-0652	8		LED-VISIBLE	28480	1990-0652
R1	0698-3441	8	1	RESISTOR 215 1% .125W F TC=0+-100	24546	C4-1/8-T0-215R-F
R2	0757-0346	2	8	RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R3	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R4	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R5	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R6	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R7	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R8	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R9	0757-0346	2		RESISTOR 10 1% .125W F TC=0+-100	24546	C4-1/8-T0-10R0-F
R10	0698-3442	4	1	RESISTOR 422 1% .125W F TC=0+-100	24546	C4-1/8-T0-422R-F

Table 7-4. 12104A Replaceable Parts (continued)

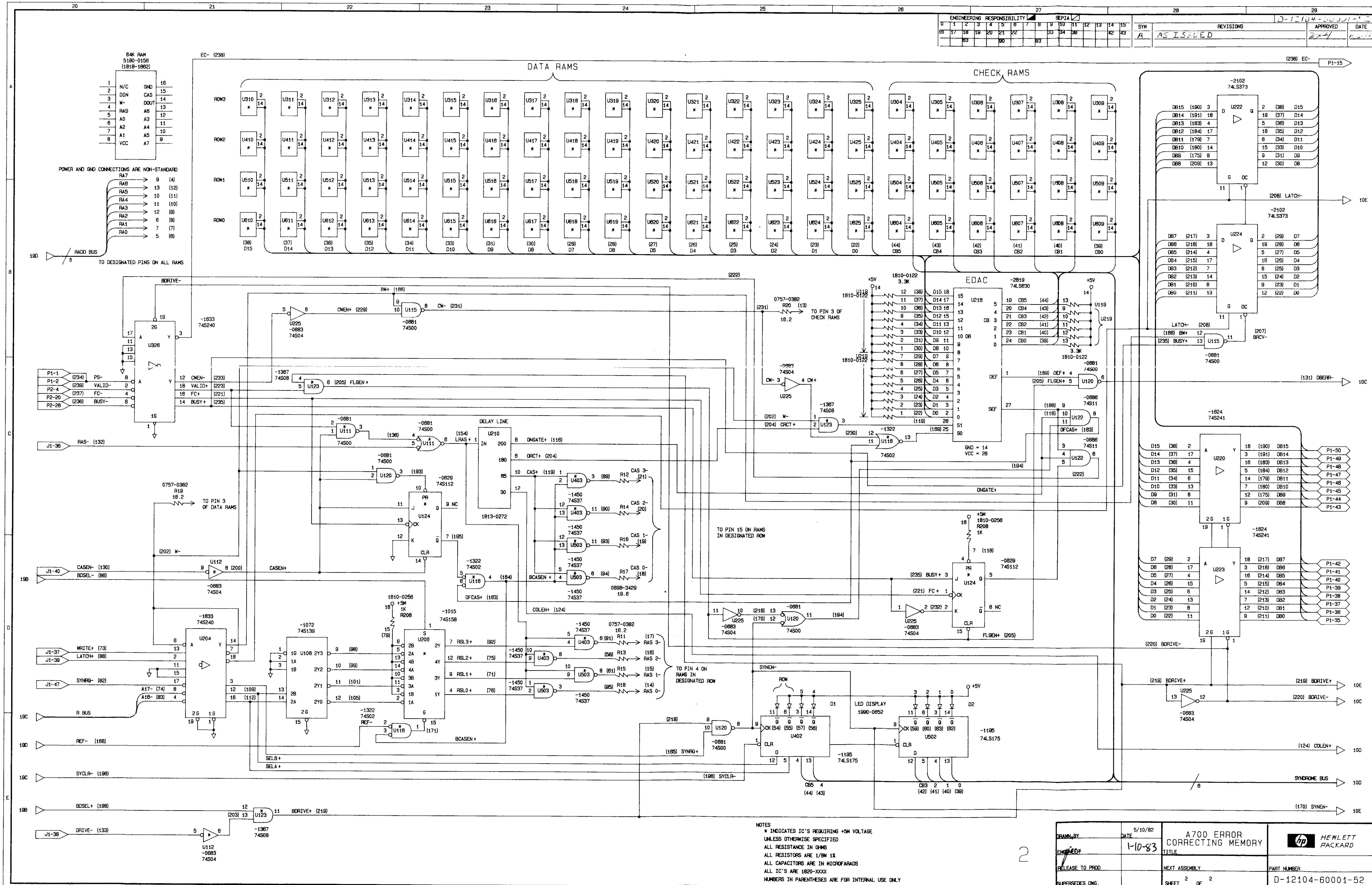
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R11	0757-0382	6	6	RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
R12	0698-3429	2	4	RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R13	0757-0382	6		RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
R14	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R15	0757-0382	6		RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
R16	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R17	0698-3429	2		RESISTOR 19.6 1% .125W F TC=0+-100	03888	PME55-1/8-T0-19R6-F
R18	0757-0382	6		RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
R19	0757-0382	6		RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
R20	0757-0382	6		RESISTOR 16.2 1% .125W F TC=0+-100	19701	MF4C1/8-T0-16R2-F
U102	1820-0694	9	2	IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U103	1820-0694	9		IC GATE TTL S EXCL-OR QUAD 2-INP	01295	SN74S86N
U104	1810-0126	1	1	RESISTIVE NETWORK-DIP	11236	760-1-R10K
U106	1820-1323	3	1	IC GATE TTL S NAND 8-INP	01295	SN74S30N
U107	1820-0683	6	3	IC INV TTL S HEX 1-INP	01295	SN74S04N
U108	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U110	1820-0682	5	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S03N
U111	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U112	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U113	1820-1989	7	1	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U115	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U116	1820-1322	2	1	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U119	1810-0122	7	2	RESISTIVE NETWORK-DIP	01121	314A332
U120	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U122	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U123	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U124	1820-0629	0	1	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U125	1820-1198	0	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS03N
U203	1820-1441	6	2	IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U204	1820-1633	8	3	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U206	1820-1015	0	1	IC MUXR/DATA-SEL TTL S 2-TO-1-LINE QUAD	01295	SN74S158N
U207	1820-1441	6		IC ADDR TTL LS BIN FULL ADDR 4-BIT	01295	SN74LS283N
U208	1810-0256	8	1	RESISTIVE NETWORK-DIP	01121	316A102
U210	1813-0272	4	1	IC-DELAY LINE	28480	1813-0272
U211	1820-1445	0	1	IC LCH TTL LS 4-BIT	01295	SN74LS375N
U212	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U213	1820-1917	1	2	IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U216	1820-1676	9	1	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U218	1820-2819	4	1		28480	1820-2819
U219	1810-0122	7		RESISTIVE NETWORK-DIP	01121	314A332
U220	1820-1624	7	2	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U222	1820-2102	8	2	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U223	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U224	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U225	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U303	1820-1917	1		IC BFR TTL LS LINE DRVR OCTL	01295	SN74LS240N
U304	5180-0156	4	88	IC-RAM, 64K 75 NS	28480	5180-0156
U305	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U306	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U307	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U308	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U309	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U310	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U311	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U312	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U313	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U314	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U315	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U316	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U317	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U318	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U319	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U320	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U321	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U322	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U323	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U324	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U325	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U326	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U402	1820-1195	7	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U403	1820-1450	7	2	IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U404	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U405	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U406	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U407	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156

Table 7-4. 120104A Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U408	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U409	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U410	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U411	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U412	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U413	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U414	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U415	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U416	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U417	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U418	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U419	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U420	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U421	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U422	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U423	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U424	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U425	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U502	1820-1195	7		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
U503	1820-1450	7		IC BFR TTL S NAND QUAD 2-INP	01295	SN74S37N
U504	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U505	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U506	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U507	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U508	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U509	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U510	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U511	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U512	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U513	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U514	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U515	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U516	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U517	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U518	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U519	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U520	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U521	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U522	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U523	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U524	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U525	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U604	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U605	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U606	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U607	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U608	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U609	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U610	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U611	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U612	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U613	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U614	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U615	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U616	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U617	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U618	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U619	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U620	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U621	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U622	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U623	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U624	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
U625	5180-0156	4		IC-RAM, 64K 75 NS	28480	5180-0156
W5	0811-3587	5	3	RESISTOR-FXD 0 OHM	28480	0811-3587
W6	0811-3587	5		RESISTOR-FXD 0 OHM	28480	0811-3587
W7	0811-3587	5		RESISTOR-FXD 0 OHM	28480	0811-3587



D-12104-60001-51
SPARE GATES
TEST SOCKET
DOUBLE BIT ERROR
SYNDROME BUS
RADD BUS
R BUS
NOTES
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY
* INDICATES PACKS SUPPLIED BY +5M
A700 ERROR CORRECTING MEMORY
HEWLETT PACKARD
DATE 3/22/82
1-10-83
SHEET 1 OF 2
PART NUMBER D-12104-60001-51



NOTES
* INDICATES IC'S REQUIRING +5M VOLTAGE UNLESS OTHERWISE SPECIFIED
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W 1%
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED	8/24	

TITLE: A700 ERROR CORRECTING MEMORY

DATE: 5/10/82, 1-10-83

HEWLETT PACKARD

PART NUMBER: D-12104-60001-52

SHEET 2 OF 2

2

8.1 INTRODUCTION

Control Store of the A700 computer extends microprogramming capability to the user. The control store may consist of either or both the HP 12153A Writable Control Store (WCS) cards and the HP 12155A PROM Control Store (PCS) cards. The HP 12156A Floating Point Processor card also operates within the control store system.

The WCS and PCS cards are both covered in this section. Paragraphs under 8.3 and 8.4 are for the WCS card and paragraphs under 8.5 and 8.6 are for the PCS card. The floating point processor card is covered in Section IX of this manual.

8.2 PHYSICAL CHARACTERISTICS

The WCS and PCS cards are installed sequentially in the A700 backplane immediately below the lower processor card. Up to a total of four cards of either WCS, PCS, or both cards and one FPP card can be used. These cards communicate with the processor through the micromachine control-store bus which is contained in the frontplane. The backplane provides mechanical support, power, and for the WCS card only the backplane is used to communicate with the main memory array.

The power supply specifications for the cards are covered in Section I of this manual (refer to Table 1-1). The HP 12153A Writable Control Store card is shown in Figure 8-1, and the HP 12155A PROM Control Store card is shown in Figure 8-2.

8.3 WCS CARD OPERATION

The 12153A Writable Control Store card functions as a control store for the processor by allowing the user to write microcode, to read microcode, and to access the microcode for the speed improvements achieved in fast operating firmware subroutines. The writing and reading of microcode requires backplane access as well as frontplane access to control store. To prevent contention between these two planes, the WCS card can be turned on for frontplane access and off for backplane access.

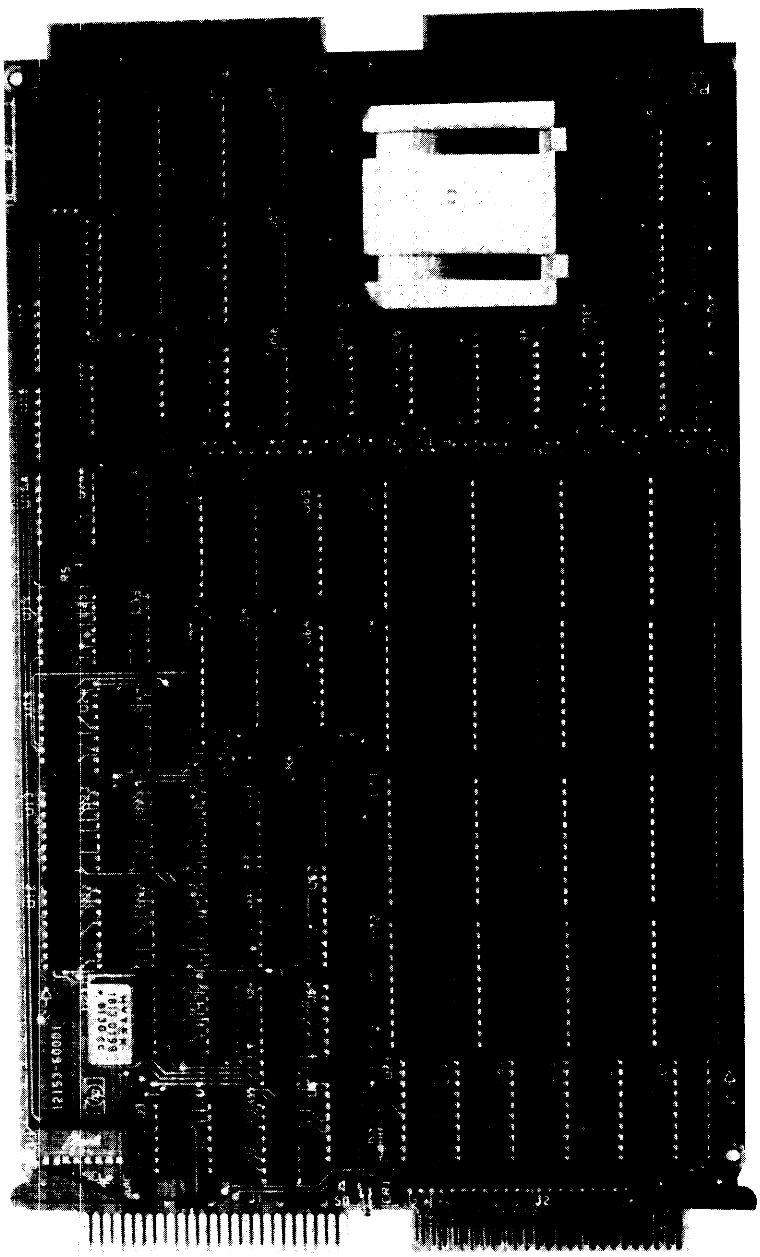


Figure 8-1. Writable Control Store Card (12153-60001)

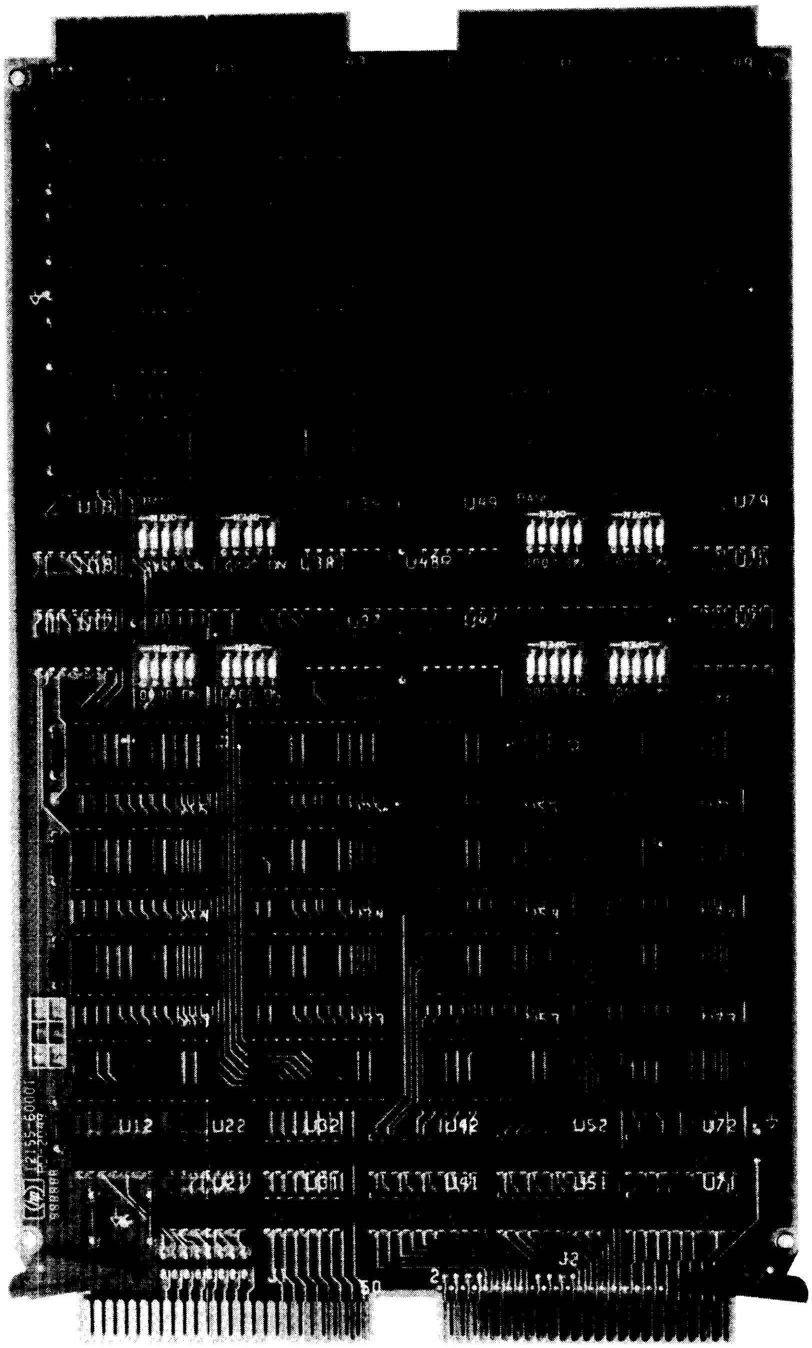


Figure 8-2. PROM Control Store Card (12155-60001)

While WCS is on, it acts as control store for the processor; when addressed it sends a signal that disables any lower priority control store and outputs data to the control store data bus. When WCS is on, all attempted backplane accesses are ignored with the following exceptions: The first exception is the instruction OTA 32 which turns WCS on or off, and the second exception is the instruction LIA 32 which reads the status of WCS.

When WCS is on the I/O Master signals are generated but signals CSON+ and CSON- prevent any changes to the card except when OTA 32 and LIA 32 instructions are given. Also, LIA 30 and LIA 31 instructions in the program will appear to read from the card but the data that is read will not be valid.

While WCS is off, the user has complete access to WCS through the backplane and any frontplane accesses are ignored. If WCS is off, it effectively does not exist as control store yet the priority line is passed through the card so that the priority chain is not broken.

Addresses and data must be multiplexed or otherwise separated between front and back planes. In general, this is done using tri-state buffers which are enabled or disabled by the on or off state of signal CSON.

To provide maximum flexibility to the user there are no write only registers in WCS. Any address, data, or status loaded into WCS can be read by the user.

WCS supports DMA and programmed I/O. The address from the backplane is loaded into a counter which can be incremented. Backplane addresses are physical but frontplane addresses are logical. A map RAM is used to provide logical to physical mapping of addresses from the frontplane. The map RAM is loaded and read through the backplane.

8.4 WCS CARD THEORY OF OPERATION

The WCS card theory of operation is covered in the following paragraphs. The schematic for this description is provided at the rear of this section of the manual. Refer to HP 1000 L-Series I/O Interfacing Guide, part number 02103-90005 for information and schematics on the I/O master. Also the block diagram for the WCS card is provided in Figure 8-3. The integrated circuits (chips) are referenced by their U-numbers and schematic locations. For example, U69 (13-C) means chip U69 on schematic sheet no. 1 is located by coordinates 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc. and on sheet no. 2 it is numbered 20, 21, etc. The hyphenated pin number with the U-number locates an input or output and the section of the chip that is being described.

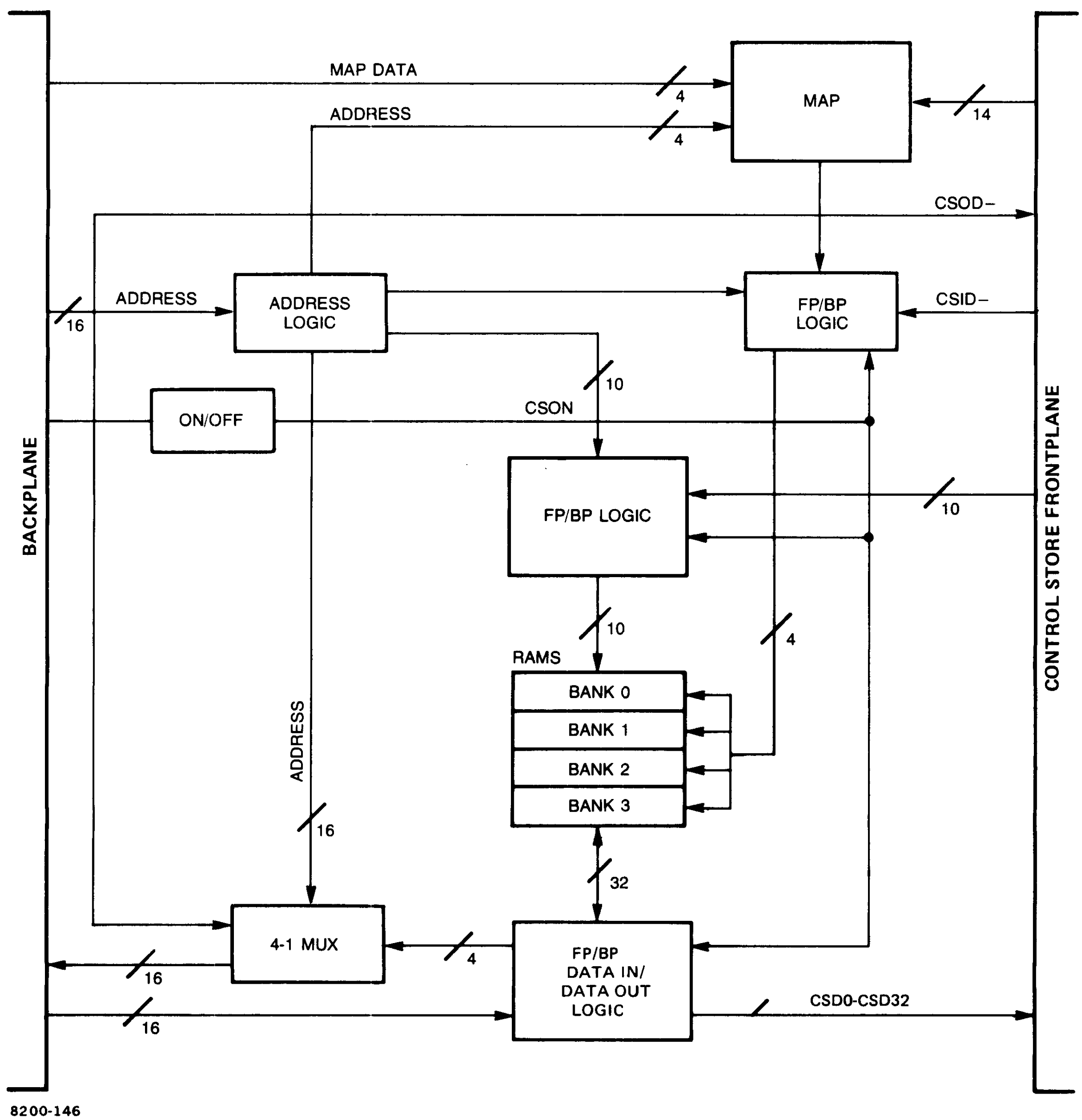


Figure 8-3. WCS Card Block Diagram

8.4.1 ON/OFF LOGIC

The WCS is turned on or off as control store by instruction OTA 32 with the sign bit of A set to 1 for on and 0 for off. OTA 32 generates a BCS3- (Bus Control Signal) output from the I/O Master. The sign bit of A (data bus bit 15) becomes the data input to a D-type flip-flop U16A-12 (22-B), a type 74LS74A chip, U16A-12 is clocked by the gating of BCS3- and CKDAT- into U16-9 and -10 (21-C) (When WCS is on, an LED (CR1) lights. It is located between the frontplane connectors.)

The clear of the U16A is tied to RST- which makes sure that power up is in the off status. CSON- and CSON+ are buffered through U41A and U41B (23-B), type 74S08 gates, to provide enough power to handle the loading on the CSON line. CSON- is connected to the test connector J1-1 through U3B, a type 74LS05 open-collector inverter, to isolate the U16A from any noise introduced by the test connector.

8.4.2 BACKPLANE INTERFACE

The backplane data bus is input to bi-directional buffers U45 and U55 (21-B), type 74LS245 chips. The direction of these buffers is controlled by the assertion of the I/O Master signals BCS1-, BCS2-, BCS3-, BCS5-, BSC6-, or BCS7- that are combined through OR gate U26 (21-C). During assertion of BCS1-, BCS2-, or BCS3-, the direction of the U45 and U55 buffers is from the backplane to the card. During the assertion of BCS5-, BCS6-, or BCS7-, the direction is from the card to the backplane.

The I/O Master requires an SRQ- signal for each data transfer. In the WCS card the SRQ- signal is the Q- output of U36A-6 (22-D),

a type 74LS74A flip-flop. The D-input of the flip-flop, U36A-2, is tied high, and the flip-flop is clocked by DVCMD- and SCLK+ through gate U16 (21-D). The U36-6 is cleared by the signal SACK- at U36-1.

8.4.3 BACKPLANE ADDRESS LOGIC

An address is output to the WCS card with an OTA 31 instruction which generates a BCS2- signal output from the I/O Master. The address latch on the WCS card is a 16-bit counter made up of four chips U42, U43, U52, and U53 (24-B, -C, -B, and -D), type 74LS191. The counter is loaded on the assertion of LDCTR- from AND gate U16-11 (22-D) when signals BCS2- and CKDAT- are applied at the same time that the backplane data inputs through U45 and U55 are present at the data pins of the counter.

8.4.3.1 Address Counter

For programmed I/O the address must be loaded for each data transfer or programmatically incremented. For DMA the address must be loaded for the first data transfer and is incremented for each succeeding transfer. The address counter is enabled to count by DVCMD- and CNTEN- through U16-6 (24-D).

Since DVCMD- is asserted on DMA in start-up, signal CNTEN- is used to prevent incrementing the counter before the first data transfer occurs. CNTEN- is the not Q-output of the D-type flip-flop U36A-8. U36A-8 is preset by BCS1- or BCS5- into OR gate U26A-12 and -13 (23-D). The D-input is tied low and it is clocked with LDCW1-. Thus, CNTEN- will be low after the assertion of BCS1- or BCS5- and the address counter will be enabled only when CNTEN- is low and DVCMD- goes low.

The LDCW1- signal will clock U36A-8 (23-D) low so that CNTEN- will be high. RST- is input to U36A-13, the clear input, to assure that CNTEN- will be high on power up. CNTEN- is output to test connector J1-5 through inverter U3 (24-E).

Synchronous counting in the address is provided by SCLK+ which is input to the CK (clock) inputs of all the counters. The ripple-carry outputs of the counters are connected to the enable inputs of the upper counters as recommended by the manufacturer.

8.4.3.2 Control-Store Word Address

The word address is in bits 0 to 11 of the data bus, and bit 15 (sign bit) is used to the select lower- or upper-half of the 16-bit control-store word. If bit 15 is 0 the lower half is selected, if it is 1 the upper half is selected. This is so the user can address the WCS card on control-store word boundaries (32 bit boundaries) and to handle the translation of 16 to 32 bits.

To insure accurate addressing and loading of the data RAMs, bit 15 of the data bus is loaded into the least significant bit of the counter. Thus, the actual address of the control-store word is in counter bits 1 through 12 and the least significant counter bit (HIEN+) is used to select the upper or lower half of the addressed word to be read or written.

Since the map RAM and the data RAMs use the same hardware for addressing and reading and writing, bit 14 of the data bus is used to select data RAMs when low or map RAM when high. This bit is loaded into the most-significant-bit of the counter and becomes MAPEN+.

8.4.3.3 Counter Controls

If the counter is incremented to a value greater than the 4k-word address space, LSBYT- and IRQ- will be asserted to generate an interrupt that will end DMA and notify the user.

To prevent an unknown state of the counter on power up, flip-flop U15 (26-C) is used. RST- is tied to the CL (clear) input so that on power up (PON+) or a CLC 0 instruction, the Q output of the flip-flop is low. LDCTR- is tied to its CK (clock) input and its D input is tied high.

In operation, when the counter is loaded, U15 is clocked high, and the Q output goes to U26A-5 (26-B) as CTON+. This signal is ANDed with CADB12 at U26A-4, inverted in U63 (26-B) and output to IRQ- and LSBYT- lines on the backplane. Thus, from PON+ or CLC 0 until the counter is loaded, IRQ- and LSBYT- are held high by U15.

When the counter is loaded, U15-5 goes low making signal CADB12 control the value of IRQ- and LSBYT-; i.e., if CADB12 goes high, IRQ- and LSBYT- go low. If set, IRQ- and LSBYT- can be cleared by instruction CLF 30 and the counter can be loaded when an address is less than 4k. Also, CADB12 is ORed with MAPEN+ at U25-1 (25-B), to generate an inhibit signal that prevents the writing of incorrect data into the data RAMs.

To avoid conflict between frontplane, backplane, data RAMS, and map RAM on the map RAM address line, the counter address bits 0-3 (CADB0 - CADB3) are input to buffer U51 (28-B). The output of this buffer is input to the map RAM address lines when enabled by GATEN- which is a result of MAPEN+ and CSON- being high into gate U31 (27-C). When GATEN- is low it means that the map RAM is selected and WCS is off.

8.4.3.4 WCS Block Selection

The lower 10 data RAM address bits are input to U51 and U62 (28-B and 28-C) that are enabled by CSON off and MAPEN+ low into gate U61 (27-C). Two additional address bits are needed to select the individual 1k-word blocks of writable control store to be addressed. These two bits (CADB10 and CADB11) are input to U5-14 and U5-13 (34-B), a 2-to-4 bit decoder. The decoder is enabled by CSON+; i.e., the WCS off signal. The eight output lines of the decoder are input to four sections of two-input AND gate U4 (34-B and 35-B). Each AND gate output is tied to the chip select of one bank of the data RAMs (i.e., 1k-word control store data).

8.4.4 BACKPLANE DATA LOGIC

The following sections describe the logic for writing data into the data RAMs and into the map RAM.

8.4.4.1 Data RAM Input Logic

The type MK4801A-90 1k x 8-bit static RAM used for the data RAMs have common data-in/data-out pins. This requires buffering the input data to prevent contention between input and output data or shorts between front and back planes. The four input buffers of eight data bits are U44, U54, U64, and U65 (31-B, -C , -B, and -D) and have their inputs coming from the card side of U45 and U55 backplane buffers. The input buffers are enabled by the assertion of signal DATIN- from gate U14-11 when BCS1- is asserted and CSON is off.

The static RAMs require that the Output Enable of the RAM be held high during a write cycle and low during a read cycle. On WCS the Output Enable is tied to DATIN+ which is an inverted DATIN- from U63 (31-D). This assures the Output Enable is high during write and low the rest of the time.

Since the control store data word is 32 bits wide and the backplane data bus is 16 bits, only half the data word can be loaded in one transfer. The HIEN+ signal which is the least significant bit output from the counter is used to select the lower or upper half of the RAM bank.

The Write Enable signal to the RAMs is a logical combination of several signals. The assertion of BCS1- and CKDAT- at U14-1 and U14-2 (23-A) generates DBVALID-. DBVALID- is gated with CSON- at U14-5 and U14-4 (25-A) to generate WRVALID- which indicates that WCS is off and input data is valid. MAPEN+ and CADB12 into U25-2 and U25-1 (25-B) provide an output when the data RAM and is within the 4k-word address range. The output U25-3 is ANDed with HIEN+ in U25-4 and -5 (26--B) to provide WRLO-. HIEN+ is inverted by U63 (26-B) and also ANDed with the output U25-2 (26-B) to provide WRHI-.

WRLO- gated with WRVALID- in U14-10 and -9 (27-B) to provide WENLO- which is the Write Enable input to the lower half of the RAM banks. WRHI- is gated with WRVALID- in U25-10 and -9 (27-B) to provide WENHI- which is the Write Enable input to the upper half of the RAM banks.

In this way, the RAMs which contain bits 0 through 15 of the control store word all get a Write Enable signal (low true) when HIEN+ is low, WCS is off, data is valid on the backplane, data RAMs are selected (MAPEN+ low), and the address is less than 4k. The RAMs which contain bits 16-31 of the control-store word all get a Write Enable signal when HIEN+ is high, WCS is off, data is valid on the backplane, data RAMs selected, and the address is less than 4k.

8.4.4.2 Map RAM Input Logic

Bits RMDB0 - RMDB3, the lower four bits output from buffer U65 (31-D), are input to the data input pins of the map RAM U6 (32-B). GATEN- (map RAM selected and WCS off) is gated with DBVALID- (valid data on the backplane) at U61-4 and -5 (32-B) and input to the Write Enable of the U6. Chip Select of U6 is tied low so that the map RAM is always enabled.

8.4.5 BACKPLANE OUTPUT LOGIC

For the user to have access to WCS data, address, map data, and status, the following signals are input to the multiplexers (MUX). The MUXs ARE U24, U32, U12, U22, U34, U13, U23, and U33 in the schematic area of 36-B, -C, -D, and 37-B, -C, -D):

C0 Inputs	Lower 16 bits of control store data output of data RAMs.
C1 Inputs	Upper 16 bits of control store data output of data RAMs.
C2 Inputs	Map RAM output, input to the two least significant MUX chips (U23,U33).
C2 Input	Status, CSON+, is the most significant C2 input of the most significant chip (U24).
C3 Inputs	Address counter contents.

The MUX output is chosen from one of the four inputs by the values of the A and B Select inputs. The following table shows the output selected for each combination of A and B inputs.

A	B	OUTPUT
0	0	C0 Low RAM bits
1	0	C1 High RAM bits
0	1	C2 Map RAM and status
1	1	C3 Address

Due to timing requirements of the backplane during DMA input, the MUX enable and select bits must be decoded and input to the MUX before the actual DMA request is made. This is accomplished by using the IN bit of DMA Control Word 1. The IN bit is bit no. 7 of Control Word 1 where "1" means IN from WCS-to-memory, and "0" means OUT from memory-to-WCS. Backplane data bus bit no. 7 is input to U16A-2 (32-D) D-type flip-flop which is clocked by LDCW1-. The Q output of this flip-flop reflects the IN bit value and it is called DMAIN+. The value of the flip-flop output will only change when LDCW1- is asserted. DMAIN+ is output to test connector J1-4 through U3-11 (33-D).

The MUX output must be disabled by signal MUXEN+ provided by the OR of DMAIN+ (DMA OUT) or BCS1-, or BCS2-, or BCS3- in gate U31-5 and -4 (33-C). It is enabled by MUXEN- by the OR of DMAIN- (DMA IN) or the assertion of BCS5-, BCS6-, or BCS7- in gate U41-12 and -13 (34-C).

8.4.6 FRONTPLANE INTERFACE

To the frontplane WCS appears as a read-only memory. The processor puts an address on the control store address bus and at a given time later expects to see data on the control store data bus.

8.4.6.1 Control-Store Address Logic

The control-store address bus is input to buffers U91 and U101 (28-D and 28-C) which are enabled by CSON. The lower 10 bits output from these buffers are tied to the address inputs of the data RAMs. The upper four bits of the address output from the buffers are tied to the address input of the map RAM, U6 (32-B). The two least significant bits output from the map RAM, MPOUT0 and MPOUT1, are input to the 2-to-4 decoder U5 (34-B) at U5-2 and -3 which is enabled by CSON-. The eight decoder outputs are input to the AND gates of U4 (34-B), each of whose output is tied to the chip select of one bank of the data RAMs. MPOUT0 and MPOUT1 are also connected to the J1-2 and J1-3 test connector through U3 (33-B).

8.4.6.2 Control Store Data Logic

The output of the data RAMs (control store data) is input to buffers U91A (48-B), U81 (48-B), U81A (48-C), and U71 (48-D). These buffers are enabled in the following way: Signals CSON and MPOUT3 are combined in AND gate U61-9 and -10 (32-C) and gated with CSID+ in U61-13 and -12D (47-D). (CSID- is buffered and inverted to CSID+ by U31-8.) The enable is delayed 60 nanoseconds through delay line U21 (47-D) to prevent contention on the control store data bus. The buffer output is enabled onto the frontplane when WCS is on, control store is not disabled by higher priority control store, and the address is in the address space located on the WCS card.

8.4.7 DAISY CHAIN LOGIC

The Control Store Input Disable (CSID-) signal is taken from the frontplane and is low true. CSID- is the CSOD- signal from another control store card and indicates that a higher priority control store is selected. The CSID- signal is tied through resistor R6, pin 10 (41-D) to +5V to enable control store cards so that they can be added to or removed from the system without affecting other cards.

The Control Store Output Disable (CSOD-) signal (for disabling lower priority control store) is generated by the gating of the most-significant-bit map RAM output MPOUT3 (U6-11) and CSON at U61-10 and -9 (32-C) which is then ORed with CSID- at U41-9 and -10 (48-E). This output becomes CSOD- which is "0" for disable lower priority control store and "1" for no disable of lower priority control store. CSOD- becomes FP_CSID WC- going into the lower processor.

8.5 HP 12155A PROM CONTROL STORE CARD OPERATION

The PROM Control Store Card provides a user with non-volatile storage for his microprograms. The PCS card for the A700 Computer becomes an integral part of the computer's control store and extends the flexibility of the micromachine.

8.5.1 PCS CARD INSTALLATION

The PCS functions properly in any control store slot but it is more useful when it is installed in the lowest priority slot on the frontplane. In this postion, the same logical address space could exist on a WCS card and a PCS card at the same time, with WCS having priority when it is enabled and PCS having priority when WCS is disabled. The card provides PROM storage for up to 8k microwords. The PROM control store card can be fully or partially loaded with PROMs. A switch setting for each bank enables or disables the bank. A bank can be disabled even if it is loaded with PROMs, however, the card must be removed from the system to have access to the switches.

8.5.2 PROM BANKS

The PROM card has sockets into which the PROMs are loaded. For each bank of sockets for 1k of microwords, there is a five-position switch. Switch settings are silk-screened on the card to use during installation. Switch position 5 of each switch should be set to OFF when there are no PROMs loaded in the bank or when a loaded bank is to be disabled. The remaining four positions represent the logical module address. The switch positions should be set to match the address located in the bank. Table 8-1 gives the settings for each module.

Table 8-1. Table 8-1. PROM Bank Switch Settings

Module Number	Decimal	Addresses Octal	Hex	Switch Settings 4	3	2	1
0	0-1023	0-1777	0-3FF	0	0	0	0
1	1024-2047	2000-3777	400-7FF	0	0	0	1
2	2048-3071	4000-5777	800-BFF	0	0	1	0
3	3072-4095	6000-7777	C00-FFF	0	0	1	1
4	4096-5119	10000-11777	1000-13FF	0	1	0	0
5	5120-6143	12000-13777	1400-17FF	0	1	0	1
6	6144-7167	14000-15777	1800-1BFF	0	1	1	0
7	7168-8191	16000-17777	1C00-1FFF	0	1	1	1
8	8192-9215	20000-21777	2000-23FF	1	0	0	0
9	9216-10239	22000-23777	2400-27FF	1	0	0	1
10	10240-11263	24000-25777	2800-2BFF	1	0	1	0
11	11264-12287	26000-27777	2C00-2FFF	1	0	1	1
12	12288-13823	30000-31777	3000-33FF	1	1	0	0
13	13824-14335	32000-33777	3400-37FF	1	1	0	1
14	14336-15359	34000-35777	3800-3BFF	1	1	1	0
15	15360-16383	36000-37777	3C00-3FFF	1	1	1	1

Note: The switch settings are don't cares if the bank is not loaded with PROMs. Switch position 5 is never a don't care.

8.6 PCS THEORY OF OPERATION

The PCS card theory of operation is covered below. For the theory of operation use the block diagram shown in Figure 8-4 and the schematic of the card at the rear of this section of the manual. The integrated circuits (chips) are referenced by their U-numbers and schematic location. For example, U69 (13-C) means chip U69 on schematic sheet no. 1 is located by coordinates 13 and C; where the horizontal grid on sheet no. 1 is numbered 11, 12, etc. and on sheet 2 it is numbered 21, 22, etc.

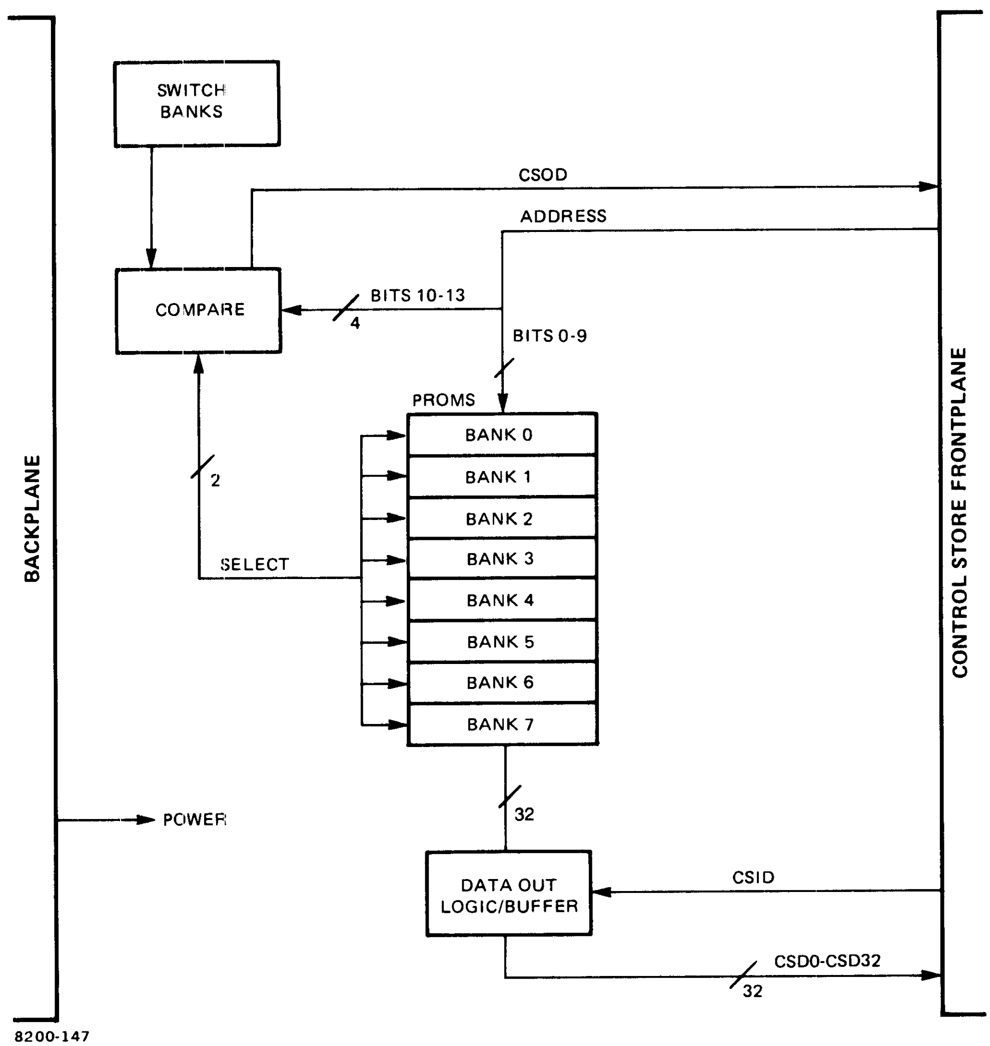


Figure 8-4. PCS Card Block Diagram

8.6.1 PRIORITY CHAIN

The PCS card plugs into the A700 Computer backplane and receives power and ground from the backplane. The priority chains on the backplane are passed through the card where on the backplane connector P1, pin-1 is tied to pin-2 and pin-3 is tied to pin-4 and on backplane connector P2, pins-11 and -12 are tied together. These are the only connections on the backplane. Frontplane interface and the daisy chain logic will be covered in the following sections.

8.6.2 FRONTPLANE INTERFACE

On the frontplane the PCS is part of the main control store. It takes an address from the control store address bus and compares it to the addresses located on PCS. If the addresses match PCS drives the control store data bus and sends a signal to to disable lower priority control store and/or the base set control store on the lower processor card.

All eight banks of PROMs use identical logic, therefore, only Bank 0 will be described in detail here. The data driver output enable logic and the daisy-chain logic will be covered in the next paragraph below.

The control-store address is input to the buffer drivers U71 and U72 (21-A and 21-B) from the control-store address bus on the frontplane. These drivers are always enabled.

The lower 10 address bits are input direct from the buffers to the address inputs of the PROMs, and the upper four address bits select the particular bank to be enabled. The upper four address bits PRA10 - PRA13 are input to quad exclusive-OR gates. These are U17, U37, U47, U77, U19, U39, U49, and U79 which are located in the schematic area of 1-A, -B, -D, -E and 14-A, -B, -D, -E. Address bits PRA10 - PRA13 are compared in the gates with the bank module number. There is one quad of gates for each of the eight banks along with a five-gang s.p.s.t. switch.

The switch settings provide the bank module number which is the second input to each of the exclusive-OR gates. For example, address bit 10 (PRA10) is paired with switch position 1, address bit 11 (PRA11) is paired with S2 for switch position 2, etc., and switch position 5 is closed to select the bank as active. Switch position 5 also activates the bank select line SEL0-, etc. going to J1, the diagnostic test connector.

If the address bit matches the switch setting, a "0" is output by the associated exclusive-OR gate. The four exclusive-OR outputs are input to NOR gate U18 (12-A) with switch position 5 as the other input. If any one of these inputs is high, the output of the NOR will be low. The PROM bank is selected with a high output from the NOR, that is, all address bits match and switch position 5 low (ON). The output of the NOR, AEN-, is input to pins 18 and 19 of the PROMs in bank 0 and into a 5-input NOR-gate in the output enable and daisy chain logic.

The PROM data output is input to four buffer drivers U41, U42, U51, U52 (38-A, -B, -C, and -C) which when enabled drive the control store data bus on the frontplane.

8.6.3 DAISY CHAIN AND OUTPUT DRIVER ENABLE LOGIC

Two NOR-gates of U22 (16-B, 17-C) are used to determine if one of the banks of PROMs is selected. The select lines, such as AEN+, are input to the gates with the unused inputs tied low. If any input is high, i.e., a bank is selected, the NOR-gate output is low. The outputs of the U22 gates are input to AND gate U32-4 and -5 (17-B). A low output from U32-6 will indicate one of the banks is chosen. This signal, PRSEL-, is input to gate U32-10 (18-B) with CSID- as the other input to U32-9. When CSID- is low it indicates a higher priority control store card is enabled. The output of this gate is driven onto the frontplane as CSOD- (FP_CSIDWC- into the lower processor).

The signal PRSEL- is also inverted by U31-4 and -5 (17-B) and input to gate U31-10 with CSID- at U31-9. The output of this gate is signal OEN- which is input to the low-true-enable inputs of the output drivers. OEN- is inverted by U31-12 and -13 (18-B) and input to the high-true-enable inputs of the drivers U41, U42, U51, and U52 (38-C, -C, -B, and -A). Thus, these drivers will be enabled when CSID- is high (no higher priority control store is enabled) and one of the PROM banks is selected.

8.6.4 DIAGNOSTIC INTERFACE

The second 50-finger edge connector on the frontplane end of the card will be used for diagnostic purposes. The eight-bank enable lines are output directly to the test connector. These lines read the status of position 5 of each of the switches, i.e., whether the bank is enabled or not. The PROM enable signals (bank is enabled and address matches) are output to the test connector through open-collector inverters U12 and U21 (16-B and 16-D) to isolate the circuit from the connector. This makes a total of 16 lines output to the test connector. (When the PCS card is enabled, and LED (CR1) lights on the card. It is located between the frontplane connectors.)

8.7 PARTS LOCATIONS

The parts locations for the HP 12153A WCS card are shown in Figure 8-5 and the part locations for the HP 12155A PCS card are shown in Figure 8-6.

8.8 REPLACEABLE PARTS LIST

The replaceable parts for the HP 12153A WCS card are listed in Table 8-2 and the replaceable parts for the HP 12155A PCS card are listed in Table 8-3. Refer to Table 3-8 for the names and addresses of the manufacturers of the parts in the Manufacturer's Code List.

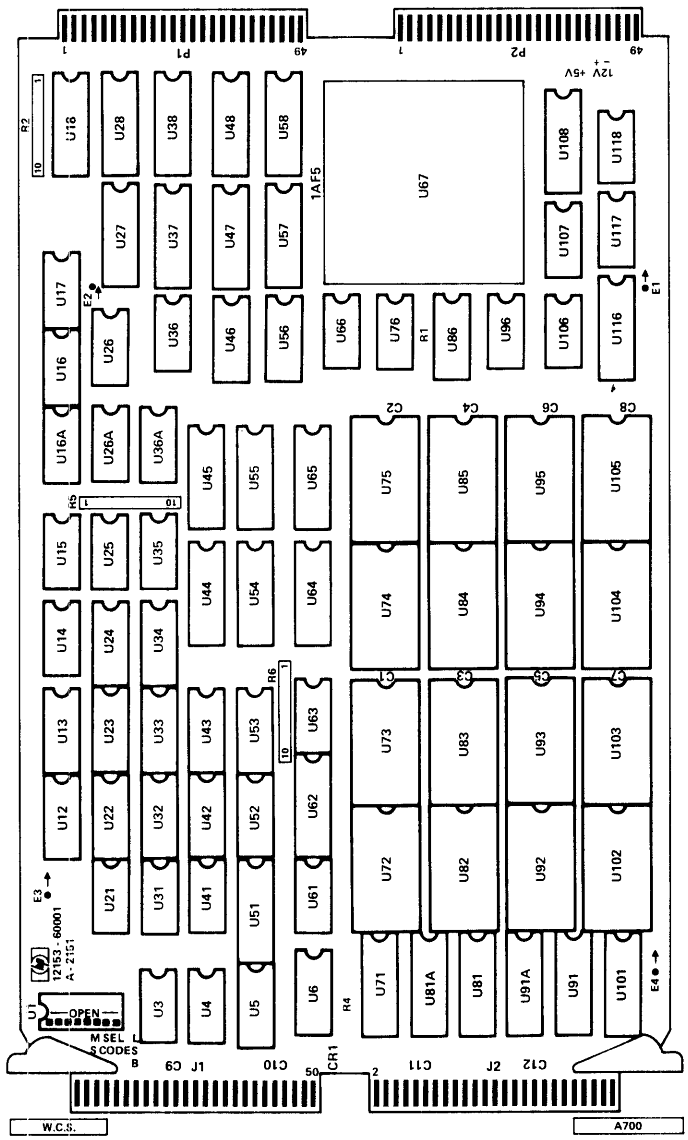


Figure 8-5. HP 12153A WCS Card Parts Locations

Table 8-2. HP 12153A WCS Card Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12153-60001	2	1	PCA-WCS	28480	12153-60001
				PART OF 12153-64001		
	12153-64001	0	1	ASSEMBLY-AUTO INSERT	28480	12153-64001
C1	0160-4832	4	12	CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C2	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C3	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C4	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C5	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C6	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C7	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C8	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C9	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C10	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C11	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
C12	0160-4832	4		CAPACITOR-FXD .01UF +-10% 100VDC CER	28480	0160-4832
CR19	1990-0485	5	1	LED-LAMP LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
R1	0757-0280	3	1	RESISTOR 1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1001-F
R2	1810-0280	8	1	NETWORK-RES 10-SIP10.0K OHM X 9	01121	210A103
R4	0757-0401	0	1	RESISTOR 100 1% .125W F TC=0+-100	24546	C4-1/8-T0-101-F
R5	1810-0279	5	2	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R6	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
U1	3101-2243	6	1	SWITCH-DIP 8 ROCKER	28480	3101-2243
U3	1820-1200	5	1	IC INV TTL LS HEX	01295	SN74LS05N
U4	1820-1367	5	3	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U5	1820-1072	9	1	IC DCDR TTL S 2-TO-4-LINE DUAL 2-INP	01295	SN74S139N
U6	1816-1005	9	1	IC-RAM 16 X 4	28480	1816-1005
U12	1820-1238	9	8	IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U13	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U14	1820-1208	3	4	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U15	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U16	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U16A	1820-1112	8	3	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U17	1820-1199	1	2	IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U18	1820-1997	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG PRL-IN	01295	SN74LS374N
U21	1813-0199	4	1	IC-DELAY HY-5003	07910	HY-5003
U22	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U23	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U24	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U25	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U26	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U26A	1820-1201	6	1	IC GATE TTL LS AND QUAD 2-INP	01295	SN74LS08N
U27	1820-2024	3	10	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U28	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U31	1820-0681	4	3	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U32	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U33	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U34	1820-1238	9		IC MUXR/DATA-SEL TTL LS 4-TO-1-LINE DUAL	01295	SN74LS253N
U35	1820-1208	3		IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U36	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U36A	1820-1112	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U37	1820-2102	8	4	IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U38	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U41	1820-1367	5		IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U42	1820-1278	7	4	IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
U43	1820-1278	7		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
U44	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U45	1820-2075	4	2	IC MISC TTL LS	01295	SN74LS245N
U46	1820-1240	3	1	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U47	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U48	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U51	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U52	1820-1278	7		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
U53	1820-1278	7		IC CNTR TTL LS BIN UP/DOWN SYNCHRO	01295	SN74LS191N
U54	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U55	1820-2075	4		IC MISC TTL LS	01295	SN74LS245N
U56	1820-0629	0	2	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U57	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U58	1820-2102	8		IC LCH TTL LS D-TYPE OCTL	01295	SN74LS373N
U61	1820-1449	4	2	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U62	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U63	1820-1199	1		IC INV TTL LS HEX 1-INP	01295	SN74LS04N
U64	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N

Table 8-2. HP 12153A WCS Card Replaceable Parts (continued)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U65	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U66	1820-1322	2	2	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U67	1AF5-6001	0	1	IOP CHIP	28480	1AF5-6001
U71	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U72	1818-1614	0	16	IC-MK4801AN-90	50088	MK4801AN-90
U73	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U74	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U75	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U76	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U81	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U81A	1820-1624	7	6	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U82	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U83	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U84	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U85	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U86	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U91	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U91A	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U92	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U93	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U94	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U95	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U96	1820-1451	8	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N
U101	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U102	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U103	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U104	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U105	1818-1614	0		IC-MK4801AN-90	50088	MK4801AN-90
U106	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U107	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U108	1820-1633	8	2	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U116	1820-1633	8		IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U117	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U118	1820-1451	8		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S38N

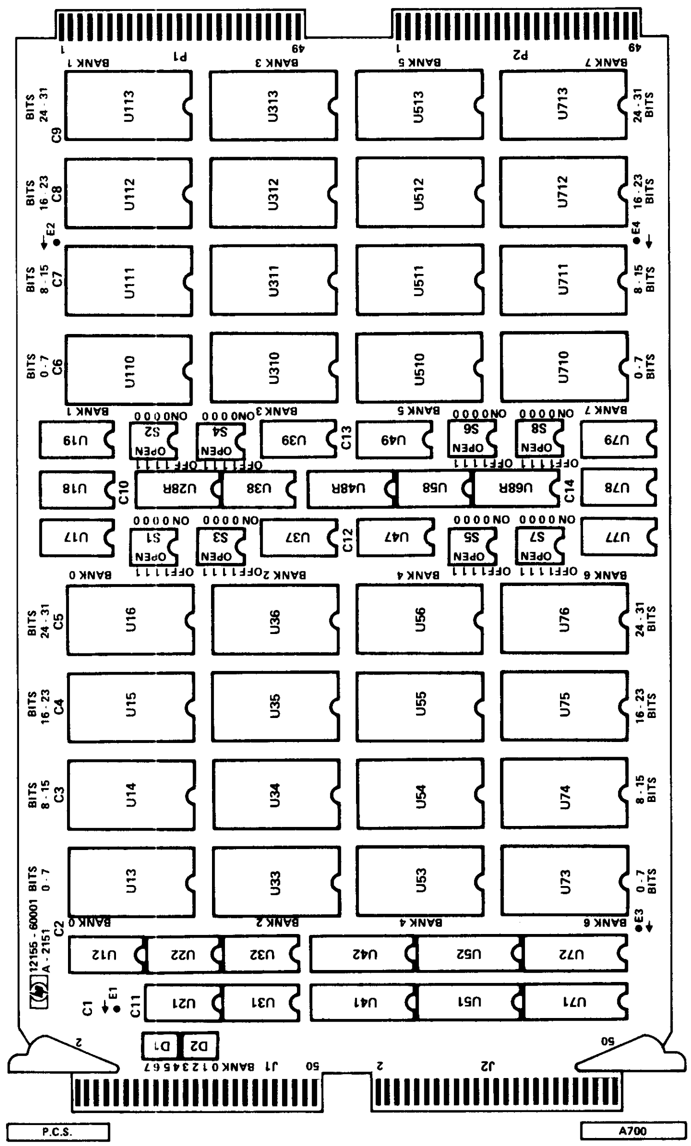


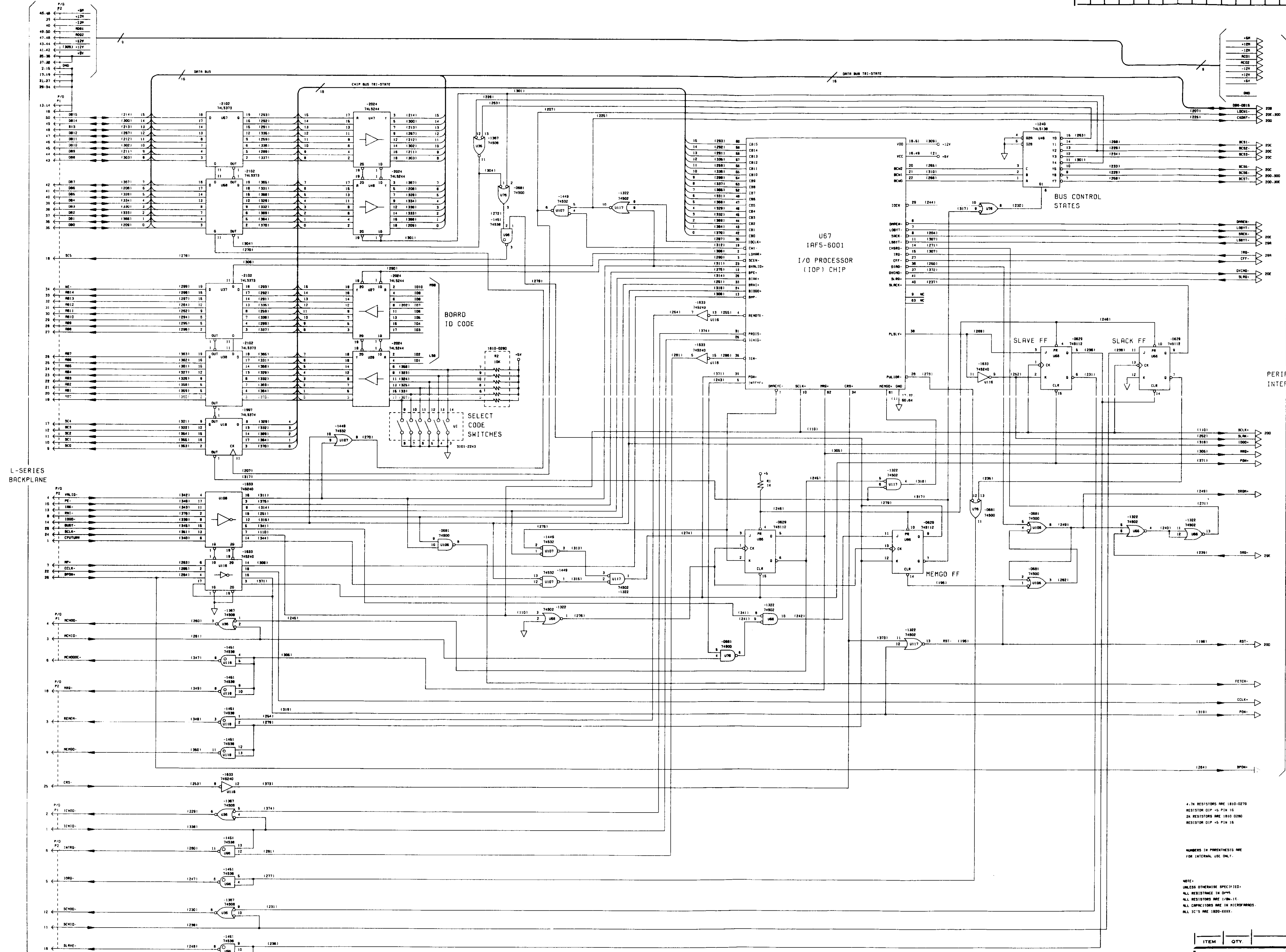
Figure 8-6. HP 12155A Card Parts Locations

Table 8-3. HP 12155A Card Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12155-60001	4	1	PROM CONTROL STR	28480	12155-60001
C1	0160-4832	4	14	CAPACITOR-FXD .01 UF	28480	0160-4832
C2	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C3	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C4	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C5	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C6	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C7	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C8	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C9	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C10	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C11	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C12	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C13	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
C14	0160-4832	4		CAPACITOR-FXD .01 UF	28480	0160-4832
D1	1990-0652	8	2	LED-VISIBLE	28480	1990-0652
D2	1990-0652	8		LED-VISIBLE	28480	1990-0652
S1	3101-2461	0	8	SWITCH-5 POSITION	28480	3101-2461
S2	3101-2461	0		SWITCH-5 POSITION	28480	3101-2461
S3	3101-2461	0		SWITCH-5 POSITION	28480	3101-2461
S4	3101-2461	0		SWITCH-5 POSITION	28480	3101-2461
S5	3101-2461	0		SWITCH-5 POSITION	28480	3101-2461
S6	3101-2461	0		SWITCH-5 POSITION	28480	3101-2461
S7	3101-2461	0		SWITCH-5 POSITION	28480	3101-2461
S8	3101-2461	0		SWITCH-5 POSITION	28480	3101-2461
U12	1820-1200	5	2	IC INV TTL LS HEX	01295	SN74LS05N
U17	1820-1211	8	8	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U18	1820-1275	4	5	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U19	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U21	1820-1200	5		IC INV TTL LS HEX	01295	SN74LS05N
U22	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U28R	1810-0424	2	3	RESISTIVE NETWORK-DIP	11236	761-1-R4.7K
U31	1820-0681	4	1	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U32	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U37	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U38	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U39	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U41	1820-1624	7	6	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U42	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U47	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U48R	1810-0424	2		RESISTIVE NETWORK-DIP	11236	761-1-R4.7K
U49	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U51	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U52	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U58	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U68R	1810-0424	2		RESISTIVE NETWORK-DIP	11236	761-1-R4.7K
U71	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U72	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U77	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U78	1820-1275	4		IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U79	1820-1211	8		IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N

D-12153-60001-51

SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	...TURN - ADD 8 FCLK - DELETE		
C	...EVGO 8 BPON+ (IOMASTERVERSION H)		



4.7K RESISTORS ARE 1810-0279
RESISTOR DIP +5 PIN 16
2K RESISTORS ARE 1810 0280
RESISTOR DIP +5 PIN 16

NUMBERS IN PARENTHESIS ARE FOR INTERNAL USE ONLY.

NOTE:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS
ALL RESISTORS ARE 1/8W.1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

ITEM	QTY.	MATERIAL-DESCRIPTION	MAT'L-PART NO.	MAT'L-DWG. NO.	MAT'L-SPEC.

DRAWN BY: 12-23-81
ENGINEER: 9-28-81
RELEASE TO PROD.
SUPERSEDES DWG

TITLE: A700 WCS CARD

NEXT ASSEMBLY
FINISH —
SCALE —

HEWLETT PACKARD

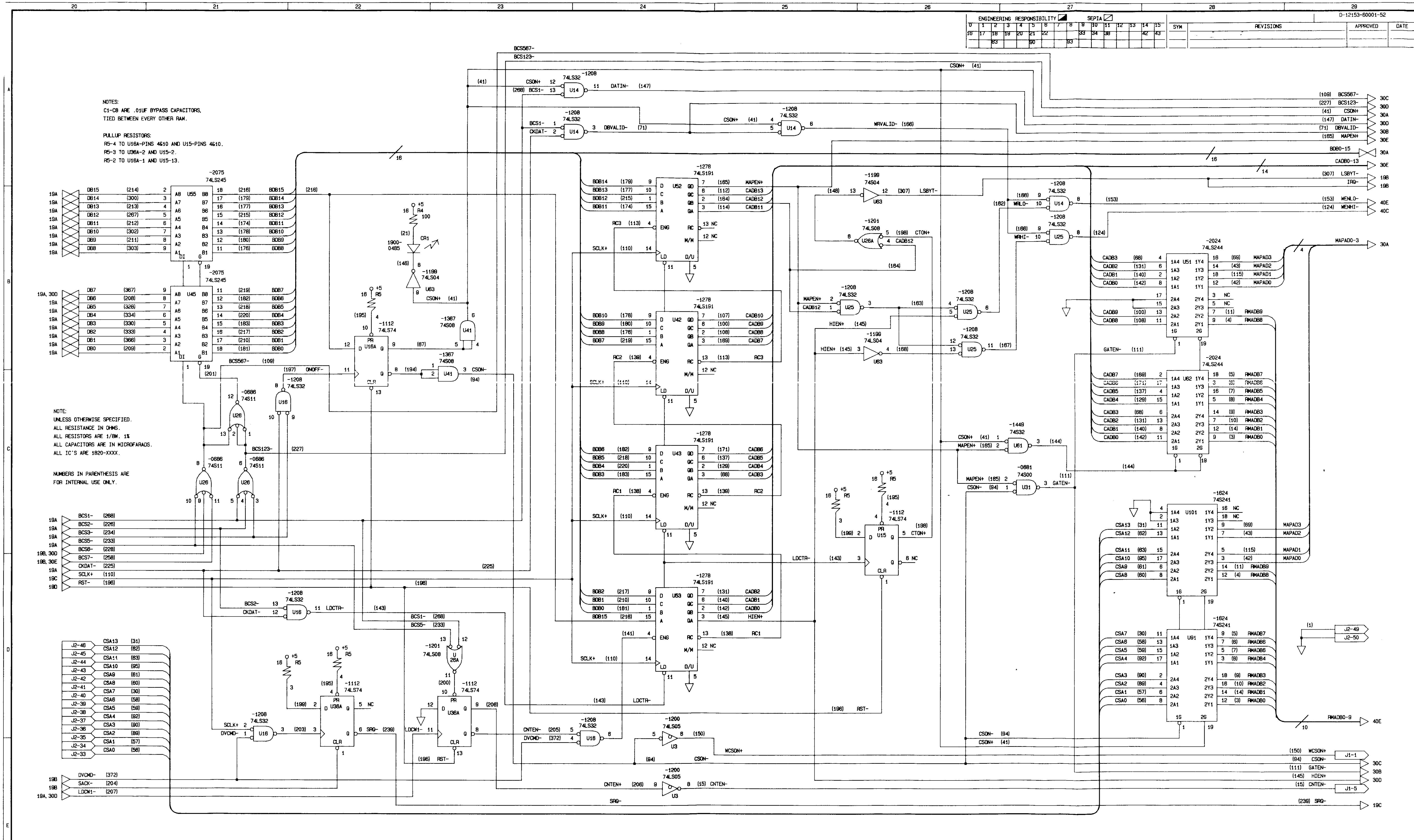
PART NUMBER 12153-60001

D-12153-60001-51

SHEET 1 OF 4

1

STOCK NO. 9280-0004 PRINTED ON DIEPO NO. 1020-10 CLEARPRINT FADEOUT



2

DRAWN BY	DATE 1/26/82
ENGINEER	9/28/81
RELEASE TO PROD	
SUPERSEDES DWG.	

TITLE: A700 WCS CARD

NEXT ASSEMBLY

SHEET 2 OF 4

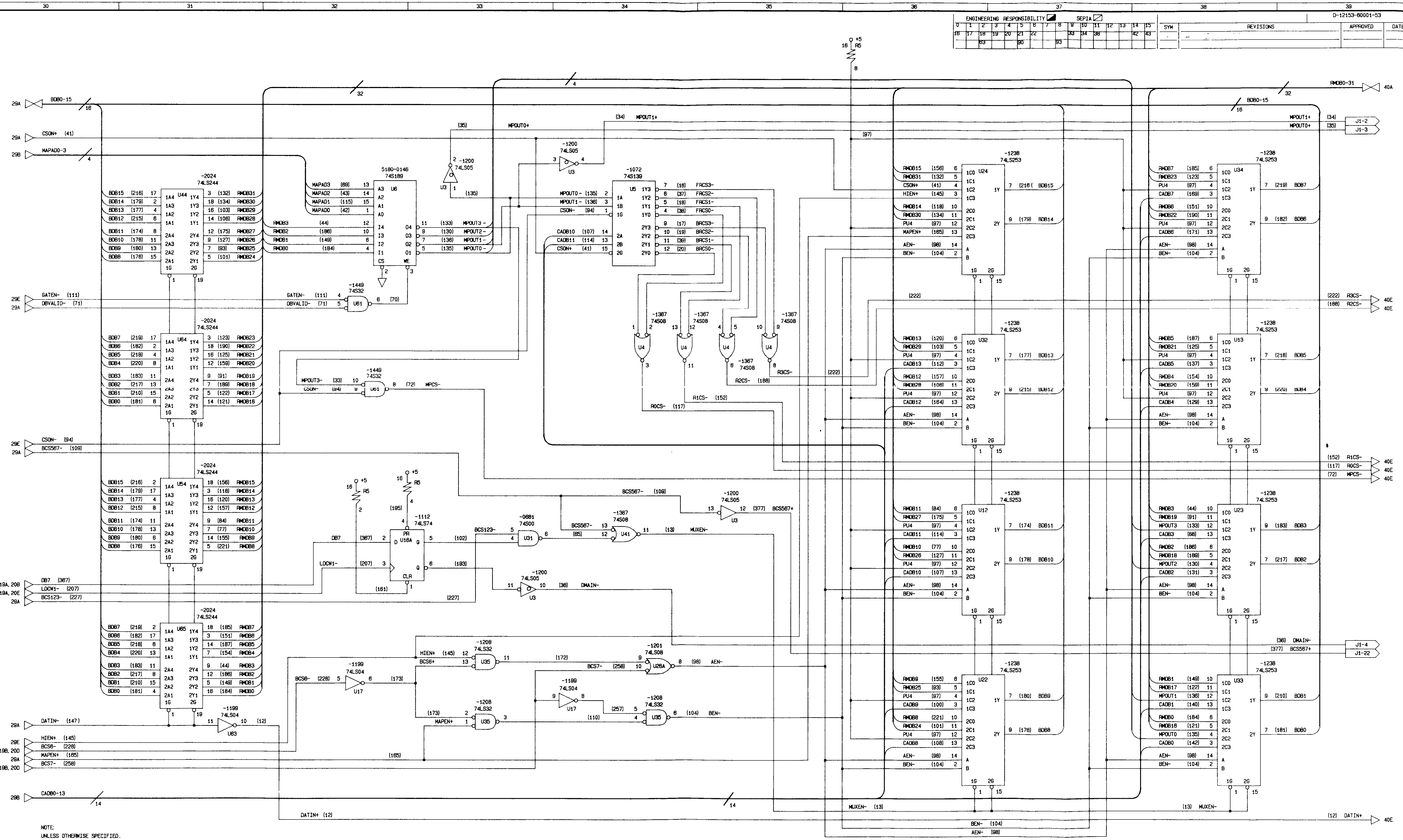
HEWLETT PACKARD

PART NUMBER 12153-60001

D-12153-60001-52

D-12153-60001-53

ENGINEERING RESPONSIBILITY	SEPIA	SYM	REVISIONS	APPROVED	DATE

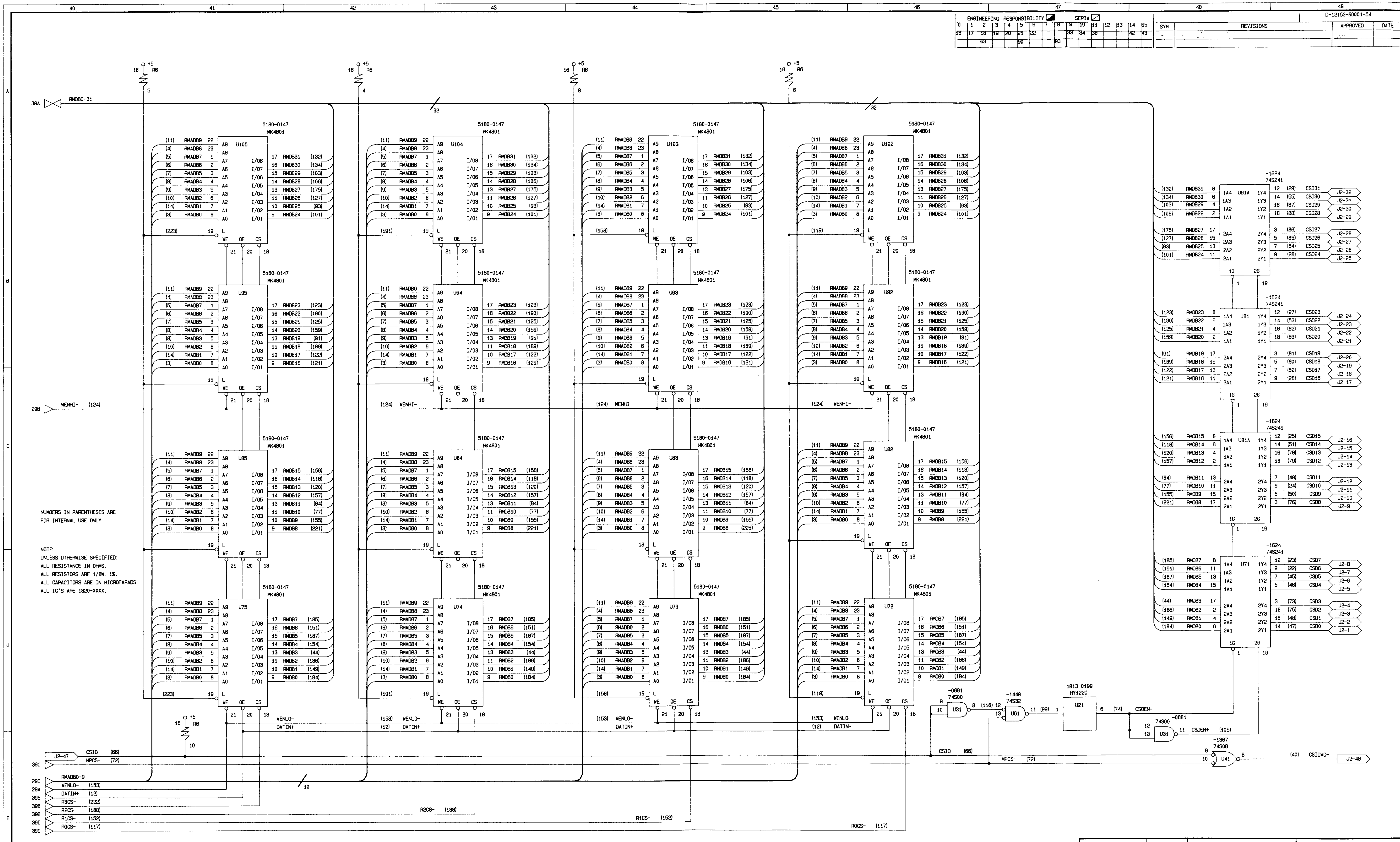


NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.

3

DRAWN BY	DATE 2/5/82	TITLE A700 WCS CARD	HEWLETT PACKARD
ENGINEER	9/28/81		PART NUMBER 12153-60001
RELEASE TO PROD		NEXT ASSEMBLY	D-12153-60001-53
SUPERSEDES DWG.		SHEET 3 OF 4	



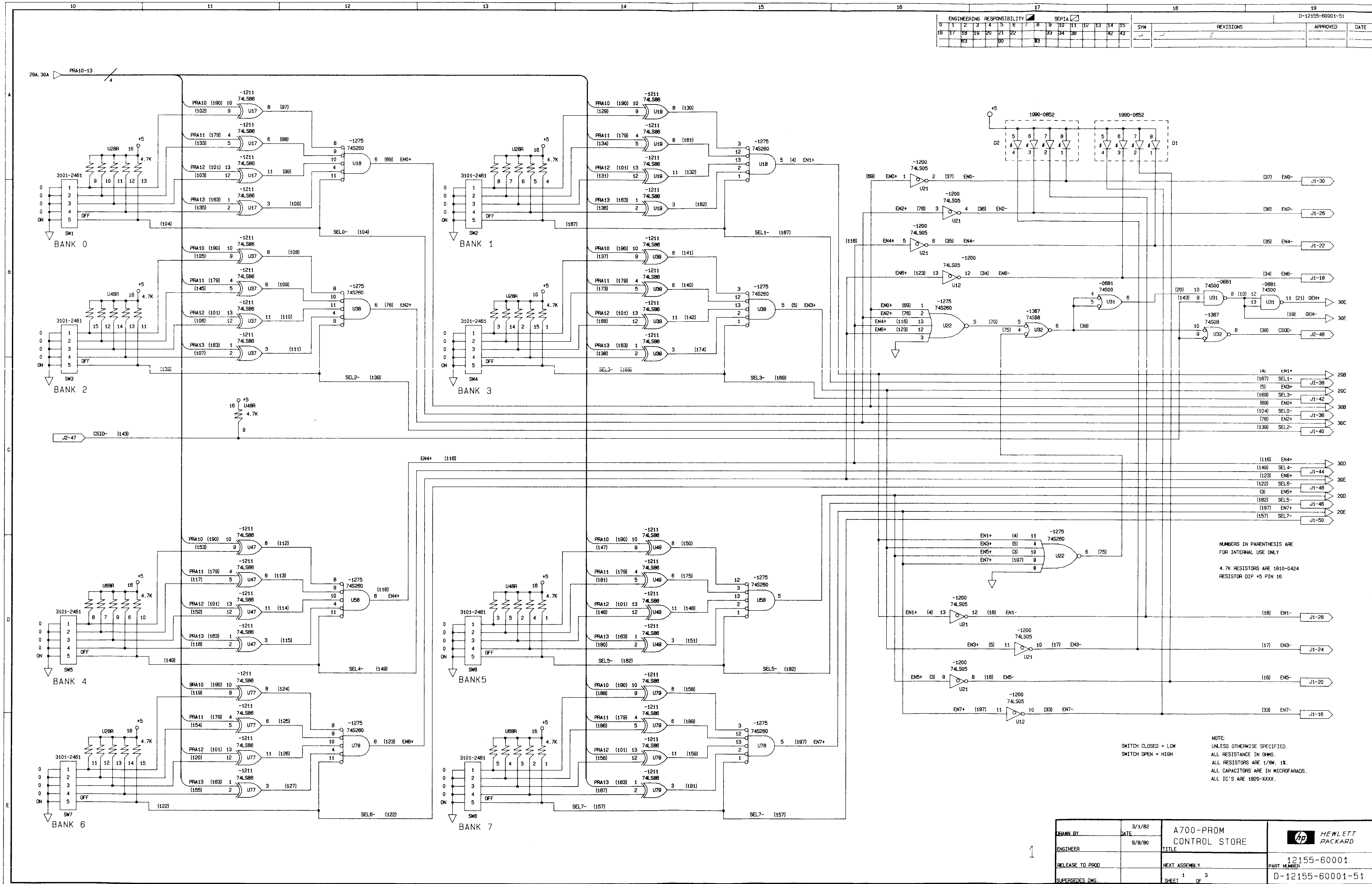
NUMBERS IN PARENTHESES ARE FOR INTERNAL USE ONLY.

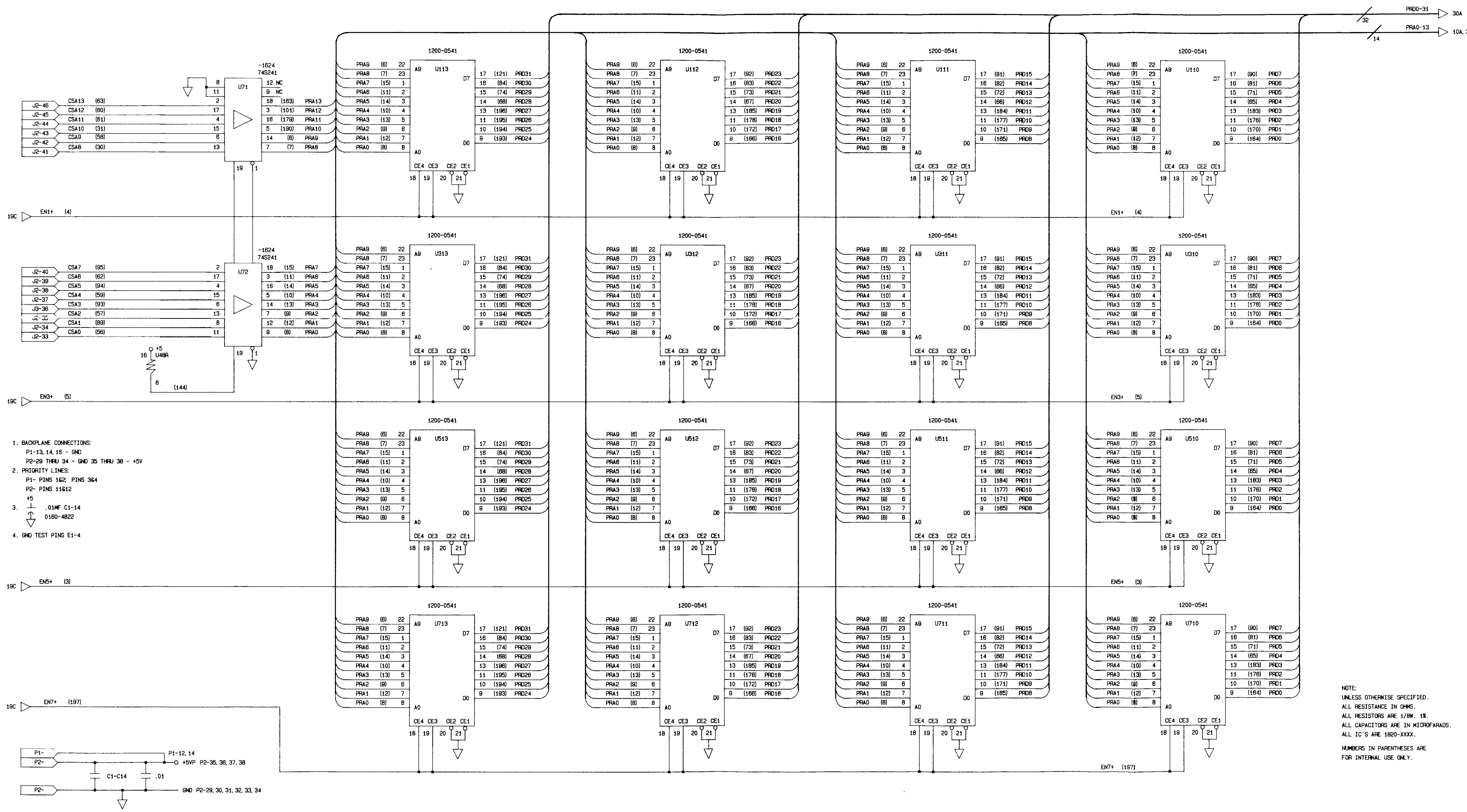
NOTE:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W, 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

DRAWN BY	DATE 1/8/82	TITLE A700 WCS CARD	HEWLETT PACKARD
ENGINEER	9/28/81		12153-60001
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER D-12153-60001-54
SUPERSEDES DWG.		SHEET 4 OF 4	

D-12153-60001-54

4


D-12155-60001-51
BANK 0
BANK 1
BANK 2
BANK 3
BANK 4
BANK5
BANK 6
BANK 7
NUMBERS IN PARENTHESIS ARE
FOR INTERNAL USE ONLY
4.7K RESISTORS ARE 1810-0424
RESISTOR DIP +5 PIN 16
SWITCH CLOSED = LOW
SWITCH OPEN = HIGH
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.
A700-PROM
CONTROL STORE
HEWLETT PACKARD
12155-60001
D-12155-60001-51
SHEET 1 OF 3



1. BACKPLANE CONNECTIONS:
   P1-13, 14, 16 - GND
   P2-29 THRU 34 - GND 35 THRU 38 - +5V
2. PRIORITY LINES:
   P1- PINS 1&2; PINS 3&4
   P2- PINS 11&12
3. +5 .01MF C1-14 0160-4822
4. GND TEST PINS E1-4

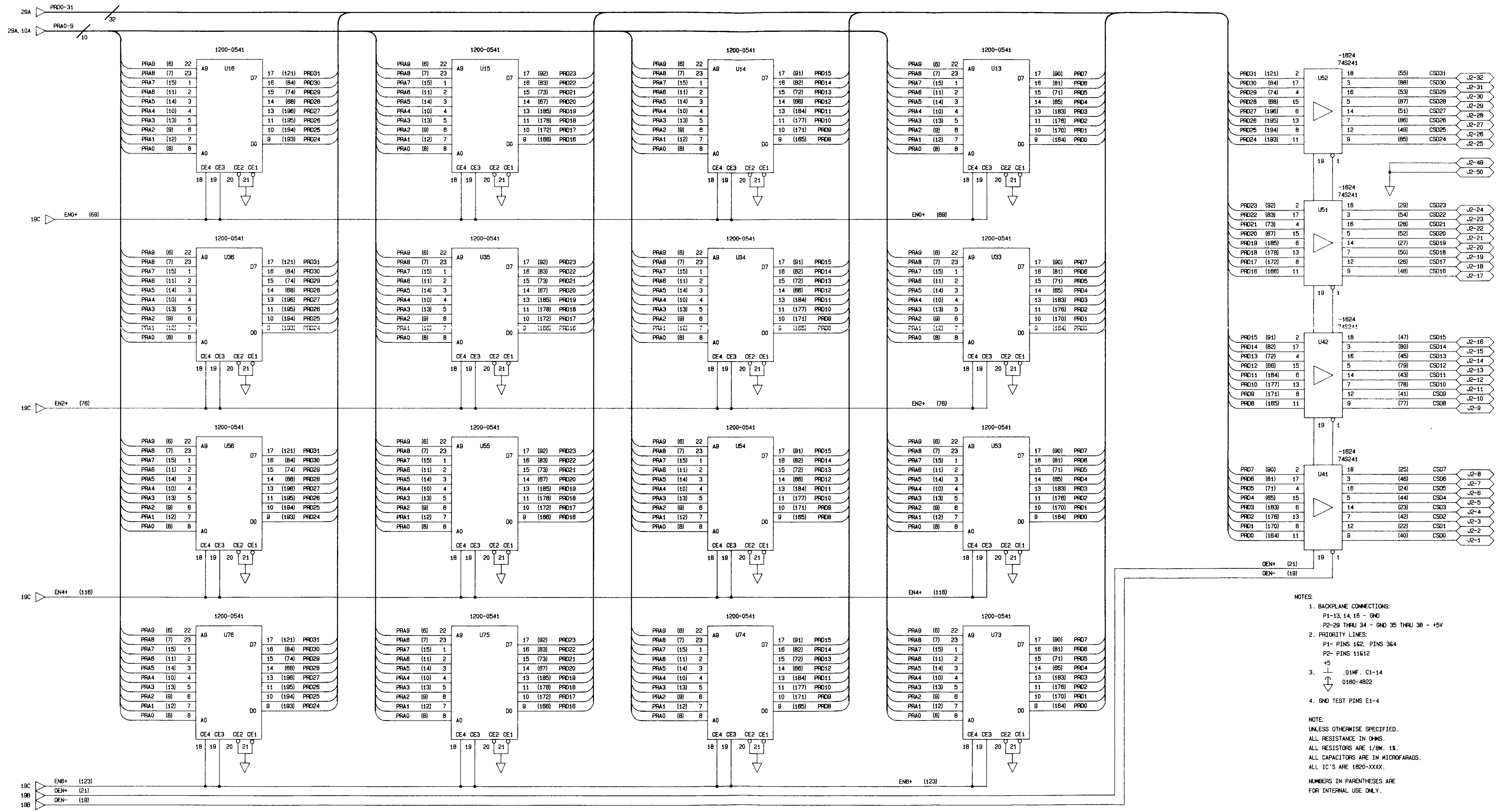
NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.

DRAWN BY	2/17/82 DATE	A700 - PROM CONTROL STORE	HEWLETT PACKARD
ENGINEER	9/8/80	TITLE	12155-60001
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER
SUPERSEDES DWG.		SHEET 2 OF 3	D-12155-60001-52

2

D-12155-60001-53



NOTES:

1. BACKPLANE CONNECTIONS:
   P1-13, 14, 16 - GND
   P2-29 THRU 34 - GND 35 THRU 38 - +5V
2. PRIORITY LINES:
   P1- PINS 1&2; PINS 3&4
   P2- PINS 11&12
3. +5 .01MF. C1-14 0160-4822
4. GND TEST PINS E1-4

NOTE:
UNLESS OTHERWISE SPECIFIED.
ALL RESISTANCE IN OHMS.
ALL RESISTORS ARE 1/8W. 1%.
ALL CAPACITORS ARE IN MICROFARADS.
ALL IC'S ARE 1820-XXXX.

NUMBERS IN PARENTHESES ARE
FOR INTERNAL USE ONLY.

3

DRAWN BY	DATE 2/16/82	TITLE A700 - PROM CONTROL STORE	HEWLETT PACKARD
ENGINEER	9/8/80		
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER 12155-60001
SUPERSEDES DWG.		SHEET 3 OF 3	D-12155-60001-53

9.1 INTRODUCTION

This section describes the internal characteristics of the HP 12156A Floating Point Processor (FPP) card for the A700 computer. The paragraphs under 9.2 describe the general operation and capabilities of the card, and the paragraphs under 9.3 is the theory of operation of the floating point card. This includes the interface to the floating point chips, the interface to the micromachine, the control logic on the card, and the on-card operand storage capability. The general frontplane and backplane interface requirements are contained in paragraphs under 9.4 and paragraphs under 9.5 describes the logic associated with the on-card firmware which contains the microcode for floating point intensive routines.

The HP 12156A Floating Point Processor (FPP) consists of three floating-point chips which implement the HP 1000 floating-point format, control logic to interface the card to the processor, on-card RAM and ROM for storage of operands, and 4k of microcode address space (expandable to 8k when higher density ROMs are available).

The power requirements for the FPP card are covered in Table 1-1 of Section I of this manual.

9.1.1 PHYSICAL CHARACTERISTICS

The FPP card is installed into the system backplane between the upper processor card and the lower processor card. A frontplane connector is used to connect the floating point card, the processor cards, the memory controller card, and the WCS or PCS cards together in the system. It has two 50-pin edge connectors that plug into the backplane, and one 160-pin connector to connect to the memory frontplane.

The signals and data of the card are Schottky-TTL levels and comply with Schottky-TTL design rules. The HP 12156A FPP card is shown in Figure 9-1.

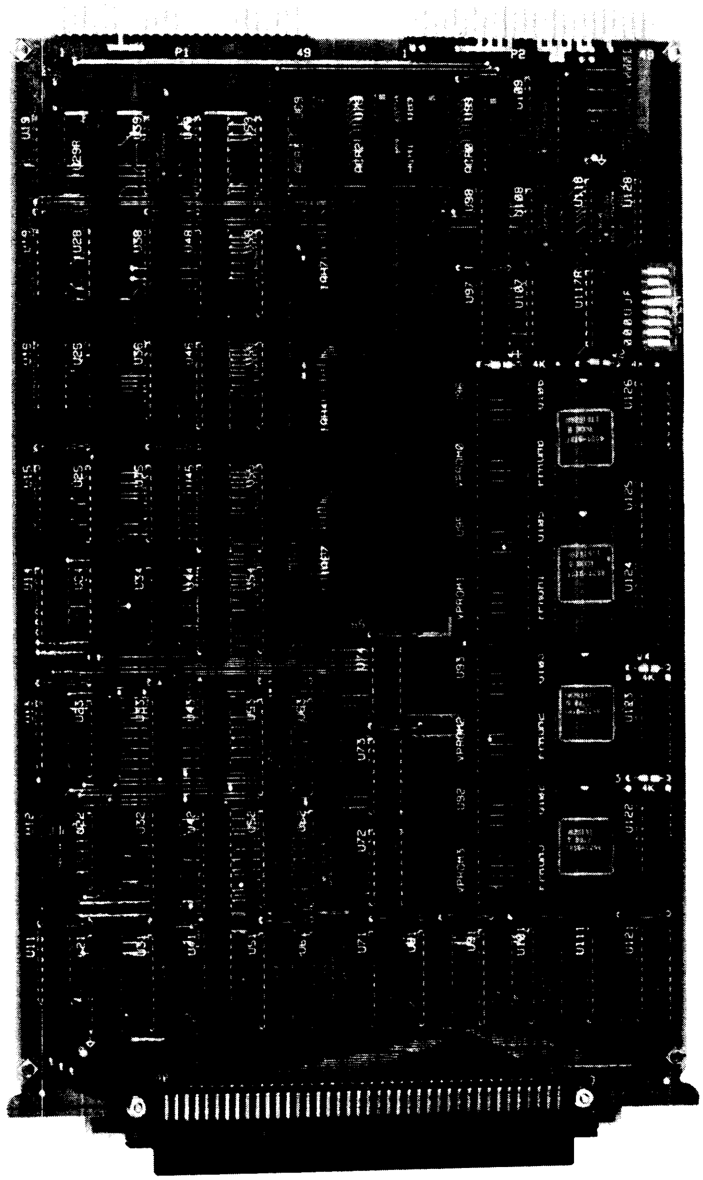


Figure 9-1. Floating Point Processor Card (12156-60001)

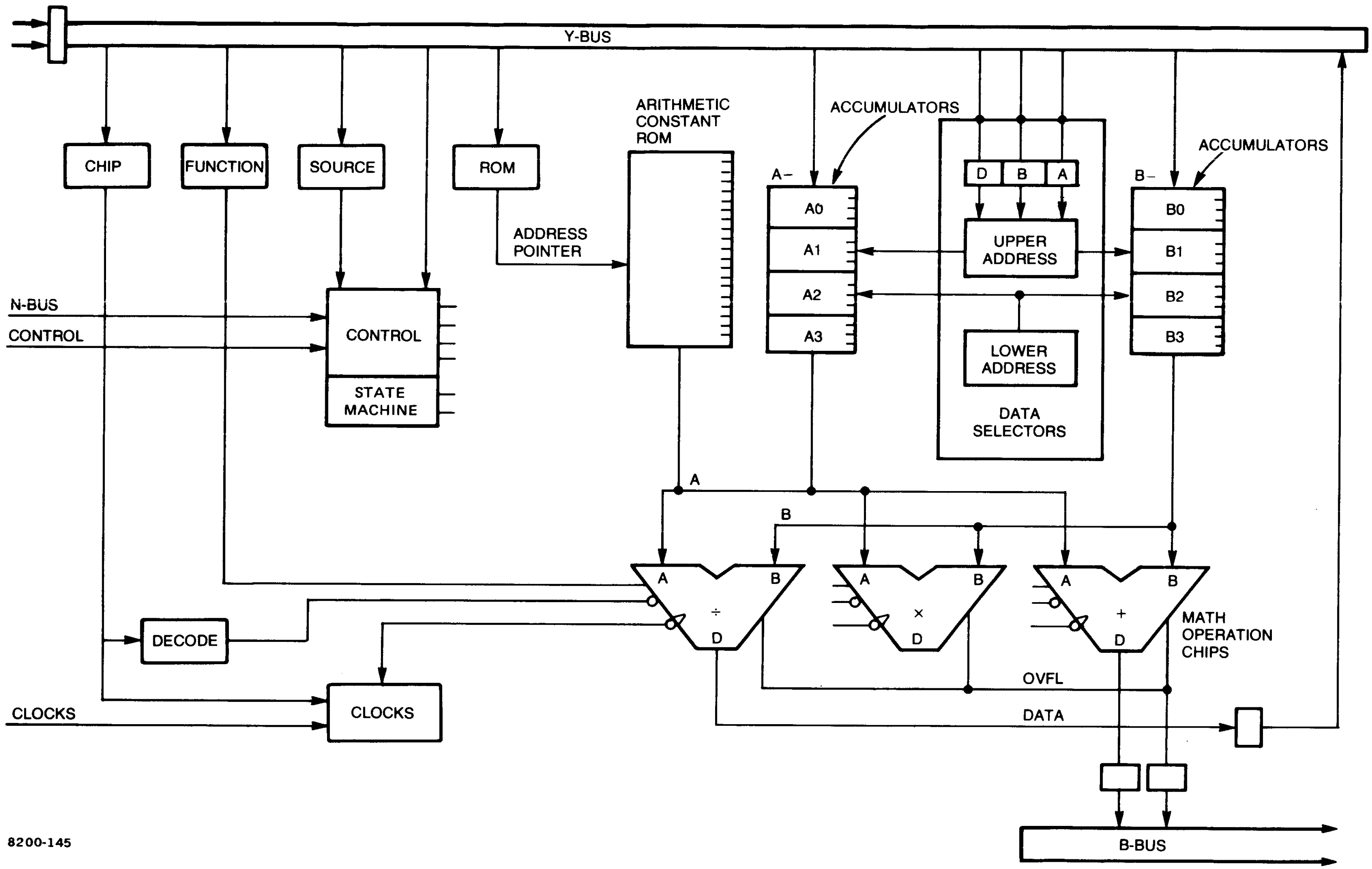


Figure 9-2. Floating Point Processor Block Diagram

9.2 OPERATING CHARACTERISTICS

The FPP is used to accelerate the execution of floating-point dependent macroinstructions and provide floating-point microprogramming capability. These macroinstructions include the basic single- and double-precision floating-point instructions, the SIS instructions, and the VIS instructions. It contains four accumulator locations, ROM for storage of 512 arithmetic constants, 4k-words of microcode address space, and logic to interface to the processor. The following paragraphs describe the overall operation of the card. The block diagram to use with this description is provided in Figure 9-2.

9.2.1 BASIC CAPABILITIES

The floating point card interfaces to the processor cards over the frontplane and can accept control words and operands over the Y-bus, perform operations on the operands, and return the results to the micromachine over the B-bus.

In operation, a control word is first passed to the card. This control word contains the information described in Control Word of Register SRIN-E, paragraph 9.3.1.1. Once a control word is passed to the FPP card, the card accepts the necessary operands and then performs the requested function. After a required propagation delay the result of the operation can be read from the card.

See Figure 9-3 for the FPP internal data paths. An on-card scratch RAM contains four 64-bit accumulators. The accumulators are included to eliminate the necessity of repeatedly passing the same floating point number to the card from the processor when it is required more than once (e.g., when calculating (1+x)/(1-x)). The accumulators also reduce the overhead required in temporarily saving the intermediate results of a polynomial expression. The ability to save intermediate results on the card (versus unloading and later reloading the value) can significantly reduce the execution time of the SIS and VIS instruction sets.

An on-card Arithmetic Constant ROM (ACR) contains up to 256 constants used in evaluating the SIS instructions. The ACR on the card is accessed indirectly through an address pointer. The ACR address pointer is automatically incremented after each use, allowing the address pointer to be set to the front of a list of constants which are to be required in a known order. The ACR eliminates the overhead required to pass fixed-valued operands (e.g., pi, pi/4, 1, 1/2, etc.) from the processor to the floating point card. These savings are most significant in the evaluation of the SIS instructions where many constants are required in the polynomial approximation of the functions.

If A or B operands are required from the processor they are passed to the card with the most-significant-word first. All numbers passed to the floating point card are stored in an accumulator. As the operands required for the operation are available on the card they are clocked into the floating point chips.

At the completion of an operation, the results can either be stored in an accumulator, or be returned to the processor over the B-bus, or both. An error/status condition word is also available and is used to determine whether an overflow or underflow occurred during the last operation.

9.3 FPP THEORY OF OPERATION

The HP 12156A Floating Point Processor card theory of operation is covered in the following paragraphs. Use Figure 9-2 and to schematic at the rear of this section of the manual. The integrated circuits (chips) are referenced by their U-numbers and schematic locations. For example, U69 (13-C) means chip U69 on schematic sheet no. 1 is located by coordinates 13 and C; where the horizontal grid on sheet no. 1 is numbered 10, 11, etc. and on sheet no. 2 it is numbered 20, 21, etc.

9.3.1 INTERFACE TO MICROMACHINE

The A700 micromachine has three 16-word register files: PRIN, GRIN, and SRIN. These files are addressed indirectly through the index register N. Communication between the micromachine and the floating point card occurs through the four registers SRIN-C through SRIN-F that are located on the FPP card. The other SRIN registers are located on the memory controller card.

The N-bus goes to the floating point card over the frontplane from the lower processor card. The four bits on the N-bus are input to two type-74S138 decoders to generate four address signals for writing and four address signals for reading of the FPP SRIN registers. Decoder U72 (11-C) is for writes, and U73 (11-C) is for reads. Two additional signals from the frontplane FP_LYSRIN- and FP_ESRINB- are asserted by the processor to distinguish between the reads and writes to the SRIN register file by enabling either U72 or U73 as appropriate.

The four SRIN locations used by the floating point card are used for the following purposes.

SRIN WRITE

F Used for loading the address pointer to the arithmetic constant ROM (ACR), and is used to accept special divide control words.

E The register that stores the main control word which is passed to the card.

D Accepts the operand when only one operand is passed to the card, or accepts the a-side operand when two operands are passed to the card.

C Accepts the b-side operand when two operands are passed to the card.

READ

F Used to read the result when the result must not be saved in an on-card accumulator.

E Used to read the result when the result is also to be saved in an on-card accumulator.

D Used to return the overflow/underflow indication from the floating point chips.

C Used for diagnostic purposes and returns what was last stored to SRIN-E in bit reversed form.

All data going into the FPP card is buffered and latched from the Y-bus by U21 (11-A) and U31 (11-B). The data is then clocked into its final destination which is determined by decoding the N-bus.

When data is read from the floating point card it is driven onto the B-bus by one of three pairs of drivers. If the information is the result of an operation, U51 (28-C), and U61(28-C) drive the B-bus. If the overflow/underflow bits are being returned, U52 (28-D) and U62 (28-D) drive the B-bus. If the diagnostic SRIN location is being read, U32 (27-D) and U42 (27-E) drive the B-bus.

9.3.1.1 Control Word of Register SRIN-E

When starting a floating point operation a control word is first passed to the floating point card by storing to register SRIN-E. The format of the control word and the information contained in its fields is shown below:

SRIN-E

15 14	13 12 11 10 9	8 7 6	5 4	3 2	1 0
CHIP	FUNCTION	SOURCE	D-ADDR	B-ADDR	A-ADDR

The CHIP field contains two bits which are used to determine which one of the three floating-point chips is to be selected as follows:

CHIP FIELD

BIT		CHIP SELECTED
00	-	select 1AE7
01	-	select 1AH4
10	-	select 1AH7
11	-	unused

The CHIP field information is latched in U22 (12-A) on the rising edge of PC- on a write to SRIN-E. The two signals FLCHP1+ and FLCHP2+ generate FLCHP0-, FLCHP1-, and FLCHP2- that enable the floating point chips 1AE7, 1AH4, and 1AH7, respectively. These two signals also are used as enable lines determining which of these chips is to receive a clock pulse.

The FUNCTION field contains the five-bit function opcode which is presented to the three floating-point chips. These opcodes and the operation performed by these chips are listed in Table 9-1.

The five-bit function OPCODE is latched in U23 (18-A) on the rising edge of PC- on a write to SRIN-E or -F. This information is then presented to all three floating point chips after passing through OR gates U33 (18-B) and U43 (18-B). The second input to the OR gates becomes asserted at the end of an operation when the results are being read from the chips. The OR-gates allow a next_out the results are being read from the chips. The OR-gates allow a next_out chip opcode (an all ones pattern) to be presented to the math chips to extract the results from the chips. This forced pattern occurs on all reads from SRIN-E or -F.

The SOURCE field selects to source for the a-side and b-side operands. The a-side operand can come from one of three places; the scratch RAM (accumulator), the constant ROM, or from the Y-bus. The b-side operand source can come from either an accumulator (RAM) or from the Y-bus.

The three-bit SOURCE field is decoded to produce the source signals for the a-side operand and the b-side operand in six possible combinations of the above sources. The decoding results of the SOURCE field are given in Table 9-2.

Table 9-1. FPP Control Word FUNCTION Field

OP CODE	F A S CHIP FUNCTION		
F	1AE7	1AH4	1AH7
0XXXX	clear	clear	clear
10000	-	-	-
10001	ft.i1.f4	-	qbit2
10010	ft.i2.f2	-	qbit3
10011	ft.i2.f4	-	-
10100	cv.f4.f2	mul.i2	div.i2
10101	-	mul.l2	div.l2
10110	fx.f4.i1	mul.f2	div.f2
10111	fx.f4.i2	mul.f4	div.f4
11000	add.f2	-	divsetup
11001	sab.f2	-	-
11010	add.f4	-	-
11011	sab.f4	-	-
11100	shr.i4	-	-
11101	shl.i4	-	-
11110	-	-	-
11111	next_out	next_out	next_out

f2 = single precision floating point
f4 = double precision floating point
i1 = single integer, i2 = double integer
l2 = two word logical (unsigned)

Table 9-2. FPP Control Word SOURCE Field

SOURCE BITS	SOURCE FIELD
000	a-side operand from Y-bus, b-side from Y-bus
001	a-side operand from Y-bus, b-side from RAM
010	a-side operand from RAM, b-side from Y-bus
011	a-side operand from RAM, b-side from RAM
100	not used
101	not used
110	a-side operand from ROM, b-side from Y-bus
111	a-side operand from ROM, b-side from RAM

The source information is latched in U22 (12-A,B) on the rising edge of PC- on a write to SRIN-E. This information is then fed to U12 (12-C), a Programmable Arithmetic Logic (PAL) chip which contains the state machine for the card. The signal FLROM from U22 enables the Arithmetic Constant ROM and disables the a-side scratch RAM.

The A-ADDR field is used as an address to select the location in the accumulator (scratch RAM) where the a-side operand is to comes from. If the a-side operand comes from ROM, the contents of this field have no effect.

The B-ADDR field is used as an address to select the location in the accumulator RAM where the b-side operand is to come from.

The D-ADDR field is used as an address to select the location in the accumulator RAM where the result is to be stored. The result is stored in RAM when a read from SRIN-E is performed. If the results are not to be stored into RAM then the results must be read from SRIN-F.

The ADDR field information is latched in U34 (14-A) at the rising edge of PC- on a write to SRIN-E. The outputs of this latch feed upper address selectors U25 (15-B) and U35 (14-B). U35 selects addresses for a-side accumulators, while U25 selects addresses for the b-side accumulators.

When an a-side operand is stored in an accumulator, both selectors present the address of the A-ADDR field to its accumulator file. When a b-side operand is stored in an accumulator, both selectors present the address of the B-ADDR field to its accumulator file. This ensures that the a-side and b-side accumulators always receive the same "write" address and therefore contain the same data.

When operands are to be read from the accumulators, the a-side selector presents the A-ADDR address to its accumulator and the b-side selector presents the B-ADDR address to its accumulator.

When the results of an operation are being written in the accumulator, both selectors, a-side and b-side, present the address of the D-ADDR field to its accumulator. The address selector output control bits and the resultant accumulators are shown in Table 9-3.

Table 9-3. FPP Control Word Address Fields

A-ADDR, B-ADDR, D-ADDR FIELD DATA SELECTION	
ADDRESS BITS	ACCUMULATOR SELECTED
00	accumulator 0
01	accumulator 1
10	accumulator 2
11	accumulator 3

9.3.1.2 Transfer of Control Word at SRIN-F

The control word passed to the card at SRIN-F has two primary uses. The first function is to access the ACR (Arithmetic Constant ROM) for the purpose of loading the control word. For ACR access the ROM address pointer must first set to the desired value. The second function of the SRIN-F control word is to apply a specific function opcode and one clock pulse to the floating point chips. This feature is used in assisting the divide operation which requires a sequence of function opcodes.

The SRIN-F control word contains the information in the fields shown below:

CONTROL WORD AT SRIN-F

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
L	C	FUNCTION						ACR ADDRESS							

The L-field determines if the address in the ACR field is to be loaded into the ACR address pointer counters. If this bit is set on a store to SRIN-F, the value in the ACR field is loaded into the address counter.

The C-field is used to indicate that the function opcode should be clocked into the floating point chip. This bit of information is clocked into flip-flop U41-2 (15-A) on the rising edge of PC- on a write to SRIN-F. The output of this flip-flop, FLCBITL, forces FL1CK high which causes FLMIDL to generate one clock pulse for the selected floating point chip.

The C-field and SRIN-F FUNCTION field are used primarily to direct the sequencing of the function opcodes required to control the divide operations of the floating point divide chip. When a store to SRIN-F is performed with the C-bit set, the contents of the FUNCTION field will be clocked into the selected floating point chip. This allows any sequence of opcodes to be presented to the chips.

The FUNCTION field contains the five-bit function opcode which is presented to the three floating point chips. This field is the same as the FUNCTION field of the control word at SRIN-E. This five bits of information is latched into U23 (18-A) on the rising edge of PC- on a write to SRIN-E or SRIN-F.

The ACR field contains the data to be stored into the ACR address pointer. This information is latched into two up counters, U49 (16-A) and U59 (17-A), on the rising edge of PC- on a write to SRIN-F that also has the bit in the L-field set high.

The eight bits of the ACR field contain the starting address of the next constant in the ACR to be accessed. The ACR consists of four 512 x 4-bit PROMs U69, U79, U89, U99 (25-E, 25-E, 25-D, and 25-D).

Each PROM has nine address lines. The ACR field containing the high eight bits of the PROM address. The low bit of the PROM address is generated by flip-flop U39-5 (17-B). This flip-flop is cleared on all writes to SRIN-E or -F, and is clocked (toggled) whenever a floating point chip receives a clock pulse.

The eight-bit ACR counter is clocked on the rising edge of PC- when both U38-8 (16-B) and U28-3 (13-C) are high. U38-8 is high when the ACR is the source for the a-side operand (FLROM high) and a read from SRIN-E or -F is not occurring. U28-3 is high when either FP_CK2 is asserted (as when both operands are on the floating card), or when RCK is asserted (RCK is asserted for one microcycle after a write to SRIN-D if the low bit of the ACR address had been a high, as when a double precision operand is passed to the card).

9.3.1.3 Transfer of Operands to the FPP

After a control word has been passed to the card at SRIN-F the logic in the PAL chip U12 (12-C) controls the flow of the input operands, determining which operands to accept from the Y-bus and which operands are to come from the FPP card RAM and ROM. When operands are passed to the floating point card they are always stored in an accumulator.

The accumulators on the floating point card appear to the microprogrammer as four-word files of 64-bits each. They are organized as dual port, four-word by 64-bit register files. Physically, there are two sets of four RAMs each made up of U44 - U48 (23-B, -C, and -D) and U54 - U58 (22-B, -C, and -D). These are 16 x 4 bit RAMs that are organized to be two 16 x 16 register files.

Each 64-bit accumulator file has four locations and four address lines. The upper two address lines select one of four accumulators. The lower two address lines select a 16-bit fraction of the 64-bit accumulator file.

There are three possible accumulator addresses (upper two address lines) associated with one operation; the a-side address (FLAU0 and FLAU1), the b-side address (FLBU0 and FLBU1), and the result address (FLDU0 and FLDU1). The two address selector chips, U25 and U35 (15-B and 14-B), determine which of the addresses to present to the a- and b-side register files during all phases of an operation.

There are four separate fraction addresses (lower two address lines) associated with one operation; the address of the fraction of the a-side operand being passed to the card (FLLA0 and FLLA1), the address of the fraction of the b-side operand being passed to the card (FLLB0 and FLLB1), the address of the fraction of the pair of operands being clocked into the floating point chips (FLLC0 and FLLC1), and the address of the fraction of the result being saved in an accumulator (FLLD0 and FLLD1).

Each of four two-bit counters U26 (16-C), U16 (16-C), and a J-K flip-flop U39-9 (17-C) provide the four lower-fraction addresses by counting input pulses from the operand read control signals (e.g., the FLWA and FLWB outputs of PAL chip U12). Each counter keeps tract of its fraction address and increments to the next fraction address when required.

The counters outputs are passed to address selector U36 (16-C) that generates the lower address signals FLL0 and FLL1 that pass through the a-side and b-side address buses to the register-file address lines.

When both operands are to come from the micromachine over the Y-bus, the card accepts the data that was stored to SRIN-D as the a-side operand and the data that was stored to SRIN-C as the b-side operand. When only one operand is required from the Y-bus (the other operand comes from RAM or ROM) the operand must be passed through location SRIN-D regardless of whether the operand is an a-side or b-side operand. The control logic of the programmable arithmetic logic chip U12 (12-C) monitors the SOURCE field and all writes to SRIN-C, -D, and -E, and asserts FLWA- when an a-side operand is being passed to the card, or asserts FLWB- when a b-side operand is being passed to the card. At the same time the lower address a-side or b-side counter is incremented, respectively.

The expressions for FLWA and FLWB generated inside U12 (12-C) are:

FLWA- = FLS1- * FLWD-
FLWB- = (FLS0- * FLS1- * FLWC-) + (FLS0- * FLS1 * FLWD-)

When an a-side operand is passed to the card it is stored in both RAM register files at the address specified by the A-ADDR field of the control word. Selector U35 (14-B) determines the upper accumulator address (signals FLUA0 and FLUA1) for the a-side register file by selecting the FLAU0 and FLAU1 signals on its C3 inputs for passing to the a-side RAMs. (The b-side and d-address lines also input to U35 inputs for read addressing.)

Similarily, selector U25 (15-B) determines the upper accumulator address for the b-side register file, will also select FLAU0 and FLAU1 to pass to the b-side register file RAMs so that both sides get the same accumulator address selected . Also selector U26 (16-C) that determines the fraction address, will also select FLLA0 and FLLA1 to pass to both of the RAM register files. The counter for the FLLA0 and FLLA1 fraction address is then clocked to be ready for the next a-side operand transfer.

When a b-side operand is passed to the card, operation is the same as for the a-side except that b-side address signals are selected so that the operand is stored in the RAM register files at the address specified by the B-ADDR field of the control word. U35 selects signals FLBU0 and FLBU1, and U25 selects FLBU0 and FLBU1 to pass to the b-side register file RAMs. U26 selects FLLB0 and FLLB1 to pass to both RAM register files. The counter for the FLLB0 and FLLB1 fraction address is then clocked to be ready for the next b-side operand transfer.

9.3.1.4 Transfer Of Results

The most significant word of the result is available at the outputs of a floating point chip after a fixed propagation delay after the last function opcode was clocked into the chip. Clocking the function opcode next_out into the chip will allow the next most significant word of the result to be available on the outputs. This is repeated until all words of the result are removed.

When the floating point chips have completed an operation, the result is available to be accessed from either register SRIN-E or SRIN-F. A read from SRIN-E or SRIN-F will assert both FLREF and FLEND from decoder U73 (11-C). These signals enable chips U51 (28-C) and U61 (28-C) to drive the B-bus with the output of the floating point chips, force FL1CK high to generate one clock pulse to floating point chip U66, and force the function opcode presented to the floating point chips to all high "next_out."

When the destination for the result is only the B-bus and not an accumulator, the result must be read from SRIN-F.

When the destination is the B-bus and an accumulator the result must be read from SRIN-E. A read from SRIN-E will assert FLRAMWE from OR gate U74-8 (12-C) enabling data to be written into the addressed accumulator. The buffers U53 and U63 are enabled allowing the output of the chips to be fed to the inputs of the RAM files (the outputs of the latches U21 and U31 are disabled at this time). The signal FLBRE is asserted and causes U25 (15-B) and U35 (14-B) to select FLDU0 and FLDU1 for the accumulator address for both RAM files, and causes U36 (16-C) to select FLLD0 and FLLD1 for the fraction address lines for both RAM files. After the transfer, the fraction address is clocked to the next address.

When the destination is only an accumulator, the data transfer can be performed at two words per microcycle by asserting CK2 during the read from SRIN-E. This asserts FP_CK2 on the frontplane which enables both the floating point chip clocking circuit and the RAM clocking circuit to generate two clock pulses per microcycle.

9.3.1.5 Transfer of Error Conditions

The floating- point chips generate an overflow/underflow indication. These lines, FLER0 and FLER1, are valid from the chips when the result is valid. These lines are latched in U62 (28-D) on the rising edge of PC-. An error condition status word can be read at SRIN-D either before, during, or after reading the result of the operation. A read from SRIN-D enables U52 (28-D) and U62 (28-D) to drive the B-bus with the error word. The most significant bit of this word is read as a one if an overflow or an underflow has occurred (according to the HP1000 floating point format) during the last operation. The bit is cleared if no error has occurred.

9.3.2 FLOATING POINT CHIPS

9.3.2.1 Clocking the Floating-Point Chips

The main computational power of the FPP is contained on three special HP CMOS/SOS chips implementing the HP 1000 floating point format. They are the following: 1AE7 is U65 (24-B,C), 1AH4 is U66 (25-B,C), and 1AH7 is U68 (27-B,C). They have two 16-bit input ports (A and B), a 16-bit output port (D), a five-bit control word (F), a two-bit error condition (ERR), a data output enable (DEN), and a single clock input (CLK). Figure 9-3 shows an external view of the chip.

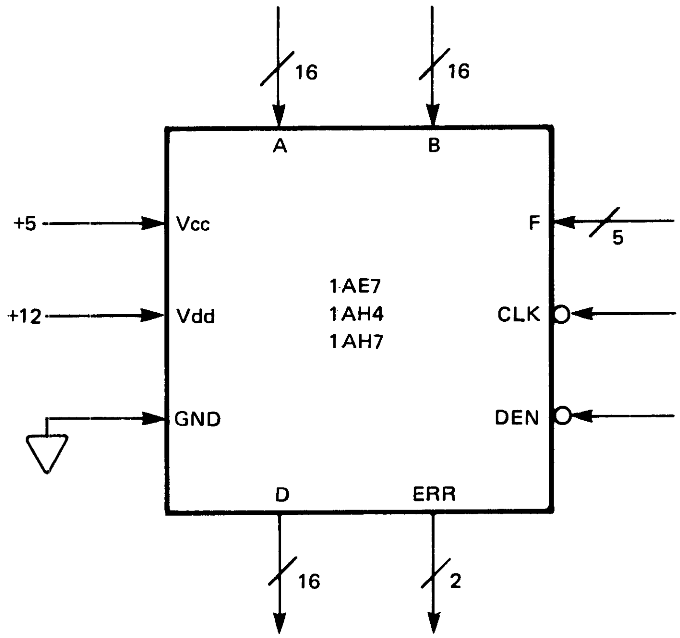


Figure 9-3. External View of Floating-Point Chip

9.3.2.2 Floating Point Chip Operation

To perform an operation with the floating point chips the function opcode must be presented to the control word inputs and the two operands must be presented to the A and B inputs at the falling edge of the chip clock pulse. The operands are clocked into the chip, 16 bits at a time with the most significant word first until the entire operand (either 1, 2, or 4 words) is entered into the chip. The function opcode must also be valid on the control word inputs when the operands are clocked in.

When the required number of operands and control opcodes have been clocked into the chip, the 1AE7 and the 1AH4 chips require no more clock pulse edges for the operation to be performed. The 1AH7 (divide chip) requires from 11 to 21 additional clock pulse edges along with a function opcode.

Figure 9-4 shows the flow of data into and out of the floating point chips for each instruction. A and B are the two 16-bit input ports, D is the 16-bit output port, and OV is the two-bit error condition. The length of the wait period is determined by the final three tables.

```
d.f2, sab.f2, mul.f2, div.f2:

         >--------time-------->
 A  -    a1 a0 .  .  .  .  .  .  .
 B  -    b1 b0 .  .  .  .  .  .  .
 D  -    .  .  . (wait*).  d1 d0
 OV -    .  .  .  .  .  .  o  o

 mul.i2, mul.12:

         >--------time-------------->
 A  -    i1 i0 .  .  .  .  .  .  .  .  .
 B  -    j1 j0 .  .  .  .  .  .  .  .  .
 D  -    .  .  . (wait*).  k3 k2 k1 k0
 OV -    .  .  .  .  .  .  .  .  .  .

 div.i2, div.12:

         >--------------time-------------------->
 A  -    i3 i2 i1 i0 .  .  .  .  .  .  .  .  .  .
 B  -    j1 j0 x  x  .  .  .  .  .  .  .  .  .  .
 D  -    .  .  .  .  .(wait* ).  k1 k0 x  x  11 10   k=quotient,
 OV -    .  .  .  .  .  .  .  .  o  o  o  o  o  o    1=remainder

 add.f4, sab.f4, mul.f4, div.f4:

         >--------------time-------------->
 A  -    a3 a2 a1 a0 .  .  .  .  .  .  .  .
 B  -    b3 b2 b1 b0 .  .  .  .  .  .  .  .
 D  -    .  .  .  .  . (wait*).  d3 d2 d1 d0
 OV -    .  .  .  .  .  .  .  .  o  o  o  o


 shl.i4, shr.i4:

         >--------------time-------------->
 A  -    i3 i2 i1 i0 .  .  .  .  .  .  .  .
 B  -    x  x  x  n  .  .  .  .  .  .  .  .  x=place holder,
 D  -    .  .  .  .  . (wait*).  k3 k2 k1 k0  n=shift lenth
 OV -    .  .  .  .  .  .  .  .  o  o  o  o   sign bit overflow on
                                              shl.i4

 ft.il.f4:

         >-----time-------------->
 A  -    i0 .  .  .  .  .  .  .  .
 B  -    x  .  .  .  .  .  .  .  .
 D  -    .  . (wait*).  d3 d2 d1 d0
 OV -    .  .  .  .  .  .  .  .  .
```

Figure 9-4. Floating-Point Chip Operating Flow (1 of 3)

```
ft.i2.f2:

         >--------time--------->
A  -     i1 i0 . . . . . . .
B  -     x  x  . . . . . . .      x=place holder
D  -     . . . (wait*).  d1 d0
OV -     . . . . . . . . .

ft.i2.f4:

         >--------time------------->
A  -     a1 a0 . . . . . . . .
B  -     x  x  . . . . . . . .      x=place holder
D  -     . . . (wait*).  d3 d2 d1 d0
OV -     . . . . . . . . . .

fx.f4.i2:

         >--------------time-------->
A  -     a3 a2 a1 a0 . . . . . .
B  -     x  x  x  x  . . . . . .
D  -     . . . . . (wait*).  i1 i0
OV -     . . . . . . . . o  o

fx.f4.i1:

         >--------------time----->
A  -     a3 a2 a1 a0 . . . . .
B  -     x  x  x  x  . . . . .
D  -     . . . . . (wait*).  i0
OV -     . . . . . . . . o

cv.f4.f2:

         >--------------time-------->
A  -     a3 a2 a1 a0 . . . . . .
B  -     x  x  x  x  . . . . . .      x=place holder
D  -     . . . . . (wait*).  d1 d0
OV -     . . . . . . . . o  o
```

a, b, d = floating point number, a3=msw, a0=lsw
i, j, k = integers
l = logical (unsigned)
n = shift length from 0 to 31
x = place holder, can be any number

* - wait time is determined by the following tables
assuming tprop = 710 for 1AE7 - adder
850 for 1AH4 - multiplier
470 for 1AH7 - divider

Figure 9-4. Floating Point Chips Operating Flow (2 of 3) wait times in states for the adder (1AE7)

		source of operand: bus	source of operand: acc(ck2)
destination of operand	bus	4	3
	acc	3	3

wait times in states for the multiplier (1AH4)

		source of operand: bus	source of operand: acc(ck2)
destination of operand	bus	4	4
	acc	4	3

wait times in states for the divider (1AH7)

		source of operand: bus	source of operand: acc(ck2)
destination of operand	bus	3	3
	acc	2	2

Figure 9-4. Floating-Point Chip Operating Flow (3 of 3)

The floating point card has two clock generating circuits, one for the floating point chips and one for the accumulator. To generate the required clock edges, the card uses quad flip-flop U128 (12-E) as a cascade counter. Signal FLPC- derived from BP_PC-, is the first stage input, and FLFCLK+ derived from BP_FCLK- is the clock input to toggle all the flip-flops simultaneously. The cascaded flip-flops in U128 provide five PC clocks each being delayed by one FCLK cycle. These are used by the RAM and the chip clocking circuits. The delayed clocks ensure correct clock operation during irregular-length microcycles (during a memory error correction and micromachine freezes).

The RAM clocking circuit flip-flop U118 (14-E) and gate U98-8 (15-E), generate two positive-edge clock pulses, one in the middle of the cycle (FLFRST) and one at the end of the cycle (FLLAST). The clock edge occurring at the end of the cycle is used to clock operands passed to the card over the Y-bus into the RAMs. The clock edge occurring in the middle of the cycle is used to clock the results of an operation back into the RAMs.

The chip clocking circuit consisting of flip-flop U108 (16-E), and gates U97 (18-E) and U98-6 (18-E) generate two negative-edge clock pulses, one of these pulses is in the middle of the cycle FLMIDL from U108-5, and the other is at the end of the cycle FLWINDO from the AND logic of U108-7 and FLPC+. Only one of the floating point chips receives the clock pulse depending on which gate is enabled at the time.

There are two mechanisms to clock operands into the floating point chips. The first mechanism occurs when one or both operands are passed to the card (i.e., when both operands are not already in an accumulator or in the ACR). The state machine in U12 (12-C) monitors the transfer of the operands from the Y-bus and asserts the signal FLENB when one pair of operands (A and B) of the same significance has been received by the card. This signal forces FL1CK high which then enables U108 clocking logic to generate one clock pulse, FLMIDL.

Clock pulse FLMIDL is passed to the selected floating point chip through one of the gates of U97. The state machine in U12, then, waits for the next pair of operands of equal significance to be available on the card before asserting FLENB again. The operands can be passed to the card in any order and the state machine will assert FLENB only when a pair of operands of equal significance is available.

Table 9-4 shows the 28 possible states of the state machine in U12 that controls the assertion of FLENB.

Table 9-4. States of the State Machine in U12

STATE (U12-	Y1 14	Y2 15	Y3 16	Y4 17	FLENB 18)	STATE DESCRIPTION
a	0	0	0	0	0	reset state, no operands in queue
b	0	0	0	1	0	have 1 word of the a-operand waiting
c	0	0	1	1	0	have 2 words of the a-operand waiting
d	0	0	1	0	0	have 3 words of the a-operand waiting
e	0	1	1	0	0	have 4 words of the a-operand waiting
j	1	0	0	0	0	have 1 word of the b-operand waiting
k	1	1	0	0	0	have 2 words of the b-operand waiting
l	0	1	0	0	0	have 3 words of the b-operand waiting
m	0	1	0	1	0	have 4 words of the b-operand waiting
f	0	1	1	0	1	lowered to 3 the no. of a-operand words waiting
g	0	0	1	0	1	lowered to 2 the no. of a-operand words waiting
h	0	0	1	1	1	lowered to 1 the no. of a-operand words waiting
i	1	0	0	1	1	lowered to 0 the no. of any operand words waiting
p	1	1	0	0	1	lowered to 1 the no. of b-operand words waiting
q	0	1	0	0	1	lowered to 2 the no. of b-operand words waiting
n	0	1	0	1	1	lowered to 3 the no. of b-operand words waiting
y	0	0	0	0	1	received an a-operand, b-operand in acc
z	1	0	0	0	1	received an b-operand, a-operand in acc or ACR

The second mechanism to clock operands into the floating point chips occurs when both operands already exist on the card (either in an accumulator or in the ACR) which allows two pairs of operands to be clocked into the floating-point chips during one microcycle. The transfer is at twice the normal speed of the input operand transfers and it is only applicable when both the a-side and b-side operands are already on the card. The two-pair operand transfer is initiated by the assertion of the SPO special microorder, CK2.

In this case, the frontplane signal FP_CK2- is asserted by the micromachine. This signal forces the output of OR-gate U14-6 high to generate signal FL1CK+ that, in turn, generates clock pulse FLMIDL through gate U38 and flip-flop U108-5.

Signal FP_CK2- also forces the output U15-1 (15-D) high to generate a second clock pulse, FLWINDO, from flip-flop U108-7 and gate U107-1 (27-E). FLWINDO is the second clock pulse that is passed to the selected floating point chip.

When operands are being clocked into the floating point chips, the data selector U35 (14-B) is addressing the accumulator location of the a-side operand (FLAU0 and FLAU1) and the data selector U25 (15-B) is addressing the accumulator location of the b-side operand (FLBU0 and FLBU1). The selector U36 (16-C) is addressing the fraction of the operand being clocked into the floating point chips (FLLC0 and FLLC1). The counter for the fraction address is clocked after each transfer to address the next fraction.

9.4 DC TO DC CONVERTER

A portion of the floating board contains the traces and connections to accept additional logic which performs a DC to DC conversion of the backplane 12.0 volts to 12.3 volts. At present this logic is bypassed by a jumper and is not loaded into the board.

9.5 INTERFACE

The FPP has a frontplane and a backplane interface. For the backplane interface, the card receives only clock signals (FCLK- and PC-) and dc power. All other required signals come from the frontplane. Refer to section X of this manual for additional details of the backplane.

The FPP receives 89 signals from the system frontplane (refer to Section XI). The Y-bus, B-bus, and N-bus are used to transfer data to and from the card. Additional control signals are received to indicate when the buses are valid.

The control-store address bus and the control-store data bus are used by the portion of the FPP containing control store ROMs. The CSIDFP- and CSIDWC- control store input disable lines are used to determine priority in the control store chain.

9.6 FPP FIRMWARE

The FPP contains sockets for two banks of control store PROMs. There are four jumpers which allow the sockets to accept either 2k x 8-bit or 4k x 8-bit PROMs. The microaddress lines are buffered by U111 (31-A) and U121 (31-B) and are passed to both banks of PROMs. The upper microaddress lines are decoded to generate the enable lines for the banks.

The length of the first bank of control store (FPROM0, FPROM1, FPROM2, FPROM3) is determined by the jumpers W2 and W4 (34-B and 31-B). The starting address of this bank of PROMs is hardwired to be 0x1000 (hex).

The first bank of control store accepts the FPP/SIS/VIS PROMs. Switch position S6 of SW1, U127 (32-C) is used to enable this bank of control store. When S6 is open the bank is disabled, when S6 is closed the bank is enabled.

When switch S6 is enabled the signal FLCS is asserted for all control store accesses to addresses 1000-17FF, causing FLENBFX to enable the bank of PROMs. Switch position S5 of U127 (32-C) is used to enable the jump table overlay. This enables a 64-word location (1180-11BF) of this bank of control store to overlay the 64-word location (0180-01BF) of the jump table that determines the location for floating point dependent instructions. The signal FLOVRLY is asserted when an access to microaddresses 0180-01BF occur, causing FLENBFX to enable the bank of PROMs.

The length of the second bank of control store (VPROM0, VPROM1, VPROM2, VPROM3) is determined by the jumpers W1 and W3 (35-B and 33-C). Three switches (positions S1, S2, S3 of SW1, U127) determine the starting address of the 2k block of control store when 2k x 8-bit PROMs are used, or two switches (S1, S2) determine the starting address of the 4k-word block when 4k x 8-bit PROMs are used. These switches are set to match the upper two or three microaddress lines of the desired location in microaddress space where open = 1 and closed = 0.

The outputs of the control store PROMs are buffered by U71 (38-B), U81 (38-B) U91 (38-C), and U101 (38-C) before being driven on the microdata bus. The frontplane signal FP_CSODWC is asserted by the WCS and PCS cards when they drive the microdata bus. This line disables the buffers on the floating point card giving the WCS and PCS cards priority.

The signal FP_CSIDFP is asserted when the control store on the floating point card is driving the microdata bus. This signal disables the control store on the lower processor card during the access.

All control store on the floating point card has higher priority in the control store chain than the control store on the processor card, but has lower priority than any control store on the WCS or PCS cards.

9.7 PARTS LOCATIONS

The parts locations for the floating point processor are shown in Figure 9-4.

9.8 REPLACEABLE PARTS LIST

The replaceable parts for the floating point processor are listed in Table 9-4. Refer to Table 3-8 for the names and addresses of the manufacturers of the parts in the Manufacturer's Code List.

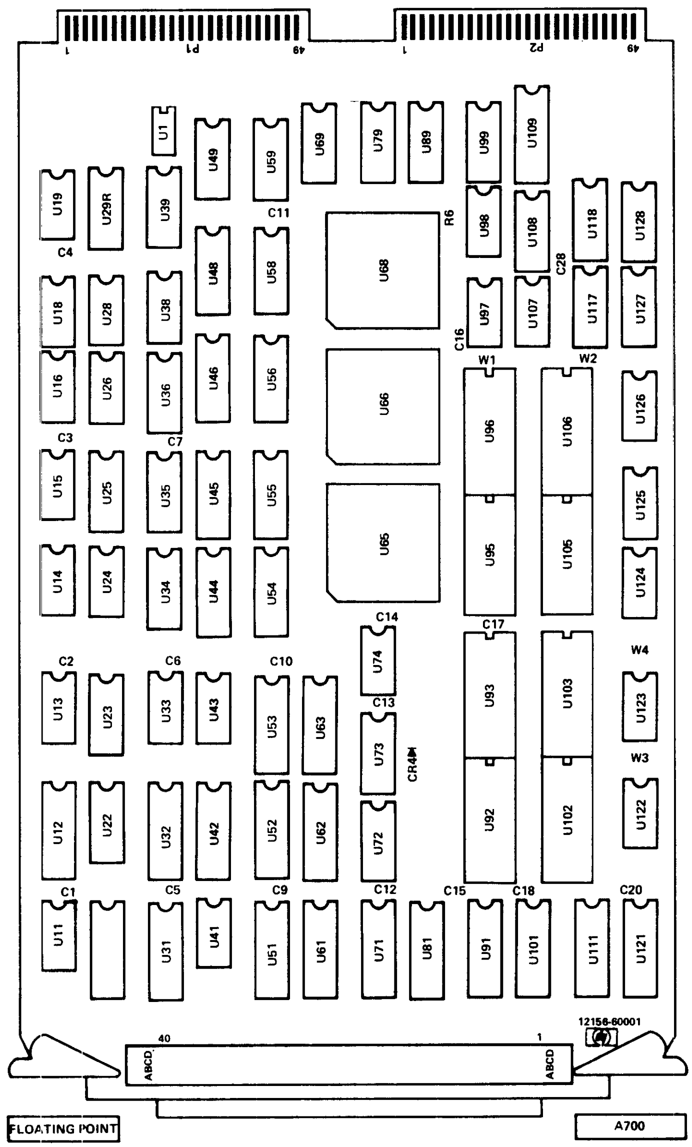


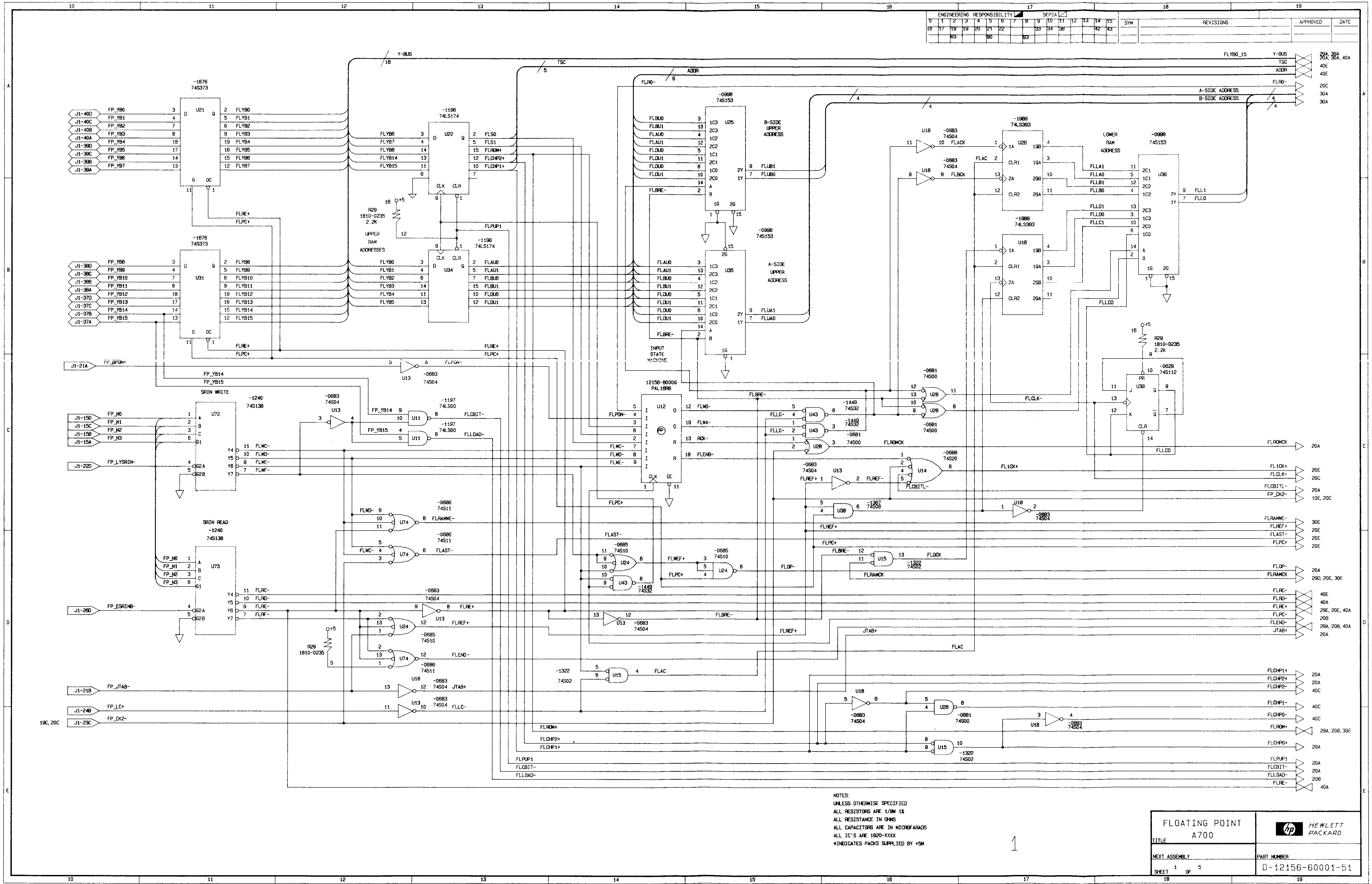
Figure 9-5. 12156A Parts Locations

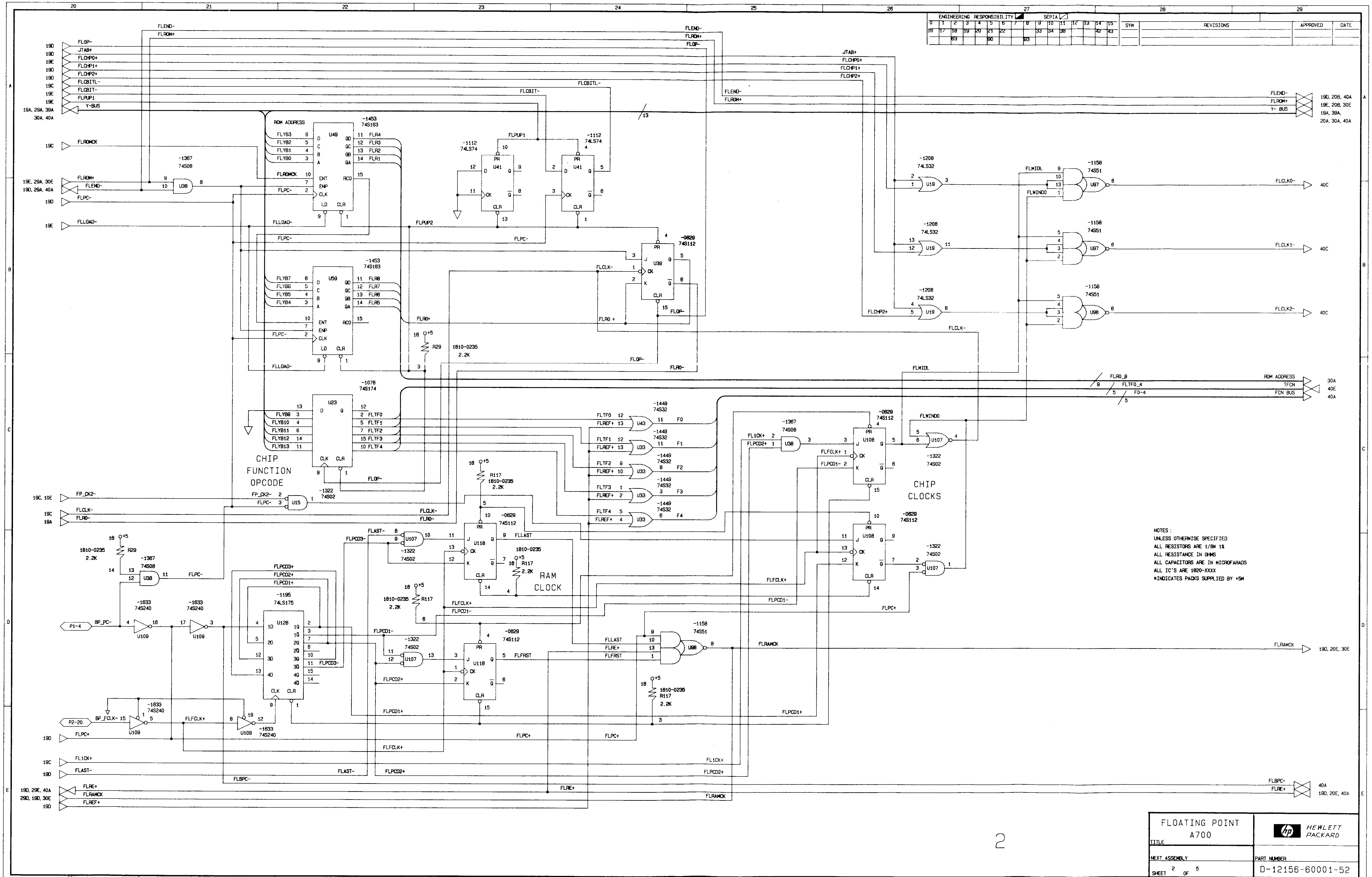
Table 9-4. Replaceable Parts for the 12156A

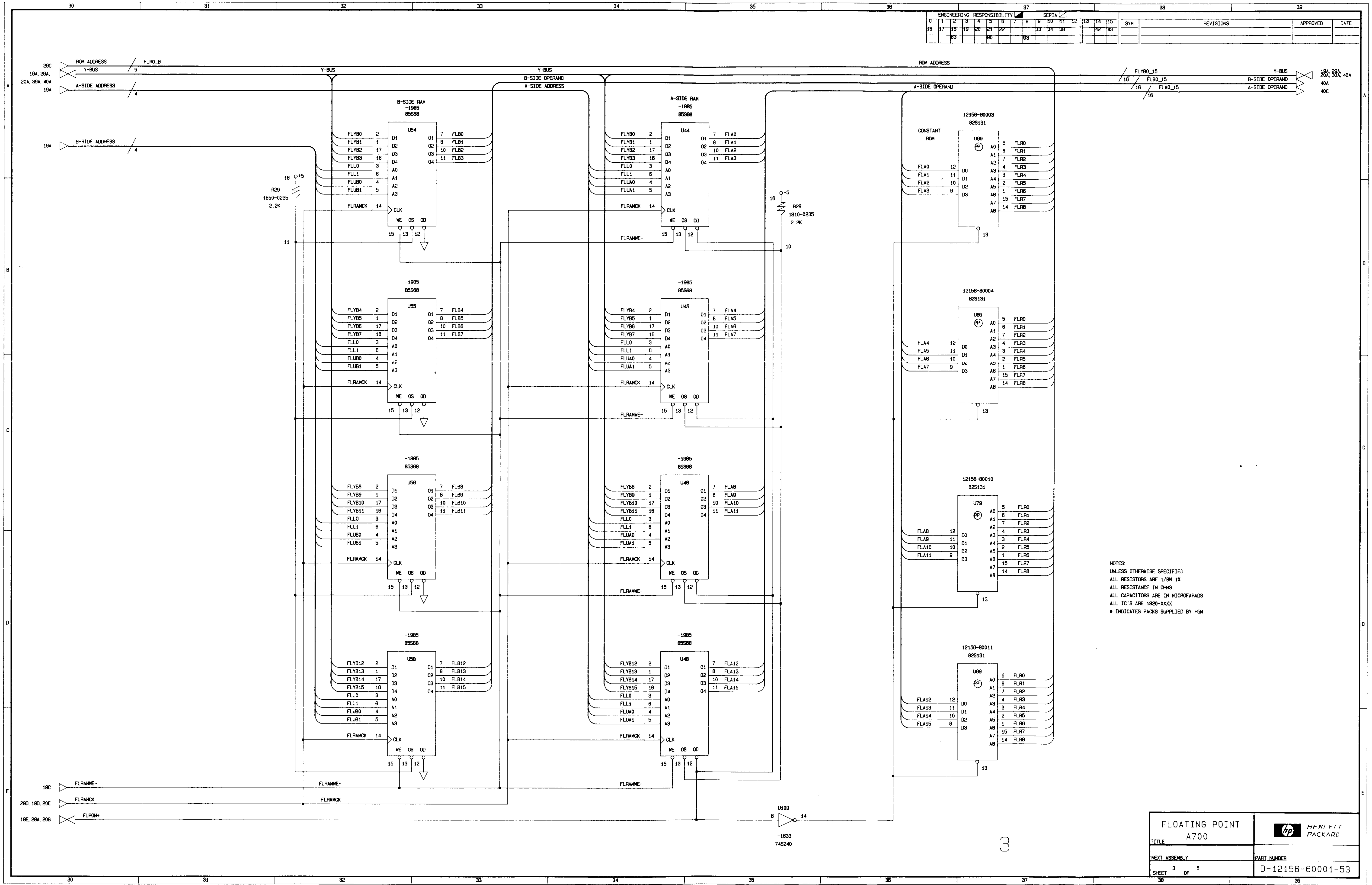
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12156-60001	5	1	PCA-FLOATING PNT	28480	12156-60001
C1	0160-4842	6	21	CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C2	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C3	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C4	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C5	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C6	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C7	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C8	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C9	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C10	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C11	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C12	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C13	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C14	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C15	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C16	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C17	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C18	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C19	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C20	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
C21	0160-4842	6		CAPACITOR-FXD .22UF +80-20% 50VDC CER	28480	0160-4842
U11	1820-1197	9	1	IC GATE TTL LS NAND QUAD 2-INP	01295	SN74LS00N
U12	12156-80009	5	1	IC-ROM, STATE MCH	28480	12156-80009
U13	1820-0683	6	2	IC INV TTL S HEX 1-INP	01295	SN74S04N
U14	1820-0688	1	2	IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U15	1820-1322	2	3	IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U16	1820-1989	7	2	IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U18	1820-0683	6		IC INV TTL S HEX 1-INP	01295	SN74S04N
U19	1820-1208	3	1	IC GATE TTL LS OR QUAD 2-INP	01295	SN74LS32N
U21	1820-1676	9	2	IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U22	1820-1196	8	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U23	1820-1076	3	1	IC FF TTL S D-TYPE POS-EDGE-TRIG CLEAR	01295	SN74S174N
U24	1820-0685	8	1	IC GATE TTL S NAND TPL 3-INP	01295	SN74S10N
U25	1820-0998	6	3	IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN74S153N
U26	1820-1989	7		IC CNTR TTL LS BIN DUAL 4-BIT	07263	74LS393PC
U28	1820-0681	4	2	IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U29	1810-0235	3	2	NETWORK-RES 16-DIP2.2K OHM X 15	01121	316A222
U31	1820-1676	9		IC LCH TTL S D-TYPE OCTL	01295	SN74S373N
U32	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U33	1820-1449	4	2	IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U34	1820-1196	8		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS174N
U35	1820-0998	6		IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN74S153N
U36	1820-0998	6		IC MUXR/DATA-SEL TTL S 4-TO-1-LINE DUAL	01295	SN74S153N
U38	1820-1367	5	1	IC GATE TTL S AND QUAD 2-INP	01295	SN74S08N
U39	1820-0629	0	3	IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U41	1820-1112	8	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG	01295	SN74LS74AN
U42	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U43	1820-1449	4		IC GATE TTL S OR QUAD 2-INP	01295	SN74S32N
U44	1820-1985	3	8	IC RGTR TTL S D-TYPE	27014	DM85S68J
U45	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U46	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U48	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U49	1820-1453	0	2	IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U51	1820-1677	0	4	IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U52	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U53	1820-1624	7	8	IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U54	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U55	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U56	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U58	1820-1985	3		IC RGTR TTL S D-TYPE	27014	DM85S68J
U59	1820-1453	0		IC CNTR TTL S BIN SYNCHRO POS-EDGE-TRIG	01295	SN74S163N
U61	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U62	1820-1677	0		IC FF TTL S D-TYPE OCTL	01295	SN74S374N
U63	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U69	12156-80011	9	1	IC-ROM, CONST 3	28480	12156-80011
U71	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U72	1820-1240	3	2	IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U73	1820-1240	3		IC DCDR TTL S 3-TO-8-LINE 3-INP	01295	SN74S138N
U74	1820-0686	9	1	IC GATE TTL S AND TPL 3-INP	01295	SN74S11N
U79	12156-80010	8	1	IC-ROM, CONST 2	28480	12156-80010
U81	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U89	12156-80004	0	1	IC-ROM, CONST 1	28480	12156-80004
U91	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U97	1820-1158	2	2	IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U98	1820-1158	2		IC GATE TTL S AND-OR-INV DUAL 2-INP	01295	SN74S51N
U99	12156-80003	9	1	IC-ROM, CONST 0	28480	12156-80003

Table 9-4 Replaceable Parts for the 12156A (continued)

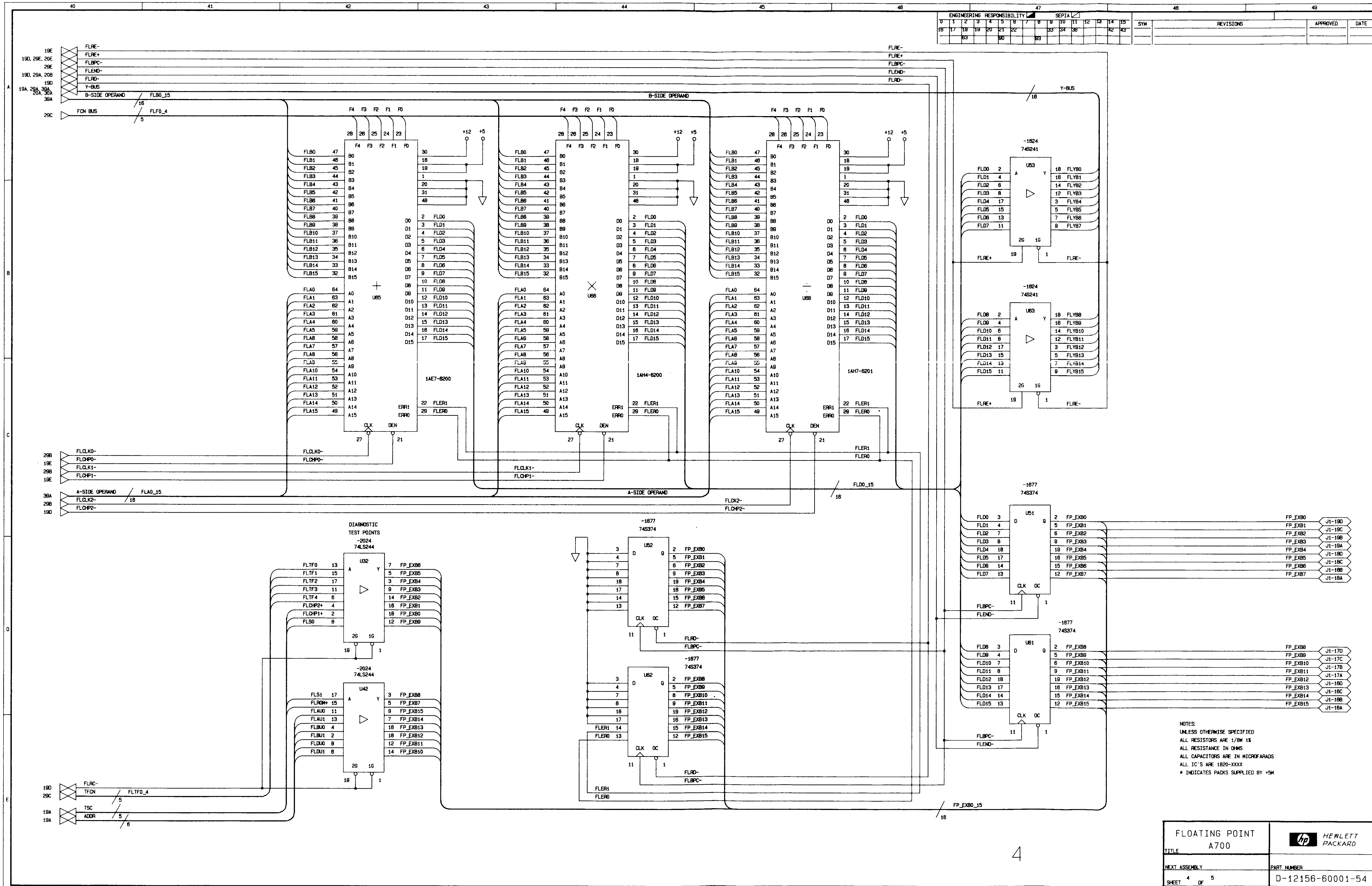
Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
U101	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U107	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U108	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U109	1820-1633	8	1	IC BFR TTL S INV OCTL 1-INP	01295	SN74S240N
U111	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U117	1810-0235	3		NETWORK-RES 16-DIP2.2K OHM X 15	01121	316A222
U118	1820-0629	0		IC FF TTL S J-K NEG-EDGE-TRIG	01295	SN74S112N
U121	1820-1624	7		IC BFR TTL S OCTL 1-INP	01295	SN74S241N
U122	1820-1322	2		IC GATE TTL S NOR QUAD 2-INP	01295	SN74S02N
U123	1820-1275	4	1	IC GATE TTL S NOR DUAL 5-INP	01295	SN74S260N
U124	1820-0688	1		IC GATE TTL S NAND DUAL 4-INP	01295	SN74S20N
U125	1820-0681	4		IC GATE TTL S NAND QUAD 2-INP	01295	SN74S00N
U126	1820-1211	8	1	IC GATE TTL LS EXCL-OR QUAD 2-INP	01295	SN74LS86N
U127	3101-2492	7		SWITCH-ROCKER 8 POSITION	28480	3101-2492
U128	1820-1195	7	1	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS175N
W1	0811-3587	5	5	RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W2	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W3	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W4	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587
W5	0811-3587	5		RESISTOR-ZERO OHMS 22 AWG LEAD DIA	28480	0811-3587


ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
INPUT STATE MACHINE
B-SIDE UPPER ADDRESS
A-SIDE UPPER ADDRESS
LOWER RAM ADDRESS
UPPER RAM ADDRESSES
SRIN WRITE
SRIN READ
NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
*INDICATES PACKS SUPPLIED BY +5M
1
FLOATING POINT
A700
TITLE
HEWLETT PACKARD
NEXT ASSEMBLY
PART NUMBER
SHEET 1 OF 5
D-12156-60001-51

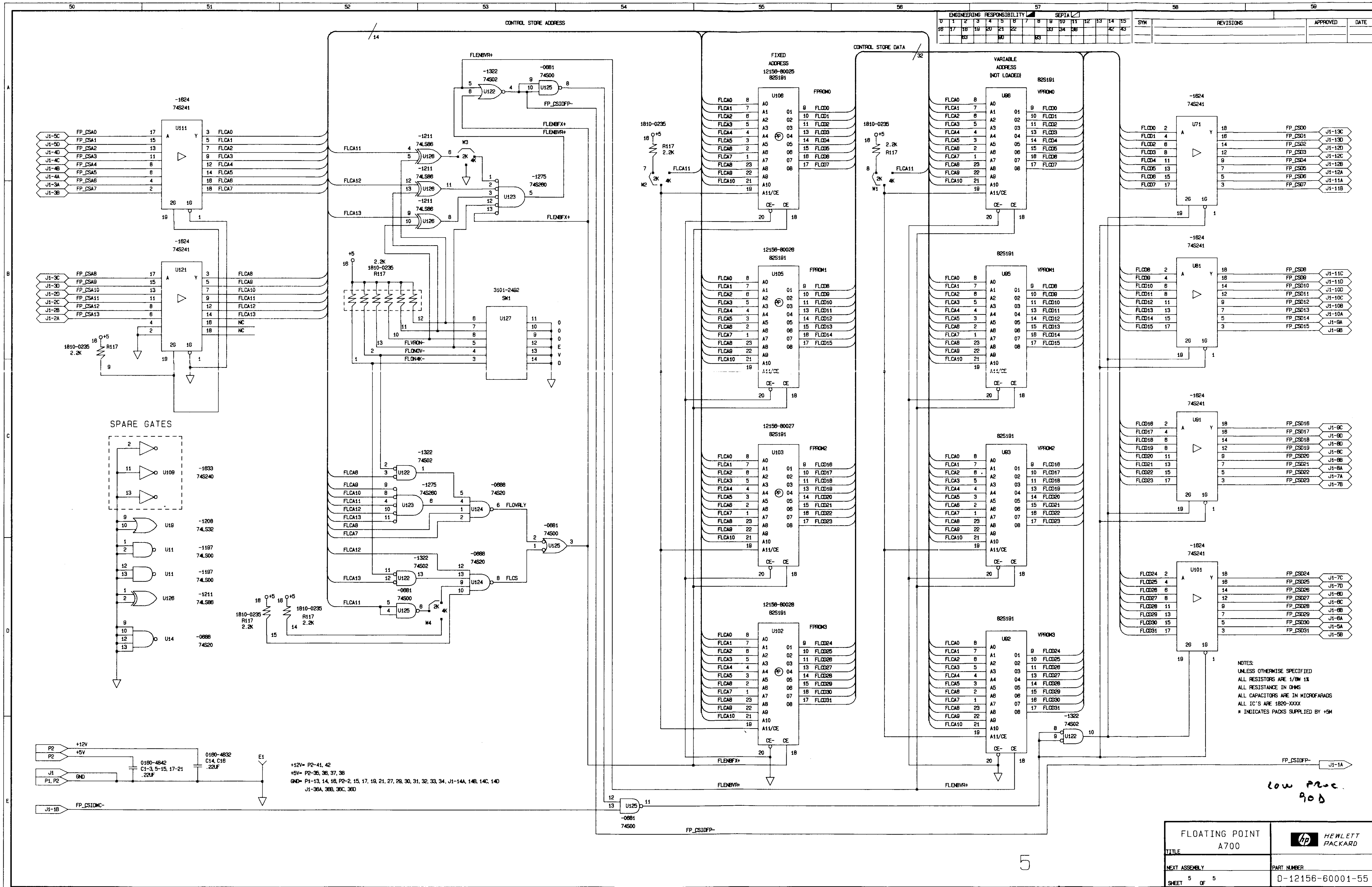

CHIP FUNCTION OPCODE
CHIP CLOCKS
RAM CLOCK
ROM ADDRESS
NOTES :
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
*INDICATES PACKS SUPPLIED BY +5V
ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
FLOATING POINT
A700
TITLE
HEWLETT PACKARD
NEXT ASSEMBLY
PART NUMBER
SHEET 2 OF 5
D-12156-60001-52
2



ROM ADDRESS
Y-BUS
A-SIDE ADDRESS
B-SIDE ADDRESS
B-SIDE OPERAND
A-SIDE OPERAND
B-SIDE RAM
A-SIDE RAM
CONSTANT ROM
U54
U55
U56
U58
U44
U45
U46
U48
U99
U89
U79
U69
R29
1810-0235
2.2K
12156-80003
12156-80004
12156-80010
12156-80011
82S131
85S68
-1985
FLRAMWE-
FLRAMCK
FLROM+
U109
-1833
74S240
NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
* INDICATES PACKS SUPPLIED BY +5M
ENGINEERING RESPONSIBILITY
SEPIA
REVISIONS
APPROVED
DATE
FLOATING POINT
A700
TITLE
HEWLETT PACKARD
NEXT ASSEMBLY
PART NUMBER
SHEET 3 OF 5
D-12156-60001-53
3



ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
B-SIDE OPERAND
A-SIDE OPERAND
FCN BUS
Y-BUS
DIAGNOSTIC TEST POINTS
-2024 74LS244
-1824 74S241
-1677 74S374
1AE7-6200
1AH4-6200
1AH7-6201
NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
# INDICATES PACKS SUPPLIED BY +5M
4
FLOATING POINT
A700
TITLE
NEXT ASSEMBLY
SHEET 4 OF 5
HEWLETT PACKARD
PART NUMBER
D-12156-60001-54



CONTROL STORE ADDRESS
CONTROL STORE DATA
ENGINEERING RESPONSIBILITY
SEPIA
SYM
REVISIONS
APPROVED
DATE
FIXED ADDRESS 12156-80025 82S191
12156-80026 82S191
12156-80027 82S191
12156-80028 82S191
VARIABLE ADDRESS (NOT LOADED) 82S191
FPROM0
FPROM1
FPROM2
FPROM3
VPROM0
VPROM1
VPROM2
VPROM3
-1624 74S241
3101-2462 SW1
SPARE GATES
FLENBVR+
FLENBFX+
FP_CSIDFP-
FP_CSIDMC-
FLOVRLY
FLCS
+12V= P2-41, 42
+5V= P2-35, 36, 37, 38
GND= P1-13, 14, 16, P2-2, 15, 17, 19, 21, 27, 29, 30, 31, 32, 33, 34, J1-14A, 14B, 14C, 14D
J1-36A, 36B, 36C, 36D
NOTES:
UNLESS OTHERWISE SPECIFIED
ALL RESISTORS ARE 1/8W 1%
ALL RESISTANCE IN OHMS
ALL CAPACITORS ARE IN MICROFARADS
ALL IC'S ARE 1820-XXXX
* INDICATES PACKS SUPPLIED BY +5M
low proc. 90D
FLOATING POINT A700
TITLE
HEWLETT PACKARD
NEXT ASSEMBLY
PART NUMBER
SHEET 5 OF 5
D-12156-60001-55

5

BACKPLANE | SECTION X

10.1 INTRODUCTION

The backplane provides a link between the A700 Computer System upper processor card, memory controller, memory array, WCS, interface cards and power supply.

In this document the backplane is viewed from two aspects: physical and logical.

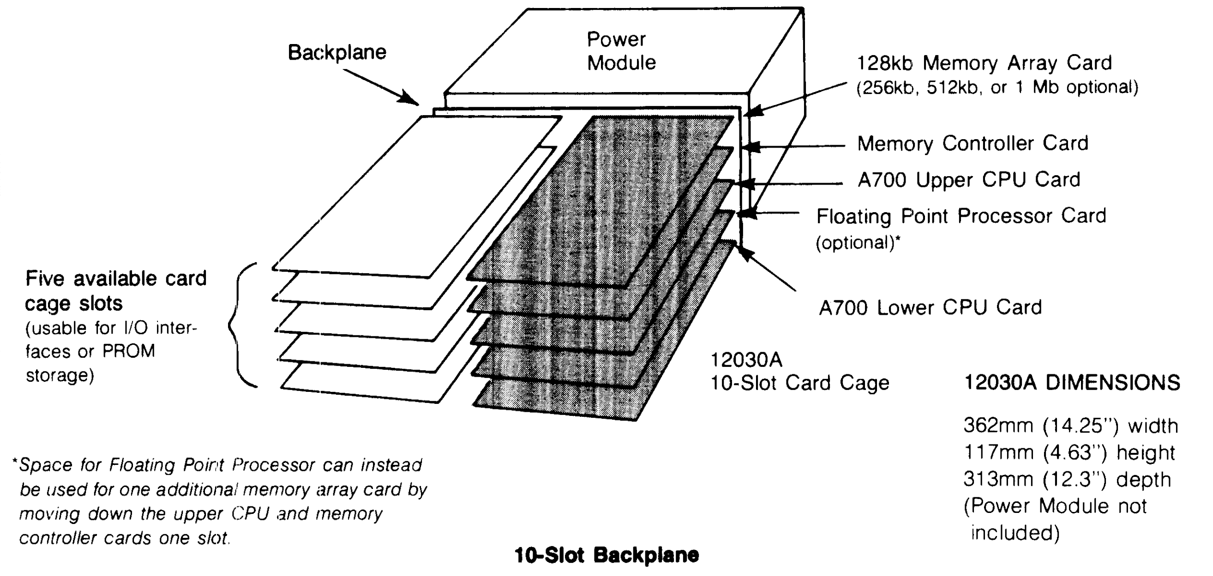
10.2 BACKPLANE PHYSICAL DESCRIPTION

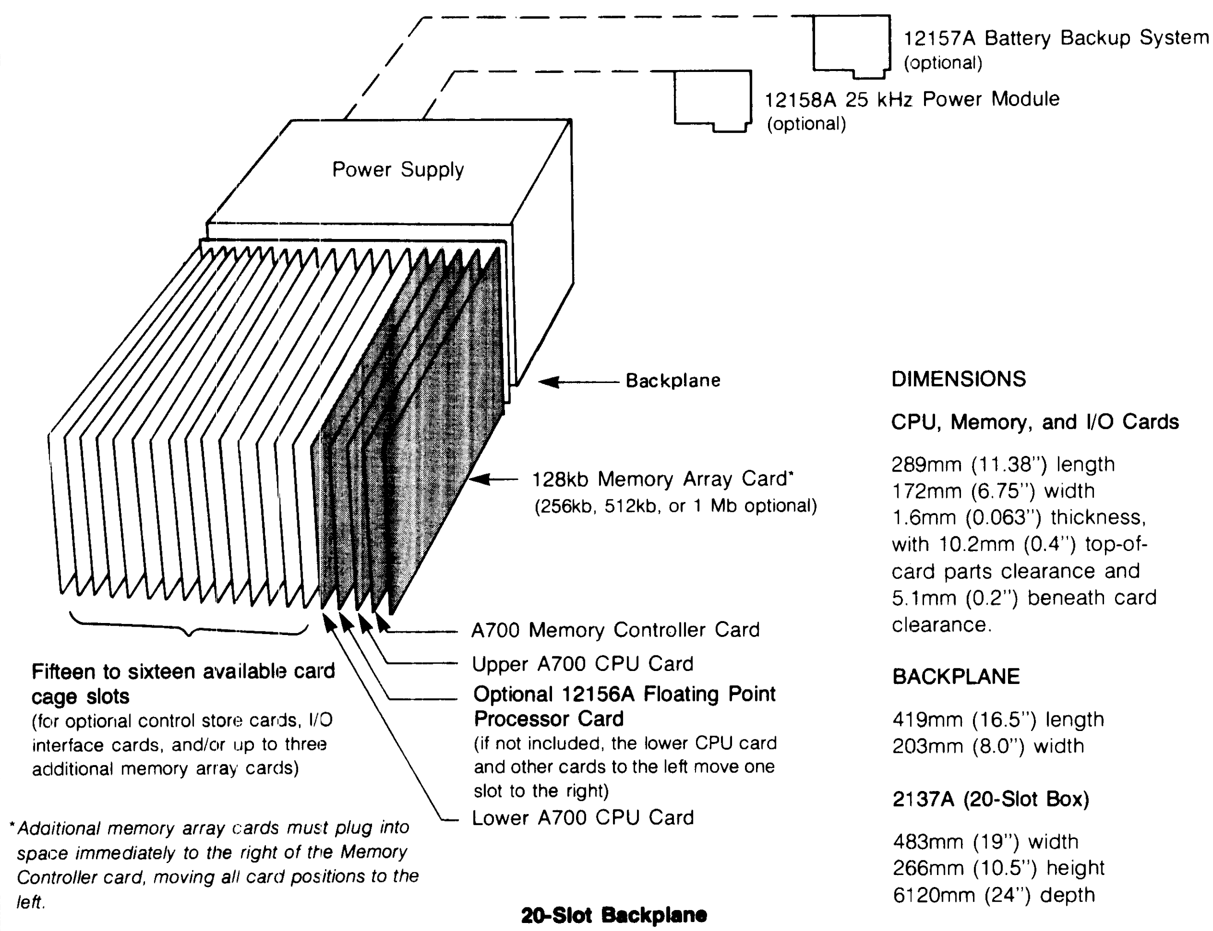
The backplane functions as a mother board for the processor, memory and interface cards. It is a printed circuit card on which the traces carry the power, ground and interconnecting signals between all the cards in an A700 Computer. Figure 10-1 shows the physical layout of the 10-slot, 16-slot, and 20-slot backplanes.

The logical backplane defines protocols for the communications between all cards in the system. The definition, function, and timing of the backplane signals, and the protocols for their interaction are all considered to be part of the logical backplane.

Thus, the physical backplane houses a set of communications channels, whereas the logical backplane defines protocols for that communication.

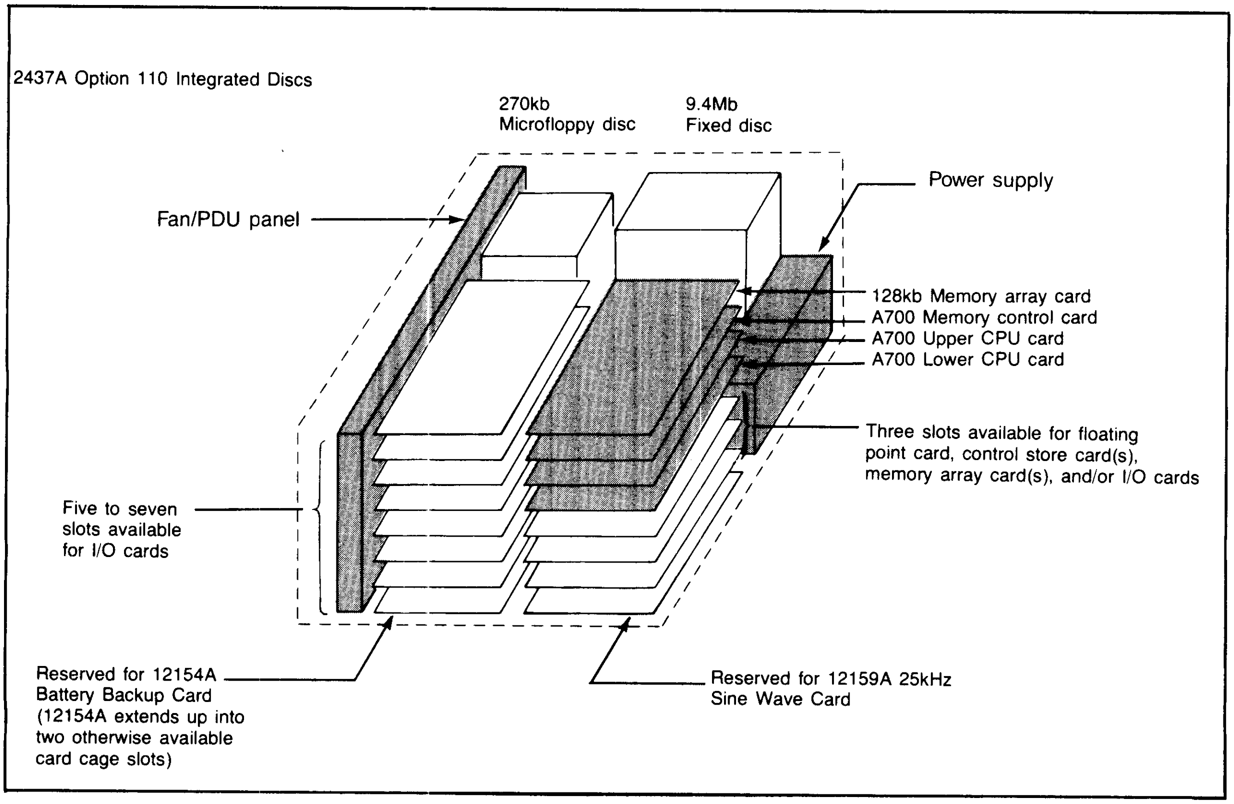
This section covers both aspects of the backplane, and is intended to provide all the information needed to design a hardware interface to the backplane and thereby successfully integrate a design of arbitrary functions into the A700 Computer.





8200-139

Figure 10-1. HP 1000 A700 Backplanes (Sheet 1 of 2)



16-Slot Backplane

Figure 10-1. HP 1000 A700 Backplanes (Sheet 2 of 2)

10.3 OVERVIEW

10.3.1 SYSTEM ENVIRONMENT OVERVIEW

A backplane integrated into a system environment is shown in Section I, Figure 1-2. The backplane holds two sets of connectors for card edge connections as follows:

A. POWER SUPPLY CONNECTOR SLOTS

On the 20-slot backplane, DC power is connected to the backplane directly from the power supply through 50-pin sockets, designated J1 and J2 (sockets XA21 and XA22); i.e, two power supply PC connector cards plug into the opposite side of the backplane from the A700 card side. On the 16-slot backplane a single 35-pin socket is used for DC power.

B. A700 CARD CONNECTOR SLOTS

Each card plugs into a set of dual 50-pin sockets (each set designated J1 and J2 of sockets XA1 through XA20) for a total of 100 connections. These pins carry signals, power, and ground connections between the card and the backplane. The 20-slot backplane shown in Figure 10-2A has a total of 20 dual card slots (the 12030A backplane has slots for ten cards and is basically the same). The 16-slot backplane shown in Figure 10-2B, used in the 2437A and 2487A, has 14 sets of dual 50-pin sockets for the CPU and I/O cards, a single 50-pin socket for the battery backup option, and a 30-pin socket for the 25 KHz card option.

Additional details are given under Specifications, para. 10.3.2.

A700 cards can be plugged into any backplane card slot subject to the following constraints.

a. The upper processor must be directly above the lower processor unless there is a floating point card which goes between the two processor cards.

b. The memory controller must go directly above the upper processor.

c. The first memory array must go directly above the memory controller followed by any additional memory arrays.

d. The first WCS or PCS card must be directly below the lower processor followed by any additional WCS or PCS cards. WCS cards are usually installed above PCS cards.

e. All I/O cards must go below the WCS and PCS cards in the order of the desired card priority.

f. Any unused slot between two I/O cards must be filled with a priority jumper card.

The terms "above" and "below" are not to be taken literally. The term "above" refers to a higher priority slot and "below" refers to a lower priority slot where the physical orientation of the slots may be horizontal. The backplane slots are numbered from the highest priority slot XA1 in order down to XAn which is the nth highest priority slot in the card cage (see Figure 10-2).

10.3.2 INTERNAL SPECIFICATIONS OVERVIEW

Refer to Figure 10-2 for backplane parts locations. The 10-slot backplane (not shown) is similar to the 20-slot backplane but arranged in two rows of five sockets each.

The three diodes on each backplane are on the +5V, +12V and -12V lines from the Power Supply. They are transient voltage suppressors, with a clamping action response of one picosecond, and the capability of handling a surge current of 50 amperes. They serve to protect the components on the cards plugged into the backplane from any power supply over-voltage or transient spike.

The physical backplane includes four different types of traces.

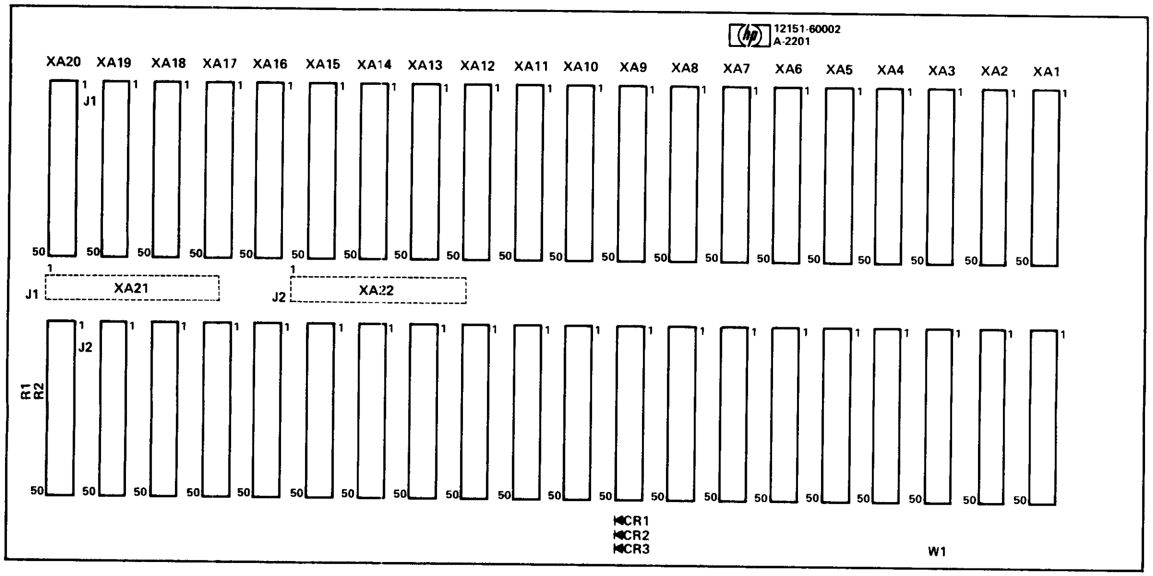
a. Bus line: This line is common to the same pin on each set of card sockets. Examples are WE- and CRS-.

b. Power Supply line: This line comes from the power supply and runs to the same pin on each set of card sockets. Examples are PFW and PON+.

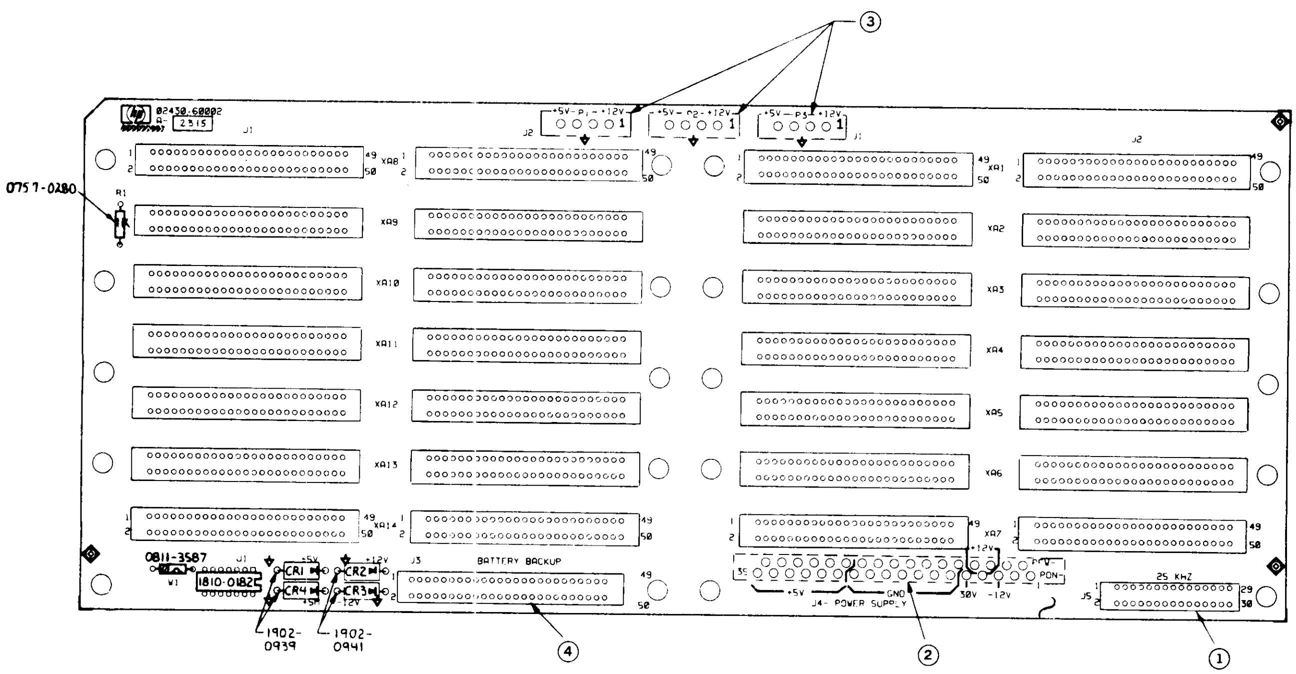
c. Ground and Voltage lines: This line comes from the power supply and typically has two or more pin assignments on each set of card sockets. Grounds and voltages are typically carried on much wider traces than other signals. Examples are +5V and +12V.

d. Chained lines: This is a set of lines which connect every pair of adjacent card sockets. Each of these lines is common to exactly two sockets. Examples are ICHID-, ICHOD-, SCHID-, and SCHOD-.

The distinction between these four types of lines is important when determining backplane compatibility.



A. 20-Slot Backplane Configuration



ITEM	MATERIAL DESCRIPTION	PART NO.
1	CONN PC EDGE	1251-8396
2	CONN 35-PIN F	1251-8346
3	CONN 4-PIN	1251-8331
4	CONN 2 X 25	1251-8053

NOTE: Backplane 02430-60002 is replaced by 02430-60015. Parts locations of the two versions are identical.

B. 16-Slot Backplane Configuration

Figure 10-2. Backplane Configurations

Update 1

10.3.3 BACKPLANE INTERFACE HARDWARE

All backplane interface hardware can be broken down into four categories as listed below. It may be helpful to become familiar with one or more of these categories.

10.3.3.1 Processor Interface

The signal interfaces are mainly located on the upper processor card and backplane clocks are located on the lower processor card. The clocks include SCLK and FCLK and the signals include such signals as RNI (Read Next Instruction) and IAK (Interrupt Acknowledge). The processor interface information is presented in Section II of this document.

10.3.3.2 Memory Interface

This interface is responsible for generating such signals as PE (memory Parity Error) and VALID (data bus Valid). The memory interface information is presented in Section IV.

10.3.3.3 I/O Master Interface

The I/O master interface consists of an IOP chip and its support logic. This circuitry is located on every A-Series I/O card and serves to standardize the I/O interface to the backplane by performing all the functions (I/O instruction recognition and execution, interrupt processing, DMA control) common to all I/O cards.

10.3.3.4 Passive Interfaces

Passive interfaces include those that supply, monitor or use power lines, or monitor signals without ever generating signals or interacting on the backplane.

10.4 SPECIFICATIONS

10.4.1 GENERAL HARDWARE SPECIFICATIONS

The backplane uses a six-layer, printed circuit card to provide all the required signal and power traces. One layer provides a +5V plane, and another is a ground plane to minimize signal crosstalk and permit the traces to maintain a consistent characteristic impedance throughout their length.

The four remaining layers are mainly to carry signals and for voltage distribution. The layout provides a characteristic impedance of 47 to 51 ohms that provides a good match with the output impedances of the backplane drivers. The driver impedances are in the range of 25 to 100 ohms; i.e., all impedances are matched within a 2 to 1 ratio.

10.4.2 POWER SUPPLY INTERCONNECT

The dc output connectors P1 and P2 of the 20-slot backplane are the edge connector type. Pin assignments for these power supply connectors are given in Table 10-1. The power supply connector of the 16-slot backplane is described in Table B-12 (Appendix B.)

Ground and +5V lines carry the highest currents and are thus transferred over whole planes. Currents for other voltages are carried over multiple traces.

Table 10-1. Power Supply Connector Pin Assignments

CONNECTOR P1 -- DC OUTPUT	
PIN NUMBER	SIGNAL NAME
1 THROUGH 36	+5 VOLTS
37 THROUGH 50	COMMON (GROUND)

CONNECTOR P2 -- DC OUTPUT	
PIN NUMBER	SIGNAL NAME
1 THROUGH 28	COMMON
29 THROUGH 32	+12V VOLTS
33 THROUGH 34	-12 VOLTS
35 THROUGH 38	+5 VOLTS MEMORY BACKUP
39 THROUGH 42	25 kHz PHASE 1
43 THROUGH 46	25 kHZ PHASE 2
47	PON+
48	PFW-
49	MLOST-
50	SPARE

10.4.3 CARD SOCKET INTERCONNECTS

Each card in the A700 has two 50-pin edge-connectors, P1 and P2, which plug into a set of 50 pin sockets J1 and J2 on the backplane, respectively. The card cage is constructed with card guides, in such a manner that the cards will slide in and then snap into place in the backplane connectors. The cards must be inserted with the component sides of the cards facing the same way as shown in Figure 10-3 (components face to the right when looking into the front of the 20-slot card cage). The pin assignments for these 100 connections are given in Table 10-2. For signal definitions, refer to Table 10-37.

10.4.4 BACKPLANE LOADING RULES

Backplane loading rules were established in order to provide guidelines for the selection of bus drivers and backplane signal drivers, and in order to insure that these drivers are not overloaded. These rules take into account the drive capabilities and loading of certain industry standard parts such as the S and LS 240 and 241. Because there may be a maximum of 16 I/O interface cards in any given A700 system, each card must adhere strictly to the rules in order to prevent possible overloading. These loading rules were established assuming a maximum of 20 cards in a system. Note that the I/O Master is designed such that all backplane lines except the data bus are buffered and cannot be used in the unbuffered form by I/O interface logic external to the I/O Master.

DC loading rules are made to ensure that a device driving any given backplane line can handle sufficient current to keep all the inputs connected to that line at the required voltage level. Low-state load on a given line is the sum of I_{IL} maximum for all receivers plus I_{OZL} for all tri-state drivers. High-state load is the sum of I_{IH} for all receivers plus I_{OZH} for all tri-state drivers.

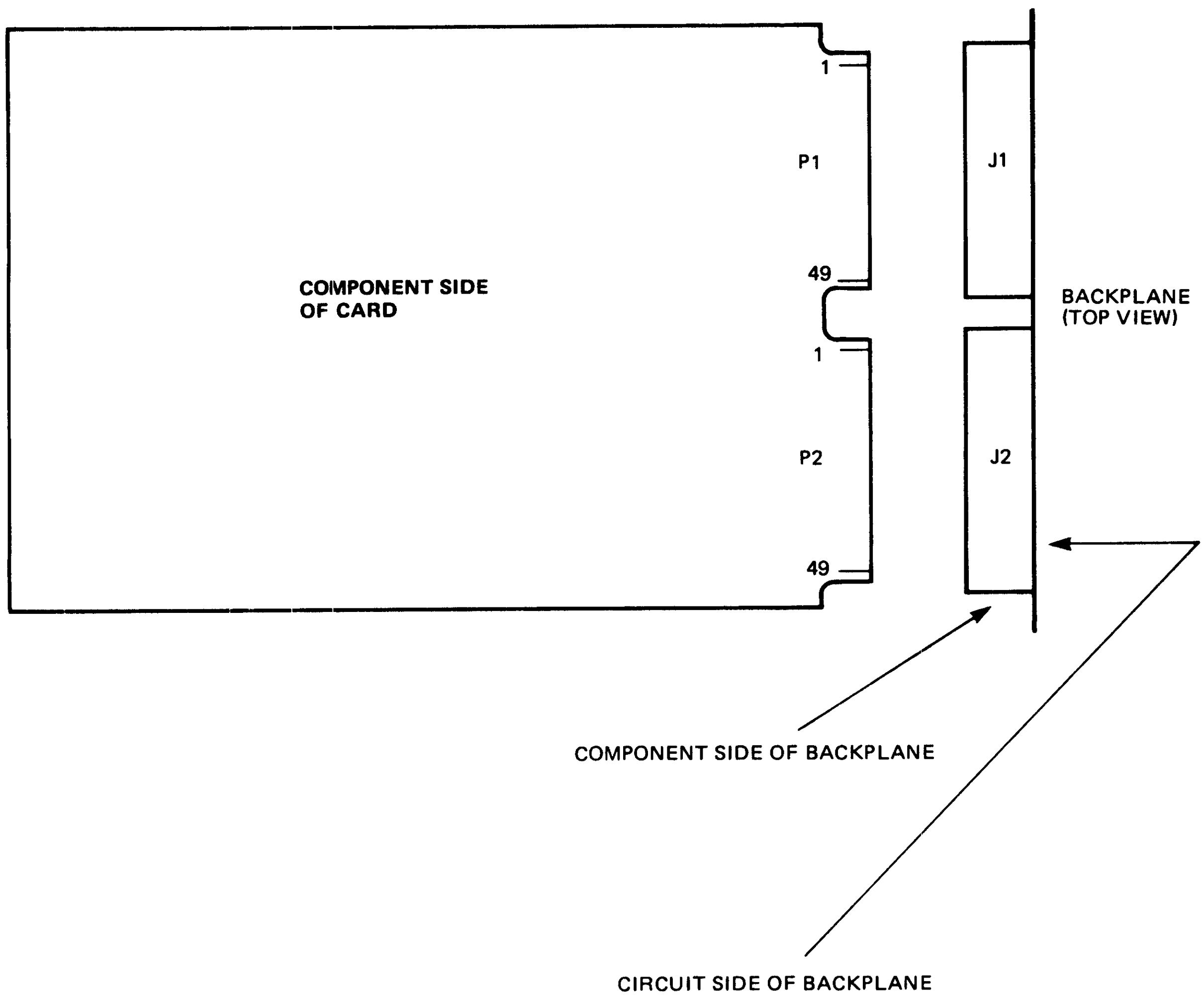


Figure 10-3. Card Socket Interconnects

Table 10-2. Pin Assignments for Backplane Sockets

PIN	XAnP1 SIGNALS		PIN	PIN	XAnP2 SIGNALS		PIN
1	ICHID-	ICHOD-*	2	1	CPUTURN	ISOGND	2
3	MCHID-	MCHOD-	4	3	REMEM-	VALID-	4
5	MLOST-	MCHODOC-	6	5	IORQ-	INTRQ-	6
7	PFW-	FETCH-	8	7	MP+	RNI-	8
9	AE0 (SC0)	AE1 (SC1)	10	9	MEMGO-	PE-	10
11	AE2 (SC2)	AE3 (SC3)	12	11	SCHID-	SCHOD-**	12
13	GND	GND	14	13	IAK-	IOGO-	14
15	EC-	GND	16	15	ISOGND	SLAVE-	16
17	AE4 (SC4)	SELFC-	18	17	ISOGND	MRQ-	18
19	AB0	AB1	20	19	ISOGND	FCLK-	20
21	AB2	AB3	22	21	ISOGND	CCLK-	22
23	AB4	AB5	24	23	SPRQ-	SCLK-	24
25	AB6	AB7	26	25	CRS-	PON+	26
27	AB8	AB9	28	27	ISOGND	BUSY-	28
29	AB10	AB11	30	29	GND	GND	30
31	AB12	AB13	32	31	GND	GND	32
33	AB14	WE-	34	33	GND	GND	34
35	DB0	DB1	36	35	+5V	+5V	36
37	DB2	DB3	38	37	+5V	+5V	38
39	DB4	DB5	40	39	+12M	-12M	40
41	DB6	DB7	42	41	+12V	+12V	42
43	DB8	DB9	44	43	-12V	-12V	44
45	DB10	DB11	46	45	+5M	+5M	46
47	DB12	DB13	48	47	25kHz Ph2	25kHz Ph2	48
49	DB14	DB15	50	49	25kHz Ph1	25kHz Ph1	50

* - Above the processor card, this signal is called PS-.
** - Above the processor card, this signal is called MEMDIS-.

10.4.4.1 Actual Worst Case Loading

Actual worst case loading for the address bus, select code bus, and the data bus is the following:

ADDRESS BUS AND SELECT CODE BUS:

	Low-State Load	High-State Load
1 Mb RAM Array (times 4)	2.0 mA	200 uA
Memory Controller	0.4 mA	50 uA
A700 Processor	0.05 mA	50 uA
I/O Master (times 13)	5.2 mA	260 uA
	-------	-------
TOTAL	7.65 mA	560 uA

DATA BUS:

	Low-State Load	High-State Load
1 MB RAM Array (1 card)	0.4 mA	40 uA
Memory Controller	0.4 mA	40 uA
A700 Processor	0.8 mA	60 uA
I/O Master (times 16)	15.5 mA	1600 uA
	-------	-------
TOTAL	17.1 mA	1.74 mA

The design rules and guidelines are shown in Table 10-3.

Table 10-3. Design Rules and Guidelines

Design Rules/Guidelines	Address Bus, AE0 - AE4	Data Bus	All Other Bussed Lines	Chained Lines
Maximum allowable load per card - high state	130 uA	250 uA	60 uA	400 uA
Maximum allowable load per card - low state	1.2 mA	1.2 mA	1 mA	10 mA
Minimum allowable drive capability - high state	2.6 mA	5.0 mA	1.2 mA	1 mA
Minimum allowable drive capability - low state	24 mA	24 mA	20 mA	20 mA

10.4.4.2 AC Loading

Every connection made to any given line places a a capacitive load on that line due to PC board trace capacitance and due to the integrated circuit input or output capacitance. Care must be taken to ensure that any given line is not capacitively overloaded as this results in a slowing down of its switching speed to below an acceptable level. Typical delays/capacitive loads are in the range of 2-nanoseconds/50-picofarads for a line driven by an LS240/241 and 4-nanoseconds/50-picofarads for an LS373/374.

The AC loading specifications, as with the DC loading rules, should be strictly adhered to for the I/O interfaces but they can be used as guidelines for processor and memory cards. Signal timing calculations are made considering actual worst case loads as shown in Table 10-3 (a 20-slot system is assumed).

10.4.4.3 Data Bus

Each card may not exceed 60-picofarads load per line.

10.4.4.4 All Other Lines

Each card may not exceed 25 picofarads load per line.

10.5 INTERFACE REQUIREMENTS

The following paragraphs deal exclusively with the logical backplane. The protocols and conventions used by all A700 cards to interact over the backplane are classified and described. An important feature of the A700 computer is its distributed intelligence. Every interface card in the system has the capability of handling its own memory accesses (DMA), of decoding its own instructions, and of forcing the central processor into slave mode processing. Each of these three capabilities and the protocols with which they are implemented are described. You may find it helpful, while working through each handshake protocol, to refer to the glossary of signal definitions in Table 10-37.

Table 10-4. Capacitance Data on 20-Slot System

PIN	SIGNAL	C_L IN pF
J1 - 1,2	ICHID, ICHOD	40
J1 - 3,4	MCHID, MCHOD	25
J1 - 5	MLOST	200
J1 - 6	MCHODOC	850
J1 - 7	PFW	200
J1 - 9,10,11,12,17	AE0 - AE4 (SC0 - SC4)	400
J1 - 18	SELFC	900
J1 - 19,20,...,34	ADDRESS BUS	500
J1 - 35,36,...,50	DATA BUS	1300
J2 - 1	CPUTURN	400
J2 - 3	REMEM	600
J2 - 4	VALID	550
J2 - 5	IORQ	580
J2 - 6	INTRQ	650
J2 - 7	MP	500
J2 - 8	RNI	500
J2 - 9	MEMGO	550
J2 - 10	PE	500
J2 - 11,12	SCHID, SCHOD	30
J2 - 13	IAK	500
J2 - 14	IOGO	500
J2 - 16	SLAVE	740
J2 - 18	MRQ	550
J2 - 20	FCLK	500
J2 - 22	CCLK	620
J2 - 23	SPRQ	250
J2 - 24	SCLK	500
J2 - 25	CRS	500
J2 - 26	PON	550
J2 - 28	BUSY	400

NOTE: All capacitances shown are worst case figures.

10.5.1 MEMORY ACCESS PROTOCOL

Every card that accesses memory uses the same handshake protocol. This approach greatly simplifies the operation of multichannel DMA. The DMA feature of every A-Series I/O interface allows input or output operations to proceed without processor intervention thus significantly easing the processing requirements on the CPU. The processor is the lowest-priority DMA device because if any other card pulls on the open-collector line MRQ (Memory Request), the processor is held off from doing a memory cycle. The processor may be locked out entirely for up to 72 microseconds by high speed interfaces using adjacent memory cycles. In order to prevent being locked out entirely, the processor can assert the RNI- signal which informs the interface cards not to reassert MRQ after their current memory request is satisfied. For more information on RNI-, refer to the definition in Table 10-37.

A priority scheme is used in the A700 to resolve contention between interfaces wanting memory cycles. An interface wanting a memory cycle will assert MRQ-, MCHOD-, and MCHODOC-. The first signal, MRQ-, will disable the processor from taking the next memory cycle. MCHOD- is part of a priority chain which will ripple down, disabling all lower-priority interfaces. MCHODOC- is a look-ahead on this chain. It is used as the top of the chain for the stack of lowest-priority slots. Although MRQ- may be asserted by one or more interfaces at any given time, MEMGO- may only be asserted by the one interface that gets the memory cycle.

An interface determines if it is entitled to a memory cycle (to assert MEMGO-) by monitoring certain backplane signals. It can initiate a memory cycle on any falling edge of SCLK- when BUSY- is high, its MCHID- is high, and its MRQ- has been asserted for at least one cycle. This stipulation means that contention among I/O cards for memory always has one cycle of SCLK in which to be resolved, namely, the cycle which occurs just before the assertion of MEMGO-.

The processor card begins its access to memory by asserting MEMGO- on the falling edge of SCLK-. If an I/O interface card desiring a DMA transfer asserts MRQ- on that same edge, the processor card must immediately relinquish its claim to accessing memory by releasing MEMGO- prior to the next rising edge of SCLK-. Therefore, contention between the processor and any I/O interface for memory is resolved during the long half cycle between the falling and rising edges of SCLK-. MEMGO- will be asserted at the completion of all current DMA requests. Refer to Table 10-20 for the aborted MEMGO- timing specifications.

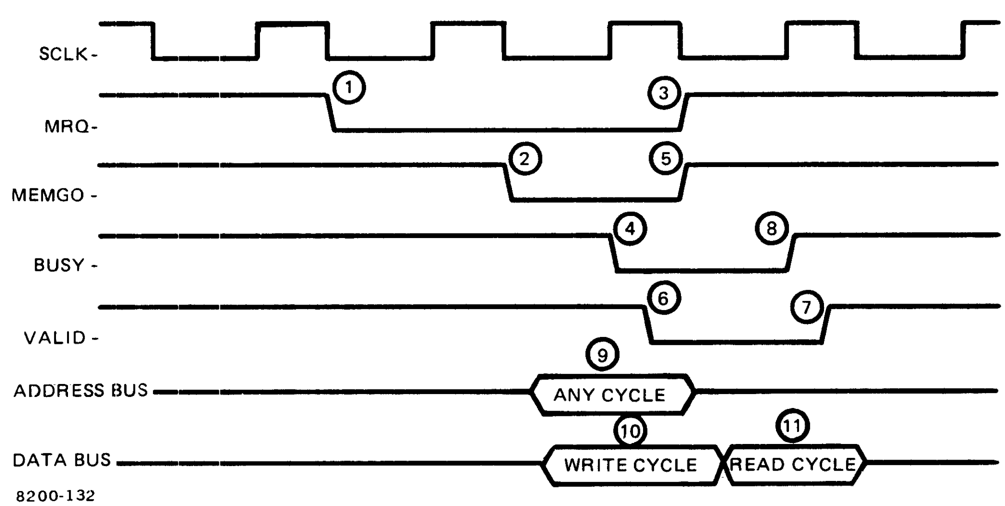
10.5.2 MEMORY HANDSHAKE TIMING

Memory handshake timing is part of the Memory and I/O state machine operation. The memory handshake timing is shown in Figure 10-4.

10.5.3 INTERRUPT PROTOCOL

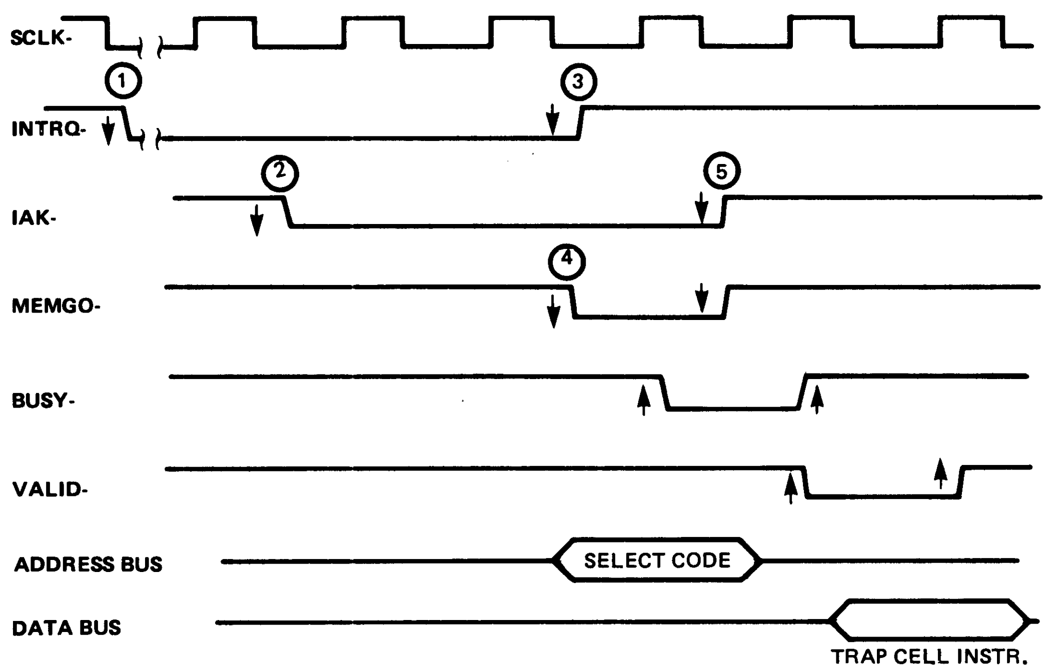
In the A700, interrupt priority is determined only by physical proximity to the processor on the interrupt priority chain. The select code is independent of a card's physical location, and it is determined by setting six switches on each I/O card, one per select code bit.

Interrupt timing is shown in Figure 10-5. An interrupt request occurs when a card's CONTROL flip-flop is set and the FLAG flip-flop gets set by either the interface itself or the execution of an STF instruction. This will cause the interface to assert the interrupt-requesting signal INTRQ- on the backplane. INTRQ- is a common signal (open collector, wired-OR) used by all interfaces to notify the processor that one of the interfaces would like an interrupt. An interrupt acknowledgement, IAK-, from the processor card, is triggered by an interrupt request from any one of the I/O interfaces. When the CPU chip reaches the state where it is ready to fetch the next instruction, and if the interrupt system is enabled and interrupts are not temporarily being held off, then the processor will assert IAK-.



* BUSY is generally asserted for one SCLK- cycle but may be asserted as long as five SCLK- cycles.

Figure 10-4. Memory Handshake Timing



1. An interface card pulls on INTRQ- to request interrupt service.

2. When the processor has reached the appropriate state and if the interrupt system is enabled, and interrupts are not temporarily being held off, then it will acknowledge the interrupt request by asserting IAK-.

3. As soon as the interface card asserts MEMGO, it knows its interrupt will be serviced so it releases INTRQ-.

4. The interface card asserts MEMGO- to initiate a memory cycle, and during the one cycle of SCLK it holds MEMGO- low, it drives the lower 6 bits of the address bus with its select code, and the upper 9 bits with zeros.

5. The processor releases IAK- upon the assertion of BUSY-.

Figure 10-5. Interrupt Timing

Because interrupt servicing is accomplished with the help of a memory cycle, the handshake in Figure 10-4 is similar to that in Figure 10-5. Since it is transparent to the memory whether or not an interrupt is being serviced, BUSY- and VALID- have exactly the same function in the two timing diagrams. MEMGO- has the same function as in a normal memory cycle except that during its assertion, the address bus is driven with the interface card's select code. The data which is read from this location in memory is used as the next instruction executed by the processor.

This instruction will normally be a jump (JSB, I) to the location of some interrupt service routine. When an interface card asserts INTRQ-, it also pulls on ICHOD-. ICHOD- will disable all lower-priority cards from requesting interrupt service. If a high-priority card preempts the request, ICHID- will go low, disabling the requesting card. The lower-priority card should maintain its request until its ICHID- goes back up and the card can be serviced.

If any contention exists between an IAK- assertion and an MRQ- assertion, the DMA request will win. Both IAK- and MRQ- assertions may occur simultaneously on the falling edge of SCLK-, but IAK- will be deasserted prior to the next rising edge of SCLK-. The assertion of IAK will be permitted at the completion of all current DMA requests. Refer to Table 10-13 for the aborted IAK- timing specifications.

10.5.4 INTERRUPT LATENCY

For this discussion, interrupt latency is defined as the time from the user interrupt request to the assertion of IAK by the processor. In the best case, the interrupt can be serviced as soon as it is received, so that with the 250-nanosecond SCLK time it is 5.25 microseconds. Generally, the interrupt cannot be serviced until a DMA cycle completes or until an instruction has finished executing.

In addition, interrupts are temporarily held off for one instruction time after a JMP,I, JSB,I, or I/O instruction is executed. Therefore, worst case interrupt latency is highly dependent on the software which is running at the time of the interrupt. Assuming no more than three channels of DMA self-configure at once, and no more than three adjacent instructions that hold off interrupts are executed back-to-back, the maximum interrupt latency is 29.75 microseconds.

MINIMUM	TYPICAL	MAXIMUM
5.25 us	7.0 us	30 us

10.5.5 REMOTE MEMORY ACCESS

All I/O interface cards have the capability of accessing a remote memory (i.e., a memory other than that plugged into the backplane directly above the processor card). In order to access the remote memory, an interface card must assert REMEM- with MEMGO-. The assertion of REMEM- will signal the local memory to ignore MEMGO-. Instead, a cycle with the remote memory will be initiated. This function is not currently used in the A700.

10.5.6 EXPANDED MEMORY ACCESS

To facilitate DMA access to expanded memory, each A700 I/O card has been designed with a five bit Address Extension Bus AE0-AE4 (previously called SC0 - SC4) that is driven onto the backplane simultaneously with the address bus during a memory access.

10.5.7 I/O TRANSFER PROTOCOL

The A700 I/O structure is such that I/O instructions are not executed by the CPU; instead, they are decoded by the interface card to which they apply, then executed by that interface card in conjunction with the CPU. The instruction decoding and executing capability of the interface card is provided by a silicon-on-sapphire (SOS) chip, the IOP chip, located on each interface card. The I/O handshake uses the two signals IORQ-, I/O request by an interface card, and IOGO-, go ahead signal from the processor card.

The processor card's IOGO- may be preempted by concurrent DMA activity. Both IOGO- and MRQ- are asserted on the falling edge of SCLK- ; thus the processor may come into contention with an I/O interface card if both signals occur simultaneously. The DMA activity has higher priority than the processor so that IOGO- must be deasserted prior to the next rising edge of SCLK-. When all concurrent DMA has completed, then IOGO- may be asserted on the backplane to complete the I/O handshake. Figure 10-6 illustrates a normal I/O handshake. For more information on a preempted I/O handshake and aborted IOGO-, refer to the timing specifications in Table 10-16.

10.5.8 I/O INSTRUCTION EXECUTION

The I/O instructions may be broken down into three groups in terms of their execution requirements, as follows:

A. Data Transfer I/O instructions - OTA/B, LIA/B, MIA/B

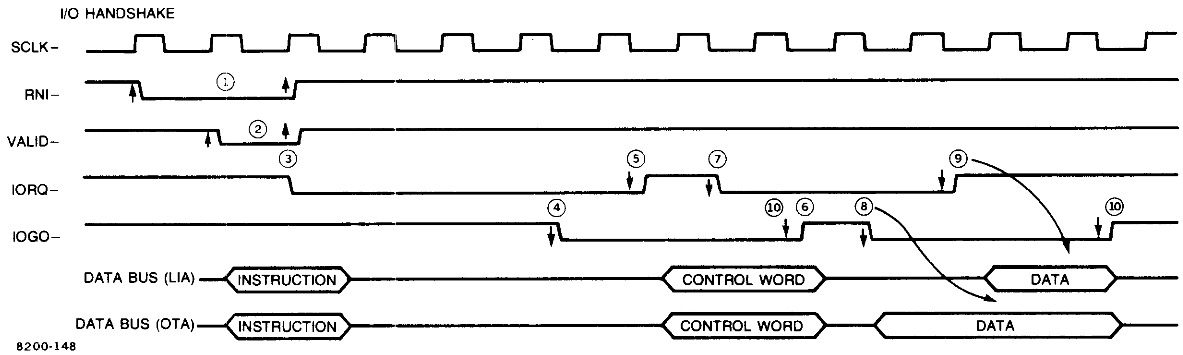
This group requires a double handshake as shown in Figure 10-6. In the first half of the handshake, a control word is transferred from the interface card to the processor card. In the second half of the handshake, the data is transferred either into or out of the A or B register, according to which of the six instructions above is being executed. I/O transfers over the backplane have lower priority than DMA transfers, and can be preempted. DMA transfers can occur while an I/O instruction is in the process of being executed (i.e., between the two halves of the handshake).

B. Status Sensing Instructions - SFS, SFC

This group requires, at most, a single handshake during which a control word from the interface card to the processor (signaling the program counter) is transferred. If no skip is required, no handshake occurs.

C. Status Altering Instructions - STC, CLC, STF, CLF

This group requires no interaction with the CPU. The interface card executes these instructions itself, and never needs to assert IORQ-.



1. Processor asserts RNI- to inform all system cards that an instruction is being fetched from memory.

2. Memory asserts VALID- to inform all system cards that data on the backplane will soon be valid. Each interface should now latch the instruction off the data bus, and decode it to see if it is an I/O instruction to its select code.

3. An interface card pulls on IORQ- to signal that it recognized the I/O instruction and needs the CPU in order to execute it.

4. The processor asserts IOGO- to indicate that it is ready to receive a command from the interface card.

5. The interface card releases IORQ- to signal the processor that the control word will be available on the data bus on the second rising edge of SCLK-.

6. The processor releases IOGO- when it has clocked the command off the backplane.

7. The interface card reasserts IORQ- one cycle after it was released if another handshake is needed in order to transfer a data word.

8. The processor reasserts IOGO- in order to indicate that it is ready to receive an operand in the case of an input operation, or that data will be valid on next falling edge in the case of an output operation.

9. The interface card releases IORQ- to indicate that it has latched an operand off the backplane in the case of an output operation, or that an operand will be valid on the backplane on second rising edge in the case of an input operation.

10. The processor releases IOGO- to indicate that it has clocked data off the backplane in the case of an input operation, or that the handshake is complete in the case of an output operation.

Figure 10-6. I/O Handshake

10.5.9 SLAVE MODE TRANSFERS

An interface card may force the processor card to enter an I/O handshake by pulling down the open-collector line SLAVE-. Once in slave mode, the interface has the capability of accessing the internal CPU registers, and does so with the use of the same handshake signals as in the I/O transfer protocol as illustrated in Figure 10-7.

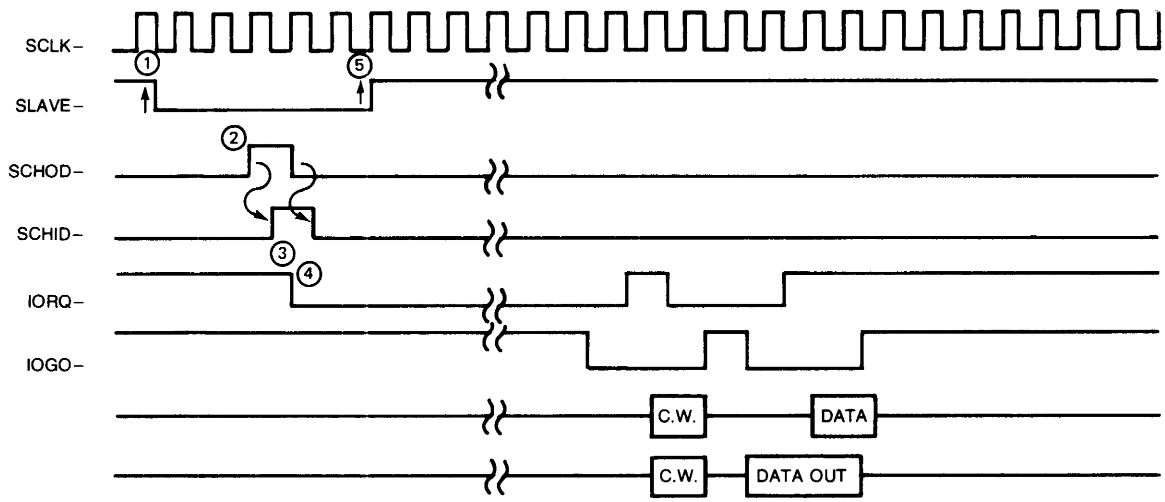
Once the slave mode has been entered, an interface card may keep the processor in that mode as long as desired by setting a bit in the control word (transferred during the first half of the handshake) which signals that another double handshake will occur. Note that the slave chain (SCHID-, SCHOD-) operates differently from the other chains in that its quiescent state is low or disabled. It is enabled only for one cycle at a time, during which the highest priority interface card pulling on SLAVE- must assert IORQ-, thereby entering slave mode. See Figure 10-7 for slave mode operation.

The control words which are sent to the CPU by an interface card during an I/O instruction (requiring a handshake), and during all slave mode processing are made up of five bits using bits 8 through 4 of the data bus.

Control words for slave mode processing are defined below:

	Data Bus Bit				
	8*	7	6	5	4
NOP	X	0	0	0	0
Load Program Counter	X	0	0	0	1
Load A	X	0	0	1	0
Load B	X	0	0	1	1
Clear O	X	0	1	0	0
Set O	X	0	1	0	1
OR into A/B	X	0	1	1	0
Increment Program Counter	X	0	1	1	1
Read E and O	X	1	0	0	0
Enable ROMs	X	1	0	0	1
Read A	X	1	0	1	0
Read B	X	1	0	1	1
Clear E	X	1	1	0	0
Set E	X	1	1	0	1
Read P	X	1	1	1	0
Read and Increment P	X	1	1	1	1

* Loop for next control word if X=1; last handshake if X=0.



NOTE: Same handshake protocols as an I/O handshake. Some slave mode transfers require only one set of IORQ−/IOGO− handshakes.

8200-81

1. An interface card asserts SLAVE- to request the processor to enter slave mode.

2. When the processor has completed executing the current instruction, it acknowledges the assertion of SLAVE- by de-asserting SCHOD- for one cycle.

3. Worse case, the SCHID/SCHOD priority chain has propogated down to the lowest-priority interface card by the end of that cycle, so that the last SCHID- will go high for one cycle.

4. The interface card received the enabling signal when its SCHID- signal went high, and can now pull on IORQ- in order to initiate the I/O handshake. The rest of the I/O handshake can then proceed exactly as shown in Figure 10-6.

5. The interface card de-asserts SLAVE- once it has asserted IORQ-.

Figure 10-7. Slave Mode Timing

10.6 SIGNAL TIMING SPECIFICATIONS

The A700 cards can be categorized into four types for backplane timing: memory, processor, analysis interface, and I/O Master. Each of these four types of cards has its timing requirements for the signals it receives and its timing guarantees for the signals it generates. In order to insure the basic integrity of all backplane interactions, it is necessary only to ascertain that all requirements are satisfied by the guarantees. All timing guarantees take into account the signal propogation delay due to line length and loading.

In Tables 10-5 through 10-36, timing specifications are given in terms of both requirements and guarantees. All backplane signals are listed in alphabetical order.

The definition of terms used in the timing specifications are provided below. All times are given in nanoseconds unless otherwise indicated.

DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS

C - Cycle
One cycle of Slow Clock (SCLK).

f - Frequency
The number of cycles per unit time of a given signal.

I/O - I/O Master
The A700 I/O Master consists of an SOS IOP chip and some TTL logic which together performs all the backplane I/O interfacing functions in the A700 computer.

LHC - Long Half Cycle
The Long Half Cycle refers to the time period when SCLK- is low.

M - Memory
A700 memory system.

P - Processor, type A700
The upper and lower processor cards.

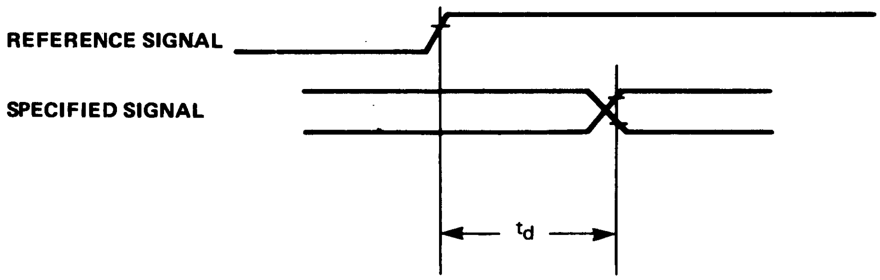
PS - Power Supply

SHC - Short Half Cycle
The Short Half Cycle is the time period when SCLK- is high.

DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS

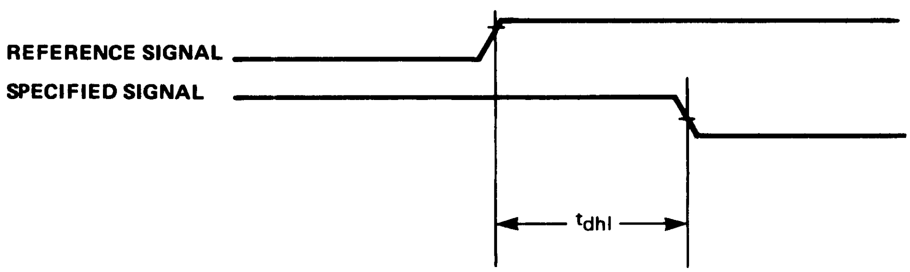
t_D - Delay time

The time interval from a signal edge used as a reference point to the point in time when the specified signal is guaranteed to be stable on the backplane.

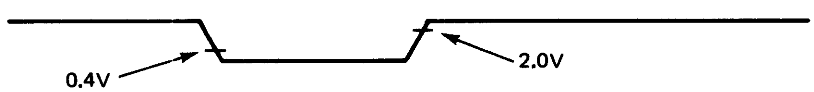


t_{DHL}- Delay time high to low

The time interval from a signal edge used as a reference point, to the point in time when the specified signal is guaranteed to be low if in fact it is going low.

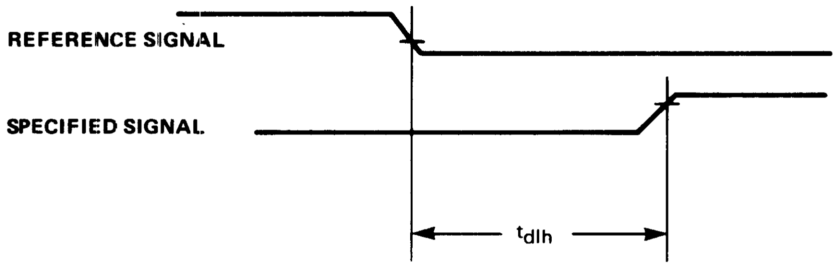


Note: In these timing diagrams, a high notch is 2.0 volts and a low notch is 0.4 volt as shown below.



t_{DLH} – Delay time low to high

The time interval from a signal edge used as a reference time to the point in time when the specified signal is guaranteed to be high if in fact it is going high.

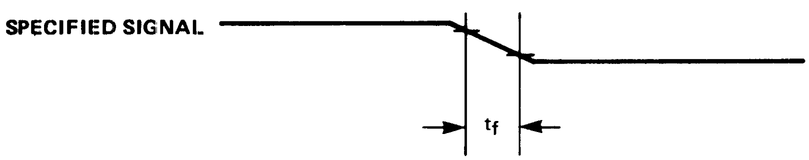


t_{DZ} Delay time to high impedance

The time interval from a signal edge used as reference to the point in time when the specified signal will no longer be actively driven.

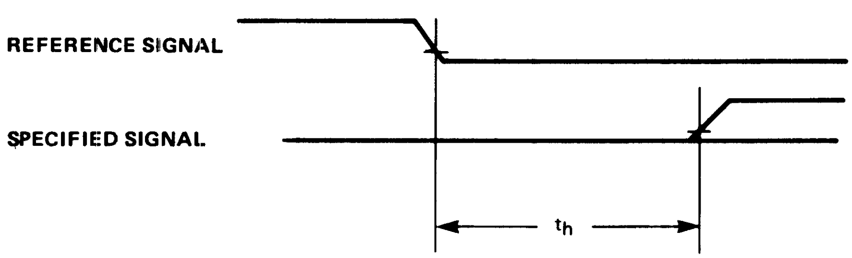
t_F – Fall time

The time interval during which a signal is in transition from high to low.



t_H – Hold time

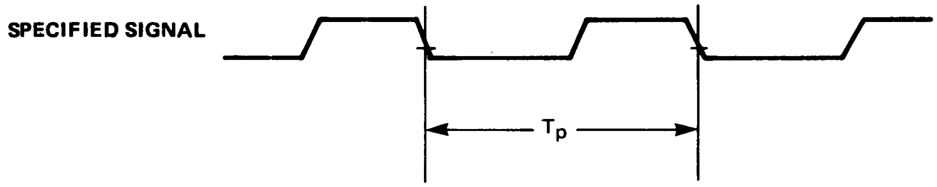
The period of time during which a specified signal must remain stable at its logic level after a certain reference edge.



DEFINITION OF TERMS USED IN TIMING SPECIFICATIONS (CONTINUED)

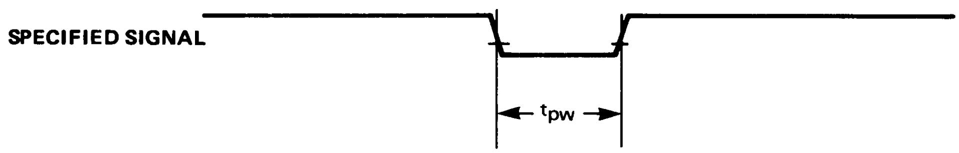
T_p - Period

The duration of one cycle of a periodic signal.



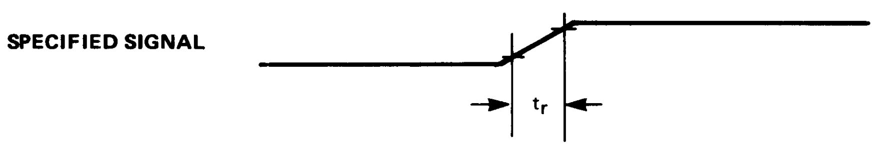
t_{pw} - Pulse width time

The time interval between the leading and trailing edge of a pulse. Specifically, for a normally high signal, tpw is the time when that signal is low. For a normally low signal, tpw is the time when that signal is high.



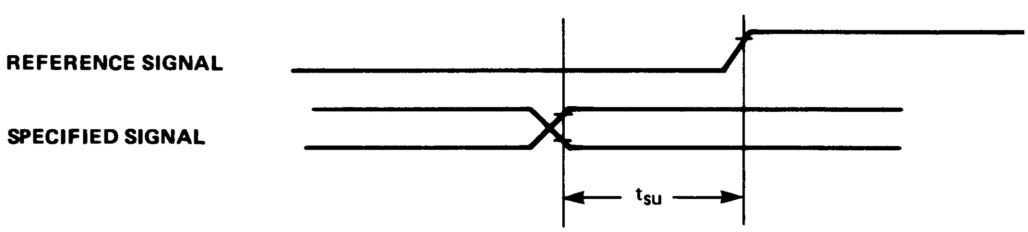
t_r - Rise time

The time interval during which a signal is in transition from low to high.



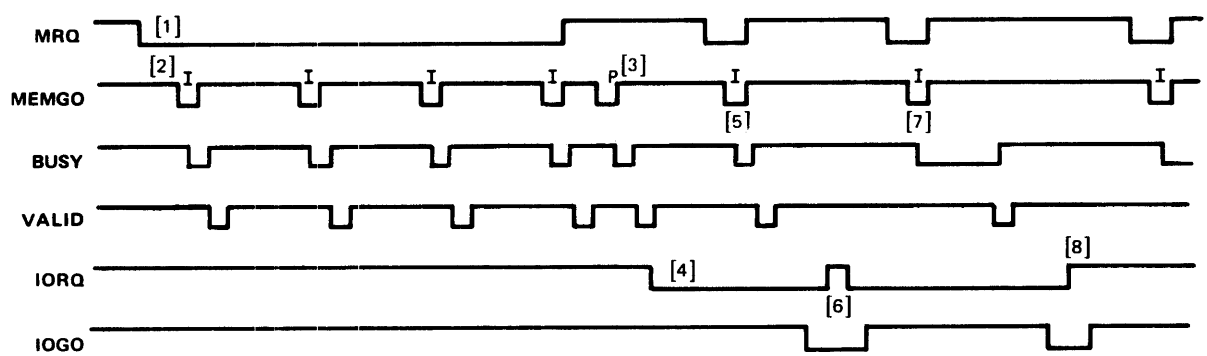
t_{su} - Set-up time

The time interval a specified signal must be at a stable logic level before a given edge of a reference signal.



10.6.1 INTERACTIVE TIMING EXAMPLES

Previous timing examples have shown handshakes or protocols by type of interaction. In actuality, however, transactions may start only to be preempted by other higher priority transactions and held off for an indefinite period of time. Figures 10-8 and 10-9 show various transactions over the backplane which begin, are preempted, and then later are allowed to complete.



1. MRQ- is held asserted for 21C during a four-word self- configuration.

2. All assertions of MEMGO- are labeled with their source; P for processor, I for I/O Master.

3. The processor fetches an LIA instruction.

4. The I/O Master asserts IORQ- upon recognition of the LIA, but the processor is held off from responding by [5].

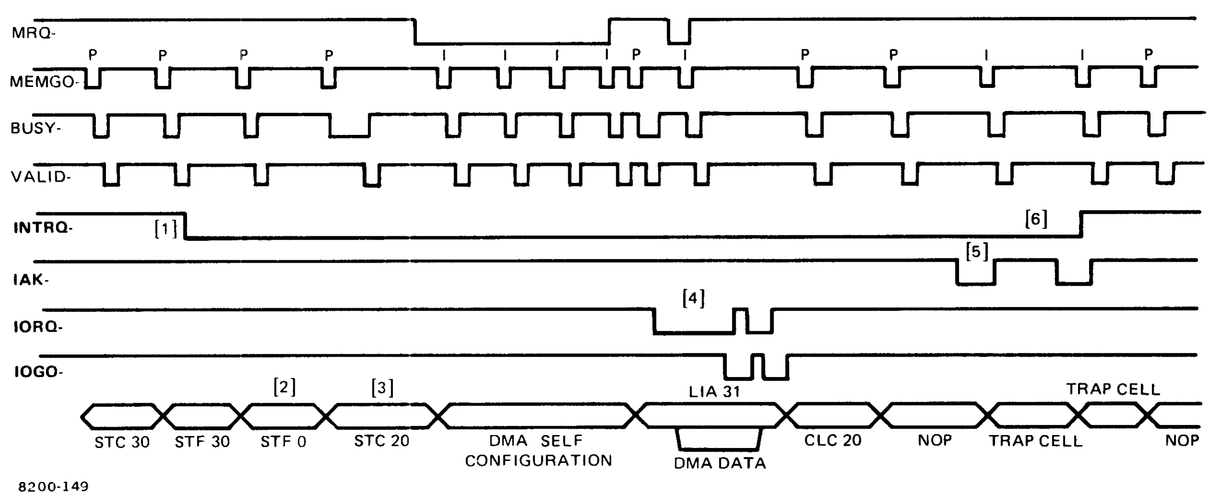
5. The first actual DMA data transfer takes place.

6. The first half of the I/O instruction handshake can now complete.

7. The second DMA data transfer takes place. It happened when memory was refreshing, so BUSY- is asserted for 5C instead of the usual 2C in order that the refresh can complete.

8. Now that this DMA transfer is complete, the I/O handshake can complete.

Figure 10-8. Interactive DMA and I/O Instruction Timing



1. The Flag and Control flip-flops are set, so the I/O Master attempts to interrupt.

2. Interrupt system is turned on with an STF 0 but processor must not respond until after the next instruction if current is an I/O instruction.

3. Self-configurating DMA is started, set up for a one-word transfer.

4. An LIA is executed, interleaved with DMA as in Figure 10-8.

5. After the NOP instruction is fetched, the processor can respond to the interrupt caused by Flag 30.

6. The I/O Master does not release INTRQ, because it now also has a DMA completion interrupt pending.

Figure 10-9. Interactive DMA, I/O Instruction, and Interrupt Timing

Table 10-5. Timing Specifications for AB0 - 14

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↑	Edges that occur during MEMGO		M	50		
t_D	SCLK-↓	Edge that causes MEMGO-↓	I/O				100
t_h	SCLK-↓	Edge that causes MEMGO-↑	I/O		0		
t_{su}	SCLK-↑	Edge that occurs during MEMGO-↓	P		53		
t_h	SCLK-↓	Edge that causes MEMGO-↑	P		20		
t_D	SCLK-↓	1st after BUSY-↑ following MRQ-↑	P				90
t_{DZ}	MRQ-↓	CPU can be held off by MRQ- from any interface	P		10		45
t_{DZ}	SCLK-↓	Due to MRQ-↓	P				95
t_H	SCLK-↑	Edge that causes IAK-↓	P				75

AE0 - AE4 ADDRESS EXTENSION BUS

This bus was previously called the select code bus SC0 - SC4. Refer to Table 10-30, Timing Specifications for SC0 - SC4.

Table 10-6. Timing Specifications for BUSY-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{DHL}	SCLK-↑	Edge that occurs during MEMGO-	M		0		60
t_{DLH}	SCLK-↑	2C later if memory was not doing refresh	M		0		60
t_{DLH}	SCLK-↑	3C-5C later if memory was doing refresh when MEMGO- occurred	M		0		60
t_{SU}	SCLK-↓	In order to hold off MEMGO-		I/O	5		
t_{h}	SCLK-↓			I/O	5		
t_{su}	SCLK-↑	Any falling edge		P	40		
t_{H}	SCLK-↑	Same edge		P	-4		
t_{pw}		Longer than 2C when doing refresh.	M		2C-50	2C	4C
t_{pw}		Longer than 2C when doing refresh.			2C-50		

Table 10-7. Timing Specifications for CCLK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	MIN	TYP	MAX
f	asynchronous	To all other backplane signals	P		14.7441 MHz	14.7456 MHz	14.7471 MHz
Duty cycle			P		30%	50%	

Table 10-8. Timing Specifications for CPUTURN-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{DHL}	SCLK-↑	That causes BUSY-↓	P				165
t_{DLH}	SCLK-↑		P				145
t_{SU}	SCLK-↓	To inhibit MRQ-		I/O	25		
t_{H}	SCLK-↓	Same edge		I/O	-5		
t_{DHL}	RNI-↓		P				10
t_{DLH}	RNI-↑		P				10

Table 10-9. Timing Specifications for CRS-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{pw}	asynchronous			M	1C		
t_{pw}				I/O	1C		
t_{SU}	SCLK-↓			I/O	-30		
t_{DHL}	SCLK-↑	No concurrent DMA	P				35
t_{DHL}	SCLK-↑	End of DMA	P				50
t_{DLH}	Next SCLK-↑		P				35

Table 10-10. Timing Specifications for DB0 - 15

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_D	SCLK-↑	During MEMGO-,DMA		M			50
t_D	SCLK-↑	Processor		M			100
t_{SU}	SCLK-↑	That causes VALID-↑	M		0		
t_H	SCLK-↑	That causes VALID-↑	M		100		
t_{SU}	VALID-↑	All cases	M		50		
t_D	SCLK-↓	Edge that causes MEMGO-↓ (DMA)	I/O				140
t_H	SCLK-↓	Edge that causes MEMGO-↑ (DMA)	I/O		35		
t_D	SCLK-↓	First SCLK-↓ after IOGO-↓* (I/O instruction)	I/O				315
t_H	SCLK-↑	Third SCLK-↑ during IOGO- (I/O instruction)	I/O		65		
t_{su}	VALID-↑	DMA read		I/O	50		
t_H	VALID-↑	DMA read		I/O	50		180
t_{su}	SCLK-↓	Second SCLK-↓* during IOGO- (I/O instr)		I/O	10		

*Provided IOGO-↓ met 10-ns set-up time to previous SCLK-↑.

Table 10-10. Timing Specifications for DBO - 15 (Continued)

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_H	SCLK-↑	Third SCLK-↑* during IOGO- (I/O instr)		I/O	40		250
t_{SU}	SCLK-↑	Edge that causes VALID-↑ (memory read)		P	20		
t_H	SCLK-↑	Same edge (memory read)		P	30		
t_{su}	SCLK-↑	Second SCLK-↑ after SCLK-↓ which causes IORQ-↑ (I/O instr)		P	10		
t_H	SCLK-↑	Same edge (I/O instr)		P	30		
t_D	SCLK-↑	Edge that causes MEMGO-↓ (memory write)	P				225
t_H	SCLK-↓	Edge that causes MEMGO-↑ (memory write)	P		160		
t_D	SCLK-↑	Edge that precedes SCLK-↓ which causes IOGO-↓ (I/O write)	P		30		180
t_H	SCLK-↑	Edge that precedes SCLK-↓ which causes IOGO-↑ (I/O write)	P		160		

*Provided IOGO-↓ met 10-ns set-up time to previous SCLK-↑.

Table 10-11. Timing Specifications for EC-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	MIN	TYP	MAX
t_{DHL}	SCLK↑	That causes assertion of VALID	Mem. array		132		278
t_{DLH}	FCLK-↑	Following SCLK-↑	Mem. array		2		8
t_{su}	FCLK-↑	Following SCLK-↑		LP	15		
t_H	FCLK-↑			LP	0		

Table 10-12. Timing Specifications for FCLK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	MIN	TYP	MAX
T_p				M	50		ns
f				M			20.0 MHz
f	While IOGO- is high		P		19.998 MHz	20.000 MHz	20.002 MHz
duty cycle			P		29%	50%	71%

Timing Specifications for FETCH

Note: Timing specifications for fetch are the same as for RNI-, refer to Table 10-29.

Table 10-13. Timing Specifications for IAK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns		
					MIN	TYP	MAX
t_{SU}	SCLK-↑			I/O	10		
t_{H}	SCLK-↑	Same edge		I/O	25		
t_{PW}				I/O	2C		3C
t_{SU}	SCLK-↓	To inhibit MRQ		I/O	25		
t_{H}	SCLK-↓	Same edge		I/O	0		
t_{D1}	SCLK-↑		P				50
t_{H}	SCLK-↑	First after VALID-↓	P		15		

Table 10-14. Timing Specifications for ICHID-/ICHOD-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns		
					MIN	TYP	MAX
ICHID- t_{SU}	SCLK-↓	Second SCLK-↓* during IAK-		I/O	10		
ICHID- t_{H}	SCLK-↓	Third SCLK-↓* during IAK-		I/O	50		
t_{D}	Asynch-ronous	ICHID-↓ to ICHOD-↓	I/O			5	7.5
ICHOD- t_{DHL}	SCLK-↑	Edge that causes INTRQ-↓	I/O				200
ICHOD- t_{H}	IAK-↑	ICHOD- is held low during the entire assertion of IAK-	I/O		SHC		

Table 10-15. Timing Specifications for INTRQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{DHL}	SCLK-↓		I/O				200
t_{DLH}	SCLK-↓	Third SCLK- after IAK-↓*	I/O				300
t_{su}	SCLK-↓			P	15		
t_{H}	IAK-↓			P	0		

*Provided IAK- met 10-ns set-up time to previous SCLK-↑.

Table 10-16. Timing Specifications for IOGO-

PARAMETER	REFERENCE	NOTES	BY	BY	MIN	TYP	MAX
t_{SU}	SCLK-↑	During IORQ-		I/O	10		
t_{h}	SCLK-↑	Same edge		I/O	25		
t_{pw}		3↑ of SCLK-		I/O	2C + LHC		
t_{SU}	SCLK-↓	To inhibit MRQ		I/O	25		
t_{H}	SCLK-↓	Same edge		I/O	0		
t_{DHL}	SCLK-↓		P				50
t_{DLH}	SCLK-↓	2nd SCLK-↓ after SCLK-↓ that caused IORQ-↑	P				40
t_{DHL}	SCLK-↓	2nd after BUSY-↑ following MRQ-↑	P				50
t_{DLH}	MRQ-↓		P				90
t_{DLH}	SCLK-↓	Due to MRQ-↓	P				85

Table 10-17. Timing Specifications for IORQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{DHL1}	Data bus valid during VALID-*	1 refers to first handshake request after RNI-↓	I/O				325
t_{DHL2}	SCLK-↓	2 refers to second SCLK-↓ after** IOGO-↓ (double handshake only)	I/O				145
t_{DHL3}	SCLK-↑	SCLK-↑ following SCHID-↑ (3 refers to initial IORQ-↓ on slave cycle)	I/O				45
t_{DLH}	SCLK-↓	First SCLK-↓ after IOGO-↓**	I/O				210
t_{SU}	SCLK-↓	5C+SHC after SCLK-↑ which causes RNI-↑ or VALID-↑		P	20		
t_h	SCLK-↓	Same edge		P	15		
t_{SU}	SCLK-↓	1C after edge which caused second assertion of IORQ-		P	20		
t_h	SCLK-↓	Same edge		P	15		
t_{SU}	SCLK-↓	Following any release of IORQ		P	20		
t_h	SCLK-↓	Same edge		P	15		

* During VALID-, there could be false assertions of IORQ- due to the data bus being in transition. This will not affect system operation, however, because the processor does not check IORQ- until two states after RNI-↑ when IORQ- is guaranteed to be valid.

** Provided IOGO-↓ met 10-ns set-up time to previous SCLK-↑.

Table 10-17. Timing Specifications for IORQ- (Continued)

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{SU}	SCLK-↓	First SCLK-↓ after SCHOD-↓		P	20		
t_h	SCLK-↓	Same edge		P	15		

Table 10-18. Timing Specifications for MCHID-/MCHOD-, MCHODOC-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
MCHID- t_{SU}	SCLK-↓			I/O	5		
MCHID- t_h	SCLK-↓	Same edge		I/O	20		
t_{DHL}		MCHID-↓ to MCHOD-↓	I/O			5	7
MCHOD- t_{DHL}	SCLK-↓	Edge that causes MRQ-↓	I/O				30
MCHODOC- t_{DHL}	SCLK-↓	Edge that causes MRQ-↓	I/O				55
MCHODOC- t_{DLH}	SCLK-↓	Edge that causes MRQ-↑	I/O				165

Table 10-19. Timing Specifications for MEMDIS-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{SU}	SCLK-↑	Edge that occurs during MEMGO-		M	30		
t_{h}	SCLK-↑	Same edge		M	0		
t_{DHL}	SCLK-↓	Next edge	P		5		
t_{DLH}	MRQ-↓		P				40

Table 10-20. Timing Specifications for MEMGO-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{SU}	SCLK-↑			M	10		
t_{h}	SCLK-↑	Same edge		M	SHC		215
t_{DHL}	SCLK-↓		I/O				45
t_{DLH}	SCLK-↓	Next edge	I/O		30		110
t_{DHL}	SCLK-↓		P				40
t_{DHL}	SCLK-↑$_{2}$	Following an I/O handshake	P				130
t_{DLH}	SCLK-↓	First SCLK-↓ after BUSY-↓	P				100
t_{DHL}	SCLK-↓	First after BUSY-↑ following MRQ-↑	P				45
t_{DLH}	MRQ-↓		P				95
t_{DLH}	SCLK-↓	MEMGO- aborted by MRQ- from edge which caused MEMGO	P				125

Table 10-21. Timing Specifications for MLOST-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME MIN	TIME TYP	TIME MAX
t_r, t_f			BB				50 ns
t_{su}	PON+↑		BB		500		us
t_h	PON+↑		BB		10 ms		1 s
t_h	PON+↑		SW*		5 ms		

* Processor does not latch MLOST-. During the pretest, the state of this line is used by the software to determine whether or not to initialize memory.

Table 10-22. Timing Specifications for MP+

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TIME IN ns TYP	TIME IN ns MAX
t_{SU}	VALID-↑			I/O	0		
t_H	SCLK-↑	Second SCLK-↑ after VALID-↑ (non-I/O instr). Second SCLK-↑ after last IOGO↑ (I/O instr)		I/O	0		
t_D	SCLK-↑		P				40

Table 10-23. Timing Specifications for MRQ-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{DHL}	SCLK-↓		I/O				50
t_{DLH}	SCLK-↓	Edge that causes MEMGO-↑	I/O		30		110
t_{SU}	SCLK-↑			P	85		
t_{H}	SCLK-↑	Edge that causes BUSY-↓		P	50		
t_{su}	SCLK-↑	Edge that occurs during MEMGO		M	30		
t_{H}	SCKL-↑	Edge that occurs during MEMGO		M	10		

Table 10-24. Timing Specifications for PE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{pw}	asynchronous	1C=250 ns	M		100		
t_{DHL}	VALID-↑	Actually caused by edge of FCLK-	M		0		40
t_{pw}		Must occur during window		I/O	50		
t_{SU}	Start window SCLK-↓	First edge after edge that causes RNI-↓ (instr fetch window)		I/O	0		
t_{h}	End window SCLK-↑	First edge after VALID-↑ (instr fetch window)		I/O	0		
t_{SU}	Start window SCLK-↓	First edge after edge that causes VALID-↓ (DMA window)		I/O	0		
t_{h}	End window SCLK-↓	Second edge after edge that causes VALID-↑ (DMA window)		I/O	0		
t_{su}	SCLK↓	First edge after VALID-↑		P	20		
t_{su}	End window SCLK-↓	First edge after VALID-↑		P	0		

Table 10-25. Timing Specifications for PFW-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{SU}	PON+↓		PS		5 ms		
t_{SU}	PON+↑		PS		10 ms		
t_r, t_f			PS				50
t_{su}	PON+↑			P	50		
t_{su}	PON+↓	Software requires time for power down routine to execute		SW	5 ms		

Table 10-26. Timing Specifications for PON+

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME MIN	TYP	MAX
t_D		Supplies up and within regulation	PS		50	65	100 ms
t_r, t_f			PS				50 ms
t_{pw}		Time required to fully initialize CPU chip		P	1C +30		ns

Table 10-27. Timing Specifications for PS-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
All		Same as data bus requirements for all memory writes		M			
t_D	SCLK-↑		P		0		20

Table 10-28. Timing Specifications for REMEM-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{su}	SCLK-↑	SCLK- that occurs during MEMGO-		M	30		
t_h	SCLK-↑	Same edge		M	0		
t_{DHL}	SCLK-↓		I/O				45
t_{DLH}	SCLK-↓	Next edge	I/O		30		110

Table 10-29. Timing Specifications for RNI-, FETCH-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{SU}	SCLK-↓	That occurs during VALID-		I/O	25		
t_H	SCLK-↓	Same edge		I/O	30		
t_{DHL}	SCLK-↑	First edge after MEMGO-↓ from CPU	P				45
t_{DLH}	SCLK-↑	Edge that causes VALID-↑	P				45
t_{pw}			P			1C	
t_{pw}				I/O	1C-t_{su}	1C	

Table 10-30. Timing Specifications for SC0 - SC4 (AE0 - AE4)
Note: In A-Series Computers this bus is labeled AE0 - AE4.

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	MIN	TYP	MAX
t_D	SCLK-↓	Edge that causes MEMGO-↓	I/O				90
t_H	SCLK-↓	Edge that causes MEMGO↑	I/O		20		
t_{su}	SCLK-↑	Edge that occurs during MEMGO-		M	50		
t_H	SCLK-↑	Edge that occurs during MEMGO-		M	-44		
t_{su}	SCLK-↑	Edge that occurs during MEMGO-↓	P		53		
t_h	SCLK-↓	Edge that causes MEMGO-↑	P		20		
t_D	SCLK-↓	1st after BUSY-↑ following MRQ-↑	P				90
t_{DZ}	MRQ-↓	CPU can be held off by MRQ- from any interface	P		10		45
t_{DZ}	SCLK-↓	Due to MRQ-↓	P				95
t_H	SCLK-↑	Edge that causes IAK-↓	P				75

(TIME IN ns: MIN, TYP, MAX)

Table 10-31. Timing Specifications for SCHID-/SCHOD-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	MIN	TYP	MAX
t_D		SCHID-↓ to SCHOD-↓	I/O			5	7.5
SCHOD- t_{DHL}*	SCLK-↑	Edge that caused SCHID-↑	I/O				25
SCHID- t_{SU}	SCLK-↑			I/O	0		

(TIME IN ns: MIN, TYP, MAX)

Table 10-31. Timing Specifications for SCHID-/SCHOD- (continued)

SCHID- t_H	SCLK-↑	Same edge		I/O	15
t_{DLH}	SCLK-↑		P		50
t_{DHL}	SCLK-↑	Next edge	P		50

* If a low priority interface asserts SLAVE-, a higher priority interface can get the slave cycle if the higher priority interface lowers SCHOD- at any time up until 1C-169 ns after the SCLK- which caused SCHID-.

Table 10-32. Timing Specifications for SCLK-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	MIN	TYP	MAX
f			P		-0.005%	4.000 MHz	+0.005%
t_p				I/O	227ns		
t_{pw}		LHC		I/O	135ns		
t_{pw}		SHC		I/O	90ns		

Table 10-33. Timing Specifications for SELFC

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{DHL}	SCLK-↓	Edge that causes MEMGO-↓	I/O				80
t_H	SCLK-↓	Edge that causes MEMGO↑	I/O		40		180
t_{su}	SCLK-↑	Edge that occurs during MEMGO-		M	50		
t_H	SCLK-↑	Edge that occurs during MEMGO-		M	100		
t_{su}	SCLK-↑	Edge that occurs during MEMGO-↓	P		53		

Table 10-33. Timing Specifications for SELFC (continued)

t_h	SCLK-↓	Edge that causes MEMGO-↑	P		20		
t_D	SCLK-↓	1st after BUSY-↑ following MRQ-↑	P				90
t_{DZ}	MRQ-↓	CPU can be held off by MRQ- from any interface	P		10		45
t_{DZ}	SCLK-↓	Due to MRQ-↓	P				95
t_H	SCLK-↑	Edge that causes IAK-↓	P				75

Table 10-34. Timing Specifications for SLAVE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{DHL}	SCLK-↑		I/O				45
t_{DLH}	SCLK-↑	First edge after SCHID-↓	I/O				130
t_{SU}	SCLK-↓			P	0		
t_h	SCLK-↑	Edge that causes SCHOD-↑		P	0		

Table 10-35. Timing Specifications for VALID-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{DHL}	SCLK-↑	First SCLK-↑ after BUSY-↓,no refresh. Second to fourth SCLK-↑ after BUSY-↓ with refresh.	M		50		70
t_{DLH}	SCLK-↑	Second SCLK-↑ after BUSY-↓ , no refresh. Third to fifth SCLK-↑ with refresh.	M		50		70

Table 10-35. Timing Specifications for VALID- (continued)

t_{SU}	SCLK-↓			I/O	10		
t_h	SCLK-↓	Same edge		I/O	30		
t_{SU}	SCLK-↑			P	60		
t_h	SCLK-↑	Same edge		P	-10		
t_{pw}				I/O	$1C-t_{su}$	1C	

Table 10-36. Timing Specifications for WE-

PARAMETER	REFERENCE	NOTES	GUAR BY	REQ'D BY	TIME IN ns MIN	TYP	MAX
t_{SU}	SCLK-↑	That occurs during MEMGO		M	20		
t_H	SCLK-↑	Same edge		M	10		
t_D	SCLK-↓	That causes MEMGO-↓	I/O				100
t_H	SCLK-↓	That causes MEMGO-↑	I/O		20		
t_D	SCLK-↓	That causes MEMGO-↓	P				100
t_H	SCLK-↓	That causes MEMGO↑	P		20		
t_D	SCLK-↓	After BUSY-↑ for MRQ-↑	P				90
t_{DZ}	MRQ-↓		P		10		45
t_{DZ}	SCLK-↓	Due to MRQ-↓	P				95
t_H	SCLK-↑	That causes IAK-↓	P				75

10.7 SIGNAL DEFINITIONS

Table 10-37 lists all backplane signals. The signals are listed in alphabetical order, along with their definitions, where they originated, where they go, functions, and general timing specifications. Timing values, when given, are nominal. For specific timing values, see Tables 10-5 through 10-37.

Table 10-37. Backplane Signal Definitions

(AB0+)-(AB14+)	
FULL NAME:	Address Bus 0-14 (Tri-state, high true)
DRIVEN BY:	The processor card or the I/O Master during a DMA transfer or while receiving interrupt service. (In the case of interrupt service, the card drives AB0 - AB5 with its select code and AB6 - AB14 with zeros.)
RECEIVED BY:	Memory and processor card.
FUNCTION:	The address bus is used to transfer a 15-bit absolute address to the memory, of which AB0 is the least significant bit. The processor will latch the address in case a parity error or memory protect violation occurs. (Will not check for these during DMA.)
TIMING:	The address bus is driven with the assertion of MEMGO- during a DMA transfer and during an interrupt cycle. In addition, the processor drives the address bus and asserts MEMGO when accessing the boot ROM. Note: The default address bus driver is the processor card, which drives the address bus at all times except the following: a. During the assertion of IAK-. b. During the assertion of MRQ-. c. From the assertion of BUSY- until the first SCLK-↓ after the release of BUSY-.
(AE0 - AE4)	
FULL NAME:	Address Extension Bus. This bus was previously called the SC (Select Code) Bus. Refer to (SC0 - SC4) for signal definition.

Table 10-37. Backplane Signal Definitions (Continued)

BUSY-	
FULL NAME:	Memory Busy (Tri-state, low true)
DRIVEN BY:	Processor and Memory cards
RECEIVED BY:	Processor and interface cards
FUNCTION:	BUSY- is asserted by the memory to indicate that it is unable to begin a new cycle.
TIMING:	BUSY- is asserted after the rising edge of SCLK-, following the assertion of MEMGO-. BUSY- is released following the rising edge of SCLK- that precedes the next possible memory cycle by one cycle of SCLK-.
CCLK-	
FULL NAME:	Communications Clock (low true)
DRIVEN BY:	Processor card
RECEIVED BY:	Interface cards
FUNCTION:	This clock provides a fixed frequency which may be used to drive a state machine, or which may be divided down for baud rate generation.
TIMING:	14.7456 MHz clock with a 50-percent duty cycle.
CPUTURN-	
FULL NAME:	Processor Turn
DRIVEN BY:	Processor Card
RECEIVED BY:	All interface cards
FUNCTION:	Asserted during RNI- and in addition, in order to signal that the processor card requests backplane priority. The assertion of CPUTURN- inhibits all interface cards from reasserting MRQ- once all current requests are satisfied.
TIMING:	When the processor wants to get out on the backplane for any one of three reasons (assessing memory, acknowledging an interrupt, or participating in an I/O handshake) but is held off by DMA, a counter counts 32 MEMGOs before asserting CPUTURN. CPUTURN stays asserted until the processor starts its transaction on the backplane.

Table 10-37. Backplane Signal Definitions (Continued)

CRS-

FULL NAME:	Control Reset (low true)
DRIVEN BY:	Processor Card
RECEIVED BY:	All cards
FUNCTION:	The assertion of CRS- completely resets the I/O system. All of the following will occur: 1. All interface control flip-flops will be cleared. 2. All interface flag flip-flops will be cleared. 3. All pending I/O interrupts will be cleared except power fail. 4. The global register will be disabled. 5. Parity valid LED on memory card will be turned on. In addition, each interface card interprets CRS- to perform its own various test functions.
TIMING:	CRS- is asserted for one cycle of SCLK- when a CLC 0 instruction is executed.

(DB0+)-(DB15+)

FULL NAME:	Data Bus 0-15 (Tri-state, high true)
DRIVEN BY:	Any memory or interface card or the processor card.
RECEIVED BY:	Any memory or interface card or the processor card.
FUNCTION:	DB0 to 15, of which DB0+ is the least significant bit, are used for all system data transfers.
TIMING:	An interface card will drive the data bus during the assertion of MEMGO- on a DMA write. The RAM card drives the data bus on a read cycle for one cycle, during the assertion of VALID-. The processor card drives the data bus with the assertion of MEMGO- on a memory write (STA), with IOGO- on an I/O write (OTA), and with VALID- clocked by start of long half-cycle on A or B fetch or Boot Read.

Table 10-37. Backplane Signal Definitions (Continued)

EC-	
FULL NAME:	Error Correct (low true)
DRIVEN BY:	Any Memory Card
RECEIVED BY:	Lower Processor Card
FUNCTION:	Asserted to indicate that the current memory read cycle requires an error correction. This causes the lower processor to extend the short half cycle of SCLK- by 150 ns.
TIMING:	Asserted by the memory array one FCLK- cycle after the start of the long half cycle of SCLK- which causes the assertion of VALID-. It is held until one FCLK- cycle after the start of t he next short half cycle.
FCLK-	
FULL NAME:	Fast clock
DRIVEN BY:	Processor card
RECEIVED BY:	Memory card
FUNCTION:	FCLK- is exactly five times the frequency of SCLK- and is used by the memory to synchronize various backplane functions.
TIMING:	FCLK- is a 50-percent duty cycle clock with a maximum frequency of 20.0 MHz. FCLK- is in synchronization with SCLK- such that a positive edge of FCLK- accompanies every transition of SCLK-.
FETCH-	
FULL NAME:	Fetch
DRIVEN BY:	Processor card
RECEIVED BY:	Logical analysis interface (not supplied by HP)
FUNCTION:	Asserted to indicate that the present memory reference is an instruction fetch.
TIMING:	Same as for RNI-.

Table 10-37. Backplane Signal Definitions (Continued)

IAK-	
FULL NAME:	Interrupt Acknowledge (low true)
DRIVEN BY:	Processor card
RECEIVED BY:	Any interrupting card
FUNCTION:	Asserted to signal that an interrupt request is about to be serviced and to freeze the interrupt priority chain.
TIMING:	IAK- is asserted by the processor card following the start of the short half cycle of SCLK-. It is held until after the trap cell instruction has commenced. (BUSY-↓ causes IAK-↑.)
ICHID-	
FULL NAME:	Interrupt Chain In Disable (low true)
DRIVEN BY:	The next higher priority card, to whom this signal is ICHOD-.
RECEIVED BY:	All interface cards
FUNCTION:	See ICHOD-
TIMING:	See ICHOD-
ICHOD-	
FULL NAME:	Interrupt Chain Out Disable (low true)
DRIVEN BY:	All interface cards, and the processor card (which is the top of the chain).
RECEIVED BY:	The next lower priority card, to whom this signal is ICHID-.
FUNCTION:	Asserted to disable lower priority cards from interrupting. A high on this line keeps interrupt generation enabled. ICHOD- is part of the ICHID-/ICHOD- daisy chain, used to determine interrupt priority.
TIMING:	Asserted by an interface card when its ICHID line goes low, or when its FLAG and CONTROL flip-flops get set. De-asserted when ICHID- goes high, and on either a CLF, CLC or PON+. Asserted by processor card on power fail, memory protect, parity error, UIT or TBG interrupts.

Table 10-37. Backplane Signal Definitions (Continued)

INTRQ-	
FULL NAME:	Interrupt Request (open-collector, low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	Processor card
FUNCTION:	Asserted to signal an interrupt request, and held low until the interrupt gets service, until PON+ goes low, or until a CLC 0 is executed.
TIMING:	Asserted by an interface card when both its CONTROL and FLAG flip-flops are set and its ICHID- signal is high. De-asserted when the CONTROL or FLAG flip-flop is cleared, or 2 cycles after the assertion of IAK- while ICHID- is high.

IOGO-	
FULL NAME:	I/O Handshake Request Acknowledge (low true)
DRIVEN BY:	Processor card
RECEIVED BY:	All interface cards
FUNCTION:	Asserted to signal that the processor card is ready to receive a command or send or receive an operand from an interface card. De-asserted when the transfer has been completed.
TIMING:	Pulled low when the data bus is available for transfers and released as soon as the data has been clocked off the backplane.
NOTE:	For some types of I/O transfers, this signal will participate in a double handshake (see Figure 10-6).

Table 10-37. Backplane Signal Definitions (Continued)

IORQ-	
FULL NAME:	I/O Handshake Request (open collector, low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	Processor card
FUNCTION:	Asserted to signal that an interface requires processor service, and de-asserted when being serviced.
TIMING:	Asserted within 2 cycles after the rising edge of RNI-, or in slave mode (refer to paragraph 10.4.8) on the next rising edge of SCLK- after SCHID- goes high. De-asserted to signal that data will be valid on the second rising edge of SCLK-, or during an input, to signal that data has just been latched. Refer to paragraph 10.4.7.
NOTE:	For some types of I/O transfers, this signal will participate in a double handshake. Refer to paragraph 10.4.7.
MCHID-	
FULL NAME:	Memory Chain In Disable (low true)
DRIVEN BY:	The next higher priority card, to whom this signal is MCHOD-.
RECEIVED BY:	All interface cards
FUNCTION:	Asserted to disable initiation of a memory cycle.
TIMING:	MCHID- is asserted a maximum of one cycle after MRQ- goes low. Released as soon as memory cycle of higher priority device is complete.

Table 10-37. Backplane Signal Definitions (Continued)

MCHOD-	
FULL NAME:	Memory Chain Out Disable (low true)
DRIVEN BY:	All interface cards and processor card.
RECEIVED BY:	The next lower priority card, to whom this signal is MCHID-.
FUNCTION:	Asserted to disable all lower priority cards from initiating a memory cycle.
TIMING:	An interface card wanting a DMA cycle asserts MCHOD- at the end of the short half cycle of SCLK-. MCHOD- is de-asserted at the end of the short half cycle, following the assertion of BUSY-. The processor card is the top of this priority chain. MCHOD- is tied high on the processor card.
NOTE:	All cards not using the memory priority chain must connect MCHOD- to MCHID-.
MCHODOC-	
FULL NAME:	Memory Chain Out Disable Open Collector (open collector, low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	Head of priority chain on lower priority stack.
FUNCTION:	Used as look-ahead for the memory priority chain. If any interface card in the higher priority stack asserts MCHODOC-, all interface cards in the lower priority stack will become disabled from initiating a memory cycle.
TIMING:	An interface card wanting a DMA cycle asserts MCHODOC- at the end of the short half cycle of SCLK-. MCHODOC- is released at the end of the short half cycle, following the assertion of BUSY-.
NOTE:	As far as the output of any given interface card is concerned, MCHODOC- is logically identical to MCHOD-. The pull-up resistor on this line is located on the 2 by 8 backplane. The two smaller backplane configurations are not large enough to require look-ahead in the memory priority chain, so this line is not terminated in these smaller configurations.

Table 10-37. Backplane Signal Definitions (Continued)

MEMDIS-	
FULL NAME:	Memory Disable (low true)
DRIVEN BY:	Processor card
RECEIVED BY:	Memory card
FUNCTION:	To initiate boot access on memory controller.
TIMING:	Asserted with MEMGO-.
NOTE:	MEMDIS- is not bussed up and down the backplane, instead, it runs above the SLAVE- chain (see PS- signal).
MEMGO-	
FULL NAME:	Memory Cycle Initiation (open collector, low true)
DRIVEN BY:	Processor and interface cards.
RECEIVED BY:	Memory, processor, and interface cards.
FUNCTION:	Pulled low to signal a memory request and released once service begins.
TIMING:	MEMGO- may be asserted by the card wishing to initiate a memory cycle after the falling edge of SCLK- that follows the release of BUSY-. MEMGO- is released by the processor card after the assertion of BUSY-. MEMGO- is released by an interface card after being held low for one cycle of SCLK-.
MLOST-	
FULL NAME;	Memory Lost (open collector, low true)
DRIVEN BY:	Processor, memory, and battery option in power supply (or battery back-up card).
RECEIVED BY:	Processor card, memory controller
FUNCTION:	MLOST- is asserted by the optional battery in power supply (or battery back-up card) to indicate that memory power was lost when system power last went down. Memory will then be cleared on the next power up. Where there is no back-up supply for the memory, MLOST- can be grounded. Do this by setting a switch on the processor card which grounds MLOST-, or by jumper settings on the memory card which shorts +5V to +5M and grounds MLOST-.
TIMING:	Asserted as soon as memory power fails. Released 10 ms after the rising edge of PON+.

Table 10-37. Backplane Signal Definitions (Continued)

MP+

FULL NAME: Memory Protect (open collector, high true)

DRIVEN BY: Processor card

RECEIVED BY: All interface cards, memory controller

FUNCTION: MP+ is asserted to indicate that the memory protect system is on. When MP+ is high, all I/O interface cards are inhibited from recognizing I/O instructions. DMA is not affected. Enables memory system protection.

TIMING: MP+ is asserted after an STC 05 instruction. It is released when IAK- is asserted, but re-asserted if an I/O group instruction is in the trap cell. MP+ is always in the proper state before RNI- is asserted and does not change until the next instruction fetch is initiated.

MRQ-

FULL NAME: Memory Request (open collector, low true)

DRIVEN BY: All interface cards

RECEIVED BY: Processor card, memory controller

FUNCTION: Asserted to indicate that an interface card performing DMA has requested a memory cycle. When MRQ- is low, the processor card is inhibited from requesting a memory cycle.

TIMING: An interface card wanting a DMA cycle asserts MRQ- at the start of the long half cycle of SCLK-. MRQ- is de-asserted on the falling edge of SCLK- after the assertion of BUSY-.

PE-

FULL NAME: Parity Error (open collector, low true)

DRIVEN BY: Memory controller.

RECEIVED BY: Processor and interface cards.

FUNCTION: Asserted if last memory read produced a parity error.

TIMING: PE- asserted for one short-half-cycle after release of VALID-.

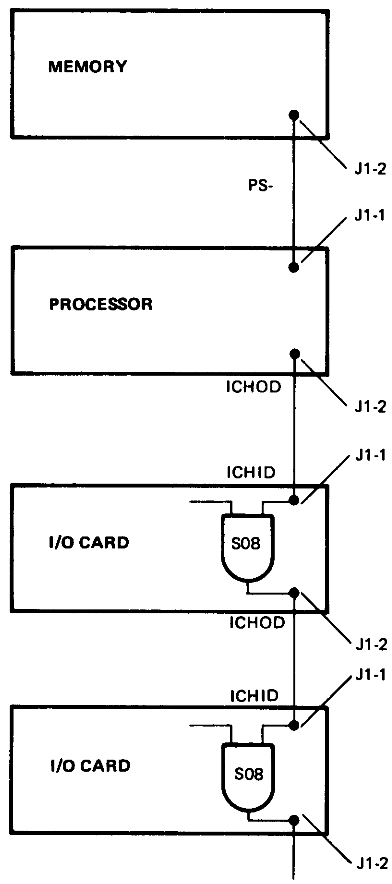
Table 10-37. Backplane Signal Definitions (Continued)

PFW-	
FULL NAME:	Power Fail Warning (open collector, low true)
DRIVEN BY:	Power supply
RECEIVED BY:	Processor card (and battery back-up card in Model 6 only).
FUNCTION:	Asserted to signal an ac line voltage failure.
TIMING:	Asserted at least 5 ms before the fall of PON+. Released before the rise of PON+.
NOTE:	The pull-up resistor on this open collector line is located on the processor card.
PON+	
FULL NAME:	Power On (open collector, high true)
DRIVEN BY:	Power supply and processor.
RECEIVED BY:	All cards in system.
FUNCTION:	PON+ is asserted by the power supply shortly after all power supply voltages are stable, to allow time for initialization on individual system cards. It is also pulsed low by a momentary switch located on the processor card in order to reset the computer.
TIMING:	Asserted 1 ms after all power supplies are stable. De-asserted if any supply falls below a tolerable level.
PS-	
FULL NAME:	Parity Sense
DRIVEN BY:	Processor card
RECEIVED BY:	Memory controller
FUNCTION:	A high level on PS- causes memory to generate and detect odd parity. A low on PS- causes memory to generate and detect even parity.
TIMING:	The level of PS- is selected by flag 5. An STF 5 selects even parity and a CLF 5 selects odd parity.

Table 10-37. Backplane Signal Definitions (Continued)

PS- (continued)

NOTE:	On power up, PS- is set for odd parity. Also note that PS- is not bussed up and down the backplane. Instead, it is sent by the processor card only to the memory card located above it. See Figure below.



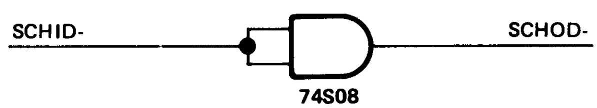
REMEM-

FULL NAME:	Remote Memory (open collector, low true)
DRIVEN BY:	Interface cards
RECEIVED BY:	Memory
FUNCTION:	REMEM- is asserted to indicate that the simultaneous MEMGO- which occurs should initiate a memory cycle with the remote memory. Any memory card in the system should ignore MEMGO- if it occurs with REMEM-.
TIMING:	REMEM- is asserted and released with MEMGO-.

Table 10-37. Backplane Signal Definitions (Continued)

RNI-	
FULL NAME:	Read Next Instruction (low true)
DRIVEN BY:	Processor card.
RECEIVED BY:	All interface cards.
FUNCTION:	RNI- is asserted to indicate that the current memory cycle is a fetch and that an instruction will be on the data bus.
TIMING:	RNI- is asserted with the fetch address for I/O instructions. It is released after the start of the short half cycle of SCLK- after VALID- is asserted.
NOTE:	The instruction is to be latched on the trailing (rising) edge of RNI-.
(SC0+) - (SC4+) or (AE0+) - (AE4+)	
FULL NAME:	Address Extension Bus 0 - 4
DRIVEN BY:	Interface Cards and Processor
RECEIVED BY:	Memory Controller
FUNCTION:	The AE (SC) bus is used to select one of 32 map sets.
TIMING:	The Address Extension Bus is driven simultaneously with AB0 - AB14.
SCHID-	
FULL NAME:	Slave Chain In Disable (low true)
DRIVEN BY:	The next higher priority card, to whom this signal is SCHOD-.
RECEIVED BY:	All interface cards
FUNCTION:	See SCHOD-
TIMING:	See SCHOD-

Table 10-37. Backplane Signal Definitions (Continued)

SCHOD-	
FULL NAME:	Slave Chain Out Disable (low true)
DRIVEN BY:	All interface cards
RECEIVED BY:	The next lower priority card, to whom this signal is SCHID-.
FUNCTION:	SCHOD- is asserted to disable lower priority cards from entering slave mode. SCHOD- is part of the SCHID-/SCHOD- priority chain, used to settle conflicts for slave mode processing (see paragraph 10.5.9).
TIMING:	SCHOD- is asserted with SLAVE-, or if a higher priority card pulls on SCHID-, and is held as long thereafter as it takes the daisy chain to ripple down. Likewise, SCHOD- is released with SLAVE- or SCHID-.
NOTE:	The top of the priority chain is the processor card. Whenever SLAVE- is asserted, and the processor card has completed executing the current instruction, SCHOD- goes high for one cycle of SCLK-. There must be exactly one non-inverting Schottky gate on each card between SCHID- and SCHOD-. Example: 
SCLK-	
FULL NAME:	Slow clock
DRIVEN BY:	Processor card
RECEIVED BY:	All system cards
FUNCTION:	SCLK- is used to synchronize many diverse system signal interactions.
TIMING:	SCLK- is a derivative of FCLK. It is generated with a divide-by-5 circuit which produces a signal with a minimum of a 250-nanosecond period and a 40-percent duty cycle. (continued next page)

SCLK (continued)	
NOTE :	In all timing descriptions, the term "short half-cycle" refers to the time (2/5 period) when SCLK- is high. The "long half-cycle" refers to the 3/5 period when SCLK- is low. So as to minimize clock skew, all cards are required to receive SCLK- into an S240.
	INSERT FIG.
SELFC -	
FULL NAME:	Self Configure (open collector, low true)
DRIVEN BY:	Interface Cards
RECEIVED BY:	Memory Controller
FUNCTION:	SELFC- is asserted to indicate that DMA self-configuration is occurring. The memory controller enables MAP 0 to use during DMA self configuration.
TIMING:	SELFC- is driven simultaneously with AB0 - AB14.
SLAVE-	
FULL NAME:	Slave Request (open collector, low true)
DRIVEN BY:	Interface cards
RECEIVED BY:	Processor card
FUNCTION:	SLAVE- is asserted to request the processor to enter slave mode, i.e., to force the processor to enter an I/O handshake.
TIMING:	SLAVE- is held asserted until the start of the long half cycle of SCLK- following the release of SCHID-.

Table 10-37. Backplane Signal Definitions (Continued)

VALID-	
FULL NAME:	Data Valid (Tri-state, low true)
DRIVEN BY:	Memory controller
RECEIVED BY:	Processor and interface cards
FUNCTION:	VALID- is asserted to signal that the data on the data bus is about to become valid during a memory read cycle.
TIMING:	On a read cycle, the memory will assert VALID- after the rising edge of SCLK- that precedes the appearance of valid data on the backplane by one cycle. VALID- will be held low for one cycle and then released after the rising edge of SCLK- right after data becomes valid. VALID- is asserted during write.
WE-	
FULL NAME:	Write Enable (Tri-state, low true)
DRIVEN BY:	Any card accessing memory
RECEIVED BY:	Memory controller
FUNCTION:	WE- is asserted to signal a memory write, and held high to signal a memory read.
TIMING:	WE- is asserted and released with (AB0+)-(AB14+).

10.8 PARTS LOCATIONS

Parts locations for the backplane are shown in Figure 10-2.

10.9 PARTS LIST

Parts lists for the backplanes are provided in Table 10-38, and Table 10-39 for the 20-slot card and 16-slot backplanes, respectively. Refer to Table 10-40 for the names and addresses of manufacturers of the parts in the Manufacturer's Code List.

10.10 DIMENSIONS AND ASSEMBLY

The dimensions for the CPU, Memory and I/O cards are as follows:

Length	289mm	(11.38 inches)
Width	172mm	(6.75 inches)
Thickness	1.6mm	(9.063 inch)
Parts Clearance:		
Top-of-card	10.2mm	(0.4 inch)
Beneath card	5.1mm	(0.2 inch

The backplane and card cage dimensions are the following:

20-Slot Backplane

Length	419mm	(16.5 inches)
Width	203mm	(8.0 inches)

16-Slot Backplane

Length	375mm	(14.75 inches)
Width	140mm	(5.50 inches)

12030A Card Cage (Power Module excluded)

Width	362mm	(14.25 inches)
Height	117mm	(4.63 inches)
Depth	313mm	(12.3 inches)

2137A (20-Slot Rack Mounted Box)

Width	483mm	(19 inches)
Height	117mm	(10.5 inches)
Depth	6120mm	(24 inches)

2437A, 2487A (16-Slot Rack Mounted Box)

Width	483mm	(19 inches)
Height	178mm	(7 inches)
Depth	648mm	(25.5 inches)

Figure 10-10 shows the assembly of the rack mounting 20-slot box and Figure 10-11 shows the assembly of the rack mounted 16-slot box.

Table 10-38. 20-Slot Backplane Replaceable Parts

REF. DESIG.	HP PART NUMBER	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
A1	12151-80002	1	20-SLOT BACKPLANE	28480	12151-80002
-	1215-8053	42	CONNECTOR, PC, 2 X 25	28480	1215-8053
CR1	1902-0939	1	DIODE-ZENER 5.0V	03287	1N5908
CR2	1902-0941	2	DIODE TRANSIENT SUP	03287	GS ICTE-12
CR3	1902-0941		DIODE TRANSIENT SUP	03287	GS ICTE-12
R1	1810-0271	1	RES NETWORK 9 X 200	04200	1810-0271
R2	1810-0272	1	RES NETWORK 9 X 330	04200	1810-0272
W1	1811-3587	1	RESISTOR-FXD 0 OHM	03123	104

Table 10-39. 16-Slot Backplane Replaceable Parts

REF. DESIG.	HP PART NUMBER	QTY	DESCRIPTION	MFR CODE	MFR PART NUMBER
	1251-8053	21	Connector-PC,2X25	28480	1251-8053
P1-P3	1251-8331	3	Connector-4 pin	00779	350424-2
J4	1251-8346	1	Connector-35 pin	00779	531920-1
J5	1251-8396	1	Connector-PC Edge	28480	1251-8053
CR1	1902-0939	2	D1ODE,IN5908	03287	IN5908
CR2	1902-0941	2	D1ODE,Transient Sup.	03287	GSICTE-12
CR3	1902-0941		D1ODE,Transient Sup.	03287	GSICTE-12
CR4	1902-0939		D1ODE,IN5908	03287	IN5908
R1	0757-0280	1	Resistor,1K,125W F TC=0+ -100	24546	C4 1/8 to 1001 F
U1	1810-0182	1	Res Net 220/330X12	04200	1810-0182
U1	0811-3587	1	Resistor 0 OHM	03123	104

Table 10-40. Manufacturer's Code List

The following code numbers are from the Federal Supply Code for Manufacturers Cataloging Handbooks H4-1 and H4-2, and their supplements.

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00779	AMP Inc	Harrisburg, PA	17105
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03123	Micro Ohm	El Monte, CA	91734
03287	General Semiconductor	Tempe, AZ	85282
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04200	Sprague Electric	North Adams, MA	01247
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
18324	Signetics Corp	Sunnyvale, CA	94086
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
31585	RCA Corp Solid State Div	Somerville, NJ	08876
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34344	Motorola Inc	Franklin Park, IL	60131
56289	Sprague Electric Co	North Adams, MA	01247

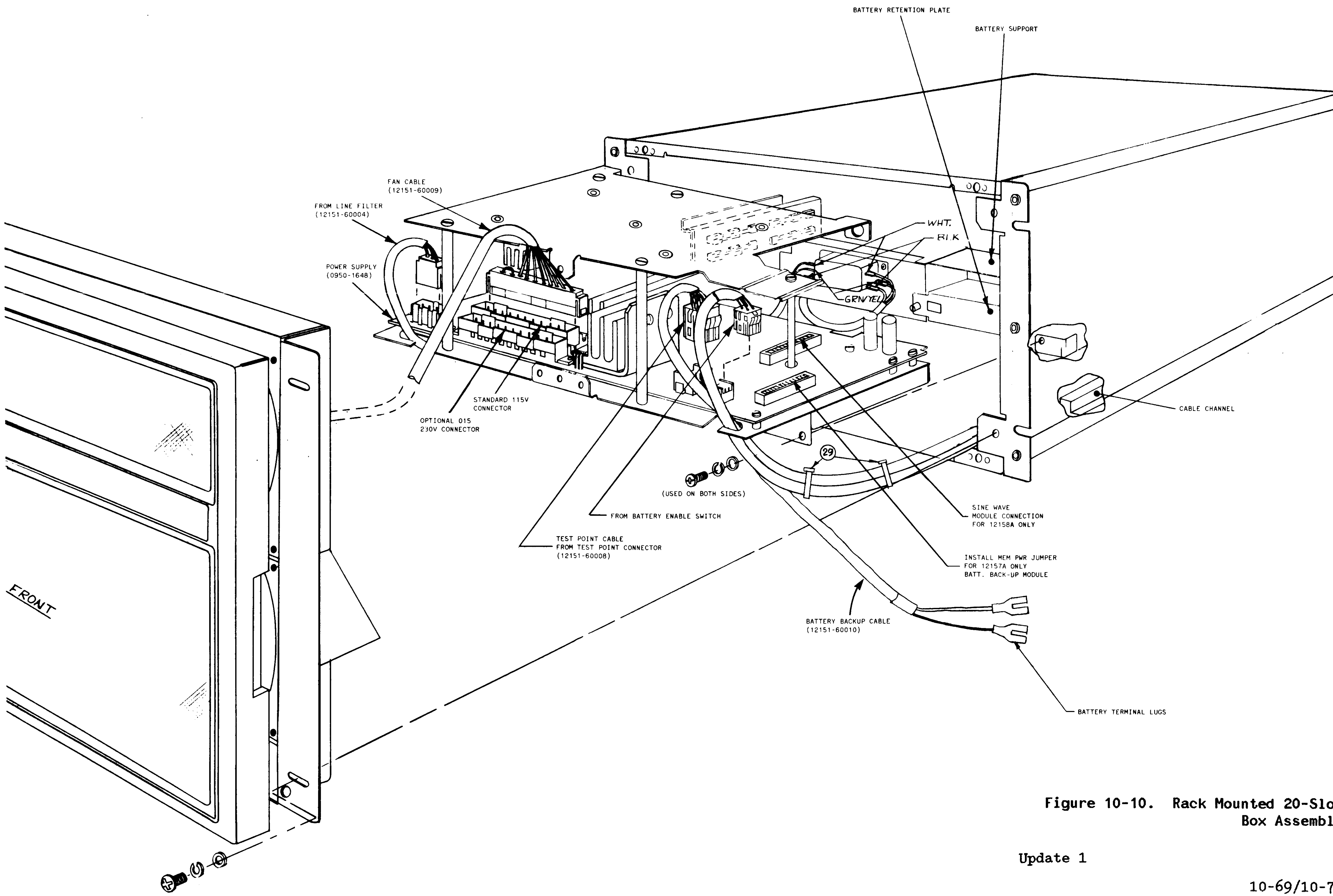
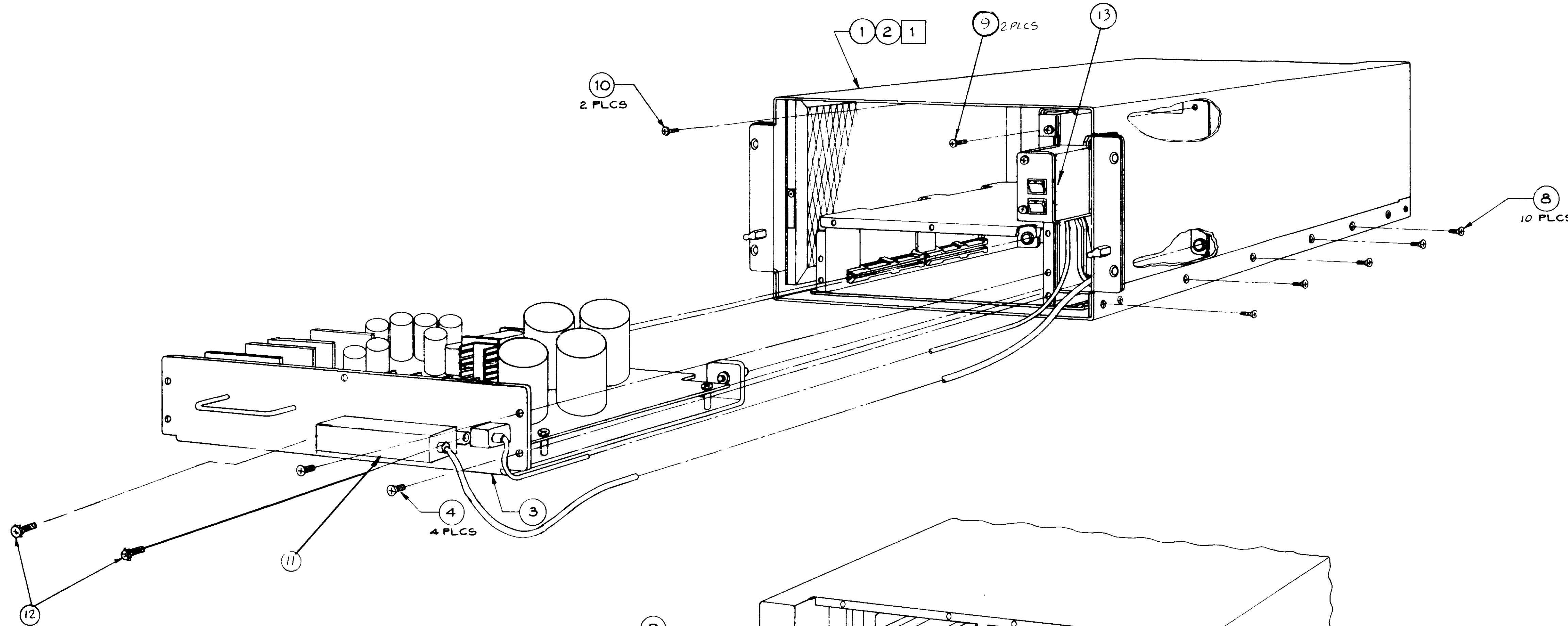
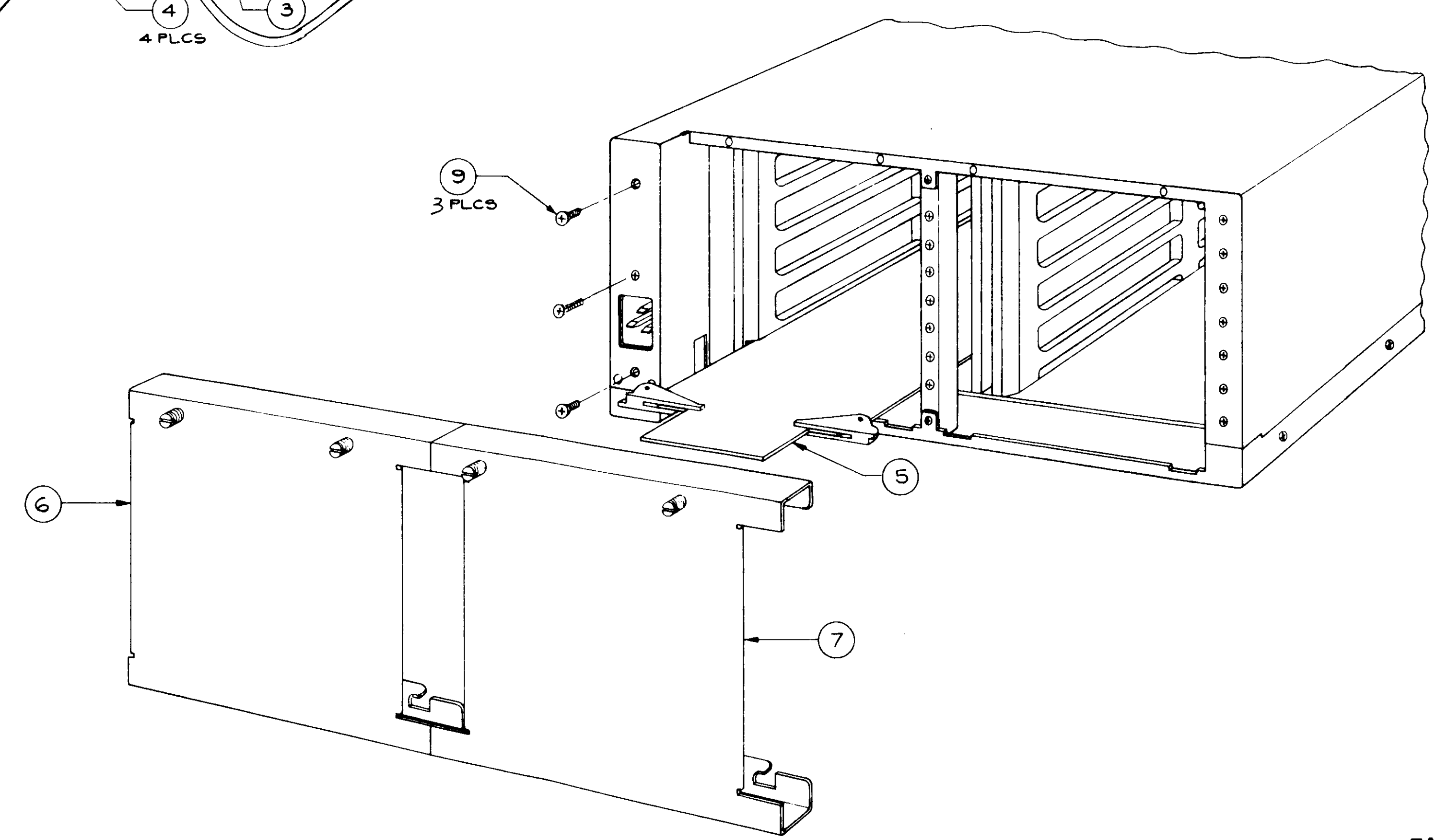


Figure 10-10. Rack Mounted 20-Slot Box Assembly



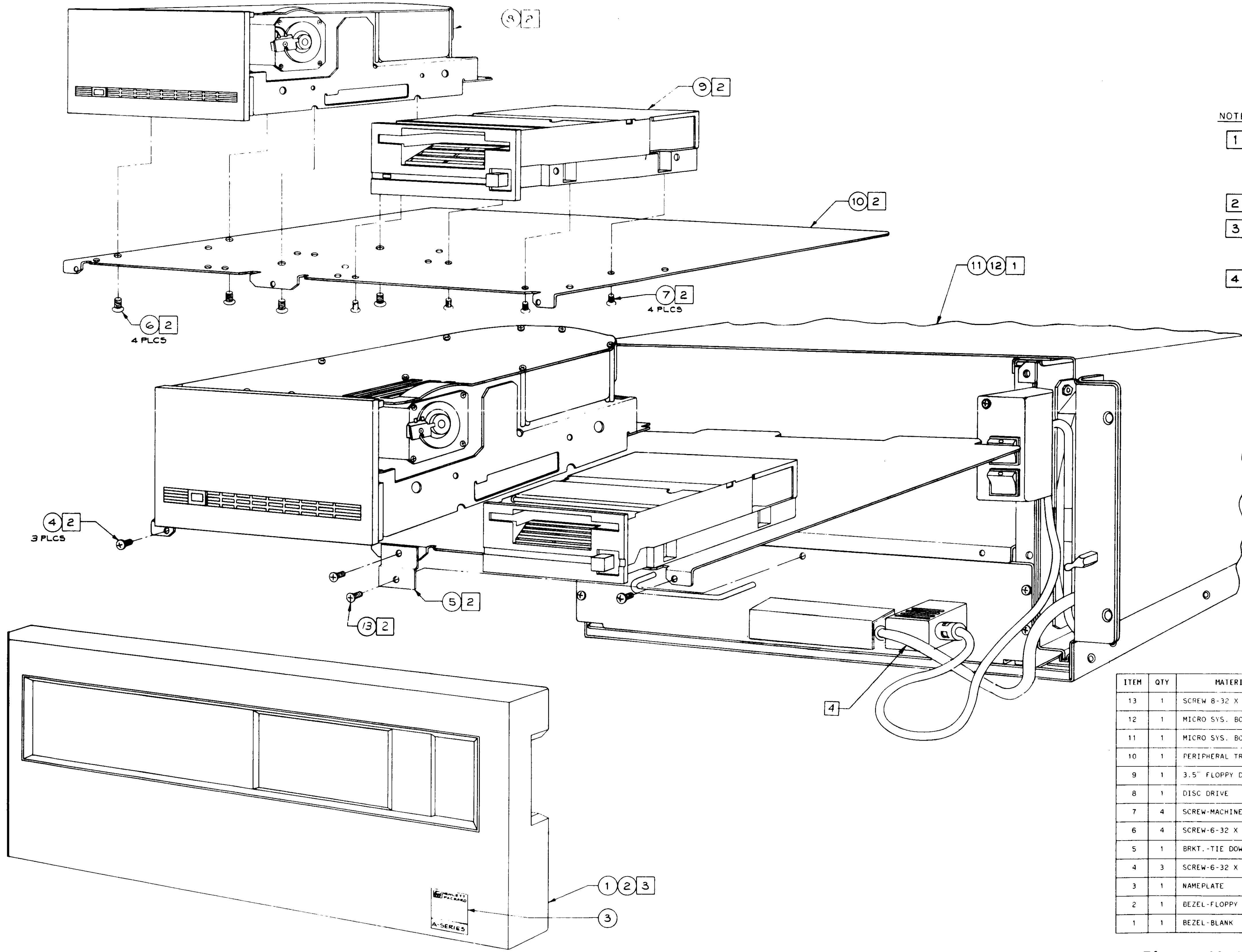


NOTE

[1] 2430A USES 02430-60001 BOX ASSY.
2430B USES 02430-60003 BOX ASSY.

ITEM	QTY	MATERIAL DESCRIPTION	PART NUMBER
13	1	PDU/FAN ASSY	02430-60005
12	2	SCREW 4.40 X .250 W/LK	2200-0103
11	1	COVER CONN.	02430-00028
10	2	SCR 6-32	2360-0429
9	5	SCR 6-32 X .250 PH	2360-0113
8	10	SCR 6-32 X .250L FH	2360-0192
7	1	PANEL - REAR, RIGHT	02430-00021 REF.
6	1	PANEL - REAR, LEFT	02430-00012 REF.
5	1	PCA MEM. PWR. JUMP	02430-60009
4	4	SCR 6-32 X .375L	2360-0117
3	1	PWR. SUPPLY - 300W	0950-1646
2	1	ASSY. - BOX A900	02430-60003
1	1	ASSY. - BOX A600/A700	02430-60001

Figure 10-11. Rack Mounted 16-Slot Box Assembly (Sheet 1 of 4)



NOTES:

1. USE 2430A (11) FOR A600/A700 COMP
AND SYSTEMS -2436A/E, 2437A, 248
2487A. USE 2430B (12) FOR A900 C
AND SYSTEM - 2439A AND 2489A.

2. INSTALL FOR OPTION 110 ONLY.

3. USE ITEM (1) FOR STANDARD COMPU
AND SYSTEM. USE ITEM (2) FOR OP
110 OF COMPUTER AND SYSTEM.

4. FOR 230V AC OPERATION, (OPTION 01
SWITCH CABLE INSTALLATION.

ITEM	QTY	MATERIAL-DESCRIPTION	MAT´L-PART NO.
13	1	SCREW 8-32 X .375	2510-0045
12	1	MICRO SYS. BOX (A900)	2430B
11	1	MICRO SYS. BOX (A600/A700)	2430A
10	1	PERIPHERAL TRAY	02430-00013
9	1	3.5" FLOPPY DRIVE	88121DT
8	1	DISC DRIVE	88234DT 015
7	4	SCREW-MACHINE M3 X 0.5	0515-0076
6	4	SCREW-6-32 X .250	2360-0192
5	1	BRKT.-TIE DOWN	02430-00025
4	3	SCREW-6-32 X .312	2360-0115
3	1	NAMEPLATE	5180-4242
2	1	BEZEL-FLOPPY	02430-40002
1	1	BEZEL-BLANK	02430-40001

Figure 10-11. Rack Mounted 16-Slot Box Assembly (Sheet 2 of 4)

ITEM	QTY	MATERIAL-DESCRIPTION	MATL'-PART NO.
11	3	CLAMP-CABLE	1400-1157
10	1	MICRO SYS. BOX (A600/A700)	2430A
9	1	MICRO SYS. BOX (A900)	2430B
8	1	FIXED DISC DRIVE	88234DT 015
7	1	3.5" FLOPPY DISC DRIVE	88121DT
6	1	CABLE-POWER, FIXED DISC	12022-60004
5	1	CABLE-POWER, MICROFLOPPY	12022-60006
4	1	DISCINTERFACE CARD	12022-60001
3	1	CABLE-CONTROL, FIXED DISC	12022-60002
2	1	CABLE-DATA, FIXED DISC	12022-60003
1	1	CABLE-SIGNAL, MICROFLOPPY	12022-60005

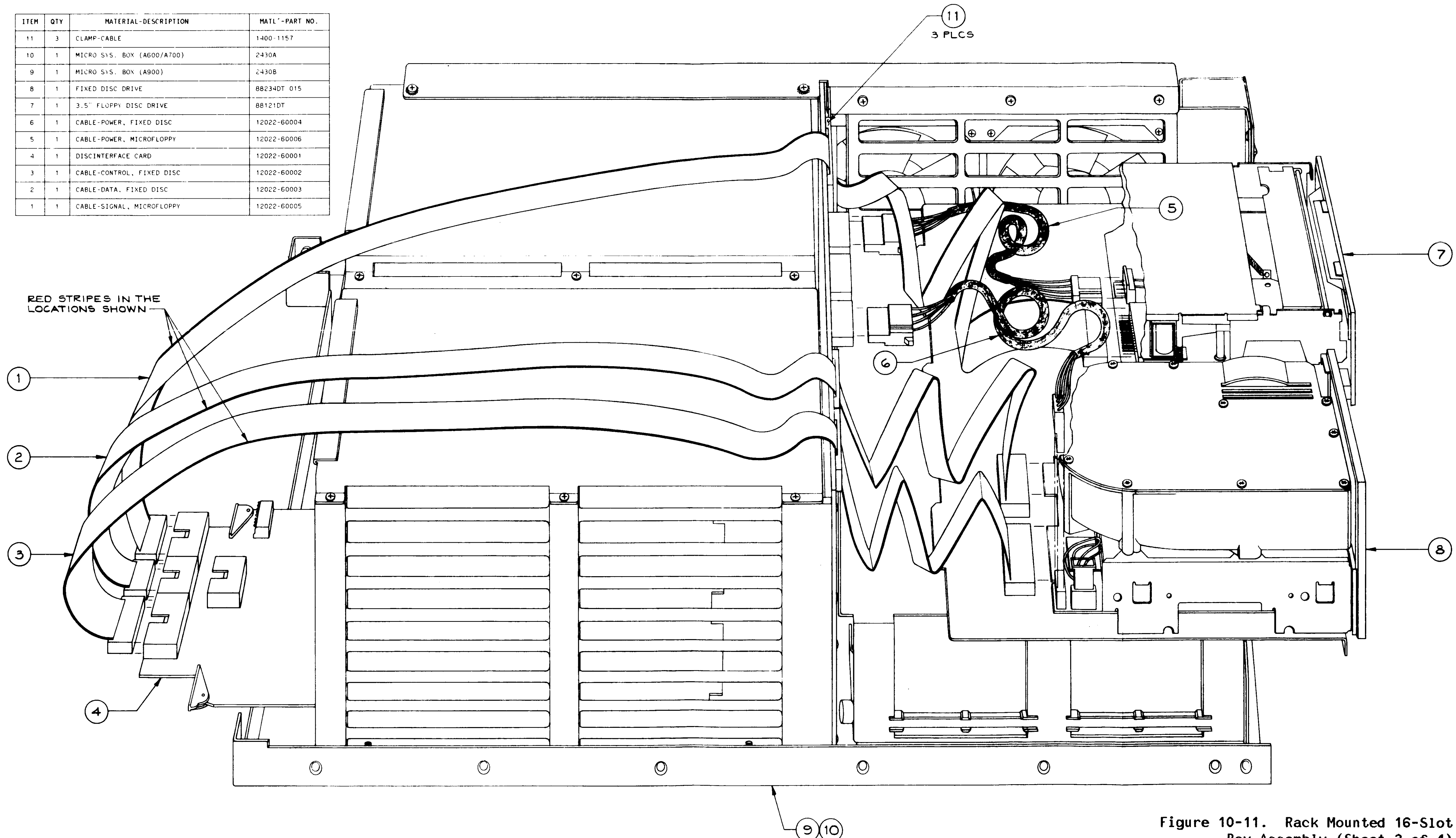
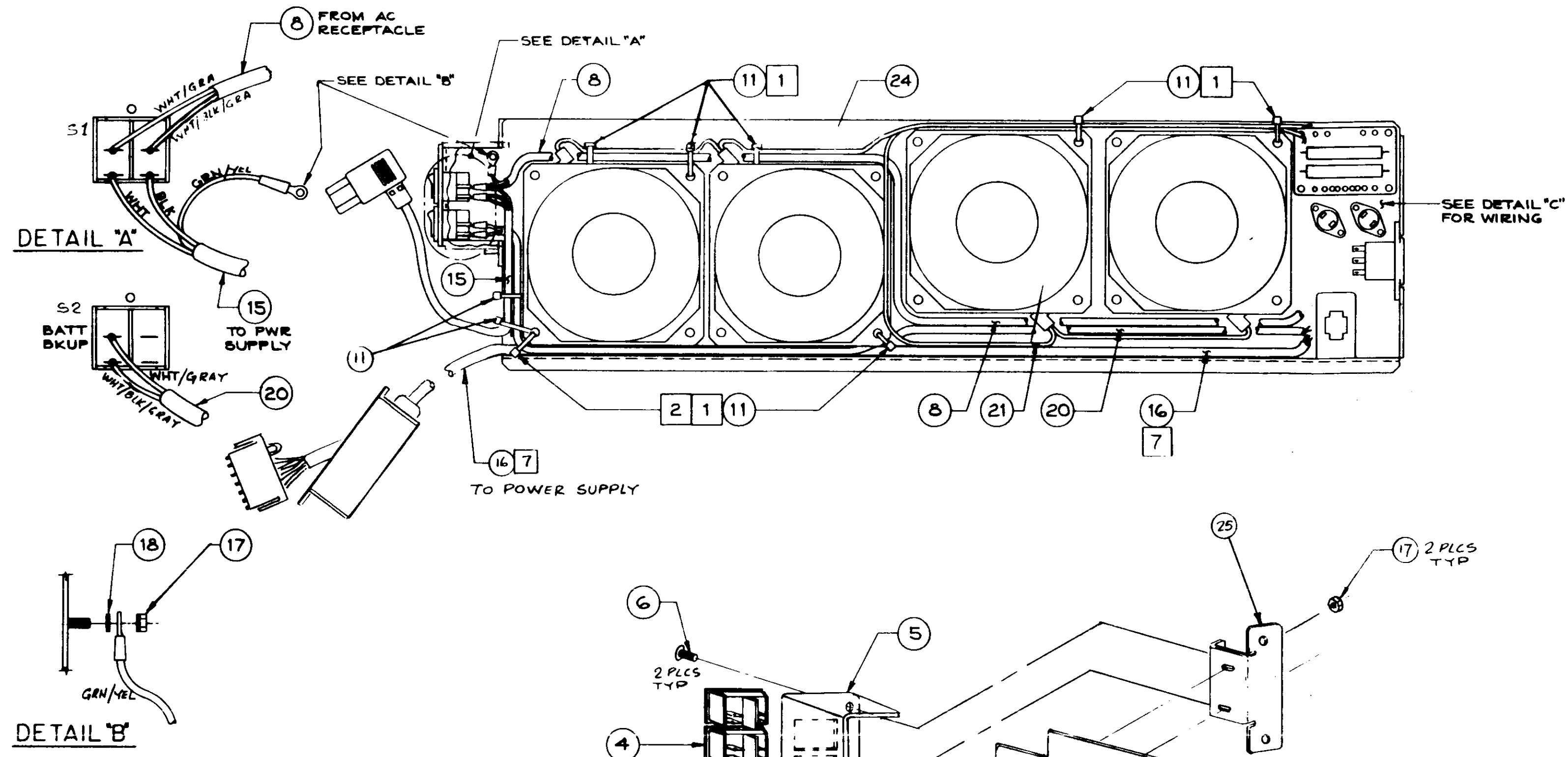
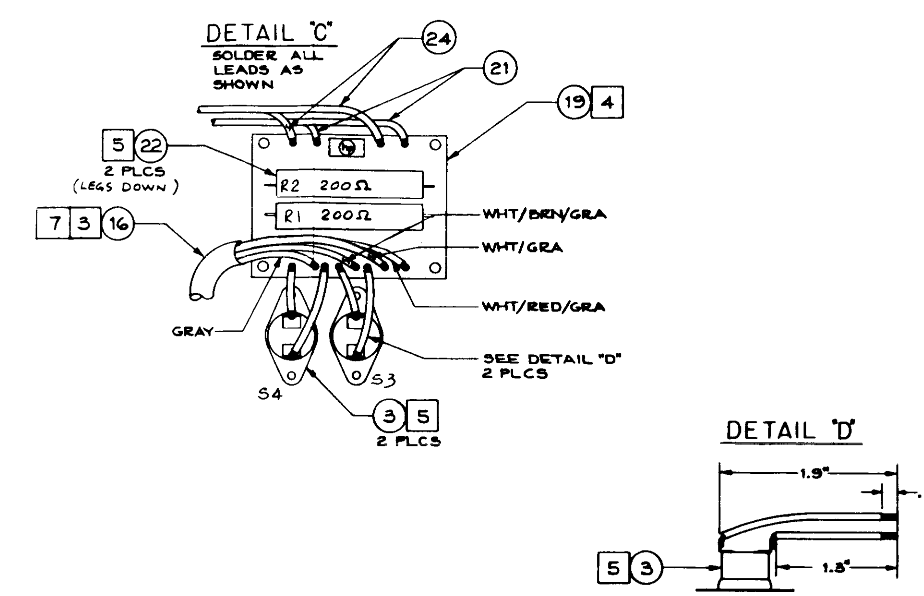
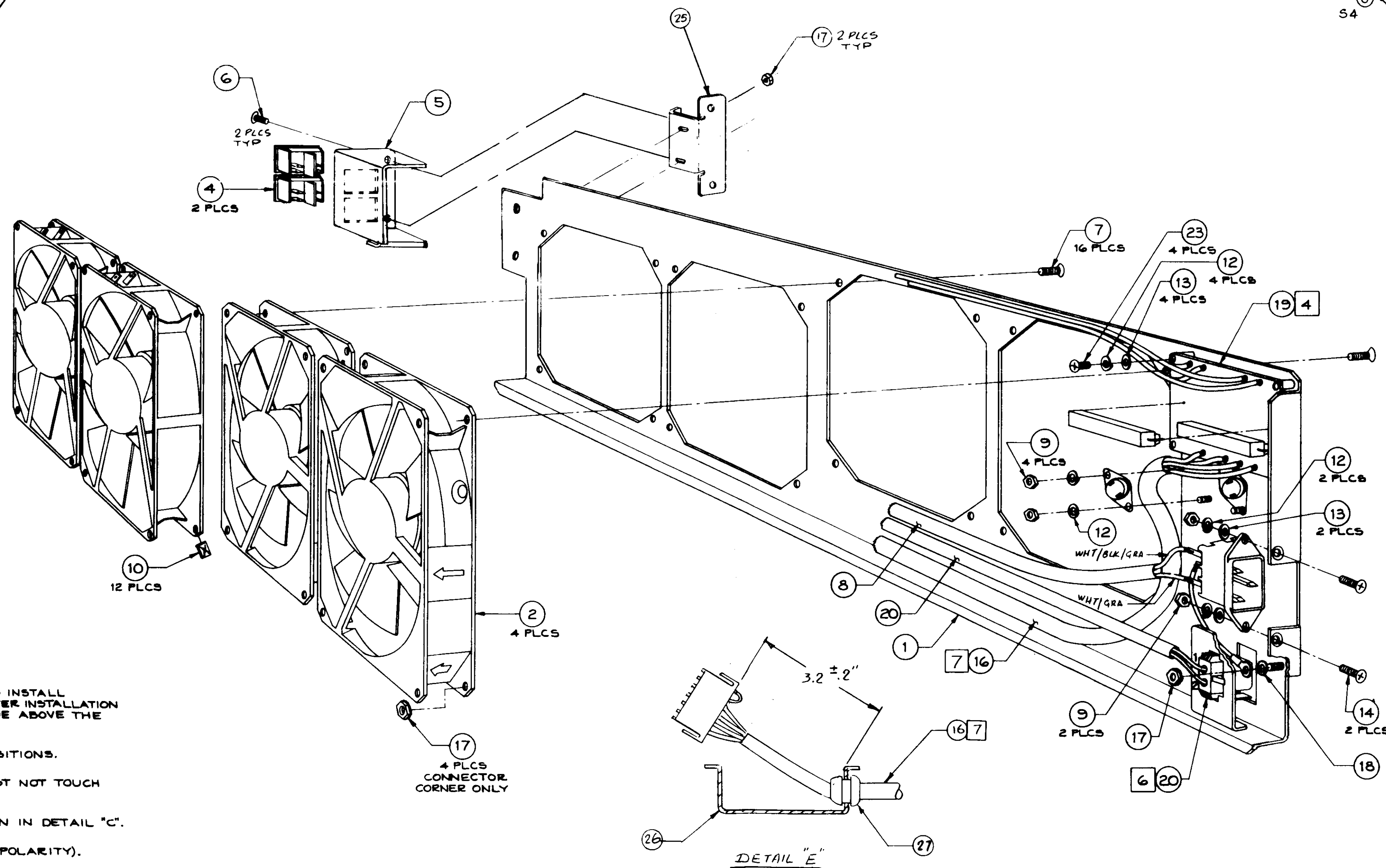


Figure 10-11. Rack Mounted 16-Slot Box Assembly (Sheet 3 of 4)

Update 1





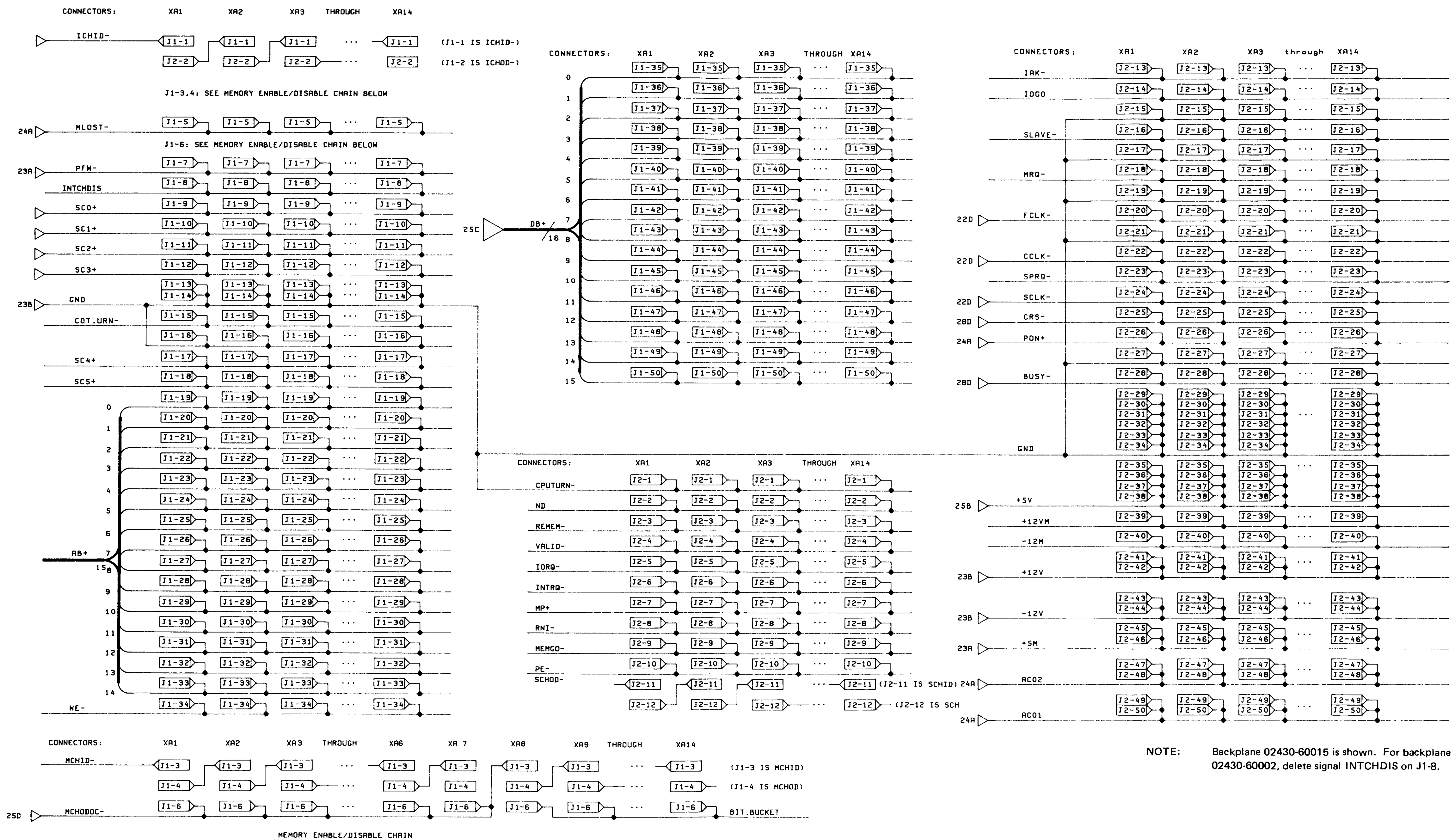


NOTES:

1. TUCK CABLE UNDER FAN FLANGE AND INSTALL CABLE TIE. ROTATE CABLE TIE AFTER INSTALLATION SO THAT HEAD DOES NOT PROTRUDE ABOVE THE PLANE OF THE FANS.
2. TIE ONLY ITEM (20) AT THESE 2 POSITIONS.
3. WIRE FROM ITEMS (16) (21) & (24) MUST NOT TOUCH ITEM (22).
4. INSTALL WITH HP LOGO AS SHOWN IN DETAIL "C".
5. ORIENTATION UNIMPORTANT (NO POLARITY).
6. INSTALL CONNECTOR WITH #1 UP.
7. INSTALL ITEMS (26) (27) BEFORE SOLDERING ITEM (16) TO ITEM (19). SEE DETAIL "E"

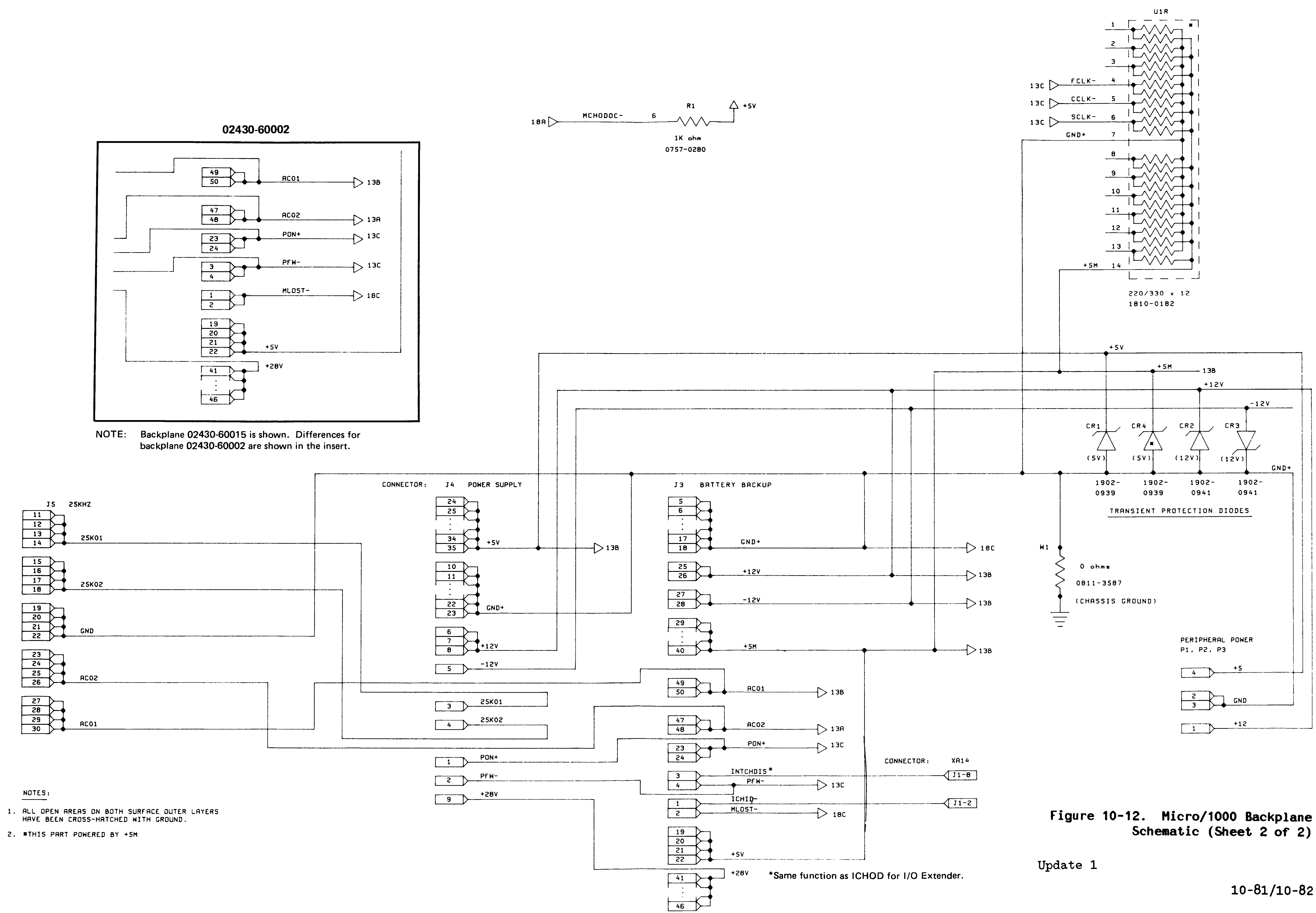
ITEM	QTY	MATERIAL-DESCRIPTION	MAT'L-PART NO.
27	1	STRAIN RELIEF GROMMET	0400-0155
26	1	COVER	02430-00028
25	1	SWITCH BRACKET	02430-00027
24	1	FAN CABLE-SHORT	8120-4271
23	4	SCREW-4-40 X .438	2200-0145
22	2	RESISTORS 200 Ω	0811-3643
21	1	FAN CABLE-LONG	8120-4272
20	1	CA. ASSY. BATT. BKUP. - SW.	02430-60011
19	1	PCB-FAN RESISTOR	02430-80010
18	2	LOCK WASHER, EXT. #6	2190-0008
17	8	NUT 6-32 W/LOCK	2420-0001
16	1	CABLE-PCA TO P.S.	02430-60008
15	1	CABLE-A.C. SW. TO P.S.	02430-60007
14	2	SCREW-4-40 X .375 F.H.	2200-0144
13	6	WASHER-FLAT #4	3050-0229
12	10	WASHER-LOCK #4	2190-0108
11	9	CABLE TIE	1400-0249
10	12	CLIP	0590-1516
9	6	NUT #4	2260-0002
8	1	A.C. POWER CABLE	02430-60006
7	16	SCREW #6 F.H. .375	2360-0196
6	2	SCREW #6 F.H. .312	3260-0194
5	1	SWITCH PLATE	02430-00009
4	2	SWITCH-RKR. DPST	3101-0402
3	2	THERMAL SWITCH	3103-0113
2	4	FAN-4.125"	3160-0420
1	1	FAN PANEL	02430-00008

Figure 10-11. Rack Mounted 16-Slot Box Assembly (Sheet 4 of 4)



NOTE: Backplane 02430-60015 is shown. For backplane 02430-60002, delete signal INTCHDIS on J1-8.

Figure 10-12. Micro/1000 Backplane Schematic (Sheet 1 of 2)



NOTE: Backplane 02430-60015 is shown. Differences for backplane 02430-60002 are shown in the insert.

NOTES:

1. ALL OPEN AREAS ON BOTH SURFACE OUTER LAYERS HAVE BEEN CROSS-HATCHED WITH GROUND.
2. *THIS PART POWERED BY +5M

*Same function as ICHOD for I/O Extender.

Figure 10-12. Micro/1000 Backplane Schematic (Sheet 2 of 2)

Update 1

11.1 INTRODUCTION

The processor frontplane has several functions. It connects the processor buses between the upper and lower processor cards, it connects the processor to the external registers in the memory controller, it links an optional floating-point processor to the computer processor using a different version of the frontplane, and it connects the computer processor to the control store. The frontplane also has a diagnostic connector, switch registers to input the B-bus, light registers to read the Y-bus, and a reset switch for self-testing.

The light and switch registers provides the user with status information and direct interface with the virtual control panel and the micromachine. For information on the meaning of the lights and the switch settings refer to the HP 1000 A700 Computer Installation and Service Manual, part no. 02137-90002.

The memory array frontplane connects the memory controller to the memory arrays. Since this frontplane is simply an interconnector, it is not covered in this document. (Installation of memory cards and memory frontplanes are covered in the HP 1000 A700 Computer Installation and Service Manual, part no. 02137-90002.)

11.2 FRONTPLANE PHYSICAL DESCRIPTION

Physically, the frontplane functions as a interconnector for the male connectors that are pushed into the frontplane female connectors of the upper and lower processors, and the connector for the board-edge terminals of the memory controller, and connector for the control-store flexible cable. It also serves as a test and diagnostic panel. This is the basic frontplane, part no. 12160-60001. When a HP 12156A Floating-Point Processor (FPP) card is installed, a different frontplane is used, part no. 12156-60002. Both frontplanes are referred to as the "frontplane" in this manual unless an exception is called out.

The frontplane includes two 160-pin male connectors J2 amd J3 for the processor cards (or an additional 160-pin male connector J6 for an FPP), a 50-pin connector J1 that plugs onto the J2 PC board frontplane terminals of the memory controller, a 50-pin connector J4 for the control store bus, and a 50-pin connector J5 for diagnostic connections. It has a cut-out area adjacent to the memory controller connector to allow room for a memory array connector.

The extension area of the frontplane (above the memory-array connector cutout) contains contains components for self-testing and boot up. The components are S1 and S2 switch registers, LED light registers, and ICs. The ICs are for buffering the B-bus inputs from the switches and Y-bus outputs to the LEDs.

The reset switch S3 is located above J2 and J3 (and J6 if it is a 12156-60002 frontplane).

The location of the frontplane parts are shown in Figure 11-1. Only the 12156-60002 frontplane is shown; however, the 12160-60001 basic frontplane is identical except that the J6 connector is omitted.

11.3 FRONTPLANE CONNECTOR PINOUTS

The bus lines and signals at the frontplane connectors are identified in Tables 11-1 through 11-6.

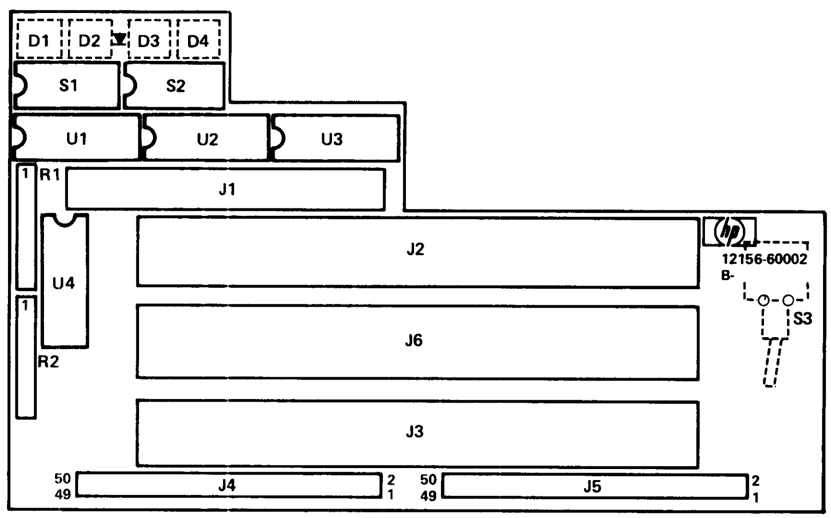


Figure 11-1. Frontplane Configuration (part no. 12156-60002)
(12160-60001 is identical except omit J6)

11.4 FUNCTIONAL DESCRIPTION

The functional description refers to the schematic located at the rear of this section. The 12160-60001 schematic is shown; however, the 12156-60002 schematic is identical except that J6 is added.

The switches (S1 and S2) have the closed side tied to ground and the open side tied high through 4.7K resistors (in resistor packs R1 and R2). The open sides of the switches are input to U1 and U4 which are octal buffers with tristate outputs. The outputs of U1 and U4 connect to the B-bus and to connector J3. The outputs of U1 and U4 are enabled by ELSRB- from connector J3 to pins U1-1 and U1-19, and U4-1 and U4-19.

The register lights are LEDs with the anode side tied to +5V. The cathode side of the LEDs receive signals from the output of U2 and U3 (octal D registers). The inputs of U2 and U3 are tied to the Y-bus from connector J3. The outputs of U2 and U3 are clocked with the signal LDLSR- from connector J3 into pins U2-11 and U3-11. The U2 and U3 registers are cleared on power up with BPON+ from connector J3 into pins U2-1 and U3-1.

The system reset switch is also on the frontplane as S3. It is a normally-closed/momentary-open switch. The common terminal of S3 is tied to ground, the normally closed terminal is tied to RESET+ from connector J3, and the momentary open terminal is tied to RESET- from connector J3.

Table 11-1. Connector J1 Terminal List

CONNECTOR J1: MEMORY CONTROLLER							
Pins 1 through 26				Pins 27 through 50			
1	GND	GND	2	27	EXBB7	EXBB8	28
3	YB0	YB1	4	29	EXBB9	EXBB10	30
5	YB2	YB3	6	31	EXBB11	EXBB12	32
7	YB4	YB5	8	33	EXBB13	EXBB14	34
9	YB6	YB7	10	35	EXBB15	N0	36
11	YB8	YB9	12	37	N1	N2	38
13	YB10	YB11	14	39	N3	LYMAP-	40
15	YB12	YB13	16	41	IIAK	ESRINB-	42
17	YB14	YB15	18	43	LYSRIN-		44
19		EXBB0	20	45	BLC-	EMAPB-	46
21	EXBB1	EXBB2	22	47		MPV-	48
23	EXBB3	EXBB4	24	49	GND	GND	50
25	EXBB5	EXBB6	26				

Table 11-2. Connector J2 Terminal List

CONNECTOR J2: UPPER PROCESSOR				
	A	B	C	D
40	YB3	YB2	YB1	YB0
39	YB7	YB6	YB5	YB4
38	YB11	YB10	YB9	YB8
37	YB15	YB14	YB13	YB12
36	GND	GND	GND	GND
35	BB0	BB1	BB2	BB3
34	BB4	BB5	BB6	BB7
33	BB8	BB9	BB10	BB11
32	BB12	BB13	BB14	BB15
31	GND	EXSPEC-	E-	GND
30	RDB2-	RDB0-	IP-	FCHB-
29		MIR20-	MIR19-	MIR18-
28		EPRINB-	EMAB-	ENB-
27	EFAB-	EMEMRB-	EMAPB-	EGRINB-
26	EISTB-	ETABB-	EPB-	ESRINB-
25	DC-	GND	CNDXSPARE	GND
24	GND	LC+	IFCH-	RDP0-
23	LDBR-		IN-	BFB-
22		RDIO-	DN-	FCHP-
21	GND	JTAB-	RDP2-	WRIO-
20		GND	CMID-	INTP+

(continued on next page)

Table 11-2. Connector J2 Terminal List (Continued)

CONNECTOR J2: UPPER PROCESSOR				
19	BPON+	LYN-	PC-	
18	TCNT-	MTO-	GND	FREEZE-
17		ABWR-	LRMABO	MABO
16	LRAB-		LYGRIN-	INT+
15	LYP-		LYWRP-	LYCWRB-
14		LYMAP-	LYWRB-	LYIST-
13	LYPRIN-	LYMEMR-		
12	GND	GND	GND	GND
11				
10				
9	FFRZ-			
8	EXBB3	EXBB2	EXBB1	EXBB0
7	EXBB7	EXBB6	EXBB5	EXBB4
6	EXBB11	EXBB10	EXBB9	EXBB8
5	EXBB15	EXBB14	EXBB13	EXBB12
4	N3	N2	N1	N0
3				
2		BLC-	MPV-	IIAK
1				

Table 11-3. Connector J3 Terminal List

CONNECTOR J3 LOWER PROCESSOR				
	A	B	C	D
40	YB3	YB2	YB1	YB0
39	YB7	YB6	YB5	YB4
38	YB11	YB10	YB9	YB8
37	YB15	YB14	YB13	YB12
36	GND	GND	GND	GND
35	BB0	BB1	BB2	BB3
34	BB4	BB5	BB6	BB7
33	BB8	BB9	BB10	BB11
32	BB12	BB13	BB14	BB15
31	GND	EXSPEC-	E-	GND
30	RDB2-	RDB0-	IP-	FCHB-
29	CSADIS-	MIR20-	MIR19-	MIR18-
28	ELSRB-	EPRINB-	EMAB-	ENB-
27	EFAB-	EMEMRB-	EMAPB-	EGRINB-
26	EISTB-	ETABB-	EPB-	ESRINB-
25	DC-	GND	CNDXSPARE	GND
24	GND	LC+	IFCH-	RDP0-
23	LDBR-	CK2-	IN-	BFB-
22	RESET-	RDIO-	DN-	FCHP-
21	GND	JTAB-	RDP2-	WRIO-
20	RESET+	GND	CMID-	INTP+

(continued on next page)

Table 11-3. Connector J3 Terminal List (Continued)

	CONNECTOR J3: LOWER PROCESSOR			
19	BPON+	LYN-	PC-	TESTSC-
18	TCNT-	MTO-	GND	FREEZE-
17	CKDIS-	ABWR-	LRMABO	MABO
16	LRAB-	ECLK	LYGRIN-	INT+
15	LYP-	LYSRIN-	LYWRP-	LYCWRB-
14	LDLSR-	LYMAP-	LYWRB-	LYIST-
13	LYPRIN-	LYMEMR-	CSD0	CSD1
12	CSD5	CSD4	CSD3	CSD2
11	CSD6	CSD7	CSD8	CSD9
10	CSD13	CSD12	CSD11	CSD10
9	CSD14	CSD15	CSD16	CSD17
8	CSD21	CSD20	CSD19	CSD18
7	CSD22	CSD23	CSD24	CSD25
6	CSD29	CSD28	CSD27	CSD26
5	CSD30	CSD31	CSA0	CSA1
4	CSA5	CSA4	CSA3	CSA2
3	CSA6	CSA7	CSA8	CSA9
2	CSA13	CSA12	CSA11	CSA10
1	CSIDFP-	CSIDWC-	+5	+5

Table 11-4. Connector J4 Terminal List

CONNECTOR J4: CONTROL STORE							
Pins 1 through 26				Pins 27 through 50			
1	CSD0	CSD1	2	27	CSD26	CSD27	28
3	CSD2	CSD3	4	29	CSD28	CSD29	30
5	CSD4	CSD5	6	31	CSD30	CSD31	32
7	CSD6	CSD7	8	33	CSA0	CSA1	34
9	CSD8	CSD9	10	35	CSA2	CSA3	36
11	CSD10	CSD11	12	37	CSA4	CSA5	38
13	CSD12	CSD13	14	39	CSA6	CSA7	40
15	CSD14	CSD15	16	41	CSA8	CSA9	42
17	CSD16	CSD17	18	43	CSA10	CSA11	44
19	CSD18	CSD19	20	45	CSA12	CSA13	46
21	CSD20	CSD21	22	47		CSIDWC-	48
23	CSD22	CSD23	24	49	GND	GND	50
25	CSD24	CSD25	26				

Table 11-5. Connector J5 Terminal List

CONNECTOR J5: DIAGNOSTIC CONNECTOR							
	Pins 1 through 26				Pins 27 through 50		
1	YB0	YB1	2	27	FREEZE-	TESTSC-	28
3	YB2	YB3	4	29	ECLK	CKDIS-	30
5	YB4	YB5	6	31	GND	GND	32
7	YB6	YB7	8	33	INT+	LYGRIN-	34
9	YB8	YB9	10	35	LYSRIN-	LYP-	36
11	YB10	YB11	12	37	LYPRIN-	LYIST-	38
13	YB12	YB13	14	39	FFRZ-	LYMEMR-	40
15	YB14	YB15	16	41	N1	N0	42
17	GND	GND	18	43	N3	N2	44
19	ESRINB-	CSADIS-	20	45	GND	GND	46
21	BPON+	JTAB-	22	47	CSIDWC-		48
23	PC-	INTP+	24	49	GND	GND	50
25	GND	GND	26				

Table 11-6. Connector J6 Terminal List

CONNECTOR J6: FLOATING POINT PROCESSOR				
	A	B	C	D
40	YB3	YB2	YB1	YB0
39	YB7	YB6	YB5	YB4
38	YB11	YB10	YB9	YB8
37	YB15	YB14	YB13	YB12
36	GND	GND	GND	GND
35				
34				
33				
32				
31	GND			GND
30				
29				
28				
27				
26				ESRINB-
25				
24		LC+		
23			CK2-	
22				LYSRIN-
21	BPON+	JTAB-		
20	GND	GND	GND	GND

(Continued on next page)

Table 11-6. Connector J6 Terminal List (Continued)

	CONNECTOR J6: FLOATING POINT PROCESSOR			
19	EXBB3	EXBB2	EXBB1	EXBB0
18	EXBB7	EXBB6	EXBB5	EXBB4
17	EXBB11	EXBB10	EXBB9	EXBB8
16	EXBB15	EXBB14	EXBB13	EXBB12
15	N3	N2	N1	N0
14	GND	GND	GND	GND
13			CSD0	CSD1
12	CSD5	CSD4	CSD3	CSD2
11	CSD6	CSD7	CSD8	CSD9
10	CSD13	CSD12	CSD11	CSD10
9	CSD14	CSD15	CSD16	CSD17
8	CSD21	CSD20	CSD19	CSD18
7	CSD22	CSD23	CSD24	CSD25
6	CSD29	CSD28	CSD27	CSD26
5	CSD30	CSD31	CSA0	CSA1
4	CSA5	CSA4	CSA3	CSA2
3	CSA6	CSA7	CSA8	CSA9
2	CSA13	CSA12	CSA11	CSA10
1	CSIDFP-	CSIDWC-		

11.5 PARTS LOCATIONS

Parts locations for the frontplane are shown in Figure 11-1.

11.6 PARTS LIST

The parts list for the frontplane is provided in Table 11-7. Refer to Table 3-8 for the names and addresses of manufacturers of the parts in the Manufacturer's Code List.

Table 11-7. Frontplane Replaceable Parts

Note: 12160-60001 parts list is identical to the 12156-60002 provided below except that J6 is omitted.

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
A1	12156-60002	6	1	PCA-FP FRONT PLAN	28480	12156-60002
D1	1990-0652	8	4	LED-VISIBLE	28480	1990-0652
D2	1990-0652	8		LED-VISIBLE	28480	1990-0652
D3	1990-0652	8		LED-VISIBLE	28480	1990-0652
D4	1990-0652	8		LED-VISIBLE	28480	1990-0652
J1	1251-4573	4	1	CONNECTOR- PC 2 X 25 .100	28480	1251-4573
J2	1251-7539	8	3	CONNECTOR- 160 PIN (MALE)	28480	1251-7539
J3	1251-7539	8		CONNECTOR- 160 PIN (MALE)	28480	1251-7539
J4	1251-7389	6	1	CONNECTOR	28480	1251-7389
J5	1251-4737	2	1	CONNECTOR- 50 PIN (MALE)	28480	1251-4737
J6	1251-7539	8		CONNECTOR- 160 PIN (MALE)	28480	1251-7539
R1	1810-0279	5	2	NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
R2	1810-0279	5		NETWORK-RES 10-SIP4.7K OHM X 9	01121	210A472
S1	3101-2492	7	3	SWITCH-ROCKER 8 POSITION	28480	3101-2492
S2	3101-2492	7		SWITCH-ROCKER 8 POSITION	28480	3101-2492
S3	3101-2429	0	1	SWITCH-TOGGLE SPDT	28480	3101-2429
U1	1820-2024	3	4	IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
U2	1820-1730	6	2	IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U3	1820-1730	6		IC FF TTL LS D-TYPE POS-EDGE-TRIG COM	01295	SN74LS273N
U4	1820-2024	3		IC DRVR TTL LS LINE DRVR OCTL	01295	SN74LS244N
	0520-0130	1	6	SCREW MACH 2-56 .375-IN-LG PAN-HD POZI	00000	ORDER BY DESCRIPTION
	1251-7835	7	6	LOCATING KEY	28480	1251-7835
	2190-0045	8	6	WASHER-LK HLCL NO. 2 .088 IN-ID	28480	2190-0045
	7121-2061	2	1	LABEL-DATE CODE	28480	7121-2061
	12156-80002	8	1	PCB-FP FRONT PLAN	28480	12156-80002

ENGINEERING RESPONSIBILITY / SEPIA

D-12160-60001-51

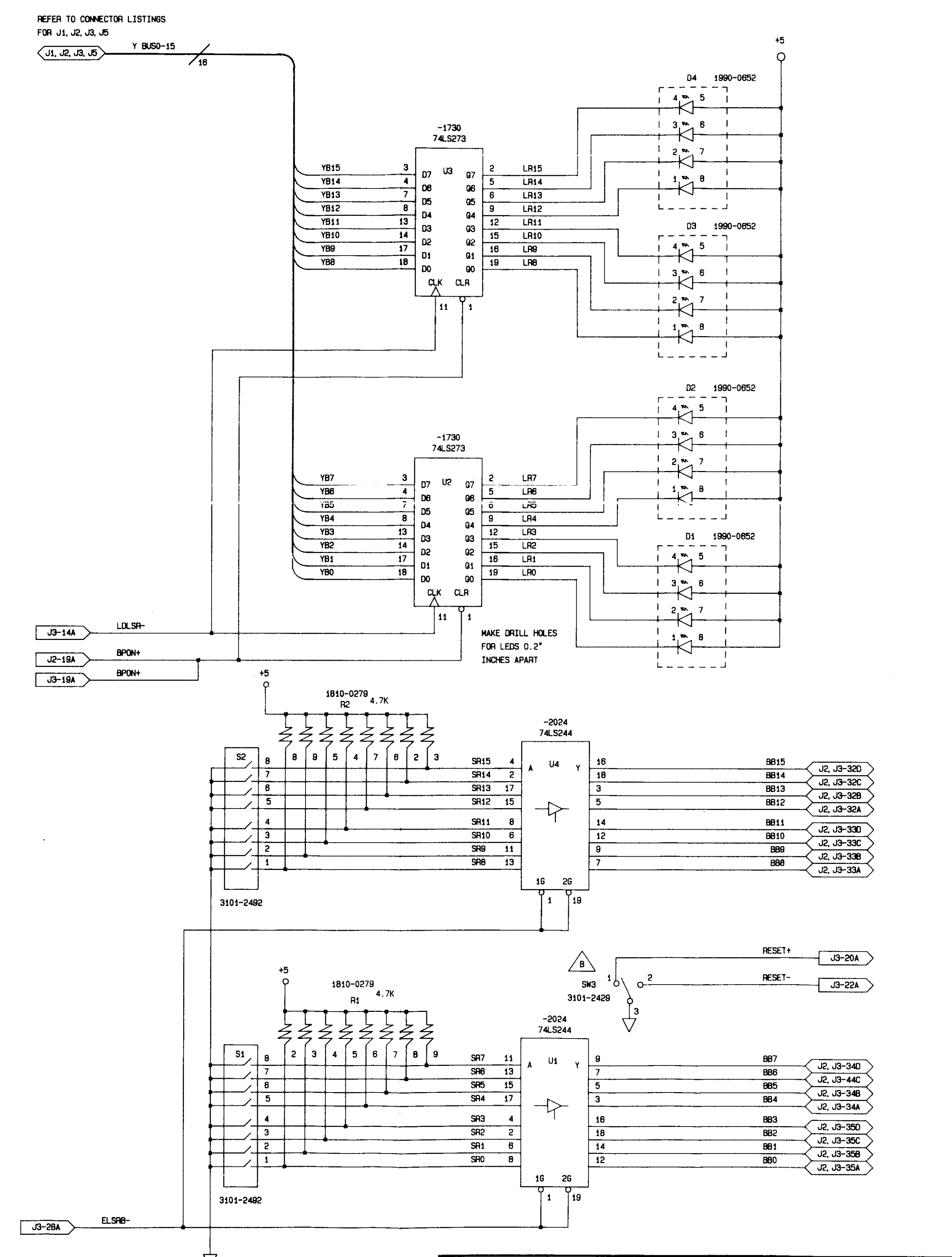
SYM	REVISIONS	APPROVED	DATE
A	AS ISSUED		
B	SW3 WAS 3101-1675 PER PRCR "B"		

MEMORY CONTROLLER

	J1	J1	
1	GND	GND	2
3	YB0	YB1	4
5	YB2	YB3	6
7	YB4	YB5	8
9	YB6	YB7	10
11	YB8	YB9	12
13	YB10	YB11	14
15	YB12	YB13	16
17	YB14	YB15	18
19		EXBB0	20
21	EXBB1	EXBB2	22
23	EXBB3	EXBB4	24
25	EXBB5	EXBB6	26
27	EXBB7	EXBB8	28
29	EXBB9	EXBB10	30
31	EXBB11	EXBB12	32
33	EXBB13	EXBB14	34
35	EXBB15	N0	36
37	N1	N2	38
39	N3	LYMAP-	40
41	IIAK	ESRINB-	42
43	LYSRIN-		44
45	BLC-	EMAPB-	46
47		MPV-	48
49	GND	GND	50

J2 UPPER PROCESSOR

	A	B	C	D
40	YB3	YB2	YB1	YB0
39	YB7	YB6	YB5	YB4
38	YB11	YB10	YB9	YB8
37	YB15	YB14	YB13	YB12
36	GND	GND	GND	GND
35	BB0	BB1	BB2	BB3
34	BB4	BB5	BB6	BB7
33	BB8	BB9	BB10	BB11
32	BB12	BBI3	BB14	BB15
31	GND	EXSPEC-	E-	GND
30	RDB2-	RDB0-	IP-	FCHB-
29		MIR20-	MIR19-	MIR18-
28		EPRINB-	EMAB-	ENB-
27	EFAB-	EMEMRB-	EMAPB-	EGRINB-
26	EISTB-	ETABB-	EPB-	ESRINB-
25	DC-	GND	CNDX SPARE	GND
24	GND	LC+	IFCH-	RDP0-
23	LDBR-		IN-	BFB-
22		RDI0-	DN-	FCHP-
21	GND	JTAB-	RDP2-	WRI0-
20		GND	CMID-	INTP+
19	BPON+	LYN-	PC-	
18	TCNT-	MT0-	GND	FREEZE-
17		ABWR-	LRMAB0	MAB0
16	LRAB-		LYGRIN-	INT+
15	LYP-		LYWRP-	LYCWRB-
14		LYMAP-	LYWRB-	LYIST-
13	LYPRIN-	LYMEMR-		
12	GND	GND	GND	GND
11				
10				
9	FFRZ-			
8	EXBB3	EXBB2	EXBB1	EXBB0
7	EXBB7	EXBB6	EXBB5	EXBB4
6	EXBB11	EXBB10	EXBB9	EXBB8
5	EXBB15	EXBB14	EXBB13	EXBB12
4	N3	N2	N1	N0
3				
2		BLC-	MPV-	IIAK
1				



NOTE:
UNLESS OTHERWISE SPECIFIED:
ALL RESISTANCE IN OHMS.
ALL IC'S ARE 1820 XXXX.
RESISTOR SIP +5 PIN 1
4.7K RESISTORS ARE 1810-0279

1

DRAWN BY	DATE 3/31/82	A700 FRONT PLANE	HEWLETT PACKARD
ENGINEER	1/8/82	TITLE	
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER 12160-60001
SUPERSEDES DWG.		SHEET 1 OF 2	D-12160-60001-51

SYM	REVISIONS	APPROVED	DATE
A	S ISSUED		

J3 LOWER PROCESSOR

	A	B	C	D
40	YB3	YB2	YB1	YB0
39	YB7	YB6	YB5	YB4
38	YB11	YB10	YB9	YB8
37	YB15	YB14	YB13	YB12
36	GND	GND	GND	GND
35	BB0	BB1	BB2	BB3
34	BB4	BB5	BB6	BB7
33	BB8	BB9	BB10	BB11
32	BB12	BB13	BB14	BB15
31	GND	EXSPEC-	E-	GND
30	ADB2-	ADB0-	IP-	FCHB-
29	CSADIS-	MIR20-	MIR19-	MIR18-
28	ELSAB-	EPRINB-	EMAB-	ENB-
27	EFAB-	EMEMAB-	EMAPB-	EGRINB-
26	EISTB-	ETABB-	EPB-	ESRINB-
25	DC-	GND	CNDX SPARE	GND
24	GND	LC+	IFCH-	ADPO-
23	LDBA-	CK2-	IN-	BFB-
22	RESET-	ADIO-	DN-	FCHP-
21	GND	JTAB-	ADP2-	WRIO-
20	RESET+	GND	CMID-	INTP+
19	BPON+	LYN-	PC-	TESTSC-
18	TCNT-	MTO-	GND	FREEZE-
17	CKDIS-	ABWR-	LAMAB0	MAB0
16	LAAB-	ECLK	LYGRIN-	INT+
15	LYP-	LYSRIN-	LYWAP-	LYCWAB-
14	LDLSA-	LYMAP-	LYWAB-	LYIST-
13	LYPRIN-	LYMEMR-	CSD0	CSD1
12	CSD5	CSD4	CSD3	CSD2
11	CSD6	CSD7	CSD8	CSD9
10	CSD13	CSD12	CSD11	CSD10
9	CSD14	CSD15	CSD16	CSD17
8	CSD21	CSD20	CSD19	CSD18
7	CSD22	CSD23	CSD24	CSD25
6	CSD29	CSD28	CSD27	CSD26
5	CSD30	CSD31	CSA0	CSA1
4	CSA5	CSA4	CSA3	CSA2
3	CSA6	CSA7	CSA8	CSA9
2	CSA13	CSA12	CSA11	CSA10
1	CSIDFP-	CSIDWC-	+5	+5

CONTROL STORE

	J4	J4	
1	CSD0	CSD1	2
3	CSD2	CSD3	4
5	CSD4	CSD5	6
7	CSD6	CSD7	8
9	CSD8	CSD9	10
11	CSD10	CSD11	12
13	CSD12	CSD13	14
15	CSD14	CSD15	16
17	CSD16	CSD17	18
19	CSD18	CSD19	20
21	CSD20	CSD21	22
23	CSD22	CSD23	24
25	CSD24	CSD25	26
27	CSD26	CSD27	28
29	CSD28	CSD29	30
31	CSD30	CSD31	32
33	CSA0	CSA1	34
35	CSA2	CSA3	36
37	CSA4	CSA5	38
39	CSA6	CSA7	40
41	CSA8	CSA9	42
43	CSA10	CSA11	44
45	CSA12	CSA13	46
47		CSIDWC-	48
49	GND	GND	50

DIAGNOSTIC

	J5	J5	
1	YB0	YB1	2
3	YB2	YB3	4
5	YB4	YB5	6
7	YB6	YB7	8
9	YB8	YB9	10
11	YB10	YB11	12
13	YB12	YB13	14
15	YB14	YB15	16
17	GND	GND	18
19	ESRINB-	CSADIS-	20
21	BPON+	JTAB-	22
23	PC-	INTP+	24
25	GND	GND	26
27	FREEZE-	TESTSC-	28
29	ECLK	CKDIS-	30
31	GND	GND	32
33	INT+	LYGRIN-	34
35	LYSRIN-	LYP-	36
37	LYPRIN-	LYIST-	38
39	FFRZ-	LYMEMR-	40
41	N1	N0	42
43	N3	N2	44
45	GND	GND	46
47	CSIDWC-		48
49	GND	GND	50

2

DRAWN BY	DATE 4/1/82	TITLE: A700 FRONT PLANE	HEWLETT PACKARD
ENGINEER	1/8/82		
RELEASE TO PROD		NEXT ASSEMBLY	PART NUMBER 12160-60001
SUPERSEDES DWG.		SHEET 2 OF 2	D-12160-60001-52

VCP, LOADERS, AND SELF-TEST PROGRAMS — APPENDIX A

This appendix contains a listing of the Test 2 portion of the self-test, loaders, and Virtual Control Panel programs contained in ROM located on the memory controller card.

The 4k ROM code is identified by HP part number 5180-0164 and 5180-0165 and is contained in ICs U15 and U35, respectively, on the memory controller card. A second set of sockets at U55 and U65 is provided for use by OEM's.

A user who intends to change the ROM code for any reason should keep in mind the considerations described below.

The A700 Computers provide two additional ROM sockets for user loaders implemented in 4k parts. A user who wants to create his own loaders should burn his own loader code into the second set of ROMs (Intel PROM 2732A). The start-up switches on the processor card may be set to execute this code on power-up; the code may also be invoked by VCP commands when the VCP program is being run.

The VCP address space is separate from the main memory of the computer, consisting of 1k words of RAM in the base page and 4k or 8k words of ROM space. The VCP program provided with the computer occupies 4k of ROM space (octal addresses 20000 to 37777). Additional space from addresses 40000 to 57777 may be assigned to user loaders, as described above, with user code starting at location 40002. Thus, locations 40000 and 40001 may be used for revision code and checksum. The RAM area of the VCP address space can be accessed only by the VCP or microcode. However, the VCP can access main memory through the use of cross-map instructions. Because the VCP memory area is not mapped, the VCP can execute even when the maps or main memory is not functional.

As the VCP runs from ROM, any instruction that might need to modify ROM cannot be used. Thus, JLB instructions are used for subroutine linkage, rather than JSB instructions.

When the VCP mode is enabled, trap cells for processor interrupts are in the VCP RAM address space, but DMA self-configuration quadruplets are not since all DMA transfers still access main memory. (I/O interrupt trap cells also remain in main memory.) In order to test DMA, the VCP reserves the last 64 locations of page 0 in main memory; these locations also are used by the VCP for passing the command string to BOOTEX or diagnostics.

The base page of VCP RAM is divided as follows:

00000 to 00077	Reserved for trap cells.
00100 to 00177	Reserved for microcode use.
00200 to 00777	Reserved for HP-supplied VCP.
01000 to 01377	Available for user ROM code (loaders or power-up).
01400 to 01777	Reserved for error logging in A700 computers (available for user ROM code in A600 computers.)

The VCP program is divided into four pages (page 0 through page 3). Page 0 contains the Pretest (Test-2 portion of the self-test). Page 1 contains the user interface. Page-2 contains the drivers for the ASIC card, the intelligent interface cards, and the DS loader. Page 3 contains the ROM loader, the CTU loader, and the disc loader.

User ROM code can call the existing loader routines through a jump table located at the beginning of page 3.

The following is a summary of points to remember about VCP addressing:

1. The boot ROM code space begins at address 20000 octal and continues to 57777 octal. Addresses above 57777 produce undefined results.

2. Boot RAM space is from 00002 to 17777 octal, but in the A600 and A700 computers, only 1k of boot RAM is installed (addresses 2 to 1777 octal).

3. Portions of boot RAM have been set aside for system functions and may not be used for other purposes.

The following pages contain a sample 4k-ROM listing of the VCP, loaders, and self-test programs. As ROM firmware is subject to change, later versions will differ in minor details from what is shown in this listing. (Note that there is a Cross Reference Symbol Table at the end of the listing.)

```
                MACRO,A,Q=S,C
*     A   -> ABSOLUTE ASSEMBLY
*     Q=S -> SHORT LISTING
*     C   -> PRINT CROSS REFERENCE TABLE
*
************************************************************************??
*
*  NAME: &VCP
*
*  SOURCE: 24998-18540
*
*  BURN TAPE: 24998-16540 AND 24998-16541
*
*  ROMS: 5180-0189 HIGH BYTE AND 5180-0190 LOW BYTE
*
*  PGMR: D.A.F.
*
*  LAST MODIFIED: 820706.0954
*
*******************************************************************
* (C) COPYRIGHT HEWLETT PACKARD COMPANY 1982. ALL RIGHTS          *
* RESERVED. NO PART OF THIS PROGRAM MAY BE PHOTOCOPIED,           *
* REPRODUCED, OR TRANSLATED TO ANOTHER PROGRAM LANGUAGE WITHOUT *
* THE PRIOR WRITTEN CONSENT OF HEWLETT PACKARD COMPANY            *
*******************************************************************
*
*
*
*
```

```
*
        020000  EPROM EQU 20000B
*
                      MACLIB ^DMS     ;PHOENIX OPCODE MACRO FILE
*
*
*
*  the first 64 locations of boot memory are reserved for trap cells
*
*
*
 00100                ORG 100B
*
*     VIRTUAL REGISTER AREA FOR PROCESSOR (64 LOCATIONS)
*
 00100 000000  WMAP  NOP              OLD WMAP VALUE ON ENTRY
*
*
*
        000001  CPUST EQU 1
*
*     CPU STATUS IS OBTAINED BY A LIA/B 1
*  SW 1   BIT 8 = BOOT SELECT 0
*     2       9 = BOOT SELECT 1
*     3      10 = BOOT SELECT 2
*     4      11 = BOOT SELECT 3
*     5      12 = SELECT ALTERNATE VCP DRIVER
*     6      13 = RESERVED
*     -      14 = MEMORY LOST  (LOW TRUE) ONLY valid for 5 ms
*     8      15 = INTERRUPT MASK BIT 1 FOR PROCESSOR BOARD
*
*          SWITCH 7 IS RESERVED ON THE PROCESSOR FOR INT/EXT CLOCK
*
*
*     CPU CONTROL OUTPUT BY AN OTA/B 1
*     BIT 0-7 = STATUS LIGHT 0-7
*
                      MIC .JLB,104600B,1
                      MIC .JLA,100600B,1
*
 00200                ORG 200B
```

```
*
*     BASE PAGE STORAGE LOCATIONS
*
          000000  A      EQU 0
          000001  B      EQU 1
          000002  GR     EQU 2
          000030  DATA   EQU 30B
          000032  STATS  EQU 32B
          000031  CMND   EQU 31B
          000030  DATA   EQU 30B
    00200 000000  SAVEI  NOP
    00201 000000  SAVEO  NOP
    00202 000000  SAVEE  NOP
    00203 000000  SAVEP  NOP
    00204 000000  SAVEA  NOP
    00205 000000  SAVEB  NOP
    00206 000000  SAVEG  NOP
    00207 000000  SAVEX  NOP
    00210 000000  SAVEY  NOP
    00211 000000  SAVEQ  NOP
    00212 000000  SAVEZ  NOP
    00213 000000  SAVEM  NOP
    00214 000000  SAVEW  NOP
*
    00215 000000  MLOST      NOP  MEMORY LOST FLAG LOW TRUE IN SIGN BIT
    00216 000000  D1SV       NOP  DATA 1 MAP SAVE FOR %CLEAR MEMORY
    00217 000000  PNTR       NOP
    00220 000000  PNTRS      NOP
    00221 000000  SVCHR      NOP
    00222 000000  SACOMN     NOP
    00223 000000  CTR        NOP
    00224 000000  MCNTR      NOP  COUNT FOR MAP DISPLAY
    00225 000000  PCNTR      NOP  PAGE COUNT FOR MAP DISPLAY
    00226 000000  PUTCT      NOP  CHAR COUNT FOR PUTS
    00227 000000  PETMP      NOP
    00230 000000  PERTN      NOP  RETURN ADDRESS FROM PE ROUTINE
    00231 000232  PEJMPI     JMP PE,I  PUT HERE DURING EXECUTION
    00232 000000  PE         NOP  PLACE FOR DEF TO PEINT ROUTINE
    00233 000000  TBG        NOP  DEF TO TBG ROUTINE
    00234 000000  ILI        NOP
    00235 000000  PFW        NOP  ETC
    00236 000000  MPT        NOP
    00237 000000  UITRTN     NOP  RETURN ADDRESS FROM UIT ROUTINE
    00240 000241  UIJMPI    JMP UIT,I  PUT HERE DURING EXECUTION
    00241 000000  UIT        NOP
    00242 000000  INTIO      NOP  DEF TO I/O INT ROUTINE
    00243 000000  PEFLAG     NOP  1 IF PARITY ERROR DURING LAST COMMAND
    00244 000000  DISPLAY    NOP  ERROR DISPLAY
```

```
00245 000000  TBGCNT      NOP  COUNT FOR 10 MS FROM TBG
00246 000000  MSIZE       NOP  NUMBER OF 32K BLOCKS OF PHYSICAL MEMORY
00247 000000  ECCCNT      NOP  NUMBER OF 32K ECC BLOCKS
00250 000000  CORCNT      NOP  NUMBER OF SINGLE BIT CORRECTIONS
00251 000000  CNTR        NOP
00252 000000  TRYCT       NOP  RETRY COUNTER FOR AUTO BOOT
00253 000000  DCTO        NOP  TIME OUT FOR DISC LOADER
00254 000000  MPTR        NOP         POINTER TO MAP REG BEING OUTPUT
00255 000000  PPNTR       NOP
00256 000000  BASE        NOP             0 => OCTAL, -1 => HEX
00257 000000  HPIT        NOP
00260 000000  TEMP        NOP
00261 000000  CHAR        NOP
00262 000000  RFTMP       NOP  TEMPORARY FOR RF ROUTINE
00263 000000  IORGN       NOP  I/O REGISTER NUMBER FOR RXX COMMAND
00264 000000  SCETC       NOP  2127 OR WHATEVER TYPED IN AFTER LOAD OR
                                  BOOT
00265 000000  LERR        NOP  LOADER ERROR
00266 000000  PARTIAL     NOP  PARTIAL COUNT FOR DISC LOADER
*
00267 000000  UNIT             NOP
00270 000000  SUBCH            NOP
00271 000000  DISC.ID          NOP
00272 000000  UNIT.HEAD        NOP          FLAG
00273 000000  CYLNDR.OFFSET    NOP
00274 000000  FILE             NOP          VECTOR WORD 1
00275 000000  HEAD.CYLINDER    NOP          VECTOR WORD 2
00276 000000  SECTR.TRACK      NOP          VECTOR WORD 3
00277 000000  VW1              NOP          ; WHEN TALKING TO
00300 000000  VW2              NOP          ;  LINUS THESE WILL
00301 000000  VW3              NOP          ;   DIFFER FROM ABOVE
*
00302 000000  PEADD       NOP    PARITY ADDRESS
00303 000000  PEMAP       NOP    BLOCK FOR PARITY ADDRESS
00304 000000  VCPTFLG     NOP    FLAG FOR %TEST COMMAND
00305 000000  TRAPFLAG    NOP    FLAG FOR TRAP CELLS CLOBBERED
00306         STRNG       BSS 40   ;BOOT COMMAND STRING (ALLOW 80
                                      CHARACTERS)
*
00356 000000  LSTR        NOP           LENGTH OF STRING
00357 000000  GSLR        NOP           LEFT/RIGHT BYTE FLAG
00360 000000  STORE.POINTER    NOP  POINTER TO STRNG
00361 000000  DPNTR       NOP
00362 000000  BFLAG       NOP
00363 000000  DFLAG       NOP  DIGIT FLAG  MSB = 1 => ONE DIGIT
00364 000000  RFLAG       NOP  ROM FLAG USED IN "TREG" ROUTINE
00365 000000  TFLAG       NOP  TRACE FLAG MSB = 1 => TRACE IN PROGRESS
00366 000000  MAP         NOP         CURRENT MAP
00367 000000  PAGE        NOP         CURRENT PAGE
```

```
00370        MPBUF     BSS 32       COPY OF CURRENT MAP
00430        MZSV      BSS 32       COPY OF MAP ZERO
00470 000000 DIG1      NOP
00471 000000 DIG2      NOP
00472 000000 DIG3      NOP
00473 000000 DIG4      NOP
00474 000000 DIG5      NOP
00475 000000 DIG6      NOP
00476 000000 DIGS      NOP
*
00477 000000 PO.CT     NOP
00500 000000 PO.T3     NOP
00501 000000 TEMP2     NOP
00502 000000 TEMP1     NOP
00503 000000 TEMPO     NOP
00504 000000 TEMP3     NOP
00505 000000 PO.A      NOP
00506 000000 PO.B      NOP
*
00507 000000 FIRST     NOP
00510 000000 NDCLR     NOP
00511 000000 POINTER   NOP
00512 000000 SIDE?     NOP
00513 000000 VCP.FLAG  NOP   IS THERE A VCP??
00514 000000 VCPSC     NOP   SELECT CODE OF VCP
00515 000000 ASFLG     NOP   NONZERO FOR TIC, ZERO FOR DS
*
00516 000000 EXLOAD    NOP EXTENDED LOAD COUNTER FOR DS LOADER
00517 000000 P3.CT     NOP RECORD COUNT FOR DS LOADER
00520 000000 .PU       NOP ASCII P AND UNIT NUMBER FOR CTU LOADER
00521 000000 DSCNT     NOP WORD COUNT FOR ABS BINARY IN DS LOADER
00522 000000 DSADD     NOP ADDRESS COUNT FOR DS LOADER
00523 000000 DSCHK     NOP CHECKSUM FOR DS LOADER
*
00524 000000 XEQT  NOP         THIS IS USED IN THE I/O
00525 000000       NOP          REGISTER ROUTINE
00526 000524     JMP XEQT,I   PLANTED HERE DURING EXECUTION
```

```
*
*     THESE ARE THE SUBROUTINE RETURN REGISTERS
*
00527 000000  RPUTS NOP
00530 000000  RENDV NOP
00531 000000  RENQAK NOP
00532 000000  RGETS NOP
00533 000000  ROUT1 NOP
00534 000000  ROUTN NOP
00535 000000  RLCH1 NOP
00536 000000  RLCHR NOP
00537 000000  ROUTD NOP
00540 000000  RECHO NOP
00541 000000  RPUTC NOP
00542 000000  RGETC NOP
00543 000000  RGETREG NOP
00544 000000  RGETN NOP
00545 000000  RSCNSC NOP
00546 000000  RRSTO NOP
00547 000000  RCOMN NOP
*
00550 000000  RCTU  NOP
00551 000000  RTI.W NOP
00552 000000  RTI.B NOP
00553 000000  RTO.B NOP
00554 000000  RTO.W NOP
00555 000000  RCTIO NOP
*
00556 000000  RRMLD  NOP
00557 000000  RDCLD  NOP
00560 000000  RPHI?  NOP
00561 000000  RPHI   NOP
00562 000000  RPHII  NOP
00563 000000  RHPIB  NOP
00564 000000  RPHIF  NOP
00565 000000  RHPIBX NOP
00566 000000  RDCIN  NOP
00567 000000  RDTPC  NOP
00570 000000  RDCRW  NOP
00571 000000  RDSLD  NOP
00572 000000  RS.SC  NOP
00573 000000  RDS.B  NOP
00574 000000  RDS.GT NOP
00575 000000  RCI.IZ NOP
00576 000000  RCI.ID NOP
00577 000000  RTG.BF NOP
00600 000000  RTG.TB NOP
```

```
00601 000000  RCL.IZ NOP
00602 000000  RDS.FT NOP
00603 000000  RDS.CM NOP
00604 000000  RCS.FT NOP
00605 000000  RCS.CM NOP
00606 000000  ROUT2C NOP
*
00607 000000  RGT01  NOP
00610 000000  RI.0   NOP
*
*
*     256 LOCATIONS RESERVED FOR USER ROM CODE
*
01000                ORG 1000B
01000                BSS 256
*
*     LAST 256 LOCATIONS RESERVED FOR ERROR LOGGING
01400                ORG 1400B
01400                BSS 256
      002000  LAST   EQU *
*
*
20000               ORG EPROM
```

VIRTUAL CONTROL PANEL PAGE 0

```
      020000  P0     EQU *           PAGE 0 REFERENCE
*    I.  PRETEST
*        THE PRETEST IS USED TO VERIFY EXECUTION OF THE BASIC
*        INSTRUCTIONS USED IN THE BOOT LOADERS.  THE ASUMPTION IS
*        MADE THAT THE JMP INSTRUCTION IS FUNCTIONAL AND WILL BE
*        USED TO STOP EXECUTION.  THE PRETEST IS NOT ENTENDED TO BE
*        A COMPLETE CHECK OF THE CPU BUT ONLY THAT THE INSTRUCTIONS
*        USED IN THE BOOT ARE FUNCTIONAL SO THAT A BOOT LOAD MAY BE
*        POSSIBLE.
*
20000 000006  RVCODE OCT 6           CONSTANT   (REV CODE GOES HERE)
20001 000000  CHKSUM NOP             CHECKSUM SPOT


*     THE FOLLOWING INSTRUCTIONS CHECK THE CPU ONLY
*     macrocode execution starts here after power up or reset
*
20002 002400  START CLA
20003 000304        STA VCPTFLG      NO TEST, POWER UP
20004 102501        LIA CPUST        get mlost bit
20005 000215        STA MLOST
20006 021711        LDA B3           TRY TO INDICATE IN INSTRUCION TEST
20007 003000        CMA
20010 102601        OTA CPUST
20011 002701        CLA,CCE,RSS      A=000000  B=XXXXXX  E=1  O=X  +SKP
20012 020012        JMP *            RSS FAILED
20013 006440        CLB,SEZ          A=000000  B=000000  E=1  O=X  -SKP
20014 002102        CLE,SZA          A=000000  B=000000  E=0  O=X  +SKP
20015 020015        JMP *            CCE-SEZ OR CLA-SZA FAILED
20016 003041        CMA,SEZ,RSS      A=177777  B=000000  E=0  O=X  -SKP
20017 006202        CME,SZB          A=177777  B=000000  E=1  O=X  +SKP
20020 020020        JMP *            CCE OR CLB-SZB FAILED
20021 007040        CMB,SEZ          A=177777  B=177777  E=1  O=X  -SKP
20022 006003        SZB,RSS                                        +SKP
20023 020023        JMP *            CME OR CMB FAILED
20024 000001        CPA B                                          -SKP
20025 002414        CLA,SLA,INA      A=000001  B=177777  E=1  O=X  +SKP
20026 020026        JMP *            CMA-CPA B-SLA,INA FAILED
20027 002002        SZA                                            -SKP
20030 002020        SSA                                            +SKP
20031 020031        JMP *            INA OR SSA FAILED
20032 006400        CLB              A=000001  B=000000  E=1  O=X
20033 003420        CCA,SSA          A=177777  B=000000            -SKP
20034 002003        SZA,RSS                                        +SKP
20035 020035        JMP *            CCA-SSA OR SZA,RSS FAILED
20036 002010        OCT 002010       ASG SLA                       -SKP
20037 002131        CLE,SSA,SLA,RSS A=177777  B=000000 E=0 O=X     +SKP
20040 020040        JMP *            SLA OR SSA,SLA,RSS FAILED
20041 102101        STO              A=177777  B=000000  E=0  O=1
```

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```
20042 102201    SOC                                                         -SKP
20043 102301    SOS                                                         +SKP
20044 020044    JMP *         STO-SOC-SOS FAILED
20045 103101    CLO           A=177777  B=000000  E=0  O=0
20046 102301    SOS                                                         -SKP
20047 102201    SOC                                                         +SKP
20050 020050    JMP *         CLO-SOS-SOC FAILED

20051 021761    LDA ALT1      A=125252  B=000000  E=0  O=0
20052 006003    SZB,RSS
20053 000001    CPA B                                                       +SKP
20054 020054    JMP *         CPA B OR CLB-SZB,RSS FAILED
20055 021761    CPA ALT1                                                    -SKP
20056 000001    STA B         A=125252  B=125252  E=0  O=0
20057 021761    LDA ALT1
20060 000000    CPB A                                                       +SKP
20061 003401    CCA,RSS       A=177777  B=125252  E=0  O=0                  +SKP
20062 020062    JMP *         CPA-STA-CPB FAILED
20063 021760    AND ALTO      A=052525  B=125252  E=0  O=0
20064 021760    CPA ALTO                                                    -SKP
20065 002001    RSS                                                         +SKP
20066 020066    JMP *         AND-CPA FAILED
20067 021761    AND ALT1      A=000000  B=125252  E=0  O=0
20070 002002    SZA                                                         +SKP
20071 020071    JMP *         AND FAILED
20072 021721    LDA B24       A=000024  B=125252  E=0  O=0
20073 021760    IOR ALTO      A=052525  B=125252  E=0  O=0
20074 021760    CPA ALTO                                                    -SKP
20075 003401    CCA,RSS       A=177777  B=125252  E=0  O=0                  +SKP
20076 020076    JMP *         XOR FILED
20077 021761    XOR ALT1      A=052525  B=125252  E=0  O=0
20100 021760    CPA ALTO                                                    -SKP
20101 002440    CLA,SEZ       A=000000  B=125252  E=0  O=0                  +SKP
20102 020102    JMP *         IOR-XOR FAILED
20103 021761    ADA ALT1      A=125252  B=125252  E=0  O=0
20104 021761    CPA ALT1                                                    -SKP
20105 002040    SEZ                                                         +SKP
20106 020106    JMP *         CLA OR ADA FAILED
20107 021760    ADA ALTO      A=177777  B=125252  E=0  O=0
20110 102301    SOS                                                         -SKP
20111 003002    CMA,SZA       A=000000  B=125252  E=0  O=0                  +SKP
20112 020112    JMP *         ADA FAILED
20113 003440    CCA,SEZ       A=177777  B=125252  E=0  O=0                  +SKP
20114 020114    JMP *         ADA FAILED
20115 021751    ADA M1        A=177776  B=125252  E=1  O=0
20116 021752    CPA .N2                                                     -SKP
20117 002041    SEZ,RSS                                                     +SKP
20120 020120    JMP *         ADA FAILED
```

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```
00372   20121 102301         SOS                                              -SKP
00373   20122 002101         CLE,RSS       A=177776  B=125252  E=0   O=0     +SKP
00374   20123 020123         JMP *         ADA FAILED
00375   20124 000000         ISZ A         A=177777  B=125252  E=0   O=0     -SKP
00376   20125 000000         ISZ A         A=000000  B=125252  E=0   O=0     +SKP
00377   20126 020126         JMP *         ISZ FAILED

00379   20127 021743         LDA B100K     A=100000  B=125252  E=0   O=0
00380   20130 021751         ADA M1        A=077777  B=125252  E=1   O=1
00381   20131 102201         SOC                                              -SKP
00382   20132 002141         SEZ,CLE,RSS   A=077777  B=125252  E=0   O=1     +SKP
00383   20133 020133         JMP *         ADA FAILED
00384   20134 103101         CLO           A=077777  B=125252  E=0   O=0
00385   20135 002004         INA           A=100000  B=125252  E=0   O=1
00386   20136 021743         CPA B100K                                        -SKP
00387   20137 002040         SEZ                                              +SKP
00388   20140 020140         JMP *         ADA FAILED
00389   20141 000001         LDA B         A=125252  B=125252  E=0 O=1
00390   20142 021761         CPA ALT1                                         -SKP
00391   20143 103301         SOS C         A=125252  B=125252  E=0   O=0     +SKP
00392   20144 020144         JMP *         B-REG. WAS MODIFIED

00394*      THE FOLLOWING SEQUENCE IS USED TO CHECK
00395*      JLA, JMP X,I, AND STA X,I
00396*
00397   20145 020207         LDA PTJPR     WILL GET RETURN ADDR IN A
00398   20146 000000         LDB A
00399   20147 100600         .JLA PTRTO    JLA TO PTRTO
        20150 020152
00400   20151 020151         JMP *         JLA FAILED
00401   20152 020206  PTRTO  CPA PTDF1     CORRECT RETURN ADDRESS?
00402   20153 002301         CCE,RSS       YES
00403   20154 020154         JMP *         NO
00404   20155 002400         CLA           CLEAR A
00405   20156 006400         CLB             &    B
00406   20157 101741         CAX             &    X
00407   20160 105751         CBY             &    Y
00408   20161 105762         JLY PTRT1     JMP & LOAD Y W/P+2
        20162 020164
00409   20163 020163         JMP *          DID NOT MAKE IT
00410   20164 002002  PTRT1  SZA           A STILL CLEAR ?
00411   20165 020165         JMP *
00412   20166 101754         CYA           COPY Y TO A
00413   20167 020211         CPA PTJYO     P+2 ?
00414   20170 006002         SZB            YEP , B STILL ZERO ?
00415   20171 020171         JMP *         LOOSE
```

```
20172 105744        CXB             CHECK X WHILE WE ARE AT IT
20173 006002        SZB              ?
20174 020174        JMP *            UH UH!
20175 020205        LDA PTDF0       SET PAGE ADDRESS
20176 021707        STA B1,I        PUT IT IN B-REG. INDIRECTLY
20177 000001        CPA B
20200 020205        LDA PTDF0,I
20201 021710        ADB B2          POINT PAST CONSTANTS & SUCH
20202 020210        CPA PTJMP       INDIRECT OK?
20203 000000        JMP 0           YES EXECUTE B-REG.
20204 020204        JMP *
20205 020210  PTDF0 DEF *+3
20206 020151  PTDF1 DEF PTRT0-1
20207 020152  PTJPR JMP PTRT0
20210 000001  PTJMP JMP 1,I
20211 020163  PTJY0 DEF PTRT1-1

20212 021762        LDA SRGP1           B-REG.       E        A-REG.
20213 000000        LDB A            1000100100100111 1
20214 021763        LDA SRGP2                         1 1001100000100000
20215 005025        BLS,ERB          1100100100100111 0
20216 005661        ELB,CLE,BRS      1100100100100111 0
20217 001124        ARS,ALR                           0 0001100000100000
20220 005026        BLS,ELB          0100100100100111 0
20221 005523        ERB,RBR          0100100100100111 0
20222 001720        ALF,ALS                           0 1000010000000010
20223 005124        BRS,BLR          0100100100100110 0
20224 001330        RAR,SLA,ALS                       0 0000010000000010
20225 005221        RBL,BRS          1100100100100110 0
20226 002300        CCE                               1
20227 001726        ALF,ELA                           0 1000000001000001
20230 001522        ERA,RAL                           1 1000000001000000
20231 005427        BLR,BLF          0010010011000001 1
20232 001122        ARS,RAL                           1 1000000001000001
20233 005220        RBL,BLS          0001001100000100 1
20234 001135        ARS,SLA,ERA                       0 1110000000010000
20235 020235        JMP *            SLA FAILED
20236 001623        ELA,RAR                           1 0110000000010000
20237 005327        RBR,BLF          1001100000100000
20240 002040        SEZ              CHECK E-REG.
20241 001460        ALR,CLE,ALS                         0000000001000000
20242 021764        CPA SRGP3
20243 102201        SOC
20244 020244        JMP *            SRG INST A-REG.
20245 000001        LDA B            CHANGE HANDS
20246 021763        CPA SRGP2
20247 006640        CLB,SEZ,CME
20250 020250        JMP *            SRG INST B-REG.
```

```
20251 102101      STO           START WITH O SET
20252 021767      LDA BEAUS     SET B=130272
20253 000000      LDB A           AND
20254 021765      LDA AEAUS         A=076310        E=1
20255 101021      ASR 1         A=037144  B=154135  E=1  O=0
20256 102301      SOS
20257 100117      RRL 15        A=066056  B=117462  E=1  O=0
20260 100022      ASL 2         A=130270  B=176311  E=1  O=1
20261 102201      SOC
20262 101100      RRR 16        A=176311  B=130270
20263 100041      LSL 1         A=174622  B=060561
20264 101025      ASR 5         A=107714  B=001413       O=0
20265 021770      CPA ASR.0     CHECK PRLIMINARY RESULTS
20266 102201      SOC
20267 020267      JMP *         EAU SHIFT FAILED
20270 101040      LSR 16        A=01413   B=0
20271 006002      SZB           INSURE B WAS CLEARED
20272 020272      JMP *         WAS NOT EAU SHIFT FAILED
20273 102101      STO
20274 100020      ASL 16        A=0       B=001413
20275 102301      SOS
20276 100026      ASL 6         A=0       B=041300
20277 102201      SOC
20300 101100      RRR 16        A=041300  B=0
20301 021771      CPA ASR.1     FINAL OK?
20302 006002      SZB
20303 020303      JMP *         NO EAU SHIFT FAILED
20304 021742      LDA B76K      A=076000  B=XXXXXX  E=X  O=X
20305 102101      STO                                    O=1
20306 100200      MPY B6412     A=154000  B=003120  E=X  O=0
20307 021740
20310 102201      SOC
20311 020311      JMP *         O WAS NOT CLEARED BY MPY
20312 100400      DIV ALT1      A=166416  B=020264
20313 021761
20314 100200      MPY MU2       A=156224  B=002046
20315 021772
20316 100400      DIV B7777     A=041161  B=007405
20317 021741
20320 100101      RRL 1         A=102342  B=017012
20321 100200      MPY ALT0      A=024412  B=15336
20322 021760
20323 100400      DIV B76K      A=125507  B=142412
20324 021742
20325 100200      MPY ALT1      A=161446  B=016075
20326 021761
20327 102101      STO                               O=1
20330 100400      DIV DV4       A=126760  B=006606
20331 021773
```

```
20332 021774         CPA RESUA     RESULT IN A
20333 102201         SOC           O=0
20334 020334         JMP *         MPY OR DIV FAILED
20335 101100         RRR 16        CHANGE HANDS
20336 021775         CPA RESUB     RESULT IN B
20337 020341         JMP *+2
20340 020340         JMP *         MPY OR DIV ERROR
20341 100400         DIV B1        TRY OVER FLOW
20342 021707
20343 102301         SOS           WAS IT ?
20344 020344         JMP *         NO
20345 100400         DIV .DO       TRY ZERO TO SET OVER FLOW
20346 021706
20347 102301         SOS           WAS IT ?
20350 020350         JMP *         NO
*                  TEST SBT AND LBT
20351 003004         CMA,INA
20352 021766         LDB BLBT      GET DEF TO LBT THING
20353 005200         RBL           MAKE IT A BYTE ADDRESS
20354 105763         LBT           A HAS HIGH BYTE
20355 001727         ALF,ALF
20356 000260         STA TEMP      SAVE ONE BYTE
20357 105763         LBT           GET OTHER BYTE
20360 000260         IOR TEMP      GET OTHER BYTE BACK
20361 021765         CPA AEAUS
20362 002001         RSS
20363 020363         JMP *


*
*
*     AT THIS POINT THE BASIC INSTRUCTION TEST HAS PASSED
*
*     VERY DESTRUCTIVE TEST OF 1K VCP RAM - CLEARS RAM MEMORY
*
*
20364 105745         LDX VCPTFLG  MUST SAVE AND RSTORE VCPTFLAG
20365 000304
20366 105755         LDY MLOST   must save and restore mlost flag bit
20367 000215
20370 021715         LDA B7
20371 003000         CMA
20372 102601         OTA CPUST     INDICATE IN BOOT RAM TEST
20373 021727         LDA B100      RAM MEMORY TEST
20374 006400         CLB
20375 101105   .MELO RRR 5
```

```
 20376 000000        STA @A       PUT ADDRESS IN LOCATION
 20377 000000        LDB A
 20400 000000        CPB @A       DID IT STORE?
 20401 007001        CMB,RSS      YES
 20402 020402        JMP *         BUMMER !
 20403 000000        STB @A       SAVE COMPLEMENT
 20404 000000        CPB @A
 20405 006401        CLB,RSS  NEXT LOCATION
 20406 020406        JMP *        DIDNT STORE, BAD BOOT RAM
 20407 000000        STB @A       STORE ZERO
 20410 000000        CPB @A       DID IT STORE?
 20411 002005        INA,RSS
 20412 020412        JMP *
 20413 100105        RRL 5        TEST BIT 10
 20414 002021        SSA,RSS      DONE 1K ?
 20415 020375        JMP .MELO    NOT YET
*
 20416 105743        STX VCPTFLG  RESTORE VCP TEST FLAG
 20417 000304
 20420 105753        STY MLOST    restore mlost bit
 20421 000215

*
*    THE BOOT RAM TEST HAS PASSED
*
*    SET UP TRAP CELLS
*
 20422 020000        LDA RVCODE
 20423 000205        STA SAVEB    REV CODE IN THE B REGISTER
 20424 021505        LDA ILDEF
 20425 000234        STA ILI      DEF TO ILINT IN LOCATION ILI
 20426 000232        STA PE
 20427 000233        STA TBG
 20430 000235        STA PFW      FOR NOW ALL INTERRUPTS ARE ILLEGAL
 20431 000236        STA MPT
 20432 021703        LDA UIT1     DEF TO UIT ROUTINE
 20433 000241        STA UIT
 20434 021716        LDA B11
 20435 021677        LDB ILJMP    JMP ILI,I IN ALL TRAP CELLS
 20436 000000  ILLP  STB A,I
 20437 002004        INA
 20440 021727        CPA B100     STOP AT LOCATION 77B
 20441 002001        RSS
 20442 020436        JMP ILLP
 20443 021676        LDA PFWJMP   SET UP OTHER TRAP CELLS
 20444 000004        STA 4
 20445 021673        LDA PEJMP
 20446 000005        STA 5
```

```
20447 000231         STA PEJMPI    SET UP FOR JSB IN PE TRAP CELL
20450 021700         LDA MPTJMP
20451 000007         STA 7
20452 021672         LDA TBGJMP
20453 000006         STA 6
20454 021702         LDA UITJSB
20455 000010         STA 10B
20456 021701         LDA UITJMP
20457 000240         STA UIJMPI
*
*     BASIC I/O ON CPU BOARD
*
20460 021733         LDA B170360   INDICATE (IF POSSIBLE) IN IO TEST
20461 102601         OTA CPUST
*
*
20462 102300         SFS 0         CHECK INTERRUPT FF
20463 102200         SFC 0
20464 021503         JMP PROER     INTERRUPT FF ERROR
*
20465 102202         SFC 2         CHECK GLOBAL REG.
20466 102302         SFS 2         SHOULD BE OFF (FLAG SET)
20467 021503         JMP PROER     GLOBAL REG. ERROR
*
20470 107706         CLC 6,C       INSURE TBG IS OFF
20471 102100         STF 0         TURN ON INTERRUPTS
20472 102200         SFC 0         CHECK IT
20473 102300         SFS 0
20474 021503         JMP PROER     INTERRUPTS NOT ON
20475 002400         CLA
20476 102600         OTA 0         CLEAR INTERRUPT MASK
20477 102604         OTA 4         CLEAR INTERRUPT REGISTER
20500 020507         LDA TBGDEF1
20501 000233         STA TBG       SET JUMP IN TRAP CELL
20502 103706         STC 6,C       TRY TIME BASE TIC
20503 002400         CLA           START COUNT AT ZERO
20504 002306         CCE,INA,SZA       NOW WAIT FOR TIC
20505 020504         JMP *-1
20506 021503         JMP PROER     LONG ENOUGH NOW ERROR

*
20507 020510 TBGDEF1 DEF ITBG      DEF TO TBG INTERRUPT
20510 103100 ITBG    CLF 0         TURN OF INTERRUPTS
20511 003004         CMA,INA       NEGATE COUNT FOR FUTURE USE
20512 001121         ARS,ARS
20513 001100         ARS           DIVIDE BY 8
20514 000245         STA TBGCNT    SAVE COUNT FOR 1.25 MS
```

```
20515 107706        CLC 6,C       TURN OFF TIC
20516 021505        LDA ILDEF
20517 000233        STA TBG       TBG IS ILLEGAL INT NOW
20520 102504        LIA 4         CHECK CENTRAL INTERRUPT
20521 021714        CPA B6        WAS IT THE TBG?
20522 102206        SFC 6         FLAG SHOULD STAY CLEAR
20523 021503        JMP PROER     NOT SO ERROR (OR CIR NOT = 6)
*
*                  DONT TEST TBG MASK BIT ON PROC SINCE NOT
*                  IMPLEMENTED ON A700
*     LIA CPUST
*     SSA          DID IT STAY CLEAR?
*     JMP PROER    NO PROCESSOR ERROR
*     LDA B2       NOW SET MASK BIT
*     OTA 0
*     LIA CPUST    GET MASK BIT
*     SSA,RSS      DID IT SET
*     JMP PROER    NO THEN ERROR
*     CLA          NOW RESTORE MASK BIT
*     OTA 0        IT WAS ORIGINALLY CLEAR
*
*
*                  SEE IF WE HAVE A VCP
*
20524 021720        LDB B20       first SELECT CODE TO TRY
20525 107602  VCPL  OTB GR,C      SET SELECT CODE
20526 021710        LDA B2        DIAGNOSE MODE 2
20527 102602        OTA GR        SET CARD
20530 102502        LIA GR        GET RESULT
20531 001710        ALF,SLA       BREAK BIT SET?
20532 020541        JMP VCPL1     YES, FOUND
*
20533 006004        INB           NEXT SELECT CODE
20534 021727        CPB B100      LAST SELECT CODE DONE??
20535 020552        JMP ION6      YES, NO VCP FOUND
*
20536 002400        CLA           TURN OFF DIAGNOSE MODE
20537 102602        OTA GR
20540 020525        JMP VCPL     GO AROUND AGAIN FOR NEW SELECT CODE
*
20541 003400  VCPL1 CCA
20542 000513        STA VCP.FLAG  GOOD VCP PRESENT !!!
20543 000514        STB VCPSC     VCP SELECT CODE
20544 002404        CLA,INA       DIAGNOSE MODE 1
20545 102602        OTA GR
20546 102502        LIA GR      GET RESPONSE
20547 021726        AND IDM     GET ID ONLY
20550 002003        SZA,RSS     IS TICK CARD??? (ZERO ID)
20551 000515        STB ASFLG   ASIC INTERFACE, NOT INTELLIGENT CARD
```

```
*
*
20552 002400  ION6  CLA            CLEAR DIAGNOSE MODE
20553 102602        OTA GR

*
*      START MEMORY ACCESS FOR FIRST TIME
*      CLEAR MEMORY IF IT WAS LOST DURING POWER DOWN
*      AND CHECK MEMORY BUT DON'T DESTROY ANY DATA IF NOT LOST
*
20554 000215  MTST  LDA MLOST      GET MLOST BIT
20555 001200        RAL            PUT MLOST BIT IN SIGN
20556 000304        IOR VCPTFLG    SAVE MEMORY IF TESTING
20557 000215        STA MLOST      YES    INDICATE MEMORY NOT LOST
20560 021732        LDA B100340    INDICATE IN MEMORY TEST
20561 102601        OTA CPUST
20562 000302        STA PEADD      NEGATIVE NUMBER FOR NO PARITY ERROR
*
20563 021047        LDB PFWDEF1    GET DEF TO PFW HANDLER FOR MEM TEST
20564 000235        STB PFW        PUT IN CELL, ALL OTHER INTS ARE
                                      ILLEGAL FOR NOW
20565               LWD1           POINT AT MAP ZERO
20566 021706        DEF .DO
20567 102704        STC 4          TURN ON POWER FAIL INTERRUPTS  (IS
                                      THIS RIGHT??????)
20570               SMAP           GET MAP ZERO DATA
20571 021706        DEF .DO
20572 000370  ..MBUF DEF MPBUF     TEST MAP ZERO FOR CORRECT INITIAL-
                                      IZATION
20573 002400        CLA
20574 020572        LDB ..MBUF     GET POINTER TO MAP BUFFER
*
20575 000001  MPLP  CPA B,I        IS MAP RIGHT?
20576 002001        RSS
20577 020774        JMP MTSTE      NO, GO REPORT ERROR
20600 002004        INA
20601 006004        INB            NEXT ADDRESS AND VALUE
20602 021723        CPA B40        DONE??
20603 002001        RSS            YES  GO SET UP FOR FIRST 32K CHECK
20604 020575        JMP MPLP       NO, GO AROUND LOOP AGAIN
20605 003400        CCA
20606 000366        STA MAP
```

```
*
*                   SET UP MAP FOR NEXT 32K AND CHECK PARITY SYSTEM
*
20607 000366  MTSTM LDA MAP       CHECK IF END OF MEMORY
20610 002004        INA           MOVE TO NEXT BLOCK
20611 000366        STA MAP
20612 021735        CPA B1000     IS IT END OF ADDRESSABLE MEMORY ?
20613 021072        JMP MTST5     YES
20614 105762        JLY STMAP     SET UP NEXT MAP
20615 027647
*                   CHECK FIRST WORD TO SEE IF MEMORY THERE
20616 106705        CLC 5         disable parity interrupts
20617 006400        CLB
20620 000215        LDA MLOST     POINT AT FIRST WORD
20621 002021        SSA,RSS       WAS MEMORY LOST?
20622 020626        JMP MTM1      YES,SKIP LOAD
*
20623 002400        CLA
20624               XLB1 '@A'   READ A WORD
20626 007000  MTM1  CMB
20627 002400        CLA
20630               XSB1 '@A'   COMPLEMENT AND STORE
20632               XSB1 '@A'   STORE AGAIN FOR RAM POWER UP PROBLEM
20634               XCB1 '@A'   GET DATA BACK
20636 007001        CMB,RSS     COMPLEMENT DATA BACK
20637 021072        JMP MTST5   DIDNT STORE, END OF MEMORY
*
20640 002400        CLA           ADDRESS ZERO AGAIN
20641               XSB1 '@A'     STORE ORIGINAL DATA BACK
20643               XCB1 '@A'     DID IT STORE?
20645 002001        RSS           YES, GO TEST NEXT 32K
20646 021072        JMP MTST5     FOUND END OF MEMORY
*
*
20647 021071  MTST3 LDA PEDEF2    POINT PE TRAP AT OTHER ENTRY
20650 000232        STA PE
20651 000366        LDB MAP
20652 005100        BRS           MAP OVER 2 FOR WHICH 64K BLOCK
20653 021736        ADB B1400     ADD START OF LOGGING RAM
20654 000503        STB TEMPO     SAVE ADDRESS
20655 000215        LDA MLOST     WAS MEMORY LOST??
20656 002020        SSA
20657               XLB1 '1700B'  GET CURRENT DATA
20661 002400        CLA
20662               XSA1 '1700B'  GET DATA
20664 102105        STF 5         CHANGE PARITY SENSE
20665 021707        XOR B1        MAKE IT A ONE BIT ERROR
20666               XSA1 '1700B'  ESTABLISH BAD PARITY
```

```
20670 103105         CLF 5          REVERSE SENSE
20671 102705         STC 5          ENABLE PARITY
20672                XLA1 '1700B'   READ BAD PARITY
20674 002002         SZA            CORRECTED??
20675 020774         JMP MTSTE      NO, ERROR
20676 000503         LDA TEMP0,I    GET ERROR LOG
20677 002003         SZA,RSS        ERROR LOGGED AND CORRECTED??
20700 020774         JMP MTSTE      IT DIDN'T SO ERROR
20701 000247         ISZ ECCCNT
20702 002400         CLA
20703 000503         STA TEMP0,I    CLEAR ERROR LOGGING RAM
20704                XSA1 '1700B'   RESTORE GOOD PARITY
20706 102105         STF 5
20707 021711         XOR B3         MAKE TWO BIT ERROR
20710                XSA1 '1700B'   STORE BAD PARITY
20712 103105         CLF 5
20713                XLA1 '1700B'   READ BAD PARITY
20715 020774         JMP MTSTE      NO PARITY ERROR, BAD PARITY SYSTEM
*

20716          MTST4 LWD1          PUT DATA 1 MAP BACK LIKE IT WAS
20717 021706         DEF .D0
20720                XSB1 '1700B' RESTORE GOOD PARITY TO LOCATON 1700
20722 021004         LDA PEDEF1
20723 000232         STA PE        PARITY ERRORS TO OTHER HANDLER NOW
20724 102705         STC 5         TURN PARITY INTS BACK ON AGAIN
*
20725 000215   MTST0 LDA MLOST    TEST A 32K BLOCK OF MEMORY
20726 002021         SSA,RSS      IF MEMORY WAS LOST SKIP LOADING DATA

20727 020740         JMP MTSTL     MEMORY CONTENTS LOST
*
20730 002400         CLA           CLEAR A AND B TO COPY DATA TO SELF
20731 006400         CLB
20732 105745         LDX B77777    COUNT FOR 32K
20733 021744
20734                MW11          READ EVERY LOCATION TO CHECK PARITY
20735                XLA1 '@A'     READ LAST LOCATION
20737 020607         JMP MTSTM
*
20740 007400   MTSTL CCB           MAKE ALL ONES
20741 002400         CLA
20742                XSB1 '@A'     STORE IT IN FIRST LOCATION
20744 007004         CMB,INB       MAKE B ONE
20745 105745         LDX B77777    COUNT FOR 32K
20746 021744
20747                MW11          WRITE ONES IN EVERY LOCATION AND
                                      READ BACK
```

```
20750                XLB1 '@A'    READ THE LAST LOCATION
20752 006006         INB,SZB      IS IT ONES???
20753 020774         JMP MTSTE    NO, MEMORY ERROR
20754 002400         CLA
20755 006400         CLB
20756                XSB1 '@A'    STORE ZERO IN FIRST LOCATION
20760 006004         INB
20761 105745         LDX B77777   COUNT FOR 32K
20762 021744
20763                MW11         WRITE ZERO IN ALL LOCATIONS & READ
20764                XLB1 '@A'    READ LAST LOCATION
20766 006002         SZB          IS IT ZEROS
20767 020774         JMP MTSTE    NO, MEMORY ERROR
20770 000503         LDA TEMPO,I  GET ERROR LOG
20771 002002         SZA          ZERO STILL??
20772 000250         ISZ CORCNT   ONE MORE CORRECTION
20773 020607         JMP MTSTM


*     MEMORY ERROR ROUTINE
*     EXTENDED MEMORY ERROR DISPLAY
*
20774 002400   MTSTE CLA
20775 105762         JLY STMAP    PUT MAP ZERO BACK
20776 027647
20777 000366         LDA MAP      GET 32K BLOCK ADDRESS
21000 000246         STA MSIZE    SAVE MEMORY SIZE
21001 001727         ALF,ALF      PUT IT IN UPPER HALF
21002 021732         IOR B100340  ADD EXTENDED MEMORY SECTION
21003 021515         JMP DSPLY    GO DISPLAY IT
*
*     PARITY INTERRUPT ROUTINE
*     A SOFT ERROR WILL NOT CAUSE CPU TO STOP
*
21004 021005   PEDEF1 DEF IPRTY   DEF TO PARITY HANDLER
21005          IPRTY LWD1         RESTORE DATA 1 MAP (KILLED BY
                                     INTERRUPT)
21006 021706         DEF .DO
21007 000215         LDA MLOST    MEMORY LOST??
21010 002021         SSA,RSS      NO, CHECK FOR SOFT ERROR
21011 020774         JMP MTSTE    YES, NO SOFT ERRORS IF MEMORY LOST
*
21012 002400         CLA
21013 105762         JLY STMAP    SET UP MAP TO FIRST 32K
21014 027647
21015 006400         CLB
21016 000215         STB MLOST    MEMORY LOST NOW
21017                XSB1 '4'     CLEAR RESTART CONDITION
```

```
21021 000366        LDA MAP
21022 000303        STA PEMAP    SAVE BLOCK WITH PARITY ERROR
21023 105762        JLY STMAP    SET MAP BACK LIKE BEFORE
21024 027647
21025 102505        LIA 5
21026 021744        AND B77777
21027 000302        STA PEADD    SAVE ADDRESS OF THIS PARITY ERROR
21030 007400        CCB
21031               XSB1 '@A'    RESTORE GOOD PARITY TO LOCATION
21033               XCB1 '@A'    READ IT BACK
21035 006005        INB,RSS
21036 020774        JMP MTSTE    NO, A REAL MEMORY PROBLEM
*
21037               XSB1 '@A'    STORE ZEROS
21041               XLB1 '@A'
21043 006002        SZB          WAS A SOFT ERROR
21044 020774        JMP MTSTE    NO, REAL MEMORY PROBLEM
*
21045 102705        STC 5        TURN ON PARITY INTS AGAIN
21046 020725        JMP MTST0    GO TEST THIS 32 K AGAIN

*                POWER GOING DOWN
21047 021050 PFWDEF1 DEF PDOWN   POWER DOWN DEF
21050 106704 PDOWN CLC 4         TURN OF POWERFAIL INTERRUPTS
21051               LWD1         RESTORE DATA 1 MAP
21052 021706        DEF .D0
21053 000302        LDA PEADD    YES CHECK IF THERE
21054 002020        SSA            WAS A PARITY ERROR
21055 021065        JMP IPF      NO
*
21056               XLA1 '@A'
21060 021711        XOR B3       MAKE TWO BIT ERROR
21061 102105        STF 5        YES - CHANGE PARITY SENSE
21062               XSB1 '@A'    WRITE AN ERROR
21064 103105        CLF 5        PUT PARITY BACK
21065 102304 IPF    SFS 4        WAIT FOR POWER TO GO DOWN
21066 021065        JMP IPF
21067 107700        CLC 0,C      TURN OFF MACHINE
21070 020002        JMP START    DIDN'T GO ALL THE WAY SO RESTART
*
21071 020716 PEDEF2 DEF MTST4    PARITY TEST ENTRY
*
21072 000366 MTST5 LDA MAP       GET LAST BLOCK NO.
21073 000246        STA MSIZE    SAVE MEMORY SIZE
21074 002003        SZA,RSS
21075 020774        JMP MTSTE    GO SAY NO MEMORY ERROR
21076 002400        CLA
21077 000366        STA MAP      RESET MAP ZERO
```

```
21100 105762         JLY STMAP
21101 027647
*
21102 103100         CLF 0         RESET THINGS
21103 102704         STC 4         REENABLE ALSO
21104 021720         LDA B20
21105 021735         LDB B1000
21106 105745         LDX B100      SAVE TRAP CELL AREA OF MAIN MEMORY
21107 021727
21110                MW10
21111 003400         CCA
21112 000305         STA TRAPFLAG  FLAG THAT TRAP CELLS ARE SWAPPED
21113 000510         STA NDCLR     NEED TO PRESET IF BREAK DURING
                                     IO TEST
21114 021671         LDA IOLP      SET POINTER FOR I/O TABLE
21115 000503         STA TEMP0
21116 002004         INA
21117 000502         STA TEMP1     SAVE PAGE ADDRESS

*     START OF I-O INTERFACE CHIP TESTS
*
*     USE DIAG. MODE 1 TO BUILD A SELECT CODE TABLE
*
21120 021747         LDA B177700  INDICATE IN IO INTERFACES
21121 102601         OTA CPUST
21122 102102         STF 2        INSURE GLOBAL REGISTER IS OFF
21123 002404         CLA,INA      SET TEST MODE 1 (PRIORITY RESPONSE)
21124 102602         OTA 2        GIVE MODE TO  CHIPS
21125 002400   IOL0  CLA          INCASE OF NO RESPONSE
21126 000503         ISZ TEMP0
21127 000503         STA TEMP0,I  GET TABLE POINTER
21130 102502         LIA 2        GET SELECT CODE
21131 002003         SZA,RSS      ANY SELECT CODE
21132 021157         JMP IONO     NO END-OF-IO CHIPS
21133 021725         AND SCM      YES - USE SELECT CODE ONLY
21134 000503         STA TEMP0,I  PUT IT IN TABLE
21135 001665         ELA,CLE,ERA
21136 021753         ADA .N20     SUBTRACT 20B
21137 002020         SSA          IS IT A VALID SELECT CODE?
21140 021155         JMP IOE4     NO - INDICATE ERROR 4 ON LEDS
21141 000502         LDA TEMP1    CHECK FOR DUPLICATE SELECT CODES
21142 000503   IOL1  CPA TEMP0    END OF TABLE?
21143 021125         JMP IOL0     YES MOVE TO NEXT IO CHIP
21144 000000         LDB A,I      GET SC FROM TABLE
21145 005665         ELB,CLE,ERB
21146 000503         CPB TEMP0,I  IS IT THE SAME AS THE NEW SC?
21147 021152         JMP *+3      YES-DUPLICATE SELECT CODES ERROR 3
21150 002004         INA
21151 021142         JMP IOL1     NO DO NEXT ENTRY
```

```
*
21152 000205        STB SAVEB    DUPLICATE SELECT CODE IN B REGISTER
21153 021711        LDA B3
21154 021513        JMP IOER
21155 021712  IOE4  LDA B4
21156 021513        JMP IOER

*     CHECK IF ANY SELECT CODES DID NOT RESPOND TO MODE 1
*     IF THEY DIDN'T PRIORITY CHAIN IS BROKEN
*
21157 102102  IONO  STF 2        INSURE GLOBAL REGISTER IS OFF
21160 002400        CLA          TURN OFF DIAGNOSE MODE
21161 102602        OTA 2
21162 021717        LDA B17      START WITH FIRST SELECT CODE -1
21163 000477        STA PO.CT
21164 000477  IOL2  ISZ PO.CT    MOVE TO NEXT SC
21165 000502        LDA TEMP1    CHECK IF IN TABLE
21166 000000  IOL3  LDB A,I      GET SC FROM TABLE
21167 006003        SZB,RSS      END OF TABLE?
21170 021176        JMP ION1     YES
21171 005665        ELB,CLE,ERB
21172 000477        CPB PO.CT    NO IS SC IN TABLE?
21173 021164        JMP IOL2     YES
21174 002004        INA
21175 021166        JMP IOL3     NO MOVE TO NEXT ENTRY
21176 000477  ION1  LDA PO.CT    GET SC
21177 021727        CPA B100     END OF SC'S
21200 021210        JMP ION2     YES
21201 102602        OTA 2        NO TRY IT
21202 002400        CLA
21203 102502        LIA 2
21204 002003        SZA,RSS      DID IT COME BACK?
21205 021164        JMP IOL2     NO MOVE TO NEXT ONE
21206 021710        LDA B2       YES - INDICATE ERROR 2
21207 021513        JMP IOER

*     CHECK INDIVIDUAL I/O CHIPS
*
21210 000502  ION2  LDB TEMP1,I  START IO CHECK WITH FIRST ENTRY
21211 002400        CLA
21212 006003        SZB,RSS      WERE THERE ANY ENTRIES?
21213 021513        JMP IOER     NO IO CHIPS PRESENT ERROR 0
21214 021275        LDA IOIDEF   SET UP DEF FOR TRAP CELL JUMP
21215 000242        STA INTIO
21216 000502        LDB TEMP1    GET SC TABLE POINTER
21217 000503        STB TEMPO    SET POINTER
21220 000503  IOL4  LDB TEMPO,I  GET SELECT CODE
21221 006103        CLE,SZB,RSS  END OF TABLE?
21222 021332        JMP ION3     YES CHECK FOR BREAK ENABLE
```

```
*
21223 105762        JLY CHKIO      CHECK I/O CHIP ON THIS CARD
21224 021546
21225 021512        JMP IOESC       * DISPLAY SELECT CODE WITH ERROR
*
*    CHECK DMA AND INTERRUPTS
*
21226 000503        LDA TEMPO,I    GET SELECT CODE
21227 021724        AND B77        MASK TO SELECT CODE
21230 103602        OTA GR,C       SET GLOBAL REGISTER
21231 021675        LDB IOIJMP
21232 000000        STB A,I       PUT I/O INTERRUPT JUMP IN TRAP CELL
21233 021720        LDA B20
21234 021720        LDB B20
21235 105745        LDX B100       UPDATE TRAP CELL AREA FOR THIS
21236 021727                          INTERRUPT
21237               MW01
21240 021330        LDA DMACF      INCLUDE DMA ADDRESS
21241 102620        OTA 20B        PASS IT TO SELF CONFIGURATION REG
21242               XSA1 'DMA+1'      AND PLACE IN TRIPLET
21244 021327        LDA DMAQD      GET DMA CONTROL WORD
21245               XSA1 'DMA'
21247 021331        LDA DMAQD+2       AND COUNT
21250               XSA1 'DMA+2'
21252 021715        LDA B7         DISABLE SRQ INTERRUPTS
21253 102602        OTA 2          DIAGNOSE MODE 7!!! MUST CLC 0,C TO
                                      GET OUT OF THIS MODE
21254 103720        STC 20B,C      DO SELFCONFIGURATION
21255 102324        SFS 24B        DID IT COMPLETE
21256 021512        JMP IOESC      NO SO ERROR
21257 102521        LIA 21B        CHECK CONTROL WORD
21260 021327        CPA DMAQD
21261 002001        RSS
21262 021512        JMP IOESC      BAD SO ERROR
21263 102523        LIA 23B        CHECK COUNT
21264 021331        CPA DMAQD+2
21265 002001        RSS
21266 021512        JMP IOESC      NO GOOD SO ERROR
21267 021711        LDA B3         NOW USE DIAG. MODE 3
21270 102602        OTA 2
21271 102100        STF 0          TURN ON INTERRUPTS
21272 002006        INA,SZA        WAIT FOR IT
21273 021272        JMP *-1
21274 021512        JMP IOESC      NO GOOD
*
```

```
21275 021276 IOIDEF DEF IOINT     DEF FOR TRAP CEEL
21276        IOINT  LWD1          PUT DATA 1 MAP BACK
21277 021706        DEF .D0
21300 102504        LIA 4         CHECK CENTRAL INTERRUPT
21301 106502        LIB 2         AGAINST GLOBAL REGISTER
21302 000001        CPA B         WELL?
21303 002001        RSS
21304 021512        JMP IOESC     CARD ERROR
21305 021330        LDB DMACF
21306 021713        ADB B5        MOVE TO CONFIGURATION ADDRESS
21307               XCB1 'DMA+2'  DID IT STORE
21311 102224        SFC 24B       AND DID IT TURN OFF
21312 021512        JMP IOESC     NO SO ERROR
21313 102523        LIA 23B       CHECK COUNT IS ZERO
21314 002002        SZA
21315 021512        JMP IOESC
21316 107720        CLC 20B,C     INSURE DMA IS OFF
21317 107721        CLC 21B,C
21320 000503        LDA TEMP0,I   GET SELECT CODE
21321 021724        AND B77
21322 021674        LDB ILIJMP    PUT TRAP CELL BACK TO ILLEGAL
                                     INTERRUPT
21323 000000        STB A,I
21324 000503        ISZ TEMP0     MOVE TO NEXT ENTRY
21325 000204        ISZ SAVEA     COUNT THIS I/O CARD
21326 021220        JMP IOL4      AND DO IT
*
      001760 DMA    EQU 1760B
21327 000200 DMAQD  OCT 200
21330 001760 DMACF  DEF DMA
21331 177775        DEC -3


*     CHECK THAT ONLY ONE INTF. HAS A BREAK ENABLE
*     NONE IS OK
*
21332 021710 ION3   LDA B2        USE DIAGNOSE MODE 2
21333 000502        LDB TEMP1     SET POINTER FOR SELECT CODE
21334 000503        STB TEMP0
21335 006400        CLB
21336 000501        STB TEMP2     CLEAR SC FLAG
21337 102102        STF 2         TURN OFF GLOBAL REGISTER
21340 102602        OTA 2
21341 002400 IOL5   CLA           CLEAR IN CASE OF NO RESPONSE
21342 102502        LIA 2         GET PARAMETERS
21343 002002        SZA           DONE WITH I O
21344 021350        JMP ION4      NO
21345 102602        OTA 2         TURN OFF DIAG.MODE 2
21346 006400        CLB           NO ERRORS
```

```
01097  21347 021364         JMP PTSTX     YES NOW CHECK IF VCP OR LOADER
01098  21350 001710  ION4   ALF,SLA       CHECK BREAK ENABLE BIT
01099  21351 021354         JMP *+3
01100  21352 000503         ISZ TEMP0     MOVE TO NEXT ONE
01101  21353 021341         JMP IOL5
01102  21354 002740         CLA,SEZ,CCE     WAS THERE A PREVIOUS ONE
01103  21355 021361         JMP IOEN4     YES SO ERROR 1
01104  21356 000503         LDB TEMP0     NO OK SAVE THIS ONE
01105  21357 000501         STB TEMP2
01106  21360 021341         JMP IOL5      NOW TRY NEXT ONE
01107*
01108  21361 000513  IOEN4  STA VCP.FLAG  NO VCP IF TWO BREAK ENABLES
01109  21362 002004         INA
01110  21363 021513         JMP IOER      DISPLAY ERROR 1

01112*
01113*     PRETEST EXIT TO VFP
01114*     PRETEST IS FINISHED
01115*
01116  21364 105762  PTSTX  JLY .PSET     CLEAR I/O SYSTEM FROM DIAGNOSE
       21365 021633                          MODE 7
01117  21366 021776         LDA ..ENT
01118  21367 102603         OTA 3         INITIALIZE BREAK ENTRY POINT
01119  21370 103603         OTA 3,C
01120  21371 000305         LDA TRAPFLAG  CHECK VCP TEST
01121  21372 002003         SZA,RSS
01122  21373 021401         JMP PTS2
01123  21374 021735         LDA B1000
01124  21375 021720         LDB B20
01125  21376 105745         LDX B100
       21377 021727
01126  21400                MW01        RESTORE TRAP CELL AREA OF MAIN MEMRY
01127  21401 000304  PTS2   LDA VCPTFLG   CHECK VCP TEST
01128  21402 002020         SSA
01129  21403 021471         JMP PTS1      IF TEST DONT CHECK SWITCHES
01130*
01131  21404 102501         LIA CPUST     GET SWITCHES
01132  21405 001727         ALF,ALF
01133  21406 021715         AND B7       SELF TEST LOOP??
01134  21407 002003         SZA,RSS
01135  21410 020002         JMP START     YES, GO AROUND AGAIN
01136*
01137  21411 000244         LDB DISPLAY   GET SELF TEST STATUS
01138  21412 006002         SZB           DID SELF TEST PASS
01139  21413 021471         JMP PTS1      NO, MUST GO TO VCP
01140*
01141  21414 021712         CPA B4        LOOP ON SELF TEST
01142  21415 020002         JMP START     YES, GO AROUND AGAIN
```

```
*
21416 021710        CPA B2        JMP TO USER ROM??
21417 021437        JMP ..USER,I  YES, GO
*
*    IF USER WANTS TO CONTINUE TO VCP MUST ENTER AT VCP IN PAGE 1
*    NOTE THAT USER ROM WILL NOT BE ENTERED IF SELF TEST FAILS
*
*    NOW SEE IF CAN AUTO RESTART
*
21420 002011        SLA,RSS
21421 021440        JMP PTS0      AUTO RESTART NOT ENABLED
*
21422 000215        LDB MLOST     CHECK MEMLOST
21423 006021        SSB,RSS       SKIP IF MEMORY SAVED
21424 021440        JMP PTS0      MEMORY LOST, GOTO VCP
*
21425               XLB1 '4'      GET TRAP CELL FOR AUTO RESTART
21427 006003        SZB,RSS       IS INSTRUCTION THERE?
21430 021440        JMP PTS0      NO INSTRUCTION, GOTO VCP
*
21431 102702        STC 2         ENABLE BREAK
21432 002400        CLA
21433 102601        OTA CPUST     INDICATE USER PROGRAM EXECUTING
21434               XJMP '.D0','4'  JUMP TO LOCATION 4 IN SYSTEM MAP
*
21437 030002 ..USER DEF 30002B   START OF USER ROM
*
*    CANT AUTO RESTART, SEE IF MUST AUTOLOAD
*
21440 021715 PTS0   CPA B7     DISC LOADER
21441 021455        JMP .PTDC,I   GO DO DISC LOADR
*
21442 021711        CPA B3
21443 021456        JMP PTDS      DS LOADER
*
21444 021713        CPA B5
21445 021447        JMP PTRM   PROM LOADER
*
21446 021471        JMP PTS1   NO, LOADR, GO TO VCP
*
21447 021705 PTRM   LDA .RMSC
21450 000264        STA SCETC      DEFAULT SELECT CODE
21451 104600        .JLB RMLDR      LOAD FROM ROM CARD
21452 026364
21453 021465        JMP .MRBT,I     GO START IT UP
21454 021466        JMP PTLER       GO REPORT ERROR
*
21455 026503 .PTDC DEF PTDC       DISC LOADER
```

```
*
21456 021704  PTDS  LDA .DSSC      DS AUTOBOOT
21457 000264        STA SCETC      SAVE DEFAULT SELECT CODE ETC
21460 104600        .JLB DSLD      LOAD FROM DS
21461 025040
21462 002001        RSS
21463 021466        JMP PTLER      ERROR, GOTO VCP
21464 021465        JMP .MRBT,I
*
21465 024072  .MRBT DEF MRBT      GO SET UP BOOT PARAMS
*
21466 021470  PTLER LDA DSCER        DISC ERROR CODE
21467 021515        JMP DSPLY
*
21470 100200  DSCER OCT 100200
*
*
*     GO TO VCP IF POSSIBLE
*
21471 000513  PTS1  LDA VCP.FLAG  IS THERE A VCP??
21472 002003        SZA,RSS
21473 021501        JMP NVCP      NO, NOTHING MORE TO DO
*
21474 102702        STC 2         ENABLE BREAK
21475 021715        LDA B7
21476 102601        OTA CPUST     SAY IN FRONT PANEL
21477 021500        JMP *+1,I
21500 022000        DEF VFP
*
*
21501 021713  NVCP LDA B5         ERROR 5, NO VCP
21502 021513        JMP IOER


*     ERROR REPORTING TO PROCESSOR LEDS
*
21503 021733  PROER LDA B170360      INDICATE PROCESSOR ERROR
21504 021515        JMP DSPLY
*
*
21505 021506  ILDEF DEF ILINT     POINT TO ILEGAL INT ROUTINE
21506 102504  ILINT LIA 4B        GET CENTRAL INTERRUPT REGISTER
21507 001727        ALF,ALF       PUT IT IN DATA
21510 021731        IOR B100300      INDICATE ILLEGAL INTERRUPT
21511 021515        JMP DSPLY
```

```
*
21512 000503  IOESC LDA TEMPO,I   GET SELECT CODE FOR DISPLAY
21513 001727  IOER  ALF,ALF       PUT DATA IN UPPER HALF
21514 021731        IOR B100300     INDICATE IO TEST ERROR

*      DISPLAY LOWER BYTE (SECTION)
*         THEN UPPER BYTE (DATA    )
*         THEN BACK TO LOWER BYTE
*
21515 000244  DSPLY STA DISPLAY   SAVE DATA AND SECTION
*
21516 000244  POCOO LDA DISPLAY
21517 002300        CCE           SET TO DO SECOND PART
21520 021734        AND B377
21521 102601        OTA CPUST
21522 021753        LDB .N20
21523 000000        ISZ A
21524 021523        JMP *-1
21525 000001        ISZ B
21526 021523        JMP *-3
21527 002041        SEZ,RSS
21530 021535        JMP PRTLP
21531 000244        LDA DISPLAY
21532 001767        ALF,CLE,ALF
21533 021755        IOR BIT7
21534 021520        JMP POCOO+2   UPPER HALF  DATA
*
21535 102501  PRTLP LIA CPUST     CHECK IF LOOP
21536 001727        ALF,ALF
21537 021715        AND B7
21540 002003        SZA,RSS       ??
21541 021067        JMP IPF+2     YES LOOP ON ERROR
*
21542 000513        LDA VCP.FLAG  IS THERE A VCP??
21543 002002        SZA
21544 021364        JMP PTSTX     GO TO VCP
21545 021516        JMP POCOO
```

```
*
*
*
*     CHECK AN I/O CARD B HAS SELECT CODE TO CHECK
*
*
21546 005623  CHKIO ELB,RBR       SAVE SELF TEST FLAG
21547 107602        OTB GR,C      SET GLOBAL REGISTER
21550 002400        CLA           CLEAR IN CASE OF NO RESPONSE
21551 102502        LIA GR        GET GLOBAL REGISTER
21552 000001        CPA B         DID IT COME BACK ?
21553 002001        RSS           YES
21554 105772  CHBR  JPY 0         NO ERROR
21555 000000
21556 002041        SEZ,RSS      DOES THIS INTERFACE HAVE SELF TEST
21557 021574        JMP ION.2    NO - THEN DON'T WAIT
21560 021754        LDA .N40     YES THEN WAIT 10 SECS FOR SELF TEST
21561 102230        SFC DATA                    !!!!!!!!!!
21562 021570        JMP ION.1
21563 000001        ISZ B
21564 021561        JMP *-3
21565 000000        ISZ A
21566 021561        JMP *-5
21567 021554        JMP CHBR     TIME OUT SO ERROR
21570 103530  ION.1 LIA DATA,C   GET SELF TEST STATUS & CLEAR FLAG
21571 002020        SSA          WAS IT GOOD?
21572 000010        SLA
21573 021554        JMP CHBR      NO SO ERROR

21574 021760  ION.2 LDA ALTO      USE ALTERNATING PATTERN
21575 102623        OTA 23B         TO CHECK I/O CHIP BUS UPPER
21576 001300        RAR           AND OPPSITE PATTERN
21577 102624        OTA 24B         FOR I/O CHIP BUS LOWER
21600 007400        CCB           CLEAR INCASE NO RESPONSE
21601 102523        LIA 23B       READ PATTERNS BACK
21602 106524        LIB 24B
21603 005200        RBL
21604 000001        CPA B         DO PATTERNS AGREE
21605 006401        CLB,RSS       YES
21606 021554        JMP CHBR      NO - I/O CHIP BUS ERROR
21607 102624        OTA 24B       REVERSE PATTERN AND
21610 001300        RAR           CHECK BUS AGAIN
21611 102623        OTA 23B
21612 102524        LIA 24B
21613 106523        LIB 23B
21614 005200        RBL
```

```
21615 000001         CPA B         DO PATTERNS AGREE?
21616 102230         SFC DATA      YES CHECK FLAG
21617 021554         JMP CHBR      BUS OR FLAG ERROR
21620 102130         STF DATA      SET THE I O FLAG
21621 102230         SFC DATA      DID IT GET SET?
21622 102330         SFS DATA
21623 021554         JMP CHBR      NO I/O FLAG ERROR
21624 103130         CLF DATA      NOW CLEAR IT
21625 102330         SFS DATA      DID IT GET CLEARED
21626 102230         SFC DATA
21627 021554         JMP CHBR      NO I/O FLAG ERROR
*
21630 106723         CLC 23B       RESET DMA MACHINE
21631 105772         JPY 1         P+3 (GOOD) RETURN
21632 000001
*
*
21633 104600  .PSET .JLB ENDVCP    EXIT FROM VCP MODE
21634 023533
21635 107700         CLC 0,C       BLOW AWAY I/O SYSTEM
21636 021746         LDA B100000
21637 000211         STA SAVEQ     CS MODE IS OFF!
21640 002400         CLA
21641 000214         STA SAVEW     CLEAR WMAP
21642 000366         STA MAP
21643 000200         STA SAVEI     INTS OFF
21644 000206         STA SAVEG     GLOBAL REG OFF
21645                LWD1          POINT DATA 1 MAP
21646 000000         DEF 0
21647 021650         JMP *+1,I   SET UP MAP ZERO
21650 027647         DEF STMAP
*
*  UIT HANDLER TO IGNORE UITS FOR R3 INSTRUCTIONS
*
21651 000227  UITINT STA PETMP
21652 000214         LDA SAVEW
21653 021722         AND .B37
21654                LWD1
21655 000000         DEF A
21656 000227         LDA PETMP
21657 000237         JMP UITRTN,I
*
```

```
*
*
*  PARITY ERROR HANDLER FOR USER INTERFACE.  IT SETS PEFLAG
*  SO THAT PARITY ERROR WILL BE OUTPUT BEFORE NEXT COMMAND ACCEPTED
*
 21660 000227  PEINT STA PETMP     SAVE A REGISTER
 21661 000214        LDA SAVEW     SET DATA ONE MAP BACK LIKE BEFORE
 21662 021722        AND .B37
 21663               LWD1
 21664 000000        DEF A
 21665 000227        LDA PETMP     RESTORE A REGISTER
 21666 102705        STC 5         TURN PARITY INTERRUPTS BACK ON
 21667 000243        ISZ PEFLAG
 21670 000230        JMP PERTN,I   GO GET ANOTHER COMMAND
*

*
*     CONSTANTS
*
*IOLP  DEF P0.CT-77B-P0-1
 21671 000370  IOLP  DEF MPBUF     PLACE FOR I/O SELECT CODE TABLE
 21672 000233  TBGJMP JMP TBG,I      TRAP CELL INSTRUCTION FOR TBG
 21673 000232  PEJMP JMP PE,I      "    "         "        "  PARITY
 21674 000234  ILIJMP JMP ILI,I
 21675 000242  IOIJMP JMP INTIO,I  I/O TRAP CELL CONTNTS
 21676 000235  PFWJMP JMP PFW,I     ETC.
 21677 000234  ILJMP  JMP ILI,I
 21700 000236  MPTJMP JMP MPT,I
 21701 000241  UITJMP JMP UIT,I
 21702 000237  UITJSB JSB UITRTN
 21703 021651  UIT1   DEF UITINT
 21704 000024  .DSSC OCT 0024
 21705 000022  .RMSC OCT 22
*
 21706 000000  .D0   OCT 0
 21707 000001  B1    OCT 1
 21710 000002  B2    OCT 2
 21711 000003  B3    OCT 3
 21712 000004  B4    OCT 4
 21713 000005  B5    OCT 5
 21714 000006  B6    OCT 6
 21715 000007  B7    OCT 7
 21716 000011  B11   OCT 11
 21717 000017  B17   OCT 17
 21720 000020  B20   OCT 20
 21721 000024  B24   OCT 24
 21722 000037  .B37  OCT 37
 21723 000040  B40   OCT 40
```

```
21724 000077 B77    OCT 77
21725 100077 SCM    OCT 100077
21726 077000 IDM    OCT 077000       ID ONLY NO SC OR REV.
21727 000100 B100   OCT 100
21730 000200 B200   OCT 200
21731 100300 B100300  OCT 100300
21732 100340 B100340  OCT 100340
21733 170360 B170360  OCT 170360
21734 000377 B377   OCT 377
21735 001000 B1000 OCT 1000
21736 001400 B1400 OCT 1400
21737 003004 B3004 OCT 3004
21740 006412 B6412 OCT 6412
21741 007777 B7777 OCT 7777
21742 076000 B76K   OCT 76000
21743 100000 B100K OCT 100000
21744 077777 B77777 OCT 77777
21745 100024 B100024 OCT 100024   DS SELECT CODE & SELF TEST ENABLE
21746 100000 B100000 OCT 100000   CS OFF BIT
21747 177700 B177700 OCT 177700
21750 177777 B177777 OCT 177777
21751 177777 M1     OCT -1
21752 177776 .N2    OCT -2
21753 177760 .N20   OCT -20
21754 177740 .N40   OCT -40
21755 000200 BIT7   OCT 200
21756 102700 NOVCP OCT 102700     NO VCP ERROR CODE
21757 021760 DALTO DEF ALTO
21760 052525 ALTO   OCT 052525
21761 125252 ALT1   OCT 125252
21762 104447 SRGP1 OCT 104447     1000100100100111
21763 114040 SRGP2 OCT 114040     1001100000100000
21764 000100 SRGP3 OCT 000100     0000000001000000
21765 076310 AEAUS OCT 076310
21766 021765 BLBT   DEF AEAUS     DEF FOR LBT TEST
21767 130272 BEAUS OCT 130272
21770 107714 ASR.0 OCT 107714
21771 041300 ASR.1 OCT 041300
21772 143746 MU2    OCT 143746
21773 123746 DV4    OCT 123746
21774 126760 RESUA OCT 126760
21775 006606 RESUB OCT 006606
21776 022114 ..ENT DEF ENTRY
*
      021777 EOPO   EQU *         END OF PAGE 0
*
```

```
01451*
01452*      ENTRY HERE ON POWERUP AFTER MICROCODED SELF TEST & PRETEST
01453*
01454*      USER ROM SHOULD ENTER HERE FOR VCP USER INTERFACE
01455*      DISPLAY HAS SELF TEST ERROR CODE
01456*
01457  22000                ORG EPROM+2000B
```

```
*
*     ENTRY HERE ON POWERUP AFTER MICROCODE SELF TEST & PRETEST
*
            022000  P1     EQU *
      22000 104600  VFP    .JLB CI.IZ      SET GLOBAL REGISTER
      22001 024411
      22002 104600         .JLB .ENQAK     DO ENQ ACK OR SEND BUFFER
      22003 024270
      22004 000244         LDA DISPLAY   GET SELF TEST ERROR CODE
      22005 002003         SZA,RSS
      22006 022037         JMP VFP.0     NO ERRORS IN SELF TEST
*
      22007 023766         LDA SELFERR   OUTPUT ERROR MESSAGE
      22010 104600         .JLB PUTS
      22011 024245
      22012 000244         LDA DISPLAY
      22013 023654         AND ..B377    LOW BYTE
      22014 104600         .JLB OUTN     OUTPUT ERROR CODE
      22015 024344
      22016 000244         LDA DISPLAY
      22017 001727         ALF,ALF
      22020 023654         AND ..B377
      22021 104600         .JLB OUTN       OUTPUT HIGH BYTE OF ERROR CODE
      22022 024344
*
*     CHECK FOR LOADER ERRORS
*
      22023 000265         LDA LERR
      22024 002003         SZA,RSS
      22025 022037         JMP VFP.0     NO LOADER ERRORS
*
      22026 023746         LDA CRLF      OUTPUT CRLF
      22027 104600         .JLB PUTS
      22030 024245
      22031 023614         LDA .LDER     OUTPUT LOADER ERROR MESSAGE
      22032 104600         .JLB PUTS
      22033 024245
      22034 000265         LDA LERR
      22035 104600         .JLB OUTD     OUTPUT ERROR NUMBER
      22036 024312
*
      22037 000302  VFP.0  LDA PEADD     ANY SOFT ERRORS???
      22040 002020         SSA
      22041 022057         JMP VFP.1     NO, GO TO FRONT PANEL
```

```
*
22042 023767          LDA SOFTERR   GET SOFT ERROR MESSAGE
22043 104600          .JLB PUTS     OUTPUT IT
22044 024245
22045 000303          LDA PEMAP
22046 000302          LDB PEADD
22047 005200          RBL           GET PAGE NUMBER OF PARITY ERROR
22050 100105          RRL 5
22051 104600          .JLB OUTN     OUTPUT BLOCK NUMBER
22052 024344
22053 000302          LDA PEADD
22054 023655          AND ..B1777   GET OFFSET IN PAGE
22055 104600          .JLB OUTN     OUTPUT ADDRESS IN BLOCK
22056 024344
*
22057 000304   VFP.1  LDA VCPTFLG   IS TEST??
22060 002020          SSA
22061 022176          JMP ENT2      GET NEXT COMAND
*
22062 023747          LDA VERMG     OUTPUT VERSION
22063 104600          .JLB PUTS     MESSAGE
22064 024245
*
22065 000246          LDA MSIZE
22066 001722          ALF,RAL       MULTIPLY BY 32
22067 001200          RAL           MULTIPLY BY 2
22070 104600          .JLB OUTD     OUTPUT THE MEMORY SIZE
22071 024312
22072 023763          LDA KMES
22073 104600          .JLB PUTS     OUTPUT "K MEMORY IN SYSTEM"
22074 024245
22075 000247          LDA ECCCNT    GET AMOUNT OF ECC
22076 001722          ALF,RAL
22077 001200          RAL           MULTIPLY BY 64
22100 104600          .JLB OUTD
22101 024312
22102 023764          LDA ECMES
22103 104600          .JLB PUTS
22104 024245
22105 104600          .JLB .ENQAK   MAKE SURE TERMINAL READY, OUTPUT
22106 024270                           BUFFER
22107 022176          JMP ENT2      GET FIRST COMMAND
*
22110 021660   PE1    DEF PEINT
22111 000230   PEJSB  JSB PERTN
*
```

VIRTUAL CONTROL PANEL PAGE 1

```
*
*      BREAK COMES HERE !!!!!!
*      SO DO HALT INSTRUCTIONS
*
*
22112 024137  .RENT DEF REENT
22113 022114  .ENT  DEF *+1
22114 103105  ENTRY CLF 5          SET PARITY TO "ODD"
22115 103200        OCT 103200     SFC 0,C
22116 000200        ISZ SAVEI      SET INTERRUPTS ON FLAG
22117 000507        ISZ FIRST
22120 002001        RSS            CHECK NOT FIRST TIME FLAG
22121 022172        JMP AGAIN      BREAK WAS DURING VCP SO DONT CHANGE
                                      REGISTERS
22122 104400        DST SAVEA+2000B  SAVE "A" REGISTER & B REGISTER
22123 002204
22124               CCQA             GET Q
22125 000211        STA SAVEQ
22126               CZA              GET Z
22127 000212        STA SAVEZ        SAVE IT
22130 002400        CLA
22131 102201        SOC              IS "O" CLEAR ?
22132 002004        INA              NO, INCREMENT "A"
22133 000201        STA SAVEO        SAVE "O" REPLICA
22134 001522        ERA,RAL          "E" INTO LSB OF "A"
22135 000202        STA SAVEE        SAVE IT
22136 102502        LIA GR           GET CURRENT VALUE
22137 102202        SFC GR           IS GLOBAL REGISTER ON ?
22140 023721        IOR BIT15        YES, SET MSB
22141 000206        STA SAVEG        SAVE FOR EXIT
22142 105743        STX SAVEX        SAVE X AND Y REGISTERS
22143 000207
22144 105753        STY SAVEY
22145 000210
22146 000100        LDA WMAP
22147 000214        STA SAVEW        SAVE WMAP VALUE
22150 023720        AND B37
22151               LWD1             SET DATA 1 MAP TO OLD XQT MAP
22152 000000        DEF 0
22153 102503        LIA 3            FETCH "P" VALUE
22154 001665        ELA,CLE,ERA      NO SIGN BIT ON P REGISTER
22155 000203        STA SAVEP        SAVE IT
22156 023724        ADA N1           IF NO, DECREMENT "P"
22157 000213        STA SAVEM        SAVE "M" VALUE
22160               XLB1 '@A'        GET INSTRUCTION WHICH GOT US HERE
22162 023644        CPB  .ENTI       IS BOOTEX CALL BACK?
22163 022112        JMP  .RENT,I     YES, GO DO REQUIRED OPERATION
```

```
*
22164 102501         LIA CPUST     IS BREAK DISABLED?
22165 001727         ALF,ALF
22166 023717         AND .B10      ISOLATE BREAK SWITCH
22167 002002         SZA           IF ITS A ONE, BREAK DISABLED
22170 023530         JMP EXEX2     RESTART IMMEDIATELY IF DISABLED
*
22171 022176         JMP ENT2
*
*
22172 000510   AGAIN ISZ NDCLR     DO WE HAVE TO PRESET??
22173 022176         JMP ENT2      NO WE DONT
22174 105762         JLY .PSET     PRESET
22175 021633
*
22176 003400   ENT2  CCA
22177 000507         STA FIRST
22200 000302         STA PEADD     NO PARITY ERROR
22201 022111         LDA PEJSB     PUT JSB IN TRAP CELL
22202 000005         STA 5
22203 022110         LDA PE1
22204 000232         STA PE        SET PARITY TRAP CELL FOR PE INTS
22205 023745         LDA .RTRN
22206 000526         STA XEQT+2    SET RETURN POINT FOR I/O INSTRUC-
                                     TION SUBROUTINE
*
22207 104600         .JLB CI.IZ    SET GLOBAL REGISTER
22210 024411
*
22211 102702         STC 2         ENABLE BREAK
*
*     OUTPUT THE REGISTERS  ( P, A, B, RW, M, & T )
*
22212 002400         CLA           INITIALIZE NUMBER
22213 000243         STA PEFLAG
22214 000510         STA NDCLR     DONT NEED TO CLEAR IF A BREAK HERE
22215 000363         STA DFLAG     OF DIGITS FLAG
22216 023771         LDA PMESS     OUTPUT A 'P' AND
22217 104600         .JLB PUTS
22220 024245
22221 000203         LDA SAVEP      THE CURRENT P VALUE
22222 104600         .JLB OUTN
22223 024344
```

```
*
22224 023772        LDA AMESS     OUTPUT AN 'A' AND
22225 104600        .JLB PUTS
22226 024245
22227 000204        LDA SAVEA      THE CURRENT A VALUE
22230 104600        .JLB OUTN
22231 024344
*
22232 023773        LDA BMESS     SAME LIKE BEFORE
22233 104600        .JLB PUTS
22234 024245
22235 000205        LDA SAVEB       ONLY THE NAMES HAVE CHANGED
22236 104600        .JLB OUTN
22237 024344
22240 023753        LDA SPC2
22241 104600        .JLB PUTS     OUTPUT TWO SPACES
22242 024245
22243 023702        LDA .R
22244 104600        .JLB PUTCH
22245 024560
22246 023707        LDA .W
22247 104600        .JLB PUTCH
22250 024560
22251 000214        LDA SAVEW     OUTPUT WMAP VALUE
22252 104600        .JLB OUTN
22253 024344
22254 022431        JMP .T02       EARLY EXIT FROM .TREG
*
22255 104600  NEXT  .JLB CI.IZ    ENABLE VCP
22256 024411
*
*
*     HERE IS MAIN COMMAND INTERPRETATION LOOP
*
*
22257 023740  COMND LDA D7          SAY IN FRONT PANEL TO LIGHTS
22260 102601        OTA CPUST
22261 000243        LDA PEFLAG    WAS PARITY ERROR IN LAST COMMAND??
22262 002003        SZA,RSS
22263 022271        JMP COMN1     NO, GO ON
*
22264 023765        LDA PEMES
22265 104600        .JLB PUTS     SAY PARITY ERROR
22266 024245
22267 002400        CLA
22270 000243        STA PEFLAG
22271 023750  COMN1 LDA PRMPT     OUTPUT THE PROMPT
22272 104600        .JLB PUTS        CHARACTER   ">"
22273 024245
```

```
*
22274 002400        CLA            CLEAR COMMAND
22275 000503        STA TEMPO       SAVE
*
22276 104600  COM1  .JLB TG.BF     INITIALIZE TO XMITT & GET BUFFER
22277 024533
22300 104600        .JLB GETCH     FETCH A CHARACTER
22301 024540
22302 023645        CPA .CR        "CR" ?
22303 022257        JMP COMND       JUST TESTING
22304 023653        CPA .?         AH A PLEA FOR HELP
22305 022416        JMP .HELP       GO DUMP HELP MESSAGE
22306 023704        CPA .T         HOW ABOUT THE "T" REGISTER ?
22307 022422        JMP .TREG       GOOD GUESS
22310 023647        CPA .%         CONTROL SEQUENCE ?
22311 023371        JMP CNTRL       YEP, GO SEE WHICH ONE
22312 023675        CPA .M         IS IT "MEMORY ADDRESS" ?
22313 022512        JMP .MREG
22314 023706        CPA .V         IS IT VIOLATION REGISTER??
22315 023164        JMP .VIO
22316 023702        CPA .R         IS IT A SPECIAL REGISTER ?
22317 022667        JMP .REGS
22320 023674        CPA .L
22321 022551        JMP .LIST      LIST MEMORY
*
22322 023726        LDB N4         INITIALIZE DATA FLAG
22323 023712        CPA .Z
22324 006005        INB,RSS
22325 023701        CPA .Q
22326 006005        INB,RSS
22327 023711        CPA .Y         IS IT "Y REGISTER" ?
22330 006005        INB,RSS        YES, BUMP DATA FLAG
22331 023710        CPA .X
22332 006005        INB,RSS
22333 023672        CPA .G
22334 006005        INB,RSS
22335 023665        CPA .B
22336 006005        INB,RSS
22337 023663        CPA .A
22340 006005        INB,RSS
22341 023700        CPA .P
22342 006005        INB,RSS
22343 023670        CPA .E
22344 006005        INB,RSS
22345 023677        CPA .O
22346 006005        INB,RSS
22347 023673        CPA .I
22350 006005        INB,RSS
```

```
22351 022412          JMP CERR      TRY AGAIN
22352 000367          STA PAGE      SAVE CHAR

22353 000363          STB DFLAG     SET TYPE FLAG (< 0 => SINGLE DIGIT)
22354 023742          LDA BUFF      BUILD ADDRESS OF
22355 000363          ADA DFLAG      DESIRED REGISTER
22356 000361          STA DPNTR     SAVE IT FOR LATER
22357 000000          LDA A,I       FETCH CURRENT VALUE
22360 104600          .JLB OUTN        PRINT IT
22361 024344
22362 104600          .JLB TG.BF    OUTPUT BUFFER AND GET INPUT
22363 024533
22364 104600          .JLB GETN        NEW VALUE
22365 024647
22366 023211          JMP COM01      NO NEW DATA TRY AGAIN
22367 006002          SZB            TERMINATION ON "CR" ?
22370 022412          JMP CERR       NO, TELL 'EM ABOUT IT
22371 000363          LDB DFLAG      WAS THIS THE "P"
22372 006003          SZB,RSS         REGISTER  ( IF DFLAG = 0 )
22373 001665          ELA,CLE,ERA      IF YES THEN FORCE MSB TO 0
22374 000361          STA DPNTR,I    YES, UPDATE REGISTER DATA
22375 023746          LDA CRLF
22376 104600          .JLB PUTS
22377 024245
22400 023754          LDA SPC3
22401 104600          .JLB PUTS
22402 024245
22403 000367          LDA PAGE       OUTPUT CHARACTER
22404 104600          .JLB PUTCH
22405 024560
22406 000361          LDA DPNTR,I
22407 023050          JMP .OUTIT      GO SEE WHAT'S NEXT


22410 104600    CERR2 .JLB CI.IZ      RESTORE INTERFACE
22411 024411
22412 023752    CERR  LDA ERMES        BEEP
22413 104600          .JLB PUTS
22414 024245
22415 022257          JMP COMND      ONE MO' TIME

```

```
*
*     OUTPUT THE HELP MESSAGE
*
*
 22416 023751  .HELP LDA HELP      OUTPUT THE HELP
 22417 104600        .JLB PUTS        MESSAGE
 22420 024245
 22421 022257        JMP COMND     TRY AGAIN
*
*
*     TOGGLE BASE BETWEEN HEX AND OCTAL
*
*
*
*     ROUTINE TO HANDLE "T" REGISTER ACCESSES
*
*
 22422 000363  .TREG STA DFLAG     SET DFLAG FOR MULTIPLE DIGITS
                                      ( DFLAG > 0 )
 22423 023746  .T00  LDA CRLF      OUTPUT CR
 22424 104600        .JLB PUTS
 22425 024245
 22426 023753        LDA SPC2      SPACE SPACE
 22427 104600        .JLB PUTS
 22430 024245
 22431 023755  .T02  LDA MMESS     OUTPUT "M"
 22432 104600        .JLB PUTS     AND THE  CURRENT
 22433 024245
 22434 000213        LDA SAVEM        "M" REGISTER
 22435 104600        .JLB OUTN         CONTENTS
 22436 024344
 22437 023756        LDA TMESS     NOW OUTPUT "T" OR "t" DEPENDING
 22440 104600        .JLB PUTS
 22441 024245
 22442               XLA1 '@SAVEM'      GET MAIN MEMORY DATA
 22444 104600        .JLB OUTN    OTPUT THE VALUE
 22445 024344
 22446 000363        LDB DFLAG     WAS THIS PART OF ( P,A,B,M,& T ) ?
 22447 006003        SZB,RSS         IF DFLAG NO. 0 THEN GET INPUT
 22450 022257        JMP COMND        ELSE BAIL OUT
 22451 104600        .JLB TG.BF
 22452 024533
 22453 104600        .JLB GETN    GET NEW DATA, MAYBE
 22454 024647
 22455 022474        JMP .T?       NO NEW DATA, CHECK FOR "N" OR "P"
 22456 006003        SZB,RSS       CR?
 22457 022465        JMP .T03
 22460 023667        CPB .D
```

```
22461 022465        JMP .T03
22462 023676        CPB .N
22463 022465        JMP .T03
22464 022412        JMP CERR       BAD INPUT AFTER VALUE
22465         .T03  XSA1 '@SAVEM'    STORE INTO MAIN MEMORY
*
22467 006002        SZB            WAS IT CR
22470 022474        JMP .T?        NO, SEE WHAT ELSE IT COULD BE
*
22471 002400        CLA
22472 000363        STA DFLAG      INDICATE ECHOING
22473 022423        JMP .T00       ECHO NEW RESULT
*
22474 023645  .T?  CPB .CR         "CR" ?
22475 022257        JMP COMND       YES, EXIT
22476 000213        LDA SAVEM      FETCH "M"
22477 002004        INA            INCREMENT, JUST IN CASE
22500 023676        CPB .N         WAS IS "NEXT" ?
22501 022506        JMP PREV+1     NOT BAD, MUST HAVE BEEN LUCK
22502 023667        CPB .D         WAS IT "DECREMENT" ?
22503 022505        JMP PREV       YES, DECREMENT "M"
22504 022412        JMP CERR       ERROR
*
22505 023725  PREV  ADA N2         DECREMENT "M"
22506 002020        SSA            IS MSB SET ?  NOT VALID FOR "M"
22507 000213        LDA SAVEM      USE OLD VALUE
22510 000213        STA SAVEM      UPDATE "M" SAVE BUFFER
22511 022423        JMP .T00       GO DISPLAY RESULTS
*
*
*
*     ROUTINE TO HANDLE "M" REGISTER STUFF
*
*
22512 000363  .MREG STA DFLAG     MSB = 0 => MULTI DIGIT OUTPUT
22513 000213        LDA SAVEM      AND M
22514 104600        .JLB OUTN         VALUE
22515 024344
*
22516 104600        .JLB TG.BF     TRANSMIT AND GET BUFFER
22517 024533
22520 104600        .JLB GETN     GET NEW VALUE
22521 024647
22522 022546        JMP MT?        NO NEW DATA
22523 006002        SZB            NEW DATA, DID IT END WITH "CR" ?
22524 023704        CPB .T          NO, WAS IT "T" ?
22525 022527        JMP STORM      EITHER WAY GO STORE NEW VALUE
22526 022412        JMP CERR       ERROR, GO BEEP AT THE TURKEY
*
```

```
22527 001665  STORM ELA,CLE,ERA   FORCE MSB TO 0
22530 000213        STA SAVEM     SAVE WHAT'S LEFT
22531 006002        SZB              CR IS OK RESULT
22532 022546        JMP MT?
22533 023746        LDA CRLF
22534 104600        .JLB PUTS
22535 024245
22536 023753        LDA SPC2
22537 104600        .JLB PUTS
22540 024245
22541 023755        LDA MMESS
22542 104600        .JLB PUTS
22543 024245
22544 000213        LDA SAVEM     ECHO THE NEW VALUE
22545 023050        JMP .OUTIT

22546 023704  MT?   CPB .T        WAS IT "T" ?
22547 022423        JMP .T00       YES, GO TO "T REGISTER" DISPLAY
22550 023211        JMP COM01
*
*
*

*
*
*     ROUTINE TO LIST MEMORY CONTENTS
*
22551 000363  .LIST STA DFLAG     MORE THAN ONE DIGIT
22552 104600        .JLB GETN     GET NUMBER TO LIST
22553 024647
22554 002404        CLA,INA       NO NUMBER, ONE LINE
22555 003004        CMA,INA
22556 000224        STA MCNTR     SAVE IN LINE COUNT
22557 006002        SZB
22560 023645        CPB .CR       ENDED WITH CR?
22561 002001        RSS
22562 022412        JMP CERR      ERROR, NO CR AT END
22563 023746        LDA CRLF
22564 104600        .JLB PUTS     OUTPUT CRLF
22565 024245
22566 023755        LDA MMESS
22567 104600        .JLB PUTS     OUTPUT M
22570 024245
22571 000213        LDA SAVEM
22572 000254        STA MPTR
22573 104600        .JLB OUTN     OUTPUT M VALUE
22574 024344
22575 023761        LDA MPMES
```

```
22576 104600         .JLB PUTS     SAY MAP
22577 024245
22600 000214         LDA SAVEW
22601 023720         AND B37
22602 104600         .JLB OUTN     OUTPUT MAP NUMBER
22603 024344
22604 023746         LDA CRLF
22605 104600         .JLB PUTS     OUTPUT CR AND LF
22606 024245
22607 023727   .LLP  LDA N8
22610 000225         STA PCNTR
22611 000254         LDA MPTR
22612 000367         STA PAGE      REMEMBER START OF LINE FOR CHAR
                                        OUTPUT
22613          .LLP2 XLA1 '@MPTR'  GET DATA
22615 104600         .JLB OUTN     OUTPUT IT
22616 024344
22617 000254         LDA MPTR      NEXT MEMORY LOCATION
22620 002004         INA
22621 001665         ELA,CLE,ERA   CLEAR SIGN BIT
22622 000254         STA MPTR      SAVE IT
22623 000225         ISZ PCNTR
22624 022613         JMP .LLP2
22625 023727         LDA N8
22626 000251         STA CNTR
22627          .LCLP XLA1 '@PAGE'  GET A WORD
22631 001727         ALF,ALF
22632 104600         .JLB .LCH1    OUTPUT A CHAR
22633 022654
22634                XLA1 '@PAGE'
22636 104600         .JLB .LCH1    OUTPUT SECOND CHAR
22637 022654
22640 000367         ISZ PAGE      NEXT WORD
22641 000251         ISZ CNTR
22642 022627         JMP .LCLP
*
22643 023746         LDA CRLF
22644 104600         .JLB PUTS     OUTPUT CRLF AT END OF LINE
22645 024245
22646 000224         ISZ MCNTR     DONE?
22647 002001         RSS
22650 022257         JMP COMND     YES, GET NEXT COMMAND
22651 104600         .JLB .ENQAK   DO ENQACK HANDSHAKE
22652 024270
22653 022607         JMP .LLP
```

```
*
22654 000535  .LCH1 STB RLCH1     SAVE RETURN ADDRESS
22655 023664        AND .DEL        ONLY LOW BYTE
22656 023664        CPA .DEL      IS DELETE??
22657 023645        LDA .CR       YES, MAKE SMALLER ILLEGAL CHAR
22660 023735        ADA N32       SUBTRACT 32
22661 002020        SSA           NEGATIVE??
22662 002400        CLA           YES, MAKE SPACE
22663 023741        ADA D32       PUT CHAR BACK
22664 104600        .JLB PUTCH    OUTPUT CHAR
22665 024560
22666 000535        JMP RLCH1,I   RETURN

*
*
*     ROUTINE TO HANDLE THE SPECIAL REGISTER STUFF
*
*
22667 000363  .REGS STA DFLAG     SET FOR MORE THAN ONE DIGIT
*
22670 104600        .JLB GETCH   GET THE NEXT CHARACTER
22671 024540
22672 000221        STA SVCHR     SAVE CHAR FOR ECHO
22673 023737        LDB D2        SET "B" JUST IN CASE
22674 023666        CPA .C        IS IT "CIR" ?
22675 023043        JMP .CIR
22676 023673        CPA .I        HOW ABOUT "INTERRUPT MASK" ?
22677 023144        JMP .MASK
22700 023707        CPA .W        IS IT WMAP REGISTER
22701 023131        JMP .WMP
22702 023664        CPA .DEL      IS DELETE?
22703 022257        JMP COMND
22704 023675        CPA .M        HOW ABOUT MAP REGISTERS
22705 023214        JMP .MAPS
22706 023700        CPA .P        "PARITY ERROR" MAYBE ?
22707 023152        JMP .PAR
22710 023703        CPA .S        "CPU STATUS SWITCHES" ?
22711 023162        JMP .STAT
22712 023651        CPA .2          I/O REG?
22713 022717        JMP IONXT
22714 023652        CPA .3
22715 006005        INB,RSS
22716 022726        JMP GLCHK
22717 005723  IONXT BLF,RBR         MULT BY 8
22720 000263        STB IORGN
22721 104600        .JLB GETCH      GET NEXT
22722 024540
```

```
22723 023650       XOR ZERO        SAVE LOW BITS
22724 000263       ADA IORGN
22725 000263       STA IORGN       I/O REGISTER NUMBER
22726 000206 GLCHK LDB SAVEG       CHECK GLOBAL REGISTER
22727 107602       OTB 2,C         TURN ON GLOBAL REGISTER
22730 006400       CLB
22731 106502       LIB 2
22732 006003       SZB,RSS
22733 022410       JMP CERR2    ERROR IF NO I/O AT THAT SELECT CODE
22734 000221       LDA SVCHR       GET FIRST CHAR BACK AGAIN
22735 023667       CPA .D
22736 023102       JMP .DIAG
22737 023671       CPA .F
22740 023053       JMP .FLAGS
22741 023651       CPA .2        "I/O"  20 THRU 27 ?
22742 022746       JMP IOREG
22743 023652       CPA .3        "I/O"  30 THRU 32 ?
22744 002001       RSS
22745 022410       JMP CERR2     YOU BLEW IT
*
22746 000263 IOREG LDA IORGN       AND SAVE THE RESULT
22747 023734       ADA N27       WAS IT GREATER
22750 002021       SSA,RSS        THAN 33B ?
22751 022410       JMP CERR2       YES, TOO BEEG
22752 000263       LDA IORGN     CLEAN COPY
22753 023733       ADA N24       WAS IT LESS
22754 002021       SSA,RSS        THAN 30B ?
22755 022766       JMP REGOK       NO => 30, 31, OR 32
22756 000263       LDA IORGN     FRESH COPY
22757 023732       ADA N23       WAS IT GREATER
22760 002021       SSA,RSS        THAN 26B ?
22761 022410       JMP CERR2     YOU DUMMY THERE AIN'T NO 27 !
22762 000263       LDA IORGN     ONCE MORE
22763 023731       ADA N16       IS IT LESS THAN
22764 002020       SSA            20B ?
22765 022410       JMP CERR2     NOW IT'S TOO SMALL
*
22766 104600 REGOK .JLB GETREG   GET REGISTER VALUE
22767 023027
22770 104600       .JLB TG.BF    TRANSMIT AND GET NEW BUFFER
22771 024533
22772 104600       .JLB GETN     GET NEW VALUE
22773 024647
22774 023211       JMP COM01     NO NEW VALUE
22775 006002       SZB
22776 022412       JMP CERR
22777 000525       LDB XEQT+1    NOW MAKE
23000 023722       ADB .B100      IT AN
```

```
23001 000525        STB XEQT+1       "OTA"
23002 000206        LDB SAVEG      SET THE GLOBAL REGISTER
23003 107602        OTB GR,C        TO THE DESIRED VICTIM
23004 000524        JSB XEQT       TRY IT OUT
23005 104600        .JLB CI.IZ       PUT GLOBAL REGISTER BACK
23006 024411
23007 023770        LDA RMESS
23010 104600        .JLB PUTS      ECHO R
23011 024245
23012 000221        LDA SVCHR        GET REGISTER NUMBER BACK
23013 104600        .JLB PUTCH     OUTPUT IT
23014 024560
23015 000525        LDA XEQT+1
23016 023740        AND D7         GET SECOND CHAR
23017 023650        ADA ZERO       MAKE ASCII
23020 104600        .JLB PUTCH
23021 024560
23022 000206        LDA SAVEG
23023 103602        OTA GR,C         ENABLE GLOBAL REGISTER
23024 104600        .JLB GETREG      GET NEW VALUE AND OUTPUT IT
23025 023027
23026 022257        JMP COMND      SEE WHAT'S NEXT
*
23027 000543  GETREG STB RGETREG
23030 023744        LDA .LIA       BUILD THE
23031 000263        IOR IORGN       APPROPRIATE
23032 000525        STA XEQT+1      "LIA" INSTRUCTION
23033 000524        JSB XEQT       GO DO IT !
23034 000503        STA TEMPO      SAVE RESULT
23035 104600        .JLB CI.IZ     PUT THE GLOBAL REGISTER BACK
23036 024411
23037 000503        LDA TEMPO      RESTORE RSULT
23040 104600        .JLB OUTN      OUTPUT THE VALUE
23041 024344
23042 000543        JMP RGETREG,I
*
*
23043 102504  .CIR  LIA 4          GET CURRENT CIR
23044 104600        .JLB COMN     OUTPUT IT AND GET NEW VALUE
23045 023166
23046 102604        OTA 4          UPDATE THE CIR
23047 102504        LIA 4
23050 104600  .OUTIT .JLB OUTN      ECHO NEW VALUE
23051 024344
23052 022257        JMP COMND      SPLIT
*
```

```
*
23053 002400  .FLAGS CLA
23054 102220         SFC 20B
23055 002004         INA
23056 001723         ALF,RAR
23057 102221         SFC 21B
23060 002004         INA
23061 001723         ALF,RAR
23062 102222         SFC 22B
23063 002004         INA
23064 001723         ALF,RAR
23065 102223         SFC 23B
23066 002004         INA
23067 001723         ALF,RAR
23070 102224         SFC 24B
23071 002004         INA
23072 001723         ALF,RAR
23073 102230         SFC 30B
23074 002004         INA
23075 000262         STA RFTMP
23076 104600         .JLB CI.IZ
23077 024411
23100 000262         LDA RFTMP
23101 023050         JMP .OUTIT
*
23102 002404  .DIAG CLA,INA
23103 102602         OTA GR
23104 000206         LDA SAVEG
23105 023654         AND ..B377     GET GLOBAL REGIUSTER
23106 023744         IOR .LIA       MAKE LIA INSTRUCTION
23107 000525         STA XEQT+1
23110 000524         JSB XEQT
23111 000503         STA TEMPO
23112 023737         LDA D2
23113 102602         OTA GR       ESTABLISH DIAGNOSE MODE 2
23114 000206         LDA SAVEG
23115 023654         AND ..B377
23116 023744         IOR .LIA
23117 000525         STA XEQT+1
23120 000524         JSB XEQT
23121 000502         STA TEMP1
23122 104600         .JLB CI.IZ   PUT GLOBAL REGISTER BACK
23123 024411
23124 000503         LDA TEMPO
23125 104600         .JLB OUTN
23126 024344
23127 000502         LDA TEMP1
23130 023050         JMP .OUTIT   GET NEXT COMMAND
```

```
*
*
*
23131 000214  .WMP  LDA SAVEW
23132 104600        .JLB COMN    KOUTPUT THE WMAP VALUE
23133 023166
23134 002001        RSS
23135 022257        JMP COMND     NO NEW VALUE
*
23136 000214        STA SAVEW
23137 023720        AND B37
23140               LWD1
23141 000000        DEF 0
23142 000214        LDA SAVEW       ECHO NEW VALUE
23143 023050        JMP .OUTIT
*
*
*
23144 102500  .MASK LIA 0         FETCH INTERRUPT MASK
23145 104600        .JLB COMN       SAME OLE'
23146 023166
23147 102600        OTA 0         NEW INTERRUPT MASK VALUE
23150 102500        LIA 0
23151 023050        JMP .OUTIT
*
*
23152 102505  .PAR  LIA 5         CURRENT PARITY REGISTER
23153 107505        LIB 5,C
23154 101032        ASR 10
23155 104600        .JLB OUTN
23156 024344
23157 102505        LIA 5
23160 023655        AND ..B1777
23161 023050        JMP .OUTIT
*
*
23162 102501  .STAT LIA 1         FETCH THE SWITCHES
23163 023050        JMP .OUTIT
*
*
23164 103507  .VIO  LIA 7,C       GET THE CURRENT VALUE
23165 023050        JMP .OUTIT
*
*
23166 000547  COMN  STB RCOMN     SAVE RETURN ADDRESS
23167 104600        .JLB OUTN    OUTPUT THE CONTENTS OF "A"
23170 024344
23171 104600        .JLB TG.BF
23172 024533
```

```
23173 104600        .JLB GETN     TRY FOR SOME NEW DATA
23174 024647
23175 023211        JMP COM01     NO SUCH LUCK ( NO NEW DATA )
23176 006002        SZB           DATA, BUT WAS THERE A CR ?
23177 022412        JMP CERR      NO, SORRY CHARLIE
23200 000222        STA SACOMN    SAVE A REGISTER
23201 023770        LDA RMESS     START THE ECHO
23202 104600        .JLB PUTS
23203 024245
23204 000221        LDA SVCHR
23205 104600        .JLB PUTCH    OUTPUT THE REGISTER NAME
23206 024560
23207 000222        LDA SACOMN    GET THE VALUE BACK AGAIN
23210 000547        JMP RCOMN,I   YES, WE DONE SOMETHING RIGHT
*
23211 023645  COM01 CPB .CR       NO DATA, BUT WAS IT A CR ?
23212 022257        JMP COMND     YES, GOOD EXIT
23213 022412        JMP CERR      NO, NOT SO GOOD EXIT

*
*
*     PROCESS REGISTER M (MAPS) COMMANDS
*
*
23214 104600  .MAPS .JLB GETN     GET THE MAP NUMBER
23215 024647
23216 022412        JMP CERR      NO NUMBER, ERROR
*
23217 002020        SSA           IS MAP NUMBER NEGATIVE?
23220 022412        JMP CERR      YES, ERROR
*
23221 000260        STB TEMP      SAVE B
23222 023735        LDB N32       MAP NUMBER MUST BE LESS THAN 32
23223 000000        ADB A         SUBTRACT 32 FROM MAP NUMBER
23224 006021        SSB,RSS       RESULT NEGATIVE?
23225 022412        JMP CERR      NO, ERROR SINCE MAP NUMBER > 31
*
23226 000366        STA MAP       SAVE MAP NUMBER (0-31)
23227 000260        LDB TEMP
23230 006003        SZB,RSS       TERMINATED WITH CR?
23231 023235        JMP MAP01     YES, GO OUTPUT A MAP
*
23232 023700        CPB .P        TERMINATED WITH P?
23233 023264        JMP MAPPG     YES, GO FIND OUT WHAT PAGE HE WANTS
23234 022412        JMP CERR      OTHER TERMINATIONS ARE ERRORS
*
```

```
*
23235        MAP01 SMAP           XSM READ MAP (A) INTO MEMORY (B)
23236 000000       DEF 0
23237 000370 MBUF  DEF MPBUF
23240 023726       LDA N4
23241 000225       STA PCNTR       4 LINES OF OUTPUT
23242 023237       LDA MBUF        GET ADDRESS OF MAP
23243 000254       STA MPTR       SAVE POINTER TO IT
23244 023727 MAP15 LDA N8          8 NUMBERS PER LINE
23245 000224       STA MCNTR
23246 023746       LDA CRLF
23247 104600       .JLB PUTS        OUTPUT CR LF
23250 024245
23251 000254 MAP02 LDA MPTR,I     GET A MAP CONTENTS
23252 104600       .JLB OUTN        OUTPUT IT
23253 024344
23254 000254       ISZ MPTR       POINT TO NEXT MAP REGISTER
23255 000224       ISZ MCNTR       DONE WITH LINE?
23256 023251       JMP MAP02       NO, GO DO ANOTHER REGISTER
*
23257 104600       .JLB .ENQAK      TERMINAL READY??
23260 024270
23261 000225       ISZ PCNTR       DONE 4 LINES YET?
23262 023244       JMP MAP15       NO, OUTPUT MORE REGISTERS
*
23263 022257       JMP COMND       DONE, GO GET NEXT COMMAND
*
*
23264 104600 MAPPG .JLB GETN        INPUT PAGE NUMBER
23265 024647
23266 022412       JMP CERR        NO NUMBER, ERROR
23267 023347       JMP MAPP2
*
23270 002020 MAPP1 SSA             IS NUMBER NEGATIVE?
23271 022412       JMP CERR        YES, ERROR
*
23272 023735       ADA N32
23273 002021       SSA,RSS         IS NUMER >= 32?
23274 022412       JMP CERR        YES, ERROR
*
23275 000366       LDA MAP         GET MAP INTO MEMORY
23276              SMAP            XSM READ MAP (A) INTO MEMORY (B)
23277 000000       DEF 0
23300 000370       DEF MPBUF
23301 023237       LDB MBUF        GET BUFFER ADDRESS
23302 000367       ADB PAGE        ADD TO POINT AT PAGE NEEDED
23303 000254       STB MPTR        SAVE PAGE ADDRESS
23304 000001       LDA B,I         GET PAGE
```

```
23305 104600         .JLB OUTN       OUTPUT VALUE AND GET NEW VALUE
23306 024344
23307 104600         .JLB TG.BF    TRANSMIT AND GET RESULTS
23310 024533
23311 104600         .JLB GETN       GET NEW VALUE
23312 024647
23313 023334         JMP NXPG    NO NEW VALUE, SEE IF HE WANTS
                                   ANOTHER PAGE
*
23314 000260         STB TEMP        SAVE LETTER INPUT
23315 006003         SZB,RSS     ERROR IF T INPUT SO DONT UPDATE MAP
23316 023324         JMP NXPG1       CR ENTERED AT END
23317 023676         CPB .N
23320 023324         JMP NXPG1     ONLY CR, N, OR D ARE LEGAL HERE
23321 023667         CPB .D
23322 002001         RSS
23323 022412         JMP CERR      ERROR SINCE BAD CHAR INPUTQ
*
23324 000254   NXPG1 STA MPTR,I      PUT NEW PAGE VALUE IN BUFFER
23325 000366         LDA MAP
23326                LMAP            XLM STORE MAP (A) FROM MEMORY (B)
23327 000000         DEF 0
23330 000370         DEF MPBUF
23331 000260         LDB TEMP        GET LETTER BACK
23332 006003         SZB,RSS         WAS CR?
23333 022257         JMP COMND       YES,DONE
*
23334 023645   NXPG CPB .CR
23335 022257         JMP COMND
23336 000367         LDA PAGE        GET CURRENT PAGE NUMBER
23337 023676         CPB .N          IS NEXT?
23340 023346         JMP NXPG2       YES, NEXT PAGE
23341 023667         CPB .D          IS PREVIOUS?
23342 002001         RSS
23343 022412         JMP CERR
23344 023724         ADA N1          YES, SUBTRACT 1
23345 002001         RSS
23346 002004   NXPG2 INA
23347 000367   MAPP2 STA PAGE        SAVE NEW PAGE NUMBER
23350 023746         LDA CRLF        ON TO NEXT LINE
23351 104600         .JLB PUTS
23352 024245
23353 023761         LDA MPMES
23354 104600         .JLB PUTS        OUTPUT MAP
23355 024245
23356 000366         LDA MAP
23357 104600         .JLB OUTN        OUTPUT MAP NUMBER
23360 024344
```

```
23361 023762        LDA PGMES
23362 104600        .JLB PUTS       OUTPUT "PAGE"
23363 024245
23364 000367        LDA PAGE
23365 104600        .JLB OUTN       OUTPUT NEW PAGE NUMBER
23366 024344
23367 000367        LDA PAGE        PAGE FOR MAPP1
23370 023270        JMP MAPP1       GO OUTPUT PAGE AND GET NEW VALUE
*

*
*
*     PROCESS "%" COMMANDS
*
*
23371 104600  CNTRL .JLB GETS    GET REST OF STRING
23372 024766
23373 023746        LDA CRLF
23374 104600        .JLB PUTS    OUTPUT CRLF
23375 024245
23376 023643        LDA SPTR,I   GET FIRST CHAR
23377 023654        AND ..B377
23400 000503        STA TEMPO
23401 023705        CPA .U       USER
23402 023434        JMP .USER,I
23403 023674        CPA .L       LOAD SOMETHING ?
23404 023553        JMP .LOAD     GO SEE WHAT IT IS
23405 023707        CPA .W       WRITE SOMETHING
23406 023553        JMP .LOAD     SORT IT OUT LATER
23407 023665        CPA .B       BOOT MAYBE ?
23410 023553        JMP .LOAD     LOAD 'EM AND RUN
23411 023643        LDA SPTR
23412 002004        INA
23413 000000        LDA A,I      GET SECOND WORD
23414 001727        ALF,ALF
23415 023654        AND ..B377   MASK OFF NEXT CHAR
23416 002002        SZA          MUST BE ZERO ( NO NEXT CHAR FOR
                                    FOLLOWING COMMANDS)
23417 022412        JMP CERR     ERROR SINCE CHARS AFTER COMMAND
23420 000503        LDA TEMPO    GET CHAR BACK AGAIN
23421 023670        CPA .E       EXECUTE?
23422 023507        JMP .EX      GO EXECUTE PROGRAM
23423 023702        CPA .R       RUN?
23424 023515        JMP .RUN     GO RUN FROM CURRENT P
23425 023704        CPA .T       TEST?
23426 023545        JMP .TRAC    GO DO PRETEST
23427 023666        CPA .C       MEMORY CLEAR ?
23430 023445        JMP CLRM      GO ZERO MEMORY
```

```
23431 023700        CPA .P        PRESET ??
23432 023435        JMP PRSET      YES, GO DO A "CLC 0,C"
23433 022412        JMP CERR      NUTHIN'

*
23434 030002  .USER DEF 30002B    JUMP TO USER ROM CODE
*
*
*
*
*
*     PRESET THE MACHINE
*
*
*
23435 105762  PRSET JLY .PSET     BLOW EVERYTHING AWAY
23436 021633
23437 104600        .JLB CI.IZ     FIX UP THE INTERFACE CARD
23440 024411
23441 023760        LDA PRMES
23442 104600        .JLB PUTS     ;*** PRESET ***
23443 024245
23444 023502        JMP FXRX      THAT'S ALL GET NEXT COMMAND
*
*
*     ROUTINE TO CLEAR MEMORY  ( ADDRESS 2 TO 77777 )
*
*
*
23445 023757  CLRM  LDA CLMES
23446 104600        .JLB PUTS        SAY CLEARING MEMORY
23447 024245
23450 002400        CLA
23451 000366        STA MAP       START WITH MAP 0
23452               SMAP          STORE MAP TO MEMORY
23453 000000        DEF 0
23454 000430        DEF MZSV     SAVE MAP ZERO IN MAP ZERO SAVE AREA
23455 002400        CLA
23456               LWD1          USE MAP ZERO FOR CLEAR MEMORY
23457 000000        DEF 0            GET ZERO FROM A REGISTER
*
23460 000366  CLRM1 LDA MAP       GET NEXT MAP TO DO
23461 000246        CPA MSIZE     DONE?
23462 023476        JMP CLDN      YES, NO MORE MAPS
*
23463 105762        JLY STMAP    SET MAP ZERO SEQUENTIALLY
23464 027647
```

```
*
23465 002400        CLA           START ADDRESS ZERO
23466               XSA1 '0'        CLEAR FIRST LOCATION
23470 006404        CLB,INB
23471 105745        LDX ..B77777    COUNT FOR 32K
23472 023656
23473               MW11          CLEAR 32K MEMORY
*
23474 000366        ISZ MAP       ON TO NEXT 32K
23475 023460        JMP CLRM1
*
*
23476 002400  CLDN  CLA
23477               LMAP          RESTORE MAP ZERO AS WAS
23500 000000        DEF 0
23501 000430        DEF MZSV       RESTORE FROM BUFFER
23502 000214  FXRX  LDA SAVEW        RESTORE REGISTER X (WMAP VALUE)
23503 023720        AND B37
23504               LWD1
23505 000000        DEF 0             PUT ALT 1 MAP BACK AS IT WAS
23506 022257        JMP COMND      YES, BACK TO PROMPT
*
*
23507 002400  .EX   CLA
23510 000205        STA SAVEB      FOR %E  B HAS ZERO
23511 003000        CMA
23512 000204        STA SAVEA      A HAS ALL 1S
23513 023737        LDA D2
23514 000203        STA SAVEP     START AT P=2
*
*
23515 003400  .RUN  CCA                SENT ALL 1'S
23516 102624        OTA 24B       TO TELL OS WE'VE BEEN HERE
23517 104600  EXEX  .JLB ENDVCP   TELL CARD TO LEAVE VCP MODE
23520 023533
23521 104600  BEXEX .JLB RSTOR   NOW PUT EVERTHING BACK
23522 024205
23523 102100        STF 0         TURN 'EM BACK ON, IF THEY WERE ON
23524 102702        STC 2         TURN ON BREAK
23525               XJMP 'SAVEW','@SAVEP' ;LAUNCH THE USER WITH HIS
                                             OLD WMAP
*
*                 IF BREAK DISABLED
23530 104600  EXEX2 .JLB CI.IZ    FIX INTERFACE CARD
23531 024411
23532 023515        JMP .RUN      RESTART
*                           SEND END VCP MODE IF INTELLEGENT DRIVER
*
```

```
 23533 000530  ENDVCP STB RENDV   SAVE RETURN ADDRESS
 23534 104600         .JLB CI.ID   IS INTELLEGENT??
 23535 024513
 23536 000530         JMP RENDV,I  NO, DO NOTHING
 23537 023544         LDA VCPEX    YES, GET END VCP COMMAND
 23540 104600         .JLB DS.FT   SEND IT TO CARD AND WAIT FOR FLAG
 23541 024463
 23542 000000         NOP          TIME OUT, DONT WORRY ABOUT IT
 23543 000530         JMP RENDV,I  RETURN
 23544 062000  VCPEX OCT 62000    EXIT VCP COMMAND
*
*     SINGLE STEP ROUTINE
*
*
*.STEP .JLB GETCH   GET ONE CHARACTER
*      CPA .CR       IS IT "CR" ?
*      JMP *+2       YES, GO TO IT
*      JMP CERR      NO, YOU BLEW IT
*      STA TFLAG     SET FLAG NON-ZERO => STEP OR TRACE
*STEP1 .JLB RSTOR   RESTORE THE REGISTERS
*      STF 0         TURN INTERRUPTS BACK ON, IF NEEDED
*      CLC 3         START I/O CHIP SEQUENCE
*      STC 2         ENABLE "BREAK"
*      XJMP SAVEW,@SAVEP ; LAUNCH THE USER WITH HIS OLD WMAP
*
*
*     SELF TEST.  GO DO CLC 0,C AND THEN ON TO START
*
*
 23545 003400  .TRAC CCA
 23546 000304         STA VCPTFLG   FLAG FOR SELFTEST
 23547 105762         JLY .PSET    CLEAR OUT MACHINE TO POWER ON STATE
 23550 021633
 23551 023552         JMP *+1,I     GO TEST
 23552 020004         DEF START+2
*
*
 23553 105762  .LOAD JLY .PSET     RESET I/O FOR LOADERS
 23554 021633
 23555 023643         LDA SPTR      GET FIRST CHAR
 23556 002004         INA
 23557 000000         LDA A,I
 23560 023657         CPA .CT       CARTRIDGE TAPE ?
 23561 023571         JMP .CTU       YES, THE LEFT ONE
 23562 023662         CPA .RM       THAT'S "R" AS IN PROM
 23563 023602         JMP .ROM       LOAD FROM PROM
 23564 023661         CPA .DC       DISC MAYBE ?
 23565 023624         JMP .DISC      A LITTLE HPIB IF YOU PLEASE
```

```
23566 023660        CPA .DS       DS LOADER??
23567 023615        JMP .DISTS    LOAD OVER DS
23570 022410        JMP CERR2     THAT AIN'T ONE OF MINE
*
23571 023716  .CTU  LDA .B20      DEFAULT
23572 104600        .JLB SCNSC    PARSE SCETC
23573 027572
23574 002404        CLA,INA
23575 102601        OTA CPUST     SAY IN LOADER
23576 104600        .JLB CTU      DO THE LOAD
23577 026004
23600 023723        JMP .BOOT?,I     ARE WE BOOTING
23601 023632        JMP BTERR     ERROR RETURN
*
*
*
23602 000503  .ROM  LDA TEMPO     READ OR WRITE ?
23603 023707        CPA .W
23604 022410        JMP CERR2     CANNOT WRITE TO ROM
23605 023715        LDA RMSC      DEFAULT
23606 104600        .JLB SCNSC    GET SELECT CODE AND FILE NUMBER
23607 027572
23610 104600        .JLB RMLDR    GO TO PROM LOADER
23611 026364
23612 023723        JMP .BOOT?,I     GOOD RETURN
23613 023632        JMP BTERR     ERROR RETURN
23614 025772  .LDER DEF MES62
*
*
23615 023714  .DISTS LDA DSSC      DEFAULT
23616 104600         .JLB SCNSC    PARSE SELECT CODE
23617 027572
23620 104600        .JLB DSLD     GO TO DS LOADER
23621 025040
23622 023723        JMP .BOOT?,I     GOOD RETURN
23623 023632        JMP BTERR     ERROR
*
23624 023713  .DISC LDA DCSC      DEFAULT
23625 104600        .JLB SCNSC    GET SELECT CODE ETC FROM STRING
23626 027572
23627 104600        .JLB DCLDR  GO TO HPIB LOADER
23630 026531
23631 023723        JMP .BOOT?,I    GOOD RETURN
*
23632 104600  BTERR .JLB CI.IZ     ENABLE VCP
23633 024411
23634 023614        LDA .LDER    OUTPUT ERROR MESSAGE
```

```
02443  23635 104600        .JLB PUTS
       23636 024245
02444  23637 000265        LDA LERR     GET ERROR NUMBER
02445  23640 104600        .JLB OUTD    OUTPUT ERROR NUMBER
       23641 024312
02446  23642 022257        JMP COMND    ERROR RETURN
02447*
02448*
02449*
02450  23643 000306  SPTR  DEF STRNG        POINTER TO STRING
02451*

02453*      CONSTANTS AND EQUATES
02454*
02455*
02456  23644 103003  .ENTI OCT 103003  HALT 03,C FOR REENTERING FRONT PANEL
02457  23645 000015  .CR   OCT 15           "CARRIAGE RETURN"
02458  23646 000024  .CTLT OCT 24        CONTROL T
02459  23647 000045  .%    OCT 45           "%"
02460  23650 000060  ZERO  OCT 60           "0"
02461  23651 000062  .2    OCT 62
02462  23652 000063  .3    OCT 63
02463  23653 000077  .?    OCT 77           "?"
02464  23654 000377  ..B377  OCT 377
02465  23655 001777  ..B1777 OCT 1777
02466  23656 077777  ..B77777 OCT 77777
02467  23657 041524  .CT   OCT 041524
02468  23660 042123  .DS   OCT 042123
02469  23661 042103  .DC   OCT 042103
02470  23662 051115  .RM   OCT 051115
02471  23663 000101  .A    OCT 101          "A"
02472  23664 000177  .DEL  OCT 177
02473  23665 000102  .B    OCT 102       ETC
02474  23666 000103  .C    OCT 103        ETC
02475  23667 000104  .D    OCT 104         ETC
02476  23670 000105  .E    OCT 105
02477  23671 000106  .F    OCT 106
02478  23672 000107  .G    OCT 107
02479  23673 000111  .I    OCT 111
02480  23674 000114  .L    OCT 114
02481  23675 000115  .M    OCT 115
02482  23676 000116  .N    OCT 116
02483  23677 000117  .O    OCT 117
02484  23700 000120  .P    OCT 120
02485  23701 000121  .Q    OCT 121
02486  23702 000122  .R    OCT 122
02487  23703 000123  .S    OCT 123
02488  23704 000124  .T    OCT 124
```

```
23705 000125  .U    OCT 125
23706 000126  .V    OCT 126
23707 000127  .W    OCT 127
23710 000130  .X    OCT 130
23711 000131  .Y    OCT 131
23712 000132  .Z    OCT 132
23713 002027  DCSC  OCT 002027    SELECT CODE OF DISC
23714 000024  DSSC  OCT 000024  SELECT CODE FOR DS LOADER
23715 000022  RMSC  OCT 000022    SELECT CODE OF ROM CARD
23716 000020  .B20  OCT 000020
23717 000010  .B10  OCT 000010
23720 000037  B37   OCT 000037
23721 100000  BIT15 OCT 100000
23722 000100  .B100 OCT 000100
23723 024077  .BOOT? DEF BOOT?
23724 177777  N1    DEC -1
23725 177776  N2    DEC -2
23726 177774  N4    DEC -4
23727 177770  N8    DEC -8
23730 177766  N10   DEC -10
23731 177760  N16   DEC -16
23732 177751  N23   DEC -23
23733 177750  N24   DEC -24
23734 177745  N27   DEC -27
23735 177740  N32   DEC -32
23736 177720  N48   DEC -48
23737 000002  D2    DEC +2
23740 000007  D7    DEC +7
23741 000040  D32   DEC +32
23742 000203  BUFF  DEF SAVEP
23743 000470  .DIG1 DEF DIG1
23744 102500  .LIA  OCT 102500
23745 000524  .RTRN JMP XEQT,I

*
*
*     MESSAGE "DEFS"
*
23746 025340  CRLF  DEF MES00
23747 025313  VERMG DEF MES01
23750 025342  PRMPT DEF MES02
23751 025350  HELP  DEF MES09
23752 025762  ERMES DEF MES46
23753 025667  SPC2  DEF MES11
23754 025703  SPC3  DEF MES22
23755 025677  MMESS DEF MES15
23756 025701  TMESS DEF MES16
23757 025705  CLMES DEF MES32
```

```
  VIRTUAL CONTROL PANEL PAGE 1

 23760 025714  PRMES DEF MES33
 23761 025720  MPMES DEF MES35
 23762 025723  PGMES DEF MES36
 23763 025726  KMES  DEF MES37
 23764 025751  ECMES DEF MES43
 23765 025734  PEMES DEF MES38
 23766 025742  SELFERR DEF MES41
 23767 025734  SOFTERR DEF MES38
 23770 025756  RMESS  DEF MES44
 23771 025671  PMESS  DEF MES12
 23772 025675  AMESS  DEF MES13
 23773 025676  BMESS  DEF MES14
       023774  EOP1  EQU *
*
 24000               ORG EPROM+4000B
```

VIRTUAL CONTROL PANEL PAGE 2

```
      024000  P2     EQU *
*
*     CONSTANTS AND SUCH FOR THIS PAGE
*
24000 000010  ..BKS  OCT 10        ASCII "BACKSPACE"
24001 000102  ..B    OCT 102
24002 023632  .BTERR DEF BTERR     DISC ERROR
24003 000177  ..DEL  OCT 177       ASCI DELETE
24004 000005  .ENQ   OCT 5         ASCII ENQ
24005 023435  .PRSET DEF PRSET     ENTRY FOR PRESET
24006 022172  .AGAIN DEF AGAIN
24007 022257  .COMND DEF COMND
24010 025704  .SPC1  DEF MES22+1
24011 025667  .SPC2  DEF MES11
24012 025347  ..BEL  DEF MES07
24013 001700  STRTR  DEF 1700B     COMMUNICATION AREA
24014 023517  EXEX.P1 DEF EXEX     CROSS TO PAGE 1
24015 022412  CERR.P1 DEF CERR           "
24016 023521  ..RUN   DEF BEXEX
24017 022255  ..NEXT  DEF NEXT
24020 000015  ...CR  OCT 15              "CARRIAGE RETURN"
24021 000127  ...W   OCT 127
24022 000077  ..?    OCT 77              "?"
24023 000060  .ZERO  OCT 60              "0"
24024 000001  .B1    OCT 000001
24025 000007  .B7    OCT 7
24026 000017  .B17   OCT 000017
24027 000024  .B24   OCT 000024
24030 000101  .B101  OCT 000101
      024003  .B177  EQU ..DEL
24031 000377  .B377  OCT 000377
24032 060000  .B60K  OCT 060000
24033 177777  .N1    DEC -1
24034 177400  .BLR   OCT  177400
24035 177773  .N5    DEC -5
24036 177772  .N6    DEC -6
24037 177771  .N7    DEC -7
24040 177770  .N8    DEC -8
24041 177766  .N10   DEC -10
24042 177730  ..N40   DEC -40
24043 177720  .N48   DEC -48       THIS IS NEGATIVE "ASCII ZERO"
24044 177745  .N27   DEC -27
24045 177746  .N26   DEC -26
24046 101400  .N32000 DEC -32000
24047 177677  .N65   DEC -65       THIS IS NEGATIVE "ASCII A"
24050 177637  .N97   DEC -97
24051 177645  .N91   DEC -91
24052 000002  .D2    DEC +2
```

```
24053 000012 .D10   DEC +10
24054 000020 .D16   DEC +16
24055 000040 .D32   DEC +32
24056 000050 .D40   DEC +40
24057 000100 .D64   DEC +64
24060 000141 .D97   DEC +97
24061 000133 .D91   DEC +91
24062 000466 .D310  DEC 310
24063 000470 .D312  DEC 312
24064 000467 .D311  DEC 311
24065 000472 .D314  DEC 314
24066 000500 .D320  DEC 320
24067 000473 .D315  DEC 315
24070 000475 .D317  DEC 317
24071 000470 ..DG1  DEF DIG1

*
24072 024001 MRBT  LDA ..B          MAKE IT A BOOT
24073 000503       STA TEMPO
24074 024765 MRBT2 LDA .SPTR
24075 001200       RAL
24076 000360       STA STORE.POINTER
*
24077 024052 BOOT? LDA .D2
24100 000203       STA SAVEP         SET P FOR STARTING ADDRESS
24101 002400       CLA
24102 000366       STA MAP
24103              LWD1              STORE STRING THROUGH MAP 0
24104 000000       DEF 0             POINT AT ZERO
24105 105762       JLY STMAP        SET UP MAP ZERO AGAIN
24106 027647
24107 024013       LDA STRTR         POINT AT COMMUNICATION AREA
24110 000205       STA SAVEB   B SHOULD POINT AT COMMUNICATION AREA
24111 000246       LDB MSIZE         GET MEMORY SIZE
24112              XSB1 '@A'           CROSS STORE
24114 002004       INA
24115 000360       LDB STORE.POINTER
24116 007004       CMB,INB           SUBTRACT STORE.POINTER
24117 024765       ADB .SPTR
24120 024765       ADB .SPTR          ADD START OF CHARS * 2
24121 000356       ADB LSTR          LAST CHAR B HAS NUMBER OF CHARS
                                        IN STRING
24122              XSB1 '@A'         SAVE NUMBER OF CHARS
24124 002004       INA
24125 001200       RAL               MAKE IT A BYTE ADDRESS
24126 006004       INB               COPY ONE EXTRA CHARACTER
24127 105741       CBX               SAVE COUNT IN X
24130 000000       LDB A             STORE LOCATION
```

VIRTUAL CONTROL PANEL PAGE 2

```
24131 000360        LDA STORE.POINTER GET FROM LOCATION
24132               MB01              MOVE STRING TO USER MAP
24133 000503        LDA TEMPO
24134 024001        CPA ..B          IS BOOT?
24135 024016        JMP ..RUN,I         YES, GO DO IT
24136 024017        JMP ..NEXT,I         NO, GO GET COMMAND
*
*
*     REENT IS WHEN BOOTEX OR A DIAGNOSTIC CALLS BACK THE FRONT PANEL
*
*
24137 002004  REENT INA      POINT AT HPIB ADDRESS
24140               XLB1 '@A'         GET SUBCHANNEL
24142 000270        STB SUBCH
24143 002004        INA      POINT AT UNIT NO.
24144               XLB1 '@A'         GET UNIT
24146 000267        STB UNIT
24147 002004        INA      POINT AT SECTOR NUMBER
24150               XLB1 '@A'         GET SECTOR NUMBER
24152 000274        STB FILE          SAVE IT          VW=1
24153 002004        INA      POINT AT CYLINDER OFFSET
24154               XLB1 '@A'         GET CYLINDER OFFSET
24156 000273        STB CYLNDR.OFFSET
24157 000275        STB HEAD.CYLINDER  ; SAVE IT      VW=2
24160 002004        INA
24161               XLB1 '@A'         GET VECTOR WORD THREE
24163 000276        STB SECTR.TRACK                    VW=3
24164 105762        JLY .PSET
24165 021633
24166 002400        CLA
24167 000265        STA LERR      NO LOADER ERROR
24170 104600        .JLB DCRLD        GO LOAD FROM DISK
24171 026524
24172 024175        JMP RENT2     GOOD RETURN
24173 102702        STC 2         ENABLE BREAK
24174 024002        JMP .BTERR,I  ERROR RETURN
24175 024001  RENT2 LDA ..B       B FOR BOOT
24176 000202        LDB SAVEE     GET E REG VALUE
24177 004010        SLB           IS SET?
24200 002400        CLA           ZERO FOR BOOT FLAG
24201 000503        STA TEMPO     SAVE BOOT FLAG
24202 003400        CCA
24203 000204        STA SAVEA     A GETS -1 FOR CALL BACK
24204 024074        JMP MRBT2
*
```

```
*
*    ROUTINE TO RESTORE "A", "B",  ETC BEFORE RUNNING
*
*    CALLING SEQUENCE:
*
*             JLB*  RSTOR
*             P+1  INTERRUPTS WERE ON
*             P+2  INTERRUPTS WERE OFF
*
*
*
24205 000546  RSTOR STB RRSTO     SAVE RETURN ADDRESS
24206 002400        CLA
24207 102601        OTA CPUST     INDICATE IN USER PROGRAM
24210 105745        LDX SAVEX     RESTORE X AND Y
24211 000207
24212 105755        LDY SAVEY
24213 000210
24214 000200        LDA SAVEI     GET INTERRUPT STATUS
24215 006400        CLB           CLEAR IT FOR
24216 000200        STB SAVEI      NEXT TIME
24217 000507        STB FIRST     RESET NOT FIRST TIME FLAG
24220 002011        SLA,RSS       WERE INTERRUPTS ON ?
24221 000546        ISZ RRSTO      NO, BUMP RETURN ADDRESS
24222 000206        LDA SAVEG     FETCH OLD GLOBAL REGISTER
24223 001621        ELA,ARS       IF IT WAS ON => E <= 1
24224 002002        SZA           WAS THE GR ZERO, IF SO NO OTA
24225 102602        OTA GR        RESTORE GLOBAL REGISTER VALUE
24226 002040        SEZ           WAS IT ON ?
24227 103102        CLF GR         YES, TURN IT BACK ON
24230 000201        LDA SAVEO     FETCH "O" REPLICA
24231 103101        CLO           WAS IT
24232 000010        SLA            OFF ?
24233 102101        STO             NO, BUT YOU WERE CLOSE
24234 000202        LDA SAVEE     PUT "E" BACK
24235 001500        ERA            THE WAY YOU FOUND IT
24236 000212        LDA SAVEZ     RESTORE Z
24237               CAZ
24240 000211        LDA SAVEQ     RESTORE Q, POSSIBLY TURN ON R3
24241               CACQ
24242 104200        DLD SAVEA+2000B NOW "A" AND  "B"
24243 002204
24244 000546        JMP RRSTO,I
*
*
*    OUTPUT A MESSAGE, TERMINATE ON NULL BYTE
*    ENTER WITH "A" = DEF MESSAGE
*
```

```
*
24245 000527  PUTS  STB RPUTS      SAVE RETURN ADDRESS
24246 001200        RAL            MAKE IT A BYTE ADDRESS
24247 000255        STA PPNTR      SAVE MESSAGE DEF
24250 024042        LDA ..N40
24251 000226        STA PUTCT      COUNTER FOR ENQ ACK
*
24252 000255  P.1   LDB PPNTR      FETCH A WORD
24253 105763        LBT
24254 002003        SZA,RSS        NULL ?
24255 000527        JMP RPUTS,I     YES, BAIL OUT
24256 104600        .JLB PUTCH     NO, PRINT IT
24257 024560
24260 000255        ISZ PPNTR       YES, BUMP POINTER
24261 000226        ISZ PUTCT      CHECK CHAR COUNT
24262 024252        JMP P.1        DO IT ALL AGAIN
24263 024042        LDA ..N40
24264 000226        STA PUTCT      COUNT FOR NEXT 40 CHARS
24265 104600        .JLB .ENQAK      DO ENQ ACK HANDSHAKE
24266 024270
24267 024252        JMP P.1
*

24270 000531  .ENQAK STB RENQAK
24271 104600        .JLB CI.ID     IDENTIFY
24272 024513
24273 024277        JMP .ENQAS     ASCII
24274 104600        .JLB TG.TB     TRANSMIT BUFFER TO DS
24275 024520
24276 000531        JMP RENQAK,I   RETURN
*
24277 102501  .ENQAS LIA CPUST     GET SWITCHES
24300 001727          ALF,ALF
24301 024055          AND .D32     MASK ENQ SWITCH
24302 002002          SZA          MUST BE ZERO FOR ENQ TO WORK
24303 000531          JMP RENQAK,I  RETURN DOING NOTHING
*
24304 024004          LDA .ENQ       GET ENQ CHAR
24305 104600        .JLB PUTCH
24306 024560
24307 104600        .JLB GETCH
24310 024540
24311 000531        JMP RENQAK,I RETURN
*
```

```
*
*
*     ROUTINE TO OUTPUT WHAT IS IN A AS A DECIMAL INTEGER.
*     POSITIVE NUMBERS ONLY
*
24312 000537  OUTD  STB ROUTD
24313 024071        LDB ..DG1      POINT TO DIGIT BUFFER
24314 000217        STB PNTR
24315 006400        CLB
24316 000251        STB CNTR       DIGIT COUNTER
24317 006400  OTDL  CLB            MAKE TWO WORD VALUE
24320 100400        DIV .D10       DIVIDE BY 10
24321 024053
24322 000217        STB PNTR,I     SAVE RMAINDER AS DIGIT
24323 000217        ISZ PNTR       POINT AT NEXT DIGIT
24324 000251        ISZ CNTR       ADD 1 TO COUNT
24325 002002        SZA            QUOTIENT ZERO YET??
24326 024317        JMP OTDL       NO, GET NEXT DIGIT
*
24327 000251        LDA CNTR
24330 003004        CMA,INA        MAKE COUNT NEGATIVE
24331 000251        STA CNTR
24332 000217  OTDL2 LDA PNTR
24333 024033        ADA .N1        SUBRACT ONE
24334 000217        STA PNTR       POINT AT THE PREVIOUS CHAR
24335 000217        LDA PNTR,I     GET DIGIT
24336 024023        ADA .ZERO      MAKE ASCII
24337 104600        .JLB PUTCH     OUTPUT THE CHAR
24340 024560
24341 000251        ISZ CNTR       MORE LEFT??
24342 024332        JMP OTDL2      YES
*
24343 000537        JMP ROUTD,I    RETURN

*
*
*     ROUTINE TO OUTPUT HEX OR OCTAL DIGITS     *
*     ENTER WITH NUMBER IN "A" REGISTER
*     IF "DFLAG" < 0 THEN OUTPUT ONLY ONE DIGIT
*
*
24344 000534  OUTN  STB ROUTN      RETURN ADDRESS
24345 000260        STA TEMP       SAVE NUMBER
24346 024010        LDA .SPC1       GO OUTPUT ONE SPACE
24347 104600        .JLB PUTS        SPACE
24350 024245
24351 000260        LDA TEMP       RESTORE NUMBER
24352 000363        LDB DFLAG      FETCH DATA TYPE FLAG
```

```
24353 006021          SSB,RSS        ONE DIGIT ?  ( < 0 => ONE DIGIT )
24354 024362          JMP OT1         NOPE, MORE THAN THAT
24355 024024          AND .B1
24356 024023          IOR .ZERO
24357 104600          .JLB PUTCH     YEP, JUST ONE OUTPUT IT
24360 024560
24361 024405          JMP OT2        NOW LEAVE
24362 024035   OT1    LDB .N5         SET DIGIT     ( DEC -5 )
24363 000251          STB CNTR        COUNTER
*
*    NONSENSE TO HANDLE SIGN BIT IN OCTAL MODE
*
24364 000066          CLE,ELA
24365 000260          STA TEMP       SAVE PARTIAL
24366 024023          LDA .ZERO       IS IT
24367 002040          SEZ             ZERO ?
24370 002004          INA              NO, MAKE IT A ONE
24371 104600          .JLB PUTCH       PRINT IT
24372 024560
24373 000260          LDA TEMP       FETCH PARTIAL
24374 001723   L1     ALF,RAR        NEXT DIGIT
24375 000260          STA TEMP       SAVE NEW PARTIAL
24376 024025          AND .B7        SAVE ONLY LOW NIBBLE  ( DEC +15 )
24377 024023          ADA .ZERO       IS IT GREATER        ( DEC -10 )
24400 104600          .JLB PUTCH      PRINT IT
24401 024560
24402 000260          LDA TEMP       FETCH PARTIAL
24403 000251          ISZ CNTR       DONE ?
24404 024374          JMP L1          NOPE
24405 024010   OT2    LDA .SPC1        YEP, NOW
24406 104600          .JLB PUTS      OUTPUT 2 SPACES
24407 024245
24410 000534          JMP ROUTN,I    BYE BYE
*
*
*
*
*    ROUTINE TO "BEEP" AT ERRORS
*
*
*
*
*    OUTPUT WHAT EVER IS IN "A"
*
```

```
*
*UTCH STB RPUTC
*     OTA DATA      SEND CHARACTER TO TERMINAL
*     STC DATA,C    START OPERATION
*     SFS DATA      DONE YET ?
*     JMP *-1        NOPE
*     JMP RPUTC,I    YES, EXIT
*
*
*     GET ONE CHARACTER, RETURNED IN THE LOW END OF "A"
*
*
*ETCH STB RGETC
*     LDA ..ICW       PUT ASIC INTO
*     OTA CMND       INPUT MODE
*     STC DATA,C    START INPUT OPERATION
*T.00 SFC DATA      IS IT SOUP YET?
*     JMP GT.01      YES !
*     LIA STATS     NO - CHECK FOR BREAK
*     RAL
*     SSA
*     JMP .PRSET,I  YES - BREAK
*     JMP GT.00     NO KEEP WAITING
*
*T.01 LIA DATA      OK, LET'S SEE WHAT YOU'VE DONE
*     AND .B377      WELL, HALF OF IT ANYWAY
*     STA CHAR      SAVE IT FOR ECHO
*     JMP RGETC,I

*
*
  24411 000575  CI.IZ STB RCI.IZ
  24412 102102        STF GR        CLEAR ALL INTERFACES
  24413 002400        CLA
  24414 102602        OTA GR
  24415 000514        LDA VCPSC    (P+1) ASCII
  24416 103602        OTA GR,C      TURN ON CARD
  24417 107723        CLC 23B,C     TURN OFF DMA
  24420 104600        .JLB CI.ID    INITIALIZE INTERFACE
  24421 024513
  24422 024616        JMP AS.IZ
*
  24423 002400  DS.IZ CLA           INITIALIZE DS INTERFACE
  24424 000000        ISZ A         DELAY TIME  this must be > 1 MS
  24425 024424        JMP *-1       FOR SET UP
  24426 024434        LDA VCPDS     VCP COMMAND
  24427 104600        .JLB DS.FT    TRY IT
  24430 024463
```

```
24431 024005        JMP .PRSET,I   NO GOOD
24432 104600        .JLB CS.CM   TELL CARD AGAIN TO GO INTO VCP MODE
24433 024577
24434 067400  VCPDS OCT 67400 ,
24435 000575        JMP RCI.IZ,I  RETURN
*
24436 024031  DS.TG LDA .B377     ADD RUB OUT <REQUEST INPUT>
24437 104600        .JLB OUT2C    OUTPUT TWO CHARACTERS          <<<<<
24440 024566
24441 104600        .JLB CS.CM    TELL CARD TO TRANSMITT
24442 024577
24443 060400        OCT 60400
24444 104600        .JLB CS.CM    NOW ASK FOR BUFFER
24445 024577
24446 061400        OCT 61400
24447 000577        JMP RTG.BF,I  RETURN
*
24450 104600  DS.IN .JLB CS.CM    ASK FOR INPUT
24451 024577
24452 061000        OCT 61000
24453 024031        AND .B377     MASK
24454 024545        JMP GETCR     RETURN VIA GETCH
*
24455 024032  DS.OT IOR .B60K     DS PUT BYTE REQUEST
24456 104600        .JLB I.O
24457 024607
24460 000541        JMP RPUTC,I
*
```

```
*
24461 000602  DS.WF STB RDS.FT    SAVE RETURN ADDRESS
24462 024466        JMP DS.FT+3  SKIP OUTPUT JUST FLAG
*
24463 000602  DS.FT STB RDS.FT    RETURN ADDRESS
24464 102630        OTA DATA
24465 103730        STC DATA,C
24466 024046        LDB .N32000 40 SEC TIME OUT, MACHINE INDEPENDENT
24467 102230  FTLP  SFC DATA      WAIT FOR FLAG
24470 024477        JMP FTGF      GOT IT
24471 000245        LDA TBGCNT
24472 002306        CCE,INA,SZA   WAIT 1.25 MS
```

```
24473 024472        JMP *-1
24474 000001        ISZ B
24475 024467        JMP FTLP       NOT DONE, CHECK FLAG AGAIN
24476 000602        JMP RDS.FT,I   TIMED OUT
24477 000602  FTGF  ISZ RDS.FT      GOT THE FLAG
24500 000602        JMP RDS.FT,I   GOOD RETURN
*
24501 067400  DSVCP OCT 67400
*
24502 000603  DS.CM STB RDS.CM     SAVE RETURN ADDRESS
24503 000001        LDA B,I        GET COMMAND
24504 104600        .JLB DS.FT     WAIT FOR FLAG
24505 024463
24506 025140        JMP DSLER      DS LOADER ERROR
24507 102530        LIA DATA       GET DATA
24510 000603        ISZ RDS.CM     ADJUST RETURN ADDRESS
24511 000000        LDB A          BOTH !!!!
24512 000603        JMP RDS.CM,I   RETURN
*
*
*
*
*
*
*

24513 000576  CI.ID STB RCI.ID
24514 000515        LDB ASFLG      CHECK WHICH INTERFACE
24515 006003        SZB,RSS
24516 000576        ISZ RCI.ID     INTELEGENT TYPE
24517 000576        JMP RCI.ID,I      RETURN
*
24520 000600  TG.TB STB RTG.TB
24521 104600        .JLB CI.ID     IDENTIFY INTERFACE
24522 024513
24523 000600        JMP RTG.TB,I   ASCII, DO NOTHING
24524 003400        CCA            TRANSMIT TWO -1 BYTES TO SAY
                                      TRANSMIT BUFFER
24525 104600        .JLB OUT2C
24526 024566
24527 104600        .JLB CS.CM     TELL CARD TO TRANSMIT
24530 024577
24531 060400        OCT 60400
24532 000600        JMP RTG.TB,I   RETURN
```

```
24533 000577 TG.BF STB RTG.BF  TRANSMIT BUFFER & REQUEST NEW BUFFER
24534 104600       .JLB CI.ID   IDENTIFY INTERFACE
24535 024513
24536 000577       JMP RTG.BF,I RETURN <NO FUNCTION>
24537 024436       JMP DS.TG    DS 1000
*
      024540 GETCH EQU *
24540 000542 IN1C  STB RGETC
24541 104600       .JLB CI.ID   IDENTIFY THE INTERFACE
24542 024513
24543 024632       JMP AS.IN    ASCII
24544 024450       JMP DS.IN    DS 1000
*
24545 024050 GETCR ADA .N97     FOLD 6BIT ASCII BY
24546 002020       SSA          SUBTRACTING TO TEST
24547 024556       JMP GETCR2   IS < a SO DO NOTHING
24550 024045       ADA .N26     CHECK FOR Z
24551 002021       SSA,RSS      GREATER THAN Z???
24552 024055       ADA .D32     DONT FOLD THESE
24553 024061       ADA .D91     DO FOLDING
24554 000261 GETCR3 STA CHAR     SAVE CHARACTER
24555 000542       JMP RGETC,I  RETURN
*
24556 024060 GETCR2 ADA .D97    UNDO SUBTRACT
24557 024554        JMP GETCR3

      024560 PUTCH EQU *
24560 000541 OUT1C STB RPUTC
24561 024031       AND .B377      MASK OFF LOWER CHARACTER
24562 104600       .JLB CI.ID   IDENTIFY
24563 024513
24564 024640       JMP AS.OT
24565 024455       JMP DS.OT    DS 1000
*
24566 000606 OUT2C STB ROUT2C
24567 000260       STA TEMP     SAVE
24570 001727       ALF,ALF      POSITION
24571 104600       .JLB PUTCH   OUTPUT UPPER HALF
24572 024560
24573 000260       LDA TEMP     GET WORD AGAIN
24574 104600       .JLB PUTCH   OUTPUT LOWER HALF
24575 024560
24576 000606       JMP ROUT2C,I
*
```

```
*
24577 000605  CS.CM STB RCS.CM    SAVE RETURN ADDRESS
24600 000001        LDA B,I       GET COMMAND
24601 104600        .JLB I.O      DO I/O
24602 024607
24603 000605        ISZ RCS.CM    ADJUST RETURN ADDRESS
24604 000605        JMP RCS.CM,I  RETURN
*
24605 000602  CS.WF STB RDS.FT    RETURN ADDRESS
24606 024466        JMP DS.FT+3   WAIT FOR FLAG ONLY
*
*
24607 000610  I.O   STB RI.O      RETURN ADDRESS
24610 102630        OTA DATA      OTB ???
24611 103730        STC DATA,C    START TRANSFER
24612 102330  I.00  SFS DATA
24613 024612        JMP I.00      KEEP TRYING
24614 102530  I.01  LIA DATA      GET DATA
24615 000610        JMP RI.O,I    RETURN
*

24616 102532  AS.IZ LIA STATS    CLEAR BREAK BIT
24617 024645        LDA TCCWO
24620 102632        OTA STATS    SET TRANSMITT
24621 102631        OTA CMND      (REMOVE DIAGNOSTIC)
24622 002400        CLA
24623 102630        OTA DATA      TRANSMIT A NUL
24624 103730        STC DATA,C
24625 102230        SFC DATA      WAIT FOR FLAG
24626 000575        JMP RCI.IZ,I  RETURN
24627 000000        ISZ A         TEST FOR TIME OUT
24630 024625        JMP *-3
24631 024005        JMP .PRSET,I      GO RESET COMPUTER
*
24632 024646  AS.IN LDA TCCWI     INPUT CONTROL WORD
24633 102631        OTA CMND
24634 104600        .JLB I.O      DO I/O
24635 024607
24636 024031        AND .B377     MASK UPPER BYTE
24637 024545        JMP GETCR     RETURN VIA GETCH
*
24640 024645  AS.OT LDB TCCWO     OUTPUT CONTROL WORD
24641 106631        OTB CMND
24642 104600        .JLB I.O      DO I/O
24643 024607
24644 000541        JMP RPUTC,I  RETURN
*
24645 001010  TCCWO OCT 001010
24646 006412  TCCWI OCT 006412
```

```
*
*
*     ROUTINE TO INPUT HEX OR OCTAL DIGITS
*     CALLING SEQUENCE:
*             JLB*  GETN
*             P+1  NO DATA ENTERED; JUST CHARACTER NOT BS OR ?
*             P+2  NEW DATA ENTERED
*
*     IF P+1:  A = XXXX  B = LAST CHAR
*     IF P+2:  A = DATA  B = 0  IF LAST CHAR WAS CR
*     IF P+2:  A = DATA  B = LAST CHAR
*
24647 000544  GETN  STB RGETN
24650 002400        CLA           INITIALIZE
24651 000470        STA DIG1       DIGIT
24652 000471        STA DIG2        STORAGE
24653 000472        STA DIG3         LOCATIONS
24654 000473        STA DIG4
24655 000474        STA DIG5
24656 000475        STA DIG6
*
24657 024036        LDA .N6        SETUP FOR OCTAL
24660 000251        STA CNTR      INITIALIZE COUNTER
24661 000476        STA DIGS       AND SPARE
24662 024071        LDA ..DG1     DEF FOR OCTAL   ( DIG1 )
24663 000217        STA PNTR      SET POINTER
24664 000220        STA PNTRS      AND SPARE
*
24665 104600  GET1  .JLB GETCH  GET ONE CHARACTER
24666 024540
24667 105762        JLY ISDIG     IS DIGIT IN RANGE??
24670 027632
24671 024703        JMP EXIT?
24672 024043        ADA .N48       MAKE "0" THRU "9" OUT OF IT
24673 000251        LDB CNTR      IS THE DIGIT
24674 006003        SZB,RSS        ZERO ?
24675 024711        JMP IERR      YES, THE BUFFER IS FULL
24676 000217        STA PNTR,I    SAVE IT IN A DIGIT BUFFER
24677 000217        ISZ PNTR      UPDATE THE DIGIT POINTER
24700 006004        INB           UPDATE THE
24701 000251        STB CNTR       DIGIT COUNTER
24702 024665        JMP GET1       WE NEED MORE
*
24703 000261  EXIT? LDB CHAR      A FRESH COPY OF "IT"
24704 024000        CPB ..BKS     IS IT BACKSPACE ?
24705 024721        JMP BKUP       YES, GO PROCESS IT
24706 024003        CPB ..DEL
24707 024007        JMP .COMND,I
24710 024735        JMP EX1
```

```
*
24711 024012  IERR  LDA ..BEL        INDICATE ERROR AND
24712 104600        .JLB PUTS
24713 024245
24714 024720        LDA BKKMS
24715 104600        .JLB PUTS      WIPE OUT THE OFFENDING CHAR
24716 024245
24717 024665        JMP GET1         GIVE 'EM ANOTHER TRY
24720 025770  BKKMS DEF MES48
*
24721 000251  BKUP  LDA CNTR       IS THERE ANYTHING
24722 000476        CPA DIGS        LEFT ?
24723 024015        JMP CERR.P1,I   NO, END OF BUFFER
24724 024033        ADA .N1         MOVE DIGIT COUNTER
24725 000251        STA CNTR        BACK ONE
24726 000217        LDA PNTR       NOW BACKUP
24727 024033        ADA .N1          THE BUFFER
24730 000217        STA PNTR         POINTER
24731 025037        LDA BKSMES
24732 104600        .JLB PUTS      MAKE THE CHAR GO AWAY
24733 024245
24734 024665        JMP GET1       TRY AGAIN
*
24735 000251  EX1   LDA CNTR       ANY NEW
24736 000476        CPA DIGS        DATA ?
24737 000544        JMP RGETN,I     NO, COUNTER NOT INC'ED
*
24740 000544        ISZ RGETN      SET FOR "GOOD" RETURN
24741 000251        LDA CNTR       HOW MANY DIGITS
24742 003004        CMA,INA         HAVE BEEN
24743 000476        ADA DIGS          INPUT ?
24744 000251        STA CNTR
24745 000220        LDA PNTRS      INITIALIZE DIGIT
24746 000217        STA PNTR        POINTER
24747 002400        CLA            START WITH A CLEAN SLATE
24750 000217  EX2   ADA PNTR,I     ADD A DIGIT TO PARTIAL SUM
24751 000217        ISZ PNTR       POINT TO NEXT DIGIT
24752 000251        ISZ CNTR       DONE ?
24753 024755        JMP *+2         NO, MORE TO GO
24754 024761        JMP EX3         YEP
24755 000066        CLE,ELA
24756 000066        CLE,ELA        MULTIPLY BY 8
24757 000066        CLE,ELA
24760 024750        JMP EX2        PROCESS NEXT DIGIT
*
24761 000261  EX3   LDB CHAR       RETRIEVE LAST CHARACTER
24762 024020        CPB ...CR
24763 006400        CLB
24764 000544        JMP RGETN,I
```

```
*
*     GETS   INPUTS A STRING FROM THE TERMINAL.  IT PUTS IT IN
*     STRNG WITH THE LENGTH IN LSTR. THE FIRST CHAR SHOULD BE IN CHAR
*     40 CHARS IS MAXIMUM INPUT.
*     IT ALLOWS BACKSPACING.
*
24765 000306  .SPTR DEF STRNG
*
24766 000532  GETS  STB RGETS       SAVE RETURN
24767 002400        CLA
24770 000356        STA LSTR        LENGTH OF STRING
24771 002004        INA
24772 000357        STA GSLR     TEMP IS LEFT/RIGHT BYTE FLAG 1 LEFT
                                     0 RIGHT
24773 024765        LDA .SPTR
24774 001200        RAL              MAKE IT A BYTE ADDRESS
24775 000360        STA STORE.POINTER       STRING POINTER
24776 000261  GETSL LDA CHAR        GET CHARACTER
24777 024000        CPA ..BKS       WAS BACKSPACE
25000 025021        JMP GSBS        BACK OUT A CHARACTER
25001 024020        CPA ...CR        CARRIAGE RETURN?
25002 000532        JMP RGETS,I      YES, RETURN. DONE WITH STRING
25003 024003        CPA ..DEL
25004 024007        JMP .COMND,I
*
25005 000360        LDB STORE.POINTER GET FLAG
25006 105764        SBT
25007 002400        CLA
25010 105764        SBT              CLEAR NEXT WORD
25011 000356        LDA LSTR
25012 024057        CPA .D64
25013 024015        JMP CERR.P1,I
25014 000356        ISZ LSTR        ADD TO CHARACTER COUNTER
25015 000360        ISZ STORE.POINTER  NEXT CHAR
25016 104600  GET.  .JLB GETCH       GET ANOTHER CHARACTER
25017 024540
25020 024776        JMP GETSL       GO AROUND AGAIN
*
*
25021 000356  GSBS  LDA LSTR
25022 024024        CPA .B1          CANT BACKSPACE OVER % CHAR
25023 024015        JMP CERR.P1,I   CANT BACKSPACE IF NO CHARACTERS
*
```

```
25024 024033          ADA .N1         DECREMENT NUMBER OF CHARS
25025 000356          STA LSTR
25026 000360          LDB STORE.POINTER
25027 024033          ADB .N1
25030 000360          STB STORE.POINTER  BACK UP A CHAR
25031 002400          CLA
25032 105764          SBT            CLEAR OUT THE LAST CHAR
25033 025037          LDA BKSMES
25034 104600          .JLB PUTS      OURPUT SPACE BACKSPACE
25035 024245
25036 025016          JMP GET.        GET NEXT CHARACTER
25037 025766   BKSMES DEF MES47

*  DISTIBUTED SYSTEMS LOADER
*
*
*
25040 000571   DSLD   STB RDSLD
25041 024024          LDA .B1
25042 102601          OTA CPUST        SAY IN LOADER
25043 102702          STC 2           ALLOWED TO BREAK FROM DS LOADER
25044 104600          .JLB S.SC       SET SELECT CODE
25045 026330
25046 025140          JMP DSLER     ERROR IN SELECT CODE SPECIFIED
25047 024062          LDA .D310
25050 000265          STA LERR      ERROR 310=TIME OUT AFTER SELF TEST
25051 104600          .JLB DS.WF     WAIT FOR DS SELF TEST
25052 024461
25053 025140          JMP DSLER     TIMED OUT
25054 000503          LDA TEMPO     CHECK IF THIS IS A DUMP
25055 024021          CPA ...W       READ OR WRITE?
25056 025225          JMP DSWR      IT'S A WRITE!!
25057 006400          CLB
25060 000516          STB EXLOAD    CLEAR EXTENDED LOAD FLAG
25061 024063   DSLDO  LDA .D312
25062 000265          STA LERR   ERROR 312=TO AFTER DOWN LOAD REQUEST
25063 025312          LDA DSDNL     ASK FOR A DOWN LOAD
25064 104600          .JLB DS.FT     WAIT FOR COMPLETION OF REQUEST
25065 024463
25066 025140          JMP DSLER     TIMED OUT
25067 000274          LDB FILE      GET FILE NUMBER
25070 000265   DSLD1  ISZ LERR       ERROR 313 TO AFTER FILE NUMBER
25071 107630          OTB DATA,C      PASS IT TO THE CARD
25072 104600          .JLB DS.WF     WAIT FOR IT TO COMPLETE
25073 024461
25074 025140          JMP DSLER     TIMED OUT SO ERROR
25075 007400          CCB           SET TO READ A FRAME
25076 000517          STB P3.CT     (FRAME COUNT TO -1)
```

```
*                         READ IN ONE RECORD
25077 104600  DSRD  .JLB DS.GT     GET WORD COUNT
25100 025175
25101 101050        LSR 8          POSITION COUNT IN B
25102 007007        CMB,INB,SZB,RSS MAKE COUNT NEG. (DONE?)
25103 025131        JMP DSDUN      YES
25104 000521        STB DSCNT      SAVE COUNT
25105 104600        .JLB DS.GT     GET LOAD ADDRESS
25106 025175
25107 000522        STB DSADD      SAVE LOAD ADDRESS
25110 000523        STB DSCHK      AND START CHECKSUM
25111 104600  DSRDL .JLB DS.GT     GET WORD REQUEST
25112 025175
25113               XSB1 '@DSADD'  STORE IT
25115 000522        ISZ DSADD
25116 000523        ADB DSCHK      ADD TO CHECKSUM
25117 000523        STB DSCHK
25120 000521        ISZ DSCNT      DONE WITH RECORD
25121 025111        JMP DSRDL      NO
25122 104600        .JLB DS.GT     GET CHECKSUM
25123 025175
25124 000523        CPB DSCHK      DOES CHECKSUM AGREE?
25125 025077        JMP DSRD       YES DO NEXT RECORD
25126 024064        LDA .D311
25127 000265        STA LERR       ERROR 311 = CHECKSUM ERROR
25130 025140        JMP DSLER      NO RETURN WITH ERROR

25131 104600  DSDUN .JLB DS.GT     GET ADDRESS AS FLAG
25132 025175
25133 006003        SZB,RSS        GOOD OR BAD
25134 025142        JMP DSCONT     GOOD COMPLETED
25135 024065        LDA .D314
25136 000265        STA LERR       ERROR 314 = BAD TRANSFER
25137 000205        STB SAVEB      SAVE STATUS IN B REG
25140 000571  DSLER ISZ RDSLD      INDICATE ERROR
25141 000571  DSEX  JMP RDSLD,I    RETURN
*
25142 000516  DSCONT ISZ EXLOAD    DONE?
25143 002001        RSS            NO
25144 025141        JMP DSEX       YES, ALL BLOCKS LOADED
*
25145 000516        LDA EXLOAD     FIRST TIME THROUGH??
25146 002020        SSA
25147 025165        JMP DSNXT      NO, GO GET NEXT FILE
```

```
*
25150                     XLA1 '0'
25152                     XLB1 '1'
25154 002003              SZA,RSS
25155 025141              JMP DSEX  IF LESS THAN ONE 32K CHUNK WE ARE DONE
25156 006002              SZB            IF PARTIAL ADD ONE
25157 002004              INA
25160 003004              CMA,INA        MAKE IT NEGATIVE
25161 000516              STA EXLOAD     SAVE COUNT
25162 000516              ISZ EXLOAD     DONE???
25163 025165              JMP DSNXT      NO, GO GET NEXT FILE
25164 025141              JMP DSEX       ALL BLOCKS LOADED
*
25165 000366        DSNXT ISZ MAP        NEXT 32K BLOCK
25166 000366              LDA MAP
25167 105762              JLY STMAP     SET MAP REGISTERS
25170 027647
25171 003400              CCA
25172 001665              ELA,CLE,ERA    ELIMINATE BIT 15
25173 000274              STA FILE       INDICATE CONTINUE LOAD
25174 025061              JMP DSLDO      DO NEXT LOAD
*
25175 000574        DS.GT STB RDS.GT
25176 000517              ISZ P3.CT      TIME FOR NEW FRAME?
25177 025216              JMP DS%GO      NO JUST READ A WORD
25200 024067              LDA .D315
25201 000265              STA LERR       ERROR 315=TO AFTER BUFFER REQUEST
25202 025250              LDA DSINR      GET BUFFER REQUEST
25203 104600              .JLB DS.FT      GIVE IT TO CARD
25204 024463
25205 025140              JMP DSLER      TIMED OUT
25206 102530              LIA DATA       NO GET BUFFER COUNT
25207 000001              STA B
25210 007004              CMB,INB        MAKE FRAME COUNT NEGATIVE
25211 000517              STB P3.CT      SAVE IT
25212 000265              ISZ LERR       ERROR 316 = TO AFTER COUNT ECHO
25213 104600              .JLB DS.FT      TELL CARD HOW MUCH TO TRANSFER
25214 024463
25215 025140              JMP DSLER      TIMED OUT
25216 024070        DS%GO LDA .D317      ERROR 317 = TO WAITING FOR DATA
25217 000265              STA LERR
25220 104600              .JLB DS.WF      WAIT FOR FLAG
25221 024461
25222 025140              JMP DSLER      IT DID SO ERROR
25223 107530              LIB DATA,C     OK GET DATA
25224 000574              JMP RDS.GT,I    RETURN
```

```
*     THIS ROUTINE DUMPS A MEMORY IMMAGE TO A REMOTE COMPUTER
*
25225 024066  DSWR  LDA .D320
25226 000265        STA LERR        ERROR 320 = VCP MODE TIME OUT
25227 024501        LDA DSVCP       TELL INTF TO GO INTO VCP MODE
25230 104600        .JLB DS.FT
25231 024463
25232 025140        JMP DSLER       TIMED OUT
25233 006400        CLB             SET STARTING ADDRESS
25234 000522        STB DSADD       SAVE IT
25235 002404  DSWR0 CLA,INA         1 PLUS RUBOUT
25236 104600        .JLB DS.B        OUTPUT 1 BYTE
25237 025302
25240 024031        LDA .B377        NOW RUBOUT
25241 104600        .JLB DS.B
25242 025302
25243 104600        .JLB DS.CM       TRANSMITT BUFFER
25244 024502
25245 060400        OCT 60400
25246 104600        .JLB DS.CM       ASK FOR BUFFER
25247 024502
25250 061400  DSINR OCT 61400
25251 104600        .JLB DS.CM       ASK FOR BYTE
25252 024502
25253 061000        OCT 61000
25254 024031        CPA .B377        CAN IT BE ACCEPTED?
25255 025277        JMP DSWEX       NO SO ERROR
25256 002003        SZA,RSS         DONE?
25257 025141        JMP DSEX        YES
25260 003004        CMA,INA         MAKE IT NEGATIVE
25261 000517        STA P3.CT       SAVE AS COUNTER
25262         DSWR1 XLA1 '@DSADD'     GET DATA
25264 000504        STA TEMP3       SAVE DATA
25265 001727        ALF,ALF
25266 104600        .JLB DS.B        TRANSFER CHARACTER
25267 025302
25270 000504        LDA TEMP3
25271 104600        .JLB DS.B
25272 025302
25273 000522        ISZ DSADD       MOVE ADDRESS UP ONE
25274 000517        ISZ P3.CT       DONE WITH THIS ONE?
25275 025262        JMP DSWR1       NO
25276 025235        JMP DSWR0       YES THEN MOVE TO NEXT TRANSFER
*
25277 000205  DSWEX STA SAVEB
25300 000265        ISZ LERR        ERROR 321=CENTRAL WONT ACCEPT DATA
25301 025140        JMP DSLER       ERROR RETURN
```

```
25302 000573  DS.B  STB RDS.B
25303 024031        AND .B377
25304 024032        IOR .B60K      DS PUT BYTE REQUEST
25305 104600        .JLB DS.FT     WAIT FOR FLAG
25306 024463
25307 025140        JMP DSLER     TIMED OUT
25310 102530        LIA DATA      GET DATA
25311 000573        JMP RDS.B,I    RETURN
*
25312 161001  DSDNL OCT 161001    DOWN LOAD COMMAND
*

*
      MESSAGES AND WORDS OF WISDOM      *
*
      SUP
*                                                          *
25313 006412  MES01 OCT 6412
25314 044120        ASC 8,HP A600/700 VCP
25315 020101
25316 033060
25317 030057
25320 033460
25321 030040
25322 053103
25323 050040
25324 006412        OCT 6412      THESE ARE "CARRIAGE RETURN"
25325 006412        OCT 6412       AND "LINE FEED" IN DISGUISE
25326 020040        ASC 9,  Type ? for help
25327 052171
25330 070145
25331 020077
25332 020146
25333 067562
25334 020150
25335 062554
25336 070040
25337 006412        OCT 6412
25340 006412  MES00 OCT 6412
25341 000000        OCT 0         NULL CHARACTER TO TERMINATE
*
25342 006412  MES02 OCT 6412
25343 053103  MES03 ASC 2,VCP>
25344 050076
25345 020021        OCT 020021    SPC AND DC1
25346 000000        OCT 000000
*
25347 003400  MES07 OCT 003400    BELL AND NULL
*
```

```
03401*
03402  25350 006412  MES09 OCT 6412
03403  25351 006412        OCT 6412
03404  25352 015463        OCT 015463    ESC 3    CLEAR ALL TABS
03405  25353 015446        OCT 015446    ESC &    MOVE THE
03406  25354 060464        OCT 060464    a   4     CURSOR TO
03407  25355 030103        OCT 030103    0   C      COLUMN 40
03408  25356 015461        OCT 015461    ESC 1    SET A TAB HERE
03409  25357 006412        OCT 6412
03410  25360 040454        ASC 9,A,B,X,Y,Q,Z,P,G,V
       25361 041054
       25362 054054
       25363 054454
       25364 050454
       25365 055054
       25366 050054
       25367 043454


       25370 053040
03411  25371 015511        OCT 015511    ESC I    TAB
03412  25372 051062        ASC 6,R20-R32 I/O
       25373 030055
       25374 051063
       25375 031040
       25376 044457
       25377 047440
03413  25400 006412        OCT 6412
03414  25401 042454        ASC 3,E,O,I
       25402 047454
       25403 044440
03415  25404 015511        OCT 015511
03416  25405 051103        ASC 3,RC CIR
       25406 020103
       25407 044522
03417  25410 006412        OCT 6412
03418  25411 046440        ASC 9,M Address  T data
       25412 040544
       25413 062162
       25414 062563
       25415 071440
       25416 020124
       25417 020144
       25420 060564
       25421 060440
03419  25422 015511        OCT 015511
03420  25423 051111        ASC 6,RI Int Mask
       25424 020111
```

```
25425 067164
25426 020115
25427 060563
25430 065440
25431 006412          OCT 6412
25432 046156          ASC 8,Lnn List memory
25433 067040
25434 046151
25435 071564
25436 020155
25437 062555
25440 067562
25441 074440
25442 015511          OCT 015511
25443 051120          ASC 5,RP Parity
25444 020120
25445 060562
25446 064564
25447 074440
25450 006412          OCT 6412
25451 015511          OCT 015511
25452 051123          ASC 6,RS Switches
25453 020123
25454 073551
25455 072143

25456 064145
25457 071440
25460 006412          OCT 6412
25461 041517          ASC 4,COMMANDS
25462 046515
25463 040516
25464 042123
25465 015511          OCT 015511
25466 051115          ASC 13,RMnn Map nn [Pnn Page nn]
25467 067156
25470 020115
25471 060560
25472 020156
25473 067040
25474 055520
25475 067156
25476 020120
25477 060547
25500 062440
25501 067156
25502 056440
```

VIRTUAL CONTROL PANEL PAGE 2

```
03432  25503 006412          OCT 6412
03433  25504 022522          ASC 3,%R Run
       25505 020122
       25506 072556
03434  25507 015511          OCT 015511
03435  25510 051127          ASC 4,RW WMAP
       25511 020127
       25512 046501
       25513 050040
03436  25514 006412          OCT 6412
03437  25515 022505          ASC 5,%E Run P=2
       25516 020122
       25517 072556
       25520 020120
       25521 036462
03438  25522 015511          OCT 015511
03439  25523 051104          ASC 8,RD Diagnose Mode
       25524 020104
       25525 064541
       25526 063556
       25527 067563
       25530 062440
       25531 046557
       25532 062145
03440  25533 006412          OCT 6412
03441  25534 022524          ASC 4,%T Test
       25535 020124
       25536 062563
       25537 072040
03442  25540 015511          OCT 015511
03443  25541 051106          ASC 6,RF I/O flags
       25542 020111
       25543 027517
       25544 020146
       25545 066141
       25546 063563
03444  25547 006412          OCT 6412
03445  25550 022503          ASC 8,%C Clear memory
       25551 020103
       25552 066145
       25553 060562
       25554 020155
       25555 062555
       25556 067562
       25557 074440
```

```
03446  25560 006412          OCT 6412
03447  25561 022520          ASC 5,%P Preset
       25562 020120
       25563 071145
       25564 071545
       25565 072040
03448  25566 006412          OCT 6412
03449  25567 022530          ASC 9,%XDVFFBUSC[string]
       25570 042126
       25571 043106
       25572 041125
       25573 051503
       25574 055563
       25575 072162
       25576 064556
       25577 063535
03450  25600 006412          OCT 6412
03451  25601 054072          ASC 13,X: Boot, Load, Write, User
       25602 020102
       25603 067557
       25604 072054
       25605 020114
       25606 067541
       25607 062054
       25610 020127
       25611 071151
       25612 072145
       25613 026040
       25614 052563
       25615 062562
03452  25616 006412          OCT 6412
03453  25617 042126          ASC 15,DV: Cart. Tape, RoM, DisC, DS
       25620 035040
       25621 041541
       25622 071164
       25623 027040
       25624 052141
       25625 070145
       25626 026040
       25627 051157
       25630 046454
       25631 020104

       25632 064563
       25633 041454
       25634 020104
       25635 051440
```

VIRTUAL CONTROL PANEL PAGE 2

```
25636 006412         OCT 6412
25637 043106         ASC 22,FF File, B Bus add., U Unit, SC Select code
25640 020106
25641 064554
25642 062454
25643 020102
25644 020102
25645 072563
25646 020141
25647 062144
25650 027054
25651 020125
25652 020125
25653 067151
25654 072054
25655 020123
25656 041440
25657 051545
25660 066145
25661 061564
25662 020143
25663 067544
25664 062440
25665 006412         OCT 6412
25666 000000         OCT 0
*
25667 020040   MES11 OCT 020040    2 SPACES
25670 000000         OCT 0
*
25671 006412   MES12 OCT 6412
25672 020040         ASC 2,   P    3 SPACES AND P
25673 020120
25674 000000         OCT 0
*
25675 040400   MES13 OCT 040400    A AND NULL
*
25676 041000   MES14 OCT 041000    B AND NULL
*
25677 020115   MES15 ASC 1, M      M AND NULL
25700 000000         OCT 0
*
25701 052000   MES16 OCT 052000    T AND NULL
25702 072000         OCT 072000    t and null
*
25703 020040   MES22 OCT 020040    SPC AND NULL
25704 020000         OCT 020000
*
```

```
03479*
03480  25705 041514  MES32 ASC 6,CLEAR MEMORY
       25706 042501

       25707 051040
       25710 046505
       25711 046517
       25712 051131
03481  25713 020000        OCT 020000
03482*
03483  25714 050122  MES33 ASC 3,PRESET
       25715 042523
       25716 042524
03484  25717 020000        OCT 020000
03485*

03487  25720 020115  MES35 ASC 2, MAP
       25721 040520
03488  25722 000000        OCT 0
03489*
03490  25723 050101  MES36 ASC 2,PAGE
       25724 043505
03491  25725 000000        OCT 000
03492*
03493  25726 045502  MES37 ASC 5,KB MEMORY
       25727 020115
       25730 042515
       25731 047522
       25732 054440
03494  25733 020000        OCT 20000   SPACE NULL
03495*
03496  25734 006412  MES38 OCT 6412      CRLF
03497  25735 050101        ASC 4,PAR ERR
       25736 051040
       25737 042522
       25740 051040
03498  25741 000000        OCT 0
03499*
03500  25742 006412  MES41 OCT 6412   CRLF
03501  25743 050124        ASC 5,PTEST ERR
       25744 042523
       25745 052040
       25746 042522
       25747 051040
03502  25750 000000        OCT 000000
```

```
03503*
03504  25751 045502  MES43 ASC 3,KB ECA
       25752 020105
       25753 041501
03505  25754 006412        OCT 6412
03506  25755 000000        OCT 0
03507*
03508  25756 006412  MES44 OCT 6412    CRLF
03509  25757 020040        ASC 2,   R    SPACE SPACE
       25760 020122
03510  25761 000000        OCT 000000    R AND NULL
03511*
03512  25762 006412  MES46 OCT 6412    CRLF
03513  25763 020477        ASC 2,!?
       25764 020040
03514  25765 000000        OCT 000
03515*
03516  25766 020010  MES47 OCT 020010    SPACE BACKSPACE
03517  25767 000000        OCT 0
03518*
03519  25770 004040  MES48 OCT 004040    BACKSPACE  SPACE
03520  25771 004000        OCT 004000    BACKSPACE NULL
03521*
03522  25772 046104  MES62 ASC 4,LDER ERR
       25773 042522
       25774 020105
       25775 051122
03523  25776 020000        OCT 020000     SPACE AND NULL
03524*
03525        025777  EOP2 EQU *
03526  26000              ORG EPROM+6000B
```

```
       026000  P3    EQU *
**********************************************************************
*                                                                    *
*                                                                    *
*    LOADER ROUTINES                                                 *
*                                                                    *
*                                                                    *
**********************************************************************
*
 26000 026004     JMP CTU
 26001 026364     JMP RMLDR
 26002 026531     JMP DCLDR
 26003 026524     JMP DCRLD
*
*  THESE JUMPS ARE FOR USER ROM CODE ENTRY TO THE LOADERS.
*  CALL THE LOADERS WITH A JLB INSTRUCTION. (JUMP AND LOAD B).
*
*  THE CALLING SEQUENCE IS
*
*          .JLB LOADER
*          JMP ERROR      ERROR RETURN ERROR NUMBER IN LERR
*  GOOD    ...            GOOD RETURN
*          ...
*
*
*  BEFORE CALLING THE LOADERS CERTAIN PARAMETERS MUST BE SET UP
*  SCETC  CONTAINS THE SELECT CODE, BUS ADDRESS, AND UNIT IN OCTAL
*  FILE   CONTAINS THE FILE NUMBER.
*  TEMPO  CONTAINS ASCII W IN THE LOW 8 BITS IF A WRITE IS TO BE DONE
*
*  THE LOADERS ASSUME THAT MAP ZERO IS SET UP PROPERLY FOR THE FIRST
*  32K OF THE LOAD, THAT THE DATA 1 MAP IS SET TO ZERO, AND THAT A
*  CLC 0,C INSTRUCTION HAS JUST BEEN EXECUTED. (THE I/O SYSTEM IS
*  QUIESCENT)
*
*  FOR THE CTU LOADER FILE 0 MEANS CURRENT LOCATION ON THE TAPE
*  FILE 1-N MEANS FIND THAT FILE ON TAPE FIRST, THEN LOAD.
*  UNIT IS 0 FOR LEFT TAPE AND 1 FOR RIGHT TAPE.
*  THE FORMAT OF THE TAPE IS ABSOLUTE BINARY. A ZERO LENGTH RECORD
*  WHICH IS NOT THE FIRST RECORD OF THE FILE INDICATES A SWITCH TO
*  THE NEXT 32K OF PHYSICAL MEMORY.
*  A WRITE TO TAPE WILL WRITE 4K WORDS WHERE THE BUS ADDRESS INDICATES
*  WHICH 4K TO WRITE.  IT WRITES IN ABSOLUTE BINARY, AND DOES
*  NOT WRITE A FILE MARK WHEN IT IS DONE.
*
*  FOR THE ROM LOADER TEMPO IS IGNORED. IT ALWAYS READS THE ROM.
*  THE FIRST TWO WORDS OF A ROM FILE ARE THE NUMBER OF 32K WORD CHUNKS
*  (BLOCK) AND THE REMAINDER AFTER THE LAST CHUNK (PARTIAL).
```

```
*  A FILE CAN HAVE MORE THAN ONE BLOCK IF IT STARTS ON A CARD BOUNDRY.
*  THE LOADER WILL GO TO THE NEXT CONSECUTIVE SELECT CODE WHE IT RUNS
*  OUT OF THE CURRENT CARD.
*  THE ROM LOADER IGNORES THE BUS ADDRESS AND UNIT FIELDS OF SCETC.
*
*  THE DISC LOADER HAS TWO ENTRY POINTS, DCLDR AND DCRLD.
*  DCLDR LOADS A DISC FILE USING THE FILE NUMBER.
*  DCRLD LOADS A DISC FILE USING A STARTING TRACK AND SECTOR.
*
*  A DISC FILE HAS THE SAME FORMAT AS A ROM FILE.  THE FIRST TWO WORDS
*  ARE BLOCK AND PARTIAL. FOR A LOAD THESE INDICATE HOW MUCH MEMORY TO
*  LOAD & THE BLOCK GOES IN PHYSICAL MEMORY LOCATION 0 (NOT THE A REG)
*  AND THE PARTIAL GOES INTO MEMORY LOCATION 1.  FOR A WRITE
*  (TEMPO IS W)  THESE TWO WORDS OF MEMORY INDICATE HOW MUCH TO WRITE
*  THUS A CRASH DUMP WOULD DUMP AS MUCH AS WAS PREVIOUSLY READ IN.
*  NOTE HOWEVER THAT THE LOADER ALWAYS TRANSFERS AT LEAST 32K WORDS.
*  BUS ADDRESS IS USED AS THE HPIB ADDRESS AND UNIT IS THE HEAD NUMBER
*  FOR 7906 DISC OR UNIT FOR FLOPPIES OR MINIFLOPPIES.
*
*  DCLDR MULTIPLIES THE FILE NUMBER BY 256 TO GET THE STARTING SECTOR
*  OF THE FILE.  FILE ZERO IS AT TRACK ZERO, SECTOR ZERO.
*
*  DCRLD EXPECTS THE GLOBAL REGISTER TO
*  BE SET TO THE SELECT CODE, THE HPIB ADDRESS IN SUBCH, THE UNIT
*  IN UNIT, THE SECTOR NUMBER OR VECTOR WORD ONE IN FILE,
*  THE CYLINDER OFFSET OR VECTOR WORD 2 IN CYLNDR.OFFSET AND
*  HEAD.CYLINDER, AND VECTOR WORD 3 IN SECTR.TRACK.
*  DCRLD DOES NOT LOOK AT SCETC.  THE VECTOR WORDS ARE FOR COMMAND SET
*  80 DISCS.
*
*     CARTRIDGE TAPE LOADER
*
*
26004 000550  CTU   STB RCTU      RETURN ADDRESS
26005 002400        CLA           CLEAR RECORD
26006 000501        STA TEMP2      FLAG
26007 104600        .JLB S.SC      SET SELECT CODE
26010 026330
26011 026157        JMP CTER         ERROR RETURN
*
26012 027756        LDA ..D110    ERRORS IN 100 RANGE FOR CTU
26013 000265        STA LERR
26014 000267        ISZ UNIT       LEFT CTU IS UNIT 1
26015 027677        LDA .PO
26016 000267        IOR UNIT      MAKE P UNIT
26017 000520        STA .PU
```

```
26020 000274         LDB FILE        FILE ZERO ?
26021 006003         SZB,RSS
26022 026061         JMP CTLD         YES, SKIP FILE FIND
26023 027676         LDA ECSAND     FIND THE FILE
26024 104600         .JLB CTO.W     OCT 15446
26025 026317
26026 000520         LDA .PU        OCT 70060
26027 104600         .JLB CTO.W
26030 026317
26031 000274         LDA FILE
26032 006400         CLB            TO GET 1ST NUMBER
26033 100400         DIV 012        DIVIDE BY 10
26034 027720
26035 000502         STB TEMP1
26036 027705         IOR .U0        OCT 72460
26037 104600         .JLB CTO.W
26040 026317
26041 000502         LDA TEMP1      DO SECOND NUMBER
26042 027723         IOR 060        MAKE IT A NUMBER
26043 104600         .JLB CTO.B
26044 026310
26045 027703         LDA .P2
26046 104600         .JLB CTO.W
26047 026317
26050 027674         LDA CDC1       OCT 41421
26051 104600         .JLB CTO.W
26052 026317
26053 104600         .JLB CTI.B     GET STATUS
26054 026301
26055 027710         CPA S          OK ?
26056 026061         JMP CTLD       YES
26057 000205         STA SAVEB      SAVE STATUS CODE IN B
26060 026157         JMP CTER       ERROR
*
26061 000503   CTLD  LDA TEMPO      CHECK IF READ OR WRITE
26062 027711         CPA W
26063 026167         JMP CT.DP       WANTS TO WRITE
*
26064 027676   GTREC LDA ECSAND         ESC    &
26065 104600         .JLB CTO.W
26066 026317
26067 000520         LDA .PU
26070 104600         .JLB CTO.W
26071 026317
26072 027704         LDA .S2
26073 104600         .JLB CTO.W
26074 026317
26075 027675         LDA RDC1             R      (DC1)
```

```
03660  26076 104600        .JLB CTO.W
       26077 026317
03661*
03662  26100 104600        .JLB CTI.W   GET FIRST WORD
       26101 026270
03663  26102 027673        CPA CTRS      DONE ?
03664  26103 026161        JMP DONE       YES, DONE WITH LOAD
03665*
03666  26104 104600        .JLB CTI.W   SKIP THE
       26105 026270
03667  26106 104600        .JLB CTI.B    COUNT WORDS
       26107 026301
03668*
03669  26110 027706        LDA .DC1      ASCII "DC1"
03670  26111 000501        STA TEMP2     INITIALIZE RECORD FLAG
03671  26112 104600        .JLB CTO.B      TELL TERMINAL TO TRANSMIT
       26113 026310
03672*
03673  26114 104600        .JLB CTI.B   GET FIRST BYTE ( RECORD LENGTH )
       26115 026301
03674  26116 003004        CMA,INA       MAKE IT NEGATIVE
03675  26117 000251        STA CNTR        INITIALIZE COUNTER
03676  26120 104600        .JLB CTI.B   SKIP UNUSED BYTE
       26121 026301
03677*
03678  26122 104600        .JLB CTI.W   GET LOAD ADDRESS
       26123 026270
03679  26124 000511        STA POINTER     INITIALIZE POINTER
03680  26125 000502        STA TEMP1       AND CHECKSUM
03681  26126 000251        LDA CNTR      CHECK FOR ZERO COUNT
03682  26127 002002        SZA
03683  26130 026141        JMP CTLDL     NONZERO, GO LOAD A RECORD
03684*
03685  26131 104600        .JLB CTI.W    SKIP THE CHECKSUM
       26132 026270
03686  26133 000366        LDA MAP
03687  26134 002004        INA
03688  26135 000366        STA MAP       NEXT MAP
03689  26136 105762        JLY STMAP    SET UP THE MAP
       26137 027647
03690  26140 026064        JMP GTREC    GET RECORDS FOR NEW MAP
03691*
03692  26141 104600  CTLDL .JLB CTI.W   GET A WORD OF DATA
       26142 026270
03693*
```

```
26143                  XSA1 '@POINTER'   STORE IT IN MAIN MEMORY
*
26145 000502           ADA TEMP1     ADD IT TO THE
26146 000502           STA TEMP1      CHECKSUM
26147 000511           ISZ POINTER     BUMP POINTER
26150 000251           ISZ CNTR      DONE WITH RECORD ?
26151 026141           JMP CTLDL      NO, GET ANOTHER WORD
*
26152 104600           .JLB CTI.W   GET CHECK SUM FROM THE TAPE
26153 026270
26154 000502           CPA TEMP1     DOES IT MATCH ?
26155 026064           JMP GTREC      YES, GET ANOTHER RECORD
*
26156 000265    .CKSM  ISZ LERR       ERROR 111 = CHECKSUM ERROR
26157 000550    CTER   ISZ RCTU       BUMP RETURN ADDRESS TO
26160 000550           JMP RCTU,I      ERROR RETURN
*
26161 000501    DONE   LDB TEMP2     WAS A RECORD
26162 006002           SZB            READ ? ( FLAG NO. 0 )
26163 000550    CTEX   JMP RCTU,I      YES, SPLIT
26164 000265           ISZ LERR
26165 000265           ISZ LERR      ERROR 112 = EOF ONLY
26166 026157           JMP CTER        OUTPUT ERROR MESSAGE
*
26167 000270    CT.DP  LDA SUBCH     WRITE TO CTU
26170 001727           ALF,ALF
26171 001700           ALF           SET ADDRESS
26172 000511           STA POINTER   ADDRESS POINTER
26173 027751           LDA M64
26174 000501           STA TEMP2     SET NUMBER OF BLOCKS
*
26175 000501    CTDP0  LDB TEMP2     END OF WRITE ?
26176 006003           SZB,RSS
26177 026163           JMP CTEX
26200 027676           LDA ECSAND    ESC &
26201 104600           .JLB CTO.W
26202 026317
26203 000520           LDA .PU
26204 104600           .JLB CTO.W
26205 026317
26206 027700           LDA .$D1
26207 104600           .JLB CTO.W
26210 026317
26211 027701           LDA ASC34     3  4
26212 104600           .JLB CTO.W
26213 026317
26214 027702           LDA WENQ      W  (ENQ)
```

```
26215 104600          .JLB CTO.W
26216 026317
26217 104600          .JLB CTI.B
26220 026301
26221 027715          CPA 06         WAIT FOR ACKNOWLEDGEMENT
26222 002001          RSS
26223 026175          JMP CTDPO      TRY AGAIN
26224 027751          LDA M64
26225 000251          STA CNTR       SET FOR ONE BLOCK
26226 003004          CMA,INA
26227 001727          ALF,ALF        PUT POSITIVE COUNT IN UPPER HALF
26230 104600          .JLB CTO.W
26231 026317
26232 000511          LDA POINTER    GET ADDRESS
26233 000502          STA TEMP1      START CHECKSM
26234 104600          .JLB CTO.W     SEND ADDRESS
26235 026317
26236           CTDPL XLA1 '@POINTER' GET WORD
26240 000000          LDB A
26241 000502          ADB TEMP1      ADD TO CHETEMP1
26242 000502          STB TEMP1
26243 104600          .JLB CTO.W
26244 026317
26245 000511          ISZ POINTER
26246 000251          ISZ CNTR       DONE ?
26247 026236          JMP CTDPL      NO
26250 000502          LDA TEMP1
26251 104600          .JLB CTO.W     OUTPUT CHECKSUM
26252 026317
26253 000501          ISZ TEMP2      MORE?
26254 000000          NOP            NO
26255 027706          LDA 021        DC1
26256 104600          .JLB CTO.B
26257 026310
26260 104600          .JLB CTI.B     CHECK RESULTS
26261 026301
26262 027710          CPA S          OK ?
26263 026175          JMP CTDPO     YES
26264 000205          STA SAVEB      SAVE STATUS CODE RETURNED
26265 027757          LDA ..D120
26266 000265          STA LERR       LOADER ERROR 120 = CTU WRITE ERROR
26267 026157          JMP CTER       ERROR
*
**********************************************************************
```

```
*
26270 000551  CTI.W STB RTI.W     RETURN ADDRESS
26271 104600        .JLB CTI.B   GET THE FIRST BYTE
26272 026301
26273 001727        ALF,ALF       PUT IN UPPER BYTE
26274 000260        STA TEMP      SAVE IT
26275 104600        .JLB CTI.B   NOW THE SECOND BYTE
26276 026301
26277 000260        ADA TEMP      BUILD A WORD
26300 000551        JMP RTI.W,I
*
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*
26301 000552  CTI.B STB RTI.B
26302 027671        LDA .ICW      PUT ASIC INTO
26303 102631        OTA CMND       INPUT MODE
26304 104600        .JLB I.O       READ A BYTE
26305 024607
26306 027731        AND 0377      SAVE LOW BYTE ONLY
26307 000552        JMP RTI.B,I
*
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*
26310 000553  CTO.B STB RTO.B
26311 027731        AND 0377      MASK OFF UPPER BYTE
26312 027672        LDB .OCW      PUT ASIC INTO
26313 106631        OTB CMND       OUTPUT MODE
26314 104600        .JLB I.O      OUTPUT A BYTE
26315 024607
26316 000553        JMP RTO.B,I
*
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*
26317 000554  CTO.W STB RTO.W
26320 000260        STA TEMP      SAVE A COPY
26321 001727        ALF,ALF       POSITION FIRST BYTE
26322 104600        .JLB CTO.B   GO OUTPUT ONE BYTE
26323 026310
26324 000260        LDA TEMP      GET A FRESH COPY
26325 104600        .JLB CTO.B   OUTPUT THE OTHER BYTE
26326 026310
26327 000554        JMP RTO.W,I
*
```

```
*     SET SELECT CODE AND OTHER USEFUL VALUES
*
26330 000572  S.SC  STB RS.SC      SAVE RETURN ADDRESS
26331 027713        LDA 02
26332 000265        STA LERR       ERROR 2 = SELECT CODE < 20
26333 000264        LDA SCETC      GET DEFAULT SELECT CODE
26334 000204        STA SAVEA      GOING TO START WITH THIS VALUE
26335 027723        AND 060        MUST BE OVER 20 OCT
26336 002003        SZA,RSS
26337 026363        JMP SCER       INTERNAL.ERROR
26340 000265        ISZ LERR       ERROR 3 = I/O CARD NO RESPONSE]
26341 000264        LDA SCETC
26342 027725        AND 077
26343 103602        OTA GR,C       SET AND ENABLE GLOBAL REGISTER
26344 002400        CLA
26345 103502        LIA GR,C       CHECK FOR RESPONCE
26346 002003        SZA,RSS
26347 026363        JMP SCER       NO RESPONSE
*
26350 000264        LDB SCETC
26351 005700        BLF
26352 005723        BLF,RBR        MOVE TO BUSS ADDRESS
26353 000001        LDA B
26354 027716        AND 07         MASK
26355 000270        STA SUBCH
26356 005723        BLF,RBR
26357 000001        LDA B
26360 027716        AND 07
26361 000267        STA UNIT
*
*
26362 000572        ISZ RS.SC      SKIP OVER ERROR RETURN
26363 000572  SCER  JMP RS.SC,I     AND RETURN

*
*
*     ROM LOADER
*
*
26364 000556  RMLDR STB RRMLD      SAVE RETURN ADDRESS
*
26365 002404        CLA,INA
26366 102601        OTA CPUST      SAY IN LOADR
26367 104600        .JLB S.SC      SET SELECT CODE
26370 026330
26371 026475        JMP RMERR        ERROR RETURN
*
```

```
26372 000274        LDA FILE       GET "FILE"
26373 003000        CMA            MAKE IT NEGATIVE
26374 000274        STA FILE        AND SET FILE COUNTER
26375 027762        LDA ..D211
26376 000265        STA LERR       ERROR 211 = END OF PROGRAMS
26377 002400        CLA            START AT ADDRESS 0
26400 006400        CLB
26401 000260  ROM2  STB TEMP       SAVE CURRENT ADDRESS
26402 106631        OTB CMND       OUTPUT IT TO THE PROM CARD
26403 102730        STC DATA       READ ONE LOCATION
26404 007400        CCB            SETUP FOR END-OF-PROGRAM TEST
26405 106530        LIB DATA       FETCH ONE WORD
26406 006007        INB,SZB,RSS    CHECK FOR ALL ONES
26407 026475        JMP RMERR      ALL ONES FOUND, END OF PROGRAMS
26410 006020        SSB            SHOULD BE POSITIVE FOR NEW FORMAT
26411 026474        JMP RMERR2     ANOTHER ROM ERROR
26412 102530        LIA DATA       GET BLOCK COUNT AGAIN
26413               XSA1 '0'         STORE NUMBER OF BLOCKS
26415 102730        STC DATA       ON TO PARTIAL
26416 106530        LIB DATA       GET PARTIAL
26417               XSB1 '1'         STORE PARTIAL
26421 000266        STB PARTIAL    SAVE PARTIAL
26422 006002        SZB            PARTIAL?
26423 002004        INA            YES, ANOTHER BLOCK
26424 003004        CMA,INA        COMPLEMENT BLOCK
26425 000216        STA D1SV       SAVE BLOCK NUMBER
26426 002007        INA,SZA,RSS    ONLY ONE BLOCK?
26427 026433        JMP ROM4       YES, DONT CHECK FOR CARD BOUNDRY
26430 000260        LDA TEMP
26431 002002        SZA            MORE THAN ONE BLOCK MUST START ON
                                      CARD BOUNDARY
26432 026473        JMP RMERR3     ANOTHER ERROR
26433 000260  ROM4  ADB TEMP       STILL IN THE RUNNING,  BUILD  NEXT
                                      ADDRESS
26434 000274        ISZ FILE       IS THIS THE GOOD ONE ?
26435 026401        JMP ROM2        NO, KEEP TRYING
*
26436 027713        LDA O2         ALREADY READ FIRST 2 LOCATION
26437 027742  ROM5  LDB O100000    32K COUNT
26440 000216        ISZ D1SV       LAST BLOCK?
26441 002001        RSS
26442 000266        LDB PARTIAL    YES,USE PARTIAL AS COUNT
26443 007004        CMB,INB
26444 000000        ADB A          ADD A TO COUNT SINCE IS TWO FIRST
                                      TIME THROUGH
26445 000251        STB CNTR       STOR COUNT IN CNTR
26446 102730  ROM3  STC DATA       NEXT ADDRESS
26447 106530        LIB DATA       READ CONTENTS
```

```
26450                    XSB1 '@A'           STORE IN MAIN MEMORY
26452 002004             INA               NEXT ADDRESS
26453 000251             ISZ CNTR          COUNT THE WORD, DONE ?
26454 026446             JMP ROM3           NO, JUST TRY ONE MORE
26455 000216             LDA D1SV
26456 002003             SZA,RSS           DONE?
26457 000556             JMP RRMLD,I       GO SEE WHAT KIND OF LOAD THIS WAS
*
26460 000366             LDA MAP
26461 002004             INA
26462 000366             STA MAP
26463 105762             JLY STMAP        SET UP MAP FOR NEXT 32K
26464 027647
26465 102502             LIA 2
26466 002004             INA               ON TO NEXT CARD
26467 102602             OTA 2
26470 002400             CLA               START AT ADDRESS ZERO
26471 102631             OTA CMND          SET ADDRESS ON CARD
26472 026437             JMP ROM5          GO LOAD NEXT BUNCH
*
26473 000265      RMERR3 ISZ LERR          LOADER ERROR 113 = BIGGER THAN 32K
                                              MUST START ON CARD
*                      BOUNDARY
26474 000265      RMERR2 ISZ LERR          LOADER ERROR 112 = BAD FORMAT
26475 000556      RMERR ISZ RRMLD          BUMP RETURN ADDRESS
26476 000556             JMP RRMLD,I       ERROR RETURN

*
*
*     HPIB DISC LOADER
*
*     AUTO BOOT FROM DISC
*
26477 024072      ..MRBT DEF MRBT
26500 021466      .PTLER DEF PTLER
26501 177704      TRYNM  DEC -60           TRY 60 TIMES EVERY 2 SECONDS FOR
                                              2 MINUTES
26502 002027      .DCSC  OCT 2027          DEFAULT SELECT CODE FOR DISC
*
26503 026501      PTDC   LDA TRYNM              NUMBER OF RETRYS ON POWERUP
26504 000252             STA TRYCT
26505 102702             STC 2             BREAK ALLOWED DURING DISC LOAD
26506 026502      PTLP   LDA .DCSC  GET DEFAULT SELECT CODE FOR AUTO BOOT
26507 000264             STA SCETC         SAVE IT
26510 104600             .JLB DCLDR
26511 026531
26512 026477             JMP ..MRBT,I  GOOD BOOT, GO FINISH IT
26513 027754             LDB M1600         WAIT 2 SECONDS BEFORE RETRY
```

```
26514 000245  PTWLP LDA TBGCNT    GET COUNT FOR 1.25 MS
26515 002306        CCE,INA,SZA
26516 026515        JMP *-1       WAIT  1.25 MS
26517 000001        ISZ B
26520 026514        JMP PTWLP
26521 000252        ISZ TRYCT     ANOTHER RETRY?
26522 026506        JMP PTLP
*
26523 026500        JMP .PTLER,I   NO, DISC ERROR
*
*
26524 000557  DCRLD  STB RDCLD    REENTER FOR DISK CALL BACK ENTRY
                                     TO LOADER
26525 103102         CLF 2
26526 002404         CLA,INA
26527 102601         OTA CPUST
26530 026546         JMP DISCO
*
*
*      NORMAL ENTRY AFTER %BOOT DISC OR %LOAD DISK
*
*
26531 000557  DCLDR STB RDCLD     SAVE RETURN ADDRESS
*
26532 002404        CLA,INA
26533 102601        OTA CPUST
*
26534 006400        CLB           ZERO SELECT CODE, UNIT, FILE, ETC
26535 000273        STB CYLNDR.OFFSET
26536 000275        STB HEAD.CYLINDER
26537 000276        STB SECTR.TRACK
*
26540 104600        .JLB S.SC     SET SELECT CODE
26541 026330
26542 026632        JMP DCER      ERROR RETURN
26543 000274        LDA FILE
26544 001727        ALF,ALF        MULT BY 256 TO GET SECTOR NUMBER
26545 000274        STA FILE
*
*
26546 002400  DISCO  CLA
26547 000271         STA DISC.ID
26550 104600        .JLB DC.IN    INITIALIZE
26551 026634
*
26552 002400        CLA              DO 64KB TRANSFER
26553 104600        .JLB DC.RW          NOW READ/WRITE IT
26554 027137
26555 026632        JMP DCER            ERROR,CAN WE RETRY ?
```

VIRTUAL CONTROL PANEL PAGE 3

```
*
26556                XLA1 '0'
26560                XLB1 '1'
26562 000266         STB PARTIAL   SAVE PARTIAL
26563 002003         SZA,RSS       ZERO BLOCKS?
26564 026633         JMP DCEX      YES, WE ARE DONE THEN
*
26565 006002         SZB           NONZERO PARTIAL??
26566 002004         INA           IF SO GET NEXT BLOCK
26567 027743         ADA  .M1    SUBTRACT ONE SO COUNT STARTS AT ZERO
26570 002003         SZA,RSS    ONE BLOCK NO PARTIAL or partial only?
26571 026633         JMP DCEX      yes, we are done
*
26572 000216         STA D1SV      SAVE BLOCK NO.
*
26573 000366         LDA MAP       CURRENT MAP (ZERO)
26574 002104   DCLP  CLE,INA           BUMP TO NEXT BLOCK
26575 000366         STA MAP
26576 105762         JLY STMAP    SET IT UP
26577 027647
*
*     BUMP TO NEXT DISC ADDRESS (NEXT FILE?)
*
26600 000274         LDA FILE      ADD VALUE OF 32K TO FILE
26601 027732         ADA 0400      IE. 256 BLOCKS
26602 000274         STA FILE      SAVE AS SECTOR ADDRESS
26603 000275         LDB HEAD.CYLINDER
26604 002040         SEZ           RIPPLE THROUGH VECTOR
26605 006104         CLE,INB
26606 000275         STB HEAD.CYLINDER
26607 000276         LDB SECTR.TRACK
26610 002040         SEZ
26611 006004         INB
26612 000276         STB SECTR.TRACK
*
26613 104600         .JLB DC.IN    SET UP
26614 026634
*
26615 002400         CLA           DO 64KB TRANSFER
26616 000366         LDB MAP
26617 000216         CPB D1SV      LAST TRANSFER??
26620 000266         LDA PARTIAL   YES, ONLY LOAD PARTIAL
26621 001200         RAL
26622 003004         CMA,INA       COMPLEMENT FOR NEGATIVE COUNT
26623 104600         .JLB DC.RW    DO THE XFER
26624 027137
26625 026632         JMP DCER      BAD NEWS
*
```

```
26626 000366          LDA MAP       GET MAP JUST USED
26627 000216          CPA D1SV      DONE?
26630 026633           JMP DCEX     YES
26631 026574          JMP DCLP      KEEP ON TRUCKING
*
*
26632 000557    DCER  ISZ RDCLD     SET FOR ERROR
26633 000557    DCEX  JMP RDCLD,I    RETURN
*

*
*     INITIALIZE BUSS
*
26634 000566    DC.IN STB RDCIN    SAVE RETURN ADDRESS
26635 027760          LDA ..D411
26636 000265          STA LERR     ERROR 411 = TO READING DISC TYPE
26637 027751          LDA M64
26640 000253          STA DCTO      SET TIME OUT TO 30 SECONDS
26641 000271          LDA DISC.ID
26642 027714          CPA O3        7906 ?
26643 026646          JMP *+3       MUST INITIALIZE !!
*
26644 002002          SZA           FIRST TIME ?
26645 026710          JMP DC.IO     NO SKIP INITIALIZE
26646 027744          LDA M2
26647 104600          .JLB PHIN
26650 027476
26651 070200          OCT 070200    PHI ON-LINE
26652 060063          OCT 060063    REN,IFC,WRITE,FLUSH FIFO
26653 000245          LDA TBGCNT    SET TIME OUT. GET 1.25 MS TIME
26654 002306          CCE,INA,SZA   THIS IS WORTH MACHINE INDEPENDENT
                                        IFC TIME
26655 026654          JMP *-1        1.25 mSEC
26656 000272          STA UNIT.HEAD   ; HEAD NUMBER ZERO
26657 104600          .JLB PHIFL        FLUSH THE FIFO
26660 027535
*
*     READ AND SET DISC TYPE
*      AND FILE POSITION
*
26661 104600          .JLB PHI.L        TELL PHI TO LISTEN
26662 027436
26663 000537          OCT 000537         WITH A SECONDARY OF UNTALK
26664 000270          LDA SUBCH      BUILD SECONDARY WITH HPIB ADDRESS
26665 027667          IOR TLK
26666 027670          IOR LSN
26667 104600          .JLB HPIB         SEND IT TO THE CARD
26670 027521
```

```
26671 104600        .JLB PHI
26672 027475
26673 001002        OCT 001002
*
26674 104600        .JLB PHI.I       GET DISC TYPE
26675 027507
26676 001727        ALF,ALF
26677 000271        STA DISC.ID      SAVE UPPER BYTE
26700 104600        .JLB PHI.I        GET SECOND BYTE
26701 027507
26702 000271        ADA DISC.ID      MERGE
26703 000271        STA DISC.ID       DISC TYPE
*
*  DO A UNIVERSAL CLEAR AND READ STATUS
*
26704 104600        .JLB PHI.TALK    PHI TALK
26705 027435
26706 000424        OCT 00424        UNIVERSAL DEVICE CLEAR
*
*    SEE IF DISC IS CS80 TYPE ??
*
26707 000271        LDA DISC.ID      DISC TYPE
26710 027737  DC.IO AND 01101         MASK
26711 027163        CPA 01001        DISC PLUS LINUS ?
26712 027107        JMP DC80         YEP
26713 027672        CPA 01000        DISC ONLY?
26714 027107        JMP DC80         YEP
26715 027736        CPA 01100        LINUS ONLY ?
26716 027121        JMP DC80.        YEP
*
*     NOPE CHECK FUTHER
*
26717 000265        ISZ LERR     ERROR 412 = TO UDC OR READ STSTUS
26720 104600        .JLB PHI.TALK
26721 027435
26722 000550        OCT 00550        PHI TALK
*
26723 104600        .JLB PHI
26724 027475
26725 000003        OCT 3            READ STATUS
*
26726 000267        LDA UNIT
26727 000271        LDB DISC.ID      CHECK FOR IDC
26730 027714        CPB 03          IF IT IS THEN
26731 002400         CLA           MAKE UNIT ZERO
26732 027672        IOR BIT9     ADD BIT 9
26733 104600        .JLB HPIB    PASS IT TO CARD
26734 027521
```

```
26735 104600          .JLB PHI.L    PHI LISTEN
26736 027436
26737 000550          OCT 00550
*
26740 104600          .JLB PHI
26741 027475
26742 001003          OCT 1003      TRANSFER 3 BYTES
*
26743 104600          .JLB PHI.I    GET BYTE
26744 027507
26745 000265          ISZ LERR   ERROR 413 = STSTUS ERROR, STSTUS IN B
26746 000205          STA SAVEB     SAVE STATUS IN B
26747 002002          SZA           CHECK FOR ERROR
26750 026632          JMP DCER        ;ERROR 13  POSSIBLE RETRY !!
26751 000265          ISZ LERR      ERROR 414 = TO DURING FILE MASK
                                        COMMAND
26752 104600          .JLB PHI.I    SKIP NEXT BYTE
26753 027507
26754 104600          .JLB PHI.I    READ DISC TYPE
26755 027507
26756 001300          RAR           ELIMINATE BIT ZERO
26757 027721          AND 017       USE 4 BITS FOR ID
26760 000260          STA TEMP      SAVE.DISC.TYPE

*
*      USE DISC TYPE TO CONVERT DISC PARAMETERS
*
26761 027766          LDB DCTYP     SET "DISC TYPE"
26762 000217          STB PNTR       POINTER
26763 000271          LDA DISC.ID   RETREIVE DISC TYPE
26764 000626          CPA 0406      MSC 9800L?
26765 027042          JMP DTYPE     YES
26766 000217          ISZ PNTR
26767 027730          CPA 0204      MINI-FLOPPY ?
26770 027042          JMP DTYPE
26771 027733          CPA 0404      sparrow
26772 027042          JMP DTYPE
26773 000217          ISZ PNTR
26774 027727          CPA 0201      88020 FLOPPY ?
26775 027042          JMP DTYPE
26776 000217          ISZ PNTR
26777 027712          CPA 01        7910 FIXED DISC ?
27000 027042          JMP DTYPE
27001 000217          ISZ PNTR
27002 027714          CPA 03        INTEGRATED DISC CONTROLLER?
27003 027013          JMP DC.ID     YES
27004 000205    DTYER STA SAVEB
27005 027763          LDA ..D460    DISC NOT IDENTIFIED
```

```
27006 000265        STA LERR        ERROR 460
27007 000274        LDB FILE        CHECK IF FILE NO. IS ZERO
27010 006002        SZB             IF SO THEN GO AHEAD
27011 026632        JMP DCER          ; ELSE, ERROR
27012 027026        JMP DCFM        USE CYLINDER MODE
*
27013 000260  DC.ID LDA TEMP        SAVE.DISC.TYPE
27014 027712        CPA 01          7920?
27015 027026        JMP DCFM        YES, DO FILE MASK FIRST
27016 000217        ISZ PNTR
27017 027714        CPA 03          7925?
27020 027026        JMP DCFM        YES, DO A FILE MASK FIRST
27021 000217        ISZ PNTR
27022 002002        SZA             7906?
27023 027004        JMP DTYER        ;NOT IDENTIFIED
27024 007400        CCB
27025 000272        STB UNIT.HEAD     ;FLAG TO INDICATE (UNIT = HEAD)
*
27026 104600  DCFM  .JLB PHI.TALK     PHI TALK
27027 027435
27030 000550        OCT 00550       SEND MASK TO 7906
*
27031 104600        .JLB PHI
27032 027475
27033 000017        OCT 17          SET FILE MASK
27034 027740        LDA 01005       ENABLE AUTO TRACK INCREMENT AND
                                      SPARING
27035 000272        LDB UNIT.HEAD
27036 006003        SZB,RSS         IS THIS A 7906?
27037 027713        IOR 02          NO THEN CYLINDER MODE
27040 104600        .JLB HPIB
27041 027521

*
*   CONVERT FILE NO. TO CYLINDER.HEAD.SECTOR
*
27042 104600  DTYPE .JLB DTPC       GO CALCULATE SEEK INFO FROM
27043 027045                          FILE NUMBER
27044 000566        JMP RDCIN,I
*
```

```
*
*
27045 000567  DTPC  STB RDTPC
27046 000217        LDA PNTR,I    GET NUMBER OF SECTORS PER TRACK
27047 027731        AND 0377
27050 003004        CMA,INA       MAKE IT NEGATIVE
27051 000276        STA SECTR.TRACK ; SAVE IT
27052 000217        LDA PNTR,I
27053 001727        ALF,ALF       SET NUMBER OF HEADS PER CYLINDER
27054 027721        AND 017
27055 003004        CMA,INA
27056 000275        STA HEAD.CYLINDER
27057 002400        CLA
27060 000274        LDB FILE      NOW GET NO SECTRS
27061 000260        STB TEMP
27062 000276        ADB SECTR.TRACK
27063 006020        SSB
27064 027067        JMP *+3
27065 002004        INA
27066 027061        JMP *-5
27067 000260        LDB TEMP      REMAINDER IS THE SECTOR OFFSET
27070 000276        STB SECTR.TRACK    ;SAVE IT
27071 000000        LDB A         NOW GET NUMBER OF CYLINDERS
27072 002400        CLA
27073 000260        STB TEMP
27074 000275        ADB HEAD.CYLINDER
27075 006020        SSB
27076 027101        JMP *+3
27077 002004        INA
27100 027073        JMP *-5
27101 000275        STA HEAD.CYLINDER ;SAVE CYLINDER
27102 000260        LDB TEMP      NOW ADD HEAD TO SECTOR WORD
27103 005727        BLF,BLF
27104 000276        ADB SECTR.TRACK
27105 000276        STB SECTR.TRACK ;SAVE
27106 000567        JMP RDTPC,I   ; NOW RETURN

*
*    SET SINGLE VECTOR
*
27107 000274  DC80  LDB FILE
27110 000277        STB VW1
27111 000275        LDB HEAD.CYLINDER
27112 000300        STB VW2
27113 000276        LDB SECTR.TRACK
27114 000301        STB VW3
27115 000267        LDB UNIT
```

```
27116 000010        SLA                     IF ODD UNIT
27117 006011        SLB,RSS                 AND LINUS TYPE
27120 027134        JMP DC80A               THEN USE LINUS NUMBERS
27121 000274  DC80. LDA FILE                LINUS TYPE
27122 000275        LDB HEAD.CYLINDER ; THEN DEVIDE BY
27123 101042        LSR 2             ; FOUR
27124 000277        STA VW1
27125 027753        LDA M350        160 SEC TIME OUT FIRST TIME FOR
                                         LONG LINUS TAPES
27126 000253        STA DCTO
27127 000275        LDA HEAD.CYLINDER
27130 000276        LDB SECTR.TRACK
27131 101042        LSR 2
27132 000300        STA VW2
27133 000301        STB VW3
27134 002404  DC80A CLA,INA           ; INDICATE CS80 TYPE
27135 000272        STA UNIT.HEAD
27136 000566        JMP RDCIN,I       ; RETURN

*
*  SEEK READ/WRITE DSJ
*
27137 000570  DC.RW STB RDCRW
27140 102623        OTA 23B       OUTPUT COUNT
27141 027764        LDA ..D415
27142 000265        STA LERR      ERROR 415 = TO DURING SEEK COMMAND
*
*
*    CHECK IF READ OR WRITE
*
27143 027665        LDA DMACW     GET DMA CONTROL WORD
27144 000503        LDB TEMPO     GET LBW CHAR
27145 027711        CPB W         WRITE?
27146 027726        XOR 0200      YES, CLEAR BIT 7
27147 102621        OTA 21B       OUTPUT TO DMA
27150 002400        CLA           SET ADDRESS TO ZERO
27151 102622        OTA 22B
27152 000272        LDB UNIT.HEAD    ;CHECK FOR CS 80
27153 004010        SLB
27154 006020        SSB
27155 027252        JMP DSEEK     NO, NOT CS 80
```

```
*
*     FOR CS 80  DO THE SPECIAL DANCE
*
27156 104600        .JLB PHI.L    PHI LISTEN
27157 027436
27160 000560        OCT 000560    SECONDARY (DSJ)
27161 104600        .JLB PHI
27162 027475
27163 001001  01001 OCT 001001    COUNTED TRANSFER OF ONE
27164 104600        .JLB PHI.I    GET IT BUT IGNORE IT
27165 027507
27166 104600        .JLB PHI.TALK
27167 027435
27170 000545        OCT 000545    COMMAND MESSAGE
27171 000267        LDA UNIT
27172 027735        IOR BIT5
27173 104600        .JLB HPIB     SEND SET UNIT
27174 027521
27175 027722        LDA 020
27176 104600        .JLB HPIB     SET ADDRESS
27177 027521
27200 000301        LDA VW3
27201 104600        .JLB HPIBX
27202 027557
27203 000300        LDA VW2
27204 104600        .JLB HPIBX
27205 027557
27206 000277        LDA VW1
27207 104600        .JLB HPIBX
27210 027557
27211 027724        LDA 076       SET STATUS MASK
27212 104600        .JLB HPIB
27213 027521
27214 027717        LDA 010       MESSAGE LENGTH
27215 104600        .JLB HPIBX
27216 027557
27217 002400        CLA
27220 104600        .JLB HPIBX
27221 027557
27222 002400        CLA
27223 104600        .JLB HPIBX
27224 027557
27225 003400        CCA           OVERRUN
27226 104600        .JLB HPIBX
27227 027557
*
```

```
27230 000265        ISZ LERR       ERROR 416 = TO DURING READ/WRITE
                                      COMMAND
27231 000503        LDB TEMPO      GET RW CHAR
27232 027711        CPB W          WRITE?
27233 027243        JMP DC.01      GO WRITE
27234 104600        .JLB PHI
27235 027475
27236 001000        OCT 001000     LOCATE > READ + EOI
*
27237 104600        .JLB PHI.L
27240 027436
27241 000556        OCT 000556     <EXECUTE>
27242 027331        JMP DS.01
*
27243 104600  DC.01 .JLB PHI
27244 027475
27245 001002        OCT 001002     LOCATE > WRITE + EOI
*
27246 104600        .JLB PHI.TALK
27247 027435
27250 000556        OCT 000556     <EXECUTE>
27251 027351        JMP DCOMN

*     SEEK    FOR NON CS80
*
27252 104600  DSEEK .JLB PHI.TALK       PHI TALK
27253 027435
27254 000550        OCT 000550
27255 104600        .JLB PHI1
27256 027475
27257 000002        OCT 000002          SEEK
27260 000272        LDB UNIT.HEAD
27261 000267        LDA UNIT            GET UNIT
27262 006020        SSB                 CHECK FOR UNIT HEAD SWAP
27263 002400        CLA                 YEP SWAP
27264 104600        .JLB HPIB           SEND TO THE CARD
27265 027521
27266 000275        LDA HEAD.CYLINDER ; SET UPPER CYLINDER
27267 000273        ADA CYLNDR.OFFSET     CYLINDER OFFSET
27270 104600        .JLB HPIBX
27271 027557
27272 000276        LDA SECTR.TRACK   ; SET HEAD
27273 001727        ALF,ALF
27274 027731        AND 0377
27275 000272        LDB UNIT.HEAD     ; CHECK FOR UNIT HEAD SWAP
27276 006020        SSB
27277 000267        LDB UNIT
27300 000001        IOR B
```

```
27301 104600          .JLB HPIB
27302 027521
27303 000276          LDA SECTR.TRACK    ; SET SECTOR
27304 027731          AND 0377
27305 027672          IOR BIT9
27306 104600          .JLB HPIB              SECTOR + EOI
27307 027521

*
*     READ OR WRITE
*
27310 000265          ISZ LERR        ERROR 416 = TO DURING READ/WRITE
                                          COMMAND
27311 104600          .JLB PHI.TALK       PHI TALK
27312 027435
27313 000550          OCT 000550
27314 000503          LDB TEMPO       CHECK READ OR WRITE
27315 027711          CPB W
27316 027337          JMP DWRT         NOPE
27317 104600          .JLB PHI1
27320 027475
27321 000005          OCT 000005      READ
27322 000267          LDA UNIT        GET UNIT
27323 027672          IOR BIT9         ADD EOI
27324 104600          .JLB HPIB        SEND IT TO THE CARD
27325 027521
27326 104600          .JLB PHI.L       PHI LISTEN
27327 027436
27330 000540          OCT 000540      SECONDARY
27331 027744   DS.01 LDA M2
27332 104600          .JLB PHIN
27333 027476
27334 001400          OCT 001400      UNCOUNTED TRANSFER
27335 060040          OCT 060040      TELL PHI TO INPUT
27336 027351          JMP DCOMN
*
27337 104600   DWRT  .JLB PHI1
27340 027475
27341 000010          OCT 000010      WRITE
27342 000267          LDA UNIT        GET UNIT
27343 027672          IOR BIT9         ADD EOI
27344 104600          .JLB HPIB        OUTPUT TO THE CARD
27345 027521
27346 104600          .JLB PHI.TALK
27347 027435
27350 000540          OCT 000540      WRITE
```

```
04390*
04391*     COMMON DMA ROUTINE
04392*
04393  27351 027666  DCOMN LDA CMDF       SET PHI FOR BYTE PACKED DMA
04394  27352 000265        ISZ LERR       ERROR 417 = TO DURING DATA READ
04395  27353 000503        LDB TEMPO      CHECK READ OR WRITE
04396  27354 027711        CPB W          WRITE??
04397  27355 001665        ELA,CLE,ERA     YES, CLEAR THE MSB
04398  27356 102631        OTA CMND       SEND TO THE PHI
04399  27357 103721        STC 21B,C     START DMA
04400  27360 002400        CLA
04401  27361 000253        LDB DCTO        LONG TIME OUT
04402*                                  START
04403  27362 101117  DC.NO RRR 15         DELAY WITHOUT MEMORY ACCESS
04404  27363 100117        RRL 15
04405  27364 102223        SFC 23B         DONE ?
04406  27365 027400        JMP DC.N1         YEP
04407  27366 101117        RRR 15
04408  27367 100117        RRL 15
04409  27370 000000        ISZ A         WAIT
04410  27371 027362        JMP DC.NO     GO WAIT SOME MORE
04411  27372 101117        RRR 15
04412  27373 100117        RRL 15
04413  27374 000001        ISZ B         TIMED OUT?
04414  27375 027362        JMP DC.NO     NO. GO WAIT
04415  27376 107721        CLC 21B,C     STOP DMA
04416  27377 027434        JMP DCRWE      TIMED OUT
04417*
04418  27400 107721  DC.N1 CLC 21B,C      KILL ANY ADDITIONAL DMA
04419  27401 027765        LDA ..D420
04420  27402 000265        STA LERR       ERROR 420 = PARITY ERROR
04421  27403 102222        SFC 22B        CHECK FOR PARITY ERROR
04422  27404 027434        JMP DCRWE       YEP, BAIL OUT
04423  27405 000265        ISZ LERR       ERROR 421 = TO DURING PHI FLUSH
04424  27406 027445        LDA UNL        GET UNLISTEN
04425  27407 000503        LDB TEMPO      READ OR WRITE??
04426  27410 027711        CPB W
04427  27411 027415        JMP DC.N2      YES, FLUSH FIFO
04428  27412 104600        .JLB PHIFL     FLUSH FIFO FOR READ
       27413 027535
04429  27414 027417        JMP .DSJ
04430*
04431  27415 104600  DC.N2 .JLB HPIB       WRITE SO OUTPUT UNL
       27416 027521
04432*
```

```
*     DSJ REQUEST
*
27417 000265  .DSJ  ISZ LERR      ERROR 422 = TIME OUT DURING DSJ
27420 104600        .JLB PHI.L     PHI LISTEN
27421 027436
27422 000560        OCT 000560    SECONDARY DSJ
27423 104600        .JLB PHI1
27424 027475
27425 001001        OCT 001001    COUNTED TRANSFER OF 1
27426 104600        .JLB PHI.I
27427 027507
27430 000205        STA SAVEB     SAVE DSJ ERROR CODE
27431 000265        ISZ LERR      ERROR 423 = BAD DSJ STATUS
27432 002003        SZA,RSS       WAS THERE AN ERROR ?
27433 000570        ISZ RDCRW     NO, TAKE GOOD EXIT
27434 000570  DCRWE JMP RDCRW,I   YES, ERROR RETURN

*
*
*     PHI SERVICE ROUTINES
*
*
*  PHI TALK AND PHI LISTEN SEND OUT TALK AND LISTEN COMMANDS
*  RESPECTIVELY TO THE SUBCHANNEL ADDRESED IN SUBCH.  THE WORD AFTER
*  THE JLB PHI... IS THE SECONDARY.
*
27435 002301  PHI.TALK CCE,RSS
27436 000040  PHI.L    CLE
27437 000560           STB RPHI?
27440 027745           LDA M3       SET COUNT
27441 104600        .JLB PHIN       "PHIN"
27442 027476
27443 031002        OCT 031002    PHI OUTPUT COMMAND
27444 000537        OCT 000537    UNT
27445 000477  UNL   OCT 000477    UNL
27446 002041        SEZ,RSS
27447 027461         JMP LISEN
27450 104600        .JLB PHI1
27451 027475
27452 000536        OCT 000536    CTLR LSN
27453 027752        LDA M100
27454 000000        ISZ A         KLUDGE TO MAKE MINIFLOPPY WORK
27455 027454        JMP *-1
27456 000270        LDA SUBCH     GET DISC ADDRESS
27457 027670        IOR LSN        MERGE LISTEN BIT
27460 027466        JMP PCOMN
*
```

```
27461 104600  LISEN .JLB PHI1
27462 027475
27463 000476        OCT 000476    CTLR LSN
27464 000270        LDA SUBCH     GET DISC ADDRESS
27465 027667        IOR TLK        MERGE TALK BIT
27466 104600  PCOMN .JLB HPIB       SEND TO CARD
27467 027521
27470 000560        LDA RPHI?,I   GET DATA
27471 104600        .JLB HPIB      SEND TO THE CARD
27472 027521
27473 000560        ISZ RPHI?     BUMP RETURN ADDRESS
27474 000560        JMP RPHI?,I   SPLIT
*
*  THIS ROUTINE UNDER ALL ITS MANY NAMES OUTPUTS ONE OR MORE WORDS TO
*  THE PHI CHIP.
*
      027475  PHI1  EQU *
27475 003400  PHI   CCA           SET FOR ONE CONTROL WORD
27476 000561  PHIN  STB RPHI      SAVE RETURN ADDRESS
27477 000223        STA CTR       SET CONTROL WORD COUNTER
27500 000561  PH    LDA RPHI,I    FETCH A WORD
27501 102630        OTA DATA      SEND IT TO THE CARD
27502 103730        STC DATA,C    PASS IT TO THE PHI
27503 000561        ISZ RPHI      MOVE POINTER
27504 000223        ISZ CTR       DONE ?
27505 027500        JMP PH         NO, TRY AGAIN
27506 000561        JMP RPHI,I     YES, BYE BYE
*
*  THIS ROUTINE INPUTS A WORD FROM THE PHI CHIP.
*
27507 000562  PHI.I STB RPHII     SAVE RETURN ADDRESS
27510 027546        LDA PIN       GET INPUT COMMAND
27511 104600        .JLB HPIB      SEND IT TO THE CARD
27512 027521
27513 104600        .JLB PHI1
27514 027475
27515 100000        OCT 100000    TELL CARD TO INPUT
27516 102530        LIA DATA      FETCH DATA
27517 027731        AND 0377      MASK OFF UPPER BYTE
27520 000562        JMP RPHII,I   RETURN
```

```
*
*  THIS ROUTINE OUTPUTS A WORD TO THE PHI CHIP AND WAITS FOR IT TO BE
*  SENT OUT TO THE BUS.  IF IT TAKES TOO LONG A TIMEOUT OCCURS
*  AND THE DISC LOAD IS TERMINATED WITHOUT FURTHER RETRIES
*
 27521 000563  HPIB  STB RHPIB     SAVE RETURN ADDRESS
 27522 102630        OTA DATA      OUTPUT DATA
 27523 103730        STC DATA,C    START THE OUTPUT
 27524 027755        LDB M5600     PROCESSOR INDEPENDENT TIMEOUT 7
                                      SECONDS FOR CS80
 27525 000245  HPIBLP LDA TBGCNT
 27526 002306        CCE,INA,SZA     WAIT 1.25 MS
 27527 027526        JMP *-1
 27530 102230        SFC DATA      FLAG 30 INDICATES FIFO EMPTY
 27531 000563        JMP RHPIB,I   RETURN WHEN FLAG SET
 27532 000001        ISZ B         DONE WITH TIME OUT?
 27533 027525        JMP HPIBLP    NO, GO AROUND AGAIN
 27534 026632        JMP DCER      ERROR, TIME OUT
*
*
 27535 000564  PHIFL STB RPHIF     SAVE RETURN ADDRESS
 27536 027666        LDA CMDF      ENABLE
 27537 102631        OTA CMND       FLAG
 27540 027746        LDA M4        SET CONTROL WORD COUNT
 27541 104600        .JLB PHIN
 27542 027476
 27543 060043        OCT 060043    FLUSH OUTBOUND FIFO
 27544 031002        OCT 031002    PHI OUTPUT COMMAND
 27545 000537        OCT 000537    TELL DISC TO SHUT UP
 27546 031004  PIN   OCT 031004    SET FLAG WHEN FIFO HAS DATA
 27547 027666        LDA CMDF      ENABLE
 27550 102631        OTA CMND       FLAG
 27551 027752        LDA M100      SET MAXIMUM LOOP
 27552 002006        INA,SZA
 27553 102330        SFS DATA      ANY DATA ?
 27554 000564        JMP RPHIF,I    NO, EXIT
 27555 103730        STC DATA,C     YES, EMPTY IT
 27556 027552        JMP *-4         TRY AGAIN
*
```

```
*      OUTPUT 2 BYTES TO THE HPIB CARD
*
  27557 000565  HPIBX STB RHPIBX    SAVE RETURN ADDRESS
  27560 000257        STA HPIT      SAVE DATA
  27561 001727        ALF,ALF
  27562 027731        AND 0377
  27563 104600        .JLB HPIB
  27564 027521
  27565 000257        LDA HPIT      GET LOW BYTE
  27566 027731        AND 0377
  27567 104600        .JLB HPIB
  27570 027521
  27571 000565        JMP RHPIBX,I
*
*
* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
*
*    SCNSC   SCANS THE SELECT CODE ETC FROM THE STRING INTO
*           THE A REGISTER. IT SKIPS IF THERE IS A NUMBER IN THE
*           STRING.
*           IT LEAVES STORE.POINTER WITH THE BYTE ADDRESS OF THE
*           FIRST CHAR AFTER THE NUMBER
*
  27572 000545  SCNSC STB RSCNSC        SAVE RETURN ADDRESS
  27573 000264        STA SCETC         SAVE DEFAULT VALUE
  27574 002400        CLA
  27575 000274        STA FILE      FILE ZERO IF NO NUMBER
  27576 000260        STA TEMP
  27577 027776        LDB ...SPTR         POINT AT START OF STRING
  27600 027713        ADB 02            POINT AT FIRST WORD OF SCETC
  27601 005200        RBL               MULT BY 2 TO MAKE BYTE ADDRESS
  27602 000360        STB STORE.POINTER SAVE POINTER TO REST OF STRING
  27603 000360  SCNLP LDB STORE.POINTER  GET BYTE ADDR OF NEXT DIGIT
  27604 105763        LBT
  27605 105762        JLY ISDIG         IS IT A DIGIT??
  27606 027632
  27607 027620        JMP SCNDN         NO, DONE
  27610 027723        XOR 060           MAKE DIGIT BINARY
  27611 000260        ADA TEMP
  27612 000274        LDB FILE      SECOND WORD OF TWO WORD NUMBER
  27613 100043        LSL 3             MULT BY 8
  27614 000260        STA TEMP
  27615 000274        STB FILE      SAVE 2ND WORD
  27616 000360        ISZ STORE.POINTER  NEXT BYTE
  27617 027603        JMP SCNLP         GO DO NEXT BYTE
*
```

```
27620 000260  SCNDN LDA TEMP
27621 000274        LDB FILE      GET TWO WORD QUANT.
27622 100041        LSL 1         SHIFT FILE NUMBER TO SECOND WORD
27623 000274        STB FILE      SAVE IT
27624 000207        STB SAVEX     PASS FILE NUMBER IN X REGISTER
27625 006400        CLB
27626 101044        LSR 4         PUT REST OF STUFF IN RIGHT PLACE
27627 002002        SZA
27630 000264        STA SCETC     SAVE IT
27631 000545        JMP RSCNSC,I     RETURN
*     ISDIG CHECKS THE CHAR IN A AGAINST RANGE ZERO TO 7 AND
*     SKIPS IF IT IS IN RANGE.DOES NOT CHANGE A OR B
*
27632 000261  ISDIG STA CHAR          SAVE CHARACTER
27633 027750        ADA M48           CHECK AGAINST ZERO
27634 002020        SSA
27635 027644        JMP ISDIGDN       NOT A DIGIT
*
27636 027747        ADA M8            CHECK AGAINST 8
27637 002021        SSA,RSS
27640 027644        JMP ISDIGDN       NO GOOD
*
27641 000261        LDA CHAR
27642 105772        JPY 1             RETURN AND SKIP
27643 000001
*
27644 000261  ISDIGDN LDA CHAR        RESTORE A REG
27645 105772        JPY 0             RETURN AND DONT SKIP
27646 000000
*

*
27647 001722  STMAP ALF,RAL      *32
27650 105745        LDX .N40      32 ENTRIES
27651 021754
27652 027662        LDB .MBUF     BUFFER ADDRESS
27653 000001        STA B,I       PUT ENTRY IN MAP BUFFER
27654 002004        INA
27655 006004        INB
27656 105760        ISX           ISZ X REG.
27657 027653        JMP *-4
27660               LMAP
27661 021706        DEF .DO       TO VALUES CONTAINED
27662 000370  .MBUF DEF MPBUF
27663 105772        JPY 0          RETURN
27664 000000
*
```

```
04634*
04635*     CONSTANTS AND STUFF LIKE THAT
04636*
04637  27665 060200  DMACW OCT 060200
04638  27666 103004  CMDF  OCT 103004
04639  27667 000500  TLK   OCT 000500
04640  27670 000440  LSN   OCT 000440
04641  27671 002400  .ICW  OCT 002400
04642  27672 001000  .OCW  OCT 001000
04643  27673 017015  CTRS  OCT 017015
04644  27674 041421  CDC1  OCT 41421
04645  27675 051021  RDC1  OCT 51021
04646  27676 015446  ECSAND  OCT 15446
04647  27677 070060  .P0   OCT 70060
04648  27700 062061  .$D1  OCT 62061
04649  27701 031464  ASC34 ASC 1,34
04650  27702 053405  WENQ  OCT 53405
04651  27703 070062  .P2   OCT 70062
04652  27704 071462  .S2   OCT 71462
04653  27705 072460  .U0   OCT 72460
04654  27706 000021  .DC1  OCT 000021
04655  27707 000122  R     OCT 122
04656  27710 000123  S     OCT 123
04657  27711 000127  W     OCT 127
04658  27712 000001  O1    OCT 000001
04659  27713 000002  O2    OCT 000002
04660  27714 000003  O3    OCT 000003
04661  27715 000006  O6    OCT 000006
04662  27716 000007  O7    OCT 000007
04663  27717 000010  O10   OCT 000010
04664  27720 000012  O12   OCT 000012
04665  27721 000017  O17   OCT 000017
04666  27722 000020  O20   OCT 000020
04667        027706  O21   EQU .DC1
04668  27723 000060  O60   OCT 000060
04669  27724 000076  O76   OCT 000076
04670  27725 000077  O77   OCT 000077
04671  27726 000200  O200  OCT 000200
04672  27727 000201  O201  OCT 000201
04673  27730 000204  O204  OCT 000204
04674  27731 000377  O377  OCT 000377
04675  27732 000400  O400  OCT 000400
04676  27733 000404  O404  OCT 000404
04677  27734 000406  O406  OCT 000406
04678  27735 000040  BIT5  OCT 000040
04679        027672  BIT9  EQU .OCW
04680        027672  O1000 EQU BIT9
04681  27736 001100  O1100 OCT 001100
```

```
04682  27737 001101  01101 OCT 001101
04683  27740 001005  01005 OCT 001005
04684  27741 007777  07777 OCT 007777
04685  27742 100000  0100000 OCT 100000
04686  27743 177777  .M1    DEC -1
04687  27744 177776  M2    DEC -2
04688  27745 177775  M3    DEC -3
04689  27746 177774  M4    DEC -4
04690  27747 177770  M8    DEC -8
04691  27750 177720  M48   DEC -48
04692  27751 177700  M64   DEC -64
04693  27752 177634  M100  DEC -100
04694  27753 177242  M350  DEC -350
04695  27754 174700  M1600 DEC -1600
04696  27755 165040  M5600 DEC -5600
04697  27756 000156  ..D110 DEC 110
04698  27757 000170  ..D120 DEC 120
04699  27760 000633  ..D411 DEC 411
04700  27761 000634  ..D412 DEC 412
04701  27762 000323  ..D211 DEC 211
04702  27763 000714  ..D460 DEC 460
04703  27764 000637  ..D415 DEC 415
04704  27765 000644  ..D420 DEC 420
04705  27766 027767  DCTYP DEF *+1       HEADS-CYL/SECTORS-TRACK
04706  27767 002037        OCT 002037        4/31  MSC9800L
04707  27770 001020        OCT 001020        2/16  MINI-FLOPPY
04708  27771 001036        OCT 001036        2/30  88010-20
04709  27772 001040        OCT 001040        2/32  7910
04710  27773 002460        OCT 002460        5/48  7920
04711  27774 004500        OCT 004500        9/64  7925
04712  27775 000460        OCT 000460        1/48  7906
04713*
04714  27776 000306  ...SPTR DEF STRNG
04715*
04716        027777  EOP3 EQU *
04717                      END
```

Lines where ORG command appeared:

42
71
264
268
273
1457
2551
3526

```
* - Volatile reference (store, jump, call...)

.$D1 . . . . . . . . 4648:  3731
.% . . . . . . . . . 2459:  1663
...CR  . . . . . . . 2573:  3158   3181
...SPTR  . . . . . . 4714:  4573
...W . . . . . . . . 2574:  3230
..?  . . . . . . . . 2575:  Symbol not referenced
..B  . . . . . . . . 2558:  2618   2650   2681
..B1777  . . . . . . 2465:  1504   2091
..B377 . . . . . . . 2464:  1472   1476   2044   2052   2250   2264
..B77777 . . . . . . 2466:  2322
..BEL  . . . . . . . 2567:  3116
..BKS  . . . . . . . 2557:  3110   3179
..D110 . . . . . . . 4697:  3617
..D120 . . . . . . . 4698:  3767
..D211 . . . . . . . 4701:  3858
..D411 . . . . . . . 4699:  4048
..D412 . . . . . . . 4700:  Symbol not referenced
..D415 . . . . . . . 4703:  4265
..D420 . . . . . . . 4704:  4419
..D460 . . . . . . . 4702:  4159
..DEL  . . . . . . . 2560:  2582*  3112   3183
..DG1  . . . . . . . 2615:  2781   3092
..ENT  . . . . . . . 1446:  1117
..MBUF . . . . . . . .714:   716
..MRBT . . . . . . . 3931:  3942*
..N40  . . . . . . . 2592:  2740   2751
..NEXT . . . . . . . 2572:  2652*
..RUN  . . . . . . . 2571:  2651*
..USER . . . . . . . 1168:  1145*
.2 . . . . . . . . . 2461:  1927   1949
.3 . . . . . . . . . 2462:  1929   1951
.? . . . . . . . . . 2463:  1659
.A . . . . . . . . . 2471:  1687
.AGAIN . . . . . . . 2563:  Symbol not referenced
.B . . . . . . . . . 2473:  1685   2258
.B1  . . . . . . . . 2577:  2822   3200   3220
.B10 . . . . . . . . 2499:  1578
.B100  . . . . . . . 2502:  1979
.B101  . . . . . . . 2581:  Symbol not referenced
.B17 . . . . . . . . 2579:  Symbol not referenced
.B177  . . . . . . . 2582:  Symbol not referenced
.B20 . . . . . . . . 2498:  2409
.B24 . . . . . . . . 2580:  Symbol not referenced
.B37 . . . . . . . . 1402:  1350   1363
.B377  . . . . . . . 2583:  2911   2921   3007   3057   3340   3348   3370
.B60K  . . . . . . . 2584:  2924   3371
```

```
.B7 . . . . . . . . 2578:  2840
.BLR . . . . . . . . 2586:  Symbol not referenced
.BOOT? . . . . . . . 2503:  2414*  2425*  2433*  2439*
.BTERR . . . . . . . 2559:  2680*
.C . . . . . . . . . 2474:  1913   2274
.CIR . . . . . . . . 2010:  1914*
.CKSM . . . . . . . 3706:  Symbol not referenced
.COMND . . . . . . . 2564:  3113*  3184*
.CR . . . . . . . . 2457:  1657   1781   1844   1895   2118   2215
.CT . . . . . . . . 2467:  2399
.CTLT . . . . . . . 2458:  Symbol not referenced
.CTU . . . . . . . . 2409:  2400*
.D . . . . . . . . . 2475:  1767   1787   1945   2202   2220
.D0 . . . . . . . . 1390:   516    710    713    796    854    888   1051
                           1166   4629
.D10 . . . . . . . . 2601:  2786
.D16 . . . . . . . . 2602:  Symbol not referenced
.D2 . . . . . . . . 2600:  2624
.D310 . . . . . . . 2608:  3225
.D311 . . . . . . . 2610:  3266
.D312 . . . . . . . 2609:  3234
.D314 . . . . . . . 2611:  3273
.D315 . . . . . . . 2613:  3310
.D317 . . . . . . . 2614:  3322
.D32 . . . . . . . . 2603:  2765   2997
.D320 . . . . . . . 2612:  3331
.D40 . . . . . . . . 2604:  Symbol not referenced
.D64 . . . . . . . . 2605:  3191
.D91 . . . . . . . . 2607:  2998
.D97 . . . . . . . . 2606:  3002
.DC . . . . . . . . 2469:  2403
.DC1 . . . . . . . . 4654:  3669   4667*
.DCSC . . . . . . . 3934:  3939
.DEL . . . . . . . . 2472:  1893   1894   1919
.DIAG . . . . . . . 2041:  1946*
.DIG1 . . . . . . . 2519:  Symbol not referenced
.DISC . . . . . . . 2436:  2404*
.DISTS . . . . . . . 2430:  2406*
.DS . . . . . . . . 2468:  2405
.DSJ . . . . . . . . 4435:  4429*
.DSSC . . . . . . . 1387:  1191
.E . . . . . . . . . 2476:  1691   2268
.ENQ . . . . . . . . 2561:  2769
.ENQAK . . . . . . . 2757:  1464*  1526   1889*  2166*  2753*
.ENQAS . . . . . . . 2763:  2759*
.ENT . . . . . . . . 1538:  Symbol not referenced
.ENTI . . . . . . . 2456:  1573
.EX . . . . . . . . 2340:  2269*
```

```
.F . . . . . . . . . 2477:  1947
.FLAGS . . . . . . . 2018:  1948*
.G . . . . . . . . . 2478:  1683
.HELP  . . . . . . . 1734:  1660*
.I . . . . . . . . . 2479:  1695   1915
.ICW . . . . . . . . 4641:  3784
.L . . . . . . . . . 2480:  1671   2254
.LCH1  . . . . . . . 1892:  1877*  1879
.LCLP  . . . . . . . 1875:  1882*
.LDER  . . . . . . . 2427:  1487   2442
.LIA . . . . . . . . 2520:  1999   2045   2053
.LIST  . . . . . . . 1838:  1672*
.LLP . . . . . . . . 1861:  1890*
.LLP2  . . . . . . . 1865:  1872*
.LOAD  . . . . . . . 2395:  2255*  2257*  2259*
.M . . . . . . . . . 2481:  1665   1921
.M1  . . . . . . . . 4686:  3998
.MAPS  . . . . . . . 2127:  1922*
.MASK  . . . . . . . 2079:  1916*
.MBUF  . . . . . . . 4630:  4622
.MELO  . . . . . . . .546:   562*
.MRBT  . . . . . . . 1198:  1186*  1196*
.MREG  . . . . . . . 1802:  1666*
.N . . . . . . . . . 2482:  1769   1785   2200   2218
.N1  . . . . . . . . 2585:  2797   3126   3129   3203   3206
.N10 . . . . . . . . 2591:  Symbol not referenced
.N2  . . . . . . . . 1426:   369
.N20 . . . . . . . . 1427:   945   1248
.N26 . . . . . . . . 2595:  2995
.N27 . . . . . . . . 2594:  Symbol not referenced
.N32000  . . . . . . 2596:  2936
.N40 . . . . . . . . 1428:  1286   4621
.N48 . . . . . . . . 2593:  3099
.N5  . . . . . . . . 2587:  2826
.N6  . . . . . . . . 2588:  3089
.N65 . . . . . . . . 2597:  Symbol not referenced
.N7  . . . . . . . . 2589:  Symbol not referenced
.N8  . . . . . . . . 2590:  Symbol not referenced
.N91 . . . . . . . . 2599:  Symbol not referenced
.N97 . . . . . . . . 2598:  2992
.O . . . . . . . . . 2483:  1693
.OCW . . . . . . . . 4642:  3794   4679*
.OUTIT . . . . . . . 2014:  1722*  1825*  2039*  2061*  2075*  2083*  2092*
                     2096*  2100*
.P . . . . . . . . . 2484:  1689   1923   2144   2276
.P0  . . . . . . . . 4647:  3620
.P2  . . . . . . . . 4651:  3639
.PAR . . . . . . . . 2086:  1924*
```

```
.PRSET . . . . . . . 2562:   2906*   3052*
.PSET  . . . . . . . 1332:   1116*   1587*   2291*   2390*   2395*   2674*
.PTDC  . . . . . . . 1189:   1173*
.PTLER . . . . . . . 3932:   3952*
.PU  . . . . . . . . .196:   3622*   3628    3655    3729
.Q . . . . . . . . . 2485:   1677
.R . . . . . . . . . 2486:   1625    1669    2270
.REGS  . . . . . . . 1908:   1670*
.RENT  . . . . . . . 1537:   1574*
.RM  . . . . . . . . 2470:   2401
.RMSC  . . . . . . . 1388:   1183
.ROM . . . . . . . . 2419:   2402*
.RTRN  . . . . . . . 2521:   1596
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.SPTR  . . . . . . . 3168:   2620    2638    2639    3175
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                       748    749    750     755     756     811     816     820
                       825    829    871     872     876     877     893     896
                       951    974    1016*   1070*   1249*   1291*   1352    1365
                      1572   1704    2135    2262    2398    2634    2641    2646
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TEMPO	.181:	766*	780	785*	832	923*	937*	938*
	943*	949	953	1002*	1003	1012	1067	1071*
	1086*	1100*	1104	1234	1653*	2003*	2005	2048*
	2058	2251*	2267	2419	2619*	2649	2685*	3229
	3649	4272	4316	4366	4395	4425		

```
TEMP1 . . . . . . . .180:   925*   948    973    995    1001   1085   2056*
                    2060   3633*  3636   3680*  3696   3697*  3703   3747*
                    3751   3752*  3757
TEMP2 . . . . . . . .179:   1088*  1105*  3613*  3670*  3710   3722*  3724
                    3759*
TEMP3 . . . . . . . .182:   3355*  3358
TFLAG . . . . . . . .164:   Symbol not referenced
TG.BF . . . . . . . 2981:   1655*  1706   1762*  1806   1973*  2105*  2193
TG.TB . . . . . . . 2972:   2760*
TLK . . . . . . . . 4639:   4074   4478
TMESS . . . . . . . 2535:   1755
TRAPFLAG . . . . . .154:    920*  1120
TRYCT . . . . . . . .125:   3937*  3949*
TRYNM . . . . . . . 3933:   3936
UIJMPI . . . . . . . .115:   601*
UIT . . . . . . . . .116:    115*   581*  1384*
UIT1 . . . . . . . . 1386:   580
UITINT . . . . . . . 1348:   1386
UITJMP . . . . . . . 1384:   600
UITJSB . . . . . . . 1385:   598
UITRTN . . . . . . . .114:   1354*  1385*
UNIT . . . . . . . . .139:   2663*  3619*  3621   3837*  4112   4241   4293
                    4340   4352   4371   4384
UNIT.HEAD . . . . . .142:   4065*  4176*  4184   4257*  4278   4339   4350
UNL . . . . . . . . 4463:   4424
VCP.FLAG . . . . . . .190:   681*  1108*  1208   1266
VCPDS . . . . . . . 2908:   2904
VCPEX . . . . . . . 2368:   2364
VCPL . . . . . . . . .665:   678*
VCPL1 . . . . . . . .680:   670*
VCPSC . . . . . . . .191:   682*  2895
VCPTFLG . . . . . . .153:   293*   539    564*   701    1127   1507   2389*
VERMG . . . . . . . 2528:   1511
VFP . . . . . . . . 1463:   1216
VFP.0 . . . . . . . 1492:   1467*  1483*
VFP.1 . . . . . . . 1507:   1494*
VW1 . . . . . . . . .147:   4236*  4248*  4302
VW2 . . . . . . . . .148:   4238*  4254*  4300
VW3 . . . . . . . . .149:   4240*  4255*  4298
W . . . . . . . . . 4657:   3650   4273   4317   4367   4396   4426
WENQ . . . . . . . . 4650:   3735
WMAP . . . . . . . . . 46:   1562
XEQT . . . . . . . . .201:   203*  1597*  1978   1980*  1983*  1989   2001*
                    2002*  2046*  2047*  2054*  2055*  2521*
ZERO . . . . . . . . 2460:   1935   1991
Macro:  No  errors total
```

B.1 INTRODUCTION

There are two power supplies used with the A-Series Computers. A 440-watt supply is for the 20-slot backplane and a 300-watt supply is for the 16-slot backplane. Both supplies are modules that plug into the back (circuit trace side) of the appropriate backplane. The A-Series supplies are considered non-repairable in the field and, in case of failure, the entire unit should be replaced with an exchange unit from Hewlett-Packard and the original unit returned for repair.

This section of the manual provides information required to evaluate the supply's performance. Included are an overall operating description, control signal descriptions, mechanical and electrical specifications. Located at the back of this section are parts location diagrams (assembly drawings), parts lists, and schematics.

This section is divided into several main parts. The paragraphs under subheading B.2 cover the 440-watt supply, Part No. 0950-1671; the paragraphs under subheading B.3 cover the Micro/1000 300-watt supply, Part No. 0950-1646, the paragraphs under subheading B.4 cover the HP 12154A battery backup module for Micro/1000 systems, the paragraphs under subheading B.5 cover the HP 12159A 25 kHz module for Micro/1000 systems, and under subheading B.6 applications of the 25 kHz power are discussed.

B.2 440-WATT SUPPLY

The 440-watt supply, Part No. 0950-1671, is used with the 20-slot backplane. The supply operates from either 115 Vac or 230 Vac. There are four fans for cooling the power supply and the computer. The fans plug into either connector P7 for 115 Vac operation or into P8 for 230 Vac operation.

The supply has four dc outputs at +5V, +5V memory backup (+5M), +12V, and -12V. It also provides 25 kHz ac power that is used as a power source for certain I/O cards. The +5M battery backup (BB) and the 25 kHz ac outputs are optional and are provided by separate cards that plug into the supply. If the battery backup is not installed, a jumper card must be placed in the BB connector of the supply. A block diagram of the 440-watt supply is shown in Figure B-1.

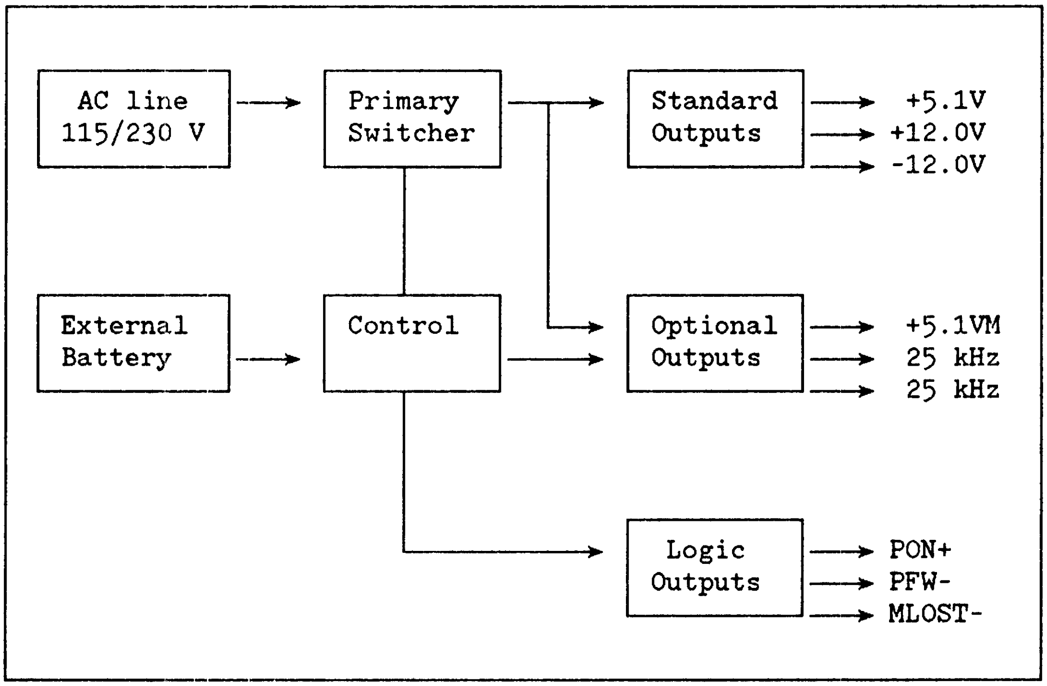

Figure B-1. 440-Watt Power Supply Block Diagram

B.2.1 LOGICAL SIGNALS

The power supply provides logical control signals to the computer to indicate power availability so that appropriate action can be taken.

B.2.1.1 PON+

PON+ is a signal that indicates the condition of the dc outputs. When the outputs are within specification, PON+ will be 2.4V to 5.2V. When the outputs are outside of specification, PON+ will be 0.2V plus or minus 0.2V. This definition includes the time when ac power is not applied (i.e., when ac power is down, the PON+ signal should be the out-of-specification condition.)

B.2.1.2 PFW-

The PFW- signal indicates the condition of ac power into the supply. When the input line voltage is above the "power fail trip point", PFW- is 2.4V to 5.2V. When the input line voltage is below the "power fail trip point", PFW- is 0.2V plus or minus 0.2V.

B.2.1.3 MLOST-

The MLOST- indicates the condition of the memory backup voltage as the main supply is being powered up. At all other times this signal is of no importance to the system. MLOST- is a pulse that is valid for 1 millisecond before and 5 millisecond after the rising edge of PON+. The MLOST- pulse during power up will be 2.4V to 5.2V if the memory supplies were within specification during the last power down. If the memory supplies are not within specification, MLOST- will be 0.2V plus or minus 0.2V.

B.2.2 MECHANICAL SPECIFICATIONS (440W Supply)

The overall mechanical dimensions and connector locations of the 0950-1671 supply are shown in Figure B-2. The connector specifications are given in Table B-1.

The cooling air flow should be a minimum of 70 CFM of air flowing across the power board in the direction indicated in Figure B-2. Power supply assembly diagrams are provided at the rear of this section of the manual.

Table B-1. Connector Specifications (440W Supply)

CONNECTOR	AMP PART NO.	AMP MATING NO.
P1/P3	Edge Card	
P2/P4	Edge Card	
P5	9-350255-2	350240
P6	9-350264-2	350243
P7	207584-1	207396-1
P8	207584-1	207396-1
P9	207365-1	207360-1

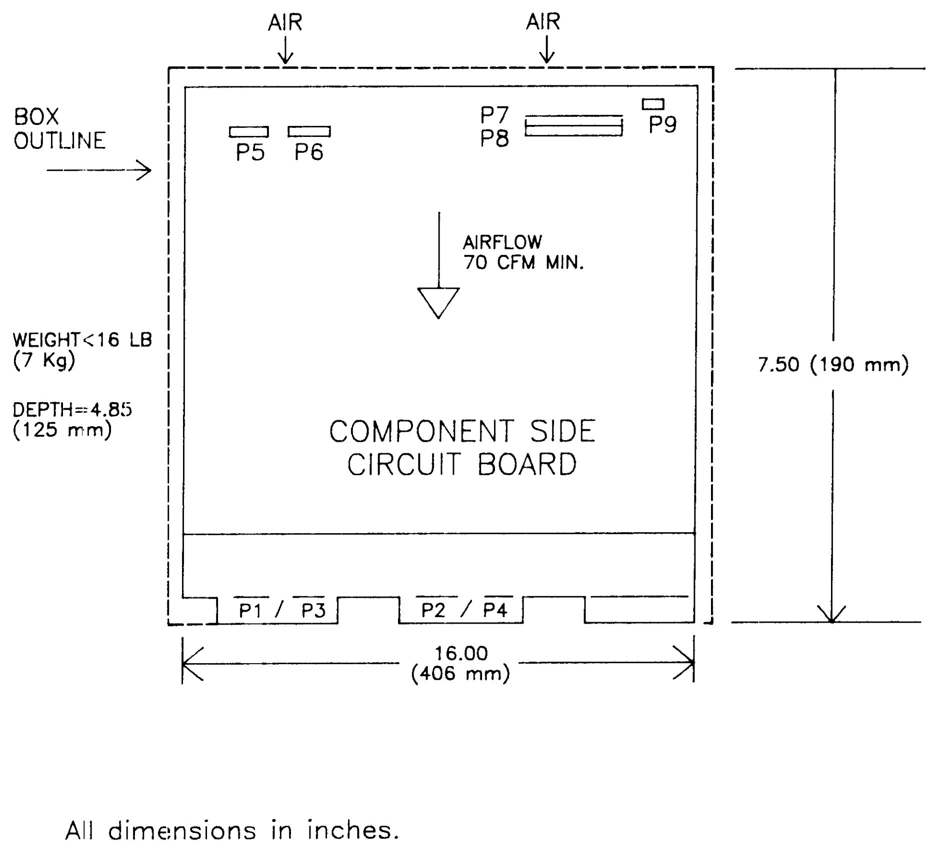

Figure B-2. Dimensions and Connector Locations (440W Supply)

B.2.3 ELECTRICAL CONNECTIONS (440W Supply)

The electrical contacts for the 440-watt power supply are provided by nine connectors. Two of these are edge-card connectors that plug into the backplane. A power supply connector diagram is shown in Figure B-3, and the electrical connector pin definitions are given in Table B-2.

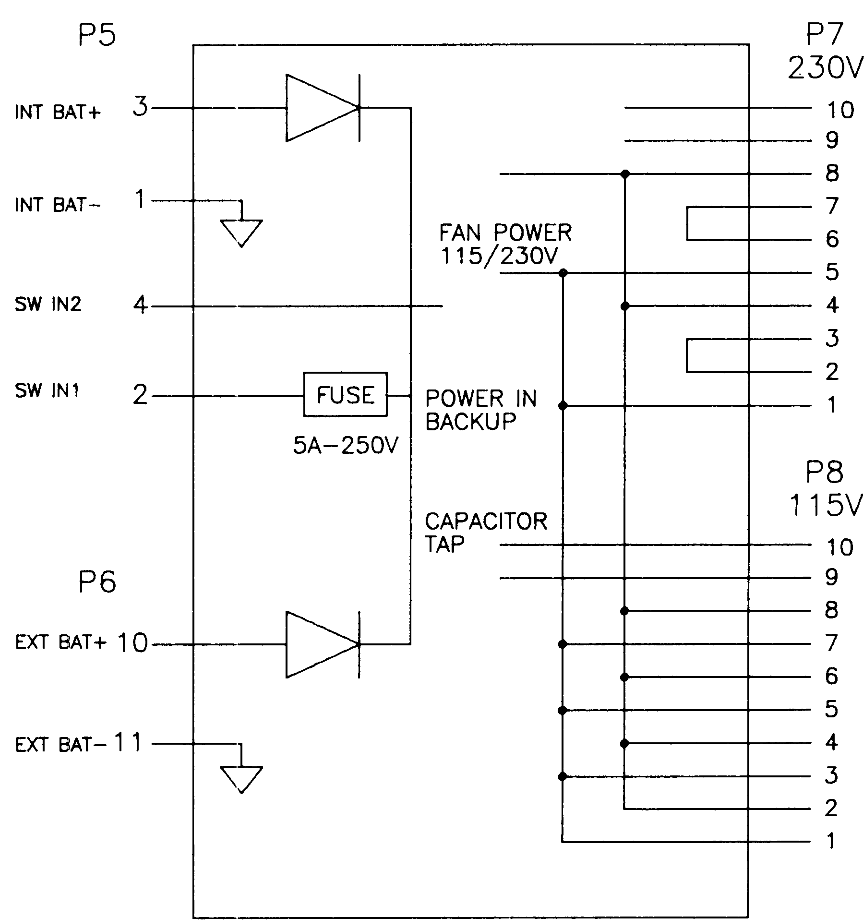

Figure B-3. 440-Watt Power Supply Connector Diagram

Table B-2. Electrical Connections (440W Supply)

P1 DC OUTPUT CONNECTOR (PC EDGE BOARD)	
Pin Number	**Signal Name**
1 thru 36	+5.1 Volts
37 thru 50	Common
P2 DC OUTPUT CONNECTOR (PC EDGE BOARD)	
Pin Number	**Signal Name**
1 thru 28	Common
29 thru 32	+12 Volts
33, 34	-12 Volts
35 thru 38	+5.1 Volts Memory Backup
39 thru 42	25 kHz Phase 1
43 thru 46	25 kHz Phase 2
47	PON+
48	PFW-
49	MLOST-
50	+5.1 Volts Memory Sense
P5 BATTERY SWITCH CONNECTOR	
Pin Number	**Signal Name**
2	Switch in 1
4	Switch in 2
1	Internal Battery -
3	Internal Battery +
P9 AC LINE INPUT	
Pin Number	**Signal Name**
1	AC Line
2	No Connection
3	AC Neutral

Table B-2. Electrical Connections (440W Supply) (Continued)

P7/P8 AC LINE CONFIGURATION / FANS	
Pin Number	Signal Name
1	Fan #1
2	Fan #1
3	Fan #2
4	Fan #2
5	Fan #3
6	Fan #3
7	Fan #4
8	Fan #4
9	230v / 115v
10	230v / 115v
P6 TEST POINTS / EXTERNAL BATTERY	
Pin Number	Signal Name
1	+5V Test
2	+12V Test
3	-12V Test
4	+5VM Test
5	PON
6	PFW
7	MLOST
8	25 kHz Test
9	25 kHz Test
10	Battery +
11	Battery -
12	Common

B.2.4 ELECTRICAL SPECIFICATIONS (440W Supply)

The electrical specifications of the 440-watt supply are provided below in several tables. Ac line input specifications are given in Table B-3, battery input specifications are given in Table B-4, and supply output specifications are given in Table B-5.

Table B-3. Input Electrical Specifications (440W Supply)

AC LINE SPECIFICATIONS

These specifications do not include the power required for the fans.

	Min	Nominal	Max	
Range 1				
Voltage	84	120	140	Volts RMS
RNS Current (Max)	9.4	7.2	6.2	Amps
Inrush	-	-	136	Amps
Range 2				
Voltage	176	230	278	Volts RMS
RMS Current (Max)	4.7	3.7	3.1	Amps
Inrush	-	-	262	Amps
Carry Over	10.6	-	-	mSec
PFW Trip Point				
Range 1	-	-	84	Volts RMS
Range 2	-	-	176	Volts RMS
Line Frequency	47	60	67	Hz
Line Fuse	-	-	10	Amps
Input Power	-	-	700	Watts

Note: Power supply input operation permits input transients of up to 3000V for periods of not less than 10 μs.

Table B-4. Battery Input Specification (440W Supply)

	MINIMUM	NOMINAL	MAXIMUM	
Battery Voltage	10.0	12.0	14.4	Volts
Discharge, Continuous	-	-	40.0	Amps
Internal Resistance	-	10.0	-	mohms
Note: 10.0V is the approximate input disconnect voltage. Disconnect occurs when Output #1 (5.1V) drops to 4.9V, as measured at the battery backup board (coincident with the assertion of MLOST-).				

Table B-5. Output Electrical Specifications (440W Supply)

Maximum Dynamic Load: **10% over 10 microseconds**

Output Stress Conditions Allowed:

a. Supply will recover from a shorted regulated output and excessive ambient temperature.

b. Over rated operated temperature.

Output Regulation (Note 4):

Output # 1	Nominal Voltage	5.1	Volts	
	Maximum Current	70	Amps	(1) (5)
Regulation	0.0 to 3.0 Amps	+10%	-10%	
	3.0 to 6.2 Amps	+5%	-5%	
	6.2 to 70.0 Amps	+2%	-2%	
Output # 2	Nominal Voltage	12.0	Volts	
	Maximum Current	5.6	Amps	
Regulation	0.0 to .03 Amps	+10%	-10%	
	.03 to 5.6 Amps	+6%	-3%	
Output # 3	Nominal Voltage	-12.0	Volts	
	Maximum Current	3.5	Amps	
Regulation	0.0 to .10 Amps	+12%	-12%	
	.10 to 3.5 Amps	+6%	-6%	

Table B-5. Output Electrical Specifications (440W Supply) (Continued)

Output # 4 (opt.)	Nominal Voltage	5.1	Volts
	Maximum Current	10.0	Amps (2)
Regulation	0.0 to .10 Amps	+10%	-10%
	.10 to 10.0 Amps	+2%	-2%
Output # 5 (opt.)	Nominal Voltage	39	Volts RMS (5)
	Split Phase	19.5	Volts RMS
	Maximum Current	1.5	Amps
Regulation	0.0 to .02 Amps	+10%	-12%
	.02 to 1.5 Amps	+8%	-8%
Output # 6 (opt.)	Battery Charger		
	Minimum Current less than	.050	Amps (3)
	Maximum Current	.200	Amps
	Maximum Voltage	14.4	Volts
Output # 7	Fan Power		
	Nominal Voltage	115	Volts RMS
	Maximum Current	1.25	Amps

NOTES: (1) When no battery backup module is installed, the Output #4 current is supplied by Output #1. The total current drawn from Output #1 will not exceed 70 Amp.

(2) Output #4 shall be limited to 7 Amps when the 0950-1666 battery backup module is installed.

(3) When the battery is fully charged.

(4) Although the sum of the maximums listed above exceeds the 440-watt specification of the power supply front end, not all of the outputs will be at maximum load at the same time and the actual maximum load will never exceed 440-watts (not including fan power).

(5) When the maximum load is applied to Output #5 the load on Output #1 will not exceed 64 Amps.

B.2.5 ENVIRONMENTAL SPECIFICATIONS (440W Supply)

The environmental specifications of the 0950-1671 440-watt power supply are provided in Table B-6.

Table B-6. Environmental Specifications (440W Supply)

Non Operating Temperature:
-40 deg C to 75 deg C

Operating Temperature:
0 deg C to 55 deg C
Type Tested
-5 deg C to 60 deg C (to insure margins)

Operating Survival Temperature:
-20 deg C to 65 deg C

Operating Humidity:
5% to 95% at 40 deg C wet bulb temperature

Vibration:

Sweep
From 5 to 55 Hz and back at a rate of one octave per minute, with an excursion of .015", for 15 minutes

Resonance
At each resonant point, not to exceed 4 points, dwell for 10 minutes at the following excursions:

5 - 10 Hz	.125"
11 - 25 Hz	.060"
25 - 55 Hz	.015"

Shock:

30g peak force applied as an 11 millisecond sine pulse. To be tested in each direction of each axis (6 tests).

Altitude:

Full operating temperature, at 440-watts output power (not including fan power), at altitudes up to 10,000 feet, at 15,000 feet a derating of up to 10 deg C, of operating temperature, is allowed.

B.2.6 REPLACEABLE PARTS (440W Supply)

Replaceable parts lists for the 440W power supply are provided in Tables B-7 and B-8. Table B-9 covers the battery backup board, and Table B-10 covers the 25 kHz sine-wave card. The parts can be located in Figures B-4 through B-7.

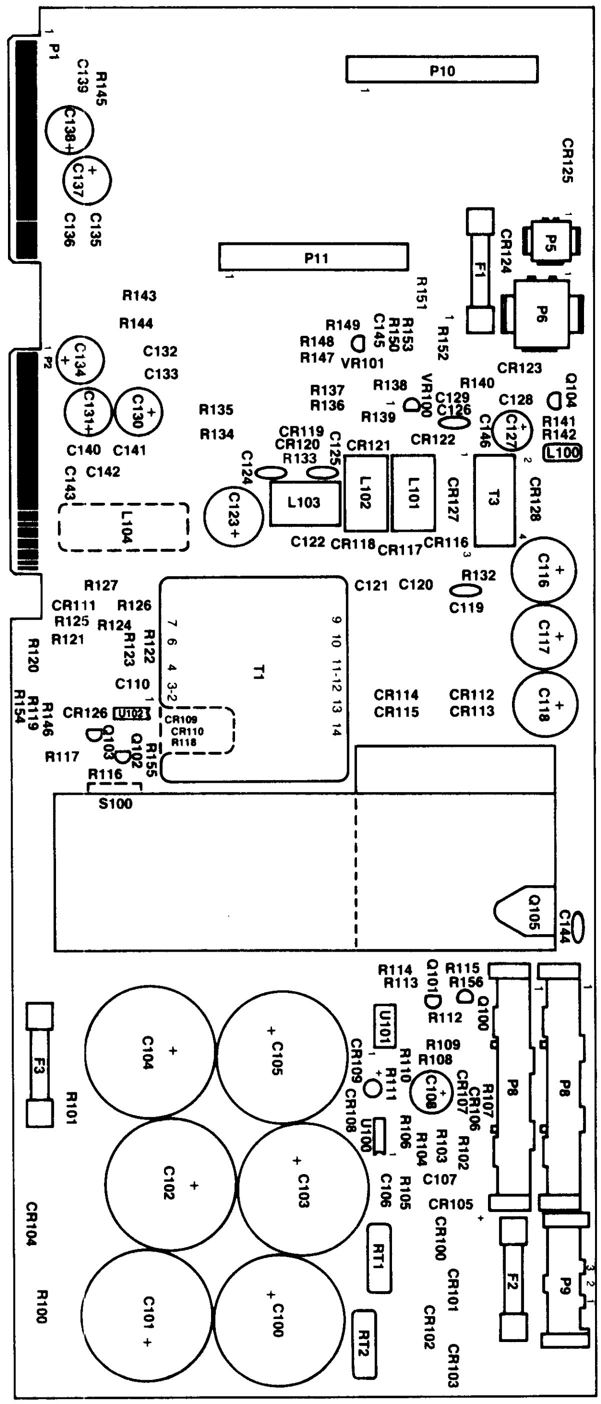

Figure B-4. Parts Locations for Board 1, 440W Supply

Update 1

Table B-7. 440W Supply Board 1 Replaceable Parts (Sheet 1 of 3) (HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	13713	P C B XL400-5411R	
002			
003	13825	SUB ASSY XFMR WIRING HARNESS BD	T1, (REF)
004	13824	SUB ASSY DIODE HEATSINK XL400-3411	R128, R129, R130, R131, C111, C112, C113, C114, CR112, CR113, CR114, CR115, (REF)
005	13835	BUS BAR RETURN	
006	13836	HEATSINK DIODE	
007			
008			
009			
010	13536	CAP ELECT 1000UF-200V SNAP-IN TERM	C100, C101, C102, C103, C104, C105
011	11659-02	CAP ELECT RAD LDS 3.3UF-250V DC	C108
012	10520-04	OBSOLETE(CAP ELECT 3.3UF-50V)	C109
013	10765-18	CAP ELECT 330UF 63V RD LDS VB	C123
014	11106-01	CAP ELECT R LDS 470UF-25VDC LO ESR	C130, C131
015	11110-01	CAP ELECT 1000UF 10V	C134, C137, C138
016	12951	CAP ELECT 10UF-100VDC LO ESR R LDS	C127
017	2032	CAP CERM .001UF 10% 1000VDC	C119
018	2060	CAP CERM 470PF-1KV	C124, C125, C126
019	10765-06	CAP ELECT 3.3UF 63V RD LDS VB	C109, REPLACES ITEM #012
020	12685-07	CAP MET POLY .47UF 5% 63/100V	C107
021	13594-02	CAP MET POLY .047UF 250V 5% .4"LS	C106, C128
022	12328-05	CAP MET POLY 0.33UF 63VDC 5%	C110, C133, C135
023	12657-07	CAP MET POLY RLD .10UF 10% 250VDC	C122, C139
024	12328-04	CAP MET POLY 0.22UF 63VDC 5%	C120, C121, C129, C132, C136, C140, C141, C142, C143, C146
025	13723-01	CAP ELECT 2200UF-16V RLD LOZ HI RIP	C116, C117, C118
026	13593-07	CAP MET POLY .01UF 630/1000V 5%	C145
027			
028	2105	CAP CERM 100PF-1KV	C144
029			
030	1021	DIODE HI CUR. AX LDS. 400V,6A MR754	CR100, CR101, CR102, CR103
031	10056-01	OBSOLETE(DIODE FAST RECV)	CR117, CR118
032	11380-04	DIODE FULL WAVE BRDG PREP/10868-04	CR105
033	1038	DIODE GEN PUR 1A IN4004 400VDC	CR106
034	12594	DIODE SILICON CASE DO-35,IN4448	CR107, CR109, CR110, CR126
035			
036	1043	DIODE GEN PUR AX LDS 3A 400V MR504	CR123, CR124, CR125
037	12577-02	DIODE RECT FAST RECV.16A 100V	CR116
038	14461-01	DIODE FST RECV 2A 100V AX LDS	CR119, CR120
039	1014	DIODE ZENER 500 MW 5.6V 5% IN5994B	CR104
040	1008	DIODE ZENER 400MW 15V 5% IN965A	CR108
041	11356-15	DIODE ZENER 500MW 8.2V 5% IN5998B	CR111
042	1042	DIODE FST RCV 200V 3A AX LDS MR852	CR121, CR122, CR127, CR128
043	10056-03	DIODE FAST RECV BYW 29-150	CR117, CR118, REPLACES ITEM #031
044			
045			
046	10180-01	FUSE 5A-250V NORMAL-BLOW	F1, F3
047	10865	FUSE 10 AMP 250V (BUSS ABC10)	F2
048	13799	HARNESS 2 PIN CONN	J14
049	13800	HARNESS 3 PIN CONN	J13
050	13801	HARNESS 4 PIN CONN	J12

Table B-7. 440W Supply Board 1 Replaceable Parts (Sheet 2 of 3)
(HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
051			
052	7421	WIRE RED 18 AWG 5" (1/4 X 1/4) UL10	JP7
053	10009-07	WIRE YEL 18 AWG 2.75 LG 1/4 X 1/4	JP3
054	7949	WIRE RED 18 AWG 3 5/8" (1/4 X 1/4)	JP8
055	10372-11	WIRE WHT 22 AWG 3.75" 1/4 X 1/4	JP4
056	10236-04	WIRE BLK 22 AWG 4.25" (1/4 X 1/4)	JP5
057	10008-06	WIRE ORN 18 AWG 3.75" 1/4 X 1/4	JP6
058			
059	14364	INDUCTOR OUTPUT 70A XL400-5411R	L104
060	10799	INDUCTOR 18 UH	L100
061	10899	INDUCTOR 14.4 UH	L101, L102, L103
062	13332	PCB PIN HEADER 4 CKT GOLD PIN	P5
063	13331	PCB PIN HEADER 12 CKT GOLD PIN	P6
064	13333-02	CONN PCB 10 CKT INLINE PIN HEADER	P7, P8
065	13333-01	CONN PCB 3 CKT INLINE PIN HEADER	P9
066	14565-04	CONN PCB 15/30 CONT PRS .125 CTR	P10, P11
067			
068			
069			
070	1016	TRANS PNP CASE TO-92 2N4126	Q104
071	12592	TRANS PNP CASE TO-92,MPS 2907A	Q102
072	12593	TRANS NPN TO-92 CASE MPS2222A	Q100, Q103
073	12591	TRANS NPN CASE TO 92 2N4124	Q101
074	14263-01	TRANS NPN POWER DARLING 10A TIP 140	Q105
075	3124	OBSOLETE(RES 150K OHM 1/4W)	R156
076	3077	OBSOLETE(RES 1.6K OHM 1/4W)	R146
077	3062	OBSOLETE(RES 390 OHM 1/4)	R141
078	3324	RES CF 150K OHM 5% 1/2W	R102
079	3091	OBSOLETE(RES 6.2K OHM 1/4W)	R104
080	3120	OBSOLETE(RES 100K OHM 1/4W)	R105, R119
081	3096	OBSOLETE(RES 10K OHM 1/4W)	R108, R112, R118, R125
082	3078	OBSOLETE(RES 1.8K OHM 1/4W)	R106
083	3122	OBSOLETE(RES 120K OHM 1/4W)	R111
084	3082	OBSOLETE(RES 2.7K OHM 1/4W)	R110
085	3072	RES CF 1K OHM 5% 1/4W	R109, R148, R154
086	3100	OBSOLETE(RES 15K OHM 1/4W)	R113
087	3088	OBSOLETE(RES 4.7K OHM 1/4W)	R115, R120, R121
088			
089	3093	OBSOLETE(RES 7.5K OHM 1/4W)	R126
090	3112	OBSOLETE(RES 47K OHM 1/4W)	R122
091	3108	OBSOLETE(RES 33K OHM 1/4W)	R124
092	10318-76	OBSOLETE(RES 3K OHM 1/4W)	R149
093	3084	OBSOLETE(RES 3.3K OHM 1/4W)	R155, R150
094	3256	RES CF 220 OHM 5% 1/2W	R133
095	10304-41	RES CF 100 OHMS 5% 1/2W	R132
096	3115	OBSOLETE(RES 62K OHM 1/4W)	R151
097	10318-102	OBSOLETE(RES 1.2 OHM 1/4W)	R142
098	3060	OBSOLETE(RES 330 OHM 1/4)	R136, R140
099	3064	OBSOLETE(RES 470 OHM 1/4W)	R138
100	3092	OBSOLETE(RES 6.8K OHM 1/4W)	R153, R147
101	10233-84	RES MET OXIDE 27K OHM 5% 2W	R100, R101
102	10233-48	RES MET OXIDE 820 OHM 5% 2W	R127

Table B-7. 440W Supply Board 1 Replaceable Parts (Sheet 3 of 3)
(HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
103	11313-51	RES MF 3.32K OHMS 1% 1/8W	R137
104	10232-57	RES MET OXIDE 1K OHM 5% 1 W	R117
105	10232-65	RES MET OXIDE 2.2K OHM 5% 1W	R116
106	3080	OBSOLETE(RES 2.2K OHM 1/4W)	R114
107			
108			
109	10522-29	RES WW 12K OHMS 5% 5W	R107
110	3820	RES WW 120 OHM 5% 2W BWH	R134, R135
111	3903	RES WW 10 OHM 5% 5W	R143, R144
112	10966-49	RES WW 1K OHM 10% 2W BWH	R145
113	3943	RES POT 5K VADJ MTURN .5W CERMET	R139
114	10519-16	RES POT 50K OHM VADJ STURN .5W CERM	R103
115	10519-10	RES POT 2K OHM VADJ STURN .5W CERM	R123, R152
116			
117			
118			
119			
120	3938	RES THERMISTOR DISC 5 OHM 15% ST LD	RT1, RT2
121	3911	THERMOSTAT SNAP-ACTING AUTO RESET	S100
122			
123	14159	TRANSFORMER T3 BIFILAR	T3
124			
125			
126			
127	10505	I C LOW POWER DUAL VOLT COMP LM393N	U100, U102
128	11498	I C OPTO-ISOLATOR OP1-1264B	U101
129	1071	I C SHUNT REG TL430	VR100, VR101
130	14381	TIE WRAP PUSH MOUNT	(REF), L104
131	11661-01	SPACER GLASS .225 OD .067 ID .185TH	(REF), R107, RT1, RT2
132	7501	TIE WRAP MEDIUM	(REF), L104
133	7500	TIE WRAP SMALL	
134	13887	INSULATOR	
135	13831	TRANSFORMER SUPPORT	(REF), T1
136	7015	FUSE CLIP PCB TYPE FOR 3AG FUSE	XF1, XF2, XF3
137	10006-12	WIRE BLU 18AWG 3.75"(1/4 X 1/4)	T3(REF)
138	10004-13	WIRE BLK 18 AWG 3.75"(1/4 X 1/4)	T3(REF)
139	10002-04	WIRE RED 18 AWG 5.50 (1/4 X 1/4)	(REF), S100
140	7578	SCREW P H 4-40 X 1/4	(REF), S100
141	7511	SCREW P H 6-32 X 1/2	(REF), H/S, T1
142			
143	7576	SCREW P H 6-32 X 1/4	Q105(REF)
144	7577	WASHER SPLIT LOCK #4	(REF), S100
145	7588	WASHER SPLIT RING LOCK #6	(REF), H/S, T1
146	7506	WASHER FLAT #6	(REF), H/S, T1
147	11828	WASHER METAL	(REF), Q105
148	12560	MTG HDW TO-220 NON CNDCT #4	(REF), CR116, CR117, CR118
149	10726-01	SPACER INSULATED #6 .250 DIA .125LG	
150	13979	STIFFENER 3.00 X 4.50	(REF), C100, C101, C102, C103, C104, C105
151	13980	STIFFENER .75 X 2.20	(REF), C116, C117, C118
152	13981	STIFFENER .50 X 1.00	(REF), C137, C138
153			
154			
155	12459	LABEL FUSE WARNING	(REF), C104
156	12569	LABEL,CSA MARK	
157	7740	LABEL DANGER HIGH VOLTAGE	(REF), C101

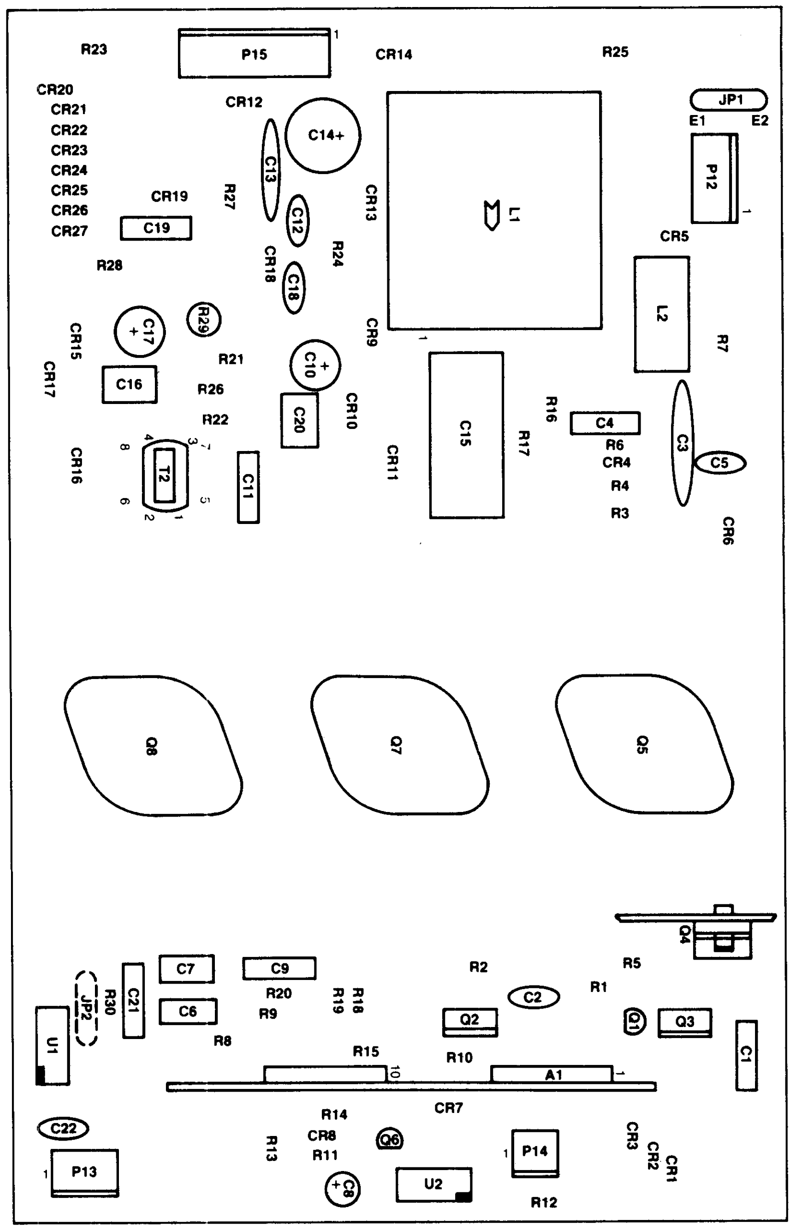

Figure B-5. Parts Locations for Board 2, 440W Supply

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Table B-8. 440W Supply Board 2 Replaceable Parts (Sheet 1 of 2)
(HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	13619	TRANS NPN POWER 400V 15A 2N6678	Q5, Q7, Q8
002	1118	TRANS NPN POWER MJE13007	Q4
003			
004			
005			
006			
007	3098	OBSOLETE(RES 12K OHM 1/4W)	R30
008	3080	OBSOLETE(RES 2.2K OHM 1/4W)	R8
009	3046	OBSOLETE(RES 82 OHM 1/4W)	R9
010	3096	OBSOLETE(RES 10K OHM 1/4W)	R11
011	3104	OBSOLETE(RES 22K OHM 1/4W)	R10, R20
012	3064	OBSOLETE(RES 470 OHM 1/4W)	R1
013	10318-22	OBSOLETE(RES 16 OHM 1/4W)	R14
014	3048	OBSOLETE(RES 100 OHM 1/4W)	R13
015	3056	OBSOLETE(RES 220 OHM 1/4W)	R12
016	3135	OBSOLETE(RES 430K OHM 1/4W)	R19
017	3040	OBSOLETE(RES 47 OHM 1/4W)	R26
018	3024	OBSOLETE(RES 10 OHM 1/4W)	R6
019	10233-78	RES MET OXIDE 15K OHM 5% 2W	R2, R23
020	13598-08	RES MF UNCUT LDS 365K 1% 1/8W	R18
021	10232-95	RES MET OXIDE 47K OHM 5% 1 W	R21, R22
022	10233-30	RES MET OXIDE 150 OHM 5% 2W	R24, R27
023	10232-16	RES MET OXIDE 20 OHM 5% 1 W	R29
024			
025	3811	RES WW 10 OHM 10% 1W BW20F	R15, R3, R4
026	3816	RES WW .2 OHM 5% 2W BWH	R16, R17
027	12261-13	RES WW 10 OHM 10% 10W	R25
028	3812	RES WW 82 OHM 10% 1W BW20F	R5
029	3918	RES WW 5 OHM 5% 5W	R7
030	10048-65	RES WW 47 OHM 5% 2W BWH	R28
031			
032			
033			
034	12872-01	TRANSFORMER DRIVE,PC MT TWO CORE 4T	T2
035	11498	I C OPTO-ISOLATOR OP1-1264B	U2
036	12975-15	OPTO ISOLATOR SORTED VDE 390 ORN	U1
037	12854	CONN JACK CLOSED ENTRY P C SWAGE MT	E1, E2, E3, E4
038	11661-01	SPACER GLASS .225 OD .067 ID .185TH	(REF), R25
039	11399	ASSY MTG HDW TO-3 CNDCT PEM STUD	(REF), Q5, Q7, Q8
040	7509	SCREW P H 4-40 X 1/2	(REF), Q4, CR6
041	7503	NUT HEX 4-40	(REF), Q4, CR6
042	7602	WASHER INT TOOTH LOCK #4	(REF), Q4, CR6
043	7010	INSULATOR ALUM TO-220	(REF), Q4, CR6
044	11572	INSULATOR TO-220	(REF), Q4, CR6
045	7930	WIRE RED 22 AWG 1 1/2" (1/4, 1/4)T	(REF), T2
046	7202	ORTV 108 CLEAR	
047			
048			
049			
050			
051			
052			

Table B-8. 440W Supply Board 2 Replaceable Parts (Sheet 2 of 2) (HP 0950-1671, Boschert XL0400-5411R)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
053	13730	P C B	
054	12983	CONTROL BOARD 723	A1
055			
056			
057			
058			
059			
060			
061	13834	HEATSINK TRANSISTOR	(REF), Q5, Q7, Q8
062	10346-01	CAP ELECT 10UF-16V RAD LDS	C8
063	12288	CAP ELECT 4.7UF 20% 100V LO ESR RLD	C10, C17
064	2071	CAP ELECT RAD.LEADS 10UF-250V	C14
065	2105	CAP CERM 100PF-1KV	C2
066	2003	CAP CERM .1UF +80%-20% 500VDC	C3
067	2073	CAP CERM DISC .001UF-3KV 20%	C12, C18
068	2062	CAP CERM 270PF-1KV	C5
069	2032	CAP CERM .001UF 10% 1000VDC	C22
070	2005	CAP CERM DISC .01UF 1KVDC 20% Z5U	C13
071	12328-04	CAP MET POLY 0.22UF 63VDC 5%	C6
072	12328-06	CAP MET POLY 0.47 63VDC 5%	C7
073	13593-05	CAP MET POLY .0047UF 630/1000V 5%	C9, C11, C21
074	12328-08	CAP MET POLY 1.0UF 63VDC 5%	C16, C20
075	13450-01	CAP MET POLY .1UF 100VDC 5% R LDS	C1, C4, C19
076	2080	CAP MET POLY 2UF-200VDC 10%	C15
077			
078			
079			
080			
081	14461-01	DIODE FST RECV 2A 100V AX LDS	CR20, CR21, CR22, CR23, CR24, CR25, CR26, CR27
082	13734	DIODE GEN PUR FST FWD REC IN4004	CR1, CR2, CR3, CR12, CR13, CR18, CR19
083	12594	DIODE SILICON CASE DO-35,IN4448	CR4, CR8
084	1045	DIODE FST RCV 100V 3A AX LDS MR854	CR5, CR14
085	11196	DIODE FAST RECV MR2404F	CR6
086	1028	OBSOLETE(DIODE RECTIFIER)	CR17, CR9
087	12260-04	DIODE HI CUR AX LDS. 30V,6A SR3773	CR10, CR11, CR15, CR16
088	11356-15	DIODE ZENER 500MW 8.2V 5% IN5998B	CR7
089	1155	DIODE FST RCV 1A 600V AX LD IN4937	CR17, CR9, REPLACES ITEM #034
090	10024-02	TERM PLUG .400	JP1
091			
092	13733	INDUCTOR 4MH	L1
093	11625	INDUCTOR 010467-01/02	L2
094			
095			
096	13195-01	CONN FRICTION LOCK 4 POS .156 CTR	P12
097	13195-04	CONN FRICTION LOCK 2 POS .156 CTR	P14
098	13195-05	CONN FRICTION LOCK 3 POS .156 CTR	P13
	13195-06	CONN FRICTION LOCK 7 POS .156 CTR	P15
	12592	TRANS PNP CASE TO-92,MPS 2907A	Q1, Q6
	12675	TRANS PNP HI VOLT 400V TO-126 CASE	Q3
	1005	TRANS NPN POWER TIP-50	Q2

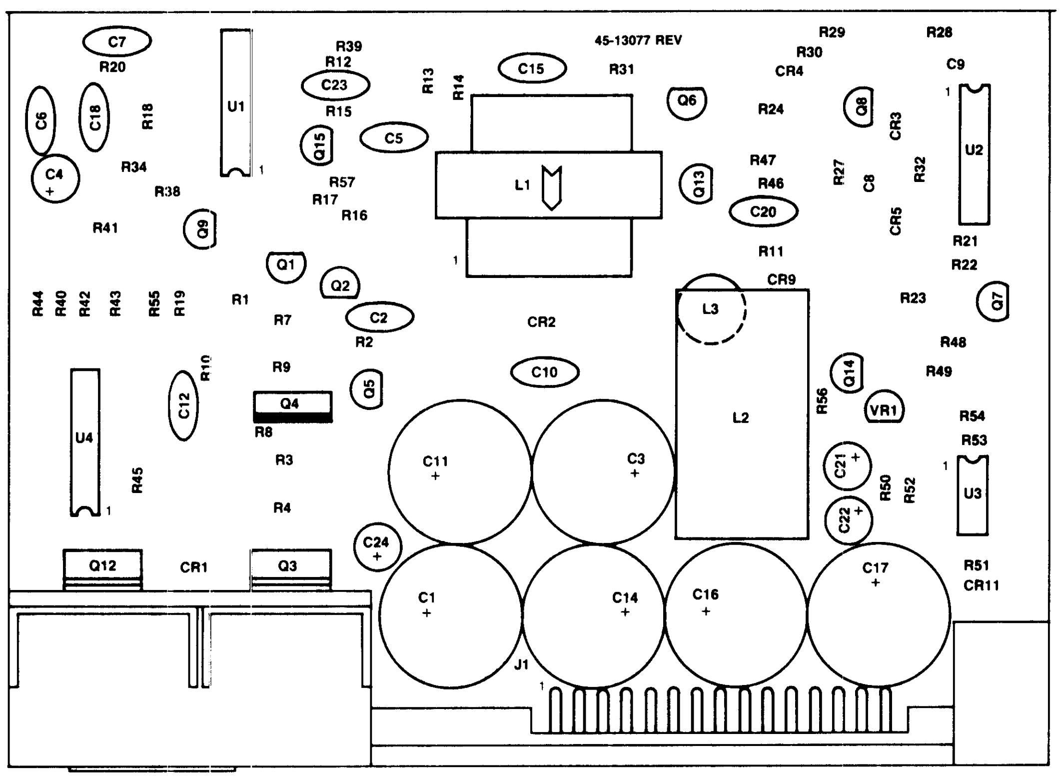

Figure B-6. Parts Locations for Battery Backup Card (BB500)

Table B-9. Battery Backup Card Option Replaceable Parts (Sheet 1 of 3)
(Boschert BB500 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	13093	P C B	
002			
003			
004	2032	CAP CERM .001UF 10% 1000VDC	C2, C18
005	2008	CAP CERM .1UF-100V	C5, C10, C23
006	2120	CAP CERM .0022UF-1KV	C6, C12
007			
008			
009	2060	CAP CERM 470PF-1KV	C7
010	2062	CAP CERM 270PF-1KV	C15
011	2059	CAP CERM .01UF-100V	C20
012			
013			
014	10520-13	CAP ELECT 470UF 50V RD LDS VB	C1, C3, C11, C14, C16, C17
015	10520-05	OBSOLETE(CAP ELECT 4.7UF-50V)	C4
016	10520-02	OBSOLETED(CAP ELECT 1.0UF-50V)	C21
017	10346-01	CAP ELECT 10UF-16V RAD LDS	C22
018	10520-04	OBSOLETE(CAP ELECT 3.3UF-50V)	C24
019	10765-07	CAP ELECT 4.7UF 63V RD LDS VB	C4, REPLACES ITEM #015
020	13593-01	CAP MET POLY .001UF 630/1000V 5%	C8, C9
021	10765-06	CAP ELECT 3.3UF 63V RD LDS VB	C24, REPLACES ITEM #018
022	10541-03	CAP ALUM ELECT 1.0UF 100W VDC	C21, REPLACES ITEM #016
023	1038	DIODE GEN PUR 1A IN4004 400VDC	CR1
024	12594	DIODE SILICON CASE DO-35,IN4448	CR3, CR4, CR5, CR9, CR11
025			
026	11730-20	HEATSINK SUB ASSY TO-220	CR2, (REF)
027			
028	12540	I C ADJ PREC SHUNT REG TO 92	VR1
029			
030			
031			
032			
033			
034	11969	INDUCTOR 3 TERM REG	L1
035	11762	INDUCTOR 011749	L2
036	12209	INDUCTOR AIR CORE	L3
037			
038			
039	11463	TRANS MPS-A56	Q1, Q2, Q5, Q9
040	11689	TRANS PNP HIGH VOLT D45C11	Q4
041	13530	TRANS NPN POWER 45V 15A D44VH4	Q3
042			
043			
044	11464	TRANS NPN MPS-A06	Q6, Q7, Q15
045	1017	TRANS NPN GEN PUR MPS-5172	Q8
046	1144	TRANS NPN POWER SIL TIP-31 TO-220	Q12
047			
048			
049	12593	TRANS NPN TO-92 CASE MPS2222A	Q13, Q14
050			
051			
052			

Table B-9. Battery Backup Card Option Replaceable Parts (Sheet 2 of 3)
(Boschert BB500 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
053			
054			
055	3074	OBSOLETE(RES 1.2K OHM 1/4W)	R1, R7, R40
056	3067	OBSOLETE(RES 620 OHM 1/4W)	R2
057	3048	OBSOLETE(RES 100 OHM 1/4W)	R8
058			
059			
060	3064	OBSOLETE(RES 470 OHM 1/4W)	R10
061			
062	3113	OBSOLETE(RES 51K OHM 1/4W)	R15
063			
064			
065	3120	OBSOLETE(RES 100K OHM 1/4W)	R17, R28
066	3103	OBSOLETE(RES 20K OHM 1/4W)	R55
067	3116	OBSOLETE(RES 68K OHM 1/4W)	R20
068	3110	OBSOLETE(RES 39K OHM 1/4W)	R53
069			
070	3096	OBSOLETE(RES 10K OHM 1/4W)	R21, R22, R45, R57, R47
071	3072	RES CF 1K OHM 5% 1/4W	R23, R29, R42
072	3091	OBSOLETE(RES 6.2K OHM 1/4W)	R24
073	3092	OBSOLETE(RES 6.8K OHM 1/4W)	R46
074			
075	3090	OBSOLETE(RES 5.6K OHM 1/4W)	R27, R50
076	3108	OBSOLETE(RES 33K OHM 1/4W)	R30
077	3134	OBSOLETE(RES 390K OHM 1/4W)	R32, R34
078			
079			
080	3087	OBSOLETE(RES 4.3K OHM 1/4W)	R38
081			
082			
083	3040	OBSOLETE(RES 47 OHM 1/4W)	R39
084	10318-05	OBSOLETE(RES 3.3 OHM 1/4W)	R44
085	3068	OBSOLETE(RES 680 OHM 1/4W)	R52
086			
087			
088	3088	OBSOLETE(RES 4.7K OHM 1/4W)	R54, R56
089	3084	OBSOLETE(RES 3.3K OHM 1/4W)	R51
090			
091	10329-91	RES MF 43K 2% 1/4W	R12
092	10329-61	RES MF 2.4K 2% 1/4W	R16
093	10329-03	RES MF 270K 2% 1/4W	R31
094	10329-74	RES MF 8.2K 2% 1/4W	R14
095			
096			
097	3094	OBSOLETE(RES 8.2K OHM 1/4W)	R43, R19
098	3102	OBSOLETE(RES 18K OHM 1/4W)	R48
099			
100			
101			
102			
103			
104	3800	RES WW .1 OHM 5% 2W BWH	R3, R4

Table B-9. Battery Backup Card Option Replaceable Parts (Sheet 3 of 3) (Boschert BB500 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
105	3811	RES WW 10 OHM 10% 1W BW20F	R9
106	10966-49	RES WW 1K OHM 10% 2W BWH	R11
107			
108	10660-10	RES POT 2K OHMS VERT ADJ .5W CERM	R13
109	3902	RES POT 5K OHM HORZ ADJ 10% .75W	R41, R49
110	10519-10	RES POT 2K OHM VADJ STURN .5W CERM	R18
111			
112			
113	1000	I C VOLT REG 723	U1, U4
114	10379-01	I C NOR GATE DUAL IN CMOS CD4001BE	U2
115	10505	I C LOW POWER DUAL VOLT COMP LM393N	U3
116			
117	13495	BRACKET BATT BACK-UP XL400-3502	
118	7577	WASHER SPLIT LOCK #4	
119	7506	WASHER FLAT #6	
120	7588	WASHER SPLIT RING LOCK #6	
121	11092-01	STANDOFF HEX 4-40 .250LG	
122	13744	MTG HDW TO-220 NON CNDCT #4	
123	14578	LABEL SMALL BOSCHERT MODEL/SER NO	
124	13570	HEATSINK TO-220 NO MTG TABS	
125	15178	LABEL CUSTOMER ID	L1(REF)
126	7863	0.0400TAPE 2 SIDED 1/16	L2, (REF)
127			
128	12891-03	PEM STUD 4-40 THREAD .625 LG	
129	13618-01	SCREW CAPTIVE PANEL .625" LG 6-32	

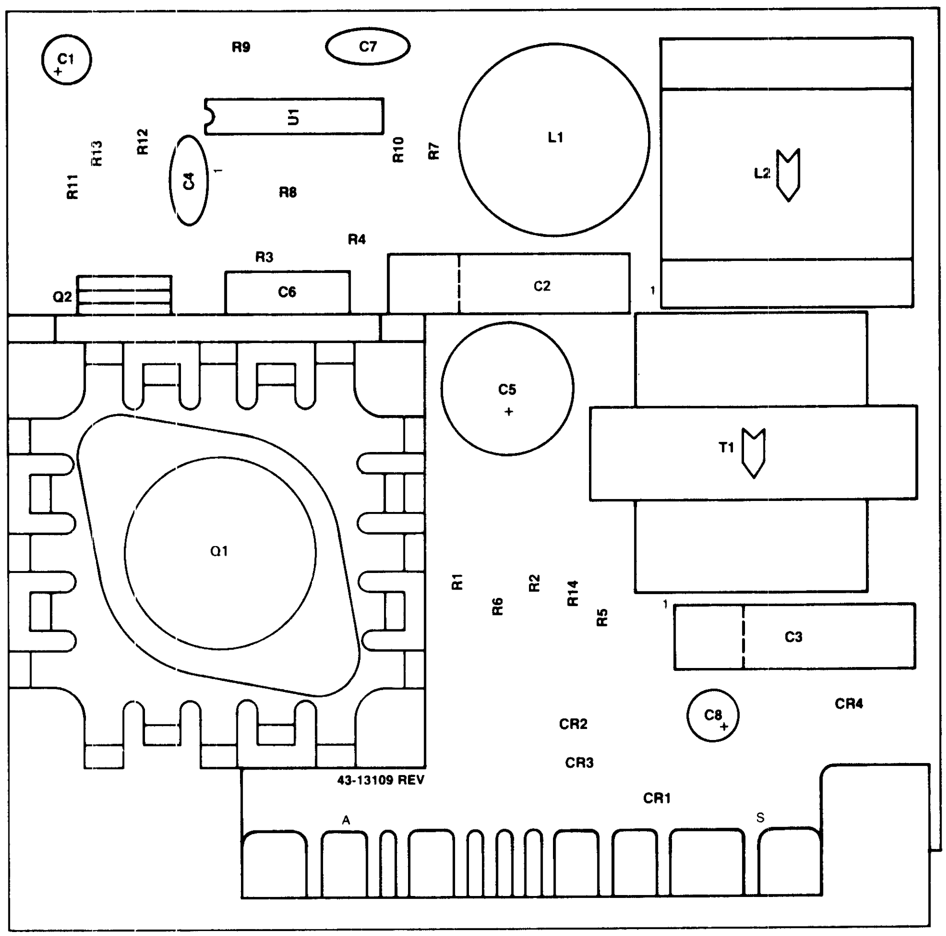

Figure B-7. Parts Locations for 25 kHz Card (SW100)

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Table B-10. 25 KHz Card Option Replaceable Parts (Sheet 1 of 2)
(Boschert SW100 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	13137	P C B SW100	
002	13527	HEATSINK TO-3	
003	13494	BRACKET SINE WAVE,SW100	
004			
005	2059	CAP CERM .01UF-100V	C4
006	11133-01	CAP MET POLY .1UF 100V 10% RLDS	C6
007			
008			
009			
010	13249-01	OBSOLETE(CAP ELECT 100UF-50V)	C5
011	14297-04	CAP ELECT 100UF 50V LO ESR RLDS RX	C5, REPLACES ITEM #010
012	10765-06	CAP ELECT 3.3UF 63V RD LDS VB	C1, C8
013	2032	CAP CERM .001UF 10% 1000VDC	C7
014			
015			
016	14580-01	CAP MET POLYP 0.22UF 250V 5% RLD	C2
017	14580-02	CAP MET POLYP 0.33UF 250V 5% RLD	C3
018			
019			
020	1088	OBSOLETE(DIODE FST RCV 100V-3A)	CR1, CR2
021	1026	OBSOLETE(DIODE 200V-1A)	CR3, CR4
022	1155	DIODE FST RCV 1A 600V AX LD IN4937	CR3, CR4, REPLACES ITEM #021
023	1042	DIODE FST RCV 200V 3A AX LDS MR852	CR1, CR2, REPLACES ITEM #020
024			
025	13163	INDUCTOR ASSY 140UH @ 1.75 ADC	L1
026	13164	INDUCTOR 100 UH @ 1.25A PQ26/25	L2
027			
028			
029	1094	TRANS NPN POWER 2N5885	Q1
030	1144	TRANS NPN POWER SIL TIP-31 TO-220	Q2
031			
032			
033			
034	3040	OBSOLETE(RES 47 OHM 1/4W)	R3
035	3082	OBSOLETE(RES 2.7K OHM 1/4W)	R9, R5
036	3068	OBSOLETE(RES 680 OHM 1/4W)	R4
037			
038			
039	3087	OBSOLETE(RES 4.3K OHM 1/4W)	R14
040	3100	OBSOLETE(RES 15K OHM 1/4W)	R13
041	3104	OBSOLETE(RES 22K OHM 1/4W)	R8
042			
043			
044	3113	OBSOLETE(RES 51K OHM 1/4W)	R11
045	3052	OBSOLETE(RES 150 OHM 1/4W)	R6
046	3092	OBSOLETE(RES 6.8K OHM 1/4W)	R10
047	3272	RES CF 1K OHM 5% 1/2W	R7
048			
049			
050	10048-02	RES WW .36 OHM 5% 2W BWH	R1, R2
051			
052	3902	RES POT 5K OHM HORZ ADJ 10% .75W	R12

Table B-10. 25 kHz Card Option Replaceable Parts (Sheet 2 of 2) (Boschert SW100 used in HP 0950-1671)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
053			
054	14578	LABEL SMALL BOSCHERT MODEL/SER NO	
055			
056	13162	TRANSFORMER DRIVE XL400	T1
057			
058	13618-01	SCREW CAPTIVE PANEL .625" LG 6-32	
059			
060	1000	I C VOLT REG 723	U1
061	11247-19	SCREW P H 6-32 X 1.5 LG	L1, (REF)
062	7504	NUT HEX 6-32	L1, (REF)
063	7506	WASHER FLAT #6	
064	7549	WASHER FENDER	L1, (REF)
065			
066	7580	INSULATOR MICA TO-3	Q1, (REF)
067			
068	7588	WASHER SPLIT RING LOCK #6	
069	11828	WASHER METAL	Q2, (REF)
070	12298	INSULATOR TO-220	Q1, Q2, (REF)
071	7505	WASHER FLAT #4	Q1, Q2, (REF)
072	7577	WASHER SPLIT LOCK #4	
073	7584	SCREW F H 4-40 X 1/2	Q2, (REF)
074	11092-01	STANDOFF HEX 4-40 .250LG	
075	11837	INSULATOR CHOMERICS	Q2, (REF)

B.3 300-WATT SUPPLY

The 300-watt supply, Part No. 0950-1646 is used with the 16-slot backplane for the Micro/1000 computers. The supply operates from either 115 Vac or 230 Vac. There are four fans for cooling (two fans blow across the supply and two fans blow through the I/O card cage). The fans plug into either connector J3 for 115 Vac operation or into J2 for 230 Vac operation.

The supply has four dc outputs at +5V, +12V, -12V and +28V (backup battery source). The power supplies for the battery backup (BB) 5M voltage and the 25 kHz ac outputs are provided by separate optional cards that plug into the backplane. The main supply generates a 25 kHz square wave that is input to the 25 kHz sine-wave card as the source for its sine-wave output. The 25 kHz sine wave is used as a power source for certain I/O cards. A block diagram of the 300-watt supply is shown in Figure B-8.

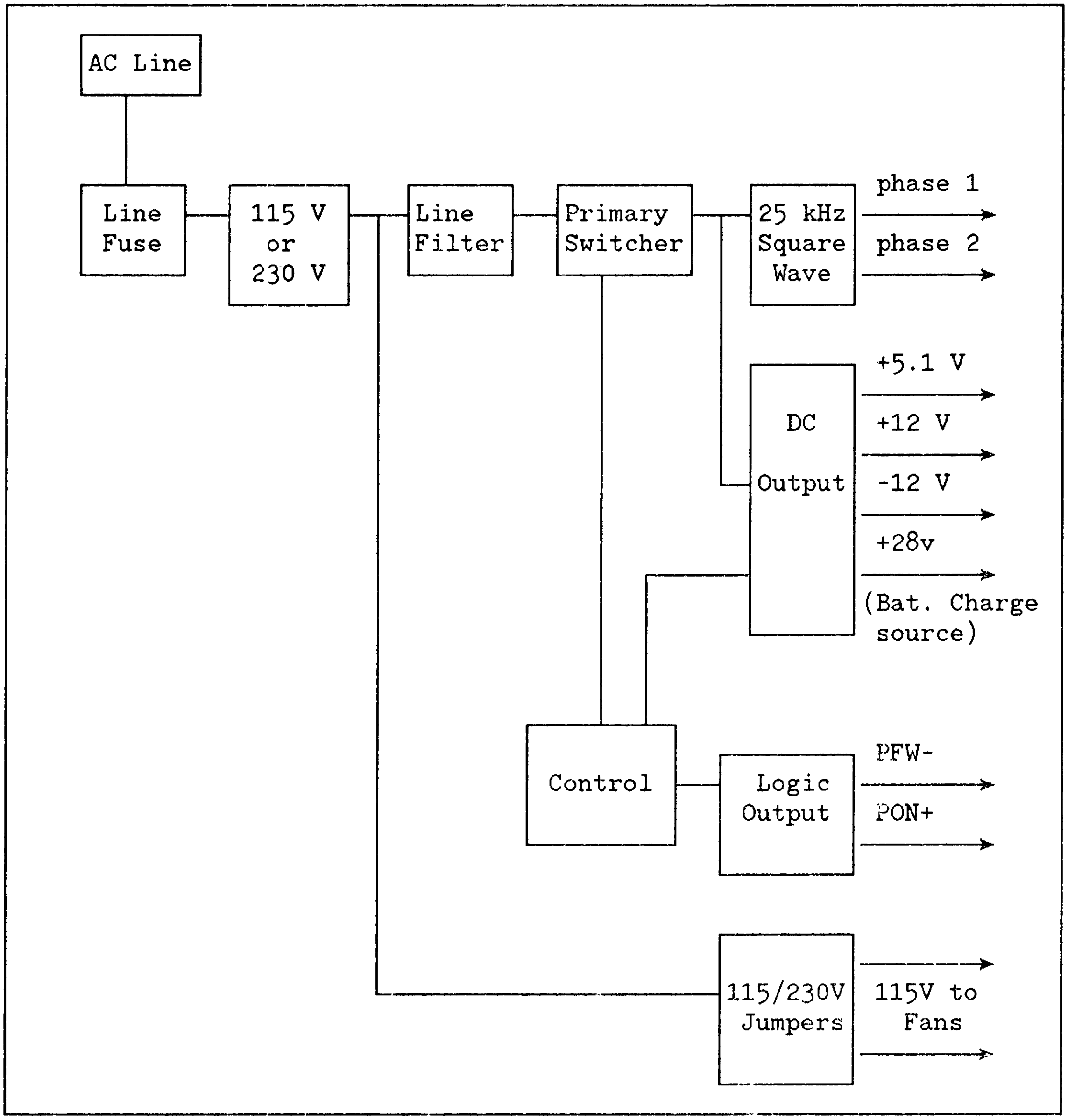

Figure B-8. 300-Watt Power Supply Block Diagram

B.3.1 LOGICAL SIGNALS

The power supply logical control signals to the computer are the same as for the 440-watt supply described in the previous subsection, except that the MLOST- signal goes directly from the battery backup card to the backplane rather than through the power supply as in the case of the 440-watt supply.

B.3.2 MECHANICAL SPECIFICATIONS (300W Supply)

The overall mechanical dimensions and connector locations of the 0950-1646 supply are shown in Figure B-9. The power supply connectors are shown schematically in Figure B-10. The connector specifications are given in Table B-11.

The cooling air flow should be a minimum of 40 CFM of air flowing across the power board in the direction indicated in Figure B-9. Power supply assembly diagrams are provided at the rear of this section of the manual.

Table B-11. Connector Specifications (300W Supply)

CONNECTOR	PART NO.	
P1	4-582390-4	(AMP)
J2	207378-1	(AMP)
J3	207378-1	(AMP)
J4	EAC-303	(SWITCHCRAFT)

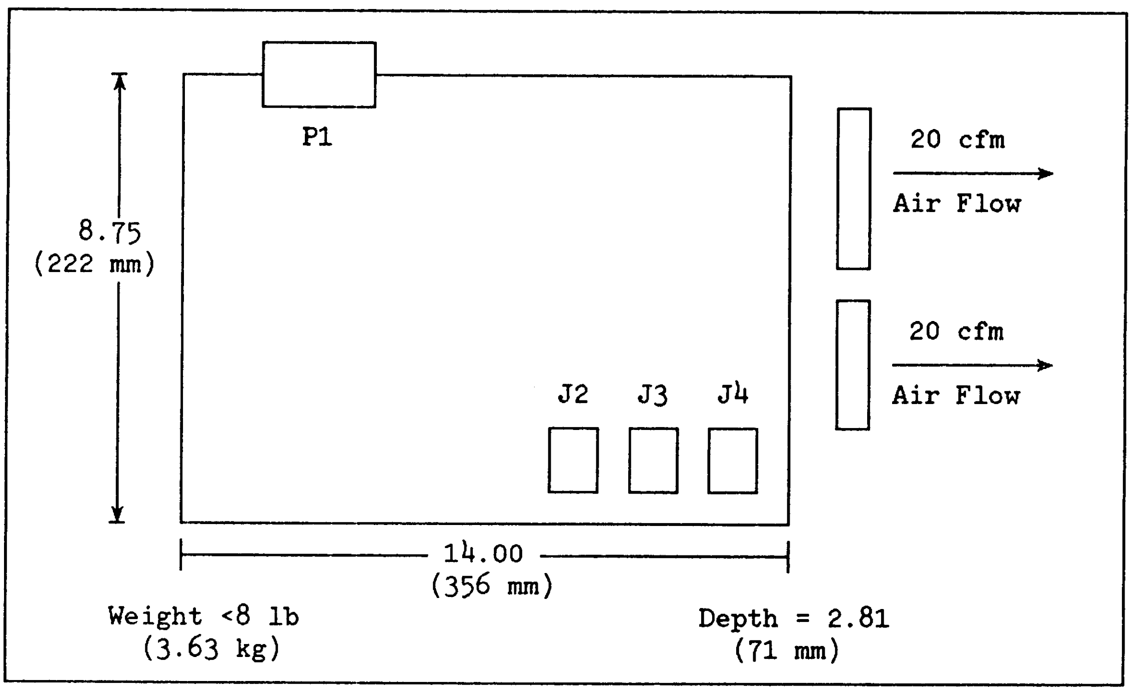

Figure B-9. Dimensions and Connector Locations (300W Supply)

B.3.3 ELECTRICAL CONNECTIONS (300W Supply)

The electrical contacts for the 300-watt power supply are provided by a plug and three jacks. The plug inserts into a jack on the backplane and the jacks are for the fans and ac input. A power supply connector diagram is shown in Figure B-10. The electrical connector definitions are given in Table B-12.

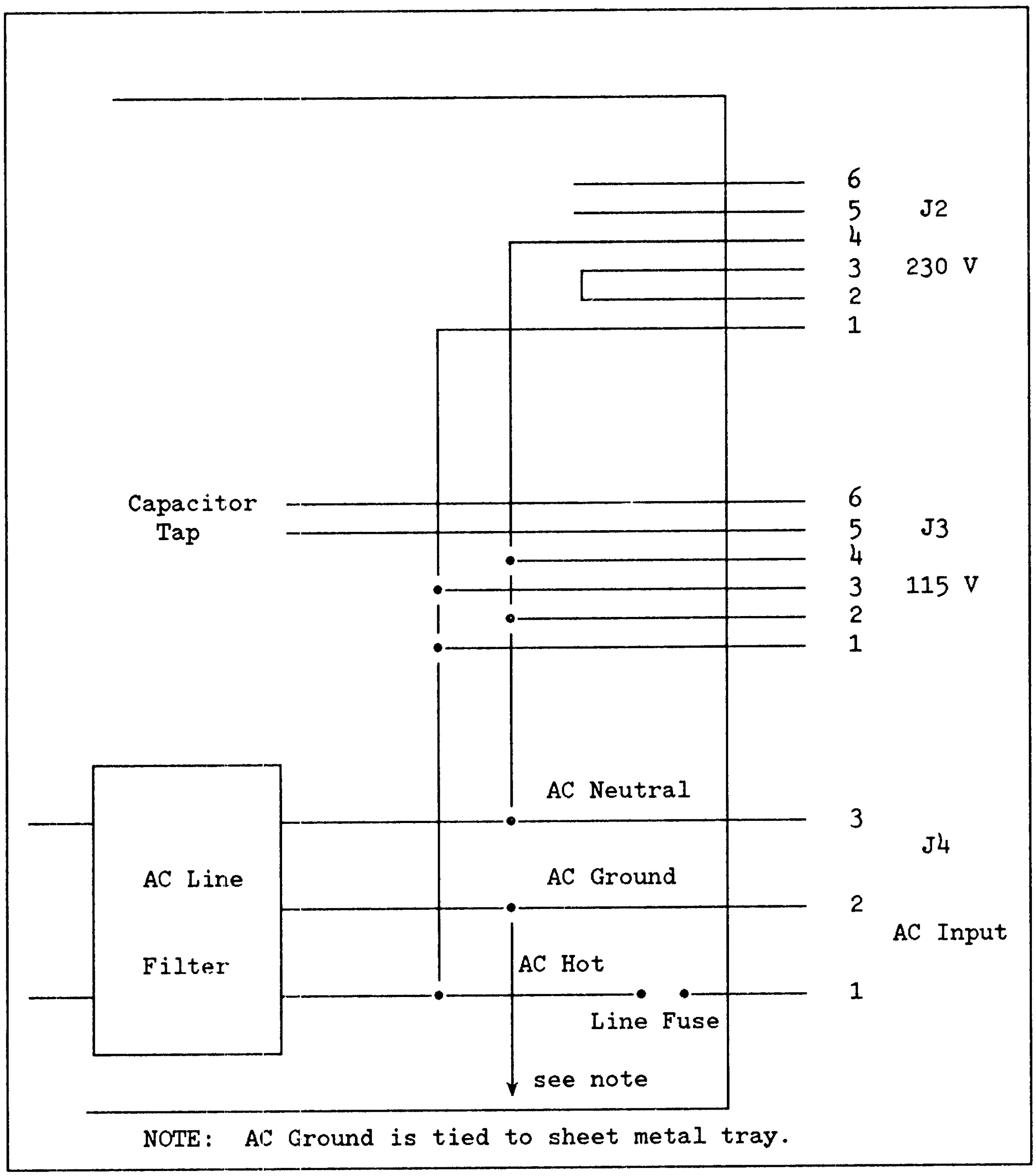

Figure B-10. 300-Watt Power Supply Connector Diagram

Table B-12. Electrical Connections (300W Supply)

ELECTRICAL CONNECTOR PIN DEFINITIONS	
P1 DC OUTPUT CONNECTOR	
Pin Number	Signal Name
24 thru 35	+5.1 Volts
10 thru 23	Common
6 thru 8	+12 Volts
5	-12 Volts
9	+28 Volts
3	25 KHz Phase 1
4	25 KHz Phase 2
1	PON+
2	PFW-
J4 AC LINE INPUT	
Pin Number	Signal Name
1	AC Line
2	AC Ground
3	AC Neutral
Pin 2 of this input connector must be tied to the sheet metal base.	
J2/J3 AC LINE CONFIGURATION / FANS	
Pin Number	Signal Name
1	Fan #1
2	Fan #1
3	Fan #2
4	Fan #2
5	230V / 115V
6	230V / 115V

B.3.4 ELECTRICAL SPECIFICATIONS (300W Supply)

The electrical specifications of the 300-watt supply are provided in the tables below. Ac line input specifications are given in Table B-13, and supply output specifications are given in Table B-14.

Table B-13. Input Electrical Specifications (300W Supply)

AC LINE SPECIFICATIONS

These specifications do not include the power required for the fans.

	Min	Nominal	Max	
Range 1				
Voltage	84	115	140	Volts RMS
RNS Current (Max)	5.7	4.5	4.3	Amps
Inrush	-	-	102	Amps
Range 2				
Voltage	168	230	280	Volts RMS
RMS Current (Max)	2.8	2.3	2.1	Amps
Inrush	-	-	204	AMps
Carry Over	16.0	-	-	mSec
PFW Trip Point				
Range 1	-	-	84	Volts RMS
Range 2	-	-	168	Volts RMS
Line Frequency	47	60	67	Hz
Line Fuse	-	-	10.0	Amps
Input Power (Not including fans)	-	-	400	Watts

Notes:

1. The line filter reduces conducted noise to 2 dBμV below the VDE 0871 Level B conducted emission specification. Conducted noise is measured with the power supply configured for 230 Vac operation and its output loaded for 300W by a resistive load. For 115 Vac operation of the supply, conducted noise must be 2 dBμV below the FCC Level B conducted emission specification.

2. Power supply operation permits input transients of up to 3000V for periods of not less than 10 μs.

Table B-14. Output Electrical Specifications (300W Supply)

Maximum Dynamic Load Change: 10% over 10 microseconds

Output Stress Conditions Allowed:

a. Supply will recover from a short to ground or to another regulated output and excessive ambient temperature.

b. Over rated operated temperature.

Output Regulation:

Note: For the following specifications to be valid Output #1 will have at least a 3.0 amp load. With a load less than 3.0 amps on Output #1, the maximum ripple on outputs #1, 2, 3, 4, and 6 must not exceed 1.5 volts peak to peak.

Output # 1	Nominal Voltage	5.1	Volts
	Maximum Current	50	Amps
Regulation	0.0 to 3.0 Amps	+10%	-10%
	3.0 to 6.2 Amps	+5%	-5%
	6.2 to 50.0 Amps	+2%	-2%
Ripple	Maximum Ripple	0.10	Volt
Output # 2	Nominal Voltage	12.0	Volts
	Maximum Current	7.0	Amps
Regulation	0.0 to .03 Amps	+10%	-10%
	.03 to 7.0 Amps	+6%	-3%
Turn-on Surge	9.0 Amps (for 10 sec. max.)	+6%	-30%
Ripple	Maximum Ripple	0.12	Volt
Output # 3	Nominal Voltage	-12.0	Volts
	Maximum Current	3.0	Amps
Regulation	0.0 to .10 Amps	+12%	-12%
	.10 to 3.0 Amps	+6%	-6%
Ripple	Maximum Ripple	0.12	Volt
Output # 4	Square Wave		

The Square Wave outputs must be in regulation when the load on +5.1 Volts is greater than 6.2 Amps.

	Min	Nominal	Max	
Phase to Phase	11.20	11.87	12.54	Volts RMS
Phase to Ground	5.60	5.94	6.27	Volts RMS
RMS Current	0.00	-	3.30	Amps/Phase
Frequency	24k	28k	32k	Hertz
Output Power	-	-	36	Watts

Table B-14. Output Electrical Specifications (300W Supply) (Continued)

Output # 5	Fan Power		
	Nominal Voltage	115	Volts RMS
	Maximum Current	1.25	Amps
Output # 6	Nominal Voltage	+28.0	Volts
	Maximum Current	2.50	Amps
Regulation	0.0 to 2.5 Amps	+20%	-20%
Ripple	Maximum Ripple	0.30	Volt

Note:
Although the sum of the maximums listed above exceeds the 300 watt specification of the power supply front end, not all of the outputs will be at maximum load at the same time and the actual power is 325-watts for a maximum of 10 seconds.

B.3.5 ENVIRONMENTAL SPECIFICATION (300W Supply)

The environmental specifications of the 0950-1671 300-watt supply are the same as for the 440-watt supply described in the subsection B.2 above.

B.3.6 REPLACEABLE PARTS (300W Supply)

Replaceable parts lists for the 300W power supply are provided in Table B-15 and they may be located in Figure B-11. The table and figures are located in the back of this section in front of the schematics.

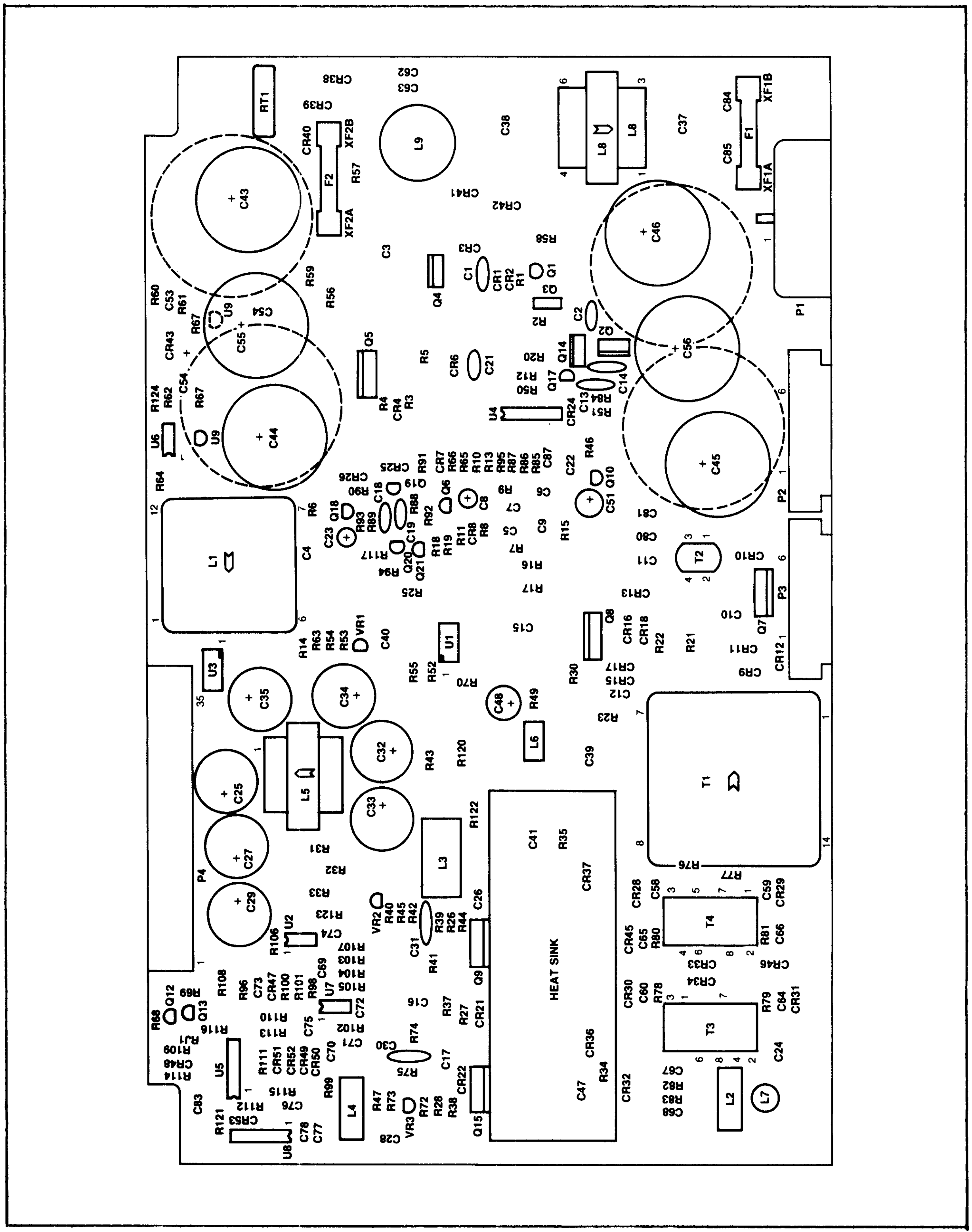

Figure B-11. Parts Locations for 300W Supply

Update 1

Table B-15. 300W Supply Replaceable Parts (Sheet 1 of 5)
(HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
001	14645	P C B XL301-5612	
002	14718	BRACKET L 300 WATT	
003	15009	STUD,LOCATING	
004	14732	HEATSINK XL301-5612	
005	15632-01	HEATSINK	Q5, S1, (REF)
006	15632-02	HEATSINK	Q7, Q8, (REF)
007	12012	HEATSINK TO-220	CR6, Q4, (REF)
008	14995	PLATE COVER	
009	2105	CAP CERM 100PF-1KV	C2
010	2000	CAP CERM .0047UF-1KV	C13, C14
011	2059	CAP CERM .01UF-100V	C18
012	2006	CAP CERM 150PF-1KV	C19
013	2008	CAP CERM .1UF-100V	C1, C41, C47
014	2062	CAP CERM 270PF-1KV	C21
015	2004	CAP CERM .1UF-16V	C30, C31
016			
017	15111-01	CAP SOLID ELECT 6.8uf 20% 25V RLDS	C11, C80, C81
018			
019	10346-05	CAP ELECT 47UF-16V RAD LDS	C51
020	10346-01	CAP ELECT 10UF-16V RAD LDS	C8
021	14992-01	CAP ELEC 1600UF 15V COMP GRLDS	C35
022	14993-01	CAP ELEC 570UF 40V COMP GRLDS	C27, C29, C32, C33, C34
023	15869-05	CAP ELEC 200V 1200UF 85deg C SNP IN	C43, C44, C45, C46, C55, C56
024	12939	CAP ELECT LO LEAK R LDS 100UF 10VDC	C23
025	14994-01	CAP ELEC 350UF 60V COMP GRLDS	C25
026			
027			
028	12951	CAP ELECT 10UF-100VDC LD ESR R LDS	C48
029			
030	15032-10	CAP F&F POLYC 0.68UF 400V 10% RLDS	C3
031	13593-07	CAP MET POLY .01UF 630/1000V 5%	C10
032	12685-03	CAP MET POLY 0.1UF 5% 63/100V	C4, C6, C69, C70, C71, C72, C73, C74, C75, C76
033	13279-07	CAP POLY RLD BOX .10UF 10% 250V	C5, C24, C39
034	12328-04	CAP MET POLY 0.22UF 63VDC 5%	C16, C17, C26, C28, C40
035	12685-07	CAP MET POLY .47UF 5% 63/100V	C7
036	13593-03	CAP MET POLY .0022UF 630/1000V 5%	C9, C87
037			
038	12328-08	CAP MET POLY 1.0UF 63VDC 5%	C83
039	11133-01	CAP MET POLY .1UF 100V 10% RLDS	C12, C53
040	2080	CAP MET POLY 2UF-200VDC 10%	C15
041			
042	15016-07	CAP F&F POLYC 1000PF 160VDC/100VAC	C58, C59, C60, C64, C65, C66, C67, C68
043	11133-03	CAP MET POLY .22UF 100V 10% RLDS	C22
044	12685-10	CAP MET POLY .022UF 5% 63/100V	C77, C78
045	13932-03	CAP MET EMI SUP X-CAP 1.00UF 250VAC	C37, C38
046			
047			
048			
049			
050	2021	CAP TANT 47UF-6V	C54
051	11414-02	CAP MET PAPER .0022UF 250VAC VDE AP	C62, C63, C84, C85
052	1038	DIODE GEN PUR 1A IN4004 400VDC	CR1, CR2, CR3, CR9, CR10, CR11, CR12

Table B-15. 300W Supply Replaceable Parts (Sheet 2 of 5) (HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
053	12594	DIODE SILICON CASE DO-35,IN4448	CR8, CR25, CR26, CR49, CR50, CR51, CR52, CR53
054	14990-01	DIODE FST RCV 9A 400V BYV29-400	CR6
055	10056-03	DIODE FAST RECV BYW 29-150	CR28, CR29
056			
057	10672	DIODE SCHOT STD POL 45V 60A SD-51	CR36, CR37
058	14482	DIODE DUAL SCHOT 20A 45V TO-220	CR32
059	12260-04	DIODE HI CUR AX LDS. 30V,6A SR3773	CR13
060	1021	DIODE HI CUR. AX LDS. 400V,6A MR754	CR38, CR39, CR41, CR42
061			
062			
063			
064	15088-01	DIODE FST RCV 3.5A 150V AXLD	CR33, CR34
065	14461-01	DIODE FST RECV 2A 100V AX LDS	CR4, CR15, CR16, CR17, CR18, CR30, CR31, CR45, CR46
066			
067	11356-15	DIODE ZENER 500MW 8.2V 5% IN5998B	CR7
068	1014	DIODE ZENER 500 MW 5.6V 5% IN5994B	CR40
069	10879	DIODE ZENER 400MW 68V 5% IN5266B	CR21, CR22
070	1008	DIODE ZENER 400MW 15V 5% IN965A	CR24
071	1056	DIODE ZENER 500MW 5.1V 5% IN5993B	CR43, CR47, CR48
072			
073			
074	7015	FUSE CLIP PCB TYPE FOR 3AG FUSE	XF1A, XF1B, XF2A, XF2B
075	10180-01	FUSE 5A-250V NORMAL-BLOW	F2
076	10865	FUSE 10 AMP 250V (BUSS ABC10)	F1
077			
078	12472	RECEPTACLE AC RT ANGLE 6A 250V	P1
079	15001-01	CONN IN LINE RT ANG PIN HDR 6 POS	P2, P3
080	14987-01	CONN RT ANG PCB 35 POS	P4
081			
082	13733	INDUCTOR 4MH	L1
083	14033	INDUCTOR PWDR IRON 3.4UH @ 6A	L4
084	14034	INDUCTOR PWDR IRON 5UH 10A	L3
085	15115	INDUCTOR 5V	L5
086	10799	INDUCTOR 18 UH	L6
087	14850	BALUN SUPER E-375 XL301	L8
088	15012	BALUN TOROIDAL 2x1mh XL301	L9
089	12209	INDUCTOR AIR CORE	L7
090	11944	INDUCTOR 18UH MIN.	L2
091			
092	12592	TRANS PNP CASE TO-92,MPS 2907A	Q1, Q6, Q18
093	1005	TRANS NPN POWER TIP-50	Q2, Q14
094	12675	TRANS PNP HI VOLT 400V TO-126 CASE	Q3
095			
096	1118	TRANS NPN POWER MJE13007	Q4
097			
098	1016	TRANS PNP CASE TO-92 2N4126	Q17
099	14988-02	TRANS NPN POWER 15A 1000V BUW 13A	Q5, Q7, Q8
100	14263-01	TRANS NPN POWER DARLING 10A TIP 140	Q9, Q15
101	13595	TRANS N-CHANNEL POWER FET VN10KM	Q12, Q13
102	12591	TRANS NPN CASE TO 92 2N4124	Q10, Q19, Q20, Q21
103			
104			

Table B-15. 300W Supply Replaceable Parts (Sheet 3 of 5) (HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
105			
106	3081	OBSOLETE(RES 2.4K OHM 1/4W)	R14, R54
107	3124	OBSOLETE(RES 150K OHM 1/4W)	R50, R51
108	3108	OBSOLETE(RES 33K OHM 1/4W)	R65, R88, R90
109	3099	OBSOLETE(RES 13K OHM 1/4W)	R66
110	3088	OBSOLETE(RES 4.7K OHM 1/4W)	R85
111	3072	RES CF 1K OHM 5% 1/4W	R86, R87
112	3110	OBSOLETE(RES 39K OHM 1/4W)	R84
113			
114			
115	10318-47	OBSOLETE(RES 180 OHM 1/4W)	R27, R28
116	3064	OBSOLETE(RES 470 OHM 1/4W)	R1, R53
117	3024	OBSOLETE(RES 10 OHM 1/4W)	R6, R34, R35, R76, R77, R78, R79, R80, R81, R82, R83
118	3098	OBSOLETE(RES 12K OHM 1/4W)	R7, R117
119	3080	OBSOLETE(RES 2.2K OHM 1/4W)	R8, R30, R67, R60
120			
121	3046	OBSOLETE(RES 82 OHM 1/4W)	R9
122	3104	OBSOLETE(RES 22K OHM 1/4W)	R10
123	3096	OBSOLETE(RES 10K OHM 1/4W)	R11, R45, R47, R63, R68, R69, R93, R100, R101, R116, R124
124			
125	3048	OBSOLETE(RES 100 OHM 1/4W)	R13
126	3020	OBSOLETE(RES 6.8 OHM 1/4W)	R95
127	3135	OBSOLETE(RES 430K OHM 1/4W)	R19
128			
129			
130	3128	OBSOLETE(RES 220K OHM 1/4W)	R62
131	3069	OBSOLETE(RES 750 OHM 1/4W)	R64
132			
133			
134	3092	OBSOLETE(RES 6.8K OHM 1/4W)	R40, R75
135	3089	OBSOLETE(RES 5.1K OHM 1/4W)	R109, R114
136	10318-102	OBSOLETE(RES 1.2 OHM 1/4W)	R49
137	3084	OBSOLETE(RES 3.3K OHM 1/4W)	R39, R73
138			
139	3106	OBSOLETE(RES 27K OHM 1/4W)	R37, R42
140	3100	OBSOLETE(RES 15K OHM 1/4W)	R46
141	3079	OBSOLETE(RES 2.0K OHM 1/4W0	R103, R104, R112
142			
143			
144	3060	OBSOLETE(RES 330 OHM 1/4)	R26, R38, R52
145	3120	OBSOLETE(RES 100K OHM 1/4W)	R89, R111
146	3130	OBSOLETE(RES 270K OHM 1/4W)	R92
147	3122	OBSOLETE(RES 120K OHM 1/4W)	R91
148			
149	10328-34	OBSOLETE(RES 680K OHM 1/4W)	R102, R105
150	10328-36	OBSOLETE(RES 820K 1/4W)	R110
151	10328-45	OBSOLETE(RES 2M OHM 1/4W)	R121
152			
153	10232-17	RES MET OXIDE 22 OHM 5% 1 W	R23
154	3336	RES CF 470K OHM 5% 1/2W	R12
155	10304-71	RES CF 1.8K 5% 1/2W	R44, R72

Table B-15. 300W Supply Replaceable Parts (Sheet 4 of 5)
(HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
156			
157			
158	11313-01	RES MF 1.0K OHMS 1% 1/8W	R94
159	11891-6491	RES MF 6.49K OHMS 1% 1/4W	R61
160	13598-08	RES MF UNCUT LDS 365K 1% 1/8W	R18
161	11891-4873	RES MF 487K OHMS 1% 1/4W	R59
162	10318-88	OBSOLETE(RES 9.1K OHM 1/4W)	R98
163			
164			
165	10966-49	RES WW 1K OHM 10% 2W BWH	R31
166	10232-95	RES MET OXIDE 47K OHM 5% 1 W	R20
167			
168	3825	RES WW 470 OHM 5% 2W BWH	R96
169	10233-78	RES MET OXIDE 15K OHM 5% 2W	R2, R22
170	10233-84	RES MET OXIDE 27K OHM 5% 2W	R21, R57, R58
171	11313-40	RES MF 2.55K OHMS 1% 1/8W	R99, R107
172	11313-35	RES MF 2.26K OHMS 1% 1/8W	R106
173	10232-60	RES MET OXIDE 1.3K OHM 5% 1W	R108
174	11306-51	RES MF 332K OHMS 1% 1/8W	R113
175	11306-93	RES MF 909K OHMS 1% 1/8W	R115
176			
177			
178	3828	RES WW .30 OHM 5% 2W BWH	R17
179	3809	RES WW .33 OHM 5% 2W BWH	R16
180	10967-41	RES WW 47K OHM 5% 5W	R56
181	3811	RES WW 10 OHM 10% 1W BW20F	R3, R4
182	3820	RES WW 120 OHM 5% 2W BWH	R32, R33, R122, R123
183	3812	RES WW 82 OHM 10% 1W BW20F	R5
184	3208	RES CF 2.2 OHM 5% 1/2W	R15
185	3903	RES WW 10 OHM 5% 5W	R25, R43, R120
186			
187			
188			
189	10519-12	RES POT 5K OHM VADJ STURN .5W CERM	R55
190	10519-10	RES POT 2K OHM VADJ STURN .5W CERM	R41, R74
191			
192	3938	RES THERMISTOR DISC 5 OHM 15% ST LD	RT1, RT2
193	13462	RES WIRE WW ZEROHM JUMPER WIRE 25A	RJ1
194			
195	3911	THERMOSTAT SNAP-ACTING AUTO RESET	S1
196	10422-11	WIRE RED 22 AWG 5"LG 1/4 X 1/4	S1, (REF)
197	7480	WIRE RED 18 AWG 1.50" (1/4 X 1/4)	T2, (REF)
198			
199	14729	TRANSFORMER XL301 VDE/RFI	T1
200	12871-02	TRANSFORMER PC MT SINGLE CORE 5T	T2
201	14923	TRANSFORMER TOROIDAL XL301	T3, T4
202			
203	12977	OPTO-RESISTOR MATCHED VDE	R70, U1
204			
205	13363	I C CMOS D PREC MONO MULTI CD4538BE	U8
206	11498	I C OPTO-ISOLATOR OP1-1264B	U3
207	14984-01	I C VOLT REF PREC 2.5V 1% MDIP	U2

Table B-15. 300W Supply Replaceable Parts (Sheet 5 of 5)
(HP 0950-1646, Boschert XL0301-5612)

ITEM NO.	COMPONENT PART NUMBER	DESCRIPTION	REFERENCE DESIGNATORS
208	14985-01	I C VOLT REF 2.5V 2% TO-92	U9
209	10505	I C LOW POWER DUAL VOLT COMP LM393N	U7
210	12219	I C OP AMP VCOMP 8 PIN MDIP LM392N	U6
211	13437	I C QUAD 2 IN SCHMITT TRIG CD4093BE	U5
212	1000	I C VOLT REG 723	U4
213	7500	TIE WRAP SMALL	S1, (REF)
214	12540	I C ADJ PREC SHUNT REG TO 92	VR1, VR2, VR3
215	7694-2	NUT KEPS CONICAL 1/4-28	CR36, CR37, (REF)
216	6009	PIN MALE BEAD .65 LG .095 DIA	E1, E2, E5
217	14957-03	JUMPER TERMINAL FEMALE	JP4
218	15696	SPRING CLIP HDWR CNDCT 12012 HTSINK	Q4, (REF)
219	11092-01	STANDOFF HEX 4-40 .250LG	P1, (REF)
220	15695	SPRING CLIP HDWR NCNDCT 12012 H/S	CR6, (REF)
221	10915	STD MTG HDW PC BD SUPPORT NYLON	
222	7501	TIE WRAP MEDIUM	
223	15451-01	STIFFENER 1.25 X 4.25" LG	C43, C44, C45, C46, C55, C56, (REF)
224	11319	RETAINING RING EXTERNAL	CR36, CR37, (REF)
225	12569	LABEL,CSA MARK	L-BRKT, (REF)
226			
227	15081-01	HANDLE .25DIA 3.0LG 1.0H 6/32THD	
228	12459	LABEL FUSE WARNING	C46, (REF)
229	14996	LABEL 115 VAC / 230 VAC	L-BRKT, (REF)
230	7740	LABEL DANGER HIGH VOLTAGE	C43, (REF)
231	7881	LABEL SERIAL NO.	T1, (REF)
232			
233	15640	SPRING CLIP HDWR (NCNDCT) TO218/220	CR32, Q7, Q8, Q9, Q15, (REF)
234	7578	SCREW P H 4-40 X 1/4	S1, (REF)
235	7511	SCREW P H 6-32 X 1/2	
236	7506	WASHER FLAT #6	
237	7588	WASHER SPLIT RING LOCK #6	
238	7577	WASHER SPLIT LOCK #4	P1, S1, L-BRKT, (REF)
239	7505	WASHER FLAT #4	P1, L-BRKT, (REF)
240	10366-01	WIRE RED 16 AWG 8" (1/4 X 1/4)	JP2, JP3
241	15633	SPRING CLIP HDWR CNDCT TO-218/220	Q5, (REF)
242	11661-01	SPACER GLASS .225 OD .067 ID .185TH	RT1, RT2, R21, R57, R58, (REF)
243	7202	0.0040RTV 108 CLEAR	L6, L7, C15, C43, C44, C45, C46, C55, C56, (REF)
244	15239	LABEL WARNING	L-BRKT, (REF)
245	15240	LABEL INFORMATION (WARNING)	L-BRKT, (REF)
246	15742	LABEL CUSTOMER I D	L-BRKT, (REF)
247	7737	0.0010LOCKTITE	
248	12891-03	PEM STUD 4-40 THREAD .625 LG	P.C. B.D., (REF)
249	7508	SCREW P H 4-40 X 3/8	L-BRKT, (REF)

B.4 HP 12154A BATTERY BACKUP MODULE

The HP 12154A battery backup module for the Micro/1000 computers is designed to provide current that will retain the current status of the system in memory if ac power is interrupted. The Hewlett-Packard part number for this card is 12154-60001. The schematic for this card is shown in Figure B-12.

B.4.1 CONFIGURATION

The battery backup module is installed in the 16-slot backplane of the Micro/1000 A-Series computers. The sixth, seventh, and eighth physical slots down from the top of the left side of the card cage are dedicated to the battery backup module. There are three slots reserved to account for the height of the batteries and the space necessary for component heat sinks.

B.4.2 PHYSICAL DESCRIPTION

The module (or card) dimensions are the following:

Width: 6.75 inches (171 mm) Standard card width

Depth: 12.75 inches (324 mm) Attaches to bulkhead connector panel

Max. Component Height: 2.0 inches (51mm) for D-size battery packs

B.4.3 ELECTRICAL SPECIFICATION

The module is comprised of the battery charging circuit, enable/disable circuit, D-size battery pack, and a control circuit. When power is present, the module will charge the 9.6V Nicad (nickel/cadmium) batteries. When power fails, the 9.6V battery voltage is reduced to 5.1V through the regulator, and supplies the +5M power line to sustain memory.

The module derives its power from the 12V dc output of the system power supply. When the voltage of the batteries drops below 8.0V, the module will inhibit the +5.1V memory regulator circuit.

B.4.4 THEORY OF OPERATION

The internal battery pack is charged from both 28V and 12V. The 12V backplane voltage is used to provide a heavy charge for discharged batteries. As the batteries charge to about 11.3V, the 28V supply is used as a trickle charger. The input selector is essentially three diodes that select the highest input voltage. Note the 28V supply would be the normal input, until a power fail when the batteries would become the input. This is important because the output of this circuit, +5VM, is produced by the circuitry on this PCA. Thus to determine if the battery or PCA is at fault, the battery pack can be disabled by turning off the battery enable switch on the front panel, and if the +5VM is present the battery pack is probably at fault (if the 28V and 5V voltages are present).

The DC to DC converter, coupled with the control circuit, make this a switching power supply. The control block switches the DC input voltage to maintain a pulse width with a constant amount of power. Thus, a 28V input will have a tall narrow pulse, a 8V input will have a low wide pulse. The pulses feed an inductor that creates a constant voltage output for a capacitor-resistor integrator that produces the +5VM. This supply will stop if the battery voltage drops below 8V (to protect the Nicad batteries) and will shut down if an over current condition exists. The 2.5V reference has a +/- accuracy of 0.5%. The feedback circuit drives the control block to regulate the pulse width of the DC to DC converter. Overall voltage regulation is 2%

The battery charger circuit consists of four parts. Diode CR2 is connected to the +12V supply and to a 10 ohm resistor R2. R2 is connected to the positive side of the battery. Diode CR1 is similarly connected to +28V and 100 ohm resistor R1 which is also connected to the positive battery connection. Diode CR2 conducts until the battery voltage approaches 11.3V. CR2 becomes reverse biased and CR1 now trickle charges the battery. Because of the simplicity of this scheme, if a battery does not retain a charge the battery pack is probably faulty.

Also on the front of this PCA are two LEDs, one green and one red. The red LED indicates that an overcurrent or overvoltage condition has occurred and the battery backup card is shutdown. This could be caused by a short in the +5VM line that goes to memory. Either a memory PCA, a processor PCA or the backplane could be faulty, as well as the battery backup PCA itself. To reset after isolating and repairing the problem, turn off the battery enable switch, turn off the power, then turn both back on.

The green LED indicates the +5VM is within specifications. If both red and green LEDs are on, the battery backup PCA is faulty. As long as the green LED is on, the memory is being sustained.

B.4.5 REPLACEABLE PARTS

Replaceable parts for the HP 12154A are listed in Table B-16 and a parts location diagram for it is shown in Figure B-13. The parts manufacturer's names and addresses are listed in the Manufacturer's Code List below.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03508	GE Co Semiconductor Prod Dept	Auburn, NY	13201
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
12969	Unitrode Corp	Watertown, MA	02172
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
31585	RCA Corp Solid State Div	Somerville, NJ	08876
56289	Sprague Electric Co.	North Adams, MA	01247
75915	Littlefuse Inc	Des Plaines, IL	60016

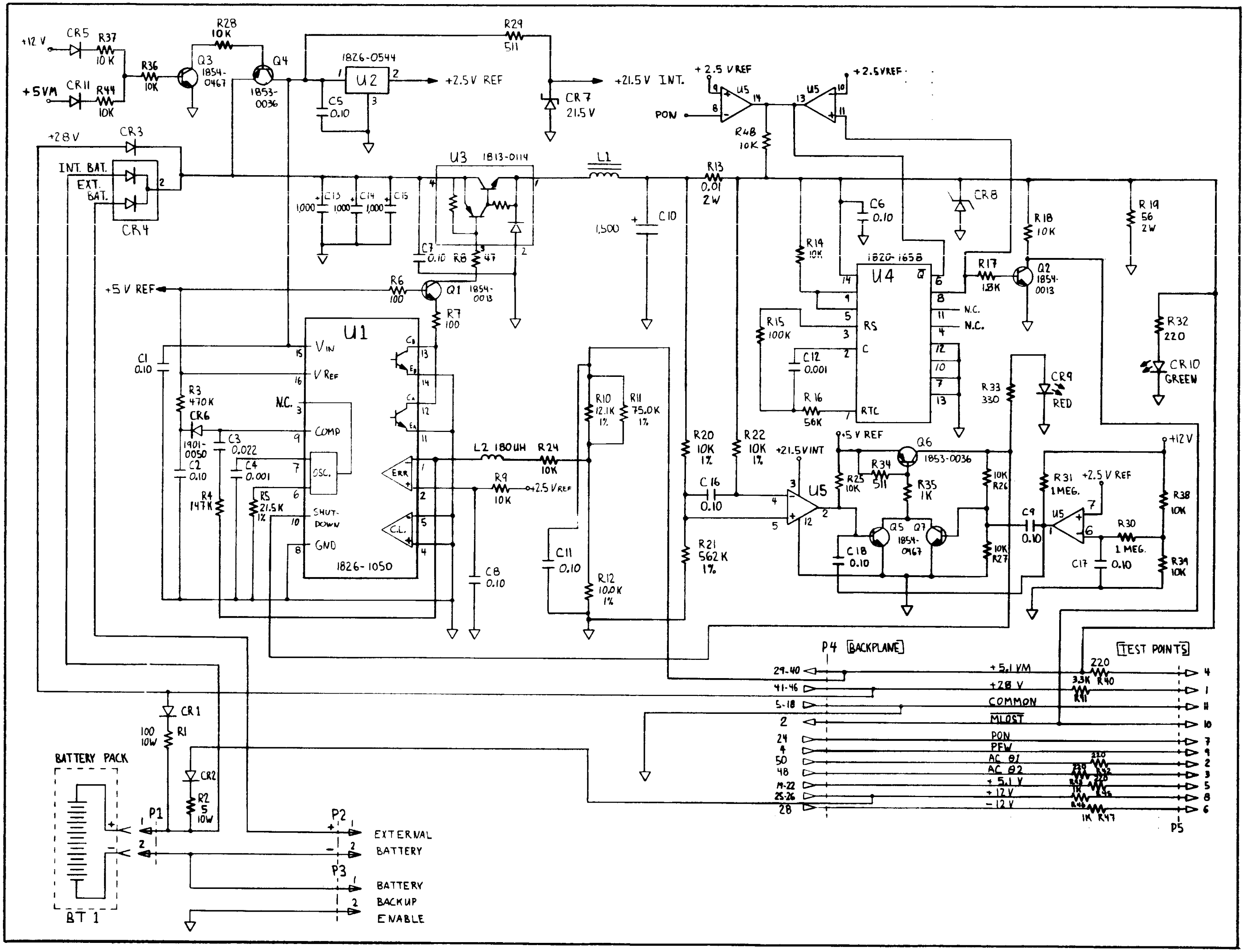

Figure B-12. HP 12154A Battery Backup Module Schematic

Update 1

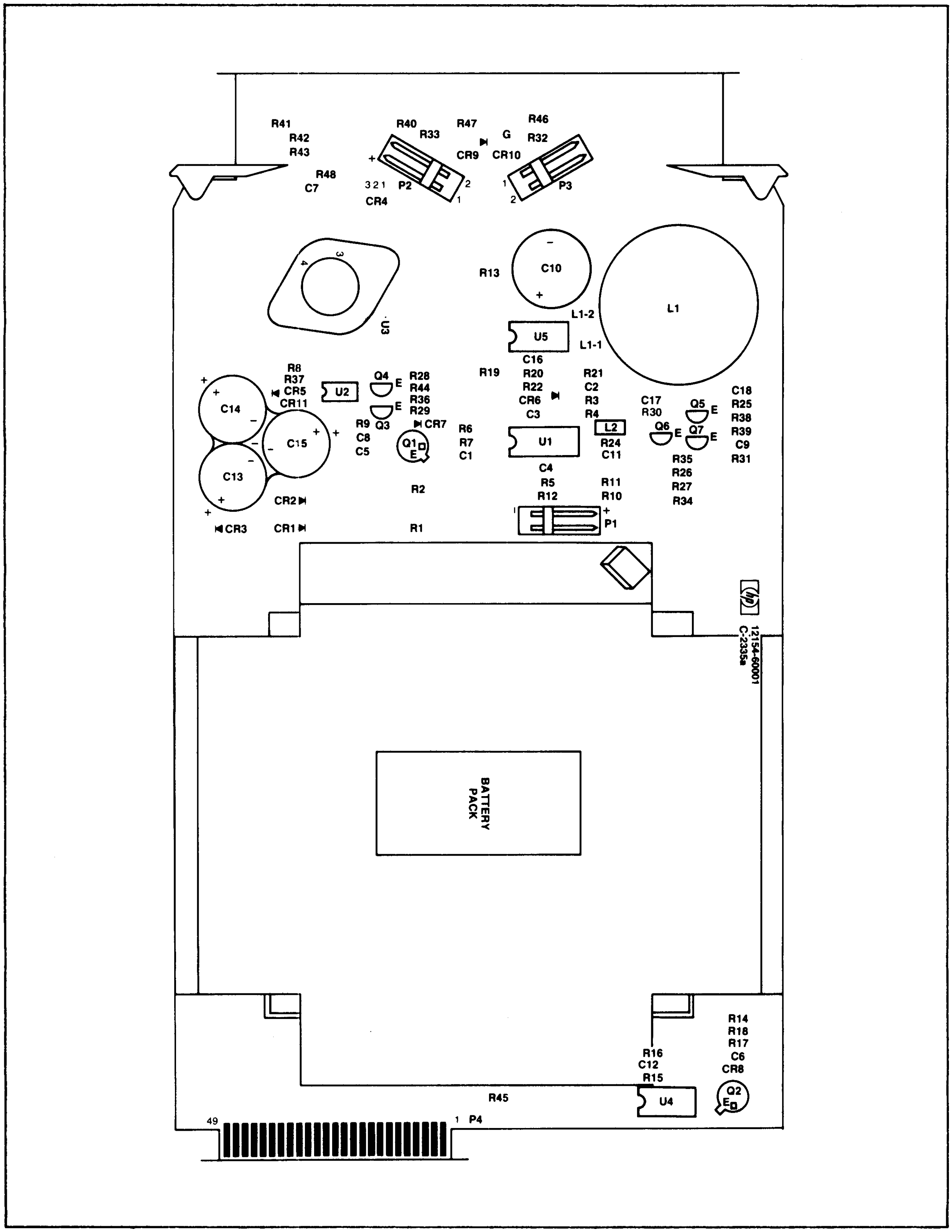

Figure B-13. HP 12154A Replaceable Parts Location Diagram

Update 1

Table B-16. HP 12154A Replaceable Parts (Sheet 1 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12154-60001	3	1	PCA-BACKUP	28480	12154-60001
B1	1420-0321	1	1	BATTERY ASSEMBLY 9.6V NOM; RECHARGEABLE	28480	1420-0321
C1	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C2	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C3	0160-4833	5		CAPACITOR-FXD .022UF +-10% 100VDC CER	28480	0160-4833
C4	0160-4847	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4847
C5	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C6	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C7	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C8	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C9	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C10	0180-2997	0	1	CAPACITOR-FXD 1500UF+100-10% 25VDC AL	56289	674D158H025HJ5A
C11	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C12	0160-4847	1		CAPACITOR-FXD 1000PF +-10% 100VDC CER	28480	0160-4847
C13	0180-3019	9	3	CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C14	0180-3019	9		CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C15	0180-3019	9		CAPACITOR-FXD 1000UF+50-10% 50VDC AL	28480	0180-3019
C16	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C17	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
C18	0160-4835	7		CAPACITOR-FXD .1UF +-10% 50VDC CER	28480	0160-4835
CR1	1901-0673	6	3	DIODE-PWR RECT 100V 5A 5US	03508	A15A
CR2	1901-0673	6		DIODE-PWR RECT 100V 5A 5US	03508	A15A
CR3	1901-0673	6		DIODE-PWR RECT 100V 5A 5US	03508	A15A
CR4	1906-0265	2	1	DIODE-RECT.	28480	1906-0265
CR5	1901-0050	3	4	DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR6	1901-0050	3		DIODE-SWITCHING 80V 200MA 2NS DO-35	28480	1901-0050
CR7	1902-3245	6	1	DIODE-ZNR 21.5V 5% DO-35 PD=.4W	28480	1902-3245
CR8	1902-0939	9	1	DIODE-ZNR 5V PD=5W TC=+.06% IR=300UA	11961	1N5908
CR9	1990-0486	6	1	LED-LAMP LUM-INT=1MCD IF=20MA-MAX BVR=5V	28480	5082-4684
CR10	1990-0485	5	1	LED-LAMP LUM-INT=800UCD IF=30MA-MAX	28480	5082-4984
CR11	1901-0460	9	2	DIODE-STABISTOR 30V 150MA DO-7	28480	1901-0460
L1	9140-0811	8	1	INDUCTOR 356UH 10% 1.7DX1.2LG	28480	9140-0811
L2	9100-2279	2		INDUCTOR RF-CH-MLD 180UH 10% .105DX.26LG	28480	9100-2279
Q1	1854-0013	7	2	TRANSISTOR NPN 2N2218A SI TO-5 PD=800MW	04713	2N2218A
Q2	1854-0013	7		TRANSISTOR NPN 2N2218A SI TO-5 PD=800MW	04713	2N2218A
Q3	1854-0467	5	3	TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q4	1853-0036	2	2	TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
Q5	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
Q6	1853-0036	2		TRANSISTOR PNP SI PD=310MW FT=250MHZ	28480	1853-0036
Q7	1854-0467	5		TRANSISTOR NPN 2N4401 SI TO-92 PD=310MW	03508	2N4401
R1	0811-3644	5	1	RESISTOR 100 10% 10W PW TC=0+-300	28480	0811-3644
R2	0811-3656	9	1	RESISTOR 5 10% 10W PW TC=0+-300	28480	0811-3656
R3	0683-4745	6	2	RESISTOR 470K 5% .25W FC TC=-800/+900	01121	CB4745
R4	0698-3452	1	2	RESISTOR 147K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1473-F
R5	0757-0199	3		RESISTOR 21.5K 1% .125W F TC=0+-100	24546	C4-1/8-T0-2152-F
R6	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R7	0683-1015	7		RESISTOR 100 5% .25W FC TC=-400/+500	01121	CB1015
R8	0683-4705	8		RESISTOR 47 5% .25W FC TC=-400/+500	01121	CB4705
R9	0683-1035	1	26	RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R10	0757-0444	1		RESISTOR 12.1K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1212-F
R11	0757-0462	3	2	RESISTOR 75K 1% .125W F TC=0+-100	24546	C4-1/8-T0-7502-F
R12	0757-0442	9	8	RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R13	0811-3511	5	1	RESISTOR .01 1% 2W PWW TC=0+-150	28480	0811-3511
R14	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R15	0683-1045	3		RESISTOR 100K 5% .25W FC TC=-400/+800	01121	CB1045
R16	0683-5635	5		RESISTOR 56K 5% .25W FC TC=-400/+800	01121	CB5635
R17	0683-1825	7		RESISTOR 1.8K 5% .25W FC TC=-400/+700	01121	CB1825
R18	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R19	0764-0013	5	1	RESISTOR 56 5% 2W MO TC=0+-200	28480	0764-0013
R20	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R21	0698-8824	1		RESISTOR 562K 1% .125W F TC=0+-100	28480	0698-8824
R22	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R24	0757-0442	9		RESISTOR 10K 1% .125W F TC=0+-100	24546	C4-1/8-T0-1002-F
R25	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R26	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R27	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R28	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R29	0757-0416	7	4	RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R30	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055
R31	0683-1055	5		RESISTOR 1M 5% .25W FC TC=-800/+900	01121	CB1055

Table B-16. HP 12154A Replaceable Parts (Sheet 2 of 2)

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
R32	0683-2215	1	10	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R33	0683-3315	4		RESISTOR 330 5% .25W FC TC=-400/+600	01121	CB3315
R34	0757-0416	7		RESISTOR 511 1% .125W F TC=0+-100	24546	C4-1/8-T0-511R-F
R35	0683-1025	9	6	RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R36	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R37	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R38	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R39	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R40	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R41	0683-3325	6	2	RESISTOR 3.3K 5% .25W FC TC=-400/+700	01121	CB3325
R42	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R43	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R44	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
R45	0683-2215	1		RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
R46	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R47	0683-1025	9		RESISTOR 1K 5% .25W FC TC=-400/+600	01121	CB1025
R48	0683-1035	1		RESISTOR 10K 5% .25W FC TC=-400/+700	01121	CB1035
U1	1826-1050	5	1	IC V RGLTR-SWG 4.9/5.1V 16-DIP-P PKG	28480	1826-1050
U2	1826-0544	0	1	V REF 8-DIP-C	04713	MC1403U
U3	1813-0114	3	1	IC V RGLTR TO-3	12969	PIC645
U4	1820-3516	0	1	IC TIMER CMOS	28480	1820-3516
U5	1826-0138	8	1	IC COMPARATOR GP QUAD 14-DIP-P PKG	01295	LM339N

B.5 HP 12159A 25 kHz POWER MODULE

The HP 12159A is a module that takes the 25 kHz square-wave power from the 300W power supply and provides 25 kHz sine-wave power to the 16-slot backplane of a Micro/1000 computer for distribution to certain I/O cards having on-card power supplies. The module plugs into slot 8 of the backplane, and does not need forced air flow for cooling.

The Hewlett-Packard part number for this module is 12159-60001.

B.5.1 HP 12159A SPECIFICATIONS

The HP 12159A electrical specifications are provided in Table B-17, and the connector pin definitions are listed in Table B-18.

Table B-17. HP 12159A 25-kHz Module Electrical Specifications

Input Specifications:

	Min	Nominal	Max	
Phase to Phase	11.28	12.00	12.72	Volts rms
RMS Current (max)	0.00	-	3.20	Amps
Frequency	24	25	32	kHz
Input Power	-	-	36	Watts

Output Specifications:

Maximum output power	30 Watts
Maximum distortion	10% total harmonic distortion
Maximum dynamic load change	10% of load over 10 microseconds

Output Stress Conditions:

The module shall recover, with no permanent damage from a shorted regulated output (it may be necessary to replace the fuse to resume normal operation)

Output Loading:

The load on the 25 kHz module can be applied from phase-to-phase (39 Vrms) or from phase-to-common (19.5 Vrms). Up to one half of the maximum rated power can be drawn from each phase (phase-to-common) or up to all of the rated power can be drawn phase-to-phase as long as the total power does not exceed the maximum rated power. The phase to common load need not be balanced between the two phases.

Regulated Output Specification:

Nominal Voltage	39	Volts rms
Split Phase	19.5	Volts rms
Maximum Current	0.84	Amps

Regulation:

0.0 to 0.02 Amps	+10%	-12%
0.02 to 0.84 Amps	+8%	-8%

Table B-18. HP 12159A Electrical Connector (P1) Pin Definitions

PIN	SIGNAL NAME
11-14	25 kHz1
15-18	25 kHz2
19-22	GND
23-26	AC02 (phase 2)
27-30	AC01 (phase 1)

B.5.2 HP 12159A THEORY OF OPERATION

For this theory of operation, refer to the schematic shown in Figure B-14. The input transformer T1 steps the input 24 volt peak-to-peak square wave up to 114 volts peak-to-peak across 3-6. The winding 5-6 regulates the output as described below.

L1, L2, C1, and C2 are the main harmonic filters of the square wave. The regulator coil L3 also contributes to filtering.

Components R1, R2, C3, and C4 attenuate the noise generated by the switching diodes CR1 and CR2.

The regulator limits the amplitude of the output sine wave to less than 59 volts and imposes no minimum value. The output of CR1, CR2, and C5 is the peak of the output sine wave. If this voltage exceeds 26 volts (zener diode CR3 voltage) plus the B-E drops across Q1 and Q2, then a current flows into the base of Q1, causing current flow through CR4 and Q2. This current adds to the main circuit current through L3, causing a voltage drop across L3. This voltage drop is a strong function of excessive output voltage which has the effect of providing regulation.

The regulator clamps the output to be less than or equal to the sum of the zener voltage plus the B-E drops of the transistors.

B.5.3 REPLACEABLE PARTS

Replaceable parts for the 12159A are listed in Table B-19 and the names and addresses of the parts manufacturers are listed in the Manufacturer's Codes List below. The parts locations are shown in Figure B-15.

Manufacturer's Code List

MFR NO.	MANUFACTURER NAME	ADDRESS	ZIP CODE
00000	Any Satisfactory Supplier		
01121	Allen-Bradley Co	Milwaukee, WI	53204
01295	Texas Instr Inc Semicond Cmpnt Div	Dallas, TX	75222
03888	K D I Pyrofilm Corp	Whippany, NJ	07981
04713	Motorola Semiconductor Products	Phoenix, AZ	85008
07263	Fairchild Semiconductor Div	Mt. View, CA	94042
07910	Teledyne Semiconductor	Hawthorne, CA	90250
11236	CTS of Berne Inc	Berne, IN	46711
11961	Semicon Inc	Burlington, MA	01803
14936	General Instr Corp Semicon Prod Gp	Hicksville, NY	11802
19701	Mepco/Electra Corp	Mineral Wells, TX	76067
24546	Corning Glass Works (Bradford)	Bradford, PA	16701
27014	National Semiconductor Corp	Santa Clara, CA	95051
28480	Hewlett-Packard Co. Corporate Hq	Palo Alto, CA	94304
32293	Intersil Inc	Cupertino, CA	95014
34335	Advanced Micro Devices Inc	Sunnyvale, CA	94086
34649	Intel Corp	Mt. View, CA	94043
50088	Mostek Corp	Carrollton, TX	75006
50364	Monolithic Memories Inc	Sunnyvale, CA	94086
56289	Sprague Electric Co	North Adams, MA	01247

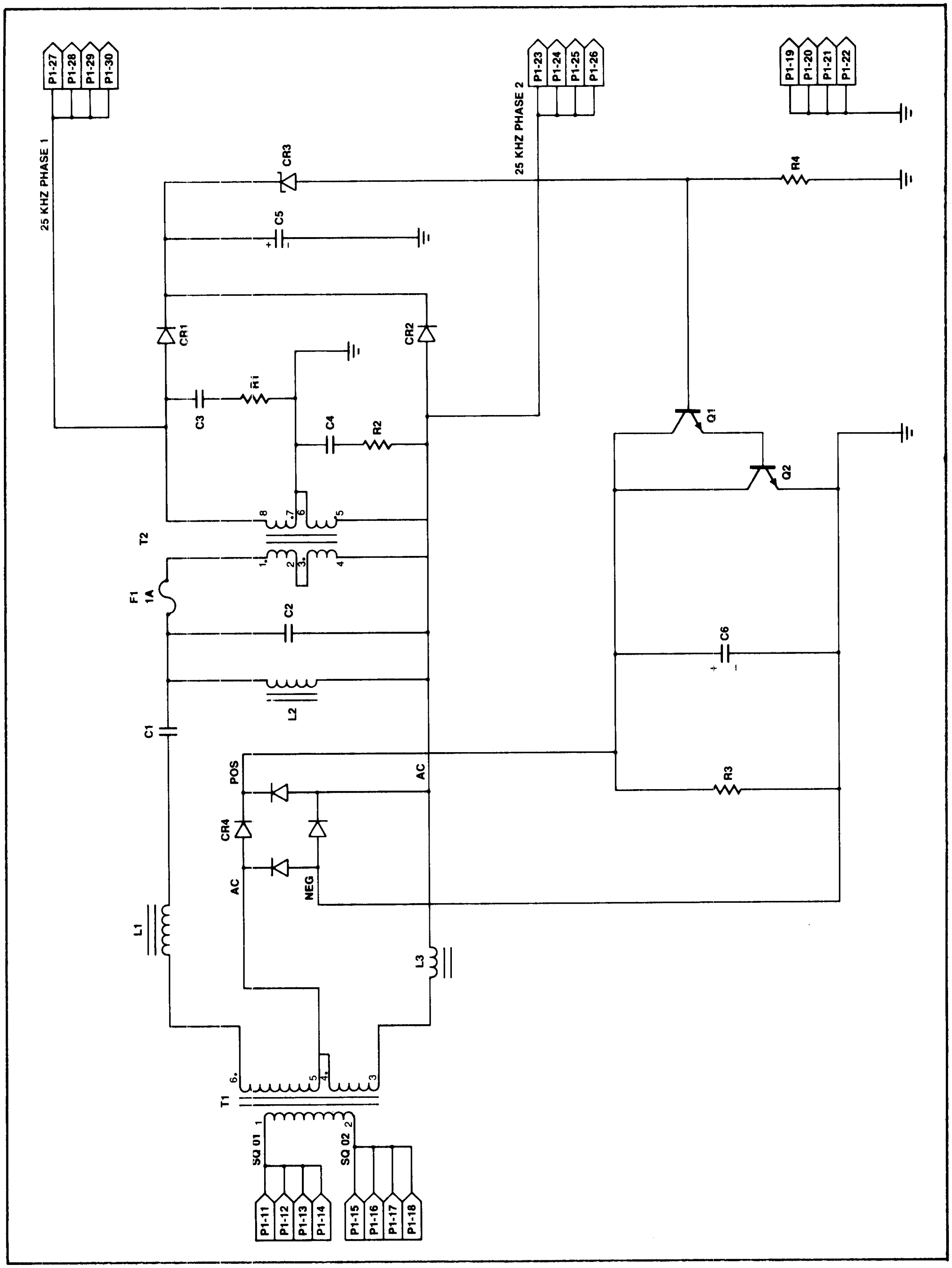

Figure B-14. HP 12159A 25 kHz Power Module Schematic

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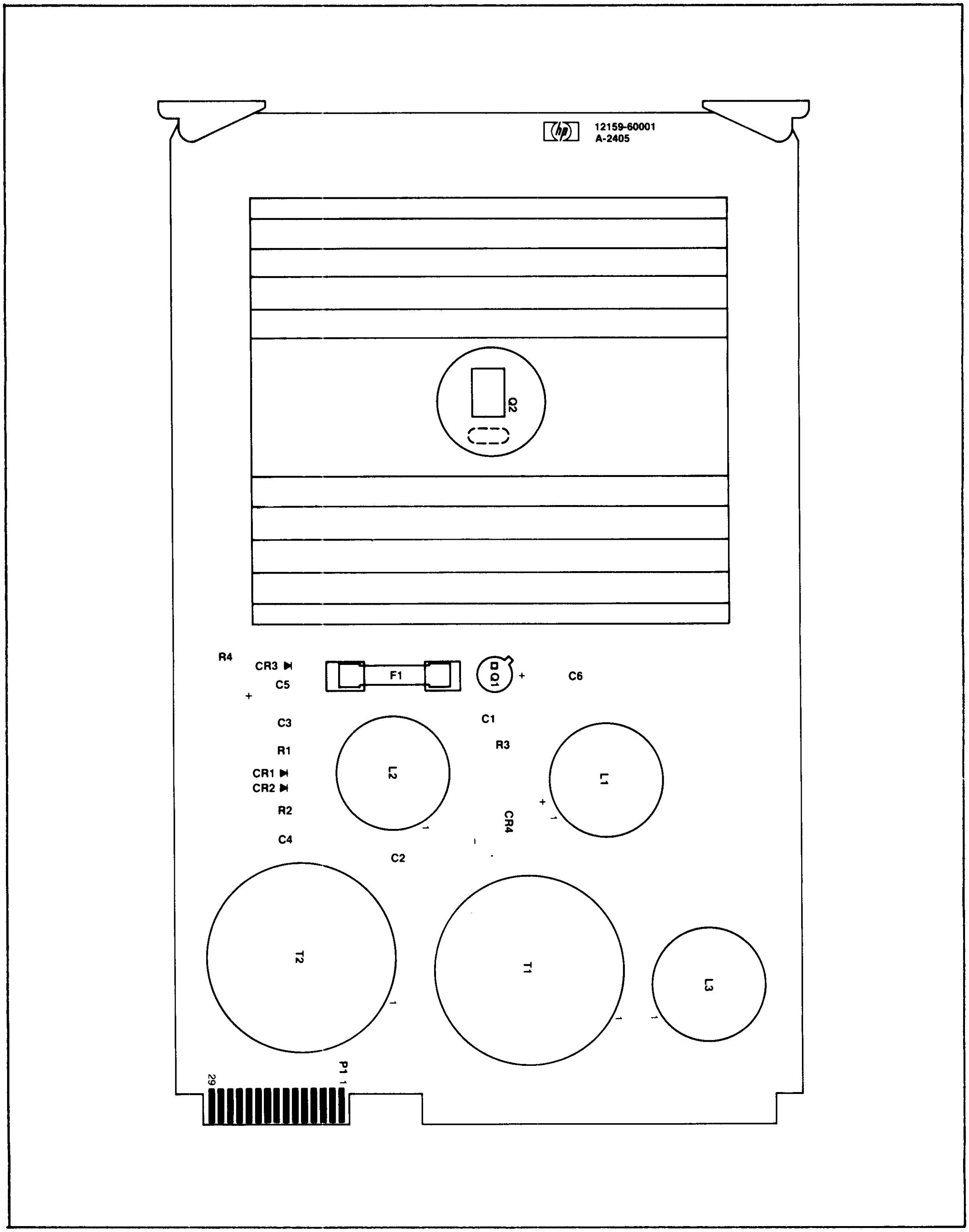


Figure B-15. HP 12159A Replaceable Parts Locations

Update 1

Table B-19. HP 12159A Replaceable Parts

Reference Designation	HP Part Number	C D	Qty	Description	Mfr Code	Mfr Part Number
	12159-60001	8	1	PCA-25KHZ	28480	12159-60001
C1	0160-6040	0	2	CAP 0.1 UF	28480	0160-6040
C2	0160-6040	0		CAP 0.1 UF	28480	0160-6040
C3	0160-0161	4	2	CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C4	0160-0161	4		CAPACITOR-FXD .01UF +-10% 200VDC POLYE	28480	0160-0161
C5	0180-0269	5	1	CAPACITOR-FXD 1UF+50-10% 150VDC AL	56289	30D105G150BA2
C6	0180-0141	2	1	CAPACITOR-FXD 50UF+75-10% 50VDC AL	56289	30D506G050DD2
CR1	1901-0096	7	2	DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0096
CR2	1901-0096	7		DIODE-SWITCHING 120V 50MA 100NS	28480	1901-0096
CR3	1902-3269	4	1	DIODE-ZNR 26.1V 2% DO-35 PD=.4W	28480	1902-3269
CR4	1906-0077	4	1	DIODE-FW BRDG 400V 5A	28480	1906-0077
F1	2110-0001	8	1	FUSE 1A 250V NTD 1.25X.25 UL	75915	312001
L1	9140-0863	0	1	IND-FXD 240UH	28480	9140-0863
L2	9140-0861	8	1	IND-FXD 335 UH	28480	9140-0861
L3	9140-0862	9	1	IND-FXD 75UH	28480	9140-0862
Q1	1854-0079	5	1	TRANSISTOR NPN 2N3439 SI TO-5 PD=1W	3L585	2N3439
Q2	1854-0727	0	1	TRANSISTOR NPN 2N6474 SI TO-220AB PD=40W	3L585	2N6474
R1	0698-3620	5	2	RESISTOR 100 5% 2W MO TC=0+-200	28480	0698-3620
R2	0698-3620	5		RESISTOR 100 5% 2W MO TC=0+-200	28480	0698-3620
R3	0683-2735	0	1	RESISTOR 27K 5% .25W FC TC=-400/+800	01121	CB2735
R4	0683-2215	1	1	RESISTOR 220 5% .25W FC TC=-400/+600	01121	CB2215
T1	9140-0859	4	1	XFMR	28480	9140-0859
T2	9140-0860	7	1	XFMR	28480	9140-0860

B.6 25 kHz BACKPLANE POWER APPLICATIONS

25 kHz backplane power can be used when designing special interfaces on the 12010A Breadboard Interface to provide ac input power for compact, lightweight on-interface dc power supplies to meet any of the following requirements.

1. Provision of dc voltages in addition to those supplied by the power supply.

2. Provision of dc supplies whose analog grounds are isolated from the computer ground.

3. Provision of multichannel isolated power to digital communication circuits to eliminate ground noise paths and maximize the reliability of serial data transfers.

4. Low voltage, high current power for supplying large arrays of integrated circuits.

B.6.1 NON-ISOLATED POWER SUPPLY

B.6.1.1 Purpose and Basic Design

Where additional +7.5V to +12V dc at up to 1 amp is needed for interface circuits, the 25 kHz backplane power can be used to provide a non-isolated positive regulated power supply as shown in Figure B-16. The 19.5V rms potential on either side of common provides at least +15.4V dc after rectification and filtering. An adjustable, off-the-shelf, three-terminal integrated circuit voltage regulator (National Semiconductor Series LM11 7 or equivalent) can be used to set the regulated output voltage within the range of +7.5V to +12V dc. The regulated voltage output is dependent upon the values of resistors R2 and R3. A negative output voltage supply similar to the positive supply shown in Figure B-16 can be made by reversing the polarities of the rectifiers and using a negative adjustable regulator, (National Semiconductor Series LM137 or equivalent).

B.6.1.2 Preserving Purity of Input Sine Wave

To maintain the purity of the input 25 kHz sine wave, near 180 degree conduction should be provided in the rectification process, which necessitates the use of a choke input filter. This filter also limits the surge current at turn-on if the requirements for Lmin are met. The equation for Lmin with a 25% safety factor is given by:

Lmin (in henries) = (K/fs) x R1

where: Fs = 25 kHz
R1 = Minimum load resistance
K = 0.06 for full wave rectifiers

This implies the need for a minimum load. If the circuits to be powered allow the load current to go to zero, a preloading bleeder resistor is required. The final value of Lmin would then be determined by the allowed power loss (dissipation) of the preloading resistor. When the Lmin requirement is met, the surge current will be acceptable and sine wave distortion will be minimized.

B.6.1.3 Rectifier Selection

Rectifiers used with 25 kHz input power must be of the fast recovery type with less than 200 nanosecond recovery time. Allowing for possible transients from leakage instances, overshoot, and MTBF derating, the rectifiers should also have 100V peak inverse voltage rating.

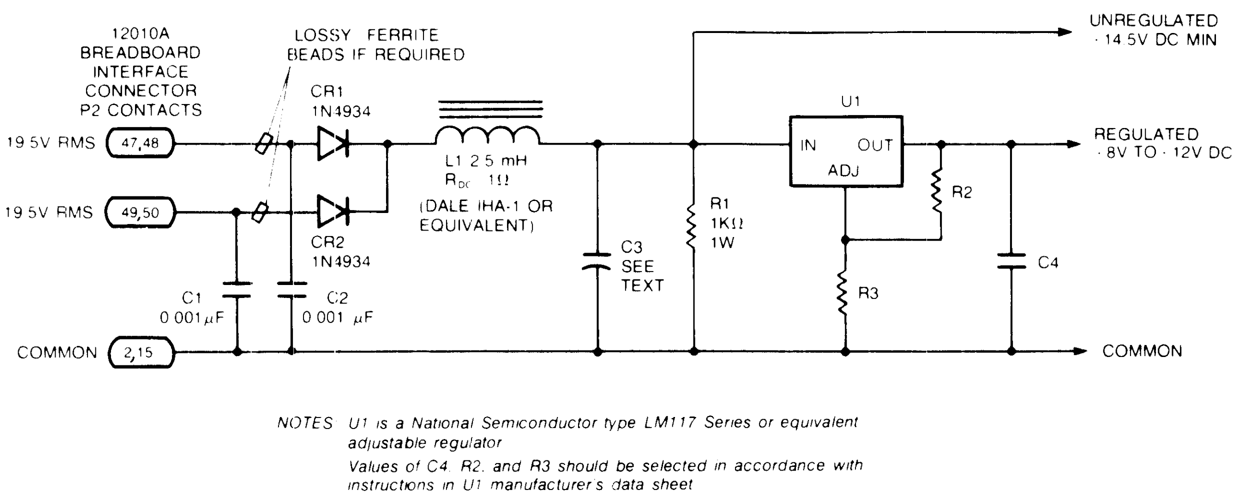


Figure B-16. On-interface Regulated Power Supply

Update 1

B.6.1.4 Input Noise Reduction

During rectifier recovery, the removal of stored charge in the rectifiers will appear as spikes on the rectifier inputs. These spikes should be suppressed to keep them from travelling along the 25 kHz ac input lines in the backplane. Small 0.001 to 0.1 microfarad ceramic capacitors (C1 and C2 in Figure B-16) will usually damp out these spikes, with the required capacitor value dependent upon the magnitude of stored charge being removed. If underdamped ringing is present because of leakage inductance, small ferrite beads, tubes, or toroids can be threaded onto the rectifier leads to provide a "lossy" inductive reactance at high frequencies to effectively dissipate undesirable recovery currents.

B.6.1.5 Input Filtering

The value of C3 is determined by the amount of ripple voltage that can be tolerated at the input of integrated circuit regulator U1. The Vin-Vout differential of 3 volts must be met for any chosen output voltage as noted in Reference 2. The Ripple factor (r) for a full-wave rectifier circuit is given by:

$$r = (0.83/(L1 \times C1) \times 5.76 \times 10^{-6}$$

The case size and construction of capacitor C3 must be capable of conducting the ripple current without excessive dissipation. Ripple current will be at 2 fs and will be sinusoidal when Lmin requirements are met. The rms ripple current in amps is given by:

$$1r = VRMS/(4\pi \times fs \times L1)$$

Where: VRMS is the input voltage phase to common

fs = 25 kHz
L1,> = Lmin

The minimum inductive value of L1 must be present with the dc current flowing through it over the complete load current range. This requires an inductor with gaps in the magnetic circuit, either fixed or distributed, such as in powdered iron cores, or solenoid-wound inductors over ferrite rods (available from Reference 9).

B.6.1.6 Regulator Dissipation.

Since the regulator is a linear series pass type, the difference between the voltage developed across C3 at the regulator input and the desired output at the load current must be dissipated in the regulator. This dissipation is given by:

$$P_{diss} = (V_{in} - V_{out}) \times (I_L + V_{in} I_q)$$

Where: I_q = the quiescent current of the regulator.

Case to junction thermal resistances are given in the regulator manufacturer's data sheet. The dominant thermal resistance will be the case to air stream, which is usually available on heat sink manufacturer's data as a function of air velocity. You can assume a minimum 200 ft/min flow across the board with a maximum air temperature on the exit side of 66 degrees C under worst case conditions. For low power on-card dc supplies, the copper foil on the printed circuit board can be used as a heat sink. However, the suitability of this arrangement should be checked carefully with thermocouples to confirm that the temperature rise of the regulator is not excessive.

B.6.2 ISOLATED OR FLOATING DC POWER

A major advantage of the 25 kHz backplane power is its ease of use for isolated power supplies that can have separate analog grounds, thereby reducing the effects of ground-conducted noise as discussed in References 3 and 4. Isolation is provided by an on-interface transformer, as shown in Figure B-17. The use of 25 kHz ac input makes it possible for the isolation transformer to be very small and inexpensive. Toroidal printed circuit mounting types or "P" core (Reference 7) shielded printed circuit mounting types generally offer the best price-performance combination. However, small E-E types can also be used at lower cost with some sacrifice in electromagnetic and electrostatic shielding. High permeability ferrite materials having low losses at 25 kHz are readily available with matching bobbins and mounting hardware from References 6 through 10.

Primary-to-secondary isolation of both dc and high frequency can be somewhat complex. References 3 and 4 describe single and double shielded transformers. It is possible to achieve high isolation with small ferrite cores and proper inter-winding shield design. Simple copper foil inter-winding shields are relatively inexpensive and are effective in decreasing primary-to-secondary electrostatic coupling at frequencies from 100 Hz to about 100 kHz. For higher frequencies, "link" coupling of two cores or other techniques may be required (Reference 3, p 117).

The ground isolation provided by the multi-channel +10V 30 MA power supply circuits depicted in Figure B-17 eliminates errors caused by ground-induced noise. In analog voltage measurement applications, power supply isolation minimizes common mode noise, improving measurement accuracy. With respect to digital data transmission uses, power supply isolation allows data terminals to operate at greater distances from the local system with fewer data errors than would otherwise be possible. When the power supply is not isolated, noise in the 50/60 Hz mains power distribution and grounding system supplying the computer can cause current noise loops that degrade signal integrity.

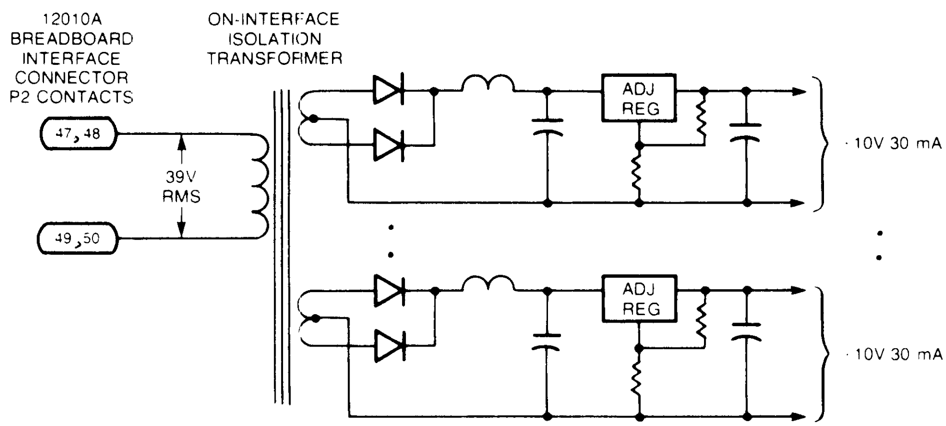


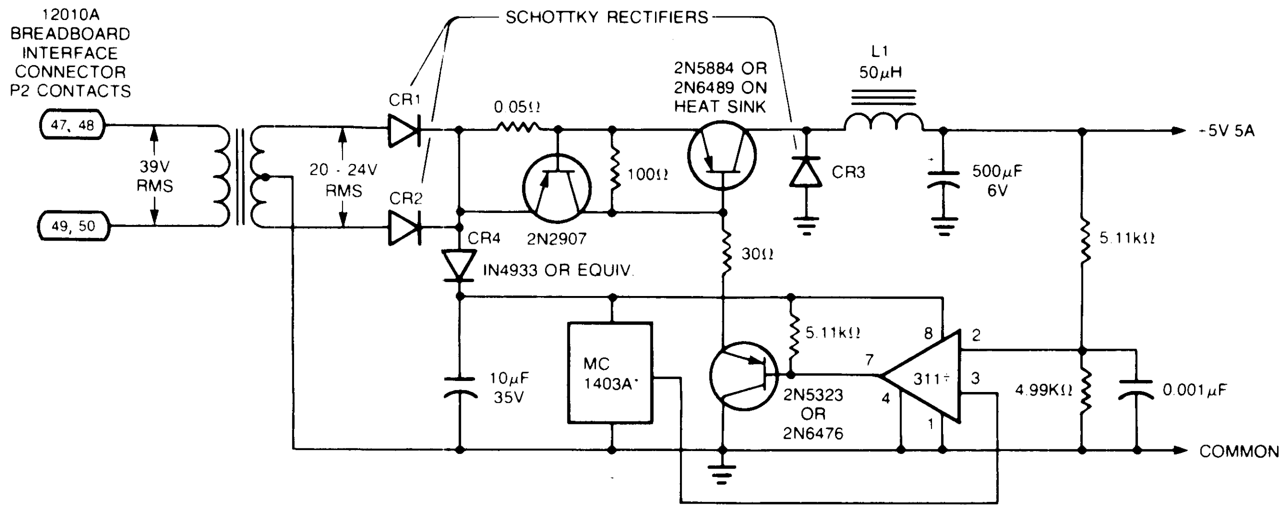
Figure B-17. Multiple, Isolated, On-interface Power Supplies

B.6.3 LOW-VOLTAGE, HIGH-CURRENT POWER SUPPLY

Heat dissipation is often the main factor limiting the current output of on-interface power supplies. This is particularly true for lower voltage, high current supplies, such as required for many digital integrated circuit families. For example, at the +5V used for TTL families of integrated logic circuits, even the dissipation of the rectifiers can be a significant 40% to 20% of total power, because of the inherent 0.7V to 1.0V forward drop across silicon rectifiers, and heat sinking may be required at 3-5 Amp currents. Use of hot carrier or Schottky junction rectifiers, which have a lower forward drop presenting a power loss of only 4%-5% of the total power output, have peak inverse voltage ratings that are suitable for lower voltage power supplies and may not require heat sinks because of their lower power dissipation.

At low output voltages, the 2-3 volt drop required across most three-terminal adjustable integrated circuit series regulators for proper regulation can account for 40%-60% of the total power output, which is lost in the regulator and must be dissipated. Regulator heat sinking becomes difficult for even 1-3 Amp current outputs and impossible for the higher current levels that larger three-terminal regulators are able to pass. Because of these efficiency and dissipation problems, a more efficient circuit approach has evolved, as shown in Figure B-18.

The circuit of Figure B-18 uses a driven switching regulator for more efficient delivery of low voltage, high current output. This circuit regulates on the basis of the conduction angle of the pulsating rectified, unfiltered dc from the on-interface Schottky rectifiers. The result is efficiencies of 70%-85% with 1 Amp to 5 Amp loads. The duty cycle control is uniform over the half sine wave and the instantaneous energy is low at the switching transitions, which minimizes waveform distortion and RFI emission. Because the regulator operates on the incoming frequency as a driven circuit, it also eliminates the generation of other frequencies that would be a problem if an on-interface switching regulator integrated circuit were used. The circuit eliminates sum and difference noise frequencies and a host of non-repetitive noise problems, while optimizing efficiency.



CR1, CR2, and CR3 are International Rectifier 80SQ10 5A Schottky rectifiers.
**Motorola MC1403A or equivalent 2.5V low TC reference source*
÷National Semiconductor LM 311 or equivalent Comparator
L1 is a Dale type IH5 or equivalent solenoid choke coil

Figure B-18. On-interface, High Current Switching Power Supply

References:

1. Reference Data for Radio Engineers, Fifth Edition, Howard W. Sams & Co., Inc., 1974; Chapter 13, pp 28-30.

2. National Semiconductor Linear, Data Book, 1978, Section I, pp 15-22 and 50-54.

3. Morrison, Ralph, "Grounding & Shielding Techniques in Instrumentation", Second Edition, Wiley Publications, Inc., 1977.

4. Ott, Henry, "Noise Reduction Techniques in Electronic Systems", Wiley Publications, Inc., 1976.

5. Fairchild "Voltage Regulator Handbook" or "Hybrid Data Book", available from Fairchild Semiconductor.

6. Ferroxcube "Linear Ferrite Materials and Components".

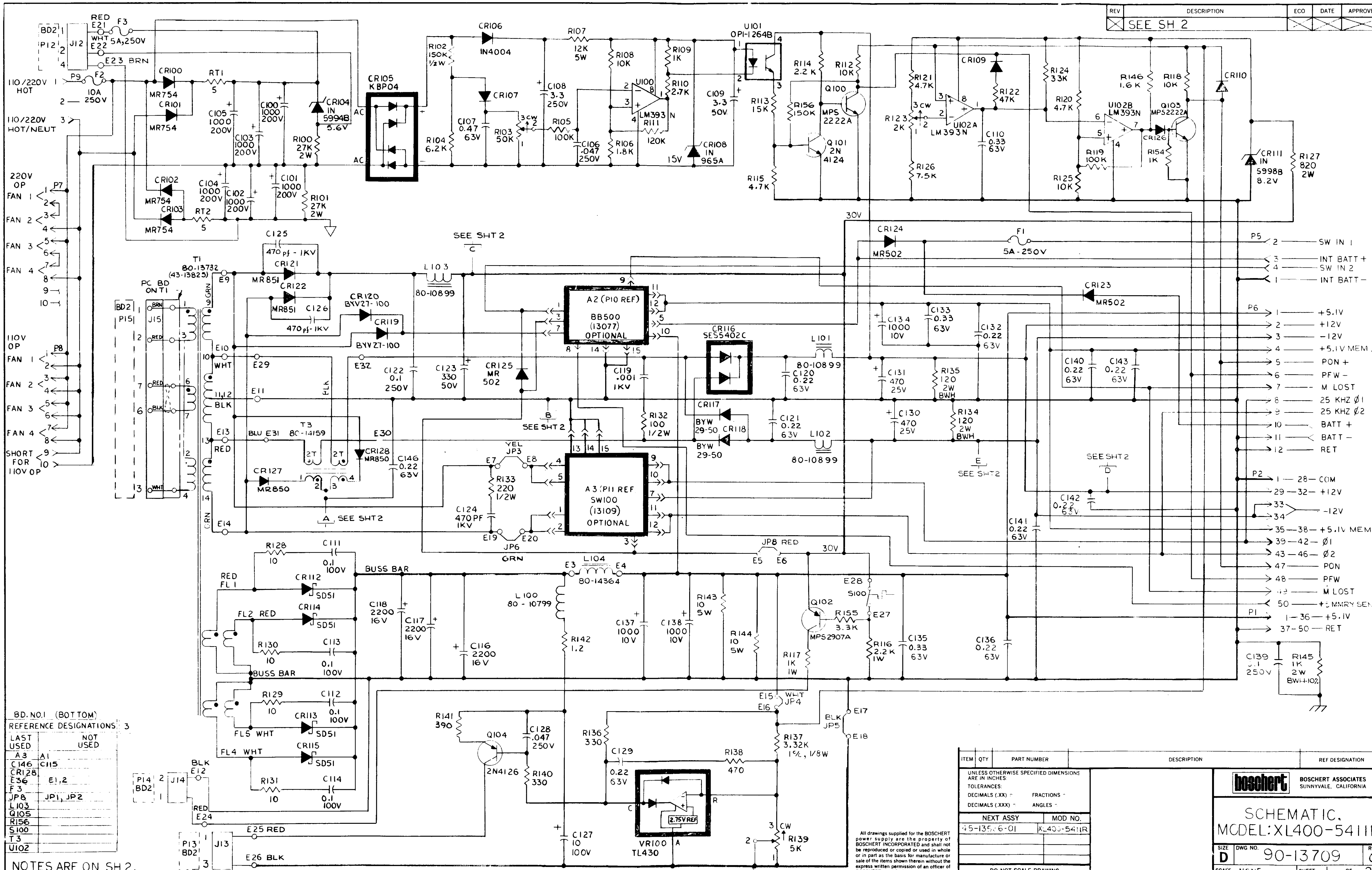
7. TDK Data Book, Ferrite Cores - 2 DLE 88-002A.

8. Siemens Data Book, "Soft Magnetic Siferit", 1975.

9. Fair-Rite Materials Data Book (Rods).

10. Micrometals "Shielded Coil Forms".

11. White, Donald, "EMI Control Methodology and Procedures", Don White Consultants, 1978.



REV | DESCRIPTION | ECO | DATE | APPROVED
SEE SH 2
110/220V HOT
110/220V HOT/NEUT
220V OP
FAN 1
FAN 2
FAN 3
FAN 4
110V OP
SHORT FOR 110V OP
F2 10A 250V
F3 5A,250V
CR100 MR754
CR101 MR754
CR102 MR754
CR103 MR754
RT1 5
RT2 5
C105 1000 200V
C103 1000 200V
C100 1000 200V
C104 1000 200V
C102 1000 200V
C101 1000 200V
CR104 IN 5994B 5.6V
R100 27K 2W
R101 27K 2W
CR105 KBP04
CR106 IN4004
R102 150K 1/2W
CR107
R104 6.2K
C107 0.47 63V
R103 50K
C108 3.3 250V
R105 100K
C106 .047 250V
R107 12K 5W
R108 10K
R106 1.8K
U100 LM393
R111 120K
R109 1K
R110 2.7K
C109 3.3 50V
CR108 IN 965A
15V
U101 OPI-1264B
R113 15K
R114 2.2K
R156 150K
R112 10K
Q100 MPS 2222A
Q101 2N 4124
R115 4.7K
R121 4.7K
R123 2K
CR109
R122 47K
U102A LM393N
C110 0.33 63V
R126 7.5K
R124 33K
R120 4.7K
R119 100K
R125 10K
U102B LM393N
R146 1.6K
R118 10K
Q103 MPS2222A
CR126
R154 1K
CR110
CR111 IN 5998B 8.2V
R127 820 2W
30V
CR124 MR502
F1 5A-250V
CR123 MR502
P5
SW IN 1
INT BATT +
SW IN 2
INT BATT −
P6
+5.1V
+12V
−12V
+5.1V MEM.
PON +
PFW −
M LOST
25 KHZ Ø1
25 KHZ Ø2
BATT +
BATT −
RET
P2
28 — COM
29 — 32 — +12V
33, 34 — −12V
35 — 38 — +5.1V MEM.
39 — 42 — Ø1
43 — 46 — Ø2
47 — PON
48 — PFW
49 — M LOST
50 — +5 MMRY SENSE
P1
1 — 36 — +5.1V
37 — 50 — RET
T1 80-13732 (43-13823)
PC BD ON T1
C125 470 pf - 1KV
CR121 MR851
CR122 MR851
C126 470 pf - 1KV
CR120 BYV27-100
CR119 BYV27-100
L103 80-10899
SEE SHT 2
A2 (P10 REF) BB500 (13077) OPTIONAL
CR116 SES5402C
L101 80-10899
C134 1000 10V
C133 0.33 63V
C132 0.22 63V
C122 0.1 250V
C123 330 50V
CR125 MR 502
C119 .001 1KV
C120 0.22 63V
C131 470 25V
R135 120 2W BWH
C140 0.22 63V
C143 0.22 63V
CR117 BYW 29-50
CR118 BYW 29-50
R132 100 1/2W
C121 0.22 63V
L102 80-10899
C130 470 25V
R134 120 2W BWH
T3 80-14159
CR128 MR850
CR127 MR850
C146 0.22 63V
E30
YEL JP3
R133 220 1/2W
C124 470 PF 1KV
A3 (P11 REF) SW100 (13109) OPTIONAL
JP6 GRN
C142 0.22 63V
C141 0.22 63V
R128 10
C111 0.1 100V
RED FL1
CR112 SD51
BUSS BAR
FL2 RED
CR114 SD51
R130 10
C113 0.1 100V
R129 10
C112 0.1 100V
CR113 SD51
FL5 WHT
CR115 SD51
FL4 WHT
R131 10
C114 0.1 100V
C118 2200 16V
C117 2200 16V
C116 2200 16V
L104 80-14364
L100 80-10799
R142 1.2
C137 1000 10V
C138 1000 10V
R143 10 5W
R144 10 5W
JP8 RED
Q102 MPS2907A
R155 3.3K
S100
R117 1K 1W
R116 2.2K 1W
C135 0.33 63V
C136 0.22 63V
C139 .1 250V
R145 1K 2W BW-10%
WHT JP4
BLK JP5
R141 390
Q104 2N4126
C128 .047 250V
R140 330
R136 330
C129 0.22 63V
R138 470
R137 3.32K 1%, 1/8W
R139 5K
VR100 TL430
2.75V REF
C127 10 100V
E25 RED
E26 BLK
BD. NO.1 (BOTTOM)
REFERENCE DESIGNATIONS
LAST USED | NOT USED
A3 | A1
C146 | C115
CR128 |
E36 | E1, 2
F3 |
JP8 | JP1, JP2
L103 |
Q105 |
R156 |
S100 |
T3 |
U102 |
NOTES ARE ON SH 2.
ITEM | QTY | PART NUMBER | DESCRIPTION | REF DESIGNATION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES:
DECIMALS (.XX) ± FRACTIONS ±
DECIMALS (.XXX) ± ANGLES ±
NEXT ASSY | MOD NO.
45-13526-01 | XL400-5411R
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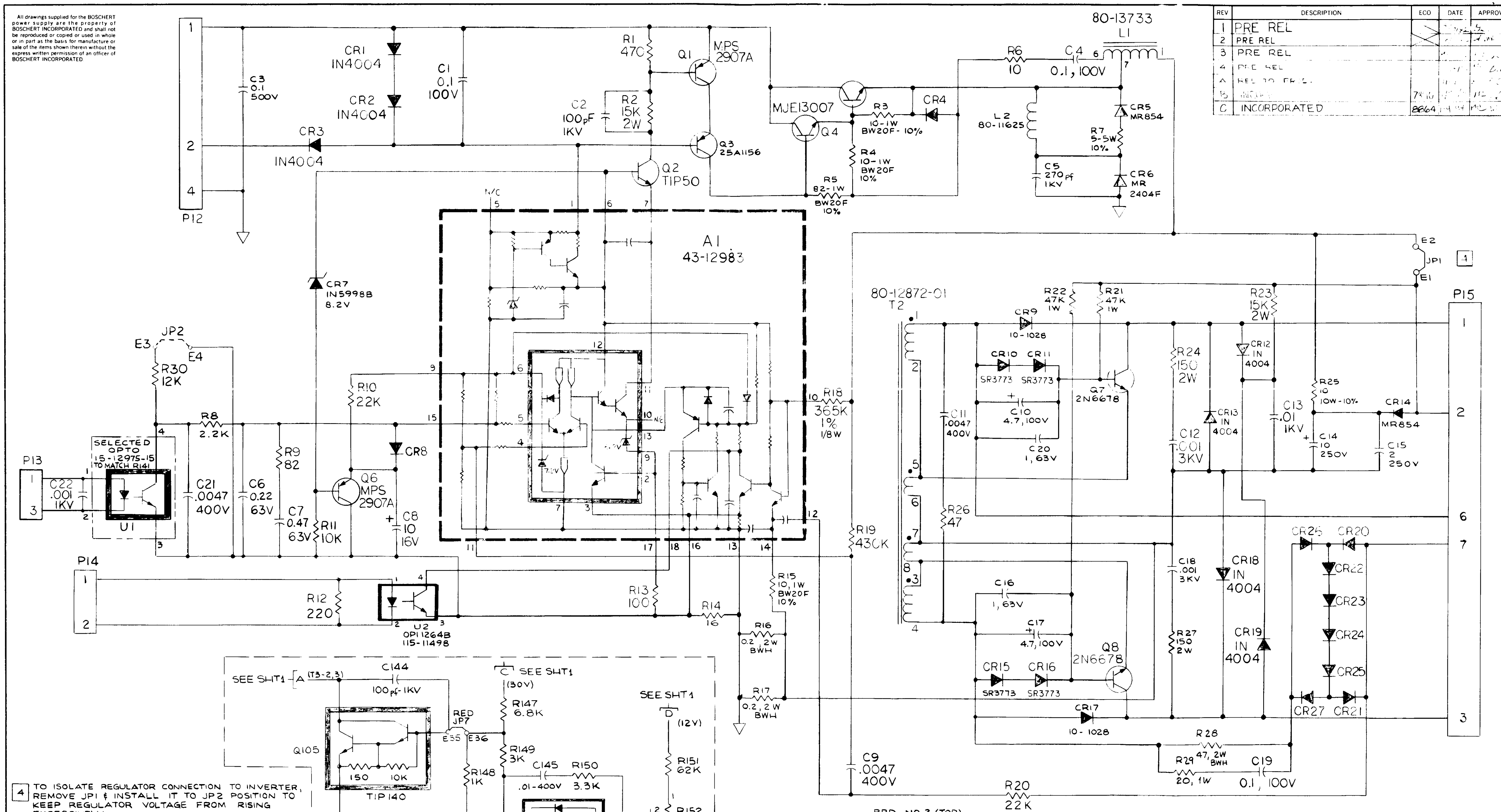
boschert
BOSCHERT ASSOCIATES SUNNYVALE, CALIFORNIA
SCHEMATIC, MODEL: XL400-5411R
SIZE D
DWG NO. 90-13709
REV C
SCALE NONE
SHEET 1 OF 2

REV	DESCRIPTION	ECO	DATE	APPROVED
1	PRE REL			
2	PRE REL			
3	PRE REL			
4	PRE REL			
A	REL TO PROD.			
B	[illegible]	7910		
C	INCORPORATED	8664		



4. TO ISOLATE REGULATOR CONNECTION TO INVERTER, REMOVE JP1 & INSTALL IT TO JP2 POSITION TO KEEP REGULATOR VOLTAGE FROM RISING EXCESSIVELY.

3. DES. NO'S. ON BOARD 1 (BOT) ARE ASSIGNED 100 ON, BOARD 2 (TOP) ARE ASSIGNED NO'S. 1-99, EXCEPT FOR A, E, F, JP, P, S, AND T DES. WILL CON'T.

2. SHEET 1 AND PART OF SHT. 2 OF SCHEMATIC ARE BD1 (BOTTOM) SHEET 2 OF SCHEMATIC IS BD 2 (TOP)

1. UNLESS OTHERWISE SPECIFIED: RESISTORS ARE IN OHMS, ±5%, 1/4W CAPACITORS ARE IN MICROFARADS (UF) DIODES ARE IN4448 VOLTAGE RATINGS ARE DC

NOTES:

BRD. NO. 2 (TOP)

REFERENCE DESIGNATORS	
LAST USED	NOT USED
A1	
C22	
CR27	
E4	
JP2	
L2	
P15	P1 - P11
Q8	
R30	
T2	T1
U2	

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
DECIMALS (.XX) FRACTIONS
DECIMALS (.XXX) ANGLES

NEXT ASSY	MOD NO.
45-13729	XL400-5411R

DO NOT SCALE DRAWING

APPROVALS: DATE
DRAWN
CHECKED
ENG
ENG MGR
MFG MGR
QA MGR
RELEASED

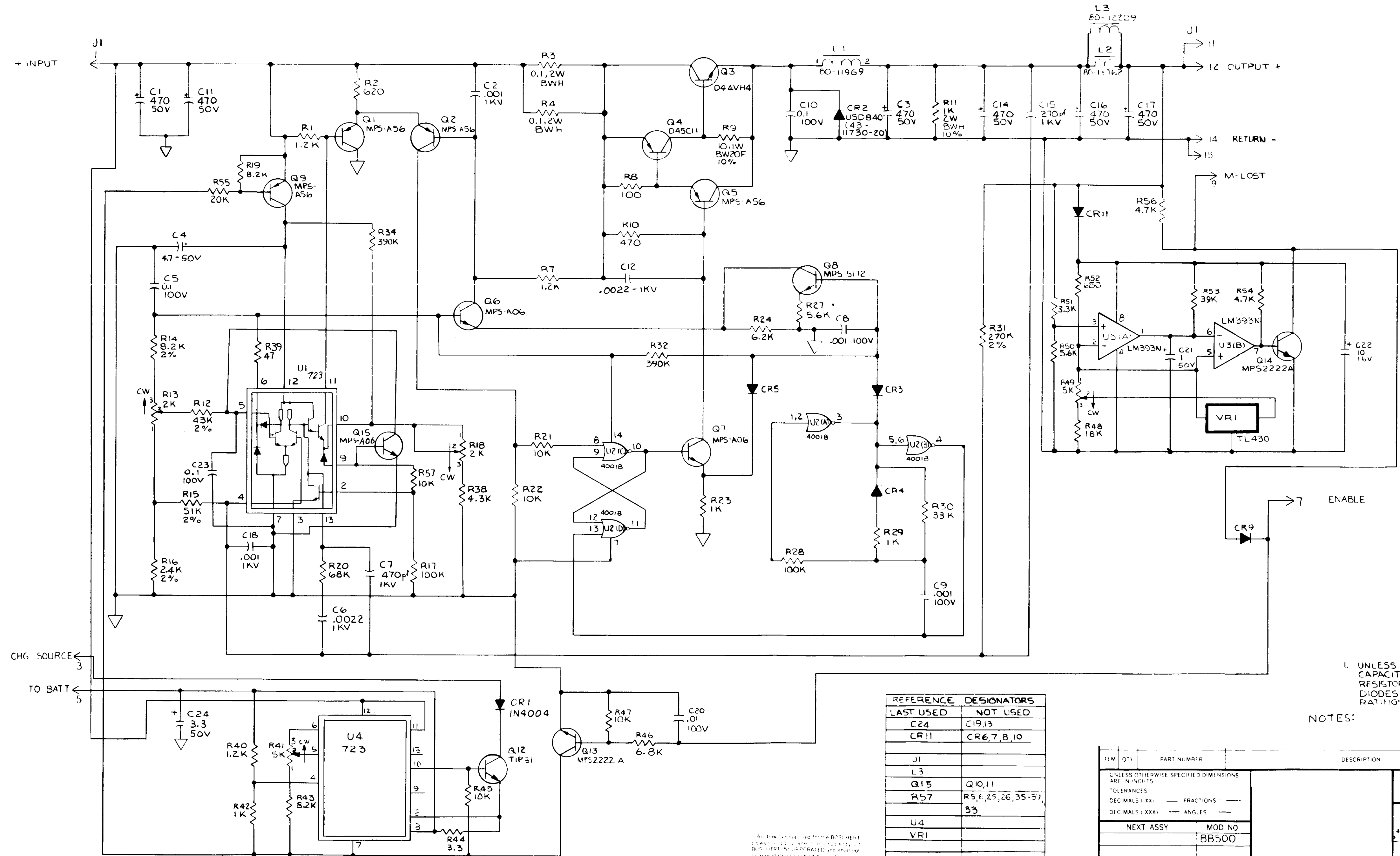
boschert BOSCHERT ASSOCIATES SUNNYVALE, CALIFORNIA

SCHEMATIC
MODEL XL400-5411R

SIZE D DWG NO. 90-13709 REV C
SCALE NONE SHEET 2 OF 2

REV	DESCRIPTION	ECO	DATE	APPROVED
	PRE-REL.		[illegible]	[illegible]
[illegible]	PRE-REL			
3	PRE-REL		2-23-[illegible]	[illegible]
4	PRE REL			
A	[illegible]		[illegible]	[illegible]
B	INCORPORATED	7825	1/14/83	[illegible]
C	INCORPORATED	8342A	[illegible]	[illegible]

DWG NO 90-13076



REFERENCE	DESIGNATORS
LAST USED	NOT USED
C24	C19,13
CR11	CR6,7,8,10
J1	
L3	
Q15	Q10,11
R57	R5,6,25,26,35-37,
	33
U4	
VR1	

NOTES:

1. UNLESS OTHERWISE SPECIFIED: CAPACITORS ARE IN MICROFARADS. RESISTORS ARE IN OHMS, 1/4 WATT, C.F., 5% DIODES ARE 1N4448. RATINGS ARE IN D.C.

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS (.XX) — FRACTIONS —
DECIMALS (.XXX) — ANGLES —

NEXT ASSY	MOD NO.
	BB500

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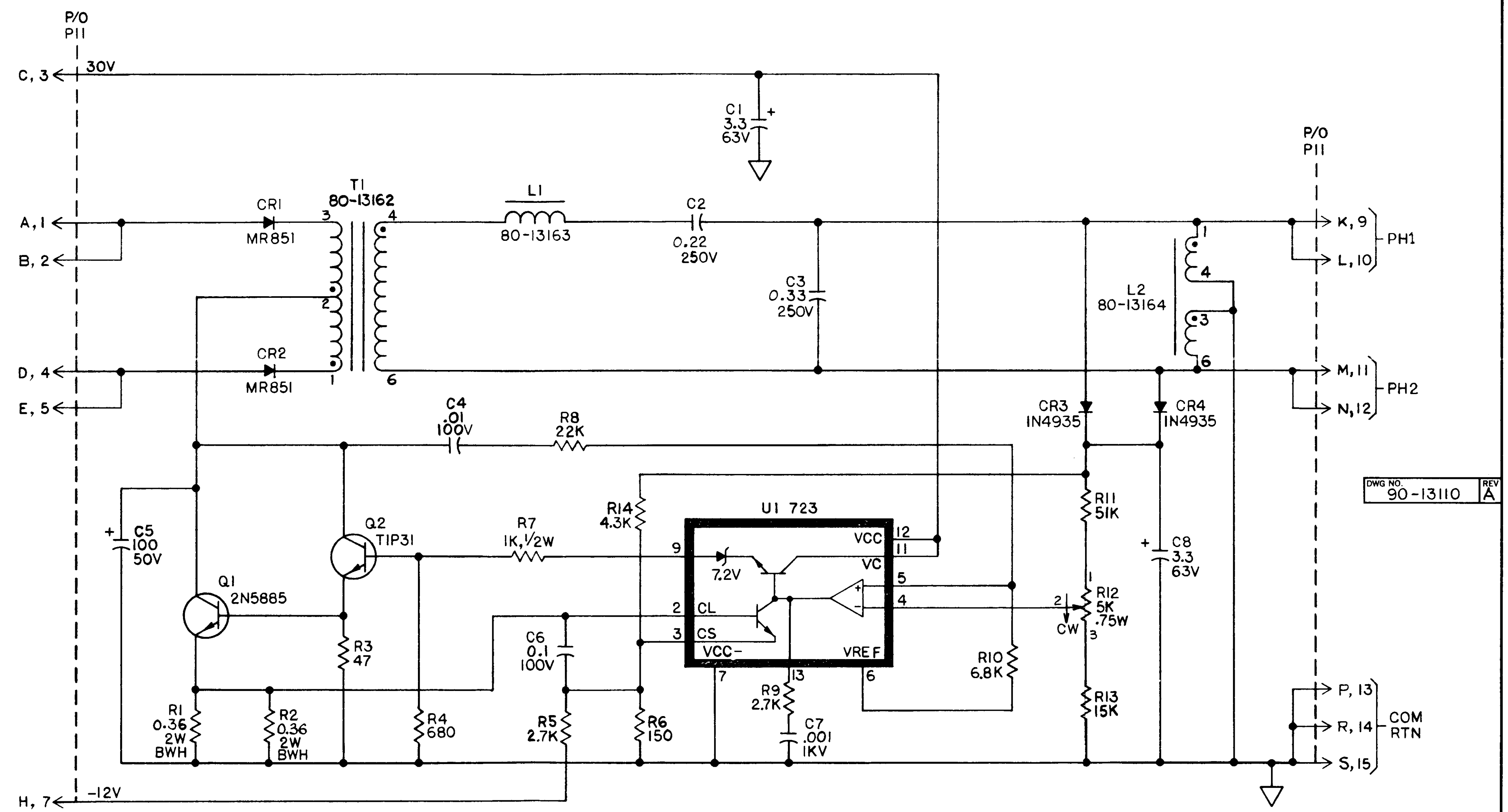
SUNNYVALE CALIFORNIA

SCHEMATIC
+5.1V BATTERY BACK-UP SUPPLY
MODEL: BB500

SIZE D | DWG NO 90-13076 | REV C
SCALE NONE | SHEET 1 OF 1

90-13076-j3

REV	DESCRIPTION	ECO	DATE	APPROVED
4	PRE REL FOR PROD		10/14/82	DR MC
5	PRE REL		12/1/82	MC
A	REL FOR PROD		1/20/83	MC DR



DWG NO.	REV
90-13110	A

NOTES: UNLESS OTHERWISE SPECIFIED,

1. ALL VOLTAGES ARE "DC".
   ALL CAPACITORS ARE IN MICROFARADS
   ALL RESISTORS ARE IN OHMS, ± 5%, 1/4 W.

LAST USED	UNUSED
CR4	
Q2	
U1	
C8	
R14	
T1	
L2	

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES:
TOLERANCES:
DECIMALS (.XX) ± FRACTIONS ±
DECIMALS (.XXX) ± ANGLES ±

NEXT ASSY	MOD NO.
43-13728	XL400-5411

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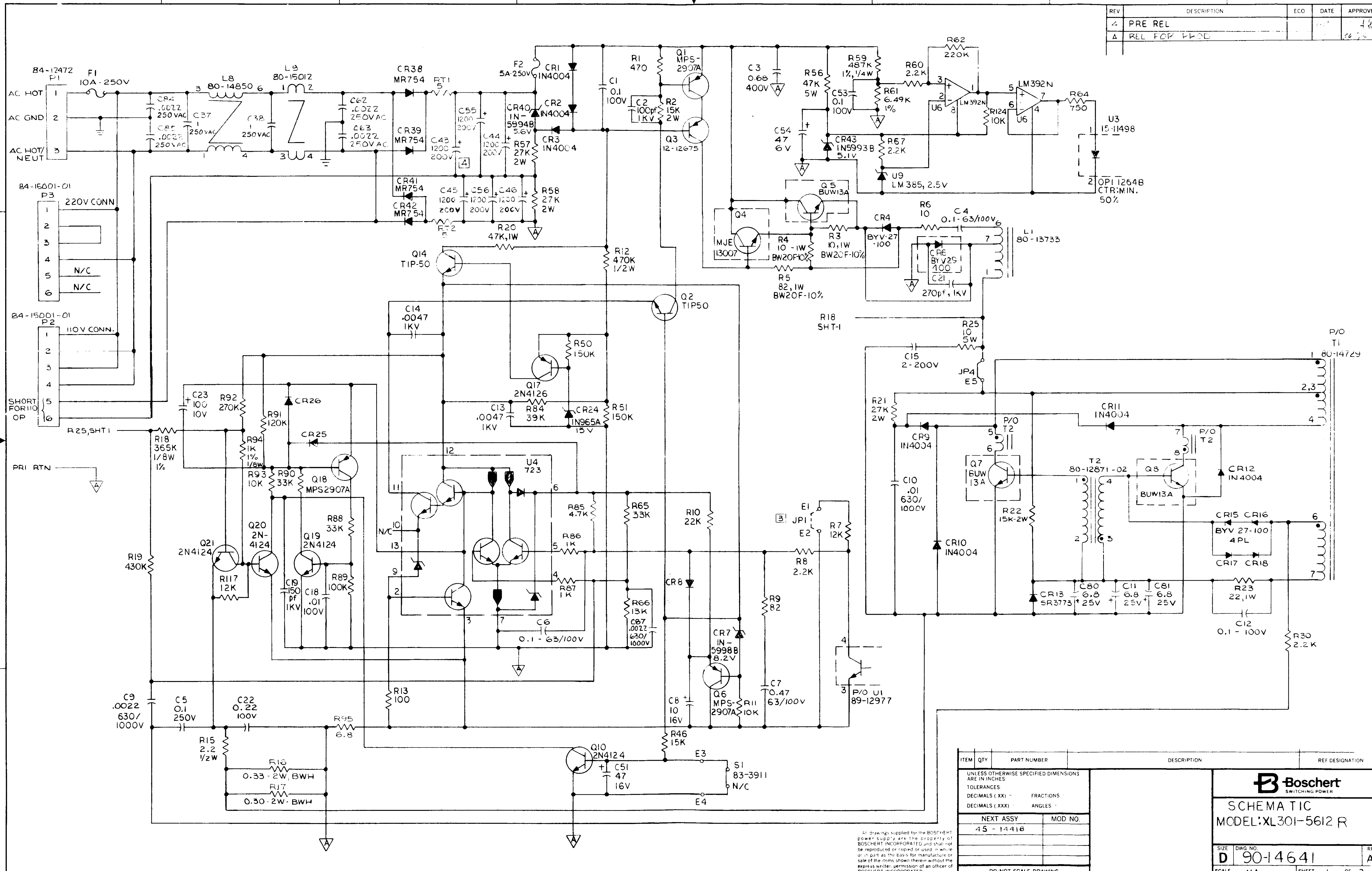
SCHEMATIC
SINE WAVE SUPPLY
SW100

SIZE C | DWG NO. 90-13110 | REV A

SCALE N/A | SHEET 1 OF 1



REV	DESCRIPTION	ECO	DATE	APPROVED
4	PRE REL			
A	REL FOR PROD			

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES
DECIMALS (XX) ± FRACTIONS ±
DECIMALS (XXX) ± ANGLES ±

NEXT ASSY	MOD NO.
45 - 14416	

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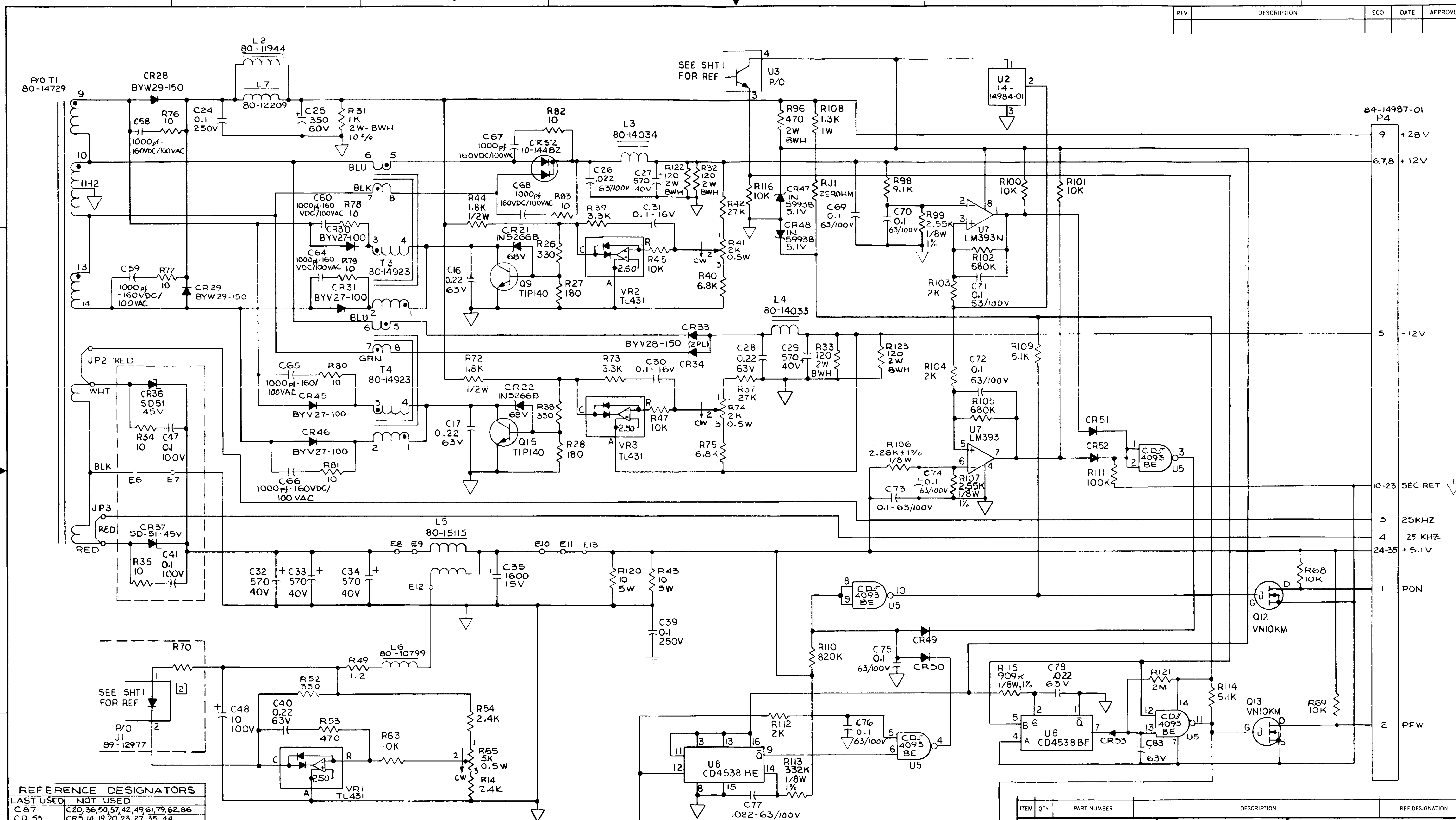
Boschert SWITCHING POWER

SCHEMATIC
MODEL: XL301-5612 R

SIZE D DWG NO. 90-14641 REV A
SCALE NA SHEET 1 OF 2



REFERENCE DESIGNATORS	
LAST USED	NOT USED
C87	C20, 36, 50, 57, 42, 49, 61, 79, 82, 86
CR 53	CR5, 14, 19, 20, 23, 27, 35, 44
E13	
F2	
JP4	
Q21	Q11, Q16
L9	
R124	R 17, 24, 29, 36, 48, 71, 97, 118, 119
RT2	
S1	
U9	
VR3	
RJ1	
P4	
T4	

NOTES: 1. UNLESS OTHERWISE SPECIFIED;
RESISTORS ARE IN OHMS, ±5%, 1/4 W.
CAPACITORS ARE IN MICROFARADS
DIODES ARE 1N4448
VOLTAGES ARE D.C.

2. U1 & R70 ARE A MATCHED SET.

3. FOR UTILIZATION OF JP1 SEE TEST PROCEDURE 91-51461.

4. C55 & C56 NOT USED WHEN 1700 µf MEPCO CAPS, C43-C46 ARE USED.

ITEM	QTY	PART NUMBER	DESCRIPTION	REF DESIGNATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES:
DECIMALS (.XX) ± FRACTIONS ±
DECIMALS (.XXX) ± ANGLES ±

NEXT ASSY	MOD NO.

DO NOT SCALE DRAWING

APPROVALS / DATE
DRAWN
CHECKED
ENG
ENG MGR
MFG MGR
QA MGR
RELEASED

Boschert SWITCHING POWER

SCHEMATIC
XL 301-5612 R

SIZE D | DWG NO. 90-14641 | REV A
SCALE N/A | SHEET 2 OF 2

A

B

C

D

E

I

L

M

READER COMMENT SHEET

HP 1000 A700 COMPUTER
Engineering & Reference Documentation

02137-90005 **June 1984**

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