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SMALL COMPUTER PRODUCT ENGINEERING	TITLE: ENGINEERING PRODUCT SPECIFICATION			
PREP. BY DATE: R.Richard 7.15.77.	LEVEL 6 GCR MAGNETIC TAPE SUBSYSTEM (GCR-MTS)			
APPR. BY DATE: 6.25.82./3.14.85.				

REVISION	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
F	BLCDC7564	06.24.82.	K.A.Kowal	1 through 111F
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G	BLCDF7174	02.22.85.	K.A.Kowal	0-1 through 9-4

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1. INTRODUCTION

1.1 Document Definition

1.1.1 Identification and Purpose

This document is an Engineering Product Specification - Part 1 (EPS-1) for the Level 6 GCR Magnetic Tape Subsystem. It describes the functionality, performance, and configurations of a device-specific adapter which, when attached to a Medium Performance Device Controller, provides the capability of interfacing with a GCR/PE Formatter/Controller.

1.1.2 Related Documents

60144409	PFS, L6 GCR Tape Subsystem
60131966	PFS, Level 6 Medium Performance Tape Subsystems
60126448	EPS-1, New Minicomputer Line System
60126298	EPS-1, Level 6 Bus (Megabus)
03850045	Purchase Specification, GCR/PE/NRZI Tape Drives (STC)
03850047	Purchase Specification, STC Formatter/Controller Unit
60129896	EPS-1, NML Maintainability
49791100	EPS, Streaming Tape Unit (STU), Buffered Keystone Model 92185-04 (STC Interface, CDC Document)
49793200	EPS, Streaming Tape Unit (STU), Model 92185-01 (CDC Document)
03850133	Purchase Specification, 1/2 Inch Start/Stop-Streamer Tape Transport (Buffered Keystone)

1.1.3 Reference documents.

Q4.1,	PWA/PWB Testability Design Rules
MG1,	Component Availability
MTG2,	PWA Test Documentation Requirements
MTG4,	PWA Test Monitor/Test Box Design
MTG5,	PWA Quality Logic Test Creation
MTG6,	PWA Test and Verification Program Creation
MTG7,	PWA IC Socket Utilization
MTG8,	Design for Producibility, Installability, Maintainability and Replaceability
MPDG1,	PWA/PWB Producibility Guidelines
58035052,	Worldwide Maintainance Requirements

1.2 Standards.

1.2.1 National Standards.

ANSI Standard (X3.40-1973)	Unrecorded Magnetic Tape for Informa- tion Interchange.
ANSI Standard (X3.22-1973)	Recorded Magnetic Tape for Information Interchange (800 CPI, NRZI).
ANSI Standard (X3.27-1974)	Magnetic Tape Labels and File Structure for Information Interchange.
ANSI Standard (X3.39-1973)	Recorded Magnetic Tape for Information Interchange (1600 CPI, PE).
ANSI Standard (X3.54-1976)	American National Standard for Recorded Magnetic Tape for Information Inter- change (6250 CPI, Group Coded Record- ing).

1.2.2 General Design, Honeywell Standards:

B01.08,	Environment, Operating
B01.09,	Equipment Safety
B01.10,	Environment, Transportation, Storage & Installation
B03.07,	Reliability - Standard Failure Rate Data Base
B03.08,	Reliability Failure Rate & MTBF Predictions
B04.06,	System Grounding

1.2.3 Product Maintainability, Honeywell Standards:

B07.11,	Logic Nomenclature
B07.12,	Location Reference Designation
B07.13,	Identification Nomenclature for IC's, Printed Cards and Card Cages

B07.38, Logic Symbology
B07.39, Logic Block Diagrams

G02.01, FE Tools and Test Equipment Catalog
G02.05, FE Product Tools & Test Equipment

G07.01, Field Product Maintenance Documentation
G07.02, Product Manual Content Guide
G07.03, Product Style Guide for Manuals
G07.08, Major and Intermediate Block Diagrams
G07.09, Repair Documentation, Draft

1.2.4 Manufacturing Testability Guidelines

D.002.01, PWA/PWB Testability Design Rules
MTG1, PWA Test Equipment Connection Requirements
MTG3, PWA Microdiagnostic Creation
60129949, Application Rules for Minicomputer & Terminal Products

1.3 Scope

The GCR Magnetic Tape Subsystem requirements for Level 6 include a capability to read and write 6250 bpi Group Coded Recording (GCR) and 1600 bpi Phase Encoded (PE) formatted 9 track tape on 25 ips/75 ips CDC, and 125 ips STC tape devices.

The Group Coded Recording Adapter (GCRA), a component of the DPS6 GCR Magnetic Tape Subsystem, is specified herein. This adapter, when attached to the Medium Performance Device Controller (MPDC) satisfies the GCR requirements by providing an interface to an OVP Formatter/Controller (F/C). The combination of GCRA and MPTC (MPDC with an appropriate firmware) becomes the GCR Magnetic Tape Subsystem (GCR-MTS).

1.4 Definitions

Block — A group of contiguous recorded characters considered and transported as a unit containing one or more logical records. Blocks are separated by interblock gaps.

BOB — Beginning Of Block on tape

BOT — Beginning Of Tape

bpi — bits per inch

CAI — Controller Adapter Interfaces

CDC — Control Data Corporation

CLI-F/C — Interface between GCRA and F/C

CPI	Characters Per Inch
CRC	Cyclic Redundancy Check
DAI	Device Adapter Interface
Density	The recording density is a longitudinal measure of the nominal number of information characters which can be recorded in 9 tracks on one inch of magnetic tape. The density is stated in characters per inch (CPI).
DLI-MTU	Device Level Interface MTU
EOB	End Of Block on tape
EOT	End Of Tape
FCI	Flux Changes per Inch
F/C	STC Formatter/Controller
File	A collection of information consisting of one or more related blocks, the boundaries of which are identified on tape by means of tape marks
GCRA	Group Coded Recording Adapter
GCR	Group Coded Recording method
GCR-MTS	Group Coded Recording - Magnetic Tape Subsystem
Hub End	The physical end of tape nearest the EOT marker
Interblock Gap	A dc-erased section of tape separating blocks of information
ips	Inches per second
Level 6	Level 6 Minicomputer Systems
LOS	Level Of Simultaneity
MPDC	Medium Performance Device Controller
MPTC	Medium Performance Tape Controller (MPDC plus GCR firmware)
MBZ	Must Be Zero
MTU	Magnetic Tape Unit
NML	New Minicomputer Line

OEM	Original Equipment Manufacturer
Off Line	A state in which the referenced unit may remain powered up and physically attached, but is logically inaccessible and, in general, is incapable of responding to any commands. This state is usually entered for purposes of field service intervention.
ORU	Optimum Replaceable Unit
OVP	Outside Vendor Product
OVP Tape Drives	Magnetic tape devices as specified in HIS Purchase Specifications 03850133 and 03850045
PE	Phase-Encoded recording method
QLT	Quick Logic Test
RAW	Read After Write
RFU	Reserved for Future Use
Rim End	The physical beginning of tape nearest the BOT marker
ROS	Read Only Store
RWS	Read/Write Storage
STC	Storage Technology Corporation
Tape Character	A column of bits across the width of the magnetic tape. Each bit is loaded in a different tape track.
Tape Mark	A special control block recorded on magnetic tape to serve as a separator between files and file labels.
Tape Track	Longitudinal rows along the length of the magnetic tape where bits of information are placed. The track number indicates the physical position on the tape.
TBD	To Be Determined
VRC	Vertical Redundancy Check

2. ARCHITECTURE

2.1 Overview

The GCR Magnetic Tape Subsystem (GCR-MTS) provides Level 6 with the facility to store and retrieve GCR/PE formatted data from 1/2-inch magnetic tape.

A GCR-MTS configuration consists of an MPTC, connected to the Megabus, with one Group Coded Recording Adapter (GCRA) controlling the Formatter/Controller (F/C) and up to four tape devices. This configuration can process simultaneously a single data transfer and one or more rewind and/or rewind and unload instructions.

Figures 2-1 and 2-2 illustrate structures of both STC and CDC subsystems and their relationship to the system as a whole. Detailed configurational information can be found in Section 9.

2.2 Major Components

Major components of the DPS6 GCR-MTS are a Medium Performance Tape Controller (MPTC), the Group Coded Recording Adapter (GCRA) and either the STC OVP Formatter/Controller (F/C) and radially connected GCR/PE tape transports or CDC daisy chain connected OVP GCR/PE tape transports.

2.2.1 Medium Performance Device Controller (MPDC)

The MPDC is a microprogrammed peripheral control unit which attaches to the DPS6 Megabus (see Megabus EPS) and which, via an adapter, is capable of supporting up to four devices. The microprocessor portion of the MPDC is generalized to facilitate its application as a control element for other controller/device types. Hardware unique to a given device/controller is localized in the device/controller adapter. The MPDC performs general purpose control functions such as:

- Execution of Level 6 bus sequences
- Command decoding
- Data transfer multiplexing between adapters

- o Status and control register storage
- o Direction of the general flow of command execution.

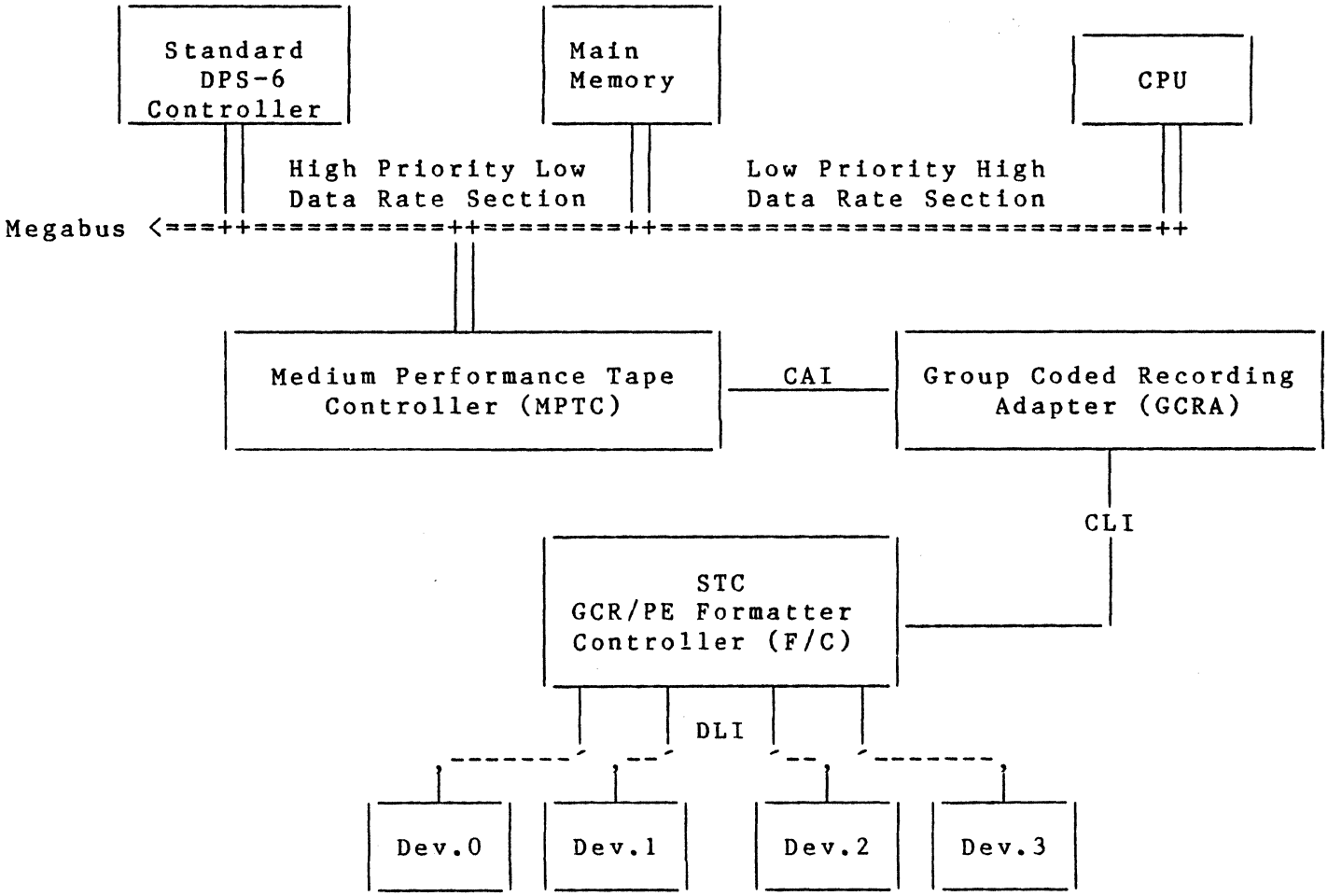


Figure 2-1 STC/DPS6 GCR Magnetic Tape Subsystem

When firmware appropriate to the Group Coded Recording Adapter is plugged in, the board becomes a unique Medium Performance Tape Controller (MPTC).

2.2.2 1/2-Inch Group Coded Recording Adapter (GCRA)

The GCRA is implemented on a triple-size D-board which plugs onto the MPTC via two 25-pin connectors and is connected via cables to the GCR-F/C tape controller. It contains the following functionality:

- o Command decoding
- o Data transfer multiplexing between controller/devices
- o Status and control register storage
- o Provides device write/read data buffers
- o Provides device identification codes
- o Provides controller/adapter interfaces (CAI)
- o Provides adapter/tape controller interfaces (DLI)

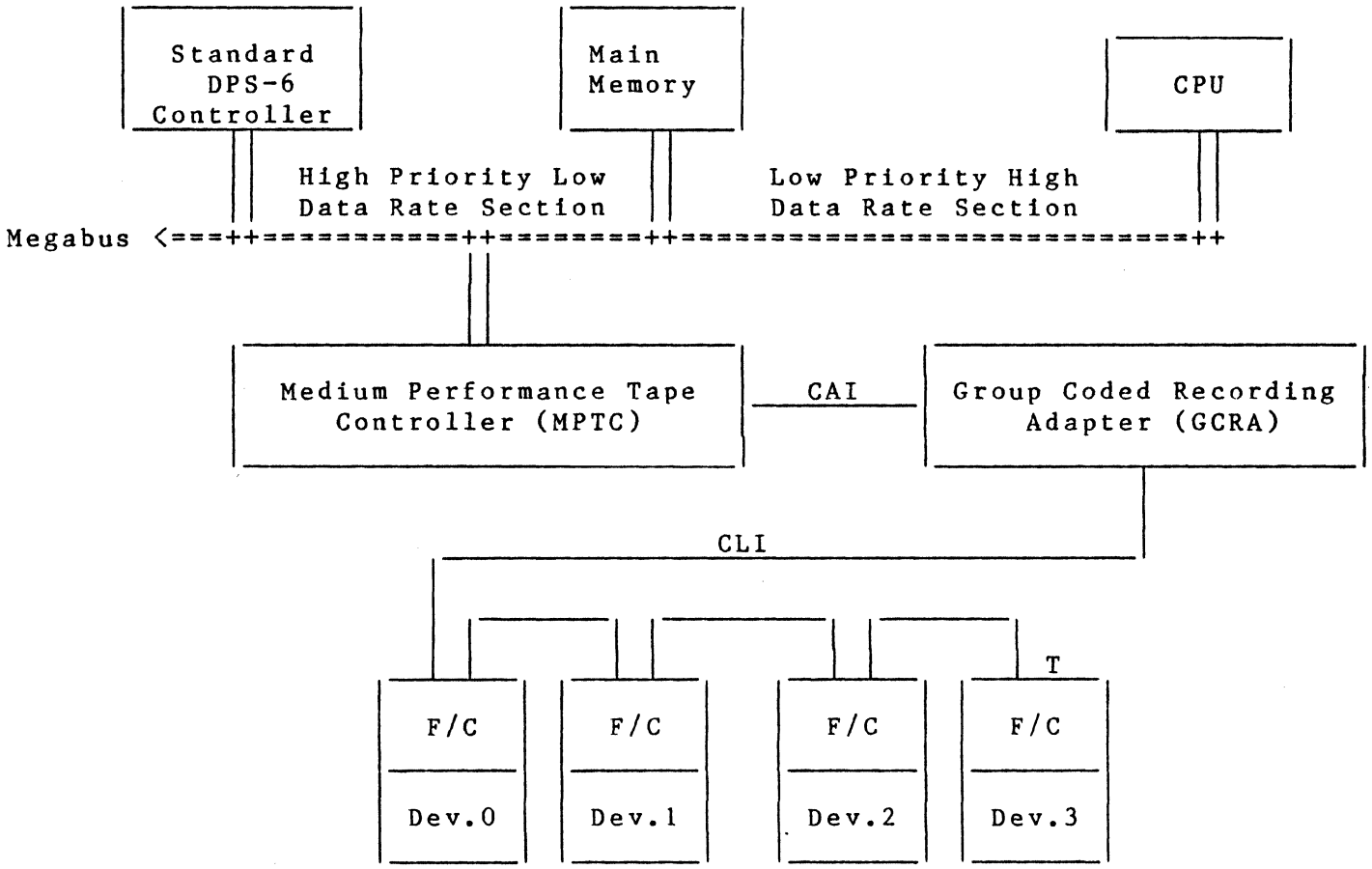


Figure 2-2 CDC/DPS6 GCR Magnetic Tape Subsystem

2.2.3 GCR/PE Formatter/Controller (F/C)

The STC F/C is an OVP Tape Controller capable of generating and reading ANSI format compatible 9-track tapes at 1600 bpi PE or 6250 bpi GCR. It interfaces with up to four STC 1900 series (1960) tape transports in a radial bus configuration (Reference Figure 2-1). The data format capability of each transport is either 1600 bpi, PE or 6250 bpi, GCR.

The CDC F/C is integral to all tape transports and the CLI daisy chain cable connects up to four tape transports together with a terminator in the last connector position in the chain (Reference Figure 2-2).

The F/C attaches to the GCRA adapter via the controller interface (CLI) and contains the following functionality:

- Performs device interface dialog control
- Provides device write/read data buffers
- Performs data integrity checking
- Provides controller/adapter interfaces (CLI-F/C)
- Performs error detection/correction for GCR/PE formats
- Provides the device interfaces (DLI).

2.2.4 1/2-Inch Magnetic Tape Unit (MTU)

The 1/2-inch magnetic tape transports are OVP tape drives which meet the governing purchase specification (refer to subsection 1.3.1). The drives read and write tapes to the following summary of functionality:

- Provides for 125 ips tape speed on STC F/C
- Provides for 25 ips and 75 ips tape speed on CDC tape drives
- Provides for Read After Write (RAW)
- Provides for up to a 10-1/2-inch tape reel
- Provides for 6250 CPI GCR density (9 channel)
- Provides for 1600 CPI PE density (9 channel)
- Provides 128 KByte cache data buffer on CDC drives

3. FUNCTIONAL REQUIREMENTS

3.1 Basic Functions

3.1.1 Configuration and Simultaneity

Devices attached to the MPTC are software addressable via channel numbers. Each individual device (drive) has two channel numbers assigned, differing only in the low-order bit position (the direction bit). When an IOLD instruction is issued to a magnetic tape device, the direction bit of the channel number specifies whether this is an input or an output data transfer. For all other commands, the direction bit is ignored by the hardware. Figure 3-1 outlines the composition of the channel number. Bits 8 through 14 are assigned at system installation and must conform to constraints defined in the Megabus EPS-1. Software visibility of the devices attached to the MPTC is such that the devices are, in general, independent of each other. For example, operations on one tape are independent of any activity on another tape except that the MPTC initiation of a command sequence addressed to one device (channel number) may be stalled (a command sequence has been accepted but not initiated) while the MPTC is busy servicing another device. Further definition of how command sequences are handled by the subsystem can be found in the MPDC EPS-1.

The MPTC provides a single level of simultaneity (only one data transfer can be active in the subsystem) and supports the following:

- A nonbusy device must accept any command directed to it over the bus (i.e., IOLD, Configuration Words A, Range, Task Word, etc.) even though a data transfer may be active over another device. A command may be "waited" (see Megabus EPS-1) for a period not to exceed 12 microseconds (assuming no higher priority bus activity).

- Following completion of a data transfer operation, any rewind orders received are initiated prior to initiation of any data transfer operations.

- Channels are serviced on a rotating priority basis so that no one channel or channels can dominate adapter usage.

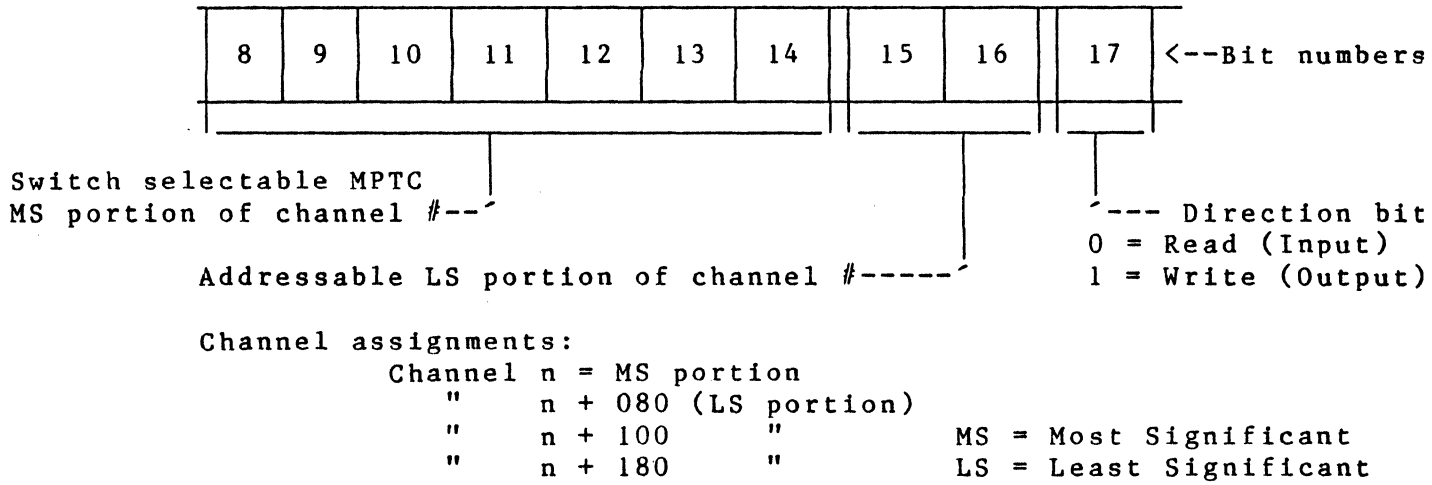


Figure 3-1 Channel Numbers

Note that the controller accepts a data transfer command to drive B while A is doing a data transfer but does not start the data transfer on B until A's data transfer has completed.

If a GCRA is configured with less than four devices, it only responds to channel numbers associated with the installed devices .

3.1.2 Megabus Control

3.1.2.1 Command Transfers

The MPTC recognizes a command transfer request on the Megabus when a valid channel number is decoded in bits 8 through 17 of the address bus (see Megabus EPS-1). If the referenced device is not busy, the contents of the data and address buses are stored in the MPTC interface hardware. If the MPTC is currently executing a data transfer operation on another channel, the command transfer request may be responded to by a WAIT signal for a period not exceeding 12 microseconds (assuming no higher priority bus activity). MPTC firmware is then invoked to process the information. For the not busy case, the MPTC completes the bus cycle by issuing an ACK to the CPU. If, however, the referenced device is busy executing a previously received command, the MPTC interface hardware completes the bus cycle by issuing a NAK (except for the Output Control Word command, see subsection 5.2.6). If the MPTC interface hardware is temporarily busy, because firmware has not had an opportunity to service a previously initiated bus cycle or because the MPTC is busy generating a read response cycle, then the MPTC

interface logic completes any new bus cycle with the WAIT response (see Megabus EPS-1). See subsection 5.2 for a description of the various commands applicable to the MPTC Tape Subsystem.

The address and data bus configurations for the various commands are detailed in subsection 5.2.

3.1.2.2 Data Transfer

All data transfers associated with the MPTC/GCRA subsystem are executed in Direct Memory Access (DMA) mode. Data transfers are normally in word mode but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer begins or ends on an odd byte boundary.

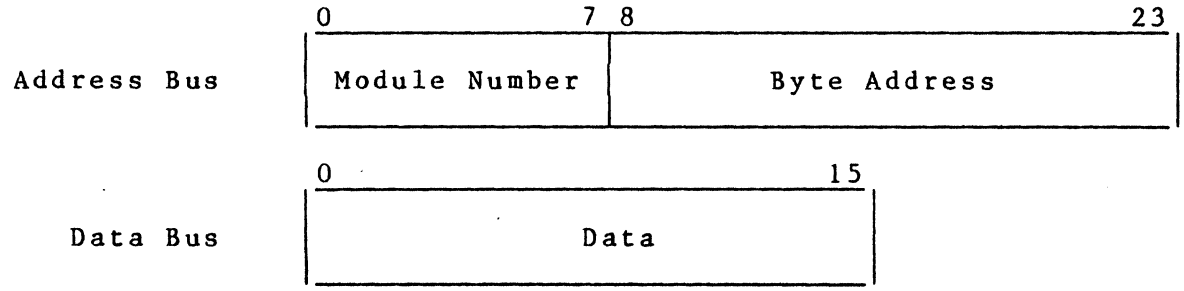
If a NAK response is received at the MPTC during a memory write or read request cycle on the Megabus, the data transfer continues to its normal termination with a nonexistent resource error posted in the status word (see subsection 5.2.14.14). If a WAIT response is received for a memory write or read request, the MPTC interface hardware retries the bus cycle. Retries continue until either a NAK or ACK response is received. Note that while a bus cycle is pending in the MPTC interface hardware, no bus cycles from the CPU to the MPTC are accepted (including the Output Control Word). This also applies to the interval between a memory read request and the read response (second-half read) cycle. Once the interface hardware is conditioned to do a memory transfer (either read or write,), other bus cycles addressed to the MPTC are completed with either NAK or WAIT (depending on channel busy status) until the memory reference is complete. Read response (second-half read) cycles from memory to MPTC are always completed with ACK (NAK and WAIT are never used for these cycles).

Figure 3-2 illustrates the address and data bus configurations for read and write data transfers. During the instruction cycle of memory read sequences, bits 10 through 15 of the data bus may contain the address of a register in the MPTC into which the returned data (from memory) is delivered. In the response (second-half read) cycle, the memory places on the address bus (bits 8 through 23) the contents of the entire data bus (bits 0 through 15) as received during the instruction cycle.

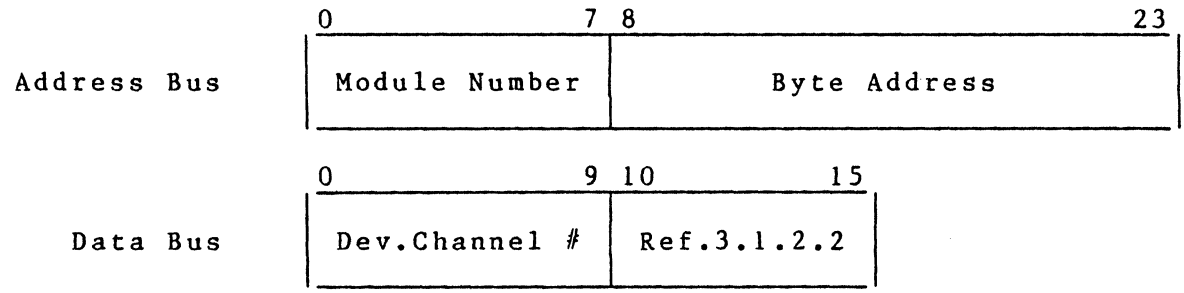
3.1.2.3 Interrupts

Whenever a channel interrupt level (see subsection 5.2.4) is nonzero and an operation initiated by an Output Task Word (see subsection 5.2.5) or Output Control Word (see subsection 5.2.6) instruction is completed or the attention bit is set in the status word (subsection 5.2.14.2), an interrupt is attempted. If a NAK response is received during an interrupt cycle, the MPTC stores the interrupt until it detects a pulse on the BSRINT

MPTC Memory Write Request.



MPTC Memory Read Request.
Request Cycle.



Response Cycle.

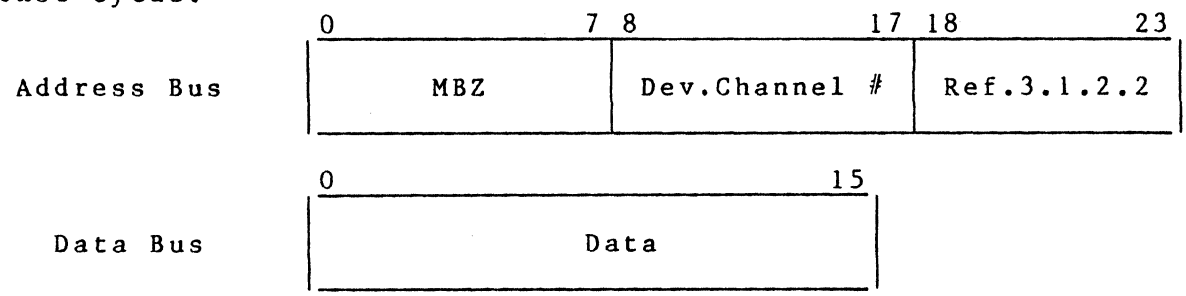


Figure 3-2 Address and Data Bus Configuration for Read and Write Memory Access.

(Resume Interrupts) line. The interrupt is then retried. Once an interrupt has been saved (as the result of a NAK response), the MPTC is capable of receiving commands and/or conducting data transfers on any of the other channels (subject to normal constraints). The channel with the pending interrupt, however,remains busy and the MPTC does not accept commands issued to that channel (except Output Control Word).

If the interrupt level of a channel is zero (either via an initialize process or loaded to zero), no interrupts are attempted for that channel. If a condition or event occurs which would normally cause an interrupt, the appropriate bits in the status word are set but no interrupt is attempted or saved.

If the interrupt level is set to zero when an interrupt is pending (via Output Control Word or Master Clear), the pending interrupt is discarded.

Figure 3-3 illustrates the address and data bus configuration for interrupt sequences. The channel number supplied on the data bus during an interrupt is the channel number used in the most recent Output Address instruction for the associated device. If no previous Output Address instruction has occurred at the time of an interrupt, the low-order bit of the channel number is Zero (see subsection 3.1.1).

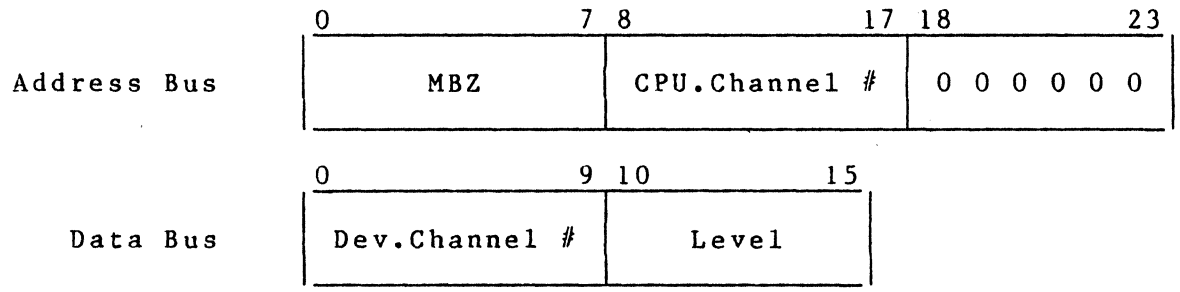


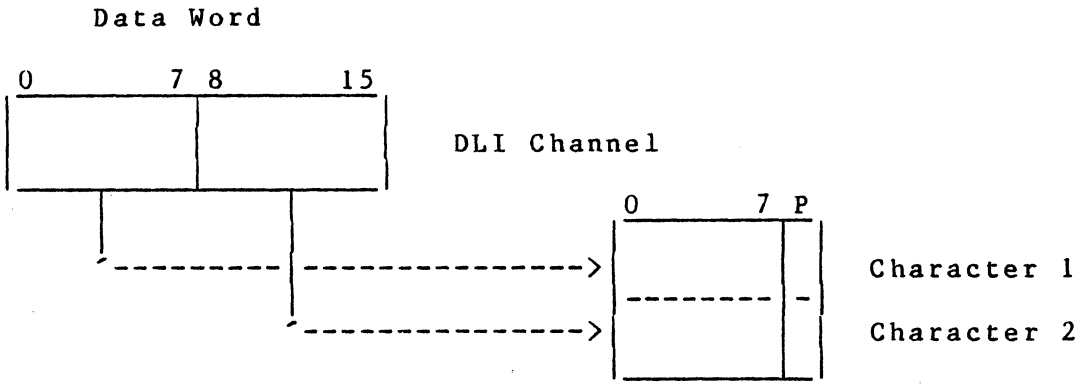
Figure 3-3 Address and Data Bus Configuration for Interrupt Sequences

3.1.3 Overview of Tape Operation

Associated with each device is a set of registers in the MPTC which are loaded by software and specify the parameters required for tape operation. In addition to range and address registers, a configuration register contains the mode of operation and a task register holds command codes. To perform a specific operation, the software first loads the configuration, address, and range registers. The task register is loaded last and specifies the operation to be performed. The MPTC begins command execution when it receives the task word.

Commands addressed to a nonbusy tape device are always accepted but execution may be delayed as described in subsection 3.1.1. All commands addressed to a busy tape device are rejected (NAK response on Megabus) except the Output Control Word (see subsection 5.2.6).

Data being written on or read from a tape is handled on a byte basis. For 9-track tapes, all 16 bits of a data word are transferred to or from the tape as follows (odd parity is written on tape and checked when read):



3.2 Compatibility

DPS6 1/2-inch magnetic tape subsystems provide read and write interchange with corresponding DPS6 and foreign tape subsystems with read and write tapes which meet ANSI standards (see subsection 1.2.3).

DPS6 software drivers read and write 9-track tapes in the PE/GCR recording method on the GCR-MTS.

Additional format and interchange information is given in subsection 5.1 and Section 8.

3.3 Main Memory Storage

Main memory requirements for the tape driver are defined in the Magnetic Tape Driver Software Specification (TBD).

3.4 Implementation

The MPDC serves as a firmware driven controller and provides the necessary bus and device/controller adapter interfaces and associated buffering and control facilities. Detailed information on MPDC implementation can be found in the Medium Performance Device Controller Product Manual (TBD).

4. INTERFACES

4.1 User Interfaces

No specific user action is required to load or initialize the GCR-MTS other than that required during subsystem installation for identification of subsystem configuration. Specific user actions required for the operation of tape devices can be found in the appropriate operation manual for the device.

4.2 External Interfaces

4.2.1 Megabus Interface

The MPDC attaches to the Megabus as a typical I/O controller. The Megabus EPS-1 contains the specific details for this interface (see Figure 2-1).

4.2.2 Controller/Adapter Interface (CAI)

The GCRA attaches to the MPDC as a standard MPDC adapter. The MPDC EPS-1 contains specific details for this interface.

4.2.3 Controller Level Interface for the GCR/PE Formatter/Controller (CLI-F/C)

Refer to the appropriate controller specification(s) for more detailed information than presented in this subsection. The controller specification also represents the governing document in terms of controller functionality.

The CLI-F/C interface consists of 54 signal lines between the GCRA and the GCR/PE Formatter/Controller (F/C). Figures 4-1 and 4-2 group these signals as input, output, and bi-directional data signals as viewed from the F/C.

Two 60 pin socket connectors, P/N 95967370 or Ansley 609-6030 or equivalent, are required with two 60 pin flat ribbon cables to interface the F/C to the GCRA.

			SIG	GND
	---- Transport Address ----	AD0- ----->	1	2
	---- " " ----	AD1- ----->	3	4
	---- Command Line ---------	CMD0- ---->	5	6
	---- " " ---------	CMD1- ---->	7	8
	---- " " ---------	CMD2- ---->	9	10
	---- " " ---------	CMD3- ---->	11	12
	---- Initiate Command -----	START- --->	15	16
	---- Density Select -------	DS0- ----->	13	14
	---- " " -------	DS1- ----->	45	46
	---- Transfer Acknowledge -	TRAK- ---->	19	20
	---- Terminate Command ----	STOP- ---->	17	18
	---- System Reset ---------	RESET- --->	39	40
	---- Select Multiplex -----	SLX0- ---->	43	44
	---- " " -----	SLX1- ---->	41	42
Group Coded Recording Adapter	---- " " -----	SLX2- ---->	47	48
	<--- Bi-directional Data --	DATA0- --->	23	24
	<--- " " --	DATA1- --->	25	26
GCRA	<--- " " --	DATA2- --->	27	28
	<--- " " --	DATA3- --->	29	30
	<--- " " --	DATA4- --->	31	32
	<--- " " --	DATA5- --->	33	34
	<--- " " --	DATA6- --->	35	36
	<--- " " --	DATA7- --->	37	38
		LSB of Data		
	<--- " "	DATAP- --->	21	22
		Odd Parity		
	<--- End Of Tape ----------	EOTS- -----	53	54
	<--- Beginning Of Tape ----	BOTS- -----	55	56
	<--- File Protected -------	FPTS- -----	57	58
	<--- Rewinding ------------	REWS- -----	59	60
	<--- Reserved ------------------------		51	52
	<--- Reserved ------------------------		49	50
A CONNECTOR			F/C J7 CONNECTOR	

Figure 4-1 CLI-F/C Interface Cable A

			SIG	GND
	<--- On line	ONLS-	49	50
	<--- Ready	RDYS-	53	54
	<--- GCR Density	HDENS-	51	52
	<--- Write Mode	WRTS-	55	56
	<--- ID Burst	IDBRST-	25	26
	<--- File Mark	TMS-	31	32
	<--- Command Reject	REJECT-	33	34
	<--- Data Overrun	OVRNS-	35	36
	<--- EPROM Error	ROMPS-	39	40
	<--- Busy	BUSY-	19	20
	<--- Data Check Error	DATACHK-	37	38
	<--- Corrected Error	CRERR-	41	42
	<--- Bus Parity Error	BUPER-	47	48
Group Coded Recording Adapter GCRA	<--- Error Multiplex Bus	ERRMX0-	3	4
	<--- " " "	ERRMX1-	5	6
	<--- " " "	ERRMX2-	7	8
	<--- " " "	ERRMX3-	9	10
	<--- " " "	ERRMX4-	11	12
	<--- " " "	ERRMX5-	13	14
	<--- " " "	ERRMX6-	15	16
	<--- " " "	ERRMX7-	17	18
	<--- " " "	ERRMXP- (Odd Parity)	1	2
	<--- Transfer Request	TREQ-	21	22
	<--- Receiving Data	RECV-	23	24
	<--- Block or File Mark	BLOCK-	43	44
	<--- End of Data Pulse	ENDATP-	29	30
	<--- Reserved		57	58
	<--- Reserved		59	60
B CONNECTOR			F/C J6 CONNECTOR	

Figure 4-2 CLI-F/C Interface Cable B

The electrical interface requires that all signals are low true and are driven by two types of 2-state devices, as illustrated below:

- Unidirectional lines -

  SN7438 or equivalent driver with DN8837 or equivalent as a receiver with two resistors at the input to the receiver at the GCRA connector input lines or at the F/C termination for GCRA output lines, 180 ohm resistor to +5 v. and 390 ohm resistor to ground.

- Bidirectional lines -

  DN8838 or equivalent receiver/driver connected together to a transmission line with 180 ohm resistor to 5 v. and 390 ohm resistor to ground at both the GCRA connector and F/C termination.

4.2.3.1 Input Lines (GCRA to F/C)

4.2.3.1.1 Address Lines (AD0, AD1)

These lines are decoded in the F/C to select one of four transports. The select code is as follows:

AD0	AD1	TRANSPORT SELECTED
0	0	0
0	1	1
1	0	2
1	1	3

If the F/C is not BUSY the address lines may change to select another transport. The delay between the selection of a new F/C and the stabilization of the selected F/C status lines is 150 ns maximum. For command operations the address lines must be stable for 90 ns prior to the START signal leading edge and must remain stable until assertion of BUSY.

4.2.3.1.2 Command Lines (CMD0, CMD1, CMD2, CMD3)

These lines are decoded in the F/C to select 1 of 16 commands. They are stable 90 ns before the rising edge of the START signal, and remain true until BUSY is asserted at which time START is reset. The commands are coded as shown in Table 4-1 and reference section 5.2.5 for command interpretation.

CMD0	CMD1	CMD2	CMD3	COMMAND	DESCRIPTION
0	0	0	0	NOP	No Operation
0	0	0	1	CLR	Drive Clear
0	0	1	0	DMS	Diagnostic Mode Set
0	0	1	1	SNS	Sense Drive Status
0	1	0	0	RDF	Read Forward a Block
0	1	0	1	RDB	Read Backward a Block
0	1	1	0	WRT	Write a Data Block
0	1	1	1	LWR	Loop Write To Read
1	0	0	0	BSF	Backspace a File
1	0	0	1	BSB	Backspace a Block
1	0	1	0	FSF	Forward Space a File
1	0	1	1	FSB	Forward Space a Block
1	1	0	0	WTM	Write Tape Mark Block
1	1	0	1	ERG	Erase a Gap
1	1	1	0	REW	Rewind to BOT
1	1	1	1	RUN	Rewind and Unload

Table 4-1 Command Codes

4.2.3.1.3 Control Lines

DENSITY SELECT (DS0, DS1):

These signals enable density selection by the controller. When the F/C is at the BOT and the local density mode is disabled (switch on the interface card), the F/C writes tapes in the density selected by DS0 and DS1 (Reference section 5.2.2, bit 8). The table below shows the density select decode:

DS0	DS1	DENSITY
0	0	PE - 1600 bpi
1	0	GCR - 6250 bpi
0	1	RFU
1	1	RFU

These lines are stable at the rising edge of the START signal and remain stable for the duration of START. The DSX lines are ignored on all commands which are not write type commands.

START:

The transition of this line from a false to a true state loads the tape Command, Address and Density into the selected F/C registers and causes the command to be executed. This signal remains asserted until the leading edge of the BUSY line is detected.

STOP:

This line is used to terminate data transfer on a read or write type command. When true in response to TREQ on a write type command, STOP indicates that the last byte of data is present on the data bus. STOP, when true in response to TREQ on a read type command, signals the F/C that no more data is to be sent across the interface.

When STOP is received on a write type command, the formatted postamble is generated after the last byte is written.

When STOP is received on a read type command, data transfer across the interface is terminated. Any bytes remaining in the record are checked for correct parity but not transmitted, and the read head stops in the gap at the end of the record. STOP remains asserted until the trailing edge (transition from a true to a false state) of BUSY is detected.

If STOP is asserted at the completion of a space type operation (FSB, BSB, FSF, BSF), no further tape motion occurs until another command is initiated.

TRAK:

Transfer Acknowledge; this signal is used in response to TREQ (Transfer Request) to send data across the interface. TREQ when true on a write type command indicates that the F/C is requesting a byte of data, and the TRAK line being true indicates that the data bus contains the desired byte.

TREQ on a read type command indicates that the F/C has placed a byte on the data bus. TRAK in response to TREQ indicates that the byte has been accepted.

The signal protocol for TREQ and TRAK is the same for both a read and a write. When TREQ is set, it remains asserted until the leading edge of TRAK (or STOP) is detected. TRAK also remains asserted until the trailing edge (transition from a true to a false state) of TREQ is detected.

RESET:

When true, this line causes the F/C to terminate any operation in progress. All status indications are reset and BUSY remains asserted until the reset operation has been completed. This line allows the addressed F/C (transport) to be cleared to initial, functional, conditions by one signal.

SLX0, SLX1, SLX2:

These three lines are used to control the data placed on the error and status bus (ERRMXP, 0 through 7). The codes used to determine the data placed on the error and status bus are shown in Table 4-2. The definitions given by the table are valid only as a part of ending status, after the reset of BUSY, and the completion of the command operation. The selected multiplexer byte is stable 150 ns after the Select Multiplexer code.

SLX2	SLX1	SLX0	CONTENTS OF ERROR AND STATUS BUS
0	0	0	Dead Track Information Tracks P-7
0	0	1	Read/Write Errors
0	1	0	Diagnostic Aid Bits
0	1	1	Drive Sense Byte
1	0	0	RFU
1	0	1	RFU
1	1	0	RFU
1	1	1	RFU

Table 4-2 Multiplex Control

4.2.3.2 Output Lines (F/C to GCRA)

4.2.3.2.1 Transport Status

ONLS - On Line Status:

When true, this line indicates that the selected transport is on line. It may or may not be READY.

RDYS - Ready Status:

When true, this line indicates that the selected transport has tape loaded in the tape path and is ready to execute a command. This line returns to a false state during the execution of a rewind command and remains at that level until the rewind is completed and BOT is detected, at which time it returns to a true state.

HDENS - High Density Status:

When true, this line indicates that the selected transport is in GCR status. It is in PE status when the line is false when the tape has just been loaded, unloaded or the transport is powered up. It is set to true when:

- on write operation from BOT reflects the device local switch setting.
- on read or space operations from BOT when the F/C automatically caused detection and interpretation of the density identification area (ID burst) and indicates the magnetic tape is written in GCR format.

EOTS - End of Tape Status:

When true, this line indicates that the selected tape transport is on or has passed over (in the forward direction) the EOT reflective tab. The EOTS signal remains asserted until a reverse direction command (such as Rewind or Backspace) is accepted by the formatter and the reflective marker passes over the sensor in the backward direction. Therefore, the program only needs to check for EOT after completion of writing each record.

BOTS - Beginning of Tape Status:

When true, this line indicates that the reflective tab at the beginning of the tape is being detected by the sensor.

FPTS - File Protected Status:

When true, this line indicates that the selected transport is inhibited from writing (i.e., the write enable ring is not inserted).

WRTS - Write Status:

When true, this line indicates that the selected transport is in write status. When false, this line indicates that the transport is in read status.

REWS - Rewinding Status:

When true, this line indicates that the selected transport is in the process of rewinding to the beginning of the tape. This line returns to a false state when the BOT reflective strip is detected. This line is also true when the F/C is on line but not READY.

4.2.3.2.2 Formatter Status

IDBRST - Identification Burst:

When true for either a PE or GCR tape, this line indicates that an ID burst has been detected off the BOT marker on read or write commands, in real time, when BUSY is true. This signal may be used in conjunction with DATACHK or REJECT to indicate that the transport was unable to write a PE or GCR ID burst correctly. The HDENS status line may be interrogated to determine if that tape was written in 1600 bpi or 6250 bpi.

If the ID procedure is performed correctly the F/C proceeds with the initiated command. If the ID procedure is incorrect the IDBRST remains asserted together with REJECT and reject code also asserted in the CDC transport in the buffered mode; in the STC transport and CDC transport in the unbuffered mode only the DATACHK is asserted.

TMS - Tape Mark Status:

When true, this line indicates that the record which the selected transport has just read is a tape mark. This line is asserted following a Write Tape Mark command or any read or space command when a Tape Mark Block is detected. The TMS is reset by the next command issued unless that command is a Sense Drive Status or No Operation.

REJECT:

When true, this line indicates that the command accompanying the START signal has been rejected by the formatter. Reference section 5.2.5.13.3 for all condition codes setting this line true.

OVRNS - Overrun Status:

When true, this signal indicates that the F/C required the transfer of data over the interface and found that a previous request for data transfer had not been acknowledged. This signal indicates the failure of the adapter to transfer a character before the next character transfer was required. It is applicable to both read and write operations; DATACHK line is also asserted following the read validity checking. The F/C terminates the data transfer on detection of an Overrun and completes formatting the data block.

ROMPS - ROM Parity Error Status:

When true, this line indicates that the control memory portion of the F/C detected a word having incorrect parity on the STC or that the I/O board microprogram had a check sum error on the CDC. This line is indicative of serious

hardware malfunctions which should be repaired before attempting to use the F/C again.

BUSY - Formatter Busy:

This signal goes true at the leading edge of the START signal when a new command is accepted. It remains at that level until the operation has finished and the transport begins to slow down in order to stop in the interrecord gap. On a REW or RUN command, this signal is asserted until the REW or RUN command has been accepted by the drive. The F/C does not remain busy for the duration of the REW or RUN command. At that time it returns to a false state. For continuous on-the-fly operation, a new command should be issued as soon as BUSY is at a false state.

4.2.3.2.3 Error Status

DATACHK - Data Check Status:

Data Check is indicated when any of the following error conditions exist:

- Not Compatible - When an attempt is made to read an NRZI tape on a PE/GCR transport. This also sets reject status.
- Multitrack Error - More than one dead track during a PE or more than two dead tracks during a GCR operation. This sets Data Check in PE.
- CRC Error - A CRC error is detected during a GCR read or write operation.
- End-of-Block is sensed before any data bytes are detected during a GCR or PE read operation.
- No data if transferred on a read operation.
- Data is detected on an erase operation.
- Write Tape Mark Check - This is set when a tape mark is not written properly.
- Partial Record - This is set when an IBG (inter-block gap) is detected before the end of data is recognized.
- ID Burst Check - This is set along with identification burst status (IDBRST) if the ID burst cannot be read on a read or write command.
- IBG Detected - This is set if an IBG is detected while writing data.

CRERR - Corrected Error:

When true, this line indicates that a single track error has been corrected during a PE read or GCR write command operation, or that single or double track error correction has taken place during a GCR read command.

BUPER - Bus Parity Error:

When true, this line indicates that the F/C detected even parity on the data bus for a byte of data sent across the interface during a write type operation. It indicates that the data written on tape may be incorrect since data transmission is not immediately halted but is allowed to proceed to normal completion.

ERRMX0 through 7, P - Multiplexed Error Bus:

These nine lines contain error, status, and diagnostic information about the previous operation. The meaning of the information on the bus is determined by the state of the SLX0, SLX1, and SLX2 lines. Up to eight bytes of additional error and status information can be sent across the interface under control of the SLX0, SLX1, and SLX2 lines. Reference section 5.2.5.13 for more details.

4.2.3.2.4 Control Lines

TREQ - Transfer Request:

When true, this line indicates that the formatter is ready to accept data on the data bus (write type operation), or has placed data on the bus (read type operation) for transmission across the interface. The transition from a true to a false state indicates the following:

- Data on the bus has been accepted by the F/C for a write type operation.
- Acknowledgment of transmission of the data across the interface (i.e., TRAK has been received for a read type operation).

Further information on this signal can be found in the description of TRAK in subsection 4.2.3.1.3, Control Lines.

RECV - Receiving Data:

When true, this line indicates that the F/C is expecting to receive data on the bidirectional data bus. It is asserted only on write type commands, and may be used by the interface to gate data out onto the bus.

BLOCK - Data Block:

When true, this signal indicates that a data block or a tape mark block is passing under the read head. The positive edge of this signal may be used by the interface to count the number of blocks passed over during a forward or backward space command.

ENDATP - End of Data Pulse:

This signal is approximately 250 to 400 ns long and occurs after all data has been transferred on a read operation. It can be used by the interface to check that the number of bytes transferred agrees with the expected amount.

4.2.3.3 Data Signals (DAT P, 0 through 7

These bidirectional lines are used to transmit data to and from the F/C in conjunction with TREQ and TRAK. The lines always maintain odd parity on both read and write commands.

The parity is checked by the F/C on write operations and by the GCRA on read operations.

4.2.3.4 Timing Considerations

Typical examples of interface timings are given for write, read, and space type operations. Refer to the appropriate timing diagrams in the OVP specifications.

4.2.3.4.1 Write Type Operation

This operation is initiated by placing the transport address on the AD0 and AD1 lines, the command on the CMD0, 1, 2, and 3 lines, and the density on the DENS line (for write commands only) before issuing the START signal. These lines may be asserted simultaneously since the F/C has an internal deskew capability of about 90 ns.

The address, command, and density lines must remain stable until BUSY is received at the interface. This signal indicates that these lines have been stored in a register. Hence, they may change state once BUSY has been received.

Upon determination that a new command has been started, the F/C resets the status from the previous operation. The status lines should be considered invalid until BUSY is reset. Initiation of a write type (WRT or LWR) command causes the F/C to generate RECV, indicating to the interface that it expects data on the bidirectional data bus.

A request for data is generated by raising the TREQ line. The interface replies by placing a byte on the data bus and raising TRAK. Both the data and TRAK may be asserted

simultaneously. If the F/C does not receive TRAK within approximately 10 milliseconds after requesting the first byte, TREQ is reset and DATACHK, REJECT, and REJPLS are generated. When TRAK is received, the F/C delays approximately 90 ns before strobing the data into its data buffer and resetting TREQ. The fall of TREQ signals to the interface that the data bus may change state and that TRAK must be reset. TREQ is not asserted again until TRAK is reset.

This handshaking sequence continues until the interface transfers its last byte of data. This event is signaled when the interface responds to TREQ by placing the data on the bus, then raising STOP rather than TRAK. Timing considerations for STOP are the same as for TRAK.

Upon receipt of STOP, the F/C resets TREQ and completes writing the record with the appropriate postamble format. Upon completion of the readback check, the F/C sets the appropriate status latches, signals to the transport to stop tape motion, and resets BUSY. For continuous on-the-fly operation, the DATACHK line should be checked for errors once BUSY is reset, and then a new command may be issued.

4.2.3.4.2 Read Type Operation

Initiation of a read forward command is begun by placing the address of the selected transport on AD0 and AD1, the appropriate command on the CMD0, 1, 2, and 3 lines, and then asserting START. Because of an internal deskew of approximately 90 ns these lines may be asserted simultaneously.

Upon detection of the START signal, the F/C stores the transport address and the command into a register and asserts BUSY. Once BUSY is seen at the interface, the address and command lines are allowed to change state.

After asserting BUSY, the F/C resets the status from the previous operation and signals the transport to begin tape motion. Data from the tape is detected, corrected when appropriate, and presented to the interface. The F/C places a byte of data on the data bus (odd parity) and delays approximately 90 ns before raising TREQ.

The interface signals to the F/C that it has accepted the data byte by asserting TRAK. When this signal is received by the F/C, it resets TREQ and changes the data on the bus. Once TREQ has been reset, it is not asserted again until new data is available and TRAK has been reset. This handshaking sequence continues until all the data has been transmitted. When the end of data has been detected and all the data has been transmitted, the F/C signals to the interface that data transmission has finished by asserting the ENDATP line for approximately 250 to 400 ns. After the transport has been signaled to stop the appropriate status lines are asserted and BUSY is reset.

For continuous on-the-fly operation, the DATACHK line should be checked for errors once BUSY has been reset. Then a new command should be issued.

4.2.3.4.3 Spacing Type Operation

Commands such as Back Space Tape Mark, Back Space Block, Forward Space Tape Mark and Forward Space Block are initiated by placing the transport address on the AD0 and AD1 lines, the command on the CMD0, 1, 2, and 3 lines, and asserting START. These lines may be asserted simultaneously since the F/C has an internal deskew capability of about 90 ns.

The address and command lines remain stable until BUSY is received at the interface. This signal indicates that these lines have been stored in a register; thus, they may change state once BUSY has been received.

Upon determination that a new command has been issued, the F/C resets the status from the previous operation. Therefore, the status lines should be considered invalid until BUSY is reset. The F/C then signals the selected transport to begin tape motion.

As a block of data passes under the read head, the signal BLOCK is sent to the interface; when the inter-block-gap is detected, this signal is reset. At this time the F/C checks to see if STOP (or TMS in the case of a Forward Space Tape Mark or Backspace Tape Mark command) is asserted. If none of these are set, the F/C allows tape motion to continue until another block of data is detected and these same lines are checked again.

The leading edge of the BLOCK signal may be used by the interface to count the number of blocks passed over. If it is determined that no more blocks are to be spaced, STOP must be asserted within 2 microseconds after detection of the leading edge of BLOCK. This action allows the STOP line to be checked when BLOCK is reset. If it is desired to space only one block, STOP may be asserted throughout the command execution. In either case it must not reset until busy is reset.

The transport begins to stop in the gap if the last record passed over was TMS for a Back Space Tape Mark or Forward Space Tape Mark command, or STOP is asserted when the inter-block gap is detected. The F/C then signals the transport to terminate motion, allowing it to stop within the proper distance.

4.2.4 Device Level Interface of the F/C (DLI-F/C)

Figure 4-5 illustrates the signal lines of the device level interface, DLI, of the F/C for STC transports only. Refer to the appropriate device product specification for a detailed description of each line.

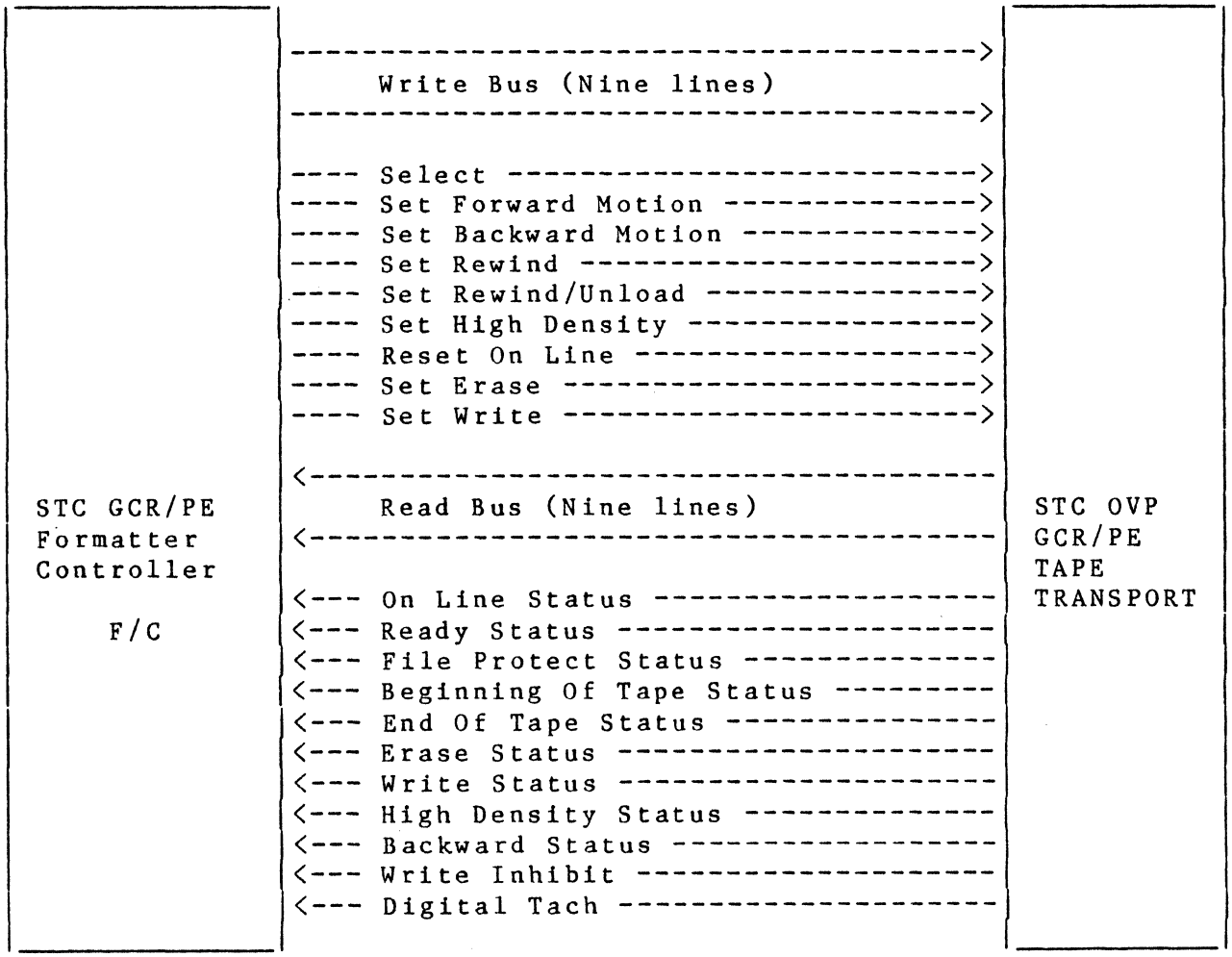


Figure 4-3 STC DLI-F/C Interface

5. MEDIA AND INSTRUCTION FORMATS

5.1 Media Formats

A detailed description of the media formats for the GCR-MTS tapes is not presented here. Detailed information is available in the appropriate ANSI specification for 6250 CPI Group Coded Recording (GCR) and 1600 CPI Phase Encoded (PE), and the specification for unrecorded magnetic tape.

The following figures and tables illustrate the various formats and physical tape layouts which the GCR-MTS is capable of recording and reading.

5.1.1 1600 CPI Phase Encoded (PE) Recording

Figure 5-1 shows the orientation and layout of the usable recording area as defined by ANSI for 1600 CPI, PE tapes.

Figure 5-2 shows the orientation and layout of the recording format as defined by ANSI for 9-track and 1600 CPI, PE tapes.

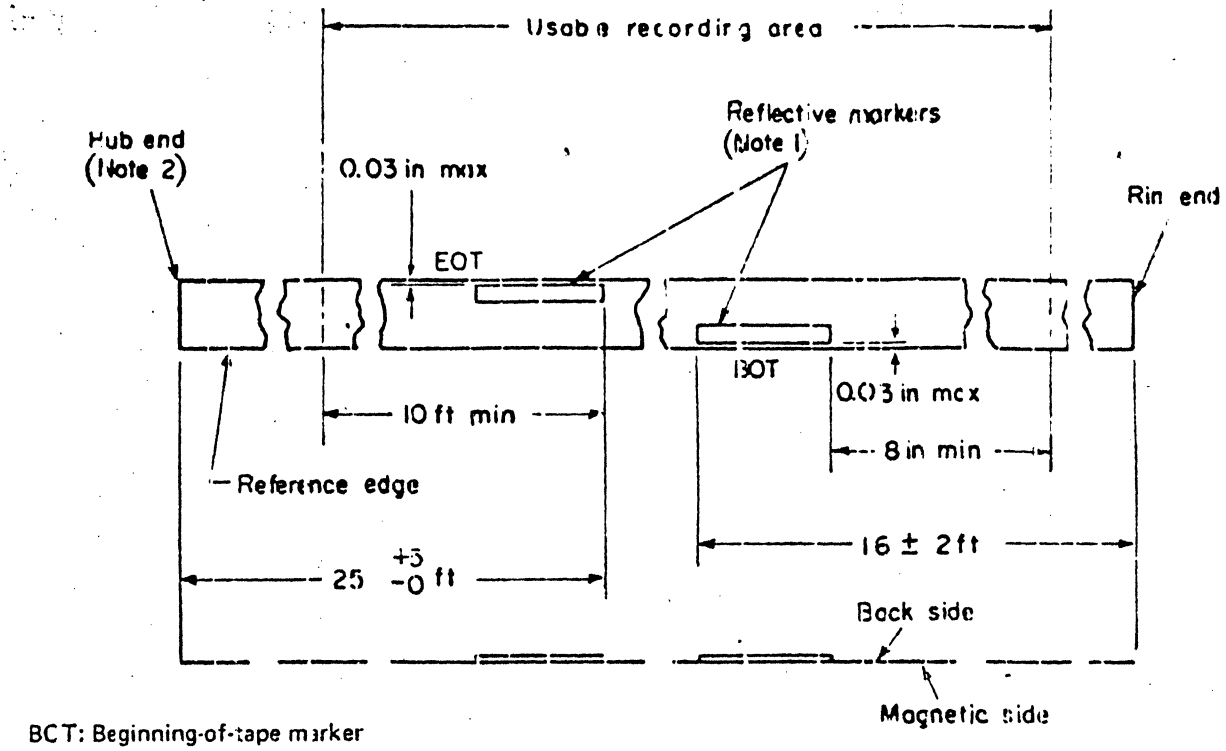
All phase encoded data blocks contain a preamble, data, and postamble.

5.1.2 6250 CPI, Group Coded Recording (GCR)

Figure 5-3 shows the orientation and layout of the usable recording area as defined by ANSI for 9-track GCR tapes.

Figure 5-4 shows the orientation and layout of the recording format as defined by ANSI for 9-track GCR tapes.

Figure 5-5 is a more detailed breakdown of the GCR format as recorded on tape. Table 5-1 represents the data groups as received by the F/C from the GCR-MTS which are then encoded into the group coded recording format and stored on tape. Table 5-2 gives the actual 5-bit record values as encoded from each 4-bit data value.

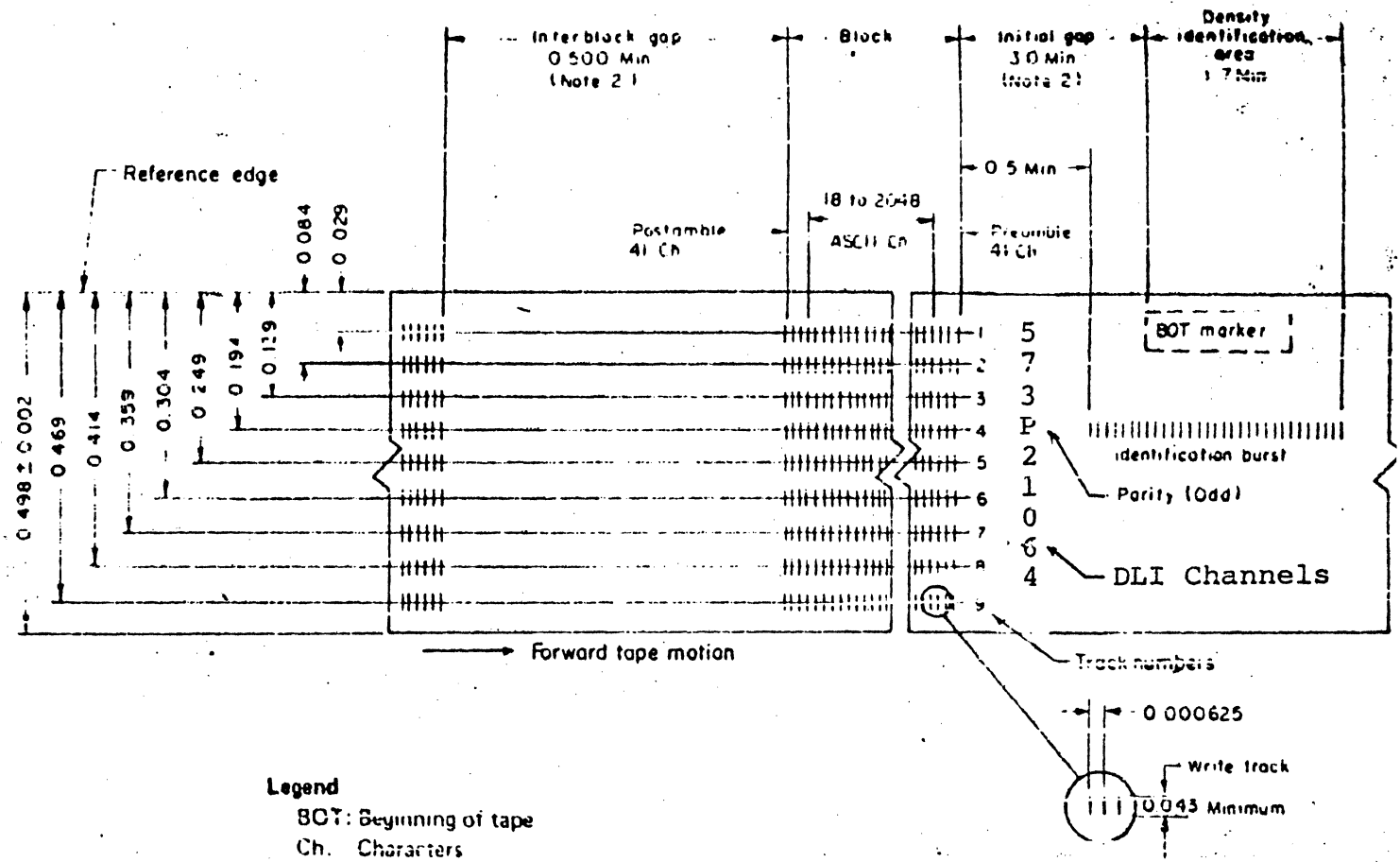


NOTES:

(1) Photoreflective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch ± 0.2 inch; width, 0.19 inch ± 0.02 inch; thickness, 0.0008 inch maximum.

(2) Tape shall not be attached to the hub.

Figure 5-1 Usable Recording Area
(1600 CPI, PE)



Legend

BOT: Beginning of tape
Ch. Characters
CPI: Characters per inch
Min: Minimum

NOTES:

(1) Tape is shown with oxide side up. Read/Write head on same side as oxide.
(2) Tape to be fully saturated in the erased direction in the interblock gap and the initial gap.
(3) The identification burst extends past the trailing edge of the BOT marker.
(4) All dimensions are given in inches.
(5) There is a track placement tolerance of ± 0.003 inch for each track.

Figure 5-2 Recording Format (1600 CPI)

The definitions of GCR terminology are as follows:

- Alternate Record Code: Five bits along any track representing encoded 4 bits of data, padding characters, check characters, residual characters, or a combination of these characters, on tape.

- Automatic Read Amplification (ARA) Burst: A string of bits in all tracks for setting up the amplifiers.

- Automatic Read Amplification (ARA) Identification (ID) Character: A special control block used at the end of the ARA burst to identify the ARA burst when reading backward to the load point.

- Auxiliary Cyclic Redundancy Check (CRC) Character: A CRC character usable for error-detection purposes.

- Beginning-of-Tape (BOT) Marker: A photoreflective marker placed on the tape to indicate the beginning of the permissible recording area.

- Block: A group of contiguous recorded characters considered and transported as a unit containing one or more logical records. Blocks are separated by an interblock gap.

- Control Subgroups: Those special subgroups of characters that (except for the subgroup containing the last character) have sets of identical control five-serial-bit values in the nine tracks.

- End Mark: A subgroup used to demark the residual area group. When the media movement is in a forward direction, it denotes that the next group is the residual group.

- Mark 1: A subgroup used to demark data groups from other control subgroups. When the media movement is in a forward direction, it denotes the onset of data groups.

- Mark 2: A subgroup used to demark data groups from other control subgroups. When the media movement is in a forward direction, it denotes the onset of other control subgroups.

- Second Control Subgroups: The second subgroup and next to last subgroup of a record.

- Sync Control Subgroup: A subgroup used to indicate recorded frequency and phase to allow synchronization of the variable-frequency clock (VFC).

- Terminator Control Subgroups: The first subgroup and last subgroup of a record.

- Cyclic Redundancy Check (CRC) Characters: Characters usable for error detection.

- Cyclic Redundancy Check (CRC) Data Group: A specially formatted data group containing one of the CRC characters, the residual character, and an error-correcting code (ECC) character.

- Data Group: Seven data characters plus an ECC character accumulated as a group prior to the record code value translation.

- Density: The nominal distribution per unit length of recorded information, usually expressed in characters per inch.

- End-of-Tape (EOT) Marker: A photoreflective marker placed on the tape to indicate the ending of the permissible recording area.

- Error-Correcting Code (ECC) Character: A special character usable for error detection and correction.

- Flux Reversal Position: The point that exhibits the maximum free-space surface flux density normal to the tape surface.

- Flux Spacing: The space between successive flux transitions.

- Group-Coded Recording (GCR): A recording technique that collects groups of characters and encodes them prior to putting them on tape.

- Interblock Gap: A dc-erased section of tape separating blocks of information.

- Last Character: The last character in each block, which restores magnetic remanence in all tracks to the dc erase polarity.

- Postamble: Groups of special signals recorded at the end of a block on tape for the purpose of electronic synchronization.

- Preamble: Groups of special signals recorded at the beginning of each block on tape for the purpose of electronic synchronization.

- Record Code: The coded representation of data, padding characters, check characters, and residual characters on tape.

- Residual Character: The character that occupies the seventh group position of the CRC data group and contains two data byte counts, one to modulo 7 and one to modulo 32.

- Residual Group (Group Positions): The group that contains the extra characters (the remainder of the number of characters divided by 7), an auxiliary CRC character, and an ECC character. Each such extra character is a residuum character.

- Resync Burst: A set of control subgroups identifying format resynchronization points in a block. It is intended that read-back circuits be able to resynchronize operations when sensing such bursts.

- Skew: The deviation of bits within a tape character from the intended or ideal placement, which is perpendicular to the reference edge.

- Storage Group: Ten characters created from the data group via the record code value translation.

- Subgroup: One half of a data or storage group. See control subgroups.

	DATA GROUP		STORAGE GROUP	
PHYSICAL TRACKS	DATA SUBGROUP "A"	DATA SUBGROUP "B"	STORAGE SUBGROUP "A"	STORAGE SUBGROUP "B"
1	D D D D	D D D E	X X X X X	X X X X X
2	D D D D	D D D E	X X X X X	X X X X X
3	D D D D	D D D E	X X X X X	X X X X X
4	P P P P	P P P P	X X X X X	X X X X X
5	D D D D	D D D E	X X X X X	X X X X X
6	D D D D	D D D E	X X X X X	X X X X X
7	D D D D	D D D E	X X X X X	X X X X X
8	D D D D	D D D E	X X X X X	X X X X X
9	D D D D	D D D E	X X X X X	X X X X X
GROUP POSITIONS	1 2 3 4	5 6 7 8	1 2 3 4 5	6 7 8 9 10

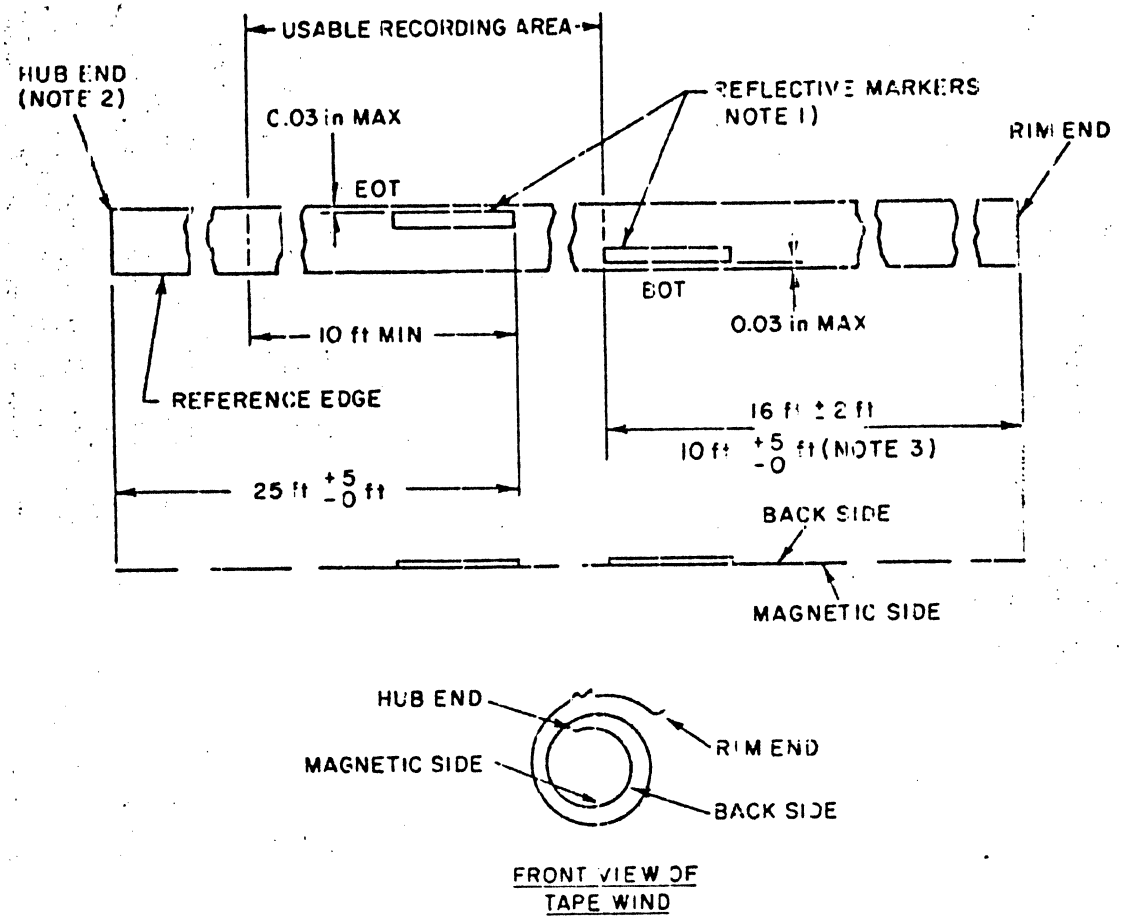
Table 5-1 Data Group to Storage Group Example

NOTE:

Tape is recorded in 9-bit characters (across tape) by 10 bits long. This 90-bit group is called a "storage group." Prior to the record code values conversion there are eight linear bits, made up of seven data bits and one check bit, This group of 72 bits is called a "data group." The 4-bit and 5-bit combinations are called "subgroups."

DATA VALUES (GROUP POSITIONS: 1 2 3 4/5 6 7 8)	RECORD VALUES (GROUP POSITIONS: 1 2 3 4 5/6 7 8 9 10)
0 0 0 0	1 1 0 0 1
0 0 0 1	1 1 0 1 1
0 0 1 0	1 0 0 1 0
0 0 1 1	1 0 0 1 1
0 1 0 0	1 1 1 0 1
0 1 0 1	1 0 1 0 1
0 1 1 0	1 0 1 1 0
0 1 1 1	1 0 1 1 1
1 0 0 0	1 1 0 1 0
1 0 0 1	0 1 0 0 1
1 0 1 0	0 1 0 1 0
1 0 1 1	0 1 0 1 1
1 1 0 0	1 1 1 1 0
1 1 0 1	0 1 1 0 1
1 1 1 0	0 1 1 1 0
1 1 1 1	0 1 1 1 1

Table 5-2 Record Code Values



Legend

BOT: Beginning-of-tape marker

EOT: End-of-tape marker

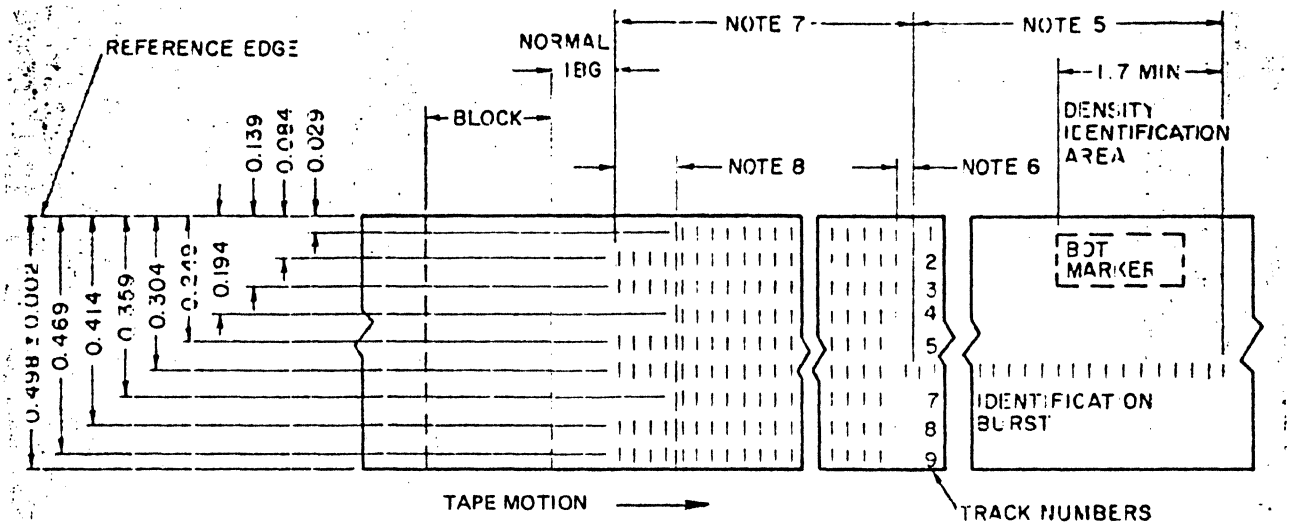
NOTES:

(1) Photoreflective markers shall not protrude beyond the edge of the tape and shall be free of wrinkles and excessive adhesive. Marker dimensions: length, 1.1 inch ± 0.2 inch; width, 0.19 inch ± 0.02 inch; thickness, 0.0003 inch maximum.

(2) Tape shall not be attached to the hub.

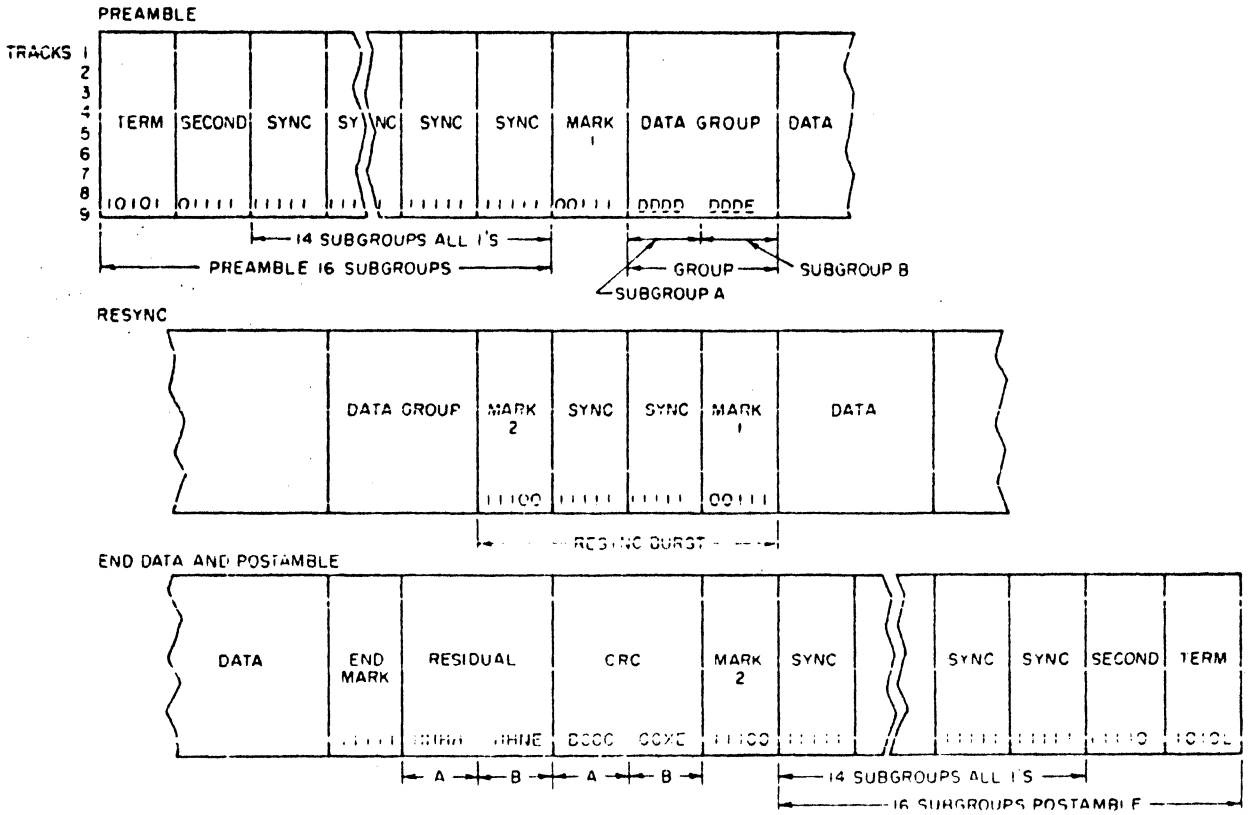
(3) Two values for placement of the BOT marker are given, both of which can be handled by most tape units. The indicated value of 16 feet ± 2 feet is the current specified dimension.

Figure 5-3 Usable Recording Area (6250 CPI, GCR)



NOTES:
(1) Tape is shown in 6250 mode, oxide side up.
(2) All dimensions are given in inches.
(3) Track placement tolerance is ± 0.003 for each track
(4) Tape to be fully saturated in the erase direction in the interblock gap and the ID area.
(5) ID burst
(6) Undefined gap
(7) ARA burst
(8) ARA ID characters

Figure 5-4 Recording Format (6250 CPI, GCR)



Legend:

D: Data characters	C: CRC character
H: Pad or data character	N: Auxiliary CRC character
X: Residual character	L: Last character
E: ECC character	B: CRC or pad character

Figure 5-5 Detailed GCR Format

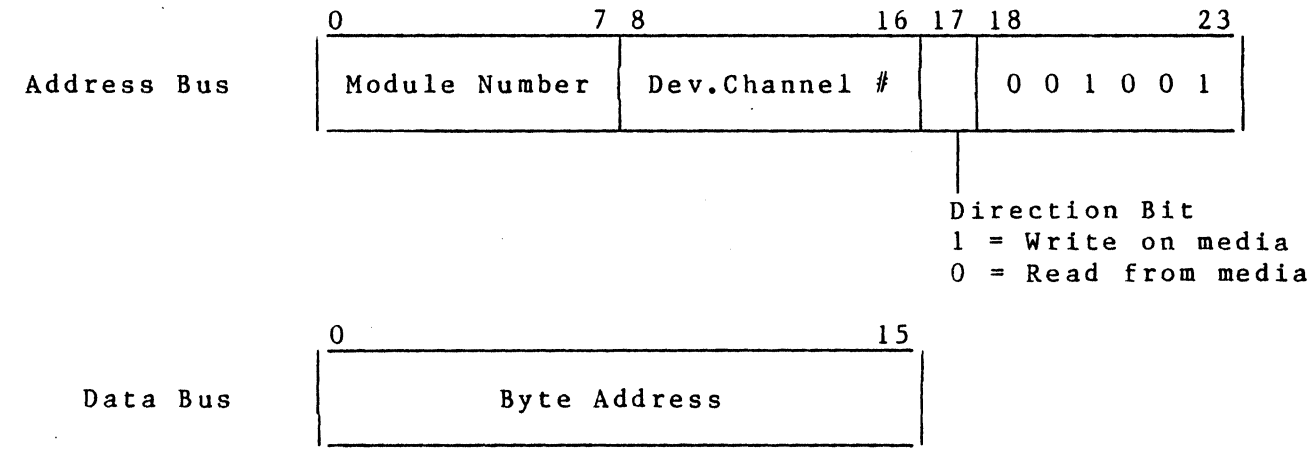
5.2 Instructions

Table 5-3 represents the instruction set which is supported by the MPTC. Allowable formats of the Task Word command are given in subsection 5.2.5.

5.2.1 I/O Load (IOLD)

The I/O Load (IOLD) instruction is transformed by the CPU into the Output Address and Output Range instructions on the Megabus. Each IOLD instruction results in an Output Address instruction followed by an Output Range instruction.

5.2.1.1 Output Address



This instruction loads a 24-bit address into the address register associated with the referenced channel (device). The address refers to the starting (byte) location in main memory where the MPTC commences input or output data transfers. Bits 0 through 7 of the address bus (module number) are the most significant bits of the address. The data bus contains the 16 least significant bits. Data transfers to or from memory are normally on a word basis but byte mode transfers can occur associated with the first and/or last memory cycle of a particular data transfer if the main memory buffer (identified by this instruction) begins or ends on an odd byte boundary.

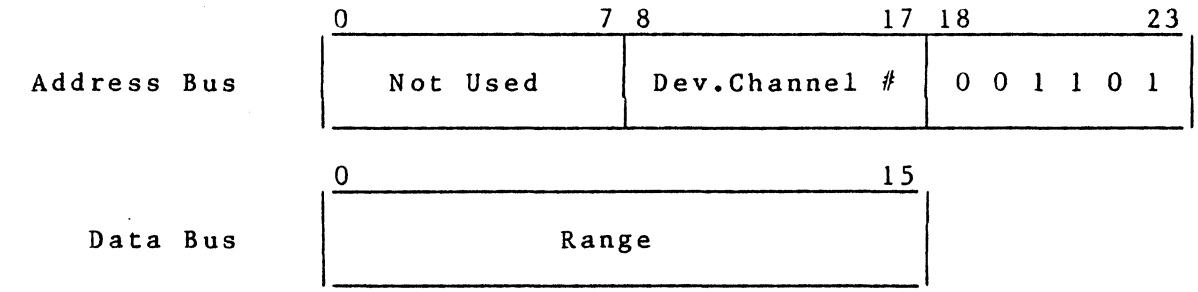
Bit 17 of the address bus (direction bit of the channel number) determines the direction of any subsequent data transfer operation. A logical One specifies an output operation (writing on media) while a logical Zero specifies an input operation (reading from media).

TYPE	FUNCTION CODE	INSTRUCTION	REFERENCE
Output	09	IOLD	5.2.1
		Address (09)	5.2.1.1
		Range (0D)	5.2.1.2
	11	Configuration Word A	5.2.2
	13	Configuration Word B	5.2.3
	03	Interrupt Control	5.2.4
	07	Task Word	5.2.5
	01	Control Word	5.2.6
Input	0C	Range	5.2.7
	08	Memory Byte Address	5.2.8
	0A	Memory Module Address/QLTI	5.2.9
	10	Configuration Word A	5.2.10
	12	Configuration Word B	5.2.11
	02	Interrupt Control	5.2.12
	26	Identification Code	5.2.13
	06	Task Word	5.2.14
	18	Status Word 1	5.2.15
	1A	Status Word 2	5.2.16
	04	Firmware/Hardware Rev.	5.2.17
	20	Fault Pointer	8.3.3
Extended Status	Sense Drive Status		
	1C(& 1D)	DSB00 and DSB01	5.2.5.16.1
	1E(& 1F)	DSB02 and MBZ	
	38 - 3F *	DSB00 thro'DSB40	5.2.5.16.2
	Detail Status Words		
	30	Read Tracks-Word 0	5.2.5.13.1
	32	Read/Write Errors Word 1	5.2.5.13.2
	34	Diagnostic Aids Word 2	5.2.5.13.3
	36	Drive Sense Word 3	5.2.5.13.4
	38	CRC Status (NRZI) Word 4	5.2.5.13.5
	Any Even Code	Read RWS	5.2.18
	Any Odd Code	Write RWS	5.2.18

* CDC drives only.

Table 5-3 Instruction Set

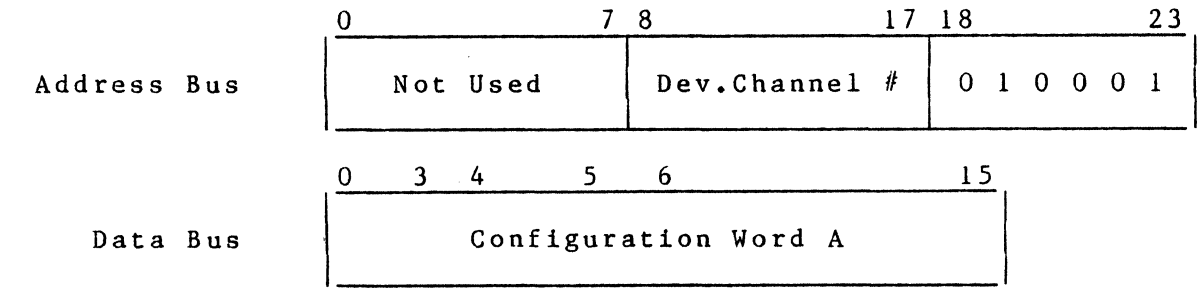
5.2.1.2 Output Range



This instruction loads the range register associated with the referenced channel. The 16-bit quantity loaded (data bus) is the number of bytes to be transferred during the data transfer being set up. The number is a positive 16 bit binary quantity and is decremented by the MPTC after each memory transfer.

A range of zero results in a subsequently issued read or write order setting the operation check bit of Status Word 1 (subsection 5.2.14.12), no data transfer, no tape motion initiated, and a termination of the order. Any address and range register residue is applied to the next command unless reset by another Output Range instruction.

5.2.2 Output Configuration Word A



This instruction loads the Configuration Word A for the device/controller corresponding to the referenced channel. The configuration word bit significance is illustrated in Table 5-4 and defined as follows:

- o Bit 0 - Recording Mode Select: Must be Zero.
- o Bit 1 - 7/9 Track Select: Must Be Zero.
- o Bit 2 - RFU: This bit is reserved for future use.
- o Bit 3 - Parity Select: This bit selects either even or odd parity for the selected controller/device. The F/C interfaces only with 9-track tape drives; therefore, the normal setting of this bit is a Zero selecting odd parity.

BIT(s)	MPTC - (F/C)GCR/PE
0-1-2	0 (Must be Zero)
3	Parity Select 0 = Odd Parity 1 = Even Parity
4	1 = Inhibit ANSI
5	RFU
6	Mode Select 0 = Normal Mode 1 = Diagnostic Mode
7	Buffer control (CDC only) 0 = Buffer Enabled 1 = Buffer Disabled
8	Density Select (Optional) 1 = 6250 GCR 0 = 1600 PE
9 - 15	RFU - Must be Zero

Table 5-4 Configuration Word A
Bit Significance

- Bit 4 - Inhibit ANSI: This mode is used for diagnostic purpose only.

- Bit 5 - RFU: This bit is reserved for future use.

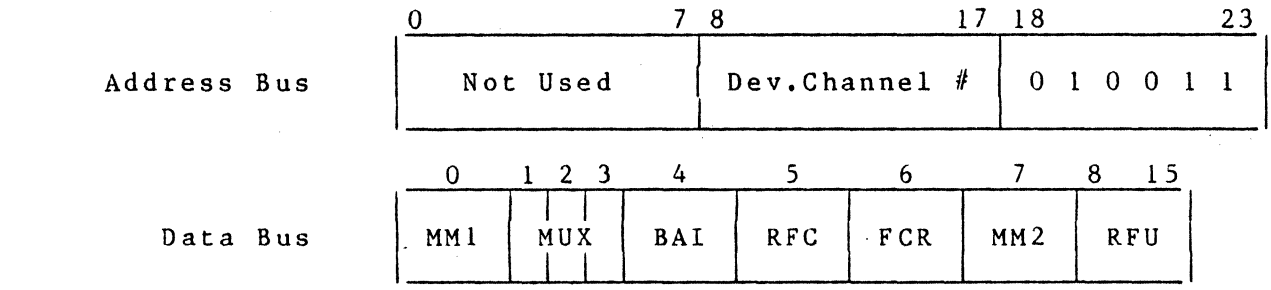
- Bit 6 - Normal/Diagnostic Mode Select: This bit is normally set to a Zero indicating that normal functionality is selected. The One state indicates that the controller selected is in a diagnostic mode. When this bit is set to a One for the F/C, the MPTC issues a Set Diagnostic Mode command to the F/C prior to the execution of the Task Word that follows. This places the F/C in the diagnostic state for the Task Word that follows the Output Configuration Word instruction. Note that the F/C enters the diagnostic state for each Task Word issued where the diagnostic mode select bit (bit 6) of the Configuration Word is set to a One. The status information, available after execution of the Task Word in the diagnostic state, has specific meaning to the T&V software. Formatted tapes are not necessarily ANSI compatible.

- Bit 7 - This bit has no meaning for STC transports. For CDC transports this bit is zero when initialized or powered up which enables the device data buffer; this buffer can also be enabled at BOT by issuing this command with bit 7 = 0. The buffer can be disabled by setting bit 7 to = 1 when the command is executed at BOT.

- Bit 8 - Density Select: This bit can be used to select one of two recording densities for the F/C operations in Diagnostic Mode only (not implemented on Mod 400) (see Table 5-4). Normally, density selection is done by a manual switch on the tape drive.

- Bits 9 through 15 - RFU, MBZ: These bits are reserved for future use and must be Zero.

5.2.3 Configuration Word B

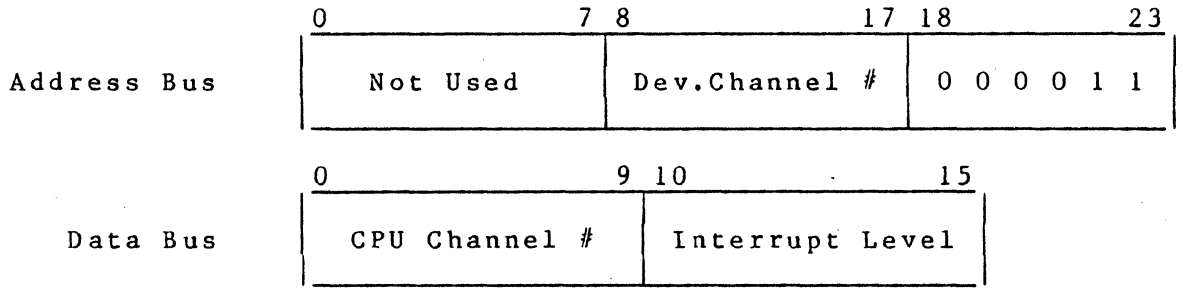


This instruction loads the Configuration Word B for the device/controller corresponding to the referenced channel. The bit significance is defined below. The command is to be used primarily for diagnostic purposes when exercising the

Formatter/Controller and device Test & Diagnostic (T&D) procedure. For further information, refer to the OVP-supplied T&D procedure.

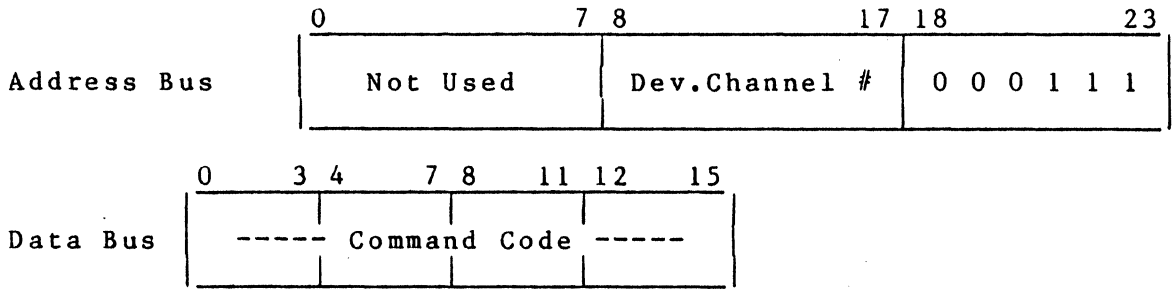
- Bit 0 - MM1 (Maintenance Mode-One): This bit, in conjunction with Configuration Word A bit 6, is used by the controller firmware to set T&D maintenance mode of operation.
- Bits 1, 2, and 3 - Multiplexer control lines: These bits, which are part of the control logic (SLX0, SLX1, and SLX2, see subsection 4.2.3.1.3), enable the error and status bus lines.
- Bit 4 - BAI, Bus Address Inhibit to the F/C.
- Bit 5 - RFC, Reset F/C.
- Bit 6 - FCR, F/C Ready.
- Bit 7 - MM2 (Maintenance Mode-Two). This bit is used to set maintenance mode of operation without Configuration Word A bit 6 being set so that the F/C is not in diagnostic mode. In maintenance mode the MPTC executes a write task by transferring only even bytes with bit 7 of the odd bytes used as the parity bit. Since the F/C is not in diagnostic mode, the data is actually written on tape.
- Bits 8 through 15 - These bits are Reserved for Future Use.

5.2.4 Output Interrupt Control



This instruction loads, for the referenced device, the interrupt level and the channel number of the CPU to which subsequent interrupts should be sent. The level number is a 6-bit quantity positioned on the data bus as illustrated above. Bits 0 through 9 of the data bus contain the channel number of the CPU loading the interrupt level. If an interrupt level of zero is loaded, the subsystem does not generate or save interrupts for any events that occur while the interrupt level is zero. For example, if the attention bit in Status Word 1 is set to One with a stored interrupt level of zero, the subsystem does not generate an interrupt on the bus. The interrupt level is set to zero whenever the subsystem is initialized.

5.2.5 Output Task Word



80	00	Rewind
C0	00	Rewind and Unload
08	NN	Forward Space Block(s)
04	NN	Back Space Block(s)
18	00	Forward Space Tape Mark
14	00	Back Space Tape Mark
09	NN	Read Forward
05	00	Read Backward
28	00	Erase
3A	00	Write Tape Mark
2B	00	Write
00	00	No Operation
00	9N	Store Detail Status
00	9A	Loop Write-to-Read
00	9B	Execute Diagnostic Command
00	9C	Drive Sense Status
00	9D	Device Clear
00	A0	Wraparound MPTC
00	A1	Adapter Wraparound

Where N implies the nibble has specific meaning for the command (refer to command description).

This command outputs a Task Word to the referenced channel. Coding of bits 0 through 15, illustrated above, represents operations that are to be performed by the controller. When this command is accepted, the channel enters the busy state. All configurations, address, and range information must be loaded prior to execution of this command. The direction of data transfer indicated by the low-order bit of the most recent Output Address command (see subsection 5.2.1.1) must agree with the direction of transfer (read or write) specified by the command code of the Output Task Word. If it does not, operation check (Status Word 1, bit 11) is set and a normal termination of the command without data transfer and tape motion results. Commands addressed to a device not in the on-line state result in the setting of an operation check bit (see subsection 5.2.14.12) prior to a normal termination of the order.

5.2.5.1 Rewind (8000)

This order rewinds the tape to the BOT marker. The drive remains in the busy state until the completion of the rewind operation. If the tape on the drive is at BOT when this order is issued, tape motion is not initiated and a normal termination of the order results. Note that the rewinding of a drive via the rewind button on the drive does not put the device in the busy state but activates rewinding (Status Word 2, bit 1) which affects the status of the device ready and attention bits of Status Word 1 (see subsection 5.2.14). When the manually initiated rewind is complete, the rewinding status condition is reset, device ready changes state, and the attention bit is set again.

5.2.5.2 Rewind and Unload (C000)

The rewind and unload order causes the addressed tape unit to rewind to BOT, remove the tape from the tape path, and rewind it completely onto the file reel. If the tape on the drive is at BOT when this order is issued, only the unload sequence is initiated prior to termination of the order. The unload sequence puts the selected tape device into the off-line state and extinguishes the on-line indicator. Operator intervention is required to place the drive back in the on-line state.

5.2.5.3 Forward Space Block(s) (08NN)

This order causes the drive to space forward over the next n blocks. The order terminates when tape is positioned in the n^{th} interblock gap. The number of blocks spaced over is a function of bits 8 through 15 of the Command Code (see subsection 5.2.5). These bits act as a counter with a range of 0 to 255_{10}. Note that a count of zero or one results in the spacing of one block.

5.2.5.4 Back Space Block(s) (04NN)

This order causes the drive to space back over the previous n blocks on tape. The order terminates when the tape is positioned in the n^{th} previous interblock gap. The number of blocks spaced over is a function of bits 8 through 15 of the command code (see subsection 5.2.5). These bits act as a counter with a range of 0 to 255_{10}. Note that a count of zero or one results in the spacing of one block. If this order is issued when the tape is positioned at BOT, tape motion is not initiated and the order is terminated; however, the tape's position beneath the read/write head will not be the same as that following the termination of a rewind operation. In order to place the tape in the proper position beneath the heads following the termination of BOT of a reverse direction command (Back Space Block, Tape Mark), a Read Forward command followed by a Rewind command is necessary. This correction sequence needs to be implemented by software.

5.2.5.5 Forward Space Tape Mark (1800)

This order causes the drive to space forward over one or more blocks until a tape mark is detected. The order terminates when the tape is positioned in the interblock gap following the block containing a tape mark. If EOT is sensed while spacing, tape motion does not stop until a tape mark is detected. This can result in the drive spacing off the end of the reel if there is no tape mark after the EOT marker.

5.2.5.6 Back Space Tape Mark (1400)

This order causes the drive to space back over one or more blocks until a tape mark is detected. The order terminates when the tape is positioned in the interblock gap preceding the block containing the tape mark or when the tape is positioned at BOT. If this order is issued when the tape is positioned at BOT, tape motion is not initiated and a normal termination of the order follows; however, the tape's position beneath the read/write head will not be the same as that following the termination of a rewind operation. In order to place the tape in the proper position beneath the heads following the termination of BOT of a reverse direction command (Back Space Block, Back Space Tape Mark), a Read Forward command followed by a Rewind command is necessary. This correction sequence needs to be implemented by software.

5.2.5.7 Read Forward (09NN)

Unbuffered Mode.

This order causes the drive to read forward over the next block on tape (Configuration Word bit 7 set to one, CDC tape transport only; reference section 5.2.2). The order terminates when the tape is positioned in the next interblock gap. The format of the data transferred from tape to memory is a function of the stored configuration word (see subsection 3.1.3). In addition to reading data, integrity checks are made (see subsections 5.2.14 and 5.2.15).

The GCR-MTS also provides for the automatic retry of records when read errors occur. The retry capability is enabled when bits 8 through 15 of the command code (see subsection 5.2.5) are non-Zero. This field (bits 8 through 15) acts as a retry counter with a range of 0 to 255_{10}. Upon successful retry, Corrected Media Error (Status Word 1, bit 4) and Retry Attempted (Status Word 2, bit 9) are set in the terminating status. Retryable Media Error (Status Word 1, bit 2) is set if the retry mechanism was unsuccessful or a read error occurred and the retry counter was Zero.

Buffered Mode.

This command causes the F/C to initiate a read operation on the tape transport and the data is transferred to the device

data buffer. Data transfer to the GCRA is not started until the complete record is in the buffer without errors. If an error is detected, the F/C issues a back space command to the tape transport, rereads the data block and updates its read error counter. If there are no errors, or an error recovery procedure was successful, BUSY is asserted to the GCRA and a normal data transfer takes place (reference section 4.2.3.4.2). Read data recovery is performed by the F/C according to the following:

- If a data check is on the first block on the tape, rewind and reread that block up to ten times.
- If a data check is on a block other than first, space reverse and reread that block up to ten times.
- If the data check persists repeat step 3 at the high threshold.
- If the data check persists repeat step 3 at an alternate speed.

NOTE
Maximum number of retries is 40.

Anticipating that other Read Commands will be issued and to maintain streaming, the F/C initiates another Read Command to the tape transport and starts transferring data into the data buffer. This continues until the buffer is full or until a command other than read is issued by the GCRA. If a file mark is detected the status is stored and another Read Command is initiated; if two successive file marks are detected prereading is terminated. On receipt of other than "Read Command" command and there are more block records in the data buffer than were requested the F/C causes the tape to be backspaced to the end of the last record to be successfully transferred to the GCRA; the pending command is then executed.

5.2.5.8 Read Backwards (0500)

This order is not available in the GCR-MTS. The issuance of this order to the subsystem results in no data transfer, no tape motion initiated, the activation of Status Word 1, bit 11, Operation Check (see subsection 5.2.14.12) and Status Word 2, bit 11, Functionality Not Available (see subsection 5.2.15.11) followed by a normal termination.

5.2.5.9 Erase (2800)

This order causes the drive to erase tape in the forward direction producing a 3 inch gap on the tape. The device channel remains busy for the duration of the erase order and terminates normally.

This command can be used to "flush" the data buffer on a CDC transport to ascertain that all the data in the buffer is written on the tape before initiating another write command or terminating present transaction; the controller remains busy until the Erase command is executed after all the data from the buffer has been transferred. Using this command for this purpose reduces both the tape capacity and the average transfer rate; some applications can perform better in the unbuffered mode.

5.2.5.10 Write Tape Mark (3A00)

This order causes the addressed tape unit to move tape in the forward direction, execute an Erase, and write a tape mark identifier appropriate to the recording mode in effect at the time the command is issued. No data is transferred during the write portion of the command. The channel remains busy for the duration of the command. During the entire write operation, the read detection circuitry verifies that a complete erasure has occurred and that the tape mark written is correct. The order terminates when the tape is positioned in the gap beyond the tape mark block.

CDC drive only.

Buffered Mode.

The task is stacked and BUSY is deactivated allowing other tasks to be issued before the Tape Mark has been written on the tape medium. If two consecutive Tape Mark commands are issued the second one causes BUSY to stay activated until that second Tape Mark is written on the tape medium.

Unbuffered Mode.

BUSY stays activated until the Tape Mark is written on the tape medium.

5.2.5.11 Write (2B00)

Unbuffered Mode.

This order causes the drive to write, in the forward direction, a data block of the format specified by the configuration word (In particular, Configuration Word bit 7 set to one, CDC tape transport only; reference section 5.2.2) most recently issued to this addressed channel. Nondata characters used for synchronization and error checking are recorded on tape; the generation of all such characters is an F/C function. The block that is written on tape is checked for validity as it passes under the read head.

The order terminates when the tape is positioned in the gap beyond the data block written. An attempt to write a data block

to a drive in write-protect (see subsection 5.2.15.3) results in no data transfer, no tape motion initiated, and the activation of the Operation Check bit of Status Word 1 (see subsection 5.2.14.12).

Buffered Mode.

The first Write Command initiates a data transfer operation between the GCRA and the F/C data buffer. BUSY is activated and TREQ is generated at the selected rate (defined by the channel rate jumpers) as data is transferred to the buffer. On receipt of the Stop from the GCRA the F/C deactivates BUSY and is ready for another command. Dependent on the speed, density and ramp time, the F/C initiates the tape motion while data transfers to the buffer are still in progress for the next block. When the tape is up to speed the F/C starts transferring data from the buffer to the tape.

As long as the GCRA continues to send Write Commands and the transfer rate of data is higher than that to tape, streaming is maintained and the data buffer is eventually filled. Buffer is not considered full if there is enough space for a block of data of the size defined by the maximum-record-size jumpers. If the GCRA attempts to send a larger block than this, when there is only one block space available in the buffer, the F/C stops transferring data but continue sending TREQ to the GCRA until the Stop is received; Data Check Error (Status Word 2, bit 15) is set to indicate that the transfer was not successful. When approaching the end of tape the F/C senses this condition and degrades the data buffer operation so that when the EOT is detected there is only one block of data in the buffer. If a command other than a Write Command is issued, the F/C continues transfering from the data buffer and then executes the new command when the buffer is empty.

If a data error is detected while writing the F/C (error counter is incremented and is available to the GCRA as a sense byte) invokes the following error recovery procedure:

- If the data check is on the first block, rewind, erase and rewrite the block up to five times.
    - o If the data check is on erase, replace media.
    - o If there is no data check on erase, rewrite. Continue to the next step if there is a date check on rewrite.
- If the data check is on a block of data other than first block, space reverse over the error block, erase and rewrite up to five times.
- If the data check persists, repeat the above step up to ten times or up to the maximum IBG permitted by ANSI standard.

In the event that an error occurs that cannot be corrected Data Check Error is set (Status Word 2, bit 15) and the number of records still in the buffer is available in the sense status.

5.2.5.12 No Operation (0000)

This order results in no data transfer, no tape motion initiated, the normal reset of status word bits upon reception of an Output Task command, and a normal termination of the order. However, this order is NAK'ed if the channel is busy. It should be noted that any status information within the F/C is unaltered by this order.

5.2.5.13 Store Detail Status (009N)

This order provides the capability of transferring to software up to eight words of detail status. The status information is stored in the starting memory location specified by the IOLD (see subsection 5.2.1). Bits 13, 14, and 15 of the command code determine which of the eight status words are sent first; for example, if bits 13, 14, 15 are set to 010, the transfer begins with Status Word 2. If the Range (see subsection 5.2.1.2) specifies more than one word (two bytes), data transfer continues until the range is exhausted or eight status words are transferred from the F/C.

Eight detail status words are associated with the F/C. To retrieve the first status word from the controller, bits 13, 14, and 15 of the command code must be Zeros.

Normal tape operations do not require the reading of detail status since sufficient information is available in Status Words 1 and 2 (see subsections 5.2.14 and 5.2.15). Detail status information is provided primarily for diagnostic visibility.

The format for the detail status words, listed below, is presented in Table 5-6; a brief description of each detail status bit follows.

90 - F/C Status Word 0 - Dead Tracks

91 - F/C Status Word 1 - Read/Write Errors

92 - F/C Status Word 2 - Diagnostic Aids

93 - F/C Status Word 3 - Drive Sense Status

94 - F/C Status Word 4 - NRZI CRC Status

95 - F/C Status Word 5 - RFU
96 - F/C Status Word 6 - RFU
97 - F/C Status Word 7 - RFU

For further information, refer to subsection 4.2.3.1.3 and Table 4-2.

CAUTION

Store Detail Status retrieves the state of a device after the last task. Any state changes during the status command are not indicated or retained. New status conditions are again available after initialize, another device state change or another functional task command when the Store Detail Status command is no longer active. Alternately, Detail Status can be read by input function codes listed on the next page.

Request Cycle

	0 — 7	8 — 17	18 — 23
Address Bus	Not Used	Dev.Channel #	1 1 X X X 0 (Table 5-5)

	0 — 9	10 — 15
Data Bus	CPU Channel #	----------

Response Cycle

	0 — 7	8 — 17	18 — 23
Address Bus	Not Used	CPU Channel #	----------

	0 — 15
Data Bus	Detail Status (Table 5-6)

FUNCTION CODE 1 1 X X X 0	F/C STATUS WORD
1 1 0 0 0 0	Dead Tracks - Word 0
1 1 0 0 1 0	Read/Write Errors - Word 1
1 1 0 1 0 0	Diagnostic Aids - Word 2
1 1 0 1 1 0	Drive Sense - Word 3
1 1 1 0 0 0	CRC Status (NRZI only)-Word 4

Table 5-5 Function Codes

This instruction causes the current contents of the referenced channel's Detail Status to be transferred to the requesting channel.

During the response cycle (second-half read), the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the instruction cycle. After completion of a functional task, the contents of the Detail Status reflect the state of that device with respect to that particular task.

NOTE

If the Range is zero for the Store Detail Status task, the MPTC enters an undefined state and must be reinitialized.

L6 BIT	WORD 0	WORD 1	WORD 2	WORD 3	WORD 4
0	DT7	WTM CHK	DA7	EOT STAT	CRC-F7
1	DT6	UCE	DA6	BOT STAT	CRC-F6
2	DT5	PART REC *	DA5	WRT INHB	CRC-F5
3	DT4	MTE	DA4	FILE PROT	CRC-F4
4	DT3	0	DA3	BKWD STAT	CRC-F3
5	DT2	END DATA CHK	DA2	HI DEN	CRC-F2
6	DT1	VEL ERR *	DA1	RDY STAT	CRC-F1
7	DT0	DIAG MODE LTCH	DA0	ON LINE STAT	CRC-F0
8	DTP	CRC ERR	TACH *	WRT STAT	CRC-FP
9	RFU	RFU	RFU	RFU	RFU
10	RFU	RFU	RFU	RFU	RFU
11	RFU	RFU	RFU	RFU	RFU
12	RFU	RFU	RFU	RFU	RFU
13	RFU	RFU	RFU	RFU	RFU
14	RFU	RFU	RFU	RFU	RFU
15	RFU	RFU	RFU	RFU	RFU

* STC drives only; MBZ for CDC drives.

Table 5-6 Formatter/Controller Detail Status Words

5.2.5.13.1 F/C Status Word 0 - Dead Tracks

Bits DT0 through DTP are asserted on detection of a dead track during a read or write operation. If diagnostic mode is set (9B), this byte represents phase errors for each track on an immediately following read or write command.

5.2.5.13.2 F/C Status Word 1 - Read/Write Errors

WTM CHK - Write Tape Mark Check:

The F/C was unable to write a correct tape mark.

UCE - Uncorrectable Error:

This error may occur during PE or GCR read/write commands. DATACHK is also asserted. UCE is also asserted during write operation to indicate excess slew.

* PART REC - Partial Record:

An IBG (interblock gap) is detected before end-of-data is read. DATACHK is also set.

MTE - Multiple Track Error:

Two or more tracks detect an error. It may occur during PE or GCR read/write commands. DATACHK may also be set.

END DATACHK - End Data Check:

This bit indicates that end-of-data characters were not detected or that the preamble/postamble did not meet format requirements. Occurs during PE or GCR read/write commands. DATACHK is also set.

* VEL ERR - Velocity Error:

When set, indicates that the MTU speed was outside limits. This may occur for all modes during write commands. DATACHK is also set.

DIAG MODE LTCH - Diagnostic Mode Latch:

Diagnostic mode is set in the F/C.

CRC ERR - Cyclic Redundancy Character Error:

This bit can set during read or write commands for all modes of operation. When set, it indicates the loss of data integrity. DATACHK is also asserted.

5.2.5.13.3 F/C Status Word 2 - Diagnostic Aids

* TACH - Digital Tachometer:

This bit pertains to both tape speed and distance used in diagnostic procedures.

---

* STC drives only; MBZ for CDC drives.

REJECT CODES:

These codes refer to specific conditions of a drive. DA7 is the MSB and DA0 is the LSB of the code. An * indicates that the line OP INC is also true. These codes are defined in Table 5-7.

REJECT CODE	DESCRIPTION
01	The addressed MTU is not in ready status.
02*#	The F/C has detected one of its internal microprogram words having wrong parity.
03*#	The TRAK responses to TREQs were not received within 75 ms on a write type command.
04*#	The F/C has detected an unimplemented word in its internal microprogram.
05	The addressed MTU is in file protect status when a write type command is attempted.
06*	The addressed MTU did not go to erase status only.
07$	Command cannot be executed as given.
08*#	The addressed MTU did not go to read status.
08$	The MTU is not responding to the formatter.
09*	The MTS does not have NRZI capability and was unable to read an NRZI tape. The MTS does not have NRZI capability and was unable to read a PE or GCR ID burst during either a read operation or during a read check after writing the ID burst.
0A*#	The addressed MTU did not drop write inhibit status.
0A$	Urecoverable write error.
0B#	The addressed MTU is not in on-line status.

* = OP INC is also set.
$ = Available on CDC, Keystone, tape transports only
# = Not available on CDC, Keystone, tape transports

Table 5-7 Formatter/Controller Reject Codes
(Sheet 1 of 3)

REJECT CODE	DESCRIPTION
0B$	Unrecoverable read error.
0C*#	The addressed MTU did not go to write status after a write type command was initiated.
0C$	Unrecoverable tape mark error.
0D*#	During a backward motion after writing the ID burst, BOT was not reached in the distance expected.
0E*#	The addressed MTU did not go to backward status.
0F*	Noise (possibly data) was detected during an erase gap command or during a write command following a read type command.
11*	The addressed MTU reset ready status.
12*#	When the PE or GCR ID burst just written was rechecked on a read, the ID burst was on the wrong track
13	A backward type command (except a rewind or a rewind unload command) was given but tape was already positioned at BOT.
14*	The ARA burst portion of the GCR ID burst just written did not have all nine tracks active.
15*	An IBG longer than 25 feet in PE or longer than 15 feet in GCR mode was detected on a read or space type command.
17*#	The addressed MTU failed to reset ready status during a rewind operation.

* = OP INC is also set.
$ = Available on CDC, Keystone, tape transports only
# = Not available on CDC, Keystone, tape transports

Table 5-7 Formatter/Controller Reject Codes
(Sheet 2 of 3)

REJECT CODE	DESCRIPTION
18$	The MTU is not in the recording density selected.
1A*	The addressed MTU failed to initiate tape motion.
1B*#	During the read-back check of a write operation, data was detected in the IBG area.
1C*#	There was no IBG detected following the ARA ID burst.
1D*#	Drive attempted to backspace over a bad record just written but was unable to detect the record.
1E*	The ARA ID burst was unreadable during a GCR read or write command.
1F*#	During the read-back check of a write or write tape mark command, no data was detected.
1F*$	During the read-back check of a write no data was detected.

* = OP INC is also set.
$ = Available on CDC, Keystone, tape transports only
# = Not available on CDC, Keystone, tape transports

Table 5-7 Formatter/Controller Reject Codes
(Sheet 3 of 3)

5.2.5.13.4 F/C Status Word 3 - Drive Sense Byte

EOT STAT - End-of-Tape Status:

This line is asserted by the F/C when the loaded tape is positioned on or past the EOT marker indicating that the tape is positioned in the end of the recording area.

BOT STAT - Beginning-of-Tape Status:

This line is asserted by the F/C when the loaded tape is positioned at BOT.

WRT INH - Write Inhibit:

This line is asserted when the IBG is being created during a write operation.

FILE PROT - File Protect:

This line is asserted by the F/C when the loaded tape reel does not contain a write enable ring.

* BKWD STAT - Backward Status:

This line is asserted when the F/C is in backward status.

HI DEN - High Density:

This line is asserted when the F/C is set to GCR mode (1950 series MTUs only).

RDY STAT - Ready Status:

This line, when asserted, signifies the F/C has tape loaded and is not rewinding.

ON LINE STAT - On-Line Status:

This line, when asserted, signifies that the F/C has been placed on-line by depression of the ON LINE push button on the MTU control panel.

WRT STAT - Write Status:

This line is asserted by the F/C when it is in write mode and erase status is asserted concurrently. When write status is asserted, both write and erase heads are active.

5.2.5.13.5 F/C Status Word 4 - CRC Status

This byte contains the contents of the CRC-F generator And is used in certain STC diagnostic tests.

5.2.5.14 Loop Write To Read (009A)

When issued to an F/C, the order is translated into the Loop Write-to-Read command which provides a means of checking the read/write data paths, inside an F/C, for proper operation. A normal Write command is simulated and the F/C loops the information presented to the write bus back to the read bus and through most of the read data path. There is no tape motion and the MTU is not involved. The operation is performed in the recording mode selected and the data rate of the selected MTU.

5.2.5.15 Execute Diagnostic Command (009B)

For a description of this command refer to subsection 5.2.2.

---

* STC drives only; MBZ for CDC drives.

5.2.5.16 Drive Sense Status (009C)

Upon power up or initialization of the MPTC, the Sense Drive Status bytes (DSB00, DSB01 and DSB02) are stored in registers 1C/1D and 1E/1F (see below); these registers can be read by performing I/O inputs 1C and 1E respectively. To obtain correct Drive Sense Status at this time requires that the tape drive must be in the READY status. The DSB00 byte is also stored in the Detail Status Word 3 during MPTC power up and as part of the automatic status retrieval after each functional task.

For an alternative method for obtaining Drive Sense Status, at any time, the following sequence must be used (The assumption is made that the tape device was Ready during initialization and is ready now.):

5.2.5.16.1 STC drives only:

- Read Detail Status Word 3 for DSB00
- Input Function code #36

o Output Drive Sense Status Task (009C) to the device.

- Read Detail Status Word 3 for DSB01
- Input Function Code #36
- Output the NOP Task (0000)

o Output Drive Sense Status Task (009C) to the device

- Read Detail Status Word 3 for DSB02
- Input Function Code #36
- Output the NOP Task (0000)

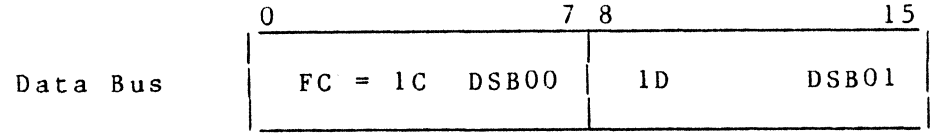
o Follow this procedure to read the Drive Sense bytes and terminate the sequence by the:

o Output the Device Clear Task (009D)

This returns the firmware pointer to DSB00 and clears the F/C busy. If the above sequence is not adhered to, the MPTC and F/C enter an undefined state which can be cleared by Master Clear only.

Reference Table 5-8 for details of all available Drive Sense Byte information on the state of the F/C and the tape transport. STC F/C provides only the first three bytes, i.e. DSB00 through DSB02. CDC F/C provides up to 40 bytes of Detailed Status, reference section 5.2.5.16.2.

Status Word 3A



Status Word 3B

	0 7	8 15
Data Bus	FC = 1E DSB02	1F (MBZ)

DSB01	D1	D0	MTU Mode	M2	M1	M0	MTU Speed PE/GCR
	0	0	RFU	0	0	0	50 ips
	0	1	RFU	0	1	0	75 ips
	1	0	PE	1	0	0	125 ips
	1	1	GCR	All other states are RFU.			

DSB02	S1	S0	MTU Switch Position
	0	0	Software Select
	0	1	RFU
	1	0	PE
	1	1	GCR

5.2.5.16.2 CDC Drive Detailed Status.

- Output Drive Sense Status Task Command (009C) to the drive then:
  - Read Detail Status Word 3 for DSB00 & DSB01
    - Input Function Code #36
  - Read Detail Status Word 3 for DSB02 & DSB03
    - Input Function Code #38
  - Read Detail Status Word 3 for DSB04 & DSB05
    - Input Function Code #3A
  - Read Detail Status Word 3 for DSB06 & DSB07
    - Input Function Code #3C
  - Read Detail Status Word 3 for DSB08 & DSB09
    - Input Function Code #3E

NOTE

Input Function Code #3X inputs two bytes of Detail Status, i.e. #3X and 3(X+1).

- o Output second Drive Sense Status Task Command (009C) to the drive to continue reading sequential Sense Status bytes, then:

  - o Read Detail Status Word 3 for DSB10 & DSB11

    - Input Function Code #36

  ---------- etc. ----------

  - o Read Detail Status Word 3 for DSB18 & DSB19

    - Input Function Code #3E

- o Device Clear Task (009D) command terminates the sequential Sense Status read procedure and resets the pointer to DSB00.

For additional Drive Sense Status bytes, up to a maximum of 40, repeat the sequence above: e.g. after the third output Drive Sense Status Task command is issued, DSB20 and DSB21 bytes are present in the Scratch Pad Memory location #36 and so on in groups of ten butes. To terminate the sequence at any status byte, output the Device Clear Task (009D) command.

	Drive Sense bits								
Drive Sense bytes	0	1	2	3	4	5	6	7	P
DSB00	EOTS	BOTS	WNHB	PROS	BWDS	HDNS	RDYS	ONLS	WRTS
DSB01	1	1	D1	D0	0	M2	M1	M0	
DSB02	0	0	S1	S0	0	0	0	0	
DSB03	Interface board micro code revision level (MSB)								
DSB04	Interface board micro code revision level (LSB)								
DSB05	Machine Fault code								
DSB06	Machine Sub-Fault code								
DSB07	0	0	0	0	0	0	0	0	
DSB08	Buffer enabled	Auto ERP enabled	Maximum record size selected			Data transfer rate selected			
DSB09	AVC enabled	Remote Density Select	---	---	---	Start delay time			

Table 5-8 Drive Sense Bytes (Sheet 1 of 4)

	Drive Sense bits							
Drive Sense bytes	0	1	2	3	4	5	6	7
DSB10	FRDPER	IDWPER	MEMLPE	MEMUPE	RDOVER	WTLATE	DCHATO	DCHBTO
DSB11	OVSIZE	---	---	---	---	---	---	---
DSB12	Write retry counter							
DSB13	Read retry counter							
DSB14	Number of records remaining in the buffer							
DSB15	Command reject	Intervention required	Drive type	Equipment check	Data check	0	Unit check	Unit exception
DSB16	Reverse	Write	Edit	Write File Mark	Erase	High speed selected	Threshold select	Long gap
DSB17	Ready	On-line	Rewind	File Protect	Early EOT	High speed	BOT	EOT
DSB18	Interface command reject	Write parity error	Read parity error	Read FIFO overflow/ underflow	Remote Density Select	Interface unit check	Formatter response check	---
DSB19	Illegal interface command	Device command check	Density conflict	File Protect	Reset key	---	Device not ready	Device off-line

Table 5-8 Drive Sense Bytes (Sheet 2 of 4)

	Drive Sense bits							
Drive Sense bytes	0	1	2	3	4	5	6	7
DSB20	Interface parity error	Interface response check	Read hardware check	Write hardware check	Device response check	Device hardware check	Velocity check	Device interrupt
DSB21	AGC fault	---	Read data check	ID fault	---	Error Recovery Code		
DSB22	Formatter Command Code							
DSB23	GCR mode	High speed mode	Adaptive velocity mode	File Mark detected	Local diagnostic mode	Start/ Stop mode	Variable long gap mode	Variable short gap mode
DSB24	Diagnostic fault code							
DSB25	Diagnostic fault sub-code							
DSB26	Write error symptom code							
DSB27	Write transfer check	Residual byte cnt. check	Write CRC parity error	45 parity error	---	Write AUX CRC parity error	---	---
DSB28	Residual check	Read CRC check	Read AUX CRC check	Resync check	ECC 3 check	Uncorrectable data	No track pointer	Excessive pointers
DSB29	Noise check	Postamble error	Skew error	Read timeout	Write tape mark check	ID check	ARA burst check	ARA ID check

Table 5-8 Drive Sense Bytes (Sheet 3 of 4)

	Drive Sense bits							
Drive Sense bytes	0	1	2	3	4	5	6	7
DSB30	EC hardware check	Read buffer in parity er	Read transfer check	Read data parity error	End mark check	Dual track correct	Single track correct	TIE 4 (P)
DSB31	TIE 7	TIE 6	TIE 5	TIE 3	TIE 9	TIE 1	TIE 8	TIE 2
DSB32	Read error symptom code							
DSB33	Reverse	Write	DSE	GCR	LGAP	S/S mode	---	---
DSB34	Remote diagnostic inhbt	Remote diagnostic	LWR interface	LWR PE	LWR GCR	---	Local Density Selected	GCR Density Selected
DSB35	Command reject	Device fault	Diagnostic request	Local density change	AGC check	Reset key	Reverse in BOT	Marginal condition
DSB36	Drive command code or, if AGC check is set in byte 20, failing bits during AGC							
DSB37	Marginal condition code							
DSB38	Fault/test completion code							
DSB39	Sub-fault/sub-test completion code							

DSB40 - DSB55 Reserved

Table 5-8 Drive Sense Bytes (Sheet 4 of 4)

5.2.5.17 Device Clear (009D)

This order is used by the F/C to reset a selected transport and associated error indicators to initial conditions. Tape motion (if any) is halted. The formatter remains busy until the reset is completed. This order results in no data transfer, no tape motion initiated, the normal reset of status word bits upon reception of an Output Task command, and a normal termination of the order.

5.2.5.18 Wraparound MPTC (00A0)

The wraparound level is at the MPTC level. Functionality is as described in the following paragraphs. The direction of data transfer (read or write) is determined by the low order bit of the channel number of the most recent Output Address command.

During a Wraparound Write command, the channel reads one to eight words from memory (at the address specified in the subsystem's memory address register) and transfer them to the MPTC FIFO buffer.

When a Wraparound Read command is received (immediately following a Wraparound Write), the bytes previously loaded into the specified FIFO buffer by the previous Wraparound Write command are returned to main memory at the address specified in the subsystem's memory address register. The bytes returned during this operation are the same as the bytes supplied by software in the preceding Wraparound Write command. The range specified for the Wraparound Write must be the same as the range for the Wraparound Read or the results are unpredictable.

A range of one to eight words must be specified for these commands. If a range of zero is selected, the command is immediately terminated (without being executed and with no status indications). If a range greater than eight words is selected, the results are unpredictable. In any case, the Wraparound Write and its associated Wraparound Read must start and end from the same memory boundary (byte or word).

A Task instruction issued to any other channel during a wraparound sequence is ignored.

5.2.5.19 Wraparound GCRA (00A1)

The wraparound level is at the GCRA level. Functionality is as described in the following paragraphs. The direction of data transfer (read or write) is determined by the low order bit of the channel number of the most recent Output Address command.

During a Wraparound Write command, the channel reads 16 words from memory (at the address specified in the subsystem's memory address register) and transfer them to the GCRA FIFO buffer.

When a Wraparound Read command is received (immediately following a Wraparound Write), the bytes previously loaded into the specified FIFO buffer by the previous Wraparound Write command are returned to main memory at the address specified in the subsystem's memory address register. The bytes returned during this operation are the same as the bytes supplied by software in the preceding Wraparound Write command. The range specified for the Wraparound Write must be the same as the range for the Wraparound Read or the results are unpredictable.

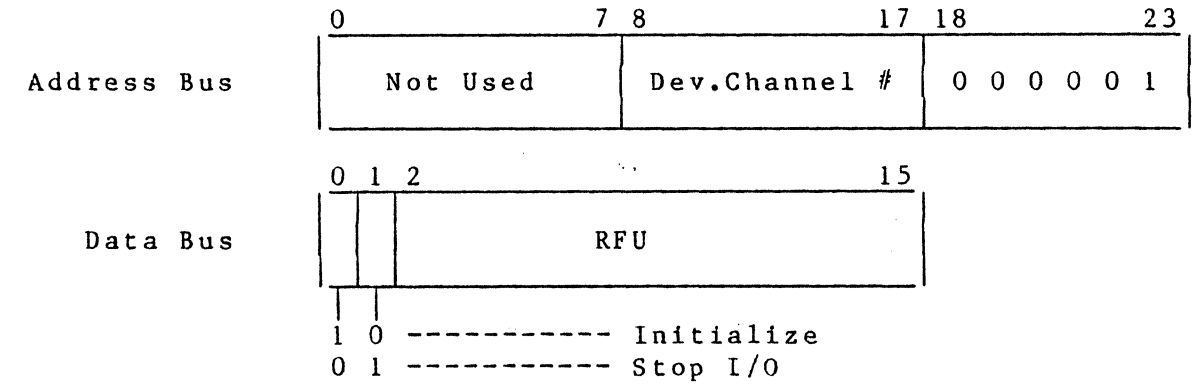
A range of 16 words must be specified for these commands. If a range of zero is selected, the command is immediately terminated (without being executed and with no status indications). If a range other than 16 words is selected, the results are unpredictable. In any case, the Wraparound Write and its associated Wraparound Read must start and end from the same memory boundary (byte or word).

A Task instruction issued to any other channel during a wraparound sequence is ignored.

5.2.5.20 Unspecified Operations

All Output Task commands issued to the MPTC-GCRA, other than those specified above, will result in unspecified operations.

5.2.6 Output Control Word



This instruction loads a control word into the referenced channel. This command is unconditionally accepted by the channel regardless of its busy status except as noted in subsection 3.1.2.

5.2.6.1 Initialize

This command causes the MPTC to reset to the same state that it enters after power up. When an Initialize command is received by the MPTC, all of its channels are initialized (regardless of which channel the command was received over).

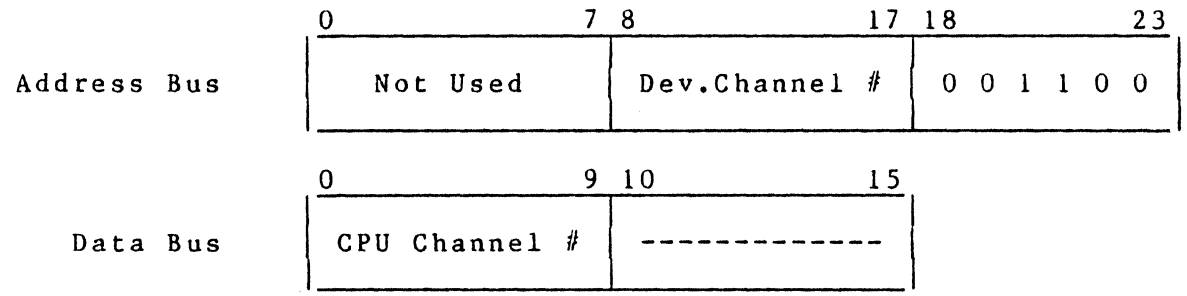
Operations in progress in the MPTC at the time of the initialization are abruptly terminated and all software addressable registers are initialized with the exception of the code conversion tables. These tables require a power on initialize to be affected. No information about the terminated operations is retained and no interrupts for the operations are generated. The interrupt level for all channels is set to zero (interrupts blocked).

5.2.6.2 Stop I/O

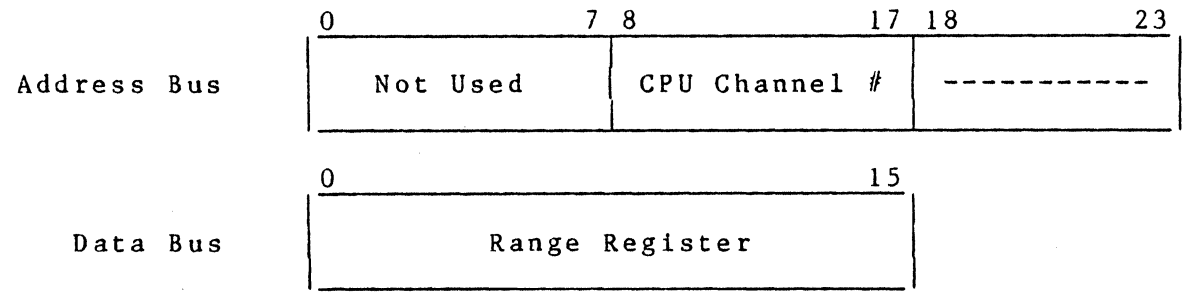
This command causes any operation currently active on the specified channel to be abruptly terminated. If a data transfer operation is in progress, it is not completed nor is any error checking done. An interrupt is generated for the operation terminated by this command as if the operation had come to a normal ending point. Status, address, and range information, present in the MPTC when this command is received, are retained.

5.2.7 Input Range

Request Cycle



Response Cycle



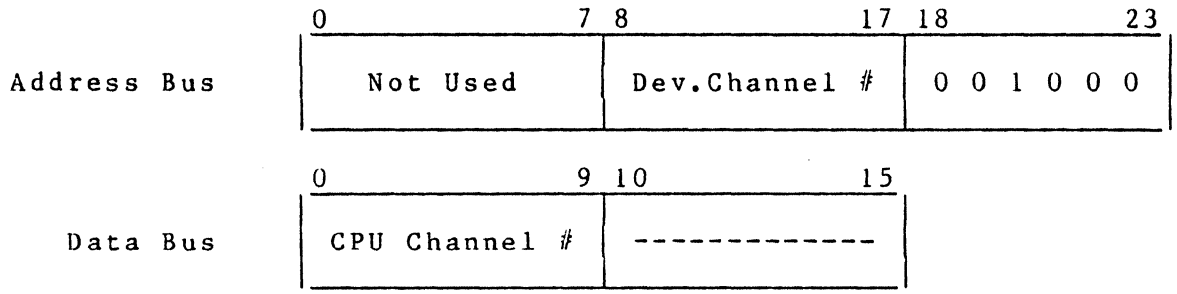
This instruction causes the current contents of the referenced channel's range register to be transferred to the requesting channel.

During the response cycle (second half read), the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the instruction cycle. After the completion of a read operation, the contents of the range register reflects the status of that transfer with respect to the physical block read.

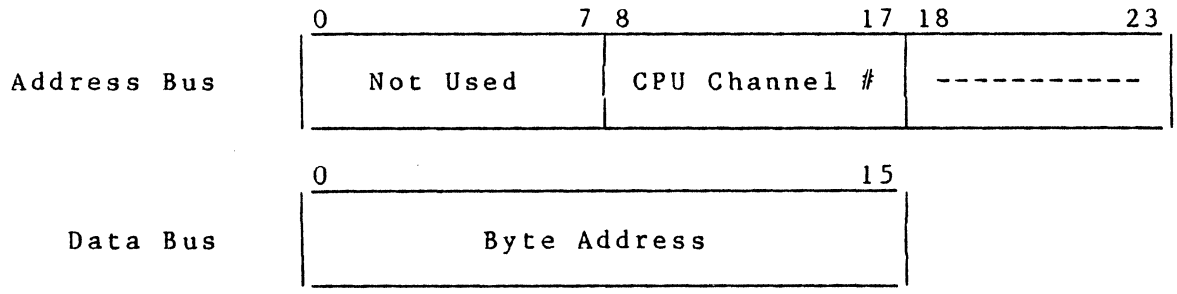
- If the contents is a positive value greater than zero and bit 8 of Status Word 1, Unequal Length Check (see subsection 5.2.14.9) is set to a logical One, the length of the physical block is less than the range.
- If the contents is zero and bit 8 of Status Word 1 is equal to One, the length of the physical block is greater than the original range.
- If the contents is zero and bit 8 of Status Word 1 is equal to Zero, the length of the physical block is equal to the original range.

5.2.8 Input Memory Byte Address

Request Cycle



Response Cycle

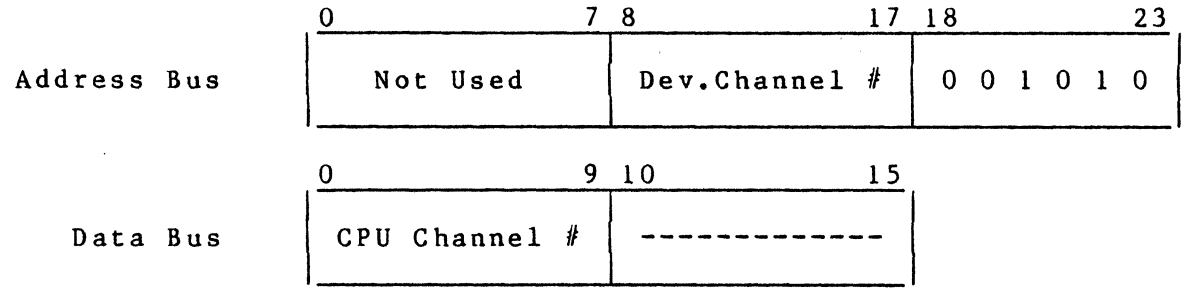


This instruction causes the current contents of the referenced channel's memory byte address to be transferred to the requesting channel.

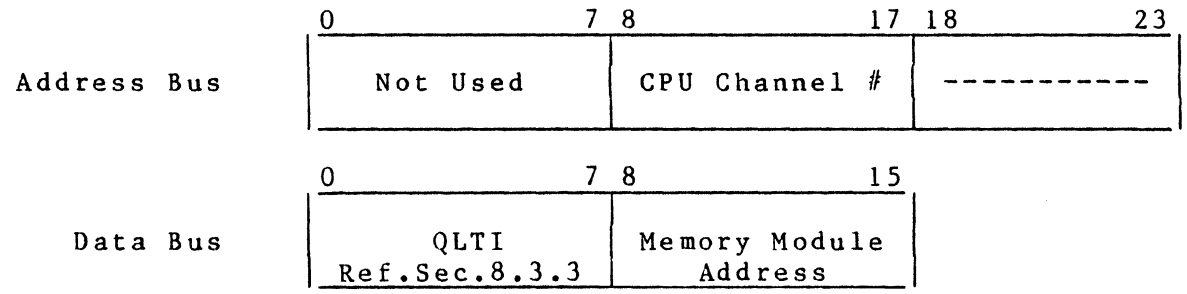
During the response cycle (second half read), the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the request cycle. The data bus contains the low order 16 bits of the memory byte address currently stored for the specified channel in the MPTC. Note that if a Write command ended at a byte boundary (high order 8 bits of word), the memory address reflects the next word (not the low order 8 bits of the previous word).

5.2.9 Input Module Address/QLTI Results

Request Cycle



Response Cycle

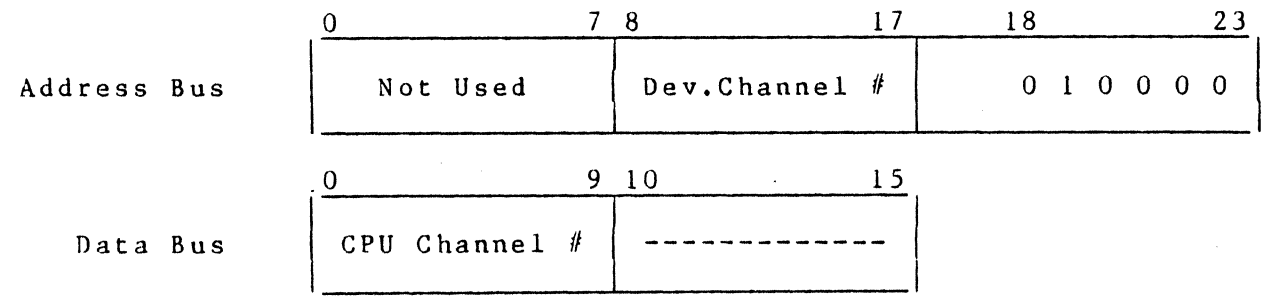


This instruction causes the current contents of the referenced channel's memory module address and QLTI register to be transferred to the requesting channel.

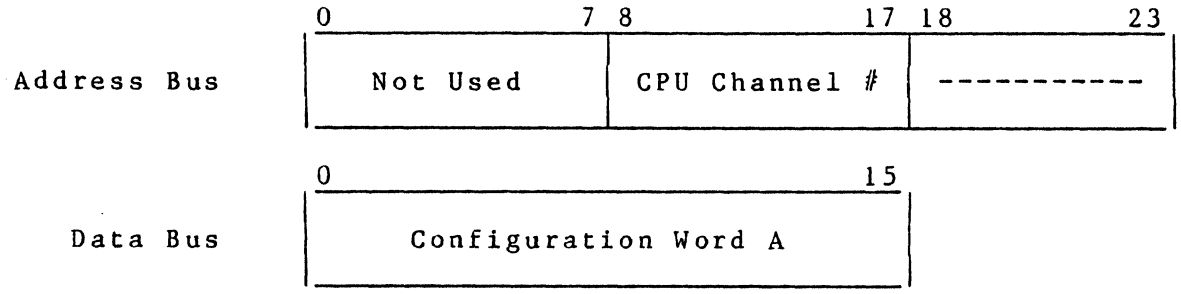
During the response cycle (second half read), the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the request cycle. The data bus contains the high order 8 bits of the memory word address currently stored for the specified channel in the MPTC. This command is used for diagnostic purposes only. For the QLTI explanation, refer to subsection 8.3.3, Maintainability Features.

5.2.10 Input Configuration Word A

Request Cycle



Response Cycle

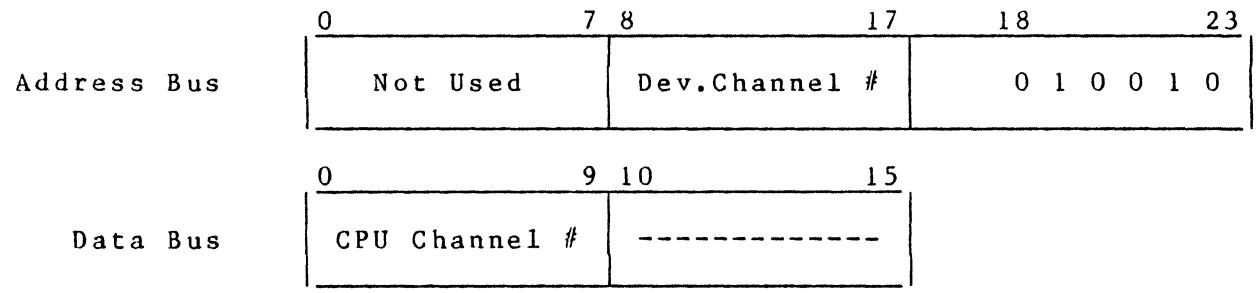


This instruction causes the current contents of the referenced channel's configuration word A register to be transferred to the requesting channel.

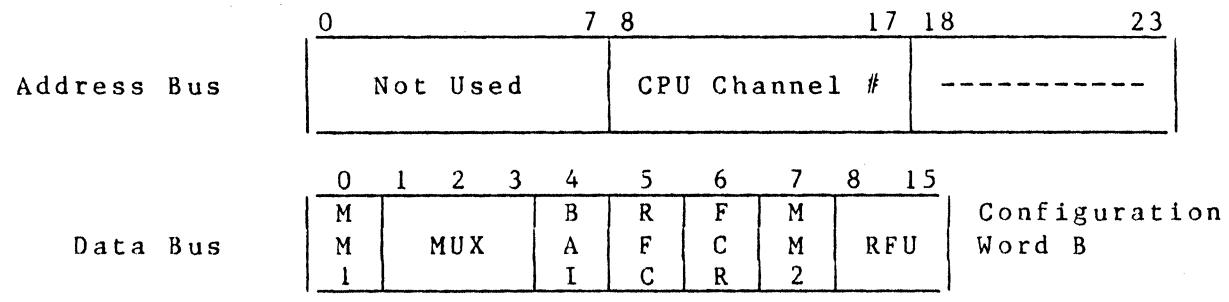
During the response cycle (second half read), the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the instruction cycle.

5.2.11 Input Configuration Word B (Used by the STC drive T&V only)

Request Cycle



Response Cycle



This instruction causes the current contents of the referenced channel's configuration word B register to be transferred to the requesting channel.

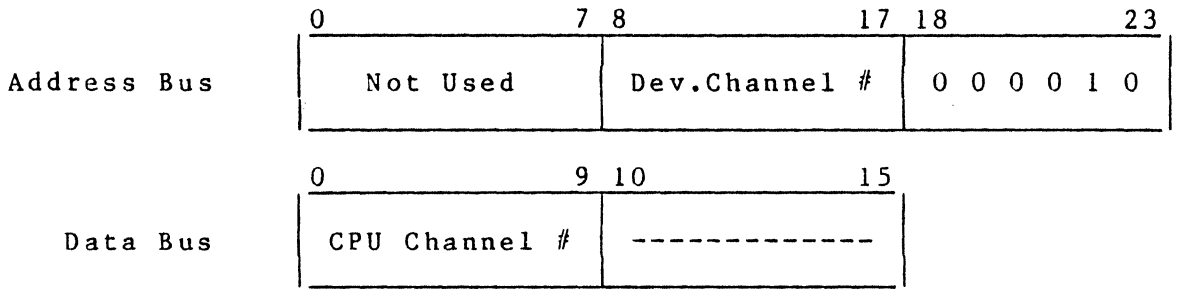
During the response cycle (second half read), the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the instruction cycle.

The bit significance is defined below. This command is intended for STC drive diagnostic and maintenance purposes.

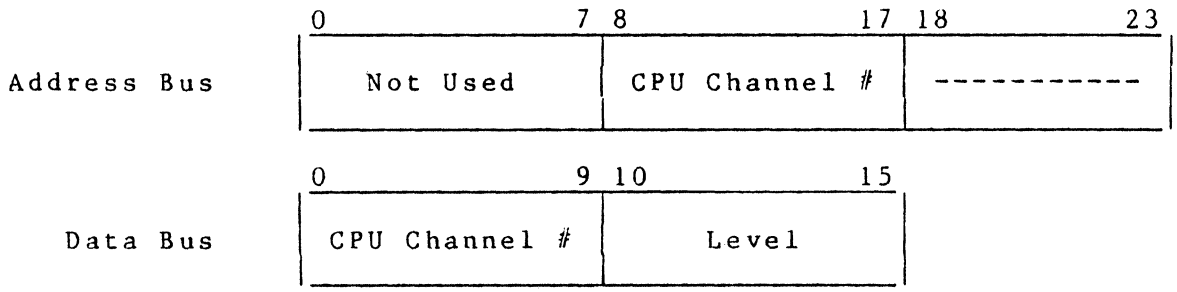
- Bits 0-3&7 R, Reserved for use in Output Configuration Word B (see subsection 5.2.3).
- Bit 4, BAI Bus Address Inhibit; Used for processing data in diagnostic mode only.
- Bit 5, RFC Reset Formatter/Controller; Diagnostic mode only.
- Bit 6, FCR Formatter/Controller Ready; Indicates that it is ready for the next command.
- Bits 8-15 RFU, Reserved for future use.

5.2.12 Input Interrupt Control

Request Cycle



Response Cycle



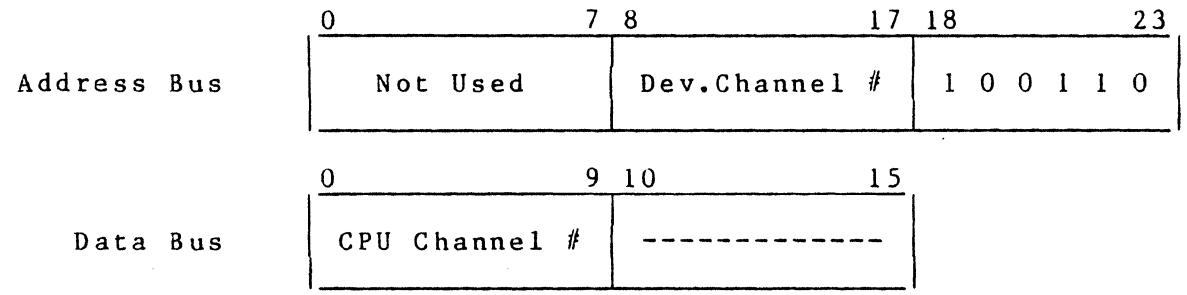
This instruction causes the channel's interrupt level to be transferred to the requesting channel. The level value is placed on data bus bits 10 through 15 (see above) with bit 15 as the least significant bit. This quantity is the value previously received in an Output Interrupt Control instruction or a default value of 00. The default value is the interrupt

level assumed by the channel when initialized. Note that the channel number returned in bits 0 through 9 of the data bus may be different than the channel number of the CPU executing this instruction if more than one CPU is attached to the Megabus.

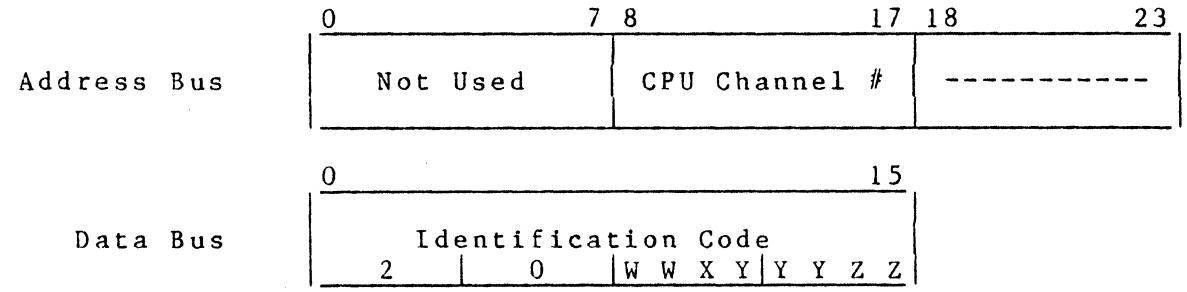
During the response cycle (second half read), the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.13 Input Identification Code

Request Cycle



Response Cycle



This instruction causes the referenced channel to transfer its identification code to the requesting channel. The codes for each type of tape controller attached to the MPTC are:

During the response cycle (second half read), the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the request cycle.

- Bits 0-7 = 20_{16} - Identifies MPTC-GCRA tape subsystem
- Bits 8-9 = WW - Identifies controller type attached to MPTC:

  00 - RFU
  01 - F/C (GCR/PE drives)
  10 - RFU
  11 - RFU

- Bit 10 = X - Number of transverse tracks

  0 - 9 tracks
  1 - 7 tracks

- Bits 11-13 = YYY - Identifies tape densities which the channel can accommodate:

  100 - 6250 CPI (GCR)
  010 - 1600 CPI (PE)
  001 - 800 CPI (NRZI, not implemented)

- Bits 14-15 = ZZ - Tape Speeds:

  00 - 25 ips
  01 - 50 ips
  10 - 75 ips
  11 - 125 ips

Code (Hex.)	Model
2058	25 ips PE/GCR - RFU
2059	50 ips " - RFU
205A	75 ips " - CDC
205B	125 ips " - STC
205F	Unloaded device

5.2.14 Input Task Word

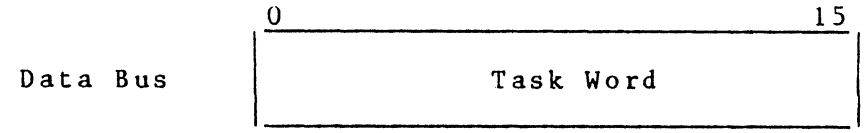
Request Cycle

	0 7	8 17	18 23
Address Bus	Not Used	Dev.Channel #	0 0 0 1 1 0

	0 9	10 15
Data Bus	CPU Channel #	----------

Response Cycle

	0 7	8 17	18 23
Address Bus	Not Used	CPU Channel #	----------



This instruction causes the task word of the referenced channel to be transferred to the requesting channel. The task word transferred contains the code for the last operation executed by the channel (unless an initialize has occurred).

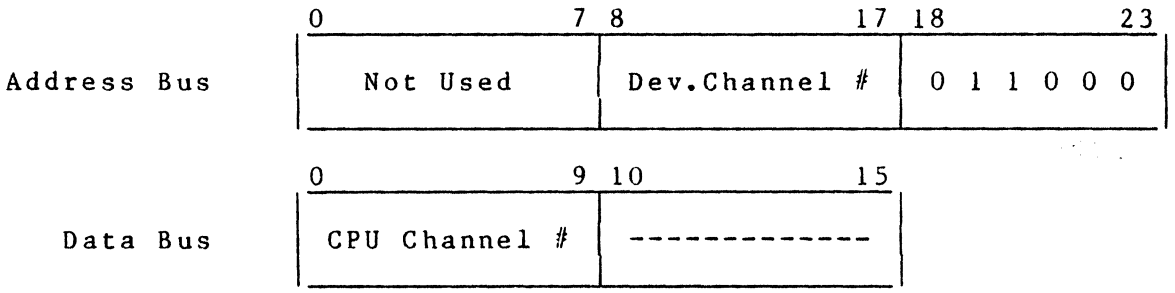
During the response cycle (second half read) the MPTC returns in bits 8 through 23 of the address bus the same data that was received in bits 0 through 15 of the data bus during the request cycle.

5.2.15 Input Status Word 1

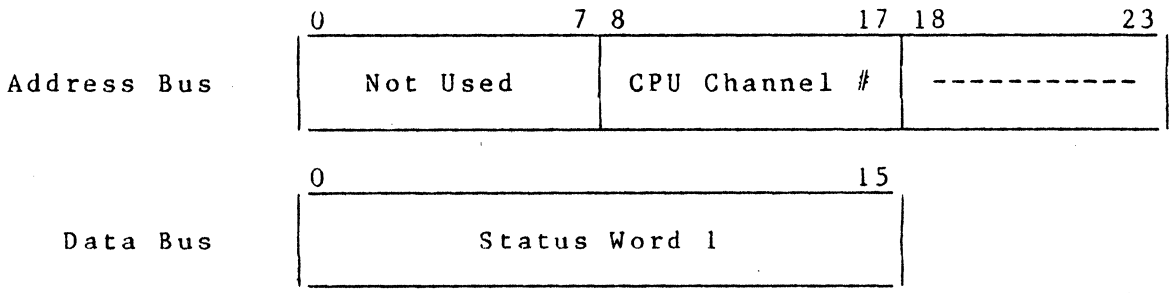
This instruction causes the referenced channel's Status Word 1 to be transferred to the requesting CPU channel.

During the response cycle (second half read), the MPTC returns, in bits 8 through 23 of the address bus, the same data that was received in bits 0 through 15 of the data bus during the request cycle.

Request Cycle



Response Cycle



Data Bus bit assignment:

Data Bit		Description
0	----------	Device Ready
1	----------	Attention
2	----------	Retryable Media Error
3	----------	Subsystem Fault
4	----------	Corrected Media Error
5	----------	Tape Mark Detected
6	----------	Beginning Of Tape
7	----------	End Of Tape
8	----------	Unequal Length Check
9	----------	Nonretryable Error
10	----------	RFU-MBZ
11	----------	Operation Check
12	----------	Corrected Memory Error
13	----------	Nonexistent Resource Error
14	----------	Bus Parity Error
15	----------	Uncorrected Memory Error

5.2.15.1 Device Ready (Bit 0)

This bit indicates that the device is on line with the medium loaded, is not rewinding, and that no further manual intervention is required to place it under program control. This bit is zero if either Status Word 2, bit 0 is a zero or Status Word 2, bit 1 is a one. Note that a change of state of this bit causes the attention bit (bit 1) to be set resulting in an interrupt (if the interrupt level is not zero).

5.2.15.2 Attention (Bit 1)

This bit indicates that an event has occurred at the device which requires software action. This event, moreover, is not related to the current task but, rather, is unsolicited. This bit is set whenever the device changes its ready condition as a result of a nonsoftware initiated command; that is, entering or leaving the on line state, rewinding state, or media loaded state. Attention status may occur following a software initiated Stop I/O or Initialize command if the device is performing a Rewind or Rewind and Unload instruction.

Whenever the attention bit is set, an interrupt is attempted (if the interrupt level is not zero). If a previously initiated operation is in progress when a device state change is sensed, the resultant interrupt (with the attention bit set) serves as notification of both the end of the operation and the device state change.

This bit is reset by the Initialize (see subsection 5.2.6.1) or the Input Status Word 1 command.

5.2.15.3 Retryable Media Error (Bit 2)

This bit indicates that a data error has occurred and is set whenever Status Word 2, bits 4, 5, 6 (conditional), or 7 are active.

This bit is reset by the Initialize or an Output Task Word command.

5.2.15.4 Subsystem Fault (Bit 3)

This bit indicates that the MPTC-GCRA has detected a controller type fault (F/C or MTU) which cannot be associated with a particular tape drive. Software treats this error as if the entire subsystem [that is, F/C and its attached tape drive(s)] is down and requires maintenance action. The cause of this fault is indicated in Status Word 2, bits 12, 13, and 14.

This bit is reset by the Initialize or an Output Task Word command.

5.2.15.5 Corrected Media Error (Bit 4)

This bit indicates that an error condition was detected on the media; however, the data read is not lost. For this subsystem, the detected condition indicates that a single track error has been corrected during a PE operation, or that single or double track error correction has taken place during a GCR operation. This bit is also set when a read retry by the MPTC-GCRA was successful.

This bit is reset by the Initialize or an Output Task Word command.

5.2.15.6 Tape Mark (Bit 5)

This bit indicates that a Tape Mark has been detected during the execution of a Write Tape Mark (In buffered CDC drive the Tape Mark command has been stacked; in unbuffered CDC and STC drives Tape Mark status has been sensed by the Read Head from the tape medium), Forward Space Tape Mark or a Back Space Tape Mark order. This status bit is also active if the block encountered during execution of a forward, a backspace or a read block instruction is a tape mark.

This bit is reset by the Initialize or an Output Task Word command.

5.2.15.7 Beginning-of-Tape, BOT (Bit 6)

This bit indicates that the BOT marker is positioned at the BOT sensor. A backspace or rewind order issued to a device with its tape at BOT results in no tape motion initiated and a normal termination of the order.

5.2.15.8 End-of-Tape, EOT (Bit 7)

This bit indicates that the EOT marker is positioned at or has passed beyond the EOT sensor. This status bit remains active until the EOT marker passes back over the sensor as the result of a tape backward motion command (for example, backspace or rewind). The state of this status bit has no effect on forward motion commands.

5.2.15.9 Unequal Length Check (Bit 8)

This bit indicates that for the previous read operation, the physical block was either greater or less than the value in the range register at the beginning of the read operation. If this bit is one and there is a residue in the range register, a short block was transferred. If this bit is a one and the range register content is zero, a long block was transferred.

This bit is reset by the Initialize or an Output Task Word command.

5.2.15.10 Nonretryable Error (Bit 9)

This bit indicates that the position of tape under the read/write and erase heads is unknown. This bit is set when:

- A write order RAW failure occurs; that is, the detection of magnetic transitions on tape before the start or following the completion of a recorded data block, the failure to detect magnetic transitions in the area where a data block is being written, or the failure to detect a GCR or PE density identification area on tape when writing a GCR or a PE tape, respectively (Status Word 2, bit 8 is set).

- An erase order RAW failure occurs; that is, the detection of magnetic transitions in the area on tape being erased.

- During a read order, a split block is detected (a split block is a data block in which its beginning and end positions cannot be guaranteed because of a detected unrecorded area within the block).

This status bit also becomes active when Status Word 2, bit 15 (Data Check Error) is set.

This bit is reset by the Initialize or an Output Task Word command except by Sense Drive Status, NOP or Store Detail Status Tasks.

5.2.15.11 RFU-MBZ (Bit 10)

This bit is reserved for future use and must be zero.

5.2.15.12 Operation Check (Bit 11)

This bit indicates that:

- o A write type order (write, write tape mark, erase) was issued to a tape drive in the write protect state (see Status Word 2, bit 2).
- o Upon acceptance of an output task word data transfer command, the direction of data transfer is not the same as that specified by the direction bit of the channel number issued by the previous Output Address command.
- o Upon acceptance of an output task word data transfer command, the content of the range register is Zero (write only or range is less than 18 on write if ANSI override is present).
- o A command was issued to a channel on which the device is in the off line or not ready state.

This bit is reset by the Initialize or an Output Task Word command.

5.2.15.13 Corrected Memory Error (Bit 12)

This bit indicates that during execution of the previous operation, main memory detected and corrected a memory read error. The data delivered to the MPTC-GCRA was assumed to be correct.

This bit is reset by the Initialize or an Output Task Word command.

5.2.15.14 Nonexistent Resource Error (Bit 13)

This bit is set whenever the MPTC-GCRA attempts a write or a read request bus cycle and receives a NAK response. Occurrence of this condition does not cause a termination of the operation in progress; however, it may result in bad data being written on the medium.

This bit is reset by the Initialize, an Input Status Word 1, or an Output Task Word command.

5.2.15.15 Bus Parity Error (Bit 14)

This bit is set whenever the MPTC-GCRA detects a parity error on either byte of the data bus during any output bus cycle (that is, odd function code), during a second half memory read cycle, or when a parity error is detected in bits 0 through 7 of the address bus during an Output Address command. Occurrence of this condition does not cause a termination of the operation in process; however, it may result in bad data being written on the medium.

This bit also indicates that the bidirectional data bus has detected an even parity data byte during a TREQ/TRAK (reference subsection 4.2.3.2.4 and 4.2.3.1.2, respectively) data transfer. On write operations, assertion of this line indicates that the data written on tape is incorrect; on read operations, assertion of this line indicates either an uncorrectable read error or an internal malfunction of the tape read data processing subsystem.

This bit is reset by the Initialize or an, error free, Input Status Word 1 command.

5.2.15.16 Noncorrectable Memory Error (Bit 15)

This bit indicates that during execution of the previous operation, the main memory detected a memory read error which the EDAC algorithm could not correct. The data that was delivered to the MPTC-GCRA was incorrect. Occurrence of this condition does not cause a termination of the operation in progress; however, it may result in bad data being written on the medium.

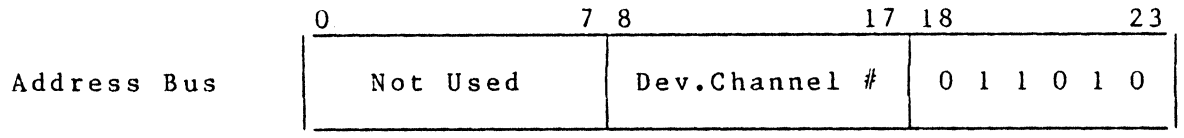
This bit is reset by the Initialize or an Output Task Word command.

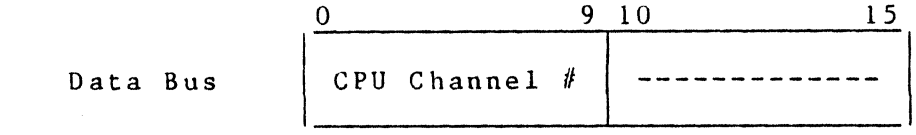
5.2.16 Input Status Word 2

This instruction causes the referenced channel's Status Word 2 to be transferred to the requesting channel.

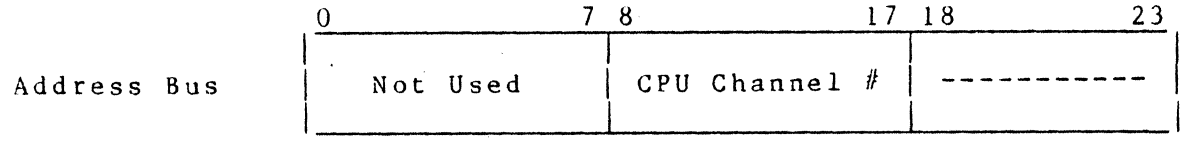
During the response cycle (second half read), the MPTC returns in bits 8 through 23 of the address bus the same data received in bits 0 through 15 of the data bus during the instruction cycle. Bits 0 through 7 of the address bus and the parity bit associated with these bits are the same data as received during the instruction cycle.

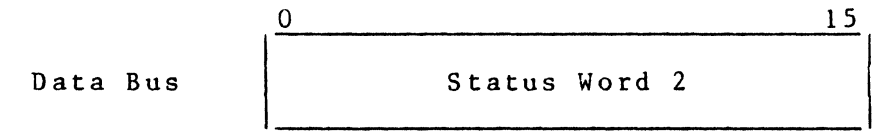
Request Cycle





Response Cycle





Data Bus bit assignments:

Data Bit		Description
0	----------	On line
1	----------	Rewinding
2	----------	File In Protect
3	----------	Density Select - HDNS
4	----------	Data Service Rate Error
5	----------	Uncorrectable Character Error
6	----------	Single Channel Error (PE)/GCR, PE, CRC
7	----------	Multiple Channel Error PE/GCR
8	----------	ID Burst Area Error
9	----------	Retry Attempted
10	----------	RFU-MBZ
11	----------	Functionality Not Available
12	----------	Reject (F/C)
13	----------	ROM Parity Error
14	----------	CLI Parity Error
15	----------	Data Check Error

5.2.16.1 On Line (Bit 0)

This bit indicates that the device is on line to the subsystem. The device can be put into an on line or off line condition via the on line/off line switch on the transport. The transport can also be put into off line status via the Rewind and Unload instruction.

5.2.16.2 Rewinding (Bit 1)

This bit indicates that the device is processing a rewind operation, either via a command issued by the subsystem or by the rewind switch on the transport. This bit is not visible to software when rewinding has been initiated by a command because I/O commands issued to a busy channel are NAK'ed.

5.2.16.3 File in Protect (Bit 2)

This bit indicates that the device is in write protect; that is, the write permit ring is not in position on the mounted file reel.

5.2.16.4 Density Select (Bit 3)

HDNS	
0	PE - 1600 bpi
1	GCR - 6250 bpi

5.2.16.5 Data Service Rate Error (Bit 4)

This bit indicates that during a read or write operation, data transfer between main memory and the F/C via the MPTC-F/C did not maintain the rate in demand. Either data was lost on input because of failure to keep up with the F/C demands, or data was unavailable on output when required by the F/C. The detection of this error condition does not affect the execution of the operation in progress.

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.6 Uncorrected Character Error (Bit 5)

This bit indicates that during a read or write operation, either a Vertical Redundancy Check (VRC) error and/or a dropped character error was detected. VRC Error (PE, GCR); one or more data characters were detected with incorrect vertical parity. Data character parity is odd unless bit 3 in the stored configuration word is set (see subsection 5.2.2). Retryable Media Error (Status Word 1, bit 2) is also set with this type of error.

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.7 Single Channel (PE)/CRC (GCR) Error (Bit 6)

This bit indicates that during a write operation for PE, a single channel error was detected. During read operations, single channel errors are corrected by the F/C and also set Status Word 1, bit 4. During write operations, single channel errors set bit 2 of Status Word 1 (Retryable Media Error). The detection of a single channel error does not prevent the detection of a multiple channel error in the block.

This bit indicates that during a read or write operation for GCR, the media CRC (Cyclic Redundancy Check) character failed to compare with the reconstructed value. It also causes the setting of Status Word 1, bit 2.

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.8 Multiple Channel (GCR/PE) Error (Bit 7)

This bit indicates that a multitrack error has occurred during a PE or GCR operation which was not correctable by the

F/C internally. Detection of these error conditions also sets Status Word 1, bit 2.

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.9 ID Burst Area Error (Bit 8)

This bit indicates that during a read or write (RAW) operation, an error was detected in the ID burst area; that is, the ID burst cannot be read or an incompatibility exists in the ID burst area (for example, PE burst when attempting to read in GCR mode). Nonretryable Error (Status Word 1, bit 9) is also set when this error occurs.

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.10 Retry Attempted (Bit 9)

This bit is set whenever the MPTC-GCRA attempts a read retry (see subsection 5.2.5.7), regardless of whether or not the retry was successful.

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.11 Functionality Not Available (Bit 11)

This bit indicates that for the Output Task Word, Read Backwards command, is not available, or that an attempt is made to utilize a feature which is not available. The order terminates without tape motion.

This bit is reset by the Initialize or an Output Task Word Command.

5.2.16.12 Reject (F/C) (Bit 12)

This bit indicates that the F/C has responded to a command sequence from the MPDC-GCRA with the Reject signal at the incorrect time. This indicates a serious error in the F/C and also causes the setting of Subsystem Fault (Status Word 1, bit 3).

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.13 ROM Parity Error (F/C) (Bit 13)

When set, this bit indicates that the control memory portion of the F/C detected a word having incorrect parity. This line points out a serious hardware malfunction which should be repaired before attempting to use the F/C again. Subsystem Fault (Status Word 1, bit 3) is also set when this error occurs.

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.14 CLI Parity Error (Bit 14)

This bit indicates that a parity error has been detected on the CLI interface (GCRA-F/C). Occurrence of this condition does not cause a termination of the operation in process; however, it may result in bad data being written on the medium. Subsystem Fault (Status Word 1, bit 3) is also set as a result of this error.

This bit is reset by the Initialize or an Output Task Word command.

5.2.16.15 Data Check Error (Bit 15)

This line is asserted by the F/C when any of the following error conditions occur. Subsection 5.2.5.13.4 (F/C Status Word 3) describes the following errors:

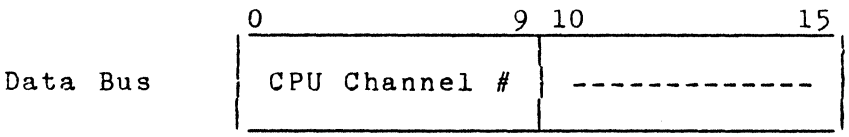
- CRC Error
- Write Tape Mark Check
- Uncorrectable Error
- * Partial Record
- Multiple Track Error (During a GCR read operation, three or more tracks must be in error to set data check.)
- End Data Check
- * Velocity Error
- BOT Reached (This error indicates that a backward command was initiated with tape positioned off BOT and BOT was reached before the end of the command. ID burst and BOT are also set.)
- Overrun (During read/write operations, the GCRA is not able to accept/select data fast enough.)

5.2.17 Input Firmware Revision

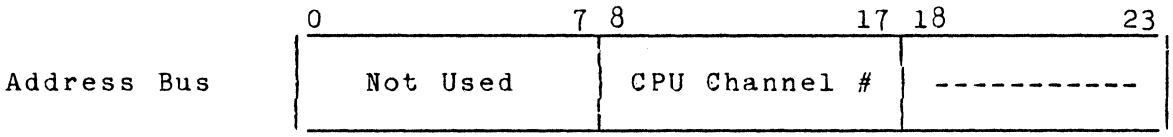
Request Cycle

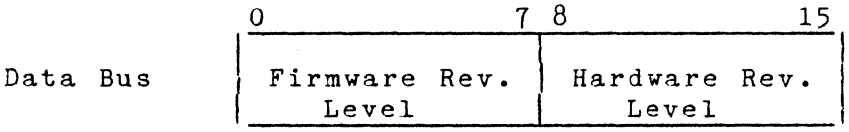
	0 7	8 17	18 23
Address Bus	Not Used	Dev.Channel #	1 1 1 1 0 0

* STC drives only.



Response Cycle





The firmware revision level is represented by a hex number; for example, 23.

The hardware revision level is represented by a hex number; for example, 3.

5.2.18 Read/Write MPTC Registers

The MPTC maintains 32 registers (16 bits per register) for each device. The address of each of the various registers in the MPTC is a combination of 2 bits of the channel number and the high order 5 bits of the function code used to write into or read from a particular register (see Figure 5-6). For example, configuration word A for MPTC device 2 is MPTC register 48 (hex).

Function Codes:

- Configuration Word A = 01000X (X = Read/Write bit)
- Device Number = 010Z (Z = Direction bit)
- Register Number = 0100 1000 = 48 (hex).

Complete software visibility to the MPTC registers is provided for diagnostic purposes. An output bus sequence addressed to one of the devices causes the information on the data bus (16 bits) to be loaded into the device specific register specified by the device port number and the high order 5 bits of the function code.

The Output Address command is a special case. When an Output Address command is executed (on part 0, for example) MPTC register 08 (hex) is loaded with the low order 16 bits of the address. The high order 8 bits of MPTC register 0B are loaded with the high order 8 bits of the address.

Any input bus sequence addressed to a device causes the register specified by the port number and the high order 5 bits of the function code to be returned to the register via the data bus (during the second half read cycle). A detailed register map for each device type is available in the MPTC/GCRA manuals.

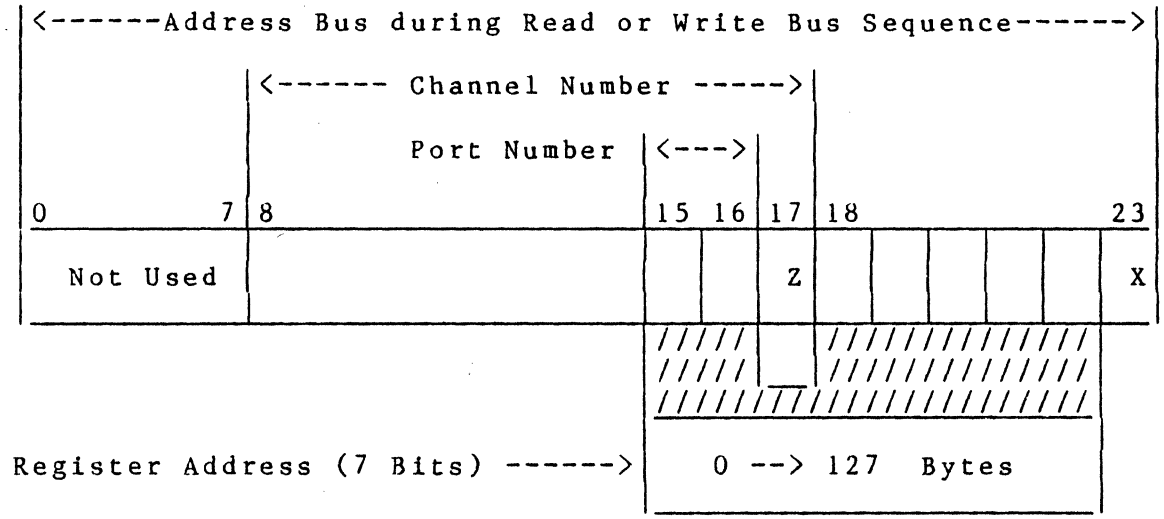


Figure 5-6 MPTC Device Specific Registers and Addressing

6. PHYSICAL AND LOGICAL STRUCTURE

6.1 Physical Structure

The GCR Magnetic Tape Subsystem consists of the MPTC (MPDC plus GCR tape firmware) M-board, the Group Coded Recording Adapter (GCRA), a 3/4-size D-board, and a 1/4-size ROS memory D-board. Also included are the OVP formatter/controller (STC only) for GCR/PE formatted tapes and up to four tape devices (F/C is included with each CDC drive).

6.1.1 Physical Specifications; MPTC

6.1.1.1 Mechanical

- Dimensions: 15 in. wide by 16 in. long by .062 in. thick M-board
- Weight: Approximately 28 oz
- Cabling: None
- Cooling: Forced unfiltered air at 125°F maximum temperature ambient at 110 CFM

6.1.1.2 Environment

- Per HIS Standard B01.08 - Class 3 (contamination requirements are waived)
- Meet all U.L. requirements.

6.1.1.3 Electrical

- Primary Power B01.08, Groups I, II, III
- Power module to share a common chassis with the printed circuit boards
- NML Power Specification (60131103).

6.1.2 Physical Specifications; Group Coded Recording Adapter (GCRA and ROS Daughter Boards)

6.1.2.1 Mechanical

- o Dimensions: 4.3 in. (36.33 cm) wide by 12 in. (30.48 cm) (combined) long by 0.062 in. (0.157 cm) thick
- o Weight: Approximately 16 oz (0.454 kg)
- o Cabling: Four 25-pin connectors to connect between M-board and D-boards. Three signal cables between the D-board and the OVP formatter/controller (STC) with a maximum distance of 30 feet.
- o Cooling: Forced, unfiltered air at 125°F (51.7°C) maximum ambient temperature at 110 CFM (51.9 liters/sec).

6.1.2.2 Environment

Same as 6.1.1.2.

6.1.2.3 Electrical

Same as 6.1.1.3.

6.1.3 Physical Specifications; OVP Formatter/Controller (for STC devices only)

6.1.3.1 Mechanical

- o Dimensions: 19.00 in. width
  21.10 in. depth (without cover)
  23.60 in. depth (with cover)
  10.50 in. height
- o Weight: 75 lb
- o Cabling: Each tape drive is connected to the F/C with two OVP supplied cables having a maximum length of 20 feet.
- o Cooling: Forced air cooling to satisfy operational temperature requirements.

6.1.3.2 Environment

The F/C shall withstand the following environmental extremes without adverse affects (reference HIS Standards B01.08 and B01.100.

- o Operational Temperature: 50°F to 100°F
- o Storage Temperature: -31°F to 149°F
- o Operating Humidity: 10% to 90% RH (noncondensing)
- o Storage Humidity: 5% to 89% RH (noncondensing)

- Operating Temperature Gradient: 19.8°F per hour
- Storage Temperature Gradient: 77°F per hour

- Meet all UL requirements.

6.1.3.3 Electrical

- Adequate storage unit protection to be provided

- Primary AC power: 120 Vac (+10%, -15%), single phase, 60 Hz ±0.5.

  220 Vac (+10%, -15%), single phase, 50 Hz ±0.5.

  240 Vac (+6%, -15%), single phase, 50 Hz ±0.5.

6.1.4 Physical Specifications; OVP GCR/PE 1/2-Inch STC Tape Drive (Used with the STC F/C Only)

6.1.4.1 Mechanical

- Dimensions: 19.00 in. width
  20.00 in. depth
  24.50 in. height

- Weight: 170 lb (without rack or cables)

- Cabling: Two signal cables connect the tape drive to the STC F/C

- Cooling: Forced air cooling to satisfy operational temperature requirements.

6.1.4.2 Environment

The tape device shall withstand the following environmental extremes without adverse affects (reference HIS Standards B01.08 and B01.10).

- Operational Temperature: 50°F to 100°F
- Storage Temperature: -31°F to 149°F

- Operating Humidity: 10% to 90% RH (noncondensing)
- Storage Humidity: 5% to 89% RH (noncondensing)

- Operating Temperature Gradient: 19.8°F per hour
- Storage Temperature Gradient: 77°F per hour

6.1.4.3 Electrical

- Adequate storage unit protection be provided

- Primary AC power: 120 Vac (+10%, -15%), single phase, 60 Hz ±0.5.

  220 Vac (+10%, -15%), single phase, 50 Hz ±0.5.

  240 Vac (+6%, -15%), single phase, 50 Hz ±0.5.

There is isolation of dc ground and frame ground in the tape drive. The two grounds are brought out to the I/O connector separately for external connection at a system level tie point.

6.1.5 Physical Specifications; GCR/PE 1/2-Inch CDC Streaming Tape Unit (STU); Buffered Keystone Model 92185-04.

6.1.5.1 Mechanical

- Dimensions: 19.00 in. width
  15.20 in. depth
  24.00 in. height
- Weight: 110 lb (without rack or cables)
- Cabling: Two signal cables connect the tape drive to the GCRA and/or to the next drive in a daisy chain connection for a maximum length not to exceed 30 feet.
- Cooling: Forced air cooling to satisfy operational temperature requirements.

6.1.5.2 Environment

The tape device shall withstand the following environmental extremes without adverse affects (reference HIS Standards B01.08 and B01.10).

- Operational Temperature: 50°F to 100°F
- Storage Temperature: -31°F to 149°F
- Operating Humidity: 10% to 90% RH (noncondensing)
- Storage Humidity: 5% to 89% RH (noncondensing)
- Operating Temperature Gradient: 19.8°F per hour
- Storage Temperature Gradient: 77°F per hour
- Operating Altitude: < 8200 Feet.

6.1.5.3 Electrical

- Adequate storage unit protection be provided
- Primary AC power: 100 Vac (+10%, -15%), single phase, 50/60 Hz ±0.5.

120 Vac (+10%, -15%), single phase, 60 Hz ±0.5.

Maximum Inrush Current: 9.0 Amps peak for 150 ms.
Maximum Operating Current: 4.2 Amps RMS
Average Input Current: 3.2 Amps RMS @ 75 ips streaming

220 Vac (+10%, -15%), single phase, 50 Hz ±0.5.

240 Vac (+6%, -15%), single phase, 50 Hz ±0.5.

Step (or slop) changes of ±15% of nominal must not exist for more than 0.1 second and occurring no more frequently than once every 10 seconds.

Partial or complete interruption of power for one cycle maximum, occurring no more frequently than once every 50 cycles and when the voltage is at the minimum of the operating range.

Average continuous power: 250 Watts RMS Low Speed Streaming
300 Watts RMS High Speed Streaming
equivalent to 1025 BTU's/hr.

Maximum continuous power: 400 Watts RMS

6.1.6 Physical Specifications; 1/2-Inch Magnetic Tape and Reels

6.1.6.1 Mechanical

The magnetic tape device provides for the front loading of tape media and reels which meet ANSI X3.40 1973. The tape handler accepts up to 10-1/2-inch diameter supply and takeup reels with a tape media capacity of up to 2400 feet; automatic cartridge loading and tape threading are accomplished through a power window.

6.1.6.2 Environment

The tape media shall withstand the following environmental extremes without adverse affects:

- B01.08 Environment: Operating
- B01.10 Environment: Manufacturing, Transportation and Installation
- B01.14 Data System Standard Unrecorded 1/2-Inch Magnetic Tape.

6.2 Logical Structure

Figure 6-1 is a block diagram of the GCRA. Major functional units and interfaces are illustrated in the figure. For

additional detail of the logical structure of the GCRA, refer to the MPTC-GCRA Product Manual.

6.3 Testability/Producibility

The product should conform to the manufacturing Testability and Producibility Design Rules outlined in the reference documents in subsection 1.1.2.

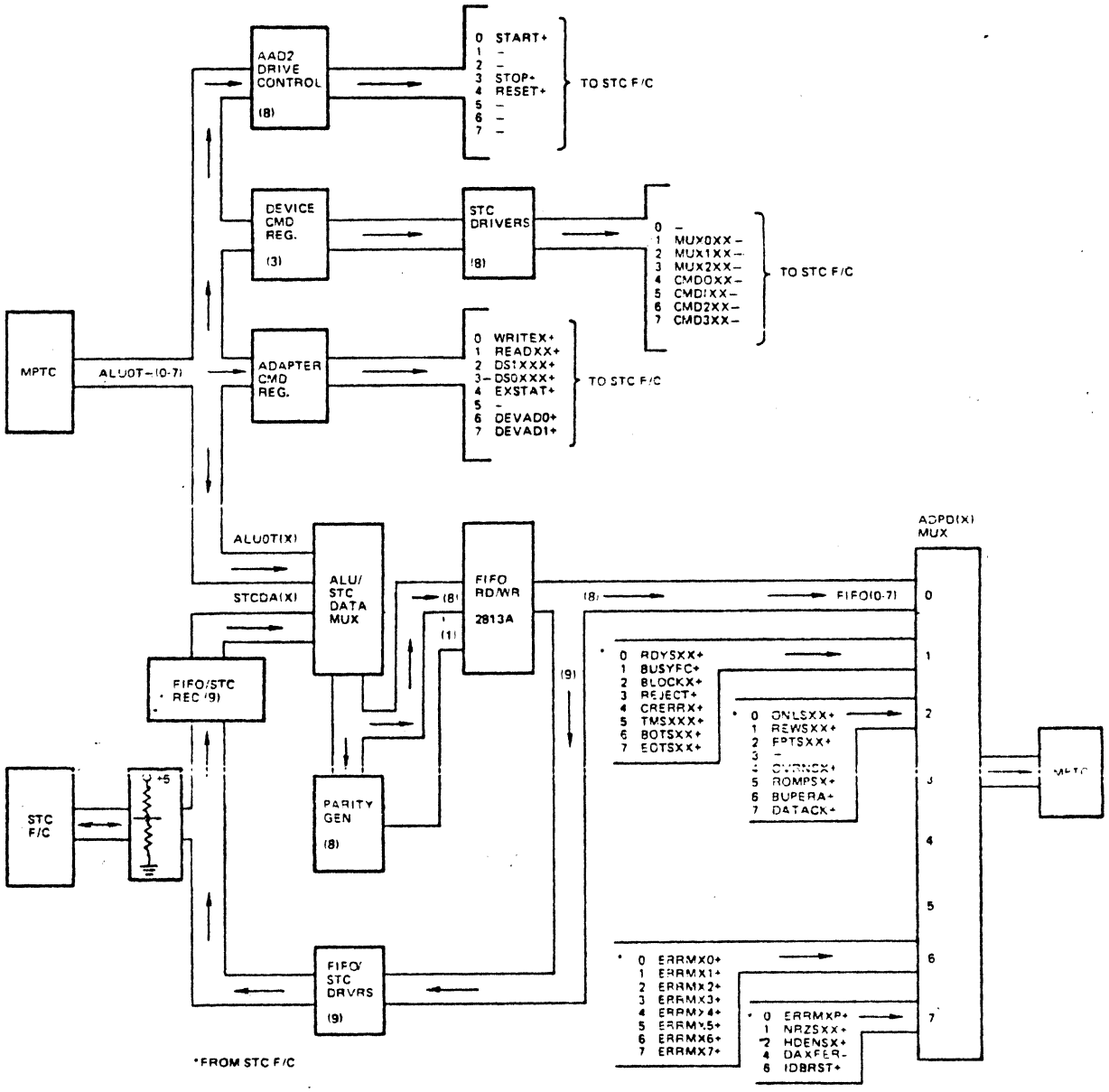


Figure 6-1 GCRA Functional Block Diagram

7. PERFORMANCE

The performance of the GCR Magnetic Tape Subsystem is expressed in terms of its maximum throughput requirements and the performance characteristics of the devices that can be configured to the subsystem. Performance characteristics are given in Table 7-1 and nominal data throughput in Table 7-2 and maximum instantaneous data rates in Table 7-3.

The MPTC-GCR, is a single level of simultaneity (LOS) subsystem, accepts up to four device specific command sequences, one for each available device. Multiple tape rewind operations may be processed concurrently with a single data transfer operation if the power distribution system allows.

DPS6 1/2-Inch Magnetic Tape Adapter Subsystems handle related tape which satisfy ANSI Standard X3.40-1973, Unrecorded Magnetic Tape for Information Exchange. The tape, having a nominal width of 1/2 inch and a thickness 1-1/2 millimeters, is normally stored on reels in lengths of 2400, 1200, 600, and 300 feet. Reels are capable of accepting a write-enable ring which, when removed from the reel, prevents the recording system from writing on media contained on the reel.

The DPS6 1/2-Inch Magnetic Tape Subsystem is capable of recording/reading tape employing the PE (Phase Encoding) and the GCR (Group Coded Recording) techniques only.

7.1 Recording Format

Compatible with ANSI Standards X3.54-1976 and X3.39-1973 for Recorded Magnetic Tape for Information Interchange (see subsection 5.1).

7.2 Capabilities

7.2.1 Recording

Write PE tapes conform to ANSI standards. Resultant recorded PE tapes are to be readable on DPS6 PE tape subsystems and foreign PE tape subsystems that have the capability to read ANSI standard PE tape media.

Write GCR tapes conform to ANSI standards. Resultant recorded GCR tapes are to be readable on DPS6 GCR tape subsystems and foreign GCR subsystems that have the capability to read ANSI standard GCR tape media.

CHARACTERISTIC	STC		CDC	
	GCR	PE	GCR	PE
Number of Data Tracks	9	9	9	9
Density of Data	6250 cpi	1600 cpi	6250 cpi	1600 cpi
Interblock Gap Nominal: Extended:	0.4"	0.6"	0.3" 0.6"	0.6" 1.2"
Tape Motion Forward	125	125	75/25	75/25
Tape Motion Rewind	500 ips	500 ips	192 ips	192 ips
Tape Head Configuration	Dual Read and Write with Separate Erase			

Table 7-1 1/2-Inch Magnetic Tape Subsystem Performance Characteristics

7.2.2 Reading

Read PE tapes in conformance with ANSI standards (tapes) which have been recorded on DPS6 PE tape subsystems, Series 700 PE tape subsystems, and/or Level 6 PE tape subsystems. PE tapes which are not in conformance with ANSI standards and are readable on HIS or foreign PE tape subsystems may or may not be able to be read by the DPS6 PE tape subsystem specified.

Read GCR tapes in conformance with ANSI standards (tapes) which have been recorded on DPS6 GCR tape subsystems, or other systems which conform to the ANSI standards. GCR tapes which are not in conformance with ANSI standards and are readable on other HIS or foreign PE tape subsystems may or may not be able to be read by the DPS6 GCR tape subsystem specified.

7.3 Data Transfer Rates and Capacity

The nominal data storage capacities and transfer rates for a 2400 foot reel of tape at 75 ips (without a data buffer), are as follows:

		2k Block		4K Block		8K Block	
IBG (Inches)		0.6	1.2	0.6	1.2	0.6	1.2
PE:	Capacity (Avg. in MB)	31	24	37	31	41	37
	Transfer Rate (KB/s)	82	62	97	82	107	107
IBG (Inches)		0.3	0.6	0.3	0.6	0.3	0.6
GCR:	Capacity (Avg. in MB)	94	64	123	94	146	123
	Transfer Rate (KB/s)	245	166	322	245	381	322

Table 7-2 PE/GCR Capacity & Transfer Rate Comparison

In buffered mode (128 KByte buffer in CDC Keystone drive, only) transfer rate is selectable by a switch setting with $\pm 2\%$ accuracy:

1. 62.5 KBytes/sec.
2. 125.0 KBytes/sec.
3. 250.0 KBytes/sec.
4. 380.0 KBytes/sec.
5. 500.0 KBytes/sec.
6. 625.0 KBytes/sec.
7. 770.0 KBytes/sec.

The Keystone streamer operating speeds are:

1. 25 ips start/stop mode

2. 25 ips streaming mode; data rate in this mode can vary, on average, up to the maximum of 75 ips dependent on how well the streaming rate approaches the optimum.

3. 75 ips streaming mode

The instantaneous maximum data transfer rates across the tape adapter GCRA to F/C interface are as follows:

DENSITY (cpi)	TAPE DRIVE SPEED (ips)	TRANSFER RATE (Bytes/sec.)
6250 (GCR)	125	780,000
	75	468,750
	25	156,250
1600 (PE)	125	200,000
	75	120,000
	25	40,000

Table 7-3 Instantaneous Maximum Data Rates

7.4 CDC Keystone Drive Characteristics

7.4.1 Maximum Block Size

a. Buffer Enabled

The maximum, switch selectable in 8 KByte increments, block size is 64 KBytes. This option defines the longest expected data block to be accommodated by the data buffer. The selected value is used to allocate the minimum data buffer space available to prevent the buffer from overflowing.

b. Buffer disabled.

64 KBytes maximum

7.4.2 Access Time, GCR Mode with buffer disabled.

a. High Speed Streaming

1. Write	150 ms
2. Read	154 ms

b. Low Speed Streaming

1. Write, after write	37 ms
2. Read, after read	28 ms
3. Write, after read	133 ms

c. Low Speed Start/Stop

1. Write	22 ms
2. Read, fixed short gap	24 ms
3. Read, fixed long gap	34 ms

7.4.3 Access Time, PE Mode with buffer disabled.

a. High Speed Streaming

1. Write	154 ms
2. Read	158 ms

b. Low Speed Streaming

1. Write, after write	70 ms
2. Read, after read	66 ms
3. Write, after read	190 ms

c. Low Speed Start/Stop

1. Write	22 ms
2. Read, fixed short gap	24 ms
3. Read, fixed long gap	48 ms

7.4.4 Interblock Gap

GCR Mode, minimum read gap supported	0.28"
Short Gap, fixed.	
- High Speed Streaming	0.3"
- Low Speed Streaming	0.3" to 0.45"
Short Gap, variable	0.3" to 0.45"
Long Gap, fixed	0.6"
Long Gap, variable	0.3" to 0.6"
Start/Stop	0.4"
Start/Stop, fixed long gap	0.6"
Extended Gap	
- Low Speed	0.3" to 1.2"
- High Speed	0.3" to 3.3"
PE Mode, minimum read gap supported	0.5"
Short Gap, fixed.	
- Low Speed Streaming	0.6" to 0.7"
- Low Speed Start/Stop	0.7
- High Speed	0.6"
Short Gap, variable	0.6" to 0.9"
Long Gap, fixed	1.2"
Long Gap, variable	0.6" to 1.2"

Extended Gap

- Low Speed	0.6" to 1.2"
- High Speed	0.6" to 3.3"

7.4.5 Positioning Time

a. High Speed	430 ms
b. Low Speed, write	130 ms
c. Low Speed. read	100 ms

7.4.6 Repositioning Time

a. Low Speed GCR, write	176 ms
b. Low Speed GCR, read	130 ms
c. Low Speed PE, write	164 ms
d. Low Speed PE, read	139 ms
e. High Speed PE/GCR, write	570 ms
f. High Speed PE/GCR, read	540 ms

NOTE

Rewind time for a 2400 foot tape on a 10.5" reel is 2.5 minutes.

7.4.7 Start/Stop Times

a. High Speed Streaming	120 ms
b. Low Speed Streaming	20 ms
c. Low Speed Start/Stop, PE	20 ms
d. Low Speed Start, GCR	20 ms
e. Low Speed Stop, GCR	60 ms

8. AVAILABILITY

8.1 Integrity

Integrity facilities in the GCR-MTS subsystem assure that data can be accurately written and retrieved from media. Data integrity is established via error detection facilities built into the data formats described in subsection 5.1. All data characters written on tape media have a parity bit appended such that when the data is subsequently read, the accuracy of the recovered data is guaranteed within the limits specified in subsection 8.4.1.4.

Error conditions detected at the device adapter subsystem (MPTC-GCRA) level are held in status registers of the MPTC (see subsections 5.2.14 and 5.2.15) for subsequent inquiry by a higher level processor. Hardware/firmware integrity is checked upon initialization of the MPTC-GCRA subsystem via test routines which determine if the subsystem can respond properly to basic input/output commands.

8.2 Security

Protection of data on media from being destroyed by unauthorized writing over or erasing is provided at the device level. Means for activation of this security, inhibiting any writing to a tape device, is by the removal of a write permit ring from a tape reel.

The detection of a write command issued to a protected device is reported in Status Word 1, bit 11 (see subsection 5.2.14.12).

8.3 Maintainability

8.3.1 Maintainability Requirements

The following design goals, measured in hours, are specified as a minimum to be achieved during the first year after the first customer ship.

8.3.1.1 Mean Time to Repair (MTTR)

MTTR represents the average repair time for a service engineer to diagnose, isolate, repair or replace, and verify the fix. MTTR does not include response time, travel time, or idle time at the site waiting for the system or needed spare parts. These MTTR times are given for each Optimum Replaceable Unit (ORU) that comprises the MPTS-GCR subsystem.

STC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	0.9 hr
Group Coded Recording Adapter	0.9 hr
OVP Formatter/Controller	1.5 hr
OVP Magnetic Tape Device	1.0 hr

CDC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	0.9 hr
Group Coded Recording Adapter	0.9 hr
OVP Magnetic Tape Device	0.75 hr

8.3.1.2 Maximum Time to Repair (XTTR)

This represents the time in which 90% of all repairs are made. XTTR is given for each ORU that makes up the GCR-MTS subsystem.

STC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	2.0 hr
Group Coded Recording Adapter	2.0 hr
OVP Formatter/Controller	2.4 hr
OVP Magnetic Tape Device	1.0 hr

CDC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	2.0 hr
Group Coded Recording Adapter	2.0 hr
OVP Magnetic Tape Device	1.0 hr

8.3.1.3 Diagnostic Facility Localization Effectiveness (DFLE)

This represents the probability that a hard failure will be localized to an ORU. The DFLE given takes into consideration the comprehensiveness, the resolution, and the accuracy of the diagnostic facility provided.

STC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	90 %
Group Coded Recording Adapter	90 %
OVP Formatter/Controller	90 %
OVP Magnetic Tape Device	80 %

CDC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	90 %
Group Coded Recording Adapter	90 %
OVP Magnetic Tape Device	80 %

The CDC Keystone tape transport diagnostics are invoked on power 'on', through the operators panel on the device or by a command, "Run Remote Diagnostics", from the GCRA. Detection effectiveness of the diagnostics package is 97% and isolation effectiveness is as follows:

a. 80% to a first replaceable assembly
b. 90% to a second replaceable assembly
c. 97% to a third replaceable assembly

8.3.1.4 Mean Time Between Preventive Maintenance (MTBPM)

This goal, the period between required or recommended preventive maintenance (PM), is given for each ORU.

STC Drive Subsystem	MTBPM
Medium Performance Tape Controller	No PM
Group Coded Recording Adapter	No PM
OVP Formatter/Controller	No PM
Run Diagnostics	Monthly
Check Fans and DC Voltages	Quarterly
OVP Magnetic Tape Device	Every eight hours for the principal tape path cleaning; weekly for the remaining tape path cleaning.

CDC Drive Subsystem	MTBPM
Medium Performance Tape Controller	No PM
Group Coded Recording Adapter	No PM
Run Diagnostics	Monthly
Check Fans and DC Voltages	Quarterly
OVP Magnetic Tape Device	Every eight hours for the principal tape path cleaning; 90 day cycle for the remaining tape path cleaning.

8.3.1.5 Mean Time to Perform Preventive Maintenance (MTTPM)

This goal applies to the OVP tape drives and is not more than four hours per year per device.

8.3.2 Maintenance Strategy

The maintenance strategy for the GCR-MTS subsystem is in accord with the governing EPS on the DPS6 System. The subsystem is partitioned into ORU's which can be effectively diagnosed for a faulty condition via a combination of firmware controlled tests, software tests, and visual indicators. Available diagnostic aids to be provided can be executed by either the customer or a service engineer. Simple repairs, such as the replacement of a defective ORU with an operational one, can be carried out by trained customer personnel or a service engineer.

8.3.3 Maintainability Features

- o Optimum Replaceable Units, ORU's, for the STC drive based subsystem are:
  - Medium Performance Tape Controller, MPTC
  - Group Coded Recording Adapter, GCRA
  - OVP Formatter/Controller, F/C; subassemblies, and components as required
  - Magnetic Tape Unit, MTU
- o Optimum Replaceable Units, ORU's, for the CDC (Keystone) drive based subsystem are:
  - Medium Performance Tape Controller, MPTC
  - Group Coded Recording Adapter (GCRA)
  - Magnetic Tape Unit (MTU)

Isolation of a failure to an ORU is achieved via a two step procedure. The first step is a hardware verification routine called a Quick Logic Test (QLT). This test supplies a go, no go visual identification of an MPTC hardware failure. Its purpose is to verify basic data paths such that appropriate ORU test and verification routines can be loaded and run. The QLT is restricted to verifing the MPTC board and the associated adapter. Successful completion of the QLT does not imply that the MPTC is free of faults but indicates that the subsystem can be responsive to commands issued to it.

The QLT is invoked in the MPTC in response to a Master Clear on the Megabus or an Initialize command, Output Control Word.

Results of the QLT appear as a visual indication on the system console and on the front edge of the MPTC board. The indicator LED turns on during execution of the QLT and turns off only if the QLT completes successfully.

Some specific function codes useful in troubleshooting hardware and firmware failures are as follows:

o Function code 04 (addressed to any active port) returns:

	0 — 7	8 — 15	
Data Bus	Firmware Rev. Level	GO Function Code	Example: 23,XX

o Function code 0A (addressed to any active port) returns:

	0 — 7	8 — 15	
Data Bus	QLTI	Memory Module Address	Example: FF,XX

Where QLTI = Quick Logic Test Indicators

During the initialization sequence, the QLTI location is used as follows:

- Set to FF on initialize.
- Set to 00 if any basic MPTC subtest fails.
- Set to FF if all basic MPTC subtests pass.
- Bits 4 through 7 are reset as a block if the Megabus QLT, executed prior to completion of an (first) input function code, fails.
- Bits 0 through 3 are selectively reset by CAI-Adapter QLT sequences when tests fail. Bit numbers correspond to port numbers.

If at the end of both QLTs (MPTC and GCRA) the QLTI register is FF, the indicator light on the front edge of the MPTC board is turned off. Conversely, if the QLTI register is other than FF, the light remains on. Examples of some QLTI contents and their interpretations are:

- FF = All QLTs were successful
- 00 = Basic MPTC (ALU, SPM, etc.) QLT failed
- F0 = Megabus QLT failed in one or more ports
- AF = Failure detected in ports 1 and 3

o Function code 20 (addressed to any active port) returns:

Data Bus

0 — 7	8 — 15
Fault Pointer	MBZ

Example: 2A,00

Fault Pointer Code	Subroutine In Error
01	RESETX-10 Low
02	STARTX+00 Low
	ERRMX7+00 Low
	ERRMXP+00 Low
03	SLX0XX-00 Hi
04	FIFOMT+00 Low
	ACKNOW+1A Low
	ERRMX6+00 Low
05	ZGND from G11
06	CMPARE+00 Hi
07	ADSTB0+10 Low
	ERRMX5+00 Low
08	DATSTB+00 Low
09	DSTWOT+00 Low
0A	ERRMX4+00 Low
0B	DSTOUT+00 Low
0C	FCSTOP-00 Hi
0D	BUSYXX-00 Hi
0E	ERRMX3+00 Low
0F	DAXFER-00 Hi
10	RESETX-10 Hi
11	AD1XXX-00 Hi
12	ERRMX2+00 Low
13	OUTRDY+10 Low
14	CMD0XX-00 Hi
15	SLX1XX-00 Hi
16	ERRMX1+00 Low
17	IDBRST+00 Low
18	CMD2XX-00 Hi
19	DS1XXX-00 Hi
1A	ERRMX0+00 Low
1B	SLX2XX-00 Hi
1C	FIF000+10 Low
1D	FIF001+10 Low
1E	BUSYFC+2A Low
1F	EORTST+10 Low
20	FIF002+10 Low
21	BLOCKX+00 Low
22	ADSTB7+10 Low
23	FIF003+10 Low
24	REJECT+00 Low
25	HDNSXX+00 Low

Fault Pointer Code	Subroutine In Error
26	FIF004+10 Low
	CRERRX+00 Low
	OVRNSX+10 Low
27	AD0XXX-00 Hi
28	FIF005+10 Low
29	ROMPSX+00 Low
2A	DS0XXX-00 Hi
2B	FIF006+10 Low
2C	BUPERA+00 Low
2D	CMD1XX-00 Hi
2E	FIF007+10 Low
	EOTXXX+00 Low
2F	CMD3XX-00 Hi
30	CMD0XX-00 Low
	CMD1XX-00 Low
	CMD2XX-00 Low
	CMD3XX-00 Low
31	SLX0XX-00 Low
	SLX1XX-00 Low
	SLX2XX-00 Low
32	DS0XXX-00 Low
	DS1XXX-00 Low
33	BUSYXX-00 Low
34	AD0XXX-00 Low
	AD1XXX-00 Low
35	HDTSRQ+00 Low
36	ADSTB0+10 Hi
37	FDTSRQ+00 Low
38	DATSTB+00 Low
39	NOHTRQ+00 Low
3A	BUSYXX-00 Low
3B	FDTSRQ+00 Hi
3C	ADSTB0+10 Low
3D	HOTSRQ+00 Low
3E	DAXFER-00 Hi
3F	HOTSRQ+00 Low
40	CMPARE+00 Low
41	DAXFER-00 Hi
42	HDTSRQ+00 Low
43	NOHTRQ+00 Hi
44	OUTRDY+10 Hi
45	HDTSRQ+00 Low

Fault Pointer Code	Subroutine In Error
46	DSTOUT+00 Low
47	ADSTB7+10 Hi
48	NOHTRQ+00 Hi
49	ADSTB7+10 Low
4A	HDTSRQ+00 Low
4B	EORTST+10 Hi
4C	FIFOMT+00 Low
4D	CMPARE+00 Low
4E	DAXFER-00 Hi
4F	FCSTOP-00 Low
50	FIFOMT+00 Low
51	CMPARE+00 Hi
52	EORTST+10 Low
53	FCSTOP-00 Hi
54	CMPARE+00 Low
55	PARITY+00 Hi

Fault Pointer Code	Subroutine In Error
56	OUTRDY+10 Hi
57	FIFO00+10 Hi
58	FIFO01+10 Low
59	PARITY+00 Hi
5A	CMPARE+00 Low
5B	CMPARE+00 Hi
5C	FIFOMT+00 Hi
5D	FCSTOP-00 Low
5E	EORTST+10 Low
5F	FCSTOP-00 Low
60	CMPARE+00 Low
61	STARTX+00 Hi
62	FCBUSY+00 Hi
63	STARTX+00 Low

Table 8-1 Firmware Fault Pointer Codes

Software isolation test routines verify all the MPTC, GCRA operational aspects of the subsystem and isolate failures to the attached tape controller, the F/C, or the device. Operator interface with these routines is via the CPU control panel or a system console. These routines cannot share the system with other programs. Diagnostic functionality has been included in the subsystem to support software diagnostic routines (see subsection 5.2.2).

The designated GCRA and MPTC are easily removable and replaceable; only a screwdriver is required. System power must be off to remove an MPTC or GCRA. Removal and replacement philosophy for the attached tape controller (F/C) and the tape devices are defined by FED. T&V's can be used as an aid in identifying failed ORUs in the F/C or in the tape devices. Power for the F/C and the tape units is independent of system power, thus enabling powering down and replacement of failed devices without affecting system operation except where the specific devices in question are involved.

A test procedure for isolating faults to the MPTC, GCRA, or controller/device is supplied to support the QLT and the GCRA T&V routines. This test procedure is for execution by nontechnical, trained, customer personnel or field engineering personnel. Note that T&V programs have access to all device diagnostic features and data. The instructions available to do this are not necessarily available for normal programming use.

8.4 Reliability

8.4.1 Product Life

Product life is defined as the period of time within which the equipment performs within established reliability goals.

STC Drive Subsystem ORU	Product Life
Medium Performance Tape Controller	10 years
Group Coded Recording Adapter	10 years
OVP Formatter/Controller	5 years
OVP Magnetic Tape Device	5 years

CDC Drive Subsystem ORU	Product Life
Medium Performance Tape Controller	10 years
Group Coded Recording Adapter	10 years
OVP Magnetic Tape Device	5 years

8.4.2 Unit Power 'On'

For purposes of specifying reliability goals, the unit power 'on' is specified to be 500 hours per month. The unit power 'on' time of a component is also expressed in usage hours of the component (see subsection 8.4.1.6).

8.4.3 Duty Factor

The duty factor of the MPTC-GCRA subsystem electronics is 100% of the power 'on' time. The duty factor of the mechanical hardware (that is, moving parts) of the transport is 10% to 25% of the power 'on' time.

8.4.4 Data Error Rate Requirements

- The error rate goals for the following three categories are:

STC Drive Subsystem	Recording Mode	
Category of Error	GCR	PE
Detected write error	1×10^{9}	1×10^{8}
Detected recoverable read error	5×10^{11}	1×10^{10}
Detected unrecoverable read error	3×10^{12}	1×10^{11}

A detected unrecoverable read error condition is an error which remains after ten attempts to read the record in which the error is located.

- The first attempt error rate goals, without retries and corrections in the disabled data buffer, for the following three categories are:

CDC Drive Subsystem	Recording Mode	
Category of Error	GCR	PE
Detected write error	1×10^{7}	1×10^{7}
Detected recoverable read error	5×10^{9}	1×10^{9}
Detected unrecoverable read error	1×10^{11}	1×10^{10}

8.4.5 Mean Time Between Failures (MTBF)

MTBF is expressed in power 'on' hours of the component or ORU and is concerned only with hardware failures. It is a minimum to be achieved.

STC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	60,000 hr
Group Coded Recording Adapter	120,000 hr
OVP Formatter/Controller	4,000 hr
OVP Magnetic Tape Device	2,500 hr

CDC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	60,000 hr
Group Coded Recording Adapter	120,000 hr
OVP Magnetic Tape Device	5,000 hr

8.4.1.6 Mean Time Between Calls (MTBC)

MTBC is expressed in usage hours of the component or ORU between unscheduled or scheduled demand or emergency calls caused by hardware, operator, or media malfunctions which cannot be corrected by the operator or required installation of FCOs (Field Change Orders). A "call" is a visit to the customer site by a field engineer. MTBC does not include calls for preventive maintenance.

STC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	50,000 hr
Group Coded Recording Adapter	90,000 hr
OVP Formatter/Controller	2,500 hr
OVP Magnetic Tape Device	1,500 hr

CDC Drive Subsystem ORU	After First Year
Medium Performance Tape Controller	50,000 hr
Group Coded Recording Adapter	90,000 hr
OVP Magnetic Tape Device	1,500 hr

9. CONFIGURABILITY

9.1 General

Configurability requirements, restrictions, options, etc. for a GCR tape subsystem are described in this section. Figure 9-1 identifies the basic configurational units of the subsystem and their interfaces. The following paragraphs specify configurational characteristics of relevant units. Performance parameters, instructions, and interfaces are described in earlier sections.

9.2 MPTC (MPDC Plus GCR Firmware)

Specific configurational limitations of the MPDC can be found in the MPDC EPS. In general, the following points are pertinent to an GCR-MTS Subsystem:

- The MPTC functions in any MegaBus position. However, because of the burst transfer mode of operation of the MPTC and its data buffering, the MPTC is normally placed at the lower priority end of the bus but with a higher priority than the CPU.
- Multiple MPTCs may be configured for a particular Megabus system, but may be limited by the system throughput.
- No modifications to the basic MPDC are necessary for the support of an GCRA. However, a new firmware load makes the MPDC into an MPTC.
- The MPTC can support only one adapter. Refer to the MPDC EPS for descriptions of attachable adapters.
- The high-order seven bits of the subsystem channel numbers are assigned at system installation by the setting of switches on the MPTC (refer to subsection 3.1).

The following configuration rules apply:

- Maximum of four tape transports is allowed in the subsystem
- The STC Formatter/Controller (F/C) can handle up to four GCR/PE model # 1960 STC drives.
- Each CDC Keystone tape transport, GCR/PE, has an F/C with 128 KByte data buffer built in.

9.3 Group Coded Recording Adapter (GCRA)

The following points are pertinent to the attachment of the Group Coded Recording Adapter:

- The GCRA attaches to the MPTC via the Controller Adapter Interface. This interface is described in the MPDC EPS.
- The GCRA supports any of the configurations described with no hardware or firmware modifications.
- Device numbers (bits 7 and 8 of the channel number, see Figure 3-1) are assigned based on the position of the device on the DLI.

9.3.1 GCR/PE Formatter/Controller (F/C)

- The STC Formatter/Controller is used in peripheral subsustems with STC tape transports only.
- The F/C attaches to the GCRA via the CLI-F/C interface defined in Section IV
- Up to four GCR/PE tape drives may be attached to the F/C.

9.3.2 Magnetic Tape Devices

- STC MTUs connect radially to the STC F/C via the Device Level Interface as defined in Section 4.
- From one to four drives may be attached to the F/C (see Configuration Rules) in a radial fashion.
- CDC Keystone tape transports attach to the GCRA in a daisy chain fashion; up to four tape transports can be connected with a terminator in the last one.

9.4 Other Configuration Considerations

Availability parameters identified in Section 8 assume support by a DPS6 Operating System.

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