Honeywell

SERIES 60 (LEVEL 6)

Test and Verification Programs

Honeywell Test and Verification (T&V) programs are an integral part of the Model 6/34 and 6/36 maintenance strategy. Featured are automatically executed processor and memory tests permanently resident in read-only-memory, and a family of free-standing programs. All members of the 6/30 Model family include hardware or microcode features identified as necessary for either a complete test or to permit diagnosis to an appropriate level.

The Operator's Console is sought for and used, if present, for an initial question and answer session and presentation of error or successful test reports. If the console is not present a standardized data entry/extraction procedure is provided.

The diagnostic process culminates in a repair or adjustment procedure designed to be executed by an operator with little or no computer maintenance training. The optimum replaceable unit (ORU) selections permit the original specifications for reliability to be met after the repair is complete.

BLT – BASIC LOGIC TESTS

The central processor control store includes a microcode routine that checks microlevel CP functions for a high degree of confidence. Control is then transferred to a ROM resident routine which tests memory through 64K words.

A multiple device controller (MDC) BLT performs a similar test, plus a ROM test and initial device configuration analysis.

The result of any BLT not successfully completed, or the detection of an incomplete or unterminated bus will cause a control panel light to remain lit and the system cannot be operated normally. The specific board failing a BLT will also have a light showing. The tests require from one half to four seconds. Portions or all may be intentionally bypassed; however, execution of the normal bootstrap load process will include the full BLT sequence.

CENTRAL SUBSYSTEM TESTS

Central Processor (CPST1)

Tests the central processor instruction set, address syllable processing and trap/interrupt handling.

Central Processor (CPST2)

Measures the execution time for each of a representative set of instructions and address syllables. Requires the console option.

Memory (CMMT1)

Tests the visible and obvious function of memory to store data, with each bit-cell uniquely addressable. Tests the normally invisible functions including the MOS refresh, Error Detection and Correction (EDAC) or parity, and error detection by I/O controllers accessing main memory. Error detection on internal bus transfers is also tested.

Power Failure Detection (PSST1)

Tests the correct processing of detection of an impending shutdown due to power failure and the autorestart feature of the central processor. Requires the memory save option.

Real Time Clock/Watchdog Timer (CPFT1)

Tests the functions of the two standard clocking features and provides a long-term time-keeping exercise. Requires that operator have an accurate clock or watch. Also tests the CP and I/O bus for all levels of program dispatch, execution and interruption.

I/O SUBSYSTEM TESTS

Console (KCMT1)

Tests the keyboard, page printer, tape reader and punch and other features of the console option. If the console device is a KSR, checks that the correct set of device optional features is enabled/disabled.

Card Reader (CRMT1)

Tests the Hollerith mode by injecting 4096 codes and observing the correct translation or illegal code detection, and by reading a prepunched two card deck. Device operation and speed is tested by repeated passes of a user-supplied random deck using the direct transcription mode.

Printer (PRMT1)

Tests all features of the line and serial printers using obvious patterns and clear text. The printing rate is reported for three different line lengths.

Diskette (DIMT1)
Tests all features of the diskette subsystem using one or two devices.

General Purpose DMA Interface (GIST1)
Tests the I/O bus interface for DMA, PIO and interrupt functions and the user interface for data turnaround and request line recognition. The program remains valid when the user has added logic as long as the interface rules are followed. The user should consider expanding this program to test his added logic in a manner analogous to building on the interface controller.

MultiLine Communications Processor (MLCT1)
Tests all features of the MLCP. Requires at least one line adapter be present.

Communications Line Adapter (DCMT1)
Tests all features of both synchronous and asynchronous Communications-Pacs installed on an MLCP. Uses the Communications Pac data and control signal loopback test features or the operator may elect to turn the line around at the local or the remote modem. The program can also direct transmissions to a specific terminal.

T&V DISTRIBUTION

T&V programs are provided in standard image text format, previously linked with a utility subroutine library, and ready to load and execute. All programs have the same starting and successful ending locations. They are supplied as one diskette volume containing all T&V programs identified by standard T&V member names, or as individual paper tapes or punched cards. The user loads the selected T&V using a standard software loader. Relocation or execution under an operating system is not permitted.

— Specifications may change as design improvements are introduced.

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