HONEYWELL EDP

HARDWARE BULLETIN

SERIES 200

TYPE 281-1H COMMUNICATION CONTROL AND TYPE 285-1H COMMUNICATION ADAPTER

SUBJECT: Equipment Specifications - the Type 281-1H Communication Control and Type 285-1H Communication Adapter for use with Bell DATAspeed Type 2 Remote Terminals on Voice-Grade Dial Telephone Lines or on Leased Voice-Grade Telephone Lines.

SPECIAL INSTRUCTIONS: This bulletin updates the Honeywell Customer Information Bulletin Number 200-47, Communication Control Unit Specifications: Models 281-1H and 285-1H, dated February 10, 1965. The text uses the following references: the bulletins Type 281-1 Single-Channel Communication Controls, Order No. 086 and Type 286-1, 2 and -3 Communication Controls, Order No. 160; also the Honeywell Series 200 Models 200/1200/2200 Programmers' Reference Manual, File No. 113.0005.0000.00.00.

DATE: April 26, 1966

FILE NO:. 112.0005.1100.0-092*

8857
3466
Printed in U.S.A.

*When ordering this publication please specify Title and Underscored portion of File Number.

TABLE OF CONTENTS

TABLE OF CONTENTS (cont)

LIST OF ILLUSTRATIONS

EQUIPMENT SPECIFICATIONS FOR THE TYPE 281-1H COMMUNICATION CONTROL AND TYPE 285-1H COMMUNICATION ADAPTER

I. GENERAL DESCRIPTION

The Type 281-1H Single-Channel Communication Control and Type 285-1H Communication Adapter provide the interconnection of a Series 200 central processor with Bell DATAspeed Type 2 high-speed punched paper tape input/output terminals by means of a Bell DATA-PHONE Dataset 202C on switched, voice-grade telephone lines or Bell DATA-PHONE Dataset 202D on leased, point-to-point voice-grade private lines.

As illustrated in Figure 1, the Type 281-1H Communication Control is used to connect one voice-grade telephone line to the Series 200 central processor. The Type 285-1H Communication Adapter is utilized in conjunction with a Type 286 Multi-Channel Communication Control to connect one voice-grade telephone line when a maximum of 63 communication lines are to be connected to a central processor.

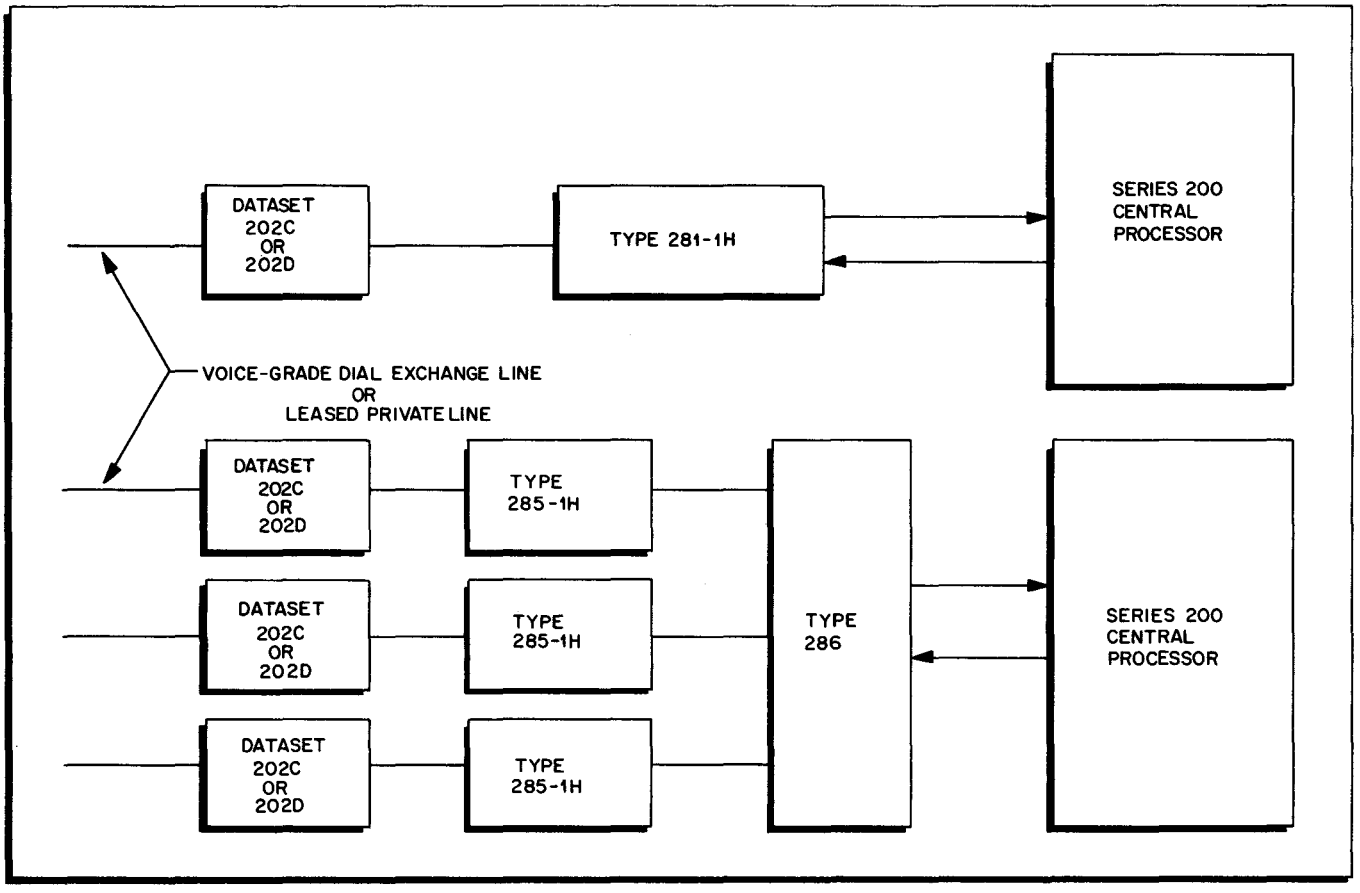

Figure 1. Type 281-1H and 285-1H Applications

The communication line is characterized by start-stop, synchronous serial transmission of any five-, six-, seven-, or eight-level code in the half-duplex (two-way, non-simultaneous) mode. The maximum line speed is 105 characters per second, 1050 bits per second, or 1050 words per minute.

Equipment at the remote stations consists of a Bell DATAspeed Type 2 in any one of the three following configurations:

Transmit Only — Paper Tape Reader and Control,

Receive Only — Paper Tape Punch and Control,

Composite Terminal — Paper Tape Reader and Punch.

The standard Series 200 logic drawer contains one Type 281-1H Communication Control or eight Type 285-1H Communication Adapters.

II. INTERFACE WITH THE SERIES 200 CENTRAL PROCESSOR OR THE TYPE 286 MULTI-CHANNEL COMMUNICATION CONTROL

A. Type 281-1H/Central Processor Interface

Standard peripheral interface logic for non-simultaneous input and output connects the Type 281-1H to the Series 200 standard peripheral bus.

B. Types 285-1H/286 Interface

Section IV of the Honeywell bulletin Type 286-1, -2 and -3 Multi-Channel Communication Controls describes this interface circuit.

III. INTERFACE WITH THE COMMON CARRIER LINE

The common carrier line termination is a Bell DATA-PHONE Dataset 202C or 202D.

The datasets convert the voltage-level signals of the communication devices into audio-frequency signals for transmission on the line.

IV. CODE CHARACTERISTICS AND REMOTE TERMINALS

A. Code Characteristics

Types 281-1H and 285-1H are capable of operation with five- through eight-level codes. The Bell DATAspeed remote terminal determines the ordering of the particular code. Arrangement of the codes in central processor memory is described in Section VI, G.

All line signals are transmitted or received in a basic ten-bit format. For eight-bit codes, this format provides a start bit, eight data bits and a stop bit, each of approximately 952 microseconds' duration.

In six-bit and seven-bit codes, superfluous bits are transferred as "marking" pulses (or bits equal to logical "1's") immediately preceding the stop bit. Six-bit code positions differ sequentially from those of the other codes, as shown in Figure 3, Section VI, G; the sixth bit precedes bits one, two, three, etc.

The first bit position of the five-bit code is superfluous and is transmitted as a "spacing" pulse (or bit equal to a logical "0"), while superfluous bit positions seven and eight are transmitted as marking bits.

B. Remote Terminals

1. Description

The remote terminals used with these communication devices are Bell DATAspeed Type 2 Stations equipped with Bell DATA-PHONE Datasets 202C for switched telephone circuit (dial exchange) service or with Bell DATA-PHONE Datasets 202D for leased point-to-point private line service, as illustrated in Figure 2, page 4.

A DATAspeed Type 2A ("Send") Terminal containing a Teletype Model CX Paper Tape Reader and Control is used for transmission of data from the remote site to the central processor.

A DATAspeed Type 2B ("Receive") Terminal containing a Teletype BRPE Paper Tape Punch and Control is utilized for reception of data from the central processor.

Each of these DATAspeed units is individually housed in a cabinet containing facilities for tape supply and "takeup." Paper tape input/output equivalents may be adjusted to accommodate five- through eight-level tapes.

DATAspeed Type 2A and 2B Stations at the same remote site may share a common dataset; this is the "composite" arrangement. In this case a manual selector switch adjusts the dataset for transmission or reception.

2. Compatibility

The Type 281-1H Communication Control and Type 285-1H Communication Adapter provide the interconnection of a Series 200 central processor with the following arrangements of Bell DATAspeed high-speed paper tape input/output terminals:

a. Basic attended operation of Type 2A ("Send"), Type 2B ("Receive") and Type 2 Composite Terminals over switched telephone circuits or voice-grade, leased, point-to-point private lines;

b. Unattended operation and automatic operation of Type 2B ("Receive") Terminals over switched telephone circuits or voice-grade, leased, point-to-point private lines;

c. Type 2A ("Send") DATAspeed terminals equipped with the five-second delay feature for unattended answer and automatic operation over leased, voice-grade, point-to-point private lines;

d. Basic configuration of five-level DATAspeed Type 1 terminals. (Although this equipment is no longer manufactured by Bell, existing units may still be encountered in the field.)

The Types 281-1H and 285-1H are not compatible with these Bell DATAspeed Type 2 combinations:

a. Dataspeed Type 2A ("Send") Terminals and Type 2 Composite Terminals equipped with "Discrete Character Recognition" for unattended answer and automatic operation;

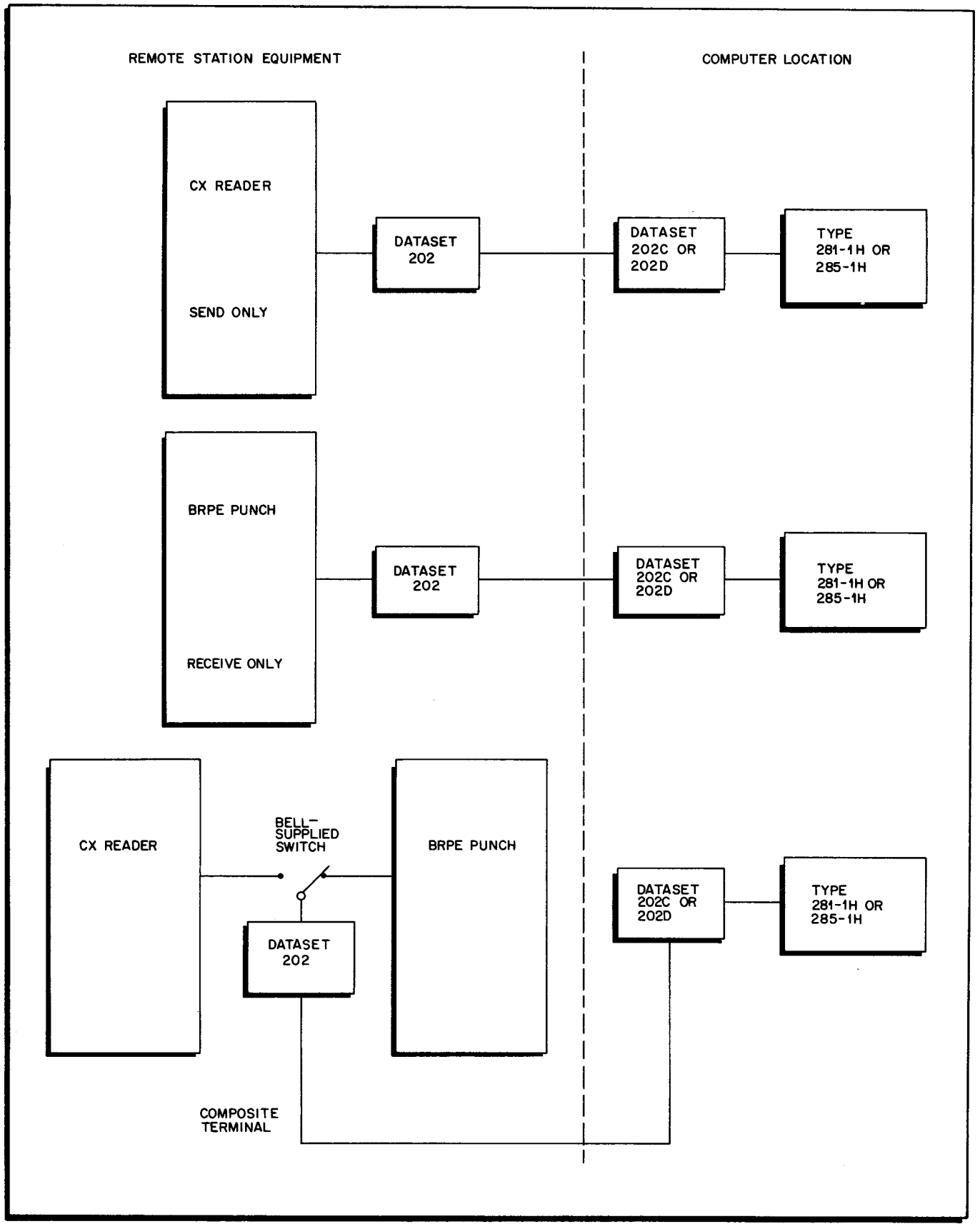

Figure 2. Bell System DATAspeed Terminals

b. DATAspeed Type 2A ("Send"), Type 2B ("Receive") or Type 2 Composite Terminals equipped for the "Reverse Channel Break" operation.

V. FUNCTIONAL DESCRIPTION

A. Type 281-1H

1. General

The Type 281-1H uses standard peripheral interface logic for non-simultaneous input or output. The logic also implements an eight-bit shift register serving as a buffer and serializer in receiving and transmitting; a strobe generator delivering a pulse to sample and shift individual bits; control functions to indicate whether the communication device is in the input or output mode and to signal activity, busy and error conditions to the central processor.

2. Reception

A "space" signal (0) on the communication line enduring more than one-half of a bit time switches the Type 281-1H to the receive mode.

A bit from the line moves into the buffer shift register, causing the bits already stored to be shifted one position. When all bits of one character are stored in the shift register, an Input Frame Demand is activated.

In the block mode of transmission, the Type 281-1H Communication Control has continuous access to the central processor by way of its read/write channel (RWC) and the Input Frame Demand is honored during the next memory cycle.

During the single-character method of transmission, two means exist for notifying the central processor of activity requests:

a. The Input Frame Demand is tested by a Peripheral Control and Branch (PCB) instruction frequently enough to ensure the removal of the stored character from the shift register within the stop-bit time.

b. A program interrupt saves repetitive testing for frame demands, although an Input Frame Demand condition should be checked before the subsequent "Input" PDT instruction is issued. (This method requires the program interrupt feature, which is standard equipment for all Series 200 central processors except the Type 201; Type 201 must be equipped with Feature 012, as described in the Models 200/1200/2200 Programmers' Reference Manual, pages 1-15 and 1-16.

3. Type 281-1H Transmission

Type 281-1H reception of an "Output" PDT instruction sets the Transmit function. Data arriving thereafter from the central processor over the output bus (six bits in parallel) is stored in the buffer shift register. Two six-bit transfers are required to transfer seven-bit or eight-bit characters.

Before the data is sent to the communication line, a start bit is generated. The character is then shifted through the shift register and onto the line. During part of the last-bit and stop-bit time an Output Frame Demand becomes active, as described in Section V, A, 2.

Activity requests to the central processor are handled as described in Section V, A, 2.

B. Type 285-1H

The functional description of the Type 285-1H is similar to that given in the preceding Section V, A, for the Type 281-1H, with these exceptions: the Type 285-1H mode of data transfer is always single-character and its activity requests are sent to the Type 286 Multi-Channel Communication Control. When a complete character is accumulated, an interrupt is sent to the central processor.

VI. PROGRAMMING REFERENCE DATA

NOTE

The following description is based on the presence of the program interrupt feature, which is standard equipment for all Series 200 central processors, except the Type 201. However, the basic Type 281-1H does not require this feature, since the system can be programmed using PCB instructions to test for "busy," thereby initiating a program branch whenever a request is made for service. Also, the following description applies mainly to the Type 281-1H; for Type 285-1H programming see the bulletin Types 286-1, -2 and -3 Multi-Channel Communication Controls.

A. General Description

Though the Type 285-1H — operating in conjunction with the Type 286 Multi-Channel Communication Control — uses only the single-character method of transmission, the Type 281-1H Communication Control handles data on a single-character or a block (message) basis.

Block transmission with the Type 281-1H permits handling of more data with less manipulation and fewer program interruptions than does single-character transmission. Therefore, block transmission is essential for use with very high-speed lines; also, it is often convenient for use with lower-speed lines, especially when communication is sharing computer time with other processing.

Whether operating on a single-character or a block basis, the Type 281-1H Communication Control requires that a record mark be set in the data storage area of main memory to terminate data transfer and to release the read/write channel.

B. Initial Start

The Type 281-1H starts when INITIALIZE is pressed on the central processor control panel.

C. Type 281-1H Stand-By Condition

Unless transmitting or receiving, the Type 281-1H is in a neutral state, permitting transmission by the program onto the communication line, but also interrupting the program when a character is received from the line.

If no characters are received from the line during a half-character period, the Type 281-1H interrupts the program with an output request. Thus, if characters are being received at less than two-thirds the line rate, there may be two interrupts per character.

D. Type 281-1H Reception

Reception of the start bit of the first character switches the Type 281-1H to the "busy" state. The first full character received causes a program interrupt if the Type 281-1H has been conditioned — by execution of a "Set Allow" PCB instruction — to allow interrupts. The Allow Interrupt function remains set until specifically reset by the program or by depression of INITIALIZE. In response to this interrupt, the program issues a Peripheral Data Transfer (PDT) instruction bringing that character and succeeding characters into main memory.

Reception continues until a record mark is encountered in main memory; then the read/write channel is released. If no further characters are received during a half-character period, the Type 281-1H reverts to not busy and sends an interrupt requesting output if Allow is set. This interrupt (identified by a positive response to the PCB "Output Request" query) may be utilized by the programmer to indicate the end of a received message.

When a received message occupies less than the assigned memory area, the record mark terminating data transfer is not encountered. A timer in the Type 281-1H is therefore activated and — after a specified interval — it releases the assigned read/write channel, sets the Device Error condition, and allows the Type 281-1H to revert to not busy. If Allow is set, an interrupt requesting output then occurs. When the Type 281-1H utilizes a Bell Dataset 202C operating on switched service, a disconnect is also generated by the "time-out."

E. Type 281-1H Transmission

Starting in the "initialized" condition (interrupts not allowed), the Type 281-1H may then accept an "Allow Interrupt" PCB instruction. This is followed by a PDT instruction beginning transmission of data from the central processor. Such data is transferred from the assigned memory location until a record mark is encountered; then the read/write channel is released. When the read/write channel is released and the last character goes onto the line, an interrupt occurs. A second PDT instruction continues data transmission or — if such transmission is complete — a "Reset Interrupt" PCB instruction acknowledges the interrupt and signifies the completion of transmission. An interrupt can still occur if data is received, or a "Reset Allow" PCB instruction can be given to the Type 281-1H to prevent further interrupts.

When interrupts are not allowed, testing of Input and Output Frame Demands is required.

F. Instruction Formats

1. Type 281-1H

The formats for the Type 281-1H Peripheral Data Transfer and Peripheral Control and Branch instructions are found in Section II of the bulletin Type 281-1 Single-Channel Communication Controls.

2. Type 285-1H

The formats for the Types 286/285-1H Peripheral Data Transfer and Peripheral Control and Branch instructions are found in Section VI of the bulletin Type 286-1, -2 and -3 Multi-Channel Communication Controls.

G. Record Marks and Characters in Main Memory

Since the Type 281-1H Communication Control and the Type 285-1H Communication Adapter accept any five-level code and since two memory locations are required to store character codes of more than six bits, the record mark requirements for the Type 281-1H (record marks are not required for the Type 285-1H) differ from those described in the bulletin Type 281-1 Single-Channel Communication Controls. The following description applies specifically to the Type 281-1H Communication Controls.

1. Record Marks Required by Five-Bit or Six-Bit Code Applications

a. Single-Character Mode

In the single-character transmission mode, a record mark is placed in memory location A+1 to terminate a character; in the single-character reception mode, a record mark in location A terminates the character.

b. Block — or Message — Mode

In the block transmission mode, a record mark is placed in memory location A+n (where n is the number of characters) to terminate a message; in the block reception mode, a record mark in memory location A+(n-1) terminates the message.

2. Record Marks Required by Seven-Bit or Eight-Bit Code Applications

a. Single-Character Mode

In the single-character transmission mode, a record mark is placed in memory location A+2 to terminate a character; in the single-character reception mode, a record mark in location A+1 terminates the character.

b. Block — or Message — Mode

In the block transmission mode, a record mark is placed in memory location A+2n to terminate a message; in the block reception mode, a record mark in location A+(2n-1) terminates the message.

3. Character Configuration in Memory

Figure 3, page 9, shows the layout of the code bits in memory for five- through eight-level codes (B1 to B8 represent the DATAspeed bits).

	8	7	6	5	4	3	2	1	BIT POSITION

5-BIT CODE — MEMORY LOCATION

Series 200 RECEIVING	IM	WM	B5	B4	B3	B2	B1	∅	A
									A + 1
Series 200 SENDING			B5	B4	B3	B2	B1	∅	A
	IM	WM							A + 1

6-BIT CODE

Series 200 RECEIVING	IM	WM	B5	B4	B3	B2	B1	B6	A
									A + 1
Series 200 SENDING			B5	B4	B3	B2	B1	B6	A
	IM	WM							A + 1

7-BIT CODE

Series 200 RECEIVING			∅	∅	∅	∅	∅	B7	A
	IM	WM	B6	B5	B4	B3	B2	B1	A + 1
Series 200 SENDING			∅	∅	∅	∅	∅	B7	A
			B6	B5	B4	B3	B2	B1	A + 1
	IM	WM							A + 2

8-BIT CODE

Series 200 RECEIVING	∅	∅	∅	∅	∅	∅	*∅	B7	A
	IM	WM	B6	B5	B4	B3	B2	B1	A + 1
Series 200 SENDING			∅	∅	∅	∅	∅	B7	A
			B6	B5	B4	B3	B2	B1	A + 1
	IM	WM							A + 2

IM = Item Mark
WM = Word Mark
IM + WM = Record Mark
Bn = Code Bit

*If hardware parity checking is used, then the eighth bit is not sent from the control unit to the central processor memory. If the hardware parity checking is not used, then the eighth bit appears in this position.

Figure 3. Character Configuration in Type 281-1H Memory

H. Program Timing

In Type 281-1H programming, the program must refill or empty the shift register during the time interval of a stop bit (952 microseconds). In the case of the Type 285-1H, the program has a full character time interval (9.52 milliseconds) in which to transfer a character to the central processor or from it.

If received data is not taken from the shift register of the Type 281-1H or Type 285-1H within the specified time, data is lost. In this event, the Error function is set in the Type 281-1H, or an error indication is stored in the Type 286.

When the central processor is transmitting data, the Type 281-1H Communication Control waits if a new character for transmission is not received within the specified time. In the case of the Type 285-1H, however, the Type 286 repeats the last character transmitted unless a "Transmit Last Character" PDT instruction is issued by the program.

During operation of the Type 281-1H in the single-character mode, data being sent into main memory for storage requires a time interval of at least 11 memory cycles after the instruction is completed. Data being transferred to the Type 281-1H by an "Output" PDT instruction cannot be changed until 14 memory cycles after extraction of the instruction.

I. Series 200 and Type 281-1H Interface Signals

1. Single-Character Transmission

During single-character transmission between the Type 281-1H and the Series 200 central processor, the following interface signals occur.

a. Device Busy

This Busy signal indicates that a PDT instruction cannot be accepted by the control unit. Busy is active whenever the read/write channel associated with a PDT instruction addressed to the control unit is busy or when the control unit is receiving or transmitting data on the line.

b. Interrupt

Activation of INTERRUPT indicates that the control unit is requesting service. INTERRUPT responds to the first "Set Allow" PCB instruction when the control unit is "initialized"; thereafter, it responds only when an Input or Output Frame Demand becomes active. The communication control Interrupt signal is reset when a PDT instruction is sent to the unit, when a "Turn Off Interrupt" PCB instruction is sent to the unit, or when the system is "initialized."

c. Input Frame Demand (IFD)

The IFD signal indicates that the communication control - having assembled a character from the line and readied it for the computer - is requesting a "Receive" PDT instruction. The next PDT instruction to the communication control resets the IFD signal; if no further PDT instruction is executed, the IFD signal is not reset.

d. Output Frame Demand (OFD)

The OFD signal indicates that the communication control is capable of accepting a "Transmit" PDT instruction. This signal may be actuated when the communication control is neither transmitting nor receiving, and when the IFD signal is inactive.

The Output Frame Demand, then, becomes active in the transmit mode when the communication control is ready to transmit the next character. In the receive mode, after a one-half character duration of inactivity on the line, and after a PDT instruction has reset the IFD signal, the Output Frame Demand becomes active.

The OFD signal is reset by a "Transmit" or "Receive" PDT instruction, or when the communication control senses a character on the line.

e. Timing Error

The Timing Error signal indicates the loss of a control-unit data character. In the receive mode, the signal is set when a "Receive" PDT instruction does not respond to an Input Frame Demand before the next character is sensed on the line.

Timing Error is reset when the next PDT instruction is issued to the communication control.

f. Parity Error

The Parity Error signal is associated only with the receive mode. The signal is set - if the communication control is capable of checking parity - by a character demonstrating bad parity when the Input Frame Demand becomes active. Parity Error is reset by the next PDT instruction issued to the communication control.

g. Turn Off Interrupt

The "Turn Off Interrupt" PCB instruction permits the effectiveness of a Resume Normal Mode (RNM) instruction without executing a PDT instruction to the communication control.

h. Reset Allow

The "Reset Allow" PCB instruction prevents future interrupts from the communication control. A current interrupt is not reset by this PCB instruction; either a "Turn Off Interrupt" PCB instruction or a PDT instruction is needed to render an RNM instruction effective.

2. Single-Character Timing Considerations

a. Set Allow

The timing of the interrupt responding to the "Set Allow" PCB instruction is unpredictable.

b. Received Data

Data offered in response to a "Receive" PDT instruction is entered into main memory within eleven memory cycles after the extraction of the PDT instruction.

c. Transmitted Data

Data in main memory which is to be transferred by a "Transmit" PDT instruction cannot be exchanged until fourteen main memory cycles are completed after the extraction of that instruction.

NOTE

The read/write channel is busy until all the data is transferred. The control unit is busy two main memory cycles longer than the read/write channel.

3. Block-Method Transmission

During the block method of transmission between the Type 281-1H and the Series 200 central processor, the following interface signals occur.

a. Input Frame Demand

The IFD signal is activated when the communication control has assembled the first block (message) character from the line for transfer to the computer. This signal is reset by a PDT instruction and not activated again by a character on the line until the assigned RWC is released. Such a release is accomplished either by the sensing of a record mark in memory or by a line inactivity period of approximately 30 seconds.

b. Output Frame Demand

The OFD signal is activated in the transmit mode when the communication control is ready to transmit a block. In the receive mode, the OFD signal becomes active after a line inactivity period of one-half a character time, providing the RWC has been released. If the RWC has not been released, an inactivity period of 30 seconds elapses before the release is effective and the OFD signal is activated.

c. Timing Error

In the receive mode, Timing Error is set when the communication control releases the RWC after the 30-second period of inactivity described in paragraph b, above.

VII. OPERATIONAL CONTROLS

Calls are originated manually, either from the central processor or from the remote terminal station. An operator at either end initiates a data connection as a telephone connection, establishing voice communication and agreement on procedure. Then both operators depress DATA on their Bell DATA-PHONE Datasets 202, placing the line in the data transmission mode.

Optional features include these possibilities:

1. Automatic answer at the remote terminal;

2. Automatic answer at the computer station;

3. Automatic call initiation from the computer by means of a Bell DATA-PHONE Dataset 801A or 801C and a Honeywell Type 285-5A Communication Adapter.

VIII. OPTIONAL FEATURES

No checking options are available for the Types 281-1H and 285-1H. Bell remote equipment performs neither a parity nor a longitudinal redundancy check on data received from the central processor. Furthermore, Bell remote equipment lacks the rereading capability necessary to utilize a parity or long check indication detected by the Series 200 central processor.

IX. MAINTENANCE FACILITIES

The Types 281-1H and 285-1H have no maintenance panel, indicator lights or switches.

HONEYWELL EDP TECHNICAL PUBLICATIONS
USERS' REMARKS FORM

TITLE: SERIES 200 TYPE 281-1H COMMUNICATION CONTROL AND TYPE 285-1H COMMUNICATION ADAPTER HARDWARE BULLETIN

DATED: APRIL, 1966

FILE NO: 112.0005.1100.0-092

ERRORS NOTED:

Fold

Cut Along Line

SUGGESTIONS FOR IMPROVEMENT:

Fold

FROM: NAME _____ DATE _____

COMPANY _____

TITLE _____

ADDRESS _____

_____

FIRST CLASS
PERMIT NO. 39531
WELLESLEY HILLS
MASS.

BUSINESS REPLY MAIL

No postage stamp necessary if mailed in the United States

POSTAGE WILL BE PAID BY

HONEYWELL
ELECTRONIC DATA PROCESSING DIVISION
60 WALNUT STREET
WELLESLEY HILLS, MASS. 02181

ATT'N: TECHNICAL COMMUNICATIONS DEPARTMENT

Cut Along Line

Honeywell
ELECTRONIC DATA PROCESSING