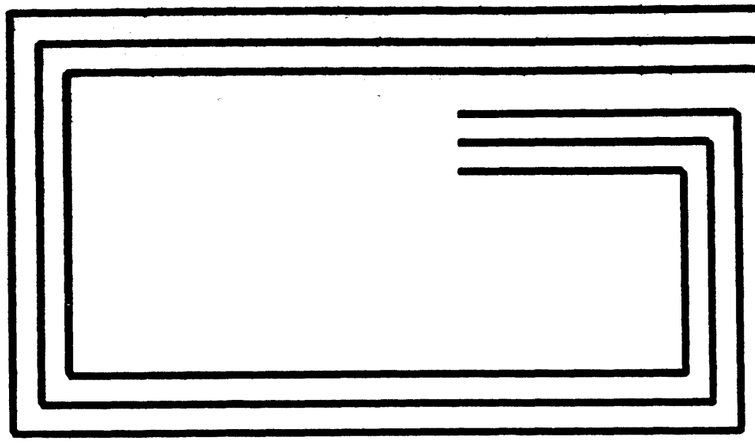
Honeywell



UNIT RECORD CONTROLLER

OPTIONS INSTALLATION MANUAL

WEUR001/2/5/6/7A

58010073

HONEYWELL CONFIDENTIAL & PROPRIETARY

58010073-500
DIST. NCO, XAN

REV B
OCTOBER 1984

Honeywell HONEYWELL INFORMATION SYSTEMS		DWG. NO. 58058443	SHEET 1/28	REV J
LOC. PHOENIX,ARIZONA	DISTR C127-7B	PROJECTION	CODE	
	DATA BASE T058443 D058443			
PREPARED BY DATE W M H Reed	TITLE		F.C.F.: OP.LST:N/A	
APPROVED BY 81FEB12 C.E. WILCOX 81FEB12	EMBEDDED UNIT RECORD CONTROLLER OPTIONS INSTALLATION INSTRUCTION			

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	LEVEL 3 ISSUE	81FEB12	SEE APERTURE CARD	1 THRU 25F
B	PHA0DP002	81MAY20	C R NOWLAND	1 THRU 26F
C	PHA0DP005	81JUL8	T GUILFORD	1 THRU 26F
D	PHA0DP020	82APR2	T. GUILFORD	1 THRU 30F
E	PHA0GD457	82NOV03	B. JAMES	1 THRU 30F
F	PHA0DP044	83NOV01	J. KNOBLACH	1 THRU 28F
G	PHA0DP053	84JAN10	N. BEHIE	1 THRU 28F
H	PHA0DP060	84SEPT07	A. WEST	1 THRU 28F
J	PHA0DP061	85JULY24	AL BYKOFSKY	1 THRU 28F

TABLE OF CONTENTS

The following notice is provided in accordance with the United States Federal Communications Commission's (FCC) regulations:

Warning: This equipment generates, uses, and can radiate radio frequency energy, and if not installed and used in accordance with the instruction manual, may cause interference to radio communications. The equipment manufactured after October 1,1983 has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

RECORD OF REVISION			
REV	DATE	AUTHORIZATION	PAGES AFFECTED
A	1/84	PHAFBE908	58010073-002,1F 58010073-031,1F 58010073-500 58010073-014,1F 58010073-530,1F 58010073-015,1-1F 58010073-051,2-1F 58010073-800,1F 58010073-900,1F 58010073-101,1F 58010073-102,1F 58010073-103,1F 58010073-104,1F
B	10/84	PHAFBE909	58010073-002,1F 58010073-031,1F 58010073-500 58010073-011,1F 58010073-014,1F 58010073-530,1F 58010073-800,1F 58010073-105,1F 58010073-900,1F

RECORD OF REVISION			
REV	DATE	AUTHORIZATION	PAGES AFFECTED

TABLE OF CONTENTS
OPTIONS MANUAL
UNIT RECORD PROCESSOR WEUR001/2/5/6/7A

REV B

(a) Option packages included only when called for on the Equipment Requisition.

1.0 GENERAL

1.1 INTRODUCTION

This section contains an introduction to the WEUR00XA Unit Record Controller Options Manual describing the scope, purpose, and makeup of the manual.

1.1.1 SCOPE

This options manual is designed as part of the Product Maintenance Documentation (PMD) for the Honeywell Series WEUR00XA Unit Record Controllers. The manual is primarily for use by the Customer Service Division (CSD) specialists and the LCPD Manufacturing specialists. The manual is Honeywell Confidential & Proprietary and is divided into sections separated by tabs.

1.1.1.1 GENERAL TAB

This section contains the introductory material.

1.1.1.2 PHYSICAL OUTLINE TAB

This section shows the location of the options installed in the various IOM/IOUs of the Level 66/DPS 8 Systems.

1.1.1.3 THEORY OF OPERATION

This section contains an operational description of the EUR controller options.

1.1.1.4 WIRE LISTS TAB

This section contains the MICROFICHE INDEX which lists the logic wire lists that are contained on Microfiche cards located in the Microfiche card box.

1.1.1.5 CKT/LOGIC TAB

This section contains the logic block diagram (LBD), the revision status sheet (RSS), and the component installation list (CIL) for the options circuit board.

1.1.1.6 PARTS TAB

This section contains drawings, parts lists, and schematics of the options components.

1.1.1.7 OPTIONS TAB

This section contains the Installation Kits and instructions for each of the EUR options.

1.1.2 PURPOSE

This manual is a reference document which supplies information to aid CSD instructors and students in training on the EUR controller and for CSD installation and maintenance of the EUR controller in the field.

1.1.2.1 CSD TRAINING

This manual can be used by CSD instructors to prepare lesson plans and by students in the classroom as their primary text. The student should become familiar with and be able to effectively use this manual even if the student is supported with additional material (handouts) by the instructor.

1.1.2.2 CSD FIELD INSTALLATION AND MAINTENANCE

This manual is for use by CSD trained specialists for installation and maintenance of the EUR controller at customer sites to isolate failures not found by T&D ORU callout and replacement.

1.1.2.3 CSD TECHNICAL ASSISTANCE CENTER (TAC)

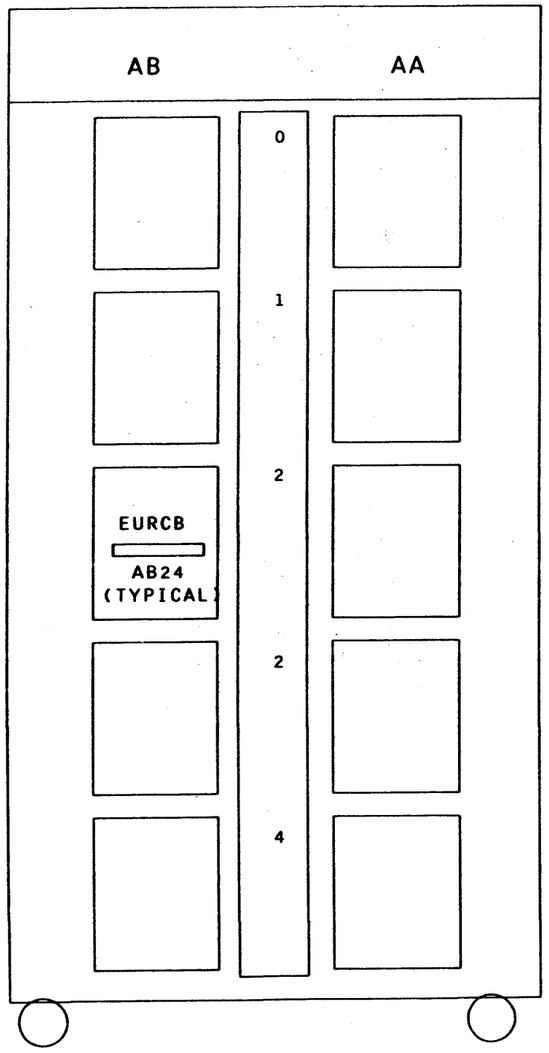
This manual can be used for remote support of field sites. It should be part of a primary reference library for use by TAC specialists in contact with a CSD specialist or a maintenance computer at a customer site.

1.2 FEEDBACK

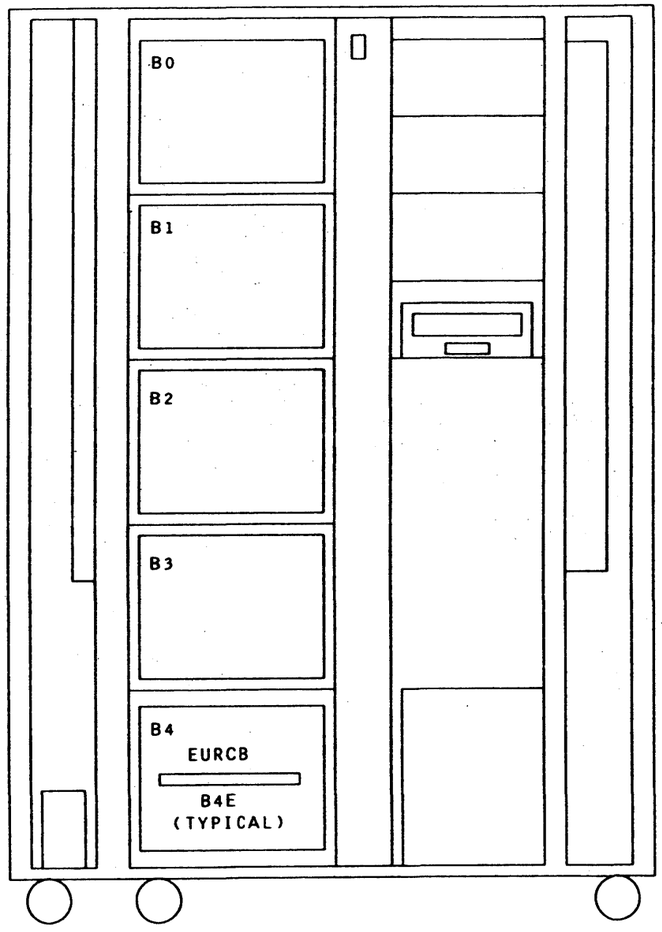
Send any comments on this manual to Honeywell Large Systems Product Support, P.O. Box 8000, MS K92, Phoenix, AZ 85066.

NOTE: PERIPHERAL CONTROLLER OPTIONS ARE INSTALLED IN THE CARD MODULE SLOTS ACCORDING TO THE FOLLOWING PRIORITIES (REF: INSTALLATION INSTRUCTION 58058443).
HIGHEST = MAG TAPE
NEXT = DISK
NEXT = EURC
LOWEST = CONSOLE

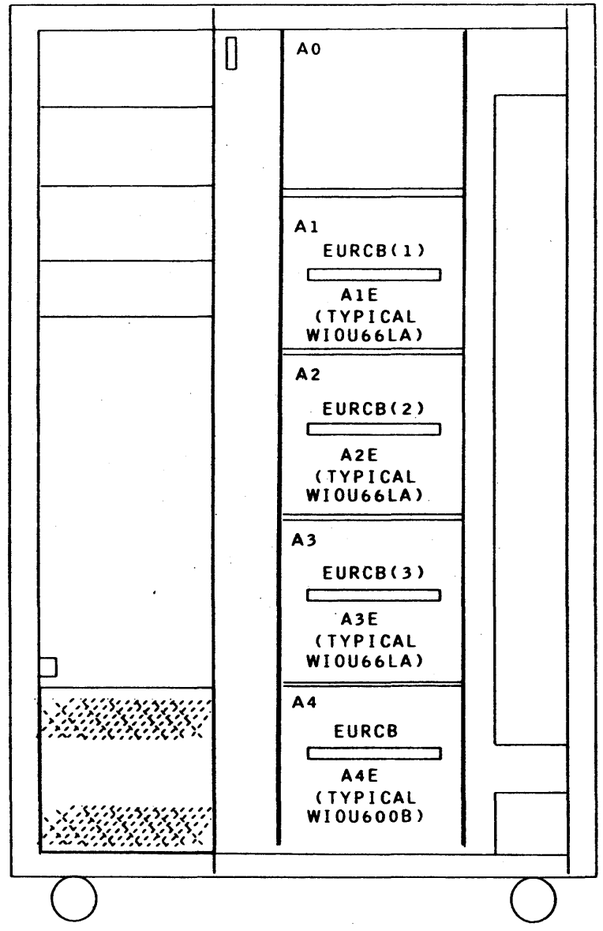
4WDC8134/8634
4WCSM001/601



WIOU600A



WIOU66LA
WIOU600B



FRONT VIEW (EXTERNAL DOORS NOT SHOWN)

FIGURE 2-1. UNIT RECORD CONTROLLER OPTIONS WEUR001/2/5/6A

Honeywell

UNIT RECORD CONTROLLER

WEUR001/2/5/6/7A

OPERATIONAL DESCRIPTION

58009986

LVL66/DPS 8

58009986-040
DIST NCO, XAN

HONEYWELL CONFIDENTIAL & PROPRIETARY

REV D
JANUARY 1985

APPENDIX A - PRT0901/PRT1201

TABLE OF CONTENTS

UNIT RECORD CONTROLLER

WEUR001/2/5/6/7A

OPERATIONAL DESCRIPTION

58009986

LVL66/DPS 8

58009986-040
DIST NCO, XAN

REV D
JANUARY 1985

RECORD OF REVISION			
REV	DATE	AUTHORIZATION	PAGES AFFECTED
A ISSUED	September 1981	PHAFPV975	58009986-040 58009986-014, 1F 58009986-017,1,2F 58009986, 1 thru 23F 58009986, A-1 thru A-3F 58009986, B-1F
B	1/84	PHAFBE908	58009986-040 58009986-014, 1F 58009986, 1,2,3
C	10/84	PHAFBE909	58009986-040 58009986-014,1F 58009986, 1,14
D	1/85	PHAFBE910	58009986-040 58009986-014,1F 58009986, 1,14,15

RECORD OF REVISION			
REV	DATE	AUTHORIZATION	PAGES AFFECTED

OPERATION DESCRIPTION

TABLE OF CONTENTS

APPENDIX A - PRT0901/PRT1201

TABLE OF CONTENTS

1.0 GENERAL DESCRIPTION

1.1 GENERAL CHARACTERISTICS

The Unit Record Controller (URC) is a one board microprocessor subsystem, EURCB, which is embedded in the I/O cabinet of the Central System. The EURCB interfaces with the Central System via the IOM bus. Two device adapter interface (DAI) ports are available for connecting card reader and card punch devices and PR71 printers. Also two peripheral device serial interface (PDSI) ports are available for connecting PR54 printers (see Figure 1.1).

1.2 PHYSICAL CONFIGURATION

The EURCB board is an option which can be installed in several I/O cabinets as follows (ref: Installation Instructions 58058443):

- 4WDC8134AA Input Output Multiplexer
- 4WDC8634BA Input Output Multiplexer
- 4WCSM001AA Integrated Control Unit
- 4WCSM601BA Integrated Control Unit
- WIOU600A/B Input Output Units
- WIOU66LA Input Output Unit

Programmable read only memories (PROMS) containing unit record device application firmware are installed on the EURCB board to provide the option of operating with specific unit record devices as follows:

- WEUR001 PROM A Option (card readers and card punches on the DAI and PR54 printers on the PDSI under GCOS).
- WEUR002A PROM B Option (PR71 printers on the DAI under GCOS).
- WEUR006A PROM C Option (same as PROM A except under CP6).
- WEUR007A PROM D Option (same as PROM A except WWMCCS/Air Force Card Option).
- WEUR005A Initialize Option (provides a local pushbutton switch to initialize the URC).

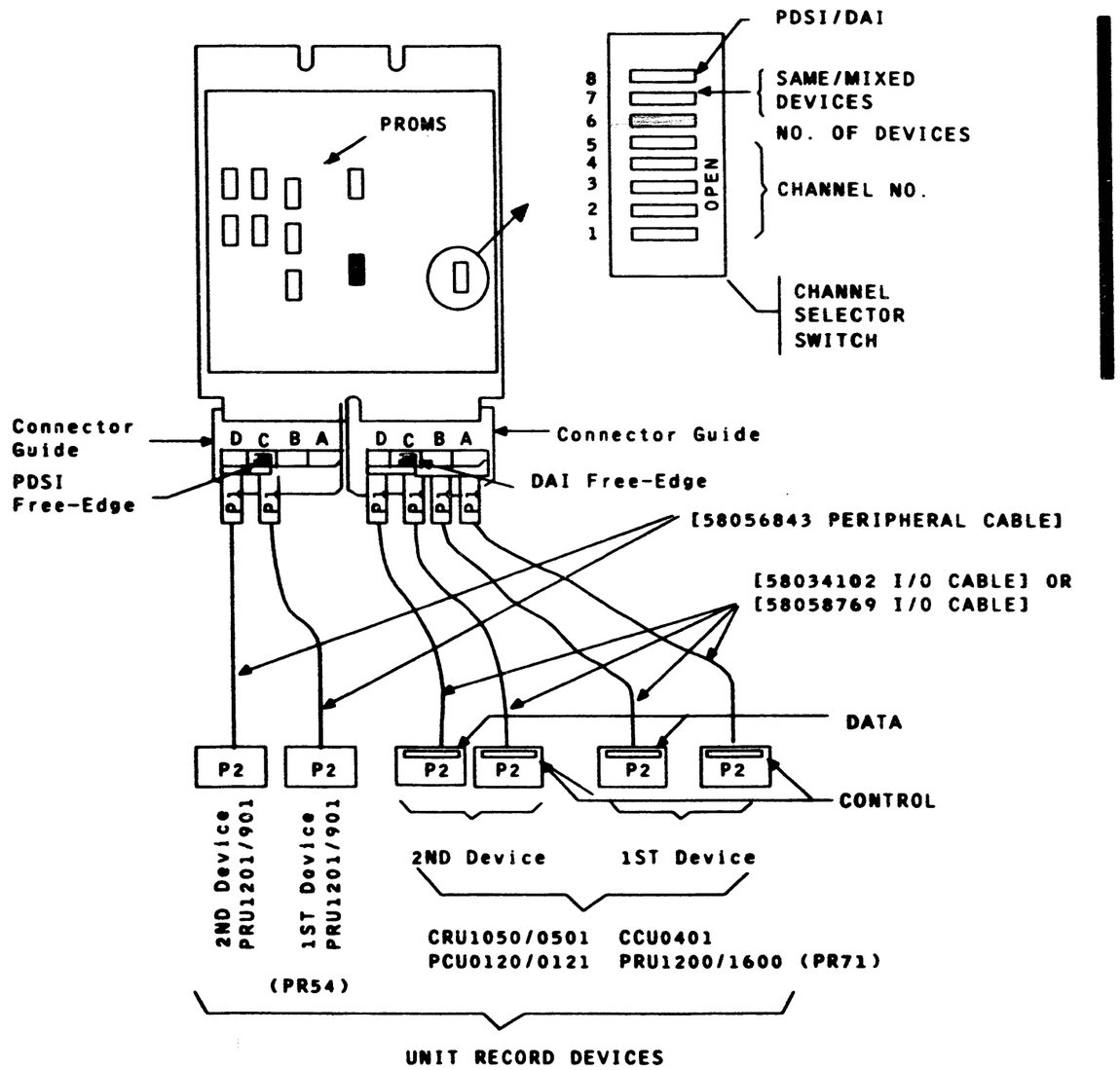


FIGURE 1.1. EURCB BOARD INTERFACES

2.0 BASIC DESCRIPTION OF OPERATION

2.1 HARDWARE OVERVIEW

The EURCB board contains the microprocessor subsystem, the IOM interface, the device adapter interface(DAI), and the peripheral device serial interface(PDSI)(see Figure 2.1). Included on the left free edge of the EURCB board are red and green light emitting diodes(LEDs) for displaying failure or passage of self tests.

2.1.1 Microprocessor Subsystem

The microprocessor subsystem uses a 5Mhz, 8-bit external, 16-bit internal microprocessor chip plus many programmable chips which include the interval timer, interrupt controller buses, and peripheral interfaces. Three data buses are associated with the microprocessor subsystem: a local bus which consists of the multiplexed address/data bus, and two remote buses (implemented through transceivers) that demultiplex the address/data bus into a data bus. For a detailed description of the microprocessor subsystem, see Section 3.1.1.

2.1.2 IOM Interface

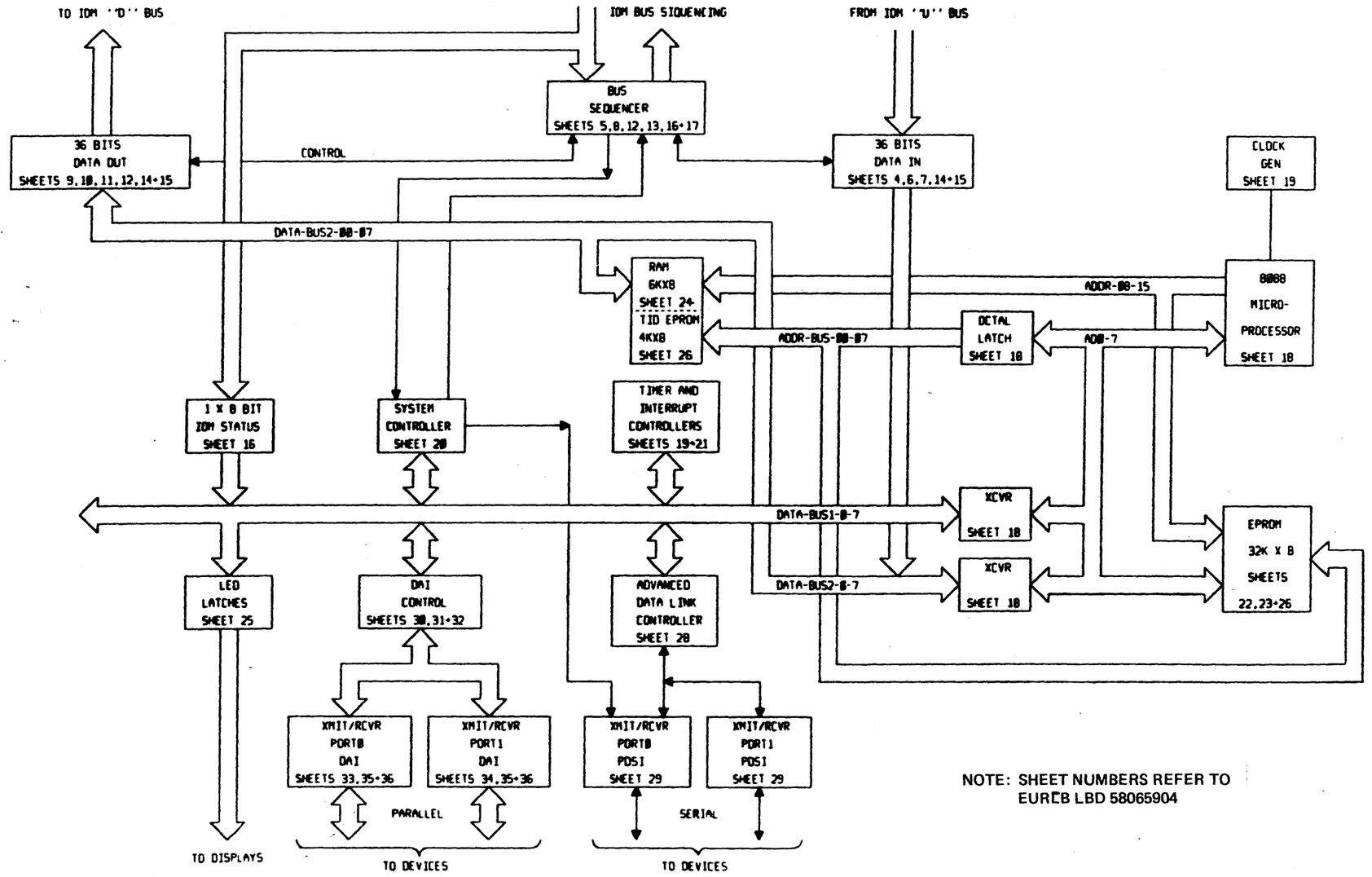
The IOM interface consists of field programmable logic array(FPLA) chips. The interface is double precision in that two words of data can be loaded or stored to or from the IOM. For a detailed description of the IOM interface, see Section 3.1.2.

2.1.3 Device Adapter Interface(DAI)

The DAI is a parallel interface which handles eight bi-directional bits of data plus parity and 12 control signals consisting of five outputs and seven inputs. The DAI connects to the right free edge of the EURCB board (see Figure 1.1).

2.1.4 Peripheral Device Serial Interface(PDSI)

The PDSI is a serial interface consisting of two serial data lines plus two clock lines. The PDSI connects to the left free edge of the EURCB board (see Figure 1.1). For a detailed description of the PDSI, see Section 3.1.3.



NOTE: SHEET NUMBERS REFER TO EURCB LBD 58065904

FIGURE 2.1. LOGIC DIAGRAM – EURCB BLOCK DIAGRAM

2.2 FIRMWARE OVERVIEW

Introduction

The EURC FW design utilizes a layered architecture. The implementation of a layer is designated as a module. Each module is intended to be independent of the other module, or free standing. The modules communicate with one another via a queued interface. An independent set of queues exists between the modules for each logical channel.

Queuing Mechanism

The queue mechanism consists of a set of 20 circular queues, support procedures to enter messages into the queues, and a dispatchery procedure which monitors the queues and delivers messages to the appropriate modules. The ordering of the queues establishes the priority between competing modules and logical channels. Section XXX describes the data structuralized for queueing the support procedures.

Logical Modularity

The firmware is divided into several logical modules, each of which is designed to perform a specific set of functions. The modules can be subdivided into 3 sets. The first set consists of the CORE module. The function of the core module is to serve as the basic operating system for the controller. The second set includes the following modules: IOM, SCC, LINK. The functions performed by these modules is to interface to the IOM, process special controller commands, and control the PDSI respectively. These first 2 sets together comprise the common firmware. The third set is the application modules. These modules are described in the appropriate device appendix.

Physical Modularity

The logical modules are supported by physical modularity. Each logical module is assigned a set of proms at a specific physical memory address. All communications with a module are done through a jump table located at the beginning of the physical module. The physical modularity allows a firmware change to be made to a logical module with minimum changes to the total prom set.

2.3 FUNCTIONAL OVERVIEW

3.0 DETAILED DESCRIPTION OF OPERATION

3.1 HARDWARE DESCRIPTION

3.1.1 Microprocessor Circuitry

The microprocessor subsystem consists of programmable LSI components, 6K bytes of RAM, 36K bytes of EPROM including self-test, address latch, data transceivers, clock generator and other MSI/SSI components. One-third of the board is taken up by this circuitry and it not only serves as a control mechanism but also handles, interprets and formats data from either the IO system or the peripheral device. Refer to Figure 3.1.1.1.

3.1.1.1 Microprocessor

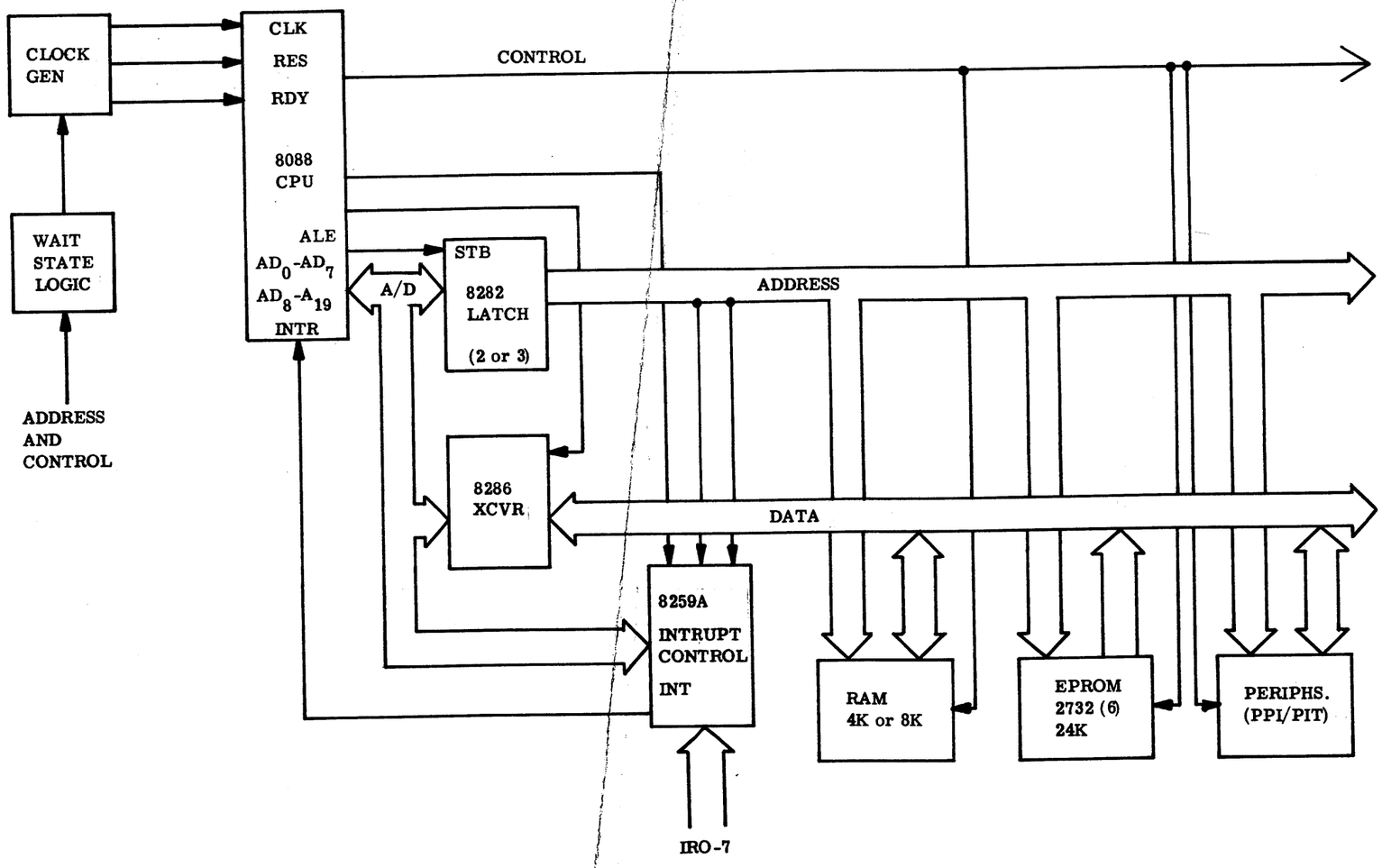
The microprocessor has an 8-bit external/16-bit internal architecture. The clock rate used is 5MHZ which means a typical instruction of 4T would take 800 nanoseconds. The microprocessor is a Honeywell 2V-688 which is compatible with the Intel 8088. It has two modes of operation consisting of a minimum and maximum mode. The micro on the EURC operates in the minimum mode.

The configuration of the microprocessor and the surrounding components are shown in Figure 3.1.1.1.1. Refer to Figure 2.1.1 for a total overview of other devices the microprocessor drives.

3.1.1.1.1 Local Bus

The multiplexed address/data lines are considered the local bus. An address latch has the local bus as an input and on the microprocessor ALE signal the input is latched and present on the output to form the ADDR-BUS bits 0-7 which makes up the least significant byte with bit 7 being the most significant. The upper 8-bits of the address bus, ADDR-BUS bits 8-15, are present throughout the micro instruction so they need not be latched as the lower order address lines need to be.

Figure 3.1.1.1.1 shows the two transceivers that reside on the 8-bit multiplexed address-data bus to form two separate data busses. The bi-directional output of one transceiver is called DATA-BUS1 and the other is called DATA-BUS2. The transceivers allow data to come in to or go out from the local bus.



MICROPROCESSOR SUBSYSTEM

FIGURE 3.1.1.1

Read-only memory is also located on the local bus. Eight EPROMs are on this bus not including the self-test EPROM. Board test chips are placed on this bus so visibility can be given to the board tester.

3.1.1.2 DATA-BUS 1

Located on this bus are many of the programmable LSI components. Two programmable peripheral interface chips, programmable interval timer, and programmable interrupt controller. The programmable serial chip for the PDSI is also on this bus. Other components are LED registers, an IOM status register and some registers that allow the EURC to read and write the IO system.

3.1.1.3 DATA-BUS 2

The 6K bytes of RAM and 4K bytes of self-test EPROM are located on this bus. Most all of the IO system data input registers and data output registers are located on DATA-BUS 2.

3.1.1.4 Memory

The memory map for the EURC is shown in Figure 3.1.1.4.1.

Random access memory consists of 3 chips with a 2K X 8 bit density. Read-only memory consists of 9 chips for the PDSI/DAI option and 8 chips for the DAI printer option. Density of these EPROMs is 4K X 8 bits per chip. The EPROMs are socketed for easy updates and easy chip replacement for failed components.

3.1.1.5 Input-Output

The I/O map for the EURC is shown in Figure 3.1.1.5.1A and 3.1.1.5.1B -- refer to it throughout this section.

Basically the I/O is set up in three sections. The first section being read/write type devices that are part of the microprocessor family of components. These components range from I/O ports 040H to 063H.

The next section is all write type of registers that are a functional part of the IO system interface. Ports 080H to 085H are the registers that store the first data word that gets sent to the I/O system. I/O ports 088H to 08DH are the registers that store the second word of data that gets sent to the I/O system. Finally I/O ports 090H to 095H are the registers that store the transaction command that gets sent to the I/O system. Service request is a write function done by the microprocessor which sets the request, CHAN*REQ*001, to signal the I/O system.

The last section is essentially all read type registers. At ports 098H through 09BH four 8-bit address extension registers reside. The data present in these registers is sent by the I/O system and located in the register based on the channel number also sent by the I/O system. Ports 0A0H to 0A3H and 0A8H to 0ABH are the locations where ASCII data from the I/O system can be found when the U-BUS-BCD bit is reset. Ports 0A0H to 0A5H and 0A7H to 0ADH when the U-BUS-BCD is set contain BCD data from the I/O system. The lower address string contains the first word of a double precision store or a don't care based on the previous transaction command. The upper address string contains the likewise based on the previously sent transaction command. Port address 0A7H with the U-BUS-BCD bit

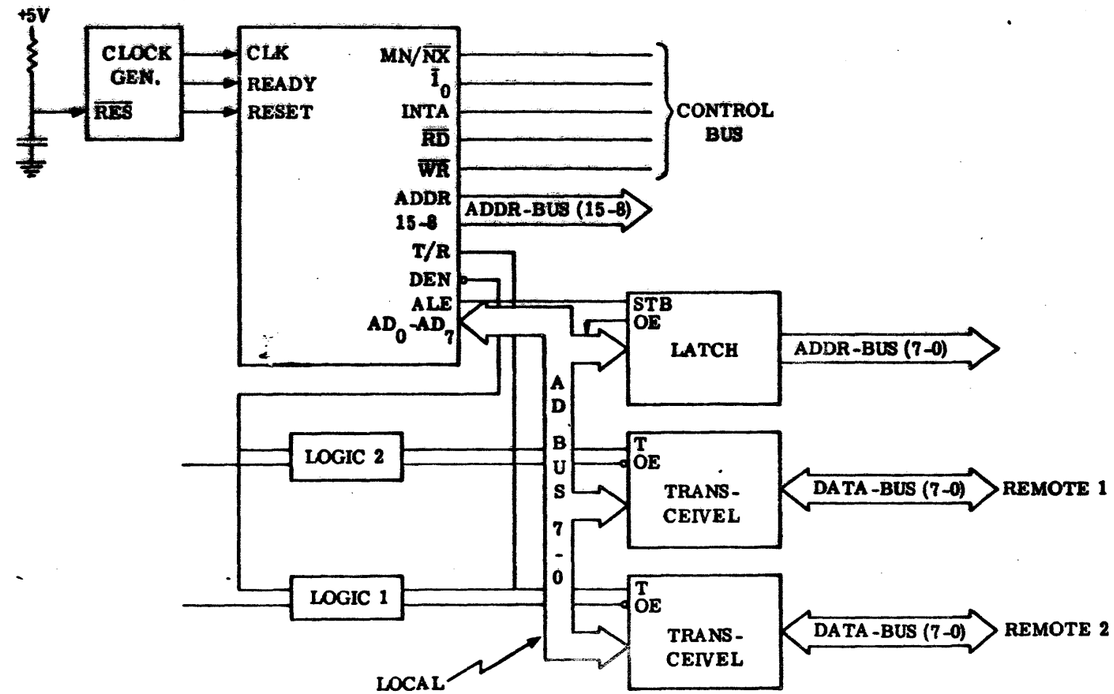


FIGURE 3.1.2-1 MICROPROCESSOR BUSES

FIGURE 3.1.1.1.1

MEMORY MAP:

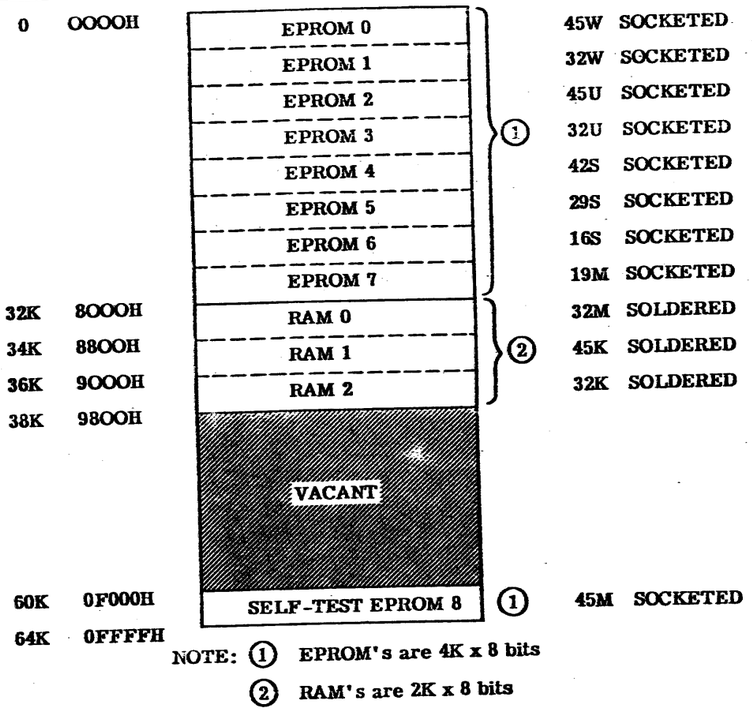


FIGURE 3.1.1.4.1

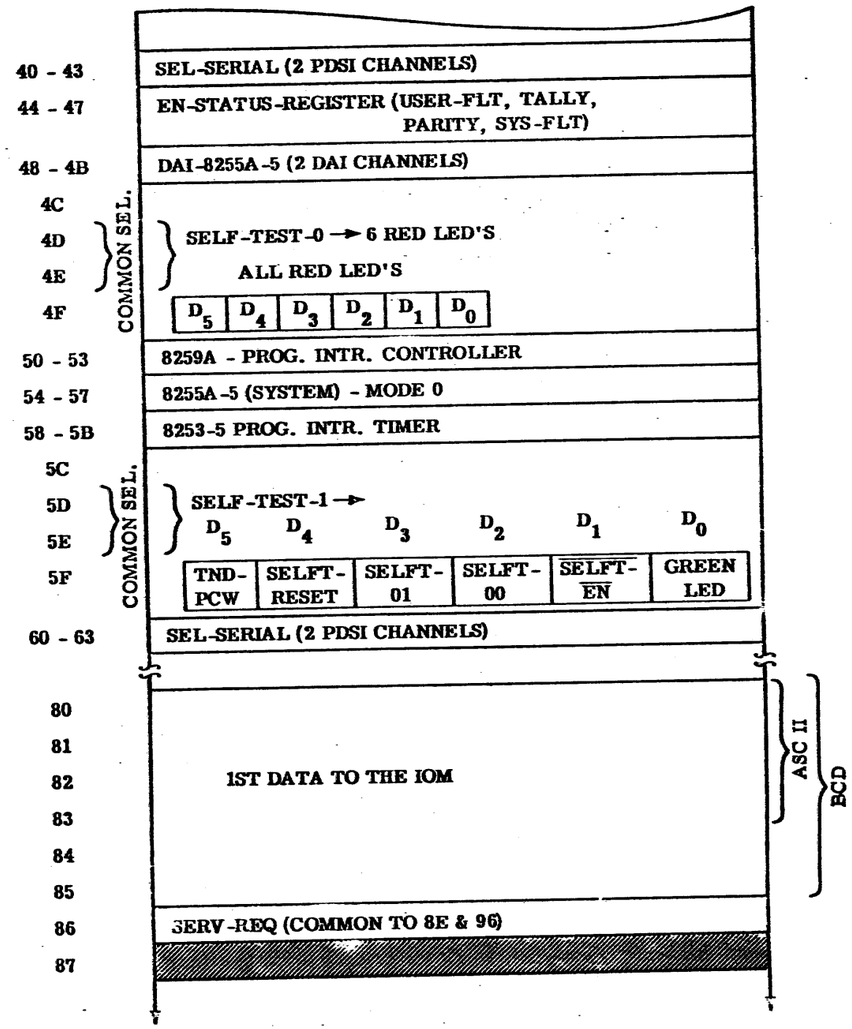


FIGURE 3.1.1.5.1.A

set is where the description of the configuration switch is read. Other I/O ports can be thought of as just self-test useful. They are just wrap paths for better visiblity. One bit in the register at port 05CH, SELFT-RESET*100, will reset the EURC hardware not including the microprocessor and the two programmable peripheral interface chips.

The formats in Figure 3.1.1.5.2 show what the microprocessor must read or write in relation to the previous description of the I/O.

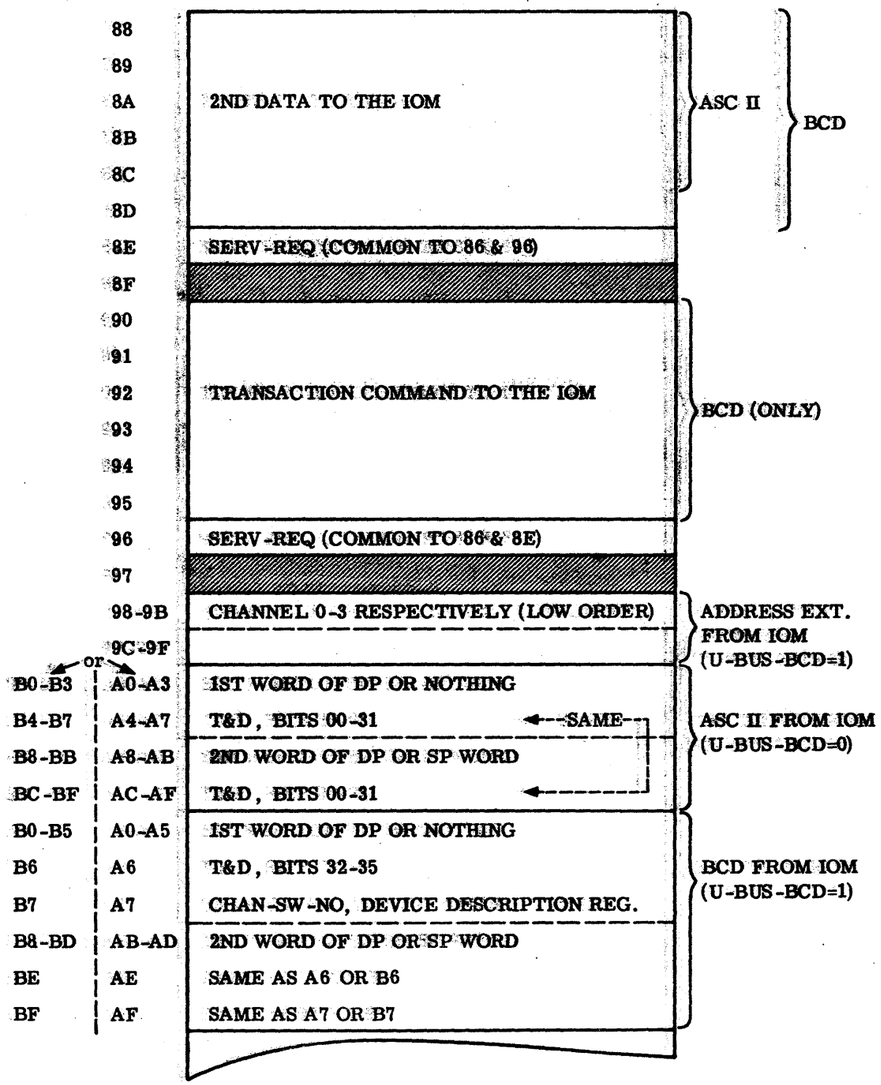


FIGURE 3.1.1.5.1.B

FORMATS:

A) SYSTEM-8255A-5 MODE 0 A-INPUT, B-OUTPUT, C-OUTPUT

LOC	7	6	5	4	3	2	1	0	
54_H	PARITY-ERR-FLG;000	MDAI-OPI;100	DAI-TD0;100	DAI-TD1;100	PCW-ACK-D;100	PCW-ACK-C;100	PCW-ACK-B;100	PCW-ACK-A;100	(A)
55_H	TD-YANK-UP;100	U-BUS-BCD;100	D-BUS-BCD;100		PCW-CLR-D;000	PCW-CLR-C;000	PCW-CLR-B;000	PCW-CLR-A;000	(B)
56_H	E-TND-RCVR-1;100	E-TND-RCVR-0;100	E-RS422 RCVR-1;100	E-RS422 RCVR-0;100	E-TND-DRVR-1;100	E-TND-DRVR-0;100	E-RS422 DRVR-1;100	E-RS422 DRVR-0;100	(C)

NOTE: T&D BITS A_7, A_5, A_4, B_7, C_7, C_6, C_5

B) DAI-8255A-5 MODE 2 A-BI-DIRECT, B-OUTPUT, C_L-INPUT, C_H-CNTL

LOC	7	6	5	4	3	2	1	0	
48_H	MDAI-DAT-7;100	MDAI-DAT-6;100	MDAI-DAT-5;100	MDAI-DAT-4;100	MDAI-DAT-3;100	MDAI-DAT-2;100	MDAI-DAT-1;100	MDAI-DAT-0;100	(A)
49_H	TND-PAR-DAI;100	TND-C/DSI-CONTL;100	TND-DAI-INTR;100	MDAI-RSO;100	MDAI-OPO*000	MDAI-OPO*010	MUX-DAI-SEL;100	RST-DAI;100	(B)
$4A_H$	OBF;000	ACK>;001	IBF;100	STB>600;001	INTR;000	MDAI-EV3-LATCH;101	MDAI-PARITY-ERR;100	TMO-B;100	(C)

C) INTR CONTROLLER-8259A

LOC	IR_7	IR_6	IR_5	IR_4	IR_3	IR_2	IR_1	IR_0	
50_H, 51_H	TIMEOUT-2;101	TIMEOUT-1;101	TIMEOUT-0;101	ENDAI-EV2-P1;101	ENDAI-EV2-P0;100	IRQ-ADLC;101	ENDAI-EV1-P1;101	ENDAI-EV1-P0;101	IRW

D) STATUS REGISTER

LOC	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
86, 8E, 96	CHAN-REG FF;000	PARITY-ERR-FLG;100	SYS-FAULT-;101	USER-FLT-00;101	USER-FLT-01;101	USER-FLT-02;101	TALLY-BIT-0;100	TALLY-BIT-1;100

TERM-SERV-VALID

FORMATS: (CONT'D)

E) ADDR EXTENTION REG FILE

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOCATION
U-BUS-21;100	IRQ-CONBUSY;101	U-BUS-12;000	U-BUS-13;000	U-BUS-14;000	U-BUS-15;000	U-BUS-16/22;000	U-BUS-17/23;000	98,99,9A,9B & U-BUS-BCD=1

MASK — PCW CONNECT WHILE BUSY — ADDR-EXT-BITS

F) BASE CHANNEL NO. REG AND FREE-EDGE DESCRIPTION

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOCATION
CHAN-SW-00;000	CHAN-SW-01;000	CHAN-SW-02;000	CHAN-SW-03;000	CHAN-SW-04;000	4-CHAN-SEL;000	SAME/MIXED;000	PDSI/DAI;000	A7,AF,B7,BF & U-BUS-BCD=1
SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	

BASE CHANNEL NO. OF EUBC (SWITCH SETTINGS) — DEVICE DESCRIPTION ON FREE-EDGE (SWITCH SETTINGS)

G) 32-35 U/D-BUS BITS FOR WRAP

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOCATION
				U/D-BUS-32;100	U/D-BUS-33;100	U/D-BUS-34;100	U/D-BUS-35;100	A6, B6, AE, BE & U-BUS-BCD=1

T&D FUNCTIONALITY FOR WRAP

FIGURE 3.1.1.5.2

3.1.2 IOM Interface

The IOM interface is located on the backpanel edge of the EURC. The IOM has the following busses which the EURC must be connected. Refer to Figure 2.1.1 and Figure 3.1.2.1.

1. U-BUS

   A unidirectional bus on which the IOM sends data and commands to the EURC. (36 bits +1P).

2. D-BUS

   A unidirectional bus on which the EURC sends data and commands to the IOM. (36 bits +1P).

3. N-BUS

   A unidirectional bus from the IOM that sends the EURC its channel number.

4. Sequence Bits

   A number of signals passed to and from the EURC that are basically of a handshaking type of nature.

3.1.2.1 U-BUS

Physically the U-BUS is 36 bits plus one odd parity bit that is sent to the EURC. The receiving register on the EURC is set up for double precision loads based on the previously sent transaction command. The sequencing logic is the governing factor on when the data is strobed into the EURC. Table 3.1.2.1.1 is a list of the backpanel signals that form the U-BUS.

TABLE 3.1.2.1.1

LOCATION	BACKPANEL SIGNAL
WA 12	U-BUS-00*000
WA 16	U-BUS-01*000
WA 20	U-BUS-02*000
WA 02	U-BUS-03*000
WA 06	U-BUS-04*000
WA 10	U-BUS-05*000
WA 14	U-BUS-06*000
WA 18	U-BUS-07*000
WC 00	U-BUS-08*000
WC 04	U-BUS-09*000
WC 08	U-BUS-10*000
WC 12	U-BUS-11*000
WC 16	U-BUS-12*000
WC 20	U-BUS-13*000
WD 02	U-BUS-14*000
WD 06	U-BUS-15*000

TABLE 3.1.2.1.1 (CONTINUED)

LOCATION	BACKPANEL SIGNAL
WD 10	U-BUS-16*000
WD 14	U-BUS-17*000
WD 18	U-BUS-18*000
WE 00	U-BUS-19*000
WG 12	U-BUS-20*000
WG 16	U-BUS-21*000
WG 20	U-BUS-22*000
WH 02	U-BUS-23*000
WH 06	U-BUS-24*000
WH 10	U-BUS-25*000
WH 14	U-BUS-26*000
WH 18	U-BUS-27*000
WJ 00	U-BUS-28*000
WJ 04	U-BUS-29*000
WJ 08	U-BUS-30*000
WJ 12	U-BUS-31*000
WJ 16	U-BUS-32*000
WJ 20	U-BUS-33*000
WK 02	U-BUS-34*000
WK 06	U-BUS-35*000
WK 10	U-BUS-PARITY*004

The block diagram in Figure 3.1.2.1.2 gives a feel on how the microprocessor interfaces with the U-BUS.

3.1.2.2 D-BUS

Physically the D-BUS is 36 bits plus one odd parity bit that is sent to the IOM from the EURC. The sending register on the EURC is set up for double precision operations plus a word for the transaction command which must be sent to the IOM on every service. The sequencing logic formed by the FPLA is the governing factor of when the information will leave the EURC to be sent to the IOM. Table 3.1.2.2.1 is a list of backpanel signals that form the D-BUS.

The block diagram in Figure 3.1.2.2.2 gives a feel on how the microprocessor interfaces with the D-Bus.

The formats in Figure 3.1.2.2.3 show how the byte data from the microprocessor is transferred into D-BUS format of 36 bits plus parity.

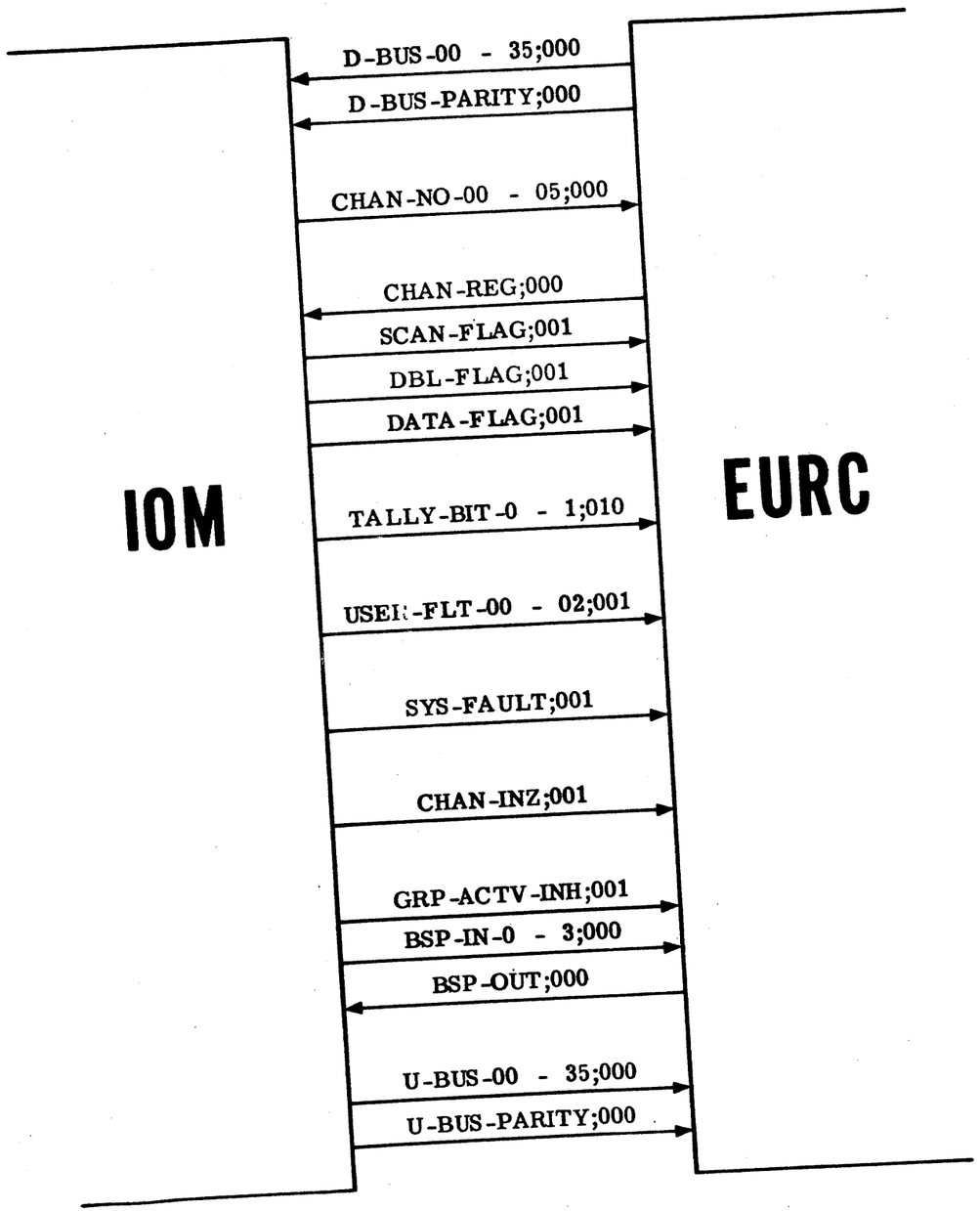


FIGURE 3.1.2.1

THE BLOCK DIAGRAM IN FIGURE 3.1.2.1-2 GIVES A FEEL ON HOW THE MICROPROCESSOR INTERFACES WITH THE U-BUS.

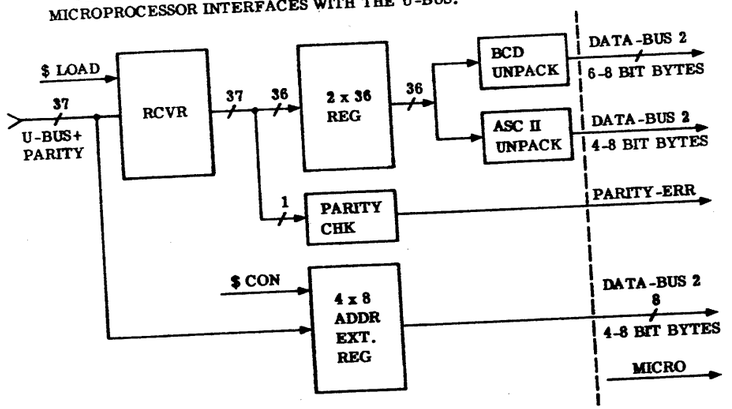


FIGURE 3.1.2.1.2

TABLE 3.1.2.2.1

LOCATION	BACKPANEL SIGNAL
WA 10	D-BUS-00*000
WA 14	D-BUS-01*000
WA 18	D-BUS-02*000
WB 00	D-BUS-03*000
WB 04	D-BUS-04*000
WB 08	D-BUS-05*000
WB 12	D-BUS-06*000
WB 16	D-BUS-07*000
WB 20	D-BUS-08*000
WC 02	D-BUS-09*000
WC 06	D-BUS-10*000
WC 10	D-BUS-11*000
WC 14	D-BUS-12*000
WC 18	D-BUS-13*000
WD 00	D-BUS-14*000
WD 04	D-BUS-15*000
WD 08	D-BUS-16*000
WD 12	D-BUS-17*000
WD 16	D-BUS-18*000
WD 20	D-BUS-19*000
WG 10	D-BUS-20*000
WG 14	D-BUS-21*000
WG 18	D-BUS-22*000
WH 00	D-BUS-23*000
WH 04	D-BUS-24*000
WH 08	D-BUS-25*000
WH 12	D-BUS-26*000
WH 16	D-BUS-27*000
WH 20	D-BUS-28*000
WJ 02	D-BUS-29*000
WJ 06	D-BUS-30*000
WJ 10	D-BUS-31*000
WJ 14	D-BUS-32*000
WJ 18	D-BUS-33*000
WK 00	D-BUS-34*000
WK 04	D-BUS-35*000
WK 08	D-BUS-PARITY*000

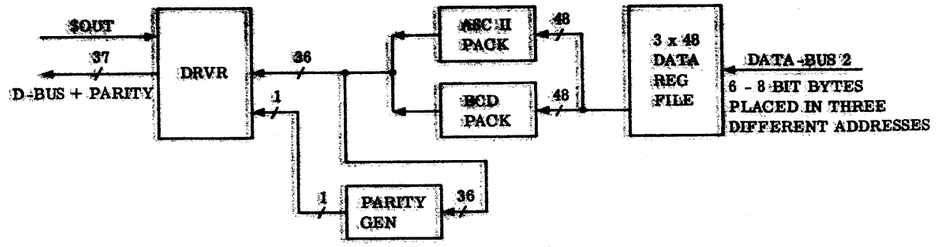


FIGURE 3.1.2.2.2

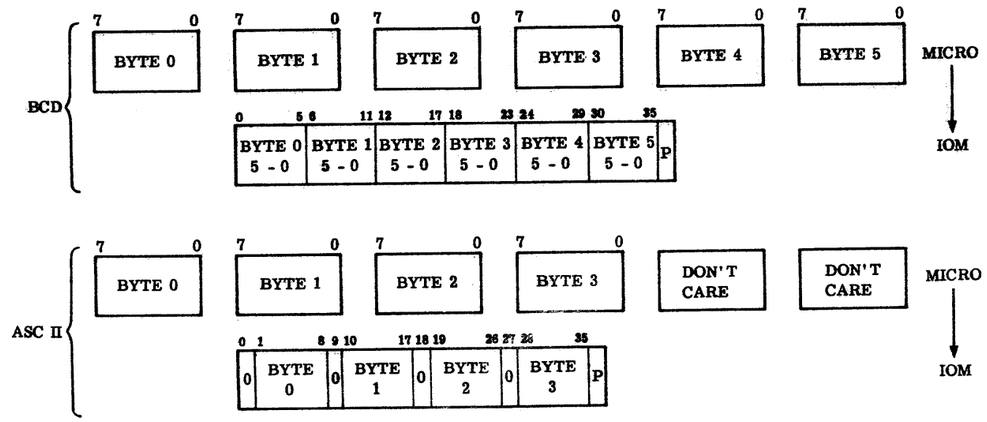


FIGURE 3.1.2.2.3

3.1.2.3 N-BUS

The N-BUS consists of 6 unidirectional signals sent to the EURC from the IOM. The signal names are CHAN-NO-0 through 5 where bit 0 is the most significant. Basically this bus is how a connect is issued to the EURC so communication between the IOM and EURC may begin. Each controller in the IOM interfaces to the N-BUS and constantly monitors this bus for a match to the controller's preset channel number. A list of the N-BUS constantly monitors this bus for a match to the controller's preset channel number. A list of the N-BUS signals and input locations can be found in Table 3.1.2.3.1. On the EURC a rocker switch is present so a channel number can be associated to the controller. Refer to Figure 3.1.2.3.2.

TABLE 3.1.2.3.1

LOCATION	BACKPANEL SIGNAL
WE 02	CHAN-NO-00*000
WE 04	CHAN-NO-01*000
WE 04	CHAN-NO-02*000
WE 08	CHAN-NO-03*000
WE 10	CHAN-NO-04*000
WE 12	CHAN-NO-05*000

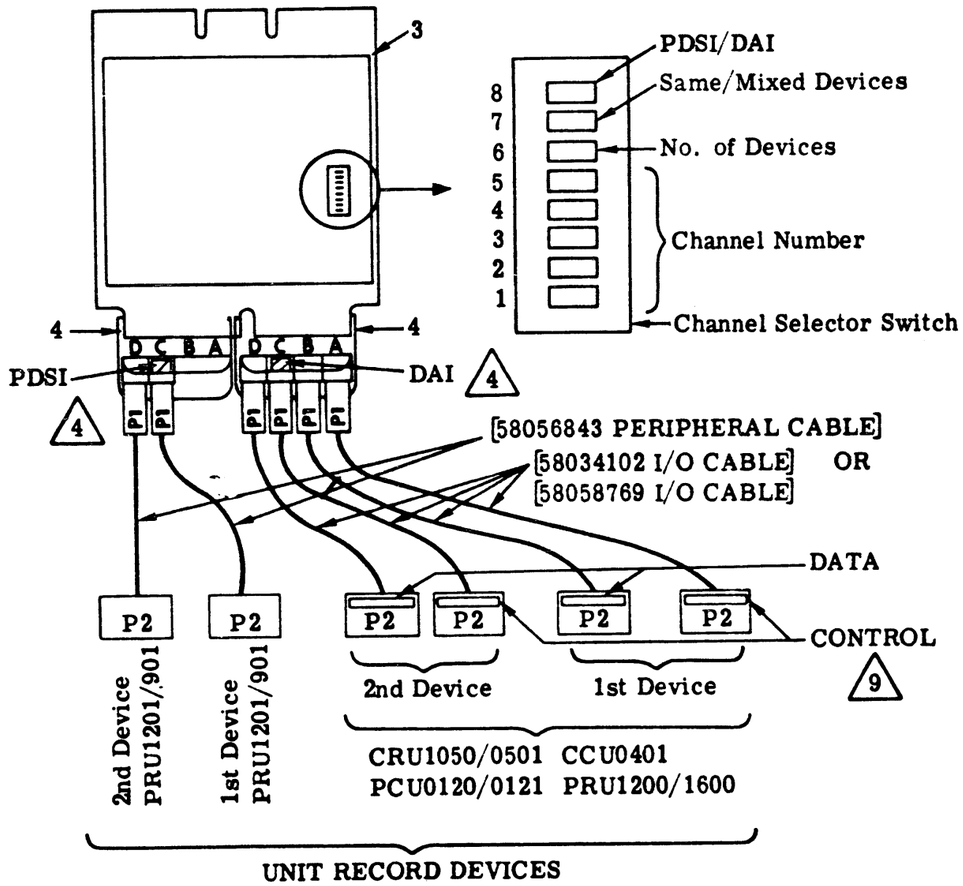


FIGURE 3.1.2.3.2

Switch 6, 4-CHAN-SEL*000, when closed places the EURC on modular 4 bounds and when open places it on modular 2 bounds. With switch number 6 closed, CHAN-NO-4*000 is masked off from the compare logic so effectively CHAN-NO-4*000 and CHAN-NO-5*000 are don't care conditions in mod 4, however switch number 5 which creates CHAN-SW-04*000 active must be open so firmware can interpret the switch set up. (NOTE: Mod 4 not supported, therefore, switch 6 always open.)

Even though CHAN-NO-4*000 and CHAN-NO-5*000 are not used in the compare logic in mod 4 they direct what port address the U-BUS connect information (i.e., address extension, mask bit) will be located in the address extension register. Refer to Figures 3.1.1.5.1, 3.1.1.5.2 and 3.1.2.3.2.

In modular 2 switch number 6 is in the open position which allows the signals CHAN-NO-4*000 and CHAN-SW-4*000 to be compared. This means that CHAN-NO-5*000 will be a don't care in the compare logic and this bit alone will govern what port address in the address extension register the connect information will be located.

Refer to Figures 3.1.2.3.3 and 3.1.2.3.5 for the previous discussion.

So basically what happens with the N-BUS is switch numbers 1 through 5 (CHAN-SW-0,1,2,3 AND 4) are logically compared with signals CHAN-NO-0 through CHAN-NO-4 and if the SCAN-FLG signal is also present a connect has been issued to the EURC.

Refer to Figure 3.1.2.3.3 and Figure 3.1.2.3.4. Four latches present on the EURC for storing which channel a connect exists. Visibility of these four latches are given to the microprocessor from the system programmable peripheral interface chip, see Figure 3.1.1.5.2. The appropriate signals are PCW-ACK-A*100 through PCW-ACK-D*100.

Switch number 7 and number 8 also have meanings but they are not hardware interpreted. Figure 3.1.2.3.4 shows the possible switch settings with priority given on a logical channel basis starting from 0. Figure 3.1.1.5.2 shows the base channel number register where the microprocessor reads the switch settings.

3.1.2.4 Sequence Bus

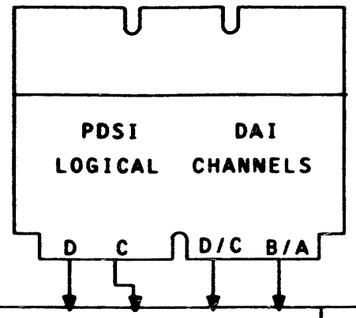
The sequence bus consists of all the signals in Figure 3.1.2.1 that have not been mentioned this far in the IOM Interface Section.

EURCB CHANNEL CONFIGURATION SWITCH SETTINGS

OCTAL		DECIMAL		CONFIGURATION SWITCHES*					
BASE CHAN	LOGICAL CHANNELS	BASE CHAN	LOGICAL CHANNELS	1	2	3	4	5	6
10	10-11	8	8- 9	1	1	0	1	1	1
12	12-13	10	10-11	1	1	0	1	0	1
14	14-15	8	12-13	1	1	0	0	1	1
16	16-17	14	14-15	1	1	0	0	0	1
20	20-21	16	16-17	1	0	1	1	1	1
22	22-23	18	18-19	1	0	1	1	0	1
24	24-25	20	20-21	1	0	1	0	1	1
26	26-27	22	22-23	1	0	1	0	0	1
30	30-31	24	24-25	1	0	0	1	1	1
32	32-33	26	26-27	1	0	0	1	0	1
34	34-35	28	28-29	1	0	0	0	1	1
36	36-37	30	30-31	1	0	0	0	0	1

*SWITCHES: 1=OPEN, 0=CLOSED

FIGURE 3.1.2.3.3



1=OPEN, 0=CLOSED

DEVICE CONNECTIONS				LOG CHANNEL REQD	SWITCH SETTING			INTERFACE PORT LOGICAL CHANNEL	
					6	7	8	0	1
NO	NO	NO	YES	2	1	1	0	DAI B/A	
NO	NO	YES	YES	2	1	1	0	DAI B/A	DAI D/C
NO	YES	NO	NO	2	1	1	1	PDSI C	
YES	YES	NO	NO	2	1	1	1	PDSI C	PDSI D
NO	YES	NO	YES	2	1	0	1	PDSI C	DAI B/A
					1	0	0	DAI B/A	PDSI C

IMPORTANT NOTICE:

PRINTER PRU1201/901 (PR54) MUST BE SET INTERNALLY TO REFLECT THE LOGICAL CHANNEL (0 OR 1) TO WHICH IT IS CONNECTED. REFER TO PR54 PRODUCT MANUAL 47240005-106, SECTION VIII "ON SITE REPAIR AND ADJUSTMENTS," PAGES 8-196,197.

LOCATE DIP SWITCH IN LOWER CENTER OF PDSI BOARD MOUNTED ON LEFT DOOR OF PR54. TO ADJUST TO LOGICAL CHANNEL 0, SET ALL SWITCHES ON DIP TO THE RIGHT (0) POSITION. IF LOGICAL CHANNEL 1 IS TO BE SELECTED, SET THE SECOND SWITCH FROM THE BOTTOM (MARKED '1') TO THE LEFT.

THERE ARE NO INTERNAL ADDRESS SWITCHES ON THE PRU 1200/1600 (PR71) PRINTER.

DO NOT MIX DEVICE TYPES ON A BOARD. PLACE CARD EQUIPMENT ON ONE BOARD AND PRINTERS ON ANOTHER.

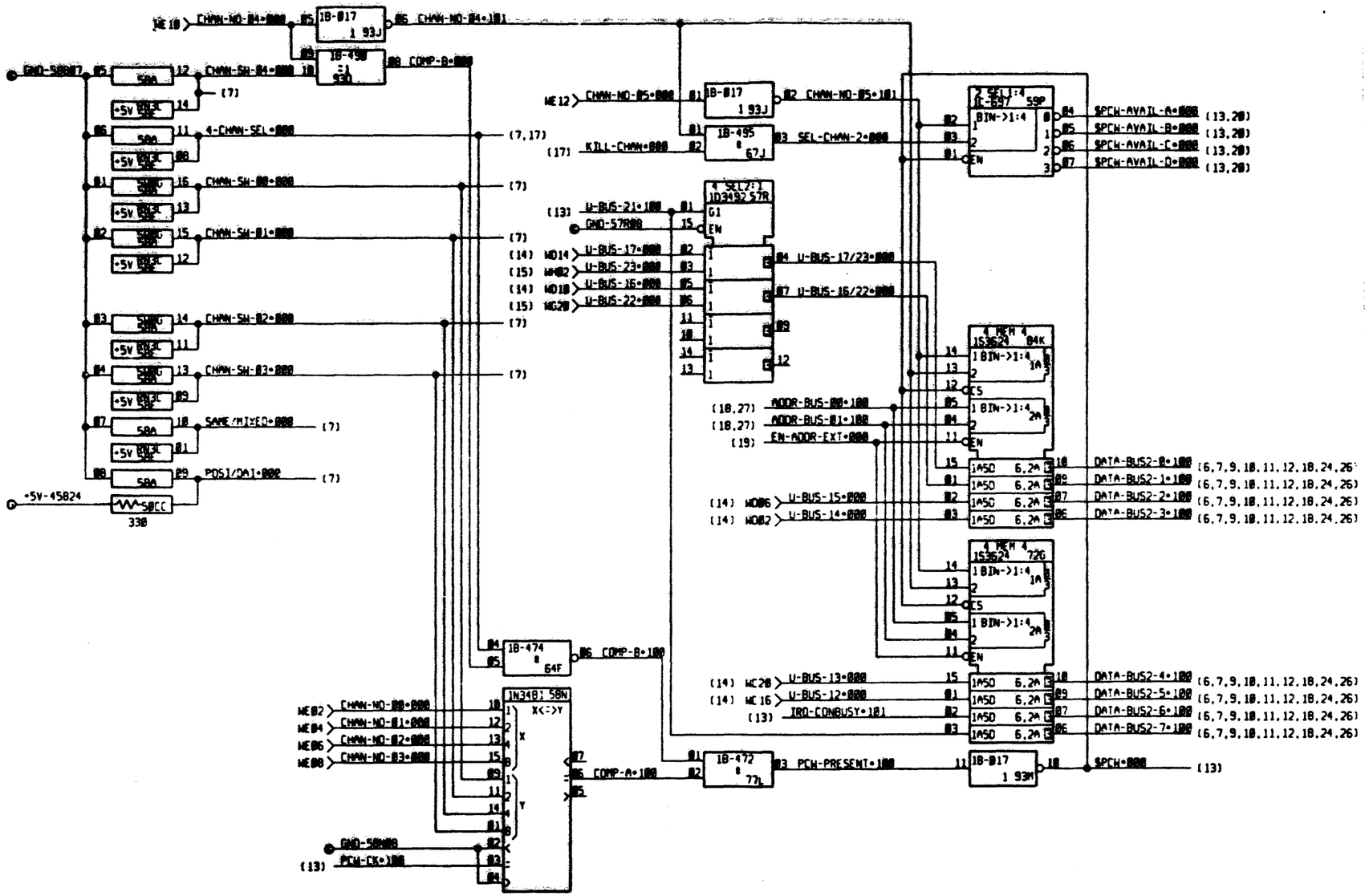


FIGURE 3.1.2.3.5

3.1.2.4.1 Reset Logic

The CHAN-INZ*000 signal is monitored by the EURC at all times. This signal is located on backpanel pin WZ 00. When this signal goes true (true = 0), all components that can be reset or placed in a known state will do so. Once this signal returns to the normal false state the microprocessor will start processing from location OFFFOH which is the beginning of the self-test routine.

3.1.2.4.2 Priority

The EURCs priority is based on the location it is placed in the IO system. It is indicated in the installation instructions, 58, that the following is the list of priorities.

The signals used for priority and the locations are listed in Table 3.1.2.4.2.1.

TABLE 3.1.2.4.2.1

LOCATION	BACKPANEL SIGNALS
WF 10	GRP-ACTV-INH*001
WF 02	NDP-IN-0*000
WF 04	BSP-IN-1*000
WF 06	BSP-IN-2*000
WF 08	BSP-IN-3*000
WF 04	BSP-OUT*000

The five inputs for priority are basically placed into a NAND gate and if any go active the EURC has lost priority and BSP-OUT*000 will be inactive. If the EURC has priority BSP-OUT will be active only if the EURC needs a service.

The BSP-IN signals are the BSP-OUT signals from the four boards above the EURC in bucket and the GRP-ACTV-INH is passed to the bucket the EURC is located from the bucket above it in the priority scheme.

3.1.2.4.3 Sequencing Bus

IOM Generated Signals:

LOCATION	BACKPANEL SIGNALS
WF 14	SCAN-FLG*001
WG 02	DBL-FLG*001
WF 18	DATA-FLAG*001
WE 14	SYS-FAULT*001
WE 16	USER-FLT-00*001
WE 18	USER-FLT-01*001
WE 20	USER-FLT-02*001
WG 06	TALLY-BIT-0*010
WG 08	TALLY-BIT-1*010

EURC Generated Signals:

External:

LOCATION	BACKPANEL SIGNALS
WG 04	CHAN-REQ*001

Internal:

SERV-REQ, HIR-CHAN, FPLA-ON, FF-DBL-FLAG, FF-SCAN-FLAG, E-XACT, E-1-DATA, E-2-DATA, DATA-OUT-1, DATA-OUT-2, FLAGS, TERM-SERV-REQ, XACT-27, XACT-29, XACT-31

3.1.2.4.3.1 Functional Description

Refer to the timing diagram in Figure 3.1.2.4.3.1.1.

t1 The EURC generates a SERV-REQ signal when a service is needed. SERV-REQ is a latched signal which lasts throughout the entire service, it causes a CHAN-REQ signal to be output to the IOM.

t2 After the CHAN-REQ is generated and latched by the EURC, two other signals must conform in order for the EURC and IOM to communicate. The order of occurrences of the next two signals does not matter, however, they both must be present at the same time in conjunction with the CHAN-REQ signal being active.

SCAN-FLAG must be inactive (high) for the FPLA-ON signal to be generated through a bistable.

HIR-CHAN must be inactive (high) and this would mean the EURC has priority and should generate the signal FPLA-ON.

With FPLA-ON just becoming active, the EURC is the only channel trying to become "active" at this time. The "normal state" is present at the output of the FPLA.

t3 SCAN-FLAG becomes active and this directly relates to the EURC sending the transaction command to the IOM with the generation of E-XACT. At this time, transaction bits 27, 29, and 31 (XACT-27, XACT-29, XACT-31) are strobed into a register to be used further into the sequence.

t4 DBL-FLAG becomes active and this signal causes two definite signals, one to be generated and one to be stopped, and causes another possible event depending on the transaction bits. At this point in time, the transaction command will be taken off the D-BUS and a bistable will be strobed and generate the signal FF-DBL-FLAG.

The possible event would be that E-1-DATA would become active if XACT-27 and XACT-29 were both at a high or low level. If the two XACT bits stated were not at the same state, E-1-DATA would not be generated and the FPLA output would indicate the "normal state."

t5 DBL-FLAG becomes inactive, could cause no occurrences or a number of occurrences on the basis of the three transaction bits.

XACT-27 = 0, XACT-29 = 0, XACT-31 = X:
Causes E-1-DATA to stay active from the event that took place in t4.

XACT-27 = 1, XACT-29 = 1, XACT-31 = 0:
Causes E-1-DATA to stay active from the event that took place in t4.

XACT-27 = 1, XACT-29 = 1, XACT-31 = 1:
Causes E-1-DATA to become inactive and E-2-DATA become active which enables the second word of data to the IOM from the EURC.

All other formats of the transaction bits would produce a "normal state" at the FPLA.

t6 SCAN-FLAG becomes inactive, at this point in time the EURC will either become an "active" channel or lose the service based on the priority, HIR-CHAN.

If HIR-CHAN is inactive, the EURC has priority and will become "active" and therefore the bistable which latched the CHAN-REQ signal is cleared.

If HIR-CHAN is active, the EURC does not have priority and will lose the service. At this point in time, CHAN-REQ must stay latched and FPLA-ON will be cleared so the EURC will not be recognizing a higher priority channel's service. Since the EURC has lost the service it will have to begin all over again to attain a new service, so t2 will be the state where the EURC is presently located.

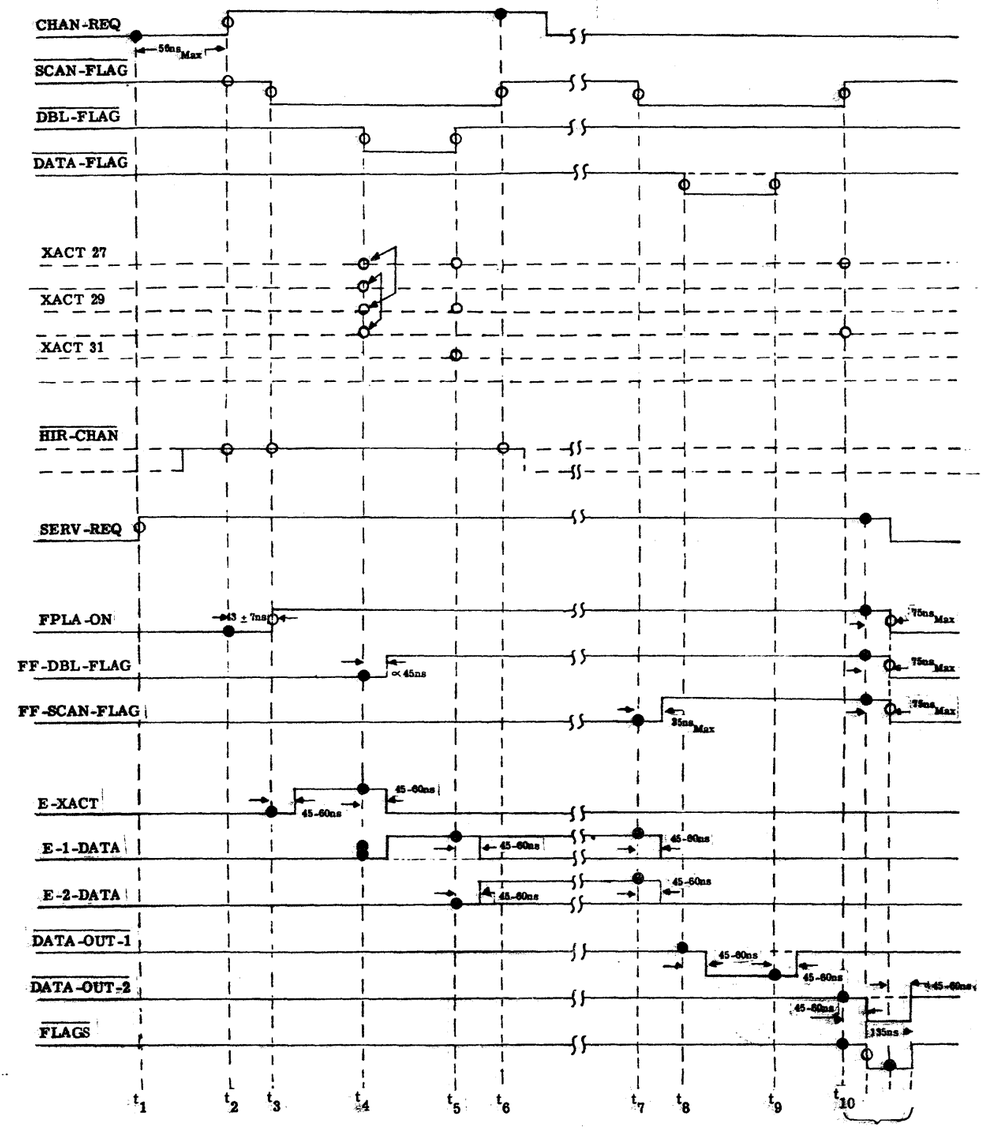
t7 At some time, SCAN-FLAG goes active once again. If E-1-DATA or E-2-DATA are present from the previous time frames they will be cleared at this point. FPLA is at a "normal state."

t8 DATA-FLAG will become active only if the IOM is doing a double precision service. This will cause DATA-OUT-1 to become active at the output of the FPLA and thus let data enter the EURC from the IOM and be placed into a 36 bit register file.

t9 DATA-FLAG becomes inactive and disables the write line on the 36 bit register file.

t10 SCAN-FLAG becomes inactive, this causes a sequence of events with one event being based on the transaction bits. This second SCAN-FLAG is indicating the end of service.

Always occur:
SCAN_FLAG will cause the FLAGS signal to become active. FLAGS will clear all bistable outputs that are connected to the inputs of the FPLA including FPLA-ON, FF-DBL-FLAG, FF-SCAN-FLAG. FLAGS will also strobe the user faults, tally bits, parity error, system fault, and terminate service valid into a status register. It also clears the bistable generating SERV-REQ.



BUS SEQUENCING

FIGURE 3.1.2.4.3.1.1

XACT-27 = 1, XACT-29 = 0, XACT-31 = X:
Causes the DATA-OUT-2 signal to become active thus enabling a word of data to enter the EURC from the IOM and be placed in a 36 bit register file.

Both the DATA-OUT-2 and FLAGS will be terminated once the FPLA is "turned-off" by the clearing of FPLA-ON.

3.1.2.4.3.2 Definition of EURC Bus Sequencing Terms

CHAN-REQ -- An active low signal recognized by the IOM and generated by the EURC as a result of wanted service.

DATA-OUT-1 -- An active low signal which allows the first word of data of a double precision service to be received by the EURC from the IOM.

DATA-OUT-2 -- An active low signal which allows a word of data to be received by the EURC from the IOM whether it be a single precision service or the second word of a double precision service.

E-1-DATA -- An active high signal which enables the first word of data to be transmitted to the IOM from the EURC.

E-2-DATA -- An active high signal which enables the second word of data to be transmitted to the IOM from the EURC.

E-XACT -- An active high signal which allows the transaction command to be sent to the IOM from the EURC.

FF-DBL-FLAG -- An active high signal generated by a bistable as the result of the EURC having the service and the signal DBL-FLAG becoming active (DBL-FLAG is genrated by the IOM).

FF-SCAN-FLAG -- An active high signal generated by a bistable as the result of the EURC being in the active state and the second SCAN-FLAG of the service becoming active (SCAN-FLAG is generated by the IOM).

FPLA-ON -- An active high signal which is the most significant input to the FPLA, if this signal is not active (low) the FPLA will not recognize any of the other inputs connected to it. Therefore, the EURC will not be communicating with the IOM.

FLAGS -- An active low signal which is generated at the end of every service. It allows the USER-FAULTS, PARITY-ERR-FLAG, TALLY-BITS and TERM-SERV-VALID bit to be placed in a status register.

HIR-CHAN -- An active low signal which is indirectly generated by the EURC, priority is governed by this signal and if low the EURC does not have priority, thus if the EURC is not active it will lose the service.

SERV-REQ -- An active high signal which is present throughout the entire service and is the signal that is generated when the EURC wants a service.

TERM-SERV-REQ -- An active high signal which is the inverted signal of FLAGS.

XACT-27, XACT-29, XACT-31 -- Bits which are latched from the transaction command, they are connected to the FPLA and govern E-1-DATA, E-2-DATA and DATA-OUT-2.

3.1.2.4.3.3 FPLA Device

The FPLA is programmed in such a fashion that it looks like a storage device. The outputs are a direct function of the inputs with a maximum delay time of 50 nanoseconds.

The FPLA can be set up with a specified "normal state" on the output, either with it disabled or enabled with inputs that are not a function of the output. For the EURC design, the FPLA is always enabled, however, when an input is present that does not cause a reaction to be generated on the output it will be at the programmed "normal state" of 000111xx. Identification of the bits starting with the most significant: E-XACT, E-1-DATA, E-2-DATA, DATA-OUT-1, DATA-OUT-2, and FLAGS. The don't cares are unused output pins on the FPLA.

The program resident in the FPLA is indicated in Table 3.1.2.4.3.4.1. I0 - I10 are the input pins used and F0 - F5 are the output pins. The "UNRECOGNIZABLE INPUTS" resulting output is the "normal state."

3.1.2.4.3.4 FPLA Used in the Sequence

Since the FPLA is going to be used in a sequencer circuit there are definite states that the output must be in with relation to time.

There are only five possible paths that can be followed with the assumption that the EURC does not lose the service. Each path is one service (two SCAN-FLAG signals) and they are as specified below.

Possible Paths that can be followed:

1. NORMAL STATE -- TRANSACTION COMMAND -- NORMAL STATE -- FAULT, TALLY AND PARITY BITS TO EURC

2. NORMAL STATE -- TRANSACTION COMMAND -- 1ST DATA TO IOM -- NORMAL STATE -- FAULT, TALLY AND PARITY BITS TO EURC

3. NORMAL STATE -- TRANSACTION COMMAND -- 1ST DATA TO IOM -- 2ND DATA TO IOM -- NORMAL STATE -- FAULT, TALLY AND PARITY BITS TO EURC

4. NORMAL STATE -- TRANSACTION COMMAND -- NORMAL STATE -- SINGLE PRECISION DATA PLUS FAULT, TALLY AND PARITY BITS TO EURC

5. NORMAL STATE -- TRANSACTION COMMAND -- NORMAL STATE -- 1ST DATA OF DOUBLE PRECISION TO EURC -- 2ND DATA OF DOUBLE PREVISION PLUS FAULT, TALLY AND PARITY BITS TO EURC

Truth Table:

FPLA-ON	FF-DBL-FLAG	FF-SCAN-FLAG	CHAN-REQ	SCAN-FLAG	DBL-FLAG	DATA-FLAG	XACT-27	XACT-29	XACT-31	HIR-CHAN	E-XACT	E-1-DATA	E-2-DATA	DATA-OUT-1	DATA-OUT-2	FLAGS
I0	I1	I2	I3	I4	I5	I6	I7	I8	I9	I10	F0	F1	F2	F3	F4	F5
1	0	0	1	1	0	x	x	x	x	1	1	0	0	1	1	1
1	0	0	1	1	1	x	0	0	x	1	0	1	0	1	1	1
1	0	0	1	1	1	x	1	1	x	1	0	1	0	1	1	1
1	1	0	1	1	0	x	0	0	0	1	0	1	0	1	1	1
1	1	0	1	1	0	x	1	1	0	1	0	1	0	1	1	1
1	1	0	1	1	0	x	1	1	1	1	0	0	1	1	1	1
1	1	0	1	0	0	0	0	0	0	1	0	1	0	1	1	1
1	1	0	1	0	0	0	1	1	0	1	0	1	0	1	1	1
1	1	0	1	0	0	0	1	1	1	1	0	0	1	1	1	1
1	1	0	0	0	0	0	0	0	0	x	0	1	0	1	1	1
1	1	0	0	0	0	0	1	1	0	x	0	1	0	1	1	1
1	1	0	0	0	0	0	1	1	1	x	0	0	1	1	1	1
1	1	1	0	*	x	1	1	0	1	x	0	0	0	0	1	1
1	1	1	0	0	0	0	0	x	x	x	0	0	0	1	1	0
1	1	1	0	0	0	0	1	0	0	x	0	0	0	1	0	0
1	1	1	0	0	0	0	1	0	1	x	0	0	0	1	0	0
1	1	1	0	0	0	0	1	1	x	x	0	0	0	1	1	0
UNRECOGNIZIBLE INPUTS											0	0	0	1	1	1

TABLE 3.1.2.4.3.4.1

Another possible way to look at the paths with a more detailed description is using a state diagram of the sequencer function (Figure 3.1.2.4.3.4.2). The binary style number in each state is the output of the FPLA in that particular state. It is important to note the transaction bits located along the paths because they govern which type of function is going to take place in the sequence.

3.1.3 Peripheral Device Serial Interface (PDSI)

The Peripheral Device Serial Interface (PDSI) is a communications style interface similar to HDLC, but tailored to unit record peripherals.

The data to be sent over the interface is read from a buffer in RAM and written to the Advance Data Link Controllers (ADLC) which does the parallel to serial conversion, performs the HDLC formatting, and outputs the serial bit stream to the output drivers. (See Figure 3.1.3.1) The hardware for the 2 PDSI ports requires only 5 chips, with most of the functionality contained in the ADLC (HIS part number 58002701, Motorola MC68B54). Two flip flops are used to divide the 5 MHZ system clock down to a 1.25 MHZ clock that is synchronized with the 8088 bus cycle to meet the unique requirements of the ADLC's enable clock input. The chip select input also has to be synchronized with the system clock to insure proper read/write timing. An address line was used as the input to the read/write line of the ADLC to satisfy further timing constraints. To write to the ADLC's 4 internal register use an output (40H-43H), for reading use input (60H-63H).

Data received from the device causes an interrupt to the 8259A (IR2). The RS422 receivers are tri-stated on the ADLC Rx Data and Rx Clock inputs and are enabled by bits 4 and 5 of ports of the system 8255. The drivers are enabled by bits 0 and 1 of port C. As an example, to enable PDSI port 0 for use you would "output (56H) = 11H" where 56H is the I/O address of port C on the system 8255. (Refer to section 3.1.1 microprocessor circuitry for further details on microprocessor support chips.)

The physical interface consists of 4 twisted pairs (send data, terminal timing, receive data, receive timing) and 2 grounds (signal gound, shield). The physical connection was patterned after RS449 and the drivers and receivers conform to CCITT V.II and RS-422A. The signal interconnections are given in Figure 3.1.3.2. Each receiver twisted pair is terminated by a 100 ohm resistor. The maximum cable length with 24 awg twisted pair is approximately 150 meters. The data rate across the interface is 750 KHZ.

EURC IOM INTERFACE
STATE DIAGRAM:

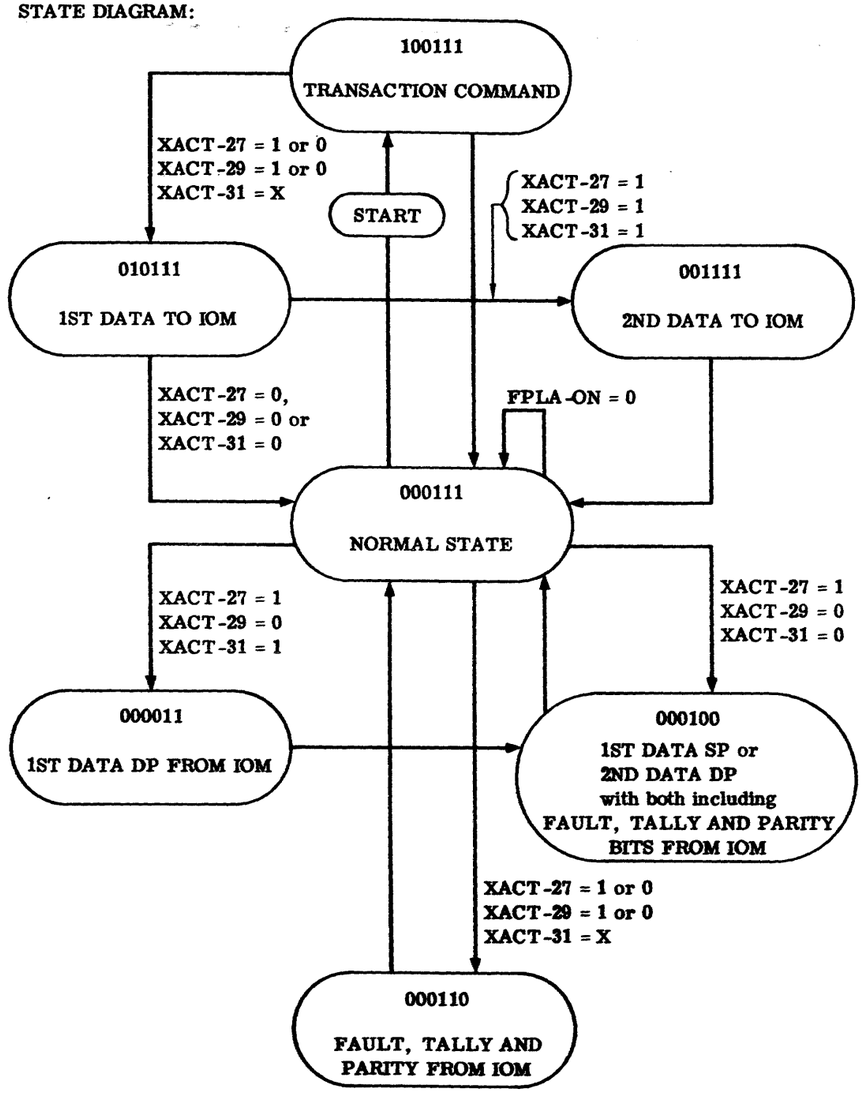


FIGURE 3.1.2.4.3.4.2

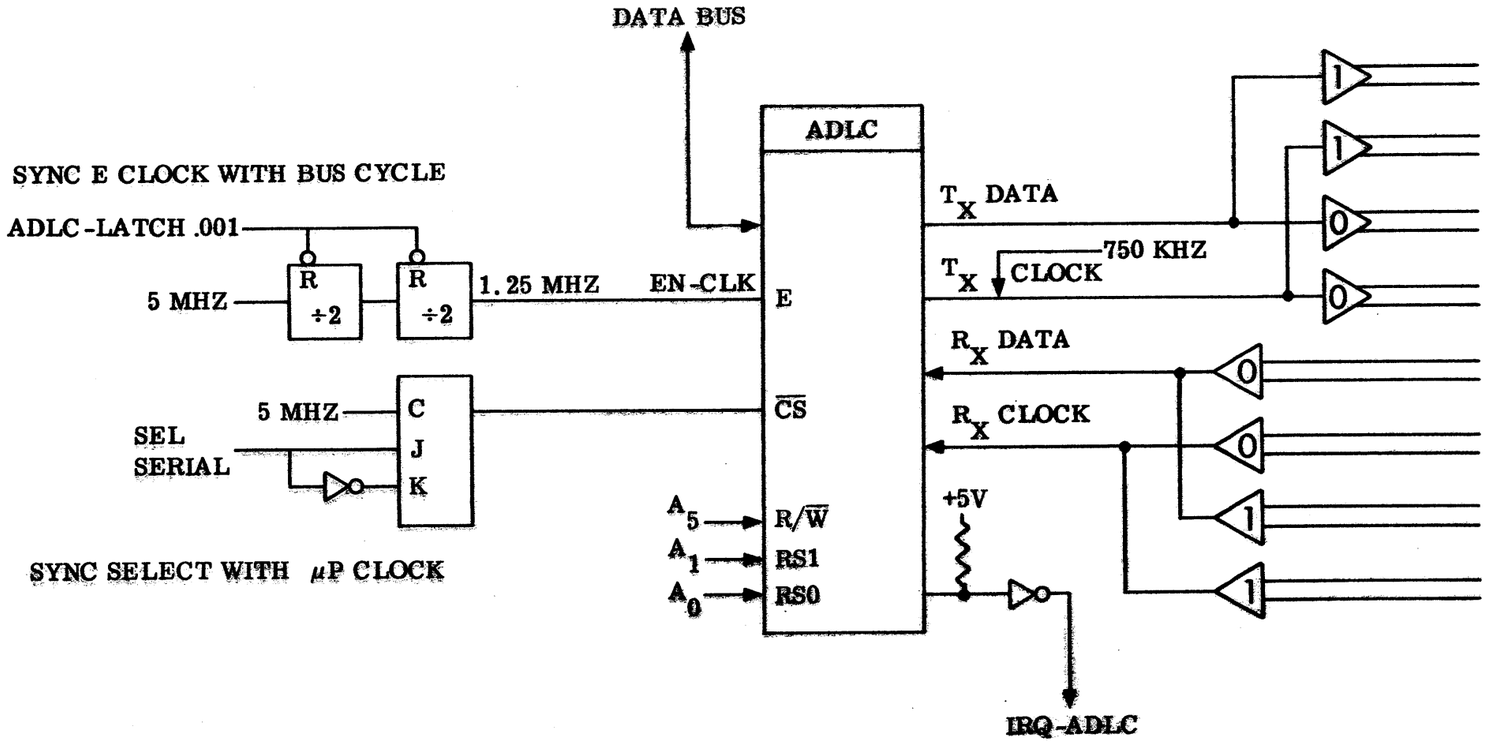

DATA BUS
ADLC
SYNC E CLOCK WITH BUS CYCLE
ADLC-LATCH .001
5 MHZ
R
÷2
R
÷2
1.25 MHZ
EN-CLK
E
T_X DATA
T_X CLOCK
750 KHZ
R_X DATA
R_X CLOCK
5 MHZ
SEL
SERIAL
C
J
K
CS
A5
A1
A0
R/W
RS1
RS0
+5V
IRQ-ADLC
SYNC SELECT WITH μP CLOCK
1
1
0
0
0
0
1
1

FIGURE 3.1.3.1

3.1.4 DAI

3.1.5 Board Test/Misc.

Since the EURC is a microprocessor based board, the board tester cannot find all the faults. To make up the difference the EURC has two stages of testing in the board tester.

3.1.5.1 Board Test Stage

The first stage is done with the normal board test vectors. Free running clocks are turned off, microprocessor is in a hold state and board test chips on the EURC are activated. The board test chips are only used in the board tester. In normal operations these chips are disabled. At the end of this stage an input vector is applied to the board and a delay is inserted before the final compare.

3.1.5.2 Self-Test State

The final stage is the self-test phase. The microprocessor and free running clocks are allowed to function and the board test chips are disabled. The purpose of the self-test in the board test environment is to move the different LSI chips on the EURC that the first stage of testing could not. The same self-test used in the board tester will be used in the IO system in the field.

3.1.5.2.1 Error Reporting

On the left free-edge of the EURC there are 6 red LEDs and 1 green LED. A fault dictionary exists and was created by Engineering to reference the 6 red LEDs. When the board is operating the first stage, all red LEDs should be on and the green one off. At the end of the first stage an input vector is applied to the EURC and the compare vector is delayed for approximately 20 seconds so the self-test can finish. At the end of the test a miscompare will be indicated on the board tester, however if the green LED is on and the red LEDs on the EURC are off the board has passed self-test. If the green LED is off and any number of LEDs on the EURC are on a fault exists and the self-test fault dictionary should be referenced because the board has failed self-test.

3.1.6 Fiber Optics Option

3.2 CORE FIRMWARE DESCRIPTION

3.3 RULES FOR APPLICATION FIRMWARE DESIGN

3.4 SPECIAL CONTROLLER COMMANDS

SIGNAL NAME	FREE EDGE	PADDLE BOARD	PR54 CONNECTOR
SD-0*100	LC15	1	6
SD-C-0*000	LC19	11	24
TT-0*100	LC09	4	8
TT-C-0*000	LC16	14	26
RD-0*100	LC04	7	17
RT-C-0*000	LC10	17	35
GND	LC07	18	1
GND	LC18	12	19

FIGURE 3.1.3.2

APPENDIX A

PRT0901/PRT1201

A.1 GENERAL OVERVIEW

General overview of this section describes the firmware required to attach a PRT0901/1201, also known as a PR54 printer, to the EURC.

A.1.1 Firmware Overview

There are two main programs that handle the PR54 printer attachment, PR54$APPLICATION processes commands queued on the IOMTOAPP$QUE, while PR54$INTERFACE processes commands queued on the LINK$TOAPP$QUE. Together these programs act as a firmware finite state machine.

The 512 byte per channel buffer is allocated as follows: Buffer (0-127) is used for responses from the printer and Buffer (128-511) = XMIT$BUF (0-383) is used for output to the printer.

A.2. DETAILED FIRMWARE DESCRIPTION

A.2.1 State Description

There are four main states in the PR54 firmware. In state 0 the firmware is waiting for a command on the IOMTOAPP$QUE. In state 1 two print lines have been sent to the PR54 and you are waiting for an end of End of Print (EOP) or End of Slew (EOS). In state 2 the firmware is waiting for an EOS from the printer or a command on the IOMTOAPP$QUE. State 3 waits for an EOP or an IOM command. In state 4 the firmware is waiting for a response from the pritner to a special function such as reading extended status registers. Figure A.2.1.1 outlines the PR54 firmware states and substates; Figure A.2.1.2 is the state transition table; Figure A.2.1.3 shows the state transition map.

A.2.2 Typical Print Sequence

The IOM firmware starts the sequence by queuing an open to the PR54 application firmware. When the dispatcher transfers control to the application, the application resets the link, if necessary, queues a command request to the IOM and transitions from state 0/0 to 0/1. When the IOM module has obtained a command, the application decodes the command then checks for illegal device address, paper out, VFC and BIB Loaded, ready status and other information. If conditions are right for the execution of the command, the program branches to the appropriate command execution routine. For print/slew commands, the application must set up variables telling the IOM edit procedure the character type (BCD or ASCII), the specific procedure to use (NON$EDIT$PRINTBCDPTR, NON$EDIT$PRINT$ASCII$PTR, EDIT$PRINT$BCD$PTR, EDIT$PRINT$ASCII$PTR), the slew type (by count, by channel) and initial slew count. The application then enques a record request to the IOM firmware and waits for a record available from the IOM that indicates the print data has been fetched, edited and placed in the appropriate location in the buffer. The application then places the appropriate PDSI command syntax around the print data, calculates the final slew count utilizing the GCOS VFC format, determines the next state, sets a timer to poll for end of print, and enques an output available to the link. The link will add the HDLC header information and transmit the print/slew commands to the printer.

The physical byte stream sent to the PR54 for a typical print/slew sequence will be as follows: (HDLC flag) (HDLC address) (HDLC control) (write PLB) (data-1) ... (data-n) (GS) (print order) (write slew) (data) (slew order) (2 byte check character) (HDLC flag).

While one line is printing the application will ask for another line of data and attempt to always be one line ahead of the printer. This is necessary for full speed operation. Up to this point all of the application processing has been done in the PR54$application procedure. The rest of the processing is handled by the PR54$interface procedure. For a typical print sequence the PR54$interface procedure only has to wait for an End Of Print (EOP) or and End Of Slew (EOS) and then transition to the required next state.

The PDSI is a poll driven interface, i.e., the printer won't speak unless spoken to. The application set a timer when it sent the print line to the PR54. On timeout, a poll command is enqued to the link. If the PR54 does not have an event to report (e.g. EOP, EOS, Alarm) the timer will be set again and another poll will be generated at a later time. If an event was reported, it will be processed.

A.2.3 Exception Processing

A.2.3.1 Going Online

When the printer is offline the application firmware is in the idle state. While in the idle state the application polls the printer every 0.5 seconds to find out if an event has occurred, e.g. printer goes ready or control button interrupt. When the printer goes from offline to online the application reads the line count register of the PR54 to synchronize the PR54 and controller VFCS, clears the PR54 and IOM status variables and sends a special status to the IOM.

A.2.3.2 Control Button Processing

When an event register that has the control button interrupt bit set is decoded the application firmware reads the PR54 control button register then goes through the same sequence as going online with the code of the button embedded in the special status and IOM substatus.

A.2.3.3 Error Processing

Most errors that are detected are reported by calling PR54$UPDATE$STATUS(module$id, error$no). The module$id tells which procedure is reporting the error (2=PR54$APPLICATION, 6=PR54$INTERFACE, 8=LINK); the error$nd uniquely identifies the error and is used as an index to PR54$STATUS$MAP which provides major and substatus. Error codes 0-49 indicate controller detected errors while codes 50-99 indicate device detected errors. PR54$UPDATE$STATUS updates IOM and PR54 status, makes an entry in the history registers, and terminates the channel program leaving the application in state 0/0.

Errors that are detected by the controller are usually reported immediately, but in some cases you must wait until there is no PR54 device activity in progress. In these cases an error pending command is pushed on to the IOMTOAPP$QUE and the error is not reported until the firmware is in state 0.

Errors that are detected by the printer are reported to the controller via the PDSI. An even register with the alarm bit set notifies the controller that an error has occurred in the printer. The controller reads the command and status registers, attempts to clear the alarm, and attempts to set the PR54 back online. The command and status register contents are saved for the anticipated extended status command. The status from the PR54 is then mapped into an error code from 50 to 99 and reported via PR54$UPDATE$STATUS. If the error was reset then the EURC and PR54 line counts must be resynchronized to account for any slews that may have been cancelled due to the alarm.

PR54 FIRMWARE STATES

STATE 0 Waiting for IOM response

SUBSTATE	
0	IDLE
1	COMMAND REQUESTED
2	PRINT/SLEW DATA REQUESTED
3	BIB DATA REQUESTED

STATE 1 Waiting for EOP/EOS

0 SLEW, PRINT, SLEW OUTSTANDING
1 PRINT, SLEW, PRINT, SLEW OUTSTANDING

STATE 2

0 NOT USED
1 SLEW OUT/COMMAND REQUESTED
2 SLEW OUT/PS DATA REQUESTED

STATE 3

0 NOT USED
1 PS OUT/COMMAND REQUESTED
2 PS OUT/PS DATA REQUESTED

STATE 4 Waiting for PR54 response to special function

0 VFC/BIB LOAD
1 EXTENDED STATUS
2 STATUS AFTER ALARM
3 CONTROL BUTTON
4 LINE COUNT

FIGURE A.2.1.1

PR54 FIRMWARE STATE TRANSITION TABLE

CURRENT STATE	NEXT STATE	DESCRIPTION
0/0	0/1	OPEN CHANNEL
0/0	4/3	CONTROL BUTTON ON PRINTER PRESSED
0/0	4/4	PR54 GOING ONLINE, READ LINE COUNT
0/1	0/2	RESET OR REQUEST STATUS EXECUTED
0/1	0/2	PRINT/SLEW COMMAND RECEIVED, DATA REQUESTED
0/1	0/3	LOAD BIB COMMAND RECEIVED, DATA REQUESTED
0/1	0/4	LOAD VFC COMMAND RECEIVED, DATA REQUESTED
0/1	2/1	SLEW 1/2/TOP EXECUTED, COMMAND REQUESTED
0/1	4/1	EXTENDED STATUS REQUESTED FROM PR54
0/2	2/1	SLEW OUTPUT TO PR54, COMMAND REQUESTED
0/2	3/1	PRINT/SLEW OUTPUT, COMMAND REQUESTED
0/3	4/0	WAIT FOR BIB LOAD VERIFICATION FROM PR54
0/4	4/0	WAIT FOR VFC LOAD VERIFICATION FROM PR54
1/0	3/1	END OF SLEW OCCURRED, COMMAND REQUESTED
1/1	1/0	END OF PRINT OCCURRED
2/1	0/1	END OF SLEW OCCURRED
2/1	2/2	PRINT/SLEW COMMAND RECEIVED, DATA REQUESTED
2/2	0/2	END OF SLEW OCCURRED
2/2	1/0	PRINT/SLEW DATA RECEIVED AND OUTPUT TO PR54
3/1	2/1	END OF PRINT OCCURRED
3/1	3/2	PRINT/SLEW COMMAND RECEIVED, DATA REQUESTED
3/2	1/1	PRINT/SLEW DATA RECEIVED AND OUTPUT TO PR54
3/2	2/2	END OF PRINT OCCURRED
4/0	0/1	EVENT WITH NO ALARM RECEIVED, I.E., LOAD OK
4/1	0/1	STORE EXTENDED STATUS, COMMAND REQUESTED
4/2	0/0	REPORT ERROR STATUS, GO IDLE
4/3	4/4	CONTROL BUTTON READ, ISSUE READ LINE COUNT
4/4	0/0	LINE COUNT READ, ISSUE SPECIAL STATUS, GO IDLE

FIGURE A.2.1.2

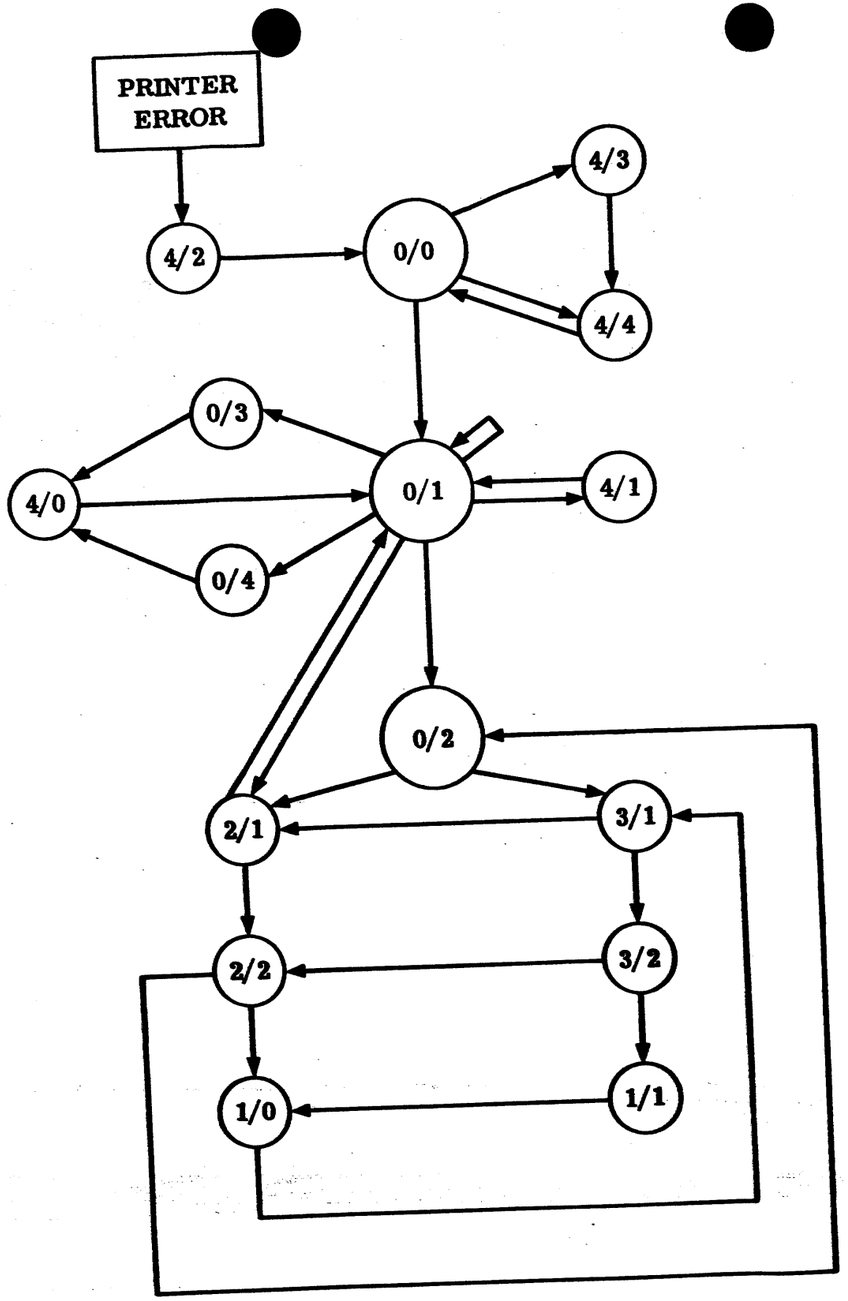


FIGURE A.2.1.3

STATE TRANSITION MAP

Card Box.....43A229674 AR
TAB (WEUR00XA).....58010073-900

MT8AC EWL.....58065905

REV	AUTHORITY	DATE
G	PHAODP028	82NOV10

SIGNAL NAME	PAGE
$CHAN-REQ•100	12.0
$CLK-1•100	8.0
$CLK-2•100	8.0
$IRQ-MASK-CON•100	13.0
$MDAI-END•000	31.0
$MDAI-PARITY-ERR•100	32.0
$PCW•000	5.0
$PCW-AVAIL-A•000	5.0
$PCW-AVAIL-B•000	5.0
$PCW-AVAIL-C•000	5.0
$PCW-AVAIL-D•000	5.0
$SERV-REQ•102	16.0
$SET•001	31.0
$SET•101	31.0
$TCR•100	17.0
+5V-00T-05	29.0
4-CHAN-SEL•000	5.0
ACK•001	30.0
ACK•100	30.0
ACK-INTR•000	18.0
ACK-INTR•101	19.0
ACK/FF2•001	31.0
ACK/FF2•001	32.0
ACK/FF2•100	31.0
AD-00•100	23.0
AD-00•100	27.0
AD-00•100	26.0
AD-00•100	22.0
AD-00•100	26.0
AD-00•100	22.0
AD-01•100	22.0
AD-01•100	23.0
AD-01•100	22.0
AD-01•100	23.0
AD-01•100	22.0
AD-01•100	26.0
AD-01•100	23.0
AD-01•100	27.0
AD-01•100	26.0
AD-02•100	22.0
AD-02•100	23.0
AD-02•100	26.0
AD-02•100	22.0
AD-02•100	26.0
AD-02•100	22.0
AD-02•100	27.0
AD-02•100	23.0
AD-03•100	23.0
AD-03•100	22.0
AD-03•100	26.0
AD-03•100	23.0
AD-03•100	22.0
AD-03•100	23.0
AD-03•100	26.0
AD-03•100	27.0
AD-04•100	26.0
AD-04•100	23.0
AD-04•100	22.0
AD-04•100	26.0
AD-04•100	27.0
AD-05•100	22.0
AD-05•100	26.0
AD-05•100	23.0
AD-05•100	26.0

SIGNAL NAME	PAGE
AD-05•100	22.0
AD-05•100	23.0
AD-05•100	27.0
AD-05•100	22.0
AD-06•100	23.0
AD-06•100	22.0
AD-06•100	27.0
AD-06•100	26.0
AD-06•100	22.0
AD-06•100	23.0
AD-06•100	26.0
AD-06•100	23.0
AD-06•100	22.0
AD-07•100	23.0
AD-07•100	22.0
AD-07•100	26.0
AD-07•100	22.0
AD-07•100	27.0
AD-07•100	26.0
ADDR-08•100	27.0
ADDR-08•100	18.0
ADDR-09•100	18.0
ADDR-09•100	27.0
ADDR-10•100	18.0
ADDR-10•100	27.0
ADDR-11•100	27.0
ADDR-11•100	18.0
ADDR-12•100	27.0
ADDR-12•100	18.0
ADDR-13•001	21.0
ADDR-13•100	18.0
ADDR-13•100	27.0
ADDR-14•001	21.0
ADDR-14•100	27.0
ADDR-14•100	18.0
ADDR-15•100	27.0
ADDR-15•100	18.0
ADDR-BUS-00•100	27.0
ADDR-BUS-00•100	18.0
ADDR-BUS-01•100	18.0
ADDR-BUS-01•100	27.0
ADDR-BUS-02•100	27.0
ADDR-BUS-02•100	18.0
ADDR-BUS-03•100	18.0
ADDR-BUS-03•100	27.0
ADDR-BUS-04•100	27.0
ADDR-BUS-04•100	18.0
ADDR-BUS-05•100	27.0
ADDR-BUS-05•100	18.0
ADDR-BUS-06•100	18.0
ADDR-BUS-06•100	27.0
ADDR-BUS-07•100	18.0
ADDR-BUS-07•100	27.0
ADDR-LATCH•001	18.0
ADDR-LATCH•100	18.0
ADDR-LATCH•101	18.0
ASCII•000	19.0
ASCII•001	19.0
ASCII/BCD-SEL•100	12.0
BCD•000	19.0
BCD•001	19.0
BSP-IN-0•000	17.0
BSP-IN-1•000	17.0
BSP-IN-2•000	17.0

SIGNAL NAME	PAGE
BSP-IN-3•000	17.0
BSP-LOW•000	17.0
BSP-OUT•000	17.0
BSP-OUT•100	17.0
CHAN-INZ•001	16.0
CHAN-INZ•101	16.0
CHAN-NO-00•000	5.0
CHAN-NO-01•000	5.0
CHAN-NO-02•000	5.0
CHAN-NO-03•000	5.0
CHAN-NO-04•000	5.0
CHAN-NO-04•101	5.0
CHAN-NO-05•000	5.0
CHAN-NO-05•101	5.0
CHAN-REQ•000	17.0
CHAN-REQ-FF•000	17.0
CHAN-REQ-FF•100	17.0
CHAN-SW-00•000	5.0
CHAN-SW-01•000	5.0
CHAN-SW-02•000	5.0
CHAN-SW-03•000	5.0
CHAN-SW-04•000	5.0
CLEAR•000	16.0
CLK-1500KHZ•100	28.0
CLK-23KHZ•100	28.0
CLK-2500KHZ•000	28.0
CLK-2500KHZ•100	28.0
CLK-375KHZ•100	28.0
CLK-3MHZ•100	28.0
CLK-5MHZ•100	19.0
CLK-750KHZ•100	28.0
CLR-1•000	8.0
CLR-2•000	8.0
CLR-3•000	8.0
CLR-PCW-CK•000	13.0
CLR-PCW-CK•100	13.0
CMP-A•000	15.0
CMP-B•000	15.0
COMP-A•100	5.0
COMP-B•000	5.0
COMP-B•100	5.0
CONTROL•000	30.0
COUNT•000	31.0
COUNT•100	31.0
D-BUS-00•000	9.0
D-BUS-01•000	9.0
D-BUS-02•000	9.0
D-BUS-03•000	9.0
D-BUS-04•000	9.0
D-BUS-05•000	9.0
D-BUS-06•000	9.0
D-BUS-07•000	9.0
D-BUS-08•000	9.0
D-BUS-09•000	9.0
D-BUS-10•000	9.0
D-BUS-11•000	9.0
D-BUS-12•000	10.0
D-BUS-13•000	10.0
D-BUS-14•000	10.0
D-BUS-15•000	10.0
D-BUS-16•000	10.0
D-BUS-17•000	10.0
D-BUS-18•000	10.0
D-BUS-19•000	10.0

SIGNAL NAME	PAGE
D-BUS-20•000	10.0
D-BUS-21•000	10.0
D-BUS-22•000	10.0
D-BUS-23•000	10.0
D-BUS-24•000	11.0
D-BUS-25•000	11.0
D-BUS-26•000	11.0
D-BUS-27•000	11.0
D-BUS-28•000	11.0
D-BUS-29•000	11.0
D-BUS-30•000	11.0
D-BUS-31•000	11.0
D-BUS-32•000	11.0
D-BUS-33•000	11.0
D-BUS-34•000	11.0
D-BUS-35•000	11.0
D-BUS-BCD•100	12.0
D-BUS-BCD•100	20.0
D-BUS-EN•000	12.0
D-BUS-EN-1•100	12.0
D-BUS-EN-2•100	12.0
D-BUS-EN-3•100	12.0
D-BUS-EN-4•100	12.0
D-BUS-PARITY•000	15.0
DAI-CSI-P0•100	35.0
DAI-CSI-P1•100	35.0
DAI-CSO-P0•100	35.0
DAI-CSO-P1•100	35.0
DAI-DATP0-0•100	33.0
DAI-DATP0-1•100	33.0
DAI-DATP0-2•100	33.0
DAI-DATP0-3•100	33.0
DAI-DATP0-4•100	33.0
DAI-DATP0-5•100	33.0
DAI-DATP0-6•100	33.0
DAI-DATP0-7•100	33.0
DAI-DATP1-0•100	34.0
DAI-DATP1-1•100	34.0
DAI-DATP1-2•100	34.0
DAI-DATP1-3•100	34.0
DAI-DATP1-4•100	34.0
DAI-DATP1-5•100	34.0
DAI-DATP1-6•100	34.0
DAI-DATP1-7•100	34.0
DAI-DSI-P0•100	35.0
DAI-DSI-P1•100	35.0
DAI-DSO-P0•100	35.0
DAI-DSO-P1•100	35.0
DAI-ENI-P0•100	35.0
DAI-ENI-P1•100	35.0
DAI-END-P0•100	35.0
DAI-END-P0•110	35.0
DAI-END-P1•100	35.0
DAI-END-P1•110	35.0
DAI-EV1-P0•100	36.0
DAI-EV1-P1•100	36.0
DAI-EV2-P0•100	36.0

DISTRIBUTION CODE C127-26

HONEYWELL
HONEYWELL INFORMATION SYSTEMS
LOC CEO PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- EURCB
LOGIC - PAGE CROSS REFERENCE

SIZE	DWG NO	SH	REV
B	58065904	1.0	G

DATA BASE L2/EURCBJ
DFIG B1FEB13

58065904

RE	AUTHORITY	DATE
G	PHAODP028	82NOV10

SIGNAL NAME	PAGE
DAI-EV2-P1•100	36.0
DAI-EV3-P0•100	36.0
DAI-EV3-P1•100	36.0
DAI-LATCH-DAT-7•100	31.0
DAI-OPI-P0•100	35.0
DAI-OPI-P1•100	35.0
DAI-OPO-P0•100	35.0
DAI-OPO-P0-FLT•000	35.0
DAI-OPO-P1•100	35.0
DAI-OPO-P1-FLT•000	35.0
DAI-PARP0•100	33.0
DAI-PARP1•100	33.0
DAI-PARP1•100	34.0
DAI-RSO-P0•100	35.0
DAI-RSO-P1•100	35.0
DAI-TD0•100	20.0
DAI-TD1•100	20.0
DATA-BUS1-0•001	25.0
DATA-BUS1-0•100	21.0
DATA-BUS1-0•100	18.0
DATA-BUS1-0•100	28.0
DATA-BUS1-0•100	16.0
DATA-BUS1-0•100	19.0
DATA-BUS1-1•001	25.0
DATA-BUS1-1•100	28.0
DATA-BUS1-1•100	19.0
DATA-BUS1-1•100	18.0
DATA-BUS1-1•100	21.0
DATA-BUS1-1•100	16.0
DATA-BUS1-2•001	25.0
DATA-BUS1-2•100	18.0
DATA-BUS1-2•100	16.0
DATA-BUS1-2•100	28.0
DATA-BUS1-2•100	21.0
DATA-BUS1-2•100	19.0
DATA-BUS1-3•001	25.0
DATA-BUS1-3•100	28.0
DATA-BUS1-3•100	21.0
DATA-BUS1-3•100	19.0
DATA-BUS1-3•100	16.0
DATA-BUS1-3•100	18.0
DATA-BUS1-4•001	25.0
DATA-BUS1-4•100	19.0
DATA-BUS1-4•100	21.0
DATA-BUS1-4•100	18.0
DATA-BUS1-4•100	16.0
DATA-BUS1-4•100	28.0
DATA-BUS1-5•001	25.0
DATA-BUS1-5•100	28.0
DATA-BUS1-5•100	16.0
DATA-BUS1-5•100	19.0
DATA-BUS1-5•100	21.0
DATA-BUS1-5•100	18.0
DATA-BUS1-6•100	16.0
DATA-BUS1-6•100	21.0
DATA-BUS1-6•100	28.0
DATA-BUS1-6•100	18.0
DATA-BUS1-6•100	19.0
DATA-BUS1-7•100	18.0
DATA-BUS1-7•100	19.0
DATA-BUS1-7•100	28.0
DATA-BUS1-7•100	16.0
DATA-BUS1-7•100	21.0
DATA-BUS2-0•100	5.0

SIGNAL NAME	PAGE
DATA-BUS2-0•100	18.0
DATA-BUS2-0•100	26.0
DATA-BUS2-0•100	24.0
DATA-BUS2-0•100	6.0
DATA-BUS2-0•100	7.0
DATA-BUS2-0•100	24.0
DATA-BUS2-1•100	24.0
DATA-BUS2-1•100	26.0
DATA-BUS2-1•100	6.0
DATA-BUS2-1•100	24.0
DATA-BUS2-1•100	18.0
DATA-BUS2-1•100	7.0
DATA-BUS2-1•100	5.0
DATA-BUS2-2•100	24.0
DATA-BUS2-2•100	7.0
DATA-BUS2-2•100	24.0
DATA-BUS2-2•100	6.0
DATA-BUS2-2•100	18.0
DATA-BUS2-2•100	26.0
DATA-BUS2-2•100	5.0
DATA-BUS2-3•100	26.0
DATA-BUS2-3•100	24.0
DATA-BUS2-3•100	6.0
DATA-BUS2-3•100	7.0
DATA-BUS2-3•100	5.0
DATA-BUS2-3•100	18.0
DATA-BUS2-3•100	24.0
DATA-BUS2-4•100	24.0
DATA-BUS2-4•100	5.0
DATA-BUS2-4•100	24.0
DATA-BUS2-4•100	7.0
DATA-BUS2-4•100	6.0
DATA-BUS2-4•100	18.0
DATA-BUS2-4•100	26.0
DATA-BUS2-4•100	24.0
DATA-BUS2-5•100	5.0
DATA-BUS2-5•100	24.0
DATA-BUS2-5•100	7.0
DATA-BUS2-5•100	18.0
DATA-BUS2-5•100	26.0
DATA-BUS2-5•100	6.0
DATA-BUS2-5•100	24.0
DATA-BUS2-6•100	18.0
DATA-BUS2-6•100	6.0
DATA-BUS2-6•100	26.0
DATA-BUS2-6•100	24.0
DATA-BUS2-6•100	7.0
DATA-BUS2-6•100	24.0
DATA-BUS2-6•100	5.0
DATA-BUS2-7•100	7.0
DATA-BUS2-7•100	18.0
DATA-BUS2-7•100	24.0
DATA-BUS2-7•100	26.0
DATA-BUS2-7•100	24.0
DATA-BUS2-7•100	5.0
DATA-BUS2-7•100	6.0
DATA-EN•000	27.0
DATA-EN•000	18.0
DATA-EN•101	19.0
DATA-FLAG•001	16.0
DATA-FLG•101	16.0
DATA-OUT-1•000	8.0
DATA-OUT-2•000	8.0
DBL-FLG•001	16.0

SIGNAL NAME	PAGE
DBL-FLG•101	16.0
DIREG-00•100	4.0
DIREG-01•100	4.0
DIREG-02•100	4.0
DIREG-03•100	4.0
DIREG-04•100	4.0
DIREG-05•100	4.0
DIREG-06•100	4.0
DIREG-07•100	4.0
DIREG-08•100	4.0
DIREG-09•100	4.0
DIREG-10•100	4.0
DIREG-11•100	4.0
DIREG-12•100	4.0
DIREG-13•100	4.0
DIREG-14•100	4.0
DIREG-15•100	4.0
DIREG-16•100	4.0
DIREG-17•100	4.0
DIREG-18•100	4.0
DIREG-19•100	4.0
DIREG-20•100	4.0
DIREG-21•100	4.0
DIREG-22•100	4.0
DIREG-23•100	4.0
DIREG-24•100	4.0
DIREG-25•100	4.0
DIREG-26•100	4.0
DIREG-27•100	4.0
DIREG-28•100	4.0
DIREG-29•100	4.0
DIREG-30•100	4.0
DIREG-31•100	4.0
DIREG-32•100	4.0
DIREG-33•100	4.0
DIREG-34•100	4.0
DIREG-35•100	4.0
DLY-FF1•000	31.0
DLY-FF2•000	31.0
DLY-FF2•100	31.0
DOREG-00•100	9.0
DOREG-01•100	9.0
DOREG-02•100	9.0
DOREG-03•100	9.0
DOREG-04•100	9.0
DOREG-05•100	9.0
DOREG-06•100	9.0
DOREG-07•100	9.0
DOREG-08•100	9.0
DOREG-09•100	9.0
DOREG-10•100	9.0
DOREG-11•100	9.0
DOREG-12•100	10.0
DOREG-13•100	10.0
DOREG-14•100	10.0
DOREG-15•100	10.0
DOREG-16•100	10.0
DOREG-17•100	10.0
DOREG-18•100	10.0
DOREG-19•100	10.0
DOREG-20•100	10.0
DOREG-21•100	10.0
DOREG-22•100	10.0
DOREG-23•100	10.0

SIGNAL NAME	PAGE
DOREG-24•100	11.0
DOREG-25•100	11.0
DOREG-26•100	11.0
DOREG-27•100	11.0
DOREG-28•100	11.0
DOREG-29•100	11.0
DOREG-30•100	11.0
DOREG-31•100	11.0
DOREG-34•100	11.0
DOREG-35•100	11.0
DOREG-36•100	12.0
DOREG-37•100	12.0
DOREG-38•100	12.0
DOREG-39•100	12.0
DOREG-42•100	12.0
DOREG-43•100	12.0
DOREG-44•100	12.0
DOREG-45•100	12.0
DOREG-46•100	12.0
DOREG-47•100	12.0
E-1-DATA•100	8.0
E-2-DATA•100	8.0
E-2-DATA•101	12.0
E-DATA•100	12.0
E-RS422-DRVR-0•100	20.0
E-RS422-DRVR-1•100	20.0
E-RS422-RCVR-0•100	20.0
E-RS422-RCVR-1•100	20.0
E-TND-DRVR-0•100	20.0
E-TND-DRVR-1•100	20.0
E-TND-RCVR-0•100	20.0
E-TND-RCVR-1•100	20.0
E-XACT•100	8.0
E-XACT•101	12.0
EN-ADDR-EXT•000	19.0
EN-BYTE-1•000	19.0
EN-BYTE-2•000	19.0
EN-BYTE-3•000	19.0
EN-BYTE-4•000	19.0
EN-BYTE-5•000	19.0
EN-BYTE-6•000	19.0
EN-CHAN-REQ•100	12.0
EN-CLK•000	28.0
EN-CLK•100	28.0
EN-DATA-BUS1•000	19.0
EN-DATA-BUS2•000	18.0
EN-DBUS2•100	18.0
EN-PERIPH•000	19.0
EN-PERIPH•101	19.0
EN-RAM-SEL•000	21.0
EN-STATUS-FLAGS•000	21.0
EN-STATUS-FLAGS•001	21.0
EN-TMO-1•100	32.0
EN-TMO-2•100	32.0
ENDAI-C-P0•100	35.0
ENDAI-C-P0•110	35.0
ENDAI-CSI-P0•000	35.0

DISTRIBUTION

FSCM NO. 07127-26

HONEYWELL

HONEYWELL INFORMATION SYSTEMS
LOC CEO PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- EURC8
LOGIC -
PAGE CROSS REFERENCE

DATA BASE	SIZE	DWG NO	SH	REV
L2/EURC8J	B	58065904	1.1	G
DFIG B1FE813				

58065904

REV	AUTHORITY	DATE
G	PHAODP028	82NOV10

SIGNAL NAME	PAGE
ENDAI-CSI-P1•000	35.0
ENDAI-D-P0•100	33.0
ENDAI-D-P0•110	33.0
ENDAI-D-P0•120	33.0
ENDAI-D-P1•100	34.0
ENDAI-D-P1•110	34.0
ENDAI-D-P1•120	34.0
ENDAI-DATP0-0•000	33.0
ENDAI-DATP0-1•000	33.0
ENDAI-DATP0-2•000	33.0
ENDAI-DATP0-3•000	33.0
ENDAI-DATP0-4•000	33.0
ENDAI-DATP0-5•000	33.0
ENDAI-DATP0-6•000	33.0
ENDAI-DATP0-7•000	33.0
ENDAI-DATP1-0•000	34.0
ENDAI-DATP1-1•000	34.0
ENDAI-DATP1-2•000	34.0
ENDAI-DATP1-3•000	34.0
ENDAI-DATP1-4•000	34.0
ENDAI-DATP1-5•000	34.0
ENDAI-DATP1-6•000	34.0
ENDAI-DATP1-7•000	34.0
ENDAI-DSI-P0•000	35.0
ENDAI-DSI-P1•000	35.0
ENDAI-ENI-P0•000	35.0
ENDAI-ENI-P1•000	35.0
ENDAI-EV1-P0•000	36.0
ENDAI-EV1-P0•101	36.0
ENDAI-EV1-P1•000	36.0
ENDAI-EV1-P1•101	36.0
ENDAI-EV2-P0•000	36.0
ENDAI-EV2-P0•101	36.0
ENDAI-EV2-P1•000	36.0
ENDAI-EV2-P1•101	36.0
ENDAI-EV3-P0•000	36.0
ENDAI-EV3-P1•000	36.0
ENDAI-OPI-P0•000	35.0
ENDAI-OPI-P1•000	35.0
ENDAI-PARP0•000	36.0
ENDAI-PARP1•000	34.0
FF-OBL-FLG•000	8.0
FF-OBL-FLG•100	8.0
FF-SCAN-FLG•000	8.0
FF-SCAN-FLG•001	11.0
FF-SCAN-FLG•100	8.0
FF-SCAN-FLG•101	11.0
FF1/FF2•100	31.0
FLAGS•000	8.0
FPLA-ON•100	8.0
GND-00D10	36.0
GND-00L08	32.0
GND-00T10	20.0
GND-00V08	29.0
GND-09F08	36.0
GND-09U01	28.0
GND-26R09	19.0
GND-42A07	20.0
GND-43J07	12.0
GND-50A07	20.0
GND-57R08	5.0
GND-58807	5.0
GND-58C07	15.0
GND-58N08	5.0

SIGNAL NAME	PAGE
GND-63T08	12.0
GND-66B08	7.0
GND-66C08	7.0
GND-66K08	10.0
GND-66V08	12.0
GND-66X08	12.0
GND-72F08	9.0
GND-72H08	10.0
GND-72T08	11.0
GND-75A08	9.0
GND-75D08	9.0
GND-75E08	4.0
GND-75R08	10.0
GND-75U08	4.0
GND-75V08	11.0
GND-75X08	11.0
GND-78M14	8.0
GND-81F08	5.0
GND-81G08	4.0
GND-81S08	4.0
GND-81T08	11.0
GND-84A08	9.0
GND-84B08	4.0
GND-84E08	4.0
GND-84J08	4.0
GND-84Q08	10.0
GND-84U08	4.0
GND-84W08	4.0
GND-90T10	17.0
GND-93N10	13.0
GRP-ACTV-INH•001	17.0
HI-LEVEL•100	17.0
HI-LEVEL•110	12.0
HIR-CHAN•000	17.0
HIR-CHAN•100	17.0
IBF•001	32.0
IBF•100	32.0
IN-DATA-EN•000	4.0
IND-0•100	25.0
IND-0•101	25.0
IND-1•100	25.0
IND-1•101	25.0
IND-2•100	25.0
IND-2•101	25.0
IND-3•100	25.0
IND-3•101	25.0
IND-4•100	25.0
IND-4•101	25.0
IND-5•100	25.0
IND-5•101	25.0
IND-GO•000	25.0
IND-GO•100	25.0
IND-GO•101	25.0
INTR•000	32.0
INTRP•100	19.0
INZ•001	16.0
INZ•012	16.0
INZ•101	16.0
IOM-PAR-A•100	14.0
IOM-PAR-B•100	14.0
IOM-PAR-C•100	15.0
IOM-PAR-D•100	15.0
IRQ-ADLC•000	28.0
IRQ-ADLC•101	28.0

SIGNAL NAME	PAGE
IRQ-CONBUSY•101	13.0
KILL-CHAN•000	17.0
MDAI-CONTROL-OUT•000	30.0
MDAI-CONTROL-OUT•100	31.0
MDAI-CSI•001	30.0
MDAI-CSI•100	35.0
MDAI-CSI-EV3•000	30.0
MDAI-CSO•100	30.0
MDAI-CSO-EV3•000	30.0
MDAI-DAT-0•100	32.0
MDAI-DAT-0•100	33.0
MDAI-DAT-1•100	33.0
MDAI-DAT-1•100	32.0
MDAI-DAT-2•100	33.0
MDAI-DAT-2•100	32.0
MDAI-DAT-3•100	33.0
MDAI-DAT-3•100	32.0
MDAI-DAT-4•100	33.0
MDAI-DAT-4•100	32.0
MDAI-DAT-5•100	32.0
MDAI-DAT-5•100	33.0
MDAI-DAT-6•100	32.0
MDAI-DAT-6•100	33.0
MDAI-DAT-7•100	32.0
MDAI-DAT-7•100	33.0
MDAI-DATA-IN•000	30.0
MDAI-DATA-OUT•000	30.0
MDAI-DSI•100	35.0
MDAI-DSI-RD•000	30.0
MDAI-DSI-WR•000	30.0
MDAI-DSO•100	30.0
MDAI-ENI•100	35.0
MDAI-ENO•100	35.0
MDAI-EV3•100	36.0
MDAI-EV3-LATCH•001	36.0
MDAI-EV3-LATCH•101	32.0
MDAI-EV3-LATCH•101	36.0
MDAI-OPI•100	20.0
MDAI-OPI•100	35.0
MDAI-OPO•000	32.0
MDAI-OPO•010	32.0
MDAI-OPO•100	32.0
MDAI-OPO•110	32.0
MDAI-PAR•100	36.0
MDAI-PAR•110	32.0
MDAI-PARITY-ERR•100	32.0
MDAI-PRTY•100	32.0
MDAI-RSO•100	32.0
MDAI-RSO•100	35.0
MEMORY•000	18.0
MEMORY•000	27.0
MEMORY•101	21.0
MICRO-SET•111	16.0
MICRO-TEST•100	18.0
MOVE•100	16.0
MUX-DAI-SEL•000	33.0
MUX-DAI-SEL•100	33.0
MUX-DAI-SEL•100	34.0
MUX-DAI-SEL•100	32.0
MUX-DAI-SEL•101	35.0
OBF•000	32.0
OBF•001	31.0
OBF•101	31.0
OBF-OUT•100	30.0

SIGNAL NAME	PAGE
OBF/FF2•100	31.0
ODD-PARITY•000	15.0
ODD-PARITY•100	15.0
OSC-15MHZ•100	19.0
PARITY-ERR-D1DP•100	13.0
PARITY-ERR-FLG•000	20.0
PARITY-ERR-FLG•000	15.0
PARITY-ERR-FLG•100	13.0
PCW-ACK-A•000	20.0
PCW-ACK-A•100	20.0
PCW-ACK-B•000	20.0
PCW-ACK-B•100	20.0
PCW-ACK-C•000	20.0
PCW-ACK-C•100	20.0
PCW-ACK-D•000	20.0
PCW-ACK-D•100	20.0
PCW-CK•000	13.0
PCW-CK•100	13.0
PCW-CK>•000	13.0
PCW-CK>120•000	13.0
PCW-CK>180•000	13.0
PCW-CK>180•101	13.0
PCW-CLR-A•000	20.0
PCW-CLR-B•000	20.0
PCW-CLR-C•000	20.0
PCW-CLR-D•000	20.0
PCW-CONBUSY-A•000	13.0
PCW-CONBUSY-B•000	13.0
PCW-CONBUSY-B-D•001	13.0
PCW-CONBUSY-B-D•101	13.0
PCW-CONBUSY-C•000	13.0
PCW-CONBUSY-D•000	13.0
PCW-PRESENT•100	5.0
PCW-SET•100	25.0
POSI/DAI•000	5.0
POWER-UP-RESET•000	19.0
QUIT•000	8.0
RC-VALUE•100	30.0
RD-0•100	29.0
RD-1•100	29.0
RD-C-0•000	29.0
RD-C-1•000	29.0
RD/WR•100	21.0
READ•000	18.0
READ•000	27.0
READ•001	18.0
READ•101	18.0
READY•100	19.0
RES-0•100	25.0
RESET•100	19.0
RESET•110	16.0
RESET-FF2•000	30.0
RST-DAI•000	36.0
RST-DAI•100	32.0
RST-DAI•100	36.0
RT-0•100	29.0
RT-1•100	29.0

DISTRIBUTION CODE C127-26

HONEYWELL
HONEYWELL INFORMATION SYSTEMS
LOC CEO PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- EURC8
LOGIC -
PAGE CROSS REFERENCE

DATA BASE L2/EURCBJ
DFIG 81FEB13

SIZE	DWG NO	SH	REV
B	58065904	1.2	G

58065904

REV	AUTHORITY	DATE
G	PHA00P028	82NOV10

SIGNAL NAME	PAGE
RT-C-0•000	29.0
RT-C-1•000	29.0
RX-CLOCK•100	29.0
RX-DATA•100	29.0
SAME/MIXED•000	5.0
SCAN-FLG•001	16.0
SCAN-FLG•011	16.0
SCAN-FLG•101	16.0
SD-0•100	29.0
SD-1•100	29.0
SD-C-0•000	29.0
SD-C-1•000	29.0
SEL-CHAN-2•000	5.0
SEL-DOREG•001	19.0
SEL-DOREG•101	19.0
SEL-PIC-0•000	21.0
SEL-PIT-0•000	21.0
SEL-PPI-DAI-2•000	21.0
SEL-PPI-SYS•000	21.0
SEL-PROM-0•000	21.0
SEL-PROM-1•000	21.0
SEL-PROM-2•000	21.0
SEL-PROM-3•000	21.0
SEL-PROM-4•000	21.0
SEL-PROM-5•000	21.0
SEL-PROM-6•000	21.0
SEL-PROM-7•000	21.0
SEL-PROM-TD•000	21.0
SEL-RAM-0•000	21.0
SEL-RAM-1•000	21.0
SEL-RAM-2•000	21.0
SEL-SELFT-0•000	21.0
SEL-SELFT-0•001	21.0
SEL-SELFT-1•000	21.0
SEL-SELFT-1•001	21.0
SEL-SERIAL•000	21.0
SEL-SERIAL•100	28.0
SEL-SERIAL•101	28.0
SELFT-00•100	25.0
SELFT-01•100	25.0
SELFT-EN•000	25.0
SELFT-RESET•100	25.0
SERV-PRIORITY•000	8.0
SERV-PRIORITY•100	8.0
SERV-REQ•000	19.0
SERV-REQ•100	16.0
SERV-REQ•101	16.0
SET•000	17.0
SET-FF-SCAN-FLG•000	8.0
SLC•100	32.0
STB•000	30.0
STB>600•001	30.0
STB>600•001	32.0
STB>600•100	30.0
STOP•000	8.0
STOP•100	8.0
SYS-FAULT•001	16.0
SYS-FAULT•101	16.0
TALLY-BIT-0•010	16.0
TALLY-BIT-0•100	16.0
TALLY-BIT-1•000	16.0
TALLY-BIT-1•010	16.0
TALLY-BIT-1•100	16.0
TALLY-BIT-1•110	16.0

SIGNAL NAME	PAGE
TD-FF-RST•000	16.0
TD-YANK-UP•100	20.0
TERM•000	17.0
TERM-CHAN-REQ•100	17.0
TERM-SERV-REQ•100	8.0
TIME-CLR•100	31.0
TIME-OUT•000	32.0
TIMEOUT-0•101	21.0
TIMEOUT-1•101	21.0
TIMEOUT-2•101	21.0
TMO-A•000	32.0
TMO-B•000	32.0
TMO-B•100	32.0
TND-C/DSI-CONTL•100	35.0
TND-C/DSI-CONTL•100	32.0
TND-DAI-INTR•100	36.0
TND-DAI-INTR•100	32.0
TND-PAR-DAI•100	32.0
TND-PCW-SET•100	25.0
TRANSMIT•100	27.0
TRANSMIT•100	18.0
TST-ADDR-BUS•000	27.0
TST-ADDR-IN•000	27.0
TST-ADDR-IN-00•100	27.0
TST-ADDR-IN-01•100	27.0
TST-ADDR-IN-02•100	27.0
TST-ADDR-IN-03•100	27.0
TST-ADDR-IN-04•100	27.0
TST-ADDR-IN-05•100	27.0
TST-ADDR-IN-06•100	27.0
TST-ADDR-IN-07•100	27.0
TST-ADDR-IN-08•100	27.0
TST-ADDR-IN-09•100	27.0
TST-ADDR-IN-10•100	27.0
TST-ADDR-IN-11•100	27.0
TST-ADDR-IN-12•100	27.0
TST-ADDR-IN-13•100	27.0
TST-ADDR-IN-14•100	27.0
TST-ADDR-IN-15•100	27.0
TST-ADDR-OUT-00•100	27.0
TST-ADDR-OUT-01•100	27.0
TST-ADDR-OUT-02•100	27.0
TST-ADDR-OUT-03•100	27.0
TST-ADDR-OUT-04•100	27.0
TST-ADDR-OUT-05•100	27.0
TST-ADDR-OUT-06•100	27.0
TST-ADDR-OUT-07•100	27.0
TST-ADDR-OUT-08•100	27.0
TST-ADDR-OUT-09•100	27.0
TST-ADDR-OUT-10•100	27.0
TST-ADDR-OUT-11•100	27.0
TST-ADDR-OUT-12•100	27.0
TST-ADDR-OUT-13•100	27.0
TST-ADDR-OUT-14•100	27.0
TST-ADDR-OUT-15•100	27.0
TST-ALE•000	18.0
TST-ALE•101	18.0
TST-DATA-BUS•000	27.0
TST-DATA-IN•000	27.0
TST-DATA-IN-0•100	27.0
TST-DATA-IN-1•100	27.0
TST-DATA-IN-2•100	27.0
TST-DATA-IN-3•100	27.0
TST-DATA-IN-4•100	27.0

SIGNAL NAME	PAGE
TST-DATA-IN-5•100	27.0
TST-DATA-IN-6•100	27.0
TST-DATA-IN-7•100	27.0
TST-DATA-OUT-0•100	27.0
TST-DATA-OUT-1•100	27.0
TST-DATA-OUT-2•100	27.0
TST-DATA-OUT-3•100	27.0
TST-DATA-OUT-4•100	27.0
TST-DATA-OUT-5•100	27.0
TST-DATA-OUT-6•100	27.0
TST-DATA-OUT-7•100	27.0
TST-DEN•000	27.0
TST-HOLD•000	27.0
TST-HOLD•100	27.0
TST-LATCH-EN•000	27.0
TST-LATCH-EN•001	27.0
TST-MEM•000	27.0
TST-RD•000	27.0
TST-TRANS•100	27.0
TST-WR•000	27.0
TT-0•100	29.0
TT-1•100	29.0
TT-C-0•000	29.0
TT-C-1•000	29.0
TX-DATA•100	28.0
U-ASCII-EN•000	19.0
U-BCD-EN•000	19.0
U-BUS-00•000	14.0
U-BUS-01•000	14.0
U-BUS-02•000	14.0
U-BUS-03•000	14.0
U-BUS-04•000	14.0
U-BUS-05•000	14.0
U-BUS-06•000	14.0
U-BUS-07•000	14.0
U-BUS-08•000	14.0
U-BUS-09•000	14.0
U-BUS-10•000	14.0
U-BUS-11•000	14.0
U-BUS-12•000	5.0
U-BUS-13•000	5.0
U-BUS-14•000	5.0
U-BUS-15•000	5.0
U-BUS-16•000	5.0
U-BUS-16/22•000	5.0
U-BUS-17•000	5.0
U-BUS-17/23•000	5.0
U-BUS-18•000	14.0
U-BUS-19•000	14.0
U-BUS-20•000	15.0
U-BUS-21•000	13.0
U-BUS-21•100	13.0
U-BUS-22•000	5.0
U-BUS-23•000	5.0
U-BUS-24•000	15.0
U-BUS-25•000	15.0
U-BUS-26•000	15.0
U-BUS-27•000	15.0
U-BUS-28•000	15.0
U-BUS-29•000	15.0
U-BUS-30•000	15.0
U-BUS-31•000	15.0
U-BUS-32•000	15.0
U-BUS-33•000	15.0

SIGNAL NAME	PAGE
U-BUS-34•000	15.0
U-BUS-35•000	15.0
U-BUS-BCD•100	19.0
U-BUS-BCD•100	20.0
U-BUS-PARITY•000	15.0
U-BUS-PARITY•001	15.0
U-BUS-PARITY•100	15.0
U/D-BUS-00•100	14.0
U/D-BUS-00•100	9.0
U/D-BUS-01•100	14.0
U/D-BUS-01•100	9.0
U/D-BUS-02•100	9.0
U/D-BUS-02•100	14.0
U/D-BUS-03•100	14.0
U/D-BUS-03•100	9.0
U/D-BUS-04•100	14.0
U/D-BUS-04•100	9.0
U/D-BUS-05•100	14.0
U/D-BUS-05•100	9.0
U/D-BUS-06•100	9.0
U/D-BUS-06•100	14.0
U/D-BUS-07•100	9.0
U/D-BUS-07•100	14.0
U/D-BUS-08•100	9.0
U/D-BUS-08•100	14.0
U/D-BUS-09•100	9.0
U/D-BUS-09•100	14.0
U/D-BUS-10•100	9.0
U/D-BUS-10•100	14.0
U/D-BUS-11•100	14.0
U/D-BUS-11•100	9.0
U/D-BUS-12•100	10.0
U/D-BUS-12•100	14.0
U/D-BUS-13•100	10.0
U/D-BUS-13•100	14.0
U/D-BUS-14•100	14.0
U/D-BUS-14•100	10.0
U/D-BUS-15•160	14.0
U/D-BUS-15•100	10.0
U/D-BUS-16•100	14.0
U/D-BUS-16•100	10.0
U/D-BUS-17•100	10.0
U/D-BUS-17•100	14.0
U/D-BUS-18•100	14.0
U/D-BUS-18•100	10.0
U/D-BUS-19•100	14.0
U/D-BUS-19•100	10.0
U/D-BUS-20•100	10.0
U/D-BUS-20•100	15.0
U/D-BUS-21•100	10.0
U/D-BUS-21•100	15.0
U/D-BUS-22•100	10.0
U/D-BUS-22•100	15.0
U/D-BUS-23•100	15.0
U/D-BUS-23•100	10.0
U/D-BUS-24•100	15.0
U/D-BUS-24•100	11.0

DISTRIBUTION CODE C127-26

HONEYWELL
HONEYWELL INFORMATION SYSTEMS
LOC CEO PHOENIX, ARIZONA U.S.A.

TITLE LOGIC DIAGRAM- EURCB
LOGIC -
PAGE CROSS REFERENCE

DATA BASE L2/EURCBJ
DES DFIG B1FEB13

SIZE	DWG NO	SH	REV
B	58065904	1.3	G

58065904

REV	AUTHORITY	DATE
G	PHA00P028	82NOV10

SIGNAL NAME	PAGE
U/D-BUS-25•100	11.0
U/D-BUS-25•100	15.0
U/D-BUS-26•100	15.0
U/D-BUS-26•100	11.0
U/D-BUS-27•100	11.0
U/D-BUS-27•100	15.0
U/D-BUS-28•100	11.0
U/D-BUS-28•100	15.0
U/D-BUS-29•100	15.0
U/D-BUS-29•100	11.0
U/D-BUS-30•100	11.0
U/D-BUS-30•100	15.0
U/D-BUS-31•100	11.0
U/D-BUS-31•100	15.0
U/D-BUS-32•100	11.0
U/D-BUS-32•100	15.0
U/D-BUS-33•100	11.0
U/D-BUS-33•100	15.0
U/D-BUS-34•100	15.0
U/D-BUS-34•100	11.0
U/D-BUS-35•100	11.0
U/D-BUS-35•100	15.0
USER-FLT-00•001	16.0
USER-FLT-00•101	16.0
USER-FLT-01•001	16.0
USER-FLT-01•101	16.0
USER-FLT-02•001	16.0
USER-FLT-02•101	16.0
WRITE•000	18.0
WRITE•000	27.0
XACT-BIT-27•100	17.0
XACT-BIT-28•100	17.0
XACT-BIT-29•100	17.0
XACT-BIT-31•100	17.0
XACT-BIT-31•100	17.0

DISTRIBUTION C127-26

HONEYWELL				
HONEYWELL INFORMATION SYSTEMS LOC CEO PHOENIX, ARIZONA U.S.A.				
TITLE LOGIC DIAGRAM- EURCB LOGIC - PAGE CROSS REFERENCE				
DATA BASE L2/EURCBJ	SIZE B	DWG NO 58065904	SH 1.4	REV G
DFIG BJEEB13				

58065904

TO IOM ''D'' BUS

IOM BUS SIQUENCING

FROM IOM ''U'' BUS

BUS SEQUENCER SHEETS 5,8,12,13,16*17

36 BITS DATA OUT SHEETS 9,10,11,12,14*15

CONTROL

36 BITS DATA IN SHEETS 4,6,7,14*15

CLOCK GEN SHEET 19

DATA-BUS2-00-07

RAM 6KX8 SHEET 24

TID EPROM 4KX8 SHEET 26

ADDR-08-15

ADDR-BUS-00-07

OCTAL LATCH SHEET 18

AD0-7

8088 MICRO-PROCESSOR SHEET 18

1 X 8 BIT IOM STATUS SHEET 16

SYSTEM CONTROLLER SHEET 20

TIMER AND INTERRUPT CONTROLLERS SHEETS 19*21

DATA-BUS1-0-7

XCVR SHEET 18

XCVR SHEET 18

EPROM 32K X 8 SHEETS 22,23*26

DATA-BUS2-0-7

LED LATCHES SHEET 25

DAI CONTROL SHEETS 30,31*32

ADVANCED DATA LINK CONTROLLER SHEET 28

XMIT/RCVR PORT0 DAI SHEETS 33,35*36

XMIT/RCVR PORT1 DAI SHEETS 34,35*36

XMIT/RCVR PORT0 PDSI SHEET 29

XMIT/RCVR PORT1 PDSI SHEET 29

PARALLEL

SERIAL

TO DISPLAYS

TO DEVICES

TO DEVICES

HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURCB BLOCK DIAGRAM	SIZE B	DWG NO 58065904	SH 2.0	REV G

58065904

I/O PIN		PAGE	SIGNAL NAME
LA01	I	18.0	TST-ALE•000
LA02	I	27.0	TST-ADDR-IN-14•100
LA05	I	27.0	TST-ADDR-IN-12•100
LA08	I	27.0	TST-ADDR-IN-13•100
LA09	I	27.0	TST-DATA-IN•000
LA10	I	27.0	TST-DATA-BUS•000
LA11	I	27.0	TST-ADDR-IN-07•100
LA12	O	27.0	TST-ADDR-OUT-07•100
LA13	O	25.0	IND-GO•000
LA17	I	27.0	TST-ADDR-IN-06•100
LA19	I	27.0	TST-ADDR-BUS•000
LA20	I	27.0	TST-ADDR-IN-09•100
LA21	I	27.0	TST-ADDR-IN-10•100
LB00	I	27.0	TST-RD•000
LB01	I	27.0	TST-HOLD•000
LB02	I	27.0	TST-WR•000
LB03	O	27.0	TST-ADDR-OUT-15•100
LB04	O	27.0	TST-ADDR-OUT-14•100
LB05	O	27.0	TST-ADDR-OUT-11•100
LB06	O	27.0	TST-ADDR-OUT-10•100
LB07	O	27.0	TST-ADDR-OUT-09•100
LB08	O	27.0	TST-ADDR-OUT-08•100
LB09	O	27.0	TST-ADDR-OUT-03•100
LB10	I	27.0	TST-ADDR-IN-15•100
LB11	O	27.0	TST-ADDR-OUT-02•100
LB12	O	27.0	TST-ADDR-OUT-06•100
LB13	O	27.0	TST-ADDR-OUT-01•100
LB14	O	27.0	TST-ADDR-OUT-00•100
LB15	O	27.0	TST-DATA-OUT-6•100
LB16	O	27.0	TST-DATA-OUT-5•100
LB17	O	27.0	TST-DATA-OUT-4•100
LB18	O	27.0	TST-DATA-OUT-3•100
LB19	O	27.0	TST-DATA-OUT-2•100
LB20	O	27.0	TST-DATA-OUT-0•100
LB21	O	27.0	TST-ADDR-OUT-05•100
LC00	I	29.0	RD-C-0•000
LC01	O	27.0	TST-DATA-OUT-7•100
LC02	I	27.0	TST-DATA-IN-7•100
LC03	I	29.0	RD-0•100
LC04	I	29.0	RT-0•100
LC05	I	27.0	TST-ADDR-IN-00•100
LC06	I	27.0	TST-ADDR-IN-11•100
LC08	I	27.0	TST-ADDR-IN-01•100
LC09	O	29.0	TT-0•100
LC10	I	29.0	RT-C-0•000
LC11	I	27.0	TST-ADDR-IN-02•100
LC12	O	20.0	E-RS422-DRVR-0•100
LC13	O	20.0	E-RS422-RCVR-0•100
LC14	I	27.0	TST-ADDR-IN-03•100
LC15	O	29.0	SD-0•100
LC16	O	29.0	TT-C-0•000
LC17	I	27.0	TST-ADDR-IN-04•100
LC19	O	29.0	SD-C-0•000
LC20	I	27.0	TST-ADDR-IN-05•100
LC21	O	27.0	TST-DATA-OUT-1•100
LD00	I	29.0	RD-C-1•000
LD02	I	27.0	TST-DATA-IN-0•100
LD03	I	29.0	RD-1•100
LD04	I	29.0	RT-1•100
LD05	I	27.0	TST-DATA-IN-1•100
LD06	O	28.0	CLK-1500KHZ•100
LD08	I	27.0	TST-DATA-IN-2•100
LD09	O	29.0	TT-1•100
LD10	I	29.0	RT-C-1•000

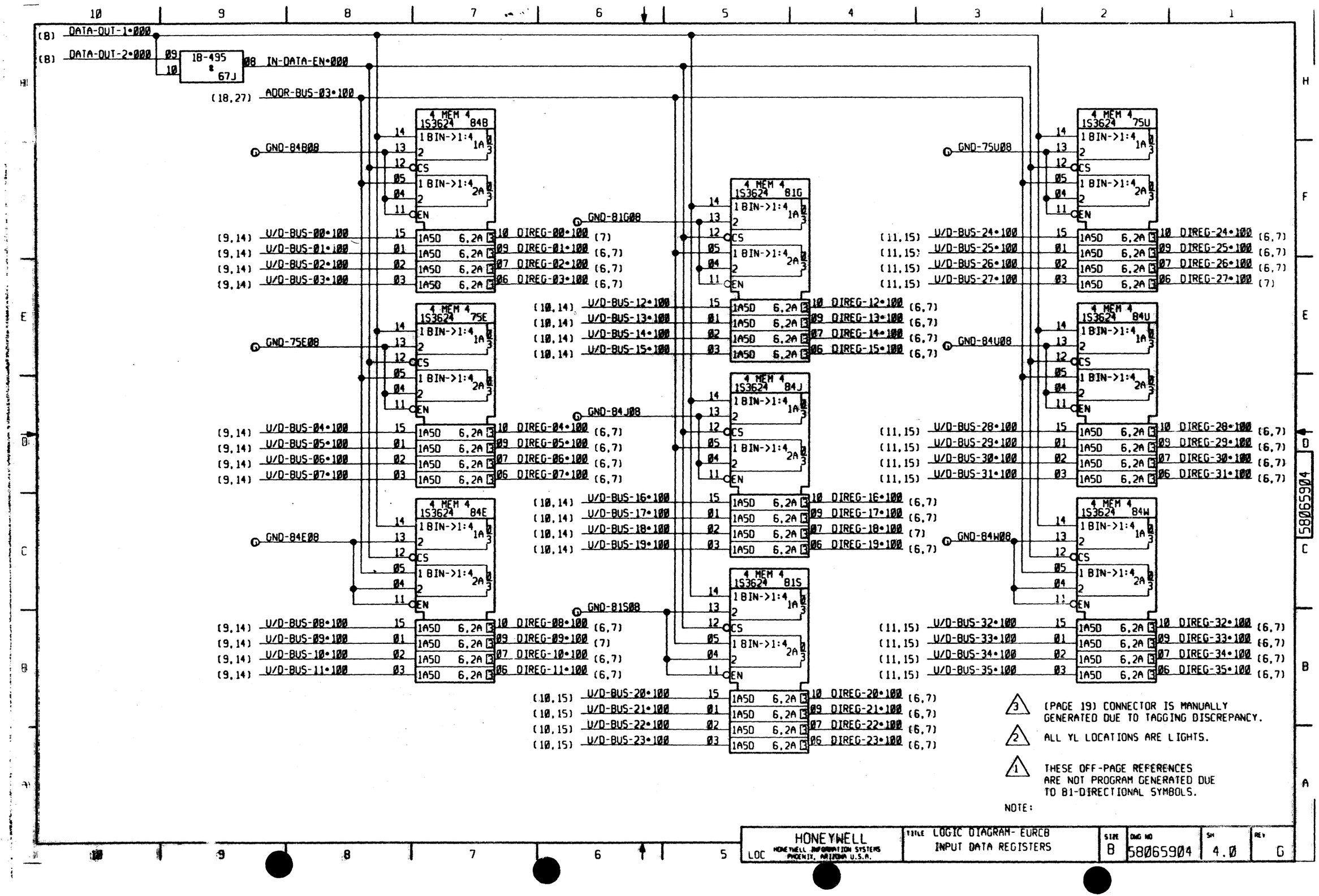
I/O PIN		PAGE	SIGNAL NAME
LD11	I	27.0	TST-DATA-IN-3•100
LD12	O	20.0	E-RS422-DRVR-1•100
LD13	O	20.0	E-RS422-RCVR-1•100
LD14	I	27.0	TST-DATA-IN-4•100
LD15	O	29.0	SD-1•100
LD16	O	29.0	TT-C-1•000
LD17	I	27.0	TST-DATA-IN-5•100
LD19	O	29.0	SD-C-1•000
LD20	I	27.0	TST-DATA-IN-6•100
LD21	I	27.0	TST-ADDR-IN•000
RA01	I	27.0	TST-LATCH-EN•000
RA04	I	27.0	TST-MEM•000
RA06	I	35.0	DAI-OPI-P0•100
RA07	I	36.0	DAI-EVI-P0•100
RA09	I	36.0	DAI-EV2-P0•100
RA10	O	35.0	DAI-OPO-P0•100
RA12	I	36.0	DAI-EV3-P0•100
RA13	I	27.0	TST-DEN•000
RA15	I	27.0	TST-TRANS•000
RA16	O	35.0	DAI-RSO-P0•100
RA18	O	35.0	DAI-ENO-P0•100
RA19	I	35.0	DAI-ENI-P0•100
RB00	O	33.0	DAI-DATP0-7•100
RB01	O	33.0	DAI-DATP0-6•100
RB03	O	33.0	DAI-DATP0-5•100
RB04	O	33.0	DAI-DATP0-4•100
RB06	I	35.0	DAI-OSI-P0•100
RB07	O	33.0	DAI-DATP0-3•100
RB09	O	33.0	DAI-DATP0-2•100
RB10	O	35.0	DAI-OSO-P0•100
RB12	O	33.0	DAI-DATP0-1•100
RB13	O	33.0	DAI-DATP0-0•100
RB15	O	33.0	DAI-PARP0•100
RB18	I	35.0	DAI-CSI-P0•100
RB19	O	35.0	DAI-CSO-P0•100
RB21	I	27.0	TST-ADDR-IN-08•100
RC01	O	27.0	TST-ADDR-OUT-12•100
RC04	O	20.0	PCW-ACK-A•000
RC06	I	35.0	DAI-OPI-P1•100
RC07	I	36.0	DAI-EVI-P1•100
RC09	I	36.0	DAI-EV2-P1•100
RC10	O	35.0	DAI-OPO-P1•100
RC12	I	36.0	DAI-EV3-P1•100
RC13	O	20.0	PCW-ACK-B•000
RC15	O	20.0	PCW-ACK-C•000
RC16	O	35.0	DAI-RSO-P1•100
RC18	O	35.0	DAI-ENO-P1•100
RC19	I	35.0	DAI-ENI-P1•100
RC21	O	20.0	PCW-ACK-D•000
RD00	O	34.0	DAI-DATP1-7•100
RD01	O	34.0	DAI-DATP1-6•100
RD03	O	34.0	DAI-DATP1-5•100
RD04	O	34.0	DAI-DATP1-4•100
RD06	I	35.0	DAI-DSI-P1•100
RD07	O	34.0	DAI-DATP1-3•100
RD09	O	34.0	DAI-DATP1-2•100
RD10	O	35.0	DAI-DSO-P1•100
RD12	O	34.0	DAI-DATP1-1•100
RD13	O	34.0	DAI-DATP1-0•100
RD15	O	33.0	DAI-PARP1•100
RD16	O	27.0	TST-ADDR-OUT-13•100
RD18	I	35.0	DAI-CSI-P1•100
RD19	O	35.0	DAI-CSO-P1•100
RD21	O	27.0	TST-ADDR-OUT-04•100

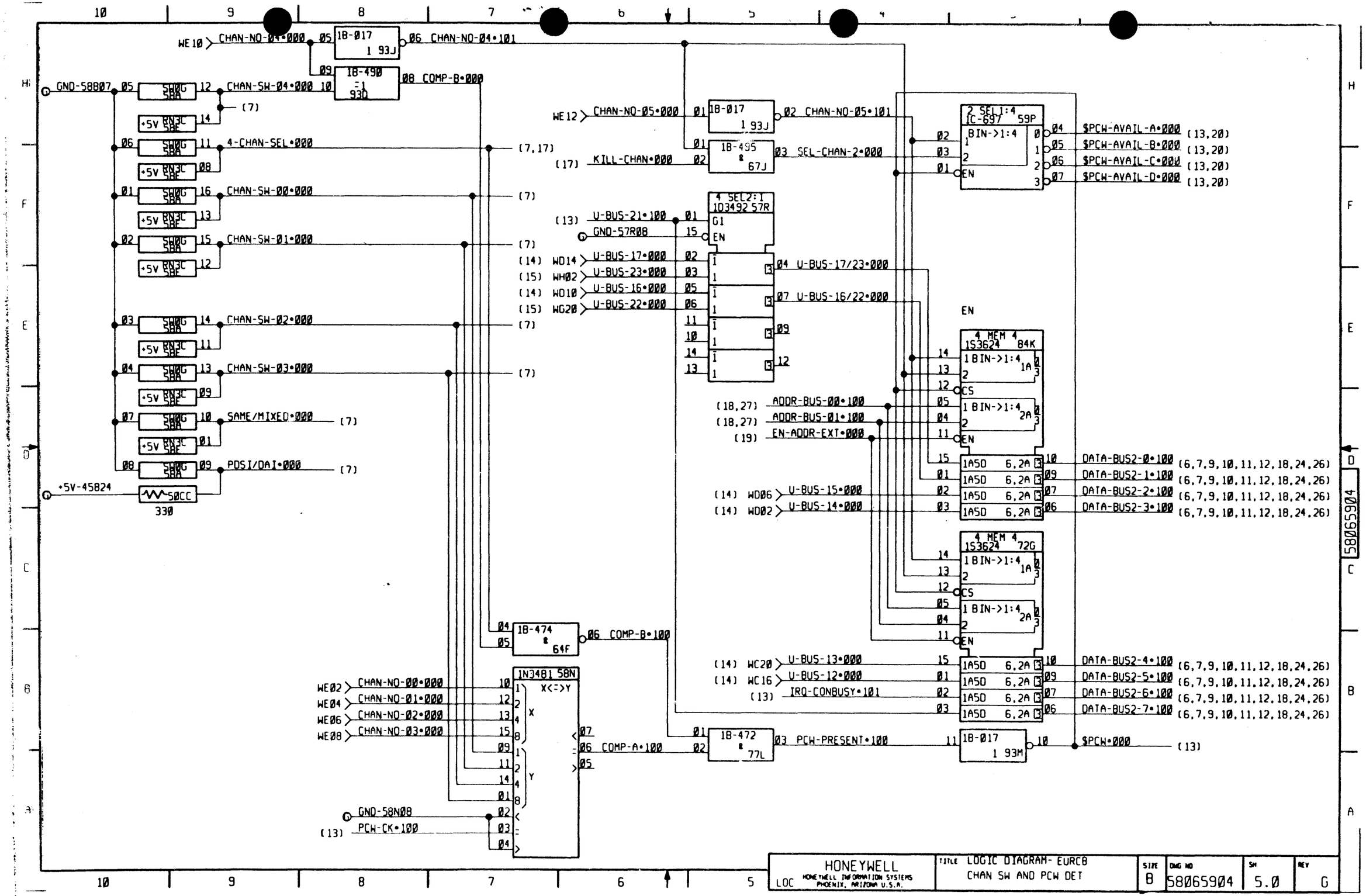
I/O PIN		PAGE	SIGNAL NAME
WA10	O	9.0	D-BUS-00•000
WA12	I	14.0	U-BUS-00•000
WA14	O	9.0	D-BUS-01•000
WA16	I	14.0	U-BUS-01•000
WA18	O	9.0	D-BUS-02•000
WA20	I	14.0	U-BUS-02•000
WB00	O	9.0	D-BUS-03•000
WB02	I	14.0	U-BUS-03•000
WB04	O	9.0	D-BUS-04•000
WB06	I	14.0	U-BUS-04•000
WB08	O	9.0	D-BUS-05•000
WB10	I	14.0	U-BUS-05•000
WB12	O	9.0	D-BUS-06•000
WB14	I	14.0	U-BUS-06•000
WB16	O	9.0	D-BUS-07•000
WB18	I	14.0	U-BUS-07•000
WB20	O	9.0	D-BUS-08•000
WC00	I	14.0	U-BUS-08•000
WC02	O	9.0	D-BUS-09•000
WC04	I	14.0	U-BUS-09•000
WC06	O	9.0	D-BUS-10•000
WC08	I	14.0	U-BUS-10•000
WC10	O	9.0	D-BUS-11•000
WC12	I	14.0	U-BUS-11•000
WC14	O	10.0	D-BUS-12•000
WC16	I	5.0	U-BUS-12•000
WC18	O	10.0	D-BUS-13•000
WC20	I	5.0	U-BUS-13•000
WD00	O	10.0	D-BUS-14•000
WD02	I	5.0	U-BUS-14•000
WD04	O	10.0	D-BUS-15•000
WD06	I	5.0	U-BUS-15•000
WD08	O	10.0	D-BUS-16•000
WD10	I	5.0	U-BUS-16•000
WD12	O	10.0	D-BUS-17•000
WD14	I	5.0	U-BUS-17•000
WD16	O	10.0	D-BUS-18•000
WD18	I	14.0	U-BUS-18•000
WD20	O	10.0	D-BUS-19•000
WE00	I	14.0	U-BUS-19•000
WE02	I	5.0	CHAN-NO-00•000
WE04	I	5.0	CHAN-NO-01•000
WE06	I	5.0	CHAN-NO-02•000
WE08	I	5.0	CHAN-NO-03•000
WE10	I	5.0	CHAN-NO-04•000
WE12	I	5.0	CHAN-NO-05•000
WE14	I	16.0	SYS-FAULT•001
WE16	I	16.0	USER-FLT-00•001
WE18	I	16.0	USER-FLT-01•001
WE20	I	16.0	USER-FLT-02•001
WE21	I	16.0	CHAN-INZ•001
WF00	O	17.0	BSP-OUT•000
WF02	I	17.0	BSP-IN-0•000
WF04	I	17.0	BSP-IN-1•000
WF06	I	17.0	BSP-IN-2•000
WF08	I	17.0	BSP-IN-3•000
WF10	I	17.0	GRP-ACTV-INH•001

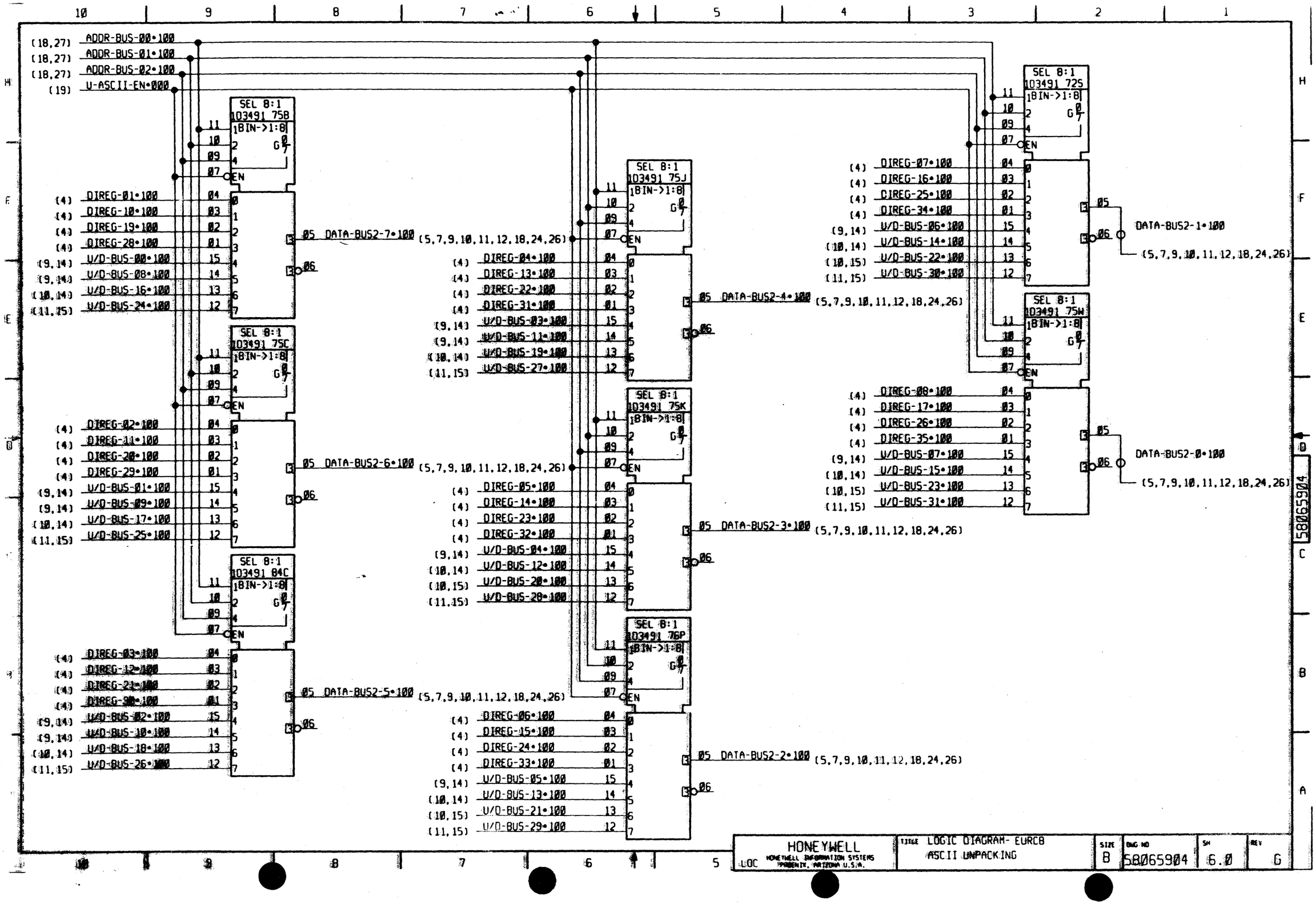
58065904

HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A. LOC	TITLE LOGIC DIAGRAM- EURC8 I/O PIN - PAGE CROSS REFERENCE	SIZE B	DWG NO 58065904	SH 3.0	REV G

I/O PIN		PAGE	SIGNAL NAME
WF14	I	16.0	SCAN-FLG•001
WF18	I	16.0	DATA-FLAG•001
WG02	I	16.0	DBL-FLG•001
WG04	O	17.0	CHAN-REQ•000
WG06	I	16.0	TALLY-BIT-0•010
WG08	I	16.0	TALLY-BIT-1•010
WG10	O	10.0	D-BUS-20•000
WG12	I	15.0	U-BUS-20•000
WG14	O	10.0	D-BUS-21•000
WG16	I	13.0	U-BUS-21•000
WG18	O	10.0	D-BUS-22•000
WG20	I	5.0	U-BUS-22•000
WH00	O	10.0	D-BUS-23•000
WH02	I	5.0	U-BUS-23•000
WH04	O	11.0	D-BUS-24•000
WH06	I	15.0	U-BUS-24•000
WH08	O	11.0	D-BUS-25•000
WH10	I	15.0	U-BUS-25•000
WH12	O	11.0	D-BUS-26•000
WH14	I	15.0	U-BUS-26•000
WH16	O	11.0	D-BUS-27•000
WH18	I	15.0	U-BUS-27•000
WH20	O	11.0	D-BUS-28•000
WJ00	I	15.0	U-BUS-28•000
WJ02	O	11.0	D-BUS-29•000
WJ04	I	15.0	U-BUS-29•000
WJ06	O	11.0	D-BUS-30•000
WJ08	I	15.0	U-BUS-30•000
WJ10	O	11.0	D-BUS-31•000
WJ12	I	15.0	U-BUS-31•000
WJ14	O	11.0	D-BUS-32•000
WJ16	I	15.0	U-BUS-32•000
WJ18	O	11.0	D-BUS-33•000
WJ20	I	15.0	U-BUS-33•000
WK00	O	11.0	D-BUS-34•000
WK02	I	15.0	U-BUS-34•000
WK04	O	11.0	D-BUS-35•000
WK06	I	15.0	U-BUS-35•000
WK08	O	15.0	D-BUS-PARITY•000
WK10	I	15.0	U-BUS-PARITY•000
WZ00	I	16.0	CHAN-INZ•001
YL01	O	25.0	IND-0•101
YL03	O	25.0	IND-1•101
YL05	O	25.0	IND-2•101
YL09	O	25.0	IND-3•101
YL11	O	25.0	IND-4•101
YL13	O	25.0	IND-5•101
YL17	O	25.0	IND-GO•101


10 9 8 7 6 5 4 3 2 1
(8) DATA-OUT-1•000
(8) DATA-OUT-2•000
09
10
18-495
67J
08 IN-DATA-EN•000
(18,27) ADDR-BUS-03•100
4 MEM 4 1S3624 84B
4 MEM 4 1S3624 81G
4 MEM 4 1S3624 84J
4 MEM 4 1S3624 81S
4 MEM 4 1S3624 75U
4 MEM 4 1S3624 75E
4 MEM 4 1S3624 84U
4 MEM 4 1S3624 84E
4 MEM 4 1S3624 84W
1 BIN->1:4 1A
1 BIN->1:4 2A
CS
EN
1A5D 6,2A
GND-84B08
GND-81G08
GND-84J08
GND-81S08
GND-75U08
GND-75E08
GND-84U08
GND-84E08
GND-84W08
(9,14) U/D-BUS-00•100
(9,14) U/D-BUS-01•100
(9,14) U/D-BUS-02•100
(9,14) U/D-BUS-03•100
10 DIREG-00•100 (7)
09 DIREG-01•100 (6,7)
07 DIREG-02•100 (6,7)
06 DIREG-03•100 (6,7)
(10,14) U/D-BUS-12•100
(10,14) U/D-BUS-13•100
(10,14) U/D-BUS-14•100
(10,14) U/D-BUS-15•100
10 DIREG-12•100 (6,7)
09 DIREG-13•100 (6,7)
07 DIREG-14•100 (6,7)
06 DIREG-15•100 (6,7)
(11,15) U/D-BUS-24•100
(11,15) U/D-BUS-25•100
(11,15) U/D-BUS-26•100
(11,15) U/D-BUS-27•100
10 DIREG-24•100 (6,7)
09 DIREG-25•100 (6,7)
07 DIREG-26•100 (6,7)
06 DIREG-27•100 (7)
(9,14) U/D-BUS-04•100
(9,14) U/D-BUS-05•100
(9,14) U/D-BUS-06•100
(9,14) U/D-BUS-07•100
10 DIREG-04•100 (6,7)
09 DIREG-05•100 (6,7)
07 DIREG-06•100 (6,7)
06 DIREG-07•100 (6,7)
(10,14) U/D-BUS-16•100
(10,14) U/D-BUS-17•100
(10,14) U/D-BUS-18•100
(10,14) U/D-BUS-19•100
10 DIREG-16•100 (6,7)
09 DIREG-17•100 (6,7)
07 DIREG-18•100 (7)
06 DIREG-19•100 (6,7)
(11,15) U/D-BUS-28•100
(11,15) U/D-BUS-29•100
(11,15) U/D-BUS-30•100
(11,15) U/D-BUS-31•100
10 DIREG-28•100 (6,7)
09 DIREG-29•100 (6,7)
07 DIREG-30•100 (6,7)
06 DIREG-31•100 (6,7)
(9,14) U/D-BUS-08•100
(9,14) U/D-BUS-09•100
(9,14) U/D-BUS-10•100
(9,14) U/D-BUS-11•100
10 DIREG-08•100 (6,7)
09 DIREG-09•100 (7)
07 DIREG-10•100 (6,7)
06 DIREG-11•100 (6,7)
(10,15) U/D-BUS-20•100
(10,15) U/D-BUS-21•100
(10,15) U/D-BUS-22•100
(10,15) U/D-BUS-23•100
10 DIREG-20•100 (6,7)
09 DIREG-21•100 (6,7)
07 DIREG-22•100 (6,7)
06 DIREG-23•100 (6,7)
(11,15) U/D-BUS-32•100
(11,15) U/D-BUS-33•100
(11,15) U/D-BUS-34•100
(11,15) U/D-BUS-35•100
10 DIREG-32•100 (6,7)
09 DIREG-33•100 (6,7)
07 DIREG-34•100 (6,7)
06 DIREG-35•100 (6,7)
3 (PAGE 19) CONNECTOR IS MANUALLY GENERATED DUE TO TAGGING DISCREPANCY.
2 ALL YL LOCATIONS ARE LIGHTS.
1 THESE OFF-PAGE REFERENCES ARE NOT PROGRAM GENERATED DUE TO BI-DIRECTIONAL SYMBOLS.
NOTE:
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- EURC8 INPUT DATA REGISTERS
SIZE B
DWG NO 58065904
SH 4.0
REV G
58065904


WE10 CHAN-NO-04•000
1B-017 1 93J
06 CHAN-NO-04•101
1B-490 E1 930
08 COMP-B•000
GND-58B07
SH0G 5BA
12 CHAN-SW-04•000
(7)
+5V RN3C 5AE
14
06 SH0G 5BA
11 4-CHAN-SEL•000
(7,17)
08
01 SH0G 5BA
16 CHAN-SW-00•000
(7)
13
02 SH0G 5BA
15 CHAN-SW-01•000
(7)
12
03 SH0G 5BA
14 CHAN-SW-02•000
(7)
11
04 SH0G 5BA
13 CHAN-SW-03•000
(7)
09
07 SH0G 5BA
10 SAME/MIXED•000
(7)
01
08 SH0G 5BA
09 PDSI/DAI•000
(7)
+5V-45824
50CC 330
WE12 CHAN-NO-05•000
1B-017 1 93J
02 CHAN-NO-05•101
(17) KILL-CHAN•000
1B-495 E 67J
03 SEL-CHAN-2•000
2 SEL 1:4 IC-697 59P
BIN->1:4
$PCW-AVAIL-A•000 (13,20)
$PCW-AVAIL-B•000 (13,20)
$PCW-AVAIL-C•000 (13,20)
$PCW-AVAIL-D•000 (13,20)
EN
4 SEL 2:1 103492 57R
(13) U-BUS-21•100
GND-57R08
G1
EN
(14) WD14 U-BUS-17•000
(15) WH02 U-BUS-23•000
(14) WD10 U-BUS-16•000
(15) WG20 U-BUS-22•000
04 U-BUS-17/23•000
07 U-BUS-16/22•000
09
12
EN
4 MEM 4 1S3624 84K
(18,27) ADDR-BUS-00•100
(18,27) ADDR-BUS-01•100
(19) EN-ADDR-EXT•000
1 BIN->1:4 1A
1 BIN->1:4 2A
CS
EN
1A5D 6.2A
DATA-BUS2-0•100 (6,7,9,10,11,12,18,24,26)
DATA-BUS2-1•100 (6,7,9,10,11,12,18,24,26)
DATA-BUS2-2•100 (6,7,9,10,11,12,18,24,26)
DATA-BUS2-3•100 (6,7,9,10,11,12,18,24,26)
(14) WD06 U-BUS-15•000
(14) WD02 U-BUS-14•000
4 MEM 4 1S3624 72G
(14) WC20 U-BUS-13•000
(14) WC16 U-BUS-12•000
(13) IRQ-CONBUSY•101
DATA-BUS2-4•100 (6,7,9,10,11,12,18,24,26)
DATA-BUS2-5•100 (6,7,9,10,11,12,18,24,26)
DATA-BUS2-6•100 (6,7,9,10,11,12,18,24,26)
DATA-BUS2-7•100 (6,7,9,10,11,12,18,24,26)
1B-474 E 64F
06 COMP-B•100
1N3481 58N
X<=>Y
WE02 CHAN-NO-00•000
WE04 CHAN-NO-01•000
WE06 CHAN-NO-02•000
WE08 CHAN-NO-03•000
X
Y
07
06 COMP-A•100
05
GND-58N08
(13) PCW-CK•100
1B-472 E 77L
03 PCW-PRESENT•100
1B-017 1 93M
$PCW•000 (13)
58065904
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- EURC8 CHAN SW AND PCW DET
SIZE B
DWG NO 58065904
SH 5.0
REV G


ADDR-BUS-00•100
ADDR-BUS-01•100
ADDR-BUS-02•100
U-ASCII-EN•000
SEL 8:1 103491 75B
SEL 8:1 103491 75C
SEL 8:1 103491 84C
SEL 8:1 103491 75J
SEL 8:1 103491 75K
SEL 8:1 103491 76P
SEL 8:1 103491 72S
SEL 8:1 103491 75H
SEL 8:1 103491 75L
DIREG-01•100
DIREG-10•100
DIREG-19•100
DIREG-28•100
U/D-BUS-00•100
U/D-BUS-08•100
U/D-BUS-16•100
U/D-BUS-24•100
DIREG-02•100
DIREG-11•100
DIREG-20•100
DIREG-29•100
U/D-BUS-01•100
U/D-BUS-09•100
U/D-BUS-17•100
U/D-BUS-25•100
DIREG-03•100
DIREG-12•100
DIREG-21•100
DIREG-30•100
U/D-BUS-02•100
U/D-BUS-10•100
U/D-BUS-18•100
U/D-BUS-26•100
DIREG-04•100
DIREG-13•100
DIREG-22•100
DIREG-31•100
U/D-BUS-03•100
U/D-BUS-11•100
U/D-BUS-19•100
U/D-BUS-27•100
DIREG-05•100
DIREG-14•100
DIREG-23•100
DIREG-32•100
U/D-BUS-04•100
U/D-BUS-12•100
U/D-BUS-20•100
U/D-BUS-28•100
DIREG-06•100
DIREG-15•100
DIREG-24•100
DIREG-33•100
U/D-BUS-05•100
U/D-BUS-13•100
U/D-BUS-21•100
U/D-BUS-29•100
DIREG-07•100
DIREG-16•100
DIREG-25•100
DIREG-34•100
U/D-BUS-06•100
U/D-BUS-14•100
U/D-BUS-22•100
U/D-BUS-30•100
DIREG-08•100
DIREG-17•100
DIREG-26•100
DIREG-35•100
U/D-BUS-07•100
U/D-BUS-15•100
U/D-BUS-23•100
U/D-BUS-31•100
DATA-BUS2-7•100
DATA-BUS2-6•100
DATA-BUS2-5•100
DATA-BUS2-4•100
DATA-BUS2-3•100
DATA-BUS2-2•100
DATA-BUS2-1•100
DATA-BUS2-0•100
(5,7,9,10,11,12,18,24,26)
HONEYWELL
LOGIC DIAGRAM- EURCB
ASCII UNPACKING
58065904
6.0
G

(18,27) ADDR-BUS-00•100
(18,27) ADDR-BUS-01•100
(18,27) ADDR-BUS-02•100
(19) U-BCD-EN•000

SEL 8:1 1D3491 66B
SEL 8:1 1D3491 66C
SEL 8:1 1D3491 66E
SEL 8:1 1D3491 63G
SEL 8:1 1D3491 63H
SEL 8:1 1D3491 63S
SEL 8:1 1D3491 66U
SEL 8:1 1D3491 66W

GND-66B08
GND-66C08

(35) DAI-OPO-P0-FLT•000
(5) CHAN-SW-00•000
(35) DAI-OPO-P1-FLT•000
(5) CHAN-SW-01•000
(4) DIREG-00•100
(4) DIREG-06•100
(4) DIREG-12•100
(4) DIREG-18•100
(4) DIREG-24•100
(4) DIREG-30•100
(16) SYS-FAULT•101
(5) CHAN-SW-02•000

(4) DIREG-01•100
(4) DIREG-07•100
(4) DIREG-13•100
(4) DIREG-19•100
(4) DIREG-25•100
(4) DIREG-31•100
(5) CHAN-SW-03•000
(4) DIREG-02•100
(4) DIREG-08•100
(4) DIREG-14•100
(4) DIREG-20•100
(4) DIREG-26•100
(4) DIREG-32•100
(11,15) U/D-BUS-32•100
(5) CHAN-SW-04•000
(4) DIREG-03•100
(4) DIREG-09•100
(4) DIREG-15•100
(4) DIREG-21•100
(4) DIREG-27•100
(4) DIREG-33•100
(11,15) U/D-BUS-33•100
(5) 4-CHAN-SEL•000

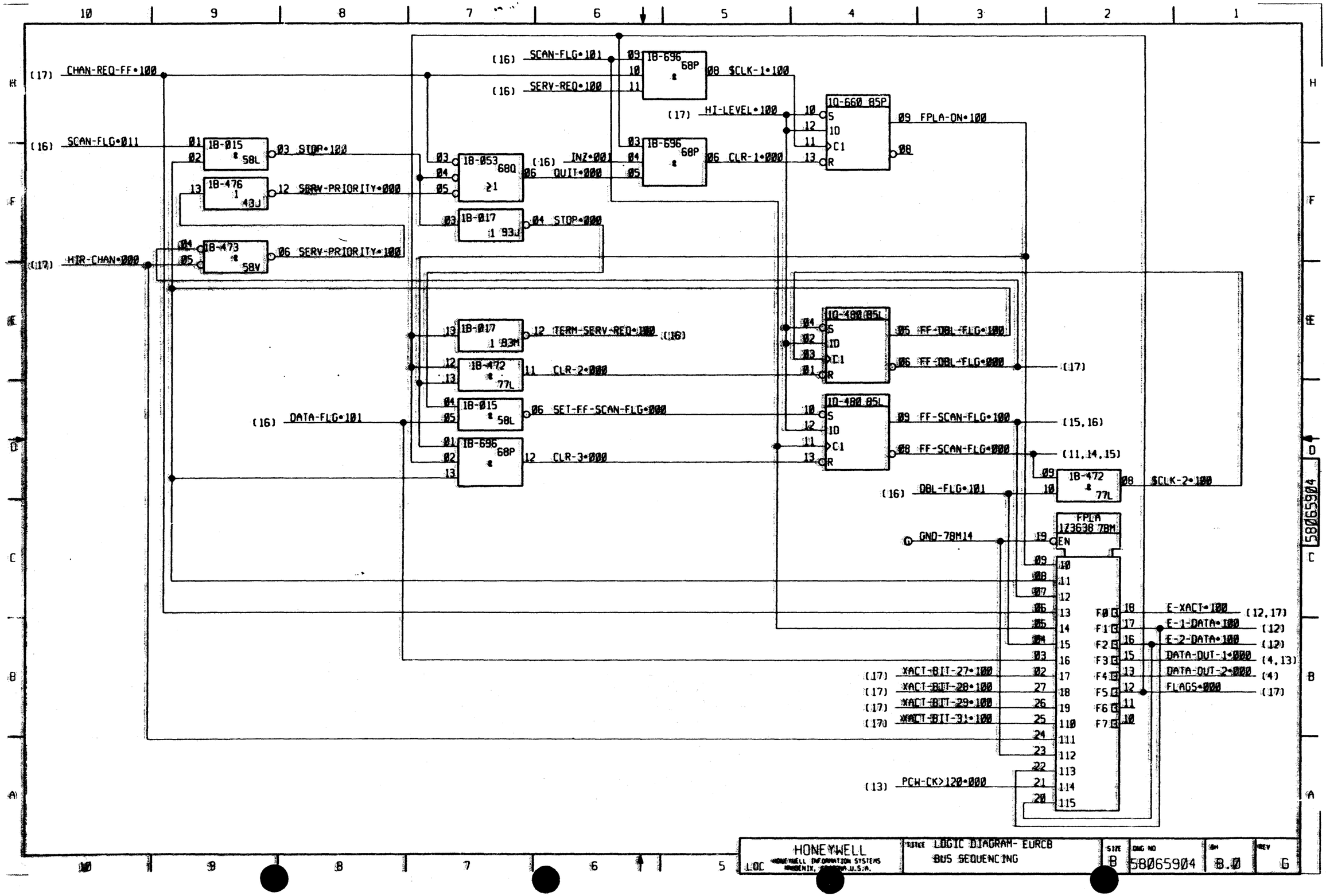
(4) DIREG-04•100
(4) DIREG-10•100
(4) DIREG-16•100
(4) DIREG-22•100
(4) DIREG-28•100
(4) DIREG-34•100
(11,15) U/D-BUS-34•100
(5) SAME/MIXED•000
(4) DIREG-05•100
(4) DIREG-11•100
(4) DIREG-17•100
(4) DIREG-23•100
(4) DIREG-29•100
(4) DIREG-35•100
(11,15) U/D-BUS-35•100
(5) POSI/DAI•000

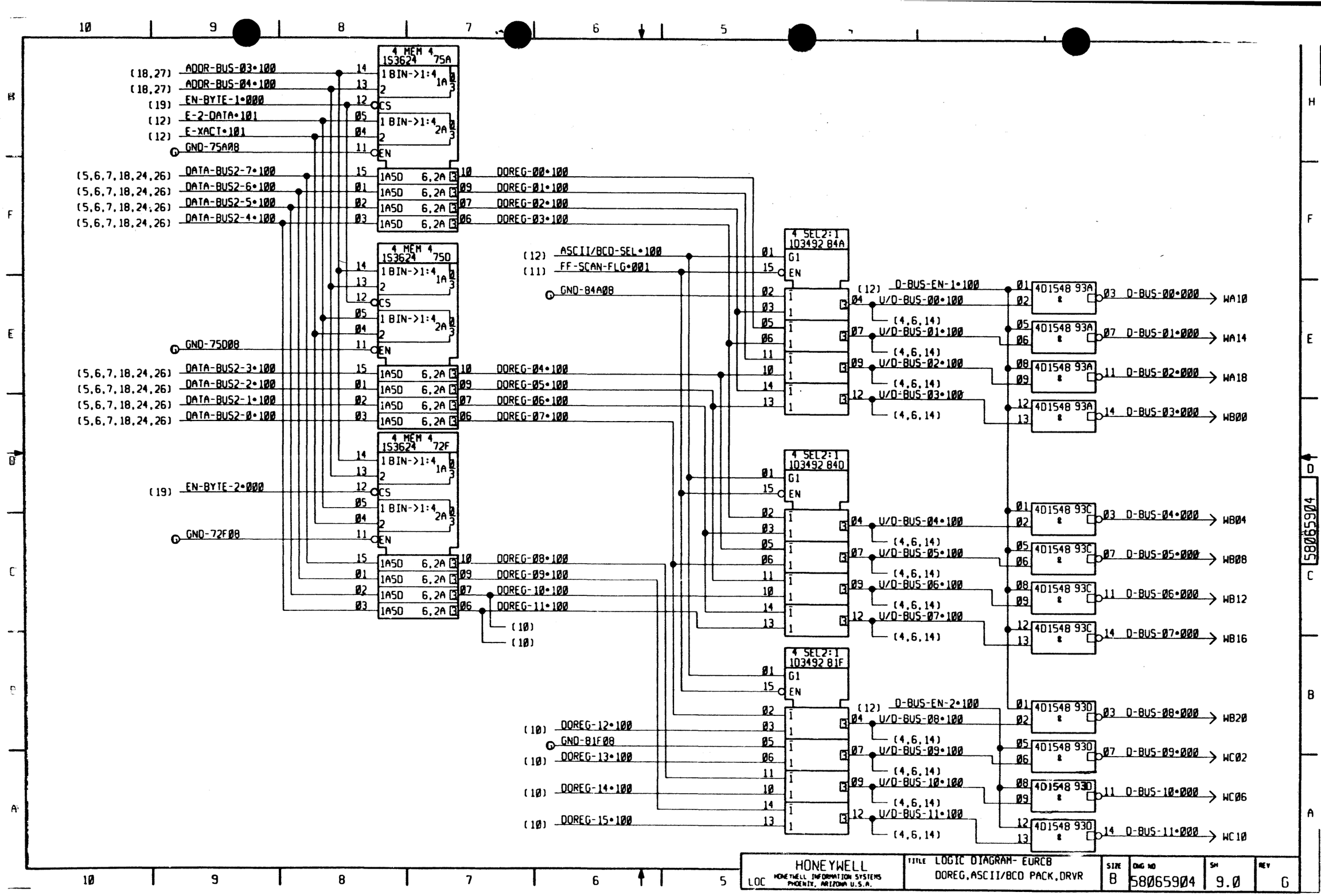
05 DATA-BUS2-7•100 (5,6,9,10,11,12,18,24,26)
05 DATA-BUS2-6•100 (5,6,9,10,11,12,18,24,26)
05 DATA-BUS2-5•100 (5,6,9,10,11,12,18,24,26)
05 DATA-BUS2-4•100 (5,6,9,10,11,12,18,24,26)
05 DATA-BUS2-3•100 (5,6,9,10,11,12,18,24,26)
05 DATA-BUS2-2•100 (5,6,9,10,11,12,18,24,26)
05 DATA-BUS2-1•100 (5,6,9,10,11,12,18,24,26)
05 DATA-BUS2-0•100 (5,6,9,10,11,12,18,24,26)

06

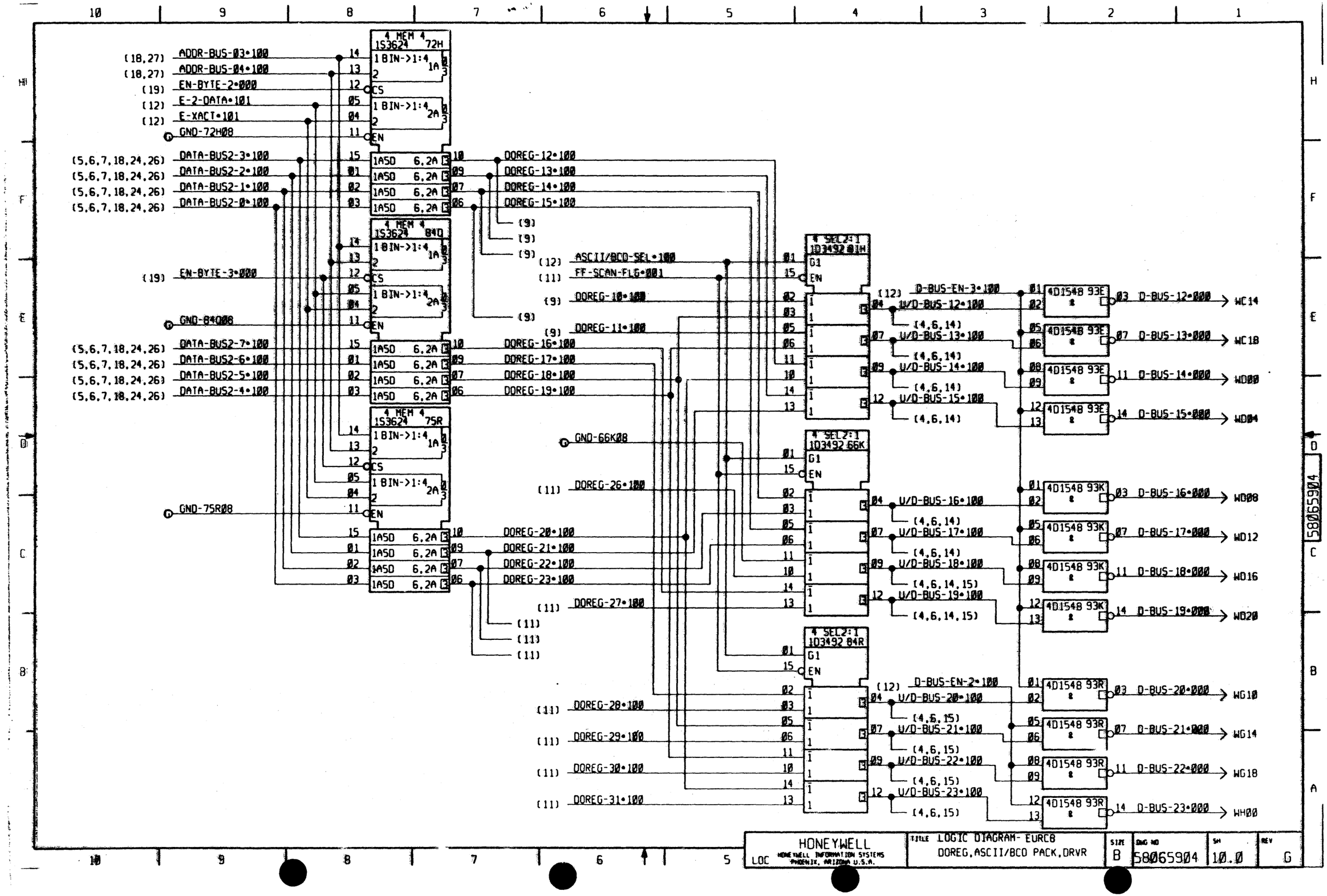
58065904

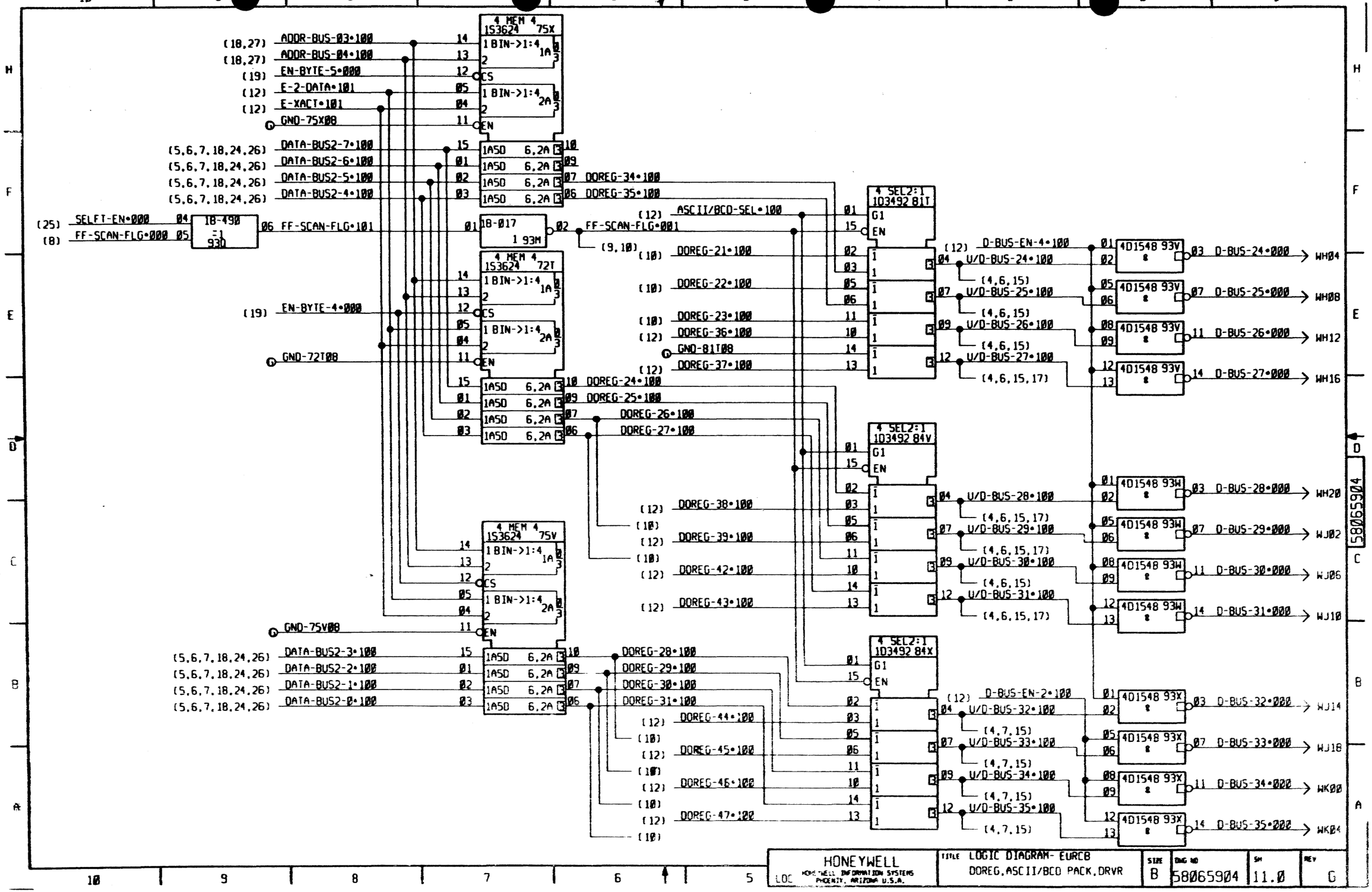
HONEYWELL LOC — HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURCB BCD UNPACKING	SIZE B	DWG NO 58065904	SH 7.0	REV G

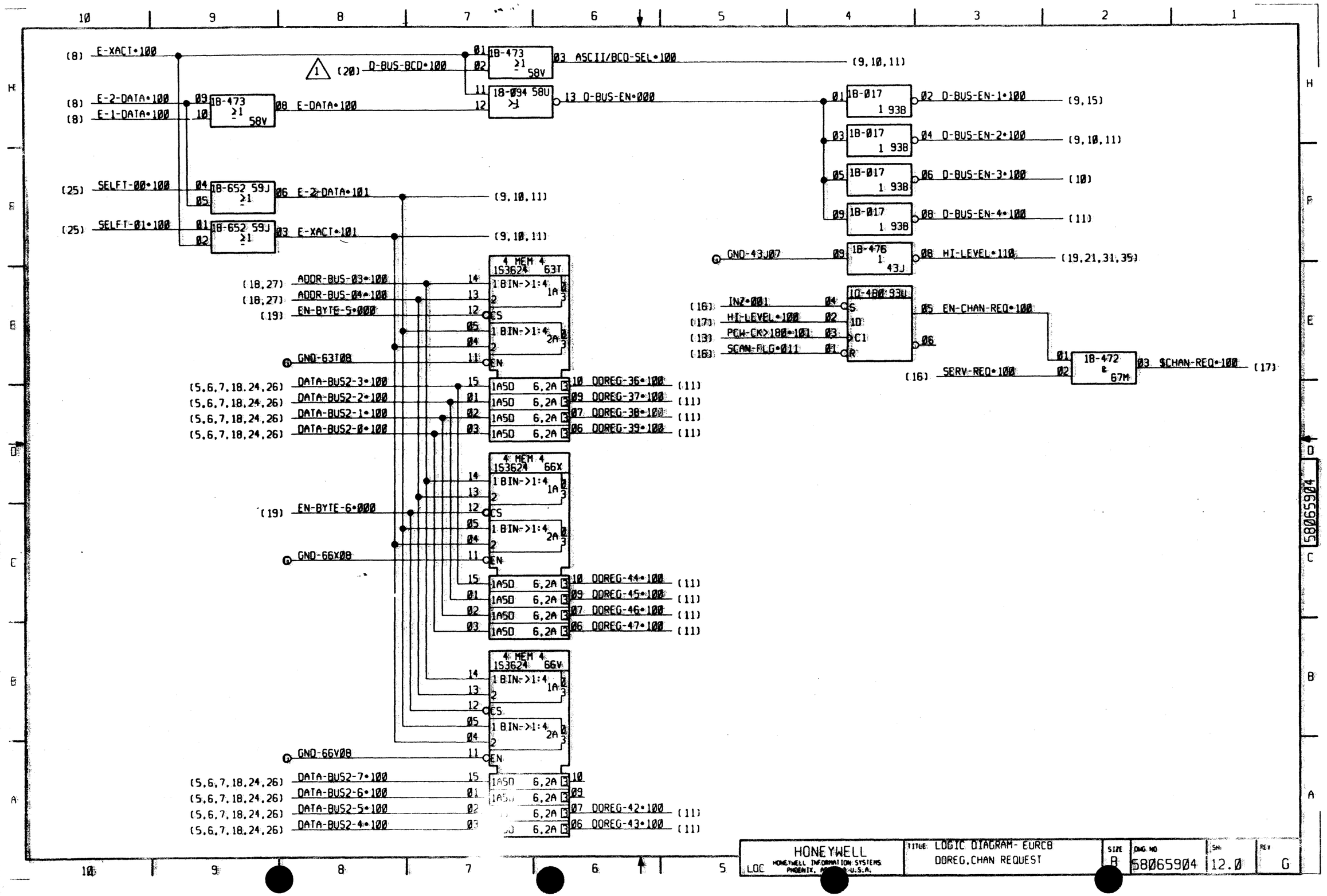

(16) SCAN-FLG•101
(17) CHAN-REQ-FF•100
(16) SERV-REQ•100
1B-696 68P
09
10
11
08 $CLK-1•100
(17) HI-LEVEL•100
10-660 B5P
10
12
11
13
S
ID
C1
R
09 FPLA-ON•100
08
(16) SCAN-FLG•011
1B-015 58L
01
02
03 STOP•100
1B-476 1 48J
13
12 SERV-PRIORITY•000
1B-053 68Q ≥1
03
04
05
06 (16) INZ•001
QUIT•000
1B-696 68P
03
04
05
06 CLR-1•000
1B-017 1 93J
03
04 STOP•000
(17) HIR-CHAN•000
1B-473 58V
04
05
06 SERV-PRIORITY•100
1B-017 1 93M
13
12 TERM-SERV-REQ•100 (16)
1B-472 77L
12
13
11 CLR-2•000
10-480 B5L
04
02
03
01
S
ID
C1
R
05 FF-DBL-FLG•100
06 FF-DBL-FLG•000
(17)
(16) DATA-FLG•101
1B-015 58L
04
05
06 SET-FF-SCAN-FLG•000
10-480 B5L
10
12
11
13
09 FF-SCAN-FLG•100
08 FF-SCAN-FLG•000
(15,16)
(11,14,15)
1B-696 68P
01
02
13
12 CLR-3•000
1B-472 77L
09
10
08 $CLK-2•100
(16) DBL-FLG•101
GND-78M14
FPLA 173638 78M
19
EN
09
08
07
06
05
04
03
02
27
26
25
24
23
22
21
20
10
11
12
13
14
15
16
17
18
19
110
111
112
113
114
115
(17) XACT-BIT-27•100
(17) XACT-BIT-28•100
(17) XACT-BIT-29•100
(17) XACT-BIT-31•100
(13) PCH-CK>120•000
F0 18 E-XACT•100 (12,17)
F1 17 E-1-DATA•100 (12)
F2 16 E-2-DATA•100 (12)
F3 15 DATA-OUT-1•000 (4,13)
F4 13 DATA-OUT-2•000 (4)
F5 12 FLAGS•000 (17)
F6 11
F7 10
10 9 8 7 6 5 4 3 2 1
H F E D C B A
58065904
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC
LOGIC DIAGRAM- EURCB
BUS SEQUENCING
SIZE B
DWG NO 58065904
REV B.0
REV G

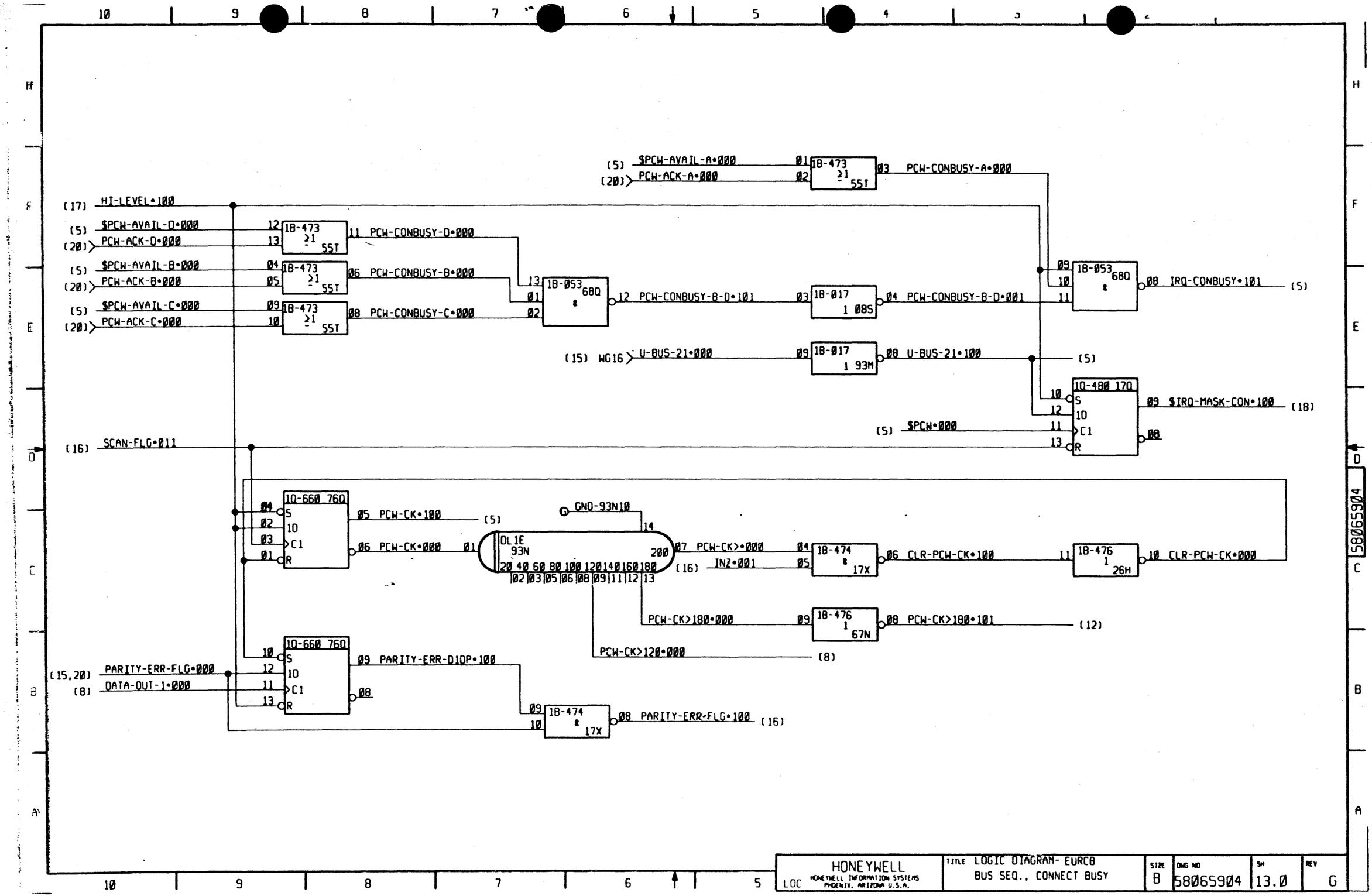


HONEYWELL LOC — HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURCB DOREG,ASCII/BCD PACK,DRVR	SIZE B	DWG NO 58065904	SH 9.0	REV G


4 MEM 4 1S3624 72H
4 MEM 4 1S3624 84Q
4 MEM 4 1S3624 75R
4 MEM 4 1S3624 66K
4 MEM 4 1S3624 84R
1 BIN->1:4 1A
1 BIN->1:4 2A
1ASD 6,2A
4 SEL2:1 1D3492 81H
4 SEL2:1 1D3492 66K
4 SEL2:1 1D3492 84R
4D1548 93E
4D1548 93K
4D1548 93R
(18,27) ADDR-BUS-03•100
(18,27) ADDR-BUS-04•100
(19) EN-BYTE-2•000
(12) E-2-DATA•101
(12) E-XACT•101
GND-72H08
(5,6,7,18,24,26) DATA-BUS2-3•100
(5,6,7,18,24,26) DATA-BUS2-2•100
(5,6,7,18,24,26) DATA-BUS2-1•100
(5,6,7,18,24,26) DATA-BUS2-0•100
(19) EN-BYTE-3•000
GND-84Q08
(5,6,7,18,24,26) DATA-BUS2-7•100
(5,6,7,18,24,26) DATA-BUS2-6•100
(5,6,7,18,24,26) DATA-BUS2-5•100
(5,6,7,18,24,26) DATA-BUS2-4•100
GND-75R08
DOREG-12•100
DOREG-13•100
DOREG-14•100
DOREG-15•100
DOREG-16•100
DOREG-17•100
DOREG-18•100
DOREG-19•100
DOREG-20•100
DOREG-21•100
DOREG-22•100
DOREG-23•100
(12) ASCII/BCD-SEL•100
(11) FF-SCAN-FLG•001
(9) DOREG-10•100
(9) DOREG-11•100
GND-66K08
(11) DOREG-26•100
(11) DOREG-27•100
(11) DOREG-28•100
(11) DOREG-29•100
(11) DOREG-30•100
(11) DOREG-31•100
(12) D-BUS-EN-3•100
U/D-BUS-12•100
U/D-BUS-13•100
U/D-BUS-14•100
U/D-BUS-15•100
U/D-BUS-16•100
U/D-BUS-17•100
U/D-BUS-18•100
U/D-BUS-19•100
(12) D-BUS-EN-2•100
U/D-BUS-20•100
U/D-BUS-21•100
U/D-BUS-22•100
U/D-BUS-23•100
(4,6,14)
(4,6,14,15)
(4,6,15)
D-BUS-12•000 → WC14
D-BUS-13•000 → WC18
D-BUS-14•000 → WD00
D-BUS-15•000 → WD04
D-BUS-16•000 → WD08
D-BUS-17•000 → WD12
D-BUS-18•000 → WD16
D-BUS-19•000 → WD20
D-BUS-20•000 → WG10
D-BUS-21•000 → WG14
D-BUS-22•000 → WG18
D-BUS-23•000 → WH00
HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- EURCB
DOREG,ASCII/BCD PACK,DRVR
SIZE B
DWG NO 58065904
SH 10.0
REV G
58065904

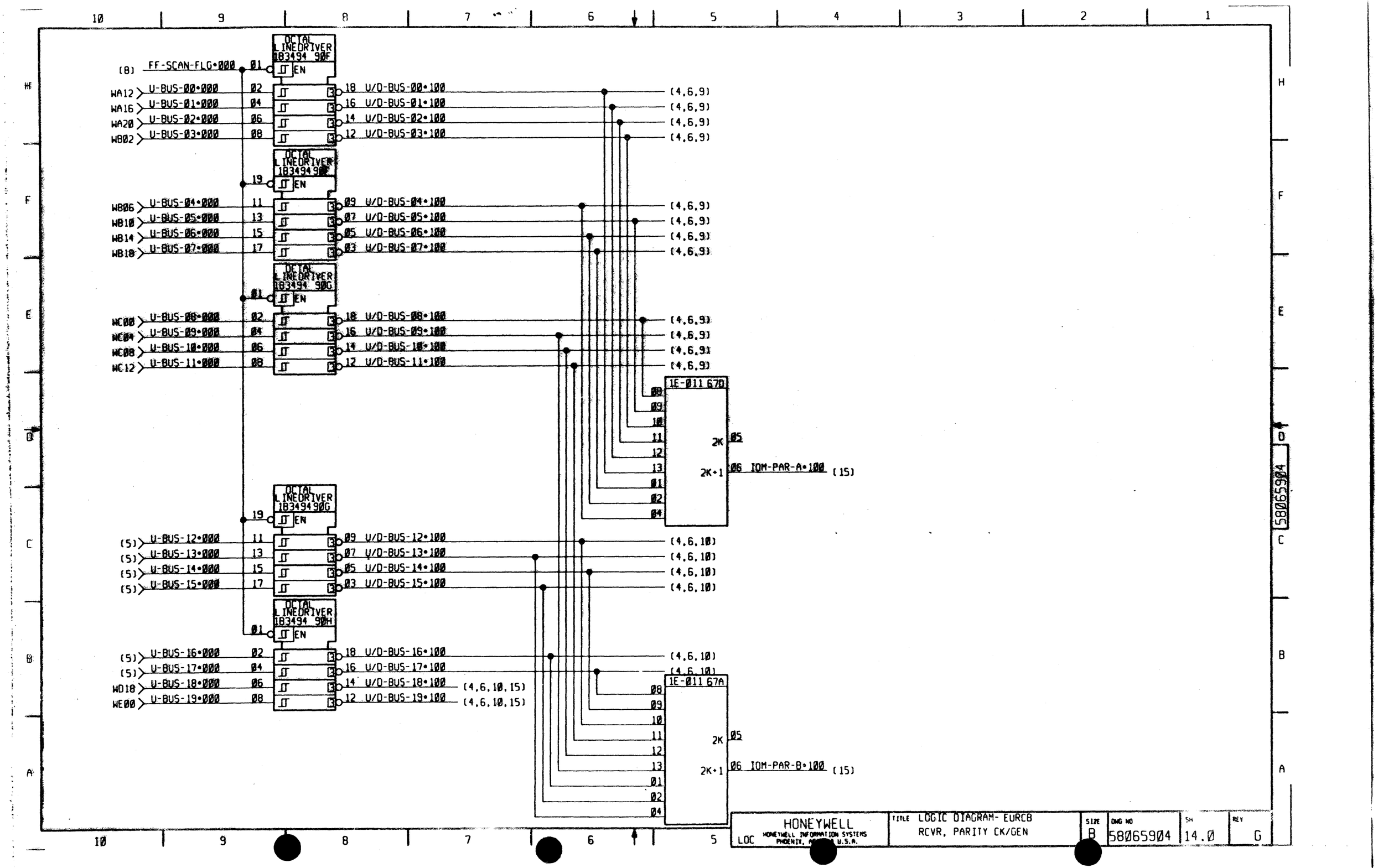

4 MEM 4 153624 75X
4 MEM 4 153624 72T
4 MEM 4 153624 75V
1 BIN->1:4 1A
1 BIN->1:4 2A
CS
EN
1A5D 6,2A
(18,27) ADDR-BUS-03•100
(18,27) ADDR-BUS-04•100
(19) EN-BYTE-5•000
(12) E-2-DATA•101
(12) E-XACT•101
GND-75X00
(5,6,7,18,24,26) DATA-BUS2-7•100
(5,6,7,18,24,26) DATA-BUS2-6•100
(5,6,7,18,24,26) DATA-BUS2-5•100
(5,6,7,18,24,26) DATA-BUS2-4•100
(25) SELFT-EN•000
(8) FF-SCAN-FLG•000
18-490 E1 930
FF-SCAN-FLG•101
18-017 1 93M
FF-SCAN-FLG•001
(19) EN-BYTE-4•000
GND-72T00
GND-75V00
(5,6,7,18,24,26) DATA-BUS2-3•100
(5,6,7,18,24,26) DATA-BUS2-2•100
(5,6,7,18,24,26) DATA-BUS2-1•100
(5,6,7,18,24,26) DATA-BUS2-0•100
DOREG-34•100
DOREG-35•100
DOREG-24•100
DOREG-25•100
DOREG-26•100
DOREG-27•100
DOREG-28•100
DOREG-29•100
DOREG-30•100
DOREG-31•100
(12) ASCII/BCD-SEL•100
(9,10)
(10) DOREG-21•100
(10) DOREG-22•100
(10) DOREG-23•100
(12) DOREG-36•100
GND-81T00
(12) DOREG-37•100
(12) DOREG-38•100
(10)
(12) DOREG-39•100
(10)
(12) DOREG-42•100
(12) DOREG-43•100
(12) DOREG-44•100
(10)
(12) DOREG-45•100
(10)
(12) DOREG-46•100
(10)
(12) DOREG-47•100
(10)
4 SEL2:1 1D3492 81T
4 SEL2:1 1D3492 84V
4 SEL2:1 1D3492 84X
G1
EN
(12) D-BUS-EN-4•100
(12) D-BUS-EN-2•100
U/D-BUS-24•100
U/D-BUS-25•100
U/D-BUS-26•100
U/D-BUS-27•100
U/D-BUS-28•100
U/D-BUS-29•100
U/D-BUS-30•100
U/D-BUS-31•100
U/D-BUS-32•100
U/D-BUS-33•100
U/D-BUS-34•100
U/D-BUS-35•100
(4,6,15)
(4,6,15,17)
(4,7,15)
4D1548 93V
4D1548 93W
4D1548 93X
D-BUS-24•000
D-BUS-25•000
D-BUS-26•000
D-BUS-27•000
D-BUS-28•000
D-BUS-29•000
D-BUS-30•000
D-BUS-31•000
D-BUS-32•000
D-BUS-33•000
D-BUS-34•000
D-BUS-35•000
WH04
WH08
WH12
WH16
WH20
WJ02
WJ06
WJ10
WJ14
WJ18
WK00
WK04
HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- EURCB
DOREG,ASCII/BCD PACK,DRVR
SIZE B
DWG NO 58065904
SH 11.0
REV G
58065904

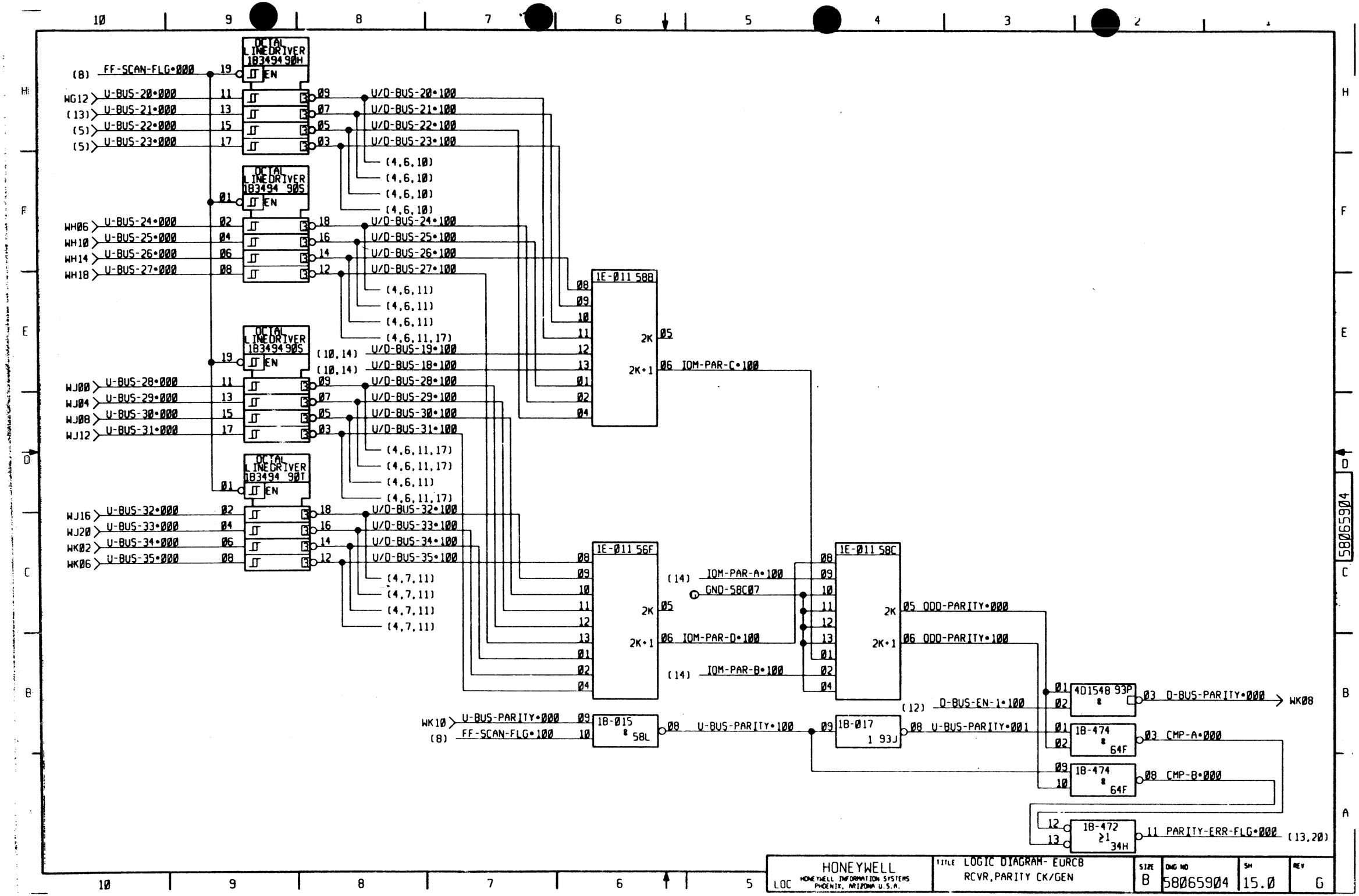

(8) E-XACT•100
(20) D-BUS-BCD•100
1B-473 ≥1 58V
03 ASCII/BCD-SEL•100
(9,10,11)
(8) E-2-DATA•100
(8) E-1-DATA•100
1B-473 ≥1 58V
08 E-DATA•100
1B-094 58U
13 D-BUS-EN•000
1B-017 1 93B
02 D-BUS-EN-1•100
(9,15)
1B-017 1 93B
04 D-BUS-EN-2•100
(9,10,11)
1B-017 1 93B
06 D-BUS-EN-3•100
(10)
1B-017 1 93B
08 D-BUS-EN-4•100
(11)
(25) SELFT-00•100
(25) SELFT-01•100
1B-652 59J ≥1
06 E-2-DATA•101
03 E-XACT•101
(9,10,11)
GND-43J07
1B-476 1 43J
08 HI-LEVEL•110
(19,21,31,35)
4 MEM 4 1S3624 63T
4 MEM 4 1S3624 66X
4 MEM 4 1S3624 66V
1 BIN->1:4 1A
1 BIN->1:4 2A
(18,27) ADDR-BUS-03•100
(18,27) ADDR-BUS-04•100
(19) EN-BYTE-5•000
(19) EN-BYTE-6•000
GND-63T08
GND-66X08
GND-66V08
(5,6,7,18,24,26) DATA-BUS2-3•100
(5,6,7,18,24,26) DATA-BUS2-2•100
(5,6,7,18,24,26) DATA-BUS2-1•100
(5,6,7,18,24,26) DATA-BUS2-0•100
(5,6,7,18,24,26) DATA-BUS2-7•100
(5,6,7,18,24,26) DATA-BUS2-6•100
(5,6,7,18,24,26) DATA-BUS2-5•100
(5,6,7,18,24,26) DATA-BUS2-4•100
1A5D 6,2A
10 DOREG-36•100
09 DOREG-37•100
07 DOREG-38•100
06 DOREG-39•100
10 DOREG-44•100
09 DOREG-45•100
07 DOREG-46•100
06 DOREG-47•100
07 DOREG-42•100
06 DOREG-43•100
(11)
(16) INZ•001
(17) HI-LEVEL•100
(13) PCW-CK>100•101
(16) SCAN-FLG•011
10-480 93U
05 EN-CHAN-REQ•100
06
(16) SERV-REQ•100
1B-472 ≥ 67M
03 $CHAN-REQ•100
(17)
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC
TITLE: LOGIC DIAGRAM- EURCB
DOREG,CHAN REQUEST
SIZE B
DWG NO 58065904
SH 12.0
REV G
58065904

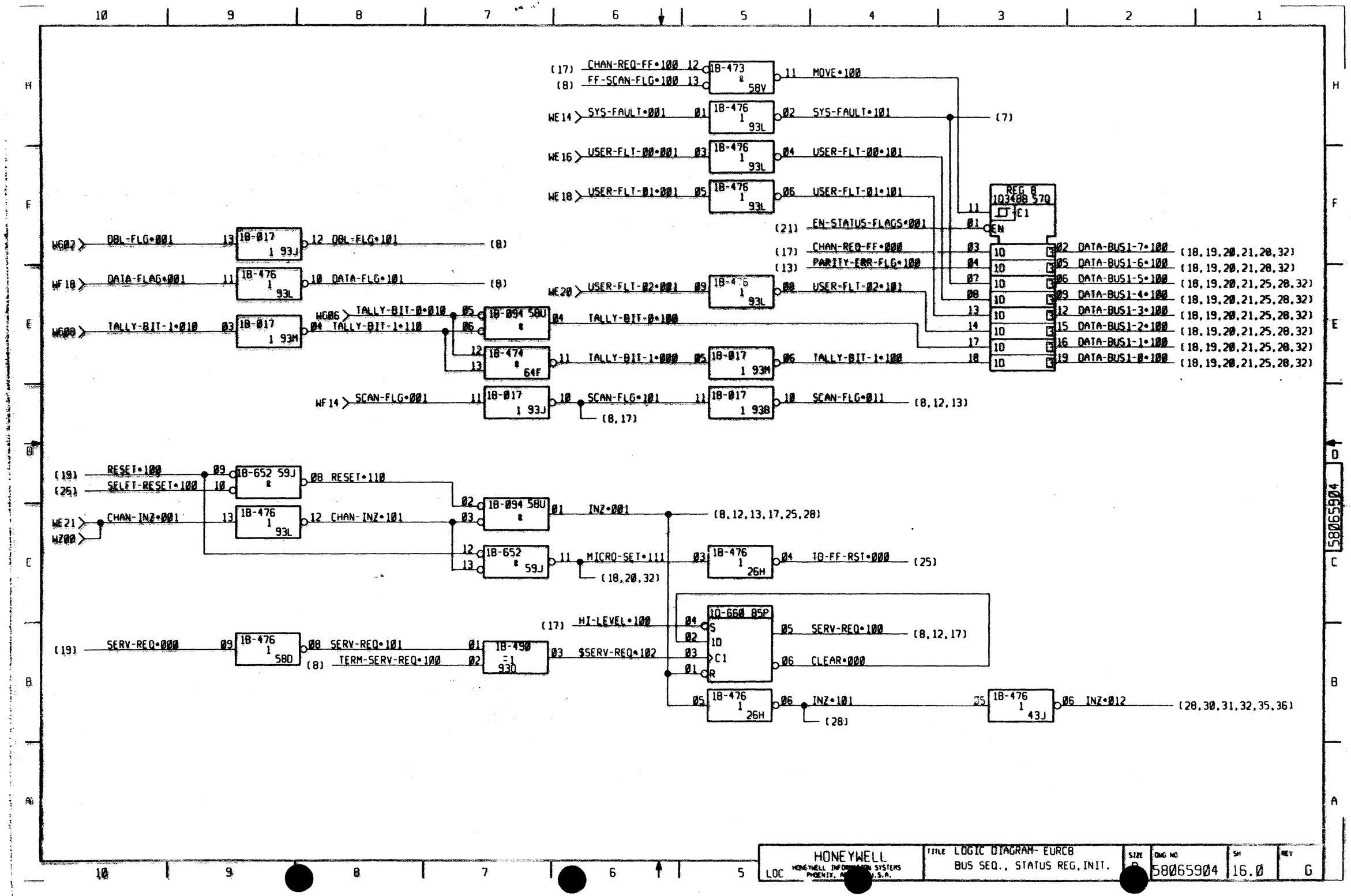


HONEYWELL LOC — HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE: LOGIC DIAGRAM- EURCB BUS SEQ., CONNECT BUSY	SIZE: B	DWG NO: 58065904	SH: 13.0	REV: G

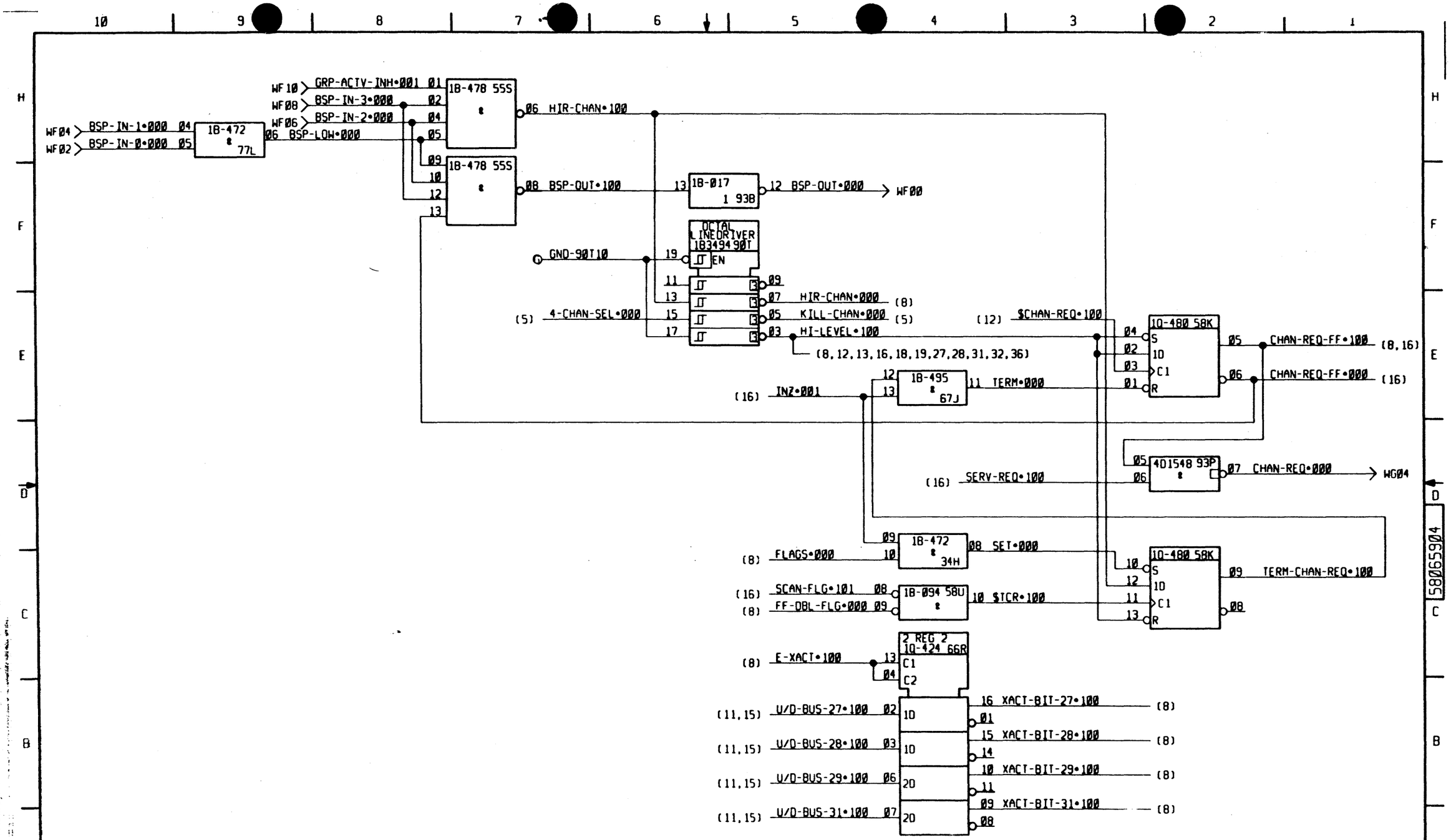
58065904


OCTAL LINEDRIVER 183494 90F
OCTAL LINEDRIVER 183494 90G
OCTAL LINEDRIVER 183494 90H
EN
(8) FF-SCAN-FLG•000
WA12 U-BUS-00•000
WA16 U-BUS-01•000
WA20 U-BUS-02•000
WB02 U-BUS-03•000
WB06 U-BUS-04•000
WB10 U-BUS-05•000
WB14 U-BUS-06•000
WB18 U-BUS-07•000
WC00 U-BUS-08•000
WC04 U-BUS-09•000
WC08 U-BUS-10•000
WC12 U-BUS-11•000
(5) U-BUS-12•000
(5) U-BUS-13•000
(5) U-BUS-14•000
(5) U-BUS-15•000
(5) U-BUS-16•000
(5) U-BUS-17•000
WD18 U-BUS-18•000
WE00 U-BUS-19•000
U/D-BUS-00•100
U/D-BUS-01•100
U/D-BUS-02•100
U/D-BUS-03•100
U/D-BUS-04•100
U/D-BUS-05•100
U/D-BUS-06•100
U/D-BUS-07•100
U/D-BUS-08•100
U/D-BUS-09•100
U/D-BUS-10•100
U/D-BUS-11•100
U/D-BUS-12•100
U/D-BUS-13•100
U/D-BUS-14•100
U/D-BUS-15•100
U/D-BUS-16•100
U/D-BUS-17•100
U/D-BUS-18•100
U/D-BUS-19•100
(4,6,9)
(4,6,10)
(4,6,10,15)
1E-011 67D
1E-011 67A
2K
2K•1
IOM-PAR-A•100
IOM-PAR-B•100
(15)
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- EURCB
RCVR, PARITY CK/GEN
SIZE B
DWG NO 58065904
SH 14.0
REV G
58065904


OCTAL LINE DRIVER 1B3494 90H
OCTAL LINE DRIVER 1B3494 90S
OCTAL LINE DRIVER 1B3494 90S
OCTAL LINE DRIVER 1B3494 90T
(8) FF-SCAN-FLG•000
WG12 U-BUS-20•000
(13) U-BUS-21•000
(5) U-BUS-22•000
(5) U-BUS-23•000
WH06 U-BUS-24•000
WH10 U-BUS-25•000
WH14 U-BUS-26•000
WH18 U-BUS-27•000
WJ00 U-BUS-28•000
WJ04 U-BUS-29•000
WJ08 U-BUS-30•000
WJ12 U-BUS-31•000
WJ16 U-BUS-32•000
WJ20 U-BUS-33•000
WK02 U-BUS-34•000
WK06 U-BUS-35•000
U/D-BUS-20•100
U/D-BUS-21•100
U/D-BUS-22•100
U/D-BUS-23•100
U/D-BUS-24•100
U/D-BUS-25•100
U/D-BUS-26•100
U/D-BUS-27•100
(10,14) U/D-BUS-19•100
(10,14) U/D-BUS-18•100
U/D-BUS-28•100
U/D-BUS-29•100
U/D-BUS-30•100
U/D-BUS-31•100
U/D-BUS-32•100
U/D-BUS-33•100
U/D-BUS-34•100
U/D-BUS-35•100
(4,6,10)
(4,6,10)
(4,6,10)
(4,6,10)
(4,6,11)
(4,6,11)
(4,6,11)
(4,6,11,17)
(4,6,11,17)
(4,6,11,17)
(4,6,11)
(4,6,11,17)
(4,7,11)
(4,7,11)
(4,7,11)
(4,7,11)
1E-011 588
1E-011 56F
1E-011 58C
2K
2K+1
05
06 IOM-PAR-C•100
(14) IOM-PAR-A•100
GND-58C07
06 IOM-PAR-D•100
(14) IOM-PAR-B•100
05 ODD-PARITY•000
06 ODD-PARITY•100
WK10 U-BUS-PARITY•000
(8) FF-SCAN-FLG•100
1B-015 8 58L
08 U-BUS-PARITY•100
1B-017 1 93J
08 U-BUS-PARITY•001
(12) D-BUS-EN-1•100
4D1548 93P 8
03 D-BUS-PARITY•000
WK08
1B-474 8 64F
03 CMP-A•000
1B-474 8 64F
08 CMP-B•000
1B-472 ≥1 34H
11 PARITY-ERR-FLG•000
(13,20)
HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- EURCB RCVR,PARITY CK/GEN
SIZE B
DWG NO 58065904
SH 15.0
REV G
58065904

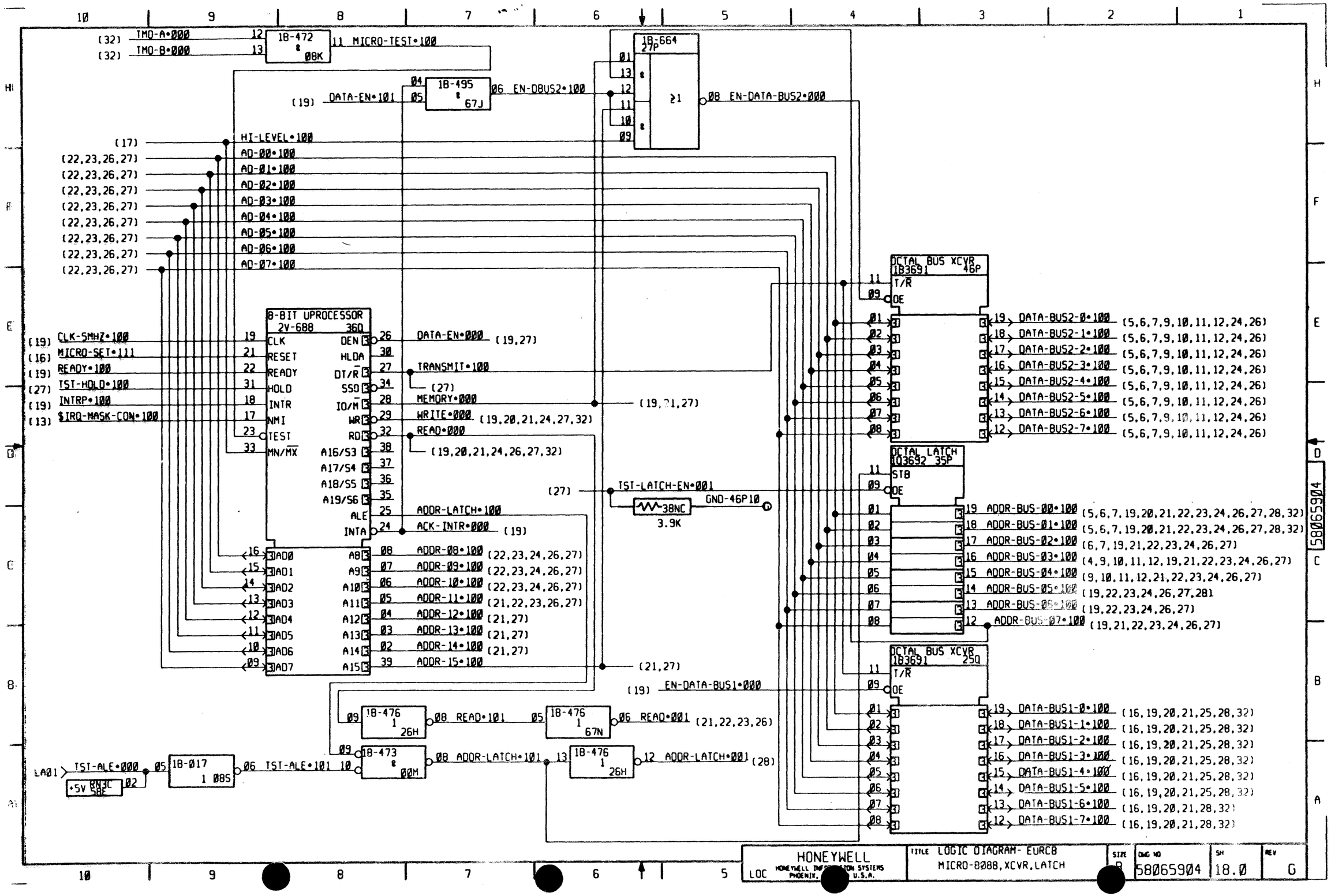


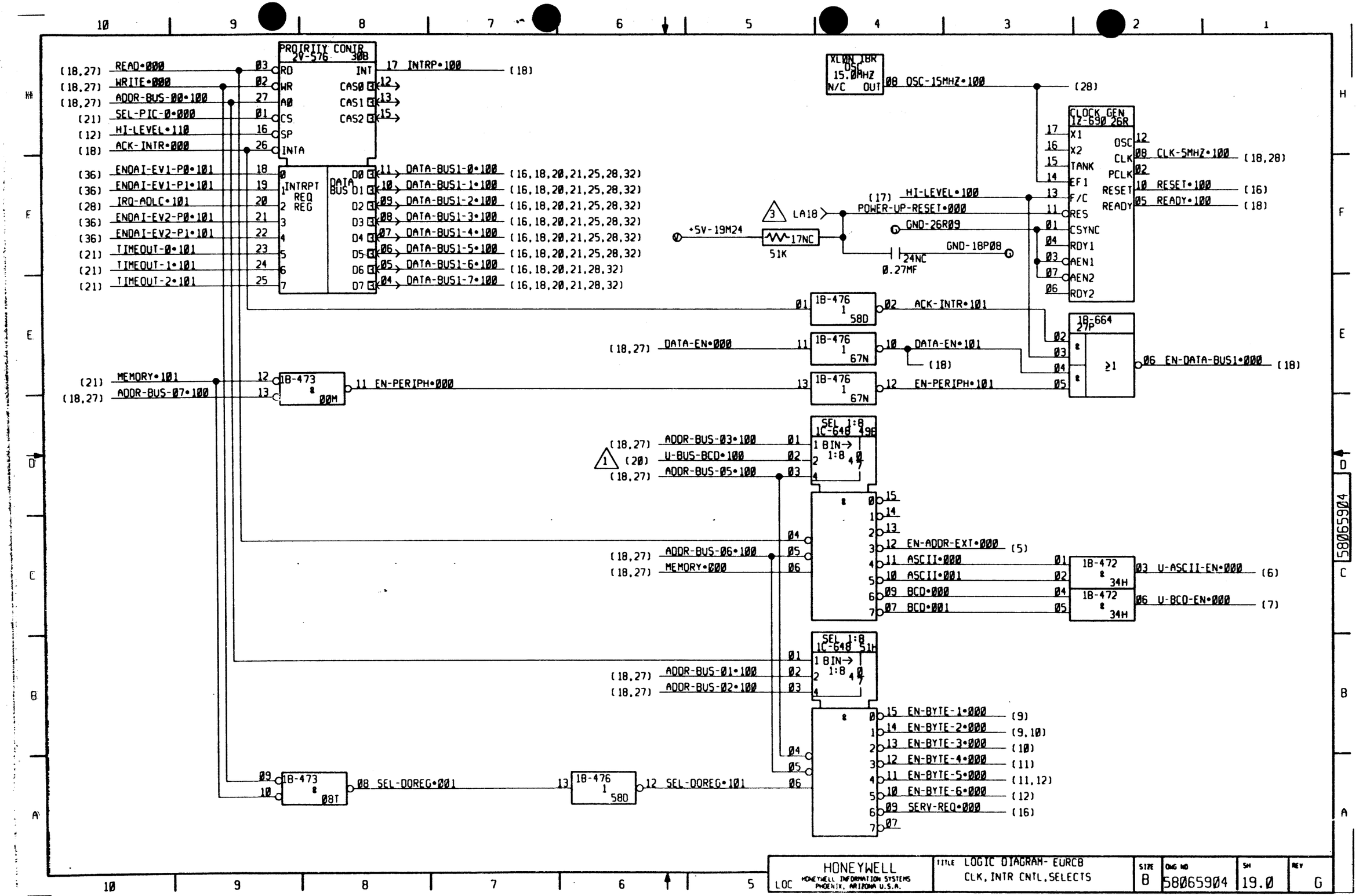
HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, AZ U.S.A.	TITLE LOGIC DIAGRAM- EURCB BUS SEQ., STATUS REG, INIT.	SIZE B	DWG NO 58065904	SH 16.0	REV G

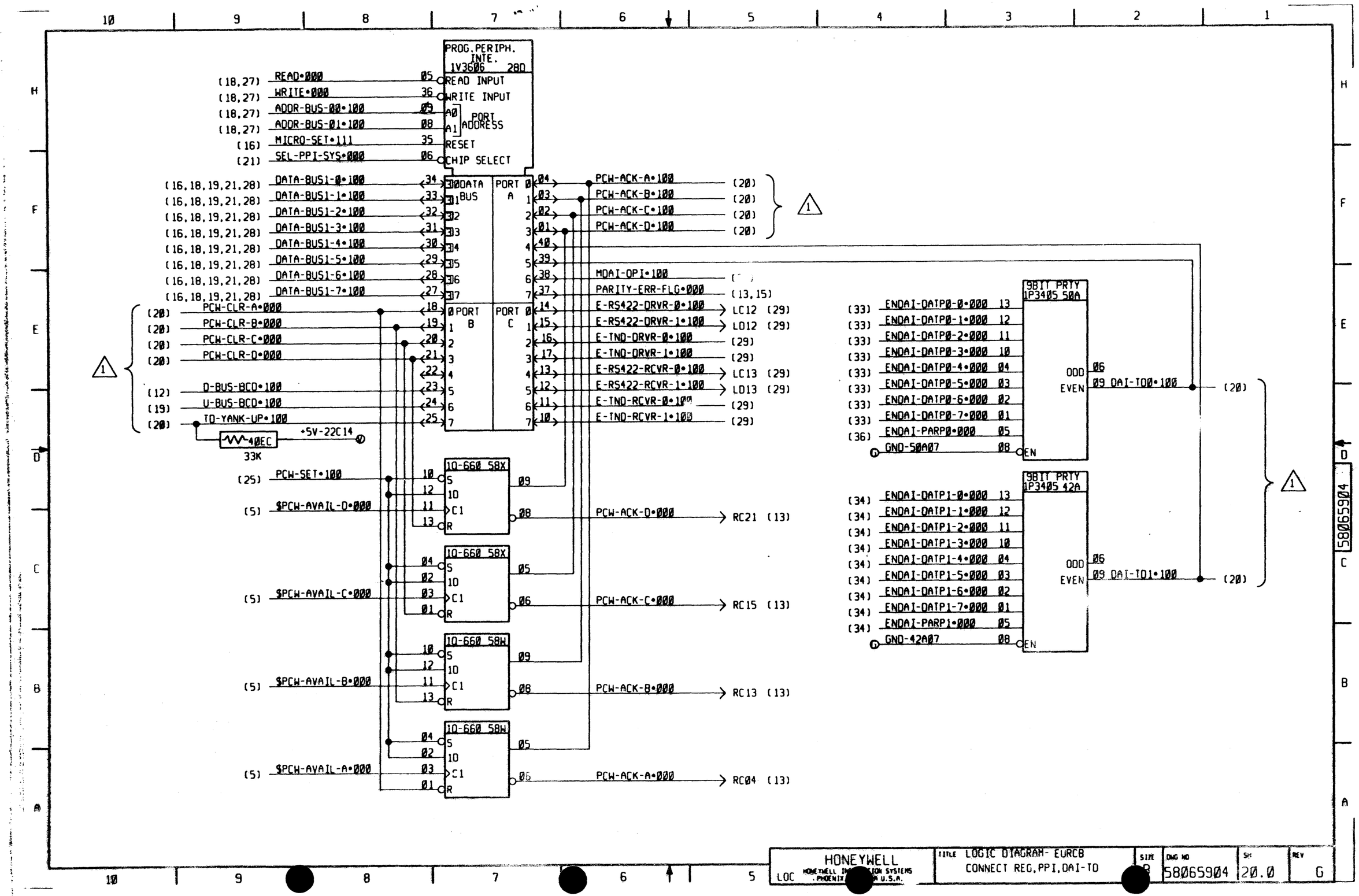


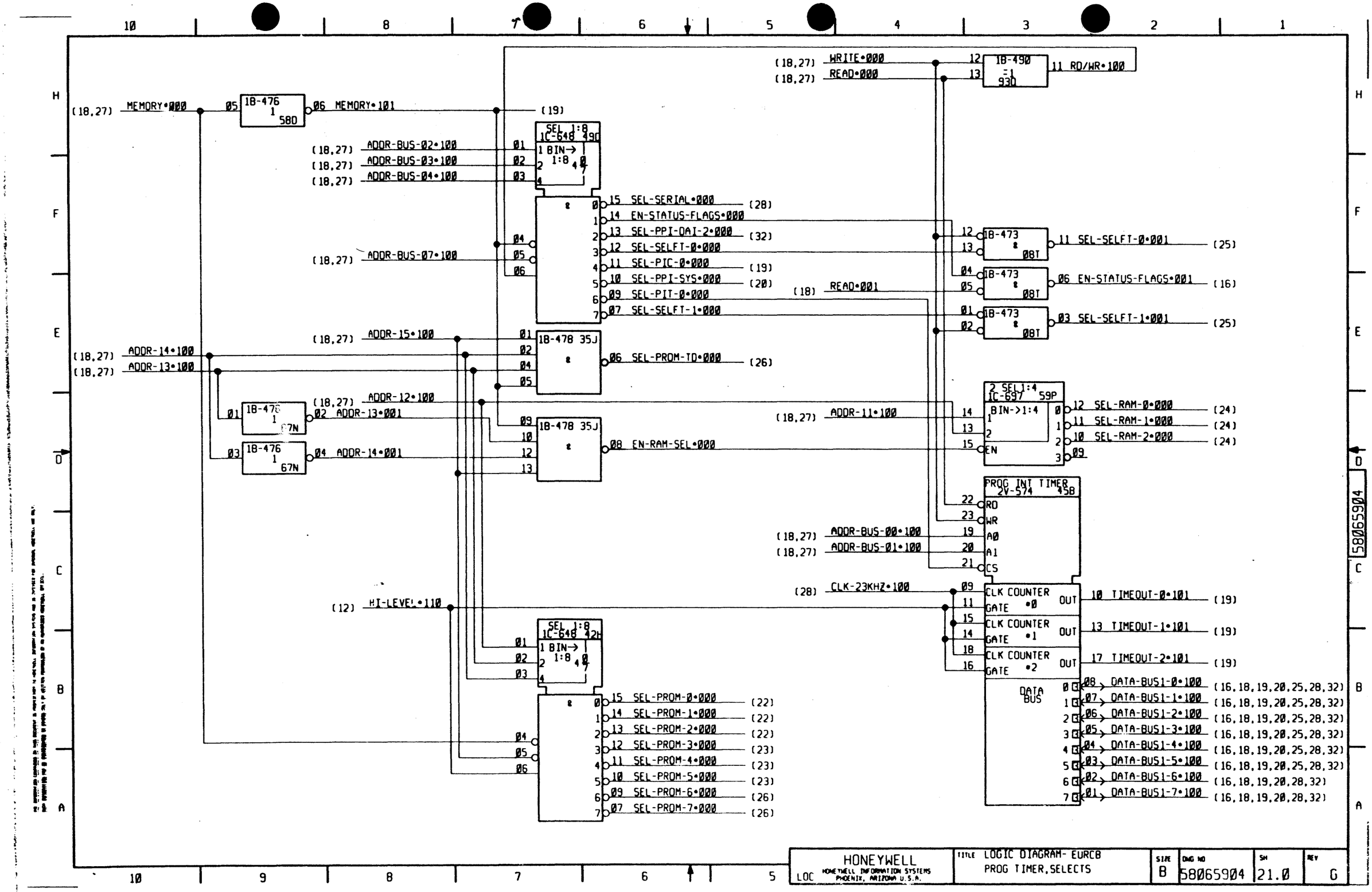
HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURC8 PRIORITY RESOLVE, CHAN REQ	SIZE B	DWG NO 58065904	SH 17.0	REV G

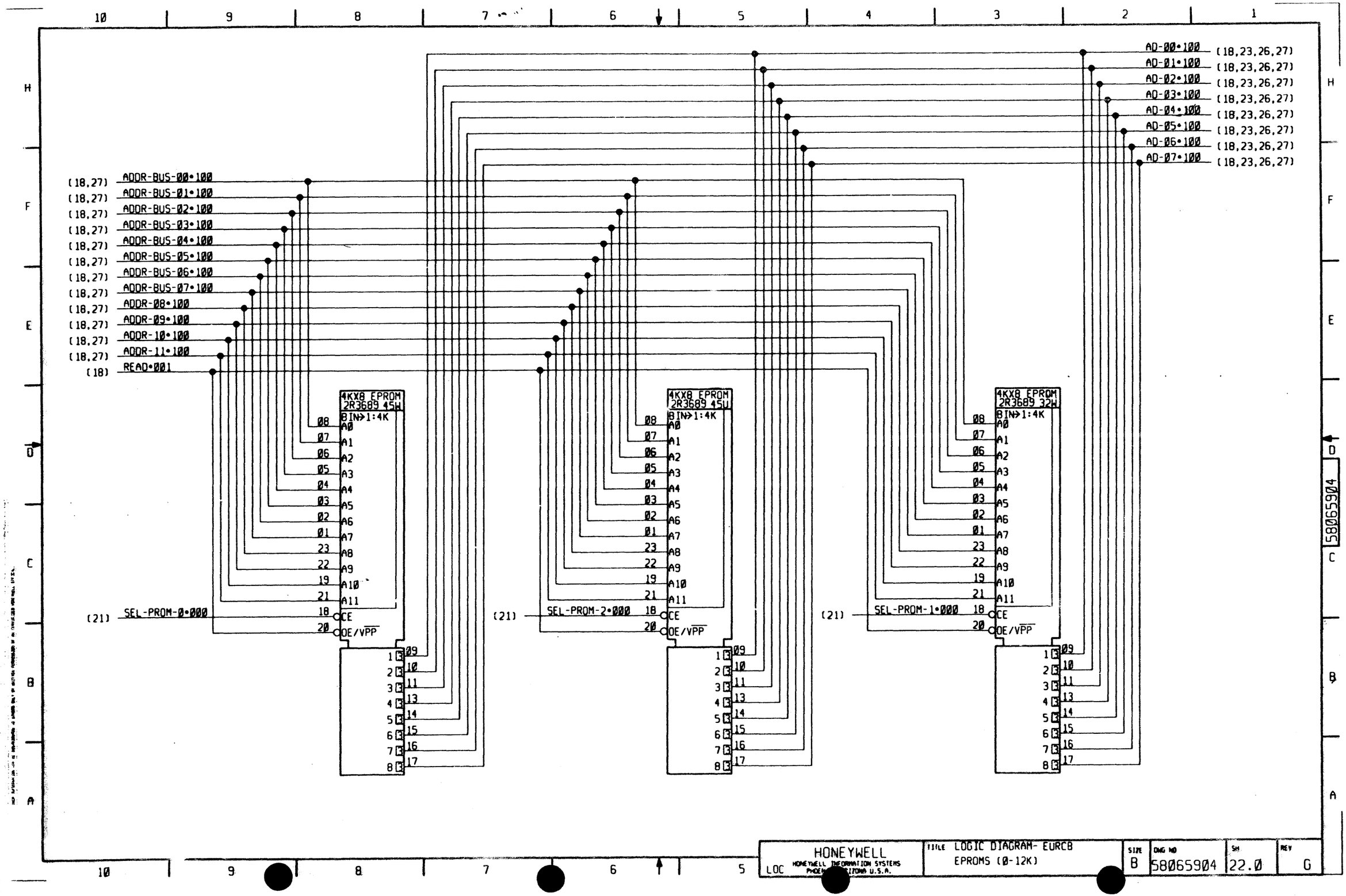
58065904

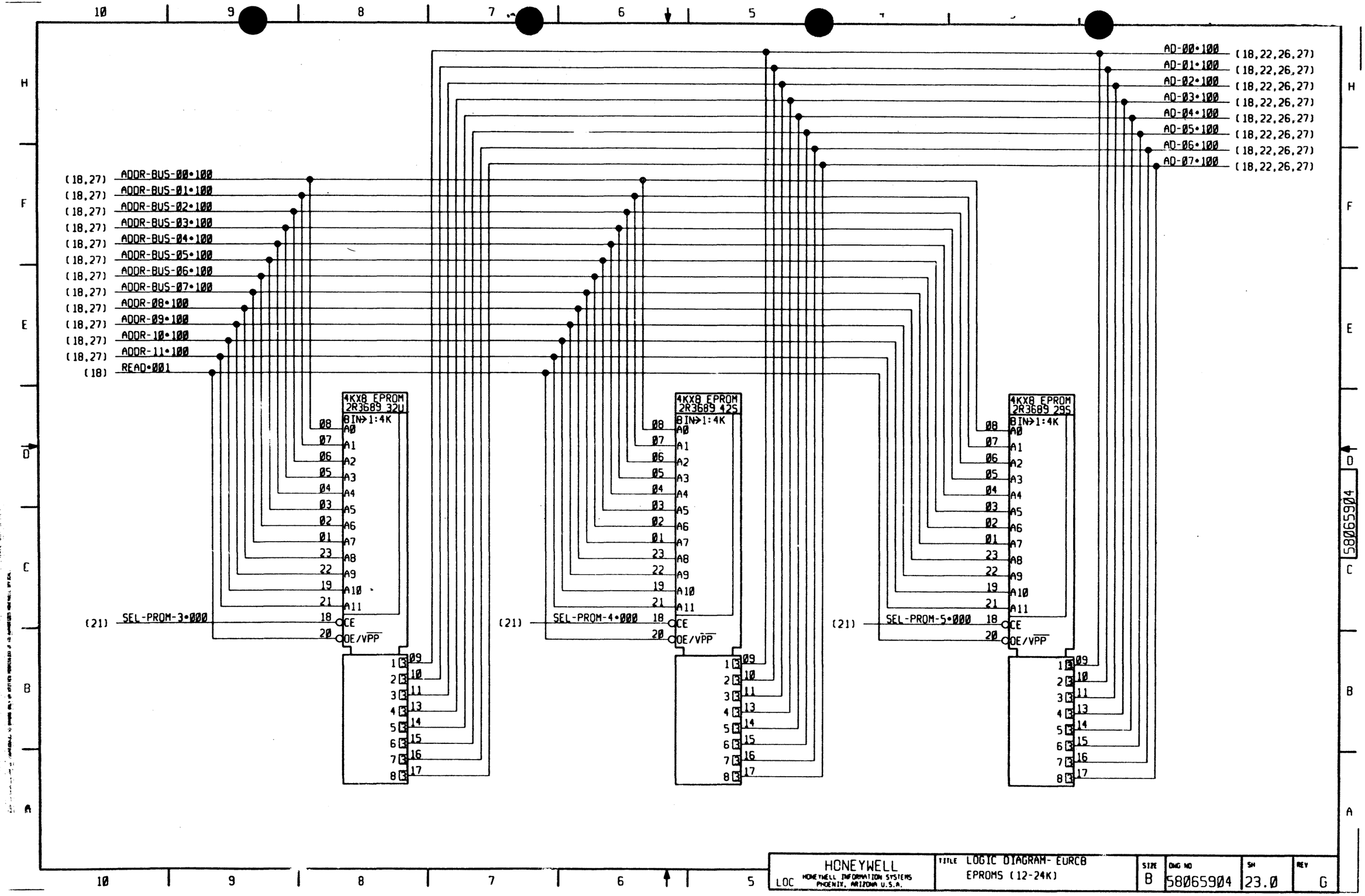

10 9 8 7 6 5 4 3 2 1
(32) TMO-A•000
(32) TMO-B•000
12
13
1B-472
8
08K
11 MICRO-TEST•100
1B-664
27P
01
13
12
11
10
09
≥1
08 EN-DATA-BUS2•000
04
05
1B-495
8
67J
06 EN-DBUS2•100
(19) DATA-EN•101
(17) HI-LEVEL•100
(22,23,26,27) AD-00•100
(22,23,26,27) AD-01•100
(22,23,26,27) AD-02•100
(22,23,26,27) AD-03•100
(22,23,26,27) AD-04•100
(22,23,26,27) AD-05•100
(22,23,26,27) AD-06•100
(22,23,26,27) AD-07•100
8-BIT UPROCESSOR
2V-688
36Q
(19) CLK-5MHZ•100
(16) MICRO-SEI•111
(19) READY•100
(27) TSI-HOLD•100
(19) INTRP•100
(13) $IRQ-MASK-CON•100
19 CLK
21 RESET
22 READY
31 HOLD
18 INTR
17 NMI
23 TEST
33 MN/MX
26 DEN
30 HLDA
27 DT/R
34 SSO
28 IO/M
29 WR
32 RD
38 A16/S3
37 A17/S4
36 A18/S5
35 A19/S6
25 ALE
24 INTA
DATA-EN•000 (19,27)
TRANSMIT•100
(27)
MEMORY•000
WRITE•000 (19,20,21,24,27,32)
READ•000
(19,20,21,24,26,27,32)
(19,21,27)
ADDR-LATCH•100
ACK-INTR•000 (19)
16 AD0
15 AD1
14 AD2
13 AD3
12 AD4
11 AD5
10 AD6
09 AD7
A8 08 ADDR-08•100 (22,23,24,26,27)
A9 07 ADDR-09•100 (22,23,24,26,27)
A10 06 ADDR-10•100 (22,23,24,26,27)
A11 05 ADDR-11•100 (21,22,23,26,27)
A12 04 ADDR-12•100 (21,27)
A13 03 ADDR-13•100 (21,27)
A14 02 ADDR-14•100 (21,27)
A15 39 ADDR-15•100
(21,27)
(27) TSI-LATCH-EN•001
38NC
3.9K
GND-46P10
OCTAL BUS XCVR
1B3691
48P
11 T/R
09 OE
01 02 03 04 05 06 07 08
19 DATA-BUS2-0•100 (5,6,7,9,10,11,12,24,26)
18 DATA-BUS2-1•100 (5,6,7,9,10,11,12,24,26)
17 DATA-BUS2-2•100 (5,6,7,9,10,11,12,24,26)
16 DATA-BUS2-3•100 (5,6,7,9,10,11,12,24,26)
15 DATA-BUS2-4•100 (5,6,7,9,10,11,12,24,26)
14 DATA-BUS2-5•100 (5,6,7,9,10,11,12,24,26)
13 DATA-BUS2-6•100 (5,6,7,9,10,11,12,24,26)
12 DATA-BUS2-7•100 (5,6,7,9,10,11,12,24,26)
OCTAL LATCH
1B3692
35P
11 STB
09 OE
01 02 03 04 05 06 07 08
19 ADDR-BUS-00•100 (5,6,7,19,20,21,22,23,24,26,27,28,32)
18 ADDR-BUS-01•100 (5,6,7,19,20,21,22,23,24,26,27,28,32)
17 ADDR-BUS-02•100 (6,7,19,21,22,23,24,26,27)
16 ADDR-BUS-03•100 (4,9,10,11,12,19,21,22,23,24,26,27)
15 ADDR-BUS-04•100 (9,10,11,12,21,22,23,24,26,27)
14 ADDR-BUS-05•100 (19,22,23,24,26,27,28)
13 ADDR-BUS-06•100 (19,22,23,24,26,27)
12 ADDR-BUS-07•100 (19,21,22,23,24,26,27)
OCTAL BUS XCVR
1B3691
25Q
11 T/R
09 OE
01 02 03 04 05 06 07 08
19 DATA-BUS1-0•100 (16,19,20,21,25,28,32)
18 DATA-BUS1-1•100 (16,19,20,21,25,28,32)
17 DATA-BUS1-2•100 (16,19,20,21,25,28,32)
16 DATA-BUS1-3•100 (16,19,20,21,25,28,32)
15 DATA-BUS1-4•100 (16,19,20,21,25,28,32)
14 DATA-BUS1-5•100 (16,19,20,21,25,28,32)
13 DATA-BUS1-6•100 (16,19,20,21,28,32)
12 DATA-BUS1-7•100 (16,19,20,21,28,32)
(19) EN-DATA-BUS1•000
09 1B-476 1 26H 08 READ•101
05 1B-476 1 67N 06 READ•001 (21,22,23,26)
LA01 TSI-ALE•000
•5V RN3C 5BF
02
05 1B-017 1 08S 06 TSI-ALE•101
09 1B-473 8 00M 08 ADDR-LATCH•101
13 1B-476 1 26H 12 ADDR-LATCH•001 (28)
HONEYWELL
LOC
TITLE LOGIC DIAGRAM- EURCB
MICRO-8088,XCVR,LATCH
SIZE B
DWG NO 58065904
SH 18.0
REV G
58065904

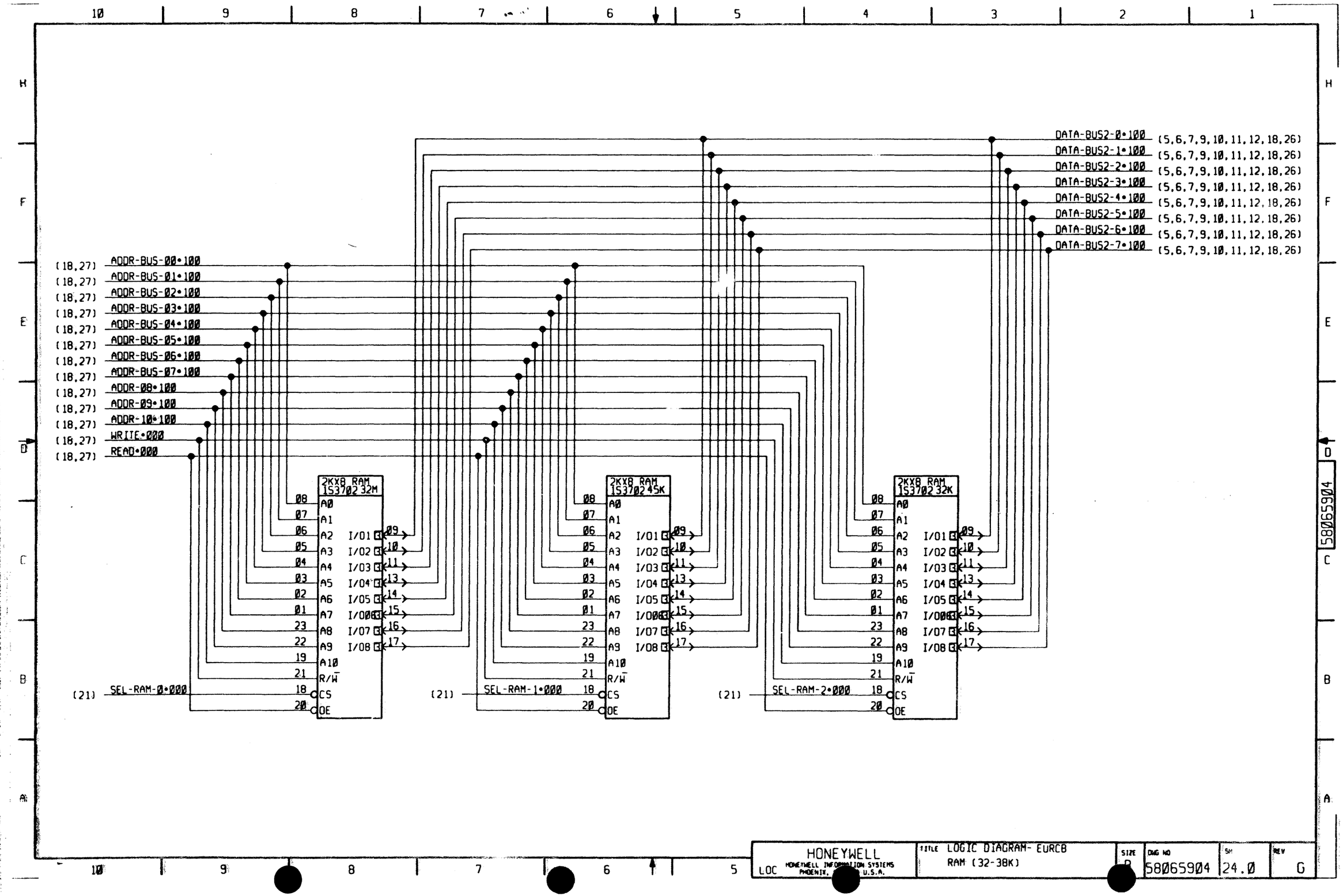

PRIORITY CONTR 2V-576 30B
(18,27) READ•000 03 RD
(18,27) WRITE•000 02 WR
(18,27) ADDR-BUS-00•100 27 A0
(21) SEL-PIC-0•000 01 CS
(12) HI-LEVEL•110 16 SP
(18) ACK-INTR•000 26 INTA
INT 17 INTRP•100 (18)
CAS0 12
CAS1 13
CAS2 15
(36) ENDAI-EV1-P0•101 18
(36) ENDAI-EV1-P1•101 19
(28) IRQ-ADLC•101 20
(36) ENDAI-EV2-P0•101 21
(36) ENDAI-EV2-P1•101 22
(21) TIMEOUT-0•101 23
(21) TIMEOUT-1•101 24
(21) TIMEOUT-2•101 25
INTRPT REQ REG
DATA BUS
D0 11 DATA-BUS1-0•100 (16,18,20,21,25,28,32)
D1 10 DATA-BUS1-1•100 (16,18,20,21,25,28,32)
D2 09 DATA-BUS1-2•100 (16,18,20,21,25,28,32)
D3 08 DATA-BUS1-3•100 (16,18,20,21,25,28,32)
D4 07 DATA-BUS1-4•100 (16,18,20,21,25,28,32)
D5 06 DATA-BUS1-5•100 (16,18,20,21,25,28,32)
D6 05 DATA-BUS1-6•100 (16,18,20,21,28,32)
D7 04 DATA-BUS1-7•100 (16,18,20,21,28,32)
XLON 18R OSC 15.0MHZ N/C OUT 08 OSC-15MHZ•100 (28)
CLOCK GEN 12-690 26R
X1 X2 TANK EF1 F/C RES CSYNC RDY1 AEN1 AEN2 RDY2
OSC 12
CLK 08 CLK-5MHZ•100 (18,28)
PCLK 02
RESET 10 RESET•100 (16)
READY 05 READY•100 (18)
(17) HI-LEVEL•100
POWER-UP-RESET•000
GND-26R09
GND-18P08
+5V-19M24
17NC 51K
24NC 0.27MF
LA18
1B-476 1 58D
01 02 ACK-INTR•101
1B-664 27P
(18,27) DATA-EN•000
1B-476 1 67N
11 10 DATA-EN•101
(18)
02 03 04 05 ≥1 06 EN-DATA-BUS1•000 (18)
(21) MEMORY•101
(18,27) ADDR-BUS-07•100
1B-473 00M
12 13 11 EN-PERIPH•000
13 12 EN-PERIPH•101
SEL 1:8 1C-648 49B
SEL 1:8 1C-648 51H
(18,27) ADDR-BUS-03•100 01
(20) U-BUS-BCD•100 02
(18,27) ADDR-BUS-05•100 03
(18,27) ADDR-BUS-06•100 05
(18,27) MEMORY•000 06
04
(18,27) ADDR-BUS-01•100 02
(18,27) ADDR-BUS-02•100 03
01
0 15
1 14
2 13
3 12 EN-ADDR-EXT•000 (5)
4 11 ASCII•000
5 10 ASCII•001
6 09 BCD•000
7 07 BCD•001
1B-472 34H
01 02 03 U-ASCII-EN•000 (6)
04 05 06 U-BCD-EN•000 (7)
0 15 EN-BYTE-1•000 (9)
1 14 EN-BYTE-2•000 (9,10)
2 13 EN-BYTE-3•000 (10)
3 12 EN-BYTE-4•000 (11)
4 11 EN-BYTE-5•000 (11,12)
5 10 EN-BYTE-6•000 (12)
6 09 SERV-REQ•000 (16)
7 07
09 10 1B-473 08T
08 SEL-DOREG•001
13 1B-476 1 58O
12 SEL-DOREG•101
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- EURCB CLK, INTR CNTL, SELECTS
SIZE B
DWG NO 58065904
SH 19.0
REV G
58065904

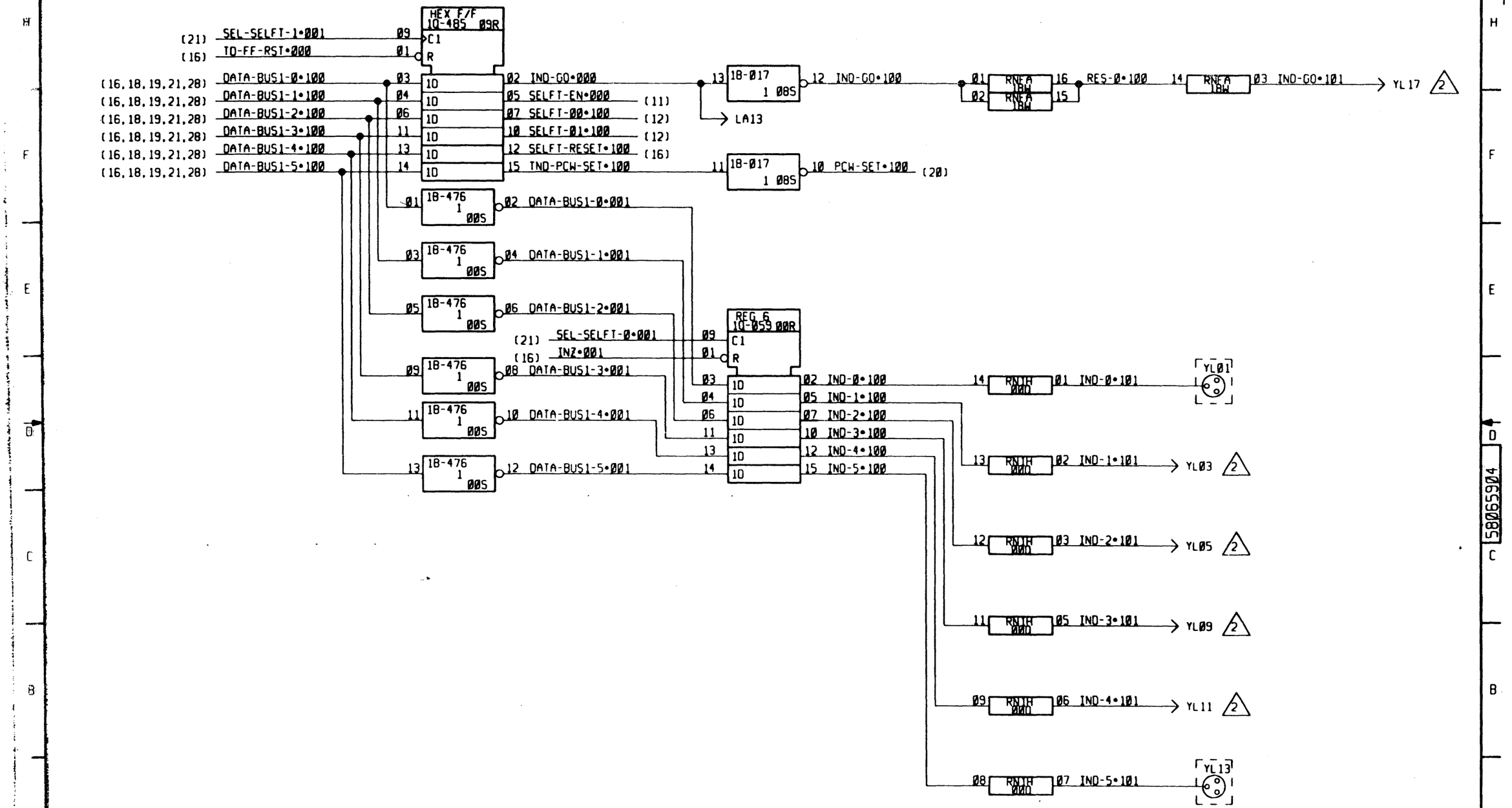

PROG.PERIPH. INTE. 1V3606 28D
READ INPUT
WRITE INPUT
A0
A1
PORT ADDRESS
RESET
CHIP SELECT
D0DATA BUS
D1
D2
D3
D4
D5
D6
D7
PORT A
PORT B
PORT C
(18,27) READ•000
(18,27) WRITE•000
(18,27) ADDR-BUS-00•100
(18,27) ADDR-BUS-01•100
(16) MICRO-SET•111
(21) SEL-PPI-SYS•000
(16,18,19,21,28) DATA-BUS1-0•100
(16,18,19,21,28) DATA-BUS1-1•100
(16,18,19,21,28) DATA-BUS1-2•100
(16,18,19,21,28) DATA-BUS1-3•100
(16,18,19,21,28) DATA-BUS1-4•100
(16,18,19,21,28) DATA-BUS1-5•100
(16,18,19,21,28) DATA-BUS1-6•100
(16,18,19,21,28) DATA-BUS1-7•100
(20) PCW-CLR-A•000
(20) PCW-CLR-B•000
(20) PCW-CLR-C•000
(20) PCW-CLR-D•000
(12) D-BUS-BCD•100
(19) U-BUS-BCD•100
(20) ID-YANK-UP•100
40EC
33K
•5V-22C14
PCW-ACK-A•100 (20)
PCW-ACK-B•100 (20)
PCW-ACK-C•100 (20)
PCW-ACK-D•100 (20)
MDAI-OPI•100 (
PARITY-ERR-FLG•000 (13,15)
E-RS422-DRVR-0•100 LC12 (29)
E-RS422-DRVR-1•100 LD12 (29)
E-IND-DRVR-0•100 (29)
E-IND-DRVR-1•100 (29)
E-RS422-RCVR-0•100 LC13 (29)
E-RS422-RCVR-1•100 LD13 (29)
E-IND-RCVR-0•100 (29)
E-IND-RCVR-1•100 (29)
1
9BIT PRTY 1P3405 50A
(33) ENDAI-DATP0-0•000 13
(33) ENDAI-DATP0-1•000 12
(33) ENDAI-DATP0-2•000 11
(33) ENDAI-DATP0-3•000 10
(33) ENDAI-DATP0-4•000 04
(33) ENDAI-DATP0-5•000 03
(33) ENDAI-DATP0-6•000 02
(33) ENDAI-DATP0-7•000 01
(36) ENDAI-PARP0•000 05
GND-50A07 08
EN
ODD
EVEN
06
09 DAI-IDØ•100
(20)
9BIT PRTY 1P3405 42A
(34) ENDAI-DATP1-0•000 13
(34) ENDAI-DATP1-1•000 12
(34) ENDAI-DATP1-2•000 11
(34) ENDAI-DATP1-3•000 10
(34) ENDAI-DATP1-4•000 04
(34) ENDAI-DATP1-5•000 03
(34) ENDAI-DATP1-6•000 02
(34) ENDAI-DATP1-7•000 01
(34) ENDAI-PARP1•000 05
GND-42A07 08
EN
ODD
EVEN
06
09 DAI-ID1•100
(20)
10-660 58X
10-660 58W
S
1D
C1
R
(25) PCW-SET•100
(5) $PCW-AVAIL-D•000
(5) $PCW-AVAIL-C•000
(5) $PCW-AVAIL-B•000
(5) $PCW-AVAIL-A•000
PCW-ACK-D•000 RC21 (13)
PCW-ACK-C•000 RC15 (13)
PCW-ACK-B•000 RC13 (13)
PCW-ACK-A•000 RC04 (13)
58065904
HONEYWELL
LOC
TITLE LOGIC DIAGRAM- EURCB
CONNECT REG,PPI,DAI-TD
SIZE B
DWG NO 58065904
SH 20.0
REV G


(18,27) MEMORY•000
1B-476 1 580
Ø6 MEMORY•101
(19)
SEL 1:8 1C-648 49D
1 BIN→ 1:8
(18,27) ADDR-BUS-02•100
(18,27) ADDR-BUS-03•100
(18,27) ADDR-BUS-04•100
(18,27) ADDR-BUS-07•100
15 SEL-SERIAL•000 (28)
14 EN-STATUS-FLAGS•000
13 SEL-PPI-OAI-2•000 (32)
12 SEL-SELFT-Ø•000
11 SEL-PIC-Ø•000 (19)
10 SEL-PPI-SYS•000 (20)
Ø9 SEL-PIT-Ø•000
Ø7 SEL-SELFT-1•000
(18,27) ADDR-15•100
(18,27) ADDR-14•100
(18,27) ADDR-13•100
1B-478 35J
Ø6 SEL-PROM-TD•000 (26)
(18,27) ADDR-12•100
1B-476 1 67N
Ø2 ADDR-13•001
Ø4 ADDR-14•001
Ø9
1Ø
12
13
Ø8 EN-RAM-SEL•000
(18,27) WRITE•000
(18,27) READ•000
1B-490 =1 93D
11 RD/WR•100
1B-473 08T
11 SEL-SELFT-Ø•001 (25)
06 EN-STATUS-FLAGS•001 (16)
(18) READ•001
03 SEL-SELFT-1•001 (25)
(18,27) ADDR-11•100
2 SEL 1:4 1C-697 59P
BIN->1:4
12 SEL-RAM-Ø•000 (24)
11 SEL-RAM-1•000 (24)
10 SEL-RAM-2•000 (24)
EN
PROG INT TIMER 2V-574 45B
RD
WR
(18,27) ADDR-BUS-00•100
(18,27) ADDR-BUS-01•100
A0
A1
CS
(28) CLK-23KHZ•100
CLK COUNTER •0 GATE OUT
CLK COUNTER •1 GATE OUT
CLK COUNTER •2 GATE OUT
10 TIMEOUT-Ø•101 (19)
13 TIMEOUT-1•101 (19)
17 TIMEOUT-2•101 (19)
DATA BUS
08 DATA-BUS1-Ø•100 (16,18,19,20,25,28,32)
07 DATA-BUS1-1•100 (16,18,19,20,25,28,32)
06 DATA-BUS1-2•100 (16,18,19,20,25,28,32)
05 DATA-BUS1-3•100 (16,18,19,20,25,28,32)
04 DATA-BUS1-4•100 (16,18,19,20,25,28,32)
03 DATA-BUS1-5•100 (16,18,19,20,25,28,32)
02 DATA-BUS1-6•100 (16,18,19,20,28,32)
01 DATA-BUS1-7•100 (16,18,19,20,28,32)
(12) HI-LEVEL•110
SEL 1:8 1C-648 42H
SEL-PROM-Ø•000 (22)
SEL-PROM-1•000 (22)
SEL-PROM-2•000 (22)
SEL-PROM-3•000 (23)
SEL-PROM-4•000 (23)
SEL-PROM-5•000 (23)
SEL-PROM-6•000 (26)
SEL-PROM-7•000 (26)
58065904
HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- EURCB PROG TIMER,SELECTS
SIZE B
DWG NO 58065904
SH 21.Ø
REV G


10
9
8
7
6
5
4
3
2
1
H
F
E
D
C
B
A
(18,27) ADDR-BUS-00•100
(18,27) ADDR-BUS-01•100
(18,27) ADDR-BUS-02•100
(18,27) ADDR-BUS-03•100
(18,27) ADDR-BUS-04•100
(18,27) ADDR-BUS-05•100
(18,27) ADDR-BUS-06•100
(18,27) ADDR-BUS-07•100
(18,27) ADDR-08•100
(18,27) ADDR-09•100
(18,27) ADDR-10•100
(18,27) ADDR-11•100
(18) READ•001
AD-00•100 (18,23,26,27)
AD-01•100 (18,23,26,27)
AD-02•100 (18,23,26,27)
AD-03•100 (18,23,26,27)
AD-04•100 (18,23,26,27)
AD-05•100 (18,23,26,27)
AD-06•100 (18,23,26,27)
AD-07•100 (18,23,26,27)
4KX8 EPROM
2R3689 45W
BIN→1:4K
A0 A1 A2 A3 A4 A5 A6 A5 A8 A9 A10 A11
CE
OE/VPP
(21) SEL-PROM-0•000
4KX8 EPROM
2R3689 45U
BIN→1:4K
(21) SEL-PROM-2•000
4KX8 EPROM
2R3689 32W
BIN→1:4K
(21) SEL-PROM-1•000
09 10 11 13 14 15 16 17
58065904
HONEYWELL
HONEYWELL INFORMATION SYSTEMS
PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- EURCB
EPROMS (0-12K)
SIZE B
DWG NO 58065904
SH 22.0
REV G

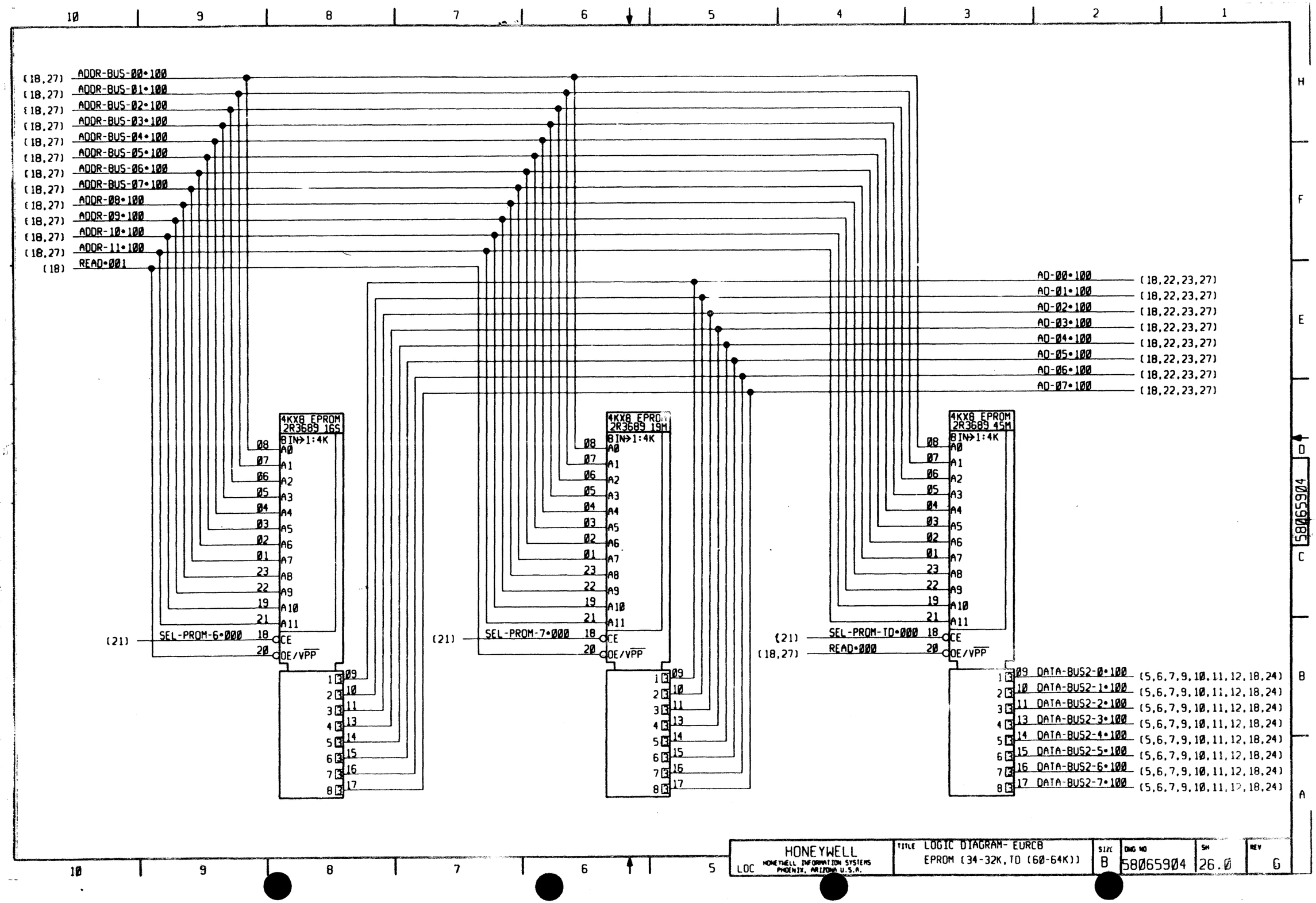

(18,27) ADDR-BUS-00•100
(18,27) ADDR-BUS-01•100
(18,27) ADDR-BUS-02•100
(18,27) ADDR-BUS-03•100
(18,27) ADDR-BUS-04•100
(18,27) ADDR-BUS-05•100
(18,27) ADDR-BUS-06•100
(18,27) ADDR-BUS-07•100
(18,27) ADDR-08•100
(18,27) ADDR-09•100
(18,27) ADDR-10•100
(18,27) ADDR-11•100
(18) READ•001
AD-00•100 (18,22,26,27)
AD-01•100 (18,22,26,27)
AD-02•100 (18,22,26,27)
AD-03•100 (18,22,26,27)
AD-04•100 (18,22,26,27)
AD-05•100 (18,22,26,27)
AD-06•100 (18,22,26,27)
AD-07•100 (18,22,26,27)
4KX8 EPROM 2R3689 32U
4KX8 EPROM 2R3689 42S
4KX8 EPROM 2R3689 29S
8IN→1:4K
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
CE
OE/VPP
(21) SEL-PROM-3•000
(21) SEL-PROM-4•000
(21) SEL-PROM-5•000
09 10 11 13 14 15 16 17
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- EURCB EPROMS (12-24K)
SIZE B
DWG NO 58065904
SH 23.0
REV G
58065904

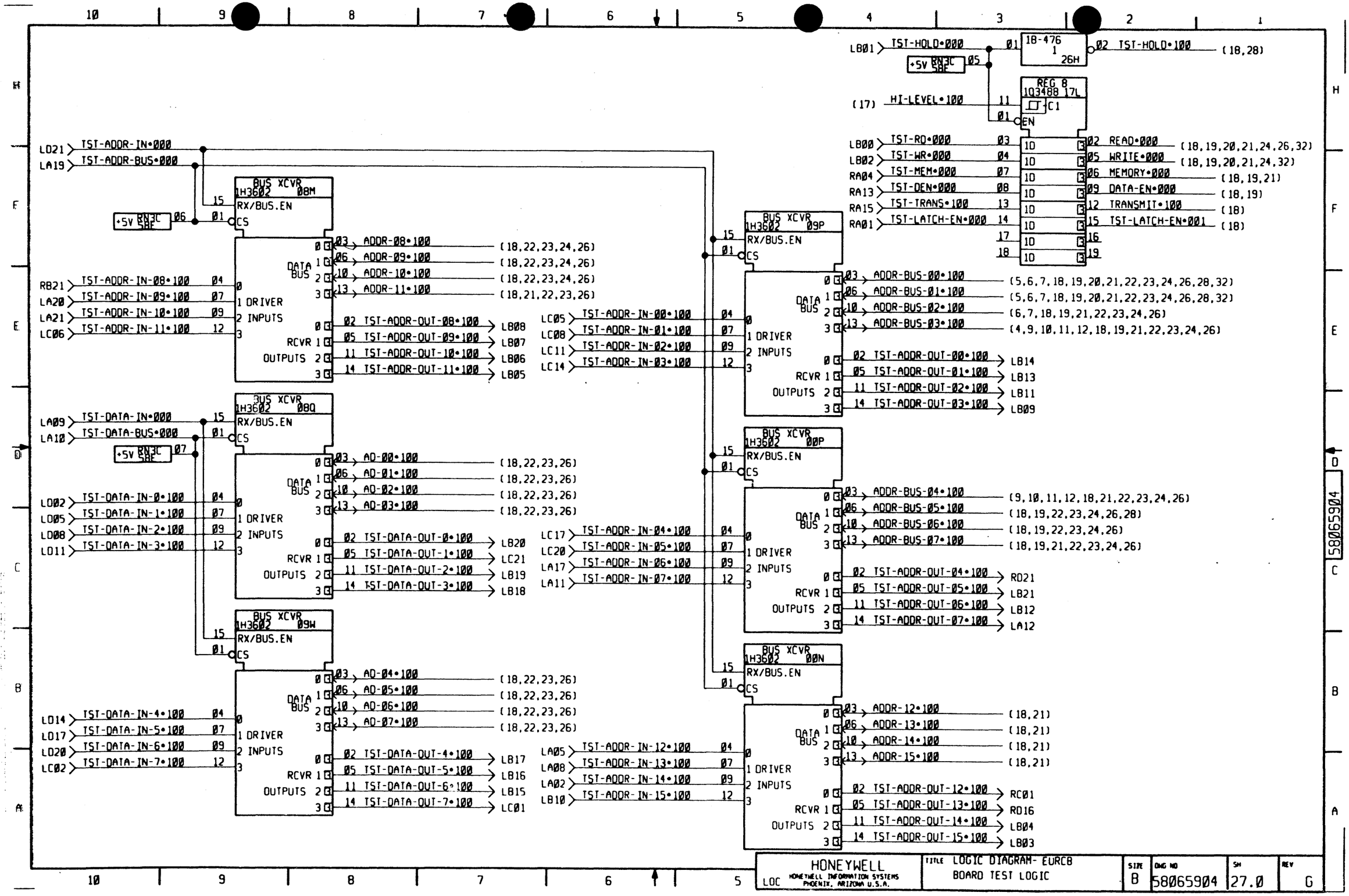

(18,27) ADDR-BUS-00•100
(18,27) ADDR-BUS-01•100
(18,27) ADDR-BUS-02•100
(18,27) ADDR-BUS-03•100
(18,27) ADDR-BUS-04•100
(18,27) ADDR-BUS-05•100
(18,27) ADDR-BUS-06•100
(18,27) ADDR-BUS-07•100
(18,27) ADDR-08•100
(18,27) ADDR-09•100
(18,27) ADDR-10•100
(16,27) WRITE•000
(18,27) READ•000
DATA-BUS2-0•100 (5,6,7,9,10,11,12,18,26)
DATA-BUS2-1•100 (5,6,7,9,10,11,12,18,26)
DATA-BUS2-2•100 (5,6,7,9,10,11,12,18,26)
DATA-BUS2-3•100 (5,6,7,9,10,11,12,18,26)
DATA-BUS2-4•100 (5,6,7,9,10,11,12,18,26)
DATA-BUS2-5•100 (5,6,7,9,10,11,12,18,26)
DATA-BUS2-6•100 (5,6,7,9,10,11,12,18,26)
DATA-BUS2-7•100 (5,6,7,9,10,11,12,18,26)
2KX8 RAM 1S3702 32M
2KX8 RAM 1S3702 45K
2KX8 RAM 1S3702 32K
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 R/W CS OE
I/01 I/02 I/03 I/04 I/05 I/06 I/07 I/08
(21) SEL-RAM-0•000
(21) SEL-RAM-1•000
(21) SEL-RAM-2•000
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- EURCB RAM (32-38K)
SIZE B
DWG NO 58065904
SH 24.0
REV G
58065904

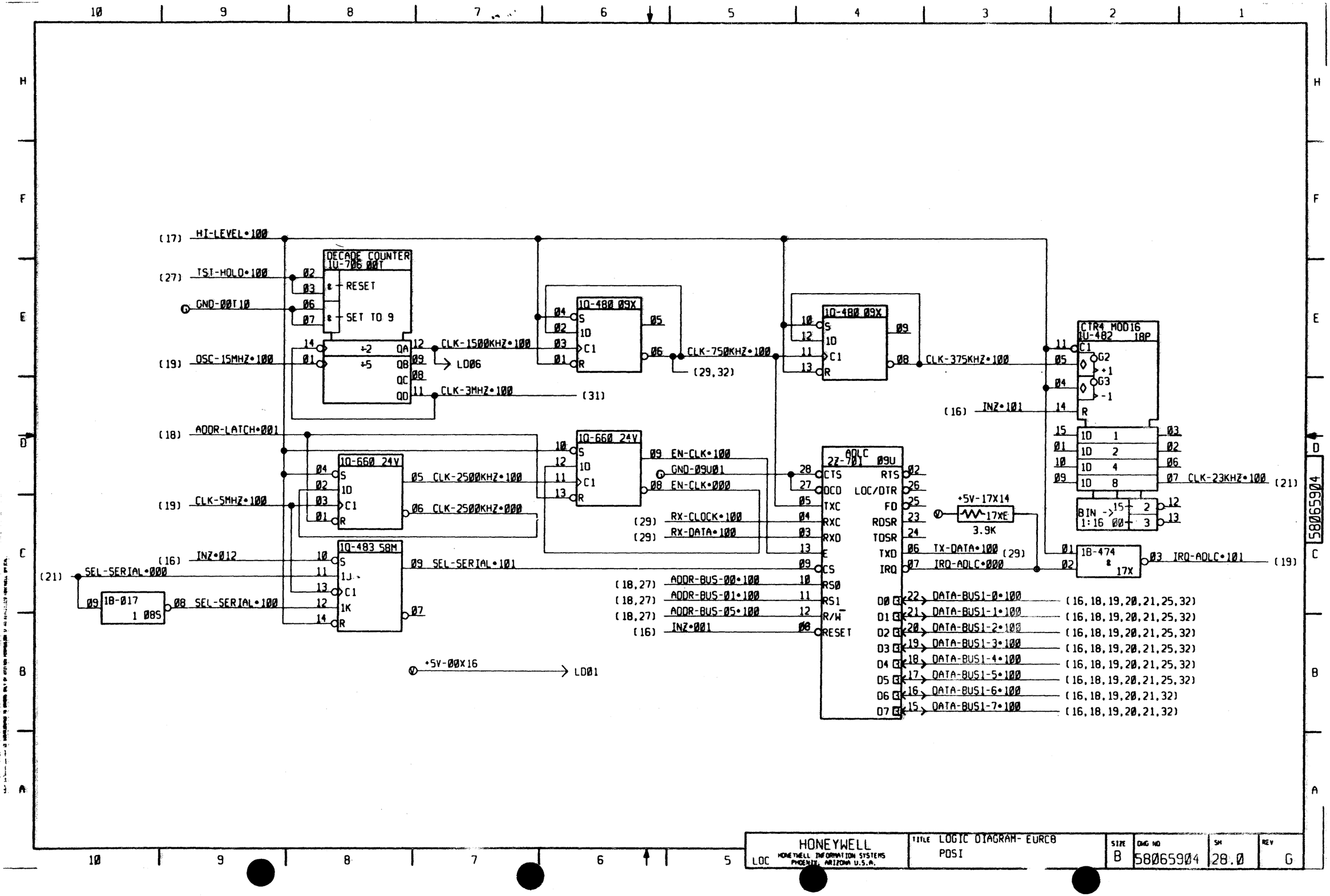


HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURCB DISPLAY, IO REG	SIZE B	DWG NO 58065904	SH 25.0	REV G
LOC					

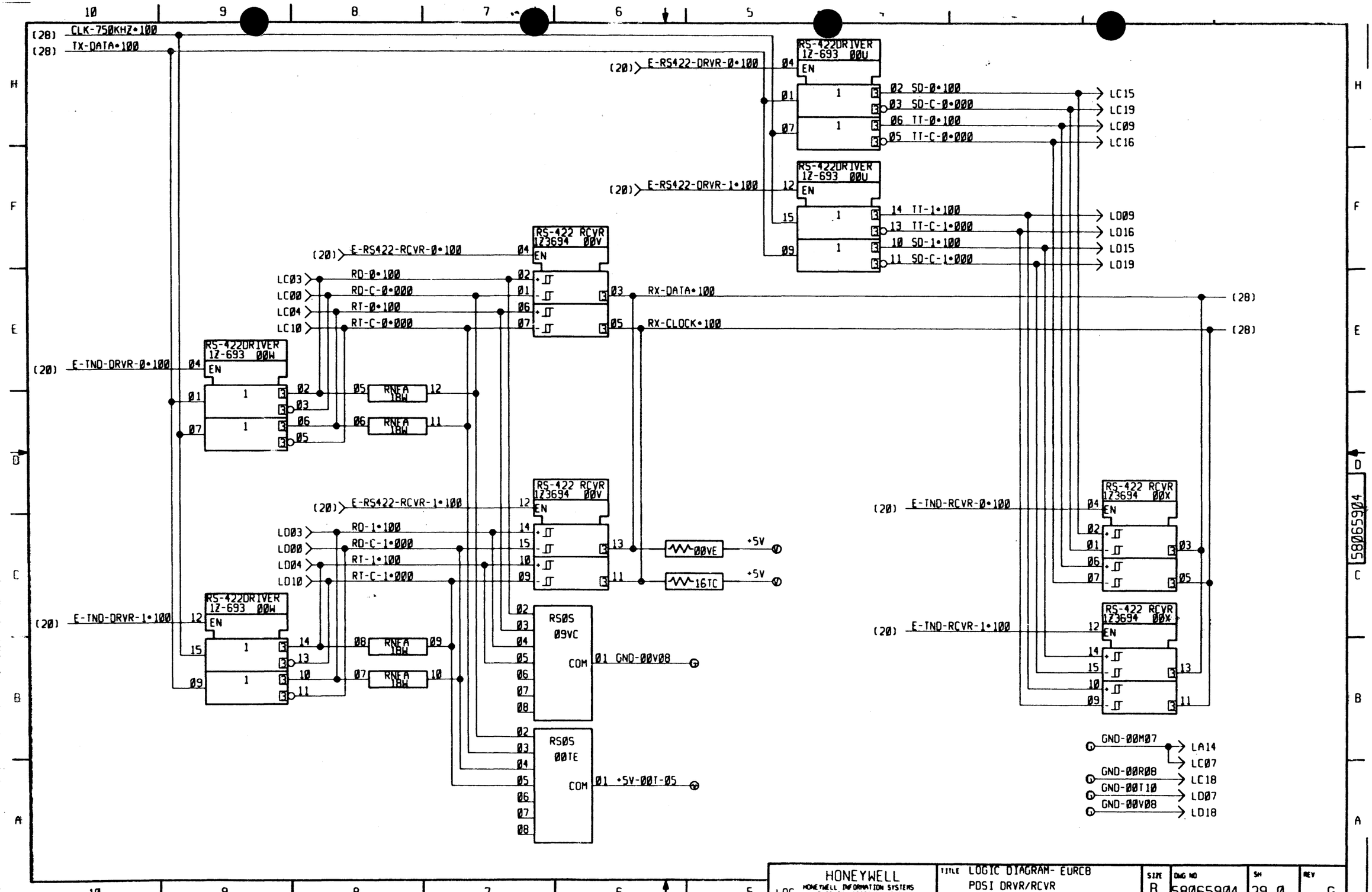
58065904


(18,27) ADDR-BUS-00•100
(18,27) ADDR-BUS-01•100
(18,27) ADDR-BUS-02•100
(18,27) ADDR-BUS-03•100
(18,27) ADDR-BUS-04•100
(18,27) ADDR-BUS-05•100
(18,27) ADDR-BUS-06•100
(18,27) ADDR-BUS-07•100
(18,27) ADDR-08•100
(18,27) ADDR-09•100
(18,27) ADDR-10•100
(18,27) ADDR-11•100
(18) READ•001
AD-00•100 (18,22,23,27)
AD-01•100 (18,22,23,27)
AD-02•100 (18,22,23,27)
AD-03•100 (18,22,23,27)
AD-04•100 (18,22,23,27)
AD-05•100 (18,22,23,27)
AD-06•100 (18,22,23,27)
AD-07•100 (18,22,23,27)
4KX8 EPROM 2R3689 16S
4KX8 EPROM 2R3689 19M
4KX8 EPROM 2R3689 45M
8 IN→1:4K
A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11
CE
OE/VPP
(21) SEL-PROM-6•000
(21) SEL-PROM-7•000
(21) SEL-PROM-ID•000
(18,27) READ•000
09 10 11 13 14 15 16 17
DATA-BUS2-0•100 (5,6,7,9,10,11,12,18,24)
DATA-BUS2-1•100 (5,6,7,9,10,11,12,18,24)
DATA-BUS2-2•100 (5,6,7,9,10,11,12,18,24)
DATA-BUS2-3•100 (5,6,7,9,10,11,12,18,24)
DATA-BUS2-4•100 (5,6,7,9,10,11,12,18,24)
DATA-BUS2-5•100 (5,6,7,9,10,11,12,18,24)
DATA-BUS2-6•100 (5,6,7,9,10,11,12,18,24)
DATA-BUS2-7•100 (5,6,7,9,10,11,12,18,24)
58065904
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- EURCB
EPROM (34-32K,TD (60-64K))
SIZE B
DWG NO 58065904
SH 26.0
REV G


BUS XCVR 1H3602 08M
RX/BUS.EN
CS
DATA BUS
1 DRIVER
2 INPUTS
RCVR OUTPUTS
BUS XCVR 1H3602 08Q
BUS XCVR 1H3602 09W
BUS XCVR 1H3602 09P
BUS XCVR 1H3602 00P
BUS XCVR 1H3602 00N
LO21 TST-ADDR-IN•000
LA19 TST-ADDR-BUS•000
+5V RN3C SHF
ADDR-08•100 (18,22,23,24,26)
ADDR-09•100 (18,22,23,24,26)
ADDR-10•100 (18,22,23,24,26)
ADDR-11•100 (18,21,22,23,26)
RB21 TST-ADDR-IN-08•100
LA20 TST-ADDR-IN-09•100
LA21 TST-ADDR-IN-10•100
LC06 TST-ADDR-IN-11•100
TST-ADDR-OUT-08•100 LB08
TST-ADDR-OUT-09•100 LB07
TST-ADDR-OUT-10•100 LB06
TST-ADDR-OUT-11•100 LB05
LC05 TST-ADDR-IN-00•100
LC08 TST-ADDR-IN-01•100
LC11 TST-ADDR-IN-02•100
LC14 TST-ADDR-IN-03•100
LA09 TST-DATA-IN•000
LA10 TST-DATA-BUS•000
AD-00•100 (18,22,23,26)
AD-01•100 (18,22,23,26)
AD-02•100 (18,22,23,26)
AD-03•100 (18,22,23,26)
LO02 TST-DATA-IN-0•100
LO05 TST-DATA-IN-1•100
LO08 TST-DATA-IN-2•100
LO11 TST-DATA-IN-3•100
TST-DATA-OUT-0•100 LB20
TST-DATA-OUT-1•100 LC21
TST-DATA-OUT-2•100 LB19
TST-DATA-OUT-3•100 LB18
LC17 TST-ADDR-IN-04•100
LC20 TST-ADDR-IN-05•100
LA17 TST-ADDR-IN-06•100
LA11 TST-ADDR-IN-07•100
AD-04•100 (18,22,23,26)
AD-05•100 (18,22,23,26)
AD-06•100 (18,22,23,26)
AD-07•100 (18,22,23,26)
LO14 TST-DATA-IN-4•100
LO17 TST-DATA-IN-5•100
LO20 TST-DATA-IN-6•100
LC02 TST-DATA-IN-7•100
TST-DATA-OUT-4•100 LB17
TST-DATA-OUT-5•100 LB16
TST-DATA-OUT-6•100 LB15
TST-DATA-OUT-7•100 LC01
LA05 TST-ADDR-IN-12•100
LA08 TST-ADDR-IN-13•100
LA02 TST-ADDR-IN-14•100
LB10 TST-ADDR-IN-15•100
LB01 TST-HOLD•000
IB-476 1 26H
TST-HOLD•100 (18,28)
REG 8 103488 17L
(17) HI-LEVEL•100
LB00 TST-RQ•000
LB02 TST-WR•000
RA04 TST-MEM•000
RA13 TST-DEN•000
RA15 TST-TRANS•100
RA01 TST-LATCH-EN•000
READ•000 (18,19,20,21,24,26,32)
WRITE•000 (18,19,20,21,24,32)
MEMORY•000 (18,19,21)
DATA-EN•000 (18,19)
TRANSMIT•100 (18)
TST-LATCH-EN•001 (18)
ADDR-BUS-00•100 (5,6,7,18,19,20,21,22,23,24,26,28,32)
ADDR-BUS-01•100 (5,6,7,18,19,20,21,22,23,24,26,28,32)
ADDR-BUS-02•100 (6,7,18,19,21,22,23,24,26)
ADDR-BUS-03•100 (4,9,10,11,12,18,19,21,22,23,24,26)
TST-ADDR-OUT-00•100 LB14
TST-ADDR-OUT-01•100 LB13
TST-ADDR-OUT-02•100 LB11
TST-ADDR-OUT-03•100 LB09
ADDR-BUS-04•100 (9,10,11,12,18,21,22,23,24,26)
ADDR-BUS-05•100 (18,19,22,23,24,26,28)
ADDR-BUS-06•100 (18,19,22,23,24,26)
ADDR-BUS-07•100 (18,19,21,22,23,24,26)
TST-ADDR-OUT-04•100 RO21
TST-ADDR-OUT-05•100 LB21
TST-ADDR-OUT-06•100 LB12
TST-ADDR-OUT-07•100 LA12
ADDR-12•100 (18,21)
ADDR-13•100 (18,21)
ADDR-14•100 (18,21)
ADDR-15•100 (18,21)
TST-ADDR-OUT-12•100 RC01
TST-ADDR-OUT-13•100 RO16
TST-ADDR-OUT-14•100 LB04
TST-ADDR-OUT-15•100 LB03
HONEYWELL
HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
LOC
TITLE LOGIC DIAGRAM- EURCB BOARD TEST LOGIC
SIZE B
DWG NO 58065904
SH 27.0
REV G
58065904

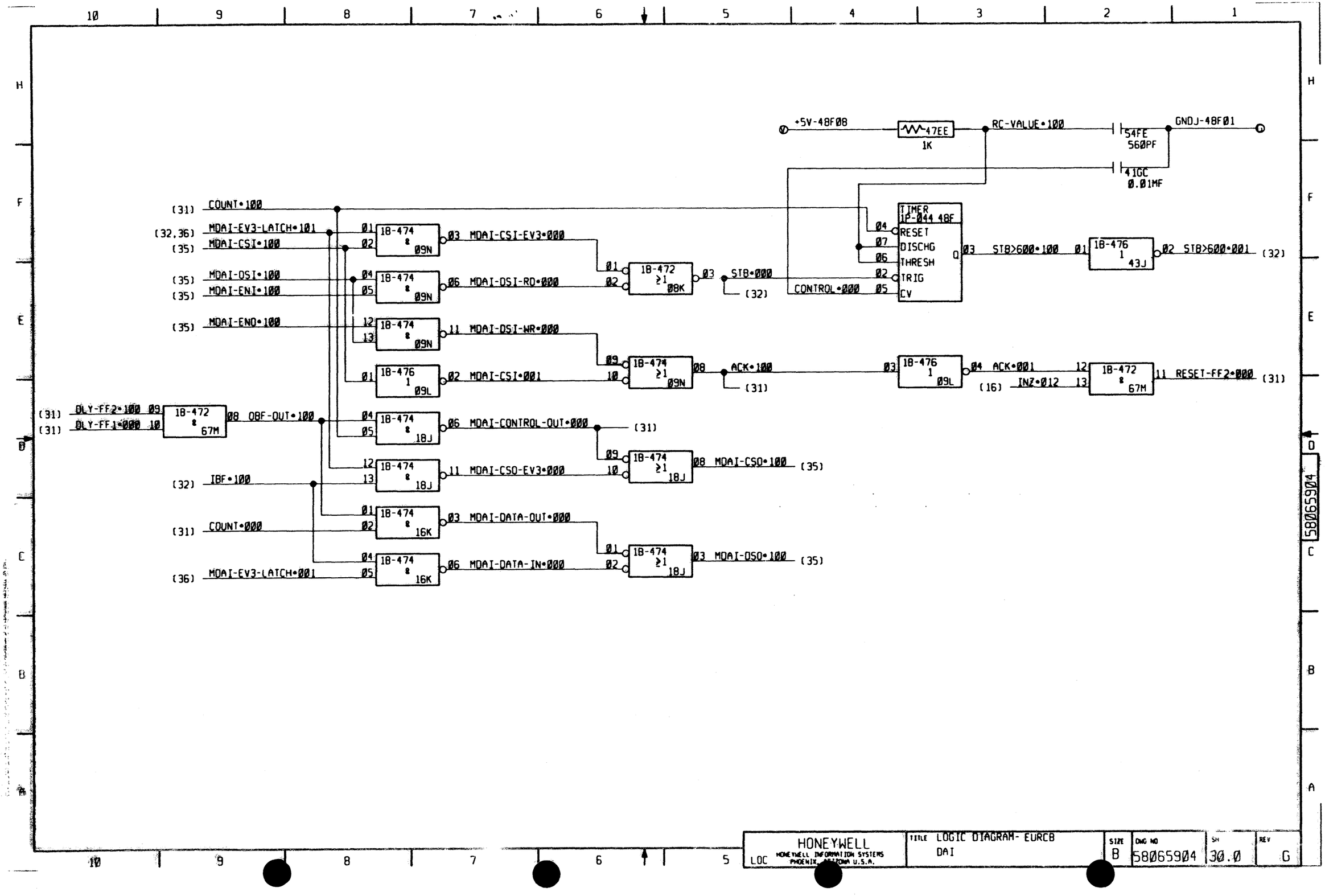


HONEYWELL LOC — HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURC8 POSI	SIZE B	DWG NO 58065904	SH 28.0	REV G



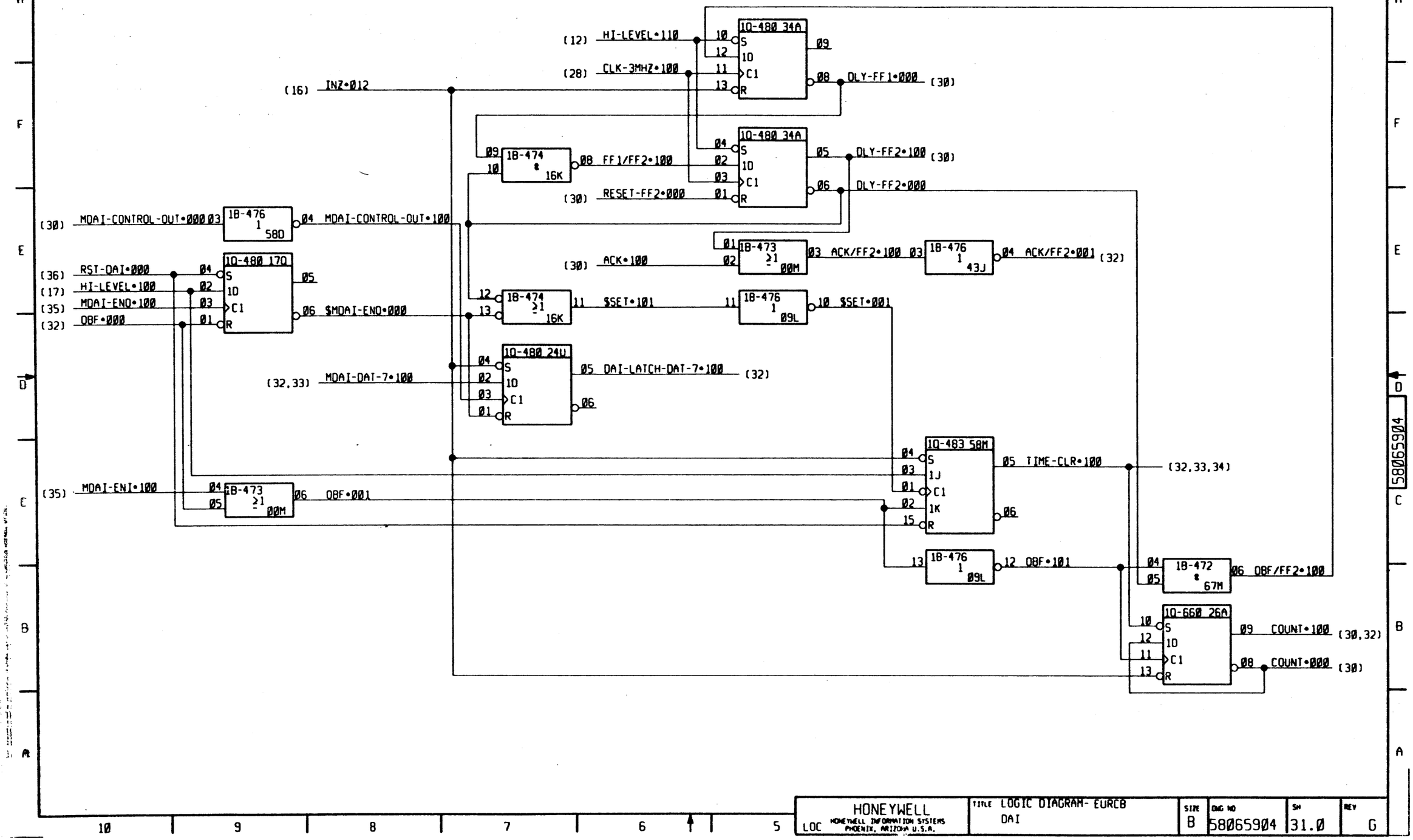
HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURCB POSI DRVR/RCVR	SIZE B	DWG NO 58065904	SH 29.0	REV G

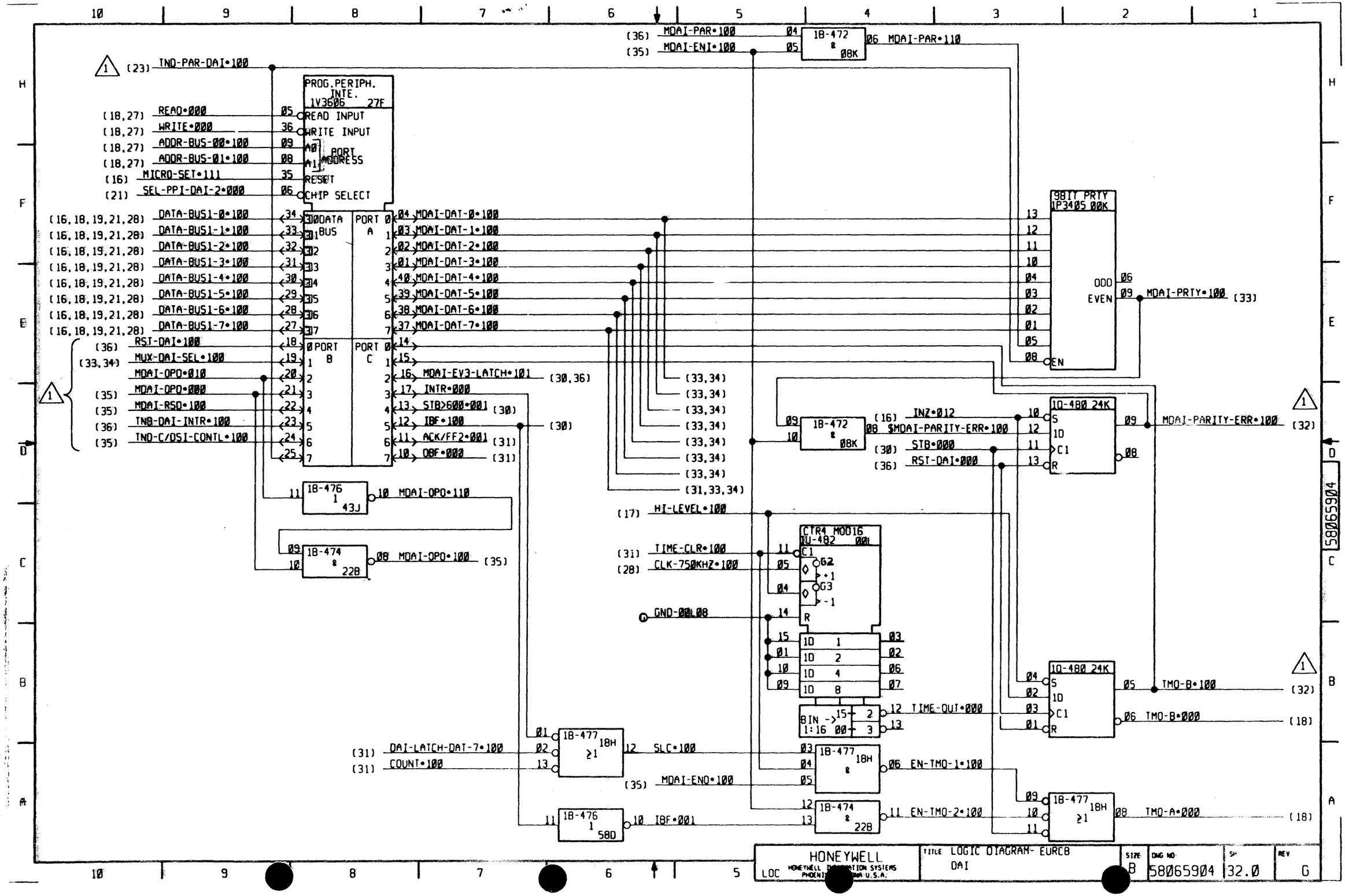
58065904

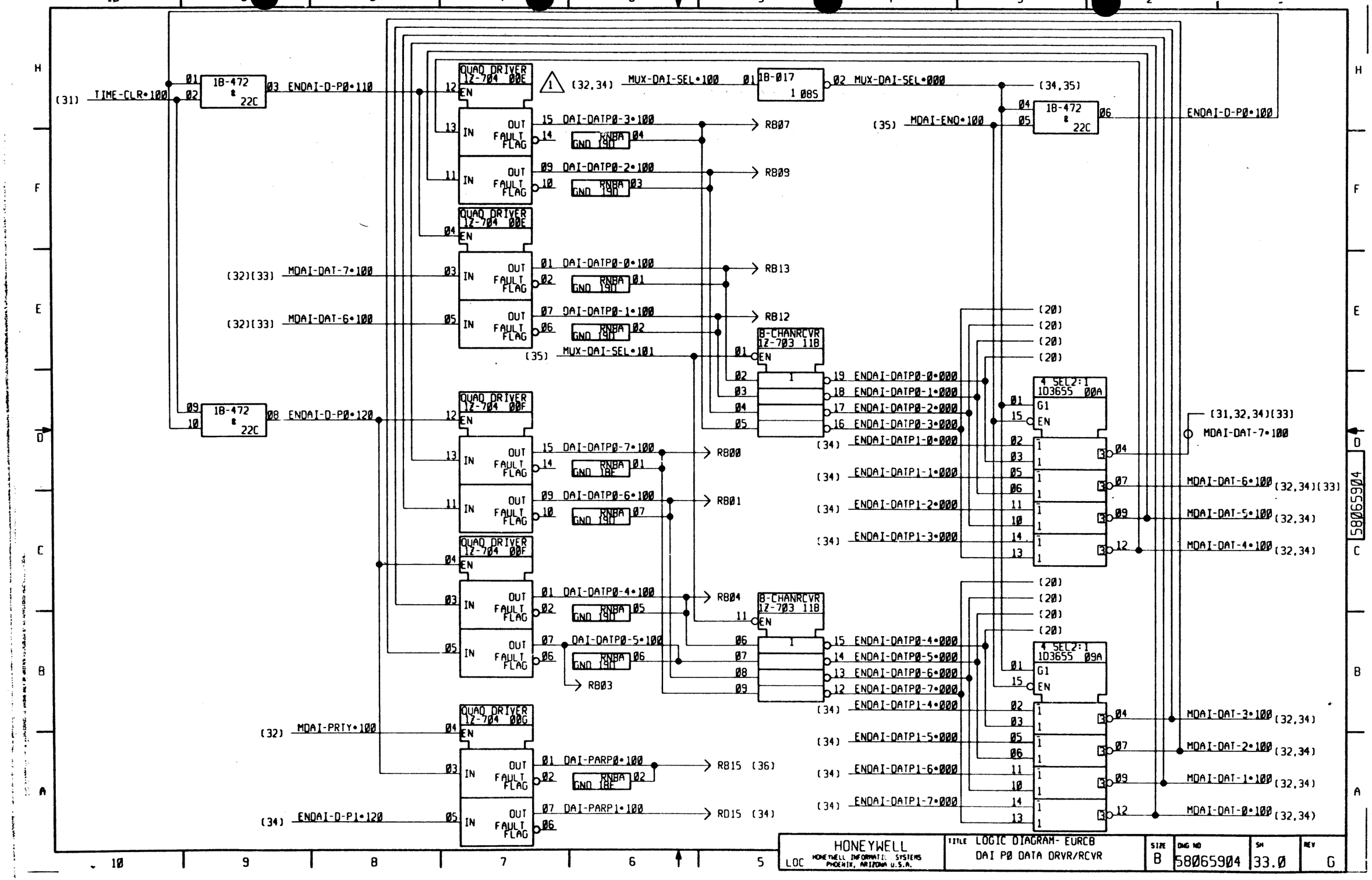


HONEYWELL LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURCB DAI	SIZE B	DWG NO 58065904	SH 30.0	REV G

58065904


10-480 34A
(12) HI-LEVEL•110
(28) CLK-3MHZ•100
(16) INZ•012
09
08 DLY-FF1•000 (30)
1B-474 ≥1 16K
08 FF1/FF2•100
(30) RESET-FF2•000
10-480 34A
05 DLY-FF2•100 (30)
06 DLY-FF2•000
(30) MDAI-CONTROL-OUT•000 03
1B-476 1 58D
04 MDAI-CONTROL-OUT•100
(30) ACK•100
1B-473 ≥1 00M
03 ACK/FF2•100 03
1B-476 1 43J
04 ACK/FF2•001 (32)
10-480 17D
(36) RSI-DAI•000
(17) HI-LEVEL•100
(35) MDAI-ENQ•100
(32) OBF•000
05
06 $MDAI-ENQ•000
1B-474 ≥1 16K
11 $SET•101
1B-476 1 09L
10 $SET•001
10-480 24U
(32,33) MDAI-DAI-7•100
05 DAI-LATCH-DAI-7•100 (32)
06
10-483 58M
05 TIME-CLR•100
(32,33,34)
(35) MDAI-ENI•100
1B-473 ≥1 00M
06 OBF•001
1B-476 1 09L
12 OBF•101
1B-472 ≥1 67M
06 OBF/FF2•100
10-660 26A
09 COUNT•100 (30,32)
08 COUNT•000 (30)
58065904
HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- EURC8 DAI
SIZE B
DWG NO 58065904
SH 31.0
REV G

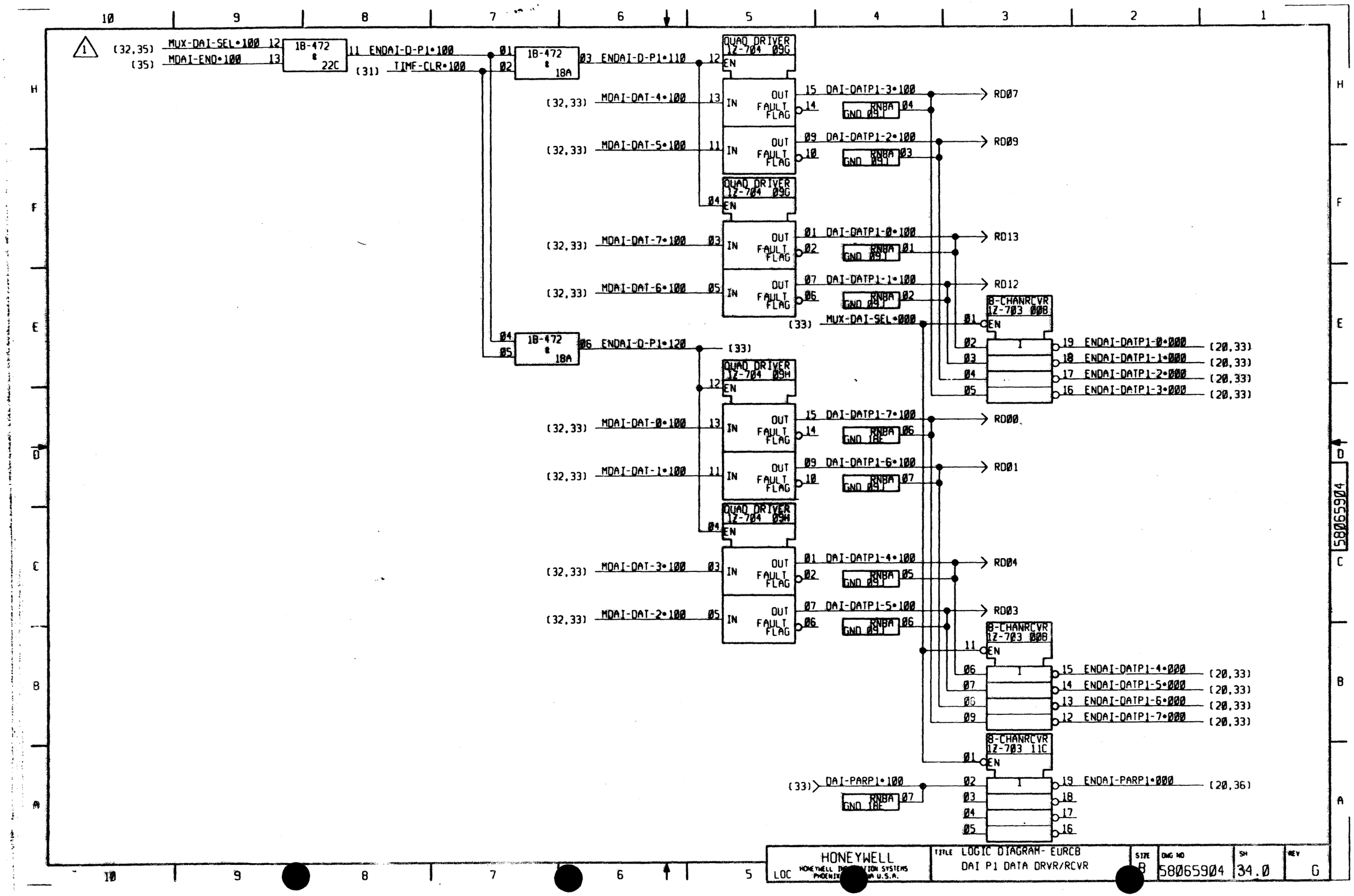

10 9 8 7 6 5 4 3 2 1
H F E D C B A
(36) MDAI-PAR•100
(35) MDAI-ENI•100
1B-472 8 08K
06 MDAI-PAR•110
(23) IND-PAR-DAI•100
PROG.PERIPH. INTE. 1V3606 27F
(18,27) READ•000 05 READ INPUT
(18,27) WRITE•000 36 WRITE INPUT
(18,27) ADDR-BUS-00•100 09 A0
(18,27) ADDR-BUS-01•100 08 A1 PORT ADDRESS
(16) MICRO-SEI•111 35 RESET
(21) SEL-PPI-DAI-2•000 06 CHIP SELECT
(16,18,19,21,28) DATA-BUS1-0•100 34
(16,18,19,21,28) DATA-BUS1-1•100 33
(16,18,19,21,28) DATA-BUS1-2•100 32
(16,18,19,21,28) DATA-BUS1-3•100 31
(16,18,19,21,28) DATA-BUS1-4•100 30
(16,18,19,21,28) DATA-BUS1-5•100 29
(16,18,19,21,28) DATA-BUS1-6•100 28
(16,18,19,21,28) DATA-BUS1-7•100 27
30 DATA BUS 37
PORT A
PORT 0 04 MDAI-DAT-0•100
1 03 MDAI-DAT-1•100
2 02 MDAI-DAT-2•100
3 01 MDAI-DAT-3•100
4 40 MDAI-DAT-4•100
5 39 MDAI-DAT-5•100
6 38 MDAI-DAT-6•100
7 37 MDAI-DAT-7•100
(36) RSI-DAI•100 18
(33,34) MUX-DAI-SEL•100 19
MDAI-OPO•010 20
(35) MDAI-OPO•000 21
(35) MDAI-RSO•100 22
(36) TNB-DAI-INTR•100 23
(35) IND-C/DSI-CONTL•100 24
25
0 PORT B 7
PORT C
14
15
16 MDAI-EV3-LATCH•101 (30,36)
17 INTR•000
13 STB>600•001 (30)
12 IBF•100 (30)
11 ACK/FF2•001 (31)
10 OBF•000 (31)
(33,34)
(31,33,34)
(17) HI-LEVEL•100
1B-476 1 43J
11 10 MDAI-OPO•110
1B-474 8 22B
09 10 08 MDAI-OPO•100 (35)
9BIT PRTY 1P3405 00K
13 12 11 10 04 03 02 01 05 08 EN
ODD EVEN 06 09 MDAI-PRTY•100 (33)
1B-472 8 08K
09 10
(16) INZ•012 10
08 $MDAI-PARITY-ERR•100 12
(30) STB•000 11
(36) RST-DAI•000 13
10-480 24K
S 1D C1 R
09 MDAI-PARITY-ERR•100 (32)
08
(31) TIME-CLR•100 11
(28) CLK-750KHZ•100 05
04
CTR4 MOD16 TU-482 00L
C1 G2 +1 G3 -1
GND-00L08 14
R
15 01 10 09
1D 1 2 4 8
03 02 06 07
BIN -> 1:16
15 00
2 3
12 13
TIME-OUT•000
10-480 24K
04 02 03 01
S 1D C1 R
05 TMO-B•100 (32)
06 TMO-B•000 (18)
(31) DAI-LATCH-DAI-7•100
(31) COUNT•100
1B-477 18H ≥1
01 02 13 12 SLC•100
(35) MDAI-ENO•100
1B-476 1 58D
11 10 IBF•001
1B-477 18H 8
03 04 05 06 EN-TMO-1•100
1B-474 8 22B
12 13 11 EN-TMO-2•100
1B-477 18H ≥1
09 10 11 08 TMO-A•000 (18)
58065904
HONEYWELL
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX ARIZONA U.S.A.
TITLE LOGIC DIAGRAM- EURCB DAI
SIZE B
DWG NO 58065904
SH 32.0
REV G

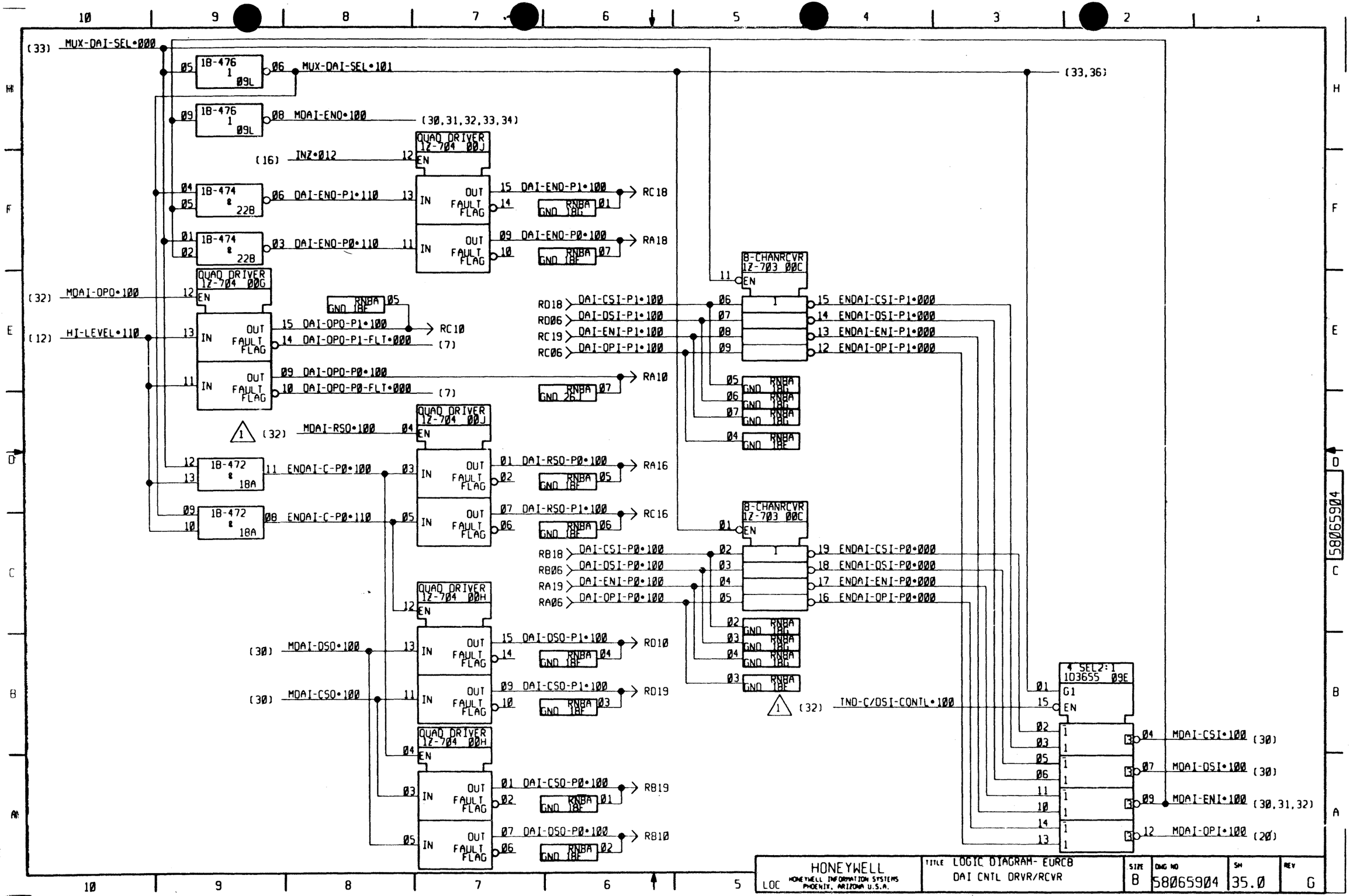


HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURCB DAI P0 DATA DRVR/RCVR	SIZE B	DWG NO 58065904	SH 33.0	REV G

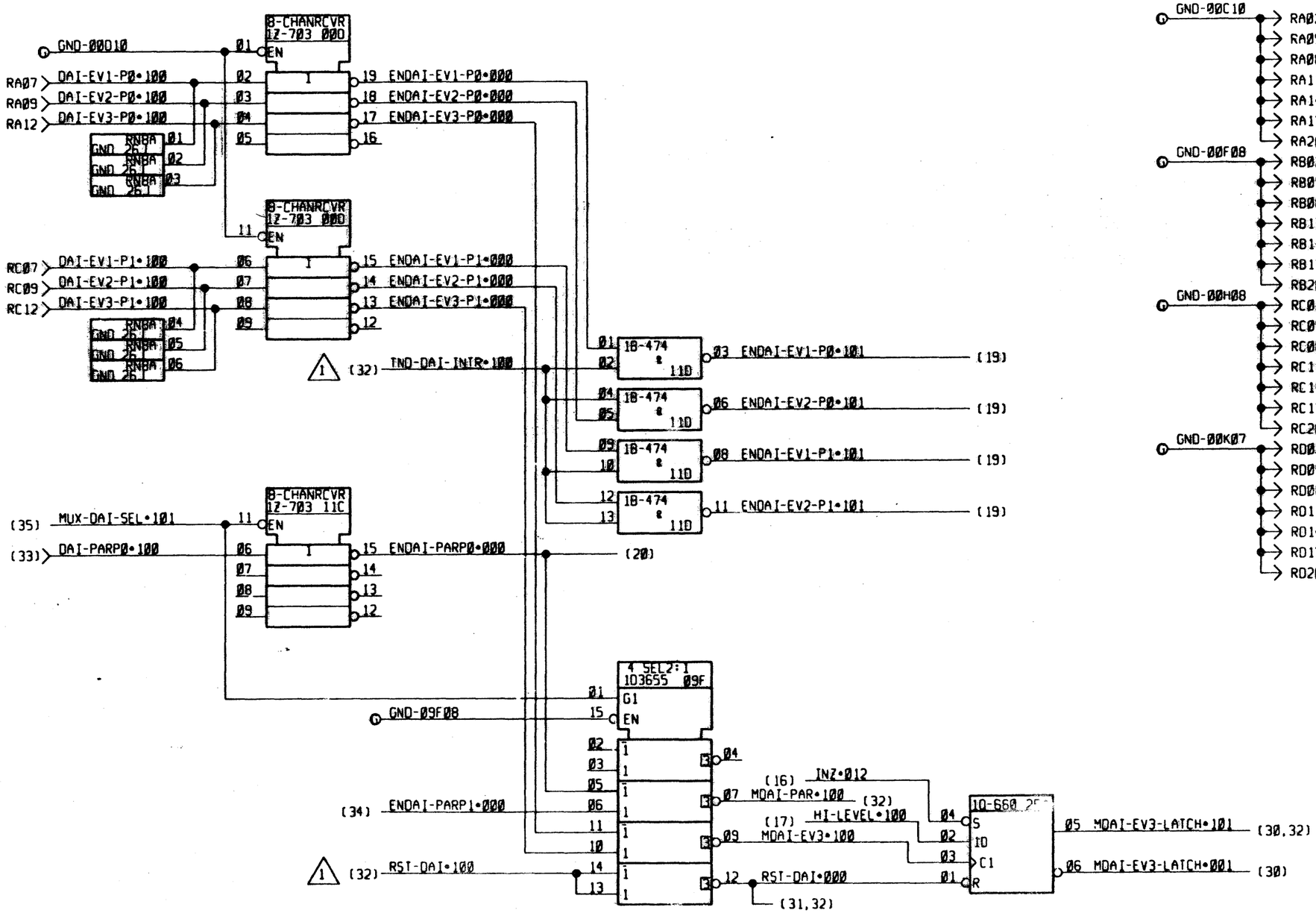
LOC

58065904


10
9
8
7
6
5
4
3
2
1
H
F
E
D
C
B
A
1
(32,35) MUX-DAI-SEL•100 12
(35) MDAI-ENO•100 13
1B-472 & 22C
11 ENDAI-D-P1•100
(31) TIMF-CLR•100
01
02
1B-472 & 18A
03 ENDAI-D-P1•110
04 ENDAI-D-P1•120
05
1B-472 & 18A
QUAD DRIVER 1Z-704 09G
QUAD DRIVER 1Z-704 09H
EN
IN
OUT
FAULT FLAG
(32,33) MDAI-DAI-4•100 13
(32,33) MDAI-DAI-5•100 11
(32,33) MDAI-DAI-7•100 03
(32,33) MDAI-DAI-6•100 05
(32,33) MDAI-DAI-0•100 13
(32,33) MDAI-DAI-1•100 11
(32,33) MDAI-DAI-3•100 03
(32,33) MDAI-DAI-2•100 05
15 DAI-DATP1-3•100
09 DAI-DATP1-2•100
01 DAI-DATP1-0•100
07 DAI-DATP1-1•100
15 DAI-DATP1-7•100
09 DAI-DATP1-6•100
01 DAI-DATP1-4•100
07 DAI-DATP1-5•100
14
10
02
06
RNBA GND 09
04
03
01
07
RD07
RD09
RD13
RD12
RD00
RD01
RD04
RD03
(33) MUX-DAI-SEL•000
8-CHANRCVR 1Z-703 00B
8-CHANRCVR 1Z-703 08B
8-CHANRCVR 1Z-703 11C
19 ENDAI-DATP1-0•000 (20,33)
18 ENDAI-DATP1-1•000 (20,33)
17 ENDAI-DATP1-2•000 (20,33)
16 ENDAI-DATP1-3•000 (20,33)
15 ENDAI-DATP1-4•000 (20,33)
14 ENDAI-DATP1-5•000 (20,33)
13 ENDAI-DATP1-6•000 (20,33)
12 ENDAI-DATP1-7•000 (20,33)
(33) DAI-PARP1•100
19 ENDAI-PARP1•000 (20,36)
HONEYWELL
LOC
TITLE LOGIC DIAGRAM- EURCB
DAI P1 DATA DRVR/RCVR
SIZE B
DWG NO 58065904
SH 34.0
REV G
58065904



HONEYWELL HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	TITLE LOGIC DIAGRAM- EURCB DAI CNTL DRVR/RCVR	SIZE B	DWG NO 58065904	SH 35.0	REV G



58065904

TOTAL NUMBER OF SHEETS = 41

HONEYWELL	TITLE	SIZE	DWG NO	SH	REV
LOC HONEYWELL INFORMATION SYSTEMS PHOENIX, ARIZONA U.S.A.	LOGIC DIAGRAM- EURC8 DAI EVENT RCVR	B	58065904	36.0F	G

58065900

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	102	002	203	103	003	304	204	104	004	405	305	205	105	506	406	306	206	PL	DWG
A	LEVEL I ISSUE	80	07	31	Chuck Vimont 7-24-80	A																		A	
B	PHAØDP001	81	04	06	Thackelford	B																		B	
C	PHAØDP003	81	07	28	[illegible]	C	C	C																C	
D	PHAØDP004	81	AUG	27	Thackelford		D	D	D	D	D													D	
E	PHAØDP008	81	10	09	Thackelford	OBSOLETE	OBSOLETE	OBSOLETE	E	E	E	E	E	E	E									E	
F	PHAØDP011	81	OCT	27	[illegible]				OBSOLETE	OBSOLETE	OBSOLETE	F	F	F	F	F	F	F	F					F	
G	PHAØDP012	81	NOV	18	Thackelford											G	G	G	G	G	G	G	G	G	G
H	PHAØDP013	82	FEB	18	Thackelford							OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	H (OBSOLETE)	H (OBSOLETE)	H (OBSOLETE)	H (OBSOLETE)	H	H
																									/
																									/
																									/
																									/
																									/
																									/
	58065904				LOGIC DIAG				A	A	A	B	B	B	B	C	C	C	C	C	C	C	C		DELETED
					TEST DATA																				

FOR CONTINUATION OF REVISION STATUS SEE SHEET 2

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

CE 300 A-3 (1-79)

MADE BY Thackelford 80 JUL 23

APPROVED J Abel 7/23/80

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE HDUHC PWA EURCB

SIZE	REVISION STATUS FOR	SHEET	REV
X	58065900	1/3	M

DIST. C127-30

58065900

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 506	406	306	206	607	507	407	307	708	508	408	008	709	609	509	109	009		PL ALL	DWG 1
H	PHAØDP013	82	02	18		H	H	H	H	H	H	H	H											H	H
J	PHAØDP015	82	03	03		OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	J	J	J	J	J	J	J	J							J	
K	PHAØDP017		ND			OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	K	K	K	K	K	K	K	K	K		K	
L	PHAØDP018	82	APR	01														L	L	L	L	L		L	
M	PHAØDP028	83	JAN	24										OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	M	M	M	M	M		M	DELETED
	58065904				LOGIC DIAGRAM	C	C	C	C	D	D	D	D	E	E	E	E	F	F	F	F	F	G		
	58065907				TEST DATA	A	A	A	A	B	B	B	B	C	C	C	C	D	D	D	D	D	E		

FOR CONTINUATION OF REVISION STATUS SEE SHEET 3

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

CE 300 A-3 (1-79)

MADE BY [signature] 80 JUL 23

APPROVED J. ABEL 7/23/80

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

DIST. C127-30

TITLE HDUHC PWA EURCB

SIZE	REVISION STATUS FOR	SHEET	REV
X	58065900	2	M

58065900

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 9/10	7/10	6/10	2/10	1/10	0/10	PL ALL
M	PHAØDP028	83	JAN	24	E R Sersanie	M	M	M	M	M	M	M
N	PHAØDP037	83	07	13	G. Miller	N	N	N	N	N	N	
P	PHAØDP052	83	12	05	T. Driscoll	P	P	P	P	P	P	
	58065904				LOGIC DIAG.	G	G	G	G	G	G	
	58065907				TEST DATA	F	F	F	F	F	F	

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY E R Sersanie 9/23-'82

APPROVED J. ABEL 1/18/83

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE HDUHC PWA EURCB

SIZE	REVISION STATUS FOR	SHEET	REV
X	58065900	3F	P

DIST. C127-30

BRUNING 44-141 40366

CE 300 A-3 (1-79)

58065902

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 001	002	003	004	005	006	SH
A	LVL 1 ISSUE	81	04	06	Chuck Vonovich 3-31-81	A						A
B	PHAØDP003	81	07	28	S Dragoun	B	B					B
C	PHAØDP004	81	AUG	27	D. Kajurski		C	C				C
D	PHAØDP008 & LVL 3 ISSUE PER EWA 28400	81	10	07	D. Kajurski	OBSOLETE	OBSOLETE	D	D	D		D
E	PHAØDP013	82	FEB	18	D. Kajurski			OBSOLETE	E	E		E 1-10F
F	PHAØDP028	83	JAN	24	T. Arcuri				OBSOLETE	F	F	F 1-10F

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY D. Kauffman 81 Mar 20

APPROVED M. Carlson 81 Mar 24

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

DIST. C127 -37

TITLE CIL EURCB

SIZE	REVISION STATUS FOR	SHEET	REV
A	58065902	1/1	F

BRUNING 44-141 40366

CE 388 A-3 (1-79)

TAB-006

STANDARD LOCATION CODE PATTERN
X-POS & Y-POS PER 58046507-002
UNLESS OTHERWISE SHOWN, ROTATION IS NORTH

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00A	1D3655	58002655-001			
00AE	P9	43A114748P9			
00B	1Z-703	58002703-001			
00C	1Z-703	58002703-001			
00CE	P9	43A114748P9			
00D	1Z-703	58002703-001			
00E	1Z-704	58002704-001			
00EE	P9	43A114748P9			
00F	1Z-704	58002704-001			
00G	1Z-704	58002704-001			
00GE	P9	43A114748P9			
00H	1Z-704	58002704-001			
00J	1Z-704	58002704-001			
00JE	P9	43A114748P9			
00K	1P3405	43C216405P1			
00L	1U-482	58002482-001			
00LE	P9	43A114748P9			
00M	1B-473	58002473-001			
00N	1H3602	58002602-001			
00NE	P9	43A114748P9			
00P	1H3602	58002602-001			
00Q	RN1H	43B216592P40			
00QE	P9	43A114748P9			
00R	1Q-059	58002059-001			
00S	1B-476	58002476-001			
00SE	P9	43A114748P9			
00T	1U-706	58002706-001			
00TE	RSOS	58020479-016			
00U	1Z-693	58002693-001			
00UE	P9	43A114748P9			
00V	1Z3694	58002694-001			
00VE	P049	70928100-049			

COMP INSTL LIST - EURCB

TAB-OD6

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
00W	1Z-693	58002693-001			
00WE	P9	43A114748P9			
00X	1Z3694	58002694-001			
08AE	P1043	43C212092P1043			
08CE	P1043	43C212092P1043			
08EE	P1043	43C212092P1043			
08GE	P1043	43C212092P1043			
08JE	P1043	43C212092P1043			
08K	1B-472	58002472-001			
08LE	P1043	43C212092P1043			
08N	1H3602	58002602-001			
08NE	P1043	43C212092P1043			
08Q	1H3602	58002602-001			
08QE	P1043	43C212092P1043			
08S	1B-017	58002017-001			
08SE	P1043	43C212092P1043			
08T	1B-473	58002473-001			
08VE	P1043	43C212092P1043			
08WE	P1043	43C212092P1043			
09A	1D3655	58002655-001			
09E	1D3655	58002655-001			
09F	1D3655	58002655-001			
09G	1Z-704	58002704-001			
09H	1Z-704	58002704-001			
09J	RN8A	43B216592P23			
09L	1B-476	58002476-001			
09N	1B-474	58002474-001			
09P	1H3602	58002602-001			
09R	1Q-485	58002485-001			
09U	2Z-701	58002701-001			
09VC	RSOS	58020479-016			
09W	1H3602	58002602-001			
09X	1Q-480	58002480-001			
11B	1Z-703	58002703-001			
11C	1Z-703	58002703-001			
11D	1B-474	58002474-001			
16AE	P1043	43C212092P1043			
16CE	P1043	43C212092P1043			

TAB-006

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
16EE	P1043	43C212092P1043			
16GE	P1043	43C212092P1043			
16JE	P1043	43C212092P1043			
16K	1B-474	58002474-001			
16LE	P1043	43C212092P1043			
16NE	P1043	43C212092P1043			
16S	SK24	58020384-006			
16S	2R3689	*---------*			
16TC	P049	70928100-049			
16TE	P1043	43C212092P1043			
16VE	P1043	43C212092P1043			
16WE	P1043	43C212092P1043			
17L	1Q3488	58002488-001			
17NC	P090	70928100-090			
17Q	1Q-480	58002480-001			
17X	1B-474	58002474-001			
17XE	P063	70928100-063			
18A	1B-472	58002472-001			
18E	RN8A	43B216592P23			
18F	RN8A	43B216592P23			
18G	RN8A	43B216592P23			
18H	1B-477	58002477-001			
18J	1B-474	58002474-001			
18P	1U-482	58002482-001			
18R	XLON	43C216118P50			
18W	RNFA	43B216592P47			
19D	RN8A	43B216592P23			
19M	2R3689	*---------*			
19M	SK24	58020384-006			
22B	1B-474	58002474-001			
22C	1B-472	58002472-001			
24AE	P9	43A114748P9			
24CE	P9	43A114748P9			
24EE	P9	43A114748P9			
24GE	P9	43A114748P9			
24JE	P9	43A114748P9			
24K	1Q-480	58002480-001			
24LE	P9	43A114748P9			

COMP INSTL LIST - EURCB

TAB-006

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
24NC	P2742	43C212092P2742			
24NE	P9	43A114748P9			
24TE	P9	43A114748P9			
24U	1Q-480	58002480-001			
24UE	P9	43A114748P9			
24V	1Q-660	58002660-001			
24WE	P9	43A114748P9			
25Q	1B3691	58002691-001			
26A	1Q-660	58002660-001			
26H	1B-476	58002476-001			
26J	RN8A	43B216592P23			
26R	1Z-690	58002690-001			
27F	1V3606	58002606-001			
27P	1B-664	58002664-001			
28D	1V3606	58002606-001			
29S	SK24	58020384-006			
29S	2R3689	*----------*			
30B	2V-576	58002576-001			
32AE	P1043	43C212092P1043			
32CE	P1043	43C212092P1043			
32EE	P1043	43C212092P1043			
32GE	P1043	43C212092P1043			
32JE	P1043	43C212092P1043			
32K	2S3702	58002702-001			
32LE	P1043	43C212092P1043			
32M	2S3702	58002702-001			
32NE	P1043	43C212092P1043			
32PE	P1043	43C212092P1043			
32RE	P1043	43C212092P1043			
32TE	P1043	43C212092P1043			
32U	2R3689	*----------*			
32U	SK24	58020384-006			
32VE	P1043	43C212092P1043			
32W	2R3689	*----------*			
32W	SK24	58020384-006			
32XE	P1043	43C212092P1043			
34A	1Q-480	58002480-001			
34H	1B-472	58002472-001			

TAB-006

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
35J	1B-478	58002478-001			
35P	1Q3692	58002692-001			
36Q	2V-688	58002688-001			
36Q	SK40	58020384-008			
38NC	P063	70928100-063			
40AE	P1043	43C212092P1043			
40CE	P1043	43C212092P1043			
40EC	P085	70928100-085			
40EE	P1043	43C212092P1043			
40GE	P1043	43C212092P1043			
40JE	P1043	43C212092P1043			
40LE	P1043	43C212092P1043			
40NE	P1043	43C212092P1043			
40PE	P1043	43C212092P1043			
40RE	P1043	43C212092P1043			
40TE	P1043	43C212092P1043			
40VE	P1043	43C212092P1043			
40XE	P1043	43C212092P1043			
41GC	P1033	43C212092P1033			
42A	1P3405	43C216405P1			
42H	1C-648	58002648-001			
42S	2R3689	*----------*			
42S	SK24	58020384-006			
43J	1B-476	58002476-001			
45B	2V-574	58002574-001			
45K	2S3702	58002702-001			
45M	SK24	58020384-006			
45M	2R3689	*----------*			
45U	2R3689	*----------*			
45U	SK24	58020384-006			
45W	SK24	58020384-006			
45W	2R3689	*----------*			
46P	1B3691	58002691-001			
47FE	P049	70928100-049			
48AE	P9	43A114748P9			
48CE	P9	43A114748P9			
48EE	P9	43A114748P9			
48F	1P6044	58002044-002			

COMP INSTL LIST - EURCB

TAB-006

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
48GE	P9	43A114748P9			
48JE	P9	43A114748P9			
48LE	P9	43A114748P9			
48NE	P9	43A114748P9			
48PE	P9	43A114748P9			
48RE	P9	43A114748P9			
48TE	P9	43A114748P9			
48VE	P9	43A114748P9			
48XE	P9	43A114748P9			
49B	1C-648	58002648-001			
49E	1C-648	58002648-001			
50A	1P3405	43C216403P1			
50CC	P037	70928100-037			
51H	1C-648	58002648-001			
54FE	P5613	43C212092P5613			
55S	1B-478	58002478-001			
55T	1B-473	58002473-001			
56AE	P1043	43C212092P1043			
56CE	P1043	43C212092P1043			
56EE	P1043	43C212092P1043			
56F	1E-011	58002011-001			
56GE	P1043	43C212092P1043			
56JE	P1043	43C212092P1043			
56LE	P1043	43C212092P1043			
56NE	P1043	43C212092P1043			
56QE	P1043	43C212092P1043			
56SE	P1043	43C212092P1043			
56TE	P1043	43C212092P1043			
56VE	P1043	43C212092P1043			
57Q	1Q3488	58002488-001			
57R	1D3492	58002492-001			
58A	SWDG	58020295-007			
58B	1E-011	58002011-001			
58C	1E-011	58002011-001			
58D	1B-476	58002476-001			
58E	RN3C	43B216592P12			
58K	1B-480	58002480-001			
58L	1B-015	58002015-001			

COMP INSTL LIST - EURCB

TAB-006

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
58N	1Q-483	58002483-001			
58N	1N3481	58002481-001			
58U	1B-094	58002094-001			
58V	1B-473	58002473-001			
58W	1Q-660	58002660-001			
58X	1Q-660	58002660-001			
59J	1B-652	58002652-001			
59P	1C-697	58002697-001			
63G	1D3491	58002491-001			
63H	1D3491	58002491-001			
63S	1D3491	58002491-001			
63T	1S3624	58002624-001			
64AE	P1043	43C212092P1043			
64CE	P1043	43C212092P1043			
64EE	P1043	43C212092P1043			
64F	1B-474	58002474-001			
64GE	P1043	43C212092P1043			
64JE	P1043	43C212092P1043			
64LE	P1043	43C212092P1043			
64NE	P1043	43C212092P1043			
64QE	P1043	43C212092P1043			
64SE	P1043	43C212092P1043			
64UE	P1043	43C212092P1043			
64WE	P1043	43C212092P1043			
66B	1D3491	58002491-001			
66C	1D3491	58002491-001			
66E	1D3491	58002491-001			
66K	1D3492	58002492-001			
66R	1Q-424	58002424-001			
66U	1D3491	58002491-001			
66V	1S3624	58002624-001			
66W	1D3491	58002491-001			
66X	1S3624	58002624-001			
67A	1E-011	58002011-001			
67D	1E-011	58002011-001			
67J	1B-495	58002495-001			
67M	1B-472	58002472-001			
67N	1B-476	58002476-001			

COMP INSTL LIST - EURCB

TAB 006

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
6BP	1B-696	58002696-001			
6BQ	1B-053	58002053-001			
72AE	P9	43A114748P9			
72CE	P9	43A114748P9			
72EE	P9	43A114748P9			
72F	1S3624	58002624-001			
72G	1S3624	58002624-001			
72GE	P9	43A114748P9			
72H	1S3624	58002624-001			
72HE	P9	43A114748P9			
72JE	P9	43A114748P9			
72KE	P9	43A114748P9			
72LE	P9	43A114748P9			
72S	1D3491	58002491-001			
72SE	P9	43A114748P9			
72T	1S3624	58002624-001			
72UE	P9	43A114748P9			
72WE	P9	43A114748P9			
73A	1S3624	58002624-001			
73B	1D3491	58002491-001			
73C	1D3491	58002491-001			
73D	1S3624	58002624-001			
73E	1S3624	58002624-001			
73J	1D3491	58002491-001			
73K	1D3491	58002491-001			
73R	1S3624	58002624-001			
73U	1S3624	58002624-001			
73V	1S3624	58002624-001			
73W	1D3491	58002491-001			
73X	1S3624	58002624-001			
76P	1D3491	58002491-001			
76Q	1B-680	58002680-001			
77L	1B-472	58002472-001			
78M	1T3618-022	58002618-022			
80AE	P1043	43A212092P1043			
80CE	P1043	43A212092P1043			
80EE	P1043	43A212092P1043			
80GE	P1043	43A212092P1043			

TAB-006

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
80JE	P1043	43C212092P1043			
80LE	P1043	43C212092P1043			
80NE	P1043	43C212092P1043			
80QE	P1043	43C212092P1043			
80SE	P1043	43C212092P1043			
80UE	P1043	43C212092P1043			
80WE	P1043	43C212092P1043			
81F	1D3492	58002492-001			
81G	1S3624	58002624-001			
81H	1D3492	58002492-001			
81S	1S3624	58002624-001			
81T	1D3492	58002492-001			
84A	1D3492	58002492-001			
84B	1S3624	58002624-001			
84C	1D3491	58002491-001			
84D	1D3492	58002492-001			
84E	1S3624	58002624-001			
84J	1S3624	58002624-001			
84K	1S3624	58002624-001			
84Q	1S3624	58002624-001			
84R	1D3492	58002492-001			
84U	1S3624	58002624-001			
84V	1D3492	58002492-001			
84W	1S3624	58002624-001			
84X	1D3492	58002492-001			
85L	1Q-480	58002480-001			
85P	1Q-660	58002660-001			
88AE	P1043	43C212092P1043			
88CE	P1043	43C212092P1043			
88EE	P1043	43C212092P1043			
88GE	P1043	43C212092P1043			
88JE	P1043	43C212092P1043			
88LE	P1043	43C212092P1043			
88NE	P1043	43C212092P1043			
88QE	P1043	43C212092P1043			
88SE	P1043	43C212092P1043			
88UE	P1043	43C212092P1043			
88WE	P1043	43C212092P1043			

COMP INSTL LIST - EURCB

TAB-006

LOC	TYPE	IDENT	X-POS	Y-POS	ROTATION
90F	1B3494	58002494-001			
9DG	1B3494	58002494-001			
9DH	1B3494	58002494-001			
90I	1B3494	58002494-001			
90T	1B3494	438216548P1			
93A	401548	58002017-001			
93B	1B-017	438216548P1			
93C	401548	438216548P1			
93D	401548	438216548P1			
93E	401548	58002017-001			
93I	1B-017	438216548P1			
93K	401548	58002476-001			
93L	1B-476	58002017-001			
93M	1B-017	438216593P15			
93N	BL1E	438216548P1			
93P	401548	58002490-001			
93Q	1B-490	438216548P1			
93R	401548	58002480-001			
93U	1B-480	438216548P1			
93V	401548	438216548P1			
93W	401548	438216548P1			
93X	401548				

A. GENERAL APPLICATIONS

1. SCOPE:

THE EURCB HAS A BANK OF CONFIGURATION SWITCHES WHICH MUST BE SET PRIOR TO INSTALLING THE BOARD INTO THE IOM. THE SWITCHES ARE USED TO SET THE BASE CHANNEL NUMBER AND THE NUMBER OF LOGICAL CHANNELS ASSIGNED TO THE EURC. SEE FIGURE 1 FOR LOCATION OF SWITCH-BANK ON THE EURCB.

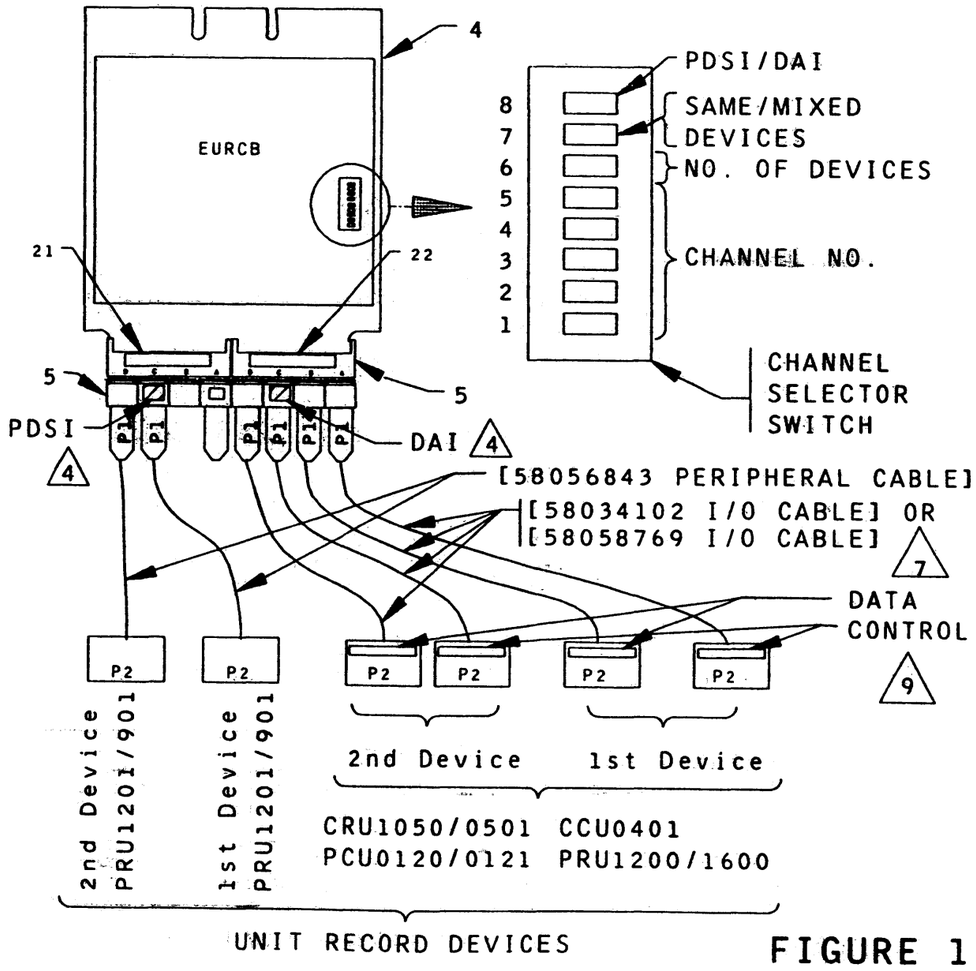
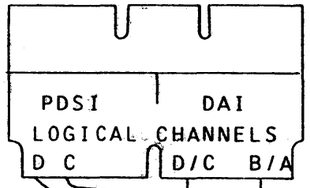


FIGURE 1

FIGURE 2 SHOWS THE LOGICAL CHANNEL ASSIGNMENTS BASED ON THE INTERFACE CONFIGURATIONS AND THE NUMBER OF LOGICAL CHANNELS USED. SWITCH 6 IS OPENED TO CONFIGURE 2 LOGICAL CHANNELS OR CLOSED TO CONFIGURE 4 LOGICAL CHANNELS. SWITCHES 6, 7 AND 8 DETERMINE WHICH INTERFACES ARE ACTIVE AND THEIR RELATIVE PRIORITIES (NOTE 1) (*) THE RECOMMENDED SWITCH SETTING FOR EACH POSSIBLE INTERFACE CONFIGURATION IS THE FIRST SWITCH SETTING LISTED FOR THAT CONFIGURATION IN FIGURE 2.

(*) SEE NEXT SHEET FOR NOTES:



1=OPEN 0=CLOSED

DEVICE CONNECTIONS 3				LOG CHAN REQD	SWITCH SETTING 6	7	8	INTERFACE PORT ASSIGNMENT LOGICAL CHANNEL 2 0	1	2	3
NO	NO	NO	YES	2	1	1	0	DAI B/A			
NO	NO	YES	YES	2	1	1	0	DAI B/A	DAI D/C		
NO	YES	NO	NO	2	1	1	1	PDSI C			
YES	YES	NO	NO	2	1	1	1	PDSI C	PDSI D		
NO	YES	NO	YES	2	1	0	1	PDSI C	DAI B/A		
					1	0	0	DAI B/A	PDSI C		
NO	YES	YES	YES	4	0	0	1	PDSI C		DAI B/A	DAI D/C
					0	0	0	DAI B/A	DAI D/C	PDSI C	
					0	1	0	DAI B/A	PDSI C	DAI D/C	
					0	1	1	PDSI C	DAI B/A		DAI D/C
YES	YES	NO	YES	4	0	0	1	PDSI C	PDSI D	DAI B/A	
					0	0	0	DAI B/A		PDSI C	PDSI D
					0	1	0	DAI B/A	PDSI C		PDSI D
					0	1	1	PDSI C	DAI B/A	PDSI D	
YES	YES	YES	YES	4	0	0	1	PDSI C	PDSI D	DAI B/A	DAI D/C
					0	0	0	DAI B/A	DAI D/C	PDSI C	PDSI D
					0	1	0	DAI B/A	PDSI C	DAI D/C	PDSI D
					0	1	1	PDSI C	DAI B/A	PDSI D	DAI D/C

FIGURE 2

NOTES:

△ 1. THE PRIORITY OF A DEVICE IS RELATED TO THE LOGICAL CHANNEL NUMBER. LOWER LOGICAL CHANNEL HAS PRIORITY OVER A HIGHER LOGICAL CHANNEL.

△ 2. THE SWITCH SETTING DETERMINES THE PHYSICAL PORT FOR EACH LOGICAL CHANNEL.

△ 3. THE SWITCHES SHOULD BE SET TO GIVE PRIORITY TO PRINTER DEVICES OVER CARD DEVICES.

IMPORTANT NOTICE :

PRINTER PRU1201/901 (PR54) MUST BE SET INTERNALLY TO REFLECT THE LOGICAL CHANNEL ("0" OR "1") TO WHICH IT IS CONNECTED. REFER TO PR54 PRODUCT MANUAL 47240005-106, SECTION VIII "ON SITE REPAIR AND ADJUSTMENTS", PAGES 8-196 & 197.

LOCATE DIP SWITCH IN LOWER CENTER OF PDSI BOARD MOUNTED ON LEFT DOOR OF PR54. TO ADJUST TO LOGICAL CHANNEL "0", SET ALL SWITCHES ON DIP TO THE RIGHT "0" POSITION. IF LOGICAL CHANNEL "1" IS TO BE SELECTED, SET THE SECOND SWITCH FROM THE BOTTOM (MARKED "1") TO THE LEFT.

THERE ARE NO INTERNAL ADDRESS SWITCHES ON THE PRU 1200/1600 (PR 71) PRINTER.

DO NOT MIX DEVICE TYPES ON A BOARD. PLACE CARD EQUIPMENT ON ONE BOARD AND PRINTERS ON ANOTHER.

FIGURE 3 SHOWS ALL POSSIBLE SWITCH SETTINGS AVAILABLE FOR THE EURC CONFIGURATIONS. SWITCHES 1 THROUGH 5 SELECT THE BASE CHANNEL NUMBER, SWITCH 6 SELECTS THE NUMBER OF LOGICAL CHANNELS REQUIRED , SWITCH 7 SELECTS IF DEVICES ARE THE SAME TYPE OR NOT AND SWITCH 8 SELECTS WHAT TYPE OF DEVICES IF THEY ARE THE SAME, FOR CHANNEL NUMBERS GREATER THAN 37 OCTAL SWITCH 1 IS CLOSED.

EURCB CHANNEL CONFIGURATION SWITCH SETTINGS

	OCTAL		DECIMAL		CONFIGURATION SWITCTHES *					
	BASE CHAN	LOGICAL CHANNELS	BASE CHAN	LOGICAL CHANNELS	1	2	3	4	5	6
	10		8		1	1	0	1	1	1
	10	10-11-12-13	8	8-9-10-11	1	1	0	1	1	0
	12	12-13	10	10-11	1	1	0	1	0	1
	14	14-15	12	12-13	1	1	0	0	1	1
	14	14-15-16-17	12	12-13-14-15	1	1	0	0	1	0
	16	16-17	14	14-15	1	1	0	0	0	1
	20	20-21	16	16-17	1	0	1	1	1	1
	20	20-21-22-23	16	16-17-18-19	1	0	1	1	1	0
	22	22-23	18	18-19	1	0	1	1	0	1
	24	24-25	20	20-21	1	0	1	0	1	1
	24	24-25-26-27	20	20-21-22-23	1	0	1	0	1	0
	26	26-27	22	22-23	1	0	1	0	0	1
**	30	30-31	24	24-25	1	0	0	1	1	1
**	30	30-31-32-33	24	24-25-26-27	1	0	0	1	1	0
	32	32-33	26	26-27	1	0	0	1	0	1
	34	34-35	28	28-29	1	0	0	0	1	1
	34	34-35-36-37	28	28-29-30-31	1	0	0	0	1	0
	36	36-37	30	30-31	1	0	0	0	0	1

* SWITCHES: 1=OPEN, 0=CLOSED, X=DON'T CARE

** CHANNEL 30_8 IS STANDARD FOR UNIT RECORD SUBSYSTEMS

FIGURE 3

II. INSTALLATION PROCEDURE

1. REFER TO INSTALLATION KITS: (PROM A) 58081720, (PROM B) 58081721, (PROM C) 58081722 AND (PROM D) 58082265 FOR ITEM NUMBERS REFERENCED IN THE FOLLOWING INSTRUCTIONS.

2. REFER TO FIGURES FOR APPROXIMATE LOCATION AND IDENTITY OF ITEMS REFERRED TO WITHIN THE FOLLOWING INSTALLATION INSTRUCTIONS. NUMBERS CONTAINED WITHIN DELTAS REFER TO APPLICABLE INSTRUCTION.

III. TEST PROCEDURE:

1. RUN MONITOR -4 PRG067

2. RUN APPROPRIATE DEVICE TESTS BEFORE CUSTOMER TURNOVER.

IV. OPTION REMOVAL PROCEDURE:

1. THE REMOVAL OF THESE OPTIONS REQUIRES ONLY THE REVERSE PROCEDURE OF THE INSTALLATION.

V. PARTS DISPOSITION:

1. RETURN THE PARTS REMOVED IN THE ABOVE STEPS TO "LCPD" MANUFACTURING.

RETURN TO:

HONEYWELL INFORMATION SYSTEMS
4001 W. INDIAN SCHOOL ROAD
PHOENIX, ARIZONA 85019-3314

C/O MGR LCPD WAREHOUSE
MAIL DROP J-2

1. EXTENDED ADDRESS IOM (4WDC8134)

I. SCOPE

.THIS INSTRUCTION PROVIDES THE NECESSARY INFORMATION FOR THE INSTALLATION OF THE EMBEDDED UNIT RECORD CONTROLLER INTO THE 4WDC8134 EXTENDED ADDRESS IOM, WITH INTERCONNECTION TO THE UNIT RECORD DEVICES.

II. PREPARATION PROCEDURE:

1. REMOVE ALL POWER FROM THE IOM AND UNIT RECORD DEVICES.

2. REMOVE THE TOP HALF OF THE SPLIT PORT PLATE IN THE THIRD POSITION FROM THE TOP OF THE IOM JUNCTION PANEL. SET ASIDE FOR RE-INSTALLATION, SEE FIGURE 5

III. INSTALLATION PROCEDURE:

1. THIS OPTION IS TO BE INSTALLED IN THE IOM CARD MODULE SLOTS AB21/AA38 OR AA21/AA39 ON A PRIORITY BASIS. USUAL PRIORITIES FOR THE OPTIONS ARE AS FOLLOWS;-

A) INTERFACE PRIORITIES;
HIGHEST=MAG TAPE
NEXT---=DISC
NEXT---=EURC
NEXT---=CONSOLE

B) HIGHEST PRIORITIES START IN AB21 AND END IN AB38.

C) THE NEXT HIGHEST CHANNEL PRIORITY STARTS IN CARD SLOT AA21 TO AA39 AND AA18 TO AA00.

4. SEE SECTION A, GENERAL APPLICATIONS FOR FIGURES 1, 2 AND 3.

5. INSTALL THE CIRCUIT BOARD, EURCB, ITEM 4, IN ACCORDANCE TO THE ABOVE LISTED PRIORITIES AND SECTION 2, FIGURE 6.

△ 5.1 TYPICAL EURCB BOARD LOCATION WITH ONE (1) PSIA CHANNEL INSTALLED.

6. INSTALL MARKERS, ITEM 8, 9 AND 23, TO THE MARKER PANEL ADJACENT TO THE EURC BOARD.

7. SECURE LABELS, ITEM 20, AT EACH END OF THE I/O CABLES, SEE FIGURE 1.

8. SECURE PORT HOLE MARKERS, ITEM 16, 17, 18 AND 19, SEE FIGURE 5.

9. INSTALL THE P1 CONNECTOR OF THE PERIPHERAL CABLE IN SLOT "C" OF THE PDSI CONNECTOR, SEE SECTION A, FIGURE 1. ROUTE THE CABLE THROUGH THE THE JUNCTION PANEL SPLIT PORT PLATE, PORT "C" HOLE, SEE FIGURE 5.

10. INSTALL THE P1 CONNECTOR OF THE ADDITIONAL PERIPHERAL CABLE WHEN REQUIRED IN SLOT "D" OF THE PDSI CONNECTOR, SEE SECTION A, FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "D" HOLE, SEE FIGURE 5.

11. INSTALL THE P1 CONNECTORS OF THE I/O CABLES IN SLOT "A" AND "B" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLES THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "A" HOLE, SEE FIGURE 5.

12. INSTALL THE P1 CONNECTORS OF THE ADDITIONAL I/O CABLES IN SLOTS "C" AND "D" OF THE DAI CONNECTOR, SEE SECTION A, FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "B" HOLE, SEE FIGURE 5.

13. SECURE THE PERIPHERAL AND I/O CABLES TO THE BACK SIDE OF THE PORT PLATE WITH CABLE CLAMPS, ITEM 11, AND FASTENING WITH ITEMS 12, 13, 14 AND 15, SEE FIGURE 5.

14. RE-INSTALL THE TOP HALF OF THE SPLIT PORT PLATE, SEE FIGURE 5.

15. ROUTE THE PERIPHERAL AND I/O CABLES DOWN THE CABLE CABINET, SEE FIGURE 5, THROUGH THE OPENING OF THE CABLE CABINET OVER TO THE UNIT RECORD DEVICES. INSTALL P2 CONNECTORS AT THE UNIT RECORD DEVICES ACCORDING TO THE DEVICE INSTALLATION INSTRUCTION.

16. REFER TO FIGURE 1. OF THIS INSTRUCTION AND APPROPRIATE DEVICE INSTALLATION INSTRUCTIONS.

17. ATTACH THE PRODUCT IDENTIFICATION NAMEPLATE, ITEM [7]/6 TO THE UPPER RIGHT CORNER OF THE JUNCTION PANEL ON THE IOM, SEE FIGURE 5,

    HALT ALL ACTIVITY RELATED TO THE INSTALLATION OF THIS OPTION FOR PROCEED AS FOLLOWS:

    IF NO ADDITIONAL OPTIONS ARE TO BE INSTALLED IN THE IOM CABINET AND THE UNIT IS READY FOR OFF LINE OPERATION, CONTINUE ON TO STEP 18 AND TEST PROCEDURE, SEE SECTION A, GENERAL APPLICATIONS.

18. POWER TO THE IOM CABINET AND DEVICES MAY NOW BE TURNED ON.

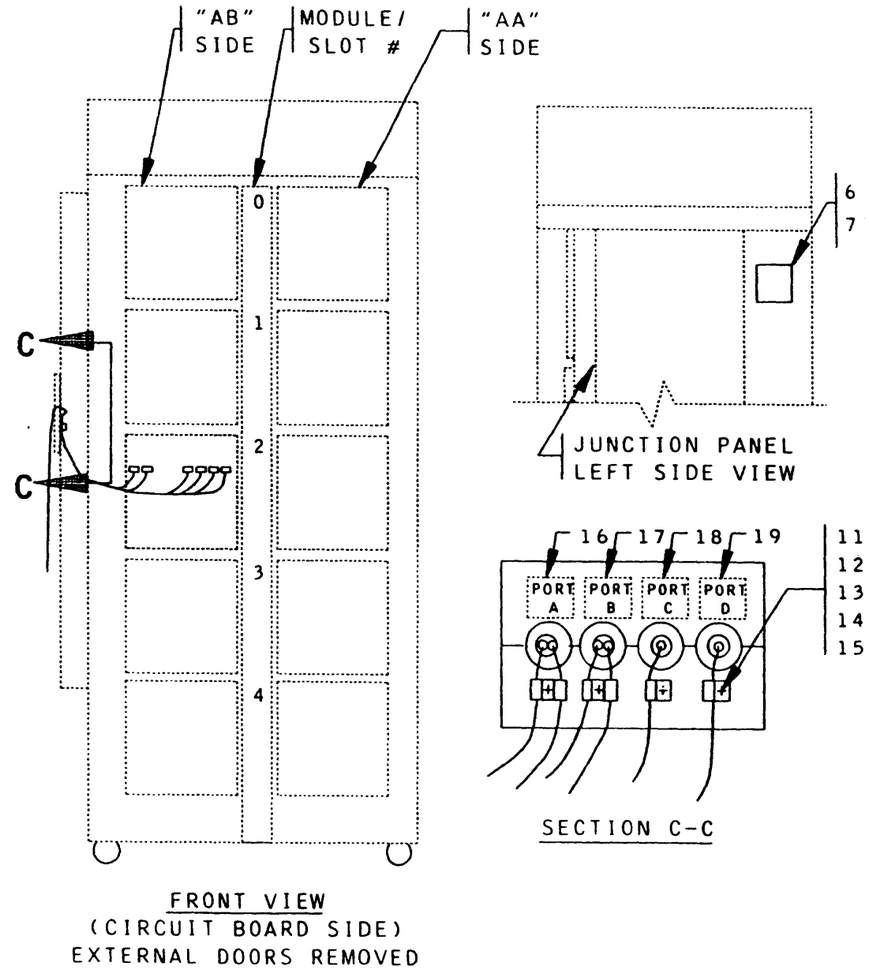


FIGURE 5

2. NSA IOM 4WDC8634

I. SCOPE

THIS INSTRUCTION PROVIDES THE NECESSARY INFORMATION FOR THE INSTALLATION OF THE EMBEDDED UNIT RECORD CONTROLLER INTO THE 4WDC8634 NSA IOM, WITH INTERCONNECTION TO THE UNIT RECORD DEVICES.

II. PREPARATION PROCEDURE:

1. REMOVE ALL POWER FROM THE IOM AND UNIT RECORD DEVICES.

2. REMOVE THE TOP HALF OF THE SPLIT PORT PLATE IN THE THIRD POSITION FROM THE TOP OF THE IOM JUNCTION PANEL. SET ASIDE FOR RE-INSTALLATION, SEE SECTION 1, FIGURE 5.

III. INSTALLATION PROCEDURE:

1. THIS OPTION IS TO BE INSTALLED IN THE IOM CARD MODULE SLOTS AB21/AB38 OR AA21/AA39 ON A PRIORITY BASIS. USUAL PRIORITIES FOR THE OPTIONS. ARE AS FOLLOWS;-

A) INTERFACE PRIORITIES;
HIGHEST=MAG TAPE
NEXT---=DISC
NEXT---=EURC
NEXT---=CONSOLE

B) HIGHEST PRIORITIES START IN AB21 AND END IN AB38.

C) THE NEXT HIGHEST CHANNEL PRIORITIES START IN CARD SLOT AA21 TO AA39 AND AA18 TO AA00.

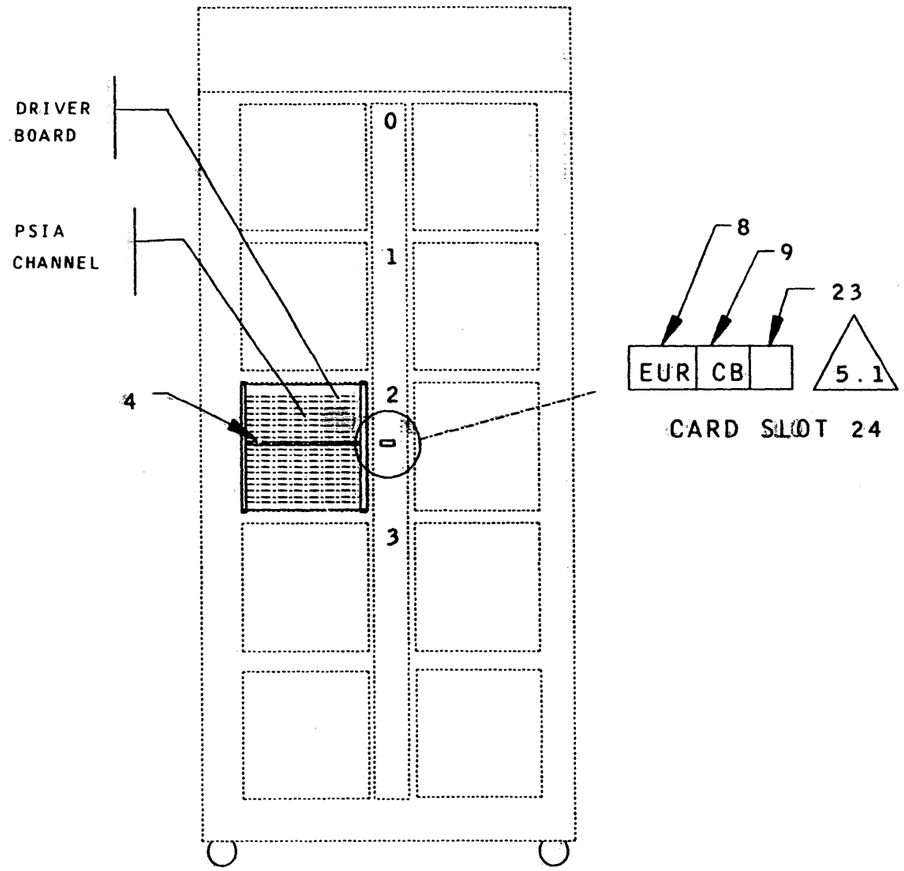
4. SEE SECTION A, GENERAL APPLICATIONS FOR FIGURES 1, 2 AND 3.

5. INSTALL THE CIRCUIT BOARD, EURCB, ITEM 4, IN ACCORDANCE TO THE ABOVE LISTED PRIORITIES AND FIGURE 6.

△ 5.1 TYPICAL EURCB BOARD LOCATION WITH ONE (1) PSIA CHANNEL INSTALLED.

6. INSTALL MARKERS, ITEM 8, 9 AND 23, TO THE MARKER PANEL ADJACENT TO THE EURC BOARD.

7. SECURE LABELS, ITEM 20, AT EACH END OF THE I/O CABLES, SEE FIGURE 1.



FRONT VIEW OF IOM
(CIRCUIT BOARD SIDE)
EXTERNAL DOORS REMOVED

FIGURE 6

8. SECURE PORT HOLE MARKERS, ITEM 16, 17, 18 AND 19, SEE SECTION 1, FIGURE 5.

9. INSTALL THE P1 CONNECTOR OF THE PERIPHERAL CABLE IN SLOT "C" OF THE PDSI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE THE JUNCTION PANEL SPLIT PORT PLATE, PORT "C" HOLE, SEE SECTION 1, FIGURE 5.

10. INSTALL THE P1 CONNECTOR OF THE ADDITIONAL PERIPHERAL CABLE WHEN REQUIRED IN SLOT "D" OF THE PDSI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "D" HOLE, SEE SECTION 1, FIGURE 5.

11. INSTALL THE P1 CONNECTORS OF THE I/O CABLES IN SLOT "A" AND "B" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLES THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "A" HOLE, SEE SECTION 1, FIGURE 5.

12. INSTALL THE P1 CONNECTORS OF THE ADDITIONAL I/O CABLES IN SLOTS "C" AND "D" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "B" HOLE, SEE SECTION 1, FIGURE 5.

13. SECURE THE PERIPHERAL AND I/O CABLES TO THE BACK SIDE OF THE PORT PLATE WITH CABLE CLAMPS, ITEM 11, AND FASTENING WITH ITEMS 12, 13, 14 AND 15, SEE SECTION 1, FIGURE 5.

14. RE-INSTALL THE TOP HALF OF THE SPLIT PORT PLATE, SEE SECTION 1, FIGURE 5.

15. ROUTE THE PERIPHERAL AND I/O CABLES DOWN THE CABLE CABINET, SEE SECTION 1, FIGURE 5, THROUGH THE OPENING OF THE CABLE CABINET OVER TO THE UNIT RECORD DEVICES. INSTALL P2 CONNECTORS AT THE UNIT RECORD DEVICES ACCORDING TO THE DEVICE INSTALLATION INSTRUCTIONS.

16. REFER TO FIGURE 1 OF THIS INSTRUCTION AND APPROPRIATE DEVICE INSTALLATION INSTRUCTIONS.

17. ATTACH THE PRODUCT IDENTIFICATION NAMEPLATE, ITEM [7]/6 TO THE UPPER RIGHT CORNER OF THE JUNCTION PANEL ON THE IOM, SEE SECTION 1, FIGURE 5,

    HALT ALL ACTIVITY RELATED TO THE INSTALLATION OF THIS OPTION FOR PROCEED AS FOLLOWS:

    IF NO ADDITIONAL OPTIONS ARE TO BE INSTALLED IN THE IOM CABINET AND THE UNIT IS READY FOR OFF LINE OPERATION, CONTINUE ON TO STEP 18 AND TEST PROCEDURE, SEE SECTION A, GENERAL APPLICATIONS.

18. POWER TO THE IOM CABINET AND DEVICES MAY NOW BE TURNED ON.

3. INTEGRATED CONTROL UNIT, 4WCSM001AA3

I. SCOPE

THIS INSTRUCTION PROVIDES THE NECESSARY INFORMATION FOR THE INSTALLATION OF THE EMBEDDED UNIT RECORD CONTROLLER INTO THE 4WCSM001 INTEGRATED CONTROL UNIT, WITH INTERCONNECTION TO THE UNIT RECORD DEVICES.

II. PREPARATION PROCEDURE:

1. REMOVE ALL POWER FROM THE ICU AND UNIT RECORD DEVICES.

2. REMOVE THE TOP HALF OF THE SPLIT PORT PLATE IN THE SECOND POSITION FROM THE TOP OF THE ICU JUNCTION PANEL. SET ASIDE FOR RE-INSTALLATION, SEE SECTION 1, FIGURE 5.

III. INSTALLATION PROCEDURE:

1. THIS OPTION IS TO BE INSTALLED IN THE ICU CARD MODULE SLOTS AB21/AB38 OR AB41/AB49 ON A PRIORITY BASIS. USUAL PRIORITIES FOR THE OPTIONS ARE AS FOLLOWS;-

   A) INTERFACE PRIORITIES;
      HIGHEST=MAG TAPE
      NEXT---=DISC
      NEXT---=EURC
      NEXT---=CONSOLE

   B) HIGHEST PRIORITIES START IN AB21 AND END IN AB38.

   C) THE NEXT HIGHEST CHANNEL PRIORITIES START IN CARD SLOT AB41 TO AB49.

4. SEE SECTION A, GENERAL APPLICATIONS FOR FIGURES 1, 2 AND 3.

5. INSTALL THE CIRCUIT BOARD, EURCB, ITEM 4, IN ACCORDANCE TO THE ABOVE LISTED PRIORITIES AND FIGURE 6.

△ 5.1 TYPICAL EURCB BOARD LOCATION WITH ONE (1) PSIA CHANNEL INSTALLED.

6. INSTALL MARKERS, ITEM 8, 9 AND 23, TO THE MARKER PANEL ADJACENT TO THE EURC BOARD.

7. SECURE LABELS, ITEM 20, AT EACH END OF THE I/O CABLES, SEE FIGURE 1.

8. SECURE PORT HOLE MARKERS, ITEM 16, 17, 18 AND 19, SEE SECTION 1, FIGURE 5.

9. INSTALL THE P1 CONNECTOR OF THE PERIPHERAL CABLE IN SLOT "C" OF THE PDSI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE THE JUNCTION PANEL SPLIT PORT PLATE, PORT "C" HOLE, SEE SECTION 1, FIGURE 5.

10. INSTALL THE P1 CONNECTOR OF THE ADDITIONAL PERIPHERAL CABLE WHEN REQUIRED IN SLOT "D" OF THE PDSI CONNECTOR, SEE SECTION A, FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "D" HOLE, SEE SECTION 1, FIGURE 5.

11. INSTALL THE P1 CONNECTORS OF THE I/O CABLES IN SLOT "A" AND "B" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLES THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "A" HOLE, SEE SECTION 1, FIGURE 5.

12. INSTALL THE P1 CONNECTORS OF THE ADDITIONAL I/O CABLES IN SLOTS "C" AND "D" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "B" HOLE, SEE SECTION 1, FIGURE 5.

13. SECURE THE PERIPHERAL AND I/O CABLES TO THE BACK SIDE OF THE PORT PLATE WITH CABLE CLAMPS, ITEM 11, AND FASTENING WITH ITEMS 12, 13, 14 AND 15, SEE SECTION 1, FIGURE 5.

14. RE-INSTALL THE TOP HALF OF THE SPLIT PORT PLATE, SEE SECTION 1, FIGURE 5.

15. ROUTE THE PERIPHERAL AND I/O CABLES DOWN THE CABLE CABINET, SEE SECTION 1, FIGURE 5, THROUGH THE OPENING OF THE CABLE CABINET OVER TO THE UNIT RECORD DEVICES. INSTALL P2 CONNECTORS AT THE UNIT RECORD DEVICES ACCORDING TO THE DEVICE INSTALLATION INSTRUCTIONS.

16. REFER TO FIGURE 1 OF THIS INSTRUCTION AND APPROPRIATE DEVICE INSTALLATION INSTRUCTIONS.

17. ATTACH THE PRODUCT IDENTIFICATION NAMEPLATE, ITEM [7]/6 TO THE UPPER RIGHT CORNER OF THE JUNCTION PANEL ON THE IOM, SEE SECTION 1, FIGURE 5, HALT ALL ACTIVITY RELATED TO THE INSTALLATION OF THIS OPTION AND PROCEED AS FOLLOWS:

    IF NO ADDITIONAL OPTIONS ARE TO BE INSTALLED IN THE IOM CABINET AND THE UNIT IS READY FOR OFF LINE OPERATION, CONTINUE ON TO STEP 18 AND TEST PROCEDURE, SECTION A, GENERAL APPLICATIONS.

18. POWER TO THE IOM CABINET AND DEVICES MAY NOW BE TURNED ON.

4. INTEGRATED CONTROL UNIT, 4WCSM601

I. SCOPE

THIS INSTRUCTION PROVIDES THE NECESSARY INFORMATION FOR THE INSTALLATION OF THE EMBEDDED UNIT RECORD CONTROLLER INTO THE 4WCSM601 INTEGRATED CONTROL UNIT INTERCONNECTION TO THE UNIT RECORD DEVICES.

II. PREPARATION PROCEDURE:

1. REMOVE ALL POWER FROM THE ICU AND UNIT RECORD DEVICES.

2. REMOVE THE TOP HALF OF THE SPLIT PORT PLATE IN THE SECOND POSITION FROM THE TOP OF THE ICU JUNCTION PANEL, SET ASIDE FOR RE-INSTALLATION, SEE SECTION 1, FIGURE 5.

III. INSTALLATION PROCEDURE:

1. THIS OPTION IS TO BE INSTALLED IN THE IOM CARD MODULE SLOTS AB21/AB38 OR AB41/AB49 ON A PRIORITY BASIS. USUAL PRIORITIES FOR THE OPTIONS ARE AS FOLLOWS;-

    A) INTERFACE PRIORITIES;
    HIGHEST=MAG TAPE
    NEXT---=DISC
    NEXT---=EURC
    NEXT---=CONSOLE

    B) HIGHEST PRIORITIES START IN AB21 AND END IN AB38.

    C) THE NEXT HIGHEST CHANNEL PRIORITIES START IN CARD SLOT AB41 TO AB49.

4. SEE GENERAL APPLICATIONS FOR FIGURES 1, 2 AND 3.

5. INSTALL THE CIRCUIT BOARD, EURCB, ITEM 4, IN ACCORDANCE TO THE ABOVE LISTED PRIORITIES AND FIGURE 6.

△ 5.1 TYPICAL EURCB BOARD LOCATION WITH ONE (1) PSIA CHANNEL INSTALLED.

6. INSTALL MARKERS, ITEM 8, 9 AND 23, TO THE MARKER PANEL ADJACENT TO THE EURC BOARD.

7. SECURE LABELS, ITEM 20, AT EACH END OF THE I/O CABLES, SEE FIGURE 1.

8. SECURE PORT HOLE MARKERS, ITEM 16, 17, 18 AND 19, SEE SECTION 1, FIGURE 5.

9. INSTALL THE P1 CONNECTOR OF THE PERIPHERAL CABLE IN SLOT "C" OF THE PDSI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE THE JUNCTION PANEL SPLIT PORT PLATE, PORT "C" HOLE, SEE SECTION 1, FIGURE 5.

10. INSTALL THE P1 CONNECTOR OF THE ADDITIONAL PERIPHERAL CABLE WHEN REQUIRED IN SLOT "D" OF THE PDSI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "D" HOLE, SEE SECTION 1, FIGURE 5.

11. INSTALL THE P1 CONNECTORS OF THE I/O CABLES IN SLOT "A" AND "B" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLES THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "A" HOLE, SEE SECTION 1, FIGURE 5.

12. INSTALL THE P1 CONNECTORS OF THE ADDITIONAL I/O CABLES IN SLOTS "C" AND "D" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "B" HOLE, SEE SECTION 1, FIGURE 5.

13. SECURE THE PERIPHERAL AND I/O CABLES TO THE BACK SIDE OF THE PORT PLATE WITH CABLE CLAMPS, ITEM 11, AND FASTENING WITH ITEMS 12, 13, 14 AND 15, SEE SECTION 1, FIGURE 5.

14. RE-INSTALL THE TOP HALF OF THE SPLIT PORT PLATE, SEE SECTION 1, FIGURE 5.

15. ROUTE THE PERIPHERAL AND I/O CABLES DOWN THE CABLE CABINET, SEE SECTION 1, FIGURE 5, THROUGH THE OPENING OF THE CABLE CABINET OVER TO THE UNIT RECORD DEVICES. INSTALL P2 CONNECTORS AT THE UNIT RECORD DEVICES ACCORDING TO THE DEVICE INSTALLATION INSTRUCTIONS.

16. REFER TO FIGURE 1 OF THIS INSTRUCTION AND APPROPRIATE DEVICE INSTALLATION INSTRUCTIONS.

17. ATTACH THE PRODUCT IDENTIFICATION NAMEPLATE, ITEM [7]/6 TO THE UPPER RIGHT CORNER OF THE JUNCTION PANEL ON THE IOM, SEE SECTION 1. FIGURE 5,

    HALT ALL ACTIVITY RELATED TO THE INSTALLATION OF THIS OPTION AND PROCEED AS FOLLOWS:

    IF NO ADDITIONAL OPTIONS ARE TO BE INSTALLED IN THE IOM CABINET AND THE UNIT IS READY FOR OFF LINE OPERATION, CONTINUE ON TO STEP 18 AND TEST PROCEDURE, SECTION A, GENERAL APPLICATION.

18. POWER TO THE IOM CABINET AND DEVICES MAY NOW BE TURNED ON.

5. ELS I/O UNIT, WIOM001A

I. SCOPE

THIS INSTRUCTION PROVIDES THE NECESSARY INFORMATION FOR THE INSTALLATION OF THE EMBEDDED UNIT RECORD CONTROLLER INTO THE 4WIOM001A ELS I/O UNIT, WITH INTERCONNECTION TO THE UNIT RECORD DEVICES.

II. PREPARATION PROCEDURE:

1. REMOVE ALL POWER FROM THE ELS IOM AND UNIT RECORD DEVICES.

2. REMOVE THE TOP HALF OF THE SPLIT PORT PLATE IN LOCATION "W03" AND "W04" SET ASIDE FOR RE-INSTALLATION, SEE FIGURE 7.

III. INSTALLATION PROCEDURE:

1. THIS OPTION IS TO BE INSTALLED IN THE IOM CARD MODULE "B3" AND "B4" ON A PRIORITY BASIS. USUAL PRIORITIES FOR THE OPTIONS ARE AS FOLLOWS;-

   A) INTERFACE PRIORITIES;
      HIGHEST=MAG TAPE
      NEXT---=DISC
      NEXT---=EURC
      NEXT---=CONSOLE

   B) HIGHEST PRIORITIES START IN CARD SLOT "B4B" AND END IN "B4U".

   C) THE NEXT HIGHEST CHANNEL PRIORITIES START IN CARD "B3S" AND END IN SLOT "B3U".

4. SEE GENERAL APPLICATIONS FOR FIGURE 1, 2 AND 3.

5. INSTALL THE CIRCUIT BOARD, EURCB, ITEM 4, IN ACCORDANCE TO THE ABOVE LISTED PRIORITIES AND FIGURE 8.

△ 5.1 TYPICAL EURCB BOARD LOCATION WITH ONE (1) PSIA CHANNEL INSTALLED.

6. INSTALL MARKERS, ITEM 8, 9 AND 23, TO THE MARKER PANEL ADJACENT TO THE EURC BOARD.

7. SECURE LABELS, ITEM 20, AT EACH END OF THE I/O CABLES, SEE FIGURE 1.

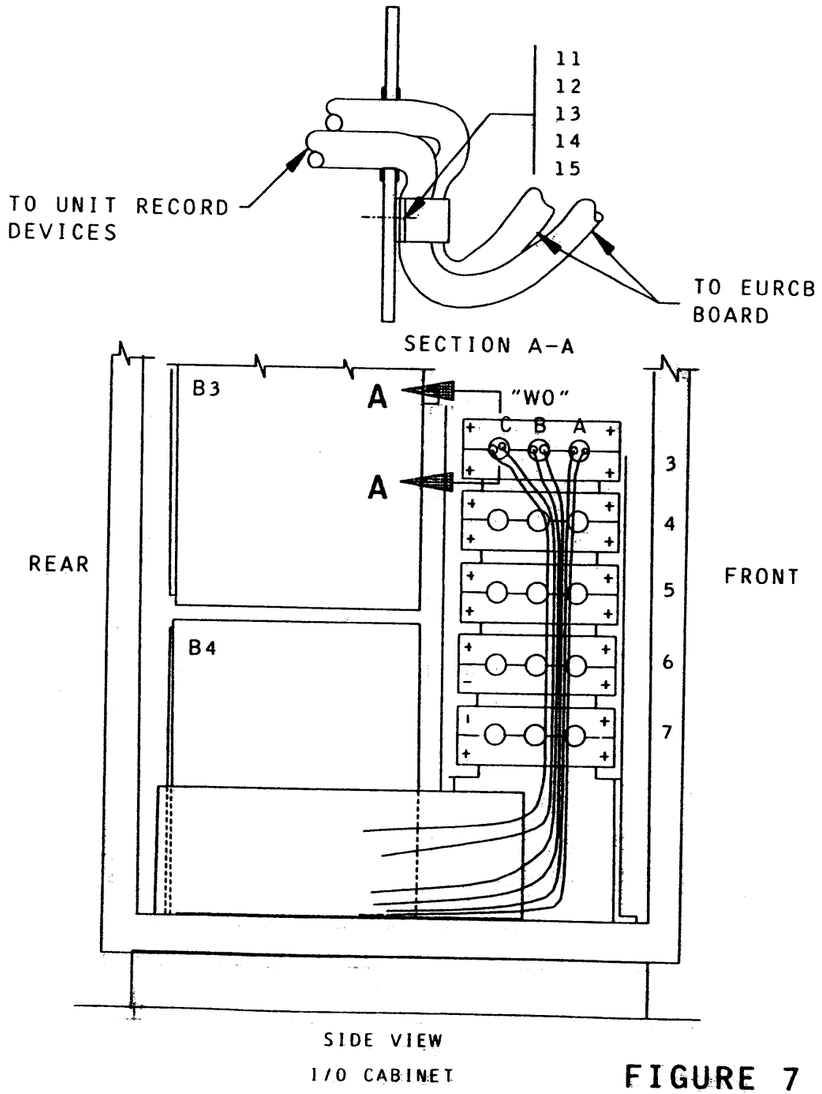


FIGURE 7

8. INSTALL THE P1 CONNECTOR OF THE PERIPHERAL CABLE IN SLOT "C" OF THE PDSI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE THE JUNCTION PANEL SPLIT PORT PLATE, PORT "C" HOLE, SEE FIGURE 7.

9. INSTALL THE P1 CONNECTOR OF THE ADDITIONAL PERIPHERAL CABLE WHEN REQUIRED IN SLOT "D" OF THE PDSI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "C" HOLE, SEE FIGURE 7.

10. INSTALL THE P1 CONNECTORS OF THE I/O CABLES IN SLOT "A" AND "B" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLES THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "A" HOLE, SEE FIGURE 7.

11. INSTALL THE P1 CONNECTORS OF THE ADDITIONAL I/O CABLES IN SLOTS "C" AND "D" OF THE DAI CONNECTOR, SEE FIGURE 1. ROUTE THE CABLE THROUGH THE JUNCTION PANEL SPLIT PORT PLATE PORT "B" HOLE, SEE FIGURE 7.

12. SECURE THE PERIPHERAL AND I/O CABLES TO THE BACK SIDE OF THE PORT PLATE WITH CABLE CLAMPS, ITEM 11, AND FASTENING WITH ITEMS 12, 13, 14 AND 15, SEE FIGURE 7.

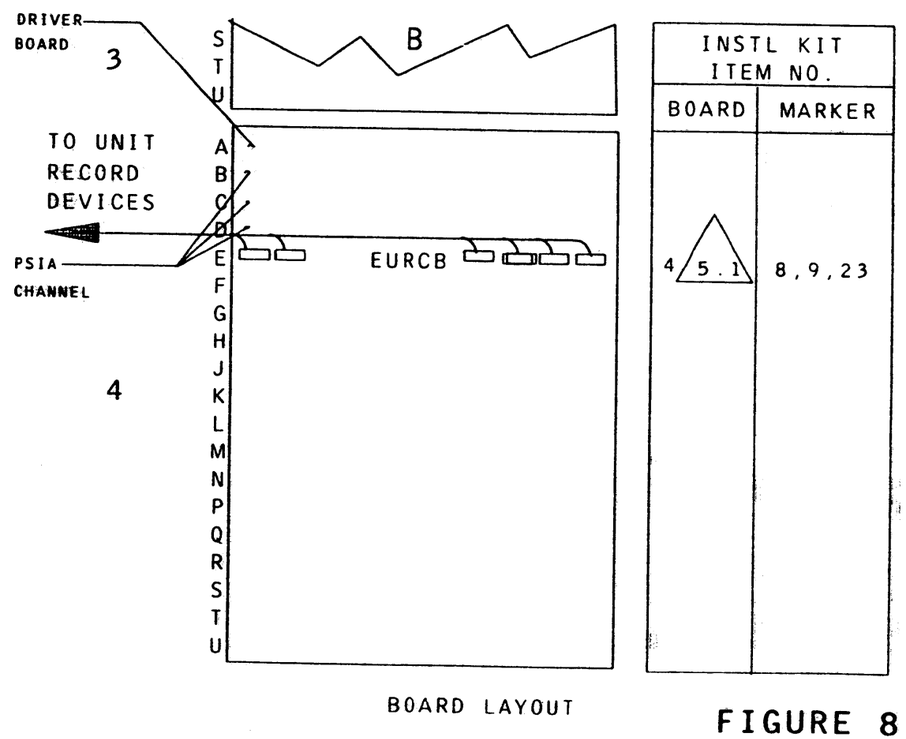


FIGURE 8

13. RE-INSTALL THE TOP HALF OF THE SPLIT PORT PLATE, SEE FIGURE 7.

14. ROUTE THE PERIPHERAL AND I/O CABLES DOWN THE CABLE CABINET, SEE SECTION 1, FIGURE 5, THROUGH THE OPENING OF THE CABLE CABINET OVER TO THE UNIT RECORD DEVICES. INSTALL P2 CONNECTORS AT THE UNIT RECORD DEVICES ACCORDING TO THE DEVICE INSTALLATION INSTRUCTIONS,

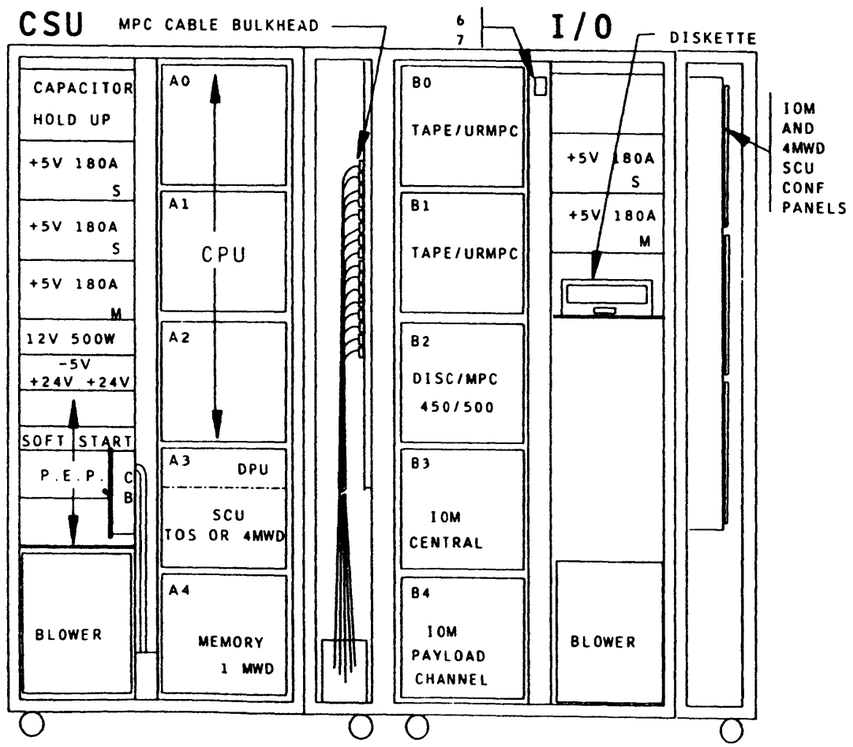
15. REFER TO FIGURE 1 OF THIS INSTRUCTION AND APPROPRIATE DEVICE INSTALLATION INSTRUCTIONS.

16. ATTACH THE PRODUCT IDENTIFICATION NAMEPLATE, ITEM [7]/6 TO THE FRONT FACE OF THE AIR PLENUM, SEE FIGURE 9.

HALT ALL ACTIVITY RELATED TO THE INSTALLATION OF THIS OPTION AND PROCEED AS FOLLOWS:

IF NO ADDITIONAL OPTIONS ARE TO BE INSTALLED IN THE IOM CABINET AND THE UNIT IS READY FOR OFF LINE OPERATION, CONTINUE ON TO STEP 17 AND TEST PROCEDURE, SEE GENERAL APPLICATIONS.

17. POWER TO THE IOM CABINET AND DEVICES MAY NOW BE TURNED ON.



ELS-1 FRONT VIEW

FIGURE 9

6. ELS I/O UNIT, WIOM001B

I. SCOPE

THIS INSTRUCTION PROVIDES THE NECESSARY INFORMATION FOR THE INSTALLATION OF THE EMBEDDED UNIT RECORD CONTROLLER INTO THE 4WIOM001B ELS I/O UNIT, WITH INTERCONNECTION TO THE UNIT RECORD DEVICES.

II. PREPARATION PROCEDURE:

1. REMOVE ALL POWER FROM THE ELS IOM AND UNIT RECORD DEVICES.

III. INSTALLATION PROCEDURE:

1. THIS OPTION IS TO BE INSTALLED IN THE IOM CARD MODULE "A3" AND "A4" ON A PRIORITY BASIS. USUAL PRIORITIES FOR THE OPTIONS ARE AS FOLLOWS;-

A) INTERFACE PRIORITIES;
HIGHEST=MAG TAPE
NEXT---=DISC
NEXT---=EURC
NEXT---=CONSOLE

B) HIGHEST PRIORITIES START IN CARD SLOT "A4B" AND END IN "A4U".

C) THE NEXT HIGHEST CHANNEL PRIORITIES START IN CARD "A3S" AND END IN SLOT "A3U".

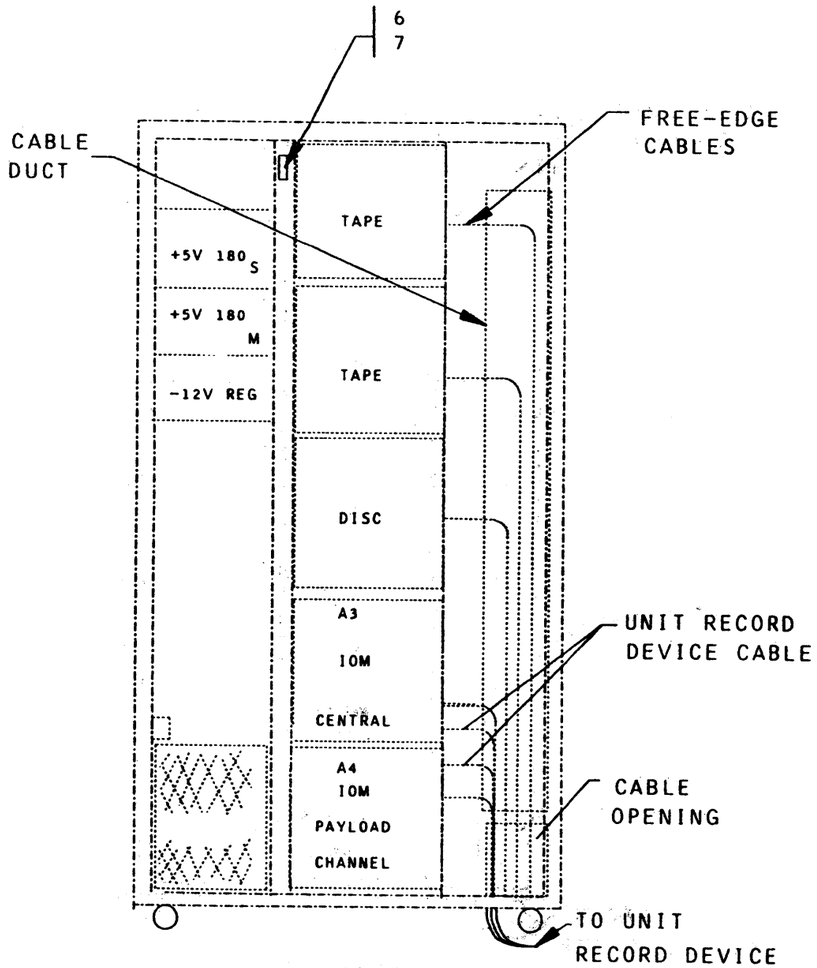
4. SEE GENERAL APPLICATIONS FOR FIGURE 1, 2 AND 3.

5. INSTALL THE CIRCUIT BOARD, EURCB, ITEM 4, IN ACCORDANCE TO THE ABOVE LISTED PRIORITIES AND FIGURE 9B.

△ 5.1 TYPICAL EURCB BOARD LOCATION WITH ONE (1) PSIA CHANNEL INSTALLED.

6. INSTALL MARKERS, ITEM 8, 9 AND 23, TO THE MARKER PANEL ADJACENT TO THE EURC BOARD.

7. SECURE LABELS, ITEM 20, AT EACH END OF THE I/O CABLES, SEE FIGURE 1.



I/O CABINET
FRONT VIEW
FIGURE 9A

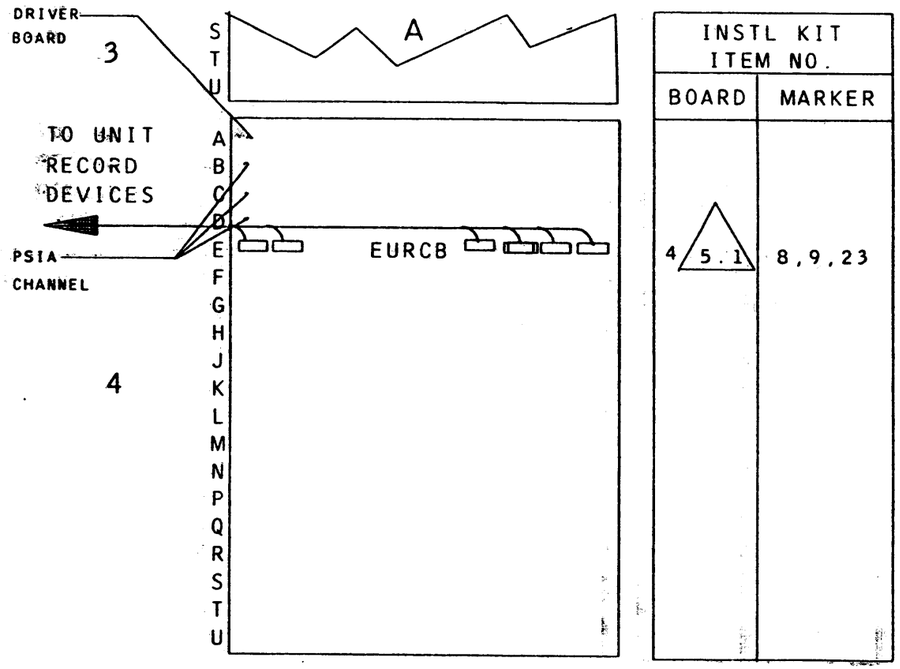
8. INSTALL THE P1 CONNECTOR OF THE PERIPHERAL CABLE IN SLOT "C" OF THE PDIS CONNECTOR, SEE FIGURE 1.

9. INSTALL THE P1 CONNECTOR OF THE ADDITIONAL PERIPHERAL CABLE WHEN REQUIRED IN SLOT "D" OF THE PDSI CONNECTOR, SEE FIGURE 1.

10. INSTALL THE P1 CONNECTORS OF THE I/O CABLES IN SLOT "A" AND "B" OF THE DAI CONNECTOR, SEE FIGURE 1.

11. INSTALL THE P1 CONNECTORS OF THE ADDITIONAL I/O CABLES IN SLOTS "C" AND "D" OF THE DAI CONNECTOR, SEE FIGURE 1.

12. ROUTE THE PERIPHERAL AND I/O CABLES HORIZONTALLY TO THE CABLE DUCT AND THEN DOWN AND OUT THROUGH THE CABLE OPENING IN THE FLOOR PLATE OF THE CABINET, AND OVER TO THE UNIT RECORD DEVICES. SEE FIGURE 9A.



BOARD LAYOUT

FIGURE 9B

13. REFER TO FIGURE 1 OF THIS INSTRUCTION AND APPROPRIATE DEVICE INSTALLATION INSTRUCTIONS.

14. ATTACH THE PRODUCT IDENTIFICATION NAMEPLATE, ITEM [7]/6 TO THE FRONT FACE OF THE AIR PLENUM, SEE FIGURE 9A.

    HALT ALL ACTIVITY RELATED TO THE INSTALLATION OF THIS OPTION AND PROCEED AS FOLLOWS:

    IF NO ADDITIONAL OPTIONS ARE TO BE INSTALLED IN THE IOM CABINET AND THE UNIT IS READY FOR OFF LINE OPERATION, CONTINUE ON TO STEP 15 AND TEST PROCEDURE, SEE GENERAL APPLICATIONS.

15. POWER TO THE IOM CABINET AND DEVICES MAY NOW BE TURNED ON.

7. INPUT/OUTPUT MULTIPLEXER,WIOU66LA

I. SCOPE

THIS INSTRUCTION PROVIDES THE NECESSARY INFORMATION FOR THE INSTALLATION OF THE EMBEDDED UNIT RECORD CONTROLLER INTO THE 4WIOU66LA INPUT/OUTPUT MULTIPLEXER, WITH INTERCONNECTION TO THE UNIT RECORD DEVICES.

II. PREPARATION PROCEDURE:

1. REMOVE ALL POWER FROM THE ELS IOM AND RECORD UNIT DEVICES.

III. INSTALLATION PROCEDURE:

1. THIS OPTION IS TO BE INSTALLED IN THE IOM CARD MODULE "A1", "A2" AND/OR "A3" ON A PRIORITY BASIS. USUAL PRIORITIES FOR THE OPTIONS ARE AS FOLLOWS;-

   A) INTERFACE PRIORITIES:
   HIGHEST=MAG TAPE
   NEXT---=DISC
   NEXT---=EURC
   NEXT---=CONSOLE

   B) PRIORITIES BETWEEN CARD MODULES START WITH "A1" (HIGHEST) AND END WITH "A3" (LOWEST).

   C) PRIORITIES WITHIN CARD MODULES START WITH SLOT "B" (HIGHEST) AND END WITH "U" (LOWEST).

4. SEE SECTION A, GENERAL APPLICATIONS.

5. INSTALL THE CIRCUIT BOARD, EURCB, ITEM 4, IN ACCORDANCE TO THE ABOVE LISTED PRIORITIES AND FIGURE 10.

△ 5.1 TYPICAL EURCB BOARD LOCATION WITH ONE (1) PSIA CHANNEL INSTALLED.

6. INSTALL MARKERS, ITEM 8, 9 AND 23, TO THE MARKER PANEL ADJACENT TO THE EURC BOARD, SEE FIGURE 10.

7. SECURE LABELS, ITEM 20, AT EACH END OF THE I/O CABLES, SEE FIGURE 1.

8. INSTALL THE P1 CONNECTOR OF THE PERIPHERAL CABLE IN SLOT "C" OF THE PDSI CONNECTOR, SEE FIGURE 1.

9. INSTALL THE P1 CONNECTOR OF THE ADDITIONAL PERIPHERAL CABLE IN SLOT "D" OF THE PDSI CONNECTOR, SEE FIGURE 1.

10. INSTALL THE P1 CONNECTORS OF THE I/O CABLES IN SLOT "A" AND "B" OF THE DAI CONNECTOR, SEE FIGURE 1.

11. INSTALL THE P1 CONNECTORS OF THE ADDITIONAL I/O CABLES IN SLOTS "C" AND "D" OF THE DAI CONNECTOR, SEE FIGURE 1.

12. ROUTE THE PERIPHERIAL AND I/O CABLES HORIZONALLY TO THE CABLE DUCT AND THEN VERTICALLY DOWN AND OUT THROUGH THE CABLE OPENING IN THE BOTTOM OF THE IOM CABINET, SEE FIGURE 11, AND OVER TO THE UNIT RECORD DEVICES.

13. INSTALL P2 CONNECTORS AT THE UNIT RECORD DEVICES ACCORDING TO THE DEVICE INSTALLATION INSTRUCTIONS.

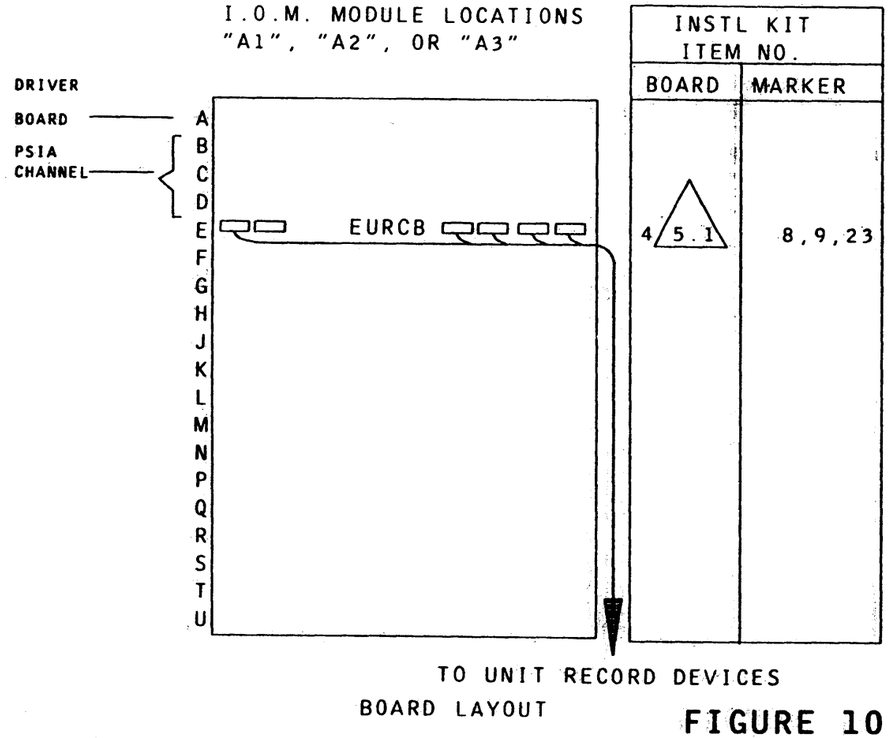


FIGURE 10

14. REFER TO FIGURE 1 OF THIS INSTRUCTION AND APPROPRIATE DEVICE INSTALLATION INSTRUCTIONS.

15. ATTACH THE PRODUCT IDENTIFICATION NAMEPLATE, ITEM [18]/19 TO THE FRONT FACE OF THE AIR PLENUM, SEE FIGURE 11.

. HALT ALL ACTIVITY RELATED TO THE INSTALLATION OF THIS OPTION AND PROCEED AS FOLLOWS:

IF NO ADDITIONAL OPTIONS ARE TO BE INSTALLED IN THE IOM CABINET AND THE UNIT IS READY FOR OFF LINE OPERATION, CONTINUE ON TO STEP 16 AND TEST PROCEDURE, SEE GENERAL APPLICATIONS.

16. POWER TO THE IOM CABINET AND DEVICES MAY NOW BE TURNED ON.

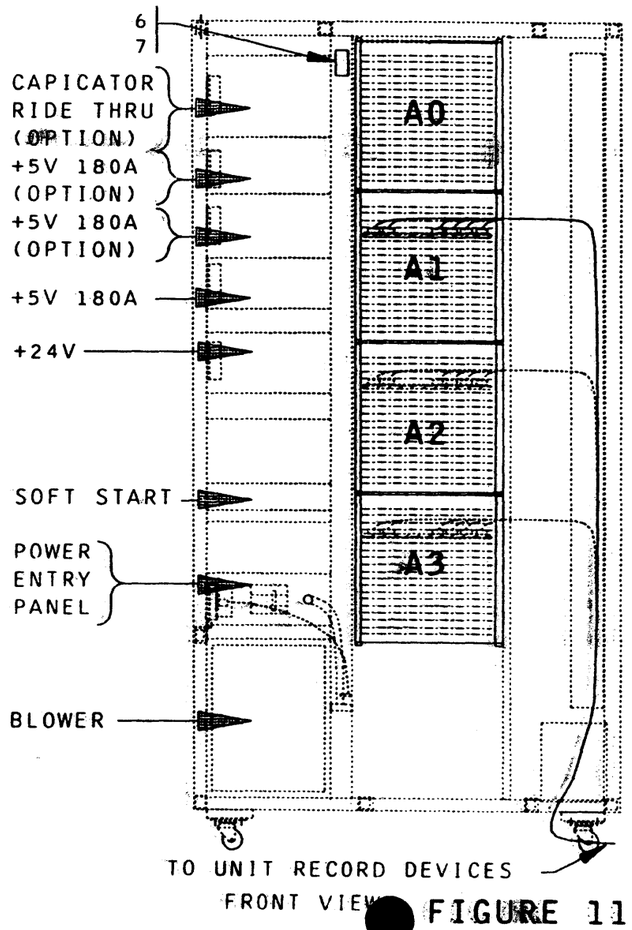


FIGURE 11

58056843

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	ASSEMBLY TAB 001	014	022	024	PL ALL	1	2	3	4	5	6
A	LEVEL 1 ISSUE	81	APR	03	T. Daly 3/18/81	A				A	A					
B	PHAØXS025	81	NOV	02	F. Van Ryper	B				B	B					
C	PHAØXW114	82	APR	02	Steve Steele	C	C	C		C	C					
D	PHAØGD535	83	DEC	23	S. Miller	D	D	D	D	D	D	D	D	D	D	D

FCF :

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY S.J. Steele 80-AUG-28

APPROVED R Albertson 3/16/81

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE PERIPHERAL CABLE ASSEMBLY

SIZE	REVISION STATUS FOR	SHEET	REV
A	58056843	1/1	D

DIST. C 106-73

BRUNING 44-141 40366

CE 300 A-3 (1-79)

					001	014	022	024	
*	1	C	58034066-001	V PADDLE BD COVER	1	1	1	1	EA
*	2	A	58000038-008	V CONNECTOR, PWB	1	1	1	1	EA
*	3	C	58058447-001	A PWB ETCH	1	1	1	1	EA
*	4	B	43B111147P19	V CABLE	787	551	866	945	IN
*	5	B	43B138943P84	V HARDWARE,D SERIES	1	1	1	1	EA
	6	B	438223079P106	V SOCKET		1			EA
*	7	B	438223079P7	V CONN SUB-MIN CR	1	1	1	1	EA
*	8	B	438223079P101	V PIN	10	10	10	10	EA
*	9	B	8788222P120	V SLEEVING	9	9	9	9	IN
*	10	B	8788222P060	V SLEEVING THERMO	4	4	4	4	IN
*	11	A	43A167218P069	V WIRE	5	5	5	5	IN
*	12	A	76951715-045	V LOCKWASHER	1	1	1	1	EA
*	13	A	76951715-059	V LOCKWASHER	2	2	2	2	EA
*	14	A	58053717	V IPL EXTRNL CBL ASM		X		X	EA

PERIPHERAL CABLE ASM

A 58056843 1/1 D

REF SPEC NO
58053700
58053717

REVISION			
REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

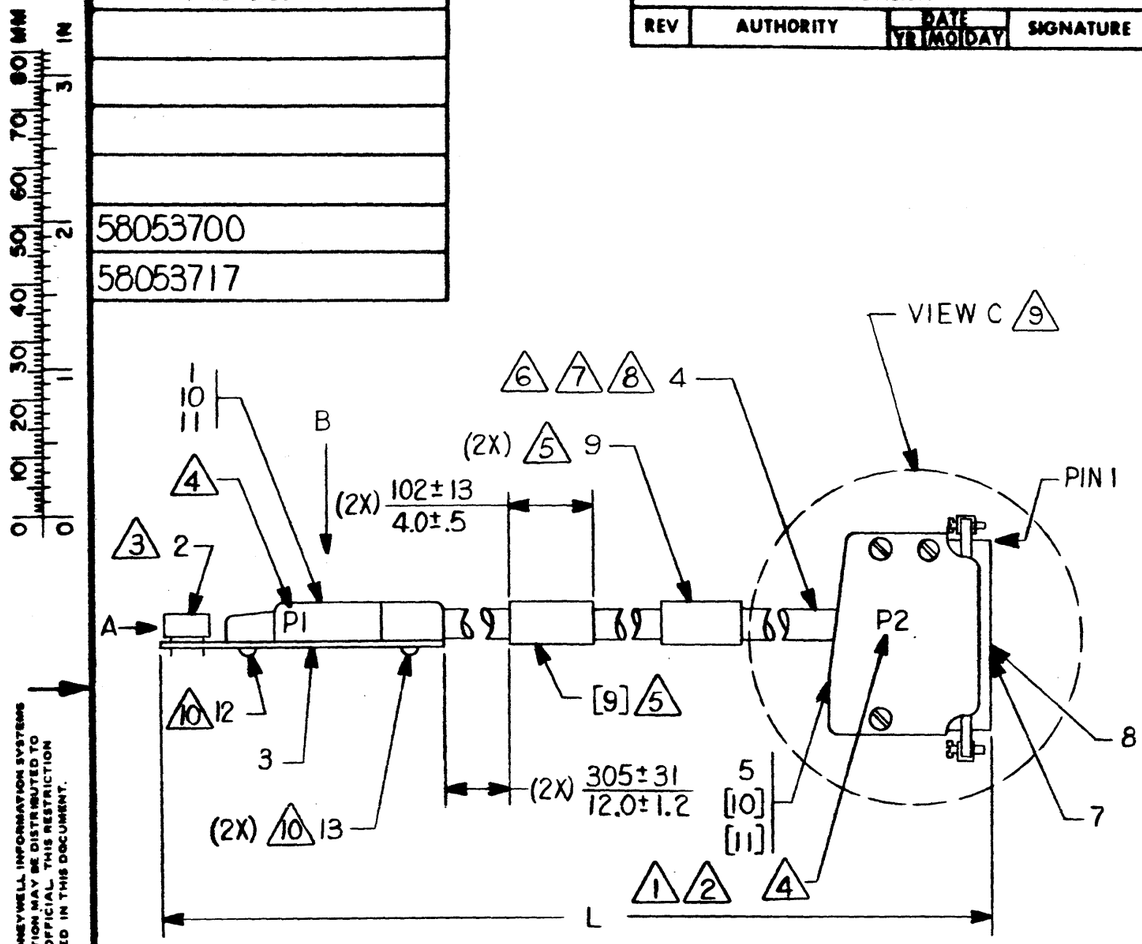
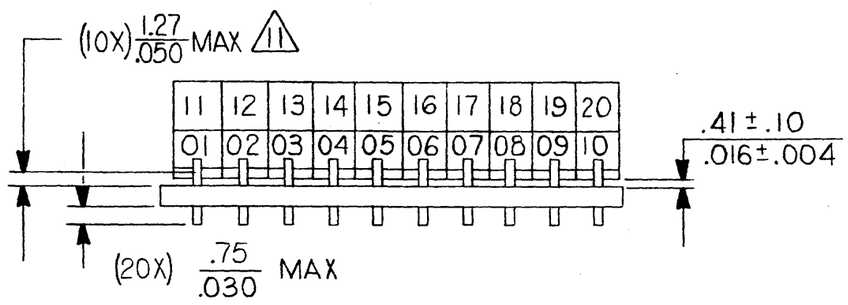


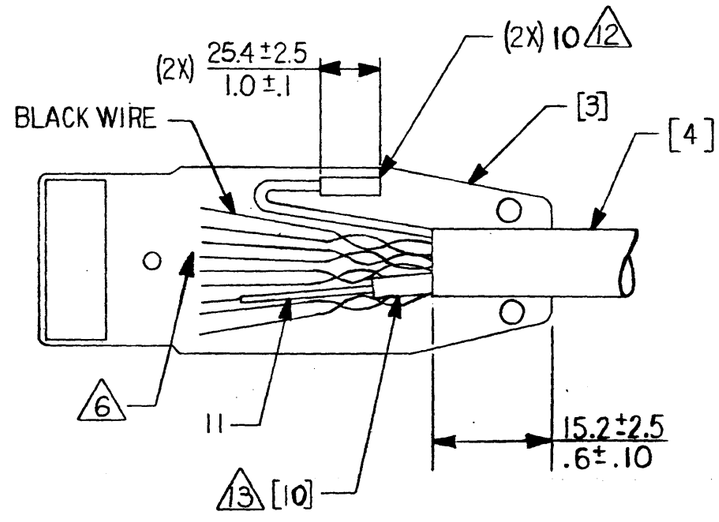
FIGURE 1. EXTERNAL CABLE ASSEMBLY

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES; TOLERANCE OF SIZE AND FORM PER ____; INITIAL DESIGN; PROJECTION	MATL	Honeywell HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U. S. A.
	TREAT.	TITLE PERIPHERAL CABLE ASSEMBLY
	FIN.	
SCALE NONE / CODE	DR S.J. STEELE 80-08-28 APPD R.F. ABRAHAM 81-03-16	SIZE A / DWG NO 58056843 / SH 1/6 / REV D



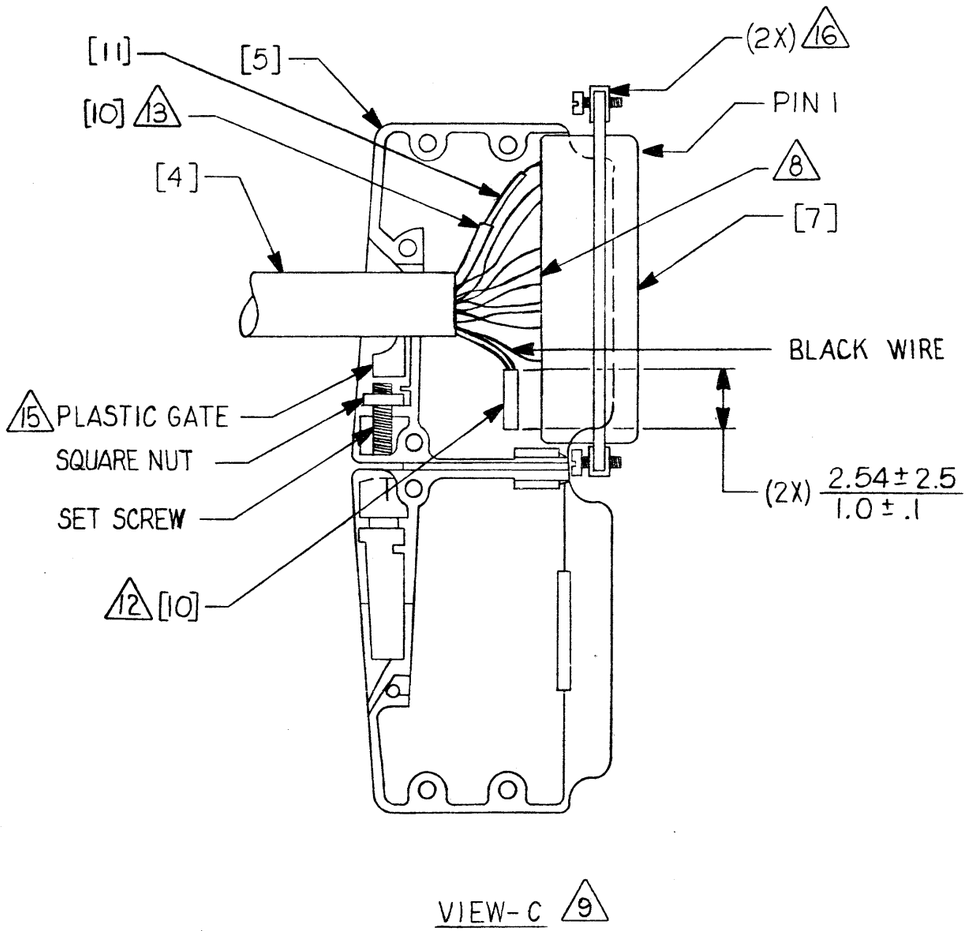
VIEW-A
PIN NUMBERING LOOKING AT CONNECTOR P1



VIEW-B 14

FIGURE 1. EXTERNAL CABLE ASSEMBLY - CONTINUED

Honeywell	SIZE A	DWG NO 58056843	SH 2	REV D



VIEW-C 9

FIGURE 1. EXTERNAL CABLE ASSEMBLY - CONTINUED

TABLE I. TOLERANCE FOR CABLE ASM LENGTH 2

LENGTH RANGE (M)	TOLERANCE (M)
1 TO 10	+.15 , -0
11 TO 20	+.20 , -0
21 TO 30	+.30 , -0
31 TO 40	+.40 , -0
41 TO 50	+.50 , -0

TABLE II. WIRE LIST 6 8 12

FROM P1	TO P2	COLOR	TYPE
01	06	BLACK	TWISTED PAIR
11	24	WHITE	
10	04	BLACK	TWISTED PAIR
20	22	WHITE	
04	08	BLACK	TWISTED PAIR
14	26	WHITE	
07	17	BLACK	TWISTED PAIR
17	35	WHITE	
12	[illegible]	BLACK	TWISTED PAIR
18	01	SHIELD	13

NOTES:

△1. TAB-001 OF THIS DRAWING SHALL BE USED ONLY FOR ADVANCE ORDERING OF MATERIAL. THE CONDUCTOR LENGTH SPECIFIED IN TAB-001 IS AN AVERAGE LENGTH TO FACILITATE ADVANCE ORDERING.

△2. THE TAB NUMBER (EXCEPT TAB 001) SPECIFIES THE CABLE ASM LENGTH IN METERS.

EXAMPLE:

580XXXXX-003 IS THE L DIMENSION OF A 3 METER CABLE ASM. TOLERANCE OF THE CABLE ASM LENGTH SHALL BE PER TABLE I.

△3. SOLDER CONNECTOR (ITEM 2) TO PWB (ITEM 3) PER 58053700.

△4. MARK PER 58053700.

△5. MARK PER 58053700 AS A UL LISTED LOGIC CABLE ASM USING DRAWING NUMBER 58056843, TAB NUMBER, AND REVISION LETTER AS THE ASM IDENTIFICATION.

△6. TERMINATE CABLE (ITEM 4) TO PWB (ITEM 3) PER TABLE II WIRE LIST AND 58053700. EXTENSION OF CABLE'S CONDUCTORS BEYOND THE BOTTOM SIDE OF PWB (ITEM 3) SHALL BE .75 MM (.030 INCH) MAX. SOLDER CONNECTIONS PER 58053700.

△7. THERE SHALL BE NO EVIDENCE OF THE CABLE'S JACKET MATERIAL HARDENING AS A RESULT OF THE SOLVENT CLEANING PROCESS.

△8. TERMINATE CABLE (ITEM 4) TO CONTACTS (ITEM 8) AND CRIMP PER 58053700. INSTALL INTO CONNECTOR (ITEM 7) PER TABLE II WIRE LIST.

△9. VIEW C SHOWN WITH HARDWARE HOUSING (ITEM 5) IN OPEN POSITION.

△10. SCREWS (ITEM 12 AND ITEM 13) ATTACH COVER (ITEM 1) TO PWB (ITEM 3).

NOTES (CONTINUED):

△11. LEADS OF CONNECTOR (ITEM 2) SHALL NOT HAVE ANY SOLDER BEYOND DIMENSION SPECIFIED.

△12. TWO TWISTED PAIR AND ONE UNTWISTED WHITE WIRE OF CABLE (ITEM 4) SHALL BE SECURED TOGETHER, USING SLEEVING (ITEM 10), FOR USE AS SPARES.

△13. TWIST WIRE (ITEM 11) AND CABLE (ITEM 4) SHIELD TOGETHER AND SOLDER PER 58053700. COVER USING SLEEVING (ITEM 10).

△14. VIEW B IS SHOWN WITHOUT COVER (ITEM 1) INSTALLED.

△15. HARDWARE'S (ITEM 5) CLAMPING MECHANISM CONSISTS OF A SET SCREW, SQUARE NUT, AND PLASTIC GATE. POSITION PLASTIC GATE AS SHOWN.

△16. FLAT SIDE OF HARDWARE'S (ITEM 5) CLIP-NUT SHALL BE ON THIS SURFACE OF CONNECTOR (ITEM 7).

17. CABLE ASM SHALL MEET THE COMPLETED CABLE ASM REQUIREMENTS OF 58053700.

18. THIS CABLE ASM IS GOVERNED BY PURCHASE SPECIFICATION 58053717.

58081041

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	ASM TAB NO. 001	014	018	022	PL ALL	DWG.NO. 1	2	3	4	5	6
A	LEVEL I ISSUE	83	JUN	10	J. M. Bell 5-24-83	A	A	A	A	A	A					
B	PHASE GD519	83	OCT	31	K. Smith	B	B	B	B	B	B					
C	PHASE GD526	83	DEC	09	B. J. [illegible]	C	C	C	C	C	C					
C1	LEVEL 2 ENX 149		ND		G DLENTH	C1	C1	C1	C1							
D	PHASE GD539	84	01	26	E. Zuck	D	D	D	D	D	D	D	D	D	D	D

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

CE 300 A-3 (1-79)

MADE BY R. Hockstra 83 April 04

APPROVED R. Hockstra 5/20/83

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CABLE I/O ASM

SIZE	REVISION STATUS FOR	SHEET	REV
A	58081041	1/1	D

DIST. C106-71, GU-71

PD 84/01/26 A 58081041 1/2 D

			001	014	018	022		
1 C	58034066-001	V PADDLE BD COVER	1	1	1	1		EA
2 A	58000038-008	V CONNECTOR, PWB	1	1	1	1		EA
3 C	58047470-003	A PWB ETCH & DRILL	1	1	1	1		EA
6 A	76951105-563	V SCREW THD FORMING	2	2	2	2		EA
7 A	58020397-001	V CABL MULTICOND COAX	600	551	709	866		IN
8 A	76951105-502	V SCREW THD FORMING	5	5	5	5		EA
9 D	60121950-001	P HOOD CONN CASTING	1	1	1	1		EA
10 C	60121964-001	P COVER	1	1	1	1		EA
11 A	60120593-001	P RING PULL	1	1	1	1		EA
12 C	60121967-001	P CAPTIVE SCREW	1	1	1	1		EA
13 B	60117607-001	P STRAIN RELIEF	1	1	1	1		EA
14 A	03910182-001	V LABEL PERMANENT	1	1	1	1		EA
15 B	58054218-003	A PWB ETCH & DRL	1	1	1	1		EA
15 B	58054218-002	A PWB ETCH & DRILL	NOINT	NOINT	NOINT	NOINT		EA
16 B	878B222P120	V SLEEVING	15	15	15	15		IN
21 A	58073431-011	V LK/WASH.EXT.TOOTH,ST	2	2	2	2		EA

CABLE I/O ASSEMBLY

A 58081041 1/2 D

					001	014	018	022	
*	22	A	76951715-045	V LOCKWASHER	1	1	1	1	EA
*	23	A	76951715-059	V LOCKWASHER	2	2	2	2	EA
*	24	A	58033849	V #608 HYSOL	AR	AR	AR	AR	OZ
*	25	B	43B111126P15	V WIRE BARE SOLID	3	3	3	3	IN
*	26	A	58053382-006	V TUBING,FLEX,CLEAR	1	1	1	1	IN
*	27	A	58053732	V IPL EXT CABLE ASM	X	X	X	X	EA

REF SPEC NO
58053700
58053732

REVISION				
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE

58081041

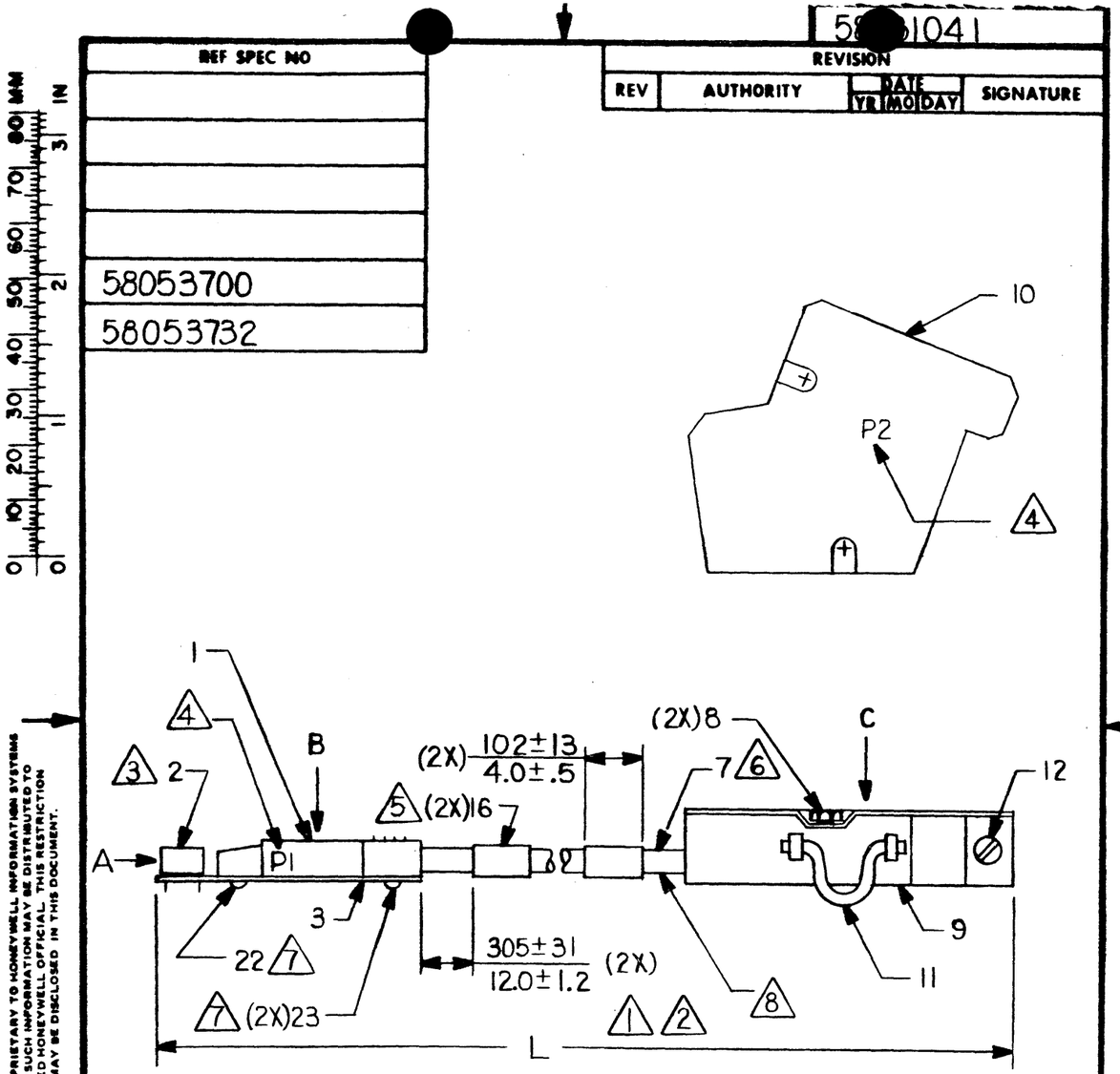
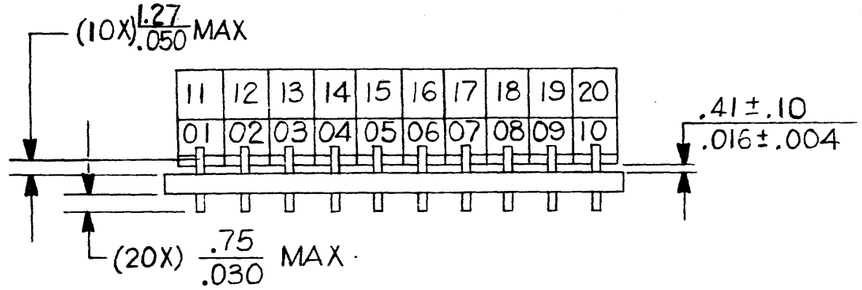


FIGURE 1. EXTERNAL CABLE ASSEMBLY

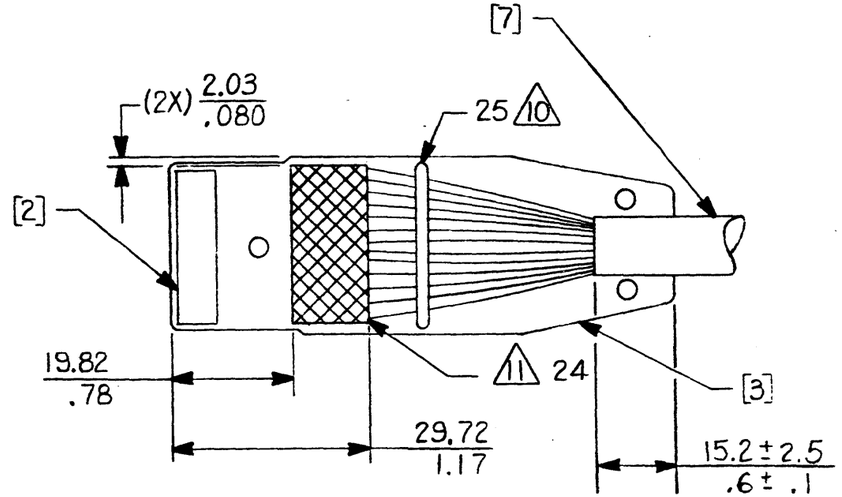
FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE MILLIMETERS / INCHES TOLERANCE OF SIZE AND FORM PER INITIAL DESIGN PROJECTION	MATL TREAT. FIN.	**Honeywell** HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U. S. A. TITLE: CABLE I/O ASSEMBLY
SCALE NONE / CODE	DR R.HOEKSTRA 83-04-05 APPD K.P.ABRAHAM 83-05-20	SIZE A / DWG NO 58081041 / SH 1/6 / REV D

CE 300 A-1 (12-71)



VIEW-A
PIN NUMBERING LOOKING AT CONNECTOR P1

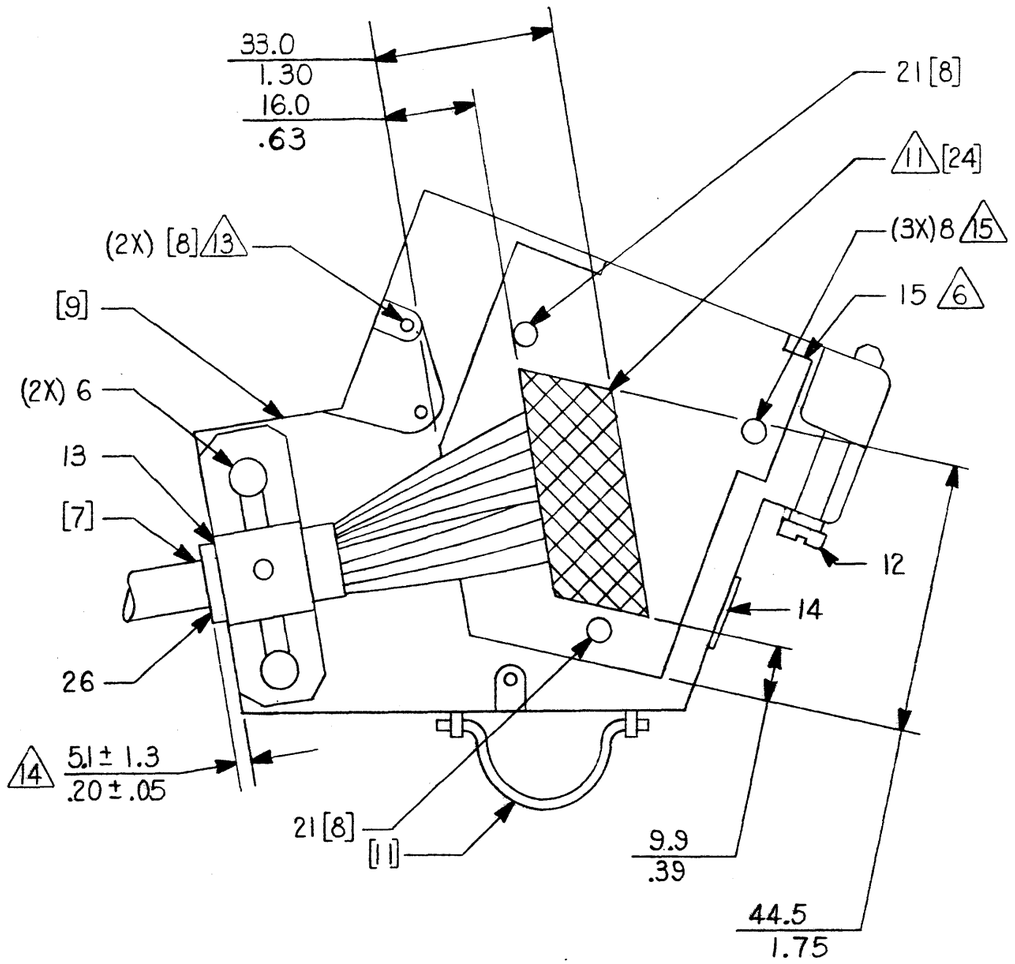


VIEW-B 12

FIGURE 1. EXTERNAL CABLE ASSEMBLY - CONTINUED

Honeywell	SIZE A	DWG NO 58081041	SH 2 / REV D

CE 300 A-2 (5-78)



VIEW- C 16

FIGURE I. EXTERNAL CABLE ASSEMBLY

TABLE I. TOLERANCE FOR CABLE ASM LENGTH 2

LENGTH RANGE (M)	TOLERANCE (M)
1 TO 10	+.15 , -0
11 TO 20	+.20 , -0
21 TO 30	+.30 , -0
31 TO 40	+.40 , -0
41 TO 50	+.50 , -0

TABLE II. WIRE LIST 6 17

FROM P1	TO P2
01	13
03	14
04	16
06	59
07	19
09	21
10	20
11	11
12	12
14	53
15	15
17	56
18	17
20	22

NOTES:

△ 1. TAB-001 OF THIS DRAWING SHALL BE USED ONLY FOR ADVANCE ORDERING OF MATERIAL. THE CONDUCTOR LENGTH SPECIFIED IN TAB-001 IS AN AVERAGE LENGTH TO FACILITATE ADVANCE ORDERING.

△ 2. THE TAB NUMBER (EXCEPT TAB 001) SPECIFIES THE CABLE ASM LENGTH IN METERS.

EXAMPLE:

580XXXXX-003 IS THE L DIMENSION OF A 3 METER CABLE ASM. TOLERANCE OF THE CABLE ASM LENGTH SHALL BE PER TABLE I.

△ 3. SOLDER CONNECTOR (ITEM 2) TO PWB (ITEM 3) PER 58053700.

△ 4. MARK PER 58053700.

△ 5. MARK PER 58053700 AS A UL LISTED LOGIC CABLE ASM USING DRAWING NUMBER 58081041, TAB NUMBER, AND REVISION LETTER AS THE ASM IDENTIFICATION.

△ 6. TERMINATE CABLE (ITEM 7) TO PWB'S (ITEM 3 AND ITEM 15) PER TABLE II WIRE LIST AND 58053700. SOLDER CONNECTIONS AND EPOXY COAT PER 58053700.

△ 7. SCREWS (ITEM 18 AND ITEM 19) ATTACH COVER (ITEM 1) TO PWB (ITEM 3).

△ 8. THERE SHALL BE NO EVIDENCE OF THE CABLE'S JACKET MATERIAL HARDENING AS A RESULT OF THE SOLVENT CLEANING PROCESS.

△ 9. LEADS OF CONNECTOR (ITEM 2) SHALL NOT HAVE ANY SOLDER BEYOND DIMENSION SPECIFIED.

△ 10. HOLD DOWN WIRE (ITEM 25) TO BE INSTALLED PER 58053700 AND SHALL HAVE A MAX EXTENSION BEYOND BOTTOM SIDE OF PWB (ITEM 3) OF .75 MM (.030 INCH).

NOTES (CONTINUED):

△ 11. CABLE TERMINATION NOT SHOWN IN ORDER TO MORE CLEARLY SHOW THE AREA TO WHICH THE EPOXY (ITEM 24) IS RESTRICTED. THE HEIGHT OF THE CURED EPOXY SHALL BE 2.21 MM (.087 IN.) MAX.

△ 12. VIEW B IS SHOWN WITHOUT COVER (ITEM 1) INSTALLED.

△ 13. SCREWS (ITEM 8) ATTACH COVER (ITEM 10) TO CONNECTOR CASTING (ITEM 9).

△ 14. CABLE (ITEM 7) SHALL BE SECURELY CLAMPED TO CONNECTOR CASTING (ITEM 9) USING STRAIN RELIEF (ITEM 13), SCREWS (ITEM 6), AND TUBING (ITEM 26). WHEN INSTALLED, TUBING (ITEM 26) SHALL EXTEND WITHIN DIMENSION SPECIFIED.

△ 15. SCREWS (ITEM 8) ATTACH PWB (ITEM 15) TO CONNECTOR CASTING (ITEM 9).

△ 16. VIEW C IS SHOWN WITHOUT COVER (ITEM 10) INSTALLED.

△ 17. PINS 02, 05, 08, 13, 16, AND 19 ARE GROUNDED TO CABLE SHIELDS IN BOTH P1 AND P2.

18. CABLE ASM SHALL MEET THE COMPLETED CABLE ASM REQUIREMENTS OF 58053700.

19. THIS CABLE ASM IS GOVERNED BY PURCHASE SPECIFICATION 58053732.

58034102

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 001	TAB 014	TAB 018	TAB 022	AL AL	ASM. 1
A	LEVEL 1-ISSUE	79	09	09	S.E. Stroda 79-09-28	A				A	A
B	PHAØFC008	79	NOV	15	C. Ripley	B					B
C	PHAØPV083	79	12	13	R.M. Delgretto	C				C	
D	PHAØPV140	80	03	24	A. Lopez	D				D	D
E	PHAØPV165	80	DEC	10	Carrie Dale	E				E	
F	PHAØXW114	82	APR	02	D.J. Steele	F	F	F	F	F	F
G	PHAØGD483	83	06	21	S. Miller	G	G	G	G		G
						INACTIVE-RESV	INACTIVE-RESV	INACTIVE-RESV	INACTIVE-RESV		

F.C.F.

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS

LOC PHOENIX, ARIZONA

MADE BY Ted Gunsford 79, MAY, 23

APPROVED R. F. Albertson 79/09/20

TITLE CABLE I/O

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

SIZE	REVISION STATUS FOR	SHEET	REV
C	58034102	11	G

CE 300 A-3 (12-71) BRUNING 44-141

DIST. C106- 73

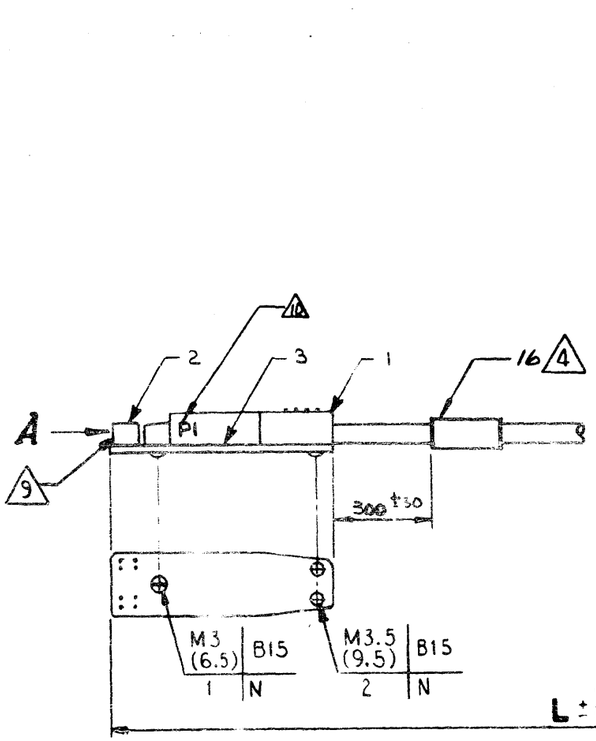
PD 82/04/02 C 58034102 1/1 F

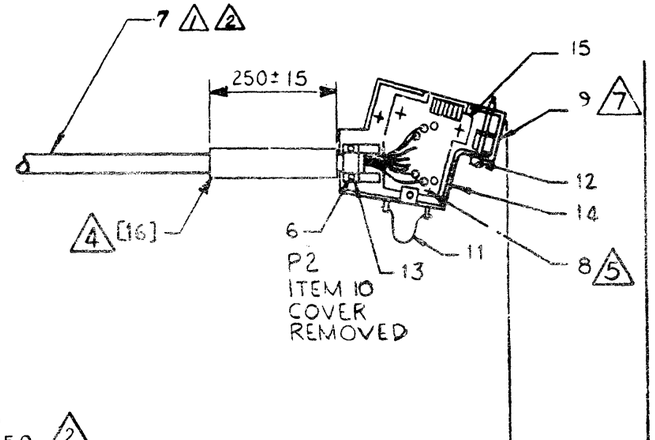
					001	014	018	022		
•	1	C	58034066-001	V PADDLE BD COVER	1	1	1	1		EA
•	2	A	58000038-008	V CONNECTOR, PWB	1	1	1	1		EA
•	3	C	58047470-003	A PWB ETCH & DRILL	1	1	1	1		EA
•	6	A	76951105-563	V SCREW THD FORMING	2	2	2	2		EA
•	7	A	58020397-001	V CABL MULTICOND COAX	600	551	709	866		IN
•	8	A	76951105-502	V SCREW THD FORMING	5	5	5	5		EA
•	9	D	60121950-001	P HOOD CONN CASTING	1	1	1	1		EA
•	10	C	60121964-001	P COVER	1	1	1	1		EA
•	11	A	60120593-001	P RING PULL	1	1	1	1		EA
•	12	C	60121967-001	P CAPTIVE SCREW	1	1	1	1		EA
•	13	B	60117607-001	P STRAIN RELIEF	1	1	1	1		EA
•	14	A	03910182-001	V LABEL PERMANENT	1	1	1	1		EA
•	15	B	58054218-002	A PWB ETCH & DRILL	1	1	1	1		EA
•	16	B	878B222P120	V SLEEVING	15	15	15	15		IN
•	17	A	43A115944P42	P TAPE POLYESTER	5	5	5	5		IN

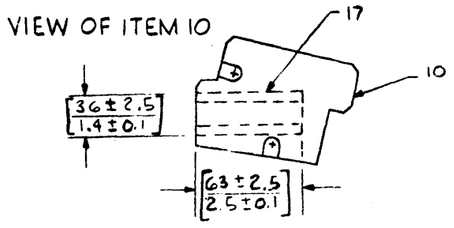
CABLE, I/O

C 58034102 1/1 F

REVISIONS				
REV	AUTHORITY	DATE YR	MO DAY	SIGNATURE







001 1

INACTIVE -
FOR NEW DESIGN
SEE DWG- 58081041

11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	10

VIEW-A
PIN NUMBERING
LOOKING AT CONNETOR P1.

WIRE LIST 7	
FROM P1	TO P2
01	13
03	14
04	16
06	59
07	19
09	21
10	20
11	11
12	12
14	53
15	15
17	56
18	17
20	22

REF SPEC NO

12. ASSEMBLE COAX ITEM 7 TO PWBS ITEM 3 AND ITEM 15 PER 58020440.

11. THE MAXIMUM SOLDERED LEAD LENGTH OF CONNECTOR ITEM 2 SHALL BE .75MM BEYOND THE SURFACE OF PWB ITEM 3.

10 MARK PER 43A226458 CLASS-C.

9. CONNECTOR ITEM 2 SHALL BE SOLDERED 0.4±0.1mm ABOVE SURFACE OF ITEM 3.

8. ASSEMBLE ITEMS 2 & 7 TO ITEM 3 AND ITEM 7 TO ITEM 15 PER 43A226454.

7. ITEM 9 IS SHOWN WITH COVER REMOVED.

6. PINS 02,05,08,13, 16 & 19 ARE GROUNDED TO CABLE SHIELDS IN BOTH CONNECTORS.

5. ITEM 8 (SCREWS) ATTACHES ITEMS 15 AND 10 TO 9.

4. MARK PER 43A144110 AS A UL LISTED LOGIC CABLE.

3. ASSEMBLE HARDWARE PER M50EB00506-CR.

2. THE TAB NUMBERS (EXCEPT TAB 001) SPECIFIES THE CABLE LENGTH IN METERS. TYPICAL EXAMPLE ARE: 58034102-003 IDENTIFIES A 3 METER CABLE PREFERRED STANDARD CABLE LENGTHS. USE CABLE LENGTHS 14 18 AND 22 METERS.

1. TAB-001 OF THIS DRAWING SHALL BE USED ONLY FOR ADVANCE ORDERING OF MATERIAL. THE CONDUCTOR LENGTH SPECIFIED IN TAB 001 IS AN AVERAGE LENGTH TO FACILITATE ADVANCE ORDERING.

NOTES:

58034102

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS / INCHES; TOLERANCE OF SIZE AND FORM PER; INITIAL DESIGN M; PROJECTION	MATL	Honeywell HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U. S. A.	
	DES [illegible] 79 JUN 4	TITLE CABLE I/O	
	CHKR [illegible] 79 SEP 27	FCF:	
	FIN.	SIZE C	DWG NO 58034102
SCALE	CODE	DR [illegible] 79 JUN 5	SH 1/1
		APPD [illegible] 79/9/20	REV G
		DISTR C106-73	

BRUNING 44 141 23041 3
CE 300 C (12 71)

0 10 20 30 40 50 60 70 80 MM
0 1 2 3 IN

58081326

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO. 001	031	038	045	PL ALL	DWG. SH. NO. 1
A	LEVEL 1 ISSUE	83	06	21	Ken J. L. 6-15-83	A	A	A	A	A	A
B	PHA#GD519	83	10	31	J Dinetz	B	B	B	B	B	B
C	PHA#GD505	83	11	28	G. Miller	C	C	C	C	C	
D	PHA#GD526	83	12	09	R Lubenow	D	D	D	D	D	D

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX, ARIZONA

MADE BY Rick Lubin 83JUN10

APPROVED R Lubenow 6/13/83

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CABLE, I/Ø

SIZE	REVISION STATUS FOR	SHEET	REV
C	58081326	1/1	D

DIST. C107-71, GU-71

BRUNING 44-141 40366

CE 300 A-3 (1-79)

				001	031	038	045	
1	C	58034066-001	V PADDLE BD COVER	1	1	1	1	EA
2	A	58000038-008	V CONNECTOR, PWB	1	1	1	1	EA
3	C	58047470-003	A PWB ETCH & DRILL	1	1	1	1	EA
6	A	76951105-563	V SCREW THD FORMING	2	2	2	2	EA
7	A	58020397-002	V CABL MULTICOND COAX	1500	1220	1496	1772	IN
8	A	76951105-502	V SCREW THD FORMING	5	5	5	5	EA
9	D	60121950-001	P HOOD CONN CASTING	1	1	1	1	EA
10	C	60121964-001	P COVER	1	1	1	1	EA
11	A	60120593-001	P RING PULL	1	1	1	1	EA
12	C	60121967-001	P CAPTIVE SCREW	1	1	1	1	EA
13	B	60117607-001	P STRAIN RELIEF	1	1	1	1	EA
14	A	03910182-001	V LABEL PERMANENT	1	1	1	1	EA
15	B	58054218-003	A PWB ETCH & DRL	1	1	1	1	EA
15	B	58054218-002	A PWB ETCH & DRILL	NOINT	NOINT	NOINT	NOINT	EA
16	B	8788222P120	V SLEEVING	34	34	34	34	IN
17	A	03010216-101	V SCREW,THD ROLL HEX	1	1	1	1	EA

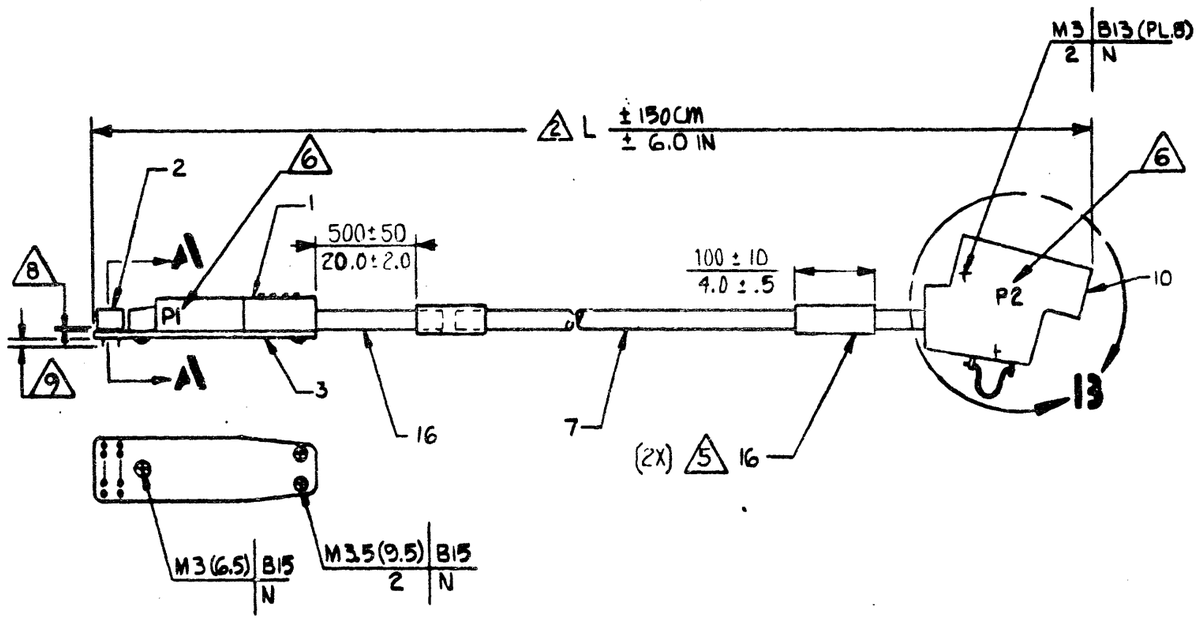
CABLE I/O

PD 83/12/10 C 58081326 2/F D

					001	031	038	045		
	21	A	58073431-011	V [illegible]K/WASH.EXT.TOOTH,ST	2	2	2	2		EA
*	22	A	58053733	V CABLE	X	X	X	X		EA

CABLE I/O

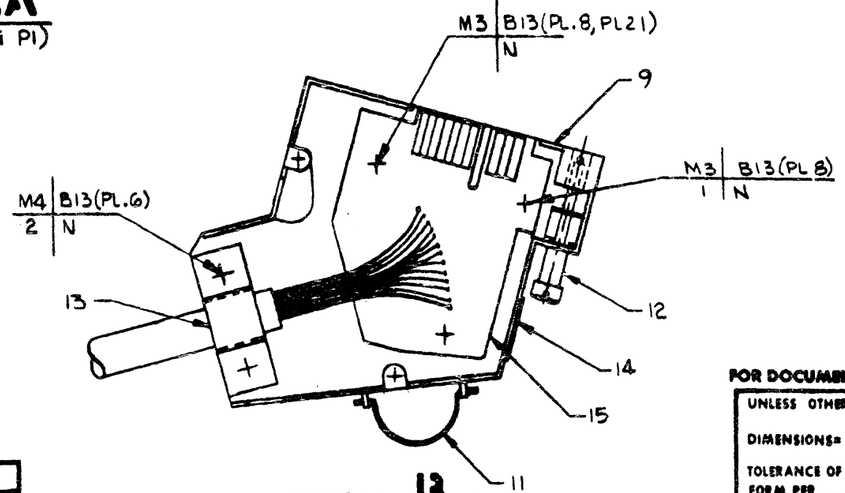
C 58081326 2/F D



11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	10

3 VIEW A-A
(PIN NUMBERING P1)

WIRE LIST	
FROM:	TO:
P1-01	P2-13
-03	-14
-04	-16
-06	-59
-07	-19
-09	-21
-10	-20
-11	-11
-12	-12
-14	-53
-15	-15
-17	-56
-18	-17
P1-20	P2-22



DETAIL 13
(COVER REMOVED)

43A144110
43A226454
43A226458
M50EB00506-CR
REF SPEC NO

001 1

REVISIONS

REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

12. THIS ASSEMBLY MAY BE PROCURED BY USING PURCHASE SPECIFICATION PL ITEM 21.

~~△11. SOLDER ITEM 20 TO UPPER SHIELDS OF ITEM 7.~~

△9. MAXIMUM SOLDERED LEAD LENGTH OF CONNECTOR, ITEM 2, SHALL BE $\frac{.75}{.03}$ BEYOND THE SURFACE OF PWB, ITEM 3.

△8. CONNECTOR, ITEM 2, SHALL BE SOLDERED $\frac{0.4 \pm 0.1}{.02 \pm .004}$ ABOVE SURFACE OF ITEM 3 PER 43A226454.

7. ASSEMBLE COAX, ITEM 7, TO PWB'S, ITEMS 3 AND 15, PER 58020440.

△6. MARK PER 43A226458, CLASS C.

△5. MARK PER 43A144110 AS A UL LISTED LOGIC CABLE.

4. ASSEMBLE HARDWARE PER M50EB00506-CR.

△3. PINS 02, 05, 08, 13, 16 AND 19 ARE GROUNDED TO CABLE SHIELDS IN BOTH CONNECTORS.

△2. THE TAB NUMBER (EXCEPT TAB -001) SPECIFIES THE CABLE LENGTH IN METERS. TYPICAL EXAMPLE. 58081041-010 IDENTIFIES A 10 METER CABLE.

△1. TAB-001 OF THIS DRAWING SHALL BE USED ONLY FOR ADVANCE ORDERING OF MATERIAL.

NOTES.

58081326

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS / INCHES	MATL	Honeywell HONEYWELL INFORMATION SYSTEMS
TOLERANCE OF SIZE AND FORM PER	DSN:	LOC PHOENIX, ARIZONA U.S.A.
INITIAL DESIGN M	CHK:	TITLE CABLE, I/Ø
PROJECTION	FIN.	FCF:
SCALE / CODE	DR Rachel Larkin 83JUN10	SIZE C / DWG NO 58081326 / SH 1/1 / REV D
	APPD [illegible] 6/13/83	
	DISTR C107-71, GU-71	

58058769

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE
A	LEVEL 1 ISSUE	81	MAR	25	J. Dooley 3/18/81
B	PHAØPV411	82	MAR	08	N.C. Oetting
C	PHAOGD483	83	06	21	S. Miller

TAB

DOC	PL	DWG SH						
	ALL	1						
A	A	A						
B	B							
C		C						

INACTIVE-RESV

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS

LOC PHOENIX, ARIZONA

MADE BY S.J. Steele 81-MAR-13

APPROVED R Albertson 3/16/81

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CABLE I/O

SIZE	REVISION STATUS FOR	SHEET	REV
C	58058769	1/1	C

CE 300 A-3 (12-71) BRUNING 44-141

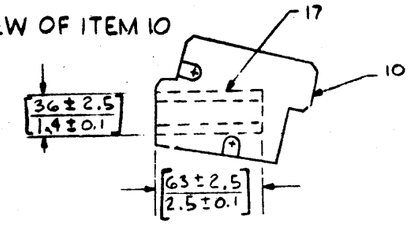
DIST: C106-73

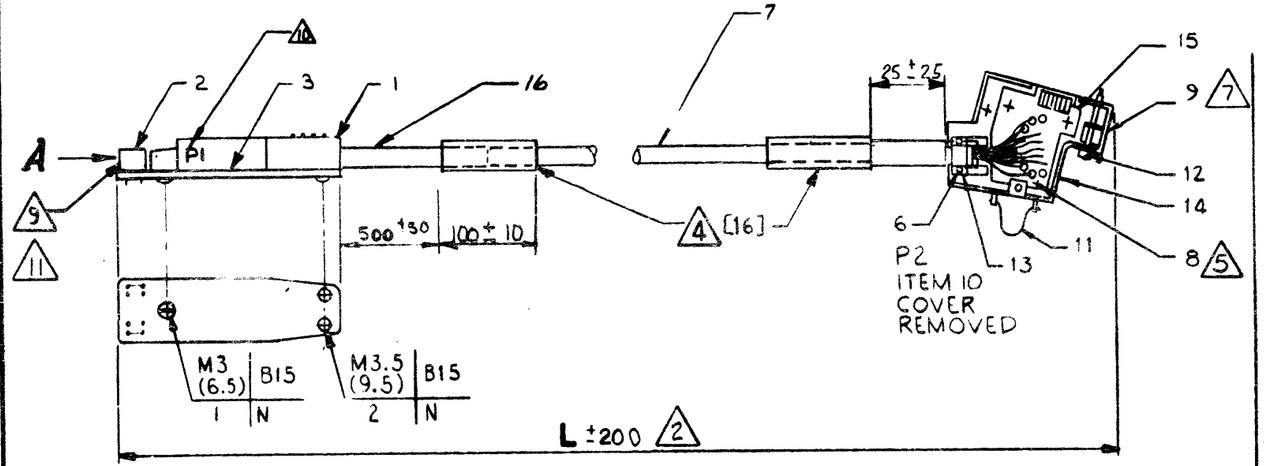
001

1	C	58034066-001	V	PADDLE BD COVER	1	EA
2	A	58000038-008	V	CONNECTOR, PWB	1	EA
3	C	58047470-002	A	PWB ETCH & DRILL	1	EA
6	A	76951105-563	V	SCREW THD FORMING	2	EA
7	A	58020397-002	V	CABL MULTICOND COAX	1500	IN
8	A	76951105-502	V	SCREW THD FORMING	5	EA
9	D	60121950-001	P	HOOD CONN CASTING	1	EA
10	C	60121964-001	P	COVER	1	EA
11	A	60120593-001	P	RING PULL	1	EA
12	C	60121967-001	P	CAPTIVE SCREW	1	EA
13	B	60117607-001	P	STRAIN RELIEF	1	EA
14	A	03910182-001	V	LABEL PERMANENT	1	EA
• 15	B	58054218-002	A	PWB ETCH & DRILL	1	EA
• 15	B	58054218-001	A	PWB ETCH & DRL	INTCH	EA
16	B	878B222P120	V	SLEEVING	34	IN
17	A	43A115944P42	P	TAPE POLYESTER	5	IN

REVISIONS			
REV	AUTHORITY	DATE YR MO DAY	SIGNATURE

VIEW OF ITEM 10





001 △1

INACTIVE-
FOR NEW DESIGN
SEE DWG 58081324

11	12	13	14	15	16	17	18	19	20
01	02	03	04	05	06	07	08	09	10

VIEW-A
PIN NUMBERING LOOKING AT CONNETOR P1.

WIRE LIST △	
FROM P1	TO P2
01	13
03	14
04	16
06	59
07	19
09	21
10	20
11	11
12	12
14	53
15	15
17	56
18	17
20	22

△12. ASSEMBLE COAX ITEM 7 TO PWBS ITEM 3 AND ITEM 15 PER 58020440.

△11. THE MAXIMUM SOLDERED LEAD LENGTH OF CONNECTOR ITEM 2 SHALL BE .75MM BEYOND THE SURFACE OF PWB ITEM 3.

△10 MARK PER 43A226458 CLASS-C.

△9. CONNECTOR ITEM 2 SHALL BE SOLDERED 0.4 ± 0.1mm ABOVE SURFACE OF ITEM 3.

8. ASSEMBLE ITEMS 2 & 7 TO ITEM 3 AND ITEM 7 TO ITEM 15 PER 43A226454.

△7. ITEM 9 IS SHOWN WITH COVER REMOVED.

△6. PINS 02,05,08,13, 16 & 19 ARE GROUNDED TO CABLE SHIELDS IN BOTH CONNECTORS.

△5. ITEM 8 (SCREWS) ATTACHES ITEMS 15 AND 10 TO 9.

△4. MARK PER 43A144110 AS A UL LISTED LOGIC CABLE.

3. ASSEMBLE HARDWARE PER M50EB00506-CR.

△2. THE TAB NUMBER SPECIFIES THE CABLE LENGTH IN METRES. TYPICAL EXAMPLES ARE: 5800XXXX-003 IDENTIFIES A 3 METER AND 5800XXXX-010 IDENTIFIES A 10-METER CABLE. PREFERRED STANDARD CABLE LENGTHS. USE CABLE LENGTHS 31, 38 AND 45 METERS.

△1. TAB-001 OF THIS DRAWING SHALL BE USED ONLY FOR ADVANCE ORDERING OF MATERIAL. THE CONDUCTOR LENGTH SPECIFIED IN TAB 001 IS AN AVERAGE LENGTH TO FACILITATE ADVANCE ORDERING.

NOTES:

43A226454
43A226458
43A144110
REF SPEC NO

BRUNING 44 141 230413

CE 300 C (12-71)

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED
DIMENSIONS= MILLIMETERS / INCHES
TOLERANCE OF SIZE AND FORM PER
INITIAL DESIGN M
PROJECTION

SCALE | CODE

MATL

DESN 81 MAR 16
CHK 81 MAR 17
FIN.
DR 81 MAR 13
APD 3/16/81
DISTR C106-75

Honeywell
HONEYWELL INFORMATION SYSTEMS
LOC PHOENIX, ARIZONA U.S.A.
TITLE CABLE I/O
FCF:

SIZE	DWG NO	SH	REV
C	58058769	1/1	C

58058769

0 10 20 30 40 50 60 70 80 MM
0 1 2 3 IN

Honeywell HONEYWELL INFORMATION SYSTEMS INC.		SPEC. NO. A 58053369	A1/1	A
LOC. PHOENIX, AZ	DISTRIBUTION CODE GU-50	PROJECTION	CODE EV4 6150	
PREPARED BY M.McMeekin DATE 82-06-11 APPROVED BY DATE	TITLE CABLE ASSEMBLY, FIBER OPTIC			

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	LEVEL 1 ISSUE	SEP 0 1 1982	M.McMeekin	RSS A1/1 & Shs. A1/6 thru A6F.

W Pickard 6-2-82
LEVEL 1 ISSUE
R L Abraham 6/11/82
APPROVAL

TITLE: CABLE ASSEMBLY, FIBER OPTIC

1.0 SCOPE

This specification defines the requirements for a series of dual optical fiber cable assemblies for indoor use.

2.0 APPLICABLE DOCUMENTS

The following documents form a part of this specification to the extent referenced herein:

Honeywell Information Systems (IS) Documents -

58053363	Connector, Fiber Optic
58053368	Cable, Fiber Optic
878B222	Heat Shrink Sleeving
58075088	Fiber Optic Connector Assembly Specification

In case of conflict, the order of precedence of the following documents is:

This specification
Other specifications referenced herein.

3.0 REQUIREMENTS

3.1 MECHANICAL

3.1.1 Outline Drawing

Cable Assembly Drawing, Figure 1.

3.1.2 Material

3.1.2.1 Fiber Optic Connector - per 58053363, tabs as follows:

Heat Shrink Sleeving	-001
Dust Cap	-002
Ferrule	-102
Metal Cap/Eyelet Assembly	-201

3.1.2.3 Shrink Sleeving (3/8" O.D., black) - per 878B222P100.

3.1.2.4 Fiber Optic Cable - per 58053368-001.

3.1.3 Connector Assembly

Connectors shall be assembled to cable per 58075088.

3.1.4 Cable Assembly Length Requirements

3.1.4.1 The drawing tab number shall specify the cable length in decameters; for example, 58053369-001 specifies a 10 meter cable and 58053369-075 specifies a 750 meter cable.

3.1.4.2 Maximum Length - The maximum length of any cable ordered shall be 2000 meters (6562 ft.).

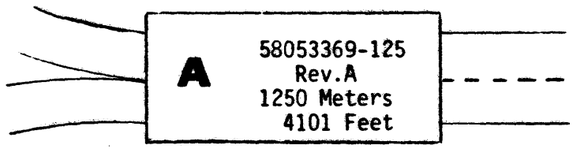
3.1.5 IN/OUT Marking

Mark "IN" or "OUT" on sleeves on both ends of the cable per Cable Assembly Drawing, Figure 1 and Fiber Connection Diagram, Figure 2. The marking shall be a permanent contrasting color.

3.1.6 Identification Marking

Mark sleeves on both ends of the cable with IS drawing/tab number, latest revision letter, and the length in meters and feet. Also, mark "A" or "B" on both ends of the cable per Figure 1 and Figure 2. All marking shall be a permanent contrasting color.

Example of an "A" end marking:



3.2 OPTICAL CHARACTERISTICS

3.2.1 Attenuation

Each fiber length in the finished cable assembly shall have a maximum attenuation that can be calculated by using the following formula.

$$\text{Maximum Cable Attenuation} = 4\text{DB}\left(\text{Max. loss for connectors and test receptacles}^{*}\right) + .006\ \text{DB} \times \text{The fiber's length in meters}$$

Maximum attenuation is measured at an 820 nm wavelength.

3.2.2 Bandwidth

Per 58053368-001.

3.2.3 Numerical Aperture

Per 58053368-001.

*Receptacles shall have matching numerical aperture and fiber diameter components.

3.3 ENVIRONMENTAL (APPLICATION)

3.3.1 Temperature Range

Cable per 58053368-001; Connector per 58053363.

3.3.2 Applied Tensile Strength (Cable only)

Per 58053368-001.

3.3.3 Cable Bend Radius (Cable only)

Per 58053368-001.

3.3.4 Applied Crush Resistance (Cable only)

Per 58053368-001.

4.0 QUALITY ASSURANCE PROVISION

4.1 The cable assembly manufacturer shall record the attenuation and Optical Time Domain Reflectometer (OTDR) waveform of each fiber in the finished cable assembly, then forward this information with the cable assembly. The two fibers will be identified as #1 (IN A - OUT B) and #2 (OUT A - IN B).

5.0 PREPARATION FOR DELIVERY

5.1 SHIPPING CONTAINER

Each cable shall be wrapped with both ends accessible for testing on a non-returnable spool (minimum 203 mm [8 inch] core diameter), then packaged inside a protective shipping carton.

5.2 Shipping cartons shall be marked as follows:

5.2.1 HISI drawing/tab number and latest revision letter.

5.2.2 Assembly Manufacturer's Name

5.2.3 Date of Assembly

5.3 Maximum cable length shall be per 3.1.4.3.

5.4 Test information per paragraph 4.1 shall be securely packed with cable.

5.5 Cable weight - Per 58053368-001.

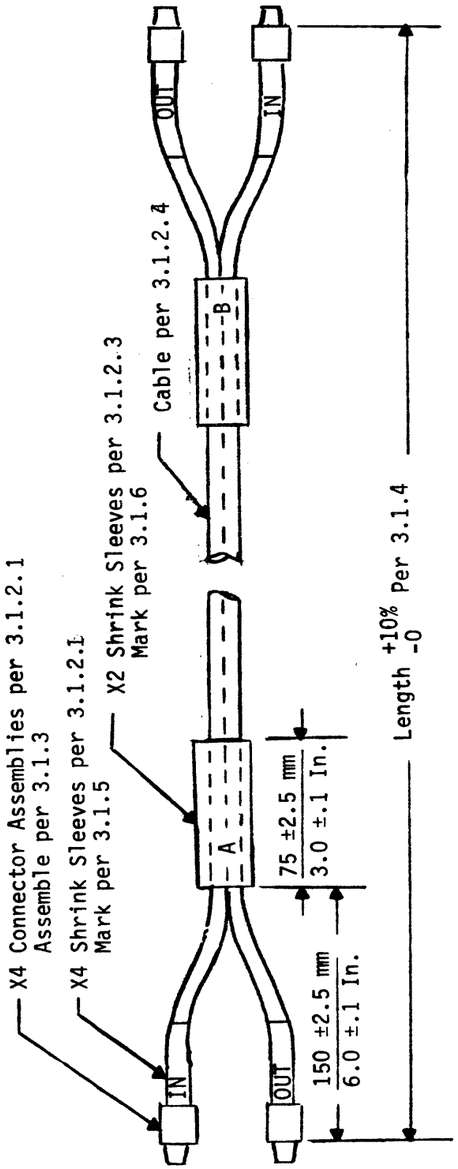
6.0 NOTES

6.1 Purchase from an approved vendor per 43A997260, Vendor Approval Listing.

6.2 Cable Installation Requirement (Important)

To prevent damaging the cable's glass fiber, the cable should not be folded, pinched or strained during installation. The bend radius (per 3.3.3) and tensile strength (per 3.3.2) limits defined in this specification must be followed. During cable installation special unreeling and handling equipment may have to be used to stay within these limits.

Honeywell
HONEYWELL INFORMATION SYSTEMS INC.
SPEC. NO. 58053369 SHEET A 6F REV. A



CABLE ASSEMBLY DRAWING
Figure 1

FIBER CONNECTION DIAGRAM
Figure 2

58034134

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB 001	TAB 002	TAB 003	TAB 004	PL ALL	DWG SH 1
A	LEVEL 1 ISSUE	79	10	01	T Chaille 12/2/79	A	A			A	A
B	PHAØPV083	79	12	13	Noel L. Diaz	B	B			B	B
C	PHAØPS308	80	DEC	09	Jim Richardson	C	C	C	C	C	C
D	PHAOPV313	82	JAN	15	Efren Anaya	D	D	D	D	D	D
E	PHAØPV563	82	DEC	10	B Warash	E	E	E	E	E	E

FCF:

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY 79 JUN 5

APPROVED R. F. Abraham 79/09/20

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CONNECTOR GUIDE

SIZE	REVISION STATUS FOR	SHEET	REV
C	58034134	1/1	E

DIST. C106-2§3

BRUNING 44-141 40366

CE 300 A-3 (1-79)

PD 82/12/11 C 58034134 1/1 E

					001	002	003	004		
	1	A	58052731-001	P CONNECTOR 88 PIN	1	1	1	1		EA
*	2	B	58059668-003	V LABEL	1	1				EA
*	2	B	58059668-001	V LABEL	INTCH	INTCH				EA
	3	C	58034050-001	V CONNECTOR GUIDE	4	4	2	2		EA
	4	A	43A216107P13	V PIN,WIRE WRAP	80	80	40	40		EA
	5	X	58054156-002	A PWB BOND & ETCH	1					EA
	6	C	58051465	D SCH-FE/CABLE ADD BD		X				
	7	X	58051464-001	A PWB BOND & DRILL		1				EA
	8	C	58054157	D SCH FE/CABLE ADP BD	X					
	9	X	58052517-001	A PWB BOND & DRILL			1			EA
	10	D	58052546	D SCHEMATIC			X			
	11	X	58052518-001	A PWB BOND & DRILL				1		EA
	12	D	58052545	D SCHEMATIC				X		
*	13	B	58059668-004	V LABEL			1	1		EA
*	13	B	58059668-002	V LABEL			INTCH	INTCH		EA

CONNECTOR GUIDE

C 58034134 1/1 E

REVISIONS					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE

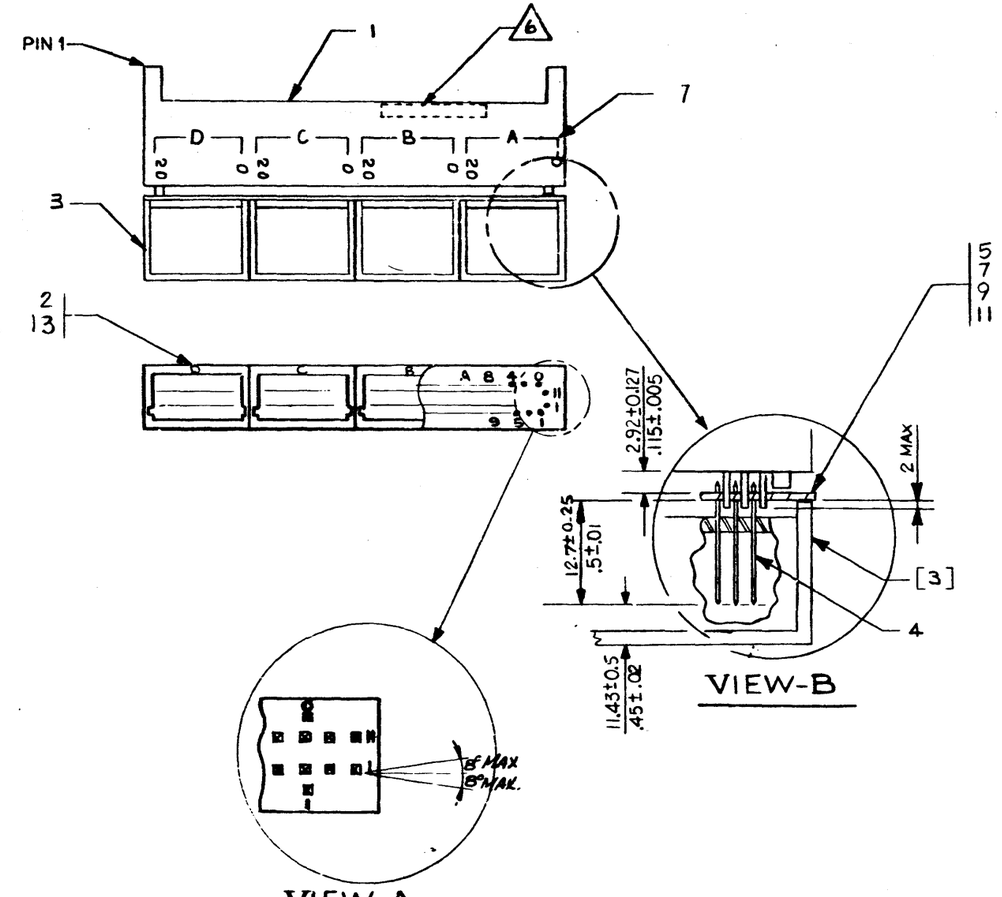


TABLE C

DWG. TAB	P.L. ITEM	LOGIC INTERFACE NAME	ITEM 3 LOCATION (5)
-001	5	MAGNETIC TAPE HANDLER	A,B,C AND D
-002	7	DISC FILE, URC/GENERAL USE	A,B,C AND D
-003	9	MPC TAPE/DISC (PSIA)	B AND C
-004	11	IOM (PSIA)	B AND C

△8. ATTACH MARKER STRIP ORIENTED AS SHOWN.

△7. CONNECTOR PIN NUMBERING FOR REFERENCE ONLY, DO NOT MARK ON ASM.

△6. MFG TO MARK ASM NO., TAB NO. AND REVISION. PER: M50EB00655.

△5. CONNECTOR GUIDE ITEM 3 SHALL BE INSTALLED IN THE LOCATIONS INDICATED IN TABLE C.

4. ASSEMBLE PER 43A226454.

3. BEFORE THE INSTALLATION OF GUIDE ITEM 3:

A. THE TIP OF PIN ITEM 4 SHALL BE WITHIN A RADIUS OF .13 MM OF ITS TRUE HOLE POSITION

B. THE MAXIMUM ITEM 4 PIN ANGULAR ORIENTATION WITH RESPECT TO ITS PIN ROW SHALL BE PER VIEW-A.

2. INSTALL PWB ITEM 5 ORIENTED AS SHOWN.

1. ITEMS SHOULD BE ASSEMBLED IN THE FOLLOWING ORDER:
A. STAKE PINS ITEM 4 INTO P.W.B. ITEM 5 AND SOLDER.

B. PLACE THE PINNED PWB OVER THE PINS OF ITEM 1 & SOLDER PARTS TOGETHER

C. PRESS ITEM 3 OVER THE SOLDERED PINS SO ITEM 3 BUTTS AGAINST THE SURFACE OF PWB ITEM 5.

NOTES:

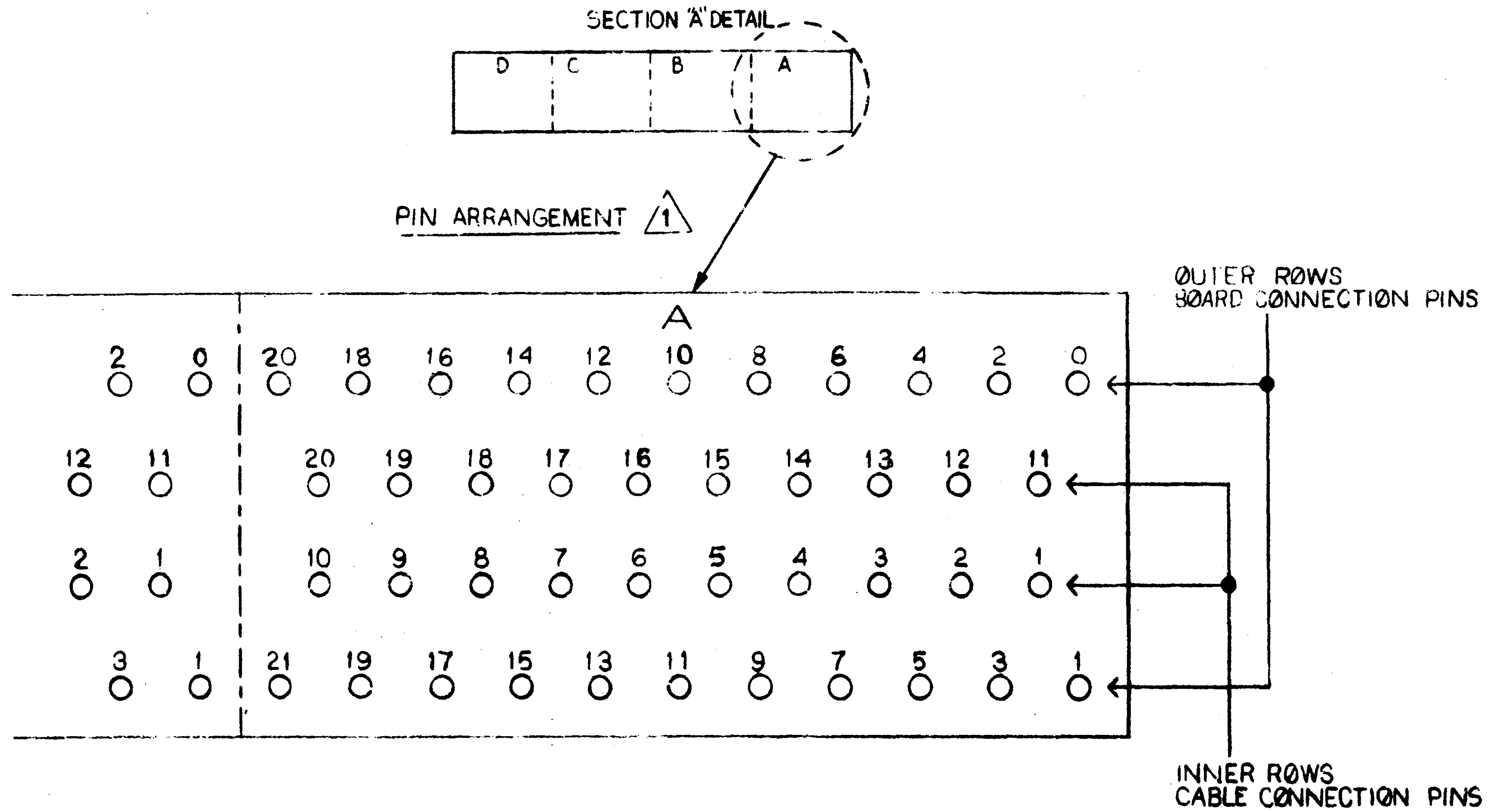
58034134

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

43A226454	
M50EB00655	
58008590	
REF SPEC NO	

UNLESS OTHERWISE SPECIFIED	MATL	Honeywell	
DIMENSIONS= MILLIMETERS / INCHES		HONEYWELL INFORMATION SYSTEMS	
TOLERANCE OF SIZE AND FORM PER	DES. T. Chandler 11/1/79	LOC PHOENIX, ARIZONA U. S. A.	
INITIAL DESIGN M	CHKR R. Hall 11/1/79	TITLE CONNECTOR GUIDE	
PROJECTION	FIN.		
SCALE 1/1 CODE	DR T. Miller 79 JUN 5	SIZE C	DWG NO 58034134 SH 1/1 REV E
T. Chandler 11/1/79	APPD R. G. Abraham 79/06/20	CISTR C106-3, C107-3	

REVISIONS					
REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE
A	LEVEL 3 ISSUE	79	07	05	[signature]
B	PHAØPV313	82	JAN	15	[signature]



PIN CØNNECTIØN LIST (note 1)

PIN NØ. ØUTER RØWS	PIN NØ. INNER RØWS
0	20
1	9
3	10
4	7
6	6
7	18
9	4
10	17
12	15
13	3
15	1
16	14
18	12
19	11
2	2
5	5
8	8
11	13
14	16
17	19
20	

2. REFERENCE ONLY: SCHEMATIC MADE FROM WIRE LISTS, 43A229856 MTC 500 DLI CABLE, 43A243630 MPCMX CABLE 43A229761 DLI CABLE & 58018104 LSMX CABLE.

1. SECTIØNS A, B, C & D HAVE THE SAME PIN INTERCØNNECTIØN & ARRANGEMENTS.

NØTES:

43A229856
43A243630
43A229761
58018104
REF SPEC NO

UNLESS OTHERWISE SPECIFIED DIMENSIONS = MILLIMETERS / INCHES; TOLERANCE OF SIZE AND FORM PER ____; INITIAL DESIGN; PROJECTION	MATL	Honeywell HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U.S.A.
	TREAT.	TITLE SCHEMATIC DIAGRAM FE/CABLE ADP BD
	FIN	
SCALE / CODE	DR [signature] 26 July 79	SIZE C / DWG NO 58051465 / SH 1/1 / REV B
[signature] 79 09 28	APPD [signature] 9/09/..	
	DISTR C106-10	

0 10 20 30 40 50 60 70 80 MM
0 1 2 3 IN

THE INFORMATION CONTAINED IN THIS DOCUMENT IS PROPRIETARY TO HONEYWELL INFORMATION SYSTEMS AND IS INTENDED FOR INTERNAL HONEYWELL USE ONLY. SUCH INFORMATION MAY BE DISTRIBUTED TO OTHERS ONLY BY WRITTEN PERMISSION OF AN AUTHORIZED HONEYWELL OFFICIAL. THIS RESTRICTION DOES NOT APPLY TO VENDOR PROPRIETARY PARTS THAT MAY BE DISCLOSED IN THIS DOCUMENT

58051465

OPTION CONTENTS
UNIT RECORD CONTROLLER
PROM B OPTION

NOTE

This option consists of a functional PWA, a PROM kit, and interface cables to connect and operate unit record devices (see common Installation Instructions 58058443 for supported unit record devices).

PARTS

Installation Kit	58081721
Installation Instructions	58059261
Functional PWA	58081254
FW Accumulation Kit	58059263
FW Installation Instructions	58081255
FW CIL	58059264

(a) Insert this option package under TAB 2 only when called for on the Equipment Requisition.
(b) Common documents are located under Table of Contents Tab -530.

5B081721

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE	TAB NO 001	PL ALL
A	LEVEL 3 ISSUE	83	12	01	Dayne Taylor	A	A
B	PHASDP053	84	02	02	J Brentle	B	B

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY G.M. Blaster 83 at 25

APPROVED J. Dale 83 Nov 18

TITLE INSTL KIT PROM B WEUROOZA

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

SIZE	REVISION STATUS FOR	SHEET	REV
X	58081721	1/1	B

DIST. C111-7B

BRUNING 44-141 40366

CE 300 A-3 (1-79)

PD 84/02/02 X 58081721 1/2 B

001

	1	A	58059261	D INS INST PROM B	X		
	2	A	58058443	D INSTL INSTR EURC	X		
	3	A	58060011-500	A IPL CABLE SELECT	1		EA
	4	X	58081254-001	A FUNC PWA EURCB-B	1		EA
	5	A	58081723-500	A IPL CONN GUIDE SEL	1		EA
	6	A	43A230400P2	V PROD IDEN PLATE	1		EA
*	7	A	58058506-069	P PROD IDENT NP	X		EA
	8	B	438219963P183	P MARKER CHAR EUR	1		EA
	9	B	438219963P217	P MARKER CHARACTER	1		EA
	10	A	58059262-001	D DOCUMENT LIST	1		EA
	11	B	877B222P07	V CLAMP CBL NYLON	6		EA
	12	A	58073400-410	V SCREW,MACH.THD.RPH,S	4		EA
	13	A	58073425-108	V WASHER PLAIN,STL.	4		EA
	14	A	58073429-038	V LOCK WASH.,SPG.,STL.	4		EA
	15	A	58073423-015	V NUT,STL.MACH.SCREW	4		EA
	16	A	58034809-017	V LABEL	1		EA

INSTL KIT PROM B

X 58081721 1/2 B

PD 84/02/02 X 58081721 2/F B

001

	17	A	58034809-016	V LABEL	1	EA
	18	A	58034809-015	V LABEL	1	EA
	19	A	58034809-014	V LABEL	1	EA
	20	A	58057326-024	V LABEL	1	EA
*	23	B	438219963P2	P MARKER CHAR B	1	EA

INSTL KIT PROM B

X 58081721 2/F B

Honeywell HONEYWELL INFORMATION SYSTEMS		DWG. NO. 58059261	SHEET 1/3	REV E
LOC. PHOENIX, ARIZONA	DISTR C111-7B	PROJECTION	CODE	
	DATA BASE T059261 D059261			
PREPARED BY DATE Ted Bullard 81JUL9	TITLE		F.C.F.: 58059260 OP.LST: N/A	
APPROVED BY C. WILCOX 81JUL 9	INSTALLATION INSTRUCTION PROM B OPTION			

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	LEVEL 3 ISSUE	81JUL9	SEE APERTURE CARD	RSS, 1 THRU 5F
B	PHA0DP010	81SEP23	S.STEELE	ALL
C	PHA0DP016	82JAN27	S.STEELE	1 THRU 5F
D	PHA0DP043	83NOV04	J. KNOBLACH	1 THRU 3F REVISED/RETYPED
E	PHA0DP053	84JAN09	N. BEHIE	1 THRU 3F

I. SCOPE:

THIS INSTRUCTION PROVIDES THE INFORMATION NECESSARY IN THE INSTALLATION OF WEUR002A AND WILL SUPPORT TWO PRINTERS. COMBINATIONS ARE TWO PDSI, TWO DAI OR ONE PDSI AND ONE DAI. THIS INSTRUCTION ALONG WITH THE COMMON INSTALLATION INSTRUCTION 58058443 (ITEM 2) WILL PROVIDE THE COMPLETE INSTALLATION OF A EURC PROM B OPTION.

THE SUPPORTED DEVICES ARE:

1) PRU1200 DAI PRINTER
2) PRU1600 DAI PRINTER
3) PRU0901 PDSI PRINTER
4) PRU1201 PDSI PRINTER

I. PREPARATION PROCEDURE:

1. TURN POWER OFF AT CABINET.

II. INSTALLATION INSTRUCTION:

1. REFER TO INSTALLATION KIT NUMBER 58081721 FOR ITEM NUMBERS REFERENCED IN THE FOLLOWING INSTRUCTIONS.

2. INSTALL CONNECTOR GUIDE, ITEM 5, TO THE EURCB-B BOARD. INSTALL EURCB-B BOARD IN THE BOARD SLOT ALLOCATED AND CONNECT THE HARNESSES. REFER TO 58058443 FOR GENERAL APPLICATIONS.

3. TURN POWER ON. CHECK THAT THE GREEN LED INDICATOR, LOCATED AT THE LEFT EDGE OF THE EURCB BOARD, IS ON. THIS VERIFIES THAT THE EURCB BOARD HAS PERFORMED A SELF TEST WITH NO ERROR CONDITIONS WHEN POWERED ON.

4. ATTACH THE PRODUCT IDENTIFICATION NAME PLATE (ITEM 6/7) TO THE UPPER RIGHT HAND CORNER OF THE JUNCTION PANEL FOR HIGH PROFILE CABINETS AND TO THE FRONT FACE OF THE AIR PLENUM FOR LOW PROFILE CABINETS.

IV. OPTION REMOVAL PROCEDURE:

1. THE REMOVAL OF THIS OPTION REQUIRES ONLY THE REVERSE PROCEDURE OF THE INSTALLATION.

V. PARTS DISPOSITION:

1. RETURN THE PARTS REMOVED IN THE ABOVE STEPS TO "LCPD" MANUFACTURING.

RETURN TO:

HONEYWELL INFORMATION SYSTEMS
P.O. BOX 8000
PHOENIX, ARIZONA 85066

C/O MGR LCPD WAREHOUSE
MAIL DROP J-2

58081254

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO. 001	PL ALL
A	LEVEL 1 ISSUE	83	NOV	30	Dayne Taylor	A	A

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44-141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

CE 300 A-3 (1-79)

MADE BY C. Ripley 83-6-8

APPROVED J. P. Abel 83 Nov 18

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

DIST. C111-7

TITLE: FUNCT PWA EURCB-B

SIZE	REVISION STATUS FOR	SHEET	REV
X	58081254	1/1	A

PD 83/11/30 X 58081254 1/1 A

							001		
*	1	X	58065900-010	A	HDUHC	PWA EURCB	1		EA
*	1	X	58065900-110	A	HDUHC	PWA EURCB	INTCH		EA
*	1	X	58065900-210	A	HDUHC	PWA EURCB	INTCH		EA
*	1	X	58065900-610	A	HDUHC	PWA EURCB	INTCH		EA
*	1	X	58065900-710	A	HDUHC	PWA EURCB	INTCH		EA
*	1	X	58065900-910	A	HDUHC	PWA EURCB	INTCH		EA
*	2	A	58081255	D	INSTL	INSTR EURCB-B	X		EA
*	3	X	58059263-006	A	ACCUM	KIT	1		EA
*	4	A	58060578-019	P	ID	LABEL F/W	1		EA

FUNC PWA EURCB-B

X 58081254 1/1 A

58059263

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE	TAB NO. 001	002	003	004	005	006	PL ALL
A	LEVEL-1-ISSUE	81	08	06	G.Kelly 7/31/81	A						A
B	PHAØDP016	82	02	09	S. J. Steele	B	B					B
C	PHAØDP019	82	03	10	S.J. Steele		C	C				C
D	PHAØDP026	82	07	16	S. Miller			D	D			D
E	PHAØDP033	83	JAN	19	S Brenth	OBSOLETE	OBSOLETE	OBSOLETE	E	E		E
F	PHAØGD525		NO		T. Accongi				OBSOLETE	F		F
G	PHAØDP043	83	NOV	30	T Accongi				OBSOLETE	G	G	G

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY Ted Gingras 81, JULY, 7

APPROVED C. E. Wilcox 7/20/81

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

DIST. C111-6

TITLE E-PROM ACCUM KIT

SIZE	REVISION STATUS FOR	SHEET	REV
X	58059263	1/1	G

BRUNING 44-141 40366

CE 300 A-3 (1-79)

PD 83/11/30 X 58059263 1/1 G

006

*	3	A	58002689-086	V UV 32K EPROM	1	EA
*	4	A	58002689-087	V UV 32K EPROM	1	EA
*	5	A	58002689-088	V UV 32K EPROM	1	EA
*	6	A	58002689-094	V UV 32K EPROM	1	EA
*	7	A	58002689-095	V UV 32K EPROM	1	EA
*	8	A	58002689-085	V UV 32K EPROM	1	EA
*	9	A	58002689-093	V UV 32K EPROM	1	EA
*	10	A	58059264-006	D COMP INSTL LIST	X	
*	11	A	58002689-089	V UV 32K EPROM	1	EA
*	12	A	58002689-090	V UV 32K EPROM	1	EA
*	13	A	58060578-001	P ID LABEL FUNCT PWA	1	EA
*	14	A	58060578-002	P ID LABEL FUNCT PWA	1	EA

ACCUM KIT

X 58059263 1/1 G

Honeywell HONEYWELL INFORMATION SYSTEMS		DWG. NO. 58081255	SHEET 1/3	REV. A
LOC. PHOENIX, ARIZONA	DISTR C111-7B DATA BASE T081255 D081255	PROJECTION	CODE	
PREPARED BY DATE 83NOV04	TITLE INSTALLATION INSTRUCTION EURCB-B EPROM FW KIT(S)		F.C.F.: 58081254 OP.LST: N/A	
APPROVED BY D. DUANE 83NOV04				

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	LEVEL 3 ISSUE	83NOV04	SEE APERTURE CARD	1 THRU 3F

I. SCOPE:

THIS INSTRUCTION PROVIDES THE INFORMATION NECESSARY IN THE INSTALLATION OF EPROMS ON THE EURCB-B BOARD.

II. INSTALLATION PROCEDURE

1. FUNCTIONAL PWA EURCB-B

1.1. REFER TO THE FUNCTIONAL PWA ASSEMBLY 58081254 PL FOR THE ITEM NUMBERS REFERENCED IN THE FOLLOWING INSTRUCTIONS UNLESS OTHERWISE SPECIFIED.

1.2. REFER TO FIGURE 1 FOR APPROXIMATE LOCATION AND IDENTITY OF ITEMS REFERRED TO IN INSTRUCTION STEPS THAT FOLLOW.

1.3. PLUG-IN THE PROGRAMMED EPROMS ON THE EURCB-B BOARD IN SOCKET LOCATIONS LISTED IN COMPONENT INSTALLATION LIST, 58059264, CALLED FOR ON ACCUMULATION KIT 58059263. USE CARE IN HANDLING AND INSTALLING THE EPROMS BY AVOIDING ANY STATIC CHARGE BUILD-UP ON THE BODY OF THE HANDLER OR PERSON.

1.4. INSTALL THE FUNCTIONAL BOARD ASM LABEL ITEM 4 ON BOARD AS SHOWN IN FIGURE 1.

1.5. INSTALL THE APPROPRIATE TAB NUMBER AND REVISION LABELS TO THE FUNCTIONAL BOARD IDENTIFICATION NUMBER USING ITEMS 13 AND 14 PROVIDED IN THE FIRMWARE ACCUMULATION KIT, 58059263. (EXAMPLE: "001 A" AS INITIALLY ISSUED)

III. REMOVAL PROCEDURE FOR BASIC OR OPTION PLUGGABLE EPROM KIT(S):

1. FOLLOW THE REVERSE PROCEDURE AND PRECAUTIONS OF THE INSTALLATION.

IV. PARTS DISPOSITION:

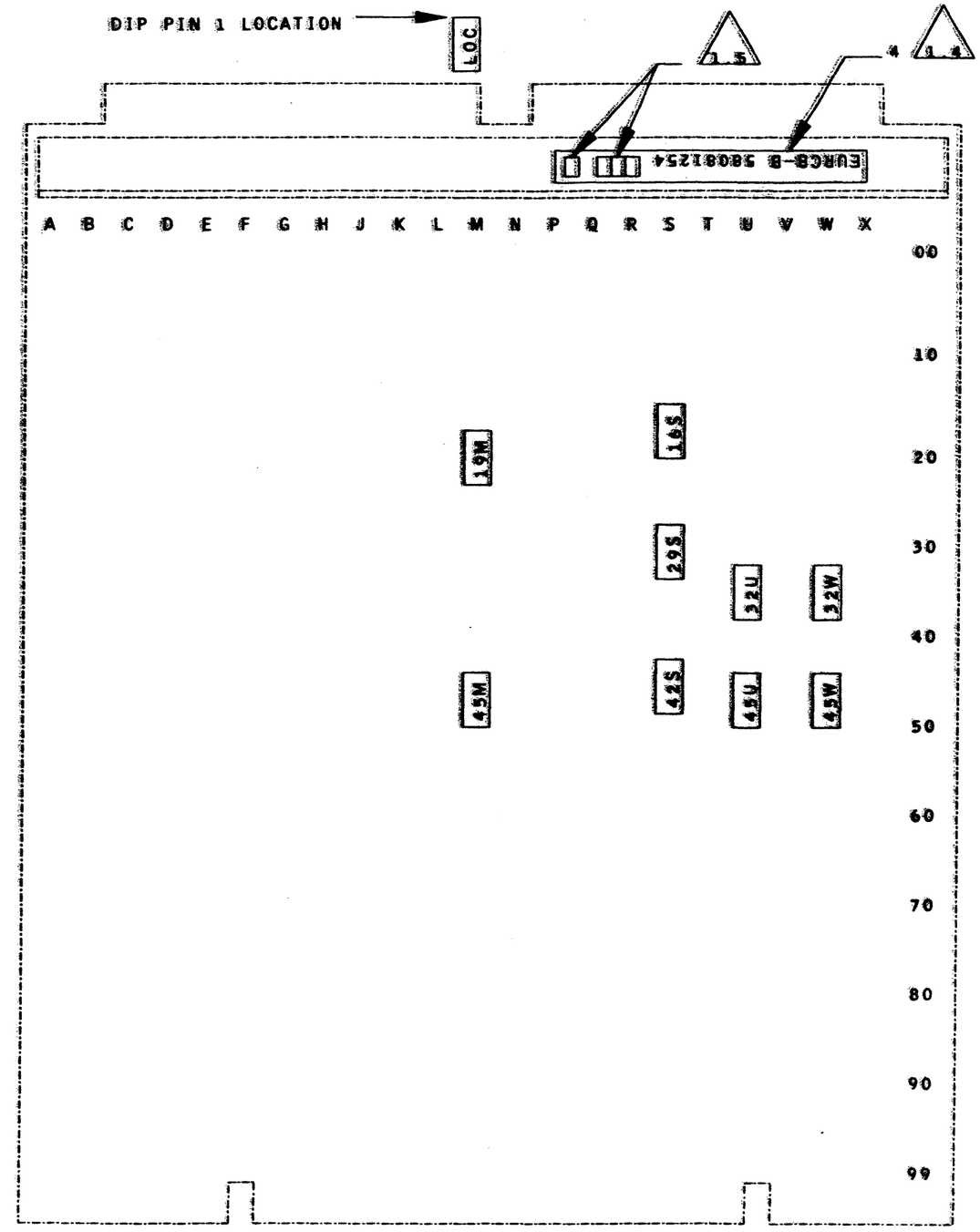
1. RETURN THE PARTS REMOVED IN THE STEP III ABOVE TO "LCPD" MANUFACTURING.

ADDRESS::

HONEYWELL INFORMATION SYSTEMS
P.O. BOX 8000
PHOENIX, ARIZONA 85066

C/O MGR LCPD WAREHOUSE
MAIL DROP J-2

Honeywell HONEYWELL INFORMATION SYSTEMS	INSTALLATION INSTRUCTION	DWG. NO. 58081255	SHEET 3F	REV A



FIGURE

58059264

REV	AUTHORITY	DATE YR	MO	DAY	SIGNATURE	TAB NO. 001	002	003	004	005	006	DWG. SH. 1	2
A	LEVEL 3 ISSUE	81	08	04	J Kelly 7/31/81	A						A	
B	PHAØDP016	82	02	09	D.J. Staab	B	B					B	
C	PHAØDP019	82	03	10	D.J. Staab	OBSOLETE	C	C				C	C
D	PHAØDP026	82	07	16	L. Miller	OBSOLETE	OBSOLETE	D	D				D
E	PHAØDP033	83	JAN	19	G Brenth	OBSOLETE	OBSOLETE	OBSOLETE	E	E		E	E
F	PHAØDP043	83	NOV	30	T Jorgensen	OBSOLETE	OBSOLETE	OBSOLETE	OBSOLETE	F	F	F	DELETED

FOR CONTINUATION OF REVISION STATUS SEE SHEET

BRUNING 44 141 40366

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY Ted Jorgensen 7/31/81

APPROVED C. E. Wilcox 7/20/81

TITLE COMP INSTL. LIST

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

SIZE	REVISION STATUS FOR	SHEET	REV
A	58059264	1/1	F

DIST. C111-9

CE 300 A-3 (1-79)

TAB-005 OBSOLETE

TAB-006

COMPONENT INSTALLATION FOR WEUR002A

LOCATION	TYPE	IDENT
45W	2R3689	58002689-085
32W	2R3689	58002689-086
45U	2R3689	58002689-087
32U	2R3689	58002689-088
42S	2R3689	58002689-089
29S	2R3689	58002689-090
16S	2R3689	58002689-094
19M	2R3689	58002689-095
45M	2R3689	58002689-093

OPTION CONTENTS
UNIT RECORD CONTROLLER
INITIALIZE OPTION

NOTE

This option consists of a connector with a pushbutton switch which can be used to initialize the URC. The PDSI cable 58056843 must be installed to use this option. This option is for restricted use by Honeywell customers.

PARTS

Installation Kit.....58059797
Installation Instructions.....58059798
Initialize Connector.....58059452 & PL

(a) Insert this option package under TAB 3 only when called for on the Equipment Requisition.
(b) Common documents are located under Table of Contents Tab -530.

58059797

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO. 001	PL ALL
A	LEVEL ISSUE	82	JAN	15	J W Bogle 1-6-82	A	A
B	PHASE DP242	83	NOV	30	H Drew III	B	B

CUSTOM PRODUCT
FOR LIMITED FABRICATION ONLY
ENGRG C.E. Wilcox 12/24/81
MFG [illegible] 1/5/82
APPROVAL
TP-1011

FCF: WEUR005A

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY S.J. Steele 81-DEC-11

APPROVED

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE INSTL. KIT EURC INITIALIZE

SIZE	REVISION STATUS FOR	SHEET	REV
X	58059797	1/1	B

DIST. C107-C127, 7

BRUNING 44-141 40366

CE 300 A-3 (1-79)

PD 83/11/30 X 58059797 1/1 B

001

	1	A	58059798	D INSTL INSTR INIT OPT	X		
	2	A	58059799-001	D DOCUMENT LIST	1		
	3	C	58059452-001	A CONNECTOR INIT	1		EA
	4	A	58057326-036	V LABEL	1		EA
*	5	A	43A230400P2	V PROD IDEN PLATE	1		EA
*	6	A	58058506-105	P PROD IDENT NP	X		EA

INSTL KIT EURC INIT

X 58059797 1/1 B

Honeywell HONEYWELL INFORMATION SYSTEMS		DWG. NO. 58059798	SHEET 1/7	REV C
LOC. PHOENIX, ARIZONA	DISTR C111-7B DATA BASE T059798 D059798	PROJECTION	CODE	
PREPARED BY DATE S.J. Steele 81DEC10 APPROVED BY C. WILCOX 81DEC10	TITLE INSTALLATION INSTRUCTION EURC INITIALIZE OPTION		F.C.F.: 58059797 OP.LST: N/A	

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	LEVEL 3 ISSUE	81DEC10	SEE APERTURE CARD	1 THRU 8F
B	PHA0DP042	83NOV04	J. KNOBLACH	1 THRU 8F
C	PHA0DP053	84JAN09	N. BEHIE	1 THRU 7F

I. SCOPE:

THIS INSTRUCTION PROVIDES THE INFORMATION NECESSARY FOR INSTALLING THE EURC INITIALIZE OPTION (WEUR005A) INTO THE PDSI CONNECTOR.

II. INSTALLATION PROCEDURE

1. REFER TO INSTALLATION KIT NUMBER 58059797 FOR ITEM NUMBERS REFERENCED IN THE FOLLOWING INSTRUCTIONS.

2. REFER TO FIGURES FOR APPROXIMATE LOCATION AND IDENTITY OF ITEMS REFERRED TO WITHIN THE FOLLOWING INSTALLATION INSTRUCTIONS.

3. INSTALL CONNECTOR ITEM 3 IN SLOT "A" OF THE PDSI CONNECTOR SEE FIGURE 1.

4. SECURE LABEL ITEM 4 TO THE TOP SIDE OF THE CONNECTOR SEE FIGURE 1.

5. ATTACH THE PRODUCT IDENT NAME PLATE ITEM 6/7 TO THE UPPER RIGHT CORNER OF THE JUNCTION PANEL ON THE IOM. SEE FIGURES 2, 3, 4, & 5 FOR THE APPROPRIATE UNIT IN WHICH THE EURCB BOARD IS INSTALLED, OR WILL BE INSTALLED.

III. OPTION REMOVAL PROCEDURE:

1. THE REMOVAL OF THESE OPTIONS REQUIRES ONLY THE REVERSE PROCEDURE OF THE INSTALLATION.

IV. PARTS DISPOSITION:

1. RETURN THE PARTS REMOVED IN THE ABOVE STEPS TO "LCPD" MANUFACTURING.

RETURN TO:

HONEYWELL INFORMATION SYSTEMS
P.O. BOX 8000
PHOENIX, ARIZONA 85066

C/O MRG LCPD WAREHOUSE
MAIL DROP J-2

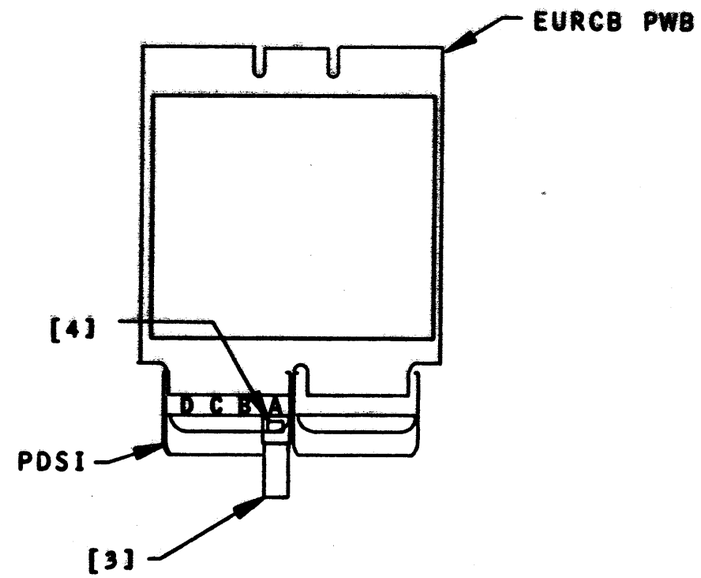
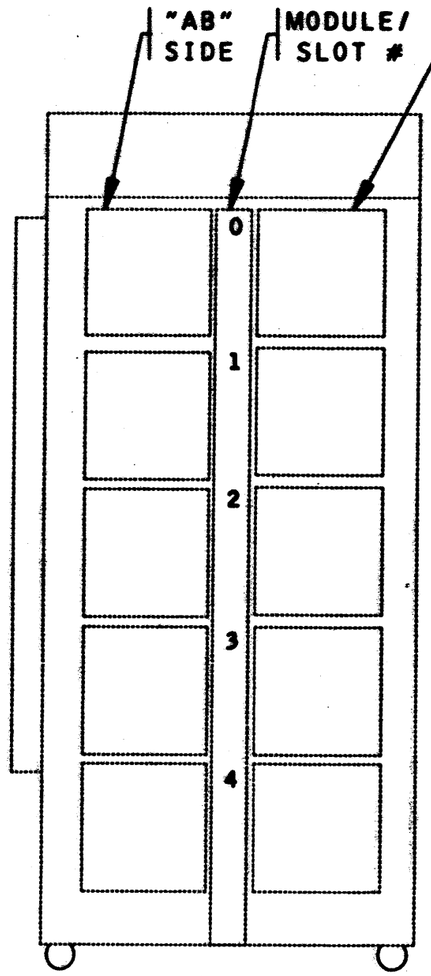


FIGURE 1



IOM

FRONT VIEW
(CIRCUIT BOARD SIDE)
EXTERNAL DOORS REMOVED

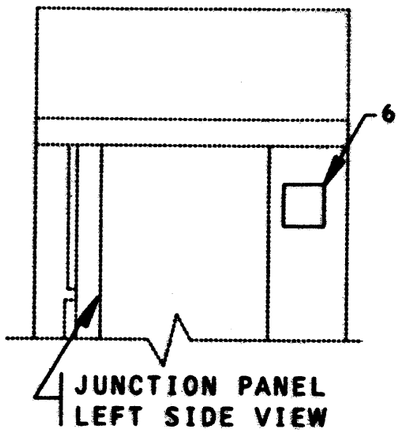
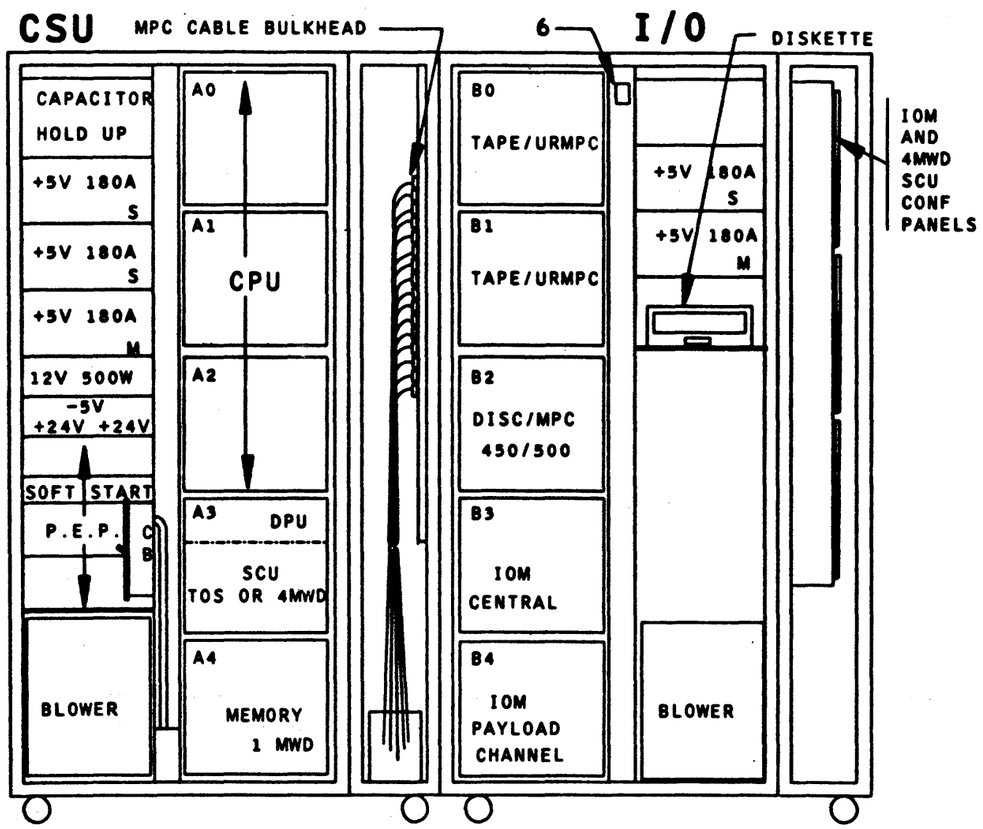
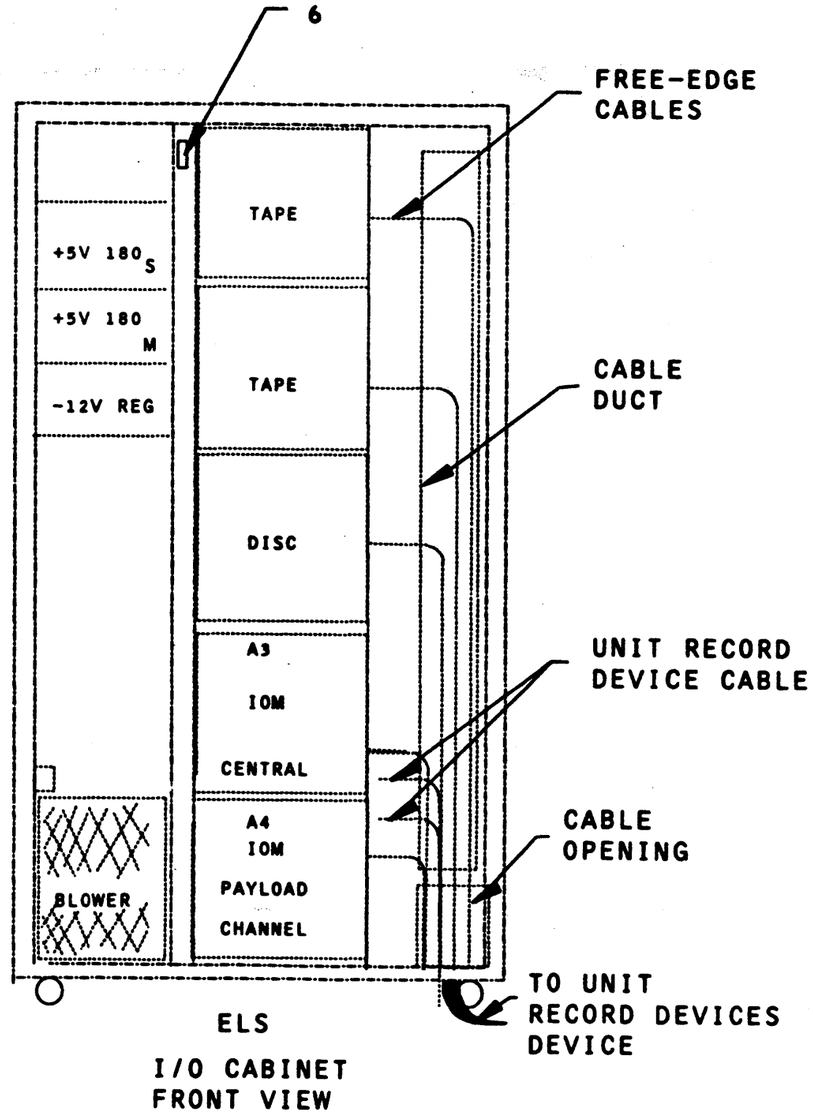


FIGURE 2



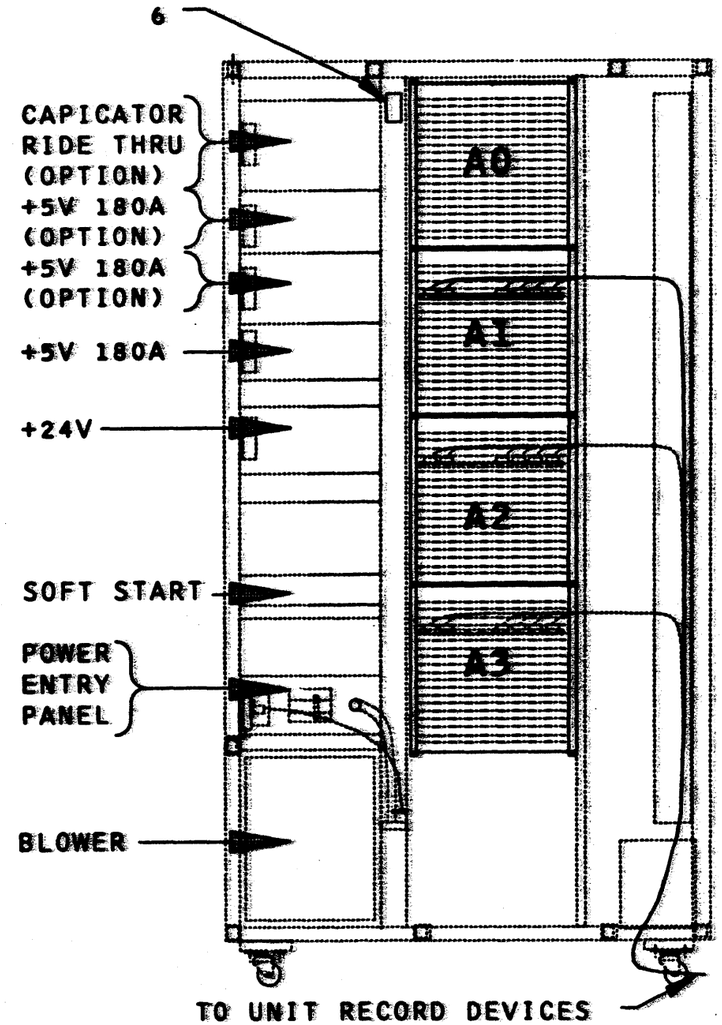
ELS-1 FRONT VIEW

FIGURE 3



ELS
I/O CABINET
FRONT VIEW

FIGURE 4



IOM
FRONT VIEW

FIGURE 5

58059452

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE
A	LEVEL 3 ISSUE	82	JAN	15	J.M. Boyle 1-6-82
B	PHA@ DP030	82	NOV	04	L. Miller

ASM TAB 001	PL ALL	DWG SH 1
A	A	A
B	B	B

CUSTOM PRODUCT
FOR LIMITED FABRICATION ONLY

ENGRG C.E. Wilson 12/31/81
MFG [illegible] 1/5/82
APPROVAL
MP-1011

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.
LOC PHOENIX ARIZONA

MADE BY S.J. Stitle 81-SEP-17
APPROVED
REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE CONNECTOR INIT.

SIZE	REVISION STATUS FOR	SHEET	REV
C	58059452	1/1	B

DIST. C84-31.34

BRUNING 44-141 40366
CE 300 A-3 (1-79)

PD 82/11/05 C 58059452 1/1 B

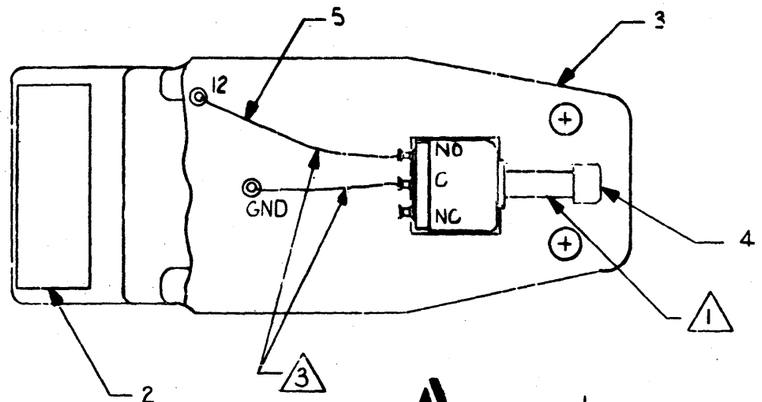
001

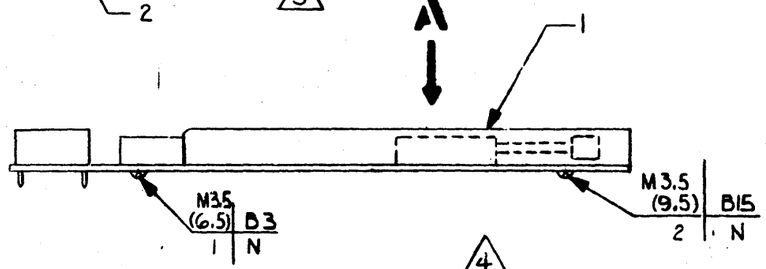
1 C	58034066-001	V PADDLE BD COVER	1	EA
2 A	58000038-008	V CONNECTOR, PWB	1	EA
3 B	58059451-001	A PADDLE BOARD ASM	1	EA
4 A	58000053-001	P SWITCH,PUSH-MOM	1	EA
5 A	43A167218P029	V WIRE	6	IN

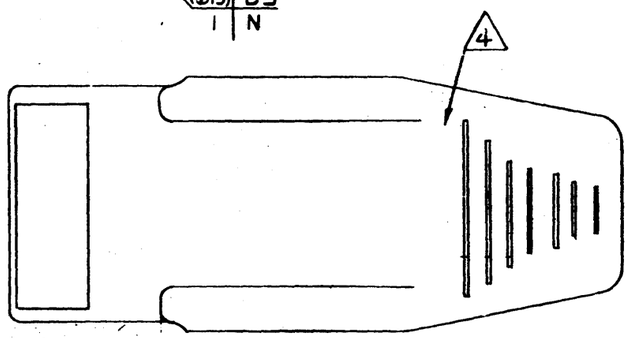
CONNECTOR INIT

C 58059452 1/1 B

REVISIONS			
REV	AUTHORITY	DATE YR MO DA	SIGNATURE







VIEW A

(001)

△ 4. MARK PER 43A226458 CLASS B

△ 3. SOLDER PER 43A226454.

△ 2. POSITION LABEL ITEM 16 AS SHOWN.

△ 1. REMOVE HARDWARE AND DISPOSE OF PRIOR TO ASSEMBLY.

NOTES:

58059452

FOR DOCUMENT STATUS, SEE REVISION STATUS SHEET

UNLESS OTHERWISE SPECIFIED DIMENSIONS= MILLIMETERS / INCHES TOLERANCE OF SIZE AND FORM PER INITIAL DESIGN M PROJECTION	MATL TREAT: CHK & K Noble 81 NOV 16 FIN. DR S.J. Stelle 81-SEP-17 APPD DISTR C84-34	Honeywell HONEYWELL INFORMATION SYSTEMS LOC PHOENIX, ARIZONA U. S. A. TITLE CONNECTOR INIT. FCF; 58058442 SIZE C · DWG NO 58059452 · SH 1/1 · REV B
SCALE · CODE		

43A226454
REF SPEC NO

CUSTOM PRODUCT
FOR LIMITED FABRICATION ONLY

BRUNING 44 141 2304 13
CE 300 C (12 71)

0 10 20 30 40 50 60 70 80 MM
0 1 2 3 IN

OPTION CONTENTS
UNIT RECORD CONTROLLER
PROM D OPTION

NOTE

This option consists of a functional PWA, a PROM kit, and interface cables to connect and operate unit record devices (see common Installation Instructions 58058443 for supported unit record devices).

PARTS

Installation Kit	58082265
Installation Instructions	58082266
Functional PWA	58082267
FW Accumulation Kit	58082269
FW Installation Instructions	58082268
FW CIL	58082270

(a) Insert this option package under TAB 5 only when called for on the Equipment Requisition.
(b) Common documents are located under Table of Contents Tab -530.

58082265

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	PL ALL
A	LEVEL 2 ISSUE	84	09	18	Allen Poole	A	A

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY D. M. D'Agostino 84/8/31

APPROVED R. Dionne 84/8/16

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE: INSTL KIT, PROM-D OPT.

SIZE	REVISION STATUS FOR	SHEET	REV
X	58082265	V1	A

DIST. 3

BRUNING 44-141 40366

CE 300 A-3 (1-79)

001

•	1	A	58082266	D INSTL INSTR PROM D	X		
•	2	A	58058443	D INSTL INSTR EURC	X		
•	3	A	58060011-500	A IPL CABLE SELECT	1		EA
•	4	X	58082267-001	A FUNCT PWA EURCB-D	1		EA
•	5	A	58081723-500	A IPL CONN GUIDE SEL	1		EA
•	6	A	43A230400P2	W PROD IDEN PLATE	1		EA
•	7	A	58081600-057	P PROD IDENT NP	X		EA
•	8	B	43B219963P183	P MARKER CHAR EUR	1		EA
•	9	B	43B219963P217	P MARKER CHARACTER	1		EA
•	10	A	58082271-001	D DOC LIST EURCB-D	1		EA
•	11	B	877B222P07	W CLAMP CBL NYLON	6		EA
•	12	A	58073400-410	V SCREW,MACH.THD.RPH,S	4		EA
•	13	A	58073425-108	V WASHER PLAIN,STL.	4		EA
•	14	A	58073429-038	V LOCK WASH.,SPG.,STL.	4		EA
•	15	A	58073423-015	V NUT,STL.MACH.SCREW	4		EA
•	16	A	58034809-017	W LABEL	1		EA

INSTL KIT PROM D

PD 84/09/18 X 58082265 2/F A

001

*	17 A	58034809-016	W LABEL	1		EA
*	18 A	58034809-015	W LABEL	1		EA
*	19 A	58034809-014	W LABEL	1		EA
*	20 A	58057326-024	W LABEL	1		EA
*	23 B	438219963P4	P MARKER CHAR D	1		EA

INSTL KIT PROM D

X 58082265 2/F A

Honeywell HONEYWELL INFORMATION SYSTEMS		DWG. NO. 58082266	SHEET 1/2	REV. A
LOC. PHOENIX, ARIZONA	DISTR -7B	PROJECTION	CODE	
	DATA BASE T082266 D082266			
PREPARED BY DATE Nancy Behie 84JUL31	TITLE INSTALLATION INSTRUCTION PROM D OPTION		F.C.F.: 58082265 OP.LST: N/A	
APPROVED BY T. FINCH 84JUL31				

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	LEVEL 3 ISSUE	84JUL31	SEE APERTURE CARD	RSS, 1 THRU 2F

I. SCOPE:

THIS INSTRUCTION PROVIDES THE INFORMATION NECESSARY IN THE INSTALLATION OF THE WEUR007A AND WILL SUPPORT DAI CARD DEVICES AND/OR THE PDSI PRINTING DEVICES. THIS INSTRUCTION ALONG WITH THE COMMON INSTALLATION INSTRUCTION 58058443 (ITEM 2) WILL PROVIDE THE COMPLETE INSTALLATION OF THE EURC PROM D OPTION. THE SUPPORTED DEVICES ARE:

1) PR54 PRINTER PDSI
2) CRU1050 CARD READER DAI
3) CRU0501 CARD READER DIA
4) PCU0120 CARD PUNCH DAI
5) PCU0121 CARD PUNCH DAI
6) CCU0401 CARD READER/PUNCH DAI

II. PREPARATION PROCEDURE:

1. TURN OFF ALL POWER TO THE CABINET.

III. INSTALLATION INSTRUCTION:

1. REFER TO INSTALLATION KIT NUMBER 58082265 FOR ITEM NUMBERS REFERENCED IN THE FOLLOWING INSTRUCTIONS.

2. INSTALL CONNECTOR GUIDE, ITEM 5, TO THE EURCB-D BOARD. INSTALL EURCB-D BOARD IN THE BOARD SLOT ALLOCATED AND CONNECT THE HARNESSES. REFER TO 58058443 FOR GENERAL APPLICATIONS.

3. TURN POWER ON. MAKE SURE THE GREEN LED INDICATOR LOCATED AT THE LEFT EDGE OF THE EURCB BOARD, IS ON. THIS VERIFIES THAT THE EURCB BOARD HAS PERFORMED A SELF TEST WITH NO ERROR CONDITIONS WHEN POWERED ON.

4. ATTACH THE PRODUCT IDENTIFICATION NAMEPLATE (ITEM 6/7) TO THE UPPER RIGHT HAND CORNER OF THE JUNCTION PANEL FOR HIGH PROFILE CABINETS AND TO THE FRONT FACE OF THE AIR PLENUM FOR LOW PROFILE CABINETS.

IV. OPTION REMOVAL PROCEDURE:

1. THE REMOVAL OF THIS OPTION REQUIRES ONLY THE REVERSE PROCEDURE OF THE INSTALLATION.

V. PARTS DISPOSITION:

1. RETURN THE PARTS REMOVED IN THE ABOVE STEPS TO "LCPD" MANUFACTURING.

RETURN TO:

HONEYWELL INFORMATION SYSTEMS
P.O. BOX 8000
PHOENIX, ARIZONA 85066

C/O MGR LCPD WAREHOUSE
MAIL DROP J-2

58082267

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	PL ALL
A	LEVEL 2 ISSUE	84	09	18		A	A

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY [illegible] 84 July 31

APPROVED R. Duane 84-8-16

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

TITLE FUNCT PWA EURCB-D

SIZE	REVISION STATUS FOR	SHEET	REV
X	58082267	1/1	A

DIST. 3

BRUNING 44-141 40366

CE 300 A-3 (1-79)

PD 84/09/18 X 58082267 1/1 A

				001		
*	1 X	58065900-010	A HDUHC PWA EURCB	1		EA
*	1 X	58065900-110	A HDUHC PWA EURCB	INTCH		EA
*	1 X	58065900-210	A HDUHC PWA EURCB	INTCH		EA
*	1 X	58065900-610	A HDUHC PWA EURCB	INTCH		EA
*	1 X	58065900-710	A HDUHC PWA EURCB	INTCH		EA
*	1 X	58065900-910	A HDUHC PWA EURCB	INTCH		EA
*	2 A	58082268	D INSTL INSTR EURCB-D	X		
*	3 X	58082269-001	A FW ACUM KIT EURCB-D	1		EA
*	4 A	58060578-043	P ID LABEL F/W FUNC	1		EA

FUNCT PWA EURCB-D

X 58082267 1/1 A

58082269

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	PL ALL
A	LEVEL 2 ISSUE	84	09	24	A.E.Bader	A	A

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY S.M.D'Agostino 84 July 31

APPROVED R. Dubois 84-8-16

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

DIST. 6

TITLE FW ACCUM KIT EURCB-D

SIZE	REVISION STATUS FOR	SHEET	REV
X	58082269	1/1	A

BRUNING 44-141 40366

CE 300 A-3 (1-79)

PD 84/09/24 X 58082269 1/1 A

001

*	3	A	58002689-085	V UV 32K EPROM	1	EA
*	4	A	58002689-086	V UV 32K EPROM	1	EA
*	5	A	58002689-087	V UV 32K EPROM	1	EA
*	6	A	58002689-114	V UV 32K (4KX8) EPROM	1	EA
*	7	A	58002689-089	V UV 32K EPROM	1	EA
*	8	A	58002689-090	V UV 32K EPROM	1	EA
*	9	A	58002689-115	V UV 32K (4KX8) EPROM	1	EA
*	10	A	58002689-116	V UV 32K (4KX8) EPROM	1	EA
*	11	A	58002689-093	V UV 32K EPROM	1	EA
*	12	A	58082270-001	D CIL EURCB-D	X	
*	13	A	58060578-002	P ID LABEL FUNCT PWA	1	EA
*	14	A	58060578-001	P ID LABEL FUNCT PWA	1	EA

FW ACUM KIT EURCB-D

X 58082269 1/1 A

Honeywell HONEYWELL INFORMATION SYSTEMS		DWG. NO. 58082268	SHEET 1/3	REV A
LOC. PHOENIX,ARIZONA	DISTR 7B	PROJECTION	CODE	
	DATA BASE T082268 D082268			
PREPARED BY DATE PMDQD 84JUL31	TITLE INSTALLATION INSTRUCTION EURCB-D EPROM FW KIT(S)		F.C.F.: 58082267 OP.LST: N/A	
APPROVED BY T. FINCH 84JUL31				

REVISION RECORD

REV.	AUTHORITY	DATE	SIGNATURE	SHEETS AFFECTED
A	LEVEL 3 ISSUE	84JUL31	SEE APERTURE CARD	RSS, 1 THRU 3F

I. SCOPE:

THIS INSTRUCTION PROVIDES THE INFORMATION NECESSARY IN THE INSTALLATION OF EPROMS ON THE EURCB-D BOARD.

II. INSTALLATION PROCEDURE

1. FUNCTIONAL PWA EURCB-D

1.1. REFER TO THE FUNCTIONAL PWA ASSEMBLY 58082267 PL FOR THE ITEM NUMBERS REFERENCED IN THE FOLLOWING INSTRUCTIONS UNLESS OTHERWISE SPECIFIED.

1.2. REFER TO FIGURE 1 FOR APPROXIMATE LOCATION AND IDENTITY OF ITEMS REFERRED TO IN INSTRUCTION STEPS THAT FOLLOW.

1.3. PLUG-IN THE PROGRAMMED EPROMS ON THE EURCB-D BOARD IN SOCKET LOCATIONS LISTED IN COMPONENT INSTALLATION LIST, 58082270, CALLED FOR ON ACCUMULATION KIT 58082269. USE CARE IN HANDLING AND INSTALLING THE EPROMS BY AVOIDING ANY STATIC CHARGE BUILD-UP ON THE BODY OF THE HANDLER OR PERSON.

1.4. INSTALL THE FUNCTIONAL BOARD ASM LABEL ITEM 4 ON BOARD. INSTALL THE LABEL ON THE BOARD STIFFENER SUCH THAT THE LABELIS VERTICAL. REFER TO FIGURE 1 FOR GENERAL LOCATION OF THE LABEL.

1.5. INSTALL THE APPROPRIATE TAB NUMBER AND REVISION LABELS TO THE FUNCTIONAL BOARD IDENTIFICATION NUMBER USING ITEMS 13 AND 14 PROVIDED IN THE FIRMWARE ACCUMULATION KIT, 58082269. (EXAMPLE: "001 A" AS INITIALLY ISSUED). SEE FUNCTIONAL BOARD ASSEMBLY RSS FOR TAB NUMBER AND REVISION LETTER.

III. REMOVAL PROCEDURE FOR BASIC OR OPTION PLUGGABLE EPROM KIT(S):

1. FOLLOW THE REVERSE PROCEDURE AND PRECAUTIONS OF THE INSTALLATION.

IV. PARTS DISPOSITION:

1. RETURN THE PARTS REMOVED IN THE STEP III ABOVE TO "LCPD" MANUFACTURING.

ADDRESS::

HONEYWELL INFORMATION SYSTEMS
P.O. BOX 8000
PHOENIX, ARIZONA 85066

C/O MGR LCPD WAREHOUSE
MAIL DROP J-2

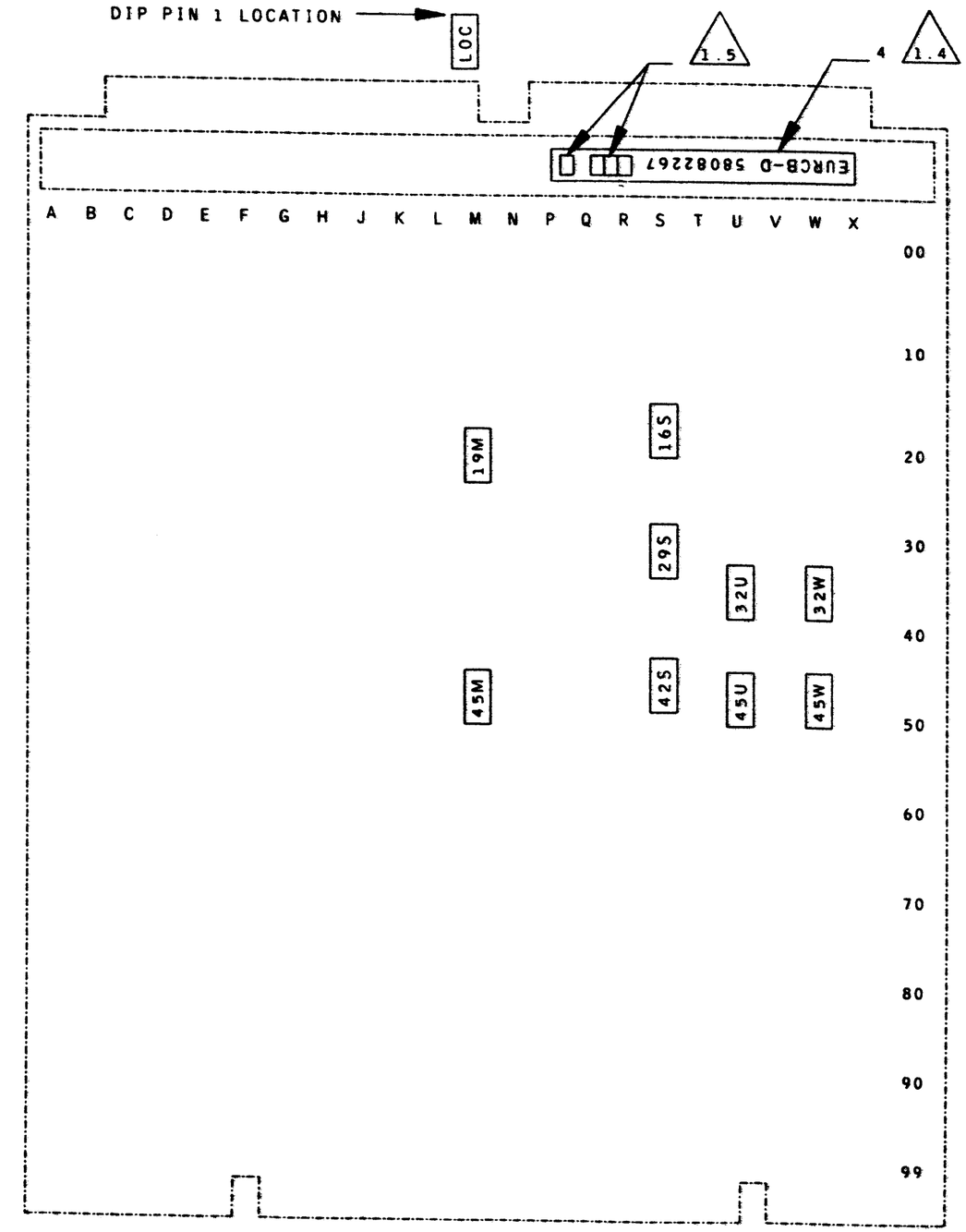

DIP PIN 1 LOCATION
LOC
1.5
4
1.4
EURCB-D 58082267
A B C D E F G H J K L M N P Q R S T U V W X
00
10
20
30
40
50
60
70
80
90
99
19M
16S
29S
32U
32W
42S
45M
45U
45W

FIGURE 1

58082270

REV	AUTHORITY	DATE YR	DATE MO	DATE DAY	SIGNATURE	TAB NO 001	DWG SH 1
A	LEVEL 2 ISSUE	84	09	18		A	A

FOR CONTINUATION OF REVISION STATUS SEE SHEET

Honeywell

HONEYWELL INFORMATION SYSTEMS INC.

LOC PHOENIX ARIZONA

MADE BY [signature] 84 July 31

APPROVED R. Duane 84-8-22

REVISION STATUS FOR EACH PAGE SHEET OR GROUP IS SHOWN BY LAST ENTRY IN THE CORRESPONDING NUMBERED COLUMN

DIST. 37

TITLE: COMP INSTL LIST

SIZE	REVISION STATUS FOR	SHEET	REV
A	58082270	1/1	A

BRUNING 44-141 40366

CE 300 A-3 (1-79)

Honeywell HONEYWELL INFORMATION SYSTEMS INC.	FW CIL	SPEC NO 58082270	SHEET 1/1	REV A

PROM TAB NUMBER TO BOARD LOCATION REFERENCE.
PROM IDENT NUMBER: [redacted] 58002689

LOC	TAB NUMBER
	001
45W	085
32W	086
45U	087
32U	114
42S	089
29S	090
16S	115
19M	116
45M	093