M228X
Fixed Disk Unit
Customer Engineering Manual

FUJITSU

B03P-4580-0100A. . .E1

REVISION RECORD		
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B	(11-15-80)	Manual updated with ECs 001 to 009, plus technical information of the model M2280/M2289 and editorial changes.
C	(4-20-81)	Manual updated with ECs 010 to 012, plus packaging materials change on pages 3-2 and 3-3.
D	(4-20-82)	Manual updated with ECs 013 to 026, plus description of Dual Port option
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Note 1. A revision of each page except "A" is indicated by the Revision Letter with the specification number of this manual in the bottom of the page.

Note 2. A bar by the page number in this page indicates pagination rather than content has changed.

Preface

This manual has been prepared for customer engineers directly involved with maintaining the M228X fixed disk unit.

The information is provided in 10 sections:

Section 1: General Description
Section 2: Operation
Section 3: Installation
Section 4: Theory of Operation
Section 5: Trouble Shooting Guide
Section 6: Maintenance
Section 7: Spare Part List
Section 8: IC Detail
Section 9: Parts and Illustration Catalog
Section 10: Schematics

Fujitsu Ltd.

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Section 1

General Description

1. GENERAL DESCRIPTION

1.1 GENERAL DESCRIPTION

1.1.1 General Description

The M228X series Fixed Disk Unit is a high performance, random access storage device. The M228X is a series of models having storage capacities of 67.4MB, 84.7MB, 134.8MB, and 168.5MB, each with an optional fixed head capacity of 655.4KB additional storage.

The basic components of these units are Disk Enclosure, spindle drive motor and brake, read/write PCB, driver/receiver interface circuitry and function-related logic PCB's. The Disk Enclosure (DE) consists of Contact Start/Stop (CSS) heads and media, rotary actuator linear motor and filters all contained in a sealed cover. The M228X series has attained performances equal to those of large storage units in a small, low price package.

The M228X FDU contains a standard SMD interface, thereby allowing the drives to be added to an existing disk configuration allowing substantial savings over removable media drives. By standardizing on this interface, development time for controllers and software will be substantially reduced.

The M228X series may be mounted horizontally or vertically. They are designed to be mounted in a standard 19 inch rack or built into a system cabinet. Up to eight drives can be daisy-chained together.

1.1.2 Features

(1) High reliability
   (a) Sealed air recirculation system continuously cleans the air within the DE, thus eliminating the need for preventive maintenance.
   (b) Contact start/stop type heads and media developed by the most up-to-date technology are employed, thus eliminating head loading and other mechanisms that could reduce reliability.
   (c) Rotary-type actuator reduces unit size, power consumption and heat dissipation.
   (d) The electrical components mounted in the disk enclosure have been reduced to a minimum.
   (e) A head IC (HIC) is mounted near each data and servo head. The HIC improves the signal-to-noise ratio for increased data integrity.

(2) Expandability
   A complete series of models having file capacities of 67.4MB/84.7MB/134.8MB/168.5MB is available. The required file configuration can be enhanced by combining with optional fixed heads for an additional capacity of 655.4KB. File capacity can be easily changed by removing three nuts holding the Disk Enclosure and installing a different capacity DE. The power supply (option) is compatible with all M228X models.

(3) Maintainability
   Routine preventive maintenance is unnecessary.

(4) Compact, Light Weight
   These units can be mounted in a standard 19 inch rack in 6 pitches.
   The weight of the unit, excluding the optional front panel (front panel and slide rails: 8kg) ranges from a minimum of approximately 35kg for the M2282 to a maximum of approximately 40kg for the M2288.

(5) Vertical Mount Capability
   FDU may be installed in a vertical direction to be built into a system.

(6) Dual Port option

Each M228X model can be connected with two controllers when a dual port option is provided.

This option is available as a separate printed circuit board which is mounted on the PCB chassis.

1.2 SPECIFICATIONS

1.2.1 Basic Specifications

These units have the following basic specifications:

Table 1-2-1 Basic Specifications

Model	Fixed-head storage capacity	Access-head storage capacity
M2282	None	67.4MB
M2280	None	84.2MB
M2283	None	134.8MB
M2284	None	168.5MB

The models with optional fixed-heads have the following specifications:

Table 1-2-2 Fixed-head Option Specifications

Model	Fixed-head storage capacity	Access-head storage capacity
M2286	655KB	67.4MB
M2289	655KB	84.2MB
M2287	655KB	134.8MB
M2288	655KB	168.5MB

1.2.2 Physical Specifications

Table 1-2-3 Physical Specifications

Item	Condition	Specification
Dimension*1	Height	250mm (9.84 in)
	Width	416mm (16.38 in)
	Depth	650mm (25.59 in)
Weight*2	Minimum unit weight (M2282)	Approx 35kg (77 lbs)
Weight*2	Maximum unit weight (M2288)	Approx 40kg (88 lbs)
Temperature	Operating	41°F ~ 104°F
		5°C ~ 40°C
	Non-operating	-40°F ~ 140°F
		-40°C ~ 60°C
	Gradient	±27°F/hour max.
		±15°C/hour max.
Humidity	Operating	20% ~ 80% RH
	Non-operating	5% ~ 95% RH
		(No condensation)
Dust		0.168 mg/m^3 max
		(Stearic acid standard)
Vibration	Operating	0.2G max (5Hz ~ 50Hz)
		1G max (50Hz ~ 500Hz)
	Non-operating	3G max (when locked for shipment)
Shock	Operating	2.0G max.
	Non-operating	5.0G max.
Altitude	Operating	10,000 feet
	Non-operating	40,000 feet

* Note 1) Same dimension with or without dual port feature.

2) The front panel assembly is excluded in the table.

1.2.3 Power Source Specifications

(1) AC Power Requirement

Table 1-2-4 AC Power Source Specifications

Voltage	Frequency	Load Current	Starting Current
100V ±10%	50/60Hz +1% -3%	2.5 A max	8 A max
115V +15% -10%	60Hz ±1%	3.0 A max	9.5 A max
AC220V +22V -25V	50Hz +1% -2%	2.0 A	5 A max*
AC 240V +24V -27V			

Note *: Starting current is specified at AC input of optional power supply unit (B14L-5100-0030A).

(2) DC Power Requirement

Table 1-2-5 DC Power Source Specifications

Voltage	Load Current	
	Basic Unit	Basic Unit with dual port option
+5V ± 5%	5.5A max	6.5A max
+12V ± 5%	0.6A max	0.6A max
−12V ± 5%	2.2A max	2.6A max **
+24V ± 20%	3.8A max*	3.8A max*

* +24V Load Current (Worst Case)
** Includes load for dual port option.

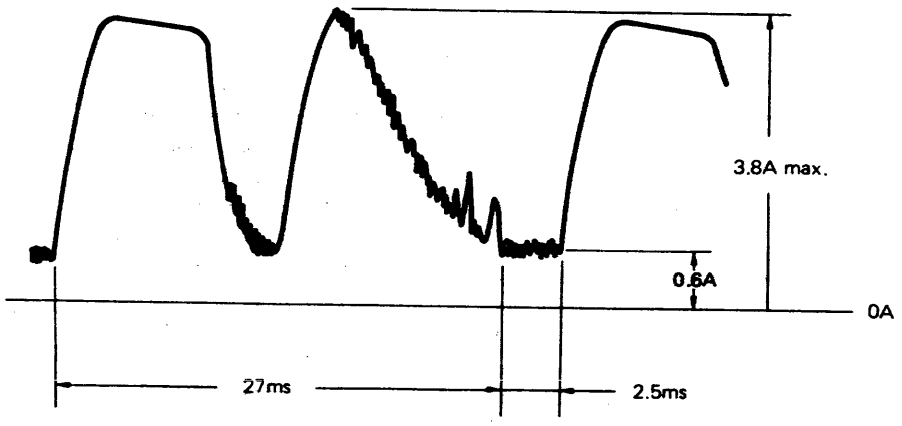


Figure 1-2-1 +24V Load Current Waveform

1.2.4 Data Recording Specifications

Table 1-2-6 Data Recording Specifications

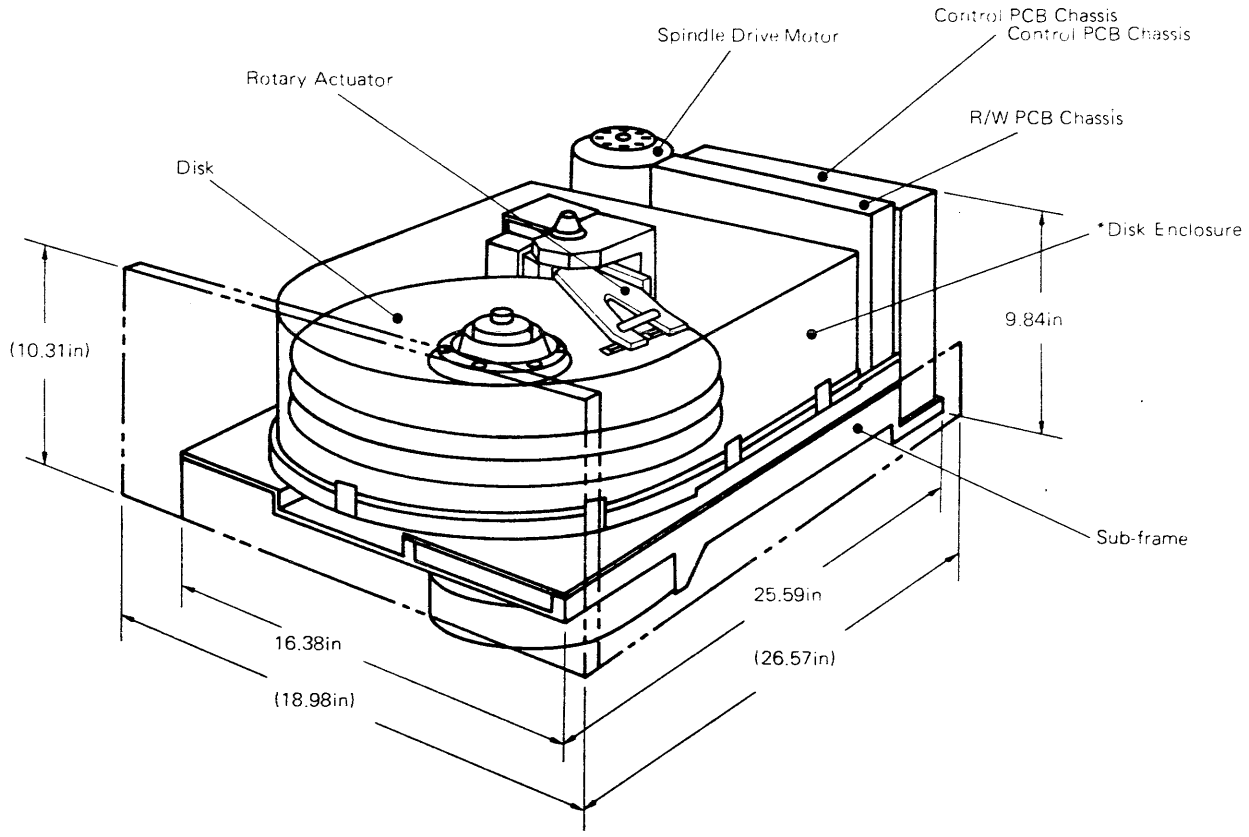
Item		Specification			
		M2282	M2280	M2283	M2284
Storage capacity (unformatted)	Access-heads	67.4 MB	84.2 MB	134.8 MB	168.5 MB
	*Fixed-heads	655.4 KB	655.4 KB	655.4 KB	655.4 KB
No. of cylinders	Access-heads	808 (+15 spare)	808 (+15 spare)	808 (+15 spare)	808 (+15 spare)
	*Fixed-heads	4	4	4	4
Tracks per cylinder	Access-heads	4	5	8	10
	*Fixed-heads	8	8	8	8
Capacity per track		20,480 Bytes			
One-track positioning time		6 mS			
Average positioning time		27 mS			
Maximum positioning time		55 mS			
Rotational speed		2,964 RPM ± 4%			
Average latency time		10.12 mS			
Recording density		6,580 BPI			
Track density		680 TPI			
Transfer rate		1,012 KB/S			
Recording method		MFM			
Interface data		NRZ			
Starting time		40 sec			
Stopping time		30 sec			
Capacity in 64-sector format		53.9 MB	67.4 MB	107.8 MB	134.8 MB

*Notes: Fixed-heads are optional.

1.3 CONFIGURATION

1.3.1 Basic Configuration

The basic configuration of this unit is given in Figure 1-3-1 and its block diagram is given in Figure 1-3-2.



(XXX) indicates measurement with front panel and slides option.

*M2282, M2286 Two disks in DE
M2280, M2289 Two disks in DE
M2283, M2287 Three disks in DE
M2284, M2288 Three disks in DE

Figure 1-3-1 Basic Configuration

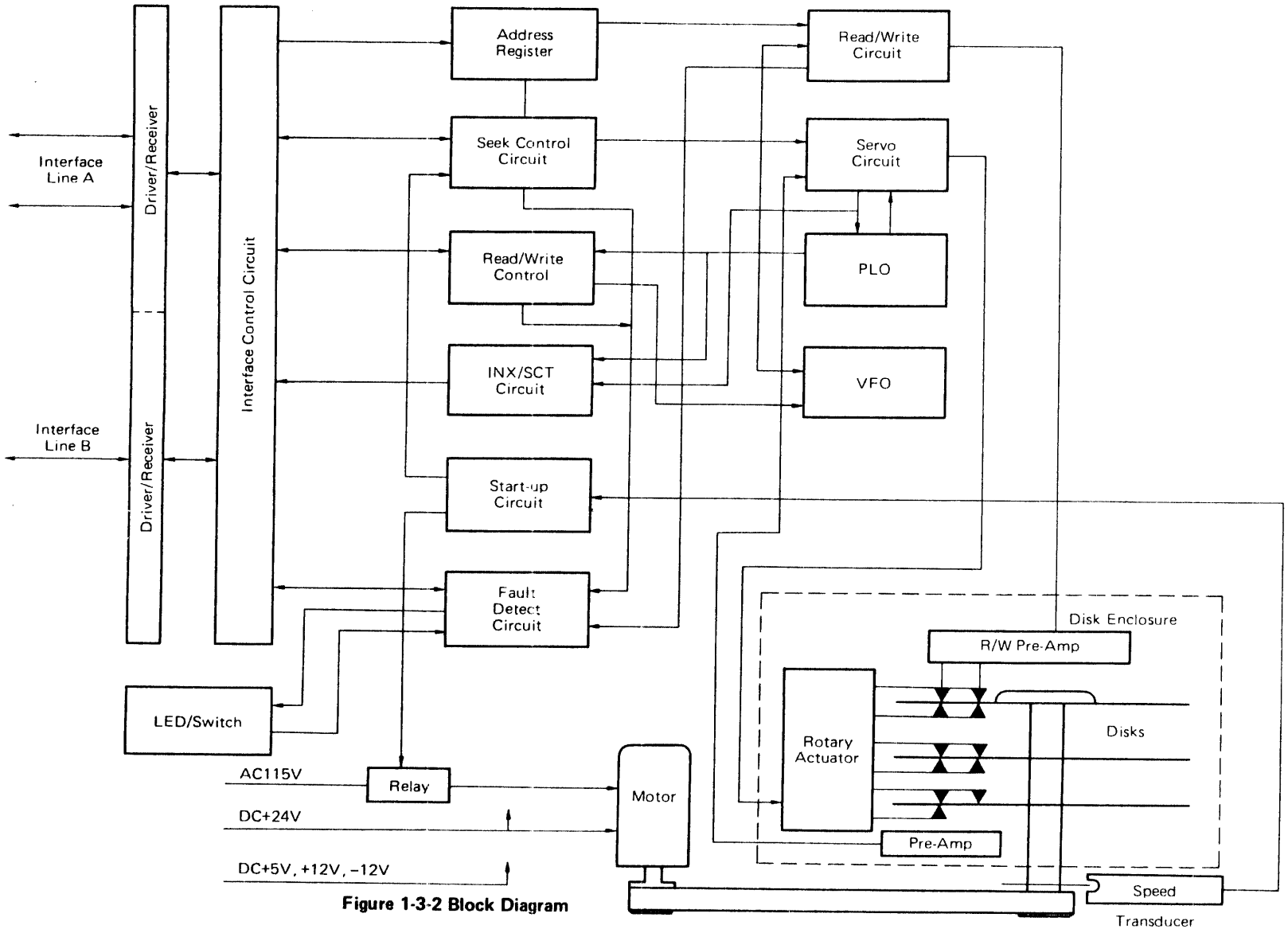


Figure 1-3-2 Block Diagram

1.3.2 Option

Table 1-3-1 Options List

Name	Specification	Remarks
Power supply	B14L-0300-0018A	Connector type 100V/115V
Power supply	B14L-5100-0030A	Connector type 220V/240V
Operator Panel and Slide rails	B03B-4540-E350A	19" rack mount type (Slide rail 27"-drawing length 29")
Operator Panel and Slide rails	B03B-4540-E353A	19" rack mount type with short slide (Slide rail 24"-drawing length 29")
Operator Panel and Slide rails	B03B-4540-E354A	19" rack mount type with short slide without Front Panel, Operator Switch and cable
Slide rail kit	B030-4540-V450A	Kit of Slide rails, Brackets, Nut Bars and Screws.
Dual Port Unit	B03B-4540-E901A	Printed circuit board and mounting plates.
Rubber shock mount	B30L-1920-0002A	Built-in type (vertical)
Cable*	B660-1065-T006A	Interface cable "A"
Cable**	B660-1065-T008A	Interface cable "B"
Terminator A	B16B-4870-0010A	A cable line terminator

Notes: * Cable length (ℓ) can be specified from 1m to 30m in 20 inch increments.

** Cable length (ℓ) can be specified from 1m to 5m in 500mm increments.

Example: B660-1065-T008A=L3R503 (for 3.5m)

$\rightarrow 3.50 \times 10^{3}$ mm

Section 2
Operation

2. OPERATION

2.1 GENERAL DESCRIPTION

The M228X Fixed Disk Unit can be mounted in a 19 inch rack or built into a system cabinet. An operator panel (with slide rails) is available as an option.

The GBNM or GBGM Printed-Circuit-Board (PCB Chassis) of the M228X Fixed Disk Unit is equipped with Maintenance Aid LED's, Device Check Clear switch and File Protect switch.

Powering up/down and the functions of the control panel indicators (LED) and switches will be described in this section. The optional operator panel will be described as well as the functions of the LED's and switches.

2.2 POWERING UP/DOWN

The M228X Fixed Disk Unit is not equipped with a power ON/OFF switch. Therefore, powering up/down of the Fixed Disk Unit is usually performed by a powering up/down of the system.

However, when the disk unit is equippped with an optional power supply, powering up/down may be performed by turning the power switch ON and OFF in Local mode at the power supply or by sending Pick/Hold signals from the control unit with the power supply in Remote mode.

2.3 CONTROL AND INDICATORS

2.3.1 Operator Panel (option)

The operator panel (front panel) is optional, however, an example will be given and the functions of the LED's and switches will be described here.

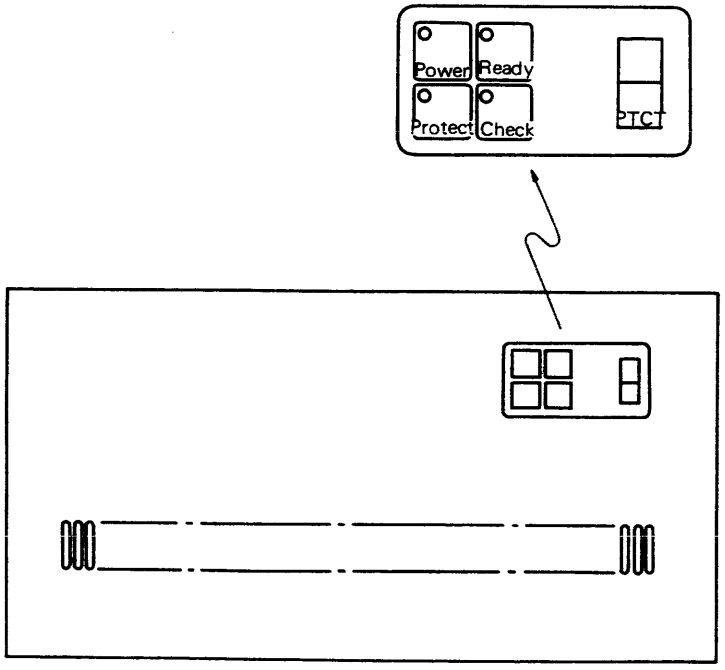


Figure 2-3-1 Operator Panel

(1) POW (power) indicator: Red
This LED lights up when the power is turned on.

(2) RDY (Ready) indicator: Red
This LED indicates the initial seek has been performed or indicates the termination of a Seek or RTZ operation.

(3) CHK (Check) Indicator: Red

This LED indicates any fault condition.

(4) PTCT (Protect) indicator: Red

This LED indicates that writing is inhibited.

(5) PROTECT switch: White

This key inhibits the write operation.

(6) CHK CLR (Check Clear) switch: Gray (flat key)

This key resets a Device Check status.

2.3.2 PCB Chassis

The unit contains a PCB chassis with Maintenance Aid Display (LED's), a Device Check Clear switch and File-protect switch.

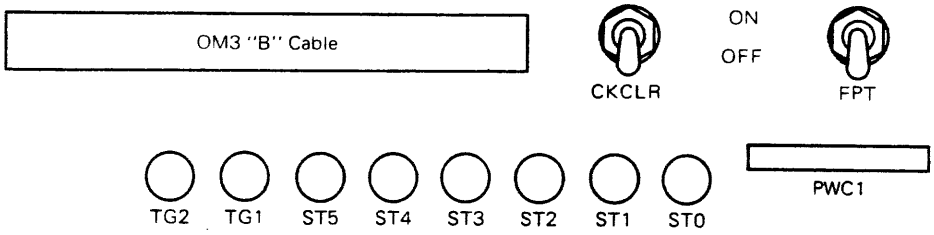


Figure 2-3-2 Maintenance Aid Display and Switches

(1) CKCLR (Check Clear) switch: (momentary)

This switch resets a Device Check status.

(2) FPT (File Protect) switch

This switch inhibits the write operation. When an optional operator panel is installed on the unit, this switch should be in the OFF position.

(3) TG1, 2 (Status Tag 1, 2) LED's: Red

Two LED's indicate four basic disk conditions in binary coded decimal, which are Not-Ready status, Device-Check status, Unit status and Seek-Check status.

(4) ST0 to ST5 (Status 0 to 5) LED's: Red

Six status conditions are displayed for each Status Tag 1 and 2 combination as shown in Table 2-3-1.

Table 2-3-1 Maintenance Aid Display Conditions

TG	Tag Decode 0	Tag Decode 1	Tag Decode 2	Tag Decode 3
ST	Not Ready	Device Check	Unit Status	Seek Check
0	Power Ready	Control Check 1	Unit Selected	RTZ or Seek Timeout
1	Channel Ready	Control Check 2	Fixed Sector Mode	Seek Guard Band
2	Speed OK	Read/Write Check 1	On Cylinder	Linear Mode Guard Band
3	Start 1 (GBENB)	Read/Write Check 2	File Protected	RTZ Outer Guard Band
4	Start 2	Read/Write Check 3	Busy	Over Track Crossing Pulse
5	Initial Seek Timeout	Read/Write Check 4	Access Head Selected	Illegal Cylinder

(1) Not Ready Status

(a) Power Ready

Indicates that +5V, ±12V DC power is up to nominal voltage.

(b) Channel Ready

Indicates the Channel Ready signal is true.

(c) Speed OK

Indicates that the rotational speed is up to 2,370 RPM (80%).

(d) Start 1

Indicates that the Start Counter has output the GBENB (Guard Band Enable) signal.

(e) Start 2

Indicates that the Start Counter has output the STARTP (Start Pulse) to initiate the Initial Seek sequence.

(f) Initial Seek Time Out

Indicates that the Initial Seek sequence was not accomplished within 640 ms after the STARTP signal.

(2) Device Check Status

(a) Control Check 1

Indicates that a read/write instruction was issued during Busy Status.

(b) Control Check 2

Indicates that Write Gate was issued during a fault condition.

(c) Read/Write Check 1

Indicates that Write Gate was issued during an off-track status or VCM-overheating has occured.

(d) Read/Write Check 2

Indicates that write current to the data head did not flow during a write operation or that write current flows without a write gate command.

(e) Read/Write Check 3

Indicates that Write Gate was issued during file-protected status.

(f) Read/Write Check 4

Indicates that Read or Write Gate was issued during a multi-head-selected condition.

(3) Unit Status

(a) Unit Selected

Indicates that the unit is selected.

(b) Fixed Sector Mode

Indicates the fixed sector mode is selected.

(c) On Cylinder

Indicates On Cylinder status.

(d) File Protected

Indicates Write-protected status.

(e) Busy

Indicates that the heads are in motion.

(f) Access Head Selected

Indicates that an access head is selected.

(4) Seek Check Status

(a) RTZ Time Out

Indicates that an RTZ sequence was not terminated within 640 ms.

(b) Seek Gurad Band

Indicates that a Guard Band was detected during a direct seek operation.

(c) Linear Mode Guard Band

Indicates that a guard band was detected during a linear mode operation.

(d) RTZ Outer Guard Band

Indicates that an outer guard band was detected during an RTZ operation.

(e) Over Track Crossing Pulse

Indicates that the head overshot the new cylinder address during settling time (2.5ms).

(f) Over Cylinder

Indicates that an illegal cylinder address (823<CYL<895) was specified by the control unit.

2.3.3 Dual Port Option

The Dual Port Option has the operational switches and LEDs as shown in Figure 2-3-3. It is operated and observed from top side.

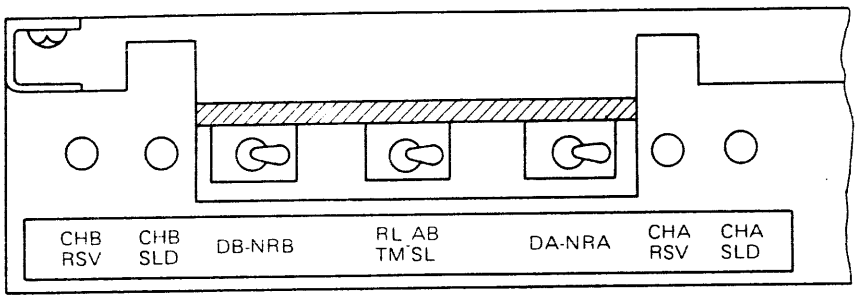


Figure 2-3-3 Switches and Indicators or Dual Port Option

(1) CHASLD LED (green)
Indicates that this unit is selected by the channel-A controller.

(2) CHARSV LED (orange)
Indicates that this unit is reserved by the channel-A controller.

(3) CHBSLD LED (green)
Indicates that this unit is selected by the channel-B controller.

(4) CHBRSV LED (orange)
Indicates that this unit is reserved by the channel-B controller.

(5) DA-NRA switch
DA (Disable A): Selected to disconnect the unit from the channel-A controller and disable it to send and receive all interface signals.
NRA (Normal A): Selected to connect the unit to the channel-A controller and enable it to send and receive interface signals.

(6) DB-NRB switch
DB (Disable B): Selected to disconnect the unit from the channel-B controller and disable it to send and receive all interface signals.
NRB (Normal B): Selected to connect the unit to the channel-B controller and enable it to send and receive interface signals.

(7) RLTM-ABSL switch
RLTM side: If this switched to RLTM (Release Timer) side, the reserved condition is released from the unit side.
ABSL side: If this is switched to ABSL (Absolute) side, the reserved condition is released from the controller side.

2.4 OPTIONAL POWER SUPPLY UNIT

The two types of optional power supply unit are provided with FDU M228X for USA and European versions. Refer to Table 1-3-1.
The front view of the power supply unit is shown in Figure 2-4-1.

(1) Main line switch
This switch controls application of site AC power to the power supply unit.
Turning on the switch applies power to fans, disk drive motor and DC power supply.

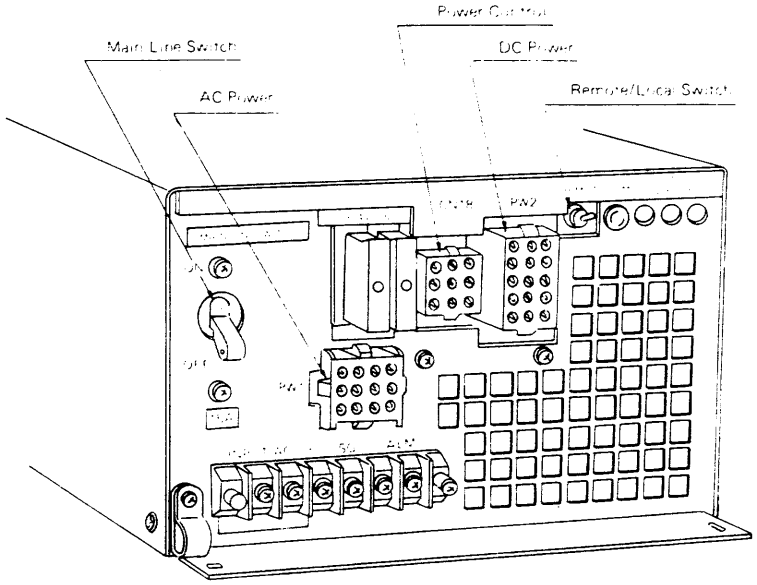
(2) Remote/local switch
This switch controls whether drive can be powered up from the power supply unit (Local mode), or the control unit through the FDU M228X (Remote mode).
In the Local mode, the power is applied to the disk drive when the Main Line Switch is turned on.

In the Remote mode, AC power to a fan, +5V DC and ±12V DC are supplied to the unit by turning on SW1 and then disk drive motor power and +24V DC are supplied when Pick/Hold signals from the control unit is grounded.

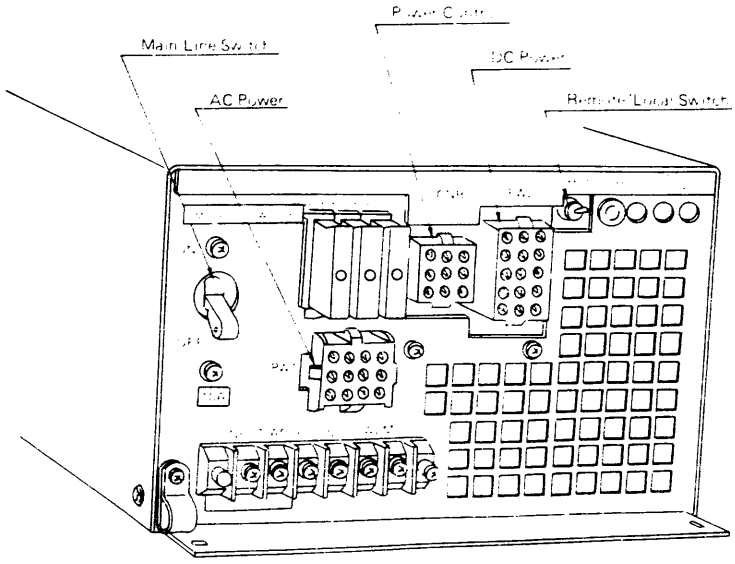
(3) Alarm lamp

Alarm lamp indicates the following power malfunction has occurred on the power supply unit or the disk unit.

(a) +5V DC: Over-current, Over-voltage and Non-voltage
(b) ±12V DC: Over-current and Non-voltage
(c) +24V DC: Fuse-blown
(d) AC input: Over-current
(e) Internal Fan: Thermal-switch
(f) AC output to disk unit fan: Over-current (european version)
(g) Disk unit fan: Thermal-switch



(1) USA Version Power Supply Unit



(2) European Version Power Supply Unit

Figure 2-4-1 Optional Power Supply Unit

Section 3

Installation

3. INSTALLATION

3.1 GENERAL DESCRIPTION

Unpacking, installation, and cabling of the unit when shipped separately, and work precautions when the unit is shipped as a system will be described in this section.

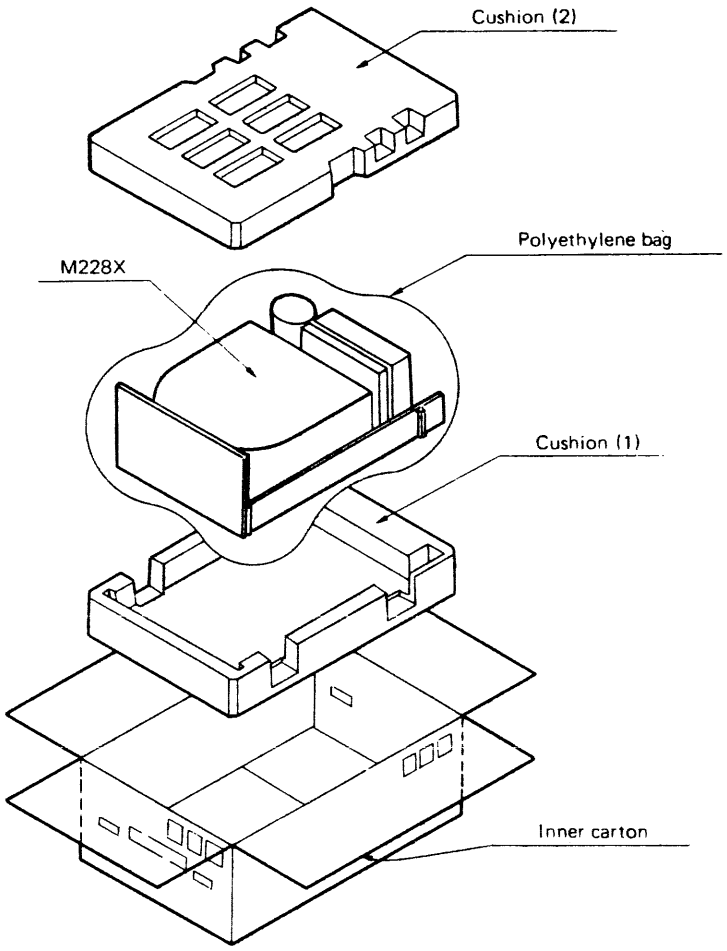
3.2 UNPACKING

M228X units are shipped in a double construction carton. (An exterior view of the carton is shown in Figure 3-2-1.) Store and open the carton on a flat surface.

To unpack the unit, first remove the inner carton. Then open the inner carton flaps to the left and right and remove the unit. Do not remove the unit by grasping the motor, PCB chassis or Disk Enclosure. Grasp the sub-frame at the bottom to avoid damage to the sub-assemblies.

Moreover, move the unit slowly and carefully so that it is not subjected to shock.

When the difference in the storage (or shipping) environment and the unpacking environment exceeds 20°C (36°F), the carton should be allowed to stand at the unpacking site for more than 3 hours prior to unpacking to avoid condensation.



* In case of no front panel, put into the spacer.

Figure 3-2-1 Construction of carton (Sheet 1 of 2)

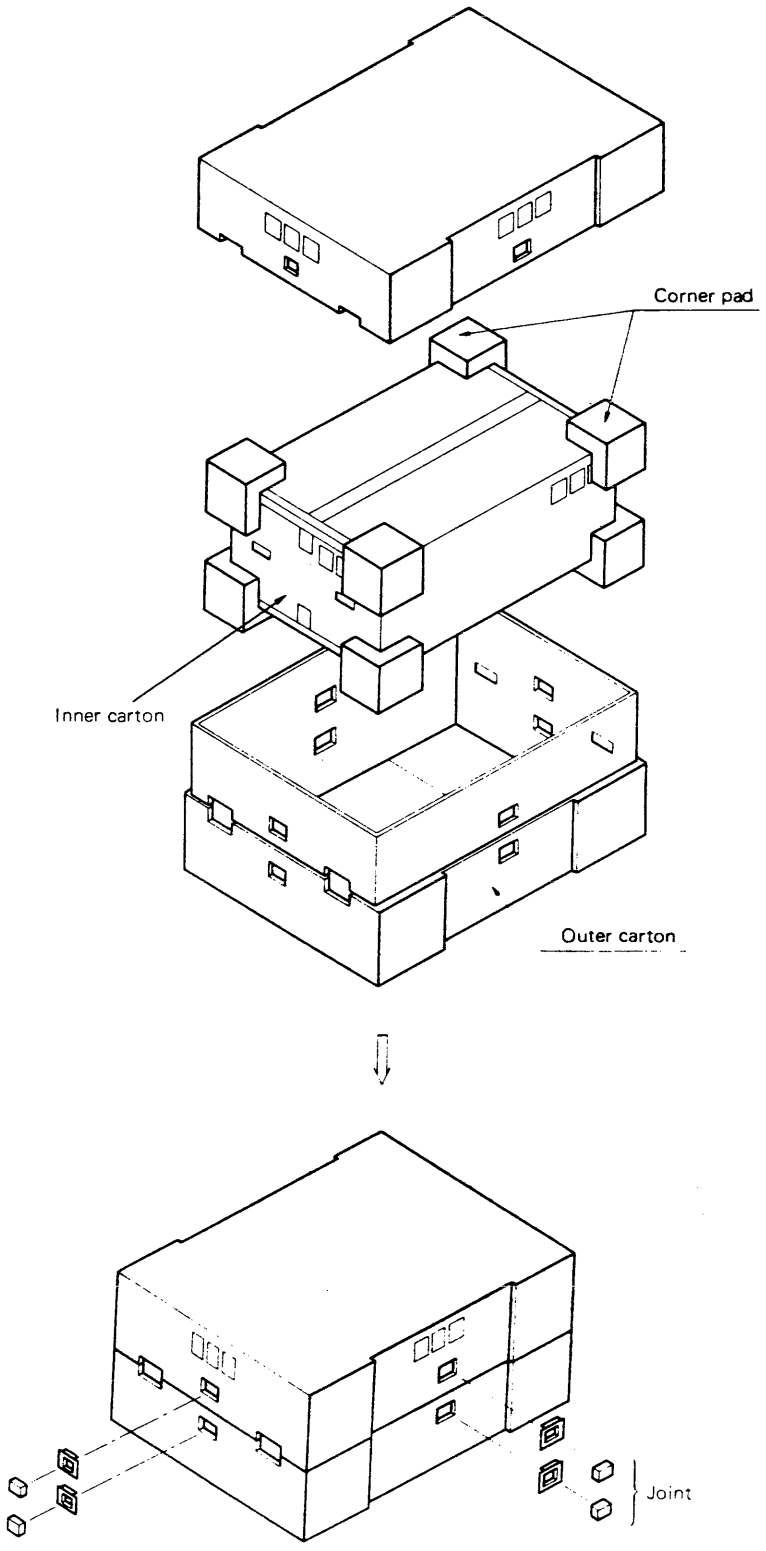


Figure 3-2-1 Construction of carton (Sheet 2 of 2)

3.3 VISUAL INSPECTION

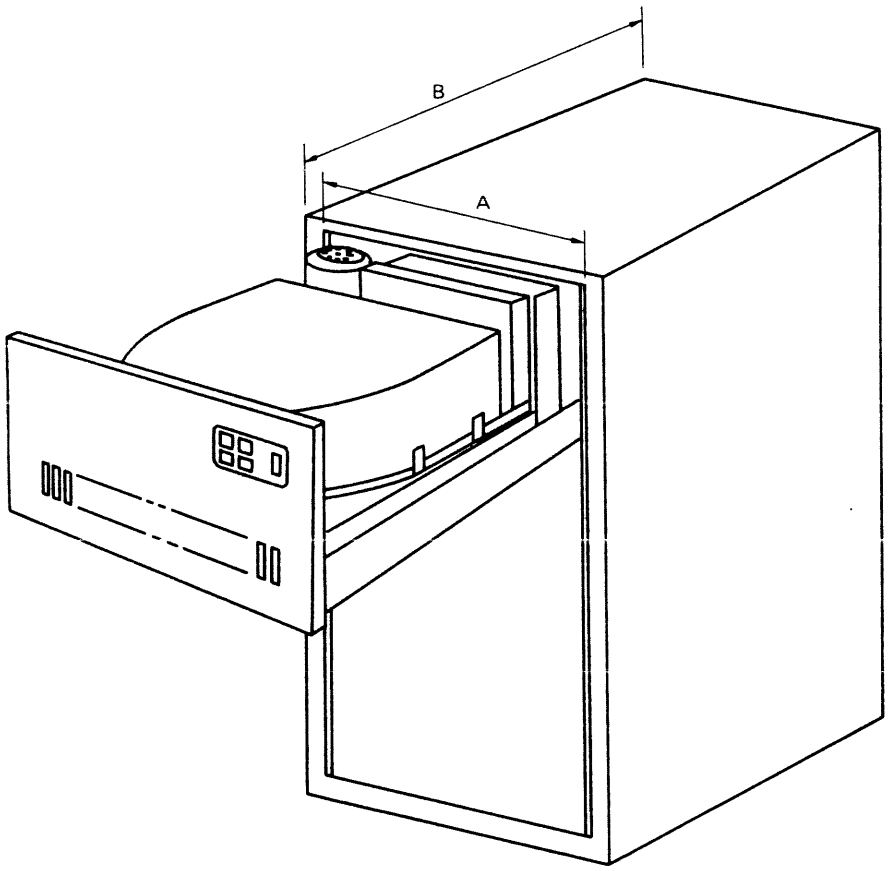
After unpacking the unit, visually inspect it as follows:

(a) Check for scratches, rust and soiling.
(b) Check for loose or missing parts and screws.
(c) Check that the printed-circuit boards in the PCB Chassis are mounted in the correct positions.
(d) Check that the specified parts, motor lock, spindle lock, and actuator lock are securely locked.

3.4 INSTALLATION

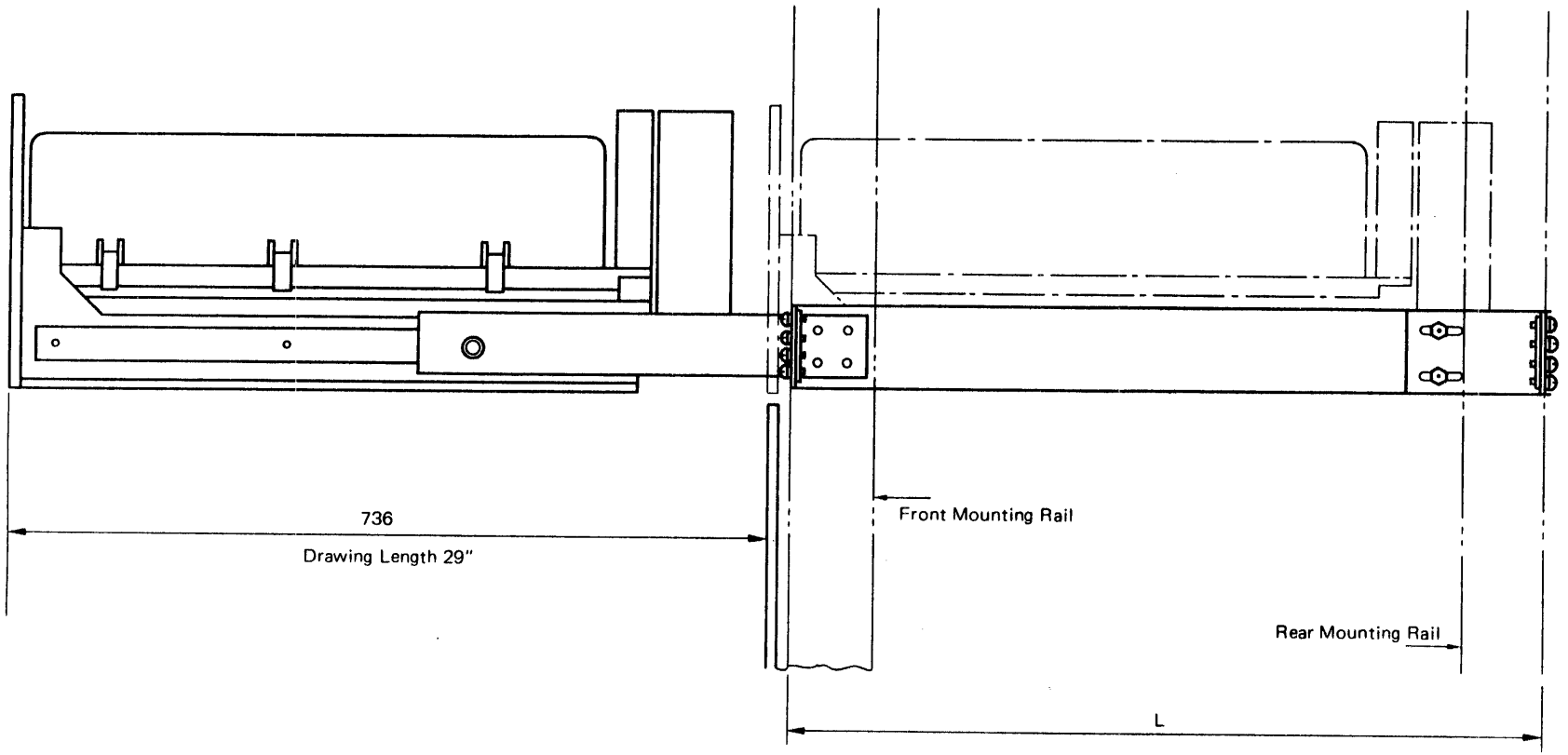
3.4.1 Mounting

The M228X may be mounted in a 19 inch rack or built into a system cabinet. The respective mounting methods are illustrated in Figure 3-4-1 and Figure 3-4-2.



Dimension A	Standard Rack:	inside	450mm (17.72")
		outside	482.6mm (19")
Dimension B	USA Standard:		762mm (30")
	European Standard:		751mm

Figure 3-4-1 19" Rack mount Installation



L: Distance between Front and Rear Mounting rail.
Front Panel Unit B03B-4540-E350A: 696 ±6 mm, 631 ±6 mm adjustable.
E353A: 24" to 30" adjustable.

Figure 3-4-2 19" Rack Mount Draw Out View

3.4.2 Vertical Mount Installation

The general installation procedure for a vertically-mounted unit is described below.

(1) Turn the unit over and place it on suitable cushioning material (the cushioning material on top of the inner carton of the shipping carton is provided for this purpose (see Figure 3-2-1)) so that the plastic cover of the disk enclosure is at the bottom. At this time, hold the unit by the aluminum casting so that excessive force is not applied to the motor and gate section or disk enclosure section. Be especially careful that shock and horizontal force are not applied to the unit when placing it onto the cushioning material with the plastic cover of the disk enclosure at the bottom. Refer to Figure 3-4-3.

(2) At this time, install the mounting fixture to the unit.
(Tighten all the mounting screws on the unit from the top.)

(3) Mount the unit in the cabinet. Refer to Figure 3-4-4.

(4) After mounting, release the spindle lock (see paragraph 3.4.3), actuator lock (see paragraph 3.4.4) and motor lock (see paragraph 3.4.5). These locks must always be locked when moving the equipment. See paragraph 3.6. (This also applies to the 19 inch rack mount installation).

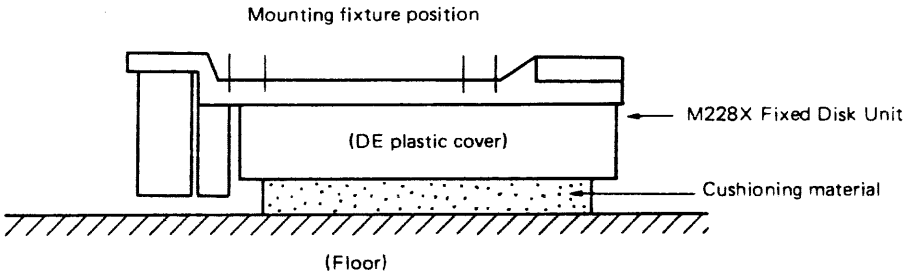
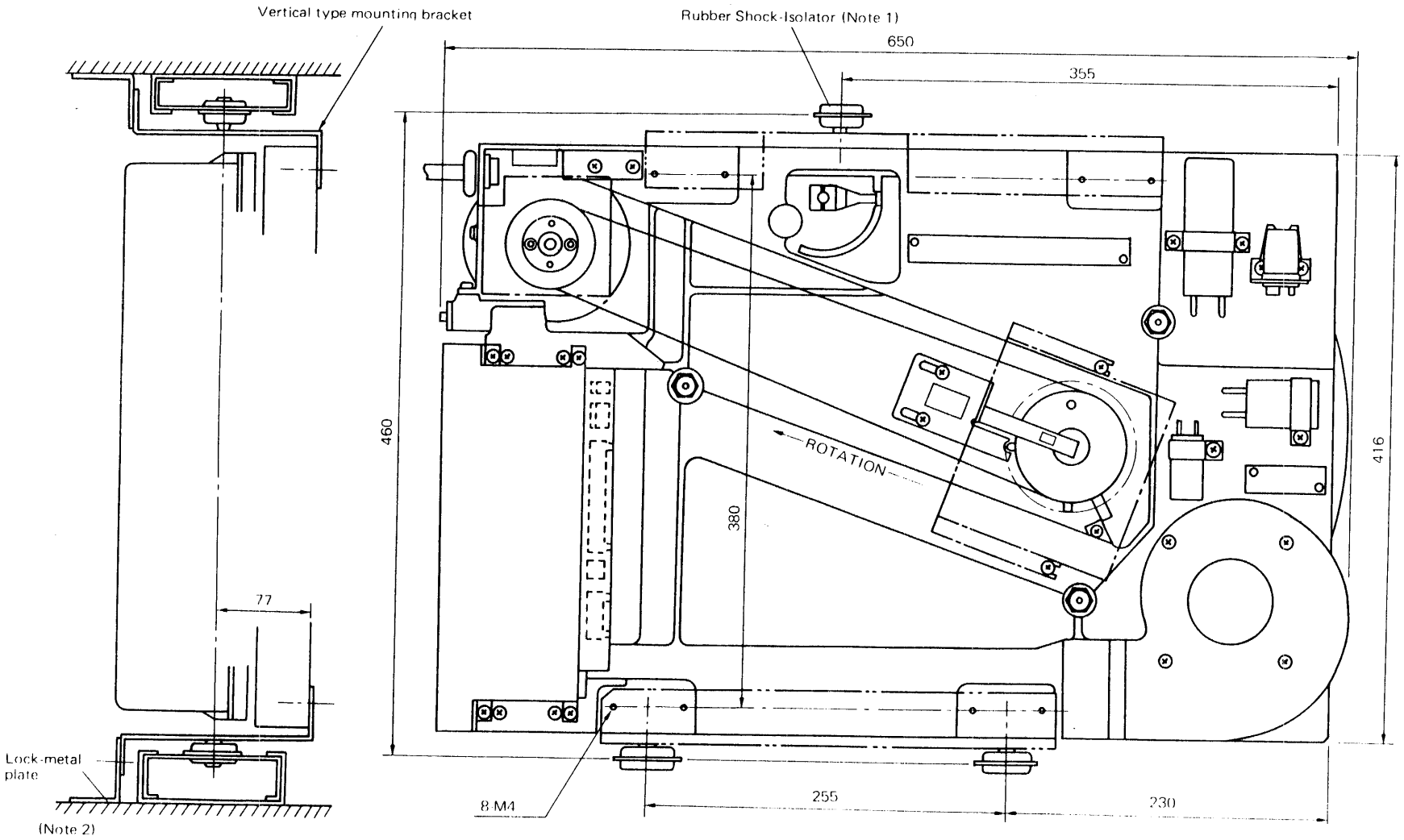


Figure 3-4-3 Mounting Fixture



Note 1: Three Rubber-Shock-Isolators are optional.

Note 2: The Unit must be locked only when it is to be shipped.

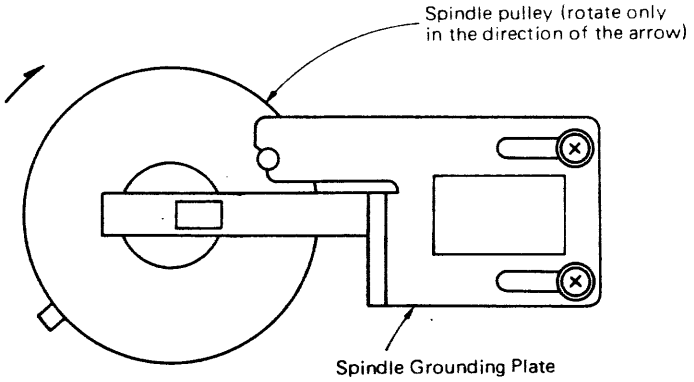
Figure 3-4-4 An Example of Vertical Mount Installation

(Unit: mm)

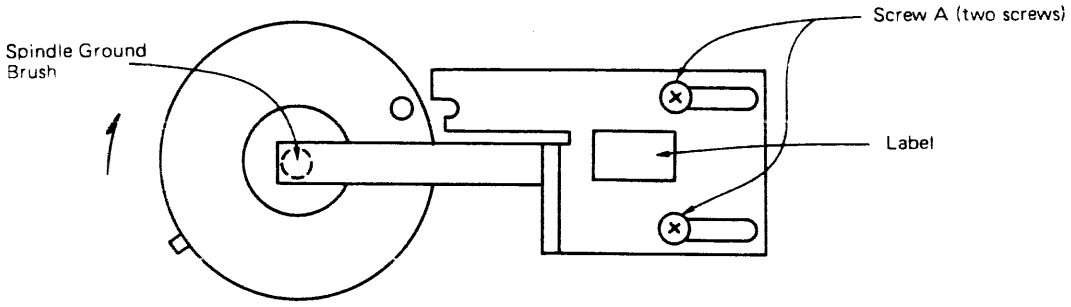
3.4.3 Unlocking Spindle

The spindle is locked with a spindle lock so that it cannot rotate during shipment. The spindle lock is located at the bottom of the spindle, and locks the spindle pulley. When installing the unit, the spindle lock must be released by loosening screws A (two screws) shown in Figure 3-4-5.

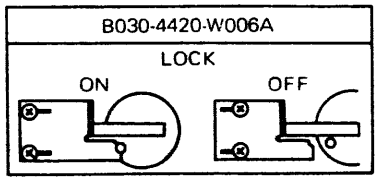
After unlocking, the spindle ground brush must be adjusted (see paragraph 6.5.5).



(a) Spindle Locked



(b) Spindle Released



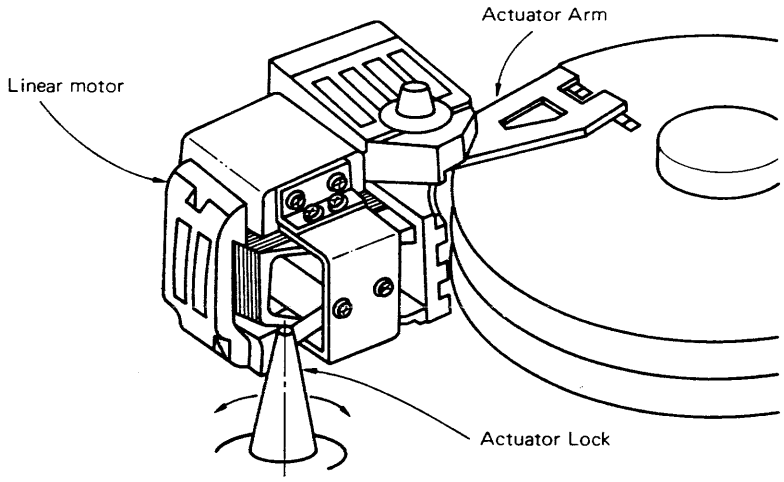
(c) Label

Figure 3-4-5 Releasing Spindle Lock

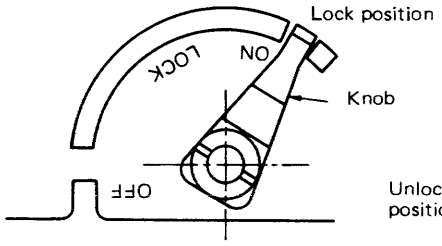
3.4.4 Unlocking the Actuator

If the actuator rotates when the disk is stopped, the heads and disks may be damaged. Therefore, the actuator is locked during shipment.

After installing the unit, the actuator must be unlocked by rotating the stopper. The stopper can be unlocked by turning the knob at the bottom rear of the disk enclosure through the hole in the sub-frame.

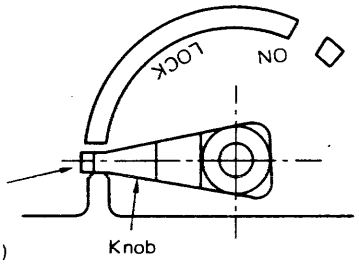


(a) Stopper positions



(Viewed from rear of disk enclosure)

(b) Actuator locked



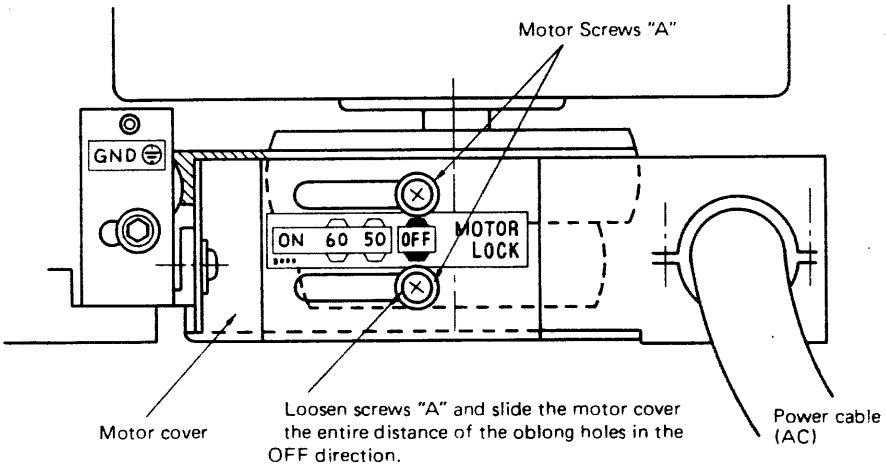
(c) Actuator unlocked

Figure 3-4-6 Actuator Lock

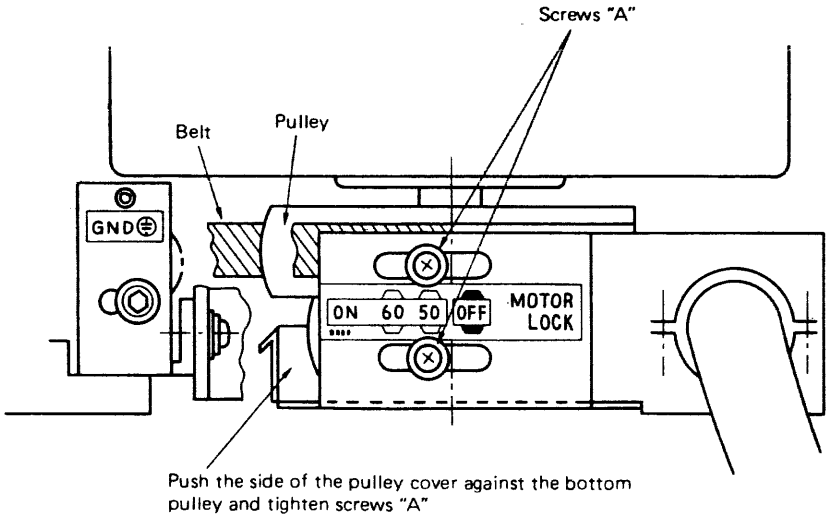
3.4.5 Unlocking the Motor

The motor must be locked during shipment to prevent unhooking the belt by vibration of the spindle. The motor is locked by pushing the side cover of the motor pulley (cover covering the motor pulley section) against the motor pulley. The motor is unlocked by loosening the two screws "A" holding the motor cover to the rear of the unit and sliding the pulley cover fully to the Left (unlock) position. Then secure screws "A". (Figure 3-4-7)

(a) Motor unlocked



(b) Motor locked

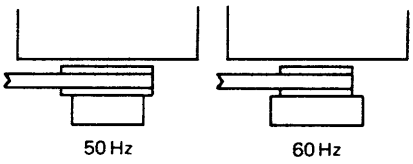


Note: Lock-on position is different according to power line frequency.

Figure 3-4-7 Motor lock and release

3.4.6 50Hz/60Hz Exchange

Check if the power line frequency is 50Hz or 60Hz, and confirm that the correct motor pulley is being used. The correct pulley diameter and belt position (50Hz/60Hz) are given on a label attached to the motor pulley cover (bottom side). The large diameter pulley is for 50Hz and the small diameter pulley is for 60Hz. (The label is illustrated in Figure 3-4-8.) When the power line frequency and the pulley mounted in the unit are different, the motor pulley must be changed and the belt tension adjusted as will be described in paragraph 6.5.3.



Tension Mark

50 H 60 H	Horizontal
50 V 60 V	Vertical

Figure 3-4-8 Frequency and pulley position (label)

3.4.7 Dual Port Installation

The Dual Port option consists of the following components:

Dual port option: B03B-4540-E901A

- Crosscall B (XCBM) PCB assembly:
  B16B-7990-0020A
- 50-pin cable (between CQFM and XCBM):
  B660-1065-T037A#L05R01 (50 mm)
- 10-pin cable (between CN32 on XCBM and CN21 on GBNM):
  B660-1060-T089A#L16R01 (160 mm)
- 26-pin cable (between CN34 on XCBM and OM3 on GBNM):
  B660-1065-T061A#L07R01 (70 mm)
- Cover:
  B030-4540-X901A
- Mounting plate:
  B030-4540-X903A
  B030-4540-X904A
- Others: Screws and label

When shipping the Dual Port option, the option is assembled with a PCB assembly, a cover and mounting plates. Three cables and four screws (M3 binding screw) are supplied as accessories.

The mounting procedure of Dual Port option is as follows:

(1) Mount the four screws (M3 binding screw) on the PCB chassis.
(2) Slide the option until the screws fit to the elogation notches on the mounting plates.
(3) Tighten these screws to fix the option.
Refer to Figure 3-4-9 for the above-mentioned procedures.
(4) 50-pin cable
  1) Remove the top cover from the PCB chassis.
  2) Insert the 50-pin cable (B660-1065-T037A#L05R01: 50mm) in CN30 on CQFM.
  3) Reposition the top cover, and fix it with screws.
  4) Insert the opposite connector in CN31 on XCBM.
(5) 26-pin cable
  1) Insert the 26-pin cable (B660-1065-T061A#L07R01: 70mm) in CN34 on XCBM.
  2) Insert the opposite connector in OM3 on mother board GBNM.
(6) 10-pin cable
  1) Insert the 10-pin cable (B660-1060-T089A#L16R01: 160mm) in CN32 on XCBM.
  2) Insert the opposite connector in CN21 on the mother board.

When doing this, see that the cable passes behind the FPT and CKCLR switches on the mother board.
Refer to Figure 3-4-10 for the above-mentioned cabling procedures.

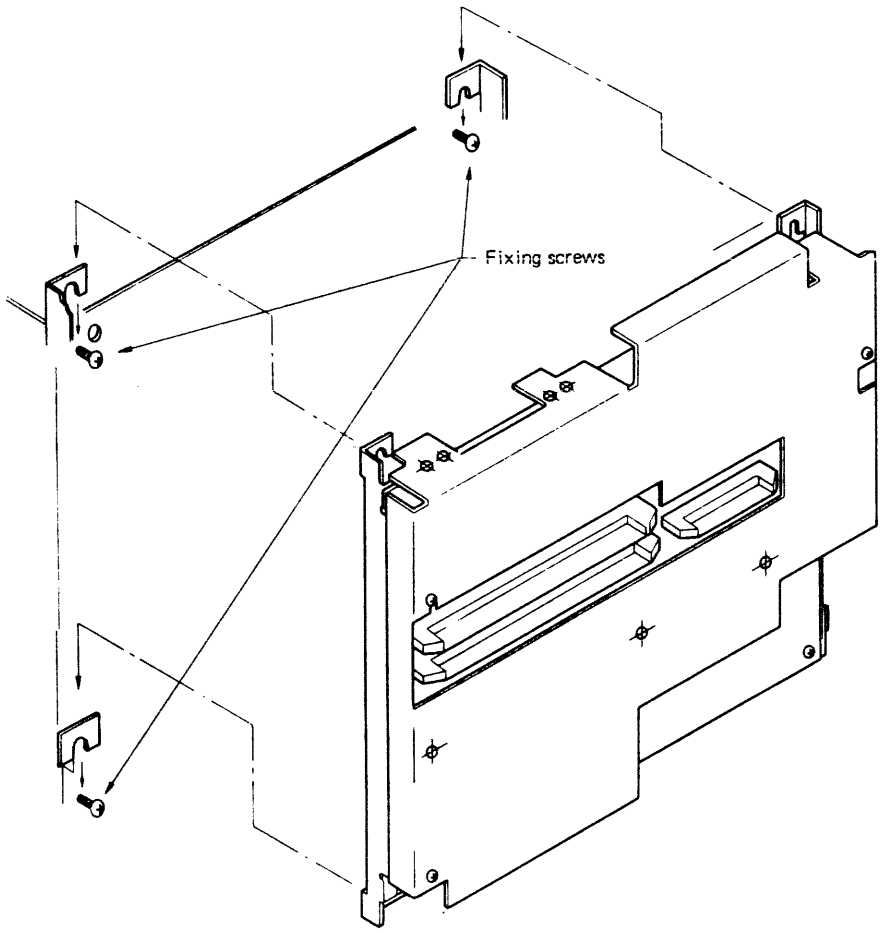


Figure 3-4-9 Fixing the Dual Port option

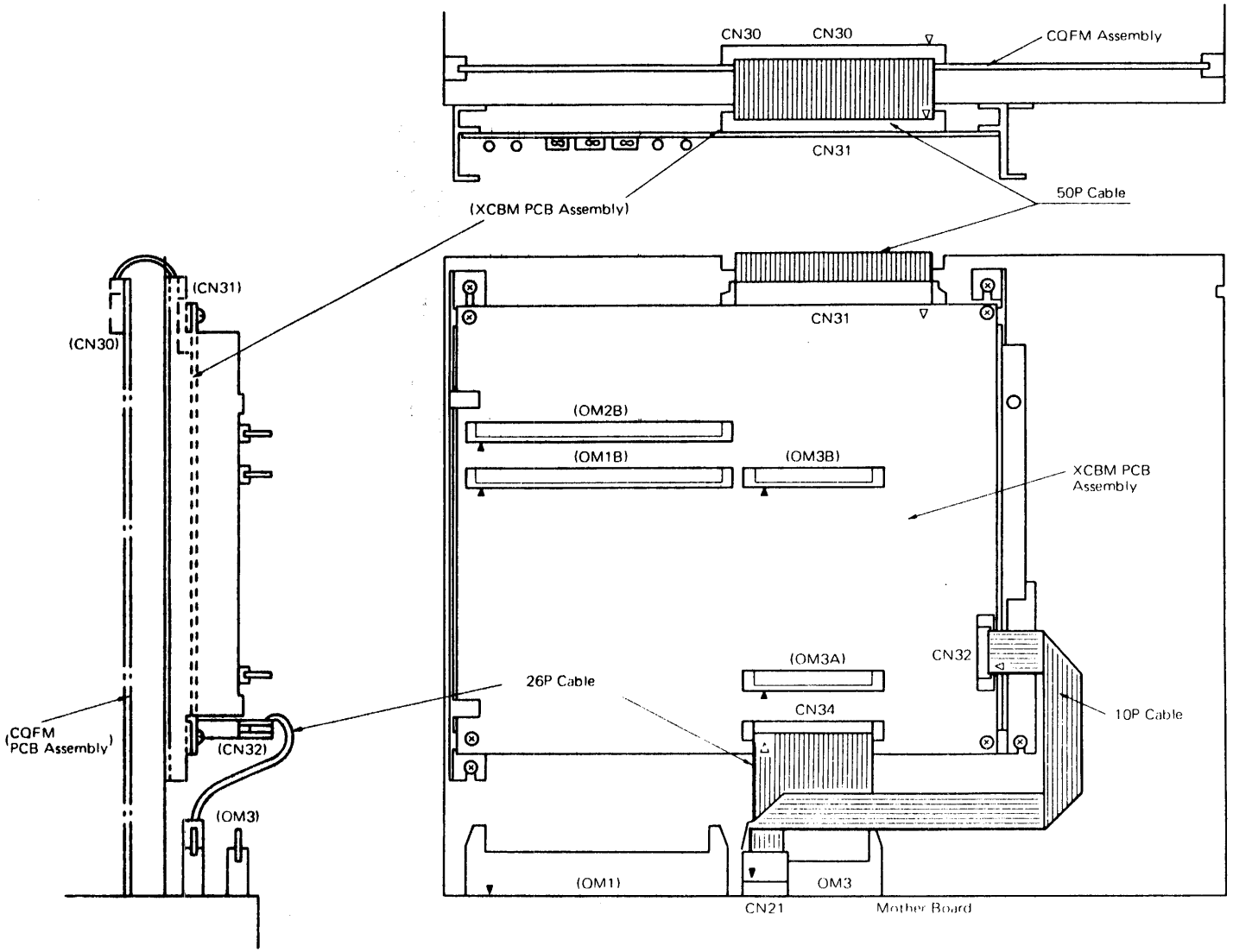


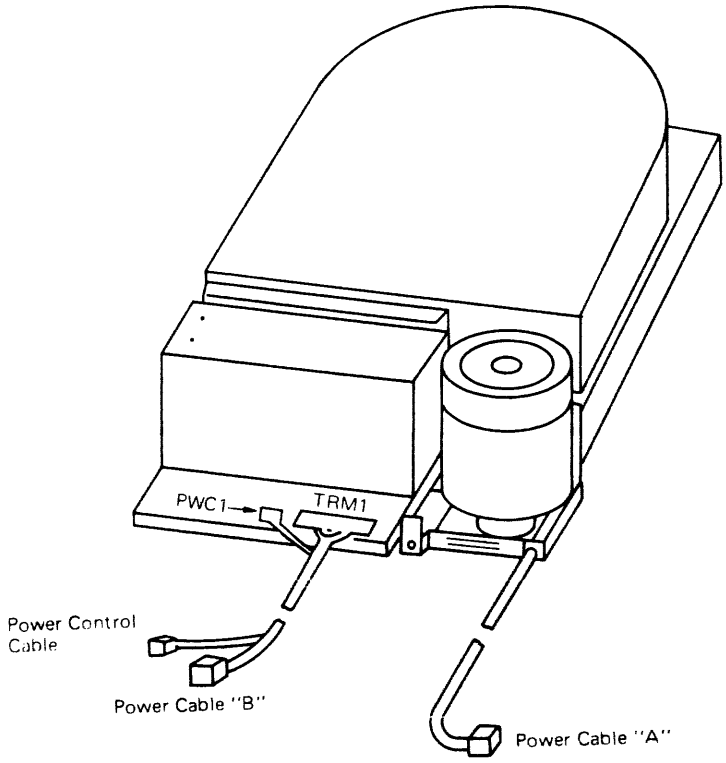
Figure 3-4-10 Dual Port Internal Cabling

3.5 CABLING

3.5.1 Power Cable

The power cable consists of an AC power supply "A" cable and a DC power supply "B" cable. The "A" cable supplies power to drive the spindle motor and brake, and blower motor, and the "B" cable supplies DC operating power to the logic and analog circuits.

The power cable connections are given in Figure 3-5-1 and Table 3-5-1.



(This figure is referred to when connectors are used.)

Figure 3-5-1 Power Cables

Table 3-5-1 Power Cables

Cable	Pin Assignment	Wire Mark	Voltage	AWG No.	Wire Color	Connector
"A"	1	AC-A1	AC Input A1	AWG 18	White/Orange	Plug (AMP) 1-480708-0
	3	AC-A2	AC Input A2	AWG 18	White	
	4	*AC-B1	AC Input B1	AWG 18	White/Orange	
	6	*AC-B2	AC Input B2	AWG 18	White	
	5	FG	FG	AWG 18	Green/Yellow	
	7	ALM	ALARM	AWG 20	Grey	Contact (AMP) 350550-2
	9	ALM	ALARM	AWG 20	Yellow	
	10	+24V	DC+24V	AWG 16	Red	
	12	0V	0V	AWG 16	Black	
"B"	5	+5V	DC+5V	AWG 14	Red	Plug (AMP) 1-480710-0
	6	0V	0V	AWG 16	Black	
	1	+12V	DC+12V	AWG 18	Red	
	2	0V	0V	AWG 16	Black	Contact (AMP) 350550-1 (3-6P) 350-551-3 (1.2P)
	7	-12V	DC-12V	AWG 18	Blue	
	8	0V	0V	AWG 16	Black	

*Note: When AC input is 220V/240V, AC-B input should be nominal AC 100V.

Table 3-5-2 Power Control Connector (CN1)

Pin Assignment	Signal	Wire Color	AWG No.	Connector
1	*RDY1	Yellow	AWG 20	
2	*RDY2	Yellow	AWG 20	Plug (AMP) 1-480706-0
3	*RDY3	Yellow	AWG 20	
4	Pick In	Black	AWG 20	
5	Hold	Black	AWG 20	
6	Pick Out	Black	AWG 20	Contact (AMP) 350550-7
7	0V	Yellow	AWG 20	
8	0V	Yellow	AWG 20	

The power cable "A" and "B" are furnished with the unit.

"A" cable is for AC power and "B" cable is for DC power with the power Control connector.

Table 3-5-3 Power Cable List

Description	Specification
"A" Power Cable with connector	B660-1055-T017A
"B" Power Cable with connector	B660-1055-T018A

The cable length shall be specified in 1, 2, 3 and 4m lengths.

Example: B660-1055-T017A#L3R003

3.00×10^3 mm = 3.0m

3.5.2 Connecting with Optional Power Supply

3.5.2.1 AC Input Select

The optional power supply unit for USA version (B14L-0300-0018A) can be operated under AC 100V or AC 115V, and the power supply unit for European version can be operated under AC 220V or AC 240V.

Therefore, before connecting with power supply, they must be selected by the transformer taps inside the unit according to site AC input.

The selected AC voltage before shipping is labelled on the unit.

AC voltage select procedure is as follows:

(1) Remove the cover by loosening screws as shown in Figure 3-5-2 (1).
After removing of the cover, the terminal is visible as shown in Figure 3-5-2 (2)/(3).

(2) AC voltages are indicated nearby the terminal.
The wire from N.F.B. must be connected to the terminal according to site AC input.

(3) Fix the cover by fastening the screws.

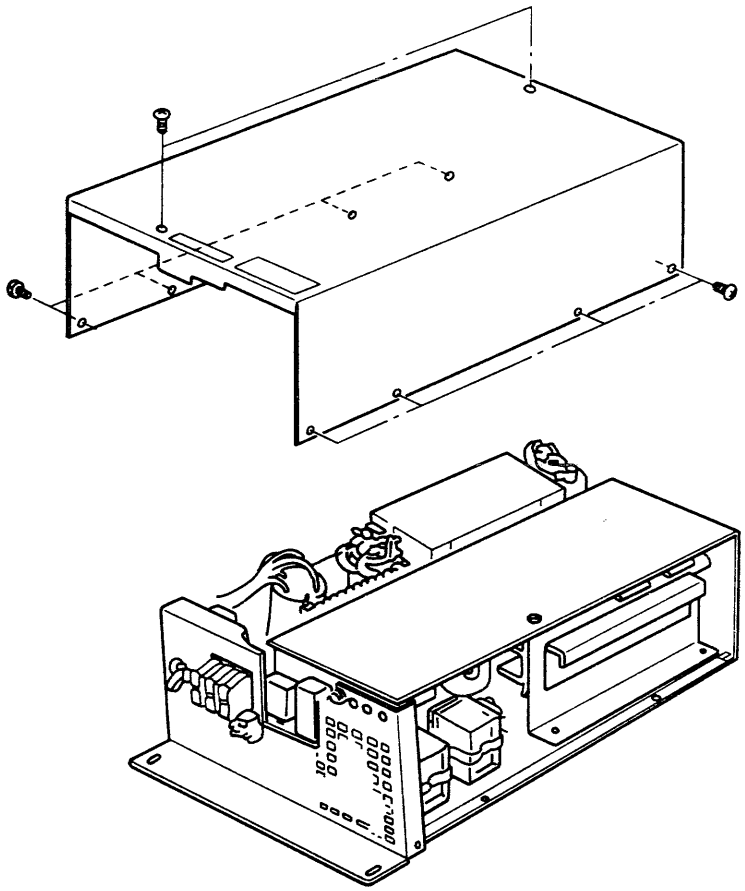


Figure 3-5-2 AC Input Select (Sheet 1 of 3)
(Removal of the cover)

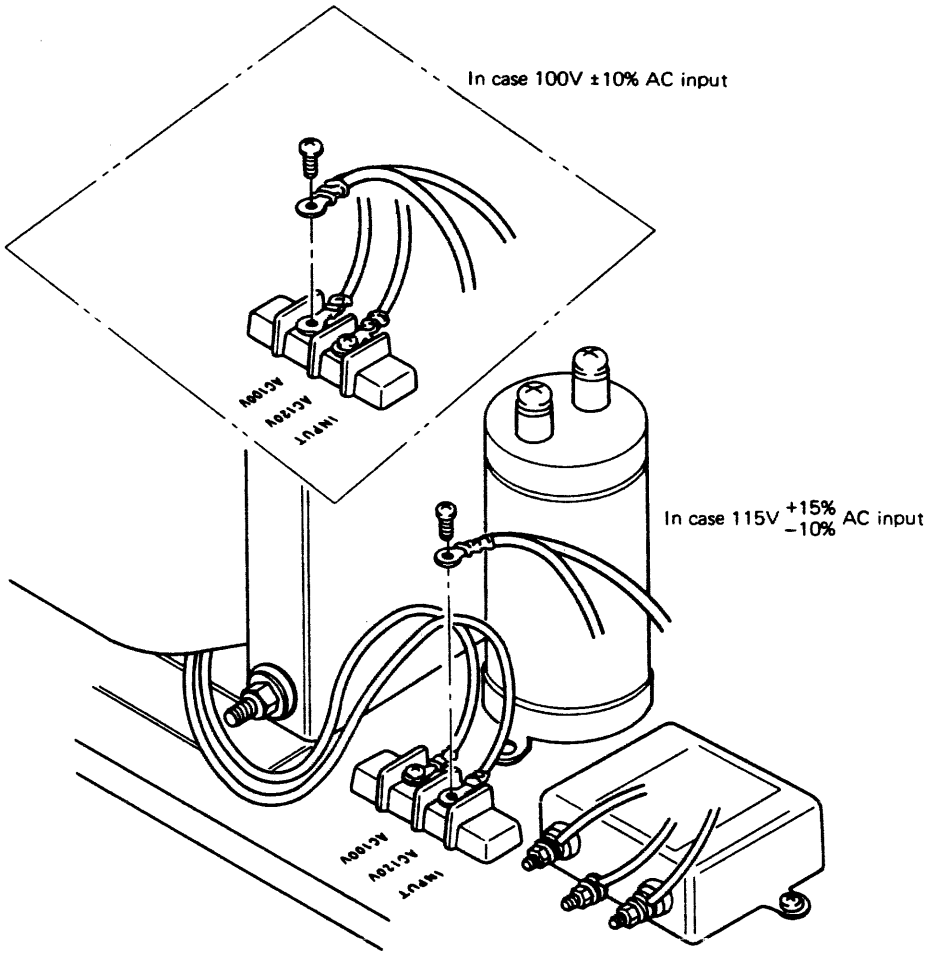


Figure 3-5-2 AC Input Select (Sheet 2 of 3)
USA Version

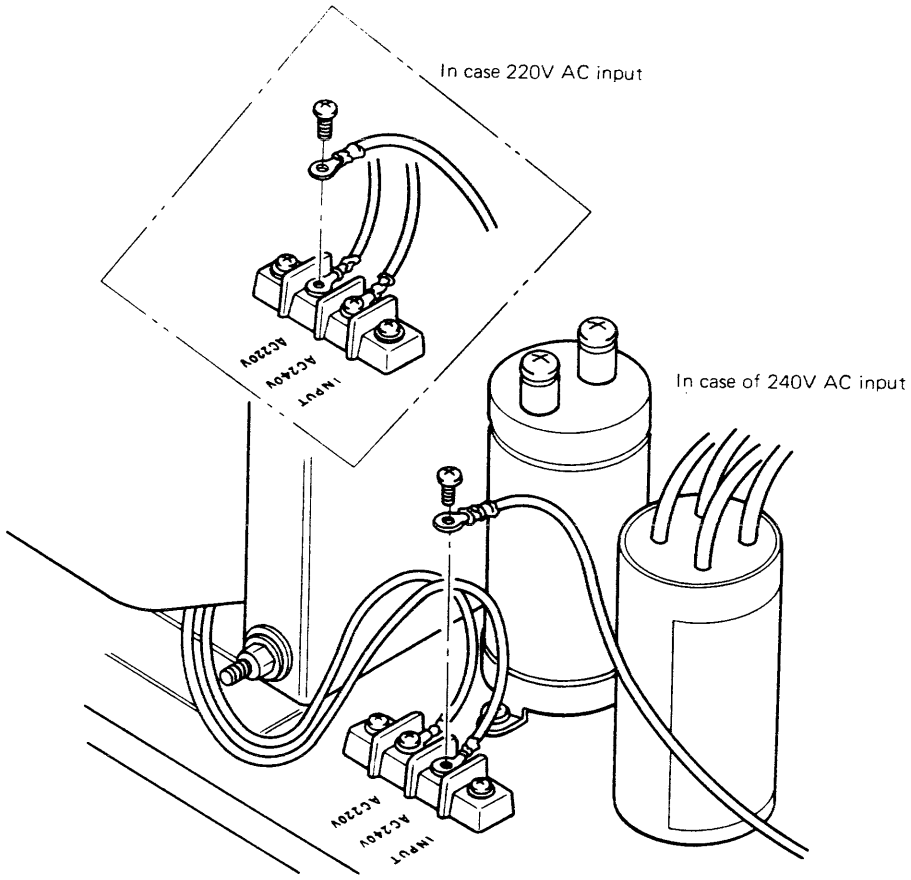


Figure 3-5-2 AC Input Select (Sheet 3 of 3)
European Version

3.5.2.2 +24V DC Select

The optional power supply unit can output +24V DC or −32V DC, however, FDU M228X must be operated by +24V DC.

Confirm that the +24V DC is selected by switch on the rear side as shown in Figure 3-5-3.

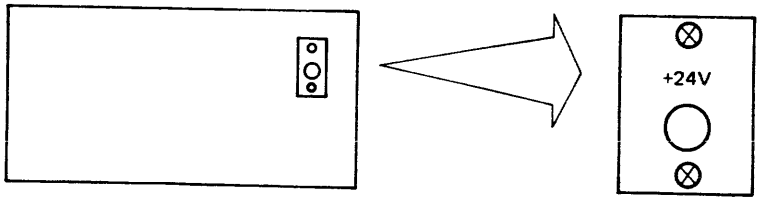
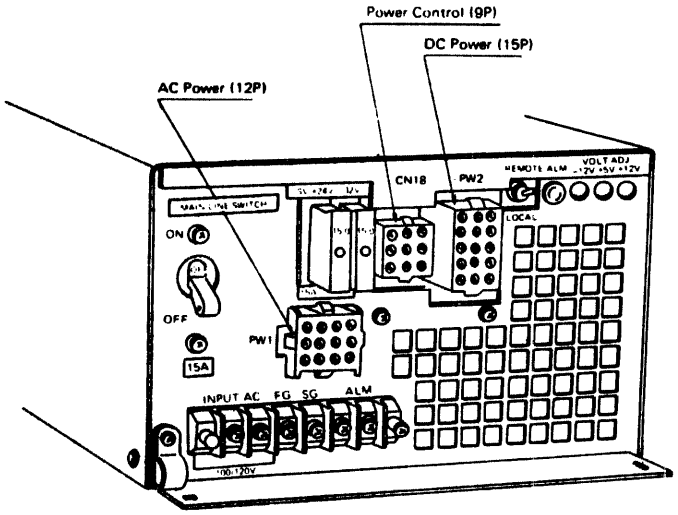


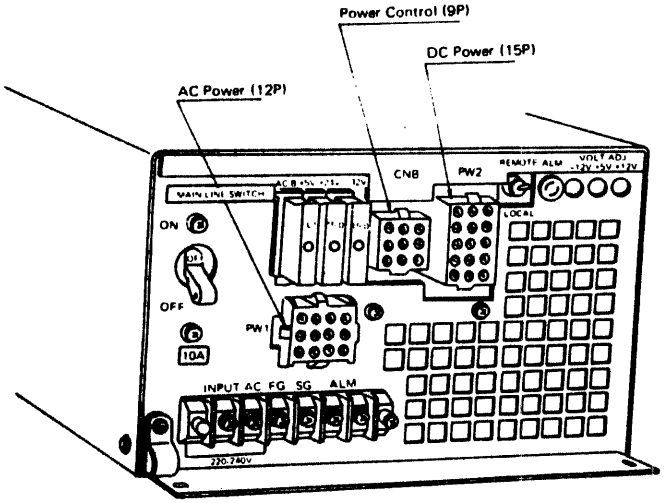
Figure 3-5-3 +24V DC Select

3.5.2.3 Power Cable Connection

The FDU M228X provides three power cables, AC cable, DC cable and Power Control cable. AC power connector (12P) is connected to PW1, DC power connector (15P) to PW2, and Power Control connector (9P) to CN18 respectively as shown in Figure 3-5-4.



(1) USA Version Power Supply Unit



(2) European Version Power Supply Unit

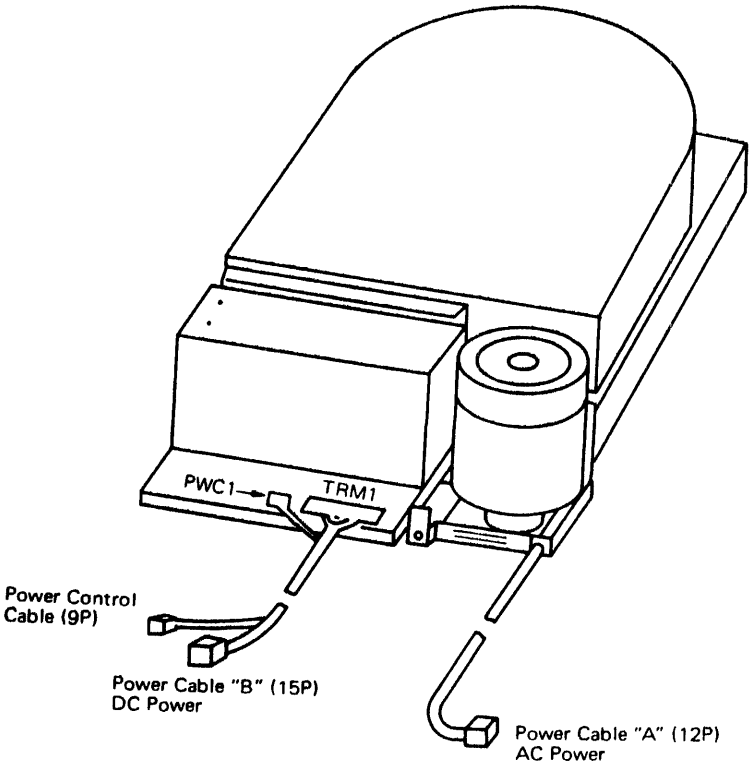


Figure 3-5-4 Power Cable Connection

3.5.2.4 DC Voltage Adjustment

After connecting the power cables between FDU M228X and a power supply unit, adjust the each DC voltage on TRM2 terminal to +5V and ±12V by specified potentiometers.

3.5.3 Interface Cabling

Interface cables include cable "A" (60P) for control signals and cable "B" (26P) for data signals.

Cables are connected the system in the star connection mode or the daisy-chain mode as shown in Figures 3-5-5, and 3-5-6.

For the star connection mode, the line termination for cable "A" is necessary for every unit.

For the daisy-chain mode only the last unit requires a Line Terminator.

The grounding wire of the Line Terminator must be connected to a signal ground TRM1-2.

In the case of dual-port operation, the interface cables from the channel-A and B controllers are also connected the system in the star connection mode or the daisy-chain mode as shown in Figures 3-5-7 and 3-5-8.

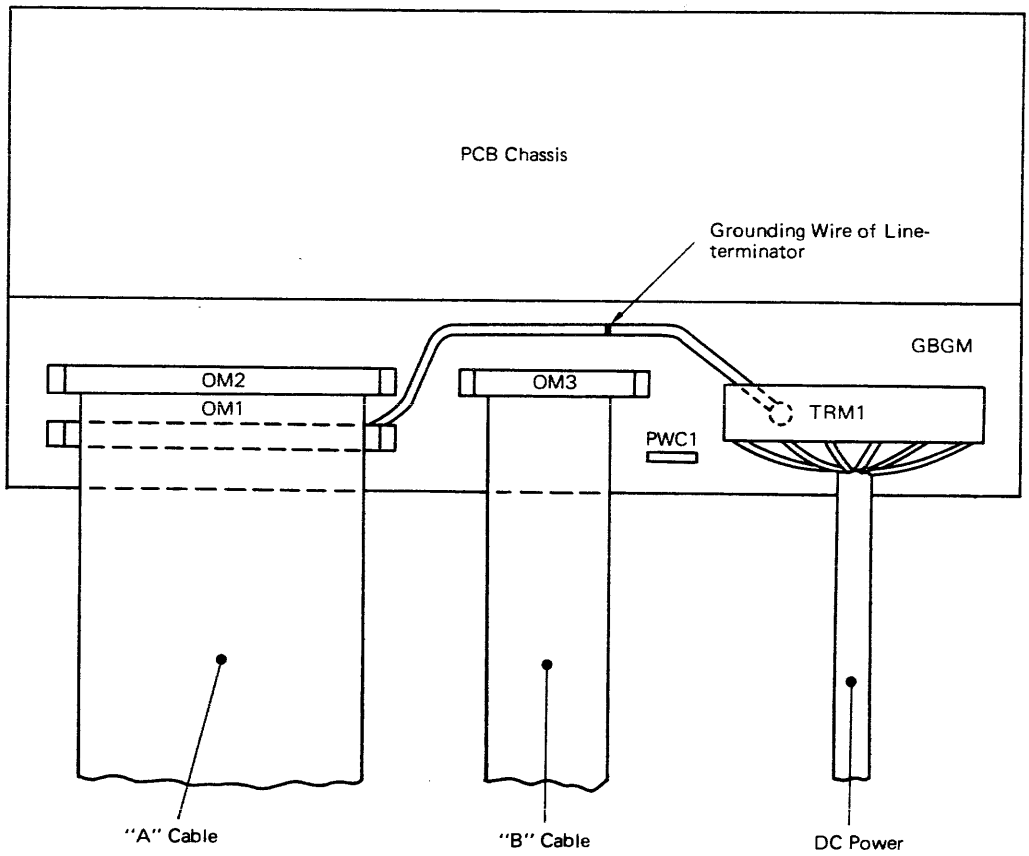
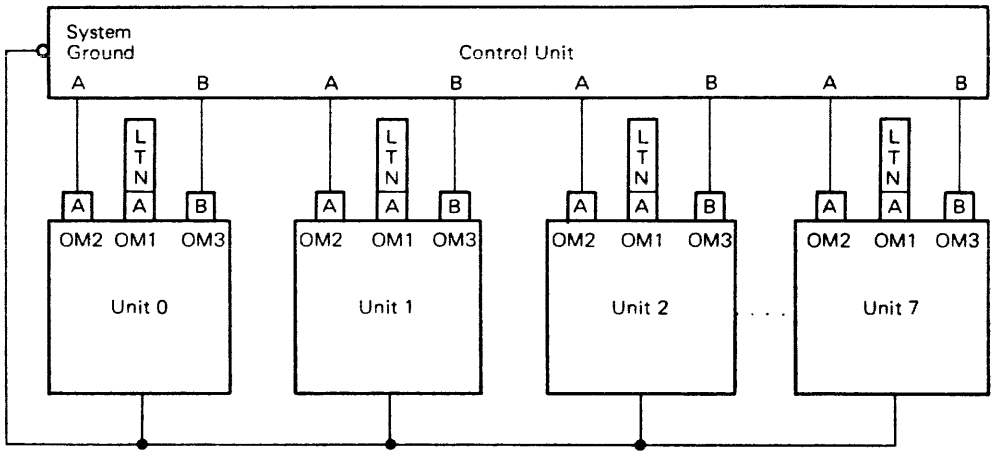
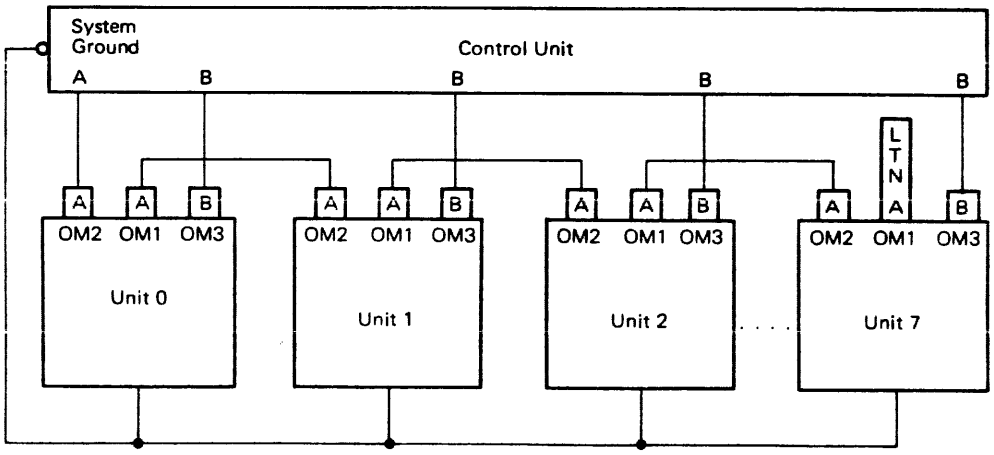


Figure 3-5-5 Interface Cabling (Single Port)



Star-Cabled Configuration



Daisy-Chain-Cabled Configuration

Figure 3-5-6 System Interface Cabling (Single Port)

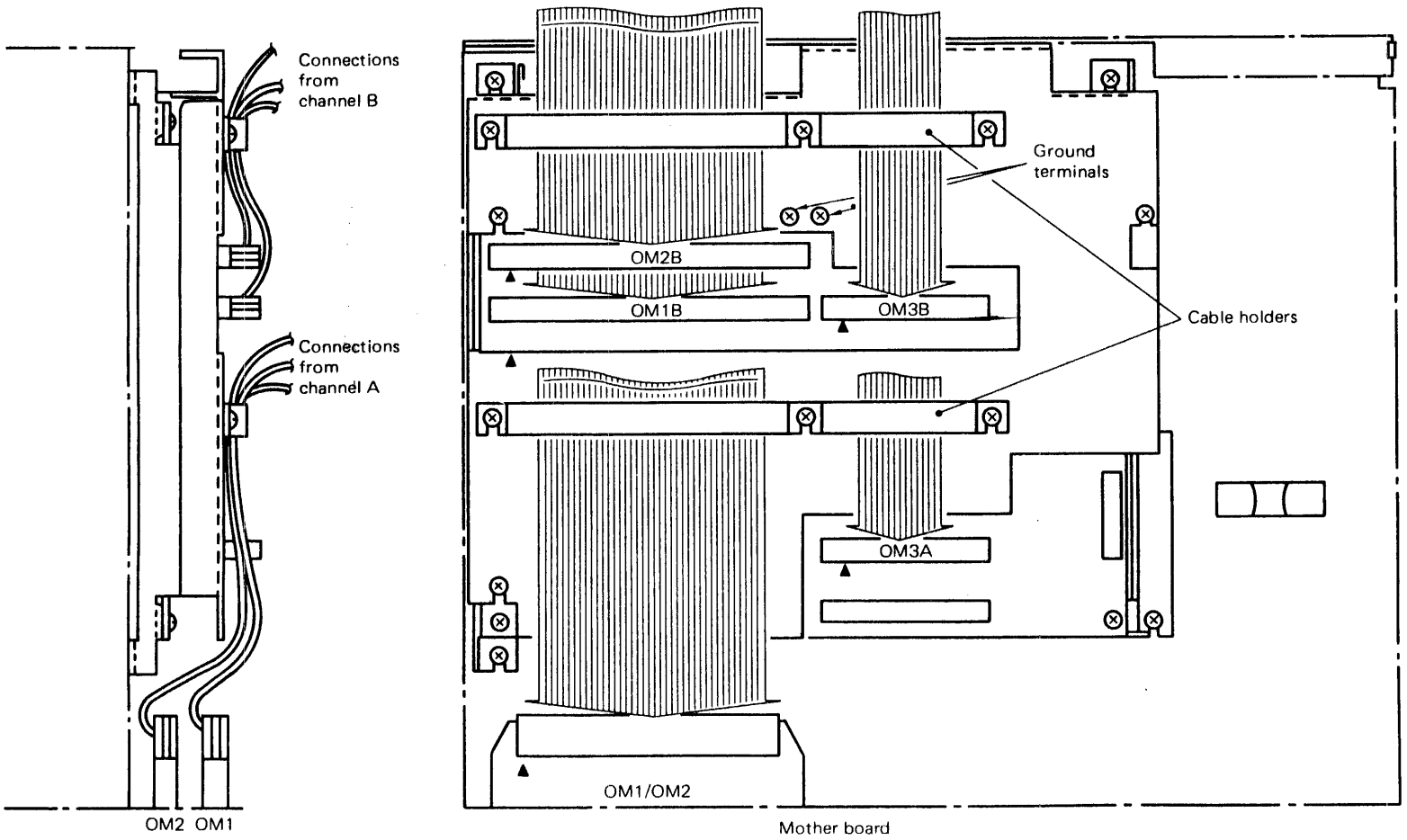
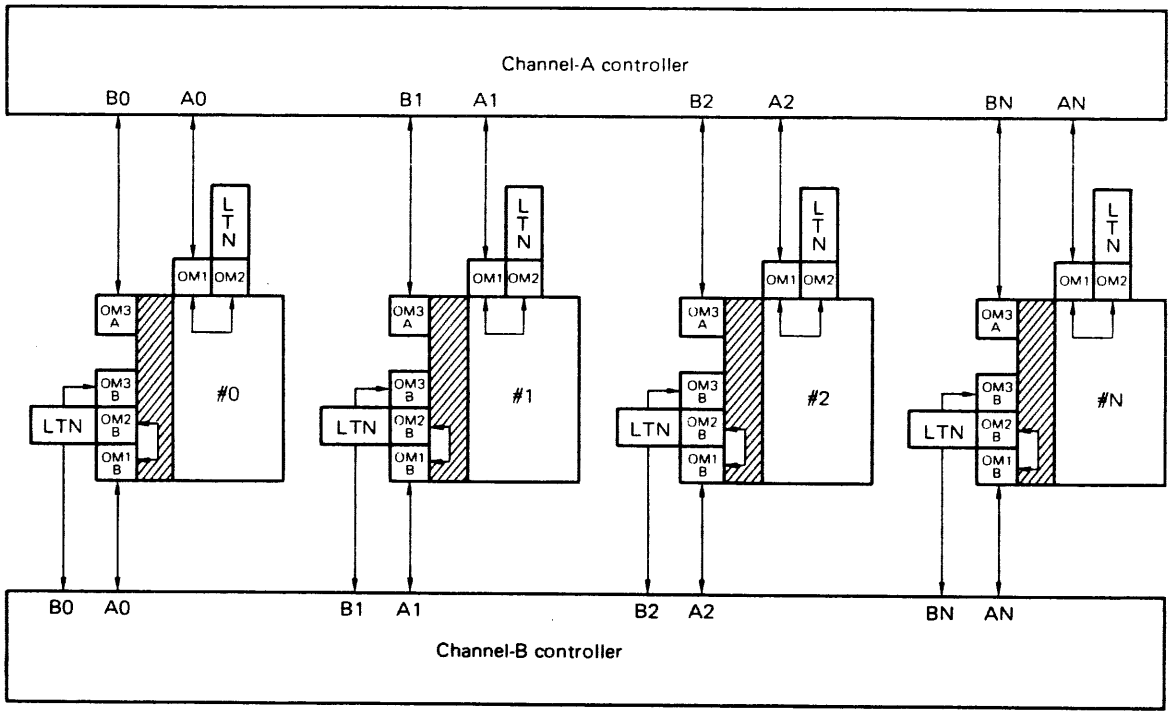
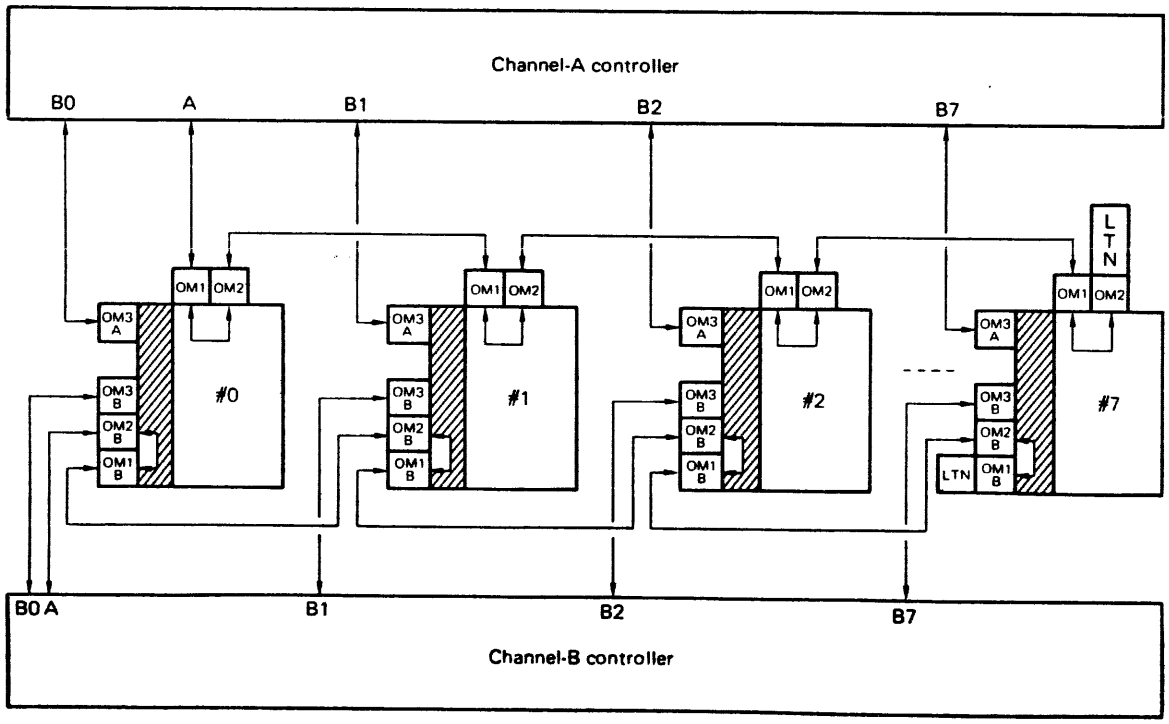


Figure 3-5-7 Interface Cabling (Dual Port)



(a) Star Connection

Note: Hatched areas denote dual port options.



(b) Daisy Chain

Figure 3-5-8 System Interface Cabling (Dual Port)

3.5.4 System Grounding

(1) The frame ground (FG) and signal ground (SG) within FDU are separated. If the FG and SG connection is required on the system, connect the grounding cable as shown in Figure 3-5-9, or if the system ground is required between the system and FDU, serve the ground conductor to the GND terminal.

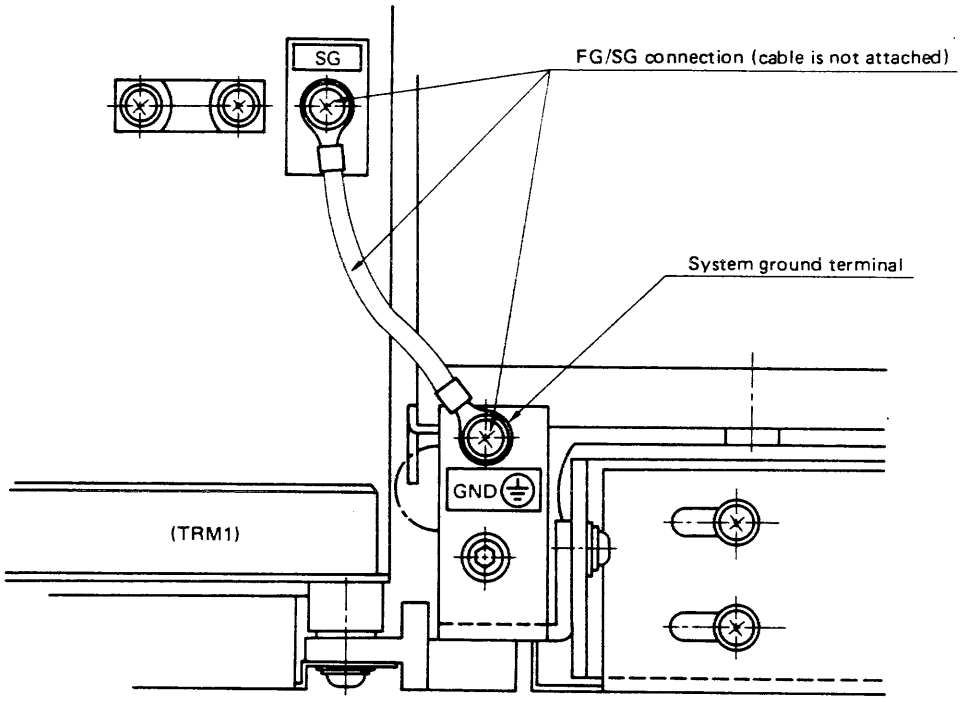


Figure 3-5-9 Ground terminal on the unit

(2) The FG and SG terminals are provided with the optional power supply unit as shown in Figure 3-5-4. Connecting or disconnecting between FG and SG on the power supply unit can be performed according to system power distribution and system ground requirement.

(3) When the interface cable is longer than 3m (10 feet), an auxiliary grounding cable should be connected among the control unit and disk units.

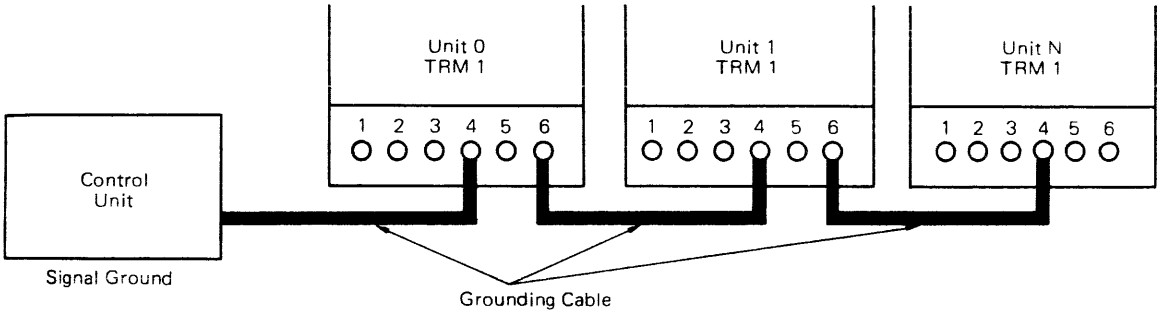


Figure 3-5-10 System Grounding

3.5.5 Mode Select Setting

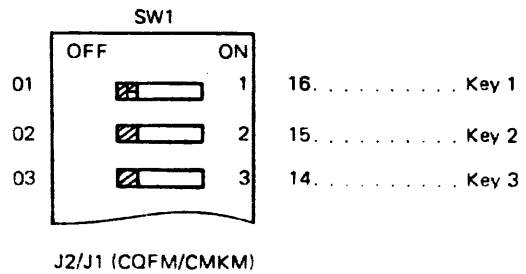
When the FDU M228X is installed to the system, the customer must set the following modes according to system requirements, that is, Disk Logical Unit Number, Tag 4/5 Enable and Sector Mode on CQFM/CMKM PCB assembly, Sector Counting on VOFM PCB assembly, and Mount Direction on the PCB Chasis (GBNM/GBGM PCB) assembly.

3.5.5.1 Disk Addressing

Disk Logical Unit Number 0 to 7 is selectable on SW1 at location J2/J1 on the CQFM/CMKM PCB assembly. Set the desired disk address with three keys on SW1 using binary code as shown in Table 3-5-4.

Table 3-5-4 Disk Addressing

Disk Address	Key 1 2^0	Key 2 2^1	Key 3 2^2
0	OFF	OFF	OFF
1	ON	OFF	OFF
2	OFF	ON	OFF
3	ON	ON	OFF
4	OFF	OFF	ON
5	ON	OFF	ON
6	OFF	ON	ON
7	ON	ON	ON



3.5.5.2 Sector Mode

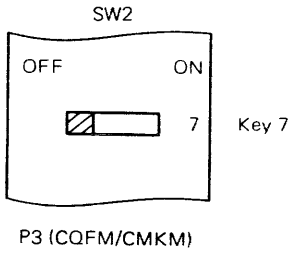
The customer can select Hard Sector mode (1 to 128 sectors) or Variable Soft Sector using Key 7 on SW2 at location P3 on the CQFM/CMKM PCB assembly according to Table 3-5-5.

In the case of Hard Sector, the customer must set the number of sectors per disk revolution as described in 3.5.3.5.

In the case of Variable Soft Sector, setting the number of sectors per disk revolution has no effect.

Table 3-5-5 Sector Mode

Sector Mode	Key 7
Hard Sector	OFF
Variable Soft Sector	ON

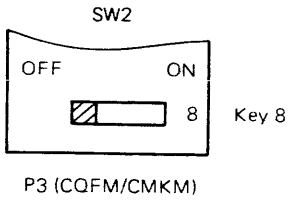


3.5.5.3 Tag 4/5 Enable

FDU M228X provides optional Tag 4 and Tag 5 functions, however, the customer may disable or enable these functions using Key 8 on SW2 at location P3 on the CQFM/CMKM PCB assembly. Disabling the Tag 4/5 functions inhibits the receivers of Tag 4 and Tag 5 on the interface.

Table 3-5-6 Tag 4/5 Enable

Tag 4/5	Key 8
Disable	OFF
Enable	ON



3.5.5.4 Sector Counting

Sector count configuration switches, SW1 and SW2, are located at L2 and L1 respectively on the VOFM PCB assembly. Each key of SW1 and SW2 represents the binary powers of the Byte Clock as shown in Table 3-5-7.

Table 3-5-7 Sector Counting Keys

SW1 Key No.	Value	SW2 Key No.	Value
1	1	1	128
2	2	2	256
3	4	3	512
4	8	4	1024
5	16	5	2048
6	32	6	4096
7	64	7	8192

SW1 and SW2 keys must be set according to the number of bytes per sector. Knowing that the number of bytes possible on a track equals 20,480, any sectoring requirement from 1 to 128 sectors per track can be configured using the following formula:

EXAMPLE

(Calculations for 9 Sectors)

(1) $\frac{20{,}480}{\text{Number of sectors}}$ = Number of Bytes per sector

$\frac{20{,}480}{9} = 2{,}275.555$

(2) If the above calculation results in a remainder, truncate the remainder and add one to the integer portion of "number of bytes per sector"

$2{,}275 + 1 = 2{,}276$

(3) Configure SW1 and SW2 to "number of bytes per sector" less one to allow for Sector Counter Reset Clock.

$2{,}276 - 1 = 2{,}275$

$2{,}275 = 2{,}048 + 128 + 64 + 32 + 2 + 1$

Key # 5 1 7 6 2 1

SW2 SW1

(4) To determine how many bytes (if any) the last sector of each track will be short, multiply "number of bytes per sector" by "number of sectors" and subtract 20,480.

$2{,}276 \times 9 = 20{,}484$

$- 20{,}480$

Last sector short 4 bytes

Table 3-5-8 Commonly Used Sector Configurations

NO SECTORS	S1							S2							BYTE/SECT	LAST SECTOR SHORT
	1	2	3	4	5	6	7	1	2	3	4	5	6	7		
4	1	1	1	1	1	1	1	1	1	1	0	0	1	0	5,120	0
8	1	1	1	1	1	1	1	1	1	0	0	1	0	0	2,560	0
12	0	1	0	1	0	1	0	1	0	1	1	0	0	0	1,707	-4
16	1	1	1	1	1	1	1	1	0	0	1	0	0	0	1,280	0
24	1	0	1	0	1	0	1	0	1	1	0	0	0	0	854	-16
32	1	1	1	1	1	1	1	0	0	1	0	0	0	0	640	0
64	1	1	1	1	1	1	0	0	1	0	0	0	0	0	320	0
128	1	1	1	1	1	0	0	1	0	0	0	0	0	0	160	0

3.5.5.5 Mount Direction Select

When the unit without the optional front panel is installed vertically, V-H switch on the PCB chassis (GBNM/GBGM PCB assembly) should be set to the "V" position.

In the other case, V-H switch should be set to the "H" poisiton. Refer to Figure 3-5-11.

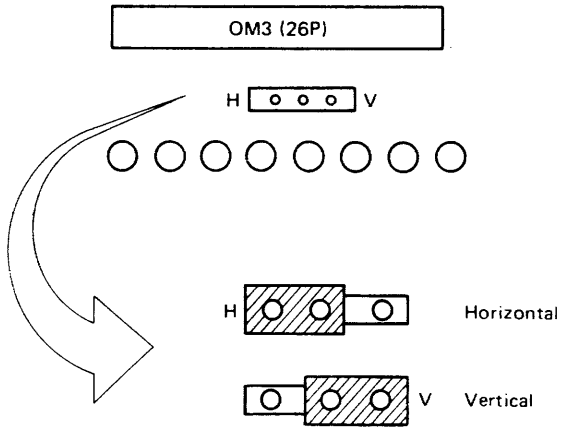


Figure 3-5-11 Mount Direction (V-H Switch)

3.6 SHIPPING

Perform the following operations when the unit is to be shipped after mounting with a system:

(a) Lock the spindle (refer to 3.4.3)

Caution: Rotate spindle in the direction indicated only

(b) Lock the actuator (refer to 3.4.4)

(c) Lock the motor (refer to 3.4.5)

(d) Fasten the unit; attach the vertical type mounting bracket to the cabinet so that excessive force is not aplied to the rubber shock isolators. Process so that shock exceeding 5G is not applied to the unit during shipment.

When the unit is shipped by itself, the same operations (a to c) are required before packing into the proper carton.

3.7 STORAGE AND REPACKING

The FDU M228X shipping carton is a reusable cardboard carton having a special double construction. When reshipping the unit, repack it in the original carton or a carton having equivalent functions.

When the environment is severe and the unit is to be stored for an extended period of time, it should be stored in the packed state.

Units can be stacked three cartons high.

When storing unpacked units, avoid dusty locations and locations where the environmental changes are extreme.

Section 4

Theory of Operation

4. THEORY OF OPERATION

4.1 GENERAL DESCRIPTION

The description of operation of the Fixed Disk Unit is divided into three parts. The first part describes the main assemblies of the unit. The second part describes the magnetic heads and magnetic disks. The third, and last part describes the interface, servo circuit, R/W control, and other electronic controls.

4.2 ASSEMBLIES

4.2.1 Disk Enclosure (DE)

The Disk Enclosure is a completely sealed unit containing the disks, spindle, actuator, and heads. Each of these are visible from the outside through a plastic cover. The DE is sealed at the factory and must not be opened in the field.

The DE is treated as one maintenance part.

The Read/Write PCB is mounted on the DE, but is an independent part.

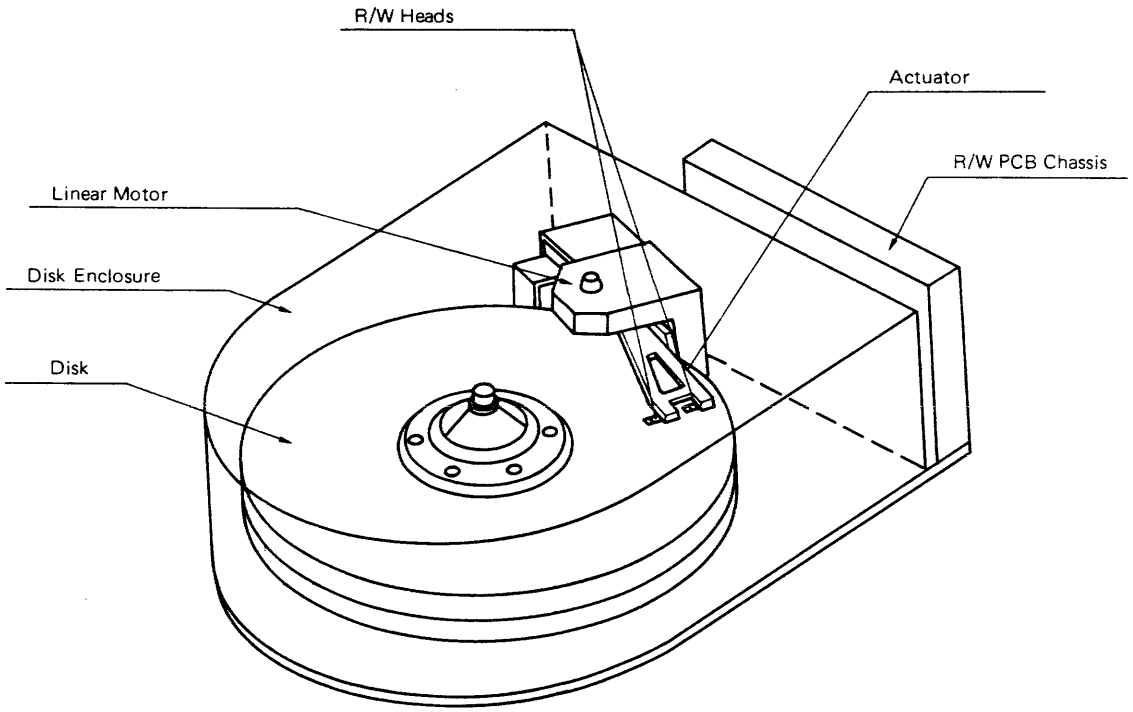


Figure 4-2-1 Disk Enclosure

4.2.2 Spindle Assembly

The disk spindle is mounted in the DE housing in the bottom of the disk enclosure. The housing is sealed to prevent air from entering through the bearings. A hub is attached to the top of the spindle, and disks (recording media) are clamped to the hub. A pulley is attached to the bottom of the spindle and is driven by the spindle drive motor with a flat belt. The spindle is grounded through a Spindle Brush mounted on the Grounding Plate.

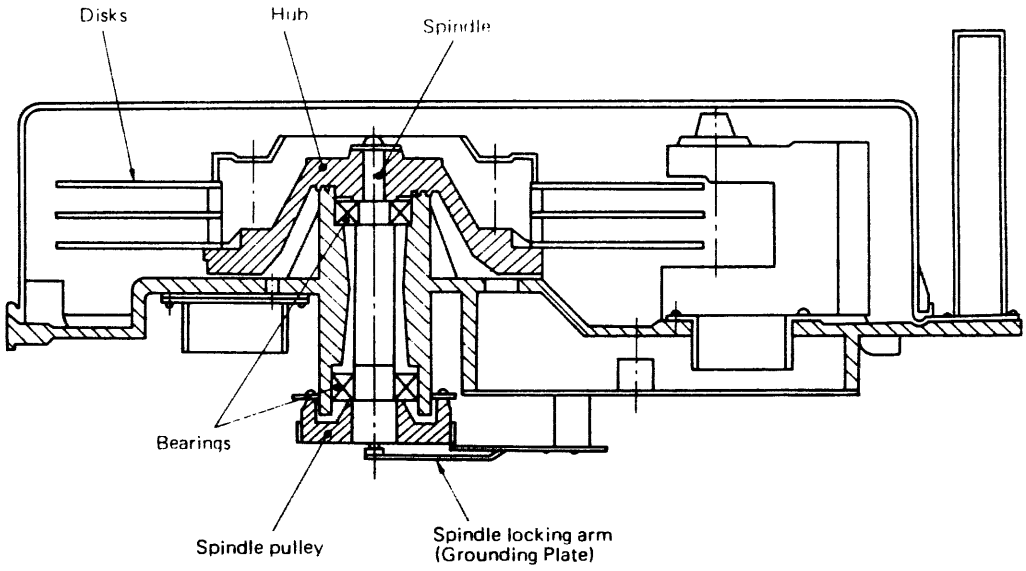


Figure 4-2-2 Spindle Assembly

4.2.3 Spindle Drive Motor and Brake

As this fixed-disk unit uses contact start/stop heads, the head-disk contact time must be minimized during rotation. Therefore, the disk drive system uses a thermally protected high torque motor for quick acceleration to nominal rotational speed and a brake for quick stopping.

Should overheating occur, the AC power to the motor is automatically disconnected and the rotational speed is gradually decreased. In this case the alarm signal is not sent to the power unit. When the temperature drops to an acceptable level, the motor will recover to nominal speed.

A flat belt connects the spindle drive motor to the spindle.

The motor is mounted so as to pivot, and sufficient tension is supplied to the belt by pulling the motor with a spring.

A brake is mounted at the top of the motor. This brake is actuated when the DC +24V is turned off. When the current at the brake coil is turned off, the brake pad is pushed to the brake plate by a spring and stops the motor.

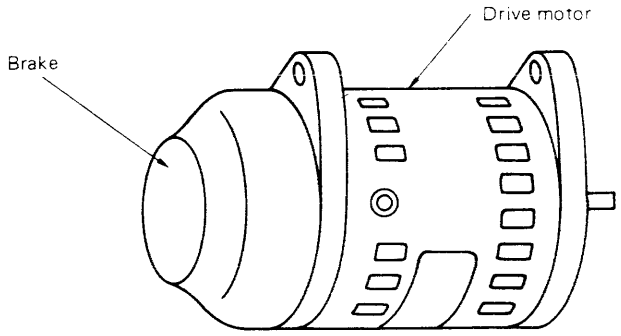


Fig. 4-2-3 Disk Spindle Motor and Brake

4.2.4 Actuator Arm Assembly

A rotary type actuator with low power consumption and low heat dissipation is used to move the data heads and servo head to the specified cylinder along a circular arc.

A moving coil is attached to the other end of the actuator arm and moves freely between fixed permanent magnets without contact. When current is applied to the coil, interaction occurs between the coil and magnets and the actuator moves around the pivot.

The actuator performs the following types of motion, which are controlled by servo feedback current from the servo head:

(1) Positioning
Heads are moved to the specified cylinder address.

(2) Track Following
Heads follow the specified track to prevent mispositioning from disturbances such as shock, vibration, or temperature change.

The servo head is located on the lower surface of the bottom disk. Servo data is written on the outer recording area of this disk.

This data is used as a control signal for the actuator, that is, it is used as a track crossing signal for positioning or as a track following signal.

The heads are in contact with the disk surfaces during start and stop (C.S.S.) at a fixed position called the landing zone. This zone is outside the recording zone area. A magnet is used to pull or fix the actuator at this position. If no current is applied to the moving coil, the heads are fixed at the landing zone to prevent C.S.S. in the recording zones.

Once the disks attain the required rotational speed, an initial seek instruction is issued. Current then flows in the coil and the heads are released from the landing zone and moved to the recording zones.

4.2.5 Actuator Lock, Spindle Lock

When the disks are stopped, the heads are in contact with the disks. The spindle and actuator are fixed with both the spindle lock and actuator lock for disk and head protection during maintenance, replacement, and transportation of the DE. (See Figures 3-4-4 and 3-4-5.)

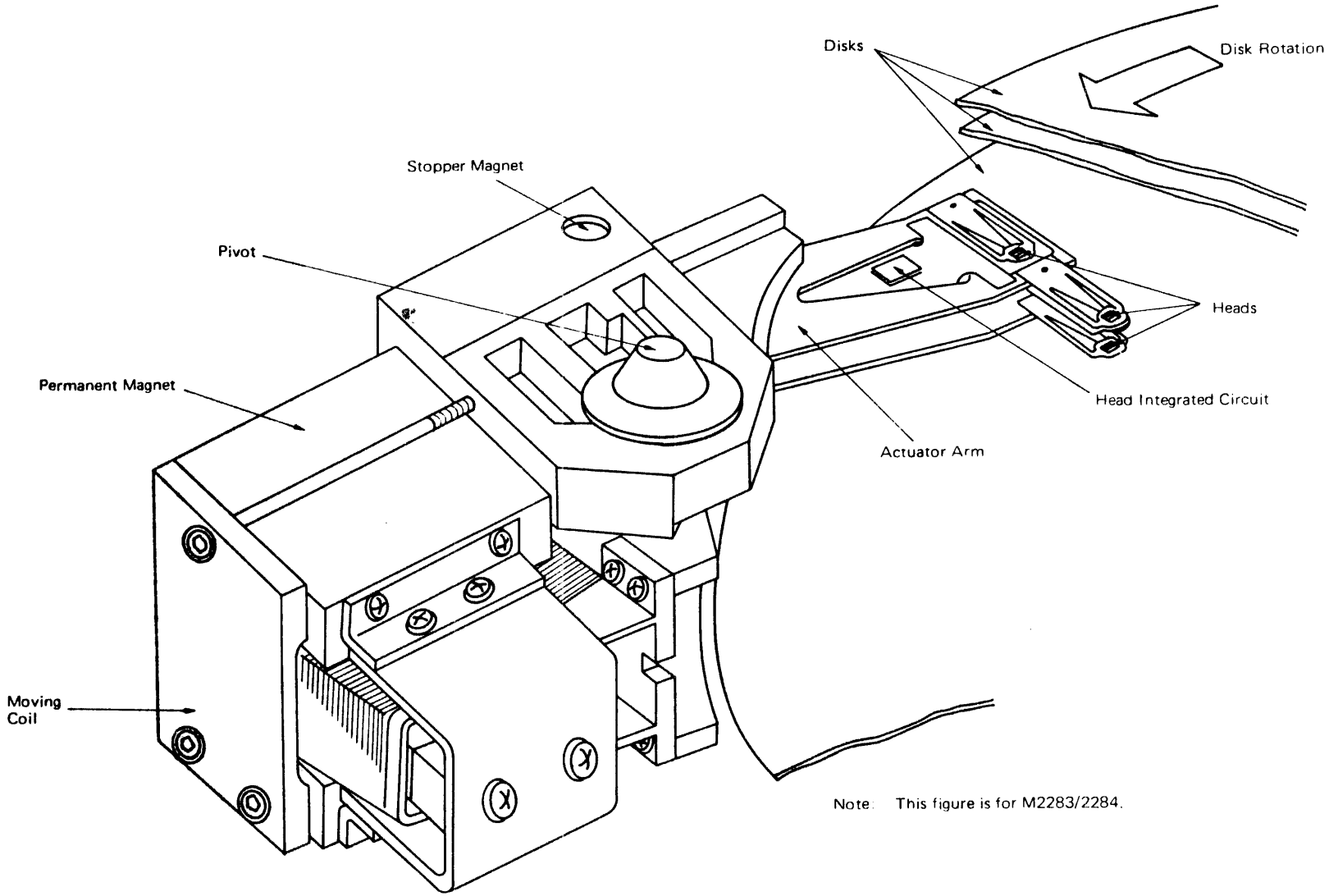


Figure 4-2-4 Actuator Arm Assembly

4.2.6 Air Circulation in DE

As the C.S.S. head used in this disk unit has a very low flying height (approximately 0.45μm) head crashes could be caused by microscopic foreign particles. To keep the inside of the DE clean, this enclosure is completely sealed and clean air is supplied through two filters. One filter is used for external air intake, while another filter is used as a re-circulation filter to keep the air inside the DE clean.

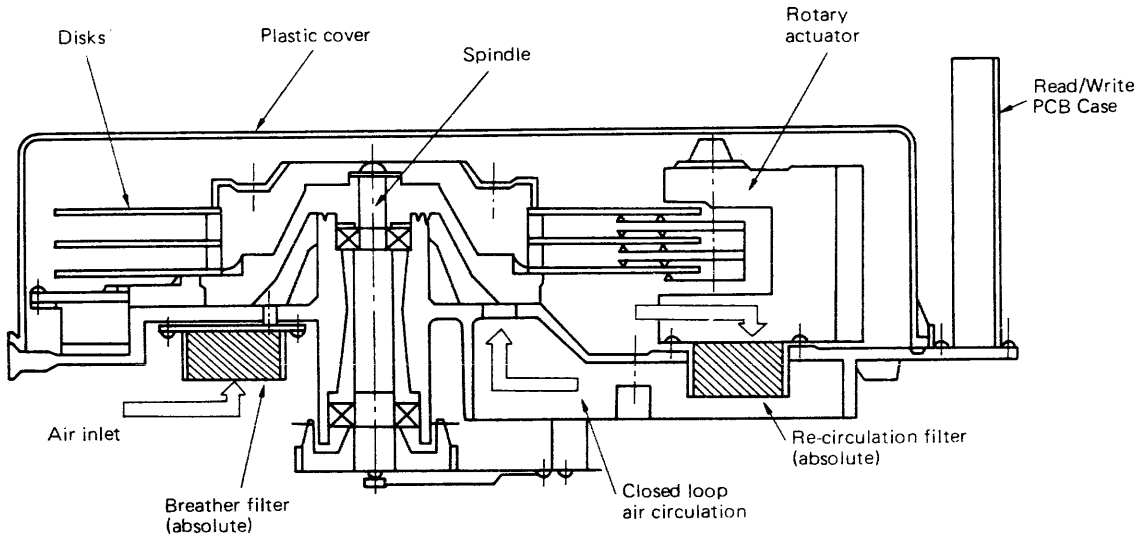
The breather filter is used for the following purposes:

(a) Prevention of negative pressure in the vicinity of the spindle when the disk begins to rotate.

(b) Prevention of dust intake when the air in the DE contracts due to a temperature difference between the DE and its environment.

The re-circulation filter, attached to the closed loop duct in the DE, is used to keep the air free of foreign particles. When a pressure difference is caused in the DE by the rotation of the spindle, the air in the DE circulates through the closed loop. Because it continually passes through this filter, the air is always kept clean.

These two filters can remove 99.97% of the dust particles (0.3 μm min.).



M2282 contains two disks in DE.

M2280 contains two disks in DE.

M2283 contains three disks in DE.

M2284 contains three disks in DE as shown in this figure.

Figure 4-2-5 Air Circulation inside DE

4.2.7 Sub-frame

The sub-frame is supported by four vibration isolating rubber supports (three rubber supports for the vertical type). The disk enclosure is mounted on this sub-frame with three bolts and nuts. The DE can be easily replaced by removing these three nuts.

The DE is insulated from the sub-frame to prevent any influence from noise and vibration.

The sub-frame contains a duct to supply air from the cooling blower to the R/W PCB and the control PCB's.

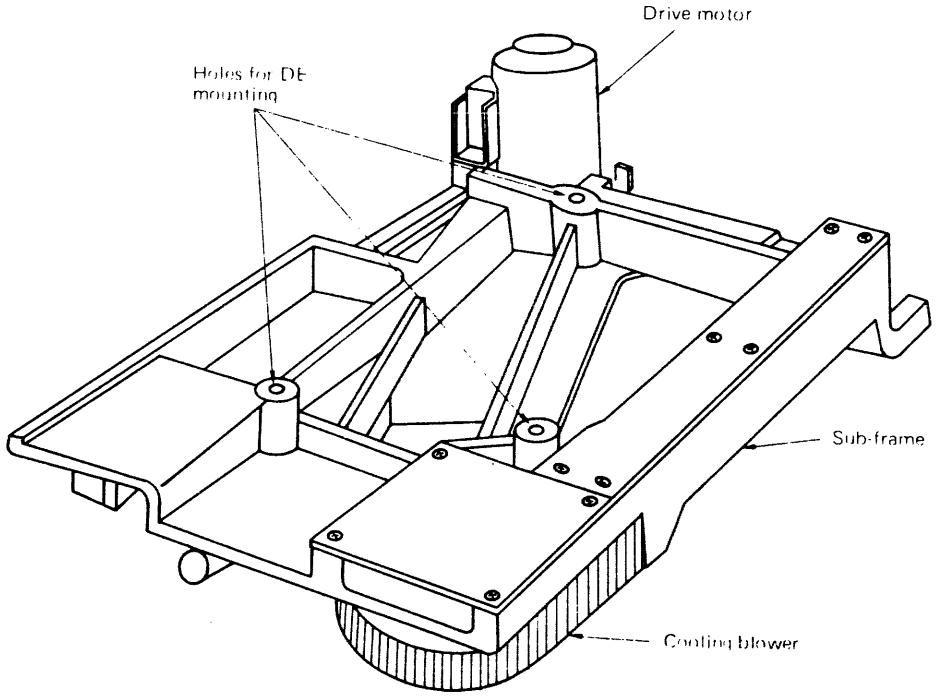


Figure 4-2-6 Sub-frame

4.2.8 Cooling

A cooling blower provides air to cool the printed circuit boards and motor. Cool air is always supplied from the front to the inside by this blower.

The air is sent through the duct in the sub-frame and divided into two channels. One cools the read/write printed-curcuit board, and the other cools the printed-circuit boards in the chassis, and then the motor.

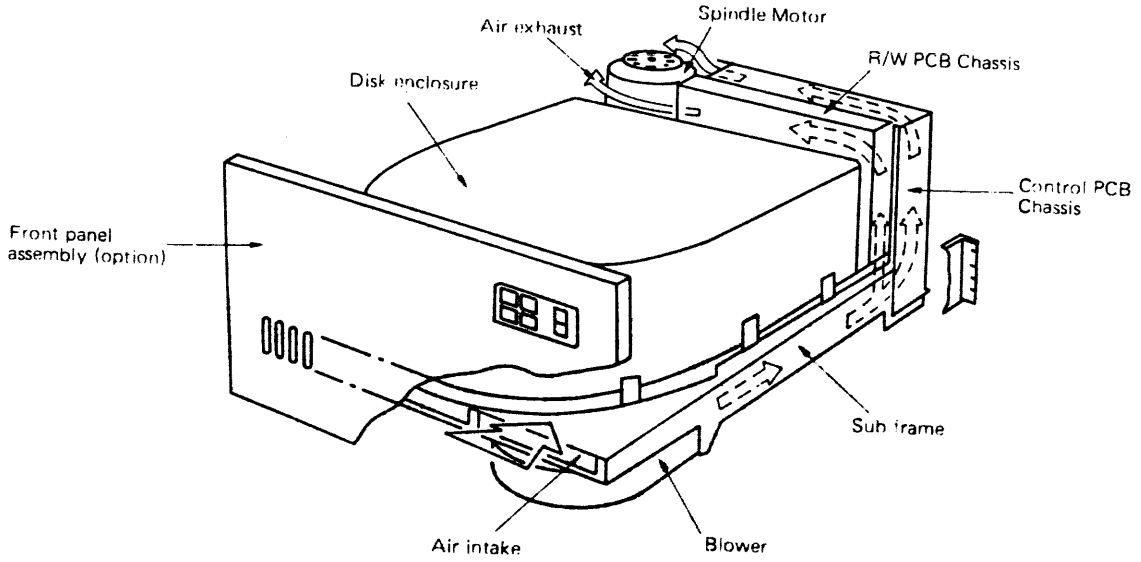


Figure 4-2-7 Cooling

4.3 MAGNETIC HEADS AND RECORDING MEDIA

4.3.1 Magnetic Heads

To accomplish high density recording, CONTACT START/STOP (C.S.S.) flying heads are employed. The heads fly on the surface air flow generated by the rotating disk. The C.S.S. system differs from the conventional rampl load system in that the heads are always over the recording media and rest on the disk surface when the disk is not rotating.

Therefore, the head and disk make contact, and the wear caused by this contact must be minimized. For thus reason, the C.S.S. type head is lightly loaded and the surface pressure is reduced by using a tapered flat slider such as that shown in Figure 4-3-2. The slider has 3 rails. The air intake end of the slider is tapered to obtain flying force by means of the air flow over the disk surface. Reads and writes are performed by a ferrite core at the rear of the head, the minimum flying height position.

There are two kinds of magnetic heads: access heads and fixed heads. These heads have the same construction but the access head has only one ferrite core whereas the fixed head has three ferrite cores.

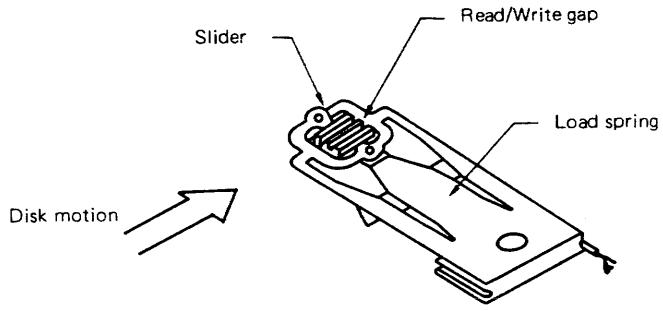


Figure 4-3-1 Read/Write Head

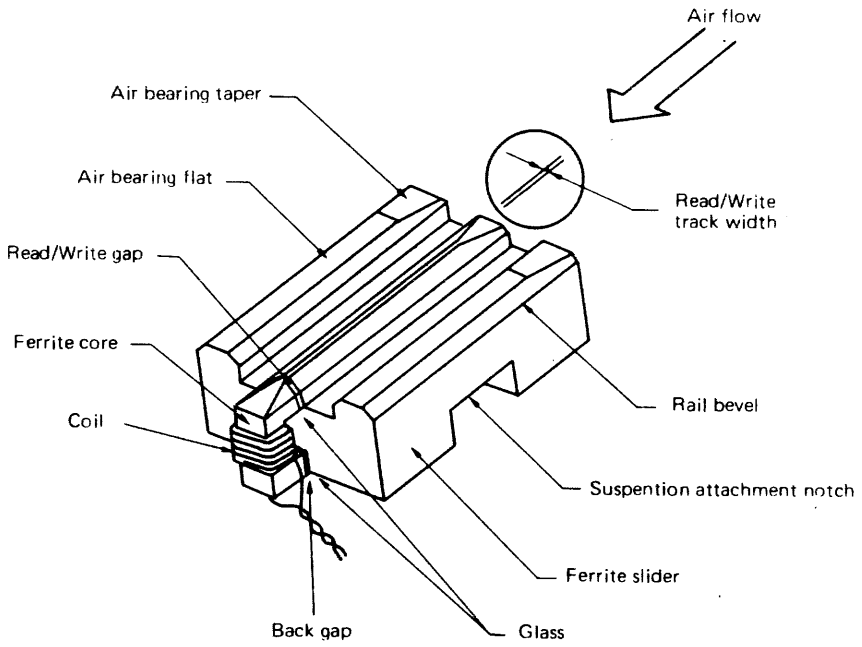


Figure 4-3-2 Tapered Flat Slider

To protect the data, the access head always performs C.S.S. in the landing zone. However, the fixed head performs C.S.S. over the data tracks becuase of its construction.

4.3.2 Recording Media (Magnetic Disk)

A magnetic disk is an aluminum disk approximately 356mm (14 inches) in diameter and approximately 2mm (75mil) thick coated with a magnetic material and is used to record data. Since this unit employs CONTACT START/STOP type heads, to prevent wear, the surface is coated with a special material. Up to three disks can be installed for a maximum storage capacity of 168.5MB. The outer portion, bottom surface of the lowest disk is for the servo area on which the positioning data and clock signals are recorded, and the inner portion head data regions.

4.3.3 Servo Track Format

4.3.3.1 Servo track configuration

The servo area is used to store the unique data patterns to generate the Track Positioning, Index, Guard Band and Clock signals. This data is prerecorded on the disk before the unit is shipped from the factory.

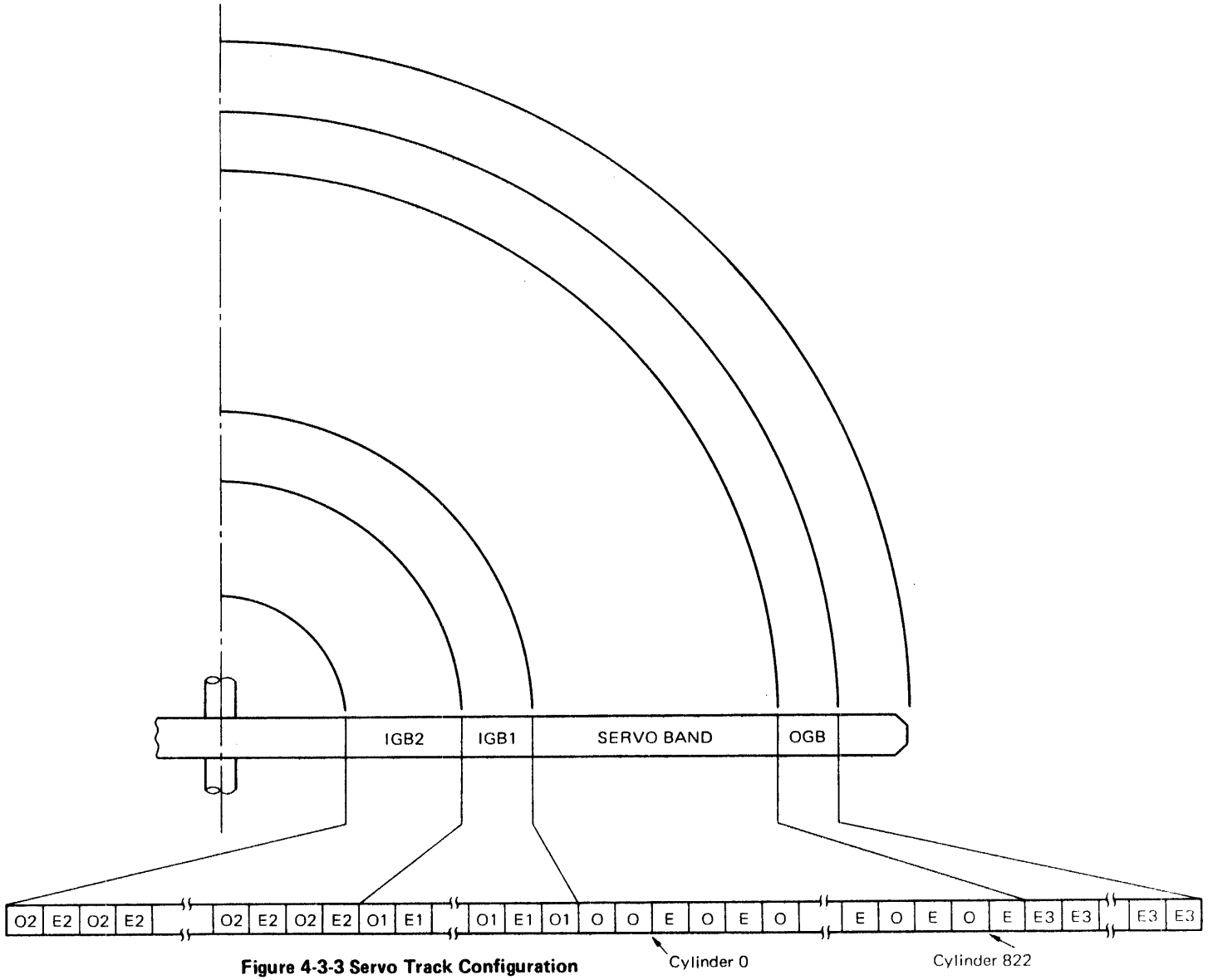


Figure 4-3-3 Servo Track Configuration

The servo area consists of a combination of ODD tracks and EVEN tracks, and is divided into the following four parts:

(a) Inner Guard Band 2 (IGB2 or Landing Zone)
This zone is used for head contact during stop and start.
IGB2 consists of 39 EVEN servo tracks and 39 ODD servo tracks.

(b) Inner Guard Band 1 (IGB1)
This area is located between IGB2 and cylinder zero. IGB1 consists of 11 EVEN and ODD servo tracks.

(c) Servo Band
This field is used for tracking to determine the center of each cylinder. ODD and EVEN servo signals are recorded on this 823 track area.

(d) Outer Guard Band (OGB)
Only EVEN servo signals are recorded in this 62 track area.

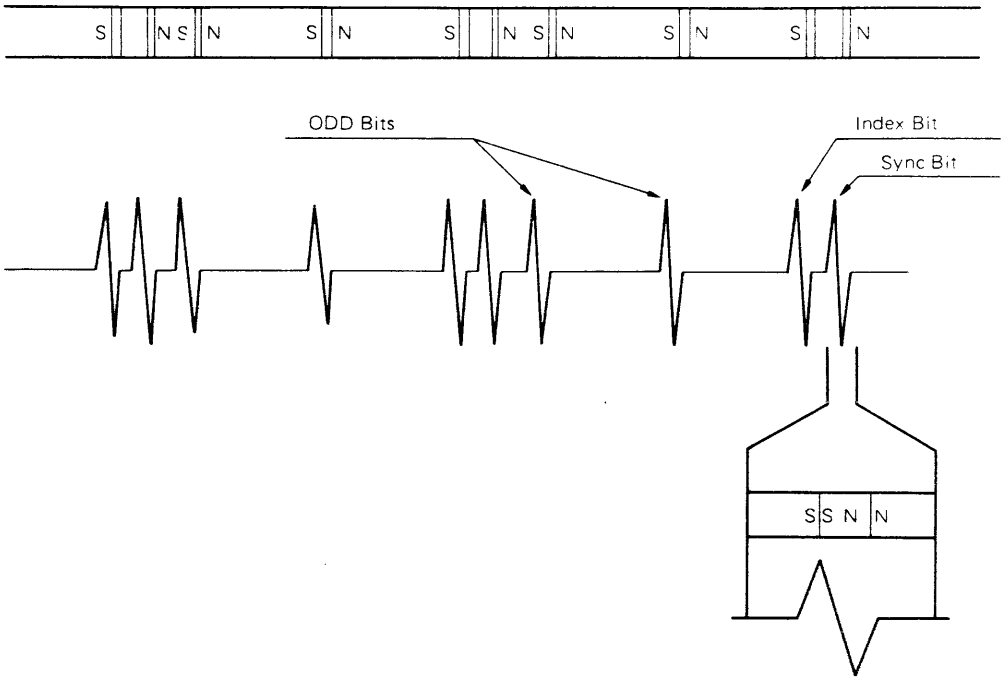
The physical placement of Servo Bands is shown in Figure 4-3-3.

4.3.3.2 Servo Pattern

The servo signal is a "composite signal." It is used to provide angular positioning (location with reference to the circumference of the disk) and radial positioning (location with reference to the radius of the disk) information. Angular positioning is determined by a series of sync bits which are written on each track. Through a combination of missing and normal index bits a "sync pattern" is developed. A series of unique sync patterns is written (see Figure 4-3-4) at the factory and used in the identification of specific disk regions. For example, Index Mark, OGB, IGB1 and IGB2 each have unique patterns as described in section 4.3.3.3.

Radial positioning information is provided by writing alternately odd and even bit patterns on each track. When the servo head is over an even bit track, the even bit signal is higher in amplitude than the odd bit signal. The opposite is true when the head is over an odd bit track. When the head is over the border of the two tracks, the odd and even bit signals are of equal amplitude. This condition means that a read/write head is directly over a data track. By detecting the odd and even bit signal amplitude changes, the drive is able to generate signals to indicate track crossing and on-track conditions.

(a) ODD Servo Signal



(b) EVEN Servo Signal

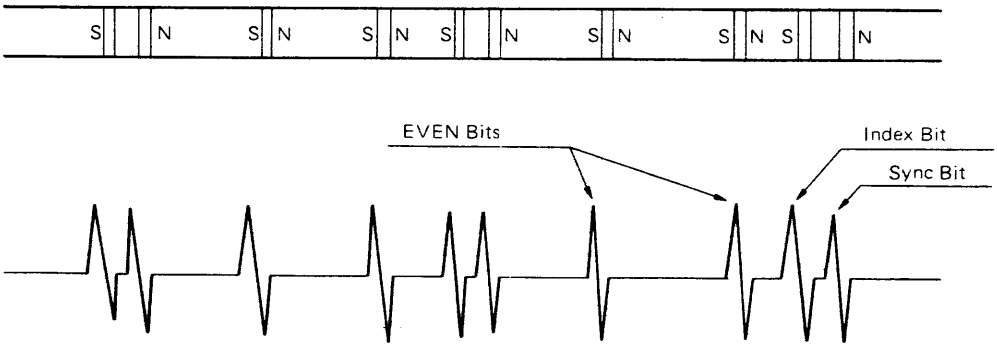


Figure 4-3-4 Servo Signals

On-track status, the servo head is positioned between an ODD track and an EVEN track, as shown in Figure 4-3-5.

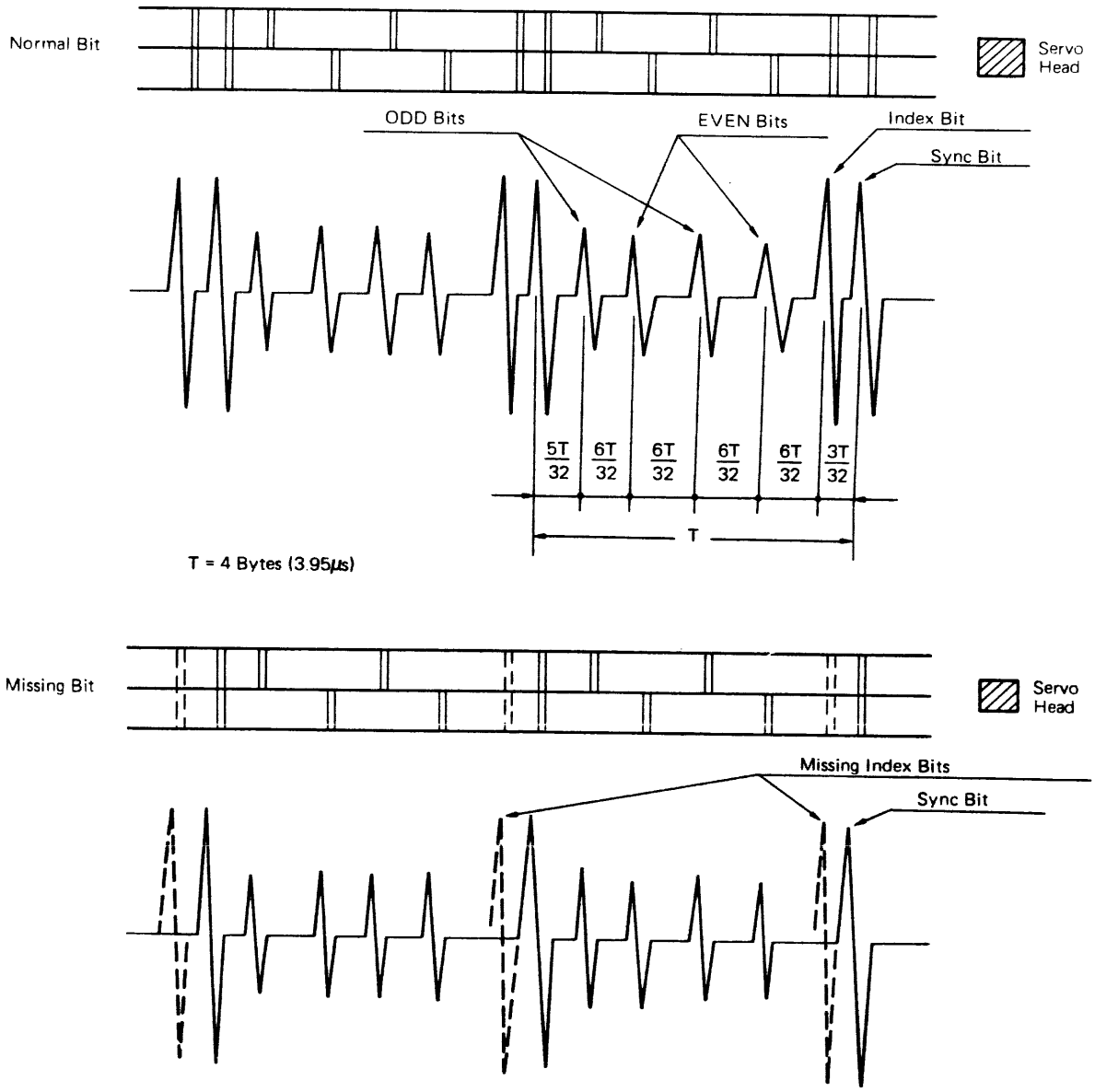


Figure 4-3-5 On-Track Servo Signal

4.3.3.3 Index, IGB2, IGB1 and OGB

Index, IGB2, IGB1 and OGB are detected by decoding the combination of Missing-bits and Normal-bits. Each of the patterns are shown in Table 4-3-1.

Table 4-3-1 Index/IGB2/IGB1/OGB Patterns

Signal	Pattern	Pattern Interval	Number/Revolution	Remarks
Even Index	01011	20,480 B	1	Normal Index
IGB2	01110	256 B	78	
IGB1	01010	256 B	78	
OGB	10011	256 B	78	
Odd Index	01101	20,480 B	1	Not used

Note: 0: Normal Bit
1: Missing Bit

4.3.4 Data Surface Format

The data surface consists of all the disk surfaces except the servo surface and is composed of three basic parts.

(1) Landing Zone (LZ)
The Landing Zone is included in the area described as behind home (BH) but is specifically the area the heads contact during Stop and Start. The Landing Zone corresponds to IGB2 on the servo surface.

(2) Behind Home (BH)
Behind Home is the transition area both sides of the data tracks and corresponds to IGB1 or OGB on the servo surface.

(3) Data Track
The data track area consists of 823 cylinders for data recording, with cylinder 0 being the innermost track and cylinder 822 being the outermost track.

4.3.5 Head and Surface Configuration

(1) M2282, M2286 (67.4MB)

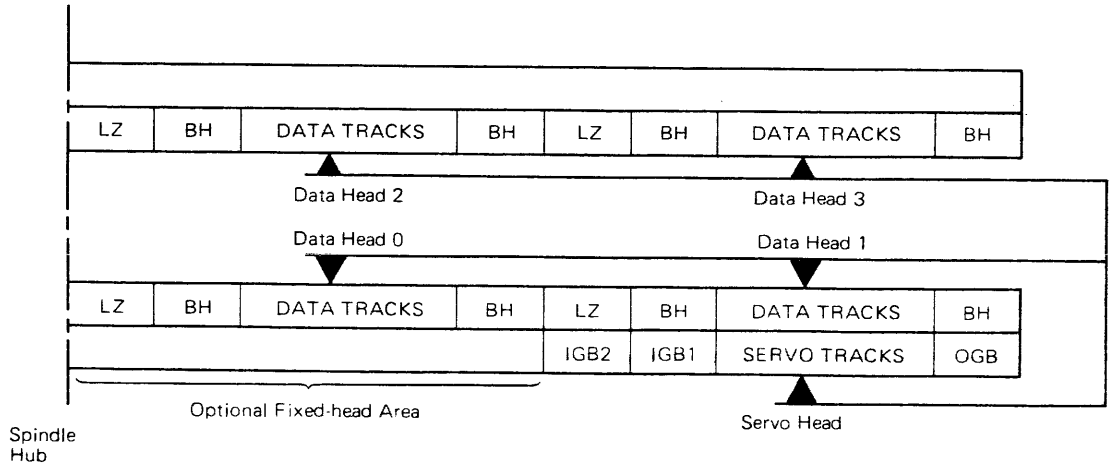
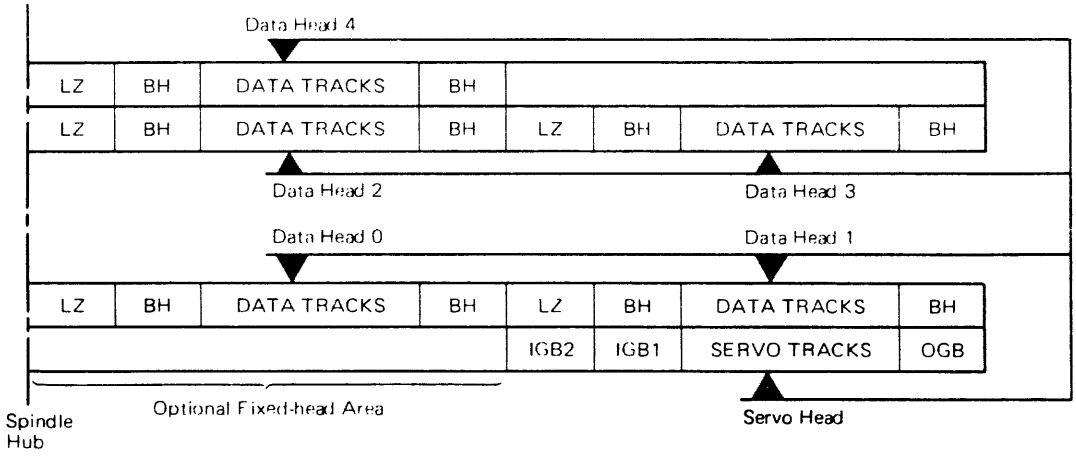
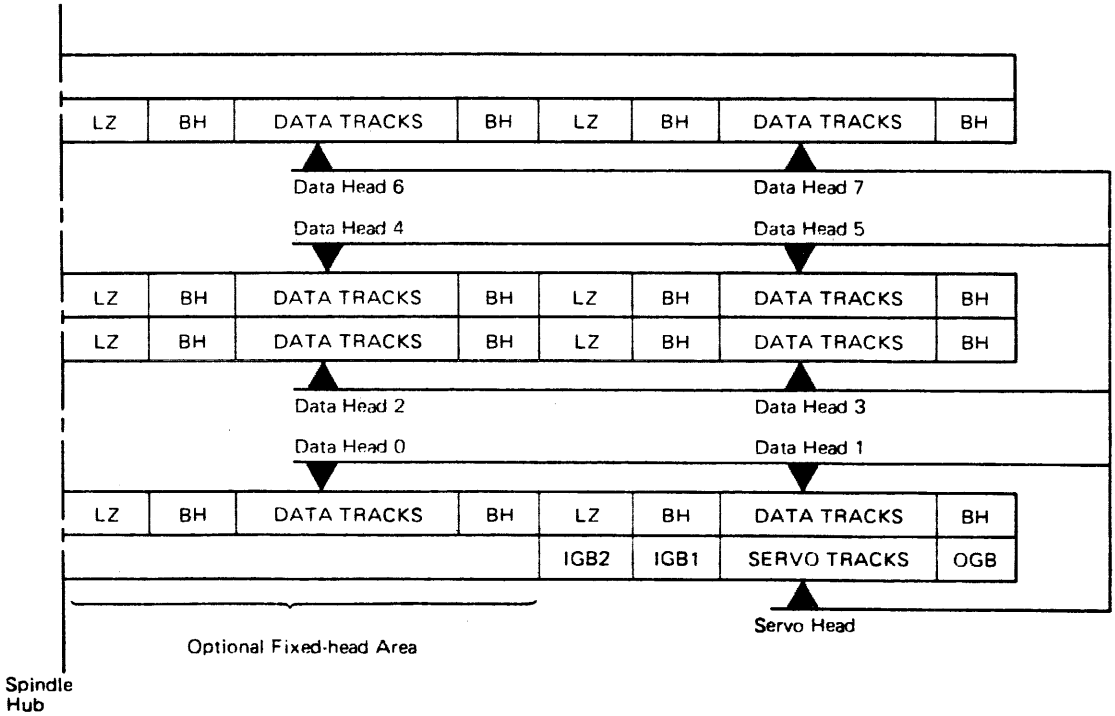


Figure 4-3-6 Head and Surface Configuration, Sheet 1 of 2

(2) M2280, M2289 (84.2MB)



(3) M2283, M2287 (134.8MB)



(4) M2284, M2288 (168.5MB)

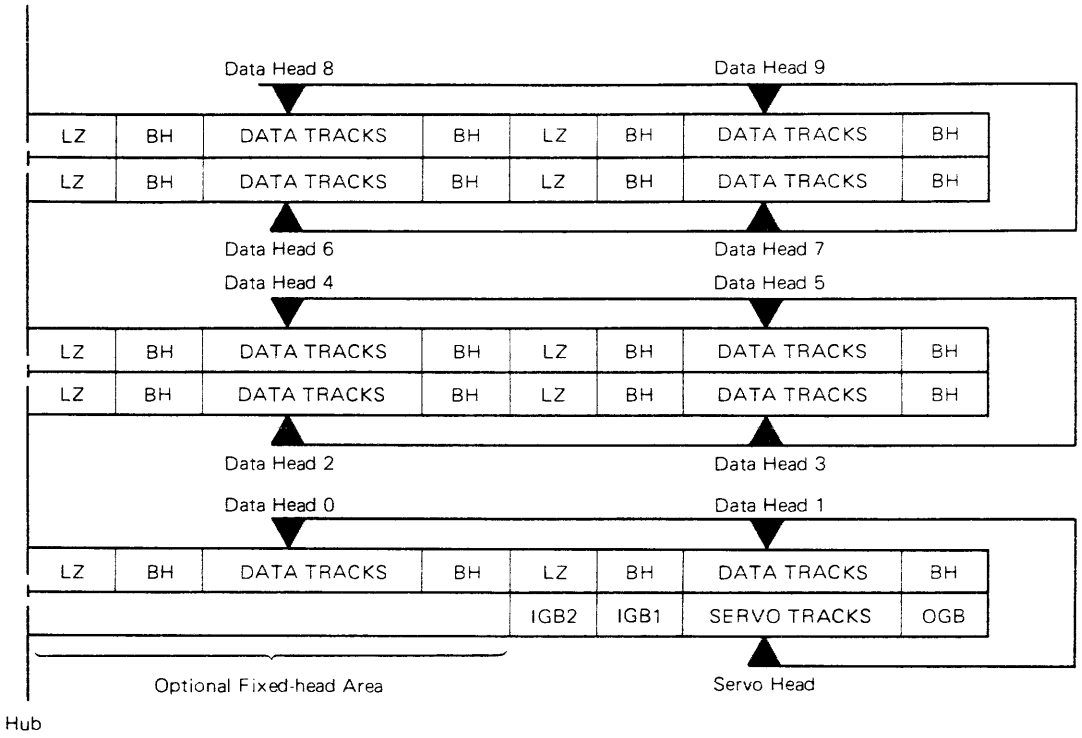


Figure 4-3-6 Head and Surface Configuration, Sheet 2 of 2

4.4 FORMAT

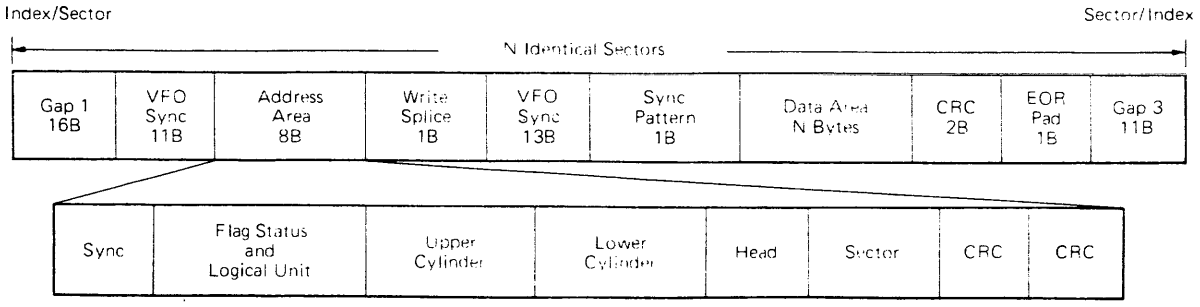
4.4.1 Description

A "sector" is an area assigned an address on the disk. Each sector consists of an Address Area (AA) to confirm that the correct sector has been read and a Data Area (DA) on which the actual data is recorded.

Index and sector pulses are used by the controller to find the beginning of the track and sector. Sector format is determined by the controller. Fixed Sector format or Variable Sector format can be used with this unit.

The recommended Fixed Sector format and Variable Sector format will be described in this section.

4.4.2 Fixed Sector Format



Example: 64 Sectors/Track

$$\text{Data Area} = \frac{\text{Total Bytes/Track}}{\text{Sector/Track}} - (\text{Gap loss} + \text{Check Bytes})$$

$$= \frac{20480}{64} - 64 = 256 \text{ Bytes/Sector}$$

$$\text{Track Efficiency} = \frac{256 \times 64}{20480} \times 100 = 80\%$$

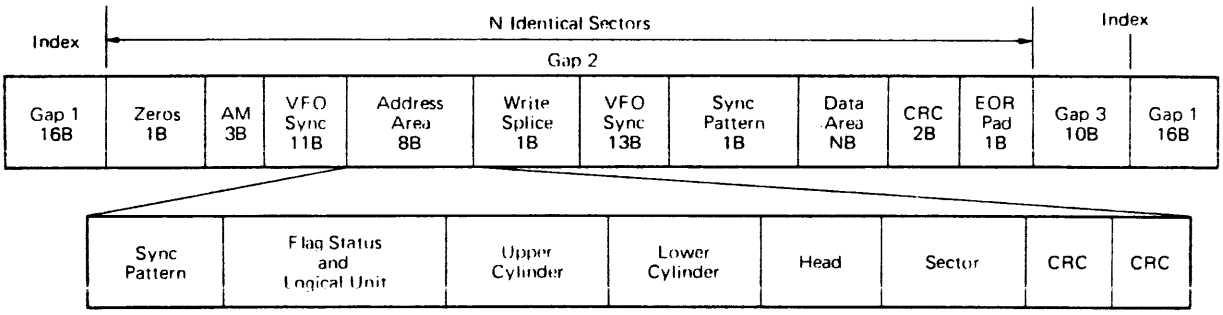
Notes: 1) This format is an example only and may be structured to suit individual requirements.

2) Sync Byte patterns for address and data areas may be different. It is recommended that Sync Byte patterns are $0E_{(Hex)}$ for address areas and $09_{(Hex)}$ for data areas.

3) Data patterns for Gap 1, VFO sync, Write Splice, EOR Pad and Gap 3 are all "0".

4) Fixed sectors per track may be any number from 1 through 128 and can be selected by setting the configurator switches on the PCB gate card.

4.4.3 Variable Sector Format



$$\text{Data Area} = \frac{\text{Total Bytes/Track - Index Loss}}{\text{Sectors/Track}} - (\text{Sync + Address Area})$$

Example 1: 64 Sectors/Track

$$\text{Data Area: } \frac{20480 - 26}{64} - 41 = 278 \text{ Bytes/Sector}$$

$$\text{Track Efficiency} = \frac{278 \times 64}{20480} \times 100 = 87\%$$

Example 2: 256 Bytes/Sector

$$\text{Sector Count} = \frac{20480 - 26}{256 + 41} = 68 \text{ Sectors/Track}$$

$$\text{Track Efficiency} = \frac{256 \times 68}{20480} = 85\%$$

Note: This format ia an example only and may be structured to suit invididual requirements.

4.4.4 Description of Format Parameters

4.4.4.1 Fixed Sector Format

(1) Gap 1
This gap allows for displacement of the head and circuit tolerances under worst case conditions. This gap must be a minimum of 16 bytes long.

(2) VFO Sync
All "0"'s are written and used to synchronize the data from the disk and the read/write clock from the disk VFO circuits.

(3) Sync Pattern
This pattern represents the start of the address area. The sync pattern is the same as that before the data area, but the address area sync and data area sync byte may be different. The recommended pattern is "$0E_{(Hex)}$".

(4) Flag Status and Logical Unit
This indicates the status of the disk on the sector. Normal record, primary record, or secondary record condition may be indicated. This specification is a function of the control unit.

(5) Upper Cylinder, Lower Cylinder
This indicates the cylinder address of the track.

(6) Head Address
This indicates the head address of the track.

(7) Sector Address
This indicates the sector address of the track.

(8) CRC (Cyclic Redundancy Check)
This is a check byte used to check whether the data was read correctly.

(9) Write Splice
When the address and data areas are written separately, this is the location of the read/write head transitions.

(10) VFO Sync
All "0"'s are written and used to synchronize the data from the disk and the read/write clock from the disk VFO circuits.

(11) Sync Pattern
Indicates the beginning of the data area. The recommended pattern is "$09_{(Hex)}$". Refer to (3).

(12) Data Area
The data is actually recorded at this area.

(13) CRC
Check byte to insure the data area information has been read correctly. Same as (8).

(14) EOR Pad
This eliminates the possibility of destroying the end of a record written with a late displacement head.

(15) Gap 3
This is the delay allowance for the control unit. It should be written all "0"'s.

4.4.4.2 Variable Sector Format

This is written in the Variable Sector Mode. Address Mark (AM) is written, prior to an Address Area, to indicate the beginning of a sector, and the data may be written in whatever length necessary to accommodate the system. The Address Mark (AM) is a 3 byte DC erase area at the beginning of the sector format.

4.5 INTERFACE

4.5.1 Introduction

4.5.1.1 Purpose

This section describes the logical and physical specifications for signal transfer within the interface between a Fixed Disk Unit (FDU) and the control unit.

4.5.1.2 Application

These specifications are applicable to the following models:

(a) FDU models M2282 and M2286 of 67.4MB storage
M2282 has no fixed head storage.
M2286 has 655KB of fixed head storage (option).

(b) FDU models M2280 and M2289 of 84.2MB storage
M2280 has no fixed head storage.
M2289 has 655KB of fixed head storage (option).

(c) FDU models M2283 and M2287 of 134.8MB storage
M2283 has no fixed head storage.
M2287 has 655KB of fixed head storage (option).

(d) FDU models M2284 and M2288 of 168.5MB storage
M2284 has no fixed head storage.
M2288 has 655KB of fixed head storage (option).

4.5.1.3 Connection

The external connection (for transmitting and/or receiving interface signals for the unit) consists of two connectors, "A" and "B", which are connected, respectively, to cables "A" and "B". "A" cables may be connected in a daisy-chain configuration. Therefore, a line terminator must be inserted into the "A" connector of the last device. "B" cables are connected in a star configuration. Therefore, the control unit requires "B" cables and connectors to match the number of units to be connected.

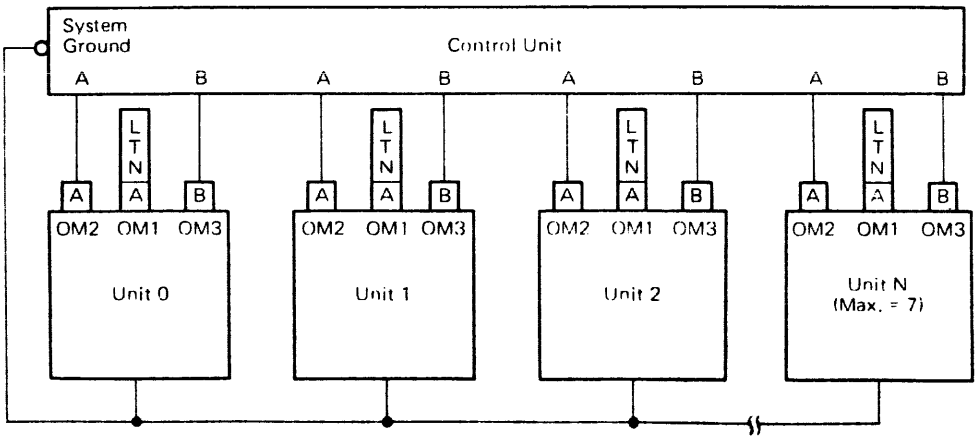
4.5.1.4 Time Specification

Timings are specified at the connector position of the unit. Accordingly, it is necessary for signal timings to consider both the delay time of the interface cable and the circuits of the disk control unit.

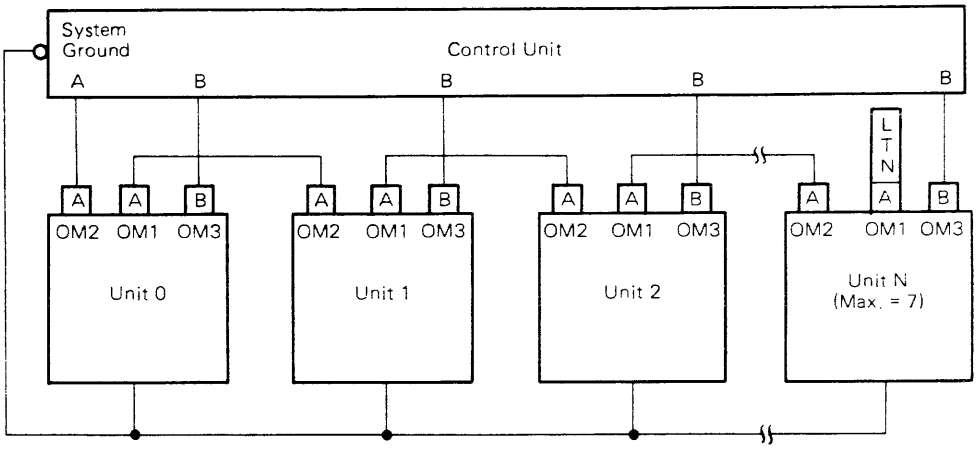
4.5.1.5 Interface Transmitter/Receiver

Transmitters and receivers of SN75110 and SN75107 or equivalent are used to provide a terminated, balanced-line transmission system. Refer to Section 4.5.7.

4.5.2 Interface Cabling



Star Cable Configuration



Daisy-Chain Cable Configuration

Notes: 1) Line terminators (LTN) are required on the control unit and each unit in a star cable configuration.

2) Line terminators are required on the control unit and last drive in a daisy-chain cable configuration.

Figure 4-5-1 Interface Cabling

4.5.3 Type and Name of Signal Lines

4.5.3.1 "A" – Cable Lines for Balanced Transmission

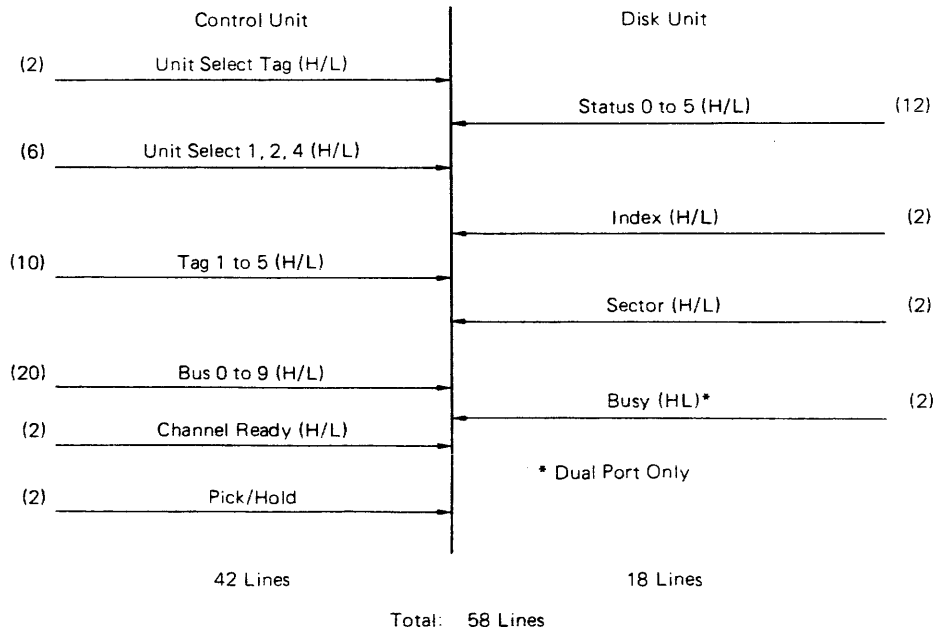


Figure 4-5-2 "A" Cable Signals

4.5.3.2 "B" – Cable Lines for Balanced-line Transmission

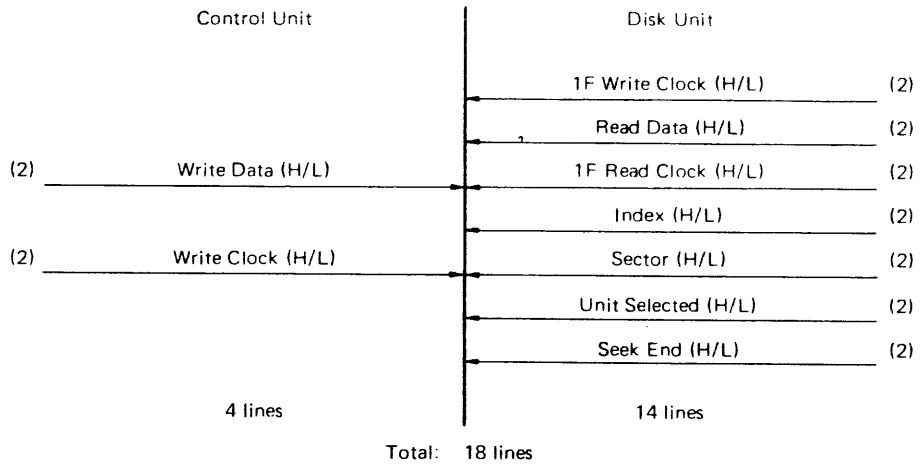


Figure 4-5-3 "B" Cable Signals

4.5.4 Description of Signal Lines

4.5.4.1 "A" – Cable Input Signal

(1) Unit Select Tag
This signal gates Unit Select 1, 2 and 4 to select the desired disk. Refer to timing of Unit Select 1, 2 and 4 (Figure 4-5-8).

(2) Unit Select 1, 2 and 4
These three signals are binary-coded to select the desired disk and are validated by the leading edge of Unit Select Tag. The logical disk number (0 through 7) is selectable by means of a switch located on the PCB card.

(3) Tag 1 to 3 and Bus 0 to 9

Table 4-5-1 Tag/Bus Lines

Bus	Tag 1	Tag 2	Tag 3	Unit Select Tag 2*
	Cylinder Address	Head Address	Control Select	
0	1	1	Write Gate	–
1	2	2	Read Gate	–
2	4	4	Servo Offset Plus	–
3	8	–	Servo Offset Minus	–
4	16	–	Fault Clear	–
5	32	–	AM Enable	–
6	64	–	RTZ	–
7	128	–	–	–
8	256	–	–	–
9	512	–	Release 1*	Priority Select 1*

Note 1: Dual Port Only.

2: Validates (or gates) the Unit Select 1, 2, and 4 lines in addition to the dual port priority select line.

(3)-1 Storage Addressing of M2280 to M2289

Each area of Fixed Head Address and the Access Head Address is specified as follows: (Storage capacity shown is unformatted)

(a) FDU Model M2282 and M2286

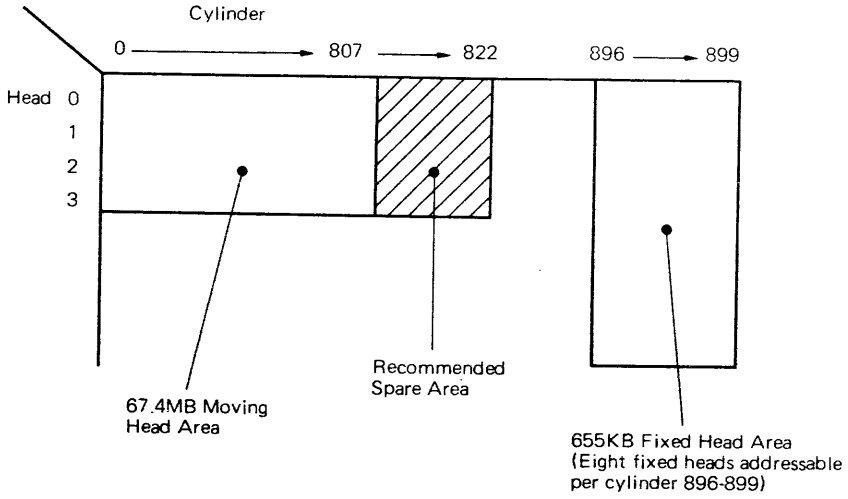


Figure 4-5-4 Storage Addressing M2282/M2286

(b) FDU Model M2280 and M2289

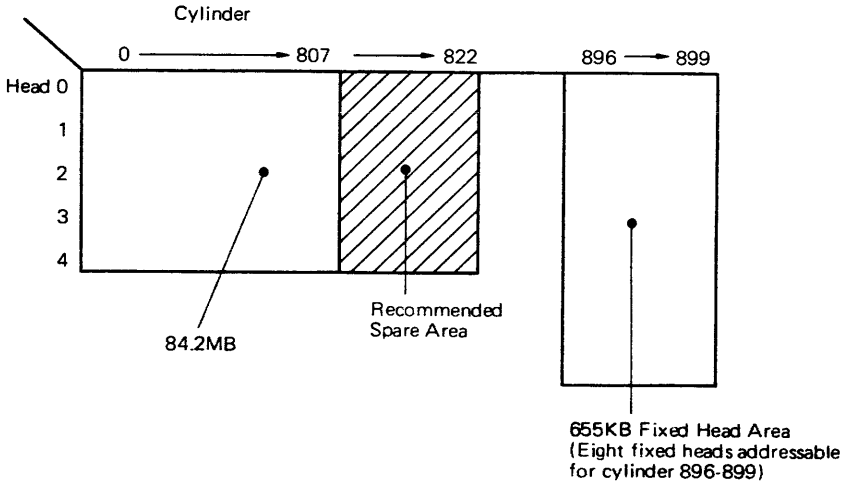


Figure 4-5-5 Storage Addressing M2280/M2289

(c) FDU Model M2283 and M2287

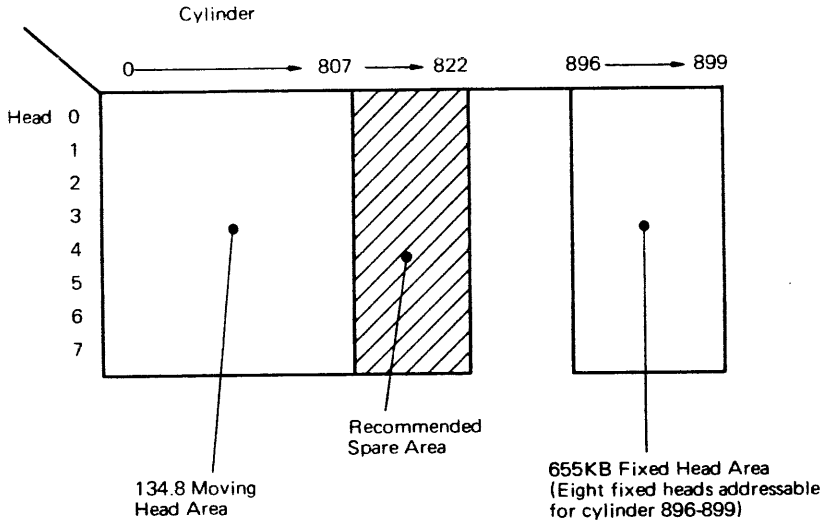


Figure 4-5-6 Storage Addressing M2283/M2287

(d) FDU Model M2284 and M2288

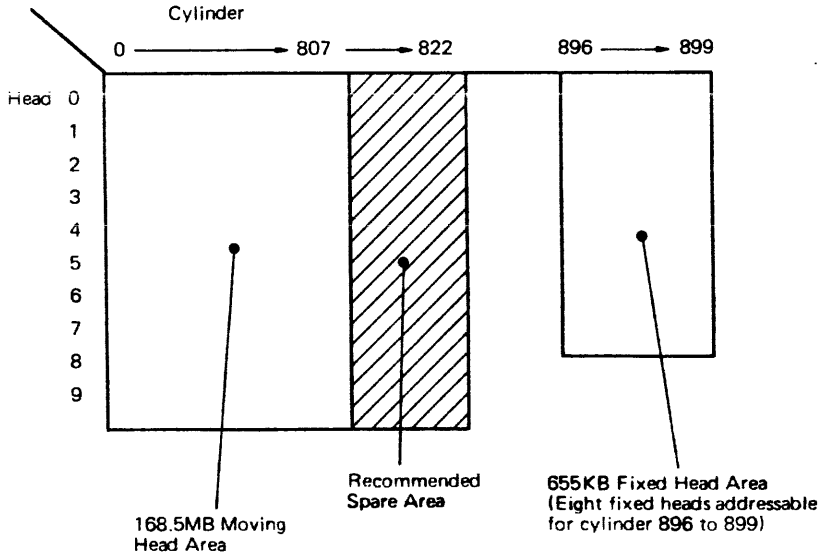


Figure 4-5-7 Storage Addressing M2284/M2288

(3)-2 Models M2286, M2289, M2287 and M2288 have fixed head capacities of 655KB which is addressed in (3)-1 above. The fixed head area will be addressed by a cylinder address specified greater than or equal to 896 (going true of Tag 1, Bus 7, Bus 8 and Bus 9).

The access head area and fixed head area can be distinguished by this bit assignment. Since the fixed area can be utilized with the access head area, the optimum address arrangement on the system can be easily constructed to minimize access times.

(4) Cylinder Address (Tag 1)

The cylinder address is set by Tag 1 and bus lines (Bus 0 to 9) on the unit. However, throughout Tag 1, the bus lines must be stable. Refer to Figures 4-5-10 to 4-5-13.

The unit must be On Cylinder prior to Tag 1. When the bus content is equal to or more than 896, the Fixed Head area is specified. When the Fixed Head area is specified, no physical movement of the heads is performed in the unit.

(5) Head Address (Tag 2)

The head address is set by Tag 2 and Bus 0 to 3 on the unit; however, throughout Tag 2, Bus 0 to 3 must be stable. Refer to Figure 4-5-12, and to (3)-1 above concerning the Fixed Head Area.

(6) Control Select

Bus lines 0 to 9 specified by Tag 3 have a different meaning in each bit. All signals are defined as control signals.

(6)-1 Write Gate (Bus 0)

This signal enables the write operation on the specified track. This signal is validated under the following conditions:

Unit Ready	True
On Cylinder	True
Seek Error	False
Device Check	False
Channel Ready	True
File Protect	False
Offset	False

If Write Gate is turned on in cases other than the above-mentioned conditions, Device Check occurs and writing is inhibited. Refer to the definition of a Device Check.

(6)-2 Read Gate (Bus 1)

This signal is used to recover data from the specified track. Refer to the timing of Read Gate and Read Data in Figure 4-5-23 and Figure 4-5-24.

(6)-3 Servo Offset Plus (Bus 2)

When Servo Offset Plus signal is ture on the unit, the head is offset 3.0μm from nominal On Cylinder position away from the spindle. Refer to Figure 4-5-14. When going false of Servo Offset Plus, a 4ms delay is required before writing.

(6)-4 Servo Offset Minus (Bus 3)

When Servo Offset Minus signal is true on the unit, the head is offset 3.0μm from nominal On Cylinder position towards the spindle. Refer to Figure 4-5-14. When going false of Servo Offset Minus, a 4ms delay is required before writing.

(6)-5 Device Check Clear (Bus 4)
This signal clears the device check status; however, if sources of a device check still exist (refer to Device Check), this status is not cleared.

(6)-6 AM Enable (Bus 5)
The AM (Address Mark) Enable, in conjunction with Write Gate or Read Gate, is used in a variable sector format. When AM Enable is true while Write Gate is true, an AM of 3-bytes is written on the desired track.

When AM Enable is true while Read Gate is true, the disk read circuit searches an AM of 3-bytes. When the AM is found, the unit will issue Address Mark Found signal to the control unit. Refer to Figures 4-5-25 and 4-5-26.

(6)-7 RTZ (Return to Zero) (Bus 6)
No matter where the access heads are located on the media, they are returned to cylinder zero and head zero by the RTZ signal, also the RTZ signal is available in the fixed head area and resets Fixed Head Select latch. This signal clears the Seek Error flip-flop. Refer to Figure 4-5-16.

(6)-8 Release (Bus 9)
The Release command releases Channel Reserve and Unconditionally Reserve in the drive, making alternate channel access possible after selection by the other channel ceases.
If the customer desires the Release Timer feature using the Release Time switch on the optional Dual Port PCB assembly, release will occur 500ms (nominal) after the deselection of the drive. Refer to Figure 4-5-8 and Figure 4-5-9.

(7) Channel Ready
This signal is used to prevent damage to the file caused by interface disturbances when the control unit power is lost. Therefore, this signal must be stable when the control unit is available, and must be disabled before logic levels decay at the interface lines when a power failure of the control unit occurs. Refer to Figure 4-5-17.

(8) Tag 4 and Tag 5 (Selectable)
When Tag 4 goes true, the unit issues Sector Address Status signals on the Status 0 to 5 lines.

When Tag 5 goes true, the unit issues Device Check Status signals on the Status 0 to 5 lines.

When both Tag 4 and Tag 5 are true, the Device Type Code will be issued in BCD on the Status 0 to 5 lines. See Table 4-5-2 and Figure 4-5-18.

(9) Pick and Hold
Power Sequencing requires that the mode switch on the power supply unit be set to Remote.

When the control unit sets the Pick and Hold lines to ground, the first FDU starts up the power sequence. Once this FDU has reached nominal speed, the Pick signal is transferred to the next FDU, and repeated until all FDU's are powered up. When the mode switch on the power supply is set to Local, each FDU must be powered up manually.

(10) Priority Select (Dual Port Only)
When the control unit issues Unit Select Tag and Bus Big 9 with a specified disk address, the disk drive will be unconditionally selected and absolutely reserved by the channel issuing the command, providing both channels are enabled and a priority select condition does not exist on the opposite channel. Once the drive is unconditionally reserved by a Priority Select command, the respective channel has exclusive access to the drive. The opposite channel can access it only after Release command has been issued by the selected channel. Refer to Figure 4-5-9. When a dual port drive is unconditionally reserved, all interface signal are inhibited on the other channel,

including unit selected and Busy signals.

4.5.4.2 A – Cable Output Signal

(1) Status 0 to 5

The status 0 to 5 lines display status information determined by combinations of Tag 4 and Tag 5 signals. Information available on status lines 0 to 5 during various status of Tag 4 and 5 is specified in Table 4-5-2.

Table 4-5-2 Status Lines Determined by Tag4/5

Tag 4	False	True	False	True
Tag 5	False	False	True	True
Status	Unit Status	Sector Address	Check Status	Device Type
0	Unit Ready	Sector Address 1	Control Check 1	Device Type 1
1	On Cylinder	2	2	2
2	Seek Error	4	Read/Write Check 1	4
3	Device Check	8	2	8
4	File Protected	16	3	16
5	AM Found	32	4	32

(A) Unit Status

(1) Unit Ready

When this signal is true, and the unit is selected, this signal indicates the unit is up to speed, and no fault condition exists within the unit.

(2) On Cylinder

This line indicates that the heads are located on the specified track (cylinder).

(3) Seek Error

This signal indicates that a seek error has occurred. In this case, the On Cylinder signal does not always go true. The Seek Error is cleared only by performing an RTZ (Tag 3 and Bus 6). Seek Error status is defined as follows:

a) Seek was unable to complete a move within 640ms.
b) RTZ was unable to complete a move within 640ms.
c) The heads have moved to a position outside the recording area.
d) An illegal cylinder address was issued to the FDU.
e) Heads have overshot the new cylinder address.

(4) Device Check

This signal indicates that a fault condition exists in the unit. The following fault conditions may be detected by the unit.

a) Control Check 1
Instructions received during Not Ready status.

b) Control Check 2
Instructions received during fault condition status. Write Gate received during an off-set operation, reading or Seek Error condition.

c) Read/Write Check 1
Write Gate received during Off-track status or VCM overcurrent.

d) Read/Write Check 2
Write fault or write current detected during a not-write operation.

e) Read/Write Check 3
Write Gate received during write protected status.

f) Read/Write Check 4
Write or Read Gate received when multiple heads are selected.

If an above-mentioned condition has occurred, writing is immediately inhibited and a Device Check signal is issued to the control unit. The device check status is cleared by the following operations:

- Fault Clear on Tag 3 and Bus 4
- Fault Clear on the operator panel (if operator panel is employed)
- Fault Clear Switch on the PCB chassis

Device Check Status turns on the check lamp on the operator panel as well as Maintenance Aid LED's on PCB chassis.

(5) File Protected
File Protected signal indicates that the FDU is in write-protected status. The File Protect function is enabled by the following switches:

- File Protect Switch on the operator panel (option)
- File Protect Switch on the PCB chassis

Attempting to write while protected will cause a Device Check (Read/Write Check 3) to be issued to the control unit.

(6) Address Mark Found
Address Mark Found is 8-byte pulse which is sent to the control unit at least 2-bytes after the recognition of 3-byte DC-erased area.

(B) Sector Address 1 to 32 (Status Lines 0 to 5)
Six-bits of binary-coded Sector Address are transferred from the Sector Counter, reset by the trailing edge of Index, clocked by the trailing edge of Sector, and indicate the current sector address in the unit. Sector Address (Status Lines 0 to 5) will be issued to the control unit by activating Tag 4.
Refer to Figure 4-5-19 for timing of Sector Address (status lines 0 to 5).

(C) Device Check (Status 0 to 5)
Refer to item (A) – (4).

(D) Device Type 1 to 32 (Status lines 0 to 5)
Enabling selectable Tag 4 and Tag 5 lines, causes key-selected Device Type Status to be issued to the control unit as Status 0 to 5 signals. Binary-coded Device Type signals are specified as show in Table 4-5-3.

Table 4-5-3 Device Type Code

Device Type	Decimal Value	Status					
		0	1	2	3	4	5
		2^0	2^1	2^2	2^3	2^4	2^5
M2282	20	0	0	1	0	1	0
M2280	21	1	0	1	0	1	0
M2283	24	0	0	0	1	1	0
M2284	28	0	0	1	1	1	0
M2286	22	0	1	1	0	1	0
M2289	23	1	1	1	0	1	0
M2287	26	0	1	0	1	1	0
M2288	30	0	1	1	1	1	0

Notes: 0: False
1: True

(2) Index
This signal occurs once per revolution and is used for reference in read/write operation.
Refer to Figure 4-6-19 for the timing of Index and Sector.

(3) Sector
The Sector Mark is derived from the servo track. The number of sectors per revolution is switch selectable and is determined by counting Byte Clock. The switches are located on the VFO/PLO card within the PCB chassis. Each key of SW1 and SW2 represents binary powers of Byte Clock.

(4) Busy (Dual Port Only)
If the drive is already selected and/or reserved, a Busy signal will be issued to the "A" cable and the Unit Selected signal will be issued to the "B" cable of the channel attempting the select function. The Busy signal will remain until the Unit Select Tag is negated or the drive is no longer busy. Unit Selected signal should be used to enable Busy in the control unit. Refer to Figure 4-5-8.

4.5.4.3 B – Cable Input Signal

(1) Write Data
This line carries NRZ data which is to be written on the disk surface and must be synchronized with Write Clock. Refer to Figure 4-5-20.

(2) Write Clock
Write Clock is a return signal of the 1F Write Clock issued from the unit, and must be synchronized with the NRZ Write Data. Refer to Figure 4-5-20.

4.5.4.4 B – Cable Output Signal

(1) 1F Write Clock
This signal is used by the control unit to synchronize Write Data and Write Clock. 1F Write Clock is available during Unit Ready Status except during read operations. Refer to Figure 4-5-20.

(2) Read Data
This line transmits the recovered data in the form of NRZ data synchronized with 1F Read Clock. Refer to Figure 4-5-21.

(3) 1F Read Clock
This line transmits 1F Read Clock which defines the beginning of a bit cell. The Read Data is synchronized with the 1F Read Clock. Refer to Figure 4-5-21.

(4) Unit Selected
When the three unit select lines compare with the logical address of the unit, and when the leading edge of Unit Select Tag is received, the Unit Selected Signal goes true and is issued to the control unit. This signal also activates all status lines at the A–Cable.

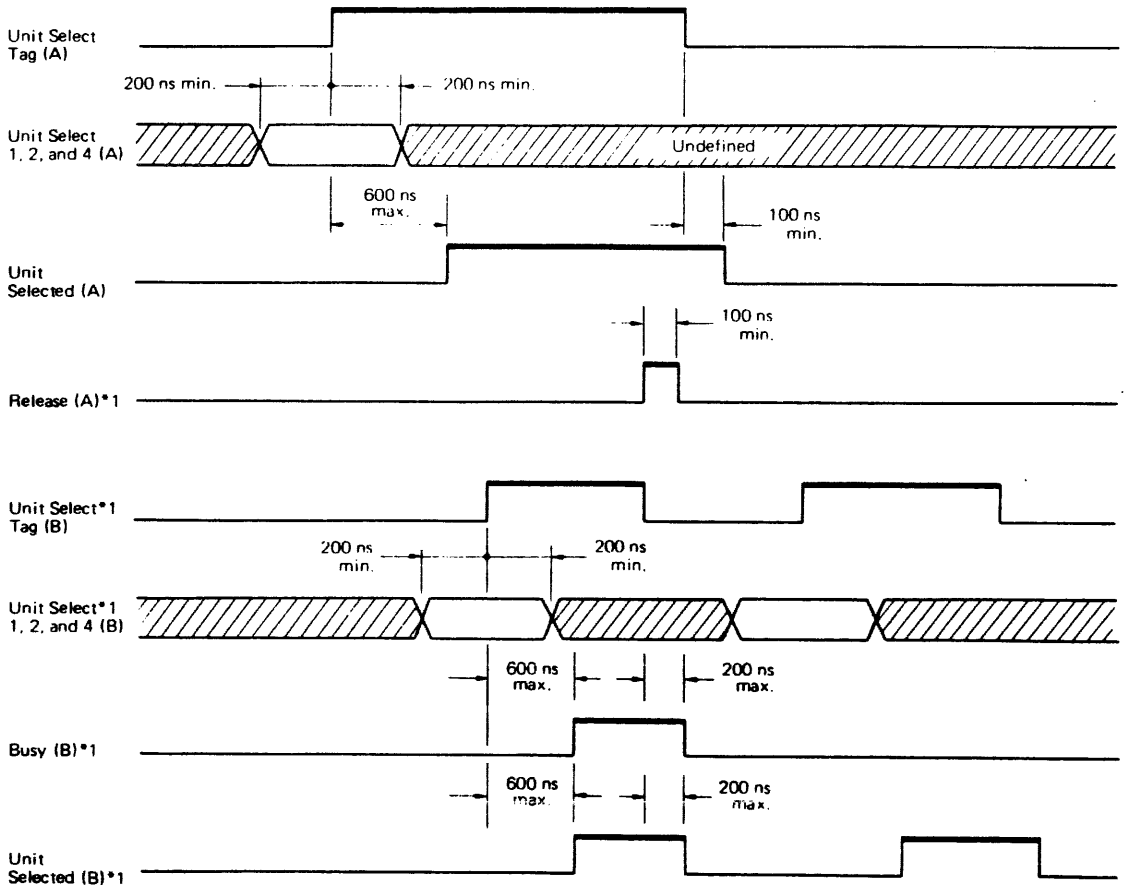
(5) Seek End
Seek End signal is a combination of On Cylinder and Seek Error, indicating that a Seek RTZ, or Offset operation has terminated.
In the Dual Port function, the Seek End signal sent to the unselected channel will normally be a constantly true signal level. However, if the drive is selected by one channel, and the other channel receives a select, the Seek End signal sent to the waiting channel will go false for 30μs, when the Select and Reserve latches are reset on the selected channel.

(6) Index, Sector
The Index and Sector pulses are issued on the interface for reference during read/write operations.

4.5.5 Control Timing

4.5.5.1 Unit Selection

Refer to Figure 4-5-8.

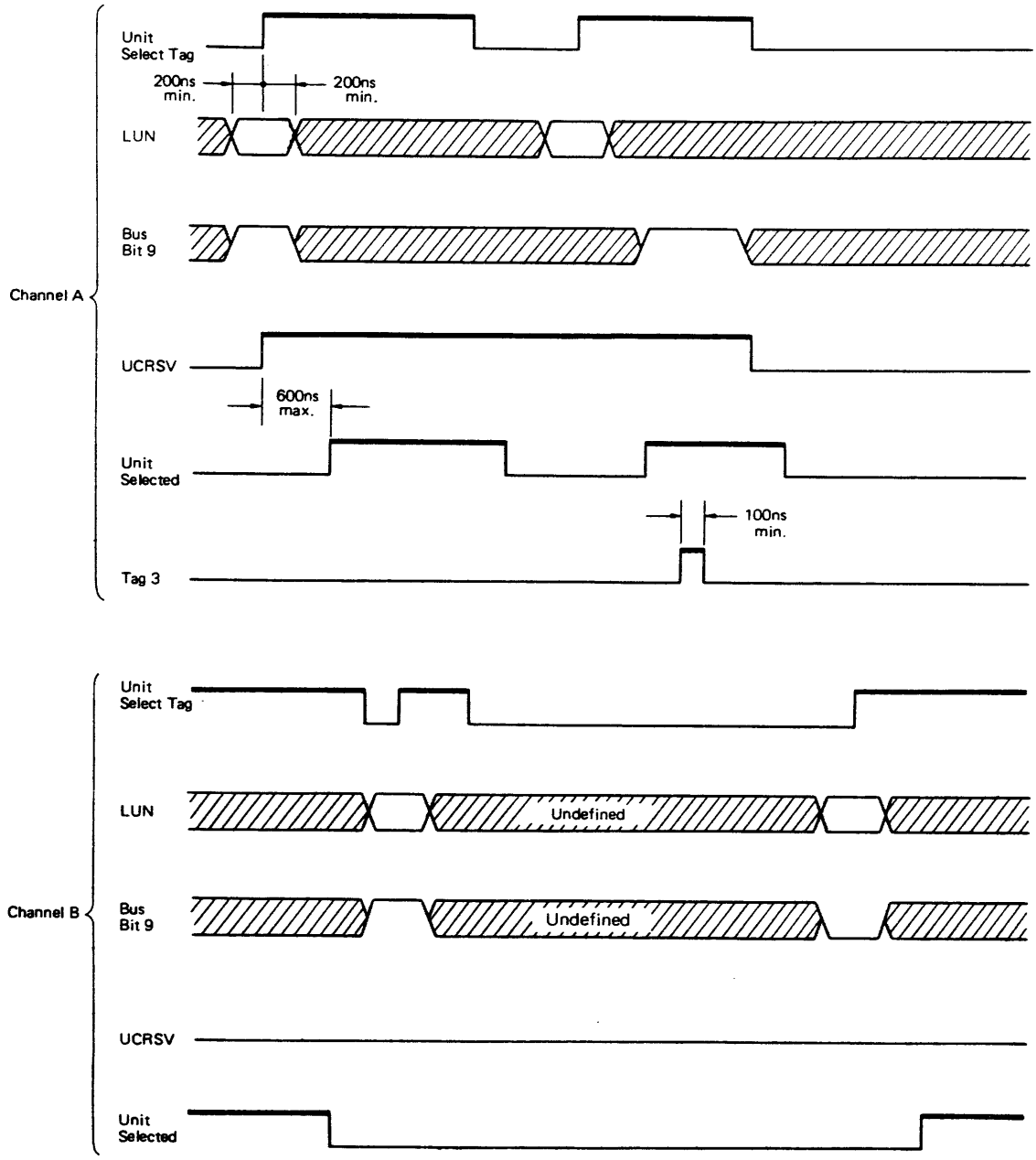


Note: * 1—Dual Port only.

Figure 4-5-8 Unit Select Timing

4.5.5.2 Priority Select Timing (sample)

Refer to Figure 4-5-9.



Notes: 1) LUN: Logical Unit Number (Unit Select 1, 2 and 4).

2) UCRSV: Unconditionally Reserved (Priority Selected).

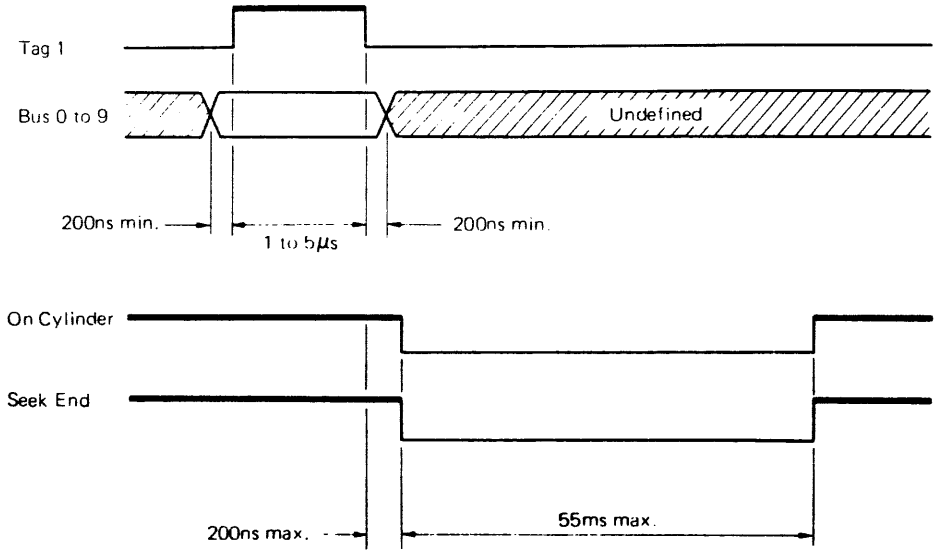
3) Sample Sequence is as follows;

CHB Selected → CHA Priority Select → CHB Priority Select → CHA Release → CHB Select

Figure 4-5-9 Priority Select Timing

4.5.5.3 Direct Seek Timing (Tag 1)

Refer to Figure 4-5-10.



Note: Cylinder Address must be less than 896 to select the access heads.

Figure 4-5-10 Direct Seek Timing

4.5.5.4 Zero Track Seek Timing

Refer to Figure 4-5-11.

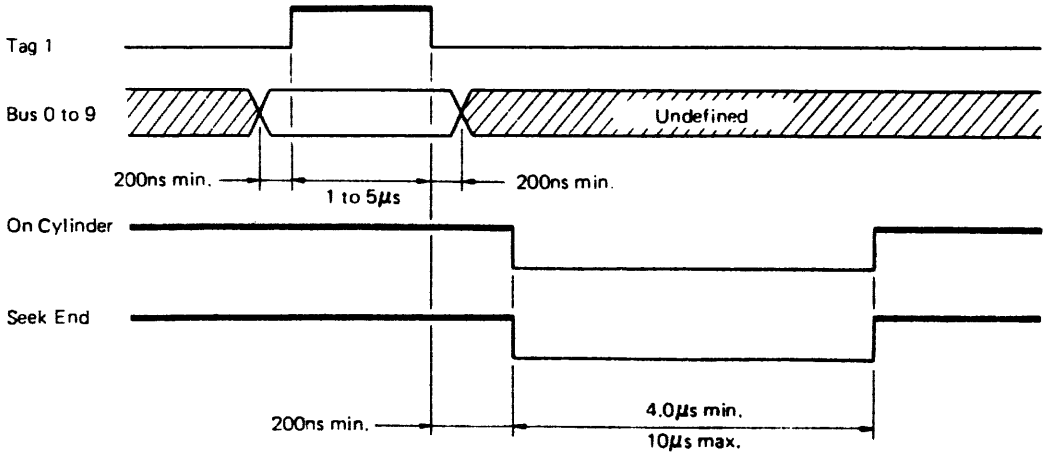
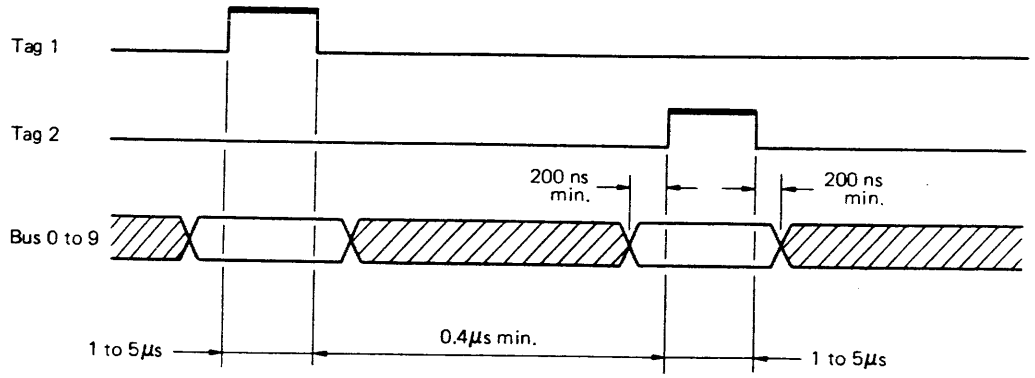


Figure 4-5-11 Zero Track Seek Timing

4.5.5.5 Tag 1 to Tag 2 Timing

Refer to Figure 4-5-12.



Notes: 1. When cylinder address is more than or equal to 896, the cylinder address is defined as fixed head area and the subsequent Tag 2 is defined as head address of the fixed head area.

2. The addressing for the fixed head area does not affect On Cylinder as Seek End signals.

Figure 4-5-12 Tag 1 to Tag 2 Timing

4.5.5.6 Fixed Head Addressing During Seek Operation

Refer to Figure 4-5-13.

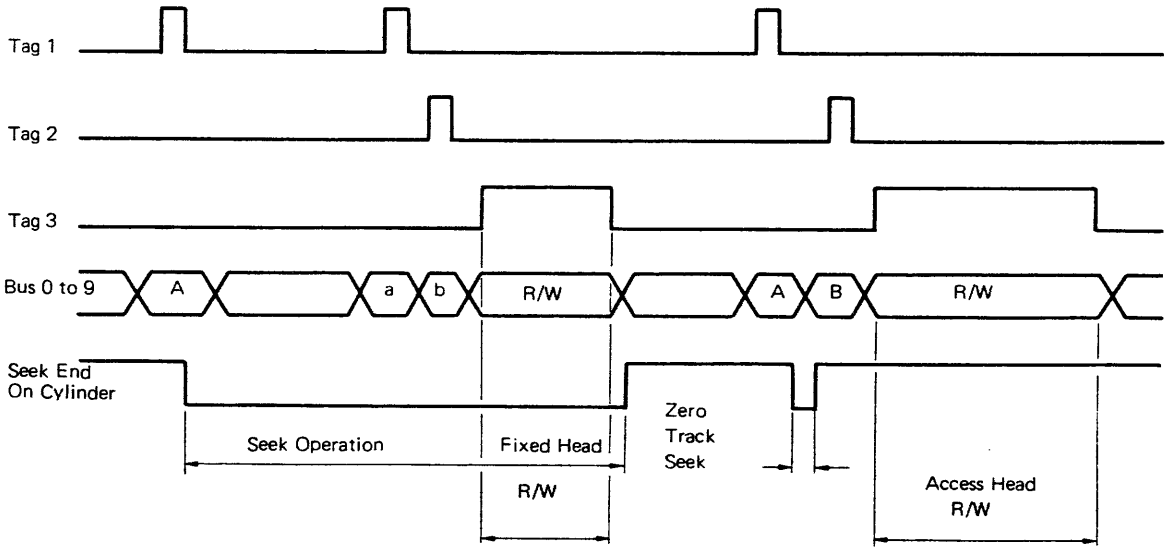


Figure 4-5-13 Fixed Head Addressing During Seek Operation (continued)

The normal sequence of this operation would occur in the following order:

(1) The control unit issues Tag 1 (cylinder select) with the desired access head cylinder address (A) on the bus. On Cylinder and Seek End will go false.
(2) The control unit access the desired fixed head area with the appropriate cylinder($\geq$ 896) (a) and head select signals (b).
(3) The control unit can read or write on the fixed head area while the access heads are in motion. Reading or writing to the fixed head area during the absence of On Cylinder and Seek End will not cause a Device Check.
(4) At the completion of the seek to the access head, On Cylinder and Seek End will go true.
(5) After the read or write operation to the fixed head area, the control unit may readdress the access head by sending the appropriate cylinder select (A) (zero track seek) and head select (B) signals. The cylinder select Tag 1 resets the fixed head mode.

Figure 4-5-13 Fixed Head Addressing During Seek Operation

4.5.5.7 Offset Plus/Minus Timing

Refer to Figure 4-5-14.

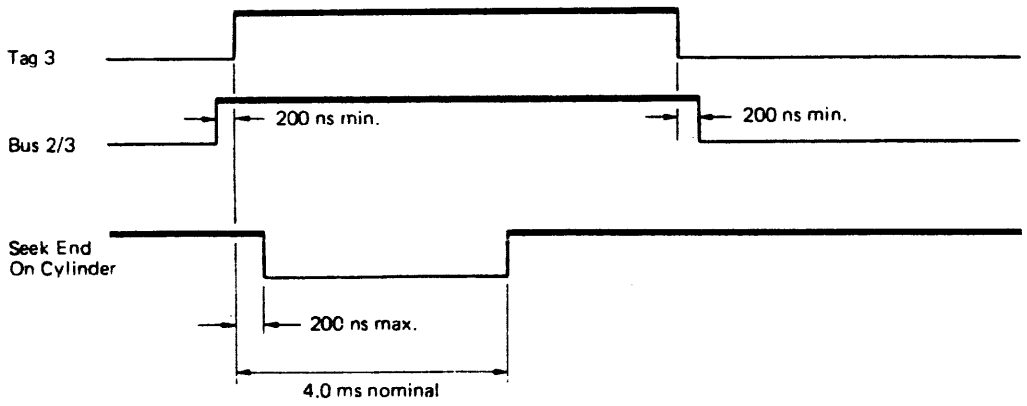


Figure 4-5-14 Offset Plus/Minus Timing

4.5.5.8 Device Check (Fault) Clear Timing

Refer to Figure 4-5-15.

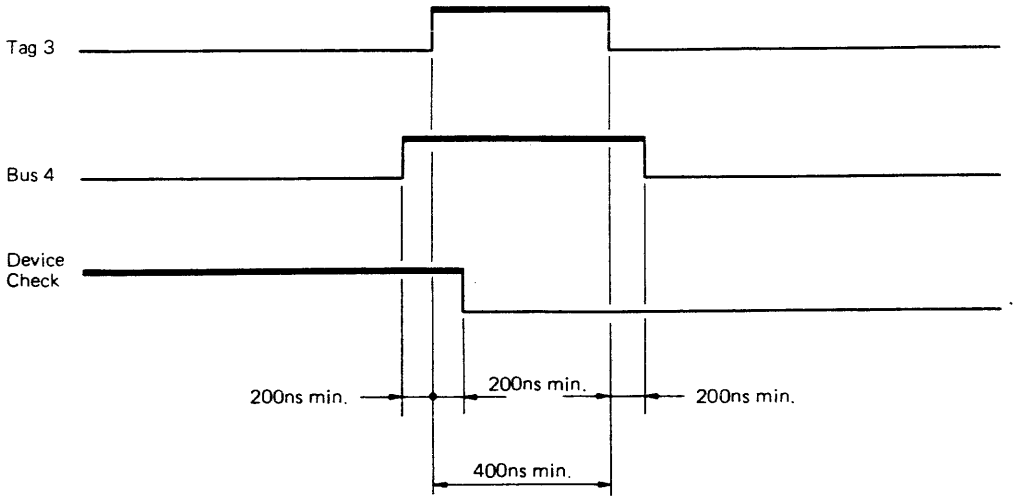
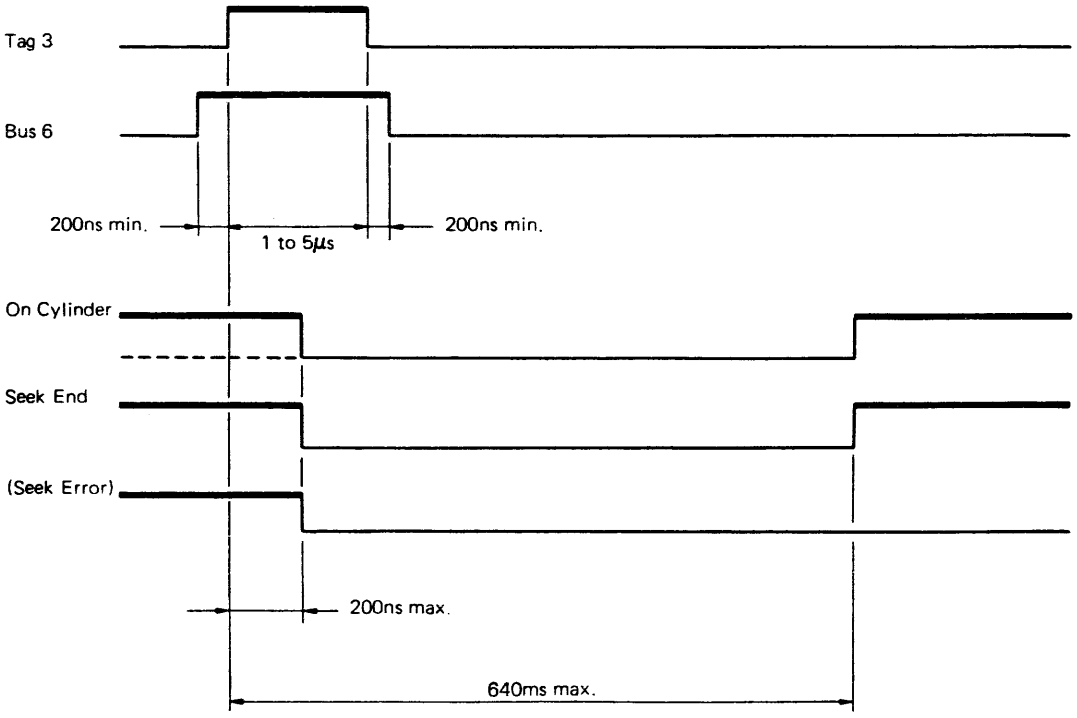


Figure 4-5-15 Fault Clear Timing

4.5.5.9 RTZ Timing

Refer to Figure 4-5-16.



Note: On Cylinder is not always set if a Seek Error occurs.

Figure 4-5-16 RTZ Timing

4.5.5.10 Channel Ready Timing

Refer to Figure 4-5-17.

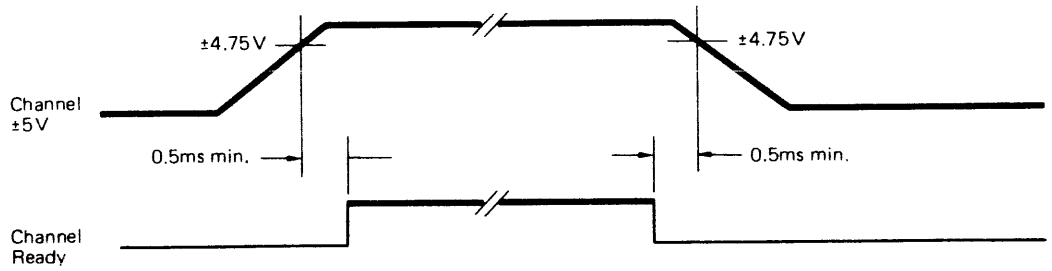


Figure 4-5-17 Channel Ready Timing

4.5.5.11 Tag 4/5 and Status 0 to 5 (optional) Timing

Refer to Figure 4-5-18.

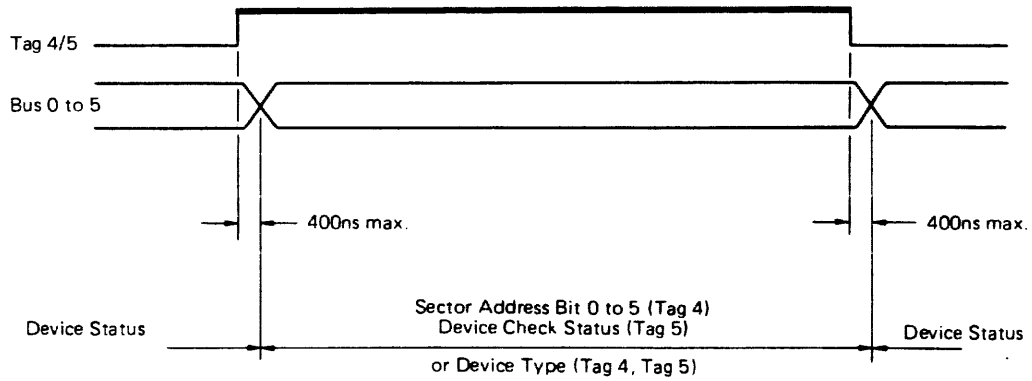


Figure 4-5-18 Tag 4/5 Timing

4.5.5.12 Index/Sector Timing

Refer to Figure 4-5-19.

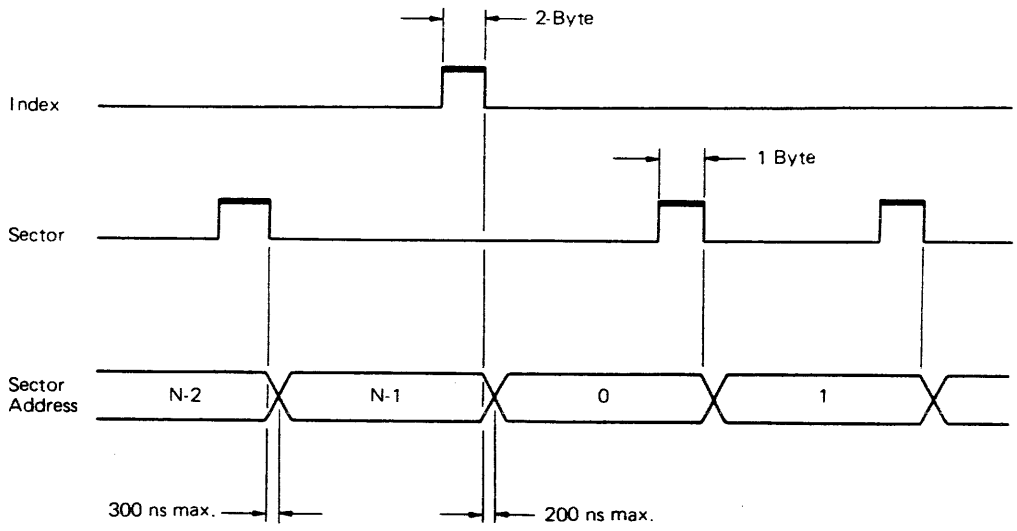
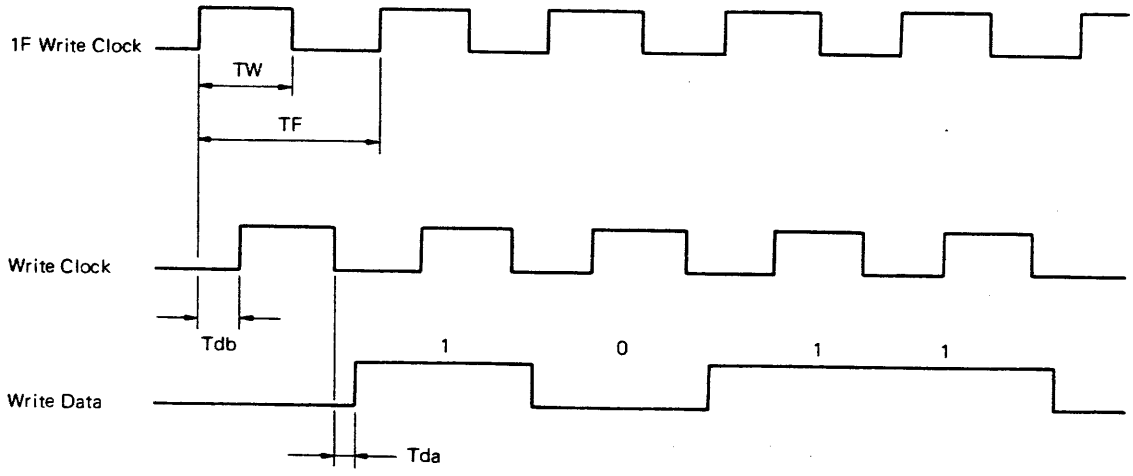


Figure 4-5-19 Index and Sector Timing

4.5.5.13 1F Write Clock, Write Data/Write Clock Timing

Refer to Figure 4-5-20.



Tw = TF/2

TF = 123.6 ns ± 6.2 ns

Tdb = Continuous delay within 2 bits

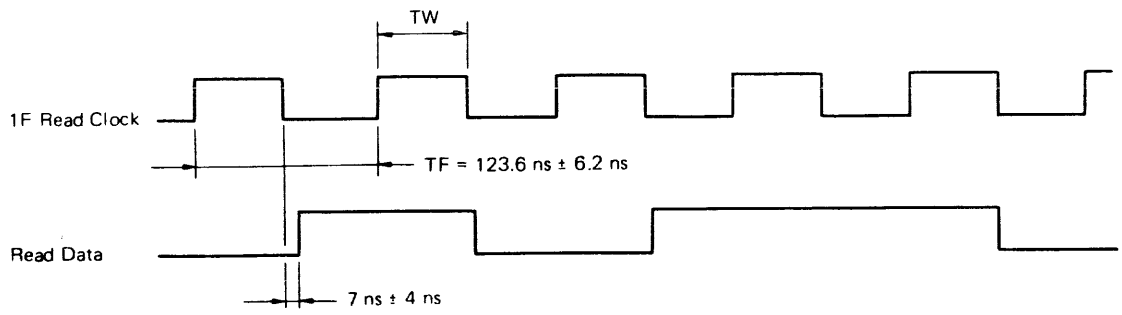
Tda = 0 ± 30 ns

Notes:
1. Write Data and Write Clock timing shall be specified at the output connector of the control unit.
2. The permissible value of TF=123.6ns ± 6.2ns is about ±5%, which includes the rotational speed tolerance, ±4% and the servo jitter, ±1%.
3. NRZ Write Data issued from the control unit is write-compensated and then MFM-modulated for writing on the disk surface.

Figure 4-5-20 Write Data and Write Clock Timing

4.5.5.14 Read Clock/Read Data Timing

Refer to Figure 4-5-21.



Tw = TF/2

Notes: 1. 1F Read Clock and Read Data timing shall be specified at the output connector of the disk unit.

2. Read Data signal should be clocked at the positive-going edge of 1F Read Clock on the control unit.

Figure 4-5-21 1F Read Clock and Read Data Timing

4.5.6 Read/Write Timing

4.5.6.1 Format Write

Refer to Figure 4-5-22.

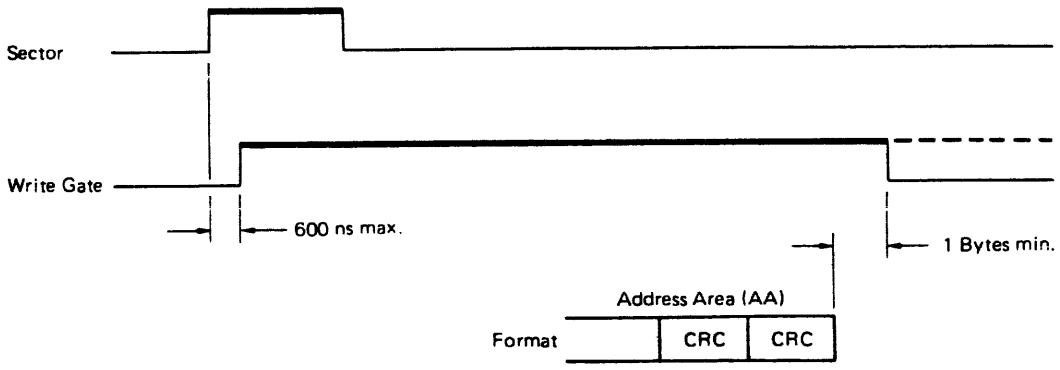


Figure 4-5-22 Format Write Timing

4.5.6.2 Data Write

Refer to Figure 4-5-23.

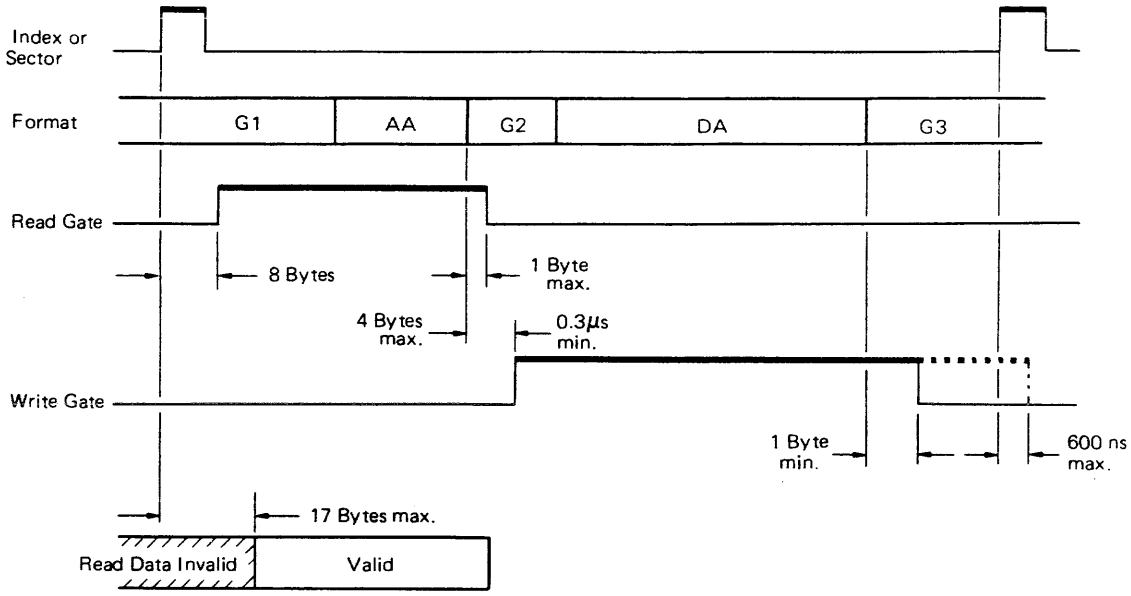
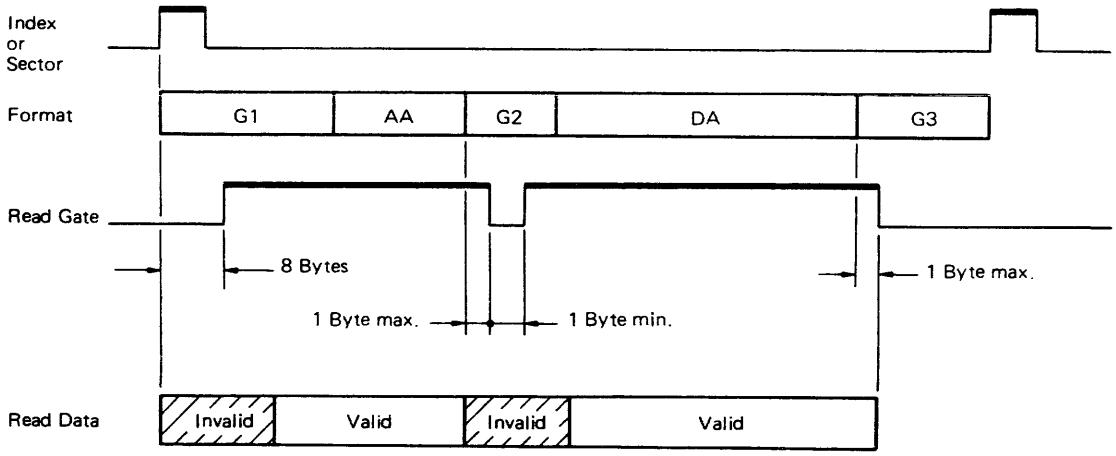


Figure 4-5-23 Write Data Timing

4.5.6.3 Data Read

Refer to Figure 4-5-24.



Notes: 1. The invalid data in the above figure is inhibited in the unit; therefore, it may be disregarded in the control unit.

2. The timing for switching to 1F Read Clock should be performed after the invalid data. In this case, a phase adjustment is required for 1 or 2 bits.

Figure 4-5-24 Read Data Timing

4.5.6.4 AM Write (Variable Soft Sector Only)

Refer to Figure 4-5-25.

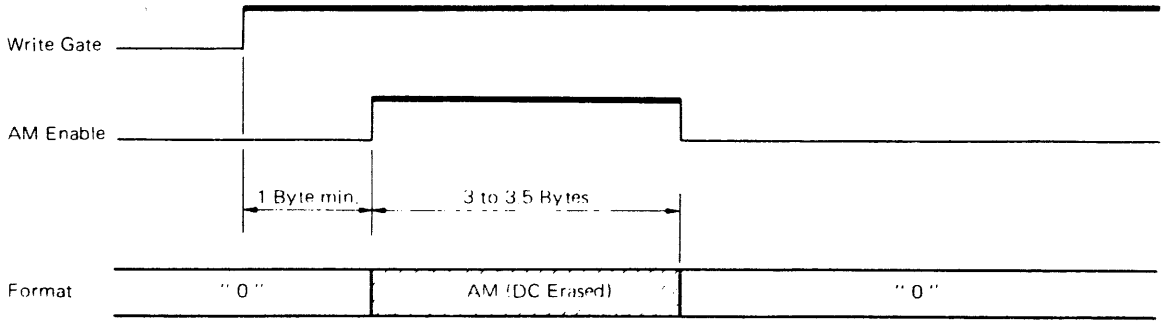


Figure 4-5-25 AM Write Timing

4.5.6.5 AM Read (Variable Soft Sector)

Refer to Figure 4-5-26.

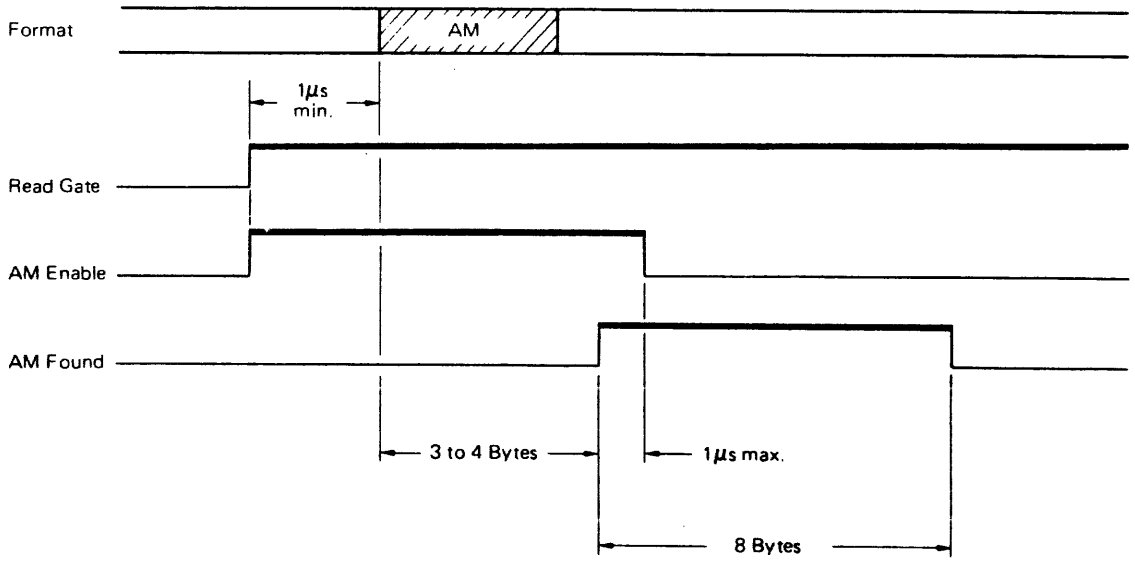


Figure 4-5-26 AM Read Timing

4.5.6.6 Write-To-Read Recovery Time

Refer to Figure 4-5-27. When head selection has been stabilized, the recovery time before Read Gate can be enabled after Write Gate goes false is 10 μs minimum.

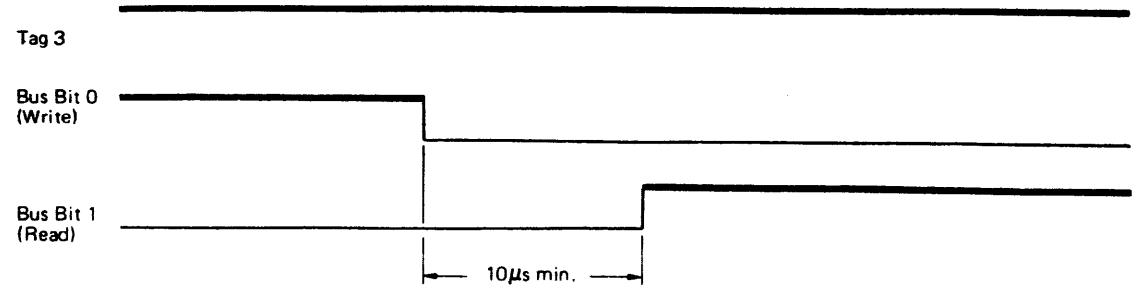


Figure 4-5-27 Write-To-Read Recovery Time

4.5.6.7 Head Select Transient

Refer to Figure 4-5-28. There is a 5 μs delay within the disk drive due to circuit characteristics between the deselection of one head and the selection of another head.

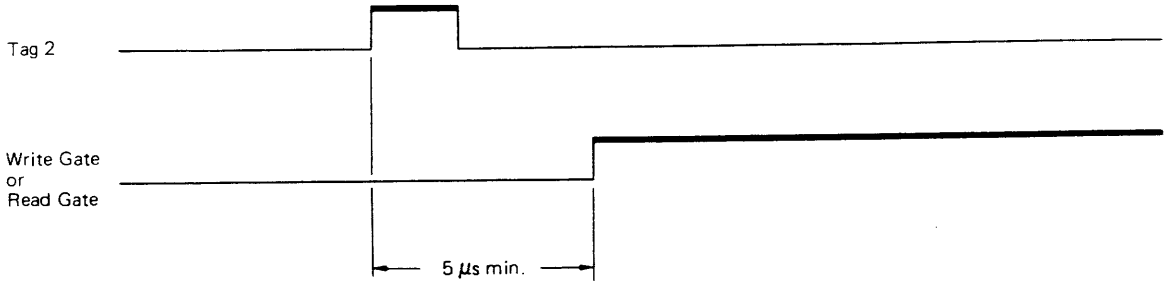
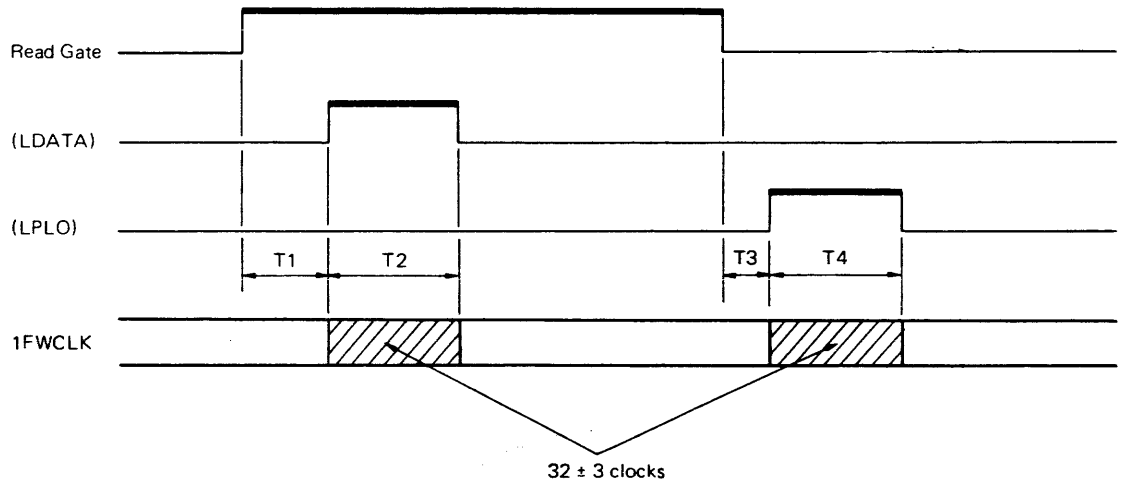


Figure 4-5-28 Head Select Transient

4.5.6.8 1F Write Clock in Reading

In the read operation, the 1F Write Clock signal fluctuates slightly within the Lock-To-Data or Lock-To-PLO signal (internal signal of Variable Frequency Oscillator circuit), in shown as Figure 4-5-29.



T1:–30 to 35 bits;
T2/T4:–32 bits (4 Bytes);
T3:–2 to 11 bits.

Figure 4-5-29 1F Write Clock in Reading

4.5.6.9 Head Address change at the last gap

This timing is specified for the customer who performs a head address change on the same cylinder in the last gap (Gap 3) of the sector.
The customer who does not require this timing should use the timings of items.

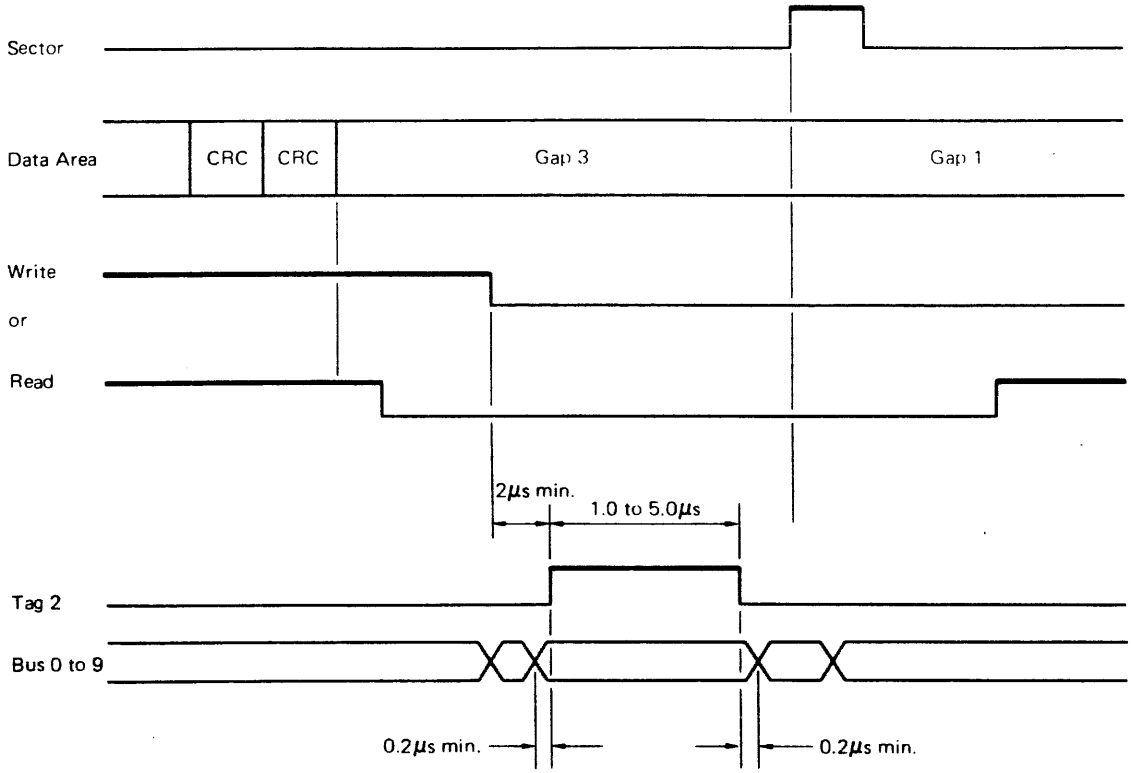


Figure 4-5-30 Head Address Change at the Last Gap

4.5.7 Interface Transmission

4.5.7.1 Driver and Receiver

Transmitters and receivers of SN75110 and SN75107 or equivalent are used to provide a terminated, balanced-line transmission. The Driver is SN75110 or equivalent, and the Receiver is SN75107/SN75108 or equivalent.

(1) Driver

Refer to Figure 4-5-31 and Table 4-5-4.

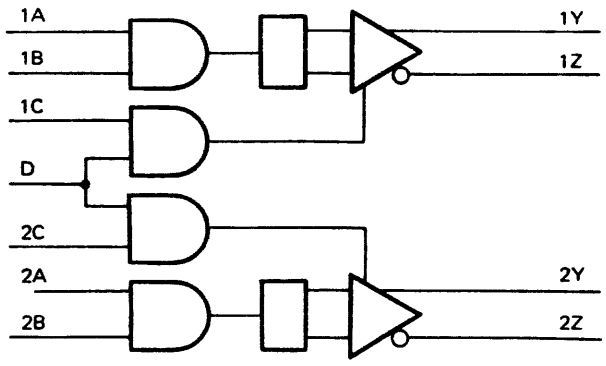


Figure 4-5-31 Drive Logic Diagram (SN75110)

Table 4-5-4 SN75110 Function Table

Logic Inputs		Inhibit Input		Outputs	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

Note: H—High Level, L—Low Level, X—Irrelevant.

(2) Receiver

Refer to Figure 4-5-32 and Table 4-5-5.

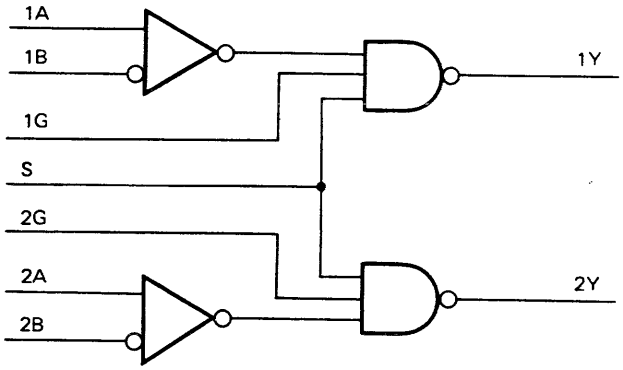


Figure 4-5-32 Receiver Logic Diagram (SN75107/75108)

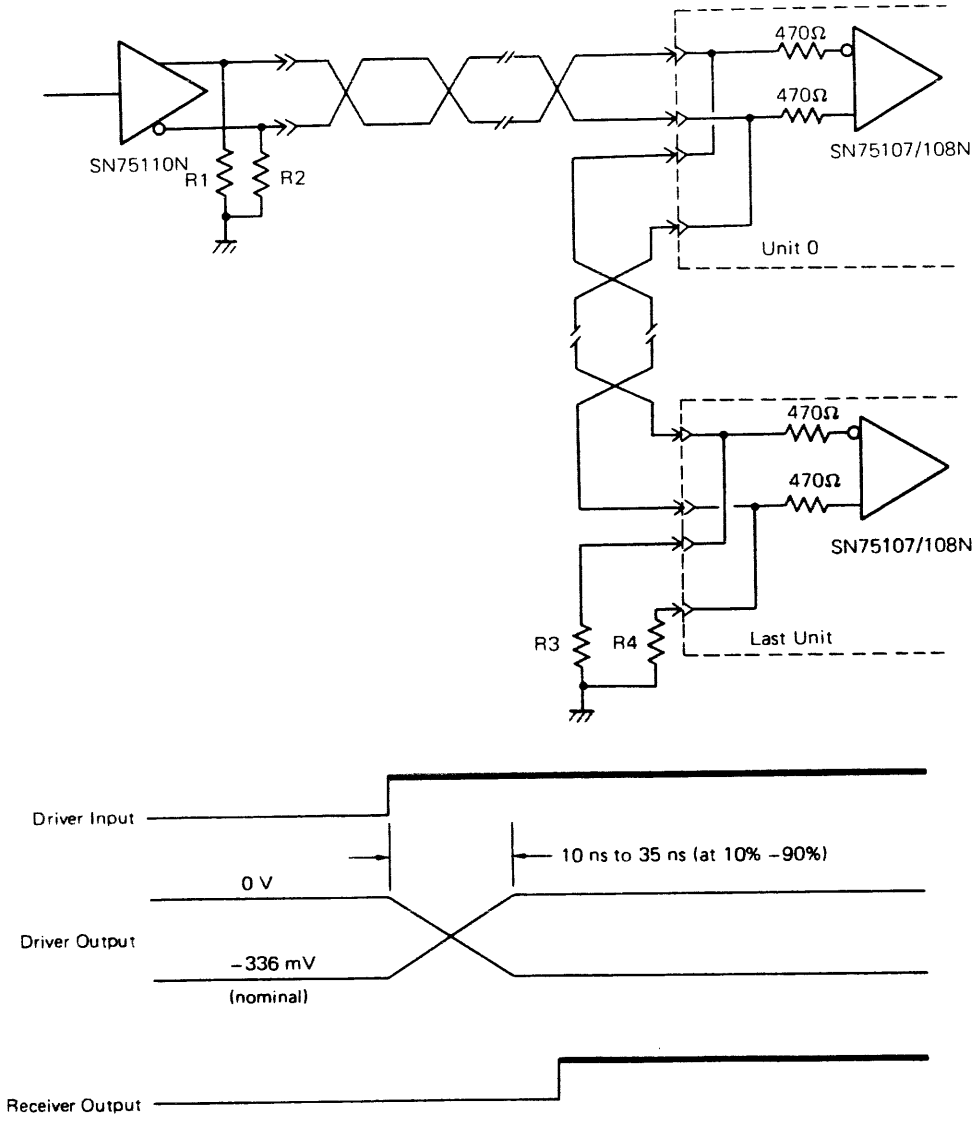
Table 4-5-5 SN75107/75108 Function Table

Differential Inputs	Strobes		Output
	G	S	Y
A–B ≥ 25 mV	X	X	H
–25 mV<A–B<25 mV	X	L	H
	L	X	H
	H	H	Indeterminate
A–B ≤ –25 mV	X	L	H
	L	X	H
	H	H	L

Note: H—High Level; L—Low Level; X—Irrelevant.

4.5.7.2 "A" Cable (Control Cable) Transmission

Refer to Figure 4-5-33.



Notes: 1. Line terminators are located on the unit and the controller. R1 to R4: 56 Ω ± 5 %, 1/10W.

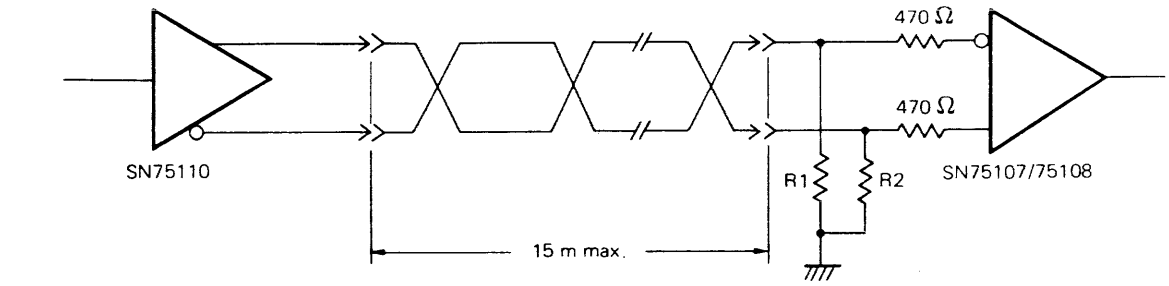
2. A line terminator is located on the terminator assembly of the last unit in the daisy chain configuration.

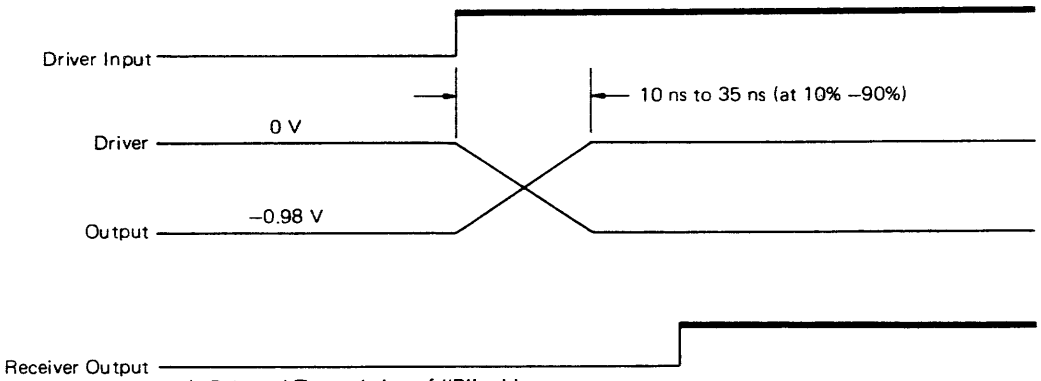
3. The maximum cable length is 30 meters.

Figure 4-5-33 Balanced Transmission of "A" Cable

4.5.7.3 "B" Cable (Data Cable) Transmission

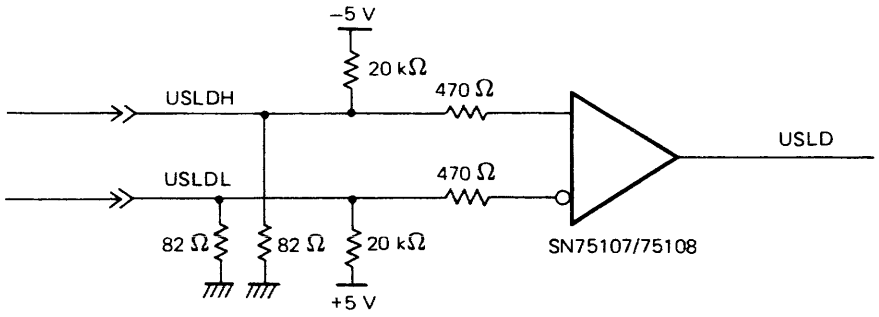
Refer to Figure 4-5-34.





a) Balanced Transmission of "B" cable

Note:
1. Cable shall be flat with characteristic impedance of 100 ± 10 ohms.
2. Line terminators are located on the receivers at the drive or control unit. R1 and R2 are 82 ohms ± 5%, 1/10W.
3. The protect resistors (470 ohms) should be located on the receiver side. 470 Ω ± 5 %, 1/10W.
4. A bias network should be used to prevent disturbance conditions by power failure at the control unit end of Unit Selected and Seek End signals as in b).



b) Bias Network to Prevent Power Failure Disturb

Figure 4-5-34 Balanced Transmission "B" Cable

4.5.7.4 Channel Ready Driver

The Channel Ready signal must be issued so that data is protected during a power failure of the control unit. Relay logic and passive terminations sometimes aid this requirement. If SN75110A drivers are used to drive the Channel Ready signal from the control unit, dual drivers should be connected in parallel, and no 56 ohm termination to ground should be used at the control unit.

4.5.8 Connector and Cable

4.5.8.1 Connector

(1) A – Cable connector 60 pos.

	Ansley	Fujitsu
Unit Side:	609-6052MR	FCN-702P060-AU/M (Wire wrapping)
	–	FCN-704P060-AU/M (Straight)
	–	FCN-705P060-AU/M (Right Angle)
Cable Side:	609-6001M	FCN-707J060-AU/B

(2) B – Cable Connector 26 pos.

	Ansley	Fujitsu
Unit Side:	609-2652MR	FCN-702P026-AU/M (Wire wrapping)
	–	FCN-704P026-AU/M (Straight)
	–	FCN-705P026-AU/M (Right Angle)
Cable Side:	609-2601M	FCN-707J026-AU/B

4.5.8.2 Cable

(1) A – Cable
SS-455-248-60 SPECTRA STRIP
ZO = 100Ω ± 10Ω, 28 AWG, 7 strands

(2) B – Cable
174-26 Ansley, 3476-26 3M
ZO = 100Ω ± 15Ω, 28 AWG, 7 strands

4.5.9 Connector Pin Assignment

4.5.9.1 A – Cable Connector 60 Pin

Table 4-5-6 A – Cable Pin Assignment

1	Tag 1 L	31	Tag 1 H
2	Tag 2 L	32	Tag 2 H
3	Tag 3 L	33	Tag 3 H
4	Bus 0 L	34	Bus 0 H
5	Bus 1 L	35	Bus 1 H
6	Bus 2 L	36	Bus 2 H
7	Bus 3 L	37	Bus 3 H
8	Bus 4 L	38	Bus 4 H
9	Bus 5 L	39	Bus 5 H
10	Bus 6 L	40	Bus 6 H
11	Bus 7 L	41	Bus 7 H
12	Bus 8 L	42	Bus 8 H
13	Bus 9 L	43	Bus 9 H
14	Channel 1 Ready L	44	Channel Ready H
15	Status 3 L	45	Status 3 H
16	Status 2 L	46	Status 2 H
17	Status 1 L	47	Status 1 H
18	Index L	48	Index H
19	Status 0 L	49	Status 0 H
20	Status 5 L	50	Status 5 H
21	Busy L	51	Busy H
22	Unit Select Tag L	52	Unit Select Tag H
23	Unit Select 1 L	53	Unit Select 1 H
24	Unit Select 2 L	54	Unit Select 2 H
25	Sector L	55	Sector H
26	Unit Select 4 L	56	Unit Select 4 H
27	Tag 5 L (Selectable)	57	Tag 5 H (Selectable)
28	Status 4 L	58	Status 4 H
29	(Pick)	59	(Hold)
30	Tag 4 L (Selectable)	60	Tag 4 H (Selectable)

4.5.9.2 B – Cable Connector 26 Pin

Table 4-5-7 B – Cable Pin Assignment

1	GND	14	1F Write Clock H
2	1F Write Clock L	15	GND
3	Read Data L	16	Read Data H
4	GND	17	1F Read Clock H
5	1F Read Clock L	18	GND
6	Write Clock L	19	Write Clock H
7	GND	20	Write Data H
8	Write Data L	21	GND
9	Unit Selected H	22	Unit Selected L
10	Seek End L	23	Seek End H
11	GND	24	Index H
12	Index L	25	GND
13	Sector L	26	Sector H

4.6 ELECTRIC CIRCUIT FUNCTION

4.6.1. Start/Stop Function

When power, AC input, DC +5V, DC ±12V and DC +24V, is applied to the FDU from the external power supply unit, the cooling blower is activated. In the case of Remote mode, the AC input to the spindle drive motor and DC +24V is controlled by Pick and Hold signals from the control unit. DC +24V is suppliied to the brake coil of the spindle drive motor assembly and releases the spindle drive motor shaft lock.

When current flows through the brake coil and is detected by the Brake Current Detection circuit, its output activates the relay circuit. Then AC input is supplied to the spindle drive motor through the relay contacts.

The spindle drive motor provides rotating motion to the spindle of the Disk Enclosure through a flat belt. When the disk rotates, a tab on the spindle assembly is detected by the speed transducer, which generates pulses that are used to determine the rotational speed. The output pulse, Speed Signal (SPSG) is applied to Speed Detection circuit. When the rotational speed comes up to 80% of operating speed, Speed OK (SPOK) signal is issued and triggers the start time circuit, and also is sent to the external power supply unit through the power control connector PWC1.
Through this step of power-up sequencing, the actuator is held in the Landing Zone (IGB2) by a stopper magnet. When the Speed OK signal goes true, current flows through the coil of the Voice Coil Motor (VCM) on the actuator and the heads are kept in the Landing Zone electrically.

Five seconds after SPOK goes true, Guard Band Enable is activated. Ten seconds after SPOK, Start Pulse (STARTP) goes true. The Guard Band Enable signal allows detection of Guard Band signals, and Start Pulse activates the Initial Seek operation.

The stop sequence is initiated when input power is shut-off. The FDU does not require DC power sequencing, therefore, the stop sequence is initiated in various ways.

If DC+24V drops below +10V, the VCM Driver circuit is turned off and the actuator returns to the Landing Zone driven by the Retract Capacitor discharge. If there is a further reduction of DC+24V, the spindle motor brake is activated and the drive motor stops. If DC+5V or DC±12V goes false, the same sequence occurs.

Also, if DC+5V or DC±12V goes false, Power Ready (PWRDY) goes false.

If PWRDY signal is disabled, the actuator returns to the Landing Zone and Unit Ready (URDY) signal goes false.

With the loss of AC input, the rotational speed will decrease slowly and then Speed OK signal will go false to retract the heads to the Landing Zone.

The Start/Stop block diagram is shown in Figure 4-6-1, timing chart in Figure 4-6-2, start sequence flow chart in Figure 4-6-3, and stop sequence flow chart in Figure 4-6-4.

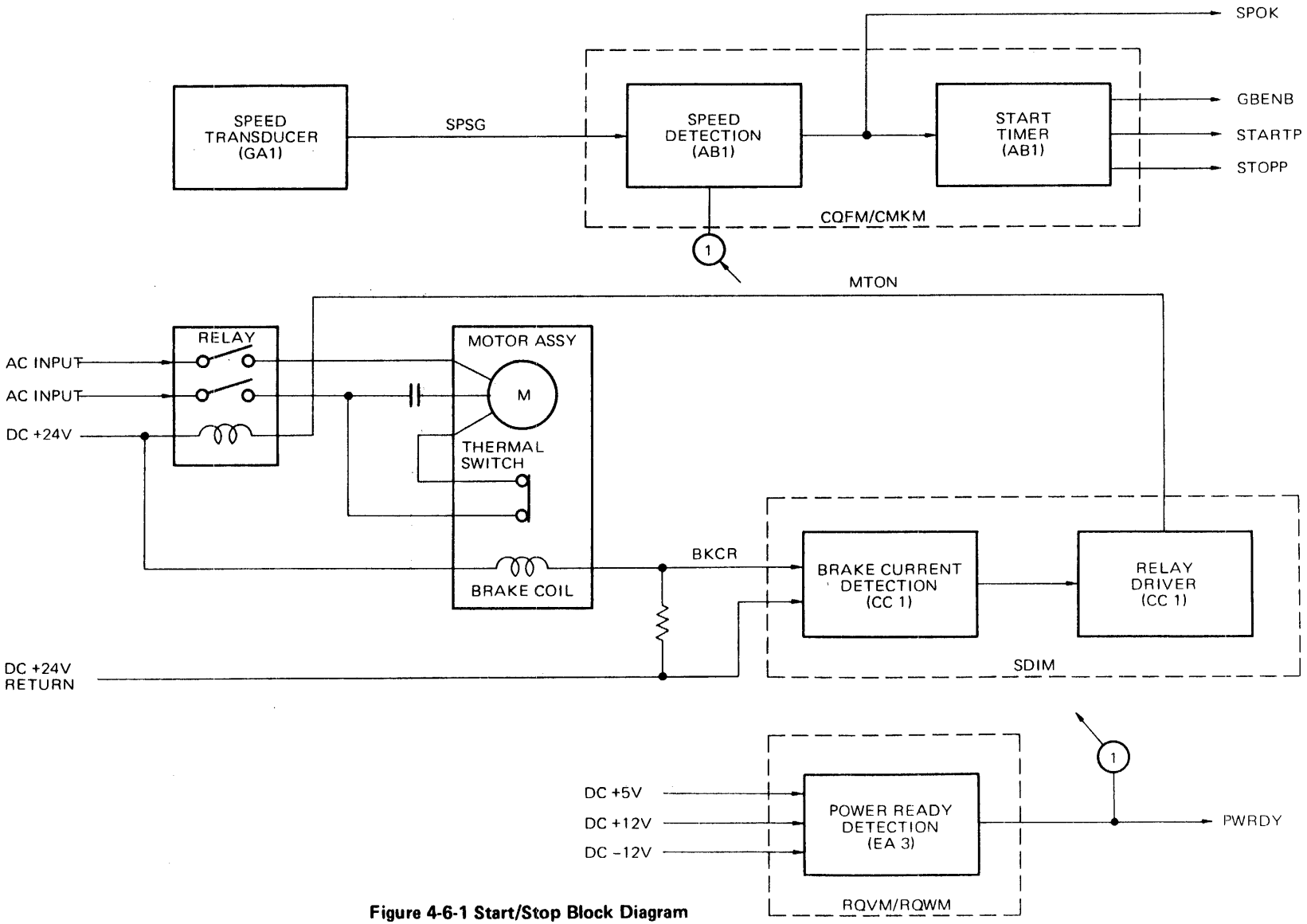


Figure 4-6-1 Start/Stop Block Diagram

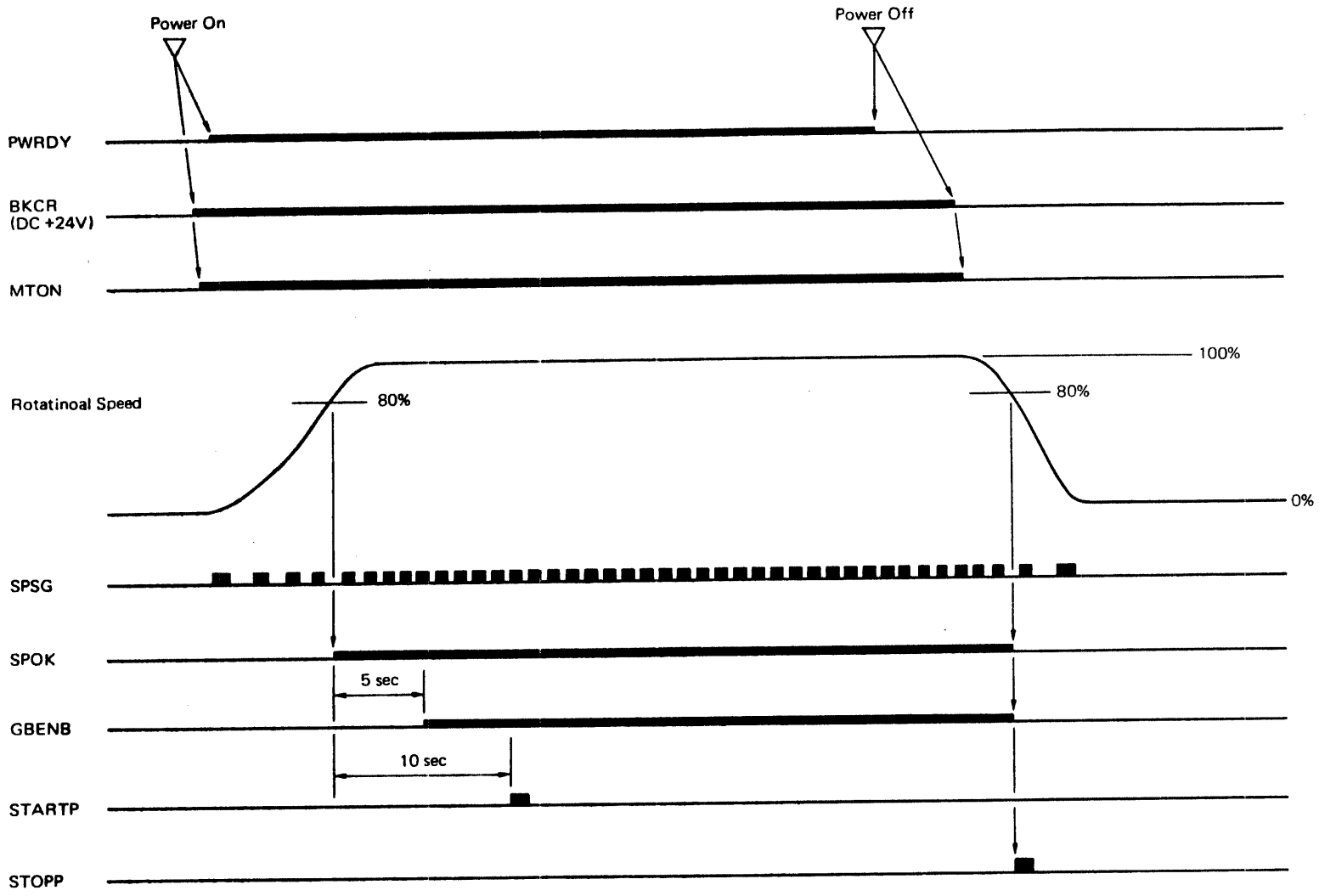


Figure 4-6-2 Start/Stop Timing Chart

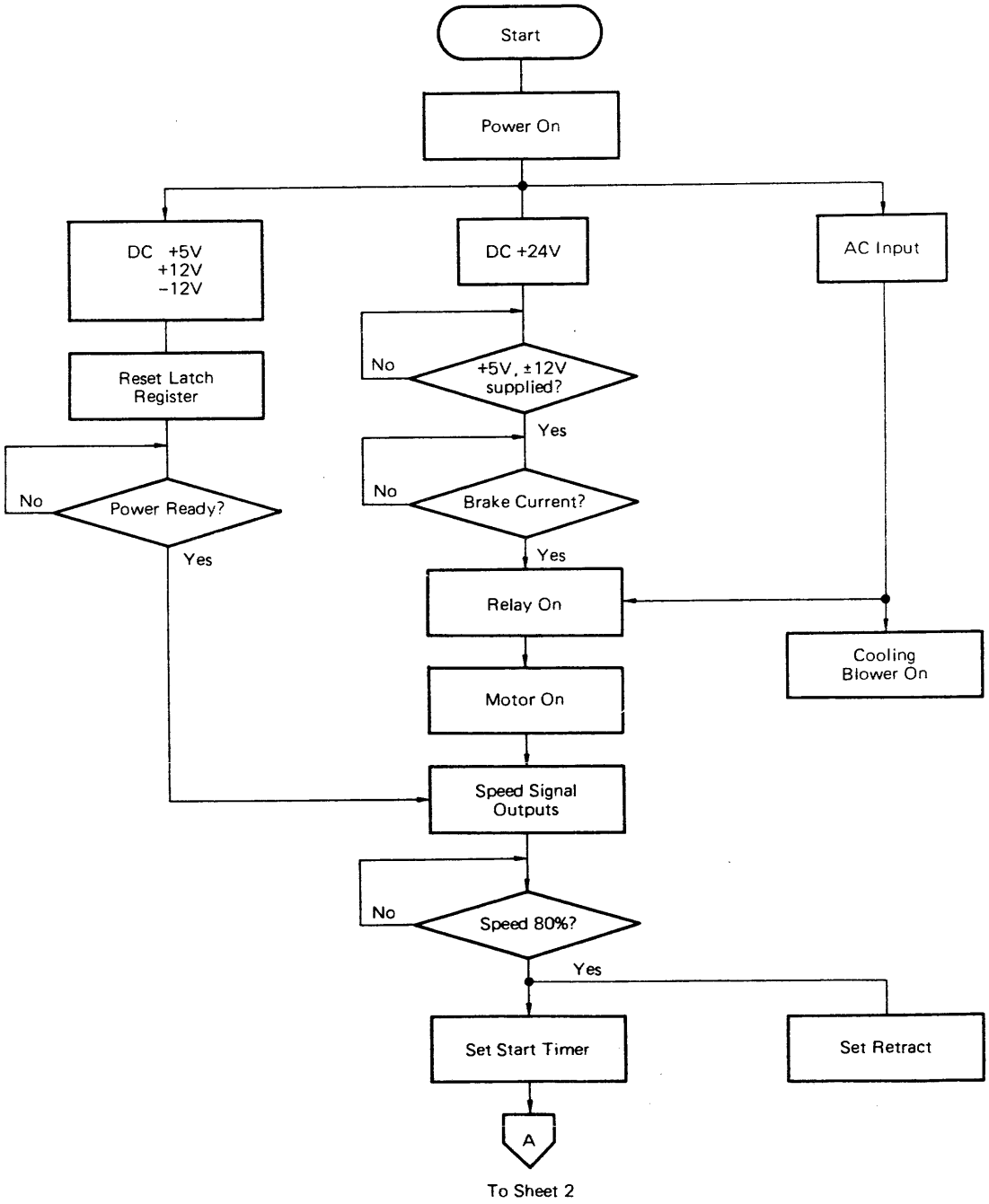


Figure 4-6-3 Start Sequence Flow Chart (Sheet 1 of 2)

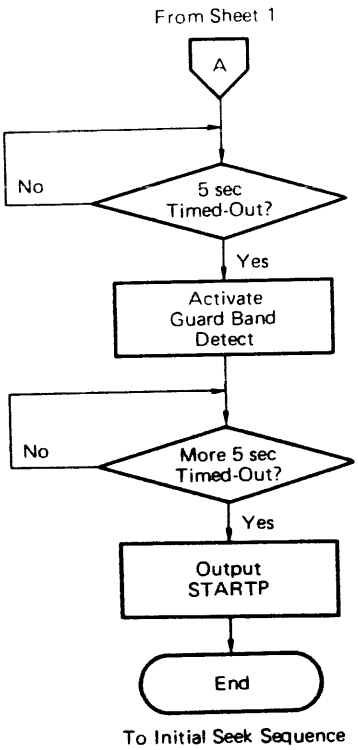


Figure 4-6-3 Start Sequence Flow Chart (Sheet 2 of 2)

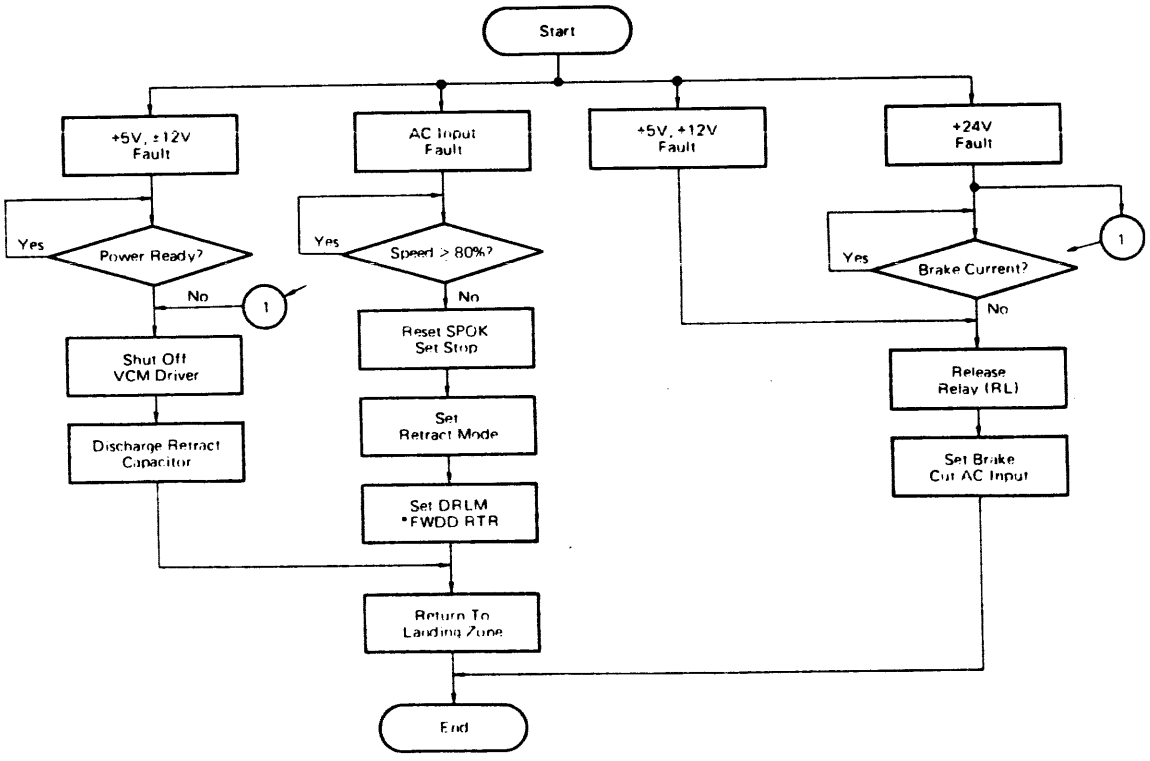


Figure 4-6-4 Stop Sequence Flow Chart

4.6.2 Unit Selection

The FDU must be selected before it will respond to any commands from the control unit. Tag and Bus receivers are not enabled until the unit is selected.

This describes the dual port functions related to selection. They are as follows:

- Unit address select
- Reserve
- Release
- Priority select (unconditional reserve)
- Disable with a maintenance switch

The functional block diagram of dual port is shown in Figure 4-6-5.

4.6.2.1 Unit Address Select and Reserve

A unit is selected or reserved in an identical sequence which is initiated by Unit Select Tag (USLTG) and a unit address signal (Unit select 1, 2, 4: USL 1, 2, 4). However, this sequence cannot start when:

- The unit is selected and reserved by the opposite channel.
- The unit is not selected, but reserved by the opposite channel.
- The channel which has attempted to select the unit is disabled by the maintenance switch on the unit or because the unit is placed in the Priority Select state by the opposite channel.

The select/reserve sequence is as follows:
Suppose that the unit is ready to be selected that is, any of the above three condition does not exist. A controller sends USLTG and USL 1, 2, 4 to the unit. If the unit address from the channel-A controller agrees with the logical unit number (LUN), the unit sends Unit Selected to the channel-A controller through cable B when Channel-A Compare (CHAMCP) is sent to the XCBM printed circuit board. This sequence is the same as with the single-port configuration.

Unless the unit is selected or reserved by channel-B and, as a result, is Busy, CHACMP causes the Channel A Selected signal (CHASLD) to be sent in synchronization with Clock 1 (CLK1) from the oscillator. CHASLD turns on the Channel-A Enable (CHAENB) signal to make the driver/receiver for Channel-A ready for transmission/reception, drive the LED to indicate CHASLD, switch the WDAT/WCLK multiplexer to Channel-A, set Busy to indicate that the unit is selected or reserved by the Channel-A controller, and trigger the Set Reserve (STRSV) one-shot multivibrator to set the reserve latch.

If channels-A and B attempt to select a unit at the same time, CLK1 and CLK2 (clocks with the same frequency and different phases) determine which channel is to access the unit. As a result, Busy is set.

The STRSV one-shot multivibrator output sets the Channel A Reserved (CHARSV) latch about 300 ns after CHASLD. This CHARSV signal turns on the LED on the XCBM printed circuit board, sets BUSY A, and sets Seek End B (SKENDB) to "1" before its transmission to Channel-B. SKEND to Channel-B is kept "1" as long as the unit is reserved by Channel-A.

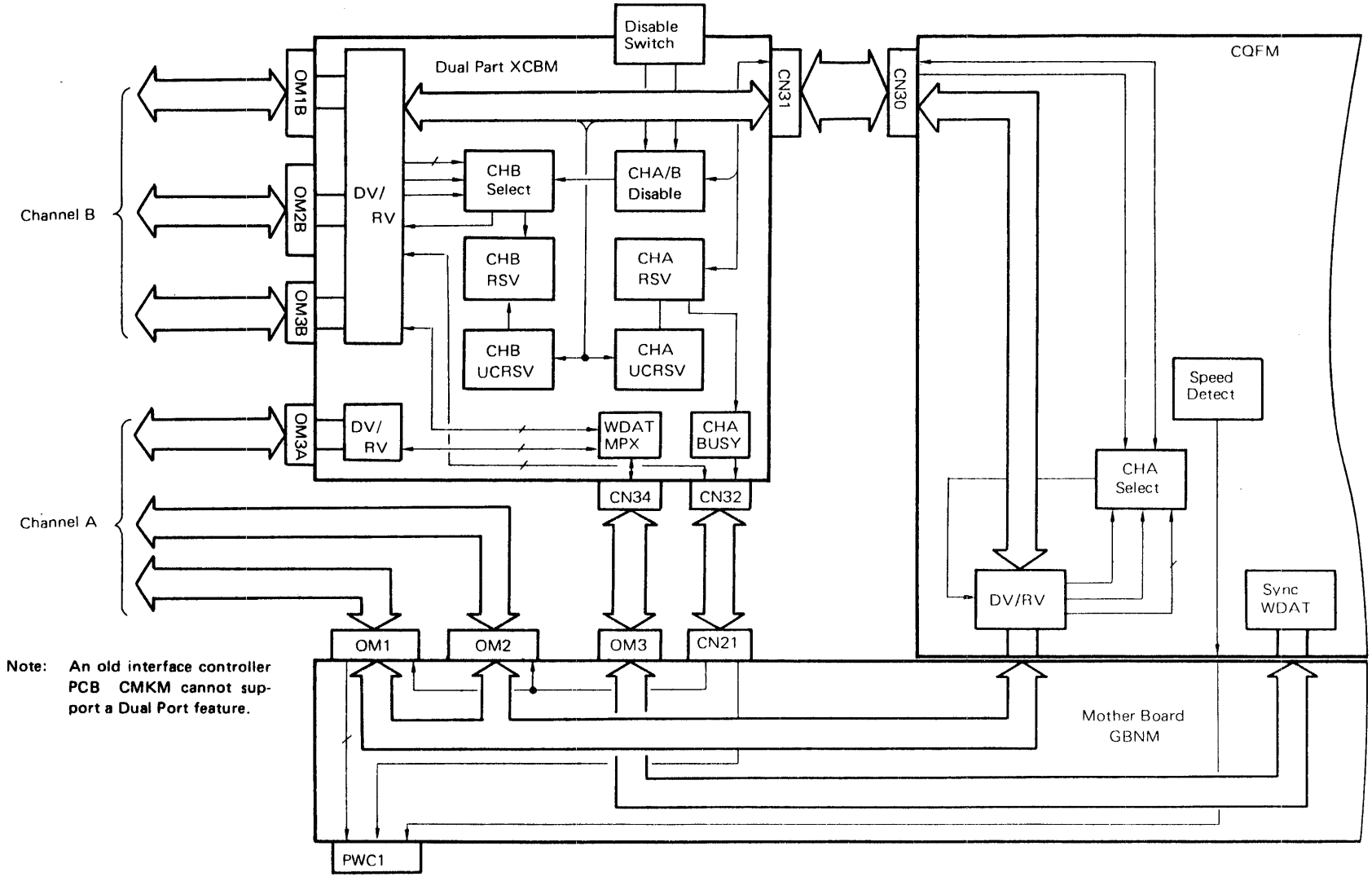
The unit is kept selected/reserved by Channel-A until Channel-A is disabled by the maintenance switch or until USLTG becomes false. When Channel-B attempts to select the unit, the unit sends BUSYA as a busy signal to Channel-B, and sends also Unit Selected B (USLDB) to indicate that it is selected/reserved by Channel-A.

Even when USLTG from Channel-A goes false after the select/reserve sequence, the unit remains reserved by Channel-A. This reserved state is not reset until a Release command comes from Channel-A, Channel-A is disabled by the maintenance switch, Channel-B performs Priority Select, or the power is turned on/off.

If the opposite channel control unit attempts to select own channel while it is selected or reserved by the own channel control unit (i.e. in Busy state), Tried Latch in the dual port is set. Thus, at the time when the own channel becomes neither selected nor reserved, Seek End goes false for 30μs so that the opposite channel having been waiting can be indicated an interrupt.

If the unit is in Disabled state (realized by Priority Select from the opposite channel or by Disable switch) and own channel attempts to select the unit, no signal response is activated.

The block diagram of the select/reserve circuit is shown in Figure 4-6-6, and the related flowchart and timing chart are shown in Figures 4-6-7 and 4-6-8, respectively.



Note: An old interface controller PCB CMKM cannot support a Dual Port feature.

Figure 4-6-5 Functional Block Diagram of Dual Port

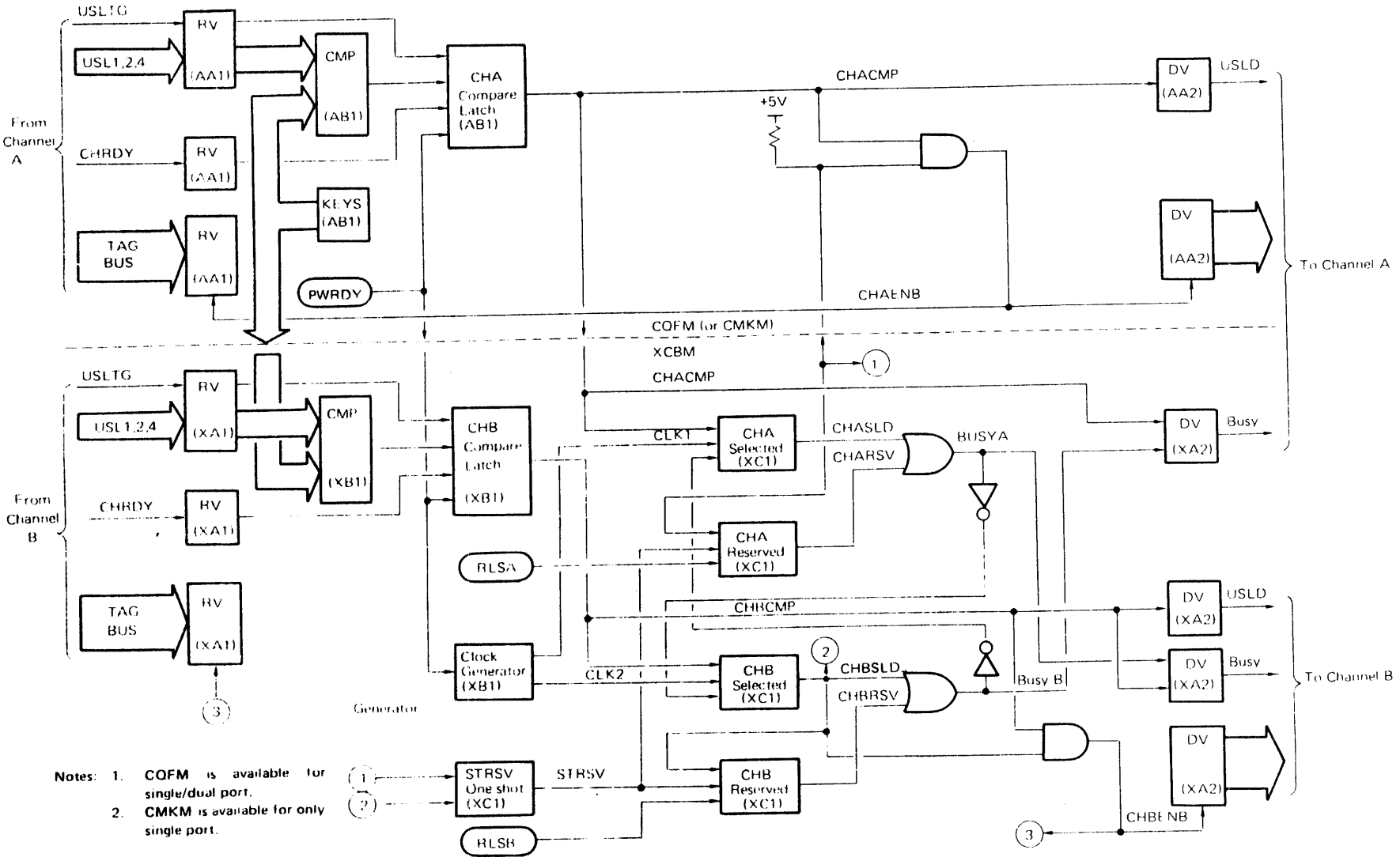


Figure 4-6-6 Functional Block Diagram of Select/Reserve

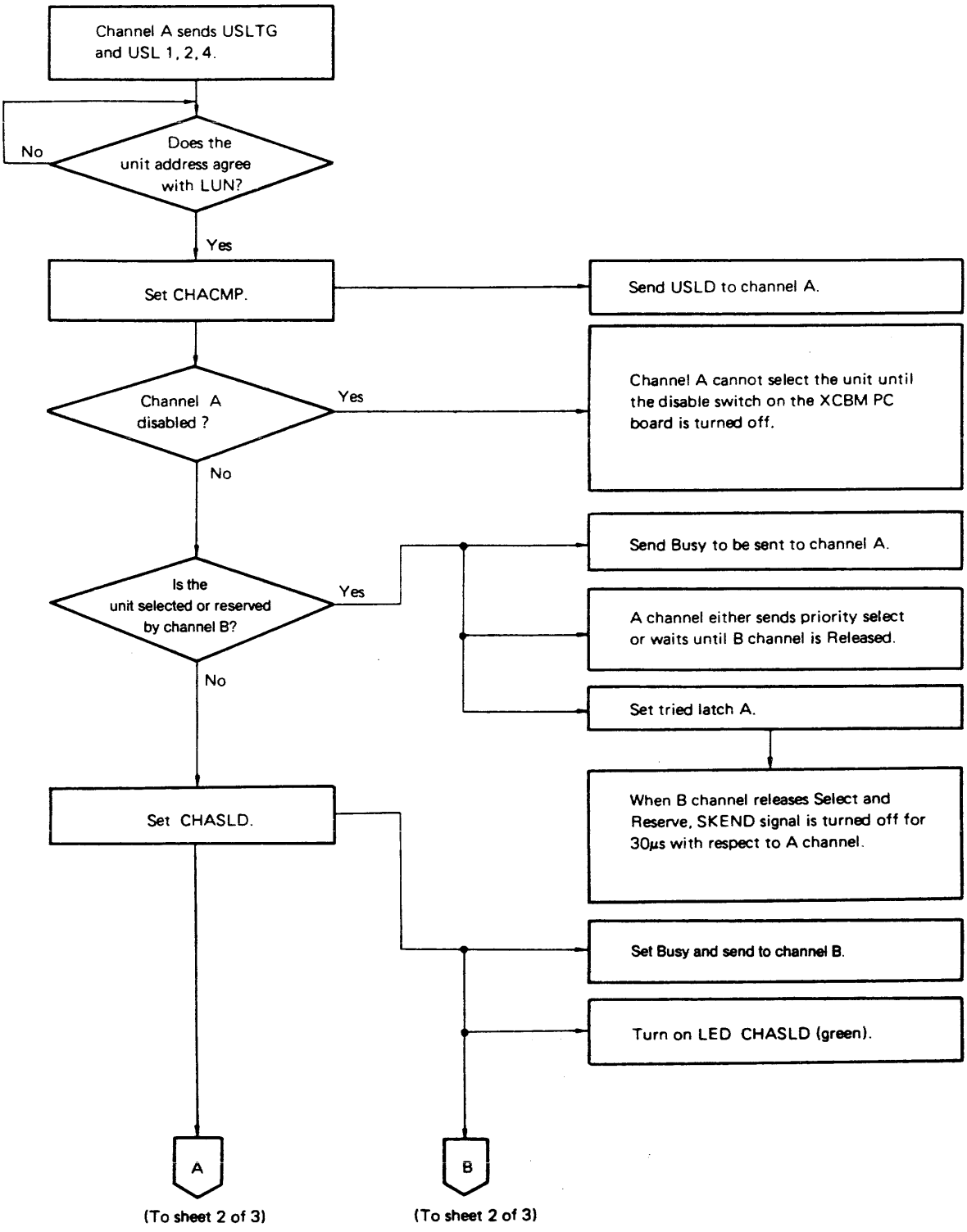


Figure 4-6-7 Select/Reserve Flow Chart (Sheet 1 of 3)

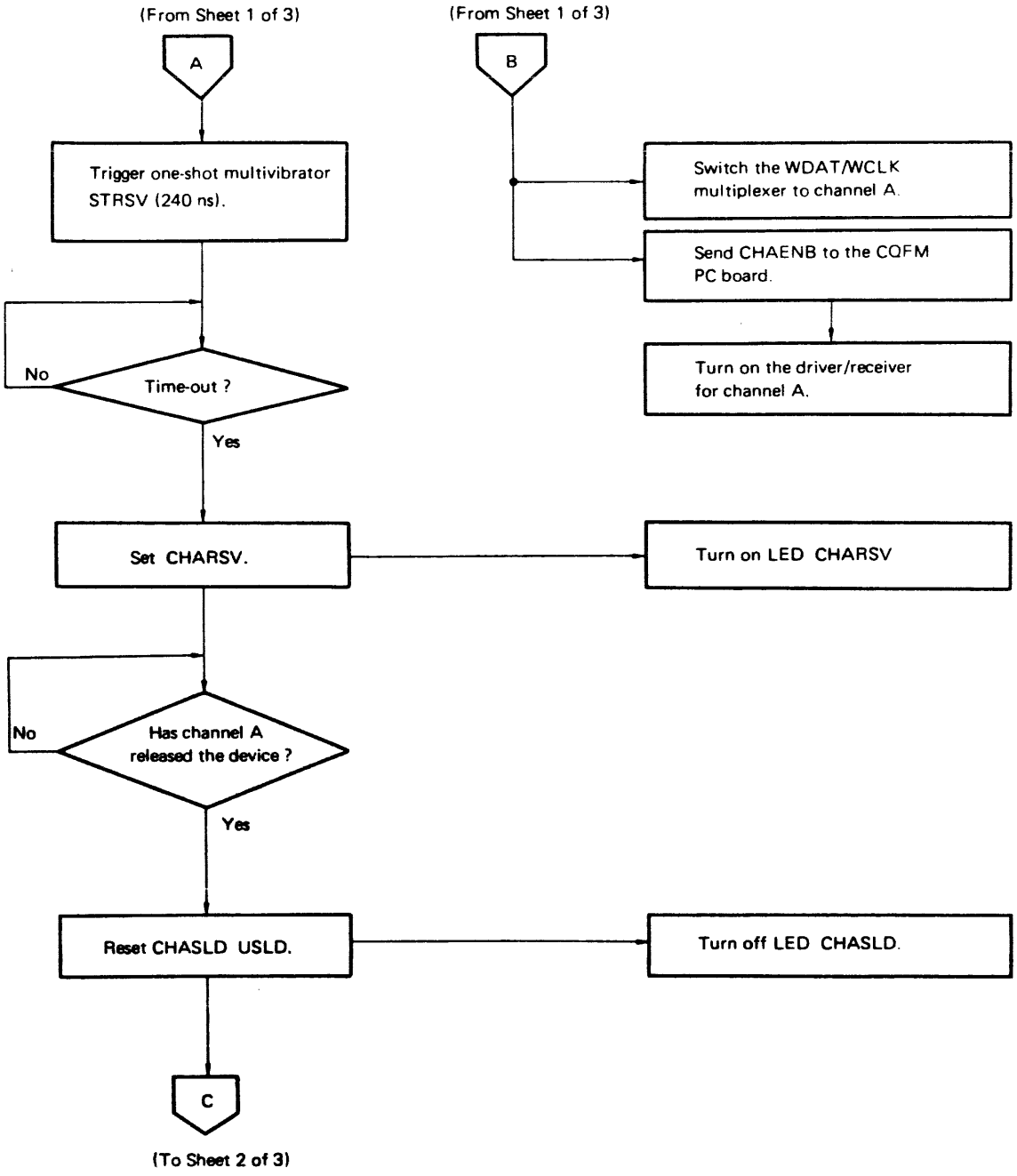


Figure 4-6-7 Select/Reserve Flowchart (Sheet 2 of 3)

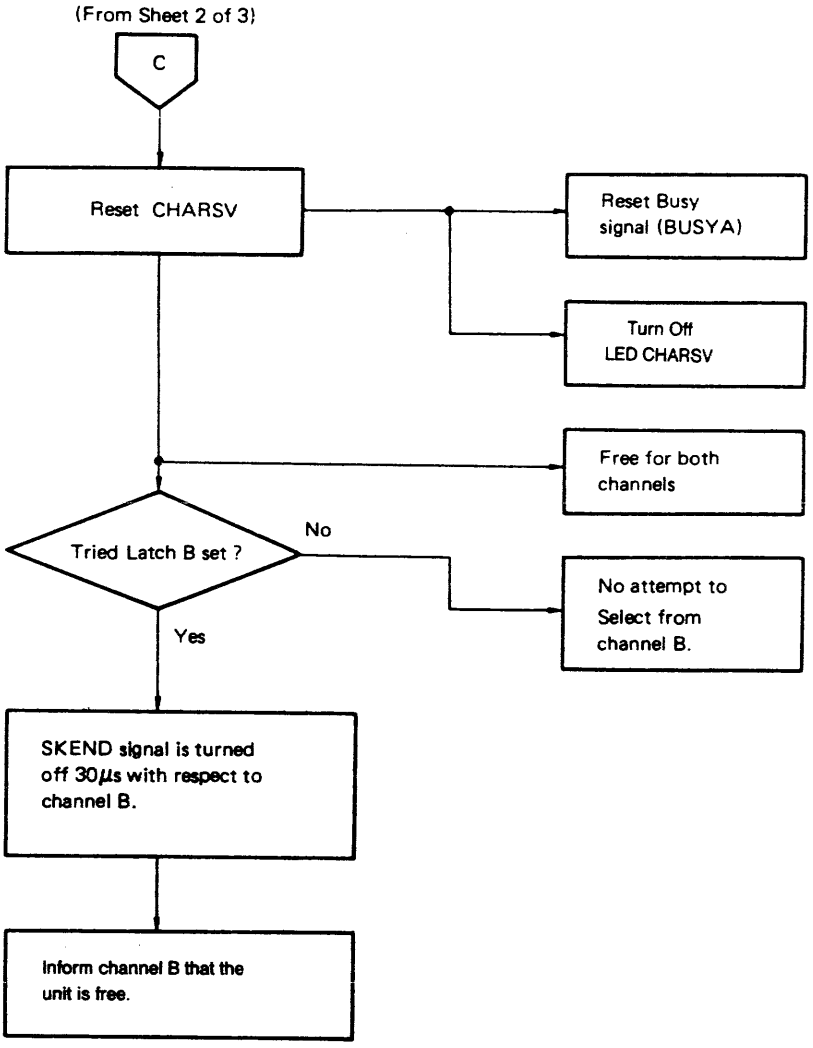


Figure 4-6-7 Select/Reserve Flowchart (Sheet 3 of 3)

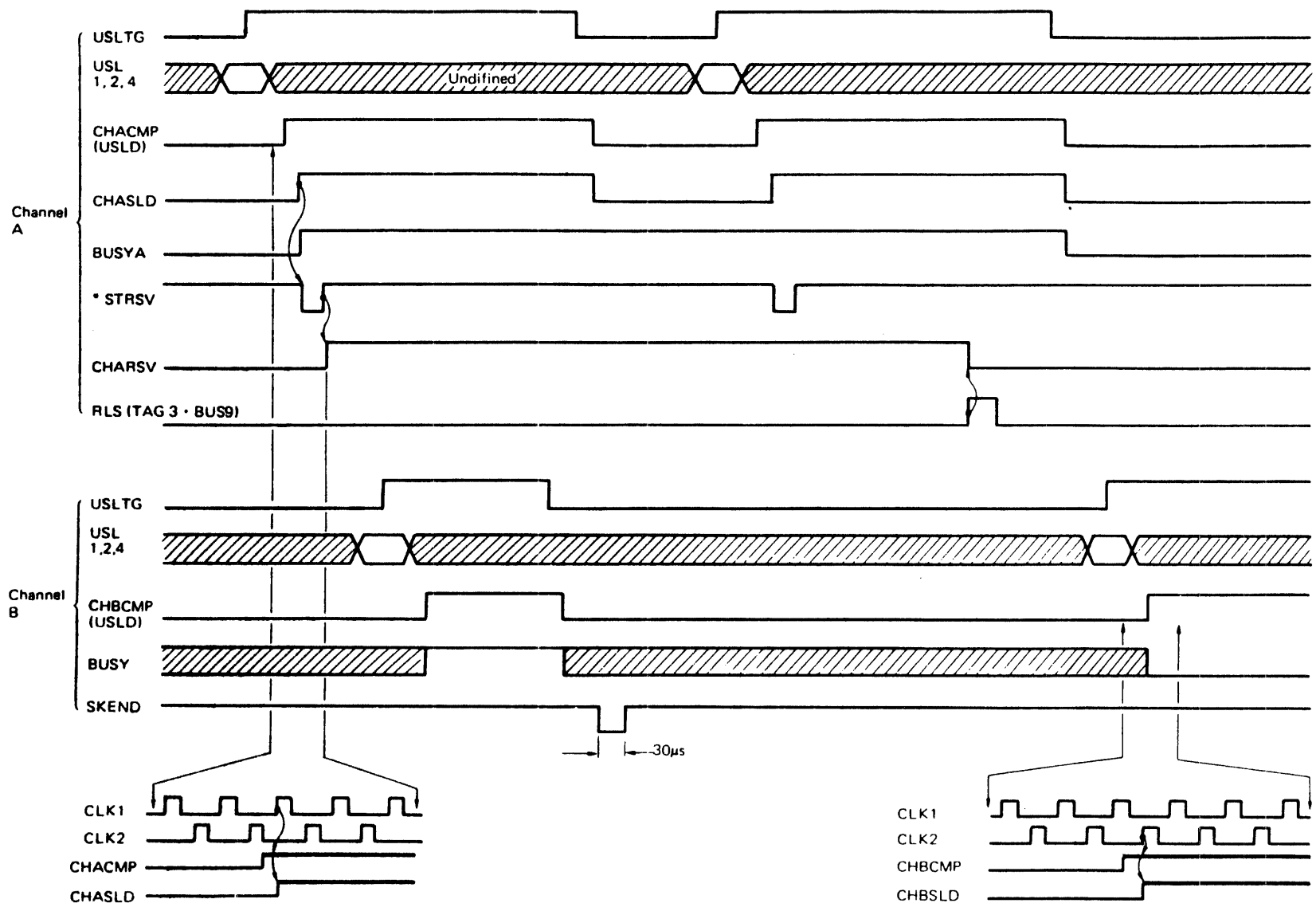


Figure 4-6-8 Select/Reserve Timing Chart

4.6.2.2 Release

The release command resets the reserved and priority select (unconditional reserve) states. Release is executed by two functions described in the following. One is a release command from a control unit (Tag 3 Bus bit 9) and the other is Release Timer of the dual port option.

(1) Release command (Tag 3, Bus bit 9)
Reserve and Priority Select (unconditional reserve) are reset by the leading edge of Tag 3 and Bus Bit 9 sent from the control unit. Thus, it is made possible to be accessed from the control unit of the opposite channel.

(2) Release Timer
If the switch on the dual port is set to the RLTM position. The Release function is enabled by the unit itself. If unit Select Tag signal goes false when the switch is being set at the RLTM position, the Release Timer one-shot of 500 ms is triggered. The Reserve Latch is reset by the trailing edge of the Release Pulse.
If the switch is set to ABSL (Absolute Reserve) side, the one-shot is disabled.

4.6.2.3 Priority Select (Unconditional Reserve)

Even if a unit is selected or reserved (except unconditional reserve) by a channel, the opposite channel can switch the unit to this channel by issuing a Priority Select (Unit Select Tag, unit address and Bus Bit 9) command.

The command sets the Unconditionally Reserved (UCRSV) latch to inhibit all signals, Select/Reserve is given to the channel and, at the same time, the channel which was previously connected is disconnected. Once it is set in an unconditional reserve state, all signals are disabled for respect to the opposite channel.

The Unconditionally Reserve is released only by the release command given by the channel exclusively connected.

4.6.2.4 Disable Switch

During maintenance the interface functions related to channels A and B can be inhibited by using the maintenance switch on the XCBM printed circuit board. This disable function can be done for the two channels separately.

4.6.3 Seek Control Function

Basically, the FDU has five types of seek modes: Initial Seek, Return To Zero (RTZ), Direct Seek by Tag 1, Head Retract and Linear mode.

(1) Initial Seek Mode
The Initial Seek mode causes the head to position onto cylinder zero from Landing Zone.

(2) Return to Zero Mode
The Return to Zero (RTZ) mode causes the heads to move to cylinder zero, regardless of where they are when the command is received. Basically Return To Zero mode is equivalent to the Initial Seek mode; therefore, they are referred to as the Go To Zero (GTZ) mode.

(3) Direct Seek by Tag 1
Direct Seek mode causes a seek to the cylinder address specified by the Tag 1 and Bus 0 to 9 signals from the control unit.

(4) Head Retract Mode
Head Retract Mode causes the heads to return to the Landing Zone if a power failure or abnormal positioning operation occurs.

(5) Linear Mode
Linear Mode causes the heads to track (follow) the center of the specified cylinder after a seek operation has been completed. An offset operation is included with this mode.

The Seek Control Block Diagram is shown in Figure 4-6-9.

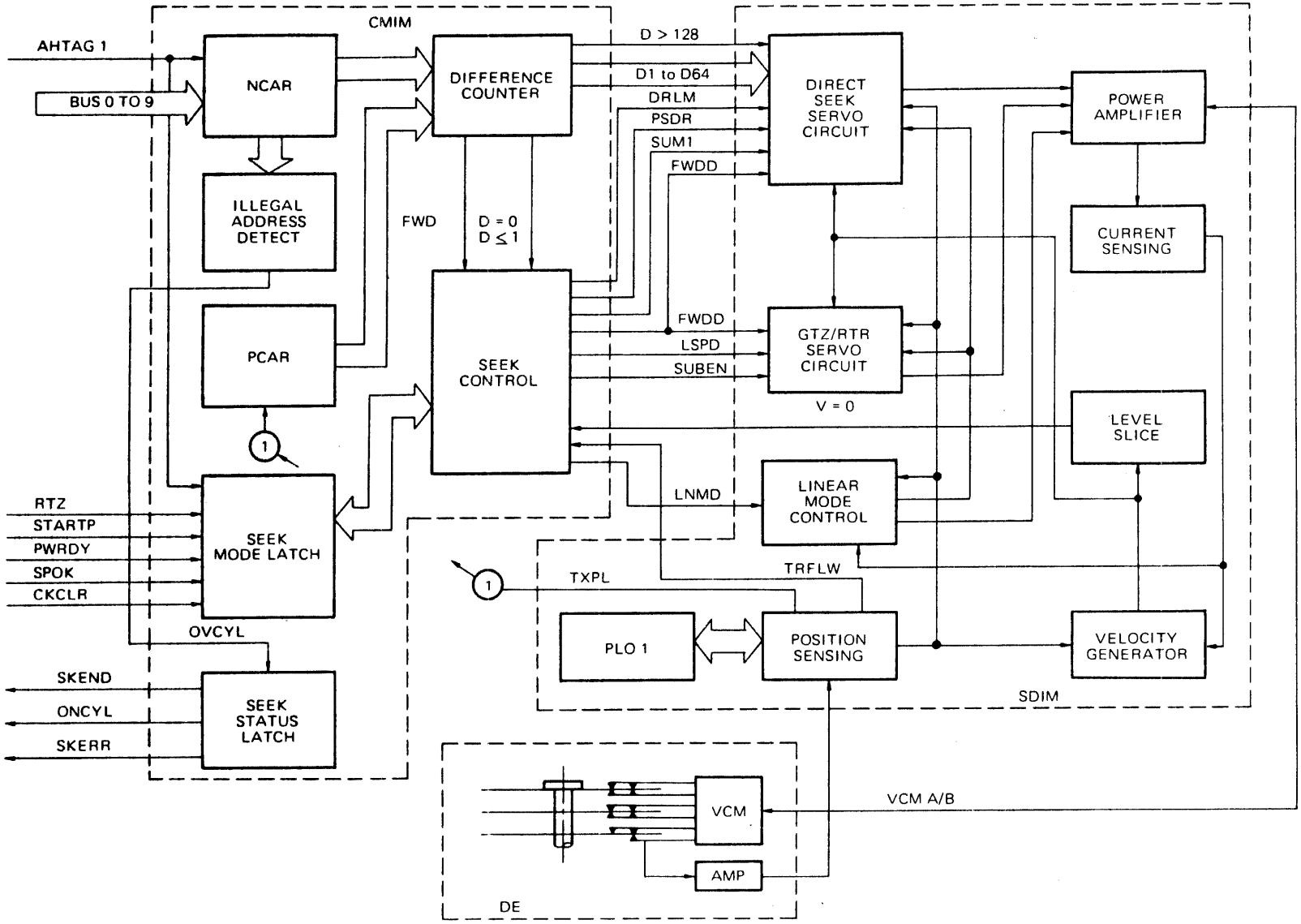


Figure 4-6-9 Seek Control Block Diagram

4.6.3.1 Initial Seek Mode

As mentioned in the Start/Stop Function section, the speed OK (SPOK) signal goes true when the rotational speed is up to 80%. The leading edge of the SPOK signal sets the Retract Mode (RTRM), Sub Enable (SUBEN) and Drive Linear Motor (DRLM) signals to keep the heads on the landing zone (IGB2). Five seconds after SPOK, the Guard Band Enable (GBENB) signal goes true to enable decoding of Index and all guard band signals. Ten seconds after SPOK, the Start Pulse (STARTP) goes true; the Retract and Velocity Equals Zero (V=0) latches are reset; and the Initial Seek Mode (INSKM), Go To Zero (GTZ), Under Sequence (UNSQ), DRLM, SUBEN, Forward Drive (FWDD) and Even latches are all set.

At the starting of Initial Seek, the heads move toward the outside of the disk (forward) at high speed by enabling FWDD and disabling Low Speed (LSPD).

When the heads have passed through the IGB2 zone and enter the IGB1 zone, the heads are driven toward the outside of the disk at low speed by enabling the FWDD and LSPD signals.

When the heads have passed through IGB1 zone, the Position Drive (PSDR) goes true when three successive Odd tracks are encountered, which changes the target velocity to the Position signal. When the velocity reaches the capture range, V=0 signal goes true, and then it resets the DRLM and SUBEN latches and sets the Linear Mode (LNMD) latch. When the LNMD signal goes true it keeps the heads precisely on the center of Cylinder 0, that is, the first ODD-EVEN servo track.

The first Index signal under the linear mode triggers the Settling 1 one-shot (STL1:2.5ms). The trailing edge of the STL1 signal sets the Seek End (SKEND), On Cylinder (ONCYL) and Unit Ready (URDY) latches, and also resets the INSKM, GTZM and UNSQ latches.

If the inital seek has not been performed within 640ms after STARTP, the Device Check goes true under the not ready status. The Device Check Clear signal, under the not ready status, which is commanded from the control unit or the Check Clear key, will cause a retry of the Initial Seek sequence.

The Return To Zero (RTZ) command under the Retract Mode during Ready status initiates the Initial Seek sequence.

The flow chart at Go To Zero is shown in Figure 4-6-10, and the timing chart for Initial Seek is shown in Figure 4-6-11.

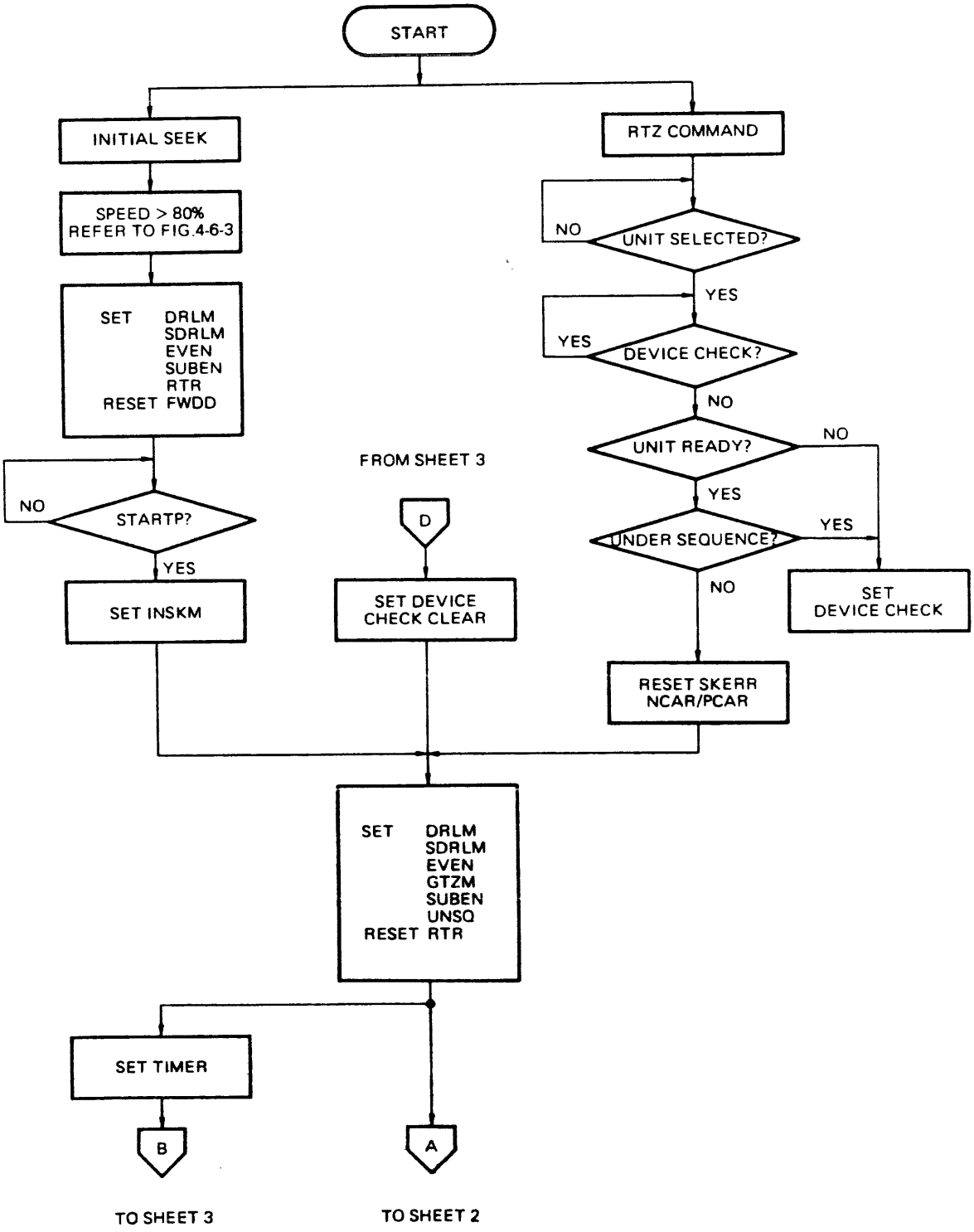
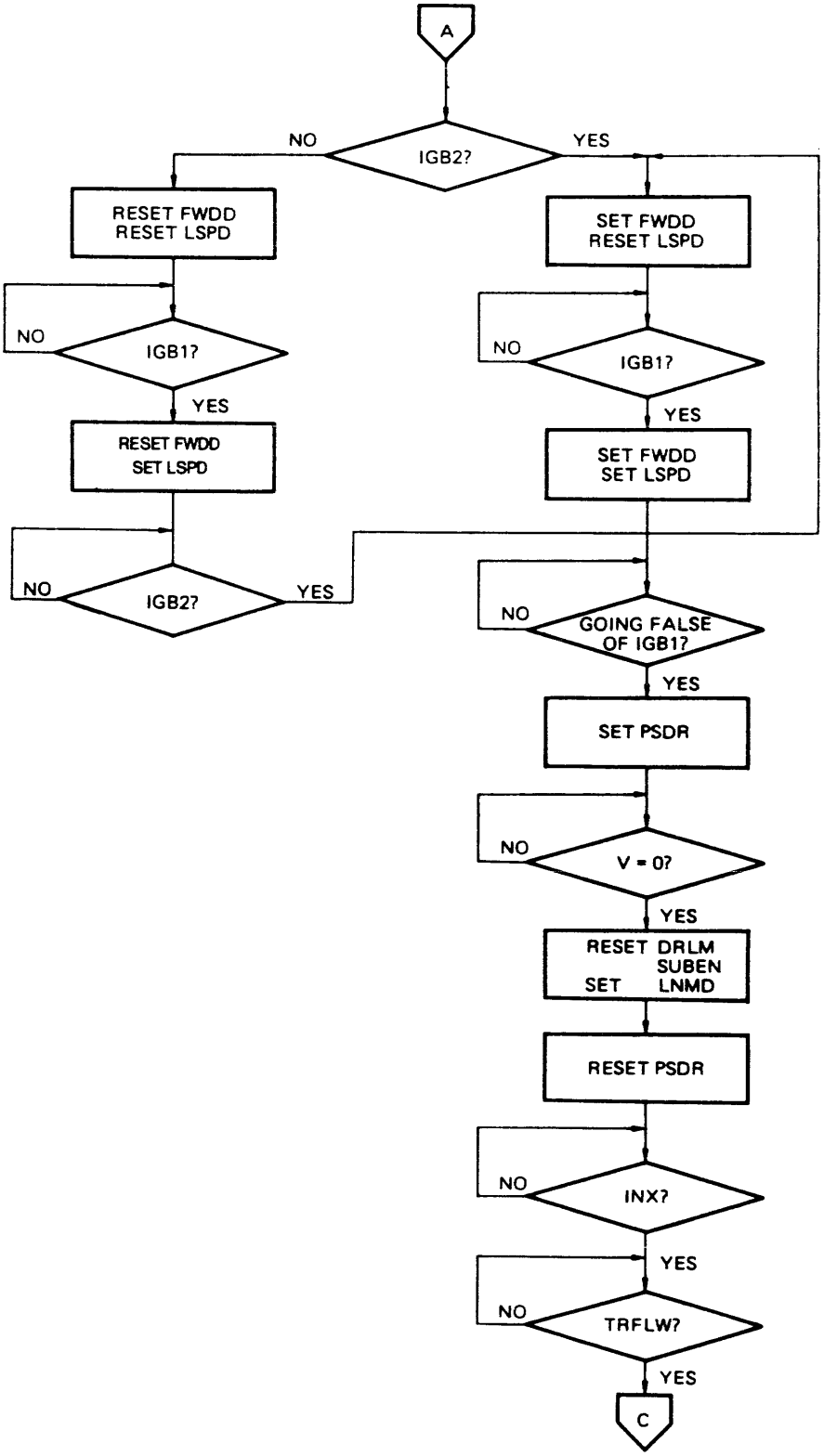


Figure 4-6-10 Go To Zero Flow Chart (Sheet 1 of 3)

From Sheet 2



To Sheet 3

Figure 4-6-10 Go To Zero Flow Chart (Sheet 2 of 3)

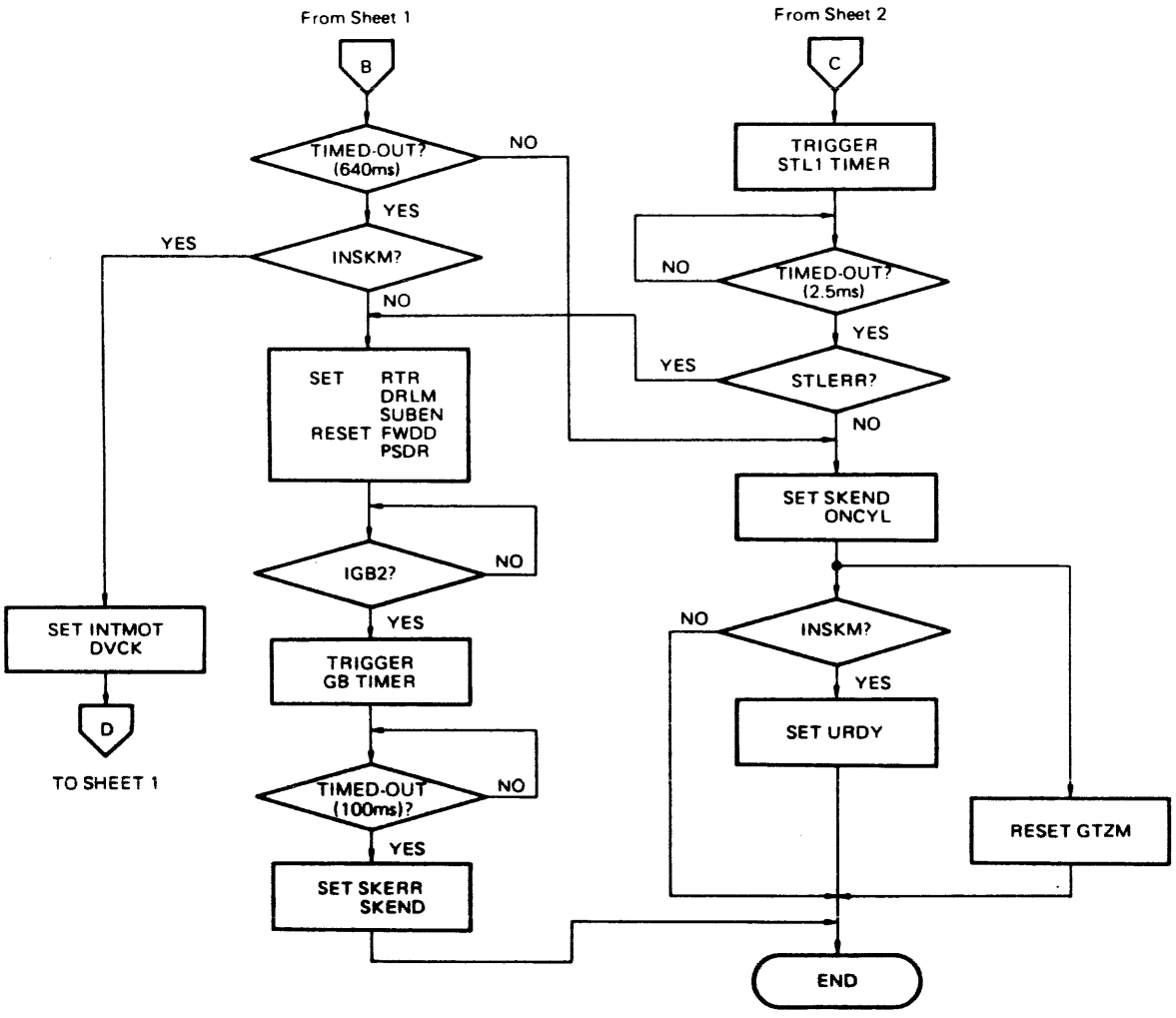


Figure 4-6-10 Go To Zero Flow Chart (Sheet 3 of 3)

Figure 4-6-11 Initial Seek Timing Chart

4.6.3.2 Return to Zero Mode

The Return To Zero Mode is initiated by the Return to Zero (RTZ) command from the control unit during Ready status and linear mode.

The RTZ command sets the GTZM, DRLM and EVEN latches and resets the V=0, LNMD and Seek End (SKEND) latches.

At the start of GTZM, the heads move toward the center of the disk (reverse) at high speed by disabling the FWDD and LSPD signals.

When the heads have passed through the Servo Zone and enter the IGB1 zone, the heads are driven toward the center of the disk at low speed.

When the heads enter the IGB2 zone, they are driven toward the perimeter (forward) at high speed. When the heads enter the IGB1 zone again, they are driven forward at low speed.

The subsequent sequence is equivalent to the Initial Seek Mode.

The RTZ timing chart is shown in Figure 4-6-12.

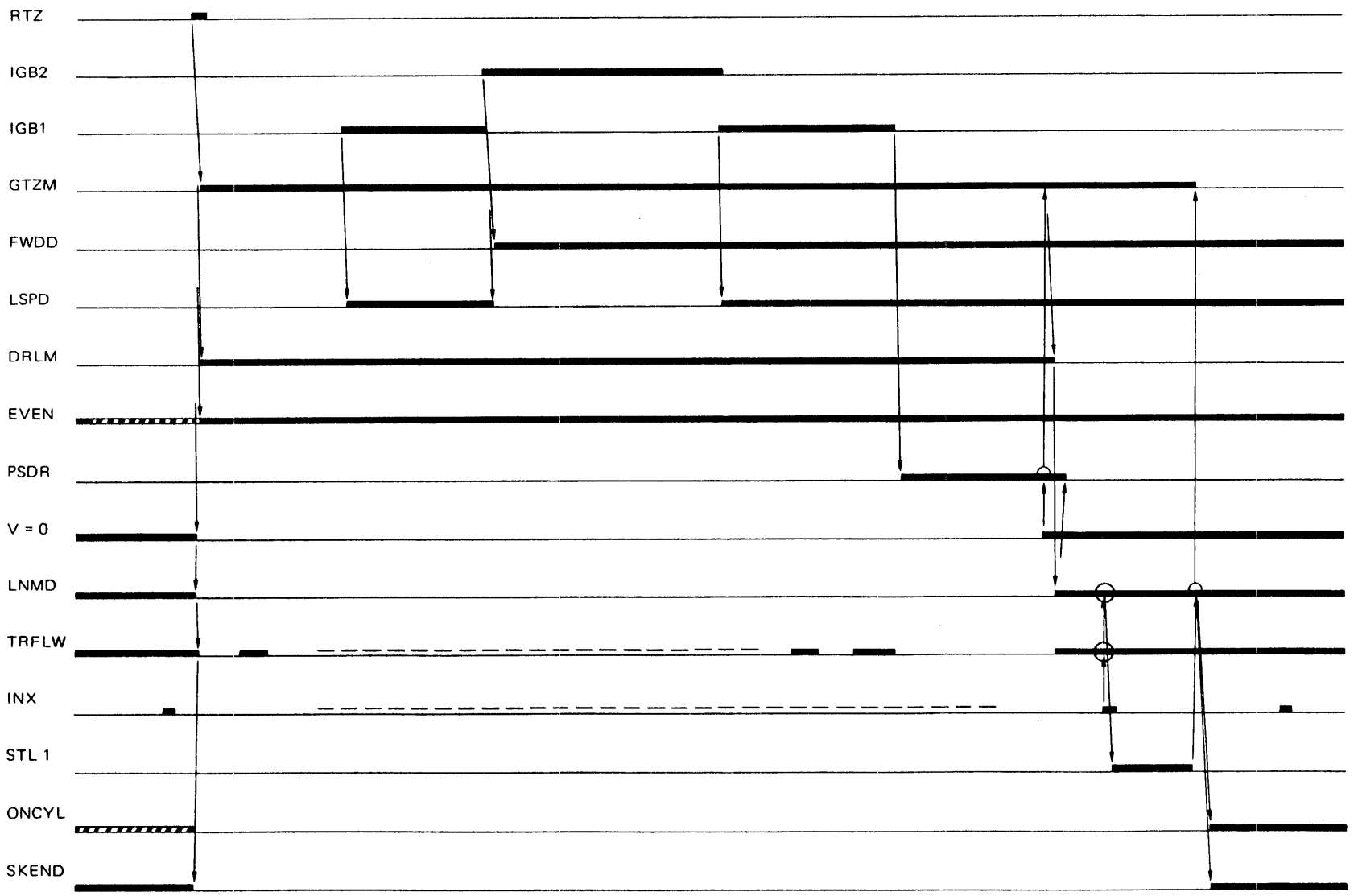


Figure 4-6-12 Return to Zero Timing Chart

4.6.3.3 Direct Seek Mode

Direct Seek is initiated by activating the Tag 1 signal.

The leading edge of Tag 1 sets the bus bits 0 to 9 into the Next Cylinder Address Register (NCAR) when the bus contents are less than 822.

When the NCAR output is not equal to the Present Cylinder Address Register (PCAR) output at the trailing edge of Tag 1 signal (Fall Tag 1: FTAG1), a Direct Seek is initiated.

The FTGA1 signal resets the ONCYL, SKEND, LNMD and V=0 latches, and also sets the SEKM, DRLM, UNSQ, and direction lathces.

Even latch is set if NCAR contains an even number cylinder address.

The diferrence between NCAR and PCAR is equal to the number of cylinders to move to the desired address. The difference counter outputs binary coded D1 to D64 and D > 128 is sent to the servo control circuit to generate the target velocity.

When the NCAR is greater than PCAR, the forward direction is set, and when the NCAR is less than the PCAR, the reverse direction is set using the FWDD signal.

When the heads start to move to the desired address, the Track Crossing Pulse (TXPL) is sent from the servo circuit to the PCAR counter every time the servo head crosses a cylinder. The PCAR counter is increased by the trailing edge of the TXPL signal in the forward direction, and is decreased in the reverse direction.

When the difference is equal to or less than one, D $\leqslant$ 1 signal goes true, and Track Follow (TRFLW) goes false, the Position Drive (PSDR) signal is activated and the velocity follows the position signal. When the difference counter output is equal to zero and V = 0 signal goes true, Linear Mode (LNMD) is set, DRLM and PADR signals are reset, and then the Setting 1 (STL1) one-shot is triggered. The trailing edge of STL1 sets the ONCYL and SKEND latches and resets the SEKM and UNSQ latches.

If an illegal cylinder address (822 < CYL < 896) is set in the NCAR, no head movement is performed; however, ONCYL and SKEND latches are reset by the trailing edge of Tag 1 and the Seek Error (SKERR) and SKEND latches are set after 5μs.

The Direct Seek flow chart is shown in Figure 4-6-13 and the timing chart is shown in Figure 4-6-14.

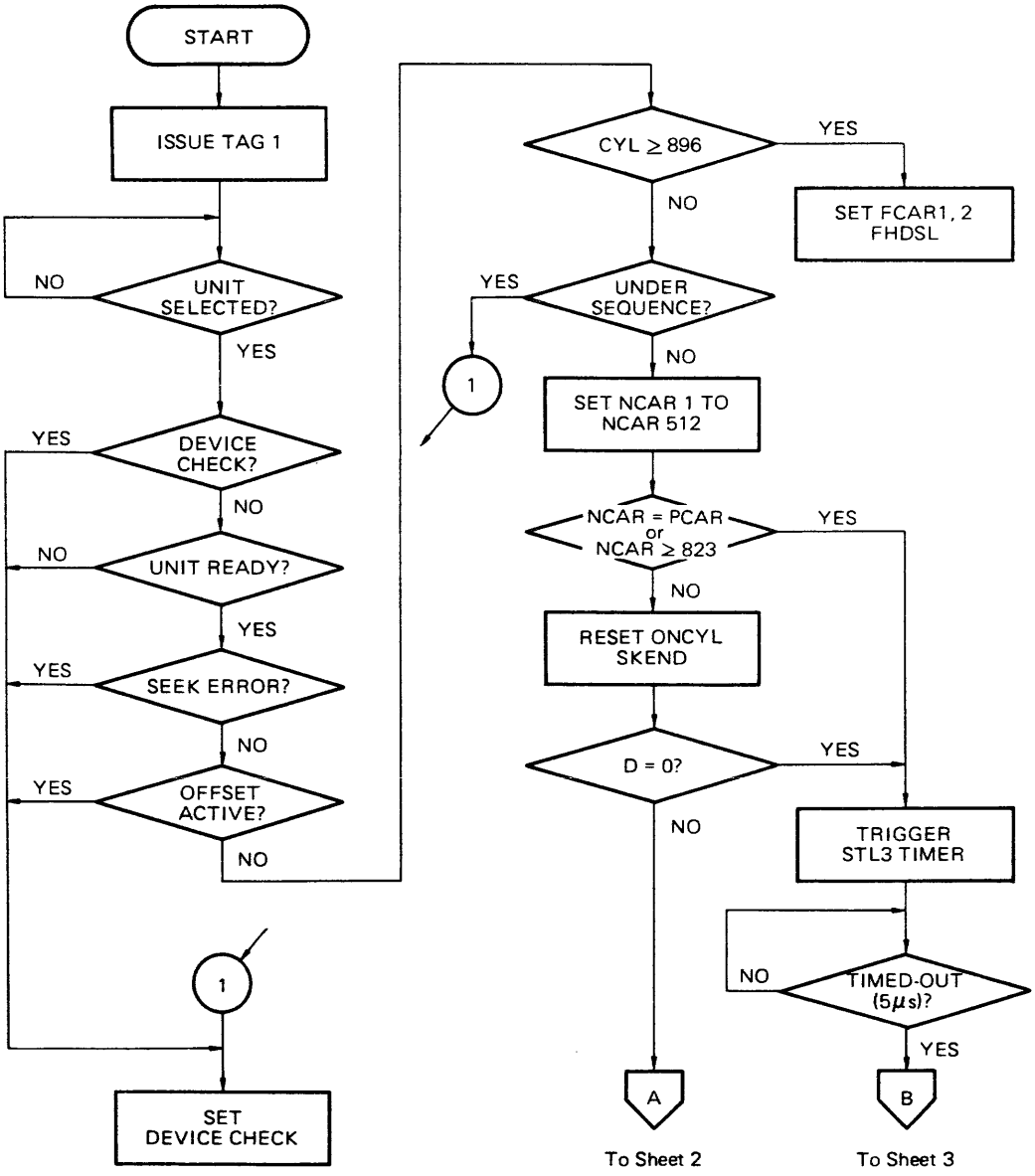


Figure 4-6-13 Direct Seek Flow Chart (Sheet 1 of 3)

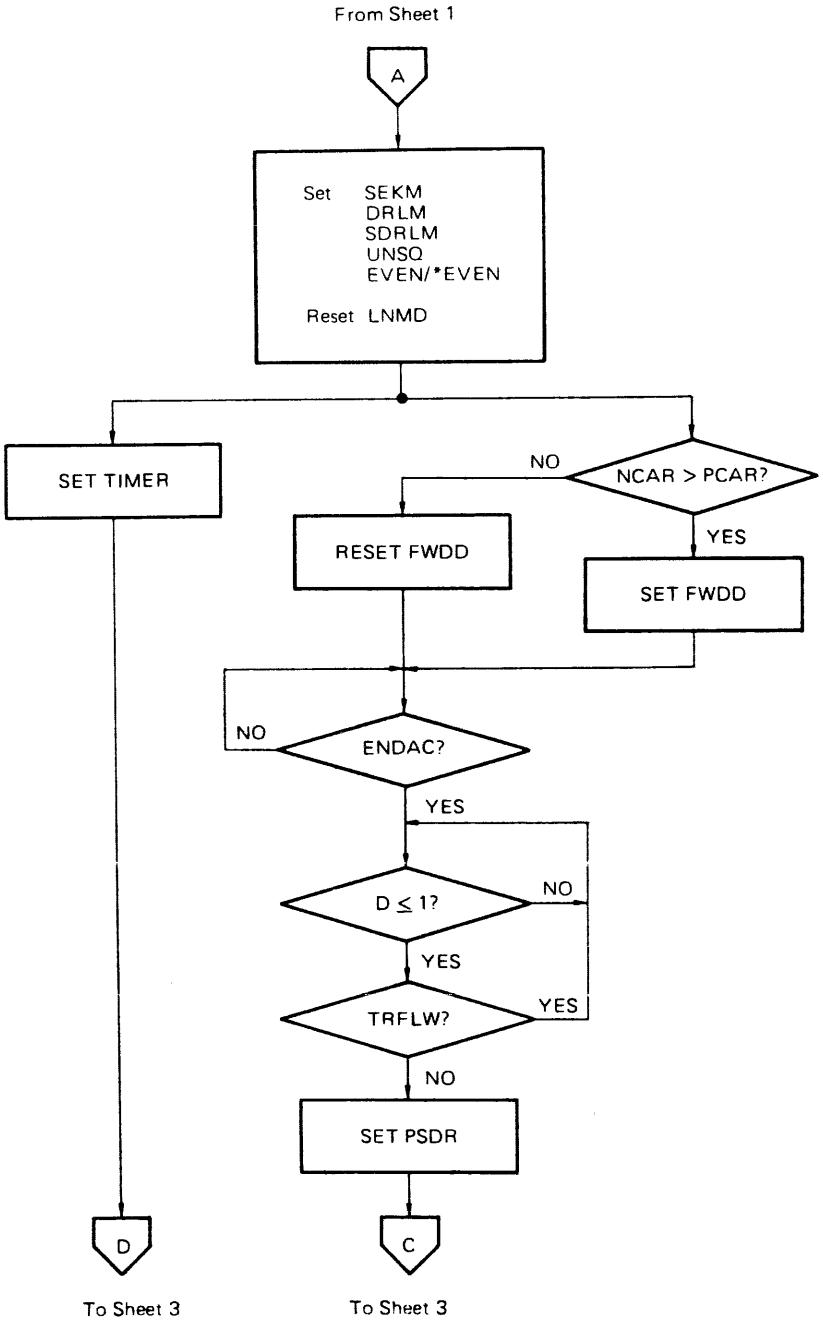


Figure 4-6-13 Direct Seek Flow Chart (Sheet 2 of 3)

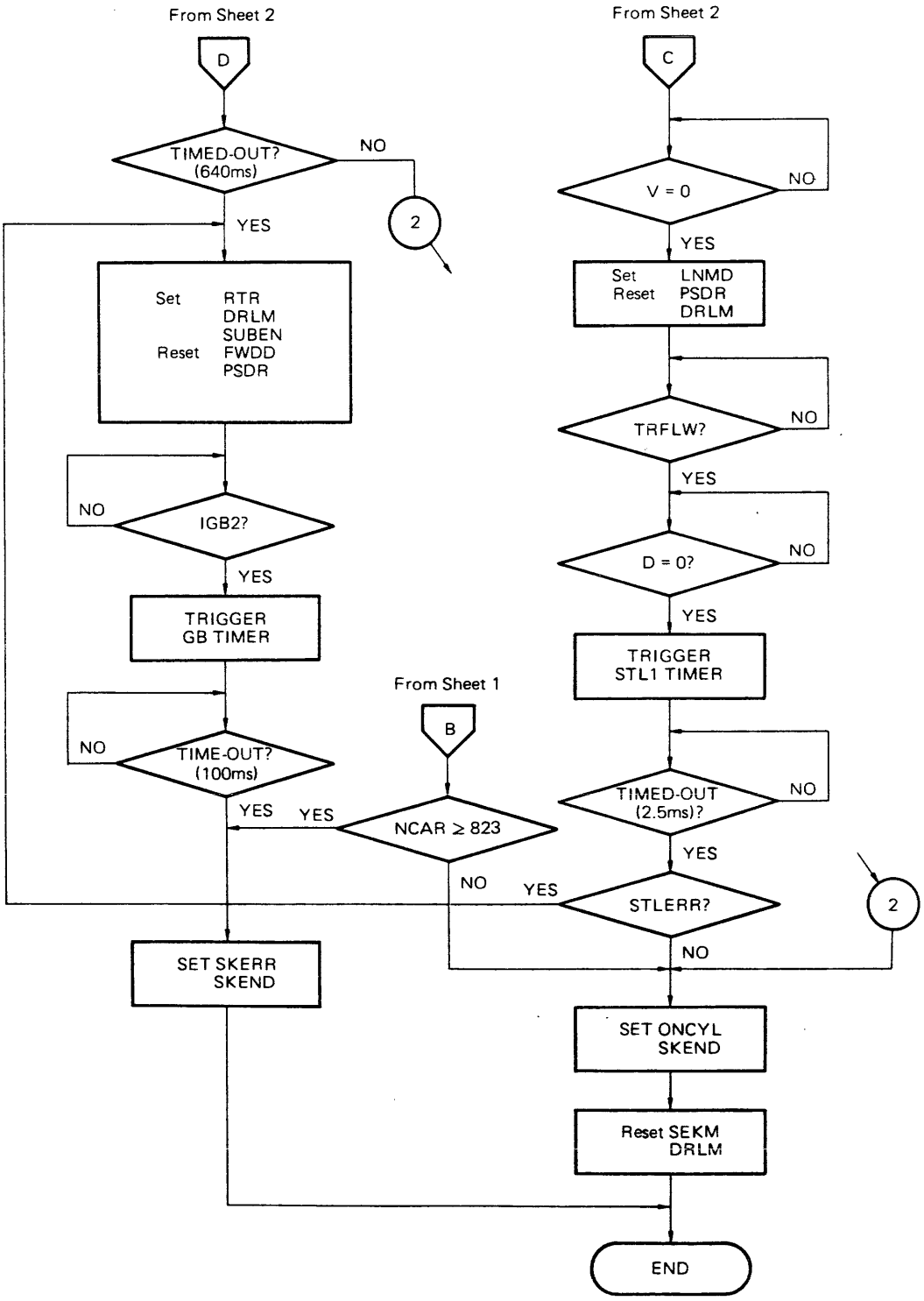


Figure 4-6-13 Direct Seek Flow Chart (Sheet 3 of 3)

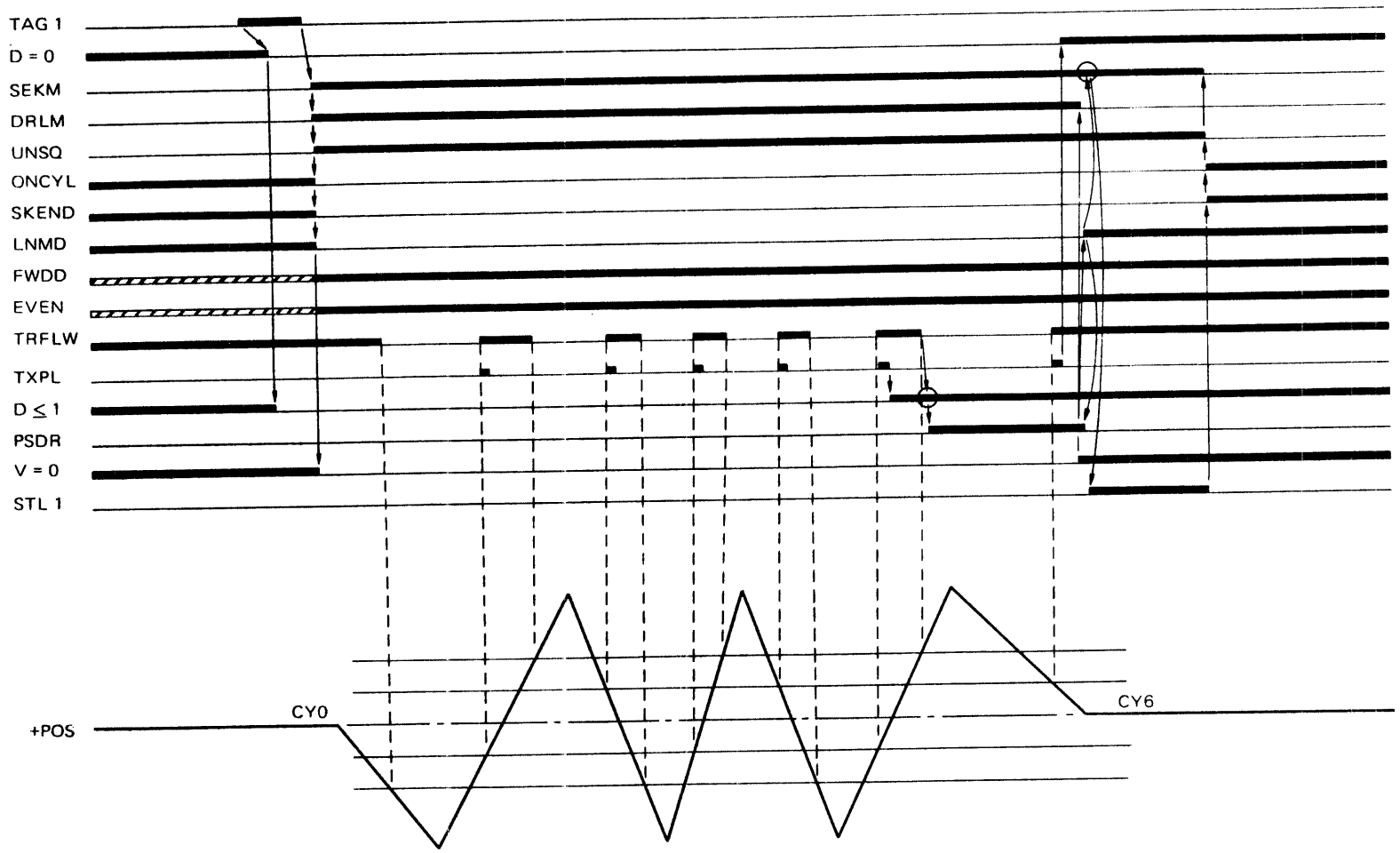


Figure 4-6-14 Direct Seek Timing Chart

4.6.3.4 Retract Mode

If the following malfunctions have occurred in the unit, Retract Mode (RTRM) is set and the heads move to the landing zone (IGB2).

ERROR	UNIT STATUS
Initial Seek Time Out	(Not Ready)
Rotational Speed Low	(To Not Ready)
DC ± 12V Fault	(To Not Ready)
Any GB in Seek Mode	(To Seek Error)
Any GB in Linear Mode	(To Seek Error)
OGB in Go To Zero Mode	(To Seek Error)
Time Out in Any Seek Mode	(To Seek Error)
Settling Error in Linear Mode	(To Seek Error)

Each malfunction sets the RTRM, DRLM and SUBEN latches and then resets the FWDD latch. The heads move in reverse at retract speed defined by the servo circuit. When IGB2 goes true under RTRM, it triggers the Guard Band Timer (GBTM) one-shot. The trailing edge at GBTM sets Seek Error (SKERR) and Seek End (SKEND).

4.6.4 Servo Circuit Function

4.6.4.1 Position Sensing

The block diagram of the position sensing circuit is shown in Figure 4-6-15 and the waveforms are shown in Figure 4-6-16 to Figure 4-6-19.

The servo data written on the servo surface is read by the servo head and amplified by the Head Pre-amplifier with a gain of 70, and applied to the Automatic Gain Control (AGC) amplifier. The AGC amplifier functions to keep the output constant if the AGC input varies. The AGC output is applied to a Low Pass Filter (LPF), which attenuates unuseful high frequencies, and then is amplified by the Carrier Amplifier, which outputs the servo (SERVO) signal.

The SERVO signal is applied to the Level Slicer and Sampling Gate circuits. The Level Slicer slices the Servo signal and separates the Sync Bit. This output is called Servo Pulse (SVPL) and is then applied to the Phase Locked Oscillator I (PLO I) circuit.

The Servo Pulse interval is 32 bits (4 Bytes). The PLOI circuit syncronizes with the Servo Pulse and generates 2 Bits Clock. The PLO output is applied to the counter, and decoded to generate a Sampling Gate. The Sampling Gate, that is Odd Gate (ODG) and Even Gate (EVG), samples odd position pulses and even position pulses respectively and holds the position pulse peaks in the Peak Hold circuit.

The Peak Hold outputs, Odd Peak (ODP) and Even Peak (EVP), are applied to an Adder Amplifier which outputs AGC control voltage. Moreover, the Peak Hold outputs are applied to a Differential Amplifier to generate a Position (POS) signal.

The Position signal is proportional to the distance of the servo head from the centerline of the servo tracks and this is 0V at the centerline of the tracks.

The Position signal (± POS) is applied to the Level Detector circuit to generate Track Follow (TRFL) and Track Crossing Pulse (TXPL) signals which are sent to the seek control circuit. Velocity Invert (VINV) and Velocity Non-Invert (VNON) signals are also produced which generate a portion of the velocity signal.

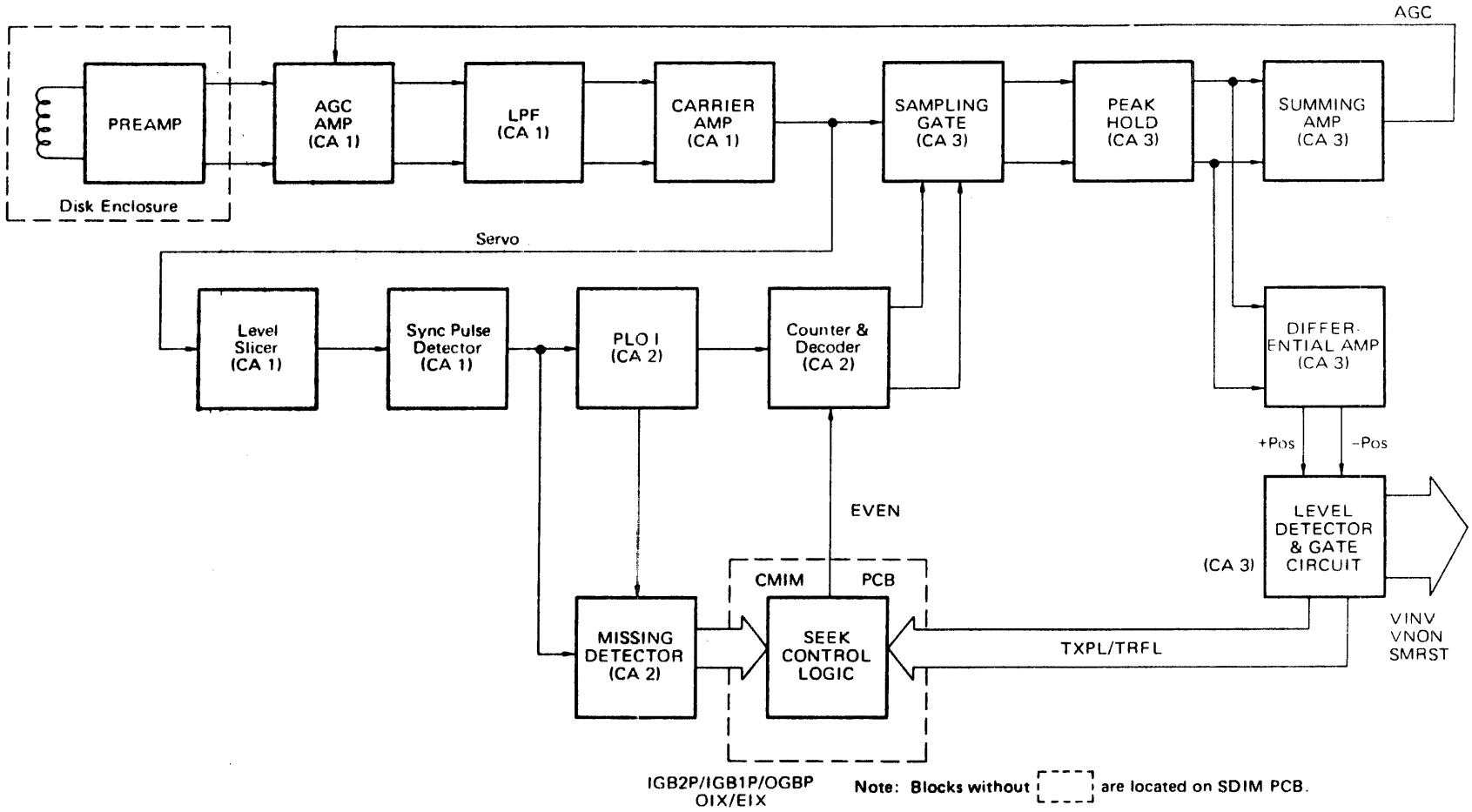
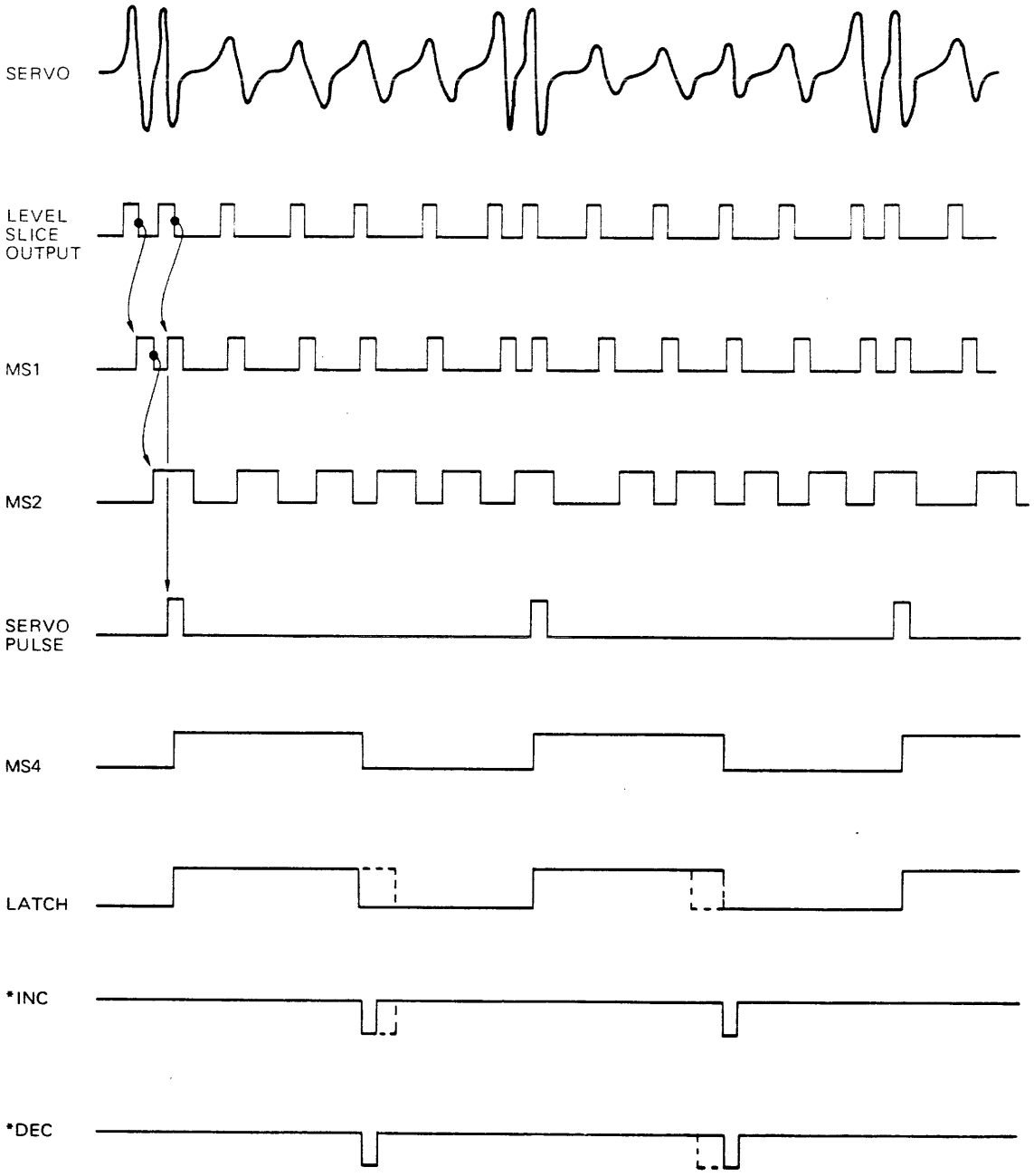


Figure 4-6-15 Position Sensing Block Diagram



Note: The above waveform is for On-Track condition.

Figure 4-6-16 Position Sensing Waveform (1)

Note: The above waveform is for On-Track condition, and EVEN is true.

Figure 4-6-17 Position Sensing Waveform (2)

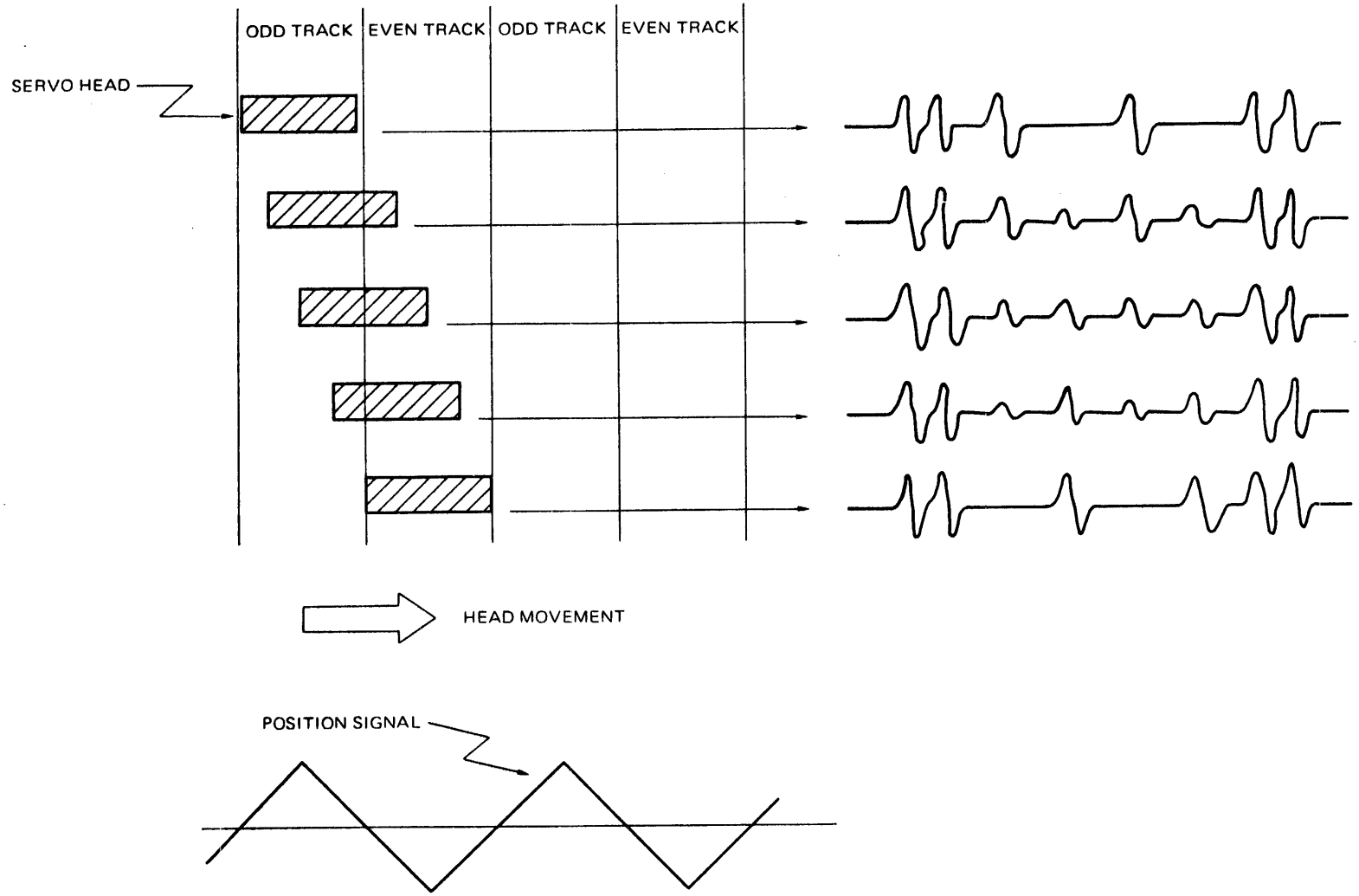


Figure 4-6-18 Position Sensing Waveform (3)

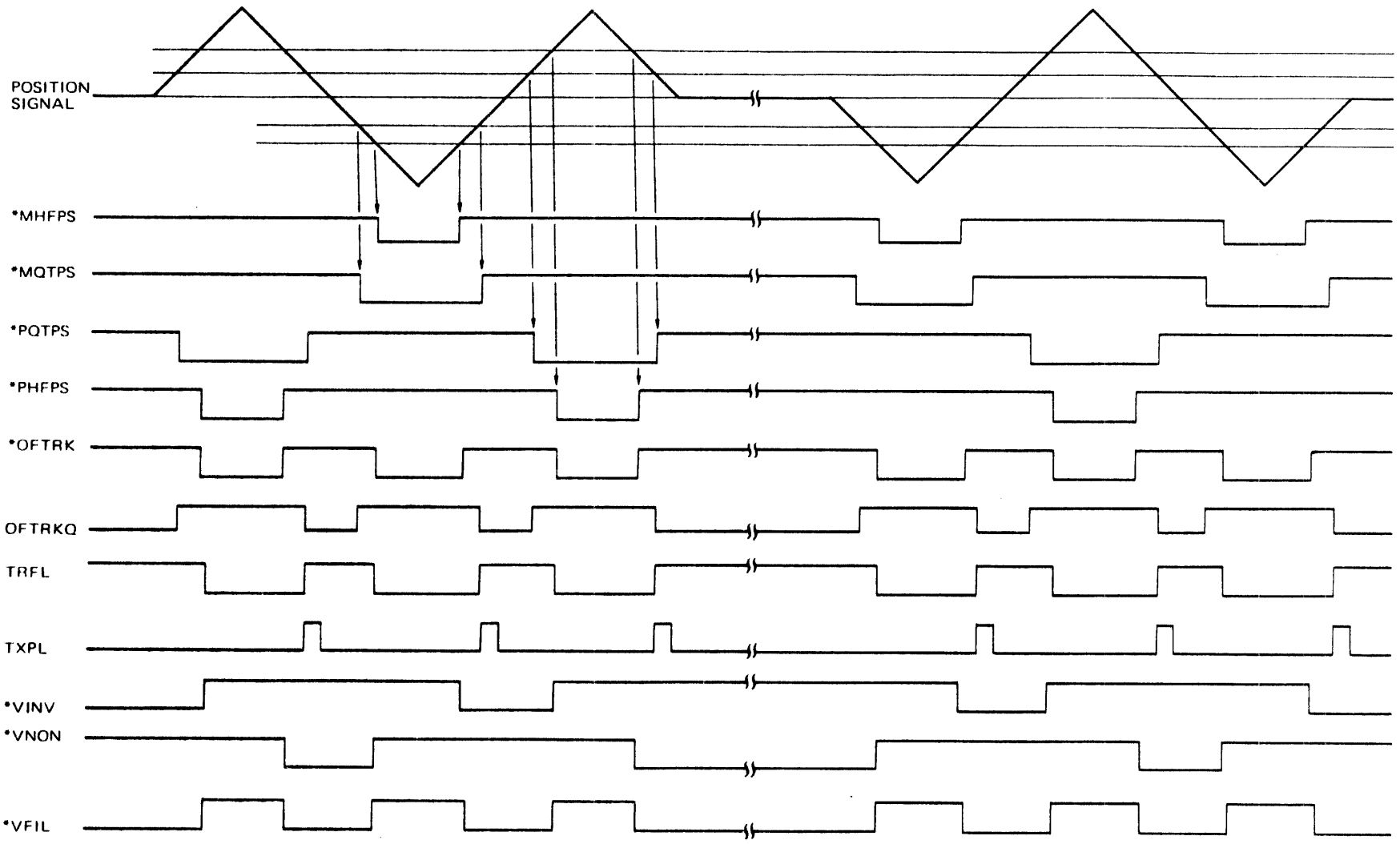


Figure 4-6-19 Position Sensing Waveform (4)

4.6.4.2 Direct Seek Control Circuit

The Direct Seek Control block diagram is shown in Figure 4-6-20 and the waveform is shown in Figure 4-6-21.

When the cylinder address is specified from the control unit, the Difference Counter outputs the difference between the Next Cylinder Address Register (NCAR) and the Present Cylinder Address Register (PCAR) in binary-code.

The Difference Counter seven-bit output D1 to D64 is applied to the DA Converter (DAC) which generates a voltage in proportion to the difference. If the Difference Counter has a value of 127 or above, the DAC output is maximum.

As the head crosses a track, the Track Crossing Pulse is detected and then the Difference Counter decrements by one.

The decrementing output of the DAC is a staircase waveform. To smooth this staircase waveform of the DAC, the Smoother signal is applied to the DAC output.

The Smoother signal is a sawtooth waveform which is generated by integrating the velocity waveform at each track crossing.

The Function Generator outputs a target velocity curve (Function Curve: FUNC), which is designed to keep positioning time to a minimum.

The Velocity Generator circuit generates a Velocity (VEL) signal in proportion to the velocity of head movement. The Velocity signal is comprised of the position signal slope and the VCM coil current sense (CS).

The difference (summing amplifier output) between the Velocity signal and Function Curve develops the Velocity Error (VER) signal. The Velocity Error signal is applied to the VCM driver circuit to move the heads to the specified track.

The servo control circuit always tries to decrease the Velocity Error.

As the heads approach the specified cylinder, the head movement is decelerated.

When the difference is equal to or less than one and the Track Follow (TRFL) latch goes false, the Target Velocity is changed to the Position signal by enableing Position Drive (PSDR) signal.

When the Velocity signal becomes very small compared to the slicing level and the Velocity-Equal-Zero (V=0) signal goes true, the seek mode is changed to Linear Mode control (Fine-servo) after 1ms.

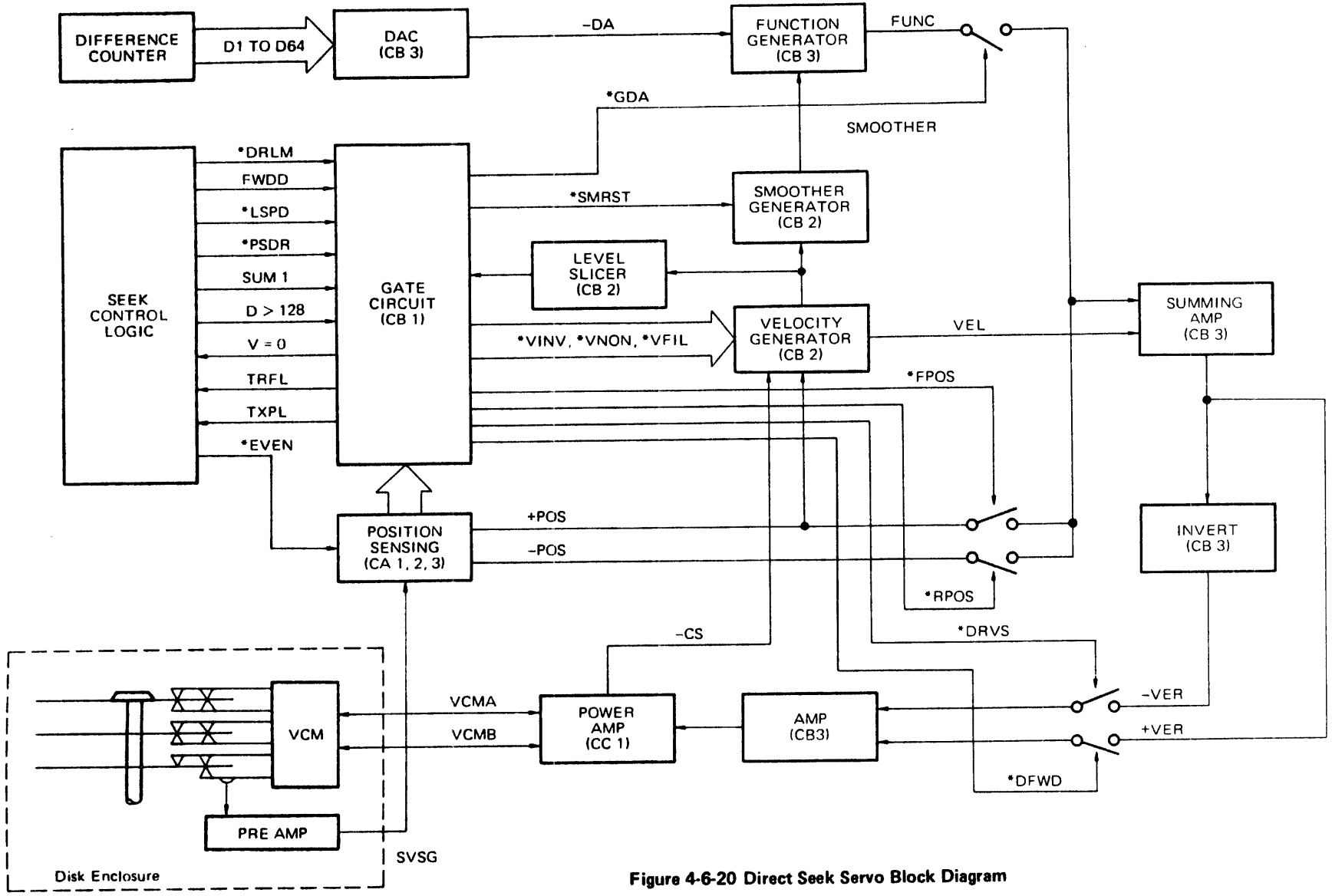


Figure 4-6-20 Direct Seek Servo Block Diagram

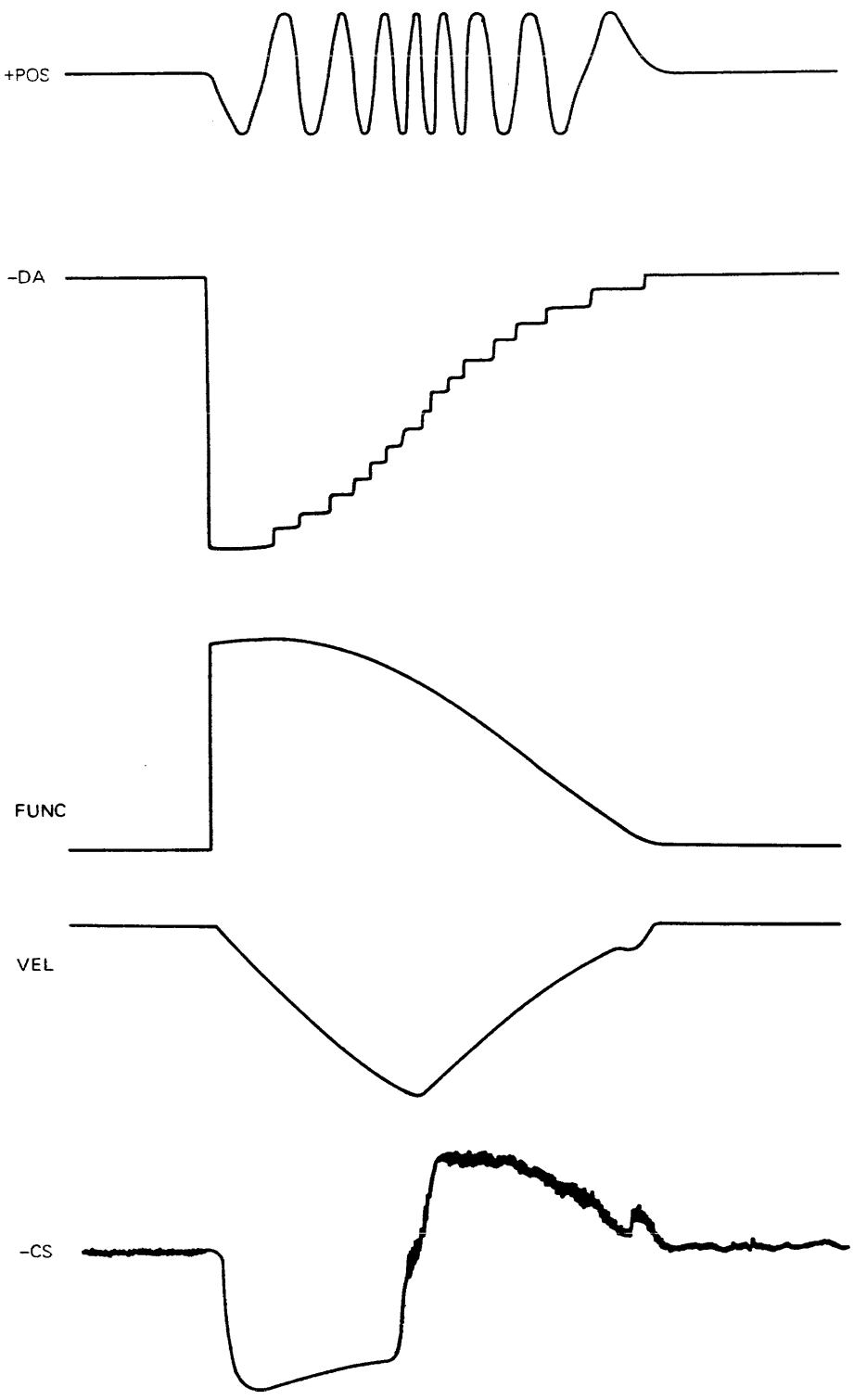


Figure 4-6-21 Direct Seek Servo Waveform

4.6.4.3 Initial Seek/Return To Zero Servo Control

The Initial Seek/Return To Zero block diagram is shown in Figure 4-6-22 Initial Seek waveform in Figure 4-6-23 and Return to Zero waveform in Figure 4-6-24.

Initial Seek/Return to Zero servo control is initiated by enabling Sub-Enable (SUBEN). The direction is specified by the Forward Drive (FWDD) signal and its reference velocity is specified by the Low Speed (LSPD) signal.

To generate an Initial Seek operation, the Start Pulse (STARTP) signal sets the Forward/High Speed (FWDD: true, LSPD: false) signal and the head begins to move up to speed from the Landing Zone (IGB2). When the head enters the Inner Guard Band 1 (IGB1), the speed is changed to Low Speed (LSPD: true). When the head passes through the IGB1, Position Drive (PSDR) goes true and the head movement follows the Position signal by changing the reference velocity to Position signal.

When the head arrives at cylinder 0, the Velocity-Equal-Zero (V=0) signal goes true. The Linear Mode is developed when V=0 signal goes true and the Initial Seek is terminated.

Return To Zero (RTZ) mode is initiated by an RTZ command from the control unit. If the RTZ command is received when the head is located on IGB2, the sequence is the same as the above-mentioned Initial Seek operation. When the head is located in the Servo Zone, the RTZ command sets Reverse/High Speed (FWDD: false, LSPD: false).

The heads move toward the spindle and enter the IGB1 area. When IGB1 is detected, Reverse Low Speed (FWDD: false, LSPD: true) is set. When the heads reach IGB2, the head movement is set to Forward/High Speed (FWDD: true, LSPD: false) until IGB1 is detected again.

When the head movement direction is changed from reverse to forward, the current-feedback in the velocity generator circuit is inhibited for 1ms to prevent a false velocity error voltage. The subsequent control is the same as that of the above-mentioned initial Seek operation.

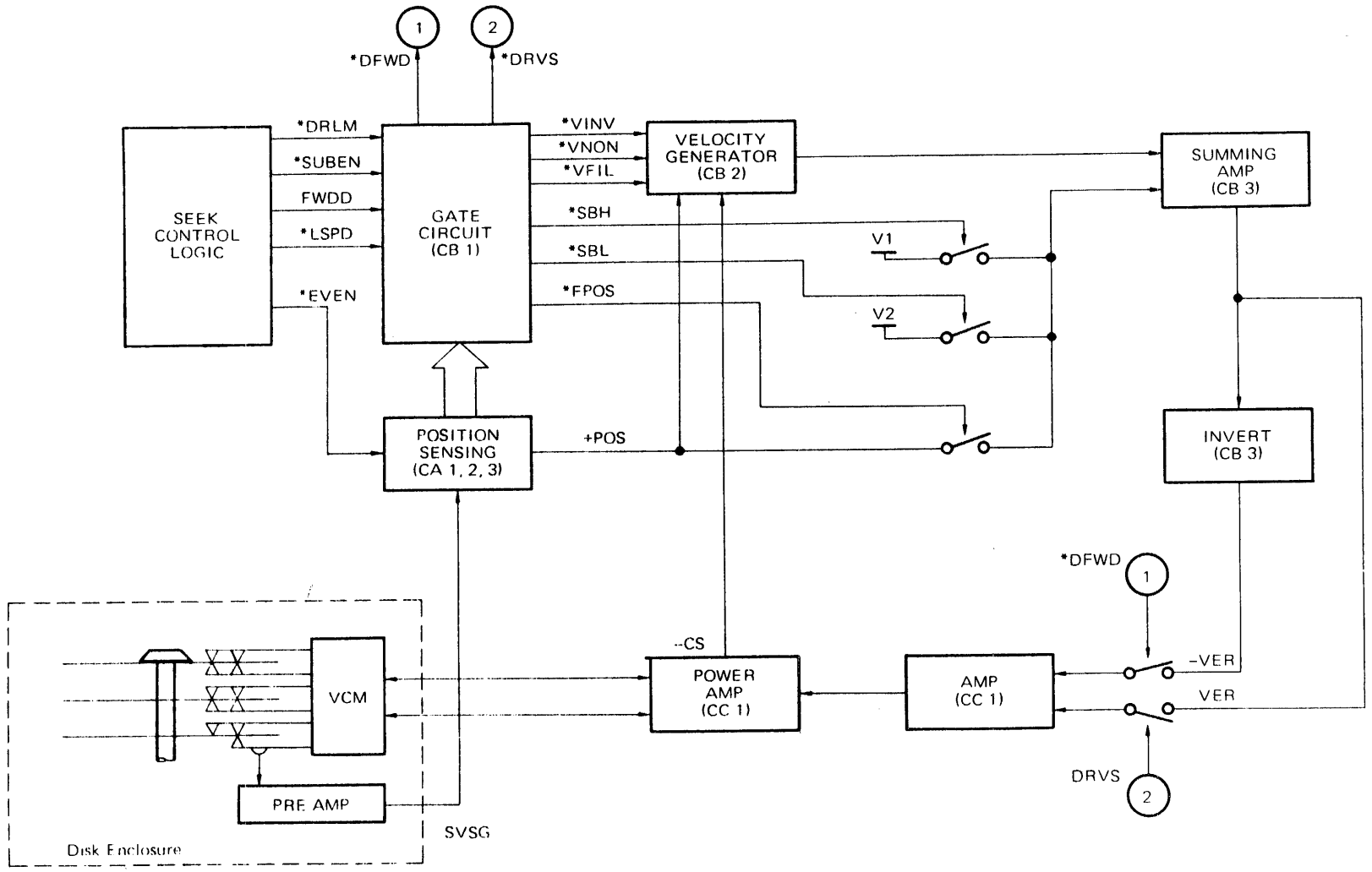


Figure 4-6-22 Initial Seek/RTZ Servo Block Diagram

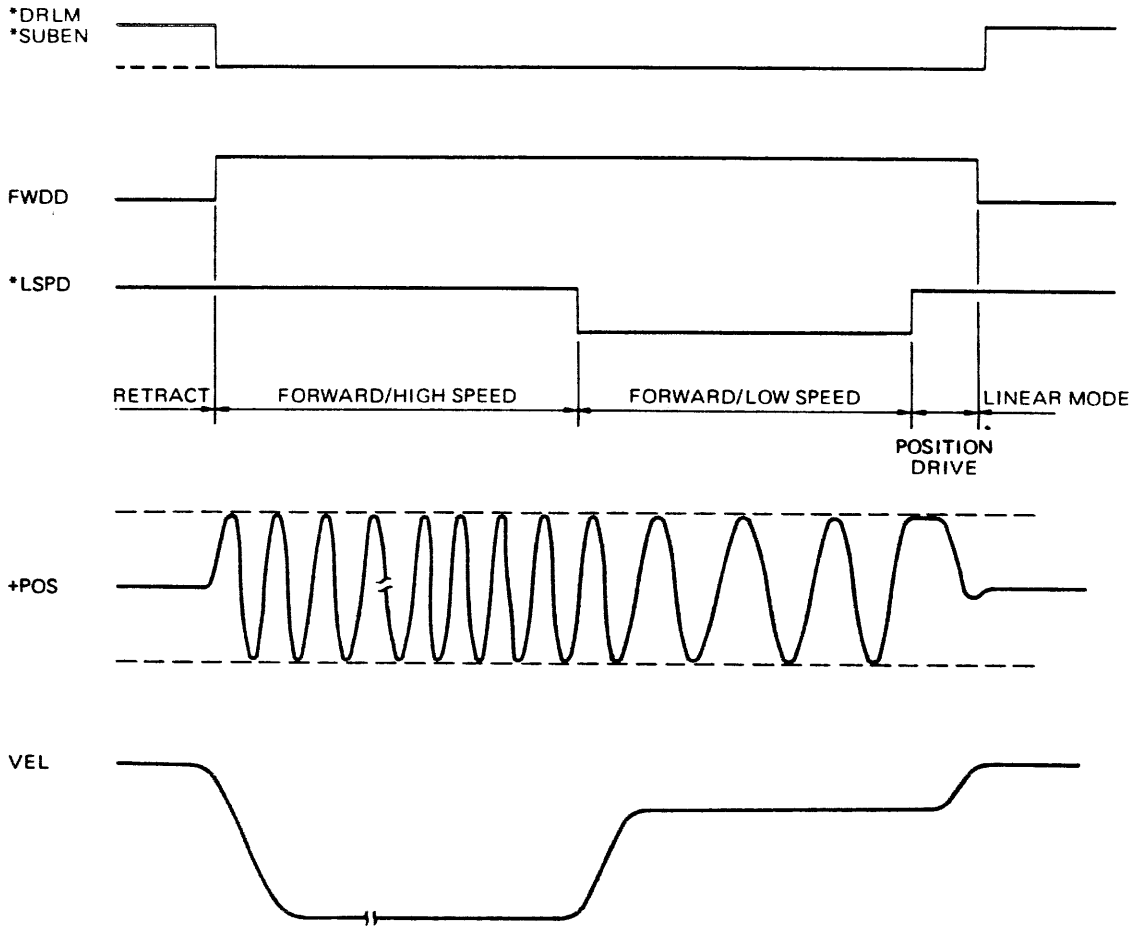


Figure 4-6-23 Initial Seek Servo Waveform

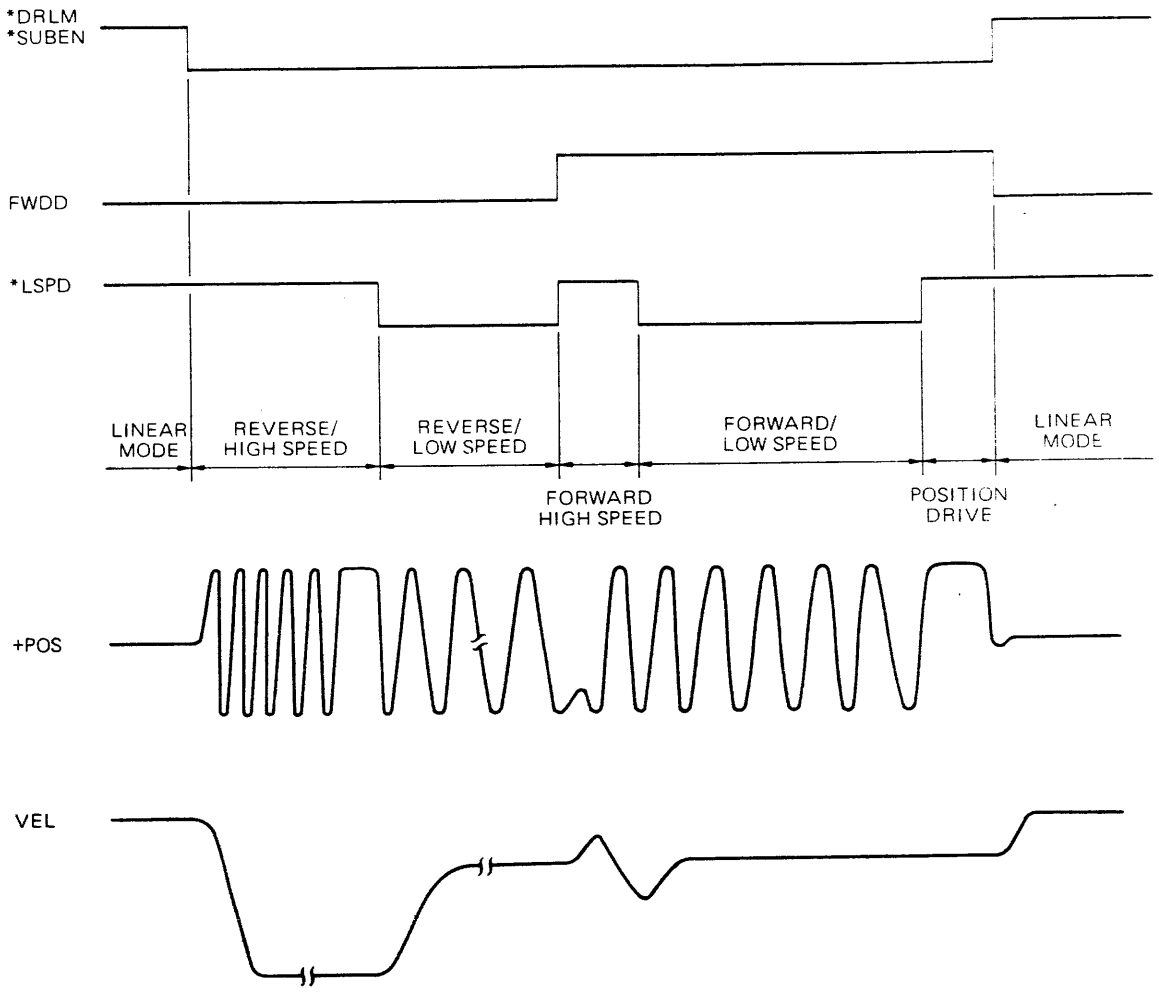


Figure 4-6-24 RTZ Servo Waveform

4.6.4.4 Linear Mode Servo Control

The Linear Mode servo block diagram is shown in Figure 4-6-25.

The Position (+POS) signal is 0V when the head is located on the center of the track. If the head is not on the center of the track, +POS signal develops voltage in proportion to the distance the head is off-center. Feedback of the off-center track value ensures that the head will remain located over the center of the track. This feedback signal is developed through the Low Pass Filer (LPF) to attenuate any unuseful high-frequencies and through the Phase Compensator circuit.

The Integrator output of VCM current sensing is used for the Phase Compensator, and it functions as a damping factor.

The offset function may be designated by the control unit to recover possible soft read errors. The Offset operation is initiated by the Offset Active (OFACT) signal from the seek control logic circuit. The value of offset is determined by the Difference signal to the DAC. The offset direction is set by the Forward Drive (FWDD) signal. During the offset operation the DAC output is applied to the summing amplifier with the position signal. Therefore, the head off-tracks by the reference voltage which is given by the DAC output.

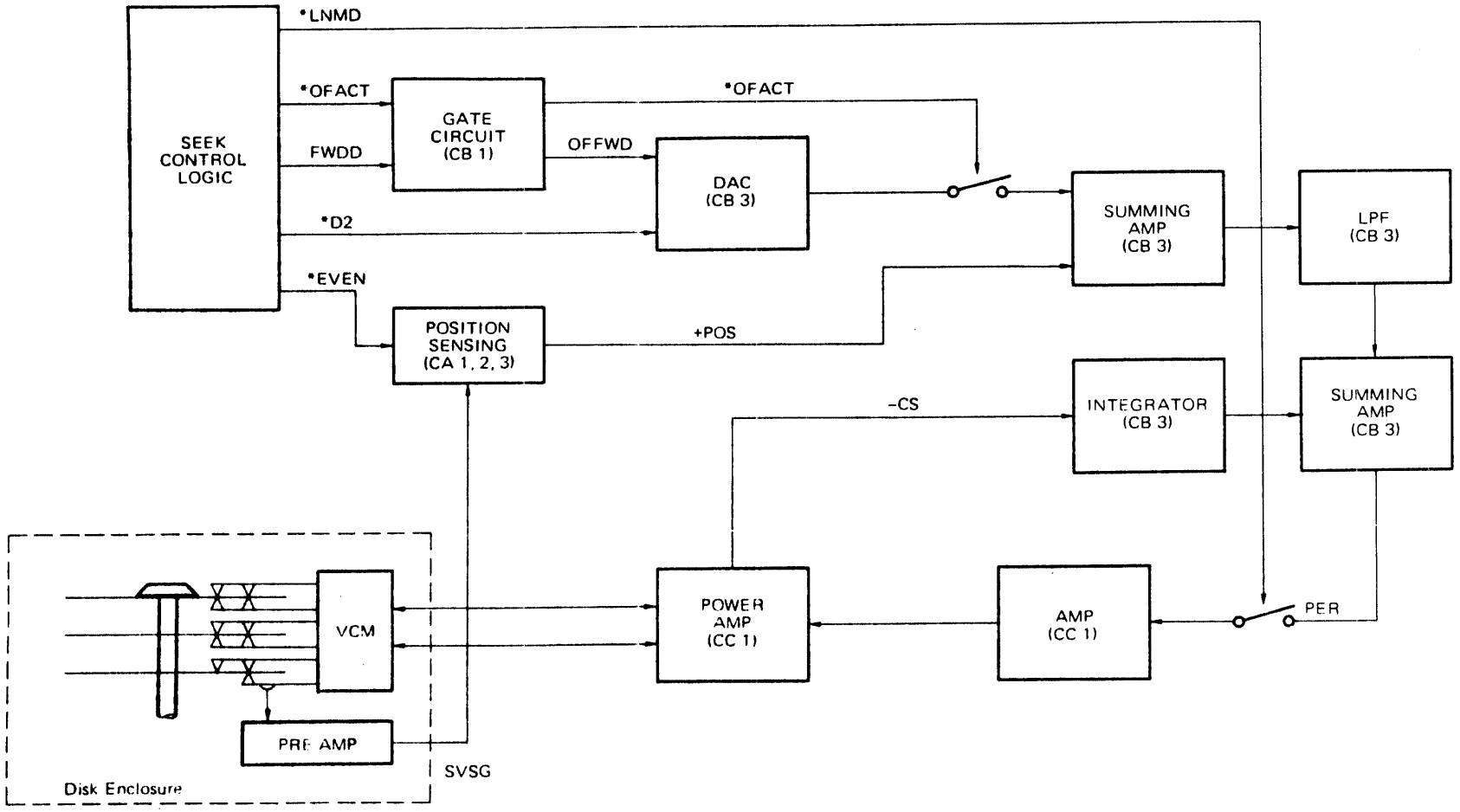


Figure 4-6-25 Linear Mode Servo Control Block Diagram

4.6.4.5 Retract Servo Control

The Retract servo control block diagram is shown in Figure 4-6-26.

The Retract operation is initiated if Retract (RTR) signal goes true, a power failure occurs, or if Emergency Retract (EMRT) signal goes true.

The Retract signal controls the head movement so that the velocity sensed from the voltage output of the VCM is equal to the reference velocity.

In the case of a DC power failure, the normally used power amplifier is deactivated and the retract capacitor discharges through the VCM coil.

If excessive current flows through the VCM coil, the VCM Heat (VCMHT) signal turns on.

When the VCMHT signal is turned on, the seek control logic issues the Emergency Retract (EMRT) signal, which breaks a relay contact supplying DC+24V to the power amplifier. After breaking the relay contact, the retract capacitor discharges through the VCM coil.

Under above-mentioned conditions, the heads always return to the landing zone (IGB2) and are held there by the stopper magnet.

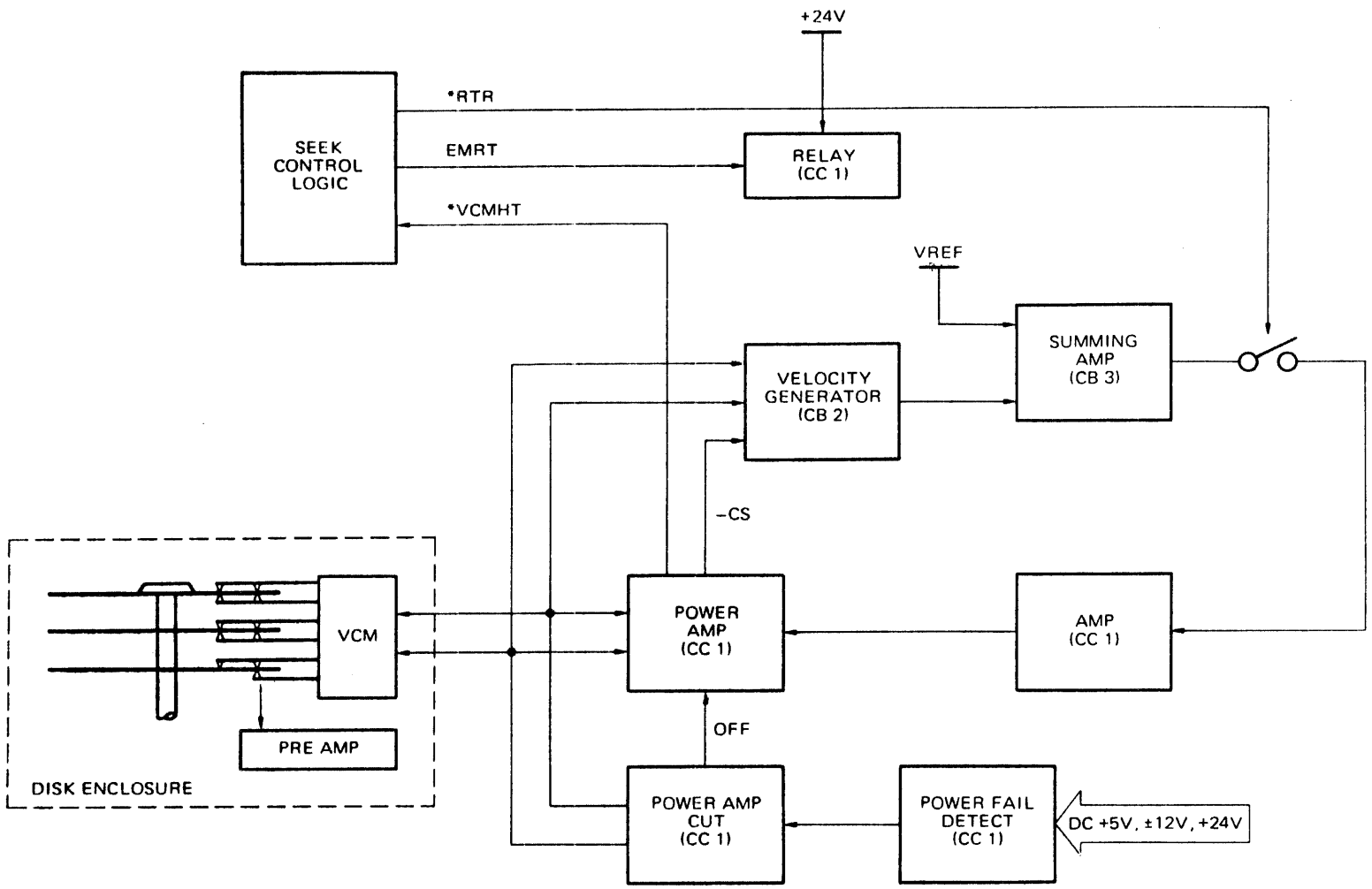


Figure 4-6-26 Retract Servo Control Block Diagram

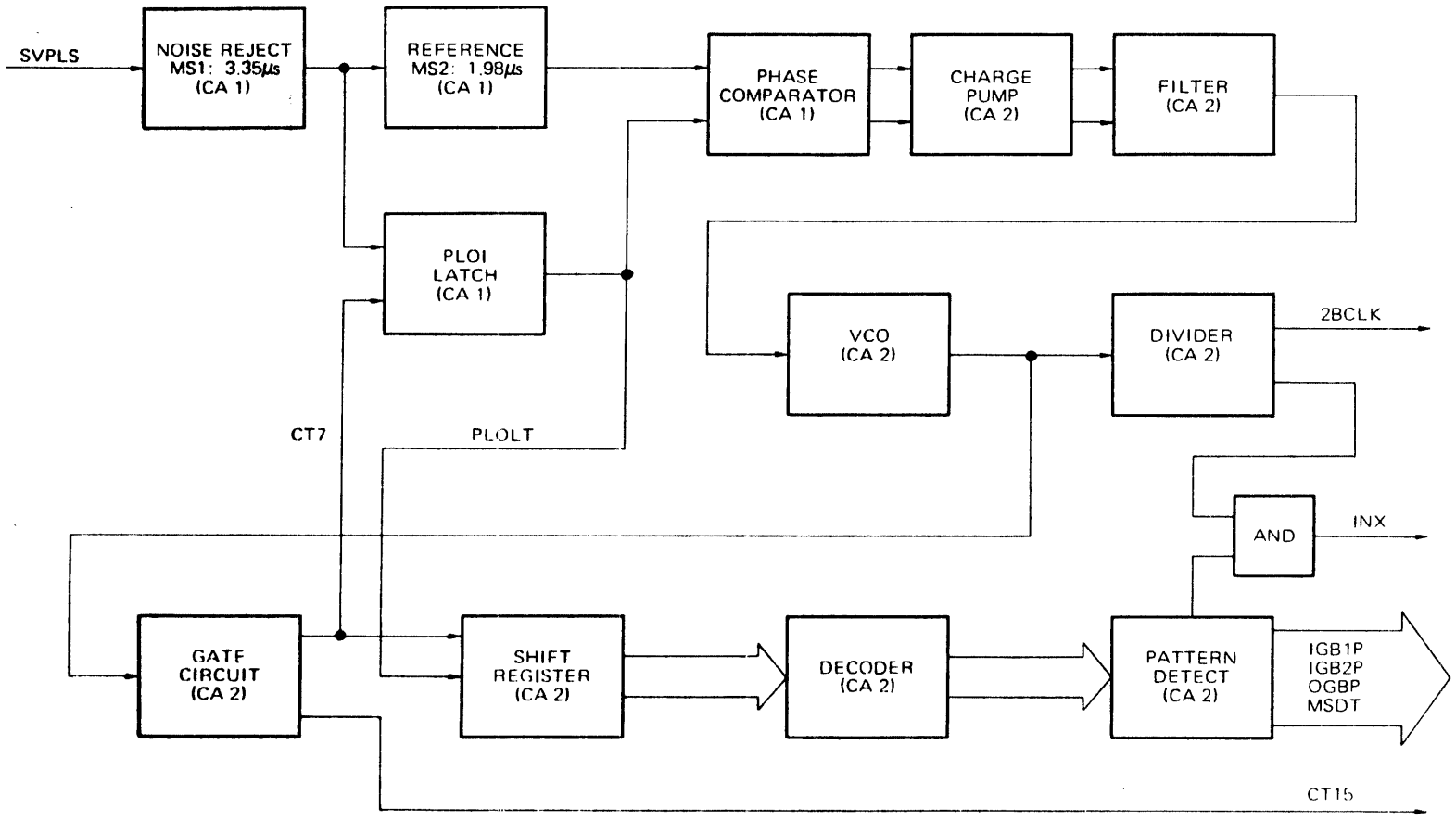
4.6.5 Index/Sector/Guard Band Generate Function

4.6.5.1 Missing Detect

As described in the Position Sensing discussion, the servo signal contains missing Sync Bits. The Servo Pulse (SVPLS) is applied to the Phase-Locked-Oscillator I (PLOI) which outputs a 2 Bit Clock.

The PLOI latch (PLOLT) which is set by the leading edge of Servo Pulse and reset by the leading edge at Count 7 (CT7), is applied to a shift register and clocked by the positive going edge of the CT7 signal.

The shift register outputs are decoded into decimal, and then Even Index, two Inner Guard Band (IGB1, 2) patterns and Outer Guard Band (OGB) are detected by the combination of the decoder outputs. The missing detect block diagram is shown in Figure 4-6-27 and the timing chart is shown in Figure 4-6-28 and Figure 4-6-29.



VCO: Voltage Controlled Oscillator

Figure 4-6-27 Missing Detect Block Diagram

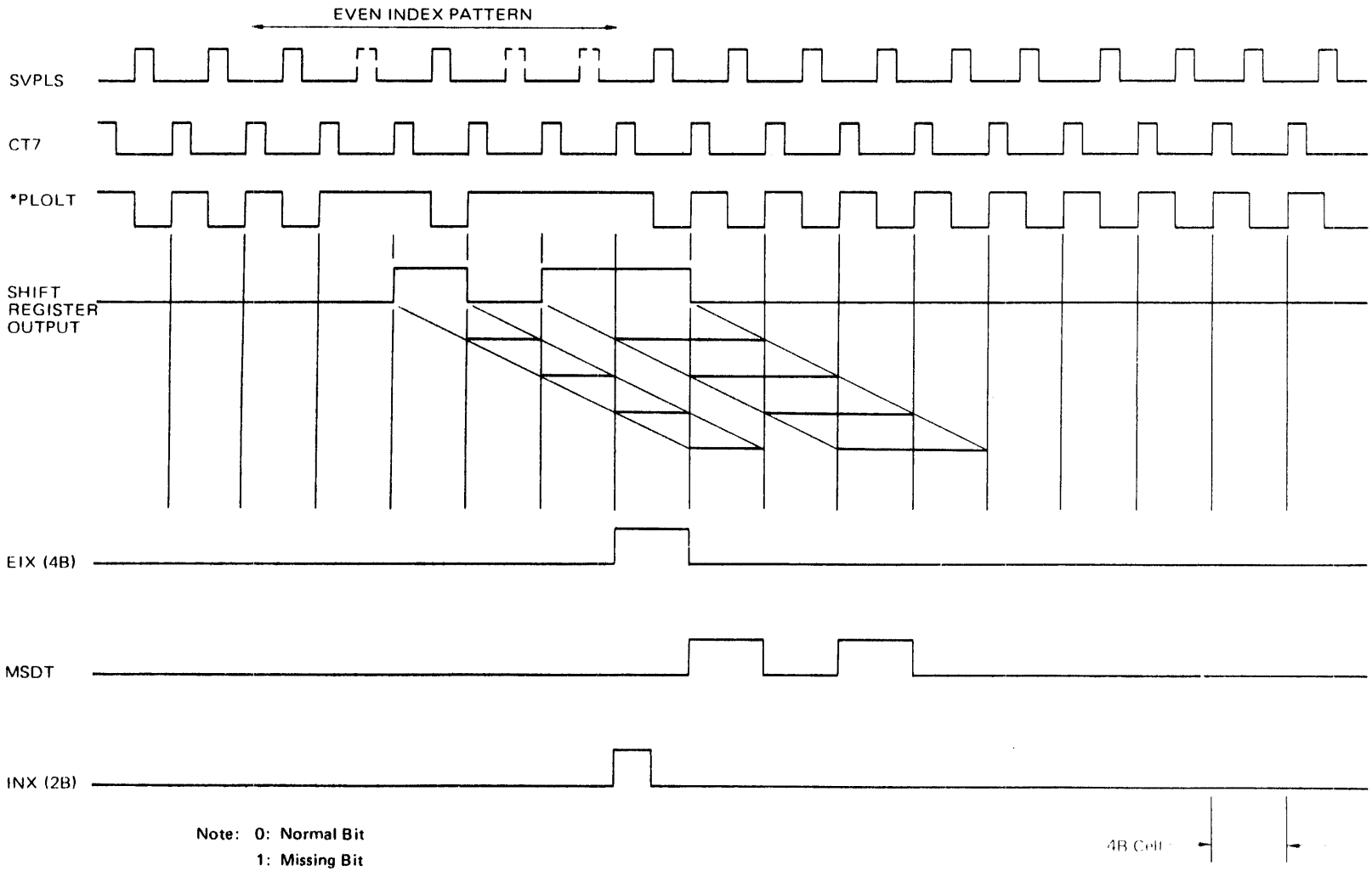


Figure 4-6-28 Index Detect Timing Chart

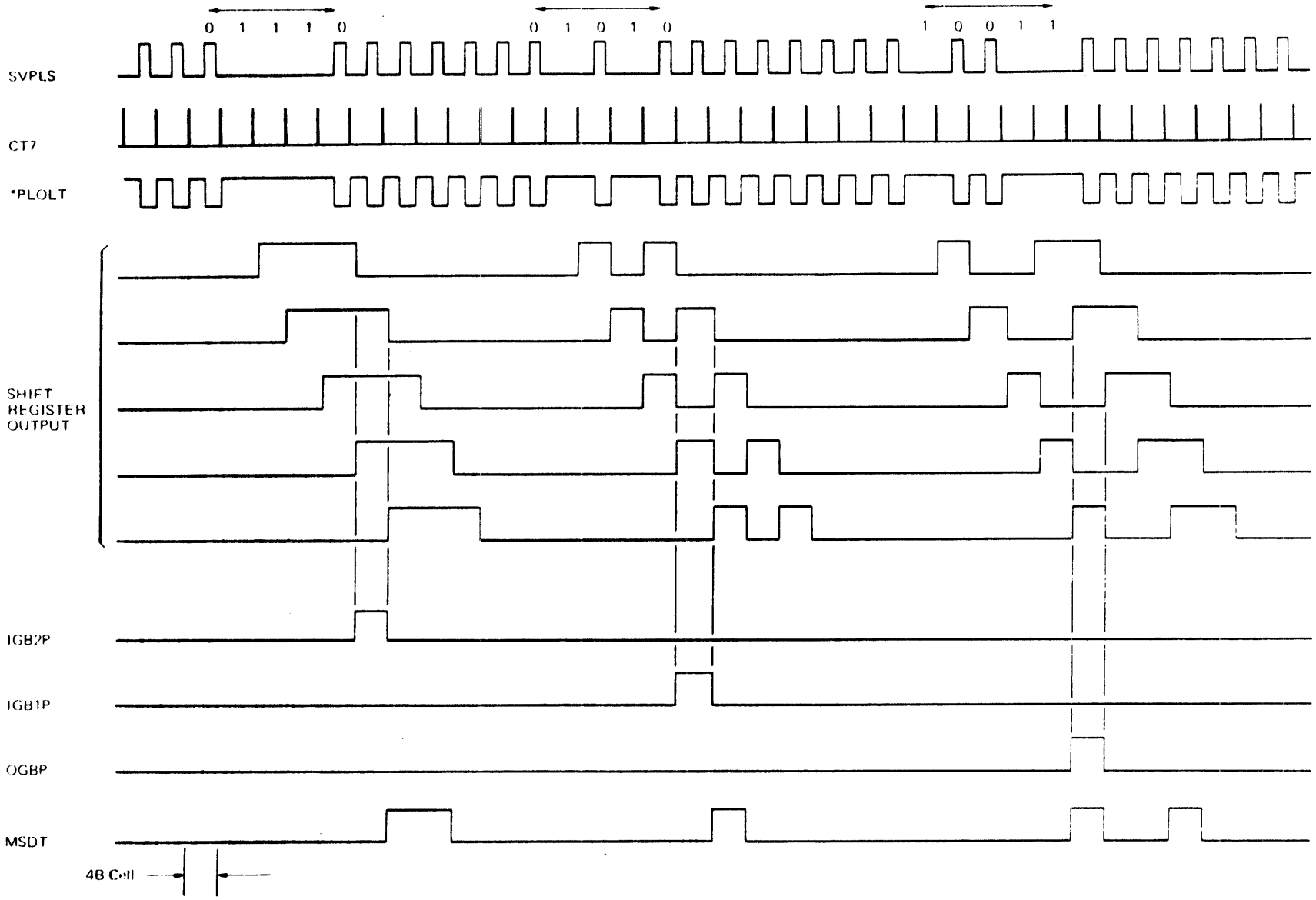


Figure 4-6-29 Guard Band Pattern Detect Timing Chart

4.6.5.2 Sector Generator

The sector pattern is not written on the servo surface. The sector pulse is derived from the Presettable Byte Counter by counting a Byte clock, which is generated by the PLO II circuit synchronized with Servo Pulse. One revolution has 20,480 Byte clocks, and sector length is determined by keys on the VOFM PCB.

The Index signal (2 Bytes) from the PLOI circuit enables the Preset Input to the Byte Counter. The value caused to be loaded into the Byte Counter is determined by the value of the VOFM PCB keys not turned on. For example, a 256 byte sector length is specified by turning on SW1 keys 1 to 7 and SW2 key 1. The binary value of the keys not turned on (SW2 keys 2 to 7) equals 65,280. The Index signal causes the Byte counter to be preset to 65,280. The counter is then clocked by the positive going edge of *1/8F clock (byte clock) until it reaches 65,535 (255 byte clocks). The next *1/8F signal would then cause a carry signal which is used as the Sector Pulse and a new preset enable to the Byte Counter. The process is repeated until the Index signal goes true.

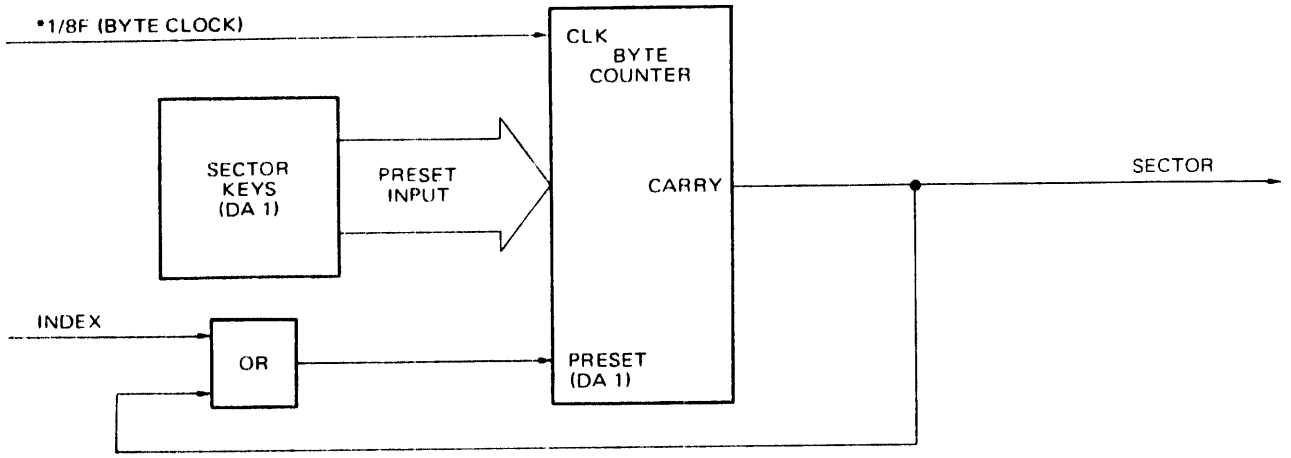


Figure 4-6-30 Sector Generating Block Diagram

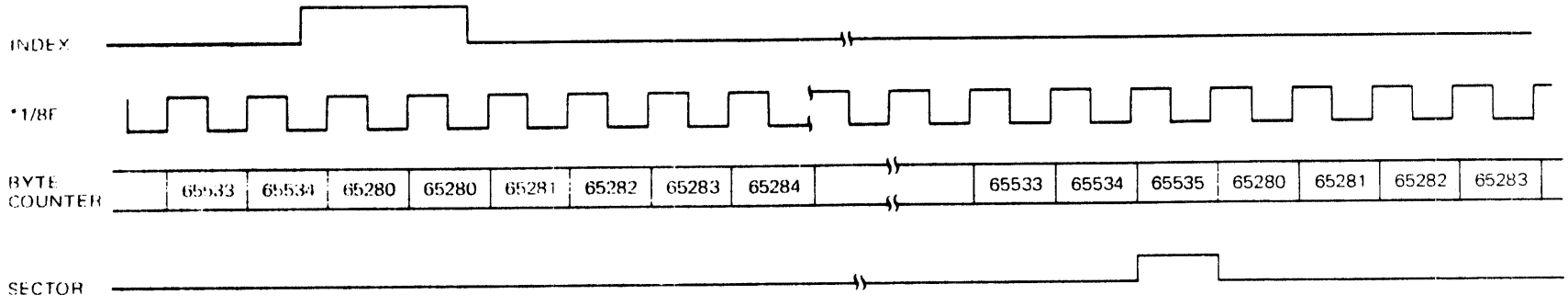


Figure 4-6-31 Sector Generating Timing Chart

4.6.6 Head Selection

A head must be selected before a read or write operation can be performed.

A cylinder address is set by Tag 1 and a head address is set by Tag 2.

Bus bits 7, 8 and 9 of Tag 1 determine whether the selected head is a fixed or access head.

(1) Access Head Selection

If Bus bits 7, 8 or 9 are false, the access head is selected and Fixed Head Selected (FHDSL) goes false. The subsequent Tag 2 signal sets Bus bits 0 to 3 into the Head Address Register (HAR). The HAR outputs, HAR 1, 2, 4 and 8, are applied to the Read Switch PCB (RQVM/RQWM). The signals HAR 4 and 8 are decoded into Chip Select 1, 2, 3 (CS1/CS2/CS3) and then applied to Head IC's in the Disk Enclosure.

On the other hand, lower bits HAR 1, 2 are converted into ECL level (Head Select 1/2/3: HS1/HS2/HS3) and then applied to each Head IC.

Through this process, the specific head is selected.

A multiple chip select error is detected by an over load current of the VCC supply.

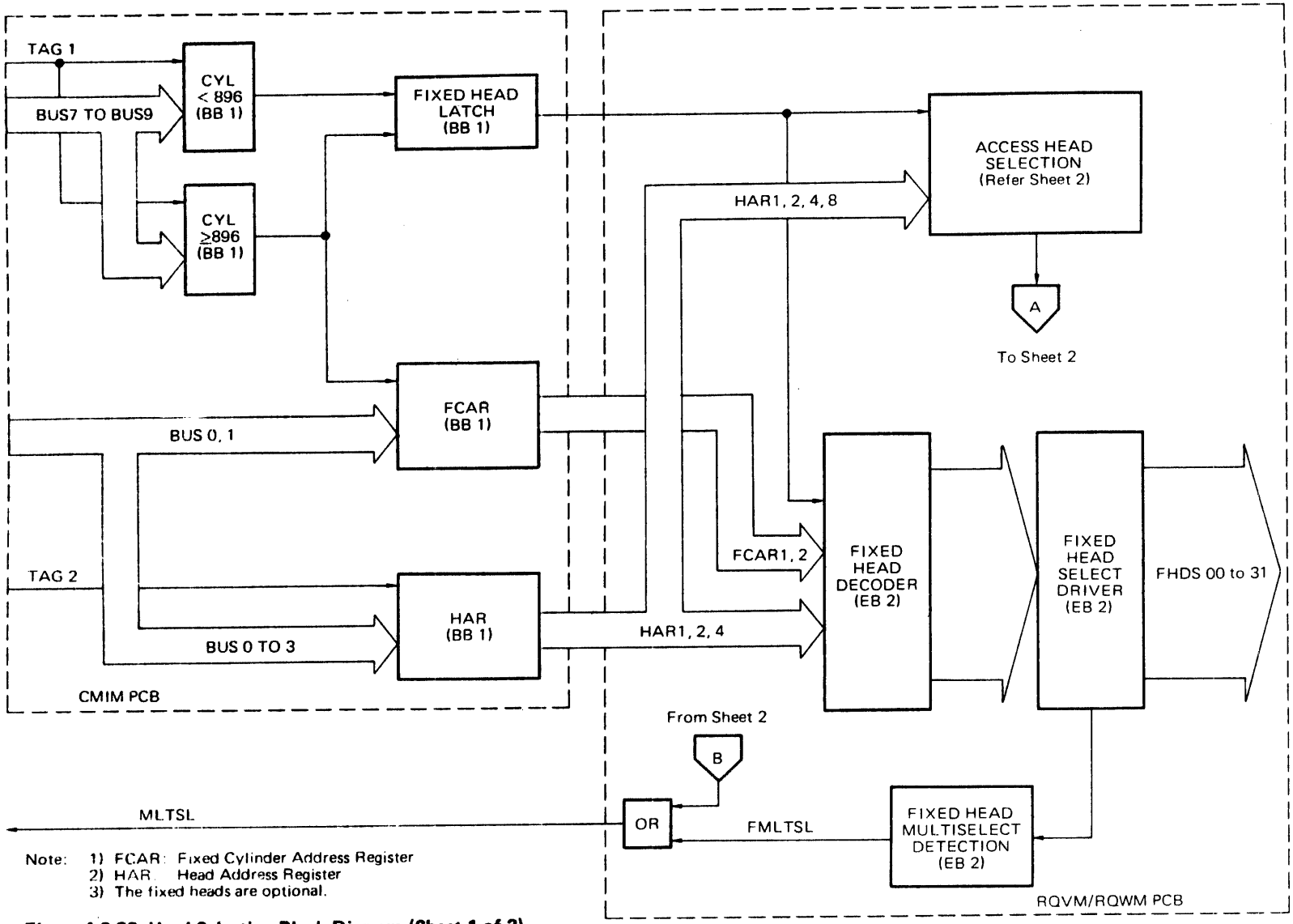
(2) Fixed Head Selection

If during Tag 1 Bus bits 7, 8 and 9 are true, the fixed heads are selected and FHDSL signal goes true. Then Bus bits 0 and 1 are set in the Fixed Cylinder Address Register (FCAR 1, 2) by the leading edge of Tag 1. The subsequent Tag 2 sets Bus bits 0 to 2 in Head Address Register.

HAR 1, 2, 4, FCAR 1 and 2 are applied to the Read Switch PCB and decoded into decimal 0 to 31. The decoder outputs are sent to the head select drivers, and then a specific fixed head is selected.

The head select driver outputs, FHDS 00 to 31, are connected to each fixed head. If more than one fixed head is selected, Fixed Head Multi-Selected (FMLSL) signal goes true. This FMLSL signal is ORed with the multi-chip selected signal and sent to a fault detection circuit.

The Head Selection block diagram is shown in Figure 4-6-32.



Note: 1) FCAR: Fixed Cylinder Address Register
2) HAR: Head Address Register
3) The fixed heads are optional.

Figure 4-6-32 Head Selection Block Diagram (Sheet 1 of 2)

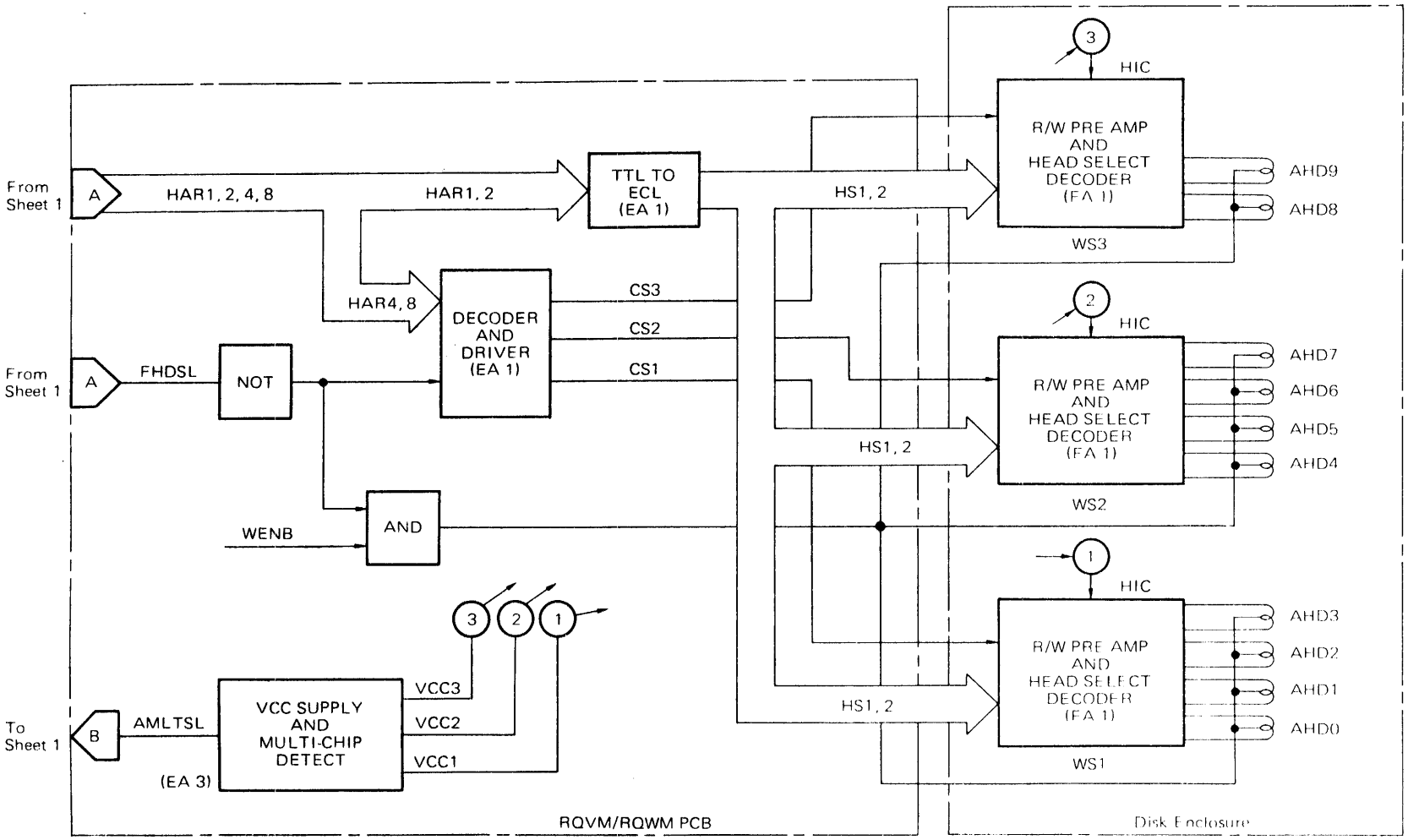


Figure 4-6-32 Head Selection Block Diagram (Sheet 2 of 2)

4.6.7 Read/Write Function

4.6.7.1 Read/Write Basic Principles

When the disk is rotating at 2,964 RPM, Read/Write is performed by means of the R/W heads. The basic principles of the read/write function will be described in the following paragraphs.

(a) Data Write

During a Write instruction, a 0 or 1 is recorded by reversing the direction of the current flowing in the data head coil. When the direction of the current flowing in the head coil is reversed, the magnetic poles of the head are reversed and the direction of magnetic flux at the gap is reversed. The direction of magnetization of the surface of the disk is then reversed. Each flux reversal means that a "1" or "0" has been recorded on the disk.

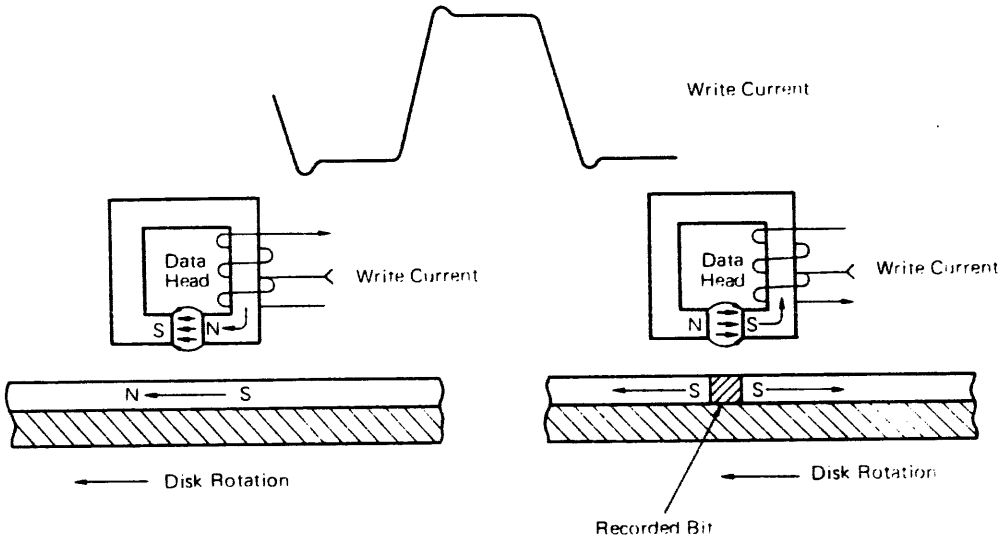


Figure 4-6-33 Data Write

(b) Data Read

During a Read instruction, the transitions recorded on the surface of the disk are detected by the head gap. When magnetized in the same direction continuously, no output is produced. However, when a recorded bit (180 degree flux reversal in the horizontal direction) passes under the head gap, the magnetic flux flowing in the ring and coil is reversed and an output pulse is obtained.

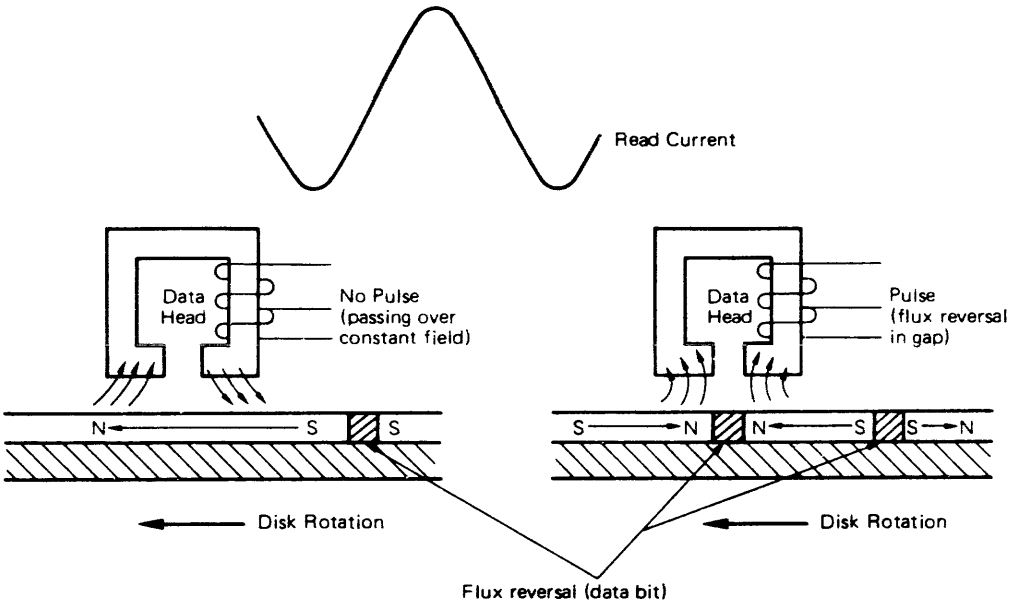


Figure 4-6-34 Data Read

(c) Principles of MFM Recording

This unit uses the Modified Frequency Modulation (MFM) recording technique. The length of time required to define one bit of information is the cell. Each cell is nominally 123 ns in width (1FW or 1FR).

MFM defines a "1" by writing a pulse at the half-cell time. A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is clock (1 FW). However, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rule for MFM recording may be summarized as follows:

1. There is a flux transition for each "1" bit at the time of the "1".
2. There is a flux transition between each pair of "0" bits.
3. There is no flux transition between the bits of a "10" or "01" combination.

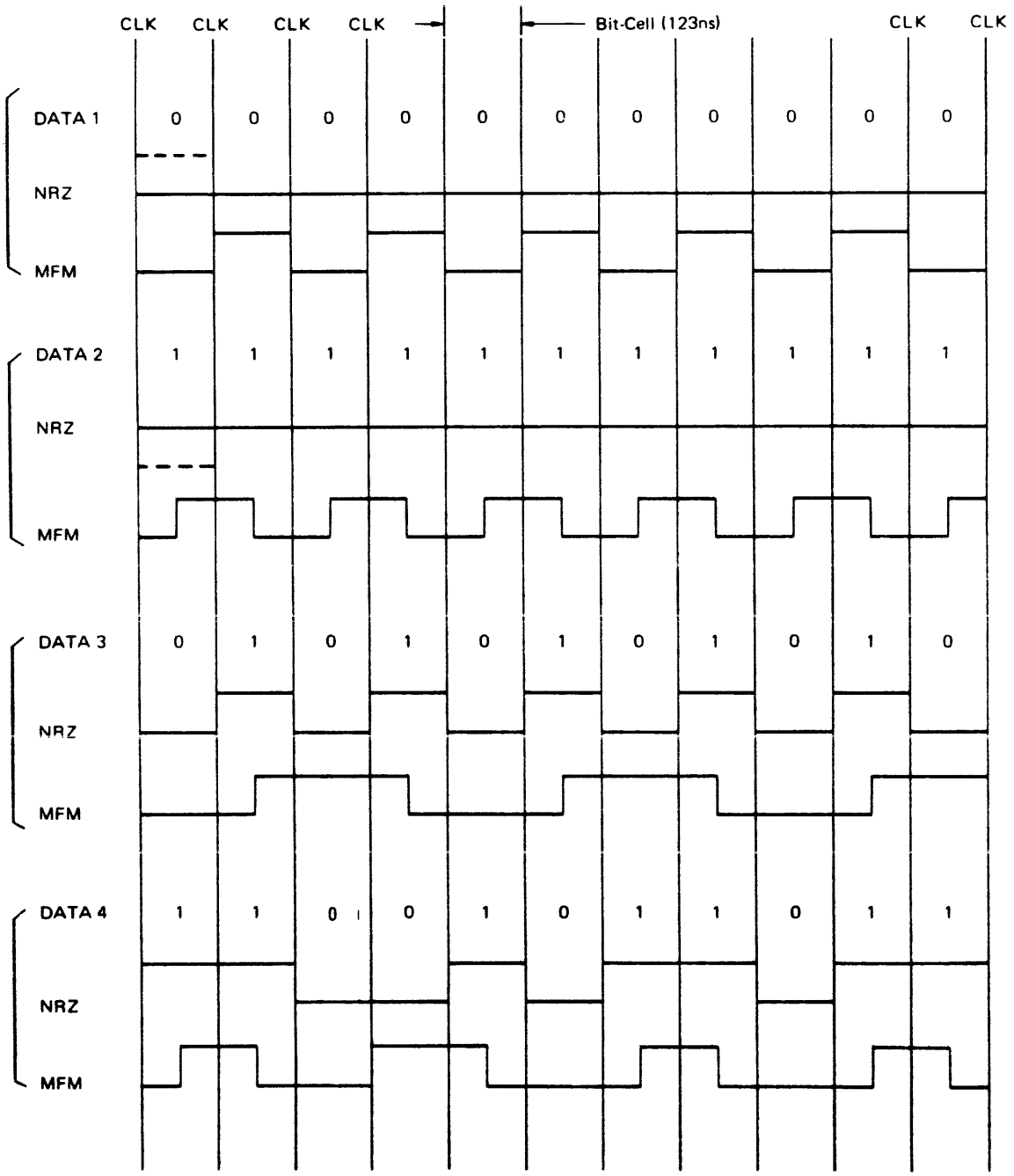


Figure 4-6-35 MFM Coding

4.6.7.2 Write Operation

The write circuit block diagram is shown in Figure 4-6-36.

The servo data written on the servo surface of the disk is read by the servo head and (transfered to) the PLOI circuit to generate 1 Byte clock, which is applied to the PLOII circuit. The PLOII circuit develops 1 bit cell PLO1F. The PLO1F is input to the VFO. The VFO is synchronized with this signal and generates a frequency double the PLO1F frequency, then outputs VFO1F and VFO2F. VFO1F and VFO2F are sent to the write compensator (W.C.P.) and VFO1F is also sent to the control unit as the 1F write clock. The control unit must use this write clock in generating the write data. A head must be selected before writing.

When a write instruction is sent from the control unit and the write clock and write data synchronized with the 1F write clock are sent, they are input to a FF (Flip Flop Circuit) through a receiver. The phase of the WRITE DATA is compensated and the data is input to the write compensator. The write compensator converts the NRZ data (WD) to MFM data pulses (*WDP) and compensates its phase. *WDP is input to a FF where it becomes MFM data. This MFM data is sent to the write driver

When Access Head Select (AHDSL) goes true, the write data passes through the Read/Write Bus Switch, and is applied to Head IC (HIC) chips as DX and DY signals. The write current is supplied to the selected HIC chip through a write current 1/2/3 (WC1/WC2/WC3) line. A Head Address line, HAR 1, changes the write current depending on whether the selected head is even or odd. A head closer to the spindle receives less current because the bit density is higher.

On the other hand, when a fixed head is selected, the Write Current drives the Write Data Driver with a constant current. One fixed head functions to write data on a specified track.

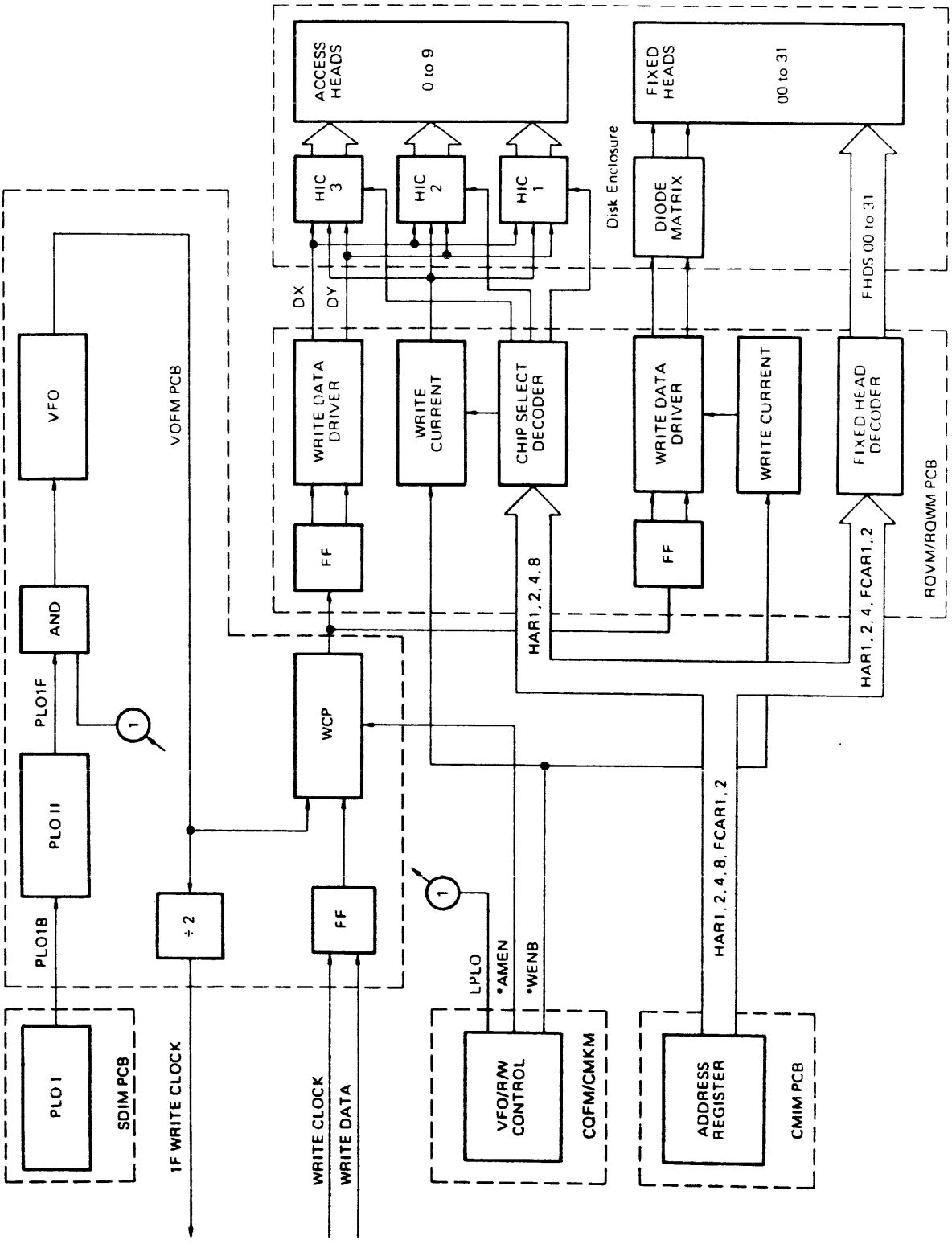


Figure 4-6-36 Write Operation Block Diagram

4.6.7.3 Write Compensation and MFM Coding

When the bit density (BPI) is high on a disk surface, and a read operation is performed, a peak shift phenomenon appears, which tends to widen the narrow part of the bit spacing because of mutual magnetic interference of the bits. Therefore, when such a phenomena appears, reading of the data will deviate from the correct bit spacing, causing errors. The write compensation circuit measures this peak shift beforehand so that the data is written by shifting the peak in the opposite direction of the peak shift appearing during the read operation.

The NRZ write data sent from the controller is synchronized by the write clock and then enters this circuit. The two clocks VFO2F and VFO1F from the VFO also enter this circuit and the write data synchronized by the above write clock is again synchronized to the VFO1F clocks.

The NRZ write data is converted to MFM write data and is simultaneously pre-shifted for write compensation by this circuit. When the variable length sector format is used, the Address Mark (DC erase) is written by this circuit so that write data pulses do not appear.

The block diagram and timing charts are given in Figure 4-6-37 and Figure 4-6-38 and Figure 4-6-39. The truth table is given in Table 4-6-1.

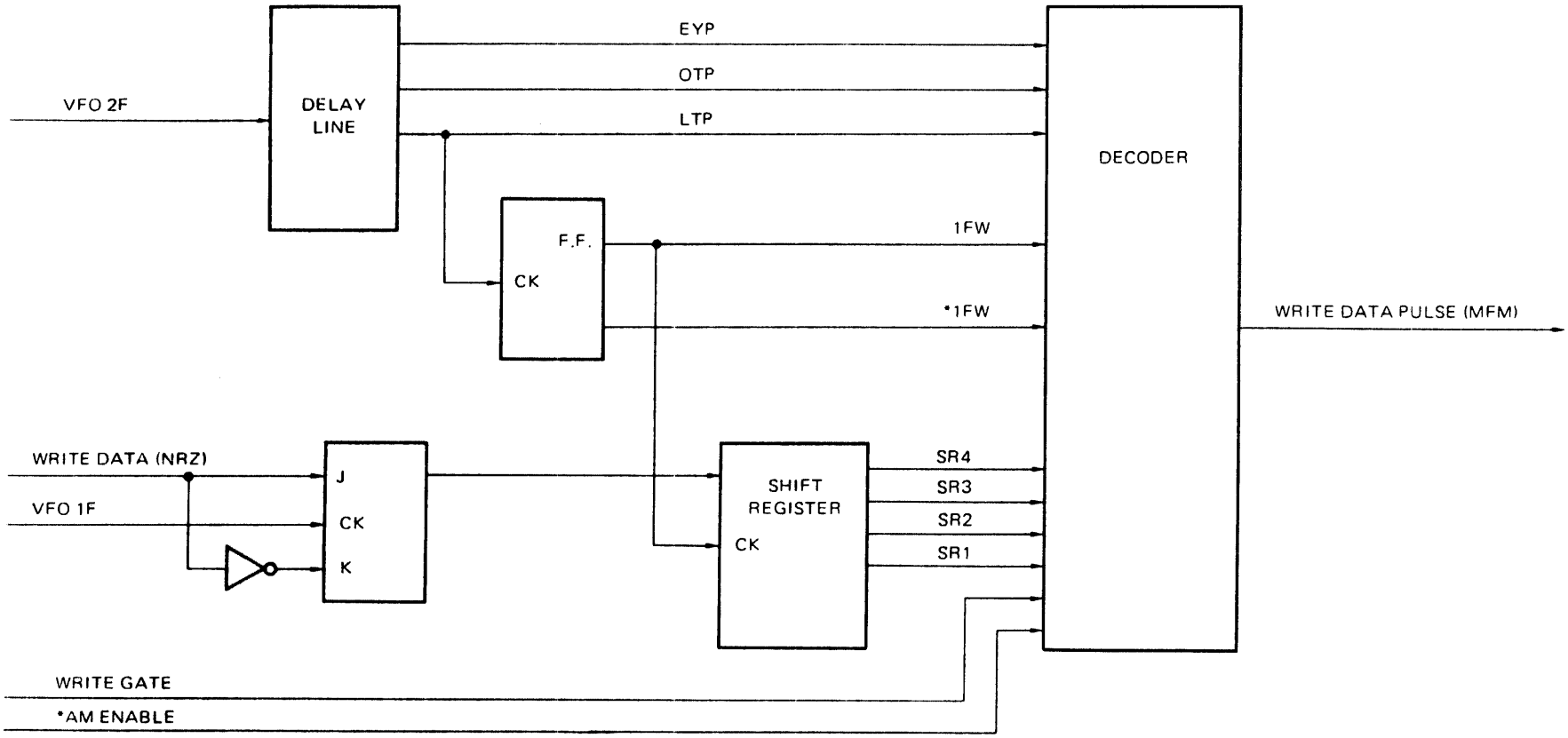


Figure 4-6-37 Write Compensation and MFM Coding Block Diagram

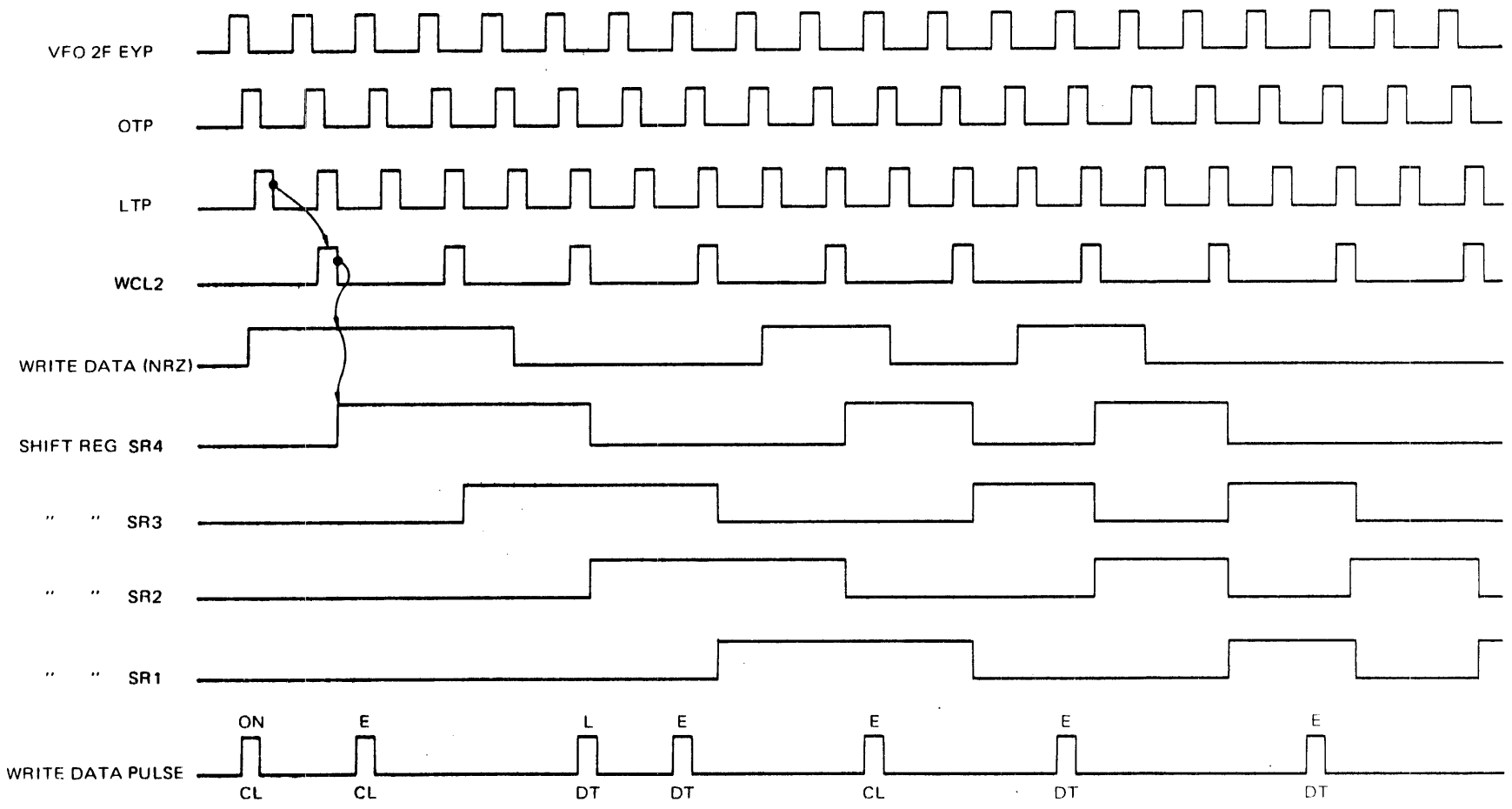


Figure 4-6-38 Write Compensation and MFM Coding Timing Chart

MFM write data/clock is early/on time/late depending on the contents in the shift register as shown in Table 4-6-1. MFM write data pulse follows contents of the shift register on SR3, and is clocked with EYP, OTP, or LTP depending on the contents of SR4, 2 and 1.

Table 4-6-1 Write Compensation and MFM Truth Table

SHIFT REGISTER STATUS				WRITE COMP			MFM	
SR4	SR3	SR2	SR1	EYP	OTP	LTP	CLP	DTP
1	0	0	*	1	0	0	1	0
0	0	0	0	0	1	0	1	0
0	0	0	1	0	0	1	1	0
0	1	*	*	1	0	0	0	1
1	1	1	*	0	1	0	0	1
1	1	0	*	0	0	1	0	1

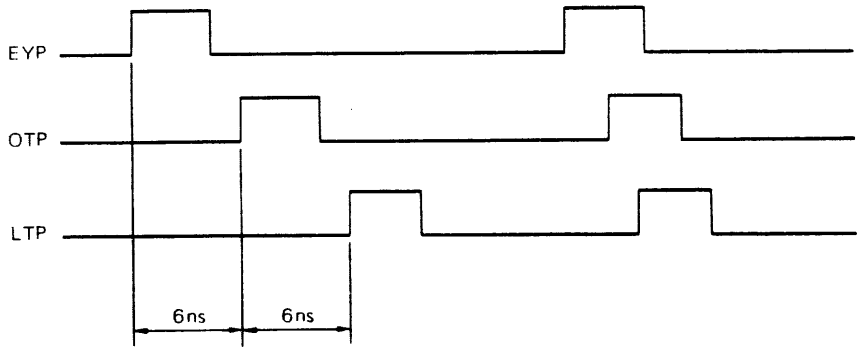


Figure 4-6-39 Write Compensation Shift

4.6.7.4 Read Operation

A Read operation is initiated by enabling Tag 3 and Bus 1 (Read Gate: RG); however, the read analog circuit is enabled by disabling Write Enable (WENB).

In the case of the Read Switch PCB with the fixed head functions (RQVM, PCB), when the access head is selected, the read preamplifier (Head IC: HIC) in the Disk Enclosure is activated after a write operation. The DX, DY HIC outputs are applied to the Read/Write Bus Switch circuit, amplified, and sent to the Multiplex Amplifier (refer to Figure 4-6-40).

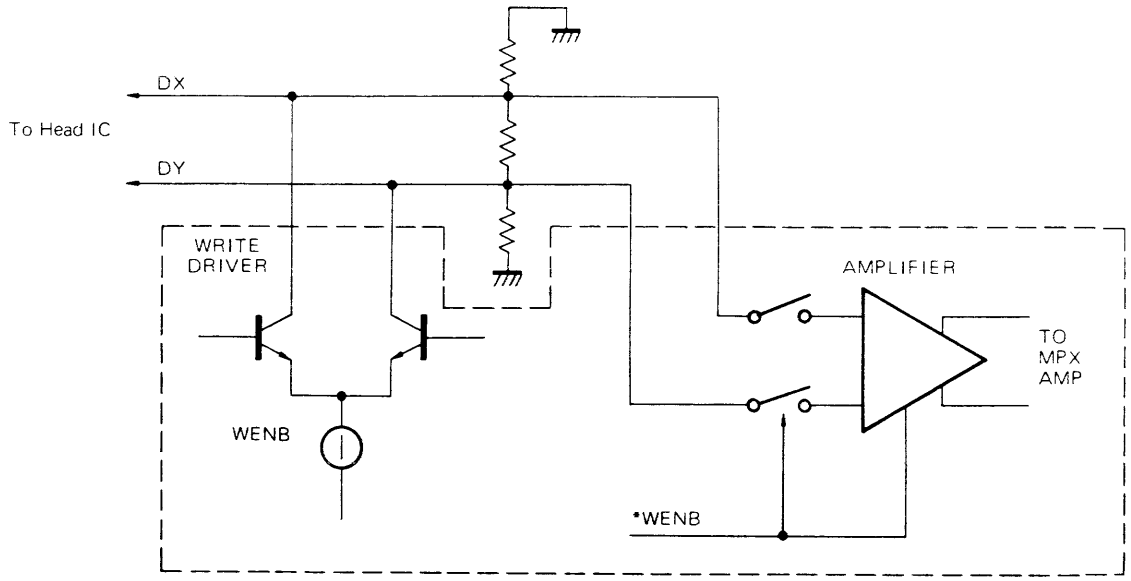


Figure 4-6-40 Read/Write Bus Switch

On the other hand, when a fixed head is selected, the magnetic field flux transitions are sensed by the head coil and then applied to the Fixed Head Preamplifier through a Diode Matrix circuit. The Fixed Head Preamplifier output (ten amplifications) is applied to a Low Pass Filter (LPF) to attenuate unuseful high frequency noise, and then applied to the Multiplex Amplifier.

In the case of Read Switch PCB without the fixed head functions (RQWM PCB), the DX, DY signals are amplified by ten amplifications and sent to LPF circuit.

The output of the Read/Write Bus Switch (without fixed head functions) or the Multiplex Amplifier (with fixed head functions) is applied to an LPF circuit to attenuate the unuseful high frequency noise, and sent to the Automatic Gain Control (AGC) circuit.

The AGC circuit develops the control voltage to the AGC amplifier and holds AGC output amplitude (280 mVp-p) at a constant level. The output of the AGC amplifier is amplified by ten amplifications (2.8Vp-p), and then sent to the Pulse Shaper circuit.

After going false at WENB, the read circuit is activated; however, a read-transient which is caused by the DC unbalance of the read pre-amplifier will occur. WENB signal squelches this read transient (refer to Figure 4-6-41).

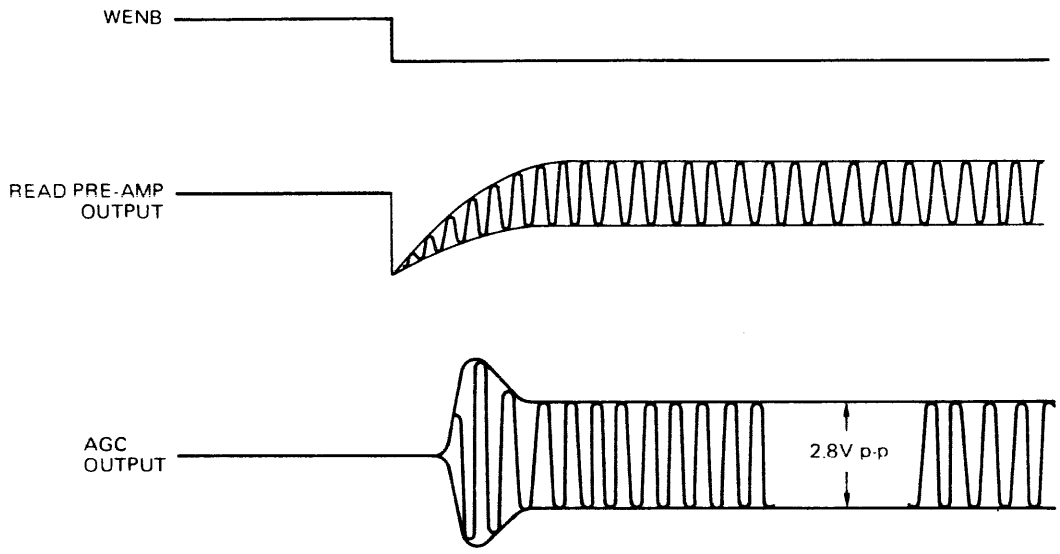


Figure 4-6-41 AGC Squelch Function

In the Variable Soft Sector mode, the Address Mark (AM) which is a DC-erased 3 Byte area is used for the beginning of sectors. When the control unit issues an AM-Read (Tag 3 -- Bus 1 -- Bus 5) command, the AM-Search (AMSH) signal goes true and surppresses the AGC output amplitude to avoid mis-detection of an AM caused by external or media noise in the DC-erased area (refer to Figure 4-6-42).

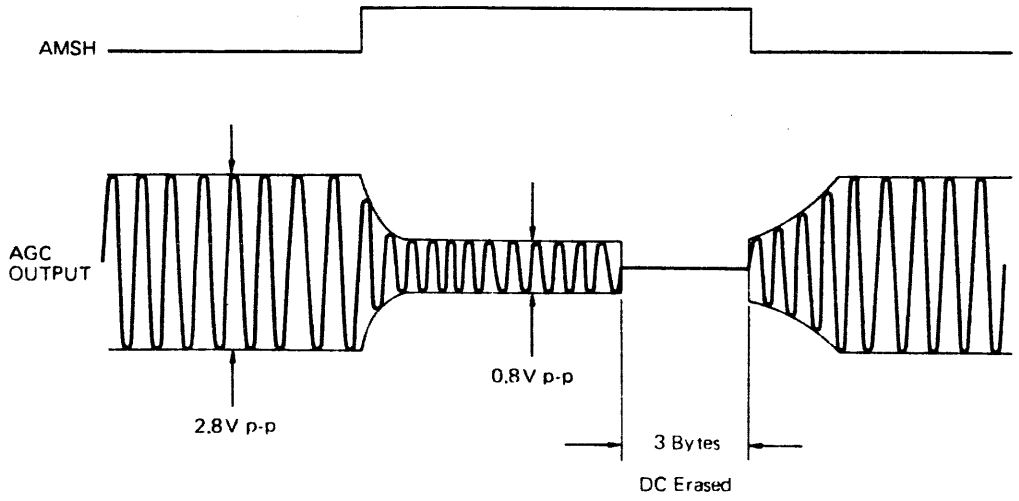


Figure 4-6-42 AM Search on Read Signal

The analog to digital convertor circuit, which is called a Pulse Shaper, has two fundamental circuits. One is a Differentiator circuit which differentiates the AGC output signal and then converts the peaks (flux transisitions) into zero-crossing signals. The other is an Integrator circuit which AC-slices the AGC output signal (floating slice) and then generates the data window for the MFM read data pulse. The block diagram is shown in Figure 4-6-43 and the detail timing chart is shown in Figure 4-6-44 and 4-6-45.

The output of the analog to digital convertor which is Raw Read Data (RRD 1/2), is sent to the VFO circuit.

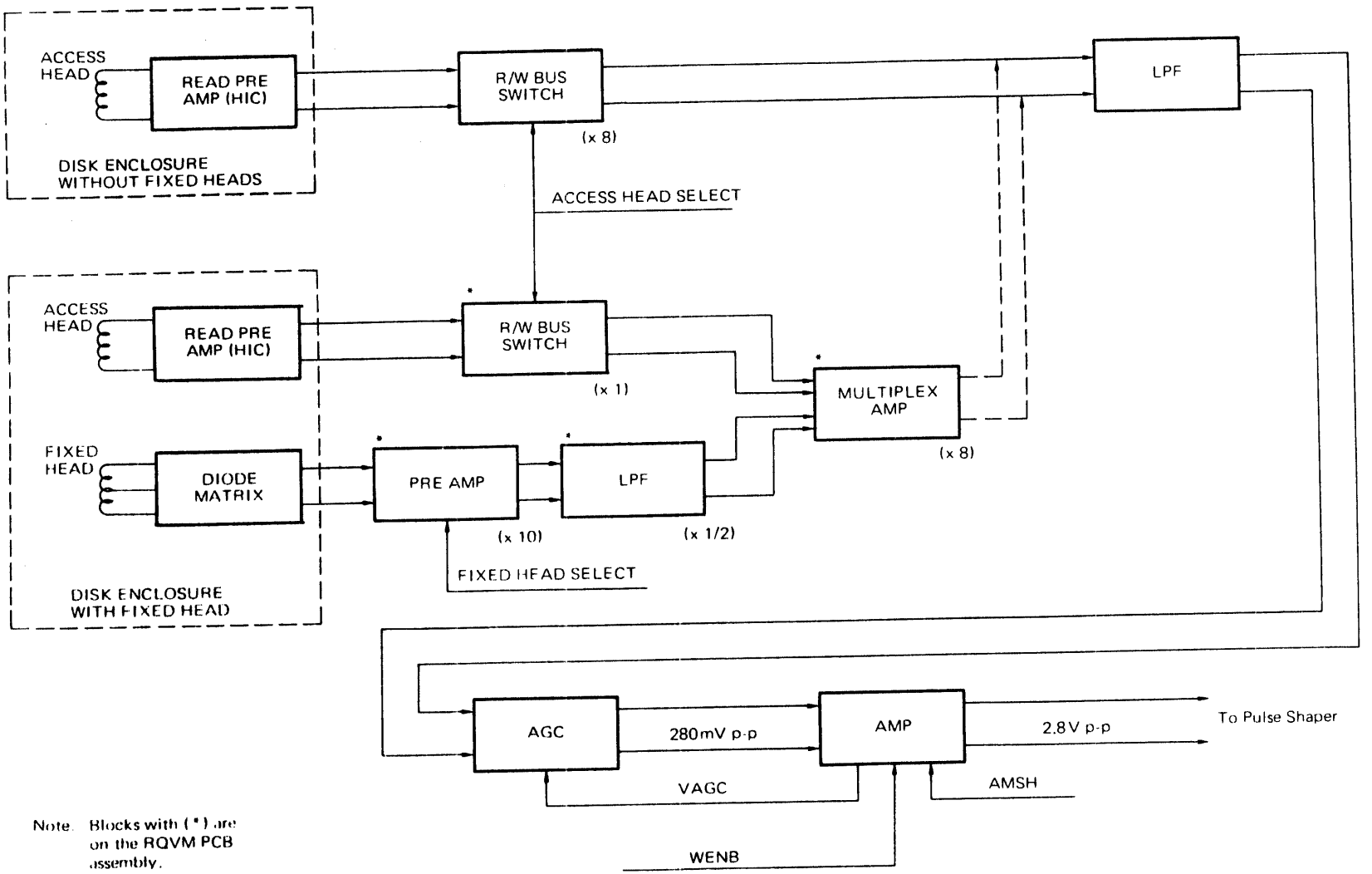


Figure 4-6-43 Analog Read Data Block Diagram

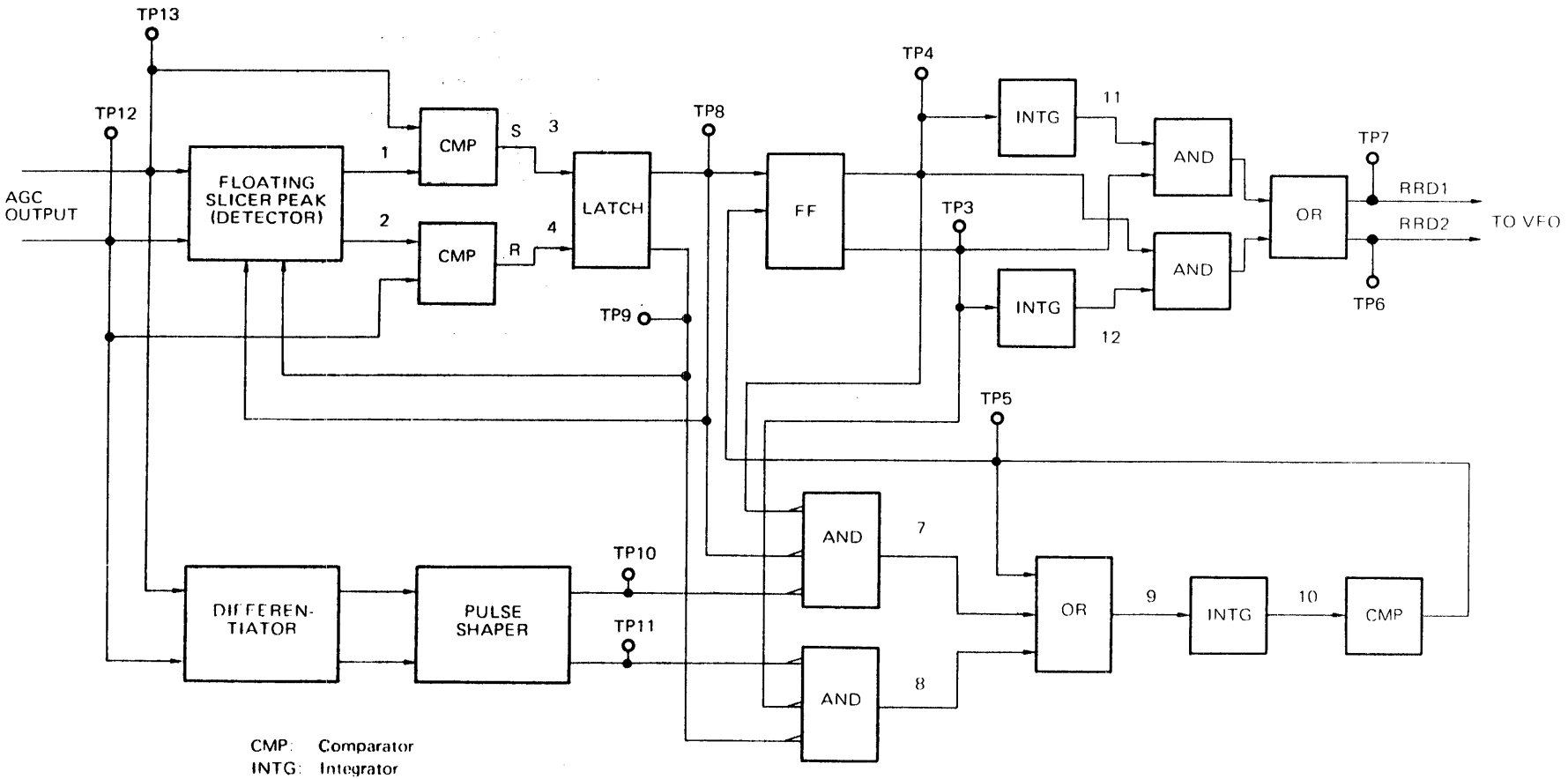


Figure 4-6-44 Read Data Analog to Digital Block Diagram

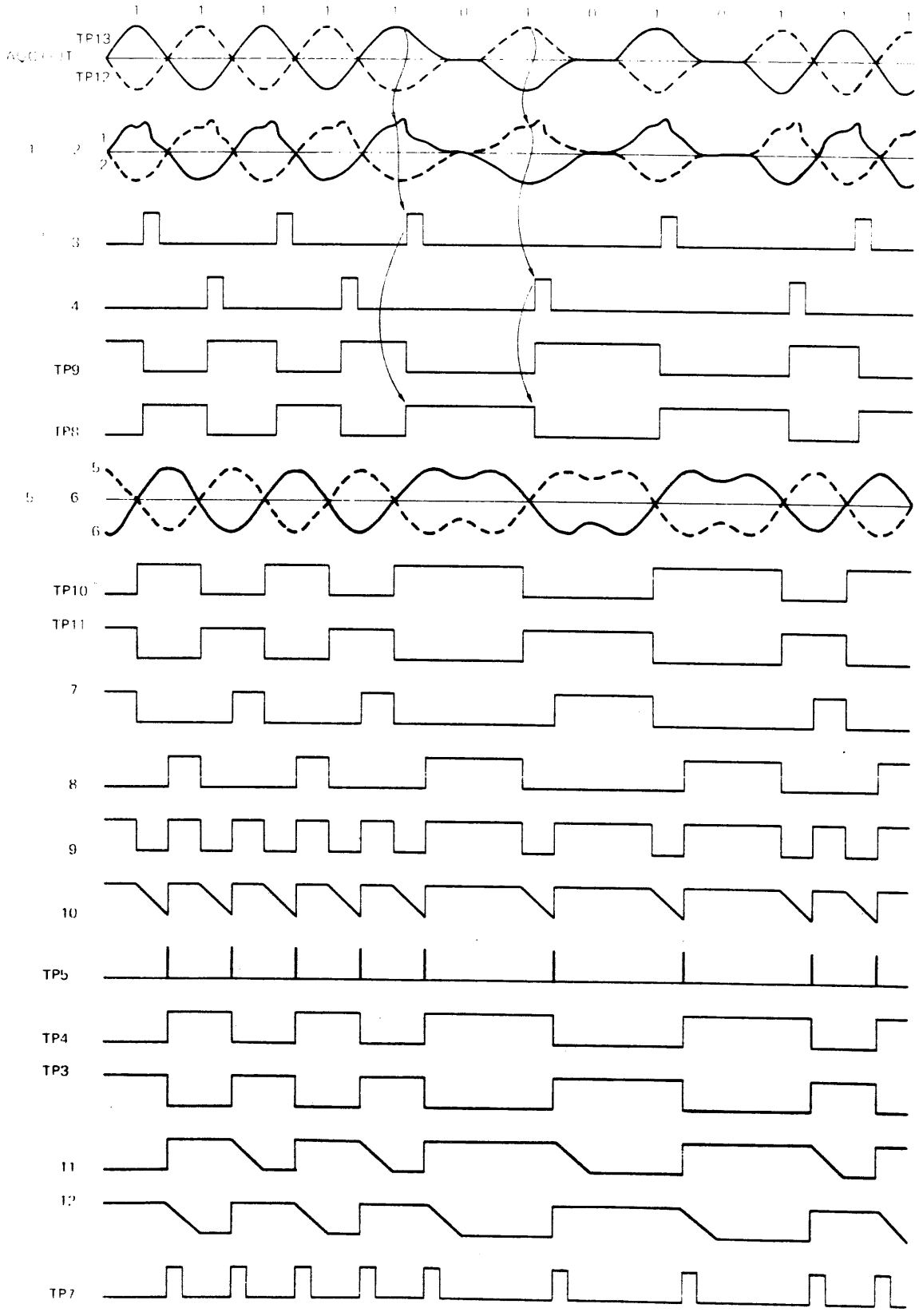


Figure 4-6-45 Read Data Analog to Digital Timing

4.6.7.5 PLO/VFO

(1) General

The PLO II (Phase-Locked-Oscillator) develops a bit clock which is synchronized with the 2 Bytes clock from the PLO I circuit.

The PLO II output signal, PLO1F, is applied to the VFO (Variable Frequency Oscillator) circuit during a not-read operation.

The VFO circuit synchronizes with a PLO1F signal from the servo track during a not-read operation and with the Raw Data signal from a data track during a read operation.

The PLO/VFO block diagram is shown in Figure 4-6-46.

(2) PLO II

The PLO II circuit develops a bit clock which is synchronized with the 2 Bytes clock from the PLO I circuit. The PLO II generates a bit clock PLO1F signal and timing clocks CLK1 and CLK2 for the VFO timing control circuit.

The functional block diagram is shown in Figure 4-6-47.

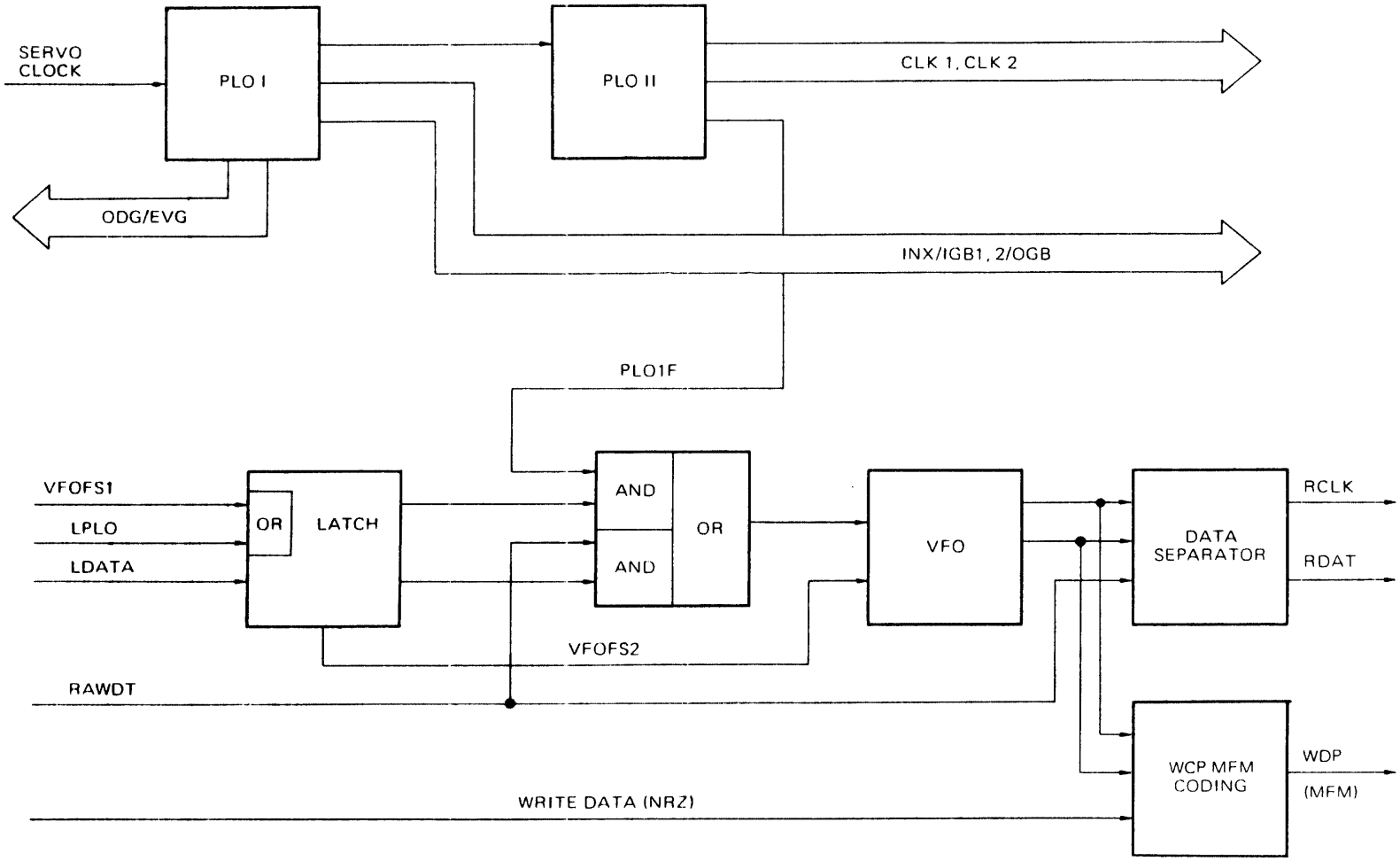
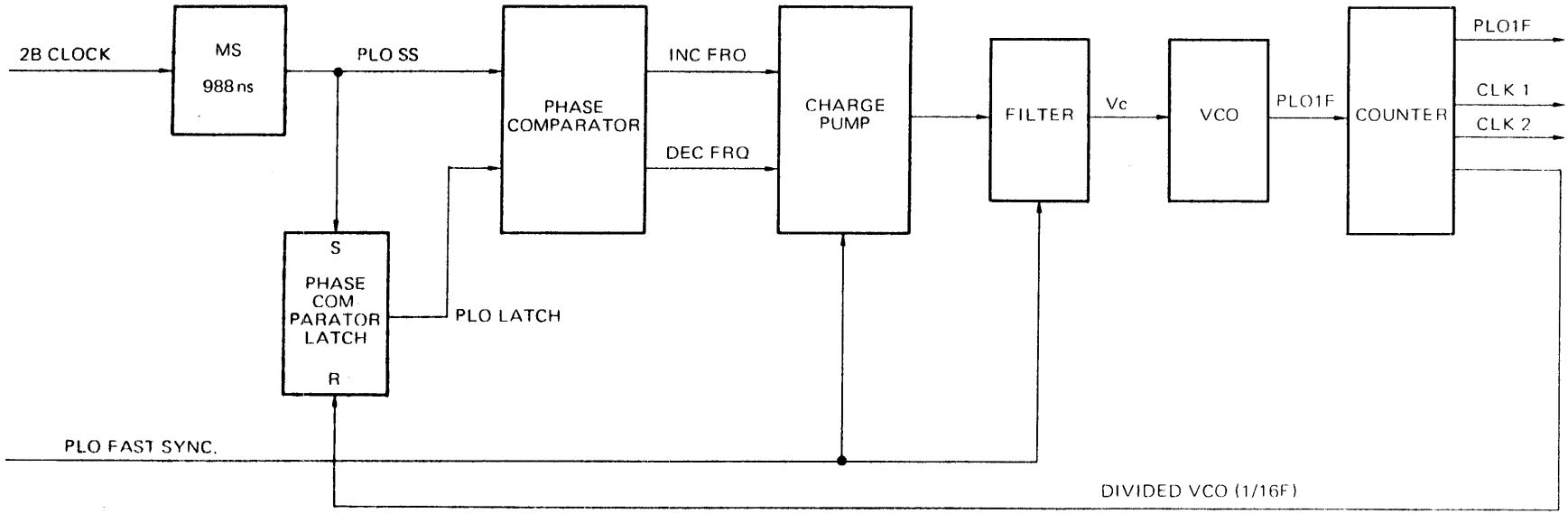


Figure 4-6-46 PLO/VFO Block Diagram



(1) VCO oscillates at 8.1MHZ when there is no input signal. (Vc=0V)
(2) When the 988ns monostable multivibrator is triggered by the positive-going edge of the 2B clock, the PHASE COMPARATOR LATCH is simultaneously set.
(3) The VCO output is divided to 1/16F by a COUNTER, and the PHASE COMPARATOR LATCH is reset by its Leading edge.
(4) PHASE COMPARATOR compares PLO SS and PLO LATCH and changes the control voltage Vc so that the phase is locked.
(5) PLO FAST SYNC is used to make the loop gain of the PLO signal high, the pull-in range large and shorten the pull-in time.

Figure 4-6-47 PLO Circuit Block Diagram

(3) Detailed description of PHASE COMPARATOR
The PHASE COMPARATOR compares PLO SS and PLO LATCH and locks the phase by changing the control voltage Vc by means of the compared result.

(a) Phase Lock
When the phases are locked, both INC FRQ and DEC FRQ are 0.

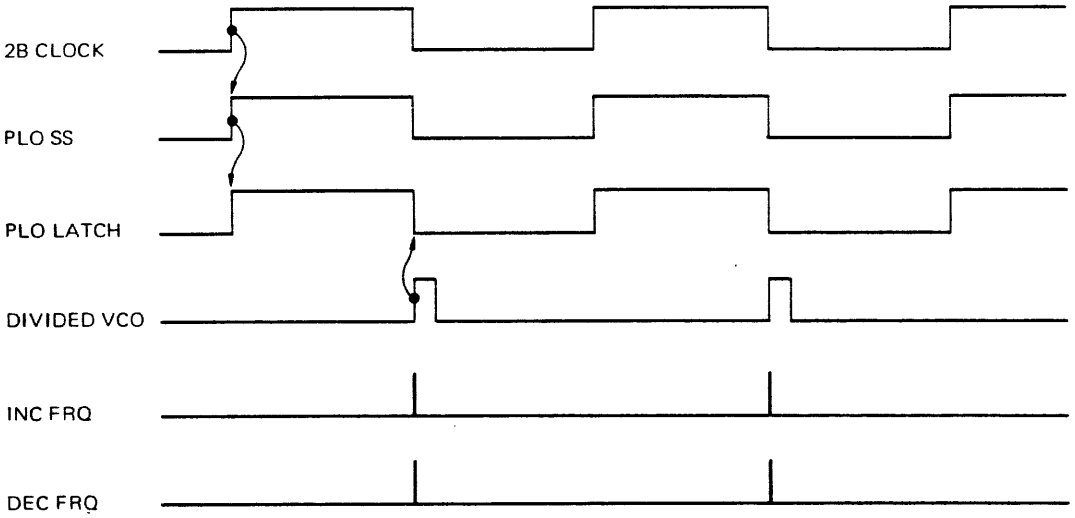


Figure 4-6-48 Phase Locked Timing Chart

(b) PLO phase leading
When the phase of the PLO is leading, the DEC FRQ output appears and the VCO operating frequency is lowered.

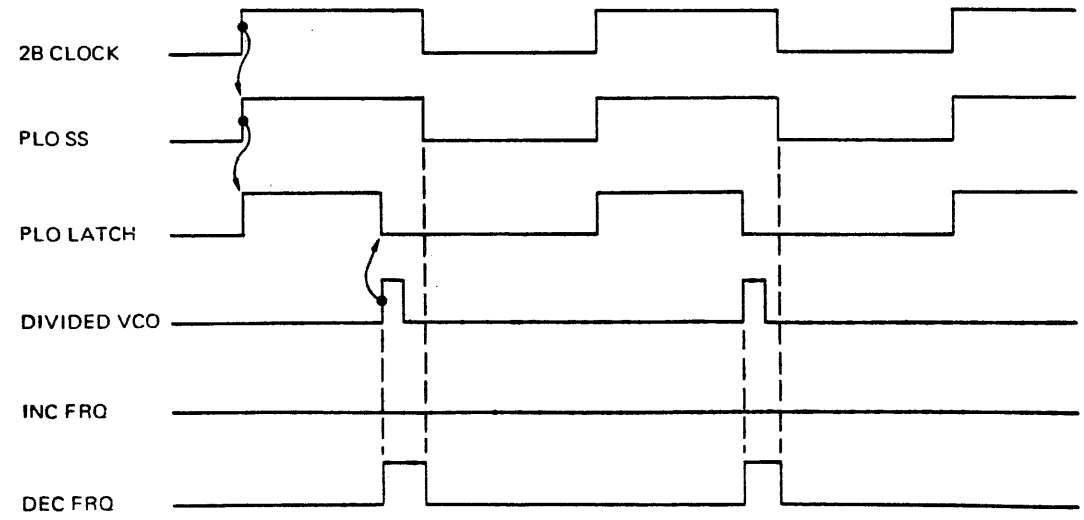


Figure 4-6-49 Timing chart when the phase of the PLO is leading

(c) PLO phase lagging
When the phase of the PLO lags, INC FRQ output appears and the VCO operating frequency is raised.

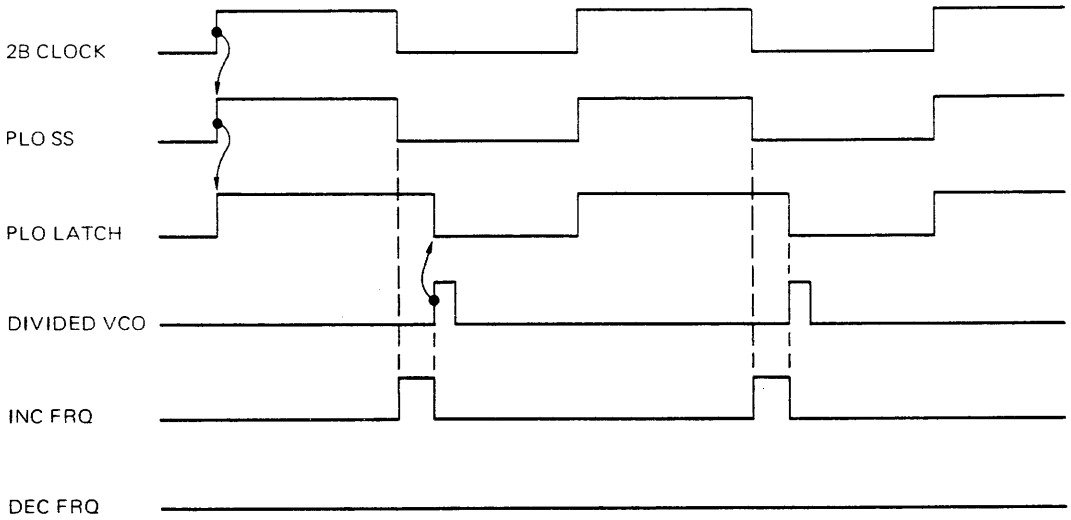
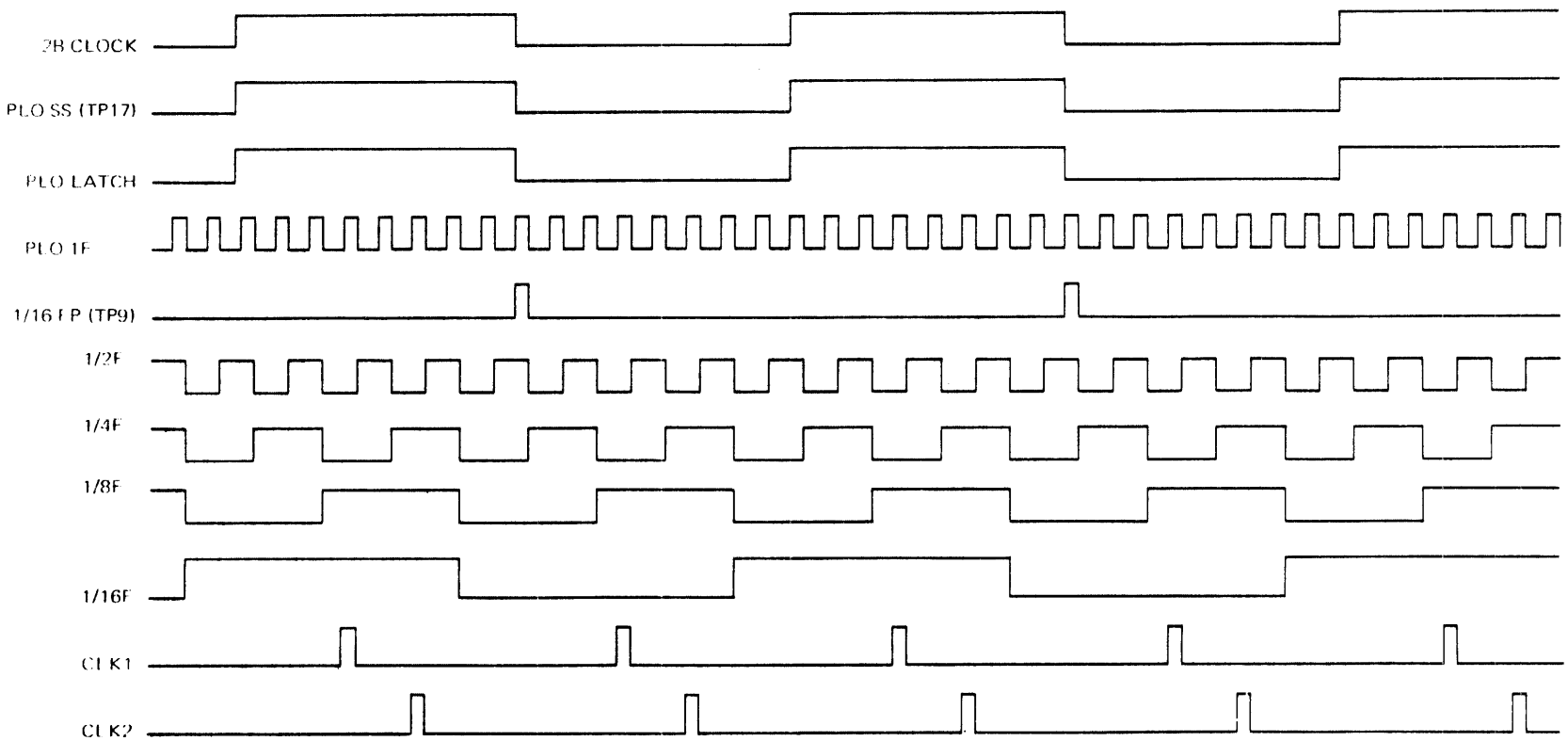


Figure 4-6-50 Timing chart when the PLO phase lags

(4) Generation of timing clocks (CLK1, CLK2)
The frequency of the PLO1F output of the VCO is gradually divided to 1/2F, 1/4F, 1/8F and 1/16F by a counter. The CLK1 and CLK2 signals are generated by combining the signals of these frequencies. The timing chart is shown in Figure 4-6-51.



Figue Figure 4-6-51 CLK1/CLK2 Generation Timing

(5) VFO and DATA SEPARATOR

During DATA READ, the VFO is locked to the phase of the RAW DATA read from the disk. At other times, it is locked to the PLO output. The synchronizing principle is the same as that of the PLO. The output of the VFO is locked to the input at a frequency of twice that of one bit cell. The DATA SEPARATOR separates the DATA from the RAW DATA (MFM pulses) and converts it to NRZ READ DATA.

The VFO increases the loop gain of the system, to widen the pull-in range, and to shorten the pull-in time by using the LOCK TO DATA signals. Moreover, Read Gate goes true, for instance, in Gap 1 where all "0s" are written. The DATA WINDOW (signal 1FA or 1FB generated by counting down the output 2F of the VFO) is phase-adjusted using the Lock To Data signal so that the demodulated data is all "0".

Furthermore, TIME MARGIN measurements can be performed by changing the monostable multivibrator MS2. The block diagram and timing chart are given in Figure 4-6-52 and Figure 4-6-53.

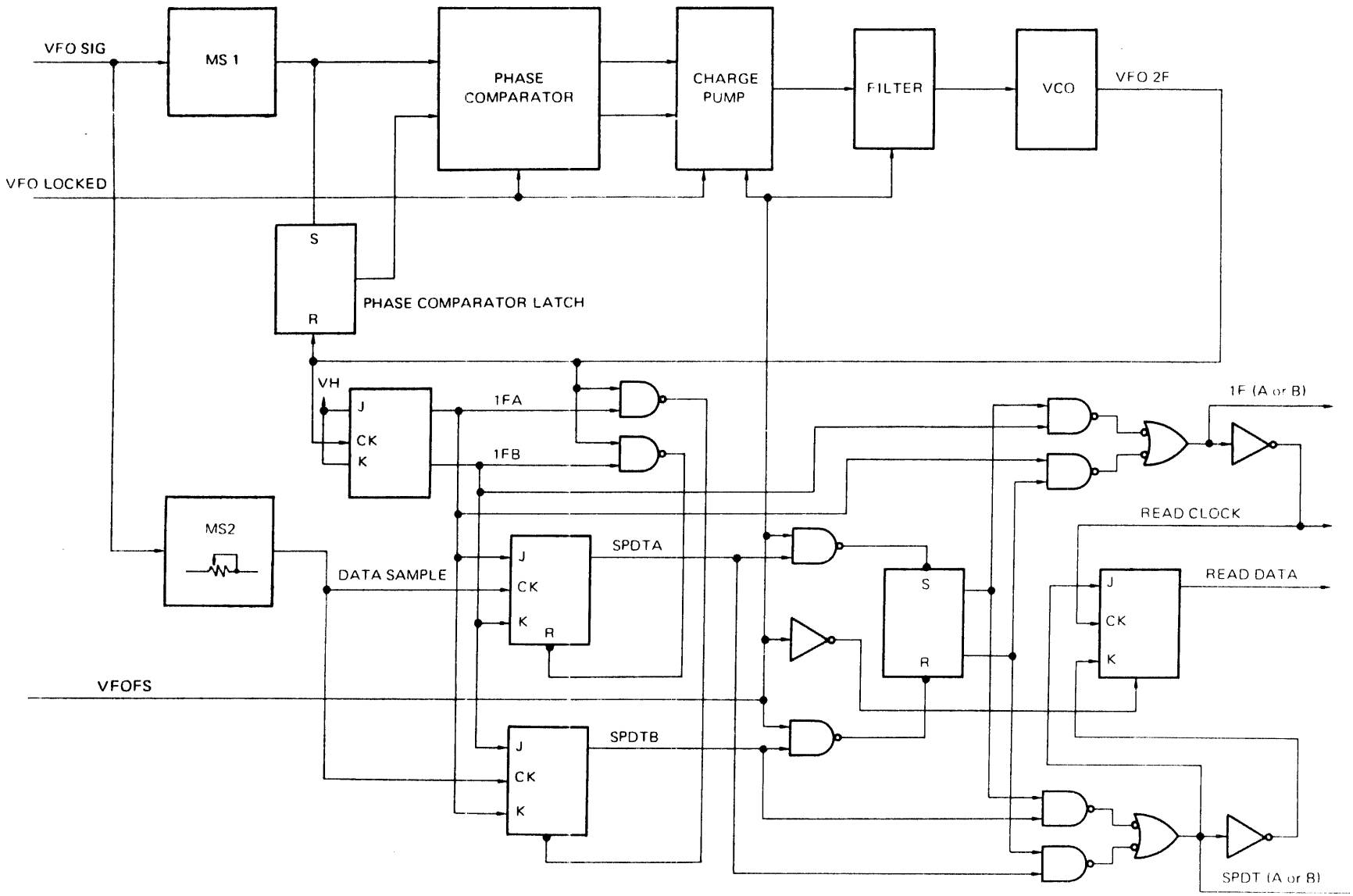


Figure 4-6-52 VFO and DATA SEPARATOR Block Diagram

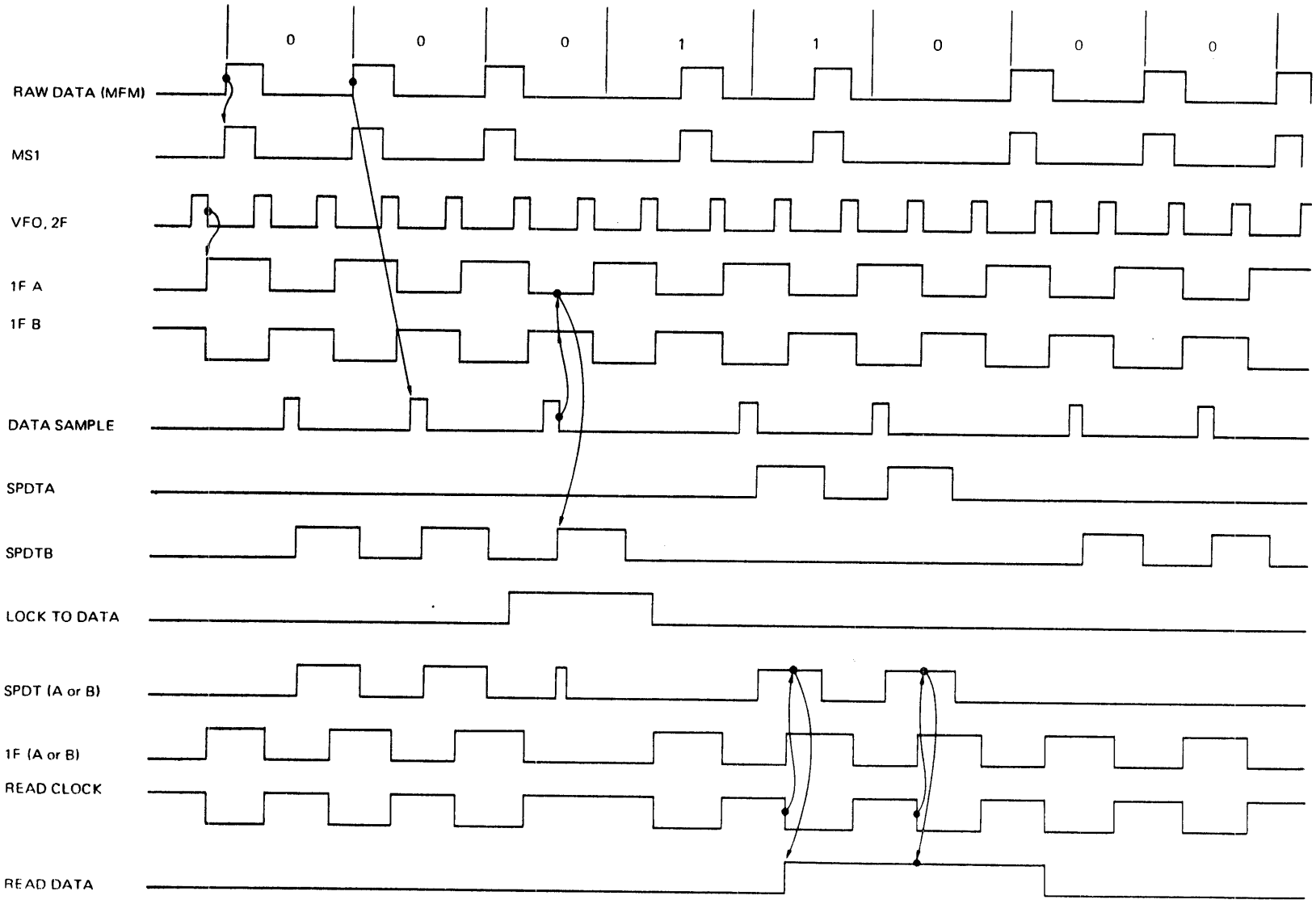


Figure 4-6-53 VFO and DATA SEPARATOR Timing Chart

(6) VFO Control

The VFO Control circuit controls the input to the VFO circuit, that is, the PLO output PLO1F or recovered read data, RAWDT, also generates VFO Fast Synchronization (VFOFS) for faster VFO synchronization with the input signal RAWDT or PLO1F.

In the start-up sequence, when the Start Pulse (STARTP) is applied to the Seek Control circuit, Initial Seek (INSK) is initiated and the heads move towards the servo zone. From the leading edge of INSK to the going false of IGB2 detect, PLO Fast Synchronization (PLOFS) is applied to the PLO II circuit on the VOFM PCB. PLOFS enables faster syncrhonization of the PLO circuit with 2B clock and also initiates the PLO counter.

The Initial Seek completion sets Linear Mode (LNMD), and also VFO Lock (VFOLK) to enable the synchronization of the VFO circuit. The leading edge of VFOLK triggers the VFO Fast Synchronization (VFOFS) one-shot (11.3 μs). VFOFS sets the PLO Latch so that the PLO output PLO1F is applied to the input of the circuit and also activates faster synchronization of the VFO circuit. When the heads are retracted to the Landing Zone, VFOLK is reset to disable the synchronization of the VFO circuit. The timing chart of Initial Seek VFO control is shown in Figure 4-6-54. When an RTZ command is issued to the unit, RTZ Enable (RTZE) is set and VFOLK is reset. The completion of an RTZ operation activates the LNMD signal, VFOLK and VFOFS signals. The timing chart of an RTZ VFO control is shown in Figure 4-6-55.

During a non-read operation, the VFO circuit synchronizes with the PLO output, PLO1F, and generates VFO clock (VFOCLK). In Hard Sector mode, at the beginning of a read operation, Read Gate is applied to the RG True Detect circuit after 4-bits and is clocked by the trailing edge of the 1-Byte clock, CLK1. Rise Read Gate (RRG) signal, which is an output of the RG True Detect circuit, is applied to a 3-Byte Shift Register and then its output presets Twelve on the Lock-To-Data counter to generate a 4-Byte Lock-To-Data (LDATA) signal. The LDATA signal is sent to the VFO Latch circuit on the VOFM PCB so that the VFO circuit synchronizes with RAWDT.

On the other hand, for Variable Soft Sector mode, the Rise AM Found (RAMF) signal sets the Lock To Data Counter to generate the LDATA signal. Refer to Figure 4-6-54. At the end of Read Gate, a 1-Byte Fall Read Gate (FRG) is detected and applied to the Lock To PLO Counter to generate a 4-Byte Lock To PLO (LPLO) signal. The LPLO signal is sent to the VFO Latch circuit on the VOFM PCB so that the VFO Circuit synchronizes with PLO1F.

LDATA and LPLO signals are converted into the VFO Fast Synchronize (VFOFS) signal and applied to the VFO Filter circuit to decrease the time constant of the Filter. This promotes faster synchronization of the VFO circuit with RAWDT or PLO1F.

The VFO control block diagram and timing chart are shown in Figure 4-6-56 and 4-6-57 respectively.

Figure 4-6-54 VFO Control During Initial Seek/Retract Operation

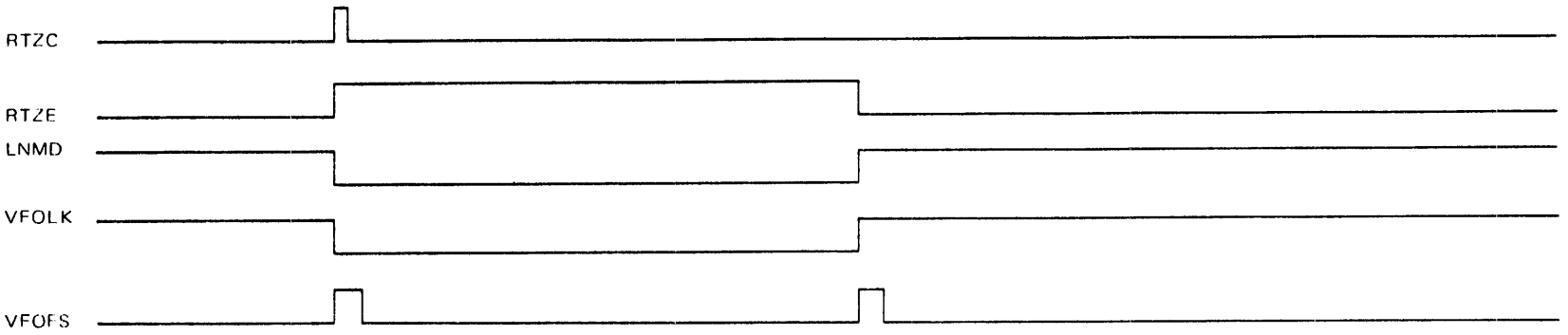
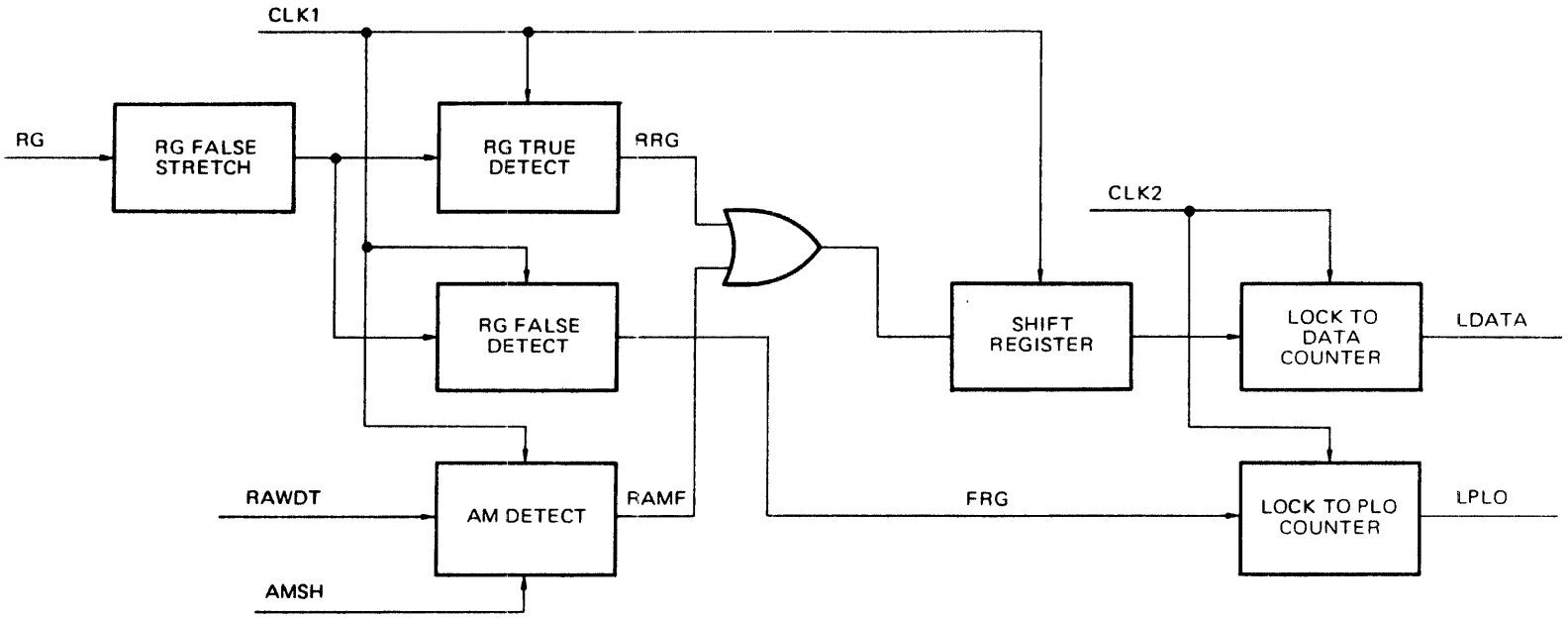


Figure 4-6-55 VFO Control During RTZ Operation



Note: All functions are included on the CQFM/CMKM PCB.

Figure 4-6-56 VFO Control Block Diagram

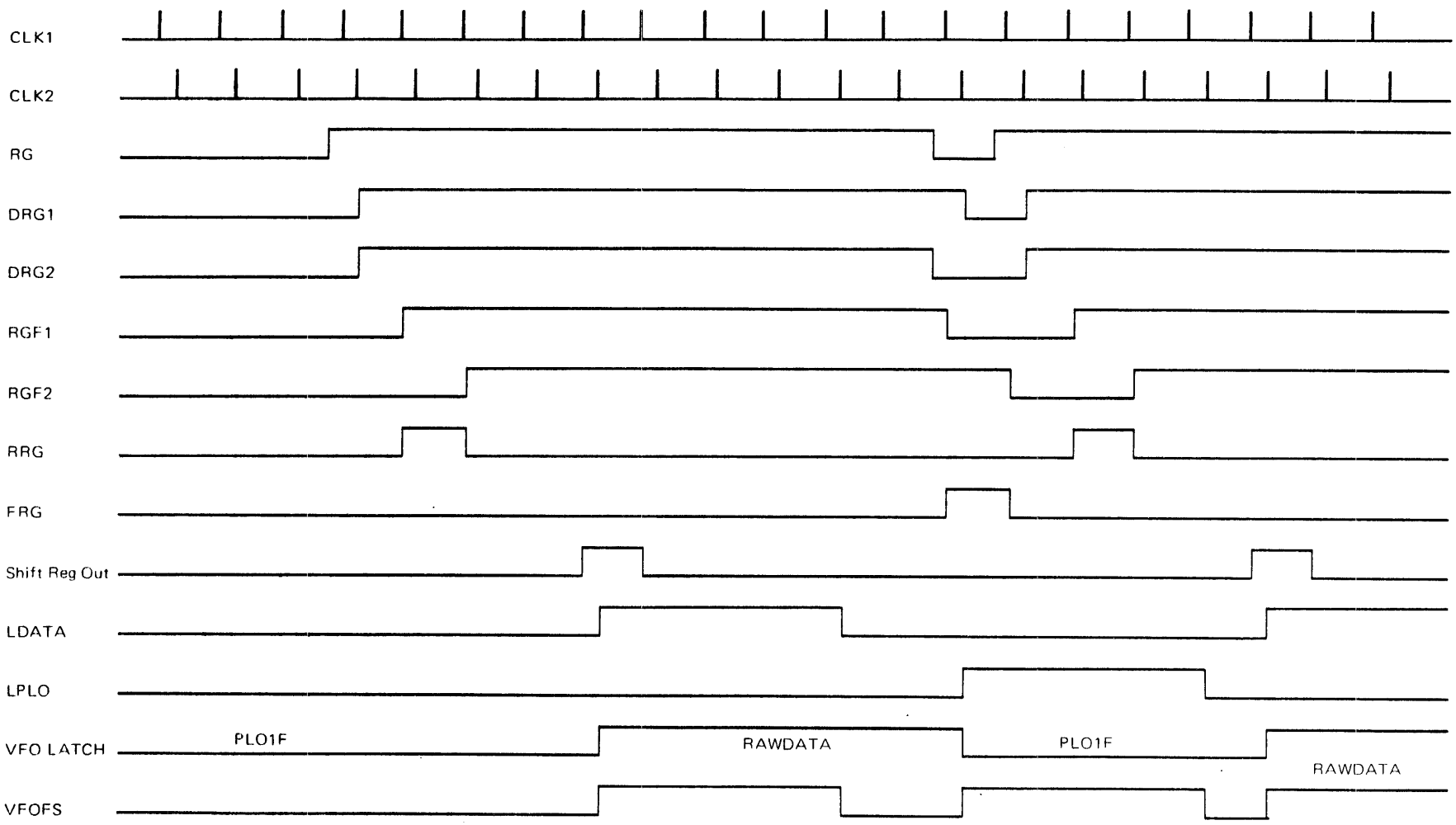


Figure 4-6-57 VFO Control During Read/Write Operation

4.6.8 Fault and Error Detection

4.6.8.1 General

The faults and errors are interpreted by the unit. These conditions are sent to the control unit and displayed on the Maintenance Aid LED's on the PCB chassis.

4.6.8.2 Device Check Register

If an error sets the Device Check (Fault) Register on the unit, the Device Check line is enabled to the control unit, the Maintenance Aid Display is lit by Tag Decode 1 and the write circuit is inhibited. Each register output is designated by the following six statuses:

(1) Control Check 1 (Status 0)
- (RG+WG) · ($\overline{\text{URDY}}$)
- AHDSL · UNSQ · (RG+WG)
- (OFACT+AHTAG1) · (UNSQ+$\overline{\text{URDY}}$+SKERR)
- $\overline{\text{URDY}}$ · RTZ

(2) Control Check 2 (Status 1)
- WG · (RG+OFACT+SKERR)

(3) Read/Write Check 1 (Status 2)
- AHDSL · $\overline{\text{ONCYL}}$· WG
- VCMHT (VCM Over-heat)
- INTMOT (Initial Seek Time Out)

(4) Read/Write Check 2 (Status 3)
- WG · $\overline{\text{WECHO}}$+$\overline{\text{WG}}$ · WECHO

(5) Read/Write Check 3 (Status 4)
- WG · FPTD

(6) Read/Write Check 4 (Status 5)
- (WG+RG) · MLTSL

The Device Check status is cleared by any of the following:
- Check clear key on the optional operator panel
- Check clear key on the PCB chassis
- Device check clear signal from the control unit.

4.6.8.3 Seek Check Latch

If a seek malfunction has occured in the unit, the malfunction will set the Seek Check Latch, enable the Seek Error (SKERR) line to the control unit, and light the Maintenance Aid Dispay by Tag Decode 3. Each latch output is designated by one of the following six statuses:

(1) Seek Check 0 (Status 0)
- Time-out in Direct or RTZ seek

(2) Seek Check 1 (Status 1)
- Any Guard Band in Direct Seek

(3) Seek Check 2 (Status 2)
- Any Guard Band in Linear mode

(4) Seek Check 3 (Status 3)
- OGB in Go To Zero mode

(5) Seek Check 4 (Status 4)
- Linear mode is lost during Settling Time
- Over track-crossing-pulse in Settling Time

(6) Seek Check 5 (Status 5)
- Illegal cylinder address.

Section 6

Maintenance

6. MAINTENANCE

6.1 INTRODUCTION

This section covers on maintenance of the unit, and is divided into General Precaution, Preventive Maintenance, Maintenance Equipment, Parts Replacement and Adjustment, and Electrical Checks and Adjustment items.

6.2 GENERAL PRECAUTIONS

6.2.1 Power ON/OFF

(1) Check the operating condition of the device before turning the power on and off.
(2) Before turning the power on after maintenance, check that all the printed-circuit boards are mounted in the correct position.

6.2.2 PCB Assembly and Connector Removal

(1) Always turn the power off before removing and inserting printed-circuit boards and connectors.
(2) Always insert the printed-circuit boards along the printed-circuit board guide.

6.2.3 Parts Replacement

(1) Use screwdrivers, wrenches, and other tools matched to the size of the screws and bolts.
(2) Do not leave removed screws in the device.
(3) Tighten all the screws securely.

6.2.4 DE Replacement

(1) A Disk Enclosure (DE) is sensitive to shock. Be careful when handling or replacing the DE. Do not apply a shock.
(2) Use the specified packing box for spare DE. When returning the replaced DE, put the DE into the specified packing box used for transporting.

6.2.5 Dual Port Switches

(1) Turn the switches to the desired position according to system configuration.
(2) After maintenance, turn the maintenance switch to the Normal A/B (NRA/NRB) position.

6.2.6 Others

(1) Use test equipment that has been correctly calibrated.
(2) Always record the data and its processing for later reference when trouble occurs.

6.3 MAINTENANCE TOOLS AND EQUIPMENT

Table 6-3-1 Maintenance Tools and Equipment

Tool and equipment	Model
Oscilloscope	TEKTRONIC 475, or equivalent
Oscilloscope probe (X10)	TEKTRONIX P6053B, or equivalent
Digital multimeter	
Extender	B16B-3190-0010A
Screwdriver	
Hexagon Wrench	
Wrench or crescent wrench	

6.4 PREVENTIVE MAINTENANCE

No special preventive maintenance is necessary.

6.5 MECHANICAL PARTS REPLACEMENT AND ADJUSTMENT

When replacing mechanical parts, always lock the spindle and actuator.

6.5.1 Disk Enclosure

The disk enclosure (DE) is attached to the sub-frame with three nuts. To replace the DE, proceed as follows:

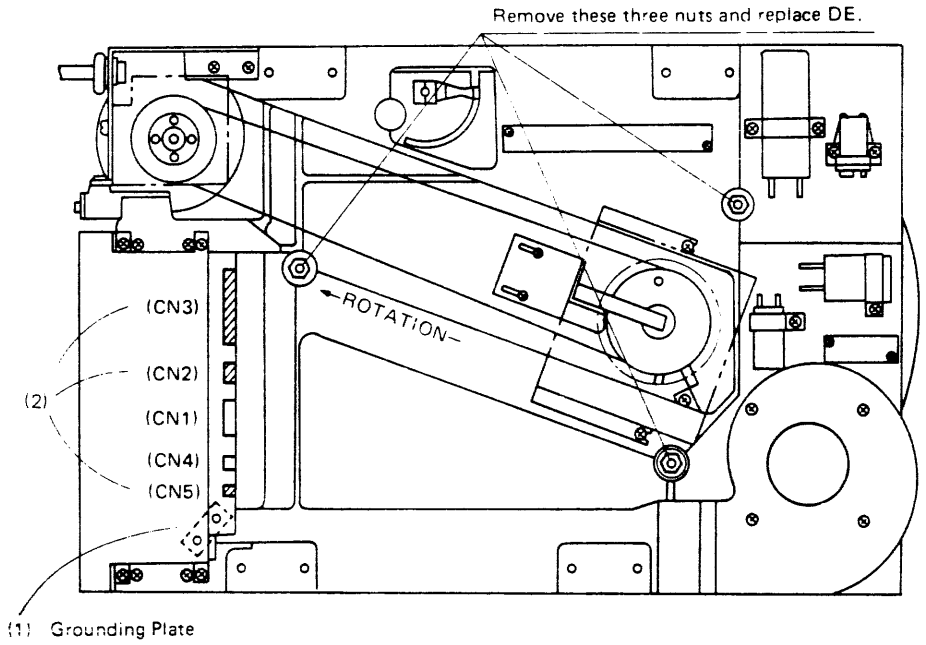


Figure 6-5-1 Disk Enclosure Replacement

(A) Removal

(1) Remove grounding plate between gate shelf and sub-shelf of unit. (Top side)
(2) Disconnect wiring (CN2, CN3 and CN5) from the gate shelf.
(3) Lock actuator. (Refer to 3.4.4)
(4) Remove belt in accordance with 6.5.4.
(5) Remove three nuts shown in Fig. 6-5-1 from rear of sub-frame.
(6) Remove DE by lifting it slowly, being careful not to damage any of the wires.

Note: Be careful not to lose disk enclosure isolating bushing (polyacetal: white) threaded part when replacing disk enclosure.

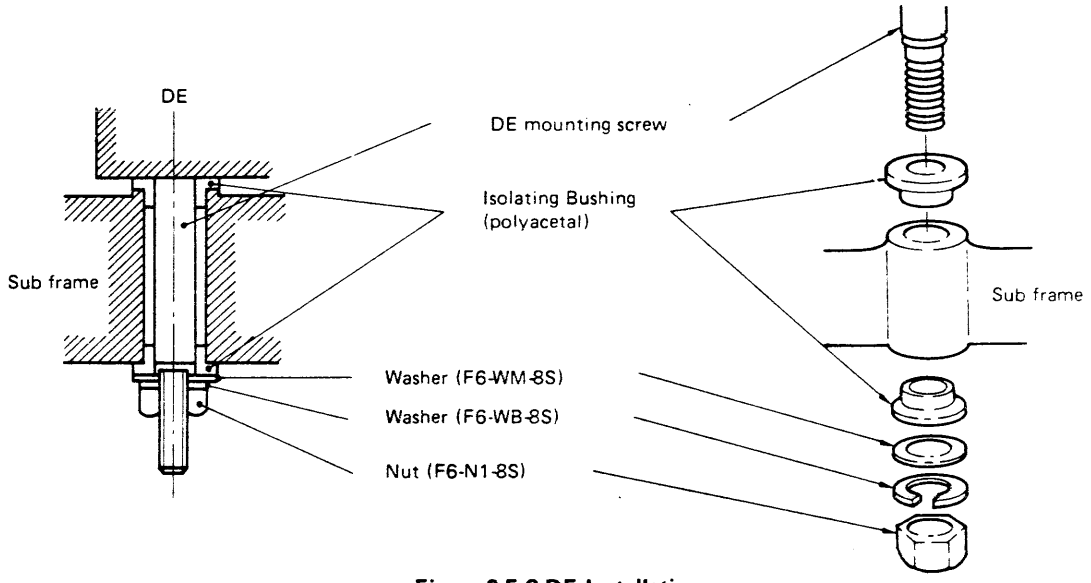


Figure 6-5-2 DE Installation

(B) Installation

(1) Fasten Disk Enclosure to the sub-frame as illustrated in Fig. 6-5-2.
(2) Install belt in accordance with paragraph 6.5.4.
(3) Unlock acutator (See paragraph 3.4.4).
(4) Fasten connectors (CN2, CN3, CN5) coming from disk enclosure.
(5) Install grounding plate between gate shelf and sub-shelf of the unit.

Note: After DE replacement, the adjustments of SDIM PCB assembly should be required as described in 6.6.3.1 to 6.6.3.3.

6.5.2 Spindle Drive Motor

The spindle drive motor is fastened to the sub-frame.
To replace this motor, proceed as follows:

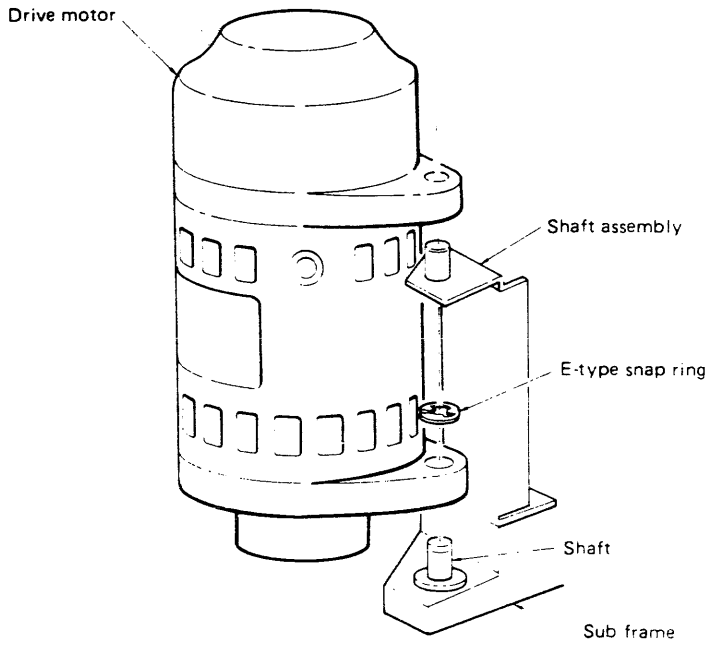


Figure 6-5-3 Disk Drive Motor Replacement

(A) Removal
(1) Disconnect motor cable from TRM2.
(2) Remove belt in accordance with paragraph 6.5.4.
(3) Remove E-type snap ring shown in Figure 6-5-3, and pull out the motor from shaft.

(B) Installation
(1) Install motor, and fasten it to shaft with E-type snap ring shown in Figure 6.5.3.
(2) Install belt in accordance with paragraph 6.5.4.
(3) Connect motor cable by terminal numbers of TRM2.

6.5.3 Motor Pully Replacement

To replace the motor pulley and change from 60Hz to 50Hz, proceed as follows: Refer to Figure 6-5-4.

(A) Removing motor pulley
(1) Remove belt in accordance with paragraph 6.5.4.
(2) Loosen and remove two screws A.
(3) Insert removed screws A into screw holes in holder, and remove the holder by tightening screws alternately.
(4) After removing holder, remove pulley from motor shaft. See Figure 6-5-4.

(B) Installing motor pulley
(1) Check line frequency. Large diameter of pulley is for 50Hz and small diameter is for 60Hz. Refer to Pulley Label.
(2) Insert the pulley onto shaft with specified frequency side on top, and push the pulley until it butts against "A" surface of shaft.
(3) Then insert holder into taper of pulley (opposite side of specified frequency), and align screw holes of pulley with holes of holder.
(4) Pass screws A through holes of holder and fasten the pulley to motor shaft by tightening screw "A" alternately.
(5) Insert belt in accordance with paragraph 6.5.4. Belt must be at center of pulley when it is rotating.

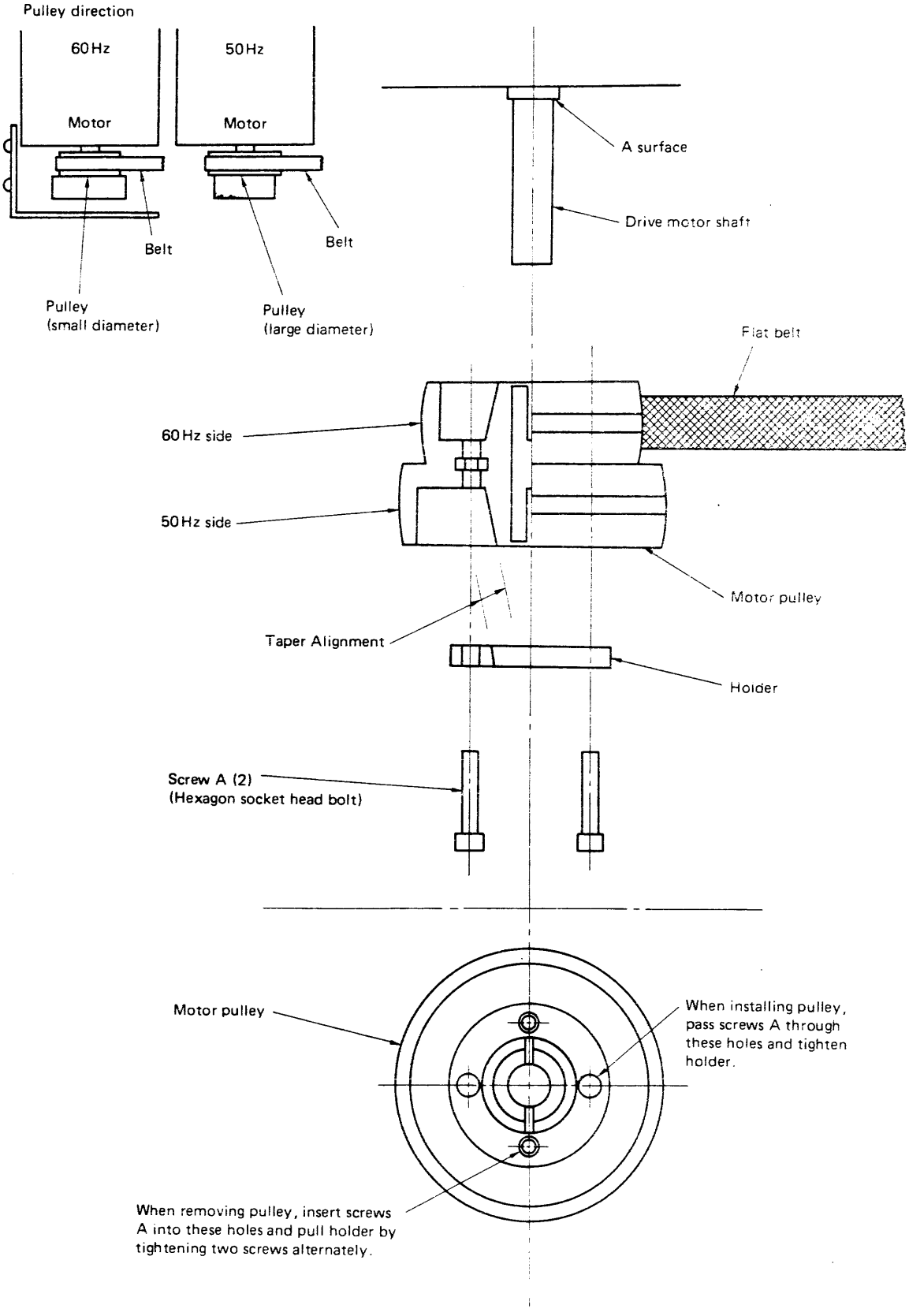


Figure 6-5-4 Motor Pulley Replacement

(C) Readjustment of belt tension

After changing the motor pulley to meet a different power line frequency, make it a rule to readjust belt tension.

Tension adjustment label is located beside the side of the slider (see Figure 6-5-5). Adjust belt tension with screw "D" so that the rear edge of the slider is aligned to proper reference line of tension adjustment label.

According to power line frequency and type of device installation, there are four setting positions (reference lines). The relation between installation position and line frequency are shown on pulley label put on motor cover. Pulley label is shown in Figure 6-5-6.

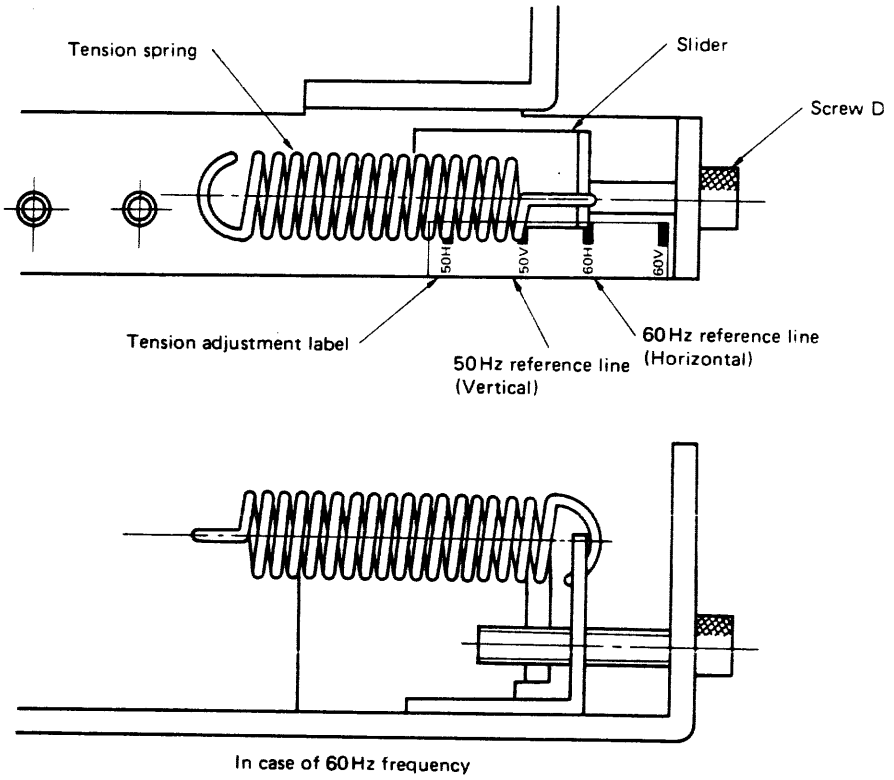
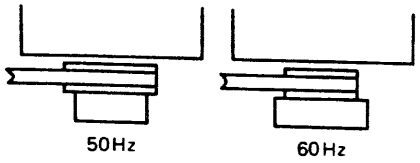


Figure 6-5-5 Belt Tension Adjustment



TENSION MARK

50H 60H	DEVICE IS INSTALLED HORIZONTALLY.
50V 60V	DEVICE IS INSTALLED VERTICALLY.

Figure 6-5-6 Pulley Label

6.5.4 Belt Replacement

To replace belt proceed as follows:

(A) Removing belt

(1) Loosen screws "B" (2) and remove screws "C" (2) shown in Figure 6.5.7, and remove spindle cover and motor cover.

(2) Lock spindle (see paragraph 3.4.3).

(3) Loosen belt by loosening screw "D" of Figure 6.5.6 with a hexagon wrench, and remove belt.

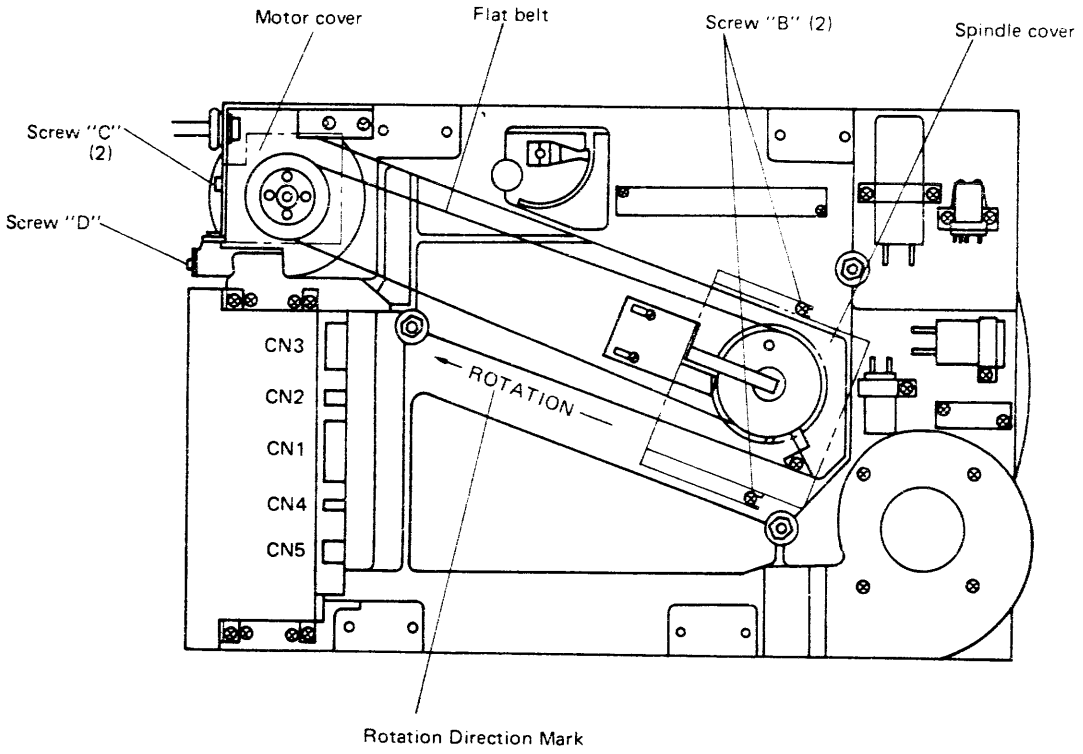


Figure 6-5-7 Belt Replacement

(B) Installing belt

(1) Position the belt, and adjust belt tension. Adjust belt tension with screw "D" so that the rear of slider is aligned to the correct line on the tension adjustment label as shown in Figure 6-5-5.

(2) Unlock spindle (see paragraph 3.4.3).

(3) Adjust spindle grounding in accordance with paragraph 6.5.5.

(4) Install motor cover and spindle cover.

6.5.5 Spindle Grounding Plate (Anti-static Brush)

To replace and adjust spindle grounding plate proceed as follows (see Figure 6-5-7).

(A) Replacement

Spindle grounding plate is replaced by removing screw "E" (2).

(B) Installation and adjustment

Confirm that the center of the spindle shaft is at the center of the spindle grounding contact, and tighten spindle grounding plate.

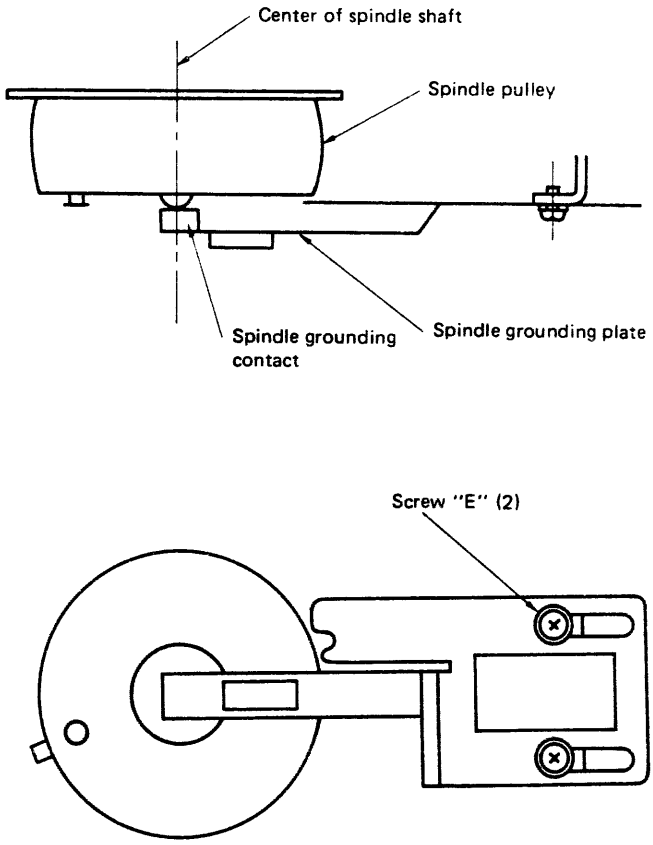


Figure 6-5-8 Spindle Grounding Plate Replacement and Adjustment

6.5.6 Speed Transducer

The speed transducer is used to detect the speed by detecting the projection attached to the spindle pulley.

(A) Removal

(1) Remove disk enclosure as described in paragraph 6.5.1.

(2) Loosen screw "F" (2) shown in Figure 6-5-9, and remove holder plate. At this time, also remove the speed transducer assembly.

(3) Loosen screw "G" (2), and replace the speed transducer assembly.

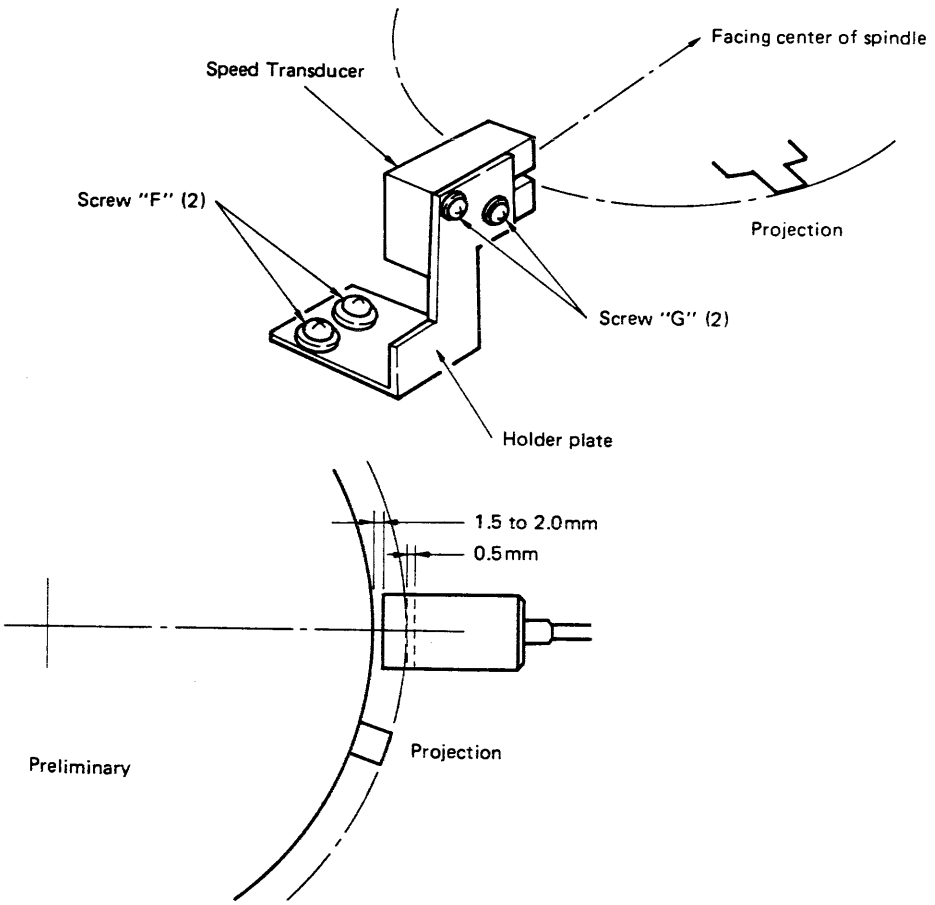


Figure 6-5-9 Speed Transducer

(B) Installation

(1) When installing the speed transducer, adjust so that it does not touch the pulley and projection. Refer to Figure 6-5-9.
Moreover, center of the speed transducer must be facing center of spindle.
After adjustment, retighten screws.

(2) Fasten Disk Enclosure to sub-frame as described in paragraph 6.5.1.

(3) Rotate the spindle pulley by hand in proper direction and ensure that projection of the pulley does not contact the speed transducer.
Also ensure that there is a gap (about 0.5mm) between the speed transducer and belt when the belt is shifted up to the speed transducer.

6.5.7 Blower Replacement

The blower is installed on the bottom, front of the sub-frame, and blows air through a duct in the sub-frame to cool the sub-frame, PCB assemblies and motor.

To replace the blower, proceed as follows:

(A) Removal

(1) Disconnect blower cable from TRM3.

(2) Remove screws "H" (4), and remove blower.

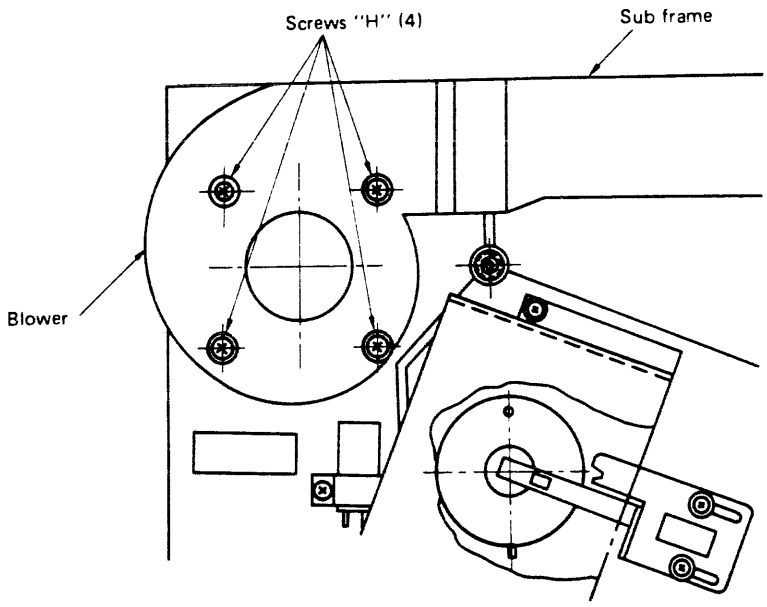


Figure 6-5-10 Blower Replacement

(B) Installation
(1) When installing blower, be sure that outlet of blower is pushed tightly against duct so that there is no air leakage.
(2) Connect blower cable by matching numbers on wires to terminal numbers of TRM3.

6.5.8 Brake Relay

Replace relay by removing holder. Remove holder by pulling it in directions of arrows in Figure 6-5-11.

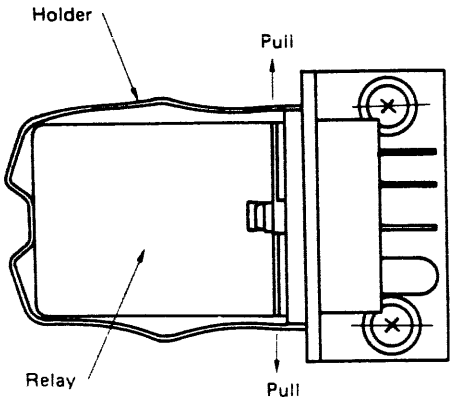


Figure 6-5-11 Replay Replacement

6.5.9 Dual Port Option

When the Dual Port option is replaced, perform the reverse procedure as described in Figure 3-4-9.

When the Cross-Call B (XCBM) PCB assembly is replaced, perform the following procedure:

(1) Loosen two screws securing the cable holder, and remove the cable holder.
(2) Disconnect the interface cables (OM1B, OM2B and OM3B) connecting to channel B.
(3) Disconnect cables on connectors CN32 and CN34 from XCBM PCB assembly.
(4) Remove the cover by loosening the three screws.
(5) Disconnect a cable on connector CN31 connecting CQFM PCB assembly.
(6) Remove XCBM PCB assembly by removing the four screws.
(7) Reposition the spare XCBM PCB assembly by reverse procedure items (1) to (6). Refer to Figure 6-5-12.

After replacement, fully check the switches for their modes and cables for their connections.

Caution: When connecting the 10-pin cable to CN32, see that this cable does not interfere with FPT (File Protect) switch function.

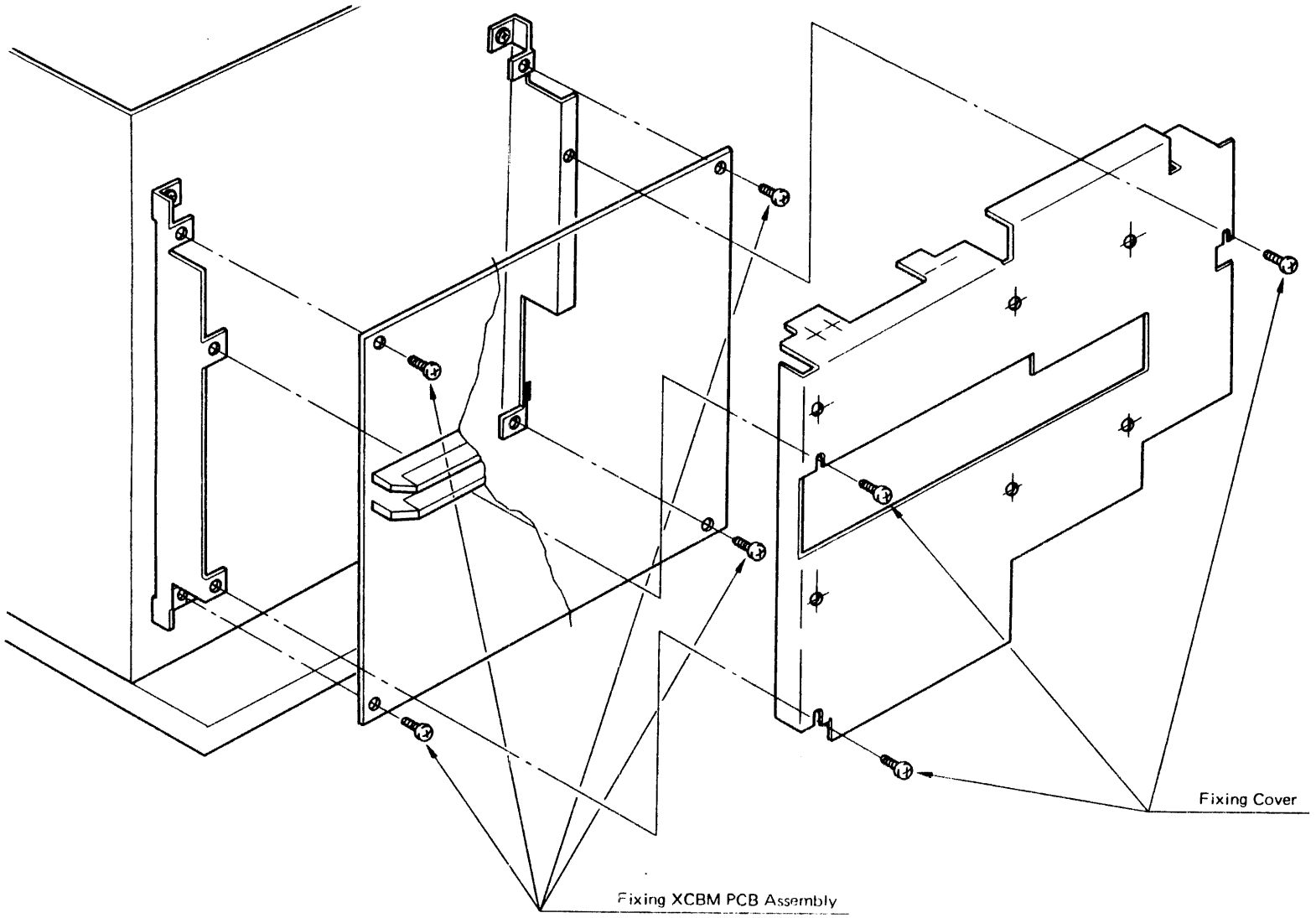


Figure 6-5-12 XCBM PCB Assembly Replacement

6.6 PCB ASSEMBLY REPLACEMENT/ADJUSTMENT

6.6.1 PCB Assembly Arrangement

The following Printed Circuit Board assemblies are mounted in the PCB chassis. To remove these PCB's, remove the top cover of the PCB chassis by loosening to screws, and then pull the levers on the PCB assemblies.

The PCB arrangement of the FDU M228X is shown in Table 6-6-1.

Table 6-6-1 PCB Arrangement

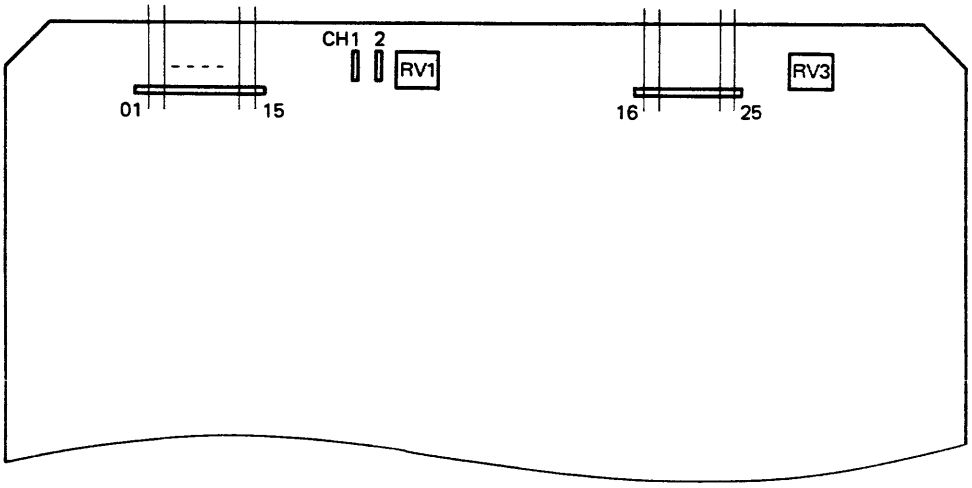
	M2282 M2280 M2283 M2284	M2286 M2289 M2287 M2288	Function
PCB Chassis	RQWM	RQVM	Read/Write Circuit
PCB Chassis	SDIM		Servo Circuit
	CMIM		Seek Control
	VOFM		PLO/VFO
	CQFM/CMKM		Interface Control

6.6.2 Test Point Arrangement on the PCB

Each PCB assembly is provided with test points and potentiometers to check and/or adjust the circuit functions.

(1) RQVM/RQWM PCB

The test points and potentiometers are located on the RQVM/RQWM PCB assembly as shown in Fig. 6-6-1.



Note: No Adjustments are required when the PCB is replaced.

Figure 6-6-1 RQVM/RQWM PCB Test Points

Table 6-6-2 RQVM/RQWM PCB Test Points

TP No.	Abbreviation	Signal Name	Schematic Page Code
1	*DIGLT	Diag Latch	EA1
2	Not Used	–	–
3	PLSH 1	Pulse Shaper 1	EA2
4	PLSH 2	Pulse Shaper 2	EA2
5	SMPCK	Sample Clock	EA2
6	RAWDT 1	Raw Data 1	EA2
7	RAWDT 2	Raw Data 2	EA2
8	INTLT 1	Integrator Latch 1	EA2
9	INTLT 2	Integrator Latch 2	EA2
10	DFROT 1	Differentiator Output 1	EA2
11	DFROT 2	Differentiator Output 2	EA2
12	AGCOT 1	AGC Output 1	EA2
13	AGCOT 2	AGC Output 2	EA2
14 (CH1)	PROT 1	Pre-Amp. Output 1	EA2
15 (CH2)	PROT 2	Pre-Amp. Output 2	EA2
16	MLTSL	Multi-Selected	EA3
17	PWRDY	Power Ready	EA3
18	AHWC A	AHD Write Current A	EA1
19	AHWC B	AHD Write Current B	EA1
20	*UNSF	Unsafe	EA1
21	Not Used	–	–
22	FHPRT	FHD Protect	EB1
23	FHWC A	FHD Write Current A	EB1
24	FHWC B	FHD Write Current B	EB1
25	*SQCHG	Squelch Gate	EA2

The RQVM/RQWM PCB assembly is provided with two/one potentiometers, however, no adjustments are required when the PCB is replaced. Each potentiometer function is shown in Table 6-6-3.

Table 6-6-3 RQVM/RQWM Potentiometer Function

Pot No.	Function/Adjustment	Reference TP
RV1	Access Head Write Current	TP18/TP19
*RV3	Fixed Head Write Current	TP22/TP23/TP24

* This potentiometer is for only, RQVM, however, is not adjustable in field.

(2) SDIM PCB

The test points, potentiometers, and switches are located on SDIM PCB assembly as shown in Fig. 6-6-2.

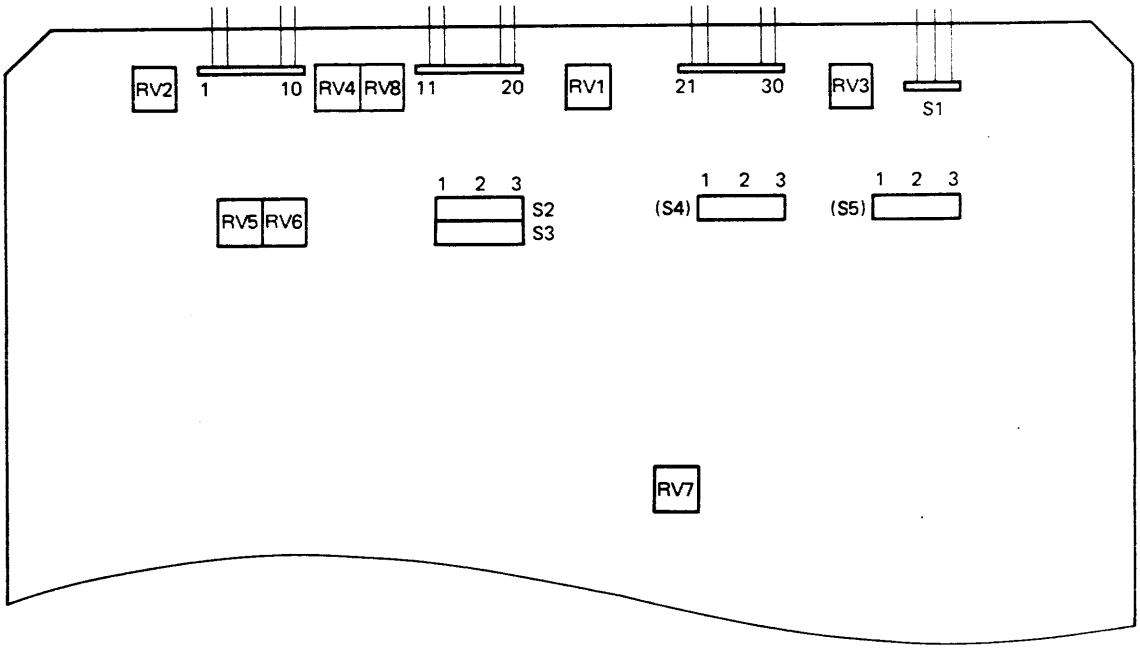


Figure 6-6-2 SDIM PCB Test Points

Each test point function is shown in Table 6-6-4.

Table 6-6-4 SDIM PCB Test Points

TP No.	Abbreviation	Signal Name	Schematic Page Code
1	SERVO	Servo Signal	CA1
2	*ODG	Odd Gate	CA3
3	*EVG	Even Gate	CA3
4	AGC	AGC Control	CA1
5	ODP	Odd Peak	CA3
6	EVP	Even Peak	CA3
7	+POS	Position Signal	CA3
8	VCX1	Control Voltage 1	CA2
9	Not Used	–	–
10	SVPWD	Servo Pulse Window	CA1
11	SVSLT	Servo Slice Out	CA1
12	SVPL	Servo Pulse	CA1
13	PLOSS	PLO Single Shot	CA1
14	PLOLT	PLO Latch	CA2
15	1/8 F	1/8 Frequency	CA2
16	EIX	Even Index	CA2
17	TRFL	Track Follow	CB1
18	TXPL	Track Crossing Pulse	CB1
19	DRLM	Drive Linear Motor	CB1
20	FWDD	Forward Drive	CB1
21	CMAG	Current Magnitude	CB2

Table 6-6-4 SDIM PCB Test Points (Continued)

TP No.	Abbreviation	Signal Name	Schematic Page Code
22	PER	Position Error	CB2
23	FUNC	Function	CB3
24	VEL	Velocity	CB2
25	SMTH	Smoother	CB2
26	DA	DA Convertor	CB3
27	TVEL	Tach Velocity	CB2
28	–CSNS	Current Sense	CC1
29	VER	Velocity Error	CB3
30	PADR	Power Amp Drive	CB3

The SDIM PCB is provided with eight potentiometers and five selecting switches, however, only the three potentiometers (RV1, RV2 and RV4) must be adjusted when the PCB is replaced.

The potentiometer and switch functions are shown in Table 6-6-5 and 6-6-6.

Table 6-6-5 SDIM Potentiometer Function

Pot No.	Function/Adjustment	Reference TP/S
RV1	Positioning Time*	TP19
RV2	Position Signal Gain*	TP7
RV3	Function Offset	TP23
RV4	Over-shoot*	TP24
RV5	PLO Free Frequency	TP15, S2, S3
RV6	PLO Phase	TP13
RV7	DA Output	TP26
RV8	Servo Pulse Window	TP10

* The potentiometer RV1, RV2 and RV4 require adjustment when the SDIM PCB is replaced.

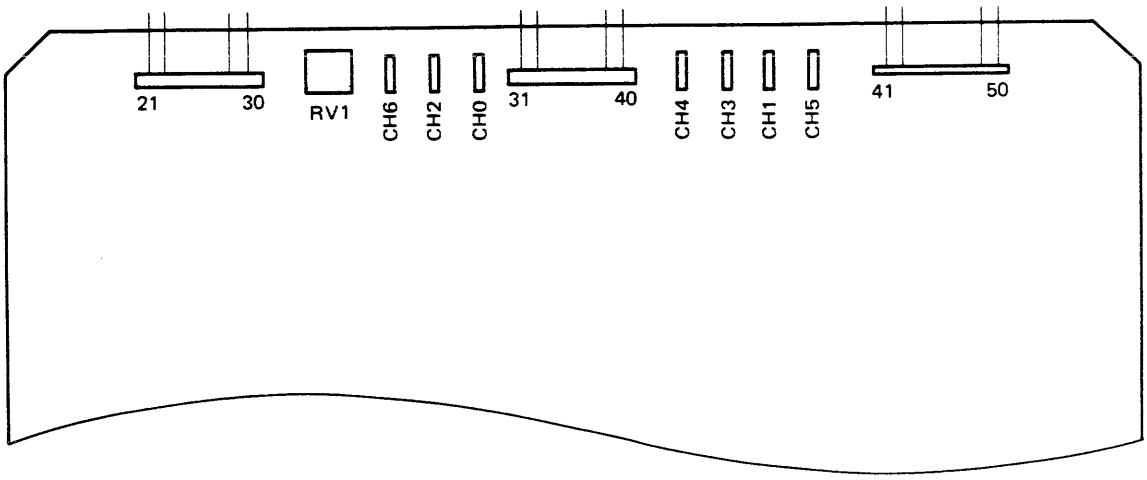
Table 6-6-6 SDIM Switch Function

Switch No.	Function	Reference TP
S1	Power Amp. Drive Cut	None
S2, S3	VCO Select	TP15

Note: S4 and S5 functions are not used.

(3) CMIM PCB

The test points, check terminals and a potentiometer are located on CMIM PCB assembly as shown in Fig. 6-6-3.



Note: No adjustments are required when the CMIM PCB assembly is replaced.

Figure 6-6-3 CMIM PCB Test Points

Each test point function is shown in Table 6-6-7 and 6-6-8.

Table 6-6-7 CMIM Check Terminals

CH No.	Abbreviation	Signal Name	Schematic Page Code
0	GND	Ground	–
1	VFOFS	VFO Fast Sync	BC1
2	STL 1	Settling 1	BE1
3	STL 2	Settling 2	BE1
4	STL 3	Settling 3	BE1
5	OVCYTM	Over Cylinder Timer	BE2
6	GBTM	Guard Band Timer	BE2

Table 6-6-8 CMIM Test Points

TP No.	Abbreviation	Signal Name	Schematic Page Code
21	GND	–	–
22	OGB	Outer Guard Band	BG1
23	IGB 1	Inner Guard Band 1	BG1
24	IGB 2	Inner Guard Band 2	BG1
25	–	–	–
26	SKEND	Seek End	BE2
27	ONCYL	On Cylinder	BE2
28	URDY	Unit Ready	BE2
29	SKERR	Seek Error	BE2
30	SKC	Seek Complete	BE1
31	GND	–	–
32	SUBEN	Sub Enable	BD4
33	EVEN	Even	BD4
34	PSDR	Position Drive	BD4
35	LNMD	Linear Mode	BD4
36	–	–	–

Table 6-6-8 CMIM Test Points (Continued)

TP No.	Abbreviation	Signal Name	Schematic Page Code
37	DRLM	Drive Linear Motor	BD4
38	LSPD	Low Speed	BD4
39	FWDD	Forward Drive	BD3
40	*OVTXPL	Over Track Crossing	BD2
41	GND	–	–
42	TMOTP	Time Out Pulse	BD2
43	RTRM	Retract Mode	BD1
44	SEKM	Seek Mode	BD1
45	GTZM	Go To Zero Mode	BD1
46	*PLO 1B	PLO 1 Byte Clock	BD1
47	–	–	–
48	*OFACT	Offset Active	BB1
49	AHDSL	Access Head Select	BB1
50	USLD	Unit Selected	BB1

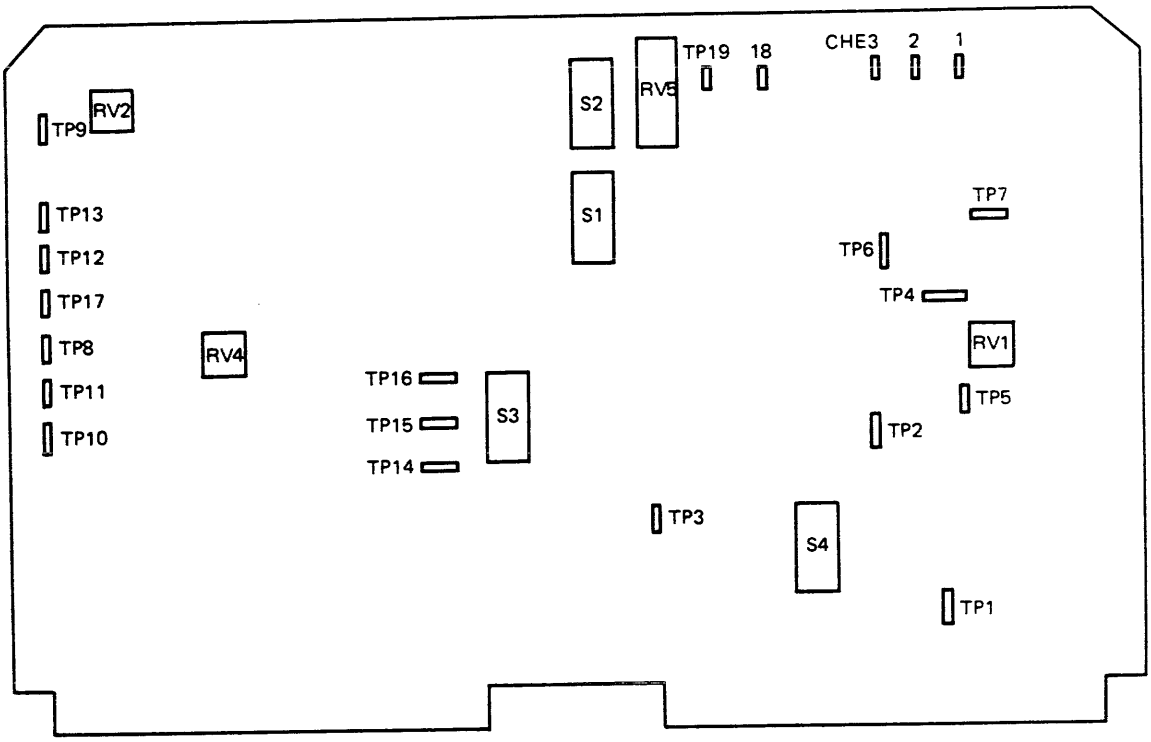
The CMIM PCB is provided with a potentiometer (RV 1), however, no adjustment is required when the PCB is replaced. The potentiometer function is shown in Table 6-6-9.

Table 6-6-9 CMIM Potentiometer Function

Pot No.	Function/Adjustment	Reference CH
RV 1	Settling Time 1	CH2

(4) VOFM PCB

The check terminals, switches, and potentiometers are located on the VOFM PCB assembly as shown in Fig. 6-6-4.



Note: S1 and S2 must be selected when the PCB is replaced.

Figure 6-6-4 VOFM PCB Test Points

Each test point function is shown in Table 6-6-10.

Table 6-6-10 VOFM Check Terminals

TP No.	Abbreviation	Signal Name	Schematic Page Code
1	VFOSS	VFO Single Shot	DD1
2	VFODIF	VFO Difference	DD1
3	TRDT	Trigger Data	DD1
4	VC VFO	Control Voltage VFO	DD2
5	VCOT	VCO Output	DD2
6	FLTCNT	Filter Control	DD2
7	FLTSQH	Filter Squelch	DD2
8	PLOSS1	PLO Single Shot 1	DC1
9	*1/16 FP	1/16 F Pulse	DC1
10	DLTP	Delta Positive	DC2
11	DLTN	Delta Negative	DC2
12	FLTOT	Filtered Out	DC2
13	VC PLO	Control Voltage PLO	DC2
14	2F EY	2F Early	DB1
15	2F OT	2F Ontime	DB1
16	2F LT	2F Late	DB1
17	PLOSS 2	PLO Single Shot 2	DC1
18	SCT	Sector	DA1
19	INX	Index	DA1

Table 6-6-10 VOFM Check Terminals (Continued)

No.	Abbreviation	Signal Name	Schematic Page Code
CHE 1	DTSMP	Data Sample	DE1
CHE 2	DTWD	Data Window	DE1
CHE 3	VC VFO	Control Voltage VFO	DD2

The VOFM PCB assembly is provided with potentiometers and switches, however, no adjustments except SW1 and SW2 are required when the PCB is replaced. These functions are shown in Table 6-6-11.

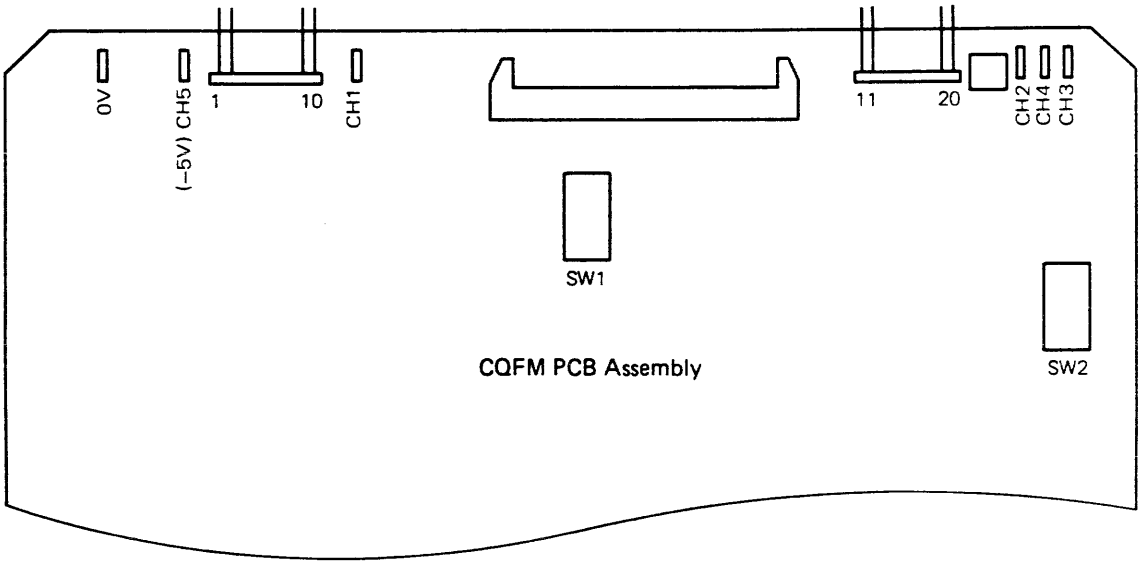
Table 6-6-11 VOFM Potentiometer/Switch Function

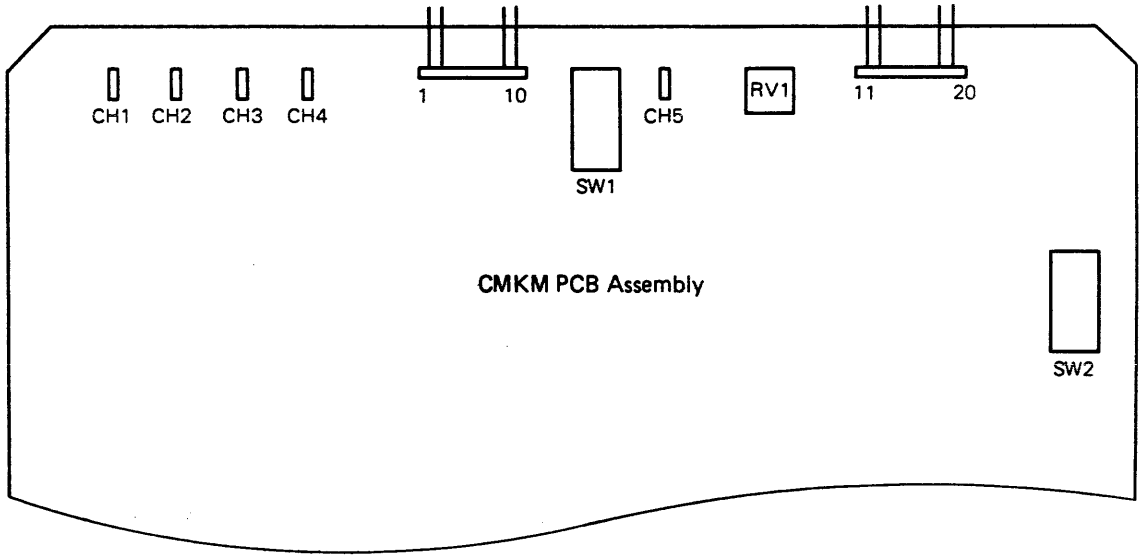
No.	Function/Adjustment	Reference TP
RV1	VFO Frequency	TP4
RV2	PLO Frequency	TP13
RV4	PLO SS2	TP17
RV5	Time Margin Measurement	CHE1/CHE2
S1	Sector Counting 1	TP18/TP19
S2	Sector Counting 2	TP18/TP19
S3	VFO Single Shot	TP1
S4	Write Compensation	TP14/TP15/TP16

(5) CQFM/CMKM PCB

CQFM PCB assembly is for an interface control logic to support dual port or single port function, and CMKM PCB assembly is only to support single port function.

The test points and potentiometers are located on the CQFM/CMKM PCB assembly are shown in Figure 6-6-5. Each test point function is shown in Table 6-6-12.





Note: No potentiometer adjustment is required when the PCB is replaced, however, the switch selecting should be performed to meet the customer's configuration.

Figure 6-6-5 CQFM/CMKM PCB Test Points

Table 6-6-12 CQFM/CMKM Test Points

No.	Abbreviation	Signal Name	Schematic Page Code
TP1	GND	–	–
TP2	LPLO	Lock to PLO	AF1
TP3	LDATA	Lock to Data	AF1
TP4	AMFD	AM Found	AF1
TP5	RG	Read Gate	AF1
TP6	PWRCNF	Power Conflict	AD2
TP7	VCMHT	VCM Heat	AD2
TP8	–	–	–
TP9	INTMOT	Initial Time Out	AD2
TP10	DVCK	Device Check	AD2
TP11	GND	–	–
TP12	WENB	Write Enable	AD2
TP13	AHDSL	Access Head Select	AD1
TP14	INX	Index	AC1
TP15	SCT	Sector	AC1
TP16	START	Start	AB1
TP17	GBENB	Guard Band Enable	AB1
TP18	SPOK	Speed OK	AB1
TP19	–	–	–
TP20	CHAENB/ CHENB 2	Channel A Enable/ Channel Enable 2	AB1
CH1	SPSG	Speed Signal	AB1
CH2	SPTM	Speed Timer	AB1
CH3	INHECH	Inhibit Echo	AD2
CH4	DLWG	Delayed Write Gate	AD2
CH5	–5V	–5V	AA3/AA2

The CQFM/CMKM PCB is provided with a potentiometer (RV1) and switches. These functions are shown in Table 6-6-13.

Table 6-6-13 CQFM/CMKM Potentiometer/Switch Function

No.	Function	Reference CH
RV1	Speed Timer	CH2
SW1	Disk Address	
SW2	Device Type/Sector Mode/TAG 4/5	

(6) XCBM PCB

XCBM PCB assembly is for the dual port function, the test points are located as shown in Figure 6-6-6, and each test point function is shown in Table 6-6-6-6-14.

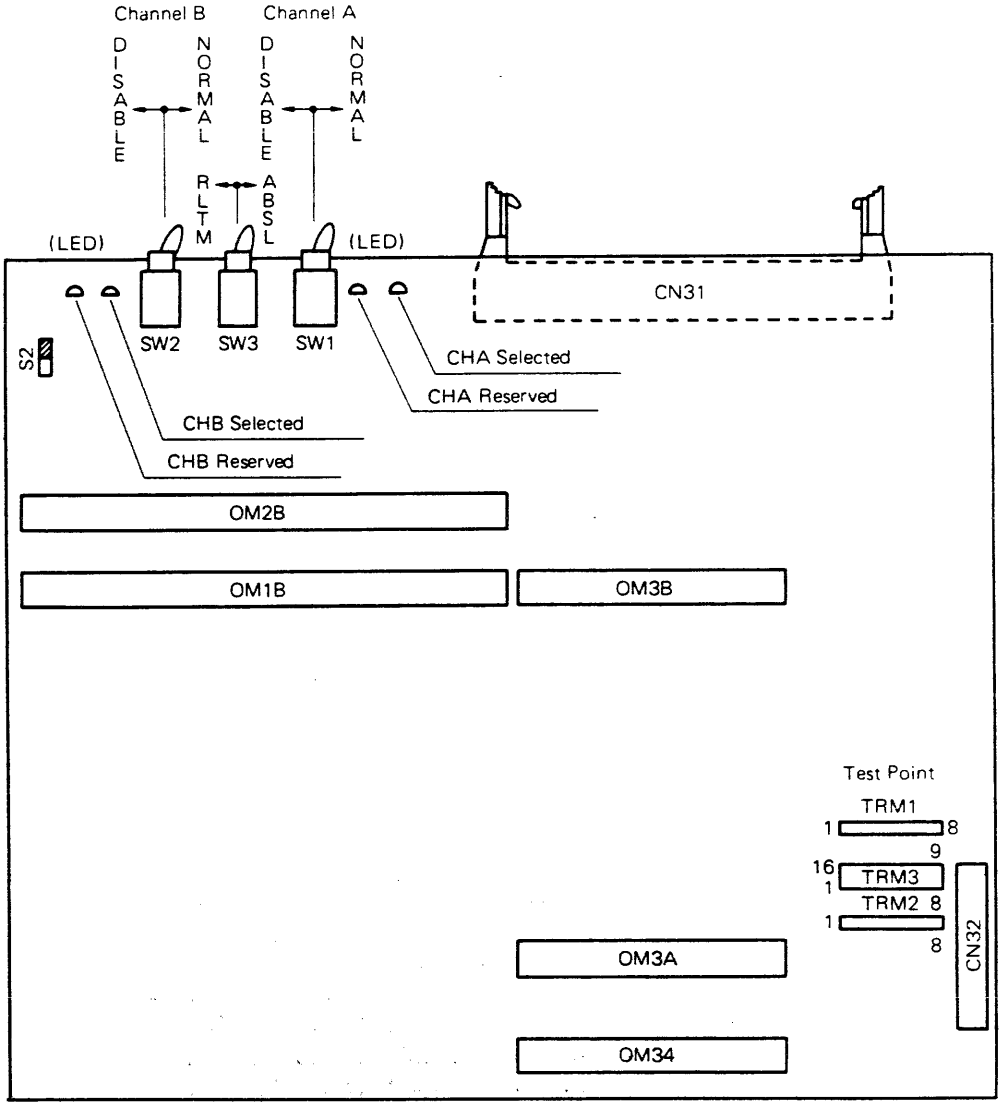


Figure 6-6-6 XCBM Test Points

Table 6-6-14 XCBM Test Points

TRM	No.	Abbreviation	Signal Name	Schematic code
TRM1	01	CHAENB	Channel A Enable	XC2
	02	DISAK	Disable Channel A Key	XC2
	03	DISBK	Disable Channel B Key	XC2
	04	*RLTMP	Release Timer Pulse	XC2
	05	CHBENB	Channel B Enable	XC2
	06	*CHBSLD	Channel B Selected	XC1
	07	*DISCHA2	Disable Channel A 2	XC1
	08	RLTMK	Release Timer Key	XC2
TRM2	01	CHACMP	Channel A Compare	XB1
	02	*DISCHB2	Disable Channel B 2	XC1
	03	BUSYB	Busy B	XC1
	04	PWRDY	Power Ready	XB1
	05	DISCHB	Disable Channel B	XC2
	06	DISCHA	Disable Channel A	XC3
	07	SKENDA	Seek End A	XC3
	08	0V		
TRM3	01	*INTR	Interrupt (30μs)	XC3
	02	SKENDB	Seek End B	XC3
	03	CHBCMP	Channel B Compare	XB1
	04			
	05	-5V		XB1
	06	CHARSV	Channel A Reserved	XC1
	07			
	08	*CHASLD	Channel A Selected	XC1
	09	0V		
	10			
	11			
	12			
	13	CLK1	Clock (200 ns)	XB1
	14	BUSYA	Busy A	XC1
	15	*STRSV	Set Reserve (300 ns)	XC1
	16	CHBRSV	Channel B Reserved	XC1

6.6.3 PCB Adjustment and Selection after PCB Replacement

6.6.3.1 Position Signal Adjustment (SDIM)

(1) Confirm that the unit has normal status.
(2) Issue the alternate seek command between Cylinder 0 and 512 repeatedly.
(3) Connect the test point TP19 (DRLM) to an oscilloscope and trigger with the positive going edge of the signal (DC coupled).
(4) Connect the test point TP7 (+POS) to the other channel at the oscilloscope (DC coupled).
(5) Adjust a potentiometer RV2 so that +POS (TP7) is 8 ± 0.4V (peak-to-peak). Refer to Figure 6-6-6.

Note: For coarse adjustment, issue the RTZ command and then adjust according to item (5).

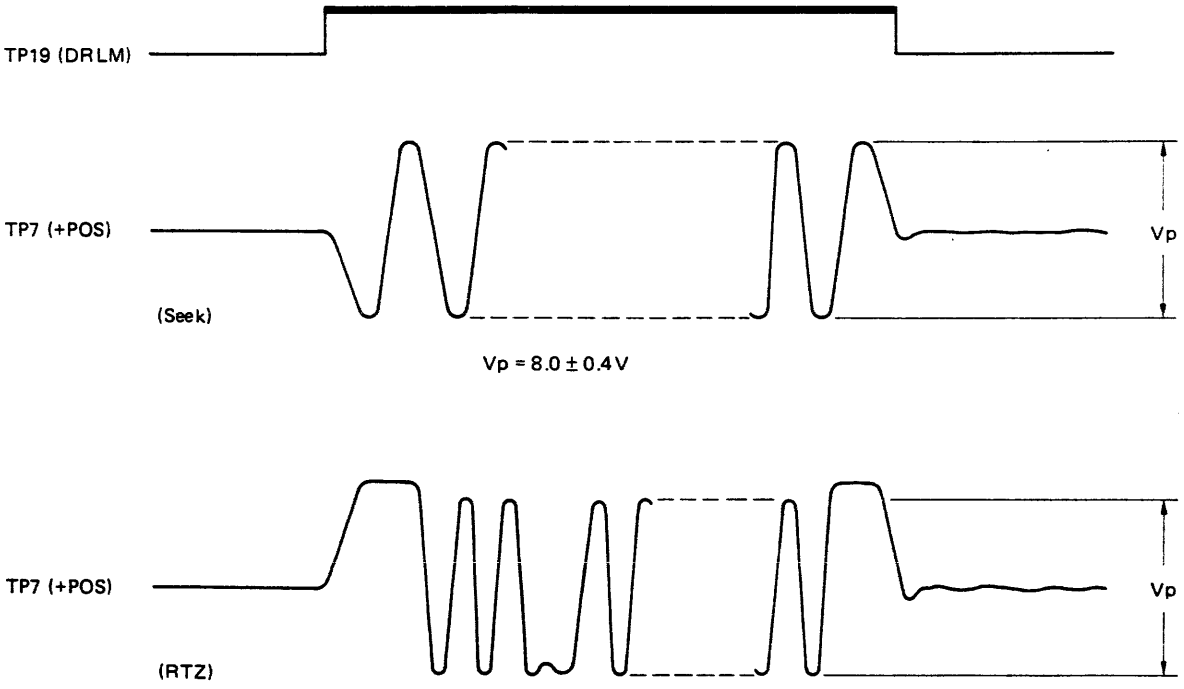


Figure 6-6-7 Position Signal Adjustment

6.6.3.2 Overshoot Adjustment (SDIM)

The Overshoot adjustment should be performed after Position Signal adjustment and Mount Direction setting.

(1) Confirm that unit has normal status.
(2) Issue the alternate seek command between Cylinder 0 and 8 repeatedly.
(3) Connect the test point TP19 (DRLM) to an oscilloscope and trigger with the positive going edge at the signal (DC coupled).
(4) Connect the test point TP7 (+POS) to the other channel at the oscilloscope (DC coupled).
(5) Adjust the Position Signal transient (overshoot) to linear mode with a potentiometer RV4 according to Figure 6-6-8.

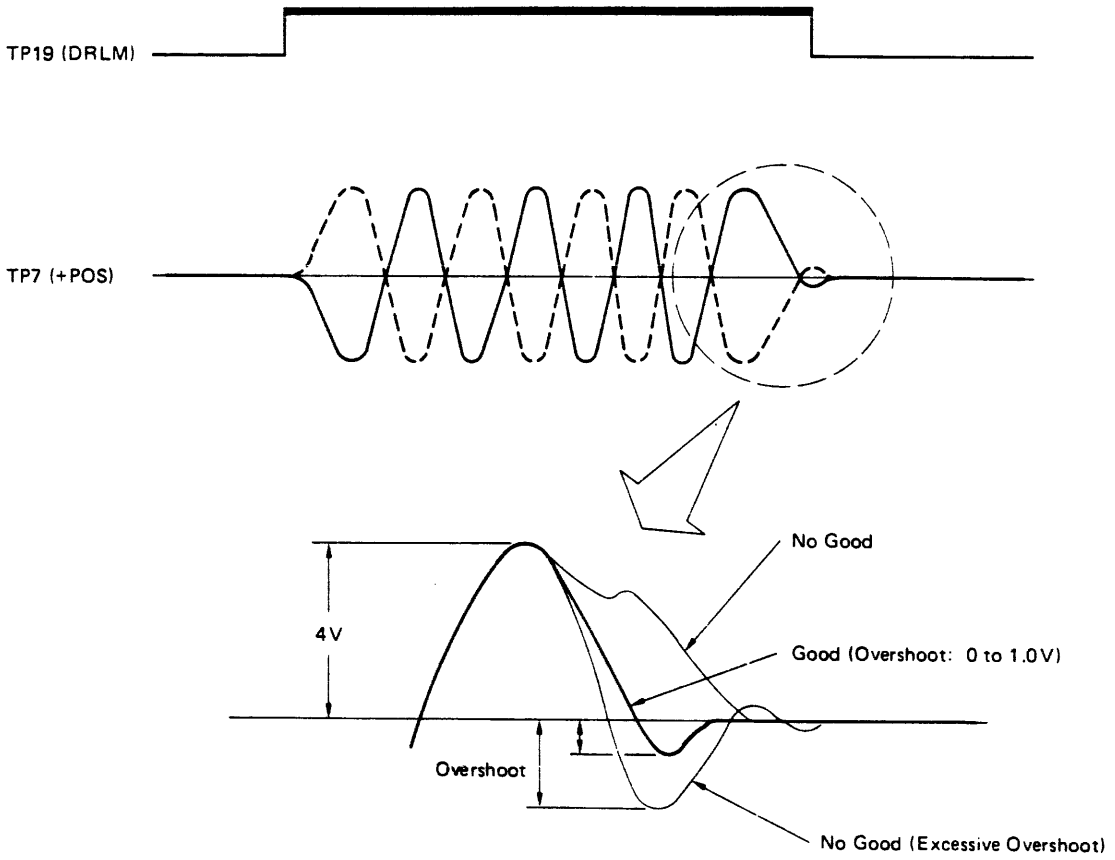


Figure 6-6-8 Overshoot Adjustment

6.6.3.3 Positioning Time Adjustment (SDIM)

(1) Confirm that unit has normal status.
(2) Issue the alternate seek command between Cylinder 0 and 512 repeatedly.
(3) Connect the test point TP26 (−DA) to an oscilloscope and trigger with the negative going edge of the signal (DC coupled).
(4) Adjust the decelerate time (Tdc) with a potentiometer RV1 to the nominal value of 13ms ± 1ms.
(5) Connect the test point TP30 (PADR) to an oscilloscope triggering with the positive going edge of TP19 (DRLM).
(6) Check the Vdc amplitude. If the Vdc amplitude is greater than 6.0V, adjust the potentimeter RV1 to be equal to or less than 6.0V. In this case, the specified Tdc may be greater than the specified time in item (4).
(7) After the Positioning Time adjustment, confirm that the Overshoot adjustment is correct. Refer to Figure 6-6-9.

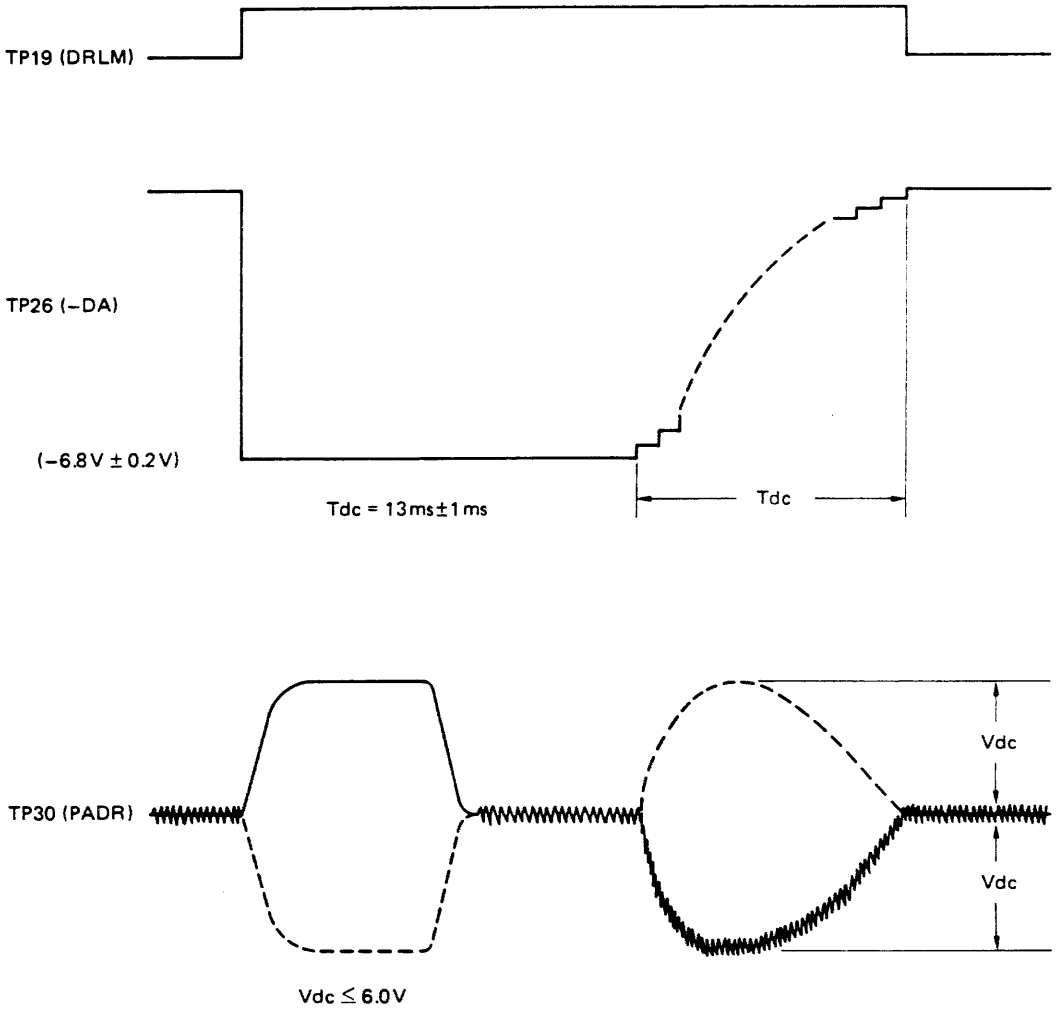


Figure 6-6-9 Positioning Time Adjustment

6.6.3.4 Mount Direction

When the unit is installed horizontally or vertically, the selecting plug on mother board GBNM/GBGM should be selected on V-H switch as shown in Figure 6-6-10.

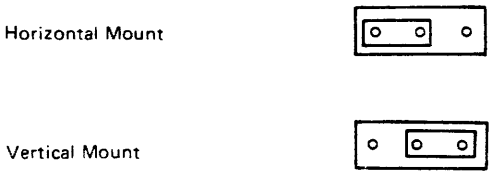


Figure 6-6-10 Mount Direction

6.6.3.5 Sector Count Selection (VOFM)

When the VOFM PCB assembly is replaced, the required number of sectors should be selected on SW1 and SW2 as follows:

Sector selection switches SW1 and SW2 are located at L2 and L1 respectively on VOFM PCB assembly.

Each key of SW1 and SW2 represents binary Byte clock, as shown in Table 6-6-15.

Table 6-6-15 Sector Selection Key

SW1	Byte	SW2	Byte
1	1	1	128
2	2	2	256
3	4	3	512
4	8	4	1,024
5	16	5	2,048
6	32	6	4,096
7	64	7	8,192

Location: VOFM L2 Location: VOFM L1

To position the proper keys on SW1 and SW2 according to the customer's requirement, calculate the Byte number by the following formula;

$$\text{Bytes/Sector} = \frac{\text{Bytes/Revolution}}{\text{Number of Sector}}$$

Bytes/Revolutions = 20,480 Bytes

Example for 8-Sector Format

$$\text{Bytes/Sector} = \frac{20{,}480}{8}$$

$$= 2{,}560 \text{ Bytes}$$

Keys to be closed	SW2	5 =	2,048
		2 =	256
		1 =	128
	SW1	7 =	64
		6 =	32
		5 =	16
		4 =	8
		3 =	4
		2 =	2
		1 =	1
Sector Counter Reset Clock			1
			2,560

Refer to Table 6-6-16.

Table 6-6-16 Sector Selection (Continued)

Sector	SW1	SW2	Byte/Sector	Last Sector Shorter
	1 2 3 4 5 6 7	1 2 3 4 5 6 7		
1			20,480	0
2	1 1 1 1 1 1 1	1 1 1 1 0 0 1	10,240	0
3	0 1 0 1 0 1 0	1 0 1 0 1 1 0	6,827	–1
4	1 1 1 1 1 1 1	1 1 1 0 0 1 0	5,120	0
5	1 1 1 1 1 1 1	1 1 1 1 1 0 0	4,096	0
6	1 0 1 0 1 0 1	0 1 0 1 1 0 0	3,414	–4
7	1 0 1 1 0 1 1	0 1 1 0 1 0 0	2,926	–2
8	1 1 1 1 1 1 1	1 1 0 0 1 0 0	2,560	0
9	1 1 0 0 0 1 1	1 0 0 0 1 0 0	2,276	–4
10	1 1 1 1 1 1 1	1 1 1 1 0 0 0	2,048	0
11	1 0 1 0 0 0 1	0 1 1 1 0 0 0	1,862	–2
12	0 1 0 1 0 1 0	1 0 1 1 0 0 0	1,707	–4
13	1 1 1 0 0 1 0	0 0 1 1 0 0 0	1,576	–8
14	0 1 1 0 1 1 0	1 1 0 1 0 0 0	1,463	–2
15	1 0 1 0 1 0 1	0 1 0 1 0 0 0	1,366	–10
16	1 1 1 1 1 1 1	1 0 0 1 0 0 0	1,280	0
17	0 0 1 0 1 1 0	1 0 0 1 0 0 0	1,205	–5
18	1 0 0 0 1 1 1	0 0 0 1 0 0 0	1,138	–4
19	1 0 1 0 1 1 0	0 0 0 1 0 0 0	1,078	–2
20	1 1 1 1 1 1 1	1 1 1 0 0 0 0	1,024	0
21	1 1 1 1 0 0 1	1 1 1 0 0 0 0	976	–16
22	0 1 0 0 0 1 0	1 1 1 0 0 0 0	931	–2
23	0 1 0 1 1 1 1	0 1 1 0 0 0 0	891	–13
24	1 0 1 0 1 0 1	0 1 1 0 0 0 0	854	–16
25	1 1 0 0 1 1 0	0 1 1 0 0 0 0	820	–20
26	1 1 0 0 1 0 0	0 1 1 0 0 0 0	788	–8
27	0 1 1 0 1 1 1	1 0 1 0 0 0 0	759	–13
28	1 1 0 1 1 0 1	1 0 1 0 0 0 0	732	–16
29	0 1 0 0 0 0 1	1 0 1 0 0 0 0	707	–23
30	0 1 0 1 0 1 0	1 0 1 0 0 0 0	683	–10
31	0 0 1 0 1 0 0	1 0 1 0 0 0 0	661	–11
32	1 1 1 1 1 1 1	0 0 1 0 0 0 0	640	0
33	0 0 1 1 0 1 1	0 0 1 0 0 0 0	621	–13
34	0 1 0 1 1 0 1	0 0 1 0 0 0 0	603	–22
35	1 0 0 1 0 0 1	0 0 1 0 0 0 0	586	–30
36	0 0 0 1 1 1 0	0 0 1 0 0 0 0	569	–4
37	1 0 0 1 0 1 0	0 0 1 0 0 0 0	554	–18
38	0 1 0 1 1 0 0	0 0 1 0 0 0 0	539	–2
39	1 0 1 1 0 0 0	0 0 1 0 0 0 0	526	–34
40	1 1 1 1 1 1 1	1 1 0 0 0 0 0	512	0
41	1 1 0 0 1 1 1	1 1 0 0 0 0 0	500	–20
42	1 1 1 0 0 1 1	1 1 0 0 0 0 0	488	–16
43	0 0 1 1 1 0 1	1 1 0 0 0 0 0	477	–31
44	1 0 0 0 1 0 1	1 1 0 0 0 0 0	466	–24
45	1 1 1 0 0 0 1	1 1 0 0 0 0 0	456	–40
46	1 0 1 1 1 1 0	1 1 0 0 0 0 0	446	–36

Table 6-6-16 Sector Selection

Sector	SW1	SW2	Byte/Sector	Last Sector Shorter
	1 2 3 4 5 6 7	1 2 3 4 5 6 7		
47	1 1 0 0 1 1 0	1 1 0 0 0 0 0	436	–12
48	0 1 0 1 0 1 0	1 1 0 0 0 0 0	427	–16
49	1 0 0 0 0 1 0	1 1 0 0 0 0 0	418	–2
50	1 0 0 1 1 0 0	1 1 0 0 0 0 0	410	–20
51	1 0 0 0 1 0 0	1 1 0 0 0 0 0	402	–22
52	1 0 0 1 0 0 0	1 1 0 0 0 0 0	394	–8
53	0 1 0 0 0 0 0	1 1 0 0 0 0 0	387	–31
54	1 1 0 1 1 1 1	0 1 0 0 0 0 0	380	–40
55	0 0 1 0 1 1 1	0 1 0 0 0 0 0	373	–35
56	1 0 1 1 0 1 1	0 1 0 0 0 0 0	366	–16
57	1 1 1 0 0 1 1	0 1 0 0 0 0 0	360	–40
58	1 0 0 0 0 1 1	0 1 0 0 0 0 0	354	–52
59	1 1 0 1 1 0 1	0 1 0 0 0 0 0	348	–52
60	1 0 1 0 1 0 1	0 1 0 0 0 0 0	342	–40
61	1 1 1 1 0 0 1	0 1 0 0 0 0 0	336	–16
62	0 1 0 1 0 0 1	0 1 0 0 0 0 0	331	–42
63	1 0 1 0 0 0 1	0 1 0 0 0 0 0	326	–58
64	1 1 1 1 1 1 0	0 1 0 0 0 0 0	320	0
65	1 1 0 1 1 1 0	0 1 0 0 0 0 0	316	–60
66	0 1 1 0 1 1 0	0 1 0 0 0 0 0	311	–46
67	1 0 0 0 1 1 0	0 1 0 0 0 0 0	306	–22
68	1 0 1 1 0 1 0	0 1 0 0 0 0 0	302	–56
69	0 0 0 1 0 1 0	0 1 0 0 0 0 0	297	–13
70	0 0 1 0 0 1 0	0 1 0 0 0 0 0	293	–30
71	0 0 0 0 0 1 0	0 1 0 0 0 0 0	289	–39
72	0 0 1 1 1 0 0	0 1 0 0 0 0 0	285	–40
80	1 1 1 1 1 1 1	1 0 0 0 0 0 0	256	0
128	1 1 1 1 1 0 0	1 0 0 0 0 0 0	160	0

Notes: 1. "1" indicates that the key is set to ON side.
2. "0" indicates that the key is set to OFF side.
3. The last sector is equal or shorter than nominal sector.

6.6.3.6 Disk Address (CQFM/CMKM)

Disk Address 0 to 7 is selectable at SW1 on location J2/J1 on CQFM/CMKM PCB assembly.

Set the desired disk address by three keys on SW1 in binary code as shown in Table 6-6-17.

Table 6-6-17 Disk Addressing

Disk Address	Key 1 2^0	Key 2 2^1	Key 3 2^2
0	OFF	OFF	OFF
1	ON	OFF	OFF
2	OFF	ON	OFF
3	ON	ON	OFF
4	OFF	OFF	ON
5	ON	OFF	ON
6	OFF	ON	ON
7	ON	ON	ON

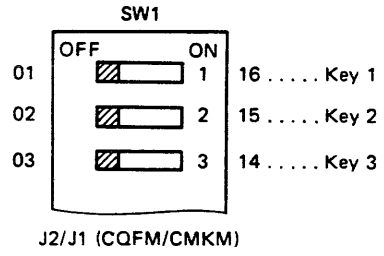


Figure 6-6-11 Disk Address

6.6.3.7 Device Type (CQFM/CMKM Optional)

If the system uses Tag 4 and Tag 5, the specified device type must be set using six keys on SW2 at location P3 on the CQFM/CMKM PCB assembly according to Table 6-6-18.

Table 6-6-18 Device Type (Optional)

Device Type	Decimal Number	Key 1 2^0	Key 2 2^1	Key 3 2^2	Key 4 2^3	Key 5 2^4	Key 6 2^5
M2282	20	OFF	OFF	ON	OFF	ON	OFF
M2280	21	ON	OFF	ON	OFF	ON	OFF
M2283	24	OFF	OFF	OFF	ON	ON	OFF
M2284	28	OFF	OFF	ON	ON	ON	OFF
M2286	22	OFF	ON	ON	OFF	ON	OFF
M2289	23	ON	ON	ON	OFF	ON	OFF
M2287	26	OFF	ON	OFF	ON	ON	OFF
M2288	30	OFF	ON	ON	ON	ON	OFF

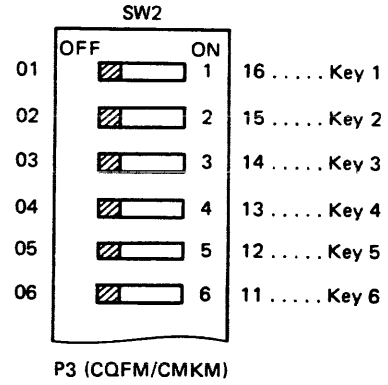


Figure 6-6-12 Device Type

6.6.3.8 Sector Mode (CQFM/CMKM)

The customer can select Hard Sector mode (1 to 128) or Variable Soft Sector mode (using Address Mark function) on SW2 at location P3 the CQFM/CMKM PCB assembly.

In the case of Hard Sector mode, the customer must set the number of sectors per disk revolution as described in 6.6.3.4.

In the case of Variable Soft Sector mode, setting the number of sectors per disk revolution is also required according to system configuration.

Table 6-6-19 Sector Mode

Sector Mode	Key 7
Hard Sector	OFF
Variable Soft Sector	ON

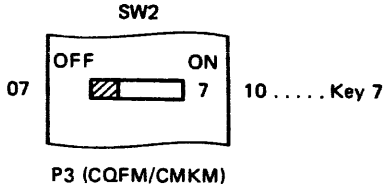


Figure 6-6-13 Sector Mode

6.6.3.9 Tag 4/5 Enable (CQFM/CMKM)

FDU M228X provides Tag 4 and Tag 5 functions, however, the customer may disable or enable these functions at SW2 (Key 8) at location P3 on the CQFM/CMKM PCB assembly. Disabling the Tag 4/5 functions inhibits the receivers of Tag 4 Tag 5.

Table 6-6-20 Tag 4/5 Enable

Tag 4/5	Key 8
Disable	OFF
Enable	ON

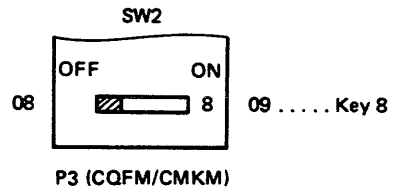


Figure 6-6-14 Tag 4/5 Enable

6.6.4 Electrical Check and Adjustment

The following description is for electrical checks and adjustments when the repair has been performed.

Caution: Do not perform the following adjustments when the PCB is replaced.

6.6.4.1 RQVM/RQWM PCB

(a) Access Head Write Current Adjustment (EA1)

1. Confirm that the unit has normal status.
2. Connect the test point TP18 (AHWCA) to an oscilloscope and connect the test point TP19 (AHWCB) to the other channel of the oscilloscope with INV mode.
3. Issue the seek command to Cylinder 0 and Head 0.
4. Issue the write command to proper number of records.
5. Add the two channel (differential mode) and adjust the potentiometer RV1 so that the difference is 460mV ± 10mV.

(b) Fixed Head Voltage Fault Protect (EB1)

This adjustment is used to inhibit the write circuit when +5V power falls below +4V approximately.

This adjustment requires a special tool, therefore, do not adjust it in the field.

6.6.4.2 SDIM PCB

(a) Servo Pulse Window (CA1)

1. Connect the test point TP10 (SVPWD) to a channel of the oscilloscope.
2. Adjust the potentiometer RV8 so that following Tss is 345ns ± 10ns.

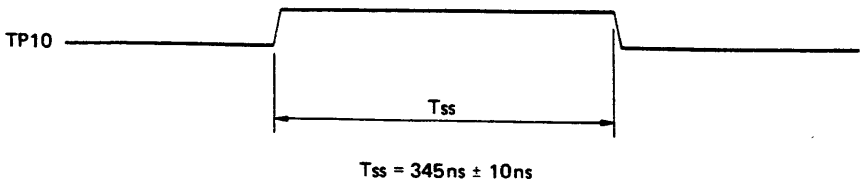


Figure 6-6-15 Servo Pulse Window

(b) PLOI Free Running Frequency (CA2)

1. Turn the power off.
2. Set the switch S1 to the OFF position.
3. Clamp the CMKM-TP17 (GBENB) to 0V.
4. Turn the power on, and wait 40 seconds.
5. Connect the TP8 (Vcx1) to an oscilloscope (DC coupled.)
6. Adjust the potentiometer RV5 so that TP8 signal is + 2.5V ± 0.1V.
7. Connect the test point TP15 (1/8F) to the Frequency Counter.
8. Select the proper capacitance as shown in Table 6-6-21 so that the frequency of TP15 is closest to 1.012MHz.
9. Finally adjust the potentiometer RV5 so that the frequency of TP15 is 1.012MHz ± 2%.

Table 6-6-21 PLOI Adjustment

Plug		Capacitance
S2	S3	
2–3	2–3	78PF
1–2	2–3	93PF
2–3	1–2	111PF
1–2	1–2	126PF

(c) Function Offset (CB3)

1. Confirm that the unit has normal status.
2. Connect the test point TP23 (FUNC) to an oscilloscope (DC coupled).
3. Adjust the potentiometer RV3 so that the signal of TP23 is +100mV ± 10mV.

(d) PLOI Phase (CA1)

1. Turn the power off.
2. Set the switch S1 to the OFF position.
3. Turn the power on, and wait 40 seconds.
4. Connect the test point TP13 (PLOSS) to a channel of the oscilloscope.
5. Adjust the potentiometer RV6 so that the following Tss is 1.85μs ± 0.1μs.

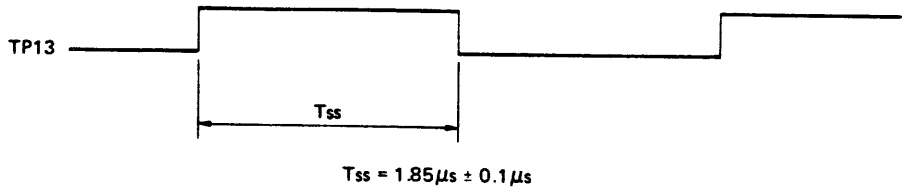


Figure 6-6-16 PLOSS Adjustment

(e) DAC Output (CB3)

1. Confirm that the unit has normal status.
2. Issue the alternate seek command between cylinder 0 and 512 repeatedly.
3. Connect the test point TP26 (DA) to an oscillator and trigger with the negative-going edge of TP26 signal.
4. Adjust the potentiometer RV7 so that VDA is −6.8V ± 0.2V.

Refer to Figure 6-6-17.

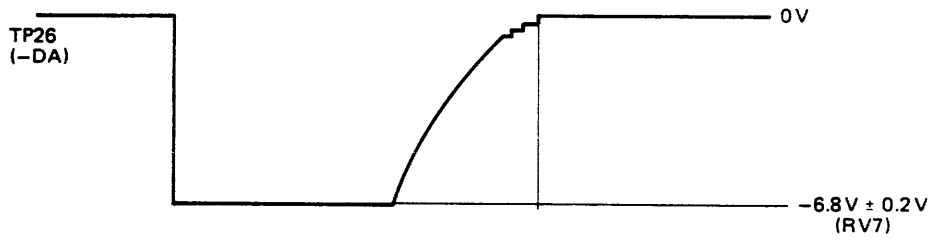


Figure 6-6-17 DAC Output Adjustment

6.6.4.3 CMIM PCB

(a) Settling Time 1 (BE1)

1. Confirm that the unit has normal status.
2. Connect the check terminal CH2 to an oscilloscope.
3. Issue the alternate seek command between Cylinder 0 and 1 repeatedly.
4. Trigger with the positive-going edge of CH2 signal, and then adjust the potentiometer RV1 so that the pulse width of CH2 signal is 2.5ms ± 0.1ms.

   Refer to Figure 6-6-18.

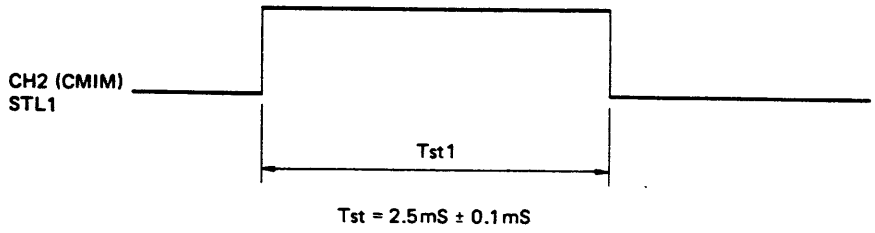


Figure 6-6-18 Settling Time 1 Adjustment

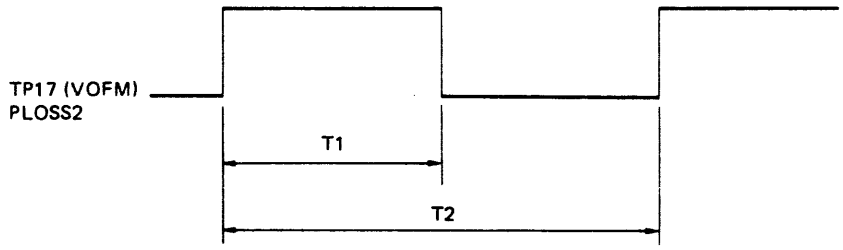
6.6.4.4 VOFM PCB

The adjustment (a) to (d) require a PCB extender.

(a) PLO II SS2 (DC1)

1. Trigger with positive-going edge of TP17 signal, and adjust the potentiometer RV4 so that T1 is 988ns ± 40ns.

   Refer to Figure 6-6-19.



T1 = 988ns ± 40ns = +2/T2
T2 = 1.98μs ± 80ns

Figure 6-6-19 PLOSS 2 Adjustment

(b) PLO II VCO Frequency (DC2)

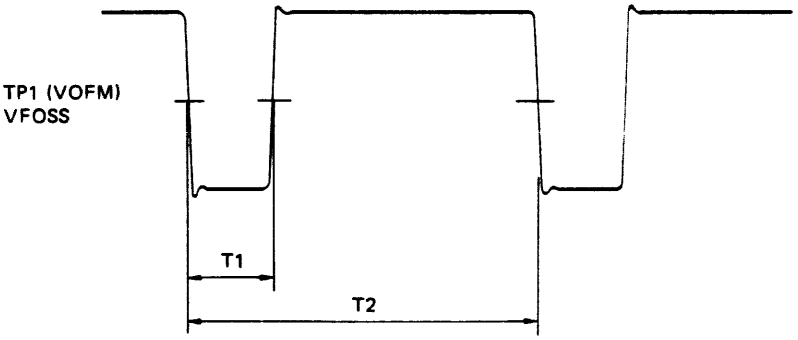
Before this adjustment, items (a) must be completed.

1. Connect the test terminal TP13 (VC PLO) to an oscilloscope (DC coupled).
2. Adjust the potentiometer RV2 so that DC level of TP13 signal is −300mV ± 200mV.

(c) VFOSS (DD1)

1. Connect the test terminal TP1 (VFOSS) to an oscilloscope (DC coupled).
2. Adjust the jumper wire on S4 so that the pulse width of TP1 is 31ns ± 2ns.

   Refer to Figures 6-6-20 and 6-6-21.



T1 = 31ns ± 2ns
T2 = 123ns (nominal)

Figure 6-6-20 VFOSS Adjustment

Note: Jumpering Method

1) Connect only one of jumper wire, Ⓓ or Ⓔ. Jumper wire Ⓓ widens about 10ns more than Ⓔ.
2) Jumper wire Ⓐ widens about 3ns.
   Selecting Plug Ⓑ widen about 2ns.
   Selecting Plug Ⓒ widen about 4ns.

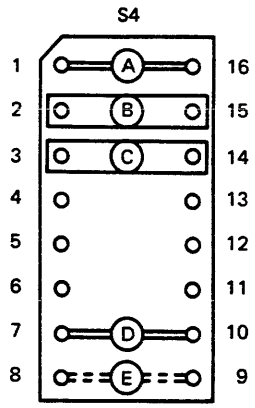


Figure 6-6-21 VFOSS Adjustment 2

(d) VFO Frequency

1. Item (d) adjustment must be performed before this adjustment.
2. Confirm that the unit has normal status.
3. Connect the test point TP4 to an oscilloscope (DC coupled).
4. Adjust the potentiometer RV1 so that DC level of TP4 signal is +100mV ± 100mV.
5. After the adjustment confirm TP4 signal as shown in Figure 6-6-22 by enabling read operation. Trigger it with the positive-going edge of TP3 (LDATA: CQFM/CMKM PCB).

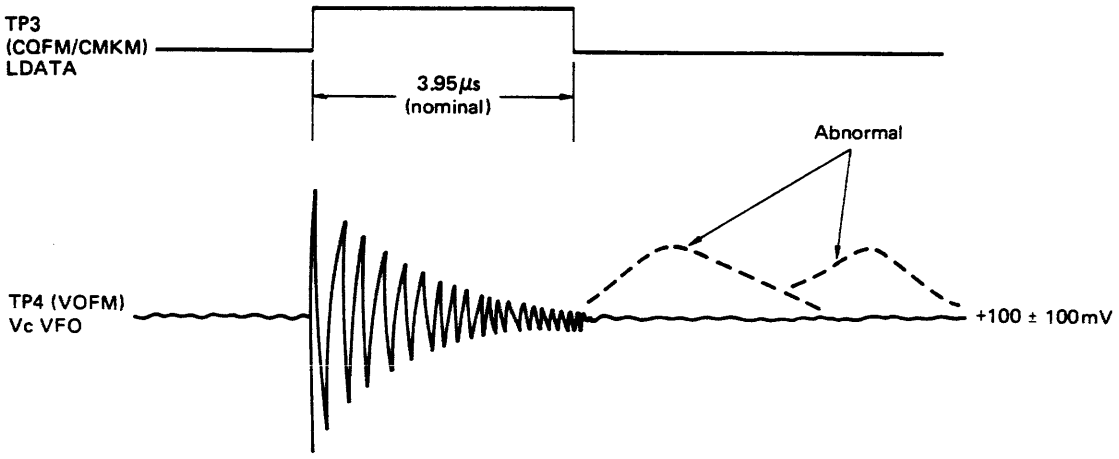
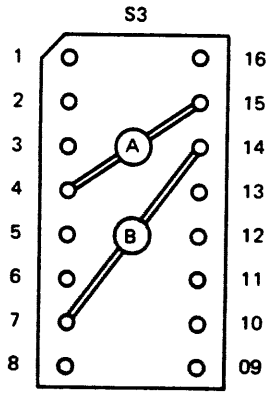


Figure 6-6-22 VFO Frequency Adjustment

(e) Write Compensation

Caution: Use the same length probes for measurement and/or adjustment of the write compensation, also use the 0V terminal near the test points TP14, 15 and 16. Otherwise some adjustment error will occur.

1. Connect the test point TP14 (2FEY) to an oscilloscope (DC coupled).
2. Connect the test point TP15 (2FOT) to the other channel (DC coupled).
3. Select a jumper wire on S3 so that Td1 is 6ns ± 2ns.
   Refer to Figure 6-6-23.
4. Similarly, connect the test points TP15 and TP16 and select a jumper wire on S3 so that Td2 is 6ns ± 2ns.
   Refer to Figure 6-6-24.



1) Adjacent pins have 2ns delay from 1 to 8.
2) Pins 16 and 09 to 13 are not used.

Figure 6-6-23 Write Compensation

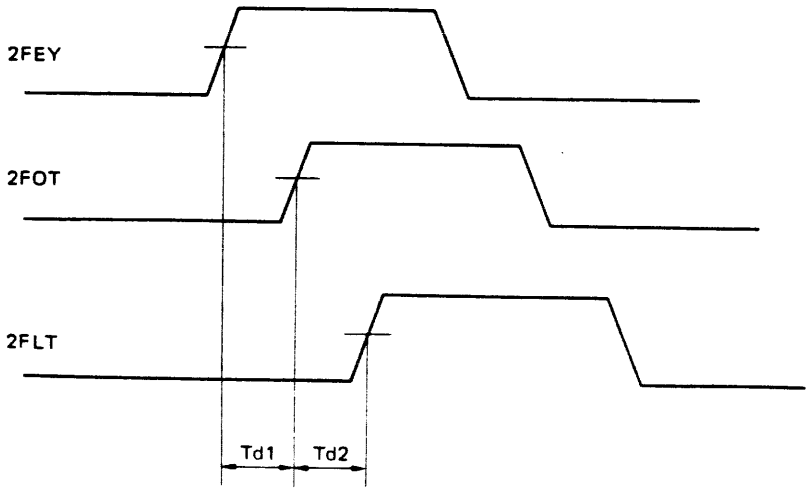


Figure 6-6-24 Write Compensation Adjustment

(f) Data Window

Caution: Use the 0V terminals near the check terminals CHE1 to 3 for the adjustment, also use 200MHz oscilloscope. Otherwise some adjustment error may occur.

1. Connect the check terminals CHE2 to an oscilloscope (DC coupled).
2. Connect the check terminal CHE1 to the other channel (DC coupled).
3. Trigger with the positive-going edge of CH2 signal.
4. Adjust the potentiometer RV5 so that TADJ is 27ns ± 2ns. Refer to Figure 6-6-25.

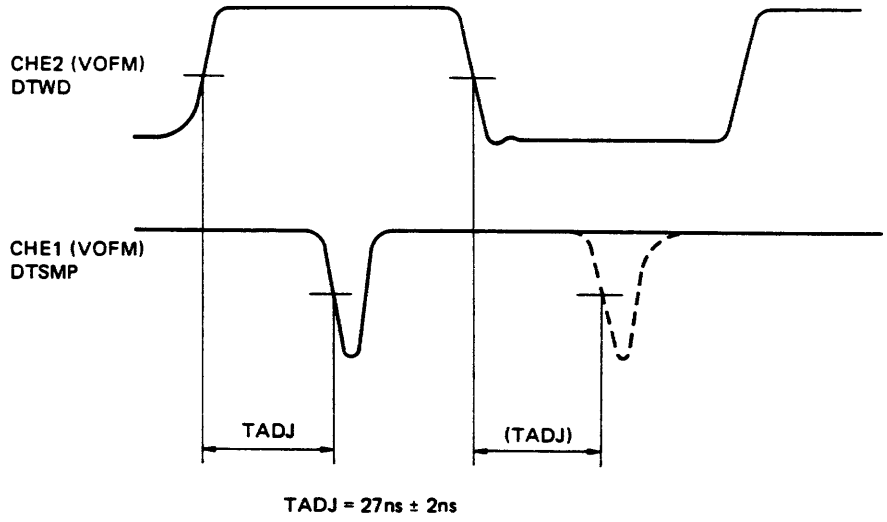


Figure 6-6-25 Data Window Adjustment

6.6.4.5 CQFM/CMKM

(a) Speed Timer

1. Turn the power off.
2. Set the switch S1 of SDIM PCB to the OFF position.
3. Turn the power on.
4. Connect the check terminal CH2 to an oscilloscope (DC coupled).
5. Trigger with the positive-going edge of CH2 signal and adjust the potentiometer RV1 so that the positive pulse is 25ms ± 0.5ms.

6.6.5 Electrical Measurement

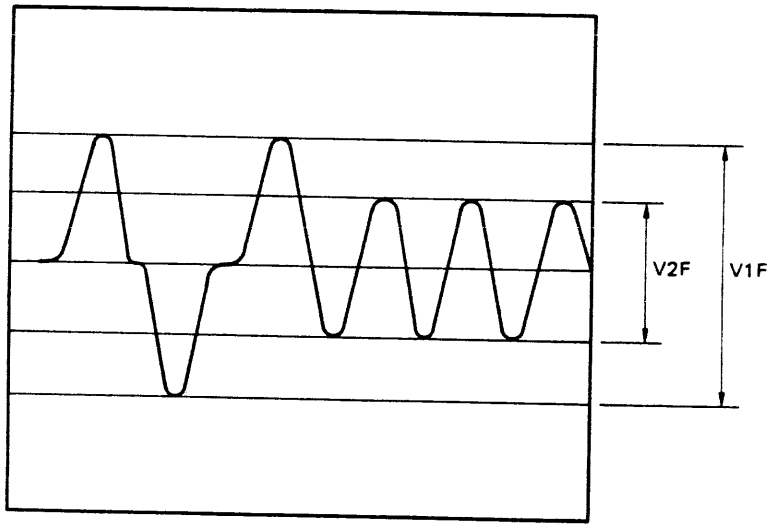
This description will give the maintenance aid to maintenance personnel for electrical measurement.

6.6.5.1 Read Output Measurement

Caution: Use the 0V terminals near the test points CH1 and CH2 on RQVM/RQWM PCB, and also use the 200MHz wide band oscilloscope. Otherwise some measurement error may occur.

1. Write a repetitive "10" pattern (all "A_{16}") to all records on the desired track.
2. Connect the test point TP1 and TP2 on RQVM/RQWM PCB with the differential mode (inverted channel 2 and add with channel 1).
3. After writing, measure the peak-to-peak level of V_{2F} and V_{1F} as shown in Figure 6-6-26.

Note: The measurement may be performed on Cylinder 0 and even Head address.



$V2F \geq 80mVp\text{-}p$

$$\text{Resolution Ratio} = \frac{V2F}{V1F} \times 100(\%) \geq 55\%$$

Figure 6-6-26 Read Output Measurement

6.6.5.2 Timing Margin Measurement

The write data pattern may be "$EB6DB6DB_{16}$". After writing on all records of Cylinder 0 – even Head address, this measurement should be performed.

Caution: Use the 0V terminals near the check terminals CHE1 to 3 for the measurement, also use 200MHz wide band oscilloscope. Otherwise some measurement error may occur.

1. Connect the check terminals CHE1 and CHE2 on VOFM PCB. Refer to 6.6.4.4 item (e).
2. Adjust CHE1 signal by the potentiometer RV5 to minimum width of critical state that no errors occur for five minutes. ——→ TW1
3. Similarly, adjust the maximum width as mentioned above. ——→ TW2
4. Perform the procedures 2 and 3 to all even Head on Cylinder 0 respectively.
5. The timing margin will be specified as follows:

$$TTMG = TW2\ (min) - TW1\ (max) \geq 10ns$$

6. Finally adjust the CHE1 signal as follows:

$$T_{ADJ} = \frac{TW2\ (min) + TW1\ (max)}{2} \fallingdotseq 27ns$$

Refer to Figure 6-6-27.

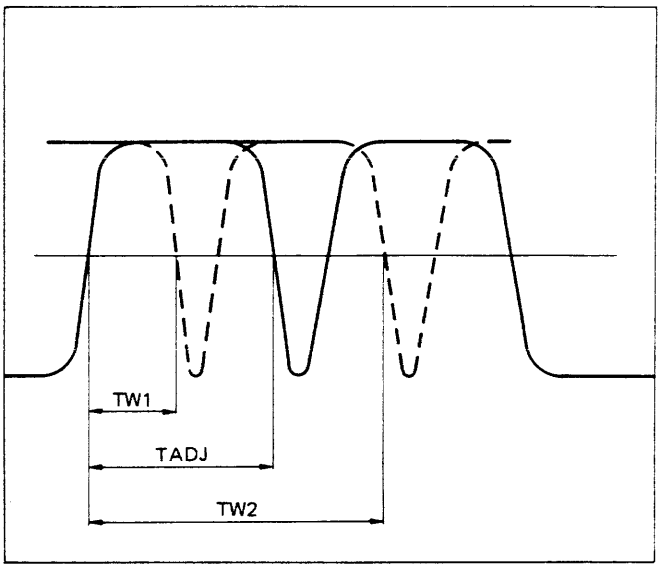


Figure 6-6-27 Timing Margin Measurement

Section 7

Spare Parts List

7. SPARE PARTS LIST

7.1 SPARE PARTS LIST

Table 7-1 Spare Parts List

Item	Designation	Specification
1.	Disk Enclosure: 67.4MB without Fixed Head Storage	B030-4540-T002A
2.	Disk Enclosure: 84.2MB without Fixed Head Storage	B030-4540-T010A
3.	Disk Enclosure: 134.8MB without Fixed Head Storage	B030-4540-T003A
4.	Disk Enclosure: 168.6MB without Fixed Head Storage	B030-4540-T004A
5.	Disk Enclosure: 67.4MB with 655KB Fixed Head Storage	B030-4540-T006A
6.	Disk Enclosure: 84.2MB with 655KB Fixed Head Storage	B030-4540-T009A
7.	Disk Enclosure: 134.8MB with 655KB Fixed Head Storage	B030-4540-T007A
8.	Disk Enclosure: 168.6MB with 655KB Fixed Head Storage	B030-4540-T008A
9.	Spindle Drive Motor (AC100/115V)	B90L-0980-0001A
10.	Spindle Drive Motor (AC220/240V)	B90L-0980-0003A
11.	Belt	B30L-1000-0006A
12.	Anti-Static Brush	B030-4420-W006A
13.	Speed Transducer Assembly	B030-4420-W030A
14.	Blower	B90L-1190-0001A
15.	Brake Relay	B58L-0170-0001A
16.	Variable Oscillator F (VOFM) PCB Assembly	B16B-6300-0010A
17.	Controller I (CMIM) PCB Assembly	B16B-6150-0010A
18.	Controller F (CQFM) PCB Assembly	B16B-6160-0030A
19.	Speed Controller I (SDIM) PCB Assembly	B16B-6240-0010A
20.	Read Switch V (RQVM) PCB Assembly (with Fixed Head)	B16B-6170-0010A
21.	Read Switch W (RQWM) PCB Assembly (without Fixed Head)	B16B-6170-0020A

Section 8

IC Details

8. IC DETAILS

8.1 INTRODUCTION

This section describes functions of TTL, ECL, Linear and FUJITSU Analog Master Slice IC's.

8.2 LOGIC CONVENTIONS AND SYMBOLOGY

8.2.1 TTL Logic

M228X Fixed Disk Unit uses +5V Transistor-Transistor-Logic. TTL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High Voltage = Logical "1"
Low Voltage = Logical "0"

The input/output logic of TTL are defined as follows:

(A) TTL Medium Speed IC

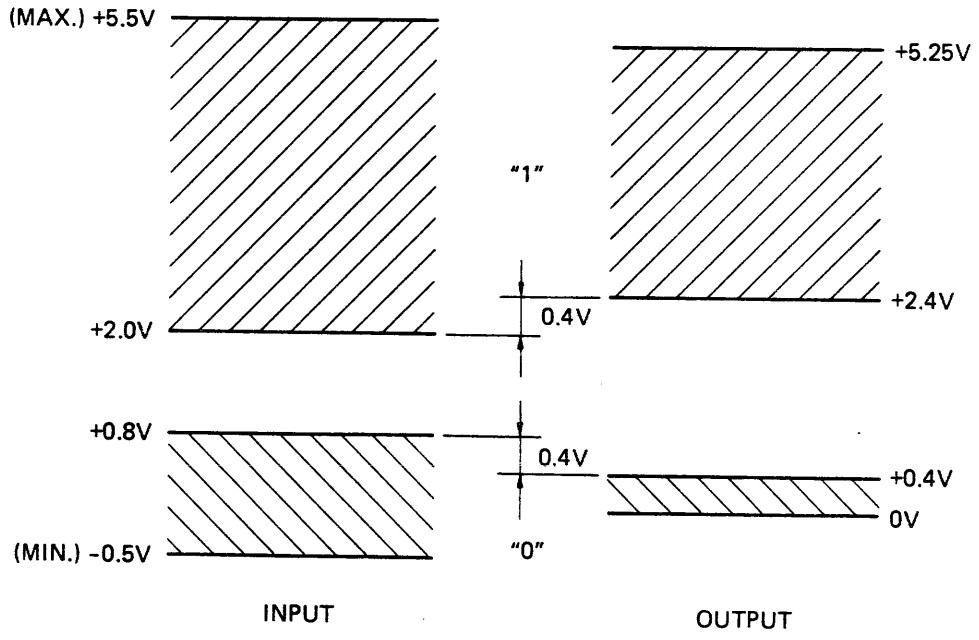


Figure 8-2-1 TTL Medium Speed IC Level

(B) TTL Super High Speed IC Level

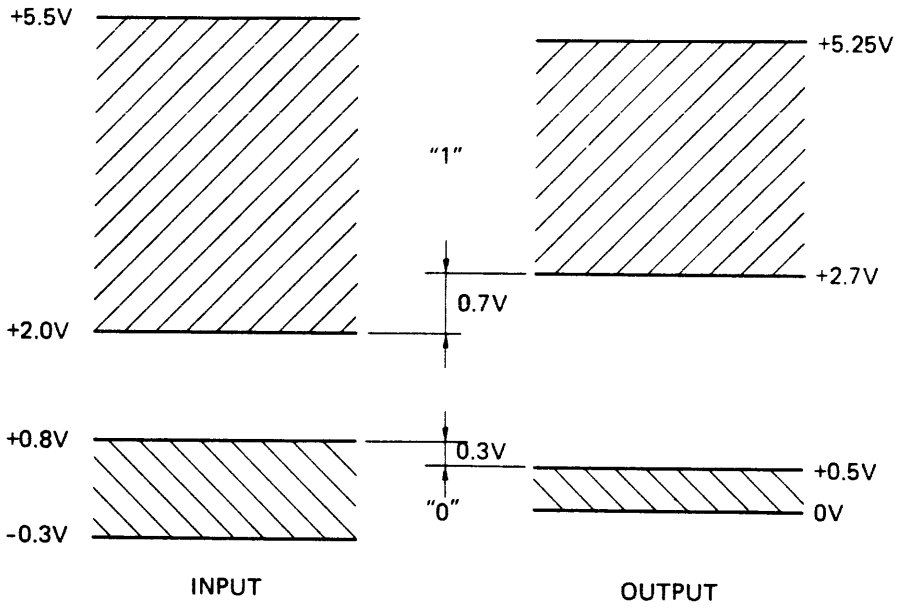


Figure 8-2-2 TTL Super High Speed IC Level

(C) TTL Medium Speed Low Power Consumption IC

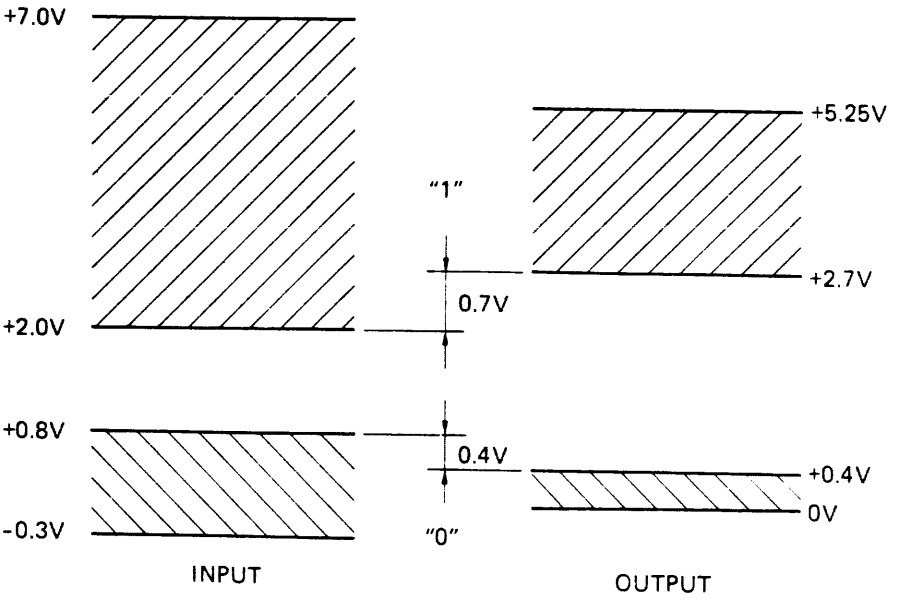


Figure 8-2-3 TTL Medium Speed Low Power Consumption IC Level

8.2.2 ECL Logic

M228X Fixed Disk Unit uses −5.2V ECL (Emitter-Coupled-Logic). The high impedance of the logic (input to differential amplifier) coupled with the low impedance of the driving source (emitter-follower output) allows high DC fan-out.

High-speed operation and high AC fan-out are possible because all circuits are designed to operate in a 50 ohms system. Complementary outputs cause a function and its complement to appear simultaneously at the device output, without the use of external inverters. In M228X each output is terminated to resistors. ECL logic is defined in terms of standard POSITIVE LOGIC using the following definitions:

High Voltage = Logical "1"
Low Voltage = Logical "0"

The input/output logic levels of ECL are defined as follows:

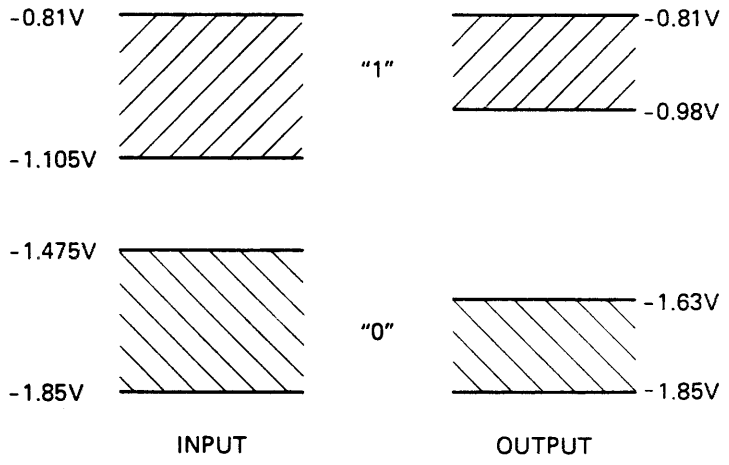
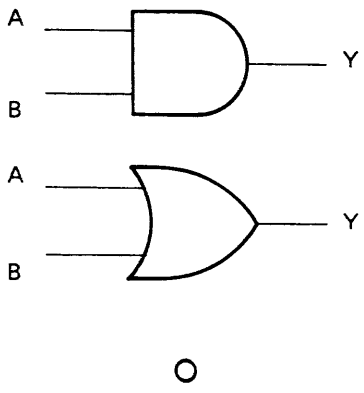


Figure 8-2-4 ECL Logic Level

8.2.3 Logic Symbology

The following conventions are provided to aid in understanding the symbology used in this manual.

1) TTL



This indicates AND gate.

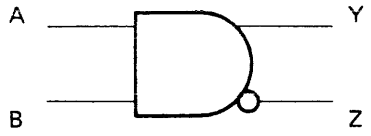
$Y = A \cdot B$

This indicates OR gate.

$Y = A+B$

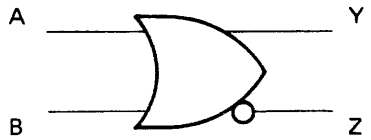
A circle placed on any input line or on the output line indicates that logical "0" is the significant state.
The absence of a circle, "1" is the significant state.

2) ECL



This indicates AND/NAND Gate.

$Y = A \cdot B = \overline{Z}$



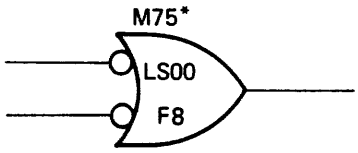
This indicates OR/NOR gate.

$Y = A+B = \overline{Z}$

This is equal to it of the TTL.

3) All logic symbols on each logic diagram are identified by a sequential numbering and element type code.

For example:



M75*: Sequential part number of each parts list.
LS00 : abbreviation (marking) of the element code.
F8 : Physical location of element on P.C.B assembly.

8.3 IC INTERCHANGEABILITY GUIDE

8.3.1 TTL IC Interchangeability

Table 8-3-1 TTL Interchangeability

FUJITSU		Direct	Functions	Page
Type No.	Marking	Replacement		
MB400M	LA01	SN7400N	Quad 2-input NAND	8-8
MB401M	LA02	SN7410N	Triple 3-input NAND	8-8
MB402M	LA03	SN7420N	Dual 4-input NAND	8-8
MB403M	LA04	SN7430N	8-input NAND	8-8
MB417M	LA17	SN7402N	Quad 2-input NOR	8-8
MB418M	LA18	SN7404N	Hex Inverter	8-9
MB420M	420	SN7474N	Dual D-type Flip-Flop	8-12
MB433M	433	SN7438N	Quad 2-input NAND Buffer	8-9
MB434M	434	SN75451P	Dual 2-input OR Buffer	8-9
MB435M	435	SN7437N	Quad 2-input NAND Buffer	8-9
MB436M	436	SN75453P	Dual 2-input OR Buffer	8-9
MB440M	440	SN74123N	Dual Monostable	8-13

Table 8-3-1 TTL Interchangeability

FUJITSU		Direct	Functions	Page
Type No.	Marking	Replacement		
MB442M	LA22	SN7442N	BCD to Decimal Decoder	8-14
MB450M	LA30	SN74161N	4-bit Binary Counter	8-15
None	LX07	SN74164N	8-bit Shift Register	8-17
None	LX16	SN75452P	Dual 2-input NAND Buffer	8-10
None	LX18	SN7408N	Quad 2-input AND	8-10
None	LX20	SN7414N	Hex Schmitt-Trigger Inverter	8-10
None	LX21	SN7432N	Quad 2-input OR	8-10
None	LX26	SN74175N	Quad D-Type Flip-Flop	8-18
None	LX27	SN74221N	Dual Monostable	8-20
MB74S00M	S00 (LH01)	SN74S00N	Quad 2-input NAND	8-8
MB74S10M	S10 (LH02)	SN74S10N	Triple 3-input NAND	8-8
MB74S20M	S20 (LH03)	SN74S20N	Dual 4-input NAND	8-8
None	S133 (LH07)	SN74S133N	13-input NAND	8-10
None	S112 (LH10)	SN74S112N	Dual J-K Flip-Flop	8-12
None	S124 (LH24)	SN74S124N	Dual VCO	8-21
None	None	SN75107N	Dual Line Receiver	8-28
None	None	SN75110N	Dual Line Driver	8-28
MB74LS00M	LS00	SN74LS00N	Quad 2-input NAND	8-8
MB74LS02M	LS02	SN74LS02N	Quad 2-input NOR	8-8
MB74LS04M	LS04	SN74LS04N	Hex Inverter	8-9
MB74LS08M	LS08	SN74LS08N	Quad 2-input AND	8-10
MB74LS10M	LS10	SN74LS10N	Trip 3-input NAND	8-8
MB74LS11M	LS11	SN74LS11N	Trip 3-input AND	8-11
MB74LS20M	LS20	SN74LS20N	Dual 4-input NAND	8-8
MB74LS32M	LS32	SN74LS32N	Quad 2-input OR	8-10
MB74LS37M	LS37	SN74LS37N	Quad 2-input NAND Buffer	8-9
MB74LS51M	LS51	SN74LS51N	Dual 2-wide 2-input AND-OR-INV	8-11
MB74LS54M	LS54	SN74LS54N	4-wide 2-input AND-OR-INV	8-11
None	LS74	SN74LS74AN	Dual D-Type Flip-Flop	8-12
None	LS85	SN74LS85N	4-Bit Magnitude Comparator	8-22
MB74LS86M	LS86	SN74LS86N	Quad 2-input EOR	8-11

Table 8-3-1 TTL Interchangeability

FUJITSU		Direct	Functions	Page
Type No.	Marking	Replacement		
MB74LS107M	LS107	SN74LS107N	Dual J-K Flip-Flop	8-13
MB74LS153M	LS153	SN74LS153N	Dual 4-to-1 Data Selector/Multiplexer	8-23
None	LS161	SN74LS161N	4-bit Binary Counter	8-15
MB74LS164M	LS164	SN74LS164N	8-bit Shift Register	8-17
MB74LS174M	LS174	SN74LS174N	Hex D-Type Flip-Flop	8-18
MB74LS175M	LS175	SN74LS175N	Quad D-Type Flip-Flop	8-18
None	LS191	SN74LS191N	4-bit Up/Down Counter	8-24
None	LS279	SN74LS279N	Quad S-R Latch	8-12
None	LS283	SN74LS283N	4-bit Full Adder Fast Carry	8-26
MB14601C	14601		Linear Motor Control	8-27

Note: Direct replacement is a device of Texas Instruments Inc.

8.3.2 ECL IC Interchangeability

Table 8-3-2 ECL Interchangeability

FUJITSU	Direct	Functions	Page No.
Type No.	Replacement		
MB10102C	MC10102L	Quad 2-input NOR	8-29
MB10106C	MC10106L	Triple 4-3-3 NOR	8-29
MB10115C	MC10115L	Quad Line Reciever	8-30
MB10116C	MC10116L	Triple Line Receiver	8-30
MB10124C	MC10124L	Quad TTL to ECL Translator	8-31
MB10131C	MC10131L	Dual D Flip-Flop	8-32

Note: Direct replacement is a device of MOTOROLA Semiconductor Product Inc.

8.3.3 Linear IC Interchangeability

Table 8-3-3 Linear IC Interchangeability

FUJITSU		Direct Replacement		Functions	Page No.
Type No.	Marking	1st	2nd		
MB3607M	A1458	MC1458 (MOTOROLA)		Operational Amplifier	8-33
MB4002M	A4002			Voltage Comparator	8-33
	A610	μPC610D (NEC)	DAC02 (DM)	10-bit D/A Converter	8-34
	A311	μPC271C (NEC)	LM311 (NS)	Voltage Comparator	8-35
	A1590	MC1590G (MOTOROLA)		AGC Amplifier	8-36
	A201	DG201BK (SILICO)		Quad Analog Switch	8-36
	3450	MC3450L (MOTOROLA)		Quad Line Receiver	8-37
	75108A	SN75108AN (TI)		Dual Line Receiver with Open Collector	8-37
	75110	SN75110AN (TI)		Dual Line Driver	8-37

Notes: 1. NEC is Nippon Electric Co., Ltd.
2. MOTOROLA is MOTOROLA Semiconductor Product Inc.
3. NS is National Semiconductor Corp.
4. PM is Precision Monolithics Incorporated.
5. SILICO is Siliconix Incorporated.
6. TI is Texas Instruments Inc.

8.3.4 FUJITSU Analog Master Slice IC

Table 8-3-4 FUJITSU Analog M/S IC

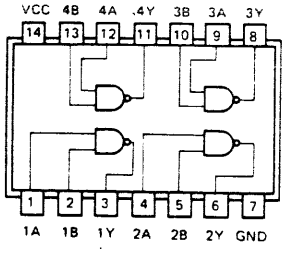
FUJITSU		Direct Replacement	Functions	Page No.
Type No.	Marking			
MB4301C	A4301		Differential Amplifier	8-38
MB4302C	A4302		Head Selection Circuit	8-38
MB4303C	A4303		AGC Amplifier	8-39
MB4305C	A4305		Write Amplifier	8-39
MB4311C	A4311		Charge Pump	8-40
MB4316C	A4316		R/W Bus Switch	8-40

Note: They are all original IC's made by FUJITSU.

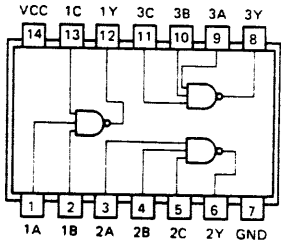
8.4 IC DETAIL

8.4.1 TTL Detail

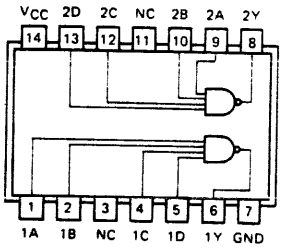
1) MB400M (SN7400N)
MB74S00M (SN74S00N)
MB74LS00M (SN74LS00N)
Quadruple 2-Input
Positive NAND Gates
Positive Logic
$Y = \overline{A \cdot B}$



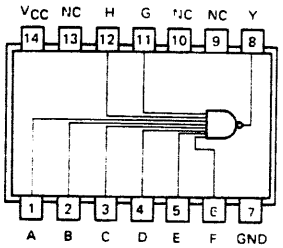
2) MB401M (SN7410N)
MB74S10M (SN74S10)
MB74LS10M (SN74LS10N)
Triple 3-Input
Positive NAND Gates
Positive Logic
$Y = \overline{A \cdot B \cdot C}$



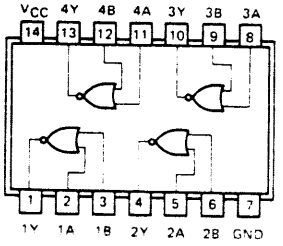
3) MB402M (SN7420N)
MB74S20M (SN74S20N)
MB74LS20M (SN74LS20N)
Dual 4-Input
Positive NAND Gates
Positive Logic
$Y = \overline{A \cdot B \cdot C \cdot D}$



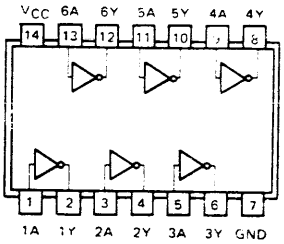
4) MB403M(SN7430N)
MB74LS30M (SN74LS30M)
8-Input
Positive NAND Gates
Positive Logic
$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$



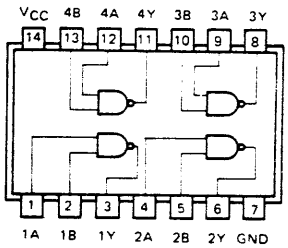
5) MB417M (SN7402N)
MB74LS02M (SN74LS02N)
Quadruple 2-Input
Positive NOR Gates
Positive Logic
$Y = \overline{A + B}$



6) MB418M (SN7404N)
MB74LS04M (SN74LS04N)
Hex Inverters
Positive Logic
$Y = \overline{A}$



7) MB433M (SN7438N)
Quadruple 2-Input
Positive-NAND Buffers
With Open-Collector Outputs
Positive Logic
$Y = \overline{A \cdot B}$

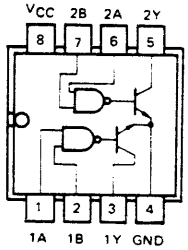


8) MB434M (SN75451B)
Dual Peripheral Positive AND Driver
Positive Logic
$Y = A \cdot B$

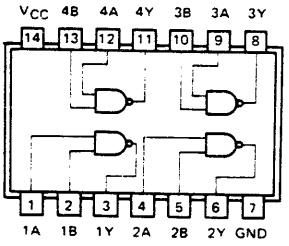
FUNCTION TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

H = high level, L = low level



9) MB435M (SN7437N)
MB74LS37M (SN74LS37N)
Quadruple 2-Input
Positive NAND Buffers
Positive Logic
$Y = \overline{A \cdot B}$

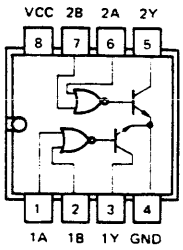


10) MB436M (SN75453B)
Dual Peripheral Positive OR Driver
Positive Logic
$Y = A + B$

FUNCTION TABLE

A	B	Y
L	L	L (on state)
L	H	H (off state)
H	L	H (off state)
H	H	H (off state)

H = high level, L = low level



11) SN75452B

Dual Peripheral Positive NAND Driver

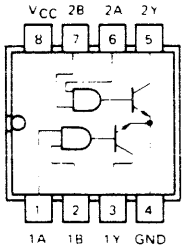
Positive Logic

$Y = \overline{A \cdot B}$

FUNCTION TABLE

A	B	Y
L	L	H (off state)
L	H	H (off state)
H	L	H (off state)
H	H	L (on state)

H = high level, L = low level



12) SN7408N

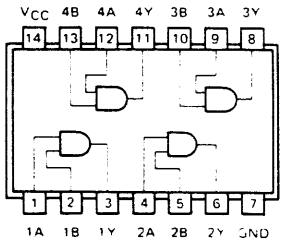
MB74LS08M (SN74LS08N)

Quadruple 2-Input

Positive AND Gates

Positive Logic

$Y = A \cdot B$



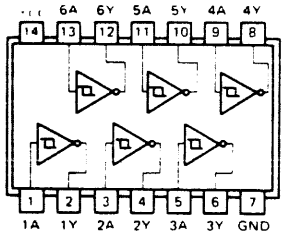
13) SN7414N

Hex Schmitt-Trigger

Inverters

Positive Logic

$Y = \overline{A}$



14) SN7432N

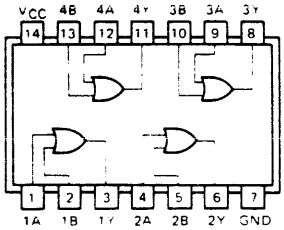
MB74LS32M (SN74LS32N)

Quadruple 2-Input

Positive OR Gates

Positive Logic

$Y = A + B$

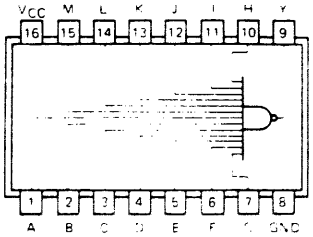


15) SN74S133N

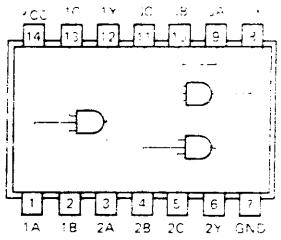
13-Input Positive NAND Gates

Positive Logic

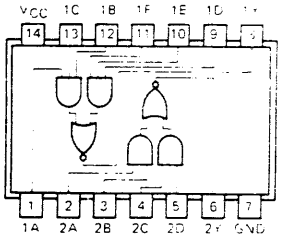
$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$



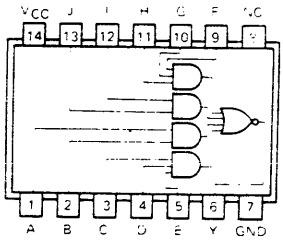
16) MB74LS11M (SN74LS11)
Triple 3-Input
Positive AND Gates
$Y = A \cdot B \cdot C$



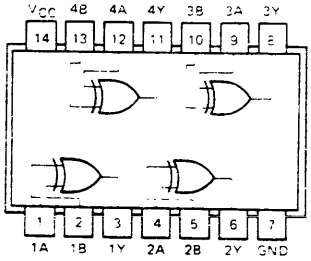
17) MB74LS51M (SN74LS51N))
Dual 2-Wide 2-Input
AND-OR-INVERT Gates
Positive Logic
$1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$
$2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$



18) MB74LS54M (SN74LS54N)
4-Wide
AND-OR-INVERT Gates
Positive Logic
$Y = \overline{(A \cdot B) + (C \cdot D \cdot E) + (F \cdot G \cdot H) + (I \cdot J)}$

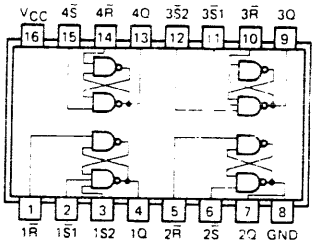


19) MB74LS86M (SN74LS86N)
Quadruple 2-Input
Exclusive OR Gates
Positive Logic
$Y = A + B = AB + AB$



20) MB74LS279M (SN74 LS279N)

Quadruple S-R Latches



FUNCTION TABLE

INPUTS S̄†	R̄	OUTPUT Q
H	H	Q_0
L	H	H
H	L	L
L	L	H*

H = high level

L = low level

Q_0 = the level of Q before the indicated input conditions were established.

* This output level is pseudo stable; that is, it may not persist when the S̄ and R̄ inputs return to their inactive (high) level.

† For latches with double S̄ inputs:

H = both S̄ inputs high

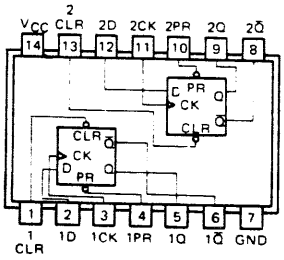
L = one or both S̄ inputs low

21) MB420M (SM7474N)
MB74LS74M (SN74LS74N)

Dual D Type Positive Edge Triggered Flip-Flop with Preset and Clear

FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$



H = high level (steady state), L = low level (steady state), X = irrelevant

⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

↑ = transition from low to high level, ↓ = transition from high to low level

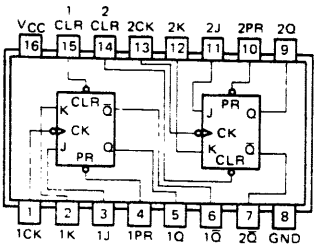
Q_0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

22) SN74S112N

Dual J-K Negative Edge Triggered Flip-Flop with Preset and Clear



FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

H = high level (steady state), L = low level (steady state), X = irrelevant

↓ = transition from high to low level

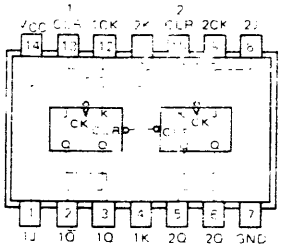
Q_0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition of the clock.

* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

23) MB74LS107M (SN74LS107N)

Dual J-k Mater Slave Flip-Flop with clear



FUNCTION TABLE

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	⎍	L	L	Q_0	$\bar{Q}_0$
H	⎍	H	L	H	L
H	⎍	L	H	L	H
H	⎍	H	H	TOGGLE	

H = high level (steady state), L = low level (steady state), X = irrelevant

↓ = transition from high to low level

⎍ = high-level pulse; data inputs should be held constant while clock is high; data is transferred to output on the falling edge of the pulse.

Q_0 = the level of Q before the indicated input conditions were established.

TOGGLE: Each output changes to the complement of its previous level on each active transition (pulse) of the clock.

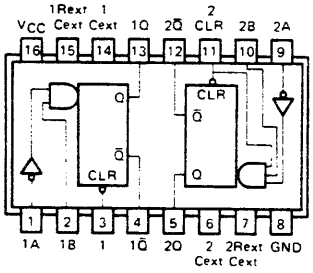
* This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

24) MB440M (SN74123N)

Dual Retriggerable Monostable Multivibrator with Clear

FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑	⎍	⎍
H	↓	H	⎍	⎍
↑	L	H	⎍	⎍



This monolithic TTL retriggerable monostable multivibrator features d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provides overriding direct clear inputs. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse terminated, the output pulses may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C. The output pulse is primarily a function of the external capacitor and resistor.

For Cext > 1000pF, the output pulse width (tw) is defined as:

$$tw = 0.32RtCext\left(1 + \frac{0.7}{Rt}\right)$$

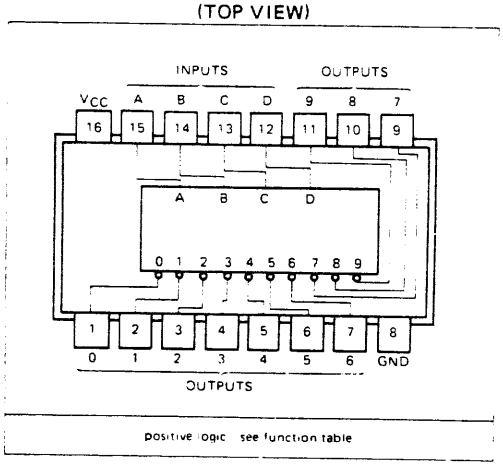
tw : ns

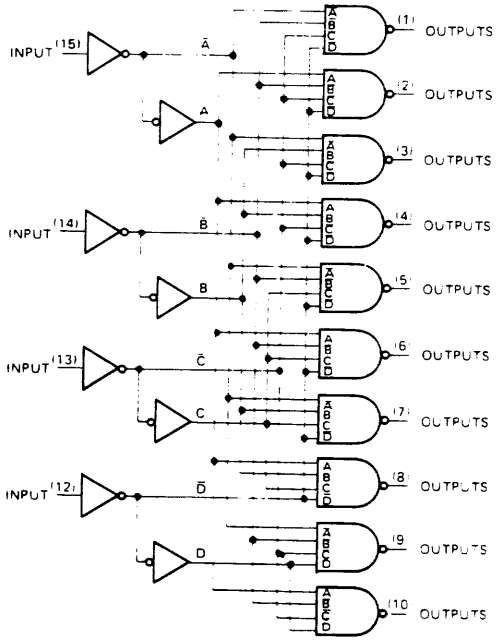
Rt : kohms

Cext : pF

25) MB442M (SN7442N)
BCD-to-Decimal Decoder

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.





BCD-TO-DECIMAL DECODERS

FUNCTION TABLE

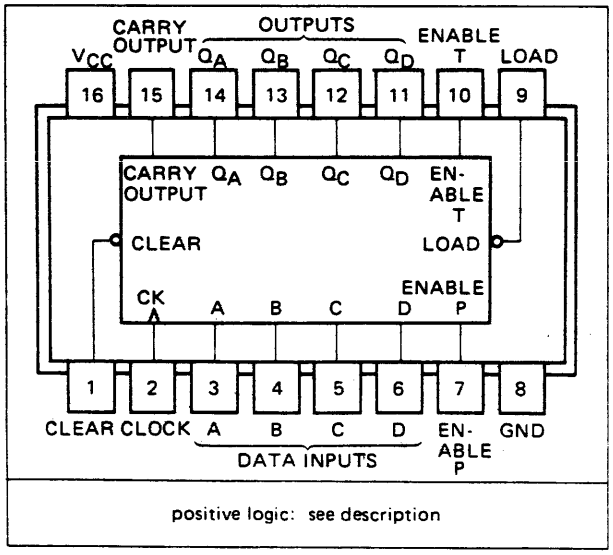
No.	BCD INPUT				DECIMAL OUTPUT									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high level, L = low level

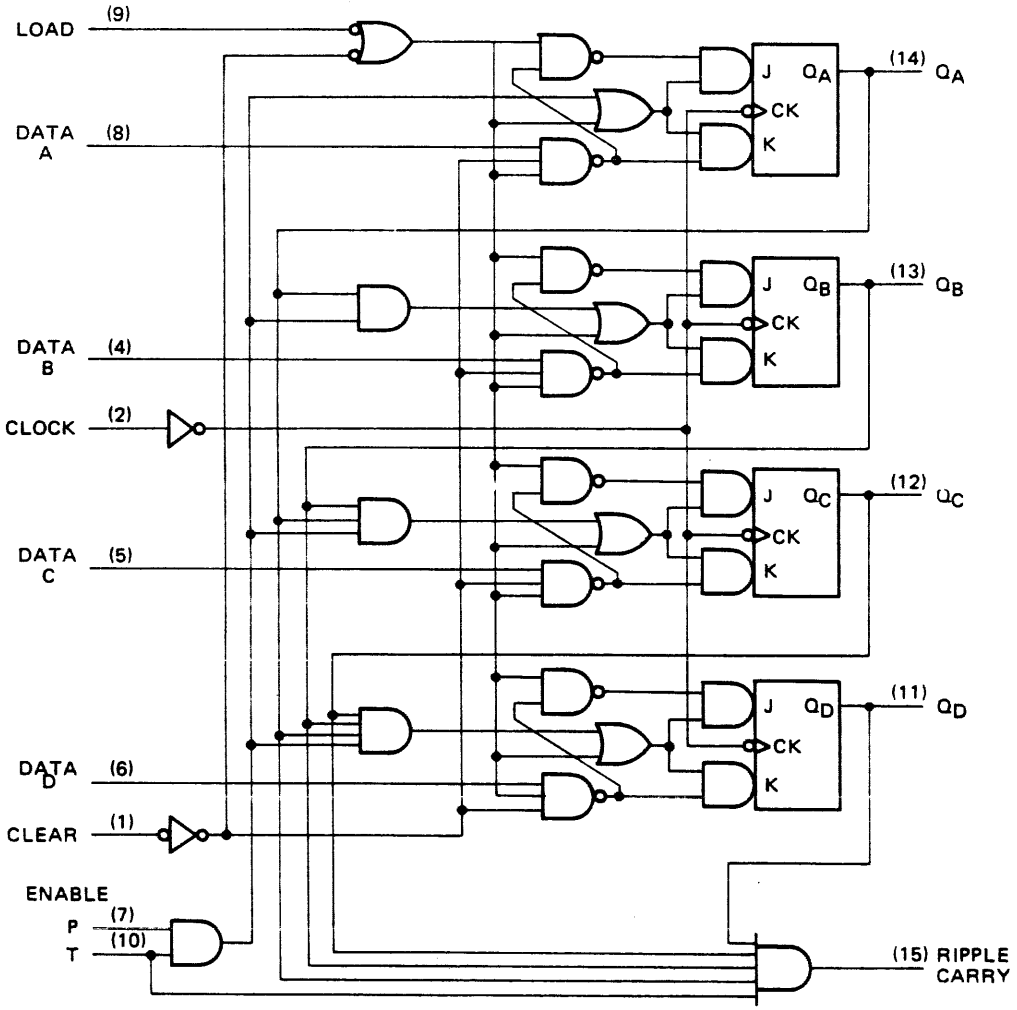
26) MB450M (SN74161N), SN74LS161N
Synchronous 4-bit Counter with Direct Clear

This synchronous, presettable counter features an internal carry look-ahead for application in high-speed counting schemes. Synchronous operation is provided by having all flip-flop clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the set-up data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function for the SN74161N is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of the clock, load, or enable inputs. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously clear the counter to 0000 (LLLL).



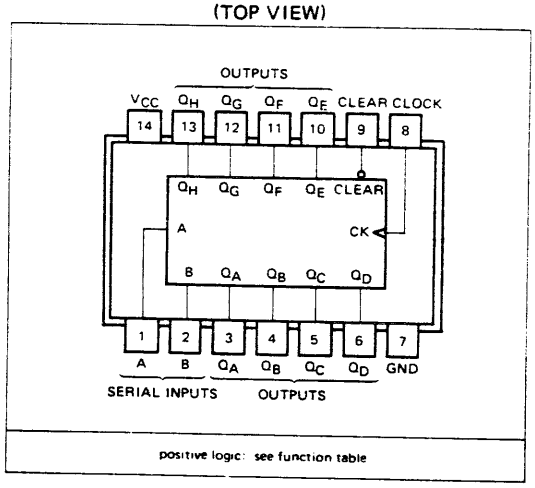
Functional block diagrams



27) SN74164N, MB74LS164M (SN74LS164N)
8-Bit Parallel-Out Serial Shift Registers

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input. All inputs are diode-clamped to minimize transmission-line effects.

(TOP VIEW)

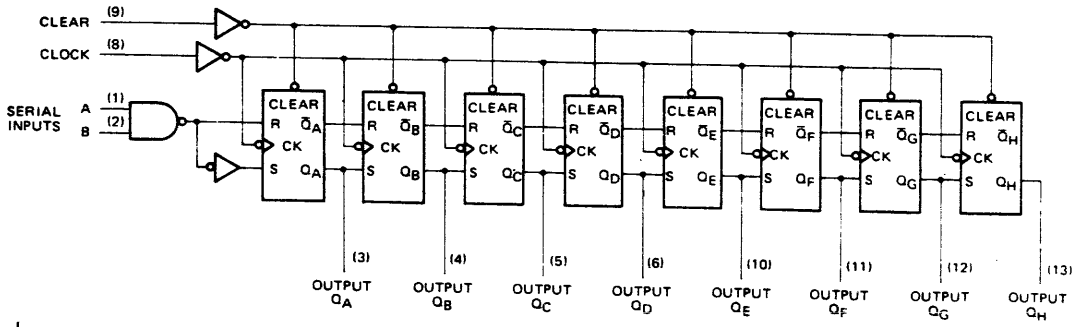


FUNCTION TABLE

INPUTS				OUTPUTS		
CLEAR	CLOCK	A	B	Q_A	Q_B . . .	Q_H
L	X	X	X	L	L	L
H	L	X	X	Q_{A0}	Q_{B0}	Q_{H0}
H	↑	H	H	H	Q_{An}	Q_{Gn}
H	↑	L	X	L	Q_{An}	Q_{Gn}
H	↑	X	L	L	Q_{An}	Q_{Gn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transitions)
↑ = transition from low to high level.
Q_{A0}, Q_{B0}, Q_{H0} = the level of Q_A, Q_B, or Q_H, respectively, before the indicated steady-state input conditions were established.
Q_{An}, Q_{Gn} = the level of Q_A or Q_G before the most-recent ↑ transition of the clock; indicates a one-bit shift.

Functional block diagram



. . . dynamic input activated by transition from a high level to low level

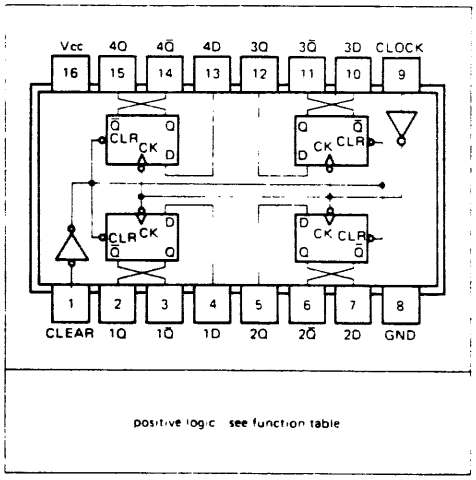
28) SN74175N
MB74LS175M (SN74LS175N)
Quadruple D-Type Flip-Flop

MB74LS174M (SN74LS174N)
Hex D-Type Flip-Flop

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. All have a direct clear input, and the '175, 'LS175, and feature complementary outputs from each flip-flops.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

'175, 'LS175
(TOP VIEW)

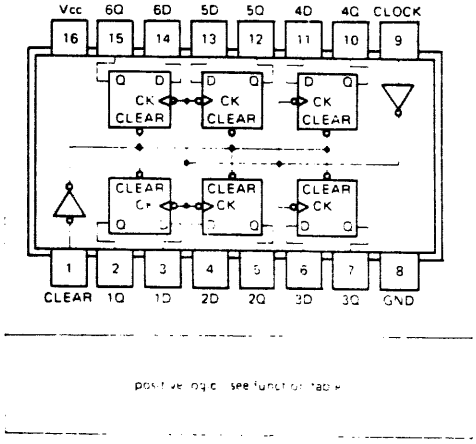


FUNCTION TABLE
(EACH FLIP-FLOP)

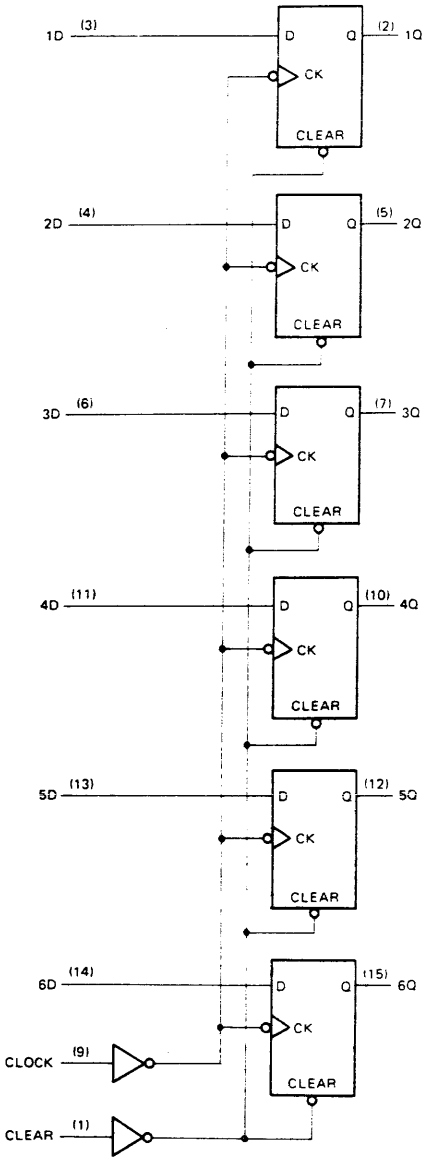
INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	$\bar{Q}$†
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\bar{Q}_0$

H = high level (steady state)
L = low level (steady state)
X = irrelevant
↑ = transition from low to high level
Q_0 = the level of Q before the indicated steady-state input conditions were established.
† = '175, 'LS175, only

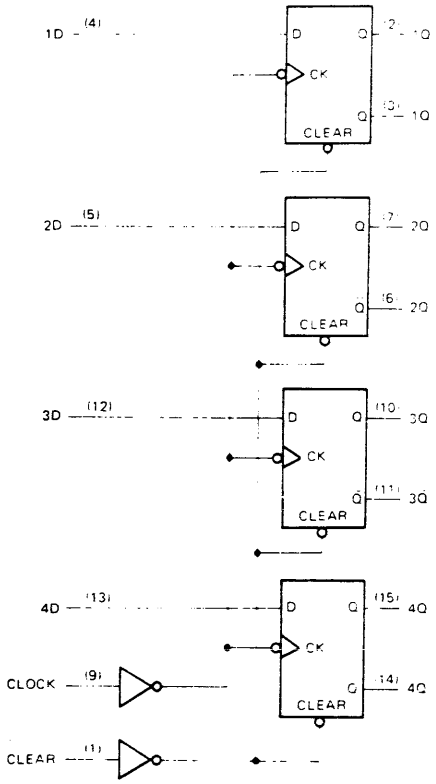
'LS174
(TOP VIEW)



'LS174,



'175, 'LS175,



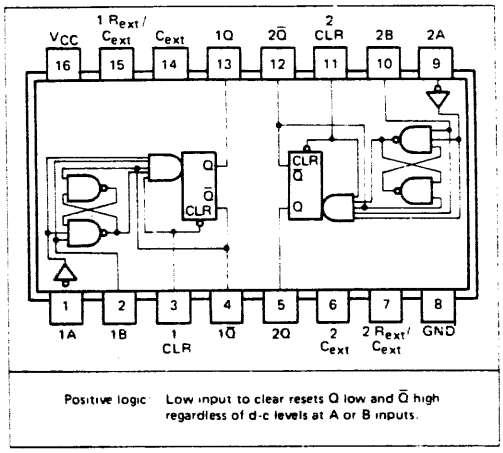
. . . dynamic input activated by transition from a high level to a low level.

29) SN74221N
Dual Monostable Multivibrator
with Schmitt-Trigger Input

The SN74221N are monolithic dual multivibrators with performance characteristics virtually identical to those of the SN74121N. Each multivibrator features a negative-transition-triggered input and a positive-transition-triggered input either of which can be used as an inhibit input.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry (TTL hysteresis) for B input allows jitter-free triggering from inputs with transition rates as slow as 1 volt/second, providing the circuit with excellent noise immunity of typically 1.2 volts. A high immunity to Vcc noise of typically 1.5 volts is also provided by internal latching circuitry.

(TOP VIEW)



Positive logic: Low input to clear resets Q low and Q̄ high regardless of d-c levels at A or B inputs.

FUNCTION TABLE
(EACH MONOSTABLE)

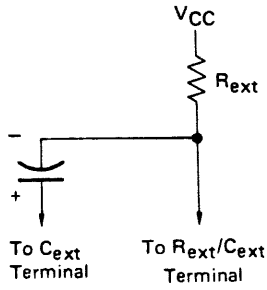
INPUTS			OUTPUTS	
CLEAR	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	0	⎍	⎎
H	↓	H	⎍	⎎
↑	L	H	⎍	⎎

Also see description and switching characteristics

The output pulse width (tw) is defined as:

$$tw = 0.7 R_{ext} C_{ext}$$

tw ; ns, rext : kohms, Cext : pf



TIMING COMPONENT CONNECTIONS

30) SN74S124N
Dual Voltage Controlled Oscillators

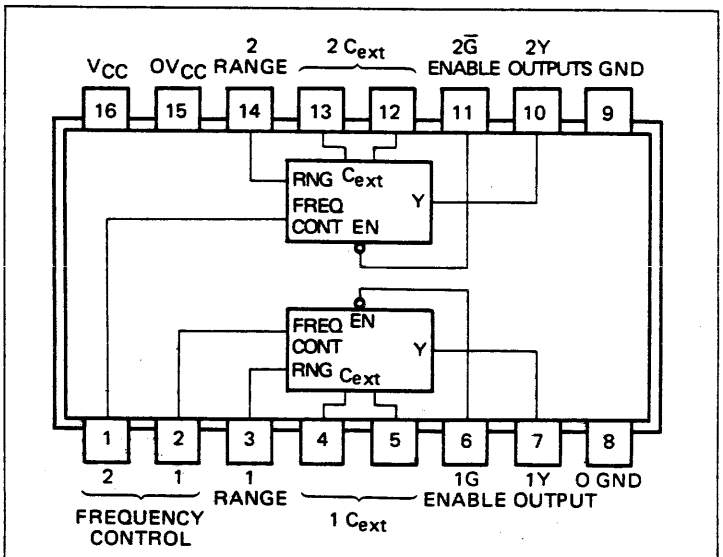
The 'S124 feature two independent voltage-controlled oscillators (VCO) in a single monolithic chip. The output frequency of each VCO is established by a single external component, either a capacitor or a crystal, in combination with two voltage-senstive inputs, one for frequency range and one for frequency control. These inputs can be used to vary the output frequency as shown under typical characteristics for the 'S124. These highly stable oscillators can be set to operate at any frequency typically between 0.12 hertz and 85 megahertz. The output frequency can be approximated as follows:

$$f_O = \frac{5 \times 10^{-4}}{C_{ext}}$$

where: f_O = output frequency in hertz

C_{ext} = external capacitance in farads.

(TOP VIEW)



Logic: While the enable input is low, the output is enabled.
While the enable input is high, the output is high.

31) SN74LS85N
4-bit Magnitude Comparators

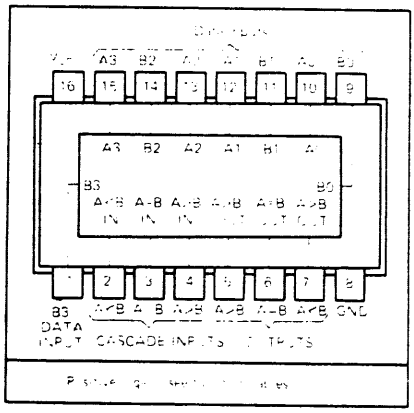
These four-bit magnitude comparators perform comparison of straight binary and straight BCD (8-4-2-1) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A > B, A < B, and A = B outputs of a stage handling less-significant bits are connected to the corresponding A > B, A < B, and A = B inputs of the next stage handling more-significant bits.

FUNCTION TABLES

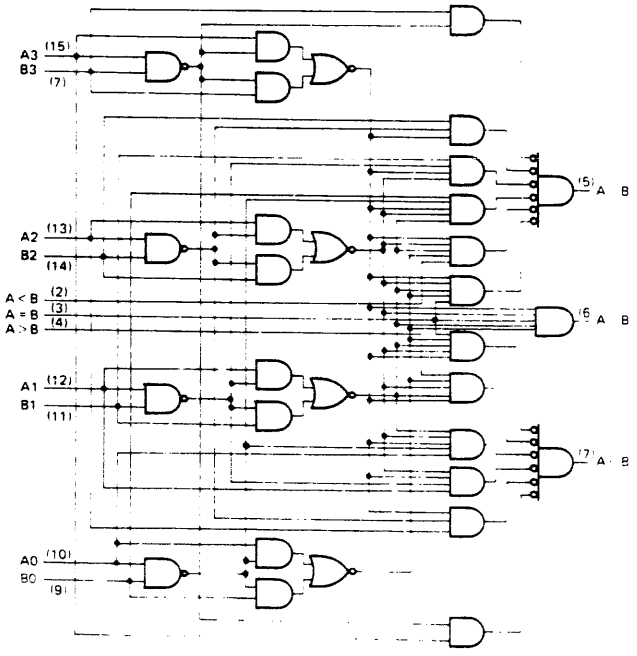
COMPARING INPUTS			CASCADING INPUTS				OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B2	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	X	X	H	L	L	H
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	H	L	L	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	L	H	H	L

H = high level, L = low level, X = irrelevant

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)



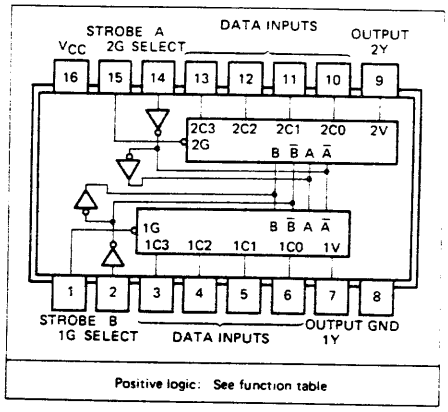
Functional block diagrams



32) MB74LS153M (SN74LS153N)
Dual 4-Line-to-Line Data Selectors/Multiplexers

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-inverter gates. Separate storobe inputs are provided for each of the two four-line sections.

(TOP VIEW)



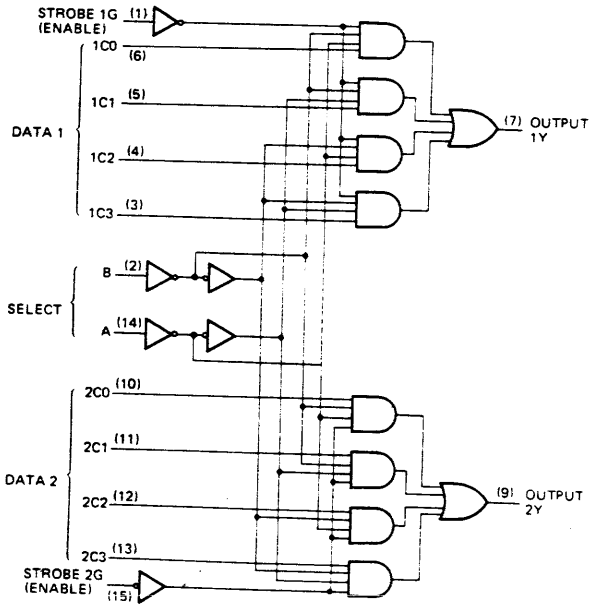
Positive logic: See function table

FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L

Select inputs A and B are common to both sections
H = high level, L = low level, X = irrelevant

Functional block diagram

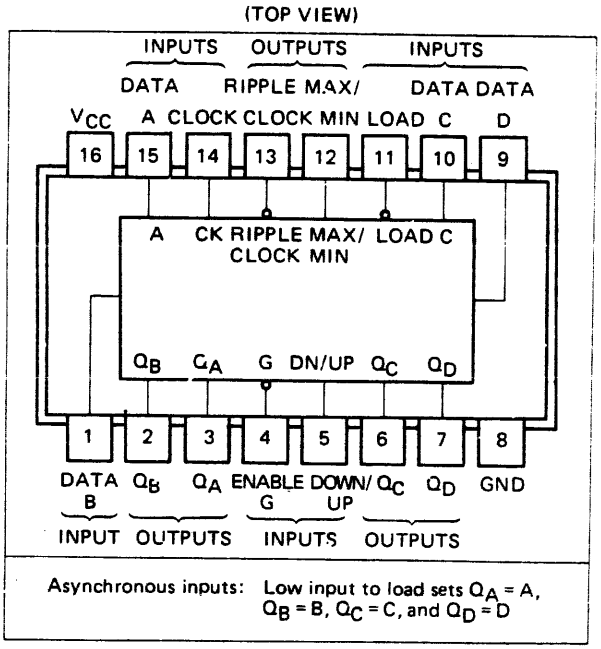


33) SN74LS191N
Synchronous UP/DOWN Counters
with DOWN/UP Mode Control

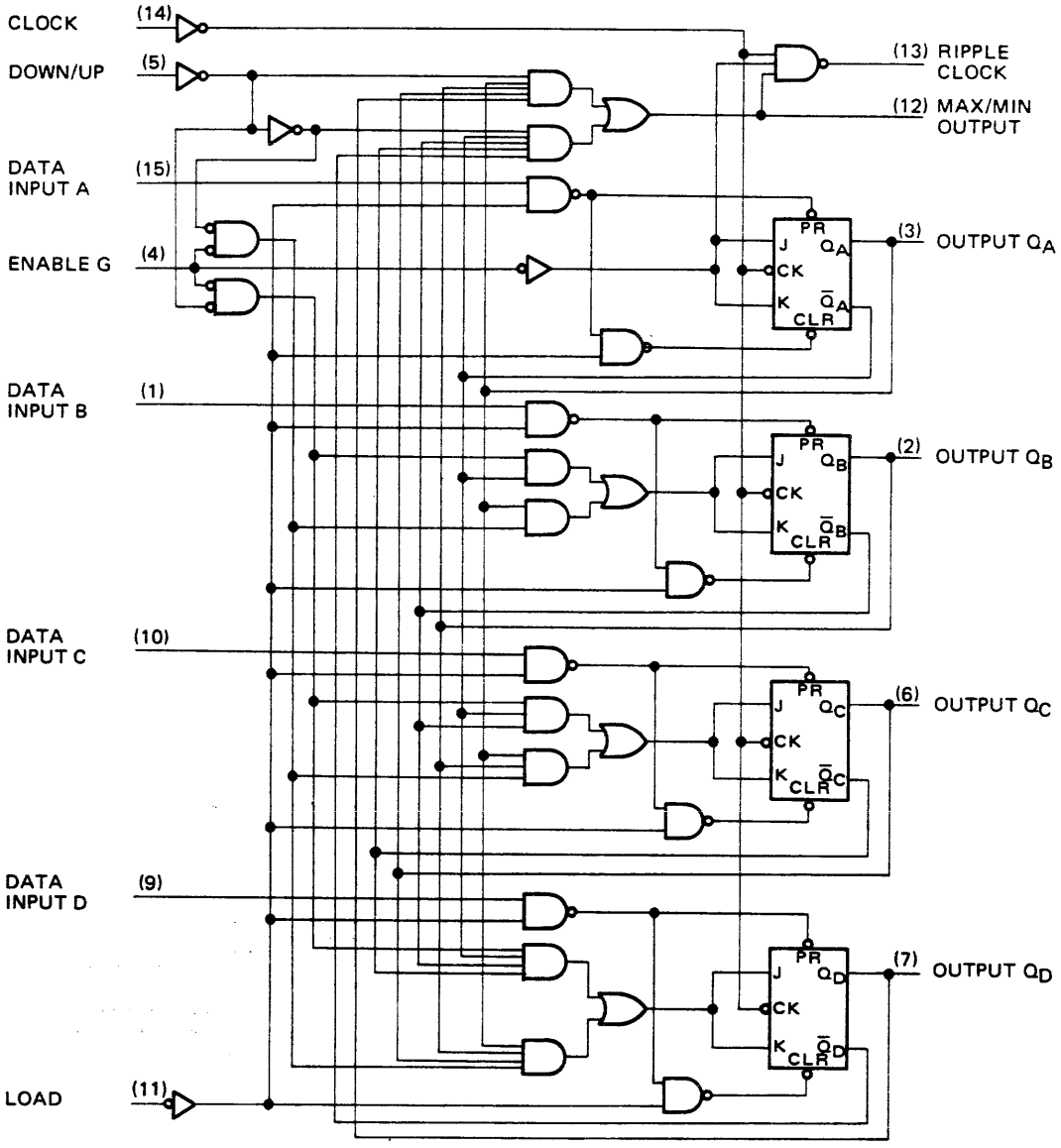
The SN74LS191N is synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The SN74LS191N is 4-bit binary counters. Synchronous operation is provided by having all flip-flop clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flop are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the level of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to either level by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the level of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the present inputs.



Functional block diagram

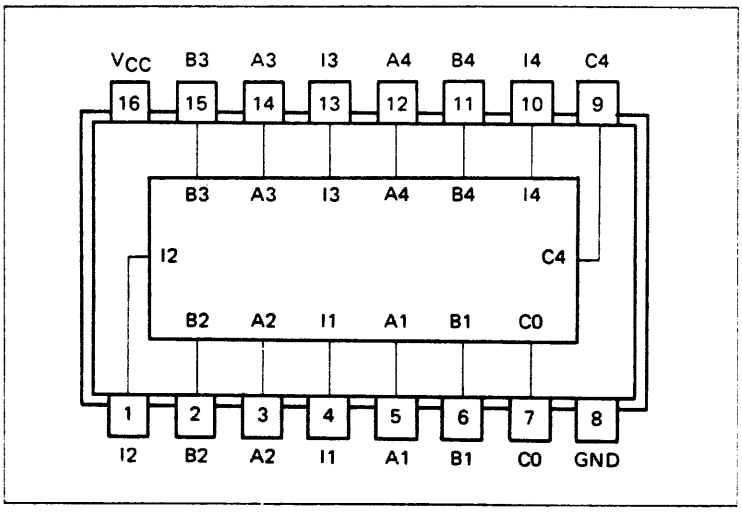


34) SN74LS283N
4-Bit Binary Full Adders with Fast Carry

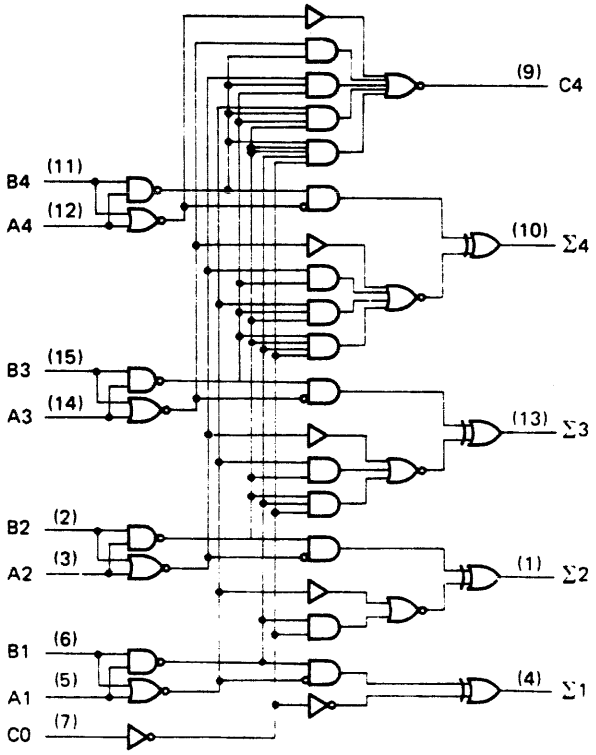
These improved 4-Bit full adders/subtractors feature full look-ahead across four bits to generate the carry term in typically 10 nanoseconds. This capability provides the system designer with partial look-ahead performance at the economy and reduced package count of a ripple-carry implementation.

These full adders are designed so that levels of the input and output, including the carry, are in their true form. Thus the end-around carry is accomplished without the need for level inversion.

(TOP VIEW)



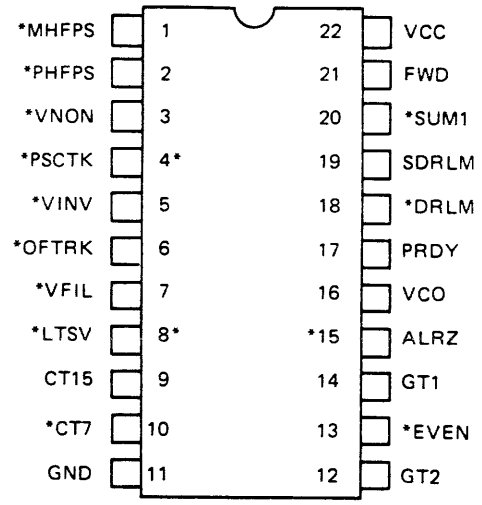
Functional block diagram



35) MB14601C
Linear Motor Control

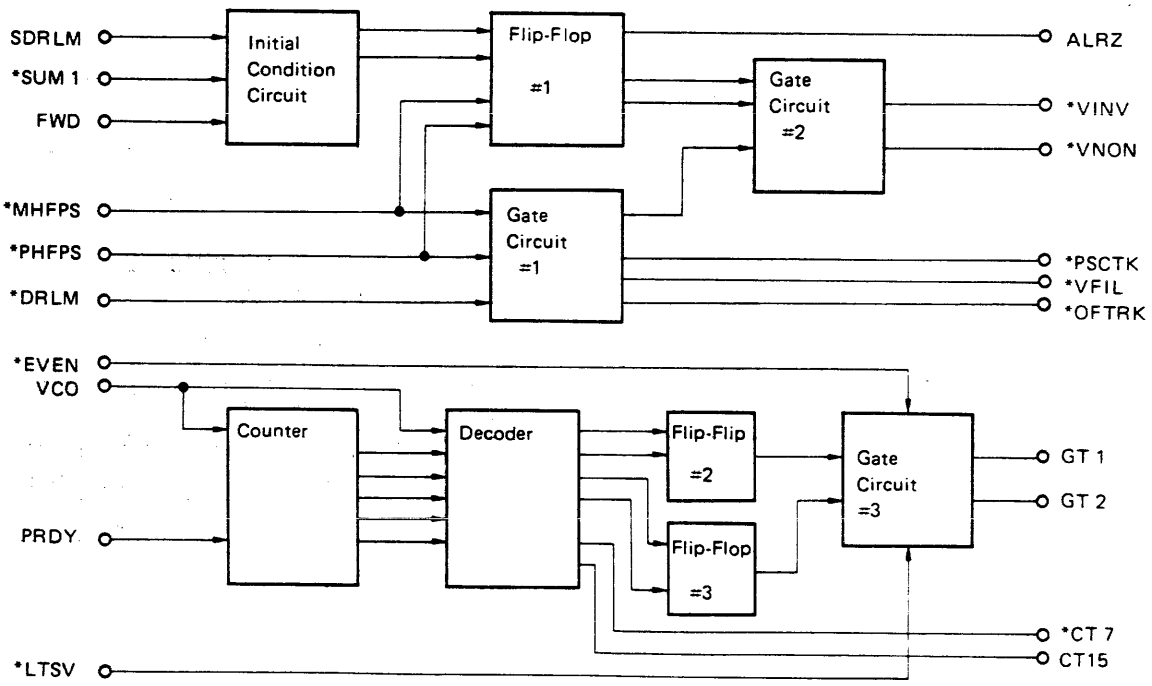
CONNECTION DIAGRAM

(TOP VIEW)



* NOT USED

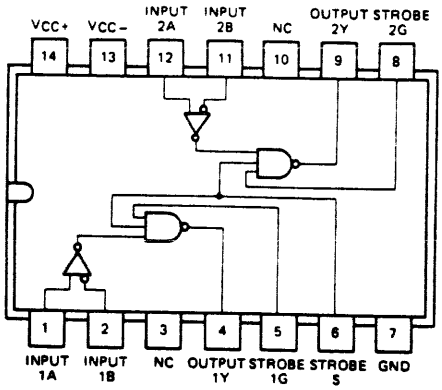
BLOCK DIAGRAM



36) SN75107AN
Dual Line Receivers

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES		OUTPUT Y
	G	S	
$V_{ID} \geq 25mV$	L or H	L or H	H
$-25mV < V_{ID} < 25mV$	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25mV$	L or H	L	H
	L	L or H	H
	H	H	L

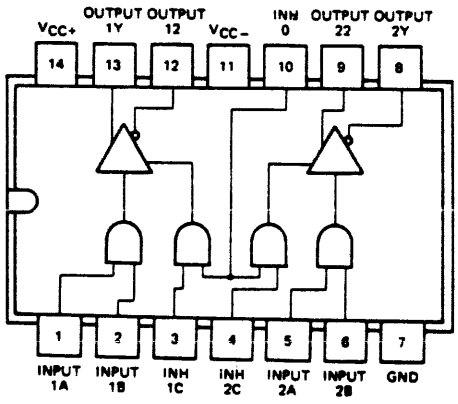


37) SN75110N
Dual Line Drivers

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state.
High output represents the off state.



8.4.2 ECL Detail

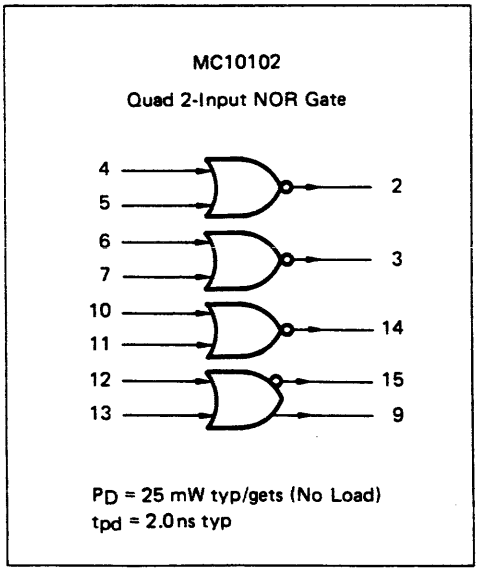
1) MB10102C (MC10102L)
   Quad 2-Input NOR Gates

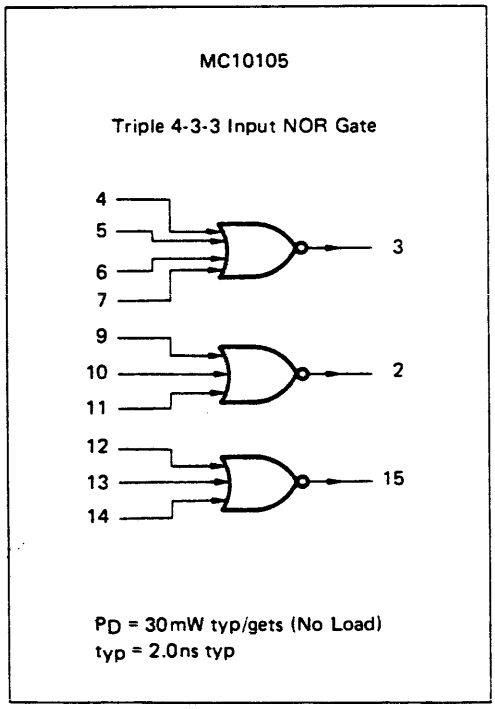
2) MD10106C (MC10106L)
   Triple 4-3-3 Input NOR Gates

These gates are low power (25mW), high speed (2.0ns) standard MECL logic functions. High impedance input pulldowns allow high dc and ac fan-out and eliminate the need to tie unused inputs to an external supply. The open emitter output allow flexibility in the selection of termination techniques and minimize the power requirements when driving transmission lines.

Wire-ORing of outputs is available with the open emitter outputs. These functions are used in control, bussing, and communications in high speed central processer, high speed peripherals, digital communications systems, minicomputer, and instruments.

The MB10102C is commonly used for control, and for bussing data by using the Wire-ORing capability of the basic ECL gate.

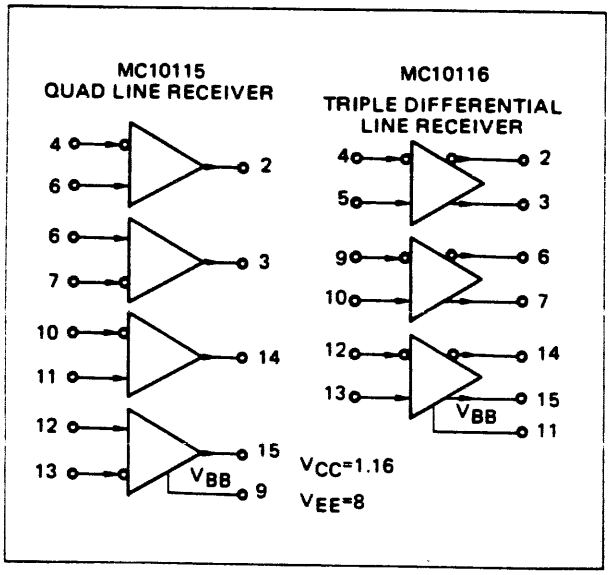




3) MB10115C (MC10115L)
   Quad Line Receiver
4) MB10116C (MC10116L)
   Triple Line Receiver

The line receivers are essentially very high speed linear differential amplifiers with standard ECL outputs. Maximum flexibility is allowed with the open-emitter outputs. Active current sources provide the line receivers with excellent common mode noise rejection. The functions are useful as both digital and linear parts in high speed central processors, minicomputers, peripheral controllers, digital communication systems, and testing and instrumentation systems.

The MB10115C is a quad line receiver with a single output per gate while the MB10116C is a triple line receiver with complementary outputs. Both functions have a V_{BB} reference provided to make the devices useful as Schmitt triggers and to permit them to be used in other applications where a stable reference voltage is necessary. They are also recommended for MOS to ECL interfacing and are used as sense amplifiers for MOS RAM's.

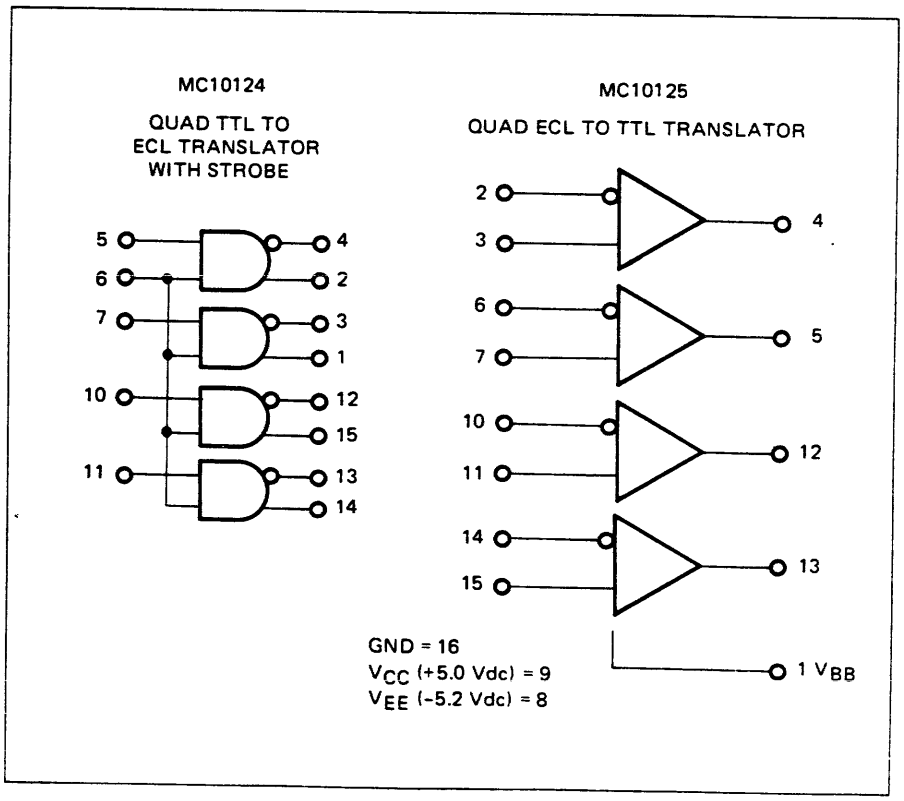


5) MB10124C (MC10124L)
Quad TTL to ECL Translator

6) MB10125C (MC10125L)
Quad ECL to TTL Translator

The 10124 and 10125 are quad translators for interfacing data and control signals between a high speed ECL section and low speed saturated logic sections of digital equipment. The 10124 has standard TTL inputs and standard ECL, complementary, open-emitter outputs. The 10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. These devices are useful in computers, instrumentation, peripheral controllers, test equipment and digital communication systems.

Power supply requirements are ground, +5Vdc and -5.2Vdc. Propagation delay of the 10124 is typically 5ns. The outputs are identical to those of a standard ECL gate. An advantage of this gate is that the translation can be done in the TTL equipment and then the information can be transmitted, via balanced twisted pair, to the ECL equipment. This isolates the ECL logic from the noisy TTL environment. The 10125 has a typical propagation delay of 5ns with a fanout of 10 TTL loads. The high speed of both of these functions makes them ideal for high speed instrumentation systems and digital communication systems.

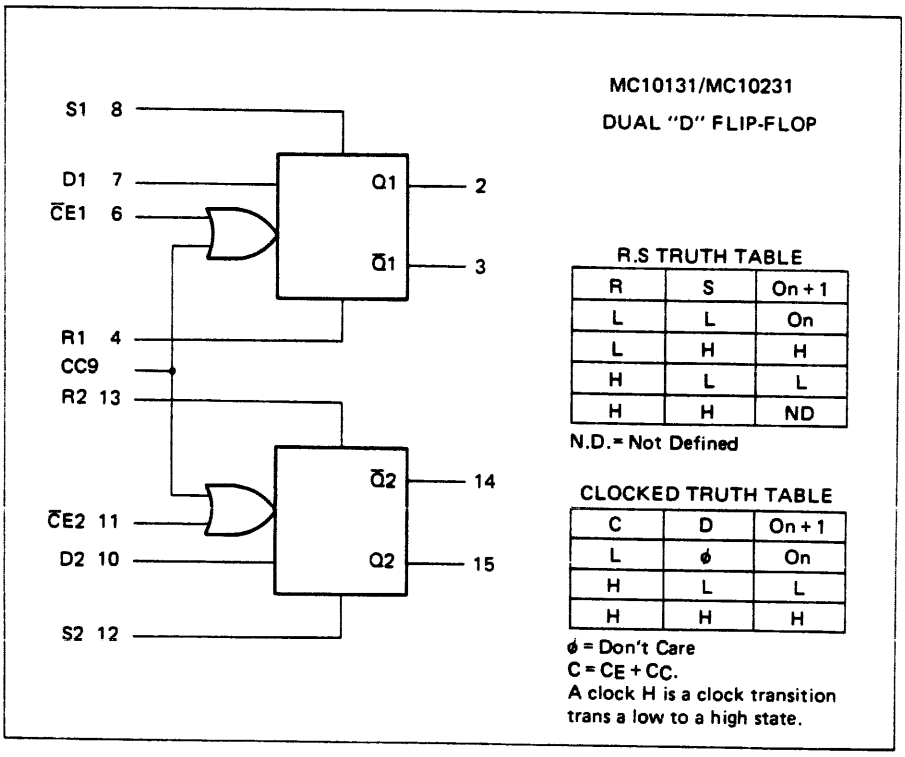


7) MB10131C (MC10131L)
Dual D-Type Flip-Flop

Dual flip-flops are standard ECL 10,000 storage and counting functions. The inputs incorporate high impedance pulldown resistors. Emitter-follower outputs are left open for maximum flexibility and minimum power dissipation. These functions are very useful for control and storage in high speed digital communication systems, instrumentation and test equipment, high speed central processors, high speed peripheral controllers and mini-computers.

The 10131 is high speed dual D master slave flip-flop with asynchronous set and reset inputs, true and complement outputs.

Set and reset inputs override the clock for asynchronous operation of the 10131.



R.S TRUTH TABLE

R	S	On + 1
L	L	On
L	H	H
H	L	L
H	H	ND

N.D. = Not Defined

CLOCKED TRUTH TABLE

C	D	On + 1
L	ϕ	On
H	L	L
H	H	H

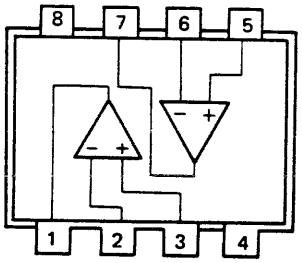
ϕ = Don't Care
C = CE + CC.
A clock H is a clock transition trans a low to a high state.

8.4.3 Linear IC Detal

1) MB3607M (MC1458C)
Dual Operational Amplifier

The MB3607M is designed for use as a summing amplifier integrator, or amplifier with operating characteristics as a function of the external feedback components.

TOP VIEW

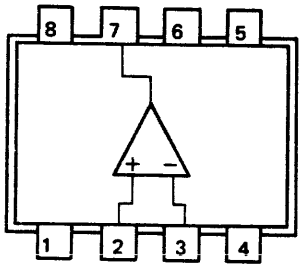


1: OUTPUT 1
2: INPUT 1 (-)
3: INPUT 1 (+)
4: V^-
5: INPUT 2 (+)
6: INPUT 2 (-)
7: OUTPUT 2
8: V^+

2) MB4002M
High Speed Differential Comparator

The MB4002M is a Differential Voltage Comparator intended for applications requiring high accuracy and fast response times. The device is useful as a variable threshold Schmitt trigger, a pulse height discriminator, a voltage comparator in high-speed A/D converters, a memory sense amplifier or a high noise immunity line receiver. The output of the comparator is compatible with all integrated logic forms.

TOP VIEW



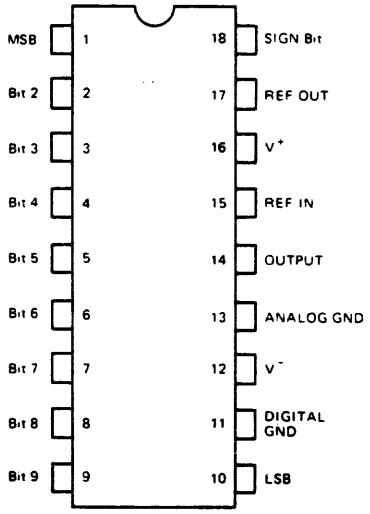
1: GND
2: INPUT (+)
3: INPUT (-)
4: V^-
5: NC
6: NC
7: OUTPUT
8: V^+

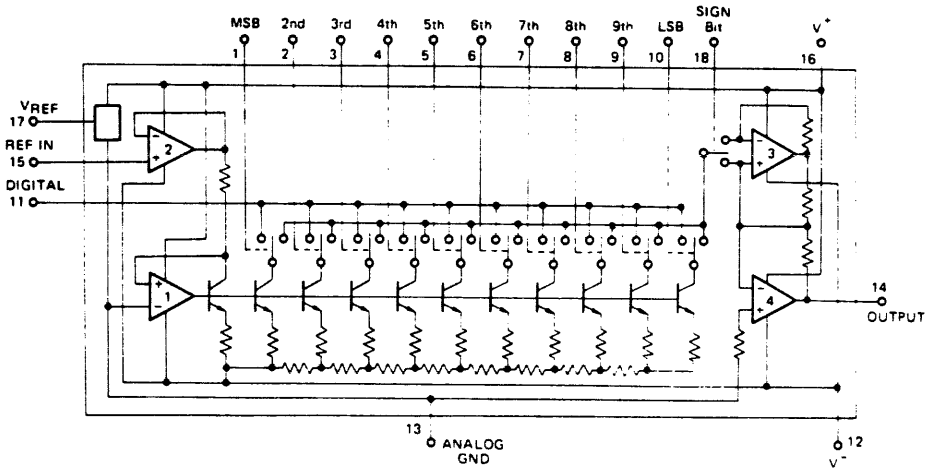
3) μPC610D

10 bit D/A Convertor

The μPC610D is a complete 10bit plus sign D/A convertor. All elements of a complete sign/magnitude DAC are included-precision voltage reference, current steering logic, current sources, R-2R resister network, logic controlled polarity switch and high speed internally compensated output of amp. The wide power supply range, low power consumption, choice of full scale output voltages and sign/magnitude coding assure utility in a wide range of applications.

Connection Diagram
(TOP VIEW)



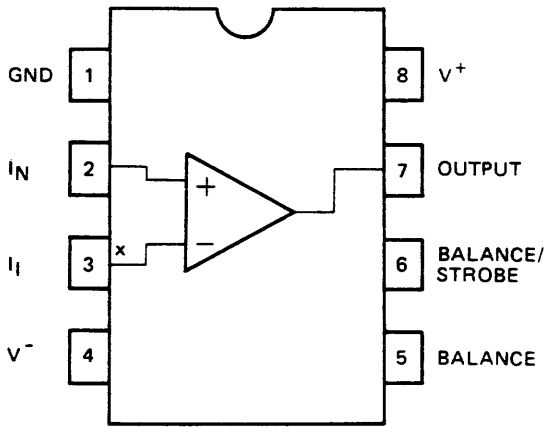


4) μpc271C

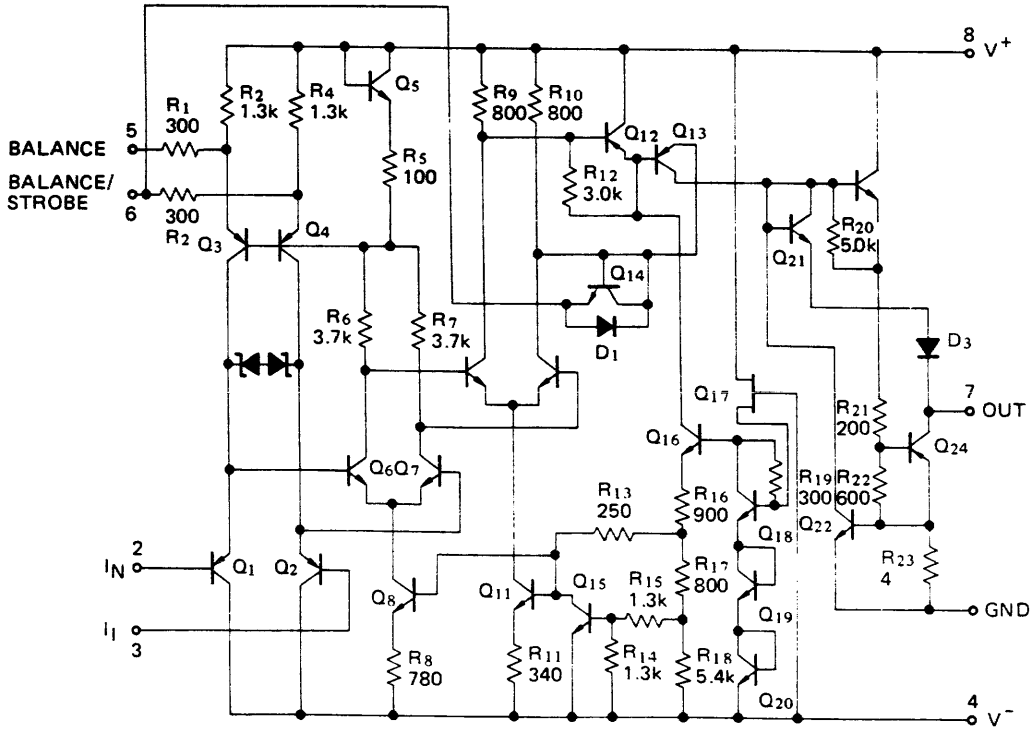
Voltage Comparator

This is a single high-speed voltage comparator. This device is designed to operate from a wide range of power supply voltage, including ± 15V supplies for operational amplifiers and +5 supplies for logic systems. The output level is compatible with most DTL, TTL, and MOS circuits. This comparator is capable of driving Lamps or relays and switching voltage up to 50V at 50mA. All inputs and outputs can be isolated from system ground. The output can drive loads referenced to ground, Vcc+, Vcc-. Offset balancing and strobe capability are available and the output can be wire-OR connected. If the strobe input is low, the output will be in the off state regardless of the differential input.

Connection Diagram
(TOP VIEW)

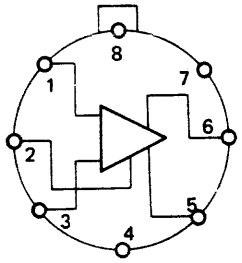


Equivalent Circuit



5) MC1590G
AGC Amplifier

(TOP VIEW)

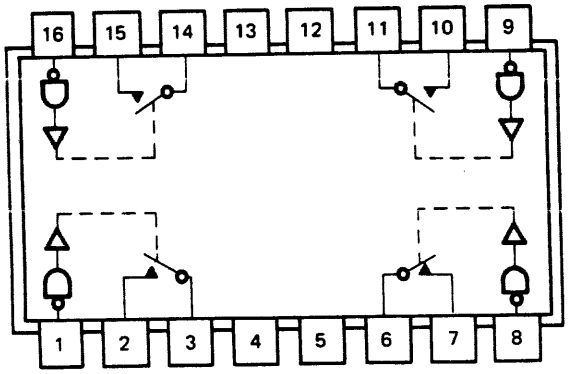


1: INPUT (-)
2: VAGC
3: INPUT (+)
4: CASE
5: OUTPUT (+)
6: OUTPUT (-)
7: V+
8: SUBSTRATE

6) DG201BK
Quad Mono lithic SPST CMOS Analog Switch

The DG201 is a 4-channel single pole signal throw analog switch which employs CMOS technology to insure low and nearly constant ON resistance over the entire analog signal range. The switch will conduct current in either direction with no offset voltage in the ON condition, and block voltages up to 30V peak-to-peak in the OFF condition. The ON-OFF state of each switch is controlled by a driver. With a logic "0" at the input to the driver (0V to 0.8V) the switch will be ON, and a logic "1" (2.4V to 15V) will turn the switch OFF. Switch action is break-before-make.

TOP VIEW



1:	IN1	9:	IN3
2:	D1	10:	D3
3:	S1	11:	S3
4:	V^-	12:	VREF
5:	GND	13:	V^+
6:	S4	14:	S2
7:	D4	15:	D2
8:	IN4	16:	IN2

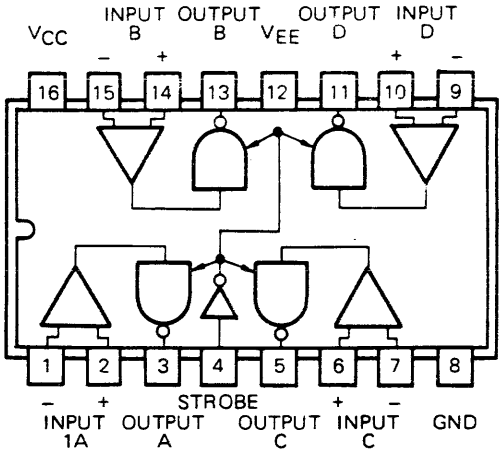
LOGIC	SWITCH
0	ON
1	OFF

7) MC3450L
Quad Line Receivers

TRUTH TABLE

INPUT	STROBE	OUTPUT
$V_{ID} \geq +24mV$	L	H
	H	Z
$-25mV < V_{ID} < +24mV$	L	I
	H	Z
$V_{ID} \leq +24mV$	L	L
	H	Z

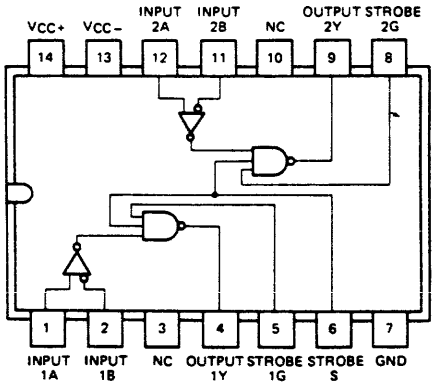
L: Low Logic Stage
H: High Logic State
Z: Third (High Impedance) State
I: Indeterminate State



8) SN75108AN
Dual Line Receivers with Open-collector

TRUTH TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25mV$	L or H	L or H	H
$-25mV < V_{ID} < 25mV$	L or H	L	H
	L	L or H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25mV$	L or H	L	H
	L	L or H	H
	H	H	L

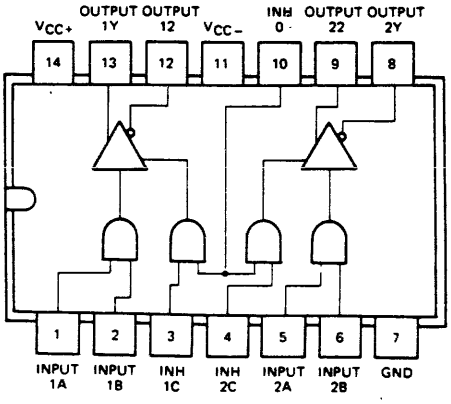


9) SN75110AN
Dual Line Drivers

TRUTH TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
L or H	L or H	L	L or H	H	H
L or H	L or H	L or H	L	H	H
L	L or H	H	H	L	H
L or H	L	H	H	L	H
H	H	H	H	H	L

Low output represents the on state.
High output represents the off state.

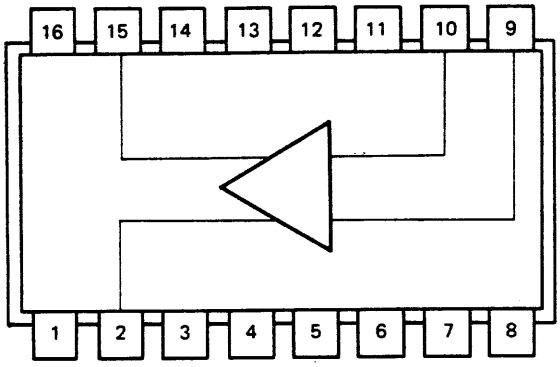


8.4.4 FUJITSU Analog Master Slice IC Detail

1) MB4301C
Differential Amplifier

The MB4301C is a three-stage Differential input, Differential output Amplifier. All stages are gain-selectable with external resistors.

TOP VIEW

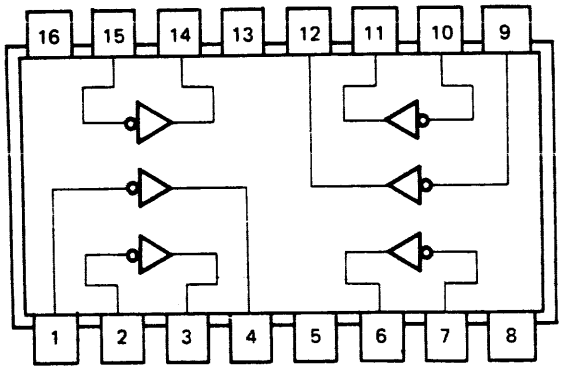


G1A G3A: GAIN
G1B G3B: SELECT
GC : GAIN CHANGE

1: Vcc2
2: OUTPUT2
3: G3A
4: G2A
5: G2B
6: AMP ENABLE
7: NC
8: GND
9: INPUT2
10: INPUT1
11: G1B
12: G1A
13: GC
14: G3B
15: OUTPUT1
16: Vcc1

2) MB4302C
Head Selection Circuit

TOP VIEW



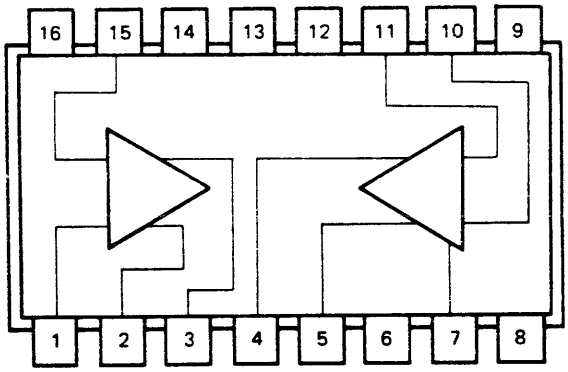
CE: Chip Enable
CD: Detection for Multi selection

1:
2:
3:
4:
5: CE
6:
7:
8: GND
9:
10:
11:
12:
13: CD
14:
15:
16: Vcc

3) MB4303C
AGC Amp

The MB4303C is a Automatic-Gain-Control Amplifier with Differential Inputs and Outputs. It contains another Differential Amplifier.

TOP VIEW

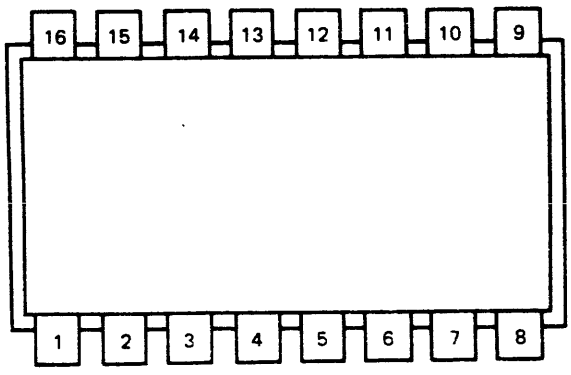


1: INPUT2
2: OUTPUT2
3: OUTPUT2
4: OUTPUT1
5: OUTPUT1
6: VR
7: VAGC
8: VG (GND)
9: Vee
10: INPUT1
11: INPUT1
12: GA
13: GB
14: VBB
15: INPUT2
16: Vcc

4) MB4305C
Write Amplifier

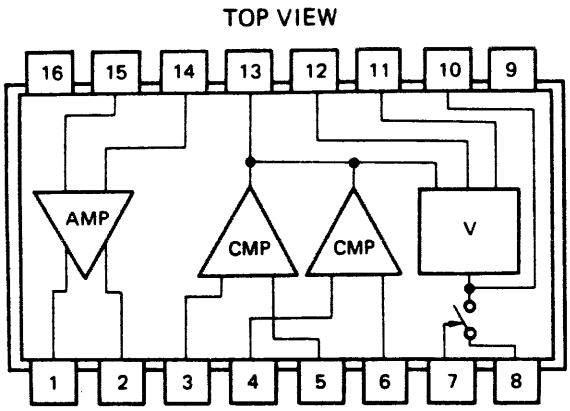
The MB4305C is a Write Amplifier with two write enables (WEN1 and WEN2), AC and DC echo detection output and Current-off circuit in case of power failure.

TOP VIEW



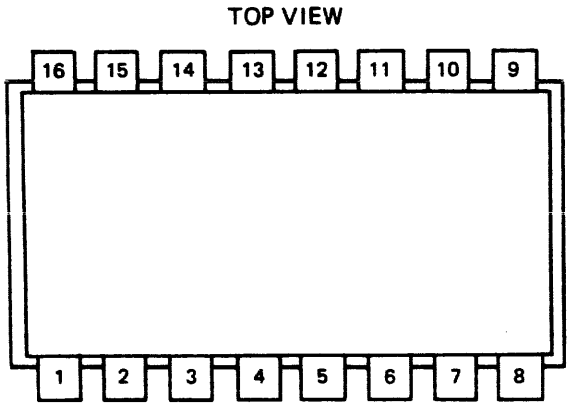
1: VB
2: VALM
3: WEN1
4: WEN2
5: Vcc2
6: DC-ECHO OUTPUT
7: NC
8: GND
9: Vee
10: CEX
11: OUTPUT
12: CURRENT INPUT
13: HD1
14: AC-ECHO OUTPUT
15: HD0
16: Vcc1

5) MB4311C
Charge Pump



1: OUT1
2: OUT1
3: IN2
4: IN2
5: VH
6: VL
7: SQ
8: GND
9: Vee
10: AGCG
11: CLA
12: CAP
13: VAGC
14: IN1
15: IN1
16: Vcc

6) MB4316C
R/W Bus Switch



1: Vee2
2: GAN2
3: GAN1
4: IN5
5: IN4
6: OUT5
7: OUT6
8: GND
9: Vee1
10: IN2
11: IN3
12: OUT4
13: OUT3
14: IN1
15: OUT2
16: OUT1

Section 9
Parts List

9. PARTS LIST

9.1 ASSEMBLY DRAWINGS (ILLUSTRATION)

The assembly drawing is the illustration that each part of every block was analyzed relationally on the assembly. Each analyzed part is given the number, which corresponds to the number in the INDEX No. column of the list. And mechanical assembly showing which part of the unit is analyzed, is given on the page.

NOTE) The parts that can't be disassembled on a usual maintenance work are not illustrated in their assembled state, and given a number of the parts. And the quantity of parts, and specification are entered in the list corresponding to the number of parts.
When all parts are entered in the list, the INDEX No. column will be blank.

9.2 LIST

The quantity of parts, the name of parts and specification are entered corresponding to the number of the illustration.

9.2.1 Index No.

A number is assigned on each part in the illustration. The number corresponds with the INDEX No. But in case INDEX No. is given at every part of assembly, the column of INDEX No. will be blank.

9.2.2 Composition & Quantity

Quantity of composition represents the major and minor relation to the setting No. of assembly parts. (The left side indicates large assembly, and the parts in the assembly shift to the right in turn).

9.2.3 Specification

Specifications of parts (drawing No.) are represented.

9.2.4 Description

Name of the part (in Japanese), maker of parts and applicable machine etc. are entered.

9.3 EXAMPLE

COMPOSITION & QUANTITY:

"B010-3110-T001A" consists of "B010-3110-V044A", "F6-SWINA-4 x 10S" "B010-3110-V035A" and "F6-SAHT-4 x 6" of these; "B010-3110-V044A" consists of 1-4 of the INDEX No. column, and "B010-3110-V035A" consists of 6-13.

The quantity of each part that is mounted is given by the number is this column.

Parts whose INDEX No. has *mark are maintenance parts.

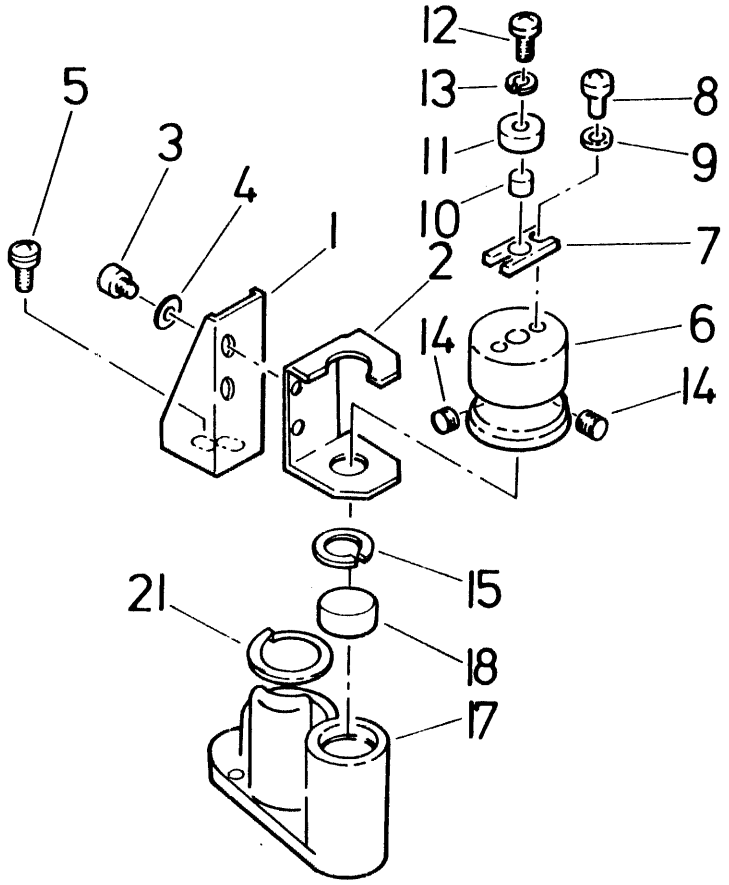


Figure 9-1 PARTS LIST EXAMPLE

Table 9-1 Part List Example

INDEX NO.	COMPOSITION & QUANTITY							SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1							B010-3110-T001A	Card Reader Unit			
		1						B010-3110-V044A	Guid			
1			1					B010-3110-X098A	Plate			
2			1					B010-3110-Y002A	Plate			
3			2					F6-SNA-3x5S65	Screw			
4			2					F6-WB-3S	Washer			
5		2						F6-SW1NA-4x10S	Screw			
		1						B010-3110-V035A	Eccentric Roller Assy.			
6			1					B010-3110-W026A	Roller Assembly			
				1				B010-3110-X068A	Roller			
*7			1					B010-3110-X077A	Plate			
8			2					F6-SNA-3x6S65	Screw			
9			2					F6-WM-3S	Washer			
10			1					B010-3110-X018A	Distance Piece			
11			1					623ZZS	Ball Bearing			
12			1					F6-SNA-3x6S65	Screw			
13			1					F6-WB-3S	Washer			
14		2						F6-SAHT-4x6	Screw			

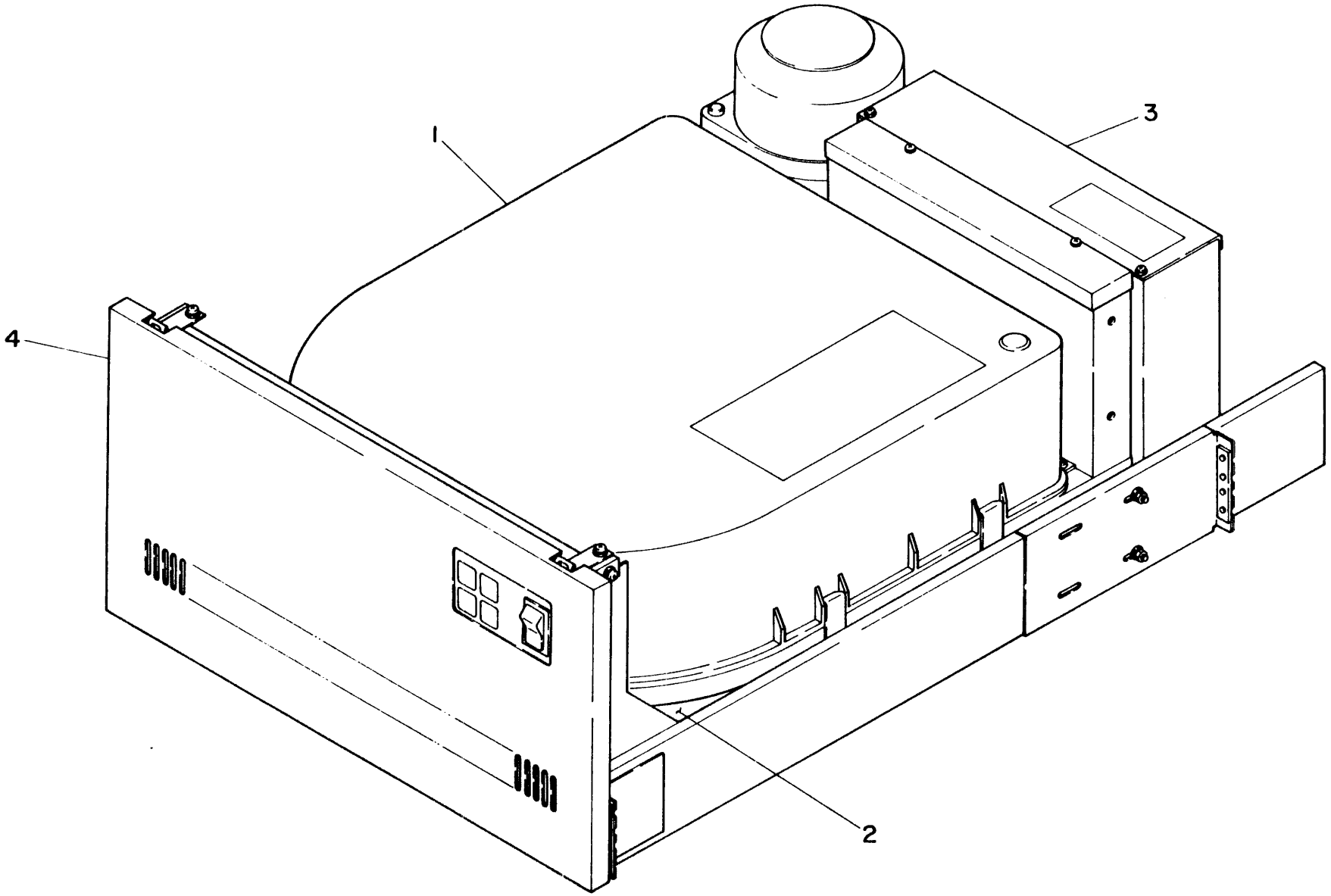


Figure 9-2 FIXED DISK UNIT

Table 9-2 Fixed Disk Unit

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1	B03B-4585-B112A	M2282K Fixed Disk		M2282K only	
	1	B03B-4585-B110A	M2280K Fixed Disk		M2280 only	
	1	B03B-4585-B113A	M2283K Fixed Disk		M2283K only	
	1	B03B-4585-B114A	M2284K Fixed Disk		M2284K only	
	1	B03B-4585-B116A	M2286K Fixed Disk		M2286K only	
	1	B03B-4585-B119A	M2289K Fixed Disk		M2289 only	
	1	B03B-4585-B117A	M2287K Fixed Disk		M2287K only	
	1	B03B-4585-B118A	M2288K Fixed Disk		M2288K only	
	1	B03B-4585-B502A	M2282N Fixed Disk		M2282N only	
	1	B03B-4585-B500A	M2280N Fixed Disk		M2280N only	
	1	B03B-4585-B503A	M2283N Fixed Disk		M2283N only	
	1	B03B-4585-B504A	M2284N Fixed Disk		M2284N only	
	1	B03B-4585-B506A	M2286N Fixed Disk		M2286N only	
	1	B03B-4585-B509A	M2289N Fixed Disk		M2289N only	
	1	B03B-4585-B507A	M2287N Fixed Disk		M2287N only	
	1	B03B-4585-B508A	M2288N Fixed Disk		M2288N only	
*1	1	B030-4540-T002A	Disk Enclosure		M2282 only	
*1	1	B030-4540-T010A	Disk Enclosure		M2280 only	
*1	1	B030-4540-T003A	Disk Enclosure		M2283 only	
*1	1	B030-4540-T004A	Disk Enclosure		M2284 only	
*1	1	B030-4540-T006A	Disk Enclosure		M2286 only	
*1	1	B030-4540-T009A	Disk Enclosure		M2289 only	
*1	1	B030-4540-T007A	Disk Enclosure		M2287 only	
*1	1	B030-4540-T008A	Disk Enclosure		M2288 only	
2	1	B03B-4585-E500A	Sub Frame Unit		M2280 ~ M2289K	
2	1	B03B-4585-E550A	Sub Frame Unit		M2282 ~ M2289N	
3	1	B03B-4540-E005A	GATE UNIT		M2280 ~ M2289	
4	1	B03B-4540-E350A	Panel Unit		Optional	
4	1	B03B-4540-E353A	Panel Unit 24" Slide		Optional	

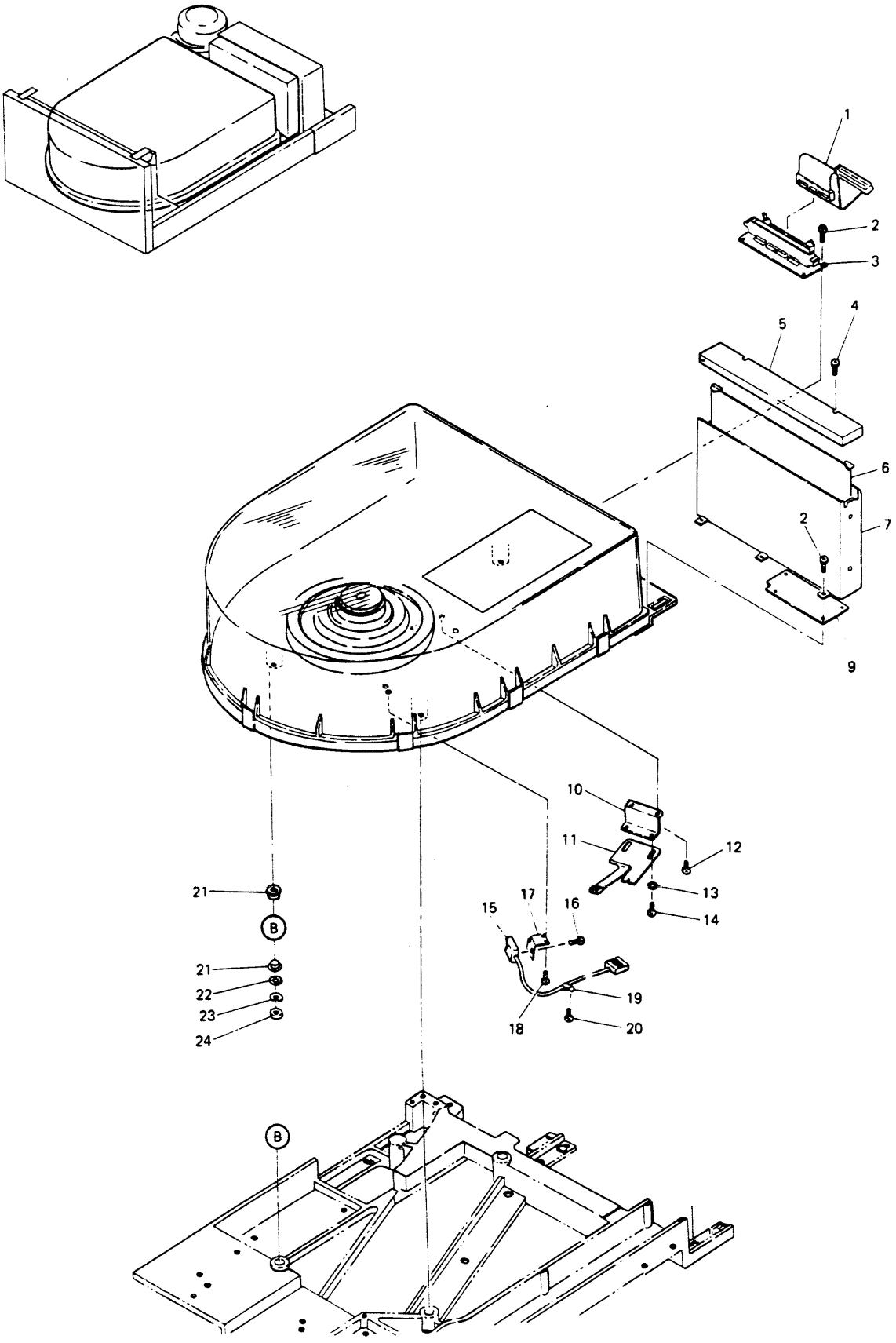


Figure 9-3 DISK ENCLOSURE

Table 9-3 Disk Enclosure

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1	B030-4540-T002A	Disk Enclosure		M2282	
	1	B030-4540-T010A	Disk Enclosure		M2280	
	1	B030-4540-T003A	Disk Enclosure		M2283	
	1	B030-4540-T004A	Disk Enclosure		M2284	
	1	B030-4540-T006A	Disk Enclosure		M2286	
	1	B030-4540-T009A	Disk Enclsoure		M2289	
	1	B030-4540-T007A	Disk Enclosure		M2287	
	1	B030-4540-T008A	Disk Enclosure		M2288	
1	1	B030-4420-W031A	Cable Assy.			
2	7	F6-SW2NA-4x12S	Screw with Washer			
3	1	B16B-6180-0010A	Through Connector W	THWM		
4	2	F6-SW2NA-3x6S	Screw with Washer			
5	1	B030-4420-X022A	Cover			
*6	1	B16B-6170-0020A	Read Switch W	RQWM	T002~T004, T010	
*6	1	B16B-6170-0010A	Read Switch V	RQVM	T006~008, T009	
7	1	B030-4420-W018A	Frame Assy.			
9	1	B030-4420-X044A	Plate			
10	1	B030-4420-X008A	Plate			
*11	1	B030-4420-W006A	Antistatic Brush			
12	2	F6-SW2NA-4x8S	Screw with Washer			
13	2	F6-WM-4S	Washer			
14	2	F6-SW2NA-4x8S	Screw with Washer			
*15	1	B030-4420-W030A	Switch Assy.		Speed Transducer	
16	2	F6-SW2NA-2.6x4S	Screw with Washer			
17	1	B030-4420-X009A	Plate			
18	2	F6-SW2NA-4x8S	Screw with Washer			
19	3	F6-NYC-2.5	Nylon Clip			
20	3	F6-SW1NA-4x8S	Screw with Washer			
21	6	B030-4420-Y043A	Bush			
22	3	F6-WM-8S	Washer			
23	3	F6-WB-8S	Washer			
24	3	F6-NI-8S	Hexagon Nut			

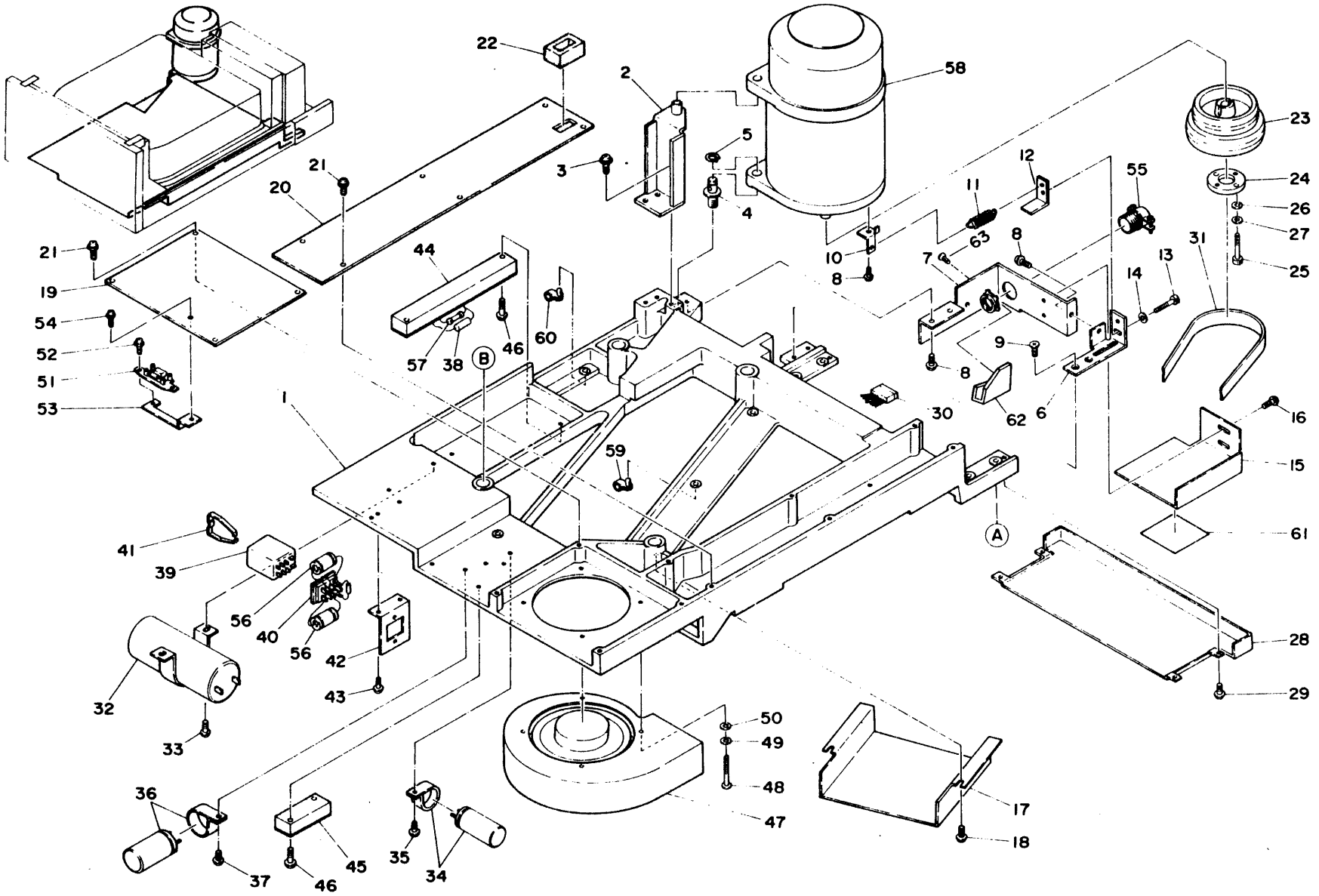


Figure 9-4 SUB FRAME UNIT

Table 9-4 Sub-Frame Unit (continued)

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1	B03B-4585-E500A	Sub Frame Unit		M2280K ~ M2289K	
	1	B03B-4585-E550A	Sub Frame Unit		M2280N ~ M2289N	
	1	B030-4585-V100A	Sub Frame Assy.			
1	1	B030-4420-Z140A	Sub Frame			
2	1	B030-4420-W103A	Pivot			
3	3	F6-SW2NA-4x12S	Screw with Washer			
4	1	B030-4420-X153A	Shaft			
5	1	F6-ER-8sus	Retaining Ring			
6	1	B030-4585-X105A	Plate			
7	1	B030-4585-X101A	Plate			
8	4	F6-SW2NA-4x12S	Screw with Washer			
9	2	F6-SSA-4x12S	Screw			
10	1	B030-4585-X102A	Plate			
11	1	B030-4420-X143A	Spring			
12	1	B030-4420-Z144A	Slide Plate			
13	1	B030-4420-Y154A	Bolt			
14	1	F6-WM-4S	Washer			
15	1	B030-4585-X103A	Cover			
16	2	F6-SW2NA-4x8S	Screw with Washer			
17	1	B030-4420-X147A	Cover			
18	2	F6-SW2NA-4x8S	Screw with Washer			
19	1	B030-4420-X156A	Plate			
20	1	B030-4420-X146A	Plate			
21	10	F6-SW2NA-4x10S	Screw with Washer			
22	1	B030-4420-X109A	Packing			
23	1	B030-4585-Y104A	Pulley			
24	1	B030-1190-Y117A	Tapered Plate			
25	2	F6-BA-4x20	Hexagon Bolt			
26	2	F6-WK-4S	Washer			
27	2	F6-WB-4S	Washer			
28	1	B030-4420-X150A	Gate Cover			
29	4	F6-SW2NA-4x6S	Screw with Washer			
30	1	C63L-0670-0011#5	Housing	CNJ4		
*31	1	B030-1000-0006A	Belt			

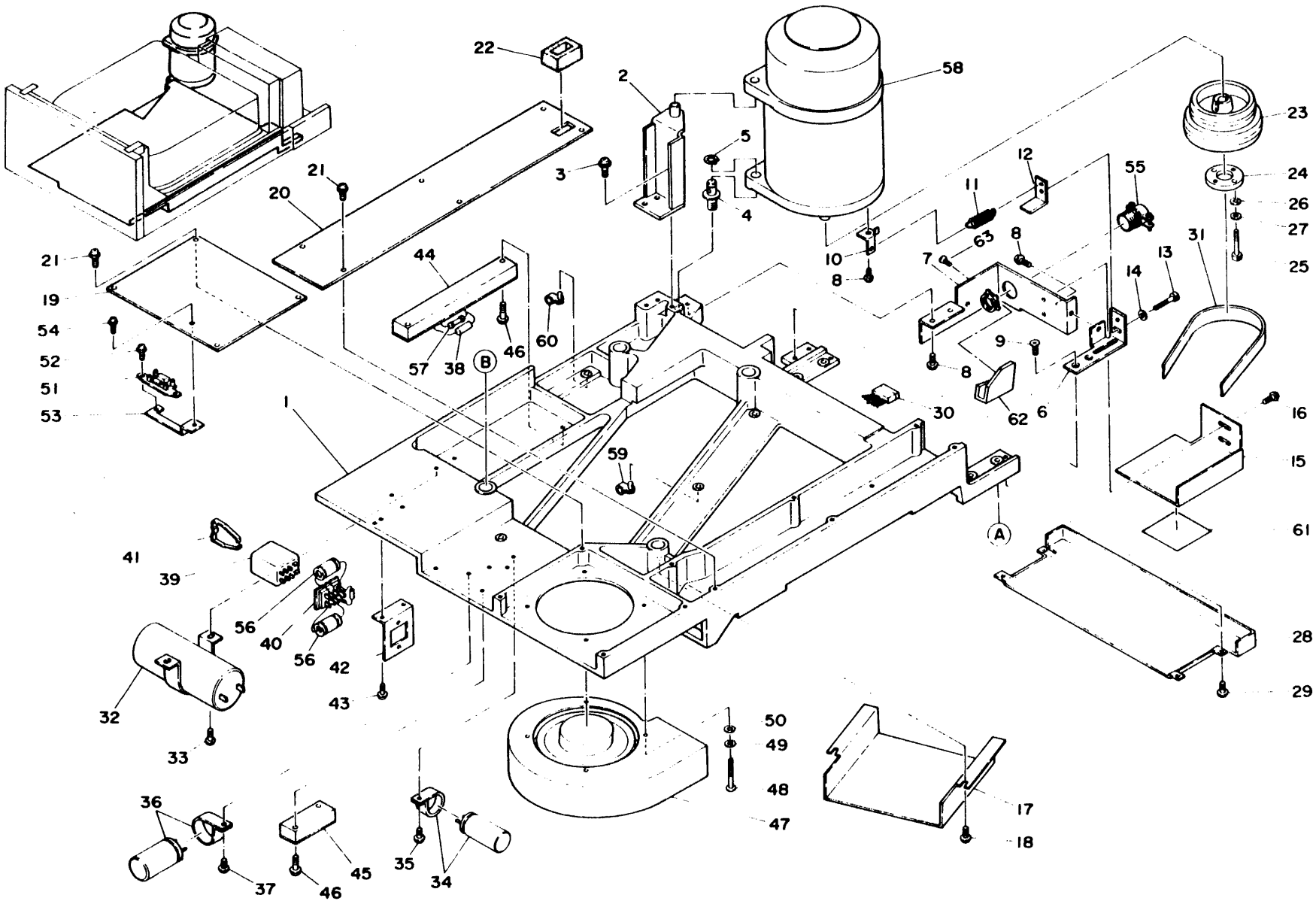
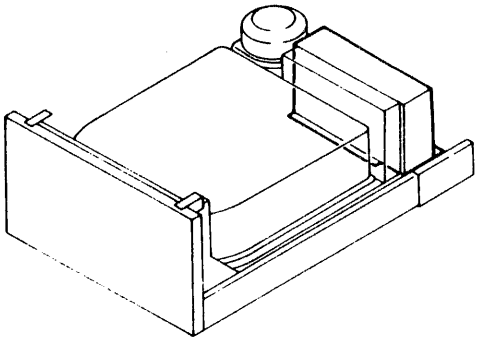


Figure 9-4 SUB FRAME UNIT

Table 9-4 Sub-Frame Unit (continued)

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
32	1	B42L-0110-0001A	Capacitor	C3	M228XK	
32		B42L-0110-0002A	Capacitor	C3	M228XN	
33	2	F6-SW2NA-4x10S	Screw with Washer			
34	1	C42L-1520-0001#2E	Capacitor	C2		
35	1	F6-SW2NA-4x10S	Screw with Washer			
36	1	CT-CE62W1E682A#P	Capacitor	C1		
37	1	F6-SW2NA-4x10S	Screw with Washer			
38	1	R010V-1G-10R00-J02	Resistor	R1		
*39	1	B58L-0170-0001A	Relay	RL		
40	1	C58L-0080-0001	Socket			
41	1	C58L-0090-0001	Holder			
42	1	B030-4420-Z106A	Plate			
43	2	F6-SW2NA-4x10S	Screw with Washer			
44	1	C65L-2100-0003	Terminal	TRM3		
45	1	C65L-2100-0008	Terminal	TRM2		
46	4	F6-SW3NA-3x16S	Screw with Washer			
*47	1	B90L-1190-0001A	Blower	FAN		
48	4	F6-SNA-4x45S	Screw with Washer			
49	4	F6-WB-4S	Washer			
50	4	F6-WM-4S	Washer			
51	1	B57L-0040-0003A	Fan Alarm Assy.	FALM		
52	2	F6-SW2NA-3x6S	Screw with Washer			
53	1	B030-4420-X157A	Plate			
54	1	F6-SW2NA-3x6S	Screw with Washer			
55	1	C30L-2010-0001	Clamp			
56	2	N42L-1911-0002 #FQ-13	Spark Killer	SQ1, SQ2		
57	2	C50L-2090-0006	Diode	D1, D2		
*58	1	B90L-0980-0001A	Motor	M	M228XK	
59	4	CT-AD-04	Clamp			
60	4	CT-AD-11	Clamp			
61	1	B370-0950-0232A	Label			
58		B90L-0980-0003A	Motor	M	M228XN	
62	1	B030-4585-X106A	Plate			
63	2	F6-SSA-4x6S	Screw			



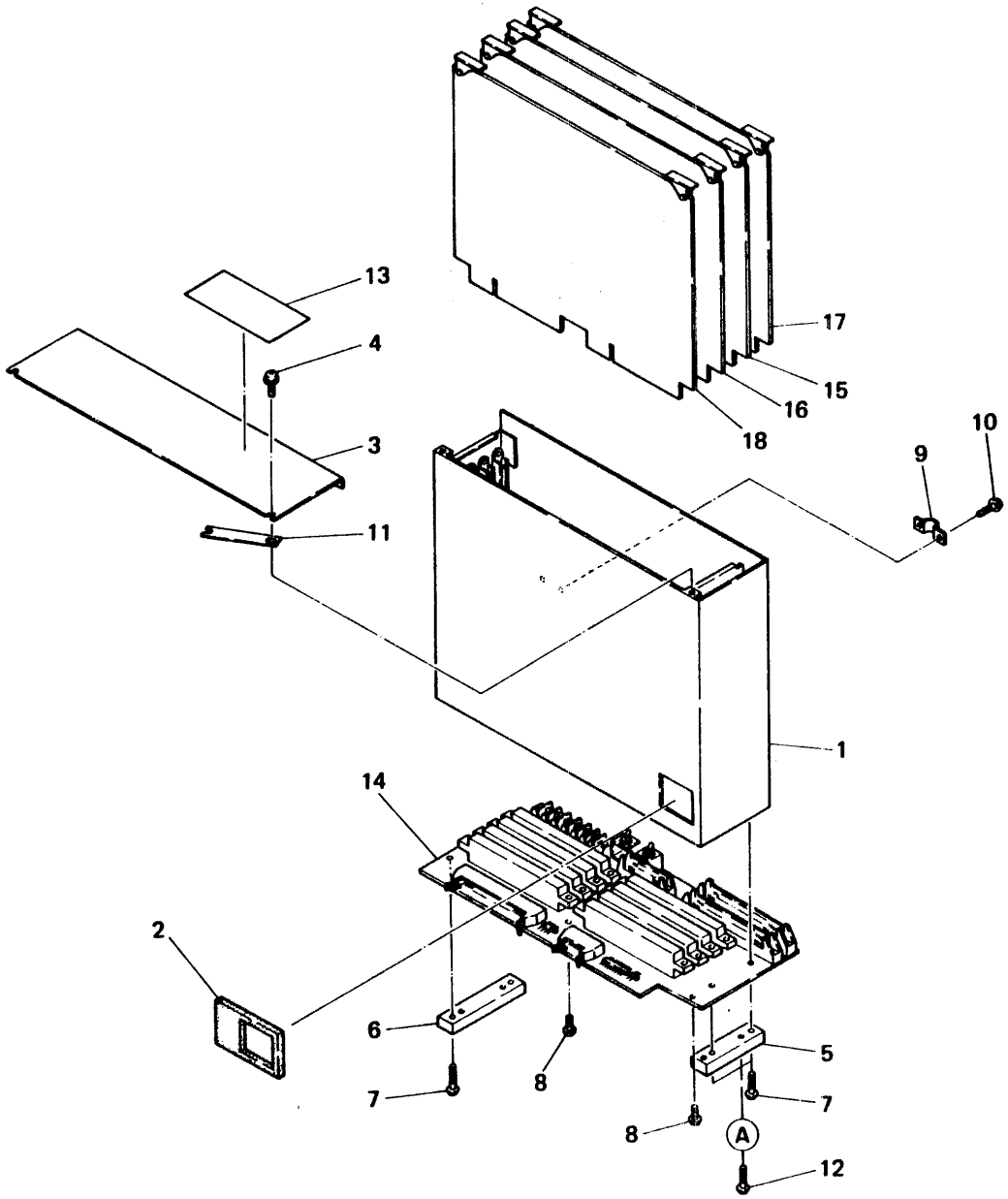


Figure 9-5 GATE UNIT

Table 9-5 Gate Unit

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1	B03B-4540-E005A	Gate Unit			
	1	B030-4420-V349A	Gate Assy			
1	1	B030-4420-W351A	Gate Box			
2	1	B030-4420-X306A	Packing			
3	1	B030-4420-W353A	Cover			
4	2	F6-SBD-3x10S	Screw			
5	1	B030-4420-Y314A	Insulator			
6	1	B030-4420-Y315A	Insulator			
7	4	F6-SW2NA-3x12S	Screw with Washer			
8	3	F6-SW2NA-3x6S	Screw with Washer			
9	1	F6-CBHB-8	Holder			
10	2	F6-SW2NA-3x8S	Screw with Washer			
11	1	B030-4420-X319A	Ground Plate			
12	4	F6-SW2NA-4x16S	Screw with Washer			
13	1	B370-0950-0326A	Label			
14	1	B030B-4540-F008A	Gate Circuit N	GBNM		
*15	1	B16B-6300-0010A	Variable Oscillator F	VOFM		
*16	1	B16B-6150-0010A	Controller I	CMIM		
*17	1	B16B-6160-0030A	Controller F	CQFM		
*18	1	B16B-6240-0010A	Speed Controller I	SDIM		

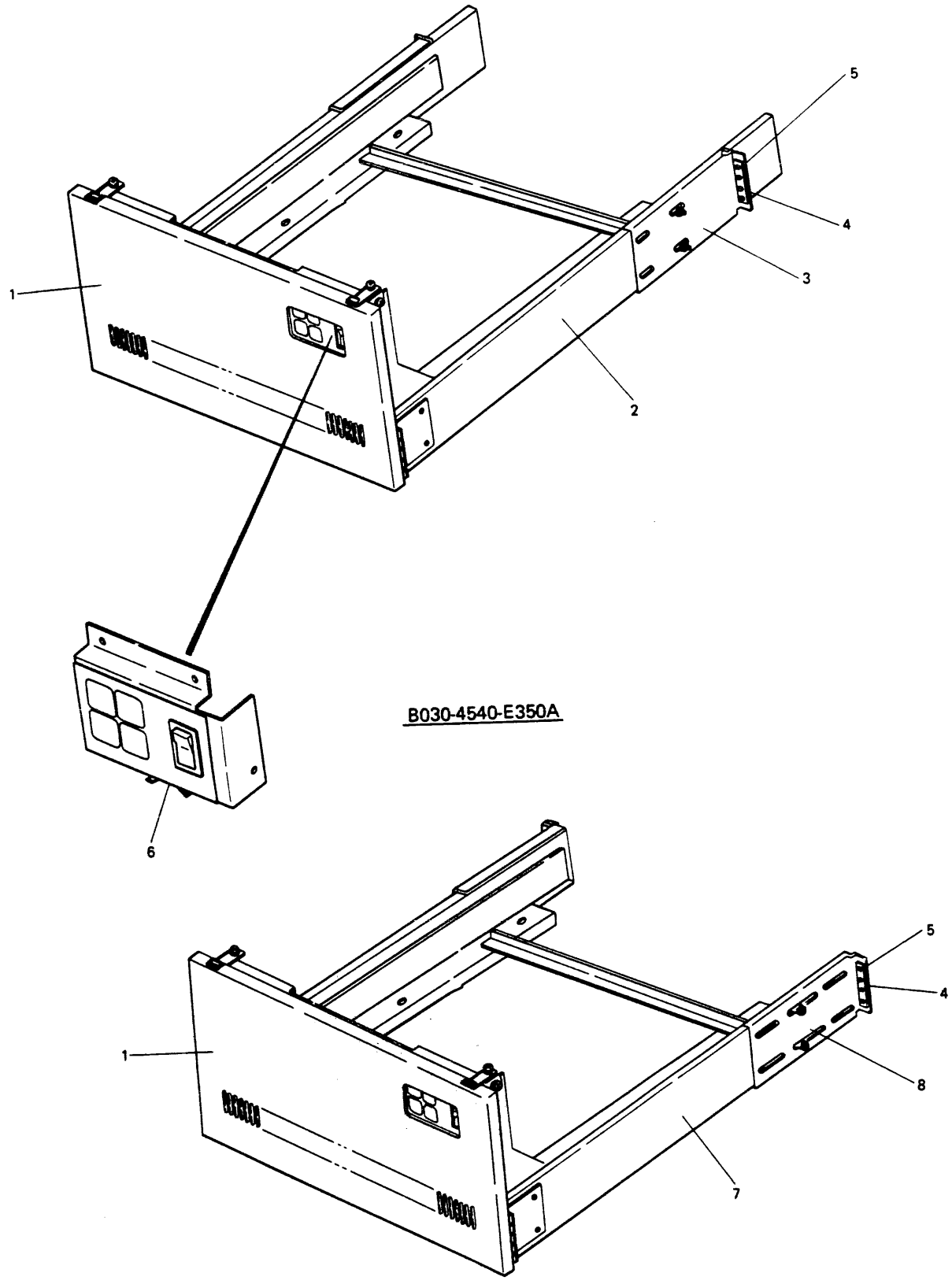


Figure 9-6 Panel Unit

Table 9-6 Panel Unit

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1	B03B-4540-E350A	Panel Unit			
1	1	B030-4540-W401A	Front Panel			
2	1	B27L-0230-0002A	Slide Guide		28", 1 pair	
3	2	B030-4540-X410A	Bracket			
4	4	B030-4380-X042A	Nut Bar			
5	16	F6-SW2NA-5x12S	Screw with Washer			
6	1	N860-3251-T002	Switch Assembly			
	1	B03B-4540-E353A	Panel Unit			
1	1	B030-4540-W401A	Front Panel			
7	1	B27L-0230-0004A	Slide Guide		24", 1 pair	
8	2	B030-4540-X418A	Bracket			
4	4	B030-4380-X042A	Nut Bar			
5	16	F6-SW2NA-5x12S	Screw with Washer			
6	1	N860-3251-T002	Switch Assembly			

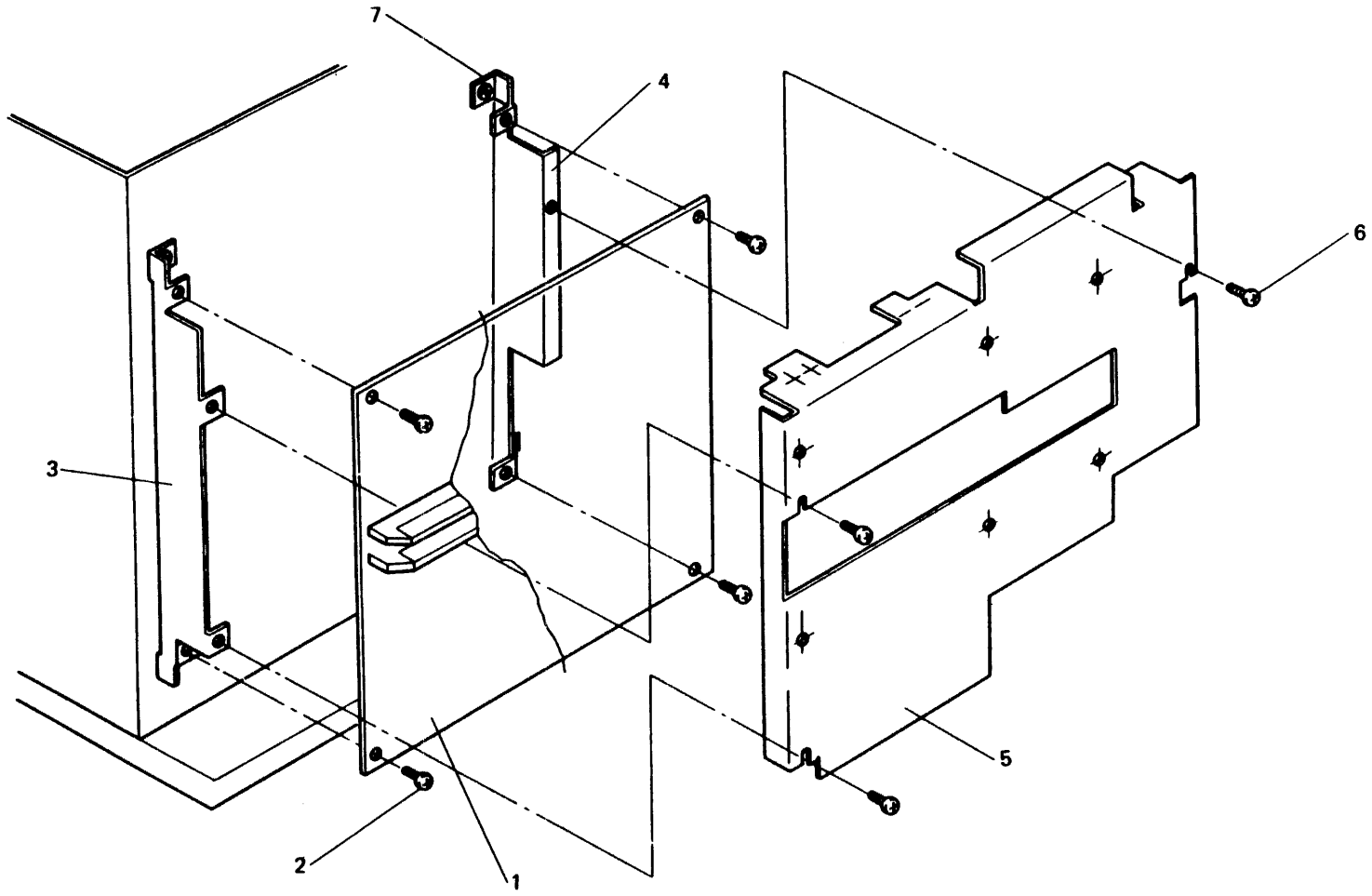


Figure 9-7 Dual Port Unit

Table 9-7 Dual Port Unit

INDEX NO.	COMPOSITION & QUANTITY	SPECIFICATION	DESCRIPTION	CHARACTER	REMARK	REVISION
	1	B03B-4540-E901A	Dual Port Unit			
*1	1	B16B-7990-0020A	Cross Call B	XCBM		
2	4	B6-SBD-3x6S	Screw			
3	1	B030-4540-X903A	Plate			
4	1	B030-4540-X904A	Plate			
5	1	B030-4540-X901A	Cover			
6	3	F6-SBD-3x6S	Screw			
7	4	F6-SBD-3x6S	Screw			
	1	B660-1065-T037A	Cable		50P	
	1	B660-1060-T089A	Cable		10P	
	1	B660-1065-T061A	Cable		26P	

Section10
Schematics

The schematics is provided in 3 parts:

Note:

PART 1 is applicable to equipment revision A8 and after supporting a Dual Port feature.
PART 2 is SMD Dual Port schematics as an optional feature.
PART 3 is applicable to equipment revision of A1 to A7.

PART 1
Basic Schematics (NeW)

SHEET	ABBR	TITLE
001		Schematics/Drawings List
002		Functional Block Diagram
003	AA0	CQFM I/O Signals
004	AA1	A-Cable Receivers
005	AA2	A/B-Cable Drivers
006	AA3	Dual Port Connection
007	AB1	Unit Selection Start/Stop Control
008	AC1	Sector Address Reg. Status Generator (1)
009	AD1	Control Check Detector
010	AD2	Read Write Check Detector
011	AE1	Status Generator (2)
012	AF1	Read Write Control
013	BA0	CMIM I/O Signals
014	BA1	Buffers
015	BB1	Head Address Reg. Offset Control
016	BC1	Write PLO Control
017	BD1	Seek Control(1)
018	BD2	Seek Control(2) Seek Error Latch
019	BD3	Seek Control(3) LED Drivers
020	BD4	Seek Control(4)
021	BE1	Seek Status Generator
022	BE2	Seek Error Detector
023	BF1	Cylinder Address Register (CAR)
024	BG1	Guard Bands Detector
025	CA0	SDIM I/O Signals
026	CA1	Position Sensing (1)
027	CA2	Position Sensing (2) PLO I
028	CA3	Position Sensing (3)
029	CB1	Servo Control (1)
030	CB2	Servo Control (2)
031	CB3	Servo Control (3)
032	CC1	Power Amplifier
033	DA0	VOFM I/O Signals
034	DA1	Sector Generator
035	DB1	Write Compensation (1)
036	DB2	Write Compensation (2)
037	DC1	PLO II (1)
038	DC2	PLO II (2)
039	DD1	VFO (1)
040	DD2	VFO (2)
041	DE1	Data Separator
042	EA0	RQVM/RQWM I/O Signals
043	EA1	Access Head Read/write(1)
044	EA2	Access Head Read/Write(2)
045	EA3	Access Head Read/Write(3)
046	EB1	Fixed Head Read/Write
047	EB2	Fixed Head Select Driver
048	FA1	R/W, Servo Head Preamplifier
049	FA2	Fixed Head Diode Matrix
050	GA1	I/O Connectors LED's/Switches
051	GA2	AC/DC Power Supply
052		CQFM PCB Assembly
053		CMIM PCB Assembly
054		SDIM PCB Assembly
055		VOFM PCB Assembly
056		RQVM PCB Assembly
057		RQWM PCB Assembly
058		GBNM PCB Assembly

Schematics/Drawings List

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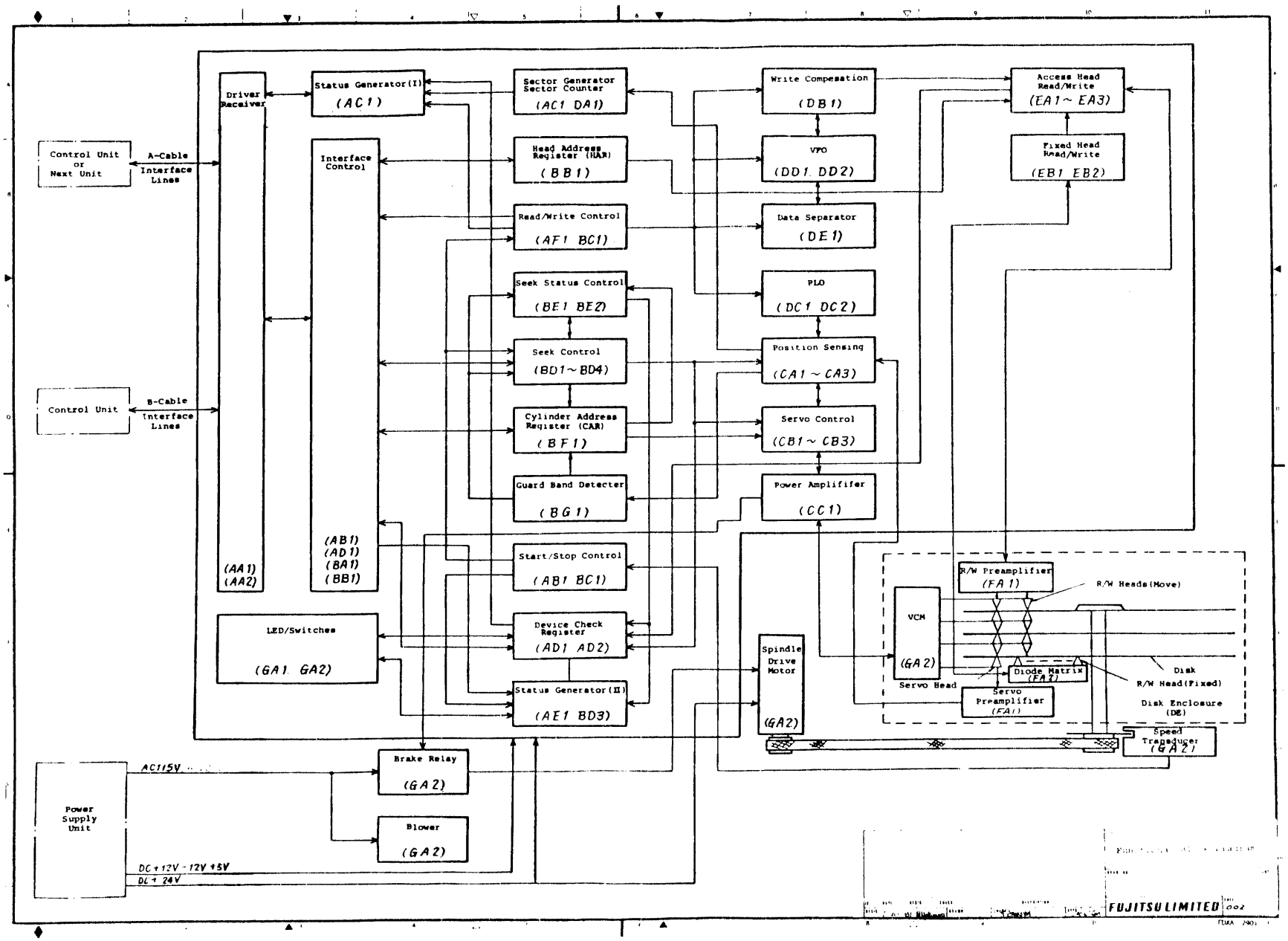
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A-Cable Interface Lines
Control Unit
B-Cable Interface Lines
Driver Receiver
(AA1) (AA2)
Status Generator(I) (AC1)
Interface Control
(AB1) (AD1) (BA1) (BB1)
Sector Generator Sector Counter (AC1 DA1)
Head Address Register (HAR) (BB1)
Read/Write Control (AF1 BC1)
Seek Status Control (BE1 BE2)
Seek Control (BD1~BD4)
Cylinder Address Register (CAR) (BF1)
Guard Band Detecter (BG1)
Start/Stop Control (AB1 BC1)
Device Check Register (AD1 AD2)
Status Generator(II) (AE1 BD3)
LED/Switches (GA1 GA2)
Write Compesation (DB1)
VFO (DD1 DD2)
Data Separator (DE1)
PLO (DC1 DC2)
Position Sensing (CA1~CA3)
Servo Control (CB1~CB3)
Power Amplifier (CC1)
Access Head Read/Write (EA1~EA3)
Fixed Head Read/Write (EB1 EB2)
R/W Preamplifier (FA1)
R/W Heads(Move)
VCM (GA2)
Servo Head
Diode Matrix (FA1)
Servo Preamplifier (FA1)
Disk
R/W Head(Fixed)
Disk Enclosure (DE)
Spindle Drive Motor (GA2)
Speed Transducer (GA2)
Power Supply Unit
AC115V
Brake Relay (GA2)
Blower (GA2)
DC+12V -12V +5V
DC+24V
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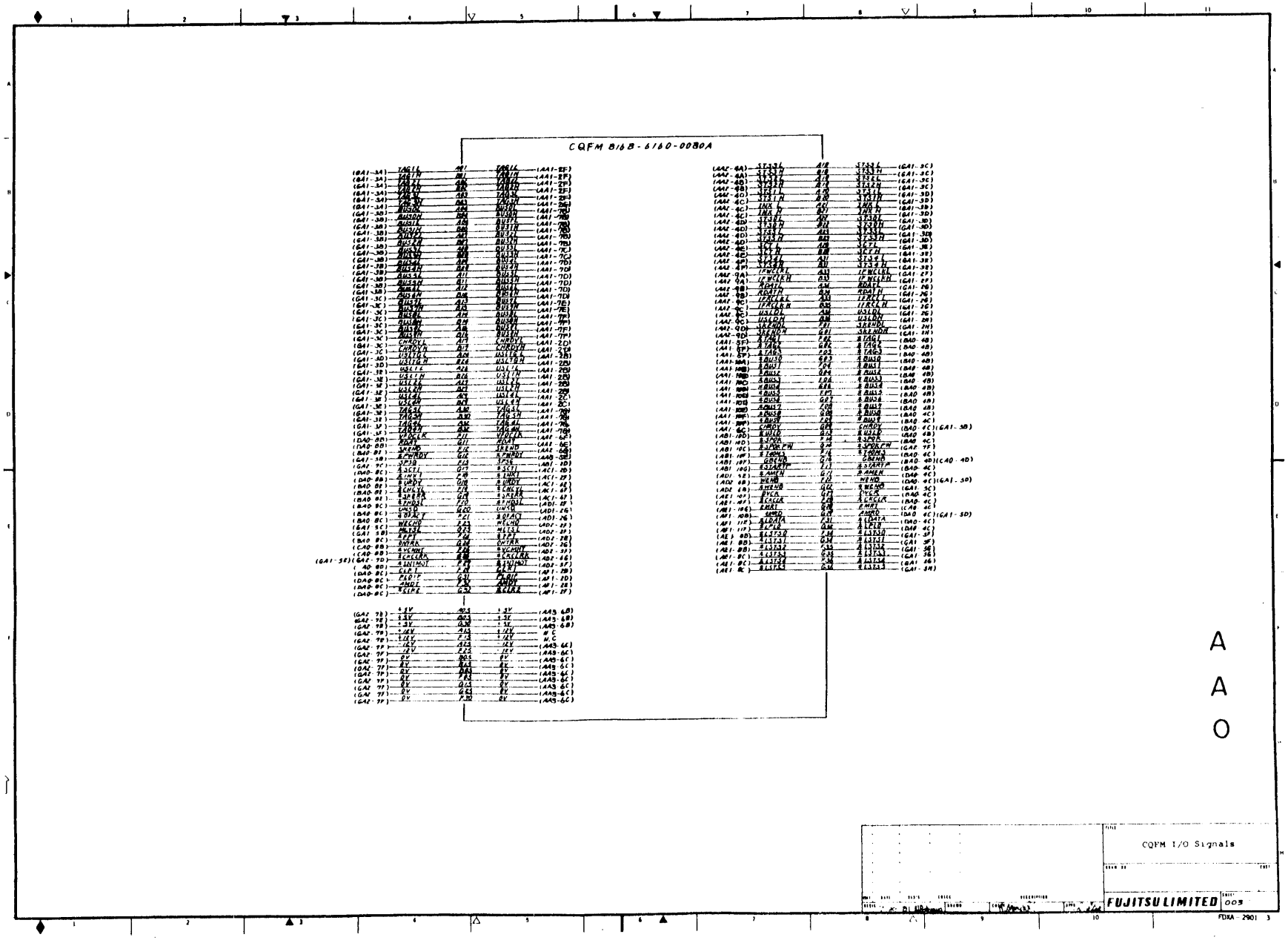
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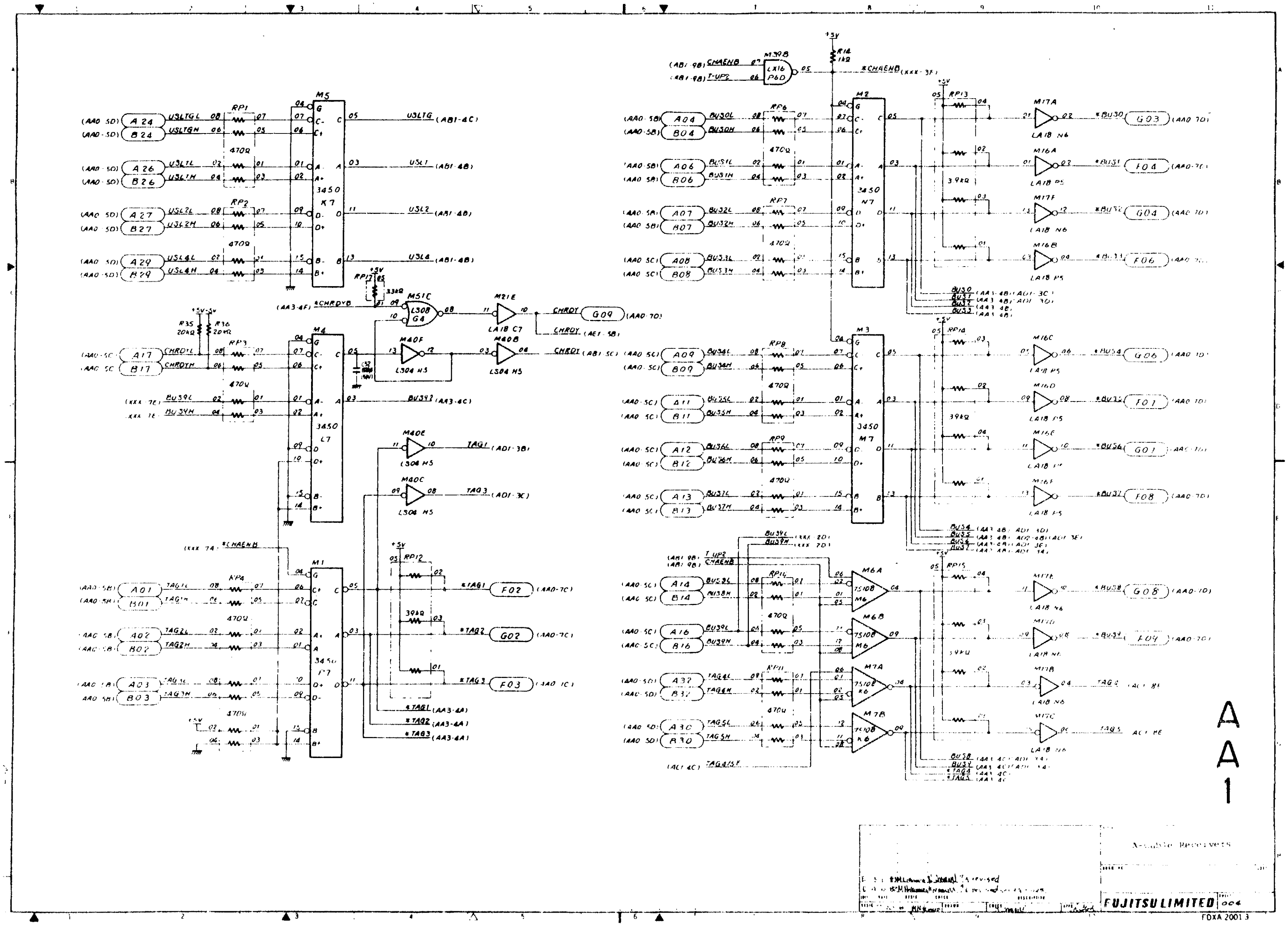
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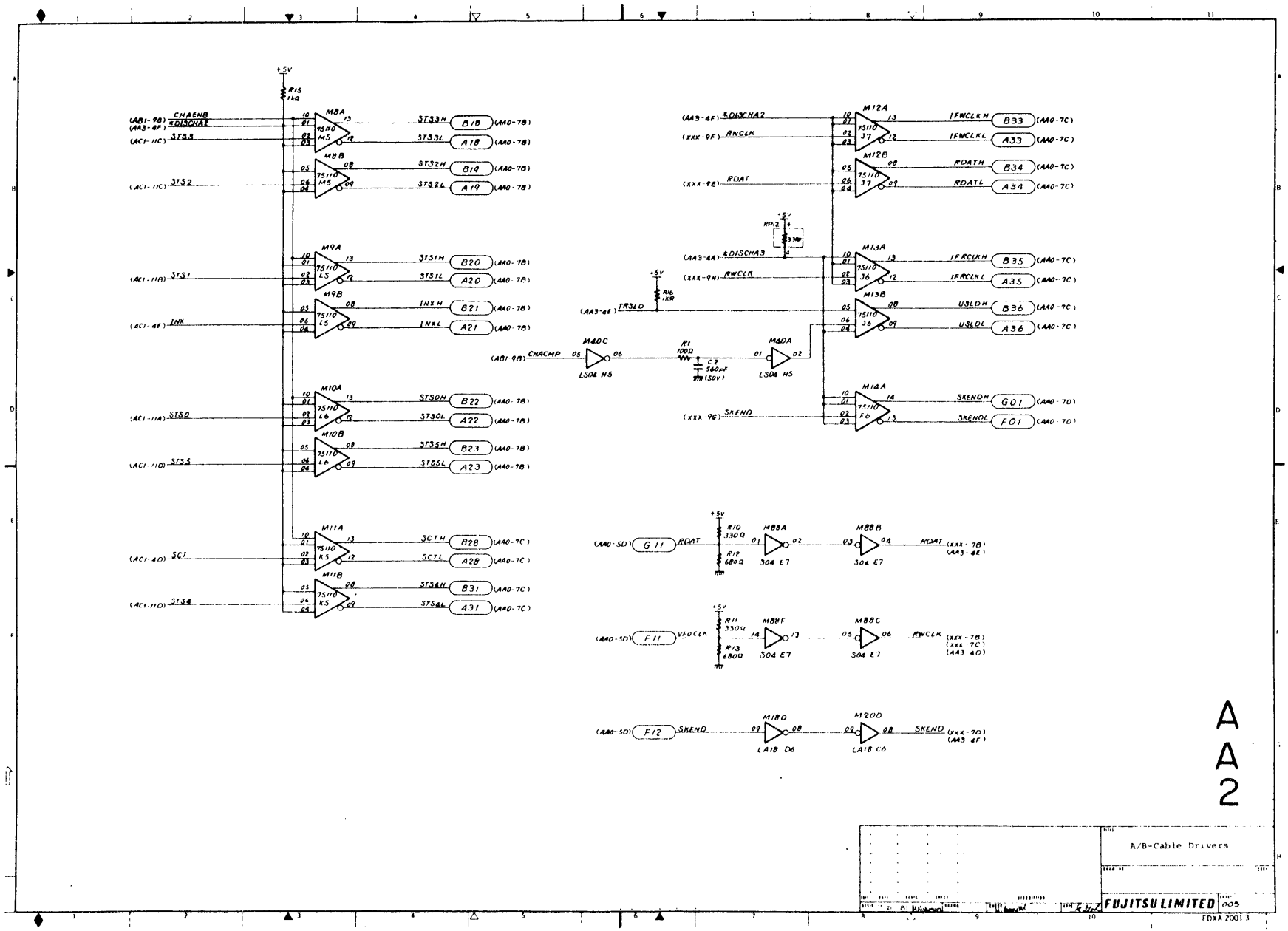
A/B-Cable Drivers
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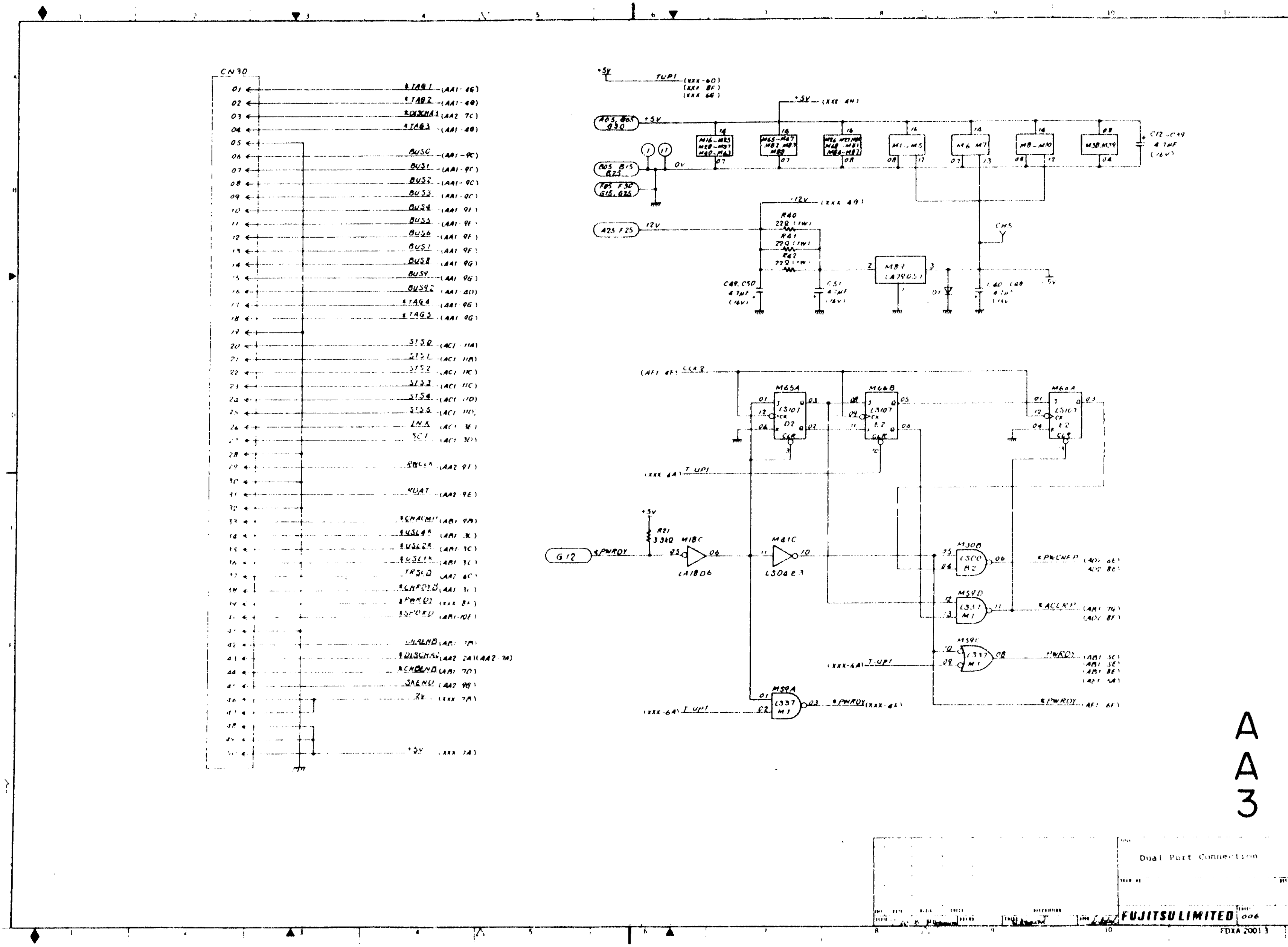

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Dual Port Connection

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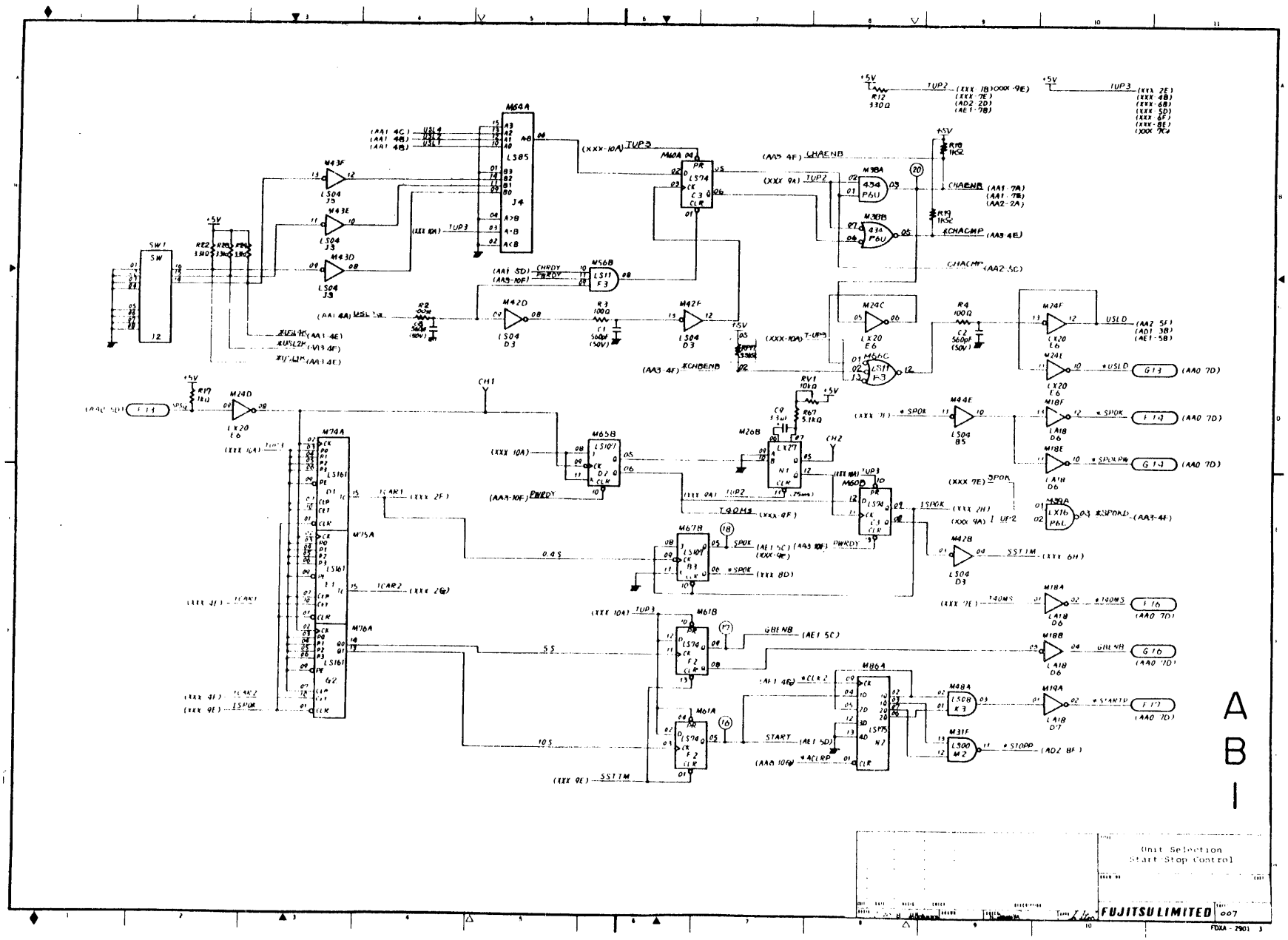
Unit Selection
Start Stop Control
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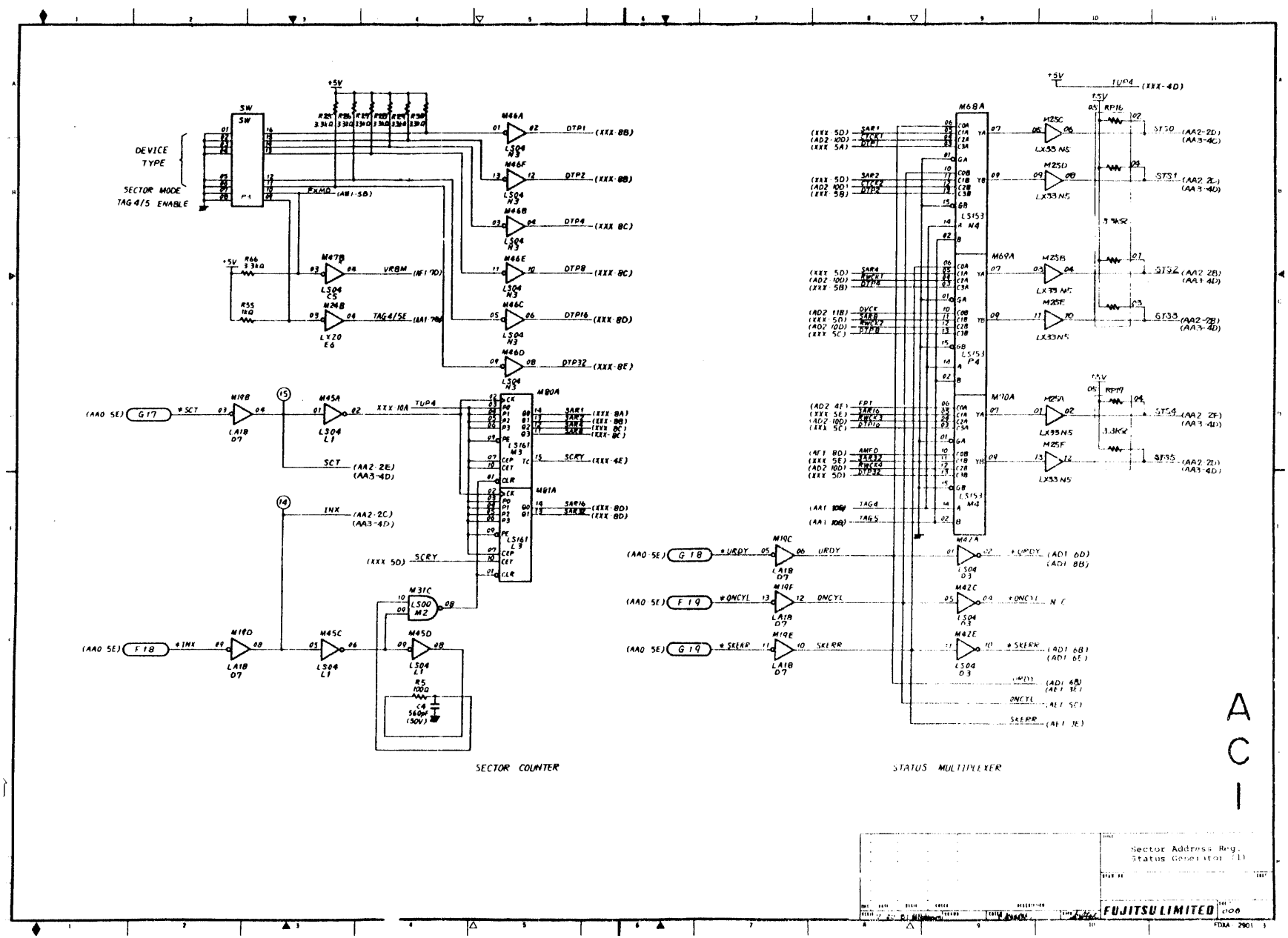
007
FDXA-2901 3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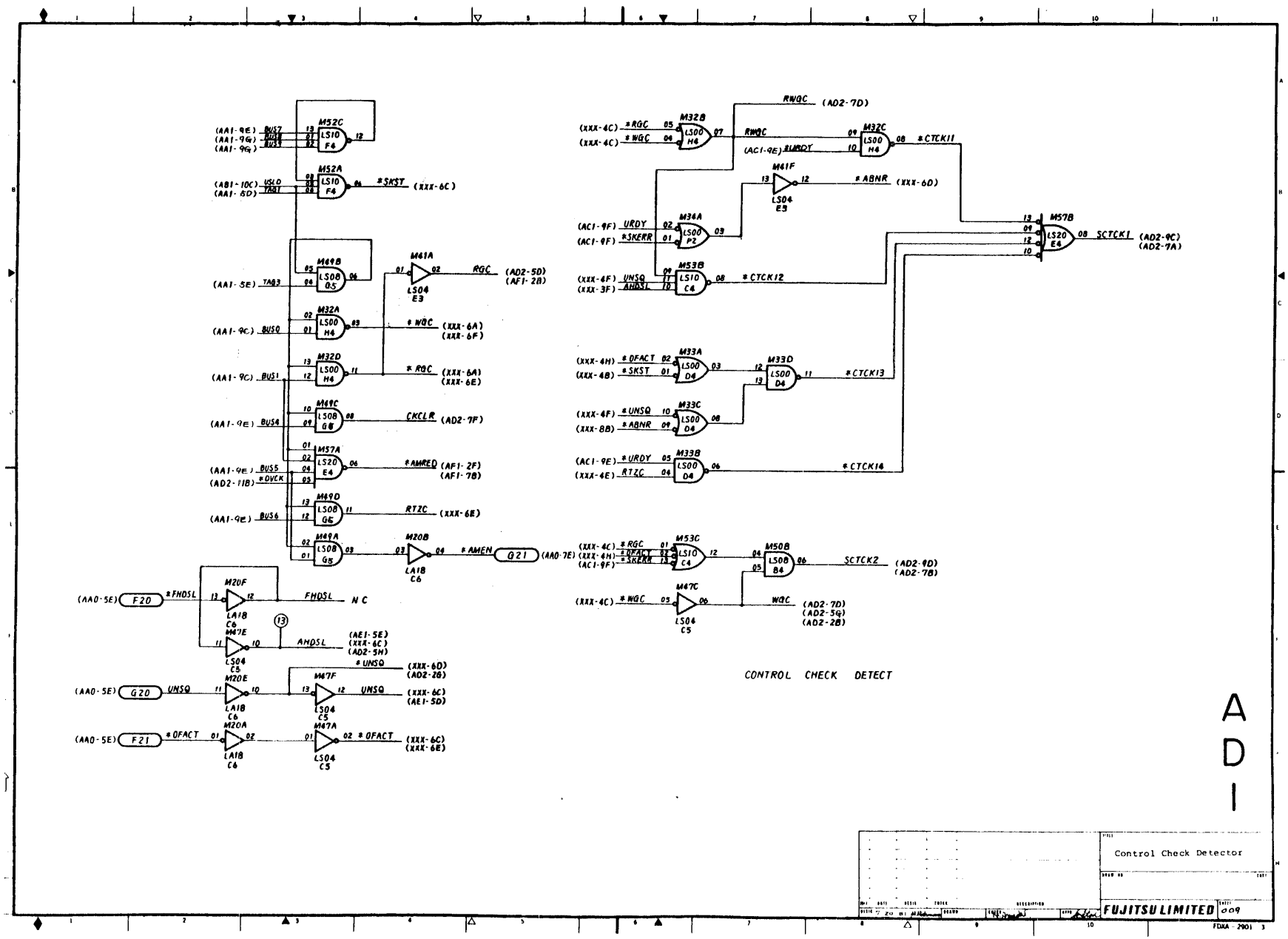
CONTROL CHECK DETECT
Control Check Detector
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D
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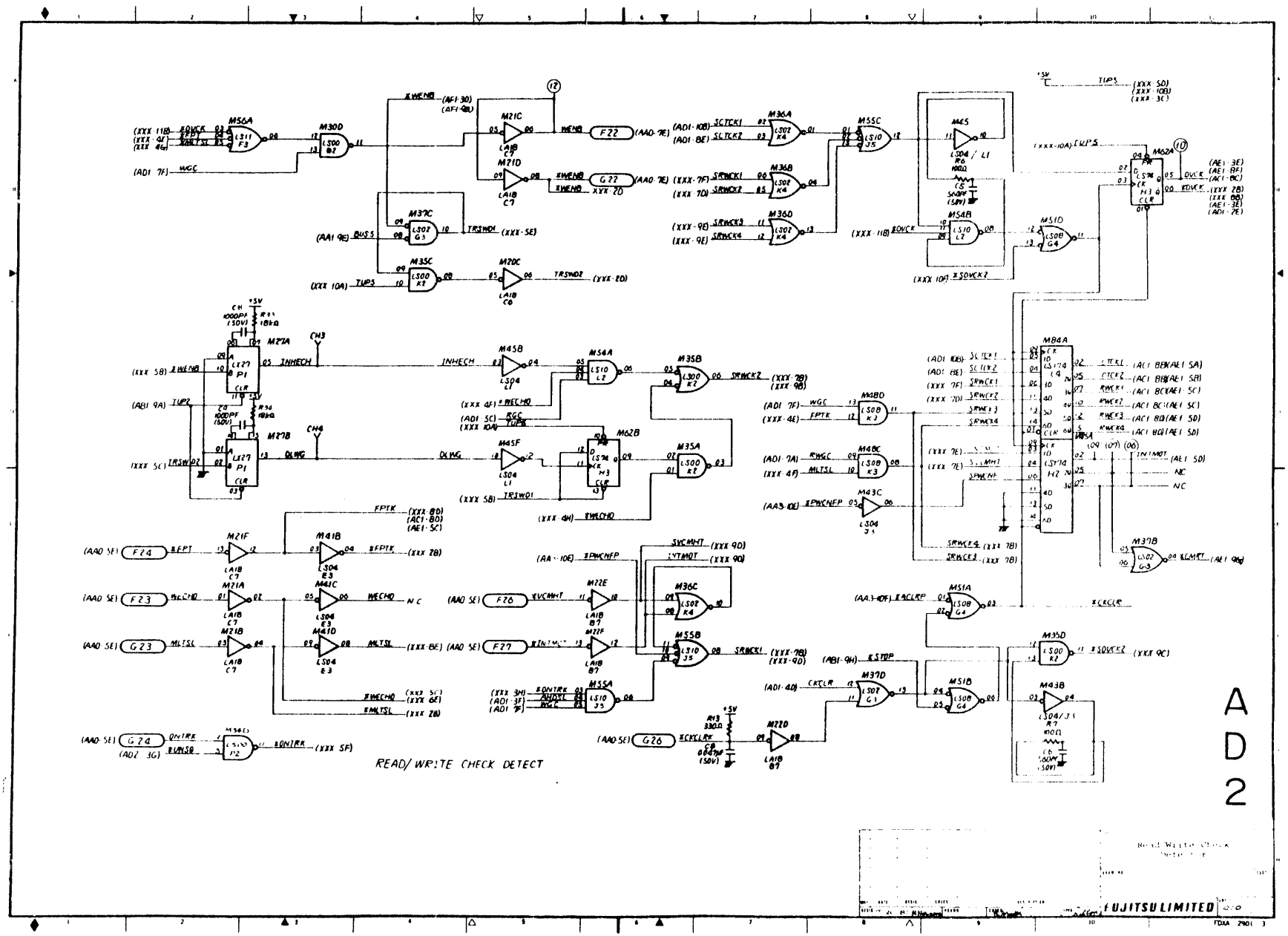
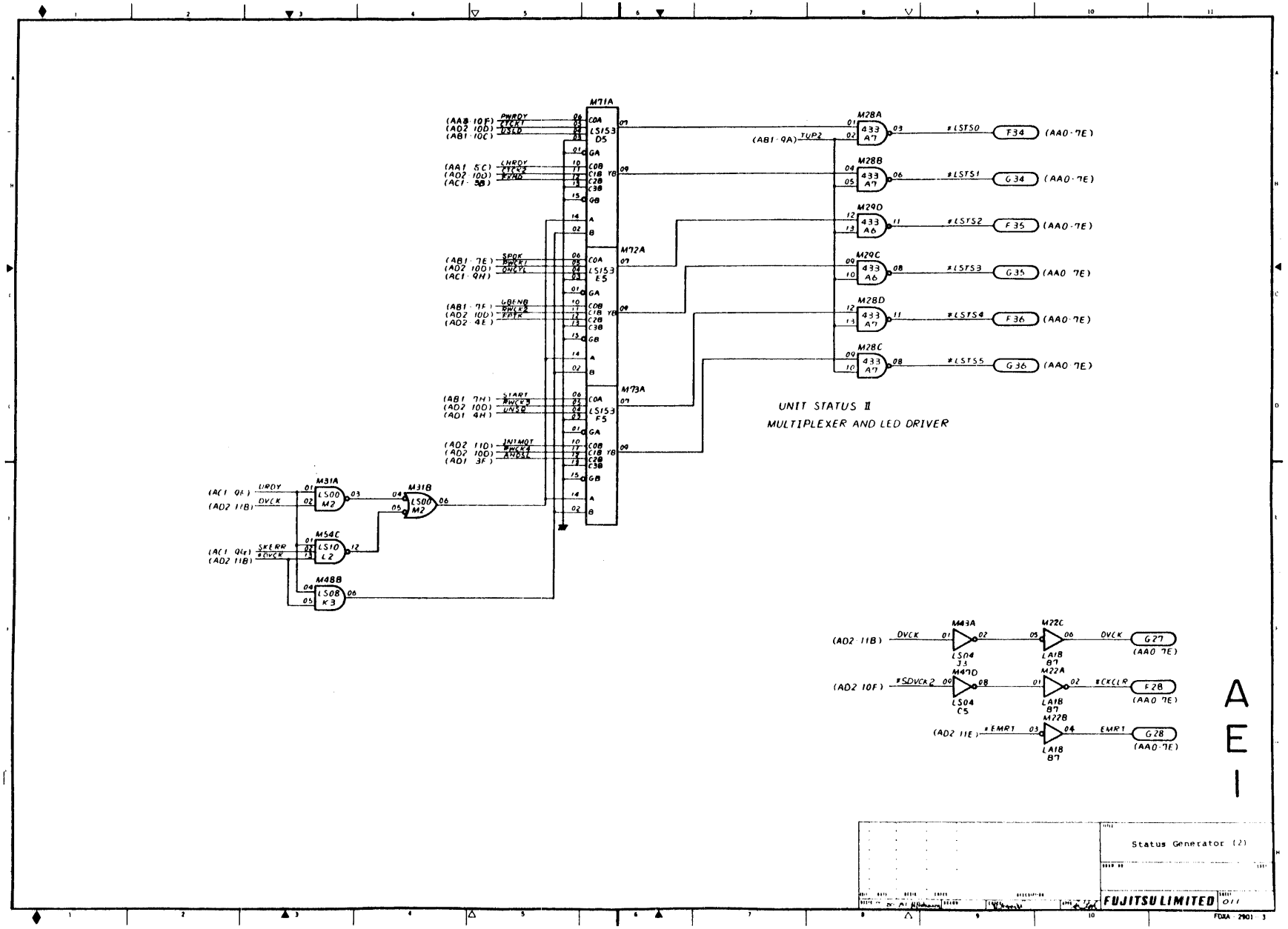
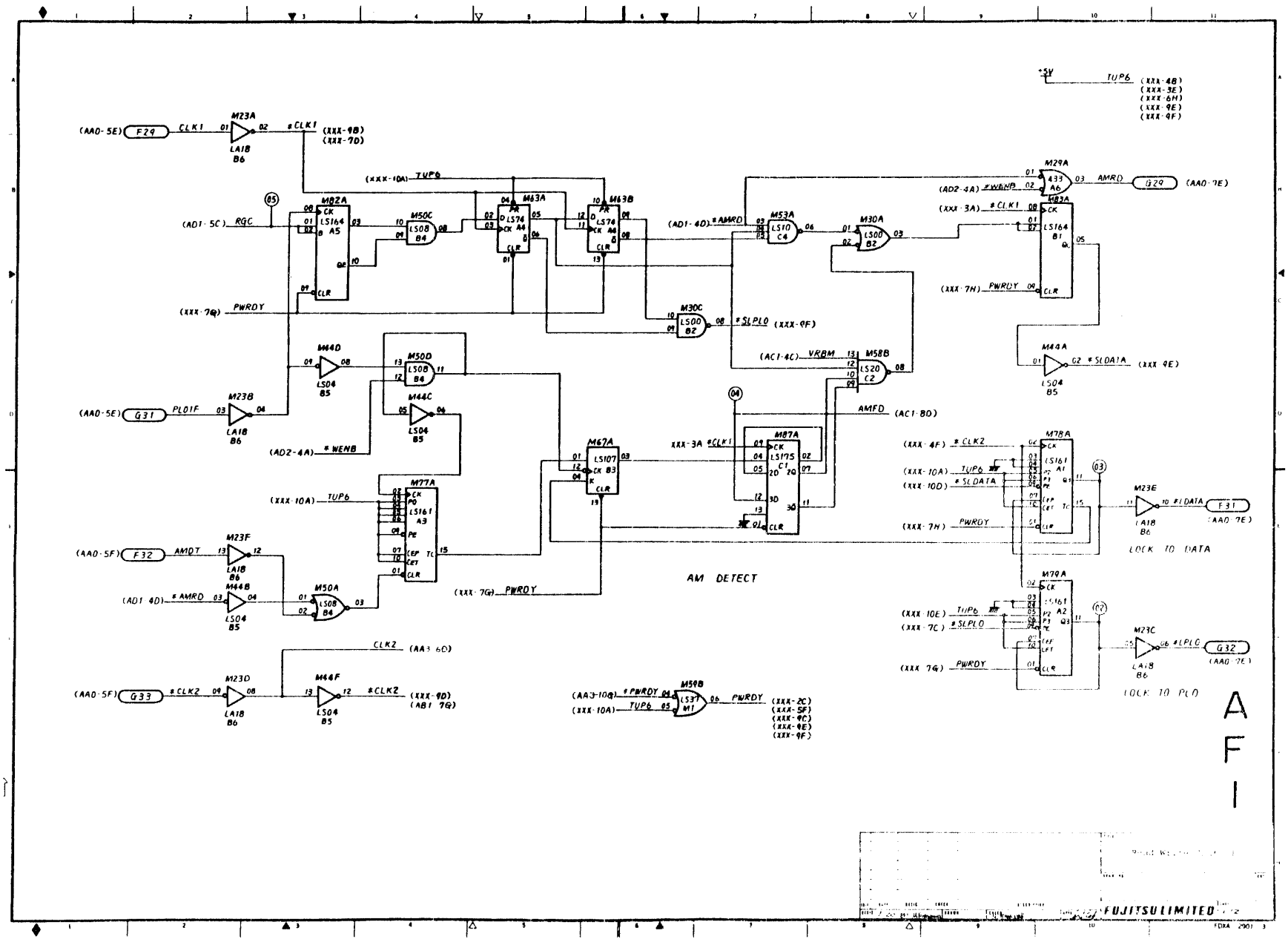
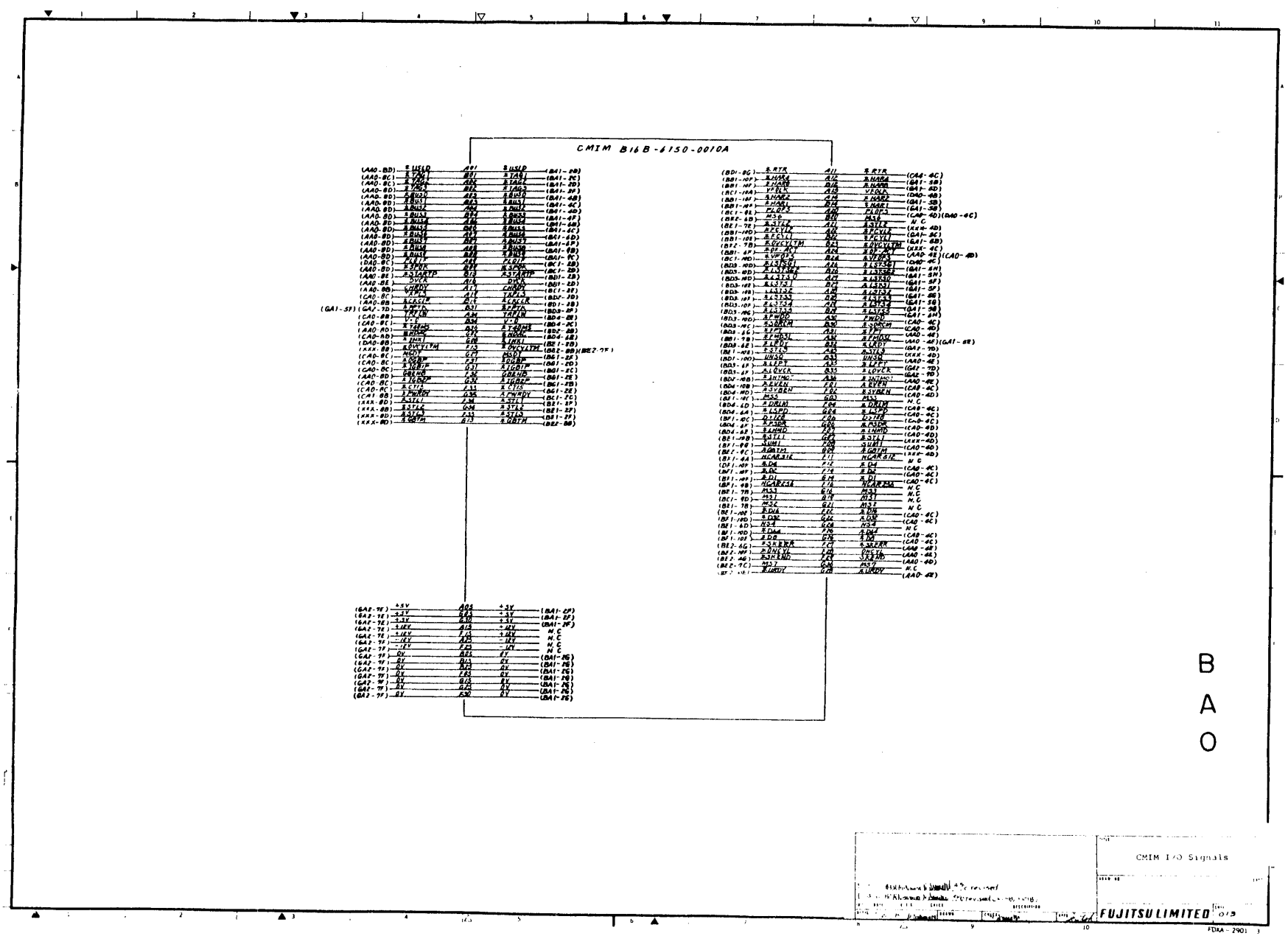

READ/WRITE CHECK DETECT
A
D
2
FUJITSU LIMITED


M71A
M72A
M73A
UNIT STATUS II
MULTIPLEXER AND LED DRIVER
M28A
M28B
M29D
M29C
M28D
M28C
M31A
M31B
M54C
M48B
M43A
M22C
M49D
M22A
M22B
Status Generator (2)
FUJITSU LIMITED
A
E
I


AM DETECT
LOCK TO DATA
LOCK TO PLO
FUJITSU LIMITED


CMIM B16B-6150-0010A
B
A
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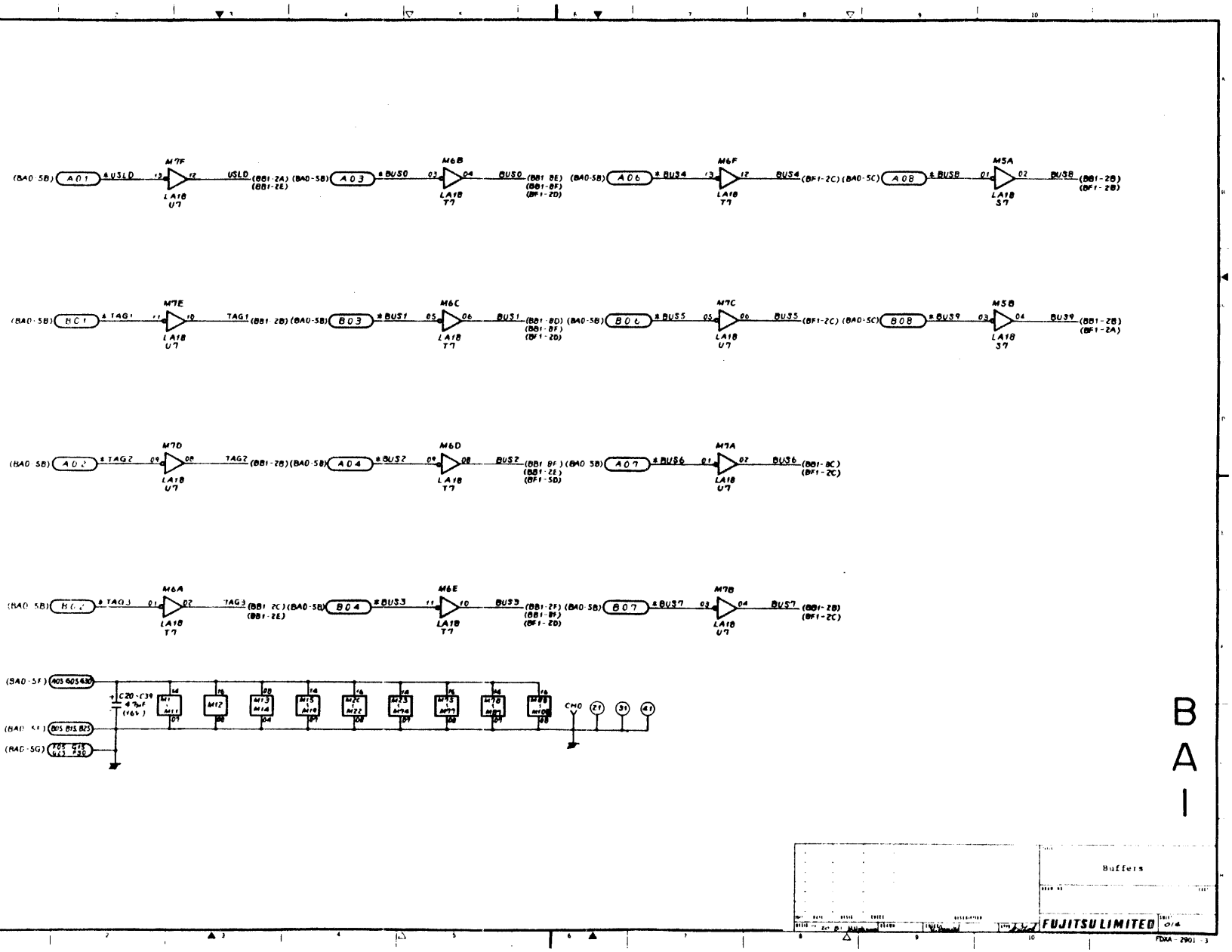
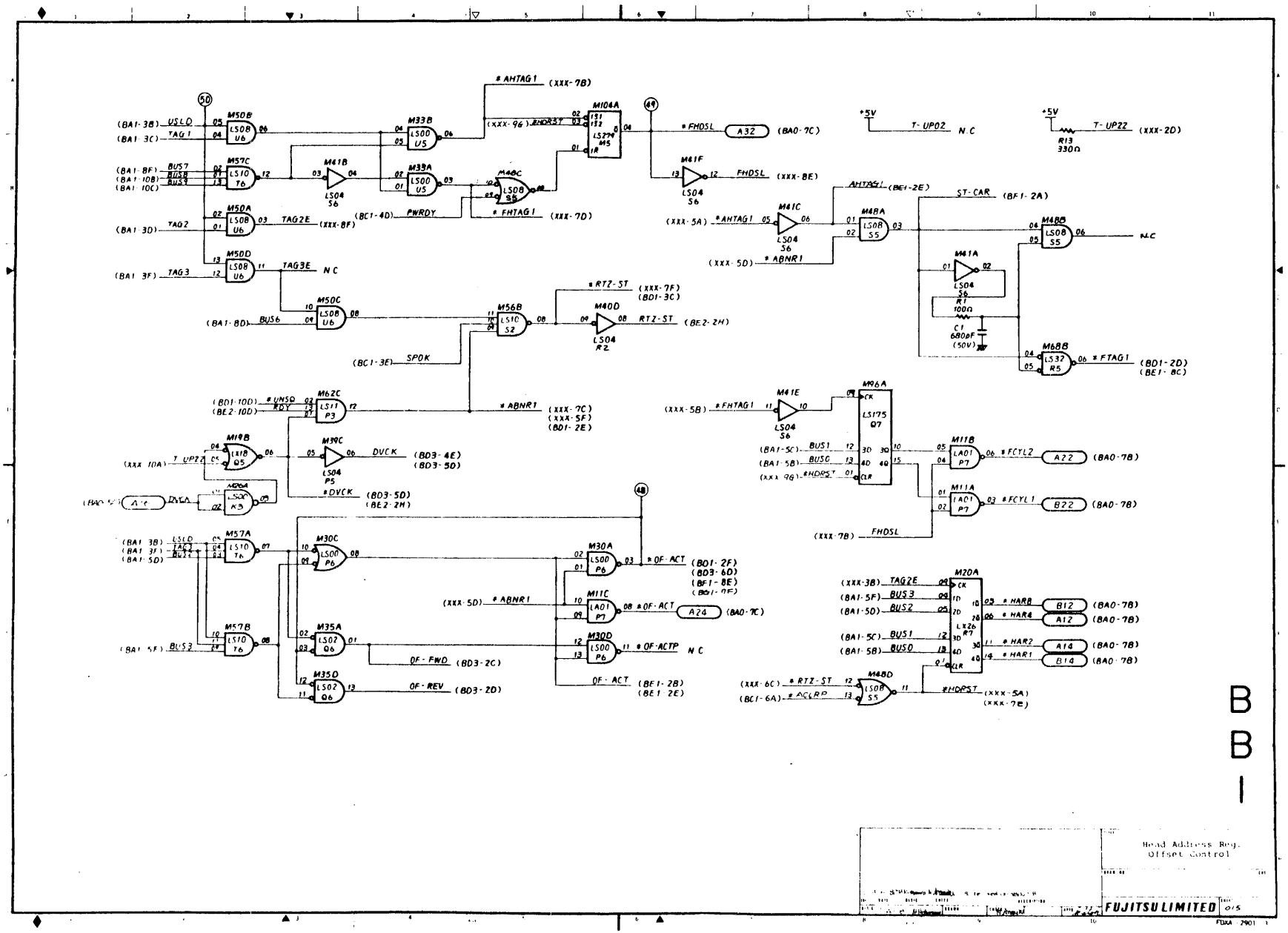
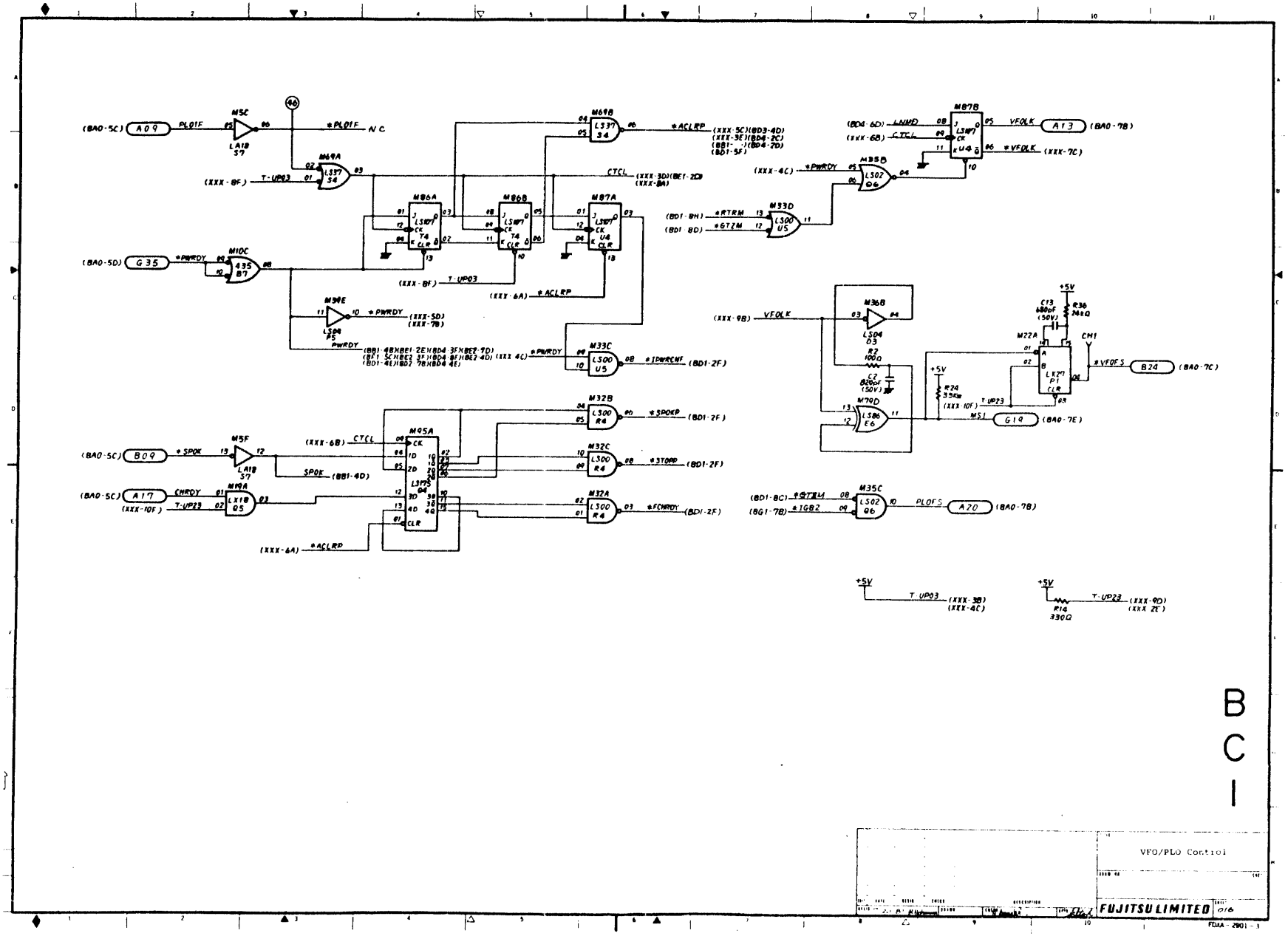
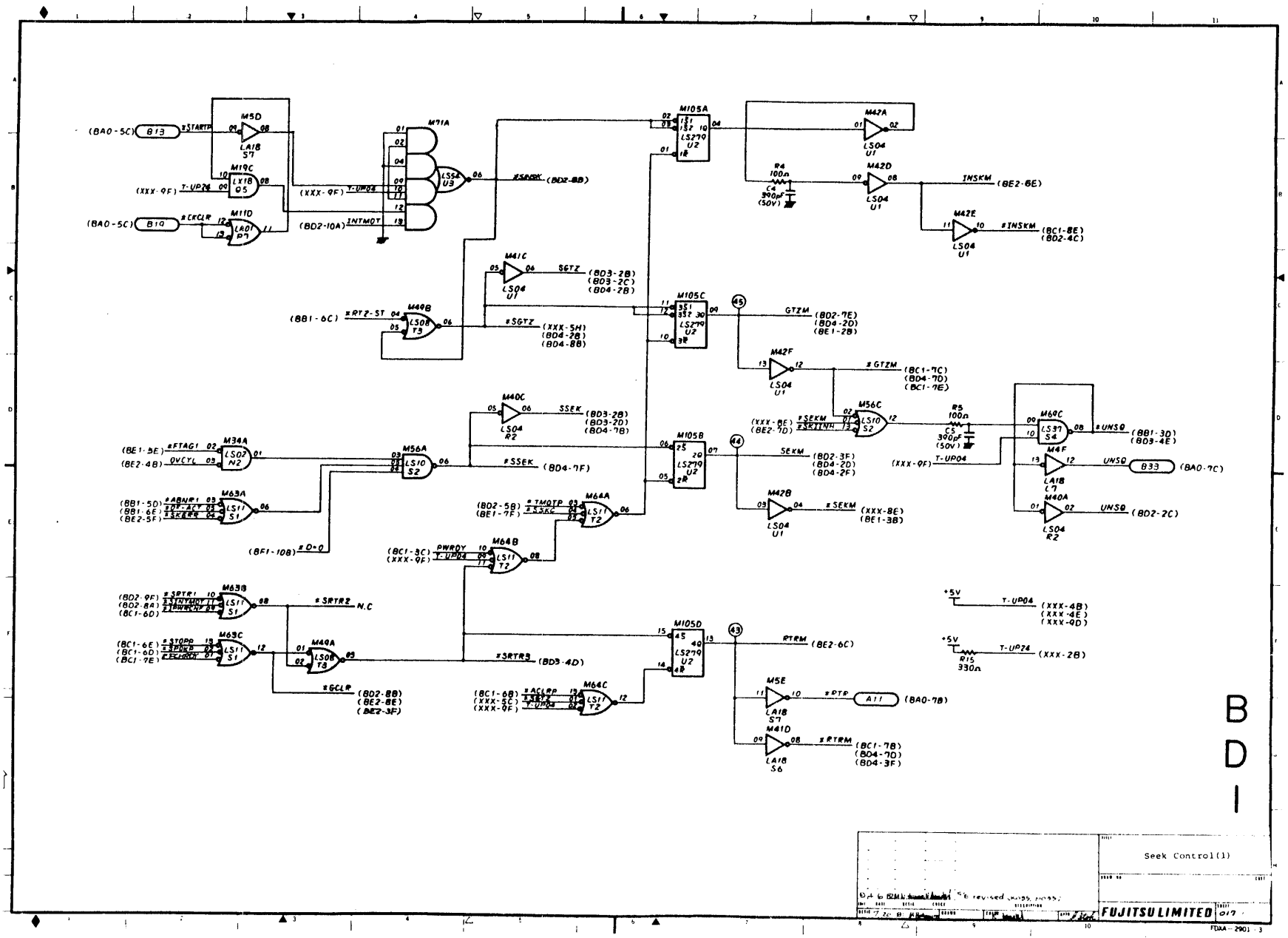
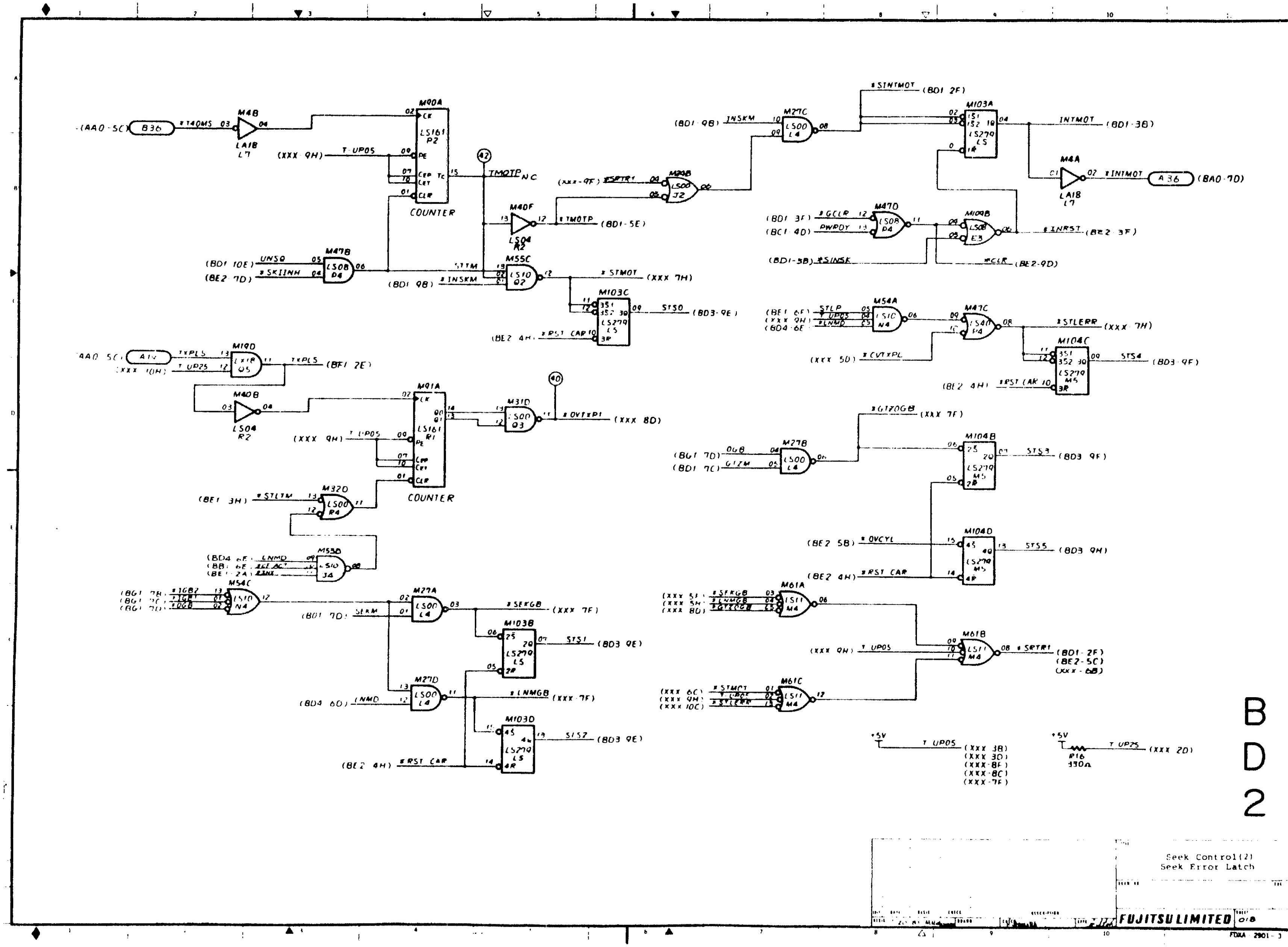
CMIM I/O Signals
FUJITSU LIMITED

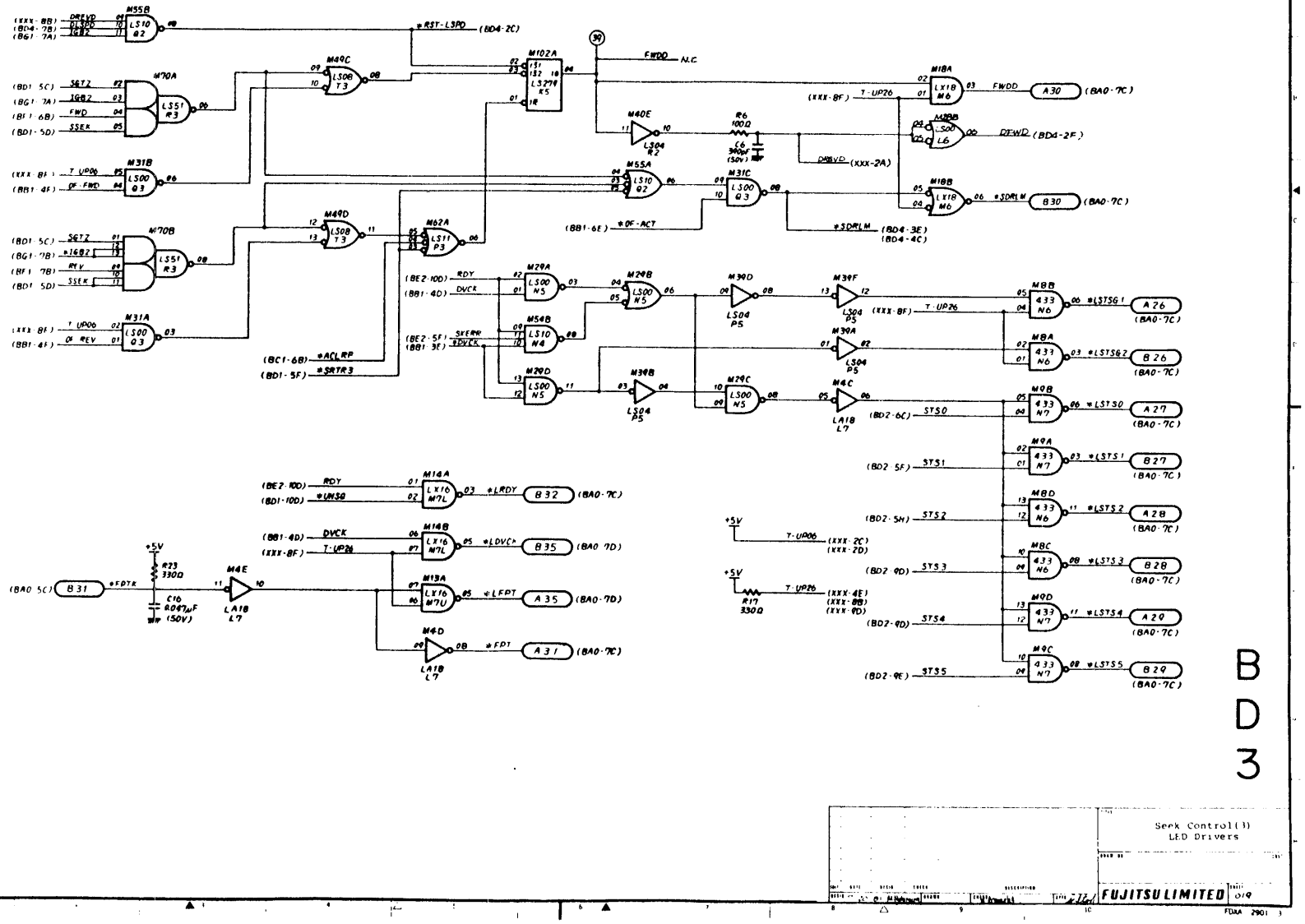

M7F
M6B
M6F
M5A
M7E
M6C
M7C
M5B
M7D
M6D
M7A
M6A
M6E
M7B
LA18
U7
T7
S7
Buffers
FUJITSU LIMITED
B
A
I

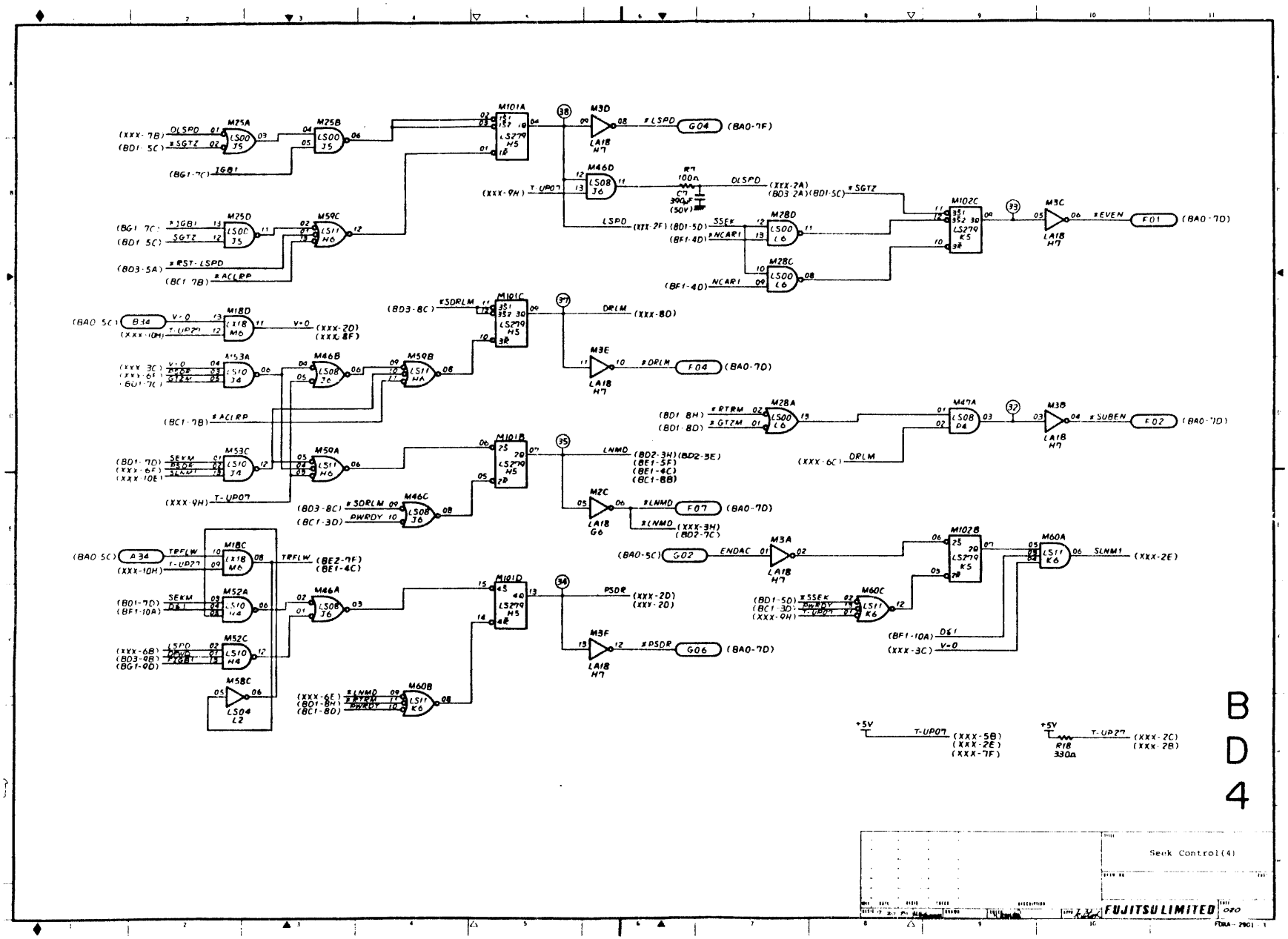

Head Address Reg.
Offset Control
FUJITSU LIMITED
B
B
I

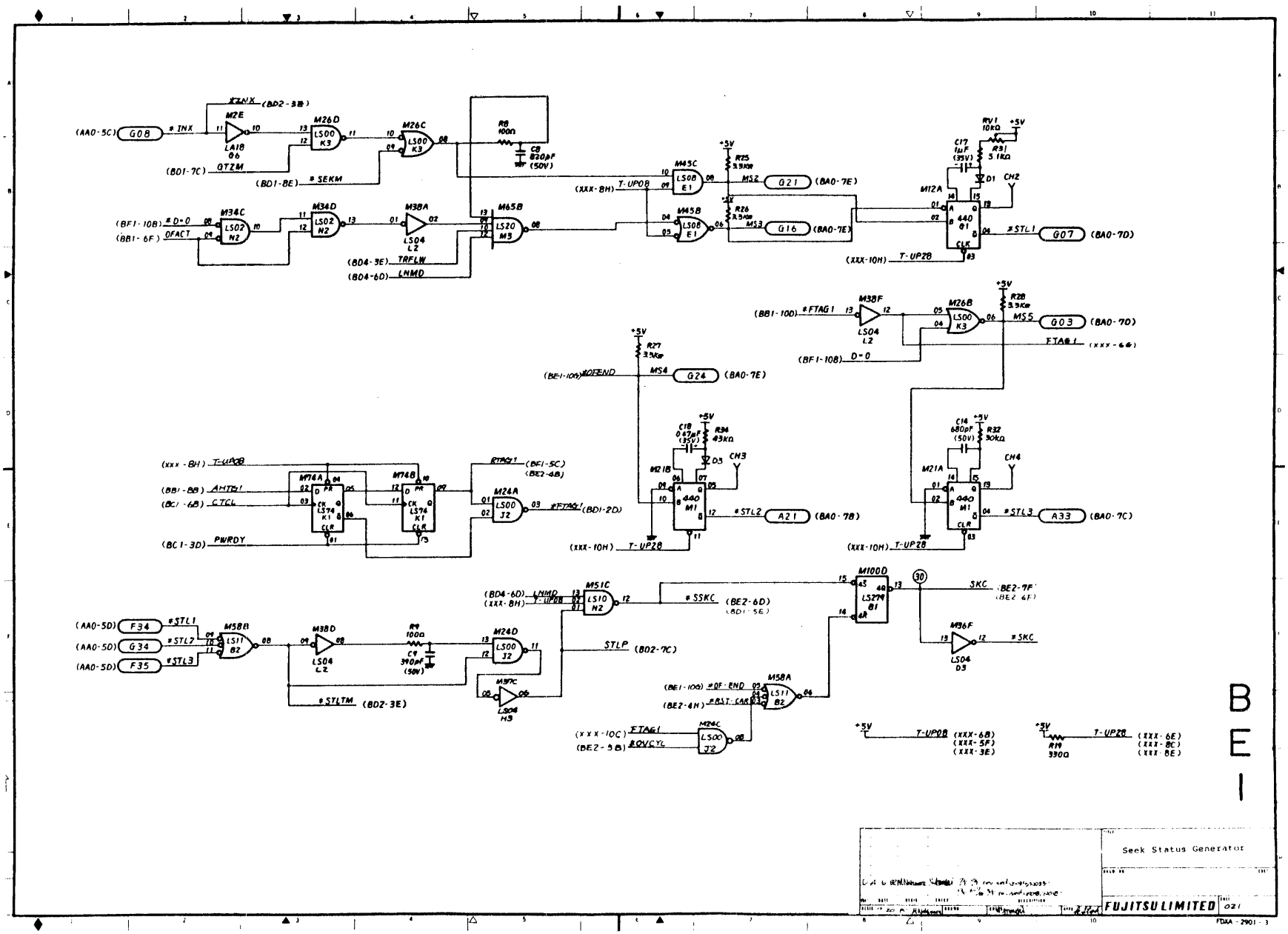

VFO/PLO Control
FUJITSU LIMITED
B C I

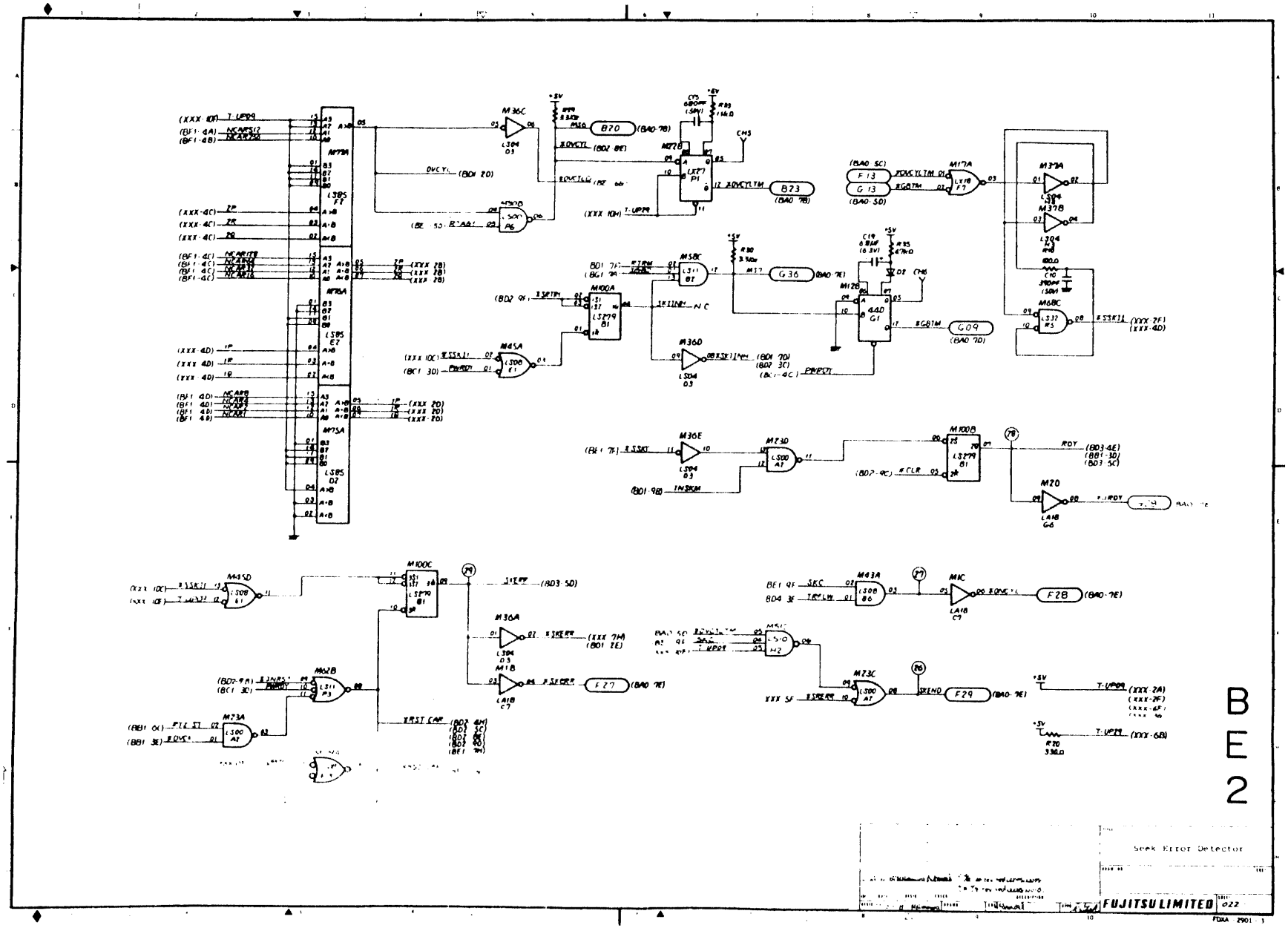

Seek Control(1)
FUJITSU LIMITED
FDAA-2901-3
B
D
I

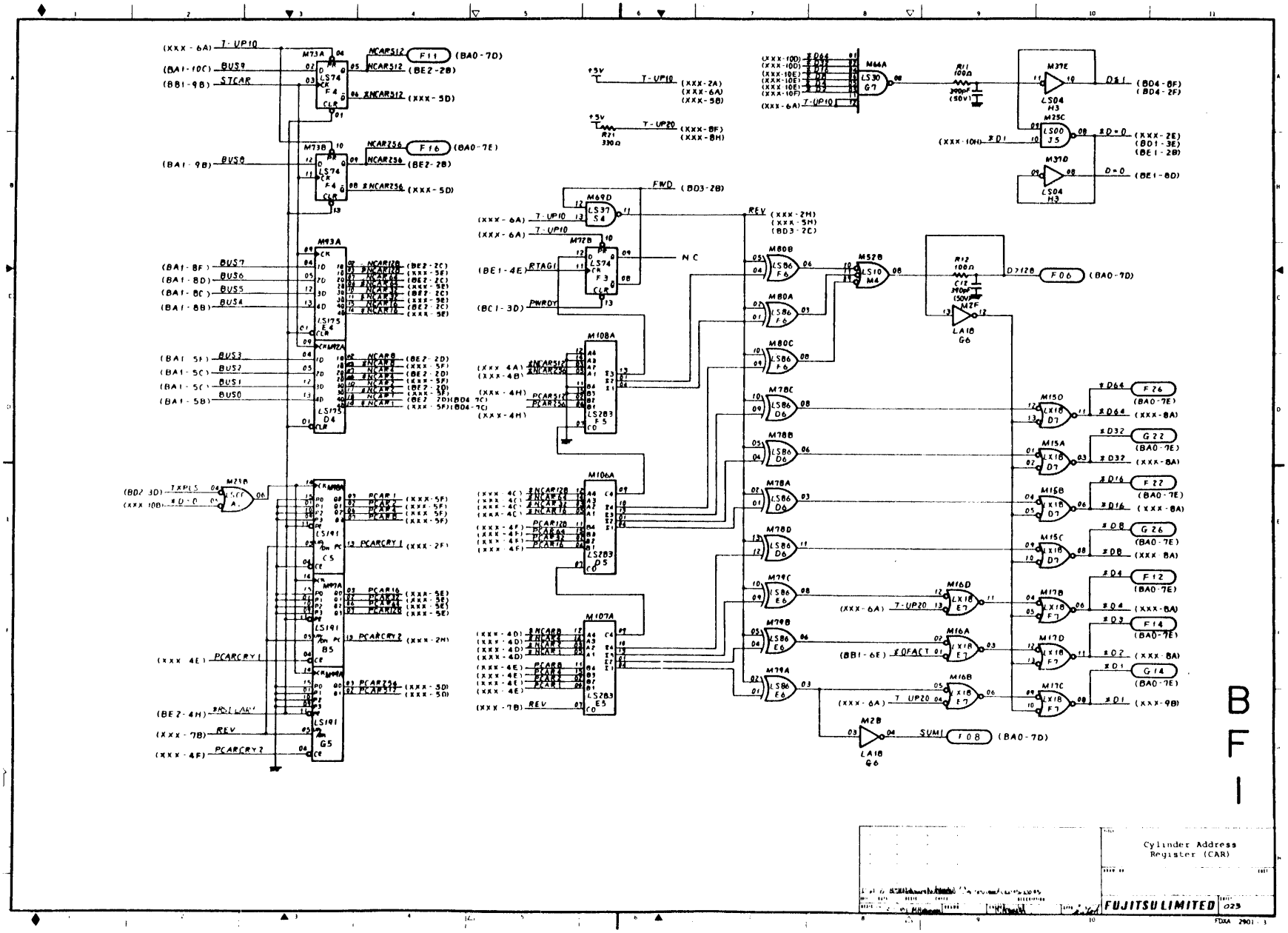

M90A
LS161
COUNTER
M91A
LS161
COUNTER
M103A
M103B
M103C
M103D
M104B
M104C
M104D
LS279
M4A
M4B
LA18
M40F
M40B
LS04
M47B
M47C
M47D
M109B
LS08
M55C
M55B
M54A
M54C
LS10
M27A
M27B
M27C
M27D
M29B
M31D
M32D
LS00
M61A
M61B
M61C
LS11
M19D
R16
390Ω
+5V
Seek Control(2)
Seek Error Latch
FUJITSU LIMITED
BD2

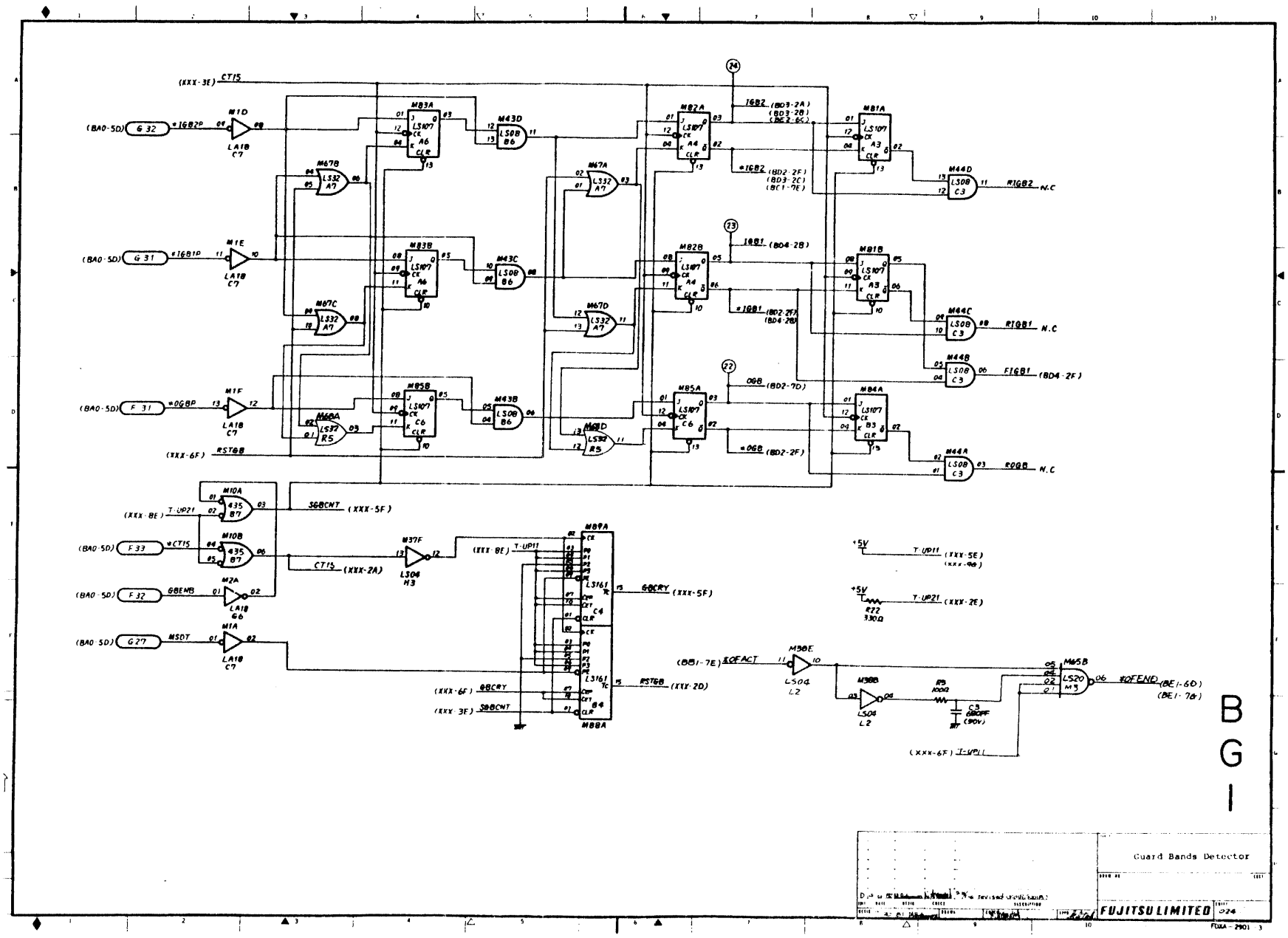

B
D
3
Seek Control(1)
LED Drivers
FUJITSU LIMITED

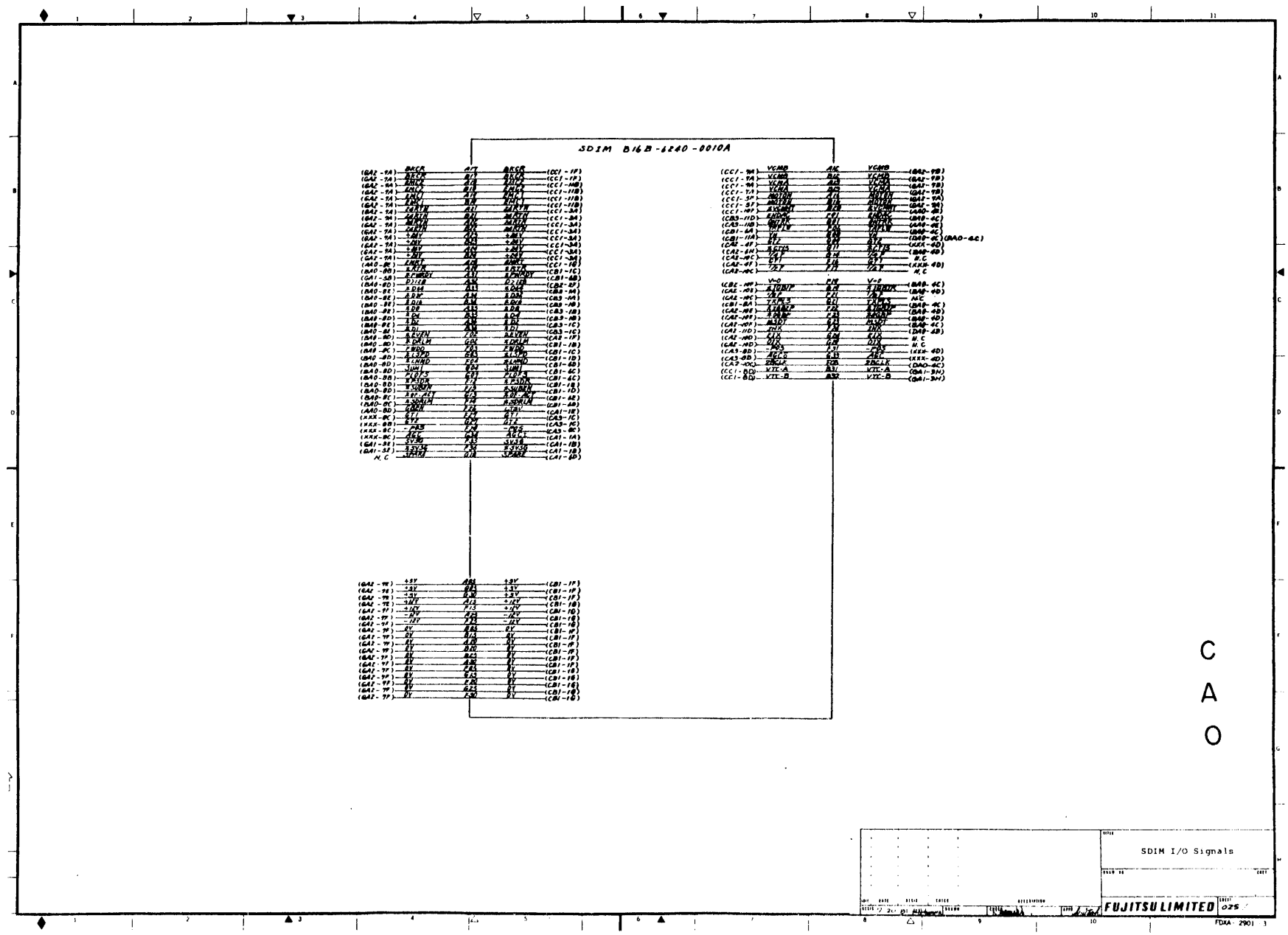

B
D
4
Seek Control(4)
FUJITSU LIMITED
020
FDBA-2901-1


Seek Status Generator
FUJITSU LIMITED
B
E
I

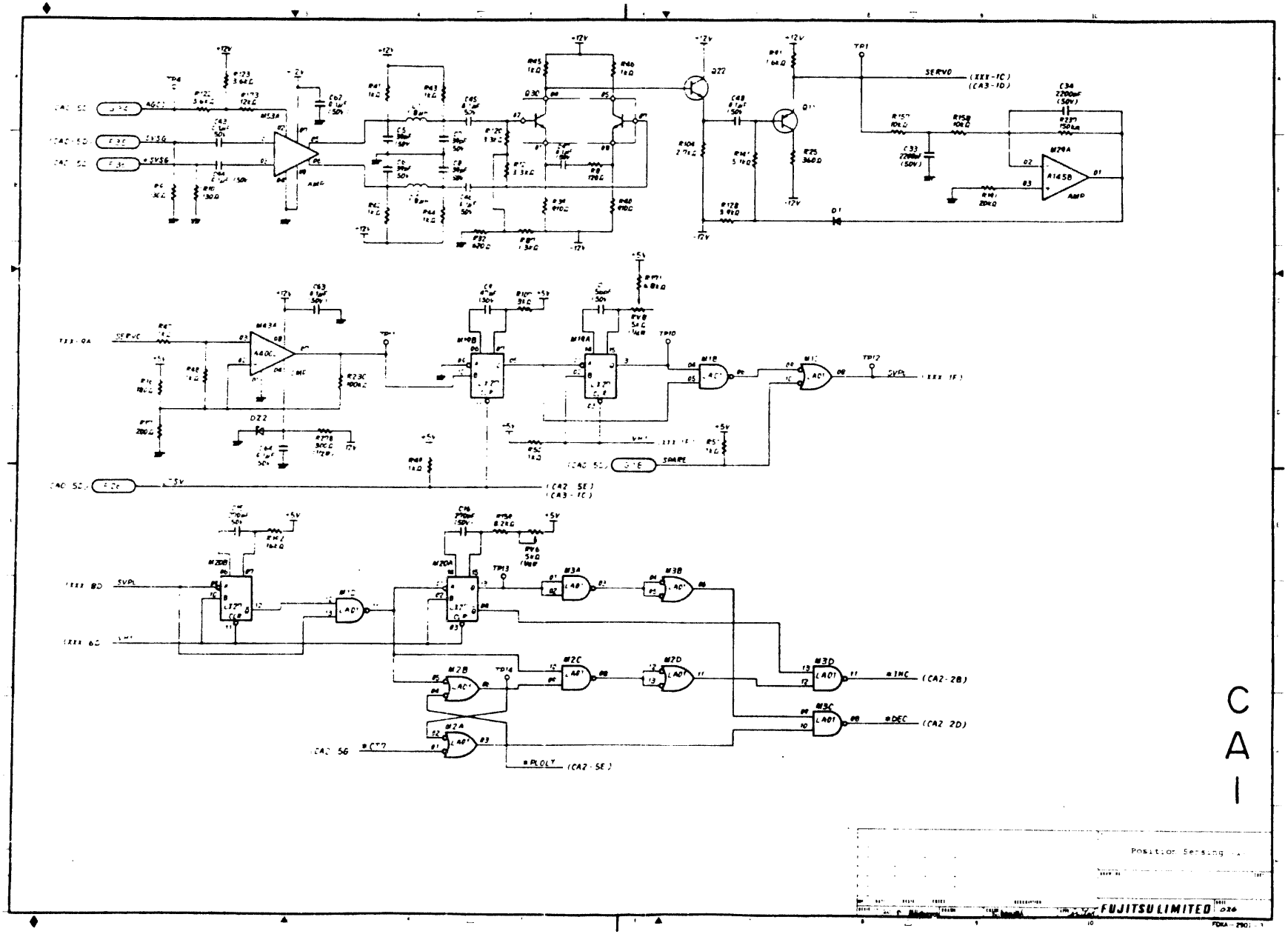

B70
B73
G36
G09
F28
F27
F29
Seek Error Detector
FUJITSU LIMITED
B E 2


Cylinder Address Register (CAR)
FUJITSU LIMITED
B F I

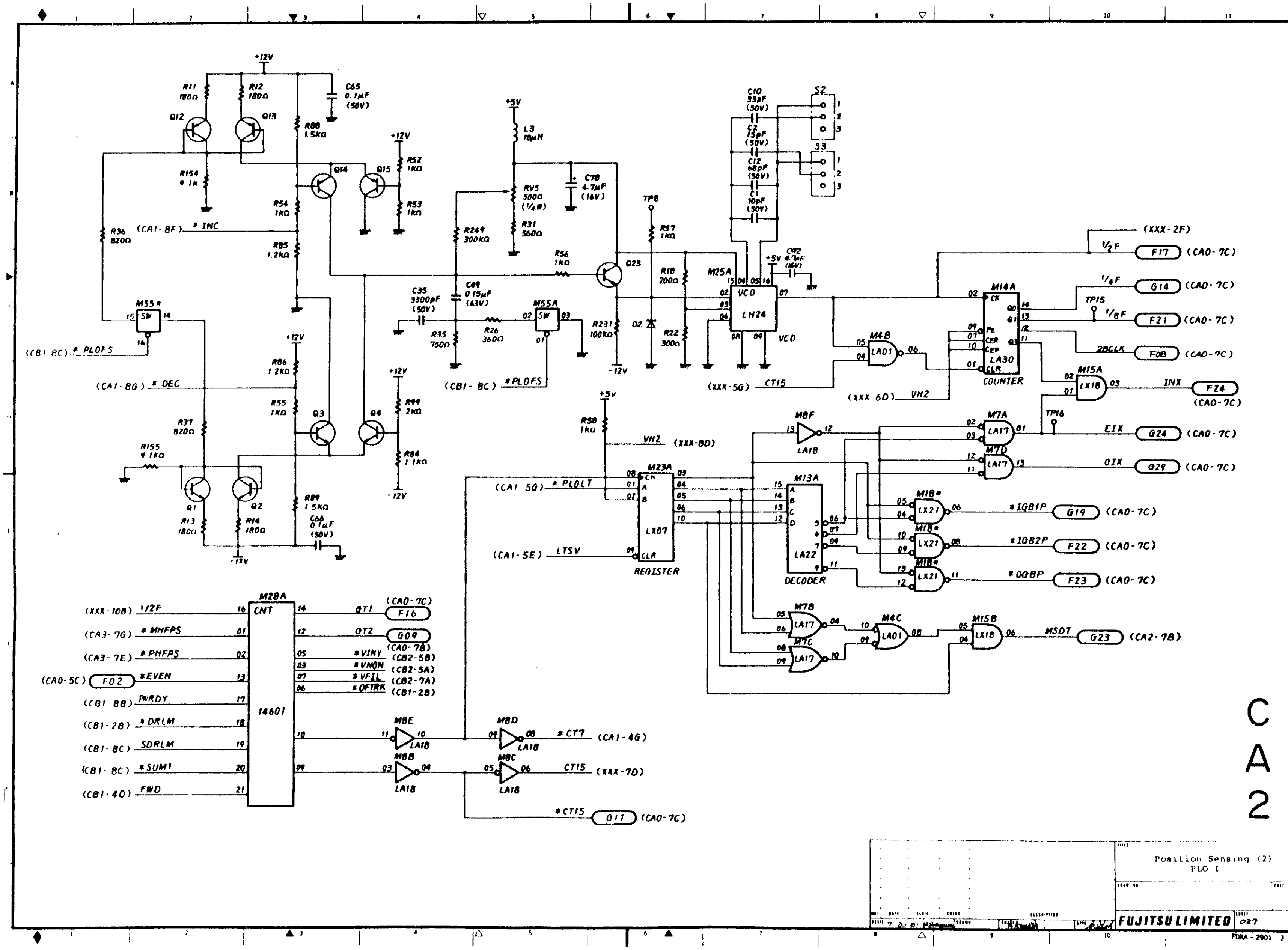

Guard Bands Detector
FUJITSU LIMITED
B G I


SDIM B16B-6240-0010A
SDIM I/O Signals
FUJITSU LIMITED
FDKA-2901

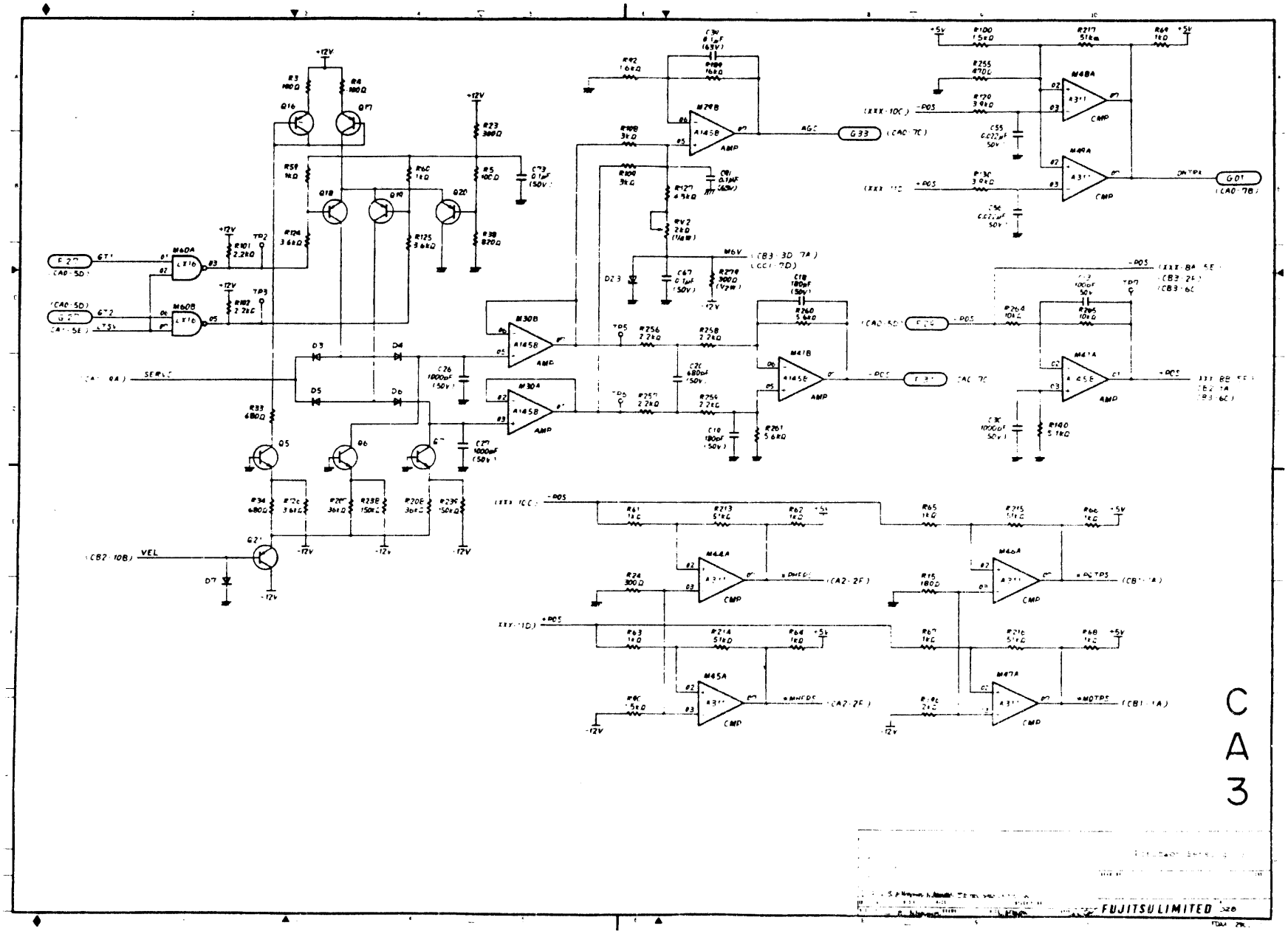
C
A
O

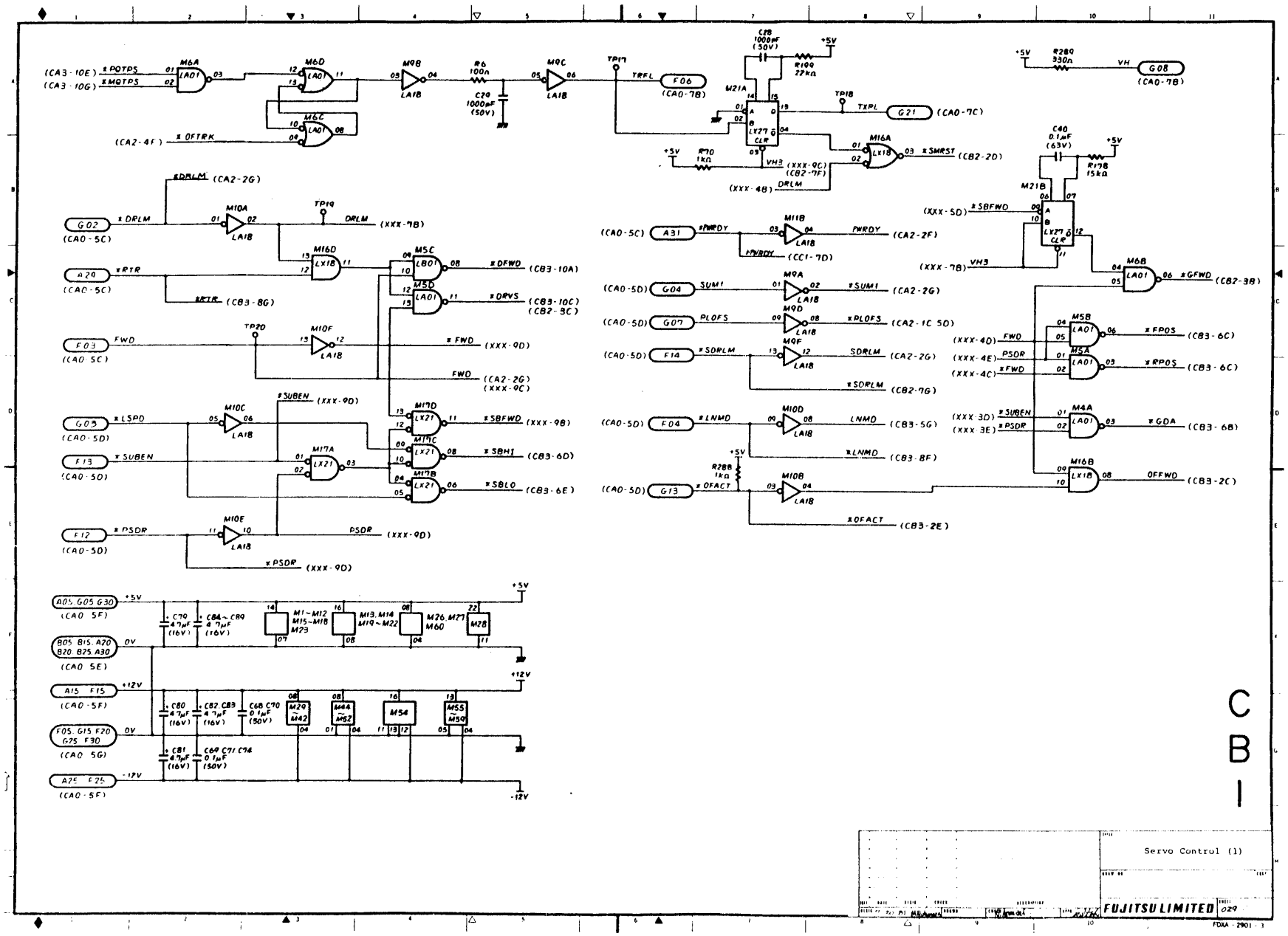

SERVO
(CA3-1C)
(CA2-SE)
(CA3-1C)
(CA2-2B)
(CA2-2D)
(CA2-SE)
Position Sensing
FUJITSU LIMITED

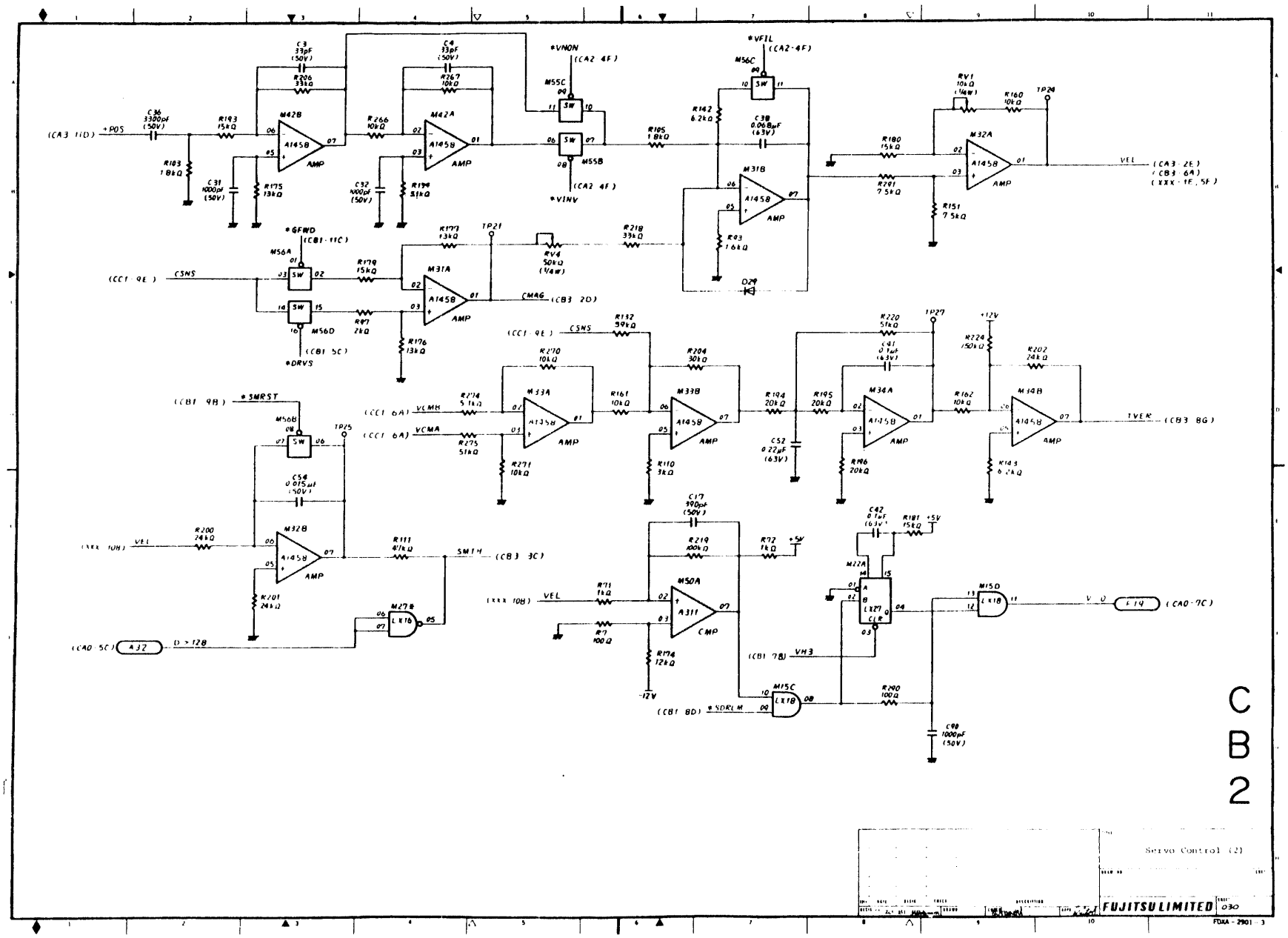
C
A
1

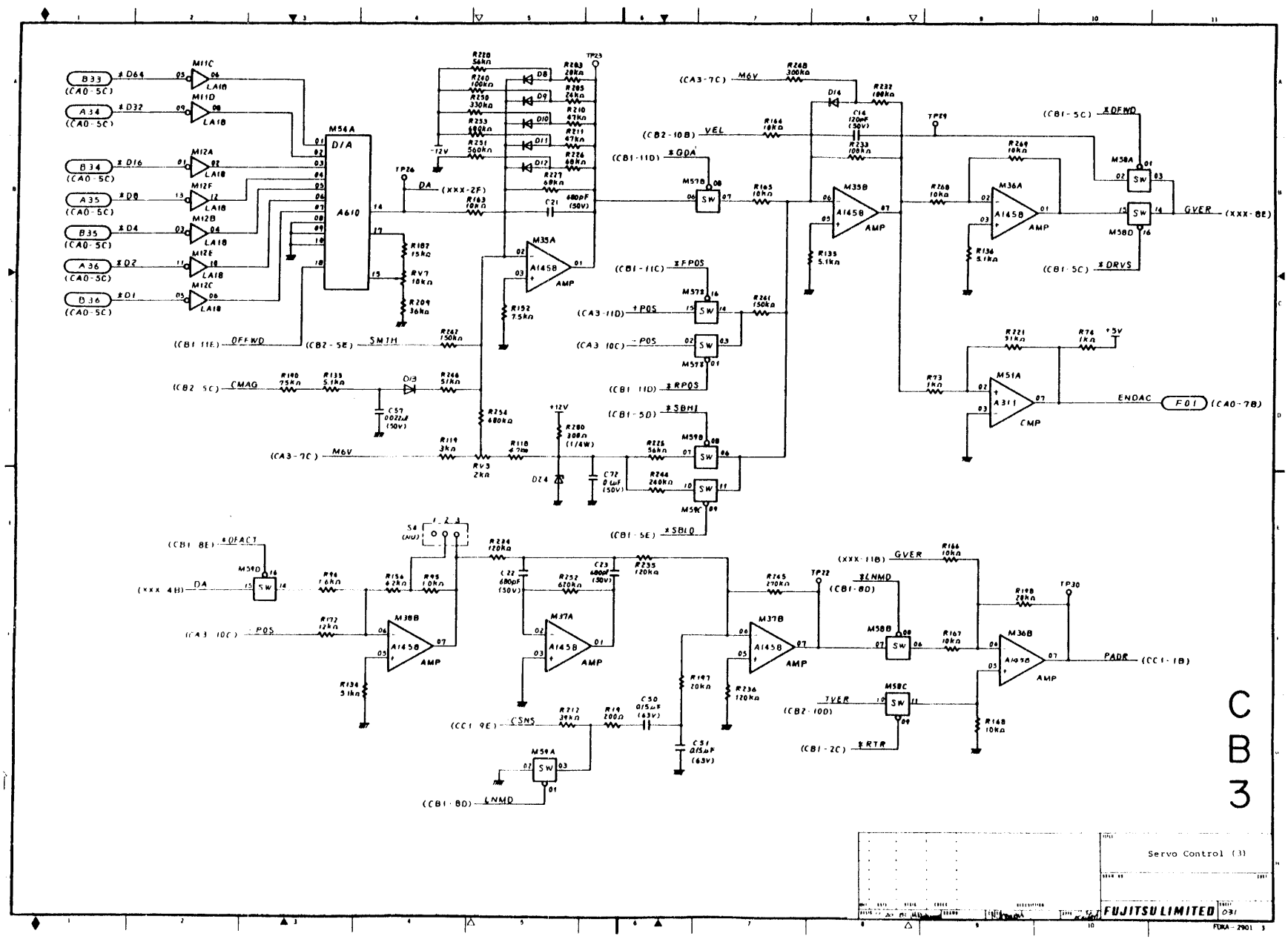


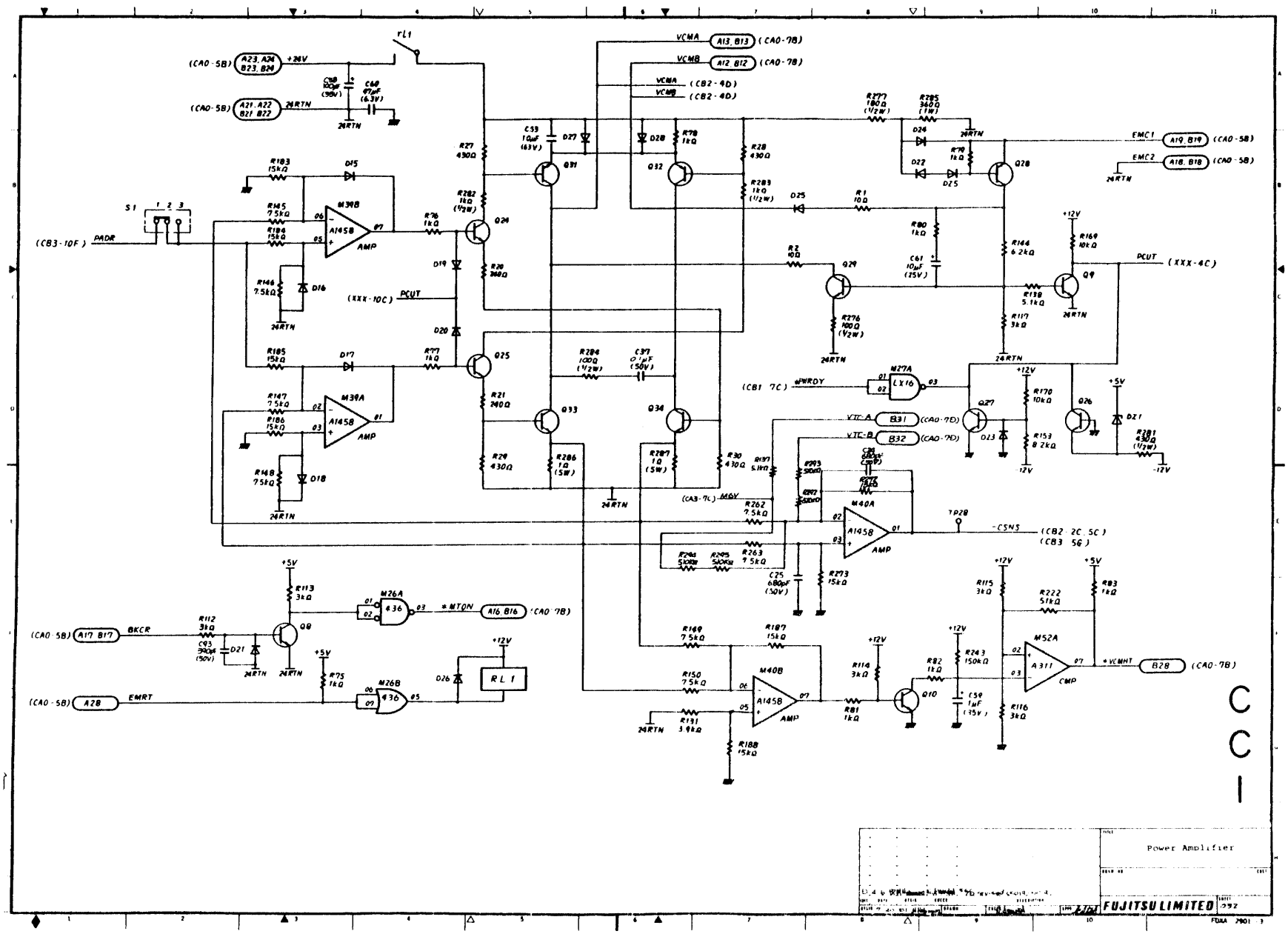
+12V
R11 180Ω
R12 180Ω
C65 0.1μF (50V)
Q12
Q13
R88 1.5kΩ
R154 9.1k
Q14
Q15
R52 1kΩ
R53 1kΩ
R54 1kΩ
R85 1.2kΩ
R36 820Ω
(CA1-8F) * INC
M55* SW
(CB1-8C) * PLOFS
(CA1-8G) * DEC
R86 1.2kΩ
R55 1kΩ
Q3
Q4
R99 2kΩ
R84 1.1kΩ
R37 820Ω
R155 9.1kΩ
Q1
Q2
R13 180Ω
R14 180Ω
R89 1.5kΩ
C66 0.1μF (50V)
-12V
+5V
L3 10μH
RV5 500Ω (1/4W)
R31 560Ω
C78 4.7μF (16V)
R249 300kΩ
C35 3300pF (50V)
C49 0.15μF (63V)
R35 750Ω
R26 360Ω
M55A SW
(CB1-8C) * PLOFS
R56 1kΩ
Q23
R231 100kΩ
TP8
R57 1kΩ
R18 200Ω
D2
R22 300Ω
C10 33pF (50V)
C2 15pF (50V)
C12 68pF (50V)
C1 10pF (50V)
S2
S3
C92 4.7μF (16V)
M25A VCO LH24
(XXX-5G) CT15
(XXX-6D) VH2
M4B LA01
M14A LA30 COUNTER
(XXX-2F)
1/2F F17 (CA0-7C)
1/4F G14 (CA0-7C)
TP15
1/8F F21 (CA0-7C)
2BCLK F08 (CA0-7C)
M15A LX18
INX F24 (CA0-7C)
TP16
R58 1kΩ
VH2 (XXX-8D)
M23A LX07 REGISTER
(CA1-5G) * PLOLT
(CA1-5E) LTSV
M8F LA18
M7A LA17
EIX G24 (CA0-7C)
M7D LA17
OIX G29 (CA0-7C)
M13A LA22 DECODER
M18* LX21
* IGB1P G19 (CA0-7C)
* IGB2P F22 (CA0-7C)
* OGBP F23 (CA0-7C)
M7B LA17
M7C LA17
M4C LA01
M15B LX18
MSDT G23 (CA2-7B)
M28A CNT 14601
(XXX-10B) 1/2F
(CA3-7G) * MHFPS
(CA3-7E) * PHFPS
(CA0-5C) F02 * EVEN
(CB1-8B) PWRDY
(CB1-2B) * DRLM
(CB1-8C) SDRLM
(CB1-8C) * SUM1
(CB1-4D) FWD
QT1 F16 (CA0-7C)
QT2 G09 (CA0-7B)
* VINY (CB2-5B)
* VNON (CB2-5A)
* VFIL (CB2-7A)
* OFTRK (CB1-2B)
M8E LA18
M8D LA18
* CT7 (CA1-4G)
M8B LA18
M8C LA18
CT15 (XXX-7D)
* CT15 G11 (CA0-7C)
CA2
Position Sensing (2) PLO I
FUJITSU LIMITED
FDXA-2901

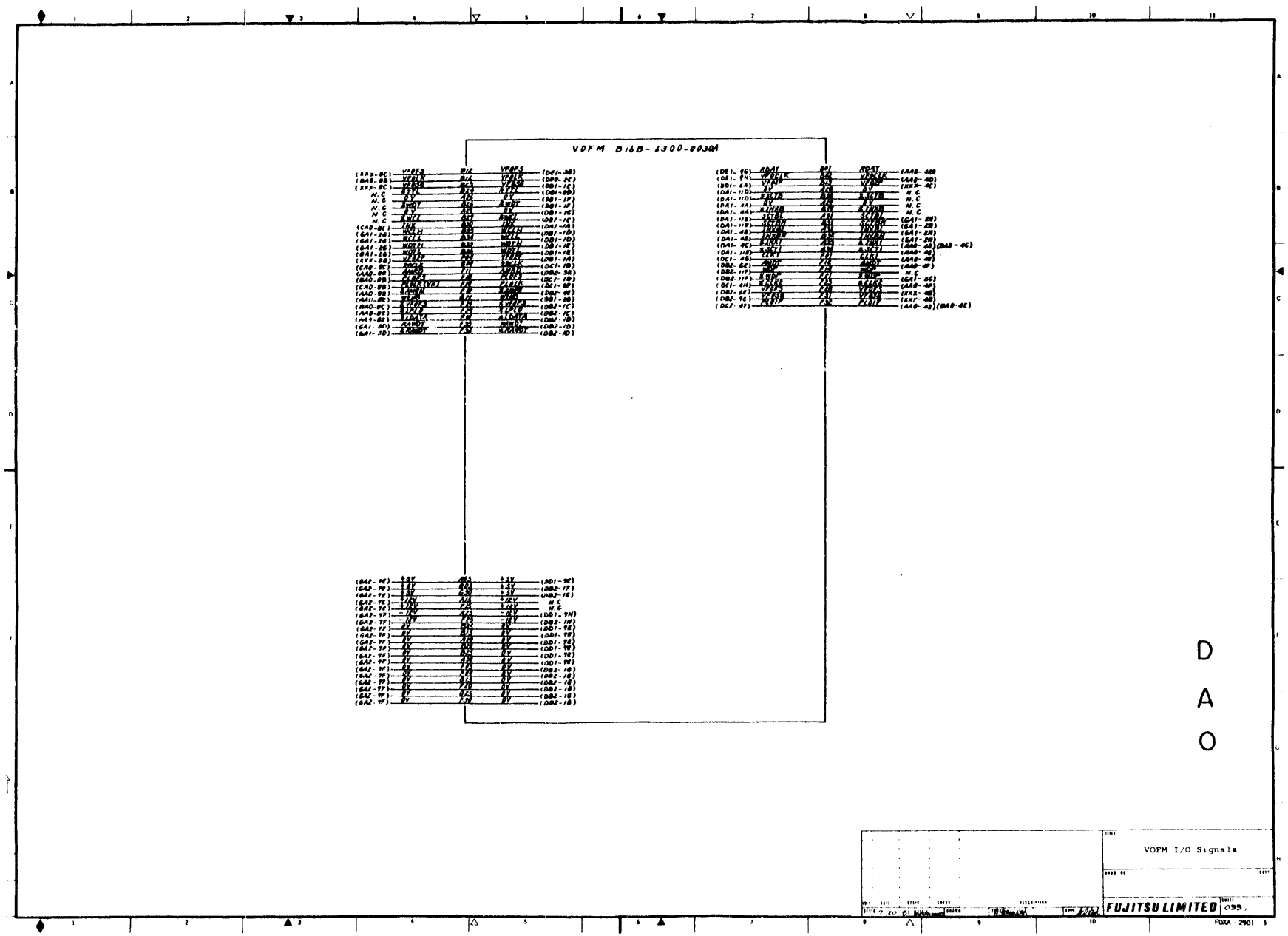

C A 3
FUJITSU LIMITED

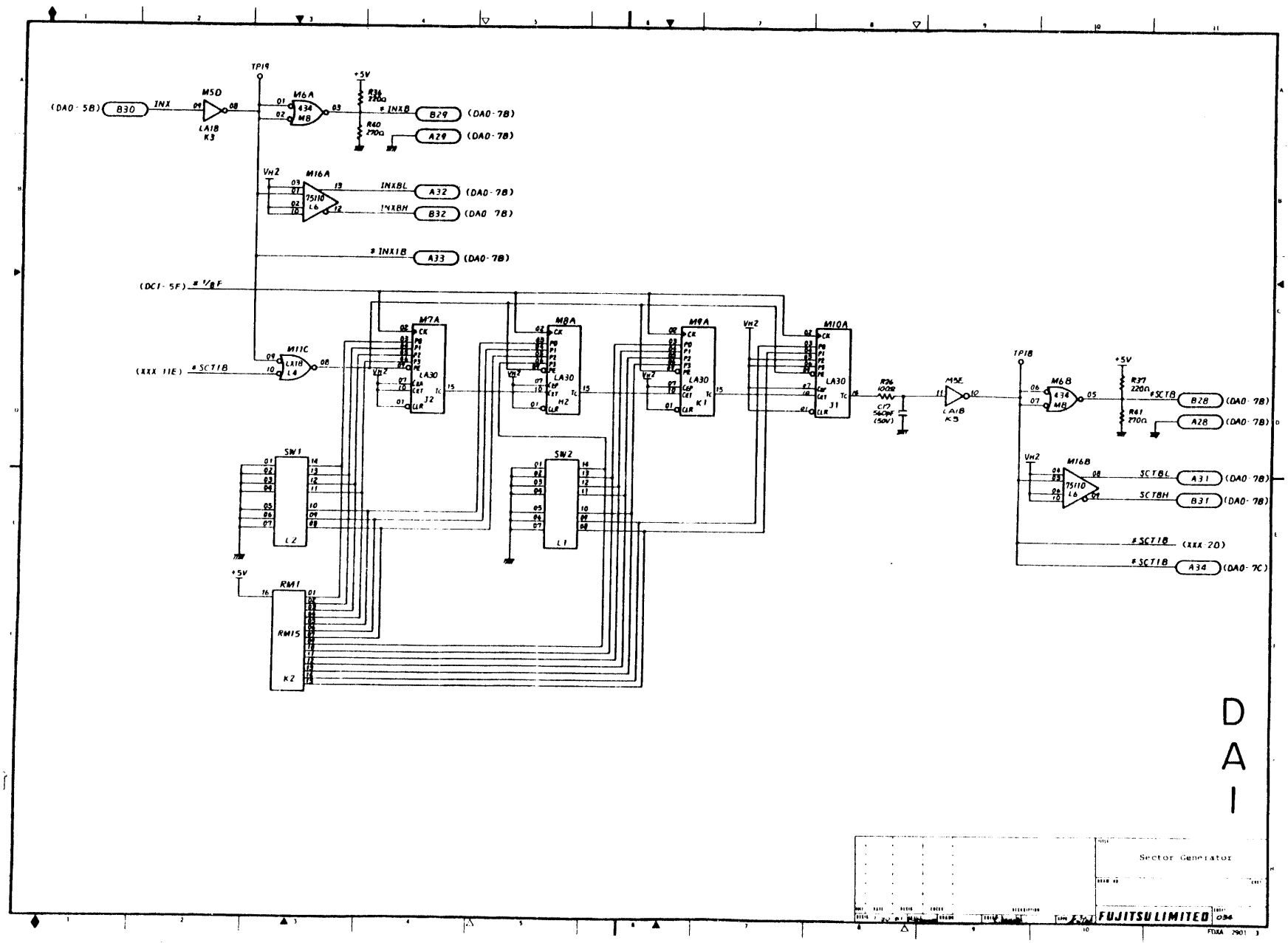

Servo Control (1)
FUJITSU LIMITED
C B I

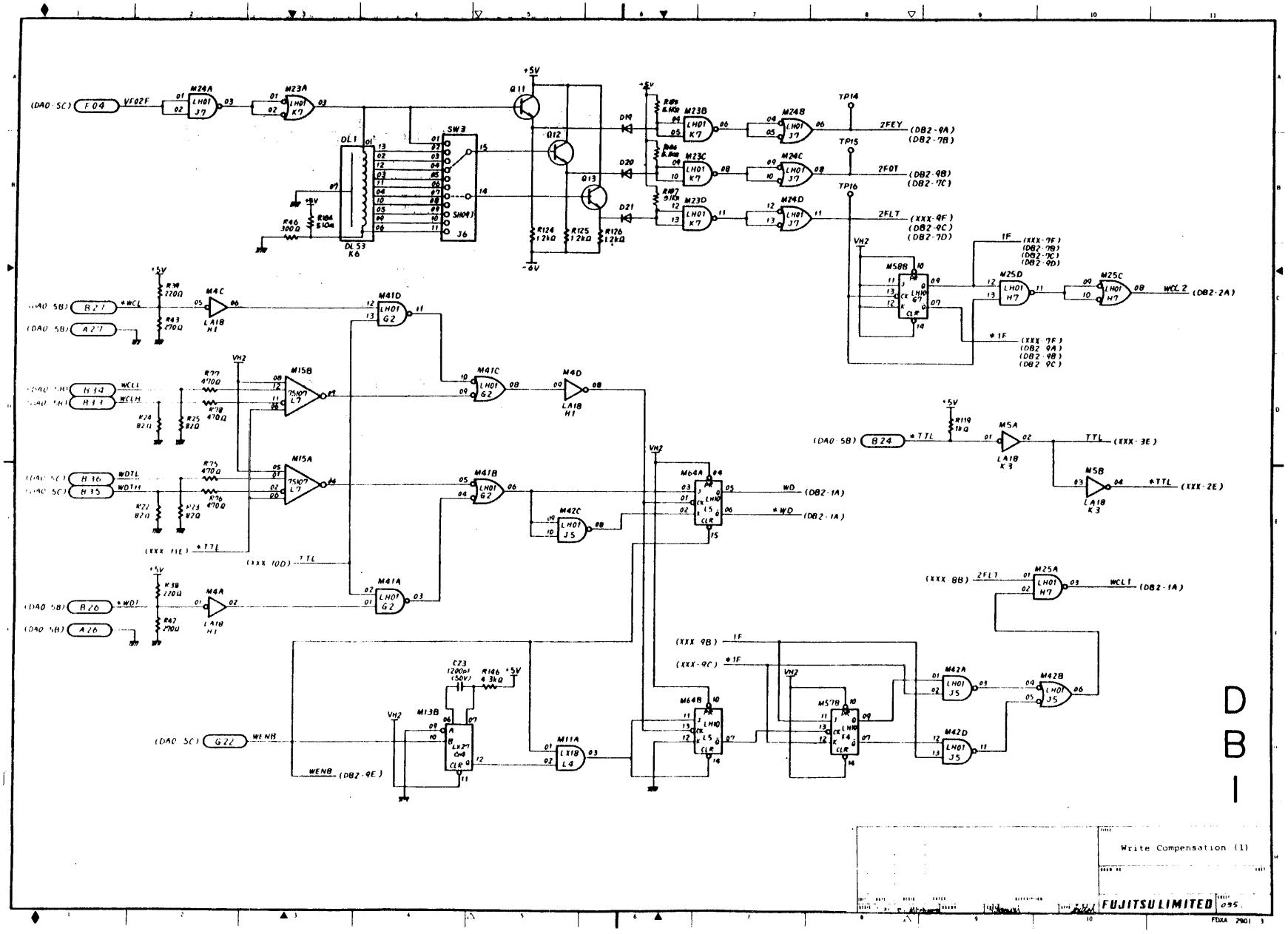

C3 33pF (50V)
C4 33pF (50V)
R206 33kΩ
R267 10kΩ
*VNON (CA2 4F)
*VFIL (CA2-4F)
M55C
M56C
C36 3300pF (50V)
R193 15kΩ
M42B
M42A
R266 10kΩ
R142 6.2kΩ
C38 0.068μF (63V)
RV1 10kΩ (1/4W)
R160 10kΩ
TP24
R183 1.8kΩ
C31 1000pF (50V)
R175 13kΩ
C32 1000pF (50V)
R199 5.1kΩ
M55B
*VINV (CA2 4F)
R105 1.8kΩ
M31B
R180 15kΩ
R191 7.5kΩ
M32A
R151 7.5kΩ
VEL (CA3 2E) (CB3 6A) (XXX-1E, 5F)
R03 1.6kΩ
D29
*GFWD (CB1-11C)
M56A
R177 13kΩ
TP21
R218 39kΩ
RV4 50kΩ (1/4W)
R179 15kΩ
M31A
CMAG (CB3 2D)
M56D
R97 2kΩ
R176 13kΩ
*DRVS (CB1 5C)
R132 59kΩ
R220 5kΩ
TP27
+12V
C41 0.1μF (63V)
R224 150kΩ
R202 24kΩ
R210 10kΩ
R204 50kΩ
M33A
M33B
R161 10kΩ
R104 20kΩ
R195 20kΩ
M34A
R162 10kΩ
M34B
TVER (CB3 8G)
R274 5.1kΩ
R275 51kΩ
R271 10kΩ
R110 3kΩ
C52 0.22μF (63V)
R196 20kΩ
R143 6.2kΩ
*SMRST (CB1 9B)
M56B
TP25
C54 0.015μF (50V)
C17 390pF (50V)
R219 100kΩ
R72 1kΩ
+5V
C42 0.1μF (63V)
R181 15kΩ
M32B
R200 24kΩ
R111 47kΩ
SMTH (CB3 3C)
R201 24kΩ
M27B
M50A
R71 1kΩ
R7 100Ω
R174 12kΩ
-12V
M22A
M27A
M15D
M15C
VH3 (CB1 7B)
*SDRLM (CB1 8D)
R190 100Ω
C99 1000pF (50V)
V_U
F14 (CA0-7C)
A32
D>128 (CA0 5C)
C B 2
Servo Control (2)
FUJITSU LIMITED
FDXA-2901-3

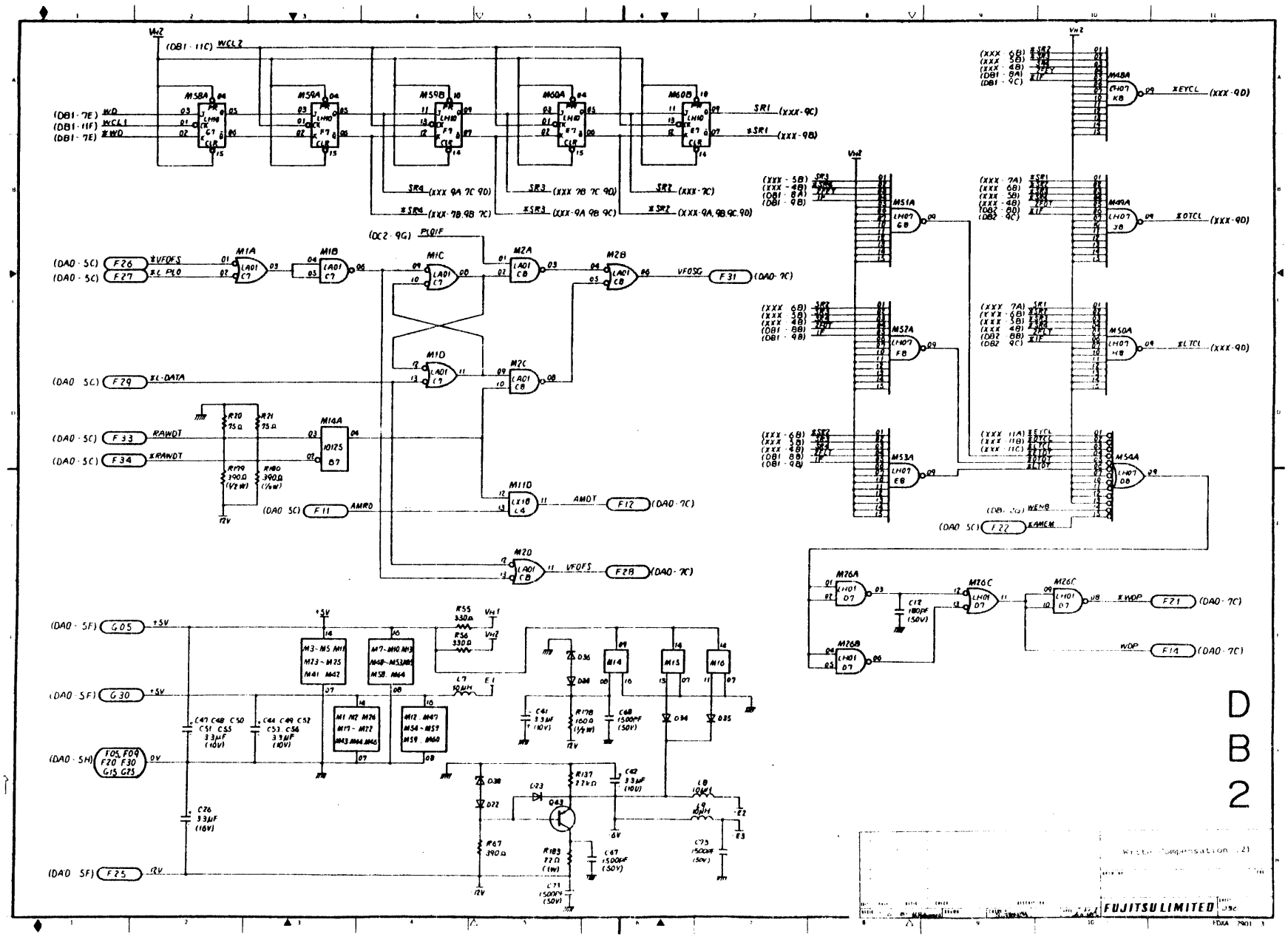

C B 3
Servo Control (3)
FUJITSU LIMITED
FUNA-2901

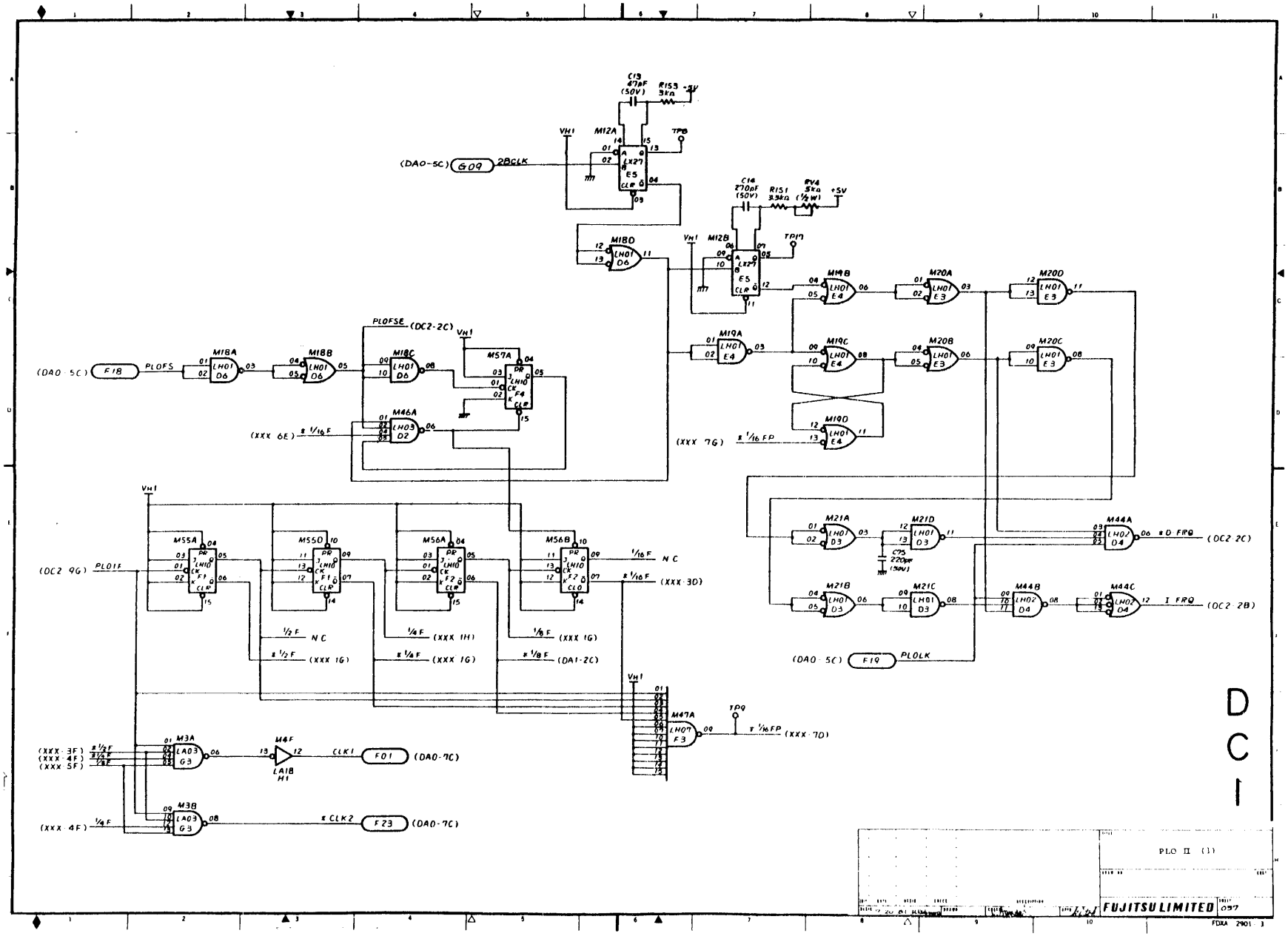

Power Amplifier
FUJITSU LIMITED
C C I
PADR
PCUT
EMRT
BKCR
EMC1
EMC2
VCMA
VCMB
-CSNS
+VCMHT
*MTON
M39B
M39A
M40A
M40B
M26A
M26B
M27A
M52A
AMP
CMP
+12V
+5V
-12V
24RTN

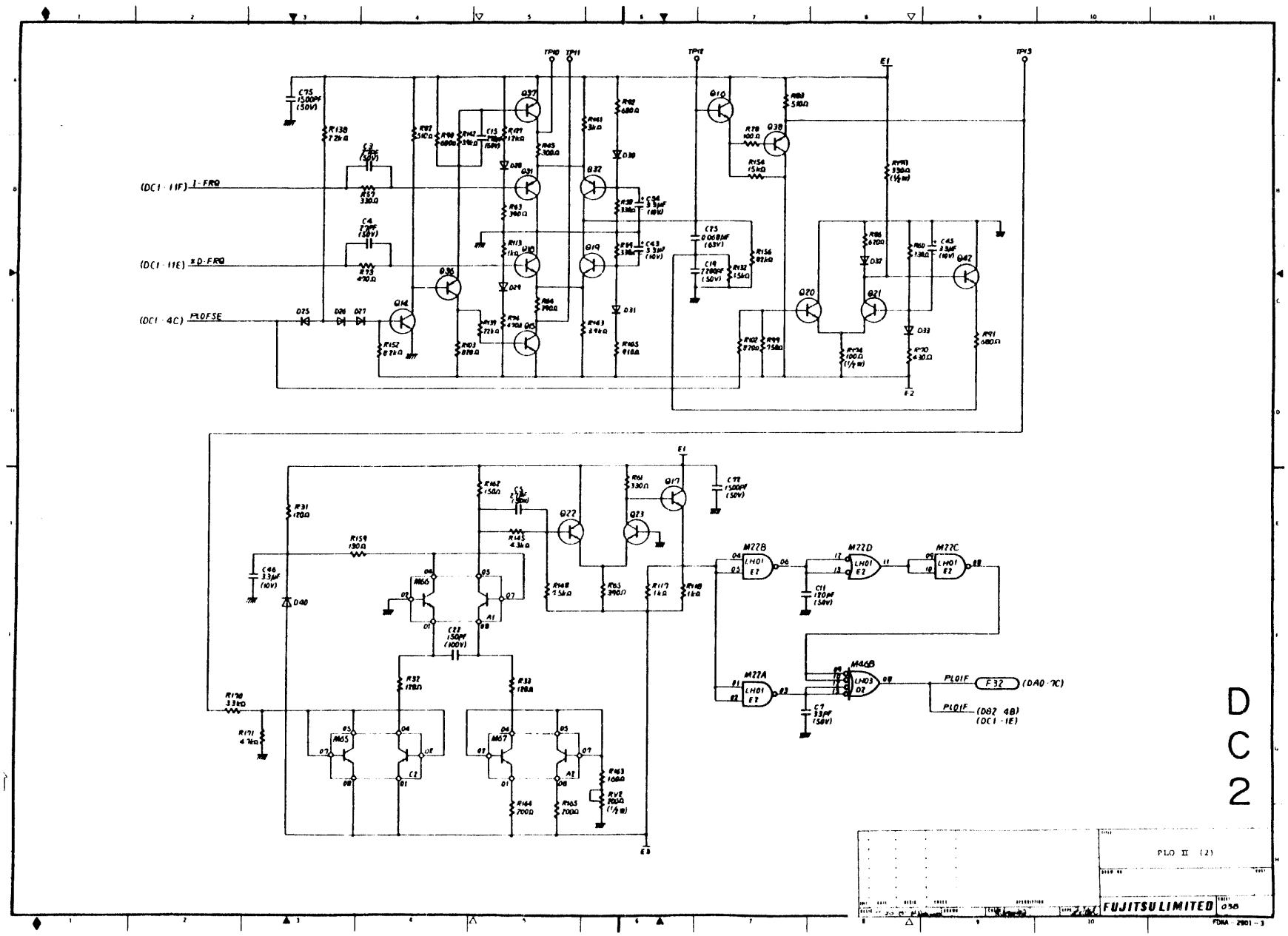

VOFM B16B-4300-0030A
D
A
O
VOFM I/O Signals
FUJITSU LIMITED
FDKA 2901 3

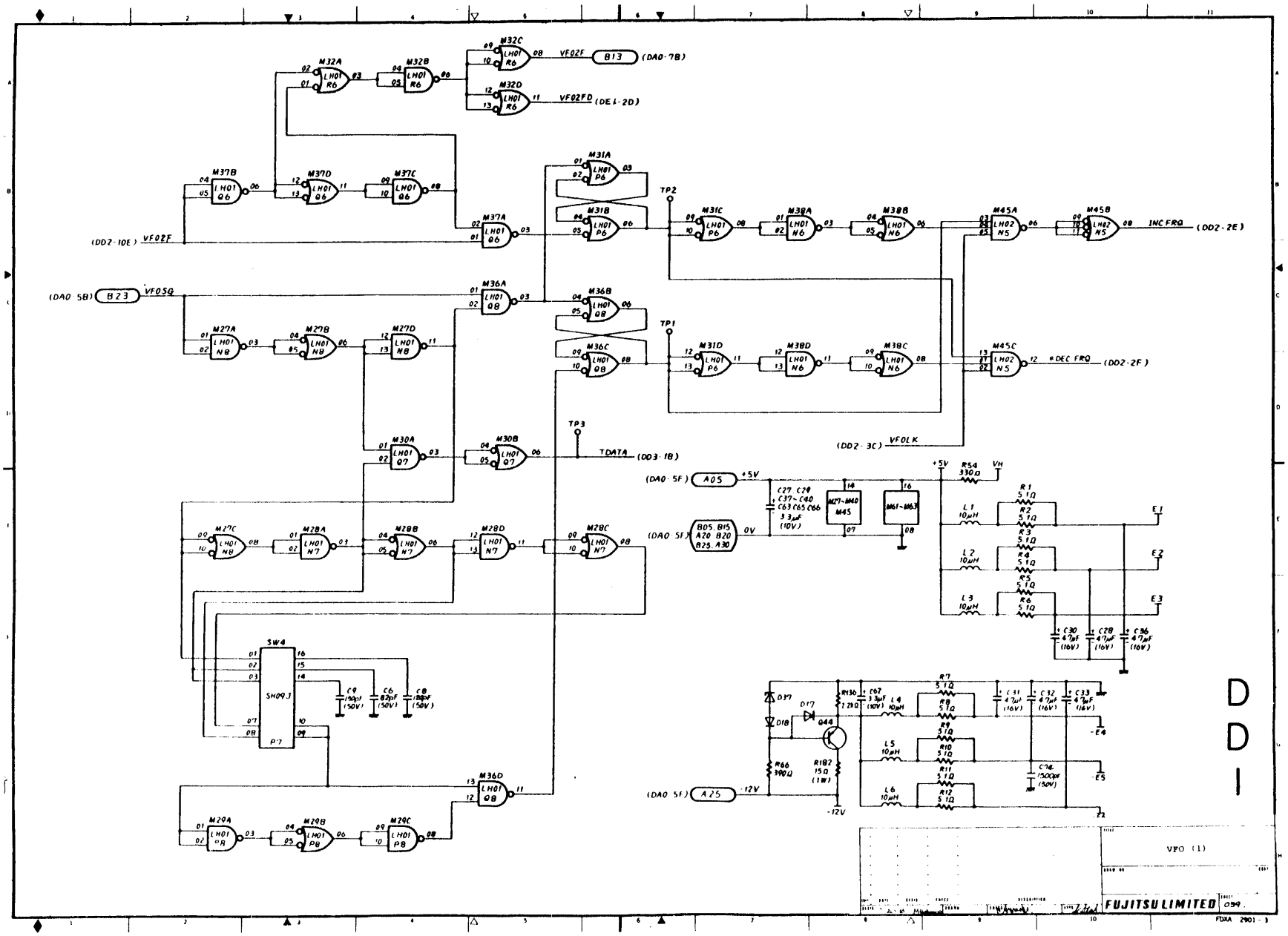

TP19
+5V
M5D
M6A
INX
(DA0-5B)
B30
LA18
K3
INXB
B29
(DA0-7B)
A29
(DA0-7B)
R34 220Ω
R60 270Ω
VH2
M16A
INXBL
A32
(DA0-7B)
INXBH
B32
(DA0-7B)
INX1B
A33
(DA0-7B)
(DC1-5F)
1/8F
M7A
M8A
M9A
M10A
M11C
(XXX 11E)
SCT1B
LA30
J2
M2
K1
J1
SW1
SW2
L2
L1
RM1
RM15
K2
R26 100Ω
C17 560PF (50V)
M5E
LA18
K5
TP18
M6B
R37 220Ω
R61 270Ω
#SCTB
B28
(DA0-7B)
A28
(DA0-7B)
M16B
SCTBL
A31
(DA0-7B)
SCTBH
B31
(DA0-7B)
SCT1B
(XXX 20)
SCT1B
A34
(DA0-7C)
75110
L6
D
A
I
Sector Generator
FUJITSU LIMITED
034

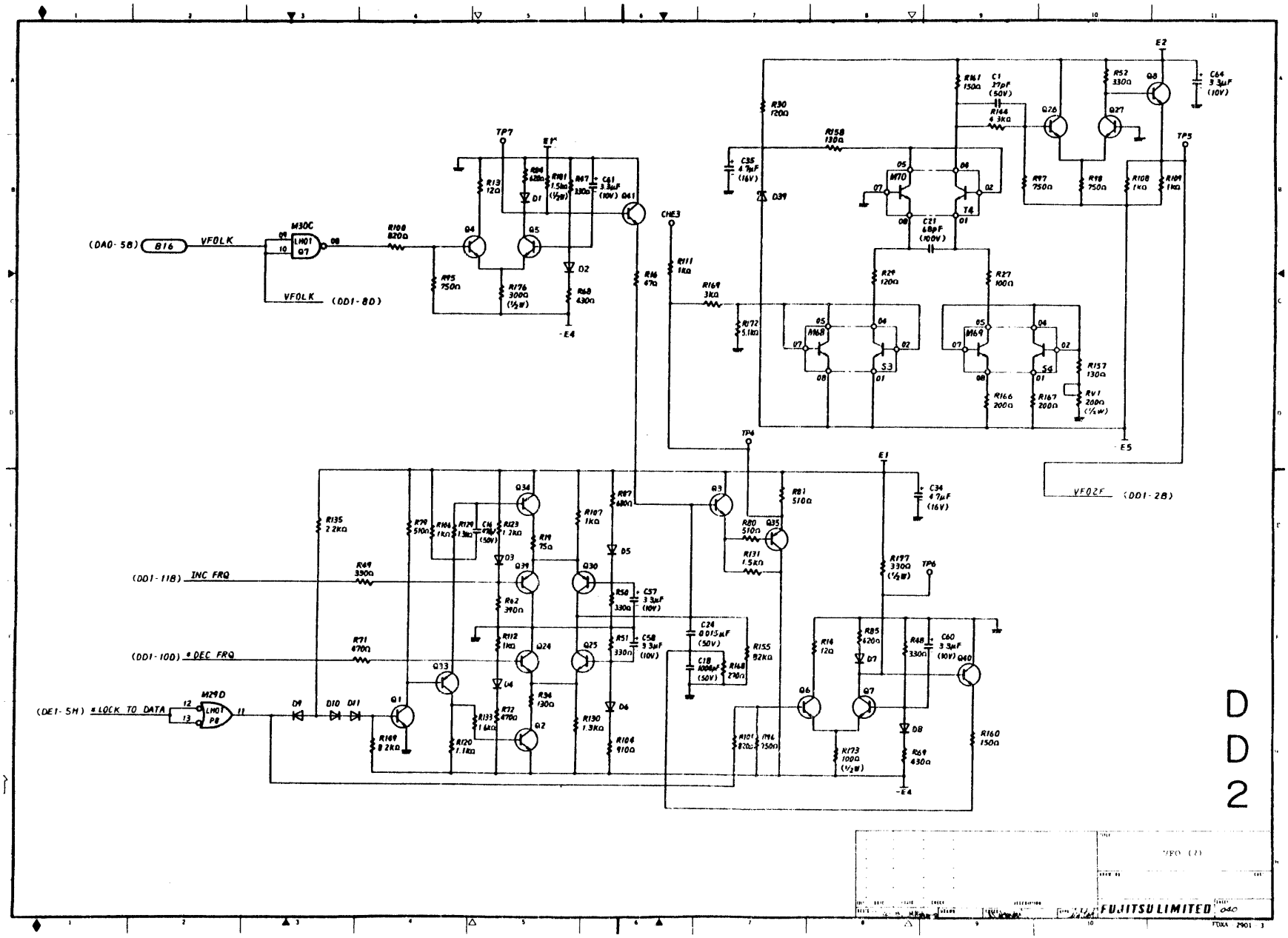

DBI
Write Compensation (1)
FUJITSU LIMITED
(DA0-5C) F04
VF02F
M24A
M23A
Q11
Q12
Q13
SW3
DL1
DL53
K6
SW03
J6
D19
D20
D21
M23B
M23C
M23D
M24B
M24C
M24D
TP14
TP15
TP16
2FEY
(DB2-9A)
(DB2-7B)
2F0T
(DB2-9B)
(DB2-7C)
2FLT
(XXX-9F)
(DB2-9C)
(DB2-7D)
VH2
M58B
M25D
M25C
WCL2
(DB2-2A)
1F
(XXX-7E)
(DB2-7B)
(DB2-7C)
(DB2-9D)
*1F
(XXX-9E)
(DB2-9A)
(DB2-9B)
(DB2-9C)
(DA0-5B) B27
(DA0-5B) A27
*WCL
M4C
M41D
M41C
M4D
M15B
M15A
WCLL
WCLH
WDTL
WDTH
B32
H11
B36
B35
M41B
M42C
M64A
WD
(DB2-1A)
*WD
(DB2-1A)
(XXX-11E)
*TTL
(XXX-10D)
TTL
(DA0-5B) B24
*TTL
M5A
TTL
(XXX-3E)
M5B
*TTL
(XXX-2E)
M41A
M4A
(DA0-5B) B26
(DA0-5B) A26
*WDT
(XXX-8B)
2FLT
M25A
WCL1
(DB2-1A)
(XXX-9B)
1F
(XXX-9C)
*1F
M64B
M57B
M42A
M42B
M42D
M13B
M11A
(DA0-5C) G22
WENB
WENB (DB2-9E)
C23
R146
4.3kΩ
+5V
-6V
FDXA 2901 3

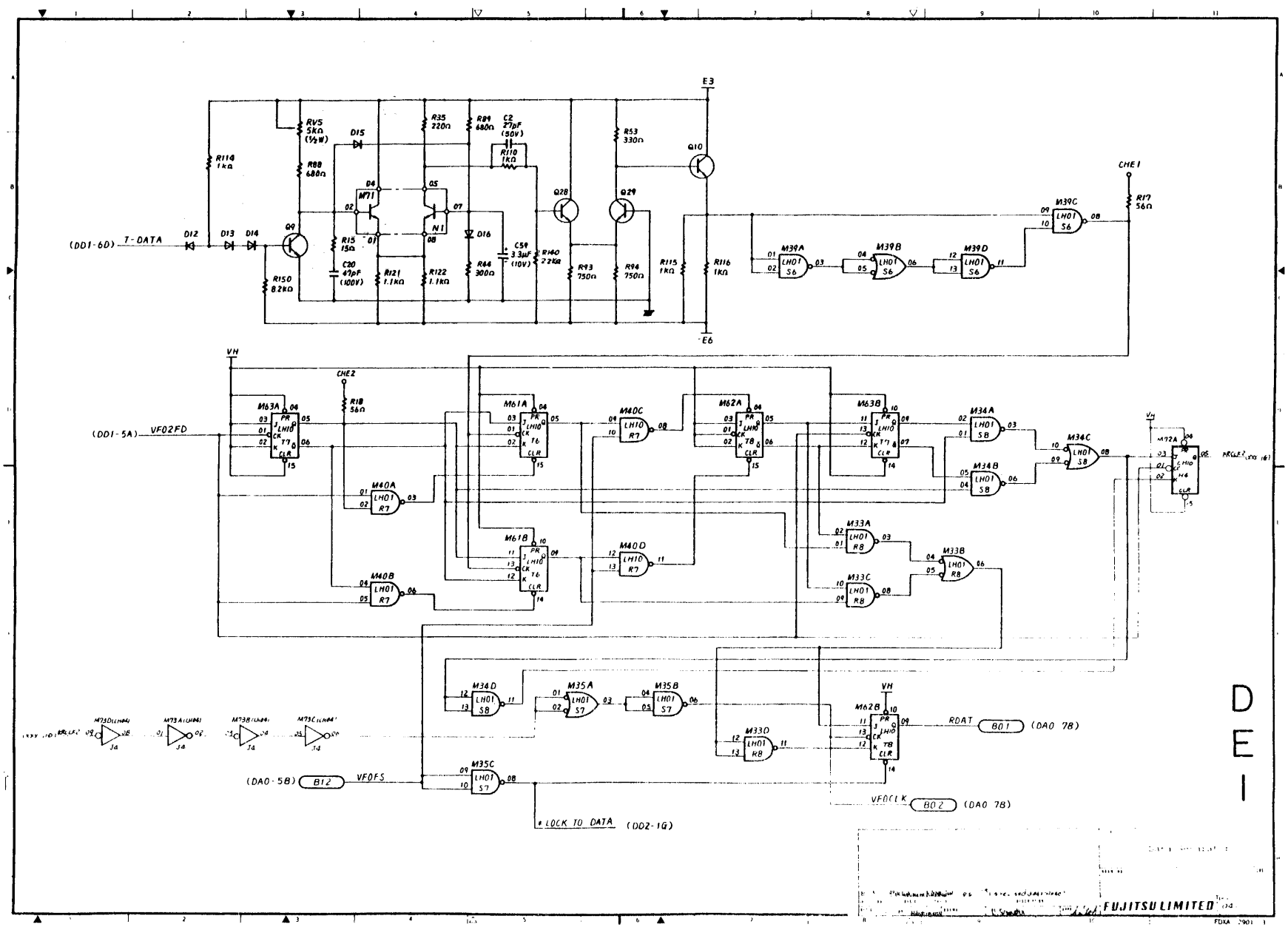

D
B
2
FUJITSU LIMITED

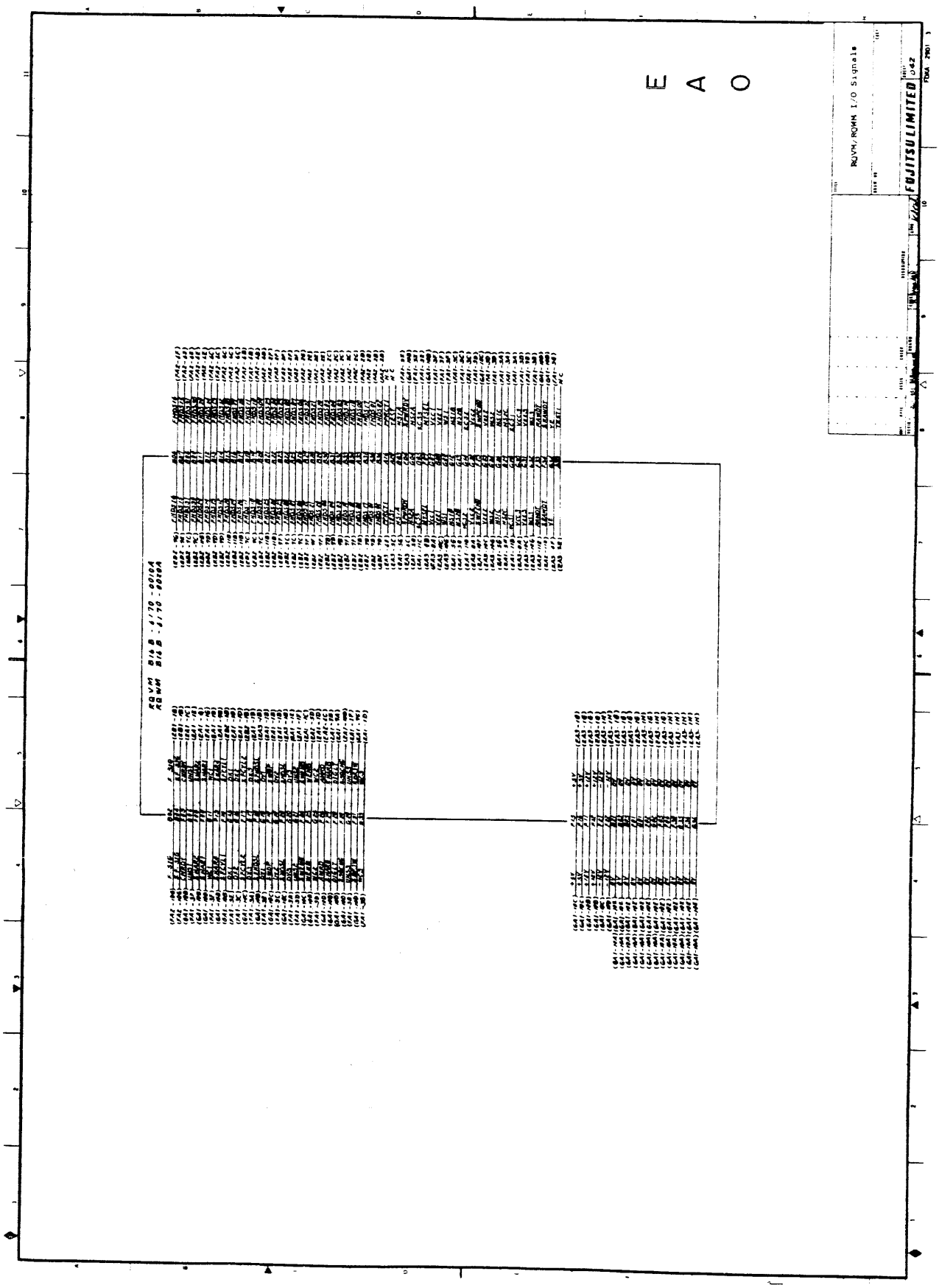

DC I
PLO II (1)
FUJITSU LIMITED
(DA0-5C) G09 2BCLK
M12A
M12B
M18A
M18B
M18C
M18D
M19A
M19B
M19C
M19D
M20A
M20B
M20C
M20D
M21A
M21B
M21C
M21D
M44A
M44B
M44C
M46A
M47A
M55A
M55B
M56A
M56B
M57A
M3A
M3B
M4F
PLOFSE (DC2-2C)
(DA0-5C) F18 PLOFS
(XXX 6E) ± 1/16 F
(XXX 7G) ± 1/16 FP
(DC2 9G) PLO1F
1/16 F NC
± 1/16 F (XXX 3D)
1/2 F NC
± 1/2 F (XXX 1G)
1/4 F (XXX 1H)
± 1/4 F (XXX 1G)
1/8 F (XXX 1G)
± 1/8 F (DA1-2C)
± 1/16 FP (XXX 7D)
(XXX 3F) ± 1/2 F
(XXX 4F) 1/4 F
(XXX 5F) 1/8 F
CLK1 F01 (DA0-7C)
± CLK2 F23 (DA0-7C)
± D FRQ (DC2 2C)
I FRQ (DC2 2B)
(DA0-5C) F19 PLOLK
C13 47pF (50V)
C14 270pF (50V)
C75 220pF (50V)
R153 3kΩ
R151 3.3kΩ
RV4 3kΩ (1/2W)
+5V
TP8
TP17
TP9

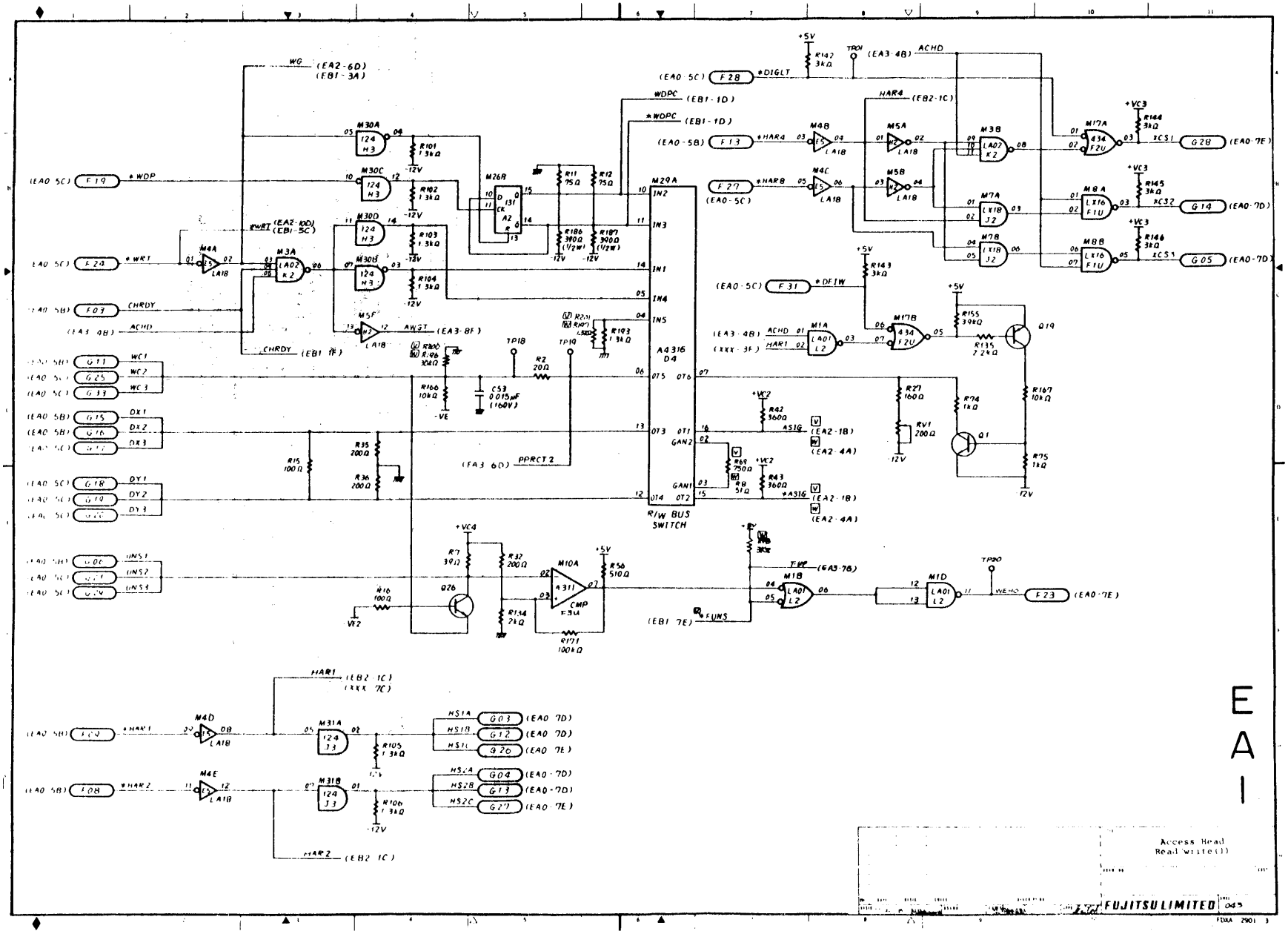

(DC1-11F) 1-FRQ
(DC1-11E) 10-FRQ
(DC1-4C) PLOFSE
PLO1F F32 (DA0-7C)
PLO1F (DB2 4B) (DC1-1E)
PLO II (2)
FUJITSU LIMITED
DC 2

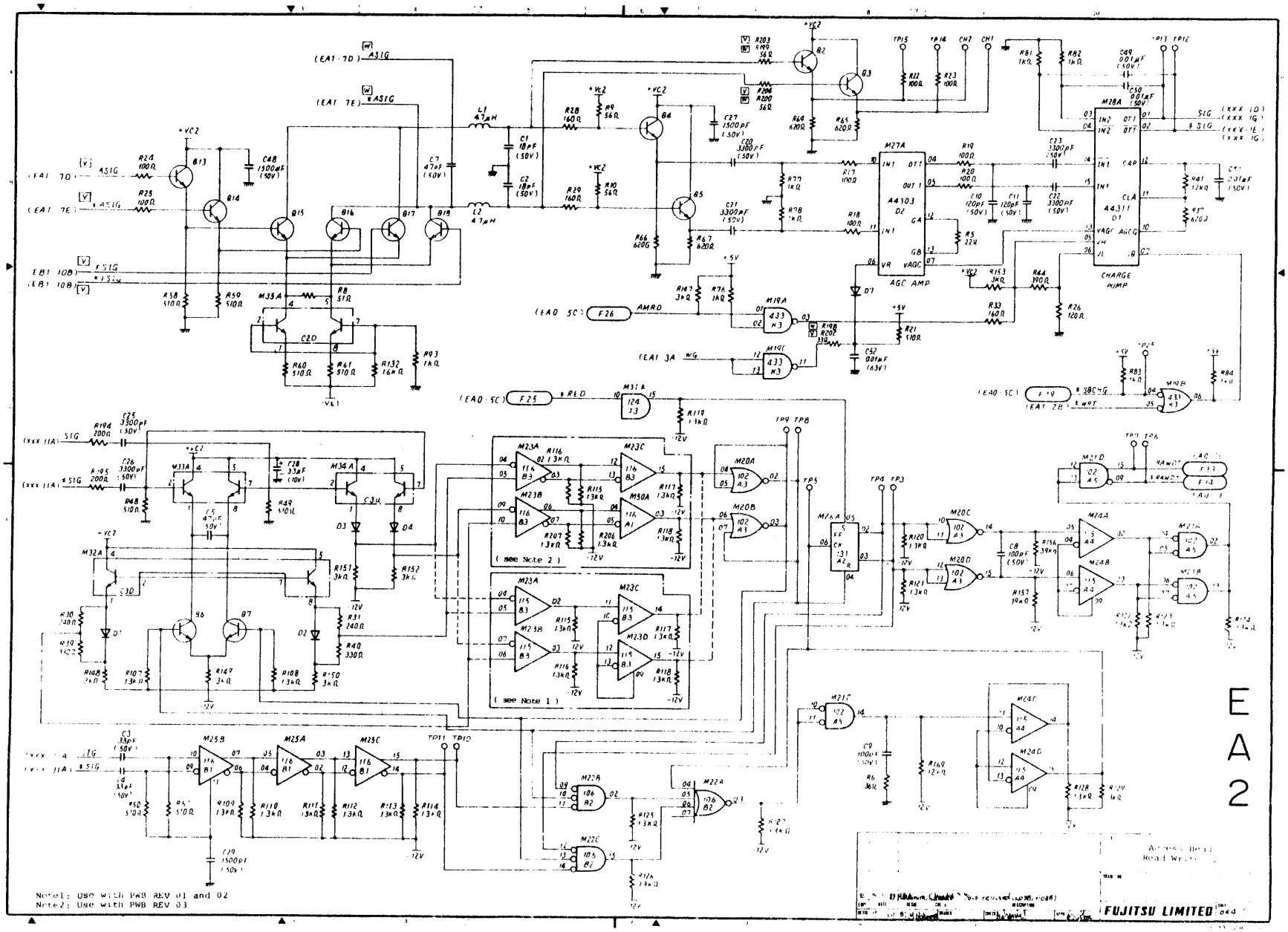

M32A
M32B
M32C
M32D
VF02F
B13
(DA0-7B)
VF02FD
(DE1-2D)
M37B
M37D
M37C
M37A
(DD2-10E) VF02F
M31A
M31B
TP2
M31C
M38A
M38B
M45A
M45B
INCFRQ
(DD2-2E)
(DA0-5B) B23 VF05Q
M36A
M36B
TP1
M31D
M38D
M38C
M45C
*DEC FRQ
(DD2-2F)
M27A
M27B
M27D
M36C
(DD2-3C) VF0LK
M30A
M30B
TP3
TDATA
(DD3-1B)
(DA0-5F) A05 +5V
(DA0-5F) B05,B15 A20 B20 B25,A30 0V
C27,C29 C37~C40 C63 C65 C66 33μF (10V)
M27~M40 M45
M61~M63
+5V
R54 330Ω
VH
L1 10μH
L2 10μH
L3 10μH
R1 5.1Ω
R2 5.1Ω
R3 5.1Ω
R4 5.1Ω
R5 5.1Ω
R6 5.1Ω
E1
E2
E3
C30 47μF (16V)
C28 47μF (16V)
C36 47μF (16V)
M27C
M28A
M28B
M28D
M28C
SW4
SN09J3
P7
C9 (50V)
C6 (50V)
C8 (50V)
M36D
M20A
M20B
M29C
D17
D18
Q44
R66 390Ω
R182 15Ω (1W)
(DA0-5F) A25 -12V
-12V
R136 1.2Ω
C67 (10V)
L4 10μH
L5 10μH
L6 10μH
R7 5.1Ω
R8 5.1Ω
R9 5.1Ω
R10 5.1Ω
R11 5.1Ω
R12 5.1Ω
C31 47μF (16V)
C32 47μF (16V)
C33 47μF (16V)
C34 1500pF (50V)
-E4
-E5
-E2
DD I
VFO (1)
FUJITSU LIMITED
FDXA 2901-3

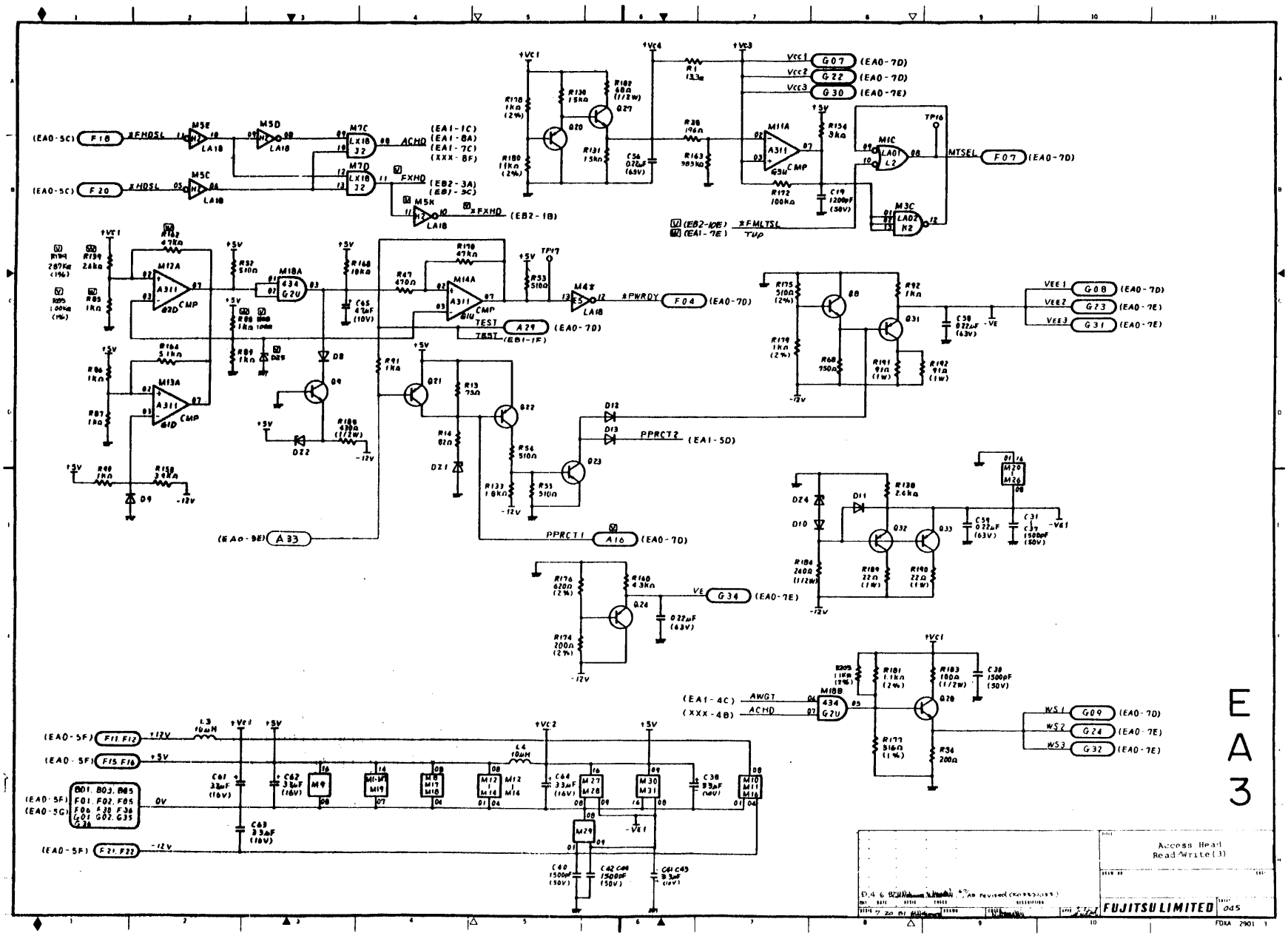

(DA0-5B) B16 VFOLK
VFOLK (DD1-8D)
(DD1-11B) INC FRQ
(DD1-10D) ¥DEC FRQ
(DE1-5H) ¥LOCK TO DATA
VFO2F (DD1-2B)
TP7
TP4
TP5
TP6
E1
E2
E4
E5
CHE3
M30C
M29D
M70
M168
M169
Q1
Q2
Q4
Q5
Q6
Q7
Q24
Q25
Q30
Q33
Q34
Q35
Q39
Q40
Q41
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D39
R30 120Ω
R158 130Ω
R161 150Ω
R144 4.3kΩ
R52 330Ω
R97 750Ω
R98 750Ω
R108 1kΩ
R109 1kΩ
R29 120Ω
R27 100Ω
R157 130Ω
R166 200Ω
R167 200Ω
RV1 200Ω (¼W)
R111 1kΩ
R169 3kΩ
R172 5.1kΩ
R16 47Ω
R95 750Ω
R176 300Ω (½W)
R68 430Ω
R81 510Ω
R131 1.5kΩ
R197 330Ω (½W)
R135 2.2kΩ
R49 330Ω
R71 470Ω
R169 8.2kΩ
R120 7.1kΩ
R133 1.6kΩ
R72 470Ω
R34 130Ω
R130 1.3kΩ
R104 910Ω
R155 82kΩ
R168 270Ω
R16 12Ω
R85 620Ω
R48 330Ω
R101 820Ω
R196 750Ω
R173 100Ω (½W)
R69 430Ω
R160 150Ω
C35 4.7μF (16V)
C21 68pF (100V)
C64 3.3μF (10V)
C34 4.7μF (16V)
C24 0.015μF (50V)
C18 1000pF (50V)
C60 3.3μF (10V)
C57 3.3μF (10V)
C58 3.3μF (10V)
D
D
2
FUJITSU LIMITED

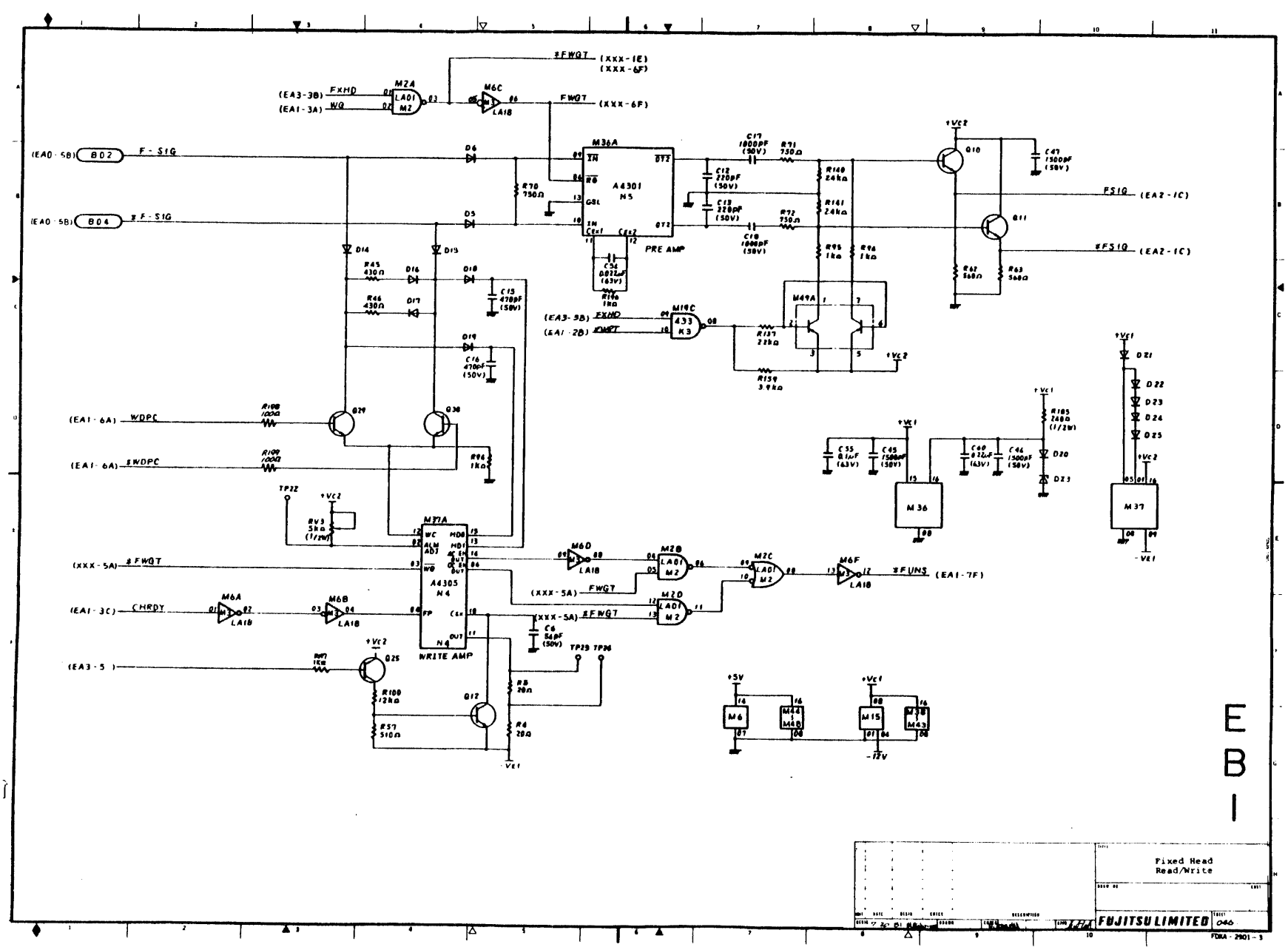

E3
E6
RV5 5kΩ (½W)
R114 1kΩ
R88 680Ω
D15
R35 220Ω
R89 680Ω
C2 27pF (50V)
R110 1kΩ
R53 330Ω
Q10
Q28
Q29
CHE1
R17 56Ω
(DD1-6D) T-DATA
D12
D13
D14
Q9
R15 15Ω
C20 47pF (100V)
R121 1.1kΩ
R122 1.1kΩ
R150 8.2kΩ
D16
C59 3.3μF (10V)
R140 22kΩ
R44 300Ω
R93 750Ω
R94 750Ω
R115 1kΩ
R116 1kΩ
M39A
M39B
M39C
M39D
VH
CHE2
R18 56Ω
(DD1-5A) VF02FD
M63A
M61A
M40C
M62A
M63B
M34A
M34B
M34C
M40A
M40B
M61B
M40D
M33A
M33B
M33C
M34D
M35A
M35B
M33D
M62B
RDAT
B01
(DA0 7B)
(DA0-5B)
B12
VF0FS
M35C
VF0CLK
B02
(DA0 7B)
* LOCK TO DATA
(DD2-1G)
FUJITSU LIMITED
D
E
I

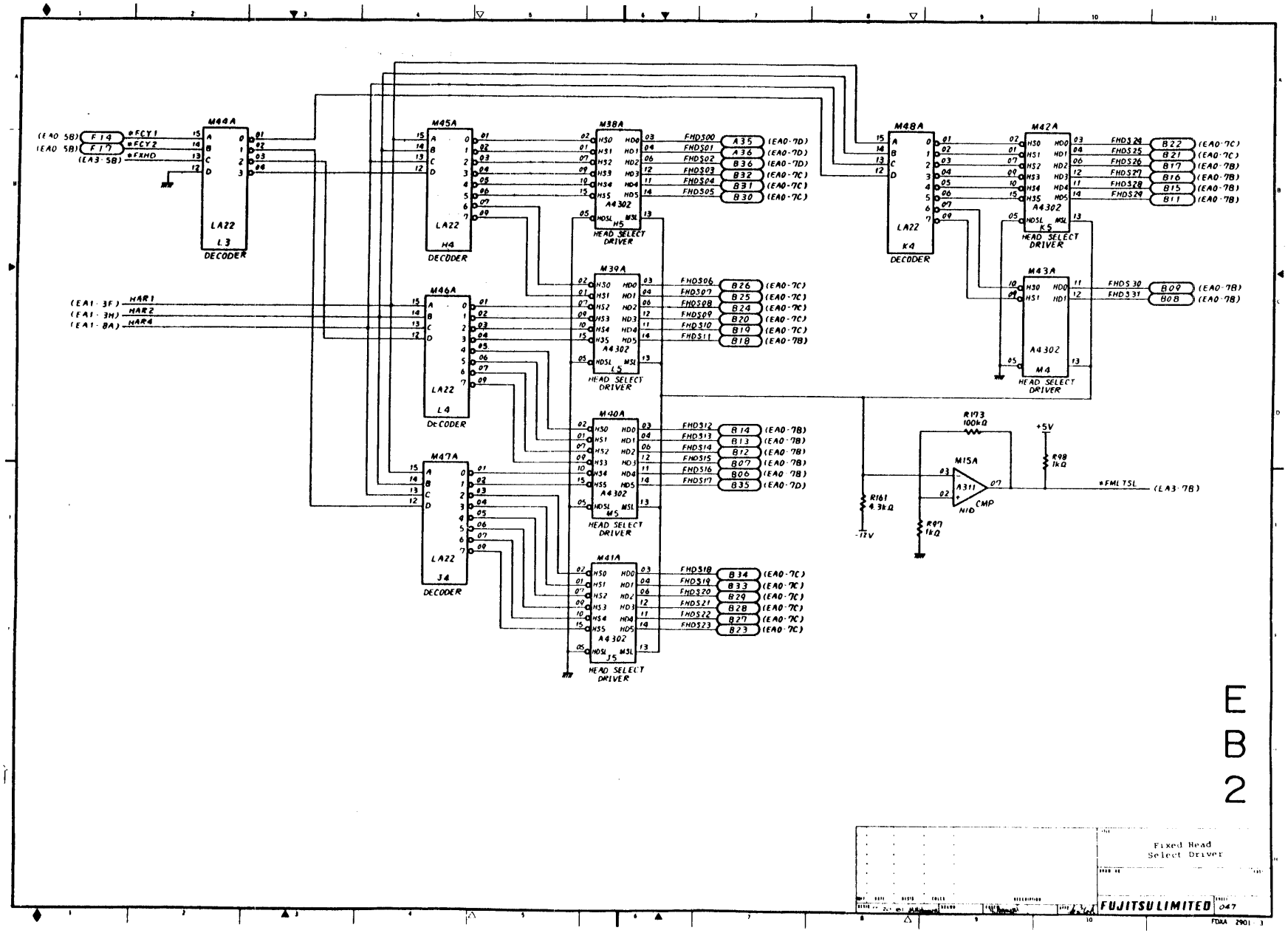

E A O
ROVM, ROMM I/O Signals
FUJITSU LIMITED

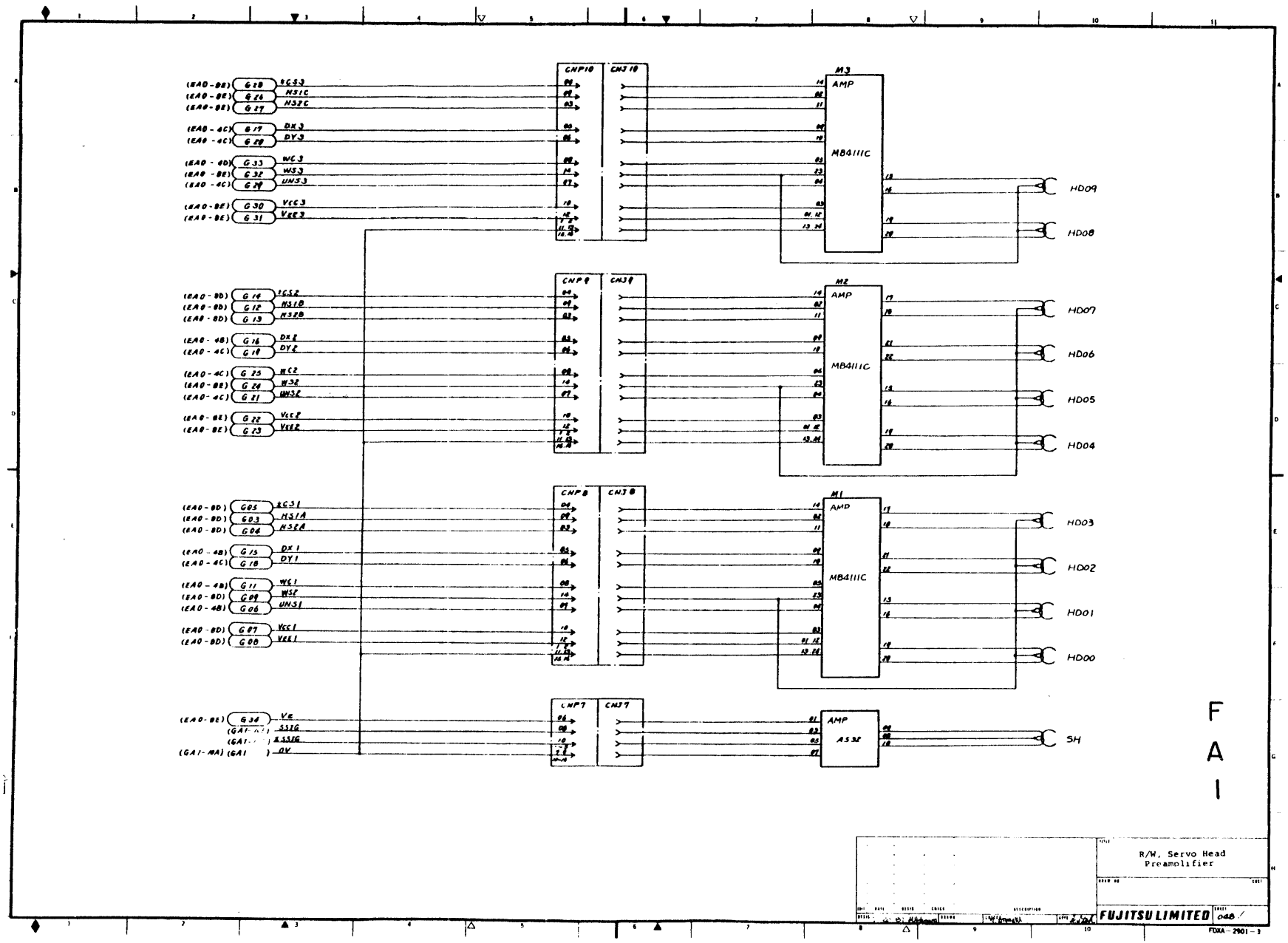

WG (EA2-6D) (EB1-3A)
WDPC (EB1-1D)
*WDPC (EB1-1D)
HAR4 (EB2-1C)
ACHD
*DIGLT
*HAR4
*HARB
*DFIW
*WRT (EA2-10D) (EB1-5C)
*WRT
CHRDY
CHRDY (EB1-1F)
AW3T (EA3-8F)
PPRCT2 (EA3-6D)
R/W BUS SWITCH
A4316 D4
CMP F34
HAR1 (EB2-1C) (XXX-7C)
HAR2 (EB2-1C)
*FUNS (EB1-7E)
FUJITSU LIMITED
Access Read Read/Write(1)
E A I


E A 2
FUJITSU LIMITED
Note1: Use with PWB REV 01 and 02
Note2: Use with PWB REV 03
(see Note 1)
(see Note 2)
AGC AMP
CHARGE PUMP
AMRO
WG
+VC2
+5V
-12V
-VE

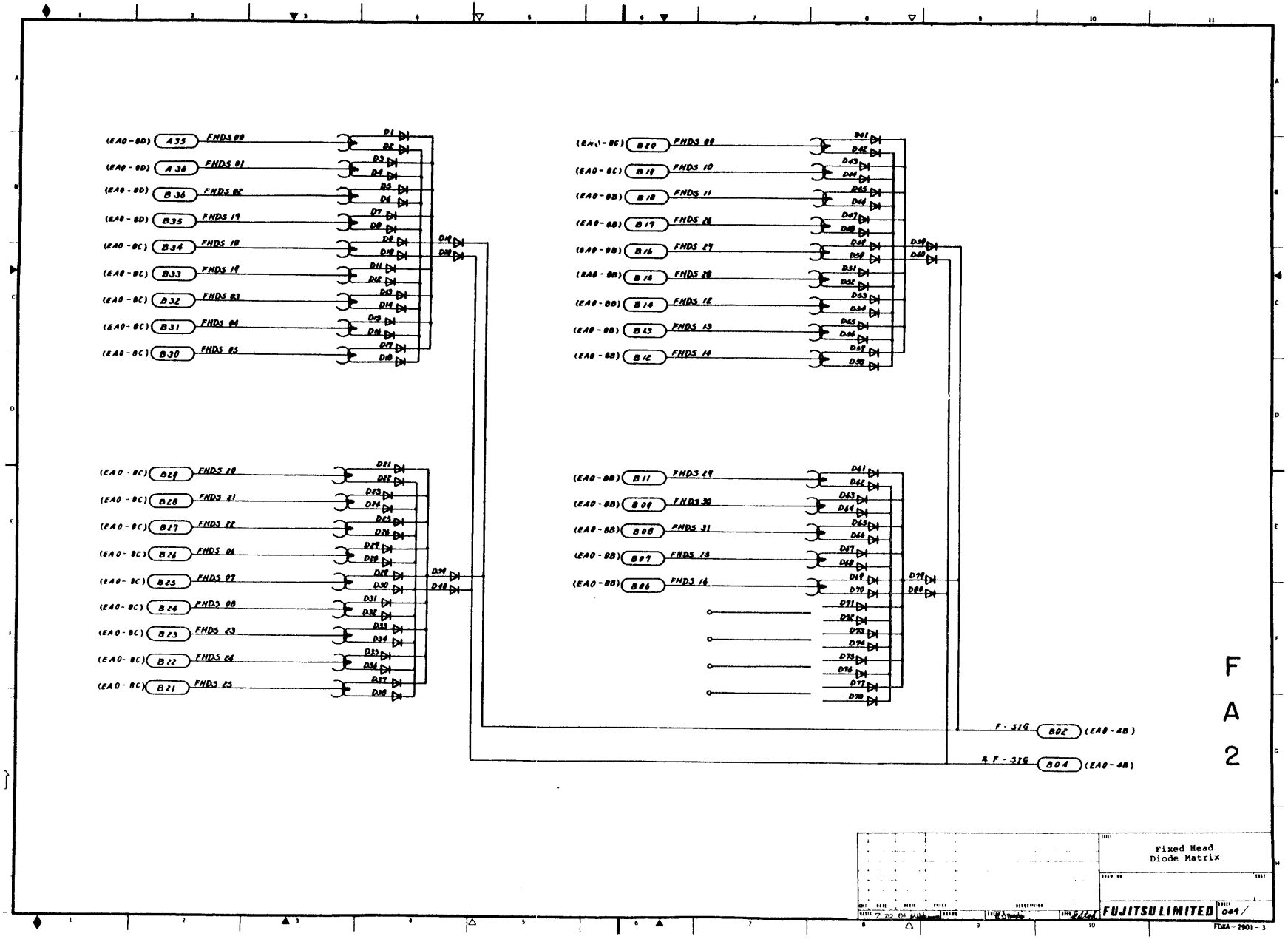

E A 3
Access Head Read/Write(3)
FUJITSU LIMITED
045
FDXA 2901 3

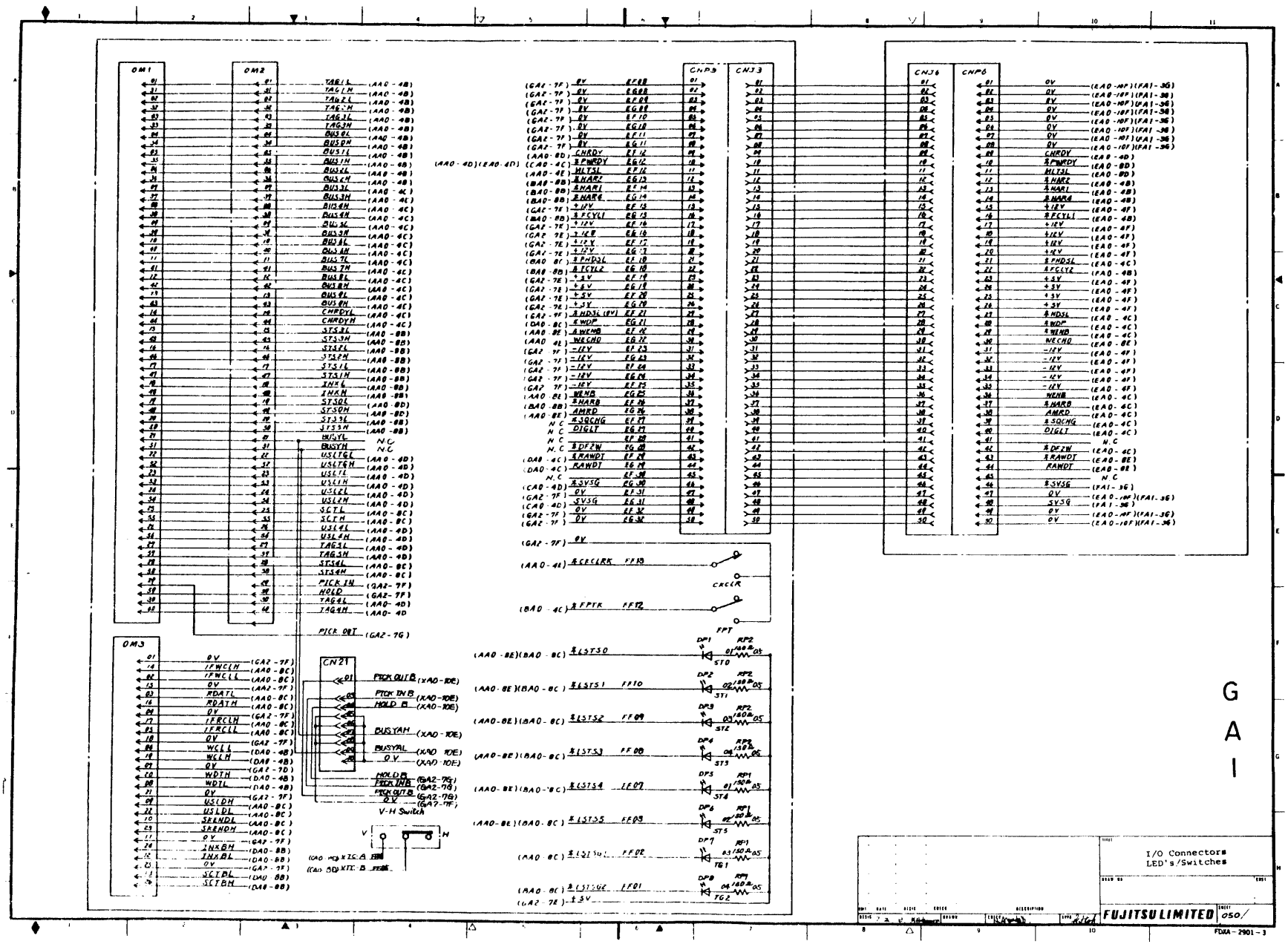

#FWGT (XXX-1E)
(XXX-6F)
(EA3-3B) FXHD
(EA1-3A) WG
M2A
LA01
M2
M6C
LA18
FWGT (XXX-6F)
(EA0-5B) B02 F-SIG
(EA0-5B) B04 #F-SIG
M36A
A4301
M5
PRE AMP
+Vc2
Q10
Q11
FSIG (EA2-1C)
#FSIG (EA2-1C)
(EA3-9B) FXHD
(EA1-2B) #WGT
M19C
433
M3
M49A
+Vc1
DZ1
DZ2
DZ3
DZ4
DZ5
M36
M37
(EA1-6A) WDPC
(EA1-6A) #WDPC
Q29
Q30
TP22
RV3 5kΩ (1/2W)
M37A
A4305
M4
WRITE AMP
(XXX-5A) #FWGT
(EA1-3C) CHRDY
M6A
M6B
M6D
M6E
M6F
M2B
M2C
M2D
#FUNS (EA1-7F)
(XXX-5A) FWGT
(XXX-5A) #FWGT
C6 56pF (50V)
TP29 TP26
(EA3-5)
Q25
Q12
R100 12kΩ
R57 510Ω
R5 20Ω
R6 20Ω
-Vc1
+5V
-12V
M6
M44
M45
M15
M38
M43
E
B
I
Fixed Head
Read/Write
FUJITSU LIMITED
FDKA-2901-3

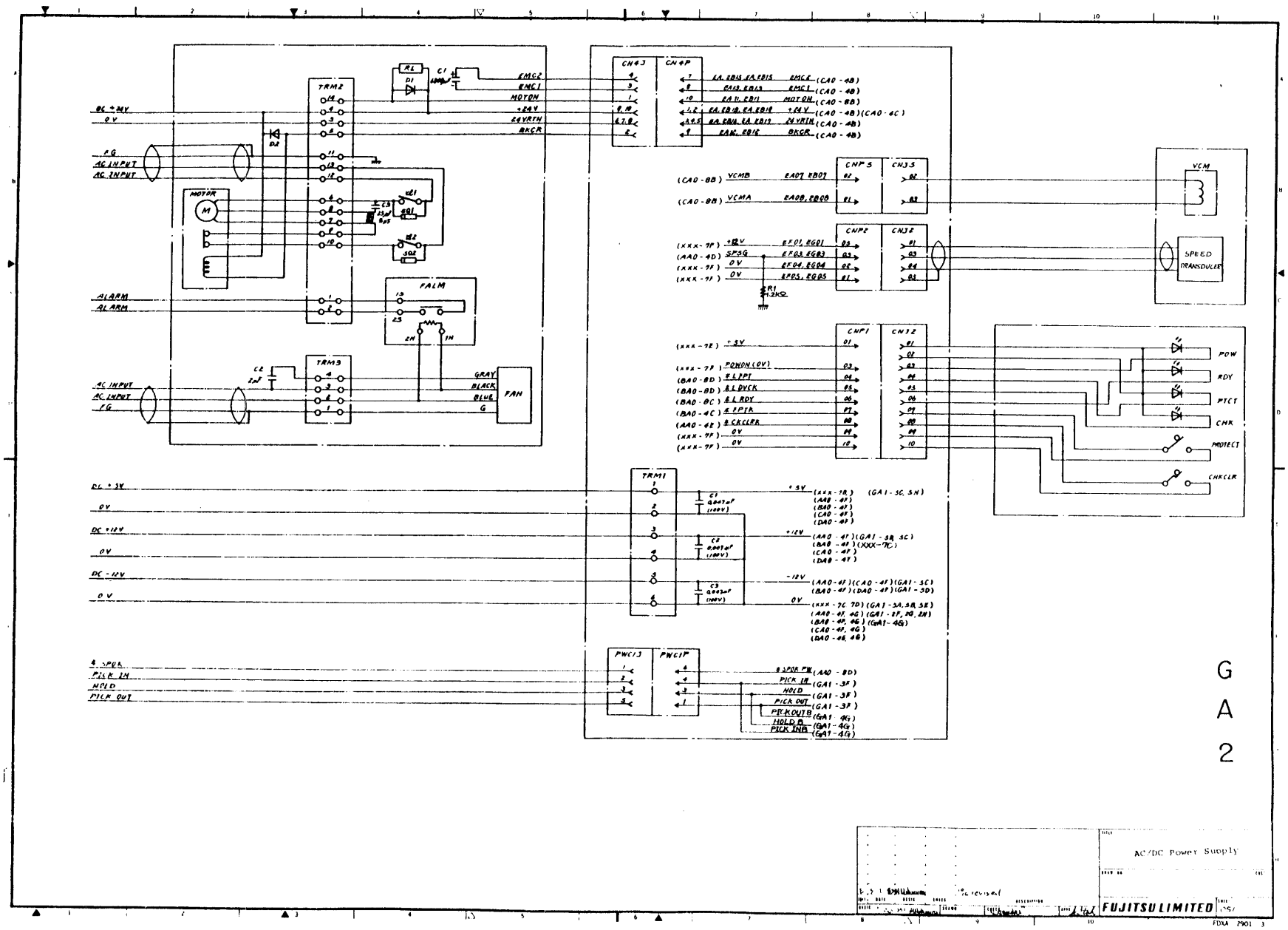

M44A
LA22
L3
DECODER
M45A
LA22
H4
DECODER
M46A
LA22
L4
DECODER
M47A
LA22
J4
DECODER
M38A
M39A
M40A
M41A
A4302
HEAD SELECT DRIVER
M48A
LA22
K4
DECODER
M42A
M43A
M15A
A311
CMP
R173 100kΩ
R161 4.3kΩ
R98 1kΩ
R97 1kΩ
+5V
-12V
*FMLTSL (EA3·7B)
E
B
2
Fixed Head Select Driver
FUJITSU LIMITED

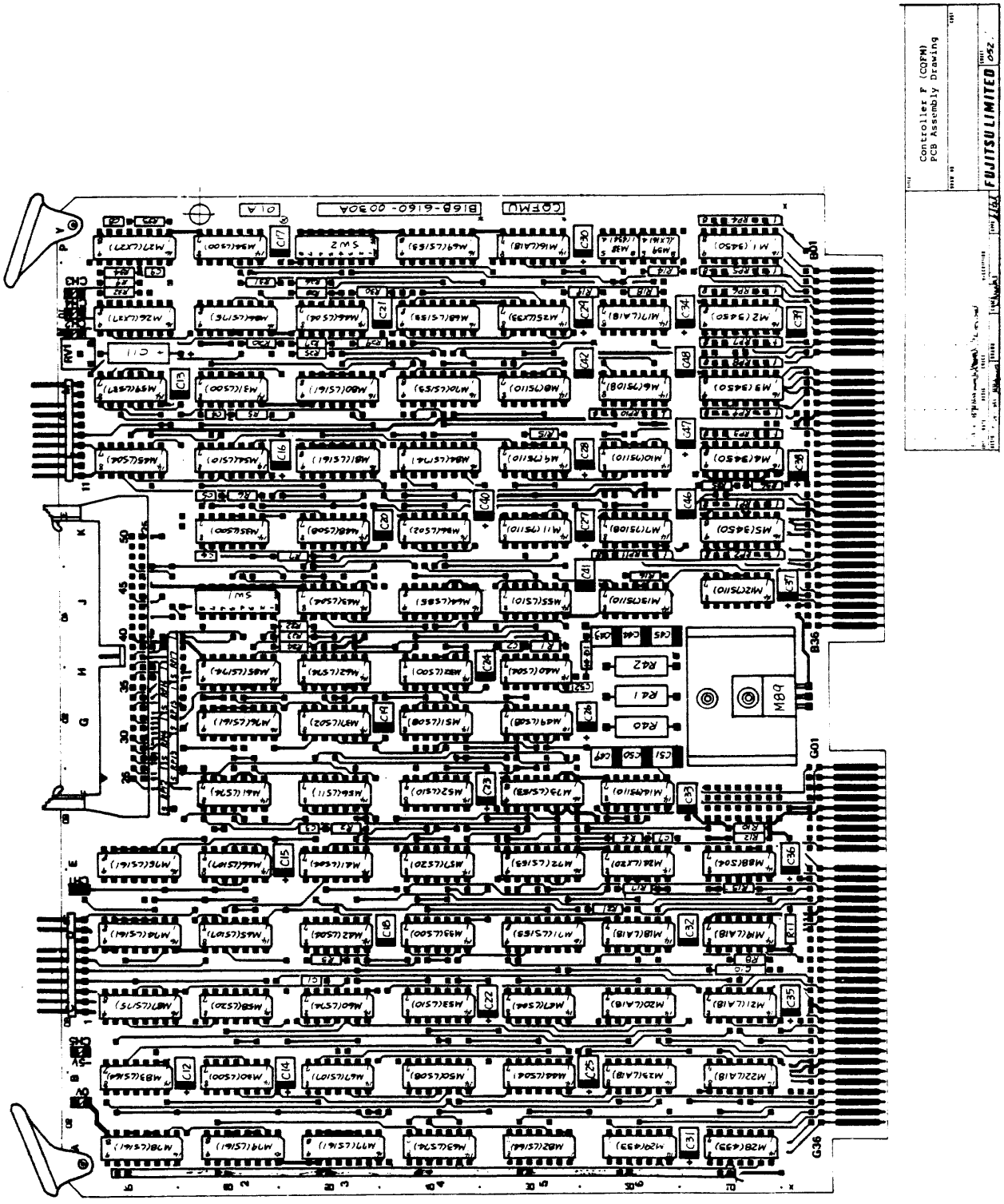

CNP10
CNJ10
M3
AMP
MB4111C
HD09
HD08
CNP9
CNJ9
M2
AMP
MB4111C
HD07
HD06
HD05
HD04
CNP8
CNJ8
M1
AMP
MB4111C
HD03
HD02
HD01
HD00
CNP7
CNJ7
AMP
AS32
SH
R/W, Servo Head
Preamplifier
FUJITSU LIMITED
FDXA-2901-3

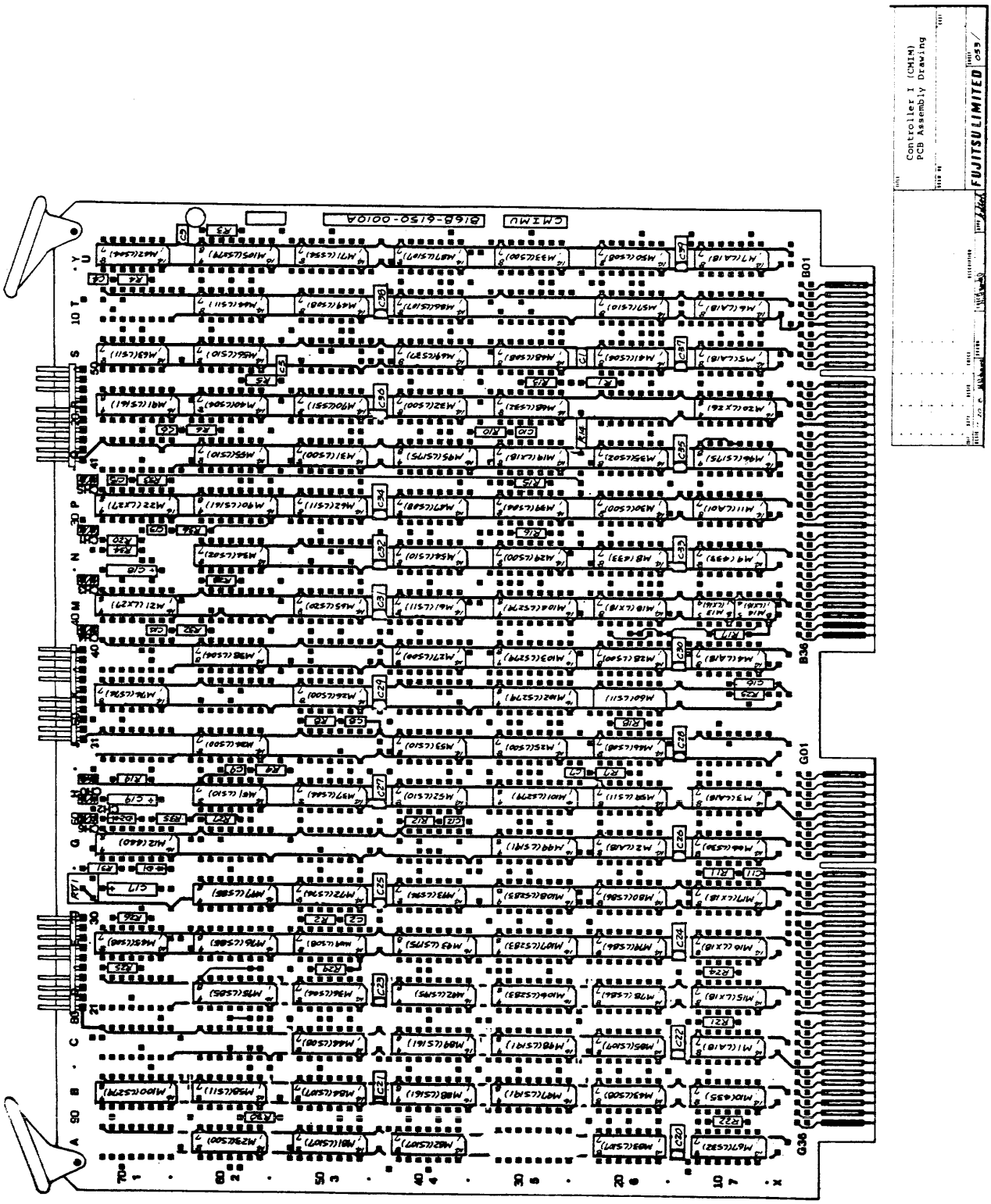
F
A
1

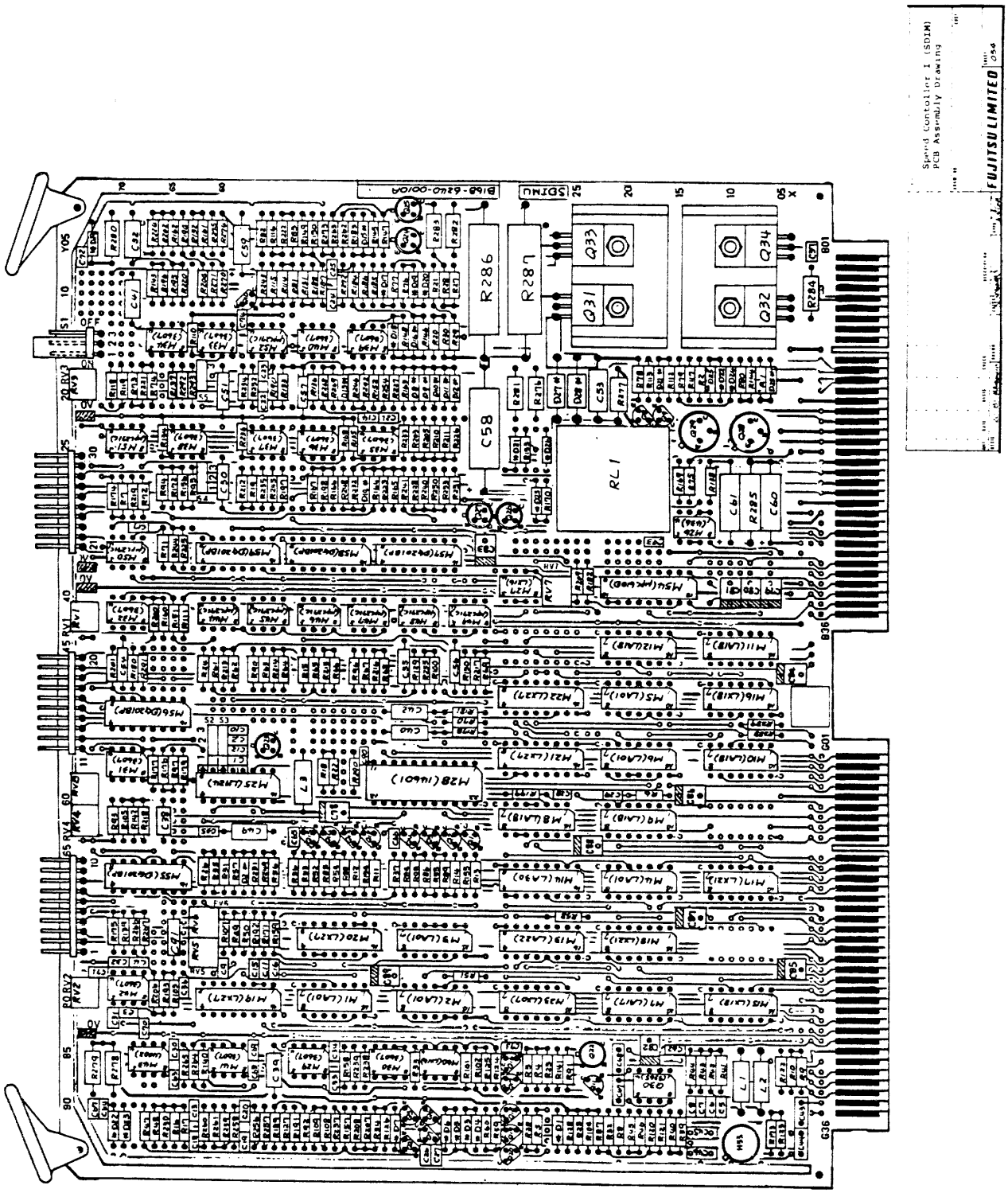

F A 2
F - SIG B02 (EA0 - 4B)
4 F - SIG B04 (EA0 - 4B)
Fixed Head
Diode Matrix
FUJITSU LIMITED
FDKA - 2901 - 3

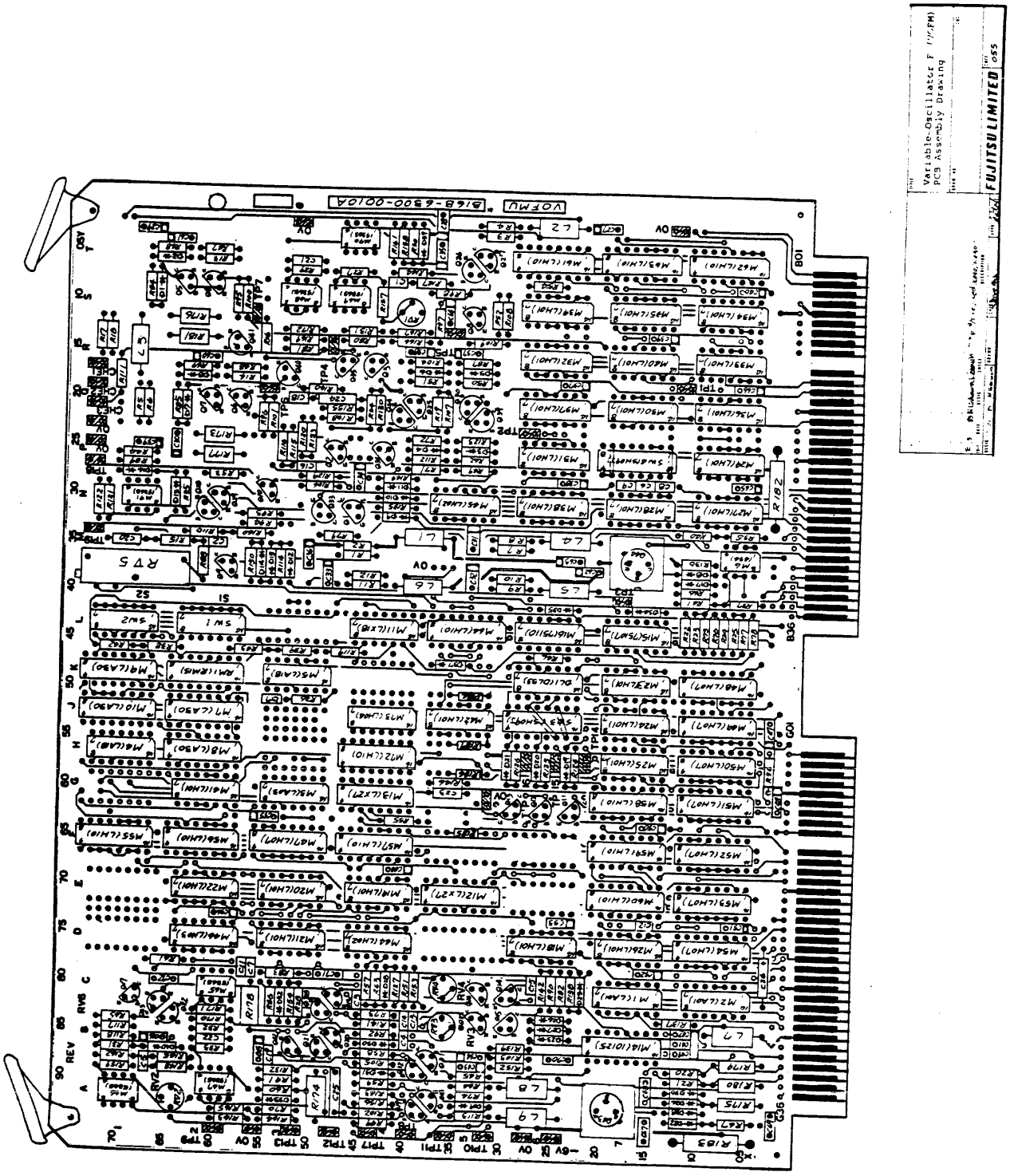

I/O Connectors
LED's/Switches
FUJITSU LIMITED
050/
FDXA-2901-3
G
A
I


AC/DC Power Supply
FUJITSU LIMITED
G A 2
TRM2
TRM3
TRM1
CN4J
CN4P
CNP5
CNJ5
CNP2
CNJ2
CNP1
CNJ1
PWC1J
PWC1P
MOTOR
FALM
FAN
VCM
SPEED TRANSDUCER
PDW
RDY
PTCT
CHK
PROTECT
CHKCLR
EMC2
EMC1
MOTON
+24V
24VRTN
BKCR
ALARM
AC INPUT
FG
GRAY
BLACK
BLUE
G
+5V
+12V
-12V
0V
PICK IN
HOLD
PICK OUT

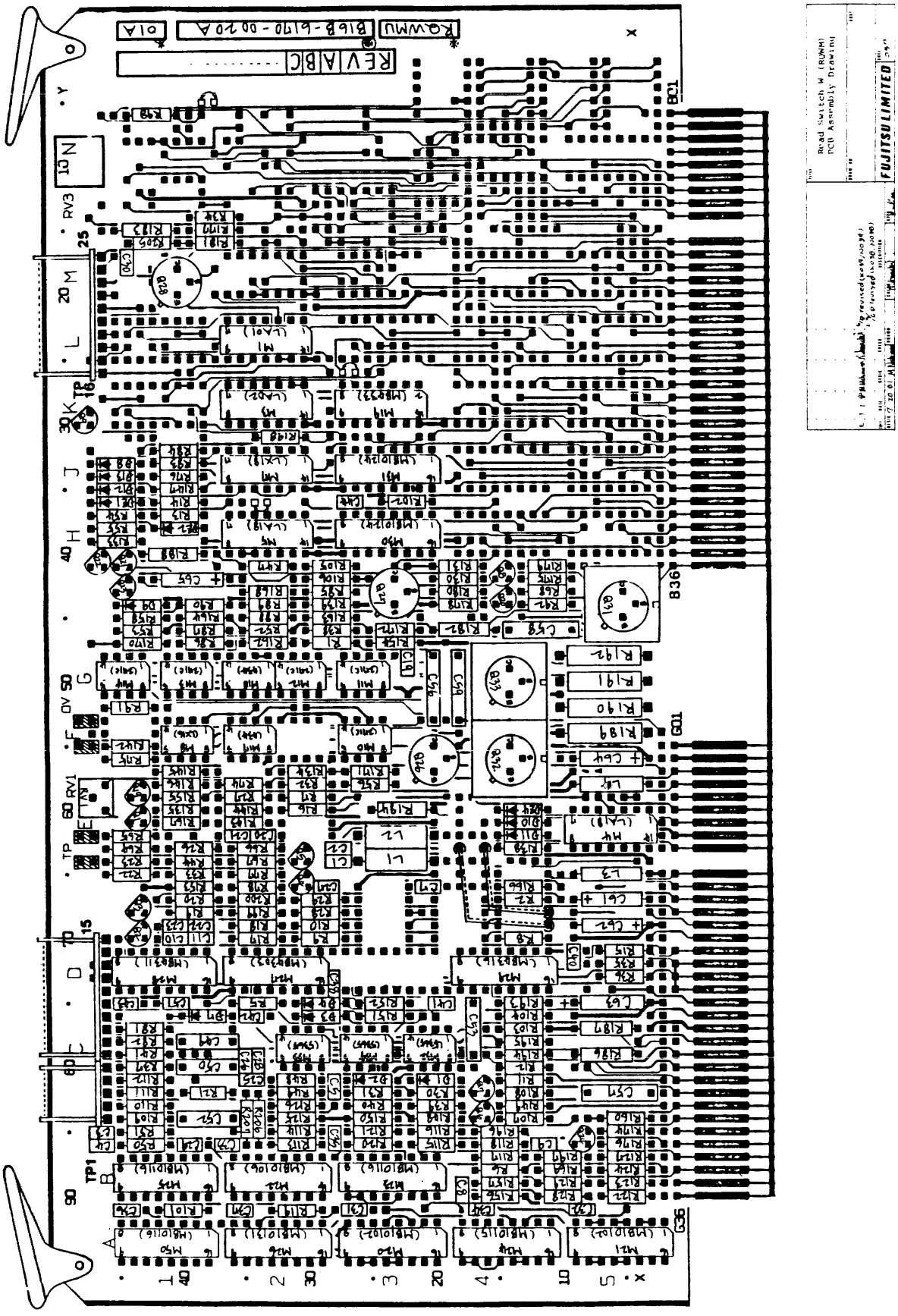

Controller F (CQFM)
PCB Assembly Drawing
FUJITSU LIMITED
B16B-6160-0030A
CQFMU

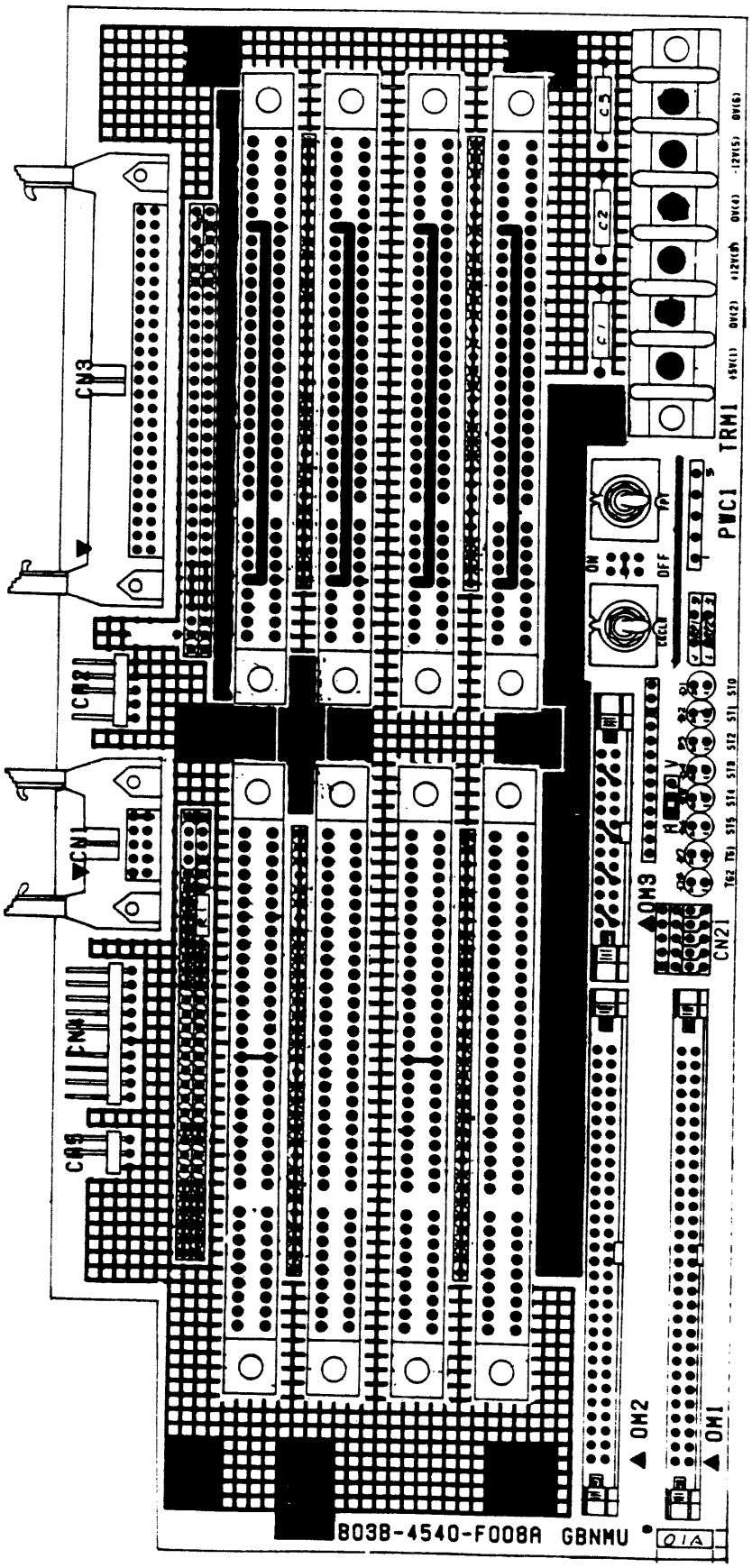

Controller I (CMIM)
PCB Assembly Drawing
FUJITSU LIMITED
B16B-6150-0010A
CMIMU
B01
B36
G01
G36

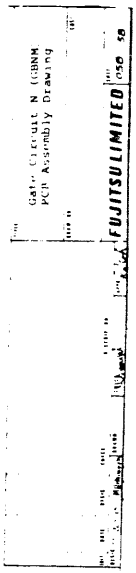

Speed Controller I (SDIM)
PCB Assembly Drawing
FUJITSU LIMITED
SDIMC
R286
R287
C58
RL1
Q31
Q32
Q33
Q34
R285
C60
C61


Variable-Oscillator F (VSPM)
PCB Assembly Drawing
FUJITSU LIMITED
B16B-6300-0010A
VOFMU

TP1
TP
RV1
RV3
REV|A|B|C
RQVMU B168-6170-00110A
01A
G36
G01
B36
B01
FUJITSU LIMITED




CN3
CN2
CN1
CN4
CN5
C3
C2
C1
TRM1
PWC1
ON
OFF
CN21
OM3
OM2
OM1
B03B-4540-F008A GBNMU
01A


FUJITSU LIMITED

PART 2
Dual Port Schematics

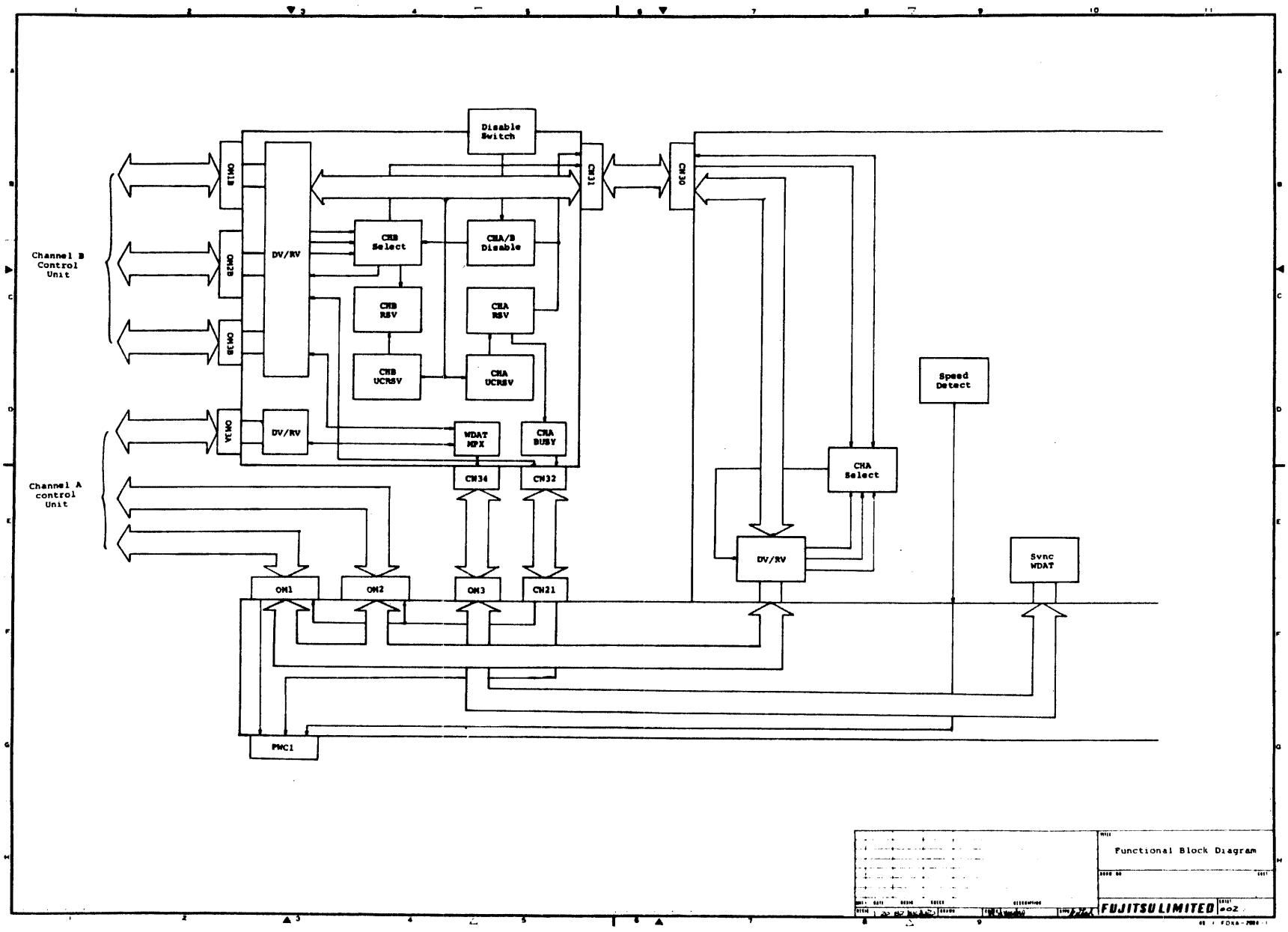
SHEET	ABBR	TITLE
001		Schematics/Drawings List
002		Functional Block Diagram
003	XA0	Interface Connection Connectionwith CQFM PCB
004	XA1	A/B-Cable Receivers
005	XA2	A/B-Cable Drivers CHA B-Cable Drivers
006	XB1	Unit Selection
007	XC1	Select/Reserve (1)
008	XC2	Select/Reserve (2)
009	XC3	Select/Reserve (3)
010	XC4	Select/Reserve (4)
011		XCBM PCB Assembly

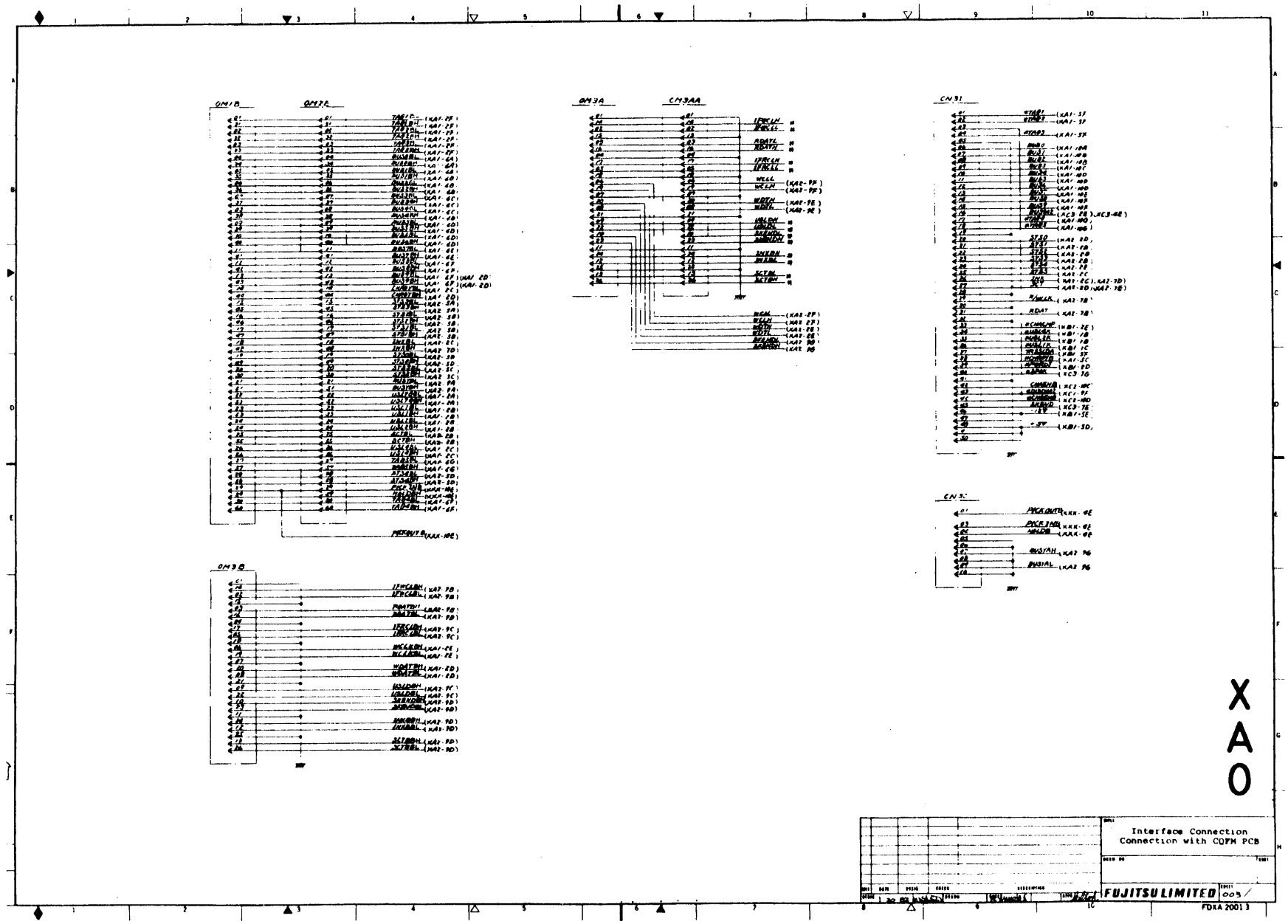
SHEET	ABBR	TITLE

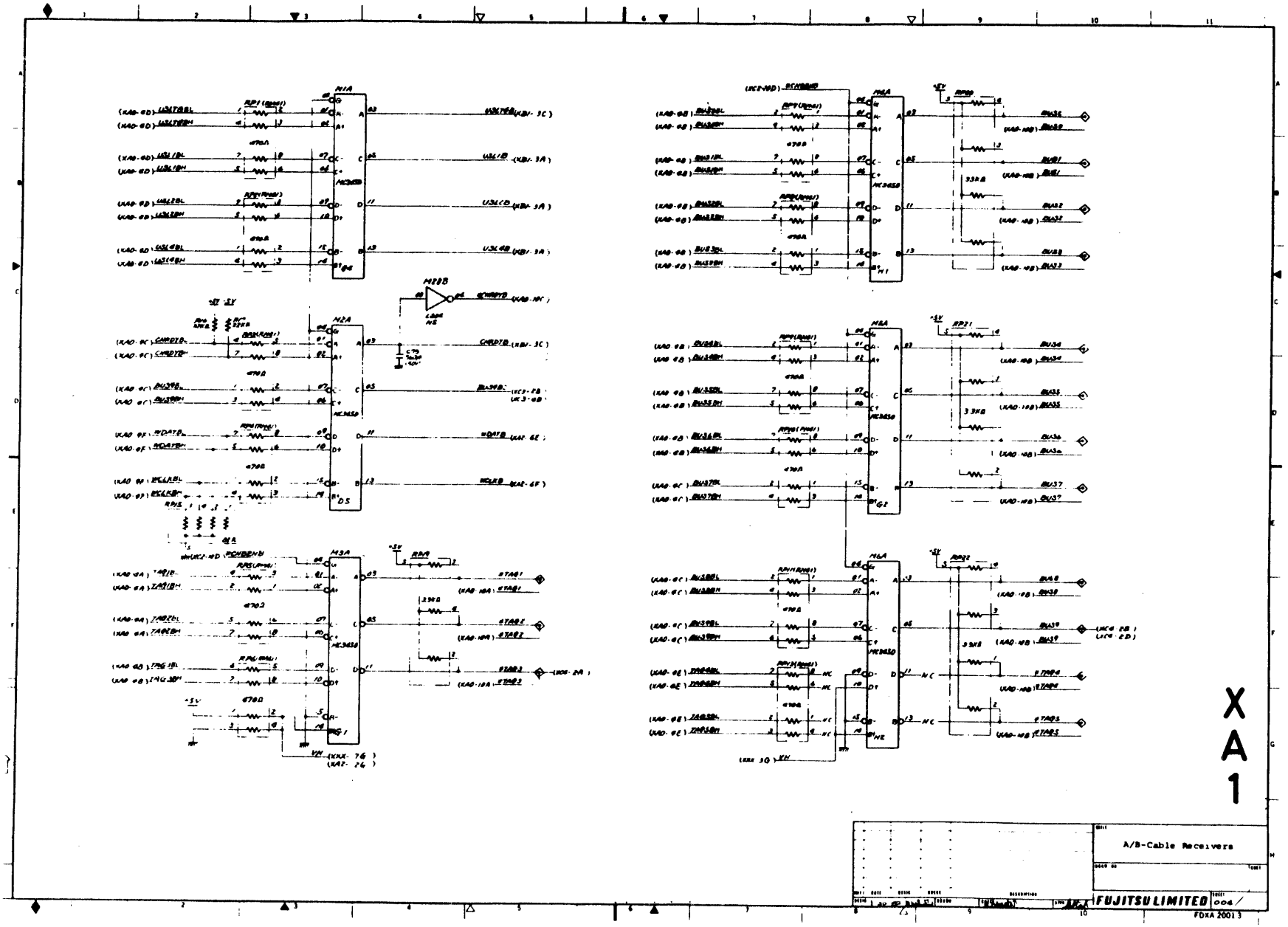
SHEET	ABBR	TITLE

Schematics/Drawings List

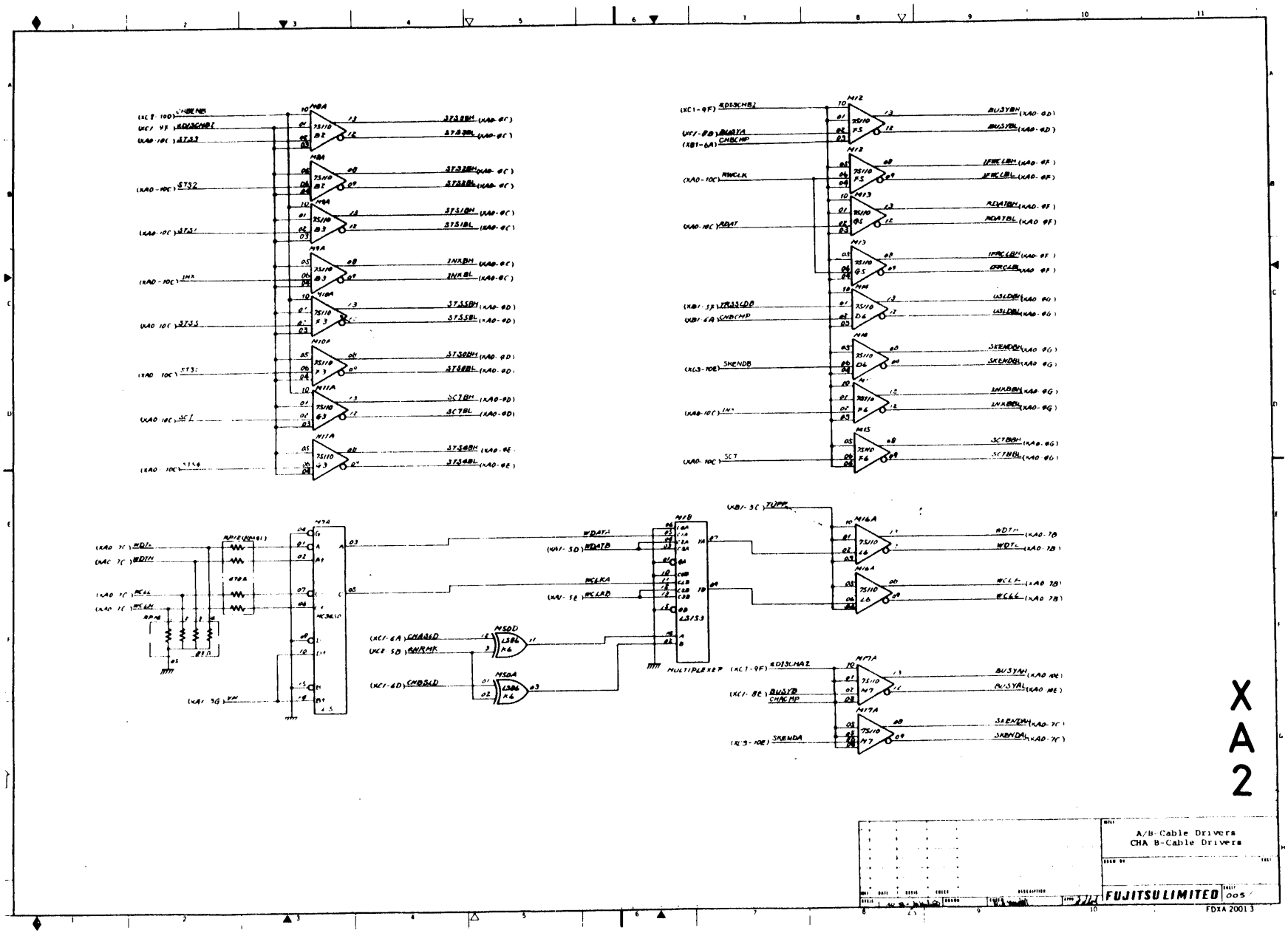
FUJITSU LIMITED

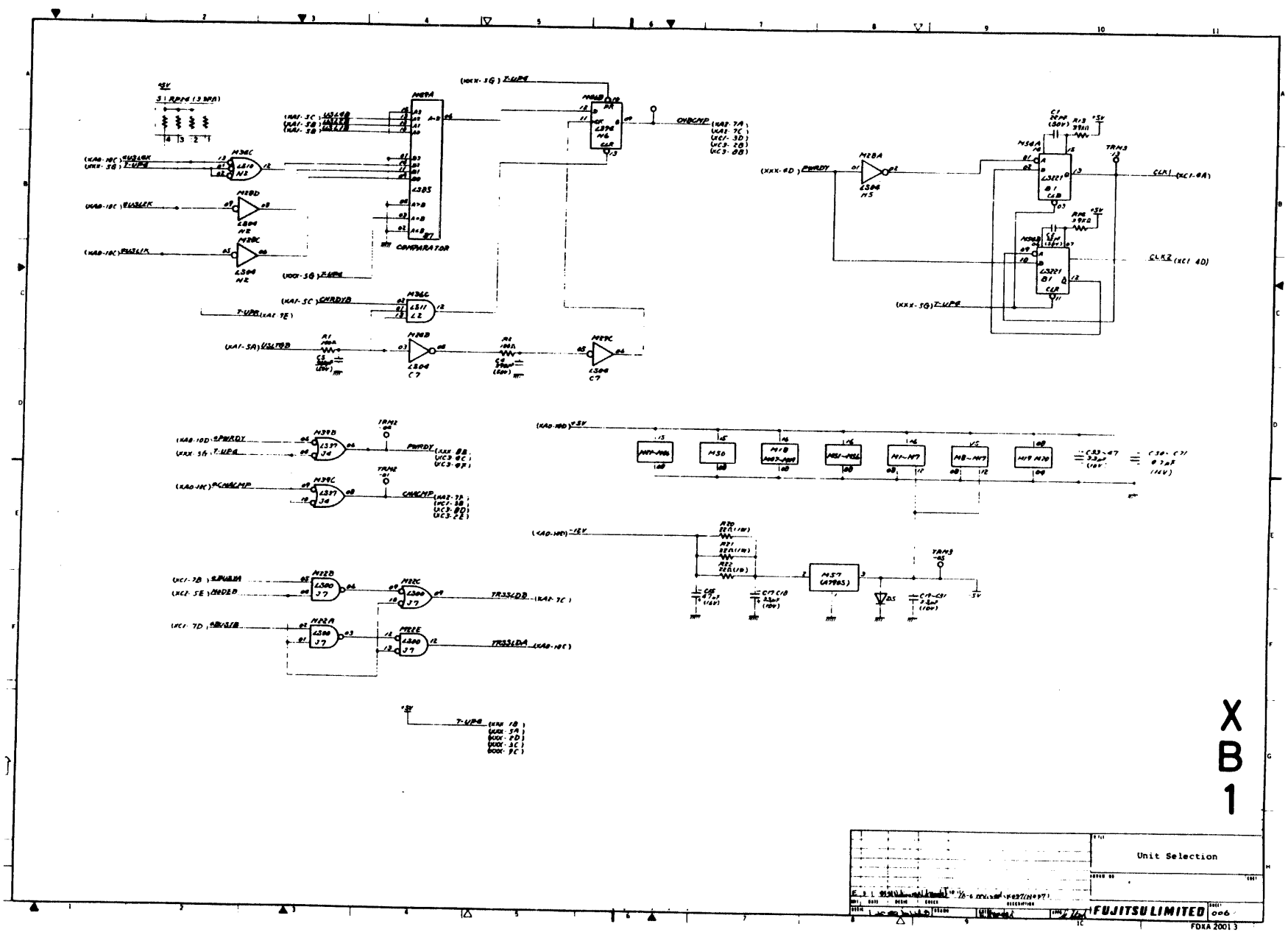

Disable Switch
CN18
CN28
CN38
CN1A
CN31
CN30
DV/RV
CHB Select
CHA/B Disable
CHB RSV
CHA RSV
CHB UCRSV
CHA UCRSV
Channel B Control Unit
Channel A control Unit
DV/RV
WDAT MPX
CHA BUSY
CN34
CN32
Speed Detect
CHA Select
DV/RV
Sync WDAT
CN1
CN2
CN3
CN21
PWC1
Functional Block Diagram
FUJITSU LIMITED

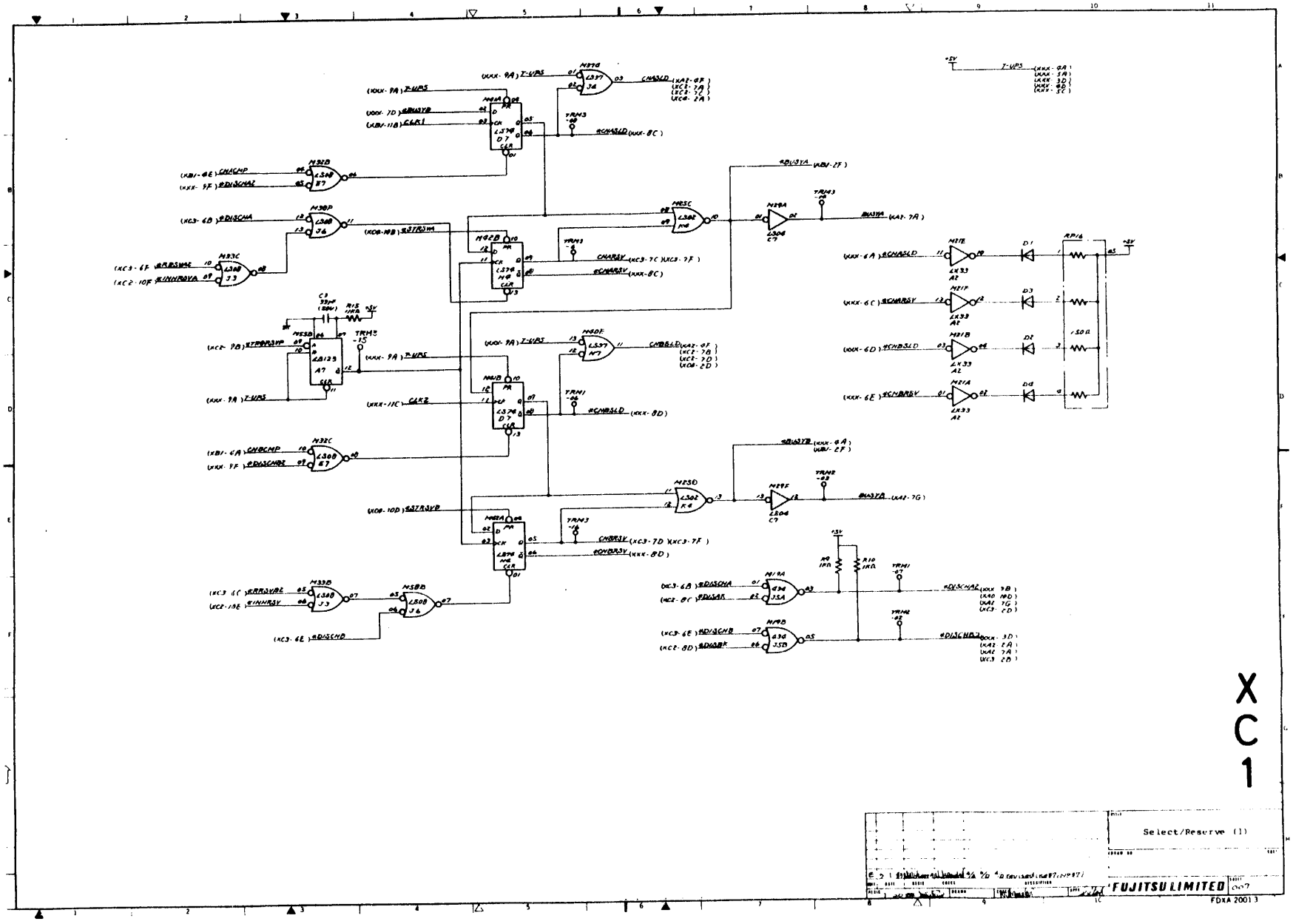

CN1B
CN2E
CN3A
CN3AA
CN31
CN3C
CN3D
XA0
Interface Connection
Connection with CQFM PCB
FUJITSU LIMITED
FDXA 2001 3

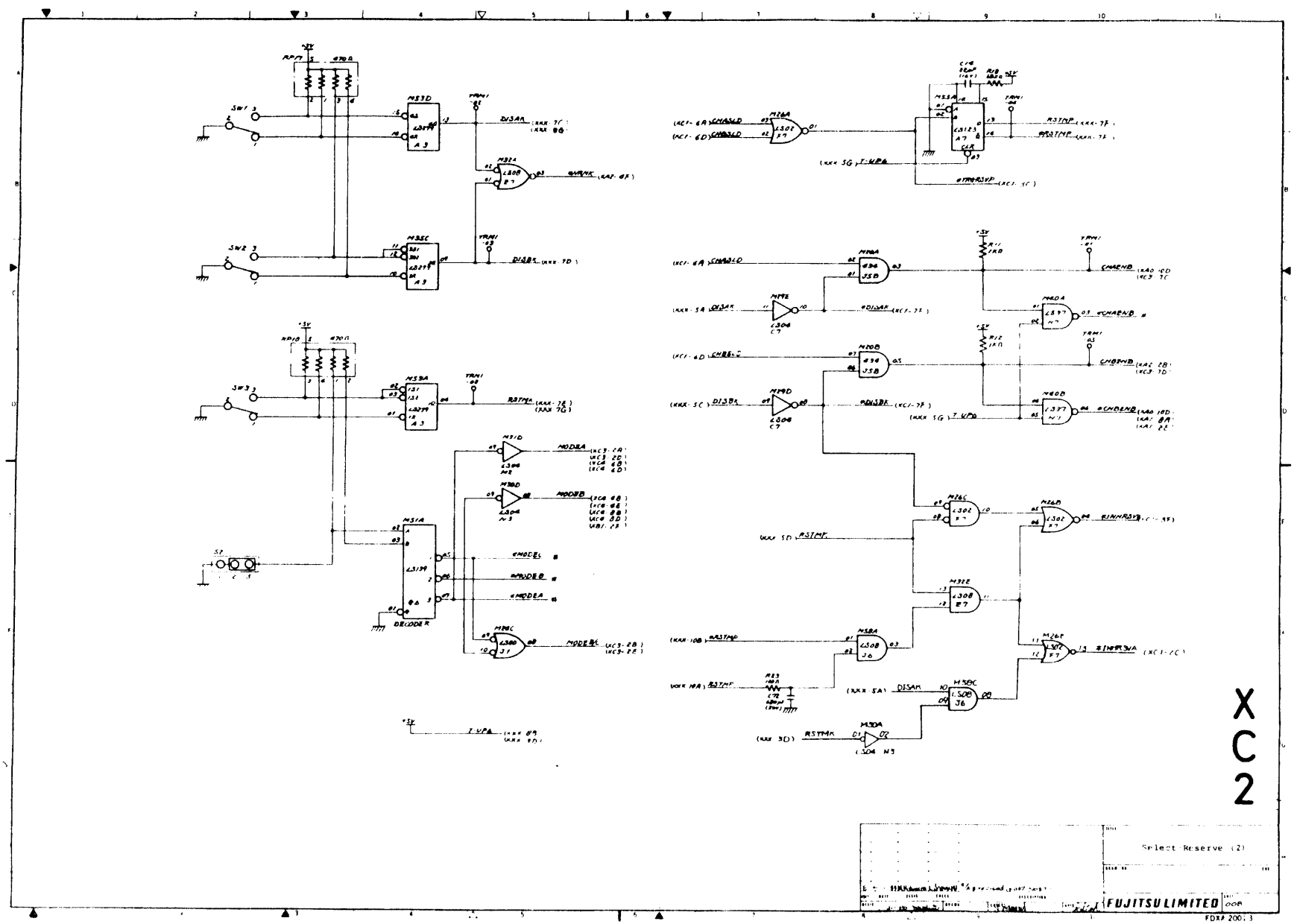


X
A
1

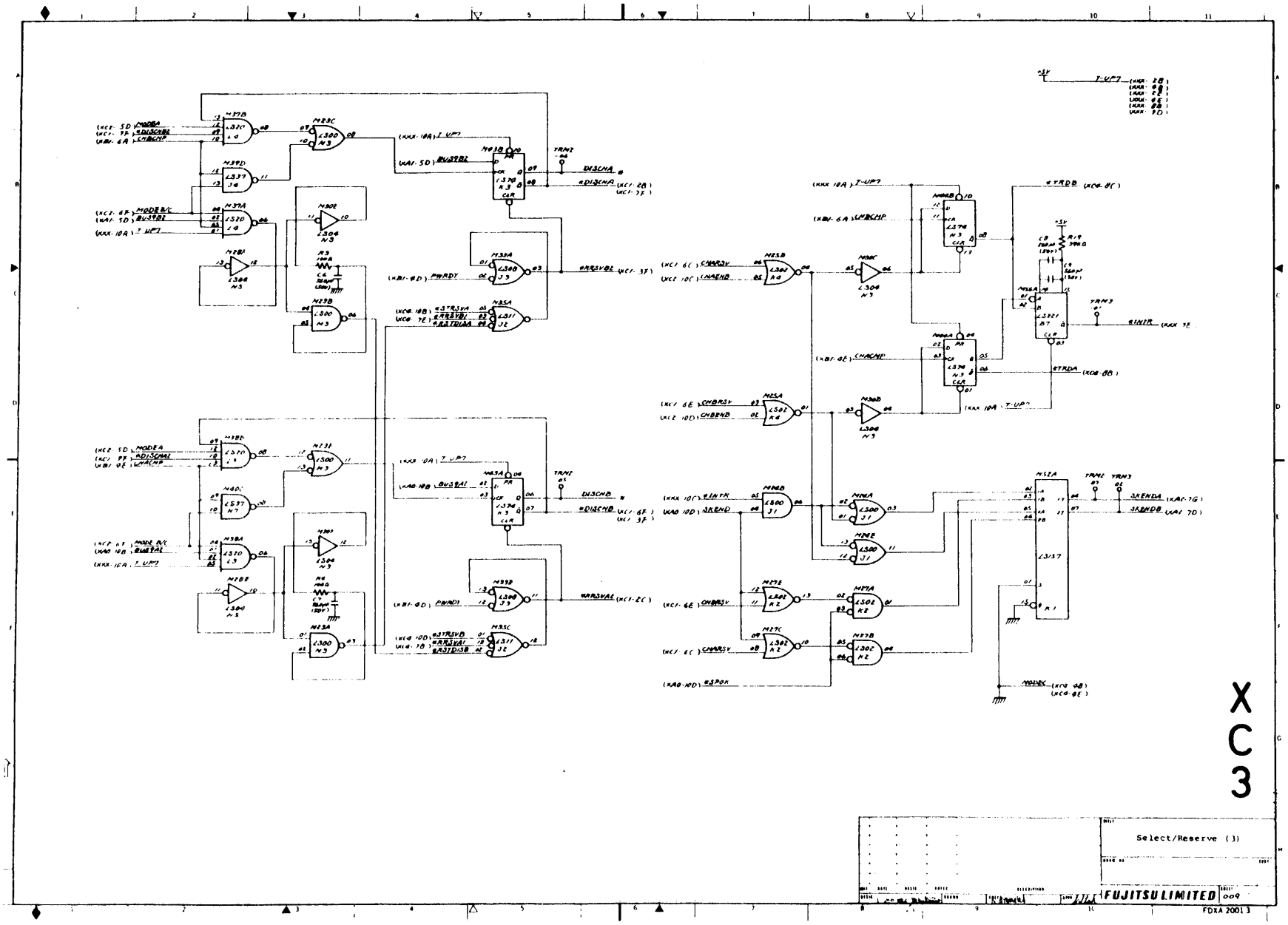

XA2
A/B-Cable Drivers
CHA B-Cable Drivers
FUJITSU LIMITED
FDxA 2001 3

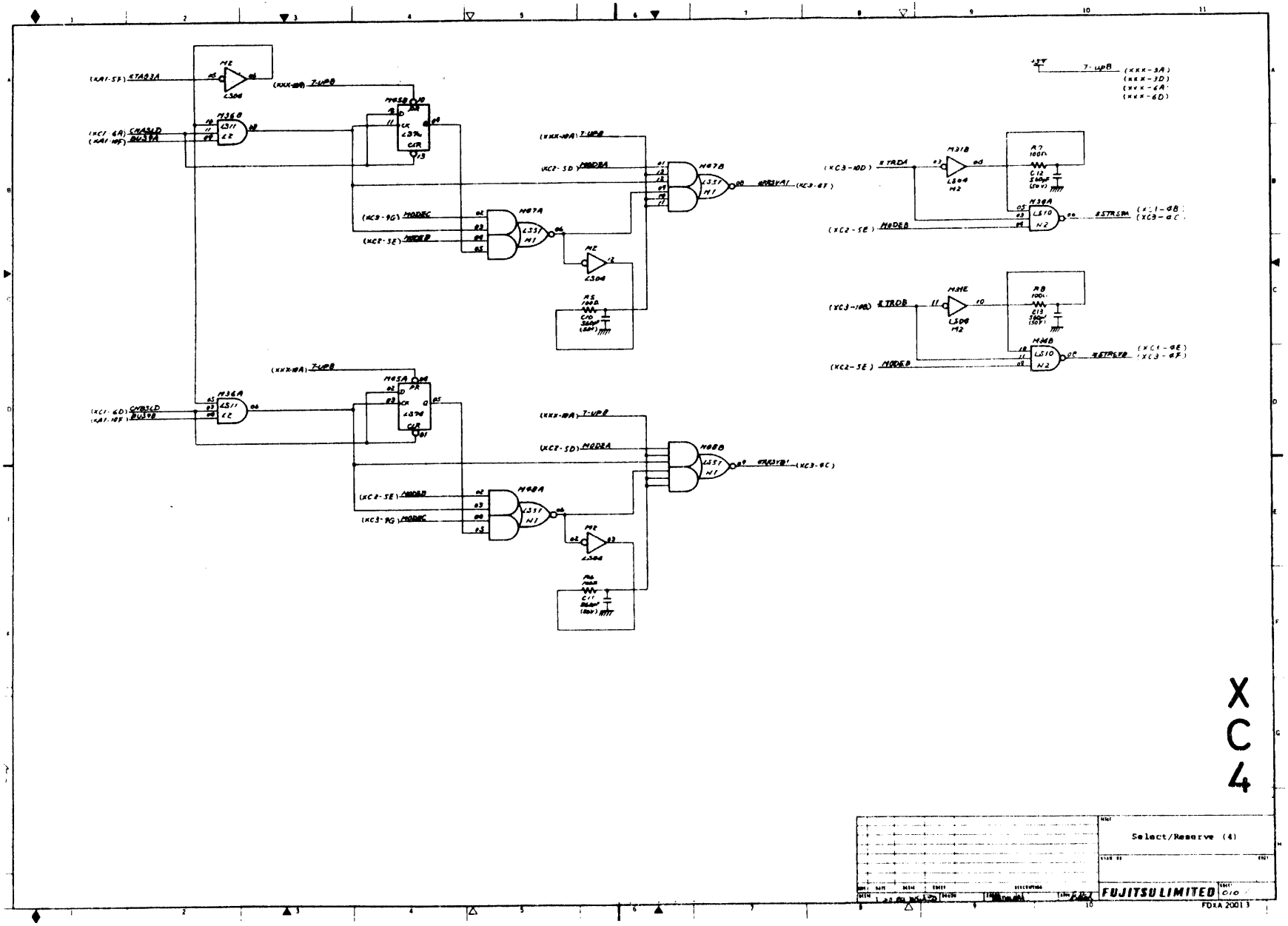

Unit Selection
FUJITSU LIMITED
FDXA 2001 3
X
B
1

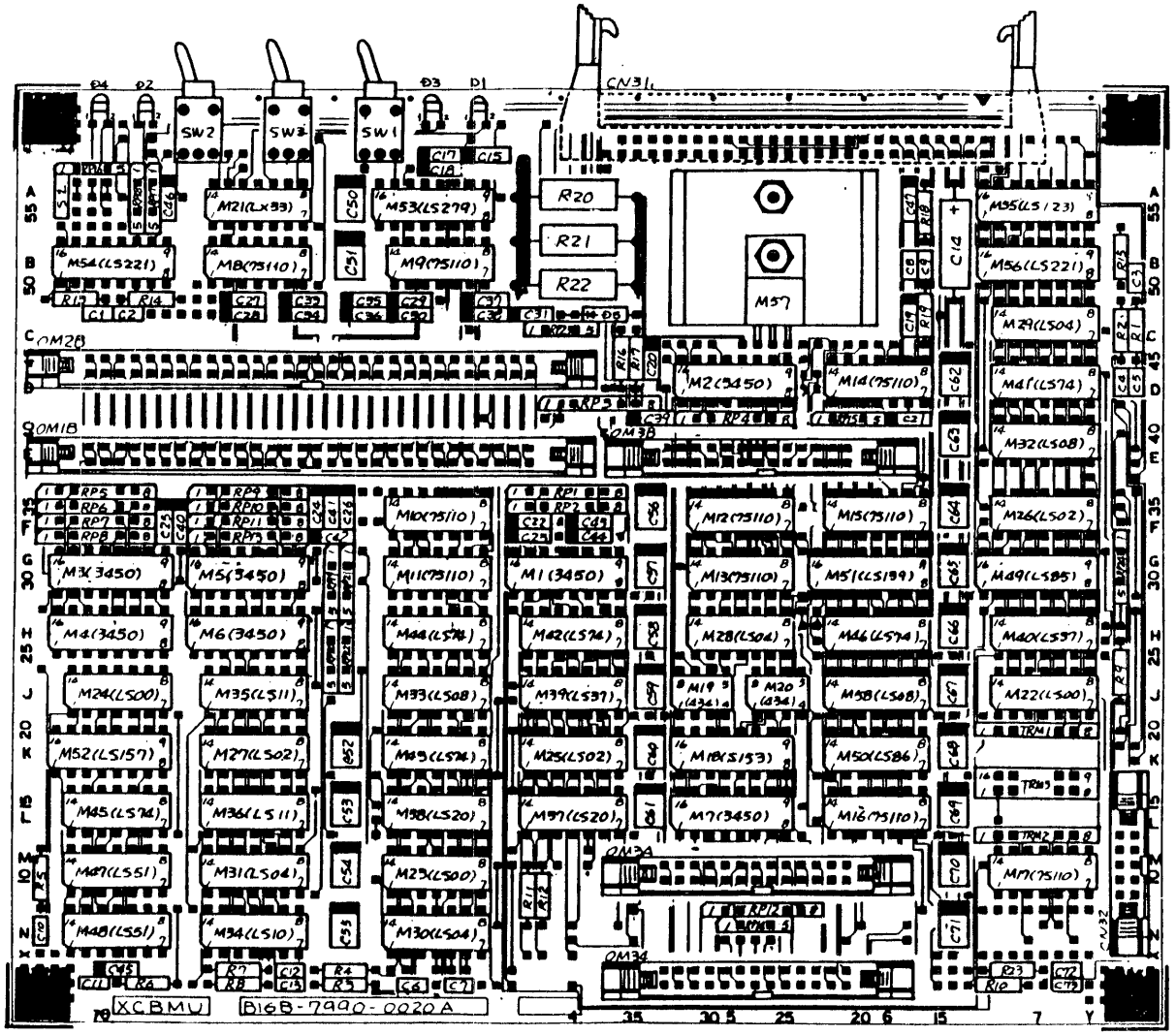

XC1
Select/Reserve (1)
FUJITSU LIMITED
FDXA 20013



XC2


XC3
Select/Reserve (3)
FUJITSU LIMITED
FDXA 2001 3


XC4
Select/Reserve (4)
FUJITSU LIMITED
FDKA 2001 3



Cross-call B (XCBM)
PCB Assembly Drawing

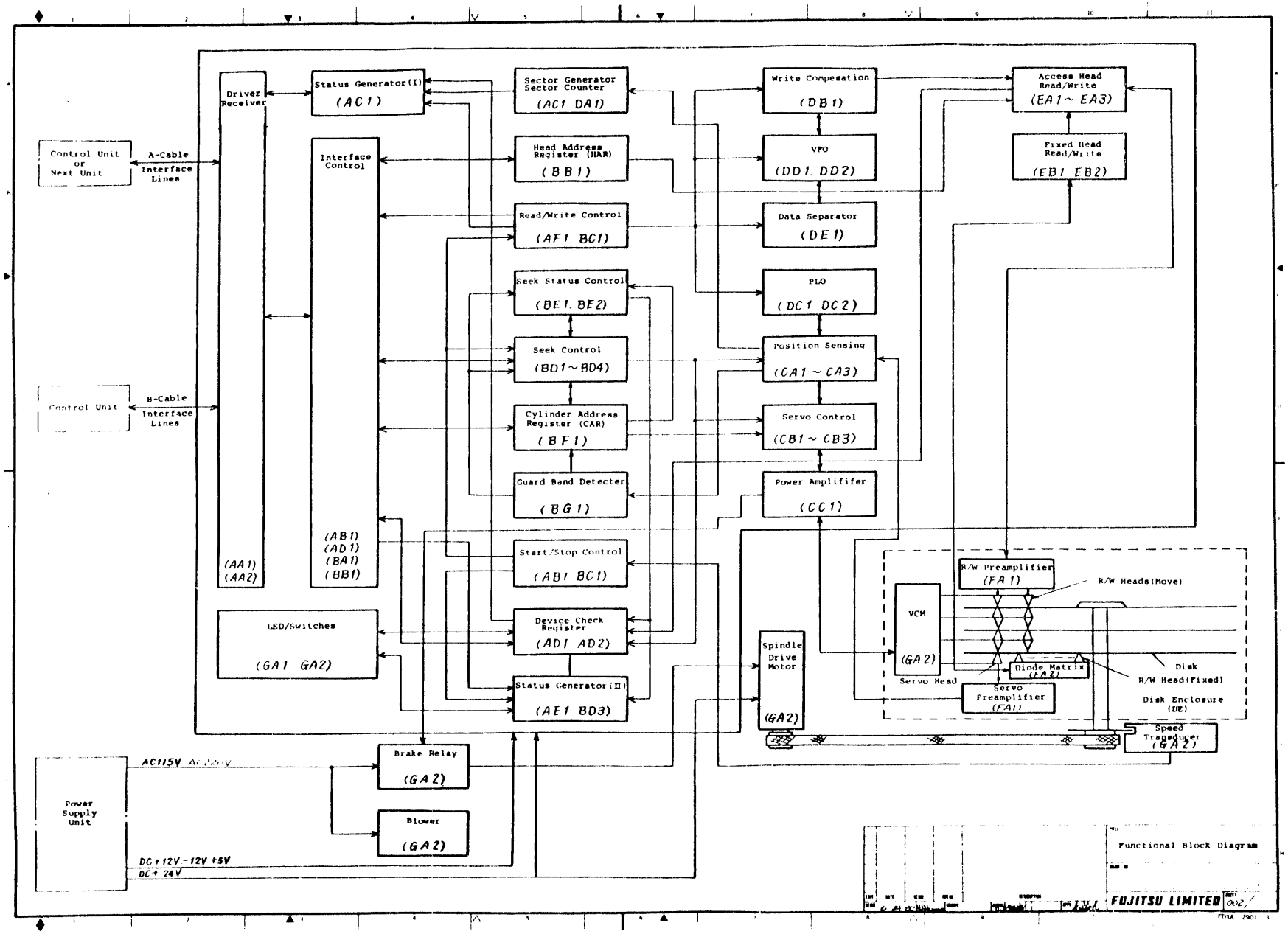
FUJITSU LIMITED

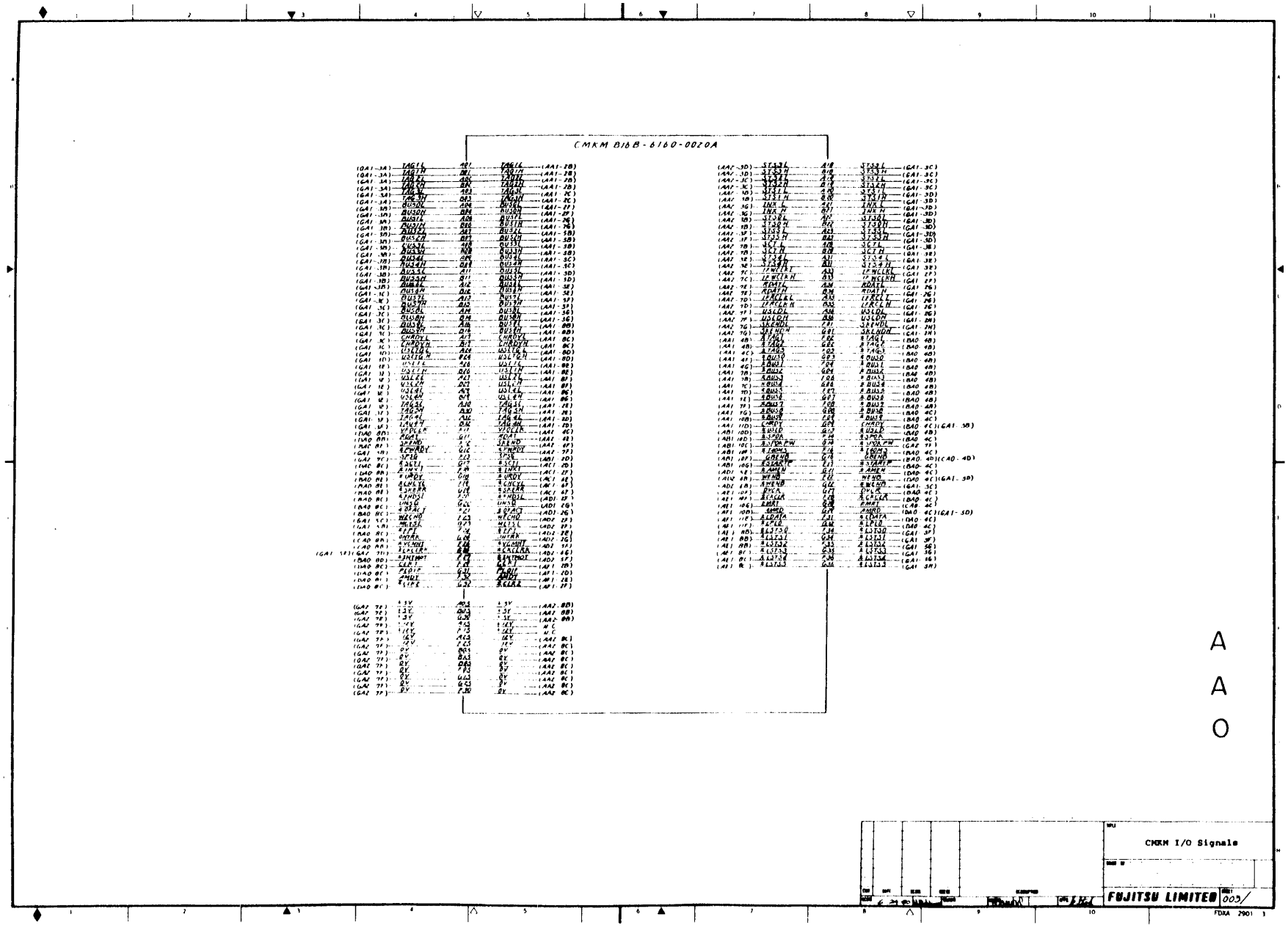
PART 3
Basic Schematics (Old)

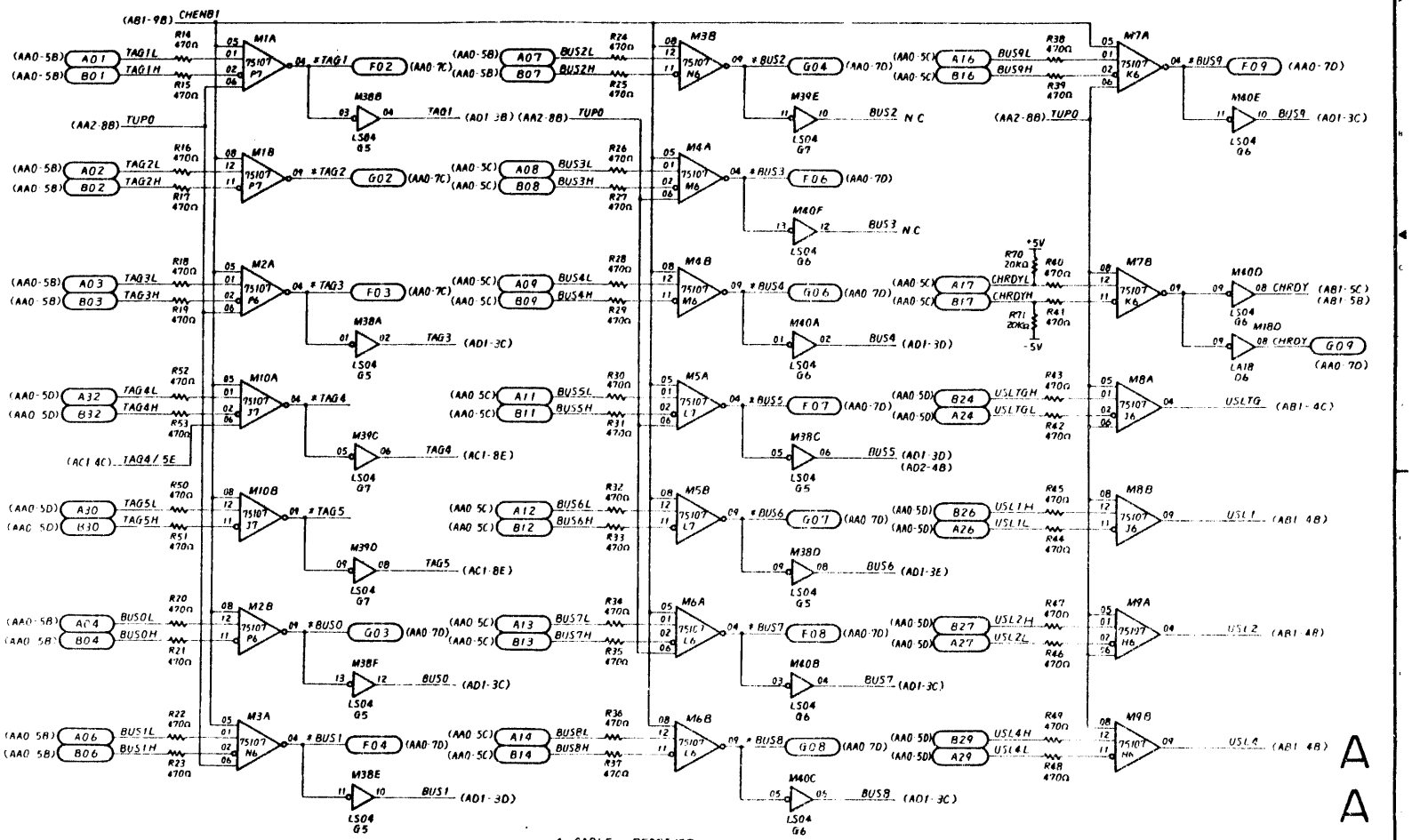
SHEET	ABBR	TITLE
001		Schematics/Drawings List
002		Functional Block Diagram
003	AA0	CMKM I/O Signals
004	AA1	A-Cable Receivers
005	AA2	A/B-Cable Drivers
006	AB1	Unit Selection Start/Stop Control
007	AC1	Sector Address Reg. Status Generator(1)
008	AD1	Control Check Detector
009	AD2	Read/Write Check Detector
010	AE1	Status Generator(2)
011	AF1	Read/Write Control
012	BA0	CMIM I/O Signals
013	BA1	Buffers
014	BB1	Head Address Reg. Offset Control
015	BC1	VFO/PLO Control
016	BD1	Seek Control(1)
017	BD2	Seek Control(2) Seek Error Latch
018	BD3	Seek Control(3) LED Drivers
019	BD4	Seek Cotrol(4)
020	BE1	Seek Status Generator
021	BE2	Seek Error Detector
022	BF1	Cylinder Address Register (CAR)
023	BG1	Guard Bands Detector
024	CA0	SDIM I/O Signals
025	CA1	Position Sensing(1)
026	CA2	Position Sensing(2) PLO I
027	CA3	Position Sensing(3)
028	CB1	Servo Control(1)
029	CB2	Servo Control(2)
030	CB3	Servo Control(3)
031	CC1	Power Amplifier
032	DA0	VOFM I/O Signals
033	DA1	Sector Generator
034	DB1	Write Compensation(1)
035	DB2	Write Compesation(2)
036	DC1	PLO II(1)
037	DC2	PLO II(2)
038	DD1	VFO(1)
039	DD2	VFO(2)
040	DE1	Data Separator
041	EA0	RQVM/RQWM I/O Signals
042	EA1	Access Head Read/Write(1)
043	EA2	Access Head Read/Write(2)
044	EA3	Access Head Read/Write(3)
045	EB1	Fixed Head Read/Write
046	EB2	Fixed Head Select Driver
047	FA1	R/W, Servo Head Preamplifier
048	FA2	Fixed Head Diode Matrix
049	GA1	I/O Connectors LED's/Switches
050	GA2	AC/DC Power Supply
051		CMKM PCB Assembly
052		CMIM PCB Assembly
053		SDIM PCB Assembly
054		VOFM PCB Assembly
055		RQVM PCB Assembly
056		RQWM PCB Assembly
057		GBGM PCB Assembly

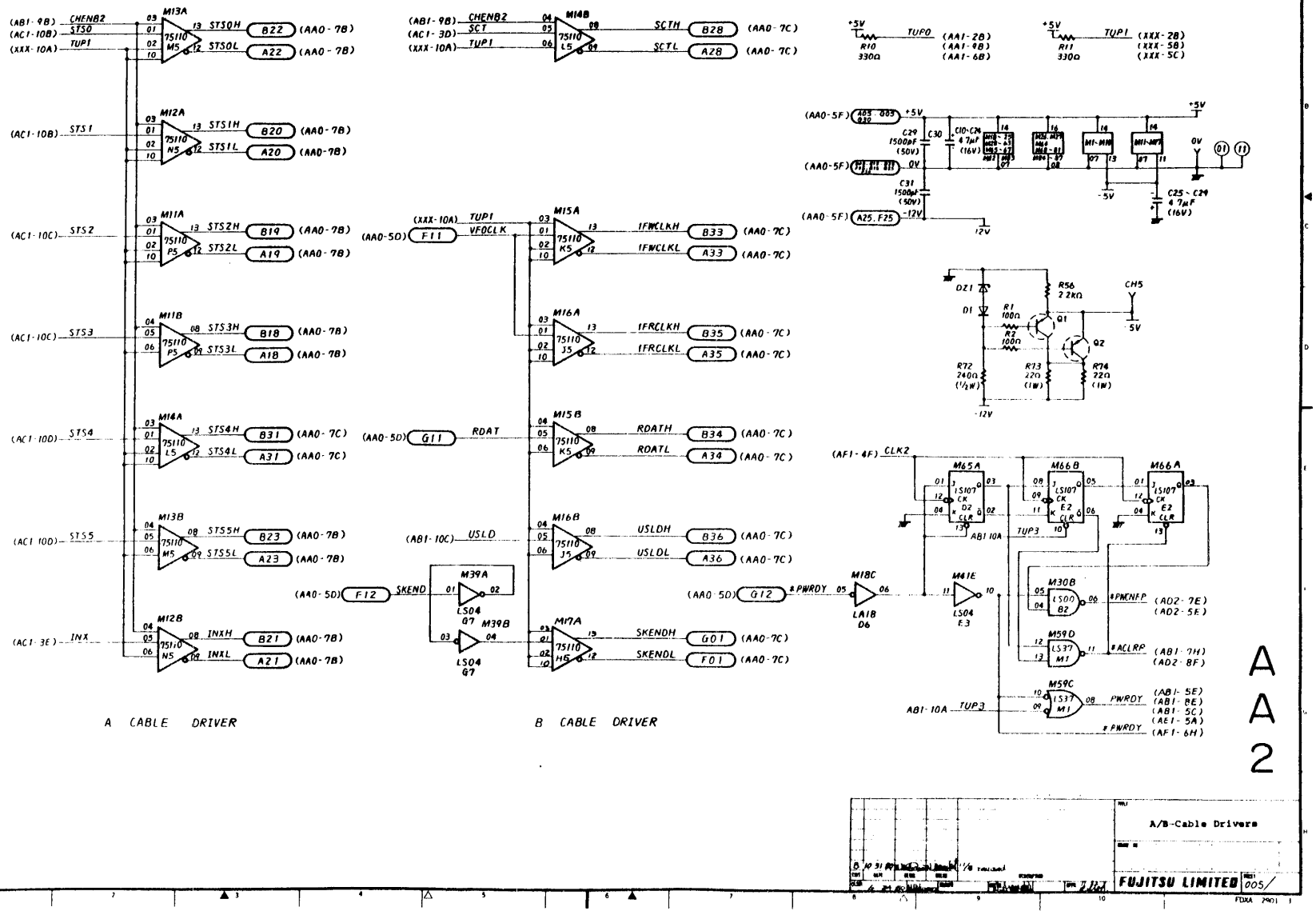
Schematics/Drawings List

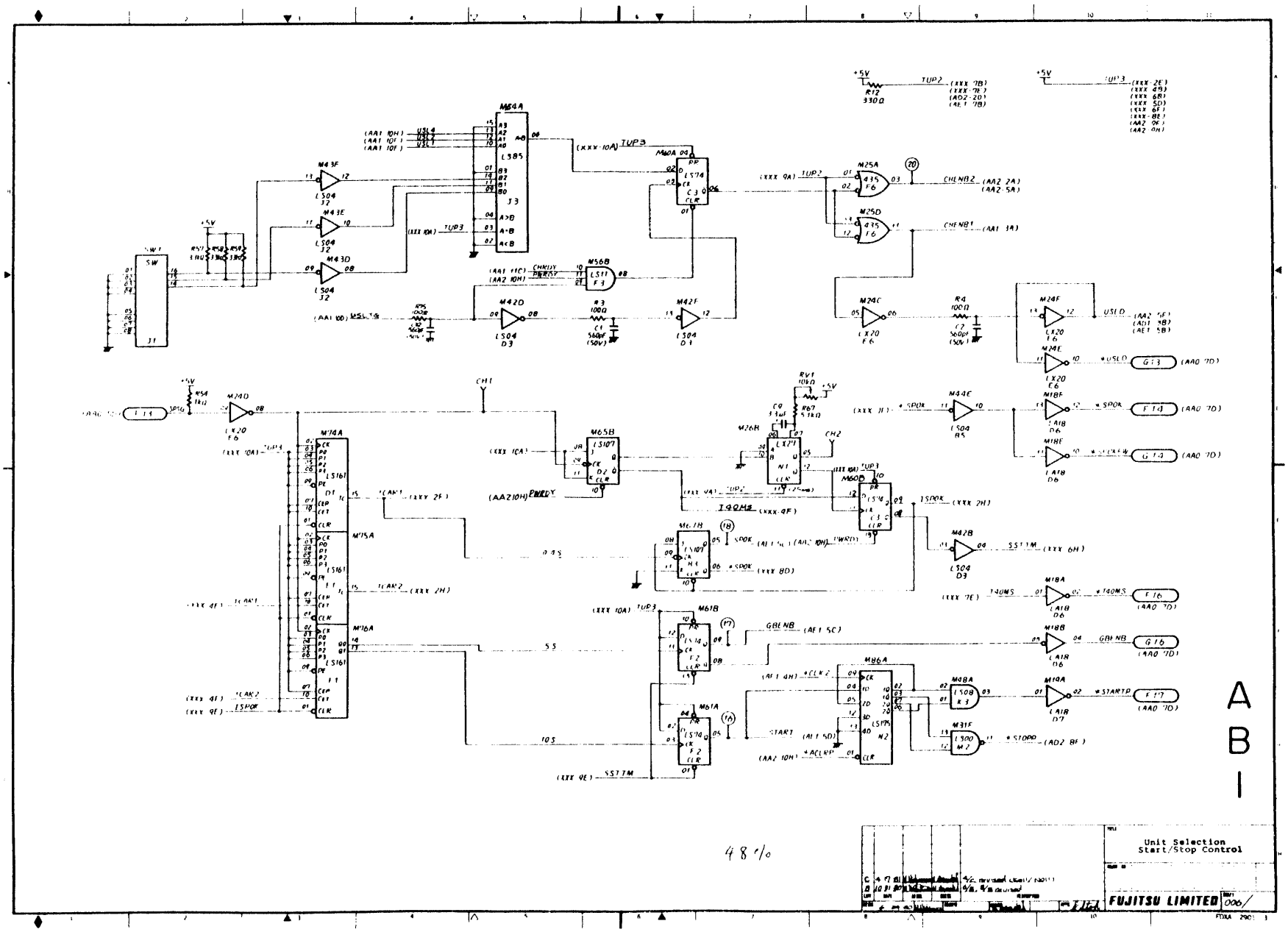
FUJITSU LIMITED 001/57

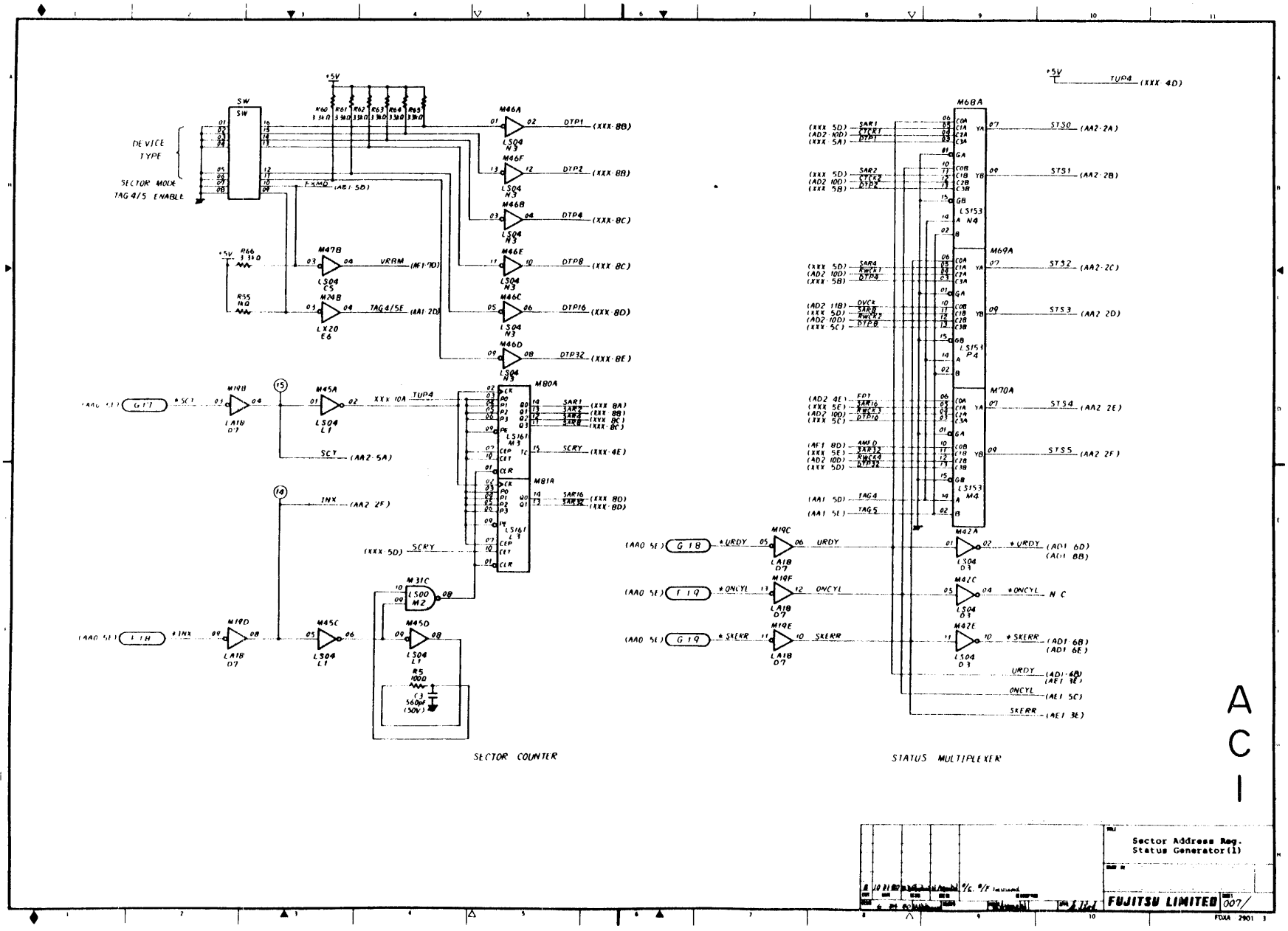

Control Unit or Next Unit
A-Cable Interface Lines
Control Unit
B-Cable Interface Lines
Driver Receiver
(AA1)
(AA2)
Interface Control
(AB1)
(AD1)
(BA1)
(BB1)
LED/Switches
(GA1 GA2)
Status Generator(I)
(AC1)
Sector Generator Sector Counter
(AC1 DA1)
Head Address Register (HAR)
(BB1)
Read/Write Control
(AF1 BC1)
Seek Status Control
(BE1 BE2)
Seek Control
(BD1~BD4)
Cylinder Address Register (CAR)
(BF1)
Guard Band Detecter
(BG1)
Start/Stop Control
(AB1 BC1)
Device Check Register
(AD1 AD2)
Status Generator(II)
(AE1 BD3)
Write Compesation
(DB1)
VFO
(DD1. DD2)
Data Separator
(DE1)
PLO
(DC1 DC2)
Position Sensing
(CA1~CA3)
Servo Control
(CB1~CB3)
Power Amplifier
(CC1)
Access Head Read/Write
(EA1~EA3)
Fixed Head Read/Write
(EB1 EB2)
R/W Preamplifier
(FA1)
R/W Heads(Move)
VCM
(GA2)
Servo Head
Diode Matrix
(FA2)
Servo Preamplifier
(FA1)
Disk
R/W Head(Fixed)
Disk Enclosure
(DE)
Spindle Drive Motor
(GA2)
Speed Transducer
(GA2)
Brake Relay
(GA2)
Blower
(GA2)
Power Supply Unit
AC115V AC220V
DC+12V -12V +5V
DC+24V
Functional Block Diagram
FUJITSU LIMITED

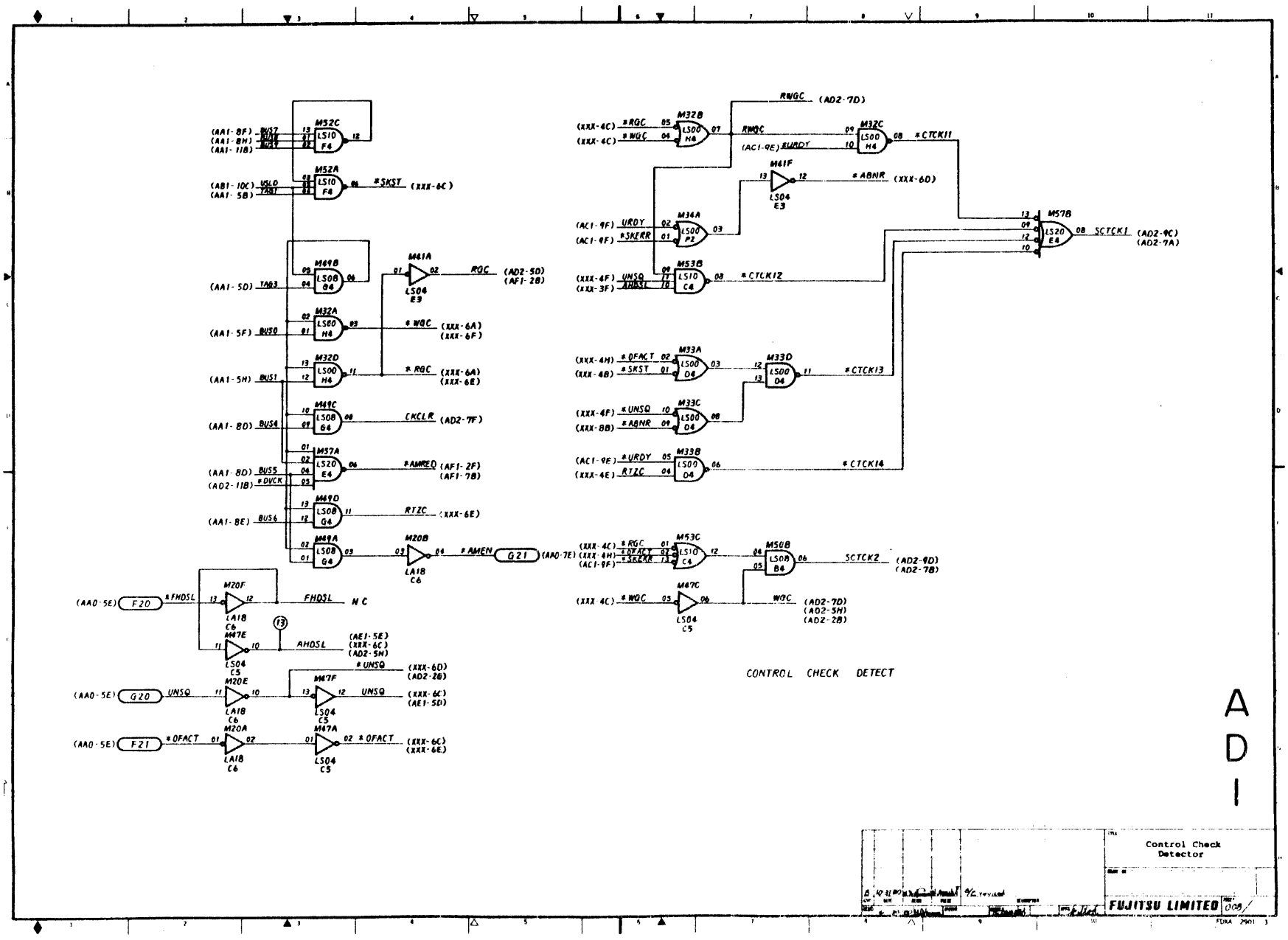

CMKM B16B-6160-0020A
A
A
0
CMKM I/O Signals
FUJITSU LIMITED
FDRA 2901

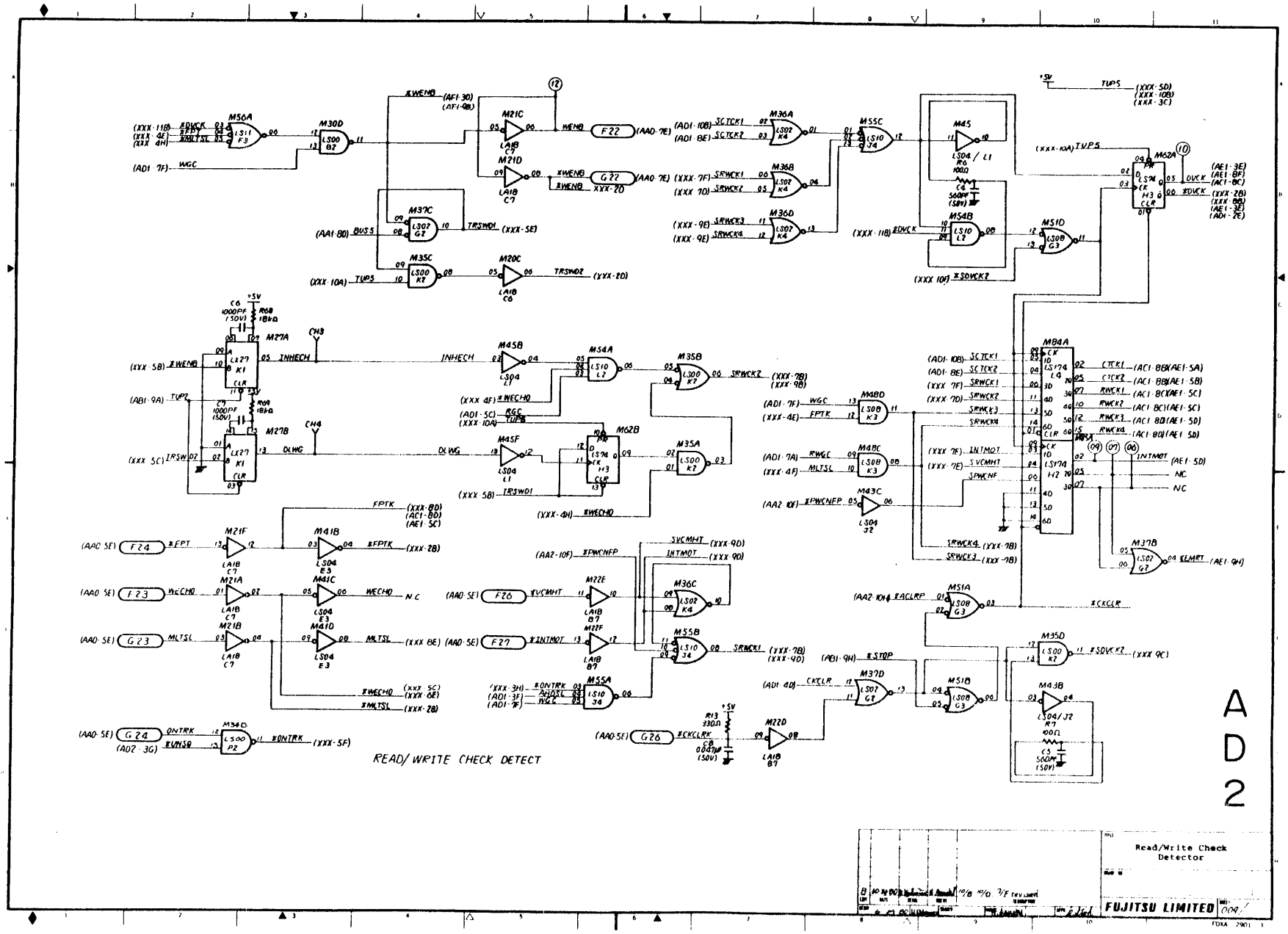

(AB1-9B) CHENB1
(AA2-8B) TUP0
(AC1-4C) TAG4/5E
A CABLE RECEIVER
A-Cable Receivers
FUJITSU LIMITED
A
A
1

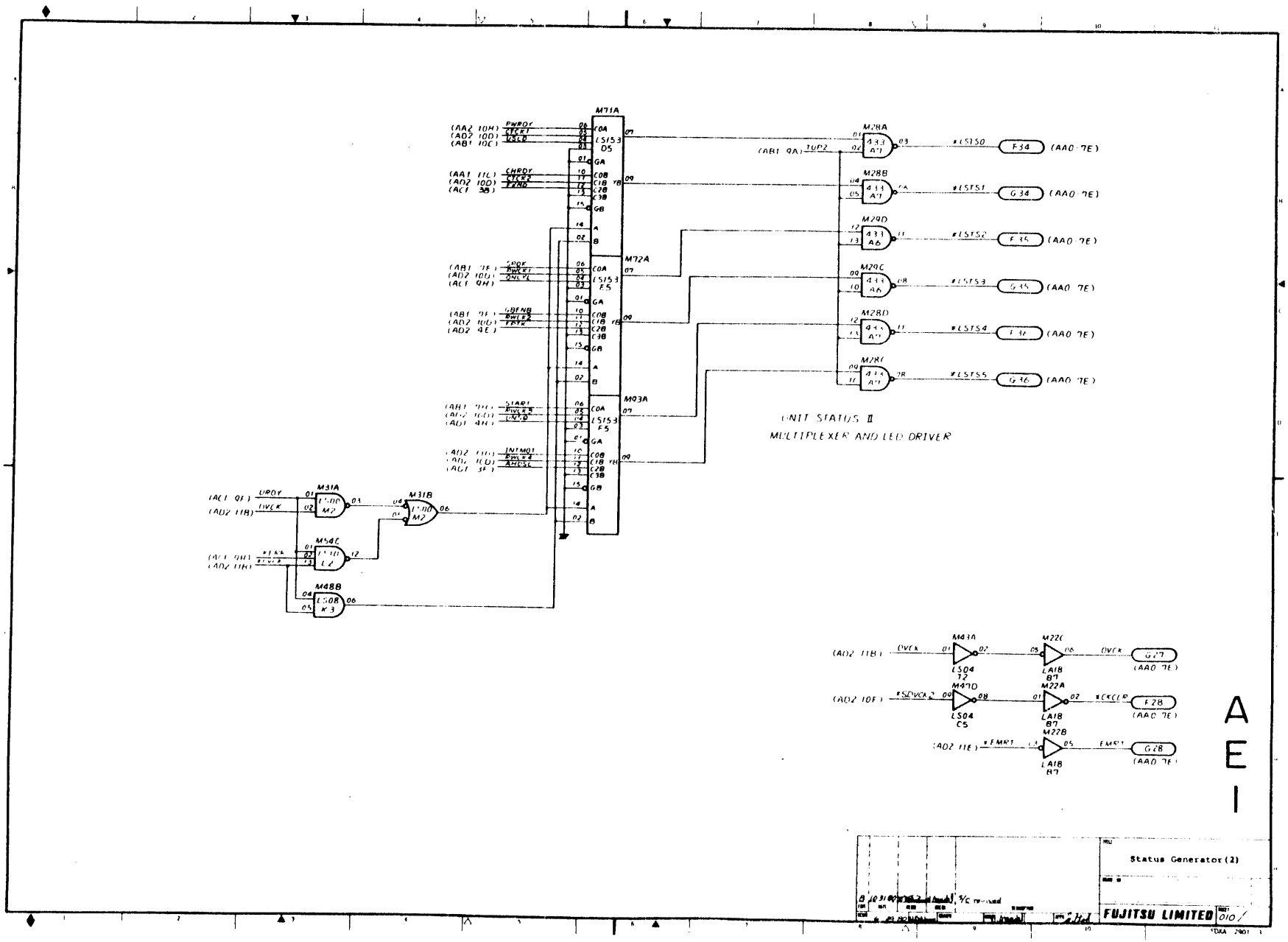

A CABLE DRIVER
B CABLE DRIVER
A/B-Cable Drivers
FUJITSU LIMITED
A A 2

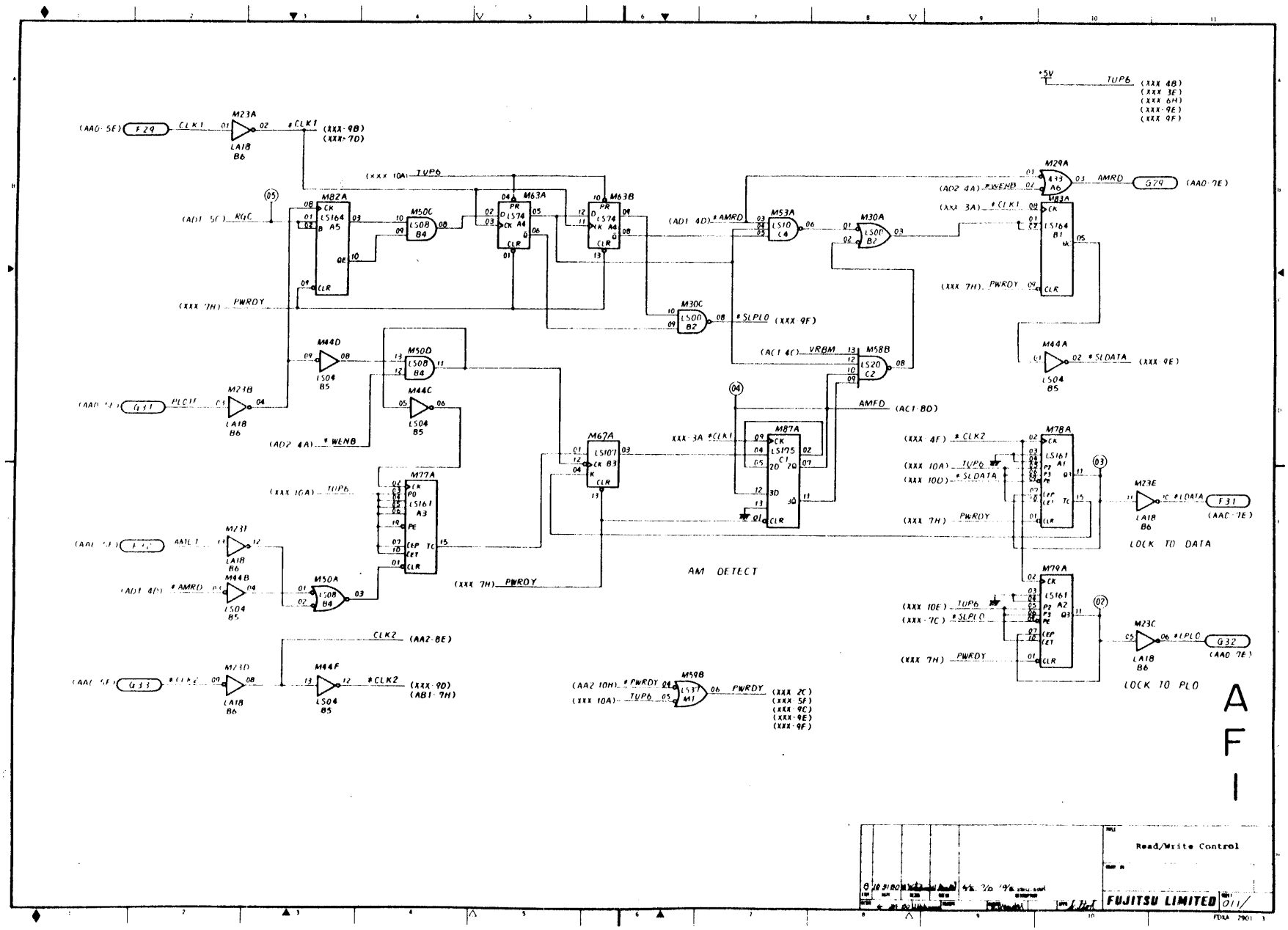

Unit Selection
Start/Stop Control
FUJITSU LIMITED
A
B
I

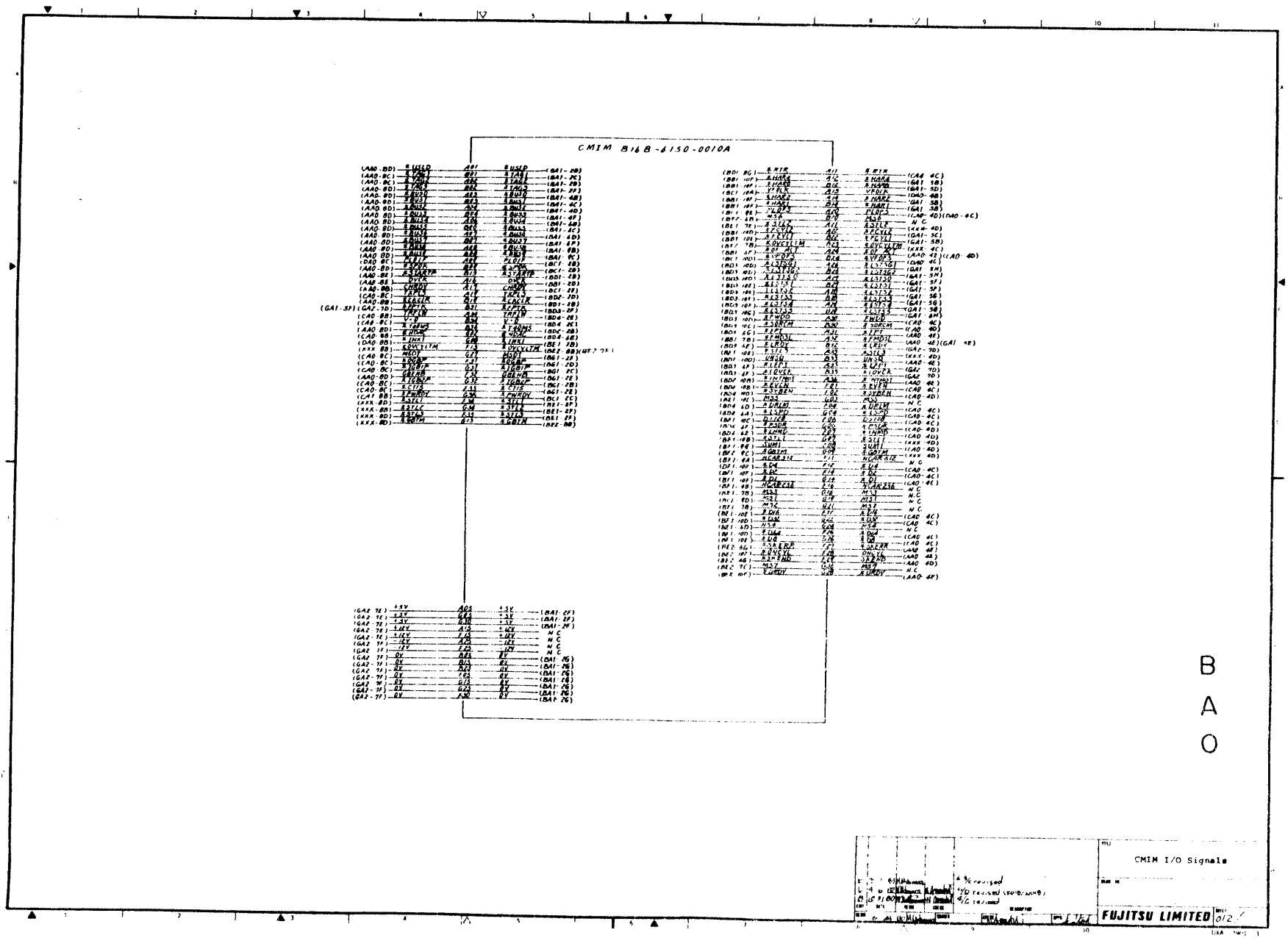

SECTOR COUNTER
STATUS MULTIPLEXER
Sector Address Reg.
Status Generator(I)
FUJITSU LIMITED
A
C
I


CONTROL CHECK DETECT
Control Check Detector
FUJITSU LIMITED
A
D
I


READ/WRITE CHECK DETECT
A D 2
Read/Write Check Detector
FUJITSU LIMITED

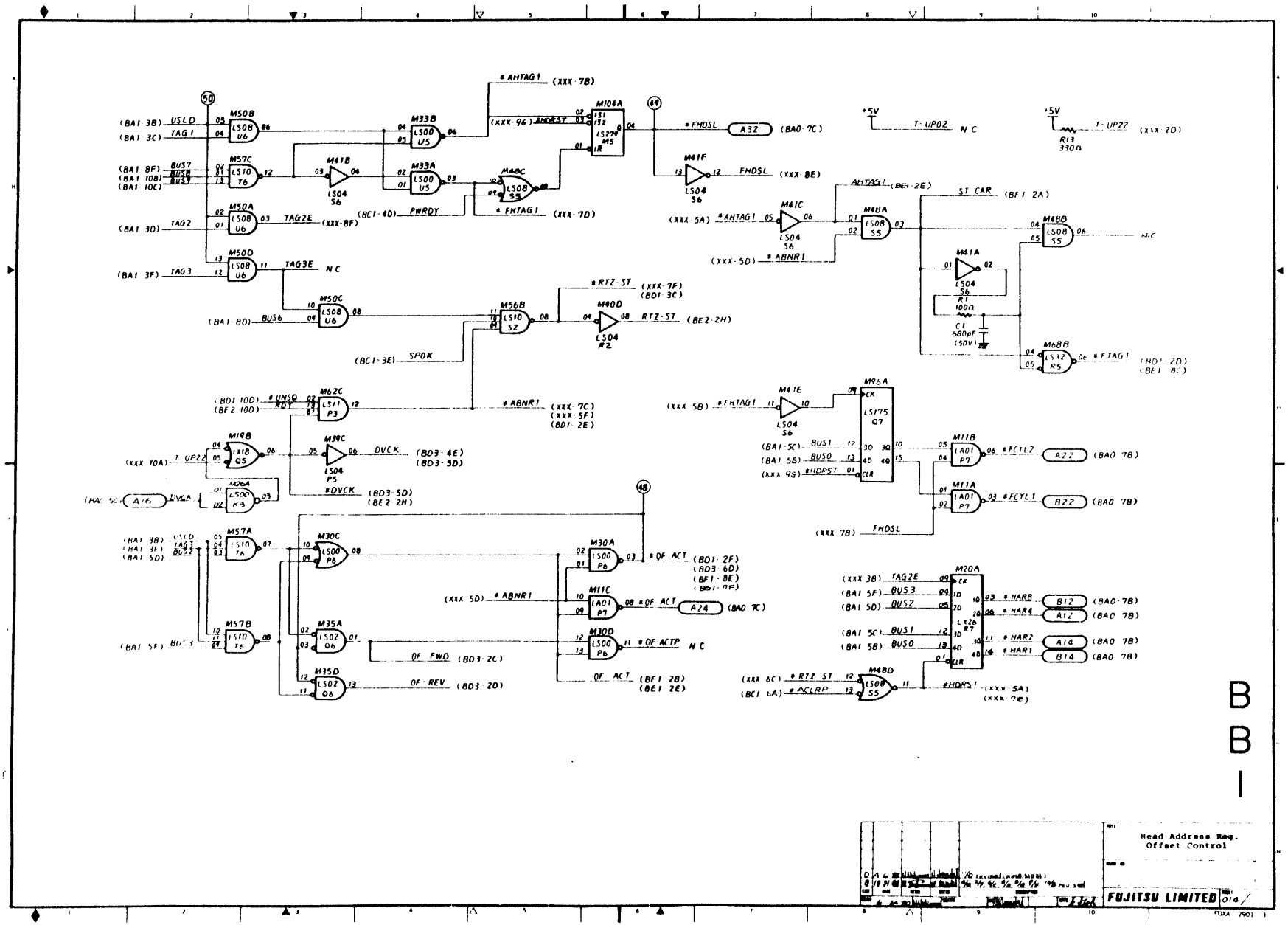

M71A
M72A
M93A
M28A
M28B
M29D
M29C
M28D
M28E
UNIT STATUS II
MULTIPLEXER AND LED DRIVER
M31A
M31B
M56C
M48B
M43A
M22C
M47D
M22A
M22B
Status Generator(2)
FUJITSU LIMITED

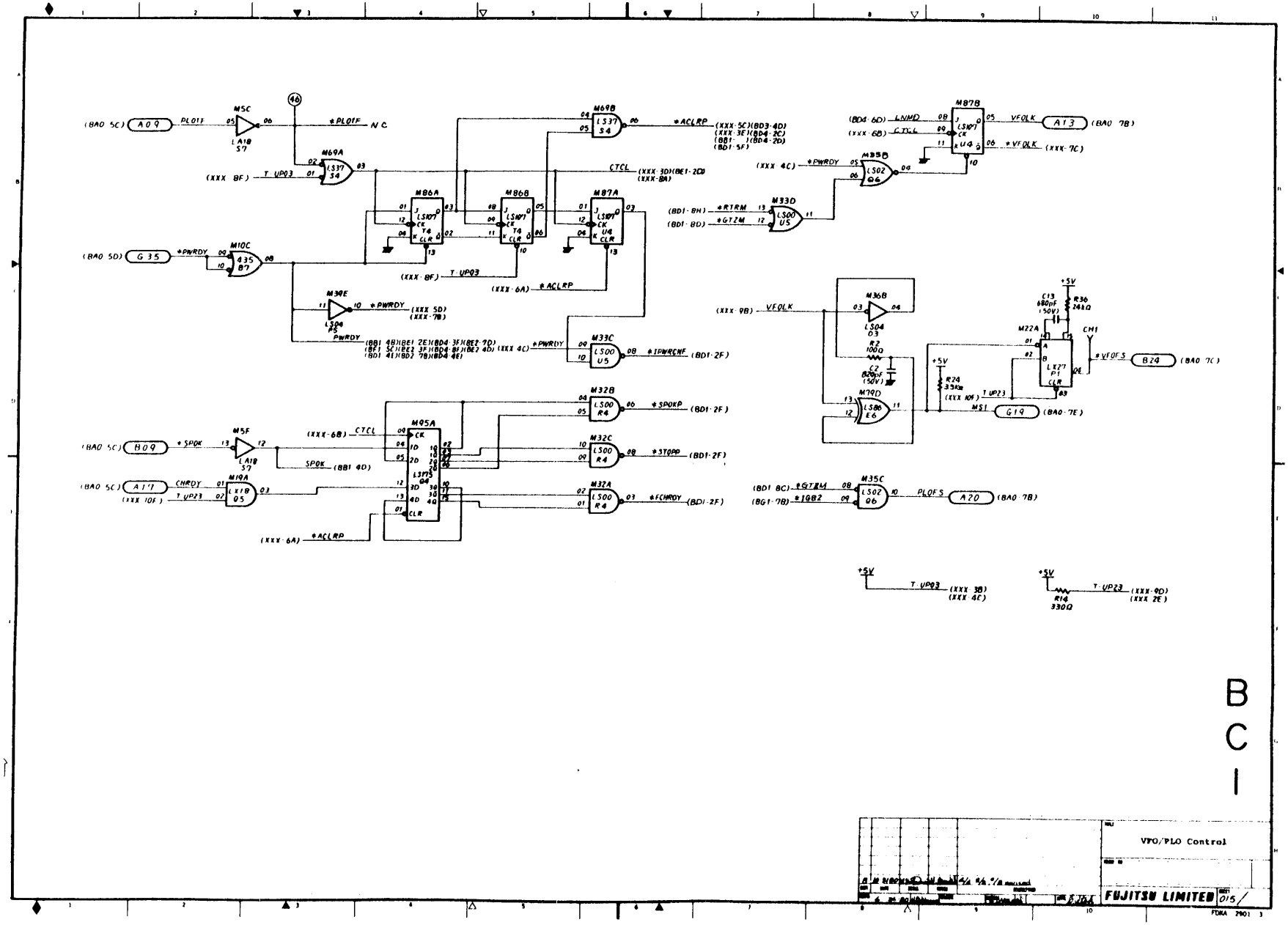

AM DETECT
LOCK TO DATA
LOCK TO PLO
Read/Write Control
FUJITSU LIMITED

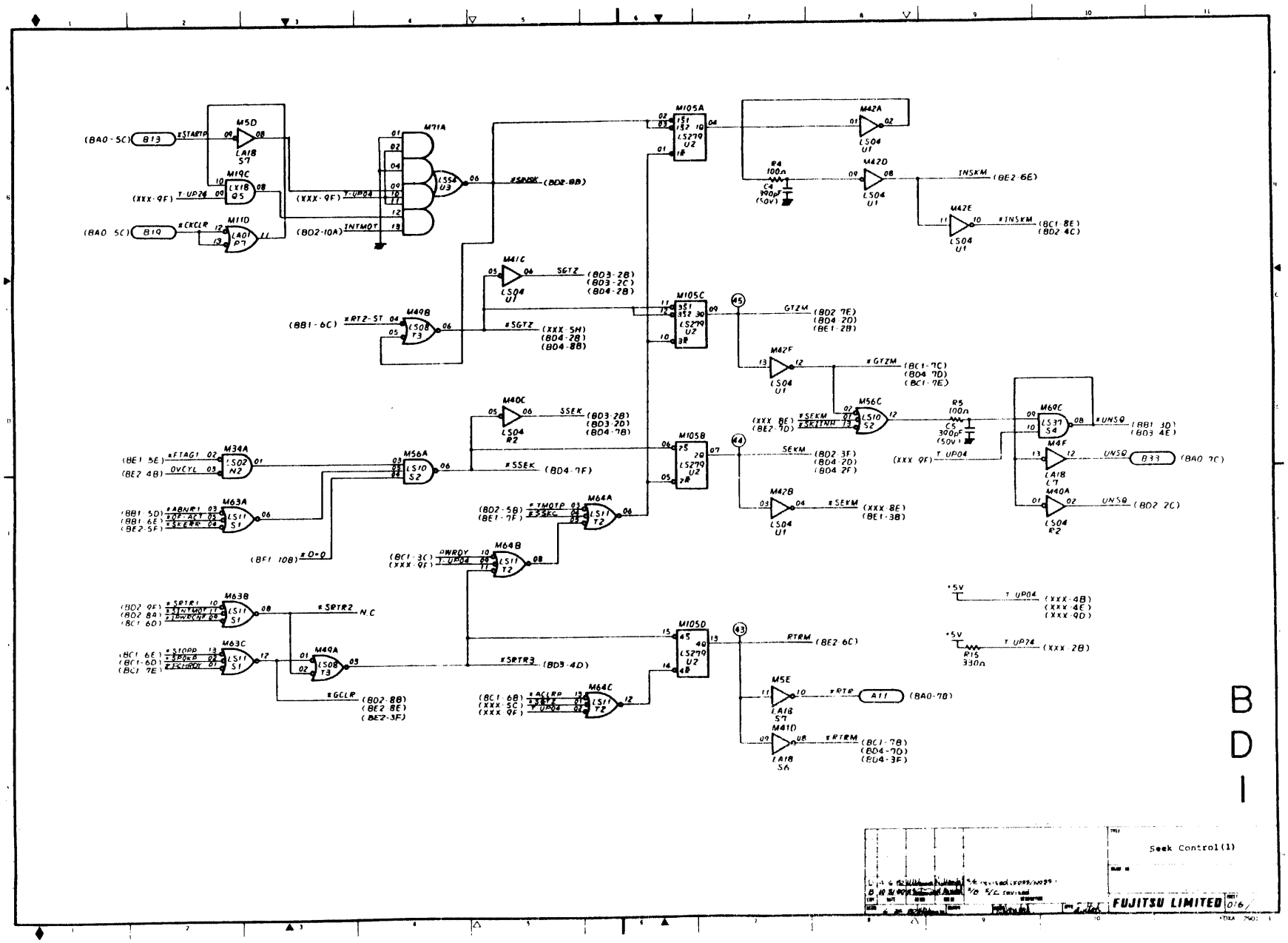


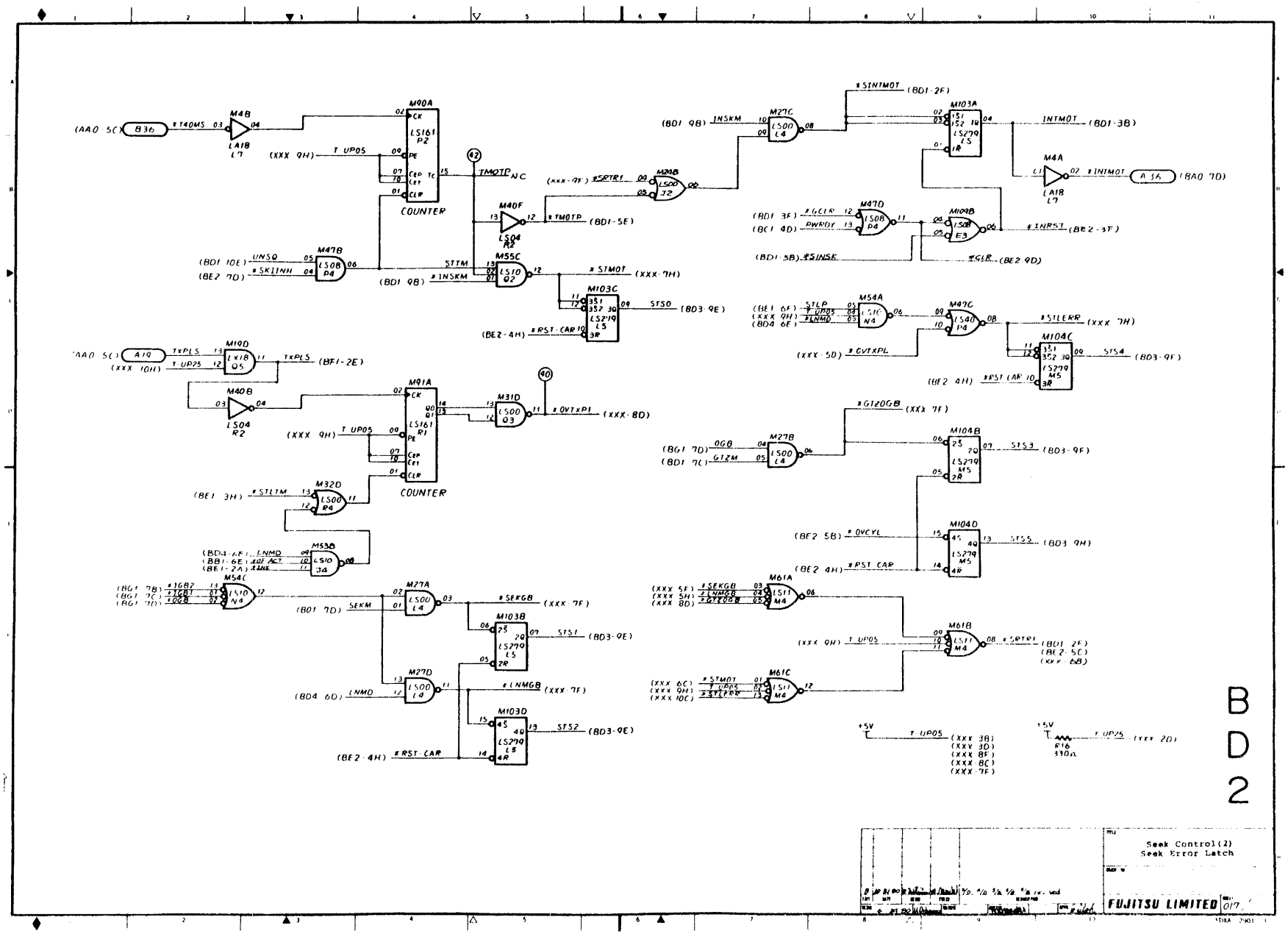
B
A
0

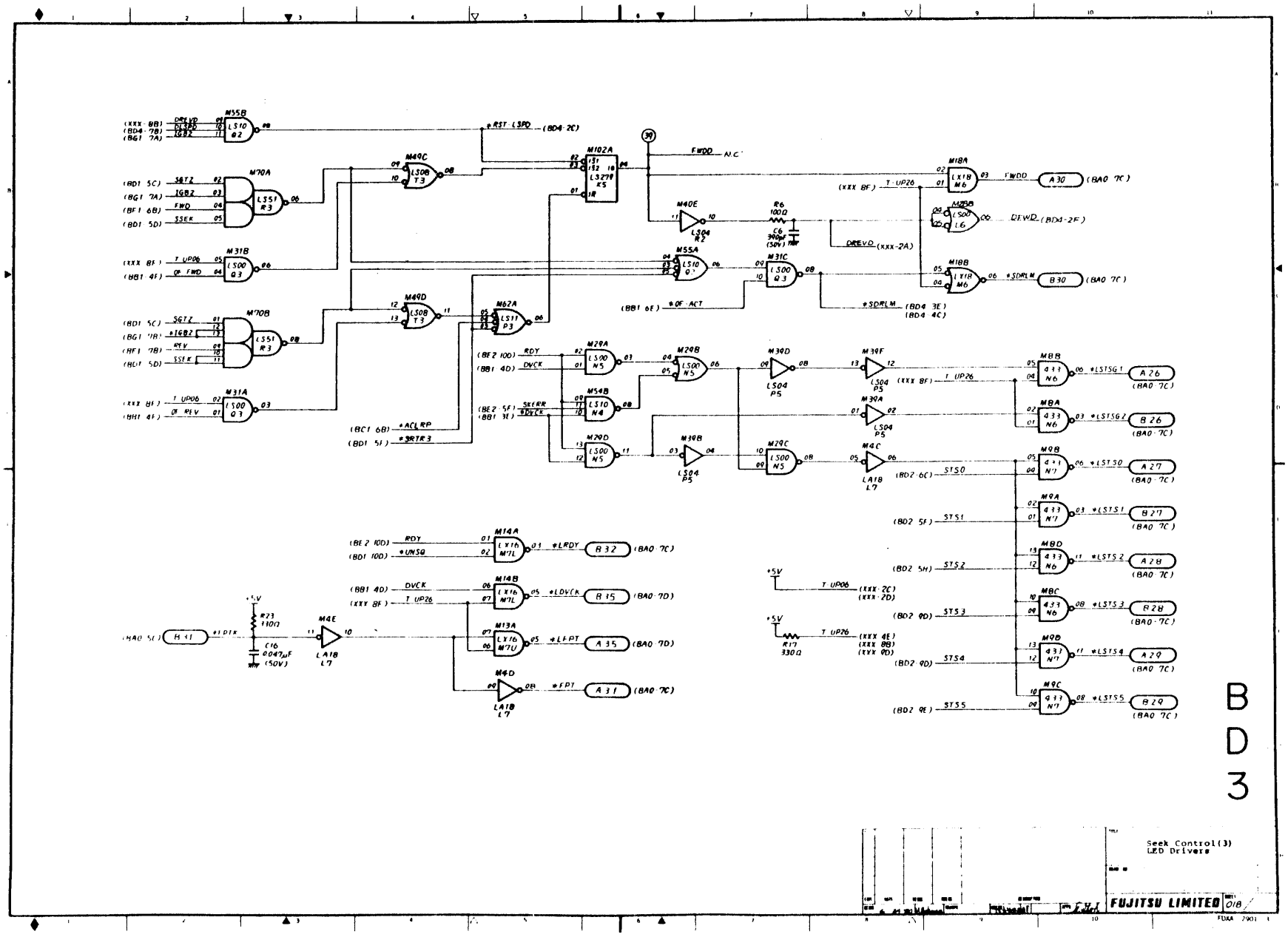

(BA0-5B) A01 *USLD M7F LA18 U7 USLD (BB1-2A) (BB1-2E) (BA0-5B) A03 *BUS0 M6B LA18 T7 BUS0 (BB1-8E) (BB1-8F) (BF1-2D) (BA0-5B) A06 *BUS4 M6F LA18 T7 BUS4 (BF1-2C) (BA0-5C) A08 *BUS8 M5A LA18 S7 BUS8 (BB1-2B) (BF1-2B)
(BA0-5B) B01 *TAG1 M7E LA18 U7 TAG1 (BB1-2B) (BA0-5B) B03 *BUS1 M6C LA18 T7 BUS1 (BB1-8D) (BB1-8F) (BF1-2D) (BA0-5B) B06 *BUS5 M7C LA18 U7 BUS5 (BF1-2C) (BA0-5C) B08 *BUS9 M5B LA18 S7 BUS9 (BB1-2B) (BF1-2A)
(BA0-5B) A02 *TAG2 M7D LA18 U7 TAG2 (BB1-2B) (BA0-5B) A04 *BUS2 M6D LA18 T7 BUS2 (BB1-8F) (BB1-2E) (BF1-5D) (BA0-5B) A07 *BUS6 M7A LA18 U7 BUS6 (BB1-3C) (BF1-2C)
(BA0-5B) B02 *TAG3 M6A LA18 T7 TAG3 (BB1-2C) (BA0-5B) B04 *BUS3 M6E LA18 T7 BUS3 (BB1-2F) (BB1-8F) (BF1-2D) (BA0-5B) B07 *BUS7 M7B LA18 U7 BUS7 (BB1-2B) (BF1-2C)
(BA0-5F) (BA0-5F) (BA0-5G) C20-C39 4.7μF (16V) M12 M13 M14 M15 M16 M17 M18 M19 M20 M21 M22 M23 M24 M25 M26 M27 M28 CH0 21 31 41
B
A
I
Buffers
FUJITSU LIMITED

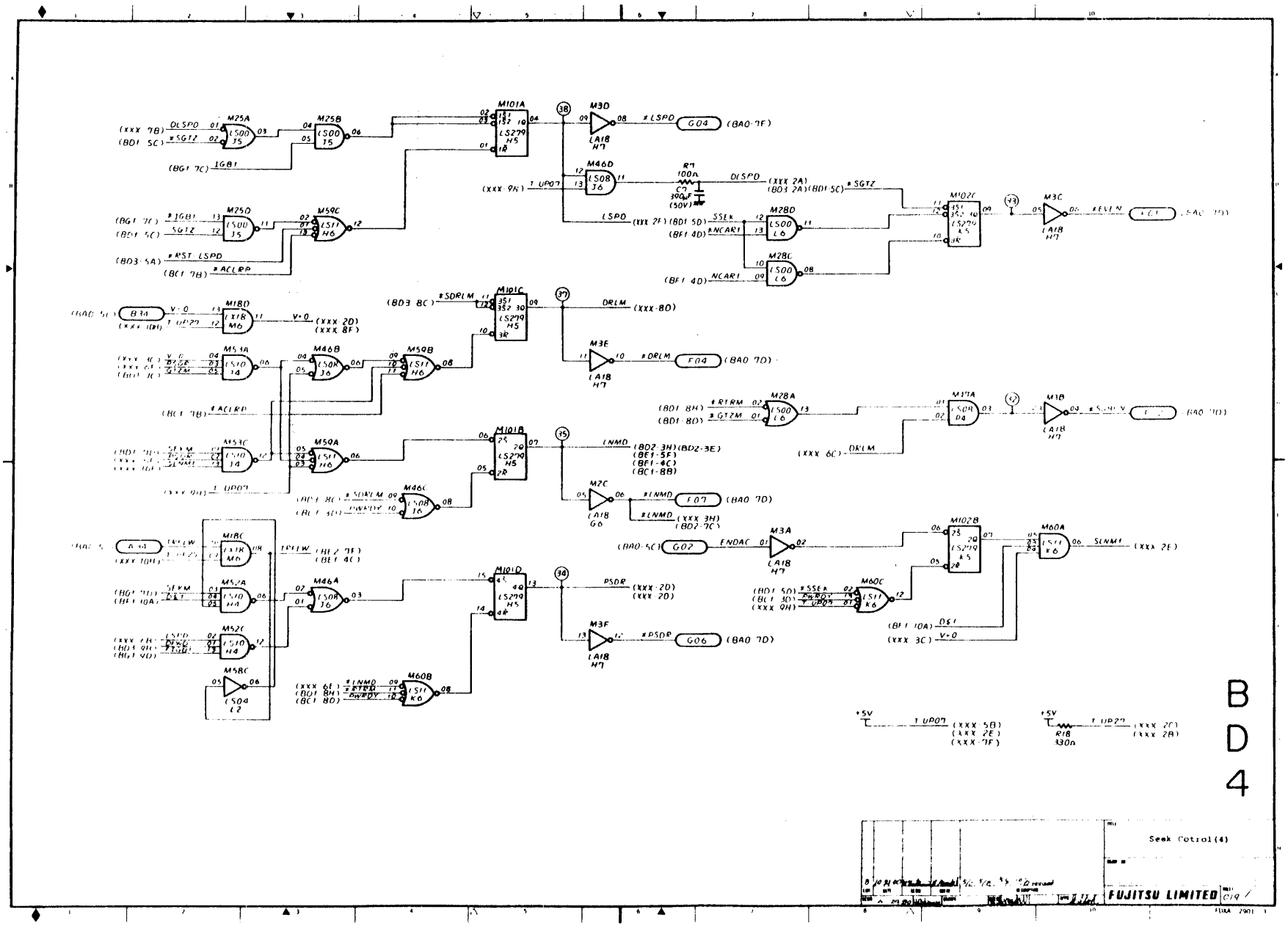

Head Address Reg.
Offset Control
FUJITSU LIMITED
B
I

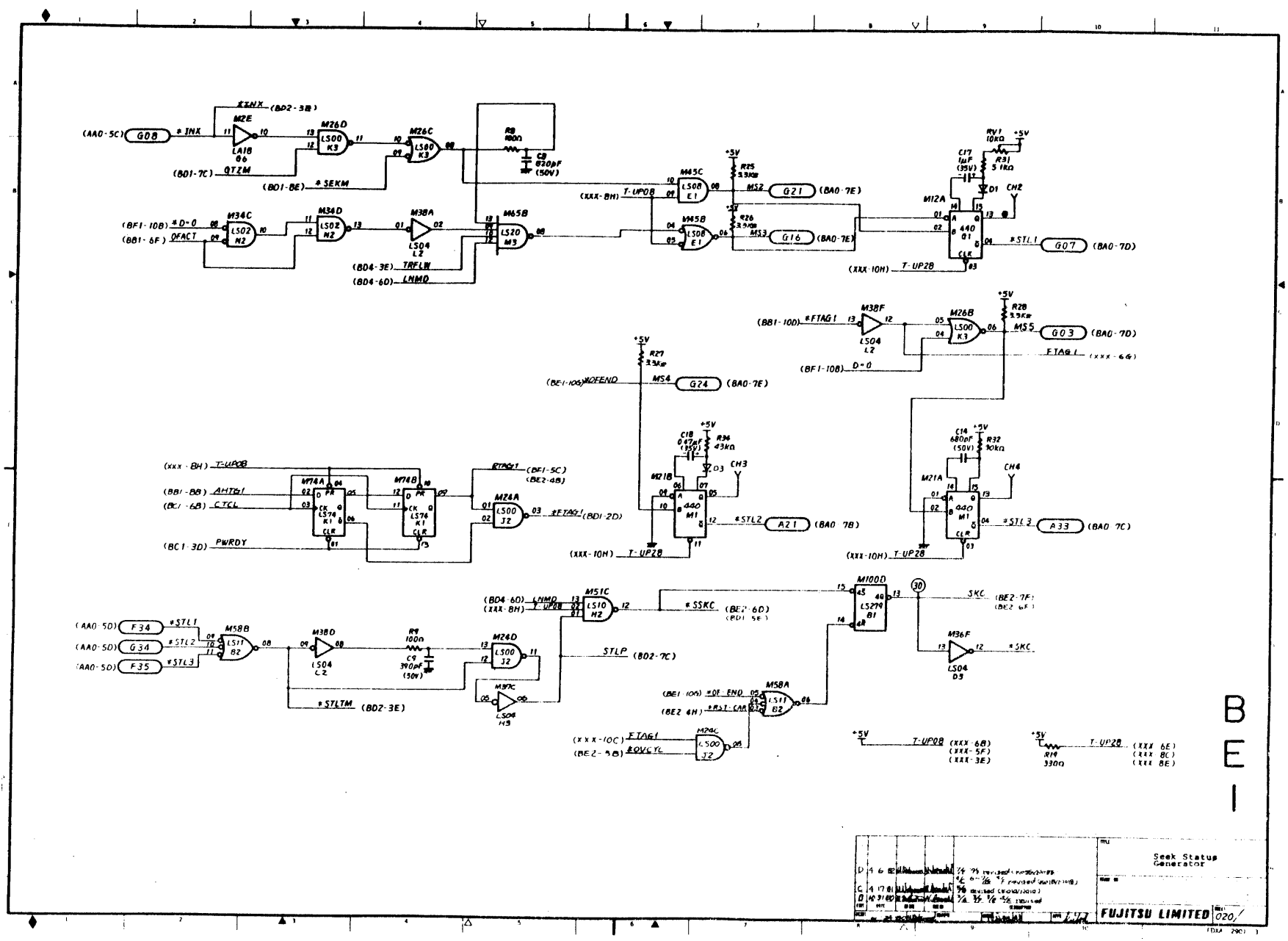

VFO/PLO Control
FUJITSU LIMITED
015
B
C
I

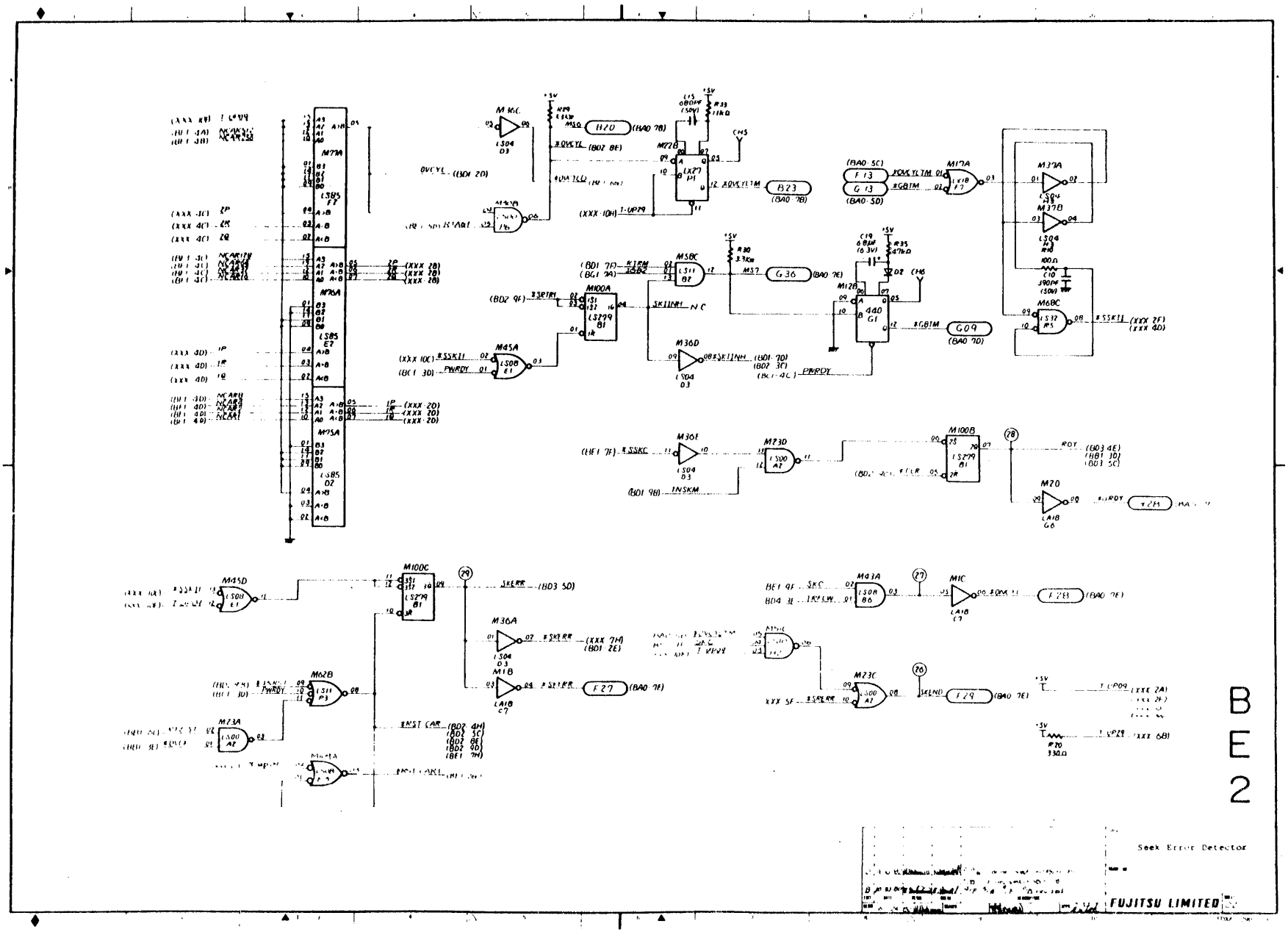

B D I
Seek Control(1)
FUJITSU LIMITED

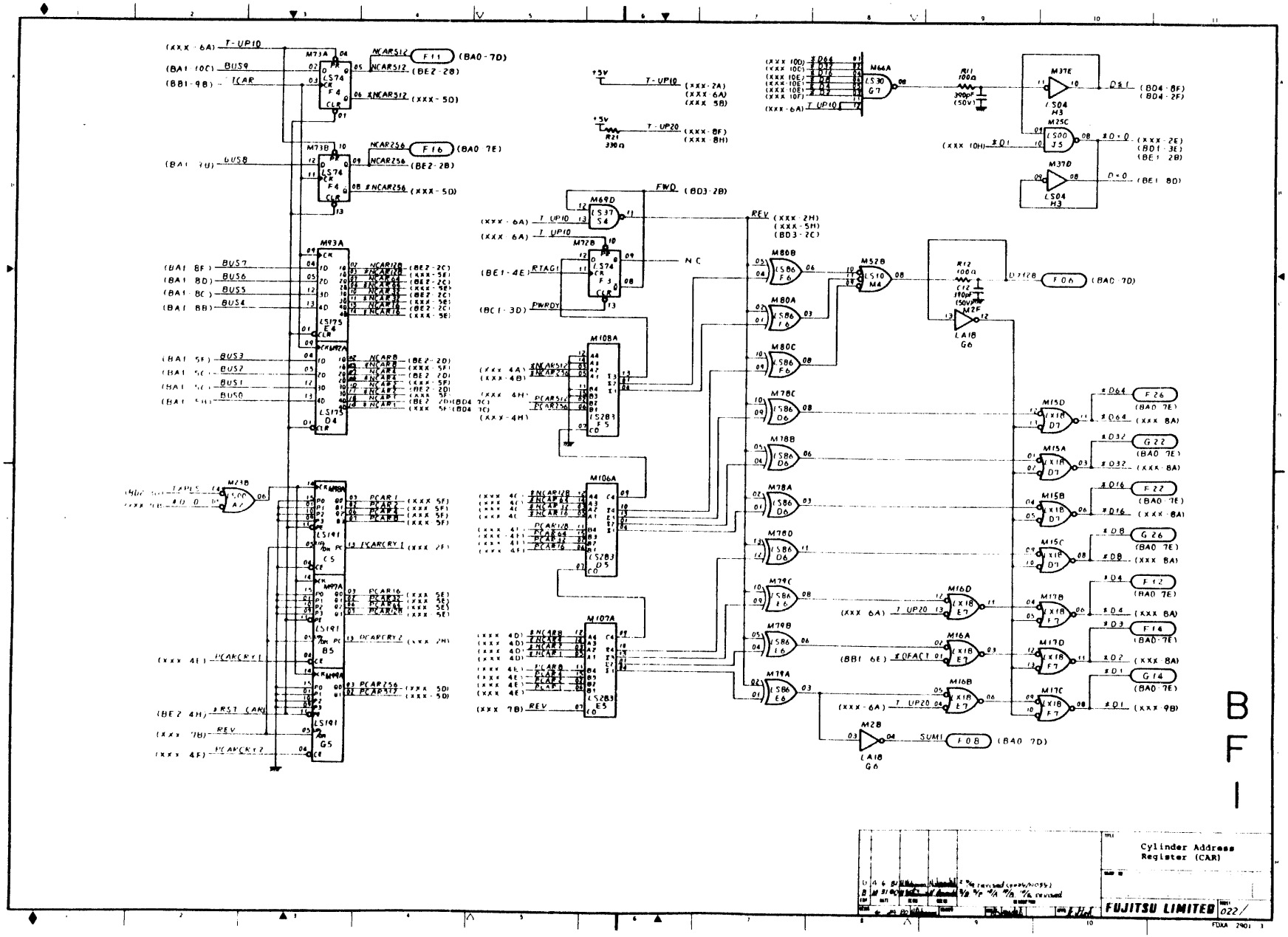

M48
LA18
L7
M90A
LS161
P2
COUNTER
M40F
LS04
A2
M47B
LS08
P4
M55C
LS10
Q2
M103C
LS279
L5
M10D
LX18
Q5
M40B
LS04
R2
M91A
LS161
R1
COUNTER
M31D
LS00
Q3
M32D
LS00
R4
M53B
LS10
J4
M54C
LS10
N4
M27A
LS00
L4
M103B
LS279
L5
M27D
LS00
L4
M103D
LS279
L5
M298
LS00
J2
M27C
LS00
L4
M103A
LS279
L5
M4A
LA18
L7
M47D
LS08
P4
M109B
LS08
E3
M54A
LS10
N4
M47C
LS40
P4
M104C
LS279
M5
M27B
LS00
L4
M104B
LS279
M5
M104D
LS279
M5
M61A
LS11
M4
M61B
LS11
M4
M61C
LS11
M4
R16
330Ω
B
D
2
Seek Control(2)
Seek Error Latch
FUJITSU LIMITED

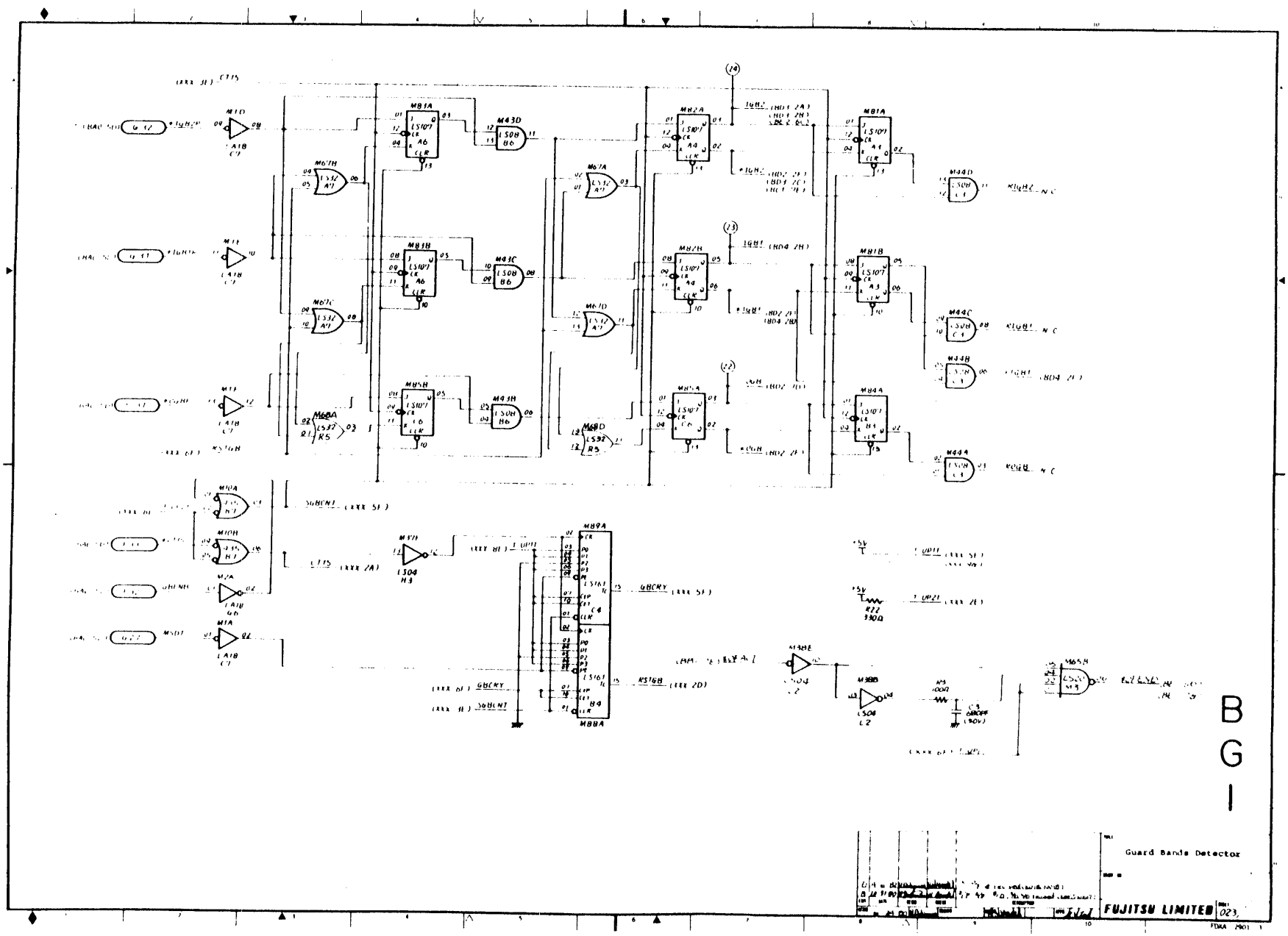

M55B
LS10 Q2
*RST (3PD) (BD4 7C)
M49C
LS08 T3
M102A
LS279 K5
FWDD N.C.
M18A
LX18 M6
FWDD
A30 (BA0 7C)
T UP26 (XXX 8F)
M70A
LS51 R3
M40E
LS04 R2
R6 100Ω
C6 390pF (50V)
M25B
LS00 L6
DFWD (BD4 2F)
DREVD (XXX 2A)
M55A
LS10 Q1
M31C
LS00 Q3
M18B
LX18 M6
*SDRLM
B30 (BA0 7C)
*OF ACT (BB1 6F)
*SDRLM (BD4 3E) (BD4 4C)
M31B
LS00 Q3
M49D
LS08 T3
M62A
LS11 P3
M70B
LS51 R3
M31A
LS00 Q3
*ACLRP (BC1 6B)
*SRTR3 (BD1 5F)
M29A
LS00 N5
M29B
LS00 N5
M54B
LS10 N4
M29D
LS00 N5
M39B
LS04 P5
M29C
LS00 N5
M39D
LS04 P5
M39F
LS04 P5
M39A
LS04 P5
M4C
LA18 L7
M8B
4 3 3 N6
M8A
4 3 3 N6
M8B
4 3 1 N7
M9A
4 3 3 N7
M8D
4 3 3 N6
M8C
4 3 3 N6
M9B
4 3 3 N7
M9C
4 3 3 N7
*LSTSG1 A26 (BA0 7C)
*LSTSG2 B26 (BA0 7C)
*LSTS0 A27 (BA0 7C)
*LSTS1 B27 (BA0 7C)
*LSTS2 A28 (BA0 7C)
*LSTS3 B28 (BA0 7C)
*LSTS4 A29 (BA0 7C)
*LSTS5 B29 (BA0 7C)
STS0 (BD2 6C)
STS1 (BD2 5F)
STS2 (BD2 5H)
STS3 (BD2 9D)
STS4 (BD2 9D)
STS5 (BD2 9E)
M14A
LX16 M7L
RDY (BE2 10D)
*UNSQ (BD1 10D)
*LRDY B32 (BA0 7C)
M14B
LX16 M7L
DVCK (BB1 4D)
T UP26 (XXX 8F)
*LDVCK B15 (BA0 7D)
M13A
LX16 M7U
*LFPT A35 (BA0 7D)
M4D
LA18 L7
*FPT A31 (BA0 7C)
M4E
LA18 L7
*IDIX (HA0 5C) H41
R23 330Ω
C16 0.047μF (50V)
+5V
T UP06 (XXX 2C) (XXX 2D)
R17 330Ω
T UP26 (XXX 4E) (XXX 8B) (XXX 9D)
B
D
3
Seek Control(3)
LED Drivers
FUJITSU LIMITED
FDAA 2901

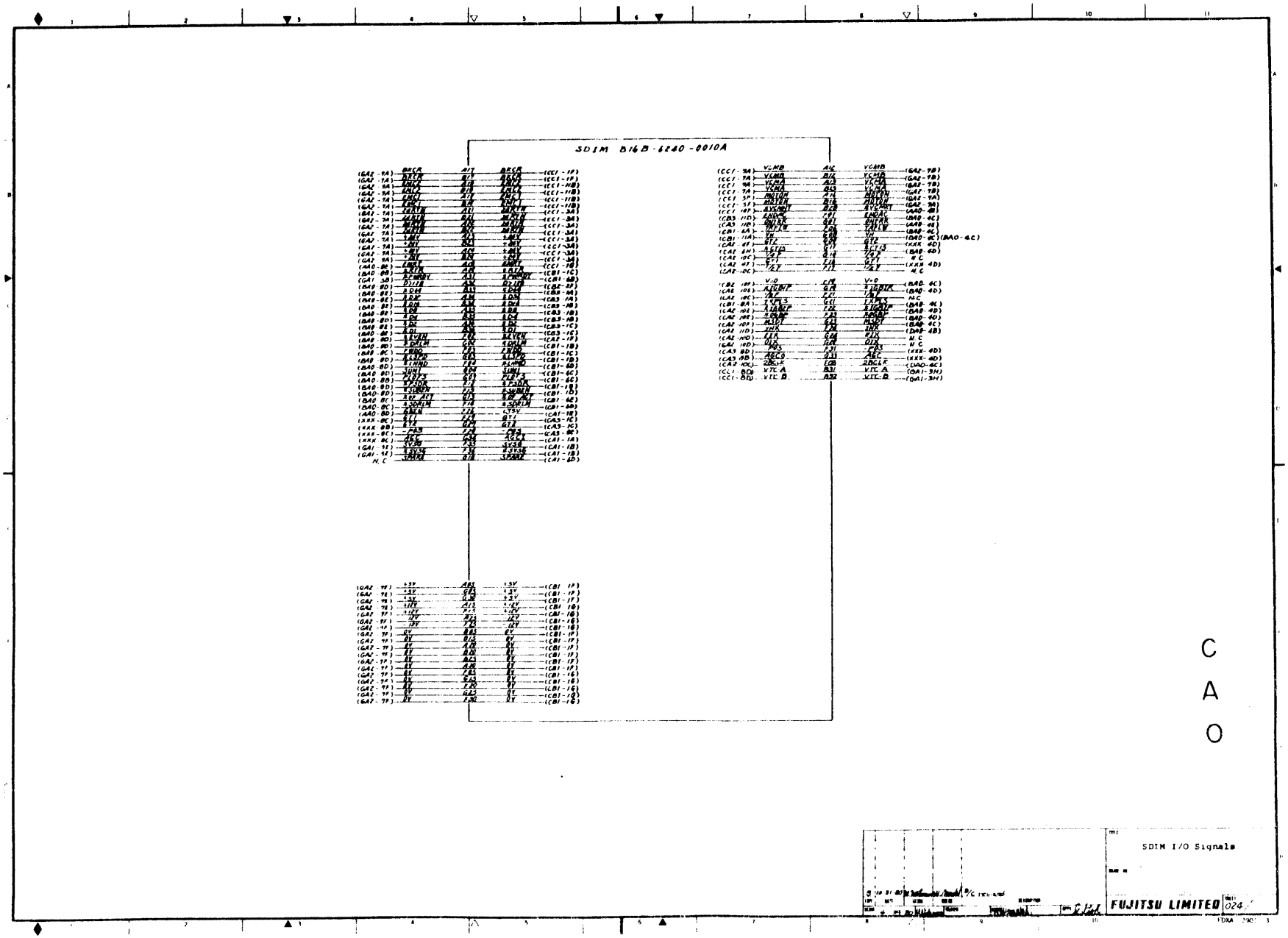

Seek Cotrol(4)
FUJITSU LIMITED
B
D
4

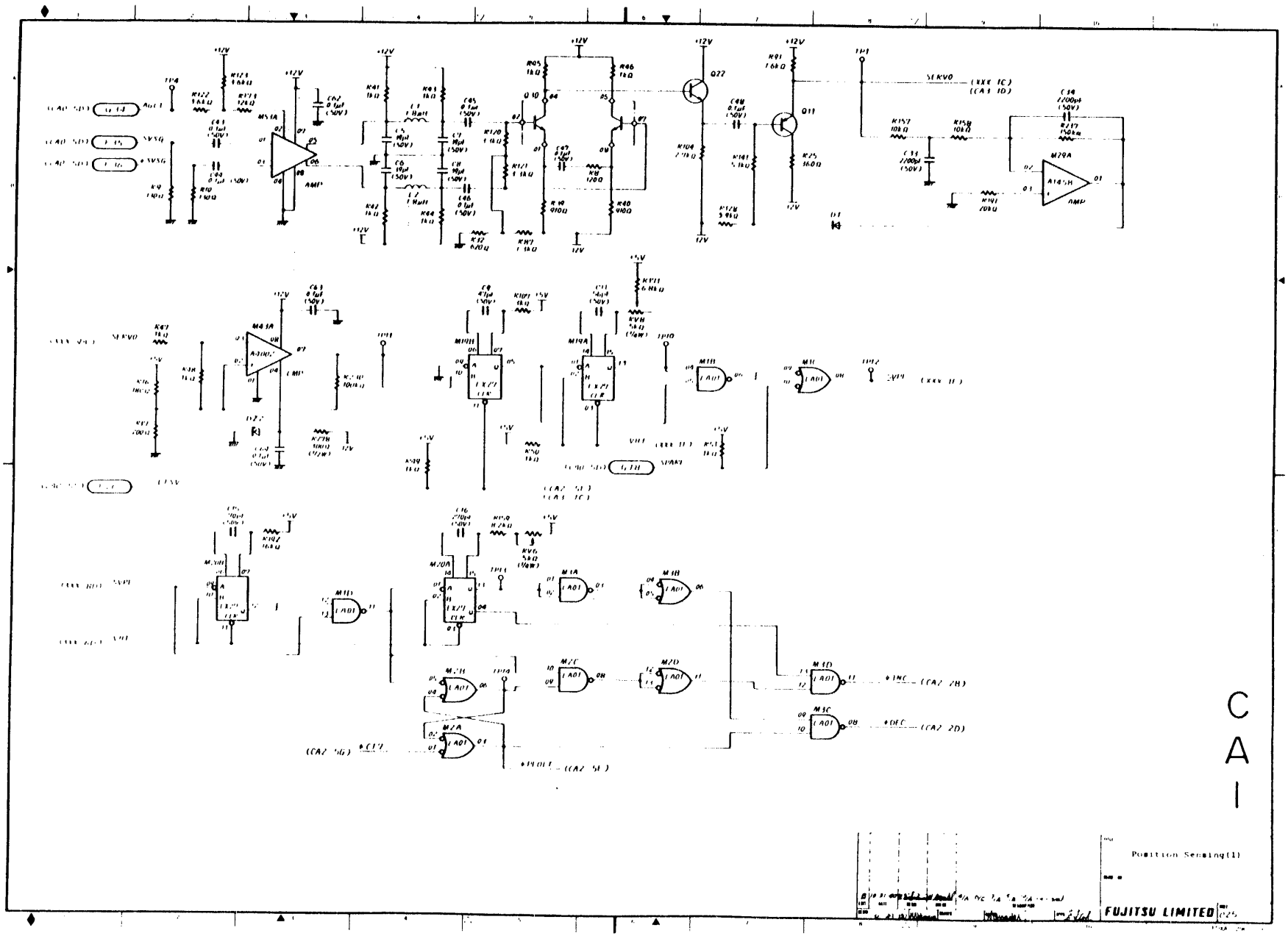

Seek Status Generator
FUJITSU LIMITED
B E I


B
E
2
Seek Error Detector
FUJITSU LIMITED

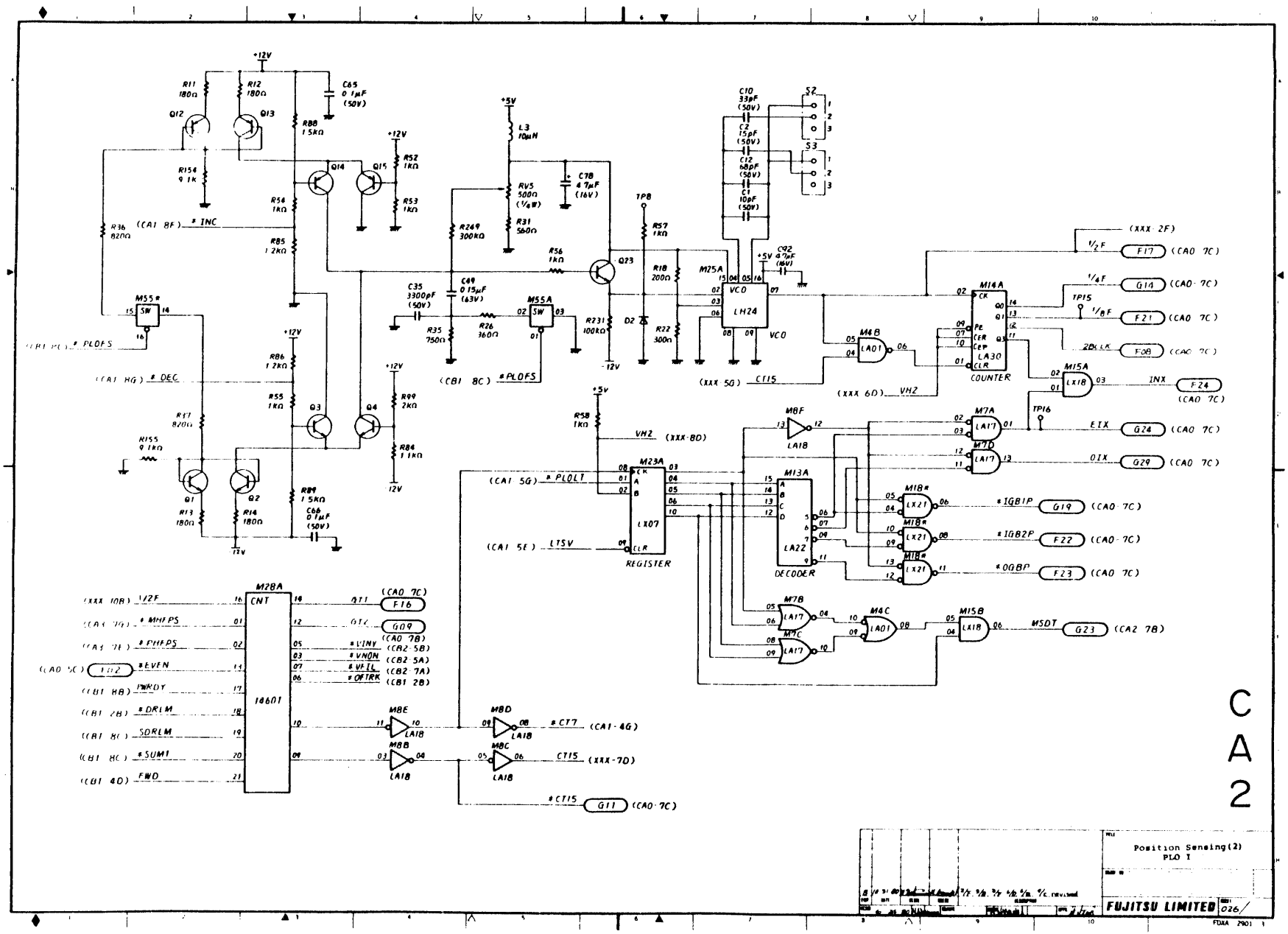

Cylinder Address Register (CAR)
FUJITSU LIMITED
B
F
I

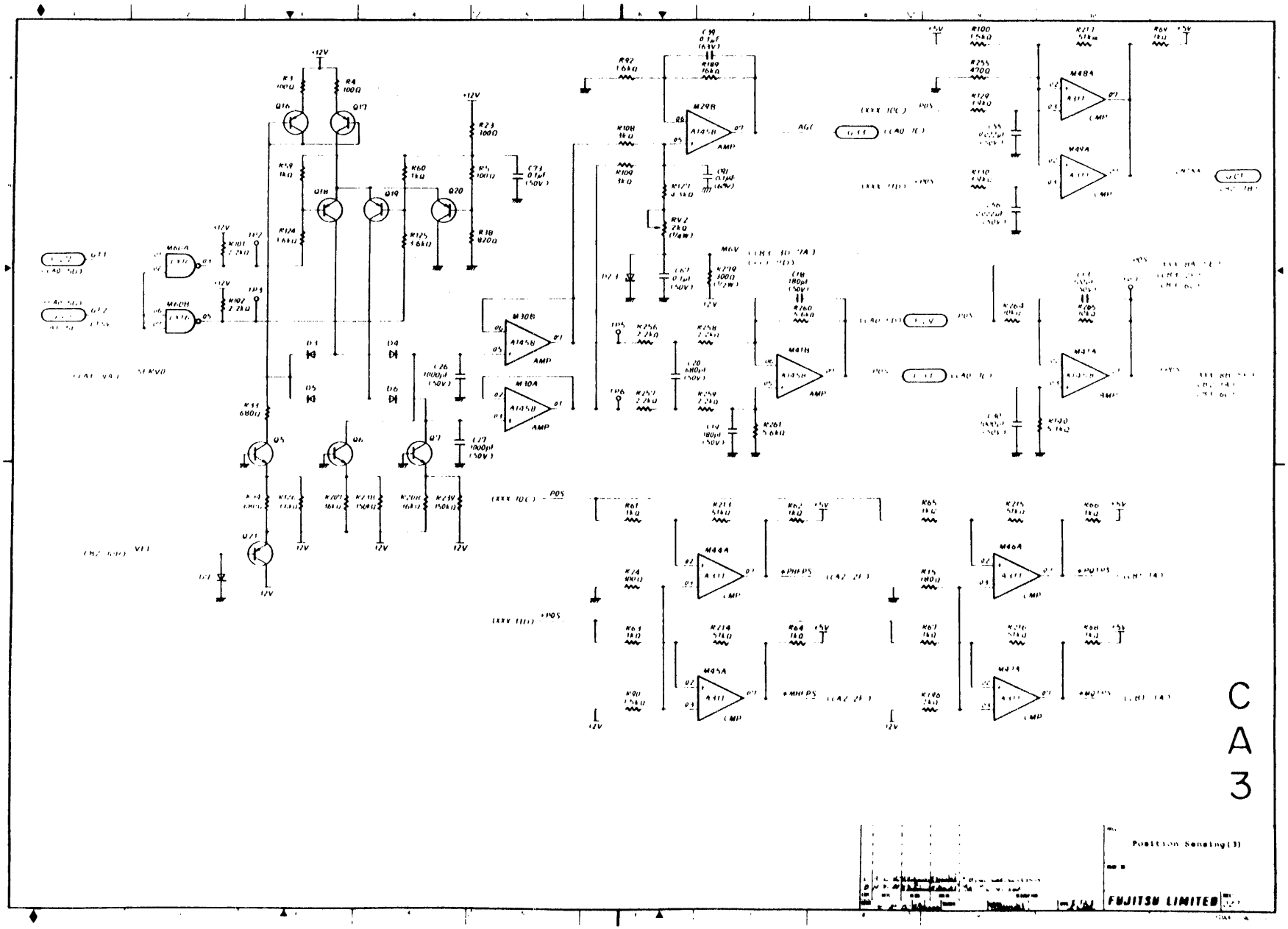

B
G
I
Guard Bands Detector
FUJITSU LIMITED

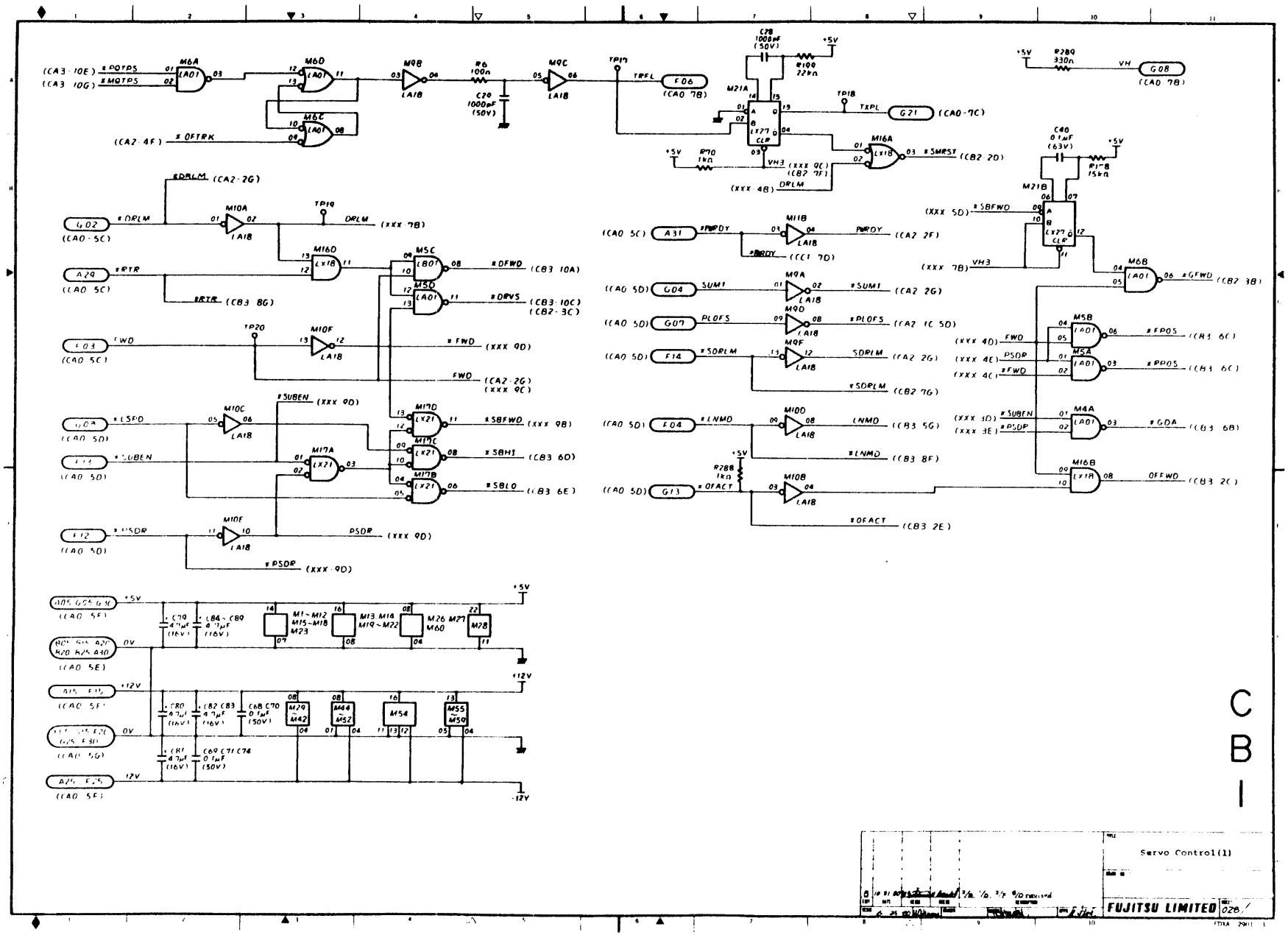

SDIM B16B-6240-0010A
C
A
O
SDIM I/O Signals
FUJITSU LIMITED

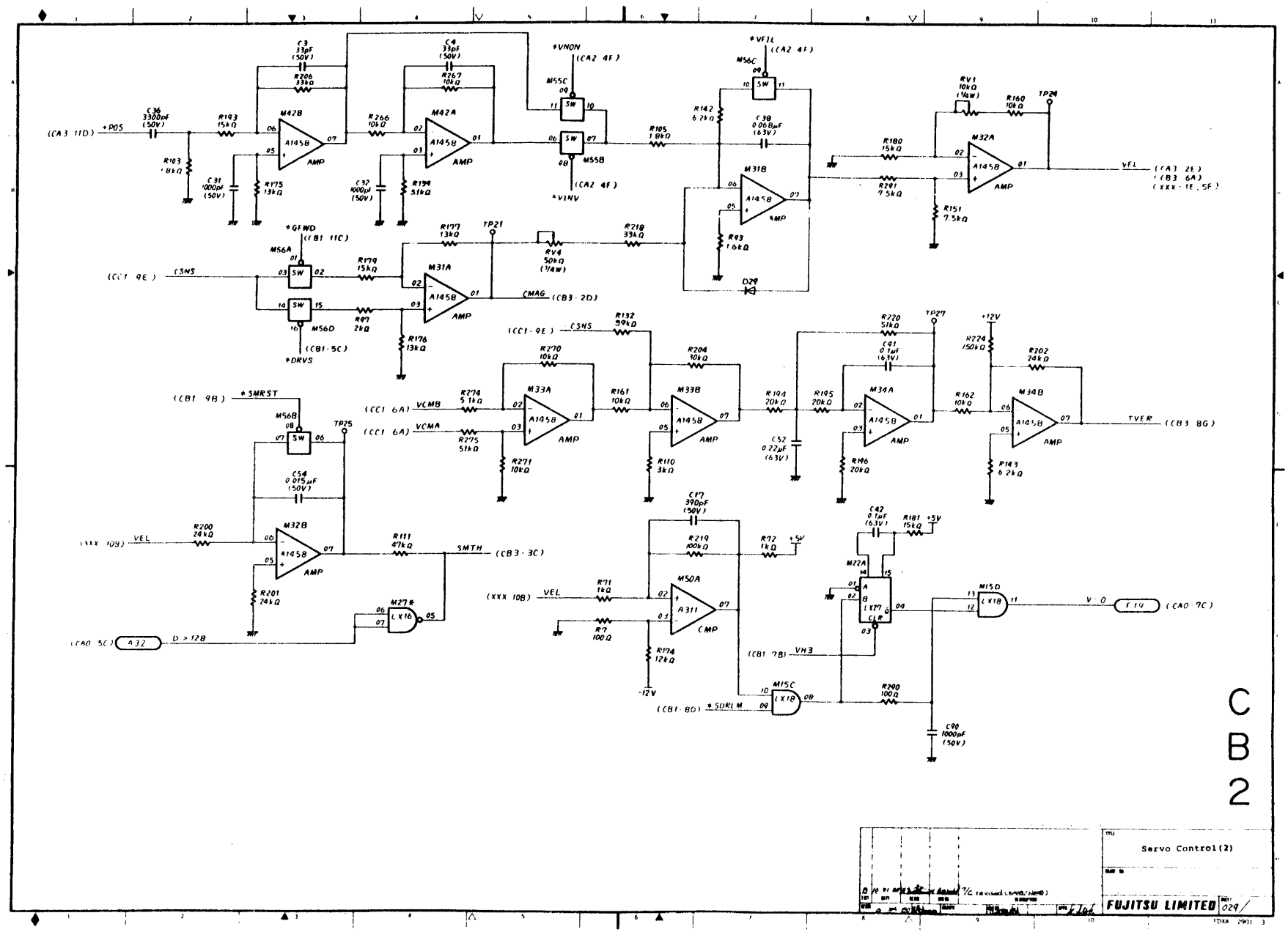


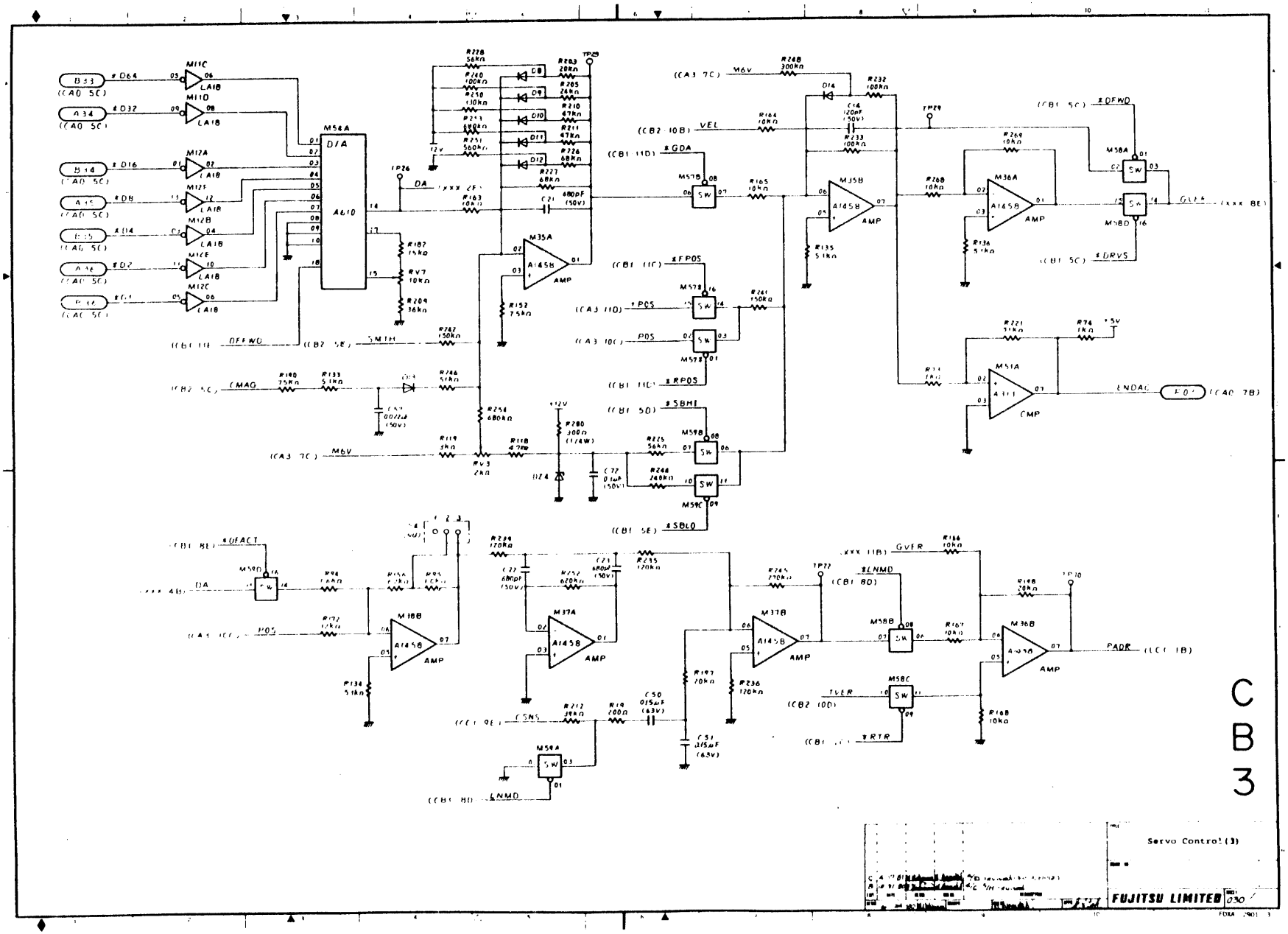
C A I

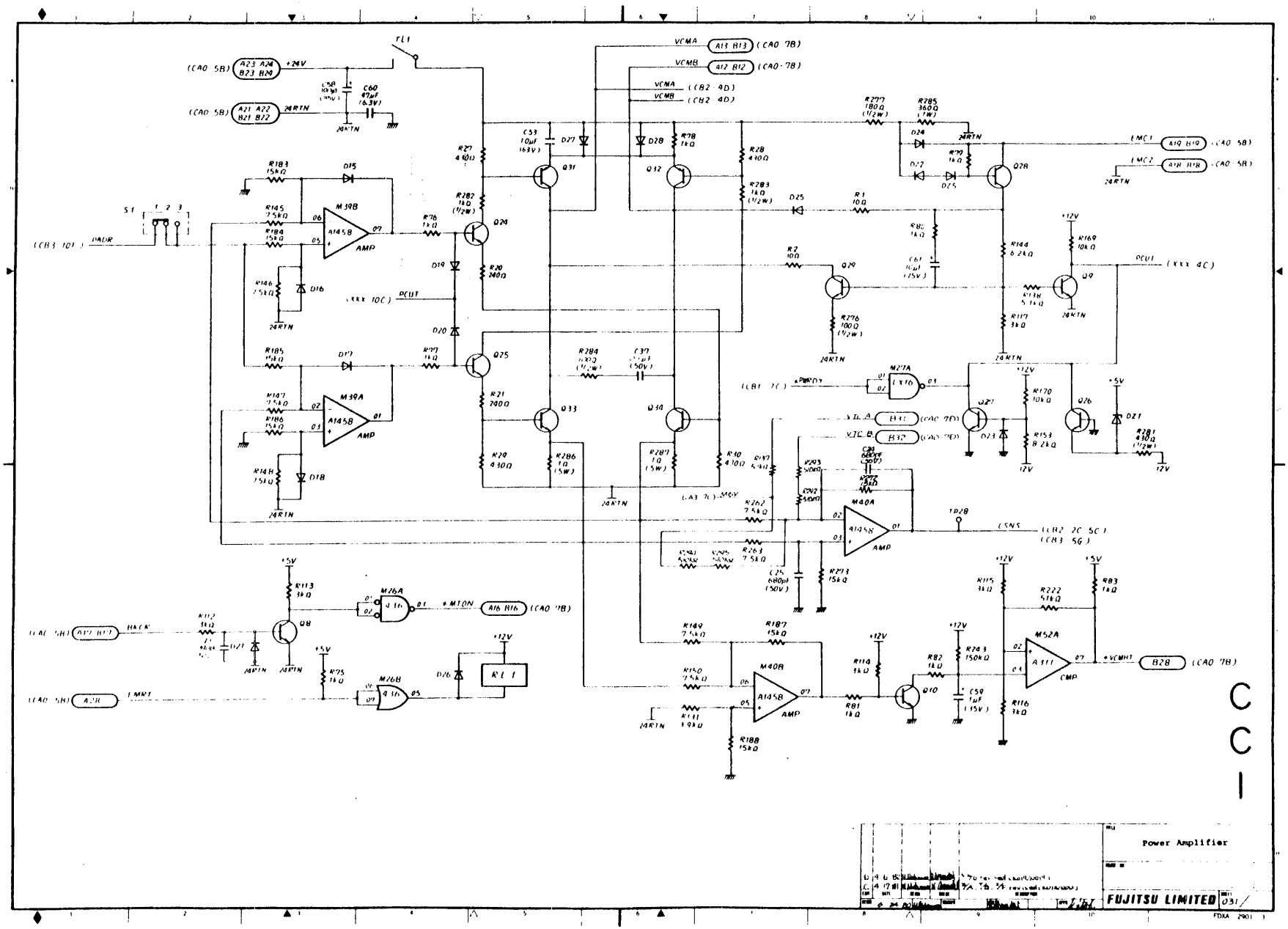

C A 2
Position Sensing(2)
PLO I
FUJITSU LIMITED
M28A
CNT
18601
LX07
REGISTER
LA22
DECODER
VCO
LH24
COUNTER
LA30
LA01
LA17
LA18
LX18
LX21
M55A
M55B
M23A
M13A
M25A
M14A
M15A
M15B
M18A
M18B
M18C
M4B
M4C
M7A
M7B
M7C
M7D
M8A
M8B
M8C
M8D
M8E
M8F
Q1
Q2
Q3
Q4
Q12
Q13
Q14
Q15
Q23
D2
S2
S3
TP8
TP15
TP16
L3
10μH
RV5
500Ω
(1/4W)
R31
560Ω
C78
4.7μF
(16V)
C49
0.15μF
(63V)
C35
3300pF
(50V)
C65
0.1μF
(50V)
C66
0.1μF
(50V)
C10
33pF
(50V)
C2
15pF
(50V)
C12
68pF
(50V)
C1
10pF
(50V)
C92
4.7μF
(16V)
R11
180Ω
R12
180Ω
R13
180Ω
R14
180Ω
R88
1.5kΩ
R89
1.5kΩ
R52
1kΩ
R53
1kΩ
R56
1kΩ
R85
1.2kΩ
R86
1.2kΩ
R55
1kΩ
R99
2kΩ
R84
1.1kΩ
R154
9.1k
R155
9.1kΩ
R17
820Ω
R36
820Ω
R249
300kΩ
R35
750Ω
R26
360Ω
R231
100kΩ
R22
300Ω
R18
200Ω
R57
1kΩ
R58
1kΩ
+12V
+5V
-12V
(CA1 8F) *INC
(CB1 8F) *PLOFS
(CA1 HG) *DEC
(CB1 8C) *PLOFS
(CA1 5G) *PLOLT
(CA1 5E) LTSV
(XXX 5G) CT15
(XXX 6D) VH2
(XXX 8D) VH2
(XXX 2F)
(XXX 10B) 1/2F
(CA0 7C) 1/2F
(CA0 7C) 1/4F
(CA0 7C) 1/8F
(CA0 7C) 2BCLK
(CA0 7C) INX
(CA0 7C) EIX
(CA0 7C) OIX
(CA0 7C) *IGB1P
(CA0 7C) *IGB2P
(CA0 7C) *OGBP
(CA2 7B) MSDT
(CA1 4G) *CT7
(XXX 7D) CT15
(CA0 7C) *CT15
(CA0 7C) 1/2
(CA0 7C) *MHPS
(CA0 7B) *PHPS
(CA0 5C) *EVEN
(CB1 8B) PWRDY
(CB1 2B) *DRLM
(CB1 8C) SDRLM
(CB1 8C) *SUM1
(CB1 4D) FWD
(CA0 7C) QT1
(CA0 7B) QTC
(CB2 5B) *VINV
(CB2 5A) *VNON
(CB2 7A) *VFIL
(CB1 2B) *OFTRK
F17
G14
F21
F08
F24
G24
G29
G19
F22
F23
G23
G09
F16
G11

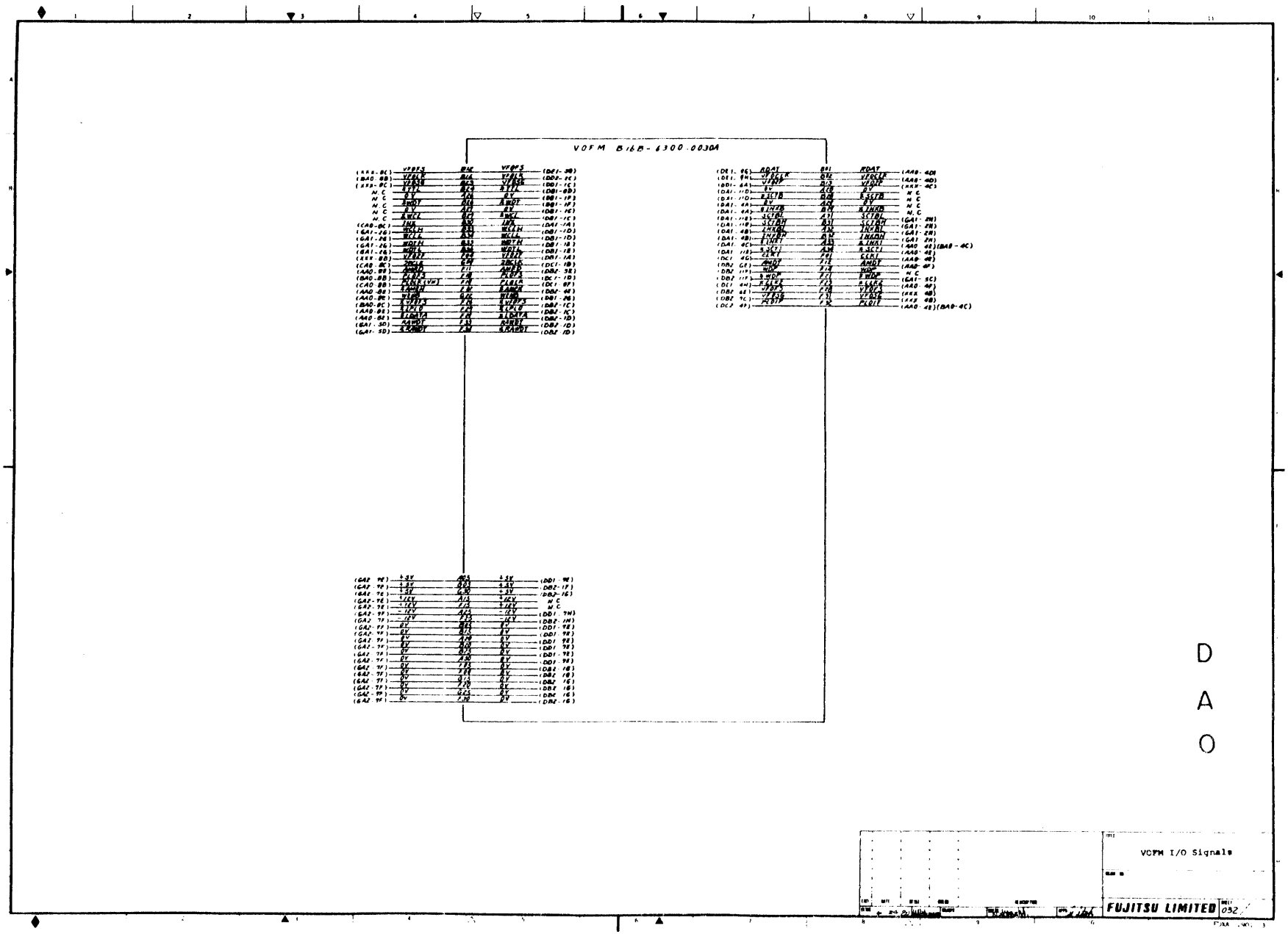

C
A
3
Position Sensing(3)
FUJITSU LIMITED

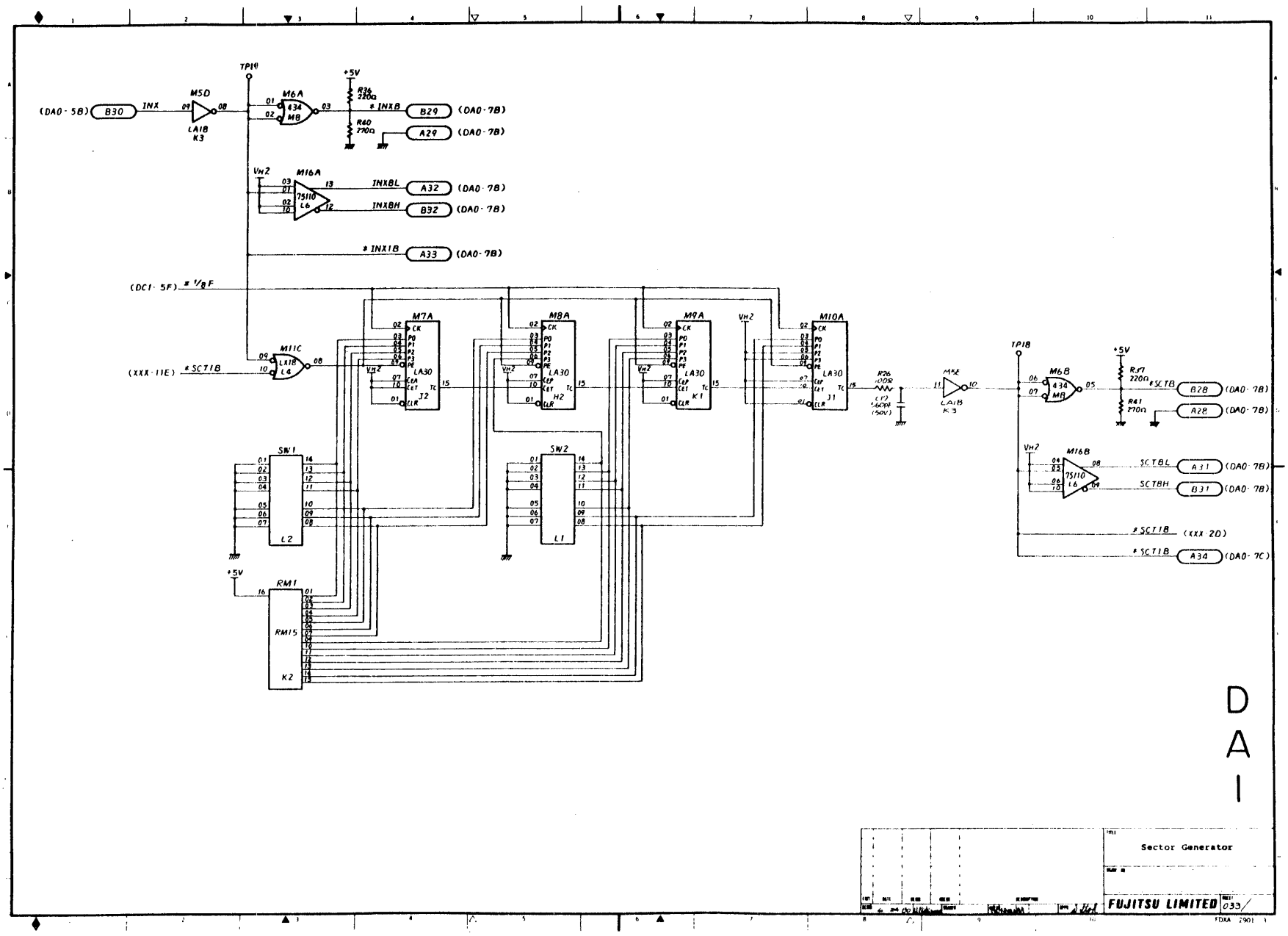

Servo Control(1)
FUJITSU LIMITED
C B I

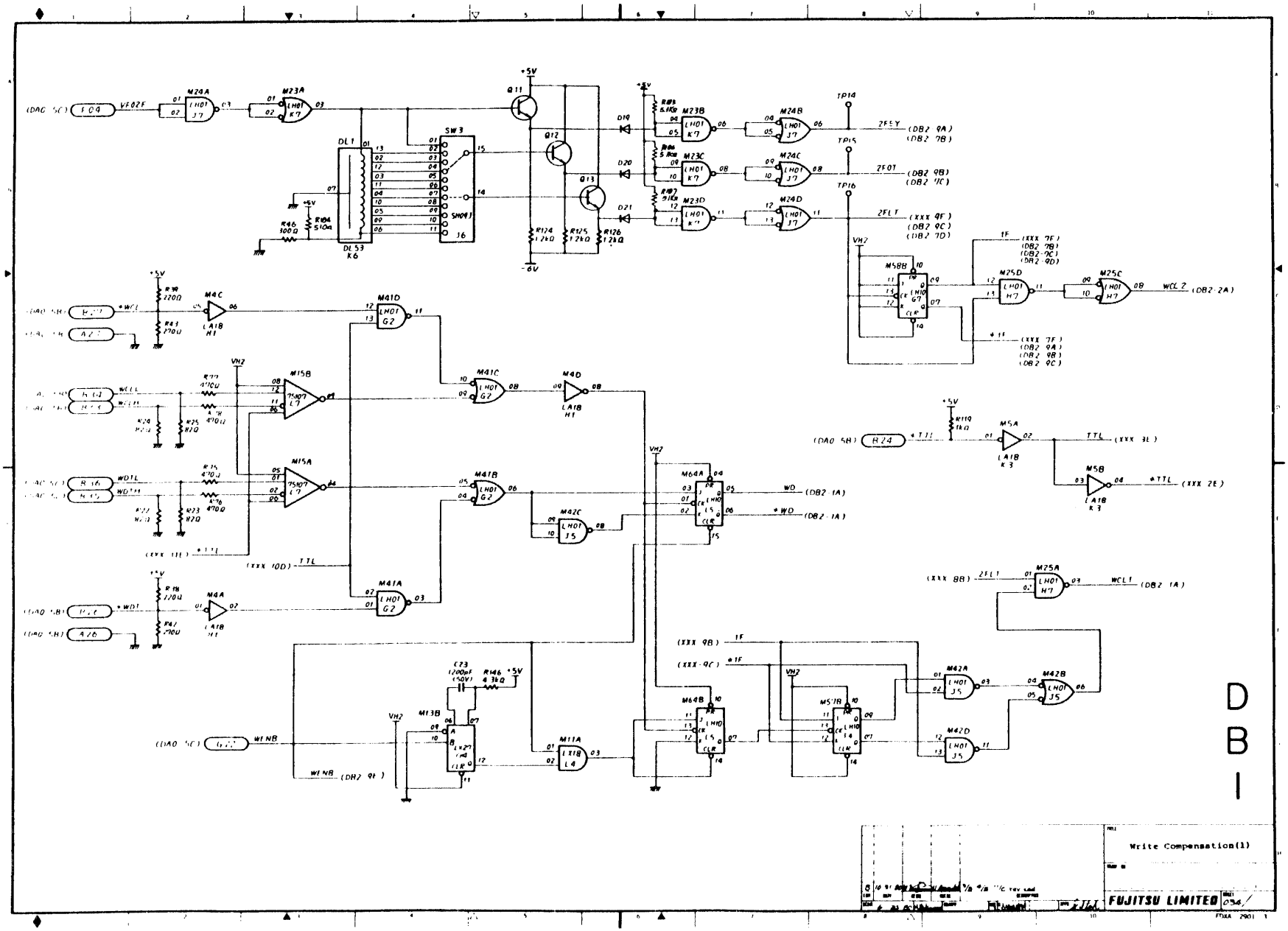

C3 33pF (50V)
C4 33pF (50V)
R206 33kΩ
R267 10kΩ
*VNON
(CA2 4F)
*VFIL
(CA2 4F)
M56C
M55C
M55B
(CA2 4F)
*VINV
C36 3300pF (50V)
R193 15kΩ
M42B
M42A
A1458
AMP
R266 10kΩ
R105 1.8kΩ
R142 6.2kΩ
C38 0.068μF (63V)
M31B
R180 15kΩ
R291 7.5kΩ
M32A
RV1 10kΩ (1/4W)
R160 10kΩ
TP24
R151 7.5kΩ
VEL
(CA3 2L)
(CB3 6A)
(XXX-1E, 5F)
(CA3 11D) +POS
R103 1.8kΩ
C31 1000pF (50V)
R175 13kΩ
C32 1000pF (50V)
R194 51kΩ
*GFWD
(CB1 11C)
M56A
M56B
(CB1 5C)
*DRVS
(CC1 9E) CSNS
R179 15kΩ
R97 2kΩ
R176 13kΩ
M31A
R177 13kΩ
TP21
RV4 50kΩ (1/4W)
R218 33kΩ
R93 1.6kΩ
D29
CMAG
(CB3 2D)
(CB1 9B) *SMRST
TP25
(CC1 6A) VCMB
(CC1 6A) VCMA
R274 5.1kΩ
R275 51kΩ
M33A
R270 10kΩ
R271 10kΩ
R161 10kΩ
R132 59kΩ
R204 10kΩ
M33B
R110 3kΩ
R194 20kΩ
R195 20kΩ
C52 0.22μF (63V)
R220 51kΩ
C41 0.1μF (63V)
TP27
+12V
R224 150kΩ
R202 24kΩ
M34A
M34B
R146 20kΩ
R143 6.2kΩ
R162 10kΩ
TVER
(CB3 8G)
C54 0.015μF (50V)
(XXX 10B) VEL
R200 24kΩ
M32B
R201 24kΩ
R111 47kΩ
SMTH
(CB3 3C)
(CA0 5C) A32 D>128
M27B
C17 390pF (50V)
R219 100kΩ
R72 1kΩ +5V
C42 0.1μF (63V)
R181 15kΩ +5V
M22A
M15D
V:0
F14
(CA0 7C)
(XXX 10B) VEL
R71 1kΩ
R7 100Ω
M50A
A311
CMP
R174 12kΩ
-12V
(CB1 7B) VH3
(CB1 8D) *SORLM
M15C
R200 100Ω
C90 1000pF (50V)
C
B
2
Servo Control(2)
FUJITSU LIMITED
029/

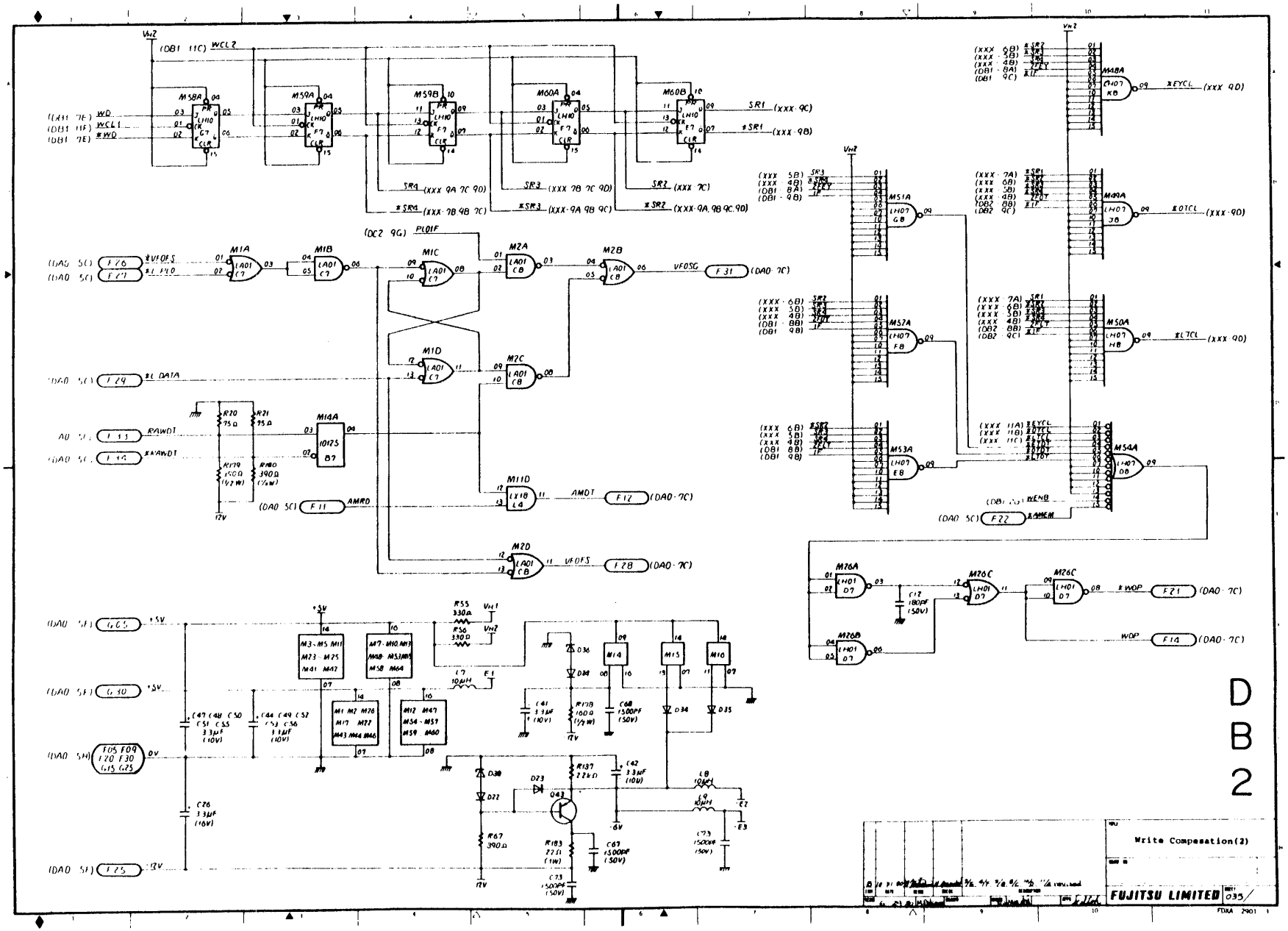

C B 3
Servo Control (3)
FUJITSU LIMITED
M58A D/A
A610
M35A
M35B
M36A
M36B
M37A
M37B
M18B
M51A
AMP
CMP
DA
VEL
GDA
FPOS
POS
RPOS
SBHI
SBLO
DFWD
DRVS
GVER
ENDAC
PADR
TVER
RTR
LNMD
SNS
CMAG
OFACT
SMTH
M6V
+12V
+5V

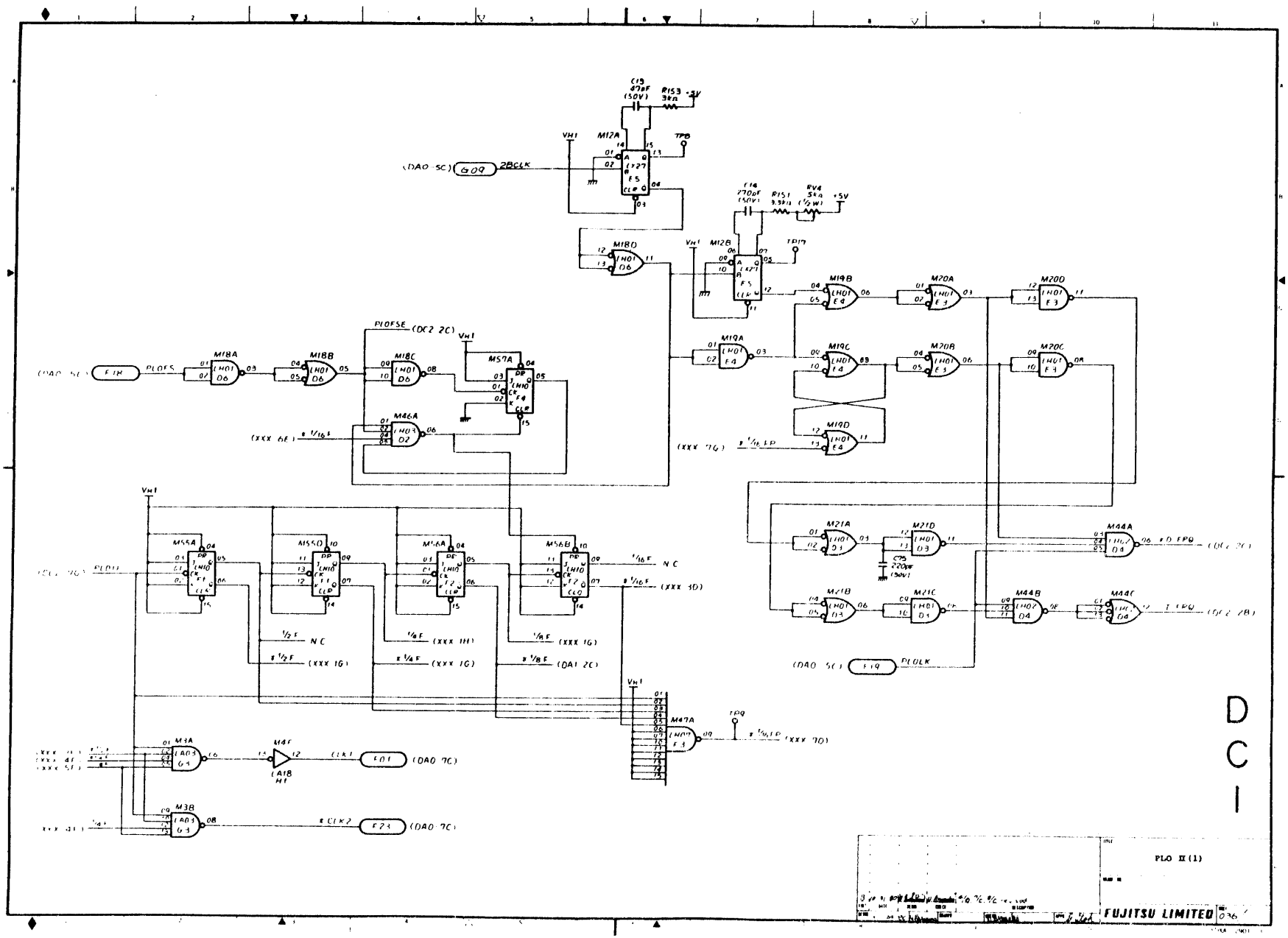

Power Amplifier
FUJITSU LIMITED
C C I

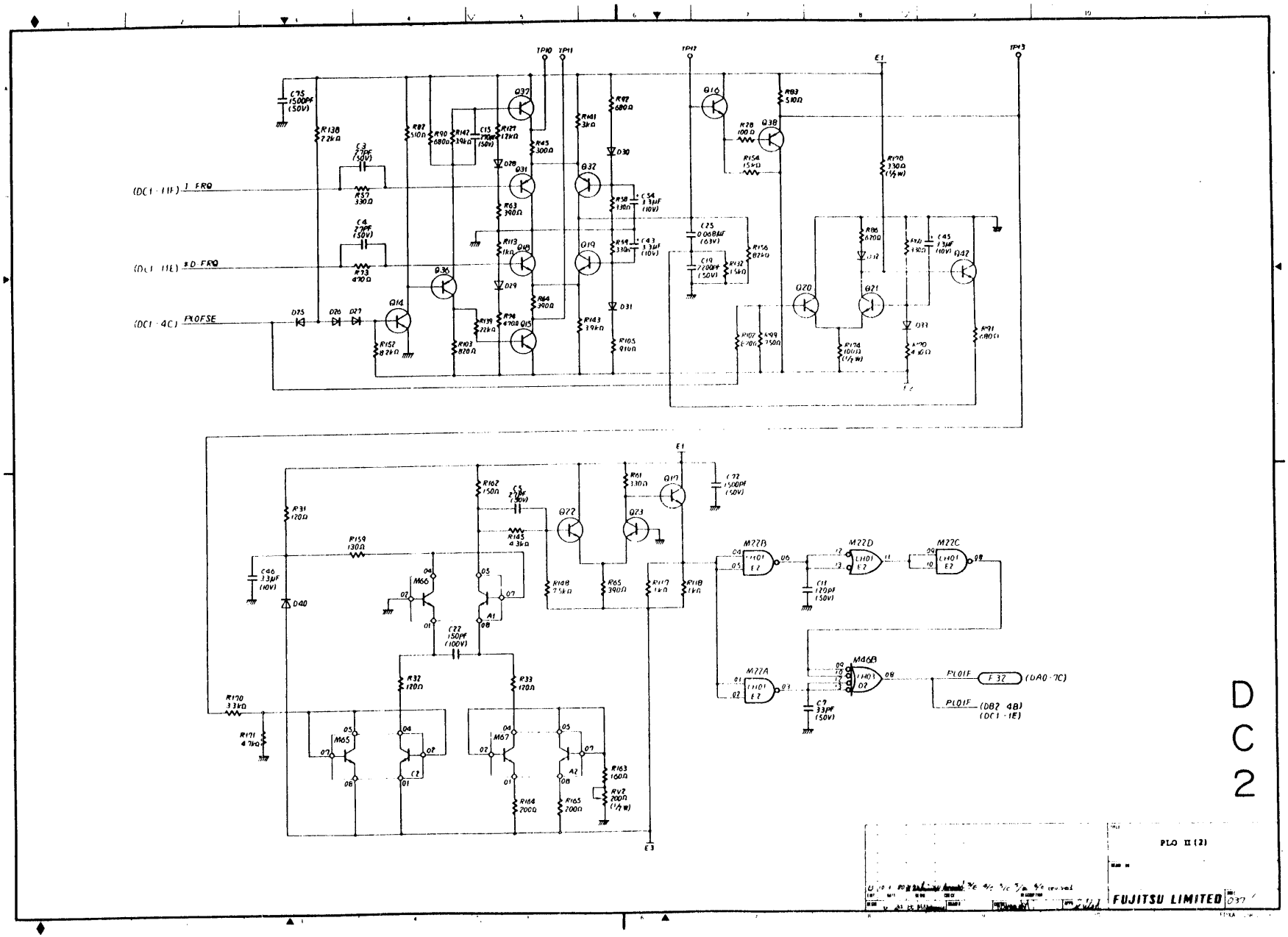

VOFM B16B-6300-0030A
D
A
O
VOFM I/O Signals
FUJITSU LIMITED

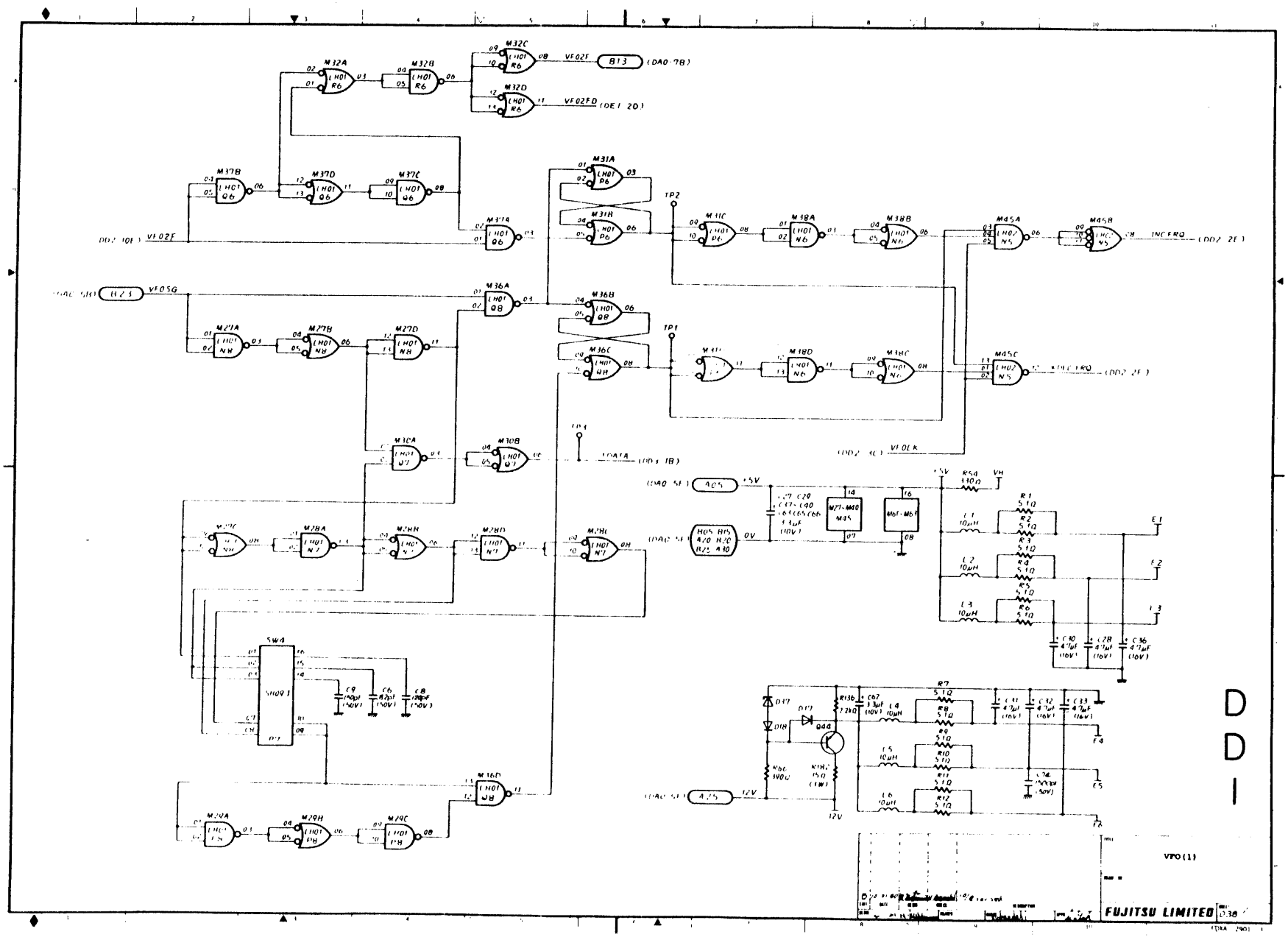

Sector Generator
FUJITSU LIMITED
D
A
I

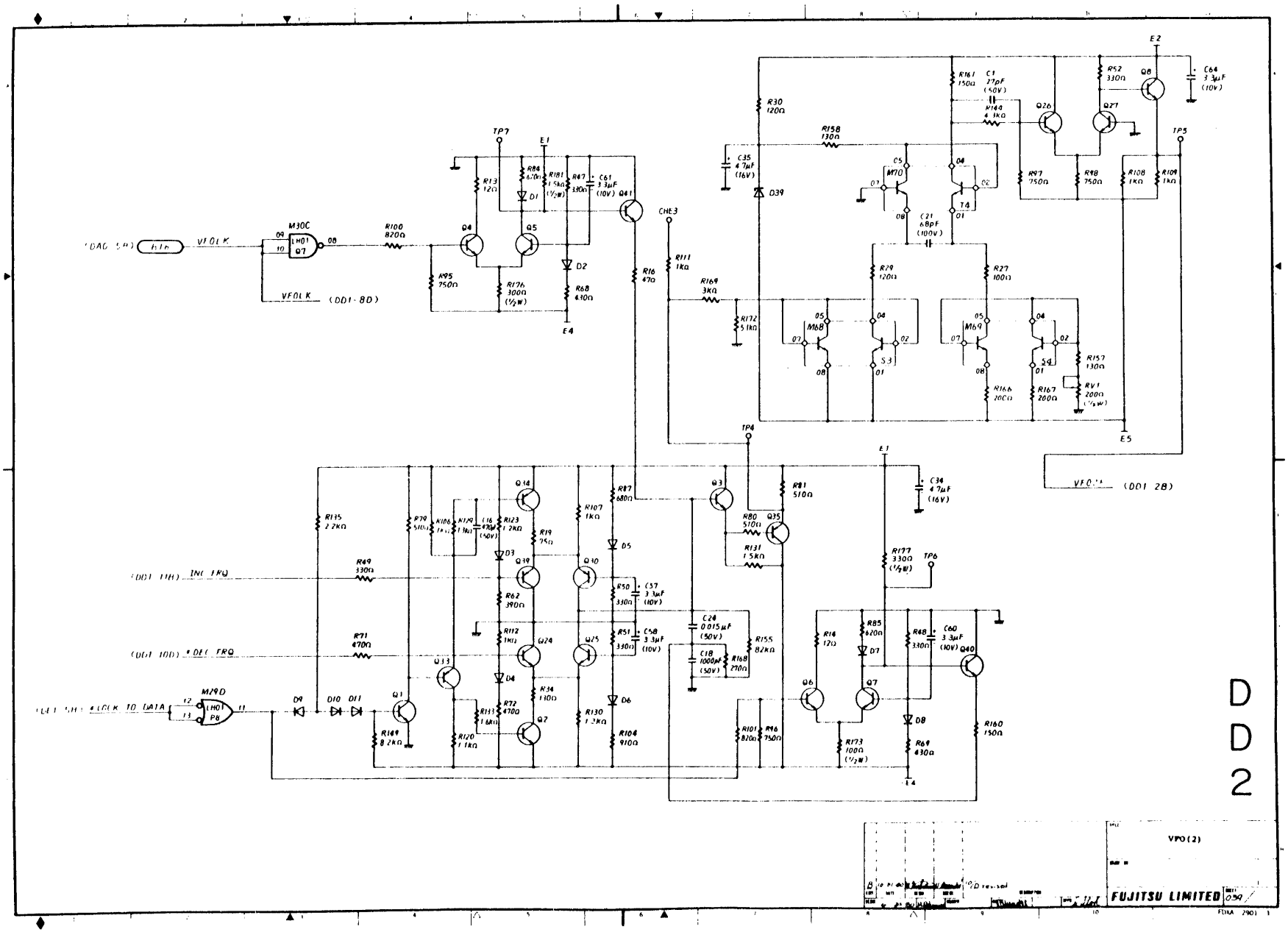

Write Compensation(1)
FUJITSU LIMITED
D
B
I

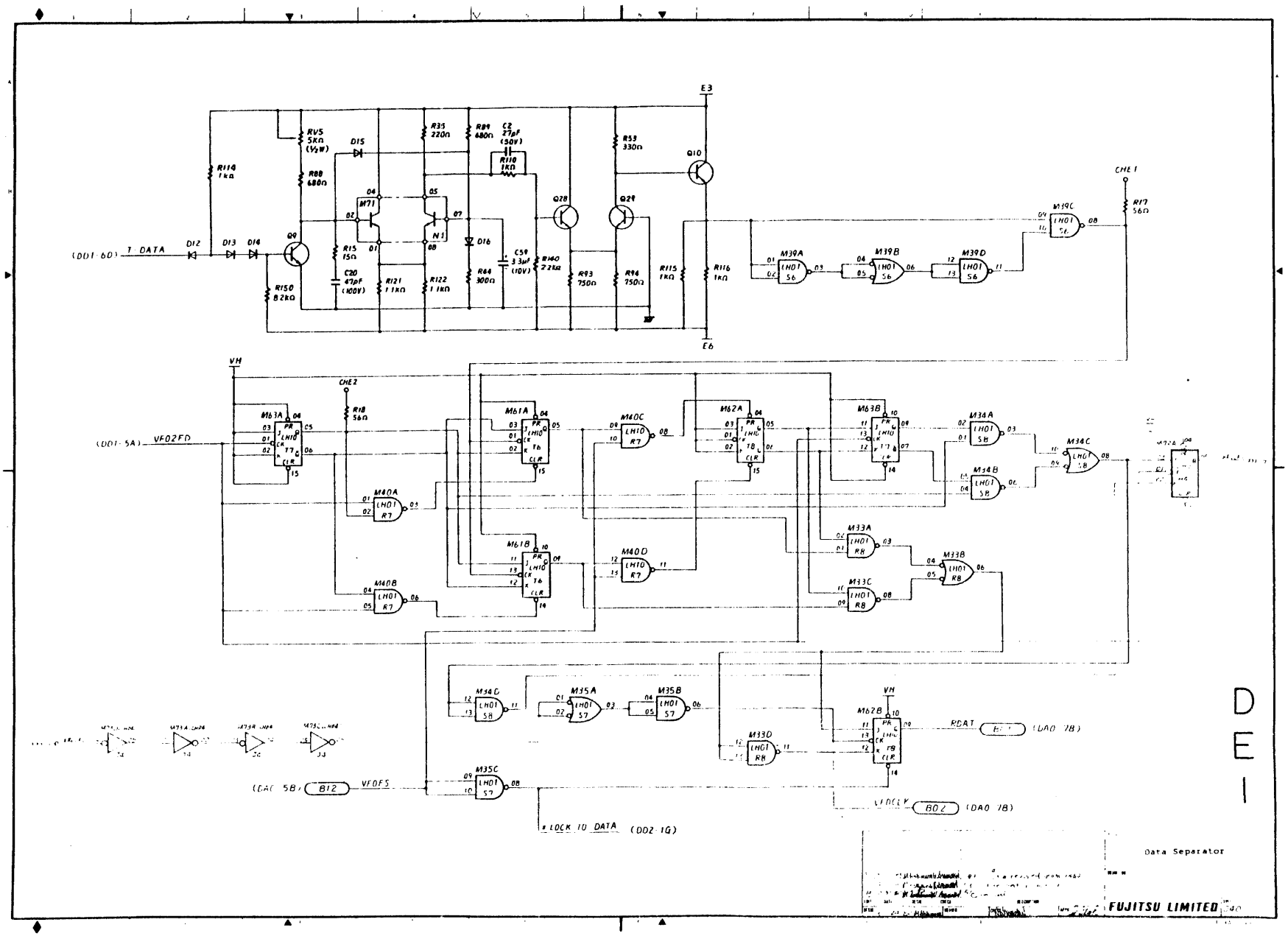

WCL2
WCL1
*WD
SR1 (XXX·9C)
*SR1 (XXX·9B)
SR4 (XXX·9A 7C 9D)
*SR4 (XXX·7B 9B 7C)
SR3 (XXX 7B 7C 9D)
*SR3 (XXX·9A 9B 9C)
SR2 (XXX 7C)
*SR2 (XXX·9A, 9B 9C.9D)
PLOIF
VFOSG
AMRD
AMOT
VFOFS
RAWDT
*RAWDT
*EL DATA
*EYCL (XXX 9D)
*OTCL (XXX·9D)
*ELTCL (XXX 9D)
WENB
*AMEM
WOP
*WOP
Write Compesation(2)
FUJITSU LIMITED
D B 2

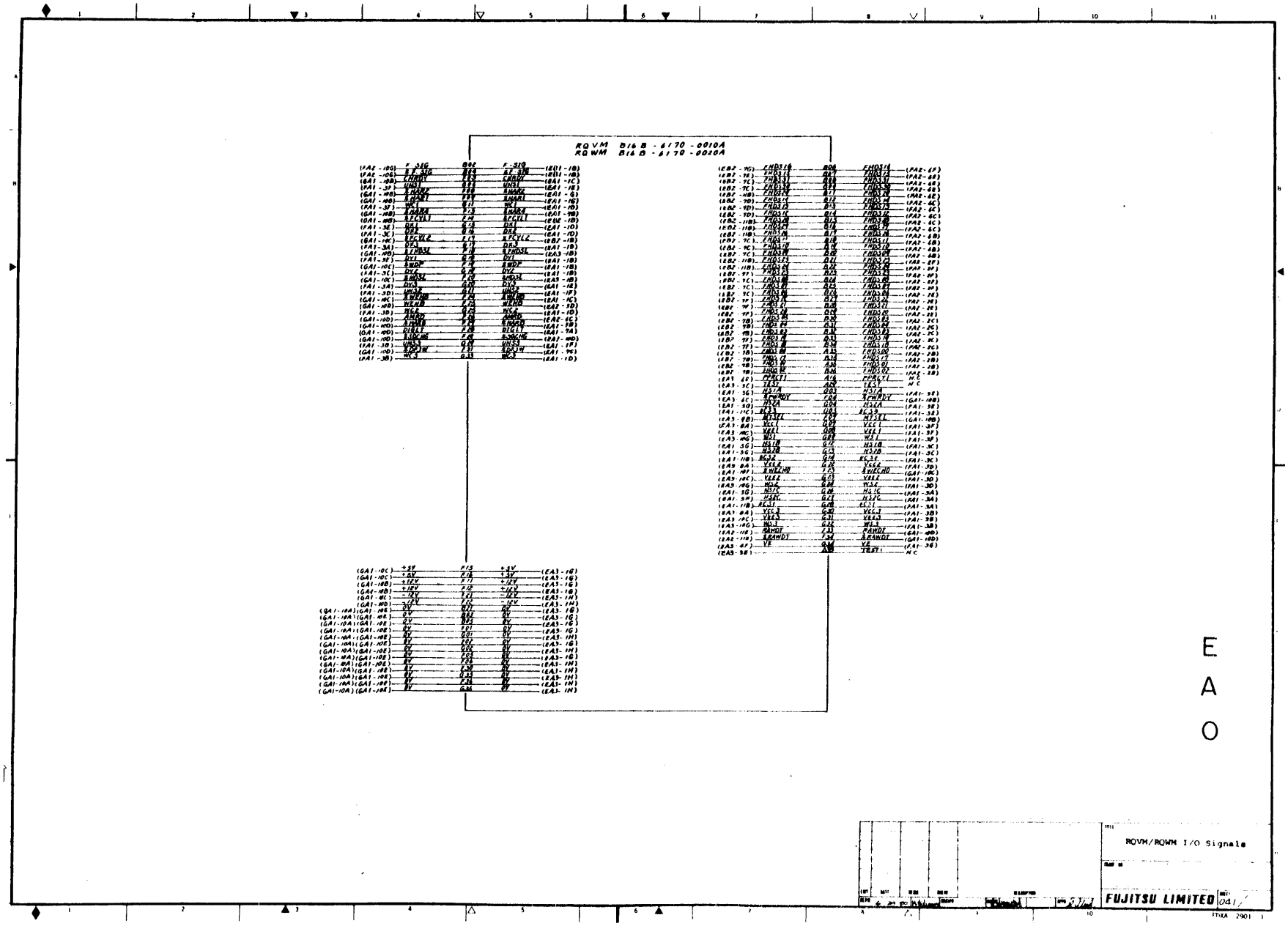

PLO II (1)
FUJITSU LIMITED
D
C
I

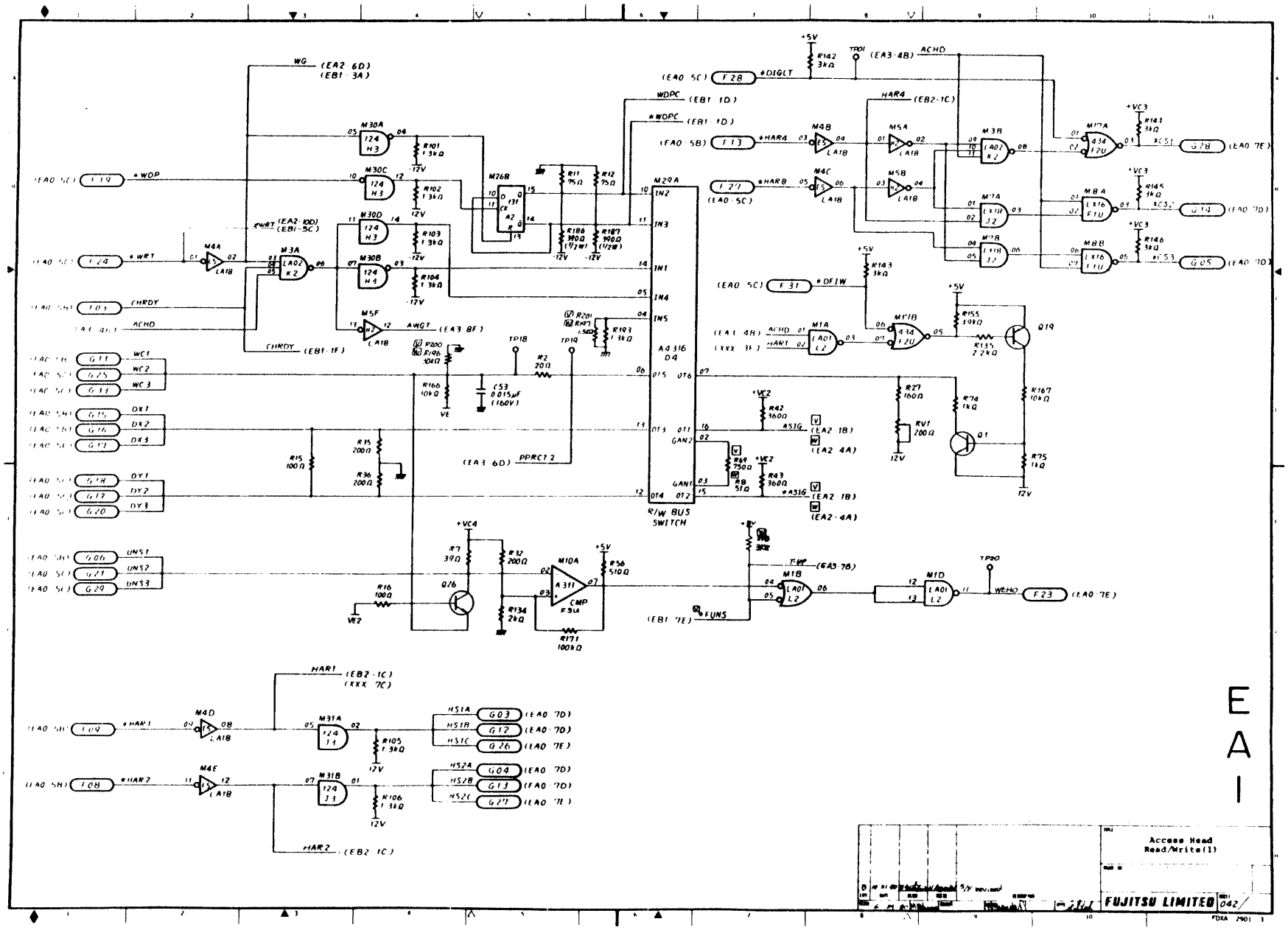

(DC1-1F) 1 FRQ
(DC1-1E) ±0.FRQ
(DC1-4C) PLOFSE
PLO1F (DA0-7C)
PLO1F (DB2 4B) (DC1-1E)
PLO II (2)
FUJITSU LIMITED
DC 2

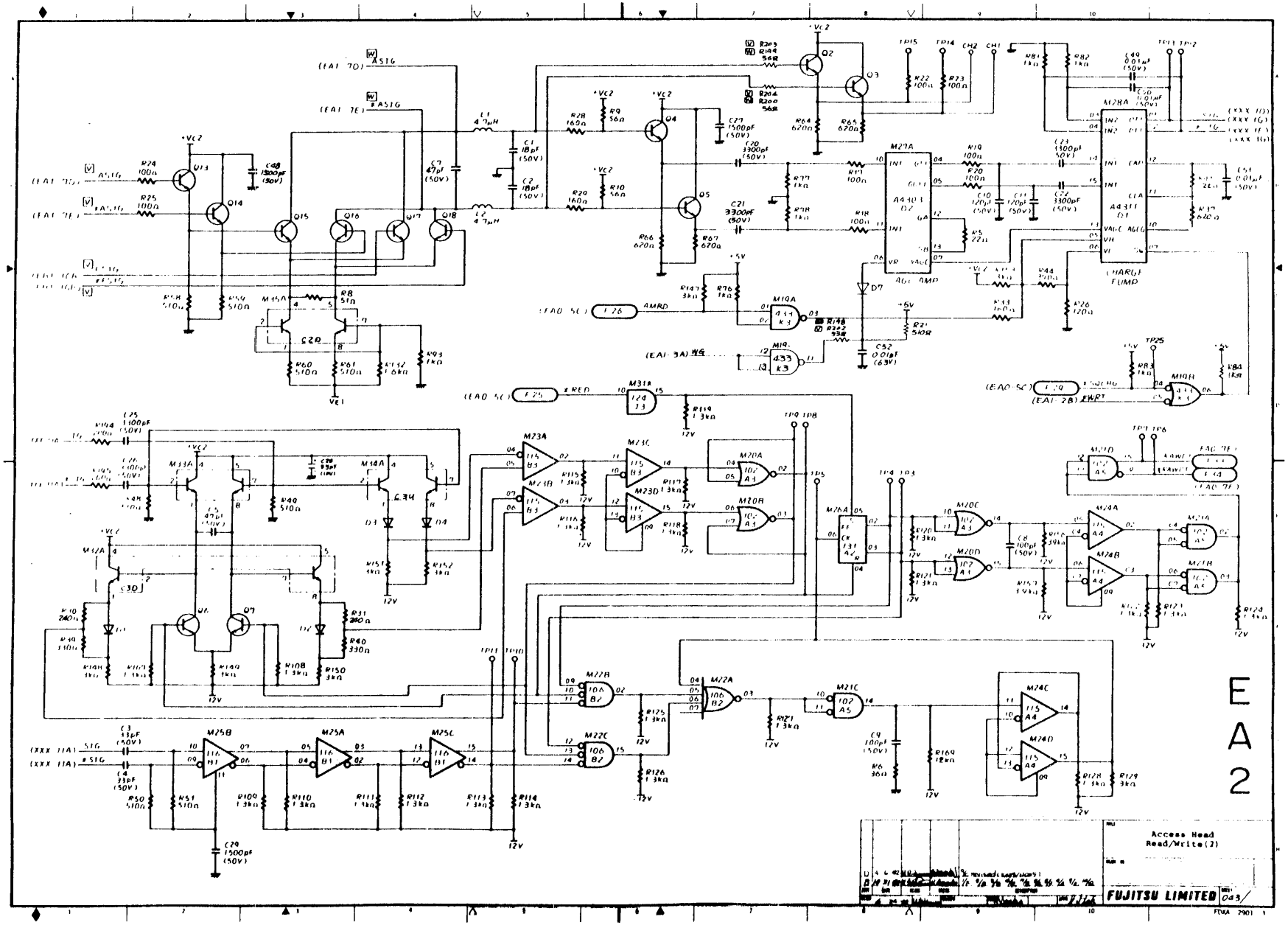

D
D
I
FUJITSU LIMITED

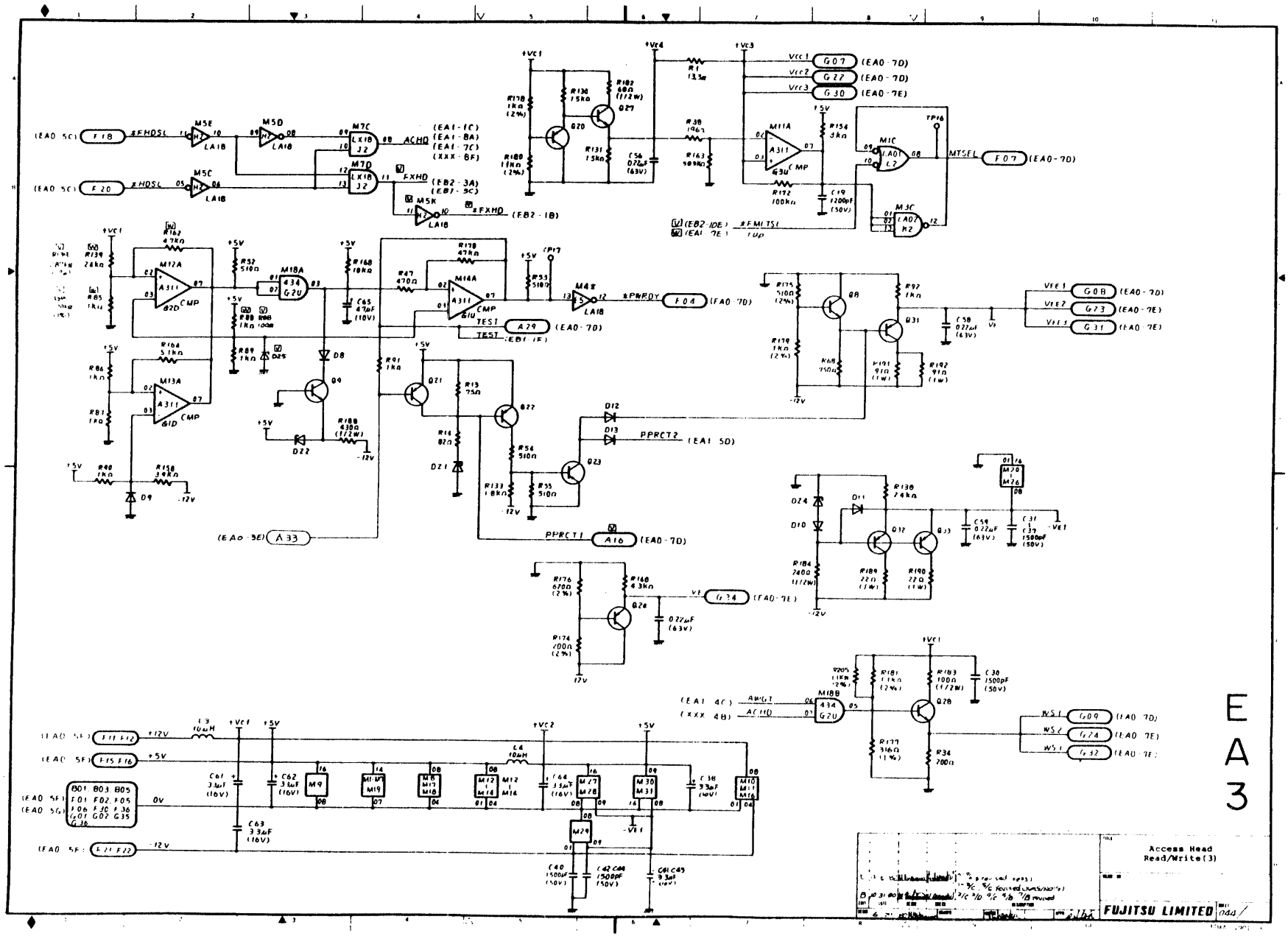

D D 2
VFO (2)
FUJITSU LIMITED
VFOLK
(DD1-8D)
(DD1 28)
(DD1 11H) INC FRQ
(DD1 10D) DEC FRQ
CHE3
TP4
TP5
TP6
TP7
E1
E2
E4
E5

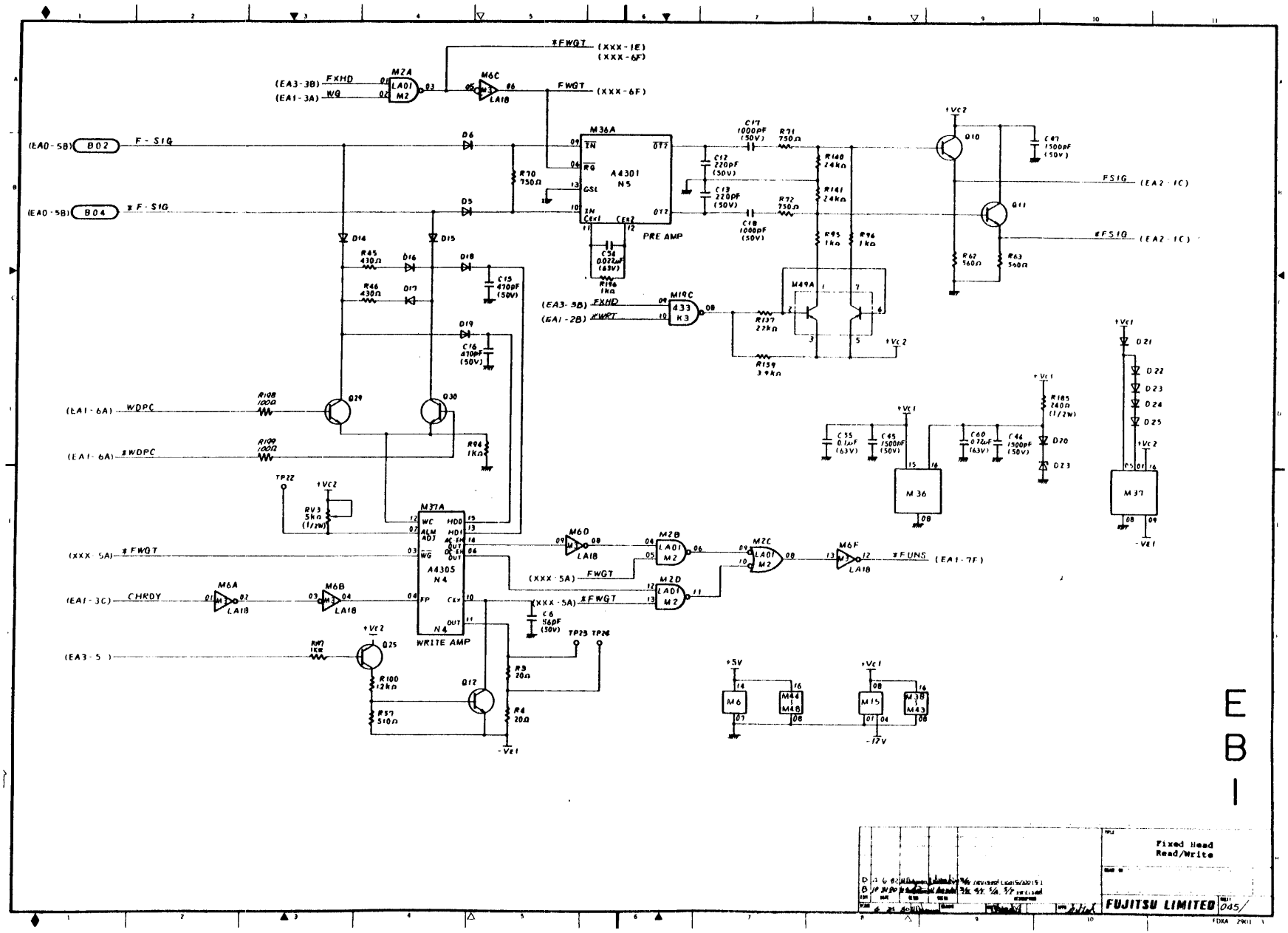

E3
E6
RV5 5kΩ (½W)
R114 1kΩ
R88 680Ω
R35 220Ω
R89 680Ω
C2 27pF (50V)
R110 1kΩ
R53 330Ω
Q10
D15
Q28
Q29
CHE1
R17 56Ω
(DD1-6D) T DATA
D12
D13
D14
Q9
R15 15Ω
C20 47pF (100V)
R121 1.1kΩ
R122 1.1kΩ
D16
R44 300Ω
C59 3.3μF (10V)
R140 2.2kΩ
R93 750Ω
R94 750Ω
R115 1kΩ
R116 1kΩ
R150 8.2kΩ
M39A
M39B
M39D
M39C
VH
CHE2
R18 56Ω
(DD1-5A) VFO2FD
M63A
M61A
M62A
M63B
M34A
M34B
M34C
M40A
M40B
M40C
M40D
M61B
M33A
M33B
M33C
M34D
M35A
M35B
M35C
M33D
M62B
RDAT
(DA0 7B)
(DA0 5B)
B12
VFOFS
WCLK
B02
(DA0 7B)
LOCK TO DATA (DD2-1G)
Data Separator
FUJITSU LIMITED

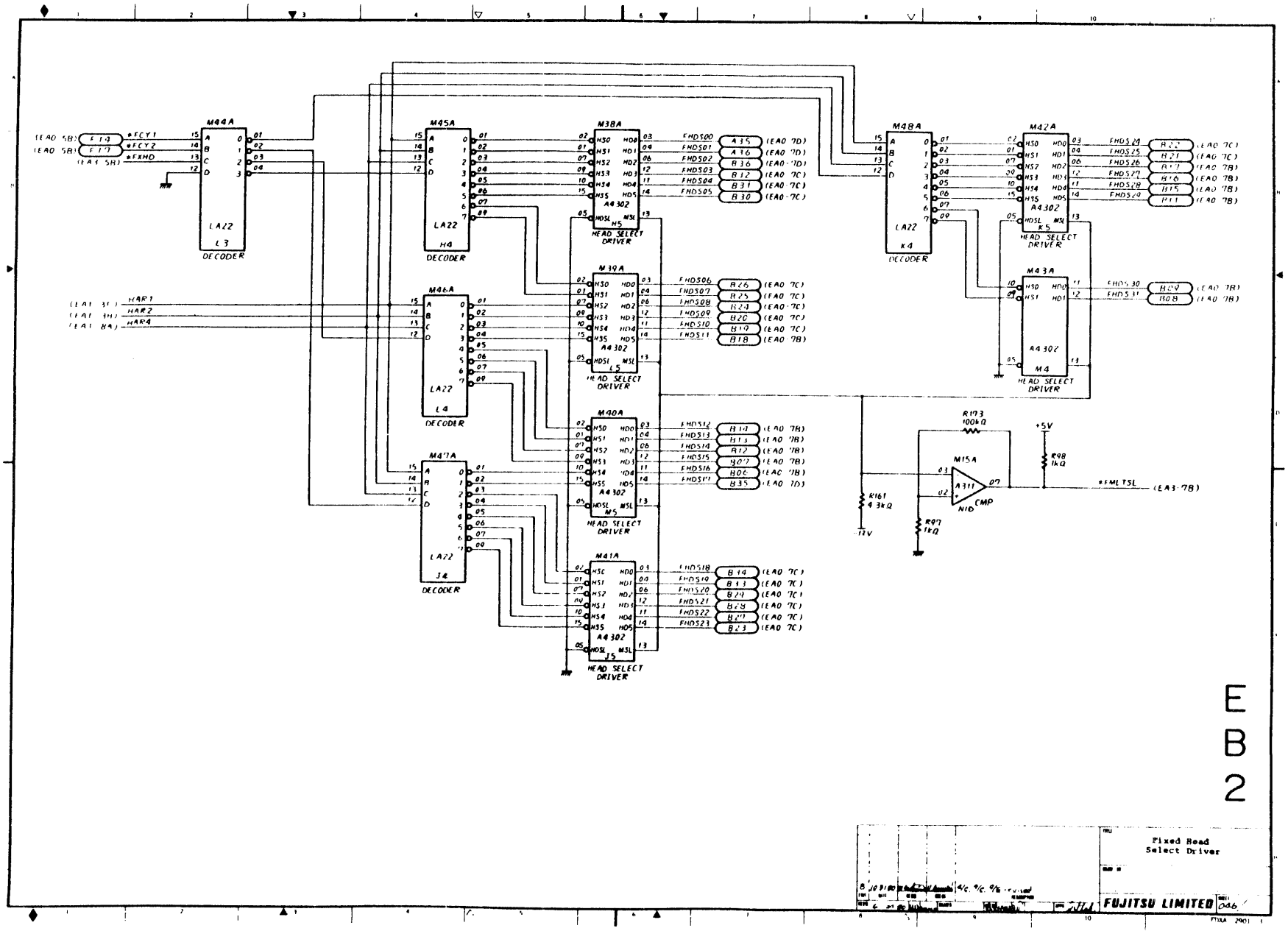

RQVM B16 B - 4170 - 0010A
RQWM B16 B - 4170 - 0020A
E
A
0
RQVM/RQWM I/O Signals
FUJITSU LIMITED

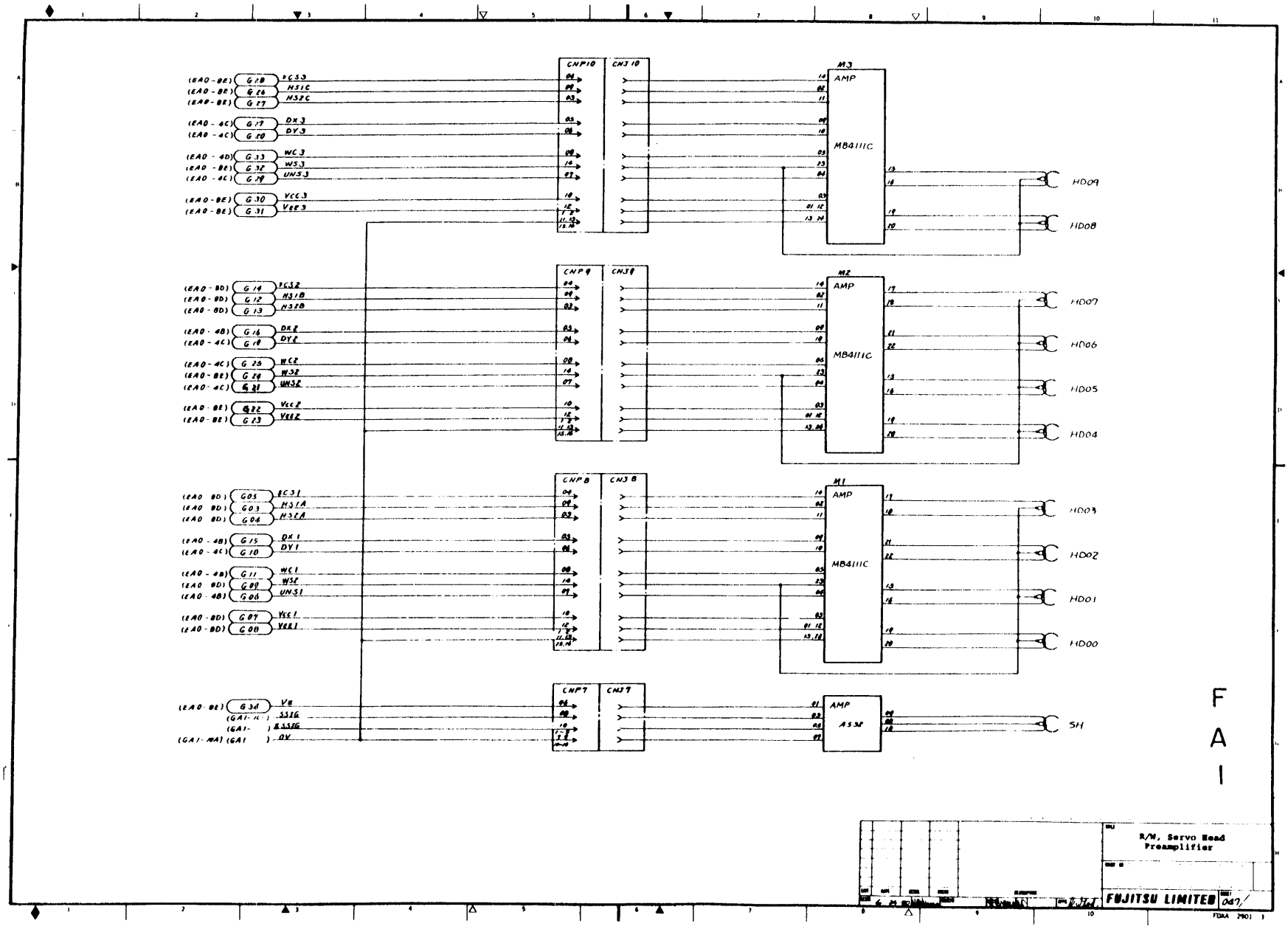

WG (EA2 6D) (EB1 3A)
WDPC (EB1 1D)
*WDPC (EB1 1D)
HAR4 (EB2 1C)
ACHD
*DIGLT
*WDP
*WRT (EA2 10D) (EB1 5C)
*HARB
*DFIW
CHRDY
AWGT (EA3 8F)
CHRDY (EB1 1F)
WC1
WC2
WC3
DX1
DX2
DX3
DY1
DY2
DY3
UNS1
UNS2
UNS3
PPRCT2 (EA3 6D)
R/W BUS SWITCH
*UNS (EB1 7E)
WRHO (EA0 7E)
*HAR1
*HAR2
HAR1 (EB2 1C) (RXXX 7C)
HAR2 (EB2 1C)
Access Head Read/Write(1)
FUJITSU LIMITED
042

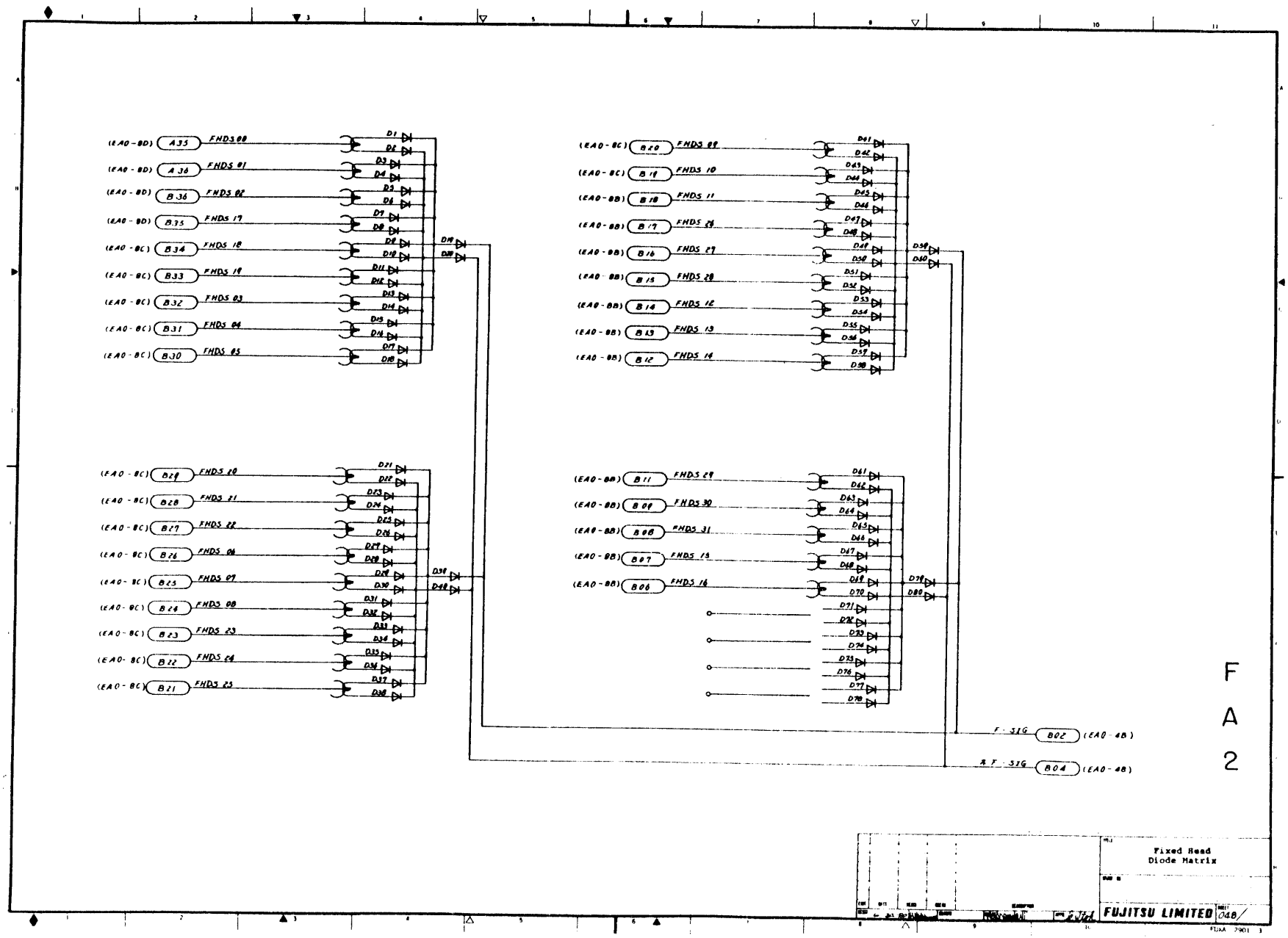

E A 2
Access Head Read/Write(2)
FUJITSU LIMITED

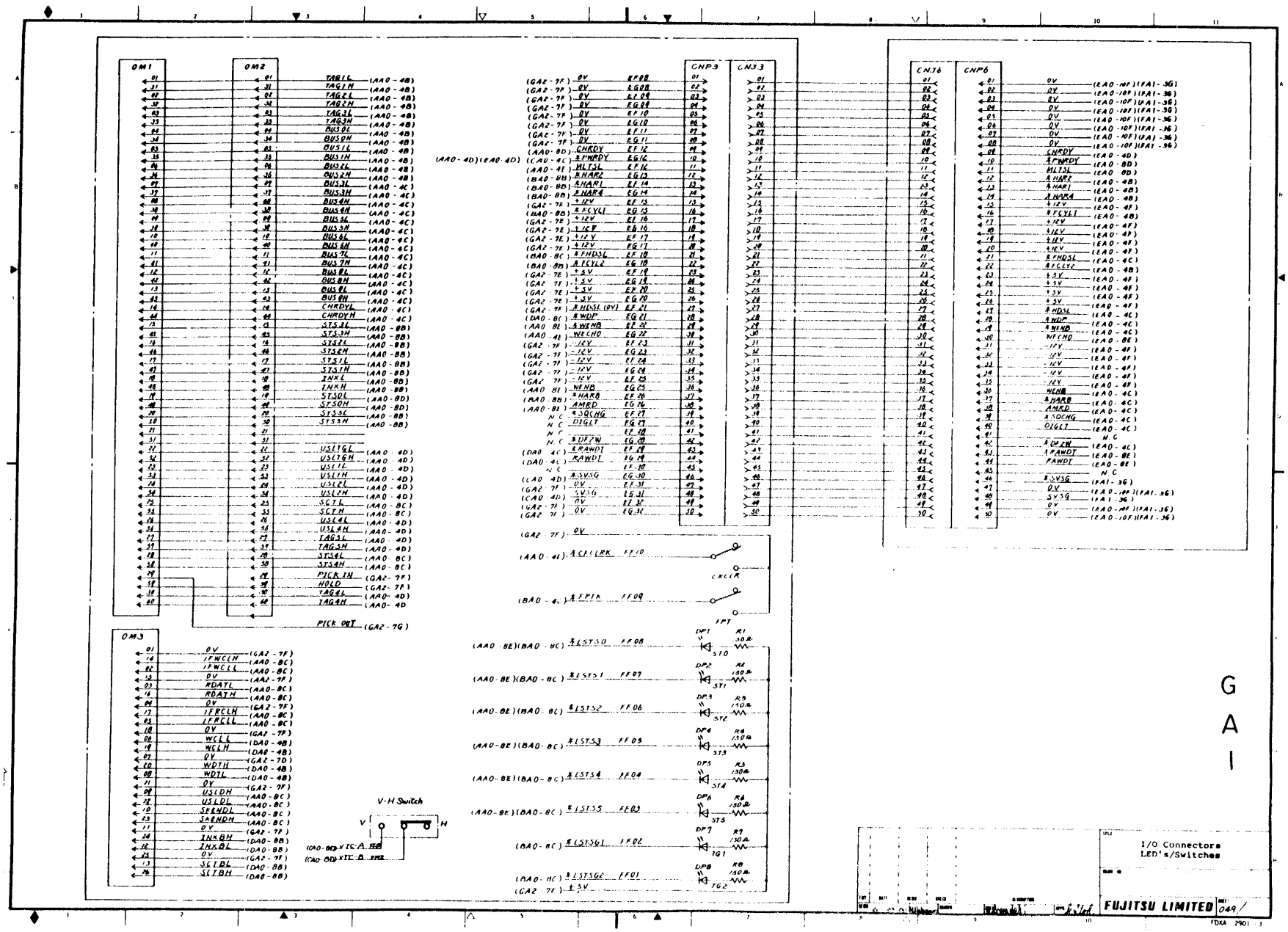

E A 3
Access Head Read/Write(3)
FUJITSU LIMITED
*FEHDSL
*FHDSL
ACHD
FXHD
*FXHD
*PWRDY
TEST
PPRCT2
PPRCT1
MTSEL
*FMLTSL
AWG1
ACHD
WS1
WS2
WS4
+VC1
+VC2
+VC3
+VC4
+5V
-12V
0V

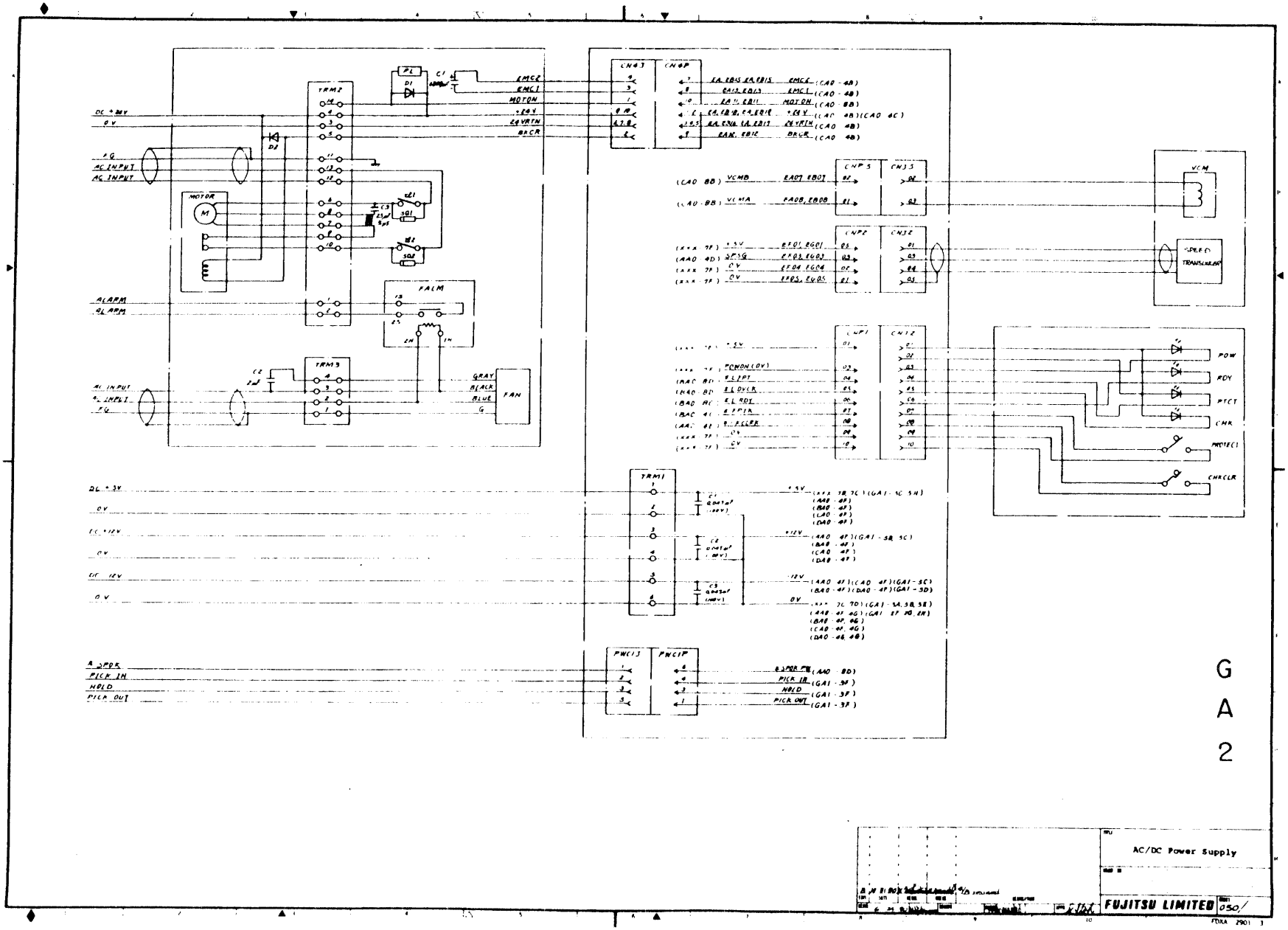

*FWGT (XXX-1E) (XXX-6F)
FWGT (XXX-6F)
(EA3-3B) FXHD
(EA1-3A) WG
M2A
M6C
LA18
(EA0-5B) B02 F-SIG
(EA0-5B) B04 *F-SIG
M36A
A4301 N5
PRE AMP
FSIG (EA2-1C)
*FSIG (EA2-1C)
Q10
Q11
M49A
M10C
(EA3-3B) FXHD
(EA1-2B) *WRT
(EA1-6A) WDPC
(EA1-6A) *WDPC
Q29
Q30
M37A
A4305 N4
WRITE AMP
(XXX-5A) *FWGT
(XXX-5A) FWGT
(EA1-3C) CHRDY
(EA3-5)
Q25
Q12
M6D
M2B
M2C
M2D
M6F
*FUNS (EA1-7F)
M36
M37
+Vc2
+Vc1
-Vc1
+5V
-12V
TP22
TP23
TP24
Fixed Head Read/Write
FUJITSU LIMITED

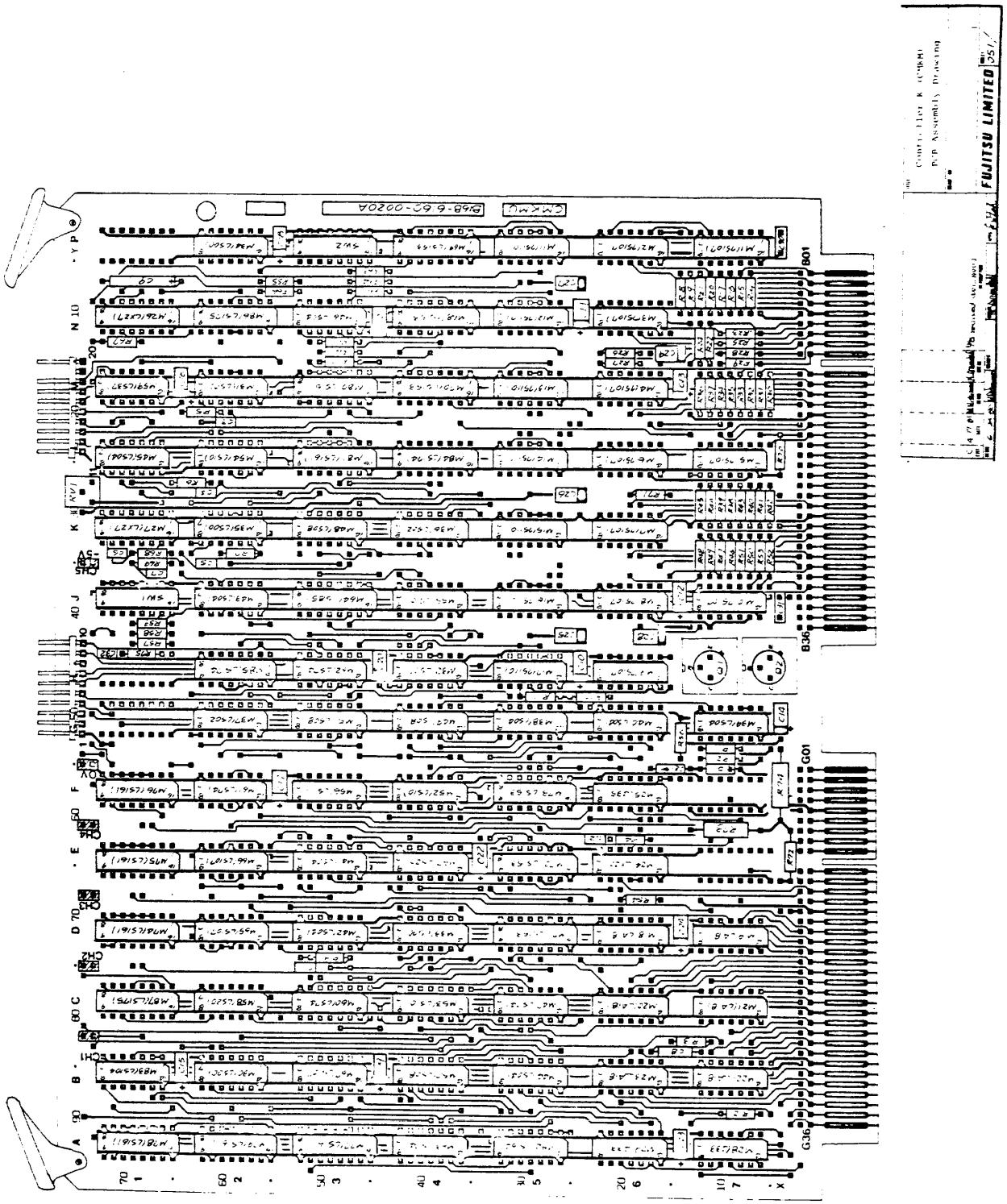

M44A
M45A
M38A
M48A
M42A
M46A
M39A
M43A
M47A
M40A
M41A
DECODER
HEAD SELECT DRIVER
A4302
LA22
M15A
A311
CMP
R193 100kΩ
R161 4.3kΩ
R97 1kΩ
R98 1kΩ
+5V
-12V
*FMLTSL (EA3:78)
E B 2
Fixed Head Select Driver
FUJITSU LIMITED

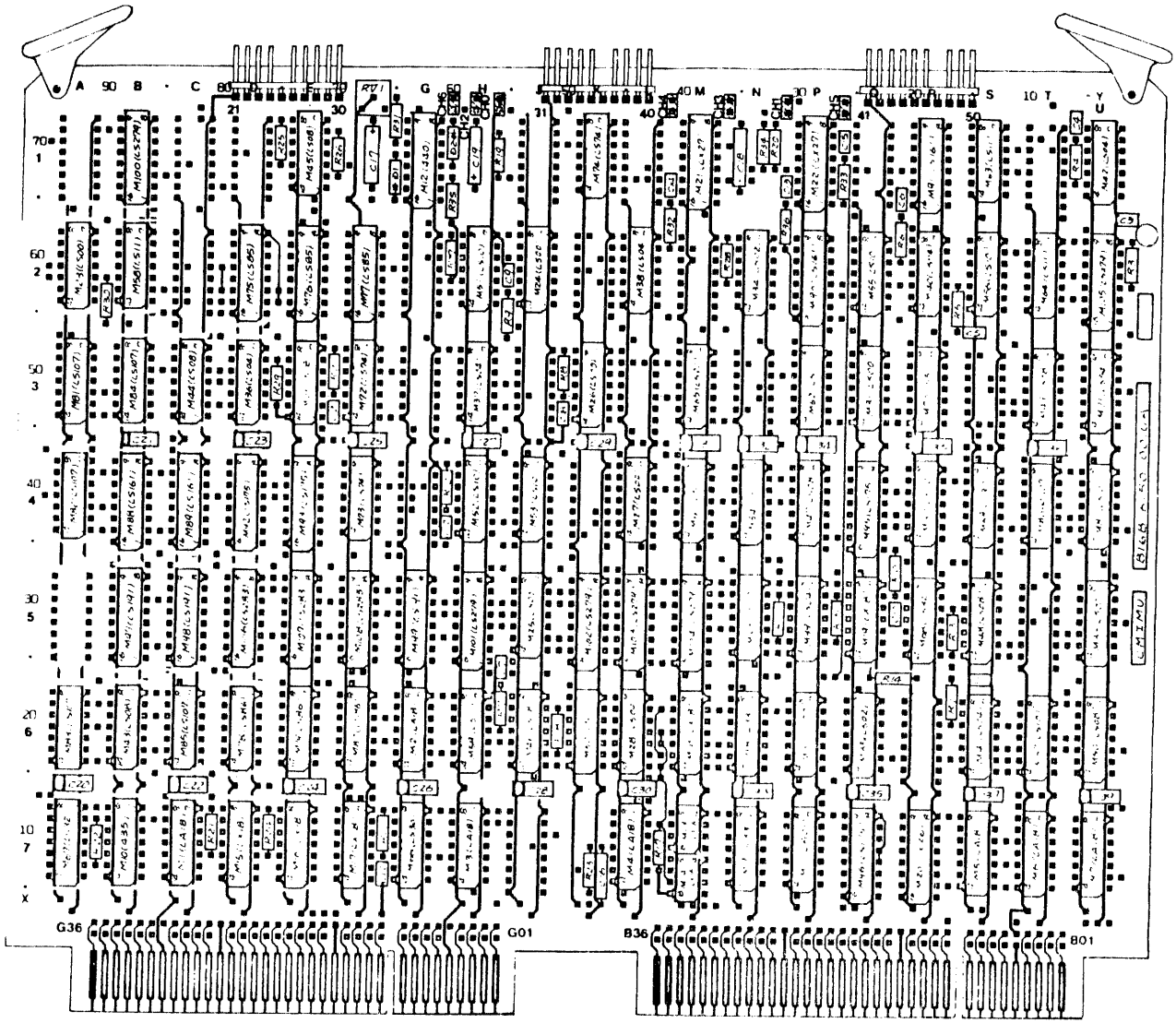

CNP10
CNJ10
M3
AMP
MB4111C
HD09
HD08
CNP9
CNJ9
M2
AMP
MB4111C
HD07
HD06
HD05
HD04
CNP8
CNJ8
M1
AMP
MB4111C
HD03
HD02
HD01
HD00
CNP7
CNJ7
AMP
AS34
SH
F
A
I
R/W, Servo Head
Preamplifier
FUJITSU LIMITED


(EA0-8D) A35 FHDS 00
(EA0-8D) A36 FHDS 01
(EA0-8D) B36 FHDS 02
(EA0-8D) B35 FHDS 17
(EA0-8C) B34 FHDS 18
(EA0-8C) B33 FHDS 19
(EA0-8C) B32 FHDS 03
(EA0-8C) B31 FHDS 04
(EA0-8C) B30 FHDS 05
(EA0-8C) B20 FHDS 09
(EA0-8C) B19 FHDS 10
(EA0-8B) B18 FHDS 11
(EA0-8B) B17 FHDS 28
(EA0-8B) B16 FHDS 29
(EA0-8B) B15 FHDS 28
(EA0-8B) B14 FHDS 12
(EA0-8B) B13 FHDS 13
(EA0-8B) B12 FHDS 14
(EA0-8C) B29 FHDS 20
(EA0-8C) B28 FHDS 21
(EA0-8C) B27 FHDS 22
(EA0-8C) B26 FHDS 06
(EA0-8C) B25 FHDS 07
(EA0-8C) B24 FHDS 08
(EA0-8C) B23 FHDS 23
(EA0-8C) B22 FHDS 24
(EA0-8C) B21 FHDS 25
(EA0-8A) B11 FHDS 29
(EA0-8B) B09 FHDS 30
(EA0-8B) B08 FHDS 31
(EA0-8B) B07 FHDS 14
(EA0-8B) B06 FHDS 16
F SIG B02 (EA0-4B)
A F SIG B04 (EA0-4B)
F A 2
Fixed Head
Diode Matrix
FUJITSU LIMITED 048/

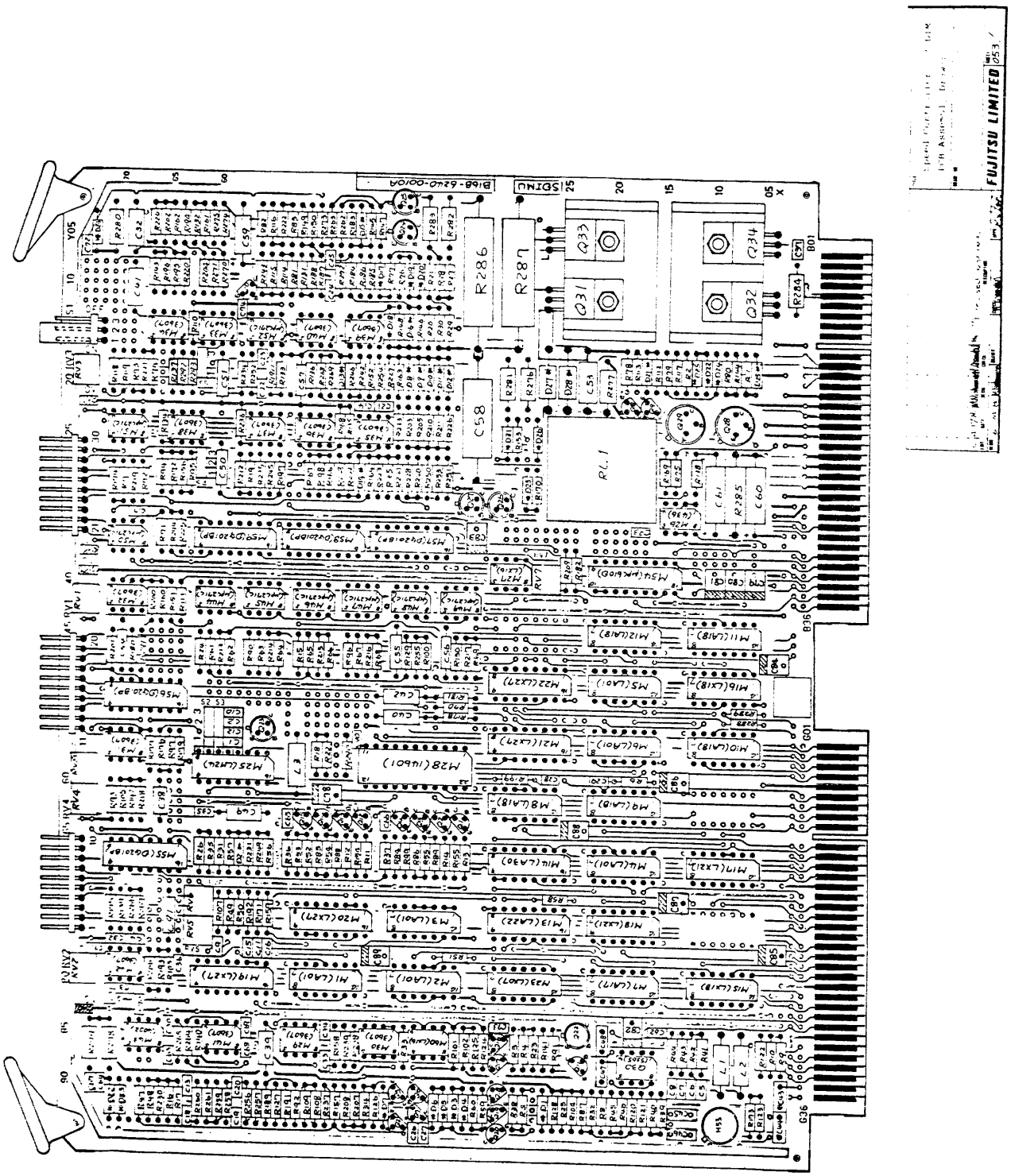

OM1
OM2
OM3
CNP3
CN33
CNJ6
CNP6
V-H Switch
I/O Connectors
LED's/Switches
FUJITSU LIMITED
049/
GAI

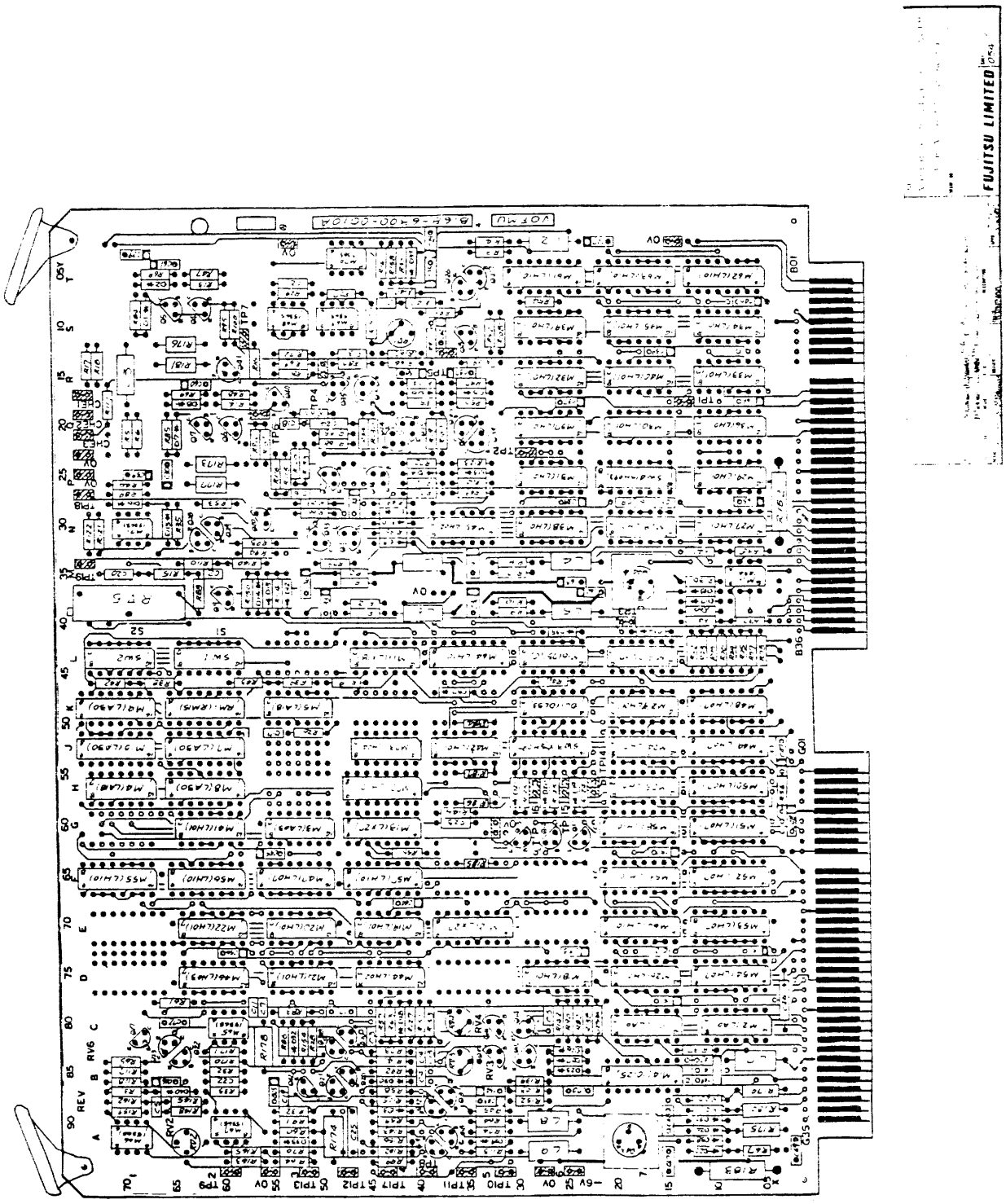

AC/DC Power Supply
FUJITSU LIMITED
G
A
2
MOTOR
FALM
FAN
TRM2
TRM3
TRM1
CN43
CN4P
CNP5
CNJ5
CNP2
CNJ2
CNP1
CNJ1
PWC1J
PWC1P
VCM
SPEED TRANSDUCER
POW
RDY
PTCT
CHR
PROTECT
CHRCLR
DC +36V
0 V
FG
AC INPUT
ALARM
+5V
+12V
-12V
HOLD
PICK OUT

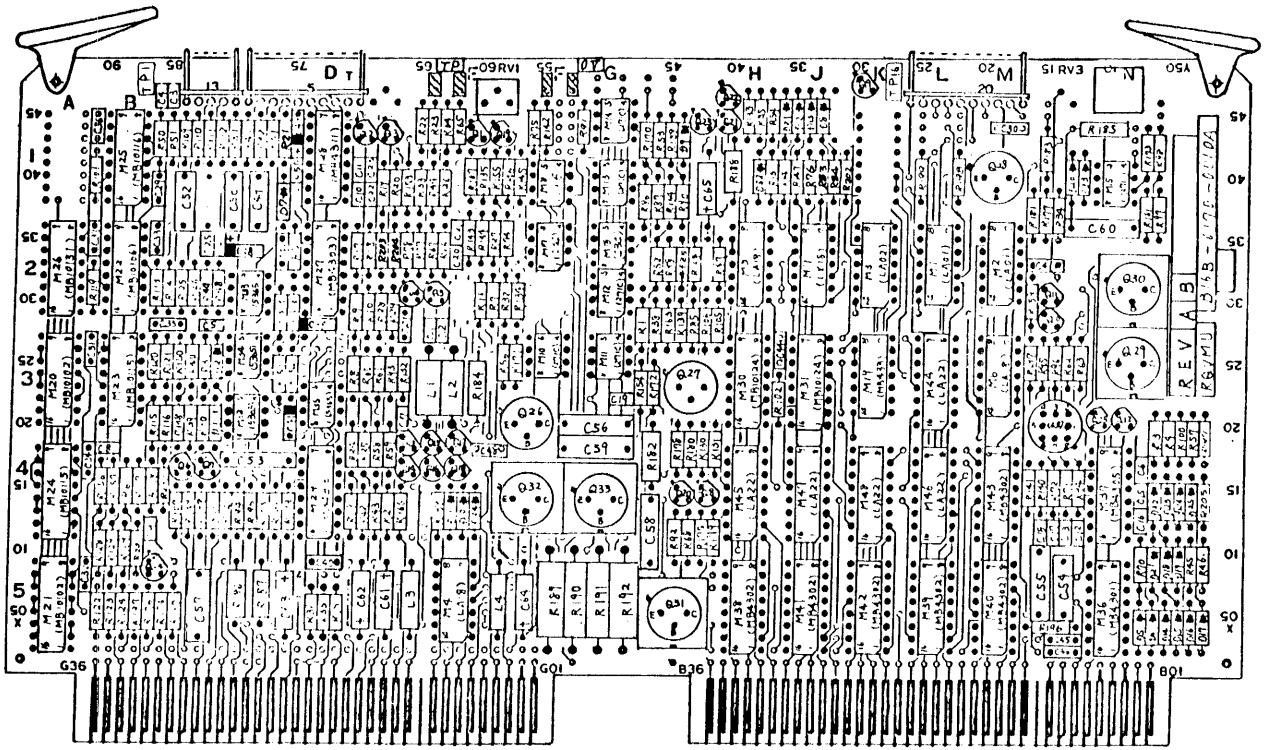

FUJITSU LIMITED



FUJITSU LIMITED

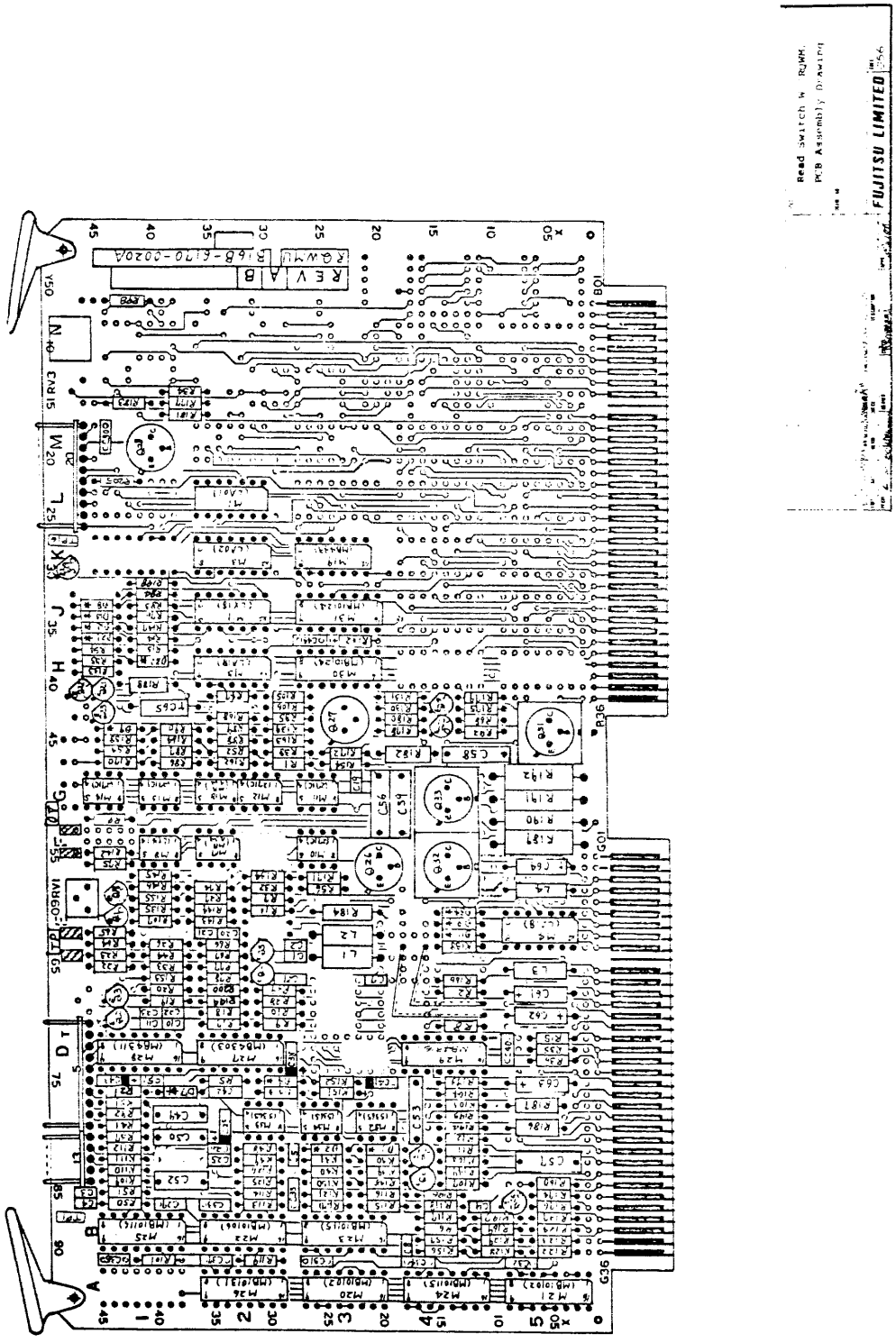

B168-6240-0010A
R286
R287
Q33
Q31
Q34
Q32
C58
RL1
C61
R285
C60
FUJITSU LIMITED

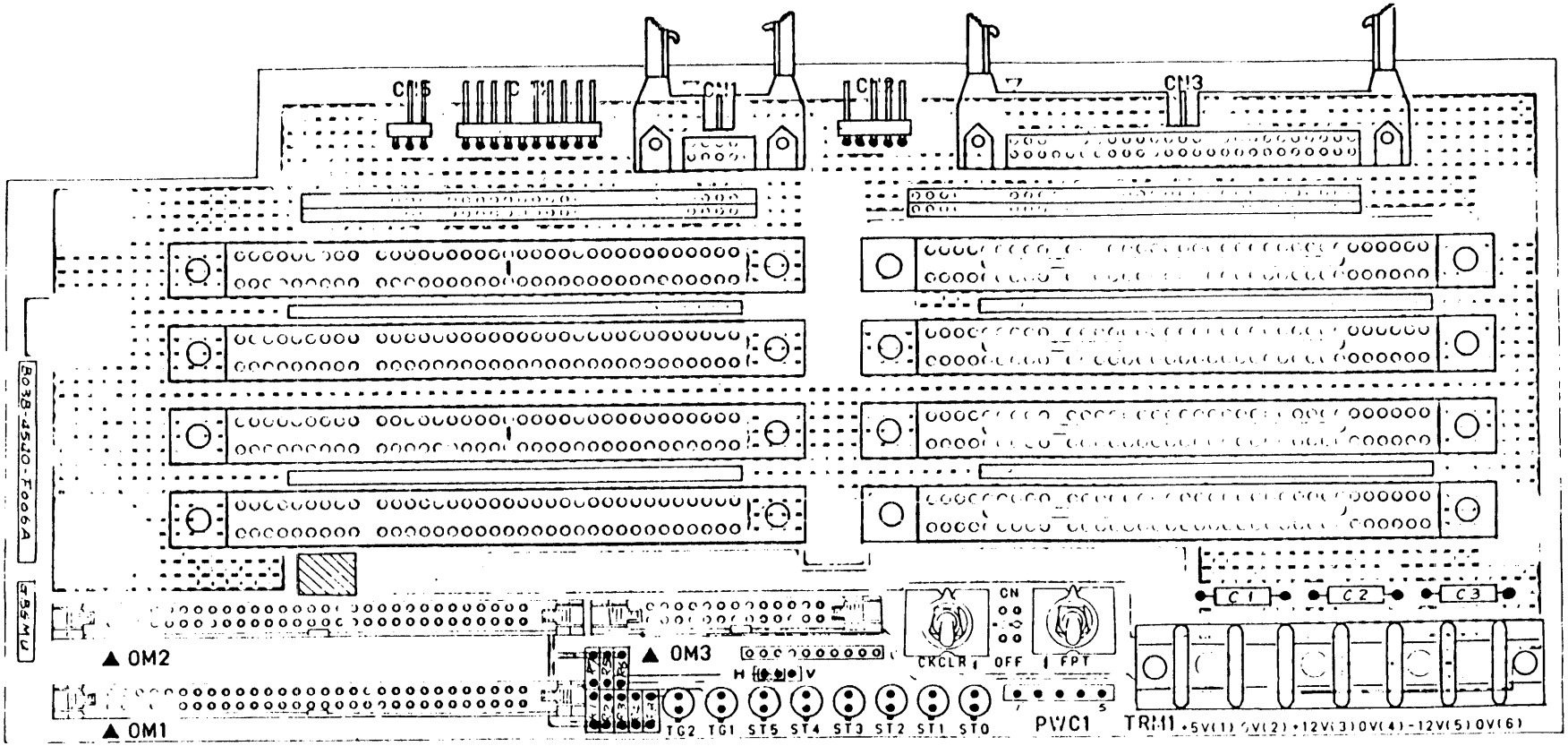

FUJITSU LIMITED

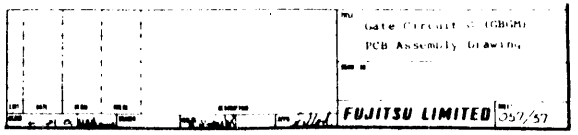


Read Switch V (RQVM)
PCB Assembly Drawing

FUJITSU LIMITED


FUJITSU LIMITED


CN5
CN1
CN2
CN3
B038-4540-F006A
GBGM
OM2
OM3
OM1
CRCLR
OFF
FPT
CN
H
V
TG2 TG1 ST5 ST4 ST3 ST2 ST1 ST0
PWC1
C1
C2
C3
TRM1 +5V(1) 0V(2) +12V(3) 0V(4) -12V(5) 0V(6)


Gate Circuit (GBGM)
PCB Assembly Drawing
FUJITSU LIMITED

Section 5

Trouble Shooting Guide

5. TROUBLE SHOOTING GUIDE

5.1 INTRODUCTION

This section will be contain trouble shooting flow charts according to the error status on the disk unit and control unit.

Note: It is recommended that before any operations, maintenance personnel read carefully Section 6 Maintenance and fully understand the details of the procedures and tools required.

Inspect each item in this list before applying power to the unit after installation.

1. Ensure that the AC line conditions satisfy the unit requirements.
2. If the control unit does not utilize Pick/Hold power sequencing lines, select "Local" mode on the power supply unit.
3. Inspect interface cables to ensure pin 1 on the cable goes to pin 1 of the connect both at the unit and control unit.
4. If the unit is in daisy chain with another unit, make sure the last unit has a Line Terminator (LTN) installed.
5. Ensure that the actuator lock is in the "OFF" position.
6. Ensure that the spindle drive motor lock is in the "OFF" position.
7. Ensure that the motor pulley and belt tension are correct per the AC line frequency.
8. Ensure that the spindle grounding plate (anti-static brush) is properly positioned.
9. Ensure that the proper logical unit number (LUN) of the unit is selected on the PCB and that each LUN is unique to only one unit.
10. Ensure that Hard/Soft sector mode is selected per the system configuration.
11. In the case of Hard Sector (fixed sector length), ensure that the correct sector count is set on the VOFM PCB.
12. Ensure that Tag 4/5 Enable/Disable per the system configuration.
13. Ensure that Disable/Normal keys are correctly set to the Normal position.
14. Ensure the Release Timer Key is set to the desired position.
15. Ensure that all PCB assemblies are firmly seated.

5.2 ERROR STATUS

The disk unit and/or the control unit will issue the following statuses.

Table 5-2-1 Error Status

NOT READY	NOT READY status results it disk drive is not ready.
DEVICE CHECK	DEVICE CHECK status indicates a fault condition has occurred in the unit.
SEEK ERROR	SEEK ERROR status results it a seek error has occurred in seek operation.
READ ERROR	READ ERROR status results it a data error has occurred in read operation.
AM MISSING	AM MISSING status indicates that AM (Address Mark) has not found in AM read operation.
DUAL PORT	DUAL PORT malfunction concerns Select/Reserve functions.

Maintenance Personnel can see the unit status on the Maintenance Aid Display at the rear of the PCB chassis in the unit. Each status is defined by decoding status tags (0 to 3) as shown in Table 5-2-2

Table 5-2-2 Maintenance Aid Display

Tag Decode	Tag Decode 0	Tag Decode 1	Tag Decode 2	Tag Decode 3
Status	Not Ready	Device Check	Unit Normal	Seek Check
Status 0	Power Ready	Control Check 1	Unit Selected	Seek or RTZ Time Out
Status 1	Channel Ready	Control Check 2	Fixed Sector Mode	Seek Guard Band
Status 2	Speed OK	Read/Write Check 1	On Cylinder	Linear Mode Guard Band
Status 3	Start 1 (GBENB)	Read/Write Check 2	File Protected	RTZ Outer Guard Band
Status 4	Start 2	Read/Write Check 3	Busy	Over Track Crossing Pulse
Status 5	Initial Seek Time Out	Read/Write Check 4	Access-Head selected	Illegal Cylinder Address
Condition	$\overline{\text{URDY}}$	URDY-DVCK	URDY.$\overline{\text{DVCK}}$. $\overline{\text{SKERR}}$	URDY.$\overline{\text{DVCK}}$. $\overline{\text{SKERR}}$

The trouble shooting guide is provided with the Error Code which is defined by the Maintenance Aid Display LED's. Each error code is represented in hexa-coded, in which TG2 is MSB (Most Significant Bit) and ST0 is LSB (Least Significant Bit). The error codes are shown in Table 5-2-3.

Table 5-2-3 Error Code

Unit Status	Error Code	TG2	TG1	ST5	ST4	ST3	ST2	ST1	ST0	Error/Fault
Not Ready Status	00/02	0	0	0	0	0	0	(*2) X	0	Not Power Ready
	01/03	0	0	0	0	0	0	X	1	Not Speed OK
	05/07	0	0	0	0	0	1	X	1	Not GBENB
	OD/1F	0	0	0	0	1	1	X	1	Not START
	1D/1F	0	0	0	1	1	1	X	1	Not STARTP
	3D/3F	0	0	1	1	1	1	X	1	Initial Seek Time Out (*1)
Device Check Status	41	0	1	0	0	0	0	0	1	Control Check 1
	42	0	1	0	0	0	0	1	0	Control Check 2
	44	0	1	0	0	0	1	0	0	Read/Write Check 1
	48	0	1	0	0	1	0	0	0	Read/Write Check 2
	50	0	1	0	1	0	0	0	0	Read Write Check 3
	60	0	1	1	0	0	0	0	0	Read/Write Check 4 *
Seek Check Status	C1	1	1	0	0	0	0	0	1	Seek or RTZ Time Out
	C2	1	1	0	0	0	0	1	0	Seek Guard Band
	C4	1	1	0	0	0	1	0	0	Linear Mode Guard Band
	C8	1	1	0	0	1	0	0	0	RTZ Outer Guard Band
	D0	1	1	0	1	0	0	0	0	Over Track Crossing Pulse
	E0	1	1	1	0	0	0	0	0	Illegal Cylinder Address

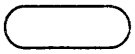
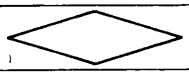
*1) Error Code "3F" activates DVCK status, which is issued to the control unit and lights the DVCK LED on the optional front panel.
*2) "X" is irrelevant.

5.3 TROUBLE SHOOTING SYMBOL

The trouble shooting flow chart contains the procedures to pursure trouble causes starting from an error status.

The following conventions are provided to aid understanding the symbols used in this trouble shooting flow charts as shown in Table 5-3-1.

Table 5-3-1 Symbol of Flow Chart

Symbol	Description
	Terminals. Starting point of the trouble.
	Decision, go ahead according to YES or NO. (Reference test point.)
	Connector, go ahead same-numbered symbol in same sheet.
	Connector, go ahead same-numbered symbol in another sheet.
	Process

5.4 TROUBLE SHOOTING FLOW CHART

In this paragraph, the following flow charts are provided.

Figure 5-4-1 Not Ready
Figure 5-4-2 Device Check
Figure 5-4-3 Seek Error
Figure 5-4-4 Read Error
Figure 5-4-5 AM Missing (for only Soft Sector)
Figure 5-4-6 Dual Port

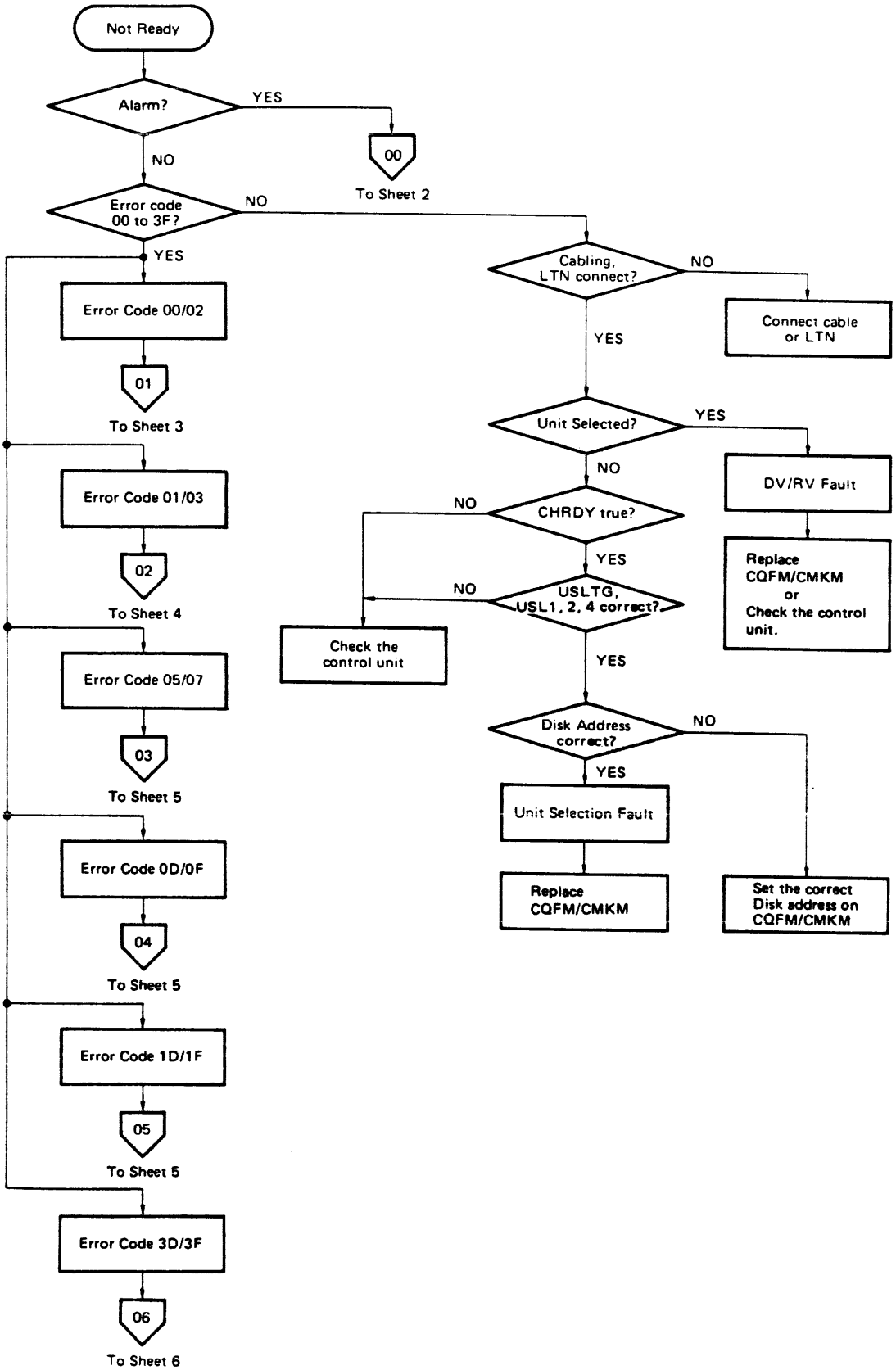


Figure 5-4-1 Not Ready Flow Chart (Sheet 1 of 6)

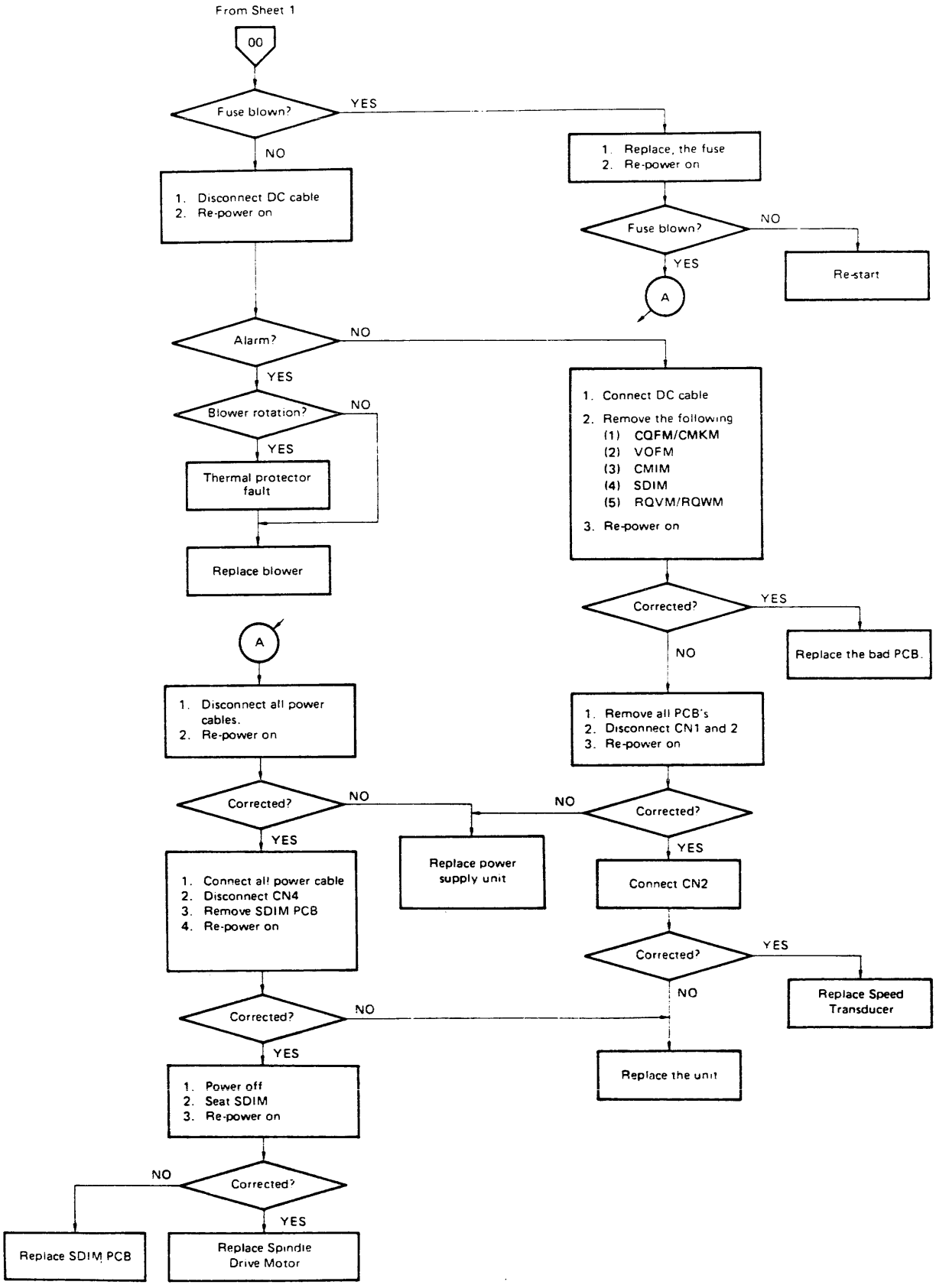


Figure 5-4-1 Not Ready Flow Chart (Sheet 2 of 6)

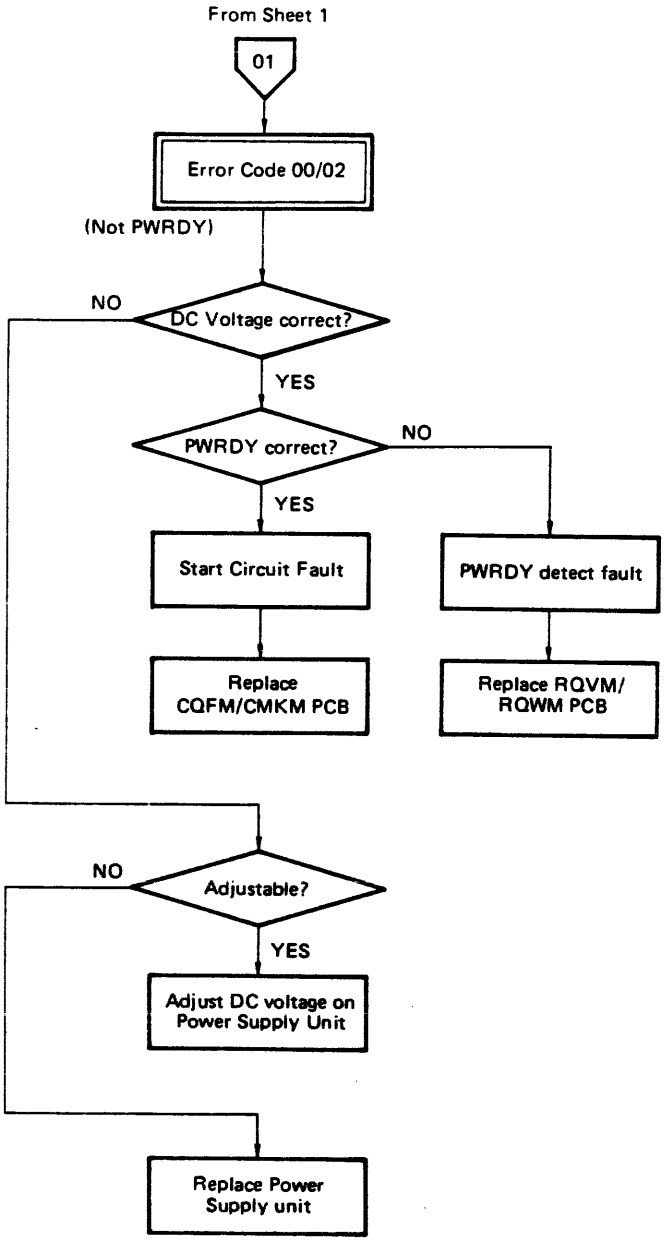


Figure 5-4-1 Not Ready Flow Chart (Sheet 3 of 6)

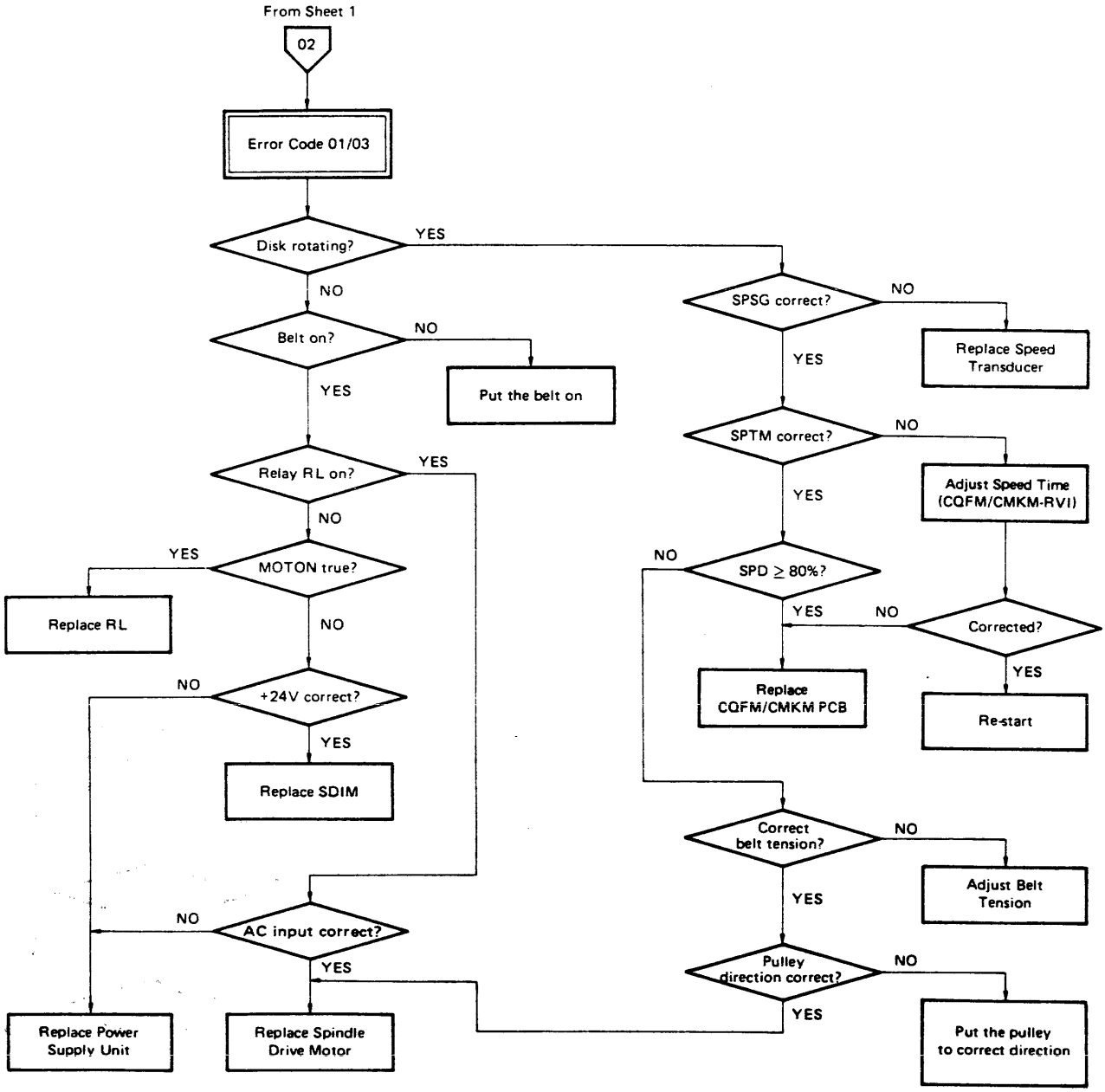


Figure 5-4-1 Not Ready Flow Chart (Sheet 4 of 6)

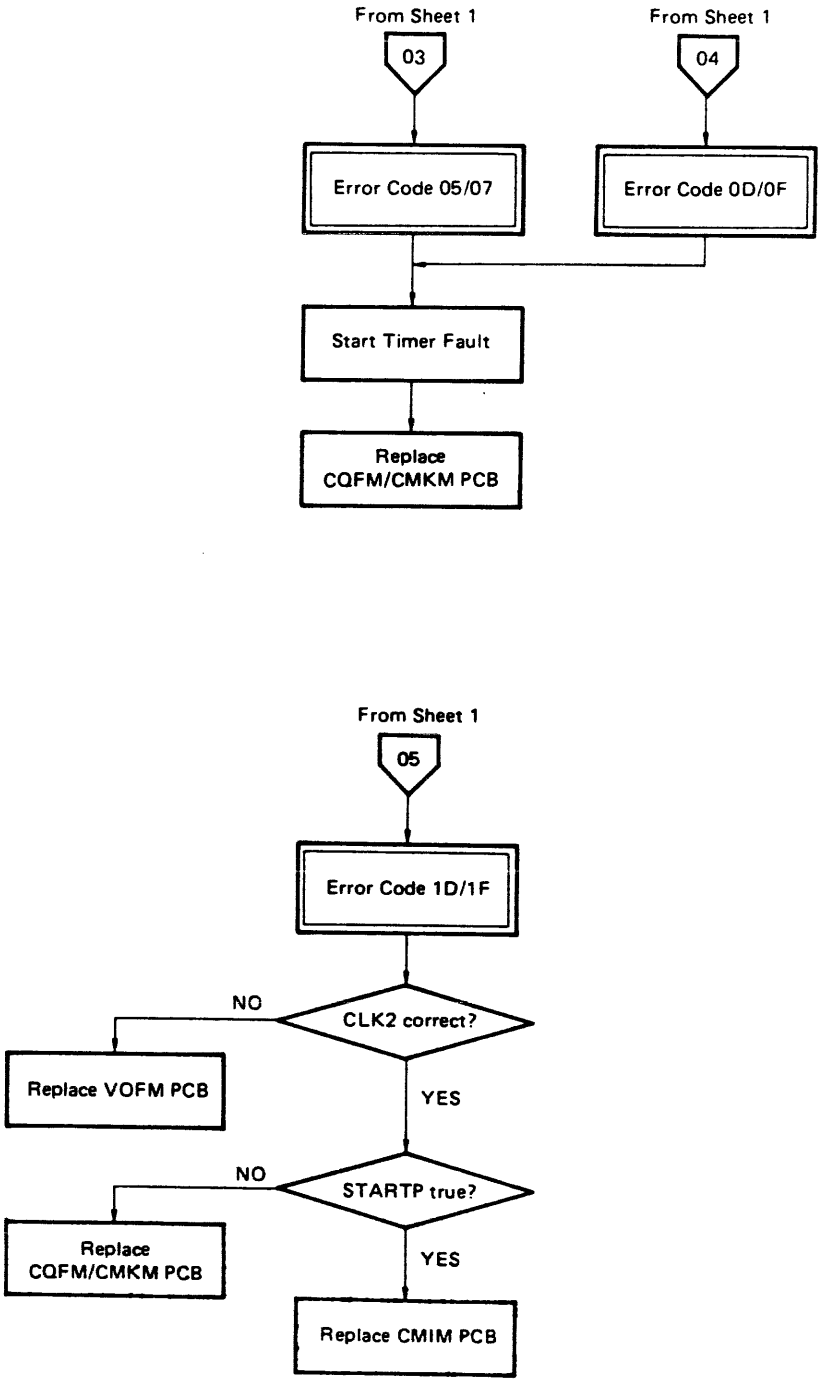


Figure 5-4-1 Not Ready Flow Chart (Sheet 5 of 6)

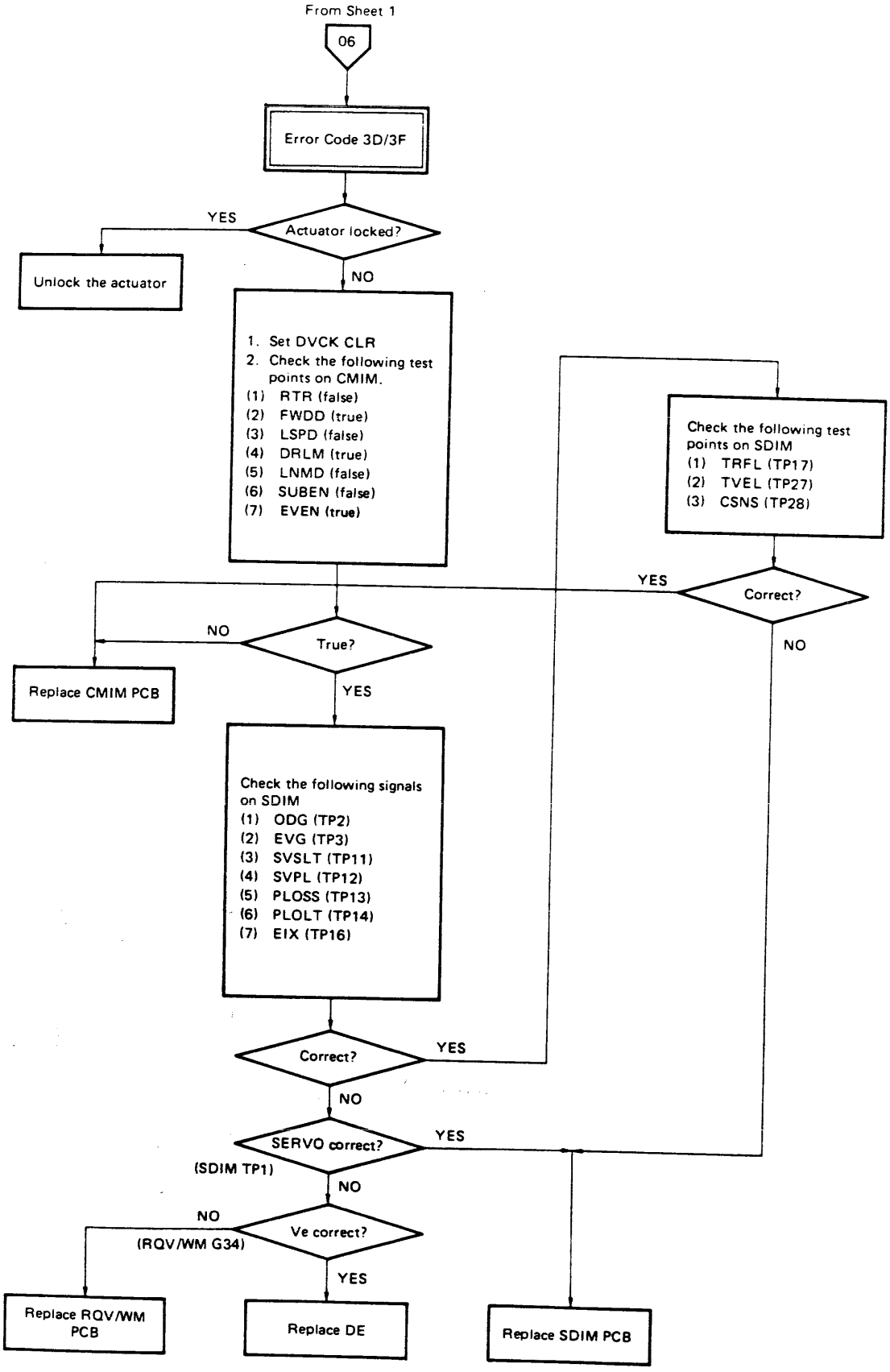


Figure 5-4-1 Not Ready Flow Chart (Sheet 6 of 6)

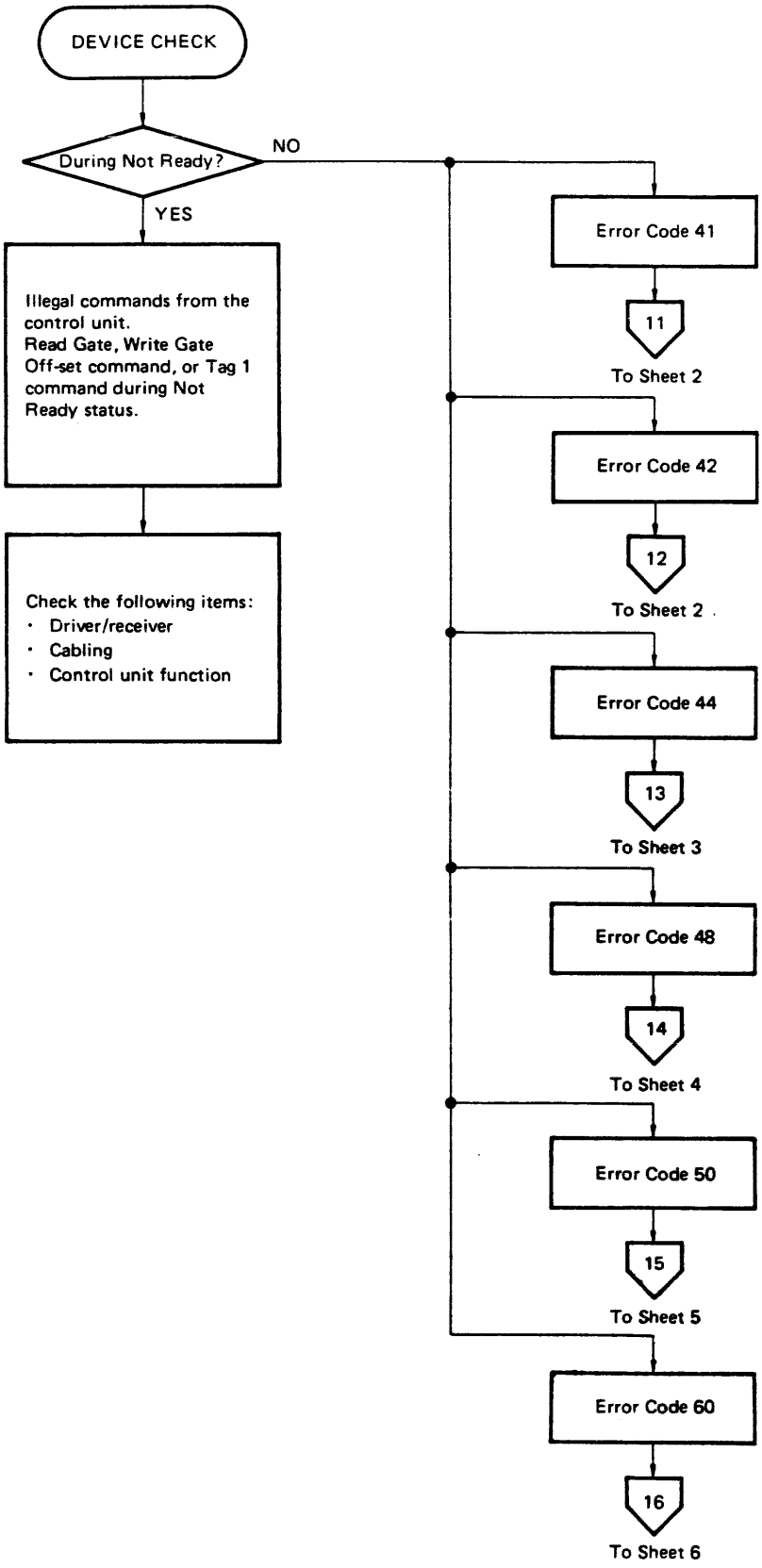


Figure 5-4-2 Device Check Flow Chart (Sheet 1 of 6)

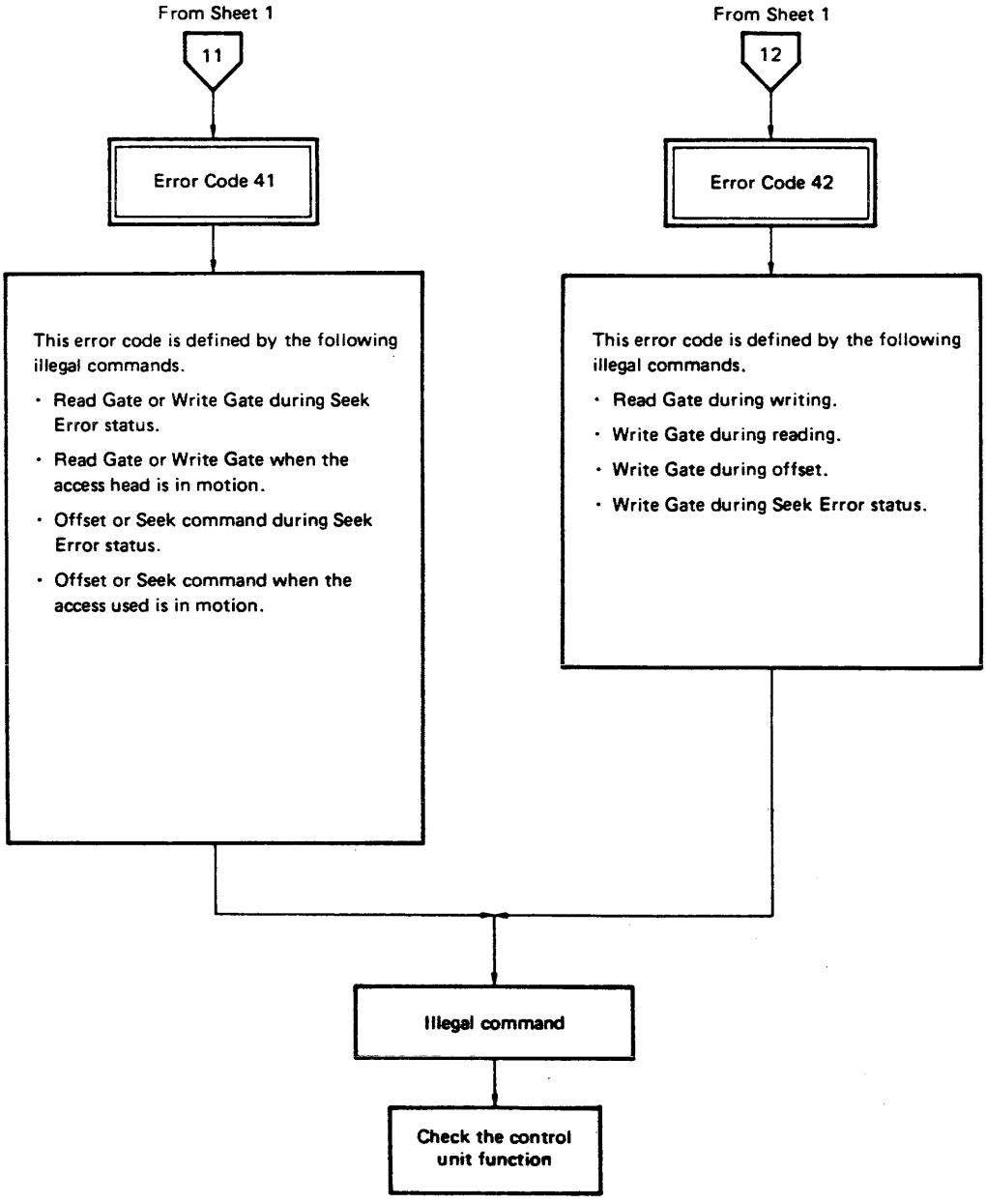


Figure 5-4-2 Device Check Flow Chart (Sheet 2 of 6)

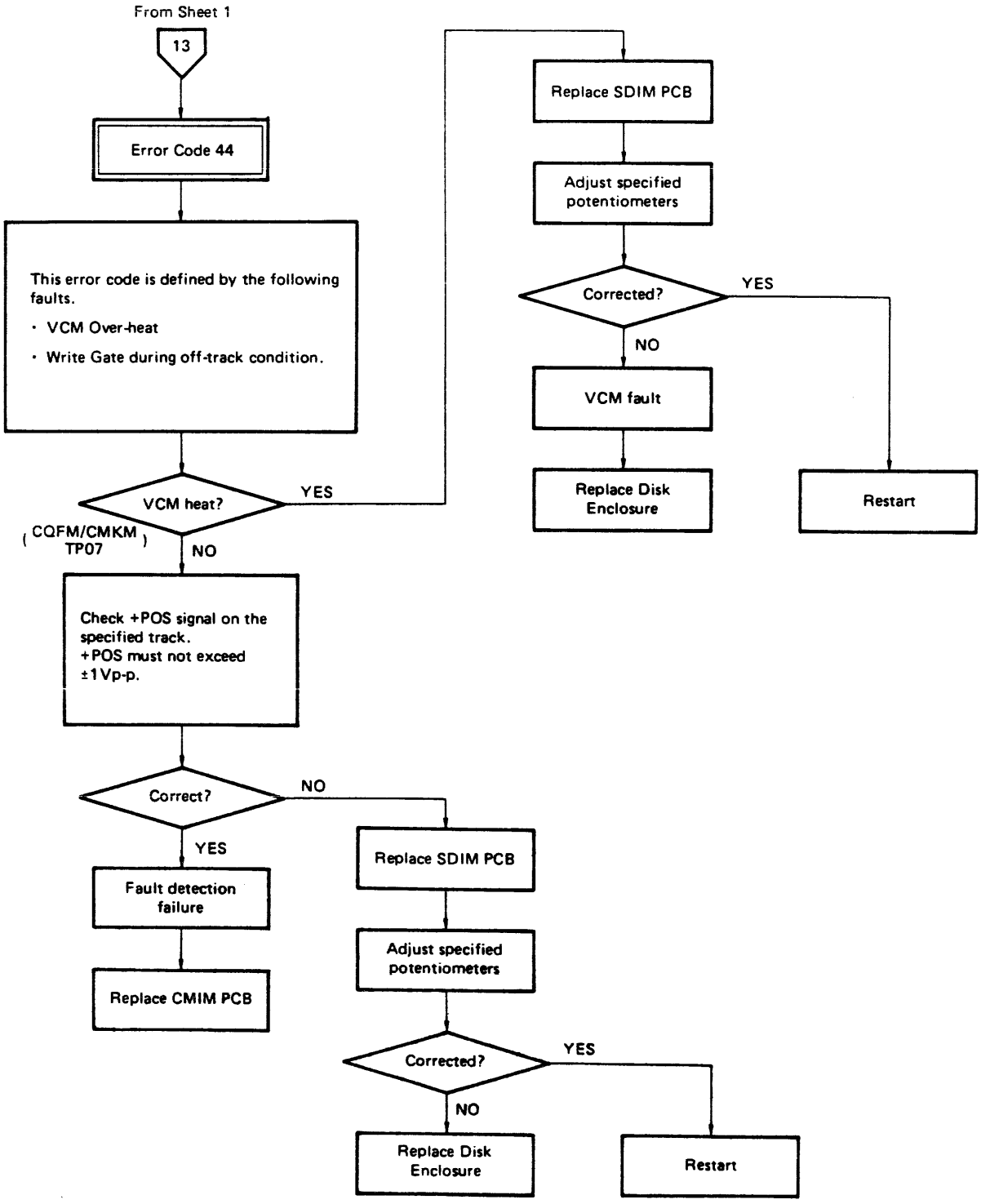


Figure 5-4-2 Device Check Flow Chart (Sheet 3 of 6)

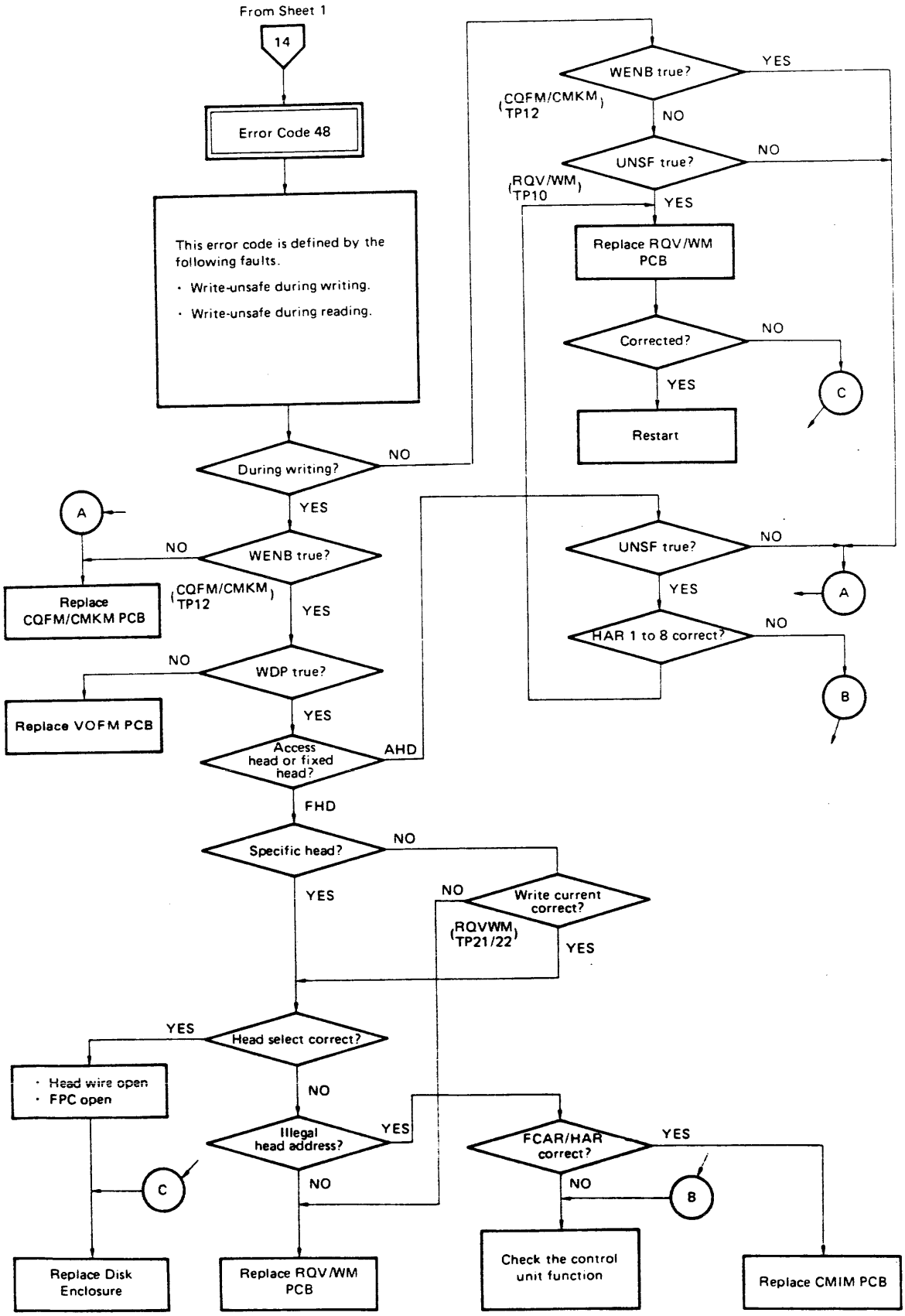
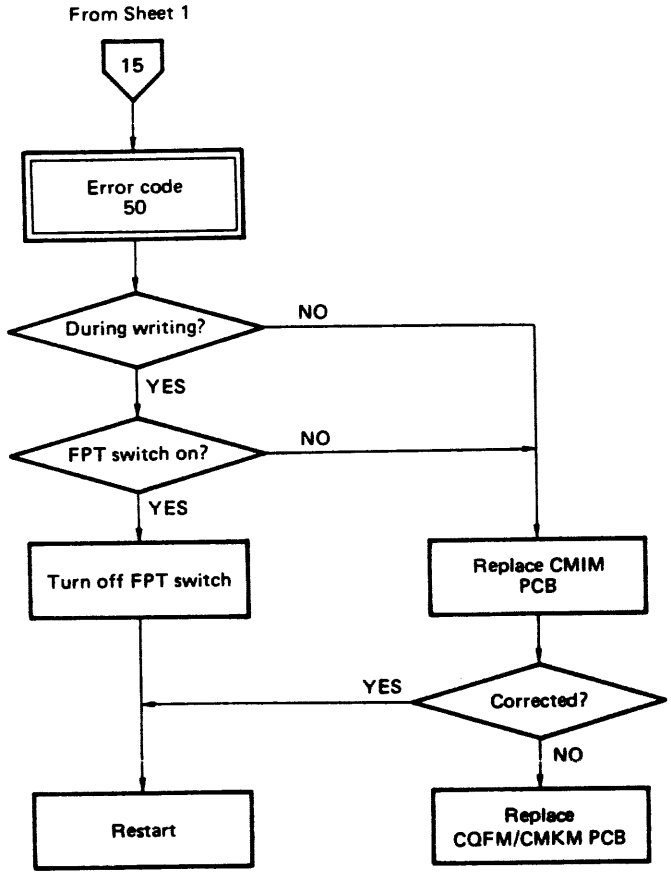


Figure 5-4-2 Device Check Flow Chart (Sheet 4 of 6)



Note: FPT (file-protect) switches are located on the front panel and the PCB chassis.

Figure 5-4-2 Device Check Flow Chart (Sheet 5 of 6)

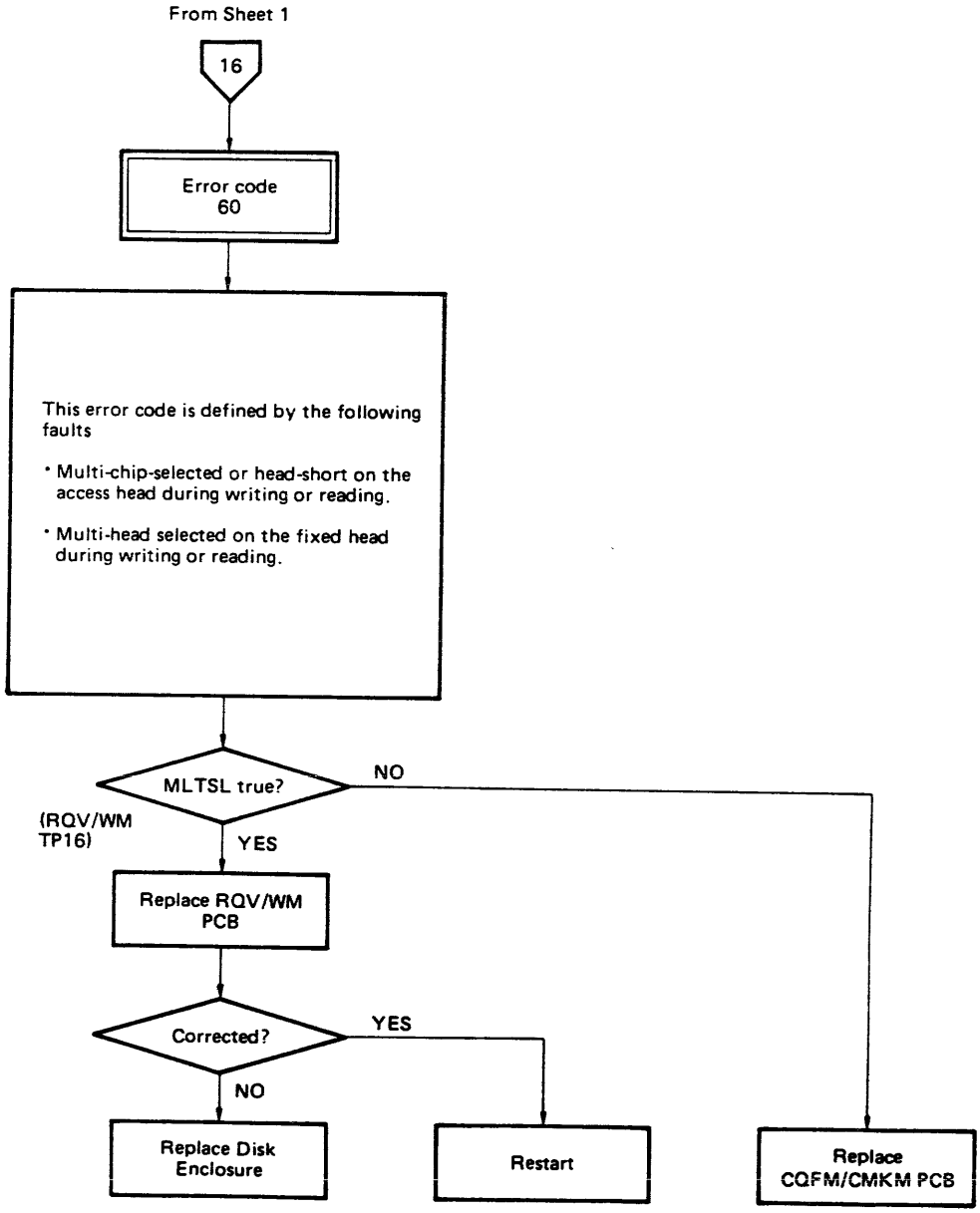


Figure 5-4-2 Device Check Flow Chart (Sheet 6 of 6)

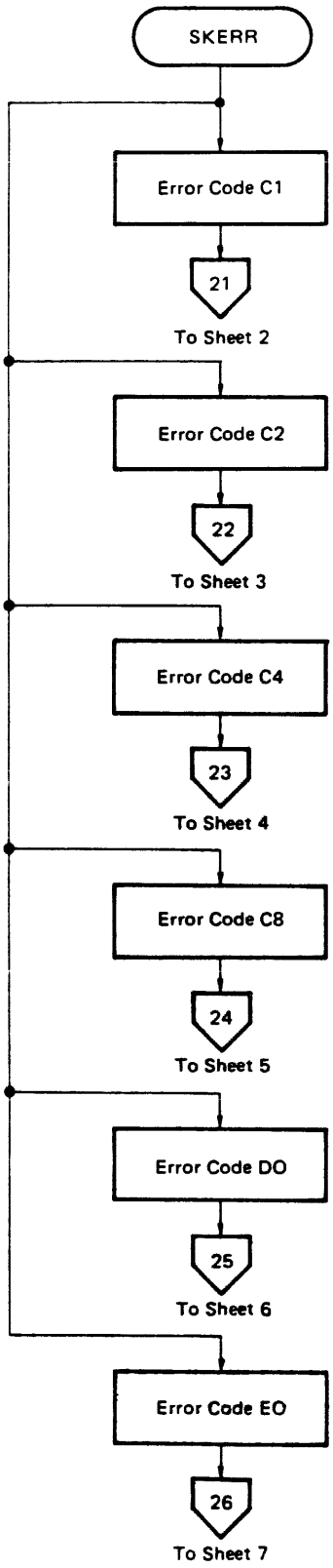


Figure 5-4-3 Seek Error Flow Chart (Sheet 1 of 7)

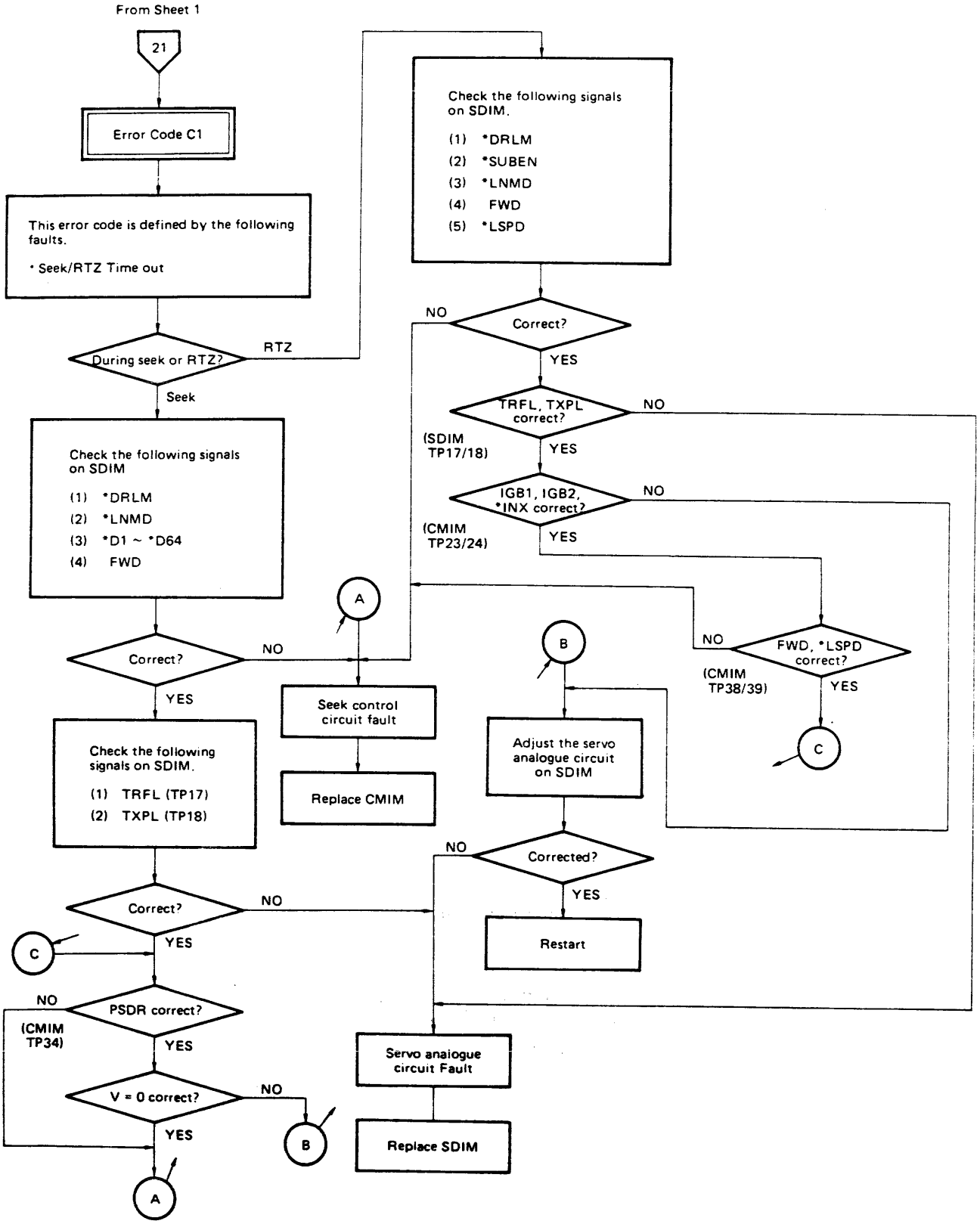


Figure 5-4-3 Seek Error Flow Chart (Sheet 2 of 7)

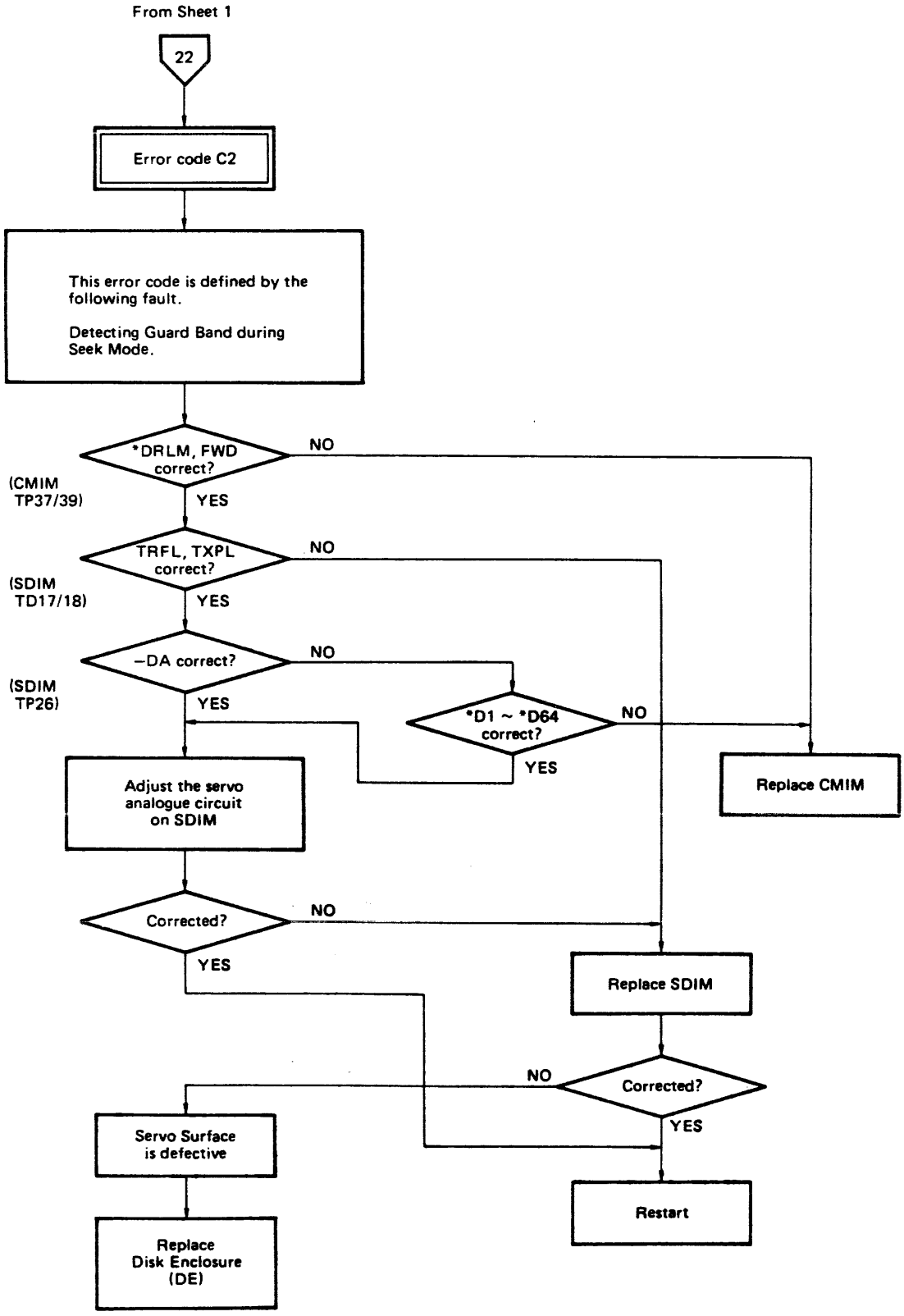


Figure 5-4-3 Seek Error Flow Chart (Sheet 3 of 7)

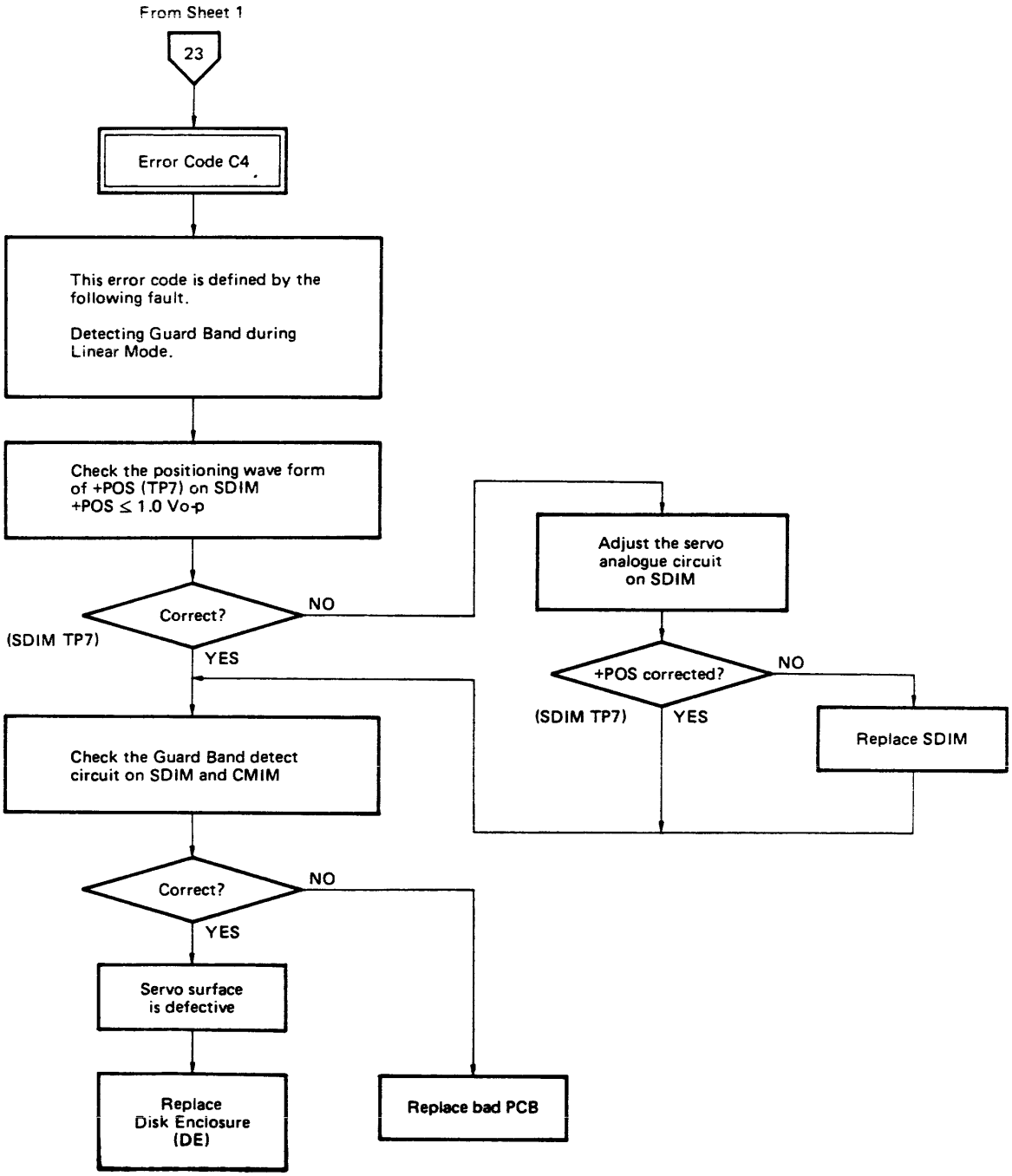


Figure 5-4-3 Seek Error Flow Chart (Sheet 4 of 7)

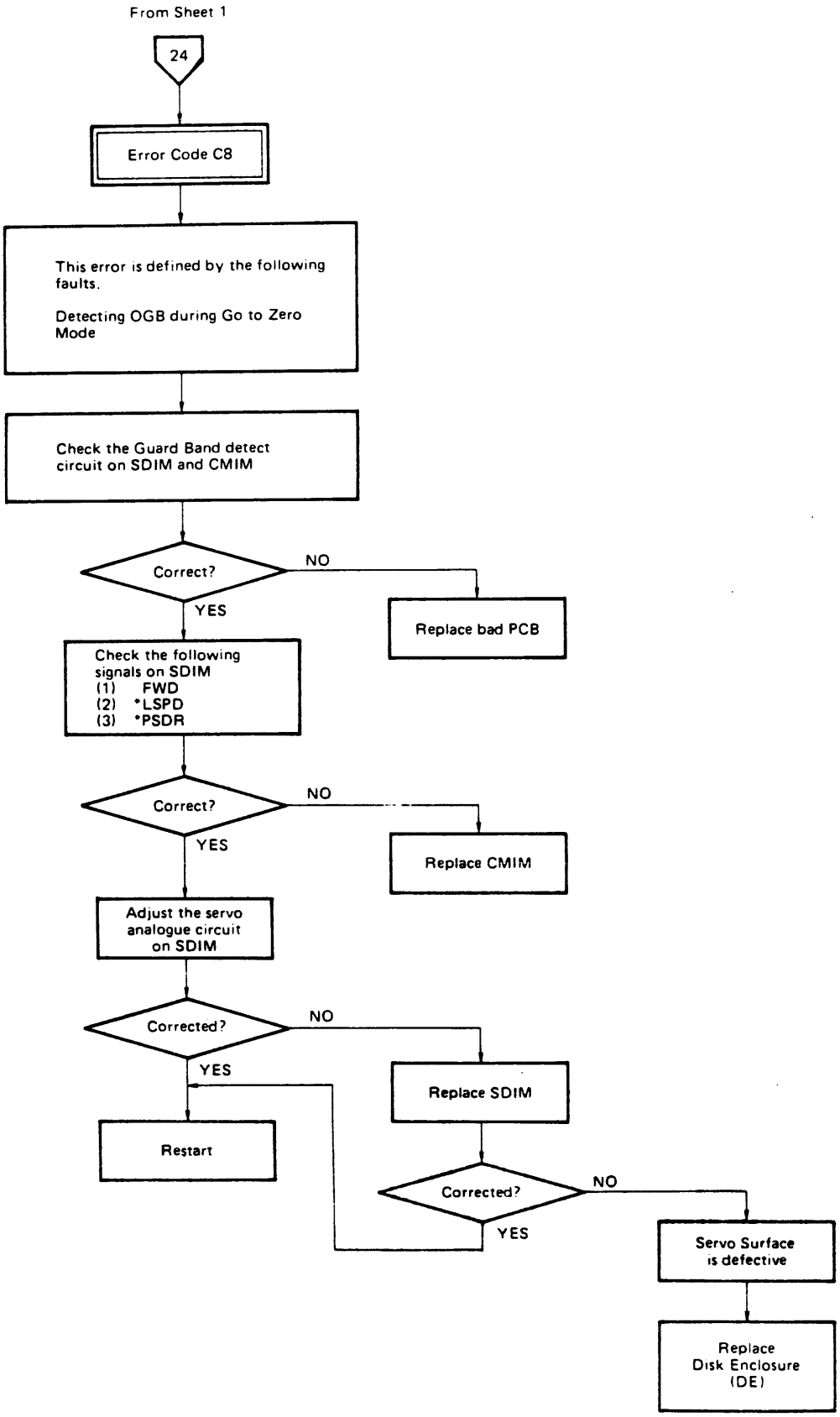


Figure 5-4-3 Seek Error Flow Chart (Sheet 5 of 7)

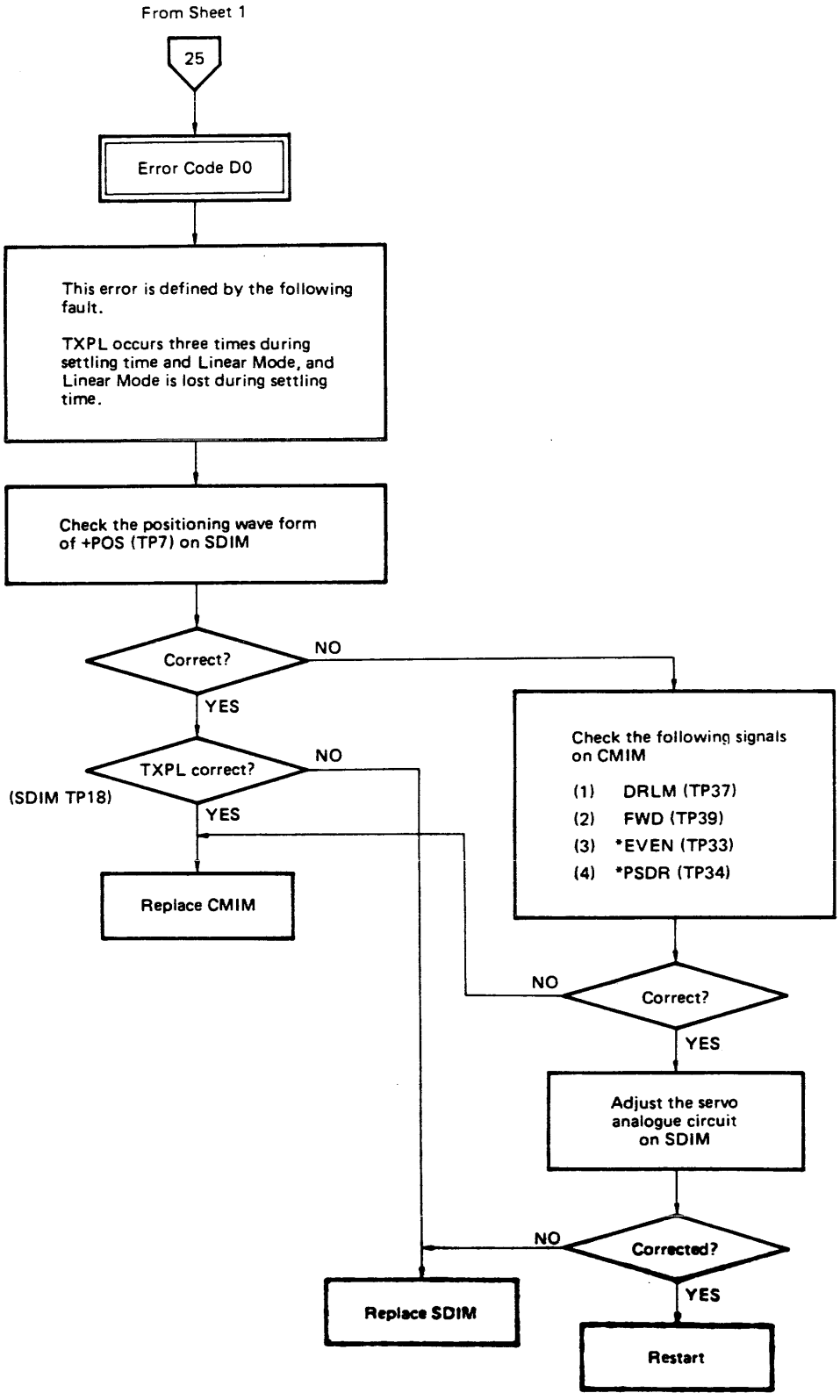


Figure 5-4-3 Seek Error Flow Chart (Sheet 6 of 7)

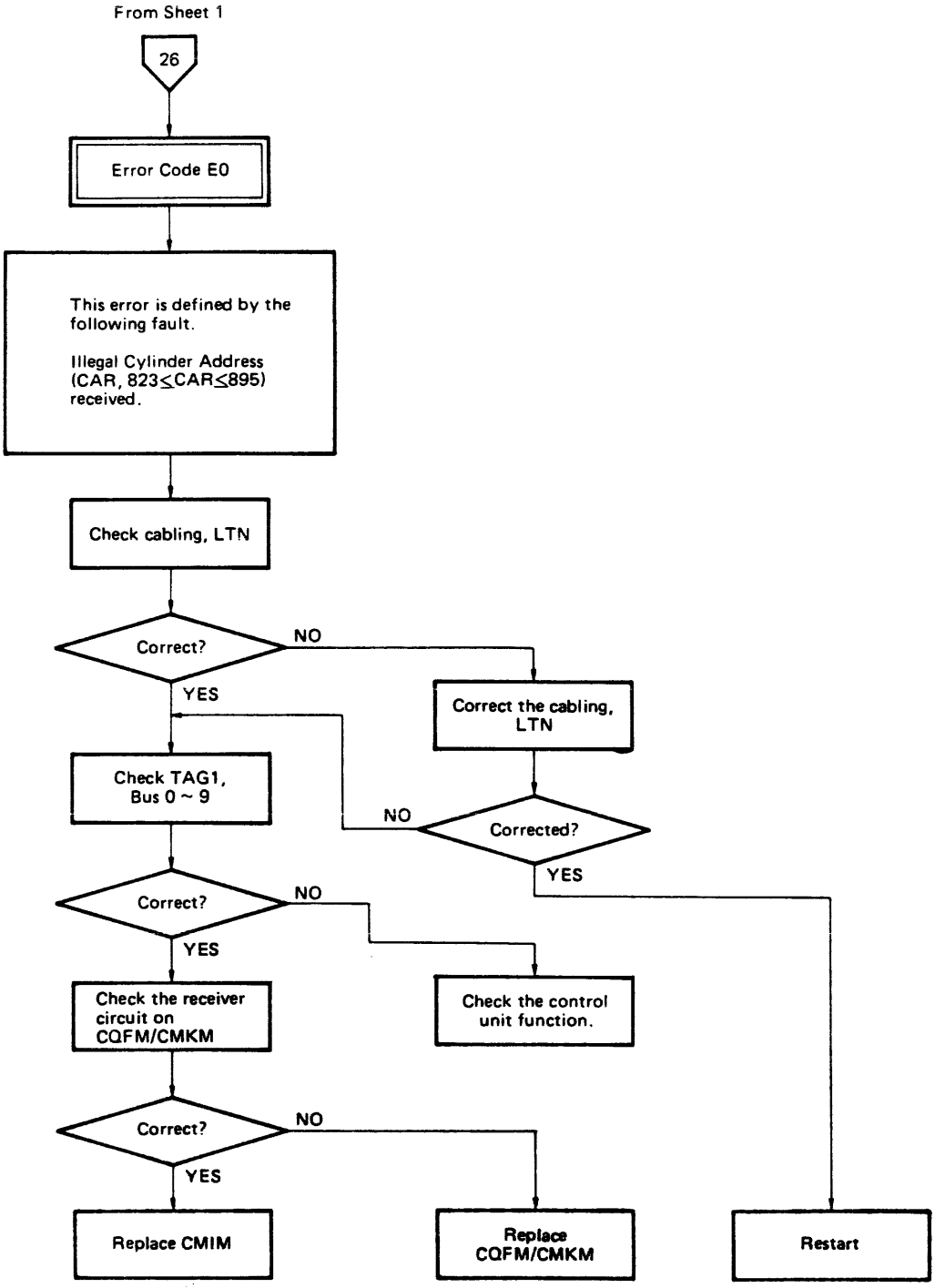
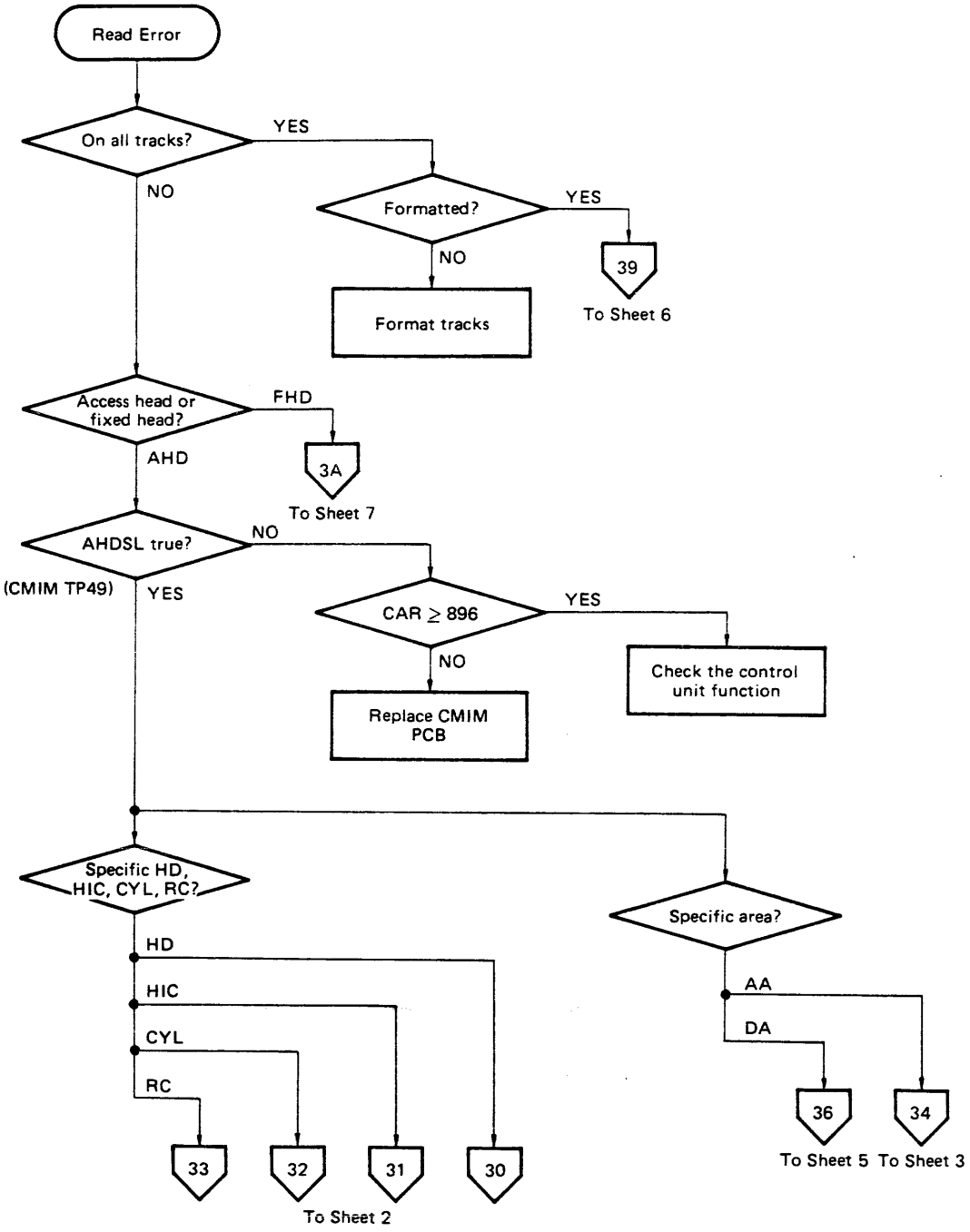
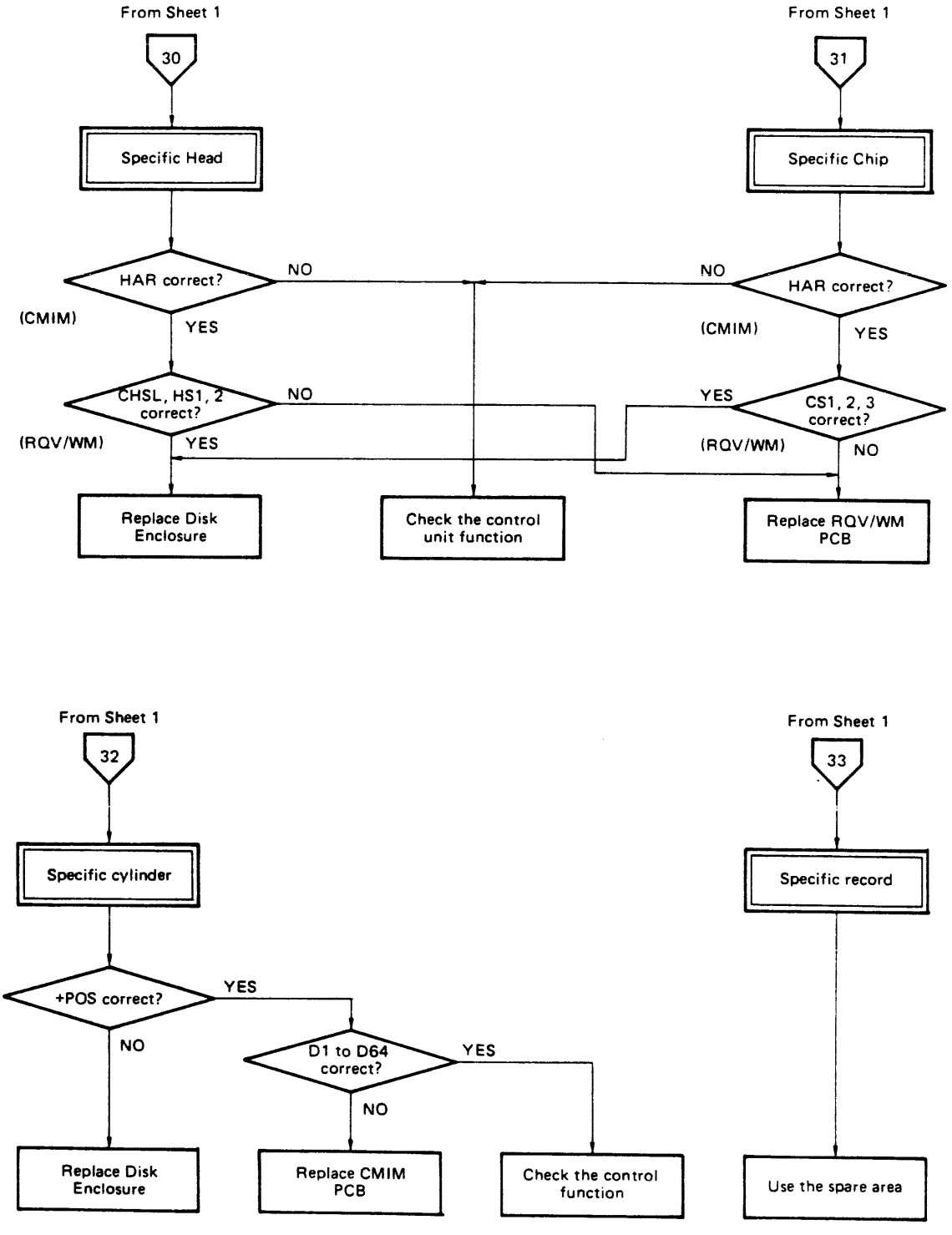


Figure 5-4-3 Seek Error Flow Chart (Sheet 7 of 7)



Note: AA is Address Area.
DA is Data Area.

Figure 5-4-4 Read Error Flow Chart (Sheet 1 of 7)



Note: One chip has four heads.

CS 1: HD0 to 3
2: HD4 to 7
3: HD8 and 9

Figure 5-4-4 Read Error Flow Chart (Sheet 2 of 7)

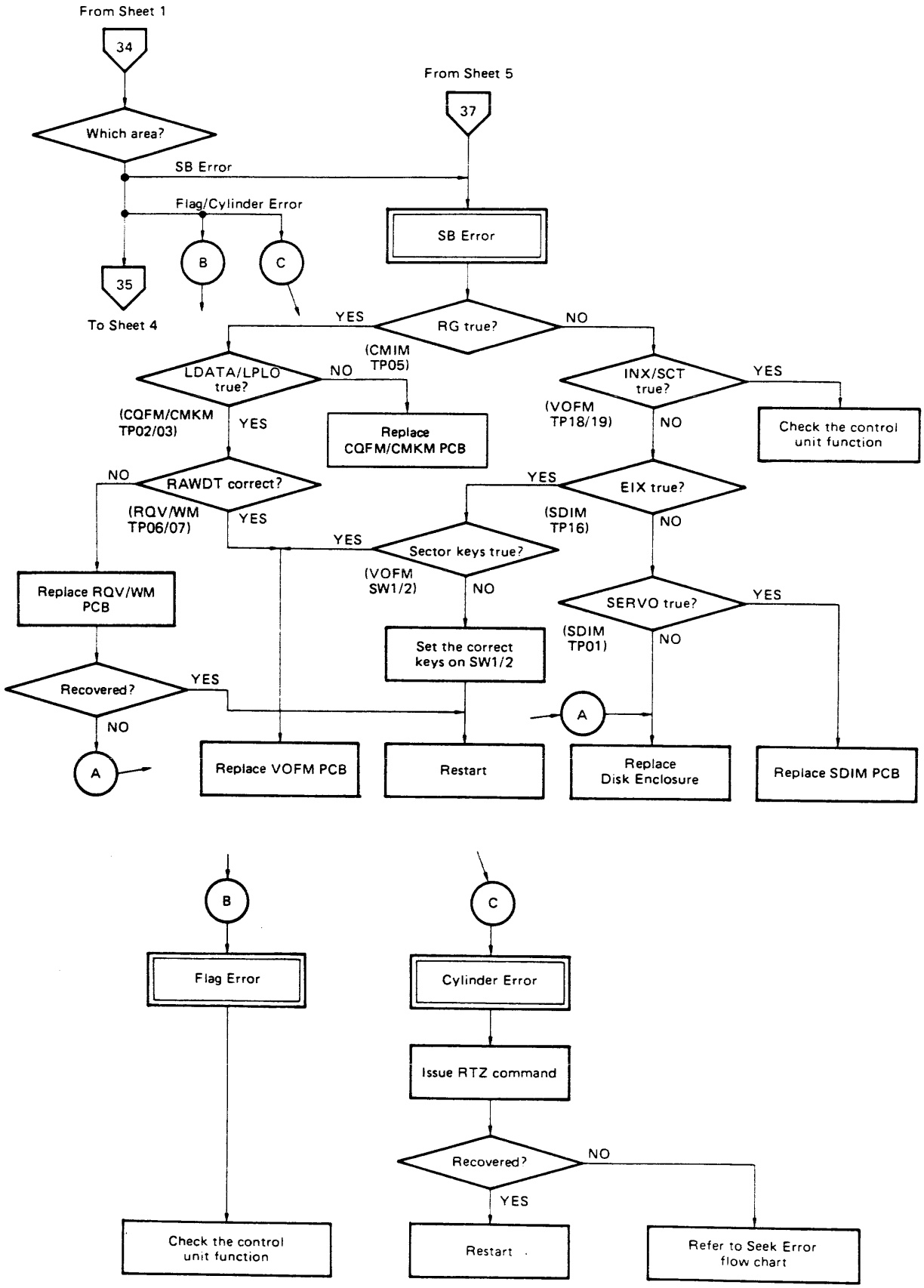


Figure 5-4-4 Read Error Flow Chart (Sheet 3 of 7)

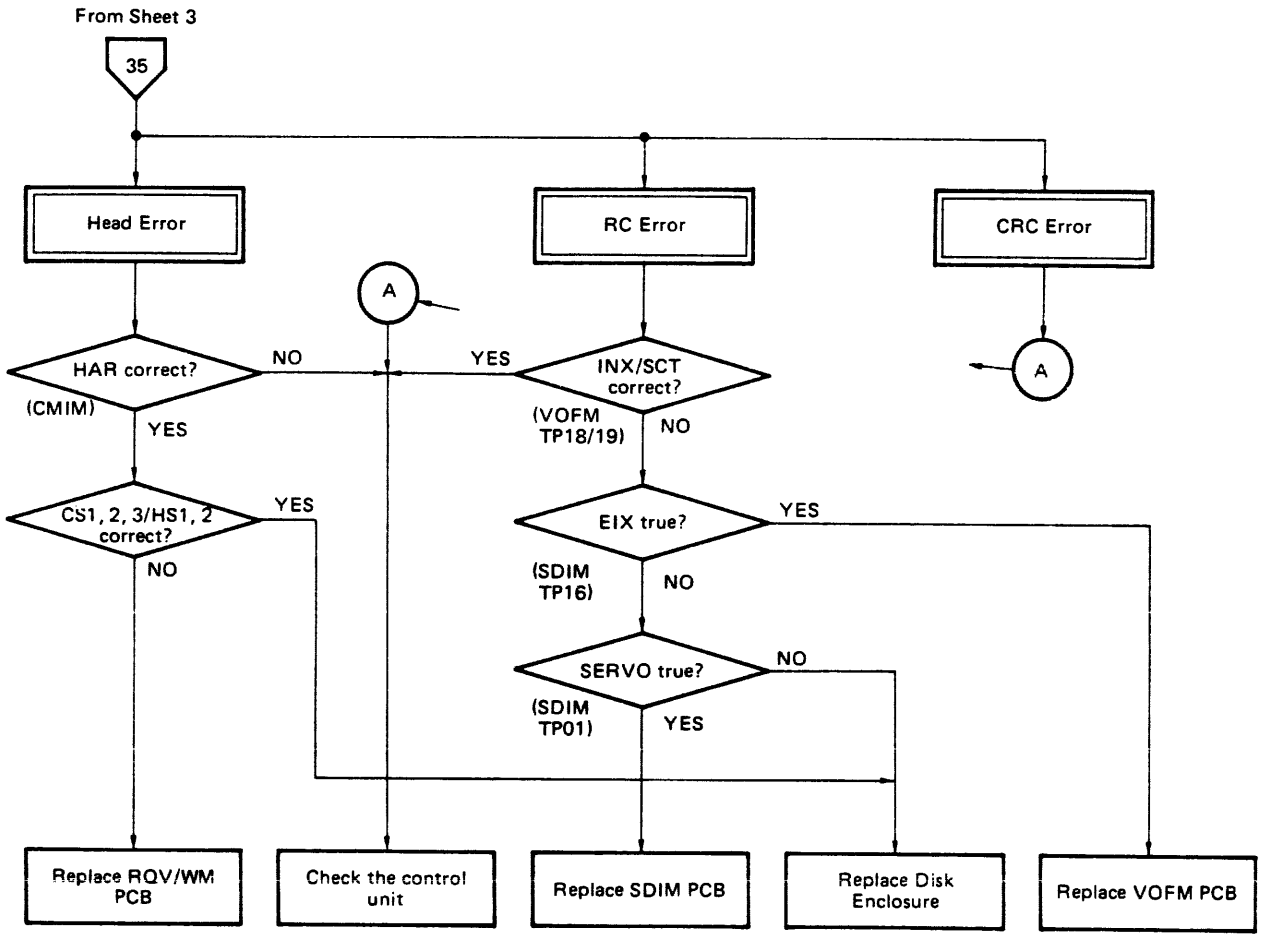


Figure 5-4-4 Read Error Flow Chart (Sheet 4 of 7)

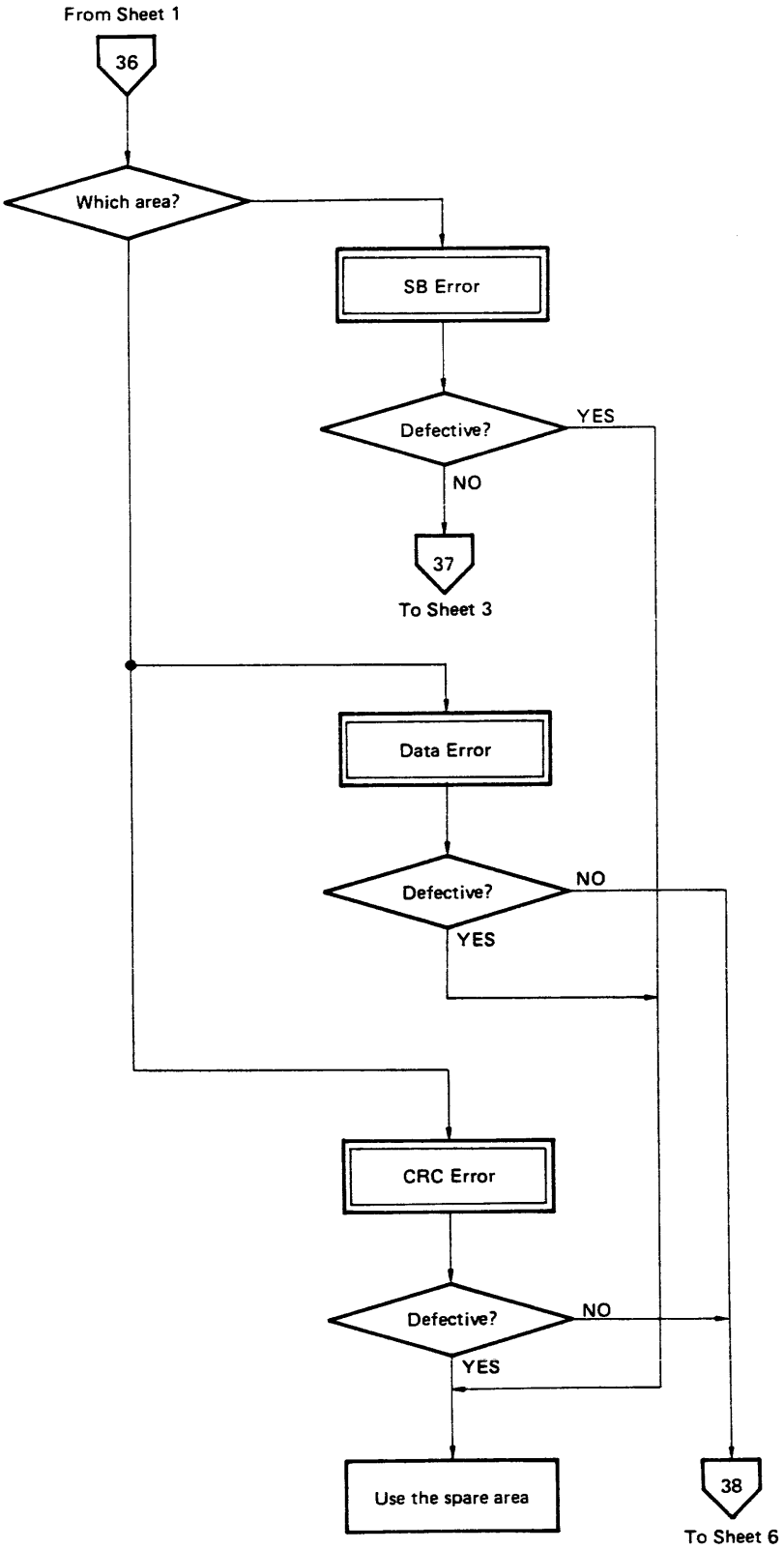
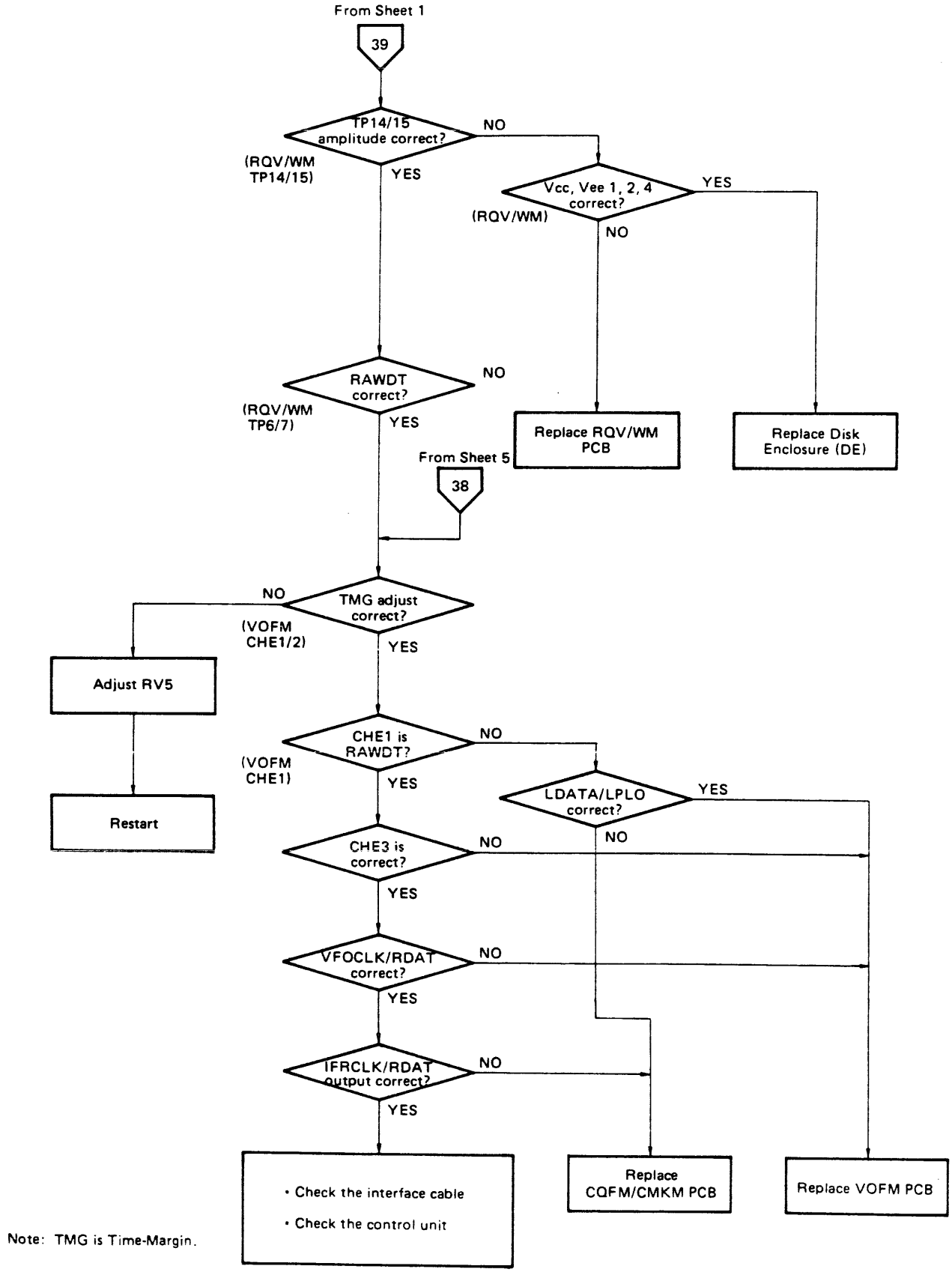


Figure 5-4-4 Read Error Flow Chart (Sheet 5 of 7)



Note: TMG is Time-Margin.

Figure 5-4-4 Read Error Flow Chart (Sheet 6 of 7)

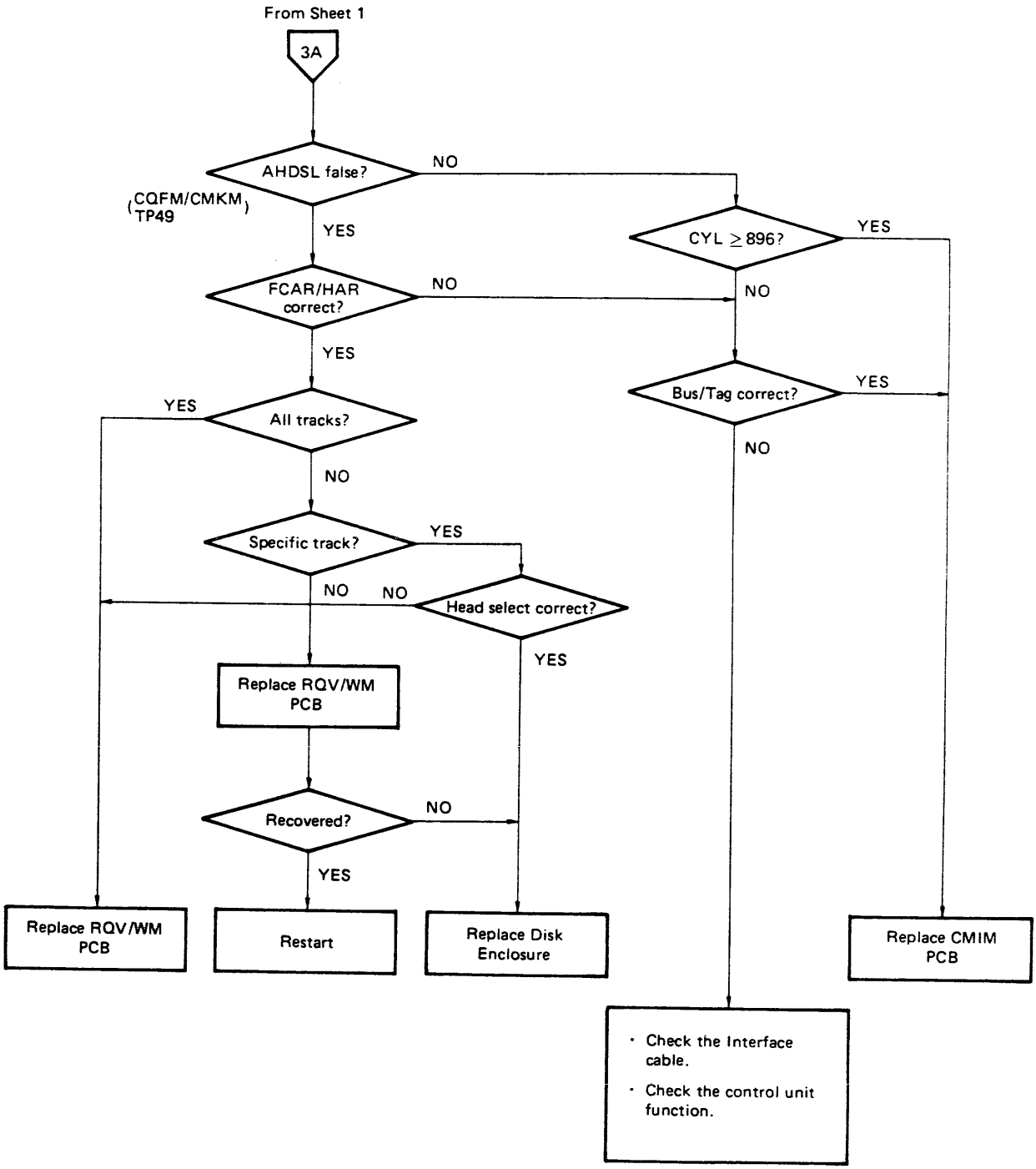


Figure 5-4-4 Read Error Flow Chart (Sheet 7 of 7)

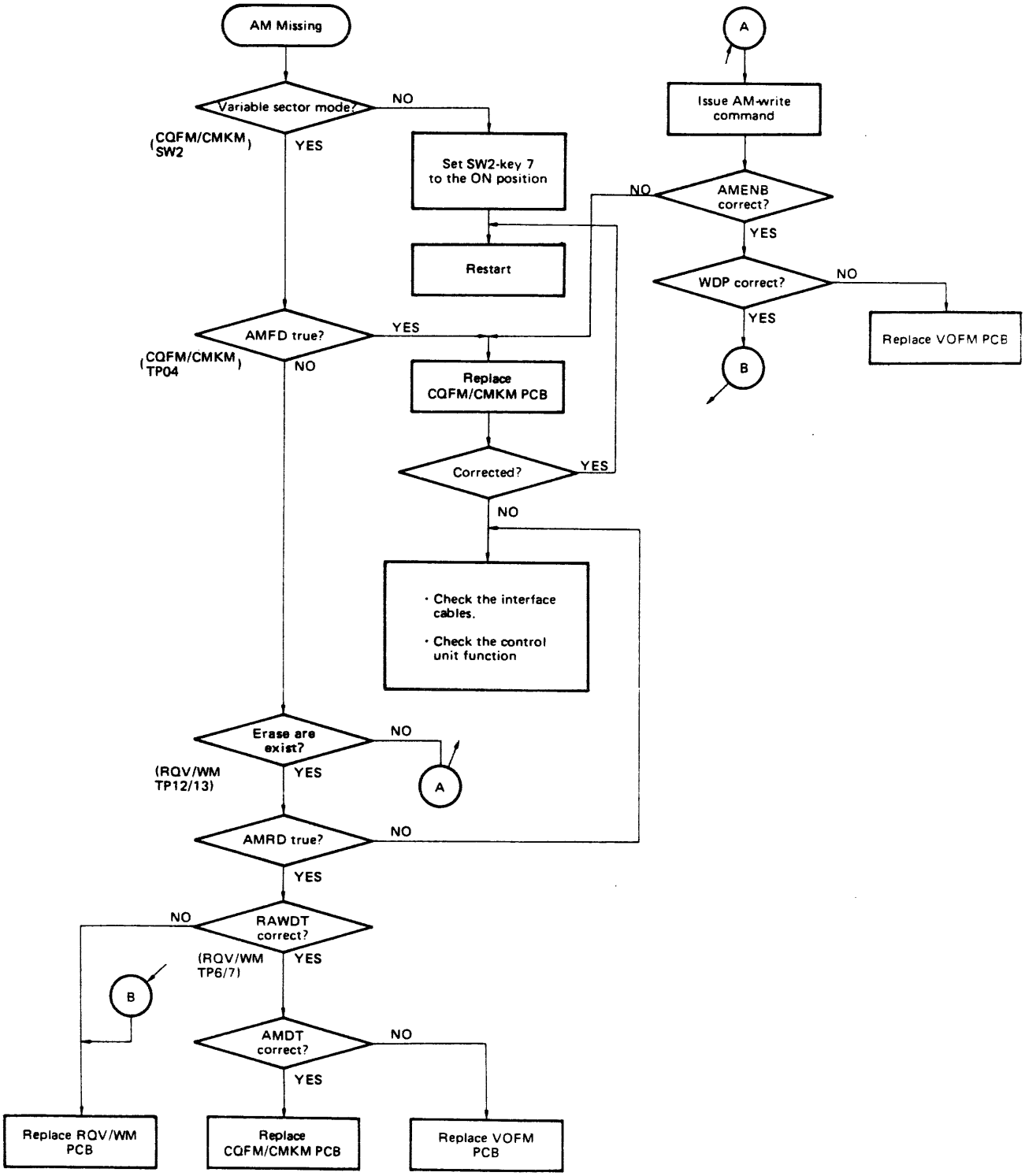


Figure 5-4-5 AM Missing Flow Chart

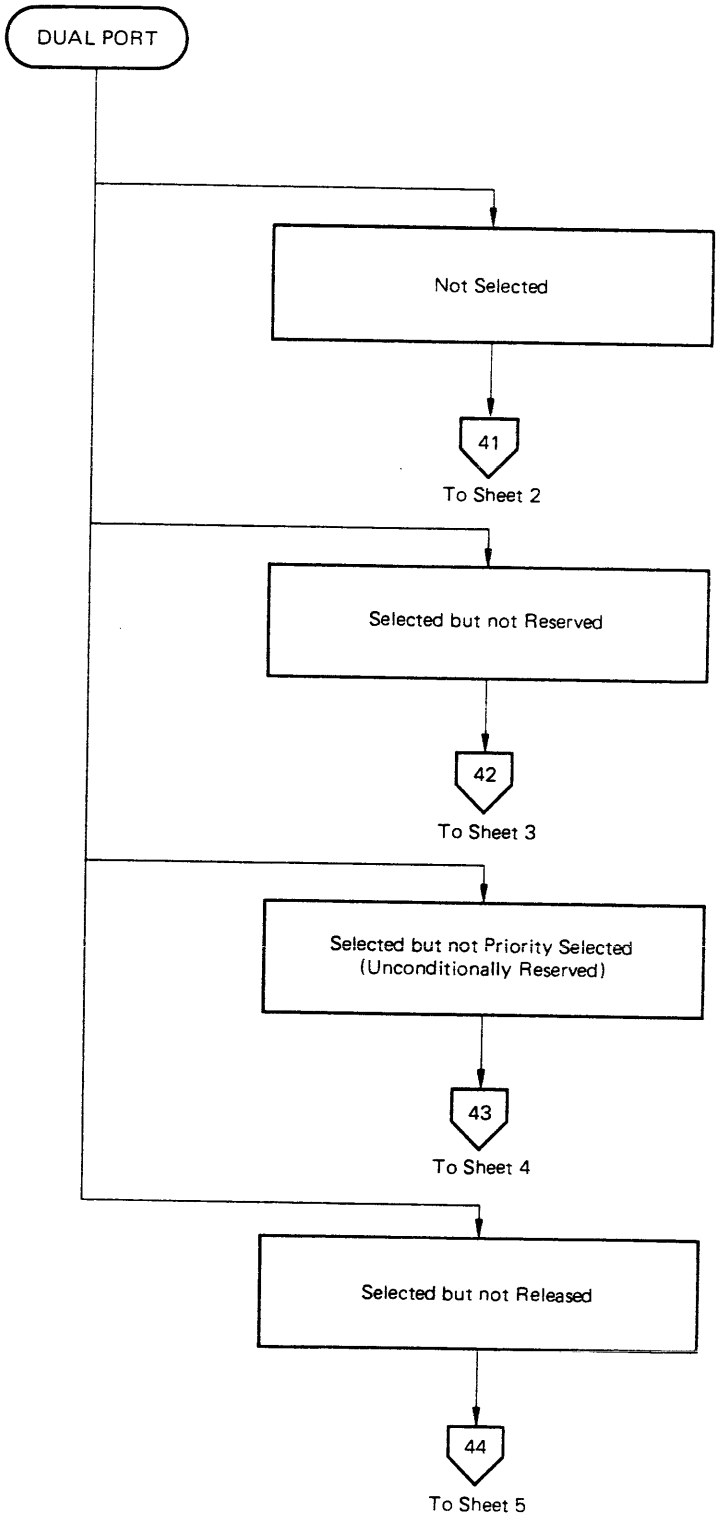


Figure 5-4-6 Dual Port Malfunction Flow Chart (Sheet 1 of 5)

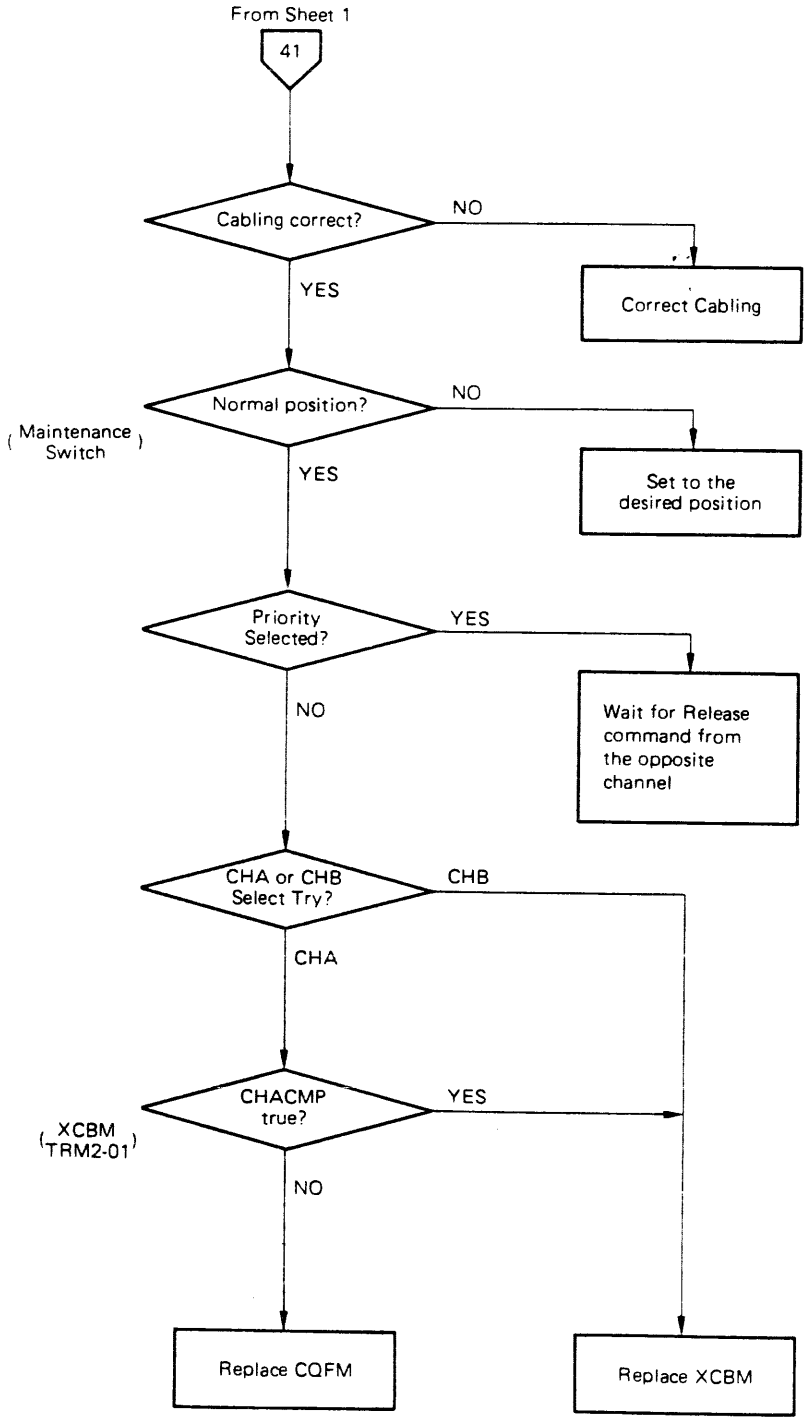


Figure 5-4-6 Dual Port Malfunction Flow Chart (Sheet 2 of 5)

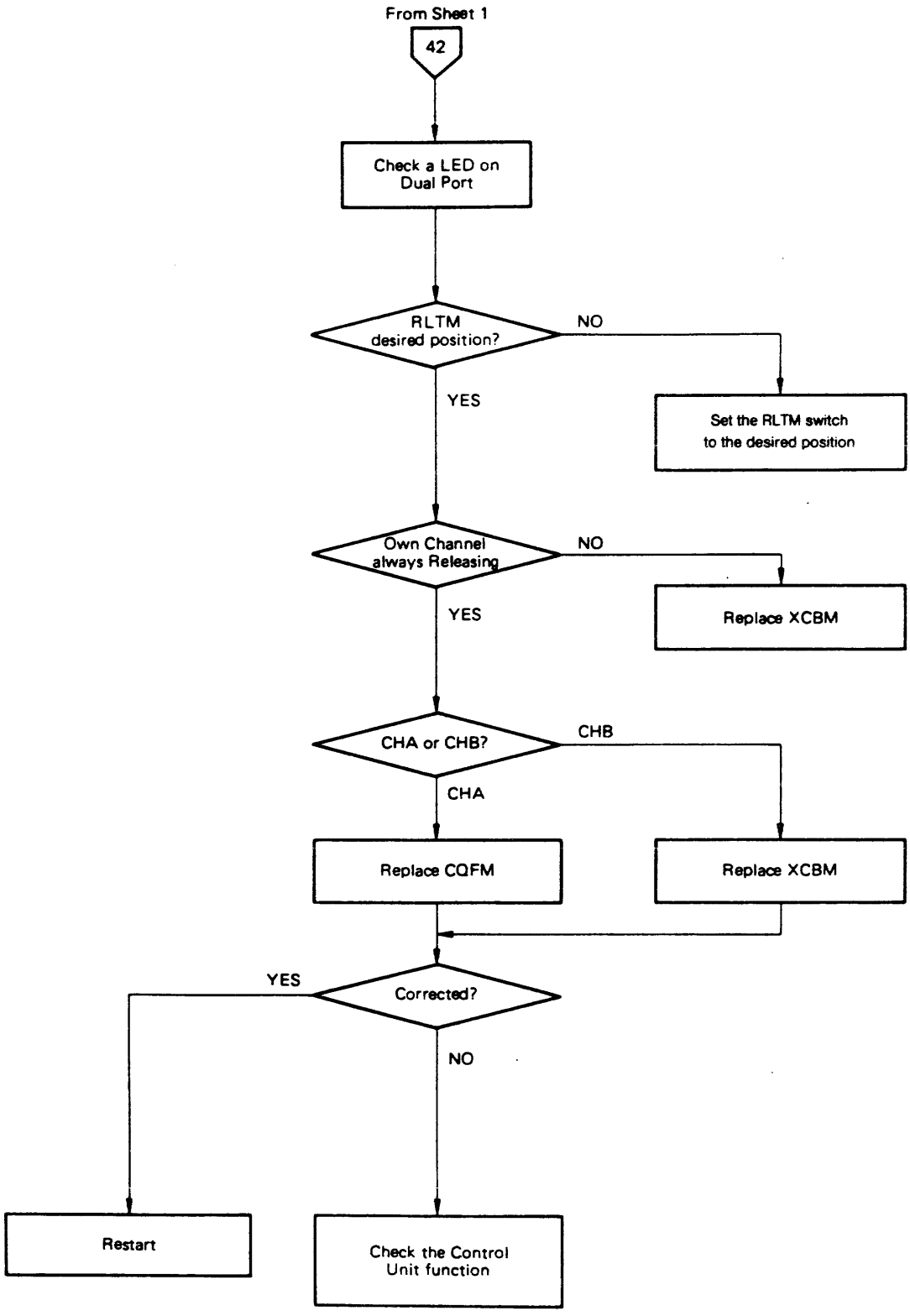


Figure 5-4-6 Dual Port Malfunction Flow Chart (Sheet 3 of 5)

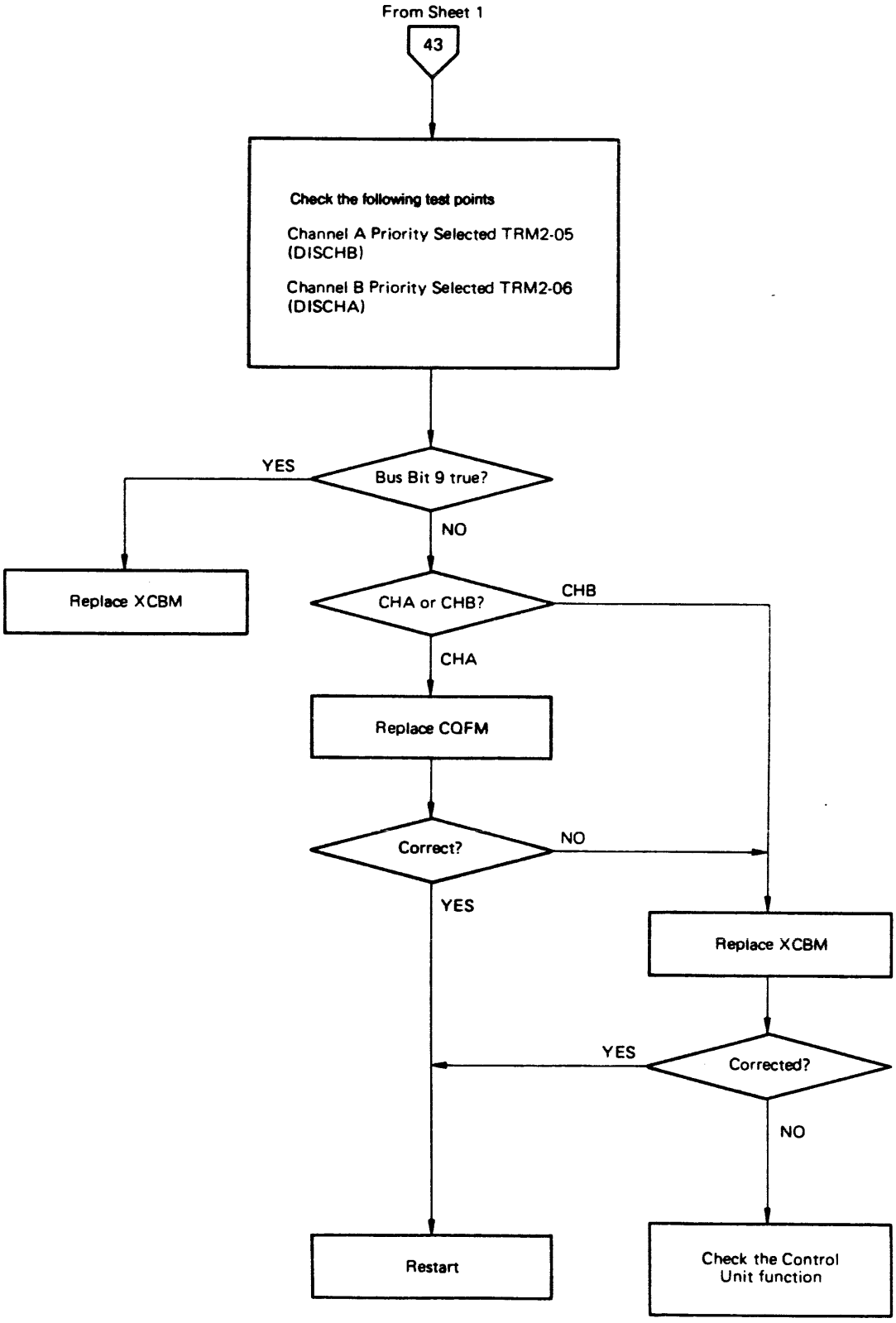


Figure 5-4-6 Dual Port Malfunction Flow Chart (Sheet 4 of 5)

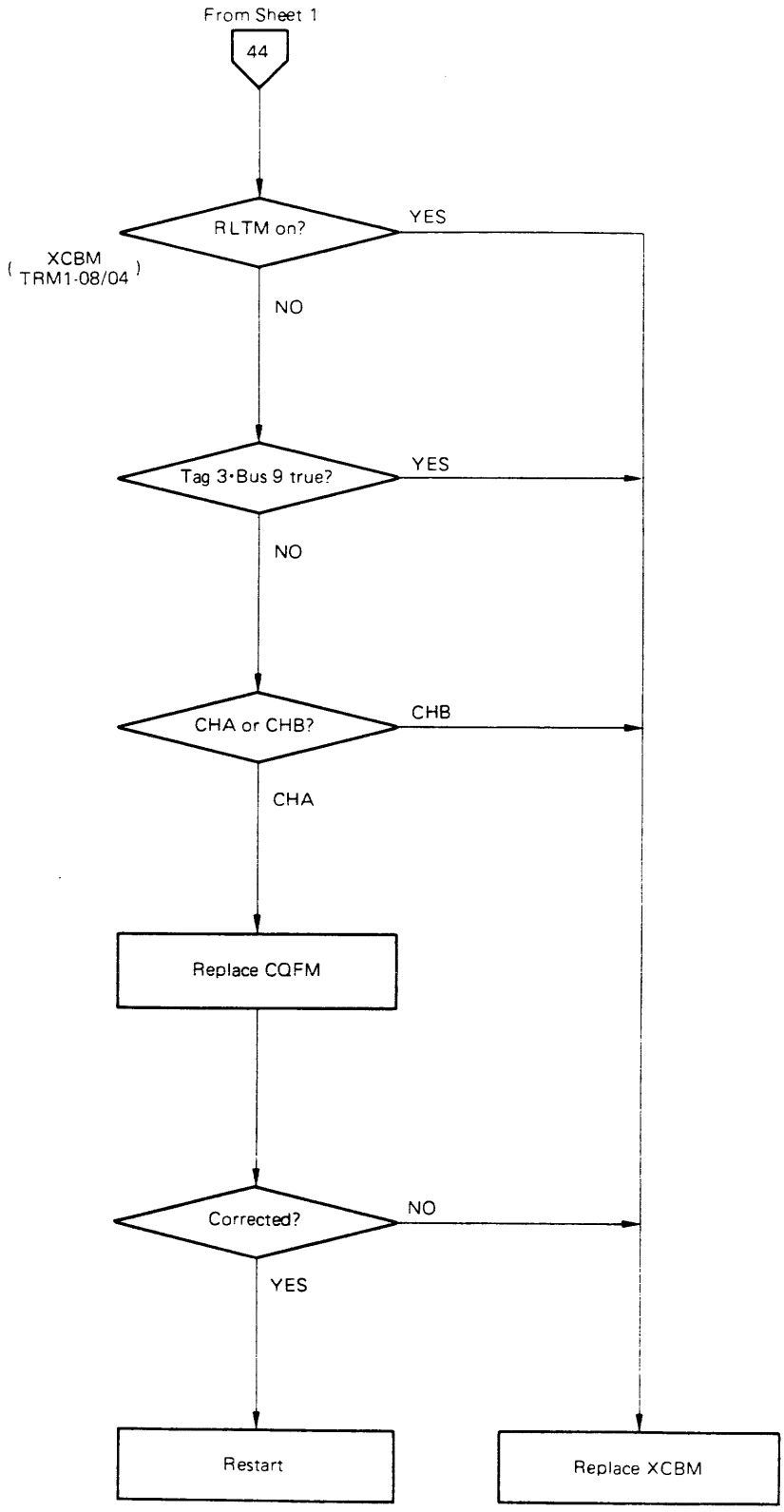


Figure 5-4-6 Dual Port Malfunction Flow Chart (Sheet 5 of 5)

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