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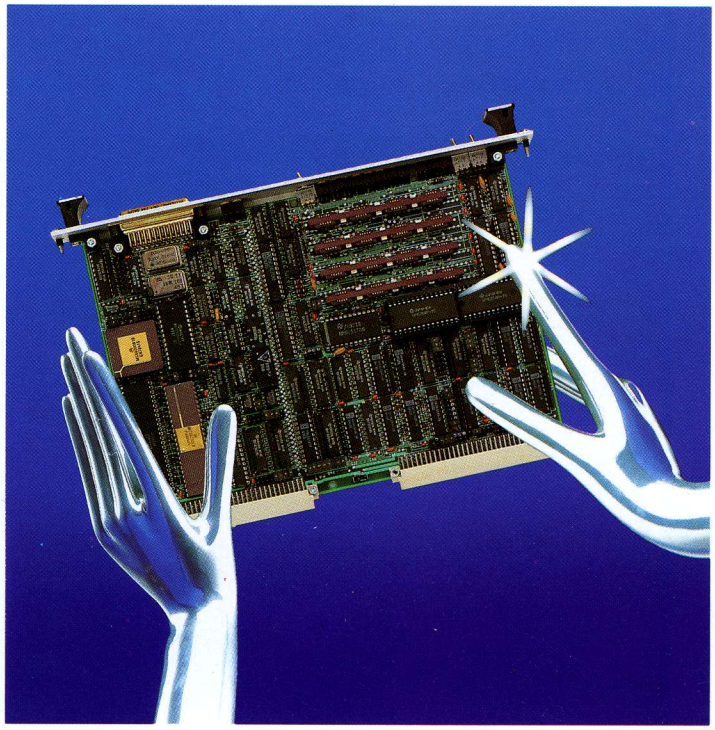
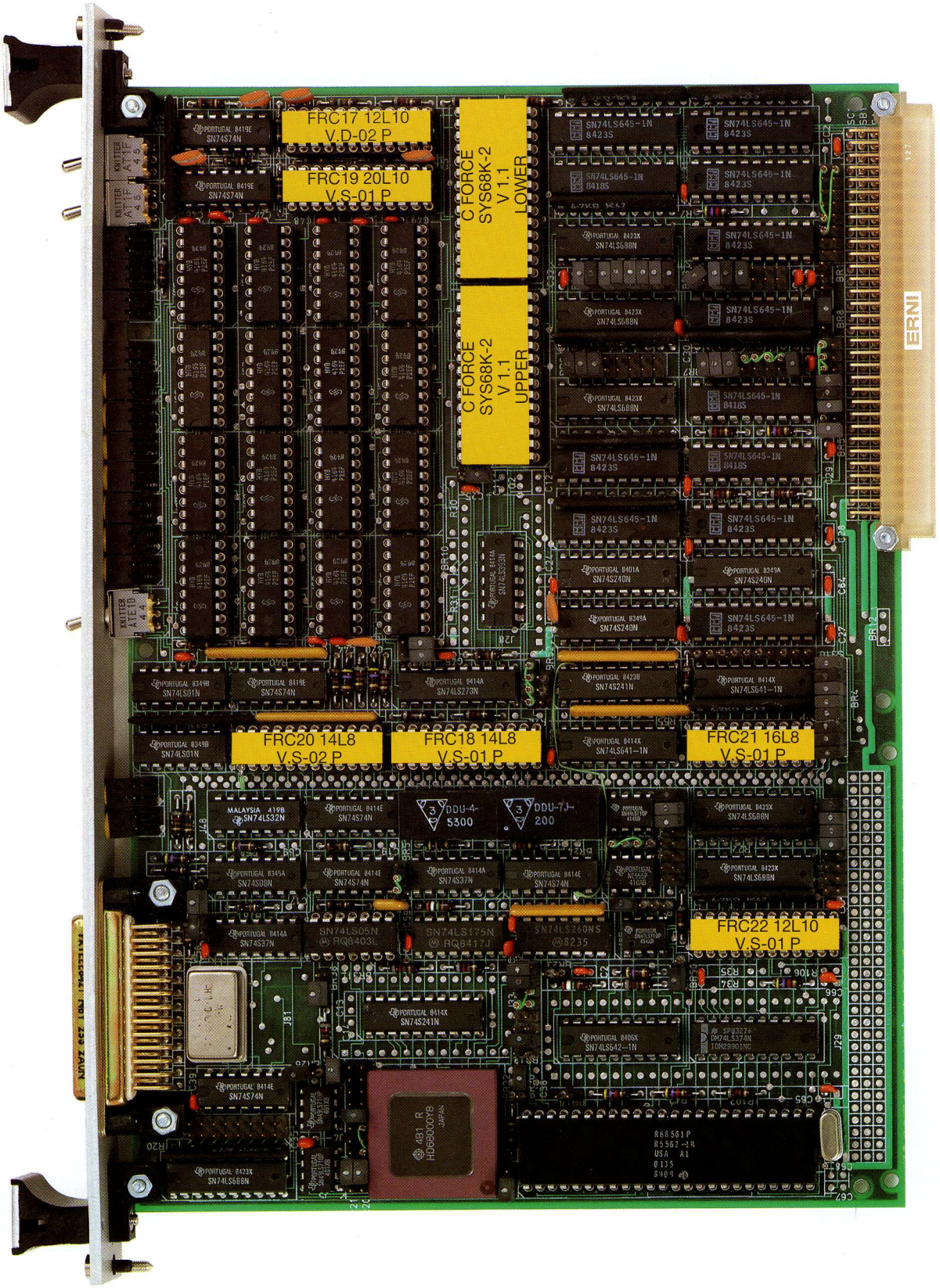


System 68000 VME
SYS68K/CPU-2/2D

High Performance Multi-Processor CPU Board


FRC17 12L10
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FRC19 20L10
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C FORCE
SYS68K-2
V 1.1
LOWER
C FORCE
SYS68K-2
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UPPER
ERNI
FRC20 14L8
V.S-02 P
FRC18 14L8
V.S-01 P
FRC21 16L8
V.S-01 P
FRC22 12L10
V.S-01 P

General Description - CPU-2D

The SYS68K/CPU-2 D board is a high performance low cost process controller card based on the powerful 68000 CPU and the VMEbus. It contains the 68000 in a Pin Grin Array (PGA) with a clock frequency of 8 MHz.

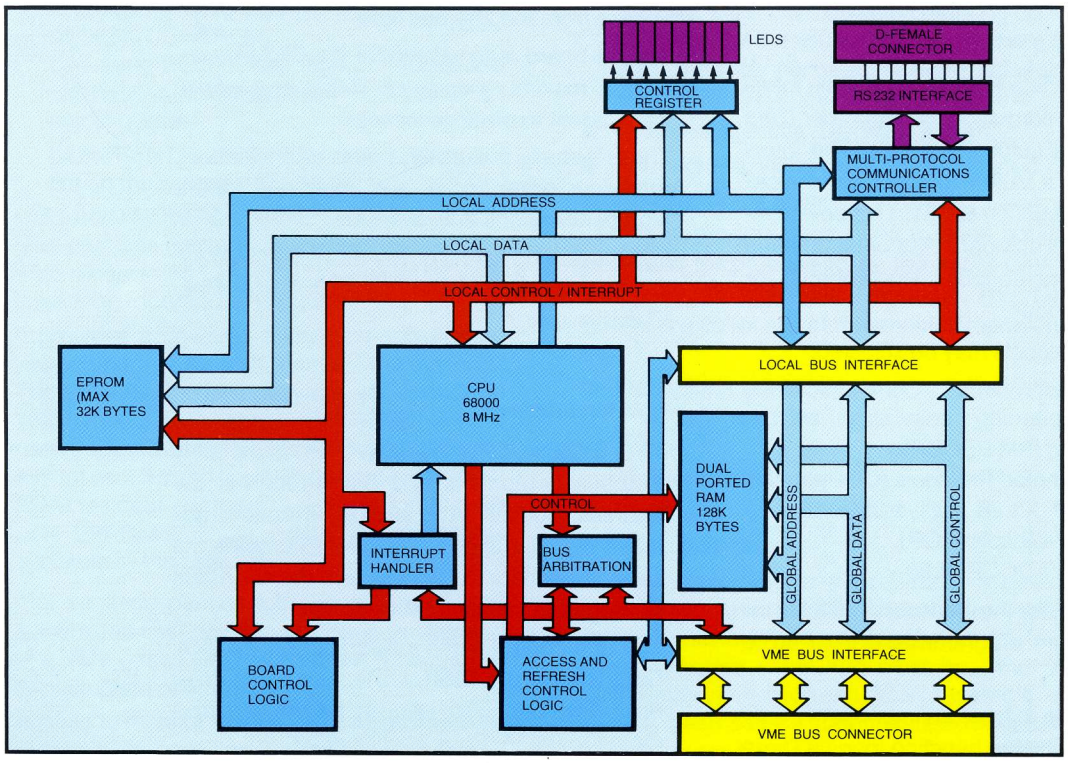
The board contains a Dual Ported RAM array (128k byte) for high speed real time and multiprocessing applications. The Multi-Protocol Communications Controller (MPCC) used on the board is able to handle all standard byte or bit oriented protocols.

For debug and selftest capabilities the board contains two 28 pin sockets for EPROM's. The firmware on-board (2 EPROM's 2764) contains memory initialization, memory test, memory modify and verify instructions. In addition a line by line assembler/disassembler with the complete 68000 instruction set.

SYS68K/CPU-2D Features

- 68000 in Pin Grid Array (8 MHz)
- Full VMEbus compatible (A24 : D16, A16 : D16)
- 128k bytes of Dual Ported Memory
- 16k bytes of firmware in EPROM (2x2764)
- Multi-protocol communication controller building a RS232 interface
- Software programmable baud rate (50 – 38400 Baud)
- Synchronous, asynchronous, isochronous mode with full or half duplex and with or without parity check
- Selectable base address via jumpers for the Dual Ported RAM, the I/O, and the EPROM areas
- On/off-board interrupt handling fully VME bus compatible
- Slave bus arbitration
- Multi-processor capability
- RESET, ABORT and HALT function switches
- RUN, LOCAL and BUS MASTER STATE indicators

BLOCK DIAGRAM OF THE SYS68K/CPU-2D



CPU-2/2D Monitor Description

Features of the resident Monitor package:

- EPROM resident system monitor/debugger
- More than 30 commands for debug, up/downline load
- One-line assembler/disassembler for assembly language program development
- Full speed execution of system and user programs operating in the VMEbus oriented monoboard microcomputer system
- Terminal capability for up/downline load from another development system or any host computer
- Powerful software and system debug command set allow access to all VME modules plus the full 16M byte direct address range of the VME system bus
- Includes all required installation and operation documentation
- Access to monitor resources via vectorized entries and TRAP 14 calling sequence
- Start of user application program or optional software by command

Optional Operating Software

A variety of optional software is available for the SYS68K/CPU-2, i. e.

- SYS68K/PDOS
  Realtime, multitasking, operating system with high flexibility. Pascal compiler optional.
- SYS68K/COHERENT
  Operating System with high portability and capabilities including C-compiler and a variety of utilities.
  COHERENT is UNIX ™ version 7 compatible on the source code base.

CPU-2/2D MONITOR is an EPROM based resident package ready for immediate use with the VME monoboard CPU-2/2D as well as for VME based microcomputer products.

It provides a powerful evaluation and system debugging tool for VME based CPU systems. The EPROM resident package will operate in 16K bytes of ROM space. CPU-2/2D Monitor uses the first 1024 words of RAM storage for interrupt vectors and temporary storage. The EPROM resident package is delivered in two 8K byte EPROM's. Table 1 lists the commands available to the user.

The package permits full speed execution of system and user developed programs operated in a VME based CPU system environment under complete operator control.

Access to monitor resources and configuration control is given by vectorized system entries and a TRAP 14 calling sequence. The MONITOR may be utilized with the VME based CPU monoboard microcomputer SYS68K/CPU-2/2D in a stand-alone environment with only a user provided standard RS232C asynchronous ASCII terminal.

Assembler/ Disassembler Capability

The on-board assembler does not allow line numbers and labels; however, it is a powerful tool for creating, modifying, annd debugging 68000 code. The on-board assembler processes each line of a program as an individual unit. Therefore the capabilities of the assembler is more restricted:

- Label and line numbers are not used. Labels are commonly used to reference other lines and locations in a program.
  The one-line assembler has no knowledge of other program lines and, therefore, cannot make the required association between a label and the label definition located on a separate line.
- Source lines are not saved. – In order to read back a program after it has been entered, the machine code is disassembled and then displayed as mnemonic and operands.
- Limited error indication.– The one-line assembler will show a question mark (?) under the portion of the source statement where an error probably occurred, or will display the word »ERROR« or another short message.
- Only one directive (DC.W) is accepted.
- No macro handling capability is included.
- No conditional assembly is used.

The symbolic language used to code source programs for processing by the assembler is called 68000 assembly language. This language is a collection of mnemonics representing:

- Operations
  – 68000 machine instruction operation codes
  – Directive (pseudo-op)
- Operators
- Special symbols

A source program is a sequence of source statements arranged in a logical way to perform a predetermined task. Each source statement occupies a line and must be either an executable instruction or a DC.W assembler directive. Each source statement follows a consistent source line format.

Each interrupt signal of the VMEbus can be enabled or disabled on the board so that in a multi-processor environment several interrupt signals may be reserved for each CPU board individually.

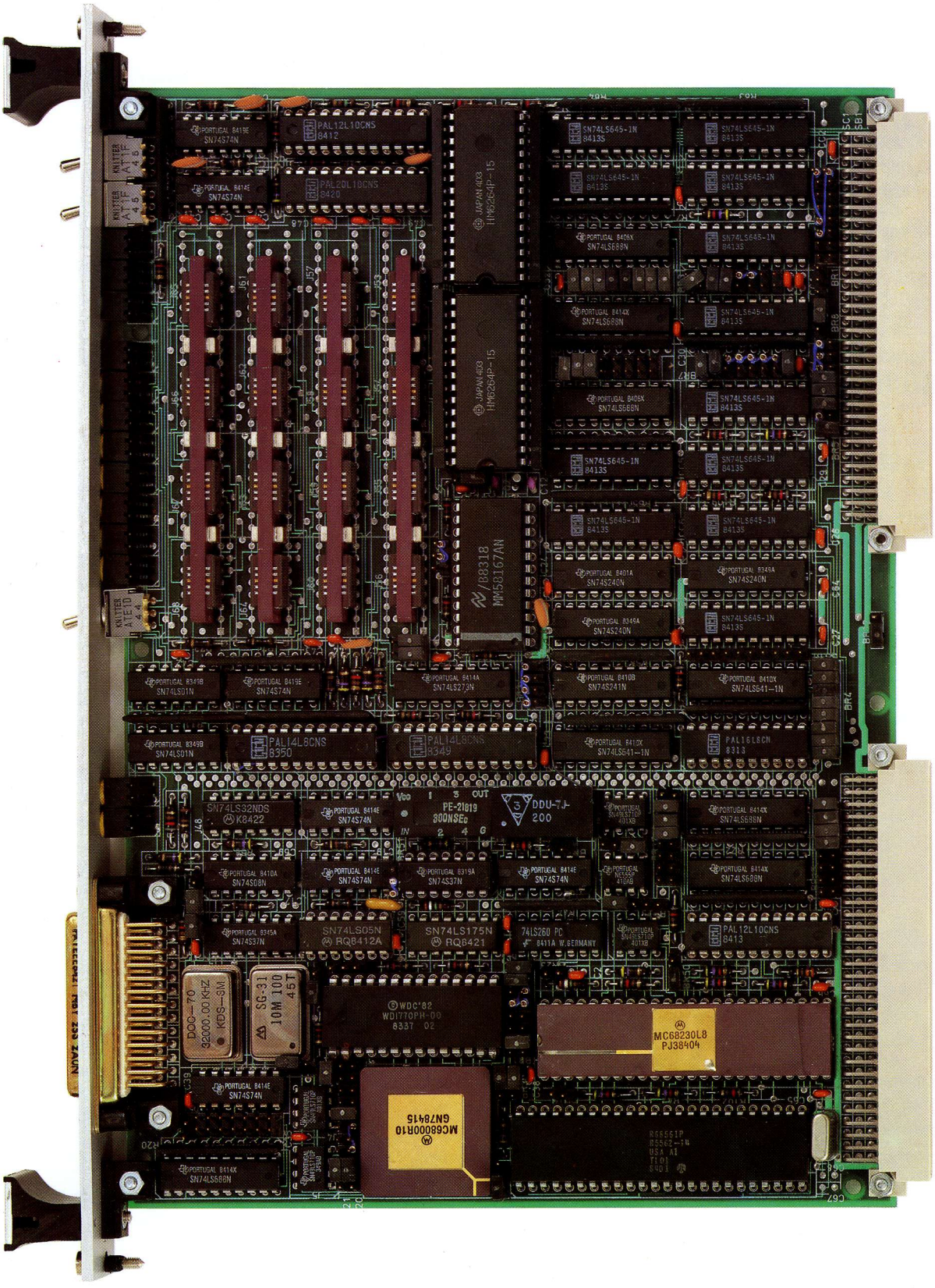
The on-board interrupt sources are handled individually offering transparent handling and self test capabilities.

For multi-master environments the board contains full slave bus arbitration on one of the four selectable daisy chain levels (specification: release on request). The board works completely asynchronous to the VMEbus and the bus master state so that on-board transfers to/from the I/O from the EPROM area and to/from the Dual Ported RAM can be initiated if another VMEbus board is the current bus master.

To provide full address decoding, all addresses which are not on-board (DPR, EPROM, I/O) are decoded as off-board addresses. This allows configuration of contigous memory space of RAM on a selected address range by means of an additional RAM board.

CPU-2/2D MONITOR COMMAND Summary

COMMAND	DESCRIPTION
BF <address1> <address2<data> <CR>	Block Fill memory – from add1 through add2 with data
BM <address1> <address2> <address 3> <CR>	Block Move – move from add1 through add2 to add3
BR[<address>[; <count>]....]<CR>	Set/display Breakpoint
BS <address1> <address2> <data> <CR>	Block Search – search add1 through add2 for data
BT <address1> <address2> <CR>	Block Test of memory
DC <expression> <CR>	Data Conversion
DF <CR>	Display Formatted registers
DU[n] <address1> <address2>[<string>]<CR>	Dump memory to object file
GO[<address>]<CR>	Execute program
GD[<address>]<CR>	Go direct
GT <address> <CR>	Exec prog: temp breakpoint
HE <CR>	Help; display monitor commands
LO[n][; <options>]<CR>	Load Object file
MD <address>[<count>]<CR>	Memory Display
MM <address>[<data>][;<options>]<CR>	Memory Modify
MS <address> <data1> <data2>....<CR>	Memory Set – starting at addr with data1, data2,..
NB[<address>....]<CR>	Remove Breakpoint
OF <CR>	Offset
PF[n]<CR>	Set/display Port Format
RM <CR>	Register Modify
TR[<count>]<CR>	Trace
TT <address> <CR>	Trace: temp. breakpoint
US	Start User Program
VE[n][=string>]<CR>	Verify memory/object file
.AO – .A7[<expression>]<CR>	Display/set address register
.DO – .D7[<expression>]<CR>	Display/set data register
.RO – .R6[<expression>]<CR>	Display/set offset register
.PC[<expression>]<CR>	Display/set program counter
.SR[<expression>]<CR>	Display/set status register
.SS[<expression>]<CR>	Display/set supervisor stack
.US[<expression>]<CR>	Display/set user stack
MD <address>[<count>]; DI<CR>	Disassemble memory location
MM <address>; DI<CR>	Disassemble/Assemble memory location



General Description CPU-2

The SYS68K/CPU-2 board can be used as a single board computer, as well as in high performance multi-processor environments. This advanced version of the standard SYS68K/CPU-2D basically offers the same features as the standard version, including a dual ported memory storage array of up to 512k byte (standard 256k byte) and additional I/O devices.

The CPU-2 board is available with an 68010 CPU (8 MHz), which is software compatible to the standard 68000, and offers additional features, such as virtual memory management and enhanced error exception handling.

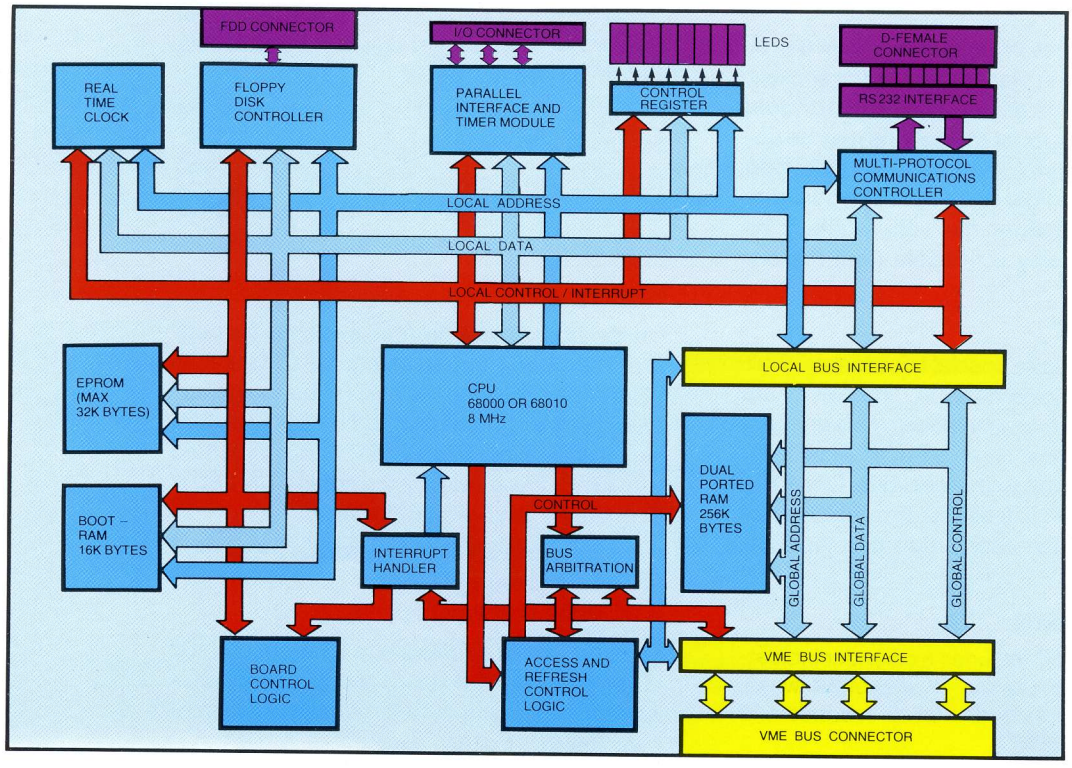
The parallel interface and timer device 68230 contains 24 bidirectional I/O lines and a 24 bit timer. For real time applications the Real Time Clock 58167A with date and time of day is used.

In addition, a Floppy Disk Controller module 1770 can control up to four different Floppy Drives with a Shugart compatible interface.

Additional Features of the SYS68K/CPU-2

- Processor 68000 (68010 optional) with 8 MHz clock frequency
- Dual Ported Memory with 256k bytes (512k bytes optional)
- Parallel Interface with 24 bidirectional I/O lines
- 24 bit Timer with 5 bit prescaler
- Real Time Clock with date and time of day
- 8 bit output register with 8 control LED's indicators on the front panel
- Floppy Disk Controller for up to 4 Floppy Disk Drives (Shugart compatible interface)
- All I/O interface devices are able to force interrupts

BLOCK DIAGRAM OF THE SYSY68K/CPU-2



Functional Description

Virtual Processor 68010

The 68010 CPU is a virtual machine software compatible to the standard 68000. Error exception handling is optimized. On occurrence of an error the program counter and the access address are stored on the stack for easy handling and diagnostic. Therefore the system software is able to correct even catastrophic failures, thus preventing system crashes. The processor clock frequency is 8 MHz for better performance in high speed real time applications.

Boot RAM

For easy system installation the Dual Ported RAM has a jumper selectable access address. For its exception vectors the CPU needs RAM space from address $8 to $3FF. SYS68K/CPU-2 provides a fast static RAM for this vector table and additional space for the stack pointer and special I/O buffer registers.

To provide high speed real time capabilities, the 16k byte boot RAM does not require any wait state for a read or write access.

Dual Ported RAM

In the advanced version SYS68K/CPU-2, the memory space of the DPR is default expanded to 256k bytes.

The board provides variable insertion of 64k or 256k bit DRAM's in stacked dual inline sockets or single inline chip carrier modules. Therefore the capacity for special apllications may be upgraded to 512k bytes. Parts of the DPR can be configured via jumper to become a global memory accessible from the bus, whereas as other parts are only accessible from the on-board CPU.

Parallel I/O (PI/T)

The board contains a special I/O interface (PI/T 68230) with 24 bidirectional I/O lines which are accessible via the second 96 pin male connector. A special jumper can enable the 24 bit timer to drive an interrupt to the local bus. Clock frequency of the PI/T is 8 MHz to provide high data throughputs for critical real time applications.

Real Time Clock (RTC)

The on-board RTC includes a calender indicating month, day of the month, day of the week, hours, minutes, seconds, 1/100 seconds and 1/1000 seconds.

An interrupt control register enables or disables the interrupt output of the RTC. A special jumper enables the interrupt signal to the local interrupt bus.

The RTC can be connected to the +5V standby power supply line of the VME bus or to a special line of the I/O connector. Therefore all the data patterns are stored during power failures or in power down mode.

Control Register (CR)

The board contains a 8 bit buffered latch which is used to define the Floppy Disk Drive to be enabled and serves as a general purpose output port.

The levels of the output lines are indicated by 8 LED's on the front panel. These LED's may be used as status and test indicators.

Floppy Disk Controller / Formatter (FDC)

The on-board FDC with its fully buffered output (48mA sink) contains a Shugart compatible interface for direct connection to Floppy Disk Drives. With the specially buffered output the drive (1–4) can be selected and controlled. The on-board controller WD1770 is able to control double and single sided drives in both double and single density modes.

For asynchronous handling, the FDC can force an interrupt to the local bus.

The interface lines are accessible via the I/O connector (flat cable 1:1 to the Floppy Drive Edge Connector).

Control Logic

On the board there are tree switches for control. The RESET button resets the CPU and all I/O devices. Pushing the ABORT button generates an interrupt on level 7. The STOP switch sets the CPU into HALT mode and is indicated with a red LED, otherwise the green RUN LED is lit when the CPU is in RUN mode.

For easy indication that the board is the current VMEbus master, a BUS MASTER LED indicator is provided on the front panel.

To abort invalid addresses, a time-out counter is provided on the board which generates a time-out from 8μs up to 2 ms (jumper selectable).

CPU-2/2D Monitor Description

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Specification	CPU-2D	CPU-2
Microprocessor	68000/8 MHz 68010/8 MHz on request (virtual processor)	68000/8 MHz 68010/8 MHz on request (virtual processor)
JEDEC Sockets	2 EPROM sockets for 2764 or 27128 (8k x 8 or 16k x 8)	2 EPROM sockets for 2764 or 27128 (8k x 8 or 16k x 8) 2 Static RAM's for stack operations 6264 (8k x 8)
I/O	Multi-Protocol Communications Controller with RS232 compatible interface	Multi-Protocol Communications Controller with RS232 compatible interface Parallel Interface (68230) with 24 bidirectional I/O lines and a 24 bit timer Real Time Clock with power back-up capability Floppy Disk Controller WD1770 with driver (up to 4 Floppy Drives), Shugart compatible interface Status is signaled by 8 LED's on the front panel
Dual Ported RAM	128k bytes of DPR 340ns (typ) write 340ns (typ) read	256k bytes of DPR 340ns (typ) write 340ns (typ) read 512k bytes of DPR optional 1 Mbyte of DPR optional
Bus	VMEbus Interface implemented A16 : D16 and A24 : D16 mode Slave bus arbitration Release on request Release after Time-out One Level Bus Arbiter Full interrupt handling Full multi-processing capabilities	VMEbus Interface implemented A16 : D16 and A24 : D16 mode Slave bus arbitration Release on request Release after Time-out One Level Bus Arbiter Full interrupt handling Full multi-processing capabilities
Included Firmware	Monitor firmware with line by line assembler/disassembler	Monitor firmware with line by line assembler/disassembler
Power Requirements	+5V/2.3A (typ) +5V/2.5A (max) +5V STDBY/0.05A (typ) +5V STDBY/0.07A (max) +12V/100mA (typ) +12V/200mA (max) −12V/100mA (typ) −12V/200mA (max)	+5V/2.8A (typ) +5V/3.2A (max) +5V STDBY/0.07A (typ) +5V STDBY/0.09A (max) +12V/100mA (typ) +12V/200mA (max) −12V/100mA (typ) −12V/200mA (max)
Operating Temperature	0 to + 50 degrees C	
Storage Temperature	−50 to + 85 degrees C	
Relative Humidity	0 − 95% (non condensing)	
Board Dimensions	Double Eurocard 234 x 160 mm (9.2 x 6.3 inch)	

Ordering Information:

SYS68K/CPU-2D Part No. 100220	68000, 8 MHz, 128KB DPR
SYS68K/CPU-2VD Part No. 100230	68010, 8 MHz, 128KB
SYS68K/CPU-2 Part No. 100200	68000, 8 MHz, 256 KB
SYS68K/CPU-2B Part No. 100202	68000, 10 MHz, 512KB
SYS68K/CPU-2F Part No. 100205	68000, 10 MHz, 1MB
SYS68K/CPU-2V Part No. 100210	68010, 8 MHz, 256KB
SYS68K/CPU-2VB Part No. 100212	68010, 10 MHz, 512KB
SYS68K/CPU-2VC Part No. 100213	68010, 10 MHz, 1MB
SYS68K/CPU-2/HUM Part No. 800002	Hardware User's Manual 1+2
SYS68K/CPU-2/SUM Part No. 800025	Software User's Manual

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