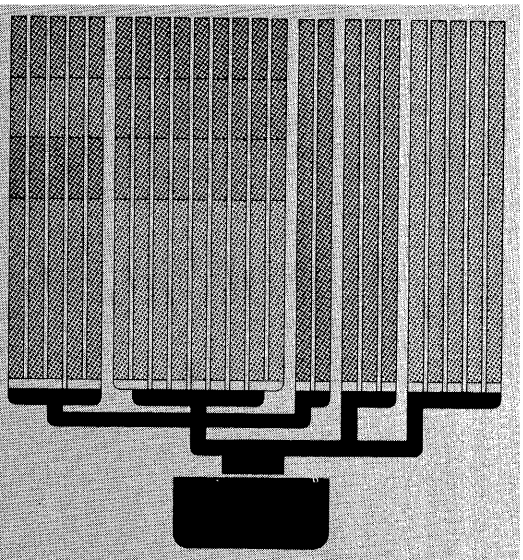


SSI
Monostable Multivibrator and Interface Circuits 9600 Series Data Sheets

The 9600 TTL elements are Monostable Multivibrator and Interface functions compatible with all SSI and MSI devices.

Full data sheets are provided on the Monostable series. Complete data sheets on the Interface series may be obtained from:

Fairchild Semiconductor
P.O. Box 880 A
Mountain View, California
94040

Attn: Distribution Services

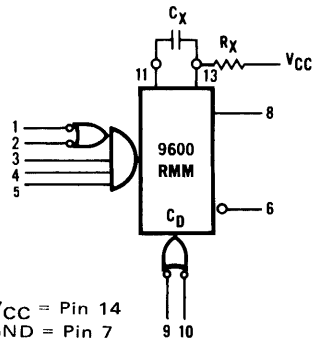
TTL/MONOSTABLE 9600

RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 9600 Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9600 has excellent immunity to noise on the V_{CC} and ground lines. The 9600 uses TTL for high speed and high fanout capability and is compatible with all members of the Fairchild TTL family

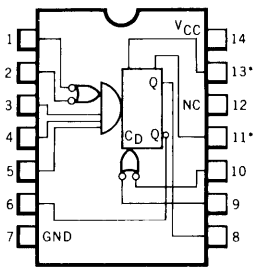
- **74 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **RESETTABLE**
- **TTL INPUT GATING – LEADING OR TRAILING EDGE TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **IMPROVED PULSE WIDTH TEMPERATURE STABILITY**

LOGIC DIAGRAM

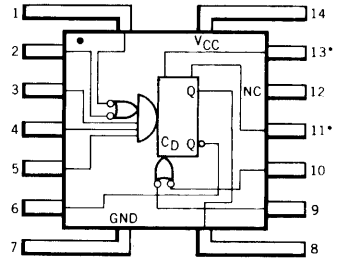


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



*Pins for connecting external timing components.

NC = No Internal Connection

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	-0.5 V to +8.0 V
Input Voltage (dc) (See Note 2)	-0.5 V to +5.5 V
Input Current (See Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output When Output is HIGH	-0.5 V to +V_{CC} value
Current Into Output When Output is LOW	50 mA

NOTES:

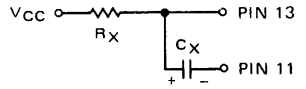
(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.

(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than -0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

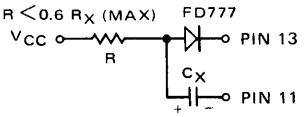
FUNCTIONAL DESCRIPTION – The 9600 monostable multivibrator has five inputs, three active HIGH and two active LOW. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9600 and result in a continuous true output. (See Rule 8.) Retriggering may be inhibited by tying the negation ($\overline{Q}$) output to an active LOW input. The output pulse may be terminated at any time by connecting either or both reset pins to a LOW logic level pin. Active pullups are provided on the outputs for good drive capability into capacitive loads.

OPERATION RULES

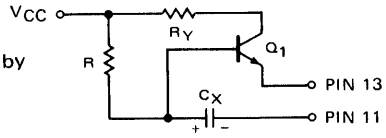
1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the logic diagram. The value of R_X may vary from 5.0 to 50 kΩ for 0 to +75°C operation and from 5.0 to 25 kΩ for -55 to +125°C operation. C_X may vary from 0 to any necessary value available.
2. The following are recommended fixed values of R_X: R_X = 30 kΩ for 0 to +75°C operation, R_X = 10 kΩ for -55 to +125°C operation.
3. The output pulse width (t) is defined as follows:
   $t = 0.32\ R_X C_X\ [1 + \frac{0.7}{R_X}]$ Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF, see Fig. 14.
   The value of C_X may vary from 0 to any value necessary and obtainable. If however, C_X has leakage currents approaching 3 μA or if stray capacitance from either pin 11 or pin 13 to ground exceeds 50 pF, the timing equation may not represent the pulse width obtained.
4. If electrolytic type capacitors are to be used, the following three configurations are recommended.



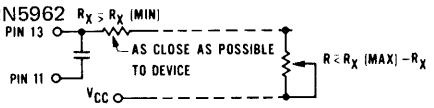
   A. Use with low leakage electrolytic capacitors.
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volts is less than 5 μA over the operational temperature range and Rule 3 above is satisfied.



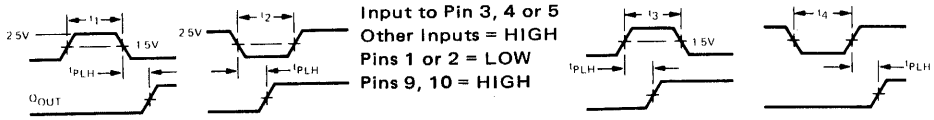
   B. Use with high inverse leakage current electrolytic capacitors.
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.
   $t \approx 0.3\ RC_X$
   The use of this configuration is not recommended with retriggerable operation.



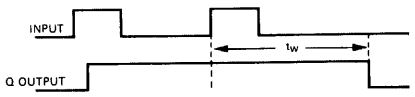
   C. Use to obtain extended pulse widths.
   This configuration obtains extended pulse widths because of the larger timing resistor allowed by Beta multiplication.
   Electrolytics with high inverse leakage currents can be used.
   $R < R_X\ (0.7)\ (h_{FE}Q_1)$ or < 2.5 MΩ, whichever is less
   $R_X(min) < R_Y < R_X(max)$ R_Y of 5 to 10kΩ is recommended.
   Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962
   $t \approx 0.3\ RC_X$
   The use of this configuration is not recommended with retriggerable operation.



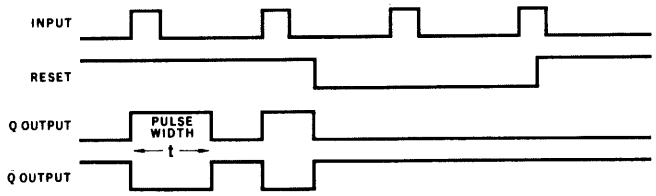
5. This circuit is recommended to obtain variable pulse width by remote trimming.
6. Under any operating condition, C_X and $R_X(min)$ must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
7. Input Trigger Pulse Rules (see Triggering Truth Table, after Fig. 15).
   Input to pin 1 or 2. Pins 2 or 1,3,4,5, 9,10 = HIGH.
   t_1, t_3 = Min. positive input pulse width > 40 ns.
   t_2, t_4 = Min. negative input pulse width > 40 ns.



8. The retrigger pulse width is equal to the pulse width t plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t.
   $t_W = t + t_{PLH} = 0.32\ R_X C_X\ (1 + \frac{0.7}{R_X}) + t_{PLH}$



   NOTE: Retriggering will not occur if the retrigger pulse comes within ≈0.3 C_X ns after the initial trigger pulse (i.e., during the discharge cycle time).
9. Two overriding active LOW resets are provided. A LOW to either or both resets can terminate any timing cycle and/or inhibit any new cycle until both reset inputs are restored to a HIGH. Trigger inputs will not produce spikes in the output when either or both resets are held LOW.



10. Use of a 0.01 to 0.1 μF bypass capacitor located close to the 9600 is recommended.

TABLE I – ELECTRICAL CHARACTERISTICS (T_A = –55°C to 125°C, V_{CC} = 5 V ±10%) (Part No. 9600XM)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS (Note 1)
		–55°C		+25°C			+125°C			
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 9.92 mA (Note 2) V_{CC} = 5.5 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	2.0		1.7			1.5		Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.90		0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		–1.6		–1.1	–1.6		–1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
			–1.24		–0.97	–1.24		–1.24	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current				15	60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current					–25			mA	V_{CC} = 5.5 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}	Quiescent Power Supply Drain		24		19	24		24	mA	V_{CC} = 5.0 V, Gnd Pins 1 & 2
t_{PLH}	Negative Trigger Input to True Output				29	45			ns	V_{CC} = 5.0 V R_X = 5.0 Ω C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				29	40			ns	V_{CC} = 5.0 V R_X = 5.0 Ω C_X = 0, C_L = 15 pF
$t_{(min)}$	Minimum True Output Pulse Width				74	100			ns	V_{CC} = 5.0 V R_X = 5.0 Ω C_X = 0, C_L = 15 pF
	Minimum Complement Output Pulse Width					112			ns	
t	Pulse Width			3.20	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

TABLE II – ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%) (Part No. 9600XC)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS (Note 1)
		0°C		+25°C			75°C			
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 11.3 mA (Note 2) V_{CC} = 5.25 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	1.9		1.8			1.65		Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		–1.6		–1.0	–1.6		–1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
			–1.41			–1.41		–1.41	mA	V_{CC} = 4.75 V, V_{IN} = 0.45 V
I_{IH}	Input HIGH Current				15	60		60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current					–35			mA	V_{CC} = 5.25 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}	Quiescent Power Supply		26		19	26		26	mA	V_{CC} = 5.0 V Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				29	56			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				29	47			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t(min)	Minimum True Output Pulse Width				74	120			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
	Minimum Complement Output Pulse Width					130			ns	
t	Pulse Width			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50		50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)
(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8.
Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.

TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 1
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

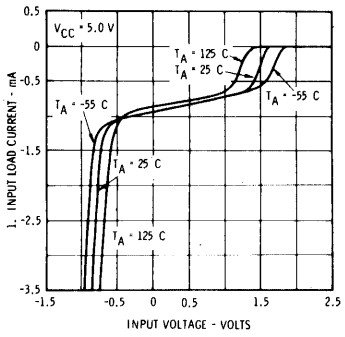


Fig. 2
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

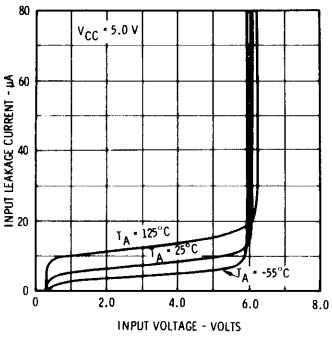


Fig. 3
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

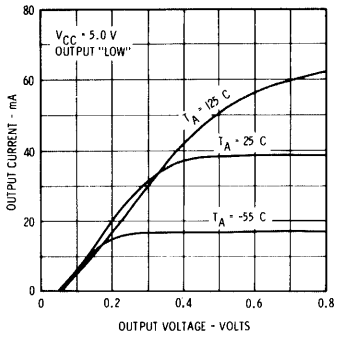


Fig. 4
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

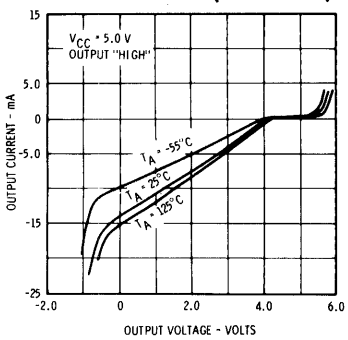


Fig. 5
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)

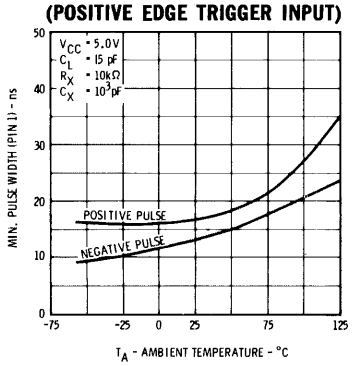


Fig. 6
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)

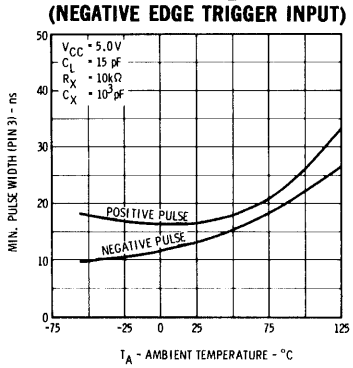


Fig. 7
MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE

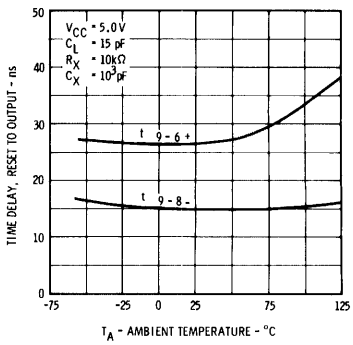


Fig. 8
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

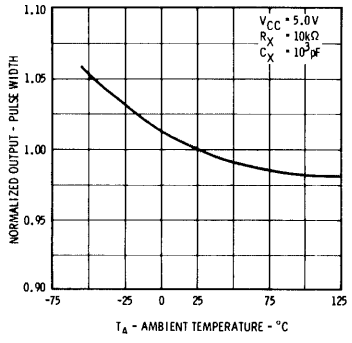


Fig. 9
PULSE WIDTH VERSUS TIMING RESISTOR

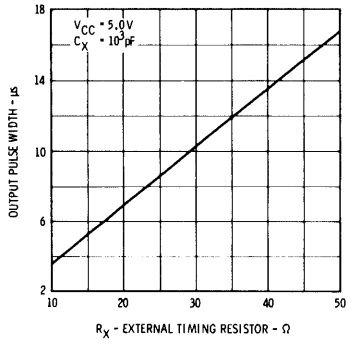


Fig. 10
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

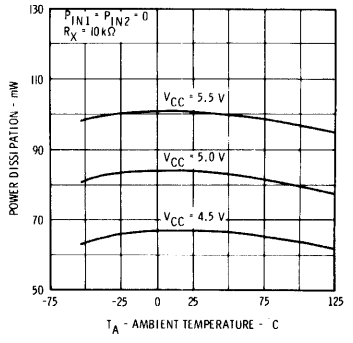


Fig. 11
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

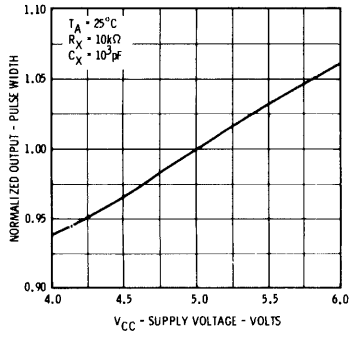


Fig. 12
MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

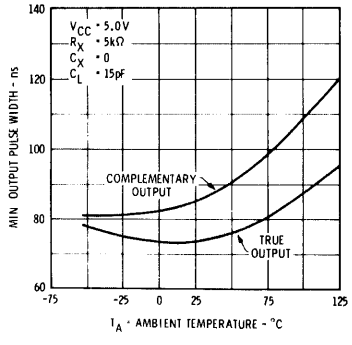
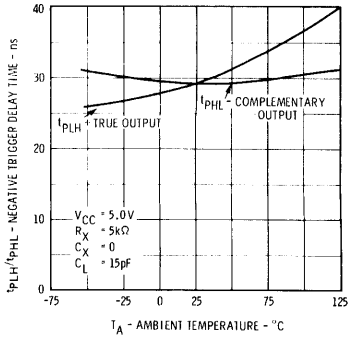


Fig. 13
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

[For $C_X \geq 10^3$ pF, $t = 0.32\ R_X C_X \left(1 + \frac{0.7}{R_X}\right)$]

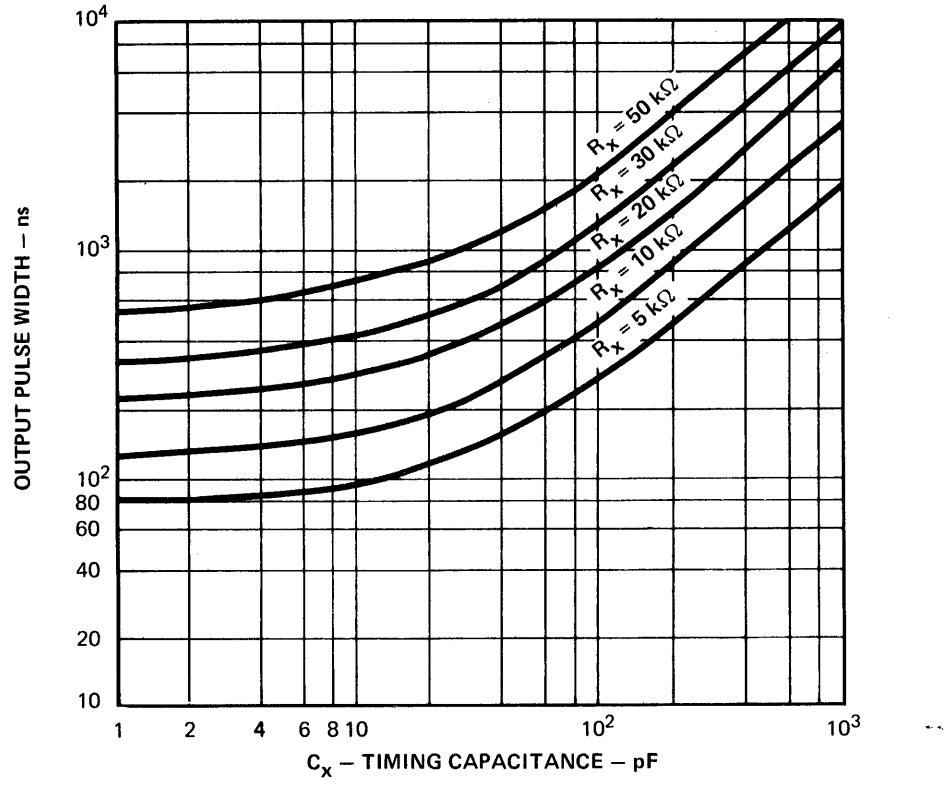
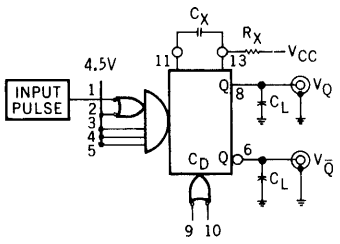
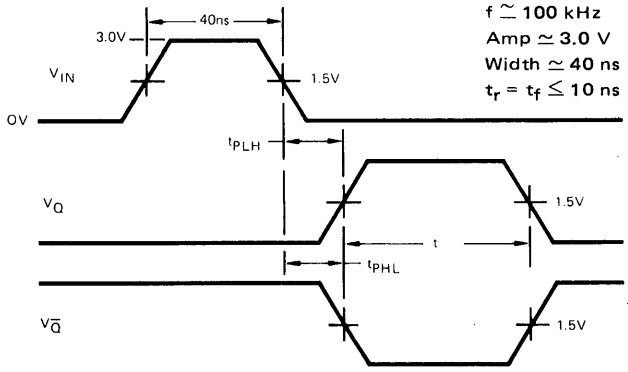


Fig. 14

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS





NOTE: Capacitance includes Jig and Probe

Fig. 15

LOADING RULES

TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
1,2,3,4,5,9,10	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6,8	16 U.L.	8 U.L.

Note: 1 Unit Load (U.L.) = 60 μA HIGH/1.6 mA LOW.

TRIGGERING TRUTH TABLE

(PIN NO'S.) 1	2	3	4	5	9	10	OPERATION
H→L	H	H	H	H	H	H	Trigger
H	H→L	H	H	H	H	H	Trigger
L	X	L→H	H	H	H	H	Trigger
X	L	L→H	H	H	H	H	Trigger
L	X	H	L→H	H	H	H	Trigger
X	L	H	L→H	H	H	H	Trigger
L	X	H	H	L→H	H	H	Trigger
X	L	H	H	L→H	H	H	Trigger
X	X	X	X	X	L	X	Reset
X	X	X	X	X	X	L	Reset

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
H→L = Transition from HIGH to LOW Voltage level
L→H = Transition from LOW to HIGH Voltage level

TTL/MONOSTABLE 9601

RETRIGGERABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 9601 Retriggerable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9601 has excellent immunity to noise on the V_{CC} and ground lines. The 9601 uses TTL for high speed and high fanout capability and is compatible with all members of the Fairchild TTL family.

FEATURES:

- **50 ns TO ∞ OUTPUT PULSE WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **TTL INPUT GATING – LEADING OR TRAILING EDGE TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

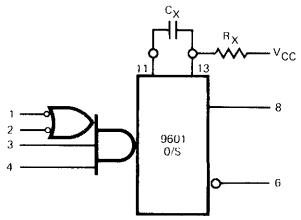
Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	−0.5 V to +8.0 V
Input Voltage (dc) (See Note 2)	−0.5 V to +5.5 V
Input Current (See Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output When Output is HIGH	−0.5 V to +V_{CC} value
Current Into Output When Output is LOW	50 mA

NOTES:

(1) The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.

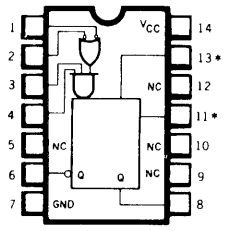
(2) Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than −0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOGIC DIAGRAM

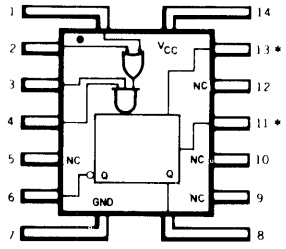


V_{CC} = Pin 14
GND = Pin 7

CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



*Pins for External Timing
NC - No Internal Connection

FUNCTIONAL DESCRIPTION

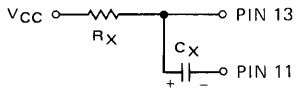
The 9601 monostable multivibrator has four inputs, two active HIGH and two active LOW. This allows a choice of leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9601 and result in a continuous true output. (See Rule 9.) Retriggering may be inhibited by tying the negation (Q) output to an active LOW input. Active pullups are provided on the outputs for good drive capability into capacitive loads.

OPERATION RULES

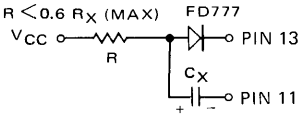
1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 to 50 kΩ for 0 to 75°C operation and from 5.0 to 25 kΩ for −55 to +125°C operation.
3. C_X may vary from 0 to any necessary value available. If however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:

$$t = 0.32\, R_X C_X \left[1 + \frac{0.7}{R_X}\right]$$ Where R_X is in kΩ, C_X is in pF, t is in ns; for $C_X < 10^3$ pF, see Fig. 12.

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:

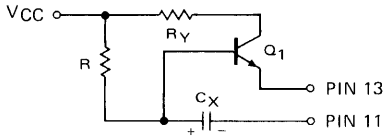


A. For use with low leakage electrolytic capacitors.
The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3 μA, and the inverse capacitor leakage at 1.0 volt is less than 5 μA over the operational temperature range, and Rule 3 above is satisfied.



B. Use with high inverse leakage current electrolytic capacitors.
The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor.

$$t \approx 0.3\, RC_X$$



C. Use to obtain extended pulse widths:
This configuration obtains extended pulse widths, because of the larger timing resistor allowed by Beta multiplication. Electrolytics with high (>5 μA) inverse leakage currents can be used.

$R < R_X\,(0.7)\,(h_{FE}\,Q_1)$ or < 2.5 MΩ whichever is lesser

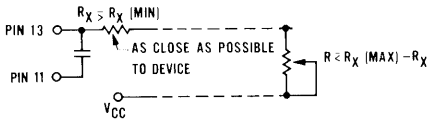
R_X (min) $< R_Y < R_X$ (max) ($5 \leqslant R_Y \leqslant 10$ kΩ is recommended)

Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$t \approx 0.3\, RC_X$

Configuration B and C are not recommended with retriggerable operation.

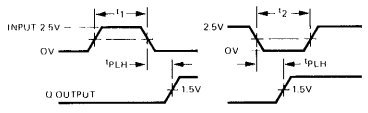
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



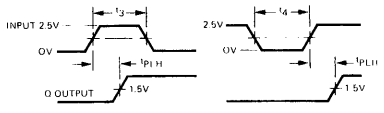
7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.

8. Input Trigger Pulse Rules. (See Triggering Truth Table on page 5.)

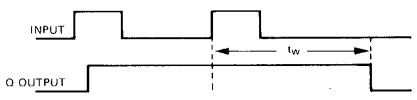
Input to Pin 1 (2)
Pins 2, (1), 3 & 4 = HIGH
t_1, t_4 = Setup time > 40 ns
t_2, t_3 = Release time > 40 ns



Input to Pin 3 (4)
Pin 4 (3) = HIGH
Pins 1 or 2 = LOW



9. The retrigger pulse width is calculated as shown below:



$$t_W = t + t_{PLH} = 0.32\, R_X C_X \left(1 + \frac{0.7}{R_X}\right) + t_{PLH}$$

The retrigger pulse width is equal to the pulse width t plus a delay time. For pulse widths greater than 500 ns, t_W can be approximated as t.

NOTE: Retriggering will not occur if the retrigger pulse comes within ≈ 0.3 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle time.)

10. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located close to the 9601 is recommended.

TABLE I – ELECTRICAL CHARACTERISTICS (T_A = –55°C to 125°C, V_{CC} = 5 V ±10%) (Part No. 9601XM)*

SYMBOL	PARAMETER	LIMITS						UNITS	CONDITIONS (Note 1)
		–55°C		+25°C			+125°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4	Volts	V_{CC} = 4.5 V, I_{OH} = –0.72 mA (Note 2)
V_{OL}	Output LOW Voltage		0.4		0.2	0.4	0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 10 mA (Note 2)
V_{IH}	Input HIGH Voltage (Note 3)	2.0		1.7			1.5	Volts	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage (Note 3)		0.85			0.90	0.85	Volts	Guaranteed Input LOW Threshold
I_{IL}	Input LOW Current		–1.6		–1.1	–1.6	–1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current				15	60	60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current			–10		–40		mA	V_{CC} = 5.0 V, V_{OUT} = 0 V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25	25	mA	V_{CC} = 5.5 V, Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				25	40		ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				25	40		ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t (min)	Minimum True Output Pulse Width				45	65		ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t	Pulse Width			3.08	3.42	3.76		μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50	50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0 25	kΩ	

TABLE II – ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%) (Part No. 9601XC)*

SYMBOL	PARAMETER	LIMITS						UNITS	CONDITIONS (Note 1)
		0°C		+25°C			+75°C		
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN. MAX.		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.4		2.4	Volts	V_{CC} = 4.75 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.45		0.2	0.45	0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 12.8 mA (Note 2)
V_{IH}	Input HIGH Voltage (Note 3)	1.9		1.8			1.6	Volts	Guaranteed Input HIGH Threshold
V_{IL}	Input LOW Voltage (Note 3)		.85			0.85	0.85	Volts	Guaranteed Input LOW Threshold
I_{IL}	Input LOW Current		–1.6		–1.0	–1.6	–1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
I_{IH}	Input HIGH Current				15	60	60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current			–10		–40		mA	V_{CC} = 5.0 V, V_{OUT} = 0V (Note 2)
I_{PD}	Quiescent Power Supply Drain		25			25	25	mA	V_{CC} = 5.25 V, Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				25	40		ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				25	40		ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t (min)	Minimum True Output Pulse Width				45	65		ns	V_{CC} = 5.0 V, R_X = 5.0 kΩ, C_X = 0, C_L = 15 pF
t	Pulse Width			3.08	3.42	3.76		μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pin 13)		50			50	50	pF	Pin 13 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0 50	kΩ	

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
(1) Unless otherwise noted, 10 kΩ resistor placed between Pin 13 and V_{CC}, for all tests. (R_X)
(2) Ground Pin 11 for V_{OL} Pin 6 or V_{OH} Pin 8 or I_{SC} Pin 8. Open Pin 11 for V_{OL} Pin 8 or V_{OH} Pin 6 or I_{SC} Pin 6.
(3) Pulse Test to determine V_{IH} and V_{IL} (Min PW 40 ns).

TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 1
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

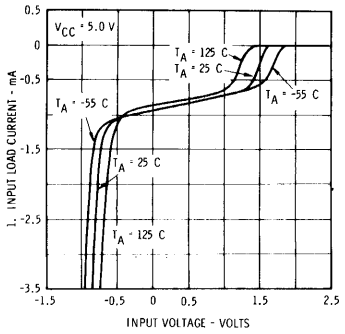


Fig. 2
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

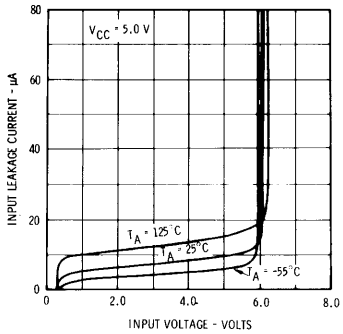


Fig. 3
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

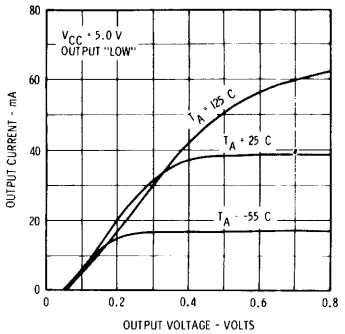


Fig. 4
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

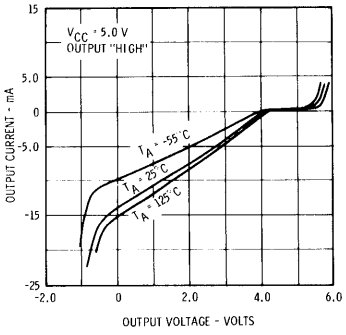


Fig. 5
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

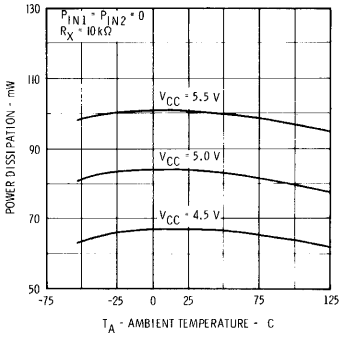


Fig. 6
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE

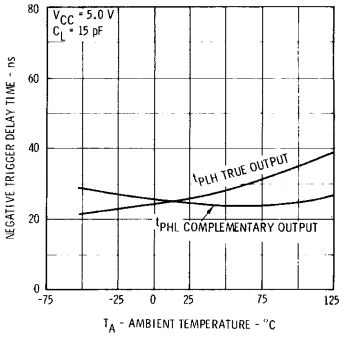


Fig. 7
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

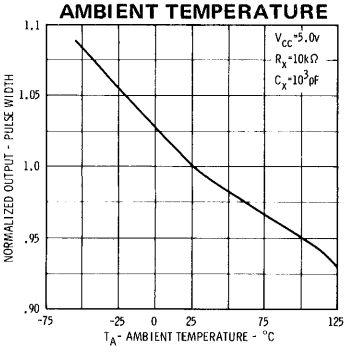


Fig. 8
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

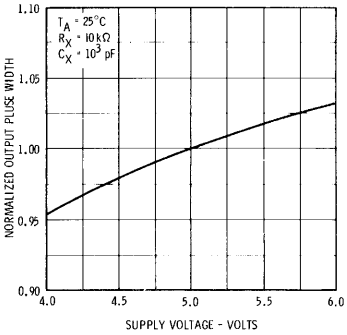


Fig. 9
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE

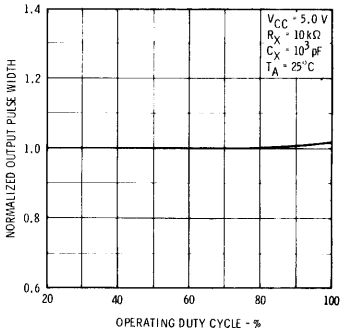


Fig. 10
PULSE WIDTH VERSUS TIMING RESISTANCE

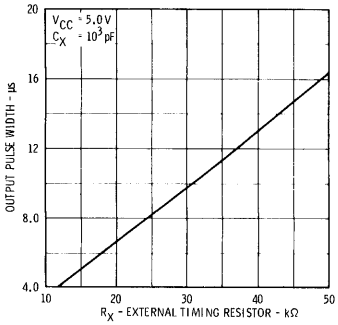
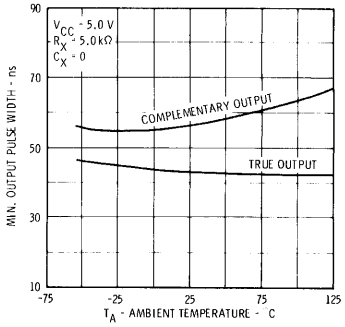


Fig. 11
OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

$$\left[\text{For } C_X \geq 10^3 \text{ pF, } t = 0.32\ R_X C_X \left(1 + \frac{0.7}{R_X}\right)\right]$$

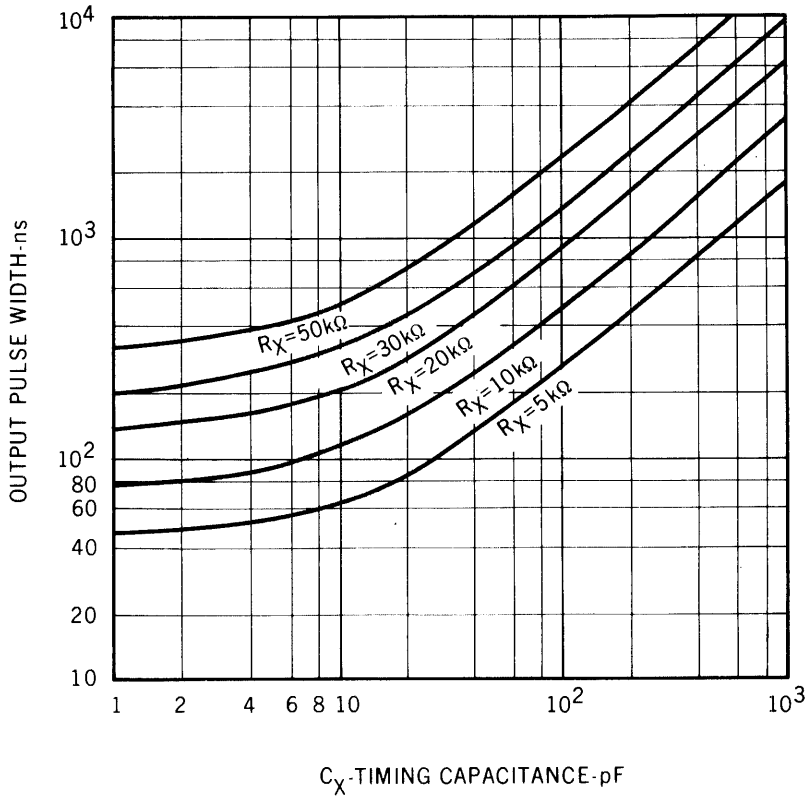
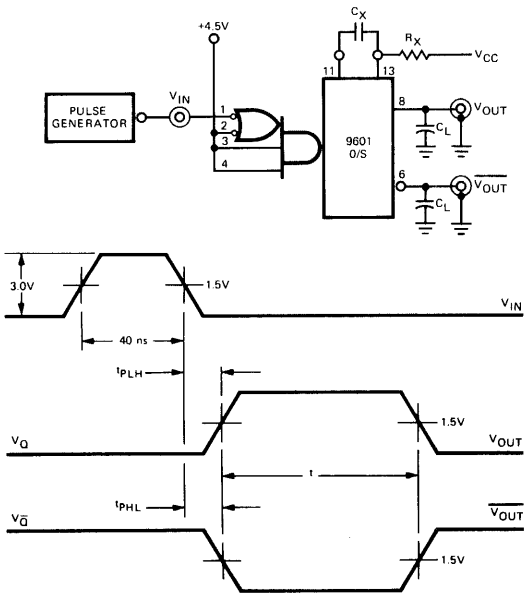


Fig. 12

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Capacitance includes Jig and Probe

LOADING RULES
TTL INPUT LOAD AND DRIVE FACTORS

-55°C to +125°C

INPUT LEVEL	LOAD FACTOR
HIGH	1
LOW	1
OUTPUT STATE	**DRIVE FACTOR**
HIGH	12
LOW	6

0°C to 75°C

INPUT LEVEL	LOAD FACTOR
HIGH	1
LOW	1
OUTPUT STATE	**DRIVE FACTOR**
HIGH	16
LOW	8

TRIGGERING TRUTH TABLE

Pin Number				
1	2	3	4	Operation
H→L	H	H	H	Trigger
H	H→L	H	H	Trigger
L	X	L→H	H	Trigger
X	L	L→H	H	Trigger
L	X	H	L→H	Trigger
X	L	H	L→H	Trigger

T (trigger) = $(\overline{1} + \overline{2}) \cdot 3 \cdot 4$

Change of T from FALSE to TRUE causes trigger.

H = HIGH voltage level ≥ V_{IH}
L = LOW voltage ≤ V_{IL}
L→H = transition from LOW to HIGH voltage level
H→L = transition from HIGH to LOW voltage level
X = Don't care (either HIGH or LOW voltage level)

TTL/MONOSTABLE 9602

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 9602 Dual Retriggerable, Resettable Monostable Multivibrator provides an output pulse whose duration and accuracy is a function of external timing components. The 9602 has excellent immunity to noise on the V_{CC} and ground lines. The 9602 uses TTL inputs and outputs for high speed and high fanout capability and is compatible with all members of the Fairchild TTL family.

- **72 ns TO ∞ OUTPUT WIDTH RANGE**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **TTL INPUT GATING –LEADING OR TRAILING EDGE TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

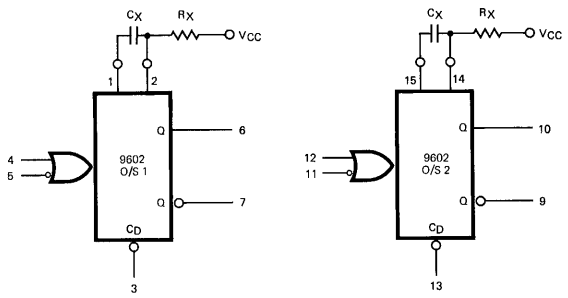
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{CC} Pin Potential to Ground (See Note 1)	–0.5 V to +8.0 V
Input Voltage (dc) (See Note 2)	–0.5 V to +5.5 V
Input Current (See Note 2)	–30 mA to +5.0 mA
Voltage Applied to Output When Output is HIGH	–0.5 V to +V_{CC} value
Current Into Output When Output is LOW	50 mA

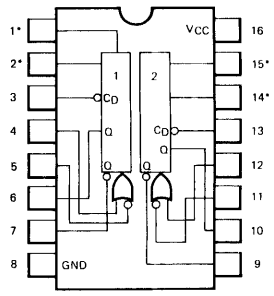
NOTES:

1. The maximum V_{CC} value of 8.0 volts is not the primary factor in determining the maximum V_{CC} which may be applied to a number of interconnected devices. The voltage at a HIGH output is approximately 1 V_{BE} below the V_{CC} voltage, so the primary limit on the V_{CC} is that the voltage at any input may not go above 5.5 V unless the current is limited. This effectively limits the system V_{CC} to approximately 7.0 volts.
2. Because of the input clamp diodes, excess current can be drawn out of the inputs if the dc input voltage is more negative than –0.5 V. The diode is designed to clamp off large negative ac swings associated with fast fall times and long lines. This maximum rating is intended only to limit the steady state input voltage and current.

LOGIC DIAGRAM

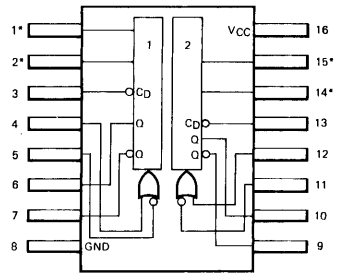


CONNECTION DIAGRAMS
DIP (TOP VIEW)



*Pins for external timing.

FLATPAK (TOP VIEW)



*Pins for external timing.

7

FUNCTIONAL DESCRIPTION — The 9602 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge or trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 9602 and result in a continuous true output. (See Rule 9) The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying $\overline{Q}$ output to an active level LOW input or the Q output to the active level HIGH input.

OPERATION RULES

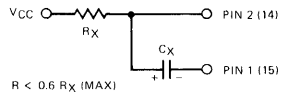
1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 5.0 kΩ to 50 kΩ for 0 to 75°C operation. The value of R_X may vary from 5.0 kΩ to 25 kΩ for −55 to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 3.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:

$$t = 0.31\ R_X C_X \left[1 + \frac{1}{R_X}\right]$$ Where

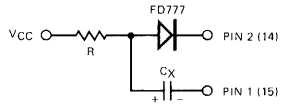
R_X is in kΩ, C_X is in pF
t is in ns
for $C_X < 10^3$ pF, see Fig. 14

5. If electrolytic type capacitors are to be used, the following three configurations are recommended:

   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 volts is less than 3μA, and the inverse capacitor leakage at 1.0 volt is less than 5μA over the operational temperature range and Rule 3 above is satisfied.

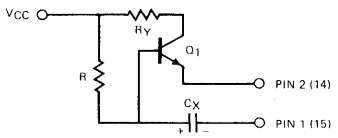


   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.



$$t \approx 0.3\ RC_X$$

   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.



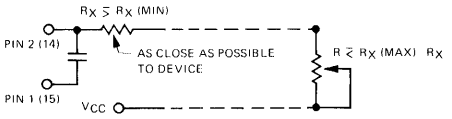
$R < R_X\ (0.7)\ (h_{FE}\ Q_1)$ or < 2.5 MΩ whichever is the lesser
$R_X\ (\text{min}) < R_Y < R_X\ (\text{max})$ $(5 \leq R_Y \leq 10$ kΩ is recommended)

Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$$t \approx 0.3\ RC_X$$

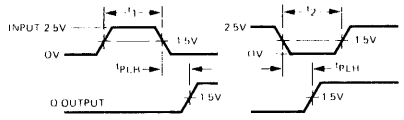
This configuration is not recommended with retriggerable operation.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

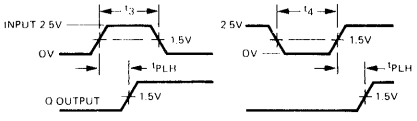


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Table, following pages.

   Input to Pin 5 (11)
   Pin 4 (12) = LOW
   Pin 3 (13) = HIGH
   t_1, t_3 = Min. Positive Input Pulse Width > 40 ns
   t_2, t_4 = Min. Negative Input Pulse Width > 40 ns

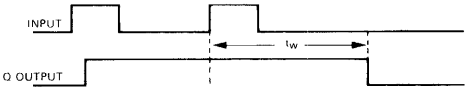


   Input to Pin 4 (12)
   Pin 5 (11) = HIGH
   Pin 3 (13) = HIGH

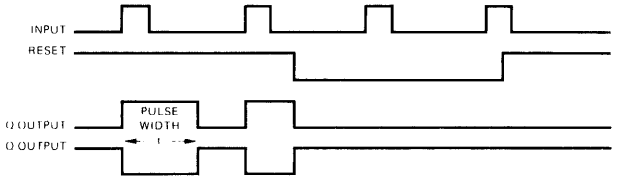


9. The retriggerable pulse width is calculated as shown below:

$$t_W = t + t_{PLH} = 0.31\ R_X C_X \left(1 + \frac{1}{R_X}\right) + t_{PLH}$$



   The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as t.
   Retriggering will not occur if the retrigger pulse comes within $\approx 0.3\ C_X$ ns after the initial trigger pulse. (i.e., during the discharge cycle)
10. Reset Operation — An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the 9602 is recommended.

TABLE I – ELECTRICAL CHARACTERISTICS (T_A = –55°C to 125°C, V_{CC} = 5 V ±10%) (Part No. 9602XM)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS (Note 1)
		–55°C		+25°C			+125°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.3		2.4		Volts	V_{CC} = 4.5 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.4		0.2	0.4		0.4	Volts	V_{CC} = 4.5 V, I_{OL} = 9.92 mA (Note 2) V_{CC} = 5.5 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	2.0		1.7			1.5		Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.90		0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		–1.6		–1.1	–1.6		–1.6	mA	V_{CC} = 5.5 V, V_{IN} = 0.4 V
			–1.24		–0.97	–1.24		–1.24	mA	V_{CC} = 4.5 V, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current				10	60		60	μA	V_{CC} = 5.5 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current					–25			mA	V_{CC} = 5.5 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}	Quiescent Power Supply Drain		45		39	45		45	mA	V_{CC} = 5.0 V
t_{PLH}	Negative Trigger Input to True Output				25	35			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				29	43			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{(min)}$	Minimum True Output Pulse Width				72	90			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
	Minimum Complement Output Pulse Width				78	100			ns	C_X = 0, C_L = 15 pF
t	Pulse Width			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pins 2 and 14)		50			50		50	pF	Pins 2 and 14 to Ground
R_X	Timing Resistor	5.0	25	5.0		25	5.0	25	kΩ	

TABLE II – ELECTRICAL CHARACTERISTICS (T_A = 0°C to 75°C, V_{CC} = 5 V ±5%) (Part No. 9602XC)*

SYMBOL	PARAMETER	LIMITS							UNITS	CONDITIONS (Note 1)
		0°C		+25°C			+75°C			
		MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.		
V_{OH}	Output HIGH Voltage	2.4		2.4	3.4		2.4		Volts	V_{CC} = 4.75 V, I_{OH} = –0.96 mA (Note 2)
V_{OL}	Output LOW Voltage		0.45		0.2	0.45		0.45	Volts	V_{CC} = 4.75 V, I_{OL} = 11.3 mA (Note 2) V_{CC} = 5.25 V, I_{OL} = 12.8 mA
V_{IH}	Input HIGH Voltage	1.9		1.8			1.65		Volts	Guaranteed Input HIGH Threshold Voltage
V_{IL}	Input LOW Voltage		0.85			0.85		0.85	Volts	Guaranteed Input LOW Threshold Voltage
I_{IL}	Input LOW Current		–1.6		–1.0	–1.6		–1.6	mA	V_{CC} = 5.25 V, V_{IN} = 0.45 V
			–1.41			–1.41		–1.41	mA	V_{CC} = 4.75 V, V_{IN} = 0.45 V
I_{IH}	Input HIGH Current				10	60		60	μA	V_{CC} = 5.25 V, V_{IN} = 4.5 V
I_{SC}	Short Circuit Current					–35			mA	V_{CC} = 5.25 V, V_{OUT} = 1.0 V (Note 2)
I_{PD}	Quiescent Power Supply Drain		52		39	50		52	mA	V_{CC} = 5.0 V, Ground Pins 1 and 2
t_{PLH}	Negative Trigger Input to True Output				25	40			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output				29	48			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ C_X = 0, C_L = 15 pF
$t_{(min)}$	Minimum True Output Pulse Width				72	100			ns	V_{CC} = 5.0 V R_X = 5.0 kΩ
	Minimum Complement Output Pulse Width				78	110			ns	C_X = 0, C_L = 15 pF
t	Pulse Width			3.08	3.42	3.76			μs	V_{CC} = 5.0 V, R_X = 10 kΩ, C_X = 1000 pF
C_{STRAY}	Maximum Allowable Wiring Cap. (Pins 2 and 14)		50			50		50	pF	Pins 2 and 14 to Ground
R_X	Timing Resistor	5.0	50	5.0		50	5.0	50	kΩ	

*X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

NOTES:
1. Unless otherwise noted, 10 kΩ resistor placed between Pin 2 (14) and V_{CC}, for all tests. (R_X)
2. Ground Pin 1 (15) for V_{OL} on Pin 7 (9), or for V_{OH} on Pin 6 (10), or for I_{SC} on Pin 6 (10); also, apply momentary ground to Pin 4 (12). Open Pin 1 (15) for V_{OL} on Pin 6 (10), or for V_{OH} on Pin 7 (9), or for I_{SC} on Pin 7 (9).

TYPICAL ELECTRICAL CHARACTERISTICS

Fig. 1
INPUT LOAD CURRENT VERSUS INPUT VOLTAGE

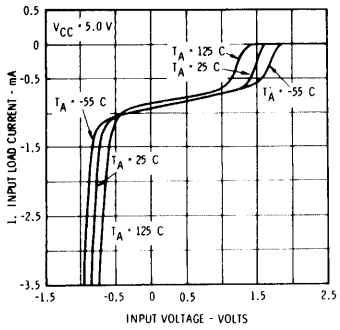


Fig. 2
INPUT LEAKAGE CURRENT VERSUS INPUT VOLTAGE

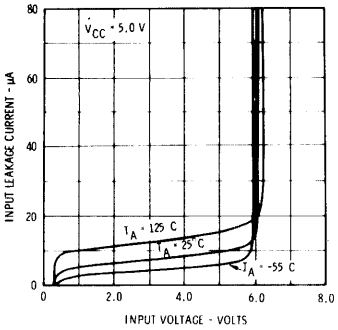


Fig. 3
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)

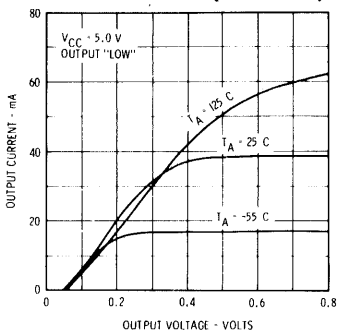


Fig. 4
OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (HIGH STATE)

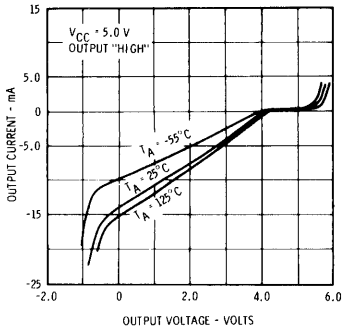


Fig. 5
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (POSITIVE EDGE TRIGGER INPUT)

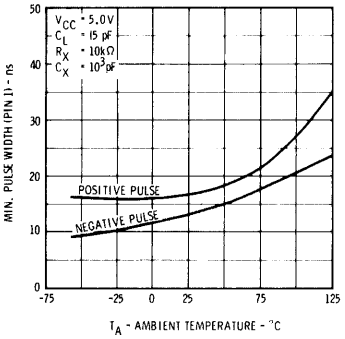


Fig. 6
MINIMUM PULSE WIDTH TO TRIGGER VERSUS AMBIENT TEMPERATURE (NEGATIVE EDGE TRIGGER INPUT)

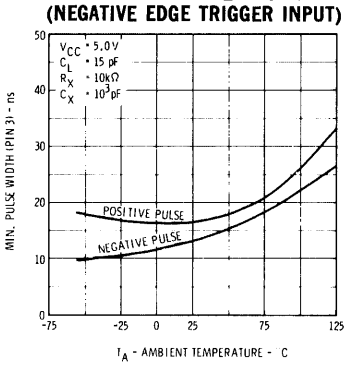


Fig. 7
MINIMUM TIME DELAY, RESET TO OUTPUT VERSUS AMBIENT TEMPERATURE

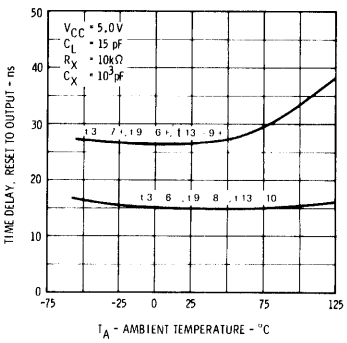


Fig. 8
NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

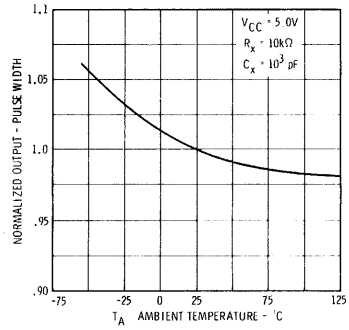


Fig. 9
PULSE WIDTH VERSUS TIMING RESISTOR

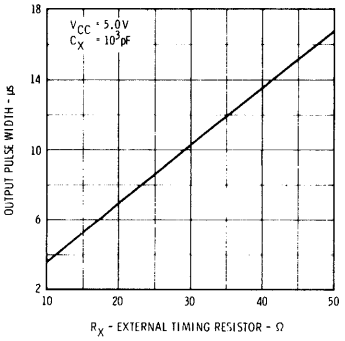


Fig. 10
POWER DISSIPATION VERSUS AMBIENT TEMPERATURE

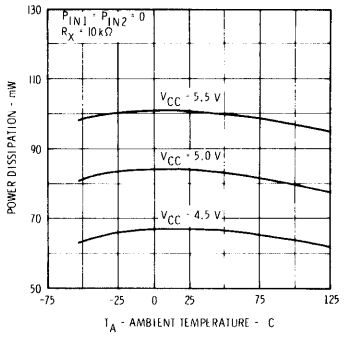


Fig. 11
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

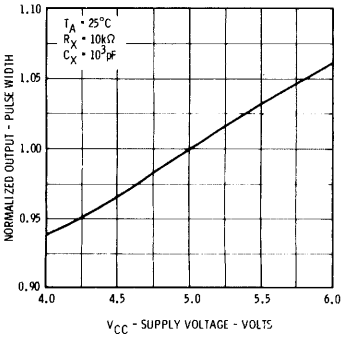


Fig. 12
MINIMUM OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

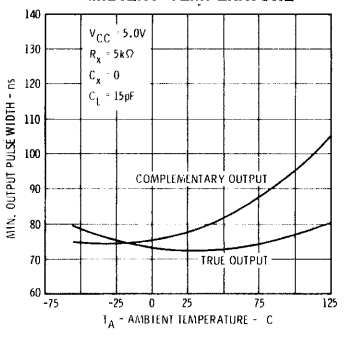
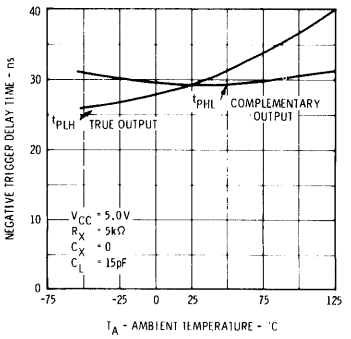


Fig. 13
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



OUTPUT PULSE WIDTH VERSUS TIMING RESISTANCE AND CAPACITANCE FOR $C_X < 10^3$ pF

For $C_X \geq 10^3$ pF, $t = 0.31\ R_X C_X \left(1 + \frac{1}{R_X}\right)$

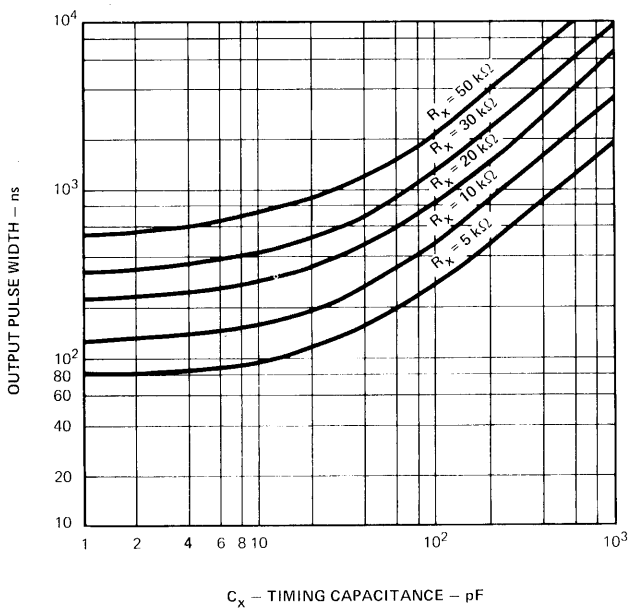


Fig. 14

LOADING RULES

TTL INPUT LOAD AND DRIVE FACTORS

INPUTS	LOAD	
	HIGH	LOW
3, 4, 5, 11, 12, 13	1 U.L.	1 U.L.

OUTPUTS	DRIVE FACTOR	
	HIGH	LOW
6, 7, 9, 10	16 U.L.	8 U.L.

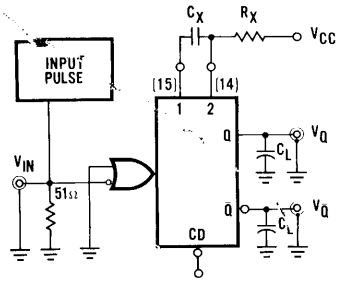
1 Unit Load (U.L.) = 60μA HIGH/1.6mA LOW

TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Don't Care
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

SWITCHING CIRCUITS AND WAVEFORMS



V_{CC} = Pin 16
GND = Pin 8

INPUT PULSE
f ≃ 100 kHz
Amp ≃ 3.0 V
Width ≃ 40 ns
$t_r = t_f \leq 10$ ns

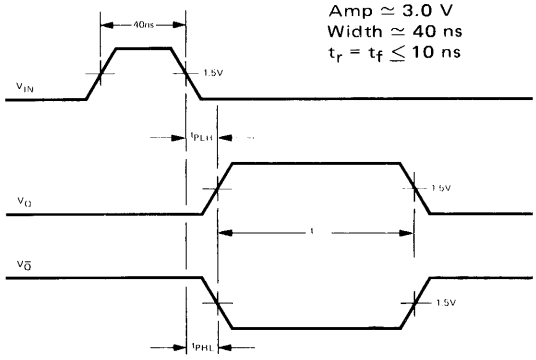


Fig. 18

LPTTL/MONOSTABLE 96L02
LOW POWER DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The TTL/Monostable 96L02 is a low power Dual Retriggerable, Resettable Monostable Multivibrator which provides an output pulse whose duration and accuracy is a function of external timing components. The 96L02 has excellent immunity to noise on the V_{CC} and ground lines. The 96L02 uses TTL inputs and outputs for high speed and high fan out capability and is compatible with all members of the Fairchild TTL family.

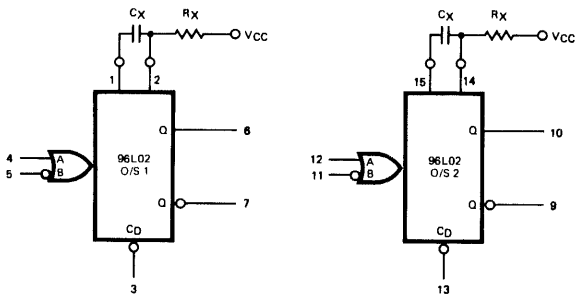
- **TYPICAL POWER DISSIPATION OF 25 mW/ONE SHOT**
- **50 ns TYPICAL PROPAGATION DELAY**
- **RETRIGGERABLE 0 TO 100% DUTY CYCLE**
- **TTL INPUT GATING – LEADING OR TRAILING EDGE TRIGGERING**
- **COMPLEMENTARY TTL OUTPUTS**
- **OPTIONAL RETRIGGER LOCK-OUT CAPABILITY**
- **PULSE WIDTH COMPENSATED FOR V_{CC} AND TEMPERATURE VARIATIONS**
- **RESETTABLE**

PIN NAMES

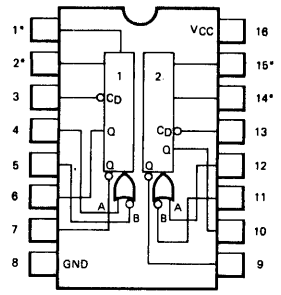
		LOADING HIGH	LOADING LOW
$\overline{B}$	Trigger (Active LOW) Input	0.5	0.25
A	Trigger (Active HIGH) Input	0.5	0.25
$\overline{C}_D$	Clear (Active LOW) Input	0.5	0.25
Q	Output (Active HIGH)	9.0	3.0
$\overline{Q}$	Output (Active LOW)	9.0	3.0

1 Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW

LOGIC DIAGRAM

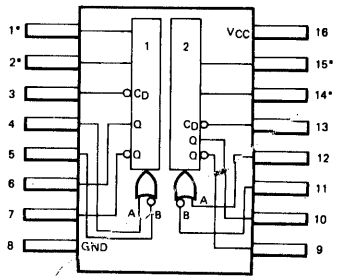


CONNECTION DIAGRAMS
DIP (TOP VIEW)



*Pins for external timing.

FLATPAK (TOP VIEW)

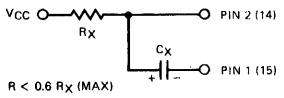


*Pins for external timing.

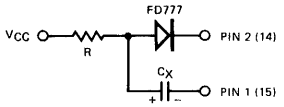
FUNCTIONAL DESCRIPTION – The 96L02 dual resettable, retriggerable monostable multivibrator has two inputs per function, one active LOW and one active HIGH. This allows leading edge of trailing edge triggering. The TTL inputs make triggering independent of input transition times. When input conditions for triggering are met, a new cycle starts and the external capacitor is rapidly discharged and then allowed to charge. An input cycle time shorter than the output cycle time will retrigger the 96L02 and result in a continuous true output. (See Rule 9) The output pulse may be terminated at any time by connecting the reset pin to a logic level LOW. Active pullups are provided on the outputs for good drive capability into capacitive loads. Retriggering may be inhibited by tying the $\overline{Q}$ output to the active level LOW input or the Q output to the active level HIGH input.

OPERATION RULES

1. An external resistor (R_X) and external capacitor (C_X) are required as shown in the Logic Diagram.
2. The value of R_X may vary from 16 kΩ to 220 kΩ for 0 to 75°C operation. The value of R_X may vary from 20 kΩ to 100 kΩ for –55 to +125°C operation.
3. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has leakages approaching 1.0 μA or if stray capacitance from either terminal to ground is more than 50 pF, the timing equations may not represent the pulse width obtained.
4. The output pulse with (t) is defined as follows:
$$t = 0.33\, R_X C_X \left[1 + \frac{3.0}{R_X}\right] \quad (\text{for } C_X > 10^3 \text{ pF})$$
Where R_X is in kΩ, C_X is in pF, t is in ns. For $C_X < 10^3$ pF, see Fig. 1
5. If electrolytic type capacitors are to be used, the following three configurations are recommended:
   A. Use with low leakage capacitors:
   The normal RC configuration can be used predictably only if the forward capacitor leakage at 5.0 V is less than 1.0 μA, and the inverse capacitor leakage at 1.0 V is less than 1.6 μA over the operational temperature range and Rule 3 above is satisfied.

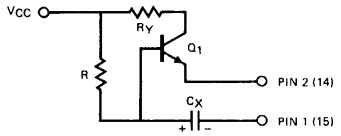


   B. Use with high inverse leakage current electrolytic capacitors:
   The diode in this configuration prevents high inverse leakage currents through the capacitor by preventing an inverse voltage across the capacitor. The use of this configuration is not recommended with retriggerable operation.



$$t \approx 0.3\, RC_X$$

   C. Use to obtain extended pulse widths:
   This configuration can be used to obtain extended pulse widths, because of the larger timing resistor allowed by beta multiplication. Electrolytics with high inverse leakage currents can be used.



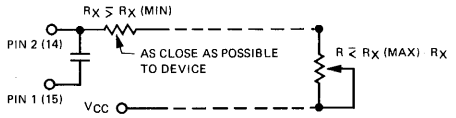
$R < R_X\,(0.7)\,(h_{FE}\,Q_1)$ or <2.5 MΩ whichever is the lesser
R_X (min) $< R_Y < R_X$ (max)

Q_1: NPN silicon transistor with h_{FE} requirements of above equations, such as 2N5961 or 2N5962

$$t \approx 0.3\, RC_X$$

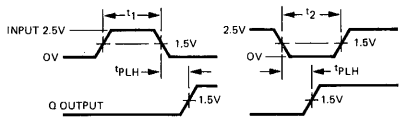
This configuration is not recommended with retriggerable operation.

6. To obtain variable pulse width by remote trimming, the following circuit is recommended:

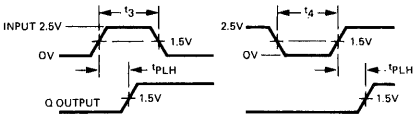


7. Under any operating condition, C_X and R_X (min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. Input Trigger Pulse Rules. See Triggering Truth Table, following pages.

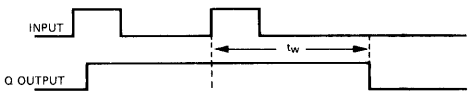
Input to Pin 5 (11)
Pin 4 (12) = LOW
Pin 3 (13) = HIGH
t_1, t_3 = Min. Positive Input Pulse Width > 60 ns
t_2, t_4 = Min. Negative Input Pulse Width > 60 ns



Input to Pin 4 (12)
Pin 5 (11) = HIGH
Pin 3 (13) = HIGH

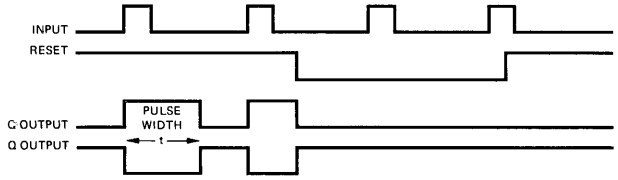


9. The retriggerable pulse width is calculated as shown below:
$$tw = t + t_{PLH} = 0.33\, R_X C_X \left(1 + \frac{3.0}{R_X}\right) + t_{PLH}$$



The retrigger pulse width is equal to the pulse width (t) plus a delay time. For pulse widths greater than 500 ns, tw can be approximated as t. Retriggering will not occur if the retrigger pulse comes within ≈ 0.9 C_X ns after the initial trigger pulse. (i.e., during the discharge cycle)

10. Reset Operation – An overriding active LOW level is provided on each oneshot. By applying a LOW to the reset, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW.



11. V_{CC} and Ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and Ground leads do not cause interaction between one-shots. Use of a 0.01 to 0.1 μF bypass capacitor between V_{CC} and Ground located near the 96L02 is recommended.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage Limit or Input Current is sufficient to protect the inputs.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN.	TYP.	MAX.	
96L02XM	4.5 V	5.0 V	5.5 V	−55°C to 125°C
96L02XC	4.75 V	5.0 V	5.25 V	0°C to 75°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise noted)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		MIN.	TYP. (Note 4)	MAX.		
V_{IH}	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Threshold Voltage For all Inputs
V_{IL}	Input LOW Voltage			0.7	Volts	Guaranteed Input LOW Threshold Voltage For all Inputs
V_{OH}	Output HIGH Voltage	2.4	3.4		Volts	V_{CC} = MIN., I_{OH} = −0.36 mA
V_{OL}	Output LOW Voltage		0.14	0.3	Volts	V_{CC} = MIN., I_{OL} = 4.80 mA
I_{IH}	Input HIGH Current			20	μA	V_{CC} = MAX., V_{IN} = 2.4 V
				1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V
I_{IL}	Input LOW Current		−0.25	−0.4	mA	V_{CC} = MAX., V_{IN} = 0.3 V
I_{SC} (I_{OS})	Output Short Circuit Current (Note 5)	−2.0		−13	mA	V_{CC} = MAX., V_{OUT} = 1.0 V
I_{CC}	Power Supply Current		10	16	mA	V_{CC} = MAX.

NOTES:
1. The actual testing procedures used to guarantee the Electrical Characteristics are contained in a detailed Customer Sample Specification. A copy of this specification can be obtained from Fairchild Digital Product Marketing, Mountain View, California.
2. Conditions for testing, not shown in the table, are chosen to guarantee operation under "worst case" conditions.
3. The specified LIMITS represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature and supply voltages extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
4. Typical limits are at V_{CC} = 5.0 V, 25°C, and maximum loading.
5. Not more than one output should be shorted at a time.

SWITCHING CHARACTERISTICS ($T_A = 25°C$)

SYMBOL	PARAMETER	LIMITS			UNITS	CONDITIONS
		MIN.	TYP.	MAX.		
96L02XM						
t_{PLH}	Negative Trigger Input to True Output		55	75	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output		45	62	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t(min)	Minimum True Output Pulse Width		110		ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t	Pulse Width	12.4	13.8	15.2	μs	V_{CC} = 5.0 V, R_X = 39 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range	20		100	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		1.3		%	R_X = 39 kΩ, C_X = 1000 pF
96L02XC						
t_{PLH}	Negative Trigger Input to True Output		55	80	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t_{PHL}	Negative Trigger Input to Complement Output		45	65	ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t(min)	Minimum True Output Pulse Width		110		ns	V_{CC} = 5.0 V, R_X = 20 kΩ C_X = 0, C_L = 15 pF
t	Pulse Width	12.4	13.8	15.2	μs	V_{CC} = 5.0 V, R_X = 39 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range	16		220	kΩ	
Δt	Maximum Change in True Output Pulse Width over Temperature Range		0.3	1.6	%	R_X = 39 kΩ, C_X = 1000 pF

7

OUTPUT PULSE WIDTH (t) USING LOW VALUES OF C_X ($C_X \leq$ 1000 pF)
(FOR C_X > 1000 pF SEE OPERATION RULES 4 AND 5.)

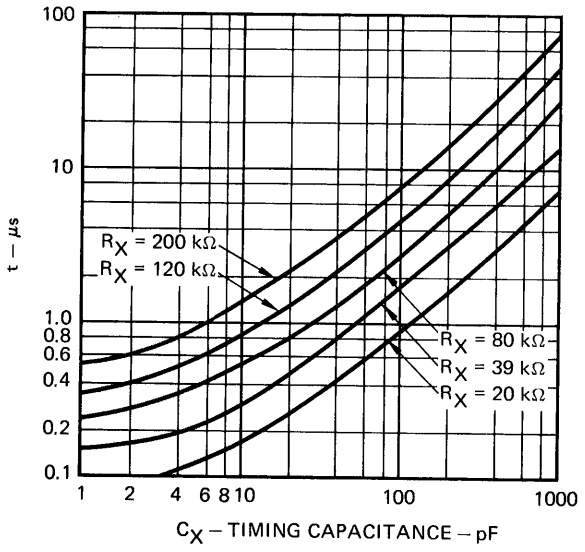
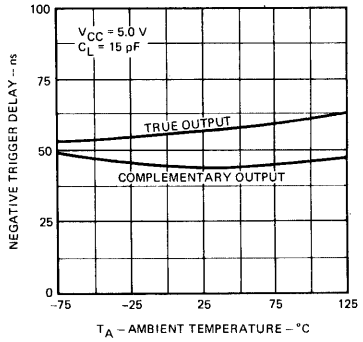


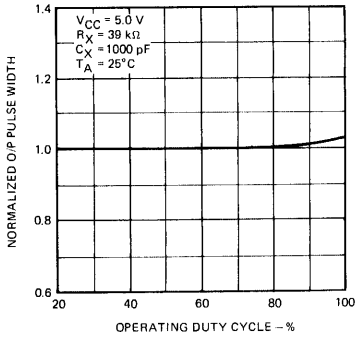
Fig. 1

TYPICAL PULSE CHARACTERISTICS

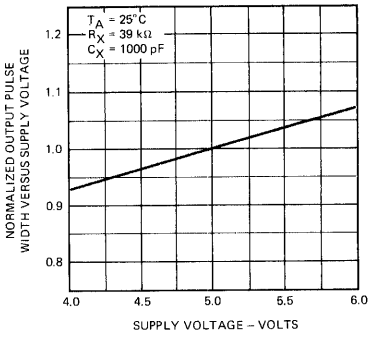
NEGATIVE TRIGGER DELAY TIME VERSUS AMBIENT TEMPERATURE



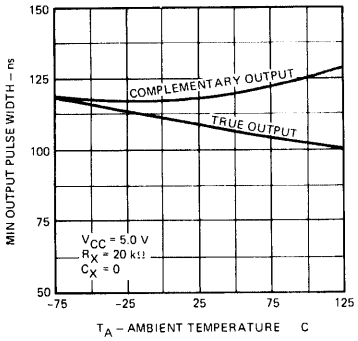
NORMALIZED OUTPUT PULSE WIDTH VERSUS OPERATING DUTY CYCLE



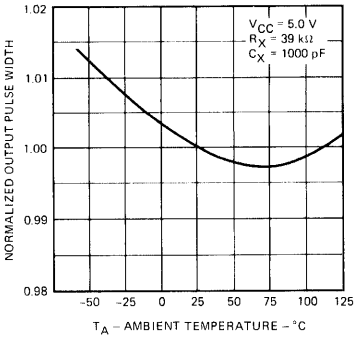
NORMALIZED OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE



MIN. OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE



NORMALIZED OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

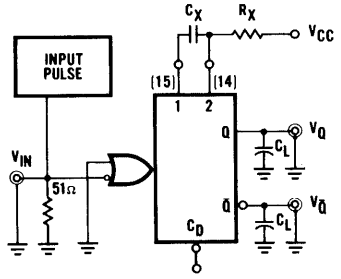


TRIGGERING TRUTH TABLE

PIN NO'S. 5(11)	4(12)	3(13)	Operation
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

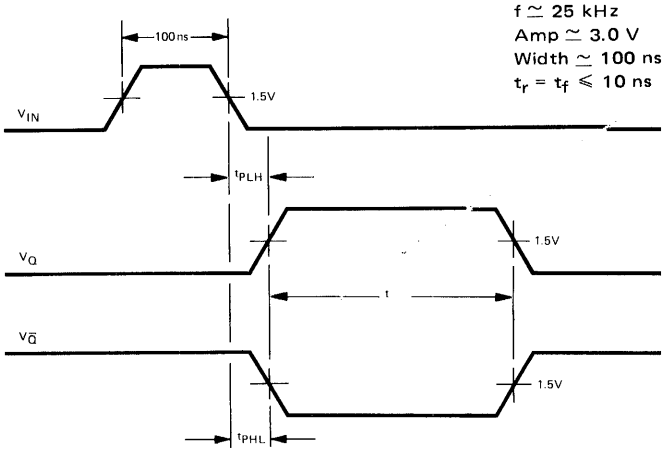
H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Don't Care (either H or L)
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

SWITCHING CIRCUITS AND WAVEFORMS



V_{CC} = Pin 16
GND = Pin 8

INPUT PULSE
f ≃ 25 kHz
Amp ≃ 3.0 V
Width ≃ 100 ns
$t_r = t_f \leq 10$ ns



TTL/MONOSTABLE 9603/54121, 74121
MONOSTABLE MULTIVIBRATOR

DESCRIPTION – The 9603/54121, 74121 is a TTL Monostable Multivibrator with dc triggering from positive or gated negative going inputs and with inhibit facility. Both positive and negative going output pulses are provided with full fan out to 10 normalized loads.

Pulse triggering occurs at a particular voltage level and is not directly related to the transition time of the input pulse. Schmitt-trigger input circuitry for the B input allows jitter-free triggering from inputs with transition times as slow as 1.0 V/S, providing the circuit with an excellent noise immunity of typically 1.2 V. A high immunity to V_{CC} noise of typically 1.5 V is also provided by internal latching circuitry.

Once fired, the outputs are independent of further transitions on the inputs and are a function only of the timing components. Input pulses may be of any duration relative to the output pulse. Output pulse lengths may be varied from 40 ns to 40 s by choosing appropriate timing components. With no external timing components (i.e., pin 9 connected to pin 14, pins 10, 11 open) an output pulse of typically 30 ns is achieved which may be used as a dc triggered reset signal. Output rise and fall times are TTL compatible and independent of pulse length.

Pulse width is achieved through internal compensation and is virtually independent of V_{CC} and temperature. In most applications, pulse stability will only be limited by the accuracy of external timing components.

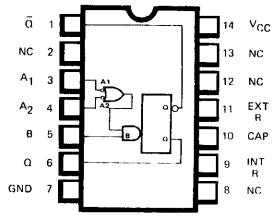
Jitter-free operation is maintained over the full temperature and V_{CC} range for more than six decades of timing capacitance (10 pF to 10 μF) and more than one decade of timing resistance (2 kΩ to 40 kΩ). Throughout these ranges, pulse width is defined by the relationship $t_{p(out)} = C_T R_T \log_e 2$.

Circuit performance is achieved with a nominal power dissipation of 90 mW at 5.0 V (50% duty cycle) and a quiescent dissipation of typically 65 mW.

Duty cycles as high as 90% are achieved when using R_T = 40 kΩ. Higher duty cycles are achievable if a certain amount of pulse-width jitter is allowed.

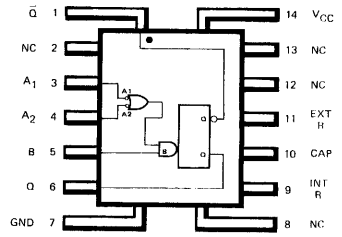
LOGIC AND CONNECTION DIAGRAM

DIP (TOP VIEW)



Note: 9–11 Timing Pins

FLATPAK (TOP VIEW)



Note: 9–11 Timing Pins

(See Notes 6 thru 9)

TRUTH TABLE (See Notes 1 thru 3)

t_n INPUT			t_{n+1} INPUT			OUTPUT
A_1	A_2	B	A_1	A_2	B	
H	H	L	H	H	H	Inhibit
L	X	H	L	X	L	Inhibit
X	L	H	X	L	L	Inhibit
L	X	L	L	X	H	One Shot
X	L	L	X	L	H	One Shot
H	H	H	X	L	H	One Shot
H	H	H	L	X	H	One Shot
X	L	L	X	H	L	Inhibit
L	X	L	H	X	L	Inhibit
X	L	H	H	H	H	Inhibit
L	X	H	H	H	H	Inhibit
H	H	L	X	L	L	Inhibit
H	H	L	L	X	L	Inhibit

Positive logic: See truth table and notes 5 and 6

H = $V_{IH} \geq 2$ V
L = $V_{IL} \leq 0.8$ V

NOTES:
1. t_n = time before input transition.
2. t_{n+1} = time after input transition.
3. X indicates that either a HIGH or LOW, may be present.
4. NC = No Internal Connection.
5. A_1 and A_2 are negative edge triggered-logic inputs, and will trigger the one shot when either or both go to LOW level with B at HIGH level.
6. B is a positive Schmitt-trigger input for slow edges or level detection and will trigger the one shot when B goes to HIGH level with either A_1 or A_2 at LOW level. (See Truth Table.)
7. External timing capacitor may be connected between pin 10 (positive) and pin 11. With no external capacitance, an output pulse width of typically 30 ns is obtained.
8. To use the internal timing resistor (2 kΩ nominal), connect pin 9 to pin 14.
9. To obtain variable pulse width connect external variable resistance between pin 9 and pin 14. No external current limiting is needed.
10. For accurate repeatable pulse widths connect an external resistor between pin 11 and pin 14 with pin 9 open-circuit.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−30 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +V_{CC} value
Output Current (dc) (Output LOW)	+30 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		9603XM/54121XM			9603XC/74121XC			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
Operating Free-Air Temperature Range		−55	25	125	0	25	70	°C
Normalized Fan Out from Each Output, N				10			10	U.L.
Input Pulse Rise/Fall Time:	Schmitt Input (B)			1.0			1.0	V/s
	Logic Inputs (A_1, A_2)			1.0			1.0	V/μs
Input Pulse Width		50			50			ns
External Timing Resistance Between Pins 11 and 14 (Pin 9 open)		1.4			1.4			kΩ
External Timing Resistance				30			40	kΩ
Timing Capacitance		0		1000	0		1000	μF
Output Pulse Width				40			40	s
Duty Cycle:	R_T = 2 kΩ			67%			67%	
	R_T = 30 kΩ			90%				
	R_T = 40 kΩ						90%	

X= package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

SYMBOL	PARAMETER		LIMITS MIN.	LIMITS TYP. (Note 2)	LIMITS MAX.	UNITS	TEST CONDITIONS (Note 1)	TEST* FIGURE
V_{T+}	Positive-Going Threshold Voltage at A Input			1.4	2.0	Volts	V_{CC} = MIN.	57
V_{T-}	Negative-Going Threshold Voltage at A Input		0.8	1.4		Volts	V_{CC} = MIN.	57
V_{T+}	Positive-Going Threshold Voltage at B Input			1.55	2.0	Volts	V_{CC} = MIN.	57
V_{T-}	Negative-Going Threshold Voltage at B Input		0.8	1.35		Volts	V_{CC} = MIN.	57
V_{OH}	Output HIGH Voltage		2.4	3.3		Volts	V_{CC} = MIN., I_{OH} = −0.4 mA	57
V_{OL}	Output LOW Voltage			0.22	0.4	Volts	V_{CC} = MIN., I_{OL} = 16 mA	57
I_{IH}	Input HIGH Current	at A_1 or A_2		2.0	40	μA	V_{CC} = MAX., V_{IN} = 2.4 V	60
				0.05	1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
		at B		4.0	80	μA	V_{CC} = MAX., V_{IN} = 2.4 V	61
				0.05	1.0	mA	V_{CC} = MAX., V_{IN} = 5.5 V	
I_{IL}	Input LOW Current	at A_1 or A_2		−1.0	−1.6	mA	V_{CC} = MAX., V_{IN} = 0.4 V	58
		at B		−2.0	−3.2	mA	V_{CC} = MAX., V_{IN} = 0.4 V	59
I_{OS}	Output Short Circuit Current at Q or $\overline{Q}$ (Note 3)		−20	−25	−55	mA	9603/54121	V_{CC} = MAX. 62 & 63
			−18	−25	−55	mA	9603/74121	
I_{CC}	Supply Current	in Quiescent (Unfired) State		13	25	mA	V_{CC} = MAX.	64
		in Fired State		23	40	mA	V_{CC} = MAX.	64

NOTES:
(1) For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions for the applicable device type.
(2) Typical limits are at V_{CC} = 5.0 V, 25°C.
(3) Not more than one output should be shorted at a time.

*See parameter measurement information in series 9N/54, 74TTL section.

SWITCHING CHARACTERISTICS (T_A = 25°C)

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS		TEST * FIGURE
		MIN.	TYP.	MAX.				
t_{PLH}	Turn Off Delay B Input to Q Output	15	35	55	ns	V_{CC} = 5.0 V C_L = 15 pF C_T = 80 pF		H
t_{PLH}	Turn Off Delay A_1/A_2 Inputs to Q Output	25	45	70				
t_{PHL}	Turn On Delay B Input to $\overline{Q}$ Output	20	40	65				
t_{PHL}	Turn On Delay A_1/A_2 Inputs to $\overline{Q}$ Output	30	50	80				
$t_{pw(out)}$	Pulse Width Obtained Using Internal Timing Resistor	70	110	150	ns	C_T = 80 pF	V_{CC} = 5.0 V C_L = 15 pF R_T = Open Pin 9 to V_{CC}	I
$t_{pw(out)}$	Pulse Width Obtained with Zero Timing Capacitance	20	30	50	ns	C_T = 0 pF		
$t_{pw(out)}$	Pulse Width Obtained Using External Timing Resistor	600	700	800	ns	C_T = 100 pF	V_{CC} = 5.0 V C_L = 15 pF R_T = 10 kΩ Pin 9 to Open	
		6.0	7.0	8.0	ms	C_T = 1.0 μF		
t_{hold}	Minimum Duration of Trigger Pulse		30	50	ns	C_T = 80 pF	V_{CC} = 5.0 V C_L = 15 pF R_T = Open Pin 9 to V_{CC}	

*See parameter measurement information in series 9N/54, 74 section.

TYPICAL CHARACTERISTICS

Fig. 1
VARIATION IN INTERNAL TIMING RESISTOR VALUE VERSUS AMBIENT TEMPERATURE

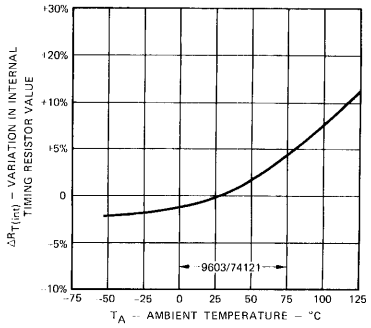


Fig. 2
VARIATION IN OUTPUT PULSE WIDTH VERSUS SUPPLY VOLTAGE

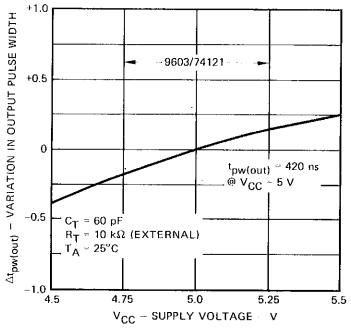


Fig. 3
VARIATION IN OUTPUT PULSE WIDTH VERSUS AMBIENT TEMPERATURE

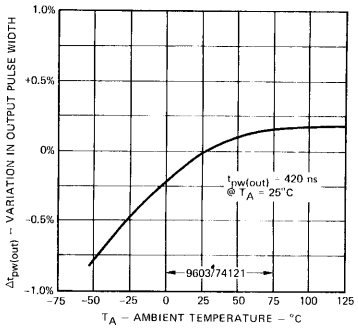


Fig. 4
SCHMITT TRIGGER THRESHOLD VOLTAGE VERSUS AMBIENT TEMPERATURE

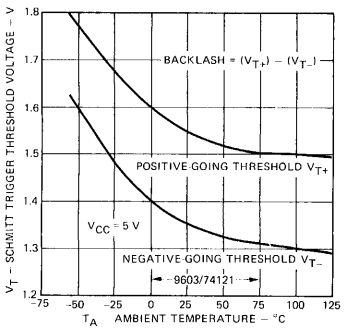


Fig. 5
TURN OFF DELAY TIME B INPUT TO Q OUTPUT VERSUS AMBIENT TEMPERATURE

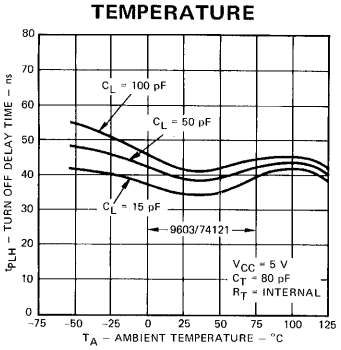
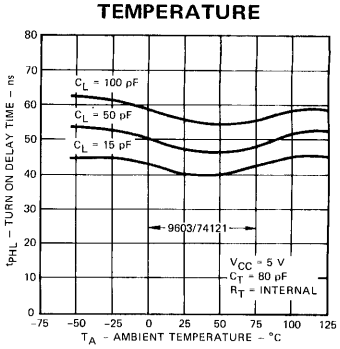


Fig. 6
TURN ON DELAY TIME B INPUT TO $\overline{Q}$ OUTPUT VERSUS AMBIENT TEMPERATURE



TYPICAL CHARACTERISTICS (Cont'd)

Fig. 7
OUTPUT PULSE WIDTH
VERSUS
TIMING RESISTOR VALUE

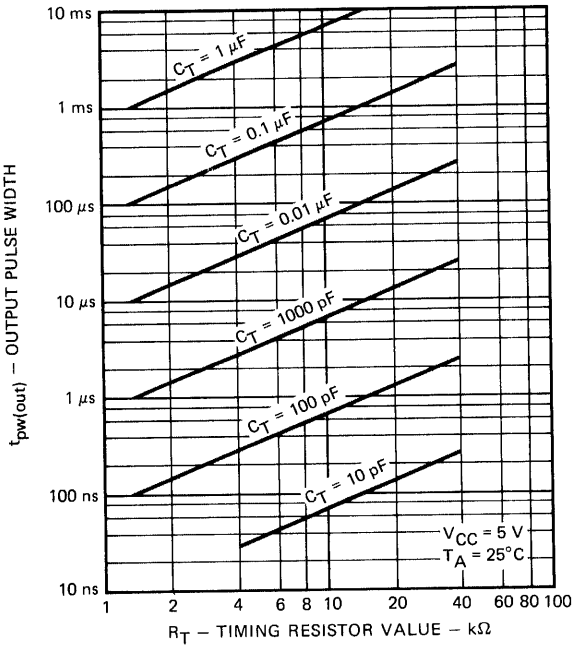
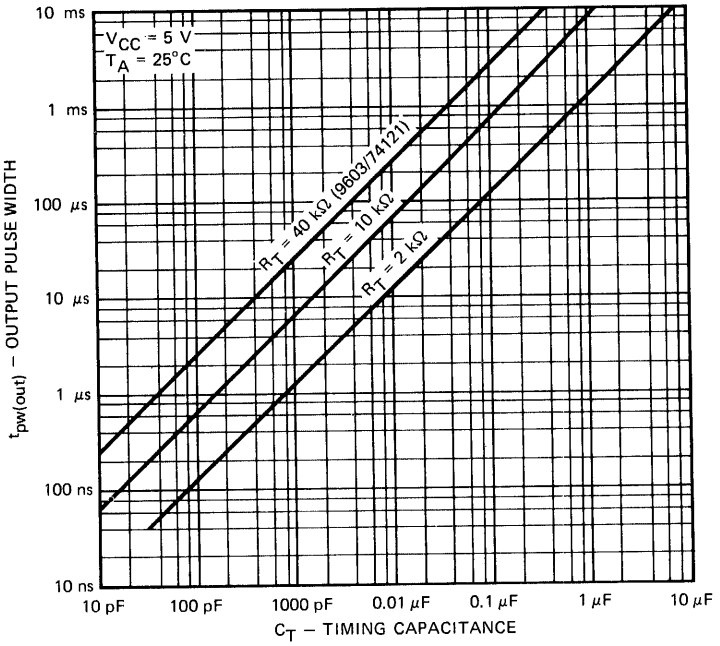


Fig. 8
OUTPUT PULSE WIDTH
VERSUS
EXTERNAL CAPACITANCE



μA9614

DUAL DIFFERENTIAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The μA9614 is a TTL compatible Dual Differential Line Driver. It is designed to drive transmission lines either differentially or single-ended, back-matched or terminated. The outputs are similar to TTL, with the active pull-up and the pull-down split and brought out to adjacent pins. This allows multiplex operation (Wired-OR) at the driving site in either the single-ended mode via the uncommitted collector, or in the differential mode by use of the active pull-ups on one side and the uncommitted collectors on the other (See Fig. 5). The active pull-up is short circuit protected and offers a low output impedance to allow back-matching. The two pairs of outputs are complementary providing "NAND" and "AND" functions of the inputs, adding greater flexibility. The input and output levels are TTL compatible with clamp diodes provided at both input and output to handle line transients.

- **SINGLE 5 VOLT SUPPLY**
- **TTL COMPATIBLE INPUTS**
- **OUTPUT SHORT CIRCUIT PROTECTION**
- **INPUT CLAMP DIODES**
- **OUTPUT CLAMP DIODES FOR TERMINATION OF LINE TRANSIENTS**
- **COMPLIMENTARY OUTPUTS FOR 'NAND', 'AND' OPERATION**
- **UNCOMMITTED COLLECTOR OUTPUTS FOR WIRED-OR APPLICATION**
- **MILITARY TEMPERATURE RANGE**

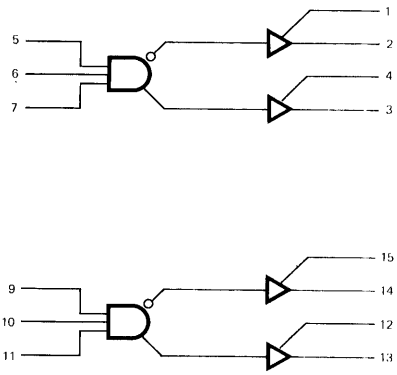
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.7 V to +7.0 V
Input Voltage	−0.5 V to +5.5 V
Voltage Supplied to Outputs (Open Collector)	−0.5 V to +12 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
Ceramic DIP	730 mW
Flatpak	570 mW

NOTE

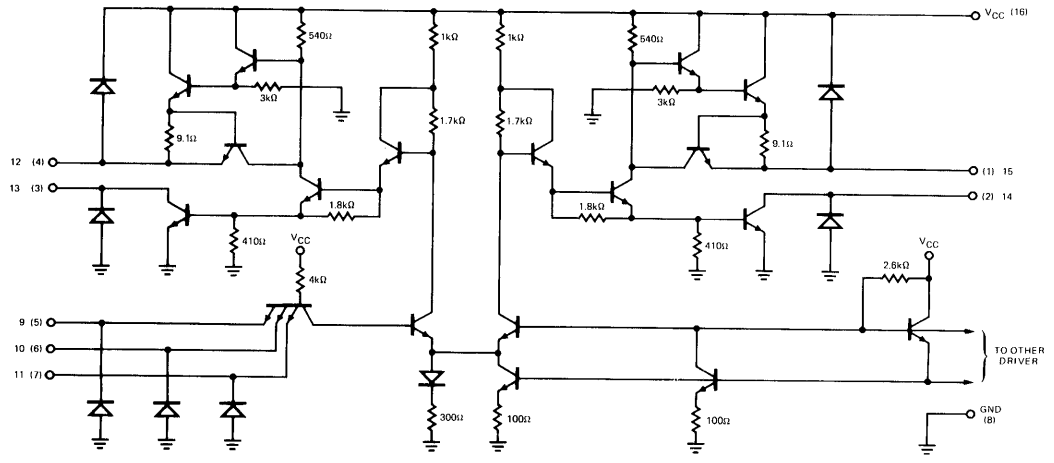
1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8

EQUIVALENT CIRCUIT (1/2 9614)



μA9615

DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9615 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges using a single 5 V supply. It can receive ±500 mV of differential data in the presence of high level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output.

The response time can be controlled by use of an external capacitor. A strobe and a 130 Ω terminating resistor are provided at the inputs. The output has an uncommitted collector with an active pull-up available on an adjacent pin to allow either "wire-or" or active pull up TTL output configuration.

- **TTL COMPATIBLE OUTPUT**
- **HIGH COMMON MODE VOLTAGE RANGE**
- **CHOICE OF AN UNCOMMITTED COLLECTOR OR ACTIVE PULL-UP**
- **STROBE**
- **FULL MILITARY TEMPERATURE RANGE**
- **SINGLE 5 V SUPPLY VOLTAGES**
- **FREQUENCY RESPONSE CONTROL**
- **130 Ω TERMINATING RESISTOR**

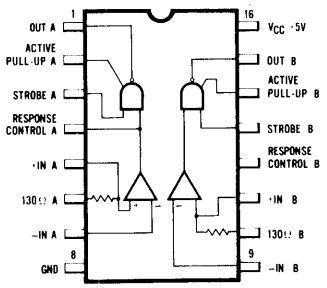
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65° C to +150° C
Temperature (Ambient) Under Bias	−55° C to +125° C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Pins 5, 6, 7, 9, 10, 11)	±20 V
Voltage Applied to Outputs for HIGH Output State without Active Pull Up	−0.5 V to +13.2 V
Voltage Applied to Strobe	−0.5 V to +5.5 V
Lead Temperature (Soldering, 60 seconds)	300° C
Internal Power Dissipation (Note 1)	
Ceramic DIP	730 mW
Flatpak	570 mW

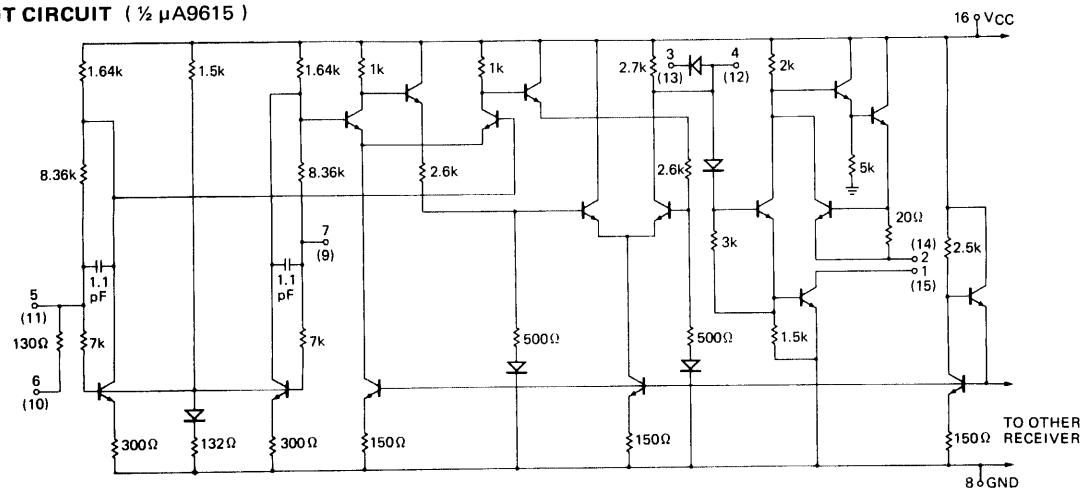
NOTE

1. Rating applies to ambient temperatures up to 70° C. Above 70° C derate linearly at 8.3 mW/° C for the Ceramic DIP and 7.1 mW/° C for the Flatpak Package.

LOGIC DIAGRAM



EQUIVALENT CIRCUIT (½ μA9615)



μA9616

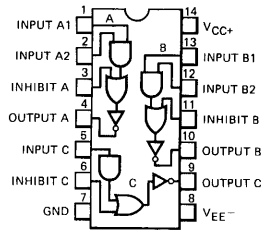
TRIPLE EIA RS-232-C LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9616 is a Triple Line Driver which meets the electrical interface specifications of EIA RS-232-C and CCITT V.24. Each driver in the μA9616 converts TTL/DTL logic level to EIA/CCITT levels for transmission between data terminal equipment and data communication equipment. The μA9617 performs the complementary functions. The output slew rate is internally limited and can be lowered by an external capacitor; all output currents are short circuit limited. The outputs are protected against RS-232-C fault conditions. A logic HIGH level on the inhibit terminal interrupts signal transfer and forces the output to a $-V_{OUT}$ or MARK state. The μA9616 is constructed on a single silicon chip using the Fairchild Planar* process.

- **INTERNAL SLEW RATE LIMITING**
- **NO EXTERNAL CAPACITORS REQUIRED**
- **THREE CHANNELS PER PACKAGE**
- **MEETS EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **LOGICAL TRUE INHIBIT FUNCTION**
- **SUPPLY INDEPENDENT OUTPUT SWING**
- **OUTPUT CURRENT LIMITING**

CONNECTION DIAGRAM
(TOP VIEW)



TRUTH TABLE

INPUT 1	INPUT 2	INHIBIT	OUTPUT
All Sections:			
L	L	L	H
H	H	L	L
L	L	H	L
H	H	H	L
For Channels A & B add:			
L	H	L	H
H	L	L	H
L	H	H	L
H	L	H	L

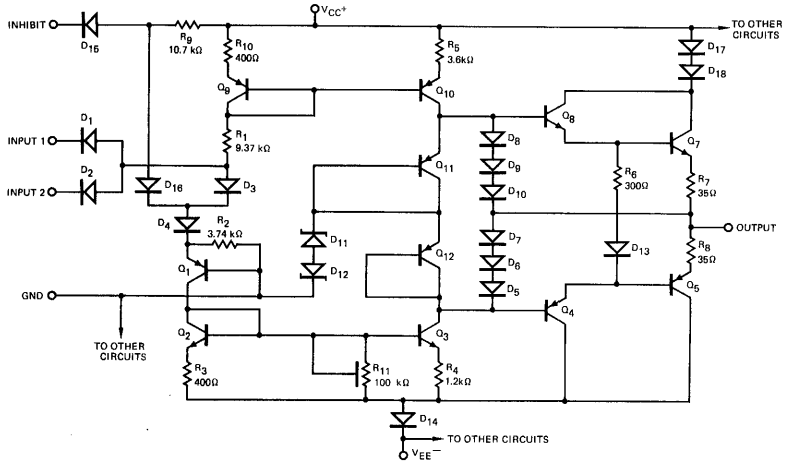
(For Channel C, omit INPUT 2 Column)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±15 V
Input or Inhibit Voltage	−1.5 to +6 V
Output Signal Voltage	±15 V
Maximum Power Dissipation (Note 1)	630 mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature	0°C to +75°C
Lead Temperature (Soldering, 60 seconds)	300°C

Note 1: Perate 8.3mW/°C above 70°C

EQUIVALENT CIRCUIT (One of three channels)



*Planar is a patented Fairchild process.

μA9617

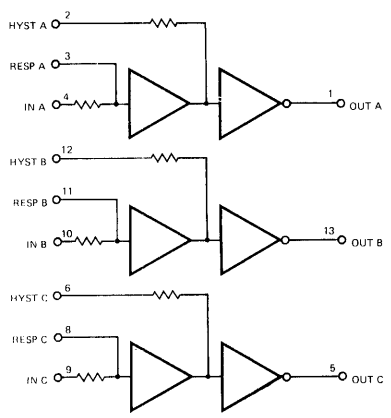
TRIPLE EIA RS-232-C LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The μA9617 is a Triple Line Receiver designed to meet the terminator electrical requirements of EIA RS-232-C AND CCITT V.24. It receives line signals produced by the μA9616, an EIA/CCITT driver, and converts them to TTL compatible logic levels. The inputs have a resistance between 3 kΩ and 7 kΩ and can withstand ±25 V. Each receiver can operate in either hysteresis or non-hysteresis (slicing) modes, and each receiver provides fail-safe operation as defined by Section 2.5 of RS-232-C. Noise immunity may be increased by connecting a capacitor between the response control pin and ground. The μA9617 is constructed on a single silicon chip using the Fairchild Planar* process.

- **MEETS ALL EIA RS-232-C AND CCITT V.24 SPECIFICATIONS**
- **FAIL-SAFE OPERATION**
- **HYSTERESIS OR NON-HYSTERESIS MODE**
- **INDIVIDUAL RESPONSE CONTROLS**
- **TTL COMPATIBLE OUTPUT**
- **SINGLE +5 V SUPPLY**

LOGIC DIAGRAM



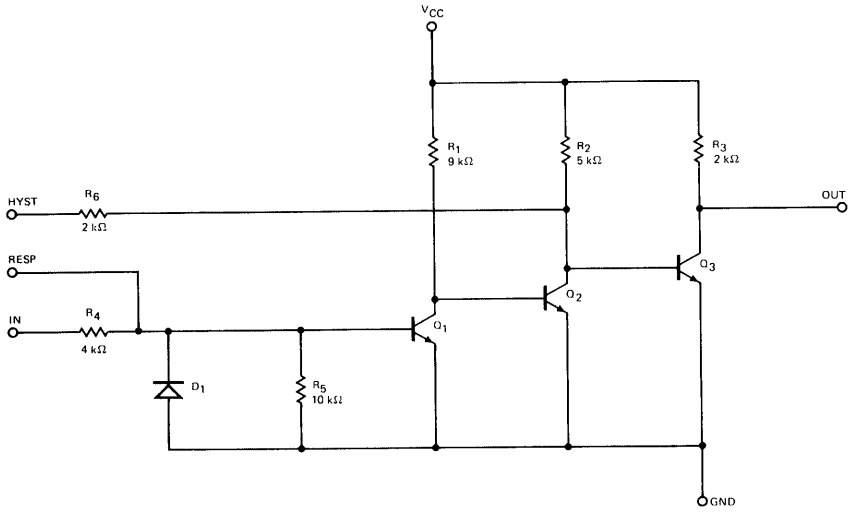
V_{CC} = Pin 14
GND = Pin 7

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7 V
Input Voltage	±25V
Output Current	25 mA
Maximum Power Dissipation (Note 1)	630mW
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +75°C
Lead Temperature (Soldering, 60 seconds)	300°C

Note 1. Derate 8.3 mW/°C above 70°C

EQUIVALENT CIRCUIT (One of three identical circuits)



*Planar is a patented Fairchild process.

μA9620

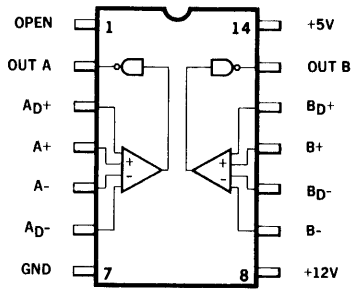
DUAL DIFFERENTIAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The μA9620 is a Dual Differential Line Receiver designed to receive differential digital data from transmission lines and operate over the military and industrial temperature ranges. It can receive ±500 mV of differential data in the presence of HIGH level (±15 V) common mode voltages and deliver undisturbed TTL logic to the output. In addition to line reception the μA9620 can perform many functions, a few of which are presented in the applications section. It can interface with nearly all input logic levels including CML, CTL, HLLDTL, RTL and TTL. HLLDTL logic can be provided by tieing the output to V_{CC2} (+12 V) through a resistor. The outputs can also be wired-OR. The μA9620 offers the advantages of logic compatible voltages (+5 V, +12 V), TTL output characteristics, and a flexible input array with a high common mode range. The direct inputs are provided in addition to the attenuated inputs (normally used) to allow the input attenuation and response time to be changed by use of external components.

- TTL COMPATIBLE OUTPUT
- HIGH COMMON MODE VOLTAGE RANGE
- WIRED-OR CAPABILITY
- DIRECT INPUTS (A_D, B_D)
- FULL MILITARY TEMPERATURE RANGE
- LOGIC COMPATIBLE SUPPLY VOLTAGES

LOGIC DIAGRAM



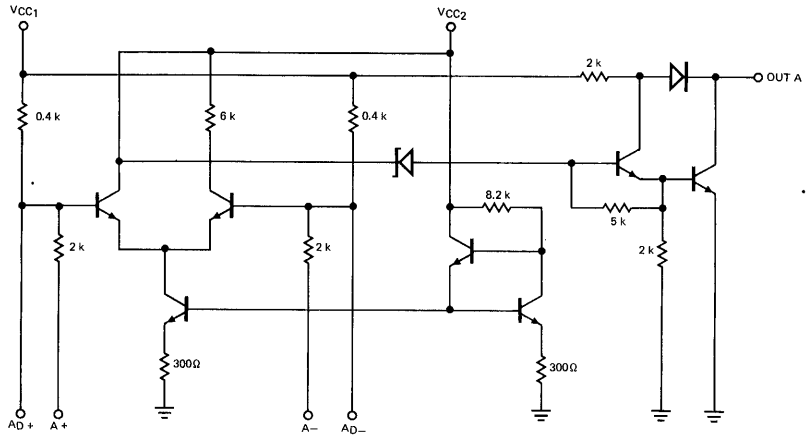
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC1} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage Referred to Ground (Attenuator Inputs)	±20 V
Voltage Applied to Outputs for HIGH Output State	−0.5 V to +13.2 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
Lead Temperature (Soldering, 60 seconds)	300°C
Internal Power Dissipation (Note 1)	
Ceramic DIP	670 mW
Flatpak	570 mW

NOTE

1. Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP and 7.1 mW/°C for the Flatpak Package.

EQUIVALENT CIRCUIT



7

μA9621

DUAL LINE DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9621 was designed to drive transmission lines in either a differential or a single-ended mode. Output clamp diodes and back-matching resistors for 130 Ω twisted pair are provided. The output has the capability of driving high capacitance loads. It can typically switch >200 mA during transients.

- **TTL COMPATIBILITY**
- **TRANSMISSION LINE BACK-MATCHING**
- **OUTPUT CLAMP DIODES**
- **HIGH CAPACITANCE DRIVE**
- **HIGH OUTPUT VOLTAGE**
- **MILITARY TEMPERATURE RANGE**

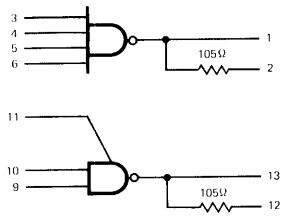
ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65° C to +150° C
Temperature (Ambient) Under Bias	−55° C to +125° C
V_{CC1} Pin Potential to Ground Pin	+3.8 V to +8 V
Input Voltage	−0.5 V to +15 V
Voltage Applied to Outputs	−2 V to +V_{CC1} +1 V
V_{CC2} Pin Potential to Ground Pin	V_{CC1} to +15 V
Lead Temperature (Soldering, 60 seconds)	300° C
Internal Power Dissipation (Note)	
Ceramic DIP	670 mW
Flatpak	570 mW

NOTE

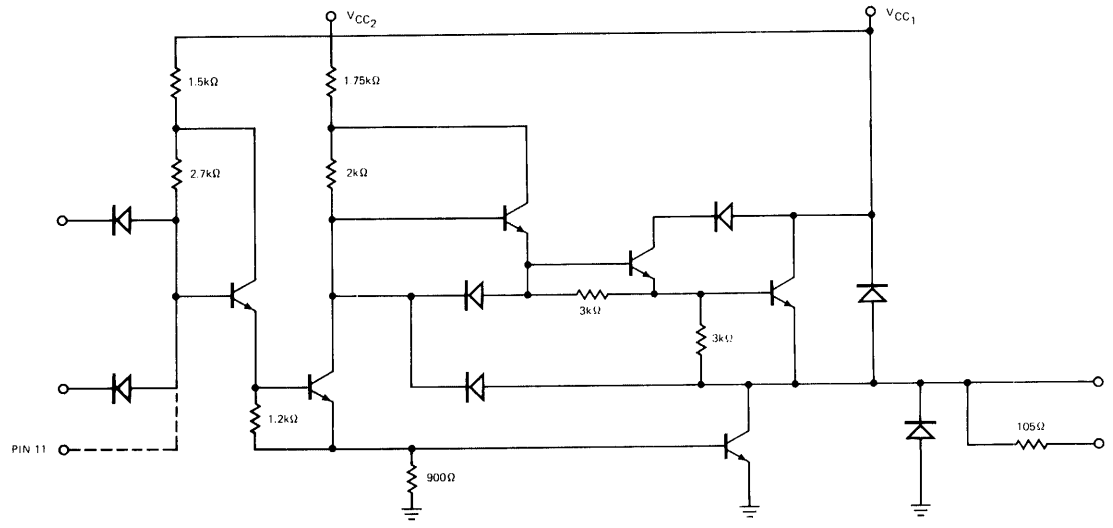
Rating applies to ambient temperatures up to 70° C. Above 70° C derate linearly at 8.3 mW/° C for the Ceramic DIP and 7.1 mW/° C for the Flatpak Package.

LOGIC DIAGRAM



V_{CC_1} = 14, V_{CC_2} = 8, GND = 7

SCHEMATIC DIAGRAM (ONE SIDE ONLY)



μA9622

DUAL LINE RECEIVER

FAIRCHILD LINEAR INTEGRATED CIRCUIT

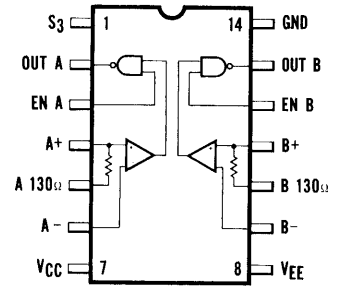
GENERAL DESCRIPTION – The μA9622 is a Dual Line Receiver designed to discriminate a worst case logic swing of 2.0 V from a ±10 V common mode noise signal or ground shift. A 1.5 V threshold is built into the differential amplifier to offer a TTL compatible threshold voltage and maximum noise immunity. The offset is obtained by use of current sources and matched resistors and varies only ±5% (75 mV) over the military and industrial temperature ranges.

The μA9622 allows the choice of output states with the inputs open without affecting circuit performance by use of S_3*. A 130 Ω terminating resistor is provided at the input of each line receiver. An enable is also provided for each line receiver. The output is TTL compatible. The output HIGH level can be increased to +12 V by tieing it to a positive supply through a resistor. The output circuits allow wired-OR operation.

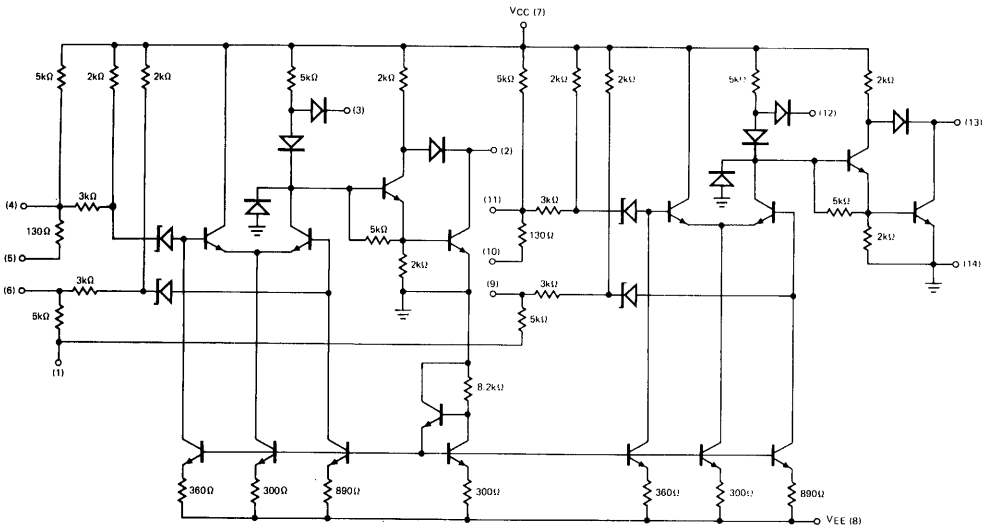
*S_3 connected to V_{CC} – open inputs causes output to be V_{OH}.
S_3 connected to Ground – open inputs causes output to be V_{OL}.

- TTL COMPATIBLE THRESHOLD VOLTAGE
- INPUT TERMINATING RESISTORS
- CHOICE OF OUTPUT STATE WITH INPUTS OPEN
- TTL COMPATIBLE OUTPUT
- HIGH COMMON MODE
- WIRE-OR CAPABILITY
- ENABLE INPUTS
- FULL MILITARY TEMPERATURE RANGE
- LOGIC COMPATIBLE SUPPLY VOLTAGES

LOGIC DIAGRAM



EQUIVALENT CIRCUIT



μA9624 • μA9625

DUAL TTL, MOS INTERFACE ELEMENTS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9624 is a Dual 2-Input TTL Compatible Interface gate specifically designed to drive MOS. The output swing is adjustable and will allow it to be used as a data driver, clock driver or discrete MOS driver. It has an active output for driving medium capacitive loads.

The μA9625 is a dual MOS to TTL level converter. It is designed to convert standard negative MOS logic levels to TTL levels. The μA9625 features a high input impedance which allows preservation of the driving MOS logic level.

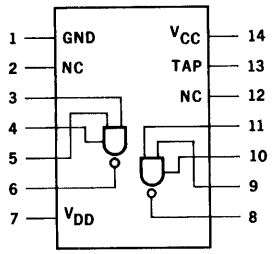
Both the μA9624 and μA9625 are available in the 14-lead Ceramic Dual In-Line Package and the 1/4 x 1/4 Flatpak.

NOTE: The TTL and MOS devices manufactured by Fairchild Semiconductor are considered as positive TRUE logic (the more positive voltage level is assigned the binary state of "1" or TRUE). Following MIL-STD-806B logic symbol specifications, the μA9624 is represented as a NAND gate and the μA9625 as a non-inverting buffer. This convention (of assuming MOS as a positive TRUE logic) has not been uniformly accepted by the industry; therefore, it is necessary to note that with negative TRUE MOS logic (the more negative voltage level is assigned the binary state "1" or TRUE), the μA9624 acts as an AND gate and the μA9625 as an inverter.

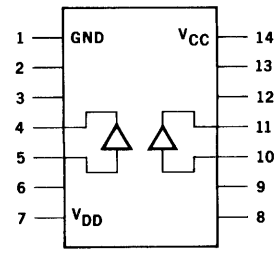
- **TTL COMPATIBLE INPUTS/OUTPUT**
- **MOS COMPATIBLE OUTPUT/INPUTS**
- **LOW POWER**

LOGIC DIAGRAMS

μA9624



μA9625



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	V_{DD} to +10 V
Voltage Applied to Outputs for HIGH Output State (μA9624)	V_{DD} to +V_{CC} value
Voltage Applied to Outputs for HIGH Output State (μA9625)	−0.5 V to V_{CC} value
Input Voltage (dc) (μA9624)	−0.5 V to +5.5 V
Input Voltage (dc) (μA9625)	V_{CC} to V_{DD}
V_{DD} Pin Potential to Ground Pin	−30 V to +0.5 V
V_{DD} Pin Potential to Tap Pin (μA9624)	−30 V to +0.5 V
V_{TAP}	V_{CC} +0.5 V
Internal Power Dissipation (Note 3)	
Ceramic DIP	670 mW
Flatpak	570 mW
Lead Temperature (Soldering, 60 seconds)	300°C

μA9644

DUAL HIGH VOLTAGE, HIGH CURRENT DRIVER

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION – The μA9644 is a Dual 4-Input NAND Gate whose output can sink 500 mA in the LOW state, and maintain 30 V in the HIGH state. The outputs are uncommitted collectors in a Darlington configuration which have typical saturation voltages of 0.8 V at low currents and 1.2 V at 500 mA. The inputs are TTL Compatible and feature input clamp diodes. The input fan in requirement is typically 1/2 a normal DTL Unit Load. An input strobe common to both gates in provided, and an expander input node on each gate is available for input diode expansion. Separate ground pins are provided for each gate to minimize ground pin offset voltages at high current levels.

- **500 mA CURRENT SINKING CAPABILITY**
- **OUTPUT VOLTAGES UP TO 30 V**
- **LOW AVERAGE POWER, TYPICALLY 30 mW PER GATE**
- **HIGH SPEED, TYPICALLY 50 ns DELAY TIMES**
- **TTL COMPATIBLE INPUTS**
- **INPUT CLAMP DIODES**
- **LOW FAN IN LOADING REQUIREMENTS**
- **COMMON STROBE INPUT**
- **EXPANDER NODE FOR INPUT DIODE EXPANSION**

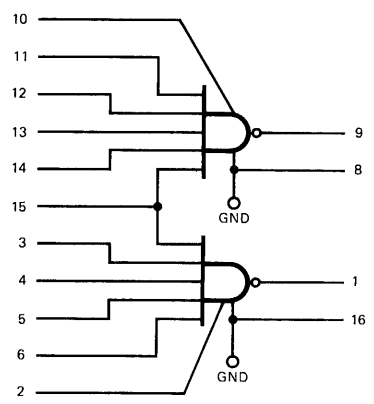
ABSOLUTE MAXIMUM RATING

Storage Temperature		−65°C to +175°C
Temperature (Ambient) Under Bias		−55°C to +125°C
V_{CC} Pin Potential to Ground Pin		−0.5 V to +8.0 V
Input Voltages (dc)		−0.5 V to +5.5 V
Voltage Applied to Outputs (Output HIGH)	See Safe Area Curves on following pages	−0.5 V to +30 V
Output Current (dc) (Output LOW)		640 mA
Internal Power Dissipation (Note)		730 mW
Lead Temperature (Soldering, 60 seconds)		300°C

NOTE

Rating applies to ambient temperatures up to 70°C. Above 70°C derate linearly at 8.3 mW/°C for the Ceramic DIP.

LOGIC DIAGRAM



V_{CC} = Pin 7

Fig. 1

CONNECTION DIAGRAM

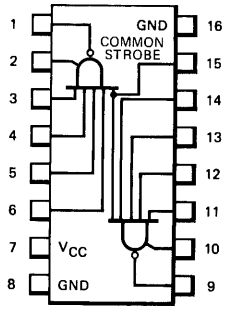
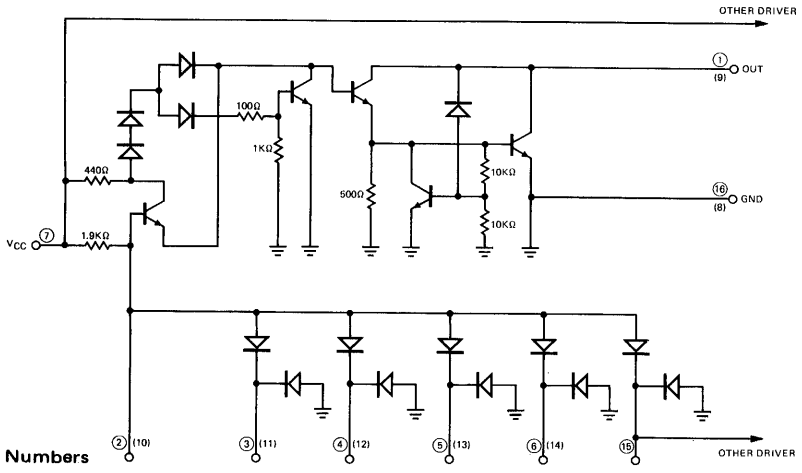


Fig. 2

EQUIVALENT CIRCUIT (One of two identical channels)



SN55107 • SN75107 • SN55108 • SN75108

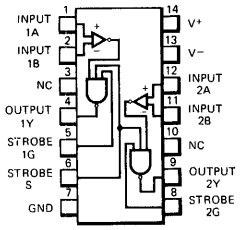
DUAL LINE RECEIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

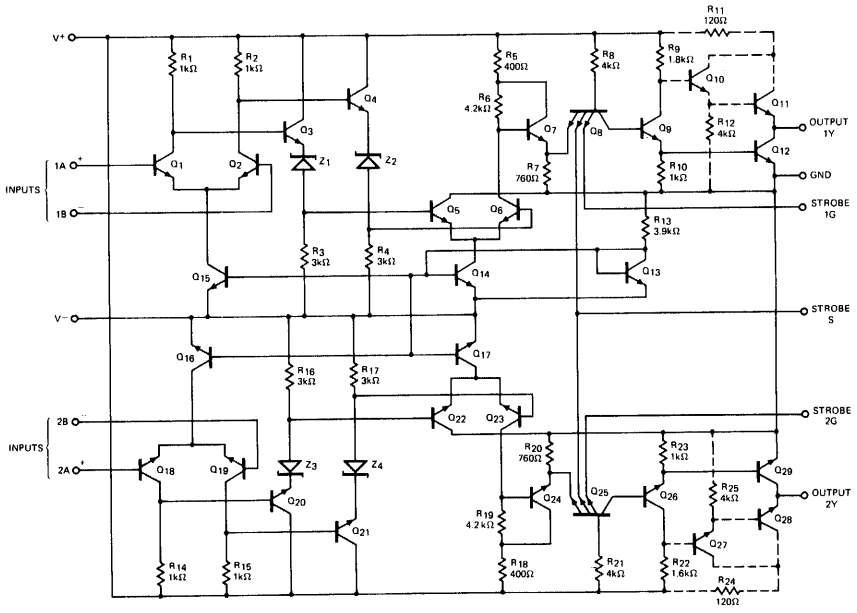
DESCRIPTION—The SN55107/75107 and SN55108/75108 are high speed, Two-Channel Line Receivers with common voltage supply and ground terminals. They are designed to detect input signals of 25mV (or greater) amplitude and convert the polarity of the signal into appropriate TTL compatible output logic levels. They feature high input impedance and low input currents which induce very little loading on the transmission line making these devices ideal for use in party line systems. The receiver input common mode voltage range is ±3V but can be increased to ±15V by the use of input attenuators. Separate or common strobes are available. The SN55107/75107 circuit features an active pull-up (totem pole output). The SN55108/75108 circuit features an open collector output configuration that permits wired-OR connections. The receivers are designed to be used with the SN55109/75109 and SN55110/75110 line drivers. The SN55107/75107 and SN55108/75108 line receivers are useful in high speed balanced, unbalanced and party line transmission systems and as data comparators.

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **HIGH COMMON-MODE REJECTION RATIO**
- **HIGH INPUT IMPEDANCE**
- **HIGH INPUT SENSITIVITY**
- **INPUT COMMON-MODE VOLTAGE RANGE OF ±3V**
- **SEPARATE OR COMMON STROBES**
- **TTL OR DTL DRIVE CAPABILITY**
- **WIRED-OR OUTPUT CAPABILITY (SN55108/75108 ONLY)**
- **HIGH DC NOISE MARGINS**

CONNECTION DIAGRAM
(TOP VIEW)



EQUIVALENT CIRCUIT



NOTE: Components shown with dashed lines are applicable to the SN55107 and SN75107 only.

SN55109 • SN75109 • SN55110 • SN75110

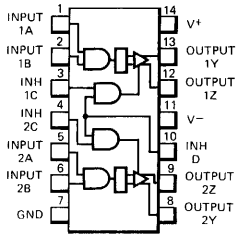
DUAL LINE DRIVERS

FAIRCHILD LINEAR INTEGRATED CIRCUITS

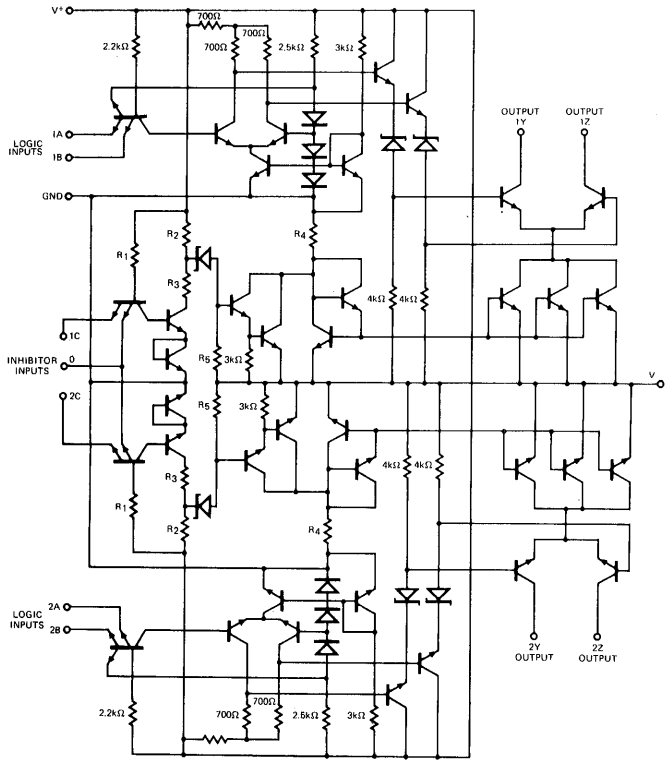
DESCRIPTION – The SN55109/75109 and SN55110 are Dual Line Drivers featuring independent channels with common supply voltage and ground terminals. The major difference between the SN55109/75109 and the SN55110/75110 drivers is the output-current specification. The output current is nominally 6 mA for the SN55109/75109 and 12 mA for the SN55110/75110. The driver circuits have a constant output that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off by appropriate logic levels at the inhibit inputs. The circuit also features an inhibit input that is common to both drivers, providing more circuit versatility. The common-mode voltage range of the driver outputs is –3 V to +10 V, which allows a common-mode voltage on the line without affecting the driver performance. For application information see SN55107 • SN75107 • SN55108 • SN75108 Data Sheet.

- **HIGH SPEED**
- **STANDARD SUPPLY VOLTAGES**
- **DUAL CHANNELS**
- **TTL INPUT COMPATIBILITY**
- **CURRENT-MODE OUTPUT (6mA or 12mA TYPICAL)**
- **HIGH OUTPUT IMPEDANCE**
- **HIGH COMMON-MODE OUTPUT VOLTAGE RANGE (–3V to 10V)**
- **INHIBITOR AVAILABLE FOR DRIVER SELECTION**

CONNECTION DIAGRAM
(TOP VIEW)



EQUIVALENT CIRCUIT



	SN55109 SN75109	SN55110 SN75110
R_1	4 kΩ	2.2 kΩ
R_2	1.5 kΩ	820 Ω
R_3	440 Ω	240 Ω
R_4	1.75 kΩ	875 Ω
R_5	2.74 kΩ	1.5 kΩ

NOTES:
1. Component values shown are nominal.
2. Resistance values are in ohms.

SN75450

DUAL PERIPHERAL DRIVER

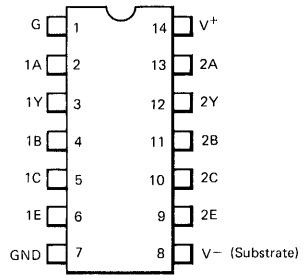
FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The SN75450 is a versatile general purpose dual interface driver circuit that employs TTL or DTL logic. The SN75450 features two standard series 74 TTL gates and two uncommitted, high current, high voltage transistors offering the system designer the flexibility to tailor the circuit to his application. The SN75450 is useful in high speed logic buffers, power drivers, lamp drivers, relay drivers, line drivers, MOS drivers, clock drivers and memory drivers.

- **HIGH SPEED**
- **300 mA CURRENT CAPABILITY**
- **HIGH VOLTAGE CAPABILITY**
- **UNCOMMITTED OUTPUT DEVICES**
- **TTL OR DTL INPUT COMPATIBILITY**

CONNECTION DIAGRAM
(TOP VIEW)

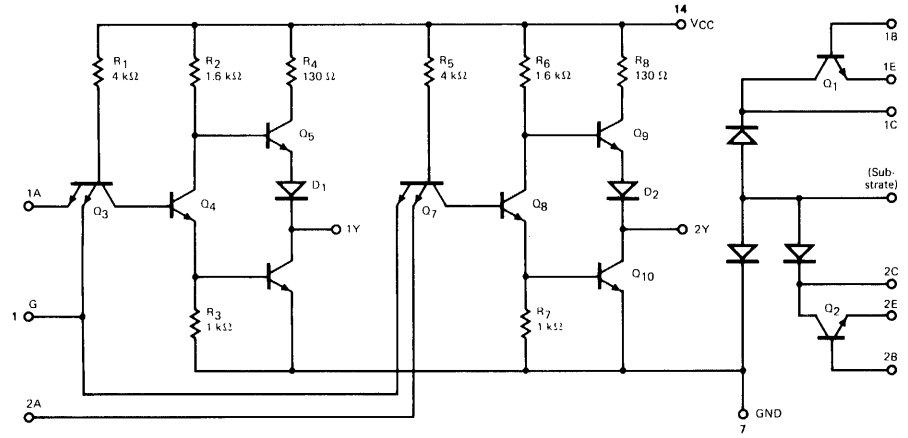
14 LEAD DIP



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (Note 1)	+7 V
Internal Power Dissipation (Note 2)	800 mW
Input Voltage (Note 3)	5.5 V
V_{CC} to Substrate or Collector to Substrate Voltage	35 V
Collector to Base Voltage	35 V
Emitter To Base Voltage	5 V
Collector to Base Voltage (Note 4)	30 V
Continuous Collector Current	300 mA
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature Range (Soldering, 60 seconds)	300°C

EQUIVALENT CIRCUIT



BLOCK DIAGRAM