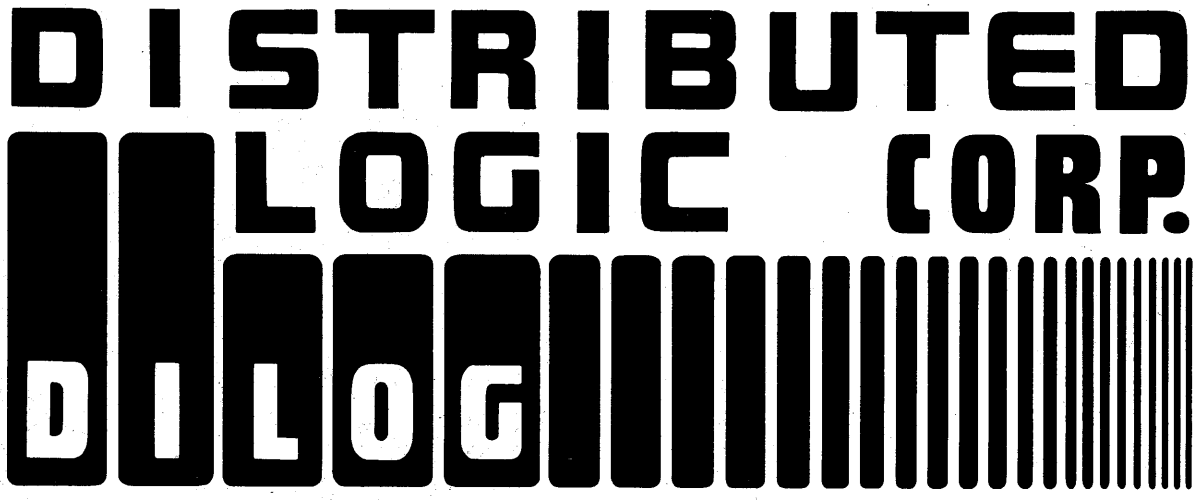
MODEL DQ215
DISC CONTROLLER
INSTRUCTION MANUAL



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MODEL DQ215
DISC CONTROLLER
INSTRUCTION MANUAL

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INTRODUCTION

This manual describes the installation, operation, programming, troubleshooting, and theory of operation of Distributed Logic Corporation (DILOG) Model DQ215 Disc Controller. The controller interfaces DEC* LSI-11 based computer systems to one or two SMD I/O disc drives, including 8- and 14-inch Winchester, SMD pack and CMD cartridge type drives. The complete controller occupies one quad module in the backplane. Full sector buffering in the controller matches the transfer rate of the disc drive and the CPU. The controller is compatible with RK06/RK07 software drivers in RT-11, RSX-11 and RSTS.

CONTROLLER CHARACTERISTICS

The disc controller links the LSI-11 computer to one or two disc storage units. Commands from the computer are received and interpreted by the controller and translated into a form compatible with the disc units. Buffering and signal timing for data transfers between the computer and the discs are performed by the controller.

A microprocessor is the sequence and timing center of the controller. The control information is stored as firmware instructions in read-only-memory (ROM) on the controller board. One section of the ROM contains a diagnostic program that tests the functional operation of the controller. This self-test is performed automatically each time power is applied. A green diagnostic indicator on the controller board lights if self-test passes.

Data transfers are directly to and from the computer memory using the DMA facility of the LSI-11 I/O bus. In addition, the controller monitors the status of the disc units and the data being transferred and presents this information to the computer upon request. An error correction code with a 56-bit checkword corrects error bursts up to 11 bits. To compensate for media errors, bad sectors are skipped and alternates assigned, and there is an automatic retry feature for read errors. The controller is capable of addressing four megabytes and controlling up to two disc drives in various configurations up to a total on-line formatted capacity of 220.32 megabytes. Figure 1-1 is a simplified diagram of a disc system.

*DEC, RSX and RSTS are registered trademarks of Digital Equipment Corporation.

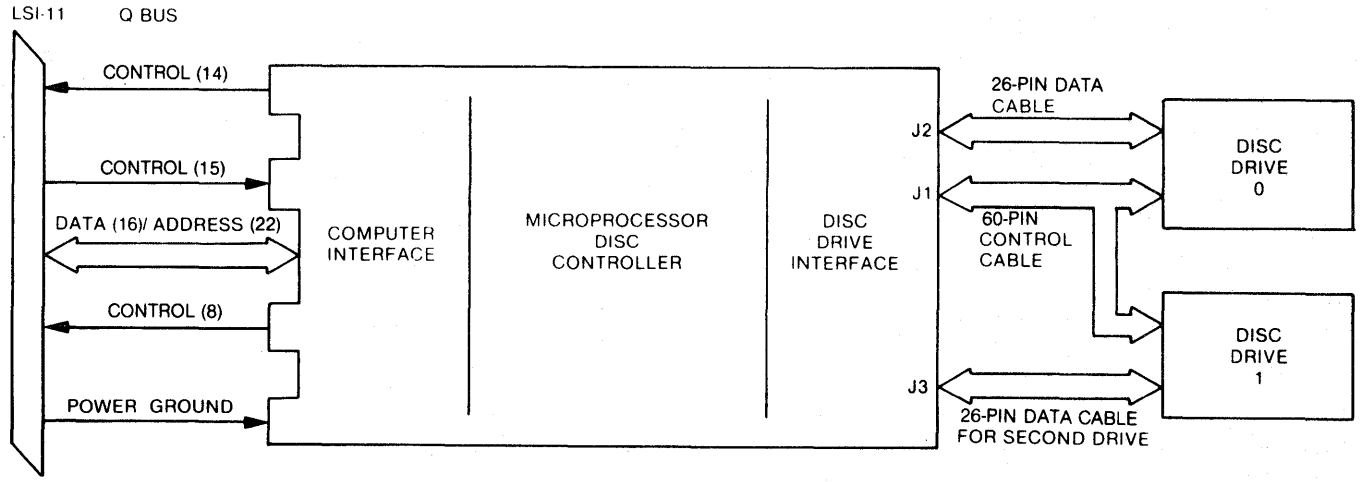


Figure 1-1. Disc Controller System Simplified Diagram

LSI-11 Q BUS INTERFACE

Commands, data and status transfers between the controller and the computer are executed via the parallel I/O bus (Q bus) of the computer. Data transfers are direct to memory via the DMA facility of the Q bus; commands and status are under programmed I/O. Controller/Q bus interface lines are listed in Table 1-1.

Table 1-1. Controller/Q-Bus Interface Lines

Bus Pin	Mnemonic	Controller Input/ Output	Description
AC2, AJ1, AM1, AT1, BJ1, BM1, BT1, BC2, CC2, CJ1, CM1, CT1, DC2, DJ1, DM1, DT1	GND	O	Signal Ground and DC return.
AN1	BDMR L	O	Direct Memory Access (DMA) request from controller: active low.
AP1	BHALT L	N/A	Stops program execution. Refresh and DMA is enabled. Console operation is enabled.
AR1	BREF L	N/A	Memory Refresh.
BA1	BDCOK H	I	DC power ok. All DC voltages are normal.
BB1	BPOK H	N/A	Primary power ok. When low activates power fail trap sequence.
BN1	BSACK L	O	Select Acknowledge. Interlocked with BDMGO indicating controller is bus master in a DMA sequence.
BR1	BEVNT L	O	External Event Interrupt Request. Real Time Clock Control.
AA2, BA2, BV1, CA2, DA2	+5	I	+5 volt system power.
AD2, BD2	+12	N/A	+12 volt system power.
AE2	BDOUT L	I/O	Data Out. Valid data from bus master is on the bus. Interlocked with BRPLY.
AF2	BRPLY L	I/O	Reply from slave to BDOUT or BDIN and during IAK.
AH2	BDIN L	I/O	Data Input. Input transfer to master (states master is ready for data). Interlocked with BRPLY.
AJ2	BSYNC L	I/O	Synchronize: becomes active when master places address on bus; stays active during transfer.
AK2	BWTBT L	I/O	Write Byte: indicates output sequence to follow (DATO or DATOB) or marks byte address time during a DATOB.
AA1, AB1, AL2, BP1	BIRQ4L,5,6,7	O	Interrupt Request.
AM2 AN2 CM2 CN2	BIAK1I L BIAK1O L BIAK2I L BIAK2O L	I O I O	Serial Interrupt Acknowledge input and output lines routed from Q-Bus, through devices, and back to processor to establish and interrupt priority chain.
AT2	BINIT L	I	Initialize. Clears devices on I/O bus.
AU2, AV2, BE2, BF2, BH2, BH2, BK2, BL2, BM2, BN2, BP2, BR2, BS2, BT2, BU2, BV2	BDAL0 L through BDAL15 L	I/O	Data/address lines, 0-15
AR2 AS2 CR2 CS2	BDMG1I L BDMG1O L BDMG2I L BDMG2O L	I O I	DMA Grant Input and Output. Serial DMA priority line from computer, through devices and back to computer.
AP2	BBS7 L	I	Bank 7 Select. Asserted by bus master when address in upper 4K bank is placed on the bus.
AC1, AD1, BC1, BD1, BE1, BF1	BDAL 16 L -BDAL 21 L	O	Extended Address Bits 16-21

INTERRUPT

The interrupt vector address is factory set to address 210 (alternate 254). The vector address is programmed in a PROM on the controller, allowing user selection.

Interrupt requests are generated under the following conditions:

1. When the Controller Ready bit is set upon completion of a command.
2. When any drive sets an associated Attention Flag in the Attention Register and the Controller Ready bit is set.
3. When the controller or any drive indicates the presence of an error by setting the combined Error/Reset bit in the Control and Status Register.
4. When the Controller Ready bit is set by conventional initialization upon completion of a controller command or when an error condition is detected. For test purposes, a forced interrupt may be generated by the Controller Ready and Interrupt Enable bits.

DISC INTERFACE

The controller interfaces one or two disc drives through 60- and 26-pin cables. If two drives are used, the 60-pin control cable ("A" cable) is daisy chained to drive 0 and 1. The 26-pin cables ("B" cable) are connected separately from the controller to each drive. The maximum length of the 60-pin cable is 100 feet. The maximum length of the 26-pin cable is 50 feet. Table 1-2 lists the 60-pin interface signals, and Table 1-3 lists the 26-pin interface signals.

OPERATING SYSTEM COMPATIBILITY

RT-11: The emulation is transparent to the RT-11 version 4.0 operating system, using the standard device handler supplied by DEC.

RSX-11: The emulation is transparent to the RXS-11 version 4.0 operating system, using the standard device handler supplied by DEC.

RSTS: The emulation is transparent to the RSTS version 7.2 operating system, using the standard device handler supplied by DEC.

Table 1-2. Controller To Drive I/O Interface—"A" Cable

Signal Name (DILOG Term)	Pin Polarity (Active) –	Pin Polarity (Active) +	Source
DEVICE SELECT 0 (USEL0)	23	53	Controller
DEVICE SELECT 1 (USEL1)	24	54	Controller
DEVICE SELECT 2 (USEL2)	26	56	Controller
DEVICE SELECT 3 (USEL3)	27	57	Controller
SELECT ENABLE (USTAG)	22	52	Controller
SET CYLINDER TAG (TAG1)	1	31	Controller
SET HEAD TAG (TAG2)	2	32	Controller
CONTROL SELECT (TAG3)	3	33	Controller
BUS OUT 0 (BIT0)	4	34	Controller
BUS OUT 1 (BIT1)	5	35	Controller
BUS OUT 2 (BIT2)	6	36	Controller
BUS OUT 3 (BIT3)	7	37	Controller
BUS OUT 4 (BIT4)	8	38	Controller
BUS OUT 5 (BIT5)	9	39	Controller
BUS OUT 6 (BIT6)	10	40	Controller
BUS OUT 7 (BIT7)	11	41	Controller
BUS OUT 8 (BIT8)	12	42	Controller
BUS OUT 9 (BIT9)	13	43	Controller
BUS OUT 10 (BIT10)	30	60	Controller
DEVICE ENABLE (OCD)	14	44	Controller
INDEX (INDEX)	18	48	Drive
SECTOR MARK (SEC)	25	55	Drive
FAULT (FAULT)	15	45	Drive
SEEK ERROR (SERR)	16	46	Drive
ON CYLINDER (ONCYL)	17	47	Drive
UNIT READY (UNRDY)	19	49	Drive
WRITE PROTECTED (WPRT)	28	58	Drive
ADDRESS MARK (AMF)	20	50	Drive
BUS-DUAL-PORT ONLY	21	51	Drive
SEQUENCE IN (PICK)	29		Controller
HOLD (HOLD)	59		Controller

Table 1-3. Controller To Drive I/O Interface—"B" Cable

Signal (DILOG Term)	Pin Polarity (Active) –	Pin Polarity (Active) +	Ground	Source
Ground			1	
Servo Clock (SCLOCK)	2	14		Drive
Ground			15	
Read Data (RDATA)	3	16		Drive
Ground			4	
Read Clock (RCLOCK)	5	17		Drive
Ground			18	
Write Clock (WCLOCK)	6	19		Controller
Ground			7	
Write Data (WDATA)	8	20		Controller
Ground			21	
Unit Selected (USEL)	22	9		Drive
Seek End (SEEK)	10	23		Drive
Ground			11	
Reserved for Index	12	24		
Ground			25	
Reserved for Sector	13	26		

CONTROLLER SPECIFICATIONS*

Mechanical—The Model DQ215 is completely contained on one quad module 10.44 inches wide by 8.88 inches deep, and plugs into and requires one slot in any DEC LSI-11 based backplane.

Computer I/O

Register Addresses (PROM selectable)

—Control/Status Register 1 (RKCS1) 777 440
—Word Count Register (RKWC) 777 442
—Bus Address Register (RKBA) 777 444
—Disc Address Register (RKDA) 777-446
—Control/Status Register 2 (RKCS2) 777 450
—Drive Status Register (RKDS) 777 452
—Error Register (RKER) 777 454
—Attention Summary/Offset Register (RKAS/OF) 777 456
—Desired Cylinder Register (RKDC) 777 460
—Extended Memory Address Register (RKXMA) 777 462
—Data Buffer Register (RKDB) 777 464
—Maintenance Register 1 (RKMR1) 777 466
—ECC Position Register (RKECPS) 777 470
—ECC Pattern Register (RKECPT) 777 472
—Maintenance Register 2 (RKMR2) 777 474
—Maintenance Register 3 (RKMR3) 777 476
—Enable Real Time Clock Control (RKERTC) 777 546

Data Transfer

—Method: DMA
—Maximum block size transferred in a single operation is 64K words.

Bus Load

—1 std unit load

Address Ranges

—Disc drive: up to 220.32 megabytes
—Computer Memory: to 2 megawords

Interrupt Vector Address

—PROM selectable, factory set at 210 (alternate 254) priority level BR5

Disc Drive I/O

Connector—one 60-pin type "A" flat ribbon cable mounted on outer edge of controller module Two 26-pin type "B" ribbon cables (1 for each drive interfaced with).

Signal—SMD A/B flat cable compatible

Power—+5 volts at 3.5 amps, +12 volts at 300 milliamps from computer power supply.

Environment—Operating temperature 40°F. to 140°F., humidity 10 to 95% non-condensing.

Shipping Weight—5 pounds, includes documentation and cables.

*Specifications subject to change without notice.

SECTION 2
INSTALLATION

INSPECTION

The padded shipping carton that contains the controller board also contains an instruction manual and cables to the first disc drive if this option is exercised. The controller is completely contained on the quad-size printed circuit board. Disc drives, if supplied, are contained in a separate shipping carton. Inspect the controller and cables for damage.

CAUTION

If damage to any of the components is noted, do not install. Immediately inform the carrier and DILOG.

Installation instructions for the disc drive are contained in the disc drive manual. Before installing any components of the disc system, read Sections 1, 2 and 3 of this manual. Figure 2-1 illustrates the configuration of the controller. Tables 2-1 and 2-2 describe switch and jumper settings.

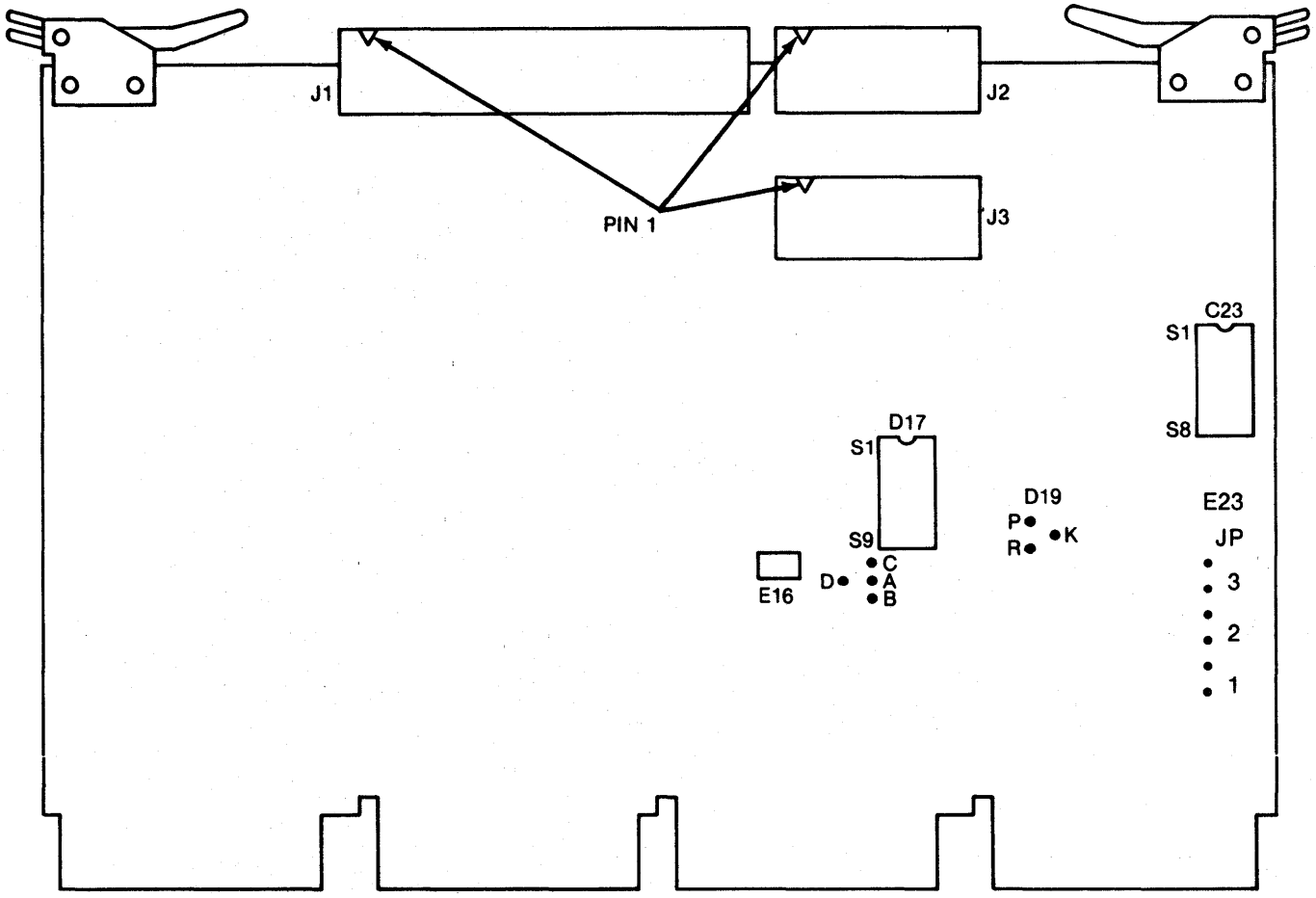


Figure 2-1. Controller Configuration

Table 2-1. Configuration Switches

LOCATION D17 SWITCHES

S1 (LSB) S2 S3 (MSB) — Binary Number of the first logical unit of the second physical drive.*

S4 — ON = Bootstrap enable; OFF = Bootstrap disable

S5 — ON = Controller error correction; OFF = CPU error correction

S6 (LSB) S7 S8 (MSB) — Binary number of last addressable logical unit.

S9 — ON = Enable Real Time Clock Control. When enabled, emulates the real time clock register, address 777 546; OFF = Disables Real Time Clock Control.

*For example, if there are four logical units (numbered 0-3) in the first drive, set the switches for the fifth logical unit (number 4) as follows:

(LSB) S1	S2	(MSB) S3
0	0	1

Note

If S1, S2, and S3 are off (000), the controller will default to all logical units on the first physical drive (drive 0). Because of the characteristics of some operating systems, the switches should be set for two drives even if only one drive is present.

LOCATION C23 SWITCHES

Switch	Position	Logical Unit and Emulation
S1	ON	LU0 = RK07
	OFF	LU0 = RK06
S2	ON	LU1 = RK07
	OFF	LU1 = RK06
S3	ON	LU2 = RK07
	OFF	LU2 = RK06
S4	ON	LU3 = RK07
	OFF	LU3 = RK06
S5	ON	LU4 = RK07
	OFF	LU4 = RK06
S6	ON	LU5 = RK07
	OFF	LU5 = RK06
S7	ON	LU6 = RK07
	OFF	LU6 = RK06
S8	ON	LU7 = RK07
	OFF	LU7 = RK06

Table 2-2. Jumper Installation

BOOTSTRAP ADDRESS JUMPERS E16	D . C	*A to B (standard) 773 000
	D . A	
	D . B	A to C (alternate) 775 000
INTERRUPT LEVEL	Jumper Installed	Level
	JP1, JP2, JP3	BR4
	JP2, JP3	BR5 (Factory Set)
	JP1, JP3	BR6
	JP1	BR7
DEVICE ADDRESS JUMPERS D19		R to K (standard) 777 440 Interrupt Vector = 210
		R to P (alternate) 776 700 Interrupt Vector = 254

*On an LSI-11/23 PLUS computer, bootstrap address 775 000 must be used.

PRE-INSTALLATION CHECKS

There are various LSI-11 configurations, many of which were installed before DEC made a hard disc available for LSI-11 based systems. Certain configurations require minor modifications before operating the disc system. These modifications are as follows:

A. If the system contains a REV11-C module, it must be placed closer to the processor module (higher priority) than the controller if the DMA refresh logic on the REV11-C is enabled.

B. If the 4K memory on the DK11-F is not used and the memory in the system does not require external refresh, the DMA refresh logic on the REV11-C should be disabled by removing jumper W2 on the REV11-C module.

C. If the system contains a REV11-A module, the refresh DMA logic must be disabled since the module must be placed at the end of the bus (REV11-A contains bus terminator).

D. If the REV11-C module is installed, cut the etch to pin 12 on circuit D30 (top of board) and add a jumper between pin 12 and pin 13 of D30.

E. If the system requires more than one backplane, place the REV-11 terminator in the last available location in the last backplane.

INSTALLATION

To install the controller module, proceed as follows:

CAUTION

Remove DC power from mounting assembly before inserting or removing the controller module.

Damage to the backplane assembly may occur if the controller module is plugged in backwards.

1. Select the backplane location into which the controller is to be inserted. Be sure that the disc controller is the lowest priority DMA device in the computer except if the DMA refresh/bootstrap ROM option module is installed in the system. The lowest priority device is the device farthest from the processor module. Note that the controller contains a bootstrap ROM.

There are several backplane assemblies available from DEC and other manufacturers. Figure 2-2 shows typical backplane configurations. Note that the processor module is always installed in the first location of the backplane or in the first location in the first backplane of multiple backplane systems.

It is important that all option slots between the processor and the disc controller be filled to ensure that the daisy-chained interrupt (BIAK) and DMA (BDMG) signal be complete to the controller slots. If there must be empty slots between the controller and any option board, the following backplane jumpers must be installed:

FROM	TO	SIGNAL
C0 x NS	C0 x M2	BIAK1/L0
C0 x S2	C0 x R2	BDMG1/L0
↑ Last Full Option Slot	↑ Controller Slot	

2. Insert the controller into the selected backplane position. Be sure the controller is installed with the components facing row one, the processor.

   The controller module is equipped with handles on the side opposite the slot connectors. Gently position the module slot connectors into the backplane then press until the module connectors are firmly seated into the backplane. Both handles must be pressed simultaneously. When removing the module, apply equal pulling pressure to both handles.

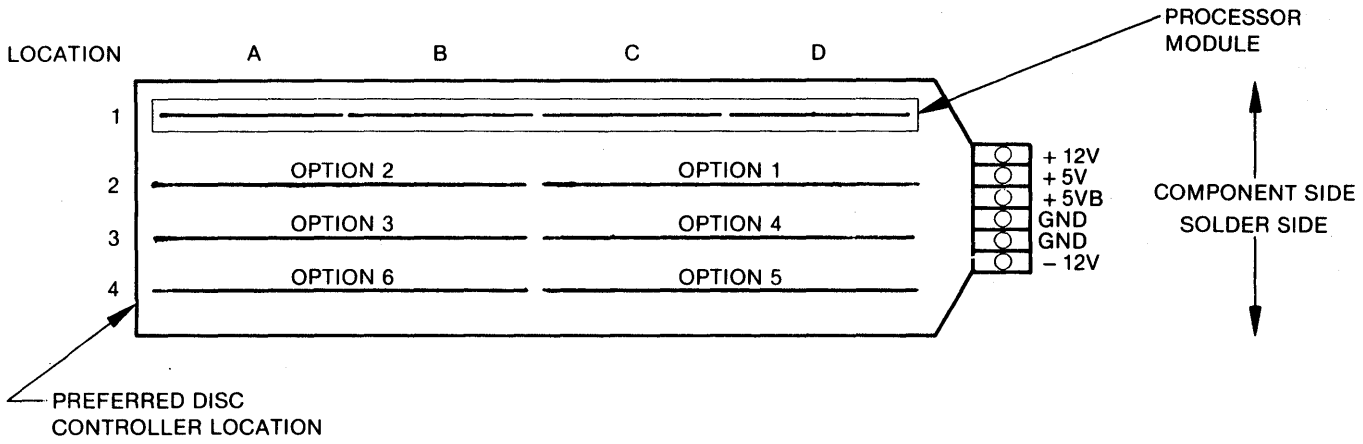
3. Feed the module connector end of the disc I/O cables into the controller module connectors. Ensure pin 1 is matched with the triangle on the connector as shown in Figure 2-1. Install the cable connectors into the module connectors. Verify that the connectors are firmly seated.

4. Connect the disc-end of the I/O cables to the disc I/O connectors. Be sure that the bus terminator is installed at the last disc in the system.

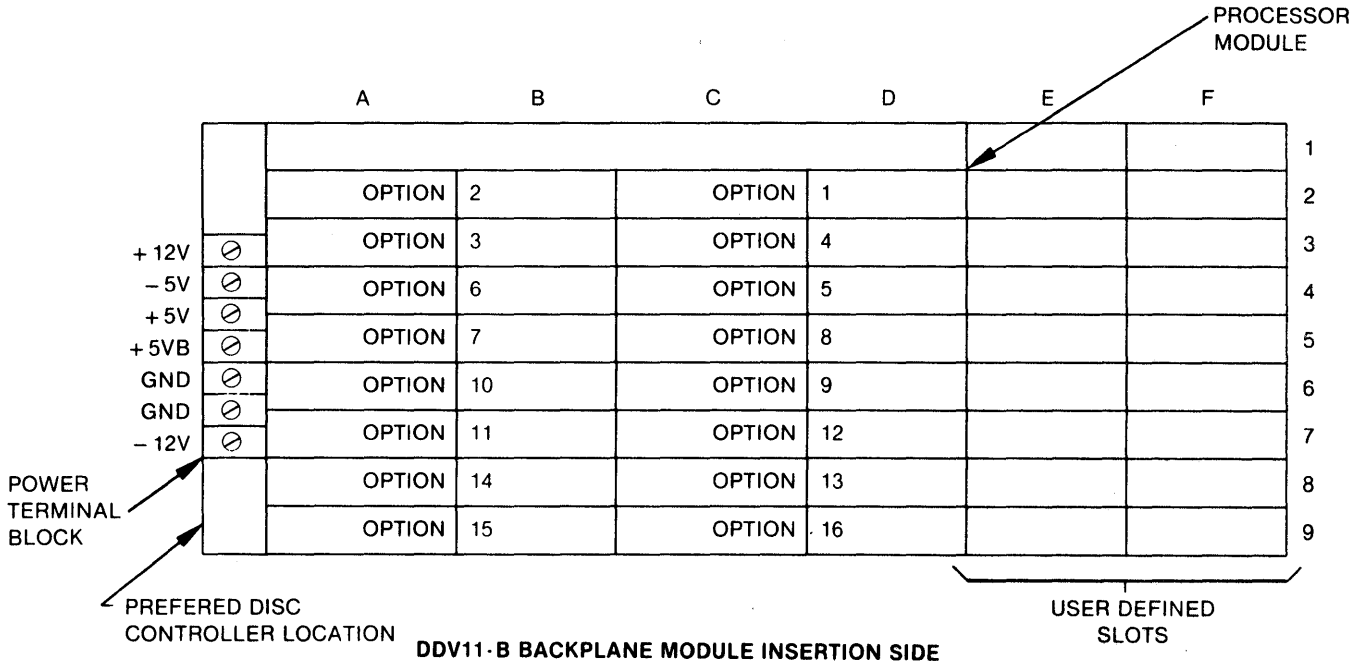
5. Refer to the disc manual for operating instructions and apply power to the disc and computer.

6. Observe that the green DIAGnostic LED on the controller board is lit.

7. The system is now ready to operate. Refer to Section 3 for operating instructions, diagnostics, and formatting.



H9270 MODULE INSERTION SIDE



DDV11-B BACKPLANE MODULE INSERTION SIDE

NOTE

MEMORY CAN BE INSTALLED IN ANY SLOT; IT IS NOT PRIORITY DEPENDENT AND DOES NOT NEED TO BE ADJACENT TO THE PROCESSOR.
CONTROLLERS ARE ALSO COMPATIBLE WITH H9273A MODULES.

Figure 2-2. Typical Backplane Configuration

GROUNDING

To prevent grounding problems, DILOG recommends standard ground braid be installed from the computer DC ground point to the disc drive DC ground point and also between disc drives at the DC ground points.

SECTION 3
OPERATION

INTRODUCTION

This section contains procedures for operating the computer system with the controller and a disc drive or drives. An understanding of DEC operating procedures is assumed. The material here is provided for "first time users" of disc subsystems and describes procedures for bootstrapping, formatting, and diagnostic testing.

The programs supplied with each controller are on floppy disc or magnetic tape media, depending on what is specified on the sales order. If the user is not able to run floppy disc or magnetic tape media, an EPROM program may be used for some subsystems to format the disc. Instructions and constraints for the EPROM program are described at the end of this section.

PRECAUTIONS AND PREOPERATIONAL CHECKS

The following precautions should be observed while operating the system. Failure to observe these precautions could damage the controller, the disc cartridge, the computer, or could erase a portion or all of the stored software.

1. If the controller bootstrap is to be used, set controller switch S4 on, and disable other bootstraps that reside at that address.
2. See Figure 2-1 for proper positions of the switches and jumpers. See Tables 2-1 and 2-2 for switch and jumper settings.
3. Do not remove or replace the controller board with power applied to the computer.
4. If system does not operate properly, check operating procedures and verify that the items in Section 2 have been performed.

Before operation the following checks should be made:

1. Verify that the controller board is firmly seated in backplane connector.
2. Verify that the cables between the controller and the disc drive are installed.
3. Be sure the disc drive cartridge is installed (if it is to be used).
4. Apply power to the computer and the console device.
5. Verify that green DIAG light on front edge of the controller board lights.
6. Be sure power is applied to disc drive and READY light is on.

BOOTSTRAP PROCEDURE

The following assumes the system is in ODT mode. Note that the bootstrap can be used under processor Power Up Mode 2 conditions. Refer to the appropriate DEC manual for a discussion of the Power Up Modes. Further note that the disc drive does not need to be READY to enter the bootstrap.

Reset the system by pressing RESET or enter the following (characters underlined are output by the system; characters not underlined are input by the operator):

@ 773000G or 775000G
Depends on jumper configuration above.

* Enter one of the following: DM0, DP0, DL0, DR0, MS0, MT0, DY0 or FT <CR>.

Definitions are as follows:

DM = RK06/07 Disc
DP = RP02/03 Disc
DL = RL01/02 Disc
DR = RM02/03 Disc
MS = TS11 Tape
MT = Tape
DY = RX02 Floppy Disc
FT = EPROM Formatter.

Booting can be executed from logical units other than "0" shown above by entering the desired logical unit number, i.e., 1, 2, 3, . . . or 7.

FORMAT AND DIAGNOSTIC TEST PROGRAM

Description

DILOG's Universal Firmware and Diagnostic Program permits the user to format a disc pack for his particular application; compensate for media errors; and test the controller and drive. When formatted, the disc may be partitioned horizontally or vertically. Either way the pack is divided into logical units which the computer recognizes. The user may select one of three types of partitioning: 1-head, 2-head or vertical.

The constraints for selecting each are:

Subsystem:

- Maximum number of logical units is 8.

1-head:

- Maximum number of heads (surfaces) is 8.
- Maximum size of logical units is 270,336 records.

2-head:

- Maximum number of heads (surfaces) is 16.
- Number of fixed and removable heads (surfaces) must be even.
- Maximum size of logical units is 270,336 records.

Vertical:

- Maximum size of logical units is 270,336 records.

Drive types CMD or DFR are formatted for a 1-head partition. SMD or MMD types are usually formatted vertically.

The disc pack is divided vertically by cylinders and horizontally by heads (or data surfaces). Each head (surface) is further divided into tracks. A track is addressed by cylinder number and head number. Tracks are further divided into sectors (or records or blocks) which the computer recognizes as increments within a logical unit. Sectors consist of overhead bytes (such as address, sync, error correction) and data bytes. The standard number of data bytes, bytes usable by the computer, is 512 data bytes per sector. Figure 3-1 illustrates vertical and head partitioning.

Table 3-1 is a partial list of disc drives and specifications for partitioning. Column 1 lists the manufacturer. Column 2 lists the model number. Column 3 lists the number of sectors (also called records and blocks) per track. Column 4 lists the number of heads (also called data surfaces) per drive. Column 5 lists the number of cylinders per drive. Columns 6

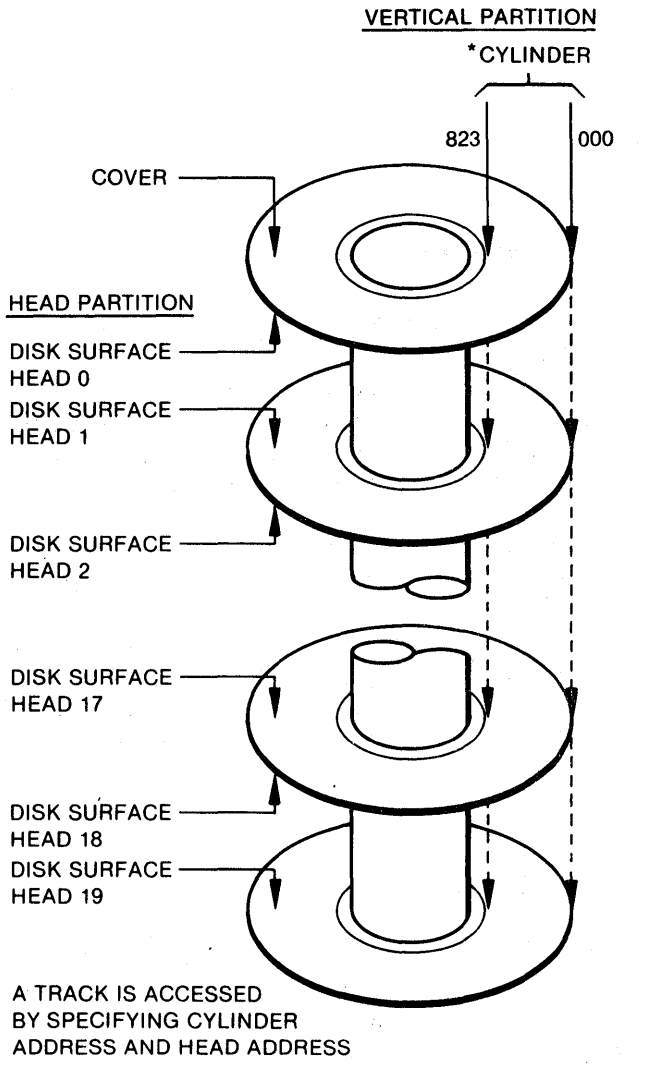


Figure 3-1. Partitions

and 7 list the emulations, the number of megabytes per logical unit, and the number of sectors per logical unit. Column 8 lists the megabyte capacity and number of sectors of the last logical unit partitioned. For CMD drives (Note c), the value listed is for all logical units as well as the last.

To use the table, consider Ampex Capricorn 165 as an example. The drive is efficiently partitioned into five RK07 units with capacity and number of sectors shown at the top of Column 6. The remaining capacity is assigned as one RK06 unit with the capacity and sectors shown at the top of Column 7; however, the RK06 unit is the remainder after partitioning five RK07 units, and as such, this remainder is not a complete RK06 unit. Instead of 13.88 Mbytes with 27,126 sectors, the partial RK06 unit is assigned the remaining 8.78 Mbytes and 17,150 sectors. Notes a and b in Column 8 state

Table 3-1. Values for Partitioning with Universal Firmware (DQ215)

(1) Manufacturer	(2) Model Number	(3) Sectors (Records) (Blocks)/ Track	(4) Heads (Data Surfaces)/ Drive		(5) Cylinders/ Drive*	(6) Total Logical Units RK07 Units 27.54MB 53,790	(7) Total Logical Units RK06 Units 13.88MB 27,126	(8)** Last Logical Unit	
			Removable	Fixed				MB	Sectors
AMPEX	Capricorn 165	35	0	10	823	5	1	8.78[a]	17,150
AMPEX	Scorpio 48	35	0	3	823	1	1 4	16.45[b] 2.25[a]	32,130 4,410
AMPEX	Scorpio 80	35	0	5	823	2	1 6	18.18[b] 3.49[a]	35,525 6,825
AMPEX	DFR-932	34	1	1	823		2	14.25[c]	27,846
AMPEX	DFR-964	34	1	3	823		4	14.25[c]	27,846
AMPEX	DFR-996	34	1	5	823		6	14.25[c]	27,846
AMPEX	DM980	34	5	0	823	2	1 6	16.10[b] 1.65[a]	31,450 3,230
BALL	BD50	23	5	0	815	1	1 4	20.19[b] 6.06[a]	39,445 11,845
BALL	BD80	34	5	0	815	2	1 6	15.40[b] .95[a]	30,090 1,870
BASF	6172	23	0	3	600		2	7.13[a]	13,938
CENTURY DATA SYS.	M80	35	0	6	650	2	1 6	14.86[b] 0.12[a]	29,028 246
CENTURY DATA SYS.	M160	35	0	6	837	5	1	3.04[a]	5,940
CENTURY DATA SYS.	Trident T-82RM	34	5	0	823	2	1 6	16.10[b] 1.65[a]	31,450 3,230
CONTROL DATA CORP.	CMD 9448-32	34	1	1	823		2	14.25[c]	27,846
CONTROL DATA CORP.	CMD 9448-64	34	1	3	823		4	14.25[c]	27,846
CONTROL DATA CORP.	CMD 9448-96	34	1	5	923		6	14.25[c]	27,846
CONTROL DATA CORP.	MMD 9730-24	35	0	2(2) = 4	320		2	8.74[a]	17,080
CONTROL DATA CORP.	MMD 9730-80	35	0	5	823	2	1 6	18.18[b] 3.49[a]	35,525 6,825
CONTROL DATA CORP.	MMD 9730-160	35	0	2(5) = 10	823	5	1	8.78[a]	17,150
CONTROL DATA CORP.	SMD 9762	34	5	0	823	2	1 6	16.10[b] 1.65[a]	31,450 3,230
CONTROL DATA CORP.	SMD 9764	34	19	0	411	4	1	23.48[b]	45,866
FUJITSU	M-2283	35	0	4	823	2	1 5	3.51[a] 3.08[a]	6,860 6,020
FUJITSU	M-2284	35	0	2(5) = 10	815	5	1	7.34[a]	14,350
FUJITSU	2311	35	0	4	589	1	1 4	14.33[b] 0.21[a]	28,000 420
FUJITSU	2312	35	0	7	589	2	1 6	18.18[b] 3.76[a]	35,525 7,350
KENNEDY	5303	35	0	3	700	1	1 3	9.83[a] 9.56[a]	19,215 18,690
KENNEDY	5305	35	0	5	700	2	1 5	7.16[a] 6.45[a]	14,000 12,600

*For a 1-head partition, the value of cylinders/drive = tracks/surface.

**Calculated using 4 alternates.

[a]Less than standard RK06

[b]Greater than standard RK06

[c]CMD

Table 3-1. Values for Partitioning with Universal Firmware (DQ215) (Continued)

(1) Manufacturer	(2) Model Number	(3) Sectors (Records) (Blocks)/ Track	(4) Heads (Data Surfaces)/ Drive		(5) Cylinders/ Drive*	(6) Total Logical Units RK07 Units 27.54MB 53,790	(7) RK06 Units 13.88MB 27,126	(8)** Last Logical Unit	
			Removable	Fixed				MB	Sectors
KENNEDY	5380	35	0	5	823	2	1 6	18.18[b] 3.49[a]	35,525 6,825
MITSUBISHI	2860-2	23	0	7	548	1	1 4	17.22[b] 3.05[a]	33,649 5,957
NEC	D1220	35	0	4	530	1	1 3	10.10[a] 9.89[a]	19,740 19,320
NEC	D1240	35	0	2(4) = 8	530	2	1 6	20.07[b] 5.87[a]	39,200 11,480
NIPPON PERIPHERALS	NP30-40	35	0	5	370	1	1 3	5.19[a] 4.03[a]	10,150 9,450
NIPPON PERIPHERALS	NP30-80	35	0	11	370	2	1 6	16.95[b] 2.16[a]	33,110 4,235
NIPPON PERIPHERALS	NP30-120	35	0	11	555	3	1 8	25.82[b] 10.64[a]	50,435 20,790
PRIAM	DISKOS 3350	35	0	3	561	1	1 3	2.36[a] 2.09[a]	4,620 4,095
PRIAM	6650	35	0	3	1121	2	1 5	4.89[a] 4.35[a]	9,555 8,505
PRIAM	15450	35	0	7	1121	5	1	2.38[a]	4,655
TECSTOR	Sapphire 160	35	0	12	700	5	1	10.96[a]	21,420
TECSTOR	Sapphire 165	35	0	10	823	5	1	8.78[a]	17,150

*For a 1-head partition, the value of cylinders/drive = tracks/surface.

**Calculated using 4 alternates.

[a]Less than standard RK06

[b]Greater than standard RK06

[c]CMD

whether the last unit is an expanded or a partial unit.

The values in the table are calculated for the most efficient use of the drive; that is, total formatting capacity of the drive with a standard number of spare cylinders. The user may require another type of partitioning for a particular application, in which case the program will prompt and calculate for that application.

Parameters for disc drives not listed in Table 3-1 may be determined from manufacturer's specifications and the following: Determine the number of bytes per track from the manufacturer's specification. The number of bytes per sector (data and overhead) for DILOG controllers is 576. Divide the number of bytes per track by the number of bytes per sector. Drop the remainder. This value is the number of sectors per track. Then, number of sectors per track × number of heads × number of cylinders per drive = number of sectors per drive.

The user may require alternate cylinders, or spares, to compensate for media flaws, soft errors, or marginal drive conditions. The values in the table provide for four alternate cylinders. All three types of partitioning in the program make provisions for sparing. The program accounts for alternates when calculating the number and size of logical units.

If the number of logical units is to be changed, the configuration switches, shown in Figure 2-1, should also be changed after completion of format and test.

The descriptions below indicate what parameters will be changed as various elements are changed; for example, if the number of logical units is changed, the size of the logical units will change.

1-Head Partition

A 1-head partition is used for CMD drives. The column numbers below refer to Table 3-1. Parameters are developed as follows:

1. Determine the number of sectors per track (Column 3), heads per drive (Column 4), and tracks per surface (Column 5). For a 1-head partition, the number of tracks per surface is the same as cylinders per drive in the table.

2. Determine the number of alternate tracks (cylinders) per drive. The standard number of alternates is four.
3. Subtract the number of alternates from the tracks per surface.
4. The number of heads corresponds to the number of logical units.
5. Then, sectors per track × heads per drive × (tracks per surface minus alternates) = sectors per drive.
6. Sectors per drive × 512 = byte capacity.

For example, an AMPEX DFR-932 has 34 sectors per track, 2 heads per drive and 823 tracks/surface. If 4 alternates are required, then:

$$34 \times 2 \times (823 - 4) = 55{,}692 \text{ sectors/drive}$$

Because there are two heads, there are two logical units.

$$\frac{55{,}692}{2} = 27{,}846 \text{ sectors/logical unit}$$

and

$$27{,}846 \times 512 = 14.25 \text{ megabytes/logical unit}$$

2-Head Partition

The parameters for 2-head partitioning are the same as for 1-head except the number of sectors/ logical unit is multiplied by 2:

1. Determine the number of sectors per track (Column 3), heads per drive (Column 4), and tracks per surface (Cylinders per Drive, Column 5).
2. Determine the number of alternate tracks (cylinders) per drive. The standard number of alternates is four.
3. Subtract the number of alternates from the tracks per surface.
4. Then, sectors per track × heads per drive × (tracks per surface minus alternates) = sectors per drive.
5. Sectors per drive × 512 = byte capacity.

For example, a CDC 9730-24 has 35 sectors per track, 4 heads per drive and 320 tracks per surface. If 4 alternates are required, then:

$$35 \times 4 \times (320\text{-}4) = 44{,}240 \text{ sectors/drive}$$

Because there are four heads, and two heads comprise one logical unit, there are two logical units.

$$\frac{44{,}240}{2} = 22{,}120 \text{ sectors/logical unit}$$

and

$$22{,}120 \times 512 = 11.32 \text{ megabytes/logical unit}$$

Vertical Partition

With vertical partitioning, the user may select the number of logical units or the size of the logical unit. If the number of logical units is selected, the logical units will be of equal size. If the size of the logical units is selected, all logical units may not be of equal size. For example there may be 2 equal RK07 logical units of 53,790 sectors/logical unit and a partial RK06 logical unit of 31,450 sectors/logical unit.

Parameters for vertical partitioning are determined as follows:

The user specifies the number of logical units (all logical units are of equal size):

1. Determine the required number of alternate cylinders per drive. Subtract the number of alternates from the number of cylinders per drive (Column 5). This value is the usable cylinders per drive.
2. Determine the number of logical units per drive required. Then,
3. Number of usable cylinders per drive divided by number of logial units required = Number of cylinders per logical unit. The remainder is assigned as alternate.
4. Number of cylinders per logical unit × sectors per track × number of heads = Number of sectors per logical unit.
5. Number of sectors per logical unit × 512 = Megabyte capacity per logical unit.

For example, if the user has a Century Data drive, Model T-82RM and 4 alternates (standard) and 3 logical units are required, then

$$823 - 4 = 819 \text{ usable cylinders}$$

and

$$\frac{819}{3} = 273$$

If there was a remainder, the number of alternates would be more than initially selected.

Then,

$273 \times 34 \times 5 = 46{,}410$ sectors per logical unit

and

$46{,}410 \times 512 = 23.76$ Mbytes per logical unit

The user specifies the size of logical units in sectors per logical unit (the last logical unit will be a different size).

1. Determine the required number of alternate cylinders per drive. Subtract the number of alternates from the number of cylinders per drive (Column 5). This value is the usable cylinders per drive.
2. Determine the required number of sectors (blocks) per logical unit. Then,
3. Sectors per track (Column 3) × number of heads (Column 4) divided into sectors per logical unit = cylinders per logical unit. If there is a remainder, the number of cylinders per logical unit is rounded off to the next higher number.
4. Number of usable cylinders divided by cylinders per logical unit = number of logical units. If there is a remainder, the number of logical units is rounded off to the next higher number.
5. Number of cylinders per logical unit × number of full (equal size) logical units = Number of cylinders full (equal size) logical units.
6. Number of usable cylinders per drive minus number of cylinders in full logical units = Number of cylinders in partial logical unit.

For example, if the user has a Century Data drive, Model T-82RM, and 4 alternates and 53,790 sectors per logical unit (standard RK07) are required, then

$823 - 4 = 819$ usable cylinders

and

$$\frac{53{,}790}{34 \times 5} = 316.41$$

which becomes

317 cylinders per logical unit

then,

$$\frac{819}{317} = 2.58 \text{ logical units per drive}$$

or 2 RK07 units and 1 partial RK06 unit.

For the partial logical unit,

$317 \times 2 = 634$

$819 - 634 = 185$ cylinders per partial logical unit

Sectors per the partial unit are calculated as follows:

$185 \times 34 \times 5 = 31{,}450$ sectors per partial logical unit.

Partitioning Program

The name of the program is DMXXD, where XX is the revision number of the program.

Figure 3-2 is a flow diagram of the program. The statements in quotes are program prompts. The pentagonoid symbols with a letter and number, such as "A1," are reference points for breaks in the flow. The "A" designation refers to the first page (Format) and the "B" designations refer to the second page (Change Parameters). The following descriptions refer to the first (Format) page of the diagrams.

When the program is initialized the following display will appear on the terminal:

DILOG'S UNIVERSAL FIRMWARE AND DIAGNOSTIC PROGRAM VERIFIES PROPER FUNCTIONING OF THE DILOG RK06/RK07 EMULATING DISC CONTROLLER AND FORMATS THE DISC TO YOUR SPECIFICATIONS.

YOUR DEFAULT PARAMETERS ARE:

SECTORS ___
HEADS ___
CYLINDERS ___

ALTERNATES ___
SIZE OF LOGICAL UNIT (RECORDS) ___

The parameters displayed are calculated for the efficiency of most applications. The units of measure are as follows: sectors/track; heads/drive; cylinders/drive; alternates/drive; and the size of logical unit in sectors/logical unit.

The next display will be:

```
****************************************
******RESTART ADDRESS IS 2000******
********^X RESTARTS PROGRAM********
******^C RESTARTS CURRENT TEST******
****************************************
```

To restart, press the CTRL and X keys at the same time, or CTRL and C.

The next query is:

ARE YOU RUNNING THE DIAGNOSTIC VIA A CRT (Y OR N)?

If the answer is no, the CRT will not display the current cylinder address during the test program.

The next prompt is:

ENTER NUMBER OF DRIVES

Enter 1 or 2. If 1 is entered, the next queries will refer only to Drive 0. If 2 drives are selected, the program will prompt for Drive 0 and Drive 1.

The next displays will be:

ENTER DM DEVICE ADDRESS <777 440> ?
ENTER DM INTERRUPT VECTOR
<000210> ?

The address is factory set unless the user requested an alternate address (see Section 2).

The next question will be:

LSI (Y OR N)?

If the controller model is DQ215, answer Y. If the model is DU215, answer N.

The menu of drives will appear next, with the following:

***** DRIVE 0 *****

ENTER NUMBER CORRESPONDING TO DISC DRIVE
OR
SELECT ANOTHER PAGE
N = NEXT PAGE P = PREVIOUS PAGE E = ENTER PARAMETERS

From the menu, the appropriate drive may be selected. If E is pressed, the program will prompt for drives not listed in the menu or will prompt to change parameters in case of conflicts in constraints.

Note

The program responds with the minimum number of inquiries; for example, if a drive is selected from the menu, the program will not prompt for the number of sectors, heads and cylinders, because these responses are predetermined.

If a drive is selected from the menu, the next display will be:

DO YOU WISH TO CHANGE FORMAT PARAMETERS (DRIVE 0)?

Note

The format parameters are those last entered. Each time there is a change, the program will retain that change.

If the response is No, the next display will show the configuration. An example is as follows:

DISC SUBSYSTEM CONFIGURATION

LOGICAL UNIT	PHYSICAL DRIVE	MEGABYTES	RECORD SIZE
DM0	0	27.59	53900
DM1	0	27.59	53900
DM2	0	27.59	53900
DM3	0	25.82	50435

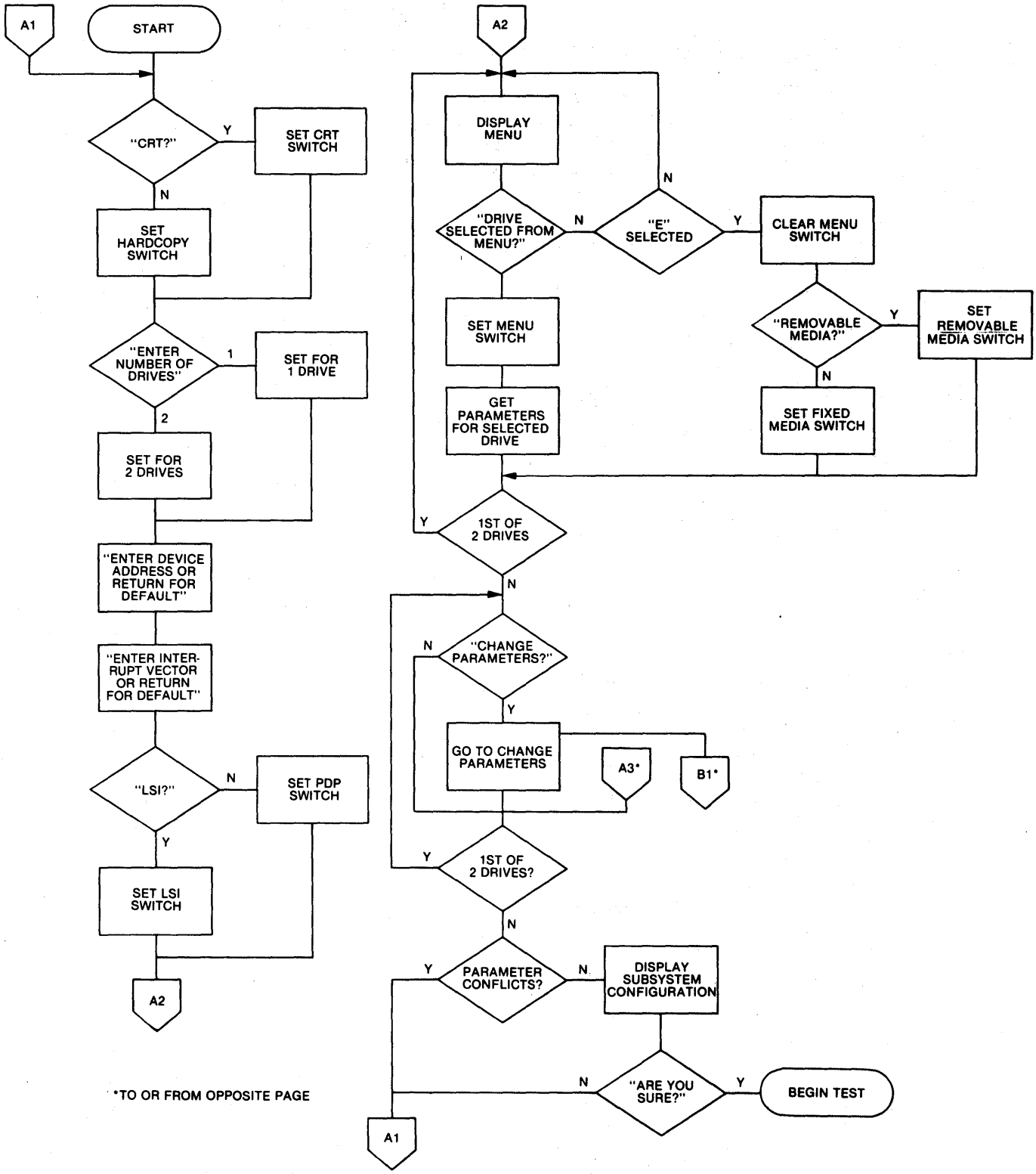


Figure 3-2(A). Universal Formatting

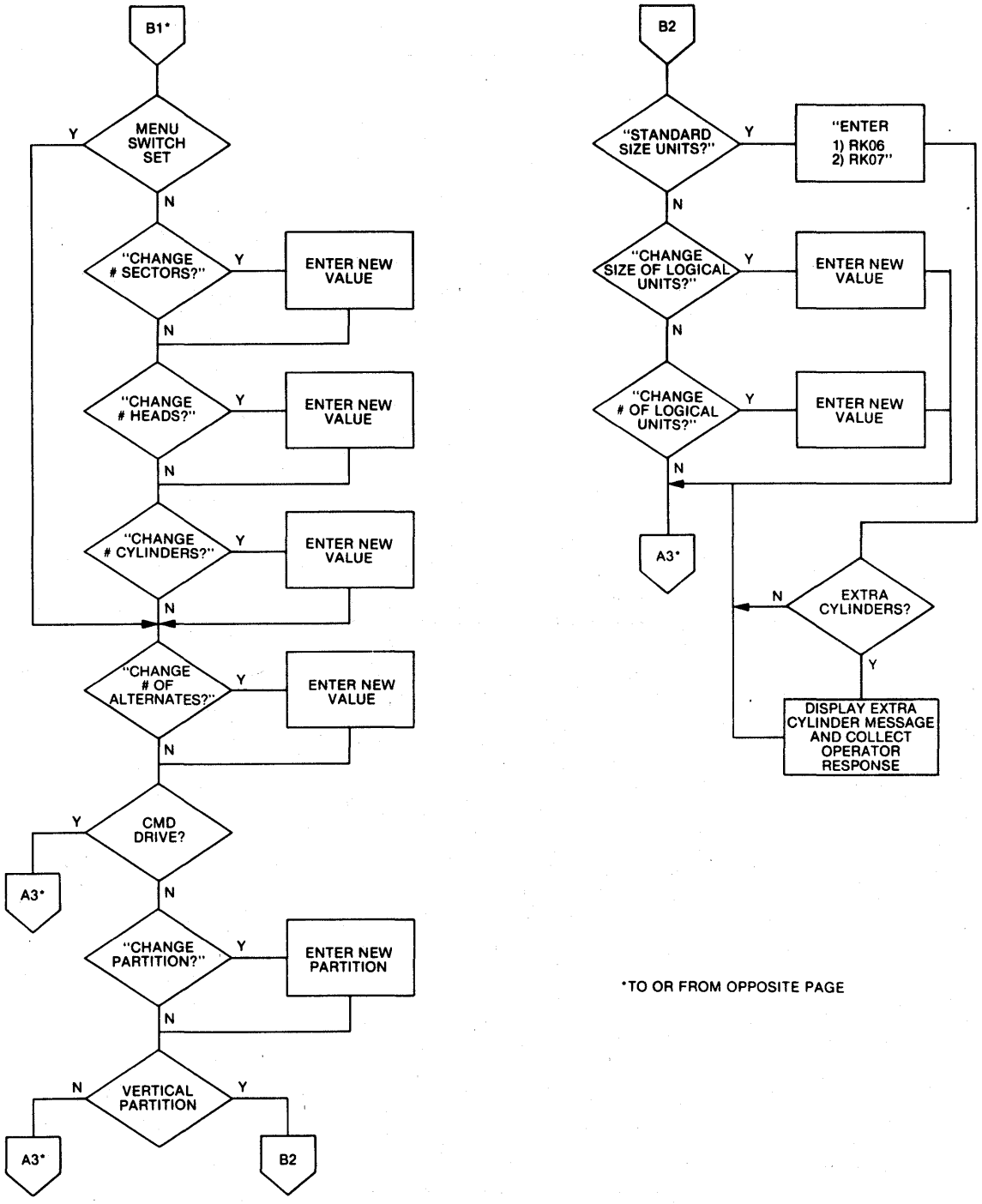


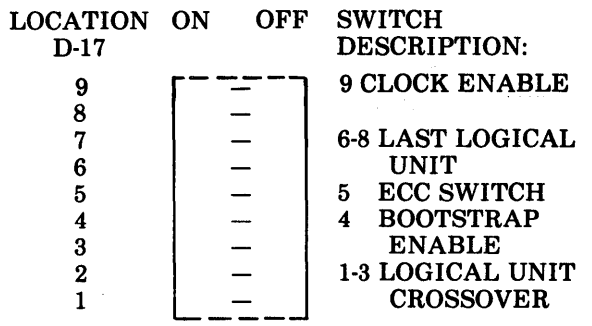
Figure 3-2(B). Universal Formatting—Change Parameters

DM4	1	27.59	53900
DM5	1	27.59	53900
DM6	1	27.59	53900
DM7	1	25.82	50435

PHYSICAL DRIVE 0 HAS 44 ALTERNATE TRACKS
PHYSICAL DRIVE 1 HAS 44 ALTERNATE TRACKS

ARE YOU SURE?

If the answer is Yes, the next display will show how the switches should be set:



DEFINITIONS:

L/U CROSSOVER: 1ST LOGICAL UNIT ON 2ND DRIVE
BOOTSTRAP ENABLE: ON = ENABLED, OFF = DISABLED
ECC SWITCH: ON = CONTROLLER MODE, OFF = SOFTWARE MODE
LAST L/U: LAST LOGICAL UNIT ON SUBSYSTEM

SET SWITCHES 1-3 TO A BINARY WEIGHTED VALUE OF X.
SET SWITCHES 6-8 TO A BINARY WEIGHTED VALUE OF X.

USE (C) TO CONTINUE

If the switches are set incorrectly, the message will repeat. Switch settings are described in Section 2. If the switches are set correctly, the program will skip to the test section.

The following descriptions refer to the second (Change Parameters) page of the diagram.

If the answer is Yes to the prompt:

DO YOU WISH TO CHANGE FORMAT PARAMETERS (DRIVE 0)?

the next prompt will be:

CHANGE NUMBER OF SECTORS (Y OR N)?
CHANGE NUMBER OF HEADS (Y OR N)?
CHANGE NUMBER OF CYLINDERS (Y OR N)?

These prompts are for adding a drive that is not on the menu. The values (after HOW MANY?) to be entered are in the drive manufacturer's manual. The next prompt of change parameters is for drives which are or are not on the menu:

CHANGE NUMBER OF ALTERNATES (Y OR N) <4> ?

The standard number of alternates selected is 4. If a CMD drive is selected, there will be no further questions. If Yes, HOW MANY? will appear. The next query is:

CHANGE TYPE OF PARTITION (Y OR N) <VERTICAL> ?

If the answer is Yes, the program will prompt with 1-HEAD, 2-HEAD, OR VERTICAL? If 1-head or 2-head is selected there will be no further queries. Next to appear is:

STANDARD SIZE UNITS (Y OR N)?

If Yes, the program will prompt with selection of RK07 or RK06. If RK07 is selected, the program will divide the record size into RK07 units, and the remaining records will be an RK06 unit. Standard sizes are shown in Table 3-1. After selection of standard units, the next message will be:

AFTER CALCULATING STANDARD SIZE UNITS ON DRIVE 0, YOU HAVE _____ CYLINDERS NOT YET ALLOCATED (_____ MEGABYTES).

IF YOU WOULD LIKE, I COULD CREATE ANOTHER UNIT, WHICH WILL BE SMALLER THAN YOUR STANDARD SIZE UNITS, OR I COULD ALLOCATE THE CYLINDERS AS ALTERNATES.

PLEASE ENTER THE NUMBER OF CYLINDERS YOU WOULD LIKE ME TO ALLOCATE AS ALTERNATES, ANY REMAINDER WILL BE ALLOCATED AS ANOTHER UNIT.

If the standard number of alternates previously selected is adequate (default is 4), enter 0.

The next display will be:

CHANGE SIZE OF LOGICAL UNIT (RECORDS) (Y OR N) <XXXXX> ?
CHANGE NUMBER OF LOGICAL UNITS (Y OR N) <X> ?

If Yes is answered to any of the last three questions, there will be no further questions. The above sequence will repeat for the second drive:

DO YOU WISH TO CHANGE FORMAT PARAMETERS (DRIVE 1)?

If the constraints are not violated, the Disc Subsystem Configuration and ARE YOU SURE? will appear. If the response is Yes, the program will begin the test sequence. If the subsystem constraints are violated, a message similar to the following will appear:

FORMAT PARAMETER CONFLICTS
SUBSYSTEM

DRIVE 0 IS CONFIGURED FOR 8 LOGICAL UNITS
DRIVE 1 IS CONFIGURED FOR 3 LOGICAL UNITS
MAXIMUM NUMBER OF LOGICAL UNITS ALLOWED IS 8

To resolve this conflict, the number of logical units may be changed on Drive 0. To provide logical units of equal size on both drives, the number of logical units may be changed to 4 on each drive. Restart the current address with ^C, repeat the sequence above up to the question CHANGE NUMBER OF LOGICAL UNITS?, and answer Y. When HOW MANY? appears, answer 4. Repeat this sequence for Drive 1.

Examples of errors on a single drive when changing the type of partition are as follows:

FORMAT PARAMETER CONFLICTS
DRIVE 0

MAXIMUM NUMBER OF HEADS WITH 1-HEAD PARTITION IS 8

or

FORMAT PARAMETER CONFLICTS
DRIVE 1

MAXIMUM NUMBER OF HEADS WITH 2-HEAD PARTITION IS 16

or

FORMAT PARAMETER CONFLICTS
DRIVE 0

MAXIMUM NUMBER OF HEADS MUST BE AN EVEN NUMBER WITH 2-HEAD PARTITION

Examples of errors on a single drive when changing the size of the logical units is as follows:

FORMAT PARAMETER CONFLICTS
DRIVE 0

LOGICAL UNIT SIZE IS 270, 720
MAXIMUM LOGICAL UNIT SIZE IS 270, 336

or

FORMAT PARAMETER CONFLICTS
DRIVE 0

LOGICAL UNIT SIZE IS BIGGER THAN THE DISC

The algorithm for mapping, that is, what the controller should map, is as follows:

$$\frac{\text{Record Number}}{\text{Sector/Cylinder}} = \text{Correct Cylinder Address} + \text{Remainder (1)}$$

$$\frac{\text{Remainder (1)}}{\text{Sector/Track}} = \text{Correct Head Address} + \text{Remainder (2)}$$

Remainder (2) = Sector Address

A mapping error is displayed during the Random Read test as follows:

*****MAPPING ERROR*****

RECORD NUMBER = XXX
SECTOR/CYLINDER = XXX
SECTOR/TRACK = XXX
DRIVE NUMBER = XXX

CORRECT ADDRESS
CYLINDER = XXX
HEAD = XXX
SECTOR = XXX

CONTROLLER ADDRESS
CYLINDER = XXX
HEAD = XXX
SECTOR = XXX

Diagnostic Test Program

The format/test program contains the following:

1. TEST CONTROLLER
   A. Registers
   B. Data Buffer
   C. DMA
   D. ECC
2. TEST DISC DRIVE
   A. Disc Ready
   B. Disc Restore (seek to cylinder 0)
3. FORMAT
   A. Write Headers
   B. Read Headers
   C. Write Data Test Pattern
   D. Read Data Test Pattern
4. SEQUENTIAL READ
5. SELECTED READ
6. RANDOM SEEK, READ
7. RANDOM SEEK, WRITE, READ, AND COMPARE
8. ASSIGN ALTERNATE TRACK

Test Controller

The program will automatically test the controller registers and data buffer. The program will only display error messages during this test; the display will be:

DATA BUFFER ERROR

or the mnemonics of the controller registers and the location and contents (in Octal). The display of the registers is followed by a 4-line message to aid in isolating the specific problem.

Note

Whenever an error occurs and the registers are displayed, an audio alarm signal is generated to notify the operator.

The 4-line message is as follows:

DISC ADDRESS _____
HEAD _____ CYLINDER _____
TYPE OF COMMAND _____
CONTROL STATUS ERROR _____
DRIVE STATUS _____

"DISC" lists the sector, head and cylinder (in decimal) where the error occurred. An example of Type of Command is Read Data Command. An example of Control Status is Seek Error.

The ECC logic test is as follows: The program selects whether a correctable or noncorrectable error is to be programmed; then the program creates an error; writes the data with an error to the controller; reads to memory; then the program decides whether the error is noncorrectable or correctable.

If noncorrectable, the program checks to ensure an error has been returned by the controller.

If correctable, the program checks to make sure there has been no error returned by the controller, and checks to ensure the error was corrected in the proper manner. If this test fails, the message is one or more of the following:

CONTROLLER INDICATES CORRECTABLE ERROR
CONTROLLER INDICATES NONCORRECTABLE ERROR
ERROR BURST IS CORRECTABLE
ERROR BURST IS NONCORRECTABLE
ERROR BURST WAS NOT CORRECTED

The space character (SP) is used to exit from this test.

The program will next display:

USE C TO CONTINUE
USE O TO TRANSFER TO ODT
USE L TO REBOOT YOUR SYSTEM

"C" is used to continue the test. "O" is used for ODT (on-line debugging technique). "L" is used to initiate the system bootstrap.

Test Disc Drive

After the controller test is performed, the program will automatically test the drive for ready and restore. The disc address is not displayed during this test. If the disc will not restore, the program will display the register for cylinder 0.

Format

The operator may either select logical units sequentially or select one or more specific logical units to be formatted. Program messages are presented for formatting in logical unit number sequence:

FORMAT ENTIRE SUBSYSTEM (Y OR N)?
FORMAT ENTIRE DRIVE 0 (Y OR N)?
FORMAT ENTIRE DRIVE 1 (Y OR N)?
FORMAT ALTERNATE CYLINDERS DRIVE 0 (Y OR N)?
FORMAT ALTERNATE CYLINDERS DRIVE 1 (Y OR N)?
FORMAT DL0 (Y OR N)?
FORMAT DL1 (Y OR N)?
FORMAT DL2 (Y OR N)?
FORMAT DL3 (Y OR N)?

Note

Before any write operation, the program will display ARE YOU SURE? This aids the operator in preventing reformatting of a previously formatted logical unit (possibly destroying good data).

During formatting, the following messages will appear sequentially:

WRITING HEADERS
CURRENT CYLINDER ADDRESS -----

READING HEADERS
CURRENT CYLINDER ADDRESS -----

WRITING DATA TEST PATTERN -----
CURRENT CYLINDER ADDRESS -----

READING DATA TEST PATTERN -----
CURRENT CYLINDER ADDRESS -----

When reading and writing headers, the program will display the cylinder addresses sequentially. The test pattern tests are also sequentially selected, and the cylinder address displayed will correspond to the current address being read.

After each logical unit is formatted, the display will be:

DM____ FORMAT AND VERIFICATION COMPLETE

Sequential Read

For this test, the display will be:

SEQUENTIAL READ (ALL CYLINDERS AND HEADS)?

If the response is No, the program will jump to the Selected Read test. If the response is Yes, the current cylinder address is displayed as each cylinder is read. If an error is detected, the register contents and location are displayed with the 4-line identification message, and the following:

ASSIGN ALTERNATE TRACK FOR DEFECTIVE TRACK?

If no alternates (spares) are available, the following will be displayed:

NO ALTERNATE CYLINDER AVAILABLE

When marking or assigning alternate tracks, the following error messages may occur:

TRACK HAS ALREADY BEEN MARKED DEFECTIVE
TRACK HAS ALREADY BEEN MARKED ALTERNATE

Selected Read

For this test, the display will be:

READ DM0? (Y OR N)?

If the response is No, the next logical unit will be displayed. If the response is Yes, the current cylinder address is displayed and each cylinder is read. If an error is detected, the register contents and location are displayed with the 4-line identification message. The ASSIGN ALTERNATE TRACK message appears, and error messages if the track has been marked DEFECTIVE or ALTERNATE.

Random Seek, Read

For this test, the display will be:

RANDOM SEEK, READ OF DRIVE (ALL CYLINDERS AND HEADS)?

This test selects a random cylinder, logical unit, and a sector address within the cylinder. The test then reads data and tests for errors. All logical units are used in this test. Alternate cylinders cannot be assigned during this test. The terminal keyboard space (SP) character is used to exit this test.

If an error is detected, the register content and locations are displayed with the 4-line identification message.

This check also ensures controller mapping is correct. The desired address and the actual address will be displayed with the drive's physical characteristics.

Random Seek, Write Data, Read Data, Compare Test

If the response is No, each logical unit will appear in sequence until the response is Yes:

DM0? DM2?
DM1? DM3?

This test selects a random cylinder address and random sector address and writes five sectors (2560 bytes) of random data. The data written is then read into CPU memory and compared for read errors. This test allows logical units to be tested. The terminal keyboard space character (SP) is used to exit from this test.

This test ensures that the controller is executing the write check command correctly and that the controller is zero-filling the disc correctly.

Assign Alternate Track

This test may be used if the disc drive manufacturer provides a map describing defective tracks.

The message is:

ASSIGN ALTERNATE TRACK FOR DEFECTIVE TRACK (Y OR N)?

If the response is No, the program will revert to:

USE R TO REPEAT

USE O TO TRANSFER TO ODT
USE L TO REBOOT YOUR SYSTEM

If the response is Yes, the display will be:

PHYSICAL DRIVE (0 or 1)?
(only if two drives are present)

CYLINDER ADDRESS (0 TO _____)

Enter the cylinder address, in decimal, of the defective track. If the cylinder address entered is incorrect, the message will be repeated.

The next message will be:

HEAD ADDRESS (0 TO _____)

Enter the head address, in decimal, of the defective track. If the head address entered is incorrect, the message will be repeated.

The next message will be:

MAP OUT
CYLINDER ----- HEAD --
ARE YOU SURE (Y OR N)?

If No, the program will repeat the first message of this test. If Yes, an alternate cylinder is assigned and the message is:

ALTERNATE CYLINDER ASSIGNED

Other messages to appear may be:

TRACK ALREADY MARKED DEFECTIVE
or
TRACK ALREADY MARKED ALTERNATE

The program will then repeat the first message of this test.

EPROM FORMAT PROGRAM

This program is a simple, fast method to format a disc. This program is not a substitute for DILOG's Universal Firmware and Diagnostic Program which is a complete and extensive program for formatting the disc and testing the controller. The EPROM program does not permit changing the number or size of logical units, ECC test, or alternate track assignments. The EPROM does not support horizontal partitioning; for example, the Format program (FT) will not support a CMD-type drive.

Note

Check the switch settings and jumper locations listed previously before using the EPROM Program.

Use the boot procedure and enter FT with <CR>. The program will display:

NUMBER OF SECTORS >
NUMBER OF HEADS >
NUMBER OF CYLINDERS >
REMOVABLE MEDIA (Y OR N)?

Consult the disc drive manufacturer's specifications and enter the numbers in decimal. After the list questions and <CR>, the following menu will appear:

1 = INTERRUPT TEST
2 = RESTORE
3 = SECTOR TEST
4 = DMA
5 = WRITE HEADERS
6 = READ HEADERS
7 = WRITE DATA
8 = READ DATA (1)
<CR> = ALL THE ABOVE
9 = READ DATA (2)
B = BOOTS
SELECT >

The above tests are selected by the numbers, or B or <CR>. The SECTOR TEST compares the sector pulses with Number of Sectors above. The READ DATA (1) test checks the mapping algorithm of the controller. READ DATA (2) tests only read data. READ DATA (1) verifies the test pattern, and READ DATA (2) does not. If <CR> is pressed, the first test to appear on the terminal will be WRITING HEADERS as the first four tests are completed very quickly.

To restore the program or for an unconditional escape to boot, enter Control C.

If an error occurs, all registers are listed on the terminal with entries such as ?? SECTOR DISCREPANCY ?? or DRIVE FAULT or DRIVE NOT READY. The following is an error printout example:

RKSC1 = 177 440 (XXXXXX)
RKWC = 177 442 (XXXXXX)
RKBA = 177 444 (XXXXXX)
RKDA = 177 446 (XXXXXX)
RKCS2 = 177 450 (XXXXXX)
RKDS = 177 452 (XXXXXX)
RKER = 177 454 (XXXXXX)
RKAS/0F = 177 456 (XXXXXX)
RKDC = 177 460 (XXXXXX)
RKXMA = 177 462 (XXXXXX)
RKDB = 177 464 (XXXXXX)
RKMR1 = 177 466 (XXXXXX)
RKECPS = 177 470 (XXXXXX)
RKECPT = 177 472 (XXXXXX)
RKMR2 = 177 474 (XXXXXX)
RKMR3 = 177 476 (XXXXXX)
Non-Existent Drive
Drive Fault
Drive Not Ready
Selected Unit Seek Error
Use (P) to Continue

SECTION 4
PROGRAMMING

PROGRAMMING DEFINITIONS

Function—The expected activity of the disc system (write, seek, read, etc.)

Command—To initiate a function (halt, clear, go, etc.)

Instruction—One or more orders executed in a prescribed sequence that causes a function to be performed.

Address—The binary code placed in the BDAL0-15 lines by the bus master to select a register in a slave device. Note memory other than computer internal memory, i.e., peripheral device registers, the upper 4K (28-32K) address space is used.

Register—An associated group of memory elements that react to a single address and store information (status, control, data) for use by other assemblies of the total computer system. Classically, registers have been made up of groups of flip-flops. More and more often registers are the contents of addressed locations in solid-state or core memory.

DISC CONTROLLER FUNCTIONS

The disc controller performs 14 functions. A function is initiated by a GO command after the processor has issued a series of instructions that store function-control information into controller registers. To accept a command and perform a function, the controller must be properly addressed and the disc drive(s) must be powered up, be at operational speed, and be ready.

The functions performed by the controller are established by bits 01, 02, 03 and 04 of the control status register (RKCS1). The function and bit codings are given in Table 4-1. Descriptions of the functions are given in the following paragraphs.

Note that the controller automatically performs certain functions during each command. For example, the controller always performs the following steps:

1. Decodes instruction
2. Selects drive
3. Acknowledges pack (tests for RK06/RK07 drive type)

Table 4-1. Function Codes

Bit 4321	Command
0000	SELECT DRIVE
0001	PACK ACKNOWLEDGE
0010	DRIVE CLEAR (RESET ATTENTION STATUS)
0011	UNLOAD (NO OP)
0100	START SPINDLE (NO OP)
0101	RECALIBRATE (RESTORE DRIVE AND RESET FAULT)
0110	OFFSET
0111	SEEK
1000	READ DATA
1001	WRITE DATA
1010	READ HEADERS (1 TRACK OF HEADERS)
1011	WRITE HEADERS (FORMAT TRACK)
1100	WRITE CHECK

4. Executes one of the remaining nine functions

Select Drive

Performed automatically as part of all functions related to drive selection (connects drive).

Pack Acknowledge

Performed automatically to verify emulation (RK06/RK07) as part of all functions related to drive selection. Controls bit 08 in RKDS.

Drive Clear

Resets attention status in RKAS/0F.

Recalibrate

Relocates the heads to cylinder zero and clears the cylinder address register. Also resets all fault conditions. Sets attention bit in RKAS/0F.

Offset

Sets drive attention bit in RKAS/0F.

Seek

Performed automatically as part of all functions related to drive selection. Sets attention bit in

RKAS/0F. During Overlapped Seeks, loads cylinder address into RKMR3 (Maintenance Register 3).

Read Data

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. Headers are read and compared with the desired disc address until the correct sector is found. Transfer of data through the data buffer to memory is initiated. When the sector data transfer is complete, the ECC logic is checked to ensure that the data read from the disc was error-free. If a data error occurred, the ECC correction logic is initiated to determine whether the error is correctable; when finished, the command is terminated to allow software or hardware (as selected) to apply the correction information. Assuming no data errors, the word count in RKWC is checked; if non-zero, the data transfer operation is repeated into the next sector. The word count is checked at the end of each sector until it reaches zero, at which time the command is terminated by setting the Ready bit.

Write Data

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. Transfer of data from memory to the data buffer is begun, and headers are read and compared with the desired disc address until the correct sector is found. Preamble, Data (256 words), and ECC bits (56) are written on the disc. If the word count in RKWC goes to zero during the sector, the rest of the sector is zero-filled. After the sector transfer, the word count is RKWC is checked and, if non-zero, the data transfer operation is continued into the next sector. The word count in RKWC is checked at the end of each sector and, when it equals zero, the command is terminated by setting the Ready bit.

Read Headers

A Seek to the cylinder in RKDC is performed. This function causes the controller to read all headers starting at the Index mark. Each 5-word header is read in the order in which it appears on the disc. If an ECC error is detected in the header, the HRE bit of RKER is set.

Write Headers

A Seek to the cylinder in RKDC is performed. The controller then waits until Index is detected. When detected, zeros are written until Index is again detected. This "cleans" the track of potential spurious signals. After Index is detected a second time, 5 header words and a 32-bit ECC are written after each sector pulse. When Index is next detected, the command is terminated and the Ready bit is set.

Note

All five words and the ECC code are prepared by the format routine (software) and treated as data by the controller. Only one complete track can be formatted at a time.

Write Check

Causes the following sequence to be executed: A Seek to the cylinder in RKDC is performed. The selected drive provides data as in a Read command, and data is obtained from memory as in a Write command. The data are compared on a word-for-word basis until the word count reaches zero or until a failure to compare occurs. If the data fails to compare, the command is terminated immediately.

Mapping and Map Override

In a typical DEC disc subsystem, the method by which the disc drive finds the proper location to read data from or write data to is as follows:

1. The application software program running under the operating system sends a record number to the disc device driver software.
2. The device driver converts this record number into head, sector and cylinder numbers.
3. The driver then sends this information to dedicated hardware registers on the disc controller.
4. The controller in turn passes these parameters on to the disc drive over I/O interface cables.
5. The drive interprets these signals and activates electronics and electromechanics enabling it to seek to the exact physical location where information will be recorded or retrieved.

In a DEC subsystem which includes a DILOG controller, the above procedure is the same up to step 4. But instead of passing on the head, sector and cylinder information to the drive, the DILOG controller first takes that information sent by the device driver software and reconverts it to the original record number. Then by invoking a special algorithm, the controller develops a new head, sector and cylinder number. This is called mapping

and it is a necessary procedure whenever the disc drive that is attached to the CPU does not contain the same specifications as the drive supplied by the CPU manufacturer.

Map Override is nothing more than a special operating mode of the DILOG disc controller which allows it to transfer the disc address to the drive as described in steps 1-5, bypassing the DILOG mapping procedure. Typically, this feature is only used in an environment in which the user requires the entire disc drive to be formatted as one large logical unit. In other words, one logical unit would equal one physical unit. For example, consider a subsystem consisting of a DQ215 and a Fujitsu Eagle 474 Mbyte drive. Obviously, the controller is not a good match for a drive that large, considering that one RK07 logical unit equals 27.6 Mbytes. If, however, the user had a definite requirement for running an RK07 instruction set, he could invoke Map Override and format the Eagle as one very large RK07. One requirement is that the device driver software has to be modified.

ENABLE REAL TIME CLOCK CONTROL

The real time clock line is from the 60-cycle power supply in the LSI. The Operating System uses the clock for time and date. The line on the Q Bus, BEVNT, can be disabled by a switch on the controller, which when ON enables real time clock control or when OFF disables control. The register, address 777 546, is shown at the end of this section.

REGISTERS

A summary of the registers is shown in Figure 4-1, followed by a description of each register.

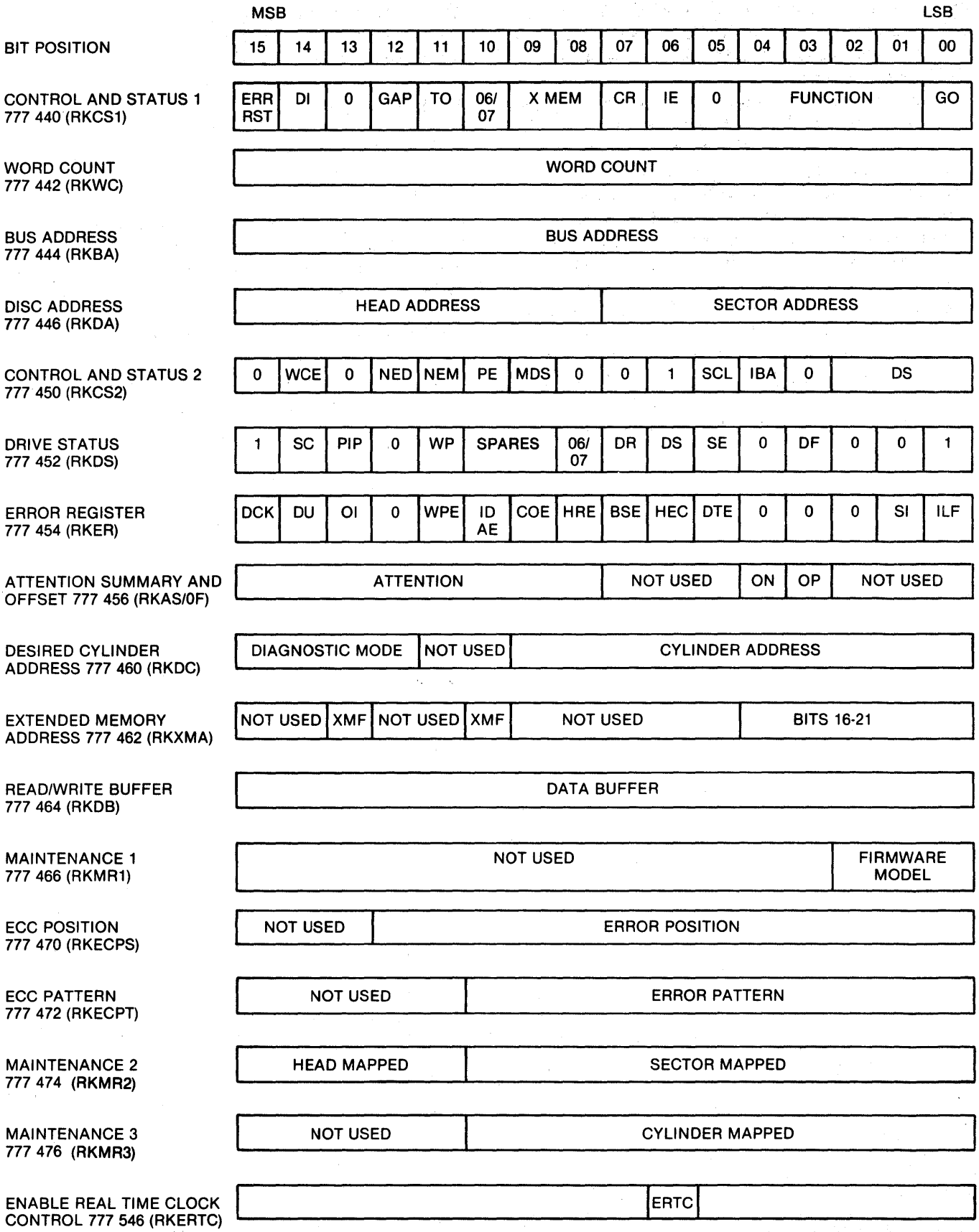
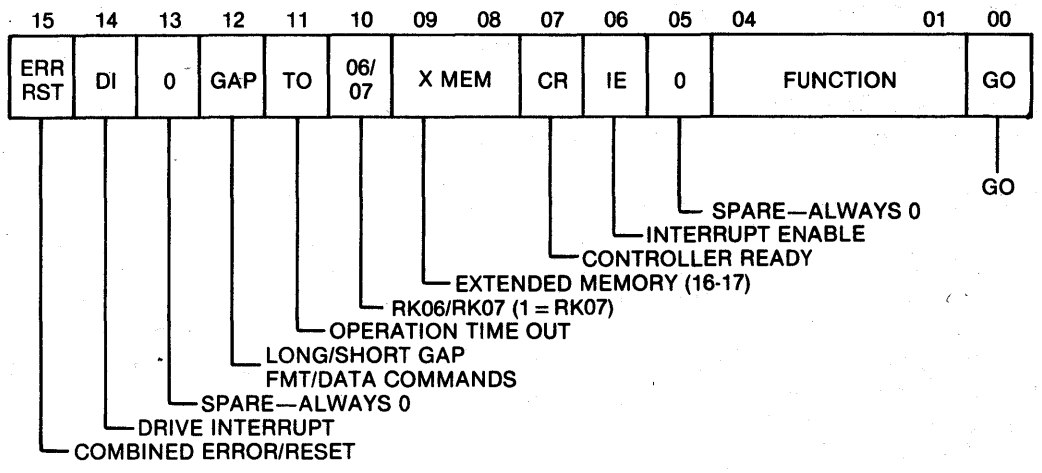


Figure 4-1. Controller Register Configuration

CONTROL AND STATUS REGISTER 1
777 440 (RKCS1)



BIT(S) DEFINITION

00 GO—When set this bit causes programmed commands (function codes) to be executed. When set, only two other bits can be set (except in the diagnostic mode); they are: Bit 15, CCLR, in RKCS1 and Bit 05, SCLR, in RKCS2.

01-04 FUNCTION CODE—

BIT 4321	0(GO)	OCTAL	COMMAND
0000	1	01	SELECT DRIVE
0001	1	03	PACK ACKNOWLEDGE
0010	1	05	DRIVE CLEAR (RESET DRIVE FAULT)
0011	1	07	UNLOAD (NO OPERATION)
0100	1	11	START SPINDLE
0101	1	13	RECALIBRATE (RESTORE DRIVE AND RESET FAULT)
0110	1	15	OFFSET
0111	1	17	SEEK (NO OPERATION)
1000	1	21	READ DATA
1001	1	23	WRITE DATA
1010	1	25	READ HEADERS (1 TRACK OF HEADERS)
1011	1	27	WRITE HEADERS (FORMAT TRACK)
1100	1	31	WRITE CHECK

05 SPARE—ALWAYS 0

06 INTERRUPT ENABLE—When this bit is set, the controller is allowed to interrupt the processor under any of the following conditions:

- When the Controller Ready bit (bit 07 in RKCS1) is set upon completion of a command.
- When any drive sets an associated Attention flag (ATN7-ATN0) in RKAS/0F, and the Controller Ready bit is set.
- When the controller or any drive indicates the presence of an error by setting the ERR/RST bit in RKCS1.

In addition, via program control, an interrupt can be forced by the simultaneous setting of the IE and RDY bits in RKCS1. The IE bit can be reset via program control as well as by conventional initialization (INIT, CCLR, SCLR).

07 CONTROLLER READY—This is a read-only bit. It is set via conventional initialization (INIT, CCLR, SCLR) upon completion of a controller command, or when an error condition is detected. The RDY bit is reset when the GO bit (bit 00 in RKCS1) is set.

08-09 EXTENDED BUS ADDRESS—These bits constitute an extension of the 16-bit Bus Address register (RKBA), which contains the memory address for the current data transfer.

10 RK06/RK07 SELECT—When set this bit selects RK07. When reset, RK06 is selected.

11 OPERATION TIME OUT—When set, this read-only bit indicates that the GO bit has been set for a specified time period and the current command has not been executed within that time period.

*12 GAP CONTROL—In the Write Header command (or write format) bit 12 will direct the controller to generate a long gap (24 bytes) or a short gap (16 bytes) between sector and header.

Bit 12 1 = Short Gap
0 = Long Gap

In the Write Data or Read Data command bit 12 will direct the controller to Write or Read a sector data field (512 bytes) with or without ECC (7 bytes) to or from memory.

Bit 12 1 = 512 Bytes + 7 Bytes
DATA ECC

0 = 512 Bytes

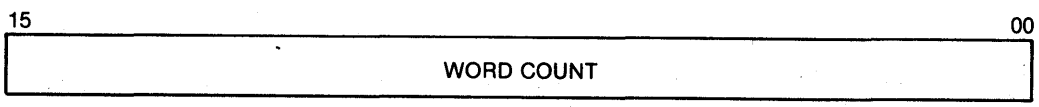
13 SPARE—ALWAYS 0

14 DRIVE INTERRUPT ENABLE (SEEK OR RESTORE)—This bit is set during a Seek or Restore operation or when any attention bit is set in the RKAS/OF register. The bit is reset by Bus Initialize (INIT), Subsystem Clear (SCLR) or by Drive Clear commands asserting attention.

15 COMBINED ERROR/RESET—When reading bit 15 via programmed control, a zero indicates an operation complete with good status; a one indicates an operation complete with an error.

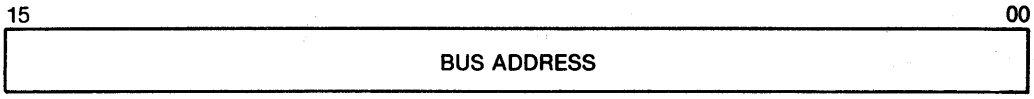
*NOTE: When bit 12 is set, the Word Count Register should be set for 520 bytes.

WORD COUNT REGISTER
777 442 (RKWC)



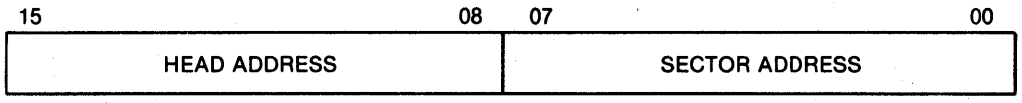
This is a Read/Write register. The bits of this register contain the 2's complement of the total number of words to be transferred during a Read, Write, or Write Check operation. The register is incremented by one after each transfer. When the register overflows (all WC bits go to zero), the transfer is complete and controller action is terminated at end of the present disc sector. Only the number of words specified in the RKWC are transferred. Cleared by INIT or RESET functions.

BUS ADDRESS REGISTER
777 444 (RKBA)



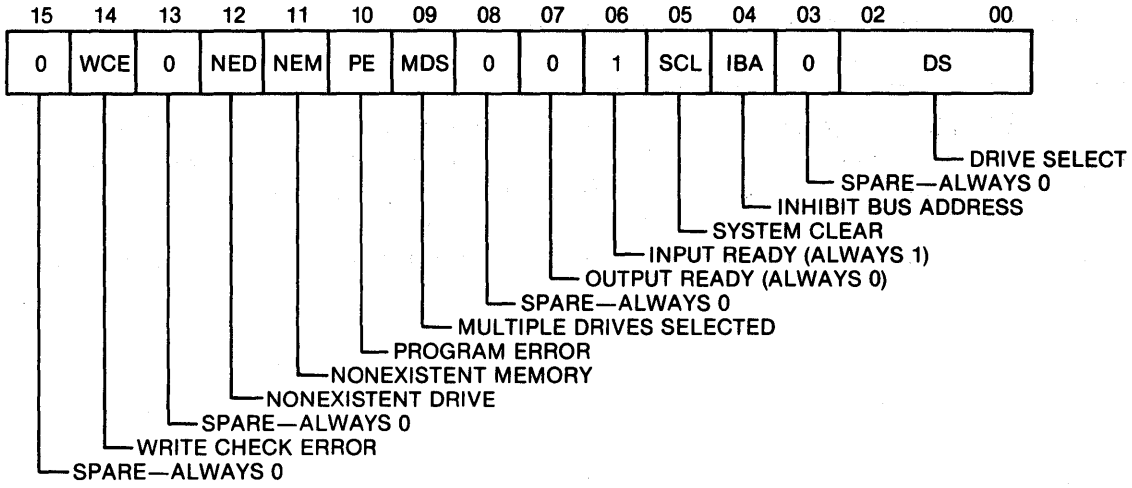
The Bus Address Register is initially loaded with the low-order sixteen bits of the bus address that reflects the main memory start location for a data transfer. With the low-order bit (bit 00) always forced to zero, the Bus Address Register bits are combined with bits 09 and 08 of the RKSC1 register (BA17, BA16) to form a complete even-numbered, 18-bit memory address. Following each data transfer bus cycle, the Bus Address Register is incremented to select the next even-numbered location.

DISC ADDRESS (TRACK AND SECTOR) REGISTER
777 446 (RKDA)



BIT(S)	DEFINITION
00-04 (00-07)	SECTOR ADDRESS—In the emulation mode, bits 00-04 select up to 20 sectors of 16-bit words. In the map override mode, bits 15, 14, 13, 12, in the Desired Cylinder Register 777 460, are set to 1000, respectively. The Sector Address then uses bits 00-07.
08-10 (08-15)	HEAD (TRACK) ADDRESS—In the emulator mode, bits 08-10 select heads 0, 1, 2. In the map override mode, bits 15, 14, 13, 12 and in the Desired Cylinder Address Register 777 460, are set to 1, 0, 0 and 0, respectively. The Head (TRACK) Address then uses bits 08-15.

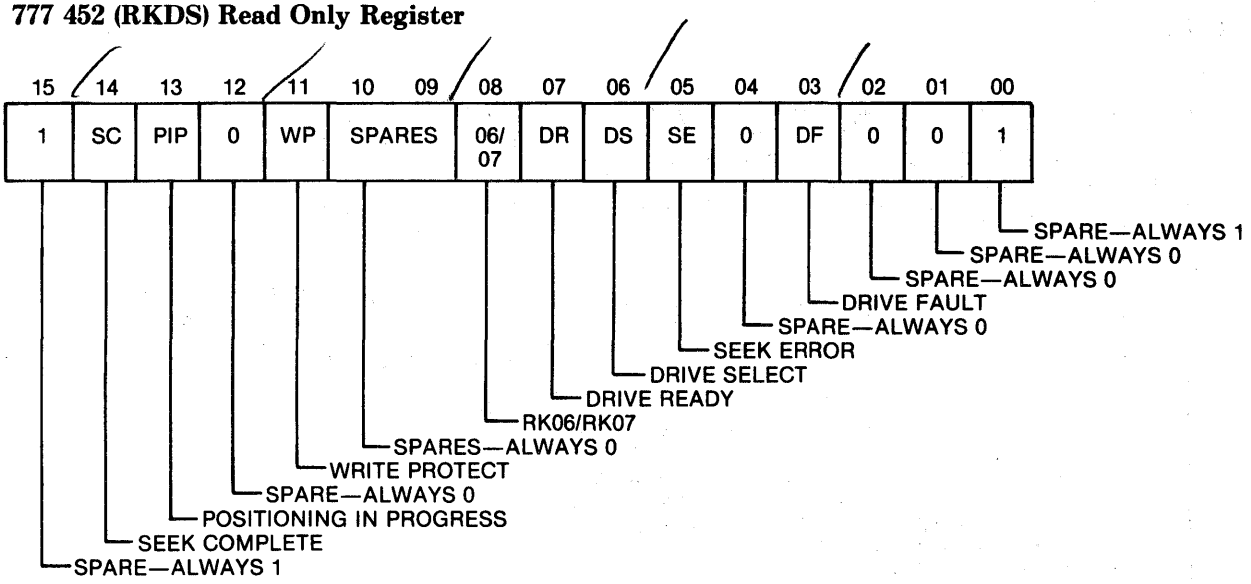
CONTROL AND STATUS REGISTER 2
777 450 (RKCS2)



BIT(S)	DEFINITION
00-02	DRIVE SELECT—These bits specify the drive to be selected.
03	SPARE—ALWAYS 0
04	INHIBIT BUS ADDRESS INCREMENT—When this bit is set, the Bus Address register is prevented from incrementing during data transfers.
05	SYSTEM CLEAR—When this bit is set the controller and drive are reset.
06	INPUT READY—ALWAYS 1
07	OUTPUT READY—ALWAYS 0
08	SPARE—ALWAYS 0
*09	MULTIPLE DRIVES SELECTED—This bit is set when more than one drive has been selected at the same time. This bit can only be cleared by INIT or SCLR.
*10	PROGRAM ERROR—This read-only error bit is set if any controller register is written (CCLR and SCLR excluded) while the GO bit in RKCS1 is set.
*11	NONEXISTENT MEMORY—This read-only error bit is set when the controller attempts to execute a bus cycle and SSYN is not returned within the specified time period.
*12	NONEXISTENT DRIVE—When set, this read-only error bit indicates that Select Acknowledge (SACK) has not been asserted by the selected drive in response to a Select Enable sent to the drive.
*13	SPARE—ALWAYS 0
*14	WRITE CHECK ERROR—When set, this read-only bit indicates that a data word read from the disc (during a Write Check command) did not compare with the data word in main memory. If a Write Check error is detected and the IBA bit (bit 04 of RKCS2) is cleared, the Bus Address register will contain the memory address of the mis-matched word plus two or plus four.
15	SPARE—ALWAYS 0

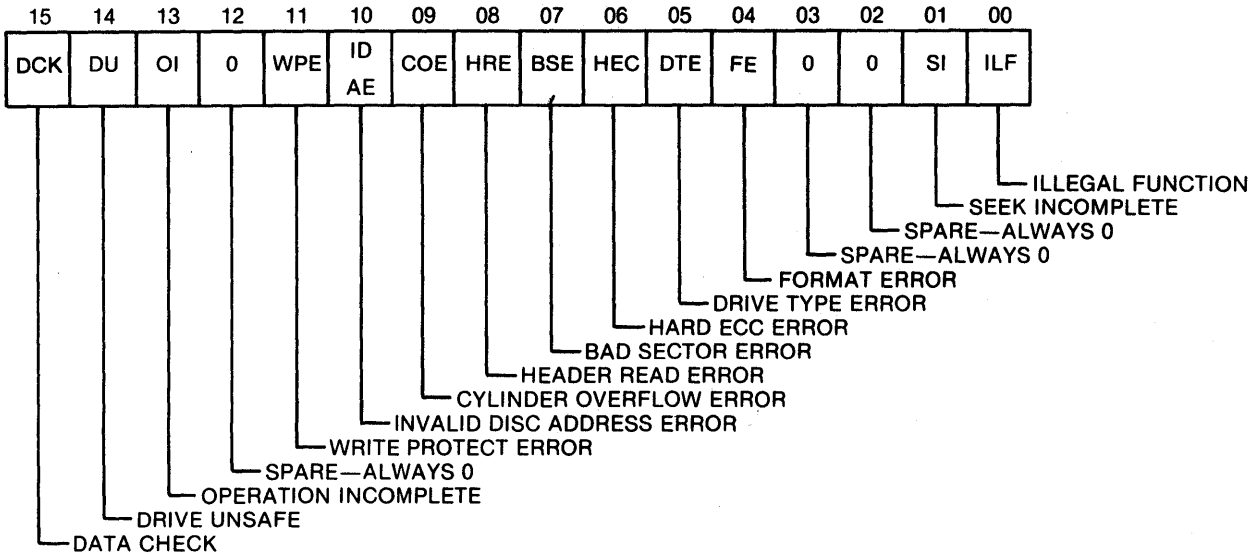
*Causes bit 15 in RKCS1 to set.

DRIVE STATUS REGISTER
777 452 (RKDS) Read Only Register



BIT(S)	DESCRIPTION
00	SPARE—ALWAYS 1
01	SPARE—ALWAYS 0
02	SPARE—ALWAYS 0
03	DRIVE FAULT—When set, indicates an error condition is detected within the drive and is prohibiting all operations. This bit is reset manually by clearing the fault condition within the drive.
04	SPARE—ALWAYS 0
05	SEEK ERROR—When set, indicates a seek was not completed within a specified time period after it was initiated.
06	DRIVE SELECTED—When set, the drive is selected and on line.
07	DRIVE READY—Drive Ready is a read-only bit which when set indicates the selected drive is up to speed, the heads are on cylinder and the drive is ready to accept commands. It is reset when these conditions are not met or when driving is seeking.
08	RK06/RK07—When set indicates RK07, when reset, RK06.
09-10	SPARES—ALWAYS 0
11	WRITE PROTECT—When set, the selected disc is write protected.
12	SPARE—ALWAYS 0
13	POSITIONING IN PROGRESS—When set, the selected disc is write protected.
14	SEEK INCOMPLETE—This read-only bit sets when the drive is ON CYLINDER. SEEK or RESTORE is completed.
15	ALWAYS 1

ERROR REGISTER
777 454 (RKER)



BIT(S) DEFINITION

00 ILLEGAL FUNCTION—When set, this read-only bit indicates that an illegal command has been loaded into the RKCS1 register.

01 SEEK INCOMPLETE—When set, this read-only bit indicates that a seek operation has not been completed by the selected drive.

02 SPARE—ALWAYS 0

03 SPARE—ALWAYS 0

04 FORMAT ERROR—When set in conjunction with bit 09, indicates that the sector pulses are too close together. Diagnostic message is "sector size too small."

05 DRIVE TYPE ERROR—This read-only bit is set when the drive type status does not compare with Control Drive Type bit (RKCS1, bit 10), i.e., RK06 instead of RK07 or vice versa.

06 HARD ECC ERROR—When set, this read-only bit indicates that a data error detected by the ECC logic cannot be corrected using ECC.

07 BAD SECTOR ERROR—When set, this read-only bit indicates that a data transfer was attempted to or from a sector and the sector is bad.

08 HEADER READ ERROR—When set, this read-only bit indicates that an uncorrectable ECC error was detected on a sector header during a data transfer. If bit 13 is also set, the error indication is header not found.

09 CYLINDER OVERFLOW ERROR—When set, the word count is not equal to zero and the operation is programmed to continue beyond the last logical sector on the disc. This will occur on a Read or Write data operation.

10 INVALID DISC ADDRESS ERROR—When set, this bit indicates that an invalid cylinder address or an invalid head address has been detected during a Seek command or Write/Read data command.

11 WRITE PROTECT ERROR—When set, this read-only bit indicates that the drive received assertion of Write Gate while in the write protect mode.

12 SPARE—ALWAYS 0

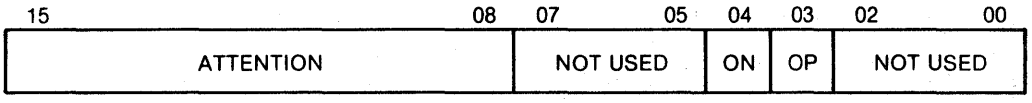
13 OPERATION INCOMPLETE—When set, this read-only bit indicates that during a data transfer, the desired header could not be found. This error can result from any one of the following:

- Head Misposition
- Incorrect Head Selection
- Read Channel Failure
- Improper Pack Formatting

14 DRIVE UNSAFE—When set, this read-only bit indicates that a Read/Write Unsafe condition has been detected.

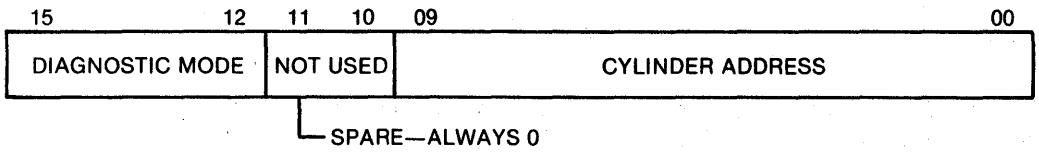
15 DATA CHECK—When set, this read-only bit indicates that a data error was detected when the current sector was read.

ATTENTION SUMMARY AND OFFSET REGISTER 777 456 (RKAS/0F)



BIT(S)	DEFINITION
00-02	SPARE—ALWAYS 0
03	OFFSET POSITIVE—Offsets the head in the positive direction from the centerline of the track (positive is from the lower cylinder number toward the higher cylinder number).
04	OFFSET NEGATIVE—Offsets the head in the negative direction from the centerline of the track (negative is from the higher cylinder number toward the lower cylinder number).
05-07	SPARE—ALWAYS 0
08-15	ATTENTION—The eight Attention bits, one for each drive, correspond to the logical unit number of each drive. Each bit indicates the state of the Drive Status Change flip-flop in the corresponding drive. All of the ATN bits are continuously scanned and updated (polled).

DESIRED CYLINDER ADDRESS REGISTER
777 460 (RKDC)



BIT(S) DEFINITION

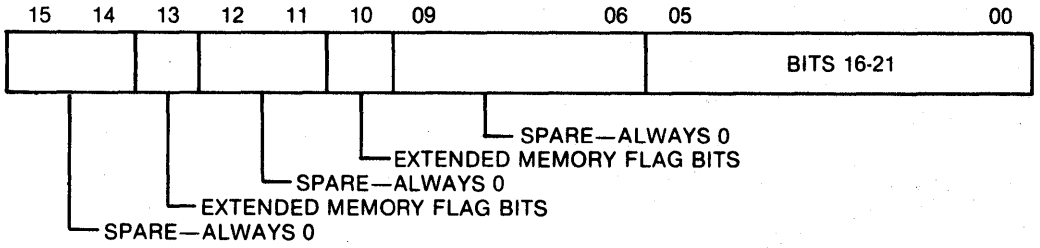
00-09 CYLINDER ADDRESS—The cylinder address in RKDC is the emulated address. The actual mapped address is contained in RKMR2. The cylinder number is written in octal in the register.

10-11 SPARE—ALWAYS 0

12-15 DIAGNOSTIC MODE—These bits are as follows:

15	14	13	12	
0	0	0	0	RK06/RK07 Emulation Mode
1	0	0	0	MAP OVERRIDE MODE—These bits can be set by the programmer to override the mapping algorithm. When set, the head, cylinder, and sector addresses supplied to the controller specify absolute address to the disc. Could be typically used to permit the device handler to be modified to take advantage of the head per track options available in some disc drives.
1	1	0	0	DMA BUFFER TEST MODE—Allows Reading/Writing of the controller data buffer using the computer DMA interface. The controller word count and memory address registers are used to set up the DMA transfer with a maximum transfer of 1024 bytes starting with location 0 of the data buffer. The write command, 23_8, will write from the buffer. The read command, 21_8, will read from the data buffer.
1	1	1	0	ECC TEST MODE
1	1	0	1	I/O BUS INTERFACE TEST MODE
1	1	1	1	I/O W/R INTERFACE TEST MODE

EXTENDED MEMORY ADDRESS REGISTER (22-Bit)
777 462 (RKXMA)



BIT(S) DEFINITION

00-05 BITS 16-21—These bits, when set, define bits 16-21 of the 22-bit extended memory.

06-09 SPARE—ALWAYS 0

10, 13 EXTENDED MEMORY—When bits 10 and 13 are set, the 22-bit address is used.

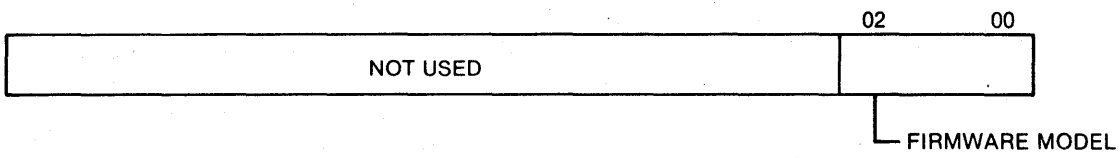
11-12, 14-15 SPARE—ALWAYS 0

READ/WRITE BUFFER REGISTER
777 464 (RKDB)

BIT(S) DEFINITION

00-15 The Data Buffer Register is a Read/Write register. Writing into the register loads data into the controller data buffer, one word at a time. Reading the register reads data from the controller data buffer. The commands INIT, CLL and SRC clears the Data Buffer address allowing writing or reading of the Data Buffer starting at location 0. Reading from or writing into the buffer will increment the address register.

MAINTENANCE REGISTER 1
777 466

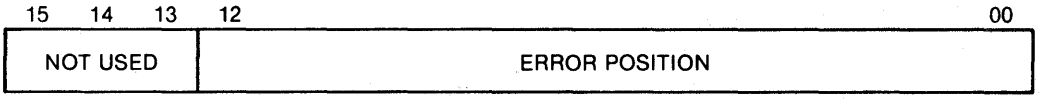


BIT(S) DEFINITION

00-02 FIRMWARE MODEL—These three bits define the model number of the firmware used in the controller.

03-15 SPARE—ALWAYS 0

ECC POSITION REGISTER
777 470 (RKECPS)

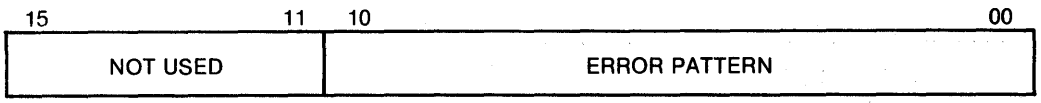


BIT(S) DEFINITION

00-12 ERROR POSITION—These read-only bits define the start location of an error burst (containing from one to eleven error bits) within a 256-word data field, sequence. The position is valid if the error is ECC correctable.

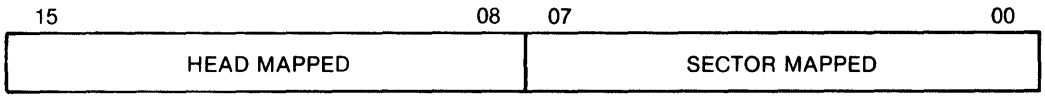
13-15 SPARE—ALWAYS 0

ECC PATTERN REGISTER
777 472 (RKECPT)



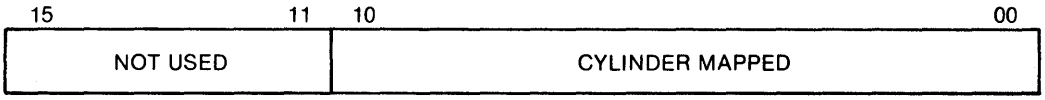
BIT(S)	DEFINITION
00-10	ERROR PATTERN—These are read-only bits that provide an 11-bit correction pattern for an error burst that does not exceed 11 error bits in length and is therefore ECC correctable.
11-15	SPARE—ALWAYS 0

MAINTENANCE REGISTER 2
777 474 (RKMR2)



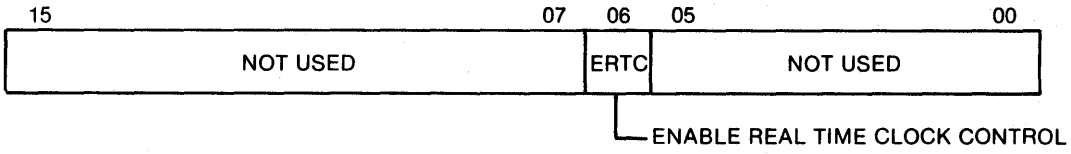
BIT(S)	DEFINITION
00-07	SECTOR MAPPED—These bits define the actual mapped sector address in the disc as opposed to the emulated address.
08-15	HEAD MAPPED—These bits define the actual mapped head address on the disc as opposed to the emulated address.

MAINTENANCE REGISTER 3
777 476



BIT(S)	DEFINITION
00-10	CYLINDER MAPPED—These bits define the actual mapped cylinder address on the disc as opposed to the emulated address.
11-15	SPARE—ALWAYS 0

ENABLE REAL TIME CLOCK CONTROL REGISTER
777 546



The Enable Real Time Clock Control register performs a separate function from the other registers. During a read operation, bit 06 is always reset. During a write operation bit 06 is set enabling the real time clock control. Switch S9 must be ON to enable this function.

SECTION 5
TROUBLESHOOTING AND THEORY

This section describes troubleshooting procedures at three levels of complexity: basic system, controller symptoms and detailed analysis. Basic system troubleshooting procedures are visual checks not requiring test equipment and may be performed by the operator. Controller symptom procedures may require a scope, meter, extender board or diagnostics and should be performed by a technician. Detailed analysis is troubleshooting at the IC level, and is presented for engineers or system analysts for controller evaluation. The latter method may require the use of test equipment and the material presented here: board layout, term listing, theory of operation and logic diagrams.

CAUTION

Any troubleshooting requires a familiarity with the installation and operation procedures in this manual, the appropriate DEC manual, and the disc drive manufacturers manual. Ensure power is off when connecting or disconnecting board or plugs.

BASIC SYSTEM TROUBLESHOOTING

The following should be checked before power is applied:

1. Verify that all signal and power cables are properly connected. Ribbon cable connectors are *not* keyed. The arrows on the connectors should be properly aligned.
2. Verify that all switches are properly set as described in Sections 2 and 3.
3. Verify that all modules are properly seated in the computer and properly oriented.

The following should be checked during or after application of power:

1. Verify that the computer and disc drive generate the proper responses when the system is powered up.
2. Verify that the computer panel switches are set correctly.
3. Verify that the console can be operated in the local mode. If not, the console may be defective.
4. With the drive power switch on, verify that the drive READY light is on.
5. Verify that the green diagnostic light on the controller is on.

CONTROLLER SYMPTOMS

Controller symptoms, possible causes and checks/corrective action are described in Table 5-1. Voltage checks should be performed before troubleshooting more complex problems. The +12V and −5V sources are shown on Logic Diagram Sheet 20. The +5V source may be checked from any component shown on the other logic diagrams.

PHYSICAL LAYOUT

The physical layout of the board is shown in Figure 5-1. Column and row numbers on the layout correspond to the numbers on each IC on the logic diagrams.

TERM LISTING

The input and output terms for each logic diagram are described in Table 5-2. The sources and destinations refer to the sheet numbers on the logic diagrams.

Table 5-1. Controller Symptoms

Symptom	Possible Causes	Check/Corrective Action
1. Green DIAG light on the controller is OFF.	1. Microprocessor section of controller inoperative: a. Bad oscillator b. Short or open on board c. Bad IC d. PROMs not properly seated	1. Controller/Place controller on extender board. With a scope, check the pins on the 2901. All pins except power and ground should be switching. Check for "stuck high" or "stuck low," or half-amplitude pulses. Check + 12V and − 5V power and + 5V at various IC's. Check PROMs A1 through A7 for proper seating. Check oscillator.
2. No communication between console and computer.	2. I/O section of controller "hanging" Q Bus: a. $\overline{\text{DEN}}$ always low b. Shorted bus transceiver IC. c. Bad CPU board.	2. Computer interface logic of controller/ a. Check signal $\overline{\text{DEN}}$ for constant assertion. b. Check I/O IC's. Remove controller board to see if trouble goes away. (Ensure slot is filled or jumpered.) c. Run CPU diagnostics.
3. No data transfers to/from disc.	3. Disc not ready, bad connection, or bad IC in register section of the controller.	3. Disc/Consult the disc manufacturer's manual for proper setting of disc switches, or READY, NO FAULT, or UNSAFE lights. Check cable connections. Controller Registers/Using ODT, examine the Drive Status Register. The DISC READY and SELECTED must be "one's." Using ODT, deposit "ones" and "zeros" in the remaining disc registers and verify proper register data.
4. Data transferred to/from from disc incorrect.	4. Multiple Causes: a. Bad memory in backplane b. Noise or intermittent source of DC power in computer. c. Bad IC in disc I/O section of controller. d. Bad area on disc. e. Disc heads not properly aligned.	4. Computer-controller-disc/ a. Run memory diagnostics. b. Check AC and DC power. c. While operating, check lines from controller to disc with a scope for short or open. d. Run the Format and Diagnostic Test program (Section 3). If errors occur at the same place on the disc, it is probably a bad area on the disc. Assign alternate tracks as specified in Section 3. e. Consult disc drive manufacturer's manual and align heads.
5. Intermittent failure—Controller runs for a short time after power is applied and then fails.	5. Failure of heat sense component on controller.	5. Isolate the bad component by using heat and cooling methods (heat gun, freon spray) and replace the bad component.

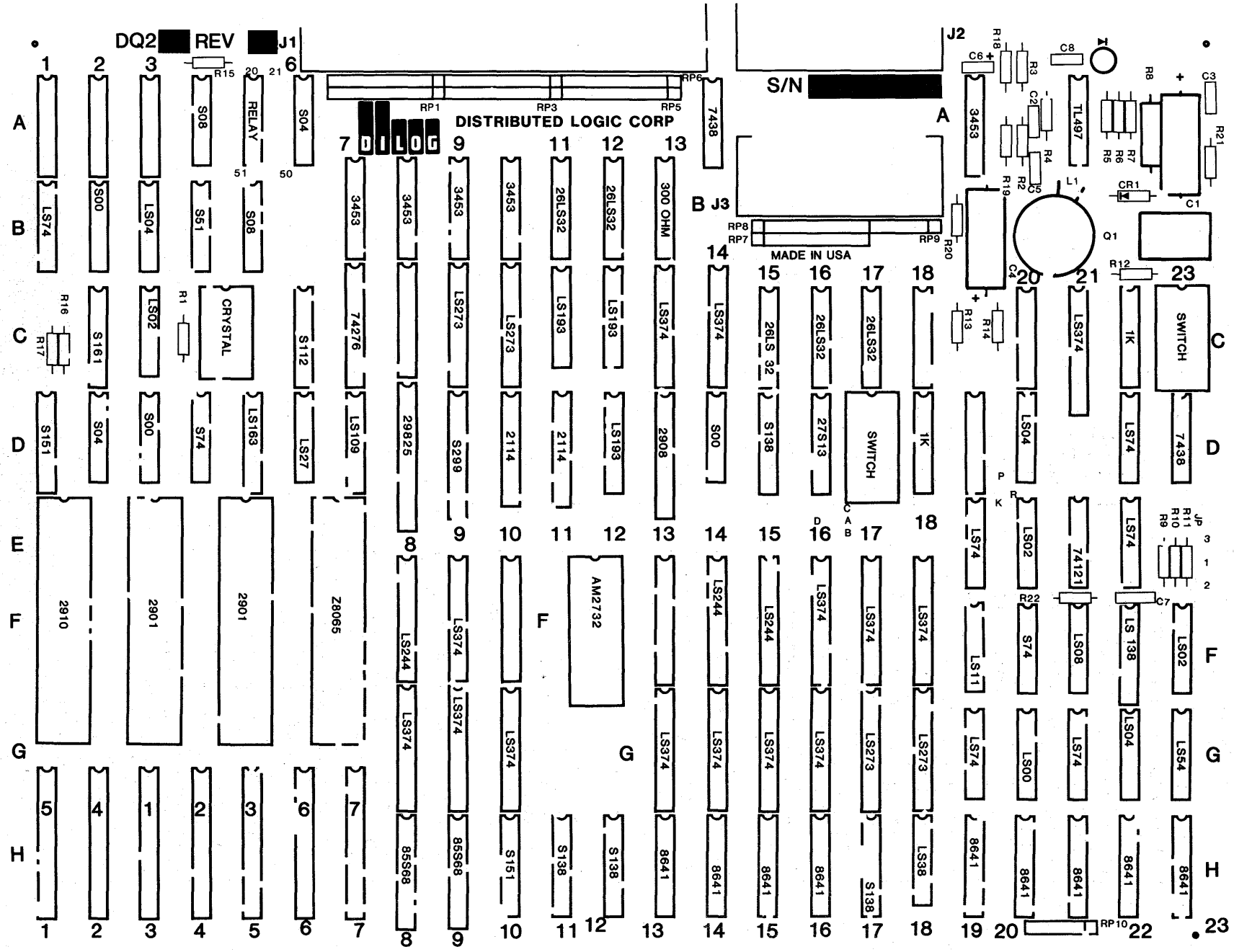


Figure 5-1. Board Layout

Table 5-2. Term Listing

Term	Origin	Description
AMF	17	Address Mark Found From Disc
BA00-BA09+	15	Buffer Address Counter Bits 00-09
BBS7L	BUS (AP2)	Bus Peripheral Address Select
BBS7+	4	Peripheral Address Select
BC4+	13	Bit Count 4 From Bit Counter
BDAL00L	BUS (AW2)	Bus Data/Address Line 00
BDAL01L	BUS (AV2)	Bus Data/Address Line 01
BDAL02L	BUS (BE2)	Bus Data/Address Line 02
BDAL03L	BUS (BF2)	Bus Data/Address Line 03
BDAL04L	BUS (BH2)	Bus Data/Address Line 04
BDAL05L	BUS (BI2)	Bus Data/Address Line 05
BDAL06L	BUS (BK2)	Bus Data/Address Line 06
BDAL07L	BUS (BL2)	Bus Data/Address Line 07
BDAL08L	BUS (BM2)	Bus Data/Address Line 08
BDAL09L	BUS (BN2)	Bus Data/Address Line 09
BDAL10L	BUS (BP2)	Bus Data/Address Line 10
BDAL11L	BUS (BR2)	Bus Data/Address Line 11
BDAL12L	BUS (BS2)	Bus Data/Address Line 12
BDAL13L	BUS (BT2)	Bus Data/Address Line 13
BDAL14L	BUS (BU2)	Bus Data/Address Line 14
BDAL15L	BUS (BY2)	Bus Data/Address Line 15
BDAL16L	BUS (AC1)	Bus Address Extension Line 16
BDAL17L	BUS (AD1)	Bus Address Extension Line 17
BDAL18L	BUS (BC1)	Bus Address Extension Line 18
BDAL19L	BUS (BD1)	Bus Address Extension Line 19
BDAL20L	BUS (BE1)	Bus Address Extension Line 20
BDAL21L	BUS (BF1)	Bus Address Extension Line 21
BDINL	BUS (AH2)	Bus Data In
BDIN+	4	Data In
BDMGIL	BUS (AR2)	Bus DMA Grant In
BDGOL	BUS (AS2)	Bus DMA Grant Out
BDMRL	BUS (AN1)	Bus DMA Request
BDOUTL	BUS (AE2)	Bus Data Out
BDOUT+	4	Data Out
BEVENT	BUS (BR1)	Real Time Clock Control
BFULE+	3	Enable Buffer Full
BFULL–	15	Buffer Full
BIAKIL	BUS (AM2)	Bus Interrupt Acknowledge In
BIAKOL	BUS (AN2)	Bus Interrupt Acknowledge Out
BINITL	BUS (AT2)	Bus Initialize—Clear
BIRQ4L	BUS (AL2)	Bus Interrupt Request Level 4
BIRQ5L	BUS (AA1)	Bus Interrupt Request Level 5
BIRQ6L	BUS (AB1)	Bus Interrupt Request Level 6
BIRQ7L	BUS (BP1)	Bus Interrupt Request Level 7
BIT0-BIT10	16	Control Bits to Disc Drives
BIT7+,–	13	"Complete Byte" Output of Bit Counter
BPOK-H	BUS (BB1)	Primary Power O.K.
BPOK–	4	Primary Power O.K.
BRPLYL	BUS (AF2)	Q Bus Reply
BRPLY+	4	Q Bus Reply
BSACKL	BUS (BN1)	DMA Select Acknowledge
BSYNCL	BUS (AJ2)	Bus Synchronize I/O
BTSPF+	2	Bootstrap Flag
BWTBTL	BUS (AK2)	Bus Write Byte
BWTBT+	4	Bus Write Byte
BYTCK+	13	Byte Clock
COUT+	10	Carry Out
CP1	12	Control Pulse 1
CP2	12	Control Pulse 2
CP3	12	Control Pulse 3
CP4	12	Control Pulse 4

Table 5-2. Term Listing (Continued)

Term	Origin	Description
CP5	12	Control Pulse 5
CP6	12	Control Pulse 6
CP7	12	Control Pulse 7
CRCER+	13	Cyclic Redundancy Check Error
CR1-0/7	9	Control Register One Bits 0-7
CR2-0/7	9	Control Register Two Bits 0-7
CR3-0/7	9	Control Register Three Bits 0-7
CR4-0/7	9	Control Register Four Bits 0-7
CR5-0/7	9	Control Register Five Bits 0-7
CR6-0/7	9	Control Register Six Bits 0-7
CSA0+/CSA9+	8	Control Store Address Bits 0-9
DA16+	3	Extended Data/Address Bit 16
DA17+	3	Extended Data/Address Bit 17
DAT0+/DAT7+	14,15	Data Buffer Bits 0-7
DBWC1+	13	Data Buffer Write Control In
DBWS–	13	Data Buffer Write Strobe
DBWS1–	13	Data Buffer Write Strobe In
DB00+/DB07+	6	Data Bus Bits 0-7
DB08+/DB15+	7	Data Bus Bits 8-15
DEN–	6	Data Enable
DMGI+	4	DMA Grant In
D00+/D07+	2,3,4,9,11, 12,14,17, 18,19	D-Bus Bits 0-7
EADD+	3	Enable Address
EADD–	6	Enable Address
EBITC+	3	Enable Bit Count
ECCO+	19	Error Correction Code Out
EDATA+	3	Enable Data
ENRD–	13	Enable Read Data Register
ENWD–	13	Enable Write Data To Buffer
FAULT	17	Drive Fault
GDATA+	13	Gated Read Data
GSCLK–	3	Gated System Clock
GTIRQ+	5	Gated Transmit Interrupt Request
IAKI+	4	Interrupt Acknowledge In
IAKIG–	2	Interrupt Acknowledge In Grant
INDEX	17	Index Pulse From Drive
INIT+	4	Initialize
LXR0–	11	Load External Register Data Out MSB
LXR1–	11	Load External Register Data Out LSB
LXR2–	11	Load External Register DMA Address MSB
LXR3–	11	Load External Register DMA Address LSB
LXR4–	11	Load External Register Data Buffer LSB
LXR5–	11	Load External Register Data Buffer MSB
LXR6–	11	Load External Register Data Buffer
LXR7–	11	Load External Register Extended Address
LXR9–	11	Load External Register Drive Control Tags
LXRA–	11	Load External Register Drive Control Bus Bits
LXRB–	11	Load External Register Vector Address
LXRC–	11	Load External Register System Control
LXRD–	11	Load External Register Bootstrap Address
LXRE–	11	Load External Register CPU Bus Control

Table 5-2. Term Listing (Continued)

Term	Origin	Description
LXRF –	11	Load External Register RAM Destination
MRQB +	3	Memory Request Q Bus
OCD + / –	16	Open Cable Detect
ONCYL + / –	17	On Cylinder From Drive
PICK	16	Power Pick
QBUSA	2	Q Bus Access
Q3	10	Q Register Shift Line
RAM3 +	10	Shift Output of ALU RAM
RCLOCKA/B + / –	18	Read Clock From Drives A or B
RDATAA/B + / –	18	Read Data From Drives A or B
RDATA +	18	Read Data
REP	19	Read Error Pattern
RESET	4	Reset Signal to Controller
RMCLK	3	RAM Clock
RSYNC –	13	Read Synchronize
R/WCK –	18	Read/Write Clock
R/WSRE +	3	Read/Write Shift Register Enable
SELA/B	18	Drives A or B Selected
SENDA/B	18	Drives A or B Seek End
SCLK	3	System Clock
SCLOCKA/B	18	Servo Clock From Drives
SDB08 +	2	Slave Data Bus Bit 8
SEEKA/B	18	Seek End From Drives
SEC + / –	17	Sector Pulse From Drive
SERR + / –	17	Seek Error From Drives
SL/IN +	2	Slave Interrupt Acknowledge Request
TAG1/2/3	16	Tag Lines To Drives
TDIN +	3	Transmit Data In
TDOUT +	3	Transmit Data Out
TDMG +	2	Transmit Direct Memory Grant
TDMR +	2	Transmit Direct Memory Request
TIAK +	2	Transmit Interrupt Acknowledge
TIRQ +	3	Transmit Interrupt Request
TRPLY	3	Transmit Reply
TSACK	2	Transmit Select Acknowledge

Table 5-2. Term Listing (Continued)

Term	Origin	Description
TSYNC	3	Transmit Synchronize
TWTBT	3	Transmit Write Byte
UNRDY	17	Drive Unit Ready
USEL0/1/2/3	16	Drive Unit Select Bits 0, 1, 2, 3
USELA/B	18	Drive Unit Select A, B
USTAG	16	Drive Unit Select Tag
VEC –	8	Vector Address Register Select
WDATA +	14	Write Data Bit Stream
WCLOCKA/B + / –	18	Write Clock To Drives A or B
WDATAA/B + / –	18	Write Data To Drives A or B
WPRT	17	Drive Write Protect
WREN –	3	Write Enable
XSD0	11	External Source Decode Slave Address
XSD1	11	External Source Decode Data Input MSB
XSD2	11	External Source Decode Data Input LSB
XSD3	11	External Source Decode CPU Bus Status
XSD4	11	External Source Decode Data Buffer
XSD5	11	External Source Decode Disc Drive Status
XSD6	11	External Source Decode Seek End Status
XSD7	11	External Source Decode Error Status Register
XSD8	11	External Source Decode Bootstrap PROM
XSD9	11	External Source Decode Configuration Switches
XSDA	11	External Source Decode Literal PROM
XSDB	11	External Source Decode RK06 Switches
XSDF	11	External Source Decode RAM
Y00/Y07	10	Y-Bus Bits 0-7
ZERO +	10	Zero Output of 2901
1K0V +	15	1024 Address Counter Overflow

THEORY

The controller may be examined as three parts: computer interface, disc interface and controller internal functions. Signals from and to the computer are described in Section 1, Table 1-1. Signals from and to the disc drive are described in Tables 1-2 and 1-3. Figure 5-2 is a simplified block diagram illustrating the interfaces and some of the functional components. Single lines in the illustration represent serial data and the wider lines represent parallel data. A detailed block diagram of the controllers is shown on Sheet 1 of the logic drawings. The numbers in the blocks on Sheet 1 refer to the sheet numbers of the other logic diagrams.

Computer Interface

The purpose of the computer interface is to (1) buffer lines between the Q Bus of the LSI-11 computer and the controller, and (2) to synchronize information transfers. The controller is a slave device during initialization and status-transfer sequences. The controller is selected by base address 777 440_8. The controller is bus master during data transfers and either receives data from or outputs data to the computer memory via the LSI-11 DMA facility.

The control lines request information transfers, select the type and direction of transfers, and synchronize the transfers. The control lines are unidirectional and used for "bus arbitration." Bus synchronization is fully controlled by the controller microprocessor. This allows the computer bus to be used by other devices when the disc controller is busy with internal functions and controller/disc data transfers.

Data bus driver/receiver registers 13H through 16H (Sheets 6 and 7) buffer the input data and distribute it as DB 00-15 in the controller. The DB

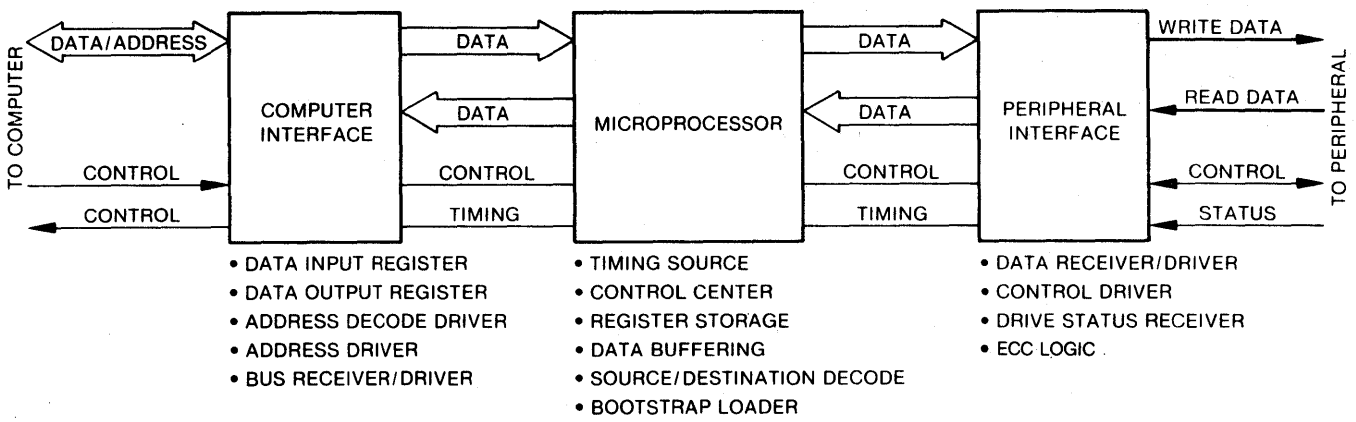


Figure 5-2. Simplified Block Diagram

signals are routed to a data input MUX and address decode registers located on Sheets 12 and 2.

Output data and addresses from the microprocessor Y Bus (Y00-Y07) is latched by registers 13G through 16G, and transferred to the Q Bus via bus driver/receivers 13H through 16H.

Note that the Device Enable signal (DEN−) is active when either Address Enable (EADD) or Data Enable (EDATA) signal is active. DEN controls the operating mode of all data and address driver/receivers, under control of the firmware, via the Y Bus (Sheets 6 and 7).

Disc Interface

The disc is connected to the controller by separate data and control cables. A common control cable is daisy-chained to both drives in a multiple-drive configuration, while separate data cables are always used.

Serial read data is received by receivers 16C or 15C (Sheet 18) and then converted to parallel data by the read/write shift register 9D (Sheet 14). In the reverse direction, parallel data from the data buffer is converted to serial data by the shift register, then sent to data cable drivers (Sheet 18).

The Control Cable drivers 7B, 8B, 9B and 10B (Sheet 16) are always enabled and are driven by the output of registers 9C and 10C, which act as latches to capture the Y Bus data from the microprocessor.

Control Cable receivers 11B and 12B (Sheet 17) supply data to the disc status register/multiplexer 13C (Sheet 17) at all times. The data is available to the microprocessor via the D Bus when signal XSD5− is active.

Controller Internal Functions

The microprocessor is the timing and control center of the controller. The microprocessor is controlled by instructions stored in programmable read-only memory (PROM). The instructions, called "firmware," cause the microprocessor to operate in a prescribed manner during each of the computer-selected functions. The functions are established by a series of instructions issued by the LSI-11.

Because the disc and computer transfer data at different rates, it is necessary to buffer data going to and from the disc. High-speed RAM allows a full sector of data to be buffered during read and write operations.

All data transfer and computer/disc protocol is under microprocessor control. This feature allows modification of controller operating characteristics by making only changes to the firmware. Input/output logic remains essentially unchanged.

The output from the microprocessor is the "Y Bus". Y Bus instructions govern all controller operations by acting as the controller source for all receivers and drivers either directly or through the source/destinations decode IC's (Sheet 11).

The "D Bus" is the data input to the microprocessor. Tri-state drivers allow many signal sources to be connected to the bus while only one at a time is enabled by the source/destination decode logic on Sheet 11.

The following list describes D Bus enabling signals:

Function	Term	Component Enabled	Sheet
Slave Address	XSD0	16F	2
Data Input (MSB)	XSD1	14F	12
Data Input (LSB)	XSD2	15F	12
Q Bus Status	XSD3	18F	12
Data Buffer	XSD4	8F	14
Disc Status	XSD5	13C	17
Seek End/Unit Select	XSD6	14C	18
Error Status	XSD7	9F	19
Boot PROM	XSD8	12F	11
Switches	XSD9	17F	3
Literal	XSDA	7H	9
RK06 Switches	XSDB	21C	5
Scratch RAM Enable	XSDF	8H, 9H	12

All data on the D Bus is under control of the firmware as decoded by source PROMs 11H, 15D on Sheet 11. The microprocessor selects the proper input data by enabling one of the above lines.

The Y Bus is the microprocessor output. Output of the microcode PROM 5H (Sheet 9) is decoded by 12H and 17H (Sheet 11) to select the destination of the data on the Y Bus.

The following list describes Y-Bus enabling signals:

Function	Term	Component Enabled	Sheet
Data Out Register (MSB)	LXR0	13G	7
Data Out Register (LSB)	LXR1	15G	6
DMA Address (MSB)	LXR2	14G	7
DMA Address (LSB)	LXR3	16G	6
Data Buffer Address (LSB)	LXR4	11C, 12D	15
Data Buffer Address (MSB)	LXR5	12C	15, 19
Data Buffer Load	LXR6	7C, 8G	13, 14
Load Extended Address	LXR7	13D	7
Drive Control (Tags)	LXR9	10C	16
Drive Control (Bus 0-7)	LXRA	9C	16
Load Vector Address	LXRB	10G	8
System Control	LXRC	18G	3
External Event	LXRD	22D	17
Q Bus Control	LXRE	17G	3
RAM Destination	LXRF	8H, 9H	12

With the single exception of bus reply detector 21E (Sheet 3), all Y Bus data and address activity is controlled by the 15 signals shown above.

Each LXR (Load External Register) signal activates a register which, in conjunction with Y Bus data, latches the appropriate data word.

Control Registers CR1 through CR6 are the outputs of the microcode PROMs (Sheet 9). These signals control the microprocessor functions and provide the data to the source/destination decode logic (Sheet 11).

Data Buffer

The data buffer and associated logic are shown on Sheets 13, 14 and 15. Data Transfers to and from the buffer are both two-step operations. First, an entire sector of data is loaded into the buffer during either a read or write operation. Once loaded, the buffer contents are then transferred to disc or LSI-11 memory in a completely separate operation. Figure 5-3 illustrates read and write operations to and from the RAM data buffer.

During a write operation, parallel data (Y00-Y07) is transferred from LSI-11 memory via microprocessor to the write data register 8G (Sheet 14). The data (DAT0-DAT7) is then transferred to the buffer 10D and 11D (Sheet 15). Parallel data (DAT0-DAT7) from the buffer is then transferred to shift register 9D, converted to serial data (W DATA), and transferred to the data cable driver 19A (Sheet 18).

During a read operation, serial read data (R DATA) from the data cable receivers is ANDED with Enable Bit Count (E BIT C) resulting in the signal G DATA. This signal enters the shift register F7 and is transfered as parallel data to the Read Data register 8D, for transfer to the data buffer while the next byte is being shifted through shift register 9D. The read data from the buffer (DAT0-DAT7) is transferred to driver 8F (Sheet 14) to the microprocessor for transfer to LSI-11 memory.

The counter located at 11C, 12C and 12D (Sheet 15) is used to address the location in the buffer into which data can be written or read from. The counter has the capability of being preset to a specific starting address via the Y Bus of the microprocessor.

ERROR CORRECTION CODE (ECC) LOGIC

Functional Operation

The ECC Generator does not correct errors; it generates codes during write and read operations and during reading generates a syndrome. A syndrome is the result of merging check characters being read with check characters generated. A zero syndrome indicates no error; a non-zero syndrome indicates an error. This syndrome contains all the information necessary to find the error location and the error pattern, i.e., to allow error correction.

The error location is found by counting the number of clock pulses required to make the EP output go high. The error pattern is then available on the LP0-LP3 and Q0-Q7 outputs and can be used to exclusive OR with data. Depending upon the position of switch S5 (location D17), either the computer or the controller corrects the error. Note that some error patterns cannot be corrected. These are flagged to the computer.

Component Description

During a write operation a 32-bit ECC is appended to the header record and a 56-bit ECC is appended to the data record of each sector of information on the disc. ECC's are also generated while information is being read from the disc. The codes generated during the read operation are compared with the equivalent codes previously written. Discrepancies detected (errors) are signalled to the microprocessor and corrected if possible.

The ECC logic is shown on Sheet 19. The ECC Generator (7E), also referred to as the Burst Error

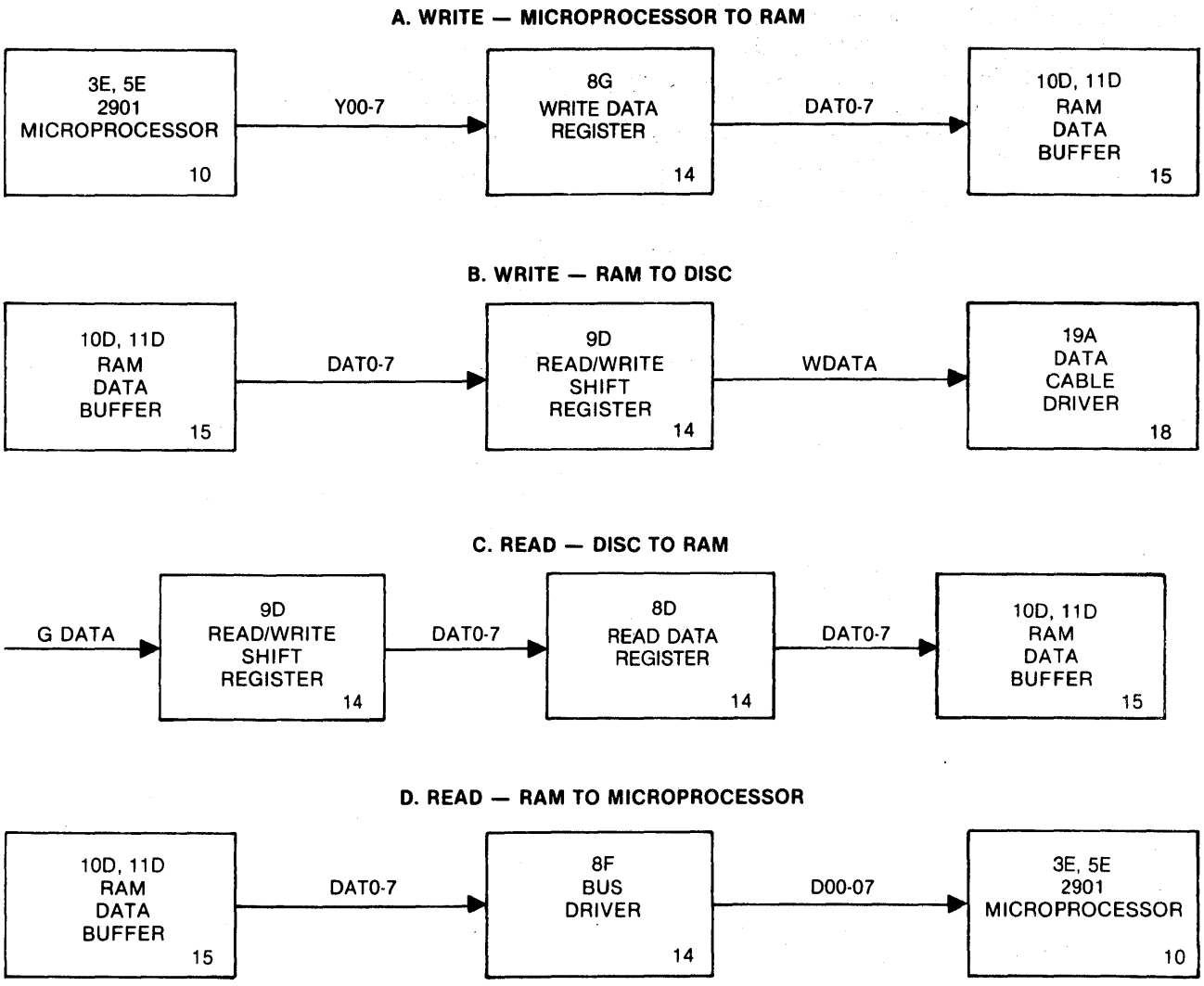


Figure 5-3. Data Paths

processor, is used in three different types of operations: write, read, and correct. Detailed information about the ECC generator is given by an AMD, AM9520/Z8065 product specification.

During writing or reading, information is connected to the D0 through D7 inputs of the ECC Generator. Select inputs S0 and S1 determine whether a 32- or 56-bit polynomial is being used. The 32-bit polynomial is used for ECC header checks, and the 56-bit polynomial is used for data record check. The Data Buffer Write Strobe (DBWS) is the source of Clock Pulses (CP) to the ECC Generator.

Control information for the ECC Generator from the Y Bus is stored by LXR5 into ECC Control Register 9G.

When MF— is asserted, the logic is initialized. Asserting REP (Read Error Pattern) makes outputs LP0-LP3 and Q0-Q7 active.

Control inputs P0-P3 are not used. The ECC Generator functions selected by the C0-C2 inputs are as follows:

C2	C1	C0	Function
L	L	L	Compute Check Bits
L	L	H	Write Check Bits
L	H	L	Read Normal
H	L	L	Load
H	H	L	Correct Normal

Check bit outputs Q0-Q7 are connected to the DAT0-DAT7 lines one byte at a time under control of REP and C0-C2. The remaining outputs of the ECC Generator are stored in ECC Status Register 9F by clock GSCLK. The microprocessor monitors ECC status on the D Bus during XSD7 time.

Outputs LP0-LP3 (Located Error Pattern), together with outputs Q0-Q7, provide the 12-bit

error pattern. Q7 is the MSB and LP0 is the LSB of the pattern. Outputs LP0-LP3 are active only when REP is asserted. Output AE (Alignment Exception) is asserted if the error pattern will not line up automatically during a correction sequence. This can occur because of the method of polynomial division implemented in the ECC generator.

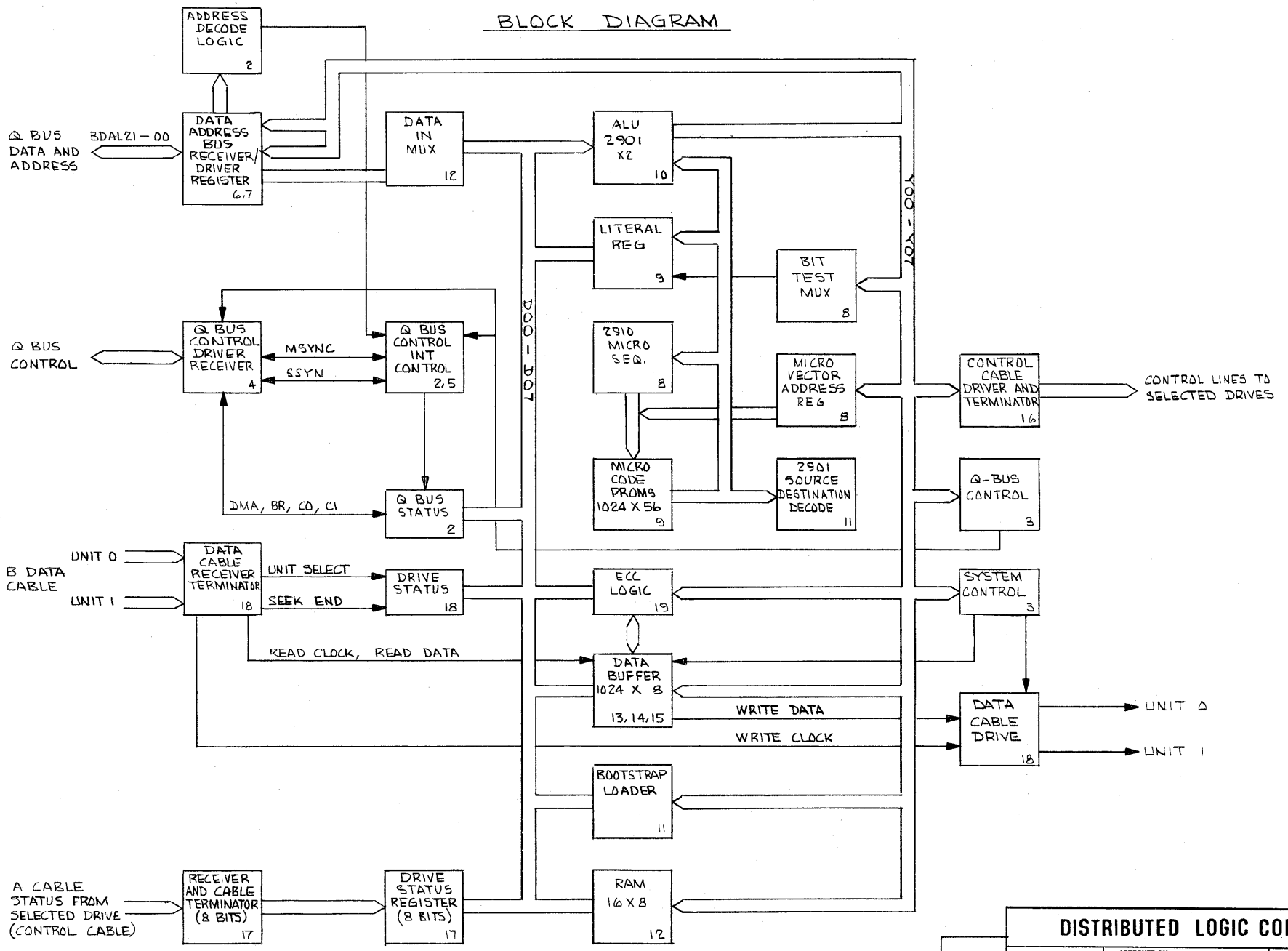
Output EP (Error Pattern) is asserted when the error pattern has been located during the correction sequence. Output ER is asserted if an error was detected after the last check byte had been read during a read function.

+12 VOLT TO −5 VOLT POWER SUPPLY

The +12 to −5 volt power supply shown on Sheet 20 is a dc-to-dc converter that produces the −5 volts required for the current mode line driver to the disc(s).

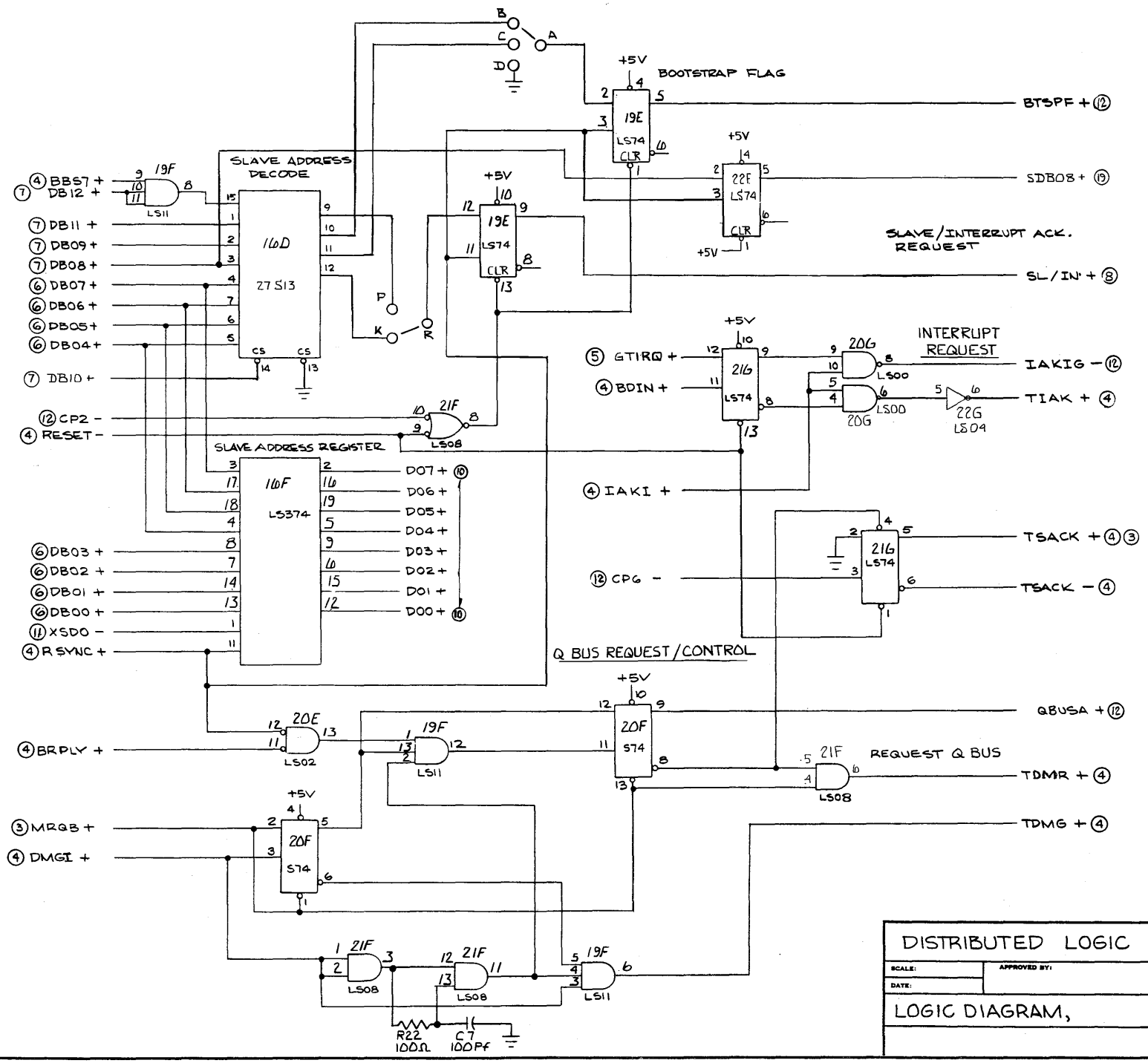
Input power is obtained from the +12 volts on the backplane. Oscillator R19, C6, 14A provides a rectangular pulse that drives current switch Q1. When the oscillator turns Q1 on, +12V is applied to L1 and an increasing current is produced. When the oscillator turns off Q1, the energy stored in L1 produces a negative voltage (at the top of L1), charging diodes C4 and C5 through diode CR1. Successive oscillator pulses cause the voltage across G5, G4 to build up to approximately −5 volts. Circuit 21A is a zener-referenced regulator that produces a threshold control voltage that regulates the duty cycle of the oscillator drive voltage applied to Q1 (increasing or decreasing "on" time). Circuit 21A thus controls the energy stored in L1 to maintain and regulate the voltage on G5, G4 at −5 volts under normal load conditions.

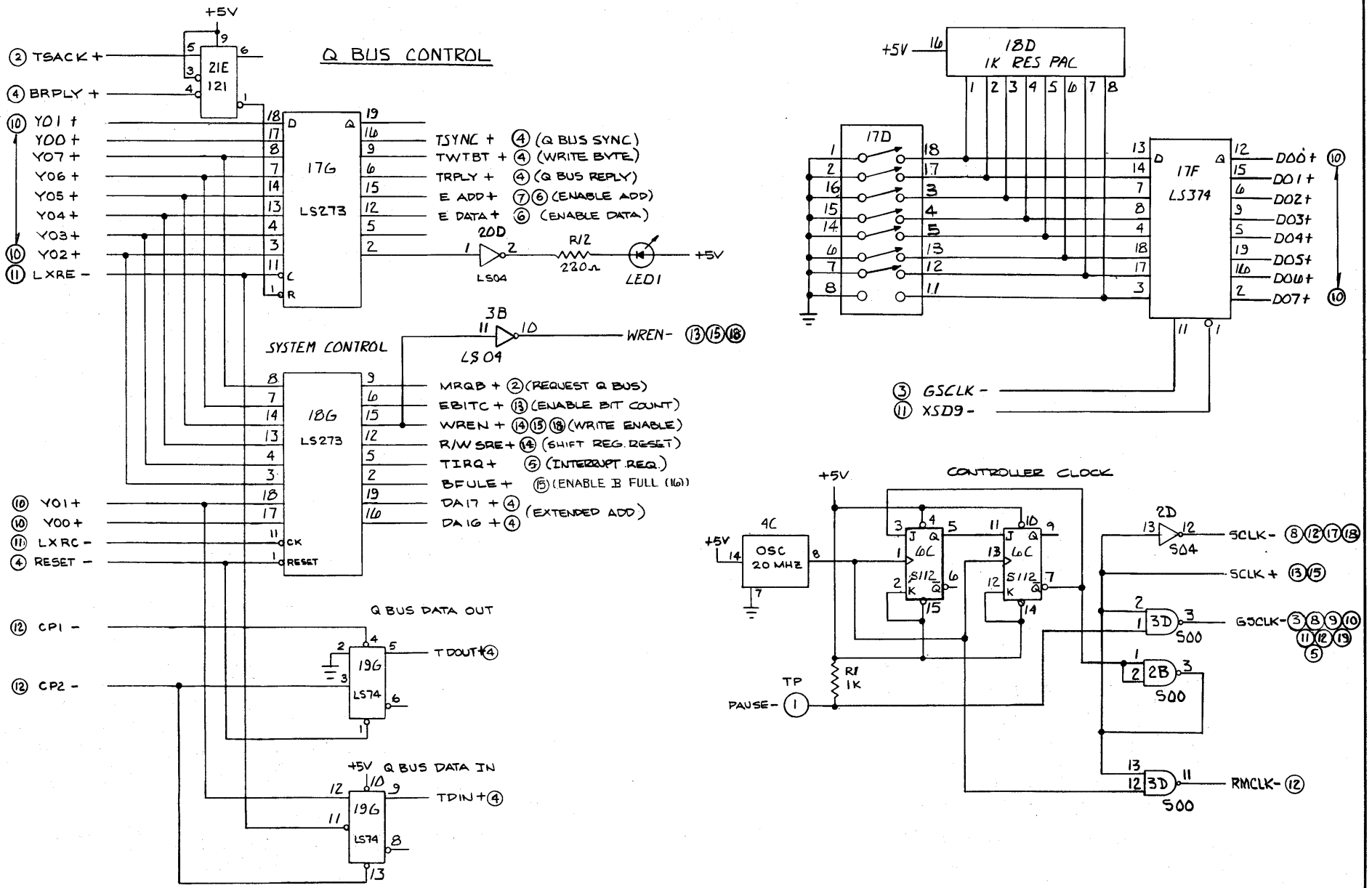
BLOCK DIAGRAM



DISTRIBUTED LOGIC CORP

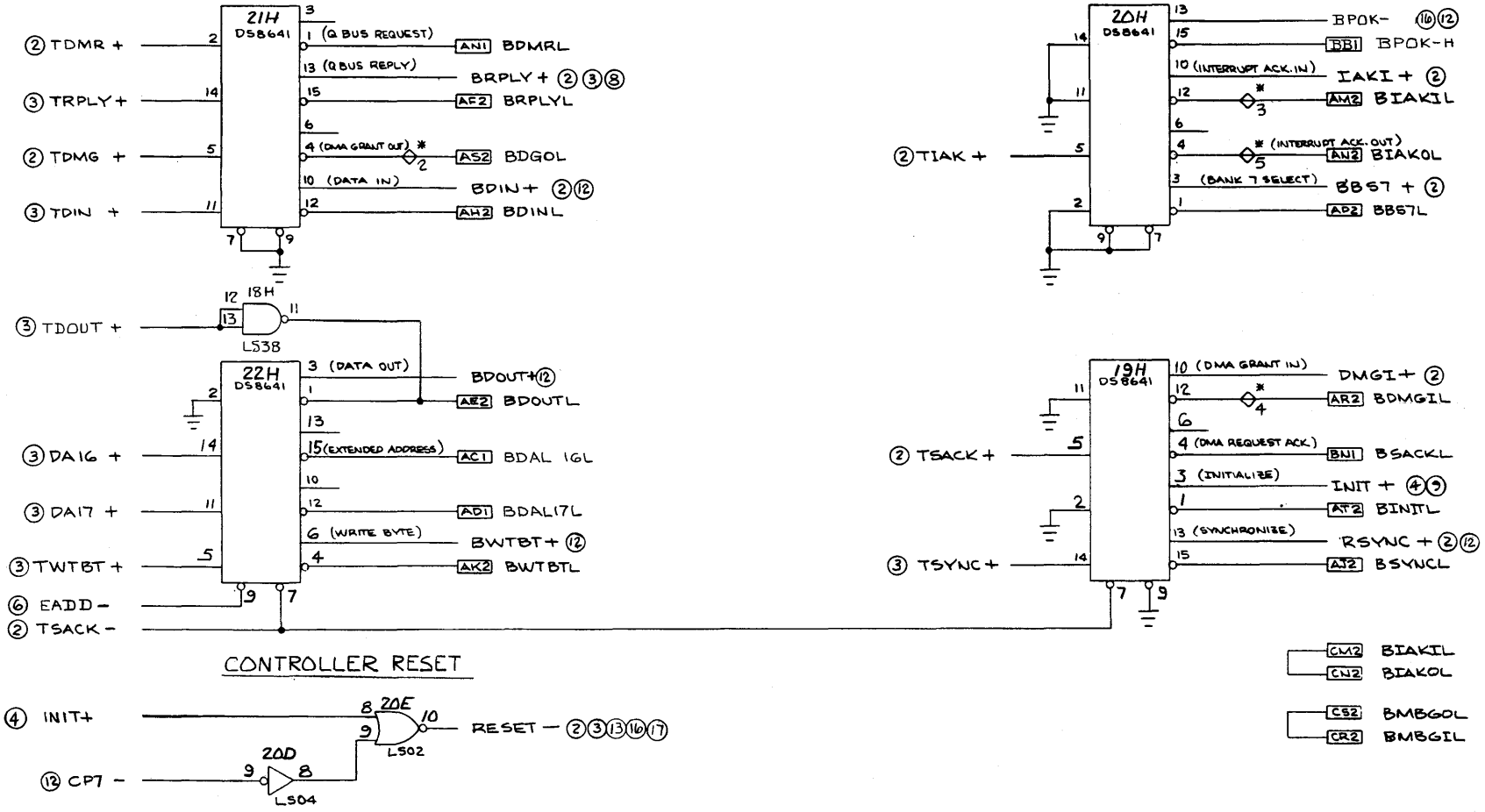
DQ22B	SCALE:	APPROVED BY:	DRAWN BY RQ
DQ21S	DATE:		REVISED 7-14-83
DQ21A	LOGIC DIAGRAM		
USED ON			DRAWING NUMBER 853027 B


BOOTSTRAP FLAG
BTSPF + (12)
SDBO8 + (19)
SLAVE/INTERRUPT ACK. REQUEST
SL/IN + (8)
INTERRUPT REQUEST
IAKIG − (12)
TIAK + (4)
TSACK + (4)(3)
TSACK − (4)
Q BUS REQUEST/CONTROL
QBUSA + (12)
REQUEST Q BUS
TDMR + (4)
TDMG + (4)
SLAVE ADDRESS DECODE
SLAVE ADDRESS REGISTER
(4) BBS7 +
(7) DB12 +
(7) DB11 +
(7) DB09 +
(7) DB08 +
(6) DB07 +
(6) DB06 +
(6) DB05 +
(6) DB04 +
(7) DB10 +
(12) CP2 −
(4) RESET −
(6) DB03 +
(6) DB02 +
(6) DB01 +
(6) DB00 +
(11) XSDO −
(4) RSYNC +
(5) GTIRQ +
(4) BDIN +
(4) IAKI +
(12) CPG −
(4) BRPLY +
(3) MRQB +
(4) DMGI +
DO7 +
DO6 +
DO5 +
DO4 +
DO3 +
DO2 +
DO1 +
DO0 +
R22 100Ω
C7 100Pf
DISTRIBUTED LOGIC CORP.
LOGIC DIAGRAM,
SHT 2 OF 20
853027 B



DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 3 OF 20
		DRAWING NUMBER 853027 B

Q BUS CONTROL
DRIVER/RECEIVER



CONTROLLER RESET

NOTE: * 12 SYMBOL INDICATES PULL-UP(180Ω)/PULL-DOWN(390Ω) RESISTORS. NUMBER SHOWN IS PIN NUMBER USED IN PACK, LOCATION RP10.

DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
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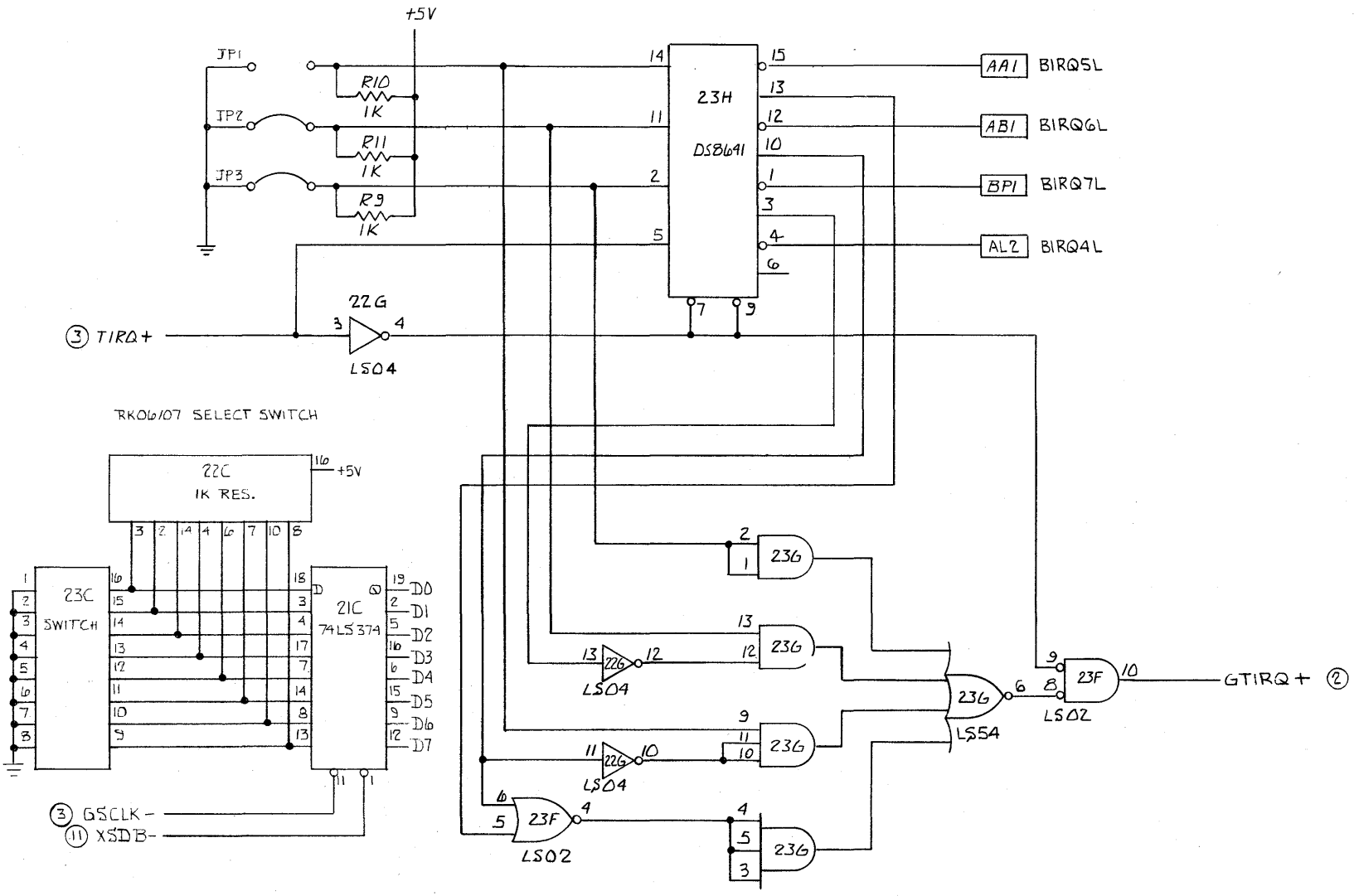
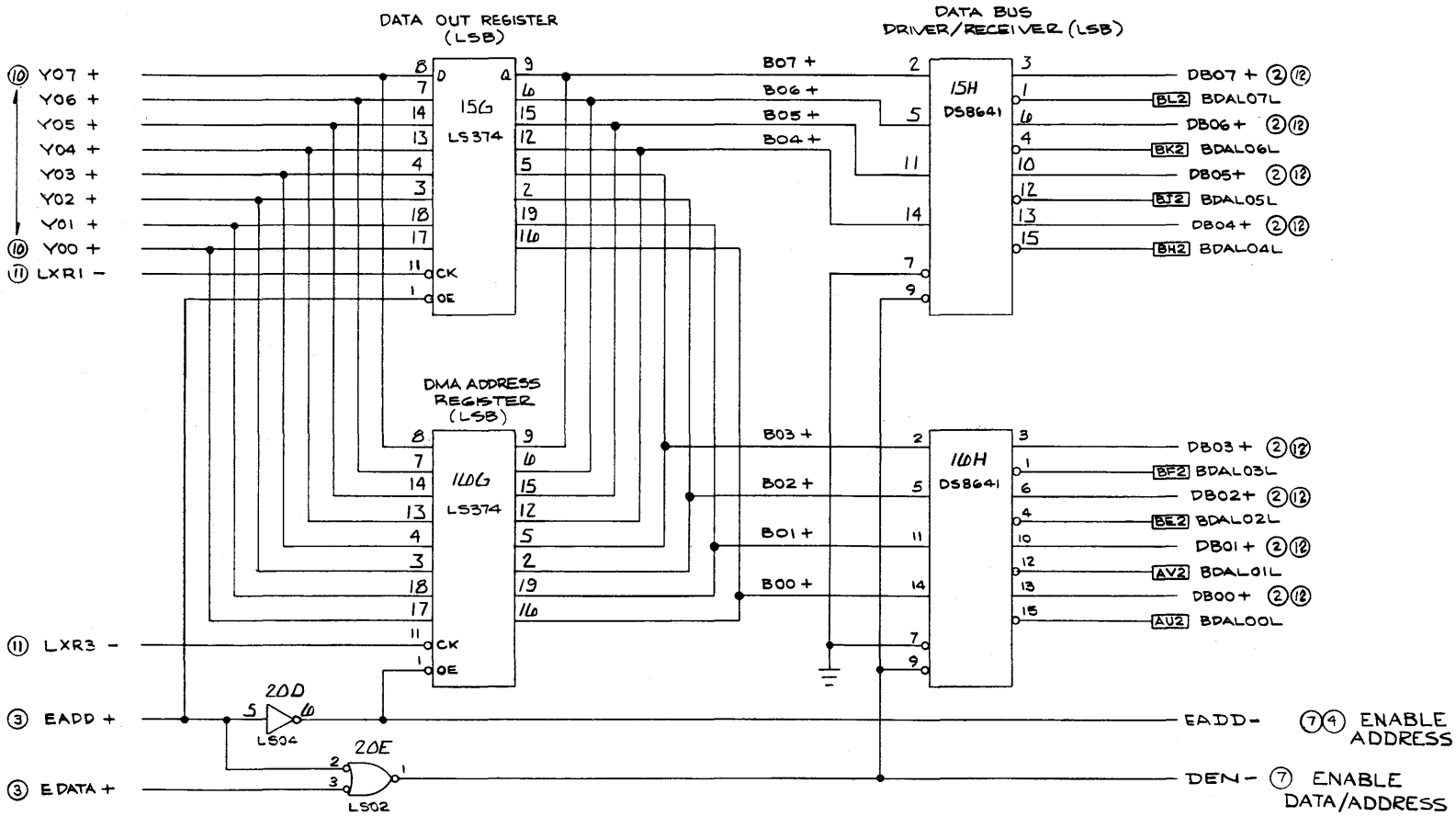
LOGIC DIAGRAM		SHT 4 OF 20
		DRAWING NUMBER 853027 B

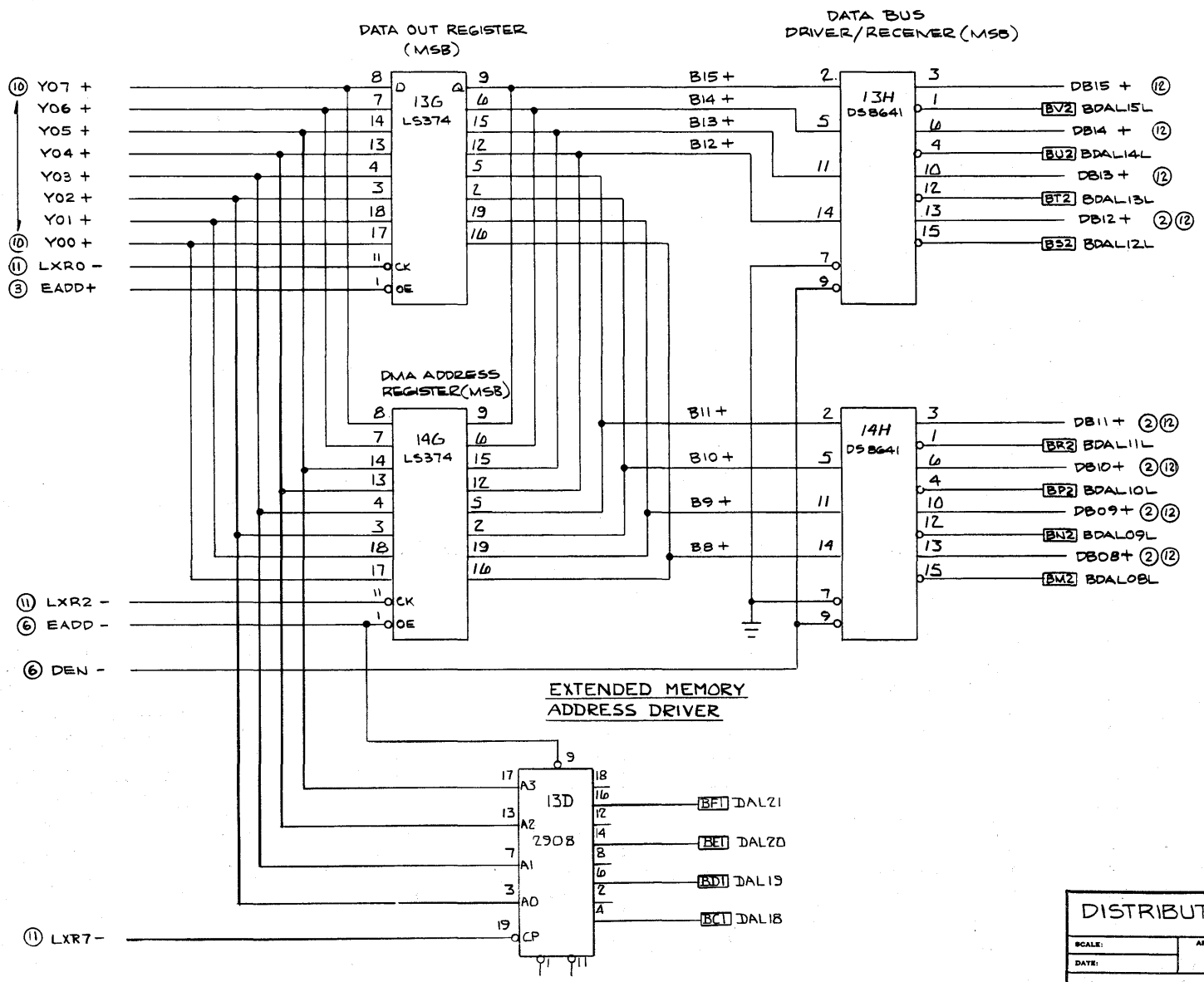
INTERRUPT LEVEL SELECT



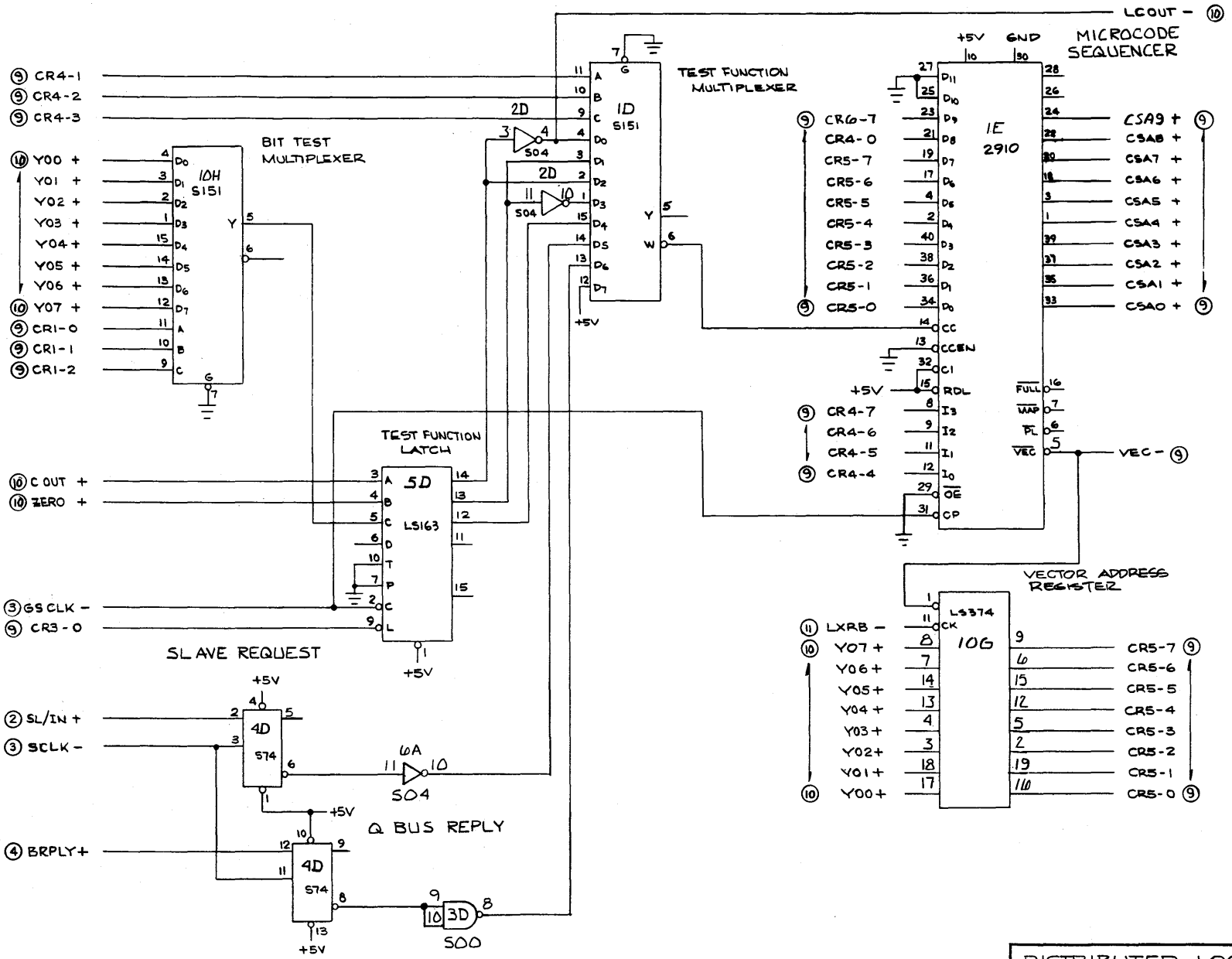
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 5 OF 20
		DRAWING NUMBER 853027 A



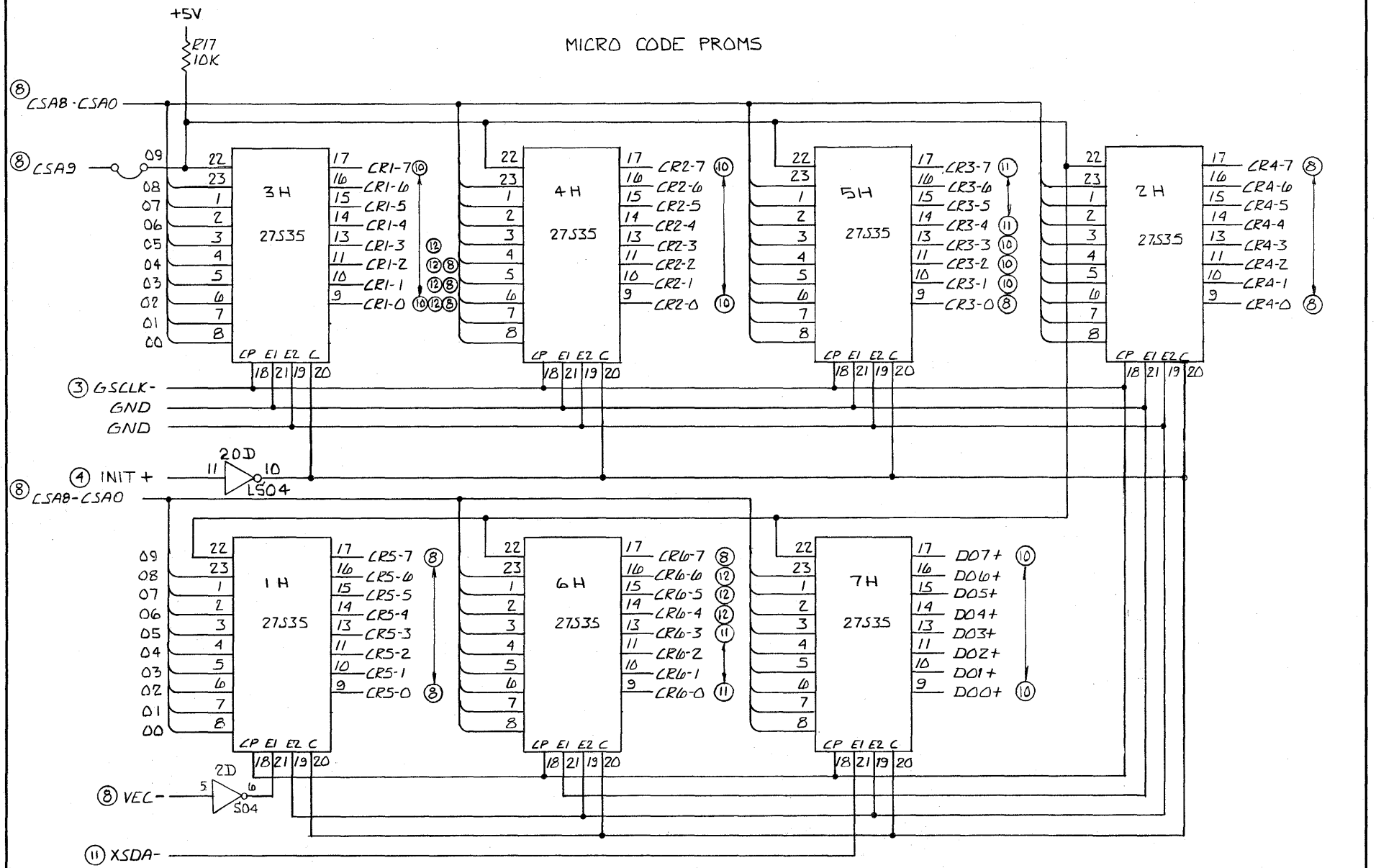
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E
DATE:		REVISED
LOGIC DIAGRAM,		SHT 6 OF 20
		DRAWING NUMBER 853027 A



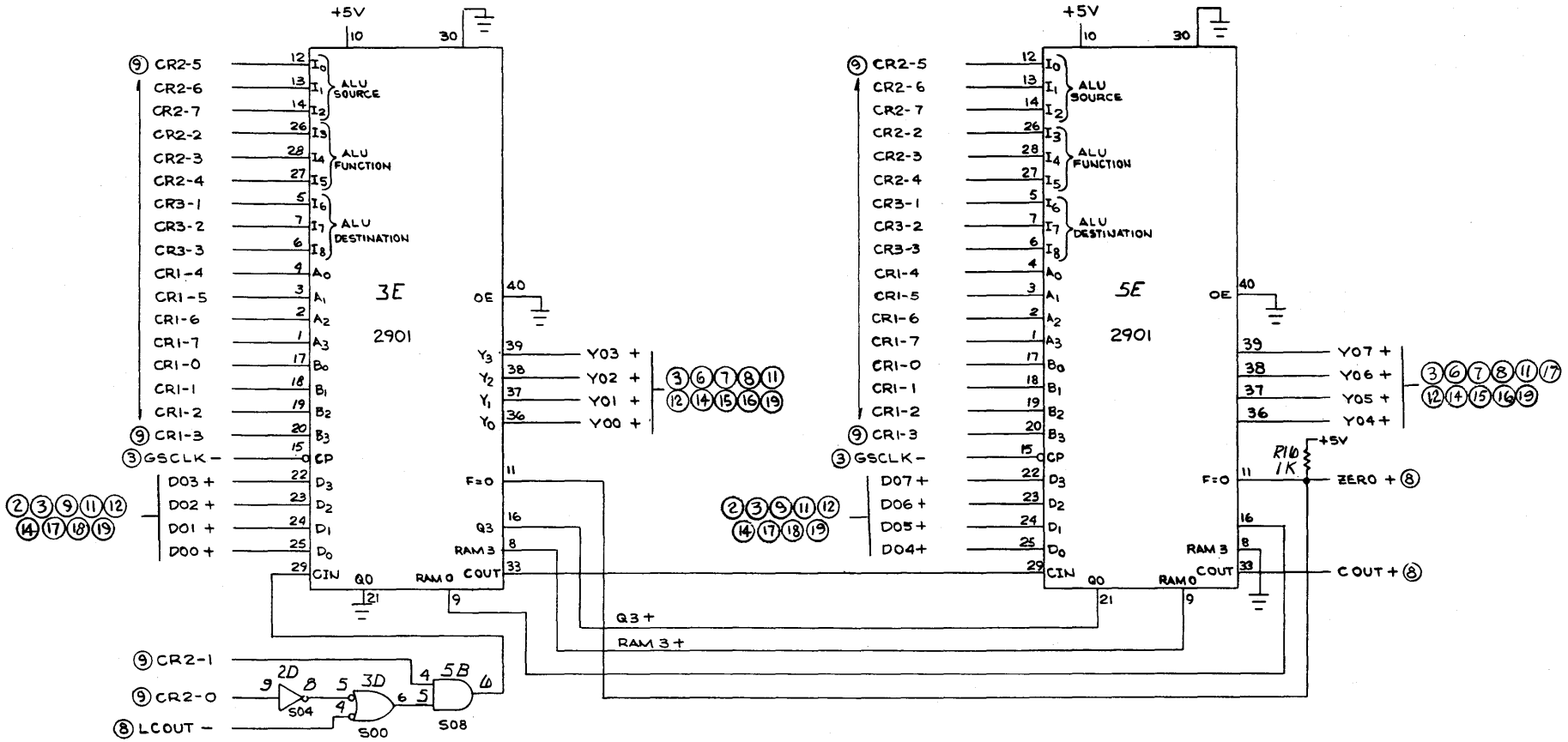
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 7 OF 20
		DRAWING NUMBER 853027 A



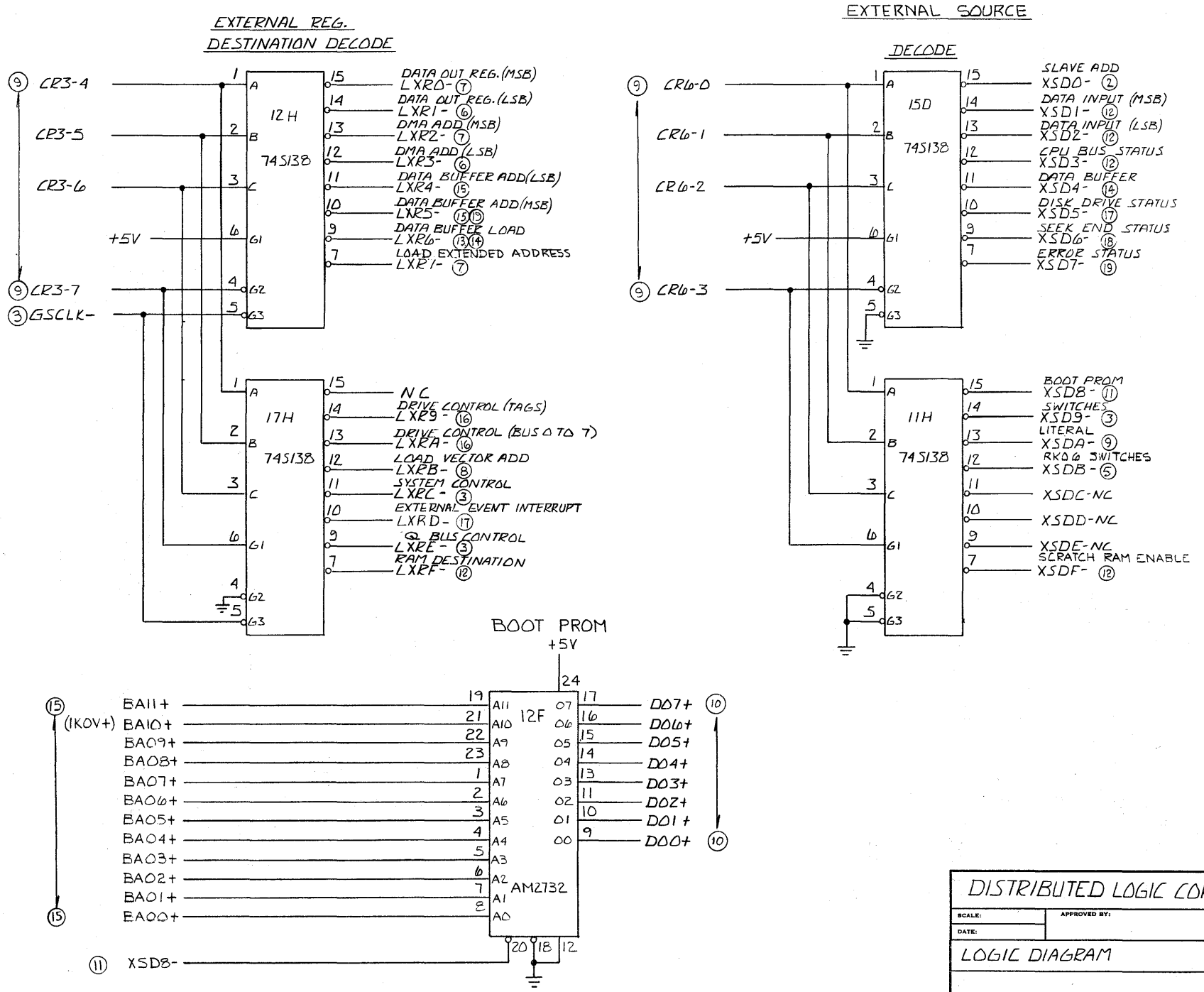
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R. E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 8 OF 20
		DRAWING NUMBER 853027 A



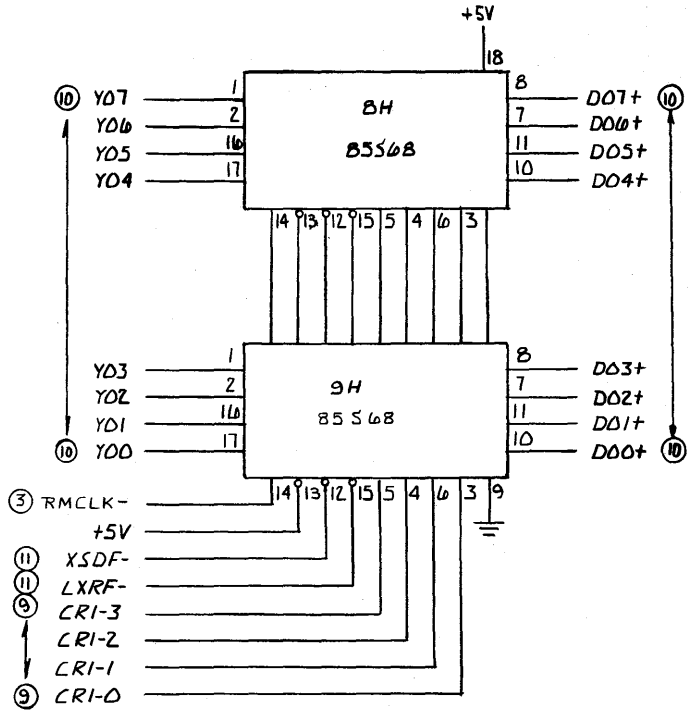
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 9 OF 20
		DRAWING NUMBER 853027 A



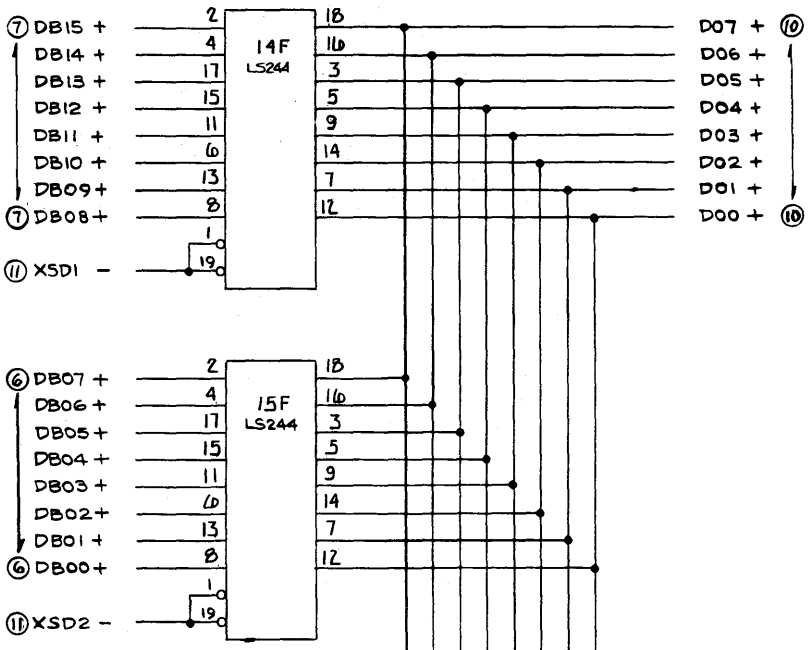
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY RE.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 10 OF 20
		DRAWING NUMBER 853027 B


EXTERNAL REG.
DESTINATION DECODE
12 H
74S138
CR3-4
CR3-5
CR3-6
+5V
CR3-7
GSCLK-
DATA OUT REG.(MSB) LXR0- (7)
DATA OUT REG.(LSB) LXR1- (6)
DMA ADD (MSB) LXR2- (7)
DMA ADD (LSB) LXR3- (6)
DATA BUFFER ADD(LSB) LXR4- (15)
DATA BUFFER ADD(MSB) LXR5- (15)(19)
DATA BUFFER LOAD LXR6- (13)(14)
LOAD EXTENDED ADDRESS LXR7- (7)
17H
74S138
NC
DRIVE CONTROL (TAGS) LXR9 - (16)
DRIVE CONTROL (BUS 0 TO 7) LXRA - (16)
LOAD VECTOR ADD LXRB- (8)
SYSTEM CONTROL LXRC - (3)
EXTERNAL EVENT INTERRUPT LXRD - (17)
Q BUS CONTROL LXRE - (3)
RAM DESTINATION LXRF- (12)
EXTERNAL SOURCE
DECODE
15D
74S138
CR6-0
CR6-1
CR6-2
+5V
CR6-3
SLAVE ADD XSD0- (2)
DATA INPUT (MSB) XSD1- (12)
DATA INPUT (LSB) XSD2- (12)
CPU BUS STATUS XSD3- (12)
DATA BUFFER XSD4- (14)
DISK DRIVE STATUS XSD5- (17)
SEEK END STATUS XSD6- (18)
ERROR STATUS XSD7- (19)
11H
74S138
BOOT PROM XSD8- (11)
SWITCHES XSD9- (3)
LITERAL XSDA- (9)
RK06 SWITCHES XSDB- (5)
XSDC-NC
XSDD-NC
XSDE-NC
SCRATCH RAM ENABLE XSDF- (12)
BOOT PROM
+5V
12F
AM2732
(15) (1K0V+) BA11+
BA10+
BA09+
BA08+
BA07+
BA06+
BA05+
BA04+
BA03+
BA02+
BA01+
BA00+ (15)
DO7+ (10)
DO6+
DO5+
DO4+
DO3+
DO2+
DO1+
DO0+ (10)
(11) XSD8-
DISTRIBUTED LOGIC CORP.
SCALE:
APPROVED BY:
DRAWN BY R.E.
DATE:
REVISED
LOGIC DIAGRAM
SHT 11 OF 20
DRAWING NUMBER
853027 B

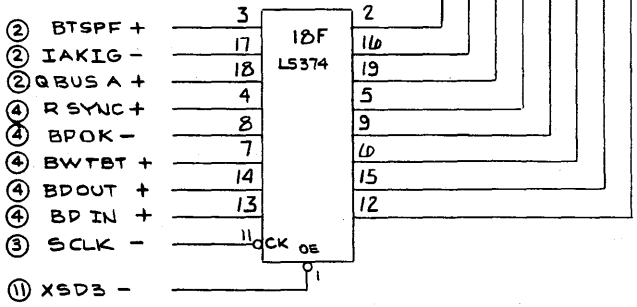
SCRATCH RAM



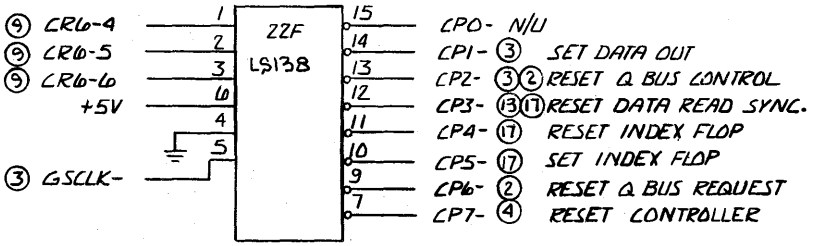
DATA INPUT MUX



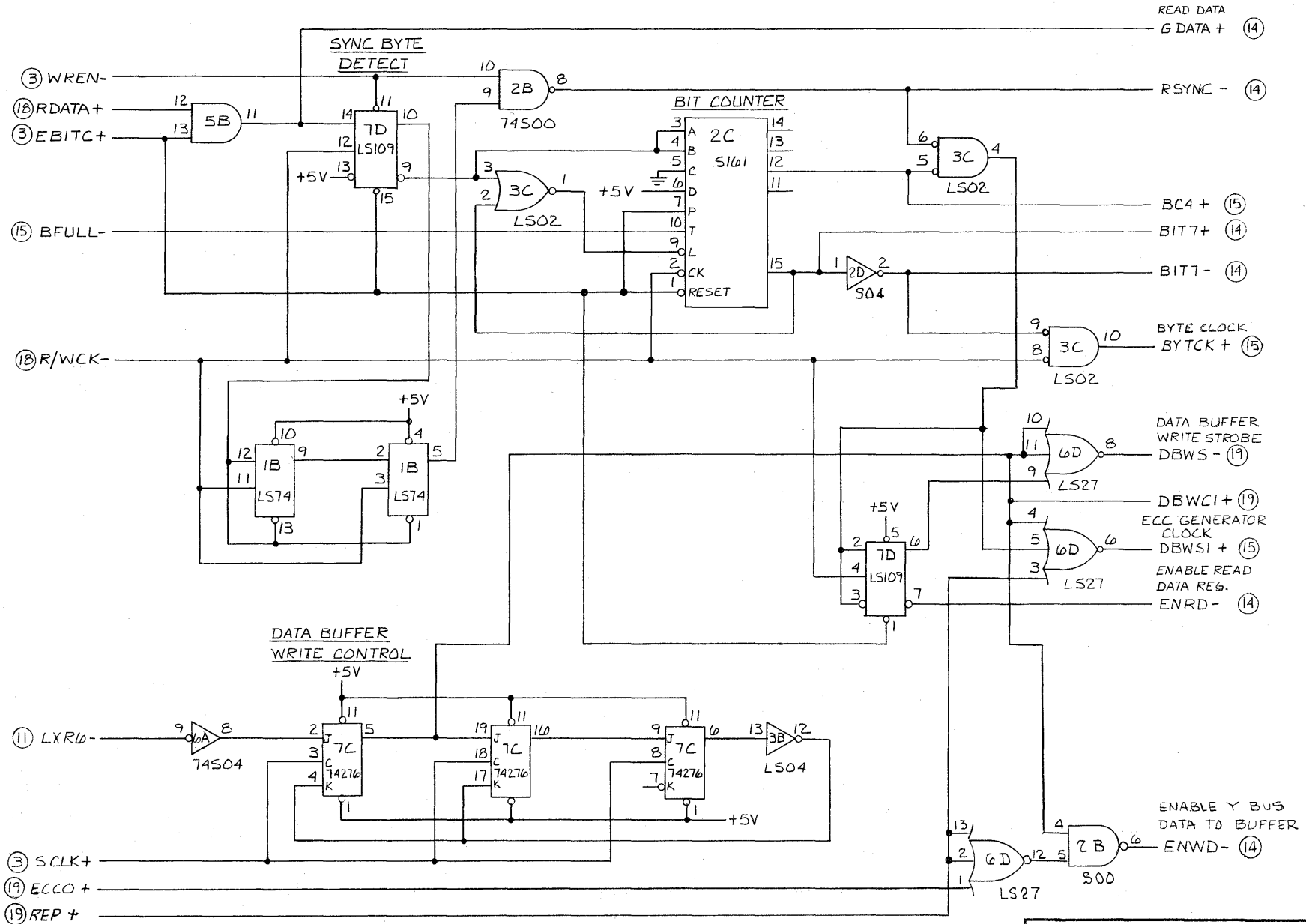
Q BUS STATUS REG.

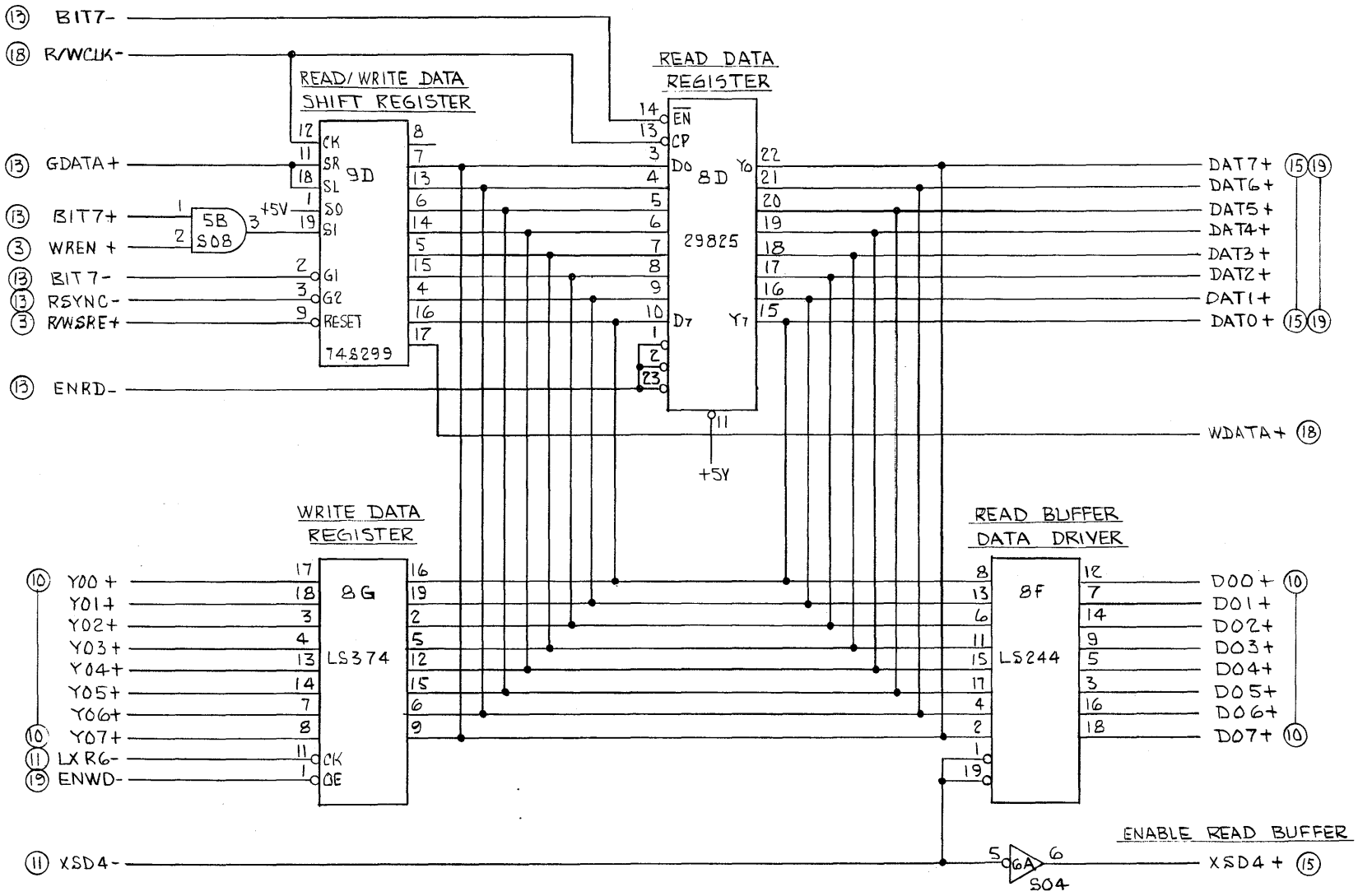


CONTROL PULSE DECODE

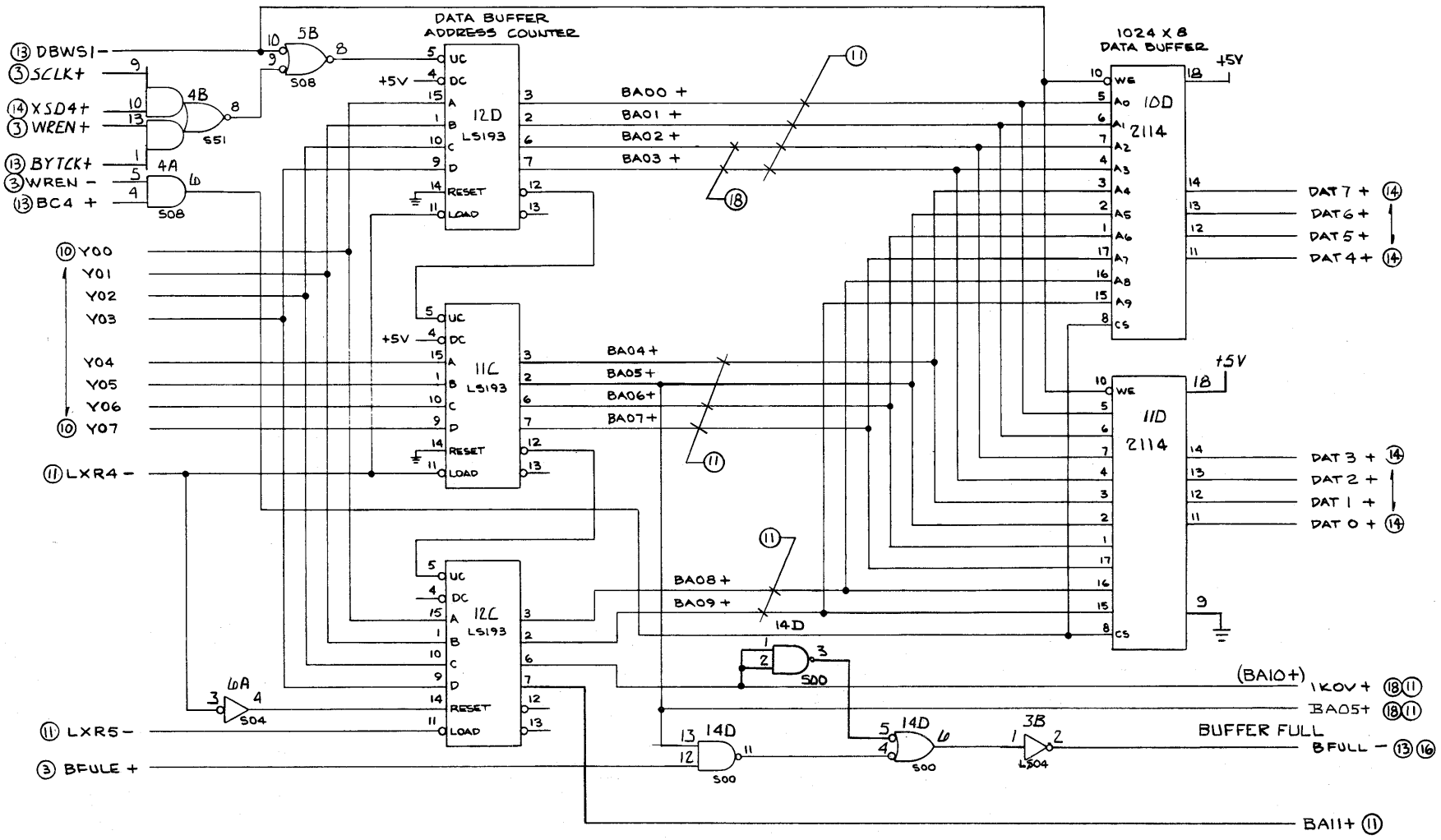


DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R.E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 12 OF 20
		DRAWING NUMBER 853027 A

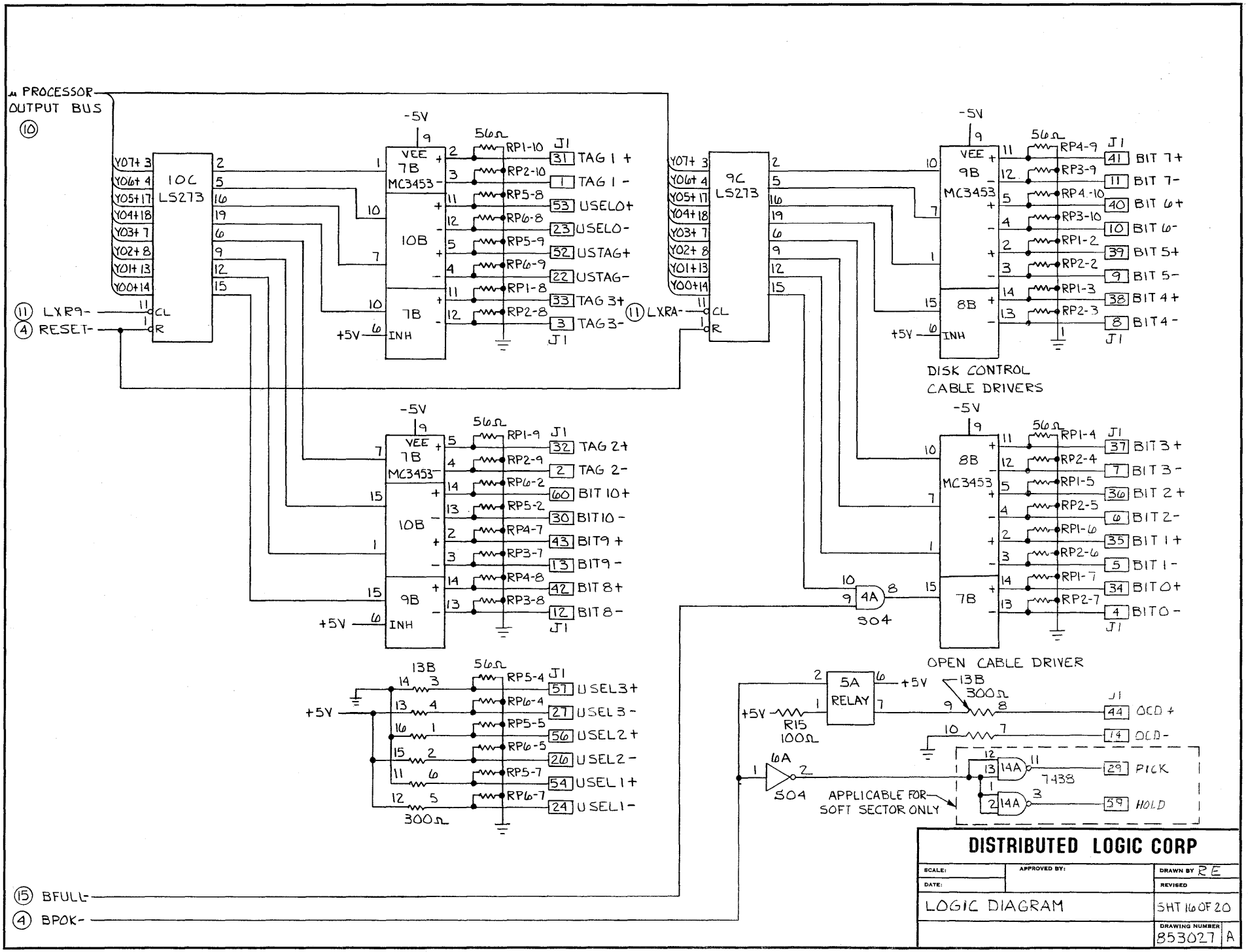

SYNC BYTE DETECT
BIT COUNTER
DATA BUFFER WRITE CONTROL
(3) WREN-
(18) RDATA+
(3) EBITC+
(15) BFULL-
(18) R/WCK-
(11) LXRW-
(3) SCLK+
(19) ECCO+
(19) REP+
5B
7D LS109
2B 74S00
3C LS02
2C S161
2D S04
6D LS27
1B LS74
6A 74S04
7C 74276
3B LS04
7B S00
+5V
READ DATA G DATA + (14)
RSYNC - (14)
BC4 + (15)
BIT7+ (14)
BIT7- (14)
BYTE CLOCK BYTCK + (15)
DATA BUFFER WRITE STROBE DBWS - (19)
DBWC1+ (19)
ECC GENERATOR CLOCK DBWS1 + (15)
ENABLE READ DATA REG. ENRD- (14)
ENABLE Y BUS DATA TO BUFFER ENWD- (14)
DISTRIBUTED LOGIC CORP
SCALE:
DATE:
APPROVED BY:
DRAWN BY RE
REVISED
LOGIC DIAGRAM
SHT 13 OF 20
DRAWING NUMBER 853027 D



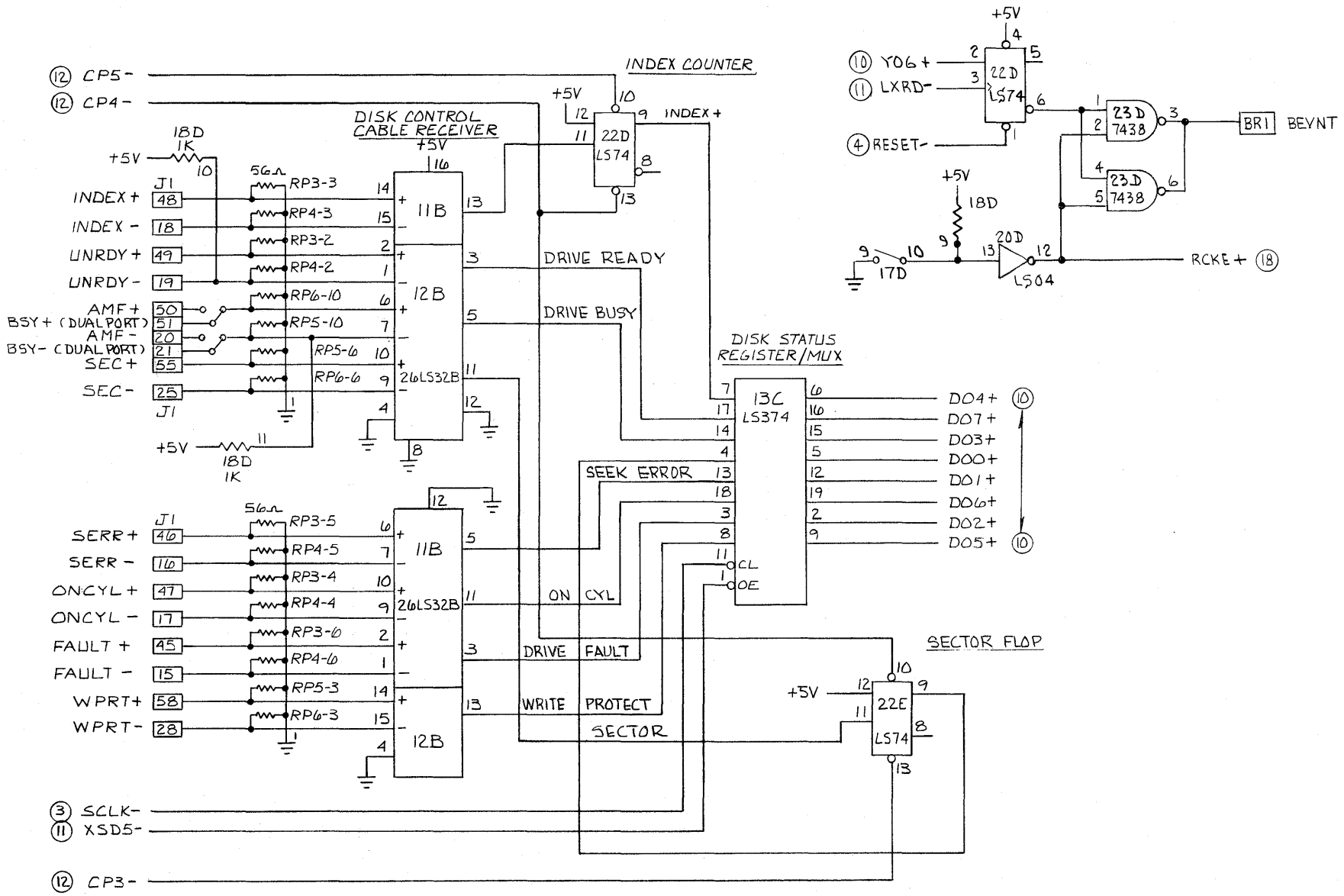
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY
DATE:		REVISED
LOGIC DIAGRAM		SHT 14 OF 20
		DRAWING NUMBER 853027 C



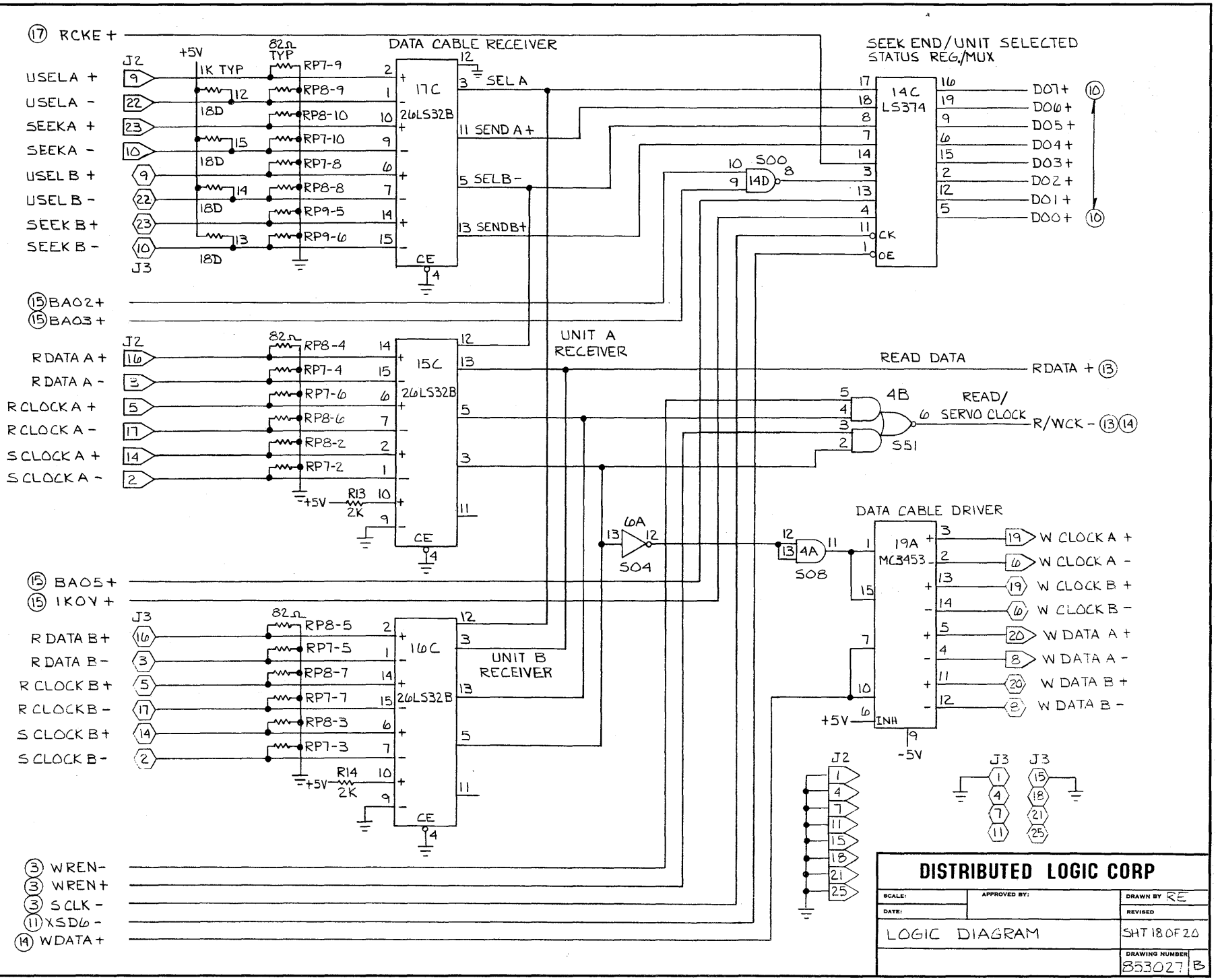
DISTRIBUTED LOGIC CORP.		
SCALE:	APPROVED BY:	DRAWN BY R. E.
DATE:		REVISED
LOGIC DIAGRAM,		SHT 15 OF 20
		DRAWING NUMBER 853027 A



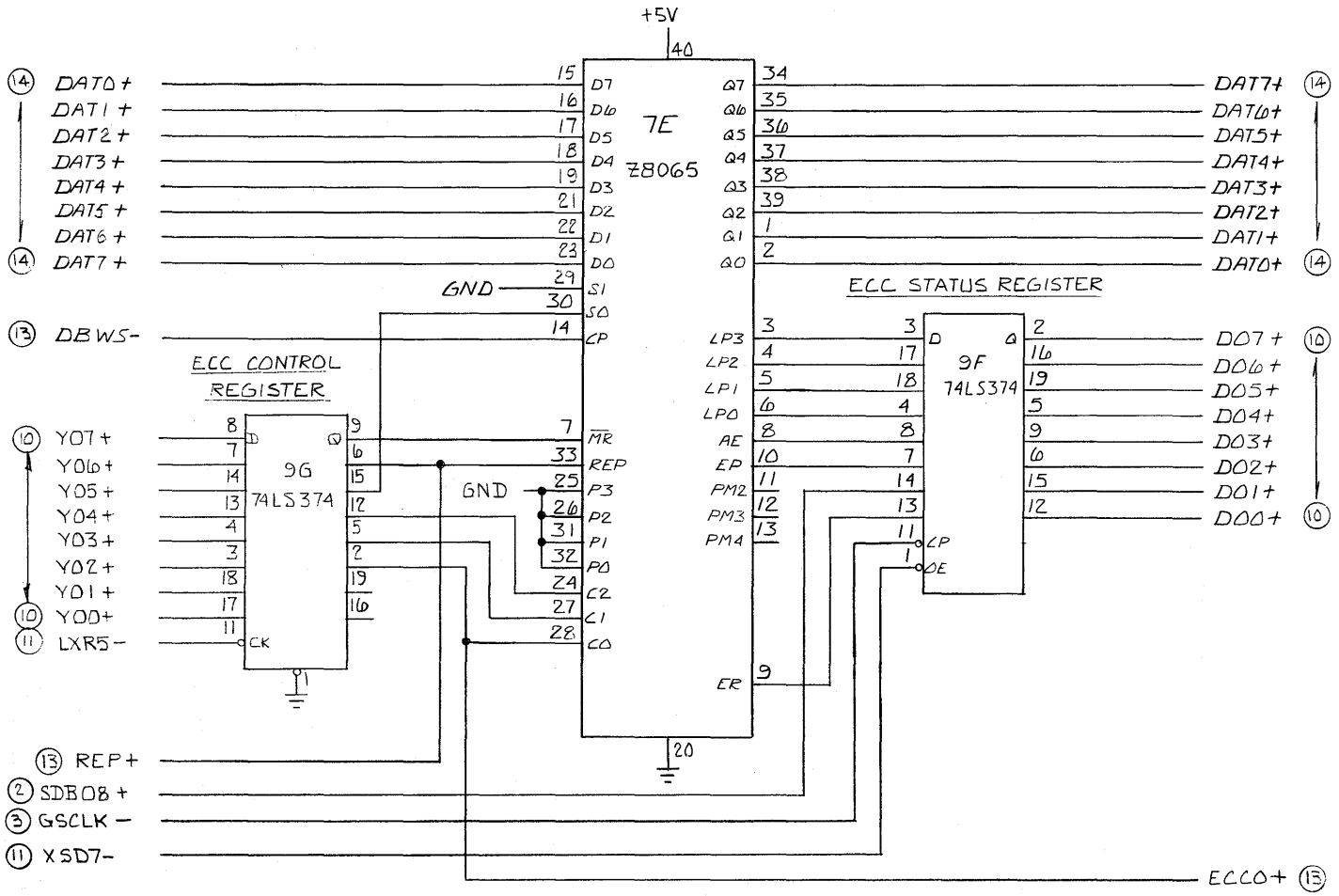
DISTRIBUTED LOGIC CORP		
SCALE:	APPROVED BY:	DRAWN BY RE
DATE:		REVISED
LOGIC DIAGRAM		SHT 16 OF 20
		DRAWING NUMBER 853027 A



DISTRIBUTED LOGIC CORP		
SCALE:	APPROVED BY:	DRAWN BY RE
DATE:		REVISED
LOGIC DIAGRAM		SHT 17 OF 20
		DRAWING NUMBER 853027 C


(17) RCKE +
DATA CABLE RECEIVER
SEEK END/UNIT SELECTED STATUS REG./MUX
USEL A +
USEL A -
SEEK A +
SEEK A -
USEL B +
USEL B -
SEEK B +
SEEK B -
J2
J3
+5V
1K TYP
82Ω TYP
RP7-9
RP8-9
RP8-10
RP7-10
RP7-8
RP8-8
RP9-5
RP9-6
17C
26LS32B
SEL A
SEND A +
SELB -
SENDB +
CE
14C
LS374
DO7 +
DO6 +
DO5 +
DO4 +
DO3 +
DO2 +
DO1 +
DO0 +
CK
OE
14D
S00
(15) BA02 +
(15) BA03 +
R DATA A +
R DATA A -
R CLOCK A +
R CLOCK A -
S CLOCK A +
S CLOCK A -
RP8-4
RP7-4
RP7-6
RP8-6
RP8-2
RP7-2
R13
2K
15C
UNIT A RECEIVER
READ DATA
RDATA + (13)
4B
S51
READ/ SERVO CLOCK
R/WCK - (13)(14)
(15) BA05 +
(15) IKOV +
R DATA B +
R DATA B -
R CLOCK B +
R CLOCK B -
S CLOCK B +
S CLOCK B -
RP8-5
RP7-5
RP8-7
RP7-7
RP8-3
RP7-3
R14
2K
16C
UNIT B RECEIVER
6A
S04
DATA CABLE DRIVER
4A
S08
19A
MC3453
INH
-5V
W CLOCK A +
W CLOCK A -
W CLOCK B +
W CLOCK B -
W DATA A +
W DATA A -
W DATA B +
W DATA B -
(3) WREN -
(3) WREN +
(3) S CLK -
(11) XSD6 -
(14) WDATA +
DISTRIBUTED LOGIC CORP
SCALE:
APPROVED BY:
DRAWN BY RE
DATE:
REVISED
LOGIC DIAGRAM
SHT 18 OF 20
DRAWING NUMBER
853027 B

ECC GENERATOR



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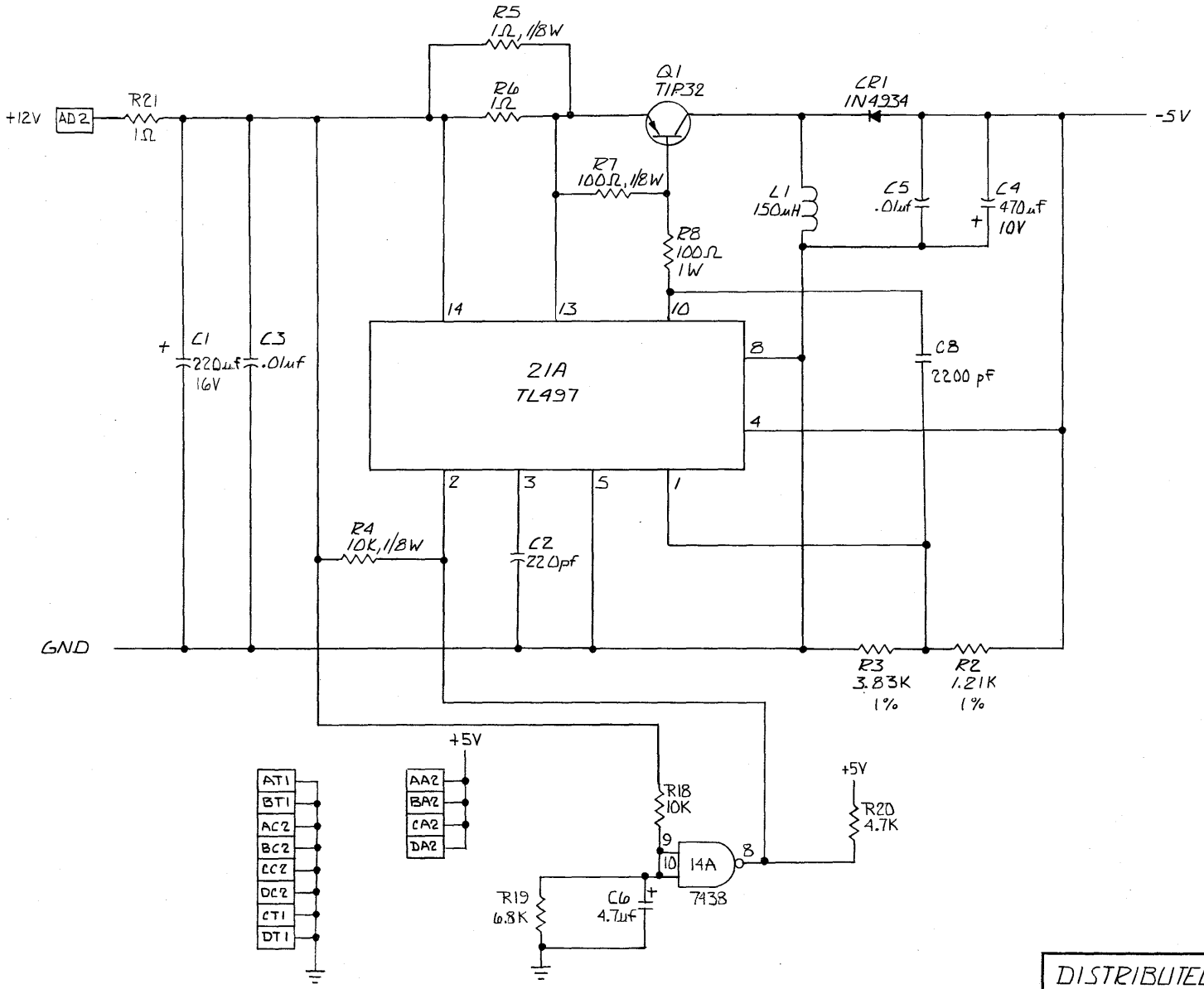
SCALE:	APPROVED BY:	DRAWN BY R. E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 19 OF 20
		DRAWING NUMBER 853027 B

+12V TO -5V POWER SUPPLY



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SCALE:	APPROVED BY:	DRAWN BY R. E.
DATE:		REVISED
LOGIC DIAGRAM		SHT 20 OF 20
		DRAWING NUMBER 853027 B

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