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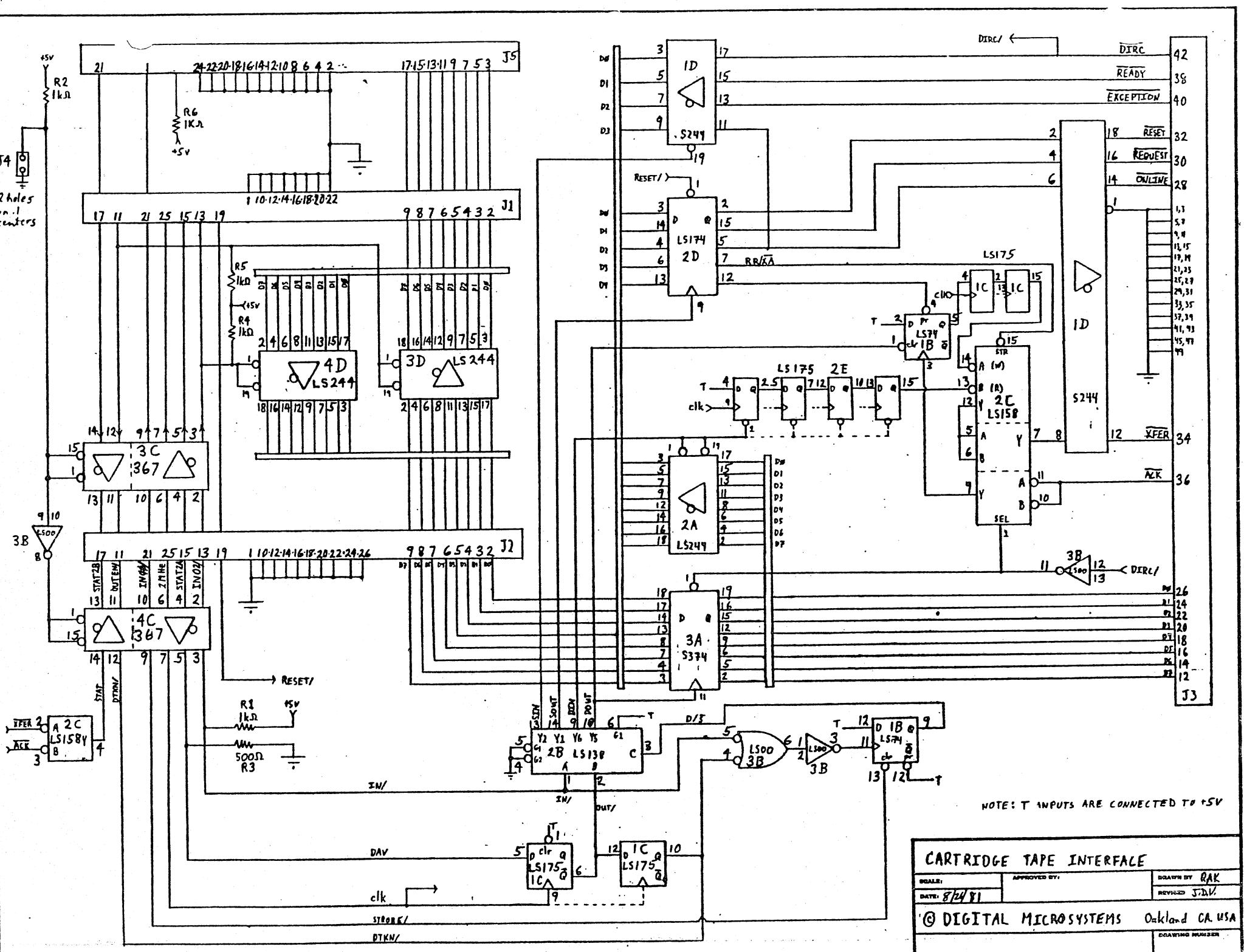
SCALE: _____ APPROVED BY: _____ DRAWN BY: J.D.V.

DATE: 7/27/81 _____ REVISED: _____

128K Byte Multibus Memory

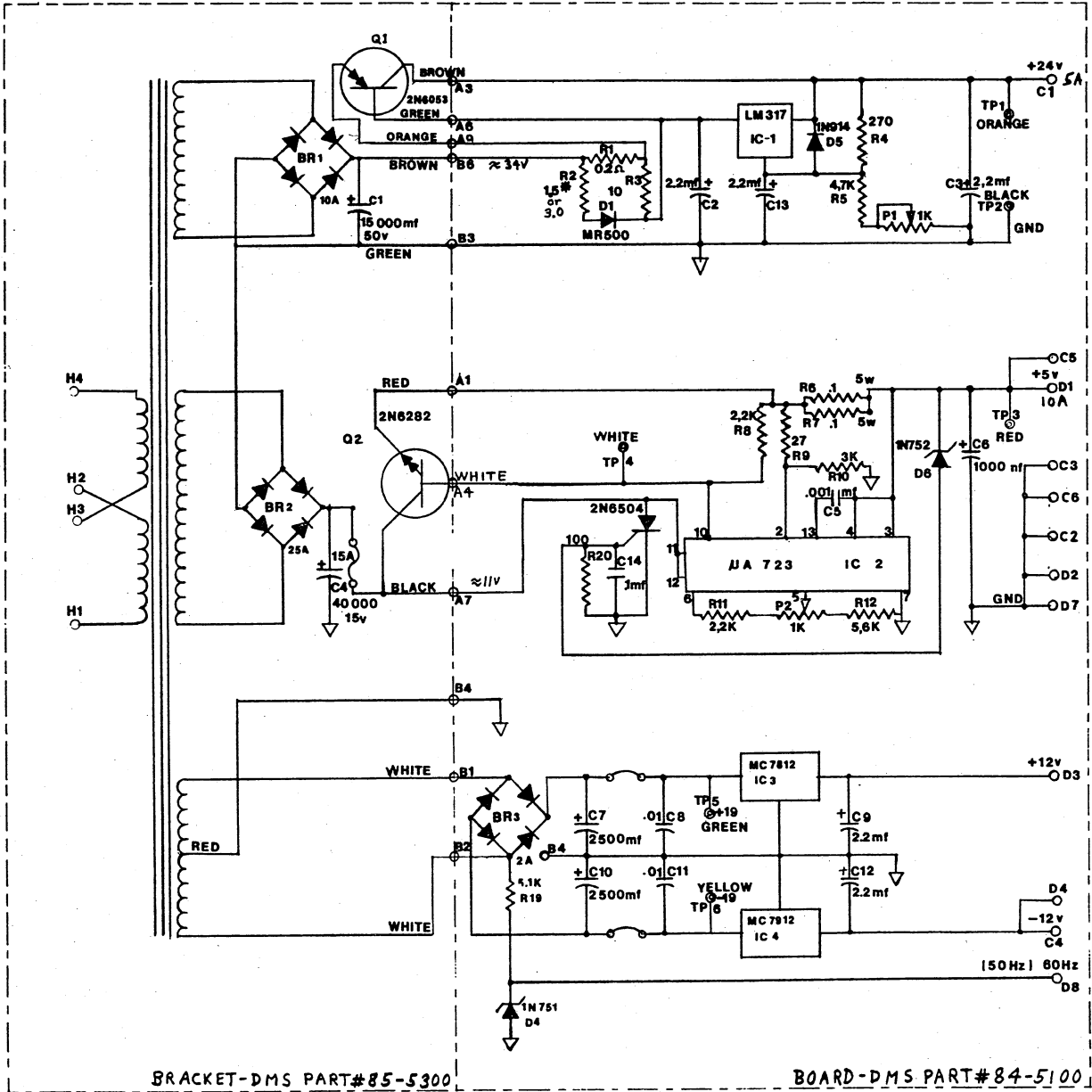
4163 Piedmont Ave., Oakland

DRAWING NUMBER: 1 of 1



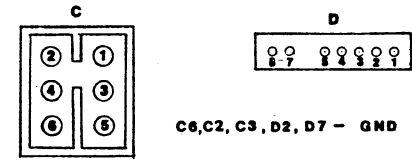
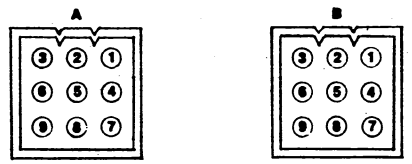
NOTE: T INPUTS ARE CONNECTED TO +5V

CARTRIDGE TAPE INTERFACE		
SCALE:	APPROVED BY:	DRAWN BY RAK
DATE: 8/24/81		REVISED J.D.V.
© DIGITAL MICROSYSTEMS Oakland, CA, USA		DRAWING NUMBER

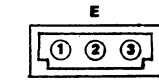


BRACKET-DMS PART#85-5300

BOARD-DMS PART#84-5100



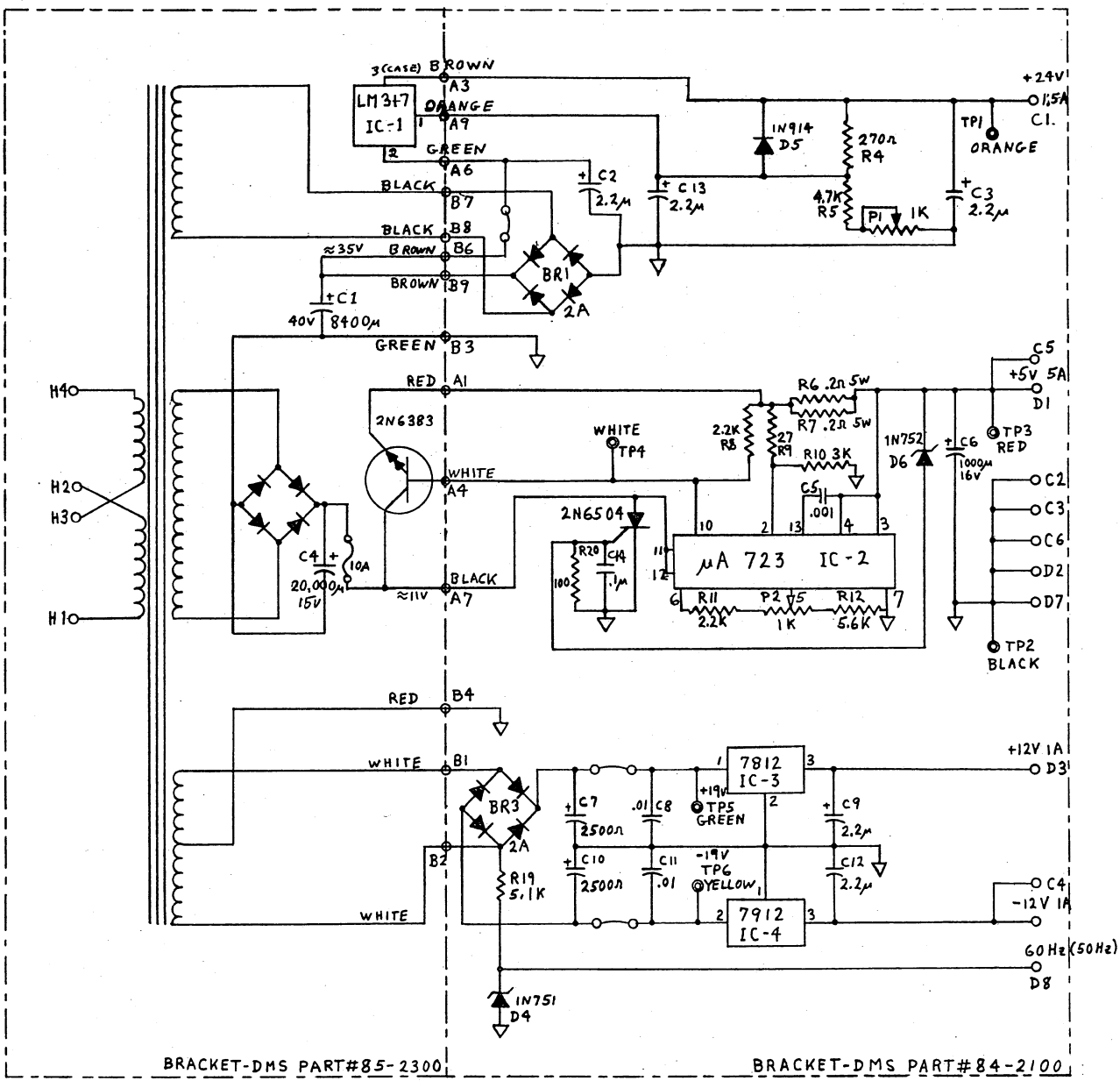
C6, C2, C3, D2, D7 - GND



NOTES:

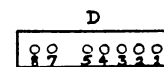
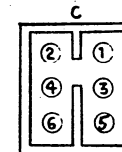
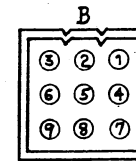
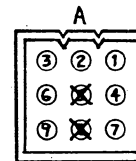
- FOR 115VAC OPERATION
 - H1 & H3 CONNECTED TO E1
 - H2 & H4 CONNECTED TO E3
- FOR 230VAC OPERATION
 - H1 CONNECTED TO E1
 - H4 CONNECTED TO E3
 - H2 CONNECTED TO H3
- *FOR HDS R2 IS 1.5Ω
- FOR HDO R2 IS 3.0Ω

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SCALE: None	APPROVED BY:	DRAWN BY Lev
DATE: 1/28/81		REVISED 9.0
HARD DISK POWER SUPPLY		
		DRAWING NUMBER 1 of 1

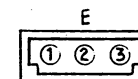


BRACKET-DMS PART#85-2300

BRACKET-DMS PART#84-2100



C2,C3,C6,D2,D7-GND

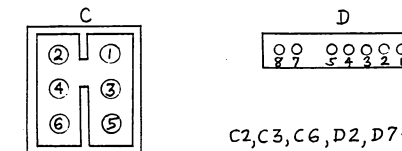
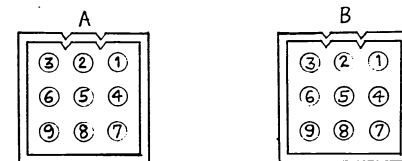
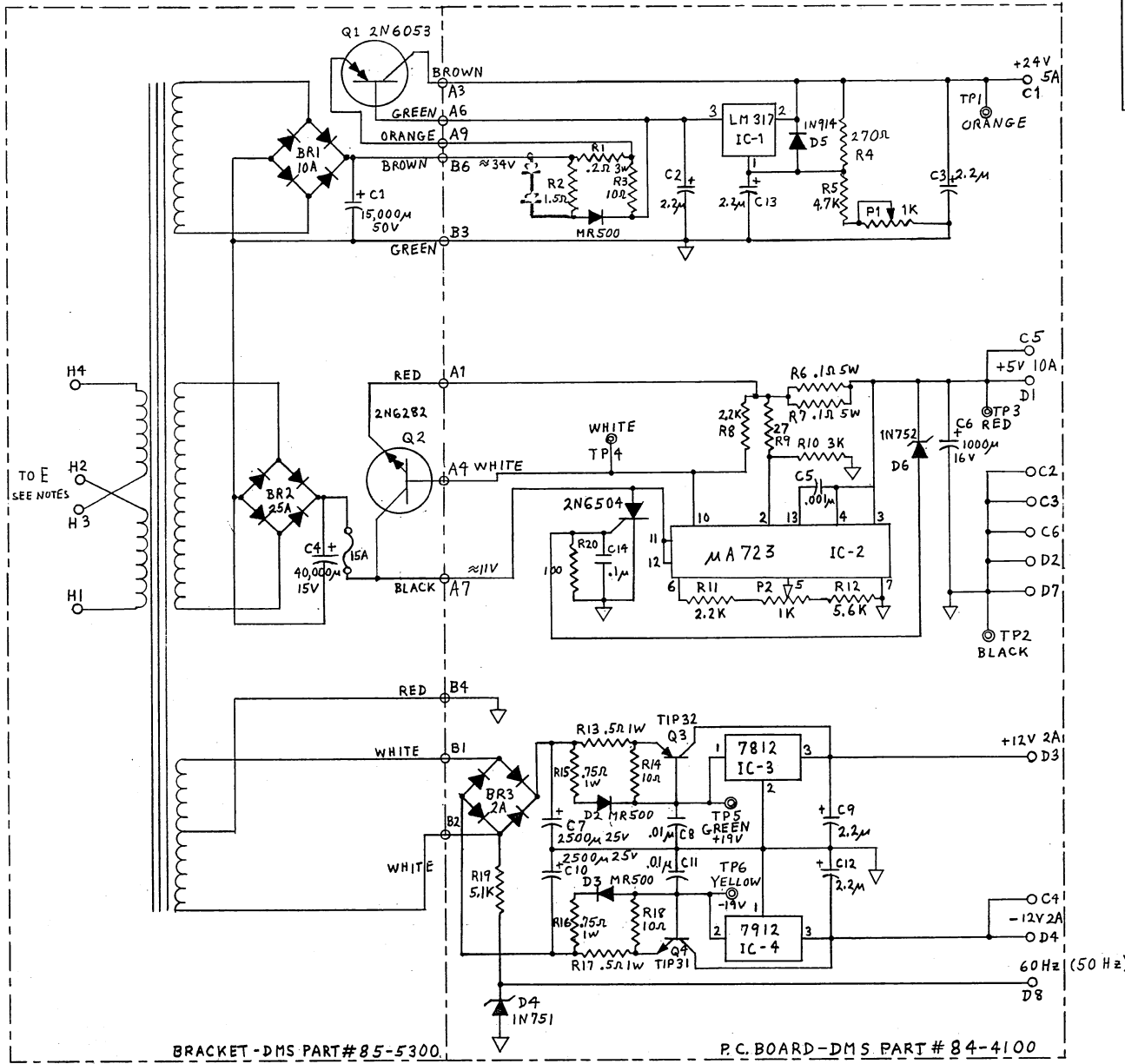


NOTES:

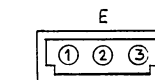
- FOR 115VAC OPERATION
 - H1 & H3 CONNECTED TO E1
 - H2 & H4 CONNECTED TO E3
- FOR 230VAC OPERATION
 - H1 CONNECTED TO E1
 - H4 CONNECTED TO E3
 - H2 CONNECTED TO H3

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SCALE: 1:0 R/C	APPROVED BY:	DRAWN BY LCV
DATE: 10/17/80		REVISED JLB
DSC 2/3 POWER SUPPLY		
DRAWING NUMBER		1 of 1

PS2.2 P.C. Board



C2, C3, C6, D2, D7 - GND



NOTES:

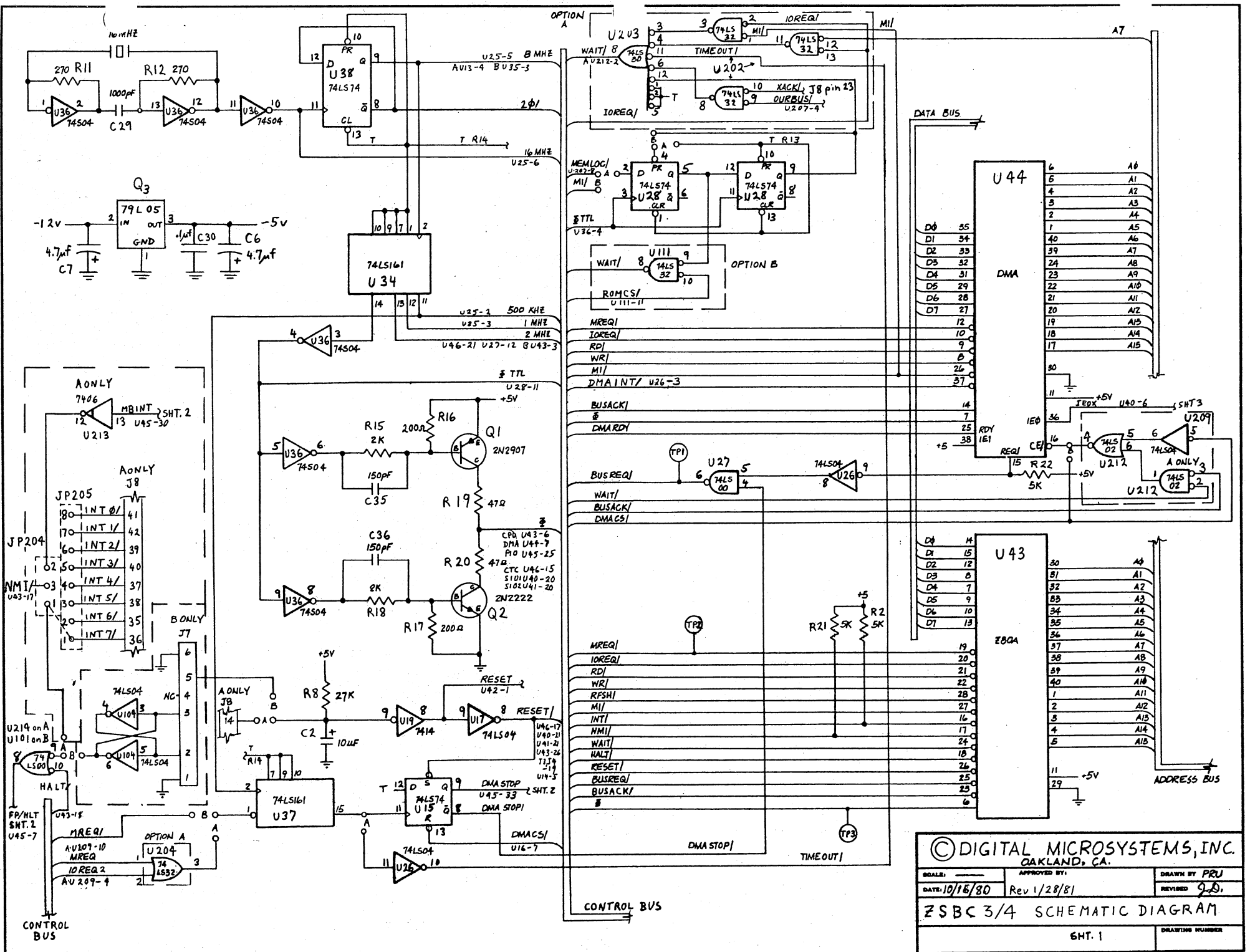
FOR 115VAC OPERATION
 H1 & H3 CONNECTED TO E1
 H2 & H4 CONNECTED TO E3

FOR 230VAC OPERATION
 H1 CONNECTED TO E1
 H4 CONNECTED TO E3
 H2 CONNECTED TO H3

2/9/81

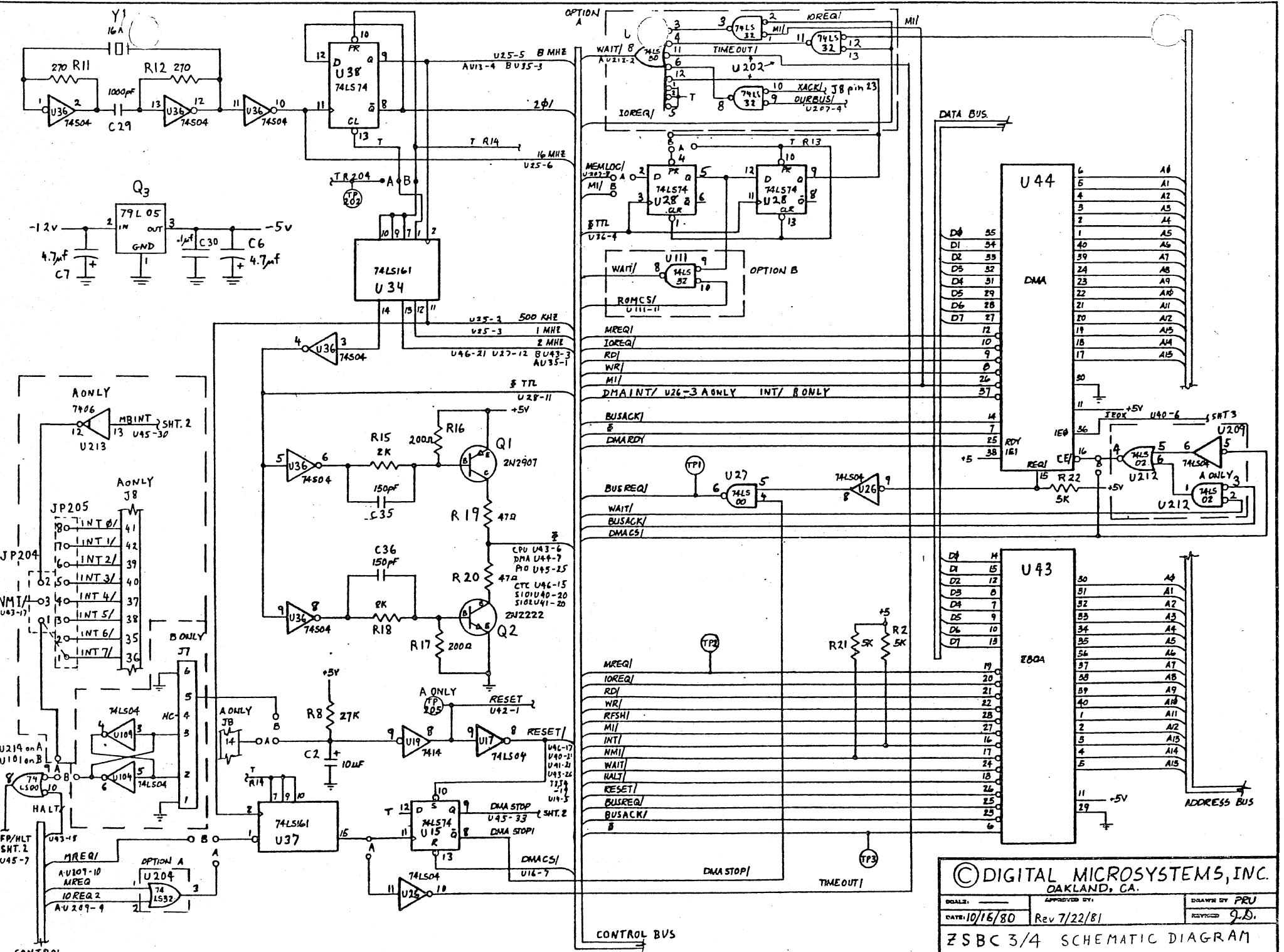
2 MR500 diodes added
 in parallel with 1.5Ω
 resistor - Provides current
 limit protection for +24V

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SCALE: N/A	APPROVED BY:	DRAWN BY Lev
DATE: 10/17/80		REVISED 9.8
DSC4 POWER SUPPLY		
		DRAWING NUMBER 1 of 1

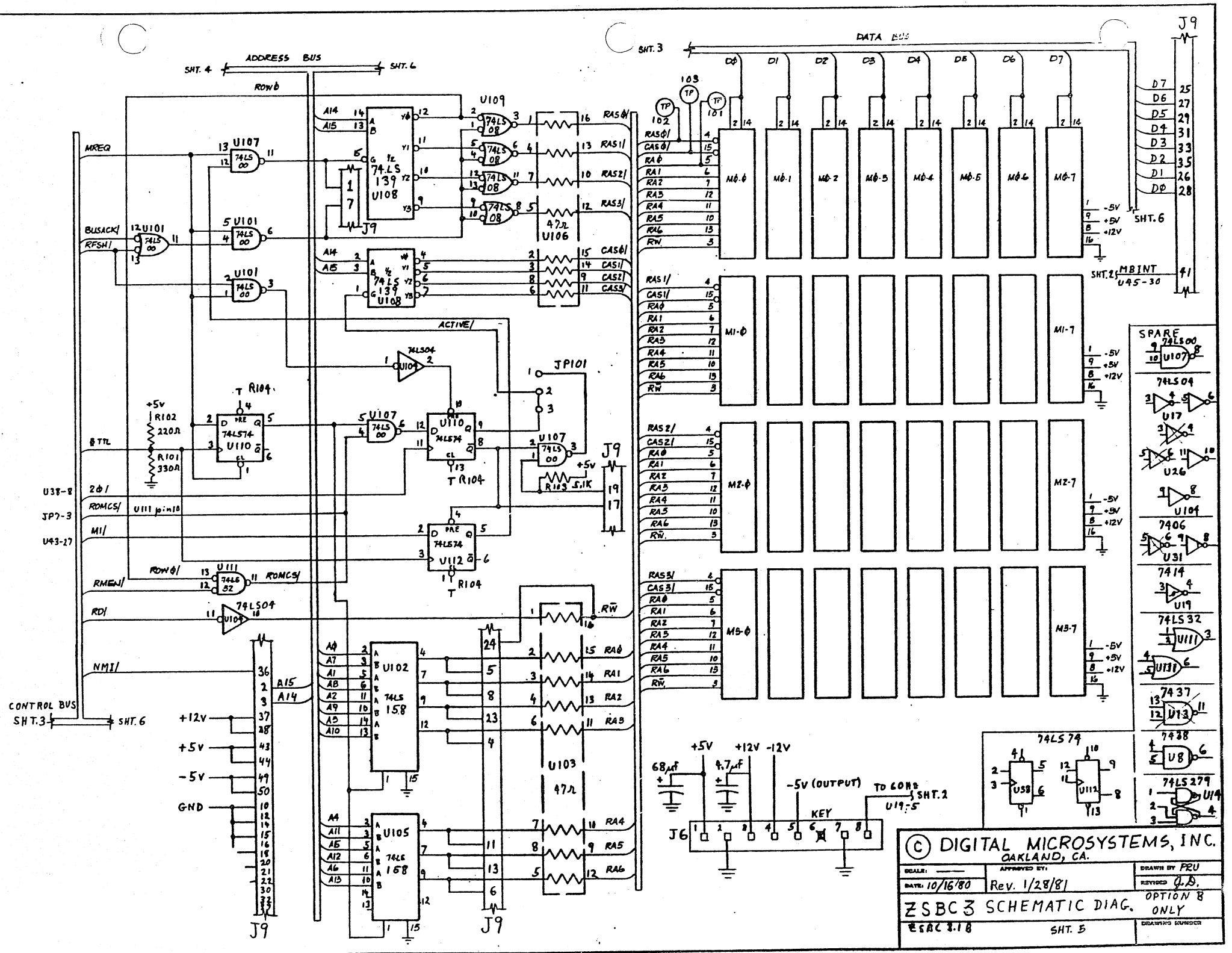


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SCALE: _____	APPROVED BY: _____	DRAWN BY: PRU
DATE: 10/16/80	Rev: 1/28/81	REVISED: 2/81
ZSBC 3/4 SCHEMATIC DIAGRAM		
SHT. 1		DRAWING NUMBER

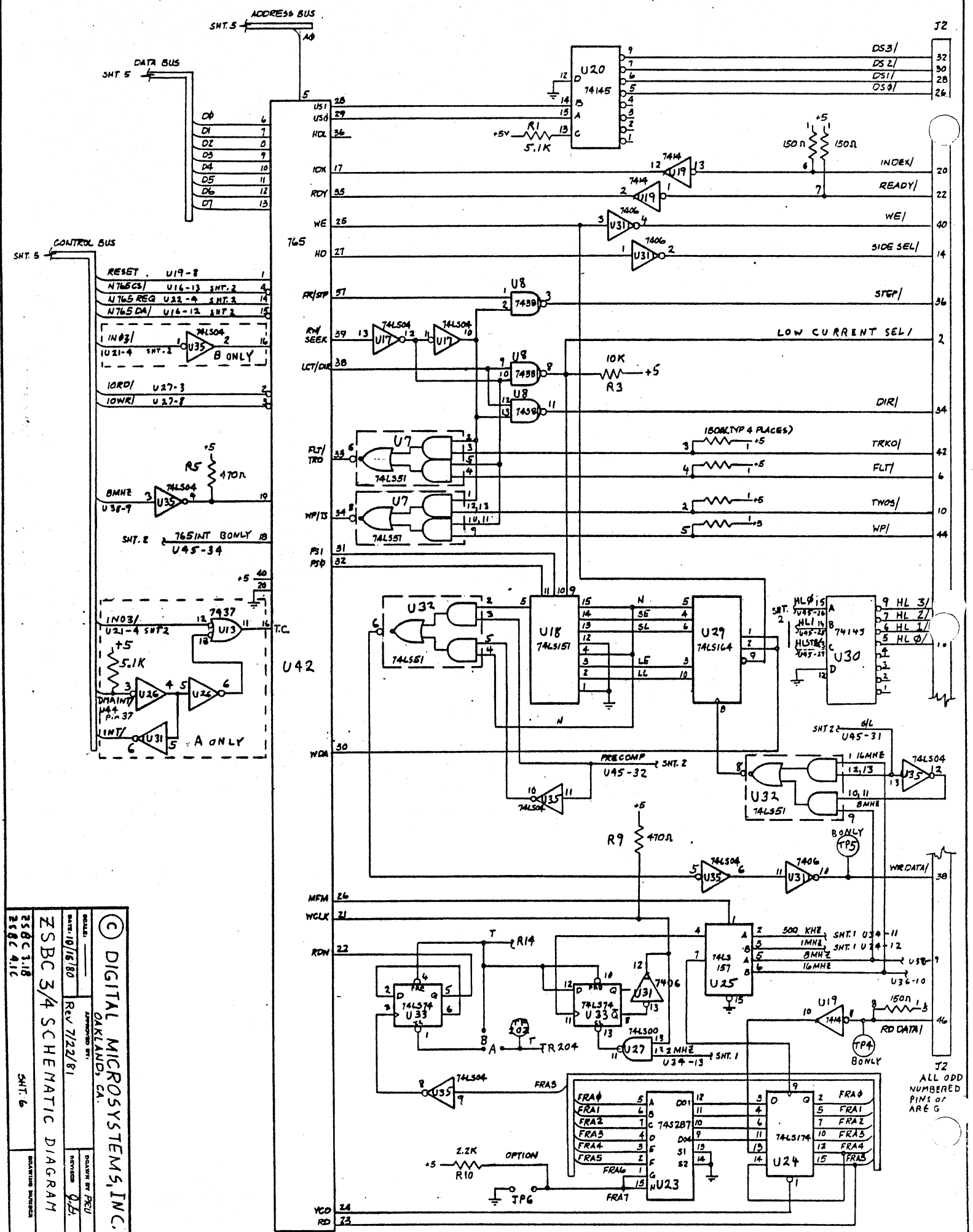


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 OAKLAND, CA.
 DATE: 10/16/80 Rev 7/22/81
 DRAWN BY PRU
 REVISED J.D.
ZSBC 3/4 SCHEMATIC DIAGRAM
 ZSBC 3.1B 6HT.1
 ZSBC 4.1C DRAWING SUBJECT



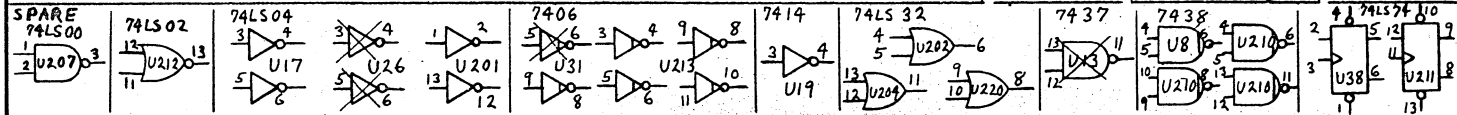
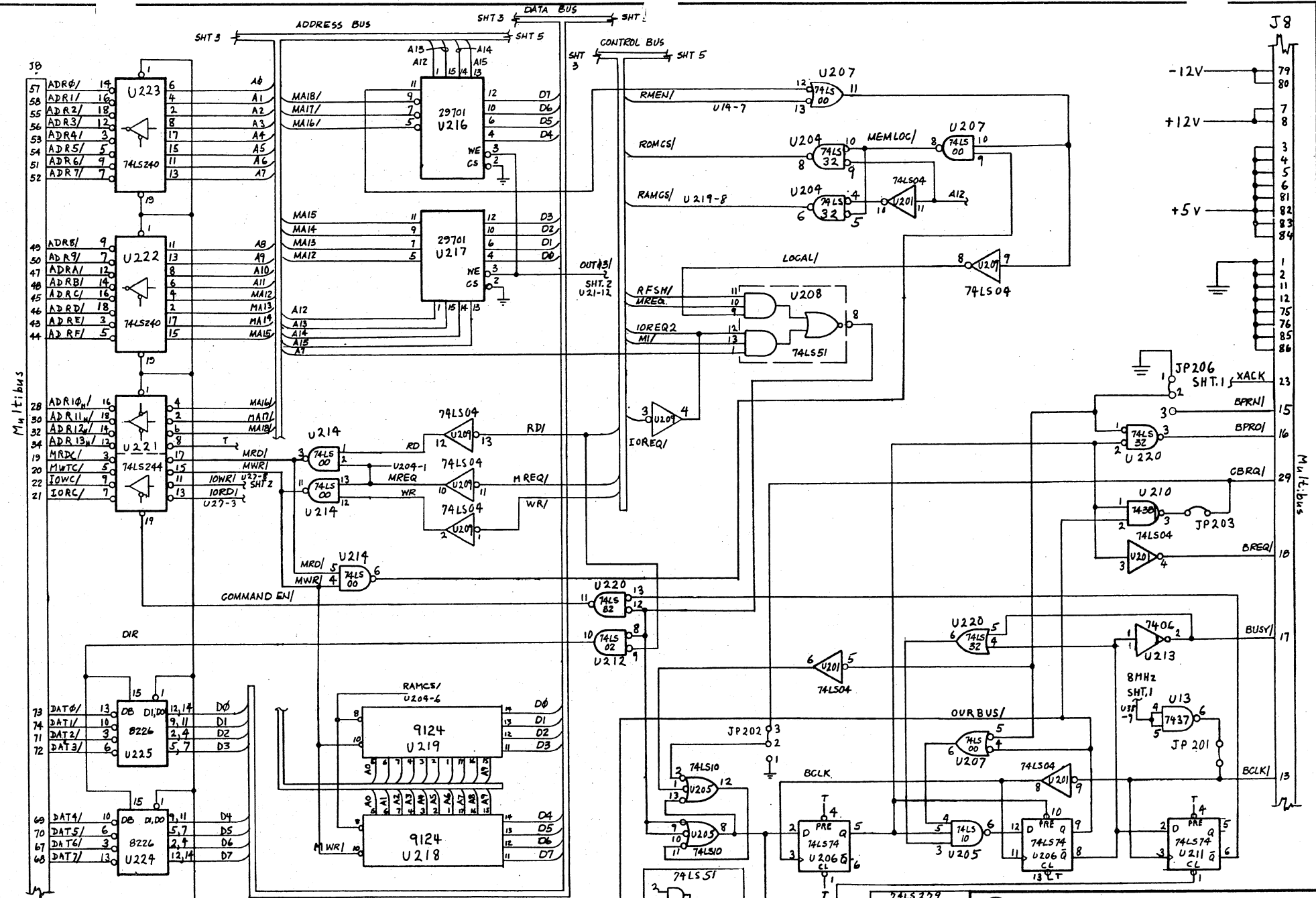
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OAKLAND, CA.

SCALE: _____ APPROVED BY: _____ DRAWN BY: PRU
 DATE: 10/16/80 Rev. 1/28/81 REVISED: J.S.
Z80C3 SCHEMATIC DIAG. ONLY OPTION 8
 85AC 3.18 SHT. 5 DRAWING NUMBER



250C 3.1B
 250C 4.1C
 SMT. 6
 REVISED BY: JEB
 DATE: 7/22/81
 DATE: 10/16/80
 DRAWN BY: JEB
 APPROVED BY: JEB
 OAKLAND, CA.
 DIGITAL MICROSYSTEMS, INC.
 ZSBC 3/4 SCHEMATIC DIAGRAM

J2 ALL ODD
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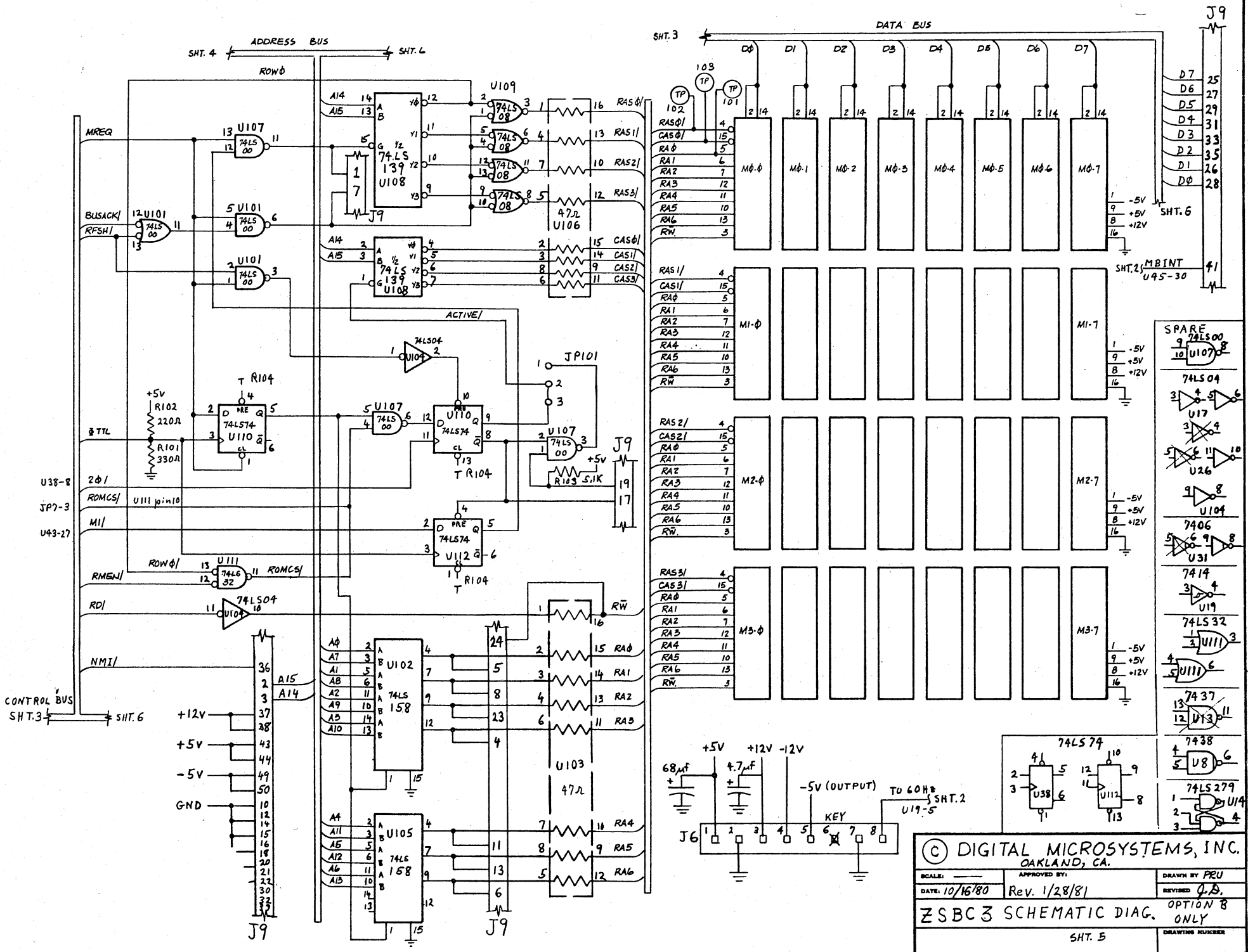


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SCALE: _____ APPROVED BY: _____
DATE: 10/16/80 Rev 1/28/81

ZSBC 4 SCHEMATIC DIAG. ONLY

DRAWN BY: PEU
REVISED: J.S.
OPTION A
DRAWING NUMBER: SHT. 4



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SCALE: _____	APPROVED BY: _____	DRAWN BY: PRU
DATE: 10/16/80	Rev. 1/28/81	REVISION: Q.S.
Z8BC3 SCHEMATIC DIAG. ONLY		OPTION B
SHT. 5		DRAWING NUMBER

