DIGI-DATA CORPORATION
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TECHNICAL INFORMATION MANUAL

PDP-11 DIRECT MEMORY ACCESS INTERFACE FOR SYNCHRONOUS TAPE TRANSPORT

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1.0 INTRODUCTION

The PDP-11 Interface is designed to provide plug to plug compatible read-write magnetic tape drives for the PDP-11 family of computers. Figure 1 shows a maximum system configuration.

Either one each, or two NRZI or PE formatters may be connected to the CU (control unit). Each formatter can handle a mixture of 7 track and 9 track transports with speeds from 12.5 to 45 ips. Since a single formatter can handle drives with two different speeds, up to four different speed drives may be operated by the system. The system writes and reads IBM compatible tapes.

Programming the interface is very simple as the instruction set is identical to that of the TM11/TU10 manufactured by Digital Equipment Corporation. Thus most software developed for the TM11/TU10 system is compatible with this system. The CU is initially set up under program control. Data transfers between the CU and processor are under hardware control, and occur at the maximum processor rate. Once an operation has started software intervention is not required until it is completed, at which time an interrupt is generated that causes a service routine to become active.

1.1 OPTIONS

In addition to the basic system, Digi-Data has the following options available:

1.1.1 Erase

A variable length erase feature for erasing a record.

1.1.2 Read Threshold

Three threshold levels are available with this option. They are 1) high, 2) normal, and 3) low.

The high threshold is used to sense that a signal was written at sufficient level. The low threshold is used to recover signals that have deteriorated to within 5% of the nominal value.

1.1.3. Edit

Allows a single record of a multi-record tape to be changed.

1.1 OPTIONS (Cont.)

The PDP-11 interface is housed in a rack-mountable box, 19" wide by 5-1/4" high and 20" deep. A cable is provided to connect the interface to the tape transport; cabling from mini-computer to interface can be furnished by Digital Equipment Corporation. A connector block, mounted to the interface box, allows for connection of additional peripheral devices.

2.0 ELECTRICAL INTERFACE

The CU conforms to all electrical interface specifications for the 1100, 1600 and 1700 series tape transports, and for the PDP-11 unibus.

3.0 LOGIC LEVELS

3.1 CU Internal

1 = true = 2.5 to +5.5 volts

0 = false = 0.0 to 0.4 volts

3.2 CU To Unibus

1 = true = 0.0 to 0.4 volts

0 = false = 2.5 to 5.5 volts

3.3 CU to Formatter

1 = true = 0.0 to 0.4 volts

0 = false = 2.5 to 5.5 volts

4.0 GENERAL DESCRIPTION

The basic system is capable of performing eight different operations, they are: (1), Off line (2), Read (3), Write (4), Write EOF (5), Space Forward (6), Space Reverse (7), Write with Extended Gap and (8), Rewind. For all these functions, interrupts are generated that cause the processor to enter the support program.

In the read operation tape data is stored in memory. In write and write with extended gap core data is written on tape. The CU formats the data for all data transfers.

4.1 OFF LINE - An off line command causes the tape unit to rewind to the BOT marker and go off line. The unit goes off line immediately after starting to rewind. When a unit is off line it can only be reactivated by operator intervention at the tape unit control panel.

4.0 GENERAL DESCRIPTION (Cont.)

4.2 READ - A read command causes the tape unit to read one record and stop, unless given a new command at the end of the record. The CU may transfer all or only a portion of a record to processor memory, i.e., first 30 characters of a 100 character record.

4.3 WRITE - A write command causes the tape unit to write a pre-determined number of characters, that are stored in processor memory, and stop. This constitutes one record.

4.4 WRITE EOF - A write EOF command causes the tape unit to write the EOF record and then stop.

4.5 SPACE FORWARD - A space forward command causes the tape unit to space a given number of records and then stop. Data is not transferred to the processor in this mode. At the end of each record the CU checks to see if the correct number of records have been spaced. If not the CU commands the tape unit to continue reading until the correct number of records have been spaced.

4.6 SPACE REVERSE - Space reverse is the same as space forward except that the tape unit is in the reverse mode.

4.7 WRITE WITH EXTENDED GAP - A write with extended gap command causes the tape unit to erase a section of tape before beginning the write operation. After a pre-determined number of characters have been written, the tape unit stops.

4.8 REWIND - A rewind command causes the tape unit to rewind to the BOT marker on the tape. The CU will accept a command while the selected tape unit is rewinding. After the rewind sequence is completed the CU will cause the tape unit to execute the stored command.

4.9 INTERRUPT - If the interrupt bit is set (MTC Bit 6) all tape operations will cause an interrupt to be generated. For rewind and off line commands the interrupt is generated at the start of the operation. For all other commands the interrupt is generated at the conclusion of an operation. In addition a second interrupt will be generated at the end of a rewind operation if the unit remains selected and in the rewind mode.

4.0 GENERAL DESCRIPTION (Cont.)

4.10 DATA - A tape data word consists of either 6 bits or 8 bits referred to as a tape character. For a nine track unit 8 bits constitute a tape character. For a 7 track unit 6 bits constitute a tape character. A processor data word is a 16 bit word that consists of two 8 bit bytes. Bits 0 - 7 make up the low byte, and bits 8 - 15 the high byte.

Data transfers between the processor and the CU may be either bytes or words. When the CU is controlling the transfer (write or read a record) it limits byte transfers to the first and/or last transfer. All other transfers are word transfers.

A nine track tape unit utilizes all memory bits. A seven track unit in normal operation does not use memory bits 6, 7, 14 and 15. In a tape write operation the unused bits are not altered when the CU accesses memory. In a tape read operation the unused bits are set to zero when the CU accesses memory. A core dump operation can occur only with a seven track unit. Core dump utilizes all 16 bits of a word. In a tape read operation 4 characters are read to make up one data word. The 4 LSB from each character are used. In a tape write operation 4 characters are written onto the 4 LSB data tracks for each data word. The unused tracks are written as zeros.

5.0 UNIBUS

All communications between PDP-11 system components is accomplished by a single high speed bus called the UNIBUS. A complete description of the UNIBUS is contained in the Digital Equipment Corporation PDP-11 Peripherals and Interfacing Handbook. The theory is given in Part II Chapter 2. Communication between the PDP-11 and the Digi-Data tape system is through the CU (Tape Control Unit).

The UNIBUS is a single, common path that connects the processor, memory and all peripherals. Address, data and control information is transmitted along the 56 lines of the bus. Figure 2 is a simplified block diagram of the PDP-11 system and the UNIBUS.

The form of communication is the same for every device on the unibus. All devices are connected in parallel including the processor. The bidirectional nature of 51 signal lines permit signals to flow in either direction. The remaining 5 unidirectional

5.0 UNIBUS (Cont.)

lines are used for priority bus control. Table 2 lists the signals used in a data transfer.

5.1.0 BUS MASTER

Bus master is a term applied to the device that is in control of the bus. Any device connected to the bus has the potential to become bus master if it is supplied with the proper hardware. A device becomes bus master through use of the bus request lines and the priority control lines. A device generally becomes bus master for one of two purposes: a) to make a non-processor transfer of data directly to or from memory, or b) to interrupt program execution, and force the processor to branch to a specific address where an interrupt service routine is located.

5.2.0 ADDRESS

Every device connected to the UNIBUS has at least one unique address assigned to it. Devices respond to UNIBUS signals only when they recognize their address. When a device recognizes its address it then responds as commanded by the bus master. The bus master supplies the address of the device it wishes to communicate with, and indicates the function to be performed, by use of the control lines C0 and C1.

5.3.0 DATA TRANSFERS

A bus master is capable of commanding two basic types of data transfers:

a. DAT0 where data is transferred from master to the selected slave or,

b. DAT1 where data is transferred from the selected slave to the master.

Two other types of data transfers are possible, but are not used in this system and will not be discussed here.

6.0 CONTROL UNIT

The CU is a programmable device that causes the functions described in 4.0 to be executed under hardware control.

After the CU is programmed and given a go command it will execute the software commanded operation until it is completed or an error occurs. In either case it will generate an interrupt that causes the service routine to become active.

6.0 CONTROL UNIT (Cont.)

If the processor should attempt a DAT0 with the CU when it is conducting an operation, the CU will cease operation and generate an interrupt. Under certain error conditions it will stop data transfers but will wait until the end of the intended operation before generating the interrupt.

The processor may conduct a DAT1 while the CU is active without interfering with the CU operation.

Figure 3 is a block diagram of a CU that is configured for a basic system. The CU may be broken into six major functional groupings. They are: 1) Address decoder, 2) input bus and multiplexer, 3) registers, 4) output bus and multiplexer, 5) Unibus request and control, and 6) CU timing and control.

6.1.0 ADDRESS DECODER

The address decoder is capable of recognizing eight consecutive addresses. The processor supplies the address on UNIBUS lines A00-A17 and the appropriate control signals. If the processor in performing a DAT0 it must also supply data on lines D00-D15. For a DAT1 it will receive data on lines D00-D15. In the basic system only five of the eight possible addresses are used. Each address is used to gain access to one of the five storage registers. For a DAT0 the selected register will be loaded with a processor word via the CU input bus and load signals. For a DAT1 the selected register contents will be transferred to processor memory via use of the CU output bus. If one of the three additional addresses is accessed the CU response is the same as if one of the five basic registers was accessed. The eight addresses and their use is given in section 7.0.

6.2.0 INPUT BUS AND MULTIPLEXER

Data may be gated onto the input bus from either the unibus or from a tape unit. The multiplexer under command of the timing and control section selects the data source. The input bus provides data for four of the registers. The MTS (status register) is not loaded from the input bus. When a clear command is received the multiplexer forces the input bus to all zeros, then all registers are set to

the INITIAL state. The MTD (data register) is cleared by this method, in a read operation, prior to transferring a tape character to the MTD register.

6.3.0 REGISTERS

The five registers of the CU are 1),MTS (status register 2),MTC (command register) 3),BRC (byte record character) 4), CMA (current memory address) and 5),MTD (data buffer).

A detailed description of each register and the function of each bit along with the programming format is given in section 7.0

The purpose of each register is:

6.3.1 MTS

The MTS is used to monitor system condition. It cannot be loaded under program control. It's contents are read by the processor on a DAT1 command. It is cleared by a DAT0 command or by a go command to the MTC.

Bits 0 through 6 are used to ascertain the condition of the selected tape transport.

Bits 7 through 14 are used to determine operational errors.

Bit 15 detects an illegal command to the CU.

Bit assignments are given in section 7.1.0.

6.3.2 MTC

The MTC is used to control operation of the tape units and data transfers.

It selects transport, function, odd or even parity, and tape density. It determines if an interrupt can be generated, and when to start the tape operation.

It also contains two bits that are an extension of the CMA register and three bits that are not accessed by an operational program. They are the error bit, power clear bit, and the CU ready bit.

The error bit is set as a function of bits 7 through 15 of the MTS register and cleared when the MTC go bit (bit 0) is set.

The power clear bit when set causes a clear command that initializes all storage elements in the CU including itself. It is set under program control. In addition the CU is initialized whenever its power is turned on, or whenever the processor is initialized.

When the CU ready bit (CURD) is set the CU is ready to execute a command. It clears at the start of a tape operation and sets when the operation is complete. A clear command sets it. It must be in the set state, or the sequence of events that set it at the end of a tape operation must be initiated before the CU will recognize a command as legal.

Bit assignments for the MTC register are given in section 7.2.0.

6.3.3 BRC

The BRC is a 16 bit counter that is used to count bytes (characters) in a read, write, or write with extended GAP operation. It is incremented by one as each character is written on or read from tape.

In a space forward or space reverse operation it is used to count records. It is incremented by one after each record is read.

The BRC is initially set to the 2's complement of the number of operations that are to occur. After the proper number of operations its contents will equal zero.

6.3.4 CMA

The CMA is an 18 bit counter that for any CU initiated data transfer supplies the processor memory address. Sixteen of the bits are contained in the CMA, the two most significant bits are located in the MTC and are loaded when the MTC is loaded.

The CMA is initially set to the starting address when the CU is placed in a read, write, or write with extended GAP mode of operation.

It is incremented by one for each character that is written on or read from tape.

A detailed description of CMA operation is given in section 7.4.0.

6.3.5 MTD

The MTD is a 16 bit register that is used for temporary data storage when the CU is in a read, write or write with extended GAP mode of operation.

The MTD along with the input multiplexer and the tape data drivers formats the data per the requirements listed in Table 1.

6.4 OUTPUT MULTIPLEXER AND BUS

The output multiplexer and bus is used to provide the contents of any of the CU registers and the interrupt vector address to the unibus. The processor may gain access to any of the registers by addressing the desired register when it performs a DATI.

The vector address is placed on the output bus, whenever the CU is generating an interrupt or whenever the processor performs a DATI to location 772536.

The MTD contents are placed on the bus during a data transfer when the CU is in the read mode.

6.5 UNIBUS REQUEST AND CONTROL

The CU uses the request and control section for two purposes; 1) to generate an interrupt that causes the processor to enter a service routine, and 2) to effect a NPR data transfer.

For either operation the CU must first gain control of the unibus. For an interrupt the request is made by use of the priority structured bus request lines.

For a data transfer the NPR (non processor request) line is used. When an NPR is granted the CU then conducts a direct memory access with the processor.

An interrupt is generated whenever an error occurs or when the CU detects that a processor commanded operation has been completed. For an interrupt, the CU

supplies the address.

When in the read mode the CU causes the contents of the MTD to be stored in processor memory at the specified location.

In the write or write with extended GAP mode the contents of the CU specified location are stored in the MTD.

The timing for bus control is supplied by the unibus request and control section.

6.6 CU TIMING AND CONTROL

The timing and control portion of the CU provides synchronization of the CU, tape units, and processor. It decodes the processor commands and causes the tape units to execute them. It establishes the timing signals necessary for system operation.

7.0 CONTROL UNIT PROGRAM FORMAT

Five registers, contained in the CU are available to the programmer for control of data transfers between the PDP-11 and the tape transports. The five registers and their addresses are:

REGISTER		ADDRESS
STATUS	(MTS)	772520
COMMAND	(MTC)	772522
BYTE RECORD COUNTER	(BRC)	772524
CURRENT MEMORY ADDRESS	(CMA)	772526
DATA BUFFER	(MTD)	772530

In addition the CU provides three other addressable locations. They are:

FUNCTION	ADDRESS
MTRD	772532
OPTIONS	772534
VECTOR ADDRESS	772536

7.0 CONTROL UNIT PROGRAM FORMAT (Cont.)

The CU will attempt to execute the command stored in the MTC register whenever MTC bit 0 (GO BIT) is set.

If the command is a write, write with extended gap or read operation, the CMA and BRC must be properly loaded before MTC bit 0 is set.

If the command is a space operation the BRC must be loaded prior to setting the go bit.

For a go off line, write EOF or rewind command it is not necessary to load any other registers before setting the go bit.

The MTC register may be set prior to the other registers if the go bit is not set.

If MTC bit 6 (interrupt bit) is set the CU generates an interrupt for the following conditions:

1. An MTC load that sets bit 6 but does not set bit 0.
2. Whenever a tape operation is completed, or for go off line or rewind whenever the tape unit acknowledges the command. For a rewind operation a second interrupt is generated at completion of the rewind sequence if no subsequent commands are given to the CU.
3. Whenever the error bit is set. The error conditions that cause the error F/F to set are of two types, A) a system or hardware error, and B) a logical error.

System and/or hardware errors cause the error F/F to set as soon as they are detected. Logical errors cause the error F/F to be set when the operation currently in progress is completed. System and hardware errors are, illegal commands, bus grant late and nonexistent memory. Logical errors occur whenever end of file (EOF), parity error (PAE), end of tape (EOT) or record length error (RLE) is detected.

To minimize the time that the CU has control of the bus, most NPR's (data transfers) are word transfers (16 bits) instead of byte transfers (8 bits). If the CU is in the write, or write with extended gap mode of operation, all NPR's are word transfers. The CU determines whether to use all or only part of the word. If the CU is in the read mode it limits byte operations to the first and/or last character of a tape record. It is not necessary for the programmer to take any special precautions when setting up the BRC and CMA registers.

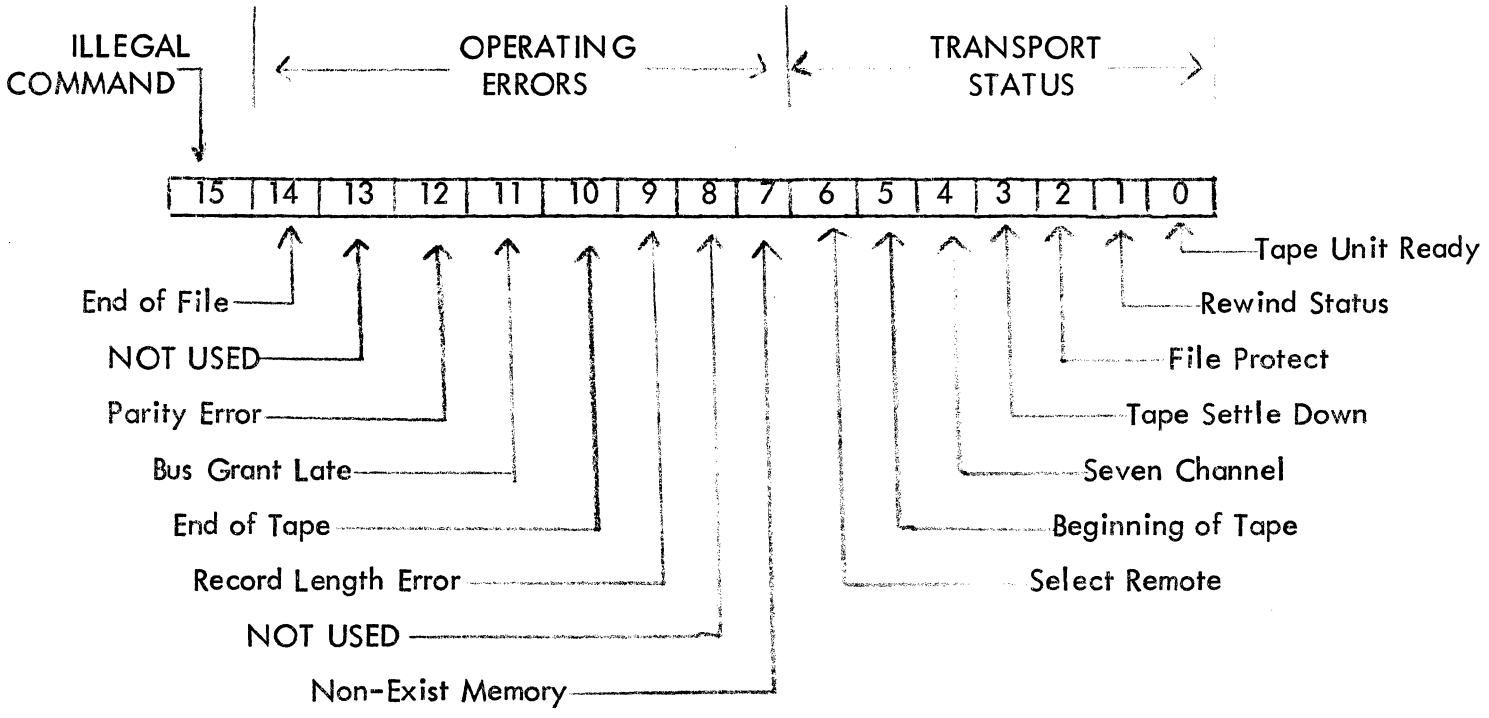
7.0 CONTROL UNIT PROGRAM FORMAT (Cont.)

7.1.0 MTS BIT FUNCTIONS

The MTS register gives the system status at all times.

Table 7-1 gives the bit functions. All bit states are for the unit that is currently addressed by the MTC.

MTS REGISTER



BIT	NAME
15	ILLEGAL COMMAND (ILLC)

Bit 15 is set by any of the following illegal commands:

1. Any DAT0 or DAT0B to the CU during the tape operating period,
2. A write, write EOF, or write with extended gap operation when the file protect bit is a one,
3. A command to a tape unit whose SELECT REMOTE (SELR) bit is a zero,
4. The SELR bit becoming a 0 during an operation.

In error conditions 1 through 3, the command is loaded into the MTC, but the GO pulse to the tape unit is not generated, and the CU ready bit remains set. The MTC error bit is set immediately when ILLC is true.

BIT	NAME	
14	END OF FILE (EOF)	An EOF character is detected during a read, space forward or space reverse operation. The EOF bit is set when the EOF character is read. The MTC error bit is set when the BEND pulse following the EOF character is detected.
13	NOT USED	
12	PARITY ERROR	This bit is set whenever an uncorrectable error has been detected. The MTC error bit is set by the BEND pulse.
11	BUS GRANT LATE (BGL)	A bus grant late error occurs when the control unit after issuing a request for the bus, does not receive a bus grant before the control unit receives the clock pulse for the following tape character. The condition is tested only for NPR operations. The error bit sets simultaneously with BGL, thus terminating the operation. If the BGL occurs during a write or write with GAP operation, a last word signal is sent to the tape unit terminating the tape operation.
10	END OF TAPE (EOT)	Set to 1 as the EOT marker is read while the tape is moving in the forward direction. The Bit is cleared as soon as the same point is read while the tape is moving in the reverse direction. The MTC error bit is set only in the tape forward direction when a BEND pulse following EOT is detected.
9	RECORD LENGTH ERROR (RLE)	This bit is set in the read mode only. It is set when the number of characters contained in a record is greater than the number of times the BRC can be incremented before becoming zero. After BRC reaches zero, data transfers to memory and incrementing of the BRC and CMA is stopped. The CU reads the entire record then sets the MTC error bit when the BEND pulse is detected.

7.0 CONTROL UNIT PROGRAM FORMAT (Cont.)

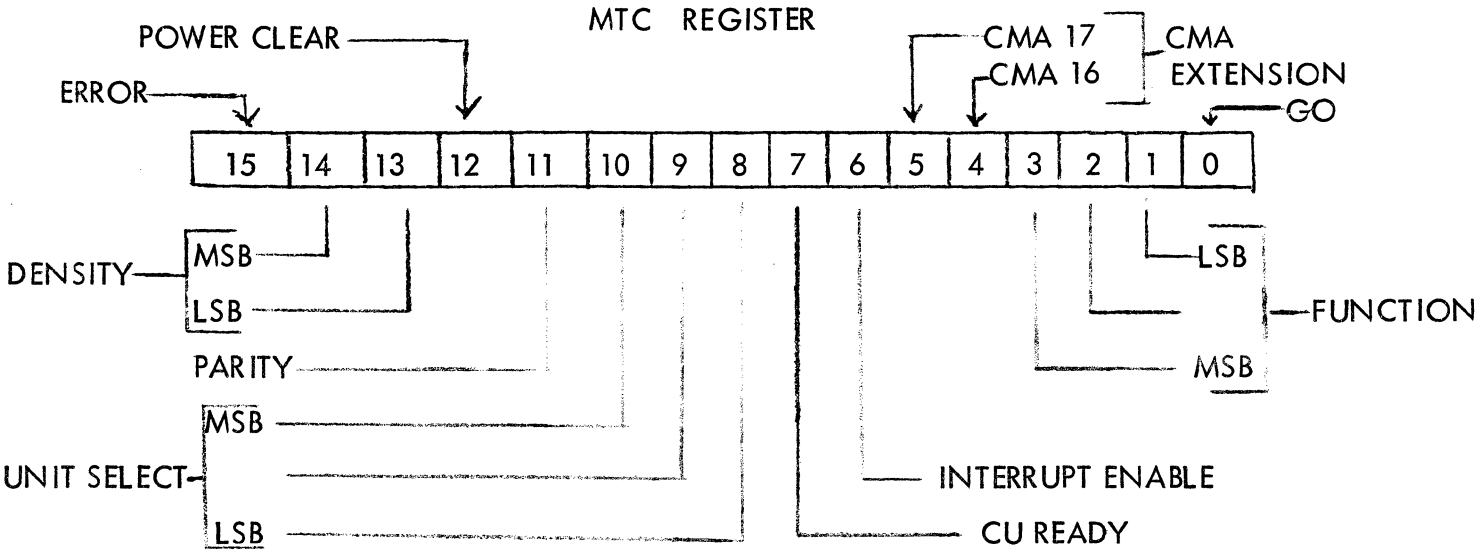
BIT	NAME	
8	NOT USED	
7	NON-EXISTENT MEMORY (NXM)	This error occurs during an NPR operation when the CU is bus master, and does not receive a slave sync (SSYN) signal within 10 micro seconds after the CU has issued a master sync (MSYN) signal. The operations which occur when this error is detected are identical to those indicated for a BGL error.
6	SELECT REMOTE (SELR)	This line is true when the selected transport is under remote control. When false the transport is off line and cannot be operated extemally.
5	BEGINNING OF TAPE (BOT)	This line is true when the selected transport is at the load point and false at all other times.
4	SEVEN CHANNEL (7CH)	This line is true when the selected transport is a seven track unit. When false it indicates a 9 track unit.
3	TAPE SETTLE DOWN (SDWN)	Set whenever the tape unit is slowing down.
2	FILE PROTECT (FPRO)	This line is true when no write ring has been installed on the supply reel of the selected transport. The transport will not write when this output is true. A write command to a unit whose FPRO signal is true is an illegal command (see bit 15).
1	REWIND STATUS (RSTAT)	This line is true when the selected transport is in a rewind or advance to load point operation.
0	TAPE UNIT READY (TUR)	TUR is true when the tape unit is stopped and when SELR (Bit 6) is true. When TUR is true the tape unit will accept a command. It is cleared when the tape unit begins an operation.

7.0 CONTROL UNIT PROGRAM FORMAT (Cont.)

7.2.0 MTC BIT FUNCTIONS

The MTC register decodes the program commands and issues the signals that are necessary for the tape units to perform the intended operation.

It also maintains system synchronization by determining if a command can be accepted, when to begin execution, and when the operation is completed.



BIT	NAME	
15	ERROR (ERR)	Set as a function of bits 7-15 of the MTS. Cleared when CU is cleared or when the GO bit is set.
14-13	DENSITY (DEN2-DEN1)	Set and cleared under program control. These bits are used to select tape density.
12	POWER CLEAR (PCLR)	When set clears CU without clearing other system devices. Clears itself after CU is cleared. It is used along with The CLR flip flop to initialize the CU. See section 7.6.0 for a description of initialize.
11	LATERAL PARITY (PEVN)	Set and cleared under program control. This bit is used to select EVEN or ODD vertical parity for the formatter parity generation and checking circuitry. When set selects EVEN parity, when cleared selects ODD parity. This line is ignored and ODD parity is forced internally if the selected transport is a 9 track unit.

BIT	NAME	
10-8	UNIT SELECT (USL3-USL1)	Set and cleared under program control. These bits are used to select one of the eight possible transports. For dual density transport (NRZI & PE) bit 10 should be cleared to select formatter address Ø (normally NRZI) and set to select formatter address 1 (normally PE). The customer can confirm these formatter address switch settings by simply referring to his formatter manual. All operations defined in the MTC and status conditions defined in the MTS pertain to the tape unit selected by these bits.
7	CU READY (CURD)	Cleared at the start of a tape operation, and set at the end of a tape operation. This bit must be set before the CU will accept a command as legal. Set by a CLR command.
6	INTERRUPT ENABLE	Set and cleared by the program. When set an interrupt is generated whenever CURD or ERR changes from 0 to 1, or whenever a rewinding tape unit arrives at the BOT marker. In addition, an interrupt occurs on an MTC program command that sets bit 6 (INBL) but does not set bit 0 (GO).
5-4	ADDRESS BITS (CMA5-CMA4)	Extended memory bits. The bits correspond to bits 17 and 16 respectively of the bus address. They are an extension of the CMA and increment on a CMA carry.
3-1	FUNCTION BITS (FUNC1-FUNC3)	Set and cleared by the program. These bits define the eight possible tape functions. Bit 1 is the LSB.
0	GO	Set under program control whenever the operation defined by the MTC function bits is to be executed. It is cleared as soon as the CU sends a go command (FOST) to the formatter.

7.0 CONTROL UNIT PROGRAM FORMAT (Cont.)

The combinations of bits 14 and 13 and their definitions are:

BIT 14	BIT 13	BPI	SELECTED TRANSPORT
0	0	200	7 CHANNEL
0	1	556	7 CHANNEL
1	0	800	7 CHANNEL
1	1	800	9 CHANNEL (NRZI)
1	1	800	7 CHANNEL (CORE DUMP MODE)
1	1	1600	9 CHANNEL (MODE PE, SGL OR DUAL DENS)

A core dump mode is possible only when the selected transport is a 7 track unit. A description of core dump mode is given in section 4.10.

The combinations of bits 3-1 and their definitions are:

BIT 3	BIT 2	BIT 1	FUNCTION
0	0	0	OFF LINE
0	0	1	READ
0	1	0	WRITE
0	1	1	WRITE EOF
1	0	0	SPACE FORWARD
1	0	1	SPACE REVERSE
1	1	0	WRITE WITH EXTENDED GAP
1	1	1	REWIND

7.3.0 BYTE RECORD COUNTER (BRC)

The BRC is a 16 bit counter that is used to count bytes (characters) in a read, write, or write with extended GAP operation. In a space forward or space reverse operation it is used to count records.

When the BRC is used in a write operation it is initially set by the program to the 2's complement of the number of bytes to be written on tape. The BRC is incremented whenever a character is written on tape. When the next to last character has been written a last character signal (LCHAR) is generated. Thus when the next write clock occurs a last word signal occurs indicating to the tape unit that it is now writing the last word of a record.

7.3.0 BYTE RECORD COUNTER (BRC) (Cont.)

When the BRC is used in a read operation it is set to the 2's complement of a number equal to or greater than the number of characters to be read from tape. If a partial record is to be read the number is less than the number of characters contained in the record. When the BRC has incremented to zero, data transfers are stopped. The CU waits until the LPC character is detected before generating an interrupt that causes the service routine to become active. If a character (not LPC) is detected after BRC reaches zero the record length error bit is set and the error bit is then set when BEND is detected.

When a space forward or space reverse operation is to be performed, a go command must be sent to the formatter for each record to be spaced. The first go command is sent to the formatter when the MTC go bit is cleared. Subsequent go commands are sent at the end of each record. The BRC is initially set to the 2's complement of the number of records to be spaced. It is incremented by the LPC pulse that occurs at the end of a record. If the LCHAR signal is not true at LPC time a new go command is sent to the formatter, which causes another record to be spaced. When LCHAR becomes true the go command is inhibited and the tape unit stops. An interrupt to the processor that signifies action completed is then generated. The LPC pulse occurs after the tape unit has traversed a complete record for both forward and reverse operations.

7.4.0 CURRENT MEMORY ADDRESS (CMA)

The CMA contains 16 of the possible 18 memory address bits. Bits 4 and 5 of the MTC are used as the two most significant bits of the CMA. The CMA is used to provide the memory address for data transfers in read, write, and write with extended GAP operations. Prior to starting a data transfer the CMA is set to the memory address into which the first byte is loaded in a read operation, or from which the first byte is read in a write or write with extended GAP operation. The CMA is incremented by one after each memory access. At any instant of time the CMA contains an address higher than the one which had most recently been accessed. When the entire

7.4.0 CURRENT MEMORY ADDRESS (CMA)

record has been transferred, the CMA contains the address plus one of the last character in the record. In the error conditions Bus Grant Late (BGL) and Non-Existent Memory (NXM), the CMA contains the address of the location in which the failure occurred.

Since the CU logic determines if a byte or word operation is to take place there are no program restrictions in loading the CMA.

It can start and end on any combination of odd or even addresses, and number of characters. If required the CU will perform byte data transfers for the first and/or last characters only. All intervening data transfers consist of a full word.

7.5.0 DATA BUFFER (MTD)

The MTD is a 16 bit register which is used during a read, write, or write with extended GAP operation. In a tape read operation the MTD acts as a temporary storage buffer that assembles a full 16 bit word. After the word is assembled the CU executes an NPR and stores the word in processor memory. The MTD is then cleared. In a write or write with extended IRG operation the CU executes an NPR and stores a 16 bit processor word in the MTD. All 16 bits are then written on the tape as characters. Table 1 shows the relation between processor bits and tape characters. Note that in normal operation two tape characters make up one processor word, and that in core dump mode 4 tape characters make up one processor word. Also note that core dump is only possible with a seven track unit.

7.6.0 MTRD

The MTRD register is not used with the Digi-Data tape unit.

Address recognition circuitry is provided so that an NXM error will not occur if an attempt is made to access this register. For a DATI to the MTRD the data will be read as all zeros.

7.70 OPTION

There is a byte reversal switch provided as a standard option on each PDP-11 controller. The purpose of the switch is to provide the customer with the option of either writing/reading the low byte as the first character of each computer word on tape (DEC standard), or writing/reading the high byte as the first tape character of each computer word (IBM standard).

The selection is made by a switch located on the controller, at the rear of the outrigger chassis. The switch position labeled DEC will enable the controller to write/read each computer word in the low/high byte order. The switch position labeled IBM will allow the controller to write/read each computer word in the high/low byte order.

The TM11 instruction test software supplied with the controller will fail the read three byte record test with the switch in position IBM. The third byte read will be stored in the high byte instead of the low byte as expected (PC = 5466 for MAINDEC-11-DZTMA-C-D). The data reliability program will run in its entirety with the switch in either position.

The OPTION register is used to implement customer specified options. A DATI to the option register will produce a data output of all ones in the basic system. If the options are specified, a DATO setting bits Ø and 1 will load the desired thresholds, and bit 2 the EDIT option. Bit Ø selects read threshold 1 while bit 1 selectes read threshold 2. A DATI to the option register with the options will produce all zeros in bits 3-15, and indicate if the desired option bits are set.

7.80 VECTOR

The VECTOR register is not programmable from the processor, it is hardwired to give the vector address at time of delivery. It may be accessed by a DATI command to ascertain the vector address. It will respond to a DATO, so that an NXM error will not occur, but its contents will not be changed. Unless otherwise specified, units will be supplied with a vector address of 224_8.

7.90 INITIALIZE

The CU and tape transports have independent power switches. The formatters receive their power from either the CU or tape transports, depending on the physical arrangement. When a unit is turned on it is automatically cleared to an initial state (ready to receive commands). The CU is also initialized whenever the PDP-11 is turned on or off, by program control, or by the start switch located on the PDP-11 control console.

TABLE 1

DATA FORMAT

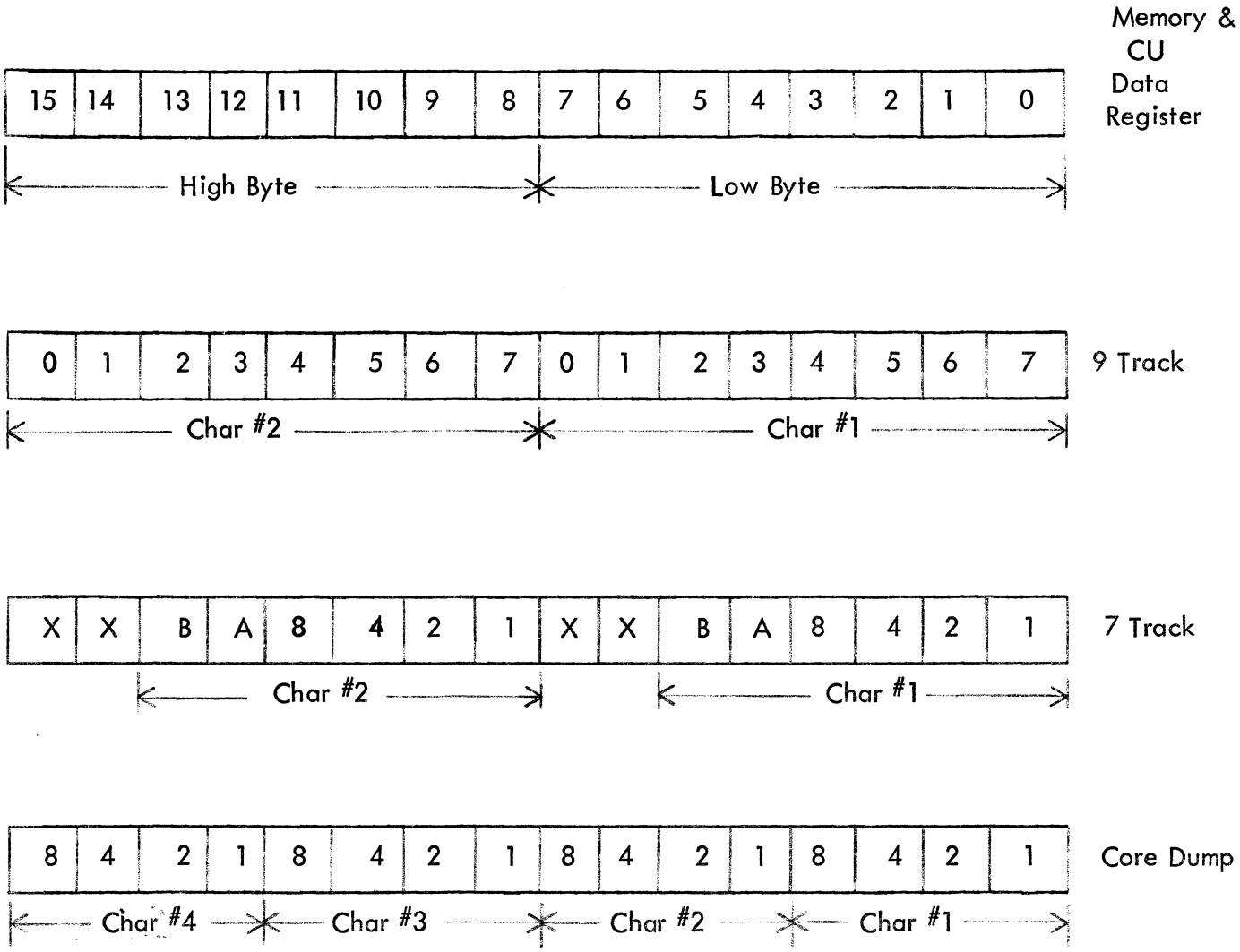


TABLE 2

DATA TRANSFER SIGNALS

NAME	MNEMONIC	NO OF LINES
DATA	D00-D15	16
ADDRESS	A00-A17	18
CONTROL	C0, C1	2
MASTER SYNC	MSYN	1
SLAVE SYNC	SSYN	1
PARITY BIT LOW	PA	1
PARITY BIT HIGH	PB	1
		40

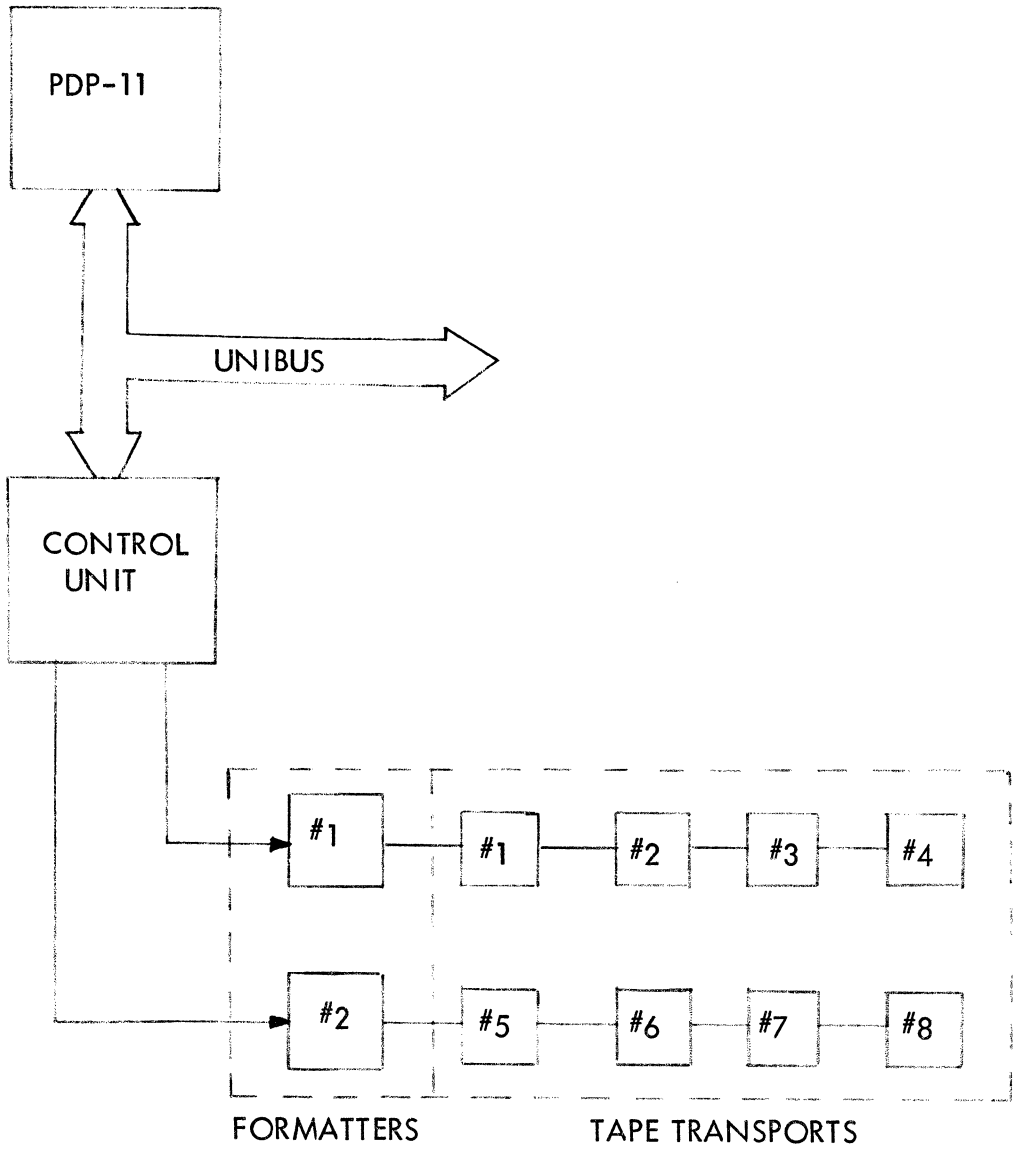

PDP-11
UNIBUS
CONTROL UNIT
#1
#1
#2
#3
#4
#2
#5
#6
#7
#8
FORMATTERS
TAPE TRANSPORTS

Figure 1

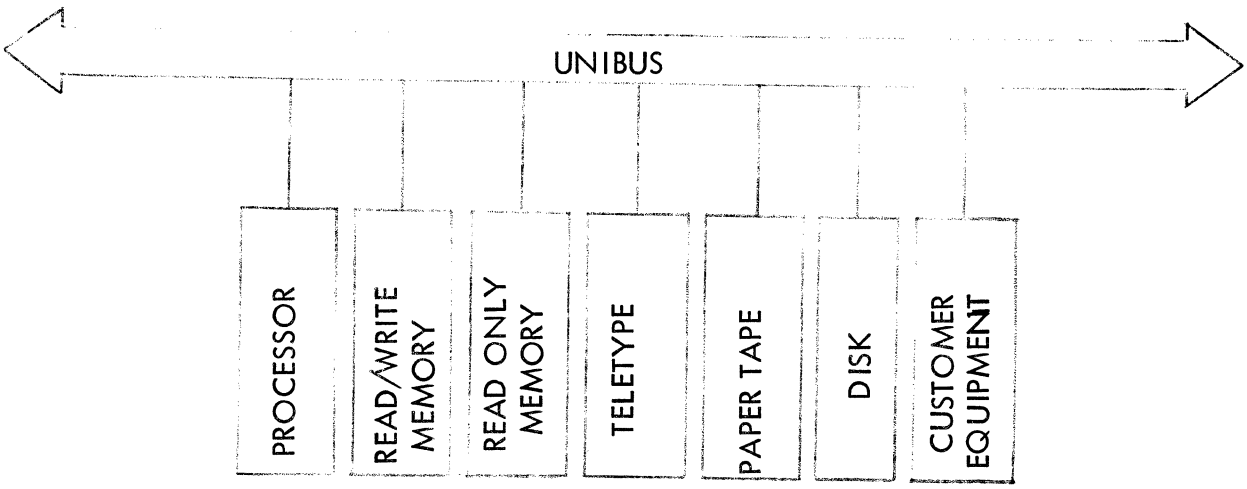
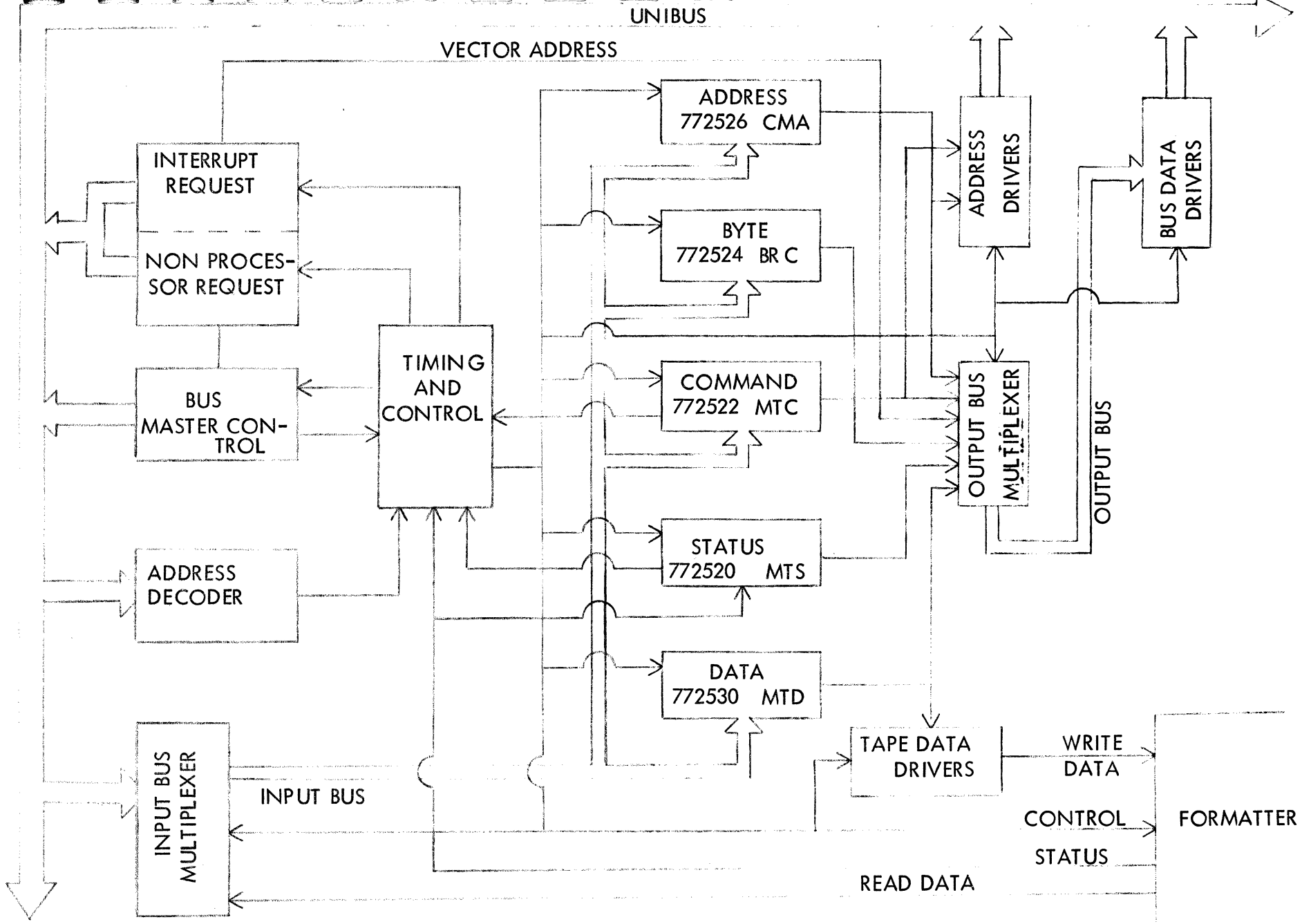

UNIBUS
PROCESSOR
READ/WRITE MEMORY
READ ONLY MEMORY
TELETYPE
PAPER TAPE
DISK
CUSTOMER EQUIPMENT

Figure 2



BLOCK DIAGRAM

CONTROL UNIT

Figure 3

OVERLAY FOR TM 11 INSTRUCTION TEST

MAINDEC-11-DZTMA-C-D

2-13-74

Address	New Contents	Instruction	
003104	000420	BR, +42	; Bit 14 of MTRD not used
005764	060013		; Incorrect density given
006112	000446	BR, +116	; Bad tape not used
006376	000005	Reset	; Skip part of
006400	000414	BR, +32	Interrupt Test
006464	064107		; WRT EOF PAR for 7 trk
007230	000137	JMP MIT	; Skip PAR, CRCC test
007232	011156		
011266	000437	BR, +100	; Select is done through cable
012346	166460	JMP START	
012422	166404	JMP START	

FOR PE ONLY

005230	000415		; Skip EOF Character Check

To use overlay first load MAINDEC Instruction Test. After load is completed load Digi-Data patch tape as any other binary tape (i.e., use same starting location used for loading instruction test). Tape will stop after NRZI only changes are loaded. If unit to be tested is a PE recorder, reload starting address and load last portion of patch tape.

TM11 DATA RELIABILITY (9 TRK)
MAINDEC-11-DZTMB-B-D

When running the 9 TRK data reliability program on a dual density drive (NRZI & PE) problems will arise if the operator selects the auto select mode (starting address 200). In this mode the program automatically selects any tape drive online. Since the first dual density drive online will be addressed as NRZI unit Ø and PE unit 4 (see MTC unit select) the program will try to write/read both NRZI and PE on the same tape. This naturally will generate an incompatible tape and cause errors.

To remedy this problem the operator should select the drive via the TTY (program starting address 204 or 208). To run dual density drives select units Ø-3 for the NRZI mode (formatter address & MTC select bit 1Ø, zero) and units 4-7 for PE (formatter address 1 and MTC select bit 1Ø, one).

OVERLAY FOR MAINDEC-11-DZTMC-A-D

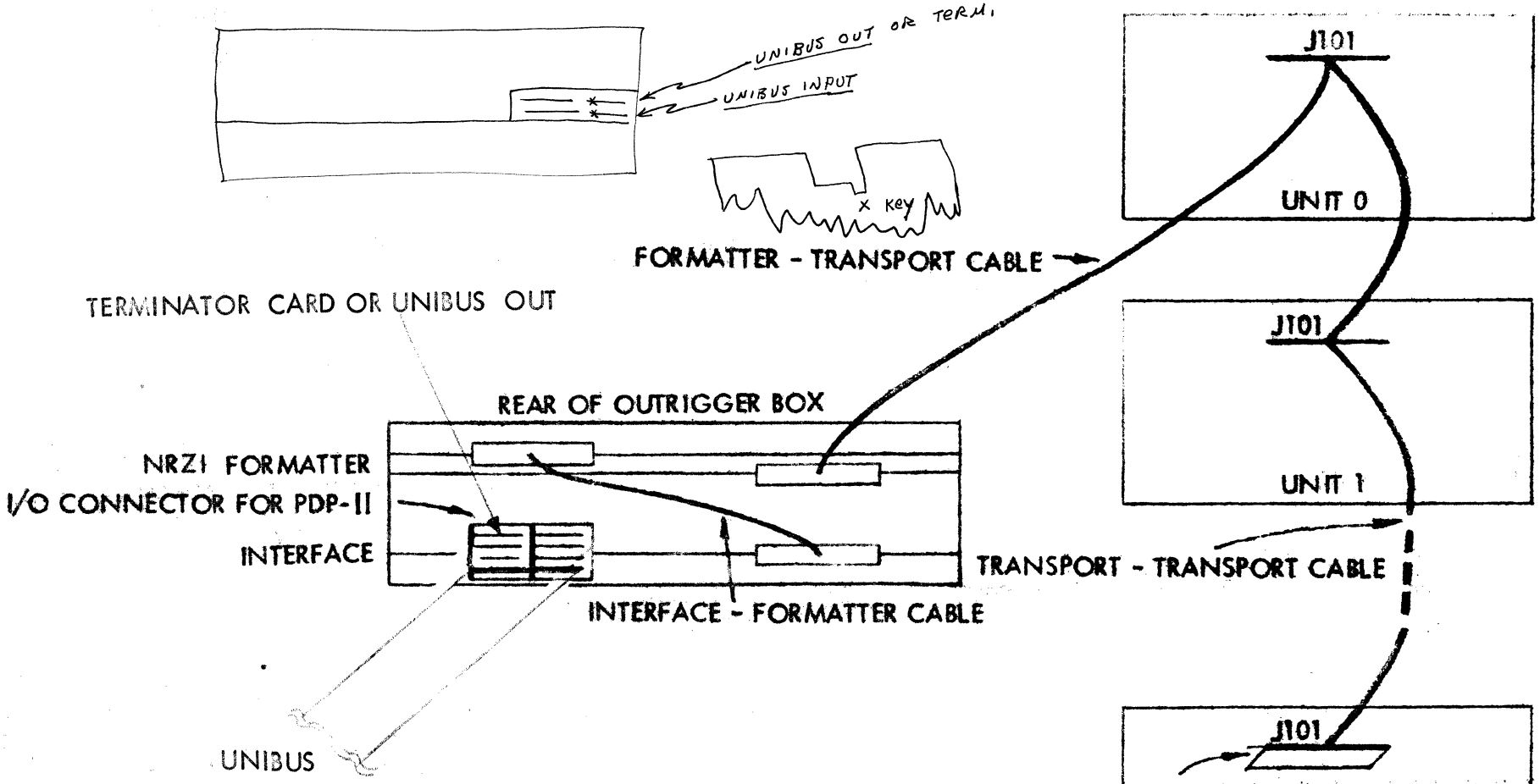
TM 11 DATA RELIABILITY (7 Trk)

May 14, 1973

This patch tape is required only for the core dump mode patterns 4 & 7, even parity. The main program doesn't take into account that when writing these two patterns the all 0's character will appear. When writing IBM compatible tapes, and the all 0's character is written in even parity, the formatter forces 1's in two tracks. This enables the formatter to detect the character when reading. Therefore when reading, the program must take this into account or discard the all 0's character when writing. The main program does discard the all 0's character for the 7 Trk non core dump, but neglects the possibility for core dump. This patch discards the all 0's character when writing.

To use overlay first load Maindec data reliability test. After load is completed load Digi-Data patch tape as any other binary tape (i.e. use same starting location used for loading data reliability test). Tape will stop after core dump changes are loaded. To restore original program, reload starting address and load last portion of patch tape.

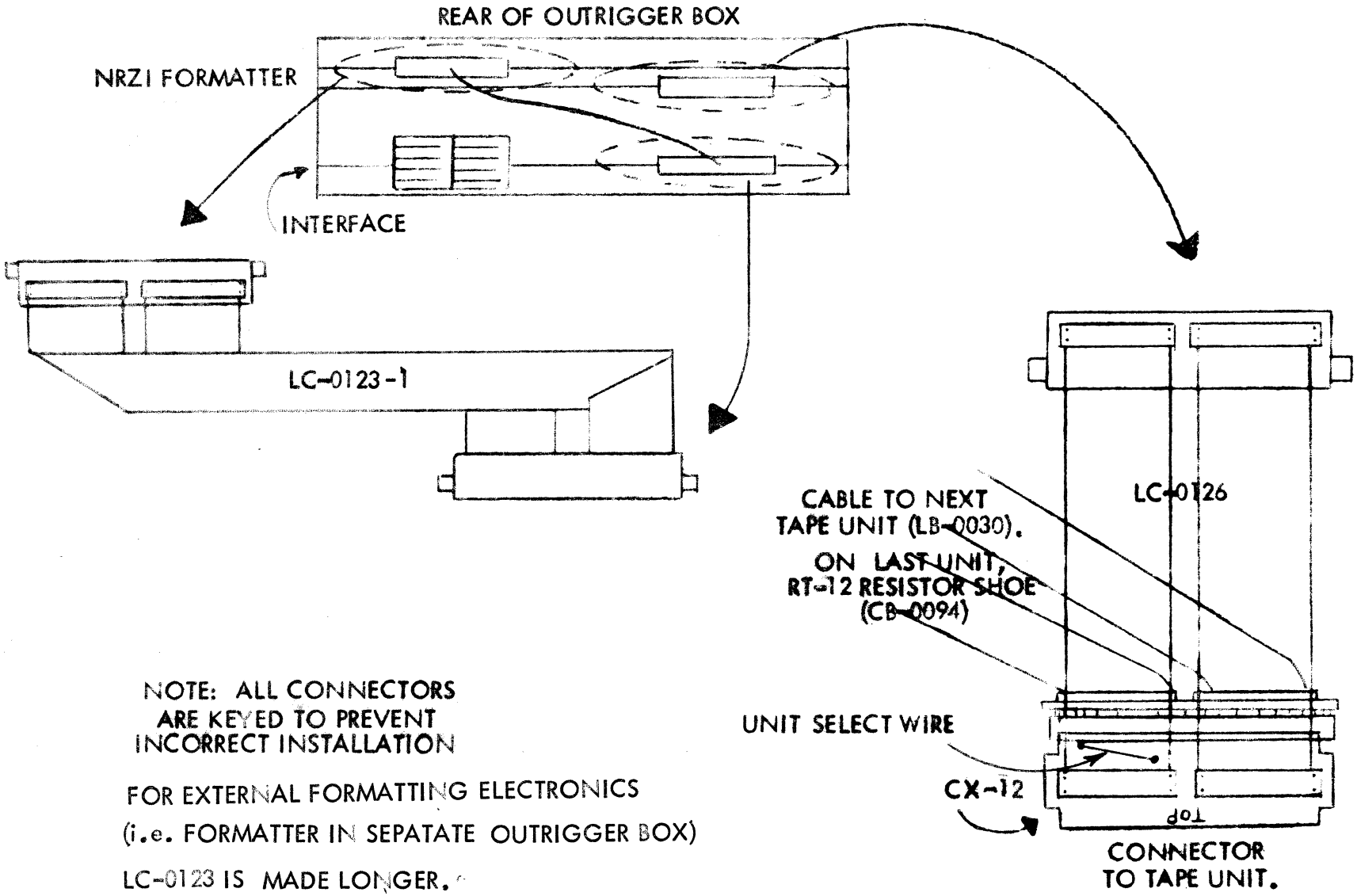
ADDRESS	NEW CONTENTS		INSTRUCTION
006624	000167		JMP INCPAT
006626	010432		
006644	000167		JMP TSTB INC
006646	010416		
006760	000167		JMP TSTB RAN
006762	010246		
006764	000240		
006766	000240		
017232	132767	TSTBRAN:	BIT B # 360, RANDOM
017234	000360		
017236	170072		
017240	001406		BEQ, + 16.
017242	132767		BITB # 17, RANDOM
017244	000017		
017246	170062		
017250	001402		BEQ, + 6
017252	000167		JMP PATE 7+10
017254	167506		
017256	000167		JMP PATE 7
017260	167472		
017262	012703	INC PAT:	MOV # 21, R3
017264	000021		
017266	132703	TSTB INC:	BIT B # 360, R3
017270	000360		
017272	001405		BEQ, + 12
017274	132703		BITB # 17, R3
017276	000017		
017300	001402		BEQ, + 6
017302	000167		JMP PATE 4 + 4
017304	167322		
017306	105203		INCB R3
017310	000766		BR, -22



SYSTEM INTERCONNECTION

DIGI-DATA CORPORATION

SHEET OF

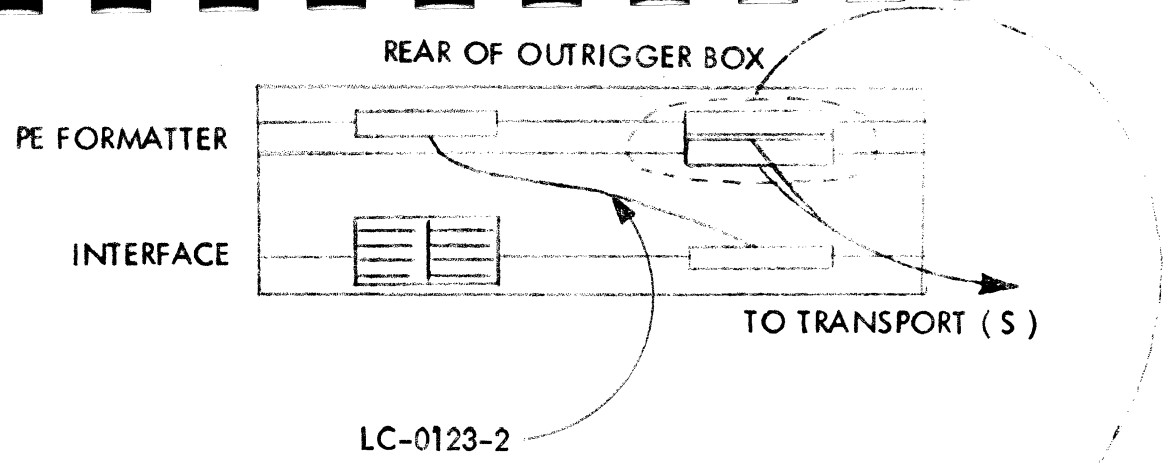


NOTE: ALL CONNECTORS ARE KEYED TO PREVENT INCORRECT INSTALLATION

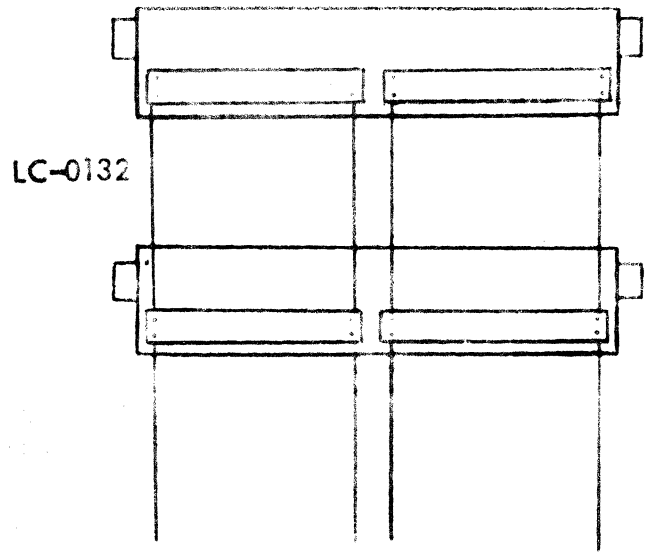
FOR EXTERNAL FORMATTING ELECTRONICS
(i.e. FORMATTER IN SEPATATE OUTRIGGER BOX)
LC-0123 IS MADE LONGER.

CONTROLLER WITH NRZI FORMATTER

DETAILED SYSTEM INTERCONNECTION	DIGI-DATA CORPORATION
	SHEET OF



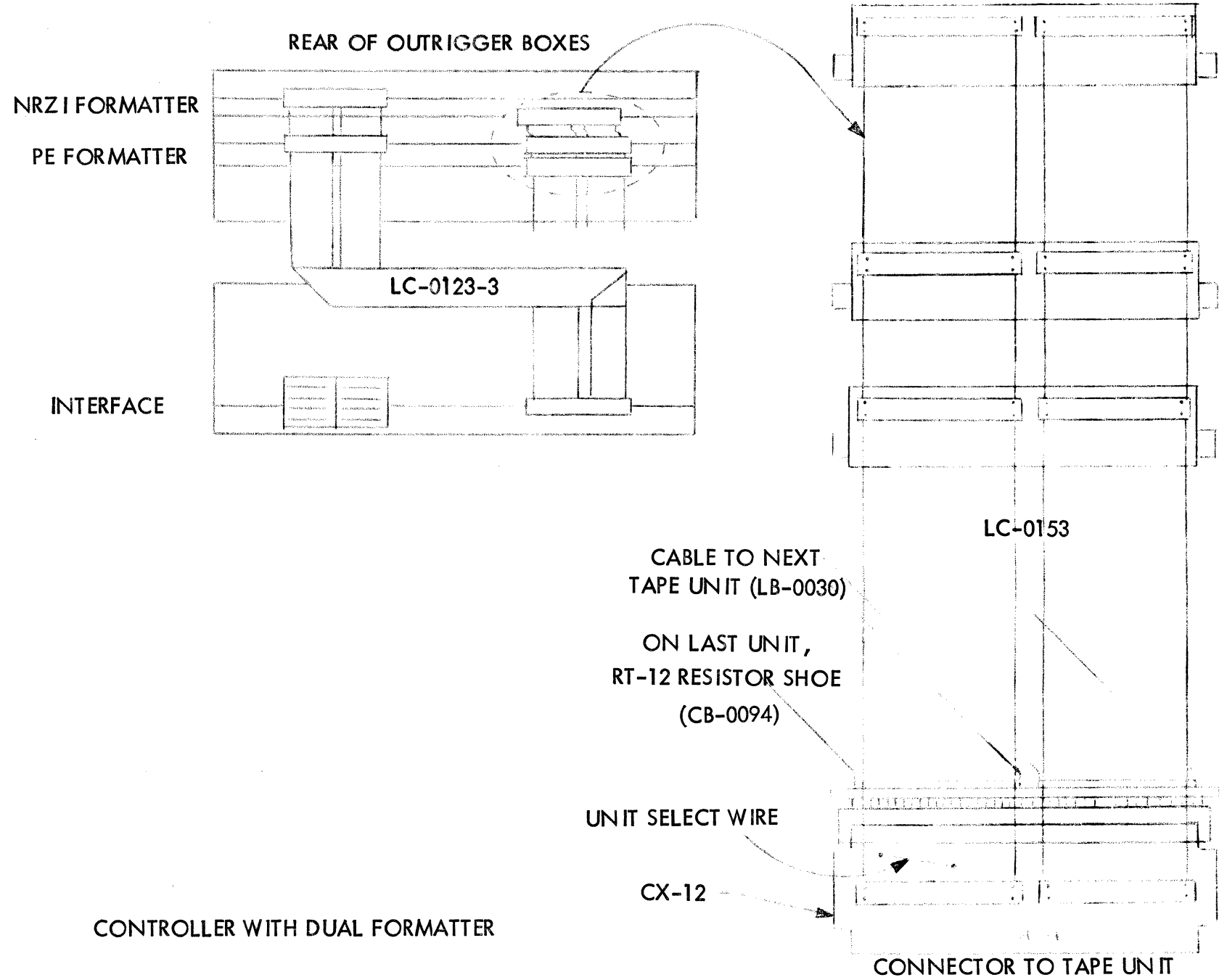
LC-0123-1 & -2 DIFFER ONLY AS TO KEYING



REMAINDER OF DRAWING IS SAME AS FOR NRZI FORMATTER

CONTROLLER WITH PE FORMATTER

DETAILED SYSTEM INTERCONNECTION	DIGI-DATA CORPORATION
	SHEET OF



CONTROLLER WITH DUAL FORMATTER

DETAILED SYSTEM INTERCONNECTION	DIGI-DATA CORPORATION
	SHEET OF

PROGRAM TO WRITE OR READ 3 BYTE RECORD

(SEE TIMING DIAGRAMS 6, 7)

Starting Address = 000400

Location	Contents	Instruction
000400	012767	MOV #177775, BRC
000402	177775	
000404	172116	
000406	012767	MOV #434, CMA
000410	000434	
000412	172112	
000414	012767	MOV #060005, MTC
000416	060005	WRITE 800 BPI, GO
000420	172100	
000422	032767	BIT #200, MTC
000424	000200	
000426	172072	
000430	001774	BEQ, -6
000432	000000	HALT

Deposit 000762 (BR 400) in location 000432 to continue writing three byte records

Data is written from location 000434 as set up by the programmed instruction MOV #434, CMA. Place desired data to be written in location 000434 and 000436.

To read 3 byte record, deposit address where data is to be read into in location 000410 of program. Deposit 060003 (read 800 BPI, go) in location 000416. Data read can then be compared with data written.

SPECIAL SCOPE ROUTINES TO EXAMINE DAT0 AND DATI SIGNALS

(SEE TIMING DIAGRAMS 1, 2)

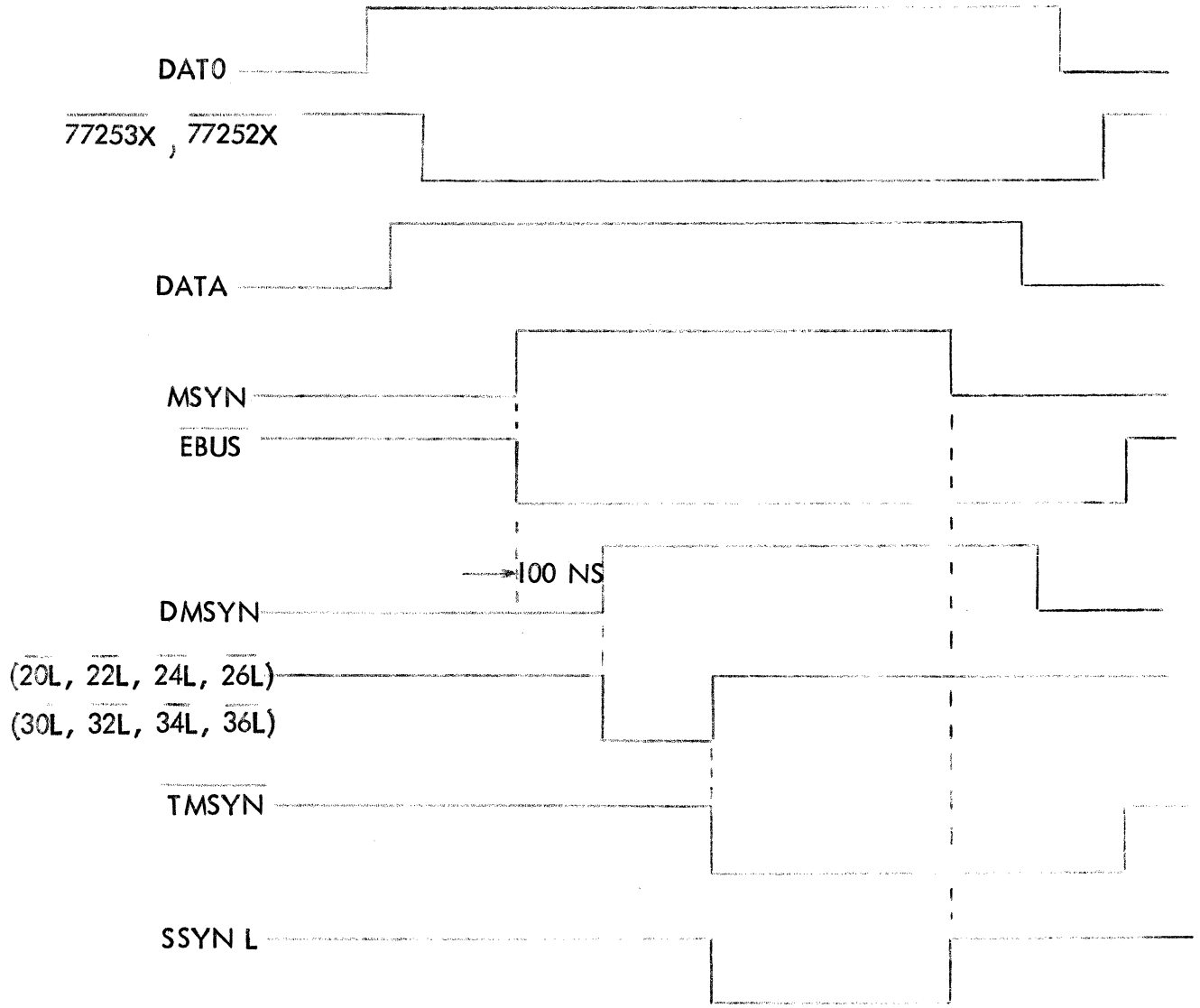
	Location	Contents	Instruction
DAT0 (MTC LOAD)	000414	012767	MOV # MTC
	000416	0XXXXX	DESIRED #
	000420	172100	
	000422	000774	BR 414

The contents of location 416 contain the desired number to be loaded in the command register. Bit 15 (error) cannot be loaded.

DATI (SEND CURD MTC Ø7)	000422	032767	BIT #200 MTC
TO PROC.	000424	000200	
	000426	172104	
	000430	000774	BR 422

The contents of location 424 contain the desired number to be sent into the processor .

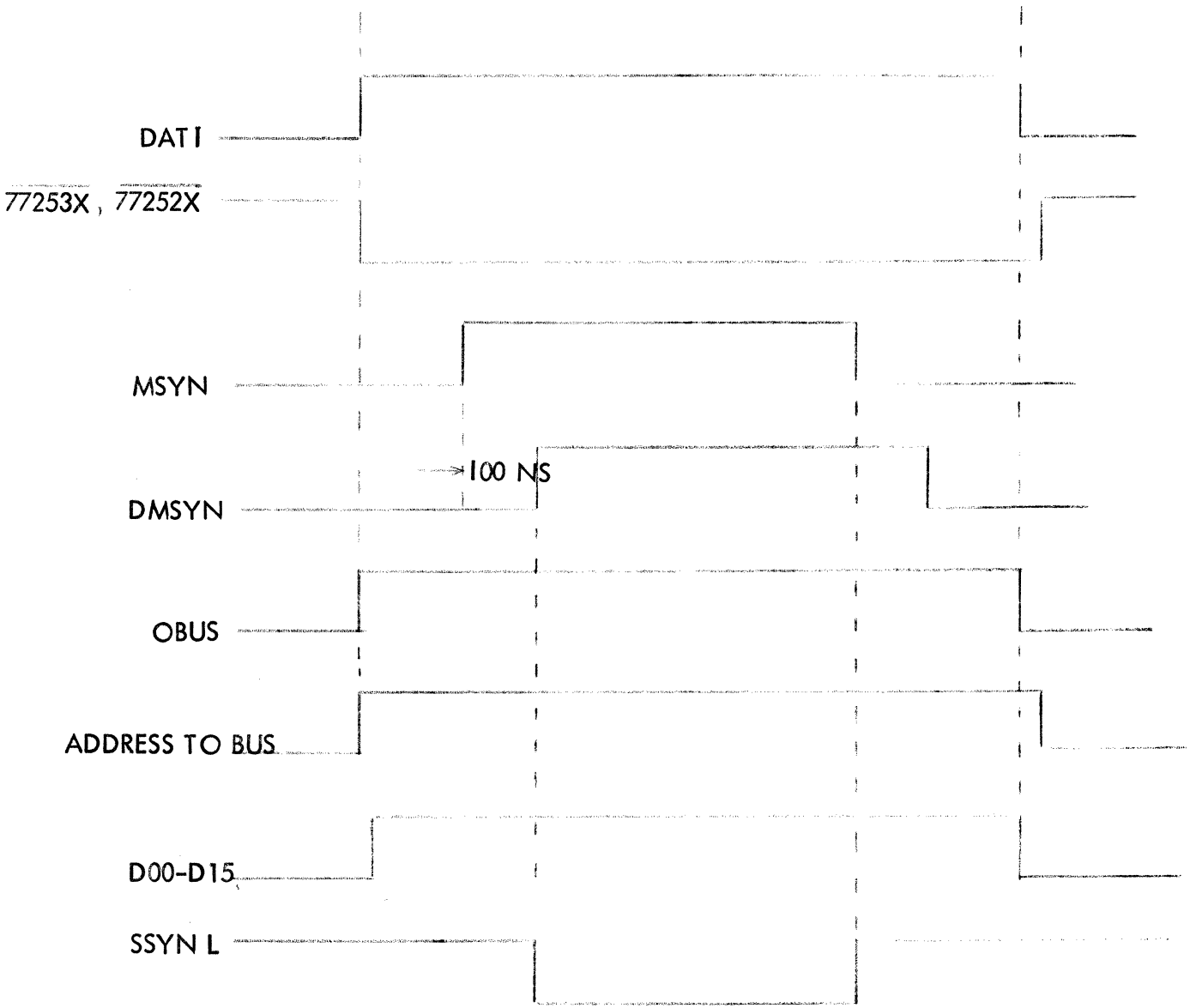
TIMING DIAGRAM 1



NOTES:
1. SEE SPECIAL SCOPE ROUTINE PROGRAMS TO OBSERVE SIGNALS IN CONTROL UNIT.

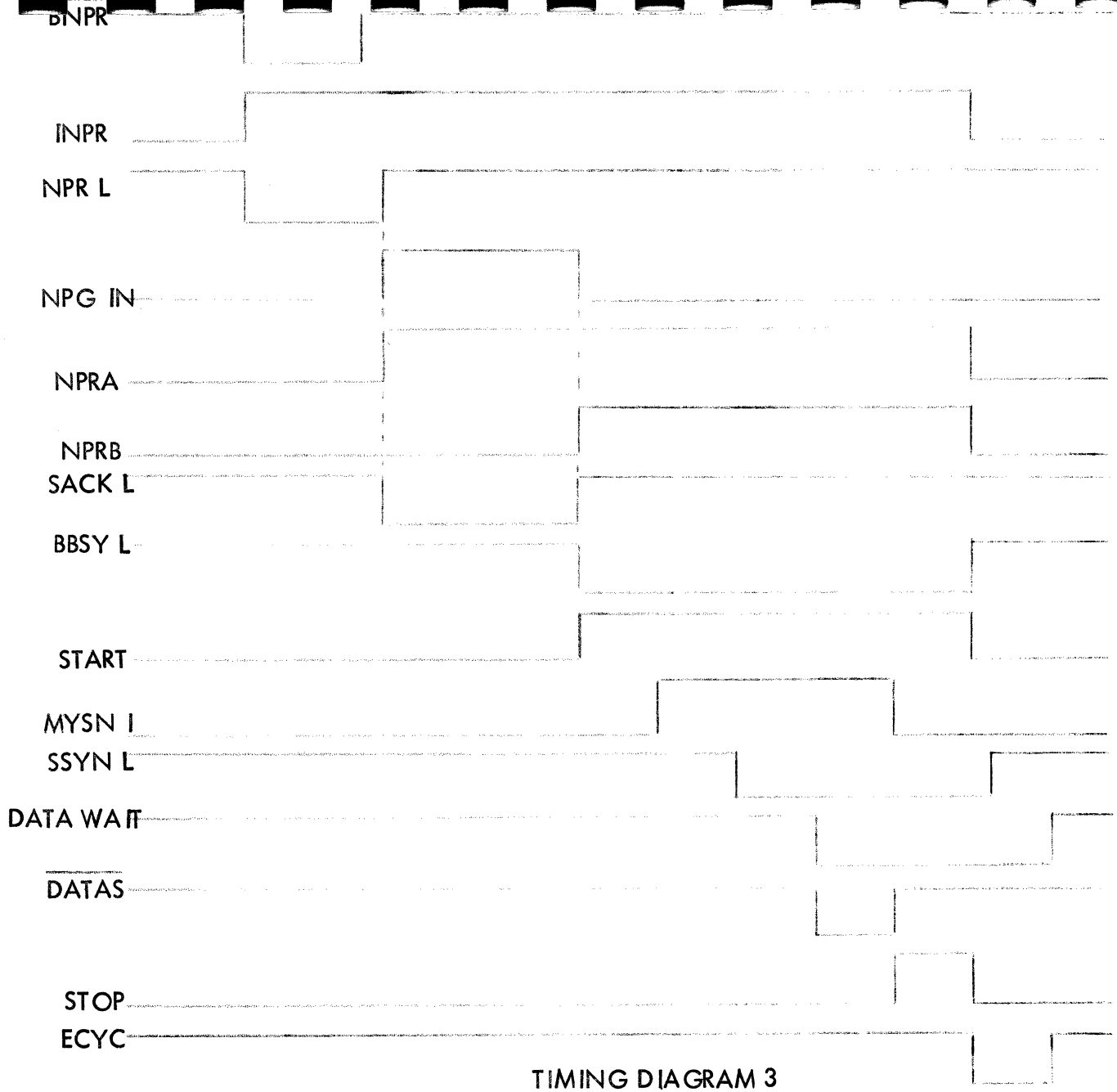
PROCESSOR DATO	DIGI-DATA CORPORATION
	SHEET OF

TIMING DIAGRAM 2



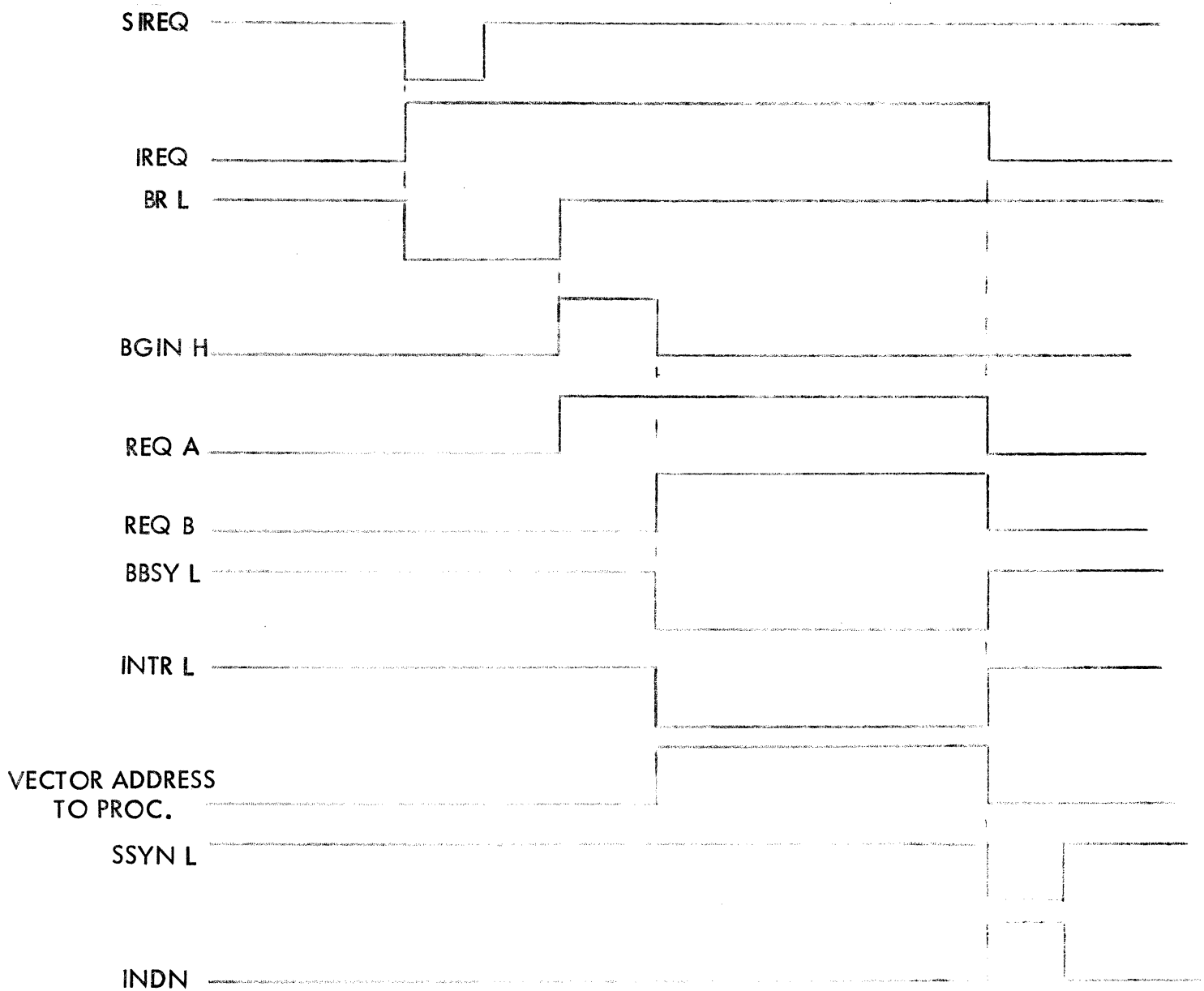
NOTES:
1. SEE SPECIAL SCOPE ROUTINE PROGRAMS TO OBSERVE SIGNALS IN CONTROL UNIT.

PROCESSOR DATI	DIGI-DATA CORPORATION
	SHEET OF



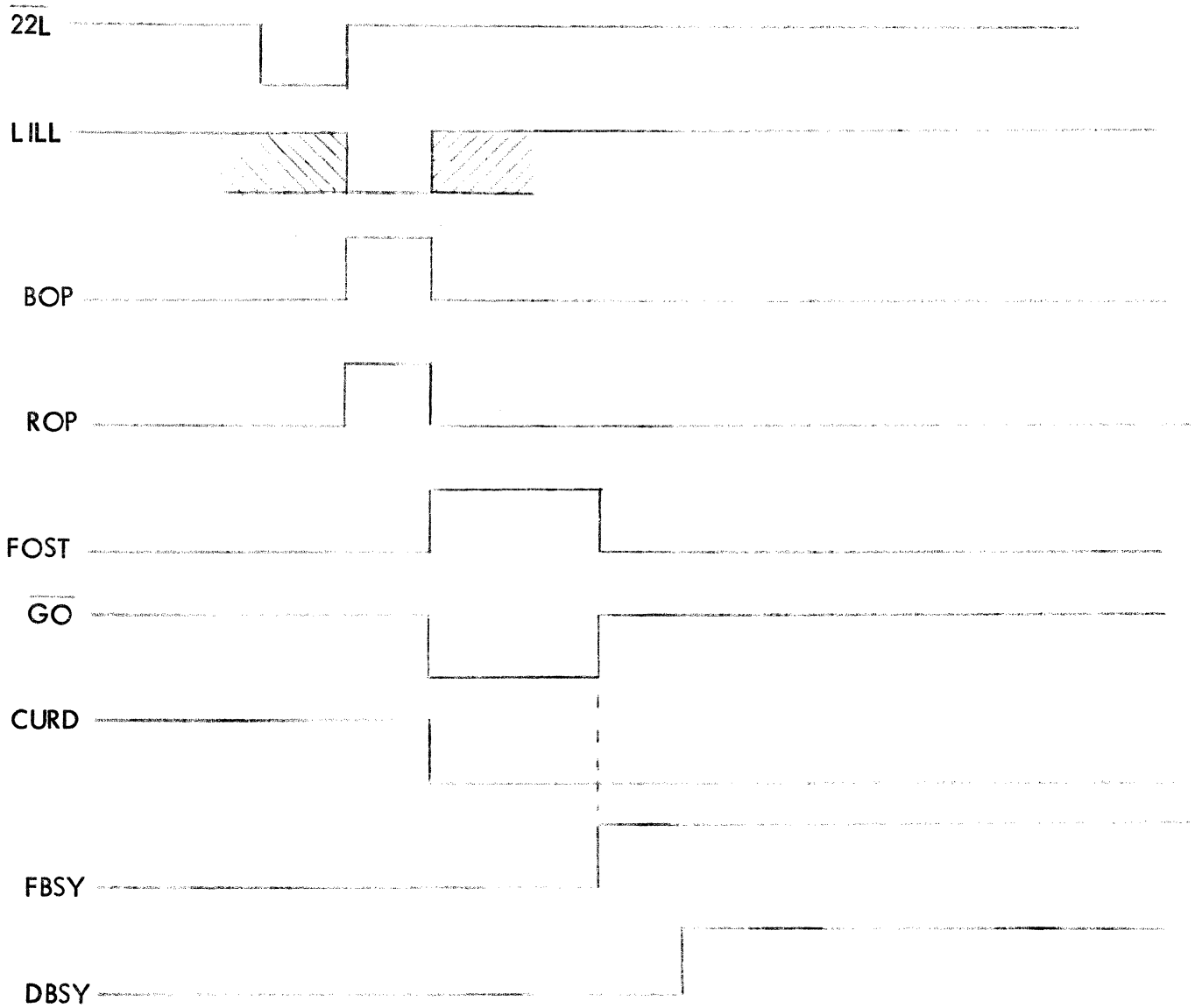
TIMING DIAGRAM 3

NPR TRANSFER	DIGI-DATA CORPORATION
	SHEET OF



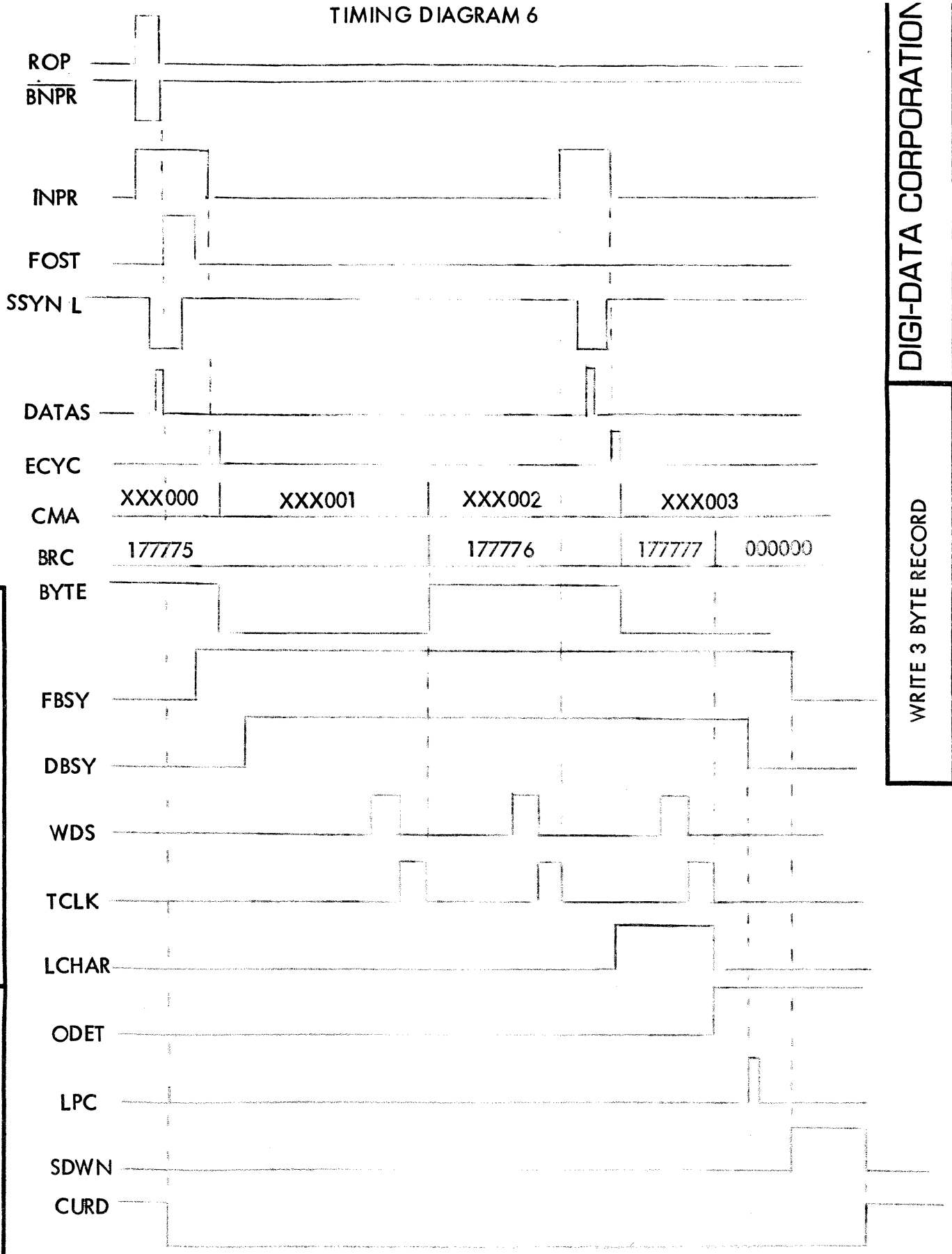
TIMING DIAGRAM 4

INTERRUPTS	DIGI-DATA CORPORATION
	SHEET OF



TIMING DIAGRAM 5

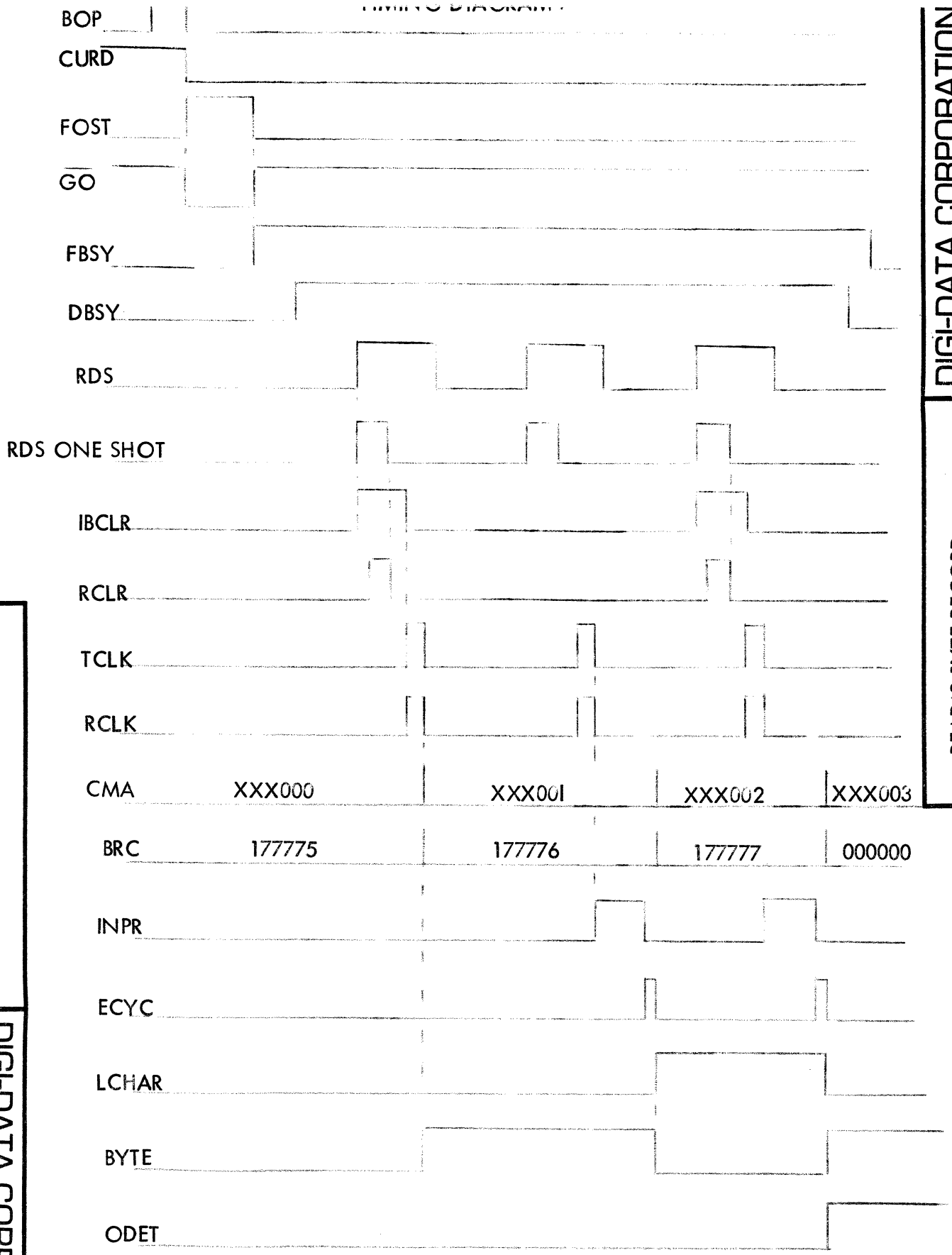
TIMING DIAGRAM 6



NOTES:
1. SEE PROGRAM TO WRITE OR READ 3 BYTE RECORD

TIMING DIAGRAM 7

READ 3 BYTE RECORD

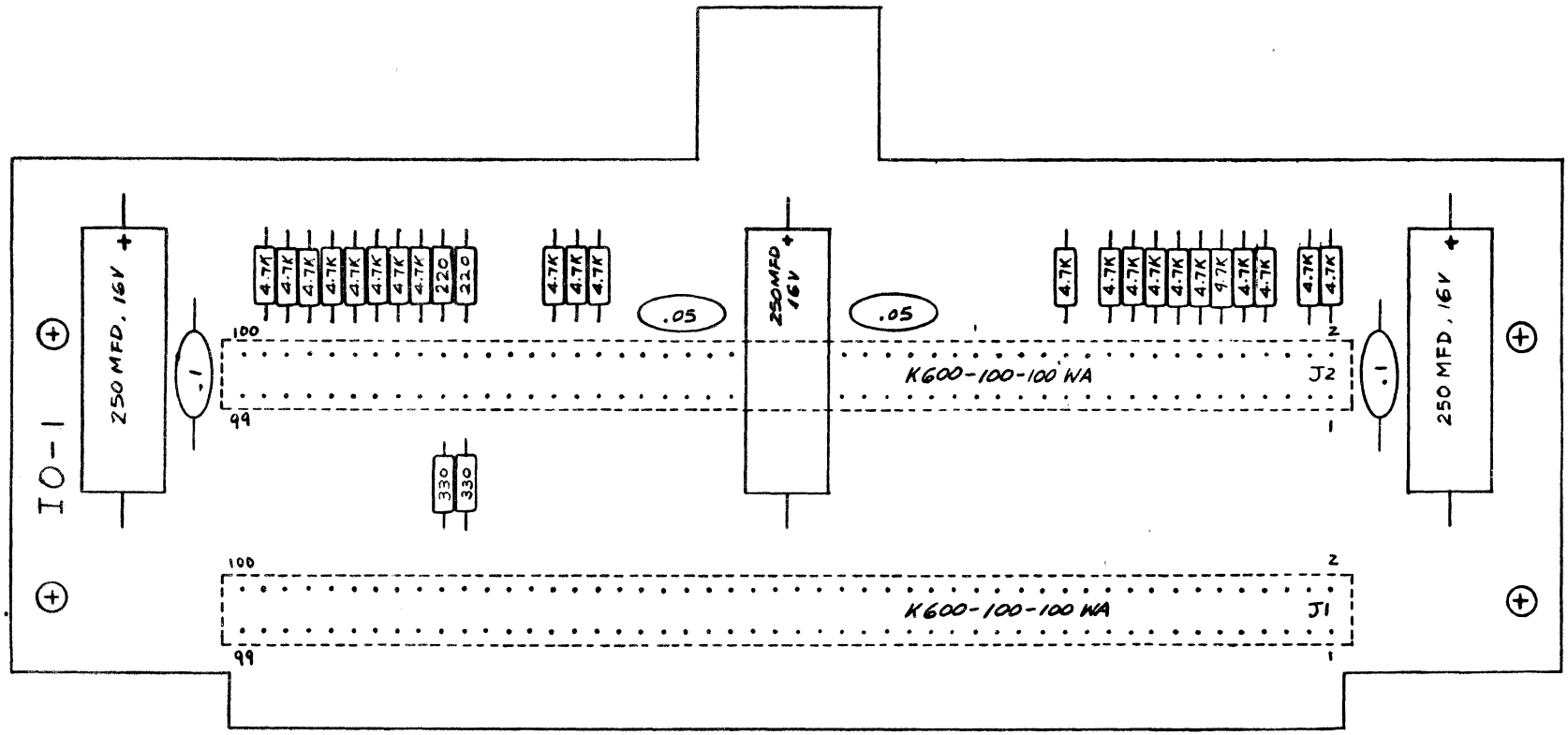


NOTES:
1. SEE PROGRAM TO WRITE OR READ 3 BYTE RECORD

DIGI-DATA CORPORATION
SHEET OF

TIMING DIAGRAM 8

REWIND COMMAND	DIGI-DATA CORPORATION
	SHEET OF

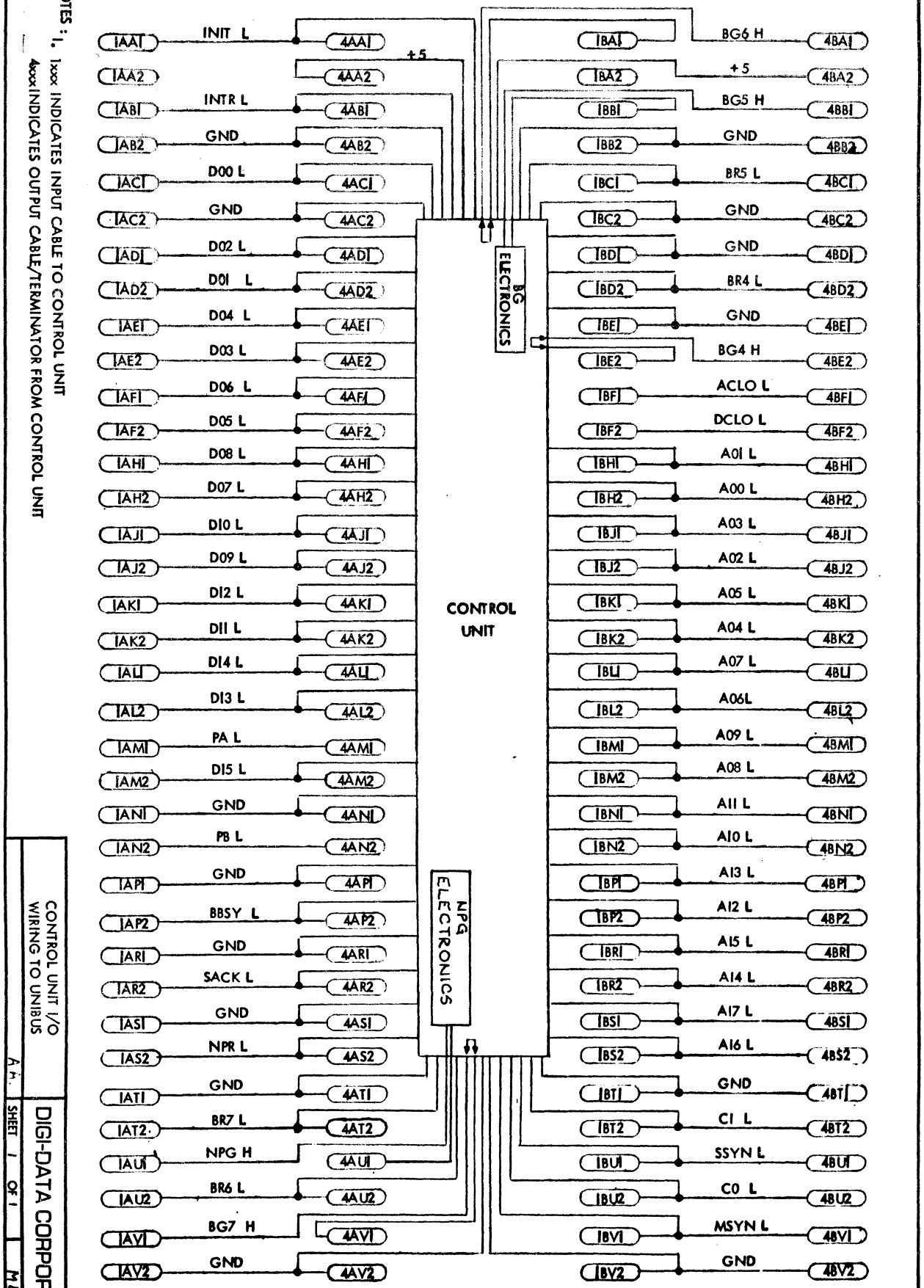


NOTES:

1. PIN 47,48,49,50,51,52,53,54 OF J2 CONNECTOR TO BE CUT OFF AFTER SOLDERING TO THE CORRESPONDING HOLES ON IO-1.
2. ALL RESISTORS ARE IN OHMS, 1/4W, ±5%.
3. ALL CAPACITORS ARE IN MFD.

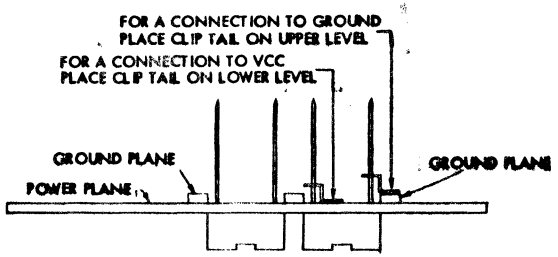
CUT KEY RECEIVING NOTCH BETWEEN PINS 43 & 45, 53 & 55, 61 & 63

ASSEMBLY - IO-1 INTERFACE, CU-PDP/11	DIGI-DATA CORP. REV. A BLADENSBURG, MD.
	SHEET 1 OF 1 | CB-0097

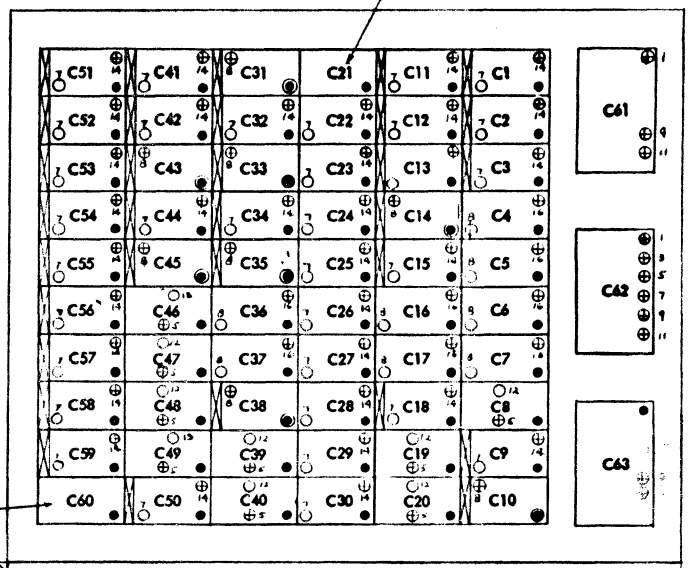

NOTES:
1. 1xxx INDICATES INPUT CABLE TO CONTROL UNIT
4xxx INDICATES OUTPUT CABLE/TERMINATOR FROM CONTROL UNIT
1AAT INIT L
4AA1
1AA2
4AA2
+5
1AB1 INTR L
4AB1
1AB2 GND
4AB2
1AC1 D00 L
4AC1
1AC2 GND
4AC2
1AD1 D02 L
4AD1
1AD2 D01 L
4AD2
1AE1 D04 L
4AE1
1AE2 D03 L
4AE2
1AF1 D06 L
4AF1
1AF2 D05 L
4AF2
1AH1 D08 L
4AH1
1AH2 D07 L
4AH2
1AJ1 D10 L
4AJ1
1AJ2 D09 L
4AJ2
1AK1 D12 L
4AK1
1AK2 D11 L
4AK2
1AL1 D14 L
4AL1
1AL2 D13 L
4AL2
1AM1 PA L
4AM1
1AM2 D15 L
4AM2
1AN1 GND
4AN1
1AN2 PB L
4AN2
1AP1 GND
4AP1
1AP2 BBSY L
4AP2
1AR1 GND
4AR1
1AR2 SACK L
4AR2
1AS1 GND
4AS1
1AS2 NPR L
4AS2
1AT1 GND
4AT1
1AT2 BR7 L
4AT2
1AU1 NPG H
4AU1
1AU2 BR6 L
4AU2
1AV1 BG7 H
4AV1
1AV2 GND
4AV2
BG ELECTRONICS
NPG ELECTRONICS
CONTROL UNIT
1BA1 BG6 H
4BA1
1BA2 +5
4BA2
1BB1 BG5 H
4BB1
1BB2 GND
4BB2
1BC1 BR5 L
4BC1
1BC2 GND
4BC2
1BD1 GND
4BD1
1BD2 BR4 L
4BD2
1BE1 GND
4BE1
1BE2 BG4 H
4BE2
1BF1 ACLO L
4BF1
1BF2 DCLO L
4BF2
1BH1 A01 L
4BH1
1BH2 A00 L
4BH2
1BJ1 A03 L
4BJ1
1BJ2 A02 L
4BJ2
1BK1 A05 L
4BK1
1BK2 A04 L
4BK2
1BL1 A07 L
4BL1
1BL2 A06L
4BL2
1BM1 A09 L
4BM1
1BM2 A08 L
4BM2
1BN1 A11 L
4BN1
1BN2 A10 L
4BN2
1BP1 A13 L
4BP1
1BP2 A12 L
4BP2
1BR1 A15 L
4BR1
1BR2 A14 L
4BR2
1BS1 A17 L
4BS1
1BS2 A16 L
4BS2
1BT1 GND
4BT1
1BT2 CI L
4BT2
1BU1 SSYN L
4BU1
1BU2 CO L
4BU2
1BV1 MSYN L
4BV1
1BV2 GND
4BV2
CONTROL UNIT I/O WIRING TO UNIBUS
DIGI-DATA CORPORATION
SHEET 1 OF 1
M8-0037

NOTES:

1. Pin 8 and Pin 9 to be put on heat shrink tubing
2. ● Pin 1
3. ⬤ Pin 1 to be put on clip to ground plane
4. ○ Pin number indicated to be put on clip to ground plane
5. ⊕ Pin number indicated to be put on clip to power plane

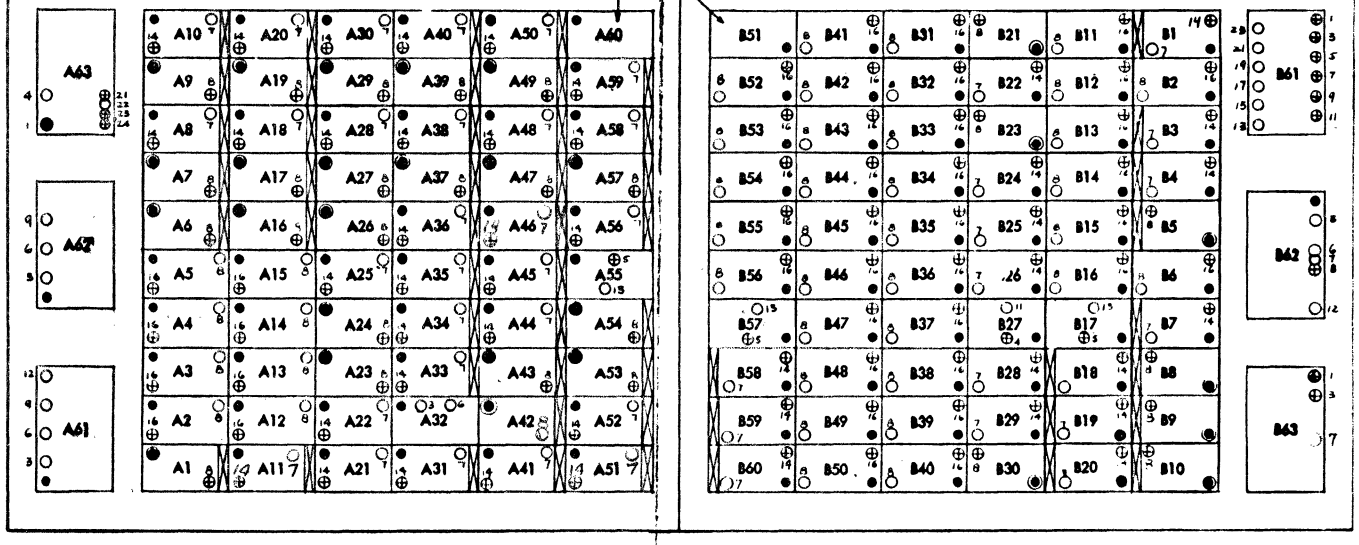


Pin 1 through Pin 7 to be put on clips to power plane
Pin 8 through Pin 14 to be put on clips to ground plane



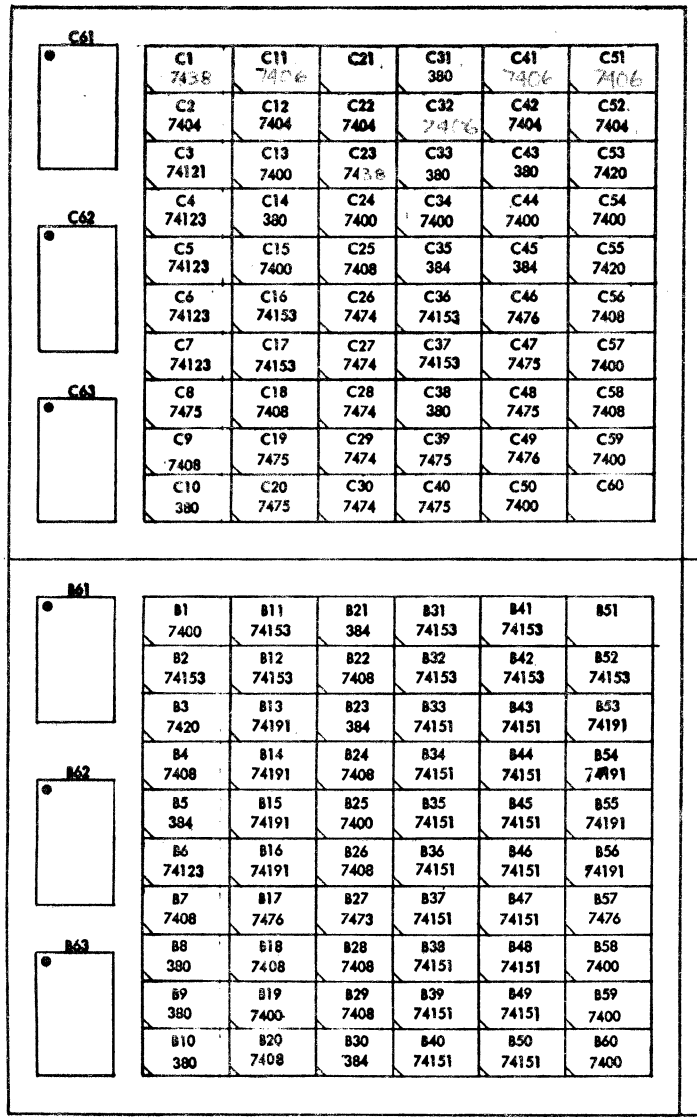
INTERDYNE PROTOWRAP KIT, #5824-63 (3 REQD.)
PIN SIDE SHOWN

Pin 1 through Pin 8 to be put on clips to power plane
Pin 9 through Pin 16 to be put on clips to ground plane



DIGI-DATA CORP.
BLADENSBURG, MD.

ASSEMBLY –
INTERFACE, CU - PDP/11
POWER & GROUND
MC - 0045



C61					
C1 7438	C11 7406	C21	C31 380	C41 7406	C51 7406
C2 7404	C12 7404	C22 7404	C32 7406	C42 7404	C52 7404
C3 74121	C13 7400	C23 7438	C33 380	C43 380	C53 7420
C4 74123	C14 380	C24 7400	C34 7400	C44 7400	C54 7400
C5 74123	C15 7400	C25 7408	C35 384	C45 384	C55 7420
C6 74123	C16 74153	C26 7474	C36 74153	C46 7476	C56 7408
C7 74123	C17 74153	C27 7474	C37 74153	C47 7475	C57 7400
C8 7475	C18 7408	C28 7474	C38 380	C48 7475	C58 7408
C9 7408	C19 7475	C29 7474	C39 7475	C49 7476	C59 7400
C10 380	C20 7475	C30 7474	C40 7475	C50 7400	C60

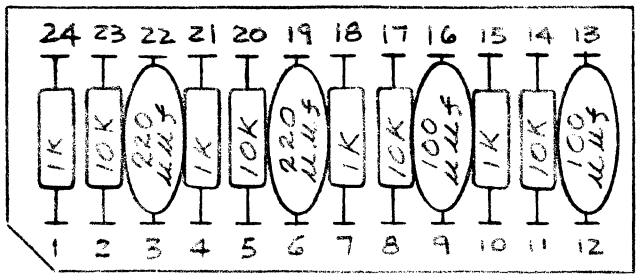
B61					
B1 7400	B11 74153	B21 384	B31 74153	B41 74153	B51
B2 74153	B12 74153	B22 7408	B32 74153	B42 74153	B52 74153
B3 7420	B13 74191	B23 384	B33 74151	B43 74151	B53 74191
B4 7408	B14 74191	B24 7408	B34 74151	B44 74151	B54 74191
B5 384	B15 74191	B25 7400	B35 74151	B45 74151	B55 74191
B6 74123	B16 74191	B26 7408	B36 74151	B46 74151	B56 74191
B7 7408	B17 7476	B27 7473	B37 74151	B47 74151	B57 7476
B8 380	B18 7408	B28 7408	B38 74151	B48 74151	B58 7400
B9 380	B19 7400	B29 7408	B39 74151	B49 74151	B59 7400
B10 380	B20 7408	B30 384	B40 74151	B50 74151	B60 7400

A60	A50 8881	A40 8881	A30 8881	A20 8881	A10 8881	A63
A59 8881	A49 380	A39 380	A29 380	A19 380	A9 380	
A58 8881	A48 8881	A38 8881	A28 8881	A18 8881	A8 8881	
A57 380	A47 380	A37 380	A27 380	A17 380	A7 380	A62
A56 7408	A46 7400	A36 7474	A26 380	A16 384	A6 384	
A55 7476	A45 7408	A35 7474	A25 7400	A15 7442	A5 7442	
A54 380	A44 7400	A34 7474	A24 384	A14 7442	A4 7442	
A53 380	A43 384	A33 7474	A23 384	A13 7442	A3 7442	A61
A52 7400	A42 380	A32	A22 7408	A12 7442	A2 7442	
A51 7414	A41 7400	A31 7400	A21 7400	A11 7432	A1 384	

DIGI-DATA CORP.
BLADENSBURG, MD

ASSEMBLY- MAIN BOARD
INTERFACE CU-PDP/11

MC-0047



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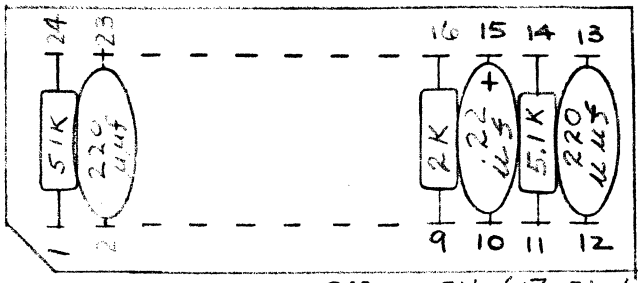

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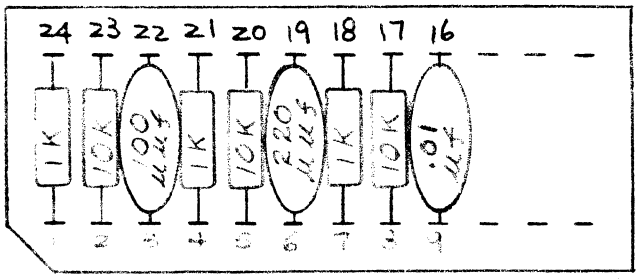

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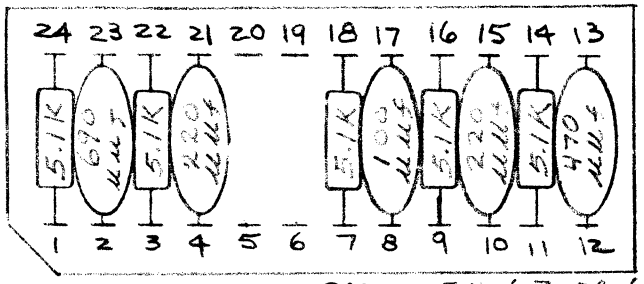

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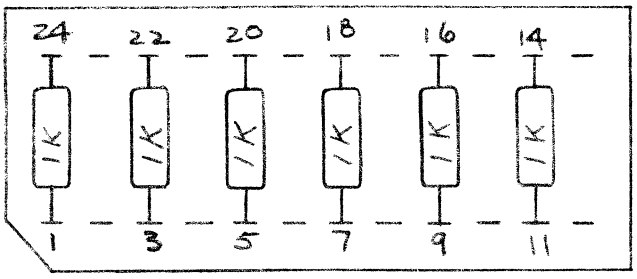

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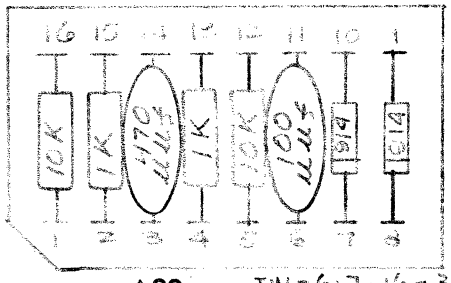

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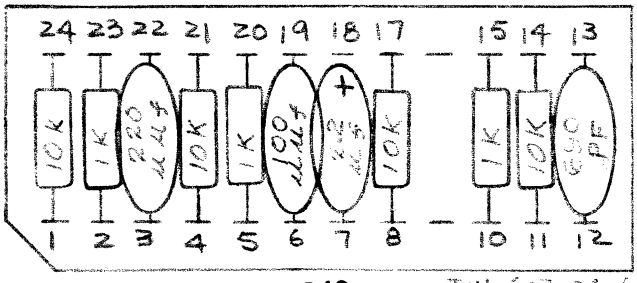

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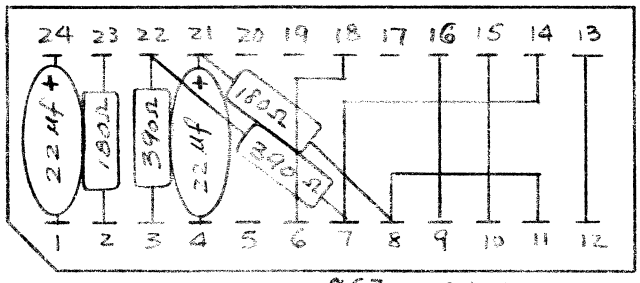

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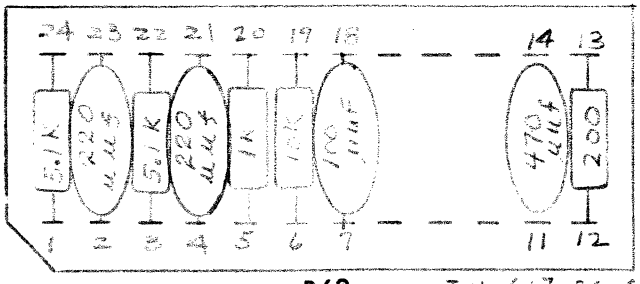


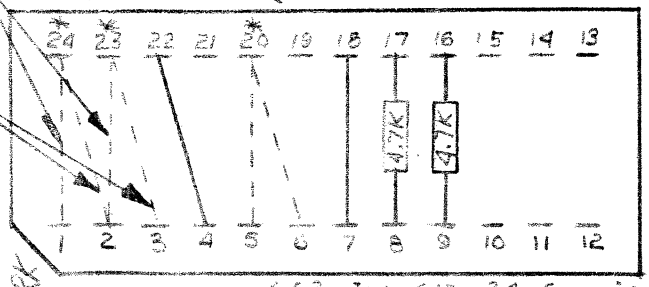
B63 IW-617-24-6

FOR 556, 200 BPI 7TRK ONLY

FOR 800, 556 BPI 7TRK ONLY

SEE NOTE 1

SEE NOTE 2



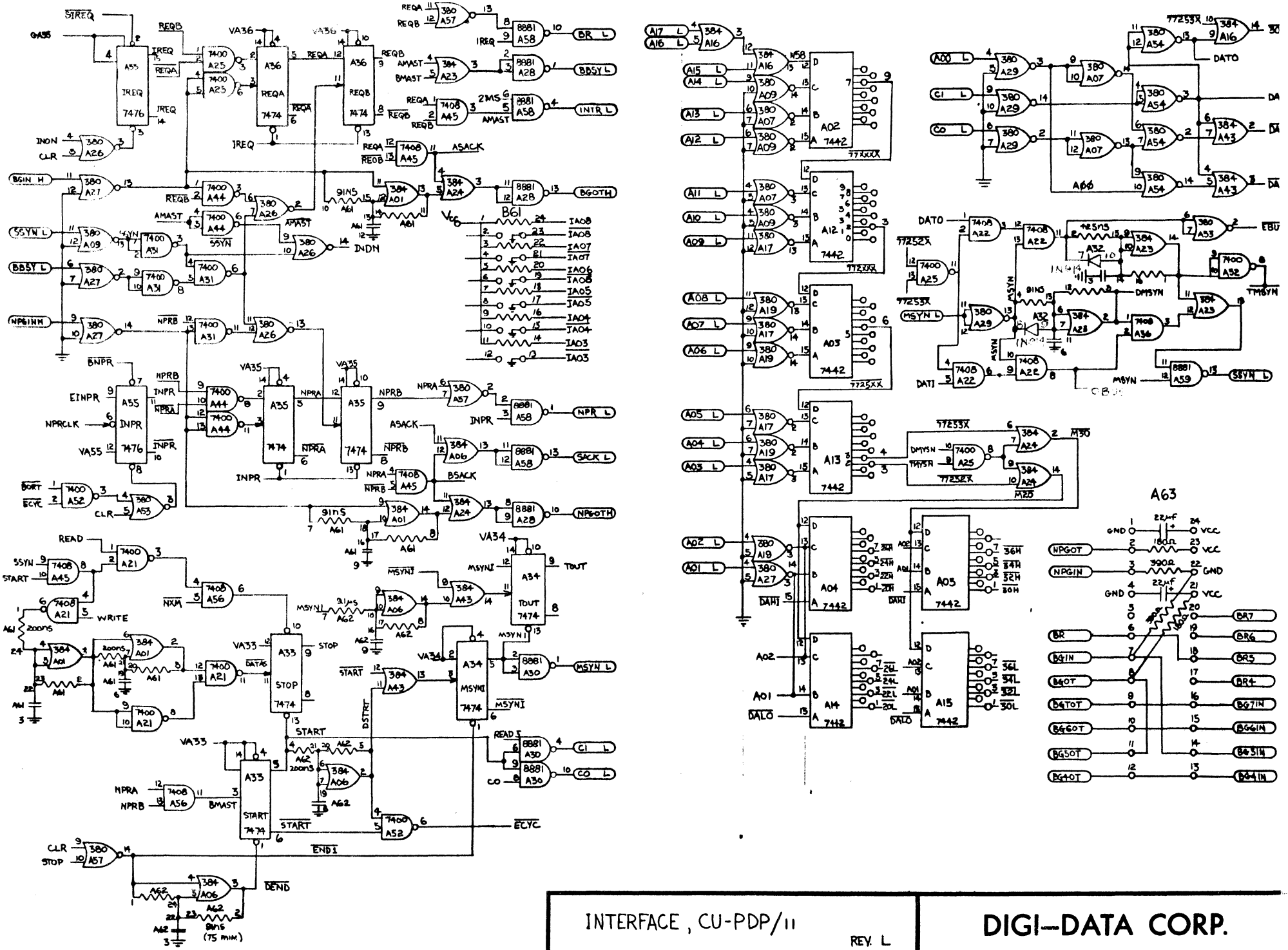
C63 IW-617-24-6

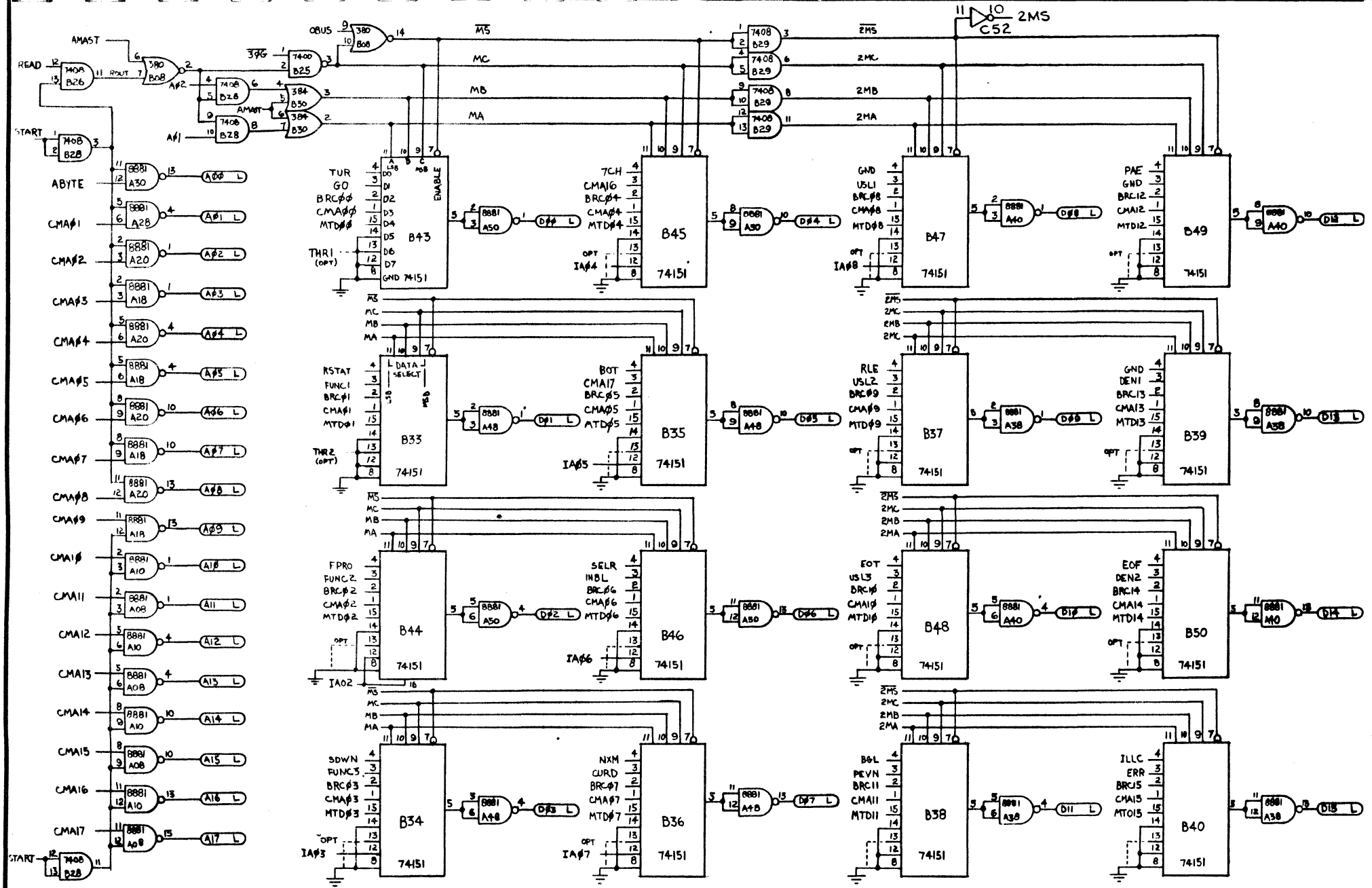
NOTES:
1. INSTALL JUMPERS TO C63-23,24 FOR 7TRK ONLY
2. FOR DUAL DENSITY(NRZI&PE) INSTALL JUMPER BETWEEN C63-6 & 20, OTHERWISE JUMPER C63-5 & 20

ASSEMBLY- INTERFACE, CU- PDP/11

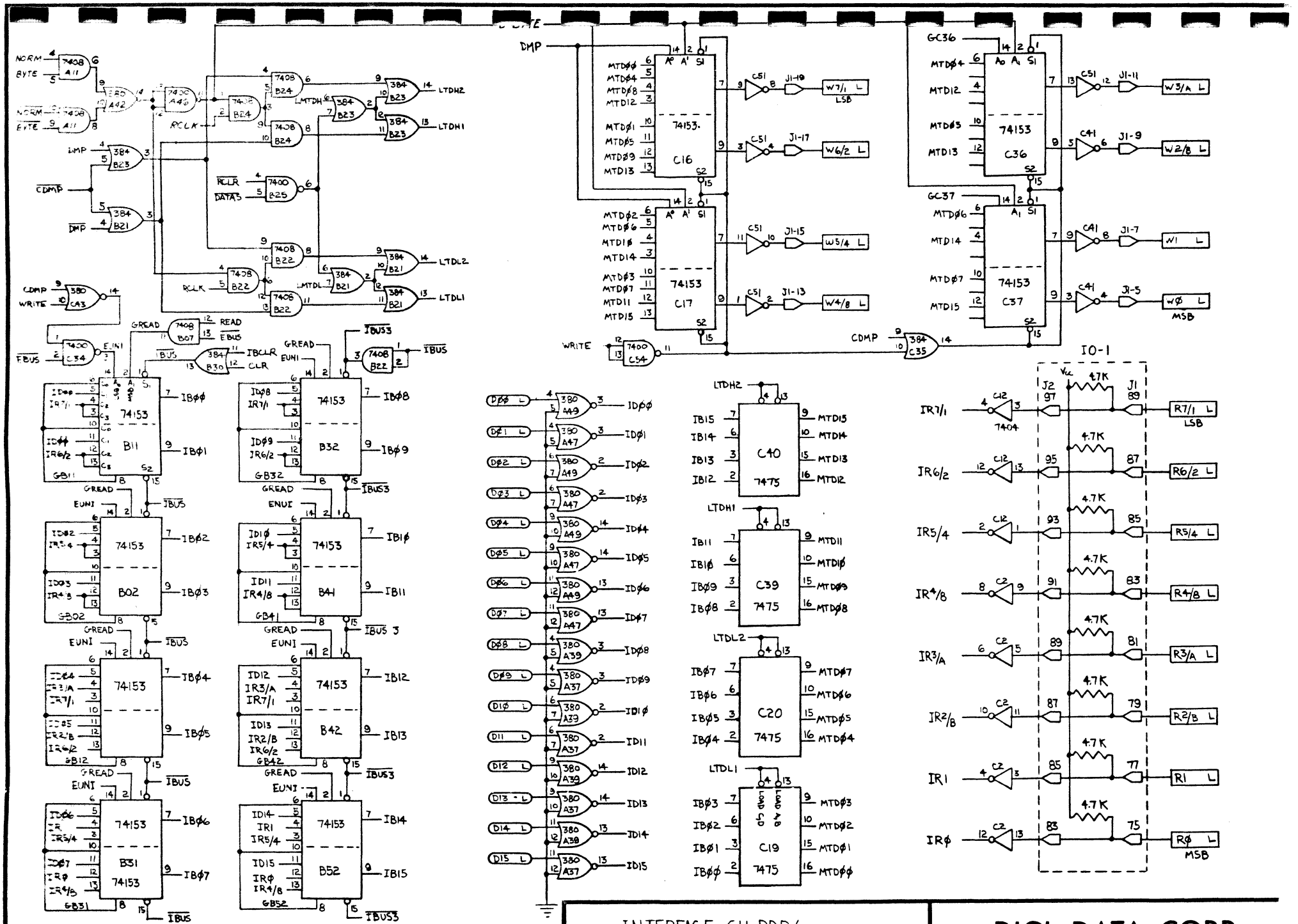
DIGI-DATA CORPORATION

REV K | SHEET 1 OF 1 | MA-0035


INTERFACE , CU-PDP/11
REV. L
DIGI-DATA CORP.
11/ /73
RFL
SHEET 1 OF 7
LC - 0136



INTERFACE, CU-PDP/11 REV L		DIGI–DATA CORP.
	SHEET 2 OF 7	LC - 0136



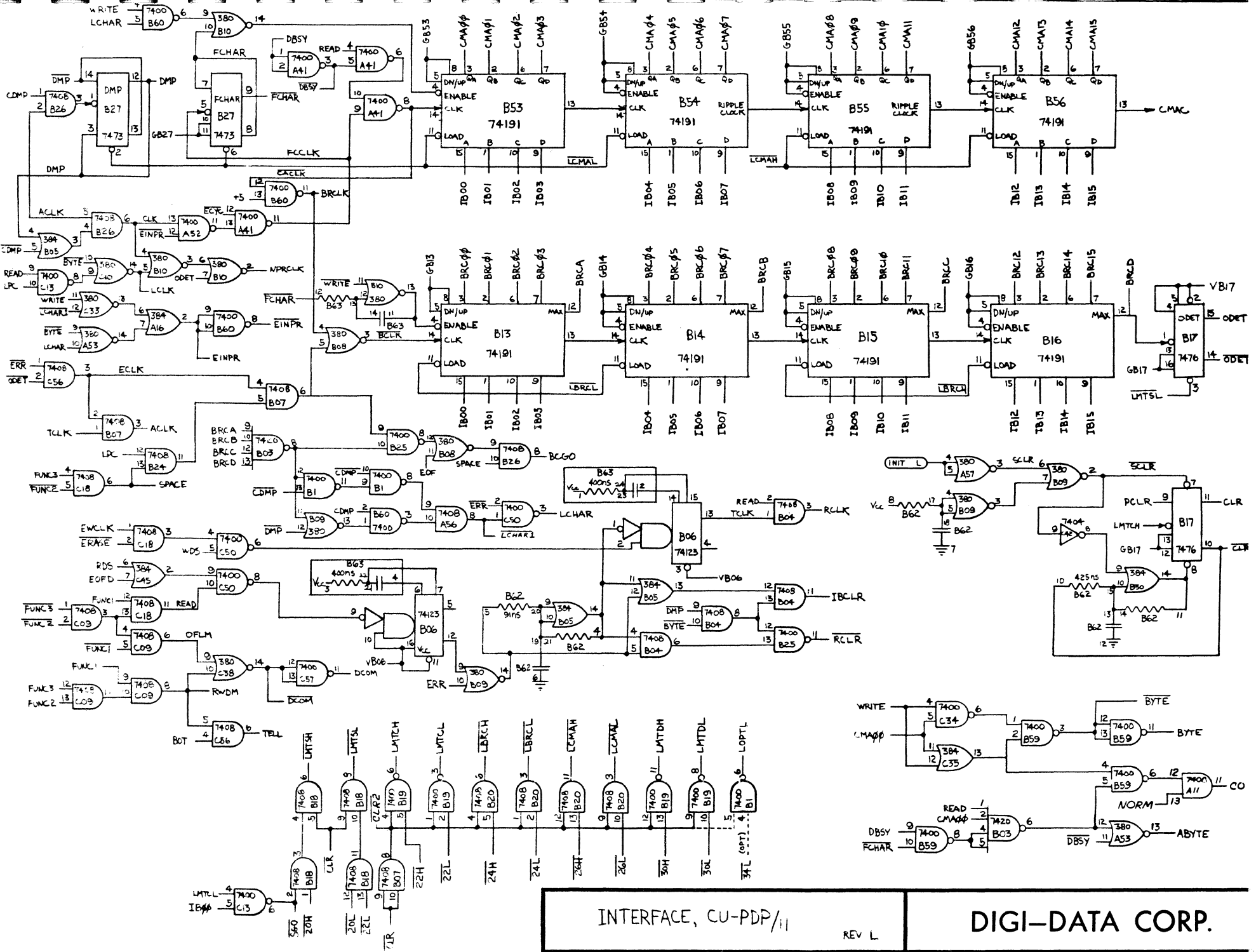
INTERFACE, CU-PDP/11

PE / L

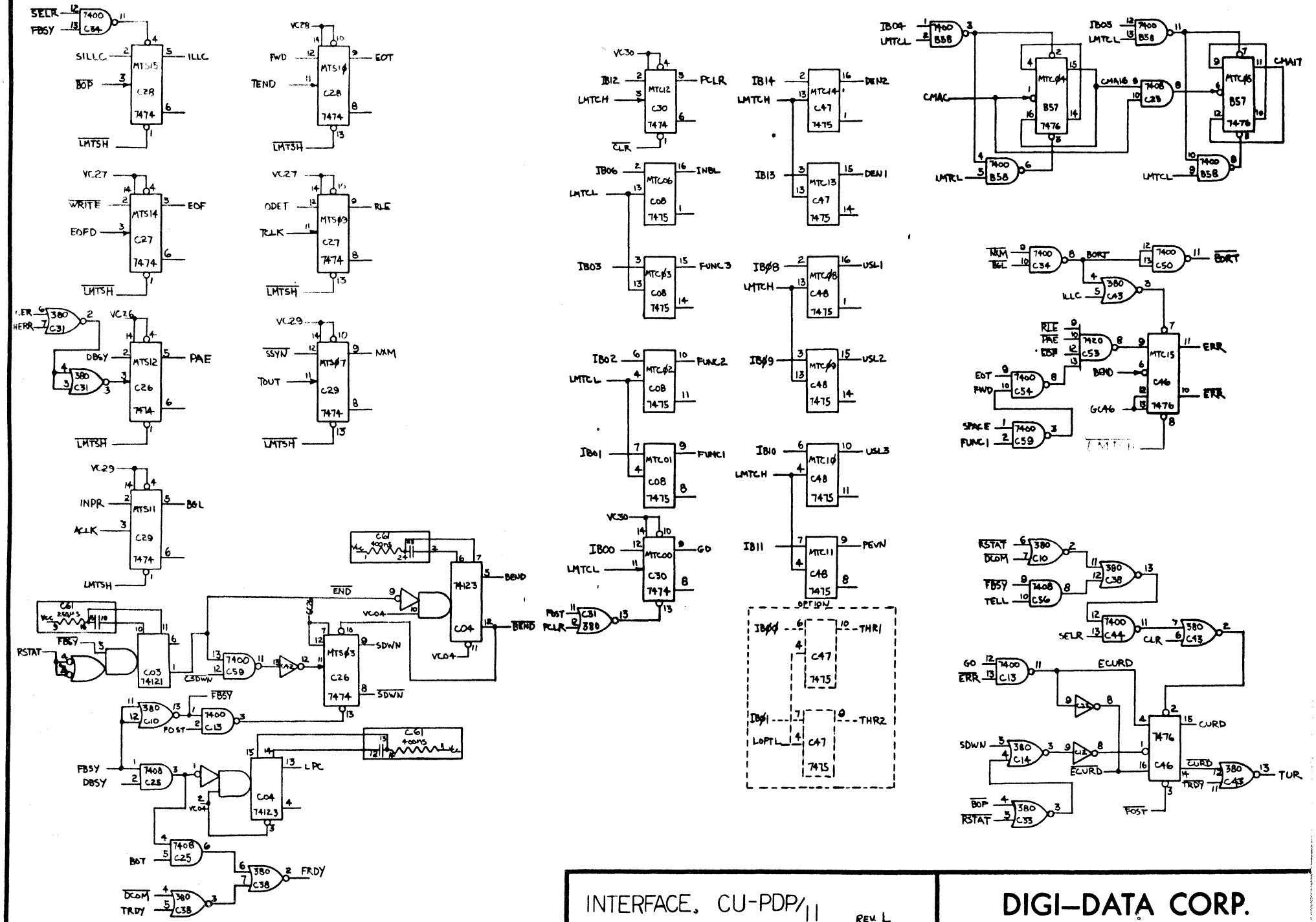
DIGI–DATA CORP.

SHEET 3 OF 7

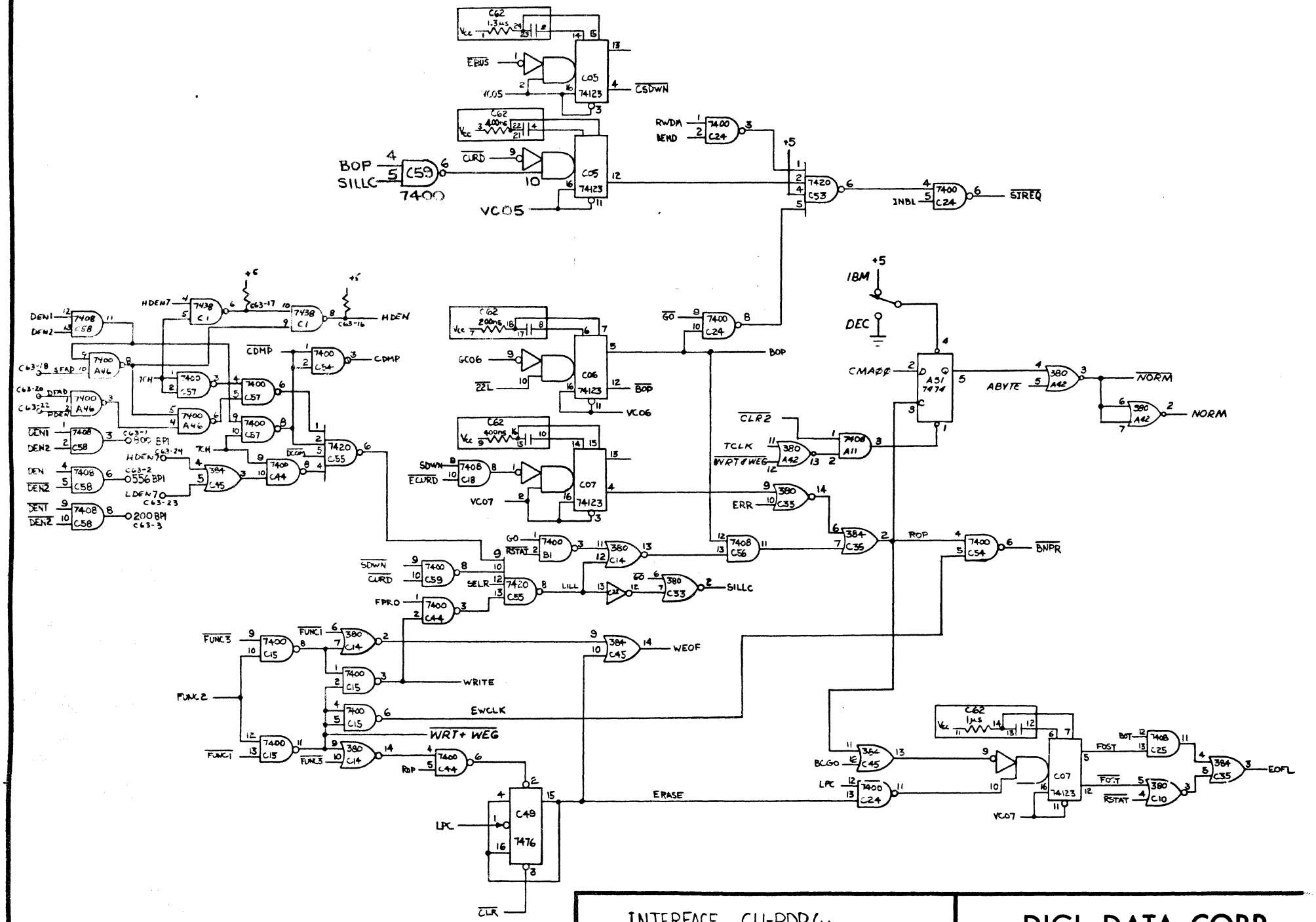
LC - 0136



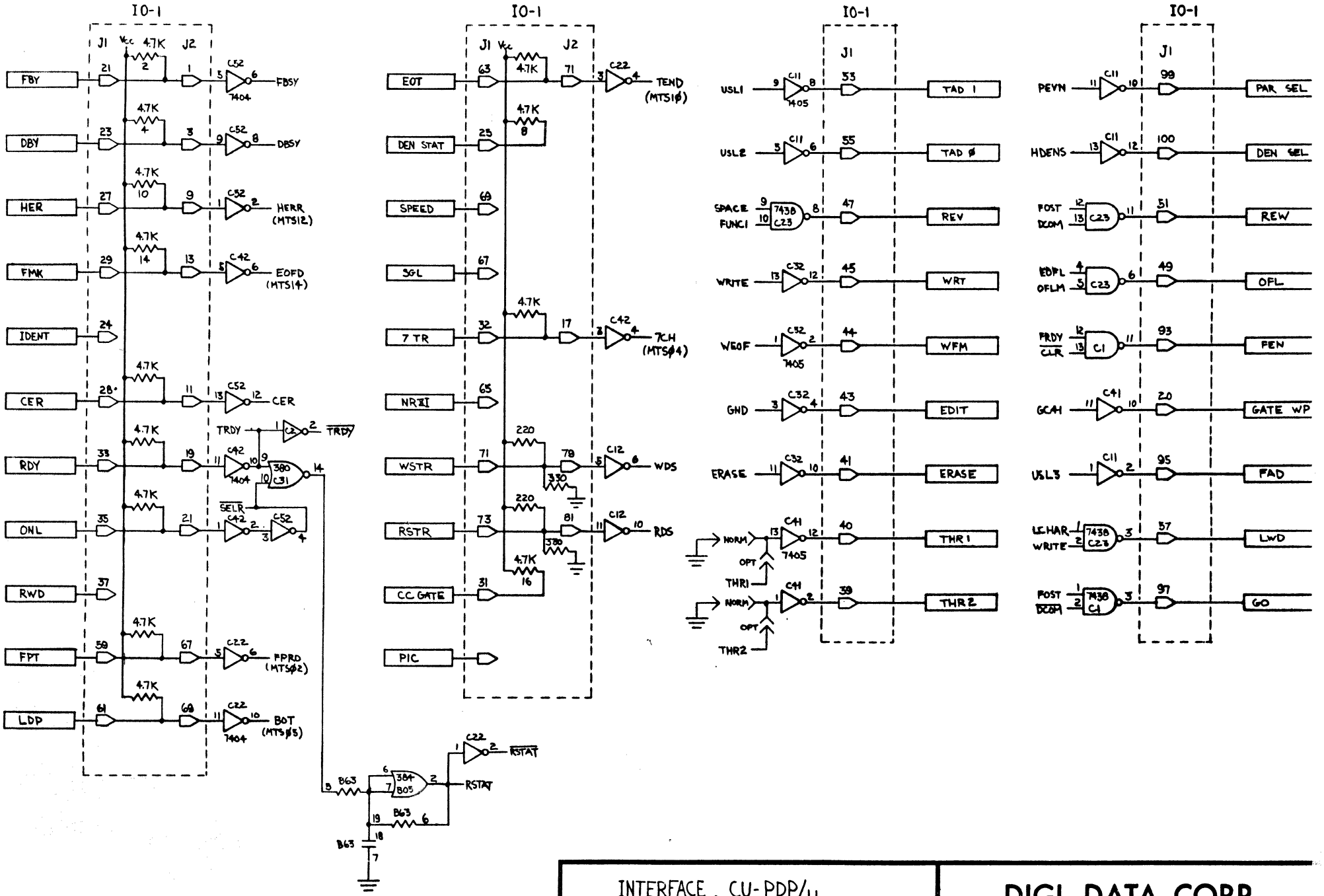
INTERFACE, CU-PDP/11 REV L		DIGI–DATA CORP.
11/73	RFL	SHEET 4 OF 7
		LC - 0136



INTERFACE. CU-PDP/11 REV L		DIGI-DATA CORP.
11/12/73 RFL	SHEET 5 OF 7	LC-0136



INTERFACE, CU-PDP/11 REV L		DIGI–DATA CORP.
11-15-73	RFL	SHEET 6 OF 7
		LC - 0136



INTERFACE, CU-PDP/11 REV L		DIGI–DATA CORP.	
11-73	RFL	SHEET 7 OF 7	LC - 0136