

Kretsschema ABC1600

Följande innehållsförteckning anger schemablad och deras huvudfunktion.

Datordel

Schemablad nr	Funktion	Sida
1	Klockgenerering datordel	
2	CPU och bootprom	
3	Funktionsavkodning och "bus error"	
4	MAC del 1	
5	MAC del 2	
6	Adressbuffertar mot videokort	
7	RAM datakanaler och "refresh"-räknare	
8	RAM adressmultiplexer	
9	RAM block 0	
10	RAM block 1	
11	RAM block 2	
12	RAM block 3	
13	RAM kontrolldel	
14	NMI + Paritet + CAUSE-register	
15	Reset	
16	I/O-avkodning	
17	Int. ack. + externbuss I/O	
18	CIO + CMOS-kalender + NVRAM	
19	SCC + DART - seriell kommunikation	
20	Flexskiveinterface del 1	
21	Flexskiveinterface del 2	
22	DMA kontroll + Z80-strobar	
23	DMA 0	
24	DMA 1	
25	DMA 2	
26	DMA-map	
100	Kontaktidon flexskiveenhet	
101	Kontaktidon seriell kommunikation	
102	Kontaktidon busskort + spänning	
103	Kontaktidon videokort	

Videodel

1	Grafikminne och buffertar del 1	
2	Grafikminne och buffertar del 2	
3	Adressmultiplexer del 1	
4	Adressmultiplexer del 2	
5	Klockgenerering videodel	
6	Sekvenskontroll	
7	Video-skiftregister	
8	CRTC + synk-signaler	
9	CPU-datakanaler + statusbitar	
10	Minnesadress-avkodning + kvittens	
11	I/O-adressavkodning + flaggregister	
12	Mover: cirkelskiftare	
13	Mover: mixer	
14	Mover: sekvenskontroll	
15	Mover: sekvensavkodning	
16	Mover: från-adress X-led + Y-led	

Videodel forts.

Schemabladd nr	Funktion	Sida
17	Mover: till-adress Y-led	
18	Mover: storlek + jämförare Y-led	
19	Mover: storlek + adress X-led	
20	Mover: jämförare X-led	
21	Mover: skrivmask + skiftfaktor	
100	Kontaktton dator del, videosignal, resetkort och spänning	

Busskort

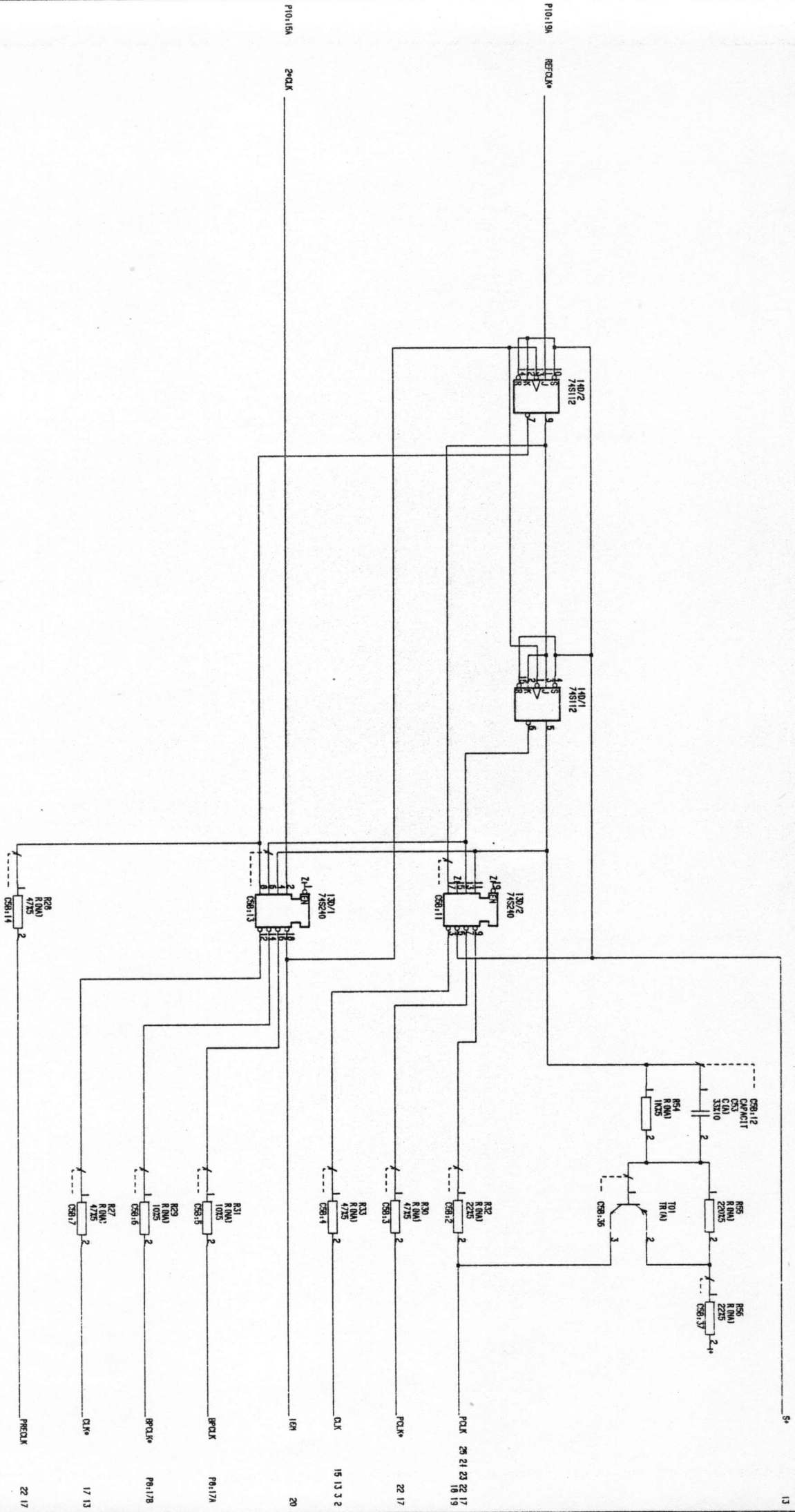
1	CSB-signaler + signalavkodning	
2	Kortval + strobar, buss 0 intern och extern	
3	Kortval + strobar, buss 1 och 2	
100	Kontaktton dator del	
101	Kontaktton buss 0 intern och extern	
102	kontaktton buss 1 och 2	

V24-kort

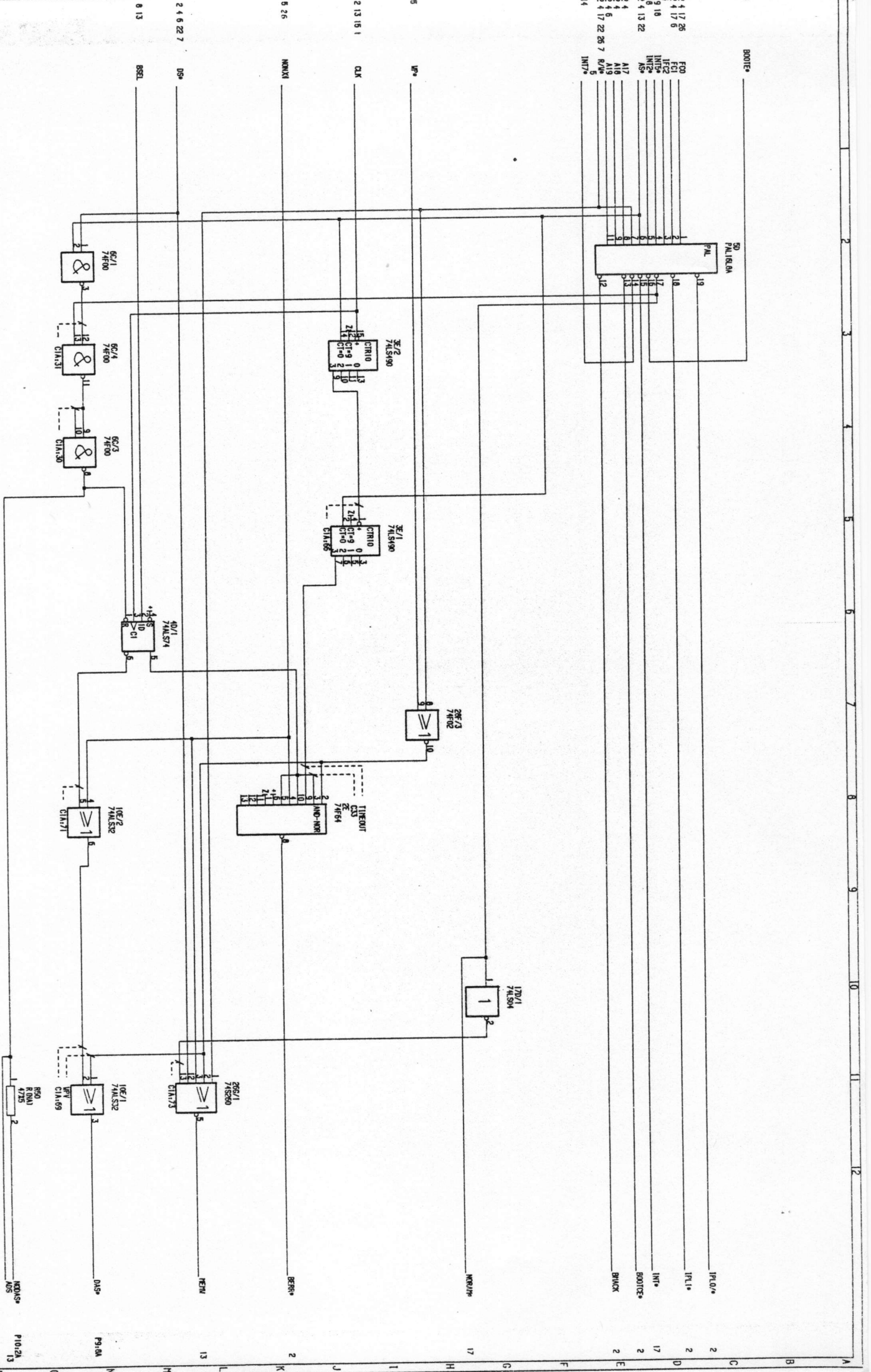
1	Buffertar + byglingar	
100	Kontaktton dator del + serieport	

Resetkort

1	Tryckknapp + kontaktton	
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DRG	1985-12-20	clock signal
ABC1600		CIRCUIT DIAGRAM
DATE		
DESIGNER		
CHECKED		
APPROVED		



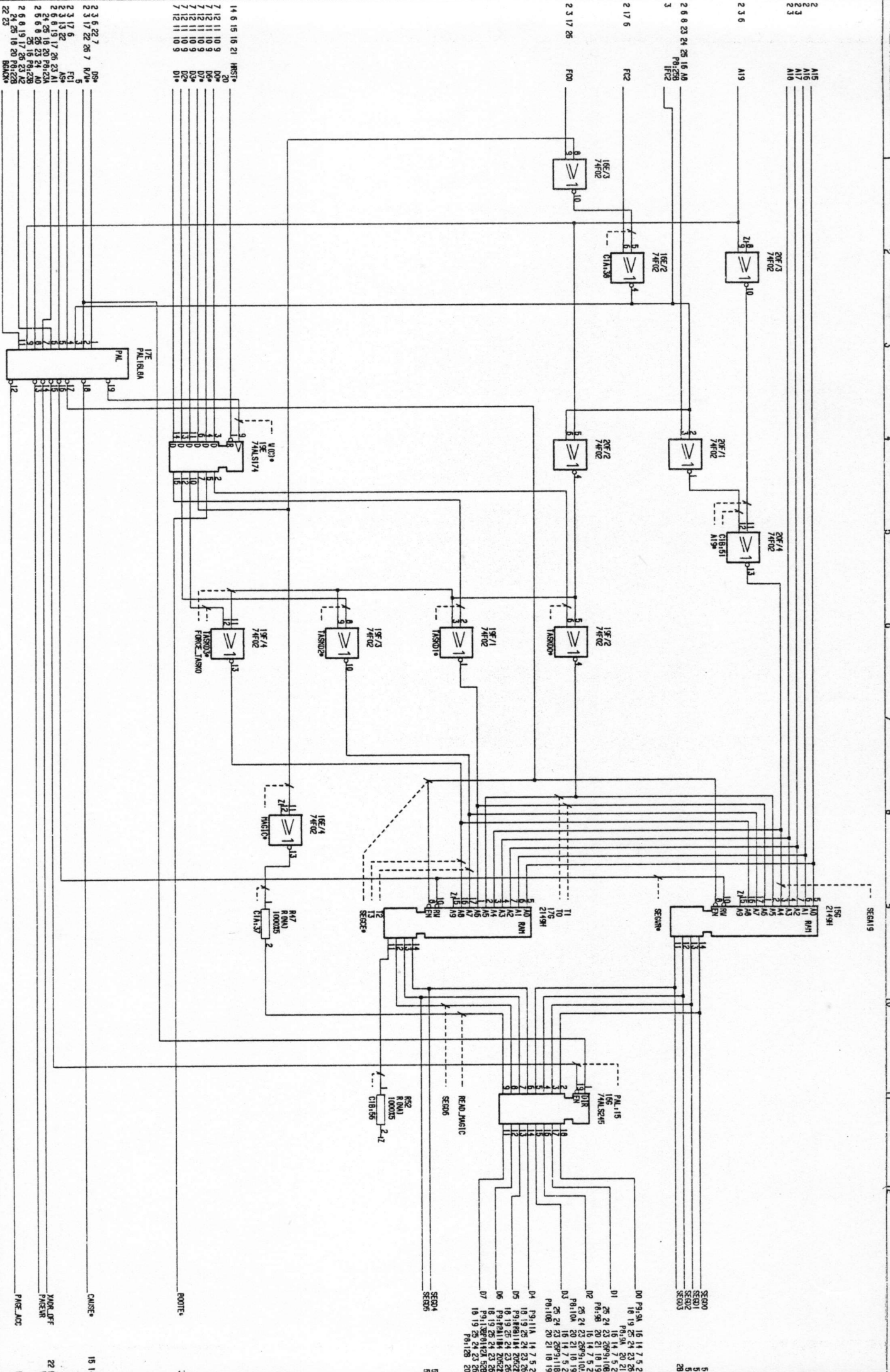
5D PAL16L8M

Pin	Signal
1	INT1*
2	INT2*
3	INT3*
4	INT4*
5	INT5*
6	INT6*
7	INT7*
8	INT8*
9	INT9*
10	INT10*
11	INT11*
12	INT12*
13	INT13*
14	INT14*

Pin	Signal
15	INT15*
16	INT16*
17	INT17*
18	INT18*
19	INT19*
20	INT20*
21	INT21*
22	INT22*
23	INT23*
24	INT24*
25	INT25*
26	INT26*
27	INT27*
28	INT28*
29	INT29*
30	INT30*
31	INT31*
32	INT32*
33	INT33*
34	INT34*
35	INT35*
36	INT36*
37	INT37*
38	INT38*
39	INT39*
40	INT40*
41	INT41*
42	INT42*
43	INT43*
44	INT44*
45	INT45*
46	INT46*
47	INT47*
48	INT48*
49	INT49*
50	INT50*
51	INT51*
52	INT52*
53	INT53*
54	INT54*
55	INT55*
56	INT56*
57	INT57*
58	INT58*
59	INT59*
60	INT60*
61	INT61*
62	INT62*
63	INT63*
64	INT64*
65	INT65*
66	INT66*
67	INT67*
68	INT68*
69	INT69*
70	INT70*
71	INT71*
72	INT72*
73	INT73*
74	INT74*
75	INT75*
76	INT76*
77	INT77*
78	INT78*
79	INT79*
80	INT80*
81	INT81*
82	INT82*
83	INT83*
84	INT84*
85	INT85*
86	INT86*
87	INT87*
88	INT88*
89	INT89*
90	INT90*
91	INT91*
92	INT92*
93	INT93*
94	INT94*
95	INT95*
96	INT96*
97	INT97*
98	INT98*
99	INT99*
100	INT100*

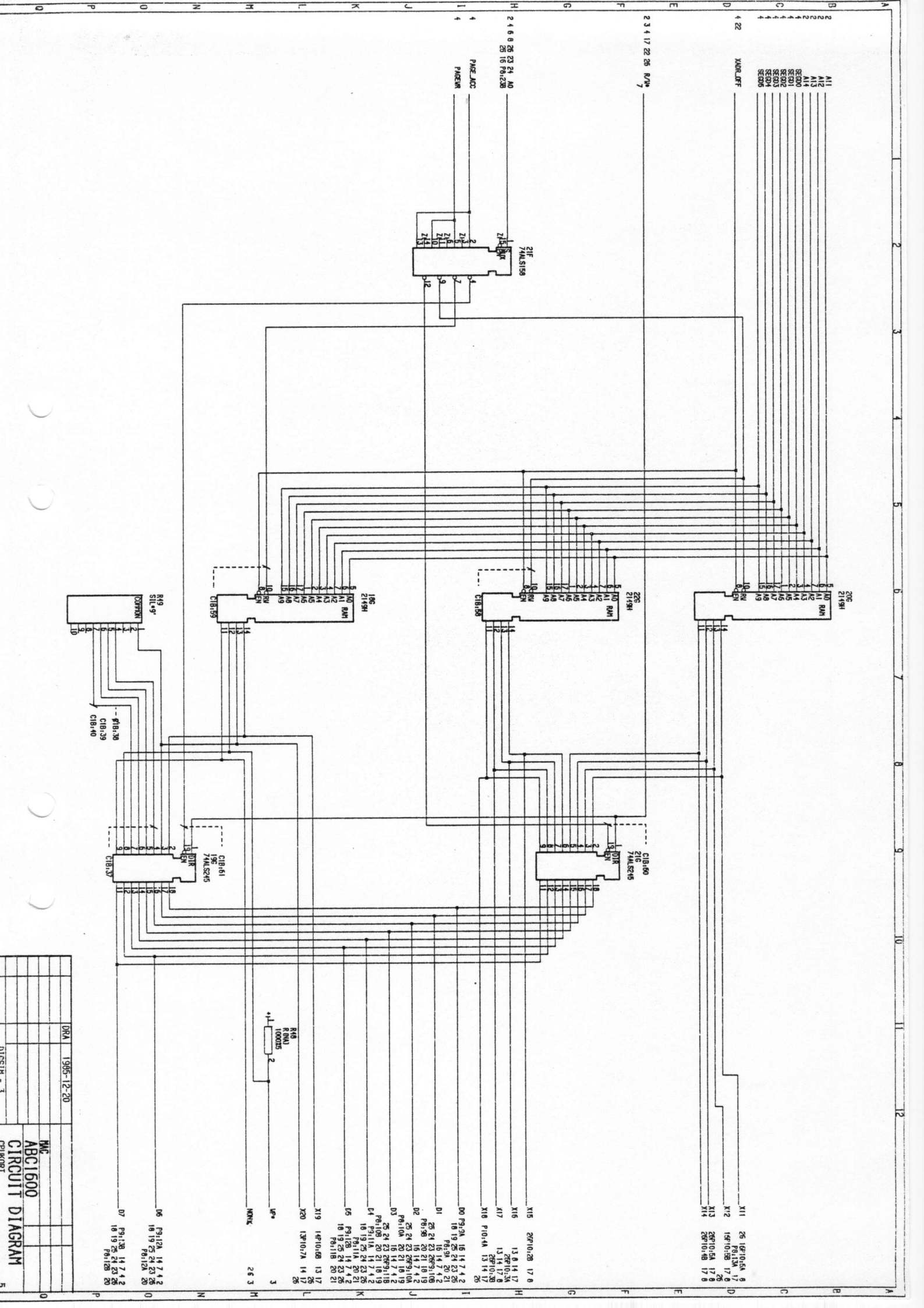
Pin	Signal
1	INT1*
2	INT2*
3	INT3*
4	INT4*
5	INT5*
6	INT6*
7	INT7*
8	INT8*
9	INT9*
10	INT10*
11	INT11*
12	INT12*
13	INT13*
14	INT14*
15	INT15*
16	INT16*
17	INT17*
18	INT18*
19	INT19*
20	INT20*
21	INT21*
22	INT22*
23	INT23*
24	INT24*
25	INT25*
26	INT26*
27	INT27*
28	INT28*
29	INT29*
30	INT30*
31	INT31*
32	INT32*
33	INT33*
34	INT34*
35	INT35*
36	INT36*
37	INT37*
38	INT38*
39	INT39*
40	INT40*
41	INT41*
42	INT42*
43	INT43*
44	INT44*
45	INT45*
46	INT46*
47	INT47*
48	INT48*
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51	INT51*
52	INT52*
53	INT53*
54	INT54*
55	INT55*
56	INT56*
57	INT57*
58	INT58*
59	INT59*
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67	INT67*
68	INT68*
69	INT69*
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71	INT71*
72	INT72*
73	INT73*
74	INT74*
75	INT75*
76	INT76*
77	INT77*
78	INT78*
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80	INT80*
81	INT81*
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85	INT85*
86	INT86*
87	INT87*
88	INT88*
89	INT89*
90	INT90*
91	INT91*
92	INT92*
93	INT93*
94	INT94*
95	INT95*
96	INT96*
97	INT97*
98	INT98*
99	INT99*
100	INT100*

ABC1600
CIRCUIT DIAGRAM

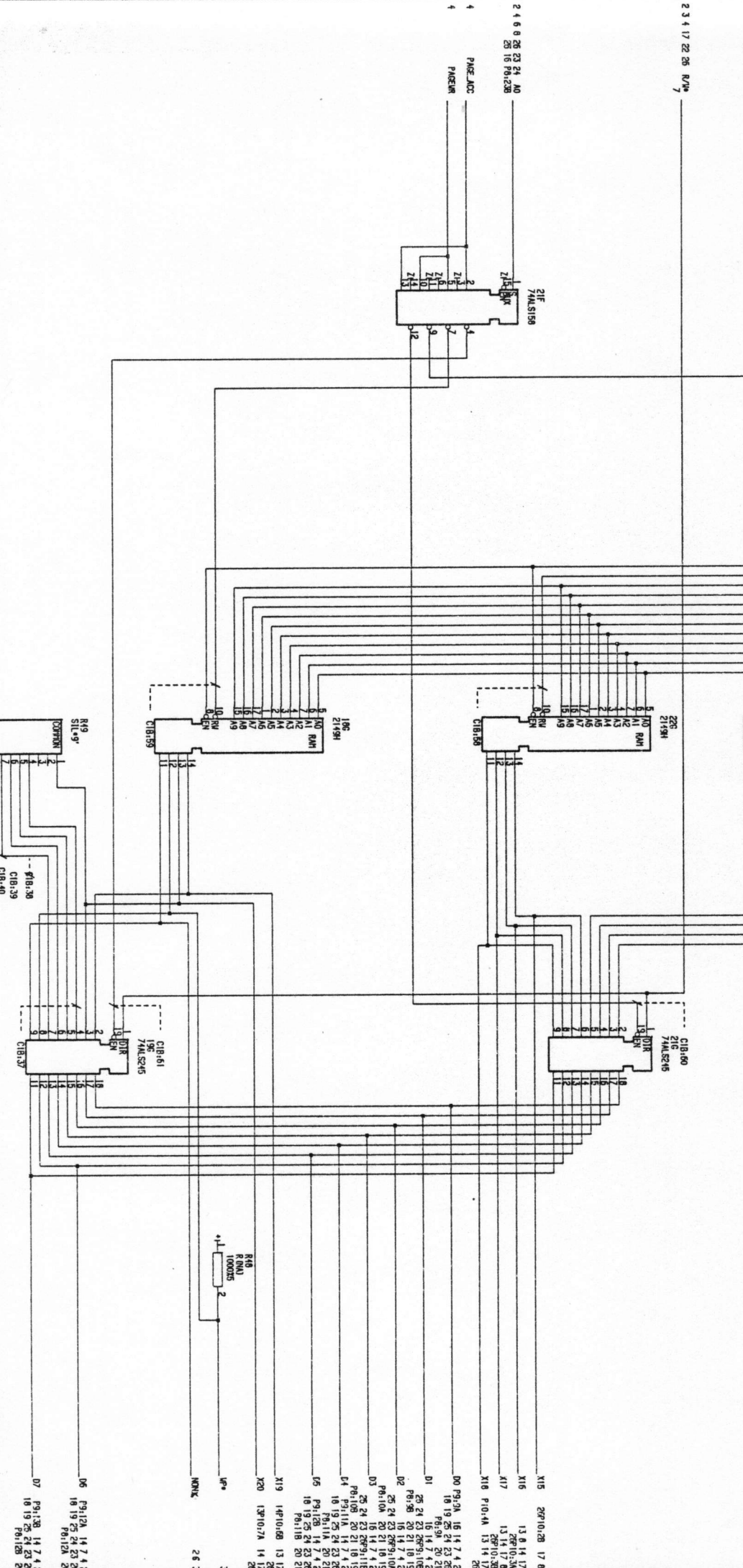


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DRA 1965-12-20
 MAC
 ABC1600
 CIRCUIT DIAGRAM
 GRANORI

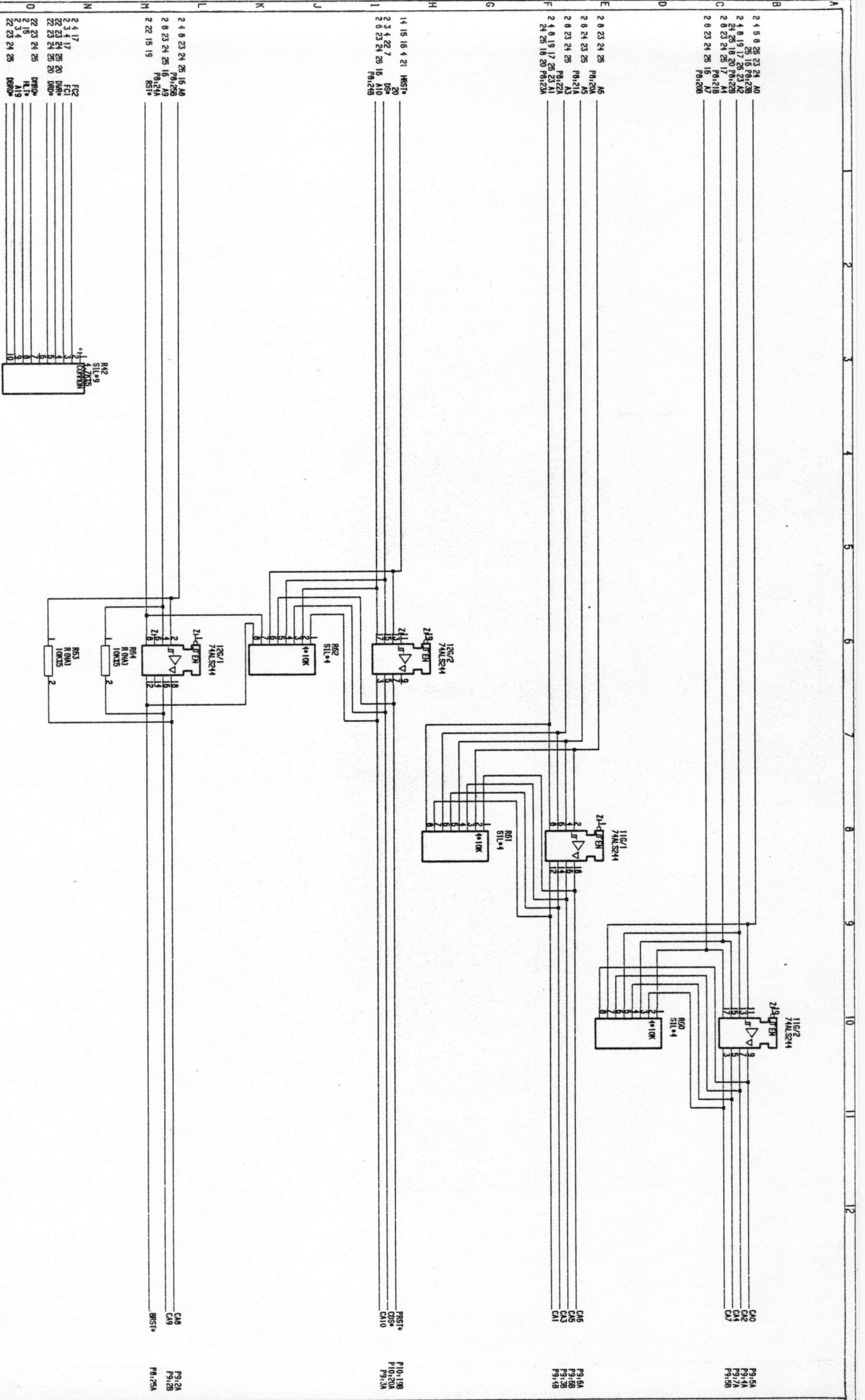


X11	25	16P10:5A	8
X12	16P1:3A	17	8
X13	26P10:5A	17	8
X14	26P10:4B	17	8
X15	26P10:2B	17	8
X16	13	8	14
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X94	13	8	14
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X97	13	8	14
X98	13	8	14
X99	13	8	14
X100	13	8	14

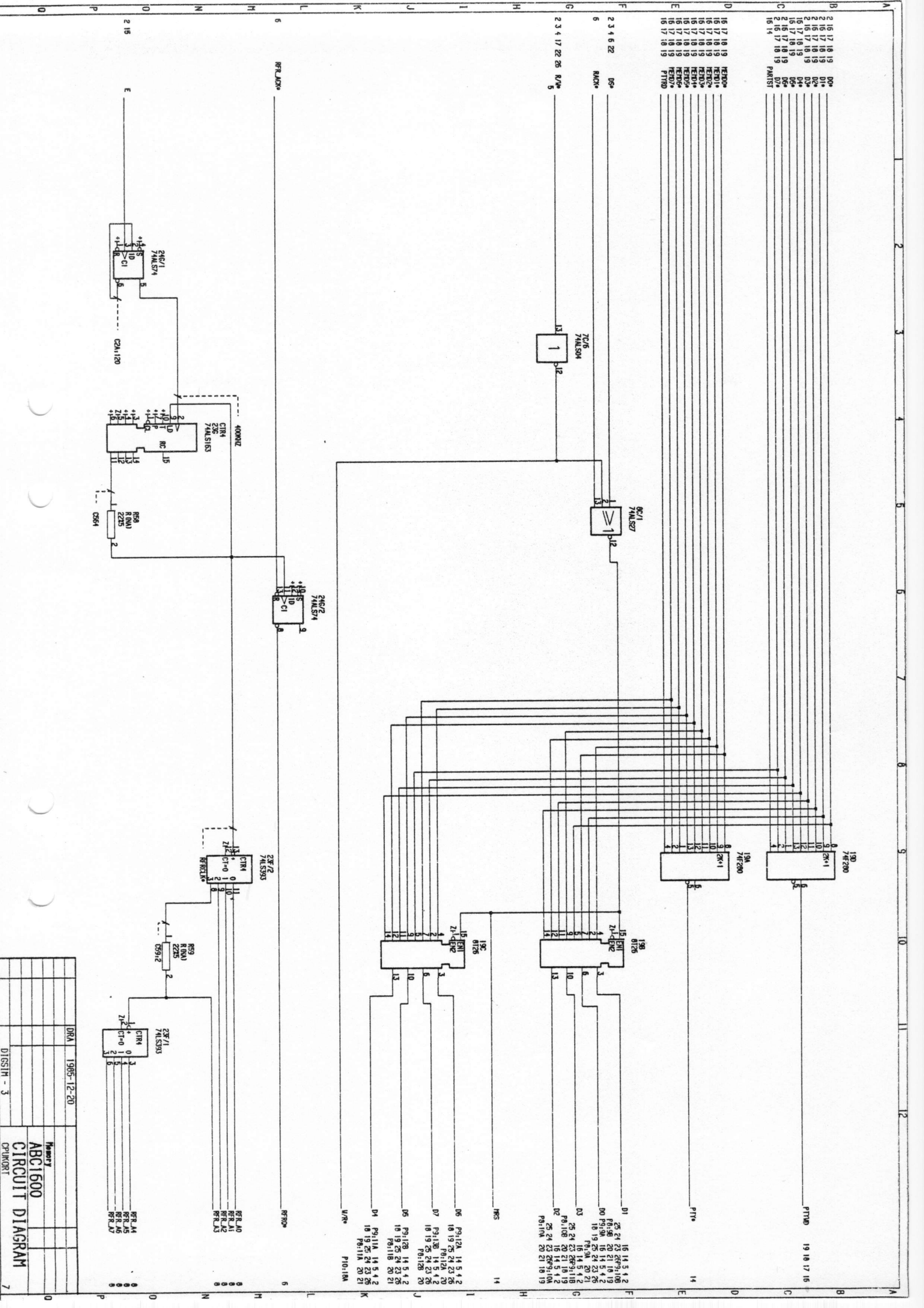


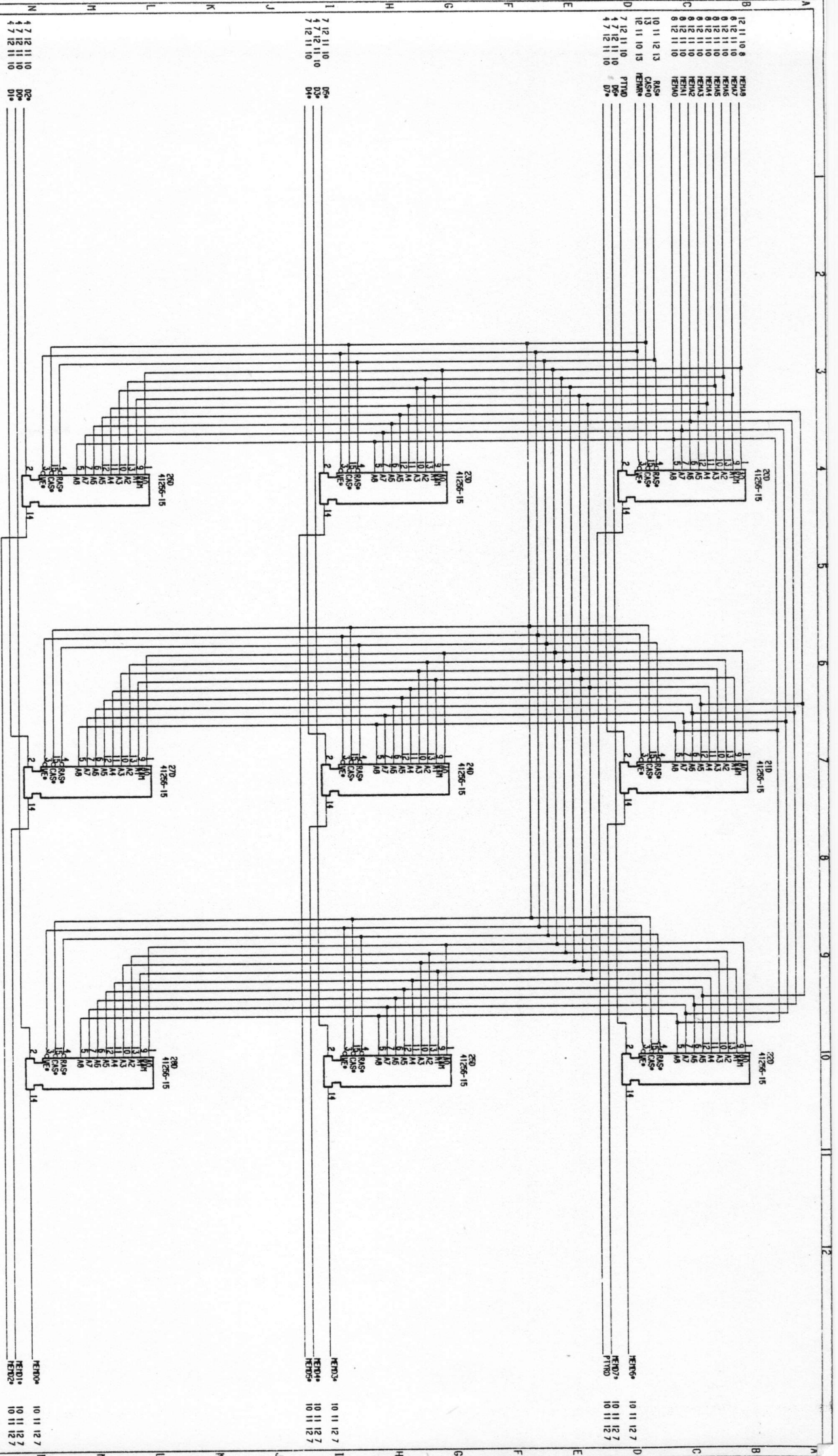
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03	P9:12B	14	7	4	2		
02	16	19	25	24	23	25	26
01	P6:12A	20					
00	P9:12B	14	7	4	2		
00	P9:12A	14	7	4	2		
00	P6:39	20	21				
00	P6:38	20	21				
00	P6:37	20	21				
00	P6:36	20	21				
00	P6:35	20	21				
00	P6:34	20	21				
00	P6:33	20	21				
00	P6:32	20	21				
00	P6:31	20	21				
00	P6:30	20	21				
00	P6:29	20	21				
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00	P6:-97	20	21				
00	P6:-98	20	21				
00	P6:-99	20	21				
00	P6:-100	20	21				

DRA 1965-12-20
 MC
 ABC1600
 CIRCUIT
 DIAGRAM



DATE	1986-02-21
REV.	1.0
DESIGNED BY	
CHECKED BY	
ABC1600 CIRCUIT DIAGRAM	





MEM00
MEM01
MEM02
MEM03
MEM04
MEM05
MEM06
MEM07
PTM0
PTM1
PTM2
D7

MEM00
MEM01
MEM02
MEM03
MEM04
MEM05
MEM06
MEM07
PTM0
PTM1
PTM2
D7

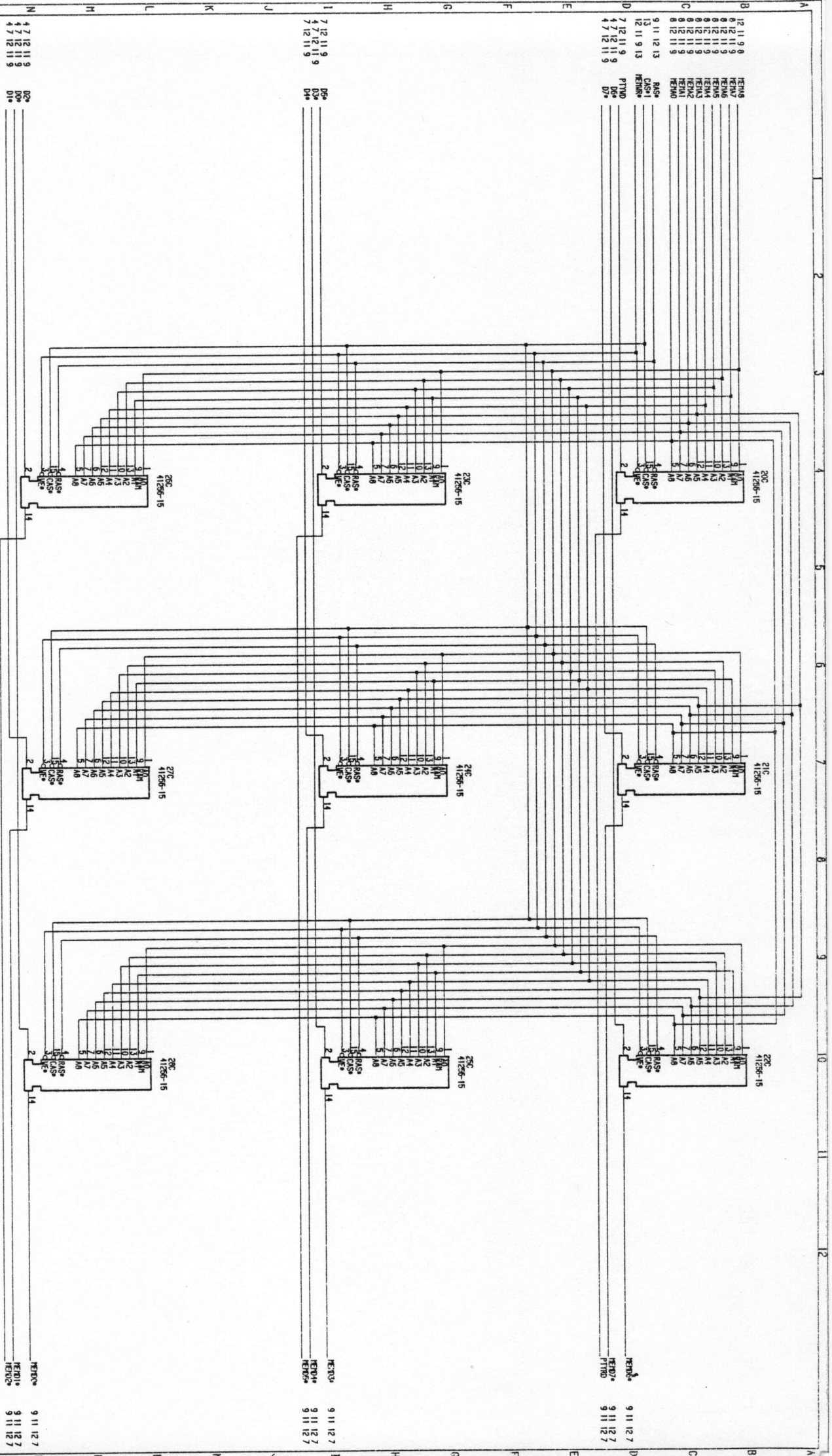
MEM00
MEM01
MEM02
MEM03
MEM04
MEM05
MEM06
MEM07
PTM0
PTM1
PTM2
D7

MEM00
MEM01
MEM02
MEM03
MEM04
MEM05
MEM06
MEM07
PTM0
PTM1
PTM2
D7

MEM00
MEM01
MEM02
MEM03
MEM04
MEM05
MEM06
MEM07
PTM0
PTM1
PTM2
D7

MEM00
MEM01
MEM02
MEM03
MEM04
MEM05
MEM06
MEM07
PTM0
PTM1
PTM2
D7

ORA	1985-12-20
Memory Bank 0	
ABC1600	
CIRCUIT DIAGRAM	



12 11 9 6 MEMA5
 6 12 11 9 MEMA7
 6 12 11 9 MEMA8
 6 12 11 9 MEMA9
 6 12 11 9 MEMA3
 6 12 11 9 MEMA2
 6 12 11 9 MEMA1
 6 12 11 9 MEMA0
 9 11 12 13 CAS=1
 12 11 9 13 CAS=0
 9 11 12 13 WE=0
 12 11 9 13 WE=1
 7 12 11 9 PTT00
 4 7 12 11 9 D7*

7 12 11 9 D5*
 4 7 12 11 9 D3*
 7 12 11 9 D4*

4 7 12 11 9 D2*
 4 7 12 11 9 D0*
 4 7 12 11 9 D1*

20C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

20C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

20C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

21C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

21C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

21C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

22C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

22C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

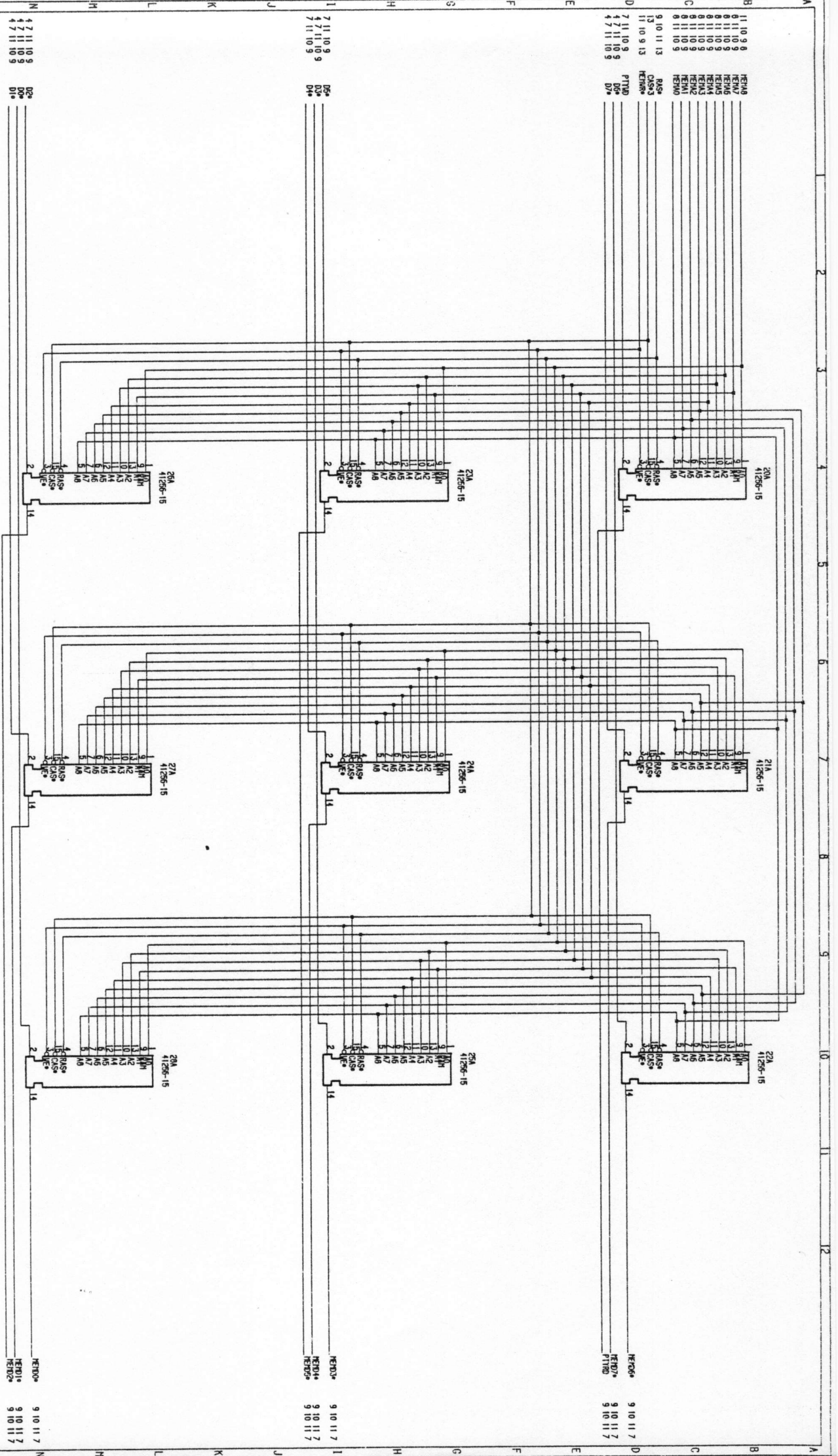
22C
 41256-15
 1 9 10 11 12 13 14
 1 2 3 4 5 6 7 8
 1 2 3 4 5 6 7 8 9 10 11 12 13 14

MEMA0 9 11 12 7
MEMA1 9 11 12 7
MEMA2 9 11 12 7
MEMA3 9 11 12 7
MEMA4 9 11 12 7
MEMA5 9 11 12 7
MEMA6 9 11 12 7
MEMA7 9 11 12 7
MEMA8 9 11 12 7
MEMA9 9 11 12 7
CAS=0 9 11 12 7
CAS=1 9 11 12 7
WE=0 9 11 12 7
WE=1 9 11 12 7
PTT00 9 11 12 7
D7* 9 11 12 7

MEMA0 9 11 12 7
MEMA1 9 11 12 7
MEMA2 9 11 12 7
MEMA3 9 11 12 7
MEMA4 9 11 12 7
MEMA5 9 11 12 7
MEMA6 9 11 12 7
MEMA7 9 11 12 7
MEMA8 9 11 12 7
MEMA9 9 11 12 7
CAS=0 9 11 12 7
CAS=1 9 11 12 7
WE=0 9 11 12 7
WE=1 9 11 12 7
PTT00 9 11 12 7
D7* 9 11 12 7

MEMA0 9 11 12 7
MEMA1 9 11 12 7
MEMA2 9 11 12 7
MEMA3 9 11 12 7
MEMA4 9 11 12 7
MEMA5 9 11 12 7
MEMA6 9 11 12 7
MEMA7 9 11 12 7
MEMA8 9 11 12 7
MEMA9 9 11 12 7
CAS=0 9 11 12 7
CAS=1 9 11 12 7
WE=0 9 11 12 7
WE=1 9 11 12 7
PTT00 9 11 12 7
D7* 9 11 12 7

DRA	1985-12-20
Heavy Bank I ABC1600 CIRCUIT DIAGRAM	



11 10 9 8
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

9 10 11 13
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

7 11 10 9
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

4 7 11 10 9
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

7 11 10 9
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

7 11 10 9
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

7 11 10 9
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

7 11 10 9
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

4 7 11 10 9
MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
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MEM1
MEM0
RAS
CAS
WE
OE

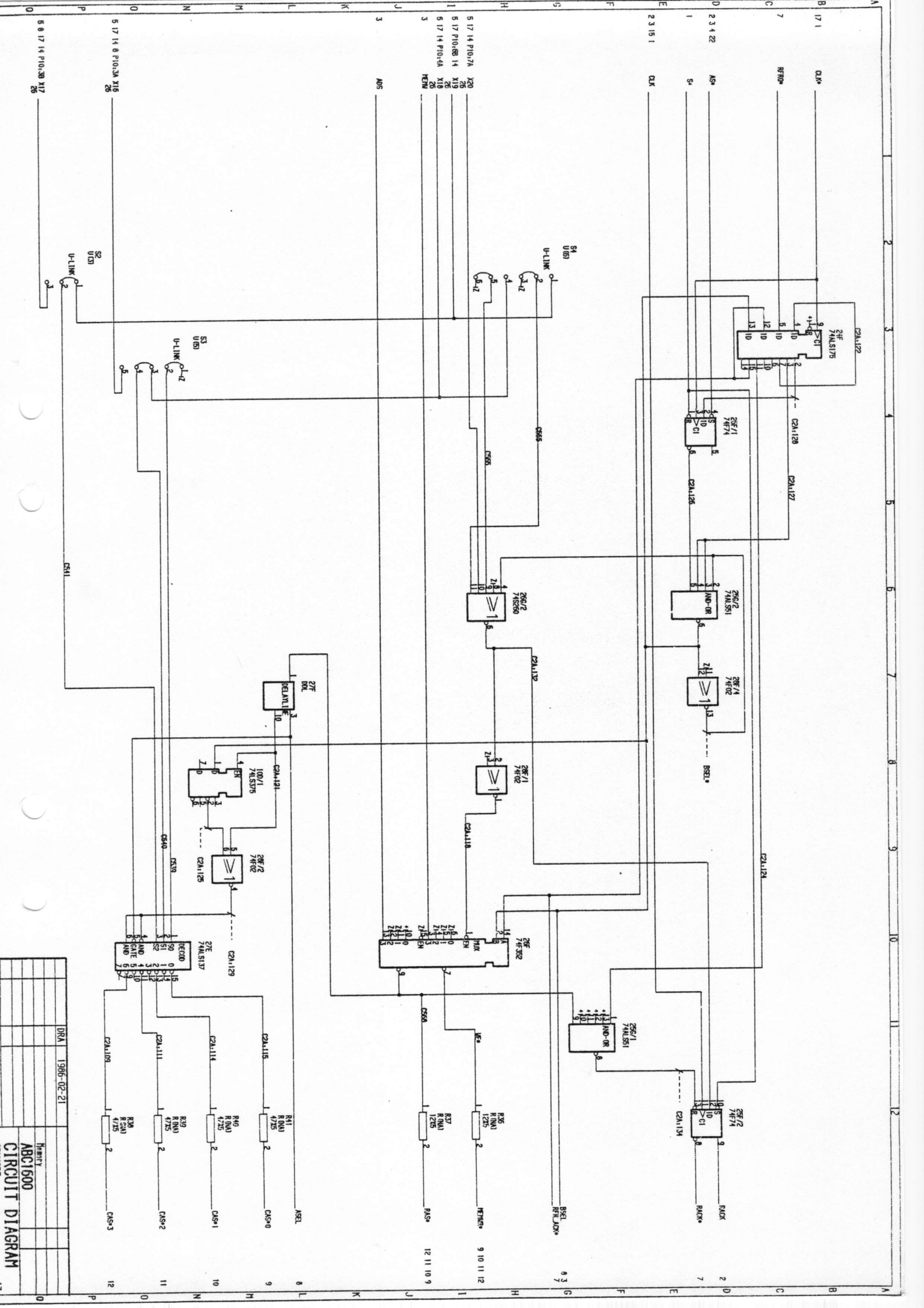
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MEM5
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MEM1
MEM0
RAS
CAS
WE
OE

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MEM8
MEM7
MEM6
MEM5
MEM4
MEM3
MEM2
MEM1
MEM0
RAS
CAS
WE
OE

4 7 11 10 9
MEM8
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MEM6
MEM5
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MEM3
MEM2
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MEM0
RAS
CAS
WE
OE

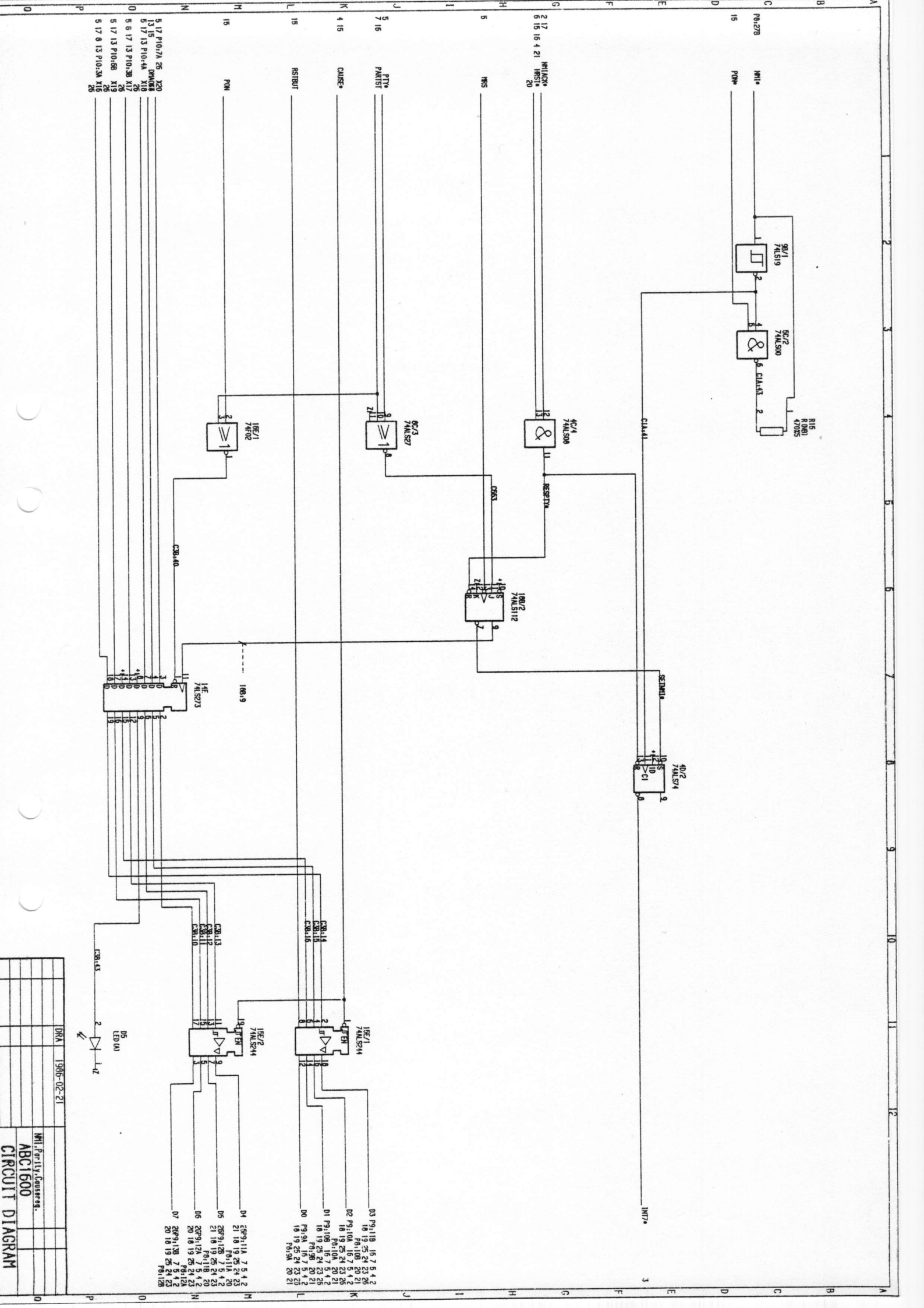
DRA 1985-12-20

Memory Bank 3
ABC1500
CIRCUIT DIAGRAM



DATE	1986-02-21
DRAWN	ABC1500
CHECKED	
APPROVED	
REVISION	
NO.	
DESCRIPTION	
BY	
DATE	

CIRCUIT DIAGRAM



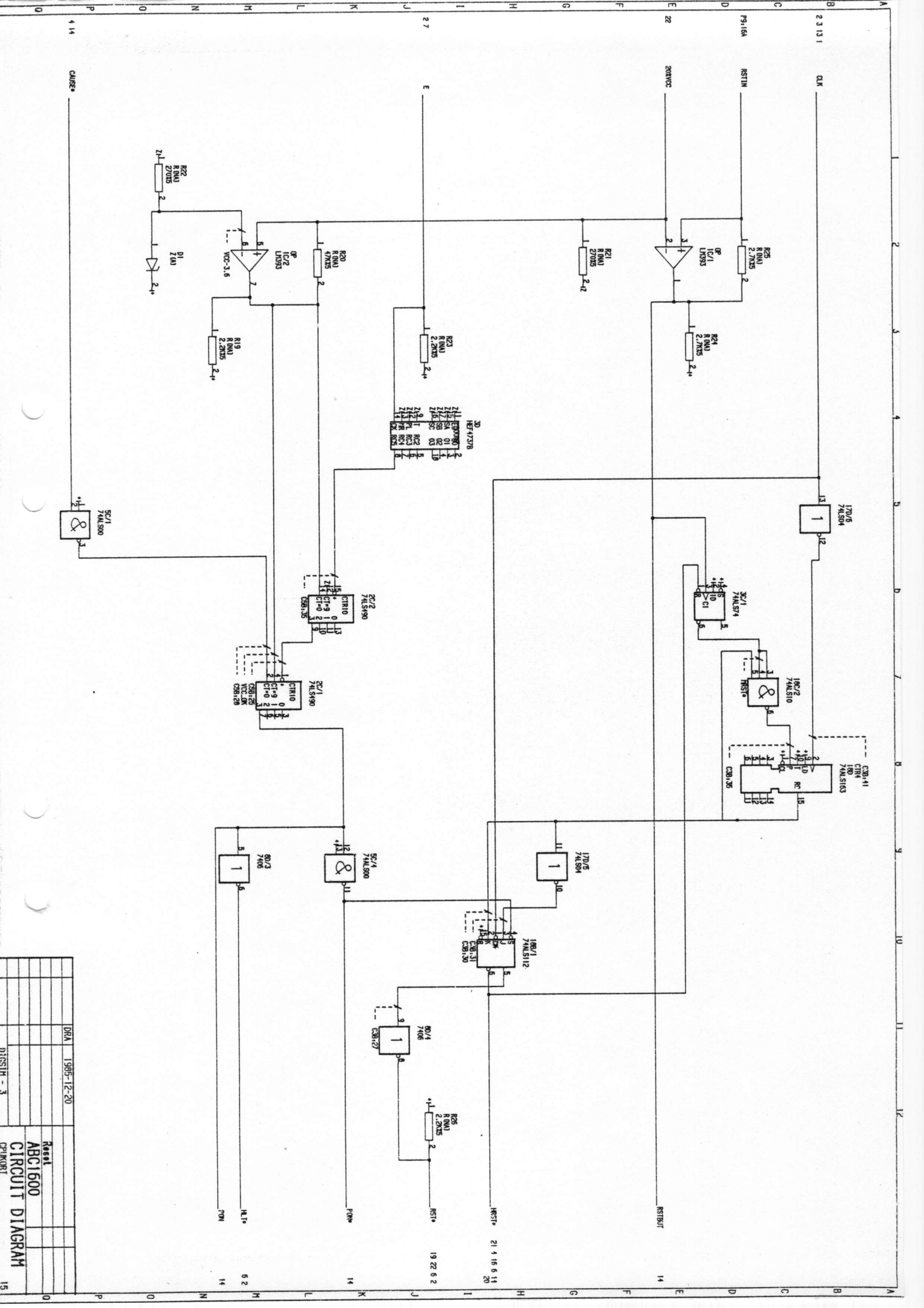
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 5 17 13 P10.6/B X19
 5 17 8 13 P10.3/A X16

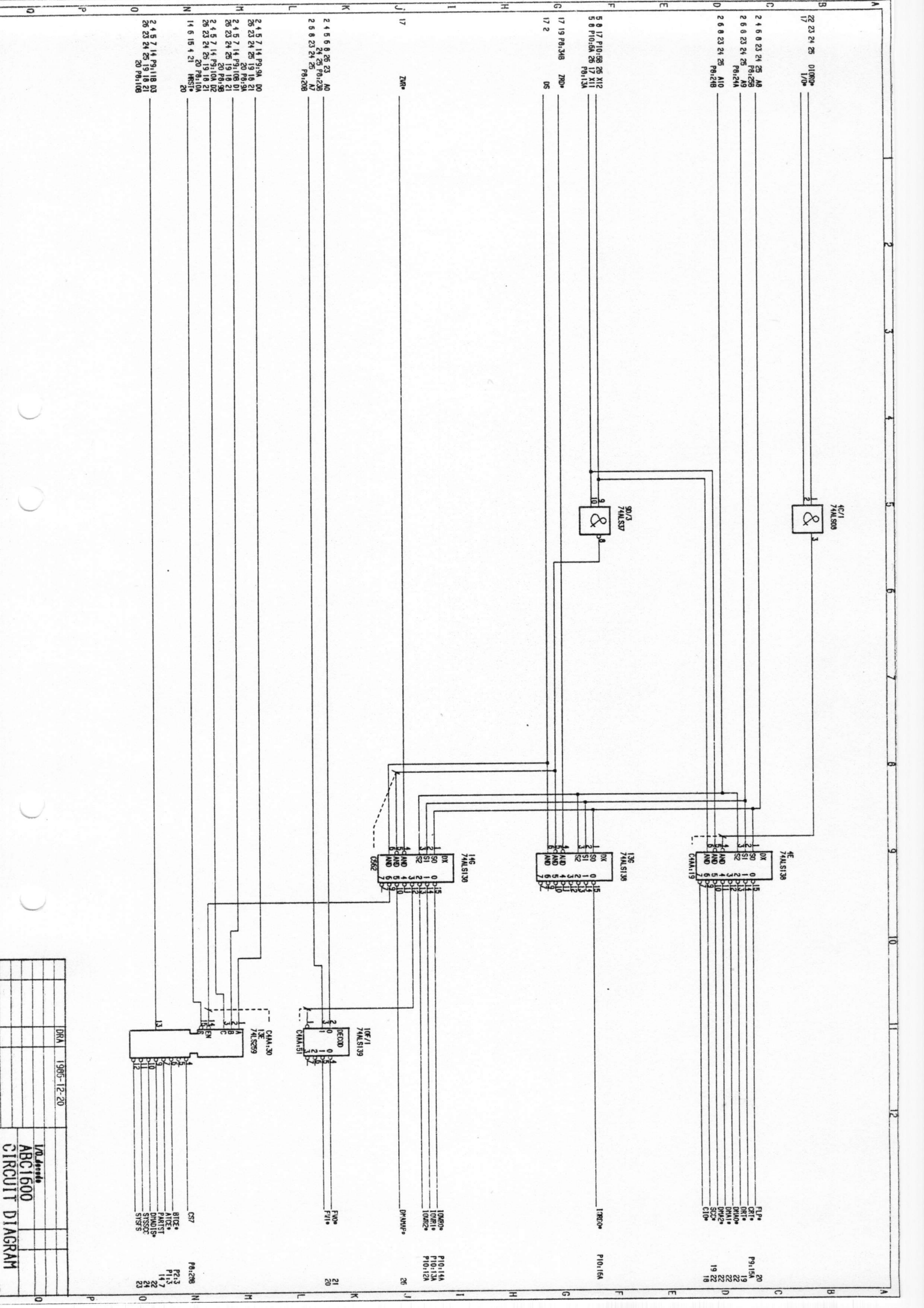
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NHF Family Decoder ABC1600 CIRCUIT DIAGRAM	

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 10 19 25 24 23 26
 02 P9.10/8 20 21
 18 P9.10/8 20 21
 10 19 25 24 23 26
 01 P9.10/8 16 7 5 4 2
 10 19 25 24 23 26
 09 P9.9/8 20 21
 10 19 25 24 23 26
 P9.9/8 20 21

04 5P9.11/1 7 5 4 2
 21 18 19 25 24 23
 05 2P9.12/3 26 24 25
 21 18 P9.11/8 20
 06 2P9.12/3 7 5 4 2
 20 18 19 25 24 23
 07 5P9.12/3 7 5 4 2
 20 18 19 25 24 23
 P9.12/3

05 100nF
 05 LED(A)





2 4 5 6 8 23 A0
24 25 P0:230
2 5 8 23 24 25 P0:208

2 4 5 7 14 P9:08 01
26 23 24 25 19 18 21
2 4 5 7 14 P9:10 03
26 23 24 25 19 18 21

14 6 15 4 21 P0:10A
20 P0:10A
20

2 4 5 7 14 P9:08 00
26 23 24 25 19 18 21
2 4 5 7 14 P9:10 01
26 23 24 25 19 18 21
2 4 5 7 14 P9:10 02
26 23 24 25 19 18 21

2 4 5 7 14 P9:11 03
26 23 24 25 19 18 21
20 P0:100

2 4 5 7 14 P9:11 03
26 23 24 25 19 18 21
20 P0:100

2 4 5 7 14 P9:11 03
26 23 24 25 19 18 21
20 P0:100

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26 23 24 25 19 18 21
20 P0:100

2 4 5 7 14 P9:11 03
26 23 24 25 19 18 21
20 P0:100

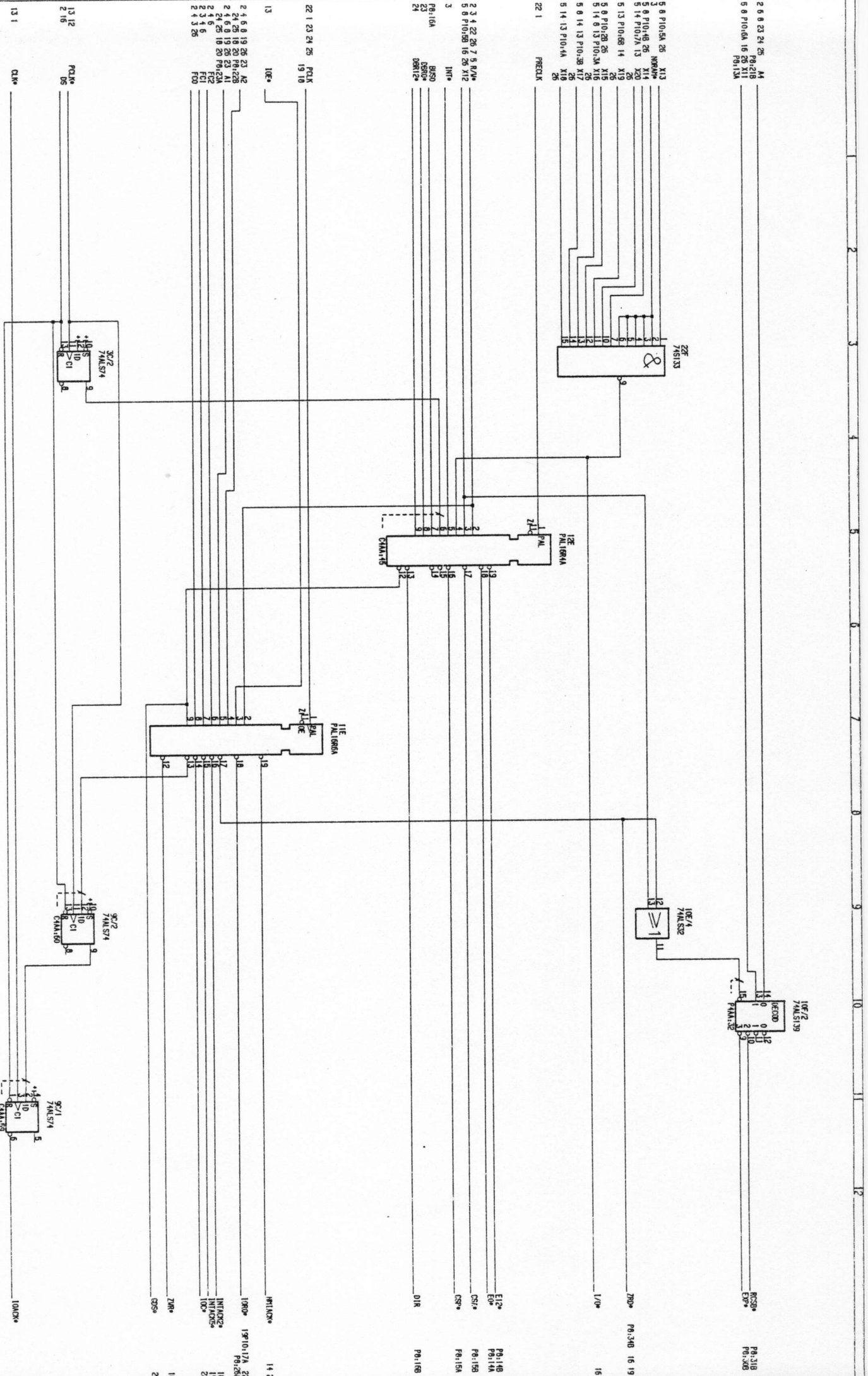
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26 23 24 25 19 18 21
20 P0:100

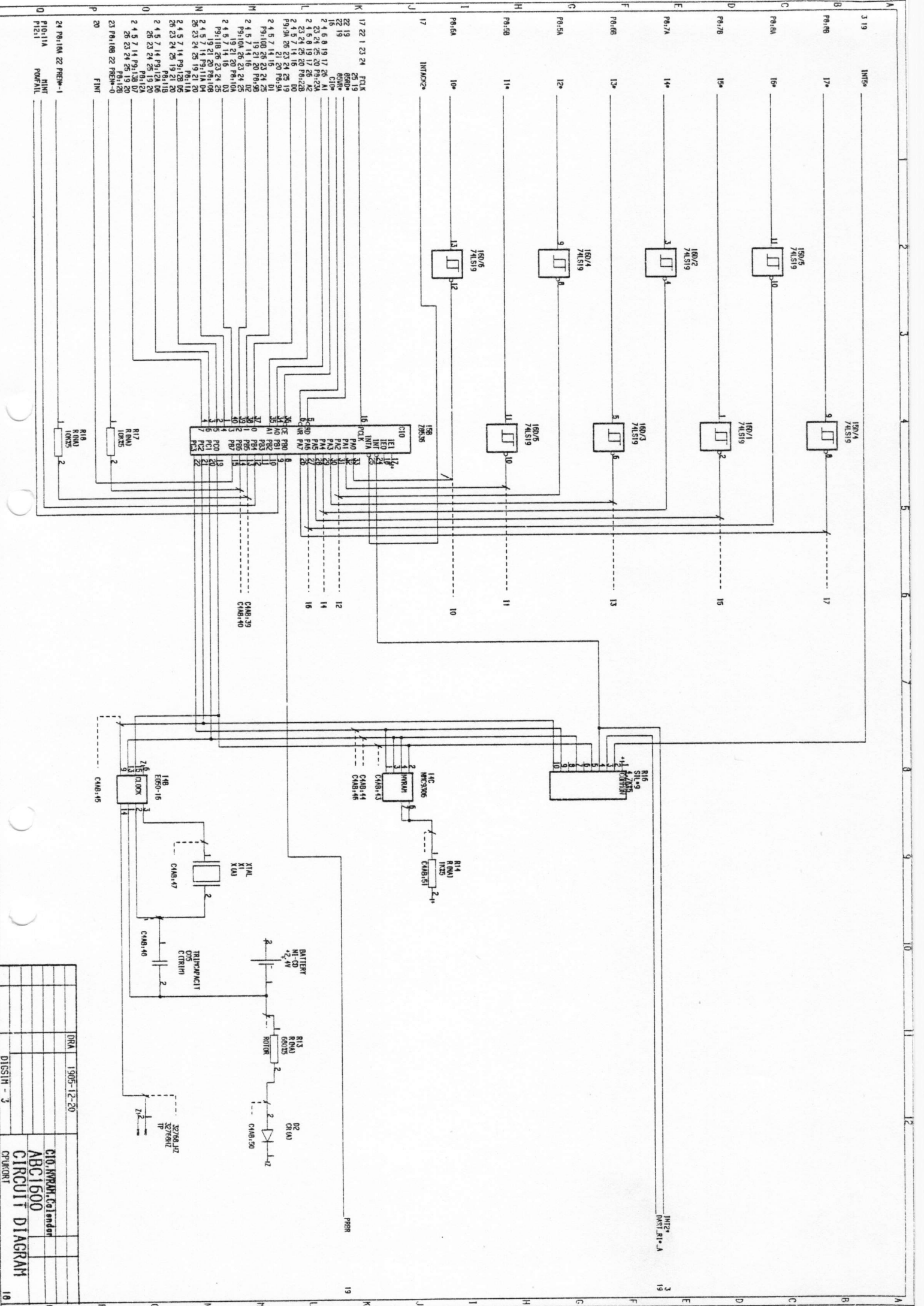
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26 23 24 25 19 18 21
20 P0:100

2 4 5 7 14 P9:11 03
26 23 24 25 19 18 21
20 P0:100

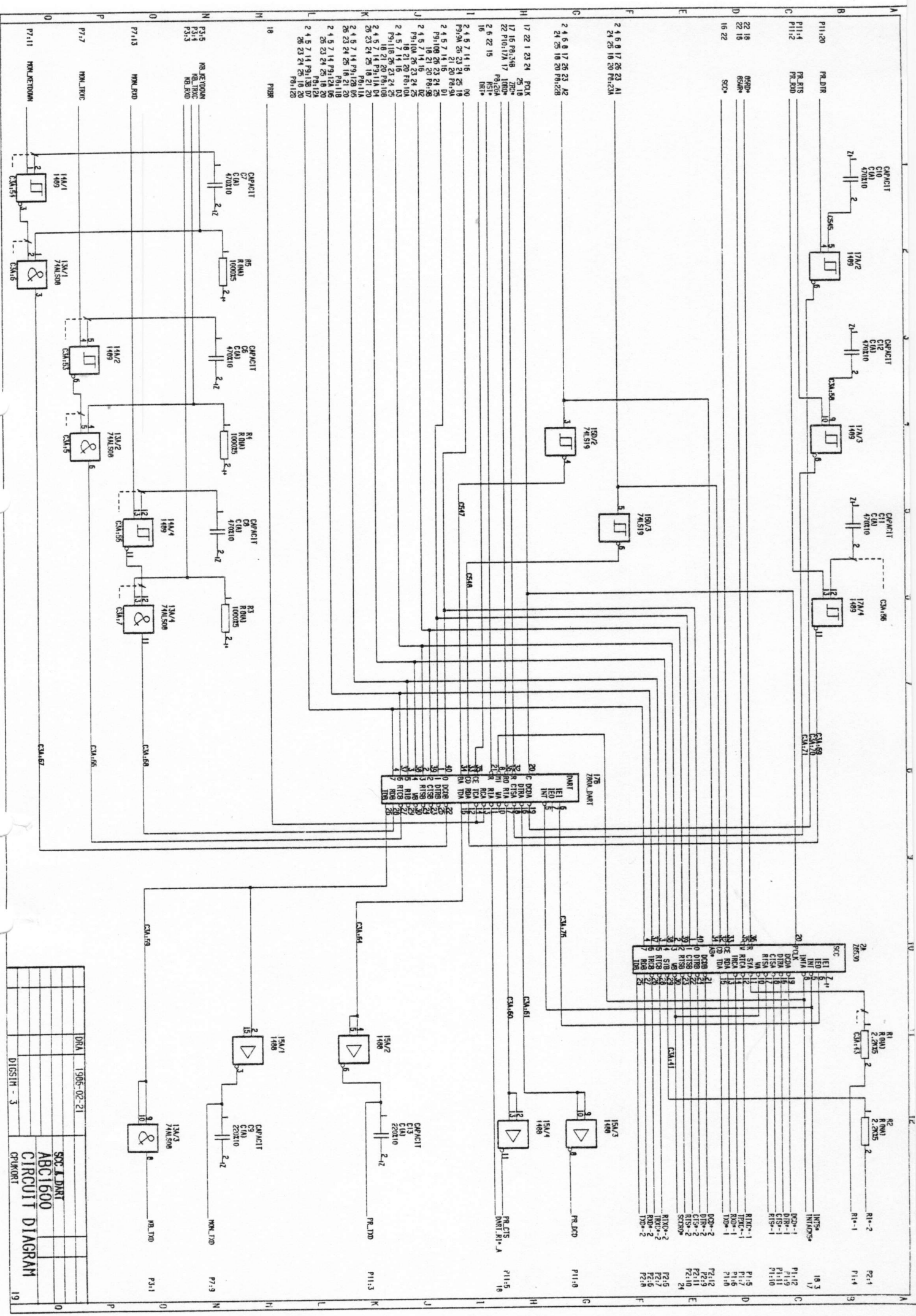
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26 23 24 25 19 18 21
20 P0:100

DRA	1985-12-20
I/O device	ABC1600
CIRCUIT DIAGRAM	





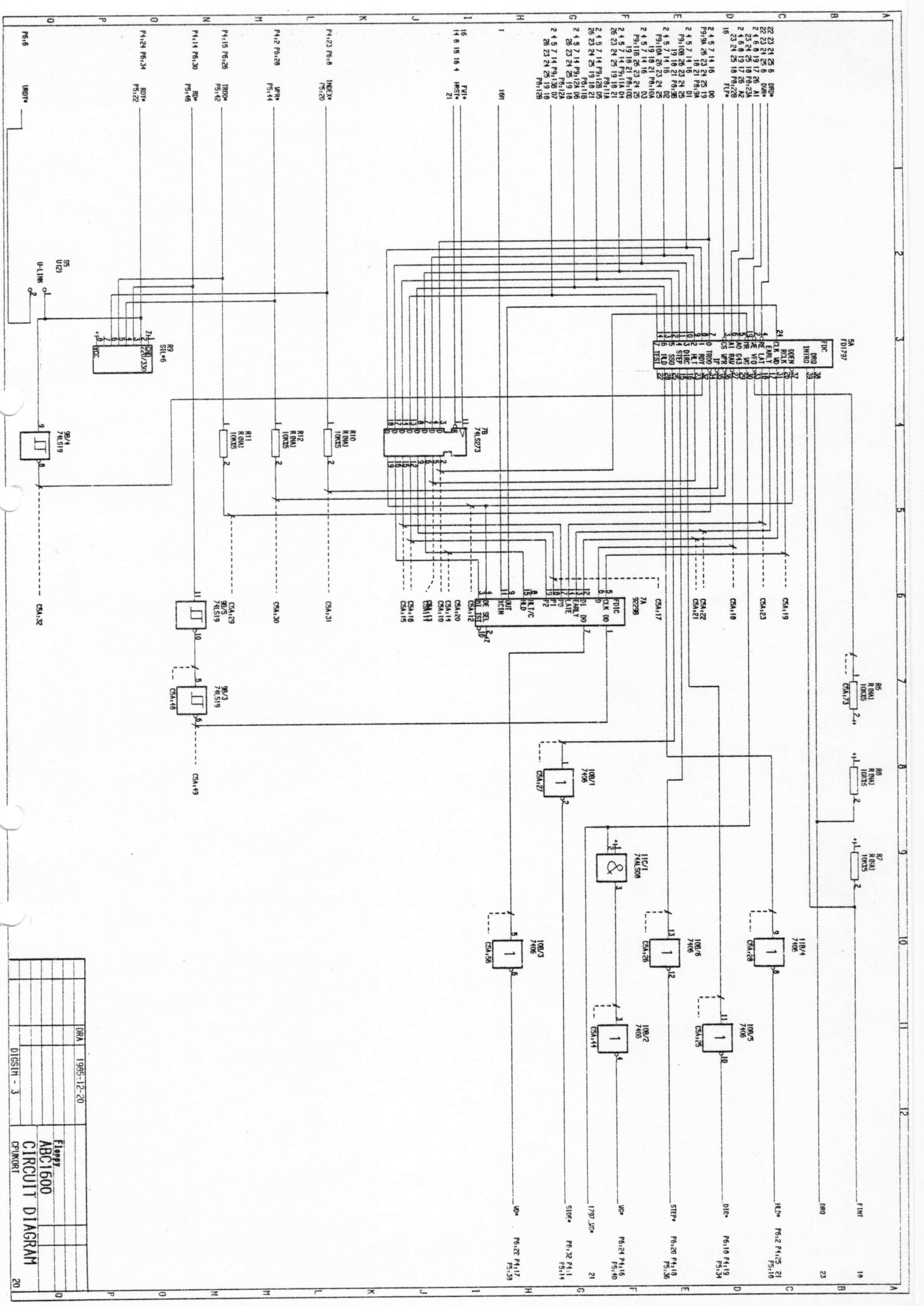
ORA	1905-12-20
C10: ANRRA: Colandor	
ABC1500	
CIRCUIT DIAGRAM	
CPURONT	



Z800-DART

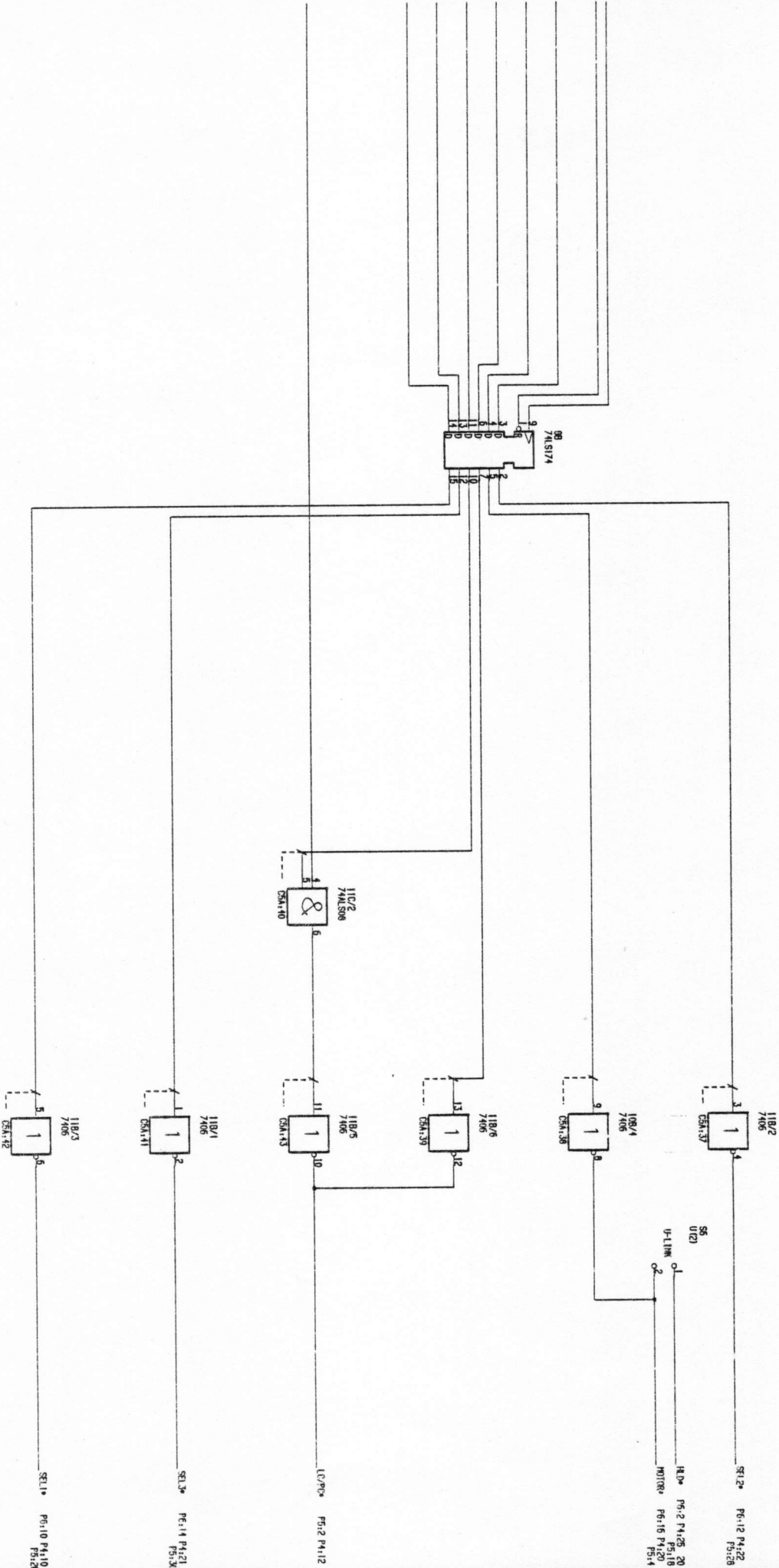
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95	INT
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97	INT
98	INT
99	INT
100	INT

DRN	1906-02-21
SCS	ABC1600
CIRCUIT	DIAGRAM
DISINH	- 3



DRN	1995-12-20
FLORRY ABC1600 CIRCUIT DIAGRAM	
DESIGN - 3	

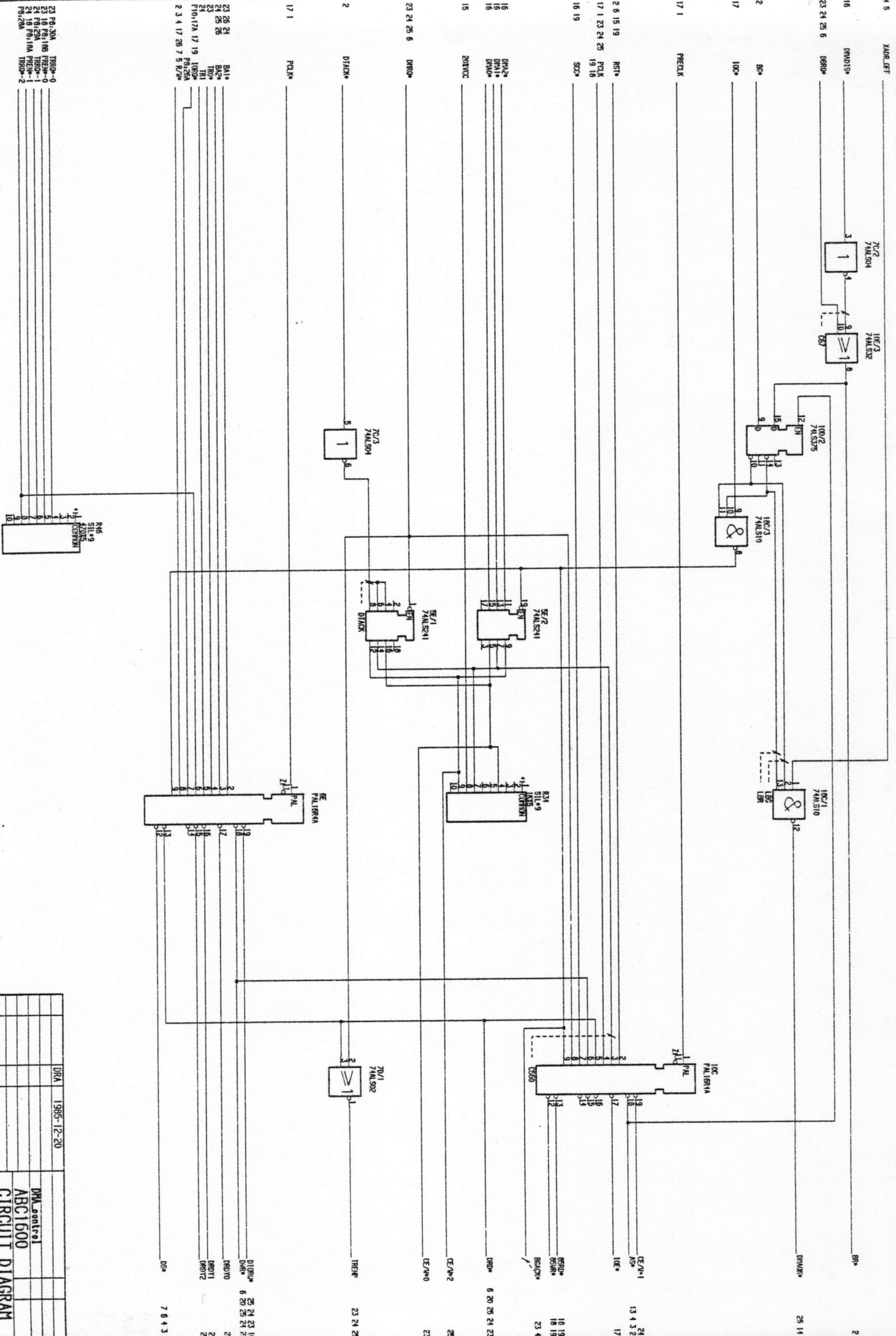
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 19 10 20 P9:98
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 P9:118 26 23 24 25
 19 10 20 P9:108
 2 4 5 7 14 15 D5
 P9:118 26 23 24 25
 19 10 20 P9:111A
 2 4 5 7 14 15 P9:128 D5
 26 23 24 25 19 10 20
 2 4 5 7 14 15 P9:1 D5
 P9:104 26 23 24 25
 19 10 20 P9:104
 2 4 5 7 14 15 D0
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 10 20 P9:9A



1797 JPC*

DRA 1985-12-20

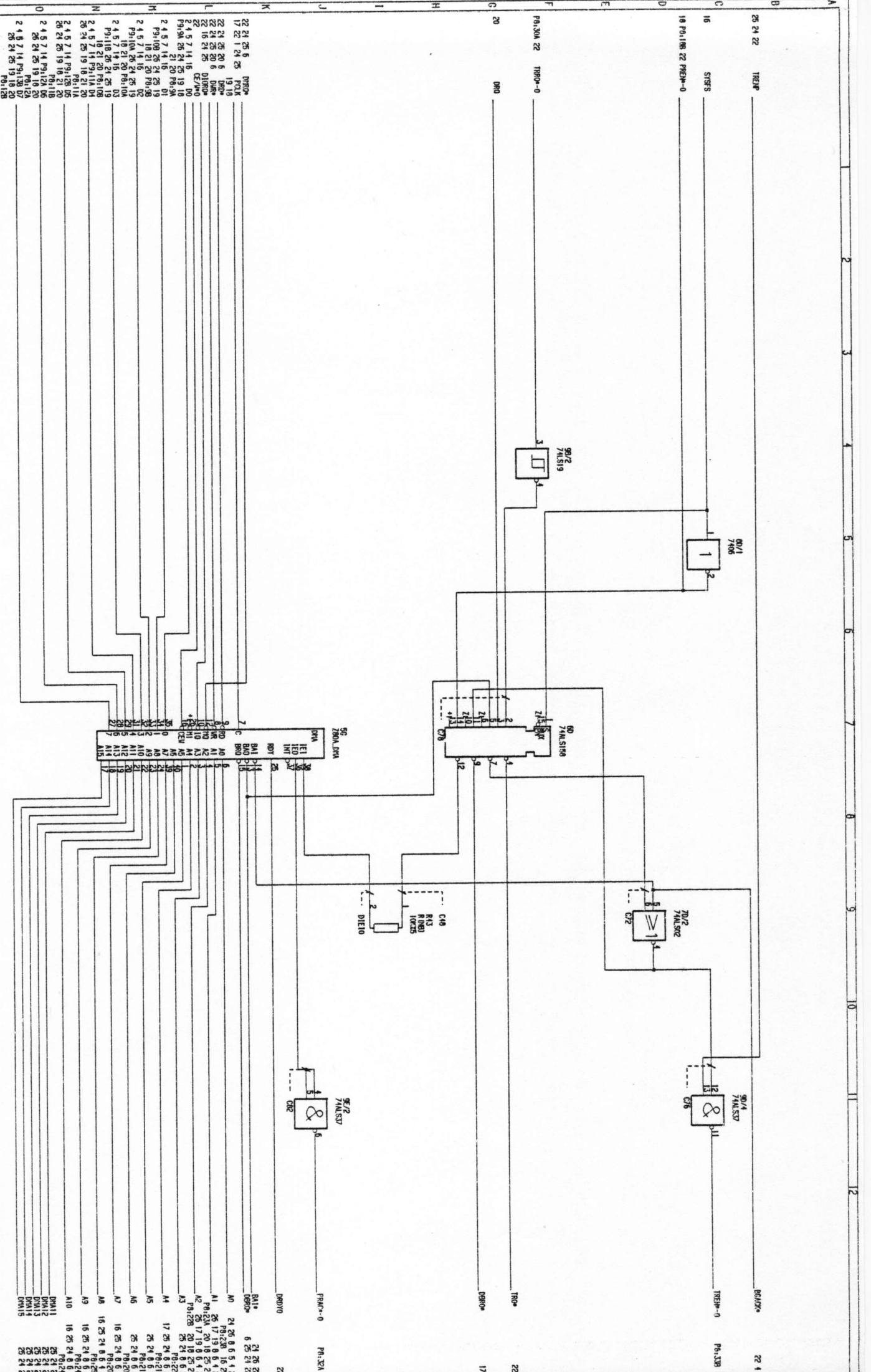
F1000
 ABC1600
 CIRCUIT DIAGRAM



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 2 B0
 100
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 17 1 PRECLX
 2 6 15 19 RST1
 17 1 23 24 25 POLX
 19 18
 16 19 SCC
 23 24 25 6 DR00
 15 20VCC
 16 DR12
 16 DR13
 16 DR14
 16 DR15
 23 24 25 6 DR00
 17 1
 17 1 POLX
 23 26 24 BA1
 24 25 26 BA2
 23 TR1
 24 TR2
 23 24 25 6 TR1
 23 24 25 6 TR2
 23 24 25 6 TR3
 23 24 25 6 TR4
 23 24 25 6 TR5
 23 24 25 6 TR6
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ORA	1985-12-20
DISINH - 3	

DM Control
 ABC1600
 CIRCUIT DIAGRAM
 22

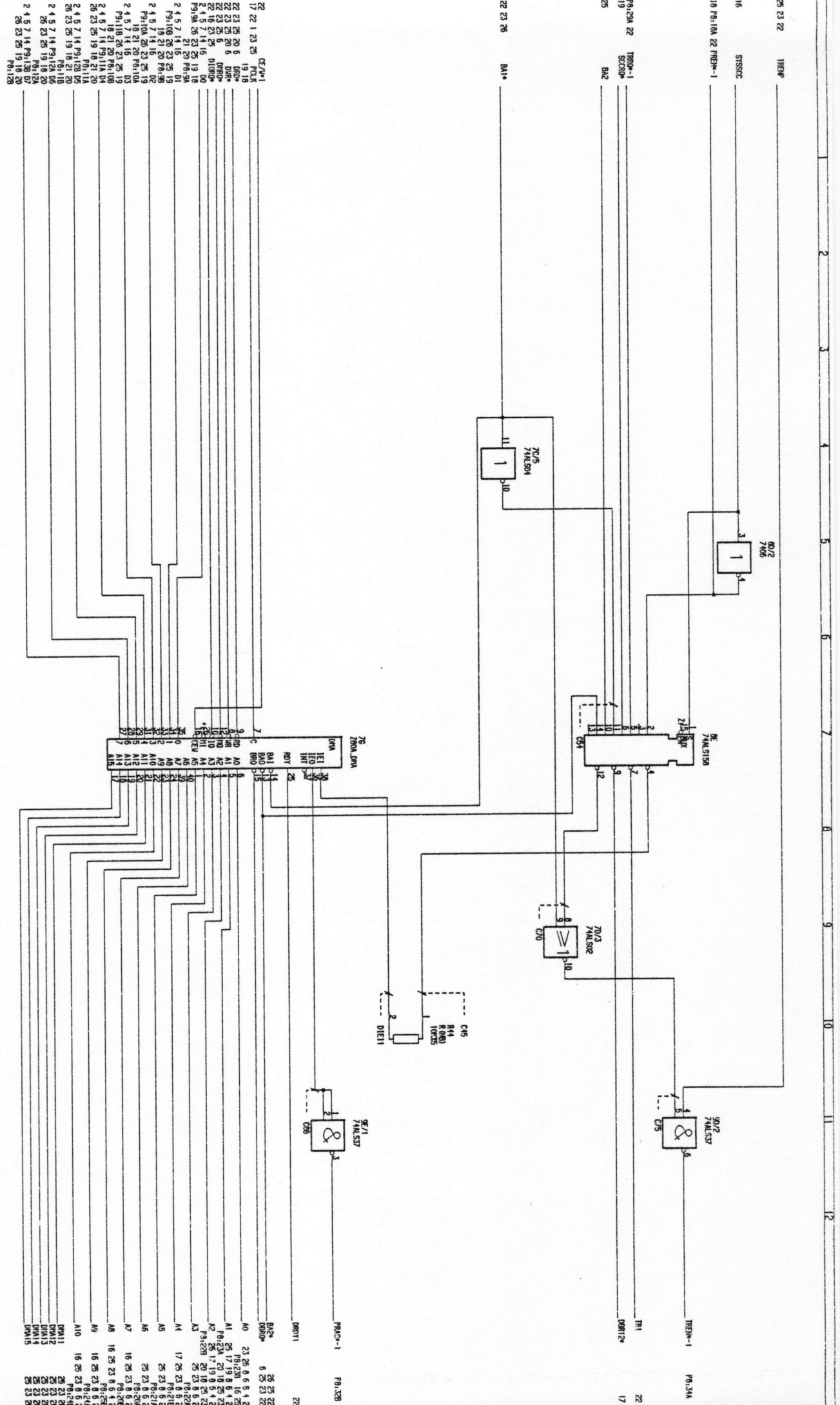


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DMN0
ABC1600
CIRCUIT DIAGRAM

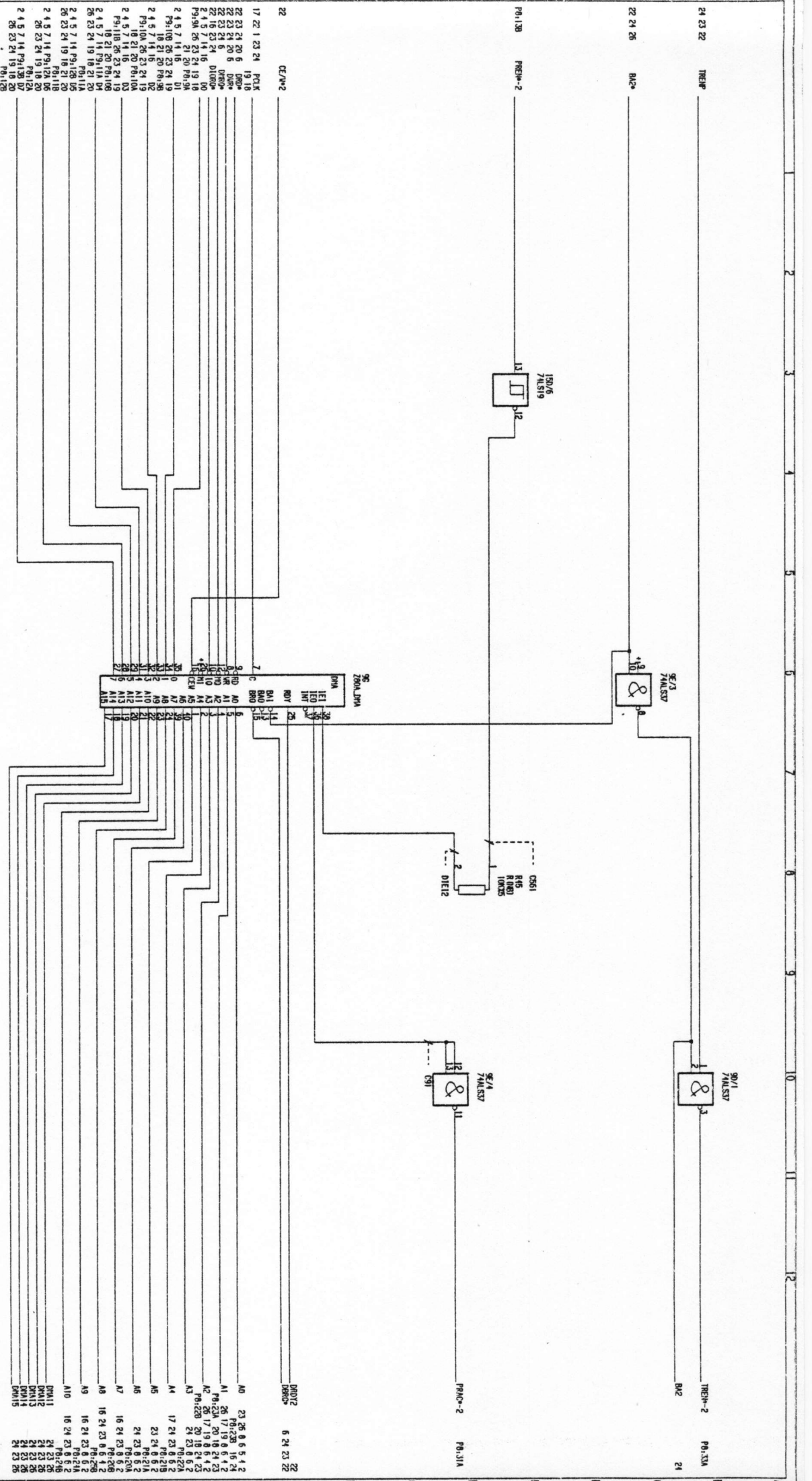
DRA	1985-12-20
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 P91,23 P91,24 P91,25
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 DNR 6 25 23 22
 A0 21 26 8 6 5 4 2
 A1 25 17 19 8 6 4 2
 A2 P91,23A 23 18 25 23
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 A7 17 25 23 0 6 5 2
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 A9 25 23 0 6 5 2
 A10 25 23 0 6 5 2
 A11 P91,24A 16 25 23 0 6 5 2
 A12 P91,24B 16 25 23 0 6 5 2
 A13 P91,24C 16 25 23 0 6 5 2
 A14 P91,24D 16 25 23 0 6 5 2
 A15 P91,24E 16 25 23 0 6 5 2
 B0 P91,24F 16 25 23 0 6 5 2
 B1 P91,24G 16 25 23 0 6 5 2
 B2 P91,24H 16 25 23 0 6 5 2
 B3 P91,24I 16 25 23 0 6 5 2
 B4 P91,24J 16 25 23 0 6 5 2
 B5 P91,24K 16 25 23 0 6 5 2
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DWA	1905-12-20
ABC1600	
CIRCUIT DIAGRAM	

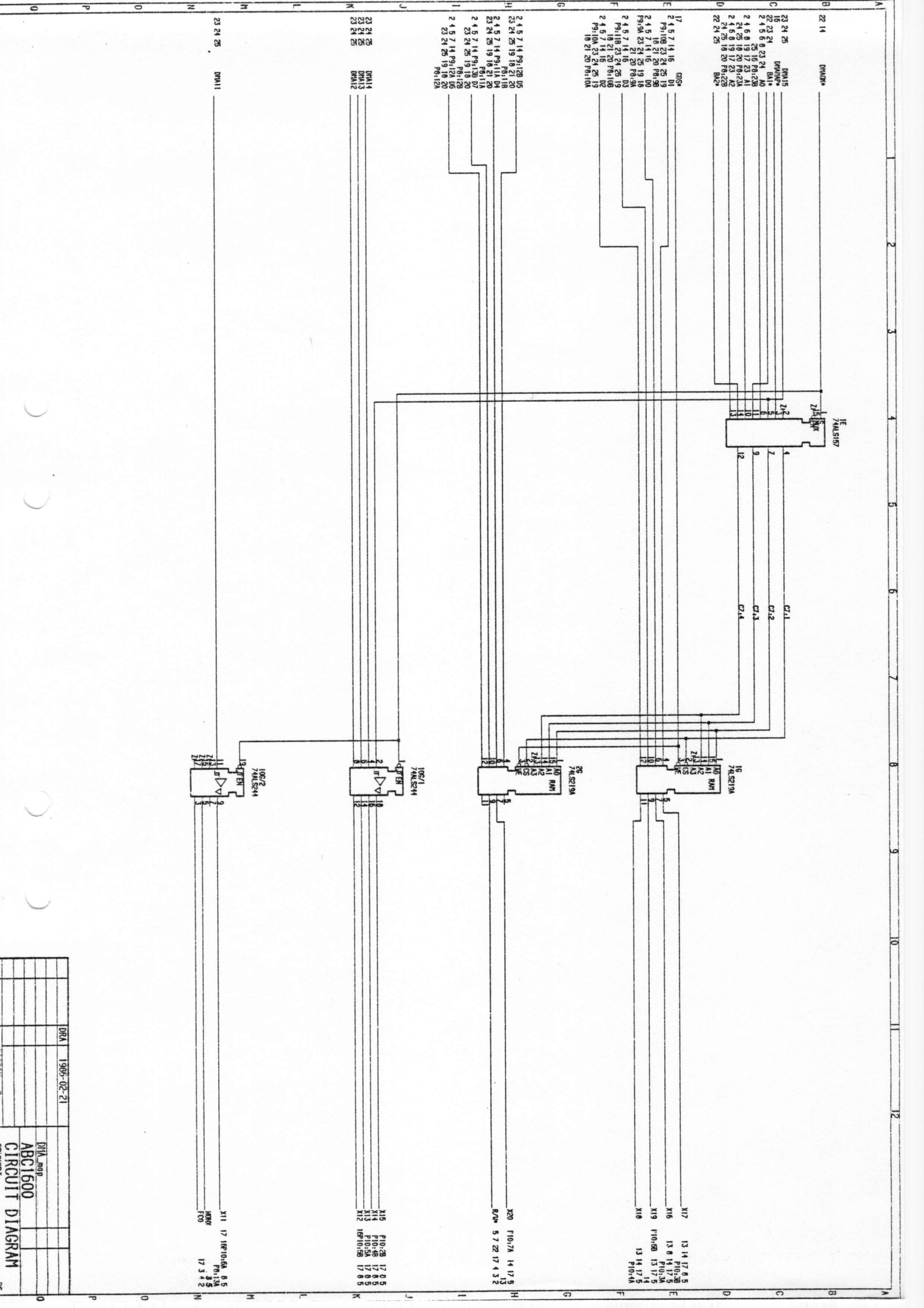


Pin	Label	Function
17	CE	Chip Enable
18	OE	Output Enable
19	WE	Write Enable
20	IO/M	IO/ Memory Strobe
21	INT	Interrupt
22	RES	Reset
23	PS	Program Status
24	CS	Chip Select
25	AS	Address Strobe
26	BS	Bus Strobe
27	CS	Chip Select
28	CS	Chip Select

Pin	Label	Function
0	A0	Address Bit 0
1	A1	Address Bit 1
2	A2	Address Bit 2
3	A3	Address Bit 3
4	A4	Address Bit 4
5	A5	Address Bit 5
6	A6	Address Bit 6
7	A7	Address Bit 7
8	B0	Bus Bit 0
9	B1	Bus Bit 1
10	B2	Bus Bit 2
11	B3	Bus Bit 3
12	B4	Bus Bit 4
13	B5	Bus Bit 5
14	B6	Bus Bit 6
15	B7	Bus Bit 7
16	C	Control Bit

DRM 2
ABC1500
CIRCUIT DIAGRAM

DRM 1985-12-20



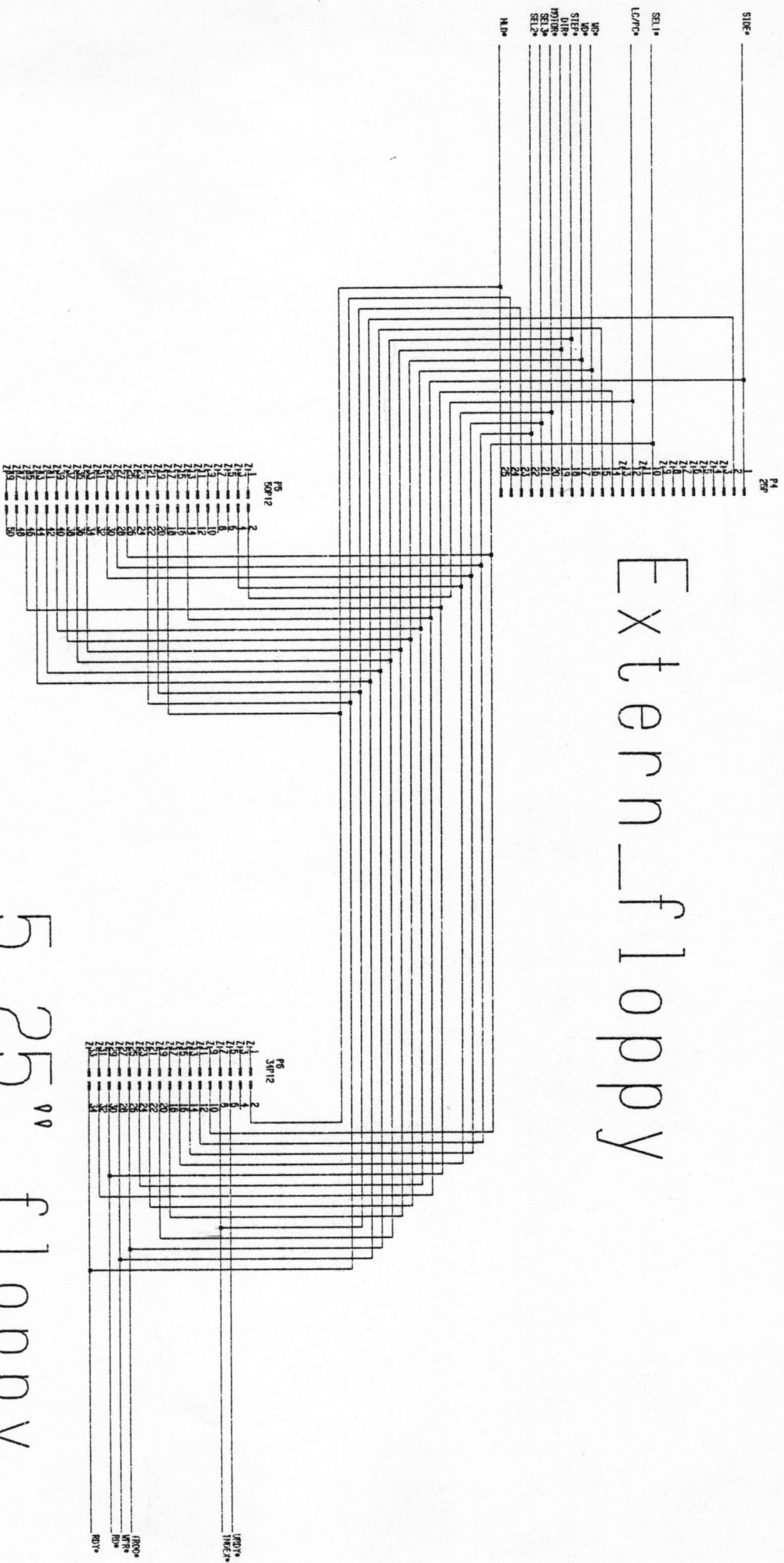
0	1	2	3	4	5	6	7	8	9	10	11	12
0	1	2	3	4	5	6	7	8	9	10	11	12
0	1	2	3	4	5	6	7	8	9	10	11	12

ABC1600
CIRCUIT DIAGRAM

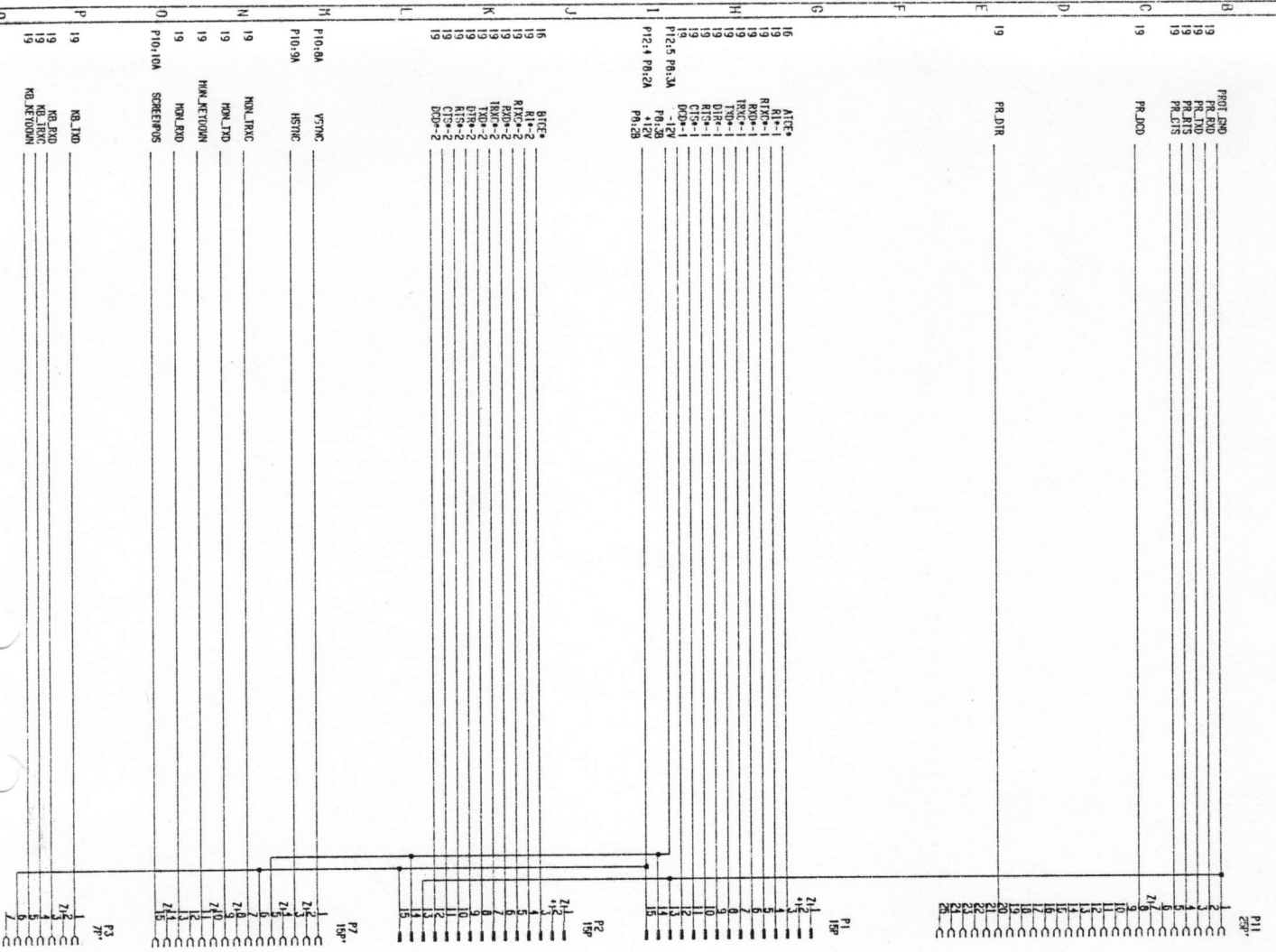
1965-02-21

8" floppy

5.25" floppy



DRG	1985-12-20	ABC1600
		CIRCUIT DIAGRAM



Printer_(Dsub)

ty02_V24-kort

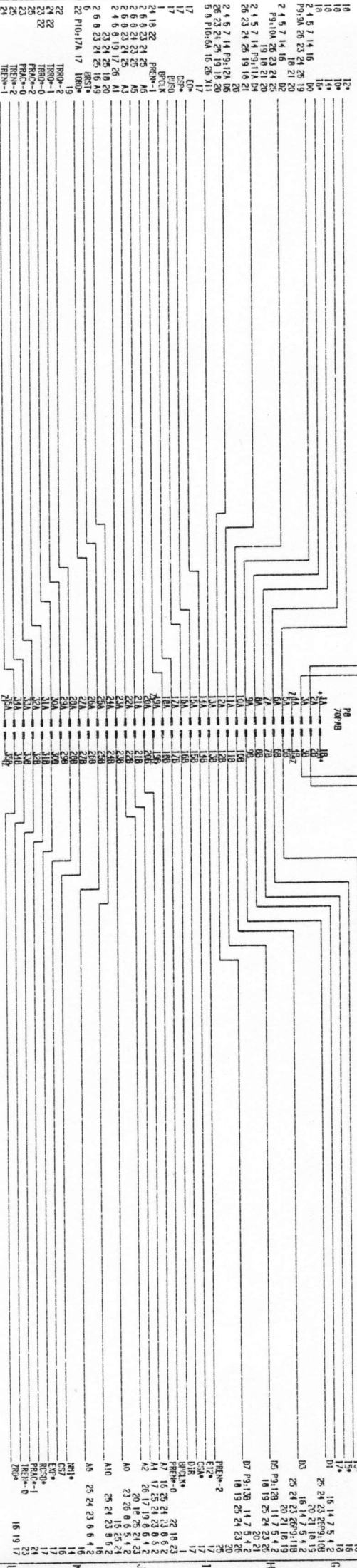
ty03_V24-kort

Display_unit_(Dsub)

Keyboard_(DIN)

ORA	1985-12-20	ABC1600
		CIRCUIT DIAGRAM

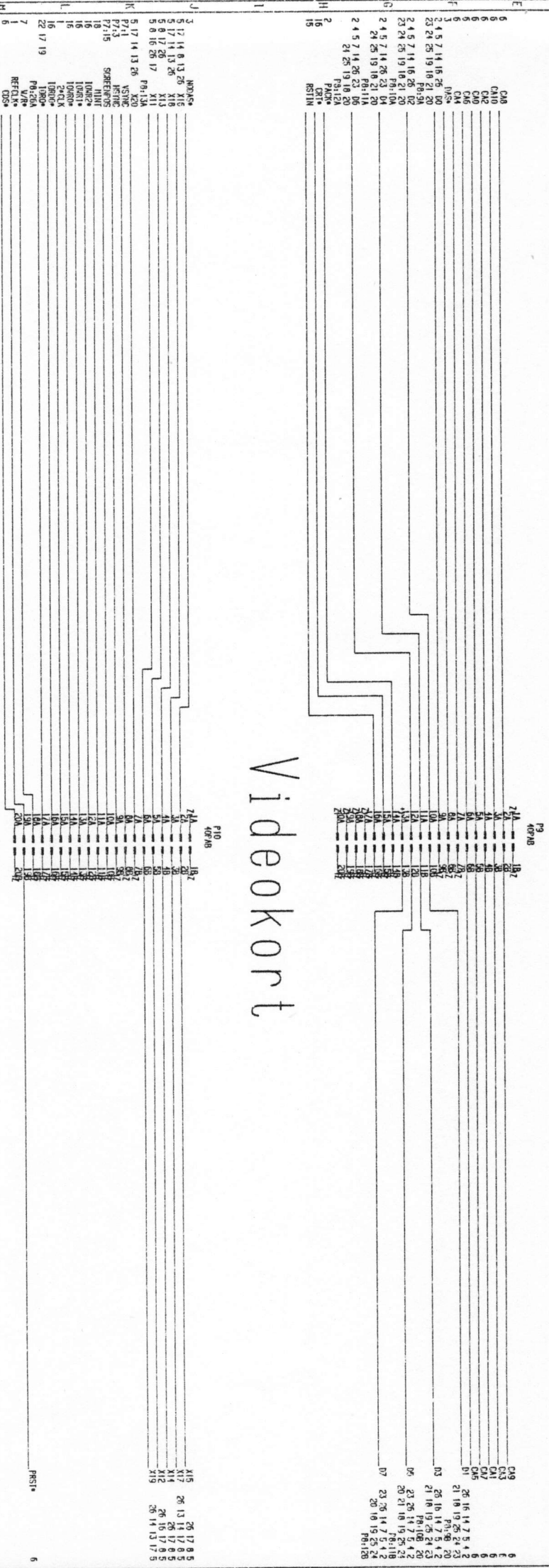
Power



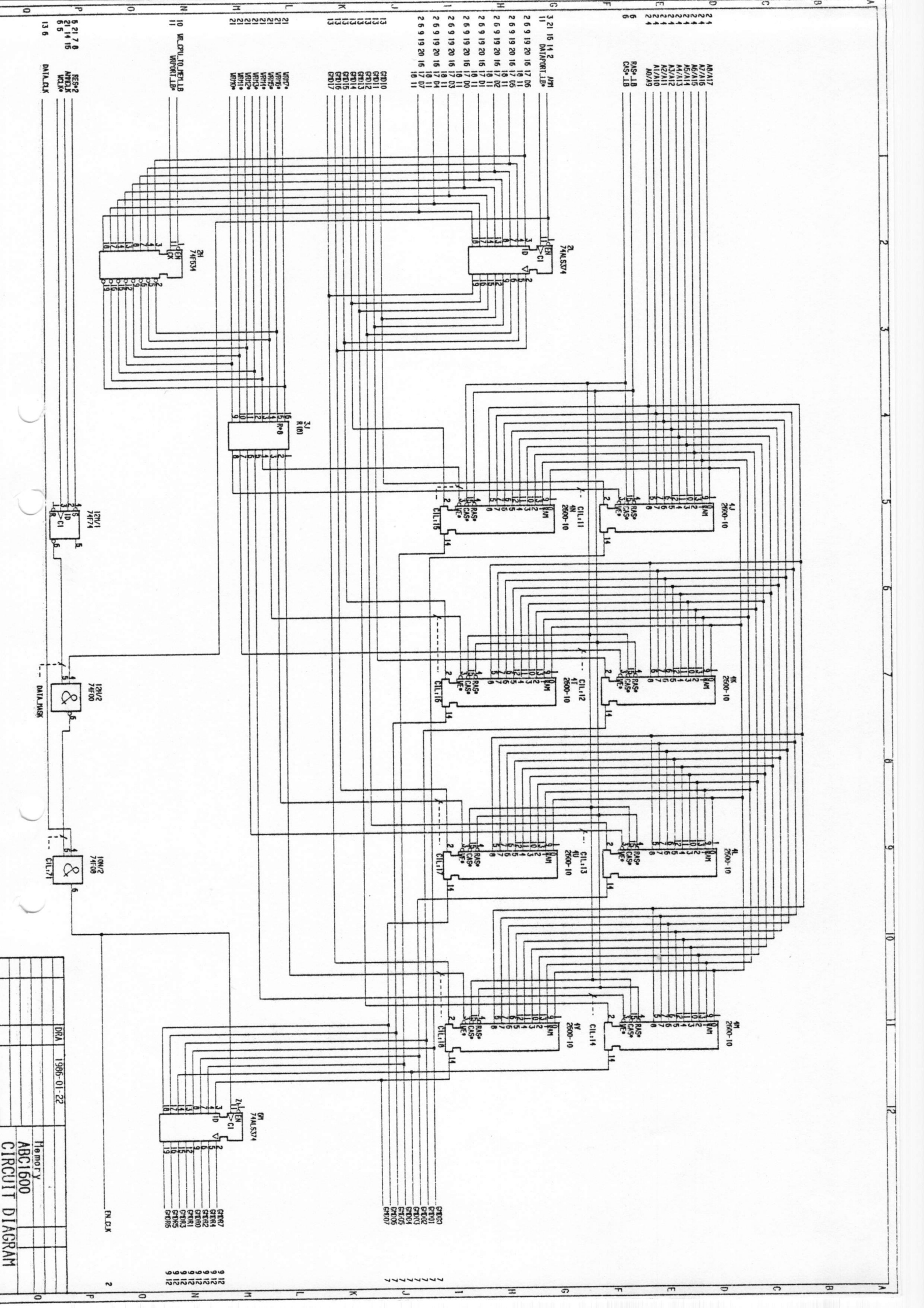
Busskort

BRN	1985-12-20
ABC1600	
CIRCUIT DIAGRAM	
002	

Videokort

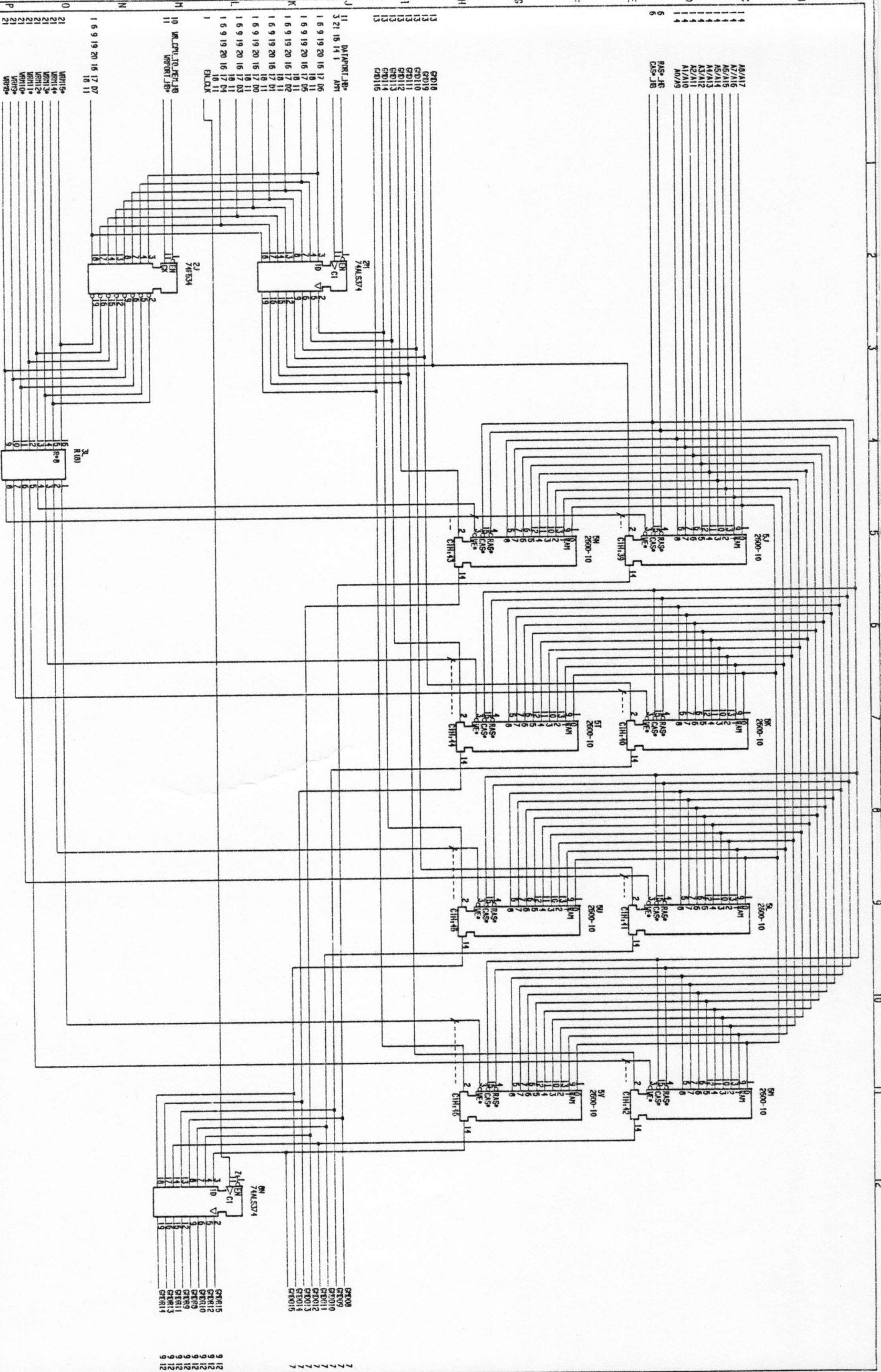


DRG	1905-12-20		
ABC1600			
CIRCUIT DIAGRAM			
103			

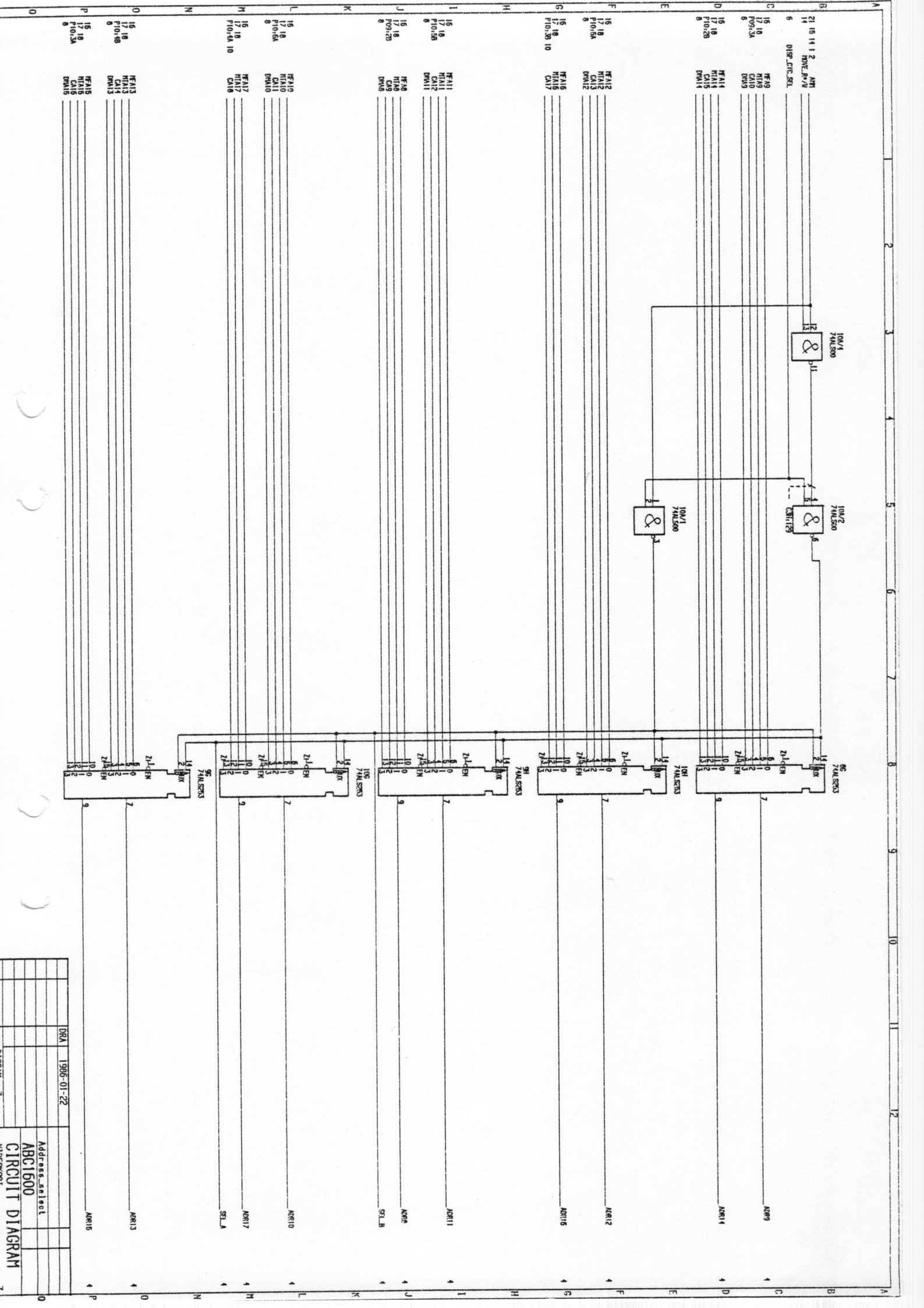


P 5.21.7.8
 21.14.15
 6.5
 13.6
 DATA BUS

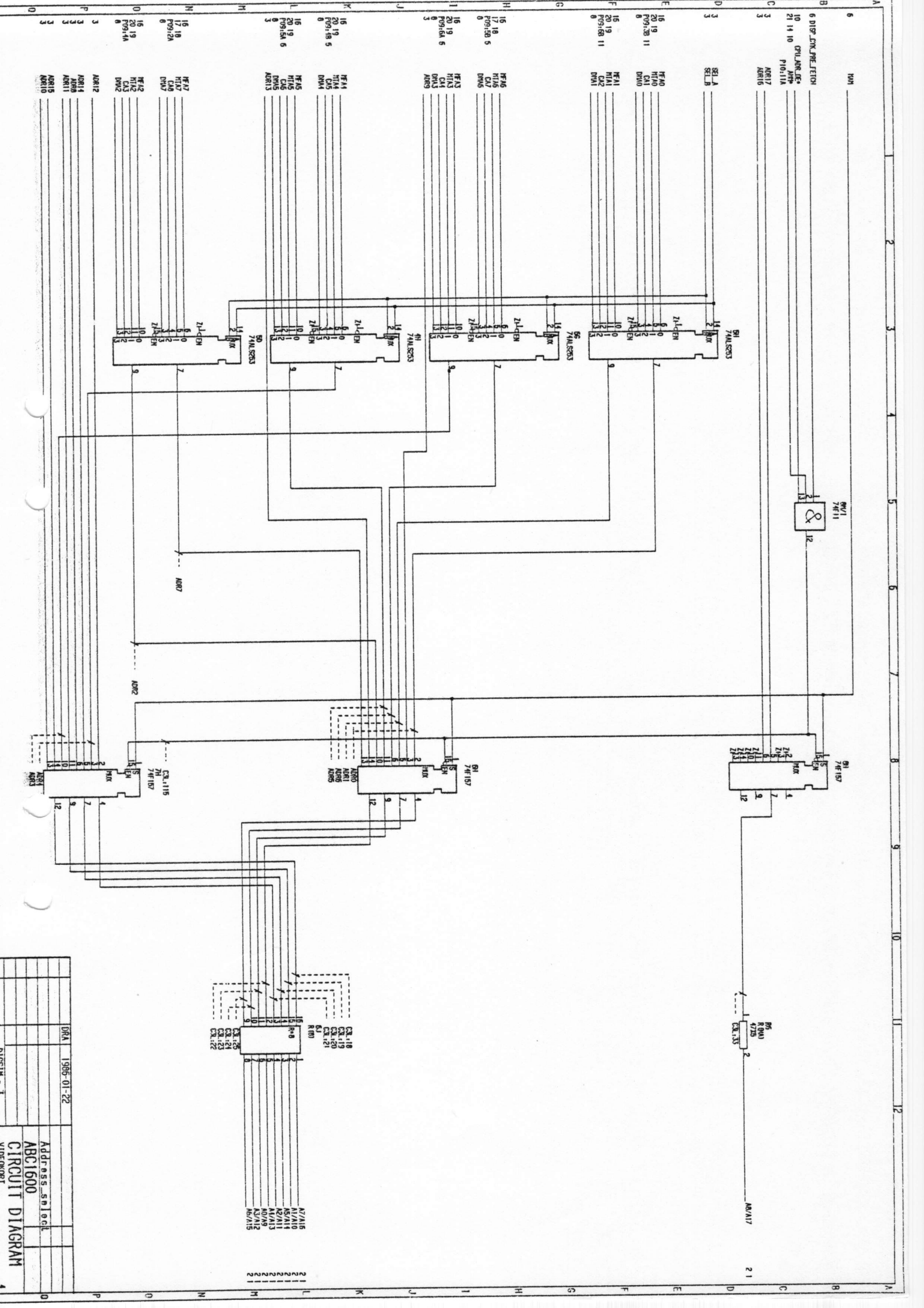
DRA 1966-01-22
 MEMORY
 ABC1600
 CIRCUIT DIAGRAM



DATE	1986-01-22
DESIGNER	Homerly
CHECKED	ABC1500
TITLE	CIRCUIT DIAGRAM
VIDEOMART	



ORA	1986-01-22	Address select
		ABC1600
		CIRCUIT DIAGRAM

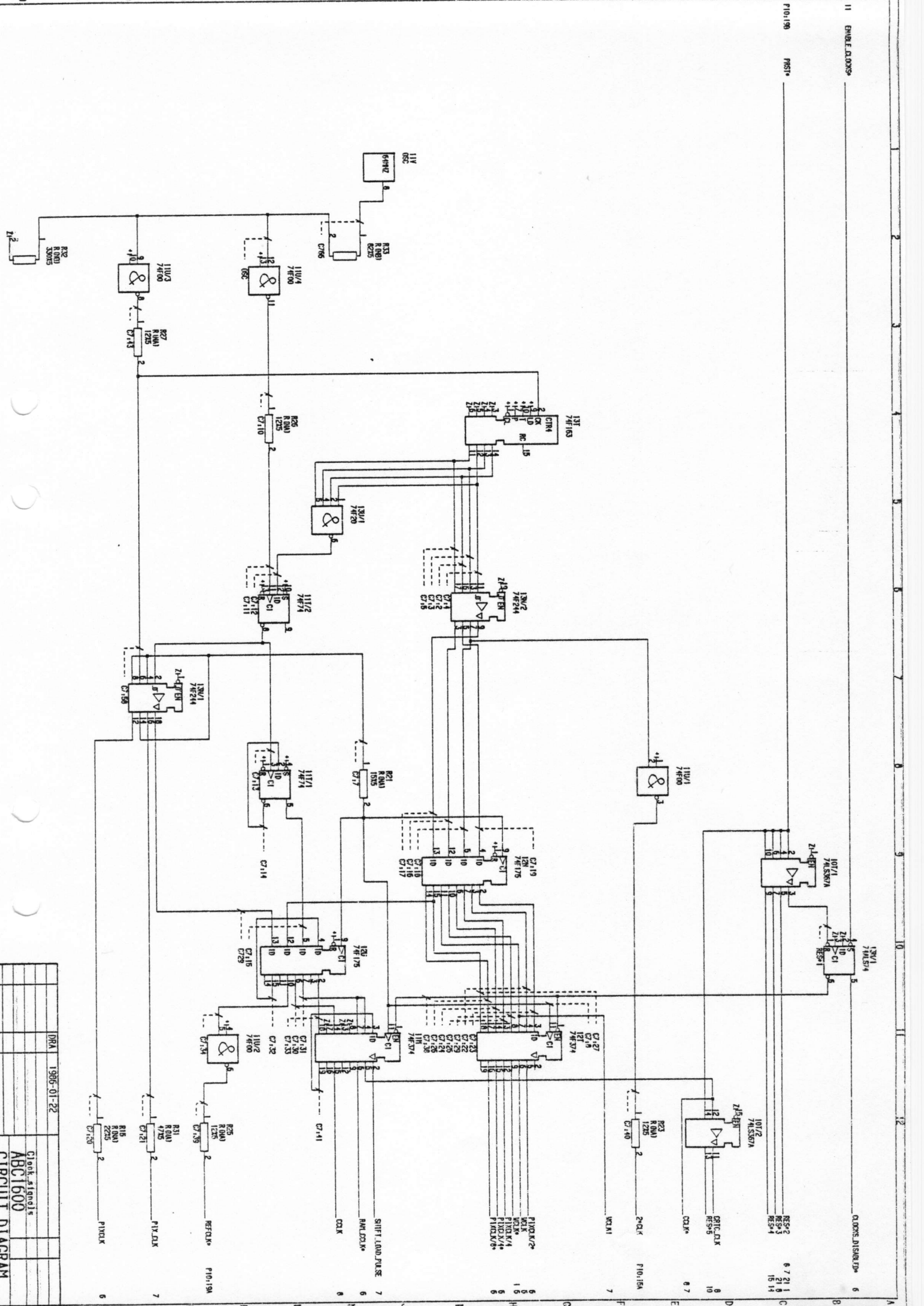


ORA 1986-01-22

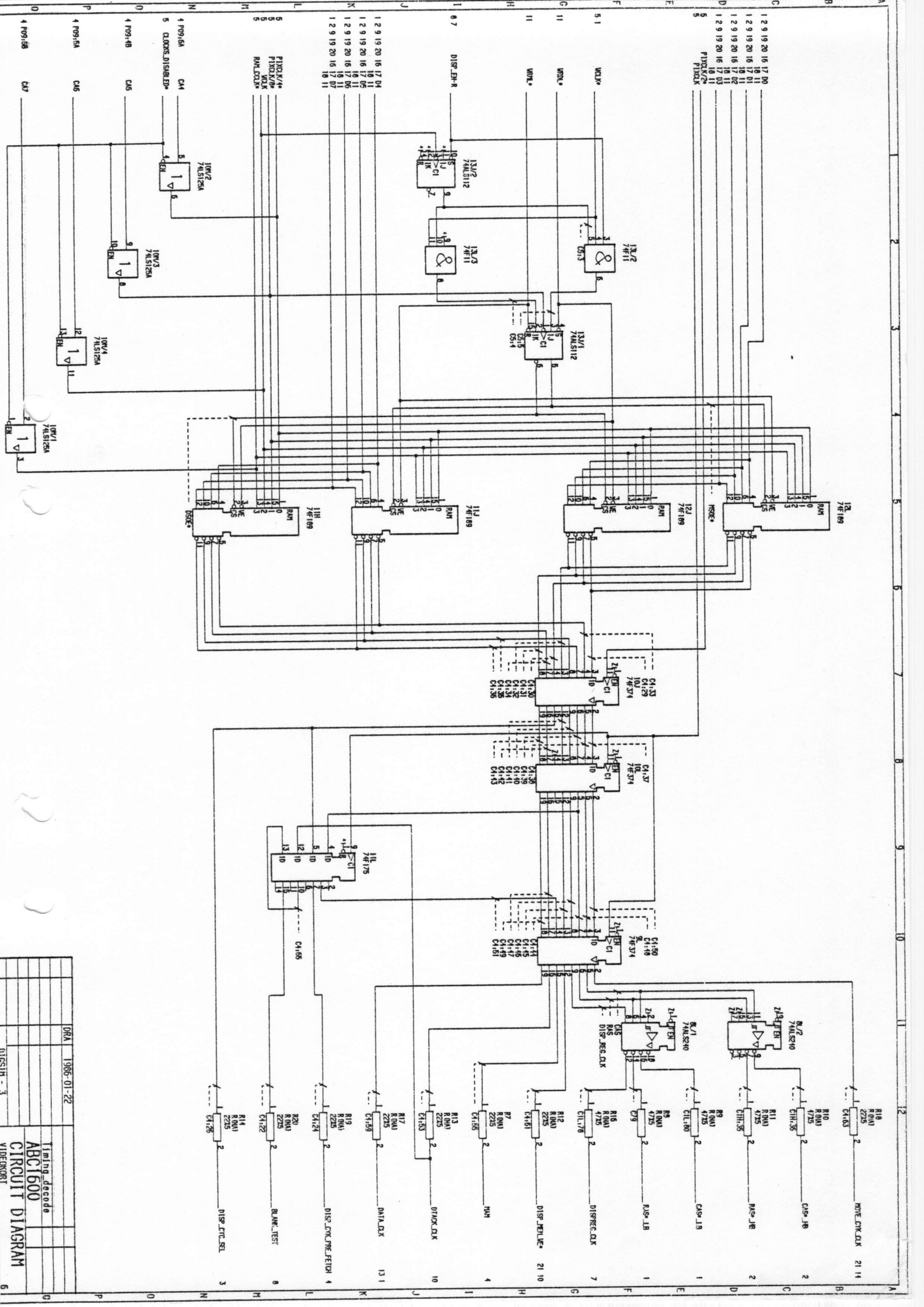
Address_sh19cl

ABC1600

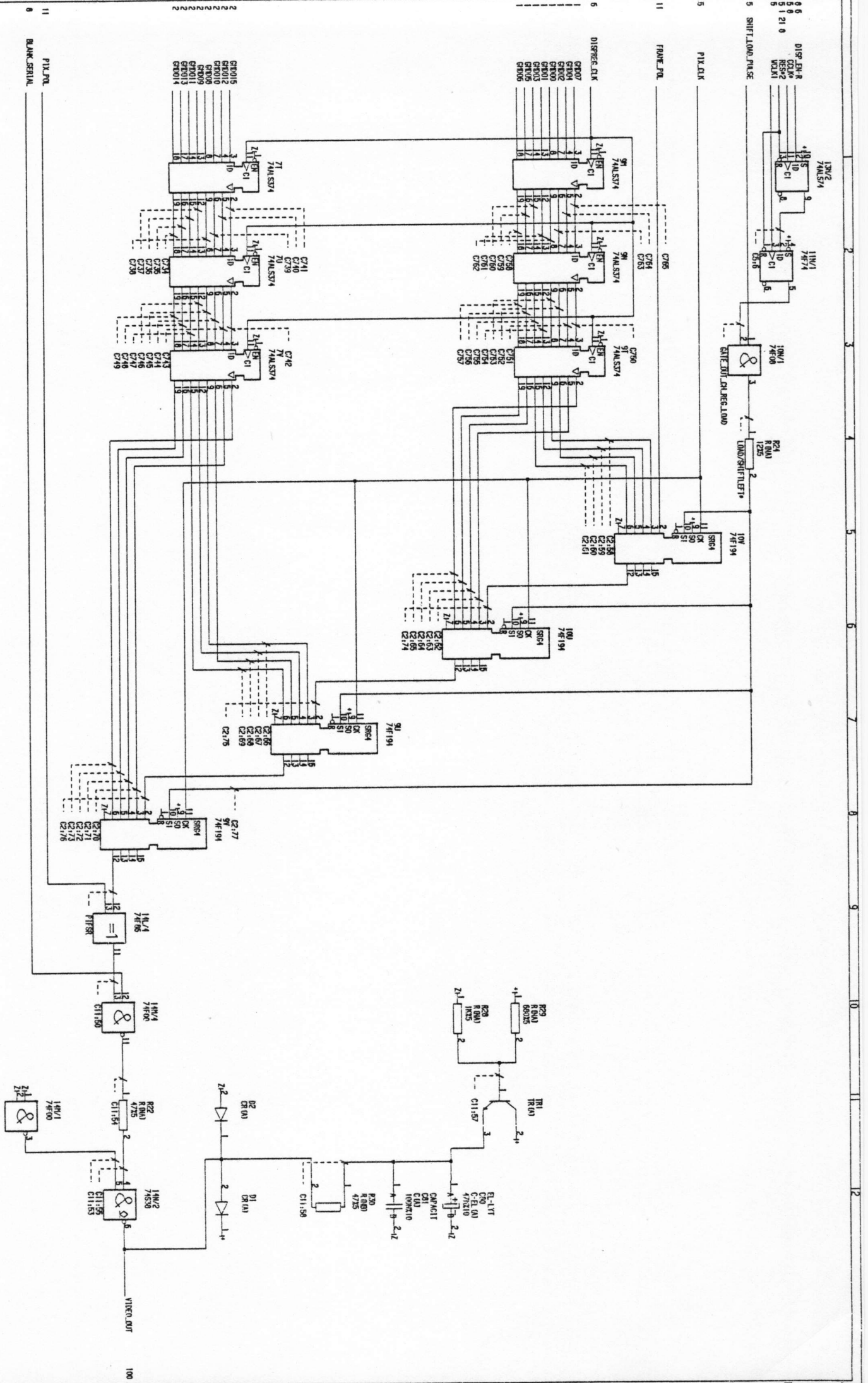
CIRCUIT DIAGRAM



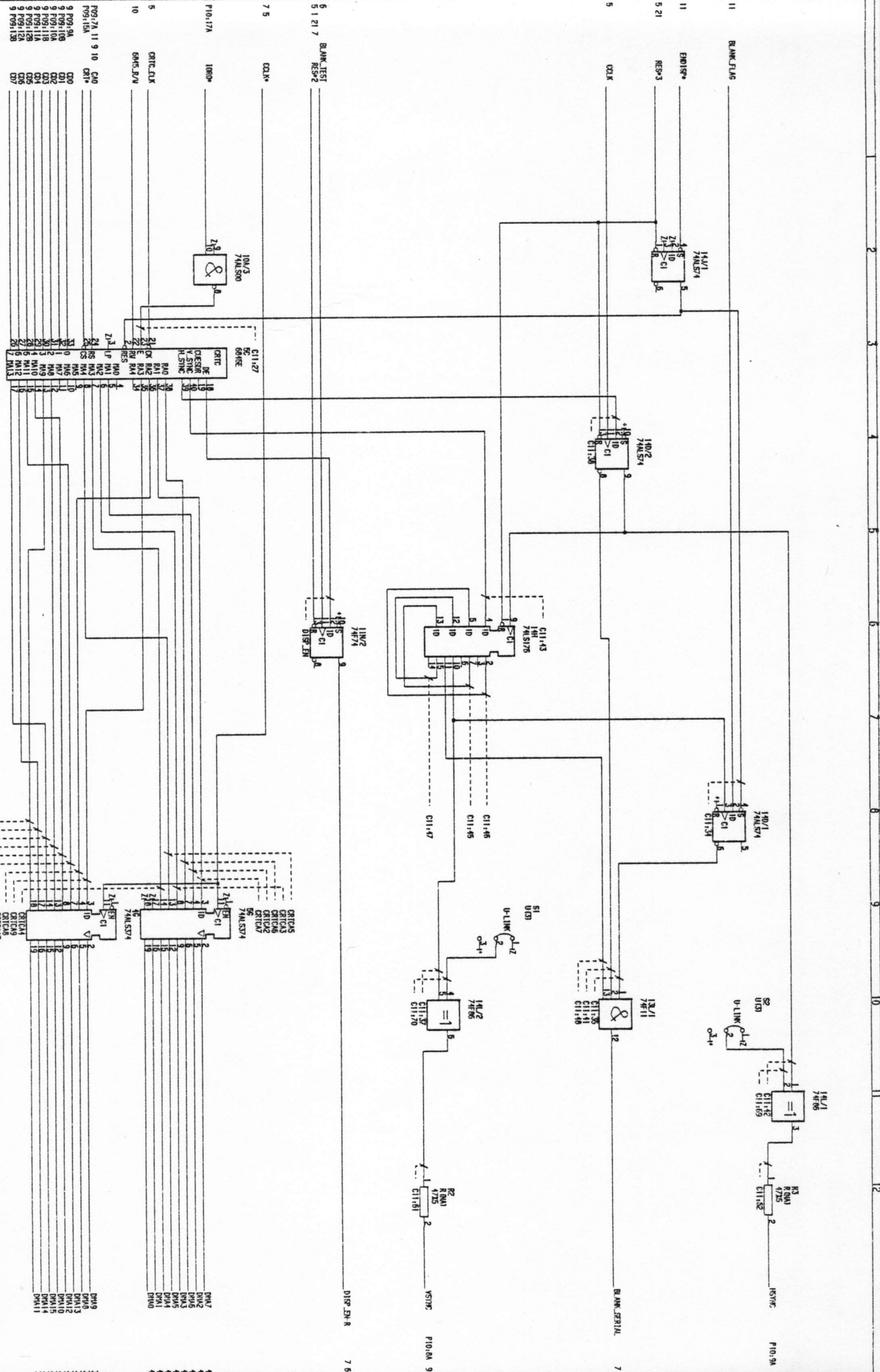
DRG	1905-01-22
Clock divider's	
ABC1600	
CIRCUIT DIAGRAM	



DR4	1966-01-22
Timing decode	
ABC1600	
CIRCUIT DIAGRAM	
D1SSH-3	
VIDEKORT	



ORA	1906-01-22
Video_output	
ABC1600	
CIRCUIT DIAGRAM	



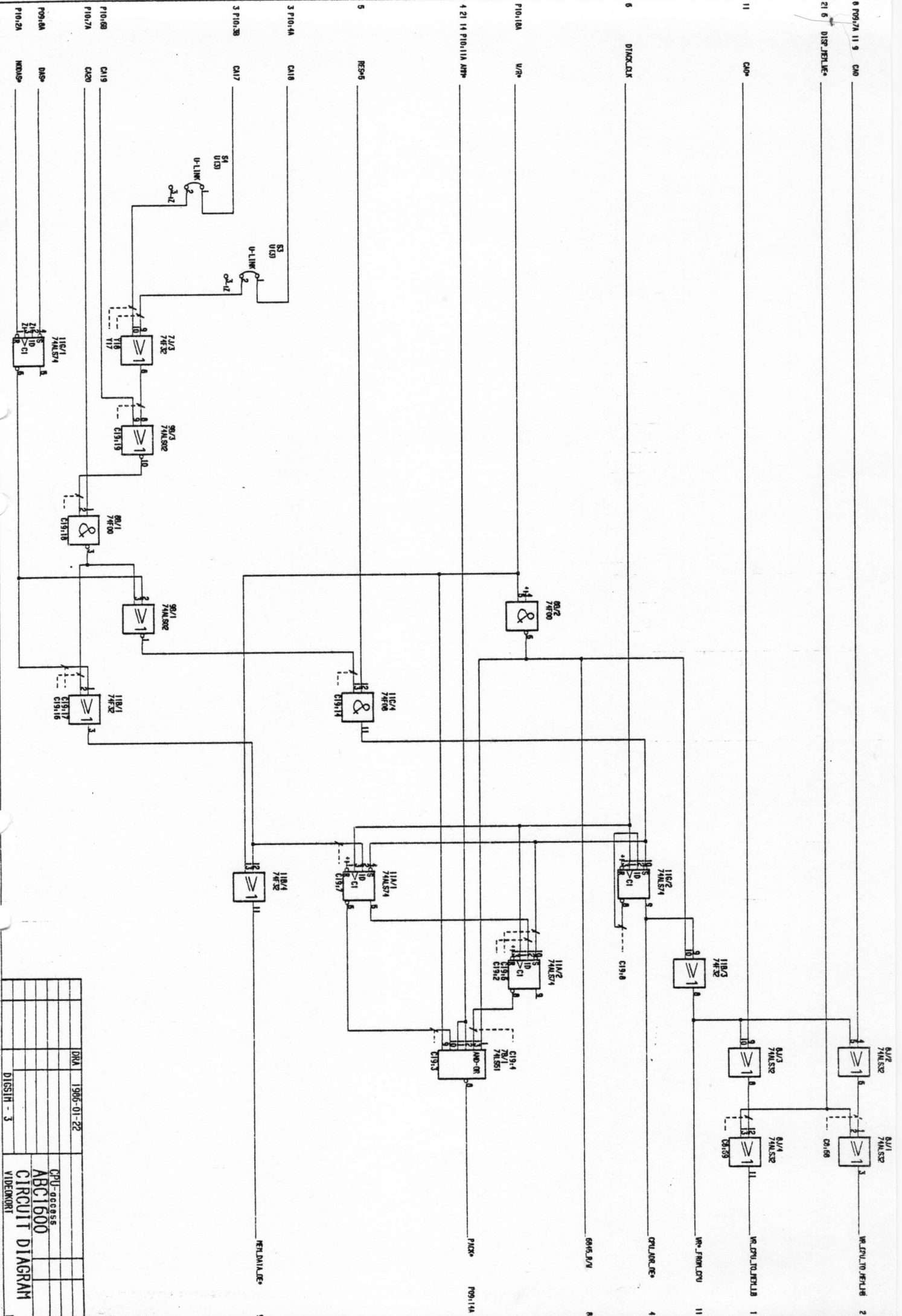
5 1 21 7 BANK_TEST
 RES*2
 7 5 CDLX*
 P10.17A 10R0*
 5 CRIC.DLX
 6M6.B/V
 10
 F09.7A 11 9 10 C/A0
 F09.15A CR1*
 9 F09.0A DD0
 9 F09.10B DD1
 9 F09.10A DD2
 9 F09.11B DD3
 9 F09.11A DD4
 9 F09.12B DD5
 9 F09.12A DD6
 9 F09.13B DD7

CRIC
 DE 10
 DRESK 10
 N SYNC 10
 M SYNC 10
 RAO 30
 R40 30
 R42 30
 R43 30
 R44 30
 R45 30
 R46 30
 R47 30
 R48 30
 R49 30
 R50 30
 R51 30
 R52 30
 R53 30
 R54 30
 R55 30
 R56 30
 R57 30
 R58 30
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 R61 30
 R62 30
 R63 30
 R64 30
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 R86 30
 R87 30
 R88 30
 R89 30
 R90 30
 R91 30
 R92 30
 R93 30
 R94 30
 R95 30
 R96 30
 R97 30
 R98 30
 R99 30
 R100 30

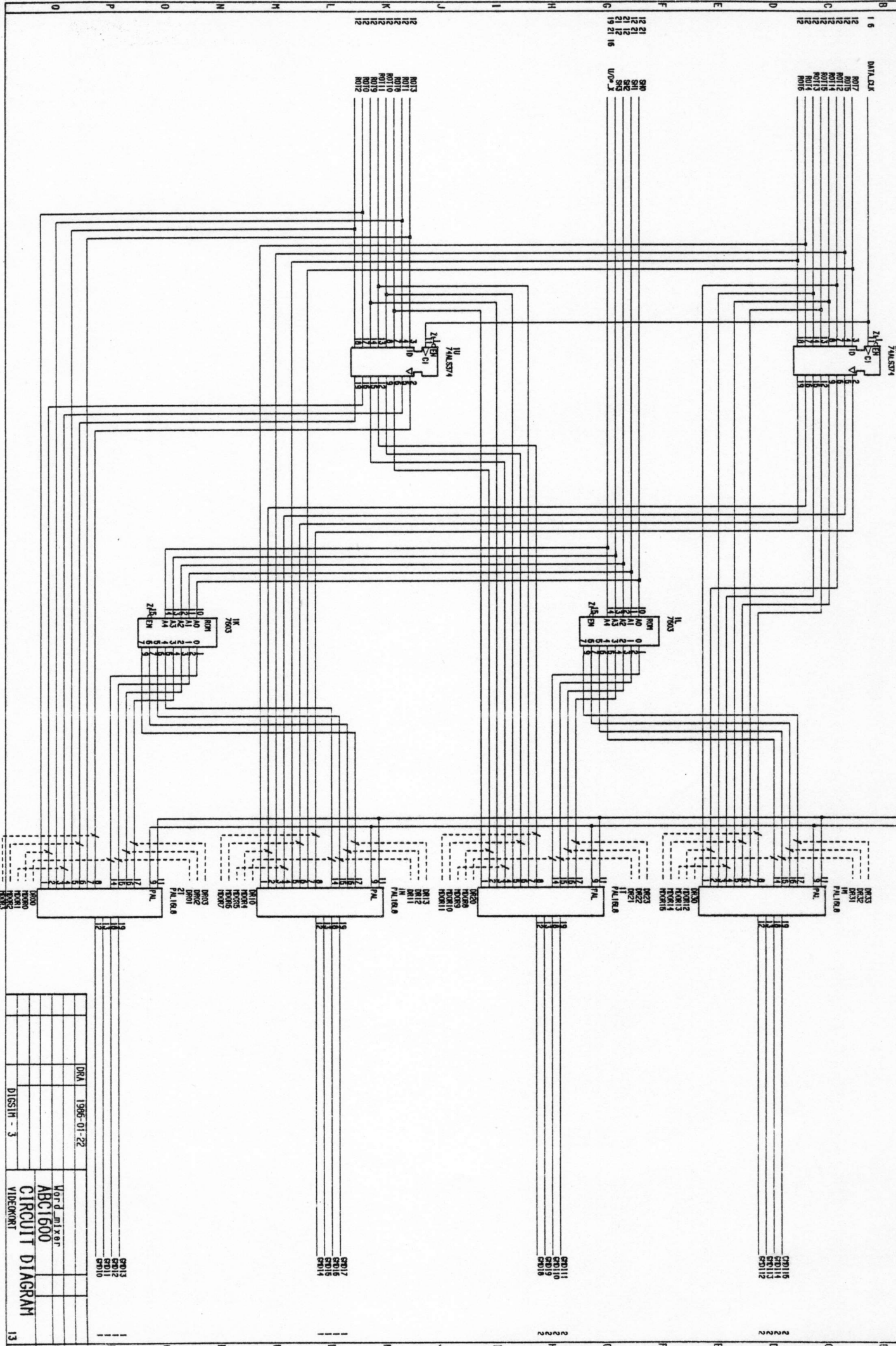
CRIC5
 CRIC45
 CRIC3
 CRIC26
 CRIC2
 CRIC17
 CRIC14
 CRIC11
 CRIC10
 CRIC9
 CRIC8
 CRIC7
 CRIC6
 CRIC5
 CRIC4
 CRIC3
 CRIC2
 CRIC1
 CRIC0

DM7
 DM6
 DM5
 DM4
 DM3
 DM2
 DM1
 DM0
 DM9
 DM13
 DM12
 DM11
 DM10
 DM15
 DM14
 DM11

DRA	1905-01-22
CRIC A. Blunking	
ABC1600	
CIRCUIT DIAGRAM	
VIDEORPT	



DWA	1986-01-22
CPU-access	
ABC1500	
CIRCUIT DIAGRAM	
VIDEO MONT	



NO13
NO14
NO15
NO16
NO17
NO18

SM0
SM1
SM2
SM3
W0-3

74ALS274
74ALS16

PAL16A8

V0-3

SM13
SM14
SM15
SM16
SM17
SM18
SM19
SM20

NO13
NO14
NO15
NO16
NO17
NO18

SM13
SM14
SM15
SM16
SM17
SM18
SM19
SM20

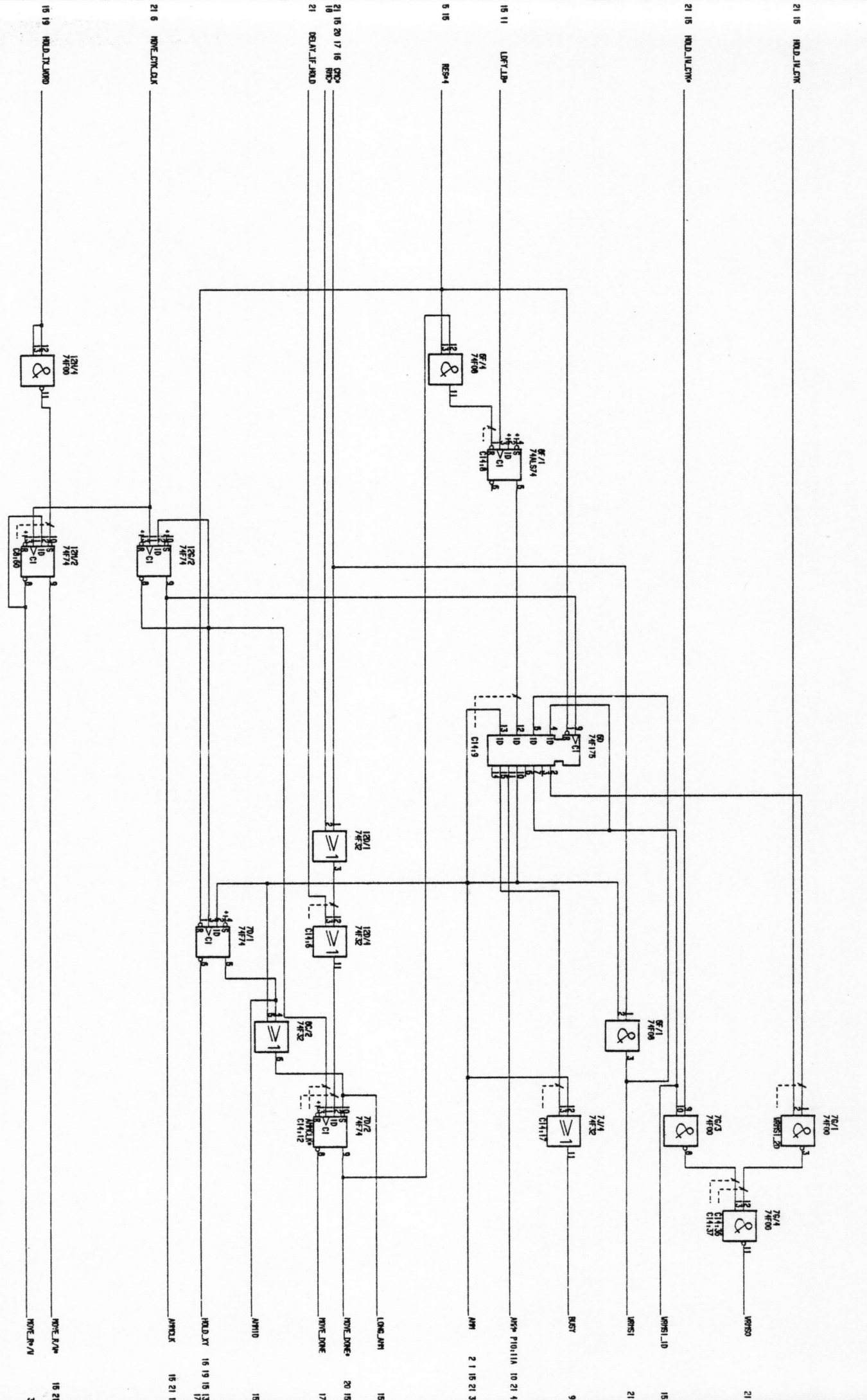
NO13
NO14
NO15
NO16
NO17
NO18

SM13
SM14
SM15
SM16
SM17
SM18
SM19
SM20

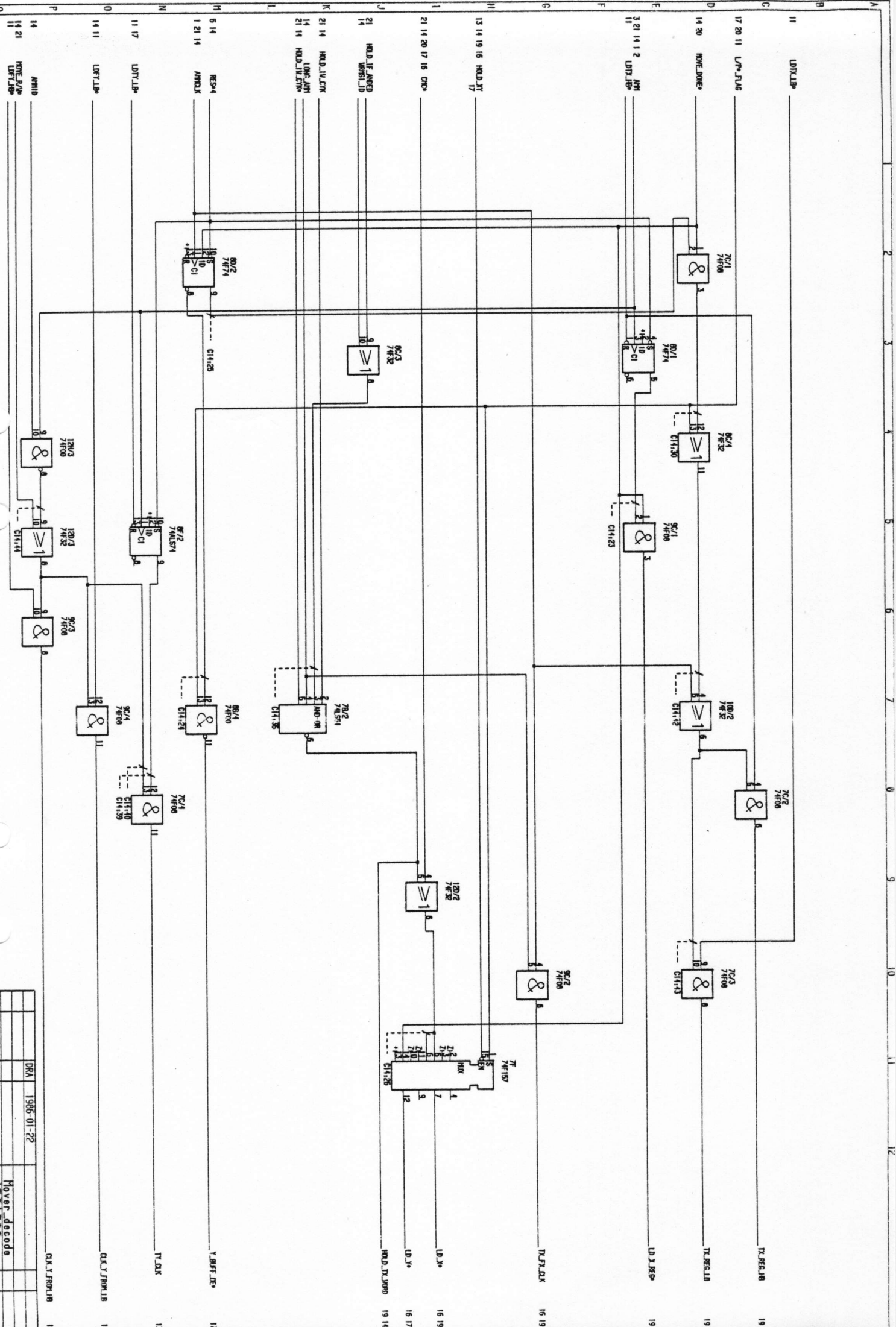
NO13
NO14
NO15
NO16
NO17
NO18

SM13
SM14
SM15
SM16
SM17
SM18
SM19
SM20

ORA	1966-01-22
Word mixer ABC1600 CIRCUIT DIAGRAM	
VIDEOPORT	
DISINH - 3	

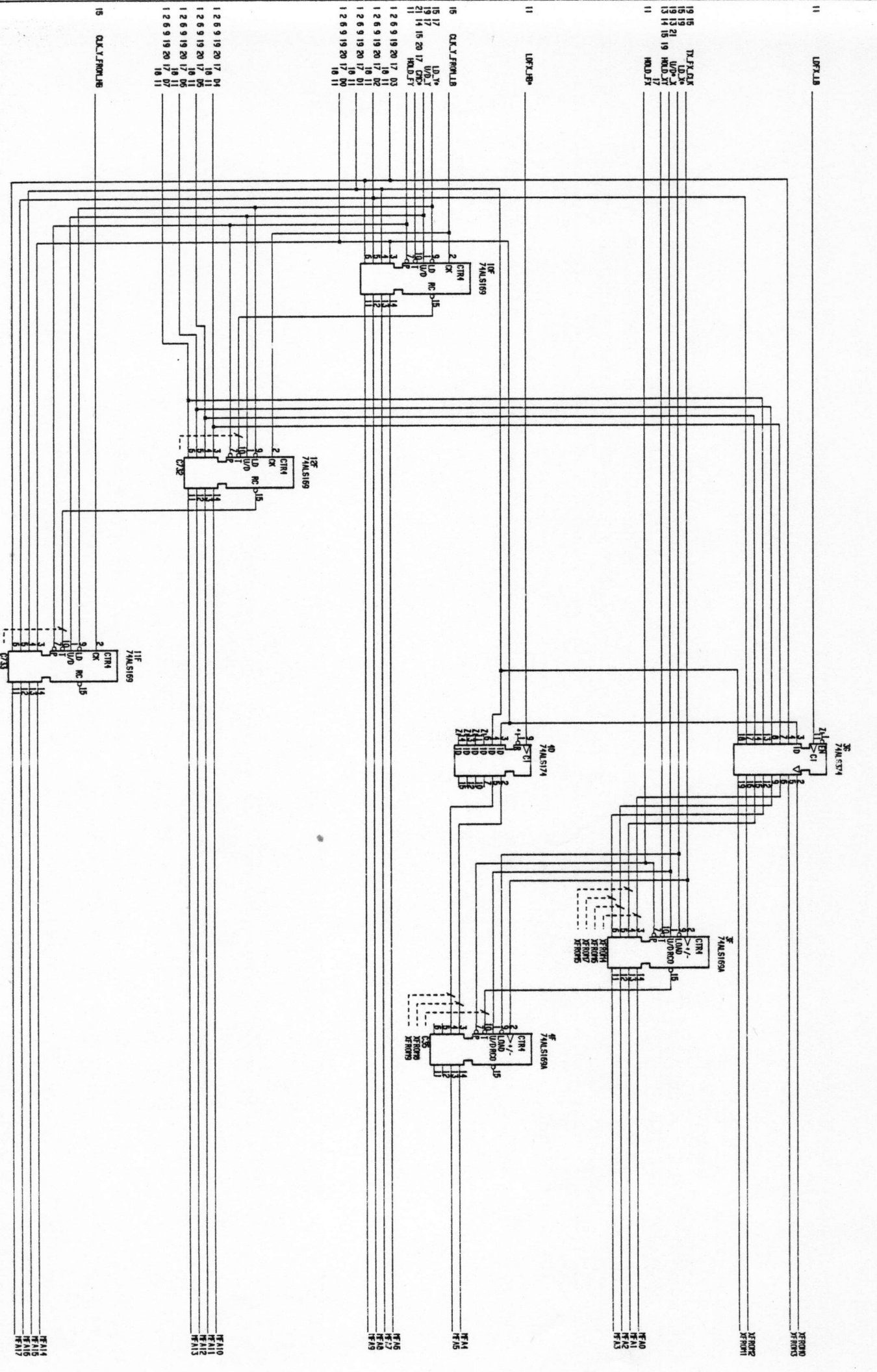


DRA	1906-01-22	Hover-Stale
		ABC1600
		CIRCUIT DIAGRAM

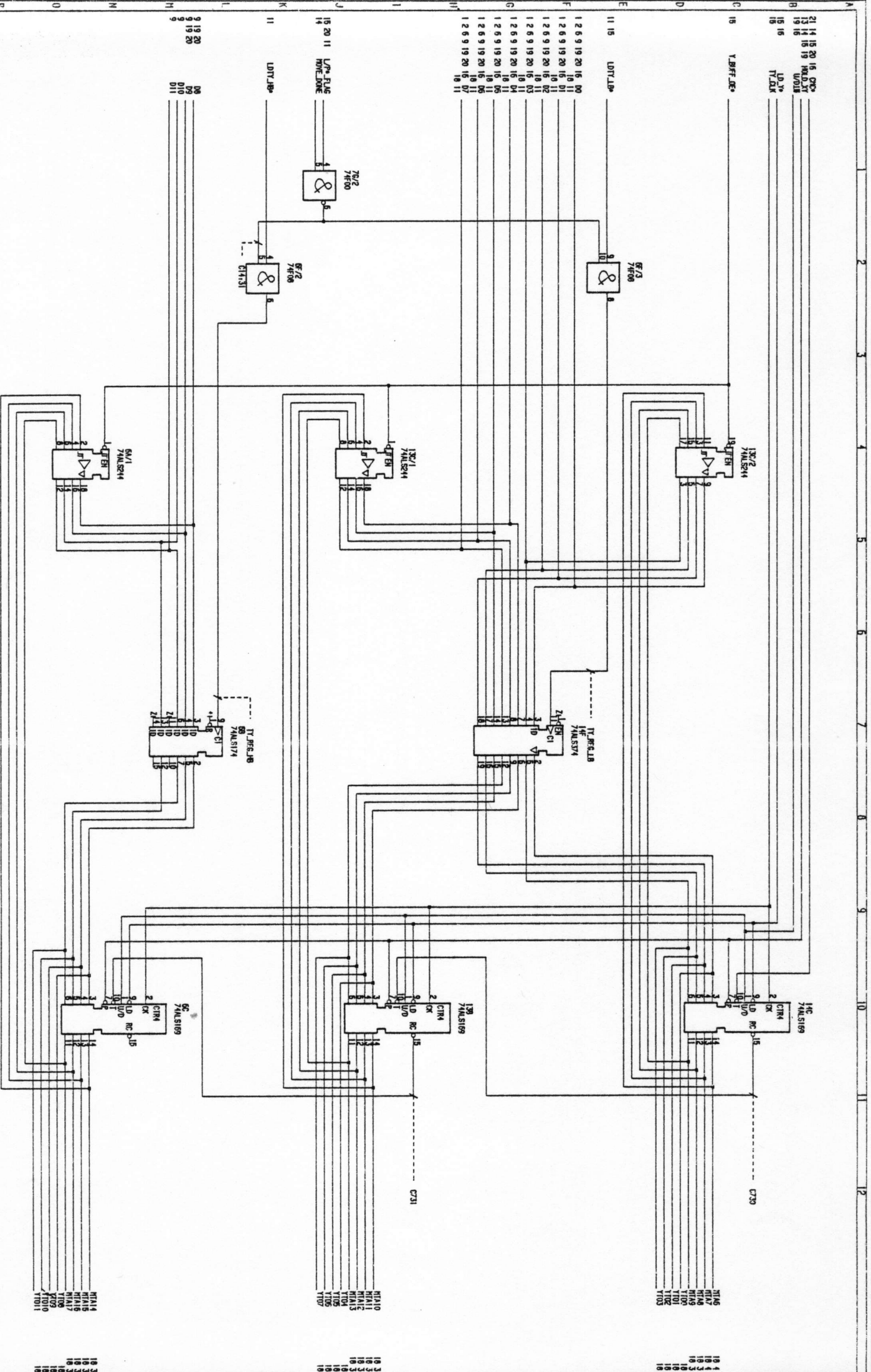


ORA	1966-01-22	CLX FROM LB
Hover decode		
ABC1600		
CIRCUIT DIAGRAM		
VIDEOCORT		

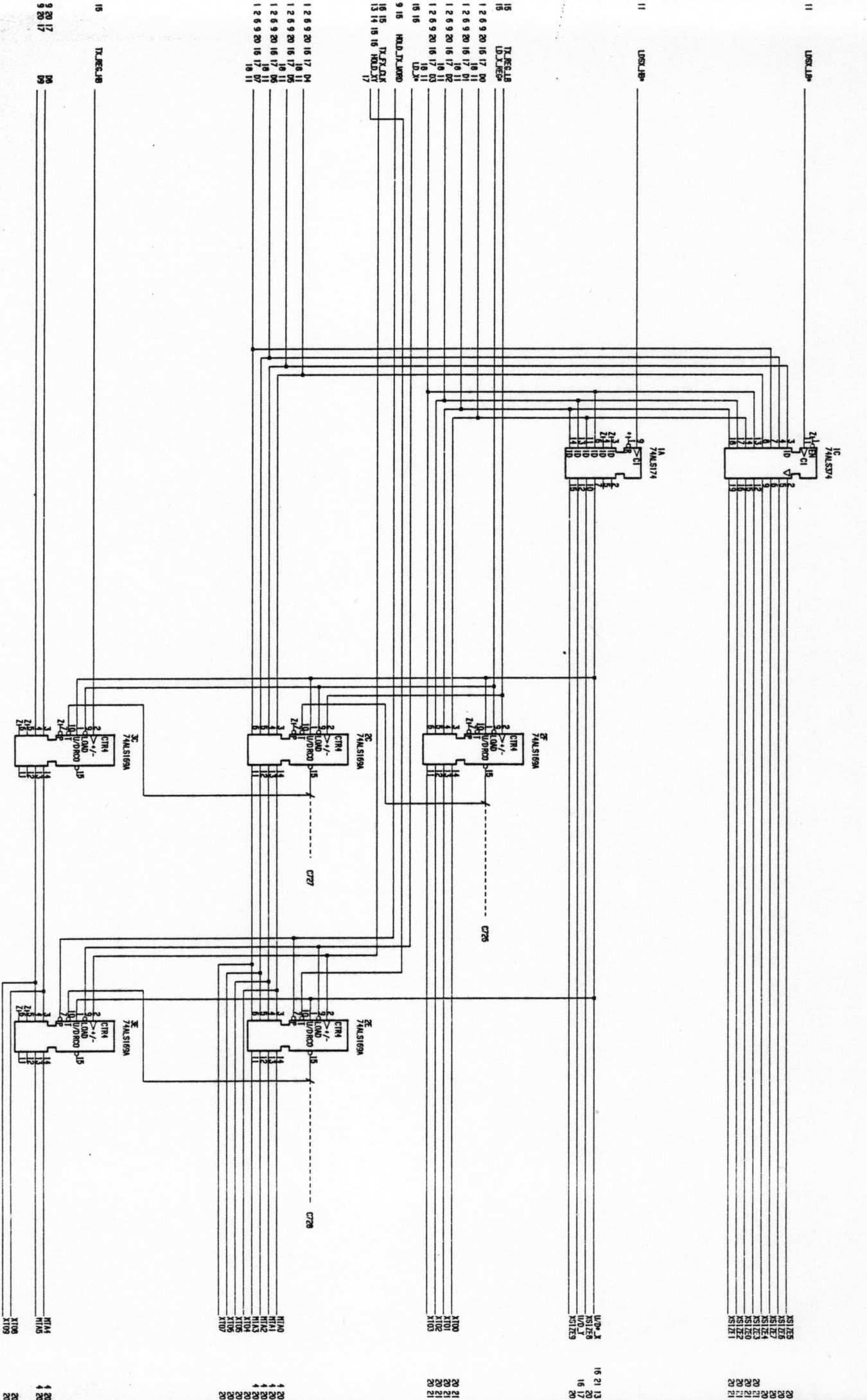
DISINH - 3



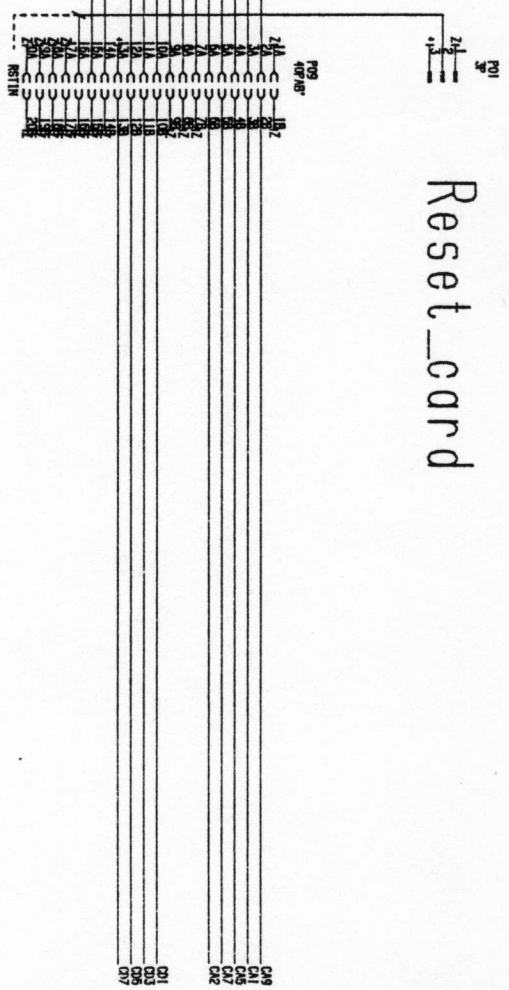
ORA	1965-01-22
From address X.A.1	
ABC1600	
CIRCUIT DIAGRAM	
VIDENCORET	



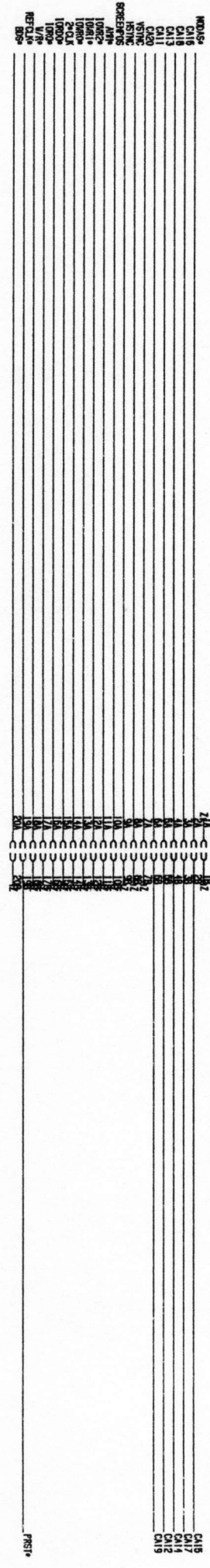
DRA	1986-01-22
Hover, J. To address	
ABC1500	
CIRCUIT DIAGRAM	



DRG	1986-01-22
Hover, X size J, add.	
ABC1600	
CIRCUIT DIAGRAM	
WIRENOO	
XT09	
XT08	
XT07	
XT06	
XT05	
XT04	
XT03	
XT02	
XT01	
XT00	

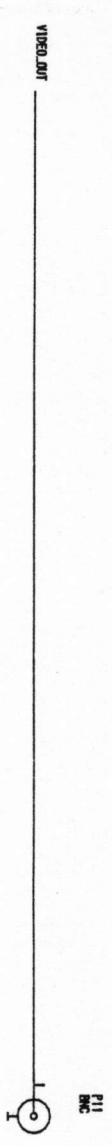


CPU-card

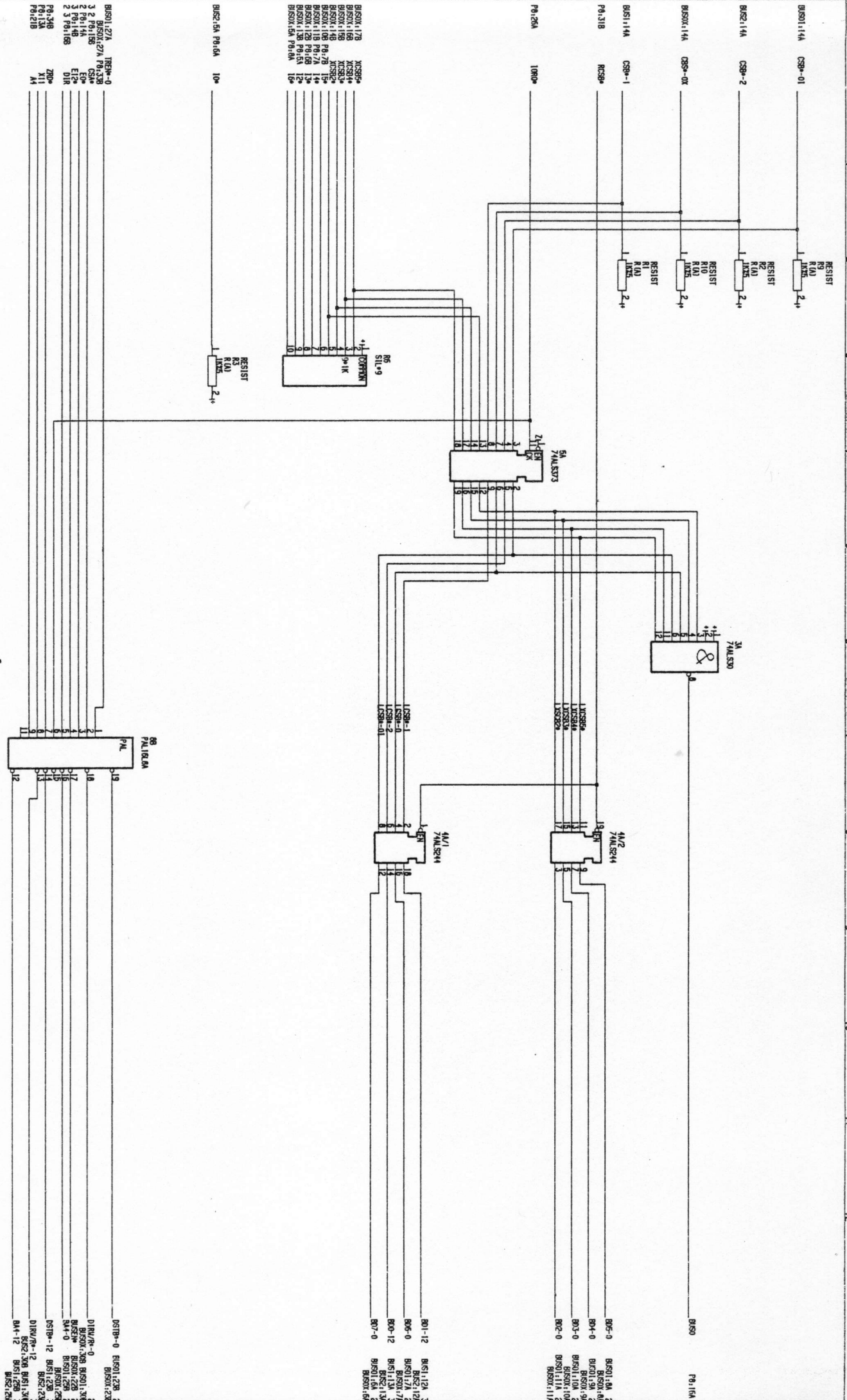


Video_output

Power

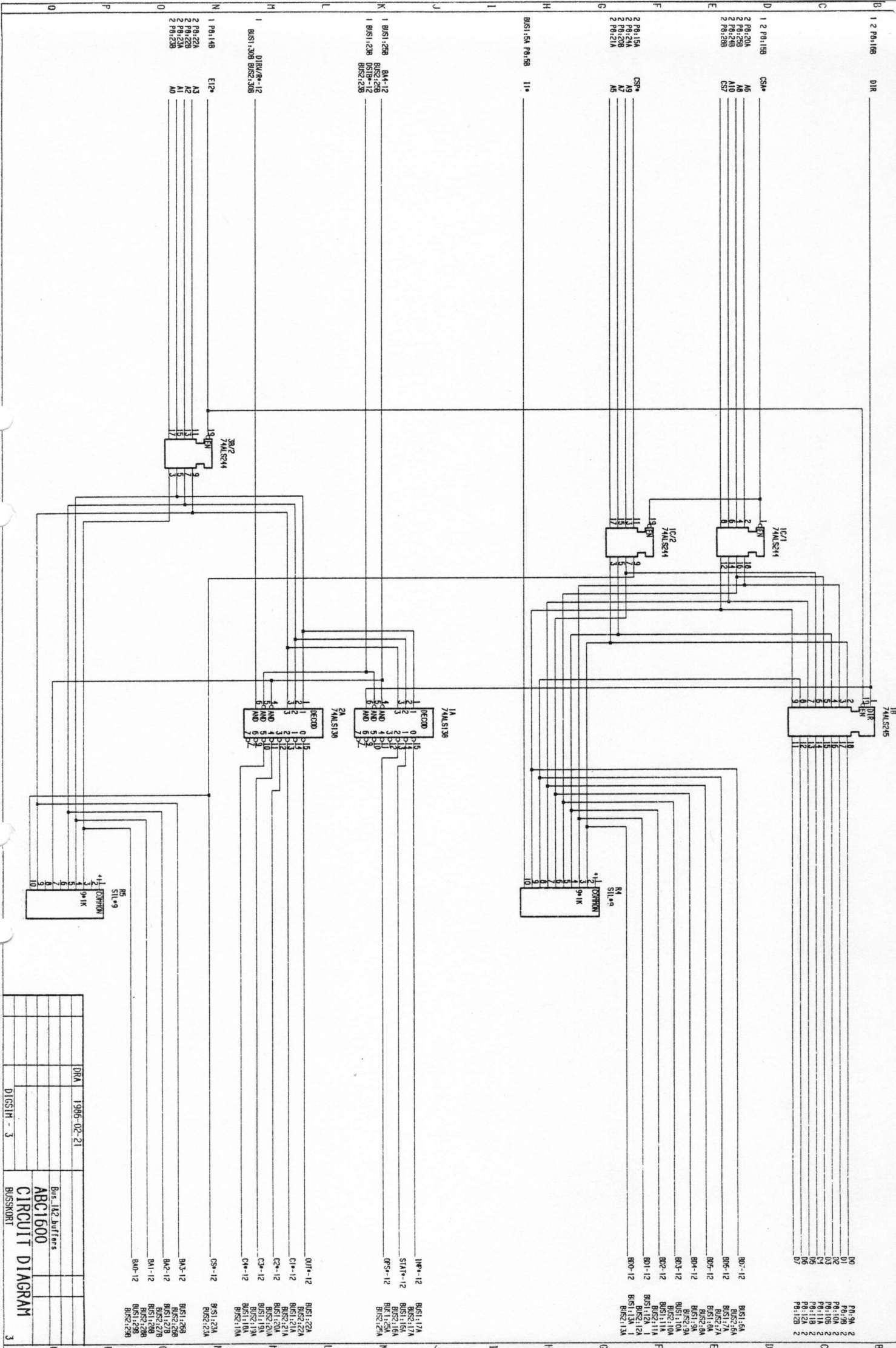


DATE	1986-01-22
DESIGN - X	
ABCT600	
CIRCUIT DIAGRAM	
VIDEOWORT	
100	



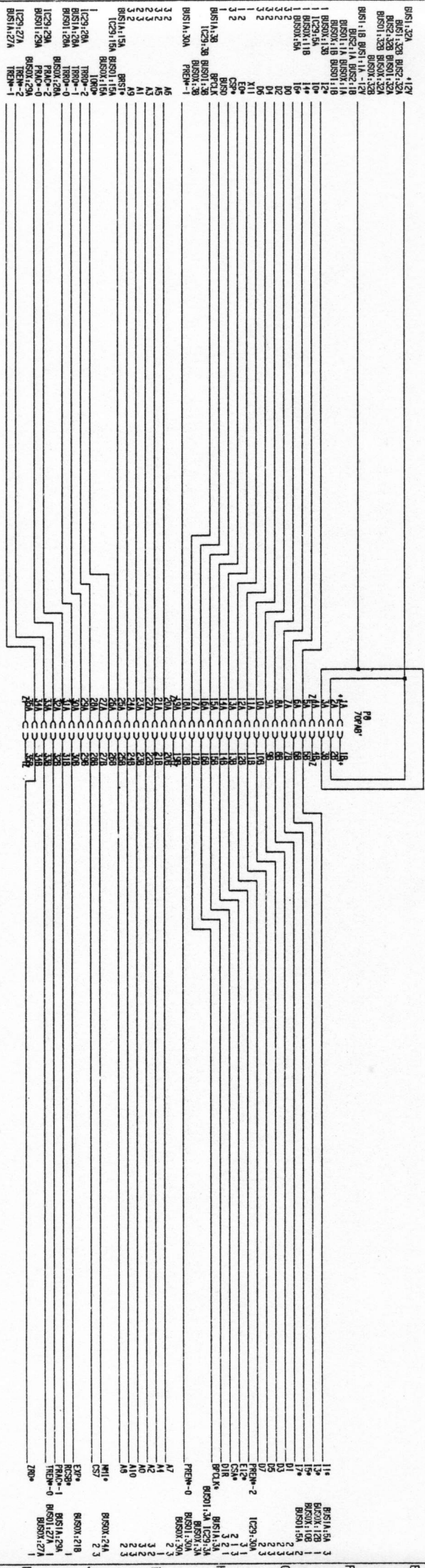
DRA	1986-02-21
CSB I Decode ABC1600 CIRCUIT DIAGRAM	
ISSORI	

BUS01:27A	TRM-0
BUS02:27A	TRM-0
BUS03:27A	TRM-0
BUS04:27A	TRM-0
BUS05:27A	TRM-0
BUS06:27A	TRM-0
BUS07:27A	TRM-0
BUS08:27A	TRM-0
BUS09:27A	TRM-0
BUS10:27A	TRM-0
BUS11:27A	TRM-0
BUS12:27A	TRM-0
BUS13:27A	TRM-0
BUS14:27A	TRM-0
BUS15:27A	TRM-0
BUS16:27A	TRM-0
BUS17:27A	TRM-0
BUS18:27A	TRM-0
BUS19:27A	TRM-0
BUS20:27A	TRM-0
BUS21:27A	TRM-0
BUS22:27A	TRM-0
BUS23:27A	TRM-0
BUS24:27A	TRM-0
BUS25:27A	TRM-0
BUS26:27A	TRM-0
BUS27:27A	TRM-0
BUS28:27A	TRM-0
BUS29:27A	TRM-0
BUS30:27A	TRM-0
BUS31:27A	TRM-0
BUS32:27A	TRM-0
BUS33:27A	TRM-0
BUS34:27A	TRM-0
BUS35:27A	TRM-0
BUS36:27A	TRM-0
BUS37:27A	TRM-0
BUS38:27A	TRM-0
BUS39:27A	TRM-0
BUS40:27A	TRM-0
BUS41:27A	TRM-0
BUS42:27A	TRM-0
BUS43:27A	TRM-0
BUS44:27A	TRM-0
BUS45:27A	TRM-0
BUS46:27A	TRM-0
BUS47:27A	TRM-0
BUS48:27A	TRM-0
BUS49:27A	TRM-0
BUS50:27A	TRM-0
BUS51:27A	TRM-0
BUS52:27A	TRM-0
BUS53:27A	TRM-0
BUS54:27A	TRM-0
BUS55:27A	TRM-0
BUS56:27A	TRM-0
BUS57:27A	TRM-0
BUS58:27A	TRM-0
BUS59:27A	TRM-0
BUS60:27A	TRM-0
BUS61:27A	TRM-0
BUS62:27A	TRM-0
BUS63:27A	TRM-0
BUS64:27A	TRM-0
BUS65:27A	TRM-0
BUS66:27A	TRM-0
BUS67:27A	TRM-0
BUS68:27A	TRM-0
BUS69:27A	TRM-0
BUS70:27A	TRM-0
BUS71:27A	TRM-0
BUS72:27A	TRM-0
BUS73:27A	TRM-0
BUS74:27A	TRM-0
BUS75:27A	TRM-0
BUS76:27A	TRM-0
BUS77:27A	TRM-0
BUS78:27A	TRM-0
BUS79:27A	TRM-0
BUS80:27A	TRM-0
BUS81:27A	TRM-0
BUS82:27A	TRM-0
BUS83:27A	TRM-0
BUS84:27A	TRM-0
BUS85:27A	TRM-0
BUS86:27A	TRM-0
BUS87:27A	TRM-0
BUS88:27A	TRM-0
BUS89:27A	TRM-0
BUS90:27A	TRM-0
BUS91:27A	TRM-0
BUS92:27A	TRM-0
BUS93:27A	TRM-0
BUS94:27A	TRM-0
BUS95:27A	TRM-0
BUS96:27A	TRM-0
BUS97:27A	TRM-0
BUS98:27A	TRM-0
BUS99:27A	TRM-0
BUS100:27A	TRM-0



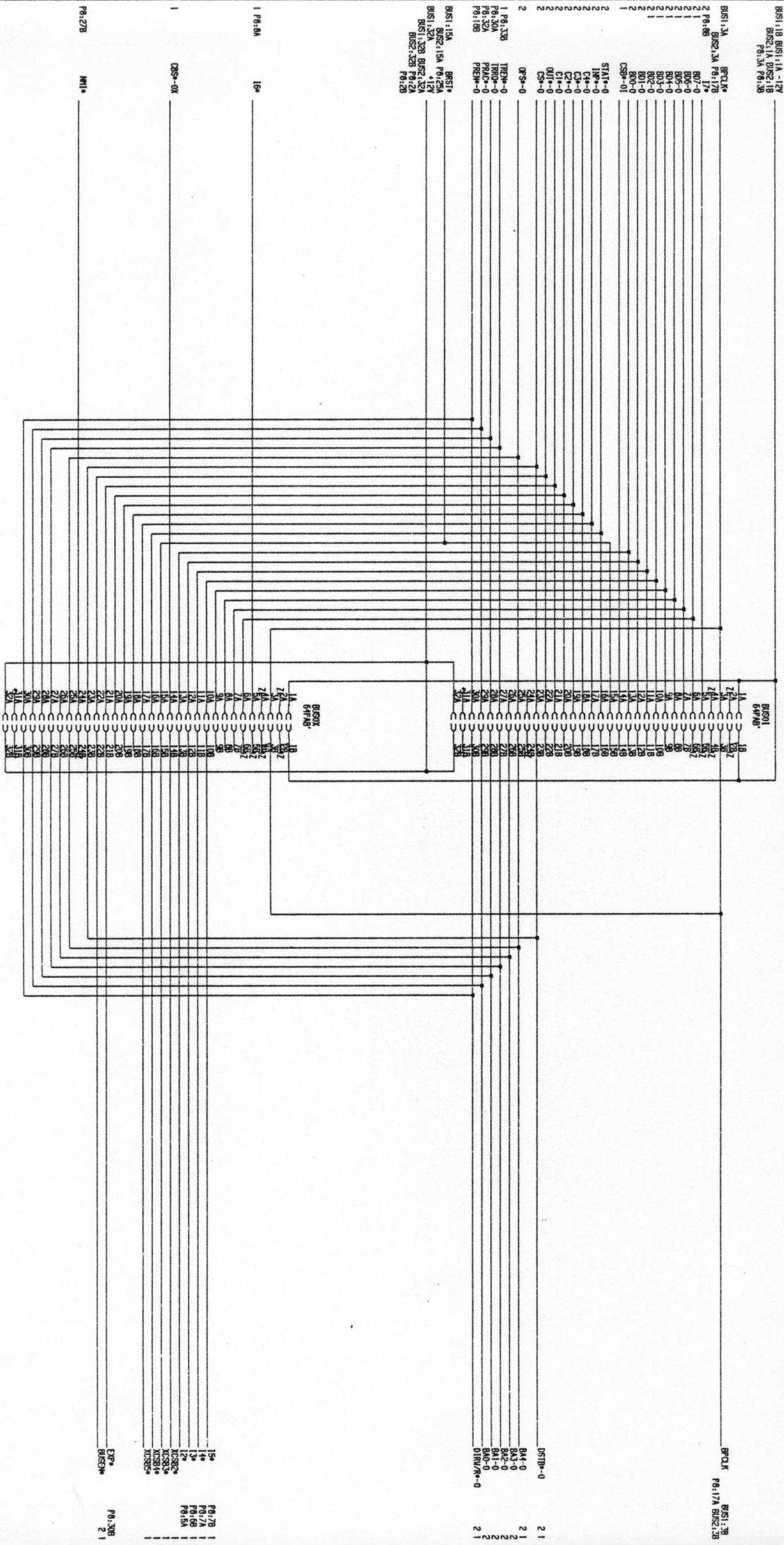
DIRA	1965-02-21	Bus 142 buffers
		ABC1600
		CIRCUIT DIAGRAM
		BUSSMORT

Processorkort



DRK	1985-12-18				
ABC1600					
CIRCUIT DIAGRAM					
BUSSKORT					
DIGSIH - 3					
100					

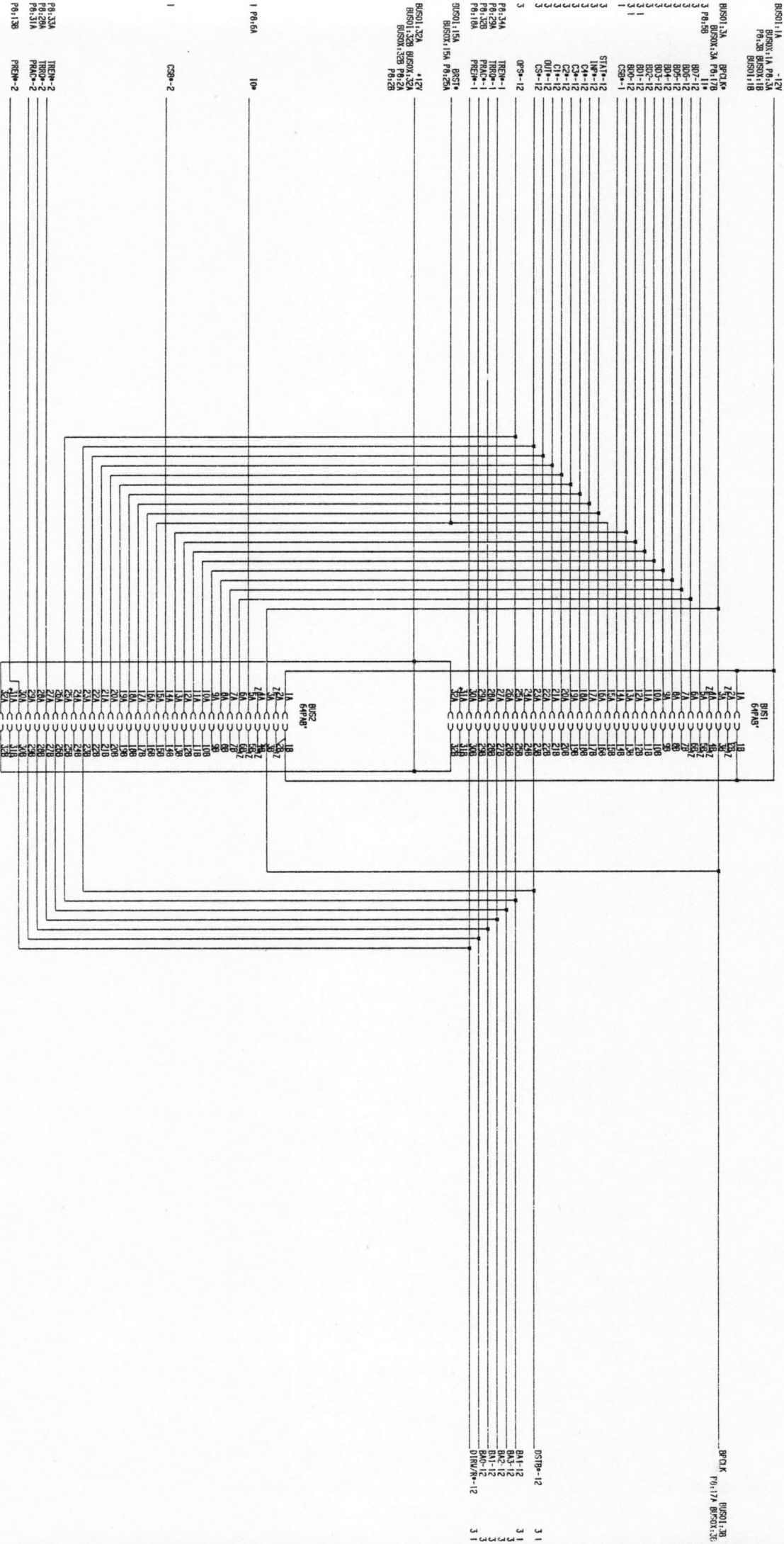
Bus_0_intern



Bus_0_expansion

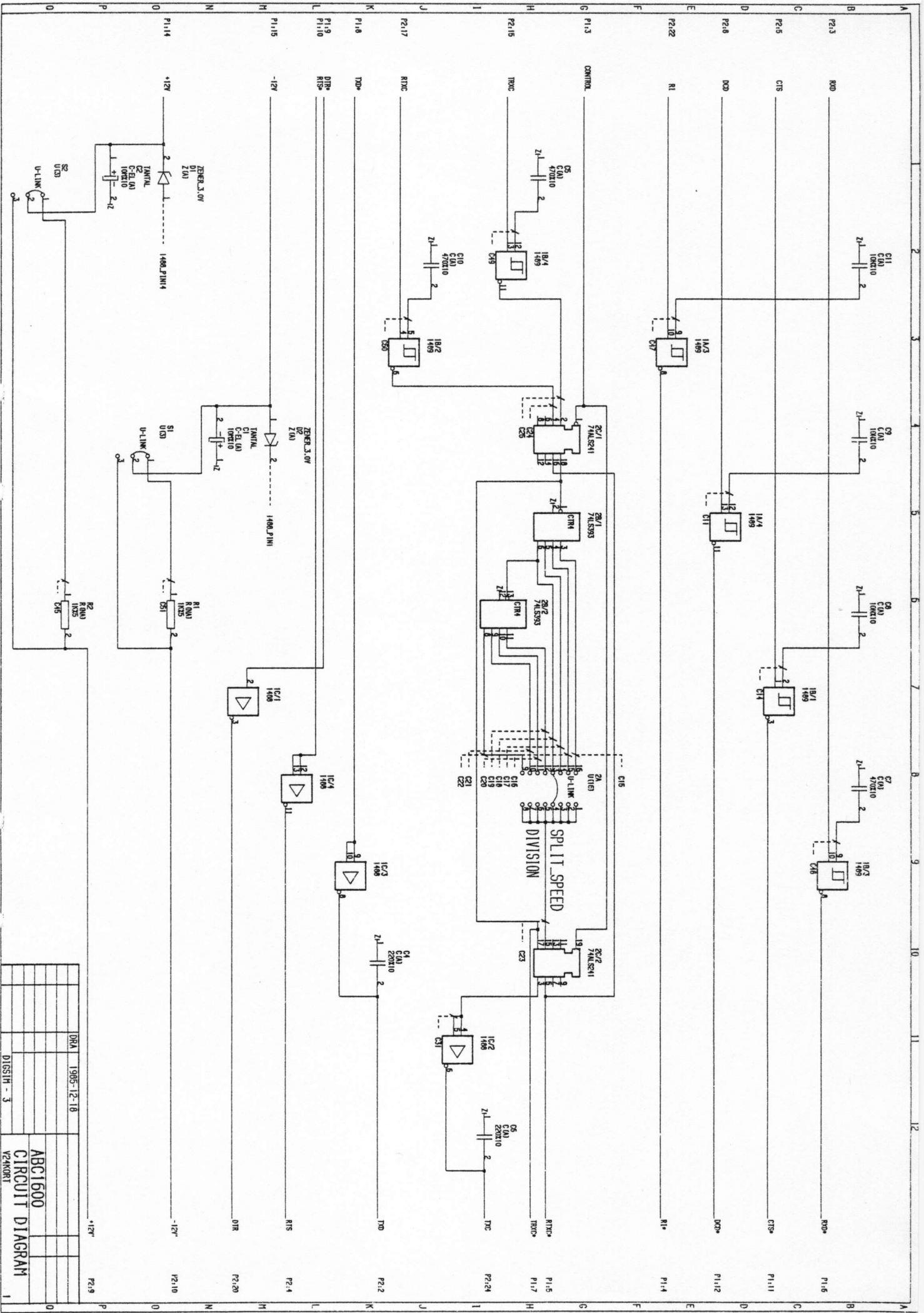
DKA	1985-12-18				
ABC1600 CIRCUIT DIAGRAM					
BUSSKORT					
DISINH - 3					
101					

Bus_1

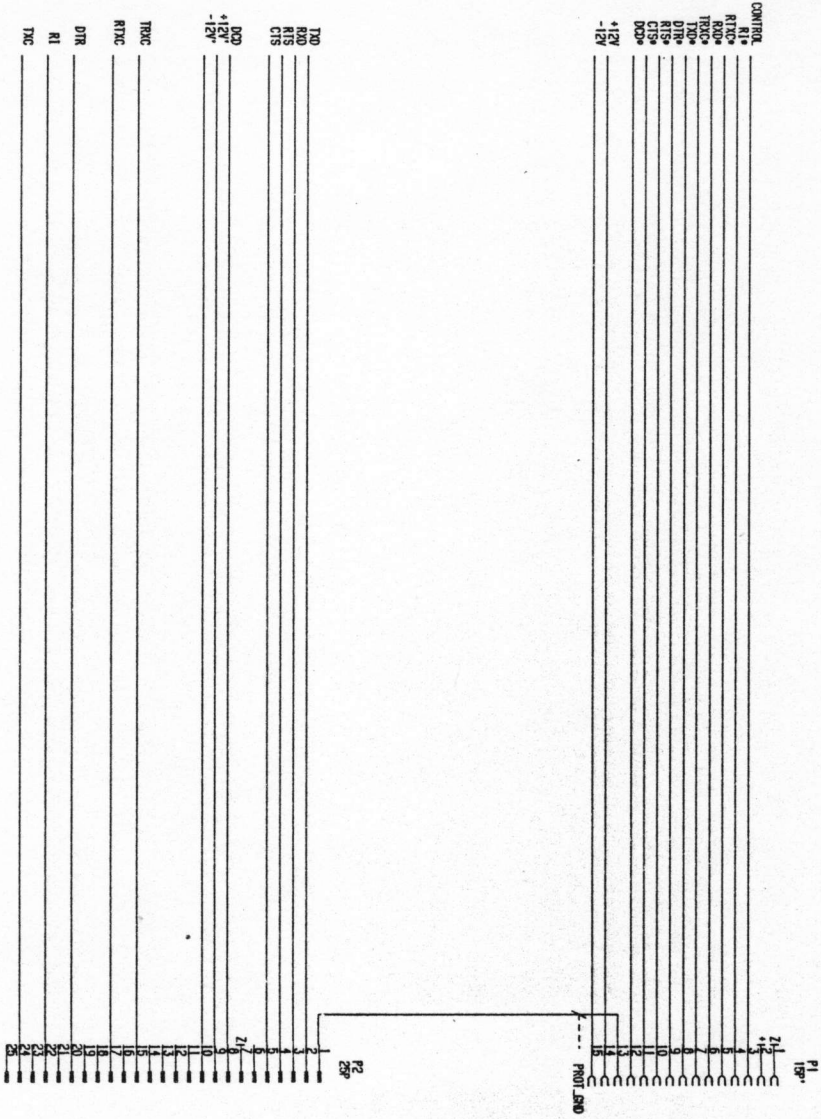


Bus_2

DRAW	1985-12-18	ABC1600
DISSEM - 3		CIRCUIT DIAGRAM
		BUSINORI
		102



DR4	1985-12-18	
ABC1600 CIRCUIT DIAGRAM		
V2AKORT		

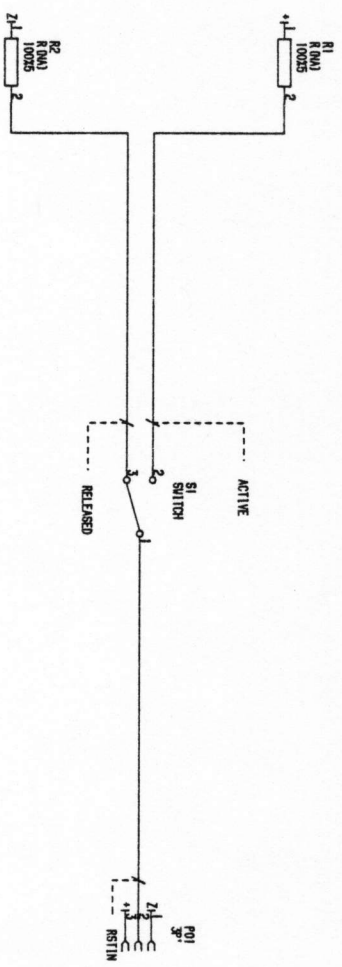


Processorkort

TTYXX

Dsub

DATA	1985-12-18				
DISINH - 3					
ABC1600 CIRCUIT DIAGRAM V2KORT1					
100					



DRAWN	1986-01-13	ABC1600
DIGSHT - 3		CIRCUIT DIAGRAM
		RESETKORT